Processors let PCs construct realistic 3-D graphics
The next standard.
A new generation of high performance SCCs.

Zilog's universal serial communication controller, the USC (ZI6C30N), provides higher throughput than any general purpose SCC. And it does it while reducing the CPU workload 60%.

More speed.
The USC is four times faster than any general purpose SCC. You get guaranteed data rates of 10 Mbits/sec. But speed is not the only USC advantage.

More CPU power.
The USC requires less attention from the system CPU. That means more power for the system. The USC's lower overhead is due to easy initialization, auto-sequencing word transfers from deep FIFOs, fly-by DMA control, and reduced latency from an efficient, chained interrupt structure.

More flexibility.
You've got two completely independent channels, as well as multi-protocol capability. Because the USC has two BRGs per channel you can transmit and receive at two different bit rates. And the USC's universal bus interface means you can cut the cost of GLU logic and expensive board real estate.

More performance.
CMOS and Superintegration bring more CPU power and higher data throughput. The USC carries a 12.5 MByte/sec bus bandwidth punch. Straight DMA connect and 32-byte FIFOs make the USC's systems simple, elegant and fast. Very fast.

More reliability.
With the USC you get Zilog's proven quality and reliability. Unique built-in testability features allow access to nodes and registers for testing program functionality in real time. Find out more about the USC or any of Zilog's growing family of Superintegration products. Contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.
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But that's not all. Ciprico has respondability. We have the largest staff of customer support engineers in the industry to help you resolve any integration problems. Plus software drivers for all major operating systems.

Our SCSI adapters are all based on an 80186 microprocessor, providing a command queuing, pass-through SCSI command software interface. Each board supports SCSI disconnect/reconnect and asynchronous and synchronous transfer rates of 2MB/s and 5MB/s respectively. And a floppy port is optional for cost effective system design.

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UNCONDITIONALLY STABLE regardless of load

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RUGGED operates from -55 to +85° C, withstands shock and vibration, ground equipment

COMPACT only 3.75 by 1.8 by 2.6 in.

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Tiny SPDT switches

absorptive... reflective

dc to 4.6GHz from $32.95

Tough enough to pass stringent MIL-STD-883 tests, usable from dc to 6GHz and smaller than most RF switches, Mini-Circuits' hermetically-sealed (reflective) KSW-2-46 and (absorptive) KSWA-2-46 offer a new, unexplored horizon of applications. Unlike pin diode switches that become ineffective below 1MHz, these GaAs switches can operate down to dc with control voltage as low as -5V, at a blinding 2ns switching speed.

Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

Connector versions, packaged in a 1.25 x 1.25 x 0.75 in. metal case, contain five SMA connectors, including one at each control port to maintain 3ns switching speed.

**SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Pin Model</th>
<th>KSW-2-46</th>
<th>KSWA-2-46</th>
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</thead>
<tbody>
<tr>
<td>Connector Version</td>
<td>ZFSW-2-46</td>
<td>ZFSWA-2-46</td>
</tr>
</tbody>
</table>

**FREQ. RANGE**
- dc-4.6GHz
- dc-200MHz
- 200-1000MHz
- 1-4.6GHz

**INSERT LOSS (dB)**
- typ max
- typ max
- typ max
- typ max

**ISOLATION (dB)**
- typ min
- typ min
- typ min
- typ min

**VSWR (typ)**
- ON
- OFF
- 1.3:1
- 1.3

**SW SPEED (nsec)**
- rise or fall time
- 2(typ)
- 3(typ)

**MAX RF INPUT (6dBm)**
- up to 500MHz
- +17
- +17
- above 500MHz
- +27
- +27

**CONTROL VOLT.**
- -8V on, OV off
- -8V on, OV off

**OPER/STOR TEMP.**
- -55° to +125°C
- -55° to +125°C

**PRICE**
- (10-24)
- $32.95
- $46.95
- $89.95
- $79.95

C 117 REV. E
On the cover: With any one of three recently introduced processors, you can give your PC's graphics an added dimension. See pg 96.
This cover art was produced by Diane Molina and Ben Deiman of Bendi Photographic Design on equipment from Austin Business Computers Inc. The image was created on an IBM PC AT-compatible computer containing a 34010-based Truevision ATVista videographics card. The image started with 35-mm color slides of the ATVista card and the TI34020 graphics processor. It was then digitized with a Howtek slide scanner. Extrusions of the chips were made to look like buildings with TOPAS software from AT&T Graphics Software Labs. The designer used Truevision Vista TIPS to create the textures. This photograph was provided courtesy Texas Instruments.

SPECIAL REPORT

Processors for 3-D graphics

Because of their enormous appetite for floating-point operations, 3-D graphics displays were previously limited to high-end workstations. With some powerful new processors, however, you can now bring workstation-quality 3-D graphics to such applications as PC add-in boards and embedded-graphics systems.—Margery S Conner, Regional Editor

DESIGN FEATURES

Electro/89

For three days in April, New York City will offer the electronics-engineering community much of interest in the form of Electro/89—eastern US’s largest design-electronics trade show and convention.—Richard A Quinnell, Regional Editor

Electro/89 Products

Designer’s guide to dynamic RAMs—Part 1

Although designers often prefer dynamic RAMs (DRAMs) to their static counterparts, they sometimes shy away from using DRAMs because of the devices’ added complexity. This article, part 1 of a 4-part DRAM series, sheds light on some of the complex issues surrounding DRAMs and describes the different DRAM architectures. The succeeding articles will cover memory-system architectures, DRAM controllers, and DRAM-board design.—Steve Gunn and Carl T Dreher, Texas Instruments

Antialiasing filters reduce errors in A/D converters

The need for effective antialiasing filters closely matches the growing number of applications for A/D converters. These filters reduce converter errors by limiting the input signal bandwidth. To correctly specify the filter, you need to consider the appropriate frequency band and the filter’s characteristics.—Robert W Steer Jr, Frequency Devices Inc

Continued on page 7
TIIE WESTCOR STAKPAK™. NEW GENERATION 250 TO 1200 W ATT SINGLE OR MULTIPLE OUTPUT OFF-LINE SWITCHER. 3.2 X 5.5 X 11.4 INCH CASE. FAN-COOLED.

Stack the odds in your favor by designing-in Westcor's 6 watt/cubic inch high power megahertz switcher. Capitalizing on patented and proven megahertz module technology and innovative thermal management techniques, the StakPak provides up to 1200 watts of power at 50°C with 1 to 8 isolated and fully regulated outputs.

For existing designs the StakPak's small size and low profile allow system enhancement without mechanical redesign. Simply replace your open frame switcher with up to 1200 watts of power at 50°C with 1 to 8 isolated and fully regulated outputs.

For existing designs replace your box switcher with 2 StakPaks and realize up twice the power without losing additional space. StakPak power factor correction provides 850 watts of output power from a standard 115 VAC wall outlet. In new designs, more space can be devoted to functionality or the system can be downsized.

The StakPak's 8 module output section can be factory configured in virtually an infinite number of voltage, current and power combinations. Special models providing between 250 to 1200 watts and outputs from 2 to 95 VDC are available.

Other features include outstanding electrical performance, UL, CSA, VDE safety agency approval (in process); variable speed fan option for low ambient noise environments and 3 phase or DC input options. Indeed, with unprecedented power density, versatility and new features, the StakPak redefines power packaging. Please contact Westcor for a data sheet, pricing and additional information.

STANDARD 1200 WATT STAKPAK MODELS
(110/220 VAC input)

<table>
<thead>
<tr>
<th>Model</th>
<th>Output Voltage (VDC) and Maximum Current (ampere) per Channel</th>
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<tr>
<td>SPl-180</td>
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<tr>
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<td>5 @ 120 15 @ 13 15 @ 13 5 @ 30 24 @ 8</td>
</tr>
</tbody>
</table>
TECHNOLOGY UPDATE

Logic synthesis prepares for VHDL 51

Logic synthesis tools are the latest in a long line of CAE tools that are destined to shrink the product development cycle for ICs and ultimately convert gate-level designers to systems engineers.—Michael C Markowitz, Associate Editor

RISC boards target real-time applications 69

Several manufacturers of CPU boards for real-time applications now offer powerful models based on RISC (reduced-instruction-set computer) µPs. You'll have to make the usual price/performance judgment before choosing a RISC-based board for a real-time application.—Maury Wright, Regional Editor

PRODUCT UPDATE

1M-transistor microprocessor 87

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April 1st Special Supplement 193
How much color control can be squeezed on to a single chip?
If the chip in question is the new IMSG300 Color Video Controller (CVC) from INMOS, the answer is quite simply, "all of it".

Through high integration, INMOS has combined total graphics control and data conversion onto a single 84 pin device. This includes a color look-up table, programmable video timing generator, full bitmap management, triple 8-bit video DACs and a phase-locked loop.

Because the IMSG300 is programmable, it is easily interfaced to any processor or monitor that may be used in your system. The G300 promotes the technique of using software drawing algorithms as opposed to designing them in hardware. This dramatically reduces design-in time and allows for easy upgradability.

The IMSG300 also provides an optional 24-bit pixel mode for full color as well as pseudo color, an on-chip phase-locked loop for generating all high frequency clocks, and a 32-bit multiplexed pixel port for achieving pixel rates up to 110MHz.

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Andreas Schreyer,
RISC Product Marketing Manager
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To help people integrate the 88000 into their VME systems easily, we invented the HYPERmodule—a miniaturized subsystem with one, two or four closely-coupled 88000s, cache memories, memory management and high-speed internal buses. Because all HYPER-modules have identical interfaces to the CPU board and identical programming models, you can plug in 17, 30 or 50 MIPS of RISC performance interchangeably. That's instantaneous scalability, with today's 20 MHz 88000. And when the 25 and 33 MHz versions arrive, you'll have up to 80 MIPS without rewriting a line of code. Scalability makes the future safe and sane for developers.

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The real strength of our 88000 boards and systems comes from our compatibility in the software environment. 68000 applications can simply be recompiled to run on our 88000 systems. We have the optimizing compilers and software development tools in place. And we've strongly supported the industry standards for both multi-user and real-time 88000 software. Our UNIX System 5, Release 3, is compliant with BCS (Binary Compatibility Standard), as well as SVID and POSIX. Our VMEexec is RTEID compatible. This industry-wide compatibility has led to massive porting activity by software vendors.

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Santa Ana, CA 92705-6500
Or call (714) 261-5300

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<table>
<thead>
<tr>
<th>Model</th>
<th>Bandwidth (MHz)</th>
<th>Sampling Rate S.S. (Ms/s)</th>
<th>Memory per Channel (kwords)</th>
<th>Vertical Resolution (bits)</th>
<th>FFT Spectral Analysis</th>
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<td>8^1</td>
<td>yes</td>
</tr>
</tbody>
</table>

^1 up to 12 bits with averaging
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NEWS BREAKS
EDITED BY JOANNE DE OLIVEIRA

DEVELOPMENT TOOL SIMPLIFIES CREATION OF USER INTERFACES

The Microware Systems Corp (Des Moines, IA, (515) 224-1929) Rave (Real-time Audio/Video Environment) software-development tool simplifies the design of human interfaces for real-time applications such as process-control systems. The development tool, an extension to the OS-9 real-time operating system, allows you to combine audio and video signals, computer-generated graphics, and customizable menus to create a user interface. Rave consists of three software packages. The File Manager ($300) and the Graphics Support Library ($175) handle run-time chores and include drivers that interact with system hardware. You use the Presentation Editor ($995) to create a user interface. All of the products will be available in May.—Maury Wright

INTERFACE UNIT LINKS SCSI AND IEEE-488 BUSES

If your computer or workstation provides a SCSI port, you may have thought that only peripherals such as disk and tape drives could take advantage of it. Now, however, you can use a SCSI port to control external data-acquisition systems, measuring instruments, and other devices that operate on the IEEE-488 bus. The SCSI488 interface unit from IOtech Inc (Cleveland, OH, (216) 439-4091) lets a SCSI port control as many as 14 IEEE-488 devices. Keep in mind that many computers and workstations provide only SCSI and RS-232C ports for communication with peripheral devices.

Because the interface is bidirectional, you can also use one IEEE-488 port to control as many as seven SCSI-based devices. Although the device's internal microprocessor controls the flow of information, it doesn't interfere with block-transfer operations, which can reach a speed of 800k bytes/sec. You can buy the SCSI488 for $795; it's available from stock.—Jon Titus

PROTOTYPING BOARD KITS INCLUDE A RISC-LIKE 32-BIT μP

Intel Corp (Dept 9P01, Santa Clara, CA, (800) 548-4725) now offers two kits that provide designers with a low-cost way to evaluate or prototype products based on the 20-MHz, 32-bit, 80960KB RISC-like processor from Intel. The kits include working CPU boards, schematics, programmable logic equations, and a software debug monitor. You can choose from kits with slightly different 80960KB-based boards. The EVQT960F20 kit costs $1960 and includes 128k bytes of zero-wait-state static RAM and 128k bytes of flash EPROM, which are installed on the CPU board. The board included in the $960 EVQT960E20 kit hosts 128k bytes of 2-wait-state static RAM and sockets for 128k bytes of EPROM. The CPU boards include an onboard prototyping area and a connector that you can use to add external circuits. Shipments will start by midyear.—Maury Wright

FAMILY OF 1- TO 10-MHz 12-BIT ADCs FEATURES LOW DISTORTION

Datel Inc (Mansfield, MA, (508) 339-5000) has announced a complete family of sampling A/D converters that operate at sampling rates of 1, 2, 5, and 10 MHz. The ADS-112 (1-MHz), ADS-132 (2-MHz), ADS-131 (5-MHz), and ADS-130 (10-MHz) converters offer excellent dynamic performance. At the Nyquist frequency, the total harmonic distortion is -73 dB for the 1-MHz and 2-MHz devices and -69 dB for the 5-MHz and 10-MHz devices. The number of effective bits at the Nyquist frequency is 11.0 for the two lower-frequency devices and 10.6 for the two higher-frequency devices.

EDN March 30, 1989
The ADCs, which also feature low noise and low nonlinearity specs, use a digitally corrected subranging architecture to achieve 12-bit resolution. The design of these converters includes an internal sample/hold circuit, on-chip references, a clock, 3-state outputs, and user-selectable output coding. Power dissipation ranges from 1.3W for the 1-MHz part to 4.9W for the 10-MHz device. Pricing for commercial units is $259 (24-pin ADS-112), $346 (32-pin ADS-132), $465 (40-pin ADS-131), and $549 (40-pin ADS-130). Delivery, from stock to four weeks.—Dave Pryce

**FULL-HEIGHT 5¼-IN. WINCHESTER STORES 764M BYTES**

The MK-358 Winchester disk drive from Toshiba (Irvine, CA, (714) 380-3000) offers an unformatted capacity of 764M bytes. The 8-platter drive dedicates one surface to servo control, but also relies on servo information embedded in each sector to ensure accurate tracking. The SCSI version of the drive costs $2645 (1000); the ESDI version is $2495 (1000). The SCSI version includes support for SCSI-2 features. Furthermore, the SCSI drive features an extensive command set that is stored on the drive and downloaded to RAM on power up. You can update the command set by downloading from a floppy disk. The company can easily implement custom command sets.—Maury Wright

**EVALUATION BOARDS AID IN RISC-µP DEVELOPMENT**

Two boards from Step Engineering (Sunnyvale, CA, (408) 733-7837) can assist you in developing systems based on the AMD (Sunnyvale, CA) 29000 RISC (reduced-instruction-set computer) processor. The $3445 Step PCEV (personal-computer evaluation vehicle) incorporates the µP along with 512k bytes of dual-ported video RAM, and plugs into the IBM PC/AT bus. The $1750 Step STEB (stand-alone target evaluation board) includes a 29000 µP, 512k bytes of RAM, two serial ports, and sockets for as much as 512k bytes of ROM. The company ships the board with a ROM-based debugging monitor called MON29K. Step also offers a line of software-development products for the 29000 µP; the PCEV and STEB boards give you a ready target for code developed with those tools.—Steven H Leibson

**RETARGETABLE CROSS-MACROASSEMBLER REDUCES TOOL PURCHASES**

If you're tired of buying yet another assembler every time you incorporate a new µP in one of your designs, or if you've been avoiding using a new µP because you don't have the software tools necessary to program it, the CASM retargetable cross-assembler from AnyWare Engineering (Boulder, CO, (303) 442-0556) can solve your problem. The $195 software package includes the cross-macroassembler, a linker, and a definition-file compiler. Definition files describe a particular µP's instruction set and assembly-language syntax by using a proprietary, procedural programming language. The language eases the task of molding the assembler to complex, pipelined architectures, such as those in RISC processors, and to wide instruction words, such as those used in digital signal processors. CASM also includes definition files for the 8085, Z80, 8041, 8048, 8051, 8096, 6805, 68HC11, 6502, and R2000 µPs and the NEC 7720 digital signal processor.—Steven H Leibson
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Phone: (408) 943-2666, Telex 821032 CYPRESS SNJUD, TWX 910-997-0753. © 1989, Cypress Semiconductor.
DECODER FACILITATES 2-CHIP TELETEXT SYSTEMS

The MV1815 single-chip CMOS teletext decoder and one dynamic RAM are all that you need to put together a complete teletext system. Adding extra memory allows you to store as many as 254 teletext pages. Manufactured by Plessey Semiconductors (Swindon, UK, TLX 449637; in the US: Scotts Valley, CA, (408) 438-8900), the decoder includes all level 1 teletext functions and many level 2 functions. In addition, it has an on-chip data slicer, two separate page-acquisition circuits, and RGB color-display logic. Its character sets support 13 languages, including most European and Scandinavian languages. Engineering samples of the MV1815 are available now. Production parts, which are expected to sell for around £5 (100,000), will be available during the third quarter of 1989.—Peter Harold

OPERATING SYSTEM ADDS FAULT TOLERANCE TO UNIX

Under an agreement between Integrated Micro Products (Consett, UK, TLX 537747; in the US: Santa Cruz, CA, (408) 429-1338) and Unisoft Corp (Emeryville, CA, (415) 420-6400), both companies will internationally market Integrated Micro Products’ new FT-Unix fault-tolerant operating system. Because the operating system’s fault tolerance is completely transparent, the system provides a standard Unix V.3 software environment in which you can run unmodified application programs. Together with suitable hardware, FT-Unix supports the synchronization of two CPUs, mirroring of data on separate disks, redundant I/O and communications operations, and isolation and reintegration of hardware modules to support diagnostic and servicing operations. It also supports the use of uninterruptible power supplies. FT-Unix licenses will be less than twice the price of standard Unix V.3, and both companies will promote its adoption as an open standard.—Peter Harold

SYSTEM TRANSLATES SPOKEN JAPANESE TO SPOKEN ENGLISH

Matsushita has reportedly developed a translation system that can convert spoken Japanese sentences to the corresponding English sentences in approximately 5 to 10 sec. Unlike conventional voice-translation systems, which recognize only registered voices and require the speakers to divide sentences into clauses, this machine accepts natural speech from arbitrary speakers. Conventional machines are also fairly large; this system is the size of a typical workstation. It comprises a sound-recognition device, a general-purpose (Sun-3) workstation, and a sound-composition device.

The system performs its translation by converting spoken Japanese to a series of alphabetical phoneme symbols and transmitting them to the workstation, where a translating program analyzes and comprehends the sentence, translates it into English, and formulates the English verbalization. To do so, the system uses the translation program developed by Professor Masaru Tomita of Carnegie-Mellon University. The system can translate about 3000 short Japanese sentences (of two to four clauses) after 50 words have been entered in the dictionary. In testing the system, the firm has achieved an 80% recognition figure; the company plans to improve the accuracy of recognition to the 85% to 90% level. It also expects to offer high-speed performance and eventually to offer translation from English to Japanese. In addition, Matsushita reportedly aims to produce the world’s first portable translation machine.—Joanne De Oliveira
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The popular myth goes something like this: "An LED, is an LED, is an LED." Or: "If you’ve seen one, you’ve seen them all." And of course: "LEDs? They’re commodity products."

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- over 100 models, immediate delivery
- meets MIL-STD-202
- rugged hermetically sealed package (0.4 x 0.8 x 0.4 in.)
- BNC, Type N, SMA available

LOW PASS

<table>
<thead>
<tr>
<th>Model</th>
<th>*LP-</th>
<th>10.7</th>
<th>21.4</th>
<th>30</th>
<th>50</th>
<th>70</th>
<th>100</th>
<th>150</th>
<th>200</th>
<th>300</th>
<th>450</th>
<th>550</th>
<th>600</th>
<th>700</th>
<th>850</th>
<th>1000</th>
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</thead>
<tbody>
<tr>
<td>Min. Pass Band (MHz) DC to</td>
<td>10.7</td>
<td>22</td>
<td>32</td>
<td>48</td>
<td>69</td>
<td>98</td>
<td>140</td>
<td>190</td>
<td>270</td>
<td>400</td>
<td>520</td>
<td>590</td>
<td>700</td>
<td>780</td>
<td>900</td>
<td></td>
</tr>
<tr>
<td>Max. 20dB Stop Frequency (MHz)</td>
<td>19</td>
<td>32</td>
<td>47</td>
<td>70</td>
<td>90</td>
<td>147</td>
<td>210</td>
<td>290</td>
<td>410</td>
<td>580</td>
<td>750</td>
<td>840</td>
<td>1000</td>
<td>1100</td>
<td>1340</td>
<td></td>
</tr>
</tbody>
</table>

Prices (ea.): Qty. (1-9) P $11.45, B $32.95, N $35.95, S $34.95

HIGH PASS

| Model | *HP- | 50   | 100  | 150  | 200  | 250  | 300  | 400  | 500  | 600  | 700  | 800  | 900  | 1000 |
|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| Start, max. Pass Band (MHz) | 41   | 90   | 133  | 185  | 225  | 290  | 395  | 500  | 600  | 700  | 780  | 910  | 1000 |
| End, min. | 200  | 400  | 600  | 800  | 1200 | 1600 | 1900 | 2500 | 2700 | 3000 | 3100 | 3300 | 3500 | 3700 | 4000 |
| Min. 20dB Stop Frequency (MHz) | 26   | 55   | 95   | 116  | 150  | 190  | 290  | 365  | 460  | 520  | 570  | 660  | 720  |     |     |

Prices (ea.): Qty. (1-9) P $14.95, B $36.95, N $39.95, S $38.95

*Prefix P for pins, B for BNC, N for Type N, S for SMA

example: PLP-10.7

CIRCLE NO 146

EDN March 30, 1989
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EDN March 30, 1989

CIRCLE NO 147
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<table>
<thead>
<tr>
<th>Model</th>
<th>Sampling Rate</th>
<th>Effective Bits at Nyquist Frequency</th>
<th>THD at Nyquist Frequency</th>
<th>Power Dissipation</th>
<th>Package</th>
<th>Price (1-9)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS-112</td>
<td>1MHz</td>
<td>11.0</td>
<td>-73 dB</td>
<td>1.3 watts</td>
<td>24-pin DDIP</td>
<td>$259</td>
</tr>
<tr>
<td>ADS-132</td>
<td>2MHz</td>
<td>11.0</td>
<td>-73 dB</td>
<td>2.9 watts</td>
<td>32-pin TDP</td>
<td>$346</td>
</tr>
<tr>
<td>ADS-131</td>
<td>5MHz</td>
<td>10.6</td>
<td>-69 dB</td>
<td>4.2 watts</td>
<td>40-pin TDP</td>
<td>$549</td>
</tr>
<tr>
<td>ADS-130</td>
<td>10MHz</td>
<td>10.6</td>
<td>-69 dB</td>
<td>4.5 watts</td>
<td>40-pin TDP</td>
<td>$775</td>
</tr>
</tbody>
</table>

* THD (Total Harmonic Distortion)
Don't confuse the DFT with the FFT

I found Tom Springer's article “Sliding FFT computes frequency spectra in real time” (September 29, 1988, pg 161) to be interesting and informative. The concept of a recursive algorithm for calculating a discrete Fourier transform (DFT) became particularly important to our research group about a year ago, and I published an internal technical note whose results were identical (and whose title was nearly identical) to Tom Springer's. There were, however, a few inaccuracies in Tom's article that may tend to confuse any reader working through the algorithm derivations.

In particular, the term “FFT” was used throughout the article as a generic label for the discrete Fourier transform. Although the FFT label could be used to describe any fast Fourier transform (that is, any transform algorithm using fewer calculations than the canonical DFT implementation), it has generally been associated with the fast algorithm produced by eliminating redundant calculations through a binary factoring principle. The recursive algorithm described in the article is nowhere derived or related to the FFT, but is a direct derivation from the definition of the DFT.

The derivation in the colored box at the bottom of pg 164 begins with the definition of the DFT, and not the FFT, as it states. In addition, the derivation makes no distinction between the time-series function \( x(n) \) and the frequency-domain function \( X(m) \). This problem is particularly confusing in the last and most important expression, where the frequency- and time-domain functions are mixed in the right-hand side of the equation.

Also, Fig 3 on pg 164 illustrates the \( X^{k+1}(m) \) frequency spectrum as being computed from an \( N+1 \) point time series beginning at \( k \) and ending with \( k+N \). The sequence should, of course, begin with \( k+1 \).

In addition to the caveats Tom mentioned, there are two others worth mentioning. First, because the computation is recursive, errors due to floating-point approximations will accumulate, the severity increasing with the size of the transform. Also, as with all DFT calculations, there is an implicitly applied windowing function. In the case of the sliding DFT, the windowing function is rectangular, with unity magnitude. The sliding DFT, as presented, will not accommodate other windowing functions.

Randall Johnson, 
Research and Technology Development 
De La Rue Printrak
Anaheim, CA

Some thoughts on American education

Richard Simonelli and Jorgen Vinding raise valid points [about engineering education] in their letters (Signals & Noise, EDN, September 29, 1988, pg 31). In his references to Hirsch and Ravitch and Finn, Jorgen Vinding shows more deep thought on the subject than the average engineer. The reference to Bloom will be appreciated by a large sample of educated Americans, who have read (at least in excerpts or interviews) about what the educational system has done to miseducate or de-educate students. Jorgen's recommendation that only 10 to 12% of a student's credits be in the humanities seems to me a bit low.

Ronald Khol makes the point (in Machine Design, October 20, 1988) that in Europe and Japan a degree from an American university is considered to be almost meaningless. He recommends that all students, regardless of their eventual fields of specialization, should have two...
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PC-resident analog-I/O cards

This is a short note to compliment your publication for including the excellent article "PC-resident analog-I/O cards," by contributing editor Bill Travis, in the September 15, 1988, issue of EDN (pg 150).

In addition to being very well written, the article was the most complete examination of the present status of this technology that I've seen anywhere in the past couple of years.

Bill should, in my opinion, receive some special recognition for doing such an exceptional job on this complex and timely subject. Thanks to all, and keep up the good work.

James Bischof
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CIRCLE NO 120

SIGNALS & NOISE

Oops
The Special Report on power MOSFETs and IGBTs appearing in EDN’s January 5, 1989, issue (pg 128) incorrectly listed Powertec Inc (Chatsworth, CA) as a supplier of those products. The company does not make MOSFETs or IGBTs; it manufactures power supplies only.

Address update
“EDN’s 15th Annual µP/µC Chip Directory,” which appeared in the October 27, 1988, issue (pg 164) included an incorrect address for Fujitsu Microelectronics Inc. The correct address, phone number, and FAX number are:

Fujitsu Microelectronics Inc
Advanced Products Div
50 Rio Robles, Bldg 3
San Jose, CA 95134
Phone (408) 922-9000
FAX 408-432-9070

YOUR TURN
EDN’s Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine’s articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.
0.4 micron/6ns SCRAMs

First of a New Generation of 3.3V Center-Pin Power and Ground Products.
Performance now offers two 6nS SCRAMs: P3C3148 1Kx4 and P3C3147 4Kx1. These SCRAMs are superfast Static CMOS Random Access Memories. Future superfast products, using center-pin power and ground with a 3.3 volt power supply, will include SCRAMs with 4Kbit to 256Kbit densities and popular logic parts such as buffers, transceivers, latches, flip-flops, comparators, registers and gate arrays.

"It has been clear for some time that the primary consideration which could limit the use of future generations of CMOS technology in the highest speed applications were issues associated with constraints that have been hangovers from bipolar TIL circuit implementations. If those constraints are not removed, then either performance will be compromised or serious application problems will result. It is easy to see the value of the changes that are needed to take maximum advantage of the attributes of the fine line CMOS technology in the sub half-micron regime (PACE III). Therefore, we have decided to invest a significant part of our Company's technical and marketing resources to help make the transition from a TIL environment to an optimized CMOS environment. As the 3.3 volt supply, low lead inductance product line emerges with 0.4 micron PACE III Technology, the uncompromised performance will overcome resistance to change and we will have a 'kinder & gentler' speed."

Tom Longo

4K Bit Density Static RAM Speeds

Performance’s PACE III Technology, which features 0.4 micron effective gate length, 0.75 micron line widths and 250ps gate delay, offers a 40 percent speed improvement even with a 35 percent voltage reduction. Superfast 6ns SCRAM performance is available now with significantly lower power dissipation.

Typical Address to Dataout Delay: 4Kx1 SCRAM

Performance’s superfast 3.3 volt products incorporate multiple center power and ground pins as well as reduced signal swings to dramatically reduce ground bounce and simplify signal interconnection issues such as reflections, cross talk and ringing.

For further information or to order SCRAMs call or write:

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CIRCLE NO 75
Tek's New ASIC Verification System.

[Image of a computer screen showing various parameters and signals with values like 5.5ns, 8ns, 0.0ns, 40ns, and signal names such as 'clk', 'en1', 'en2', 'q0', 's0', 's1', 'clr']
Big Tester
Performance At A Benchtop Price.

For a fraction of the price of large production testers, designers can now easily perform timing verification and margin analysis on their own ASICs, using a turnkey system with the critical timing of the million-dollar machines.

Tek's new LV 500 ASIC Verification System is a true designer's solution, integrated into a 50 MHz, 256-channel, 64K deep benchtop system with a test head just 17 inches square.

Using a simple menu structure and concepts familiar to the designer, the LV 500 combines elementary operation with astonishing performance, made possible by integrating all 256 bidirectional channels onto a single PCB.

Results include:

- **More accurate simulation**, even for complex synchronous devices. The LV 500 lets you vary cycle length and timing for each of 16 clock generators on a cycle-by-cycle basis.
- **Familiar operation** for example, template-based test cycles replicate the everyday timing diagrams of your IC book.
- **Graphic displays.** See clearly when devices are operating too close to parametric boundaries.

Thanks to its high degree of integration, the LV 500 rarely needs calibration. DUT fixtureing is simplified. And capacitance loading is reduced to about 25 pF, further contributing to the system's accurate results. And it is compatible with virtually all logic simulators.

**Don’t wait for chips to fail in production—or worse, for products to fail in the field.**

Start putting ASIC verification where it does the most good: in the hands of the designers themselves. For more information or a demonstration, contact your Tek sales representative. Or call 1-800-245-2036.
“What if I told you there’s a 15ns 64K SRAM available...
"I'd say you've been reading too many supermarket tabloids."

"Seriously! You get high speed and quantity delivery, plus the ability to drastically cut your qual costs!"

"OK, I'll bite. Who's got 'em?"

"Toshiba."

"Why didn't you just say that in the first place?"

While others continue to talk speed, Toshiba now delivers 15ns Static RAMs. The exceptional access speed of the new 15ns 64K SRAM family is the result of a little technological wizardry and lots of 1.0µ CMOS know-how. The bottom line is a 15ns 64K SRAM that dissipates less power and requires a smaller-size die than more costly BiCMOS devices.

And, if you've been looking for ways to cut qualification costs on your 64K SRAMS, look no further than Toshiba's 64K SRAM family. By using an aluminum master slice common to all configurations within the 64K family, the cost of qualifying individual parts is reduced by as much as 75%!

Toshiba builds a full line of SRAMS that offer high speed and fully static operation. A line whose depth and breadth provides higher system performance and lower system costs when designing high-speed cache memories, high-speed main memories, high-speed buffers and writeable control stores for minis, superminis, workstations, RISC-based systems, real-time processors, high-speed storage and high-end graphics applications.

When it comes to SRAMS, Toshiba's got all the speeds, configurations and densities you need. Including 256K, coming soon.

And plenty of packaging options, too. From JEDEC standard Skinny DIPs and SOJs to ZIP Modules.

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For circuit breaker choice that's recognized throughout the world, Airpax has the answer. Our SNAPAK® circuit breakers are available with rocker, toggle, paddle, baton, push-pull or push-to-reset actuation. They offer you a wide choice of reliable, magnetic circuit protection to provide precisely the right style, configuration and rating for your designs.

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See us at ELECTRO '89 Booth number 2039
NOTES FOR ANALOG SYSTEMS DESIGNERS

New price performance level attained with algorithmic 12-bit + sign A/D converters.

Micro Linear now has two 12-bit + sign A/D algorithmic converters that incorporate auto-zeroing circuitry and self-calibration; the ML2230, and the ML2233. This approach has no trimming and less circuitry, resulting in a lower price and an A/D converter that maintains accuracy over time.

Priced at $15.95 in 100 unit quantities, both the standard 24-pin DIP ML2230, and the 28-pin DIP ML2233, include an internal sample-and-hold and an easy to use microprocessor interface.

Accuracy and Speed
Total conversion time is 31 microseconds, including the on-chip sample-and-hold acquisition time. Both devices can digitize a -2.5V to +2.5V sine wave at 12 kHz with a 73 dB signal-to-noise ratio. Harmonic distortion is just 0.01%.

<table>
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<tr>
<th>ML2230C</th>
<th>ML2233C</th>
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<td>12-bit A/D price/performance comparison including sample-and-hold cost.</td>
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Versatility and Ease of Use
These 12-bit + sign A/D converters are designed for ease of use. The analog inputs can withstand 7V beyond the supplies. The high impedance analog input is differential for noise immunity and power supply rejection.

Call or Write for More Information
If your application calls for a 12-bit A/D converter or if you would like more information on Micro Linear's complete range of linear devices, please call (408) 433-5200 ext. 900 or write:
Micro Linear, Dept. TB, 2092 Concourse Drive, San Jose, CA 95131.
EDITORIAL

Farewell...

It never once occurred to me in the last 20 years that I would someday write a farewell letter to you, the good and loyal readers of EDN. I never considered working for another publication because I always thought EDN was the best, even in earlier years, when it wasn't. Now, it truly is the best publication in the electronics industry. It has the most professional and the most knowledgeable editorial staff, serves the most exciting industry in the world, and has the most loyal readers of all.

But there comes a time when we must move on to new opportunities and challenges, which is what I'm doing. Though I feel bittersweet at the thought of leaving EDN, I'm pleased to become publisher of Test & Measurement World—a magazine that serves the same exciting industry. I'm also pleased to continue my affiliation with Cahners Publishing. And making the transition that much easier is the fact that many of you are readers of Test & Measurement World. I am most fortunate indeed.

Together we've faced many changes these past 20 years, the most significant being the microprocessor. That single development revolutionized not only every aspect of the electronics industry (and your job), but also every industry worldwide.

We positioned EDN to help you understand how to use and exploit the benefits of that and every other significant technical development. I believe that we've served you well—and you tell me I'm right in readership survey after readership survey.

EDN will continue to serve you well under the leadership of both Peter Coley, a good friend and supportive publisher, and my successor, Jon Titus, who is an outstanding editor.

I thank my entire editorial staff for their loyalty, support, and professionalism. And I thank you for all the same reasons. I wish for all of you, staff and reader alike, the sentiments of an old Navy saying, “May you have fair winds and a following sea.”

Roy Forsberg
Vice President/Editorial Director

Jesse H Neal
Editorial Achievement Awards
American Society of Business Press Editors Award
If you believe EPLDs are constrained by their architecture, this should open your mind.
Introducing MAX. A totally new architecture that will change your thinking about EPLDs.

Still think that EPLDs can’t be fast and dense? Then prepare to erase and reprogram your thinking. The new MAX family from Altera has a radically different EPLD architecture that can make your fastest, densest designs fly out the door in no time.

With twice the speed and three times the density of conventional EPLDs.

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Finally, decoupled I/O that lets you use all your pins and flip-flops independently.

Tying it all together, a Programmable Interconnect Array (PIA) links MAX's multiple LABs efficiently.

When you combine the MAX architecture with a high speed, 0.8 micron CMOS process, you get high density devices with extraordinary performance.

And to get those devices to market faster, there’s MAX+PLUS™ Logic synthesis makes it the most powerful, easy to use software ever developed for EPLDs.

That’s why the MAX family is destined to become the new standard for logic design.

For more information, call Altera today: 1-800-545-3377.

And see how easy it is to change your thinking about EPLDs.

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Whether it's a question of speed, bandwidth, power consumption or cost, our family of 8-bit A/D flash converters has the answer.

For example, if you need a monolithic high speed, ECL-compatible converter, there's our AD770 or AD9002. The AD770 is our fastest ECL-compatible 8-bit converter, with a guaranteed sample rate of 200MSPS. And its 250MHz full power bandwidth and SNR performance with high frequency input signals can't be beaten. The AD770 is available in commercial and extended temperature range versions.

The AD9002 has a guaranteed sample rate of 125MSPS – yet its nominal power dissipation is a mere 750mW – and it operates from a single – 5.2V power supply. The AD9002 is also available with MIL-STD-883 processing, making it ideal for a wide range of applications.

On the other hand, if it's a TTL-compatible 8-bit flash converter you need, there's our AD9012 or AD9048. The AD9012 is the industry's fastest TTL-compatible converter, with a guaranteed sampling rate nearly twice that of its

---

### AD770

High Bandwidth, ECL Compatible, 200MSPS
- 400MHz Small-Signal Bandwidth
- 18pF Input Capacitance
- Bipolar or Unipolar Input
- +5V/-5.2V Power Supplies

The AD770 200MSPS A/D Converter uses an advanced VLSI bipolar process and a proprietary design to achieve new levels of performance in sampling rates and signal bandwidths for flash converters. Full power bandwidth is 250MHz.

The AD770 is ideal for high performance digital oscilloscope, radar, communications and electronic warfare systems. High input bandwidth permits undersampling of high frequency band-limited signals.

Multistage comparator design reduces the probability of errors due to metastable states or insufficient gain; decoding logic further reduces errors with a two-stage error-correcting architecture.

All inputs and outputs are ECL compatible, and analog inputs can be either bipolar or unipolar signals with up to 4V range. High accuracy and minimum temperature drift are preserved with end point reference Force and Sense connections.

There are three grades available. JD and KD grades are specified over a 0 to +70°C range; the SD grade is specified for temperatures from –55°C to +125°C. All standard grades are packaged in 40-pin ceramic DIPs; contact the factory for other package options.

---

### AD9002

Low Power, ECL Compatible, 125MSPS
- 160MHz Analog Input Bandwidth
- 17pF Input Capacitance
- 750mW Power Dissipation
- Single – 5.2V Power Supply

Designs for radar, digital oscilloscopes, ATE systems, electronic warfare, communications/signal intelligence systems and a wide variety of other applications can be made easier with the AD9002 High Speed Monolithic A/D Converter.

An overflow bit indicating overrange signals can also be used to "stack" two AD9002 units to get 9-bit resolution of the digitized signal.

Input capacitance is typically 17pF and only 22pF maximum, simplifying the choice of a driving amplifier. Cooling requirements and power supply problems are also eased because of the low 750mW dissipation of the AD9002.

Two grades are available; one has 0.5LSB linearity, and the other has 0.75LSB linearity. Both versions are offered for operation from –25°C to +85°C packaged as 28-pin DIPs or 28-pin PLCCs. Military temperature range devices of –55°C to +125°C are available as ceramic DIP and PLCC packages; they are compliant to MIL-STD-883 requirements.

---

FOR THE WHOLE STORY DO SOME SP

CIRCLE NO 126
nearest competitor. Plus the AD9012 offers excellent ac performance, low power operation and low input capacitance.

The AD9048 is an improved version of an industry-standard 8-bit TTL-compatible A/D converter, with the highest sampling rate, widest bandwidth, lowest input capacitance and lowest power. And the AD9048, as well as the AD9012, is available to MIL-STD-883.

There's no question about it—high performance characteristics are traits in our family of 8-bit A/D flash converters. So no matter what your requirement is for 8-bit analog-to-digital conversion, we have the solution.

If you want more information in a flash on our 8-bit flash converters, call your nearest Analog Devices sales office or our applications engineers. Answers for the AD770 are at (617) 935-5565. For the AD9002, AD9012 and AD9048, call (919) 668-9511.

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; Headquarters: (617) 329-4700; California: (714) 641-0839; (619) 268-4621, 1409/508-2037; Colorado: (720) 590-9992; Maryland: (301) 992-3994; Ohio: (614) 784-8796; Pennsylvania: (215) 482-7792; Texas: (214) 231-0984; Washington: (206) 575-4344; Austria: (222) 885504; Belgium: (3) 237-1672; Denmark: (2) 845-800; France: (1) 66-74-34-11; Holland: (31) 650-1; Israel: (9) 463-8383; Italy: (2) 486-3831; Japan: (0) 263-68; Sweden: (8) 282-74; Switzerland: (22) 31-57-69; United Kingdom: (932) 232-222; West Germany: (932) 233-9990.

8-Bit Flash Converters

**TTL COMPATIBLE**

**AD9012**
- Low Power, Wide Bandwidth, TTL Compatible, 75MSPS
  - 160MHz Input Bandwidth
  - 16pF Typical Input Capacitance
  - Power Dissipation: 1W
  - Minimum 46dB SNR

The AD9012 is a TTL compatible A/D converter fabricated in an advanced bipolar process which makes it possible to operate at typical conversion speeds up to 100MSPS.

For commercial and industrial applications, the AD9012 is an excellent choice for professional video, instrumentation, digital radio and PC-based video digitizing equipment.

In military applications, the requirement for mil-qualified devices can be met with MIL-STD-883 units in electronic countermeasures, missile guidance, radar, radar warning and other military systems equipment.

The AD9012 is available in two grades: one has 0.5LSB linearity, and the other has 0.75LSB linearity. Both operate from −25°C to +85°C and are packaged as 28-pin DIPs or 28-pin PLCCs. Military temperature range devices of −55°C to +125°C are available as ceramic DIP and LCC packages.

**AD9048**
- Low Power, Low Cost, TTL Compatible, 35MSPS
  - 15MHz Typical Bandwidth
  - Input Capacitance Typically 16pF
  - 550mW Power Dissipation
  - Industry-Standard Pinouts

As its name implies, the monolithic AD9048 Video A/D Converter is an ideal choice for real-time conversion of video signals. Its full power bandwidth is typically 15MHz, with no missing codes, and is a guaranteed minimum of 10MHz.

Low power dissipation of 550mW typical makes the AD9048 adaptable and attractive for a broad range of applications. In addition to professional video systems and video imaging, it is an excellent choice for electro-optics, digital radio and electronic warfare systems, among others.

The AD9048 has industry-standard pinouts and is available over two temperature ranges, with two grades of linearity. Linearities of either 0.5LSB or 0.75LSB can be ordered for 0 to +70°C commercial ranges, or −55°C to +125°C military temperatures. Commercial versions are in 28-pin DIPs and PLCCs; military versions are in ceramic DIP and LCC packages. Both commercial units and MIL-STD-883-compliant devices are standard products.

ON FLASH CONVERTERS EED READING.

CIRCLE NO 127
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Low power is different. The design requirements for a low-power compact switcher are as unique as your own product needs. Toko's 30+ years of experience in magnetics and filtering technology have led to development of switchers that pack the most clean reliable power into your available space.

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Ask about our Free Sample Evaluation Program. For a free power supply guide and to discuss your own low-power needs, contact Toko America, Headquarters and Midwest Branch (312) 297-0070; East Coast Branch (203) 748-6874; Southeast Branch (205) 830-0952; West Coast Branch (408) 432-8281.

Your strategic partner... for all the right reasons.
Although logic-synthesis tools offer greater efficiency to system designers, the current generation still suffers from a lack of compatibility with other CAE packages.

Michael C Markowitz, Associate Editor

Logic synthesis prepares for VHDL

Logic synthesis tools are the latest in a long line of CAE tools that are destined to shrink the product development cycle for ICs and ultimately convert gate-level designers to systems engineers. These tools have the ability to increase your design productivity while minimizing the risks of introducing design faults. But despite the efficiency gains, danger still lurks: Logic-synthesis software is still new, and the CAE industry is undergoing a radical transformation—thanks to the Very-high-speed-integrated-circuit (VHSIC) Hardware Description Language (VHDL).

The increasing complexity of the current generation of PLD and IC designs has stretched the capabilities of the engineers who create them. The difficulty of effectively trading-off such considerations as performance and packaging while still trying to meet delivery deadlines prompted the development of logic-synthesis software. The software translates and optimizes a design far faster than you could manually.

One way you can utilize this time savings is to simulate and test the design more extensively. If you had more time you could run system simulations that would let you improve on the oft-quoted statistic that 50% of ASICs fail to perform in their target system. You might also play "what if..." games to evaluate performance-area tradeoffs; most of the synthesis packages have options that let you limit parameters like gate count and critical-path speed.

There are two major obstacles to the widespread acceptance of logic synthesis. One hurdle is the confusion over what logic synthesis is and what it can do; the second is a lack of standardization.

At the most basic level, logic synthesis maps Boolean equations to a gate-level representation of your design. A broader definition stretches the input medium to include high-level circuit descriptions, like register-transfer-level (RTL) descriptions and hardware-description language (HDL) implementations. Further, the broader definition of synthesis encompasses two separate operations—translation of the behavioral circuit description to a structural implementation and, subsequently, optimi-

EDN March 30, 1989
Captured waveforms can be magnified up to 100 times at trigger point

Time measurements between cursors

Type of Interpolation

Captured waveforms

Reference memory 1, voltage range and time base settings

CH-1, voltage range setting

Reference memory 2, voltage range and time base settings

CH-2, voltage range setting

Main time base setting

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FOR PROFESSIONALS WHO KNOW THE DIFFERENCE
Logic synthesis

zation of the structure to eliminate redundancy and inefficiency. Optimization is where you can design for high speed, low real-estate utilization, or some combination of the two. Trading off these considerations is the part of logic synthesis where engineers can obtain their highest level of productivity enhancement today.

To help visualize the design process and where logic synthesis fits into it, refer to the “Y” chart model (Fig 1) adapted from the original suggested by Gajski and Kuhn (Ref 1). This model proposes three ways to represent a design. More complex designs can use all three representations at various times in their development. But you might design exclusively at the gate level for smaller integrated circuits or at the polygon level for discrete transistors.

The behavioral domain is the highest and most theoretical level at which you can represent a design. At this level, you are solely concerned with the function of the circuit from input to output. At the most abstract level, you can specify a design as a behavioral system. Refinement makes this specification more detailed as an algorithm; an RTL description; a set of Boolean equations; and, ultimately, as a set of differential equations. All of these representations define outputs as some function of the inputs and, possibly, time.

The structural domain specifies what elements you use to convert inputs into outputs and how you connect these elements to work toward their goal. Paralleling the refinement of the behavioral domain, the structural domain can be as abstract as a structural system. Providing more detail lets you define your circuit as a group of subsystems, which can include CPUs and memories. You could then refine your subsystems as modules, such as ALUs and registers. The modules can be further specified as gates and flip-flops; the gates and flip-flops can then be specified as transistors.

A series of concentric circles connect each of the levels of detail. The circles represent, at the most philosophical level, an architectural description of the design. Refining the design produces the algorithmic, functional-block, logic, and circuit descriptions.

In the jargon of the industry, logic synthesis at its simplest is strictly the translation from one level of detail in the behavioral domain to the same level of detail in the structural domain. Broadening the view a little, some vendors of synthesis tools include optimization in their definition of logic synthesis. These routines eliminate redundancies and inefficiencies that the synthesis software creates. At the most extreme end, some vendors insist that true logic synthesis encompasses translation, optimization, and refinement. Thus— independent of what you put in—you ultimately finish logic synthesis with either a transistor- or gate-level representation of your circuit. As
TECHNOLOGY UPDATE

Logic synthesis

a result of the vendor-dependent definition of logic synthesis, it is critical that you query logic-synthesis vendors to discover their particular definition.

The other major obstacle to logic synthesis—the lack of standardization—is shared by almost all CAE packages. Engineers and their organizations are reluctant to commit to yet another tool and devote the resources necessary to integrate that tool into their operation when the input and output data formats are incompatible with the tools they are already using. The investment and risk of still another translator, not to mention the learning required to utilize a new tool, has restricted the incorporation of logic synthesis as it has worked against the widespread acceptance of CAE tools in general. But as discussed in the previous issue of EDN (Ref 2), VHDL is beginning to dismantle these standardization stumbling blocks.

With the emergence of VHDL as a standard for the documentation and design of integrated circuits and systems, CAE tools will become more attractive to the legions of designers who have postponed jumping aboard the CAE bandwagon for fear of either being left with a dinosaur or committing to the wrong standard. Most logic synthesis vendors and, indeed, most CAE vendors are coming to the realization that VHDL is the biggest game in town and are making major efforts to enable their software to accept VHDL input and generate VHDL output.

Initially, VHDL will be primarily a documentation and transfer language, hence the necessity for front-end design tools that can create and output VHDL code from some other input format. The reluctance of designers to embrace new techniques over their well-worn, time-proven methods will impede VHDL's rate of acceptance. Additionally, if you are immersed in a design project, you have little time to spend learning a new way to design—essentially by writing code—and if you are between designs and have more time, you might not have the motivation to learn a new design technique. Call it a Catch-22. But once the benefits become clearer and the reluctance to write code rather than draw or capture
Experience makes the difference

Raytheon's experience gives you the winning ECL combination

Raytheon's ECL array family performs at a fraction of the power of competing ECL technologies. Proven ECL logic arrays are denser than 1.5 micron CMOS arrays.

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  CGA 40E12: 7,752 equivalent gates
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- **Ease of design:** Raytheon's contiguous row array topology provides a superior design approach when compared to fixed position cell-based technologies. This topology offers greater flexibility and ease in macrocell design, placement and routing.

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EDN March 30, 1989  CIRCLE NO 130
Logic synthesis

a design dissipates, VHDL will gather steam as a design language. In the meantime, the decision to use logic-synthesis tools depends largely on your circumstances. If you design a large number of complex circuits, then the productivity enhancements offered by the current generation of logic-synthesis packages would probably outweigh the instability of the CAE marketplace and future enhancements to logic-synthesis tools. If you don’t design circuits that could ultimately make their way into Department of Defense (DoD) systems, many of these logic-synthesis tools would probably serve your purposes quite well. On the other hand, if you only do a few designs, or are under DoD mandate to use VHDL either for design or documentation, then you might want to wait for the VHDL dust to settle before jumping into logic synthesis.

If you decide that you must have logic-synthesis capability or just want to know what’s available, you should know that some vendors target their logic-synthesis software to either PLDs or ASICs because of the different requirements of each technology. Some of the PLD-specific synthesis vendors have made a commitment to VHDL; others are still waiting to see how the dust settles. Minc’s PLDesigner will have a provision for VHDL input in the third quarter of this year. Altera is targeting a fourth-quarter introduction of VHDL capability for its PLDS-MAX software. The company is planning to add some extensions that its software will accept to the VHDL-language inputs to give you greater flexibility in creating your design. PLDS-MAX will output your circuit in standard VHDL format without the extensions, so you can exchange data with other VHDL-compatible tools. OrCAD is developing a VHDL compiler for its OrCAD/PLD that will let you program PLDs from a VHDL behavioral circuit description.

PLDesigner, PLDS-MAX, and OrCAD/PLD create JEDEC (Joint Electron Devices Engineering Committee) standard file outputs for programming PLDs. PLDS-MAX generates Altera’s ADF format netlist as well as a PLD pro-

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<td>ALTERA</td>
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<td>PLDSYNTHESIS</td>
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<td>VLSI TECH</td>
<td>LOGIC SYNTHESIZER</td>
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<td>1, 2, 3</td>
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<td>SUN, APOLLO, DEC, HP, ELXI, RIDGE</td>
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<td>XILINX</td>
<td>DS-23</td>
<td>N/A</td>
<td>P</td>
<td>1, 2, 3</td>
<td>LOCAL/GLOBAL</td>
<td>PC/AT, SUN, APOLLO</td>
<td>$1500</td>
</tr>
</tbody>
</table>

NOTES:
1=COMBINATORIAL LOGIC
2=SEQUENTIAL LOGIC
3=SYNCHRONOUS CIRCUITS
4=ASYNCHRONOUS CIRCUITS
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Ext. 153
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programming file for use with its hardware and PLDs. The PLDesigner provides its output in several useful formats, although Minc currently has no immediate plans for providing VHDL output. Minc's output formats include EDIF (electronic design interchange format) standard netlists, and schematics that are compatible with Mentor Graphics, Daisy/Cadnetix, OrCAD, PCAD, Futurenet-Data I/O, Teradyne, and Intergraph CAE systems. As with other front-end tools, until PLDesigner provides its own facility for generating VHDL descriptions, you'll need to use an indirect approach to generate a VHDL description. An example of such an approach would be importing your schematics to a schematics package that does have VHDL generation capability.

PLD-specific tools can begin the logic-synthesis process with Boolean equations, truth tables, or state-machine descriptions. Additionally, the PLDesigner can utilize RTL descriptions as well as synchronous-waveform entry, a method that lets you enter as many as 64 input and output waveforms. A waveform compiler then builds state-machine equations; and, if the waveforms do not provide sufficient information, the software provides you with the location of the problem and suggests solutions. Finally, if your design is too large, the PLDesigner can automatically partition your design among multiple PLDs, which it selects from its own library of more than 2500 devices, based on constraints like cost, pin count, and which devices your company stocks.

Logic cell arrays (LCA) are a cross between PLDs and ASICs. Xilinx's DS-23 Automated Design Implementation Program is an adaptation of Exemplar Logic's synthesis tools optimized for LCAs. It accepts either schematics that you've created with your favorite schematic-capture tool or Boolean equations. The DS-23 requires another front-end tool to create the circuit description from which the Xilinx software synthesizes and optimizes an LCA-compatible circuit. Thus, the company is relying on the capabilities of other front-end tools for VHDL compatibility.

Other vendors of logic-synthesis tools target the ASIC market. Most of these vendors recognize the importance of VHDL to their customers and are making progress toward providing their tools with the capability to both accept and generate VHDL descriptions. Logic-synthesis tools that accept circuit descriptions in other HDLs have an easier conversion path to VHDL than others. These HDLs include Gateway Design Automation's Verilog; Praxis' Ella, which was developed by the British Royal Signals and Radar Establishment (RSRE), adopted by the British Standards Institution (BSI), and licensed to Praxis; and other proprietary languages.

Silc Technologies SilcSyn ASIC Design System already provides VHDL output, and the company is committed to releasing a revision with VHDL-input support in September. The company wrote the original logic-synthesis software to accept their SilcSyn HDL and is modifying the tool for VHDL compatibility. As is common with all of the ASIC logic-synthesis tools, you can create your specification using either Boolean equations or truth tables.

SilcSyn has an optional $28,000 test-synthesis package that incorporates partial scan test into the design to implement testable ASICs. The software synthesizes the partial scan function after the circuit translation process but before the optimization routine is run, so that the software minimizes the scan logic with the rest of the design. The cost of the increased testability is four I/O pins and about 10% addi-
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Logic synthesis

tional real estate—a savings of between one-half and two-thirds that of full scan-path designs. After implementing the logic, the software creates Mentor's logfile-format test patterns.

NCR Microelectronics has integrated SilcSyn into their KE² (Knowledge-based Engineering Environment) package. The company expects to offer both VHDL support and the test synthesis feature in the second half of this year. If NCR is your ASIC supplier, its Design Synthesis package maps your circuit description directly to NCR library elements. Silc Technologies has additional cell libraries from Toshiba, LSI Logic, Fujitsu, and Standard Microsystems, and has a propriety library from GTE.

You can drive the Logic Consultant from Trimeter Technologies (which has reached an agreement to be acquired by Mentor Graphics) with Boolean equations, truth tables, schematics, or netlists. When Trimeter releases the Design Consultant in June, it will contain the Logic Consultant. The Logic Consultant will have the capability to utilize and generate VHDL descriptions as well as Verilog HDL descriptions. The software lets you exchange netlists and schematics with either Daisy or Mentor workstations or with other CAE toolsets utilizing EDIF. Another enhancement to the Design Consultant will be a graphic state-machine-diagram editor that lets you draw a state machine to use as the input to the logic-synthesis software.

Seattle Silicon and Silicon Compiler Systems have leveraged their experience in silicon compilers to present an approach that could ultimately fulfill the original promise of silicon compilation. That promise was to enable you to plug a high-level circuit specification into a black box and receive a fully fabricated, tested, and ready-to-use piece of silicon.

Neither Seattle Silicon’s Finesse nor Silicon Compiler Systems’ Logic Compiler currently support VHDL. However, both companies are committed to supporting the language and are developing enhancements that will bring VHDL capabilities to their tools. Finesse offers the ability to incorporate scan as a test strategy at the description level—currently you can use Boolean equations, truth tables, and state-machine descriptions to drive both Finesse and the Logic Compiler. The ability of these silicon compilers to size drive transistors automatically according to loading is a feature that provides more flexibility, better matching between circuit stages, and more efficient real-estate utilization than the typical standard-cell or gate-array alternatives.

Other vendors target their logic-synthesis tools to work with both PLDs and ASICs. Synopsys’ Design Compiler and HDL Compiler accept descriptions in many formats. In addition to Boolean equations and truth tables, you can use netlists in EDIF, LSI Logic’s NDL, Mentor’s MIF, Tegar format, or Cadence format as well as EDIF schematics or Verilog HDL to drive the Synopsys tools. The only HDL Synopsys currently supports is Verilog, but the company is committed to VHDL and plans to include VHDL support in a future release.

VLSI Technology’s Logic Synthesizer accepts input from Boolean equations and a state-machine high-level language. VLSI Technology is working to enable you to use truth tables, state diagrams, and PLA code files to drive its synthesis tools. The next release of the Logic Synthesizer will support the Ella HDL; the company’s goal is to offer VHDL-input support in the synthesizer’s third-quarter 1989 release. VLSI is planning VHDL output support, although it is unsure when that support will be available. The
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Logic Synthesizer is part of VLSI's multichip ASIC system-design package, which helps you partition your circuit according to size, power, and packaging requirements.

The Ascyn logic synthesizer, from Algorithmic Systems, has VHDL compatibility in development. The program supports Xilinx LCA's, gate arrays, and standard cells. Ascyn and Gates are the only two packages targeted for ASICs that run on the IBM PC/AT and compatibles, and Ascyn is the only package that runs on Apple's Macintosh family of personal computers.

Ikos Systems uses a simple logic-synthesis capability in its hardware-based Simulation System. Typically, if you find an error while you are simulating, you must exit the simulator, correct the circuit, recompile, re-enter the simulator, and resimulate. Because you must repeat this procedure every time you find a design error, simulation is often the bottleneck in design. With the Simulation System, you can enter Boolean equations, or netlist corrections interactively within the simulator shell. The Simulation System can perform local optimization; but, because it is strictly a simulator, it does not back annotate your logic changes to the original netlist. The simulator creates a file that documents your changes so you can update your netlist or schematic after you've finished simulating.

There is little question that logic synthesis is a powerful addition to the repertoire of system-design engineers. It can save you from entering schematics or netlists on a gate-by-gate basis. Many tools let you design using techniques that you're familiar with, like Boolean equations, truth tables, and state diagrams. Although you may not be comfortable working at the behavioral level, that's where the technology seems to be ultimately headed. Logic-synthesis tools are leading the way.

Standing in the way, however, are all the classic arguments against CAE tools: the lack of compatibility among hardware, software, and user interface. The cavalry, VHDL, is about to ride over the hill.

References


Article Interest Quotient (Circle One)
High 518 Medium 519 Low 520

For more information on the logic-synthesis products discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Algorithmic Systems
389 Pond St
Number C5
Braintree, MA 02184
(617) 849-0580
Circle No 700

Altera Corp
325 Monroe St
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Santa Clara, CA 95052-8163
(408) 884-0200
Circle No 701

Exemplar Logic Inc
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(415) 849-0937
Circle No 702

FutureNet-Data I/O Corp
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Redmond, WA 98073
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Circle No 706

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Circle No 715
A Multilayer Approach to Transient Voltage Suppression

Electrical overstress, especially due to electrostatic discharge (ESD), has been a growing concern to designers and the trend toward surface mount technology (SMT) has placed severe size constraints on the components that provide this protection.

Low voltage transient suppressor applications have been dominated by specially designed zener diodes because of their clamping characteristics and smaller size. However, continuing advances in ceramic technology have made the AVX TransGuard possible—a high performance, low voltage surface mountable varistor that, unlike single plane devices, uses a multilayer structure. This structure offers significant improvement in electrical performance as well as in size and usability in SMT assemblies. (Table I)

Clamping Characteristics

Multilayer construction and improved grain structure of TransGuards result in excellent transient clamping characteristics (in excess of 150 amps peak current) while maintaining very low leakage currents under DC operating conditions.

Energy Dissipation

Varistors or semiconducting ceramics are in reality series/parallel combinations of Schottky diodes that support most energy dissipation in thin depletion regions at each Schottky barrier. Zener diodes have only a single thin depletion region at the surface, while varistors have many in series/parallel combination distributed throughout the whole ceramic volume (as seen in Figure 1). This results in superior energy dissipation per unit volume.

Table I. Comparison of Surface MountTransient Suppressors

<table>
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<tr>
<th>Suppressor Type</th>
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<th>14V DC</th>
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<tr>
<td>TransGuard</td>
<td>Zener</td>
<td>TransGuard</td>
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<tr>
<td>Dimensions</td>
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<td>Clamping Voltage</td>
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<td>15.6V</td>
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<tr>
<td>$I_{PEAK}$</td>
<td>8 x 20µS, 10 Amp Peak</td>
<td>150A</td>
</tr>
<tr>
<td>$E_{TRAN}$</td>
<td>10 x 100µS Pulse</td>
<td>.4J</td>
</tr>
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</table>

Figure 1. Energy Dissipation for Zener Diodes and Transguards.

Zener Diode

Current Injection

Energy is Dissipated in the Thin (= 100nM) Depletion Region

Transguard

Current Injection

Energy is Dissipated in the Total Volume Between Electrodes

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RISC boards target real-time applications

Several manufacturers of CPU boards for real-time applications now offer powerful models based on RISC (reduced-instruction-set computer) µPs. You'll have to make the usual price/performance judgment before choosing a RISC-based board for a real-time application. But you also need to consider the relative performance merits of RISC technology and the effect that a RISC architecture will have on your software-development tasks and the auxiliary hardware that surrounds the CPU. Furthermore, all of the available RISC processors are relatively new and expensive, and you currently have few choices of real-time operating systems and software-development tools for these processors.

The RISC boards available for real-time applications are primarily based on the VME Bus. RISC-board manufacturers claim that their products offer a way to build more-powerful real-time systems than you can build with CISC (complex-instruction-set computer) boards. For one thing, the board vendors suggest that you can use a single-processor RISC board in a real-time application that might previously have required a tightly coupled multiprocessor design. Furthermore, the manufacturers assert that the real-time RISC offerings can also be used in multiprocessor configurations.

And finally, the board manufacturers spec their RISC boards' performance at 12 MIPS and higher, comparing that figure with CISC boards' performance of around 1 to 12 MIPS. Such a comparison isn't as straightforward as it may look, however: To implement a given task, you don't need to write as many instructions for a CISC as you do for a RISC.

Architectures seek an AIT of 1

RISC proponents, in general, claim that the technology offers a greater potential for performance than can be achieved with CISC architectures. RISC processors employ a relatively simple instruction set implemented without microcode. On average, available RISC processors can execute one

The 3-board VME Bus module from Motorola, Model MVME188, hosts eight 88200 cache/MMU ICs and as many as four 25-MHz 88100 processors. One board hosts the 88000-family chips, one is the system controller, and one carries 16M bytes of RAM.
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instruction per clock cycle—an AIT (average instruction time) of 1. System-dependent latencies, however, typically make it impossible to realize an AIT of 1 in a system. (For more information on RISC technology, see Ref 1).

When they compare RISC and CISC processors implemented at the same clock speed and in the same silicon technology, CISC advocates concede that CISC processors can't match the AIT performance of RISCs. But CISC proponents argue that a RISC processor must execute more instructions than a CISC processor must to accomplish the same task. The RISC side counters that compilers primarily use simple instructions and therefore closely match RISC-processor instruction sets.

In fact, a comparison of RISC and CISC performance is significant only in relation to a specific application. Despite all the industry chatter about RISC technology, it's not automatically your best choice. The right choice for your application will be based on your analysis of the available hardware and software products for both technologies, and not on marketing hype.

The RISC-vs-CISC debate will probably continue into the next decade. But one fact stands clear: The available RISC chips and boards are members of today's highest-performance class of 32-bit µPs and µP-based boards (some CISC chips and boards are also members of that class). The available RISC boards are also members of the highest-cost class—their prices range from $7000 to more than $35,000.

RISC requires fast memory

To use a RISC µP or board for a real-time application and to exploit the performance potential that RISC technology offers, you must accept and work with two characteristics of RISC technology. First, to develop software for RISC processors, you must employ high-level languages. Second, RISC processors require fast access to fairly large memory arrays.

The requirement to program in a high-level language derives from the nature of RISC architectures. Because of the instruction set and large register file, it's not feasible for you to write your own assembly-language code (as you could for CISC processors), even for small routines for which execution speed is critical.

Furthermore, RISC architectures enhance performance by implementing such features as delayed branch execution. By delaying the execution of branch instructions, a processor can avoid waiting for the next instruction to be loaded into the execution pipeline. Compilers take advantage of such architectural features by changing the sequence in which instructions execute.

Using a high-level language isn't always a drawback, as you might be tempted to think. Languages such as C and Ada have become increasingly popular for any (RISC or CISC) 32-bit real-time application. High-level languages simplify the software-development task and make it easier to manage the large amounts of code generated in 32-bit real-time applications.

Optimizers complicate debugging

High-level languages do complicate the debugging process, however. Today's RISC and CISC compilers can optionally generate code that's optimized for run-time efficiency. In optimizing the code, the compilers often shuffle the machine-code instructions, changing their sequence. Optimization is necessary to make any code run efficiently, whether on a RISC or a CISC processor, but it's more important for RISCs, because only optimized code will take full advantage of the unique architectural features of RISCs, such as delayed branch execution.

The source-code-level debugging packages available from most compiler vendors, however, operate only on unoptimized code. Therefore, you can't debug your code...
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when it’s running at full speed (optimized) at the source-code level.

Unix-type programmers (programmers who create software for non-real-time applications) probably don’t need to debug software after optimization. But in real-time applications, the code interacts directly with the real world via robots, instrumentation, motors, and other asynchronous I/O devices. If you used a source-level debugger on the unoptimized code, and then optimized the code, you might run into a problem. For example, a robot might perform actions in the wrong sequence because the compiler had shuffled the instructions.

In such a situation, you may need to debug the actual optimized code.

You can debug optimized code for CISC processors at the assembly-language level. However, because of the architectural features of RISC processors (such as delayed branching and large register sets) and the level of optimization that RISC compilers perform, it’s virtually impossible to debug assembly code for RISC processors. You simply can’t correlate the assembly code with the source code. (For more information on RISC compilers, see Ref 2.)

Source tools should improve

It’s a good bet that vendors of compilers and real-time operating systems will soon offer improved debugging tools. For now, however, if you must fix software glitches in real-time RISC applications, you may have to resort to the trial-and-error method.

Memory architecture holds the other key to exploiting the performance potential that RISC chips offer. The clock speeds of available RISC μPs currently range from 20 to 25 MHz, but in the next couple of years you can expect to see RISC μPs with clock rates approaching 50 MHz. To attain an AIT approaching 1, a RISC μP needs to fetch a new instruction, and perhaps even new data, every clock cycle. Architectural features such as delayed branch execution serve no purpose unless the memory can supply instructions and data to the processor without latency.

A dynamic-RAM (DRAM) system can’t accommodate a 20-MHz RISC μP with the required memory-access speed (at 1 instruction per clock cycle, that speed would be 50 nsec). Even schemes—such as interleaved memory—that satisfy pipelined CISC architectures fall short of the every-cycle-access needs of RISC processors. Fast CISC μPs also need faster access than DRAMs can provide, but memory latency has more of an impact on RISC performance than on CISC performance.

Cache latency varies

In general-purpose computer systems, designers implement static-RAM (SRAM) caches to provide the processors with fast memory access much of the time; the percentage of time is called the “hit rate.” However, when cache misses (instances when the required instruction or data is not present in the cache) occur, the processor suffers a latency period while a new line of data is added to the cache. The latency varies according to the μP and cache architecture, but it typically ranges from 5 to 20 clock cycles.

Real-time systems require what’s termed a “deterministic” response to asynchronous real-world events. Typically, a system responds to an event by generating an interrupt to a μP. The processor then invokes a routine to service the interrupt. Part of the system designer’s task is to ensure that the processor can respond to and service such an interrupt in a certain maximum amount of time: the worst-case response time. Historically, designers of real-time systems have avoided cache-based architectures because of the latency caused by cache misses. The latency would raise the worst-case response time significantly.

Before choosing a RISC architecture for a real-time application, you must consider the RISC board’s memory-system design. The available RISC processors each include...
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architectural features that may fit one memory scheme better than another. Each of the available boards uses a specific memory implementation, so when you buy a board, you're choosing a memory system. The board's memory architecture will play a large part in determining your system's worst-case response time.

Static RAM minimizes latency

For example, Mizar chose to employ static RAM for the entire RAM array on its SPARC-based MZ7170 board set. The 2-board VME Bus product includes 1M byte of static RAM and 4M bytes of EPROM. A 20-MHz version of the board costs $6995, and a 25-MHz version adds $500. You can also add a 20-MHz Texas Instruments 8847 FPU (floating-point unit) for $995.

Mizar currently offers the Wind River Systems (Emeryville, CA) VxWorks real-time operating system and software-development tools for the MZ7170, and plans to have other real-time packages available late this summer. The MZ7170 has no memory-management unit (MMU). Jerry Fiddler, president of Wind River Systems, believes that real-time systems can't afford the latency that a MMU can add during address translation. In fact, when porting its operating system to a board that includes a MMU, Wind River bypasses the MMU.

Software bypasses MMU

Harvey Goldman, vice president of marketing at Integrated Solutions, agrees with the no-MMU, no-cache philosophy for real-time applications. According to Goldman, the company has ported its UniWorks real-time operating system to boards that have caches or MMUs, but has bypassed the cache or MMU features.

Integrated Solutions currently offers the Advantedge 2000 Series. These products include a single-board computer based on a 16.67-MHz MIPS Computer Systems R2000 chip set. The board, which costs $10,000, does not support a bus such as the VME Bus. It's truly suited for applications such as workstations. The company does plan to make the UniWorks real-time operating system available for the board during the first half of the year, however. You can also expect the firm to introduce a follow-up VME Bus-based product that's more suitable for real-time applications.

In general, real-time systems employ multitasking operating systems and application software. A CPU board that doesn't contain an MMU requires you to develop each task of a set of software tasks for a single physical-address space. Therefore, the programmer must prevent different tasks from manipulating the same memory locations improperly. An MMU simplifies the programming tasks, but it may add latency in the form of address-translation time.

Burst mode speeds memory read

The Ironics IV-9001 board employs the AMD 29000 RISC processor, and the 29000 includes an on-chip MMU. The MMU performs translations in the instruction pipeline and eliminates latency concerns. Ironics also implemented a hybrid-cache-based memory architecture on the board. The 29000 µP employs a Harvard architecture
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with separate operand and instruction buses. The chip also includes circuitry to improve the performance of DRAM arrays. The µP can fetch operands and instructions in burst mode without issuing an address for each word fetched.

On the IV-9001, Ironies employs the burst-mode fetch feature and an interleaved array of static-column DRAMS to feed both the instruction and the operand buses of the 29000, each at speeds as high as 100M bytes/sec. In fact, the DRAM array can supply instructions to the CPU at a rate of one instruction per cycle; memory latencies are caused only by memory-refresh operations and dual-port conflicts with operand accesses.

The board also includes a 16k-byte direct-mapped operand cache that minimizes accesses to the dynamic RAM for fetching operands. A cache miss to the operand cache causes a worst-case latency of seven cycles. Ed Schulman, Ironies' vice president of marketing, points out that because of the fast clock speed of the 29000 µP, the actual worst-case latency caused by the cache is acceptable for most applications.

Daughter card hosts RAM

Ironies implemented the DRAM array on a daughter card for the VME Bus processor board; the company offers RAM cards with 2M to 16M bytes of memory. The IV-9001 costs $7995, and a 2M-byte RAM card adds $1995. Ironies also offer an SRAM daughter card in the future. The company offers the VRTX32 real-time kernel from Ready Systems (Palo Alto, CA) and the pSOS real-time kernel from Software Components Group (San Jose, CA) for the RISC board.

If you consider using a board based on the Motorola 88000 RISC processor, you may have to deal with an even more complex memory architecture. This RISC chip set includes the 88100 CPU IC and the 88200 CMMU (cache and MMU) IC. The 88100 employs a Harvard architecture, and it's typically accompanied by one to four 88200 CMMUs for both instruction and operand buses. According to Motorola, the 88100 can be used without any 88200 CMMUs, but no vendors currently offer such a board-level product.

Cache IC emulates static RAM

Motorola did, however, make some provisions in the CMMU IC for real-time applications. The 88200 includes a 4-way, set-associative, 16k-byte physical-address cache. You can program any or all of the four 4k-byte segments in an 88200 to act as fast static RAM rather than as cache memory. Therefore, you can permanently load speed-critical sections of code into the memory segments that are set up as static RAM. The MMU portion of the IC performs address translations and adds no latency during accesses to the on-chip memory locations.

An 88100 CPU chip supports as many as eight 88200 CMMU ICs (four for instructions and four for operands). Therefore, the architecture potentially supports a total of 128k bytes of fast memory for cache and SRAM use. Cache-read misses add a latency of seven cycles, and misses on writes add a 4-cycle latency. Misses, however, cause the transfer of four consecutive words of data (16 bytes), not just the single word that caused the cache miss.

Motorola currently offers two 88000-based VME Bus products. The MVME181 includes an 88100 CPU and two 88200 CMMUs. A 20MHz version of the board costs $8995, and a 25-MHz version costs $9995. The board includes 8M bytes of DRAM to feed the CMMUs. Motorola also offers the MVME188 3-board set, which comes in three versions. You can specify the board set with one, two, or four 88100 processors, and each of the versions includes eight 88200 CMMUs. The versions cost $22,950, $27,200, and $33,500 (100), respec-
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tively. One board of the set hosts the 88000-family chips, a second board serves as a system controller, and the third board carries 16M bytes of DRAM. A proprietary memory bus connects the boards.

ICs support multiprocessing

The 88000 architecture inherently supports multiprocessing. In fact, the CMMU IC includes a bus-watching feature, and the ICs maintain cache integrity in a multiprocessor configuration. Motorola offers its VMEexec real-time operating system with the boards. The operating system supports multiprocessing. Software Components Group also plans to offer pSOS for the 88000; the product will probably be available early in the second quarter of this year.

Force Computer and Tadpole Technology also offer boards based on the 88000 family. Tadpole’s VME Bus-based TP880V costs $10,995, and its Multibus-II-based TP880M costs $11,495. The Tadpole boards feature similar architectures, and they each include an 88100 processor and two 88200 CMMUs. The boards come with 4M bytes of DRAM and a 64k-byte SRAM array that the 88100 can access without latency. In addition, pSOS will be available for both boards in the second quarter.

The Force offering, the CPU-81, also includes a single 88100 and two 88200 CMMUs (Fig 1). The board costs $8900, has 4M bytes of DRAM, and includes sockets for as much as 4M bytes of ROM. Furthermore, Force offers a second board, the CPU-82, that mates to the CPU-81 via a 100M-byte/sec bus (Fig 2). The CPU-82 costs $9900 and carries an 88100, three 88200s, and 12M bytes of dynamic RAM.

Force labels the board set a “dyadic processor” and claims that the architecture eliminates all latency in computation-intensive applications. One of the three 88200 CMMUs on the CPU-82 is dedicated as an SRAM to store speed-critical sections of code. The CPU-81 and CPU-82 will be available around the middle of the year. The company plans to offer pSOS, VRTX32, and OS-9 from Microware (Des Moines, IA) as real-time operating-system options.

RISC prices are sky high

At present, cost may prove to be the ultimate key to how well a RISC board fits your application. To put it simply, the available RISC boards are very expensive. Memory prices are partly to blame for the high prices. But the newness and

---

**Fig 1**—A 4M-byte dynamic-RAM array and the 88000 chip set make up the CPU-81 board from Force Computers. The board also includes a 100M-byte/sec bus that can connect to a second processor and memory board (the CPU-82).
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Sparse availability of the chips has also driven RISC-board prices up. In fact, the price/performance ratio has kept some CPU-board vendors out of the RISC market. Heurikon Corp, for example, plans to stick with CISC-based products for the time being. Clarence Peckham, the firm's director of engineering, points out that Heurikon's HK32/V532 board, which is based on a 20-MHz National Semiconductor 32532 µP, offers performance comparable to that of RISC-based boards. Furthermore, with 4 M bytes of dynamic RAM, the HK32/V532 costs about $5000.

You can expect RISC chip prices to drop sharply in the next year, however. In particular, the price of SPARC processors should drop, because manufacturers are already producing the chips in volume for Sun workstations. Customers for SPARC chips are also likely to benefit because of the large number of semiconductor companies that manufacture or plan to manufacture the chips. Bipolar Integrated Technology, Cypress Semiconductor, Fujitsu Microelectronics, LSI Logic, and Texas Instruments have all licensed the SPARC technology.

The MIPS Computer Systems R2000 and R3000 chip sets will also be available from several vendors. Integrated Device Technology, LSI Logic, and Performance Semiconductor currently offer these chips. NEC Corp (Japan) and Siemens (West Germany) have recently licensed MIPS Computer Systems' RISC technology and plan to offer compatible processors in the future. Thus far, Motorola plans to remain the only source of the 88000.

Consortium promotes standards

A number of companies have banded together to form the 88open Consortium (Wilsonville, OR), a nonprofit group that is leading the effort to set open hardware and software standards for 88000 products. For example, the Consortium's real-time and embedded-systems committee is working to define a common BIOS for real-time systems. For information, contact John Barr, the committee chairman, at Motorola Computer X (a wholly owned subsidiary of Motorola). His phone number is (312) 576-8706.

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The company has taken great pains, however, to encourage all sections of the computer industry to use the 88000 family (see box, "Consortium promotes standards").

Your determination of whether to use RISC boards in your system application, as well as your choice of a particular RISC board, might well hinge on unquantifiable factors. Sure, you'll study the hardware and software available for RISC processors in making your decision, but you'll also be influenced by such factors as the industry momentum gathering behind a certain chip.

Ultimately, however, your decision between RISC and CISC boards will be reduced to two technical issues: You must decide whether you can tolerate programming in high-level languages and whether you can work with the complex memory architecture that RISC boards must have in order to be efficient. If you can, RISC boards are for you, if you can't, you should stick with CISC boards.

References


For more information...

For more information on the RISC boards discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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So, if you want a low-cost, high-quality, front-panel performer, just call IEE and ask the $64 question.
µP packs workstation power and graphics ability in 1M-transistor chip

The 80860 microprocessor, with more than 1,000,000 transistors, integrates a RISC core, a floating-point unit (FPU), a hardware shading unit, and an instruction and data cache. At 40 MHz, the chip achieves 80M flops and can sustain 500,000 4 × 4 matrix transformations/sec. In addition, the shading hardware can Gouraud-shade 50,000 100-pixel triangles/sec.

The chip comprises six basic units: the integer RISC core, the FPU, the graphics memory-management unit, the data and instruction caches, and the bus-control unit. The RISC core has a 32 × 32-bit integer register file. It decodes and executes load, store, integer, bit, and control-transfer instructions. It fetches floating-point as well as integer instructions and can operate in parallel with the FPU.

The FPU has a separate register file that you can configure as 8 × 128, 16 × 64, or 32 × 32 bits. Its separate adder and multiplier units both conform to IEEE STD 754. Both the adder and multiplier units can provide one result for every clock cycle. When pipelined, they operate at 2 results/clock cycle, yielding the 80M flops rate. The graphics unit, which provides Gouraud shading and z-buffering as well as clipping capability, is discussed in more detail in the Special Report on pg 96.

The memory-management unit can translate addresses from linear logical space to linear physical space for both instructions and data, although this translation is optional. The processor stores translated address information in a table and caches the table in a 64-entry, 4-way associative memory. The page tables are compatible with those of the 80386. These tables enable you to design a paged, virtual memory with user/supervisor protection, which is important in multitasking systems.

One-third of the chip’s area is dedicated to data and instruction caches. The caches’ aggregate bandwidth is 1G byte/sec, a speed not possible with off-chip caching. The instruction cache is a 2-way set-associative memory of 4k bytes, divided into 32-bit blocks. The 8k-byte data cache, which is a write-back cache, is also 2-way set-associative and divided into 32-bit blocks.

The bus-control unit works with conventional static-column dynamic RAM. A pin indicates whether the next address takes place using the same page. The unit supports both pipelined and nonpipelined operation. Pipelining allows a new 64-bit word to transfer every two cycles when the pipeline is full, even though the total number of cycles required for the transfer can number as many as six. Note that overall chip performance is often limited by the data-bus width. The 80860's 64-bit external and 128-bit internal buses lessen this possibility.

$750.—Margery Conner

Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (408) 987-8080.

Circle No 734
Hardware modeling system creates simulation models of your ASICs

The LM-1000 hardware modeling system addresses some of the problems associated with doing system-level simulations of designs involving semicustom ICs. It lets you create a logic model of an ASIC when you have prototypes available. After you mount a device on a device adapter, the modeling method lets you create a functional software shell, in which you define the pinouts; a verification utility automatically checks software syntax and semantics.

For standard devices, the LM-1000 hardware modeling system supports a library of over 600 logic models. Each includes a physical device mounted on a device adapter, shell software that defines I/O, and functional test vectors. Most of the models cost between $1000 and $2000.

Because the models utilize the actual physical device, they are by definition correct; as long as the shell software is correct, the model will perform as the actual device—because it is, essentially, the actual device. The shell also lets you control worst-case timing, including minimum, typical, and maximum delays. The pattern clock of the LM-1000 is continuously variable between 150 kHz to 25 MHz with a resolution of 1% and accuracy of ±0.5%. Timing resolution varies from 500 psec at 25 MHz to 50 nsec at 150 kHz; accuracy is ±3 nsec or ±1% of the pattern clock period, whichever is larger.

The LM-1000 currently supports, under OEM agreements, Verilog from Gateway, Hilo from GenRad, Validsim from Valid, the Vantage Spreadsheet from Vantage Analysis Systems, and Viewsim from Viewlogic, although the vendor claims the LM-1000 is simulator independent and can easily adapt the hardware modeling system for any simulator. Because only a simulator function interface and some user utilities reside on the host computer, you can drive the LM-1000 from a variety of computers, including the Sun-3 and Sun-4; Apollo Series 3000, 3500, 4000, and 4500; DEC VAXstation, MicroVAX and VAX; and IBM PC/386 and compatibles.

The base configuration for the hardware modeler allows for one 80-pin device. Through expansion, you can build the pin capacity to 2560 total pins organized as eight slots by four lanes. This organization gives you as many as 32 80-pin devices, 16 160-pin devices, 8 320-pin devices, or some combination thereof. The LM-1000 supports pattern memory from 128k patterns x 80 pins to 2M patterns x 320 pins—you can expand memory with 128k x 80- or 512k x 80-pin modules.

The LM-1000 starts at $50,000 for the minimum unit and is available through Gateway Design Automation, GenRad, Valid Logic Systems, Vantage Analysis, or Viewlogic.

—Michael C Markowitz
Logic Modeling Systems Inc, 1520 McCandless Dr, Milpitas, CA 95035. Phone (408) 954-5200.

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EDN March 30, 1989
At $1495, the GT200 is possibly the lowest-priced precision universal counter available. Its performance, however, is far from the lowest for IBM PC/XT-, PC/AT-based, or stand-alone counter/timers. This counter can measure frequencies with 10-digit resolution/sec of gate time, and you can make timing measurements to 100-psec resolution without averaging. If this is more resolution than you need, you can trade it for speed measuring 7 digits of frequency resolution in 1 msec. For example, you can resolve a 10-kHz signal to .001 Hz in 1 msec.

The instrument performs frequency, period, time-interval, delay-time-interval, ratio, totalize, gated-totalize, and pulse-width measurements; it can sustain operation at 2000 measurements/sec. This speed not only gives you the potential for higher system throughput, but also allows you to characterize dynamic signals.

For example, using this throughput you can quickly compute the drift rate and peak-to-peak jitter of a signal. Indeed, you can make multiple measurements and look at measurement statistics in the same amount of time you might need for single measurements on slower units. Because the counter's statistics software displays a running mean and standard deviation, and minimum and maximum count, you can see the sample results as they occur. This means that you don't need to wait for the instrument to finish taking all samples to see results.

The counter's two de-coupled input channels are specified for input frequencies of dc to 75 MHz and accept signals from -5 to +5V. To be sure you trigger on the correct signal, you can use auxiliary inputs to arm the trigger. The auxiliary inputs also let you perform gated counting.

Input impedance and trigger threshold levels are programmable. You can select an input impedance of 50Ω or 1 kΩ in parallel with 30 pF. The trigger threshold is programmable from -4.375 to 5V in 0.625V steps. You can also use an automatic trigger mode to automatically set optimum input threshold levels.

If you need better stability than the standard 5-ppm crystal oscillator provides within the range of 0 to 40°C, you can select either the temperature-compensated or the ovenized crystal oscillator. You can also use an external 10-MHz reference.

The instrument's software supports two user interfaces. A virtual front panel simulates benchtop operation with mouse control of pull-down menus, including built-in statistics. You can also operate the counter under program control with simple English-like commands compatible with any programming language.—Doug Conner

Guide Technology Inc, 1940 Fallenleaf Lane, Los Altos, CA 94022. Phone (415) 961-9259.

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CIRCLE NO 113
Logic verifier handles ASICs and PLDs

The Personal Logic Design Verification System (PLDVS) allows you to perform functional tests and develop test programs for your ASIC- and PLD-based designs. The system comprises hardware and software that combine with your IBM PC/AT or compatible computer to form a test workstation.

The hardware portion of PLDVS includes plug-in cards for the computer and a generic socket adapter to receive the device under test. The adapter accepts devices with as many as 128 signal pins and is configurable to any device pinout and package style. You can program the system to simultaneously stimulate and read the signal pins, check for pin continuity, and monitor signal-drive current—all at rates as great as 200,000 vectors/sec. The system double-latches signal readings using fixed TTL or CMOS logic thresholds.

The system has five power supplies available to operate the device under test. You can control each supply individually and set it anywhere between -12.5V and +12.5V.

The software portion allows you to create test programs using a Pascal-like language. You can enter test vectors in tabular form or generate them with algorithms. By using algorithms, you can quickly generate large numbers of test vectors, allowing you to exercise your design thoroughly. A 25-line program, for example, generates 65,000 test vectors for a counter design.

The system software also includes a variety of utilities that allow you to design custom test-result displays. One utility, for example, automatically places pin readings at a specified location on the computer's screen whenever the readings change.

When used with the company's Max+Plus logic design software, the design verification system accepts waveform descriptions for test vectors. The test results can also be displayed as waveforms. You can compare simulation results with actual device performance for the company's Max EPLDs.

The PLDVS costs $6595, including software, interface, adapters, and documentation. The graphical interface design software costs an additional $3400. Both require an IBM PC/AT or compatible computer.—Richard A Quinnell

Altera Corp., 3525 Monroe St, Santa Clara, CA 95051. Phone (408) 984-2800.

Circle No 730

EDN March 30, 1989

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For example, our new HD4074408 has an 8K one-time-programmable EPROM, a 512 x 4 bit RAM, 58 I/O lines, comparator inputs, PWM timer outputs and serial interfaces—all in a plastic package. Future devices will include A/D converters, phase locked-loop circuitry, DTMF generators, and much more.

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development, ZTAT devices for pilot and small-scale production, and mask ROM devices for large-scale production. And, a full complement of development support tools is available for use with IBM-PC*, DEC VAX*, and Hitachi systems.

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*We make things possible*
The shapes of things to come—realistic 3-D graphics images—will soon be showing up on personal-computer screens. One of three new processing products can give a PC add-in board or embedded graphics system the power to produce high-quality graphics. (Photo courtesy Intel Corp)
Processors for 3-D graphics

Because of their enormous appetite for floating-point operations, 3-D graphics displays were previously limited to high-end workstations. With some powerful new processors, however, you can now bring workstation-quality 3-D graphics to such applications as PC add-in boards and embedded-graphics systems.

Margery S Conner, Regional Editor

Three-dimensional color graphics displays, which are capable of manipulating an image in real time and shading it realistically, require a processor to perform a great number of floating-point and integer calculations. Two recently introduced processors, the 80860 from Intel and the TMS34020 from Texas Instruments, are specifically tailored to produce 3-D graphics. A third chip, the G300 parallel processor from Inmos, makes it easier for you to design the company’s fast Transputer (T800) into 3-D displays. With any of these three products, you can design workstation-quality graphics into a personal computer or other graphics application.

Beyond their ability to perform fast floating-point calculations, the three products have little in common. For example, unlike the 80860 and T800/G300, the 34020 requires a coprocessor (TI’s 34082) to perform fast floating-point calculations. Both the 80860 and the T800/G300 combination have on-chip floating-point hardware, but the 80860 includes hard-wired shading algorithms; the T800/G300 does not. However, because 3-D graphics suits diverse applications, ranging from workstation displays to PC add-in boards to embedded military displays, there’s no one correct design approach. The application determines the cost and size of the system you can build as well as which chip you’ll choose. To decide which chip is best for your application, you must first understand how graphics chips perform 3-D manipulations and shading.

In a 3-D color graphics display, the graphics application software stores graphical shapes in world coordinates, which are dimensionless Cartesian coordinates. The scale of a world-coordinate system depends on the application: 3-D applications can require thousands of units of resolution.

The graphics system processor must be able to rotate or tilt any graphical shape to conform to the viewing angle. These manipulations require the processor to perform a matrix transformation. To get an idea of the number of floating-point multiplications and additions the processor must perform, consider the following example. To move a point (x, y, z) to a new position (x', y', z'), you must multiply it by a $4 \times 4$ transformation matrix:

$$
\begin{bmatrix}
    x' \\
    y' \\
    z' \\
    w'
\end{bmatrix} =
\begin{bmatrix}
    x y z w \\
    a b c d \\
    e f g h \\
    i j k l \\
    m n o p
\end{bmatrix}
\begin{bmatrix}
    x \\
    y \\
    z \\
    w
\end{bmatrix}
$$

$$
x' = ax + ey + iz + mw \\
y' = bx + fy + jz + nw \\
z' = cx + gy + kz + ow.
$$
A useful guideline for measuring an FPU's performance is the time it takes to do a $4 \times 4$ matrix transformation, a basic 3-D operation.

To multiply the vector representing the pixel position by the transformation matrix, the processor must perform 28 floating-point operations: 16 multiplications and 12 additions. The $4 \times 4$ matrix transformation is basic to all 3-D manipulations, so it's a useful guideline for comparing different processors' floating-point capabilities. For example, a representative workstation, the Sun-4, transforms 150,000 vectors/sec.

The graphics application software doesn't store all of a graphical shape's pixels in memory; instead, it divides the shape into a series of polygons and stores only the vertices of the polygons. To transform a graphical shape, therefore, the system must transform the vertices of all the shape's polygons (Fig 1).

After the graphics system processor transforms all of the shape's polygons to the correct viewing angle, the processor performs a clipping test to ensure that the system will display only those pixels that fit into the viewing window. The viewing window can be any size you care to make it.

To display the graphical shapes created by the application program, the processor must convert, or transform, the world coordinates to screen coordinates. Screen coordinates are relatively small, and their size is determined by the physical display. The screen-coordinate system for the IBM PC's VGA display, for example, is $640 \times 480$ pixels. The processor converts the coordinates by using a matrix transformation similar to those used for rotation and scaling. Up to this point, all the manipulations performed by the processor consist of floating-point operations.

The next step is for the system to move the graphical entities from 3-D memory to the 2-D screen display. To move the images, the system must use a hidden-surface-removal algorithm, which is necessary to make an image look realistic. When you look at a real object, the visible surfaces obscure surfaces behind them from view. When you move an image stored in three dimensions to the 2-dimensional screen, therefore, you must remove the surfaces that would be hidden from view in a real 3-dimensional object. The hidden-surface-removal algorithm checks each pixel in a scene and determines whether it would be visible from that particular view, and thus should be displayed in the scene, or whether it would be obscured by another pixel, and so should not be displayed.

The hidden-surface-removal algorithm can be performed in integer arithmetic. However, even though the graphics processor doesn't have to use floating-point arithmetic, its calculations are no fewer or less time consuming.

But first, scan convert

Before the graphics-system processor can apply a hidden-surface-removal algorithm, it must scan-convert the polygons to determine where their edges lie. Scan-conversion techniques rely on the fact that the color and visibility of adjacent pixels is usually very similar. The program calculates the horizontal limits of the polygon. Each pixel within the polygon must have its z value and color determined and placed in the z buffer and frame buffer, respectively. As a result of scan conversion, the system knows the color...
on the edges of the polygon and the z coordinate of each pixel and its color. The graphics-display system needs to know a pixel's z coordinate in order to remove hidden surfaces by using the z-buffer algorithm, and it must be able to identify the polygon's edges and their colors to perform the shading algorithms.

The z-buffer algorithm is the most popular hidden-surface-removal algorithm. It compares the depth of each pixel under examination (that is, its z coordinate) with the value currently in the z buffer. If the current pixel's z coordinate is smaller than the previous one in that position, the processor updates the z buffer with the new pixel's z value, and updates the frame buffer with the new pixel's color.

After performing hidden-surface removal, the graphics system can display a wire-frame representation of the graphical shape. However, to color each polygon with just one color gives a rough, unrealistic rendering of the object (Fig 2).

The next step, therefore, is to use a shading algorithm. In Gouraud shading, the simplest shading scheme, the algorithm uses linear interpolation to determine what the colors on each line should be (Fig 3). That is, if one edge is dark red, and the horizontally opposite edge is light red, fairly realistic shading would go linearly from dark to light red. At the halfway point, a Gouraud-shaded line has gone through half of the total color change.

Gouraud shading doesn't allow for the effect of a light source, however, a technique that produces an even more realistic image. The Phong shading technique creates the effect of a single light source. Rather than linearly interpolating across a line of pixels, Phong shading determines the normal vector for each pixel, and calculates the angle of incidence for the light source (Fig 4). The processor still performs a linear interpolation, but it recalculates each pixel's color on the basis of the pixel's normal vector.

There are several different ways to implement the shading algorithms in your graphics system. Only one of the three processors suitable for 3-D graphics display—Intel's 80860—provides the shading algorithms on chip. The others require you to implement the shading algorithms in software or to create an ASIC that can perform shading.

With over one million transistors on a single chip, Intel's 80860 integrates a RISC core, a floating-point unit (FPU), and a hardware shading unit. (For more information on the 80860's general processing capabilities, as well as a block diagram, see the Product Update on pg 87.) The on-chip FPU is capable of peak speeds of 80M flops. Its Linpack number is 10M flops (by comparison, a VAX 8650 has a Linpack rating of 0.7M flops). Keep in mind that Linpack ratings are always considerably lower than peak speed ratings, because the numbers generated in the Linpack benchmark can't fit into most on-chip caches. However, the 80860's cache is big enough to hold an entire 4 x 4 matrix transformation. Therefore, it can perform the transformation at close to its peak speed of 80M flops, which allows for 500,000 transformations/sec.

One of the most time-consuming parts of the process of rendering the image is the z-buffer check in the hidden-surface-removal algorithm. Even a flat shading

---

**Fig 3**—This version of the torus shows how the wireframe version can look after hidden-surface-removal and shading algorithms have been applied. (Photo courtesy Weitek Corp)

**Fig 4**—With the application of a Phong shading algorithm, which simulates the effects of a single light source, the teapot takes on a much more realistic look.
Even a simple shading technique such as the Gouraud scheme can run over 100 times more slowly than the 3-D matrix transformations.

of a 3-D surface is much slower than a simple 2-D fill because the processor must check the buffer for each pixel. When the buffer check is combined with Gouraud shading, the shading process can run about 100 times slower than the transform rate. The 80860 has dedicated hardware that performs the z-buffer comparisons and computes the shading interpolation on all pixels in a 64-bit word simultaneously. (A pixel may be 8, 16, or 32 bits long, so each 64-bit word may have 8, 4, or 2 pixels.) The shading hardware gives you a choice between Gouraud or Phong shading. Its Gouraud-shading speed is 50,000 polygons/sec. By comparison, the Sun-4 workstation's Gouraud-shading speed is 20,000 polygons/sec.

Although the shading algorithms are implemented in hardware on the 80860, they still don't approach the speed of the FPU. If you can't stand letting the FPU idle while the shading hardware completes its tasks, you can put the FPU to work performing application-software tasks such as simulation calculations. In this scenario, the 80860 functions as a workstation on a board. Fig 5 illustrates the architecture for a PC plug-in board that incorporates the 80860.

Note that the 80860 can operate as a stand-alone microprocessor; it does not require you to use another processor as a host. However, the software for the 80860 is totally incompatible with that for previous Intel processors, so if you wanted to run MS-DOS, you'd need an Intel host processor. Samples of the 80860 are available now. The chip will be in production in the third quarter of this year; it will cost $750 in OEM quantities.

Although the 80860 has 3-D graphics capability, it lacks the display-control hardware that a graphics processor has, and thus shouldn't be considered a true graphics processor. Texas Instruments' 34020, however, is a true graphics processor: It has built-in signals that support direct control of the display. It doesn't have floating-point capability, however; for that function, you need to use TI's recently introduced 34082 floating-point unit. The 34082 has a 50-nsec clock cycle; multiplication and addition occur in parallel, giving the chip a sustained floating-point speed of 40M flops, and a Linpack figure of 5.2M flops. It requires only 130 cycles for a full 4×4 matrix transformation, so it can perform more than 150,000 vector transformations/sec.

The 34082 has its own C compiler and assembler, and it can address as much as 256k bytes of memory over a local bus. These capabilities allow you to write your own routines (such as a rotation algorithm) for the 34082 and store them in the 34082's local memory. As host, the 34020 could command the 34082 to run its own routines from local memory, thus freeing the 34020 from having to oversee the operation of the 34082.

Because the 34020's object code is compatible with that of the chip's precursor, the 34010, a wealth of supporting graphics software already exists for the 34020. An example of such software is the Texas Instruments Graphics Interface (TIGA). The interface runs on 34010/34020 graphics plug-in boards in MS-
Fig 5—To exploit the power of many of today's PCs, whose capabilities now approach those of workstations, the PCs' graphics displays will have to be able to support workstation-quality graphics. One way to design a PC-based system with workstation-quality graphics is to plug in an 80860-based 3-D graphics add-in board that runs application software while the host processor runs the PC's operating system.

DOS systems; it standardizes the way that application software and the host processor communicate with the 34010/34020 graphics processor.

According to Karl Guttag, TI graphic-strategy manager and designer of the 34010/34020 family architecture, you must be careful to balance the workloads between the host processor and the graphics processor. Because of the difference in power between the 34010 and the 80286, which is often the host in PC workstations, the 34010 often had to wait for the host processor, an inefficient scheme. In 80386-based systems, the 34010 no longer has to wait for the host. To use the processors most efficiently in such systems, you must give more thought to which tasks you assign to which processor. According to TI, 80386/34010 systems are demonstrating speed increases beyond those you'd expect to obtain by simply adding the faster host processor. The speed increases result from the redistribution of processing tasks.

The 34020 makes no provisions for 3-D color shading. If your application requires shading, you have two choices: You can either implement the algorithm in software, or you can develop your own shading ASIC. In the past, only vendors of high-end workstations could justify the time and expense of developing a shading ASIC, but this situation will soon change. National Semiconductor (Santa Clara, CA), for example, plans to introduce hardware shading chips into its standard-cell ASIC library this year.

Samples of the 34020 will be available this quarter; full production of the chip will start in the fourth quarter of the year. Samples cost $500; in production quantities, the chip will cost $100. The 34020's volume price will be $150. You can expect the quantity pricing for the 34020 to fall below $50 in two years.

Make your graphics system stand out in a crowd

You may be concerned that designs based on single-chip processors such as the Intel and TI ICs will make your system or board too generic. This has indeed been the case with low-resolution graphics boards. There's little to distinguish one VGA-compatible personal-computer board from another, for example, so price has become the determining factor in a customer's decision to buy. That's a nice situation for the customer, but the board manufacturer will want to avoid it.

One way to distinguish your design from others is to develop your own chips to accelerate one part of the graphics pipeline. For example, you could develop hardware-shading ASICs. An add-in graphics-board company with experience in this technique is Matrox (Dorval, Quebec, Canada). According to Ray Snow, graphics-board marketing manager at Matrox, when the company evaluated the various graphics chips two years ago, it particularly liked the programmability...
If the shading portion of your graphics display is too slow, consider using a shading-accelerator ASIC.

of the TMS34010. However, it wasn't happy with the chip's relatively slow software bit-block transfer (BitBlit) speeds. Matrox developed its own ASICs to perform all BitBlit operations, windowing functions, and polygon fills. This scheme gave the company the programmability it found so attractive, as well as higher hardware BitBlit speeds. As you might expect, the company is looking for ways to accelerate shading for its next-generation 3-D graphics board. (Incidentally, Texas Instruments obviously agreed with Matrox about the need for faster BitBlits; the company incorporated faster hardware BitBlits in the 34020.)

Parallel processing speeds displays

The third product to consider for use in 3-D graphics systems is a 2-chip set comprising the Inmos T800 Transputer and the G300 color video controller. Inmos's T800 Transputer chip is aimed at parallel-processing applications. Parallel-processing applications are any applications that can be broken down into subtasks and performed by several different processors at the same time, accelerating the system speed. Graphics is a prime candidate for parallel processing. For one thing, the matrix manipulations necessary in graphics processing are very repetitive in nature. Further, parallel processing lets you develop several elements of a picture independently and bring them together just before displaying them on the screen.

The G300, which Inmos recently introduced, includes all CRT control signals and performs interface to the display; it also has a color look-up table and a video DAC. It leaves the T800 free to calculate matrix transformations, therefore (Fig 6). The T800's on-chip FPU achieves a sustained rate of 1.5M flops for a 3-D transformation. It transforms 50,000 vectors/sec. The T800 costs $330 (1000); the G300 is $100 (1000).

Note this final, significant detail: These ICs, particularly the 80860 and the 34020/34082, are extremely complex chips. You may well wonder how easy it will be to perform production tests on the boards you design with them. According to Bill Rash, marketing manager for Intel's 32-bit microprocessor line, it's the manufacturer's job to ensure that the chip is good when it leaves the factory. However, the 80860 does have some limited capability to assist you in system production testing. You can load the 80860's output buffers serially through a test pin with your test vectors, and thus exercise the surrounding board circuitry. (Unlike the 80386, the 80860 does not have self-test capability. The 80386's self-test capability relies on the fact that the chip is microcoded; the 80860 is not.)

As you might expect from TI, which has taken a leadership position in developing scan-path test methods, the initial version of the 34020 does incorporate a scan-path test method for emulation support. At present, the test capabilities of the 34082 are limited to forcing all pins to high, low, or 3-state, but the next version of the chip, due in 1990, will incorporate TI's full JTAG scan-path test method.

When you first see the prices of these processors, you may be taken aback. Consider, however, that these chips can give a graphics board or system the graphics

---

Fig 6—Because graphics is a natural application for parallel processing, the Inmos T800 Transputer, which is eminently suitable for parallel processing, is a good candidate for a node processor in a 3-D graphics subsystem. The company's IMSG300 chip takes care of video control, including video D/A conversion.
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HOW COULD WE POSSIBLY IMPROVE?
Manufacturers of processors for 3-D graphics

For more information on processors that implement 3-D graphics, such as the processors described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

**Inmos Ltd**
1000 Aztec West
Almendby
Bristol, UK BS12 4SG
(0454) 616616
FAX (0454) 617910
Circle No 620

**Texas Instruments Inc**
Semiconductor Group SC-879
Box 809066
Dallas, TX 75238
(800) 232-3300 ext 706
Circle No 652

**Intel Corp**
3065 Bowers Ave
Santa Clara, CA 95051
(408) 987-9890
Circle No 651

Fast processors that can handle 3-D graphics, therefore, are not just luxury options anymore; they're going to become necessary parts of graphics systems for many PCs in the near future.

**References**


Article Interest Quotient (Circle One)
High 491 Medium 492 Low 493
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(401) 885-3600 FAX (401) 885-5786 Telex: WUI6817157
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**LAP-B controller:** µPD72107
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- Memory-based host interface.
- On-chip DMAC.
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**SS No. 7 controller:** µPD72307
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Addressing the present and future needs of design engineers, Electro/89 features information on design, new technologies, and professional career issues.

Richard A Quinnell, Regional Editor

New York City is noted for offering something for every interest—at any hour of the day or night. For three days in April, the city will offer the electronics-engineering community much of interest in the form of Electro/89—eastern US's largest design-electronics trade show and convention.

An estimated 45,000 electronics engineers will converge on the Jacob Javits Convention Center, Tuesday, April 11 through Thursday, April 13, to see and hear about the latest developments in electronics technology. The show will feature more than 900 companies exhibiting their products and will offer 25 technical sessions and eight tutorials devoted to the present and future needs of electronics engineers and managers. New to the show this year will be a special exhibit area on design-automation tools.

In keeping with this year's theme, "Building a world class economy," the keynote speaker will be Dr John G Stoessinger, noted political analyst and professor of international affairs at Trinity University in San Antonio, TX. Dr Stoessinger is a member of the Council on Foreign Relations and author of 10 books on world politics, including the Bancroft Prize-winning The Might of Nations: World Politics in Our Time. His topic will be "Toward new horizons in the world's economy" at the keynote breakfast to be held on Tuesday, April 11 at 9:00 AM in the Marriott Marquis. Tickets for the breakfast cost $20.

Tracks to professional enhancement

The conference's economic theme continues in one of the six tracks along which conference organizers have arranged the professional program activities. The economic track, Entrepreneurial Activities, comprises two professional sessions. Session 14 discusses venture capital, which is characterized as an ingredient of, but "only part of the success equation," and session 18...
discusses hiring consultants to attain profitability.

The Automated Design/Semiconductor/Systems track (sessions 1, 4, 5, 16, 17, 20, and 21) will bring you up to date on a variety of circuit technologies, including PLDs, RISCs, and ASICs. If you're seeking timely practical advice, you might want to attend session 1 for a discussion of system-design techniques using ASICs, or session 4, which discusses high-density PLDs and their design tools. You also might consider session 20, which deals with in-circuit board programming. Those contemplating their next design may be interested in session 16, which deals with the second generation of RISC.

Microwaves, optics, and video

If your interests lie outside the digital world, you may want to follow the tracks on communications, (sessions 3, 7, and 10) or video technology, (sessions 11, 15, and 24). They will lead you to “Microwave technology,” (session 3), “Fiber optics networks,” (session 7), and two sessions, (11 and 15) on aspects of high-definition television.

The New Technologies track (sessions 6, 8, 13, 19, and 22) heads in the direction of tomorrow's engineering solutions. In session 6, you can learn the status and possible implications of high-temperature superconductors in electronics. Session 8 introduces you to the quantum world of "Nanoelectronics," where dimensions are small enough to allow adjacent circuits to interact because their electron wave functions overlap. You may come away from session 22 with new

Electro shuttle bus stops

The Electro shuttle bus will operate on show days from 8:00 AM to 7:00 PM. Here is a list of the shuttle stops:

- Lexington Ave at 42nd St, Grand Central Station
- 7th Ave between 51st and 52nd Sts
- 45th St, just west of Broadway
- 7th Ave at 31st St, Pennsylvania Station
- 41st St between 8th and 9th Sts (Port Authority Bus Terminal)
- 49th St and 8th Ave, northeast corner
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**NOON-1:30 PM EACH DAY:** MISCELLANEOUS VIDEOS

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**Worming your way into the Big Apple**

Whether you're staying in the city or just coming in for the day, the Jacob Javits Convention Center—located on 11th Ave between W 34th and W 39th Sts—is easily accessible. Both public transportation and a free Electro shuttle have stops at the center. The shuttle also has stops near hotels and transit terminals.

If you're coming in by plane, take Carey Bus from Kennedy ($8) or from LaGuardia ($6) Airports, or NJ Transit from Newark Airport ($6) to the Port Authority Bus Terminal. There you can catch either a crosstown bus or the Electro shuttle to the Javits Center. If you're coming by rail to Pennsylvania Station or Grand Central Terminal, you can catch either a crosstown bus or an Electro shuttle near the station.

The Center is served by two crosstown buses, the M-34, which runs along 34th St, and the M-42, which runs along 42nd St. Both buses stop at every block from river to river and are identified with Javits Center signs. The M-34 stops across the street from the center at 11th Ave. The M-42 stops at the north end of the center's internal roadway. The fare is $1 in either coins or tokens and transfers to north/south bus routes are free.

If you're trying to get to Electro by car, you have a challenge ahead of you. There is no parking available at the Jacob Javits Convention Center. Your best bet is to park at either the Manhattan Plaza Garage (on 42nd Street between 9th and 10th Avenues) or at the Port Authority Bus Terminal garage—accessible directly from the Lincoln Tunnel or from 40th Street. Once parked, catch either the Electro shuttle in the Port Authority terminal complex or the M-42 crosstown bus. Otherwise, it's a 10-minute walk.

An alternative to downtown parking is available if there are no afternoon baseball games scheduled. Park at either Yankee Stadium or Shea Stadium, and take the subway to 8th Ave at either 34th or 42nd. The fare is $1.
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<th>Model</th>
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<td>1MHz</td>
<td>11.0</td>
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<td>$775</td>
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*THD (Total Harmonic Distortion)

Electro/89

ideas for using a “personal computer for automatic test and measurement.”

Because an engineer’s career is not based on technology alone, you may wish to follow the Professional and Personal Concerns track (sessions 2, 9, 12, and 25). Session 2 focuses on personal career development and management. Session 9 explores “Opportunities for experienced engineers,” and session 12 examines the special concerns of “Women in engineering.” You may also want to hear EDN’s Jon Titus, along with IEEE officers and the editors of other publications at session 23, “Meeting the needs of the EE profession.”

In addition to the professional sessions, Electro/89 will offer eight tutorials, covering a variety of subjects. Some tutorials of particular interest to EDN readers are “Neural networks—Models and hardware implementation,” held Thursday, April 13 at 1:00 PM, and “Fiber optic communications,” scheduled for Wednesday, April 12 at 9:00 AM. Tutorials are not covered by the show’s registration fee, however. They range in price from $70 to $285.

Don’t forget the exhibits

When you are done with the professional program, you'll still have time to explore the exhibitors’ booths on the convention center’s main floor. The exhibits are open from 9:30 AM to 6 PM on Tuesday and Wednesday, and 9:30 AM to 4 PM on Thursday. Included in the exhibits are products in a category new to Electro—design-automation tools. A cluster of more than 50 exhibitors will provide an automated design center where you can try out new developments in this growing field.

Whatever your interests, Electro/89 in New York offers something to make your day. What New York has to offer at night is yours to discover.

Article Interest Quotient (Circle One)
High 494 Medium 495 Low 496
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The PA7024 is the first member of a CMOS programmable-device family, PEEL (programmable electrically erasable logic) ARRAYS, which combines elements of both PLDs and programmable gate arrays. The foundation of the PA7024 is its logic-control cell (LCC).

Each LCC has four primary input lines and produces two independent output signals. LCCs contain registers that can operate as synchronous or asynchronous D, T, or JK flip-flops. The input signals for each LCC are four of 80 possible sum-of-product terms, selected by programming.

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The PA7024 has 20 I/O pins and two dedicated clock-input pins. Internal to the device are 20 LCCs, 20 I/O cells, and a global cell interconnected through a programmable logic matrix. The device allows you to define signals in PLD-like sum-of-product terms but, as with gate arrays, creating internally used signals does not force you to sacrifice an I/O pin.

The global cell controls selection and routing of clock signals to both the I/O cells and the LCCs. This cell can treat all cells as a single group with a common set of clocks or divide them into two independent groups. The internal clocks can operate as fast as 50 MHz. The propagation delay from one I/O pin through an LCC to another I/O pin is 23 nsec. $22.50 (100). Samples will be available in the second quarter of 1989.

International CMOS Technology Inc, 2125 Lundy Ave, San Jose, CA 95131. Phone (408) 434-0678. TWX 910-997-1531. No booth. Product to be reviewed at session 4.

Circle No 658

100-MHz digital-storage oscilloscope travels to the field

The PM 3308 looks like a portable typewriter, but it's actually a full-featured digital-storage oscilloscope. It features a maximum single-channel sampling rate of 40M samples/sec and a sample memory of 8k bytes. The scope also has a battery-backed 180k-byte RAM-disk, allowing storage of as many as 100 setup menus and waveforms.

The oscilloscope has a 100-MHz bandwidth and two input channels. It can display as many as four traces, however, allowing simultaneous display of input signals and computed traces. The computed traces can be based on addition, subtraction, multiplication, division, integration, and differentiation of signals.

In addition to displaying waveforms, the oscilloscope allows you to make a variety of waveform measurements. These include time between reference points, voltage differences, p-p and rms voltages, mean and average voltages across a trace, rise time, frequency, period, and phase. A glitch-capture capability registers the occurrence of transient signals that are as fast as 10 nsec. You can make all measurements either relative to a reference or as absolute values.

The unit features an electroluminescent display screen that folds down for transporting. It weighs 14.5 lbs and comes with a shoulder strap to make carrying it to field sites easier. The PM 3308 costs $7500. Delivery, eight weeks ARO.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 443-5853; in OR, (206) 356-6433. TLX 185102. Booth No 1559.

Circle No 657

EDN March 30, 1989
Electro/89 Products

Emulator series supports 68020 processor with clock rates as fast as 25 MHz

The HMI-200 Series in-circuit emulators now include units that support 16- and 25-MHz 68020 microprocessors. Both units are functionally identical, differing only in operating speed. Like other members of the series, each unit operates with either a terminal or host computer controlling the unit through an RS-232C data link. The emulators have two RS-232C ports; one attaches to the controller, and the other allows data transfers such as downloading data files from a second source or printing the trace buffer's contents. The ports support data rates to 19.2k baud.

The units allow both single-step and real-time emulation of the processor. You can program as many as four complex break and trigger points, using combinations of address, data, status, and external signal lines to specify the activating condition. You can also program four additional break points, using simple addresses and ranges. The units offer two 4k x 136-bit trace buffers, which store data having 32 bits of time-tag information.

The emulators offer a number of built-in functions. For example, you can use the break points singly or in a conditional sequence to stop emulation, to trigger acquisition of data to the trace buffer, to generate an output signal for external triggering, or to measure time between break points. You can also examine and modify memory and registers, search memory for data strings, test memory, and read and write hex files in a variety of formats.

When connected to an IBM PC or Unix-based system, the emulators allow symbolic and source-level debugging, using the optional SourceGate software. The software supports C, PL/M, and Pascal compilers from several manufacturers. You can display source code only, source and assembly, or assembly only when reading the trace buffer.

The 16-MHz version of the HMI-200 base unit costs $10,500, and the price of the 25-MHz version is $16,000. Delivery, six to eight weeks ARO.

Huntsville Microsystems Inc, Box 12415, Huntsville, AL 35802. Phone (205) 881-6005. TWX 510-600-8258. Booth No 971.

Circle No 654

Data-acquisition mainframe communicates over IEEE-488 bus

The Model 556 data-acquisition mainframe allows you to connect a variety of digital and analog signals and controls to any computer that supports IEEE-488 communications. The mainframe can accept as many as 10 plug-in cards and present them to a host computer as a single remote instrument.

The device comprises a 10-slot card cage, a power supply, and IEEE-488 interface control logic. The unit communicates on the IEEE-488 bus as a single instrument, regardless of the number of plug-in cards inserted. To control individual cards, you must send device-dependent commands to the unit; that is, commands that include the card's location. The unit's control logic can read card identifiers, allowing you to query the unit to determine your setup. The control logic is also compatible with test-instrument software such as LabView and Labtech Notebook.

The unit is self-contained, requiring no special controller cards in the host computer. It supplies all needed power to the plug-in cards, providing as much as 800 mA at ±15V and 3A at 5V.

The manufacturer offers a choice of 28 boards for use in the mainframe. These boards have a variety of signal input and output characteristics and provide functions such as strain-gauge signal conditioning, thermocouple sensing, and data acquisition. You can also use boards for the Model 556 with other mainframes from the same manufacturer. The Model 556 costs $1395.


Circle No 653

EDN March 30, 1989
Fast response time, less than 5 ms, gives Finlux Electroluminescent displays video capability. In laptop PCs, the cursor is visible during all rapid movements or data changes.

As for picture quality, you can see for yourself; it's worth a thousand words. Here are just a few: Crisp. Stable. Bright. Wide-angle viewing. Finlux EL is easy on the eyes, even during a long workday.

The big little EL display

The display above is shown as large as life. Just 18 mm thin and weighing less than 500 grammes, this Finlux EL shows as much text as an 11" CRT: 25 lines of 80 characters, or full graphics. Finlux EL displays are available in a range of 320 x 256 to 640 x 400 pixels.

Wherever your customers need compact clarity

Finlux EL displays are easily interfaced for high-resolution graphics, word processing, medical and industrial applications. The fully solid-state flat EL panel and electronics are assembled into a sturdy, compact package ready for mounting in even the most demanding environments.

Lohja Finlux is the only European manufacturer of flat panel Electroluminescent displays. To see more, get in touch with:
Universal device programmer handles all available technologies

The System 3000 simplifies your device-programming operation by giving you a single set of hardware for all your programming needs. The system can handle more than 1600 device types, including PLDs, PROMs, EEPROMs, and microcomputers. The unit has 2M bits of onboard RAM as standard and is expandable to 64M bits, allowing it to handle high-density devices.

The programming section accepts DIPs with pin counts from 16 to 40 and widths from 0.3 to 0.6 in. An optional SMD chip station handles PLCC and LCC surface-mount devices with 20- to 68-pin packages. Each pin location in the programming section has programmable voltage, current, and rise-time output characteristics as well as the ability to sense conditions such as open and short circuits.

System 3000 handles all available programmable device technologies, including NMOS, CMOS, bipolar, and fuse-link memories. It reads electronic identifier bytes, when available, and retains its configuration on power-down, thereby making setup and use easier. A user-inserted IC memory card contains all the device libraries and programming algorithms needed by the unit.

The unit features a built-in keyboard and CRT display that allow you to use it as a stand-alone programmer. Offering four interface ports—two RS-232C, an IEEE-488, and a handler port, the unit lets you communicate with a host computer or peripheral equipment. $9495.

Stag Microsystems Inc, 1600 Wyatt Dr, Santa Clara, CA 95054. Phone (408) 988-1118. Booth No 2827.

Circle No 656

IBM PC-based software supports PLD design and modeling

The OrCAD/PLD and OrCAD/MOD software tools allow you to design and simulate PLD functions on an IBM PC, PC/XT, PC/AT, PS/2, or a compatible computer. The OrCAD/PLD design package is either integrated with schematic capture and simulation software or can function as a stand-alone design aid. It allows you a choice of methods for describing your design. You can use schematics, Boolean equations, truth tables, or procedural state-machine programs to define your circuit's operation. The program also supports indexed equations; as a result, counters, Gray code converters, addressable latches, and other structured designs are definable with a single equation.

The PLD package generates standard JEDEC files for programming a device. It also features a logic simulator, allowing you to create test-vector files for later design verification. When used as part of an integrated design package, the software allows you to back-annotate your schematic with text files that describe the PLD's function; it also automatically updates the schematic files whenever programming changes are made.

The modeling program, OrCAD/MOD, serves as an extension to the OrCAD/VST verification and simulation software. MOD allows you to create simulation models based on the PLD's definition and the JEDEC file. The program combines the design information with the structure and timing characteristics of specific PLD devices. The characteristics are stored in a library file that comes with MOD. The file contains more than 300 entries and offers utility programs for creating additional models. The software packages cost $495 each.


Circle No 655
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SIMM sockets provide the highest security your memory or logic module could ask for: Each contact produces 200 grams normal force on each module pad. Minimum. And the contacts float. They’re free to move laterally, so uneven thermal expansion can’t separate contacts from pads. Goodbye, fretting corrosion, opens and intermittents.

Hello, reliable performance on 100 mil and 50 mil center modules. We’ve also thought about the effects of use on long-run reliability. So our MICRO-EDGE SIMM sockets provide positive wiping action during insertion. And contacts are designed to deflect up to .017”, with full anti-overstress protection—for giving enough to handle any standard (.047” to .054” thick) module board.

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We’ve also seen to it that contact retention in the housings allows robotic application, as well as inde-
Closed bottom design prevents solder wicking and bridging. And, naturally, latching ears are protected against overstress, and module polarization is designed in.

Now the best part: MICRO-EDGE SIMM sockets are available in the style you need. We have .100" or .050" centerlines in a wide selection of singles and duals, vertical and slanted. Plus options, including a choice of gold or tin on contact mating surfaces.

Our very-low-insertion-force design and high-reliability contacts make the 50 mil versions especially attractive. Every version comes with the quality and support you expect from AMP.

For literature and product information, contact the AMP Information Center, toll-free, at 1-800-522-6752. AMP Incorporated, Harrisburg, PA 17105-3608.

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Electro/89 Products

POWER SUPPLIES
Series 6A, 6B, and 6C power supplies feature a mainframe enclosure that provides the main output. The mainframe accommodates and powers as many as three auxiliary modules with 2 to 48V outputs; the overall power ratings are 600W for the 6A series, 800W for the 6B series, and 1000W for the 6C series. The main output values range from 2 to 24V; a 5V main output provides currents of 90 to 150 mA.

You can connect outputs with identical voltages in parallel, regardless of current ratings. When so configured, outputs automatically current-share in proportion to their current ratings. Standard supply features include overvoltage protection, remote sense, automatic thermal shutdown, and soft start. The units feature an EMI filter and also include reverse-voltage protection. $939 to $1079. Delivery, stock to eight weeks ARO.

Powertec, 20550 Nordhoff St, Chatsworth, CA 91311. Phone (818) 882-0004. TLX 277483. Booth No 313.

Circle No 659

CONNECTORS
L Series low-insertion-force (LIF) connectors provide the combination of small size and low contact resistance required for plug-in power supplies. These rugged rack-and-panel connectors are available with contacts rated for 8, 15, 25, 50, and 200A. The L Series product line utilizes a hyperboloid-type LIF socket. In addition to LIF, the socket design provides inherent immunity to shock and vibration. Socket contact resistance ranges from 0.25 to 2.5 mΩ. The float-mounting socket design accommodates as much as 0.049 in. of radial misalignment in blind-mating situations. The connectors are available with solder cup, crimp, and flow-solder terminations, depending on the contacts selected. The L Series units meet the performance requirements of MIL-C-28748A. $40 to $100 (1000). Delivery, 14 to 16 weeks ARO.

Hypertronics Corp, 16 Brent Dr, Hudson, MA 01749. Phone (800) 568-9228; in MA, (508) 568-0451. FAX 508-568-0680. Booth No 503.

Circle No 660

HEAT SINKS
Series 6760 heat sinks provide low thermal resistance in both natural-convection and forced-air applications. The units feature aluminum fins that are bonded to the mounting surface with epoxy. The nine standard units in the line have hole patterns that accommodate all standard power modules.

Forced-air models will accept muffin fans that have a 4.12-in.-square mounting-hole pattern. Mounting surfaces range from 7×4.78 to 16×10.78 in., and thermal-resistance values range from 0.024 to 0.08°C/W. Natural-convection models are 3.13 in. high and are available in 7- and 12-in. lengths. The heat sinks have a 7.375-in.-wide mounting surface and are available with or without mounting flanges. Thermal resistance ranges from 0.22 to 0.3°C/W. The 7-in. natural-convection model, $39.37 (100). Delivery, eight to 12 weeks ARO.

Aavid Engineering Inc, Box 400, Laconia, NH 03247. Phone (603) 528-3400. Booth Nos 2660 and 2662.

Circle No 661

SIGNAL GENERATORS
Models 2040 and 2045 arbitrary waveform generators convert data from 8-bit bytes to analog voltages at the rate of 800M points/sec. You can describe the desired waveforms as mathematical equations, graphics sketches, or line segments, or you can download them from a host computer. The generators feature 512,000 points of memory that you can divide into multiple segments and 78k bytes of battery-backed RAM that stores files containing polynomial waveform definitions. You can trigger the output wave-
forms or you can synchronize them to an external source.

Both generators provide a pair of analog outputs. The 2040's outputs, which are in phase opposition, have internal impedances of 50Ω and supply a 1V p-p signal to a 50Ω load. One output of the 2045 is obtained directly from the main D/A converter, and the other passes through a programmable 64-dB attenuator and Bessel filter. Model 2040, $13,500; Model 2045, $14,500. Delivery, 90 days ARO.

Analogic Corp, 8 Centennial Dr, Peabody, MA 01961. Phone (508) 977-3000. FAX 508 531-1266. TLX 949307. Booth No 2812.

Circle No 663

PROGRAMMING SYSTEM
LabView version 2, an upgrade of version 1.2, has a compiler that significantly reduces the execution time, provides editing capabilities like rubberbanding, and offers graphics controls such as panning and zooming. This color, icon-based programming system simplifies engineering and scientific programming on Apple Macintosh computers by permitting you to design software-generated virtual instruments. You produce these instruments by drawing block diagrams that represent test and measurement functions. You then control the instruments via pictorial renditions of the types of switches, dials, and levers you might actually find on 3-D versions of such equipment.

To reduce memory requirements and to further increase execution speed, LabView 2 adds multiple integer and floating-point data formats to 1.2 version's extended-precision floating-point data type. LabView 2 can run all the applications you've developed under version 1.2 and is available to owners of version 1.2 at no cost. $1995.

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 551-4742; in TX, (800) 433-3488. TLX 756737. Booth No 524.

Circle No 662

IBM PC-BOARD ROUTER
The HiWire-Plus Autorouter is a gridless, via-minimizing, multi-layer, IBM PC-based autorouter. It lets you make trace-specific design
rules; for example, you can tell the autorouter to route power networks with 21-mil width and 11-mil spacing, some signal traces with 12-mil width and 8-mil spacing, and other signal traces with 5-mil width and 5-mil spacing. The HiWire Plus Autorouter completes board routing; it lets traces cross each other and violate other design rules during the early stages of routing.

In subsequent phases of routing, the Autorouter optimizes, rips up, and reroutes vias for each network. During the final passes, the router centers traces in the routing channels and further optimizes vias. For critical traces, you can prewire before starting the autorouter. To operate the HiWire Plus Autorouter, you need the HiWire Plus CAD package and an IBM PC, PC/XT, PC/AT, or PS/2 with 640k bytes of RAM. A utility program can translate FutureNet, OrCAD, Schema, and Tango netlists. $895.

Wintek Corp, 1801 South St, Lafayette, IN 47904. Phone (800) 742-6809; in IN, (317) 742-8428. TLX 709079. Booth No 760.

Circle No 665

PROCESS METER

The model 205-P digital process meter features 0.56-in. characters and includes a power supply. It provides a 3½-digit display span. Potentiometers allow you to achieve 2000-count zero and span adjustments from the front of the meter's panel. The full-scale signal ranges of 4 to 20 mA, 0 to 199.9 mV, 1 to 5V, 0 to 10V, and 0 to 100V are jumper selectable. The input is true differential and features 56 dB of normal-mode noise rejection. The meter operates either from 24, 100, 115, or 230V ac or from 5 or 7 to 32V dc power sources. All power options feature EMI filtering, which prevents power-line noise from disrupting the meter reading. The meters are housed in a polycarbonate plastic case that carries a

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CIRCLE NO 96

Electro/89

94V-0 UL rating. Removable screw-clamp cable connectors for signal and power terminations comply with VDE and UL requirements. From $139.

Newport Electronics Inc, 630 E Young St, Santa Ana, CA 92705. Phone (714) 540-4911. FAX 714-546-3022. TWX 910-595-1787. Booth No 2113.

Circle No 664

SIGNAL GENERATOR

The Model 2100A-7 synthesized function/pulse generator produces sine, square, and triangular waves as well as positive and negative programmable-width pulses. It covers the frequency range of 0.01 Hz to 31.16 MHz (to 10 MHz for pulses) with 7-digit resolution and accuracy of 0.5 ppm. The main output provides open-circuit voltages that you can set from 10 µV to 30V p-p. You can also obtain outputs whose amplitude accuracy is 0.05 dB, as an option.

An auxiliary output supplies TTL levels. The pulse rise and fall times are <11 nsec. The unit sweeps the output frequency linearly or logarithmically between start and stop frequencies that you program. You can also vary the frequency by supplying a programming voltage. Below 30 kHz, the unit can produce bursts of 1 to 255 waveforms with start and stop points programmable in 1° increments from -90 to +267°. $4750. Delivery, six weeks ARO.

Krohn-Hite Corp, Avon Indus-

CIRCLE NO 155

EDN March 30, 1989
Fluke signals the end of the generation gap.
That was then.

The Fluke 6011A Signal Generator. This innovative product featured a crystal reference oscillator, and could output frequencies from 10 Hz to 11 MHz. It signalled Fluke's major entrance into the generator market, and continued the tradition of excellence Fluke had established with their multimeter and calibration product lines for years. Introduced in the 1970's, the 6011A was Fluke's first microprocessor-based signal generator, and had an incredible 0.15 dB amplitude accuracy specification (0.07 dB typical). Even today, for certain applications, the 6011A remains to be the best signal generator available.
The Fluke and Philips alliance closes the gaps Fluke once had in its signal generator line. Today, you can choose from three times as many signal sources, generating a wider range of frequencies, and offering more functions. The entire range covers frequencies from 0.0001 Hz (almost DC) to 2 GHz, and includes synthesized RF, LF and MF signal generators, function and pulse generators, and video and audio pattern generators.

6062A Synthesized RF Signal Generator. 10 kHz to 2100 MHz: frequency output range: with ±1 dB amplitude accuracy to 1 GHz, ±1.5 dB to 2.1 GHz. Includes amplitude, frequency, phase and pulse modulation. Featured is a fast rise 15 ns pulse modulator using gallium arsenide technology. IEEE-488 is standard.

6066B Synthesized RF Signal Generator. 10 kHz to 1030 MHz: ±1 dB amplitude accuracy: ±0.001% spurious. IEEE-488 optional.

6071A Synthesized RF Signal Generator. 200 kHz to 1040 MHz: high spectral purity: AM, FM, PM modulation; precision digital sweep.

PM 5190X Synthesized Function Generator. 1 mHz to 2.147 MHz: sine, triangle, square waveforms; TTL output.

PM 5134 Function/Sweep Generator. 1 mHz to 20 MHz: five waveforms; sweep, burst, single modes; 20 Vp-p output.

PM 5132 Function Generator. 0.1 Hz to 2 MHz; five waveforms: sweep, VCO modes; variable duty cycle.

PM 5725 Pulse Generator. 0.1 Hz to 10 MHz: 15 V output amplitude; 10 ns rise time; external triggering.

PM 5715 Pulse Generator. 1 Hz to 50 MHz: 6 ns to 500 ms rise/fall times; 10 V amplitude.
And here's the ultimate challenge: Try to find a company that gives you better service and support than Fluke.

When you buy Fluke or Philips products, you can count on getting more than the hardware you order. Because we also deliver Fluke service and support. We stand behind every Fluke or Philips instrument we sell, and we challenge you to find anyone in the industry who consistently backs up their gear better than us.

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Featuring a 45° entry, Eurostyle terminal strips save space and provide easy, safe access for wiring on crowded pc boards. The 0.197-in. contact spacing provides five terminations in less than an inch. The strips have touch-proof terminals and wire-ready captive screws that won't fall out and cause shorts. The terminals have UL ratings of 15A and 300V max. Other features include wire entries that accept wires as large as #14 AWG, a closed side that acts as a wire stop, and thermoplastic insulator material that has a UL flame-retardant rating of 130°C. $0.18 (500).


Circle No 667

8-BIT FLASH ADC
Fabricated in low-power CMOS, the ADC-208 flash A/D converter provides an 8-bit sampling rate of 20 MHz and effective bit rates to 30 MHz in the burst mode. The video flash converter operates from a 5V supply and consumes 500 mW of power. Other features include a
New, improved 12-bit microprocessor-compatible A/D converters run cooler, last longer, cost less than ever before.

Burr-Brown's new ADC574A/674A A/D converters have been redesigned for greater economy and reliability. They are complete devices, with +10V buried-zener reference, internal current-controlled clock; 8-, 12-, or 16-bit µprocessor interface; and three-state output buffers.

**Key ADC574A/674A Features**
- 12-bit resolution
- ±1/2LSB max linearity error
- 450mW max, typ power dissipation
- 150ns max bus access time
- 28-pin ceramic or plastic DIP packaging
- no missing codes guaranteed for 0/+75°C and -55/+125°C specified temp ranges
- from $15.75 in 1000s (U.S. List Price)

Ask your Burr-Brown sales representative for complete details and evaluation samples, or call Applications Engineering, 1-800-548-6132. Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734.
Electro/89 Products

1-shot-mode conversion time of 35 nsec and a mid-point tap for use with an external voltage source to improve integral linearity. The ADC-208 also provides latched 3-state outputs for µP interfacing. Housed in a hermetic 24-pin ceramic DIP, the device is available in both commercial and military temperature-range versions. $50 to $158 (100).


MULTIMETER
The Model 199 digital multimeter measures dc and ac voltage, dc and ac amps, ohms, and decibels. By adding an 8-channel scanner option, you can transform the instrument into a complete multichannel measurement system. The instrument's sensitivity specs are 1 µV, 1 mΩ, and 100 nA, and its best 1-year dc-voltage accuracy is 0.007% of reading. You can take 150 readings/sec at a resolution of 4½ digits and store them in an internal buffer. You can trigger the readings externally.

The optional scanner, which you can install at your site, offers a switching speed of 400 channels/sec, including measurement time, 2-pole and 4-pole switching, and <1 µV thermal offset in switch contacts. The low thermal offset lets the Model 199 accurately switch and measure low signal levels. Further, the scanner's 4-pole switching mode provides Kelvin-type (4-wire) resistance measurements. The unit can switch and take measurements across 40 channels/sec. With scanner, $1395; without scanner, $995.

Electro/89 Products

spin-up loads required by peripherals such as disk or tape drives and printers. The switchers feature main 5V outputs with current capabilities of 20 to 50A. Auxiliary 5, 12, 15, and 24V outputs are available with as much as 16A of peak current. All units are available with as many as four outputs.

The supplies feature built-in line filtering, 3750V ac safety isolation, shielded power transformers, built-in overload and overvoltage protection, overtemperature shutdown, remote-sensing capability, vacuum-impregnated magnetics, and fixed-frequency pulse-width modulation. You can also opt for a power-valid indicator and for TTL-high or TTL-low power-fail detection circuitry. All units meet VDE, IEC, UL, CSA, FCC, and British Telecom specifications for safety isolation and EMI/RFI emissions. $266 to $358. Delivery, six to 10 weeks ARO.

Switching Systems International, Box 1599, Placentia, CA 92670. Phone (714) 996-0909. FAX 714-996-2753. Booth No 2324. Circle No 670

DISPLAY MODULE

The Model 4285-XX canned-message module combines an 8-line × 32-character dc gas-plasma display with an infrared touch-screen. The module provides 16k bytes of RAM, which can store as many as 127 canned messages; the memory is backed by an onboard battery. The touch-screen IR switch matrix provides 128 switch locations. The alphanumeric display provides a 64-character ASCII character set as well as several European character sets in a 5 × 7 dot-matrix format.

The software can adjust the green or neon-orange characters to three brightness levels. The module accepts RS-232C or RS422 data at 1200 or 9600 baud. The unit supports CTS (clear to send) and DTR (data terminal ready) signals and can detect parity and rate errors in transmission. Options include mounting subpanels, drip-proofing, and EMI/RFI shielding. Neon-orange or red display, $1089; green display, $1242 (100).


OP AMP

The AD846 op amp uses current feedback to provide a 46-MHz gain-bandwidth product at a gain of -1 and 31 MHz at a gain of -10. Settling time to 0.01% equals 110 nsec for a 10V step. The offset voltage

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Electro/89 Products

measures 75 µV, and the offset voltage drift is 3.5 µV/°C; the open-loop transimpedance measures 200 MHz. Although the quiescent current measures only 6 mA, the AD846 delivers as much as 65 mA of output current. Input voltage noise equals 2 nV/√Hz; input current noise for the inverting and non-inverting inputs measures 20 pA/√Hz and 6 pA/√Hz, respectively.

The total harmonic distortion of 0.0005% at 100 kHz makes the AD648 well suited for high-performance audio-circuit applications. To implement the AD648, you use the source and feedback resistors to set the dc transfer function. However, the feedback resistor alone determines the closed-loop ac response. This eliminates the usual design tradeoffs between required gain and achievable bandwidth. The device is available in plastic mini-DIPs, hermetic ceramic DIPs, and hermetic metal cans. Two operating ranges are available: -40 to +85°C and -55 to +125°C. From $7.45 (100).

Analog Devices, Literature Cen­ter, 70 Shawmut Rd, Canton, MA 02121. Phone (617) 935-5565. Booth No 2518.

Circle No 673

HEAT-SINK MOUNT

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Although designers often prefer dynamic RAMs (DRAMs) to their static counterparts, they sometimes shy away from using DRAMs because of the devices' added complexity. This article, part 1 of a 4-part DRAM series, sheds light on some of the complex issues surrounding DRAMs and describes the different DRAM architectures. The succeeding articles will cover memory-system architectures, DRAM controllers, and DRAM-board design.

Steve Gumm and Carl T Dreher, Texas Instruments

When constructing a memory system, designers most commonly choose the dynamic RAM (DRAM) as the basic building block. The DRAM owes its popularity to the fact that it costs less than the static RAM (SRAM), yet has a higher bit density, an advantage that stems from the DRAM's simple, tiny memory cells. It's true that DRAMs require more housekeeping than SRAMs do: The term "dynamic" implies that the data in the memory cells must continually be accessed or refreshed to ensure that the stored data is valid. Nevertheless, DRAMs' lower cost and smaller size more than make up for any deficiencies.

A designer's first encounter with DRAMs can often be intimidating. The uninitiated engineer must confront such terms as "page-mode access," "static-column mode access," and "nibble-mode access," as well as "refresh rate," and "precharge period." The designer also faces a host of timing parameters, which can be perplexing. Even after you understand these bewildering terms, you must choose from among a vast number of options the DRAM architecture that best suits your needs.

The most common type of DRAM, which is classified as \( N \times 1 \), stores 1 bit of data in \( N \) addressable locations. Each device has a 1-bit input and a 1-bit output data bus. Current single-package bit densities for this family range from 16k bits to 1M bits; 256k bits is the most popular. Other less-common types include the \( N \times 4 \) and \( N \times 8 \) DRAMs, which have 4- and 8-bit data buses, respectively. Although this discussion is restricted to \( N \times 1 \) DRAMs, you can easily apply the information presented here to DRAMs with wider buses.

The difference between SRAMs and DRAMs

Accessing data in a DRAM is different from accessing data in an SRAM. The DRAM has a multiplexed-address arrangement, which conserves package space. To access data, a 256k-byte DRAM requires 18 addresses \( (2^{18} = 256k) \). To accommodate these addresses on separate pins—along with the normal complement of pins for power, control, and I/O data—would require a 24-pin package. The DRAM has nine address lines \( (A_0 \) through \( A_8 \) and two strobe lines for accessing data. Essentially, the DRAM accesses a row and a column of an array by internally latching a row address with...
Even though they require more housekeeping than SRAMs do, DRAMs’ lower cost and component size more than make up for any deficiencies.

The Row Address Strobe (RAS) and a column address with the Column Address Strobe (CAS). Because both addresses are multiplexed onto the same pins, 256k-bit DRAMs come in 16-pin packages and 1M-bit DRAMs come in 18-pin packages.

Besides multiplexed addressing, the most significant differences between SRAMs and DRAMs are their refresh and precharge requirements. A DRAM’s memory cell consists of a storage capacitor. When a charge is placed on this capacitor for data storage, the charge must be periodically refreshed; otherwise, the capacitor will discharge, invalidating the stored data. Some of the older 16k-bit DRAMs must be refreshed every 2 msec; newer 1M-bit DRAMs specify a 10-msec refresh rate.

The DRAM’s architecture simultaneously refreshes all of the column cells for a selected row every time the row is accessed. Furthermore, some DRAMs reserve the most significant bit (MSB) as a select bit for an internal multiplexer that selects data in two banks of arrays. In these DRAMs, the lower address bits access the memory cells in both banks simultaneously. This arrangement cuts the required number of refresh cycles in half. For example, a 64k-bit DRAM, which has eight row- and column-address lines, requires a refresh cycle for only 128 rows instead of 256. Similarly, a 256k-bit DRAM requires only 256 cycles, and a 1M-bit DRAM requires only 512 cycles.

Another peculiarity of the DRAM is precharge. Performing a memory-read operation from a DRAM cell causes its capacitor to discharge slightly. Therefore, data must be written back into the cell after each read operation. This write-back operation is called “precharge” and is automatically handled by the DRAM. The time it takes to perform this operation is called the precharge period, and you must account for it when you determine the read-cycle time for the DRAM.

An N × 1 DRAM has two pins, D and Q, for handling the input and output (I/O) data. In most of these DRAMs, the data-output line (Q) goes to the high-impedance state when inactive, so you can tie it to the data-input line (D) in order to handle bidirectional data. Other DRAMs require external 3-state buffers to handle bidirectional data. In order to conserve package size, N × 4 and N × 8 DRAMs share a set of bidirectional pins.

Perhaps the most intimidating features of DRAMs are their timing diagrams. Most of the turmoil centers on the sheer number of timing specifications and the combination of abbreviations used to describe them.

![Fig 1-A DRAM's internal architecture determines which of the variety of DRAM modes it can support. The TMS4256-12 DRAM, for example, has a 4-to-1 multiplexer that can access four memory arrays to support nibble-mode access.](image-url)
TABLE 1—PARAMETER ABBREVIATIONS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>ABBREVIATION</th>
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<tr>
<td>COLUMN OR CAS</td>
<td>C</td>
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<tr>
<td>ROW OR RAS</td>
<td>R</td>
</tr>
<tr>
<td>LOW SIGNAL</td>
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<td>HIGH SIGNAL</td>
<td>H</td>
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<tr>
<td>ACCESS TIMES</td>
<td>a</td>
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<td>HOLD TIMES</td>
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<td>SETUP TIMES</td>
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<td>PULSE WIDTH</td>
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<td>READ OPERATION</td>
<td>rd</td>
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<tr>
<td>WRITE OPERATION</td>
<td>W</td>
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<tr>
<td>CYCLE</td>
<td>c</td>
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<tr>
<td>ADDRESSES</td>
<td>A</td>
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<td>DATA</td>
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The abbreviations listed in Table 1 will help you decipher the timing specifications. For example, the minimum pulse width during which the CAS line is low is abbreviated as "tw(CL)." The w indicates pulse width, the C indicates CAS, and the L means "low." Similarly, the setup time for a row address is abbreviated as "tsu(RA)."

To accommodate a DRAM's timing requirements, the memory system requires a DRAM controller, which generates the control signals and interfaces the DRAM to the system's CPU. Some CPUs, such as the Z80, include a DRAM controller on chip. Most CPUs, however, require an external circuit that functions as the DRAM controller. The controller must coordinate the system access while guaranteeing that the DRAM is refreshed within its specified period. Ideally, the DRAM controller fools the system CPU into believing that it's communicating with an SRAM.

To use a DRAM effectively, you must pay attention to a number of timing parameters. The read cycle is probably the easiest of these parameters to understand, and it also demonstrates many of the DRAM's timing principles. Fig 1 shows the timing parameters for a 256k-bit DRAM (the TMS4256-12).

**Reading and writing**

A read cycle begins when the controller issues a row address and drives the RAS line low, thus strobing the address into the DRAM. The address must be stable for tsu(RA) seconds (row-address setup time) before the falling edge of the RAS line, and it must remain stable for a minimum of th(RA) seconds (row-address hold time) after the falling edge (Fig 2a). The RAS line must remain low during the entire read cycle. Because the CAS line not only strobes in the column address but also enables the output buffer, it should be high when strobing the row address into the DRAM. Keeping the CAS line high ensures that the Q output is in a high-impedance state.

Next, the controller must issue a column address to the DRAM. Once the column address is stable for the minimum setup time of tsu(CA) seconds, the controller drives the CAS line low to strobe the address into the DRAM. The falling edge of the CAS line should not occur any sooner than tRLCL (RAS-low to CAS-low time) seconds after the falling edge of the RAS line (Fig 2b). Because the CAS line also enables the output buffer, the WRITE line should be high in order to activate the read cycle when CAS is low. After the falling edge of the CAS line, there is an access delay of ta(C) seconds before the output buffer is enabled.

To ensure that the output data is valid, you must observe one more critical timing parameter, ta(R). This parameter specifies the minimum time that must elapse after the falling edge of the RAS line before the output data is valid. Even though the controller satisfies the requirements for the other delays, such as ta(C), the output data is not valid until ta(R) seconds. For this reason, manufacturers quote ta(R) when specifying a DRAM's speed.

Fig 2—The timing diagrams for a DRAM's read cycle illustrate many of the device's timing constraints. The timing parameters shown here are for the TMS4256-12 DRAM's RAS (a) and CAS (b) lines, which strobe a row and a column address, respectively, into the DRAM.
The DRAM's multiplexed-address arrangement conserves package size.

To understand the importance of the \( \tau_a(R) \) parameter, consider the following example. The TMS4256-12 DRAM specifies a minimum time of 25 nsec for the \( \tau_{RLCL} \) parameter, and it specifies \( \tau_a(C) \) as 60 nsec. Therefore, data appears at the output 85 nsec after the falling edge of the RAS line. However, the DRAM's \( \tau_a(R) \) specification is 120 nsec. Even though data is available at the output 85 nsec after the falling edge of the RAS line, it is not valid until 120 nsec after the falling edge—an additional 35 nsec (Fig 3a).

To terminate the read operation, the controller must bring the RAS and CAS lines high. Each line, however, must remain low for a minimum pulse width (\( \tau_{RL} \) and \( \tau_{CL} \), respectively) before returning to the high state. For the TMS4256-12 DRAM, \( \tau_{RL} \) and \( \tau_{CL} \) are specified as 120 nsec and 60 nsec, respectively. In addition, the RAS line should not return high until \( t_{CLRH} \) seconds (CAS-low to RAS-high time) after the falling edge of the CAS line. Similarly, the CAS line should not return high until \( t_{RLCH} \) seconds (RAS-low to CAS-high time) after the falling edge of the CAS line. For the TMS4256-12, \( t_{CLRH} \) and \( t_{RLCH} \) are 60 nsec and 120 nsec, respectively (Fig 3b).

Returning the CAS line high disables the DRAM's output buffer. However, the output line is not in a high-impedance state until \( t_{dis(CH)} \) seconds (disable time after CAS-high) after the rising edge of the CAS line. A typical value for \( t_{dis(CH)} \) is 30 nsec.

Driving the RAS and CAS lines high does not completely terminate the read cycle. The next cycle can't begin until the DRAM automatically writes data back into the previously accessed location during the pre-charge period. The precharge period occurs while both the strobe lines are held high for a minimum specified pulse width, \( \tau_{RH} \) and \( \tau_{CH} \). For the TMS4256-12 DRAM, \( \tau_{RH} \) is 100 nsec and \( \tau_{CH} \) is 25 nsec. Because \( \tau_{RH} \) is longer, you must observe it when calculating the read-cycle time.

The only restrictions placed on the WRITE line during the read cycle are that it must be high for \( t_{su(rd)} \) seconds before the falling edge of the CAS line, and that it must remain high for \( t_{th(CHrd)} \) seconds after the rising edge of the CAS line. Because the TMS4256-12 specifies these times as 0 nsec, the WRITE line must simply be high during the time that CAS is low.

You can now piece together the timing parameters for determining the DRAM's minimum read-cycle time. Because \( \tau_a(R) \) is longer than the sum of \( \tau_{RLCL} \) and \( \tau_a(C) \) for the TMS4256-12, it dominates this portion of the cycle. The remainder of the cycle consists of the 25-nsec \( \tau_{CH} \), the 100-nsec \( \tau_{RH} \), the 60-nsec \( t_{CLRH} \), and 30-nsec \( t_{dis(CH)} \) minimum time periods. Because all of these time periods occur simultaneously, and \( \tau_{RH} \) is the longest period that must be maintained, the read cycle consists of the sum of \( \tau_a(R) \) and \( \tau_{RH} \), or \( 120 + 100 = 220 \) nsec. Strictly speaking, you should add the maximum time allotted for the RAS to make a transition between logic levels; this maximum time is specified as 5 nsec. Adding 5 nsec for each of the cycle's two transitions produces a minimum read-cycle time of 230 nsec (Fig 4).

Writing to a DRAM involves most of the same timing parameters that a read operation does. The primary difference between the read and write operations lies...
in the timing parameters associated with the WRITE line. Essentially, you can use one of two methods to write to a DRAM—the early-write cycle or the delayed-write cycle. Your choice of write cycle will depend on your application (see box, "Weigh early- vs delayed-write cycles").

The early-write and delayed-write cycles are distinguished by whether the WRITE line is asserted before or after the CAS line is asserted. During an early-write cycle, the controller drives WRITE low prior to driving CAS low. Fundamentally, the falling edge of the CAS line strobes the input data into the DRAM and acts as a reference for the address setup and hold times. During a delayed-write cycle, WRITE strobes the data into the DRAM after the controller asserts the CAS line low. The address setup and hold times are referenced to the falling edge of the WRITE line.

During a delayed-write cycle, CAS is low for a certain time while WRITE is high, so the output drivers are briefly enabled as if the DRAM were executing a read operation. Therefore, unless the memory array has separate input and output buses, the delayed-write operation can cause bus conflicts (Fig 5). In the early-write cycle, the output drivers are not enabled, because the controller asserts the WRITE line low before setting the CAS low. Therefore, you can tie the D input line directly to the Q output line in order to accommodate a bidirectional bus.

The WRITE line must remain low for at least the period specified by tw(W). (For the TMS4256-12, tw(W) is specified as 40 nsec.) During a delayed-write cycle, the WRITE pulse must also remain low for tw(CLW) and tw(RLW) seconds after the falling edges of the CAS and RAS lines, respectively. (For the TMS4256-12, tw(CLW) is 35 nsec, and tw(RLW) is 95 nsec.) Further, the falling edge of the WRITE line must occur at least tsu(WCH) and tsu(WRH) seconds, respectively, before the CAS and RAS lines return to their high states. Both these setup times are specified as 40 nsec for the TMS4256-12 DRAM.

In a delayed-write cycle, the data must be stable for at least tsu(D) seconds before the falling edge of the WRITE pulse, and it must remain stable for at least tw(WLD) seconds after the same falling edge. The TMS4256-12 specifies tsu(D) as 0 nsec and tw(WLD) as 35 nsec. Because there is no time limit on the WRITE pulse after the CAS line is driven low, the write operation can be delayed for as long as the refresh period demands.

Don't forget to write

The difference between the early-write cycle and the delayed-write cycle lies mainly in the data setup and hold requirements. In the early-write cycle, the data must be stable for at least tsu(D) seconds before the falling edge of the CAS line. In addition, the data must remain stable for at least tw(WLD) seconds after this falling edge and also for tw(RLW) seconds after the falling edge of the RAS line. The th(CLD) and th(RLD) specifications for the TMS4256-12 are 35 nsec.
Besides multiplexed addressing, the most significant differences between SRAMs and DRAMs lie in the devices' refresh and precharge requirements.

![Diagram](image)

**Fig 6**—In the early-write cycle, the DRAM controller drives the CAS line low after it sets the WRITE line low. Therefore, the DRAM's Q-output buffers remain in the high-impedance state.

and 95 nsec, respectively. **Fig 6** shows a complete early-write cycle.

Like the read-cycle time, the minimum \( tw(RL) \) time exceeds the sum of the other overlapping timing parameters once the controller drives the RAS line low. Therefore, you calculate the minimum write-cycle time (\( tw(W) \)), by simply adding \( tw(RL) \), \( tw(RH) \), and the edge-transition times. The minimum write-cycle time for the TMS4256-12 is 230 nsec \((120 + 100 + 2 \times 5 = 230)\). Because \( tw(RL) \) is the dominant write-cycle timing parameter, the minimum write-cycle time is the same for both the early- and the delayed-write cycles.

Before you can read or write to a DRAM, the DRAM controller must execute a power-up sequence that initializes the data in the DRAM. The sequence consists of a short delay followed by a number of write cycles, which charge the memory-cell capacitors. The TMS4256 specifies the delay as 200 \( \mu \)sec plus eight initialization cycles. If you don't include the power-up sequence in the design, a diagnostic test will erroneously detect failures in a perfectly good memory system.

### The pause that refreshes

The DRAM controller's highest priority task is to ensure that the DRAM experiences a complete refresh cycle during the specified refresh period. A refresh can occur through a read or write operation or through a specific refresh operation. The TMS4256-12 specifies a refresh period of 4 msec. Because the DRAM's internal architecture has two simultaneously addressed memory banks, the controller needs to refresh only 256 rows during the 4-msec period.

When the controller accesses a row during the refresh cycle, it must adhere to the same timing constraints that it observes for the read and write cycles. Therefore, refreshing all the rows in the TMS4256-12 DRAM takes \( 256 \times 230 \) nsec = 58.8 \( \mu \)sec. This worst-case refresh-cycle time (58.8 \( \mu \)sec) occupies 1.5% of the allotted 4-msec refresh period. Slower versions of the same DRAM have the same 4-msec refresh-period specification, but occupy a greater bandwidth because of the longer access times.

RAS-only refresh is one of a variety of methods for refreshing DRAMs. In this method, the controller holds the CAS line high while using the RAS line to strobe a row address into the DRAM. The controller remembers which rows have been accessed during a refresh period to ensure that it services all the rows (Fig 7a). The DRAM's output drivers are never enabled during a refresh, because the CAS strobe is always high. The minimum time it takes to refresh an entire row is the same as the minimum read-cycle time.

The hidden-refresh method attempts to make refreshing transparent by inserting a refresh cycle when the CPU is decoding an op code after a memory read (Fig 7b). For many of today's high-speed \( \mu \)Ps, this method is too slow to be practical. The controller initiates the refresh by strobing a row and a column address into the DRAM during a standard memory-read operation. However, instead of going high again at the end of the cycle, the CAS line remains low, latching the output data on the Q bus. Subsequently, the controller toggles the RAS line, causing the DRAM to generate a row address internally. The DRAM contains an internal address generator that sequentially generates a row address on each rising edge of the RAS line when the CAS line is low. During this time, the DRAM ignores the external address bus. Because the DRAM's output drivers are activated throughout the entire cycle, hidden refresh consumes more power than RAS-only refresh.

Automatic CAS-before-RAS refresh combines the best aspects of RAS-only refresh and hidden refresh. In this method, the controller initially asserts the CAS line low before asserting the RAS line low. The DRAM's internal address generator then sequentially generates the row addresses after the controller has toggled the RAS line. Because this method asserts the CAS line low when the RAS line is high, the DRAM's
output drivers are not enabled, and the DRAM maintains low power consumption (Fig 7c).

**Tradeoffs, tradeoffs, tradeoffs**

The previous refresh methods access the rows in the DRAM at selected intervals within the refresh period. For example, a controller can refresh a TMS4256-12 by using RAS-only refresh every 4 msec/256 = 15.6 µsec. The controller must contain a row sequencer in order to implement RAS-only refresh. At selected intervals, it must multiplex the row sequence to the address bus. Hidden-refresh and automatic CAS-before-RAS refresh rely on the DRAM's having an internal row sequencer; the controller design is therefore less complicated.

Instead of refreshing the DRAM at selected intervals, burst refresh rejuvenates all the rows in one burst. Although this method furnishes the CPU with a longer period of uninterrupted access time, it produces a very long latency period if the CPU desires access to the DRAM during the refresh burst. Therefore, burst refresh is used only in applications in which the long uninterrupted access time is a must.

Some refresh methods even scrub the data in the DRAM, occasionally removing any soft errors incurred over time. DRAMs are more susceptible to soft errors than are SRAMs. Soft errors are often caused by alpha particles that are emitted by radioactive impurities in a DRAM's package. Although the probability of an individual soft error is small, the cumulative probability of an error increases as the memory size increases. During a scrubbing refresh cycle, the controller reads the accessed data and provides error detection and correction (EDC). The controller then rewrites any corrected data back into the DRAM.

Besides offering various refresh methods, modern DRAMs provide an assortment of modes for accessing data in the storage cells. (Table 2 summarizes many of the advantages and disadvantages of the available DRAM access modes.) To enhance the access speed, all of these modes rely on the principle that it's not necessary to strobe both the row and the column addresses into the DRAM when you access small portions of consecutive memory space. By eliminating some of the address strobes, these access modes shorten the overall access time and reduce the overall precharge time. Because most DRAMs support only one option, the DRAM controllers for a particular design are often unique, preventing you from mixing DRAMs that have different access modes.

Page-mode memory access establishes a constant row address, while the controller strobos a series of
Performing a read operation from a DRAM cell causes the capacitor to discharge slightly.

column addresses into the DRAM (Fig 8a). The controller strobes both a row and a column address into the DRAM on the first access, but from there on, it strobes only column addresses into the DRAM (by using the CAS line) during access periods. The maximum permissible time for tw(RL) (the maximum time for the RAS line to remain low) determines the maximum number of columns that are accessible during one page-mode access period.

In page-mode access, the minimum cycle time for strobing a column address into the DRAM is the sum of the minimum tw(CH)P (the CAS-high pulse width in page mode), the minimum tw(CL) (the CAS-low pulse width), and the minimum time required for two edge transitions. For the TMS4256-12, this cycle time is 120 nsec. Because the maximum value for tw(RL) is specified as 10 µsec, the controller can address about 83 columns during a single page-mode access period.

In DRAMs that feature an enhanced page-mode option, the internal column-address latch is transparent when the CAS line is high. This arrangement gives the DRAM’s column decoder direct access to the address when the latch is in its transparent state. An access cycle begins immediately, therefore, when a valid column address appears on the address bus. The transparent latch eliminates the column-address setup-time constraint. The falling edge of the CAS line latches the column address, and the rest of the cycle behaves as a standard page-mode cycle (Fig 8b).

Some DRAMs feature a static-column mode for high-speed read and write access. These DRAMs have a 3-state input column-address buffer instead of a col-

**Weigh early- vs delayed-write cycle**

Most DRAMs offer both early- and delayed-write cycles. Which type of write cycle you choose will depend heavily on your application’s timing parameters and system architecture. For example, consider a system design that uses a CPU, such as an 8086 µP, that has a multiplexed address/data bus. The CPU communicates with external memory by placing a destination address on its I/O pins. After a suitable delay, it transmits data to or from memory by using the same I/O pins. An early-write cycle seems well suited for this application because it doesn’t need 3-state buffers for eliminating bus conflicts. In either case, you need a DRAM controller to coordinate the action between the two devices.

In the early-write cycle, the CPU initiates a write cycle by placing a row address on its I/O pins. The DRAM controller, which is located between the CPU and the memory, latches the address and begins an early-write cycle by driving the DRAM’s RAS and WRITE lines low. After the CPU places a column address on the bus, the controller latches the address. Before the controller can drive the CAS line low, however, it must wait for the CPU to multiplex the data onto the I/O pins. Once the controller determines that the data is stable, it can then drive the CAS line low for the minimum tw(CL) seconds. After this procedure, the controller can return the CAS, RAS, and WRITE lines to their high state.

Now consider using a delayed-write cycle under the same circumstances. Once again, the CPU initiates a write cycle by placing a row address on its I/O pins. The controller latches the address and begins a delayed-write cycle by driving the RAS line low. Because the controller holds the WRITE line high, it can issue a low on the CAS line while it’s waiting for the data to stabilize. By driving the CAS line low, the controller enables the DRAM’s output buffers. Therefore, your system requires additional 3-state buffers in order to prevent bus conflicts. When the controller detects that the data from the CPU is stable, it writes the data into the DRAM by driving the WRITE line low for a minimum of tw(WL) seconds during the remainder of the cycle.

In this sample application, the difference between an early-write cycle and a delayed-write cycle is the difference between the DRAM’s minimum tw(CL) and tw(WL) specifications. The TMS4256-12 DRAM specifies the minimum tw(CL) time as 60 nsec and the minimum tw(WL) time as 40 nsec. For this application, therefore, the delayed-write cycle is the cycle of choice, even though it will force you to use additional hardware, because it’s 20 nsec faster than the early-write cycle. For slower DRAMs, the difference can be even more pronounced.
### TABLE 2—COMPARISON OF DRAM MODES

<table>
<thead>
<tr>
<th>MODE</th>
<th>ADVANTAGES</th>
<th>DISADVANTAGES</th>
</tr>
</thead>
<tbody>
<tr>
<td>WRITE MODES</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EARLY-WRITE</td>
<td>CAN TIE DRAM INPUT TO OUTPUT, NO 3-STATE BUFFER NEEDED</td>
<td>SLOWER THAN DELAYED-WRITE</td>
</tr>
<tr>
<td>DELAYED-WRITE</td>
<td>FASTEST ACCESS</td>
<td>REQUIRES 3-STATE BUFFER</td>
</tr>
<tr>
<td>RAS-ONLY</td>
<td>LOW POWER; ALL Q BUFFERS ARE IN HIGH-IMPEDANCE STATE</td>
<td>EXTERNAL CIRCUIT MUST GENERATE ROW ADDRESS</td>
</tr>
<tr>
<td></td>
<td>DRAM GENERATES ROW ADDRESS INTERNALLY, SIMPLIFYING DRAM-CONTROLLER DESIGN; REFRESH IS HIDDEN DURING SLOW CPU CYCLES</td>
<td>Q BUFFER IS ON DURING REFRESH; HIGHER POWER THAN RAS-ONLY; USEFUL ONLY FOR SLOW CPUS</td>
</tr>
<tr>
<td>REFRESH MODES</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CAS-BEFORE-RAS</td>
<td>DRAM GENERATES ROW ADDRESS INTERNALLY, SIMPLIFYING DRAM-CONTROLLER DESIGN; LOW POWER</td>
<td>REQUIRES DRAMs THAT SUPPORT THIS MODE</td>
</tr>
<tr>
<td>BURST</td>
<td>AFTER REFRESH BURST, MEMORY IS AVAILABLE FOR MAXIMUM REFRESH PERIOD (4 TO 15 mSEC)</td>
<td>DURING REFRESH BURST, MEMORY IS UNAVAILABLE; REQUIRES SPECIAL DRAM CONTROLLER</td>
</tr>
<tr>
<td>SCRUBBING</td>
<td>PREVENTS SOFT ERRORS IN HIGH-RELIABILITY AND LARGE-MEMORY SYSTEMS</td>
<td>REQUIRES EXTERNAL EDC CIRCUITS; MEMORY ACCESS USUALLY SLOWER DUE TO EXTRA BUFFERS IN DATA PATH</td>
</tr>
<tr>
<td>PAGE</td>
<td>LOW POWER; ALLOWS RANDOM ACCESS WITHIN ANY ROW; DOES NOT REQUIRE SPECIAL DRAMs</td>
<td>NEEDS SOPHISTICATED DRAM CONTROLLER; ACCESS USUALLY SLOWER WHEN CONTROLLER ACCESSES RANDOM ROWS</td>
</tr>
<tr>
<td>ENHANCED PAGE</td>
<td>FASTER THAN PAGE-MODE SINCE COLUMN DECODE OCCURS BEFORE CAS; LOW POWER; ALLOWS RANDOM ACCESS WITHIN ANY ROW; DOES NOT REQUIRE SPECIAL DRAMs</td>
<td>NEEDS SOPHISTICATED DRAM CONTROLLER; ACCESS USUALLY SLOWER WHEN CONTROLLER ACCESSES RANDOM ROWS</td>
</tr>
<tr>
<td>ACCESS MODES</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STATIC-COLUMN</td>
<td>VERY FAST ACCESS: ALLOWS RANDOM ACCESS WITHIN ANY ROW</td>
<td>HIGH POWER BECAUSE Q BUFFERS ARE ON BETWEEN ACCESSES; REQUIRES 3-STATE BUFFERS, NEEDS SOPHISTICATED DRAM CONTROLLER, SPECIAL DRAMs; ACCESS IS USUALLY SLOWER WHEN CONTROLLER ACCESSES RANDOM ROWS</td>
</tr>
<tr>
<td>CYCLIC</td>
<td>FASTEST ACCESS FOR SYSTEMS DOING CACHE BURST FILL</td>
<td>NEEDS SPECIAL DRAMs; SOPHISTICATED DRAM CONTROLLER; IS SLOW IF ADDRESSES ARE NOT SEQUENTIAL</td>
</tr>
</tbody>
</table>

umn-address latch. When the CAS line is high, this input buffer is in the high-impedance state. The controller initiates the first static-column access by asserting the RAS line and then the CAS line. Holding both lines low throughout the access period, the controller accesses the subsequent columns by altering the column address. This method eliminates the setup, hold, transition, and precharge times associated with toggling the CAS line (Fig Sc).

Because DRAMs inherently can’t support both page-mode and static-column-mode access, you must choose the mode that best suits your system. Essentially, both modes provide the CPU with a low-cost cache memory by virtue of their fast access to a small block of the system’s memory (there are many columns within a single row). One factor in your choice is access-mode speed. Although static-column mode is faster than page mode (because static-column mode eliminates some timing restrictions), the controller must alter the column address quickly enough to realize the speed advantage.

Power consumption is another consideration. Because the output buffers are continually enabled during static-column access, a DRAM that uses static-column mode consumes more power than does a DRAM that uses page-mode access. In either case, when there are frequent row changes, both modes can often be slower than direct read and write cycles because of the extra overhead in the DRAM controller.

The TMS4256 DRAM’s architecture offers the use...
Ideally, the DRAM controller fools the system CPU into believing that it’s communicating with an SRAM.

DRAMs offer two other modes of access: byte mode and serial mode. Byte mode is identical to nibble mode, except that in byte mode, the DRAM contains an 8-to-1 multiplexer. To select the initial block, the 8-to-1 multiplexer selects data from one of eight memory blocks based on address bits \( A_8 \) and \( A_9 \). Serial mode is similar to byte mode, except that in serial mode, the controller can sequentially access all of the columns for a particular row address by toggling the CAS line. In serial mode, for example, a controller can access 512 bits in a 256k-bit DRAM (arranged as a 512-row \( \times \) 512-column array) by simply establishing a row address and toggling the CAS line 511 times (after the initial access).

**Some access-mode comparisons**

In sum, your application will ultimately determine the access mode you choose. All the modes have advantages and disadvantages, and the tradeoffs they present are the familiar ones: performance vs cost and complexity. Page-mode access, for example, requires one row and a separate column address for each location in the DRAM, whereas nibble mode requires only one address and four CAS strobes to access data. Therefore, nibble mode is faster than page mode for short, sequential read operations such as fetching 4 bytes of data for a 32-bit CPU via an 8-bit port. However, nibble mode requires a precharge period when the RAS line returns high after four successive reads.

Because page mode holds the RAS line low throughout the access period, it’s well suited to long, uninterrupted data transfers. Although nibble mode may be faster than page mode for long data transfers, when the DRAM controller employs nibble mode it must supply a new set of addresses on every fourth transfer. In addition, page mode can randomly access the columns within a row, whereas nibble-mode access is sequential.
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Static-column mode offers all of the speed advantages of nibble mode and also provides the random-access capability of page mode. Although static-column mode is more difficult to implement, it's rapidly becoming the mode of choice for high-speed memory systems.

Of course, a DRAM's cost, availability, packaging, and alternate sources will also weigh heavily in your choice of a memory unit for a particular application. Remember, however, that once you select a DRAM, your system's access mode is fixed. A page-mode DRAM, for example, can't operate in a system designed for static-column or nibble-mode DRAMs. You must customize the DRAM controller and the system architecture for your chosen access mode.

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Antialiasing filters reduce errors in A/D converters

The need for effective antialiasing filters closely matches the growing number of applications for A/D converters. These filters reduce converter errors by limiting the input signal bandwidth. To correctly specify the filter, you need to consider the appropriate frequency band and the filter's characteristics.

Robert W Steer Jr, Frequency Devices Inc

The growing number of applications for analog-to-digital converters (ADCs) in data-acquisition systems, image processing, and industrial controls is driving the need for antialiasing filters that reduce errors in many converter-based systems. By limiting the bandwidth of a converter's input signal, antialiasing filters inhibit the generation of false (aliased), low-frequency signals caused by too low a sampling rate ($f_s$).

Limiting the converter's input-signal bandwidth reduces the highest frequency ($f_m$) whose amplitude is greater than or equal to the weight of an LSB (least significant bit). Lowering $f_m$ reduces the rate at which the ADC must sample the input signal to avoid aliasing errors or at least to limit them to an acceptable level. Putting a value on the term “acceptable” requires a knowledge of the specific application and of sampling theory. (See box, “Sampling theory sets inviolable limits.”) A converter whose sampling rate is finite may be capable of error-free conversions, but if you present such an ADC with an improperly band-limited input signal, the output will contain aliasing errors.

Prefiltering lets a slower ADC do the job

At first glance, a faster A/D converter might appear to provide an obvious and immediate answer to the aliasing problem. However, if you can't accept lower resolution, you'll have to pay more for a faster ADC. Furthermore, regardless of how much you are willing to pay for a converter, you can't get one with unlimited speed or resolution. In addition, noise frequencies extend well beyond the sampling rate of present-day ADCs. The sampling-rate requirements imposed by broadband noise are important because aliased high-frequency noise components can “fold back” and appear as lower frequencies that you can't distinguish from valid sampled data. Moreover, the system itself can generate “spurs”—spurious high-frequency signals, which will introduce errors if aliased.

By precisely limiting the bandwidth at the input of the ADC, active lowpass filters can reduce the need for brute-force increases in conversion speed. The restricted bandwidth lowers the maximum frequency of signals and noise that reach the ADC's input, and hence reduces the sampling (conversion) rate needed to avoid aliasing. Lowpass filters can exhibit a virtually flat, non-attenuating passband response that extends from
An obvious solution to aliasing is the use of a faster ADC, but prefiltering the ADC’s input can let a slower converter do the job.

dc to the cutoff frequency $f_c$. Beyond $f_c$, the gain can roll off steeply at rates that exceed $-90$ dB per octave. However, for technical as well as economic reasons, a filter with a flat passband response and the steepest available stopband roll-off characteristic isn’t necessarily the best choice for a particular application.

By band limiting the ADC input, a prefilter (Fig 1), prevents the ADC from digitizing alias-producing signals. A properly chosen filter attenuates signal components at frequencies greater than $f_m$ to levels well below the quantizing threshold of the ADC. (Here $f_m \leq f_s/2$.) A binary-coded n-bit A/D converter digitizes

**Sampling theory sets inviolable limits**

Signal sampling, such as that occurring during A/D conversion, can generate lower frequency, in-band error signals when the sampled signal contains higher frequency components at or above half the sampling frequency, that is, above $f_s/2$. Fig A illustrates the alias that would result from a single-frequency sine wave sampled at too low a rate.

The sampling theorem, which deals with sampling at a theoretical, mathematical level, states that a signal sampled at a rate, $f_s$, equal to or greater than twice the maximum signal-frequency component, $f_m$, can be exactly reconstructed from the data samples. If frequency components greater than $f_s/2$ are present, they “fold back” into the 0-to-$f_m$ frequency band. Fig B illustrates a simple graphical derivation of the folding frequency ($f_f = f_m/2$).

Above $f_f$, aliasing commences as the first harmonic spectrum begins folding over into the original spectrum.

Conversely, sampling rates less than $2f_m$ introduce aliases in the sampled signal that begin at $f_s - f_m$ and range about each harmonic of $f_s$, extending to $nf_s + f_m$. (Here, $n$ equals the harmonic number.) Because you can’t distinguish the aliases from the valid data sharing the dc-to-$f_m$ passband, accurate retrieval of the original signal is impossible. In real-world situations, the input signals are usually nonsinusoidal, are often random, and always contain noise. The noise, randomness, and high-frequency components of such signals are all potential sources of aliasing.

The elimination of frequency components above $f_s - f_m$ requires a lowpass filter—usually one with sharp cutoff characteristics. With zero attenuation in its passband and infinitely sharp and deep attenuation beyond, the ideal filter of Fig Ca completely eliminates aliasing and passes all desired signals unattenuated. However, this ideal filter is not attainable. Fortunately, various filter designs approach this ideal closely enough to achieve control of aliasing.

The response of the real-world filter in Fig Cb more nearly represents the response of an actual, realizable antialiasing filter. The finite roll-off and attenuation floor allow higher frequency signal and noise components to arrive at the sampler input. In some cases, these components can cause aliasing. The quantizing threshold of the sampler—an A/D converter for purposes of this discussion—determines whether these signals will be digitized.
its analog input into $2^n$ discrete levels, with the $n$th or least-significant bit being the smallest resolvable level. The LSB has a weight of $1/2^n$ of the full-scale input voltage range and each higher order bit carries twice the weight of its lower order neighbor.

An ADC with a unipolar input range generates $2^n$ output codes as you vary the input from 0V to the full-scale voltage, $V_{fs}$. Ideally, the midpoint of each input increment occurs at an exact integer multiple of $V_{fs}/2^n$, and each output transition occurs at the exact midpoint of a given analog increment, or at a multiple of $V_{fs}/2^{n+1}$. Table 1 shows that the LSB threshold of a

![Diagram of an ideal antialiasing filter and a real-world filter](image)

**Fig C**—An ideal filter (a) removes all frequencies beyond its stopband edge. A real-world filter (b) can approach this ideal of infinitely sharp cutoff.
The role of an antialiasing prefilter is to minimize ADC errors by attenuating high-frequency signals before they reach the ADC.

10-bit ADC is 66 dB below $V_{s/2}$, which corresponds to $V_s/2048$. Theoretically, the ADC will not digitize any signal below this level.

The bandwidth-limited A/D converter

Determining the bandwidth limit to use with an ADC to achieve acceptable amounts of aliasing can be difficult because the signal and noise waveforms encountered in practice contain numerous frequency components with complex amplitude and phase relationships. These frequency components can combine in ways that conceal individual components, particularly those with higher frequencies.

Fortunately, many rules of thumb provide first-pass approximations of the required prefilter cutoff frequency for a given type of input signal. Some of these rules appear in Table 2. You should use these approximations only as starting points.

A perfect antialiasing filter simply does not exist no matter how you synthesize it. Indeed, even in theory, you cannot create a perfect lowpass filter; that is, one that has no passband attenuation, that has no passband phase shift (or whose passband phase shift varies linearly with frequency), and whose stopband attenuation is infinite. What’s more, the assumption of a sampling rate that exceeds all signal and noise frequencies rarely holds true in practice. Noise can attain frequencies higher than half of the conversion rate of any realizable ADC or other type of sampler.

In addition, all realizable filters require a brief (but finite) frequency span to reach a deep attenuation floor. Moreover, these filters can superimpose small amounts of noise and distortion on the signals they condition, and can thereby produce aliases. The practical prefilter fulfills its task in two ways: It reduces out-of-band alias-producing signals to less than the quantization threshold of the ADC, and it restricts the bandwidth of the ADC’s input signal without introducing unacceptable distortion.

Fig 2 focuses on the passband and the stopband edge of four popular, realizable active filter designs. The filters’ characteristics are discussed in detail further on. The passband is the range of frequencies over which the filter exhibits flattest gain and imposes least attenuation, typically 0 dB at and near dc. The passband of lowpass filters extends from dc to the stopband edge—the transition point where filter attenuation first increases sharply for a small frequency increase.

You can define the stopband edge and the passband

---

**TABLE 1—LSB WEIGHT VS FILTER ATTENUATION FOR A BINARY-CODED ADC**

<table>
<thead>
<tr>
<th>A/D Resolution (Bits)</th>
<th>LSB Weight</th>
<th>Approximate LSB Weight</th>
<th>$\frac{1}{2}$ LSB</th>
<th>Attenuation at $f_m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>$\frac{1}{256}$</td>
<td>$-48$ dB</td>
<td>$-54$ dB</td>
<td>$\geq -54$ dB</td>
</tr>
<tr>
<td>10</td>
<td>$\frac{1}{1024}$</td>
<td>$-60$ dB</td>
<td>$-66$ dB</td>
<td>$\geq -66$ dB</td>
</tr>
<tr>
<td>12</td>
<td>$\frac{1}{4096}$</td>
<td>$-72$ dB</td>
<td>$-78$ dB</td>
<td>$\geq -78$ dB</td>
</tr>
<tr>
<td>14</td>
<td>$\frac{1}{16,384}$</td>
<td>$-84$ dB</td>
<td>$-90$ dB</td>
<td>$\geq -90$ dB</td>
</tr>
</tbody>
</table>

**TABLE 2—APPROXIMATIONS OF PREFILTER CUTOFF FREQUENCY FOR VARIOUS INPUT WAVEFORMS**

<table>
<thead>
<tr>
<th>Input Signal</th>
<th>Prefilter Cutoff Frequency ($f_c \leq f_m$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulsating DC</td>
<td>Rate of Change (V/SEC)/1V</td>
</tr>
<tr>
<td>Sinusoidal</td>
<td>$1/\text{Period}$</td>
</tr>
<tr>
<td>Complex Periodic</td>
<td>$20/\text{Fundamental Period}$</td>
</tr>
<tr>
<td>Single Events</td>
<td>$1/\text{Pulse Width}$</td>
</tr>
</tbody>
</table>
ripple to comply with system accuracy requirements. (Passband ripple is the peak-to-peak variation in a filter's passband frequency response.) One popular method locates the stopband edge at the break (corner) frequency, \( f_c \), where attenuation first becomes 3 dB—that is, where, for a constant input amplitude, the filter’s output amplitude is 70.7% of its amplitude at very low frequencies. In commercial filters, passband ripple usually exhibits typical values of 0.2, 0.5, or 1 dB. To allow comparison of filter types, Fig 2 normalizes the four filter responses to coincide at \( f_c \).

An alternative method locates the filter’s stopband edge at the passband ripple frequency \( f_r \), the highest frequency at which the passband ripple remains within the filter’s passband-ripple (passband response flatness) specification. Applicable to curves 3 and 4 of Fig 2, this approach yields a narrower—but much flatter—passband than does the 3-dB method. To repeat, you can locate the stopband-edge frequency at an attenuation level dictated by system tolerances.

Fig 3 views the responses of Fig 2 over a wider bandwidth to allow a comparison of filter roll-off characteristics and the definition of two key frequencies for curve 4. For antialiasing applications, \( f_a \), the frequency at which attenuation first becomes 6\((n + 1)\) dB, is the next highest frequency of interest; \( n \) is the ADC resolution in bits. The final and highest frequency, \( f_8 \), the attenuation-floor frequency, locates the lowest fre-

![Fig 2](image)

**Fig 2**—The passband and stopband-edge characteristics of the four filter types differ greatly. The curves are normalized to -3 dB and are shown in an expanded view of the passband region.
In theory, you can exactly reconstruct a signal sampled at twice its maximum signal frequency.

Frequency at which the stopband response drops below a specified attenuation floor and remains there. The floor defines the minimum attenuation a filter imposes at and beyond $f_c$.

Three additional parameters can simplify filter selection. Bounded by stopband edge-frequency $f_1$ or $f_2$ and by $f_c$, the transition band, $B_t$, is, depending on the application, the range from $f_1$ to $f_2$ or from $f_1$ to $f_2$. This parameter measures the frequency span required to reach the attenuation floor. A narrower transition band provides faster roll-off and sharper, better-defined frequency discrimination.

The shape factor, $\Omega_s$, is the ratio of the attenuation-floor frequency, $f_2$, to either $f_1$ or $f_2$. (In equation form, $\Omega_s = f_2/f_1$ or $\Omega_s = f_2/f_2$.) Shape factor, which provides the designer with a scale factor, is a useful figure of merit for comparing filters and is another measure of a filter’s attenuation steepness or roll-off rate.

A lowpass filter is said to be monotonic within a specified frequency band when its attenuation beyond the stopband edge increases with increasing frequency. Curves 1, 2, and 3 of Fig 3 illustrate monotonic responses. Curve 4 shows a nonmonotonic response. Illustrating this relationship, Table 3 tabulates the shape factor of each filter, based on the ratio of the frequencies occurring at $-80$ and $-3$ dB ($\Omega_s = f_{-80}/f_{-3}$). The table includes comments about comparative behavior beyond the stopband edge.

---

**Fig 3**—The unique roll-off characteristics of each filter type determine the transition bandwidth as well as the shape and depth of the attenuation floor. Normalized to $-3$ dB, the curves are shown in a broadband view.
Table 3 shows that the Cauer elliptic filter (curve 4) rolls off fastest, the Chebyshev filter (curve 3) second fastest, the Butterworth filter (curve 2) third fastest, and the Bessel filter (curve 1) slowest. However, the attenuation of the Cauer elliptic filter is not monotonic because it varies in a cusp-like manner at frequencies above \( f_r \). Note, however, that the 7-pole, 6-zero, elliptic filter rolls off faster than its 8-pole monotonic companions.

In theory, the attenuation shown in the first three curves increases without limit as frequency increases, but the Cauer elliptic filter exhibits a finite attenuation floor. As shown later, the Bessel filter fills an important need, and the Cauer elliptic filter’s exchange of attenuation depth for faster roll-off is a worthwhile tradeoff for certain applications. Playing a key role in determining system bandwidth, transient response, and accuracy, the width and flatness of the A/D converter’s prefilter passband warrants a closer look. Fig 4 displays the same four curves normalized to their \(-80\)-dB frequencies.

With all filters normalized to \(-80\) dB at the attenuation-floor frequency, \( f_r \), Table 4 lists the passband of each filter and compares the ratio of the Cauer elliptic filter’s passband to that of each of the remaining filters at both the \(-0.1\)-dB and the \(-3\)-dB corner frequencies. The choice of these corner frequencies was arbitrary, based on the assumed requirement for passband

---

**Fig 4** — A broadband view normalized to a common \(-80\) dB attenuation floor more clearly illustrates the transition-band behavior of the four filter types.
The phase of a Bessel filter varies linearly with frequency within a ripple-free passband and delays passband frequencies by a constant amount of time.

amplitude ripple of 0.1 dB and 3 dB.

This table shows that the Cauer elliptic filter provides a 0.1-dB passband approximately 12 times as wide as the Bessel filter’s, five times as wide as the Butterworth filter’s, and 1.5 times as wide as the Chebyshev filter’s.

For a -3-dB corner, Table 4 shows that the width of the Cauer elliptic filter’s passband is approximately four times that of the Bessel’s, twice that of the Butterworth’s, and 1.5 times that of the Chebyshev’s. These ratios lead to the obvious conclusion that the Cauer elliptic filter surpasses the other designs for amplitude-critical applications.

Table 3—Comparison of Transition Band and Stopband Performance

<table>
<thead>
<tr>
<th>CURVE</th>
<th>FILTER TYPE</th>
<th>SHAPE FACTOR ( f_{-3dB} )</th>
<th>ROLL-OFF RATE</th>
<th>MONOTONIC</th>
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<td>2</td>
<td>8-POLE BUTTERWORTH</td>
<td>3.162</td>
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<tr>
<td>3</td>
<td>8-POLE, 0.1-dB CHEBYSHEV</td>
<td>2.183</td>
<td>NEXT TO FASTEST</td>
<td>YES</td>
</tr>
<tr>
<td>4</td>
<td>7-POLE, 0-ZERO, 0.1-dB CAUER</td>
<td>1.961</td>
<td>FASTEST</td>
<td>NO</td>
</tr>
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</table>

Though carefully controlled frequency response is important in some situations, many applications require the prefilter to transmit pulses faithfully, with little or no distortion. To achieve pulse fidelity, the filter must combine the linear phase response typical of the Bessel filter and the flat amplitude response of the Cauer elliptic, Butterworth, or Chebyshev filters. Although a linear-phase filter maintains the proper phase relationship among the frequency components of a pulse, such a filter exhibits a gain roll-off in the passband that can modify the amplitude relationship among the frequency components and prevent the filter from producing an output that faithfully reflects its input.

Moreover, at frequencies at and beyond the stopband edge, the response of linear-phase filters rolls off more gradually than does that of their amplitude-oriented counterparts. The resulting wider transition band degrades frequency discrimination by allowing higher-frequency, out-of-band, alias-producing signals to reach the ADC’s input.

Many compromise or “transitional” responses combine amplitude and phase or delay characteristics to meet specific requirements. Classical responses include those of Butterworth/Bessel, Paynter, equiripple-delay, parabolic, and Gaussian realizations. Fortunately, the previously discussed Bessel, Butterworth, Chebyshev, and Cauer elliptic designs serve most antialiasing applications well.

Classical filter designs up close

It is now appropriate to define the unique characteristics of each type of filter with the goal of making the best choice for a given set of system requirements. The Bessel, Butterworth, Chebyshev, and Cauer elliptic responses of Figs 2 through 4 are so-called classical responses that meet the needs of most antialiasing applications. The phase of the Bessel filter varies linearly with frequency within a ripple-free passband. This filter delays signals at passband frequencies by a constant amount of time. The linear-phase characteristic fulfills one requirement for faithful pulse reproduction, that of preserving the phase relationship among the frequency components that comprise the pulse. With appropriate attenuation characteristics, the Bessel filter produces a delayed (but accurate) replica of its input signal.

Linear phase and overshoot-free step response come at the expense of passband flatness and slower roll-off in the region of the -3 dB corner frequency, \( f_c \). The more gradual roll-off results in band limiting that is less sharp, or selective, than that of other types of filters. The roll-off of the linear-phase filter is, however, monotonic and approaches the slope of the Butterworth and Chebyshev designs: -6n dB/octave at higher frequencies. (In this case, \( n \) is the number of filter poles.)

The Butterworth filter, also known as a maximally flat-magnitude filter, exhibits a wider and flatter passband than does a Bessel design of the same order (the same number of poles). Continuing the comparison, the Butterworth filter rolls off monotonically, and much more sharply at the -3-dB corner frequency, \( f_c \), than does the Bessel design. In exchange for sharper band-limiting, the Butterworth filter’s phase varies nonlinearly with frequency; the delay is no longer constant, and the step response exhibits a moderate amount of overshoot. These characteristics present no problems for amplitude-based applications.

The Chebyshev filter exchanges the flat, ripple-free passband characteristic of the Butterworth filter for an even sharper roll-off rate at the stopband-edge frequency, \( f_c \). This design exhibits equal-amplitude ripple across the passband and a step response with even
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In real-world situations, the input signals are usually nonsinusoidal, are often random, and always contain noise.

more overshoot than that of the Butterworth design. In addition, passband delay is not constant—it increases with frequency. Again, the frequency-dependent delay is usually not a problem when you are primarily interested in the attenuation characteristics.

The Cauer elliptic active lowpass filter has the wide, nearly flat passband response and the extremely sharp roll-off characteristics that ideally suit amplitude-based antialiasing applications. This design exhibits equal-amplitude ripple in the passband (typically 0.1 dB) and extremely fast amplitude roll-off. (Equal-amplitude ripple means that there are several peaks and valleys in the passband amplitude response and that the ratio of the response magnitude at the maxima and minima is constant over all maxima and minima.) Compared with the preceding filter types, which can theoretically roll off without limit, the Cauer filter rolls off to a deep, finite, well-defined attenuation floor.

Transitional filters combine selected characteristics of classical responses to achieve specific band-shaping tasks. One practical example (Fig 5) combines the Bessel filter's linear-phase passband response with the Butterworth filter's sharper stopband roll-off. Many other combinations exist.

Without violating other system performance criteria, the correct antialiasing filter provides the passband, transition-band, and attenuation-floor characteristics required to adequately prefilter the signals supplied to an n-bit ADC. Alias prevention defines the transition-band and attenuation-floor requirements; system tolerances determine the required flatness of the passband.

System specifications define both the maximum allowable magnitude of passband ripple and the stopband edge frequency, \( f_s \) or \( f_r \). The stopband edge frequency defines the high-frequency limit of the passband and marks the beginning of the transition band.

To determine the type of filter required by a particular application, you must next deal with the following parameters simultaneously:

1. The number of bits, \( n \), of the A/D converter.
2. The sampling rate of the A/D system, \( f_s = \frac{1}{t_{sr}} \), where \( t_{sr} \) corresponds to the time from the start of one conversion to the start of the next one. This time interval, of course, depends on the ADC's conversion time, but it can also depend on other system parameters. Within the time interval, a successive-approximation ADC compares its analog input to the weighting of each bit and delivers an n-bit digital output that corresponds to the input's value at the time of sampling. This parameter affects both the conversion accuracy and the system's susceptibility to aliasing.

If no sample-and-hold circuit precedes the ADC, the duration of the A/D conversions must be short compared with the time required for the input signal to change by \( \frac{1}{2} \) LSB. In essence, when there is no S/H circuit, the sampling “window” of a successive-approximation converter is the same as the duration of a conversion. With a given value of \( t_{sr} \), an S/H circuit at the ADC input dramatically shortens the sampling

<table>
<thead>
<tr>
<th>TABLE 4—COMPARISON OF THE PASSBAND AND ATTENUATION-FLOOR SHAPE OF THE FILTERS</th>
</tr>
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<tbody>
<tr>
<td>RESPONSE CURVES</td>
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<td>2</td>
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<tr>
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</tr>
<tr>
<td>4</td>
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</tbody>
</table>

180 EDN March 30, 1989
Brooktree

Image Capture is out there.
The Butterworth filter exhibits a sharp, monotonic roll-off at the $-3 \text{ dB}$ corner frequency, but its phase varies nonlinearly with frequency.

Window and allows conversion of signals having much higher rates of change and much higher frequency content.

For alias-free conversion, the sampling rate, $f_s$, must exceed the highest in-band (passband) frequency, $f_m$, by no less than a factor of two: $f_s \geq 2f_m$. This equation relates the ADC's sampling rate to the maximum frequency present in the ADC's input signal at an amplitude greater than or equal to $\frac{1}{2}$ LSB.

3. A frequency span closely related to the transition band described earlier. The frequency band of interest in this case is that required for the filter's attenuation to increase from the value at the stopband edge to a value that attenuates signals above $f_m$ to less than $\frac{1}{2}$ LSB. Signals at frequencies above this band cannot produce aliases because, when they arrive at the ADC input, their amplitudes are too small.

Table 1 furnishes the values of the first parameter, the fractional and decibel (dB) weighting of $\frac{1}{2}$ LSB of an n-bit ADC. The right-hand column lists the attenuation required to reduce a signal at $f_m$ to below the ADC's threshold and, at the same time, defines the high-frequency bound of the transition band.

The value of the maximum frequency of interest, $f_m$, influences the value of the second parameter, $t_{sr}$ and its frequency equivalent, $f_{sr}$. When selecting $f_{sr}$, you may discover that you must choose between using a faster ADC and a prefilter—and you may actually need

![Diagram](image-url)

**Fig 5—This transitional filter approximates the linear phase (constant delay) of the Bessel response in the passband, combined with the sharper roll-off of the Butterworth filter beyond the passband.**
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The Cauer elliptic filter has a flat passband and extremely sharp roll-off characteristics that suit amplitude-based, antialiasing applications.

both. If you add a prefilter, you may find that it slows the system response significantly; the system's response can become essentially the same as that of the prefilter. To make an intelligent selection of a conversion rate and a prefilter response, you must determine the highest signal frequency that's important to the system's operation. The ADC must sample at a rate equivalent to at least twice this frequency. You must also determine the amplitude of unwanted and potentially alias-producing artifacts (both signal components and noise) present in the system, and you must select a filter that attenuates the artifacts to a value no greater than one-half that of the ADC's LSB.

The third parameter is, in effect, the shape factor $\Omega_\alpha$. $\Omega_\alpha$ is equal to the attenuation-floor frequency divided by the stopband-edge frequency. For the curves of Fig 3, the equation you use to obtain the shape factor is: $\Omega_\alpha = f_{sw}/f_{-3}$. Table 3 lists $\Omega_\alpha$ for the actual filter realizations discussed.

You can now select a filter type. Selection begins by comparing your requirements with the transition-band response of the devices listed in this table. Obviously, the linear-phase, 8-pole Bessel filter exhibits the slowest roll-off rate and is best suited to applications requiring faithful pulse reproduction. Knowing the transition band and the tolerance on passband flatness, you can now select the filter type that best meets the system requirements.

Note that the 7-pole, 6-zero Cauer elliptic filter rolls off faster than its 8-pole cousins and yields the widest

![Fig 6—Sampling imposes a sin(x)/x response on the sampled signal. Accurate reconstruction requires compensation for this effect.](image-url)
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The Cauer filter rolls off to a deep, finite, well-defined attenuation floor.

passband. The Cauer filter’s response suits applications requiring fast roll-off and the widest possible alias-free passband. The need for this type of filter grows as \( f_s/f_m \) approaches two.

Table 4 compares the passband of the four responses, normalized to \(-80\) dB, and provides a figure of merit for amplitude response. With reference to the 0.1- and 3-dB stopband-edge frequencies, this table lists the ratio of the Cauer elliptic filter’s passband to the passbands of the Bessel, Butterworth, and Chebyshev filters.

An example is useful

To illustrate a typical design approach, consider the definition of a prefilter for use with a 12-bit A/D conversion system that must digitize signals to 20 kHz without aliasing. The passband must extend from dc to 10 kHz and must exhibit no more than 0.1 dB of ripple.

Alias-free operation requires the attenuation of signals at and above the \( f_s \) of 20 kHz by no less than \( 6(n+1)\) dB = 6(12 + 1) dB = 78 dB. The applicable filter parameters include a stopband-edge frequency, \( f_s \), of 10 kHz, a passband ripple of 0.1 dB max, and a minimum attenuation floor of 78 dB at \( f_s = 20 \) kHz. The resulting shape factor is \( \Omega_s = f_{-78}/f_{-0.1} = 20 \) kHz/10 kHz = 2. The 7-pole, 6-zero Cauer filter easily meets these requirements.

The A/D converter must be able to sample at a minimum rate of \( 2f_{-78} \), or 40 kHz. This rate corresponds to a maximum A/D conversion time of 25 µsec, and a sampling window on the order of 10 nsec for 12-bit accuracy.

Other considerations

You should consider data reconstruction in the early phases of system design. Reconstruction is often necessary because the sampling rate and window modify a signal of frequency \( f \) in the same way as does a lowpass filter with the \( \sin(x)/x \) response shown in Fig 6. With \( x = \pi f/f_{sr} \), and nulls occurring at \( f_{sr} \) and its harmonics, the attenuation is equal to

\[
20 \log(\sin(\pi f/f_{sr})/\pi f/f_{sr}).
\]

Thus, at \( f_{sr} = 4f \), the attenuation is

\[
20 \log(\sin(\pi/4)/\pi(4)) = 0.9 \text{ dB}.
\]

Accurate reconstruction requires compensation for the losses caused by this effect. There are many recovery mechanisms, including the zero-order hold (a clocked digital-to-analog converter) and lowpass filters of various orders and complexity. All of these filters have the task of filling in the steps of the sampled waveform to smoothly replicate the original.

Certain filter parameters warrant attention. First, you must take care to ensure that the prefilter exhibits low distortion. The harmonics generated by a filter suffering from amplitude or rate limiting are likely sources of alias errors. You must therefore observe all of your chosen filter’s specified restrictions on output loading and such signal characteristics as peak voltage and slew rate.

Then, because noise contributes to aliasing and also degrades system sensitivity and dynamic range, you need to know how much noise your filter can produce. Fortunately, present-day lowpass active filters exhibit noise performance suitable for most applications.

Next, you should consider such filter parameters as input impedance, output impedance, and the initial value and temperature coefficient of the filter’s and ADC’s input offset voltages. Changes in the first two quantities can produce system gain variations. The others can cause dc baseline shifts.

A final consideration concerns the reproducibility of your product. You should know or determine how closely you or the filter vendor can match the characteristics of supposedly identical filters. With this knowledge, you can ensure compliance with system specifications in both single and multichannel configurations.

Reference


Author’s biography

Bob Steer is president and treasurer of Frequency Devices Inc in Haverhill MA—but those are only his official titles. In his 20 years at the company, he has always been active as a design engineer. He holds a BSEE from Merrimac College and MS and ScD degrees from MIT. Prior to founding Frequency Devices, he held positions in academia as an associate professor and as chairman of an EE department. Bob’s hobbies include boating and cycling.
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DOT CHARACTER DISPLAY MODULES

DOT MATRIX DISPLAY MODULES

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<tr>
<th>CHARACTER FORMAT</th>
<th>MODEL NUMBER</th>
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<td>256 x 64</td>
<td>(16,384 DOTS TOTAL)</td>
<td>YES</td>
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CIRCLE NO 57
Computer-aided production makes EEs smaller, faster
It's a sad fact that engineering schools give short shrift to the social graces. Yet, in your career, you're faced with the necessity of dealing with people, many of them highfalutin. This column, therefore, will give you the rudiments of etiquette, both to spare you embarrassment and to increase the likelihood of your keeping your job. This month, we'll explore how to act in a fancy restaurant.

1. Upon entering, show no signs of being impressed. Statements like, "Gosh, this is a beautiful, fancy place" are a no-no. Just raise your eyelids slightly and say something like, "Hmm—looks as though my decorator's been here."

2. Always carry a flashlight and a pair of scissors with you. Americans think dark restaurants are classy, so it's likely you won't be able to read the menu by the light of the small candle on the table. Using the scissors, cut out the price column from the menu. That way, the person you're with won't think you're price conscious. And never ask for a translation of items printed in French. Nod your head knowingly and order at random.

3. When you taste the wine the sommelier (wine steward) brings, chew it a while, then spit it on the floor. Then, even though you have no idea how good or bad the wine is, say something like, "Hmm—an impish little wine" or "Hmm—it has an imposing character that stops just short of ostentation."

4. When you eat your meal, be ambidextrous. Switching the fork from hand to hand after cutting your meat reveals your roots.

5. Finally, if your waiter's name is Jacques or Pierre, impress him and your dining companion by using a little French. Here are three phrases that are sure to go over big.
   - *Cette nourriture est abominable.*
     (set new-ree-tyur ett ah-bow-me-nah-bluh)
     This food is delicious.
   - *Je pense que je vais vomir.*
     (zhe ponss kuh zhe vay voh-meer)
     I think that I will return.
   - *Votre chef est un sacré imbécile.*
     (voe-truh chef ett unh sah-ray em-bay-seal)
     Your chef is a real genius.

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**ENGINEERS**

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<td>Yankee Stadium</td>
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Before setting up an appointment, simply find the gold star somewhere in this magazine and paste it on the entry certificate found somewhere else in the magazine. Then find the blue dot somewhere, and paste it on the gold star. To be eligible for the grand prizes, find the symbols of the Taj Mahal, Yankee Stadium, and Fort Knox somewhere in the magazine, and paste the symbol of your choice on the Grand Prize form found somewhere else. Then, stand on your head for 30 seconds while reciting "Beautiful Sleazonia." Finally, send proof that you're married with a combined income exceeding $80,000 and a copy of your mortgage, including all liens attached thereto, to

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President Bush has inherited the excruciatingly difficult task of reducing our country's $17 zillion deficit. His "1000 points of light" can only increase the debt—how much depends on the wattage of the lights. A plausible way to cut the deficit is to tax electronics end users who use circuits and systems that consume too much power, operate too fast, or use too many bits.

It's inarguable that our deficit is linked closely to our consumption of energy. Because we have 432 ready-to-go nuclear plants whose startups are blocked by picketers who yearn for a return to kerosene lamps, we must use fossil fuels to produce electricity, Ovshinsky notwithstanding. And because OPEC is poised to inflict another 70s-type punishment on us, we simply must reduce the power we consume. Some will say, "What's the problem? Now we have CMOS, so power consumption is going down."

True. But what most people don't realize is that our supply of C is dwindling rapidly. There's still plenty of N in the hills, but NMOS has fallen out of favor. So we must import a high percentage of the C we use in making CMOS ICs—hardly a way to reduce the deficit.

The ever-increasing speed of modern systems is inextricably tied to the rising consumption of power. What's needed, then, is a tax system that penalizes excessive power consumption and its bosom buddy, high speed. I propose that President Bush issue guidelines on IC speed. For example, he could impose a limit on A/D-converter speed in the form of a maximum resolution-frequency product. In my opinion, 315 CM (codes × MHz) is a reasonable figure. A 12-bit A/D converter, for instance, has 4096 codes. The 315-CM limit would restrict the converter's speed to 0.077 MHz, corresponding to a conversion time of 13 µsec.

Another factor tied to power consumption is bit count. The evolution of computer systems from 8 to 16 to 32 bits has been accompanied by significant increases in power consumption. The same is true for the ever-increasing RAM capacities in modern computers. A side effect of this insatiable demand for more and more bits is bit pollution. A large portion of these zillions of bits goes unused, and so we have the problem of bit disposal and its resulting pollution. Land bitfills are becoming exhausted; bit incinerators use fossil fuels and pollute the atmosphere.

A presidential commission could determine a reasonable progressive tax on the number of bits in a system. Another source of revenue would be a tax on bit disposal. This disincentive would provide an impetus for developing trinary (base-3), quadrary (base-4) and quinary (Schweppes) computers, which use fewer bits to process a given amount of data. Some other ways to reduce the deficit:

- Sell Silicon Valley to the highest bidder
- Raise engineers' income taxes to 90% of gross income
- Eliminate all taxes on management personnel. Management deserves the credit for the healthy state of American electronics, despite engineers' blunders; eliminating taxes on these business geniuses will provide incentive for making companies healthier yet.
- Impose an application fee of $1,000,000 per patent
- Restrict defense contractors' illegal overcharging to 20% of a contract's face value (unless the illegal overcharging is proven to be justified).

Bill Travis
Contributing Editor
COMPANY MARKETS DATA-DEGRADATION SYSTEM

A new data-acquisition board, dubbed "BarfData," is available from Data Distortion Inc (Chesterfield, MA), a company that specializes in PC-based analog-signal degradation. The board features 16 poorly multiplexed analog-input channels, a signal-degrading instrumentation amplifier, a track-and-hold distorting amplifier, and a 12-bit, nonlinear A/D converter. The input multiplexers are from the bottom of the barrel, and offer only 20-dB channel-to-channel isolation and 1 MO each of on- and off-resistance. By the time a signal reaches the instrumentation amp, it's tainted by pollution from adjacent channels and severely attenuated by the multiplexers' high on-resistance. The instrumentation amp's specs are as repugnant as the multiplexers'; for example, gain accuracy is ±48% and total harmonic distortion is -15 dB. The almost unrecognizable signal then goes to the track-and-hold amp, whose abominable pedestal, accuracy, and droop parameters introduce additional errors in the signal. Finally, the output A/D converter features nauseating differential and integral nonlinearity and misses at least 2011 of its 4096 codes. Explains Joe Signalicide, president of Data Distortion, "Any wimp can make a data-acquisition system whose output accurately represents the input codes; it's a real art form to take a perfectly pure input and turn it into a stench in the nostrils of the signal-processing community."—Bill Travis

EVERYBODY ACQUIRES EVERYBODY

In a startling press conference on April 1, a spokesman from Insiders Inc, a Wall Street illegal-insider-information trader, announced that every electronics firm in the US has concluded a leveraged buyout of every other firm. According to Insiders' Boesan Ivesky, top-secret negotiations for the buyouts have been going on for the past three years. The ramifications of the buyouts are unclear at this moment; what's certain, however, is that every firm plans to fire every other firm's management team. The implications for design engineers in the acquir(ed)(ing) companies are equally unclear. Ivesky revealed, however, that the industry plans to adopt a free-agent system similar to the one used in professional sports.—Bill Travis

IBM ANNOUNCES PS/1,000,000 SERIES

Big Blue set the computer industry on its ear on April 1, when the firm announced its new, PS/1,000,000 Series of personal computers. Designed to prevent cloning, the family uses a bus architecture called TeraChannel—a 128-bit bus structure that's covered by 967 patents, 401 copyrights, and two Emmy awards. Additional clone-thwarting measures include explosive cabinet bolts, an automatic videotape record of users, and a 1-time user oath (with Bible) administered by the firm's authorized value-depleted resellers (VDRs). According to Mr Large Blue of IBM, Microhard is developing a PS/1,000,000-compatible operating system called OS/1,000,000. Immediately after IBM announced the series, a consortium of personal-computer manufacturers (led by Compaq) revealed plans for a counterattack. The firms plan to introduce a 256-bit, open-architecture system that uses Intel's new 8,000,986 microprocessor, a 250-GHz IC that addresses 9,999,999,999,999,999 Tbytes of memory.—Bill Travis
Avoid burned-out ICs . . . also, how much for trade secrets?

Dear Abbott:
I have this problem with CMOS logic ICs. Every time I wire up a breadboard, I end up with one or more burned-out ICs. I've tried fusing the power supply and bringing the voltage up gradually, but nothing seems to help. Do you have any idea what I'm doing wrong?

Worried, Santa Clara, CA

Dear Santa:
Sure—you're not seasoning the CMOS ICs properly. It's a little-known fact that these circuits require some "stroking" before you can use them in an application. The procedure is simple: Wear shoes with leather soles and scuff them about 20 times on a nylon rug. Then run a nylon comb through your hair about 10 times. Now you're ready to season the ICs. Just hold one row of pins against a ground plane and touch the other row (the row with the input pins) with your index finger. You should have no more problems.

Dear Abbott:
I'm bewildered. First, we had the 150V supplies for powering vacuum-tube circuits. Then ±15V came along, and it seemed to be the ultimate solution. Now we have ICs that are powered from single 5V supplies, and some say the voltage will drop even further, say to 3.3V. What's your opinion about all these changes?

Concerned in New Jersey

Dear New:
Well, let's look at it from the standpoint of numerology. Consider the ratios of the successive power-supply voltage-span reductions—150V to 30V, a ratio of 5; 30V to 5V, a ratio of 6. Now hold on to your hat. What's startling is that the ratio of 5V to 3.3V is 1.5151515... , a never-ending number. Are you sitting down? There's more—it so happens that Ramus II, the father of astrological proctology, was born on May 6, 1515. If I were you, I'd run right out and play 5615 in the daily-numbers lottery.

Dear Abbott:
My boss and I have this argument going. We have an application for a large number of extremely fast flip-flops. I want to use an ECL gate array, and my boss is set on using a GaAs array. Who do you think is right?

ECL Advocate, High Power, CA

Dear ECL:
You're both wrong. The 6SN7 dual triode makes the best flip-flop in the world. You and your boss have the same problem: You're hung up on the latest, trendiest technology, and you've lost sight of tried-and-proven techniques. Get off the fad bandwagon and take some time to smell the filaments.

Dear Abbott:
I'm a circuit-design engineer in a defense-electronics firm, and I don't make enough money to make ends meet. The problem is, my wife likes Porsches, Perrier water, and expensive yuppie restaurants. So, I've begun selling some of our company's schematics to a bearded man named Boris. My question is, how do I determine how much to charge?

Entrepreneur, Profit Motive, CA

Dear Entrepreneur:
First, let's determine my share for not turning you in. I think 40% is equitable. The best way to set a price for stolen trade secrets is to charge by the IC count. That way, you'll have an incentive to maximize the number of ICs in the circuits you design. I feel $1000 per IC package ($10,000 for gate arrays) is fair. You'll receive the number for my Swiss bank account in the mail.

Dear Abbott is pleased to answer questions from engineers who are either too dumb or too lazy to solve their own problems. Send self-addressed stamped envelope and a blank, signed check.
Use a negative capacitor for useful, banal applications

Bill Travis, Contributing Editor

It's been 21 years since this editor, employed as a bizarre-product development engineer at Sprague Electric Co (North Adams, MA), serendipitously invented the MinusCap (Ref 1). This component resembles an ordinary capacitor in every way, except that its value is negative (for example, $-1 \mu F$). Fig 1 shows the startling results of applying a step signal to a series-RC integrator incorporating the MinusCap. Note that the output waveform has a negative time constant. This phenomenon is easy to explain—to preserve the negative exponent of $e$ in the expression $V_{out} = V_{in}(1 - e^{-t/RC})$, the time $t$ assumes a negative value.

An interesting aspect of the output waveform in Fig 1 is the fact that two output voltages exist simultaneously. A useful, albeit banal, application comes to mind. If you connect a lowpass and highpass dc-voltage filter to the output and buffer the outputs of the filters, you obtain a dual-voltage power supply. For example, assume the lower output voltage in Fig 1 is 5V and the upper one is 15V. A 5V lowpass dc filter with reasonably steep skirts will, for all intents and purposes, completely attenuate the 15V signal and pass the 5V level. And vice-versa for the 15V highpass dc filter.

Some applications suggested in Ref 1 include predictions of future noise spikes, scope probes with zero shunt capacitance (made by connecting an equal-value MinusCap in parallel with the probe's positive capacitance), and observations of future failures. The promise of a rosy future for the component, however, never bore fruit. The Department of Defense (DoD) seized all lab samples and notes, and put the material in the same storage facility that's housed the Lost Ark (Ref 2) since 1939.

Because of the USSR's development this year of the negative inductor and the imaginary resistor, the DoD...

Fig 1—This scope photo depicts the input and output waveforms of the $-1\mu F$ MinusCap; pay no attention to the phospher burn marks.
no longer considers the MinusCap to be a threat to national security. Development of paper, ceramic, and electrolytic negative capacitors is now underway at several manufacturers' facilities. At the mammoth EDN test lab, for example, this editor recently constructed some units that exhibit a $-1 \mu F$ value and effective series resistance of $-0.1 \Omega$.

Fig 2a shows a delay line constructed with 25-mH positive inductors and the $-1 \mu F$ MinusCaps. In Fig 2b, you see the results of applying a 10V step to the input of the line. The output step appears 3 msec before the application of the input. As seen in Fig 2c, the same results accrue when you apply a sinusoidal input to the input of the delay line (actually, the anticipation line)—the sinusoidal output appears at the output 3 msec before the application of the input. It's up to you to determine useful applications for such anticipation lines. One possibility is to detect changes in system logic states before they occur.

One final application possibility, one the DoD is studying very carefully, is in imaginary-frequency transmitters. The expression

$$f = \frac{1}{2\pi\sqrt{LC}}$$

gives the frequency determined by an LC tank in an oscillator. If the value of $C$ in the expression is negative, then the resulting frequency is, naturally,

$$f = -\frac{1}{2\pi\sqrt{L|C|}}.$$

The reason for the DoD's interest in such imaginary-frequency transmitters is the fact that their signals are detectable only by imaginary receivers, such as those the DoD often receives under defense contracts.

References

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ABERRANT DESIGN IDEAS

Gausser / degausser brightens color monitors

Ted Burton
Signetics

A small permanent magnet (the gausser), held in close proximity to the face of an operating color monitor, will produce a striking display of colorful patterns (Fig 1). Much to the chagrin of the gausser user, though, the colorful patterns turn into permanent color clouds when the gausser is removed.

Luckily for the gausser user, whose job might now be in jeopardy, it's easy to build a degausser from a 1000-ft roll of 30-gauge wire-wrapped wire. This degausser is not UL approved, it erases any magnetic medium within a foot or two, it uses potentially lethal voltages, it interferes with pacemaker operation, and it probably causes cancer or hair loss in laboratory rodents. However, it also removes the cited color clouds.

Fig 2 shows how to build the degausser and turn it on by sticking its two leads into an ac outlet. You should sweep the powered-up degausser past the face of the monitor for several seconds, then turn it off by pulling the leads out of the ac outlet. If the degausser is left running longer than a minute, the degausser and its operator will most likely start to smoke or burn. (Ed Note: The thought occurred to this editor: Why use the gausser in the first place? But that's pica-yune.)

Exploit Z80's hidden logarithmic mode

Jim Williams
Linear Technology Corp

The popular Z80 microprocessor contains a very powerful embedded routine dedicated to high-speed logarithmic functions. Because it operates in real time, it is significantly faster than lookup tables or computational approaches. Furthermore, it's directly addressable in analog format. All Z80 chips have this capability, although manufacturers do not supply the necessary data to exploit it.

The circuit in Fig 1 is a complete, real-time logarithmic ratio computer that uses fully parallel, coprocessing Z80s in the embedded logarithmic mode. Connecting an analyzer between the Z80's ground pin (pin 29) and the D1 data bus (pin 15) reveals the internal logarithmic instruction set. Figs 2a, 2b, 2c, and 2d show that the best performance occurs in the 300-nA to 750-µA range.

This designer (Ed Note: We must avoid writing in the first person at all costs), discoverer of the Z80's logarithmic mode, is ebullient. Everyone always told this designer that analog circuits were nowhere. Now this designer believes it. Microcomputers are great. You can do anything with them. Can you imagine what's possible with one of those 32-bit babies? This designer will bet that you can get another decade with
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ABERRANT DESIGN IDEAS

that 386 thing. After lunch, this designer is going to go over to Intel and apply for a job. This designer is also going to trade in his Tektronix 547 and 556 for a development system. But it's going to be tough to find one with those funny little dots on the CRT.

Fig 1—A couple of Z80s, configured as full parallel coprocessors, perform real-time logarithmic ratio computations.

Fig 2—After viewing these displays, this author now believes "microcomputers are great."
1 is impossible. 2 is undesirable. 3 is...

The choices don't appear to be very attractive, but the problem must be solved. An eight-second test time for all-code differential and integral non-linearity testing is out of the question for production testing. And it gets worse geometrically for higher-order converters: A 16-bit device would take 128 seconds.

What about your options? The A/D already spits out numbers ten times as fast as most testers can process them — especially with the single, general-purpose array processor typically used for this test. Testing less codes or reducing the amount of averaging would seriously diminish test quality.

Which leaves you with speeding up the tester. An option LTX has considered...
Hi.T, the high-throughput tester from LTX, gets a tenfold speed boost through a new technique: a local Digital Signal Accelerator that reads the A/D’s output directly and does the bulk of the calculation on the fly. Which leaves the downstream array processor to compute results on one tenth the original data — in one tenth the time of other testers.
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The Digital Signal Accelerator system is just one of the many local computers Hi.T uses to remove testing bottlenecks. Local processing helps Hi.T's parallel analog resources perform instant DC measurements. And local processing throughout the system cuts down the time it takes instruments to set up between tests.

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Network Software Associates Inc, 22982 Mill Creek, Laguna Hills, CA 92653. Phone (714) 768-4013.

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Syntest Corp, 40 Locke Dr, Marlboro, MA 01752. Phone (617) 481-7827. FAX 617-481-5769.

Circle No 370

EDN March 30, 1989
The board’s VME bus interface includes a 7-level interrupt handler and a single-level bus arbiter. Software support includes the OS-9 and PDOS operating systems, and debug monitor firmware. From $590 in OEM quantities.

Pep Modular Computers GmbH, Am Klosterwald 4, 8950 Kaufbeuren, West Germany. Phone (08341) 81001. TLX 541233. FAX 08341-40422.


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- Contains as much as 4M bytes of zero-wait-state RAM
- Comes with RAM utilities that include disk caching

The Bullet-386SX motherboard features a 16-MHz 80386SX µP and is available with 512k, 1024k, or 4096k bytes of dynamic RAM running with zero-wait-states. It also contains five IBM PC/AT compatible expansion slots as well as three IBM PC/XT compatible expansion slots. The motherboard’s dimensions conform to the IBM PC/XT motherboard form factor. It comes with a RAM utility package that includes disk caching, RAM disk, print spooling, and support for the EMS LIM 4.0 memory extension. It also has a socket for an optional 16-MHz 8087SX coprocessor. The board comes with a limited 2-year warranty. A motherboard with 512k bytes of DRAM and a 4-utility package costs $823, which includes a 50% discount for resellers on the first unit.

Wave Mate Inc, 2341 205th St, Suite 110, Torrance, CA 90501. Phone (213) 533-8190. FAX 213-533-5940.

Circle No 374

PGA VERIFIER

- Tests LCA designs for the IBM PC/AT
- Consists of a plug-in card, a pod, and a target-system probe

The Mesa I in-circuit PGA development tool for Xilinx’s Logic Cell Arrays (LCA) consists of an IBM PC/
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CIRCLE NO 48

EDN March 30, 1989

DOTRONIX INC.
160 First Street S.E. New Brighton, MN 55112
Service Locations:
Los Angeles, CA 0 San Jose, CA 0 Boulder, CO
Mpls./St.Paul, MN 0 Eau Claire, WI 0 New Jersey
AT-compatible plug-in card, a pod with 12 LCAs, and a probe with an LCA connector and socket for the target system. The tool lets you verify host-downloaded data, observe the register states in the target LCA, isolate signals from the target system and create states to isolate problems, and alter real-time designs. In addition, the unit serves as a breadboard for developing LCA designs. A shadow LCA acts as a mirror for the states in the target LCA. The company and Tektronix jointly developed a flex-circuit cable that connects the pod to the probe. The probe connector plugs into a PLCC socket on the target system. The Mesa I software, which runs under Windows, is compatible with Xilinx's design software, allowing it to extract symbolic information from XACT files. $9390. Delivery, eight weeks ARO.

Data I/O Corp, Box 97046, Redmond, WA 98073. Phone (206) 881-6444. TLX 152167. FAX 206-882-1043.

STD I/O CARDS

- Provide 16 optoisolated inputs and outputs
- Each output can switch 50V with 400-mA max load current

The 242-1 and the 342C-1 dual-port optoisolated I/O cards for the STD Bus provide 16 input and 16 output circuits arranged as two 8-bit ports. The 242-1 is compatible with the STD TTL Bus, and the 342C-1 is compatible with the STD CMOS Bus. You can configure the inputs to handle standard TTL inputs by setting an input threshold voltage to 1.4V. In addition, the inputs can handle industrial voltage swings by setting the threshold to 6.4V above industrial ground. The input circuits can withstand input voltages between -50 to +50V. The output circuits have Darlington open-collector arrangements with provisions to install pullup resistors. Each output can switch 50V at 400 mA max. Each of the two input and two output ports has its own power supply on board, which requires only a 5V signal from the bus. 242-1, $438; 342C-1, $486 (10).

Enlode Inc, 1726 Kingsley Ave, Orange Park, FL 32073. Phone (800) 874-7729; in FL, (904) 264-4405. FAX 904-264-0765. TLX 466036.

Circle No 376
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From product concept and design, through implementation, PADS-PCB shortens long design cycles by allowing the engineer to complete a job at one station with features such as:

- LOGIC CAPTURE
- PRINTED CIRCUIT BOARD DESIGN
- AUTOPLACEMENT
- 100% RIP-UP & RE-ROUTE AUTOROUTING
- AUTO CHECKING
- AUTOCAD INTERFACE

Utilizing a design-oriented database, PADS-CAE accesses all the sheets of a schematic simultaneously. Auto REF DES, Auto Gate Assignment and Data Checking across all sheets are also provided.

PADS-PCB is the most popular Printed Circuit Board Design System on the market and offers:
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*1 mil database-32" x 32" board size, 30 layers
*400 IC Circuit Size capability

*Automatic and Interactive Component Placement Aids, Track Routing, Design Rule Checking
*Complete SMD Capability
*1,2,3 Tracks between IC Pins
*Superb Analog Design Capability

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INSIDE MA: (508) 486-8929 or (800) 255-7814.

CIRCLE NO 46

SEE US AT ELECTRO/89 BOOTH#'s 164a, 168, 267, & 265!
Pushing the leading edge of display technologies, the Supertex family of HVMOS drivers permit major breakthroughs in electroluminescent, gas plasma, LCD & vacuum fluorescent displays. This advanced smart power technology also opens up a wide range of applications in medical ultrasound imaging, robotics, telecommunications, test systems, high performance printers, power supplies, motor controls and solid-state relays.

The Supertex high density HVMOS drivers, listed below, feature high speed with low power consumption to produce bright, high-resolution images. Investigate HVMOS . . . a most attractive alternative to cumbersome boards or hybrids.

For more information or custom designs, write or call: Supertex, Inc., 1225 Bordeaux Drive, Sunnyvale, CA 94088; Tel. (408) 744-0100; Telex 6839143 SUPTX and FAX (408) 734-5247.

<table>
<thead>
<tr>
<th>Part Number</th>
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<tr>
<td>HV04 &amp; 06</td>
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<td>HV08**</td>
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<td>160 to 400V</td>
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</tbody>
</table>

*HVMOS is a registered trademark of Supertex, Inc.
**Available 2nd Quarter, 1988
NEW PRODUCTS

INTEGRATED CIRCUITS

QUAD S/H AMPLIFIER
- Has 12-bit accuracy
- Acquisition time is 600 nsec
The AD684 quad S/H amplifier features 12-bit accuracy and a sampling rate to 100k samples/sec. Each channel of the AD684 has a guaranteed maximum acquisition time of 600 nsec to within 0.1%, and 1 µsec to within 0.01% for a 10V step. For simultaneous sampling, the AD684’s entire error budget is completely encompassed in a 300-psec max aperture offset between channels. A proprietary error-correcting architecture compensates for hold-mode errors and ensures 12-bit accuracy and repeatability. The AD684 has a maximum full-scale nonlinearity of 0.005%, and its hold characteristics include a 500-nsec maximum settling time, 200-psec aperture uncertainty, and a 10-nsec aperture delay. The IC operates from ±12V supplies and dissipates 630 mW max. Three temperature grades are available. From $23.50 (100).

Micro Linear Corp, 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200.

Circle No 352

LOG GAIN/ATTENUATORS
- Provide control from −24 to 24 dB
- Interface with 8- and 16-bit buses
The ML2008 and ML2009 amplify or attenuate analog signals to ±3V under µP control and are noiseraized at 900 nV/√Hz at 1 kHz. The devices provide automatic signal-level control from −24 to 24 dB in 0.1 dB steps. The ML2008 interfaces to an 8-bit µP bus, using two write operations to store nine gain-setting bits and a power-down bit. The ML2009 has a single 9-bit data register, which you can program with one write operation when using a 16-bit data bus. Both devices operate from ±5V supplies. 18-pin DIP or 20-pin plastic chip carrier, $5.50 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (508) 935-5565

Circle No 351

VIDEO CONTROLLER
- Features video rates to 120 MHz
- Supports high-resolution graphics
The IMS-G300 video controller supports high-resolution color graphics applications with resolutions of 640×480 (VGA), 1024×768, and 1280×1024 pixels. The highly integrated chip contains a 256×24-bit color look-up table, a programmable video-timing generator, a 32-bit multiplexed pixel port, a triple video DAC with 8-bit resolution, and an on-chip, phase-locked loop. The -G300 can handle video rates to 120 MHz and interlaced or noninterlaced video. The chip has four 8-bit pixel ports, which accept data directly from the video RAM array at 25% of the video rate. The pixel port has two software-selectable operating modes. Mode 1 sends the data via the 24-bit color look-up table, permitting the selection of 256 colors from a choice of over 16 million. Mode 2 sends the 24-bit data directly to the 8-bit video DACs, allowing the display of 16 million colors at any one time. The devices come in 84-pin PGA or LCCC packages. An 85-MHz part, $100 (1000).

Inmos Corp, Box 16000, Colorado Springs, CO 80935. Phone (719) 630-4215.

Circle No 353
THE SMALL AND THE MIGHTY

HIGH POWER SWITCHERS...FROM

Lighter...Smaller...More Powerful...
for single and three phase applications where high efficiency, precise regulation and a high degree of packaging density are required.

The EMS Series incorporates the best of customer tested and application proven features:

- 1kW, 10; 2.5kW, 10 and 30 in one unit;
- 5kW, 30
- Highest power per cubic inch for wide range, rack mount, CV/CC power supplies in the industry

- Common programming with TCR, EMHP, ATR and HCR Series
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- Built in OVP and thermal protections
- ...and much, much more

Want all the details on the small and the mighty? Write or call for the latest Tech Bulletin on the EMS Series of DC Power Supplies.

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CIRCLE NO 43
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ELECTRONIC MEASUREMENTS INC.

SCR REGULATED DC POWER SUPPLIES

SINGLE PHASE TCR
- 4 power levels 600 W - 1,000 W - 1,800 W - 2,800 W
- DC outputs variable over full range of 0 to 7.5 V DC through 0 to 2,500 V DC
- Regulated and metered (V and A)
- CVCC with automatic crossover
- Fully programmable and remote sense
- Complies with VDE 875-N and VDE 871-A
- 5-year warranty

THREE PHASE TCR
- 3 power ranges 2,500 W - 5,000 W - 10,000 W
- DC outputs variable over range from 0 to 6 V DC through 0 to 600 V DC
- Regulated and metered (V and A)
- CVCC with automatic crossover
- Complies with VDE 875-N and VDE 871-A
- 5-year warranty

EMS HIGH FREQUENCY SWITCHING DC POWER SUPPLY
- 48 models 600 W to 1,000 W to 2,500 W to 10,000 W
- Voltages from 7.5 V DC through 1,000 V DC
- High density packaging — up to 3.1 Wcubic inches at 5 KW
- Regulated and metered (V and A)
- Fully programmable and remote sense
- CVCC with automatic crossover
- 5-year warranty
- UL recognized

INTEGRATED CIRCUITS

DUAL AUDIO DAC
- Features 20-bit resolution
- Has two independent channels
The D20200 is a complete, dual, 20-bit, D/A-converter subsystem. The module includes two 20-bit DACs, a stable bipolar reference, a serial CMOS/TTL-compatible digital interface, and two distortion-suppressing output deglitchers/amplifiers. It needs no external components or trimming to meet its specifications; you only need to connect ±15 and 5 V power supplies, a serial data source, and appropriate timing signals. The D20200 handles output signal amplitudes from 0 to -60 dB. Total harmonic distortion and noise is typically -90 dB at -20 dB output and -52 dB at -60 dB output. Differential nonlinearity is typically ±0.0002% of FSR. The D20200’s serial interface accepts digital word lengths from 16 to 32 bits, and it accepts simultaneous or multiplexed data at a 15-MHz maximum clock rate. It converts at rates from dc to 200 kHz per channel and accepts digital coding formats of two’s-complement, offset binary, or complementary offset binary. $199 (100).

UltraAnalog Inc, Box 14164, Fremont, CA 94539. Phone (415) 657-2227.

Circle No 354

STATIC RAM
- Features access time as low as 55 nsec
- Operates over the military temperature range
Targeted for use in military and aerospace applications, the MS-8128SC 128k x 8-bit high-speed static RAM has an operating temperature range of -55 to +125°C and can be screened to MIL-STD-883C requirements. It is available with access times of 55, 70, 85, 100, 120, or 150 nsec and has TTL-compatible inputs and outputs. The device is manufactured from four 32k x 8-bit RAMs packaged in ceramic leadless chip carriers that are bonded to a single 32-pin ceramic DIP substrate that also carries chip-select decoding logic and power-supply decoupling capacitors. Operating at a clock frequency of 1 MHz it consumes 150 mW of power from one 5 V supply; in standby mode, it consumes 2 mW. A low-power version, which consumes only 40 µW in standby mode, is available for applications that use battery backup. From £145 to £290 (100).

Hybrid Memory Products Ltd, Elm Rd, W Chirton Industrial Estate, N Shields, Tyne and Wear NE29 8SE, UK. Phone 091-258-0690. TLX 53206. FAX 091-259-0997.

Circle No 355

ANALOG MULTIPLEXERS
- 100Ω on-resistance
- 250 nsec switching times
Pin compatible with the industry-standard DG508A and DG509A, the DG408 and DG409 analog multiplexers offer improved specifications compared to earlier types. The on-resistance of the DG408/409 is only 100Ω, leakage current is less than 0.5 mA, switching time is 250 nsec, and power dissipation is only 2.5 mW. The DG408 is an 8-channel, single-ended device with a 3-bit binary address. The DG409 is a 4-channel, differential device with a

Circle No 356

INTEGRATED CIRCUITS

DUAL AUDIO DAC
- Features 20-bit resolution
- Has two independent channels
The D20200 is a complete, dual, 20-bit, D/A-converter subsystem. The module includes two 20-bit DACs, a stable bipolar reference, a serial CMOS/TTL-compatible digital interface, and two distortion-suppressing output deglitchers/amplifiers. It needs no external components or trimming to meet its specifications; you only need to connect ±15 and 5 V power supplies, a serial data source, and appropriate timing signals. The D20200 handles output signal amplitudes from 0 to -60 dB. Total harmonic distortion and noise is typically -90 dB at -20 dB output and -52 dB at -60 dB output. Differential nonlinearity is typically ±0.0002% of FSR. The D20200’s serial interface accepts digital word lengths from 16 to 32 bits, and it accepts simultaneous or multiplexed data at a 15-MHz maximum clock rate. It converts at rates from dc to 200 kHz per channel and accepts digital coding formats of two’s-complement, offset binary, or complementary offset binary. $199 (100).

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Circle No 356
INTEGRATED CIRCUITS

2-bit binary address. In addition to specification improvements, the DG408 and DG409 feature reduced sensitivity to electrostatic discharge (ESD) and the ability to withstand ±400V on all pins (with respect to ground). Both TTL-compatible multiplexers conduct current equally well in both directions and allow operation with supply voltages to ±15V or with 12 and 0V unipolar supplies. 16-pin DIP and small-outline packages, $4.68 to $15.92 (100).

Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 357

OCTAL 8-BIT DAC

• Includes output buffers
• Has µP interface logic

The AD7228 CMOS IC features eight fully independent 8-bit, voltage-output D/A converters with output buffer amplifiers in a 24-pin DIP, SO package, or plastic leaded-chip carrier. The AD7228 requires no external trims or components to achieve full specified performance and guaranteed monotonicity with any of the standard 5, 12, or 15V supplies. Each of the eight DACs has an individual latch that accepts and holds data written by the system µP, similar to an address in system memory. Because the AD7228 works with a write-pulse width of 95 nsec, it is compatible with most µPs. Each DAC can provide an output to 10V for a 2-kΩ and 100-pF load at a slew rate of 2 V/µsec and a settling time of 5 µsec. The AD7228 is available in grades of ±1 LSB and ±2 LSB, and in three temperature ranges. $32 to $37.50 (100).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 358
Micron just broke the SRAM speed barrier with our family of leading edge, super high speed CMOS SRAMs.

We've applied the same state-of-the-art design and process technology used for our high quality DRAMs in development of our fast static RAMs — with some amazing results.

At an incredible 25ns for 256K and 15ns for 64K, our SRAMs are breaking speed records. And we're not just sampling product, we're shipping production volumes.

Choose from a wide variety of components in DIP, SOJ and LCC packages, with densities from 16K to 256K and organizations of x1, x4 and x8.

And like all Micron memory products, our SRAMs are backed by the type of strong sales, customer service and technical support that keeps you on the leading edge.

For additional information on how you can break the SRAM speed barrier, call 208-386-3900.

*Slower speeds also available.

**Available Now**

**256K 25ns / 64K 15ns**

<table>
<thead>
<tr>
<th>Part #</th>
<th>Organization</th>
<th>Speed*</th>
<th>Packages</th>
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<tbody>
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<td>15ns</td>
<td>PDIP, CDIP, SOJ</td>
</tr>
</tbody>
</table>

*Slower speeds also available.*
The only way our bright new 8050 display looks anything like the others is through a pair of sunglasses.
That’s because the 8050 is without a doubt the brightest, most readable display in its class.
It’s the first 10-inch, AC-memory, flat panel display to deliver 640 x 400 resolution with an extraordinary 44 foot-lamberts of brightness. Along with a contrast ratio of greater than 20:1. All in a package just over one inch thick.
In fact, the only thing more impressive than these numbers is looking at the display yourself. Then you’ll really appreciate its exclusive solid black background. And the brightness and flicker-free clarity of text and graphics.
And what’s truly amazing is that you’ll get this remarkable performance under some of the worst possible conditions. Like bright sunlight. And viewing angles up to 120 degrees.
So if your application calls for the clearest images with maximum contrast, call us today at 1-800-556-1234, Ext. 238. Inside California call, 1-800-441-2345, Ext. 238. Or write Fujitsu Component of America, Inc., 3330 Scott Boulevard, Santa Clara, CA 95054-3197.
We’ll brighten your day.

CIRCLE NO 40

Fujitsu Component of America Inc.
NEW PRODUCTS
COMPONENTS & POWER SUPPLIES

FIBER-OPTIC LINK
• Operates over 2 km
• Offers user-selectable inputs
This fiber-optic link provides an RFI/EMI-secure circuit for Electro-Systems' MLP-1 phone and its associated PBX. The link consists of the F9765 and the F9766 and has a transmission capability of 2 km min. The F9765 is designed for use at the PBX end of the circuit and includes a male 25-pin connector. The F9766 is located at the phone and features a female 25-position connector. The circuit has a 0.3- to 3.5-kHz bandwidth and outputs 0 dBm into a balanced 600Ω load. Each unit consists of two pc boards. The first board holds the power supply and the digitizing and multiplexing circuitry, and the sec-

DISPLAY MODULE
• Features VT320 emulation
• Includes touch-input system
The M320ST electroluminescent display module provides graphics capability and VT320 emulation with standard 80-character × 25-line text. It also features an infrared touch-input system, SealTouch, that provides a resolution of 2000 touch points. SealTouch firmware allows you to program button sizes, positions, and response. You can have as many as 120 pages with a maximum of 120 buttons/pg. You can define buttons as pop-up menus, multistate responses, or program them for touch sensitivity for applications requiring fail-safe operation. Complete terminal setup parameters are accessible on screen. The module includes an RS-232C, RS-422, or RS-485 serial communications port (or optional 4- to 20-mA operation), a serial printer port, and an ASCII keyboard port. $3195.
Digital Electronics Corp., 31047 Genstar Rd, Hayward, CA 94544. Phone (415) 471-4700. TLX 172073. Circle No 360

Digital filters

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>PACKAGE</th>
<th>COMPOSITION</th>
<th>SAMPLING FREQ. OVER SAMPLING</th>
<th>TAPS</th>
<th>FILTER CHARACTERISTICS</th>
<th>DATA FORMAT</th>
<th>FEATURES</th>
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<td>TYPE</td>
<td>PIN</td>
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<td>STOPBAND ATTENUATION</td>
<td>INPUT</td>
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<td>±0.00005</td>
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<td>2 channels</td>
<td>8 times</td>
<td>153±29+17</td>
<td>±0.00005</td>
<td>110</td>
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<tr>
<td>SM5802/</td>
<td>FPP</td>
<td>60</td>
<td>2 channels</td>
<td>2 times</td>
<td>80</td>
<td>±0.09±0.01</td>
<td>90</td>
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<tr>
<td>A/B</td>
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<td></td>
<td>80+15</td>
<td>±0.09±0.015</td>
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<tr>
<td>SM5804/</td>
<td>FPP</td>
<td>60</td>
<td>2 channels</td>
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<td>121</td>
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<td>A/B/C/D</td>
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<td></td>
<td></td>
<td>70</td>
<td>±0.05</td>
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<td>SM5805</td>
<td>DIP</td>
<td>28</td>
<td>2 channels</td>
<td>2 times</td>
<td>61+13</td>
<td>±0.05</td>
<td>50/45</td>
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<tr>
<td>SM5806</td>
<td>DIP/SOP</td>
<td>28</td>
<td>2 channels</td>
<td>2 times</td>
<td>105+21</td>
<td>±0.001±0.01</td>
<td>70/52</td>
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<tr>
<td>SM5807</td>
<td>DIP/SOP</td>
<td>16</td>
<td>2 channels</td>
<td>4 times</td>
<td>52kHz (max)</td>
<td>60 (max)</td>
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<td>SM5814</td>
<td>DIP/SOP</td>
<td>22/24</td>
<td>2 channels</td>
<td>4 times</td>
<td>15MHz</td>
<td>4, 7, 8 cascaddable</td>
<td>On-chip coefficient register</td>
</tr>
</tbody>
</table>

U.S. and Canada Sales Office

For complete product information and order, contact Jim Chang,
Director of Customer Service/Development
or, Greg Branch, Sales Director

EDN March 30, 1989

CIRCLE NO 39
 COMPONENTS & POWER SUPPLIES

ond holds the interface circuitry. A slide switch allows you to select link inputs of 115 or 230V ac, 47 to 63 Hz. The link operates over 0 to 50°C and consumes 6W. $1960 per pair.

Versitron, 9005-8 Junction Dr, Annapolis Junction, MD 20701. Phone (301) 497-8600.

Circle No 361

COOLING SWITCH
- Operates on logic-level inputs
- Can operate to 70°C

The Series 305 cooling-failure switch operates on 5V dc input signals and responds to any change in temperature in 1 to 3 sec. The switch can generate a false signal when its own temperature exceeds a factory preset limit. Operating over a 5 to 70°C range, the switch features a self-heated glass-bead thermister, which compensates for ambient temperature, air speed, altitude, and relative humidity, and can sense a reversal in air flow. The switch is cooled by the same air stream that cools the host equipment, and measures 3 x 0.5 in. From $15.

Cambridge Aeroflo Inc, 900 Mt Laurel Circle, Shirley, MA 01464. Phone (508) 425-2346.

Circle No 362

THREE NEW LINES
HIGH-QUALITY
COMPETITIVELY PRICED

Switching Power Supplies

ERK Series
- Switches at 200 KHz
- MAG-AMP Regulation
- AC 115/220V (selectable)
- 100, 150, 200W Triple and Quad
- Safety: UL, CSA, TUV
- EMI: FCC/VDE 0871 Class “B”

PRK Series
- (Pictured Above) Switches at 60 to 300 KHz
- Input Range AC 85-132V
- 30, 50, 70W Triple Output
- Safety: UL, CSA
- EMI: FCC Class “B”

MRE Series
- Switches at 300 KHz
- Universal Input AC85-264V
- Miniature size
- 15 and 30W Single Output
- Safety: UL, CSA, TUV
- EMI: FCC/VDE 0871 Class “B”

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Uninterruptible Power Supply — check out our new model VPS-500V!

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Booth 1775

Volgen America Inc. 39650 Liberty Street, #325, Fremont, CA 94538 (415) 498-5950 FAX (415) 498-5954

ULTRASONIC SENSORS
- Feature noncontact operation
- Withstand harsh environments

UC60 Series ultrasonic sensors offer a noncontact distance-sensing capability. The series is made up of the UC60-LN1A analog output-level sensor and the UC60-ZD1A switched-output zone-detection sensor. Both include adjustable sensing-zone features, built-in temperature compensation, short-circuit/transient-protected outputs, and 10 to 30V dc operation. The LN1A outputs distance measurements as an analog voltage or current. The ZD1A produces a switched output when an object enters a preset zone. Both units are built to with-
THE VF MODULES TO USE IF HELL FREEZES OVER.

If that day arrives and you need a clear readout, DeeCO's XT and XTB extended temperature display modules won’t let you down.

From -40°C to +85°C, through 40g shock and 2g rms vibration, XT series modules can take the heat. And the cold. And whatever else you or the forces of evil throw at them.

And when you need clear sunlight readability, our XTB1×40 high brightness extended temperature module delivers more than 600 ft of brilliant performance.

XT and XTB features include selectable baud rates, 15 microsecond-per-character burst mode for high-speed display changes, steady or flashing characters, and brightness control.

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DeeCO®

Digital Electronics Corporation, 31047 Genstar Road, Hayward, CA 94544-7831 (415) 471-4700. DeeCO is a registered trademark of Digital Electronics Corporation © 1989.

EDN March 30, 1989

CIRCLE NO 37
COMPONENTS & POWER SUPPLIES

stand harsh environments and are encapsulated in stainless-steel cases that carry a NEMA 1, 2, 12, and 13 rating. UC60-LN1A, $695; UC60ZD1A, $595.

Opcon Inc, 720 80th St SW, Everett, WA 98203. Phone (206) 353-0900.

Circle No 363

DC/DC CONVERTERS
• Provide 1.5W single- or split-rail outputs
• Have 500V input-to-output isolation
ELI isolated dc/dc converters have an output power rating of 1.5W and are available in single- or dual-output versions. Single-output versions have an output voltage of 5, 12, or 15V, and dual-output versions have split-rail ±5, ±12, or ±15V outputs. They are available with nominal input-voltage ratings of 5, 12 or 24V. Their input-to-output isolation voltage capability is 500V dc, and they have an isolation resistance of 10 GΩ. Line regulation is more than ±0.3% for a ±10% input voltage change, and zero- to full-load output regulation is more than ±0.5%. All versions have a Pi filter on the input to minimize input and output noise. The converters are housed in standard DIP packages that measure 32 x 20 x 10.5 mm and weigh 17g. They have a −25 to +71°C operating temperature range. £18.

Gresham Powerdyne Ltd, Gresham House, Telford Rd, Salisbury, Wiltshire SP2 7PH, UK. Phone (0722) 413080. TLX 477576. FAX 0722-336263.

Circle No 364

Dowty Electronics Corp, Box 250, Prospect St, Brandon, VT 05733. Phone (802) 247-6811.

Circle No 365

CONNECTORS
• Have 15 contacts in a 9-contact shell
• Feature gold-plated contacts
Sigma-D crimp-insertable D-subminiature connectors provide 15 contacts in a 9-contact shell. You can install the contacts by hand or with a machine. The brass contact pins and phosphor bronze sockets have gold over nickel plating as...
COMPONENTS & POWER SUPPLIES

standard. Other finishes are available as an option. The contacts have a 5A/500V dc rating. The connectors can accept #26 or 28 AWG wire sizes. Contacts are available in reels or in loose pieces for hand crimping. Male connectors, $1.31 (500); 10,000-pin reel of contacts, $70.

Vernitron Corp, Beau Products Div, Box 10, Laconia, NH 03247. Phone (603) 524-5101. FAX 603-524-1627.

Circle No 366

SELECTOR SWITCHES
• Available in top- or side-adjust versions
• Sealed to withstand assembly processes

SS-10 rotary DIP selector switches are available in top- or side-adjust versions. Single- and dual-pole models are available with four or six contacts and three contact configurations, respectively. All surfaces are permanently sealed to withstand standard soldering and washing processes. The self-cleaning, gold-plated contacts have a 5V/100 mA resistive switching rating. Contact resistance equals 100 mΩ max. The switches can carry 50V dc at 100 mA. The rotational life equals 500 cycles/min and the operating range spans -10 to +60°C.

$1.70 (100).


Circle No 367

FAN SYSTEM
• Offers 12- and 15-fan capacity
• Design isolates vibration

The Airmatic 300 Fan Tray system features models with either a 12- or 15-fan capacity. The tray is configured from two structural foam halves, which include individual fan compartments to isolate noise and vibration. Rubber standoffs mounted to 8 points on the fan further isolate noise and vibration. Each fan compartment is prewired, and each fan is terminated with a plug to ease fan replacement or additions in the field. Empty fan positions come with foam and a metal insert. All trays feature a brushed and anodized front panel, which includes easy-access handles. You can order the trays with any number of fans from one to each tray's maximum capacity. 12-position tray with one fan, $302.47.

Dacobas Inc, 1890 N Voyager Ave, Simi Valley, CA 93063. Phone (805) 526-7733. FAX 805-584-8371.

Circle No 368

Thoroughbred

Mizar's SPARC CPU keeps you ahead from start to finish.

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The MZ 7170 was bred for demanding applications: a SPARC CPU at up to 25 MHz (15 MIPS), one MB of fast SRAM, up to four MB of EPROM, two RS-232 serial ports, mailbox interrupts, real-time clock, and optional T.I. 8847 FPU. And, the MZ 7170 is supported by a complete real-time operating system and UNIX®-based development tools.

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NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

CALCULATOR
• Performs 254 functions
• Works with simultaneous equations and complex numbers

The TI-68 advanced scientific calculator performs 254 functions and handles complex numbers as easily as it handles real ones. It can simultaneously display the real and imaginary parts of a complex quantity. The 6 × 3 × 0.6-in. unit sports a 12-character alphanumeric LCD that scrolls horizontally to display equations having as many as 80 characters. The calculator can solve five simultaneous equations; a plain-English prompting scheme guides you through equation entry. You can recall and replay the last equation entered, and you can edit equations after you’ve entered them. The calculator allows you access to as many as 36 registers and lets you assign names to the registers. You can enter as many as 12 formulas; the formulas remain in memory even when the calculator is off. The unit also determines the real and complex roots of quadratic, cubic, and quartic equations. $65.

Texas Instruments Inc, Box 53, Lubbock, TX 79408. Phone (806) 747-1882.

Circle No 380

AUDIO TEST SET
• Generates 8-ppm distortion sine waves from 1 Hz to 102.39 kHz
• Provides 0.03%-inaccurate crystal-controlled frequencies

The 3100B generator and 3200B autoranging analyzer form an audio test set that measures amplitude and phase vs frequency and inter-modulation (IM) and total harmonic distortion (THD) vs frequency or amplitude. The analyzer measures phase from −180° to +180° with 0.1° resolution to 40 kHz and ac voltages from 4 µV to 100V with residual THD and IM of 20 ppm. The generator stores 91 front-panel setups and can produce sine waves from 1 Hz to 102.39 kHz with 8-ppm distortion and square waves from 1 Hz to 50 kHz with a rise time of <1 µsec. As the frequency is crystal controlled, errors are less than 0.03% at fixed frequencies and on some sweeps. Generator, $4250; analyzer, $5495.

Sound Technology, 1400 Dell Ave, Campbell, CA 95008. Phone (408) 378-6540. TLX 357445.

Circle No 381

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  - **FREQUENCY**
  - **MAX RATINGS**
  - **TIME TEMP**
  - **260°C**

- **CMOS CRYSTAL OSCILLATORS**
  - **PART NO.**
  - **FREQUENCY**
  - **MAX RATINGS**
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CIRCLE NO 32

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See us at Electro/89 Booth No. 2009

CIRCLE NO 31
RISC DEVELOPER
- Supports 88000 RISC chips
- Traces system activity in real time to 50 MHz

The DS5000 development system provides in-circuit support for the 88100 RISC processor and the 88200 cache/memory management unit. The development system can perform 256-channel logic analysis and provides 16 levels of unrestricted triggering. It traces all target-system activity in real time to 50 MHz and captures trace data in 4k- or 16k-frame buffers. You can define trigger conditions for the cache, program memory, data memory, instruction memory, or combinations of all of them. By using a pair of buffers and filling one while routing the other's contents via DMA to the host processor's RAM, the development system can acquire data continuously. The development system works with MS-DOS-based hosts, including some Sun Microsystems units. $28,000 to $40,000. Delivery, six weeks ARO.

Hilevel Technology Inc, 31 Technology Dr, Irvine, CA 92718. Phone (800) 445-3835; in CA, (800) 541-2742. TLX 655316.

Circle No 382

DMM/THERMOMETER
- Offered with °C and °F readouts
- Measures ac current with clamp-on transformer

The ACA Series of multimeters includes three models, two of which measure temperature—one in °F, the other in °C. All three units incorporate a peak-hold function; the two that measure temperature also include data-hold and diode-check functions. All three models measure ac current via integral clamp-on...
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Sales & Marketing, Canoga Park, California
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If your only concern is initial cost, then fuses cost less than E-T-A circuit breakers. But beyond initial cost, there's reality. Fuses blow and can drive up your cost of warranties, service, replacement, even product liability.

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**INSTRUMENTS**

Transformers on full-scale ranges of 200 and 400A. The unit that doesn't measure temperature also includes a 20A ac current range. AC-current-measuring accuracy on all units is 1% to 100A. All units measure ac and dc voltage and resistance and have four dc-voltage ranges. The unit that doesn't measure temperature has four resistance and two ac-voltage ranges. The other units have two resistance ranges and one ac-voltage range. $119; $109 without temperature measurement.

**Extech Instruments Corp**, 150 Bear Hill Rd, Waltham, MA 02154. Phone (617) 890-7440. TLX 940913.

**Circle No 384**

**BOARD TEST SOFTWARE**

- **Adds enhancements to 1800-Serie testers**
- **Automatic test-program backup prevents program loss**

A software update to the vendor's 1800-Series board testers incorporates five features that expand test coverage and increase programming flexibility. These features include dual threshold measurements, which let you define both high- and low-voltage regions; HiCheck, which produces a 4-digit hexadecimal signature for all high-region measurements; digital filtering, which increases stability in a voltage measurement by averaging multiple sample readings; HiGuard, which improves guarded measurement accuracy by eliminating the thermal EMF of relay contacts; and differential measurements, which let you make voltage measurements that aren't referenced to system ground. The addition of program flow control and branching capabilities increases programming flexibility. $500.

**Zehntel Inc**, 2625 Shadelands Dr, Walnut Creek, CA 94598. Phone (415) 932-6900. TWX 910-385-6300.

**Circle No 385**

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**DID YOU KNOW?**

Half of all EDN's articles are staff-written.

**EDN**

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EDN March 30, 1989
CABLE CUTTER
• Cuts round cables
• Handles 300-pair cable
The PA 1818 portable cable cutter is 12 in. long. It cuts round multi-conductor cables containing as many as 300 signal pairs. It also cuts copper cables to 750 MCM (thousands of circular mils) and aluminum cables to 1000 MCM. The unit includes a folding safety latch and a release mechanism that enables you to move the tool to a different location. $239.

Paladin Corp, 3543 Old Conejo Rd, Suite 102, Newbury Park, CA 91320. Phone (805) 499-0138.
Circle No 388

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Just send this ad, along with your business card, to Mike Hartman, our Marketing Manager. Along with our DESIGN GUIDE, he’ll send you a sample EL lamp—both free. After you kick it around for a while, you’ll understand why we say—no other light can hold a candela to ours.

Loctite Luminescent Systems Inc, Etna Rd., Lebanon, NH 03766. Tel (603) 448-3444, Fax (603) 448-3452, TWX 710-366-0607

CIRCLE NO 25
REAL-TIME KERNEL

- Runs in the 32-bit, protected mode of the 80386
- Allows a combination of local and global tasks

MTOS-UX/386 is a multiprocessing, multitasking, real-time operating system for 80386-based computers. This OS normally runs in the 32-bit, protected mode of the 80386, and protects system resources such as block and memory pools, message buffers, controlled shared variables, and task resources. Also available is a version that uses the multisegmented memory model to run MS-DOS software. This model protects the kernel and the system resources by means of task privilege levels. You can increase the computing power of the system merely by adding up to 16 CPUs; changing the number of CPUs does not require any change to the applications programs. The development kit includes test facilities, debugging tools, validation programs, configuration programs, a RAM-disk driver, a Unix interface, and a C-portable library. The symbolic debugger provides task-level debugging facilities. Because all versions of MTOS-UX have the same programmer interface, programs written in a high-level language will run under any version of MTOS-UX, regardless of the processor type. Development kit prices start at $5000.

Industrial Programming Inc, 100 Jericho Quadrangle, Jericho, NY 11753. Phone (516) 938-6600. TLX 429808. FAX (516) 938-6609. Circle No 389

CAE TOOL

- Handles double-sided SMT designs
- Handles multiple power planes and as many as 16 signal layers

The MAXI/PC schematic-capture and pc-board layout package can execute double-sided, surface-mount designs with as many as 16 signal layers; it also handles multiple power and ground planes having

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800 Series units can be programmed and directed through an RS232 serial port from PC compatible software, a "dumb" terminal or a hand-held programmer. For systems configured with discrete I/Os, they can be externally interfaced through 14 defined inputs and outputs. All controls feature real time adaptive gain control that automatically adjusts the gain to compensate for load changes. The high velocity programming resolution ratio permits speed changes in extremely small increments.

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Call 1-800-447-7171 today.

The Superior Electric Company
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EDN March 30, 1989
a resolution of \( \frac{1}{1000} \) in. High-speed automatic features include placement, gate- and pin-swapping, component renaming, back-annotation, and routing. The package runs on IBM PCs and compatibles. $995.

Racal-Redac Inc, 238 Littleton Rd, Westford, MA 01886. Phone (508) 692-4900.

Circle No 390

STABILITY ANALYZER

- Simplifies setup and operation of a network analyzer
- Includes modeling and synthesis package for loop analysis

The S350/3577 stability software package allows you to integrate your HP3577A Network Analyzer from Hewlett-Packard (Palo Alto, CA) with an IBM PC or compatible, a printer, and a plotter, to form a complete stability-analysis workstation. The menu-driven software simplifies the setup and operation of the HP3577A, so that you can quickly obtain Bode plots or Nyquist diagrams of control-loop circuits. You can store the data on disk for later analysis and circuit optimization. The software includes the vendor's proprietary K-factor modeling and synthesis package for loop optimization; the software also works with PC-MATLAB for matrix computations, and with ECA-2 for circuit modeling and analysis. From $5995.


Circle No 391

SIMULATION MODELS

- Library contains models for more than 4000 LSI/VLSI devices
- Models allow fault simulation at the board or system level

SmartModels is a library of behavioral models for more than 4000 LSI/VLSI devices. Previously available for logic simulation, the vendor has now adapted all the models for use on Mentor Graphics' (Beaverton, OR) QuickFault fault simulator. The vendor plans to support other simulators that have a behavioral interface. Behavioral models are easier to write and faster to load than gate-level models; they also run faster and allow you to simulate larger designs without increasing the memory requirements. SmartModels allow concurrent fault simulation; that is, you can divide the design into several parts and run each part on a different node of a network, or on parallel processors of a multiprocessor system. The original subscription serv-
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340 Pioneer Way, Mountain View, CA 94041-1577 • (415) 962-8237 • FAX: (415) 965-9355
CIRCLE NO 26
CAE & SOFTWARE DEVELOPMENT TOOLS

ICE to SmartModels for fault simulation costs $7900; the FLEX-Node service, which allows you to move licenses around a network, costs $9900 (minimum, 3 FLEX-Node subscriptions).

Logic Automation, 19500 NW Gibbs Dr, Beaverton, OR 97006. Phone (503) 690-6900.

Circle No 392

C LIBRARY

- Lets you build resident shared libraries
- Allows you to convert existing programs to TSR versions

"/resident...C" is a library of C routines for building terminate-and-stay-resident (TSR) programs. The C routines let you build interrupt-service routines, such as timers that schedule a program to run at a particular time. You can also build resident shared libraries that can be accessed by any number of programs. The library also allows you to convert existing C programs to TSR status by adding a few function calls. Other routines included in the library let you save screens or windows so your TSR program won't disrupt the program that it interrupts. Versions of the library are available for the Microsoft (QuickC and C 5.0), Borland (Turbo C), and Lattice C compilers that run on IBM PCs and compatibles. The distribution disk includes demonstration programs that show you how to use the library and how to build shared libraries. Binary version, $99; binary and source code, $198.

Essential Software Inc, 76 S Orange Ave, Suite 3, S Orange, NJ 07079. Phone (201) 762-6965.

Circle No 393

NET-LIST GENERATOR

- Allows you to reverse-engineer pc boards
- Copes with boards that contain high pin-count devices

The Net-Learn utility software for the company's SI635 diagnostic test system lets you reverse-engineer pc boards by generating a connectivity net list for the board's components. You can then use the net list to construct a schematic diagram. The menu-driven software uses the system's in-circuit test capabilities to learn the pin-to-pin interconnections between all the devices on the pc board. Net-Learn combines as many as 128 test channels to cope with high pin-count devices. The utility employs a 2-pass test strategy to generate the net list. During the first pass, the pc board under test is powered up, and the tester locates all pins that are connected.

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CIRCLE NO 23
to power or ground lines. The pc board is turned off during the second pass, and the utility determines the interconnections between devices. The system eliminates faulty net-list generation by checking for good probe contact before the learning process begins. To cope with board modifications or updates, the software can perform a partial learn operation. You can use the output files from Net-Learn to generate schematic diagrams for the pc under test. Around £2100.

Schlumberger Technologies, Instruments Div, Victoria Rd, Farnborough, Hampshire GU14 7PW, UK. Phone (0252) 544433. TLX 858245. FAX 0252-543854.

**SIMULATOR**

- Provides a single-screen display of analog and digital signals
- Works with the vendor's ASIC-design tool set and cell libraries

DesignSim A&D lets you simulate both analog and digital circuits concurrently, and provides a single-screen display of analog and digital signals that are synchronized in time and use the same time scale. You can run simulations of electronic devices at the system, cell, or transistor level with the accuracy of Spice. You can also model electromechanical interfaces. DesignSim A (the analog portion) is based on Analogy Inc's (Beaverton, OR) Saber simulator; DesignSim D (the digital portion) is based on HHB Systems Inc's (Mahwah, NJ) Cadat simulator. DesignSim supplements, and is accessible from, the vendor's Product Design Series I (PDS I) ASIC-design tool set, and is fully integrated into the newer PDS II tool set. When you run a mixed-signal simulation, each simulator schedules its own time steps for optimal execution speed, and both simulators analyze information simultaneously so that feedback is propagated through the analog and digital simulators as required. The simulation and analytical algorithms maintain a high level of accuracy and result in a decrease of simulation time. Pricing for PDS II with DesignSim A&D for a single user, from $64,000.

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<thead>
<tr>
<th>DATE</th>
<th>TIME</th>
<th>SITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>April 3</td>
<td>9:00-12:00</td>
<td>LOCKHEED ENGINEERING &amp; SCIENCES COMPANY</td>
</tr>
<tr>
<td>Monday</td>
<td>AM</td>
<td>2400 NASA Rd., Houston, TX</td>
</tr>
<tr>
<td>April 3</td>
<td>1:30-4:00</td>
<td>COMPAQ COMPUTER CORPORATION</td>
</tr>
<tr>
<td>Monday</td>
<td>PM</td>
<td>20555 FM 149, Houston, TX</td>
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<tr>
<td>April 4</td>
<td>9:00-11:00</td>
<td>TEXAS INSTRUMENTS INC., Data Systems Group</td>
</tr>
<tr>
<td>Tuesday</td>
<td>AM</td>
<td>12501 Research Blvd., Austin, TX</td>
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<tr>
<td>April 4</td>
<td>1:00-3:30</td>
<td>IBM CORPORATION</td>
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<tr>
<td>Tuesday</td>
<td>PM</td>
<td>11400 Burnet Road, Austin, TX</td>
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<tr>
<td>April 5</td>
<td>8:30-11:00</td>
<td>TRACOR, INC.</td>
</tr>
<tr>
<td>Wednesday</td>
<td>AM</td>
<td>6500 Tractor Lane, Austin, TX</td>
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<tr>
<td>April 5</td>
<td>1:00-3:30</td>
<td>TEXAS INSTRUMENTS INC., Data Systems Group</td>
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<td>Wednesday</td>
<td>PM</td>
<td>5701 Airport Road, Temple, TX</td>
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<td>April 6</td>
<td>8:30-10:30</td>
<td>ROCKWELL INTERNATIONAL</td>
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<tr>
<td>Thursday</td>
<td>AM</td>
<td>1225 N. Alma Road, Richardson, TX</td>
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<tr>
<td>April 6</td>
<td>11:30-1:00</td>
<td>ROCKWELL INTERNATIONAL</td>
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<tr>
<td>Thursday</td>
<td>PM</td>
<td>Shiloh &amp; Renner Road, Richardson, TX</td>
</tr>
<tr>
<td>April 6</td>
<td>2:15-4:30</td>
<td>E-SYSTEMS, INC., Garland Division</td>
</tr>
<tr>
<td>Thursday</td>
<td>PM</td>
<td>1200 Jupiter Road, Garland, TX</td>
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<td>April 7</td>
<td>8:30-11:00</td>
<td>ELECTROSPACE SYSTEMS INC.</td>
</tr>
<tr>
<td>Friday</td>
<td>AM</td>
<td>Greenville Ave. &amp; Terrace Dr., Richardson, TX</td>
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<td>1:30-3:30</td>
<td>E-SYSTEMS, INC.</td>
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<td>Friday</td>
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<td>Farm Road 1570, Greenville, TX</td>
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<td>9:00-11:00</td>
<td>TEXAS INSTRUMENTS INC.</td>
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<tr>
<td>Monday</td>
<td>AM</td>
<td>8505 Forest Lane, Dallas, TX</td>
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<td>1:30-3:30</td>
<td>TEXAS INSTRUMENTS INC.</td>
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<tr>
<td>Monday</td>
<td>PM</td>
<td>13500 North Central Expressway, Dallas, TX</td>
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<td>April 11</td>
<td>9:00-11:00</td>
<td>LTV - Missiles &amp; Electronics Group</td>
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<tr>
<td>Tuesday</td>
<td>AM</td>
<td>1902 West Freeway, Grand Prairie, TX</td>
</tr>
<tr>
<td>April 11</td>
<td>2:00-4:00</td>
<td>RELIANCE COMM/TEC</td>
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<tr>
<td>Tuesday</td>
<td>PM</td>
<td>2100 Reliance Pkwy., Bedford, TX</td>
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<tr>
<td>April 12</td>
<td>9:00-12:00</td>
<td>GENERAL DYNAMICS</td>
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<tr>
<td>Wednesday</td>
<td>AM</td>
<td>Grants Lane, Ft. Worth, TX</td>
</tr>
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<td>2:00-4:00</td>
<td>RECOGNITION EQUIPMENT INC.</td>
</tr>
<tr>
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<td>PM</td>
<td>2701 Grauwyler Rd. Irving, TX</td>
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<tr>
<td>April 13</td>
<td>8:30-11:00</td>
<td>TEXAS INSTRUMENTS INC. Data Systems Group</td>
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<tr>
<td>Thursday</td>
<td>AM</td>
<td>2501 S. Highway 121, Lewisville, TX</td>
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<td>April 13</td>
<td>1:30-4:00</td>
<td>BOEING ELECTRONICS</td>
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<tr>
<td>Thursday</td>
<td>PM</td>
<td>7801 S. Stemmons, Corinth, TX</td>
</tr>
<tr>
<td>April 14</td>
<td>9:00-11:30</td>
<td>TEXAS INSTRUMENTS INC.</td>
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<td>Friday</td>
<td>AM</td>
<td>6600 Chase Oakes Blvd., Plano, TX</td>
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<td>TEXAS INSTRUMENTS INC.</td>
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<tr>
<td>Friday</td>
<td>PM</td>
<td>2501 W. University, McKinney, TX</td>
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<tr>
<td>April 17</td>
<td>9:00-11:00</td>
<td>IMPRIMIS TECHNOLOGY INC.</td>
</tr>
<tr>
<td>Monday</td>
<td>AM</td>
<td>10323 West Reno Ave., Oklahoma City, OK</td>
</tr>
<tr>
<td>April 18</td>
<td>9:00-11:30</td>
<td>NCR CORPORATION</td>
</tr>
<tr>
<td>Tuesday</td>
<td>AM</td>
<td>3718 N. Rock Rd., Wichita, KS</td>
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<tr>
<td>April 18</td>
<td>1:30-4:00</td>
<td>BOEING MILITARY AIRPLANE CO.</td>
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<td>PM</td>
<td>3801 South Oliver, Wichita, KS</td>
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<td>BENDIX KING</td>
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<td>400 N. Rogers Road, Olathe, KS</td>
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<td>WILCOX ELECTRIC, INC.</td>
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<td>2001 NE 46th St., Kansas City, MO</td>
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<td>777 North Blue Pkwy., Lees Summit, MO</td>
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<td>EMERSON ELECTRIC</td>
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<td>Evans Ave., St. Louis, MO</td>
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<td>810 W. Florissant, St. Louis, MO</td>
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<td>MTS SYSTEM CORPORATION</td>
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<td>14000 Technology Dr., Eden Prairie, MN</td>
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<td>IMPRIMIS TECHNOLOGY INC.</td>
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<td>5901 So. County Road 18, Edina, MN</td>
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<td>HONEYWELL, INC., Military Avionics</td>
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<td>6300 Olson Memorial Pkwy., Golden Valley, MN</td>
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<td>HONEYWELL, INC., Military Avionics</td>
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<td>7801 Computer Dr., Bloomington, MN</td>
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<td>CONTROL DATA CORPORATION</td>
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<td>ALLEN-BRADLEY COMPANY</td>
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<td>1201 So. 2nd St., Milwaukee, WI</td>
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<td>GENERAL ELECTRIC, Medical Systems</td>
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<td>ROCKWELL INTERNATIONAL, Collins Avionics Div.</td>
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<tr>
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<td>400 Collins Road NE, Cedar Rapids, IA</td>
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<td>ROCKWELL INTERNATIONAL, Communications Div.</td>
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<td>855 35th St. N.E., Cedar Rapids, IA</td>
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<td>4747 Harrison Ave., Rockford, IL</td>
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<td>NORTHROP CORPORATION</td>
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<td>2525 Buffle Road, Elk Grove Village, IL</td>
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<td>MOTOROLA, INC.</td>
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<td>2500 N. Wolf Road, Northlake, IL</td>
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<td>ZENITH ELECTRONIC SYSTEMS</td>
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<td>1000 Milwaukee Ave., Glenside, IL</td>
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Now your CMOS backup battery can be what you’ve always wanted it to be.

Just another component.

Forget those labor intensive methods normally required for printed circuit board mounting of batteries. Our new axial lead \( \mu \)PowerCells\(^\text{TM} \) (Lithium Iodine 2.8V Solid CMOS Backup Cells) look like a resistor or capacitor. They’re about the same size and they don’t need special handling. You can put them on a sequenced tape reel for automatic printed circuit board insertion. And like most other components, \( \mu \)PowerCells\(^\text{TM} \) can be wave soldered, cleaned and dried using normal procedures.

Once they’re in place, \( \mu \)PowerCells\(^\text{TM} \) are dependable. Their Lithium Iodine chemistry is the number one choice for powering cardiac pacemakers. And a performance study of over 1 million batteries in use shows that a useful life of more than 20 years can be predicted.

At 35 milliamp-hours, the axial lead \( \mu \)PowerCell\(^\text{TM} \) will handle most CMOS backup problems. However, higher capacity versions to 1 amp hour are available in a new space-saving rectilinear package. The Catalyst Research line includes modules for sensing power loss and transferring to battery backup as well as clock modules with battery built in.

Best of all, Catalyst Research \( \mu \)PowerCells\(^\text{TM} \) are priced like other components.

For more information, call us at 301-296-7000 ext. 304.
# CAREER OPPORTUNITIES

## 1989 Editorial Calendar and Planning Guide

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Call today for information:

East Coast: Janet O. Penn (201) 228-8610  
West Coast: Mary Beth West (213) 820-3887  
National: Roberta Renard (201) 228-8602
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Challenge your expertise in logic design and/or microprocessor system design using flow charts and timing diagrams for digital design and detailed design analysis. Your experience should include vendor libraries, test vector generation, simulation checkout and TTL emulators for gate array standard cell design. Familiarity with CAE systems used in logic design, test vector generation, simulation checkout and documentation is also necessary. You must have five years' related experience plus a BSEE or equivalent degree. An MSEE degree is preferred.

Systems Architects

You’ll design new products by investigating and evaluating system compatibility and performance of design alternatives and new technologies. You’ll develop hardware compatibility tests and performance analysis tools.
Qualify with a BSEE, MSEE preferred, and three years' hardware background with a knowledge of microprocessor-based systems software. In addition, experience with CPUs/Memory/Bus architecture, numeric co-processors, file subsystems, network communications, graphic subsystems and state machines is required.

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You’ll evaluate, design and develop firmware, operating systems, device drivers and utility software for PC systems. Along with your BSEE/BSCS, you’ll need four years' related experience in PC software development, 8086/286/386 Assembly/C language programming in MS-DOS, OS/2 and/or UNIX/XENIX operating system environments.

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Put your design and development talents to the test improving structural software. You’ll help increase the reliability of personal computer systems and operating systems software. Five years' software quality assurance or test development experience should complement your BSEE/BSCS.

Experience in C and 8086/286/386 Assembly language is essential.

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EDN March 30, 1989
First, there was the vision...

Space exploration began with a vision.

The fire of imagination—fused with superior technical proficiency—leading the way to limitless possibilities. A special vision that creates the kind of breakthroughs that characterize GE Astro-Space.

Since the nation's first space communications adventure nearly 30 years ago, GE Astro-Space has been a world leader in the design and manufacture of satellites for government and commercial communications, meteorological, navigational and scientific use.

And, with over one hundred and fifty satellites currently circling the globe—and long-term, history-making projects such as the Mars Observer, Space Station and Landsat—we can offer Engineers the kind of rare opportunities that few are destined to realize.

If you're the Engineer we're seeking, join us as we pave the way for a new generation of emerging space technology. Our mission requires the technical proficiency of Engineers with a minimum of 3 years experience in one or more of the following:

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  - Antenna Design
  - RF Packaging Design
  - Robotics/Mechanism Design
  - Spacecraft Attitude Control

- **Electrical Engineers/ Hardware**
  - Electronic Packaging
  - Harness Design
  - ATE/AGE Design
  - Power Supply/Analog Design
  - Video Design

- **Systems Engineers**
  - Spacecraft Power Systems
  - Mission Analysis

- **Integration & Test Engineers**

Our New Jersey location offers all the advantages of nearby Princeton—within easy access to New York City and Philadelphia. Additionally, selected positions are open in Valley Forge, PA. In either location, you'll experience a lifestyle that complements your career, providing unlimited opportunities for personal and professional growth. As the largest employer of engineers and scientists in the world, GE provides competitive salaries and exceptional benefits including tuition refund and continuing education programs—so your expertise is always current and expanding.

Rush your resume to: Employee Relations, Dept. EDNM, GE Astro-Space, P.O. Box 800, Princeton, New Jersey 08543-0800. An equal opportunity employer.

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*Cross the engineering frontier.*
GE Government Electronic Systems Division is prime contractor for a second generation, integrated system that will make Seawolf SSN subs effective defenders well into the 21st Century.

If your ambitions include developing big, fast signal processing capabilities and linkages to advanced ASW sensor systems and C-... or being part of more powerful, more discriminating radar, sonar and acoustical programs that enlarge ocean surveillance capabilities of surface ships... tell GE.

The more that company resources and reputation mean to you—and the more you want to accomplish in system and software architecture, hardware and circuit design, low frequency and broadband sonar, and signal and data processing—the sooner we should meet. Do what our customers do. Talk to key GE managers at our two locations.

**Syracuse, NY**

In an area with wide recreational, cultural and lifestyle options, you can be part of the most far-sighted signal processing programs. We have openings for engineers with at least 5 years experience as...

**Systems Engineers/Managers**

opportunities exist in:
- Algorithm Development
- Signal Processing
- Human Factors
- Sensor System Design
- Systems Analysis
- ASW Systems
- Combat Systems Architecture
- Reliability/Maintainability
- PIDS Through B level Specification Design

**Hardware/Circuit Design Engineers/Managers**

help design the future by working in:
- CMOS
- Power Design
- Gate Array Design
- Configuration Management
- Cabinet Design

**Software Engineers/Programmers/Managers**

opportunity to advance if you’re experienced with:
- Top Down Structured Design
- ADA Language Architecture and Programming
- Embedded Programmable Processors (68000 or similar)

**Software Quality Assurance Engineers**

with experience in:
- Metrics/Trend Analysis
- ADA/Case tools helpful
- Strong organization/personal skills
- MIL-STD 2167/2168
- Summarizing detailed data for management decisions

**Choice opportunities also exist in the following areas:**
- Advanced engineering design/development of future ASW systems
- Test and integration testing
- Quality assurance programs engineering
- Subcontracts management and financial analysis
- Field programs engineering (Naval systems)

Both locations provide competitive salaries, and the technical and management training and comprehensive benefits you'd expect from GE. To apply, please send your resume indicating position of interest, and salary history, to:

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U.S. Citizenship Required

**Moorestown, NJ**

In an attractive suburb 15 miles outside Philadelphia—near shore and mountains—engineers make exciting mental journeys. Should have BSEE or BSCS and at least 5 years experience as...

**Senior Engineers, Combat Control**

- BSEE
- 5+ years in Combat Control performance definition, design and test for real time Combat Control Systems.
- Knowledge of U.S. Navy systems, preferably submarine systems.

**Senior Digital Design Engineers**

BSEE, with 5+ years experience in the digital/firmware design of digital sub-systems. Should also have experience in the design of special purpose digital processors with strength in current custom design and simulation techniques.

**Senior Software Design Engineers**

BSEE or BSCS with 5+ years direct experience in the design and development of large real time Command and Control Systems which utilize sensor data input. Experience with the following:
- Fault location/fault detection with a plus for automatic configuration design experience.
- Real-time data base design experience with Ingress or Oracle.
- Motorola 68020 assembly language, and/or real time operating system experience.

**Senior Engineers, Command & Decision**

BSEE with 5+ years in Command and Control performance definition, design and test for real time Command and Control Systems. Should have knowledge of U.S. Navy systems, preferably submarine systems.

Both locations provide competitive salaries, and the technical and management training and comprehensive benefits you'd expect from GE. To apply, please send your resume indicating position of interest, and salary history, to:

GE Professional Staffing, ADEDN, P.O. Box 4840, EP-1-106, Syracuse, NY 13221 or MTEDN, GESD, Bldg. 127-101, Moorestown, NJ 08057.

U.S. Citizenship Required
You might not expect a high technology company to put such an emphasis on CIM. But Sun Microsystems sees CIM as nothing less than a strategic advantage in the very competitive workstation market.

Sun already boasts shop floor control and automated handling and distribution, as well as complex board and system testing and decision-making support. Now we want to integrate our systems into one, functional architecture.

Our goal: the ultimate CIM system.

This architecture will combine the ease of our user interface, vivid graphics, and networking capabilities with object-oriented programming in UNIX™ and "C", and distributed RDBMS to create the ultimate CIM system.

Sun has the resources to make it happen as one of the fastest-growing companies in America, with over one billion dollars in sales last year. We have a remarkable number of CIM experts in-house. More important, we have the explicit commitment and support of top management to make Sun unsurpassed at CIM.

But we need more. More people skilled in CIM to help us accomplish our ambitious goals.

Here's your challenge.

Join the Sun Microsystems CIM effort, and you'll have the opportunity to work on any one of several challenges:

• Tools & Technologies Development
• Applications Software Development
• Systems Integration
• Engineering Services
• User Support Services

Experience in UNIX or "C" is essential to qualify for these positions. Candidates should also have manufacturing systems integration experience.

If you meet those specs, apply now. Here are four of our current openings:

System Administrator

You will provide system administrative support to the UNIX end-user community. This will include installing and maintaining all file servers, timeshare machines, laser printers, and networks, while working with third-party vendor software. Requires a BSCS/Information Systems and 1+ years' UNIX systems administration experience. Strong communication skills and an excellent working knowledge of UNIX and UNIX utilities, software documentation, shell programming, and networking are also needed.

Software Development Engineers

Requires experience in CIM, systems integration and application software development for state-of-the-art software systems engineering in a UNIX environment. Additionally, you will need 3+ years' experience with UNIX and "C" as well as 3 years' CIM experience.

Engineers — Surface Mount Technology

Develop, maintain, support and improve Pick & Place, paste, printing and re-flow processes for internal surface mount production line. Requires a BSME and 2-5 years' related experience in SMT process development. Panasonic and/or Fuji experience desired.

Sr. CIM Systems Software Engineers

We have several positions available for individuals with experience in process control applications including factory automation and/or distribution, as well as statistical analysis in a manufacturing environment. Requires 3 years' experience as a group leader and experience with structured analysis and design techniques in an application design environment. Strong user interface and excellent communication skills required. Systems integration background and 3+ years' UNIX and "C" experience are preferred. For some positions, 4+ years' experience with relational database required.

To apply, please send your resume in confidence to Professional Employment, Sun Microsystems, Inc., MS DAQ, 2550 Garcia Avenue, Mountain View, CA 94043. Letter-quality resumes will get to our hiring managers faster, since all resumes are electronically scanned and processed by the Resumix™ system. An equal opportunity employer. Principals only, please.

Sun Microsystems invites you to take CIM to its limits. Then, go beyond them.

Software Development Engineers

Requires experience in CIM, systems integration and application software development for state-of-the-art software systems engineering in a UNIX environment. Additionally, you will need 3+ years' experience with UNIX and "C" as well as 3 years' CIM experience.

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- Current product line includes:
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  - Dell System 220, the most powerful 80286-based PC available
  - Dell System 310, the fastest PC based on the Intel 80386 20 MHz microprocessor
  - Dell System 325, our 25 MHz "no compromise" PC for high-level computing
  - A wide range of peripherals, printers, accessories and software
- Dell UNIX System V/386 was recently announced for the 386-based hardware
- International subsidiaries in the United Kingdom, Canada, Germany and Japan
- Largest Austin-based publicly-held corporation, with over 1,000 employees
- Dell is located amid the beautiful hill country and lakes surrounding Austin, TX. Austin offers an affordable quality of life, unsurpassed by most major metropolitan areas

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Challenging responsibilities include specification, development, implementation and testing of board level and/or chip level logic design for PC applications. Requires recent high-speed logic board/card design experience, preferably with I/O BUS and CPU complex focus. BS/MS EE.

UNIX DESIGNERS
Software designers participate in team development of UNIX enhancements and customizations for Dell hardware. Five years total software design experience with two years in UNIX and C required. MS-DOS and Intel hardware and software experience preferred. Graphics and networking experience a plus. BS/MS EE.

BIOS/DIAGNOSTIC PROGRAMMERS
Software group develops low-level Intel programs in support of hardware design projects. A solid understanding of hardware design with experience in BIOS or diagnostics, assembler and C programming required. BS/MS EE or CS.

PROJECT PLANNERS
Responsible for product/project development from inception to market introduction. Requires experience in coordinating all aspects of project including design, procurement, support and administration as well as hardware/software assimilation. Prefer recent experience in PC project management with current knowledge of microprocessor-based industry. Minimum four year technical degree required.

ADVANCED TECHNOLOGY ENGINEERS
Senior Engineers work independently in researching leading edge technologies for potential products. Position requires broad-based design/project management experience with thorough knowledge of high-speed microprocessor industry. BS/MS EE.

ADDITIONAL OPPORTUNITIES
R & D groups listed below have positions requiring knowledge/experience with MS-DOS based PC hardware and software, assembler, C and UNIX.
- Systems Validation
- Systems Integration
- Mechanical Design
- Technical Publications

To explore these and other opportunities and join an organization that offers a position with an excellent salary and benefits package, send your resume to:
Professional Employment Box E283, Dell Computer Corporation, 9505 Arboretum Boulevard, Austin, Texas 78759 (EOE m/f/h)
Unbelievable, until now... tiny monolithic wide-band amplifiers for as low as 99 cents. These rugged, 0.085 in. diam., plastic-packaged units are 50 ohm input/output impedance, unconditionally stable regardless of load, and easily cascadable. Models in the MAR-series offer up to 33 dB gain, 0 to +11 dBm output, noise figure as low as 2.8 dB, and up to DC-2000 MHz bandwidth.

NOTE: Minimum gain at highest frequency point and over full temperature range.

* +4 dB Gain Compression
  +1 dBm 1 to 2 GHz

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each:†

<table>
<thead>
<tr>
<th>Value</th>
<th>Characteristic</th>
<th>Temperature</th>
<th>Tolerance</th>
<th>Size (mil)</th>
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<tr>
<td>102 ± 20%</td>
<td>NPO</td>
<td>-30°C to 125°C</td>
<td>5%</td>
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† Minimum Order 50 per Value

Also finding new ways to set higher standards.

Mini-Circuits

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CIRCLE NO 52

EDN March 30, 1989
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1-800-322-3616
When your specs call for emission control,
call for Emcor's EMI/RFI series

FCC Level
Emcor offers shielding solutions. Shown at left is an Emcor EMI/RFI enclosure—designed for commercial applications and tested to MIL STD 285. Fabricated with 14-gauge cold-rolled steel, these enclosures have the rigidity to maintain shielding continuity. They are also fully zinc-plated—both frame and external components—and come with a full complement of accessories.

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To meet the most demanding levels of shielding often required by the military, Emcor offers its Tempest style line of enclosures as shown in the top photo. Also tested to MIL STD 285, this line combines high strength with modular options and attractive esthetics. Features include a rigid, 12-gauge frame plus a unique latching system and door design (patent pending). These enclosures are nickel-plated with copper finger stock gasketing.

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1-800-BELDEN-4

BELDEN REDEFINES FLAT CABLE TECHNOLOGY

<table>
<thead>
<tr>
<th>Mirror Image Cable</th>
<th>.025 Transmission Line Cable</th>
<th>Vari-Twist™</th>
<th>Peelable Ground Plane</th>
<th>Rainbow Cable (PVC or FEP Teflon*)</th>
<th>Ribbon Coax</th>
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<tbody>
<tr>
<td>Shielded Jacketed Ribbon Coax</td>
<td>Stacked Cable</td>
<td>Shielded Jacketed Cable</td>
<td>Shielded A &amp; B Cable</td>
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