DEC Directory

GCR Improves Data Recording
Shortened DFT Speeds Computation
Controller Mates Disks To DEC Bus
Cyclic Code Redundancy
When you ask some people about backup — they back off.

And for good reason. Ask any other supplier of peripheral products for system backup, and you'll find that some can supply a disk, some can supply a cartridge recorder, others a streaming transport. But none can supply the choice which Kennedy can offer. Kennedy is the only company that can offer an SMD compatible. 8" 40 MByte disk drive (Model 7300) and an 80 MByte 14" Winchester disk drive (Model 5380). To back them up, Kennedy has a 1/4" cartridge recorder (Model 6450), and Model 6809, 1/2" Data Streamer Tape Transport.

Kennedy was the first to utilize the 1/2" 3M cartridge for disk backup; Kennedy was the pioneer in Winchester disk technology, and was a leader in developing a low cost streaming tape drive.

All of these products were conceived and designed to meet the need for reliable, low cost backup — for our systems or for any other system.

Kennedy has always backed its products. That's why we're No. 1. Call or write us about your problem.

We won't back off.

KENNEDY INTERNATIONAL INC.
U.K. and Scandinavia
McGraw-Hill House
Sheppenhangs Road
Maidenhead
Berkshire SL6 2OL England
Tel: (0628) 73939
Telex: 867857 KEN UKS G

KENNEDY INTERNATIONAL
Koningin Elisabethplein, 8
B-2700 Sint-Niklaas
Belgium
Tel: (031) 771962
Telex: 71870 KEN CO
Dec Users: Corvus Lowers the Price of Admission to the Winchester Club.

Attention DEC* users: Here's the price breakthrough you've been waiting for on DEC compatible Winchester disk systems. Our new 5¼-inch 5-megabyte Winchester sells for one half the price ($2900 in OEM quantities of 100) and takes up one half the space of the DEC RL01 it replaces. It's a complete disk sub-system, including disk drive, intelligent controller, and interface card.

It brings sealed-environment reliability to your DEC LSI-11 system while directly emulating the RL01 with 100% hardware and software compatibility. Or if you need greater capacity, we can set you up with a 10 or 20 megabyte system.

Here are more of our exclusive features and benefits:

- Single quad-size interface card to Q-bus
- Compact rack or table top models
- Multiprocessor backend network, the CORVUS CONSTELLATION, supports up to 8 LSI-11 s
- Low cost removable-media backup, the CORVUS MIRROR, uses proven video technology.

For the full story, contact CORVUS today.

PRICE: UNDER $2900
WHEN: NOW!
WHERE: YOUR LOCAL CORVUS REPRESENTATIVE

CORVUS SYSTEMS
2029 O'Toole Avenue
San Jose, California 95131
408 946-7700 TWX: 910-338-0226

* Trademark of Digital Equipment Corporation

Circle 5 on Reader Inquiry Card
Image processing systems
Modular graphic display systems
Frame buffers—Television monitors

Grinnell has them all, for almost any application: from simple black and white line drawing to full color image processing. Select a packaged system, or configure one "your way."

**GMR 270 Series**: 512 × 512 frame buffers and full color pipeline image processing systems.

**GMR 260 Series**: 1024 × 1024 frame buffers for grayscale, black and white, pseudo color and full color.

**GMR 27 Series**: 256 × 512 to 1024 × 1024 high speed, modular graphic and image display systems.

All systems are available in both U.S. and European versions, with plug-compatible interfaces to most minicomputers (including DEC, Data General and PRIME). Proven system designs ensure reliability, and an expanded FORTRAN library and driver package makes operation easy.

So, whether you need a complete system, or just a card set to embed in a larger system, Grinnell has an optimum cost/performance solution. For complete specifications and/or a quotation, call or write today.

---

**GRINNELL SYSTEMS**
2159 Bering Drive, San Jose, California 95131 (408) 263-9920  TWX 910-338-2145

Circle 4 on Reader Inquiry Card
22 Shortened Algorithm
A shortened DFT algorithm achieves real time processing. This article describes both SDFT theory and its realization.

26 Microprogrammable Processor
The flag status bit storage concept fulfills microprogrammable processor needs.

34 GCR Increases
This article discusses data groups, AuxCRC or auxiliary cyclic redundancy character, ECC, resync bursts and other components that make up a CRC data block.

40 DEC Product Directory

54 DEC Compatible Products Continue Upward Growth
The rapid growth of the DEC compatible market makes it all the more important that the OEM protects himself by carefully investigating.

62 Bit-Slice Design
Interfacing up to four 80- to 300-MB disks to a Unibus backplane at low cost.

74 SIGGRAPH '81 Blends Art With Science
A showcase for the latest graphics razzle-dazzle, this eighth annual conference is an educational forum.

77 Cyclic Code Redundancy
Here is an efficient and effective means of accomplishing error detection using CRC.

6 Letters

8 Speakout
Do Prices Count?

10 Technology Trends
- Users Graduate to Superminis
- Software Trends Spark Competition
- Minis Continue To Gain On Mainframes
- Printers: Key To Computer Growth
- Low-Cost Graphics Systems Aid OEM Designers
- CAD Package Improves Engineering Productivity
- Computer Graphics Will Improve Sagging Managerial Productivity

88 COMPAT Design
- PDP-11 Cross-Compiler Remedies "Brute-Force" µP Software Development
- Compatible Multifunction Controllers Deliver Backplane Breathing Room

96 Innovative Design
- Glare Screen Provides Cure For Terminal Eyestrain
- Printer Produces Color Graphics
- Smart Storage Tube Terminal Displays Two Colors

100 New Products

109 Designers Notebook
Use "TouchGraphics" Panels As On-Off Switch, Adjustable Vernier And X-Y Controller

112 Advertisers' Index
Do you need to add peripherals or additional cable lengths to an overloaded bus? Do you have unknown system crashes such as caused by a type 4 trap—delayed response from a slave sync? Is your current repeater too slow for your current system?

If these questions are relevant, then Datafusion Corporation has a device that can answer your needs, the OSB11-A Bus Repeater. It is a functional equivalent of DEC’s DB11-A, and is designed to drive at least 19 bus loads and 50 foot of bus cables.

**Ultra Fast:** 80 nanoseconds MSYNC to return SSYNC maximum (40 nsec one way). This is due, primarily, to the specially designed patented integrated circuit employed by the OSB11-A.

**Reliable:** Only 34 operational circuit components. Tested in environments from 0° to 70°C with virtually no degradation of signal quality.

**Easy to Install:** Remove a M920 Jumper and replace it with a OSB11-A. No extra system unit is needed; no wires or plugs to connect (or disconnect); no lost time in reconfiguration.

**Available:** Off-the-shelf. And, it’s fully supported and warranted.

**Cost:** About 25% below DEC* Quantity discounts are available.

Other PDP11 products available are a Busrouter (a Unibus Switch) to reconnect multiple peripherals to one or more PDP11 cpu’s, a Unibus Cable Tester, and an Associative File Processor for high speed text search—a hardware approach.

We also have some ideas for the application of our products which might not have occurred to you. If you can’t get the performance that you would like from your PDP11 system, maybe we can help. Please telephone our Marketing Manager at (213) 887-9523 or write to Datafusion Corporation, 5115 Douglas Fir Road, Calabasas, California 91302.
2 NEW WAYS TO PROTECT YOUR INVESTMENT
from PLESSEY, Your Full Service Memory Bank

Increase system speed. End single-bit errors. Plessey's two new dynamic MOS memories increase your system throughput. And maintain data integrity.

COMPLETE YOUR VAX* MEMORY. Up to 4 Mbytes for maximum return on investment. Plessey's S780 provides 256 Kbytes of MOS memory on a single hexwide board. Hardware and software compatibility with VAX-11; 8-bit ECC for data integrity. IMMEDIATE DELIVERY.

HIGH YIELD PDP-11/44* MEMORY. Uses 64K RAM technology to achieve 512 Kbytes on a single hexwide board, the S11E/2. One bus load to the Unibus* — either PDP-11/34 or 11/44. Integral ECC/ELR logic with LED indicators. AVAILABLE NOW.

MEMORIES YOU CAN BANK ON
ALL MEMORY PRICES REDUCED!

Plessey Peripheral Systems is your full service memory bank for all your memory needs — LSI-11*, PDP-8, PDP-11, VAX, and DG NOVAT. Plessey built its reputation on performance. Billions of bits strong and growing stronger. Backed by years of experience. Put your money in the bank. The Plessey Memory Bank. For memories you can trust.

Plessey Peripheral Systems

*Trademark of Digital Equipment Corporation.

†Trademark of Data General Corporation

Circle 8 on Reader Inquiry Card
Dear Editor:

I am writing to inform you of a very significant event that occurred at the conclusion of my talk on May 19, 1981 before IEEE's Philadelphia section. My talk, "Engineering Societies and Leaky Umbrellas" was about the new organization, the American Association of Engineering Societies, that you described in your May Speakout. IEEE forced members to support AAES. In my talk, I tried to point out how AAES benefits only college professors and corporate executives.

At the conclusion of my talk, a very significant vote was taken: by an overwhelming margin, 16 to 1, the Philadelphia section voted that "IEEE should not be affiliated with the American Association of Engineering Societies." There were 9 abstentions and many others simply did not vote. I am informed that the turnout was slightly above average for a meeting of the Philadelphia section. Thus, this represents the first known break in the ranks of IEEE as regards participation in AAES.

Irwin Feerst
Committee of Concerned EEs
Box 19
Massapequa Park, NY 11762

programmable gain amplifier

Dear Editor:

Many adjustment problems of the programmable gain amplifier described in a Designers' Notebook (December 1980) would be eliminated if the designer had used a non-inverting amplifier configuration rather than the inverting configuration used.

Prof. S. Ben-Yaakov
Electronic Engr.
Ben-Gurion University
Beer-Sheva, Israel
Family pride.

Now there's an advanced technology family of single board controllers for DEC* computers from Western Peripherals—the number one name in controllers. The TC-131 (for PDP-11s*) is the first TM-11 emulating controller to combine PE and NRZ on one standard hex board. It lets you mix 9-track, PE, NRZ or dual density tape units in any combination up to 125 ips. A 64 byte data buffer allows installation at any point on the unibus without consideration of NPR priority.

The TC-151 single board NRZI tape controller interfaces any industry-standard drive to the LSI-11~. Add a dual width Phase Encode Board for the same performance as the TC-131.

The DC-231 accommodates up to four SMD disc drives of 40 to 600 mb each with RMO2 emulation. Its four sector (2048 bytes) data buffer makes “data-late” errors a thing of the past. The advanced technology “micro-engine” allows a complete track to be written on a single drive revolution. A measurable performance advantage for your PDP-11.

All three controllers are software compatible. All have self test. All are backed by one of the best factory service organizations in the business. And all can be delivered in 30 days.

For more information, call or write today: Western Peripherals Division, Wespercbrp, 14321 Myford Road, Tustin, CA 92680, U.S.A. (714) 730-6250.

TWX: 910 595-1775. CABLE: WESPER

Number 1 in controllers for DEC and Data General computers.

* Trade name of Digital Equipment Corporation.
Do Prices Count?

Paul Snigier, Editor

Do you consider price an important factor when specifying a service or product? From the lack of pricing information on some new product releases that we've received, you'd get the distinct impression that prices don't matter to these firms, their agencies and their PR departments. Unfortunately, our readers see it in a different light: if a firm doesn't bother to give a price, it has something to hide — namely a price that's too steep. If written in this (or any other) computer publication, such items draw less response. Certain high-interest items draw more than those in highly-competitive product areas. Different magazines and tabloids have come up with different figures, but all agree that reader response to these "priceless wonders" is down significantly. We agree that it's a serious disservice to new product editors, to readers and to the company introducing these products.

If a new product is priced high, then the press release should begin with the product's "claim to fame." Yes, a high price will turn off some readers. But it is far better to qualify readers and eliminate those uninterested engineers at the start and not force them to request material. They will not specify the product anyway, and it is a disservice to the firm and a waste of its money to send out material to such readers.

Other reasons for priceless product releases include the great variety of certain product lines. This applies to semiconductor families released at the same time, to cables, to power supplies and a few other items. In such cases, we suggest that it's better to include a price range or the price of a typical or anticipated best-selling member of the family rather than on price.

This type of reasoning, using the priceless new product as a come-on, has been with the trade press as far back as anyone remembers; it has constituted roughly 15% of all new product releases. Today, however, a new type of priceless product release is arriving with growing frequency; it is due to inflation and rapid product changes. Activity is so brisk that prices decline rapidly to meet competitors' price threats. All of this has created a hectic, chaotic and rapidly-changing price situation. It's not surprising that more manufacturers are leaving off prices on their new product releases; they reason that it's safer for them to be on the cautious side. This creates problems for everyone. The new product editors must phone the firms. Too often the individual authorized to provide the information isn't in; too frequently he may not return the call; or, if he does, cannot reach the editor. At times the new product editor may get an argument. This consumes time, and still does not get us the correct pricing information. Many times editors don't bother on many publications; and we notice that this trend is growing.

It's the privilege of any agency, PR department or firm not to include pricing on a new product release. We feel it's also the right of every new product editor to take this factor into consideration when he makes the decision to publish — or not publish — that particular product.

We would like your views on the matter of priceless new product releases. Do you feel that we should not publish new product releases that lack prices? Or, should we merely consider it as a negative factor in the overall judgment? If so, how would you want to see it weighted? Let us know.
The DR-144S is another industry first from Dataram. This 1.0MB semiconductor ADD-IN quadruples the size of 16K RAM-based ADD-INs available from either Digital Equipment Corporation (DEC) or ADD-IN memory suppliers.

Unlike other manufacturers, Dataram’s ADD-IN memory for the PDP-11/44 uses a double word organization with ECC (32 data + 7 ECC) making it completely software compatible with DEC’s memory diagnostics. A Mother Board and two Array Boards are joined together by pluggable pins (as shown below) to provide the 1.0MB DR-144S system.

The Mother Board is the only board of the DR-144S assembly which interfaces to the host PDP-11/44. This means that there is only one unit load and that 1.0MB power requirements are dramatically reduced compared to the approach of using four separate 256KB modules. Also, the DR-144S current drains are much lower in the battery backup mode.

The DR-144S is available with only the Mother Board and in versions including one or two array boards. The DR-144S Mother Board provides a capacity of 256KB. The DR-144S Mother Board with one array board is 512KB; with two array boards, the DR-144S capacity can be either 768KB or 1.0MB.

The DR-144S is an exciting product, but we’re not resting on our laurels. You can be assured that when 64K RAMs are more cost effective than the 16K RAMs, the DR-144S will be able to accommodate them. Think of it — a 4.0MB PDP-11/44 ADD-IN!
Users Graduate to Superminis

High-performance superminicomputers have become "hot" items, with more than a dozen suppliers struggling to keep pace with "scorching" user demand. IRD of Norwalk, CT, in a report, attributes supermini popularity to an increased user sophistication and "irresistible" price-performance characteristics. Shipments of 32-bit superminis this year should reach $300 million, with 60% increase to $480 million predicted for 1982.

**applications support growing**

Although traditionally superminis have been sold as "barebones" hardware, tailored and programmed by users or systems houses for particular applications, vendors are tending to provide more sophisticated programming tools and special-purpose I/O equipment for such applications as aerospace simulators, oil drilling analysis, process control and business transaction-processing, according to the report. Will the current phenomenal growth in this market last forever? No. Soon, in-depth support of particular applications niches will become the deciding force in market leadership.

**major challenge from HP — not IBM**

With almost 40% of the current market (in terms of the value of equipment installed), DEC is the leader in 32-bit superminis, with its VAXes. Runners-up are Perkin Elmer (22%), SEL/Gould (17%) and Prime (16%). IRD predicts an "important" new supermini, from H-P, which may be announced soon. The machine will be comparable in power to mid-range VAX equipment and configured as a desk-top. A head-on competitive machine from IBM is unlikely; an IBM supermini product would damage IBM's 32-bit commercial offerings in the 4331 and 4341 series, with which superminis compete in some applications.

**DGC readies "Fountainhead" for introduction**

Data General, which introduced its MB/8000 series of superminis last year, is readying a new supermini for introduction to the market later in 1981 or in 1982, as reported earlier ("Minicomputers", December 1980 pp. 26-28, P. Snigier). The "Fountainhead Processor" is a key element in DGC's growth strategy. Linked with this product is the possible acquisition of one or more specialized systems vendors to provide DGC with "instant" applica-
Software Trends Spark Competition

Competition is intensifying among companies vying for control of vital software areas. The strengths of different software companies will establish their predominance in their respective market focuses over the next five years, relative to operating systems, languages utilities and specific market applications. Contention among several companies is the battle for dominance of 16-bit operating systems. Digital Research's CP/M operating system achieved the status of de facto standard for 8-bit µCs. However, efforts to control operating systems at the 16-bit level as well are encountering formidable competition from UNIX and UNIX-like operating systems produced by companies such as MicroSoft Inc., Bell Labs, Onyx, Cromemco and others. Standards of 16-bit operating systems will be determined within the next two years, according to Creative Strategies International of San Jose, CA, in a new report.

As software houses solidify into major marketing forces for hardware, their allegiances to certain computers and/or operating systems will largely determine the success of those computers. Trends in the µC industry are toward standardization more than in any other aspect of the data processing industry. Especially at the operating system level, incompatibilities will severely hinder developments. Only those hardware manufacturers with very strong in-house software development can afford incompatible, proprietary operating systems. Software, and good documentation of that software, will control the sales of microcomputers. Hardware manufacturers that ignore this fact will not do well.

Most of the best software available today is from third-party software houses, and this trend will continue. With few exceptions, hardware manufacturers have not moved to develop software in-house, but have acquired software from suppliers outside the manufacturers' environment.

The fast-changing technology of µC industry requires distribution across as large a base of systems as possible. There is an escalating rush among software houses to generate "Lathe" type software converters, which allow quick transfer and translation from one machine to another, within and without a similar operating system and µP.

Minis Continue To Gain On Mainframes

The sophisticated end user has become the rule, not the exception. This, in turn, has fueled demand for greater user control and encouraging the trend towards DP decentralization. Even within the minicomputer industry, effects of changing user needs can be seen. Conventional minis will continue to be well-suited for automation control and advanced communications work, as well as laboratory analysis and "number crunching." On the other hand, microminis, sometimes called microcomputers, are becoming increasingly attractive as an alternative to conventional minis. These small, one-board systems are particularly cost effective for tasks such as control of machine tools where data handling requirements are modest.

Minis with more powerful processors are evolving in the other direction to become "superminis." While the prices of these computers are substantially higher than those of conventional minis, the greatly increased data handling capability and ease of programming will make superminis the fastest growing minicomputer category.

Printers: Key To Computer Growth

What the computer world needs is a low-cost printer to solve the current dilemma of peripheral cost exceeding many basic computers. While lower mini and µC prices have made computers accessible to broader business and personal applications, the peripheral costs, particularly printers, inhibit their full development.

The 20-, 40-, and 80-column printers, such as offered by Alphacom, and others, will grow rapidly in the low-end small business and personal computing market, which will increase in the 1980-1985 window by over 23% a year, from today's $1.2 billion, rising to $3 billion. Printers now range from thumbnail-sized calculator-based printers to the largest and most refined thermal and impact printers at all market levels.

markets are changing

The 20-, 40-, and 80-column alphanumeric and graphics printers are attractive to business and professional
end users, because hard copy of data, graphs, charts and tables are increasingly becoming a standard requirement. Now, hobby, educational and home computer users also have a feasible printer option. Professional and business users, lacking alternatives, use printers costing $1000 to $3000 for all hard copy, including rough draft. The cost limits their number to one per business computer. With the low cost of newer 80-column printing systems, more than one printer can be connected to a shared-logic type system in an office environment.

Presently, shared logic system throughput is slowed considerably because one printer is shared by every terminal. Now, however, one printer can be cost-effectively attached to each display keyboard-based terminal, and users operating each terminal can generate printouts for editing, proofreading and approval. After correction, final documents are generated on a central printer.

Currently in the printing systems market, companies such as Centronics, Printronix, Diablo, Qume and Data Products Corp. and others offer units ranging from $900 to $5,000. The most expensive 80-column printing system Alphacom offers is priced at $595 per unit with print speed four times that of more expensive units.

Personal computer prices continue their drop, with the basic CPU price at $500 to $1500. The big fly-in-the-ointment is printer prices: many users cannot pay for a printer that costs two to four times the CPU! Big markets remain dormant. But, now the newer 20-, 40-, and 80-column printers, ranging from $175 to $595, provide many users hard copy capability at more-affordable prices.

but, can they deliver?
The printer boom continues. Inexpensive, fast and reliable models are the fuel behind sales. Can suppliers deliver? Key to this growth is suppliers meeting volume demands inherent in an expanding, price-competitive market. Will traditional, computer-oriented companies geared to lower-volume manufacturing requirements keep pace with demand and price changes? Not unless they change.

Some firms are well-positioned to take advantage of this growing market. For example, Alphacom of San Jose ensured its ability to deliver through an exclusive North American distribution agreement with Olivetti and manufacturing agreement with Rockwell, which invested over $2 million in production facilities for Alphacom's Sprinter Series.

Quality, volume and engineering support are keys to the printer field of the 1980s. Traditional companies specialize in limited-capability machines or market niches, making their products less flexible for the broader requirements of the OEM concerned with end users' immediate applications.

Low-Cost Graphic Systems Aid OEM Designers

In a major expansion of CAD/CAM product lines, firms are introducing low-cost graphics workstations and software packages configured for use by OEMs.

Avera of Scotts Valley, CA, has such a system. Its four workstations are built around a dual processor architecture based on Intel’s 16-bit 8086 microprocessor and an OS with 200,000 lines of Pascal code. The four workstation configurations include the GS1100, including 2 diskette drives, 192-KB parity memory, dual processors, two RS-232C ports, keyboard and control electronics, B/W display and control electronics, data tablet and control, 64-KB bit map, supplies and enclosures. GS1200 is like GS1100 with one diskette drive and one 10-MB Winchester drive. The GS1200 is like GS1100, but with a 13" color display. GS1220 is like GS1200 with one diskette drive and one 10-MB Winchester drive.

dual processor architecture
Key to the power of the workstations is a dual processor architecture with two 8086s sharing the command and graphics processing load, with the processor's arbitrating through a multitasking OS. One processor interprets commands, the other supports graphics. The main processor has 128 KB of RAM; the graphics processor, another 64-KB RAM plus a 64-KB bit map. Main storage RAM has parity checking, but the bit map does not. Memory (combined) can be expanded to a total of 1 MB.

graphics input and software
A 564-by-832 pixel CRT display is oriented vertically, with a 9"-by-12" viewing area and 24 on-screen functions that respond to cursor control. The graphics area contains 512-by-512 pixels. The display unit also features a two-digit LED display for indicating...
self-diagnostic codes and speaker to acknowledge a command input.

Software, designed for ease of use, is organized into five command groups: control, editing, manipulation, status and viewing — an organization that eliminates the need to display all commands simultaneously. Once a command category is selected, commands within that group are displayed. The user strings together functions and demands syntax of a given command. Using the data tablet, he draws symbols representing commands.

recursive data structure
Via the Pascal-based OS (common to all systems), a flexible recursive data structure is utilized. A recursive structure allows users to associate any graphics or text components in the data structure with other components to an arbitrary level of complexity by nesting. It forms hard associations; for example, a line can be associated with a symbol so that if the line is later moved, the symbol cannot be inadvertently left behind. Via an intermediate data structure for external communications, these systems are amenable to design partitioning and uploading to larger computers, including IBM mainframes.

CAD Package Improves Engineering Productivity
Advanced CAD software package Medusa provides complete 2-D and 3-D design, drafting and documentation. Based on Prime Computer's general-purpose 32-bit computer systems, Medusa enables designers to customize their own design system, a capability unavailable with turnkey or software-only offerings.

The system is packaged with its own integrated workstation, available with color or B&W terminals. Workstations are configured for easy access to control elements and provide a high 1000-line resolution display to enhance operation and increase performance.

The 2-D entry-level model is used for layouts, schematics and detailing tasks in mechanical, electrical, structural and electronic applications. The advanced 3-D model is for designing a complex 3-D object and then producing an engineering drawing. The workstation has a 19" display, joystick for easy manipulation and control of cursors, a data tablet, PT25 character-mode terminal and graphic controller.

Cost? Don't expect to buy one for your home computer lab. A typical entry-level Prime/Medusa system costs $235K and includes one Prime 250 CPU, 768-MB memory, one 96-MB disk drive and two workstations with B&W terminals. Licensed software includes 3-D Medusa, Primos, Fortran, Midas and CPL. Medusa software can be licensed separately at $30K and $60K for the 2- and 3-D models, respectively.
design
your
own
printer

If a standard RS-232
printer won’t work . . .
call us!

low cost

and oem
monitors

data ed
data-ed
18 Bridge St.
Salem, N.H. 03079

(603) 893-2047
TWX 710-366-0502
(UDENG SEML)

technology trends

scientific and engineering applications
to combat this problem. A single glance
can reveal in seconds subtle trends and
relationships that can take hours to
decipher from a table of numbers.

In a special OARS report, entitled
"Graphics in the Office," IDC of
Framingham, MA, forecasts a sharp
rise in the overall use of computer
graphics, averaging 35% growth per
year through 1984. In dollars, this
represents an increase in revenues
from just over $1 billion in 1979, to over
$4.5 billion in 1984. It certainly is no
revelation that graphics — pie charts,
bar graphics, etc. — are easier to
comprehend than a table of numbers.
Executives used graphics for presenta-
tion and analysis for years. What is new
is the concept of generating graphics
interactively without involving graphic
arts to bring immediate answers to
management’s questions. An example
of what can be done is the use of "what
if" gaming techniques, which allow the
manipulation of variables such as price,
return on investment, etc.

CAD/CAM systems are the domi-
nant force in the graphics market.
While CAD/CAM systems are much
more sophisticated and more expensive
than business systems, it is actually the
business applications market which
will show the fastest growth: shipments
of some $1 billion are forecast by
IDC for 1984. CAD/CAM systems
may dominate the overall market
dollarwise, but in terms of sheer
numbers, the business graphics market
will far surpass it in units shipped. In
fact, business applications will soon
rival CAD/CAM applications as the
major driving force. Most of the tech-
nology is in place; all that is needed is
to refine and tailor it to the specific needs
of business.

Display devices accounted for a little
over half of all graphics expenditures.
Hard copy devices accounted for just
over a third, while the remainder of the
expenditures went for such other equip-
ment as business/personal computers
and photographic output devices.

Things will change rapidly, how-
ever, on the computer graphics scene
over the next five years. Much of this
change will be due to a sharp rise in
the number of personal computers used
for graphics. Additionally, as the tech-
nology improves, the price of low-cost,
hard copy will begin to fall. These
devices — dot matrix printers/plotters,
color cameras, and ink jet printers, etc.
— will grow in numbers, though dol-
larwise shipments of these devices will
drop to 22% of the total business
graphics market by 1984. Furthermore,
IDC is predicting that business/
personal computers will account for
20% of the graphics market (by dollar
value) in 1984. Display devices will dip
slightly — to under half of total ex-
penditures at that point, while photo-
graphic equipment will rise to ap-
proximately 8% of the market.

Display devices use three primary
technologies: the direct view storage
tube (DVST), raster refresh tubes, and
random scan tubes. Each of these tech-
nologies has its own cost/performance
trade-offs. IDC views raster tubes
(which operate much like a TV set) as
the technology of choice for business
purposes mainly due to high-quality
color, good resolution, selective
erasure, and the ability to display
photographic images. The big draw-
back to raster scans right now is cost.
The images of raster scan must be
refreshed many times a second, and this
requires the definition and storage in
memory of every pixel (picture ele-
ment), whether part of the image or not.
Obviously, the memory and processing
cost in this method are prohibitive, but
as memory costs continue to drop it will
become less of a factor.

The other methods of display men-
tioned also have their pros and cons.
Direct view storage tubes, for example,
don’t need to be refreshed 30-60 times a
second, and they offer high resolution
at low cost. However, selective erasure
is not possible in a DVST, and low light
output is another factor to be con-
sidered. Random scan tubes offer
selective erasure and higher resolution
than raster refresh tubes, but only
limited color. These displays have been
employed mainly by the engineering/
scientific community where resolution
is very important and color less so.

Of the 180,000 shipments of display
devices forecast in 1984 by IDC, 75%
will be raster scan tubes. Additionally,
approximately 90% of these will be
color tubes, as compared to 63% for
raster tubes shipped in 1979. Users will
drive the graphics display market
toward increasing use of color graphics
for business applications.

With color displays soon to dominate
the market, the demand for color hard
copy will also increase dramatically.
Color displays and color hard copy
devices will grow hand in hand. If
inexpensive, convenient hard copy
output devices are slow in coming, we
can expect this to have a dampening
Remote Terminals

JAPAN: Matsushita is planning to bring CAD into the Japanese home. The principle is that a lady customer, shopping for dresses is filmed by video camera. The video film, together with size statistics, is stored by company. Whenever the shopper wants to buy a dress, she telephones the company, her film is recalled from data and displayed on TV. Dresses are then superimposed on image as though she were trying them on. Hopefully, she will select one that looks good on her.

BARBADOS: A $9 million plant (with more than 100 employees) for manufacturing resistors has opened on this Caribbean island.

Backer is TRW of the US. The range of resistors is designed for a variety of electronic systems from basic telephone equipment to sophisticated space research.

LONDON: Scientific Calculations has opened a London office. The company produces printed circuit designs and applications.

SOMALIA: This country has become the 106th member of INTELSAT (International Telecommunications Satellite Organization.) INTELSAT operates the global satellite system that provides 2/3 of the world’s international telecommunications services.

FRANCE: British and French telecommunications officials have agreed to adopt a new technical standard for Viewdata by the mid-1980’s. This will end the rivalry between Britain’s Prestel and the French Antiope. A working method with Germany is also being developed. Japan has been waiting for such an agreement and should be among the first to produce new standard Viewdata terminals. Viewdata transmits such things as telephone directories service (500,000 directory terminals for France alone); electronic mail; stock market; news; information; etc.

IRELAND: A high technology research center is being set up in Limerick. It will concentrate on the application of electronic technology and the material sciences with particular emphasis on alternate energy sources.

ITALY: The Italian Olivetti group is acquiring control of the Swiss company, Hermes Precisa, manufacturer of office equipment.

WEST GERMANY: Production of West Germany’s electronics industry rose 4.9% to $44.5 billion in 1980. This increase occurred despite the recession. (1979, however, was a much better year.)

HAWAII: The Fourth Annual Pacific Telecommunications Conference takes place Jan. 18-20, 1982, at the Ilikai Hotel, Honolulu. (Never too early to plan for such events.) Papers and exhibits invited. Contact Richard J. Barber, (Director), 1110 University Ave., Suite 303, Honolulu, HI 96826.

SINGAPORE: A conference and exhibition for the quality control/quality assurance field in Southeast Asia has been scheduled for June 17-19, 1982 in Singapore.

HONG KONG: A new firm has been launched to manufacture magnetic recording heads. The company is SAE Magnetics (H.K.) Ltd., a division of Stanford Applied Engineering Corp. of Santa Clara, CA.

SCOTLAND: The worst recession in Great Britain since the 1930’s has served as a stark contrast to the continuing growth and prosperity of the energy and electronics industries in Scotland. Scotland has been the home of several American firms for about half a century and has been attracting high-technology manufacturers for decades. The 1970’s, however, has seen a strong burst of growth in the high technology areas, spurred by government financial incentives, a growing pool of skilled labor, research and development resources, and experienced executives willing to start new ventures.

Effect on the color display market. By the same token, if color hard copy output becomes available quickly, then the color display market will be boosted.

What’s in store for users regarding output devices? Quite a few things, including: color cameras — useful for the preparation of slides, transparencies, and color microfilm; photo-composition devices — offering superior resolution previously available only to graphics designers, and dot matrix printer/plotters — simple adaptations of alphanumeric matrix printers, which can not only produce shades of gray, but by striking over can also produce color.

Whether you have a need for three phase or single phase AC power control. Marway Products has a high quality, low cost unit available to satisfy you. In fact our DEC interchangeable units are so economical that we are attracting a large following of non-DEC OEM’s, system integrators, and quantity end users.

Marway’s three phase power controllers are mechanically and electrically interchangeable with the DECIVAX model 889 and feature:

- Model MPD 416 for 240/416 VAC @ 45 amps
- Model MPD 208 for 120/208 VAC @ 90 amps
- 18 AC receptacles — 6 unswitched
- 12 switched
- High level control bus
- High performance EMI line filter
- Pricing: MPD 416—$1375.00
- MPD 208—$1650.00
- Availability: 30 days ARO

Marway’s MPD 115 and MPD 230 AC power controllers are mechanically and electrically interchangeable with the DEC model 861 and feature:

- Control of 115 or 230 VAC @ up to 30 amps
- Twelve AC receptacles — 4 unswitched, 8 switched
- High performance EMI line filter
- Pricing: $325 (MPD 115)
- Availability: off the shelf

Additional Marway models that are available to meet your needs are: The MPD 110, the lowest cost rack mountable unit, priced at $149.00, and the MPD 117, the floor or wall mountable unit for use in the office or personal computer environments, priced at only $89.00.

For more information, please call or write:

M AR W AY P R O D U C T S I N C .
17747 S. Birch Street, Santa Ana, CA 92707 (714) 549-0623

Circle 15 on Reader Inquiry Card
Factory Systems

Based on the experience of hundreds of Japanese factories diagnosed and advised by the author during his ten years as a factory management and production control consultant. It is used by more than 4,000 factories in Japan today.

With instructions on how to use them.
All reproducible for in-plant use.
Bound looseleaf in slipcover.

Price: $80.
Pre-Publication Price: $60. Prepaid (Until August 1, 1981)

CONTENTS
Chapter 1 ANALYSIS
Analysis Manual
Analysis Master Sheet
Processing Cost Analysis Chart (1)
Productivity Analysis Chart
Analysis of Processing Cost for Selling Price Based on a Set Rate and Selling Price Based on Performance
Calculation of Overhead by Category
Profit and Loss Analysis by Customer and by Product
Profit and Loss Analysis by Division
Analysis of Personnel Expenses and Labor Cost Distribution Rate
Analysis of Conditions Necessary for Improvement of Labor Productivity
Quality Control Check Sheet (1)
Quality Control Check Sheet (2)
Punctual Delivery Check Sheet
Operation Rate Survey Work Sampling Statistics Sheet
Operation Rate Survey Work Sampling Sheet (1)
Operation Rate Survey Work Sampling Sheet (2)
Plant and Equipment Check Sheet
Total DEC Compatibility with the ComPll-LE

And much more . . .

The ComPll-LE, which is equivalent to the DEC BAIL-LE™, is a general purpose PDP-II™ expansion mounting chassis. The 120V ac input power unit supplies 32 amps of output power at +5Vdc with regulators to support either MOS or core expansion memory.

The chassis can be equipped optionally with up to two Comp-CK or one Comp-DK (DEC DDII-CK and DDII-DK equivalent backplanes) units, enabling the ComPll-LE to support a wide variety of PDP-II systems.

. . . For a lot less

For more information call or write:

COMPUMATION
2326 Walsh Avenue
Santa Clara, CA 95051
(408) 988-8600

“DEC BAIL-LE is a trademark of Digital Equipment Corp.”
SIGMA's chassis can be the beginning of DEC based systems or can provide expansion for Unibus or Q bus devices.

ANOTHER Σ SIGMA INFORMATION FIRST!
Sigma chassis provide low-cost, flexible configurations for your DEC systems. The complete line of 5.25” and 10.5” chassis provide mounting space and power for Unibus and LSI-11 series systems, as well as almost any combination of floppy/Winchester/tape cartridge drives. Most chassis include an 8-row quad backplane and front operator control panel. Some are available in either tabletop or rackmount versions with styles that are easy on your eyes and prices that are easy on your total system cost.

Sigma is in the business of serving DEC users. Chassis are optionally available with CPU's, memories, controllers, interfaces, etc., depending on client needs.
Sigma personnel are experienced in design and development of DEC-related products and have a comprehensive background in system compatibility. This expertise is available to develop chassis with user-configured front panels, power supplies, backplanes and drive enclosures.

Sigma Sales 6505C Serrano Ave. Anaheim, CA 92807

Circle 34 on Reader Inquiry Card
Shortened Algorithm

speeds DFT computation

A shortened Discrete Fourier Transform (DFT) or SDFT algorithm was developed to achieve real time processing. Use is made of new fast components such as video A/D converter, multiplier/accumulator, RAM and PROM. A DFT processor based on the shortened algorithm can calculate power spectrum of 32 samples in about 300 µs, giving a maximum sampling rate of 100 KHz.

by Dan Cohen and Avidgor Margalit

A number of methods for the realization of a digital real time DFT processor have been published in recent years. In the past, contemporary technology limitations on the speed of digital components, especially multipliers, prevented the realization of a satisfactory processor. The introduction of new components, such as the monolithic multiplier/accumulator family and video 30 ns-6 to 10 bit ADCs helped solve some major problems. We describe a new method which, with the aid of new components, permits realization of a satisfactory real time DFT processor.

SDFT is fourfold faster

This shortened algorithm for DFT (SDFT) calculation method fills in the gap between a complicated fast FFT processing and a simple-but-relatively-slow direct DFT computation. Use of shortened DFT gives a four times faster processor in comparison with a direct DFT assuming the

Dan Cohen and Avidgor Margalit are from Haifa, Israel.
same techniques of realization. Such a processor for 32 points was designed and built by the authors, fulfilling the expectations of a fast, low power, low volume and low price unit. A 5-W, one-board processor computes a 32-point DFT in less than 300 μs (100 KHz sampling rate), for less than $500 (qty. 100).

**direct DFT**
The DFT is defined as

\[
S(m) = \frac{1}{N} \sum_{n=0}^{N-1} x_n \exp\left(-\frac{2\pi i}{N} (m n)\right)
\]

(1)

where “exp” signifies a base e (or natural) exponential; \(m, n = 0, 1, 2 \ldots N-1; x_n\) samples are taken at \(\Delta t\) intervals; \(x_n\) are real or complex sample values; and \(N\) is the total number of samples in an integration.

Direct DFT is calculated by solving Eq. 1 for each \(m\) separately. This is the simplest way to realize the processor, hence the name “direct.” Despite its simplicity, the introduction of such a processor does cause difficulties in fast real-time systems.

The shortened DFT method eliminates these difficulties by reducing the number of complex multiplications (\(N^2/4\)) by a factor of 4.

**shortened DFT or SDFT**
As is well known, an FFT processor implies \(N\log_2 N\) multiplications, while direct DFT processing requires \(N^2\) multiplications (\(N\) is the processing block length). This number of multiplications can be reduced by partial realization of the FFT algorithm (theoretically it could be done until the complete FFT algorithm is achieved), according to the following equations:

\[
\exp(-j2\pi r/N) = (-1)^r \exp(-j2\pi r/N)
\]

(2)

\[
S(m) = \frac{1}{N} \sum_{r=0}^{N/2-1} \left\{ X_r \exp(-j2\pi rm/N) + X_r \exp\left(-\frac{2\pi i}{N} (m + N/2)\right) \right\}
\]

(3)

Substituting Eq. 2 into the second expression on the right-hand side of Eq. 3 we obtain:

\[
S(m) = \frac{1}{N} \sum_{r=0}^{N/2-1} \exp\left(-j2\pi rm/N\right) X_r + (-1)^{m} X_r \exp\left(j2\pi r m/N\right)
\]

(4)

**Eq 4** shows a reduction of the number of multiplications in the frequency domain. That means \(N^2/2\) multiplications instead of \(N^2\) in the direct DFT. On the other hand this algorithm adds \(N\) additions/subtractions in the time domain, which results in addition of 1 bit to the input dynamic range.

An additional reduction of the computing time for real signals is achieved by using:

\[
S(N-m) = S^*(m)
\]

(5)

This indicates that the whole procedure is reduced to computation of the spectrum \(S(m)\) for \(m = N/2\), and then computation of its conjugate \(S^*(m)\). Thus, \(N^2/2\) multiplications for computation of \(S(m)\) and \(N/2\) additions for computation of \(S^*(m)\) will complete the procedure. When quadrature channels are used, each channel should be computed separately.

In summary, the shortened DFT algorithm will produce the spectrum after the following computations:

- \(N^2/4\) multiplications,
- \(N\) complex additions in the time domain and \(N/2\) real additions in the frequency domain.

**realization of shortened DFT**
Realization of a direct DFT filter depends on desired specifications: sampling rate, block length, power dissipation, volume, price etc. The most convenient realization, the serial method, utilizes a multiplier/accumulator and satisfies most typical system requirements — except for the case of very high-sampling-rate systems. It is possible to overcome this shortcoming by paralleling two serial processors for a single channel or four serial processors for quadrature channels.

**Fig 1** describes a serial realization of the shortened DFT method. Quadrature video signals \(X_I\) and \(X_Q\) are sampled by
an analog switch and converted by a single ultra-high-speed A/D converter, resulting into two binary words represented in fractional 2s complement notation. The classical A/D conversion of quadrature channels has been achieved by two parallel assemblies each containing S/H, A/D, and a register in series. Although the shortened method saves two S/H, one A/D and two registers, it requires a faster A/D and analog switch in order to reduce the inaccuracy due to delay between samples from the two channels. Fortunately, new components make possible the realization of this method. For our purpose we chose the 4066 bilateral switch and TDC 1014J A/D converter (6 bit, 30 nsec).

Assuming N = 32, the first 16 converted samples of each block are stored in a 8 bit word-length RAM (I and Q channels separately). Starting with the 17th sample, their binary equivalents are not stored directly but are transformed into new expressions according to Eq. 4. For example, X(16) transforms into X(16) + X(0) and X(16) - X(0), or X(31) into X(31) + X(15) and X(31) - X(15). This transformation adds one bit to the original word length, so the RAM has to be enlarged accordingly. Therefore two 931422 TTL-Ts RAM were chosen (75-nsec access time, 250-mw power dissipation). Fig 2 describes RAM organization during the two phases, between the 1st and the 16th and between the 17th and the 32nd samples.

The procedure mentioned above occurs at the sampling rate and spends only a small portion of the time interval between two samples. For example, with sampling rate of 10 kHz, the duration of A/D conversion, read memory, add or subtract, and write memory for quadrature channels is about 400 nsec, or only 0.4% of the sampling cycle. The remaining 99.6% of the time is exploited for DFT processing of the preceding block of samples (W and WQ in Fig 2).

The processing unit is based on an 8 x 8 multiplier/accumulator TDC 1008J (it could be 12 x 12 or 16 x 16 according to specific demands). This component performs multiplications, accumulations, squaring, and additions (A + B = A x 1 + B x 1; A - B = A x 1 - B x (-1)) according to the algorithm described in a following section, "shortened DFT algorithm," resulting in a power spectrum for each m (A.11). Word length considerations are presented in a following section, "word length considerations," indicating the specific bits that are ignored as noise, others that are compared with a calculated margin level and finally those that are detected directly by a limiter.

**shortened DFT algorithm**

Spectral line S(m) normalized to 1/N is:

\[ S(m) = \sum_{r=0}^{N/2-1} \left\{ \exp(-j2\pi mr/N) \left[ X_r + (-1)^m X(r+N/2) \right] \right\} \]

**A1**

if \( Y_r = X_r + (-1)^m X(r+N/2) \)

then quadrature channels are expressed as:

\[ Y_r = Y_{Ir} + jY_{Qr} \]

**A2**

Combining Eq A1 with A3 and substituting the Euler expressions for the exponent we obtain:

\[ S(m) = \sum_{r=0}^{N/2-1} Y_{Ir} \cos(2\pi rm/N) + \sum_{r=0}^{N/2-1} Y_{Qr} \sin(2\pi rm/N) \]

**A4**

\[ \text{if: } a = \sum_{r=0}^{N/2-1} Y_{Ir} \cos(2\pi rm/N) \]

\[ b = \sum_{r=0}^{N/2-1} Y_{Ir} \sin(2\pi rm/N) \]

**A5**

\[ c = \sum_{r=0}^{N/2-1} Y_{Qr} \cos(2\pi rm/N) \]

**A6**

\[ d = \sum_{r=0}^{N/2-1} Y_{Qr} \sin(2\pi rm/N) \]

**A7**

The real expression will be:

\[ g = a + d \]

**A9**

The imaginary one will be:

\[ h = c - b \]

**A10**

The final result for the power spectrum will be:

\[ PS(m) = g^2 + h^2 \]

**A11**

**word length consideration**

The following explanation will be accompanied by a numerical example based on: number of DFT points per block (32), input dynamic range of quantized video signals (6 bits), noise level of white Gaussian noise (\( \Sigma X_0 = 0 \); \( \sigma_{n-1} \) LSB and coefficient accuracy (form = 32) (5 bits).

According to the DFT algorithm, quantized input signals are processed to obtain new 7-bit-long expressions. The result is a 12-bit word. Accumulator of 32 multiplications adds to the result 5 bits at the most. In order to avoid truncation, a 17 bit word is needed. Assuming the noise level of 1 LSB is accumulated according to \( N^0.5 \) law, at the end of the process the noise level will reach the 9th bit out of the 17th result.

Calculations of g, h (see the previous section), their squares and the PS(m), are performed while ignoring 8 LSB (which are considered noise). Thus, if the processing unit is based on an 8 x 8 multiplier accumulator, only bits 9 to 16 are considered for obtaining PS(m). The 1 MSB indicates immediately existence of a signal for the proper m.

**calculation time**

Calculation time of 32 points DFT processor based on the shortened algorithm is based on the following data: Q (quadrature) = 2, TSW (switch on) = 200 ns, TAD (A/D conversion) = 30 ns, TWR (write RAM) = 75 ns, TRR (read RAM) = 75 ns; TLS (LS-TTL operation) = 30 ns, TAP (read PROM) = 125 ns and TMA (multiply/accumulate) = 125 ns.

Duration of sampling, A/D conversion, additions and writing in RAM on 32 quadrature input signals: \((N/2)\) (TSW + Q (TAD + TWR)) + (N/2) (TSW + Q (TAD + TWR + TLS + TWR)) = 16.5 \( \mu \)s. Multiplication/accumulation time of a complete block: \((N/2)\) (TAP + TMA) + TLS = 256 \( \mu \)s. PS(m) calculation time of 32 spectral lines: (2N/2)(2 x 2 x (TLS + TMA) + TLS + TMA) = 24.8 \( \mu \)s. Total calculation time is approximately 300 \( \mu \)s; and maximum sampling rate, 100 kHz.

**references**

Barney Stevenson just spent two years programming and de-bugging a process control system in assembly code.

Now Barney thinks he deserves some congratulations for his efforts.

Sorry Barney,

NO CIGAR.

Barney Stevenson thought he deserved a pat on the back. As project manager at Smart Widgets, Inc., he had taken on the biggest real-time process control headache of his life. And after 24 months he'd finally succeeded in programming and de-bugging Smart's newest product.

We think Barney missed the boat.

Barney thought it was simple. High level languages like Pascal and Fortran could program quickly, but would run too slowly and take up too much memory. Assembly code would take longer to program and de-bug, but was the only answer for real-time applications. Wrong. Real wrong.

Barney didn't know about FORTH: a language that runs nearly as fast as assembly, is just as compact (if not more so), yet can cut development time by a factor of 10 over assembly language.

He also didn't know about FORTH, Inc. They're the people who invented this remarkable tool, evolved it, and for 10 years have seen it used in thousands of applications... from running an observatory to sorting baggage, from video games to industrial robotics. Virtually every real-time application imaginable.

The latest evolution of FORTH is called polyFORTH: An incredible programming environment available for just about any mini or micro processor.

For Barney? Still no cigar. But for you, FORTH offers a software tool that in speed, compactness and extensibility, simply has no match.

So call us at (213) 372-8493. Or write FORTH, Inc., 2309 Pacific Coast Highway, Hermosa Beach, California 90254. We'll rush you the latest on polyFORTH: and tell you where you can see it in action.

FORTH, Inc.
...the real-time saver.

Circle 75 on Reader Inquiry Card
Microprogrammable Processor

single-bit storage concept

The single bit storage concept is adaptable and may be varied to meet systems requirements. Expanding bit storage is an efficient method, and permits a doubling of total data bits stored for each added bit of microcode. The ease of enable control circuitry modification, which changes the division between latches assignable to status bits only, (or to either status or flag bits,) permits rationalization of system requirements and design implementation.

by Alan W. Bentley

This design illustrates the principle of simultaneous and rapid processing. On a given microcode instruction, one flag status bit may be modified while several other bits may be referenced by different sectors of the microcode which are performing independent functions. Finally, latches differ from edgetriggered-storage devices as the latch-enable activates input gates, permitting track of D input during enable time.

At enable completion, the latch stores the last internally propagated input. Therefore, because the latch is enabled during the second half of the clock period, the latch input stabilization time is maximized to permit proper status storage. Specific instructions, however, may have long execution times.

Although instruction driven microprocessors fulfill the majority of processing applications, the high capability portion of the performance spectrum is dominated by microprogrammable processors. This follows from their architectural differences. An instruction driven microprocessor is a serial device with a fixed architecture and a given repertoire of instructions. Its performance is limited by the necessity of sequentially executing those instructions. Its operating modes are relatively inflexible and it is difficult to adapt either the instruction set or the architecture to increase performance. Conversely, the microprogrammable organization is more flexible. It is packaged as vertical slices through a register array, arithmetic and logic unit, instruction decoding and execution logic and connecting paths.

Interconnecting slices establishes bit widths of the data word and processing unit. To support and control the processing unit, additional hardware is added and microcode instruction control is implemented. Processor performance is improved by increasing the number of tasks that may be performed simultaneously. This is achieved by expanding the support hardware and the microcode, obtaining a finer division of tasks and an increased capability to manipulate control and enable lines. Thus, the increased performance of a microprogrammable processor system is due to its organization which permits a number of tasks to be performed simultaneously.

single bit storage concept

In microprogrammable processor design, microcode controlled storage for status and flag bits must be provided. An approach has been developed that uses both microcode and hardware efficiently, and is adaptable, so it may fulfill varying system requirements. An 8-bit multiplexer (LS151) and an 8-bit addressable latch (LS259) perform the data selection and storage functions, controlled by 4 bits of microcode. The lower three bits of microcode \((2^0 - 2^2)\) address both the multiplexer and the latch, the upper code bit, \(2^3\), is used as a multiplexer strobe and when true, drives its output false. Also, the upper two code bits, \(2^2\) and \(2^3\), when both true, suppress the latch enable. This divides the microcode word into three sectors; \(0_{16}\) through \(7_{16}\) stores the

(text continued on page 33)
Build your own DEC system with CRDS...

**MF-211**
10½" Enclosure for LSI 11/23 System with built-in RX02 equivalent floppy disk system. Available with or without processor and memory.

**HD-11/T**
20.8 Megabyte Winchester disk software equivalent to 4 RL01 units. Optional cartridge tape backup.

**FD-311**
RX02 equivalent dual floppy system, single or double sided. Includes bootstrap loader, self-tester, formatter and diagnostic diskette.

**MB-211**
5¼" enclosure with 8 quad slot backplane. Front panel console with switches for Enable/Halt, Boot/Init and Line Time Clock.

**Complete software compatibility at a savings!**

With CRDS, you can configure your own DEC system and be assured of complete software compatibility. Each of the above systems is provided with slides for rack mounting or can be used in desk top applications. All DEC LSI 11 based modules and associated software packages are available through CRDS, if desired.

**Attractive Packaging**
Careful attention is given the CRDS repertoire of enclosures in assuring you an attractive yet comfortable blending of product in the DEC environment.

**Significant Savings**
Flexibility of procurement plus attractive OEM schedules allows you to optimize dollar savings in configuring your CRDS system. Use the time tested technique. Compare.

**Warranty and Maintenance**
A 90 day warranty is offered with your CRDS system. In the event of malfunction, by use of provided diagnostic routines, the defective submodule is normally found within minutes. After verification with the CRDS Maintenance Department, a replacement for your defective module will be promptly forwarded.

Call or write for a comprehensive literature package and prices.
### Table 1: Microcode and input assignment for typical 8-bit storage application.

<table>
<thead>
<tr>
<th>Usage Assignment</th>
<th>Multiplexer Input</th>
<th>Connection</th>
<th>Output Latch</th>
<th>Microcode Flag Set</th>
<th>Reset</th>
<th>Status Storage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flag 0</td>
<td>D0</td>
<td>VCC</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Flag 1</td>
<td>D1</td>
<td>VCC</td>
<td>1</td>
<td>1</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>Flag 2</td>
<td>D2</td>
<td>VCC</td>
<td>2</td>
<td>2</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Status A</td>
<td>D3</td>
<td>Parameter A</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status B</td>
<td>D4</td>
<td>Parameter B</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status C</td>
<td>D5</td>
<td>Parameter C</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status D</td>
<td>D6</td>
<td>Parameter D</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status E</td>
<td>D7</td>
<td>Parameter E</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Microcode B_{16} illegal — use unconditionally resets Q_3, status a latch
2. Microcodes C_{16} - F_{16} surpass latch Enable input

### Table 2: Microcode and input assignments for a 16-bit application with 6 status bits, that are handled by one multiplexer. For flag bits 0 through 7, the 2^1 bit is the octal latch D input, requiring that the flag bit set and reset microcode be reversed from those in Table 2.

<table>
<thead>
<tr>
<th>Usage Assignment</th>
<th>Multiplexer Input</th>
<th>Connection</th>
<th>Output Latch</th>
<th>Microcode Flag Set</th>
<th>Reset</th>
<th>Status Storage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flag 0</td>
<td>D0</td>
<td>VCC</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Flag 1</td>
<td>D1</td>
<td>VCC</td>
<td>1</td>
<td>1</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>Flag 2</td>
<td>D2</td>
<td>VCC</td>
<td>2</td>
<td>2</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Flag 3</td>
<td>D3</td>
<td>VCC</td>
<td>3</td>
<td>3</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td>Flag 4</td>
<td>D4</td>
<td>VCC</td>
<td>4</td>
<td>4</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>Flag 5</td>
<td>D5</td>
<td>VCC</td>
<td>5</td>
<td>5</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>Status A</td>
<td>D6</td>
<td>Parameter A</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status B</td>
<td>D7</td>
<td>Parameter B</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status C</td>
<td>D0</td>
<td>Parameter C</td>
<td>8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status D</td>
<td>D1</td>
<td>Parameter D</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status E</td>
<td>D2</td>
<td>Parameter E</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status F</td>
<td>D3</td>
<td>Parameter F</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status G</td>
<td>D4</td>
<td>Parameter G</td>
<td>12</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status H</td>
<td>D5</td>
<td>Parameter H</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status I</td>
<td>D6</td>
<td>Parameter I</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status J</td>
<td>D7</td>
<td>Parameter J</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:**
1. Microcode 16_{8} + 17_{8} illegal, use unconditionally resets its 6 and 7 respectively
2. Microcodes 30_{8} - 37_{8} suppress latch Enable input

### Table 3: Expansion to 32 bits of storage. For each octal latch, shown is its enable equation and its microcode assignment.

<table>
<thead>
<tr>
<th>Microcode</th>
<th>Enable Equations</th>
<th>Use</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>00_{8} - 17_{8}</td>
<td>Clock · 2^1 · 2^4</td>
<td>Flag Only</td>
<td>Set 10_{8} - 17_{8}, Reset 00_{8} - 07_{8}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Flag or Status</td>
<td>Multiplexer input 00_{8} - 07_{8}, Low input 10_{8} - 17_{8}</td>
</tr>
<tr>
<td>20_{8} - 37_{8}</td>
<td>Clock · 2^1 · 2^4</td>
<td>Flag Only</td>
<td>Set 30_{8} - 37_{8}, Reset 20_{8} - 27_{8}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Flag or Status</td>
<td>Multiplexer input 20_{8} - 27_{8}, Low input 30_{8} - 37_{8}</td>
</tr>
<tr>
<td>40_{8} - 57_{8}</td>
<td>Clock · 2^1 · 2^4</td>
<td>Flag Only</td>
<td>Set 50_{8} - 57_{8}, Reset 40_{8} - 47_{8}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Flag or Status</td>
<td>Multiplexer input 40_{8} - 47_{8}, Low input 50_{8} - 57_{8}</td>
</tr>
<tr>
<td>60_{8} - 77_{8}</td>
<td>Clock · 2^1 · 2^4</td>
<td>Status Only</td>
<td>Multiplexer input 60_{8} - 67_{8}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Status or Flag</td>
<td>Enable Suppressed 70_{8} - 77_{8}</td>
</tr>
<tr>
<td>Clock · 2^1 · 2^4</td>
<td>Clock · 2^1 · 2^2</td>
<td>Status or Flag</td>
<td>Q_1 - Q_3 Status of Flag Use</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Q_4 - Q_7 Status Use Only</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Enable Suppressed 74_{8} - 77_{8}</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Three latches may be assigned flag only or flag or status use, corresponding multiplexer only requires in later case.
2. If flag only, the latch D input is microcode 2^1 bit, if flag or status the same input is multiplexer Y output.
3. One latch normally assigned status use only, alternate enable equation and configuration shown if assigned to status or flag use

Digital Design JULY 1981
Who makes NTDS interfaces for PDP-11, VAX and LSI-11?

Rockwell, Rockwell and Rockwell.

It's true. Rockwell International NTDS interfaces provide the communications link between the three DEC computers and USN standard tactical computers, or NTDS peripherals with FAST, SLOW or ANEW input/output channels.

This interface equipment performs all NTDS transfers including input, output, external function and external interrupt. And it allows PDP-11, VAX and LSI-11 to respond as a peripheral to the NTDS computer, or to perform as a computer to NTDS peripherals, or to communicate via intercomputer channel.

In addition, software drivers are available at no cost.

Figure 1: Sixteen bit storage with 8 or fewer status bits. Parameter selection performed by single multiplexer.

**INSTANT REAL-TIME CONTROL**

Dynabyte's BASIC CONTROLLER is a versatile measurement and control computer that can:

- Directly sense mechanical contact closures and/or digital logic levels
- Measure and generate analog signals
- Perform arithmetic computations, detect limits and manipulate data
- Directly control electronic and electromechanical devices
- Communicate with computer peripherals

All this and more in a single-board system that includes ZIBL™ an easy-to-use BASIC programming language which features special commands for direct input/output control. Call or write today for free descriptive literature.

Circle 21 on Reader Inquiry Card
We're in the mass storage business. State of the art mass storage—and we're specialists. Our line of tri-density magnetic tape subsystems represents state of the art technology and total reliability. Because there's more to mass storage than capacity—it's got to work.

If you're a DEC, Perkin-Elmer or Raytheon user, we've got news for you. IPS has the highest performance tape subsystems around. With features like: Telex, STC or Pertec drives; Dual-Density (1600/6250 BPI) or Tri-Density (800/1600/6250 BPI) capabilities; tape speeds up to 125 ips; storage capacity up to 180 megabytes per reel; a 32K Byte FiFo buffer; and Data Chaining for reading and writing gapless tapes. We also offer complete, integrated subsystems or individual control units.

For performance and reliability: IPS works.

IPS
6567 Rookin St.,
Houston, Texas 77074
Phone (713) 776-0071;
wire IPS-HOU TELEX 792413
Regional offices located in Ca. and Mass.
Figure 2: Sixteen bit storage handling more than 8 status bits. Two multiplexers are needed to provide adequate parameter selection.

**LSI-11 SYSTEMS FROM ANDROMEDA**

Any size you want.

No matter what your LSI-11 system needs are, Andromeda can satisfy them.

For example, the 11/M1 system shown on the right weighs only 14 pounds yet contains 102kb of mini disk storage (expandable to 389kb), 64kb of RAM, space for up to 16kb of EPROM, 4 serial ports, and the LSI-11/2 CPU. All of this for less than $4000. While the 11/M1 will run the RT-11 operating system, it is best suited for dedicated applications where its small size but large processing power are needed.

Near the other end of the scale is the 11/H23-DF system shown at the left. The mobile enclosure includes the LSI-11/23 processor, 256kb main memory, 10mb of storage on the double density RK-05 cartridge disk and 1.2mb on the double density floppy disks. This system also has 4 serial ports and 7 empty dual width slots for additional interfaces. The $22,500 price includes the video terminal shown, a 150 CPS matrix printer, and the RT-11 operating system.

These are just two examples of the many LSI-11 based systems available from Andromeda. And the standard systems are just starting points; we will provide any combination of package, processor, memory, interfaces, and peripherals to meet your requirements. In addition to general purpose systems, we also have turnkey packages for word processing, time-sharing, data acquisition, and graphics.

We also provide individual boards, software and accessories to support LSI-11 systems. LSI-11, RT-11, and RK-05 are trademarks of the Digital Equipment Corp.

Circle 23 on Reader Inquiry Card
logic level of the addressed multiplexer input in the corresponding latch, $8_{16}$ through $B_{16}$ cause the multiplexer output to be false, resetting latches $0$ through $3$ respectively, and $C_{16}$ through $F_{16}$ suppress the latch ENABLE command, leaving the latched outputs unchanged.

During systems operation, there are two categories of single bit information that must be stored for later use; they are the status and flag bits. Status bits are associated with specific parameters and store their values when programmed. Examples of such parameters are: sign bit, carry out bit and the result of a register equal zero test. Conversely, flag bits are not associated with specific parameters, rather they may be programmed set or reset, and system requirements determine their definition. Therefore, to store a status bit only one microcode is required, the parameter is routed from the corresponding multiplexer input and the coded latch stores the digital value. Flag bits require both a setting and resetting microcode, which are formed by code pairs differing by the $2^3$ bit. If the $2^3$ bit is false, the multiplexer input, tied to $V_{CC}$, sets the addressed latch. If it is true, the multiplexer strobe input causes the multiplexer output to be false, resetting the latch. Thus, if the multiplexer D1 input is tied to $V_{CC}$ microcoding $1_{16}$ sets $Q_1$ and $9_{16}$ resets $Q_1$.

When assigning microcodes and multiplexer inputs, codes $C_{16}$ through $F_{16}$ suppress the latch ENABLE command. Codes $4_{16}$ through $7_{16}$ control latches $Q_4$ through $Q_7$ respectively and must be assigned as status bits. Codes $0_{16}$ through $3_{16}$ paired with $8_{16}$ through $B_{16}$ control $Q_0$ through $Q_3$ and may be assigned as either status or flag bits. Table 1 shows a typical application, that requires 3 flag and 5 status bits. Shown for each bit is its assignment, multiplexer input, controlling microcode and latch output. Typically, the required number of status bits exceeds the number of flag bits. The division of 4 status bits and 4 bits assignable to either the status or flag category is satisfactory. If not, by expanding the input gate of the ENABLE circuitry to include the $2^3$ microcode bit, the microcodes that inhibit ENABLE are reduced to $E_{16}$ and $F_{16}$. The latches assigned to status bit only are reduced to $Q_6$ & $Q_7$. The remaining 6 latches may be assigned to either the status or flag category.

storage expansion

The flexibility of this approach allows expansion, if additional bit storage is required. Generally, each bit added to the microcode doubles the capability of storing status or flag bits, and to implement this capability, multiplexers and octal latches are added in equal numbers. However, if a latch is used to store flag bits only, its corresponding multiplexer is not required, for with proper address assignments, a microcode bit can supply the D input to the flag latches.

For expansion to 16 bits of storage with more than 8 status bits required, the hardware configuration is shown in Figure 1 with the input connections and coding shown for a typical assignment in Table 2. If 8 or fewer status bits are required, the reduced hardware configuration of Figure 2 may be used. Three variations of the ENABLE equation are shown; with the enable inhibit gate progressively expanded, to reduce both the microcode combinations that are inhibited and the number of latches committed to status bit use only. Thus, the implemented latches are divided between the two categories by adjusting the ENABLE equation.

Controlling four octal latches with a 6 bit microcode illustrates the principle of expansion. Table 3 shows each latch's specific design information, and alternate configurations that permit design optimization.
Group-coded recording (GCR) of data onto magnetic tape has been around for a number of years. IBM first announced it in 1973. Even though GCR increased data recording rates and reliability, most manufacturers originally stayed out of the GCR race. They felt that improved tape rate and reliability would prove unnecessary, because other storage media (such as disk) might push tape aside. They were wrong: the GCR tape market, $3.5 billion four years ago, should reach three times that in 1981-82. Today, over 70% of large computer systems installed in the U.S. utilize GCR-equipped tape subsystems.

Why this dramatic growth? The reason: tape remains the least expensive medium for data storage — approximately one-tenth the cost of disk. It is the only legal electronic means of archiving data, and is the most interchangeable medium.

Designing faster tape drives did not appear to be a solution for improving tape-subsystem performance, because electromechanical limitations make speeds above 250 ips impractical. The alternative (putting more data on the same amount of tape by increasing flux density) seemed more practical. However, increased density called for improved methods for detecting and correcting errors in the data.

by Mike Newton

Non-return to zero (NRZI) recording, the earliest method, writes 800 bits of information per inch of tape. Magnetically, NRZI relies on a flux change in the oxide coating of the tape to indicate a '1' bit of information, while the absence of a flux change signifies a '0'. Because NRZI requires one flux change for one bit of information, the format provides 100% recording efficiency. Unfortunately, mechanical skew considerations limit NRZI density to the 800 bpi range, and the format cannot correct errors.

Phase encoding (PE), which uses a self-clocking approach, was next developed to overcome the deficiencies of NRZI. Like NRZI, PE records nine tracks on the tape. However, it records the '1' and '0' bits via a flux change — the difference between the two bits depends on direction of flux change. PE suffers from the drawback of needing at least one flux change per bit. Two like bits in succession require a second flux change at the boundary between the cell bits. This flux allows write current to return to a state from which it can write a flux change in the same direction as flux change of the preceding bit of information. Thus, PE can record as many as two flux changes per bit of information that give it a recording efficiency of 50%.

At least one flux change occurs per bit cell in PE. The technique benefits from the fact that each of the nine tracks can have its own clocked detection circuit. This circuit will have a variable-frequency clock running in a phase-locked loop with data on the track. With a clocking circuit monitoring each track, added hardware can sense flux

Mike Newton is from Storage Technology Corp.

Figure 1: Flux change patterns shows that NRZI recording uses a flux change for a logic 1 and no flux change for a 0; PE recording uses a flux change for 1s and 0s; GCR, like PE, uses a flux change for the binary numbers, the data is coded before recording.
OEM terminals for the future...TODAY
The industry standard, smart DM terminals from Beehive

A terminal whose parameters can change with your requirements!

Now available with attractive discounts

Call for applications assistance and delivery
TOLL FREE USA (800) 453-9454

BEEHIVE INTERNATIONAL
“A proven competitive manufacturer of smart terminals”

Circle 26 on Reader Inquiry Card
change amplitude and position within each bit cell. Detection of either of these two conditions occurring outside normal parameters indicates erroneous data within a specific track. Byte-by-byte parity checking can further pinpoint the incorrect bit or bits within that track and correct errors on the fly. However, in any given data record, only single-track error correction is possible via these safeguards.

Since the independent clock of each of the nine tracks virtually frees PE from skewing problems experienced with NRZI, it allows PE recording at 1600-bpi density. It is possible to use PE at higher densities, but the increased frequency of flux changes begins to cause an unacceptable signal-to-noise ratio. Also, dual-track error correction — not provided for by PE — becomes important at higher densities.

what is GCR?

Very simply, GCR is a recording format that takes advantage of the efficiency of NRZI while implementing the clocking procedures of PE. Aided by a sophisticated approach to error correction, GCR has resulted in a 6250-bpi recording density, plus a dual-track error detection and correction capability. The 6250 density was selected, because 6250 bpi processed at 200 ips equals 1.25 Mbytes/sec., which is a data rate compatible with many of today's high-performance computer channels.

how does it work?

Like its predecessors, GCR records on nine tracks. Basically, it uses the NRZI convention: a flux change represents a '1' bit of information, while the absence of a flux change indicates a '0' bit. However, it requires a modification. Originally, a NRZI recorder utilized no clocking system, and it could write a string of '0' bits, represented by a series of bit cells with no flux change. Incorporating a clocking system into the GCR approach eliminated this capability, since periodic flux transitions are necessary to ensure the synchronization of the clocks on the nine tracks. Essentially, GCR can write no more than two '0' bits consecutively.

This is where the term “group-coded” comes in. Before the GCR system records the information, it collects the data in an eight-byte buffer. The tape controller adds seven data bytes and an eighth byte for error checking and correcting information. This function produces an eight-byte data group. Although the information comes in broadband (byte-serial) from the CPU, it is coded bit-serially in subgroups of four bytes.

For clarity, let’s number the bits in each byte, #1 through #9. The translator receives data bits four at a time, and converts the four #1 bits into a five-bit code character, the four #2 bits into a five-bit code character, and so on down through the four #9 bits. The resulting nine five-bit characters are then recorded onto tape. Thus, each eight-byte data group is recorded as a ten-byte storage group. For retrieval, the process is reversed. The four-to-five translation scheme was devised to provide a five-bit storage subgroup that, for each four-bit data subgroup, contains no more than two consecutive '0' bits and no more than one '0' bit on either end. This scheme insures that no recorded track will ever contain more than two consecutive bit cells without a flux transition.

error detection and correction

PE error-correction system provides single-track error correction. The more extensive GCR approach utilizes a system of cyclic codes recorded with the data. GCR uses the same hardware as PE — amplitude sensing (noting the fluctuations in flux-change amplitude) and phase error (checking the exactness of the flux location within the bit cell) — to give the system its multiple-bit error-correction ability.

The error-checking and correcting (ECC) byte of information (attached to the data subgroup in the buffer prior to encoding) is generated by a polynomial as described in ANSI spec ×3.54. This polynomial is based on the 56 bits of information that make up the data group. Thus, a direct mathematical relationship exists between construction of the ECC byte and all data from which it is generated. When the data is read back, control hardware reworks the polynomial generation and checks the resulting error-correction byte against the ECC byte originally written. If a discrepancy occurs, it can be used to calculate exact position of the erroneous bit or bits within the data group. Although this technique can correct only single-bit errors, amplitude sensing and phase error checking can correct multiple-bit errors.

<table>
<thead>
<tr>
<th>4-Bit Data Value</th>
<th>5-Bit Recording Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>11001</td>
</tr>
<tr>
<td>0001</td>
<td>11011</td>
</tr>
<tr>
<td>0010</td>
<td>10010</td>
</tr>
<tr>
<td>0011</td>
<td>10011</td>
</tr>
<tr>
<td>0100</td>
<td>11101</td>
</tr>
<tr>
<td>0101</td>
<td>10101</td>
</tr>
<tr>
<td>0110</td>
<td>10110</td>
</tr>
<tr>
<td>0111</td>
<td>10111</td>
</tr>
<tr>
<td>1000</td>
<td>11010</td>
</tr>
<tr>
<td>1001</td>
<td>01001</td>
</tr>
<tr>
<td>1010</td>
<td>01010</td>
</tr>
<tr>
<td>1011</td>
<td>01101</td>
</tr>
<tr>
<td>1100</td>
<td>01110</td>
</tr>
<tr>
<td>1101</td>
<td>01111</td>
</tr>
<tr>
<td>1110</td>
<td>01110</td>
</tr>
<tr>
<td>1111</td>
<td>01111</td>
</tr>
</tbody>
</table>

Figure 3: Group coding starts with the data entering the controller from the CPU in byte-serial order. The data bytes are stacked in the controller buffer. An error-correcting code (ECC) byte is generated by, and added to, every 7 data bytes to make an 8-byte data group. The translator converts the data into storage code. This process is byte-serial in which each 4-bit data subgroup is assigned a 5-bit storage code. See Figure 4 for a more detailed explanation.
You may think it's a simple task to build your own laser scanner. After all, the technology is direct and the components are readily available. But, when you consider system performance versus cost, you'll come to realize that people... people with scanner sense are necessary for success.

We at Tropel, who have manufactured scanning systems for every conceivable application from non-impact printing to COM, command a capability and expertise that insures you a high performance system at a cost lower than you can do yourself.

For more information and scanner sense, contact: Tropel Division, Coherent, Inc., 1000 Fairport Park, Fairport, N.Y. 14450, 716 377-3200.
Two additional error check characters, incorporated into each storage record, supplement the GCR error detection and correction systems. A polynomial, defined by ANSI specs, generates the AuxCRC (auxiliary cyclic redundancy character). A different polynomial, based on all the data, plus the pad bytes (inserted after the residual customer data bytes to fill out the last storage group) and the AuxCRC itself generates. The AuxCRC and the CRC are generated in a manner similar to the ECC, and provide a final check to insure the integrity of the data after it is read. These characters do not locate or correct errors, but simply indicate that an error or errors exist. Whenever that happens, the computer is automatically alerted to switch to retry procedures.

Figure 5: GCR group consists of preamble (A), resync burst (B), end mark (C), postamble (D), storage groups (E), and residual and GCR groups. (F).
resynchronization

Amplitude sensing, used with GCR to allow multiple-bit, double-track error correction, works the same way with GCR as it does with PE recording. When an erroneous bit is sensed, the dead-track register causes faulty track shut down. This action could create a real problem in GCR, since long data blocks are desirable to optimize the advantages of GCR’s increased density and to avoid devoting too much tape space to interblock gaps. It is obviously unsatisfactory for one or perhaps two tracks to shut down for the duration of a record of that length. Consequently, the GCR format provides an opportunity to reset the dead-track register. It also resynchronizes the read detection circuits during recording by writing a resync burst in all tracks after every 158 data groups, provided that at least one more data group remains to be written. The resync burst consists of a Mark 1 subgroup, ten ‘1’-bit bytes, and a Mark 2 subgroup. The burst is unique and automatically triggers resynchronization of the nine read detection circuits. Because error probability relates directly to record length, and since resynchronization occurs after every 1,106 data bytes, the inclusion of this precaution reduces the probability of an uncorrectable error in an 8000-byte data block by a factor of almost seven.

the GCR data block

So far, we’ve discussed data groups, AuxCRCs, CRCs and resync bursts. Next we will discuss the other components that make up a GCR data block and their assembly on tape.

The Preamble. Just as PE does, the GCR record begins with a block of information designed to alert the amplitude sensors of the beginning of a block, and to synchronize the read-detection clock for each tape track. The preamble consists of a term subgroup and a secondary subgroup. These subgroups announce the beginning of a data block, followed by 14 subgroups made up entirely of ‘1’ bits which allow the read-detection circuits to synchronize. A Mark 1 subgroup ends the preamble.

Storage Groups. Groups of coded data are then written on the tape. Each group consists of 10 bytes. When decoded, the 10 storage bytes are reconverted back into seven bytes of data and the ECC byte.

Resync Burst. After each 158 storage groups (data), a written resynch burst resets the dead-tracking circuits and brings the read-detection circuits back into sync.

End Mark. When the system has finished writing all the storage groups (data), it writes End Mark on all tracks.

Residual Group. Each group contains (prior to coding) eight bytes of information (7 data + ECC). Therefore, if after the system has coded and written all data groups, fewer than seven bytes of customer data remain, they are written into the residual group. The system then fills the group up with pad bytes of zeros, plus an AuxCRC byte and an ECC byte.

CRC Data Group. Next, the system writes a CRC group containing the CRC bytes and the residual count byte. The count byte describes the number of actual data bytes vs. pad bytes in the preceding residual group. Five or 6 CRC bytes (all identical) plus an ECC byte make up the CRC group prior to conversion by coding into a 10-byte storage group.

The Postamble. A mirror image of the preamble, the postamble which finishes the record contains a Mark 2 subgroup (the reverse of a Mark 1), 14 subgroups made up entirely of ‘1’ bits, a secondary character and a term character.

We’ve seen how GCR provides nearly error-free storage of information at low cost. Keep these fundamentals in mind when selecting tape storage subsystems.
DEC Products Directory

current listing includes models, specs, and prices

This directory of products from Digital Equipment Corporation lists products that include: microcomputers, minicomputers, super minicomputers, mainframes and peripherals. Peripherals include storage peripherals such as disks and tape storage. It also includes terminals, printers, and card readers.

The prices listed are only representative and may not represent the highest or lowest prices available. In general, prices for processors tend to represent smallest configurations with minimum memory. Where a system price only is available, this is noted with "(sys)." For peripherals, generally the controller is not included in the price. These prices represent typical United States prices and may vary in other countries. Unless otherwise noted, all prices are representative single-unit prices.

Next month's issue will complement this issue by providing a computer compatible directory. This month's DEC directory and next month's computer compatible directory are the first of their kind. Make sure to save them, they will be valuable for future reference in the upcoming year.

Processors

microcomputers


AED'S INCREDIBLE GRAPHICS MACHINE. STILL THE PERFORMANCE LEADER FOR CAD/CAM APPLICATIONS.

Since its introduction, the AED512 has gained a reputation as 'The Incredible Graphics Machine'. A nickname it continues to merit. This 256K byte desktop terminal has proved more than equal to the full challenge of CAD/CAM applications: printed circuits, integrated circuits, schematics, mechanical design, architectural design, stress analysis, finite analysis and more. Why? Because the AED512 is features ahead of the competition.

The capability of the AED512 includes full-color graphics and imaging; parallel and serial data transfer; 8 video memory planes (256 simultaneous colors); contiguous (1-16) integer zoom; hardware pan and scroll; 8 special function keys; 8 blink colors and AED's unique Superoam™ feature that allows you to trade color for additional drawing size.

The lightweight, compact terminal is easily attached to your computer and is available with or without the color monitor. Software command transparency for Tektronix Models 4010 thru 4015, and compatibility with Compeda's 'Dragon' software is, of course, provided.

Contact our marketing department for a descriptive color brochure on the AED512 system today. They'll also put you in touch with your nearest AED sales office or representative in your area.

Advanced Electronics Design
440 Potrero Avenue
Sunnyvale, CA 94086
Phone 408-733-3555
Telex 357-496

Circle 30 on Reader Inquiry Card
**minicomputers**


**PDP-11/34. Midrange minicomputer.** Wordlength — 16 bits. Maximum memory 256 KB. Uses parity MOS memory. Uses UNIBUS. 2 KB cache memory available as option. Floating-point processor available as option. $12,800.


**PDP-8/A Low- to midrange minicomputer** with traditional architecture. Wordlength — 12 bits. Maximum memory 128 K words. Uses MOS or core memory. Uses OMNIBUS. Floating-point processor available as option. $4,500.

**super-minicomputers**


**VAX-11/780. Top-of-the-line superminicomputer.** Wordlength — 32 bits. Maximum memory 8 MB (except for multiport configurations where an additional 4 MB can be used). Can employ UNIBUS and MASSBUS. Floating-point processor is available as option. $128,000.

**mainframes**

**DECsystem-1090 Mainframe.** Wordlength — 36 bits. Maximum memory 18 MB. Uses core memory. 2-Kword cache memory standard. $639,800.

**DECsystem-1091 Mainframe.** Wordlength — 36 bits. Maximum memory 13.5 MB. Uses MOS memory. 2 K word cache memory standard. $476,000.


**DECsystem-2040 Mainframe.** Wordlength — 36 bits. Maximum memory 9 MB. Uses MOS memory. $357,100.

**DECSYSTEM-2060 Mainframe.** Wordlength — 36 bits. Maximum memory 9 MB. Uses MOS memory. 2-Kword cache memory standard. $431,000.

**Storage Peripherals**

**disks**


Pre-Register for the First National Exposition Dedicated Exclusively to the Expanding World of Compatible Computer Products

FILL OUT THE REGISTRATION FORM ON THE REVERSE SIDE AND MAIL THIS PAGE IN A COMPANY ENVELOPE TO

Save time and the $5 entrance fee.

REGISTRAR
COMPAT.'81
Digital Design
1901 S. Bascom Avenue
Suite 1005
Campbell, CA 95008
THE FIRST NATIONAL EXPOSITION
DEDICATED EXCLUSIVELY TO
THE EXPANDING WORLD OF
COMPATIBLE COMPUTER PRODUCTS

SEPTEMBER 16 & 17, 1981 SAN FRANCISCAN HOTEL (Across the street from WESCON) SAN FRANCISCO, CA

Pre-register now. Advance registration by mail is more convenient for you and saves time and money. Avoid long waiting lines. Since seminars are limited in size, they are available on a first-come, first-served basis. Badge will be waiting for you at the registration desk. MORE . . . with advance registration your entrance to the exhibits only will be FREE!

Please read carefully. Fill in form completely. Use envelope if enclosing remittances. Deadline for returning pre-registration August 1, 1981. Later registration must be done at Registration Desk at the Exposition.

I. For which of the CPU's listed below do you plan to purchase computer compatible products and/or services?

- Data General
- Digital Equipment Corp.
- Hewlett-Packard
- IBM
- Intel
- Motorola
- Perkin Elmer
- Other

II. For the CPU's you have checked, what types of plug compatible products do you specify or purchase?

A. Computers/Controllers
- Programmable Controllers
- Single Board Computers/Chips
- Alphanumeric Display Terminals
- Graphic Terminals

B. Data Terminals
- Programmable/Intelligent Terminals

C. Memory
- Add-in and Add-on Memory Systems
- Bubble Memory Systems
- Semiconductor Memory (RAM/ROM, etc.)

D. Mass Storage/Drives
- Disk Pack/Removable Cartridge
- Fixed Disk/Large
- Floppy Disk
- Magnetic Tape
- Tape Cassette/Cartridge
- Winchester Drives
- CRT Display Copiers/Printers
- Line Printers
- Plotters
- Serial Printers
- Teleprinters
- COM Equipment
- Digitizer/Light Pens
- Facsimile Equipment
- Magnetic Card Equipment
- Optical Input Units
- Voice Response Equipment
- Other, please explain

G. Controllers/Interfaces
- Communications Interfaces/Adapters
- Data Acquisition and Control Modules/Subsystems
- Intelligent Interface Modules/Subsystems
- Peripheral Controllers/Formatters

H. Communications
- Communications Multiplexers
- Concentrators/Message Switching Systems
- Data Transmission Equipment
- Modems/Data Links

J. Software/Firmware
- Applications
- Communications
- Development Aids for Microcomputers/Minis
- Languages
- Operating Systems

PLEASE PRINT IN BLOCK LETTERS

NAME

TITLE

COMPANY NAME

ADDRESS

CITY STATE ZIP

AREA CODE TELEPHONE NUMBER

Signature Date

I would like to attend:

ADVANCE REGISTRATION AT DOOR

1) Exhibits only □ Free □ $5 per day
2) Seminars □ $25.00 □ $35.00

- SEMINAR 1-1-CSF Controllers
- SEMINAR 1-2-CSF Data Storage Peripherals
- SEMINAR 1-3-CSF Terminals and Printers
- SEMINAR 1-4-CSF Software

Check or money orders are enclosed
P.O. enclosed
Please invoice

Seminars are subject to changes, substitutions or cancellations without prior notice.

Return completed form to:

REGISTRAR
COMPAT '81
Digital Design
1901 S. Bascom Ave., Suite 1005
Campbell, CA 95008
before August 1, 1981.

Registration will be refunded if cancellation is received prior to August 15, 1981.

Minors cannot be accommodated.


**Terminals and Printers**

**terminals**


LA34-VA Receive-only hardcopy terminal. Uses dot-matrix (9 x 7) for alphanumeric characters. Character set: 96 ASCII. Also has graphics-output printing from raster-screen video terminal. Maximum printing speed: 300 baud. Paper type: roll feed. $1,650.

LA34-WA Receive-only hardcopy terminal. Uses dot-matrix (9 x 7) for alphanumeric characters. Character set: 96 ASCII. Also has graphics-output printing from raster-screen video terminal. Maximum printing speed: 300 baud. OEM version sold without paper option. $1,700.


VT100 Video terminal. Character set: 96 ASCII. Maximum communication rate: 19,200 baud. User-selectable functions such as reverse video, choice of 80- and 132-column lines, jump or smooth bidirectional scrolling, double-width or -size characters, and split screen scrolling. Video in and video out. Movable keyboard. $2,150.

VT100T Video terminal with emission shielding. Character set: 96 ASCII. Maximum communication rate: 19,200 baud. User-selectable functions such as reverse video, choice of 80- and 132-column lines, jump or smooth bidirectional scrolling, double-width or -size characters, and split screen scrolling. Video in and video out. Movable keyboard. $7,100.

VT103 Video terminal with provisions for addition of LSI-11/2 or LSI-11/23. Character set: 96 ASCII. Maximum communication rate: 19,200 baud. User-selectable functions such as reverse video, choice of 80- and 132-column lines, jump or smooth bidirectional scrolling, double-width or -size characters, and split screen scrolling.
TI leadership.
In 64K DRAM technology.
In Memory Systems.

Whatever bus you're using — VAX†, PDP-11†, LSI-11†, or even Multibus — TI can supply add-in memory system boards with dynamic RAMs from our own high-performance 64K series.

When you specify TI's high-density, low-power boards, you save rack space. So you have more room for I/O — or whatever else you need. And, the low-power consumption of TI 64K DRAMs, compared to the old-fashioned 16Ks, cuts temperature levels and increases reliability. The reduction in memory package count by as much as four boosts reliability even more.

System reliability will be higher, too. Thanks to error correction/detection available on many TI memory boards. Using our own bipolar EDAC chip helps cut component count and system temperature, as well as improving basic system reliability. The EDAC chip replaces about a quarter of a board of TTL circuitry.

All TI boards are 100% tested. 100% burned-in. All in TI's modern, high-capacity Houston facility. Delivery normally ranges from stock to four weeks.

Low cost
Representative pricing* for TI memory boards is as follows: $1600 for TMM10000-04 (192KB); $3800 for TMM20000-02 (256KB); $9000 for TMM30000-01 (1MB); $1845 for TMM40000-07 (64KB).

Custom capability
If you need custom memory systems in production quantities, be sure and talk to TI. We'll custom design boards for specific applications with the same meticulous attention to cost/performance effectiveness that our standard boards offer.

So for the latest DRAM technology, highest packing densities, lowest power consumptions, all at competitive prices, remember memory systems from Texas Instruments.

To find out more about TI boards call your local TI field sales office or authorized distributor. For details, call (713) 778-6549, or write to Texas Instruments Incorporated, Integrated Memory Systems, P.O. Box 1443, M/S 6404, Houston, Texas 77001.

TI MEMORY BOARDS — CURRENT AVAILABILITY

<table>
<thead>
<tr>
<th>System</th>
<th>TI Series</th>
<th>64K</th>
<th>128K</th>
<th>192K</th>
<th>256K</th>
<th>512K</th>
<th>768K</th>
<th>1M</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSI-11†</td>
<td>TMM10000†</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>PDP-11†</td>
<td>TMM20000§</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>TMM30000</td>
<td>X</td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>VAX†</td>
<td>TMM40000</td>
<td>X</td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>MULTIBUS</td>
<td>TMM40010†</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

*Price for production quantities
†Trademarks
‡Trademarks
§U.S. Single-unit price, subject to change without notice.

TEXAS INSTRUMENTS
INCORPORATED

Circle 3 on Reader Inquiry Card

© 1981 Texas Instruments Incorporated
Video in and video out. Movable keyboard.

$3,200.

**VT105 Scientific/laboratory video terminal.** Character set: 96 ASCII. Limited graphics capabilities (charts and histograms). Maximum communication rate: 19,200 baud. User-selectable functions such as reverse video, choice of 80- and 132-column lines, jump or smooth bidirectional scrolling, double-width or -size characters, and split screen scrolling. Video in and video out. Movable keyboard. $3,100.

**VT173 Video terminal for typesetting computer systems.** Uses LSI-11/2. Special typesetting keyboard (105 keys in reporter version; 123 keys in classified-advertisement version). Has 32-Kb internal memory. Maximum communication rate: 19,200 baud. User-selectable functions such as multiple text creation and editing areas. Movable keyboard. $5,195.

**VSV11 Engineering video terminal for PDP-11 and VAX-11 computers.** Raster-scan unit available with either monochrome or full color presentation. Character set: 96 ASCII. Has joystick for cursor positioning. Image memory to $12 \times 526 \times 4$ noninterlaced. Image range: 16 colors or 16 shades of gray. $6,480.

**VSV11 Engineering video terminal for LSI-11 and PDP-11/03, PDP-11/23.** Raster-scan unit available with either monochrome or full color presentation. Character set: 96 ASCII. Has joystick for cursor positioning. Image memory to $12 \times 526 \times 4$ noninterlaced. Image range: 16 colors or 16 shades of gray. $5,730.

**VK100 Keyboard subsystem.** µP-based unit for connection to video display (monitor). Has graphics, alphanumericics. Can be used with color or monochrome monitors. Has 8 colors or 8 levels of gray in picture presentations. Has graphics output port for use with LA34-V terminal. Has ROM-based BASIC. Has interface for use with (user supplied) graphics tablet. $4,200.

---

**High-Speed MAXiram Storage System**

Offers superior performance, throughput and reliability!

Compatible with:
- D.E.C.
- Data General
- Westinghouse

The non-rotating MaxiRam is a solid-state disc replacement storage system that operates at the speed of main memory. It is ideal for the following:
- ... if your processor is disc I/O bound.
- ... if your CPU spends too much time in the 'wait' state.
- ... if your present disc gives you reliability headaches.

Write or call to find out how your memory performance and reliability can be dramatically improved. Units available in both core and semiconductor.

Imperial Technology, Inc.
831 S. Douglas Street • El Segundo, California 90245 • Telephone: (213) 679-9501

Circle 63 on Reader Inquiry Card
Don’t Get Lost in the Maze.

BRAEGEN can help you find your way. We offer you:

**DEC COMPATIBILITY AND MORE...**

Now you have a choice of six fully software/hardware compatible disk subsystems that provide higher storage capacities (up to 256 Megabytes per drive), higher throughput (1.209 Megabytes/sec transfer rate), and several features not available on some other systems ie: automatic disk format; automatic bootstrap; data checksum, automatic self-test, and more.

**OUR OWN NATIONWIDE SERVICE...**

Now you can count on fast, local service by more than 275 factory-trained technicians in more than 55 service centers across the country (more locations are planned). Each center is staffed by Braegen personnel who are thoroughly familiar with your peripheral.

**A QUALITY PRODUCT AT A DEFINITE PRICE ADVANTAGE...**

Compare our product line to that of DEC. You’ll soon discover that feature-for-feature and value-for-value, BRAEGEN is your best cost/performance choice. And we come through for you with FAST DELIVERY and a unique 1 year warranty.

**A UNIQUE TRADE-IN POLICY...**

We offer you an alternative to expensive growth. Our unique trade-in policy allows you to upgrade your system at a fraction of the usual cost. We’ll give you fair market value for your DEC disk drive as a credit toward reducing the overall cost of your system expansion.

**LET BRAEGEN BE YOUR SINGLE SOURCE FOR ALL DEC-COMPATIBLE PERIPHERALS...**

Only BRAEGEN can offer you a full line of Disk Subsystems, Magnetic Tape Subsystems, Add-in RAM Memory boards, VT-100 Emulating Display Terminals, and Line Printers to help you get the most out of your DEC system. And all of our products come complete with pre-installation site survey, installation, training, and documentation.

Let us help you through the maze...and show you true cost/performance in Disk Storage. Call your local BRAEGEN Sales Office listed below.
VISACOM/23

GRAPHIC/IMAGE SYSTEM.
SUPER CAPABILITIES,
SUPER FAST, SUPER PRICE.

DeAnza's VISACOM/23 now offers you features and capabilities previously only found in large-scale systems. Features like proven and superior image and graphic display software, advanced computing capabilities and proven operating systems software. All at a very reasonable price.

The VISACOM/23 and the DeAnza Library of Image Processing Software (LIPS) allows you to perform work you only thought possible on the large, expensive systems.

Graphic and display efforts like convolutions, rotations, classification, amplifications, addition, subtraction, image and graphic zoom and scroll as well as much more.

And, the VISACOM/23 incorporates the powerful LSI-11/23 computer so you perform graphic and image processing more easily and much faster.

It allows you to do more work in less time. VISACOM/23 has a full 512K byte memory for dedicated computer operation or image display as well as 128K bytes of dedicated memory outside of the image memory, four independent graphic overlay channels, alphanumeric character generators, color and monochrome transformation units and cursor overlays.

If your graphic and imaging application calls for a system that provides quality, flexibility and added capabilities all in an economical package, find out more about the VISACOM/23 today.

Call or write:

DeAnza Systems Incorporated

Corporate Headquarters: 118 Charcot Avenue • San Jose, California 95131 • (408) 263-7155 • TWX (810) 339-7655

Regional Offices: 100 First Avenue N.E., Suite 114F, Cedar Rapids, IA 52401, (319) 364-1366, TWX (615) 629-1366 • 3918 Prosperity Avenue, Suite 204, Fairfax, VA 22031, (703) 686-0600, TWX (710) 633-0366 • 500K Middle Country Road, Middle Island, NY 11953, (516) 736-3440 • 4401 Atlantic Avenue, #28, Long Beach, CA 90807, (213) 422-4445.

GIVE YOURSELF A BETTER IMAGE

Circle 71 on Reader Inquiry Card
**printers**


**LP11-BA Band printer.** Output speed: 285 or 204 lines per minute. Character set: 64 or 96. Paper feed: pin feed. Uses horizontal-font printing. For computers with UNIBUS. $8,950.


**LP11-V Impact line printer.** Output speed: 300 lines per minute. Character set: 64. Paper feed: pin feed. For LSI-11 bus PDP-11s. $16,400.


**LP100-B Impact line printer.** Output speed: 1200 lpm. Character set: 64 or 96. Paper feed: pin feed. For DECSYSTEM-10 computer systems. $63,100.


---

**Add SMDs To Your PDPs**

Get The Disk Storage You Need...

- Single board controllers featuring Xylogic's exclusive PERIPHERAL PROCESSOR technology
- Complete subsystems with your choice of drives from all major vendors
- 100% DEC emulation
- Mixed drive capacities and up to eight drives controlled by a single Peripheral Processor
- Nationwide CDC service available on Xylogics/CDC subsystems
- Aggressive OEM discounts
- Significant savings compared to DEC disk subsystem prices

... When You Need It

For PDQ response to your SMD requirements call Xylogics today. In Mass call (617) 272-8140.

U.S. Headquarters: 42 Third Avenue, Burlington, MA 01803 Tel: (617) 272-8140 (TWX 710-332-0252)
European Headquarters: 46-48 High Street, Slough, Berks SL1 1ES U.K. Tel: (0753) 78921, Telex 847978

Circle 33 on Reader Inquiry Card
**LP-100-F Impact line printer.** Output speed: 900 lpm. Character set: 64. Paper feed: pin feed. For DECSYSTEM-20 computer systems. **$44,300.**

**LP200-B Band printer.** Choice of font styles and character sets (64 or 96). Paper feed: pin feed. For DECSYSTEM-20 computer systems. **$54,600.**


**LQP Letter-quality printer for word processors.** Daisy-wheel impact printing. Paper feed: pin feed. Used with WS 78 and WP200 systems. **$4,495.**

---

**Card Readers**

**CR11 Punched card reader.** Card type: 80-column. Reading speed: 300 cards/min. For PDP-11. **$8,250.**

**CD20-A Punched card reader.** Card type: 80-column. Reading speed: 300 cards/min. For DECSYSTEM-20 computer systems. **$7,920.**

**CD20-C Punched card reader.** Card type: 80-column. Reading speed: 1200 cards/min. For DECSYSTEM-20 computer systems. **$27,960.**

---

Moving?
1. For FASTEST service attach old mailing label in space below.
2. Print your NEW business address here.
3. Mail to: Circulation Manager
   Digital Design
   1050 Commonwealth Ave.
   Boston, MA 02215

---

Clary Corporation
320 W. Clary Ave. San Gabriel, CA 91776 (213) 287-6111
TWX 910 589-3369

Circle 35 on Reader Inquiry Card
COMMUNICATIONS PRODUCTS

ABLE DH/DM* (16-LINE LINE PROCESS DMI & DMI INSTALLS: IN: UNIVERSAL...her SPC slot.
DATA RATES: 14 standard rates plus 19.2K baud and Impedance.
ADVANTAGES: Word transfer (in lieu of byte DMM) permits the use of operating MOD-UP (with modem control). IMPLEMENTATION ADVANTAGES: Off-board pencil switches are used for selection backplane and full system software compatibility with all DV11 performance features.

ABLE DZ/16 (16-SLOT DZ11-E REPLACEMENT)
INSTALLS: IN: All PDP-11's, in less than one half the space of SPC slot. (Unibus, PDP-11's, PDP-11/40, -11/45, etc.) put-up of up to 30,000 characters/2 (19.2K baud full duplex). ONBOARD SELECTABLE RATES and BINARY ADDRESS: Word transfers (in lieu of byte DMA) permit user to operate within one half the DV11 bandwidth for data transfers. OPERATING ADVANTAGES: User may mix sync and async in combinations of 4 or 8 lines with modem control and full system software compatibility with all DV11 performance features.

MEMORY PRODUCTS

SCAT/45* (ADD-IN FASTBUS MEMORY)
INSTALLS: IN: PDP-11/40, -11/50 and -11/55. EXPANDS IN: 22K word per board. One-half of the available Fastbus slot will accept full 124K word complement. ADDRESSES ON: Any 4096 word boundary across entire 124K word range. User has full memory control at 330 nsec cycle-time memory instead of 22K word limitation imposed by the computer manufacturer.

CACHE/45* (CACHE/45 MEMORY)
INSTALLS: IN: PDP-11/45, -11/50 and -11/55. CAPACITY: 2048 byte (1K word). ENHANCEMENT FACTOR: Run time reductions to 90% (100% speed improvement) are achievable. CACHE PARITY: Automatically goes off-line in event of any data error. RANGE SELECTION: User may optimize hit ratio by upper/lower limit switch settings. SPECIAL FEATURE: Cache/45 can be enabled via software or console switches.

CACHE/484* (4K WORD CACHE MEMORY)

CACHE/440* (4K WORD CACHE MEMORY)

QNIVERTER* (Q-BUS TO BUS CONVERTER)
INSTALLS: IN: LSI-11, LSI-11/23, PDP-11/03 and PDP-11/23 via quad-wide card. APPLICATIONS: Allows Unibus-compatible controllers and memories to be used with LI computer systems, or LSI-based peripherals to be used with PDP-11 computer systems. FEATURES: Supports features of LSI-11/23 including the full 128K address capability.

REBUS* (BUS REPEATER - DR11 REPLACEMENT)
INSTALLS: IN: All PDP-11's, without using any additional backplane space. MECHANICAL: One dual-wide card plugs into the same pair of connectors as the Unibus extension cable which is then plugged into the RBUS connectors. COMPATIBILITY: Allows for 18 additional bus loads and 50 foot extension on Unibus. BUS CYCLE TIME: Unaffected for devices on CPU side of RBUS - increased by 250 nsec max. for devices on outboard side.

DUAL I/O* (GENERAL INTERFACE-DR11-C REPLACEMENT)
INSTALLS: IN: All PDP-11's in any PDP slot via quad-wide card. APPLICATION: DUAL I/O is equivalent to two (2) DR11-C's and provides the logic for program-controlled parallel transfer of 16-bit data between two (2) external user devices and a Unibus system. OPERATING ADVANTAGE: Provides the hardware equivalent of a dual DR11-C in one-half the space and one-half the bus loading of DR11-C's.

INTERLINK/UNI
(DR11-B AND D DA11-B REPLACEMENT)
INSTALLS: IN: All PDP-11's in any PDP slot via hex-wide card. APPLICATION: Provides full DR11-B (DMA INTERFACE) and one side of DR11-B (UNIBUS/LINK) capability on a single card. OPERATING ADVANTAGE: Requires only one hex-wide card in each computer to effect link vs. full four-slot systems. SELECT-image capability. BUS INTERFACE: Supports the following signals: Full DR11-B replacement or when expanded to DA11-B equivalency.

BUSLINK/UNI, LSI OR U TO Q (CPU TO CPU LINE: UNIBUS TO UNIBUS, UNIBUS TO Q-BUS OR Q-BUS TO Q-BUS)
INSTALLS: IN: All PDP-11's and/or LSI-11's via pairs of hex-wide, hex-wide, and/or D or Q-BUS cards and cables. APPLICATION: Provides full DA11-B (Unibus or Q-bus link) compatibility on single cards. BUSLINK operates at DA11-B transfer rates over distances of up to 50 feet. OPERATING ADVANTAGE: Requires only one card per CPU to effect link at minimal bus loading vs. full system unit per computer.

ABLE cards give you the best way to make your present PDP-11 run better than ever and avoid upgrading to a more expensive model. We give you time to plan ahead and to control your cash flow with the most sophisticated line on the market today. Our cards are priced competitively. They install in minutes. They provide immediate results. And they always out-perform the competition. They should. We are the only computer people in the computer-system-enhancement business. Write for details.

ABLE the computer experts
ABLE COMPUTER, 1761 Langley Avenue, Irvine, California 92714. (714) 979-7098. TWX 910-555-1279. ACT VRN
ABLE COMPANY EUROPE, 74/76 Northbrook Street, Newbury, Berkshire, England ROX 1AE. (0365) 32123. TELEX 941757 HJULMH.

Circle 36 on Reader Inquiry Card.
DEC Compatible Products Continue Upward Growth
also, how not to get caught in your own trap

The early days of DEC compatibility saw financially shaky companies often offering products that later proved to be unreliable. From that unpromising beginning has emerged a generally healthy, dynamic industry, most of whose offerings begin with unqualified reliability. But there are still some pitfalls in this comparatively new supply source. This article will hopefully guide you safely past those consumer traps. Best tip: know your supplier!

by Paul Snigier

DEC compatible products continue their inroads, taking more market share, and improving from previous days of poor boards and poorer service. DEC compatibility has gained respectability. Unlike the earlier days of DEC compatibility, which was set off by the introduction of the PDP-11, respectability has come to the field. Many of the manufacturers of DEC compatible products are relatively long-term survivors in this field. They have survived the shakeout and lean years, and have grown into well-staffed, well-fielded outfits that can design, manufacture and support their DEC compatible products for years to come. Others, frequently cottage shop outfits started by college students and others, lacked the staying power or motivation to adequately service their products. More than one product was made with substandard parts, assembled in a cellar, with solder bridges inserted backwards. These products were foisted off onto unsuspecting OEMs. If the boards or products didn't work — which all too often became frequent enough to create monumental design and production headaches — then the only thing that was more aggravating was the promised field service from the DEC compatible manufacturer which wasn't all that had been promised. Times have changed.

Large semiconductor makers, such as National Semiconductor, which provided some material used in this article, and others like Mostek and TI, are actively pursuing this market. Obviously, they have a decided edge over other add-in/add-on memory makers when volume is the driving force. We wish to thank System Industries, Imperial Technology, and other manufacturers for providing us with technical material and answering our questions.

vendor selection

If the product you're specifying is something you can service and is simple enough, or commonly-used and easily serviceable by other field techs, then vendor selection may assume less significance than if the products are more complex or less well-known.

In investigating, insist on answers; your job and your firm are on the line — not theirs. Check the reputation of the firms you investigate by calling several. But, with myriad firms and new startups dotting this field, it's impossible to evaluate reputations, much less keep track of them. While compiling our August Computer Compatible (COMPAT) Directory issue — which will be distributed at our COMPAT show next month — we discovered firms not listed anywhere else by any other source of information. To check on them, you might start by using next month's directory issue. Ask colleagues within your department and company. While visiting shows, make contacts and ask them. Phone contacts for recommendations and what bad or good experiences they've had. If they work in a non-competing field, they may be glad to talk, hoping you'll reciprocate sometime. Find out what your competitors prefer — and what firms they avoid.

Get customer references from the firm. Contact them and determine their level of sophistication and breadth of experience. Each contact may provide you with two or three additional leads, giving you a good idea of how that firm conducts its business from the customer's viewpoint. This may not be what the firm tells you.

You have the right to ask for proof that the firm has staying power and commitment to that product line. Obtain a written financial report. Get bank references. Interpret growth patterns. That is, interpret them in terms of what's going on with other firms in that same sector of the DEC compatible market. If many have gone belly-up in the past three years that marketed this product and committed their main marketing effort to this product line, then it's very likely that this firm will more likely than not also end up on credit-hold with suppliers and be unable to correct the problems. Or, a firm may grow too rapidly, with sales skyrocketing, and wind up in receivership with cash flow problems. Slowed deliveries (and the related worsening field support) will hurt your firm's reputation.

You should check training; your people must be trained on the product you'll buy. Is it at the end user's site? At yours? Or at the maker's site? It's a good idea to have some independence in having your own service capability in case something happens to your supplier's field service. It's also a plus in selling your customers, and makes a good advertising

Paul Snigier is the Editor of Digital Design magazine.
and sales pitch. See if you can negotiate manufacturing rights to the product that you purchase. It’s just one more safety net in case the manufacturer goes under or decides to get out of this product line, or put it on the back burner.

**documentation: key to quality**

Poor firms provide poor documentation; good firms, usually good to excellent documentation. Insufficient information about, say, a controller, could mean the difference between a disaster and a maintainable product. If the product is unsophisticated, then a basic instruction list, theory of operation and schematics might be satisfactory. Perhaps it leaves something to be desired, but it’s something you and your designers and field techs can live with. Such a documentation is “adequate,” although annoying and tedious to interpret.

For more sophisticated equipment, documentation becomes critical. Check the manuals and documentation to maintain, field repair and even build your own one day. Does the manufacturer provide on-going support for his documentation, providing decent retrofits and upgrades?

Failure to provide adequate documentation at this stage in the development of the DEC compatible marketplace is inexcusable; it is an indication of the lack of concern that this manufacturer feels towards his customers. It may be a sign of things that are waiting in store for you if you deal with him. Poor documentation is rarely a sign of incompetence: it’s usually due to lack of concern or a tight-fisted company that’s overlooking its EEs. When a design project is behind, guess what gets put off until later? Finally, at the end of the design cycle, there is a sudden rush to put together some documentation — anything — just to meet the commitment. Programmers, and to a greater degree, designers, are judged primarily on the code they generate and the circuits they design and package — not mainly on the quality of documentation. Project leaders are usually not judged primarily on the quality of the documentation. And they know it. So, documentation gets the short end of the stick. Make sure you’re not the victim. Demand quality documentation.

Your own documentation to the end user will also be written in part from the documentation you receive. In the case of military systems, a market that is targeted to grow in the eighties, poor documentation can prove your undoing. With more functionally illiterate students coming from public schools and entering the military, and with the exodus of skilled and technically-trained men from the military to industry, the armed forces must train an increasing number of recruits rapidly. Unfortunately, the quality of the recruits, in terms of their reading comprehension, is declining. With increasing classroom size and lack of meaningful punishment, and school discipline problems at epidemic proportions, there is no chance of any real improvement in reading comprehension within the eighties. The alternative, aside from simpler and less sophisticated military systems, is the generation of simpler documentation and training materials from OEMs. Tediuous documentation will only make it harder for you to write decent documentation for military systems. Demand good documentation. If the firm has mediocre documentation, even if you don’t specify that product, let them know how you feel. A few complaints to their president will get some changes.

**DEC-compatible makers cite plusses**

Add-in memory from non-DEC sources offers the following advantages: (1) Products cost thousands of dollars less than non DEC, yet offer many additional features. (2) 97% of the time, you get delivery within, say, 20 days. DEC guarantees delivery within 6-9 months. (3) Products offer extras. An add-in memory may give you an ON/OFF switch that DEC doesn’t. In such a case, on-site reconfiguration/trouble

### Vendor Selection Criteria

<table>
<thead>
<tr>
<th>Vendor Selection Criteria</th>
<th>Vendor And Product Selection Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>Financial stability</td>
<td>critical</td>
</tr>
<tr>
<td>product commitment</td>
<td>important</td>
</tr>
<tr>
<td>field service</td>
<td>moderate</td>
</tr>
<tr>
<td>training</td>
<td>unimportant</td>
</tr>
<tr>
<td>manufacturers' rights</td>
<td></td>
</tr>
<tr>
<td>reputation</td>
<td></td>
</tr>
<tr>
<td>other</td>
<td></td>
</tr>
</tbody>
</table>

### Product Considerations

<table>
<thead>
<tr>
<th>Product Considerations</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>cost</td>
<td></td>
</tr>
<tr>
<td>delivery</td>
<td></td>
</tr>
<tr>
<td>extras</td>
<td></td>
</tr>
<tr>
<td>warranty</td>
<td></td>
</tr>
<tr>
<td>reliability</td>
<td></td>
</tr>
<tr>
<td>installation costs</td>
<td></td>
</tr>
<tr>
<td>field service</td>
<td></td>
</tr>
<tr>
<td>flexibility</td>
<td></td>
</tr>
<tr>
<td>other</td>
<td></td>
</tr>
</tbody>
</table>

### Sources

<table>
<thead>
<tr>
<th>Sources</th>
<th>completed?</th>
<th>date</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEC Directory (this issue)</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>COMPAT Directory (next month)</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>colleagues' experiences</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>customer references</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>examine vendor list</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>trade press articles</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>market reports</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>visits to vendors</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>examine vendors' records</td>
<td>no</td>
<td></td>
</tr>
</tbody>
</table>

Figure 1: Develop an evaluation sheet and use one per product. The above evaluation criteria worksheet is only an example; yours will include more criteria tailored to your specific applications.
YOU ARE CORDially INVITED TO

COMPAT '81

COMPATIBLE COMPUTER PRODUCTS EXPOSITION

SEPTEMBER 16 & 17, 1981 SAN FRANCISCAN HOTEL

COMPAT '81 was conceived to:

- Enhance Computer Capabilities
- Provide Computers with Greater Flexibility
- Assure Availability of Peripherals, Accessories and Software for ALL Branches of the Computer Industry

THE COMPATIBLE COMPUTER EQUIPMENT MANUFACTURERS (CEMs), MEMBERS OF A SPECIALIZED INDUSTRY, WILL SHOW AND TELL ALL ABOUT THEIR PRODUCTS AND SERVICES

LISTEN TO authoritative speakers give you information on how CEMs (Compatible Equipment Manufacturers) help OEMs, systems integrators, turn-key houses and large volume sophisticated end users SOLVE COMPUTER APPLICATION PROBLEMS

ANOTHER EXPOSITION ORGANIZED BY:

The Benwill Conference Group who also bring you the ATE Seminar/Exhibit, PC '81 — the International Printed Circuits Conference and the Electronics Test and Measurement Conference
THE FIRST NATIONAL EXPOSITION
DEDICATED EXCLUSIVELY TO
THE EXPANDING WORLD OF
COMPATIBLE COMPUTER PRODUCTS

EL (Across the street from WESCON)  SAN FRANCISCO, CA

A MARKETING FORUM
for CEMs

his exposition is dedicated to the proposition that the unprecedented growth and expansion in the use of computers for all kinds of applications will continue at an exponential rate. No one company can solve everyone’s applications problems; no one company can supply everyone’s needs for complete systems, add-ons, peripherals and software.

Building around the central processing unit, the OEMs, the systems integrators, the turn-key houses and the sophisticated large volume end users will continue to use compatible computer equipment to devise special systems to solve applications problems with greater versatility and flexibility.

IF YOU ARE a buyer and specifier of plug-in electronics and appropriate software, you have a need to know about currently available products you can design into your systems as well as future trends in the state-of-the-art. THIS EXPOSITION GIVES IT TO YOU.

PRODUCED BY:

Digital Design

copyright by Circuits Manufacturing,
Design Engineering and Electronics Test magazines.
Figure 2: Selecting DEC-Compatible products will involve a number of criteria, shown above, that fall into the design or business category.

(continued from page 55)

shooting is enhanced via an on-line/off-line switch to allow you to easily remove the card from the system without physically extracting it from the memory backplane. Where battery backup is employed, memory retains data while on-line or off-line. (4) More makers now give you a good warranty deal, unlike the past fly-by-night boards made from questionable parts. Sometimes they worked; if not, too bad. Service was a bear. Times have changed; DEC compatibility has gained respectability. (5) Check MTBFs, MTRRs and how the data was obtained. If all components are preconditioned to A+ status, and if, say, over 98% of all boards are entirely free from defects, consider yourself lucky. Few approach this reliability. (6) Consider low installation cost. Lower installation cost means it's easy to install and easier to maintain. (7) Is it backed by a big semi or other giant? If it's an industry leader in the design and testing of systems, fine; but sometimes you'll pay extra for this.

To illustrate the above points, let's use the following cases.

disk storage for large minis

A “Compaq” maker's disk storage can bring out the best in your DEC minicomputers, whether they be VAX-11/780, PDP-11/70 or any of the Unibus machines. When your system can’t afford downtime — for example, during electronic funds transfer — it can securely database on-line, expand performance and allow for myriad configuration options necessary in such time-critical applications as printing, graphics, and transaction processing. It can substantially increase storage capacity with superior price/performance, while reliability insures a low ownership cost. The basic emulation capability would let you configure it as an RPOX or RMOX disk system; you free yourself from the CPU manufacturer's system constraints, and achieve 100% software transparency with existing disk drives.

Manufacturers' system features include the following, or are features you should look for: (1) Field-proven reliability, serviced with many installations, spanning years of field experience. Beware of novices. (2) Individually-tailored service plans insuring low cost of ownership. (3) Provides more storage per spindle than RPOX and RMOX drives. (4) Requires hardware or software changes? Better that it doesn't. (5) Multiple CPU option that allows accessibility to database for up to, say, four different DEC minis. (6) Dual-channel drive capability that permits greater throughput, redundant system configurations. (7) Easy expansion via hardware modularity and software transparency. These aren't the only criteria, by a long shot, and they may not suit your needs, but they're guidelines.

flexibility counts

Is the system built around an emulating controller? It can offer maximum flexibility in database storage systems. As storage needs grow, you then add on drives. Add one controller and a single SBI interface (emulator) to the VAX-11/780, for example, and link up to, say, eight 675-megabyte drives in a daisychain configuration, as one DEC-compatible maker puts it, thus providing up to 4,800 megabytes of on-line storage. This avoids software or hardware changes to the present system. As you configure the system, select from different disk drives. Different firms select different drives, which will vary, because of their in-house reliability. The systems expand flexibility options with configurations. Besides daisychaining drives, you configure them radially. Or, if you need more than one CPU to share the same database, you use the controller's multiple CPU option to increase throughput by interfacing several DEC CPUs — say, VAX 11/780's, PDP-11/34's or PDP-11/70's — in any combination.

reliability improves security

Maximize security and integrity of the database by using multiple CPU and dual-channel drives in environments where downtime is intolerable.

As an example, one manufacturer uses a configuration that transforms a single-CPU/controller system to a dual, redundant configuration consisting of two controllers and up to four drives. Two, three or four CPUs can interface with the two controllers, all sharing a common database. The quadruple connections and complete redundancies assure continuous on-line operation, increased throughput, and maximum system performance, without changing applications software or degrading response time.

Other cases can be investigated, but specifying reliability boils down to a few selection criteria.

What about overall dependability of system hardware? Is the system field-proven in thousands of installations? Do they span a broad range of applications? And do one or more resemble your own? Are these systems ones that have rendered years of reliable trouble-free service to hundreds of customers? Caveat emptor. Investigate.

is system support a mirage

Do they back up the system’s reliability with reliable service and support during factory system integration, at time of installation and afterwards on an ongoing contract basis tailored to your needs? Go to the plant for an on-site visit. Talk to their service people. Are they specially trained, top-notch engineers and managers? Or front men who merely hold your hand until a competent tech is available? Do they work out of a worldwide network of service centers offering total repair capability and fast turnaround?

Continuing requirements of maintaining data storage systems count. Is there fast, effective service? If you're located within a 50-mile radius of a large metropolitan area, do you get a 4-hour response service? Is it 24 hours a day, 7 days/
If Thomas Edison had used a Monochip, he might have been a color copy machine. His lightbulb might have been a laser. And his phonograph might have been a stereo system. Why? Because with Monochip, IC turnaround time could have kept pace with the speed of his imagination and the limitations of his budget.

Monochip is the semi-custom IC. That means its circuit components—the first five layers—are already in place when you start designing. All you do is tell us how to connect them to make the circuit your application requires. Working from your layout, we etch the sixth layer and deliver prototypes in only 6 to 8 weeks for $5,000 or less. Once you’ve approved them, we’ll make production runs of 1,000 to 500,000 parts. It’s that easy. Monochip Design Kits are only $25 to $59 each, and include everything needed to develop your own custom linear, CMOS, NMOS, CML or bipolar IC.

There’s no telling what Edison might have designed if he could have used a Monochip. Now, just imagine how far you can go. Call or write for more information. Interdesign, 1285 Reamwood Avenue, Sunnyvale, CA 94086. (408) 734-8666.

Interdesign is a Ferranti Company.
week? Or do you need a faster, on-site contract? This is appropriate where several systems are centrally located. How many service plans, which can be customized to meet your specific needs, do exist? Or is response time less critical? Then, an 8-, 12-, 16- and 24-hour service "window" (on a normal workday basis) is better.

**Peripheral Controller**

To waste chassis space on peripheral controllers that only interface a single device type to UNIBUS is a one-to-one approach, driving Unibus system costs up and reliability down. A hex-wide peripheral controller that simultaneously handles several RM02/RM03 80 MB disk drives, several TU10½ tape drives and 8-MB of semiconductor disk from just a single slot offers big plusses.

Such a one-board approach, which will grow in popularity, enables one board to do the work of three or more — with no degradation — thus saving in other ways. Immediate savings come from elimination of two comparably-priced controller boards. Down the line, upgrade flexibility permits expanding configuration less expensively: you don’t (necessarily) need to buy additional boards or larger chassis.

This cuts spares inventory costs in the factory. It increases system reliability because of fewer ICs. Such cost-benefits mean rebalancing system operational costs, bringing price of I/O processing back in line costs of instruction processing and memory.

**Fixed-Head Disk Replacement**

You will look for maximum throughput, reliability and transparency when examining alternatives or replacements for fixed-head disks used with DEC computers. A reliable, solid state memory can feature a built-in controller which attaches to the Unibus on, say, DEC’s PDP-11 series. Let’s look at one example. The memory would respond through the controller in the same manner as RJS03 and RJS04 fixed-head disks. It should be faster and more reliable than disk storage (otherwise, why specify it?). As for modular flexibility, the memory storage is packaged in pluggable modules of 524K bytes (262, 144 words by 18 bits). Each 19” chassis accepts up to eight modules.

The chassis would accept a pluggable controller unit and a pluggable power supply module. Modules would be interconnected by means of a printed wire backplane; a rack-mount chassis would offer built-in forced-air cooling, thus making it self-contained.

As for chassis storage expansion, a second chassis, containing eight storage modules, could be interconnected so that 8,388 megabytes are available through one controller. Parity would be generated and checked for all data transfers; errors would be flagged. What about the pluggable feature of storage modules? Field expansion is easier, obviously, since maintenance is simplified by modular construction.

This storage system would offer total transparency to all operating software and diagnostics (because of a built-in controller). Each unit would feature two Unibus port interfaces: the first, for control and data; the second, for data only, with data transmission switched between ports under program control.

Are hardware or software changes required in the computer system to utilize the performance and reliability which the product offers? If so, investigate. If users may incorporate software patches for even greater performance, it’s a decided plus.
With LSI 11/PDP 11 Software Compatible Disc/Tape Controllers Offering Single Board Low Power µP Based Design and Low Cost...

Plus Many Other Good Reasons!

The reasons start with DILOG'S (Distributed Logic Corp's.) full time engineering and design staff. Not outside suppliers. That means when you contact DILOG for product selection or after sale service, you'll get "first hand" assistance...along with years of experience manufacturing µP based controllers that interface with DEC 11 CPUs.

The intelligent products you'll discuss all utilize common proprietary architecture and DILOG automated design techniques—products with exceptional reliability and cost efficiency...mostly available from stock. And when you plug a DILOG controller into your DEC CPU it's ready-to-run because it's fully operating system software compatible.

These high performance data storage interface products also feature • minimum bus/space requirements • up to 60% less power • 10 to 50% lower cost • automatic self-test...and numerous other features for easy system integration.

Consult the DILOG/disc-tape compatibility table for your needs. Then ask for detailed data on existing, or future products from DILOG...#1 in single board DEC 11 compatible disc/tape controllers.

Distributed Logic Corp., 12800-G Garden Grove Blvd., Garden Grove, CA 92643, Phone: (714) 534-8950 • TELEX: 681 399 DILOG GGVE

### DISC/TAPE DRIVE MANUFACTURER COMPATIBILITY CHART

<table>
<thead>
<tr>
<th>MAGNETIC TAPE</th>
<th>DISC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1½&quot; REEL-TO-REEL</td>
<td>CMD CARTRIDGE CLASS</td>
</tr>
<tr>
<td>STD. &amp; STREAMER</td>
<td>AMPEX, CAELUS, CENTURY DATA, CONTROL DATA, DEC, DIABLO, IOMEC, MICRODATA, PERTEC, TANDBERG DATA (IDT), WANGCO, TDX</td>
</tr>
<tr>
<td>2315/6440/RK05</td>
<td>AMPEX CONTROL DATA</td>
</tr>
<tr>
<td>CARTRIDGE CLASS</td>
<td>AMPEX CONTROL DATA</td>
</tr>
<tr>
<td>SMD STORAGE MODULE</td>
<td>BASF, CONTROL DATA, FUJITSU, KENNEDY, MEMOREX, PRIAM, SHUGART, SEAGATE, QUANTUM, TANDBERG DATA, MICRODATA, WANGCO, WESTERN DYNEX, DRI</td>
</tr>
<tr>
<td>WINCHESTER 5½&quot;</td>
<td>DEI, KENNEDY, PERTEC, QUANTUM</td>
</tr>
<tr>
<td>8&quot; OR 14&quot;</td>
<td>BASF, DECITEK, MICROPOLIS, PERTEC, REMEX, SHUGART</td>
</tr>
<tr>
<td>½&quot; TAPE CARTRIDGE</td>
<td></td>
</tr>
<tr>
<td>FLOPPY DISC DRIVE</td>
<td></td>
</tr>
</tbody>
</table>

CAPACITIES .25 TO 300 MB

Circle 38 on Reader Inquiry Card

*Trademark Digital Equipment Corp.*
Final bit-slice emulation provides important user benefits. The most basic is reduction in IC chip count that allows a card reduction from 24 to one. This size shrinkage uses less mainframe or expansion chassis backplane space, less power and lowers system and operating costs. It inherently increases system reliability and lowers maintenance costs. The second major benefit is technological, allowing potentially higher data throughput than the original, improved DMA operation, increased data buffering, and ability to modify firmware executed by the µP to meet custom user needs. Interfacing up to four 80- to 300-MB disks to a standard Unibus backplane at low cost, Storm-02 is software and disk media compatible with the RJM02 subsystem.

by Hildon Gold and Robert Deisher

For the past several years now, the µP has displaced functions formerly performed by hard-wired logic. These new designs are yielding circuit functions of lower cost, smaller size, lower power consumption, increased reliability and easier maintainability. Such was the case with our own design team. We were able to develop a single-board controller capable of interfacing multiple, 80-megabyte storage module drives with DEC PDP 11s.

An alternative to the RJM02 mass storage system, the Storm-02 Controller provides interfacing for four drives. Each drive offers 80- to 300-megabyte unformatted storage for the PDP-11/04 through the PDP-11/60 Computer Systems. The Storm-02 was designed to emulate DEC's RJM02, including the RM-02 disk drive and RH-11 adapter. Unlike the DEC system that required up to 24 cards plus an expansion chassis to provide an interface for mass storage drives, the new design accomplished the same functions on a single board (Figure 2). What's more, when a Storm-02 and companion mass storage modules are selected instead of the DEC System, cost savings are considerable. For the first 80-

Hildon Gold is Senior Hardware Engineer and Robert Deisher is International Marketing Manager (Europe and Mid East) for AED, 440 Potrero Ave., Sunnyvale, CA 94086.

Figure 1: DEC implementation of the interface containing an RH-11 and RM02 interface to an 80 megabyte disk. Lines A, B and C show the major division points.
enables a single controller card to mate multiple storage disks to a DEC bus
configured storage system is 35% below the cost of the equivalent DEC system. Savings upon expansion to three additional 80-megabyte drives, for a total of 269 megabytes formatted, is considerably more.

Configured as a single Hex card, Storm-02 plugs directly into a standard SPC slot and, in combination with the drive, emulates DEC’s RJM02 providing both software and media compatibility. The new Controller fully emulates DEC’s RM02 disk system and is Unibus-compatible. It is also software-transparent to PDP-11 operating systems. What’s more, Storm-02 provides media interchangeability with the RM02 since disk pack formatting is the same.

In designing Storm-02, we wanted to meet the capabilities of high data-transfer-rate, mass-storage drives while avoiding interference with other OMA hardware communications activities on the Unibus. When a DEC-based mass storage system is employed, data throughput is limited. Disk drives are limited to those with rotational speeds of 2400 rpm. In such cases data transfer suffers since it is limited to a rate of 800 kilobytes-per-second.

However, Storm-02 is capable of handling data interchange with drives running at 3600 rpm and, accordingly, a transfer rate of 1.2 megabytes per second. In doing so, the Controller allows utilization of mass storage drives having a higher data transfer rate without adversely impacting other Unibus DMA activity.

Another benefit is the ability to modify system firmware to meet the needs of other applications. This benefit will be obtained through a new product (soon to be released) allowing for any mix of 80 megabyte or 300 megabyte drives from one to four, with a single card. Other varied and specialized applications are possible by altering the card firmware.

the original system

A DEC CPU interface to a single drive is illustrated in Figure 1. The System consists as shown, of an RH-11 Massbus-to-Unibus adapter and an RM-02 subsystem. The latter contains the Massbus-to-SMD interface and the SMD drive interface (CDC 9732 unit) with the drive and media.

RH-11 contains the DMS (Direct Memory Access) controller and the programmed input/output function. It also provides the hardware interface between the CPU bus (Unibus) and an intermediate bus known as the Massbus. Other features include interrupt support, ability to perform a ‘write check’ of the data from the CPU memory and the peripheral, elastic buffering of data for the DMA transfer and special control and status registers. The elastic buffer in the original system allows for limited buffering up to 66 words (about one quarter of a sector). This hardware is contained on a complement of 6 to 7 Hex cards as illustrated in Figure 3a. Normally the cards are housed in the CPU mainframe, or in a separate expansion chassis.

Each RM-02 requires a 6- to 8-card Massbus-to-SMD interface adapter. As shown in Fig. 3a, a set of such cards is contained in each disk subsystem. The balance of the RM-02 subsystem contains the disk hardware, the power supply, drive and the media.

The actual system configuration selected for hardware implementation is shown in Figure 4. Storm-02 supports up to four 300-megabyte SMD drives. It allows for storage capacity of 80- to 300-megabytes by merely selecting or adding the drives and interconnection cables. This complete system configuration is contained in the single hex card (Figure 2). It replaces all cards (Figure 3a) ranging from 12 to 24, depending on the number of SMDs employed.
Digi-power has all the power you'll ever need in OEM power supplies.

Select from a complete line of compact power supplies, 50 to 250 watts. Each unit is burn-in for a full 12 hours at 100% rated load before final testing and packaging for shipment. Reliability is assured with a one year warranty. Digi-power has the size you need for your microprocessor, mini-computer Winchester-type modules or peripheral equipment.

Units are available open-frame or enclosed to meet your specific requirements. Standard or optional features include brown-out protection, short circuit protection, power-fail option, over-temperature protection, and OVP for all outputs. Each Digi-power component is EMI filtered and constructed of tested and proven quality materials. All units deliver up to 80% efficiency. UL approval expected in the immediate future.

The 50 watt DU50 unit is 4.25" x 7.75" x 2" height; the 250 watt DU250 Series is 4.7" x 12.25 x 2.45" height. Custom designs are available for OEM customers requiring special electrical, mechanical or physical parameters. A staff of service personnel and off-the-shelf replacement parts can be readily accessed should the need arise. Call or write for informative booklet and specification sheets.

686 E. Gish Road / San Jose, CA 95112 / (408) 288-5600 / TWX 910-338-0579

Circle 39 on Reader Inquiry Card
achieving transparency

To accomplish user transparency, the Storm-02 card had to function as in the original system. It was necessary for the hardware to electrically interface the Unibus. Also, the firmware had to cause the card to respond identically to the software commands of the RH-11/RM02 subsystem. Furthermore, the media and its pack formatting had to be the same as the original. Only then could the computer systems user proceed as if an RJM02 disk system were actually installed on the Unibus.

The software commands to which the card must respond include recognizing the positioning, data transfer, and housekeeping commands listed in Table 1. The Controller also had to provide the twenty-two, 16-bit Command/Status registers, the DMA buffering and the generation of the CRC (Cyclic Redundant Code) and ECC characters that are added to the sector header and data records, respectively. There had to be provisions to verify the CRC and ECC during a read and to generate the ECC syndrome. Finally, additional hardware was necessary to handle the SMD interface for one to four

| Table 1: 16 Software commands that are recognized by the emulated card (identical to the RJM02 commands). |

<table>
<thead>
<tr>
<th>Positioning (no data transfer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEEK</td>
</tr>
<tr>
<td>RECALIBRATE (Return to zero cylinder)</td>
</tr>
<tr>
<td>±OFFSET</td>
</tr>
<tr>
<td>RETURN TO CENTERLINE</td>
</tr>
<tr>
<td>SEARCH (SEEK and find header)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Data Transfer Commands (DMA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write header and data (&quot;FORMAT&quot;)</td>
</tr>
<tr>
<td>Write data only</td>
</tr>
<tr>
<td>Write check header and data (&quot;FORMAT VERIFY&quot;)</td>
</tr>
<tr>
<td>Write check data only</td>
</tr>
<tr>
<td>Read header and data</td>
</tr>
<tr>
<td>Read data</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Housekeeping (Status Setting or Error Clearing)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO OP</td>
</tr>
<tr>
<td>DRIVE CLEAR</td>
</tr>
<tr>
<td>RELEASE (Dual Access Command)</td>
</tr>
<tr>
<td>Read in PRESET</td>
</tr>
<tr>
<td>Disk pack acknowledge</td>
</tr>
</tbody>
</table>

Figure 4: A DEC four drive configuration showing the Unibus interfaced to four disks. This configuration was selected by AED for emulation on a single HEX card, the STORM 02.
adac... Everything for LSI-11 data acquisition and control.

- mV Level A/D Conversion
- Temperature Measurements
- High Level, High Speed A/D Conversion
- TTL Level Digital I/O
- Discrete, High Voltage, AC/DC Interfaces
- Pulse Counters And Pulse Trains Out
- Optically Isolated Discrete I/O
- Contact Closure Sensing
- Discrete High Current Outputs
- Programmable Clock
- Serial Interfaces
- PDP-11 Unibus To LSI-11 Bus Translator
- Specially Designed Enclosures
- Screw Termination Panels
- Rack Mount System Cabinets
- CPUs/Memories
- Floppy/Tape Peripherals
- CRT Terminals
- Real Time Operating Systems
- FORTRAN, BASIC, Process Language

ADAC offers the widest selection of function cards and complete systems for LSI-11. Both analog and digital.

Call, write or circle the number below and we'll send you a complete packet of information, including ADAC's new Model Configuring Guide and Price List.

Circle 40 on Reader Inquiry Card
The implementation

Identified in the block diagram in Figure 5 are five subsystems implemented in the single Storm-02 Hex board controller. This subsystem includes Host Interface to the Unibus; a Microsequencer and Bit Slice ALU operated as a sequential machine; SMD Drive Interface; Disk Data-Pathing and Elastic Storage; and Data Error Detection and Correction Circuits.

The µP controls the operation of all blocks. It runs at a 200-ns microcycle rate enabling eight instructions to be executed with each 16-bit word that is transferred to or from the SMD. The µP memory is 2048 words deep, each word 56-bits wide. This memory is called the “Control Store.” The processor ALU is 16 bits wide (size of the standard data word which it must process). The Bit-Slice Elements chosen for the system are the 2900 bipolar series that include the 2901 Bit Slice ALU and 2910 microprogram sequencer chip.

The µP operates in classical “pipeline” fashion. That is, the control word for the next operation is brought out of memory while the function fetched from the last operation is acted upon by the µP. In addition, the very wide word enables sequencer, ALU, and Source and Destination Addresses to be acted upon in parallel. This results in an unusually high controller throughput speed compared to a conventional 8- or 16-Bit machine which is otherwise impeded by vertical architecture and sequential operations.

This 56-bit word is shown in Figure 6. The 11-bit address enters the control store from the 2910 sequencer. The several fields of the word are the microsequencer instruction field (10 bits), the ALU instruction field (18 bits), the immediate data field (16 bits) and the miscellaneous control field (12 bits). During each micro-instruction cycle, the entire word is available for use in the control sequences and as commands that are sent to each of the other five blocks. The actual functions performed by the µP are command sequencing (execution), decision-making and bookkeeping. These responsibilities can be summarized as follows: software command interpretation, sequencing SMD’s (select drive, position heads, etc.), comparison of disk sector with the desired one, switching and routing of data in the data pathing block, data comparison for write verify, overall system timing, communications of status to host Interface, and error handling and recovery.

the interfaces

The Host Interface (Figure 5) provides communications between Host CPU and Disk Controller and also implements Unibus Protocol. It contains the 22 Command/Status registers. The Host PDP-11 has full priority over these registers. The Host Interface provides the user programmable I/O addressing, interrupt priority and interrupt vector as provided.
STATE-OF-THE-ART INFORMATION

Each Proceedings offers original technical papers by testing technology experts involved in management, manufacture and application of automated testing for electronics manufacturing. Plus, the Proceedings from January 1978, June 1979, January 1980 and June 1980 include testing article reprints from either Circuits Manufacturing or Electronics Test magazines. The January 1980 Proceedings also includes technical papers from the Test Instruments Conference.

- Burn-in
- Hardware
- Economics of ATE
- Innovative Techniques
- In-circuit vs. Edge Card ATE
- LSI Testing
- Software for ATE
- Bare Board Testing
- ATE Management
- Analog and Digital ATE

VOLUMES PRICE/VOLUME

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>January 1978</td>
<td>$15*</td>
</tr>
<tr>
<td>June 1978</td>
<td>$15*</td>
</tr>
<tr>
<td>June 1979</td>
<td>$15*</td>
</tr>
<tr>
<td>January 1980</td>
<td>$15*</td>
</tr>
<tr>
<td>June 1980</td>
<td>$15*</td>
</tr>
<tr>
<td>January 1981</td>
<td>$35*</td>
</tr>
<tr>
<td>June 1981</td>
<td>$55</td>
</tr>
</tbody>
</table>

* Special discount

Payment or purchase order must accompany order. Please add $2.50/volume for postage and handling (domestic book rate). Add $5.50/volume for air mail orders to Mexico and Canada, and $15.00/volume for air mail orders to all other countries. Mass. residents add 5% sales tax. Make checks payable (in US dollars only) to ATE Proceedings.

To place an order or to request more information, return the coupon below to ATE Proceedings, c/o Benwill Publishing Corp., 1050 Commonwealth Avenue, Boston, MA 02215, USA. (617) 232-5470.

Name _____________________ Title _____________________
Company ____________________________________
Address ____________________________________
City __________________ State ____________ Zip __________

☐ Please send me the volume(s) I have indicated. I have enclosed $________.
☐ Please send me more detailed information about each of the Proceedings I have checked.
☐ I do not wish to order a book, but please add my name to your mailing list.
Figure 6: The 56 Bit word used for the State Sequential Bit-Slice Machine and how it ties into the system. The firmware contains up to 2048 such words that are executed in pipeline fashion.

EYECOM II
the IMAGE PROCESSING PERIPHERAL

Add this image processing peripheral to your present PDP-11* or LSI-11* to measure variations in image brightness, separate image features, enhance edges and contrast, measure areas of interest, do real time image integration, and real time image differencing.

A basic software package is provided to apply the EyeCom System to your particular problem.

FEATURES:
- Real Time Digitizing, 640x480x8-bits
- Add, Subtract and Convolution of images at video frame rates
- Joystick Cursor, 640x480 Resolution
- Graphic & Alphanumeric Overlay
- Color & Gray Scale Mapping Tables
- Terminal or Rack Mount Configuration

Call or write for complete information:

Spatial Data Systems, Inc.
P.O. Box 978, 508 So. Fairview Ave., Goleta, CA 93117 • Tel: (805) 967-2383

The Image Processing Company

Circle 42 on Reader Inquiry Card
Figure 7: The "elastic" data buffering in the system. This buffering accommodates the asynchronism between the disk and the Unibus™.

in the original DEC system. It also arbitrates DMA requests on the BUS, servicing the interrupts and generates the Unibus protocol.

Like the main µP the HOST Interface consists of a state sequential machine built around 4-bit binary counters with a 16-bit control word and a 100-ns cycle time. There are 256 words in its separate control memory and its operation is "pipelined" as with the main µP instruction bus.

The SMD Drive Interface communicates with the standard Storage Module Drives. These drives are equipped with NRZ-to-MFM and NRZ-data protocol conversion. Although the original system supported a disk drive with a 2400 RPM spindle speed, our design supports spindle speeds up to 3600 RPM. This permits data transfer rates of up to 1.212 MB/sec when necessary (16 bits per 1.648 ms). All parallel and serial data passes through this block via the SMD individual read/write cables. This block also contains I/O latches and differential line receivers and transmitter implemented in

---

IEEE 488 ↔ DEC

On the highway, speed limits are necessary. But in the world of data processing, faster is better.

That's why National Instruments will introduce the GPIB I/V-2 Q-Bus Interface to link with IEEE standard 488 instrumentation bus. Since it uses DMA the speed far exceeds our existing high performance non-DMA GPIB/I IV-1.

Software greases the wheels.

Software support? NI has utility and driver programs available as MACRO source files. You can assemble them as FORTRAN, BASIC, or MACRO subroutines.

NI also makes two versions of IEEE 488 interfaces for the PDP-11. For the kind of transferring horsepower we offer, you'd expect a high-octane price. But we think you'll be pleasantly surprised.

Contact us today. We'll get you where you want to be—in a hurry.

NATIONAL INSTRUMENTS

The faster the better.

National Instruments
8900 Shool Creek Blvd.
Austin, TX 78758
512/454-3526 or 1-800/531-5066

Circle 43 on Reader Inquiry Card

JULY 1981 Digital Design 71
The Data Pathing and Elastic Storage (Figure 5) contains circuitry that performs appropriate serial-to-parallel and parallel-to-serial conversion during data transfer to and from the SMD interface. It also provides 768 words (3 sectors) of data buffering between controller and disk. This allows the temporary storage required for the asynchronism that exists between the Host CPU's memory, other peripherals, and the SMD. The Serializer andDeserializer with a 16-word hardware FIFO are all implemented in LSI. The 768-word buffer is a firmware-controlled data FIFO using RAM array organized as 1K × 16 bits.

Figure 7 illustrates the "elastic" buffering of data to and from the disk. Data transfers bidirectionally through the Serializer/Deserializer FIFO, entering and leaving the 768 (1K) work RAM that operates under the control of the μP. At the appropriate time for the Unibus, it is strobed on or read from the Unibus through the port registers. The actual sequence is an effective asynchronous "bucket brigade" of data from disk to 16-word FIFO, to the RAM buffer, to the Bit-sequencer, and finally to the Unibus port on a read. The reverse data flow occurs on a disk write. This approach allows the μP to accommodate asynchronism within the system.

The Data and Header Error Detection and Data Correction Block (Figure 5) contains the circuitry to provide these functions. It has two basic sections. The first contains the Header CRC generation and checking functions and is implemented with a single LSI device. The second performs the ECC generation and checking and is implemented with MSI logic elements.

**self-test capability**

It was possible to add automatic and continuous built-in-test to a large portion of the circuitry in the emulator card. The emulated system supports all pertinent DEC test diagnostics as well as performing those of its own. A thorough self-test is performed just after power-up with some continuous self-testing being performed in normal card operation. The results are displayed by on-board LEDs. This can dramatically decrease system down time to locate a failed card. Thus, it enhances the already decreased troubleshooting requirements provided by the reduction in system cards from 12 or more to just one.

Once a failed card is returned for field repair, the bad component still must be located. This is not easily accomplished with end-to-end tests. By altering the μP's "Control Store" in the form of its firmware, special tests can be generated that thoroughly test the system and locate failed parts. The first approach was to generate a special set of Control Store firmware to work in conjunction with the host CPU. This ROM set is placed into the system in place of normal firmware.

During the design phase, it was recognized that a more powerful approach to testing would be of significant advantage in the system. In this case, the ability to replace the μP Control Firmware with an external RAM was added to the system. Now, the normal firmware would be replaced by these RAM-stored microcode diagnostic sequences that are loaded from the outboard CPU's own mass storage medium (floppy, cartridge, magnetic tape, etc.). This approach was called "Writable Control Store." With such a special fixture, far more complex testing can be done on a failed card to locate problem components. This feature is valuable to volume OEM houses that choose to purchase such a system to establish their own field repair depot.
COMTAL brings you image processing for the 80's with their Vision One/20. The system that has been developed to handle your image analysis and interpretation through the 80's. With advanced features that give you a cost-effective real-time image enhancement system.

Hardware options from COMTAL include continuous zoom (COZO), an interactive spatial warping system (MAPPER), multimegabyte virtual refresh memory (VREFM), and a digital video input processor (DVIP) for high quality film imagery.

Applications for the 80's
Besides the traditional areas of Landsat interpretation and enhancement as major applications for the 80's, there are several new emerging applications that are already taking advantage of digital image processing techniques.

These include:
• Seismic Analysis — Major oil and gas companies are using COMTAL's Vision One/20 for analysis of seismic data.
• Printing/Graphics — New applications are developing for using digital image processing in graphic arts composition and printing.
• LANDSAT/Meteorology/Oceanography — Interpretation of remote sensing and satellite data to better understand the world around us.
• Medical — Enhancement, even in color, of X-rays and other medical imagery.
• Non-destructive testing — More and more industries are using image processing to better analyze non-destructive testing data.

To find out how COMTAL's Vision One/20 can take your images into the 80's, call or write today.

Real-time image analysis for the 80's

505 W. Woodbury Road, Altadena, CA 91001, (213) 797-1175  TWX 910-588-3256  See Us At Siggraph/81, Booth #325  Circle 47 on Reader Inquiry Card
SIGGRAPH '81 Blends Art With Science
dallas hosts eighth annual conference

Following the computer industry's rapid growth, SIGGRAPH '81 will have ten times the attendance that SIGGRAPH '74 had. And with reports painting a bright picture for computer graphics in the future, SIGGRAPH members are confident the growth trend will continue.

By Bob Hirshon

Computer match-making may not be the most highly regarded use of advanced digital electronics. But some of the resulting couples, as well as their progeny, have gone on to attain considerable note. The SIGGRAPH conference, held this year in Dallas, celebrates one unlikely couple, science and art, and especially their illustrious offspring, computer graphics. Representatives from both the scientific and artistic families will participate in the celebration, featuring exhibits of state-of-the-art hardware, introductory graphics courses, and advanced technical sessions.

"The exhibits, which we started in the '75 conference, went from five exhibitors, that were given space, to 124 this year, covering 40,000 square feet of exhibit space," says Tony Lucido, committee co-chairman. This year's vendors will be demonstrating turnkey applications (CAD/CAM, cartography, image processing), OEM products, film and paper hard copy devices, interactive vector and raster displays, graphical input devices, software support packages and time-sharing services.

Unlike most computer shows, SIGGRAPH's primary aim is to educate, not sell. In fact, the original show consisted only of seminars — there were no vendors at all. Today, even with exhibitors playing a large role in SIGGRAPH, education is the show's first responsibility. "We're predominantly an educational and technical group — not to the exclusion of the practitioner, but really in support of the practitioner," says Lucido. "We don't have any intentions to discard that — we intend to make sure it remains strong."

"Some of the vendors in the past," adds Doug Green, SIGGRAPH's other co-chairman, "have made the statement that they'd sure like to get as many potential paying customers as possible — but, on the other hand, we have to look to the future of the enterprise also, and make sure that the students of today are the buyers of five years from now."

During the first two days of the con-

This computer-generated art represents just a few of computer graphics' many applications. Top, left to right: Virus protein coat, Nelson Max, Lawrence Livermore National Lab; Fractal curves, Loren C. Carpenter, Boeing; 3-D bar chart, P. Preuss and A. Vinberg, ISSCO. Bottom, left to right: Atlantic Ocean Bathymetry, Larry McCleary, Naval Ocean System Center, San Diego; Steel cylinder bending over rail, Bruce Eric Brown, Lawrence Livermore National Lab; Mathematical function summation, M. Prueitt.
ference, there will be 18 one- and two-day tutorials and seminars. Tutorials are introductory courses in such topics as “How to Design User-Computer Interfaces” and “Introduction to Raster Graphics.” Seminars will be somewhat more in-depth, and will include subjects such as “Introduction to Computer-Aided Design” and “Graphical CAD Systems for VSLI.”

Thirty-five technical programs will be presented during the final three show-days. Each will last from one to two hours and most will be presented sequentially, allowing attendees to participate in most of the 35. Eight topic areas in computer graphics will be covered: Theory and Algorithms, Graphics Hardware, Interaction Techniques, Graphics Software and Languages, CAD/CAM, Applications, Animation, and Raster Graphics. “We received in the neighborhood of 150 papers this year,” says Green. “They were reviewed by a team of reviewers and then the senior reviewers got together and the 35 best were chosen to actually be presented at the meeting.”

Traditionally, evening film and videotape extravaganzas highlight SIGGRAPH, and this year will be no exception. Great pains have been taken to provide the best audiovisual equipment in ideal projection environments. Master of Ceremonies for the first of three evening shows will be Tony Lucido, of Intercomp Resource Development and Engineering, presenting an introduction to computer graphics.

On the following night, Pat Cole, of Lucasfilm, will deliver a show devoted to science and technology. “Material will be picked for how interesting the content is, for variety of techniques using computer graphics, for variety of sciences represented and for aesthetic appeal,” explains Cole. “The film shows are just purely visual treats,” she adds. “The content will be such that people will be able to learn something from it, but it’s there mainly for the people to go and enjoy visually.”

Thursday night is art and entertainment night, presented by Tom Defanti, of the University of Illinois. As an added feature, the A/V equipment in the theater will be available during lunch hours for attendees’ informal showings.

Because of the climatic conditions of Dallas in August, SIGGRAPH planners put much effort into insuring that attendees keep their cool. “We’re putting on extra busses, and making sure they’re all air-conditioned,” says Green. “And everything is under one roof this year; as a result, once people get to the convention center, they won’t have to go out into the heat.”

SIGGRAPH committee members expect about 8000 people to brave the Dallas summer and attend the conference this year. That’s up about 20% from last year. What’s behind this rapid growth? “Graphics is one of those things that has previously been very expensive,” explains Green, “but with the cost of memory and the cost of computer display systems coming down so rapidly, it’s becoming much more affordable to a larger number of folks. Three or four years ago, the number of attendees who actually owned systems was fairly modest, because of the high cost. The cost factor is the driving factor behind the tremendous growth we’ve had.”

This rapid growth has brought its share of problems, says Lucido, but nothing the committee can’t handle. “It’s grown fast enough so there have been growth pains,” Lucido sums up, “but I think it’s all been for the benefit of graphics.”
Don't connect remote terminals to your Unibus*-based computer

UNTIL YOU'VE READ ABOUT DCA'S SYSTEM 205 UNIBUS-INTERFACE STATISTICAL MULTIPLEXOR.

A DZ11 emulator and stat mux in one.
That's what DCA's System 205 gives you. In fact, a single DCA 205 acts as a host-end multiplexor for PDP-11, VAX or 2020 computers while eliminating up to 16 DZ11 modules!

Supports up to 128 remote terminals.
With a 205 and another DCA statistical multiplexor at the remote end, you can support up to 128 remote asynchronous terminals. Any DZ11's already in use for remote-site service can be transferred to local service.

Requires just a single Unibus slot.
That's right, the 205 only uses one Unibus hex slot, freeing up from three to fifteen additional slots. Costly and unsightly cables are eliminated, too.

Superb response time.
The 205 is, in effect, a DZ11 and statistical multiplexor in one integrated unit. So the character delay that normally occurs between a DZ11 and a multiplexor is eliminated. Result: Your terminal users will enjoy a crisper echo.

Statistical multiplexing.
Our 205 gives you all the benefits of DCA's statistical multiplexing, including full ARQ error control that maintains data integrity, network transparency, reduced CPU overhead — and more.

Multipoint multiplexing.
This isn't a promise, it's a fact: DCA's customers have been multidropping several remote terminal locations to a single telephone line since 1979. And multipoint multiplexing with the 205 lets you enjoy

Multipoint multiplexing lowers costs dramatically.

the lowest cost communications possible from Unibus-based DEC computers.

Reliable, proven performance.
Like our other statistical multiplexors, the 205 is a field-proven, reliable system. In 1974, DCA introduced statistical multiplexing — we've been the technological leader ever since!

Unparalleled growth potential.
For networks that are bound to grow, DCA is the clear-cut choice. Because complete system compatibility lets you start with a 205 today, and grow into a larger, more powerful network tomorrow. And DCA users enjoy the lowest-cost network growth in the industry!

Excellent cost efficiency.
There is no better value for DEC users — the 205 will dramatically reduce your datacomm costs while providing high throughput and reliable operation. Interested? Send in the coupon or call DCA at 404/448-1400 today.

Digital Communications Associates, Inc.
303 Research Drive, Suite 225
Norcross, GA 30092

* Unibus, DEC, DZ11, PDP-11, VAX and 2020 are trademarks of Digital Equipment Corp.

Circle 49 on Reader Inquiry Card
None of the methods described here will detect all possible errors that could occur in a data transfer system. The effectiveness of a code is a measure of how low the probability is that an error could get through the code system undetected.

Cyclic Redundancy Code or CRC-based systems have different effectiveness factors dependent on randomness of data transferred and on the actual generator polynomial used. Storage systems impose their own characteristics in determining randomness of errors, and thus which method of error detection to employ.

CRC-16 is most common in data communications and in disk applications because it is especially effective where errors are more likely to occur in bursts. Where errors are more likely to be single-bit, or two-bit errors, LRC may prove equally effective. Checksums are used to protect assembler object code integrity in development software, since it is virtually independent of the storage media, and also since it is relatively easy to generate and check.

The four-bit CRC algorithm described offers a good trade-off between execution speed and memory usage for applications that include data communications controllers mini-floppy disk controllers, tape controllers and many more. The approach outlined can be used to advantage in any computer that facilitates table look-up.

By Rich Lee

This article describes an efficient and effective means of accomplishing the task of error detection using Cyclic Redundancy Codes, (CRC). The principles described are generally applicable.

CRC background

Codes are usually described in mathematics as closed sets of values that comprise all the allowed number sequences in the code. In data communications, transmitted numbers are essentially random data patterns which are not related to any predetermined code set. The sequence of data, then, is forced into compliance with the code set by adding to it at the transmitter. Thus, a string of original data would become the original string concatenated with a string of extra numbers that make the total string one of allowed code set values.

At the receiver, incoming data is checked to see if it is one of the allowed code set values. The assumption is made that if an error occurred in transmission, likelihood of the result also being a valid set member is very low. If the received data string is found to be of the allowed code set, it is assumed that no errors have occurred and that the data is valid.

Several points have emerged from the above discussion. (1) There is a need to have a scheme of determining what precise extra string to append to the original data stream, to make the concatenation of transmitted data a valid member of the code set. (2) There must be a consistent way of extracting the original data from the code value at the receiver, to deliver the actual data to the location where it is ultimately used. (3) For the code scheme to be effective, the set must contain allowed values sufficiently different from one another that expected errors will not be able to alter one allowed value such that it becomes a different allowed value of the code set.

A system for coding and detecting errors in common use in Data Communications and in systems using serial data storage devices is called CRC. The code set is made up of all strings of binary data that are evenly divisible by what is referred to as a "generator polynomial" — a specially selected number that results in a code set of values different enough from one another to achieve a certain low probability.

Richard H. Lee is Strategic Marketing and Application Engineer for the Microcomponent Product Division, Mostek Corp, 1215 West Crosley Road, Carrollton, TX 75006
Figure 1: Error detection system.

Figure 2: Register implementation.
other to achieve a certain low probability of an undetected error. To determine what to append to the string of original data, a division is made of the original string as it is being transmitted. When the last data is past, the remainder from the division is the required string to add since the string including the remainder will be evenly divisible by the generator polynomial. Since the generator polynomial is of a known length, the remainder added to the original string is of a fixed length.

At the receiver, the incoming string is divided by the generator polynomial, and if the incoming string does not divide evenly — that is if the remainder after division is not zero — then an error is assumed to have occurred. If the remainder is zero, then the data is assumed to be error free, and the data delivered to the ultimate destination is the incoming data with the fixed length remainder field removed. Figure 1 illustrates the stages of this coding method.

In binary CRC schemes, the generator polynomial is designated as a sum of terms of "X" raised to the power of the bit the term represents. For example, the CRC-16 generator polynomial is actually the binary number, 1 1000 0000 0000 0 101, while it is customary to represent it with the following expression: \(x^{16} + x^{15} + x^2 + x^0\).

**Shift Register Implementation**

The division process is simpler in modulo-two arithmetic than it is in decimal arithmetic. Implementation of a divider for a 17-bit polynomial can be done using a 16-bit shift register with an exclusive-OR feedback gate for each term of the polynomial, except the most significant bit, (bit 16). The exclusive-OR gate that corresponds to bit 16 of the polynomial is designated as a sum of the term the bit represents. For example, the CRC-16 generator polynomial is (16) 0, while it is customary to represent it with the following expression: \(x^{16} + x^{15} + x^2 + x^0\).

The division process is simpler in modulo-two arithmetic than it is in decimal arithmetic. Implementation of a divider for a 17-bit polynomial can be done using a 16-bit shift register with an exclusive-OR feedback gate for each term of the polynomial, except the most significant bit, (bit 16). The exclusive-OR gate that corresponds to bit 16 of the polynomial is designated as a sum of the term the bit represents. For example, the CRC-16 generator polynomial is (16) 0, while it is customary to represent it with the following expression: \(x^{16} + x^{15} + x^2 + x^0\).

**Figure 2** shows the classical shift register circuit used to perform the division for the case of the CRC-16 polynomial. To generate the remainder for transmission, the shift register is first preset to all zeros. The serial data is shifted in at the point marked Input. When the end of the data is reached, the final contents of the shift register are appended to the serial data stream by lowering the feedback enable input labelled ENFB. The stream thus generated is a member of the CRC-16 code set, since it is evenly divisible by the polynomial.

The box in Figure 2 labeled FEEDBACK POLYNOMIAL is an AND gate array. The output signals PXX refer to the X terms in the polynomial. CRC-16 would have the outputs, P00, P02 and P15 enabled such that when the input went high, those outputs would go high but the other outputs would not go high. In applications not requiring more than one polynomial, much of the indicated circuitry could be eliminated. This example is intended to be general enough to handle any seventeen term CRC polynomial, simply by enabling the appropriate PXX outputs. The shift register cells are shown in detail in the insert at the bottom of the figure. The inverter inside the detail is used when testing the contents of the shift register for zero at the end of the receive operation.
The selector in the lower right hand portion of Figure 2 is used to select the data on the signal labelled INPUT to be forwarded to the OUTPUT line, while the shift register is accumulating the CRC. The shift register contents are selected at the same time as the feedback enable is removed when it is desired to concatenate the CRC value to the data stream. The rightmost bit in the shift register is the first to be shifted out.

The shift register can also be implemented with a software algorithm. Assembly language is used to define the algorithm (Figure 3). Like the hardware implementation, the software algorithm also accommodates any polynomial.

By altering the value in the equation for POLYU and POLYL, any CRC generator polynomial can be facilitated. It is necessary to call the subroutine for each bit of data. As this routine may take up to 111 μs to execute with a 4-MHz clock, the software implementation is often only useful for slower data transmission rates. The calling program is responsible for initializing the values of CRCU and CRCL, shifting each bit of data, and making the call to CRCSHF for each data bit. When the end of data is reached, the calling program places the CRC bytes into the data stream, CRCL first, followed by CRCU.

The table of Figure 4 shows the values taken on by the shift register in the single bit shift approach in response to the input stream in the left column. The feedback gating, generated by the exclusive-OR of input data with the rightmost bit of the register, is shown in the next column. Notice its value in the lower half. Each line of the table shows the register contents after the clocking takes place. These values are the same whether the hardware or the software implementation is used.

classical implementations

The hardware implementation of the single shift logic is usually fast enough for most applications. There are components made with selectable polynomials integrated into a single chip. The main drawbacks to hardware implementation are inherent cost, and single-sourcing of most single chip hardware. The drawbacks to software emulation center

<table>
<thead>
<tr>
<th>Input</th>
<th>Feedback</th>
<th>CRC-16 Value After Shift Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0000 0000 0000 0000</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1010 0000 0000 0000</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0111 1000 0000 0000</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1101 1110 0000 0000</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0110 1011 1000 0000</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0011 1100 0101 1110</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1101 0101 1100 0011</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0101 1011 1100 1100</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0111 0000 0000 0000</td>
</tr>
<tr>
<td>(Input value from this point is current shift register contents)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0011 1100 1011 1010</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0001 0101 1110 1100</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0000 0111 0011 0110</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0000 0000 1011 1000</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0000 0000 0000 0000</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1110 1110 1100 1110</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1011 1001 0001 1110</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0010 1011 1100 1100</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0000 0000 0000 0000</td>
</tr>
</tbody>
</table>

Figure 4: CRC shift table

<table>
<thead>
<tr>
<th>After First Shift</th>
<th>After Second Shift</th>
<th>After Third Shift</th>
<th>After Fourth Shift</th>
</tr>
</thead>
<tbody>
<tr>
<td>F(0)</td>
<td>C(15)</td>
<td>F(1)</td>
<td>F(2)</td>
</tr>
<tr>
<td>F(0).XOR.</td>
<td>C(14)</td>
<td>F(0).XOR.</td>
<td>C(15)</td>
</tr>
<tr>
<td></td>
<td>C(13)</td>
<td>F(1).XOR.</td>
<td>C(14)</td>
</tr>
<tr>
<td></td>
<td>C(12)</td>
<td>F(0).XOR.</td>
<td>C(13)</td>
</tr>
<tr>
<td></td>
<td>C(11)</td>
<td>F(0)</td>
<td>C(15)</td>
</tr>
<tr>
<td></td>
<td>C(10)</td>
<td>F(0).XOR.</td>
<td>C(14)</td>
</tr>
<tr>
<td></td>
<td>C(09)</td>
<td>F(1)</td>
<td>C(15)</td>
</tr>
<tr>
<td></td>
<td>C(08)</td>
<td>F(0).XOR.</td>
<td>C(13)</td>
</tr>
<tr>
<td></td>
<td>C(07)</td>
<td>F(0)</td>
<td>C(12)</td>
</tr>
<tr>
<td></td>
<td>C(06)</td>
<td>F(0).XOR.</td>
<td>C(11)</td>
</tr>
<tr>
<td></td>
<td>C(05)</td>
<td>F(1)</td>
<td>C(10)</td>
</tr>
<tr>
<td></td>
<td>C(04)</td>
<td>F(0).XOR.</td>
<td>C(09)</td>
</tr>
<tr>
<td></td>
<td>C(03)</td>
<td>F(0)</td>
<td>C(08)</td>
</tr>
<tr>
<td></td>
<td>C(02)</td>
<td>F(0).XOR.</td>
<td>C(07)</td>
</tr>
<tr>
<td></td>
<td>C(01)</td>
<td>F(0)</td>
<td>C(06)</td>
</tr>
<tr>
<td></td>
<td>F(0).XOR.</td>
<td>F(0).XOR.</td>
<td>C(05)</td>
</tr>
<tr>
<td></td>
<td>C(01)</td>
<td>F(1).XOR.</td>
<td>C(04)</td>
</tr>
</tbody>
</table>

Figure 5: Four Bit CRC-16 Shift Table
Figure 6: Four Bit CRC-16 Look-up Table

Figure 7: Four-bit shift CRC hardware implementation.
around the large cost in time needed to execute the shift algorithm. The hardware implementation uses exclusive-OR gates and other simple components available for many years. The software implementation actually does a "blind emulation" of the hardware. Some micros, for example, manipulate data in a much more sophisticated way than doing simple exclusive-ORs and shifting a bit at a time. There is actually very little gained by restricting the software CRC accumulation function to one bit at a time. A possible reason for restricting the treatment to one bit at a time might be to maintain very strict emulation of the hardware.

Looking back for a moment at the hardware shift implementation of Figure 2, a few key functions are evident. The least significant accumulated amount is exclusive-ORed with the incoming data to produce a gating function that activates the feedback paths. The result of the gating function from above activates a feedback pattern that depends strictly on the generator polynomial. The activated legs to the shift register are exclusive-ORed with the previous stage of the shift register and accumulated.

The single feature about the single bit implementation that makes it attractive also makes it deceptively simple. The exclusive-OR of two single bits can only result in either a "one" or a "zero". Thus, the polynomial is either gated into the register or is not. This fact is not true of hex numbers, for example. Two hex numbers exclusive-ORed together can form any of 16 different values. Bytes exclusive-ORed form a set of 256 different values.

**four-bit CRC method**

In deriving a multi-bit method for CRC calculating, it should be sufficient to compare the new method with the old and show that the differences are in implementation only and do not alter the function. This is true, since shifting several bits

---

**Figure 8: CRC 4-Bit Shift Software Implementation**

In deriving a multi-bit method for CRC calculating, it should be sufficient to compare the new method with the old and show that the differences are in implementation only and do not alter the function. This is true, since shifting several bits
Examine the fourth column of values in the table. The following points emerge. Cells used to contain C(12) through C(15) now contain a value determined by an operation on I(0) through I(3) and C(0) through C(3). The lower three groups of four cells contain values made up of the previous contents of cells four shifts upstream from them and of the function of C(0)-C(3) or I(0)-I(3). The functions F(C,I) can be expanded to show that no terms other than C(0)-C(3) or I(0)-I(3) occur, meaning that the function is entirely made up of those terms, and so it may be implemented with a single exclusive-OR of I(0)-I(3) with C(0)-C(3) followed by a table look-up.

Each group of four cells of the CRC register is entirely dependent on the four cells upstream and the feedback function. It can be seen that continuation of the shifting would not alter the conclusions drawn, as the original values of the register would propagate toward the rightmost position without losing their respective positions in sequence. The F terms would eventually take the places of the C terms. The property of the F function that makes it a deterministic result of the input and the rightmost shift register contents hinges on the number of bits and the number of shifts used. The number of shifts — whether one, two, four, eight, or even 16 — must equal the number of bits of the register that go into calculating the function, F. This is intuitively correct, since the number of shifts equals the number of input bits, which must be the same as the number of bits of the register in order to have a meaningful exclusive-OR.

Looking into what makes up the F functions, a basis for the table look-up scheme begins to appear. F(0) is the exclusive-OR of the terms I(0) and C(0). If f(i).XOR.C(i) is replaced by the term T(i), the following simplifications can be made:

- F(0) = T(0)
- F(1) = T(1).XOR.T(0)
- F(2) = T(2).XOR.T(1).XOR.T(0)
- F(3) = T(3).XOR.T(2).XOR.T(1).XOR.T(0)

This is intuitively correct, since the number of shifts equals the number of input bits, which must be the same as the number of bits of the register in order to have a meaningful exclusive-OR.

Looking into what makes up the F functions, a basis for the table look-up scheme begins to appear. F(0) is the exclusive-OR of the terms I(0) and C(0). If f(i).XOR.C(i) is replaced by the term T(i), the following simplifications can be made:

- F(0) = T(0)
- F(1) = T(1).XOR.T(0)
- F(2) = T(2).XOR.T(1).XOR.T(0)
- F(3) = T(3).XOR.T(2).XOR.T(1).XOR.T(0)

The T functions are what result from exclusive-ORing the input with the rightmost CRC shift register contents. If a four bit wide exclusive-OR is taken, the bit-by-bit result can be expressed this way: C(3),C(2),C(1),C(0) = XOR. I(3),I(2),I(1),I(0) = T(3),T(2),T(1),T(0).

A table is then generated using T values as the index into the table. The contents of the table are the F functions that must be exclusive-ORed with CRC register contents (Figure 5). The table need only contain seven-bit entries, corresponding to the seven bits in Figure 5 that require other than a straight shift. Furthermore, the index made up of the vector T(3),T(2),T(1),T(0) defines the depth of the table to be 16 words. In order to preserve generality and accommodate all polynomials, the table should be 16 words by 16 bits. The bits of the CRC register that do not require modification would result in the table value being zero.

Figure 6 shows the table contents for the CRC-16 polynomial. The individual bits were generated using exclusive-ORs over the index, as suggested by the simplified equations for the F terms from the preceding paragraph.

The T values in the figure represent the index into the table. The E values are the entries, which are exclusive-ORed with their respective bits in the CRC shift register as presented in Figure 5. The exclusive-OR is done after the shift.

The four-bit shift algorithm for CRC calculation can be implemented in hardware or in software. Figure 7 shows the

<table>
<thead>
<tr>
<th>X</th>
<th>S</th>
<th>L</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>T</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

...
The four bit CRC algorithm described in this article offers a good tradeoff between execution speed and memory usage for applications that include data communications controllers, mini-floppy disk controllers, tape controllers and many more.
hardware implementation, while Figure 8 shows the software approach. The hardware implementation is shown mainly for reference and would not offer a great improvement in cost effectiveness over the single-bit shift approach.

The boxes in Figure 7 marked XOR are 7486's, or equivalent. The ROMs and 4-bit registers are best implemented with 32 x 8 PROMs and 8-bit D-flip-flops, such as 74288 and 74273s. For CRC-16, ROM A and ROM B contain the portion of the table of Figure 6 designated E(15) through E(0), while ROM C and ROM D are programmed with E(07) through E(00). Each shift of the clock accomplishes what four clock shifts did in the implementation in Figure 2.

This implementation takes eight ICs, not counting those required for testing for all zeros. An advantage gained by this approach is that readily available parts are used throughout, and cycling at a 5-MHz clock rate would yield an equivalent data rate of 20 Mbits/sec.

The software implementation is a straightforward emulation of the hardware implementation of Figure 7. The table is the same as that in Figure 6 for CRC-16. A different generator polynomial would require a different table, but the rest of the routine would be the same.

The software implementation is listed in Figure 8. The routine, including the CRC-16 table, takes up 84 bytes of memory. CRC4BT is called once for each byte of data and executes in 150 µs in a K3870 with a 4 MHz crystal. This is six times as fast as the single shift routine listed in Figure 3, which occupies 42 bytes of memory. The speed improvement realized using the four-bit method permits µCs to play an even more important role in data communications applications, where data rates up to 9600 Baud can be readily protected with CRC.

Let's consider some of the variations and alternatives for data protection.

**eight-bit shift algorithm**

We covered the grouping of the basic CRC shift algorithm into four bits at a time. It is also possible to gain additional speed at the expense of memory usage by extending the approach to eight bits. The hardware would use two eight-bit exclusive-OR gates, two eight-bit registers, and a 256X16 ROM.

Figure 10 lists the software routine for implementing the eight-bit approach. The 256X16 table is built by first continuing the symbol shift procedure, outlined in Figure 5, until the eighth shift. This produces the following list after eighth shift:

F(7)
F(6)
F(5).XOR.F(7)
F(4).XOR.F(6)
F(3).XOR.F(5)
F(2).XOR.F(4)
F(1).XOR.F(3)
F(0).XOR.F(2)
F(1).XOR.C(15)
F(0).XOR.C(14)
C(13)
C(12)
C(11)
C(10)
C(09)
F(7).XOR.C(08)

Then, as before, the next step is to build the generator expressions for the F functions in terms of the T functions as follows:

\[
\begin{align*}
F(0) &= T(0) \text{ where } T(i) = l(i).XOR.C(i) \\
F(1) &= T(1).XOR.T(0) \\
F(6) &= T(6).XOR.T(5).XOR.T(4).XOR.T(3).XOR.T(2).XOR.T(1).XOR.T(0) \\
F(7) &= T(7).XOR.T(6).XOR.T(5).XOR.T(4).XOR.T(3).XOR.T(2).XOR.T(1).XOR.T(0) \\
F(5).XOR.F(7) &= T(7).XOR.T(6) \\
F(4).XOR.F(6) &= T(6).XOR.T(5) \\
F(3).XOR.F(5) &= T(5).XOR.T(4) \\
F(2).XOR.F(4) &= T(4).XOR.T(3) \\
F(1).XOR.F(3) &= T(3).XOR.T(2) \\
F(0).XOR.F(2) &= T(2).XOR.T(1)
\end{align*}
\]

The table is generated by computing parity over the address, as indicated in the above expressions, letting each T term refer to the corresponding table address bit, (assuming the table base address to be zero). The C terms without coefficients in the list are assumed to have zero entries in the table, and so the corresponding column in the table would be filled with zeros.

The eight-bit routine shown in Figure 10 executes in an average of about 82 µs/byte, or about 45% faster than the four-bit method. Memory usage for the eight bit routine plus one look-up table is 568 bytes.

**LRC**

LRC, Longitudinal Redundancy Code, is a special case of CRC where the particular polynomial chosen results in the same CRC code as would be obtained by doing a 16-bit wide exclusive-OR once every 16 bits. If the data stream were represented as a succession of 16-bit words, the LRC code added to the end of the stream would equal the first word exclusive-ORed with the second, exclusive-ORed with the third, and so on. When the check is made at the receiver, the result is zero if no errors occurred, since the exclusive-OR of anything with itself is zero.

LRC is also often done on an eight-bit word length, since software implementation is a little bit simpler than with sixteen bits. LRC, a form of CRC, can be handled by the CRC implementations discussed in this article. The polynomial for LRC-16 is X(16)+1; and that for LRC-8 is X(8)+1. A table for LRC-16 in the four-bit implementation of section 2 could be constructed in the same way as the table for CRC-16 was done. The result is in Figure 9.

**checksum**

The checksum — an accumulation of the remainder of modulo 256 addition of a string of data organized in bytes — is a method of error detection in widespread use throughout the µC industry since it is easily-generated and is very effective in detecting errors. Often, in the case of data which is coded into ASCII characters that represent the data in hexadecimal form, the checksum is taken over the values of the hex numbers rather than over the actual bit patterns themselves.

Typically, the initial value of the eight-bit checksum is minus one. This is so that when zero occurs often in the data, the effectiveness of the code is not diminished. Thus, when the checksum has been taken over received data, the final value is minus one — not zero.
The Only Midwest Conference and Exhibition Devoted Exclusively to Test Instrument and ATE Technology

Leaders in the ATE and test industry will focus on the technology and management involved with the application and use of INSTRUMENTS and ATE in testing COMPONENTS, SYSTEMS and SUBASSEMBLIES.

A four-day technical program of specialized courses, workshops and invited papers will address the following problem areas:

**EFFECTIVE MANAGEMENT OF TEST RESOURCES**
Paul J. Giordano, Chief Executive Officer
Giordano Associates, Inc.

**FUNCTIONAL BURN-IN TESTING: TRADE OFFS AND SOLUTIONS**
Bob Scholl, Engineering Manager
Eaton-Pacific Reliability
Jerry Koran, Special Projects Manager
Eaton-Pacific Reliability

**EVALUATING ATE TO ACHIEVE COST EFFECTIVE TESTING**
Al Cota, Department Chief
Circuit Pack Testing, Western Electric Co.

**COMPONENT FUNCTIONAL TESTING**
John J. Theodore, Senior Research Engineer,
Lockheed Missile and Space

**UNDERSTANDING AND EFFECTIVELY USING TODAY'S NEW BREED OF TEST INSTRUMENTS**
Stan Kubota, Vice President
Interface Technology

**ATE: HOW TO SELECT IT — APPLY IT — MANAGE IT**
Arnold Greenspan, President
AMG Associates
Ralph P. Anderson, Product Line Manager
GenRad, Inc.

**INTRODUCTION TO DIGITAL TESTING**
Lutz P. Henckels, Ph.D., President
HHB, Inc.
René Haas, Executive Vice-President,
HHB, Inc.
Andrew Herman, Director of Testing Engineering Institute,
HHB, Inc.

**ADVANCED ATE TECHNOLOGY AND MANAGEMENT**
Philip C. Jackson, President
Giordano Associates
Paul J. Giordano, Chief Executive Officer,
Giordano Associates, Inc.

**ATE SOFTWARE TUTORIAL — DEFINITIONS, STRATEGIES, LANGUAGES, APPLICATIONS**
Damon C. Hart, President,
Lexico Enterprises, Inc.
Roger L. Williams, General Manager,
Allocations Support Division, Lexico Enterprises, Inc.
The Exhibit is devoted exclusively to manual and automated test and measurement equipment and services

**TEST AND MEASUREMENT INSTRUMENTS**
- Hand Held Instruments — from DVM’s to Logic Probes
- Microprocessor Troubleshooting and Development Tools
- Automatic Measuring Instruments — meters, generators, analyzers, scopes, counters
- Field, Depot and Maintenance Testers
- Instrument Controllers
- Calibration Instruments

**ATE EQUIPMENT/SERVICES/SOFTWARE**
- Handlers
- IC Testers
- VLSI Testers
- Memory Testers
- Microprocessor Testers
- System Testers
- In-Circuit Testers
- Bare Board Testers
- PCB Assembly Testers
- Burn-In/Temperature Cycling Systems
- Cable/Wiring/Harness Testers
- Compilers/Translators
- Test Services
- Software Packages
- Interfaces

**List of Exhibitors as of May 29, 1981**

- ACOC ELECTRONICS
- A.D. DATA
- ADDISON DIV. OF MUIRHEAD
- AEROTRONIC ASSOCIATES
- AMERICAN ELECTRODATA
- ANALOG DEVICES
- AUTOMATIC SYSTEMS
- DEVELOPERS
- ATE SYSTEMS
- AUTAE SYSTEMS
- B&K PRECISION/DYNASCAN
- CARLTON INDUSTRIES
- CHATSWORTH DATA
- CLARKE-HESS
- COMPIC
- COMPUTER CONSOLES/RLG
- COMPUTER AUTOMATION
- CONTROL
- DAYMARC
- DIT-MCO INTERNATIONAL
- DRANETZ ENGINEERING LABORATORIES
- DYTEC/CENTRAL
- EAGLE TEST SYSTEMS
- ELECTRO-MECHANICAL SYSTEMS
- ELECTRO SCIENTIFIC INDUSTRIES
- ELECTRONIC SYSTEMS and PROGRAMMING
- EVERETT/CHARLES TEST EQUIPMENT
- FAIRCHILD TEST SYSTEMS GROUP
- FLUKE AUTOMATED SYSTEMS
- FTS SYSTEMS
- GENRAD
- GLOBAL SPECIALTIES
- HAMEG
- HUNTRON INSTRUMENTS
- INSTRUMENTATION
- ENGINEERING
- INTERFACE TECHNOLOGY
- INTERSTATE ELECTRONICS
- KEITHLEY INSTRUMENTS
- LOGICAL SOLUTIONS
- LUTHER & MAELZER
- MARTIN MARIETTA
- AEROSPACE
- MICRO COMPONENT TECHNOLOGY
- MICRO CONTROL
- NORLAND
- OSTBY & BARTON
- PIER ELECTRONICS
- PLANTRONICS/ZEHNTEL
- POINMASTER
- PRACTICAL TECHNOLOGY
- PRAGMATIC DESIGNS
- PYLON
- Q CORP.
- RACAL-DANA
- ROD-L ELECTRONICS
- SENSITEK
- SIEMENS
- SINCLAIR ELECTRONICS
- SOLARTRON INSTR. GROUP
- SYSTRON-DONNER
- T&B/CABLESCAN
- TEST ENGINEERING SOLUTIONS
- TEST SYSTEMS
- THERMONICS
- TRACE INSTRUMENTS
- UTI
- VERSATILE INTEGRATED MODULES
- VIRGINIA PANEL
- ZIATECH

Produced by *Electronics Test* and co-sponsored by *Circuits Manufacturing, Digital Design*, and *Design Engineering* Magazines.

**For more information contact**
Dona Atwood, *Electronics Test & Measurement Conference*, 1050 Commonwealth Ave., Boston, MA 02215
(617) 232-5470.

**Electronics Test & Measurement Conference**

Please send me more information on the *Electronics Test & Measurement Conference* at the Hyatt Regency Chicago, Chicago, IL, October 5-8, 1981.

[ ] Attending  [ ] Exhibiting

Name ____________________________

Title ____________________________

Company _________________________

Address/Mailstop __________________

City __________ State ________ Zip __________

Phone ____________________________

PDP-11 Cross-Compiler Remedies
"Brute-Force" µP Software Development

Now you can harness the power of your DEC minicomputer for Intel 8086 µP software development. PasPort is a cross-compiler developed by Intermetrics, Inc. that eliminates the need for "brute-force" software development. Rather than muscling out programs with multiple Microprocessor Development Systems (MDSs), PasPort allows you to develop software on any PDP-11 minicomputer systems running under UNIX or RSX-11M operating systems.

According to Ron Kole, manager of Intermetrics' Software Products Division, most developers have access to corporate mainframes or laboratory minis. By using them for software development, relying on an MDS only for final testing and integration, companies can save the price of several MDSs—quite a savings, considering MDSs cost from $15K to $25K each.

PasPort uses Pascal language conforming to the International Standards Organization (ISO) proposal. It supports comprehensive diagnostic capabilities, via an interpretive language, allowing the user to test application software on the host before sending it on to the MDS. This allows use of the many tools inherent in PDP-11 systems, including file management, source control systems, archives, large disks and high-speed printers. In addition, running PasPort on a multi-user host allows sharing of files and procedures; separately compiled routines can then interact via parameter passing or through global data areas.

PasPort consists of three segments: Compilation, Host Run-Time Support, and Target Run-Time Support.

**compilation**
Compilation is essentially an error-checking process. The idea is to take the original Pascal algorithm created by the developer and translate it into a lower level, so that it can run on the PDP-11. First, the compilation process checks for syntactic errors (illegal sentences and punctuation) and semantic errors (sentences that don't make sense), creating error messages to indicate where in the program the errors are. In addition, it lets the developer know if there are any variables he hasn't used, or if a variable hasn't been given a value. If the program checks out, the compiler then converts it to intermediate language, which is an object representation for a virtual machine; this intermediate form is similar, but more compact, then the standard P-code. PasPort compilation rates commonly reach 2000 to 3000 lines per minute.

**host run-time support**
The next step is to run the program on the PDP-11 "in an environment that is hostile to your program," as Kole puts it. "If you attempt to do anything in that program in any way fishy or illegal, you'd sure like to know about it, and that's the whole point of running it on the host," he explains. "Traditionally, this was done on the MDS, but it's very difficult, while you're running on the actual hardware, to get a lot of checking going on."

In addition to automatic dynamic checking, other run-time diagnostic features are available as options. A "profiler" records which source lines executed and how many times they were executed, so the developer knows which program paths have been tested. Also produced is an estimate of how much execution time each source statement required, revealing which
compatible Multifunction Controllers Deliver Backplane Breathing Room

The design freedom one extra card slot provides system designers can be price-
less, often saving considerable design time, hardware expense (expansion
chassis and bus repeaters), and aspirin. One indication of how valuable that
space is will be provided by the sales
figures for multifunction controller
boards introduced by Spectra Logic and
National Semiconductor.

Spectra Logic's Spectra 20 and
Spectra 21 handle removable pack or
Winchester SMD disk drives and start/stop or streaming half-inch tape drives
simultaneously, all on one board. Both
models attach up to four SMD disk
drives and up to eight formatted tape
drives without modifying the operating
system software. Spectra 20 is for Data
General Nova and Eclipse users, and
has been available since May; Spectra
21 is geared to DEC PDP-11 users, and
should be available this month.

National Semiconductor's Hexacon controls three peripheral subsystems:
disk, tape and a fixed-head-disk emu-
lator they've introduced, called
NURAM. Aggregate device transfer
rate exceeds 2 MB/sec for up to four
CDC 9762-type 67-MB disk drives, up
to four Cipher Microstreamer tape
drives (start/stop or streaming) and up
to 8 MB of NURAM auxiliary memory.
Hexacon works on any DEC
UNIBUS system and is compatible
with DEC operating systems. Production
shipments are slated for Septem-
ber; NURAM production shipment
should begin in October.

Each company uses a different
design approach for its controller and,
not surprisingly, each believes its ap-
proach is the only approach. One major
difference between the two boards is
that Spectra Logic uses two μPs, with a
larger total chip count, and National
Semiconductor uses one. As Jim
Anderson, National Semiconductor
staff engineer, puts it: "They (Spectra
Logic) have a separate microengine for
the tape unit. Tape units typically spend
20 to 22 hours a day not being used.
That portion of their logic is wasted

by Bob Hirshon

Intermetrics, Inc, 733 Concord Ave,
Cambridge, MA 02138. Circle 199.

Multifunction controller boards, manufactured by National Semiconductor and Spectra Logic (above) handle multiple peripheral subsystems, but use up only one card slot.
during those periods of the day. We wanted to be able to use that same expense more efficiently, and we believe we got a better plan for being able to take the logic we invested in and spread it across three peripherals.’’

Spectra Logic, however, believes that the one µP approach has its drawbacks: ‘‘It’s the opinion of our engineers,’’ says Steve Roberts, Spectra Logic Executive Vice President, ‘‘that they (National Semiconductor) really had to cut so many corners that there’s no way they can do all those functions with just one µP.’’

‘‘We do it successfully,’’ counters Bill LeDuc, National Semiconductor Product Marketing Manager, ‘‘so what he (Roberts) thinks really isn’t too material.’’ LeDuc did add, ‘‘We were a little bit concerned as far as handling all three functions — whether or not we could get down the UNIBUS as rapidly as we hoped — and it far, far exceeded our expectations.’’

‘‘We may be in for a surprise,’’ says Roberts, ‘‘but our engineers believe that with four levels of interrupts going into one µP, there’s absolutely no way that that can keep the disk, the tape, the UNIBUS and that NURAM thing all going at one time without jeopardizing and sacrificing a tremendous amount of performance.’’

‘‘If you take their approach, that’s true,’’ answers LeDuc, ‘‘but we think it’s the other way around: we think they’re going to have a helluva time making theirs work with some high speed peripherals. This is my own impression, but the two microengine approach can lend itself to some arbitration problems between the two microengines — which one is going to have access to the UNIBUS — and when you start making that coordination between the two microengines — which one’s going to transfer — somebody’s clock has got to slow down.’’

‘‘I don’t think there’s any point that can be made there,’’ states Roberts, ‘‘we’re shipping the Data General one, so there’s no question but that it works and that it streams and does everything else.’’

On paper, Spectra Logic has the edge in transfer rate and also supports eight tape drives to National Semiconductor’s four. In addition, Spectra Logic makes both Data General and DEC models. However, National Semiconductor has the advantage of being able to handle their high-speed bulk NURAM memory, and also has a larger buffer than Spectra Logic’s. But the real test for the two controllers will be in the field, where reliability and maintenance of recorded specs will tell the story. And that’s the test by which both companies say they’re eager to be judged.

by Bob Hirshon
National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051.

Spectra Logic Corp., 2316 Walsh Ave, Santa Clara, CA 95051.

COMPAT Design is a new Digital Design department featuring the latest in computer compatible technology. Each month, COMPAT Design brings you the nuts and bolts of new hardware and software products, and the views of the engineers who designed them.
Manufacturers of Electronic Components, Systems, Subsystems and Test Instruments

AN UNPARALLELED OPPORTUNITY TO SELL YOUR PRODUCTS IN THE FAR EAST

ANNOUNCING...

DATA and TELECOMMUNICATIONS

20-23 January 1982
Harumi Exhibition Center — New Hall
Tokyo Japan

The telecommunications market in Japan is huge, conservatively estimated at $47.7 billion over a ten-year period. With bilateral government agreement for competitive bidding in Japan now a reality, the way has been opened for international manufacturers to supply a large part of Japan's estimated US $3.4 billion initial need for communications equipment and technology.

This exposition is designed to provide sales opportunities in this newly-opened market for suppliers in the United States, Europe, the United Kingdom, Southeast Asia and elsewhere . . . as well as to establish a convenient forum for Japanese manufacturers who already serve the market. The exhibition will be augmented by a comprehensive technical program.

FOR DETAILS ON EXHIBITING, CONTACT:

In the US
Cahners Exposition Group
222 West Adams St.
Chicago, IL 60606
Phone: (312) 253-4866
Telex: 256148

In Europe
Cahners Exposition Group S.A.
(formerly River Communications S.A.)
David House, Lichfield
Guildford, Surrey GU1 1BZ, England
Phone: Guildford (0483) 38085
Telex: B99466

In Singapore
ISCM, Ltd.
Cahners Exposition Group
D7—4th Floor
International Bldg.
36 Orchard Rd
Singapore 0923
Phone: 235-9465
Telex: R5 25932

In Japan
CfG Japan
(formerly ISCM Japan)
Koito Bldg. 3F
3-4-11 Uchikanda
Chiyoda-ku
Tokyo 101, Japan
Phone: 03-254-6041
Telex: 27290

In Hong Kong
ISCM, Ltd.
Cahners Exposition Group
9/F, Flat C
Wing Cheong Commercial Bldg.
19-23, Jervois St.
Hong Kong
Phone: 5-437715
Telex: 02270 ISCM HX
What's Coming Up
august ’81 editorial emphasis....

COMPAT™ ’81 Show Issue
And Product Directory

This special computer compatible COMPAT issue next month will contain an industry first — the first directory that lists plug-compatible computer products from manufacturers offering compatible products for DEC, Data General, Hewlett-Packard, Perkin-Elmer, IBM, Intel, Motorola and other minicomputer and microcomputer makers. This directory will be saved and referred to for the next 12 months by OEM system designers and integrators whenever they need to compare or specify computer compatible products. No other compatible computer source or directory in existence lists such information. COMPAT is the industry’s first show exclusively devoted to computer compatible products.

Graphic and Alphanumeric Display Terminals

A product showcase will spotlight current graphics and alphanumeric display terminal technology and list terminals of interest to system designers and OEM integrators and builders.

Computer System Power Supplies

This article will present criteria for selecting a power supply that is best suited for a particular application. This power supply report will cover various aspects of recent power supply technology and product choices that include linears and switches, build vs. buy criteria, and related design problems.

Sales Offices

MA, ME, NH, RI & VT: Jeffrey C. Hoopes, National Sales Manager, Jackson Parker, Regional Sales Manager, (617) 232-5470, 1050 Commonwealth Ave., Boston, MA 02215

NO, CA, OR & WA: Neal W. Manning, Western Sales Manager, Deanna D’Zamba, Vernon D. Swart, Jr., (408) 371-9620, Suite 1005, 1901 S. Bascom, Campbell, CA 95008

SOUTHERN CA: Carol Stagg, Regional Sales Manager, Linda Horwitz, Lloyd Clinkenbeard, (213) 981-3300, Suite 1215, 15910 Ventura Blvd., Encino, CA 91436

NYC, L.I. & CT: Jack Flynn, (203) 673-0300, The Flynn Group, P.O. Box 675, Avon, CT 06001

MID-ATLANTIC STATES: Warren Smith, (201) 221-0184, The Flynn Group, P.O. Box 754, Bernardsville, NJ 07924

SOUTHEASTERN STATES: E. Harold Mitchell, (404) 634-7070, The Flynn Group, P.O. Box 13611, Atlanta, GA 30324

OHIO VALLEY: Doug Horst, (313) 476-3757, The Flynn Group, 27333 Bramwell, Farmington Hills, MI 48018

MID-WESTERN STATES: David Kingswill, Ed Kruckowski, (312) 774-9660, The Flynn Group, 5526 N. Elston Ave., Chicago, IL 60630

SOUTHWESTERN STATES: Jerry Ambroze, (713) 780-3326, The Flynn Group, 2168 Augusta, Houston, TX 77057

JAPAN: K. Yanagihara, (03) 350-0272, 10-10 Shinjuku 3-chome, Shinjuku, Tokyo, 160, Cable Address: Yanacour, Tokyo

Circle 53 on Reader Inquiry Card

Circle 54 on Reader Inquiry Card
ATE SEMINAR/EXHIBIT
Automated Testing for Electronics Manufacturing

JUNE 14 - 17, 1982, JOHN B. HYNES VETERANS AUDITORIUM, BOSTON, MA

We invite technical papers on these subjects for presentation in General Sessions and Workshops:

- Field Testing
- Bare-Board Testing
- Loaded Board Functional and In-Circuit Testing
- LSI Board Test
- LSI Component Test
- Digital Diagnostics
- Microprocessor Bus Fault Isolation
- Analog Board Test
- Analog Diagnostics
- Bubble Memory Testing
- Burn-In/Temperature Cycling
- Logic Analysis Techniques
- Waveform Analysis
- Electro-Optic Testing
- Test Requirements Analysis
- Interfacing Devices
- Simulation
- Automatic Test Generation
- Systems Support Management
- ATE Management
- ATE Acquisition
- Testability
- Economics of Loaded Board Testing
- Using IEEE Bus Instruments
- Signature Analysis

Abstract Deadline: September 15, 1981

Abstract Submission Form

Please attach this form with your abstract or paper idea.

Name ____________________________
Title ____________________________
Company _________________________
Address __________________________
City ___________________ State ______ Zip ______
Phone No. (________) _______ ext. ______
PAPER SUBJECT ________________________

Please complete one: Abstract attached _______________________ Abstract to come by ______________________

Send abstracts (200 - 500 words) and short biographies by September 15, 1981 to Mary Habosian, ATE Seminar/Exhibit, c/o Benwill Publishing Corp., 1050 Commonwealth Ave., Boston, MA 02215. Or call: (617) 232-5470.

Produced by Electronics Test and cosponsored by Circuits Manufacturing, Digital Design and Design Engineering magazines.

JULY 1981 Digital Design 95
Glare Screen Provides Cure For Terminal Eyestrain

Every occupation has its hazard, from writer’s cramp to tennis elbow — not to mention the newly-diagnosed "Space Invaders wrist" (reported in a recent issue of the New England Journal of Medicine). For video display terminal (VDT) operators, eyestrain is the ailment, and several display phenomena (flicker, radiation, and glare among them) currently receive blame for the problem.

Undoubtedly, surface glare is one major contributor to visual fatigue. Various light sources reflect on the surface of the VDT, distracting the eye of the VDT operator. Eyestrain results because the reflection appears to the observer, to be at whatever distance from the operator the original object occurs. For example, the reflection of a window located ten feet from a VDT screen which is, in turn, located 14 inches from the operator will appear to the operator, to be over ten feet away. As a result, the operator’s eye, when distracted by the reflection, must refocus from 14 inches to ten feet. Constantly refocusing between these disparate points throughout an eight-hour day creates eye fatigue.

Polaroid, which has had some experience dealing with glare, recently announced a circular polarizing filter that "absorbs harsh reflections and glare while improving contrast to make the VDT screen easier to read." according to Dr. Stewart Bennett, General Manager of Polaroid’s Polarizer Division.

The filter traps not only reflections of light sources from around the room, but also ambient room light; eliminating this light results in a higher contrast image.

Inescapably, the CP-70 also filters some light produced by the VDT. According to Bennett, "the observer sees about half the light coming from the screen." However, he’s quick to add, "if the brightness control on the VDT is turned up a bit, the letters are as bright as they are without the filter, although this is usually unnecessary because of the improved contrast."

Polaroid claims their filter is superior to conventional frosted or tinted glare filters because these methods reduce image clarity and don’t completely eliminate glare. Model CP-70 filters come in a variety of sizes and fit on existing terminals via adhesive Velcro fasteners. Unit quantity prices range from $68 to $125.

by Bob Hirshon

Polaroid Corp, Polarizer Div, 1 Upland Rd, Norwood, MA 02062.

Circle 197.
Growth of color displays for small business systems has long been hampered by lack of inexpensive color hard copy. While this is merely one limiting factor in an otherwise booming area, it's an annoying weak link for designers of low cost business systems.

This fall, Integral Data Systems will introduce industry's first answer to the problem: the Model 570 color printer. The Model 570 looks, sounds, feels and basically is just like a Model 560 Paper Tiger printer. But a newly-designed multicolor ribbon system and software package enable the 570 to print in eight colors, producing business graphics with surprisingly high color saturation and quality.

Like color printers from IBM, Ramtek and Trilog, Model 570 works by hammering conventional impact print wires against cyan, magenta, yellow or black ribbons. As with the IBM system, the colors are arranged in parallel, horizontal strips, which the print head accesses by shifting up and down. Like Trilog and Ramtek models, the 570 can mix primary colors to create additional colors (green, violet, orange and brown). And like Ramtek and IBM units, Model 570 makes one pass over each line for each color that the line requires. But unlike any of the above-mentioned printers, the 570 will sell for under $3K, less than a third the price of other impact color printers.

Thanks to the overlapping dots produced by IDS's staggered nine-wire print head, Model 570's image quality equals or exceeds that of the other color printers. Although resolution is only 84 x 84 dots per inch, dot overlap eliminates most of the inter-dot white space, resulting in denser, higher-quality colors.

What you don't get with the 570 is high throughput. As a printer, it sails along at a respectable 150 cps. But multi-colors require multi-passes, and this can slow things down considerably. Plot speed is application-dependent: the more colors per line, the slower the 570 travels. Also, graphics that are more complex on the right side of the paper require more time than graphics that are detailed on the left, since the former requires the print head to travel the entire length of the line more times. Because plot speed is so application dependent, throughput benchmarks are difficult to calculate. To give some idea, however, the business chart (Figure 2) requires about three minutes.

Making the 570 compatible to the many color graphic terminals currently in use was the most difficult design difficulty for IDS engineers to overcome, according to Peter Eisenhauer, IDS Marketing Manager. "The biggest problem we ran into was not so much the implementation of the mechanism," explains Eisenhauer, "but marrying the software with the design and trying to come up with a control scheme for shifting from color to color that was reasonably compatible to the types of color operating systems that are out in the field."

Since it's impossible to develop a software driver compatible with every graphic display on the market, IDS had to select only the more popular offerings. They're developing some software in-house; the rest, they're farming out. "One of the key things in the color marketplace," says Eisenhauer, "will be to identify the key hardware to be involved with. Then we're going to
find the people that are using it, and go to them and say, ‘here’s a color printer we’ll be shipping in the fall. It will be very price competitive in relationship to your color system and, if you want to, it’s yours — go develop a software driver for it.’”

“In one fashion or another,” Eisenhauer concludes, “we will assure that all the key marketplaces have a driver that operates with their system.”

As a printer, the 570 produces correspondence quality print in a 24×9 matrix cell and features six software selectable character sizes, mono or proportional character spacing, programmable horizontal and vertical tabbing, six or eight lines/inch spacing and automatic text justification. Model 570’s print mechanism uses ballistic print heads and is bidirectional, logic seeking.

“Model 570 will be a system-oriented design,” says Eisenhauer.

OEMs designing small business systems will be the primary potential market. According to a recent report by International Data Corporation of Framingham, MA (see Tech Trends, p. 13) the business graphics market will top $1 billion by 1984. The report, titled “Graphics in the Office,” predicts that most of these systems will be color and, furthermore, that the lack of ready availability of color hard copy will be a major factor in either hindering or propelling that trend. IDS’s autumn introduction of the Model 570 will be industry’s first step towards assuring the latter course.

by Bob Hirshon


Smart Storage
Tube Terminal Displays Two Colors

Two of the more imposing drawbacks of Direct View Storage Tube (DVST) displays have traditionally been lack of operator interactivity and lack of colors. Despite DVST’s extremely high resolution, these liabilities have limited the displays’ penetration in many markets. With the introduction of the new 4114 intelligent graphics terminal, however, Tektronix has made dramatic progress in overcoming the first of these problems. And, thanks to the 4114’s two-color option, DVSTs have finally flown the monochromatic pigeonhole.

On-board microprocessing power enables the 4114 to manipulate data locally, without depending on the host computer. RAM capacity that is expandable to 800K bytes further reduces host dependence.

As a result, users can store a group of MOVE and DRAW commands — defining commonly used symbols, codes, background graphics, etc. — and then recall them to the screen as they’re needed, without tying up the CPU. These picture segments can be drawn simply by specifying a segment identifier and a screen location.

In addition, 3000 short vectors of flicker-free refresh capability enables the 4114 to translate, rotate and scale picture segments locally, without erasure or repaint. This two-dimensional transform capability defines picture segments — potentially
quite complex ones — as display cursors, which are manipulated with the 4114’s thumbwheel cursor control.

Another feature made possible by the 4114’s refresh memory is a user-definable dialog area. This enables operators to specify a screen area expressly for scrollable text, so that terminal/host interactions don’t overlap with graphics workspace.

Problems of slow repaint were overcome in the 4114, thanks to the large local RAM. Extremely complex graphics of up to 26,000 short vectors can be erased and redrawn in under 0.5 sec.

The new interactivity capabilities of the 4114 don’t arise from any new technological breakthroughs, according to Mike Kondrat, display terminal Marketing Manager, but simply from increased memory and processing capacity. In fact, before introduction of the 4114, some of the less intelligent terminals were somewhat enhanced by OEMs who built in their own limited refresh memory.

As memory and processing costs come down further, user-interactivity of DVSTs will increase even more. But for now, according to Kondrat, being limited to 3000-vector interactivity isn’t much of a limitation at all. “There are very few applications where users want selectable erase across the whole screen. So, from the applications aspect, the selective erase problem has been solved.”

Unique to the 4114 is a two-color screen that Tektronix refers to as Option 31. Terminals equipped with this option display stored information in conventional green, but display refresh information in orange. For high-density applications, this enables users to distinguish the user-interactive picture area from the stored area.

A two-phosphor mix allows the 4114 to achieve two colors. These two phosphors get excited at different potentials. “You can excite the reddish phosphor,” says Kondrat, “by not giving it enough potential, so it gets just excited enough to emit the red. But if you want to store it, you jack it up a little more in voltage, and that stores it on the screen.”

Other key features of the 4114 include resolution of $4096 \times 4096$ addressable points ($4096 \times 3072$ displayable) and data communications rates of up to 19.2K baud. Options include single and dual flexible disks, up to 512K bytes additional RAM, graphic tablets, a bus extender, and a three-port peripheral interface. Model 4114 sells for $17,500, or $19,500 with color enhanced refresh, in unit quantities (OEM discounts available).

by Bob Hirshon

Tektronix, Inc, PO Box 500, Beaverton, Oregon 97077.

Circle 198.

DEC Compatible Sealed Terminal....

The terminal that defies damp, dirty environments

- Nonventilated (no fans, no filters)
- Fully Gasketed
- NEMA 12 rated structural foam enclosure
- Sealed Membrane Keyboard
- VT 52 or Hazeltine 1420 compatible

Perfect for:
- Plant floor information center
- Operator Workstation
- Shipping and Receiving

xycom™

THE HARDHAT COMPUTER PEOPLE

P.O. Box 984
Ann Arbor, MI 48106
313-429-4971

© 1981 by XYCOM Inc.

Circle 52 on Reader Inquiry Card

JULY 1981 Digital Design 99
EPROM MODULE
Adds 8K Memory To LSI-11
The CCS-1220 EPROM Module provides LSI-11's with 8K words of EPROM type memory using 8 Intel 2716 compatible EPROMS. A R/W switch sets the card in program mode, and disable programming when set in Read-Only mode. It allows programming of any memory location, individually, sequentially, or randomly under software control. Programming software consists of writing to the desired location, and timing out for 50 nsec. $475 with user's manual describing board operation and programming considerations. Control Logic Inc, Nine Tech Circle, Natick, MA 01760. Circle 126

COMPUTER SYSTEMS
Compatible Alternatives To DEC Systems Marketplace
The 34 MAGNUM provides enhanced PDP-11/34 class performance while the 44 MAGNUM is an economic alternative to the PDP-11/44. Standard system configuration consists of a CPU with floating point and memory management, serial console interface, extended memory addressing to 4MB, dual TU58 cartridge tape units including interface, programmable line time clock, bootstrap loader, 8kB cache memory, microcoded ODT and maintenance console. The 34 MAGNUM comes with 256kB of memory, the 44 MAGNUM with 512kB as standard. Other Unibus compatible controllers are optional. They are supported by RSTS/E, RSX-11M and RT11 operating systems. $21,000 for the 34 MAGNUM, $27,000 for the 44 MAGNUM, 60 days ARO. Able Computer, 1751 Langley Ave, Irvine, CA 92714. Circle 129

STATIC 64K RAM
Uses New 100 nsec Chip
The SCP-110, a 64kB IEEE S-100 memory card, uses the 100 nsec Intel 2167 16K static chip. The chip allows memory management functions of offset and protection to be performed with the 8 MHz. 8086 CPU without a wait state. The card performs both 8-bit and 16-bit transfers, switching automatically. The chips are used in a power down mode to minimize current. $1295, OEM qty. discounts available. Seattle Computer Products, 1114 Industry Dr, Seattle, WA 98188. Circle 130

DEC-COMPATIBLE VIDEO TERMINAL
Emulates The VT100 With Advanced Video Option
Model 3100 is designed for users who don't need the powerful editing capabilities of Cobar's 3132 terminal. Standard features include printer port, non-glare screen, 4 video attributes, set up prompt legends, 19,200-baud operation and screen save. $1595, OEM and qty discounts available. Cobar Inc, 1181 North Fountain Way, Anaheim, CA 92806. Circle 132

PACKAGED VOICE TERMINAL
Features Expanded Vocabulary
This fully-integrated voice data input terminal doubles the standard vocabulary from 64 words to 128 words. Model 5300 combines the Model 5000 speech recognition circuit board with the Lear Siegler ADM-5 terminal. The two units are assembled, integrated and fully tested by Heuristics. The final product is a stand-alone, integrated voice input terminal, supplied with a noise-cancelling headset microphone. The terminal can accept either keyboard or voice input, or both simultaneously. $3925. Heuristics Inc, 1285 Hammerwood Ave, Sunnyvale, CA 94086. Circle 127

LXI-11 DISK CONTROLLER
Interfaces Two Shugart, Memorex or Fujitsu Disk Drives
This low cost, single quad size disk controller interfaces DEC LSI-11, 11/2 or 11/23 microcomputers with two each Shugart SA4000, Fujitsu 2301 or 2302, and Memorex 101 or 102 along with other hard disk drives having a Shugart SA4000 type interface. Model DQ401 µP-based controller, is compatible with RT-11 and RSX-11 software. Features include data buffer, automatic media flaw compensation, data error checking, on-board bootstrap and extended memory addressing to 256 KB. $1580. Dilog, 12800-G Garden Grove Blvd, Garden Grove, CA 92643. Circle 146

DUAL TRACE OSCILLOSCOPE
Inexpensive Scope For Floppies
The Scopex 14D-10 has a full 10 X 8 cm display on a flat face tube backed by IC circuitry with switched mode power supplies. Features include 10 MHz plus bandwidth at a Y sensitivity of 2mV/cm on both channels, full X-Y facility, Add and Invert capability, wide range time base with push button selection of trigger modes, Measuring accuracy is 3% on both X and Y axes. Trace locate and probe compensation are included. $699. Intratec, Div. of British Aerospace, Dulles Int'l Airport, Box 17414, Washington, DC 20041. Circle 152
µP-BASED CONTROLLER/DRIVER
For Use With 3, 4 or 5 Phase Stepping Motors

Suitable for OEM applications in automation, robotics and research and development, the MCU-3 provides all the required power supplies to drive a stepping motor, control bus buffering and optical isolation for field connections. Up to 16 MCU-3's can be paralleled on the system control bus, which is directly compatible with most of the 8-bit µP's. Three groups of instructions - initialize, command and read status - provide the flexibility for a wide range of motion control applications. The MCU-3 is $245. Also available is the MDB-6B high speed, high power stepping motor driver for use with 4 phase stepping motors. It is suitable for OEM applications in multi-axis motion controllers. $245. Advanced Control Systems Corp, 213 Centre St, Quincy, MA 02169. Circle 131

TERMINAL SWITCHERS
Manual or Remote Control

This family is fully compatible with WANG, H/P, IBM and DEC equipment. The GBNC-S8 can switch one terminal between 3 or more CPU's or modems. A 3 position switch allows selection of which CPU or modem will be connected to the terminal. The GBNC-S8RC, with remote control, connects 3 terminals to one common CPU port. Each terminal has a small control box which requests a connection to the CPU. Only one terminal is connected while the other two wait until the CPU port becomes available. The GBNC-S8 is $139; the GBNC-S8RC is $298. OEM discounts available. Gittronix Inc, 450 San Antonio Ave, Palo Alto, CA 94306. Circle 141

CONVERSION PACKAGE
For PDP-11 to VAX-11 Assembly Language Conversion

CONFAX runs on both PDP-11 and VAX-11 computers and produces VAX-11 assembler source code in less time than with fewer errors than manual conversion. Editing procedures and a post-processor allow the user to select the desired conversion and eliminate unwanted alternatives. It automatically handles details such as supplying octal radix indicators, translating ASCII literals to VAX-11 format, and substituting standard VAX-11 register names. The conversion process is controlled by tables which can be used to fine tune the conversion for particular programming environments and to produce special conversions (including multi-line) of PDP-11 opcodes, macros, or operands. An initial $1500 fee includes consultation, training and conversion of 500 lines. Additional conversion is $.50/line. Permanent license is $5000. PSI, (Pennington Systems Inc), 65 S. Main St, Pennington, NJ 08534. Circle 138

WINCHESTER STORAGE MODULE
EXORbus Compatible Series

Each configuration of the 9670 series is a complete storage system with one or more drives, an intelligent controller and a power subsystem. Normal configuration includes an 8" Winchester disk drive and an 8" double sided floppy drive. Variations can include any combination of Winchester and 8" floppy disk drives to a max of 4 drives. The storage module controller responds to 10 high level commands and features full sector buffering and burst error correction. The system also supports Enhanced Programmed Data Transfer. The 10MB Winchester/1MB floppy configuration is $5295. Creative Micro Systems, 11642-8 Knott St, Garden Grove, CA 92641. Circle 180

COLOR GRAPHICS TERMINAL
For VT100 Users

The ColorScan-10 has a built-in line ruling set and 8 colors for both foreground and background information. Includes a non-glare 12" screen in either an 80- or 132-column by 24-line format and a detachable type-writer-style keyboard with separate numeric pad. Features split screen, regional scrolling, smooth scrolling and double high/white characters. $3,795. OEM discounts available. Datamedia Corp, 7401 Central Highway, Pennsylvania, NJ 08109. Circle 151

SERIES/1 CONTROLLER FOR IBM 3203-5 LINE-PRINTER

The Computerm Line Printer Controller for the IBM 1403, 3211 and 3203-5 line printers provides complete line printer support with no changes required in the Series/1 system software. The controller is transparent to the host and operates in Cycle Steal and Direct Program Control (DPC) modes. It is completely compatible with the host computer drivers and operating systems through emulation of the Series/1 4973 Printer.

The price of this interface is $2,995.00. OEM and quantity discounts available, 90 days ARO. Computerm Corporation, 1670 Golden Mile Highway, Monroeville, PA 15146. (412) 925-1344. Circle 56 on Reader Inquiry Card

Circle 74 on Reader Inquiry Card

JULY 1981 Digital Design 101
INTERACTIVE TERMINAL

Supported by SDRC Graphics System

The Series II features a high contrast vector display with 2048 X 2048 addressability and built-in firmware for fast, dynamic interaction. Used with SDRC SUPERTAB, it simplifies finite element pre-processing because menus and segmented pictures stored in the terminal improve response time. Using a light pen or data tablet, the Series II supports direct interaction with the geometric model and finite element mesh. SDRC OUTPUT DISPLAY, the supplemental post-processing software, enables designers to visualize analytical results with accurate line drawings or contour plots. Local processing and picture storage permits observation of animated behavior under static and dynamic loads. Series II Graphics Terminal is $15,750. Imac, 150 A St, Needham Heights, MA 02194.

DEVELOPMENT SYSTEM

Provides Full 8-Bit Support

This series of upgradable, entry level development system packages provide complete 8-bit chip hardware and software development capability, upward compatibility with 2302 slave emulation systems and hard-disk-based cluster networks. They support the 8080, 8085, Z80, 6800 and 6802 processors and include CRT, keyboard, selected CPU, 64K of static RAM, in-circuit emulator and logic analyzer in one compact console; plus a 1MB dual-drive, double-density disk and programmers for 2704/2708 and 2716/2732/2732 EPROMs. Each system offers a full complement of hardware and software features, $17,950.

PLOTTING WORK STATION

Offers Remote Graphics Manipulation and Plotting

The 444 supports remote job entry, electrostatic plotting/plotting and graphics manipulation capability — scaling, rotation, mirroring, window-operating system. Components include µP with 64 kB of memory, CRT display, 24 MB disk, and a bipolar algorithmic processor (BAP) to perform vector sorting and raster generation. The system will support any two Versatec printer/plotters in any mix of paper widths. It can generate up to 15 different font styles and create different line styles and widths. The 444 Remote Plotting Work Station is $35,000, 90 days ARO. Versatec, a Xerox Co., 2805 Bowers Ave, Santa Clara, CA 95051.

COMMUNICATION PROCESSOR

Microcomputer System for Datacomm Applications

Designed for data communications requirements using both async and sync communications protocols, the OrangeBox can be used to implement a broad range of terminal and communications controllers, concentrators, and front end devices, using software developed by the user. It is packaged as a stand-alone unit or in a 19" rack mount configuration with 2 to 18 communication interfaces. Low-cost integral modems are available for operation at 2400, 4800 and 9600 bps. It has a Z80-A microcomputer and associated SIO integrated circuits for implementation of communications firmware using EPROMs. The standard Micro30 OrangeBox with 6 RS-232C I/O interfaces is $1500, qty and OEM discounts available. Micom Systems Inc, 9551 Irondale, Chatsworth, CA 91311.
OFFICE/BUSINESS MICROCOMPUTER

Self-Contained, Typewriter-Size System

This stand-alone system contains the µP as well as all other essential components in a single console. The typewriter keyboard has 100 key stations, a numeric pad and 32 function keys. The Microlite II also has a 24-line by 80-character plasma display and houses two 5-1/4" floppy disk drives that can store up to 350,000 characters per disk. An optional dot matrix printer can also be housed in the console. Other options include floppy disk drives with a 500 kB, 8" capacity. Up to 4 drives can be supported. Rigid disk drives with 27/54/208MB removable or 24/40MB Winchester fixed media are available for high speed and larger capacity needs. Letter-quality printing is provided by a separate printer that provides high volume printing.

Q1 Corp, 125 Ricefield Lane, Hauppauge, NY 11787. Circle 189

SERIAL MATRIX PRINTER

No Duty Cycle Limitations

This unit has a 180 cps print speed and up to 136 column output. It can produce data processing as well as correspondence quality characters. In graphics mode it has a resolution of 70 dots/in. on both the vertical and horizontal axes. The printer stores a standard ASCII 96-character set together with an alternate character set in ROM, and a third character set may be downloaded from the host CPU. Other features include bidirectional printing with logic seeking, vertical and horizontal tabbing, up to 6 copies, adjustable form-feed tractors to handle paper widths from 1.5 to 16", options of 10, 12 and 16.5 cpi may be selected at either 6 or 8 lpi, and double-wide and double-density printing. The input buffer can be expanded from 1024 characters to 4096 characters. Foreign or special character sets may be used. The Infoscribe 1000 is $1795, under $1000 in OEM qty. Infoscribe Inc, 2720 S. Croddy Way, Santa Ana, CA 92704. Circle 182

TAPE SYSTEMS INTERFACE

Group 3000 Tape Systems Shared Between HP CPUs

With the SMASH (Shared Mass Archive Storage Host) interface, high performance 6250 tape technology can be shared over a network of CPUs, providing the advantages of higher recording density, increased throughput, and access to a larger, expandable, data base. The unit is contained within the cabinet of the Group 3000 tape controller. Switching selection for network CPUs is operator-activated between 2, 3 or 4 HP CPUs. Group 3000 operates at a speed of 125 ips, records at triple density 800/1600/6250 bpi or dual density 1600/6250 bpi. The SMASH unit is from $14,000 to $28,000. Qualex Technology Inc, 6925 Canby Ave, Building 109, Reseda, CA 91335. Circle 190

OUT FRONT

As a distributed graphics processing system

Compare our new VG 33000 graphics system with any other and you'll see why we're out front with features no one else can offer. At a price that's comparable. In fact, there's a lot more to our VG 33000 than meets the eye. There's our distributed graphics library that moves the processing load off the host computer. There's our remote capability, with a synchronous serial line interface, that lets you locate work stations up to a mile away while communicating at rates up to a megabit. You get true 3D with the VG 33000. There are industry standard network protocols, local picture editing, off-line diagnostics, and a geometric shape generator. The VG 33000 has the fastest 3D clip/zoom rate available. All features you won't find on any other system. Plus, the VG 33000 can operate as a stand-alone system without host computer involvement to save you valuable computer time.

Our VG 33000 is so far out front in state-of-the-art technology, it has no competition. Find out today how you can be out front.

Call or write:

Vector General, Inc.
More than meets the eye.
21300 Oxnard Street, Woodland Hills, CA 91367
(213) 346-3410 TWX: 910-494-2764

Circle 58 on Reader Inquiry Card
See Us At Siggraph/81, Booth #707

JULY 1981 Digital Design 103
Our new, slower, cheaper array processor.

Our new MSP-3X is only about half as fast as our MSP-3. But at $4950 its price is also less than half that of any other array processor on the market.

"Slower," of course, is relative: MSP-3X lets your PDP-11 computer perform arithmetic and signal analyses 20 to 50 times faster than it can alone. A 1024-point real Fast Fourier Transform in 14.3 milliseconds, for example. That's plenty of speed for most analyses of vibration, sonar, communications, radar, medical image, and dozens of other kinds of data.

And you needn't sacrifice convenience, either. Operation is simple and reliable, based on straightforward execution of an extensive library of functions, accessed through Fortran calls. And MSP-3X's two hex boards simply plug into your PDP-11.

All in all, MSP-3X is a most intelligent trade-off. Write us for detailed specifications.

Computer Design & Applications, Inc.
377 Elliot Street
Newton, MA 02164 (617) 964-4320

Circle 59 on Reader Inquiry Card

Is your system Constipated?

For quick relief, try our Formula 80
(8 Milliseconds access time)

The Alpha Data Model 80 discs are used by our customers to relieve system slow down due to the swapping of software in and out of main memory by their CPU. The Model 80 comes in 1, 2, 4, & 8 megabyte models that can be daisy chained up to eight units per channel.

For further information, call or write:

alpha data
20750 MARILLA STREET, CHATSWORTH, CALIFORNIA 91311
(213) 882-6500

Circle 60 on Reader Inquiry Card

LOGIC ANALYSIS SYSTEM

For Standard 19" Rack Mounting

The rack mounting package allows up to 96 channels of logic analysis for ATE and other system test applications. Five configurations are possible which arise from the package's ability to accept one or two PI-600 series modules so that the user can specify the analysis configuration best suited for his system test application. A keyboard, CRT, and the associated electronics are not required. The analysis system is designed to be incorporated into an IEEE-488 set-up and acts as a LISTENER/TALKER on the bus. The PI-600 rack mounting package is from $6,750 to $14,900. Paratronics Inc., 2140 Bering Dr, San Jose, CA 95131.

Circle 188

PRINTER CONTROLLERS

Give DG Computers Up To 1500 LPM Capability

These controllers, for the Nova and Eclipse, accommodate BDS band printers with speeds of 300, 600, 900 and 1500 lpm. Speed selection is through on-board switches. Both are completely bus and software compatible with the minicomputer. Model DPC 40-DS employs an 8-bit parallel data-transfer bus which handles a full ASCII 96-character set along with vertical format paper-movement instructions. Model DPC 50-DS has a 16-bit parallel input from the computer with an 8-bit parallel output bus to the computer for handshake signals. It has a 256-bit RAM, permitting the
computer to set and clear horizontal tabs in any of 132 positions. Both controllers buffer two data words with transfer rates to 100kB/sec. With controller, printers range from $3250 to $34,400. BDS Corp, 1120 Crane St, Menlo Park, CA 94025. Circle 134

DISK CONTROLLERS
Drive Winchester Market Faster

These two controllers bring Winchester capabilities to the marketplace with less development time and cost to design custom drive controllers. Containing 56 devices, the WD1000 controller board features all necessary buffers, a 5 Mbits/sec transfer rate, and control for up to 4 drives and 8R/W heads. The WD1100’s 5 MSI chips (address mark detector, CRC generator/checker, MFM generator, serial/parallel converter, and parallel/serial converter) take the place of 75 chips to provide an ST500/SA1000 interface. Available in a plastic 20-pin dual-in-line package or a 20-pin ceramic DIP. In quantity 250, the WD1000 board is $395, and the WD1100 chip set is $48. Western Digital Corp, 3128 Red Hill Ave, Newport Beach, CA 92663. Circle 143

MICRO-BASED COMPUTER SYSTEM
Personal Computer for Professionals

The PC-8000 desktop computer houses processor, memory and flexible disk subsystem in a compact keyboard/display unit, available with monochrome or 8 color graphics. It supports multiple operating systems, programming languages and application packages, along with a wide variety of peripheral devices. Uses include data and word processing by professionals and managers in small businesses, and in large corporations as a remote terminal and as a standalone desktop support system. Hardware configuration consists of a Z-80 compatible µP with up to 64 kB RAM plus optional 32 kB ROM. The 12" CRT permits selection of variable screen widths, variable-size U&L case characters, 3 types of viewing—static paging, scrolling and split-screen—graphics, selection of an alternate character set, blinking, inverse video and an operator prompt line. From $1600. NEC Information Systems Inc, 5 Militia Dr, Lexington, MA 02173. Circle 186

The EST Company offers a complete line of pedestal bases and components for stationary or movable stands for terminals or printers. We offer seven styles of 4-leg pedestal bases in sizes from 19” to 34”, and three styles of 5-leg pedestal bases in sizes ranging from 22” to 28” spreads. Our line of uprights and top plates can match your needs for those stands. Let us quote your custom casting needs or work with you on your stand unit design.

EST COMPANY, BOX 25H, GRAFTON, WI 53024 (414) 377-3270 A DIVISION OF LEGGETT & PLATT, INC.

Clifton brushless dc motors work hard for more precise control in Winchester drives.

Compact size
Easy packaging
Better air flow

Low cost
Inexpensive to buy and use

• High torque • High efficiency • High braking torque

Plus, you get:
Better speed control • Fewer moving parts for better reliability
• No arcing—no brush dust • Performance customized to meet your needs

To review your requirements, call
Cárey Walter today at
(215) 622-1000.

...We make it happen with motors

Circle 186 on Reader Inquiry Card

JULY 1981 Digital Design 105
Our 10-year history of creative systems design and fast delivery has built a strong and trusted name in the international marketplace. We'll win you over too. Dial this hotline:

(408) 738-3368

IDS international data services, inc.
1020 Stewart Drive, Sunnyvale, CA 94086
TWX 172-189

Circle 31 on Reader Inquiry Card

SINGLE BOARD COMPUTERS
16-Bit Multibus Compatible
Each of the products conforms to the Multibus standards, including multimaster capability, and are compatible with both 8- and 16-bit peripheral boards. The FT-86C and FT-86M are designed around Intel's 8086. The FT-86C/FP and FT-86M/FP incorporate Intel's 8087 Numeric Data Processor. The FT-68M is designed around Motorola's MC68000. Using the 8086/8087 combination, focus is on 6 OEM and System House application segments: Business Data Processing, Process Control, Numeric Control, Robotics, Graphics, and Data Acquisition. The FT-86M and FT68M are designed for users needing to both support and protect large memory requirements. The FT-86M directly addresses 1MB and supports mapping addresses of 8MB. The Motorola 68000 based FT-68M directly addresses 15MB. The GATEWAY SERIES products, including the

8087 NDP, range from $1,250 to $2,950. Forward Technology Inc., 1440 Koll Circle, Suite 105, San Jose, CA 95112.

Circle 163

DC SERVO MOTORS BROCHURE
For Computer Peripheral and WP Equipment
The Snapper series, permanent-magnet servo motors offer a range of 10 off-the-shelf motor lengths, 2 motor diameters and 8 standard winding options to provide the designer with broad mechanical and performance flexibility. Features include fast accelerations, low clogging, long brush life and rugged construction. The brochure includes a Motor Characteristics chart, notes on communication, conversion tables, diagrams and a list of options. EG&G Torque Systems, 36 Arlington St., Watertown, MA 02172.

Circle 161

COMPUTER SYSTEMS
Expanded DecSystem 10/20 Compatible Product Line
Models F4 and F5 are based on generalized, user-microprogrammable processors which can emulate the Dec-System 10/20 family. They can execute the same instruction set as any of the PDP-10 models and are capable of running the TENEX, TOPS-10, TOPS-20 or other PDP-10 operating systems. Also offered is the language C and the Unix operating system supported by a microcoded architecture. They are equipped with a display based diagnostic µP for remote hardware and software maintenance. With these new additions, the F series covers a performance range from very small (personal) configurations to the fastest PDP-10 compatible machine available. The F5 is from $50-$80,000, the F4 is $200,000. Foonly, 160 S. Whisman Rd, Mountain View, CA 94041.

Circle 162
DESKTOP BUSINESS COMPUTER

Includes Integral 5MB Winchester Disk

System 1500 expands the use of low-cost desktop computers to business applications previously reserved for higher-priced minicomputers. Several applications may be on-line concurrently without changing floppies. An integrated 700 kB double-sided, double-density flexible disk drive is used as backup to the Winchester for program and data transfer via removable flexible diskettes. Eight flexible diskettes can back up the full Winchester capacity. The high speed Winchester disk transfers data at a speed of 5 Mbits/sec. The disk can be configured to appear as one continuous disk with a capacity of 5.2 MB or as two separate 2.5 MB disks. An automatic error correction feature allows the disk controller to automatically correct up to 11 bits per physical sector. The system includes a solid state keyboard with a 60-key typing array and a 13-key adding machine cluster, up to 64 kB RAM, a 12" CRT formatted in 24 lines of 80 characters, an 8 bit Z80 processor and interfaces for communications and printer output. A complete set of accounting and word processing applications software packages are available. $9995. Digilog Business Systems Inc, Babylon Rd, Horsham, PA 19044.

THREE PHASE AC POWER CONTROLLER

VAX Compatible

The MPD-416 is electrically and mechanically interchangeable with the DEC 869 AC power controller and is lower in cost. It distributes 3 phase power in computer, industrial control and electronic test systems. The controller is rated at 240/416 VAC @ 45A (15A per phase) with 6 unswitched and 12 remotely switchable outlets. Standard features include a high performance EMI filter, transient suppressors, magnetic circuit breakers, local-off-remote switch, delayed output for multi-controller sequencing, remote disable, emergency shut down. The MPD-416 is $1300. OEM and qty. discounts available. Marway Products Inc, 2421 S. Birch St, Santa Ana, CA 92707.

EXATRON'S

RS-232C STRINGY/FLOPPY MASS STORAGE SYSTEM.

Mini-disk speed, capacity and reliability for only $349.50.

- Standard RS-232C communications link
- Built-in operating system
- Two file management structures: ASCII and binary
- Three baud rates available: 300, 1200 and 9600
- Busy/ready handshaking supported

Call our HOTLINE...
(800)-538-8559
In California,
Call (408)-737-7111

Circle 64 on Reader Inquiry Card

HIGH RESOLUTION CRTs

P.S.

Switching Power Supplies
open frame, outputs
+5V/4A, -5V/0.5A, +12V/1A
Input 110V AC 60 cycle — others on request

Handwellcorp.

267 Castro Street, Suite 2G
Mountain View, California 94041
Tel: (415) 962-9265 Tlx. 171947 HANDWELL MNTV

Circle 65 on Reader Inquiry Card

JULY 1981 Digital Design 107
SESSION PLAYBACK SOFTWARE

DEC VT100 Compatible

This package runs against session documenting log files produced by the program DOC. The combination of DOC to create a log file of a complete session, together with IMAGE, allows replay of the session back to the screen for subsequent reference and training. The dynamic application run example may be played back one frame at a time for inspection. Also, an accurate mapping may be put out as a printed document. The IMAGE package is $295, may be used with any number of VT100s connected to the system. Clyde Digital Systems, Box 348, Bedford, MA 01730. Circle 149

COLOR GRAPHIC CRT TERMINAL

Wide Variety of Features

The display has 1,920 alphanumeric characters in a 24 line by 80 column format with 720 x 288 graphic resolution. In addition to the full ASCII character set, each unit has 1,280 user defined programmable symbols on a single plane. The keyboard is detached and has 87 keys. There are 8 keys for editing and special functions plus 24 programmable function keys. The user can view two pages of data by horizontal or vertical scrolling. Split screen is standard with up to 4 independently addressable and scrollable screens. The direct access by location into area data bases. One of the features of this architecture is the ability to use the aggregates to store general representations of the information content of their constituent data points. For users of graphic display systems this means that wide area displays showing general features and small area displays showing great detail can be obtained with equal ease from a common data structure. High speed processing of masses of pixels is also possible. It supports simultaneous usage by multiple users and features rapid access rates. The IMS uses the VAX 11/780 as the host processor and may be interfaced to Megatek or any of several others. As a turn-key system with the host computer, all software, peripherals and graphic display, the IMS is $400,000. Interactive Systems Corp, 5500 S. Sycamore, Littleton, CO 80120. Circle 167

NTR COMMUNICATIONS PROTOCOL

For DG Minicomputers

This data communications software allows the NOVA and ECLIPSE to connect to UNIVAC mainframes using the NTR remote job entry protocol. It supports all standard features of the protocol, including multiple I/O streams, a console, full duplex operation, space compression, and extensive remote operator control over output peripherals. It interfaces with RTOS, RDOS and AOS. Any peripheral supported by the operating system may be used for input or output, and each I/O stream is treated independently and can be assigned to different peripherals. Initial CPU license is $2750, discounts for multiple sites or OEM. Gamma Technology Inc, 2452 Embarcadero Way, Palo Alto, CA 94303. Circle 135

PDP-11 WP SOFTWARE

For RSX-11M, -11M-Plus Operating Systems

Under RSX-11M, it runs on PDP-11/23's through 11/70's and can be tailored to the size of the system. It allows running extensive word processing tasks concurrently with data processing. Features include an expanded dictionary of 30,000 words supplied, and 35,000 available for customized applications. WORD-11 is a multi-user, menu-driven system allowing the interactive creation, editing and printing of documents. Written entirely in MACRO-11. A single CPU license for WORD-11 on RSX-11M is $7500 including installation, training and support. Data Processing Design, 181 W. Orangethorpe, Suite F, Placentia, CA 92670. Circle 147
Use "TouchGraphic" Panels As On-Off Switch, Adjustable Vernier And X-Y Controller

Since the TouchGraphic panel processes and outputs information digitally, you can interface it to a computer bus, enabling users to convert serial data outputs to parallel data. In Figure 1, buffer RAMs store data, freeing the computer for other tasks. Then, once RAMs are filled with X-Y data, it quickly retrieves data when necessary or upon request, thus providing optimum utilization of the computer in applications like laser drilling, numeric-controlled systems, computer-controlled medical instrumentation, etc.

Since each system and application is different, TouchGraphic provides flexibility in applying the X-Y data to the system. In computer-controlled systems, you need accurate timing data to determine the relationship of the various signals. In this application, TouchGraphic's panel frame sync output provides this timing signal.

Figure 2 shows how the TouchGraphic panel can provide X-Y data and serve as an on-off switch in applications such as laser beam drilling or E beam systems. In the X-Y mode, the operator draws the finger across the panel to create the desired pattern or to position the cursor. By tapping the panel, he triggers the system to fire or automatically change programs.

TouchGraphic provides extra pulses automatically, so the system can be programmed to detect number of panel taps or pulses sent to indicate the changes which must be made.

For example, in the laser drilling application, it is easy to multiplex the X-Y to position laser number one. Then, by tapping the panel — say twice — you can move on to position the second laser and so on. Or, the tapped input can be processed to move the system into a different mode of operation. This permits the operator to change from gross cursor movements to very fine cursor movements simply by tapping the "light table."

Using the system's clock, the designer sets up the system to determine how rapidly the finger moves across the panel by counting the pulses and speed from point A to point B. Then, by tapping the panel, the system can be reconfigured to permit the user to change from gross to fine movements. Finger movements across the entire four inches of the TouchGraphic panel may result in only four or five data input movements. In this way, very accurate and fine movements can be made even if the finger is very shaky on the panel.

Figure 3 shows how the designer can also use the presence switch detection circuitry in TouchGraphic to provide an adjustable vernier. In this application, TouchGraphic provides direct counts of one on one. Or, it can provide 1/2, 1/4, 1/8... on the X or Y axis. In this application, the operator gets a predetermined movement with a certain number of taps on the panel. Then, by tapping the panel a different number of times, the operator gets another level of movement. Thus, with single-hand operation, users change the resolution of the cursor movement. In this application, the presence detection switch and counters not only detect finger presence but also reformat the pulse count control.

Let's look at some general applications, construction and advantages in greater detail. The TouchGraphic unit replaces trackballs, joysticks, light pens, twin knobs, pushbutton cursors and other controlling devices. It provides smooth, accurate, real-time X-Y control. In applications that involve computer graphics, freehand graphics,
1. X count output shown for left-right finger motion; Y count outputs similar for up-down finger motion. Arbitrary terms left-right, are for reference only.

2. Since a valid output pulse may only occur when frame sync is high, there will be a minimum of about 675 µs between one output pulse and the next. Since there are 15 sensors/inch, internal logic and timing limits the maximum finger velocity which may be sensed at approximately 60"/sec.

3. Presence output and frame sync output are both internally pulled up to V+, and should be connected to a high impedance input (CMOS 4045 or 4050).

4. When a finger touches anywhere on the TouchGraphic surface, there will be a low-going pulse on the presence output. Activated from a minimum of 45 µs for one sensor to a maximum of ≈630 µs for 14 sensors activated. If the length of the TouchGraphic surface covered is greater than 1", 15 or more sensors will be activated disabling all count output pulses (X_L, X_R, Y_U, Y_D), until the number of sensors activated drops to 14 less.

5. All count outputs (X_L, X_R, Y_U, Y_D) are open collector and must be pulled up externally to user's logic level (4.7 kilohms to +5V suggested, V_H cannot exceed +15V).

6. All X and Y count output pulses will be ≈5µs wide, with Y up or down pulses going true ≈7µs after the leading edge of frame sync, and X left or right pulses going true ≈12 µs after the leading edge.
drawing, tracing, digitizing and tracking, it is a far superior and more economical input device. It provides even greater capabilities and flexibility in many applications where previously only a simple positioner was justified. For example, it provides capabilities found individually in a trackball, joystick and light pen. It is a solid-state 2-D positioning and tracking device that produces X-Y positioning signals, as we said, when the finger is moved across its surface. It has no moving parts to break down or wear out, since moving a fingertip across the surface as though rolling an imaginary ball or small thumbwheel permits sensors embedded under the MicroProximity sensing surface to detect the presence, motion and direction of motion. For many applications it provides coarse and fine control of the X-Y movement. It can be wiped up to 60 ips for rapid slewing to a distant position or wiped one step at a time even in high resolution systems.

As the finger moves, proprietary sensing circuitry produces X-right, X-left, Y-up and Y-down output signals on four lines. A fifth output line provides a "presence" signal, indicating fingertip presence on the surface even when stationary. The positioner digital output is TTL- and CMOS-compatible, so it interfaces to computers, microprocessors or digital counters. The surface is compact and virtually indestructible. The entire control mechanism is 4"x4"x1/2". It is rugged and chemical resistant.

**How does it work?**

It is a VSL hybrid system operating on the proprietary high-speed MicroProximity "capacitive" sensing principle. As the fingertip touches and glides across the sensing surface, capacitive coupling causes sequential activation of one or more of 3600 sensors on two axes simultaneously. This information is internally processed to produce an output pulse train, which then provides information on the number of incremental steps and the moving finger's direction.

It is constructed as a block-like multi-laminate of an insulated touch surface, sensor array, circuit carrier board, mounting bezel and back panel. The sensor array and circuit board are connected inside the block. On the circuit board, active elements are wire-bonded chips.

After final test, layers are permanently laminated and sealed to form a self-contained device. It handles high-G forces, wide temperature and climatic ranges, and abuse. Lifespan is several decades.

by the Engineering Staff

**Engineering Staff, TASA, Inc., 2346 Walsh Ave., Santa Clara, CA 95051.**
Fast, low cost printer.

This DC-4004A discharge printer prints 48 columns at 144 cps. Printing alphanumericics in 5 x 7 matrix format on 4.72" paper, its MTBF is 144 million characters. Just 2.6" H x 6.7" W x 5.9" D, it's only $127 in 100 quantity. Other printers with interface electronics available.

Call or write HYCOM, 16841 Armstrong Ave., Irvine, CA 92714 — (714) 557-5252

Circle 66 on Reader Inquiry Card

---

**Filling Up Fast**

Space is filling up fast for our August '81 Computer Compatible Directory. See Sales Listing on page 92 if you haven't placed your ad yet.

---

**MODEL MAP-20S THERMAL PRINTER**

World's smallest complete 20 column alphanumeric panel mount printer. Has RS232C and 20 mA loop interface, is microprocessor controlled, has internal self test program and includes all drive circuits and AC power supply. Weighs 4.2 lbs and occupies 14.8 sq. inches of panel space.

Price $725.00 each and in stock.

Write for color brochure to:

**Memodyne Corporation**
220 Reservoir Street
Needham Heights, MA 02194
(617) 444-7000

Circle 68 on Reader Inquiry Card

---

**Input-Output**

Have you got something to say and no place to say it?

Write us, your comments and suggestions are always welcome.

---

**Advertisers' Index**

Able Computer .................. .53
ADAC .................................. 67
Advanced Electronics Design ...... 41
Alpha Data .......................... 104
Andromeda Systems ................ 32
ATE January '82 ................... 48
ATE June '82, Call for Papers .... 95
ATE Proceedings ................... 69
Beehive International ............ 35
Braegen .............................. 49
Burroughs OEM Marketing ......... 75
California Computer Systems ..... 39
Charles River Data Systems ...... 27
Clary ................................. 52
Clifton Precision Div. ............... 105
Comdesign ........................ 13
Compat '81 Pre-registration Form .. 43,44
Comp 81 .............................. 56,57
Compumart ........................ 72
Compumation ....................... 18
Compumetr ........................ 101
Computer Design & Applications .. 10,104
Comtal, Sub. of 3M ................ 73
Controlled Power .................. C-3
Corvus Systems .................... 1
Data Electronic Devices (Data Ed) 14
Datafusion .......................... 4
Data-MATE ......................... 72
Data & Telecommunication Japan '82 91
Dataram ............................ 9
DeAnza ............................. 80
Digi-Power .......................... 85
Digital Communications Assoc ...... 76
Distributed Logic (Dilog) ....... 61
Dolch Logic Instruments ........... C-4
Dynabyte, Industrial ................ 30
Eaton ................................. 60
Electronics Test & Measurement Conference '81 86,87
Electro Design ..................... 101
EST Div., Leggett & Platt .......... 105
Exatron .............................. 107
Factory Management Systems .... 16,17
FOC '81 .............................. 90
Forth ................................. 25
Grinnell Systems ................... 2
G.R. Electronics .................. 33
Handwell ........................... 107
Howard Johnson's ................ 102
Hycom ............................... 112
Imperial Technology ............... 48
Information Products System ...... 31
Interdesign ......................... 39

International Data Services .......... 106
Kennedy ................................ C-2
Marway Products ................... 15
Memodyne .......................... 112
National Instruments .............. 71
North Atlantic Industries .......... 6
Pacific Digital Systems .......... 92
Plessey Peripheral Systems ....... 5
Rockwell International, Autonetics Div. 29
Andrew Rubel & Associates ........ 92
Scherer's Mini Computer Mart ...... 33
Selanar ............................. 98
Sigma Sales ........................ 21
Spatial Data Systems ............. 70
Texas Instruments ................ 47
(Semiconductor Group) .............
Tropel Div., Coherent .............. 37
Vector General ..................... 103
WESPERCORP Div. .................
Western Peripherals ............... 7
Zycom ................................ 99
Xylogics ............................ 51
Zendex ............................. 112

---

112 Digital Design JULY 1981