SiS Flexible Design Solutions

SiSM661MX/648MX/963
Pentium M Architecture Chipset

Silicon Integrated Systems Corp.
Integrated Product Division
Dec, 2003
Agenda

- SiS roadmap update
- Chipset introduction
<table>
<thead>
<tr>
<th>Mass Production</th>
<th>Q1’04</th>
<th>Q2’04</th>
<th>Q3’04</th>
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<tr>
<td>648MX, Pentium M</td>
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<td>DDR400, AGP8X</td>
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<td>M661MX, Pentium M</td>
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<td>M652, Pentium M</td>
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<td>Real256 GPU</td>
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<tr>
<td>MP: Now</td>
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</table>
Chipset Introduction

- SiS Integrated Product History
- SiSM661MX/SiS648MX Family w/ SiS963 Block Diagram
- Feature List
- Performance Analysis
- S/W Information
- SiS Technology
- Schedule Information
- Third Party Information
## Integration and Graphics Chipset

<table>
<thead>
<tr>
<th>Year</th>
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### SiS 300
- 64-bit 2D/3D Engine
- 64-bit Memory Bus
- MCLK: 133MHz
- MP: Now

### SiS 305
- 128-bit 2D/3D Engine
- 64-bit Memory Bus
- MCLK: 125MHz
- MP: Now

### SiS 315
- 256 bit New 3D Engine
- 128/64 bit Memory Bus
- 2’nd Gen. T&L engine
- Hyper FSAA
- Dx8 Compatible
- MCLK: 166MHz
- MP: Now

### SiS 630S 730S
- 3DMark 2001 > 900
- 3D WB > 25 FPS

### SiS 650/651 740 M652
- 3DMark 2001 > 1300
- 3D WB > 37 FPS
- MP: Now

### SiS 661 M661 M661FX 3DMark 2001 > 2200
- 3D WB
SiSM661MX/963 System Architecture

Pentium M CPU

DDR400/DDR333/DDR266
2 DIMM Unbuffered DDR400 Support
3 DIMM Unbuffered DDR333 Support
Max. 1GB per DIMM

1GB/sec Bi-directional 16 bit data bus

MuTIOL®1G

IEEE 1394a

V.90 Modem

AC3 Digital Out
Analog 6 Chann

AC'97

MII

LPC ROM
(Optional)

PHY

PHY

10Mb HPNA

10/100Mb LAN

EC

Joystick

LPC S/IO

BIOS

Legacy

MID 1

Keyboard

RAG

6 USB 2.0/1.1
6 PCI Master

SIS963

SIS302LV

CRT

Dual View

Dual IDE

ATA133/100/66

SIS M661MX

2 x 12-bit
Or
1 x 24-bit
Host Interface
- Support Intel Pentium M Hyper Threading CPU
- FSB 533/400MHZ w/ 2X Address and 4X Data Rate
- 12 Outstanding Transactions support
- Quasi-Synchronous/Asynchronous Host/DRAM Timing support
- Support 2M/4M/8M/16M TSEG SMRAM
- Support Dynamic Bus Inversion.

DRAM Controller
- DDR400/DDR333/DDR266 Support
- Support Up to 2 un-buffered DIMMs DDR400
- Support Up to 3 un-buffered DIMMs DDR333/266
- Up to 1GB per DIMM with 512Mb tech.
- Dynamic Clock Enable (CKE) control placing the Memory into Suspend to DRAM state.

AGP3.5 and AGP2.0 Compliant
- 8X/4X Mode Support
- Fast Write Support
- Support 1.5V interface only

SiS MuTIOL Technology Delivering 1GB/sec Bandwidth
**SiSM661MX VGA Key Feature**

**DX9 S/W Compliant**

**High performance 256Bit 3D/128Bit 2D Graphic Engine**
- 2 pixel rendering pipelines and 4 texture units per cycle (2P4T)
- Up to **200 MHz** ECLK

**SiS Ultra-AGPII™ Technology w/ up to 3.2GB/s Data Transfer Rate**
- Successor of Ultra-AGPII™ Technology and double the bandwidth up to 3.2GB/s with DDR400
- AGP8X equivalent bandwidth for 3D/2D/Video

**Advanced Hardware Acceleration for DVD playback**

**Share Memory Size 32MB and 64MB**

**Dual 12-bit DDR Digital Interface for Digital LCD/TV-OUT support**
- NTSC/PAL TV-OUT
- DVI LCD Monitor
- Dual view function support for LCD-TV, LCD-CRT or CRT-TV

**Built-in high performance 333MHz RAMDAC**

**Graphic support mode**
- CRT highest resolution mode: 2048x1536x32@75NI
- LCD highest resolution mode: 1600x1200x32@60NI
USB 2.0/1.1 Support
- Integrated Two Independent Open HCI Controllers includes Root Hub w/ two USB 1 ports each
- Integrated One EHCI Controller includes Root Hub w/ six USB 2.0 ports
- Support a maximum of 6 USB Ports. Dynamic connection to USB 1.1 or USB 2.0.

IDE Controller
- Dual Independent IDE Channels with ATA133/100/66 support

Integrated MAC Controller with Standard MII Interface

Integrated Audio Controller w/ AC97 2.2 Compliance Interface
- Support 5.1 channel of Audio output and V.90 HSP Modem
- Support 4 Separate SDATAIN Pins for 3 x 2 ch Audio Codec + 1 Modem Codec

3 ports IEEE 1394a

PCI 2.2 Compliant
- Support up to 6 PCI Masters

LPC Interface 1.0 Compliance

ACPI 1.0b Compliance

I/O APIC Support

PC2001 Compliance

SiS MuTIOL Technology Delivering 1GB/sec Bandwidth
Support Intel CPU Speed Step Technology
Advanced Power Management ACPI 1.0b Compliance

Sleeping States
– S0: Normal Run
– S1: Internal CPU Clock Stop
– S3: Suspend-To-DRAM
– S4: Suspend-To-HDD
– S5: System Power Off

Processor Power States
– C0, C1, C2, C3, C4

Wake up Events
– Power Button
– USB Keyboard/Mouse/Devices
– Ring In
– PME#
– RTC Alarm
– MAC
– Audio
### M661MX/648MX/M652 Feature Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>M661MX</th>
<th>648MX</th>
<th>M652</th>
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<tr>
<td>South Bridge</td>
<td>963</td>
<td>963</td>
<td>962</td>
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<tr>
<td>FSB</td>
<td>533/400</td>
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<td>DRAM</td>
<td>DDR400</td>
<td>DDR400</td>
<td>DDR333</td>
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<td>AGP</td>
<td>8X/3.5</td>
<td>8X/3.5</td>
<td>4X/3.0</td>
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<tr>
<td>Gfx</td>
<td>Real256E</td>
<td>No</td>
<td>Real256</td>
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<tr>
<td>DirectX</td>
<td>DX9 SW compliant</td>
<td>NA</td>
<td>DX7</td>
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</table>

PS: M661MX/648MX are Pin Compatible
SiS Technology Advantage

- SiS HyperStreaming Technology
- SiS Ultra-AGPII TM Advantage
SiS HyperStreaming Technology

- HyperStreaming Architecture
- Performance Advantages
What is HyperStreaming Technology?

“HyperStreaming” Makes Streams of Data Flow All Over the Paths with More

- Efficiently
- Concurrently
- Smoothly
- Intelligently

Optimizing System for

- “Low Latency” with Single Stream
- “Pipelining” and “Concurrent Execution” with Multiple Stream
- “Prioritized Channel” with Specific Stream
- “Smart Flow Control” and “Intelligent Arbitration” with Smart Stream
HyperStreaming Architecture

- Smart Arbitration
- Split Transaction
- Pipelining
- Concurrent Exec.
- MuTIOL® 1G

AGP8X 2 GB

FSB800 HyperThreading 6.4 GB/s

1GB/s

CFast Transaction

Audio USB2 MAC ATA133 ...

1.2GB/s

DDR400/DDR333 (PC3200/PC2700)

HyperStreaming Architecture

HyperStreaming Links Fast Together
Split Transaction:

Bus occupied until “Response” is returned. Bus can not be released until the request and response phase completed.

Bus released after “Request” phase and Bus can be used by next transaction (either request or response), then be occupied while the response is return. The Bus utilization is better.
Pipelining Transaction:

Transaction in four steps:
- A1: Instruction Fetch
- A2: Instruction Decode
- A3: Fetch Data
- A4: Execution

Transaction 2
- A1 A2 A3 A4

Transaction 1
- A1 A2 A3 A4

8 unit times

Transaction 2
- A1 A2 A3 A4

Transaction 1
- A1 A2 A3 A4

5 unit times
Concurrent Exec. and Pipelining Transaction:

Transaction 4  Transaction 2  Transaction 1

A1 A2 A3 A4

16 unit times  Pipelining

A1 A2 A3 A4

A1 A2 A3 A4

5 unit times  Save more time

7 unit times

Concurrent Exec. and Pipelining

A1 A2 A3 A4
SiS Ultra-AGPII TM Advantage

- High Bandwidth @ 3.2GB/s > AGP 8X @ 2.1 GB/s
- Shorter Data Transfer Path vs. External AGP Path
- Bus Cycle Advance Pipeline vs. Pipeline
SiS Unified VGA Driver
  • Backward compatible w/M650/651/650/740 family
  • Support Win98SE, WinME, Win2000 and WinXP

SiS Unified AGP Driver
  • Backward compatible w/648/650/645/735/635/730/630 family

SiS7012 Unified Audio Driver
  • Backward compatible w/962/961/735/635 Family

SiS Unified LAN Driver
  • Backward compatible w/962/961/735/635/730/630 family

SiS Unified IDE Driver for ATA133
  • Backward compatible w/962/961 family
**USB2.0**

- WinXP SP1 and later one in-box USB2 driver support SiS USB2
- Win2000 and WinXP USB2 logo driver v1.00 released
- Win98SE and WinME USB2 driver supported from the third party.
<table>
<thead>
<tr>
<th>Product</th>
<th>Sample</th>
<th>Mass Production</th>
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<tr>
<td>North Bridge- M661MX</td>
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<td>North Bridge- M652</td>
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<td>North Bridge- 648MX</td>
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<tr>
<td>South Bridge- 963</td>
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Third Party Information
Thank You!!