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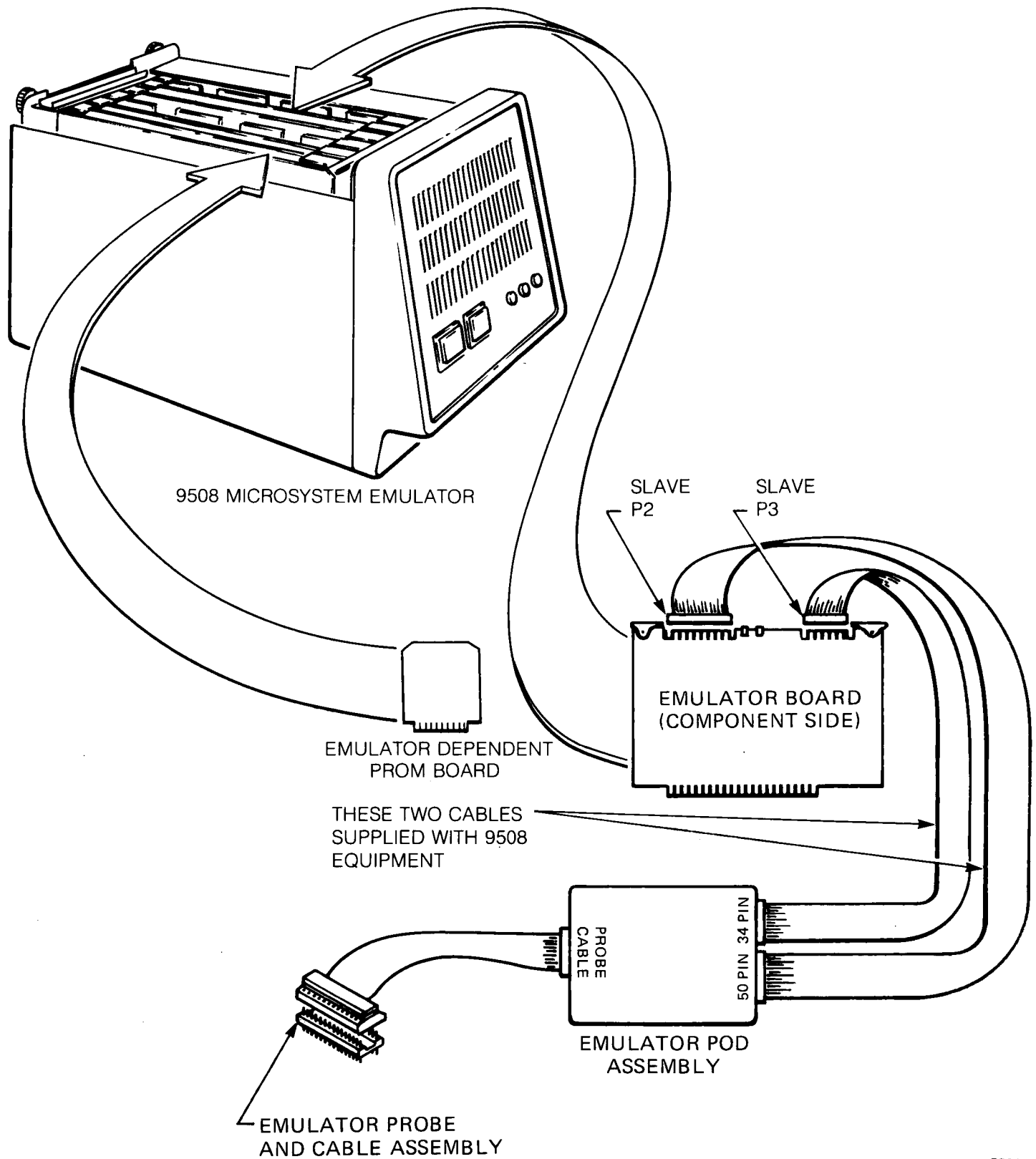
**9508 MICROSYSTEM EMULATOR  
USERS MANUAL ADDENDUM**

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**8085 EMULATOR OPTION**

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Gould Millennium Products



7501

### 8085 Emulator Option Components

**WARNING:**

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

The following procedures may help to alleviate the Radio or Television Interference Problems:

1. Reorient the antenna of the receiver receiving the interference.
2. Relocate the equipment causing the interference with respect to the receiver (move or change relative position).
3. Reconnect the equipment causing the interference into a different outlet so the receiver and the equipment are connected to different branch circuits.
4. Remove the equipment from the power source.

**NOTE:**

The user may find the following booklet prepared by the FCC helpful: "How to Identify and Resolve Radio-TV Interference Problems". This booklet is available from the U.S. Printing Office, Washington, D.C. 20402. Stock No. 004-000-00345-4.

This addendum to the 9508 MicroSystem Emulator Users Manual describes the capabilities, functions and operations of the 8085 Emulator Option. This option contains the necessary hardware components to configure the 9508 MicroSystem Emulator for testing/debugging user programs and hardware that are developed to support the 8085 Microprocessor chip. This addendum includes procedures for installing the optional equipment at the user's site and operating the 9508 MicroSystem Emulator to exercise the 8085 hardware/software functions. This addendum is to be used with, and inserted in back of the 9508 MicroSystem Emulator Manual.

The material in this addendum is up-to-date at the time of publication, but is subject to change without notice.

Copies of this publication and other Millennium publications may be obtained from the Millennium sales office or distributor serving your locality.

## RELATED PUBLICATIONS

### Manuals:

- 9508 MicroSystem Emulator Users Manual

### Application Notes:

- Diagnostic Programming for Microprocessor Based Systems
- Guide to Testing Microprocessor Unit Data Sheet

### Data Sheets:

- Intel® MCS-85™ Users Manual

If you require any assistance on this product, please call Millennium Systems Customer Service on the toll-free, hot-line numbers listed below:

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## 8085 EMULATOR OVERVIEW

This manual explains the operation of the 8085 Emulator Option for the 9508 MicroSystem Emulator.

The 8085 Emulator Option permits the user of 9508 equipment to expand the emulation capability to support microprocessor-based systems that are configured with the 8085 microprocessor chip.

Emulation on the 9508 System is accomplished in real-time processing and allows the user to perform the following functions:

- Set Breakpoints for hardware and software
- Step through user programs
- Run, display or modify user programs in the unit under test (UUT)
- Display and alter contents in registers, memory, and I/O ports
- Perform real-time trace and record the events
- Specify memory mapping and clock modes
- Display emulation environment
- Use emulator memory to make patches for program ROM

The 9508 MicroSystem Emulator with the 8085 Emulator Option installed, contains two microprocessors as follows:

1. The MC6800 control microprocessor is located on the control processor board that drives the 9508 system; it supervises system resources and executes commands that control the system processing functions for emulation.
2. The 8085 microprocessor used in the target system is located on the pod interface circuit board inside the Emulator Pod Assembly; it executes the users software and activates user hardware functions. The emulator pod contains special circuits that adapt the emulator/microprocessor to operate identically to the UUT system microprocessor.

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## INTRODUCTION

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### HARDWARE DEBUGGING

The 8085 Emulator Pod Assembly interfaces with the users unit under test via the 8085 Probe and Cable Assembly (see figure 1-1). This cable is terminated by a 40-pin probe that plugs into the microprocessor socket of the unit under test (UUT). By replacing the users microprocessor in the UUT with the emulator probe, the user can execute UUT programs under the control of the 9508 assembly language programs that reside in the following memory areas:

9508 Emulator RAM

UUT RAM

UUT ROM

This feature allows rapid debugging of both UUT hardware and software. Figure 1-1 shows the 9508 MicroSystem Emulator connected to a UUT.

### SOFTWARE DEBUGGING

Any 8085 executable object program can be executed/tested using the 9508 MicroSystem Emulator. Such a program may have been written in 8085 Assembly Language and appropriately assembled and linked at a host software development system and then downloaded from the host to reside in the 9508 emulator memory. The software system can be tested and debugged by the emulator without interfacing to a user hardware system.

1. The user can make patches to the program using assembly language mnemonics for opcodes. The emulator In-Line Assembler will automatically translate these mnemonics to the machine language used by the target system.
2. Likewise, the emulator In-Line Disassembler allows the user to display memory using the assembly language mnemonics.
3. The users software can be debugged using the 9508 memory and emulator, or the software can be tested using only the memory in the UUT.



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## INTRODUCTION

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9508 Emulator RAM  
UUT RAM  
UUT ROM

This feature allows rapid debugging of both UUT hardware and software. Figure 1-1 shows the 9508 MicroSystem Emulator connection to a UUT.

### SOFTWARE DEBUGGING

Any Z80A executable object program can be executed/tested using the 9508 MicroSystem Emulator. Such a program may have been written in Z80 Assembly Language and appropriately assembled and linked at a host software development system and then downloaded from the host to reside in the 9508 emulator memory. The software system can be tested and debugged by the emulator without interfacing to a user hardware system.

1. The user can make patches to the program using assembly language mnemonics for opcodes. The emulator In-Line Assembler will automatically translate these mnemonics to the machine language used by the target system.
2. Likewise, the In-Line Disassembler allows the user to display memory using the assembly language mnemonics.
3. The users software can be debugged using the 9508 Memory and emulator, or the software can be tested using only the memory in the UUT.



Figure 1-1. 9508 MicroSystem Emulator Connected to a Unit Under Test

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## INTRODUCTION

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### DESCRIPTION OF 8085 EMULATOR OPTION COMPONENTS

The 8085 Emulator Option contains the following items which are packaged in a kit for installation by the user in his 9508 system hardware.

- One 8085 Emulator Processor Board (Part No. 13000108) that is to be installed in the 9508 chassis to replace the existing emulator board.
- One 8085 Emulator Dependent PROM Board (Part No. 13000236-04) that contains 8K PROM space for 8085 emulator dependent code.
- One 8085 Emulator Pod Assembly (Part No. 15000109) that houses one printed circuit board containing the 8085 target system microprocessor and interface circuitry. This pod assembly is interfaced to the emulator board by two six-foot ribbon cables that are a part of the 9508 equipment (\*see the note that follows).

```
* * * * *
*                                     *
*                               NOTE   *
*                                     *
* The two 6-foot ribbon cables with 50-wire and 34-wire *
* conductors, respectively, are standard accessory items *
* that are supplied with the 9508 system, and therefore *
* are not included in the kit. These two cables are      *
* used to connect the 8085 Emulator Pod Assembly to the *
* 8085 Emulator Board.                                *
* * * * *
```

- One 8085 Probe and Cable Assembly (Part No. 15000054) that consists of the probe tip and a 1.5-foot, 40-conductor ribbon cable. One end of the cable connects to the Emulator Pod Assembly; the other end terminates in the 40-pin probe tip to interface with the UUT.
- One Users Manual (Publication No. 87000076) which describes the installation and operation procedure for the 8085 Emulator Option.

Information on how to order the 8085 Emulator Option as a complete package or individual parts of the package is presented in Appendix D.

## **DIFFERENCES IN 8085 EMULATOR VS ON-CHIP FUNCTIONS**

### **Operating Speed**

The 8085 emulator will operate at 3.12 MHz or 5 MHz. The emulator pod adds a 36-nanosecond delay for accessing user memory at 5 MHz.

Jumper connections on the emulator board allow the user to select timing conditions for memory wait states as determined by the users UUT memory. The description of these jumper connections is given in Chapter 2.

### **Halt Instruction**

If a HALT (HLT) instruction is executed in user mode after the GO command is issued, the emulator will halt execution of the users program and wait for an interrupt from the UUT. When the interrupt occurs, the users program will continue execution. Halt instructions encountered during execution in the System Mode are reported to the user immediately and emulation is stopped.

Interrupts that are initiated from the console keyboard after a HLT instruction has been executed, and no user interrupt has occurred, will terminate the emulation mode. The PCNEXT display for Trace line and Status will show the address of the HLT instruction and the display will indicate the mnemonic for the HLT instruction (opcode 76).

### **DMA Operation**

The HOLD line of the 8085 UUT is active at all times, even when the emulator is not executing in a continuous run condition. The HOLD acknowledge signal is generated to provide the HOLD request handshake. This feature allows external devices in the UUT to gain control of the bus for DMA cycles or memory refresh, even when not emulating the 8085.

### **Restart 7.5 Operation**

The users edge-sensitive RST 7.5 is latched when the emulator is not executing in a continuous run condition. When execution is resumed, the RST 7.5 signal will be recognized by the 8085 emulator. This is done to avoid losing interrupts while the emulator is not in the continuous run condition.

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**INSTALLATION**

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**GENERAL**

This chapter describes the installation of the 8085 Emulator Option components in the 9508 MicroSystem Emulator unit. The installation involves replacing the existing components in the card cage with the 8085 Emulator Board and the 8085 Emulator Dependent PROM Board supplied in the Emulator Option Kit. The existing emulator pod assembly and probe cable assembly are also replaced with corresponding components from the 8085 Emulator Option Kit.

Only one emulator board and dependent PROM board may be installed in the card cage at a time. For example, if a Z80 type emulator board and its corresponding dependent PROM board are presently installed in the 9508 chassis, then both boards must be removed and the 8085 boards installed in their place.

Approximately ten different types of microprocessor emulators are available for the 9508. Each type of emulator board interfaces with its corresponding emulator dependent PROM board and pod assembly. These parts contain unique hardware, logic and software routines that support a specific type of microprocessor and cannot be interchanged with similar components used for other types of emulators. For example, the Z80 or 6800 emulator components will not function with the 8085 emulator, or vice versa, and a mismatch could cause damage to the components. It is therefore necessary to ensure that all installed emulator components correspond to the type of microprocessor associated with the target system.

**UNPACKING AND INSPECTION**

All of the hardware items that are necessary for a user to install and operate the 8085 Emulator Option is contained in a packaged kit. Two printed circuit boards are provided to be installed in the 9508 chassis. The emulator pod assembly and probe cable are to be connected in the system as described in the procedure which follows.

Table D-1 in appendix D contains a list of individual parts and assemblies that are supplied in the kit. Use this table and the shipping papers to verify that all items are received.

If the equipment received from the carrier is incomplete or damaged, do not install the equipment. File a claim with the shipping firm immediately, and notify Millennium System's Customer Service department at once. Millennium will arrange for repair or replacement of the equipment without waiting for settlement of the claim against the carrier.

If the equipment must be returned to Millennium, attach a tag showing the owner, address, serial number, and a description of the failure. The original shipping carton and packing material should be reused with the RMA (Returned Material Authorization) number prominently displayed. An RMA number can be obtained by calling Customer Service on the toll-free, hot-line numbers listed in the Preface.

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## INSTALLATION

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Millennium System's Technical Support Representatives and Customer Engineers are available to provide consultation and assistance on request.

### MAINTENANCE AND SERVICE POLICIES

Unless notified to the contrary, any claims for operations assistance and/or service will be provided by Millennium Systems, Inc., from its plant in Cupertino, California. Should assistance be required, call Customer Service.

### SPECIAL ON-BOARD CONNECTIONS

The 8085 emulator board contains jumper connections that are set by the manufacturer to support standard conditions for 8085 emulation processing. These on-board circuit connections are described in the back of this chapter. Any adjustment of these connections, if required for special testing conditions, should be accomplished during the installation.

### INSTALLATION PROCEDURE

Before any kind of system testing is performed, the 8085 emulator board and emulator dependent PROM board must be installed in the 9508 chassis. Refer to figures 2-1 and 2-2, and perform the following step-by-step procedures:

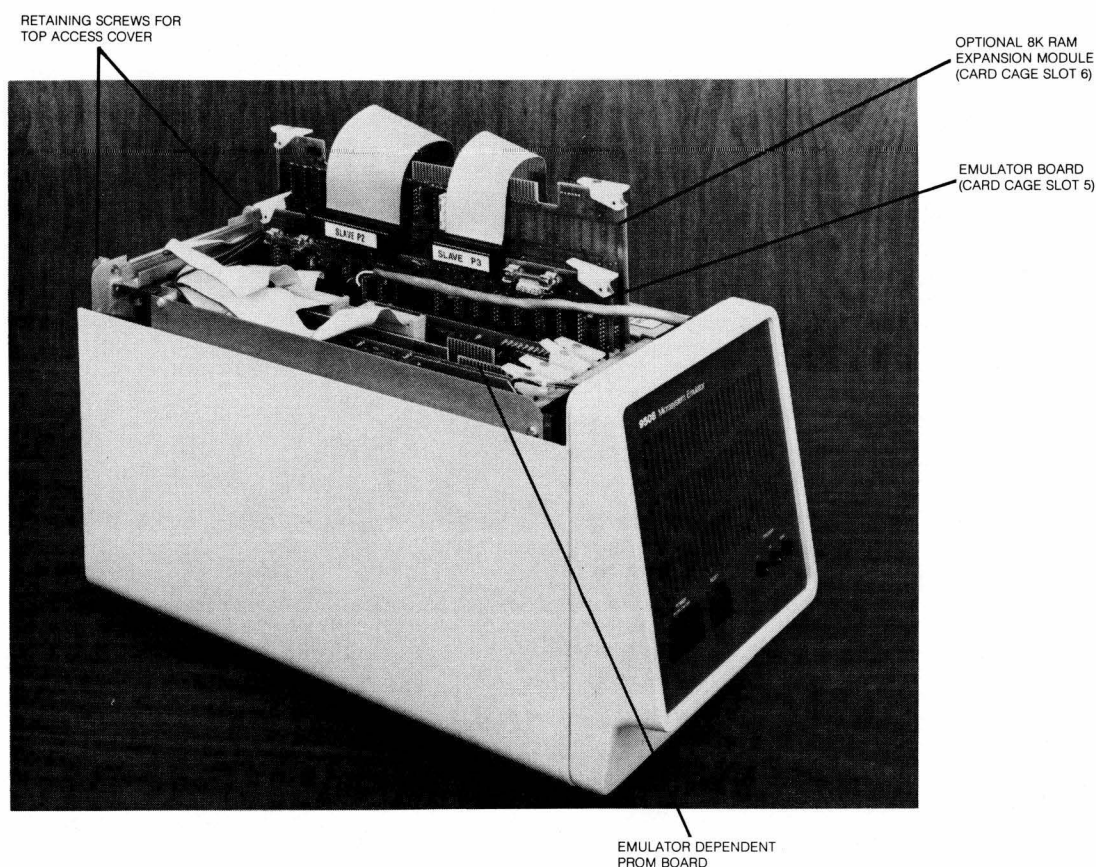
1. Remove power from the 9508 system and the UUT by pressing the POWER ON/OFF switch.
2. Loosen the two retaining screws at the rear of the chassis and remove the top access cover.
3. Locate the emulator board in the card cage. It can be identified by the name of the microprocessor that is labeled at the top of the board (Z80, 8080, 6801, etc.). It is located in the fifth slot from the left side of the card cage as shown in figure 2-1.
4. Disconnect the two ribbon cable edge connectors (SLAVE P2 and SLAVE P3) from the emulator board.
5. Using both hands, grasp the release tabs on each side of the emulator board and simultaneously pull out on the tabs so that the board is pulled out of its connector.
6. Remove the emulator board from the 9508 and store.
7. Insert the 8085 emulator board into the same slot of the card cage and simultaneously push down with both hands until it is fully seated.

```

* * * * *
*                                     *
*                               CAUTION                               *
*                                     *
*   Be careful not to damage the ribbon cable connectors             *
*   when installing the emulator board.                               *
*                                     *
* * * * *

```

8. Connect the two ribbon cable connectors (Slave P2 and P3) onto the P2 and P3 mating edge connectors on the emulator board. Fold and route the ribbon cables carefully through the horizontal slot at the rear of the chassis. The cables must be positioned flat against the slot to avoid interference when the top access cover is installed.



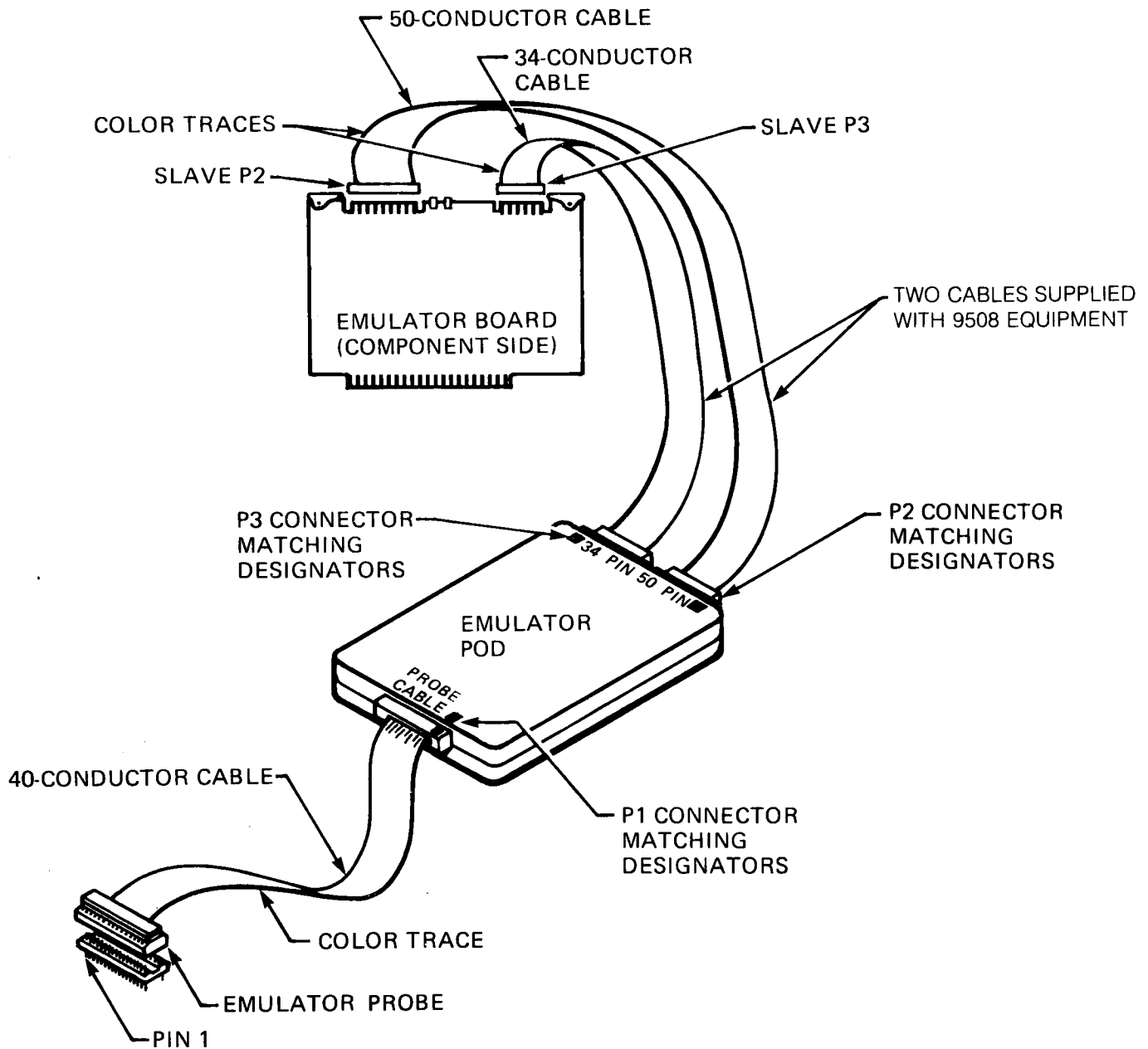
**Figure 2-1. Location of Emulator Board and Emulator Dependent PROM Board in 9508 Chassis**

## INSTALLATION

```

* * * * *
*                                     *
*                                     *
*          WARNING                   *
*                                     *
*   Installing the cables incorrectly may *
*   result in damage to the emulator board *
*   or the pod.                      *
*                                     *
* * * * *

```



### Figure 2-2. Connecting the 8085 Emulator Pod

7504

10. Install the top access cover and tighten the two retaining screws at rear of the chassis.

```

* * * * *
*                                     *
*                               CAUTION *
*                                     *
* The top access cover must be replaced to *
* provide proper air circulation before AC *
* power is applied. Ensure that the top *
* access cover is properly secured. The *
* buildup of heat due to improper air flow *
* will result if the top cover is not *
* secured. *
*                                     *
* * * * *

```

11. Disconnect the existing emulator pod from the emulator cables and connect the 8085 emulator pod. Match the 34-Pin and 50-Pin socket designators on the pod with the corresponding designators on the cables and connect the cables.
12. Connect the emulator probe cable with attached probe to edge connector P1 on the emulator pod.

```

* * * * *
*                                     *
*                               CAUTION *
*                                     *
* If the pod is plugged in incorrectly, it could *
* damage the pod or the emulator board. *
*                                     *
* * * * *

```

13. Remove the 8085 microprocessor from the UUT socket and plug the emulator probe tip into the microprocessor socket. Make sure that pin 1 of the socket is aligned with pin 1 of the probe tip.
14. After checking all connections, turn on power to the 9508 and UUT.



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## INSTALLATION

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### OPTIONAL USER CIRCUIT CONNECTIONS

The emulator board contains two jumper connections shown in figure 2-3, that can be modified by the user for the following test conditions:

MEM    --   Memory Wait States  
DEBUG --   Debug Wait States

#### Memory Wait States

The setting for Memory Wait States (MEM 0-2), while the emulator is accessing memory in the 9508, is determined by the read access cycle of the memory contained on the emulator. The 8085 emulator will operate at 3.12 MHz, or at 5 MHz, which causes an additional 36 nsec delay of memory access time for the pod interface.

Table 2-1 shows the location of jumper connections to achieve the various wait states for 3.12 MHz and 5 MHz operation.

No wait state is required when the emulator is operating at 3.12 MHz. To operate at higher frequencies, 1 to 2 wait states may be required.

The 8085 emulator is designed to operate at 5 MHz, and during emulation, additional propagation delays are inserted as shown in table 2-1. When the 8085 emulator is shipped from the factory, the MEM jumper is set for MEM 1 location, which provides 1 wait state.

If the emulator option is already installed, the power must be removed from the 9508 equipment and UUT before changing the circuit connections. The requirements for the UUT clock generator are presented in Chapter 3 of this addendum. Further information is provided in the Intel MCS-85 Users Manual listed in the Preface.

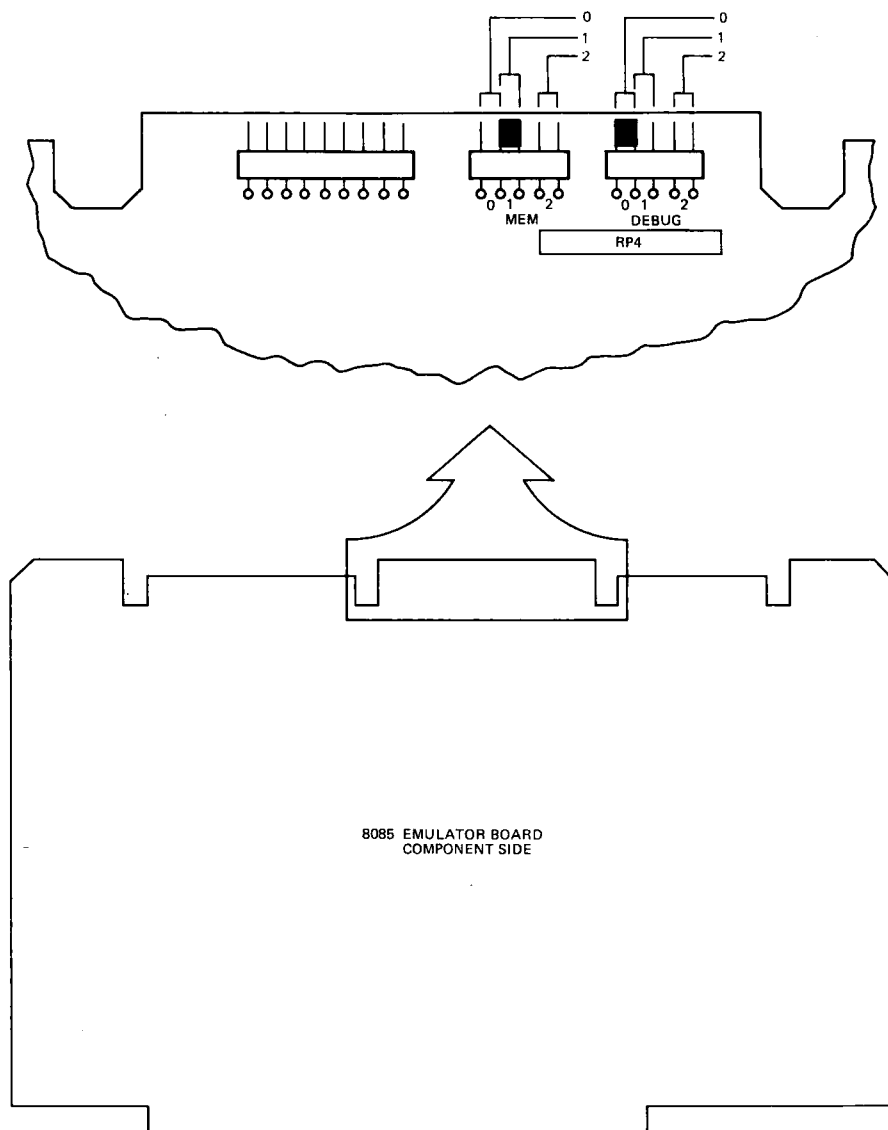
#### Debug Wait States

The Debug Wait States insert wait states for all instructions, either in the UUT or from the 9508 RAM.

The setting of Debug Wait States (DEBUG 0-2) is determined by the read access cycle of the emulator and UUT memory and is shown in table 2-1. The factory setting for the DEBUG Wait State is DEBUG 0.

**Table 2-1. Jumper Settings for Wait States**

Number of Wait States	Access Time (Worst Case)			Jumper Locations	
	5 MHz	3.12 MHz	Units	Memory Access	DEBUG Access
0	12	172	nsec	MEM0	*DEBUG 0
1	212	492	nsec	*MEM1	DEBUG 1
2	412	812	nsec	MEM2	DEBUG 2
*Indicates factory settings					



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**Figure 2-3. Location of On-Board Jumpers**

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**FUNCTIONAL DESCRIPTION**

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**GENERAL**

When the 9508 MicroSystem Emulator unit is powered on or reset, the 8085 becomes reset, and is initialized to a useable state. The emulator is controlled by the master microprocessor in the 9508 MicroSystem Emulator. During the execution of user programs, the emulator runs at full speed until a breakpoint is encountered, or a command is issued from the console, thereby causing the emulator to become paused.

The emulator power interface is +5V (TTL) level. MOS level is not supported. Except for the electrical and timing differences indicated in Appendix A, there are only a few cases where the 8085 emulator is functionally different from the users 8085 microprocessor in the UUT. These differences are associated with (1) the execution of a Halt (HLT) instruction after the GO command is issued, (2) interrupts initiated from the console keyboard after a HLT instruction has been executed, and (3) the state of the HOLD line which is held active at all times. These conditions are described in Chapter 1 of this addendum (see Differences in 8085 Emulator and On-Chip Functions).

**OPERATING CONCEPT**

Circuits in the interface pod assembly reconstruct the internal 8085 functions so that the emulator can be used to select, examine and operate the CPU functions in a real-time test environment. Primary functions of the CPU are:

1. To fetch instructions from memory in a sequential manner until instructed otherwise.
2. To perform the operation called out by the instruction.
3. To control the execution of the instruction.
4. To monitor and control the remaining elements of the system.
5. To control the flow of data throughout the system.

The emulator allows the user to manipulate CPU functions to select the serial I/O control, examine registers, change the register contents, and transfer data. The emulator can also trace the execution of individual instructions and record status for the resulting operations.

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## FUNCTIONAL DESCRIPTION

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### 8085 INSTRUCTIONS

The 8085 instruction set summary is presented in Appendix C. These instructions are classified into five different groups as follows:

1. Data Transfer Group
2. Arithmetic Group
3. Logical Group
4. Branch Group
5. Stack, I/O and Machine Control Group

The 8085 emulator executes all legal opcodes only. Illegal opcodes are not detected. Each instruction, upon execution, will cause the CPU to perform a unique type of response to manipulate and control the processing and transfer of data.

### 8085 CPU CHARACTERISTICS

The 8085 Microprocessor is an 8-bit, parallel central processor unit that is driven by +5 volts. Like most microprocessors, the 8085 architecture is organized around its internal registers, input controls, I/O controls, and internal buses. Registers are used to store data, point to addresses, store constants and perform add and subtract functions, etc.

The serial I/O port is controlled by the Serial Input Data (SID) and Serial Output Data (SOD) lines. Input data on the SID line is transferred when the Read Interrupt Mask (RIM) instruction is executed. The output data, SOD line is set or reset as specified by the Set Interrupt Mast (SIM) instruction.

The 8085 uses a multiplexed address and data bus. The address is divided between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first cycle, the upper 8 bits for the address are transferred while the lower 8 bits are latched into the peripherals.

Additional 8085 features include an internal clock generator, three maskable, Restart Interrupts (RST 5.5, RST 6.5 and RST 7.5), and one nonmaskable (TRAP) Interrupt. Additionally, an Interrupt Request (INTR) input line and Interrupt Acknowledge (INTA) output line are used to communicate with off-chip peripherals.

## 8085 CPU CHARACTERISTICS (Continued)

Complete details of the 8085 Microprocessor features are described in the Intel MCS-85 User's Manual which is listed in the Preface.

### EMULATOR OPERATING MODES

The 8085 Emulator Option employs two modes of operation: System Mode and User Mode. The emulator operating mode is selected by entering the EMUL command at the console keyboard. The emulator defaults to System Mode whenever a system reset occurs. The command is entered as follows:

EM) ul  $\begin{bmatrix} s \\ u \end{bmatrix}$

where: the input parameters, u and s indicate the following conditions:

s = System Mode is selected for emulation

u = User Mode is selected for emulation

### User Mode Function

The User Mode selects the UUT resources for processor clock and memory, or memory can be mapped by the emulator. In User Mode, the debug access wait states may be inserted to propagate delays according to jumper settings on top of the emulator board as described in table 2-1 of Chapter 2 in this addendum. The User Mode operates at 3.12 MHz with no wait states required. If higher frequencies are used, one to two wait states may be required. Refer to table 2-1 for details.

### System Mode Function

The System Mode selects the emulator resources for clock and memory. Therefore, all user programs must reside in the emulator RAM. In System Mode, the emulator operates at 3.12 MHz without propagation delays. The 8085 Emulator is designed to operate at 5 MHz, and during emulation, memory access wait states may be inserted as shown in table 2-1.

---

## FUNCTIONAL DESCRIPTION

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### UUT CLOCK REQUIREMENTS

Power and clock fault conditions are detected and reported as an emulator fault. The 8085 microprocessor has an internal clock generator. The inputs to the clock may be a crystal, resistor and capacitor, or a TTL signal as shown in figure 3-1.

Listed below are the operating characteristics of the clock oscillator located on the emulator probe. Refer to the Intel MCS-85 User's Manual and/or supplement for a detailed explanation of the following specifications.

#### Crystal Mode

Frequency, maximum	10.0 MHz (Parallel Resonant)
Frequency, typical	6.25 MHz
Connections	See figure 3-1a.

#### R-C Mode

Time constant, maximum	3 MHz operational (R = 10K, C = 20pF)
Connections	See figure 3-1b.

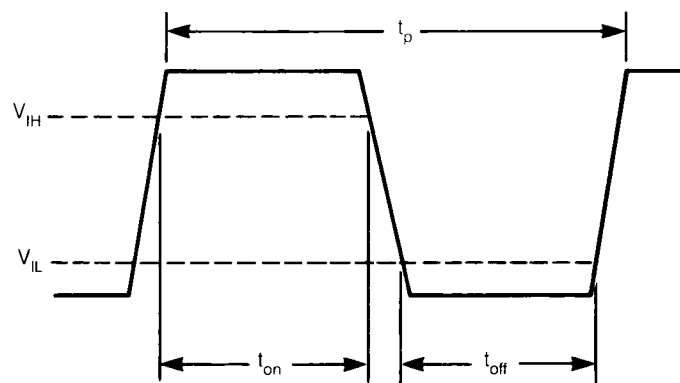
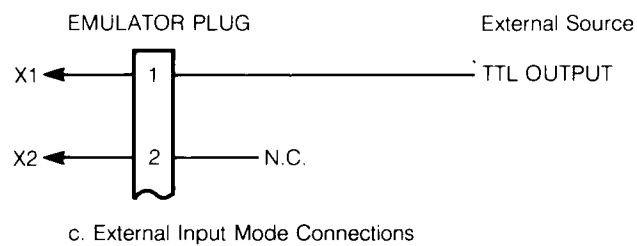
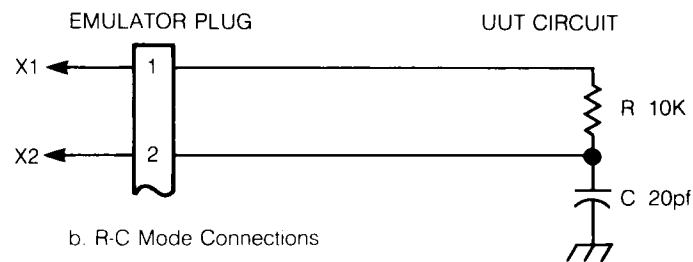
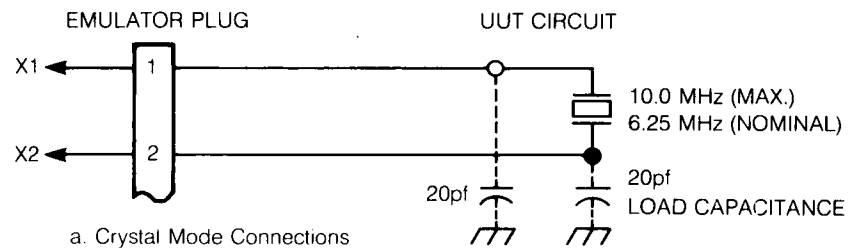
#### External Input Mode

Probe Input Characteristics at X1	One TTL input (X2 should not be connected)
Connections	See figure 3-1c. The timing requirement for $t_{off}$ must be >40 nsec as shown in figure 3-1d.

### 8085 EMULATOR DEPENDENT COMMANDS

The 8085 emulator dependent commands initiate and control emulation processing for unique characteristics of the 8085 microprocessor used in the target system. These characteristics are established by the CPU architecture and chip design features which include the following:

- CPU Instruction Set Mnemonics and Opcodes
- CPU Register Identification and Functions
- I/O Port Configuration and Control
- CPU External System Controls



d. External Input Mode Timing Requirements

7602

Figure 3-1. External Connections and Timing for 8085 UUT Control Probe Oscillator



---

## FUNCTIONAL DESCRIPTION

---

### 8085 EMULATOR DEPENDENT COMMANDS (Continued)

The 9508 MicroSystem Emulator employs 28 basic commands for system operations. Several of these basic commands, as follows, are configured by the software to control emulation processing for unique 8085 chip functions:

<u>COMMAND NAME</u>	<u>MINIMUM ENTRY</u>
ASM	A)sm
DISM	DI)sm
DRT	DR)†
DUMP	D)ump
RESET	RES)et
REG	REG
REGBRK	REGB)rk
STATUS	S)tatus
PORT	P)ort†

### COMMAND DESCRIPTION

The use of these commands for 8085 emulation processing is described in subsequent paragraphs.

## ASM Command

The A)sm command is used to modify instructions and data in memory. The 8085 Instruction Set mnemonics and syntax described in appendix C, can be specified in the input instead of the hexadecimal opcode. The operand value for addresses and data can only be set in hexadecimal values.

The following example indicates input requirements for modifying instructions using the ASM command, where the Bias W register = 100, and addressing modes are included to emphasize the assignment of bytes per instruction:

```

A)sm      W

W+0000  ORA B           (Register)
W+0001  LDA  W15        (Direct)
W+0004  MVI  B, 10      (Immediate)
W+0006  LXI  H, 2000    (Immediate)
W+0009  MOV  A, M       (Register Indirect)
W+000A  DCR  B          (Register)
W+000B  JNZ  W6         (Direct)
W+000E                      (Direct)

```

For this example, the user types Asm W to assemble at location W (address of Bias W Register). The system responds with the prompt address of W+0000. The user types ORA B (carriage return). The system calculates and enters the required hexadecimal value of the instruction at location W+0000. The system then calculates the address of the next instruction location, W+0001, and prompts the user for input. This interactive sequence is repeated until the user terminates the sequence with a null line (carriage return) or control Z input.

The following example indicates input requirements for modifying data in memory by reserving space at specific locations:

```

A)sm 1000

1000 BLOCK 15          (Reserve 15 decimal bytes of storage)
100F BYTE OF1         (Reserve 1 byte. Place F1 in BYTE location.)
1010 WORD OFW10       (Reserve 2 bytes. Place W10(=0110) in WORD location)
1012

```

---

## FUNCTIONAL DESCRIPTION

---

### ASM Command (Continued)

For this example, the user types `Asm 1000` to establish the starting address where the assembly will occur. The system responds with the prompt address of 1000. The user enters `BLOCK 15`. The system calculates and reserves 15 decimal bytes of storage at location 1000. The system then calculates the address of the next storage location, 100F, and prompts the user for input. This interactive sequence is repeated until the user terminates the sequence with a null line (carriage return) or control Z input.

Two types of error conditions, recovery and non-recovery, may occur in the input line. The recovery type errors, such as, `**INVALID OPERATION**` and `**INVALID OPERANDS**`, etc. are discarded, and the user is reprompted to enter the correct input using the same address location that was given for the invalid entry.

The non-recovery type errors, such as, `**ERROR 14**`, `**ERROR 12**`, `**ERROR 11**`, etc. will make it necessary for the user to specify a different address (error #11, #14), or use a valid CPU operating mode to make memory available (error #12).

## DISM Command

The Dism command translates hexadecimal memory data to an assembled mnemonic line form. The 8085 Instruction Set mnemonics are used in the display format. Areas of memory that are unrecognizable in the form of instruction mnemonics are displayed as question marks (e.g. ???=). The following example indicates the output display for data that was assembled by the Aism command:

Dism W WD

ADDR	OBJECT	INSTRUCTION
W+0000	B0	ORA B
W+0001	3A 15 01	LDA W+0015
W+0004	06 10	MVI B, 10
W+0006	21 00 20	LXI H, W+1F00
W+0009	7E	MOV A, M
W+000A	05	DCR B
W+000B	C2 06 01	JNZ W+0006

The following example indicates the result of executing the program. The ESC key can be used to stop emulation.

GO W STEP 7 TRACE ALL

LOC	MNEM	OPERAND	EFADDR	A	SZAPC	BC	DE	HL	SP	PCNEXT
W+0000	ORA	B		00	01010	0000	0000	0000	0000	W+0001
W+0001	LDA	W+0015		20	01010	0000	0000	0000	0000	W+0004
W+0004	MVI	B,10		20	01010	1000	0000	0000	0000	W+0006
W+0006	LXI	H,W+1F00		20	01010	1000	0000	2000	0000	W+0009
W+0009	MOV	A,M	W+1F00	00	01010	1000	0000	2000	0000	W+000A
W+000A	DCR	B		00	00010	0F00	0000	2000	0000	W+000B
LOC	MNEM	OPERAND	EFADDR	A	SZAPC	BC	DE	HL	SP	PCNEXT
W+000B	JNZ	W+0006		00	00010	0F00	0000	2000	0000	W+0006

STEP COUNT COMPLETE  
EMULATION STOPPED

---

## FUNCTIONAL DESCRIPTION

---

### DRT Command

The DRT command displays data captured in the real time trace buffer. The hexadecimal opcode is disassembled for bytes of instruction fetches and the mnemonic opcode is presented in the display. The following example shows the 8085 format for the trace buffer display:

DRT+

LOC	DATA	BUS	7 CLIPS 0	INSTRUCTION	DATA
W+0000	B0	MRF	0000 0000	ORA B	
W+0001	3A	MRF	0000 0000	LDA W+0015	20
W+0002	15	MR	0000 0000		
W+0003	01	MR	0000 0000		
W+0015	20	MR	0000 0000		
W+0004	06	MRF	0000 0000	MVI B, 10	
W+0005	10	MR	0000 0000		
W+0006	21	MRF	0000 0000	LXI H, W+1F00	
W+0007	00	MR	0000 0000		
W+0008	20	MR	0000 0000		
W+0009	7E	MRF	0000 0000	MOV A, M	00
W+1F00	00	MR	0000 0000		
W+000A	05	MRF	0000 0000	DCR B	
W+000B	C2	MRF	0000 0000	JNZ W+0006	
W+000C	06	MR	0000 0000		
W+000D	01	MR	0000 0000		

### DUMP Command

The Dump command displays memory contents in hexadecimal and ASCII format. The display of data that was assembled using the Asm command is presented in the following example:

**D)ump    1000   1012**

ADDR =	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	ASCII
1000 =	84	A3	A0	81	20	81	01	04	05	00	81	81	10	81	01	F1	.... ... .....
1010 =	A7	F2	80	01	A5	85	81	35	81	01	04	10	24	81	04	01	.....5.....\$...

---

## FUNCTIONAL DESCRIPTION

---

### RESET Command

The RESET command performs a simulated reset of all the control registers of the emulated chip as well as actually providing a reset to the chip input. The next GO command will then function as though a reset was actually applied to the chip, as far as execution of programs is concerned. To attain a real reset condition during execution of the user program, the reset must come from the user hardware.

When the RESET command is issued at the keyboard console, the PC NEXT register is reset to 0000. If the reset is user initiated, all the registers are reset, i.e.:

A	SZACP	BC	DE	HL	SP	PCNEXT
00	00000	0000	0000	0000	0000	0000

## REG and REGBRK Commands

REG Command. The REG command is used to examine and optionally, to modify the internal registers of the 8085 microprocessor. The syntax of the REG command is:

REG [parameter]

where parameter entry is defined in the list which follows:

The following list describes standard register names, flags, response values, and other conditions associated with the parameter when the REG or REGBRK command is issued. The effectivity for REG and/or REGBRK is indicated in the X column. Unique parameters that are effective for the REGBRK command only are presented at the end of the list.

If no parameter is specified in the command entry, the system will default to the first parameter (Register A, Accumulator). The REG command interacts with the user in the same manner as the EXAM command.

### LIST OF PARAMETERS FOR REG AND REGBRK COMMAND

<u>PARAMETER</u>	<u>EFFECTIVITY</u>		<u>DESCRIPTION</u>	<u>ALLOWED VALUE</u>
	<u>REG</u>	<u>REG BRK</u>		
A	X	X	A Register (Accumulator)	Hex Byte
S	X	X	Sign Flag Bit	0,1 Bit
Z	X	X	Zero Flag Bit	0,1 Bit
AC	X	X	Auxiliary Carry Flag Bit	0,1 Bit
P	X	X	Parity Flag Bit	0,1 Bit
CY	X	X	Carry Flag Bit	0,1 Bit
B	X	X	B Register (Accumulator)	Hex Byte
C	X	X	C Register	Hex Byte
D	X	X	D Register	Hex Byte
E	X	X	E Register	Hex Byte
H	X	X	H Register	Hex Byte
L	X	X	L Register	Hex Byte
SP	X	X	Stack Pointer Register	Address
PC		X	Program Counter (Points to location of the next instruction)	Address



---

## FUNCTIONAL DESCRIPTION

---

### REG, REGBRK (Continued)

REGBRK Command. The REGBrk command is used to define a register breakpoint as determined by one to eight test conditions involving specific registers. The break occurs only when all conditions are true. The emulator operates in a SINGLE STEP MODE whenever a REGBRK condition has been established. The syntax of the REGBrk command is:

REGBrk [clear] [condition 1... [condition 8]... ]

where parameters for:

Clear = Clear current conditions. If this parameter is not specified, any new conditions, 1...8 will be appended to the existing breakpoint conditions.

Condition = The parameters for conditions 1 through 8 are associated with the Register-Relations value that is specified with the register name to establish when or where the break is to occur. If no parameters are specified, the current register breakpoint conditions are displayed.

For all registers, the relation values are shown below. Note that a period is used as a delimiter in front of, and after the specified value.

<u>REGISTER RELATION VALUE</u>	<u>DESCRIPTION</u>
.EQ.	Equal
.NE.	Not equal
.LT.	Two's complement - Less Than
.ULT.	Unsigned - Less Than
.GT.	Two's complement - Less Than
.UGT.	Unsigned - Greater Than
.LE.	Two's complement - Less Than or Equal
.ULE.	Unsigned - Less Than or Equal
.GE.	Two's complement - Greater Than or Equal
.UGE.	Unsigned - Greater Than or Equal

**REG, REGBRK (Continued)**

Since the same register name can appear in more than one break condition, a range of values can be established. For example, the entry of register name, PC and register relation value, .UGE. is entered as follows:

**REGBR** PC.UGE.100 PC.ULE.1FF

This command entry will cause a break to occur whenever the Program Counter is positioned between the range of 100 and 1FF.

---

## FUNCTIONAL DESCRIPTION

---

### STATUS Command

The S)tatus command is used to query and display the current status of the emulator test environment and/or CPU dependent register and test conditions for the 8085 microprocessor.

The syntax of the STATUS command is:

S)tatus [parameter]

where the parameter entry is one of the following:

E)nv - Display only the emulation test environment information

R)eg - Display only the CPU dependent register information

If no parameter is specified, the system will display both the emulator test environment and the CPU dependent register information.

The emulation test environment information is standard regardless of the microprocessor type and includes the following testing conditions:

- |                                      |  |
|--------------------------------------|--|
| ● Name of Processor Version          | ● Emulator State:                        |
| ● Bias Setting                       | --Paused                                 |
| ● Mapping Information                | --Address Specified in<br>Go Encountered |
| ● Event Definitions                  | --Faulted                                |
| ● Real-Time Trace Qualification      | --Single Cycle Completed                 |
| ● Trigger and Breakpoint Definitions | --Memory Write Failure                   |
| ● Register Break Definition          |  |

The 8085 CPU dependent test conditions consist of data, flags and test criteria as defined in subsequent paragraphs.

The information displayed for the STATUS REG command is formatted as follows:

PROCESSOR = 8085 V1.0

LOC	MNEM	OPERAND	EFADDR	A	SZAPC	BC	DE	HL	SP	PCNEXT
0000	ORA	D		00	0000	0000	0000	0000	0000	0000

## STATUS (Continued)

The effective address is displayed whenever an indirect-HL memory reference occurs (M operand or PCHL instruction). As in the Z80 display, the status flags, sign (S), zero (Z), auxiliary carry (A), parity (P) and carry (C) are displayed as bits, rather than a hex byte, and are individually labeled. Also, the registers are displayed in pairs. The 8085 Trace Line and STATUS REG display are identical.

The information presented in the various data fields of the STAT REG display presents the following status conditions. The allowed values for each STAT REG data field are described in the List of Parameters for REG and REGBRK command.

### DESCRIPTION OF DATA FIELDS DISPLAYED FOR STATUS REG COMMAND

<u>MNEMONIC</u>	<u>DESCRIPTION</u>
LOC	Address of the last instruction executed
MNEM	Instruction Mnemonic
OPERAND	Operand of the last instruction executed
EFADDR	Effective Address (displayed when Indirect-HL Memory Reference occurs)
A	Register A Contents
SZAPC	Flag Register Status Bit Settings, where: <div style="margin-left: 40px;">             S = Sign Flag Bit              Z = Zero Flag Bit              A = Auxiliary Carry Flag Bit              P = Parity Flag Bit              C = Carry Flag Bit           </div>
BC	Register Pair, BC Contents
DE	Register Pair, DE Contents
HL	Register Pair, HL Contents
SP	Stack Pointer Contents
PCNEXT	Address of Next Instruction Fetch

---

## FUNCTIONAL DESCRIPTION

---

### PORT Command

The P)ort command is used to read data from, or write data to an I/O device in the 8085 unit under test and is only used in the emulator user mode.

The syntax of the PORT command is as follows:

**P)ort** addr [hh] [Rep]

where:   addr   =   Valid port address for 8085 which is a hexadecimal number ranging from 00H through FFH. The address is initialized to zero by the RESET switch.

          hh   =   Hexadecimal Data. If this parameter is used, the data hh is written to the port. If this parameter is omitted, a read from the port occurs.

          rep   =   Repeat parameter which causes the emulator to repeat the read or write operation until the user aborts the process with an ESCAPE.

**GENERAL**

The 9508 MicroSystem Emulator Manual describes all system commands and includes general operating procedures for the system. This chapter describes unique system operations for the 8085 Emulator Option as related to the design characteristics and operating conditions for the 8085 microprocessor chip.

The 8085 Emulator hardware components must have been installed, connected and checked out for emulation as described in Chapter 2 of this addendum. Operation of the 8085 Emulator Option involves the following types of user activity:

- Initializing the emulator system
- Downloading the users program from host computer system to the emulator system via the communication link
- Displaying microprocessor status and modifying the content of internal CPU registers using the STATUS and REG commands
- Examining and modifying CPU instructions in memory by using the DISM and the ASM commands
- Setting register breakpoint and displaying the trace buffer contents using the REGBRK and DRT commands
- Uploading the debugged program from the emulator to the host computer system via the communications link.

**INITIALIZATION**

The 9508 system can be initialized from a cold start by operating the POWER switch or by restarting system operations with the RESET switch. Refer to the Installation and Checkout Procedure in Chapter 3 of the 9508 MicroSystem Emulator Manual. This procedure describes the 9508 self test diagnostic, system initialization and error conditions associated with the startup. Use the following procedure to power up the system from a cold start:

1. Turn on the power switch at the display terminal.
  - a. On the 9501 Terminal, a bell will beep within 1 second to indicate power is on.

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## OPERATION

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### INITIALIZATION (Continued)

- b. After a few seconds, the cursor will appear in the upper left-hand corner of the screen. At this time, the operator can adjust the contrast to obtain the desired brilliance for the screen.
2. Turn on the POWER switch at the 9508 MicroSystem Emulator.
  - a. The system will perform a self test and initialization process. If no errors are present during start up, a message is displayed, ending with the prompt character as shown in the 8085 Emulator Start Up Message example presented below.
  - b. If an error condition is encountered during start up, the following message is displayed:

\*\* System Error xx \*\*  
continue Y or N?

where: xx is an error code number that is described in Chapter 3 of the 9508 MicroSystem Emulator Manual.

The query, Y or N?, allows the user to specify Yes to continue the self test program by overriding the error condition, or No to stop the program. The description of user action for responding to the query is presented in Chapter 3 of the 9508 MicroSystem Emulator Manual.

#### 8085 EMULATOR START UP MESSAGE

9508 READY VER xx

(Where xx equals software revision level.)

PROCESSOR=8085 VXX

W=0000 X=0000 Y=0000 Z=0000

MAPPED RAM 1 START=0000 END=1FFF

Event	Address	Data	Bus	7 CLIPS	0 TRig	Pass cnt	Delay cnt	TMode	SEL	TRIG	
1	= OFF	=OFF	All	XXXX	XXXX	1	0 E1	0 MS	T1	IND	T1
2	= OFF	=OFF	All	XXXX	XXXX	2	0 E2	0 MS	T2	IND	T2

BReak T1=Dsbl T2=Dsbl Count= 0 MS Qual=ALL

LOC	MNEM	OPERAND	EFADDR	A	SZAPC	BC	DE	HL	SP	PCNEXT
0000	ORA	D		00	00000	0000	0000	0000	0000	0000

REGBRK CONDITIONS:

SYSTEM MODE

D>

## **INITIALIZATION (Continued)**

The emulator start up message contains 12 lines of information which presents the standard emulator test environment (lines 1-8) and CPU dependent test conditions (lines 9-12).

The abbreviations used for the standard emulator test environment (lines 1-8) are described in Chapter 8 of the 9508 MicroSystem Users Manual which defines the contents displayed for each line of information.

The abbreviations used for the 8085 CPU dependent test conditions (lines 9-14) are described in Chapter 3 of this addendum (see description of STATUS REG command).

## **DOWNLOADING USERS PROGRAM FROM HOST**

Details of intersystem communication for downloading and uploading data between the emulator and host system is described in Chapter 6 of the 9508 MicroSystem Emulator Manual. Refer to this information which presents procedures for the following coverage.

- Communication Link Protocol (Electrical, ACK/NAK, None)
- Data Block Characteristics (TEKHEX, Binary Formats)
- Channel Characteristics (Half/Full Duplex; Parity Designation, None, odd, even; Baud Rate)
- Details of Message Block Formats
- Use of RHEX/WHEX commands for upload/download operation with description of defaults and error conditions

After the download operation is completed, the communications link can be disconnected from the host system and the emulation processing can be conducted at the emulator in a stand-alone mode.

## **CONFIGURING EMULATION TEST ENVIRONMENT**

The emulation test environment can be established after the users program is downloaded from the host. Set up of the emulation test environment involves the use of various commands to select test conditions for the 8085 target system microprocessor. The Start Up Message display, described in previous sections



---

## OPERATION

---

### CONFIGURING EMULATION TEST ENVIRONMENT (Continued)

for initialization, contains 12 lines of information that must be specified by the user for the following emulation test conditions:

- Setting of Bias Registers, W, X, Y, and Z.
- Control Settings for Event, Data Bus, Trace Clips, Triggers, Pass Count, Delay Count, etc.
- Brake and Trace Conditions for Trigger Setting, Counter and type of data to be collected.
- Specific conditions for the 8085 microprocessor to be emulated (i.e., registers, flags, interrupts, program counter, etc.).
- Register Breakpoint Conditions
- Emulator Operating Mode for either System Mode (S) where the processor clock is supplied by the emulator with mapped memory used for emulation, or User Mode (U) where the processor clock is supplied by the UUT and resident memory is either the UUT source or mapped by the emulator.

After the test environment is configured by the user, the status of the test conditions can be displayed by entering the S)tatus command. The various commands for setting the test conditions and parameters are described in Chapter 5 of the MicroSystem Emulator Manual.

The established configuration of the emulation test environment remains available for use until it is either changed by the user, or when the system is reset or powered down.

### CPU REGISTER FUNCTIONS

A detailed description of the 8085 internal registers is presented in the Intel MCS-85 User's Manual. The CPU registers can be accessed by entering the REG and REGBRK commands at the console.

The REG command allows the user to select, examine and modify content of CPU internal registers. The user must specify the register name in the command string by entering the name of the register as a parameter. For example, altering the stack pointer (SP) register contents allows the user to set the SP address to begin execution at a specified memory location. Note that the user cannot select the PC register with the REG command.

## CPU REGISTER FUNCTIONS (Continued)

The REGBRK command is used to select a register or CPU operating condition as determined by the parameters that specify the various breakpoint conditions provided by the emulator. Note that all register parameters specified for the REG command can also be accessed by the REGBRK command.

## I/O FUNCTIONS

Emulator I/O functions allow the user to read from, or write to an I/O device in the users 8085 unit under test. The PORT command described in Chapter 3 of this addendum is used to select the I/O device address which is a hexadecimal number within the range of 00H through FFH as defined by the users hardware. Refer to the description of the PORT command in Chapter 3 of this Addendum for making the PORT command keyboard entry and assigning the required parameters to initiate I/O read/write operations.

## BREAKPOINT AND TRACE LINES

The GO command is used to begin execution at a specified address. The mode of execution for continuous run, single step, etc. can be specified in the command along with break and trace requirements. Breakpoint and trace lines appear on the display as a result of conditions specified in the GO command. These conditions include instruction fetches encountering, breakpoints, event comparisons, machine status, and CPU timing conditions. Addresses and data are displayed in hexadecimal format. Instructions are displayed in the 8085 Instruction Mnemonic Format. (See Appendix C.)

The trace line display format is as follows:

### GO W STEP 7 TRACE ALL

LOC	MNEM	OPERAND	EFADDR	A	SZAPC	BC	DE	HL	SP	PCNEXT
W+0000	ORA	B		00	01010	0000	0000	0000	0000	W+0001
W+0001	LDA	W+0015		20	01010	0000	0000	0000	0000	W+0004
W+0004	MVI	B,10		20	01010	1000	0000	0000	0000	W+0006
W+0006	LXI	H,W+1F00		20	01010	1000	0000	2000	0000	W+0009
W+0009	MOV	A,M	W+1F00	00	01010	1000	0000	2000	0000	W+000A
W+000A	DCR	B		00	00010	0F00	0000	2000	0000	W+000B
LOC	MNEM	OPERAND	EFADDR	A	SZAPC	BC	DE	HL	SP	PCNEXT
W+000B	JNZ	W+0006		00	00010	0F00	0000	2000	0000	W+0006

STEP COUNT COMPLETE  
EMULATION STOPPED

---

## OPERATION

---

### BREAKPOINT AND TRACE LINES (Continued)

where: The processor status flags (SZAPC) in the trace line are presented as bits and are individually labeled. The following information is presented in the trace line:

- LOC - - Address of the last instruction executed
- MNEM - - Instruction Mnemonic
- OPERAND - - Operand of the last instruction executed
- EFADDR - - Effective Address (displayed when Indirect-HL Memory Reference Occurs)
- A - - Register A Contents
- SZAPC - - Flag Register Bit Settings:

where:

- S = Sign Flag Bit
- Z = Zero Flag Bit
- A = Auxiliary Carry Flag Bit
- P = Parity Flag Bit
- C = Carry Flag Bit

- BC - - Register Pair, BC Contents
- DE - - Register, Pair, DE Contents
- HL - - Register Pair, HL Contents
- SP - - Stack Pointer Contents

- PCNEXT - - Address of the next instruction fetch

For purposes of the JMP trace the following list of jump mnemonics is applicable.

JMP	CALL	RET	RST 0
JNZ	CNZ	RNZ	RST 1
JZ	CZ	RZ	RST 2
JNC	CNC	RNC	RST 3
JC	CC	RC	RST 4
JPO	CPO	RPO	RST 5
JPE	JPE	RPE	RST 6
JP	CP	RP	RST 7
JM	CM	RM	PCHL

## 8085 ELECTRICAL CHARACTERISTICS

The AC electrical characteristics of the 8085 Emulator are presented in table A-1. The 8085 Emulator interface is TTL, the MOS level is not supported. The propagation delays added by the probe are indicated in the column titled DIFFERENCE.

Table A-1. 8085 Electrical Characteristics

( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ;  $V_{CC} = 5\text{V} \pm 5\%$ ;  $V_{SS} = 0\text{V}$ )

SYMBOL	PARAMETER	MIN	MAX	DIFF	UNITS
$T_{CYC}$	CLK Cycle Period	200	2000	0	nsec
$t_1$	CLK Low Time	30		0	nsec
$t_2$	CLK High Time	50		0	nsec
$t_r, t_f$	CLK Rise and Fall Time		30	0	nsec
$t_{AL}$	Address Valid Before Trailing Edge of ALE	50		0	nsec
$t_{LA}$	Address Hold Time After ALE	50		-12	nsec
$t_{LL}$	ALE Width	80		0	nsec
$t_{LCK}$	ALE Low During CLK High	50		-3	nsec
$t_{LC}$	Trailing Edge of ALE to Leading Edge of Control	60		-15	nsec
$t_{AFR}$	Address Float After Leading Edge of $\overline{\text{READ}}$ ( $\overline{\text{INTA}}$ )		0	0	nsec
$t_{AD}$	Valid Address to Valid Data In		350	-40	nsec
$t_{RD}$	$\overline{\text{READ}}$ (or $\overline{\text{INTA}}$ ) to Valid Data		150	-58	nsec
$t_{RDH}$	Data Hold Time after $\overline{\text{READ}}$ ( $\overline{\text{INTA}}$ )	0		-24	nsec
$t_{RAE}$	Trailing Edge of $\overline{\text{READ}}$ to Re-enabling of Address	80		-6	nsec
$t_{CA}$	Address (A8-A15) Valid After Control	60		-6	nsec
$t_{DW}$	Data Valid to Trailing Edge of $\overline{\text{WRITE}}$	230		-6	nsec
$t_{WD}$	Data Valid After Trailing Edge of $\overline{\text{WRITE}}$	40		-6	nsec
$t_{CC}$	Width of Control Low ( $\overline{\text{RD}}$ , $\overline{\text{WR}}$ , $\overline{\text{INTA}}$ )	230		0	nsec
$t_{CL}$	Trailing Edge of Control to Leading Edge of ALE	25		0	nsec
$t_{ARY}$	READY Valid from Address Valid		100	-18	nsec
$t_{RYS}$	READY Setup Time to Leading Edge of CLK	100		-16	nsec
$t_{RYH}$	READY Hold Time	0		0	nsec
$t_{HACK}$	HLDA Valid to Trailing Edge of CLK	40		-14	nsec
$t_{HABF}$	Bus Float After HLDA		150	+7	nsec
$t_{HABE}$	HLDA to Bus Enable		150	+7	nsec
$t_{RV}$	Control Trailing Edge to Leading Edge of Next Control	220		0	nsec
$t_{AC}$	Address Valid to Leading Edge of Control	115		-6	nsec
$t_{HDS}$	HOLD Setup Time to Trailing Edge of CLK	120		-16	nsec
$t_{HDSH}$	HOLD Hold Time	0		0	nsec
$t_{INS}$	INTR Setup Time to Falling Edge of CLK (M1, T1 only). Also RST and TRAP	150		-56	nsec
$t_{INH}$	INTR Hold Time	0			nsec

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---

**ERROR MESSAGES**

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Command and execution errors are displayed at the console terminal. Command errors are indicated by pointing to the error location in the command line and displaying an error code message. The following examples present a typical error message:

```
D > BIES      W=20          ** ERROR FF **
    ^

D > DUMP      30      10    ** ERROR 14 **
                   ^

D > EXAM      4P          ** ERROR 02 **
                   ^
```

where: ERROR #FF = INVALID COMMAND

ERROR #14 = LOWER ADDRESS IS NOT LOWER THAN  
OR EQUAL TO UPPER ADDRESS

ERROR #02 = INVALID PARAMETER

Execution errors that occur during emulation processing may also indicate other types of error information

The complete description of all error conditions that are presented for a given error code number is provided in Appendix A of the 9508 MicroSystem Emulator Manual.

## 8085 INSTRUCTION SET

## OPCODE INDEX OF INSTRUCTIONS

The 8085 Emulator executes all legal opcodes only. Unimplemented opcodes are not detected.

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	2B	DCX H	56	MOV D,M	81	ADD C	AC	XRA H	D7	RST 2
01	LXI B,D16	2C	INR L	57	MOV D,A	82	ADD D	AD	XRA L	D8	RC
02	STAX B	2D	DCR L	58	MOV E,B	83	ADD E	AE	XRA M	D9	—
03	INX B	2E	MVI L,D8	59	MOV E,C	84	ADD H	AF	XRA A	DA	JC Adr
04	INR B	2F	CMA	5A	MOV E,D	85	ADD L	B0	ORA B	DB	IN D8
05	DCR B	30	—	5B	MOV E,E	86	ADD M	B1	ORA C	DC	CC Adr
06	MVI B,D8	31	LXI SPD 16	5C	MOV E,H	87	ADD A	B2	ORA D	DD	—
07	RLC	32	STA Adr	5D	MOV E,L	88	ADC B	B3	ORA E	DE	SBI D8
08	—	33	INX SP	5E	MOV E,M	89	ADC C	B4	ORA H	DF	RST 3
09	DAD B	34	INR M	5F	MOV E,A	8A	ADC D	B5	ORA L	E0	RPO
0A	LDAX B	35	DCR M	60	MOV H,B	8B	ADC E	B6	ORA M	E1	POP H
0B	DCX B	36	MVI M,D8	61	MOV H,C	8C	ADC H	B7	ORA A	E2	JPO Adr
0C	INR C	37	STC	62	MOV H,D	8D	ADC L	B8	CMP B	E3	XTHL
0D	DCR C	38	—	63	MOV H,E	8E	ADC M	B9	CMP C	E4	CPO Adr
0E	MVI C,D8	39	DAD SP	64	MOV H,H	8F	ADC A	BA	CMP D	E5	PUSH H
0F	RRC	3A	LDA Adr	65	MOV H,L	90	SUB B	BB	CMP E	E6	ANI D8
10	—	3B	DCX SP	66	MOV H,M	91	SUB C	BC	CMP H	E7	—
11	LXI D,D16	3C	INR A	67	MOV H,A	92	SUB D	BD	CMP L	E8	RPE
12	STAX D	3D	DCR A	68	MOV L,B	93	SUB E	BE	CMP M	E9	PCHL
13	INX D	3E	MVI A,D8	69	MOV L,C	94	SUB H	BF	CMP A	EA	JPE Adr
14	INR D	3F	CMC	6A	MOV L,D	95	SUB L	C0	RNZ	EB	XCHG
15	DCR D	40	MOV B,B	6B	MOV L,E	96	SUB M	C1	POP B	EC	CPE Adr
16	MVI D,D8	41	MOV B,C	6C	MOV L,H	97	SUB A	C2	JNZ Adr	ED	—
17	RAL	42	MOV B,D	6D	MOV L,L	98	SBB B	C3	JMP Adr	EE	XRI D8
18	—	43	MOV B,E	6E	MOV L,M	99	SBB C	C4	CNZ Adr	EF	RST 5
19	DAD D	44	MOV B,H	6F	MOV L,A	9A	SBB D	C5	PUSH B	F0	RP
1A	LDAX D	45	MOV B,L	70	MOV M,B	9B	SBB E	C6	ADI D8	F1	POPPSW
1B	DCX D	46	MOV B,M	71	MOV M,C	9C	SBB H	C7	RST 0	F2	JP Adr
1C	INR E	47	MOV B,A	72	MOV M,D	9D	SBB L	C8	RZ	F3	DI
1D	DRC E	48	MOV C,B	73	MOV M,E	9E	SBB M	C9	RET	F4	CP Adr
1E	MVI E,D8	49	MOV C,C	74	MOV M,H	9F	SBB A	CA	JZ Adr	F5	PUSH PSW
1F	RAR	4A	MOV C,D	75	MOV M,L	A0	ANA B	CB	—	F6	ORI D8
20	—	4B	MOV C,E	76	HLT	A1	ANA C	CC	CZ Adr	F7	RST 6
21	LXI H,D16	4C	MOV C,H	77	MOV M,A	A2	ANA D	CD	CALL Adr	F8	RM
22	SHLD Adr	4D	MOV C,L	78	MOV A,B	A3	ANA E	CE	ACI D8	F9	SPHL
23	INX H	4E	MOV C,M	79	MOV A,C	A4	ANA H	CF	RST 1	FA	JM Adr
24	INR H	4F	MOV C,A	7A	MOV A,D	A5	ANA L	D0	RNC	FB	EI
25	DCR H	50	MOV D,B	7B	MOV A,E	A6	ANA M	D1	POP D	FC	CM Adr
26	MVI H,D8	51	MOV D,C	7C	MOV A,H	A7	ANA A	D2	JNC Adr	FD	—
27	DAA	52	MOV D,D	7D	MOV A,L	A8	XRA B	D3	OUT D8	FE	CPI D8
28	—	53	MOV D,E	7E	MOV A,M	A9	XRA C	D4	CNC Adr	FF	RST 7
29	DAD H	54	MOV D,H	7F	MOV A,A	AA	XRA D	D5	PUSH D		
2A	LHLD Adr	55	MOV D,L	80	ADD B	AB	XRA E	D6	SUI D8		

NOTES: D8 = constant, or logical/arithmetic expression that evaluates to an 8-bit data quantity.  
D16 = constant, or logical/arithmetic expression that evaluates to a 16-bit data quantity.  
Adr = 16-bit address

7604

---

**ORDERING INFORMATION**


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The 8085 Emulator Option for the 9508 MicroSystem Emulator is ordered by the following order number:

<u>Order Number</u>	<u>Description</u>	<u>Price</u>
XE8085	8085 In-circuit Emulator Option for the 9508 MicroSystem Emulator	See current price list

The Emulator Option parts are listed in table D-1. The parts may be ordered separately, directly from MILLENNIUM or from the MILLENNIUM sales office or distributor serving your locality. See the current price list for the price of each item.

**Table D-1. Emulator Option Parts List**

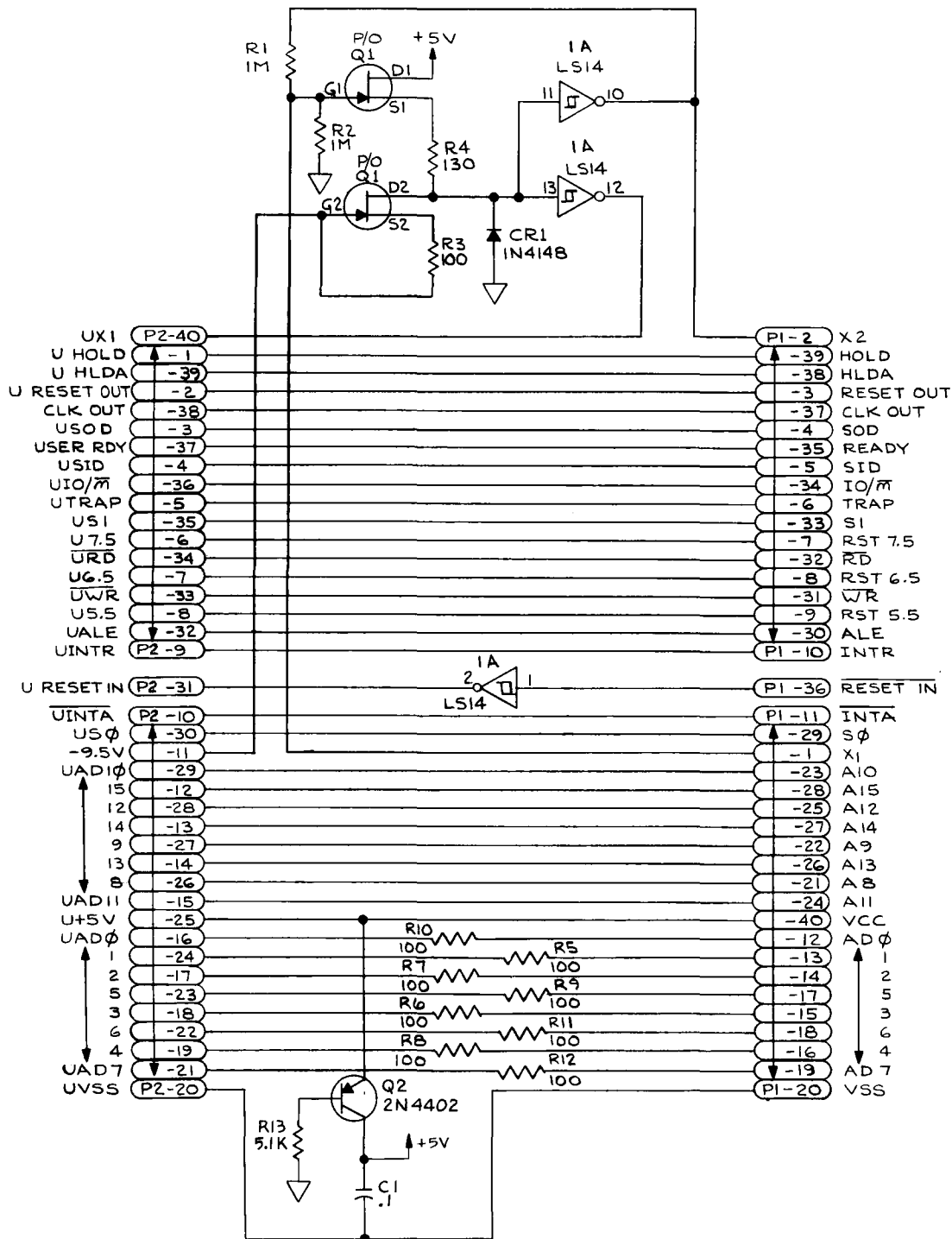
Part Number	8085 Emulator printed circuit board assembly
13000108	8085 Emulator printed circuit board assembly
15000109	8085 Emulator Pod assembly
15000054	8085 Emulator Probe
13000236-04	8085 Emulator Dependent PROM printed circuit board assembly
87000076	9508 MicroSystem Emulator Users Manual, Addendum for 8085 Emulator Option

Table D-2 lists the sources of accessory equipment for the emulator option.


**Table D-2. Accessory Equipment Sources**

Equipment	Source	Vendor Part Number
40-Pin header, male/male	Augat	640-AG1
40-Pin header, male/female	Augat	540-AG10D

DWG. NO. 12000054		REV. E	1
REVISIONS			
ZONE	REV	DESCRIPTION	DATE
	51	PILOT RELEASE ECO 1265	12/9/78
	A	PROD RELEASE PER ECO 1515	5/23/79
	B	PER ECO 1573	7/13/79
	C	PER ECO 1948	6-28-80
	D	PER ECO 2046	7-29-80
	E	REV ROLL ONLY ECO 2095	9-21-81



NOTES: UNLESS OTHERWISE SPECIFIED.  
 1 RESISTOR VALUES ARE IN OHMS 1/8W, ±5%  
 2 CAPACITOR VALUES ARE IN MICROFARADS

QTY REQD		CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES = / .XX ± / °			CONTRACT NO.		
MATERIAL			APPROVALS	DATE	 <b>Millennium Systems Inc.</b>  <b>SCHEMATIC, P8085</b>
FINISH			DRAWN <i>Charles Brown</i>	10-9-78	
NEXT ASSY			CHECKED <i>[Signature]</i>	10-9-78	
USED ON			ISSUED <i>[Signature]</i>	5/23/79	SIZE FSCM NO. <b>D</b> DWG. NO. <b>12000054</b> REV. <b>E</b>
APPLICATION			DO NOT SCALE DRAWING		
			SCALE NONE SHEET 1 OF 1		



8

7

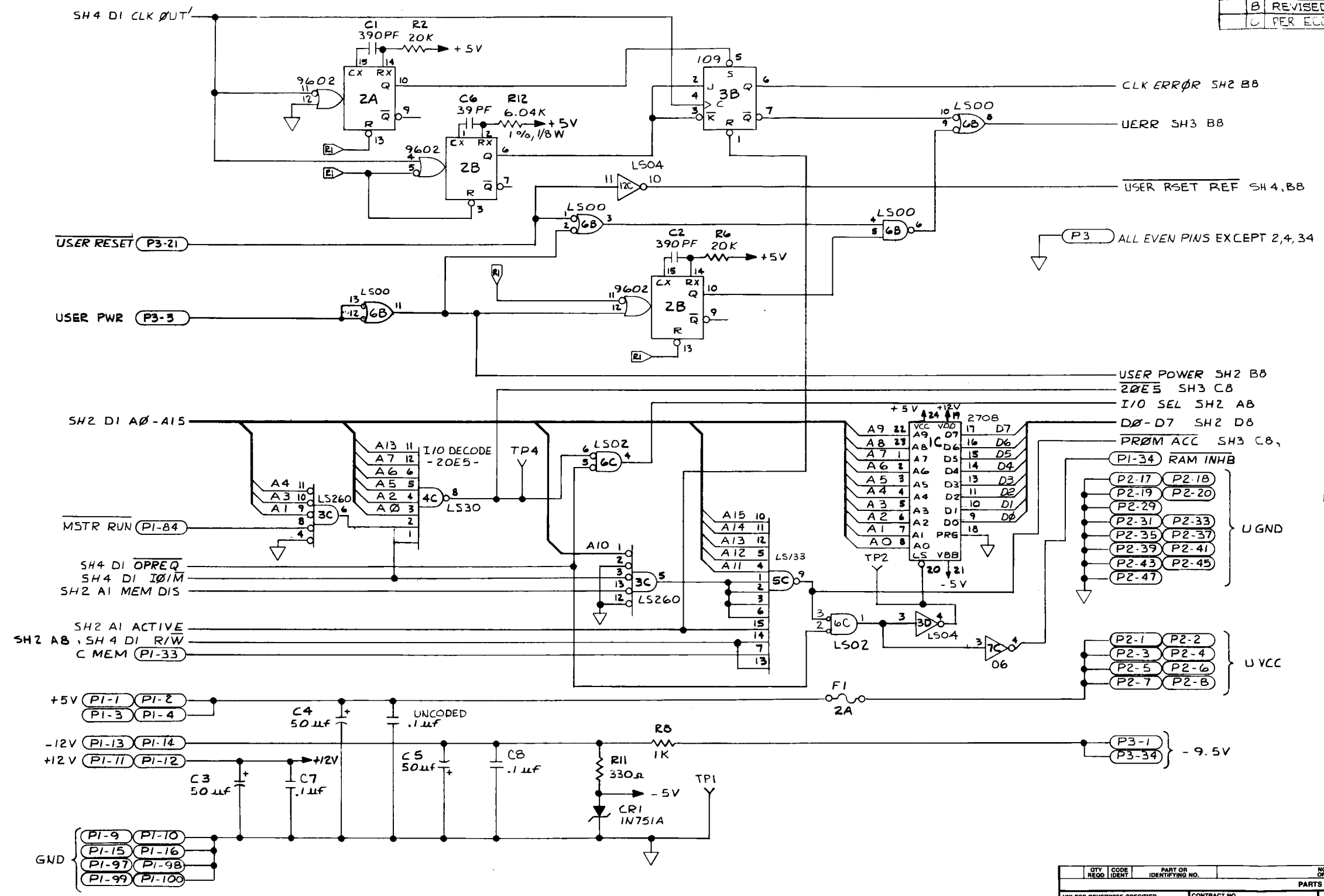
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4

3

DWG. NO.	12000108	REV.	1	1
REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
A	PRODRELEASE	PER ECO 1515	5/23/79	6/2/80
B	REVISED	PER ECO 1657	1-16-80	09/1
C	PER ECO	2.610. REV. ROLL ONLY	5/3/79	6/18/81



NOTES: UNLESS OTHERWISE SPECIFIED.

1. RESISTOR VALUES ARE OHMS AND ARE 1/4W, 5%.
2. CAPACITOR VALUES ARE IN MICROFARADS.
3. SYMBOL  IS A 5.6K. COMMON PULL-UP RESISTOR.
4. RESISTOR PACKS ARE 100 OHMS.

QTY	CODE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
PARTS LIST				
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ± °				
CONTRACT NO.		APPROVALS DATE		
13000108		P. DALE 8-25-78		
NEXT ASSY		CHECKED: 5-30-79		
USED ON		ISSUED: 5/29/79		
APPLICATION		DO NOT SCALE DRAWING		
MILLENNIAL SYSTEMS INC.		SCHEMATIC, USA 8085 EMULATOR		
SIZE		FSCM NO.		
D		DWG. NO. 12000108		
SCALE NONE		SHEET 1 OF 4		

8

7

6

5

4

3

DWG. NO. 12000108

2

REV

1

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	1	SEE SH 1		

D

D

C

C

B

B

A

A

SH 3 B1 BUS ADDR EN

EAD 15 P2-28  
14 P2-27  
13 P2-26  
12 P2-25  
11 P2-24  
10 P2-23  
9 P2-22  
EAD 8 P2-21

SH 4 A1 ALE

SH 1 C3 D0-D7

SH 3 D8, D4

D7 PI-43  
D6 PI-42  
D5 PI-41  
D4 PI-40

SH 3 C1 BUS IN

SH 3 C1 BUS OUT

D3 PI-39  
D2 PI-38  
D1 PI-37  
D0 PI-36

SH 3 A1 JMP HI

SH 3 A1 JMP LO

SH 3 C1 85 RD

SH 3 C1 85 WR

SH 4 D1 FETCH

SH 1 C2 USER POWER

SH 1 D2 CLK ERROR

SH 4 B1 HALT

SH 4 B1 USER PAUSE

SH 3 B1 RUN

SH 4 B1 SYS RST

E5.5 P3-17

E6.6 P3-15

E5.0 P3-27

SH 3 D1 UDTS

SH 4 D1 R/W

SH 1 C2 I/O SEL

SH 3 A1 JMP INST

SH 4 C1 WRP

RESET PI-59

SLV IN P PI-79

PI-72

W3  
W2+5V  
5.6K  
R15

A15 9  
A14 11  
A13 13  
A12 1  
A11 3  
A10 5

LS04  
8 A15  
10 A14  
12 A13  
2 A12  
4 A11  
6 A10

A9 13  
A8 11  
A7 9  
A6 1  
A5 3  
A4 5

LS04  
12 A9  
10 A8  
8 A7  
2 A6  
4 A5  
6 A4

A3 13  
A2 11  
A1 9  
A0 1

LS04  
12 A3  
10 A2  
8 A1  
2 A0

JMP ADDRESS

LS244

A15 2  
A14 4  
A13 6  
A12 8  
A11 17  
A10 15  
A9 13  
A8 11

A7 2  
A6 4  
A5 6  
A4 8  
A3 17  
A2 15  
A1 13  
A0 11

EAD 15  
EAD 14  
EAD 13  
EAD 12  
EAD 11  
EAD 10  
EAD 9  
EAD 8

LS244  
18  
16  
14  
12  
10  
8  
6  
4  
2  
1

D7 18  
D6 17  
D5 14  
D4 13  
D3 3  
D2 4  
D1 7  
D0 8

D7 18  
D6 17  
D5 14  
D4 13  
D3 3  
D2 4  
D1 7  
D0 8

D3 2  
D2 3  
D1 4  
D0 5  
D7 18  
D6 17  
D5 14  
D4 13  
D3 3  
D2 4  
D1 7  
D0 8

D7 11  
D6 4  
D5 9  
D4 10  
D3 8  
D2 5  
D1 2  
D0 6

D7 11  
D6 4  
D5 9  
D4 10  
D3 8  
D2 5  
D1 2  
D0 6

D7 11  
D6 4  
D5 9  
D4 10  
D3 8  
D2 5  
D1 2  
D0 6

D7 11  
D6 4  
D5 9  
D4 10  
D3 8  
D2 5  
D1 2  
D0 6

PI-32 A15  
PI-31 A14  
PI-30 A13  
PI-29 A12  
PI-28 A11  
PI-27 A10  
PI-26 A9  
PI-25 A8

PI-24 A7  
PI-23 A6  
PI-22 A5  
PI-21 A4  
PI-20 A3  
PI-19 A2  
PI-18 A1  
PI-17 A0

P2-16 AD7  
P2-15 AD6  
P2-14 AD5  
P2-13 AD4

P2-12 AD3  
P2-11 AD2  
P2-10 AD1  
P2-9 AD0

MEM INST SH 3 D8

M0 SH 3 B8

P3-4 OPEN LOOP

P3-2 WAIT DIS

MSTR RD SH 3 CB

MEM DIS SH 1 B8

DEBUG SEQ SH 4 AB

INT EN SH 3 D8

M0 SH 3 CB

M1 SH 3 CB

ACTIVE SH 3 D8, SH 4 CB,

SH 1 B7

MODE 0 SH 3 B8

MSTR WR SH 3 CB

P3-29 MODE 0

8

7

6

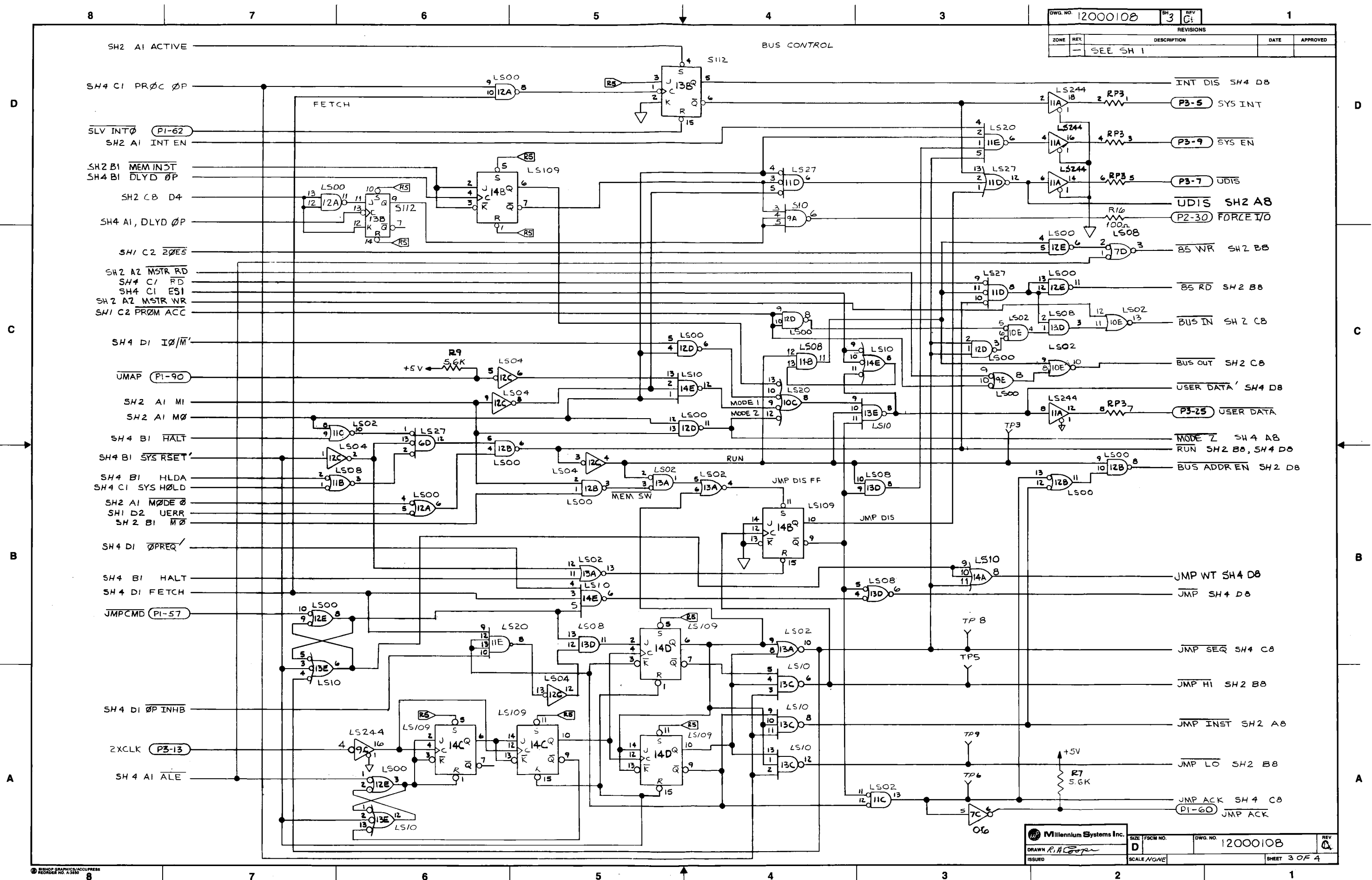
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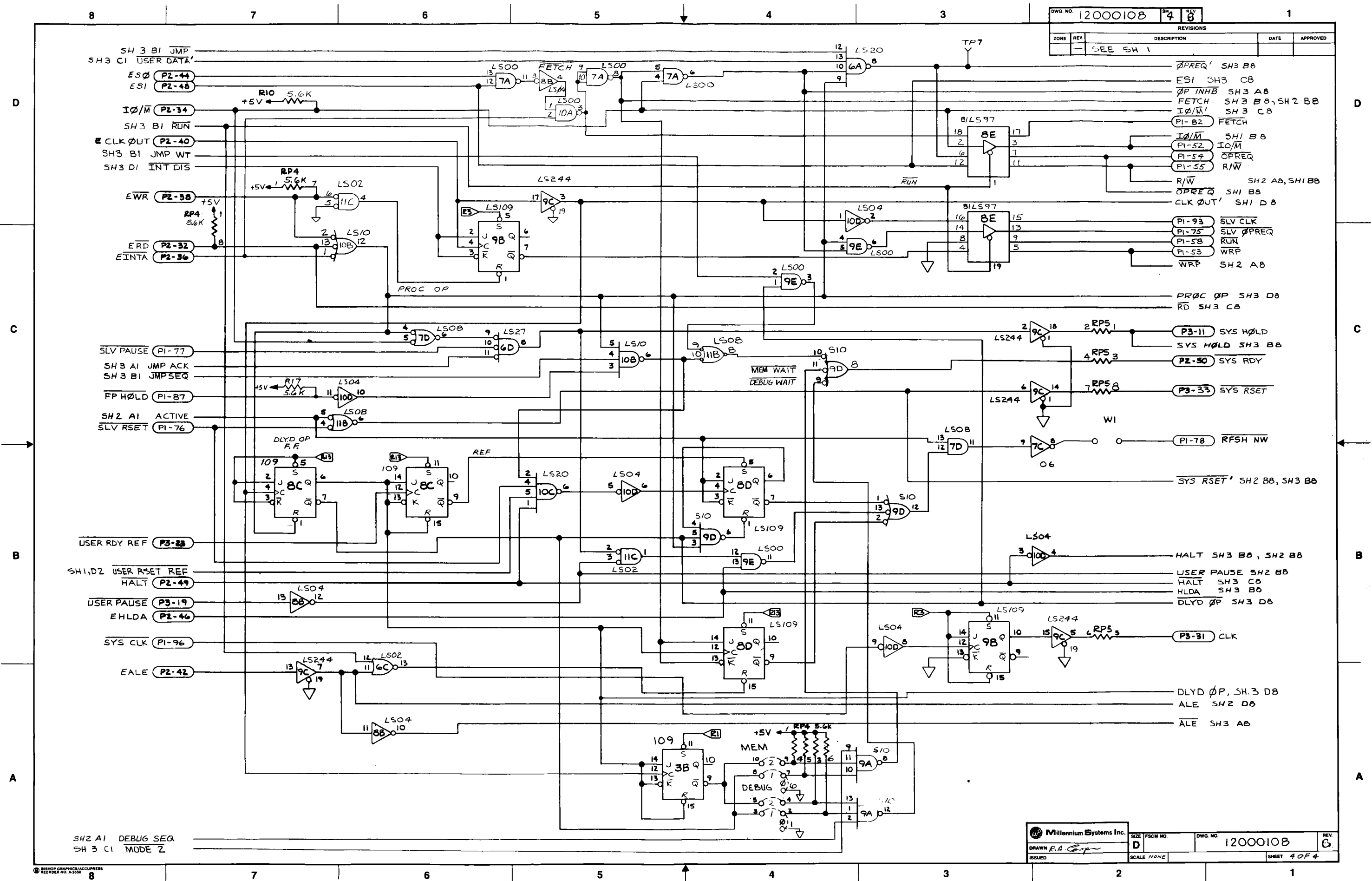
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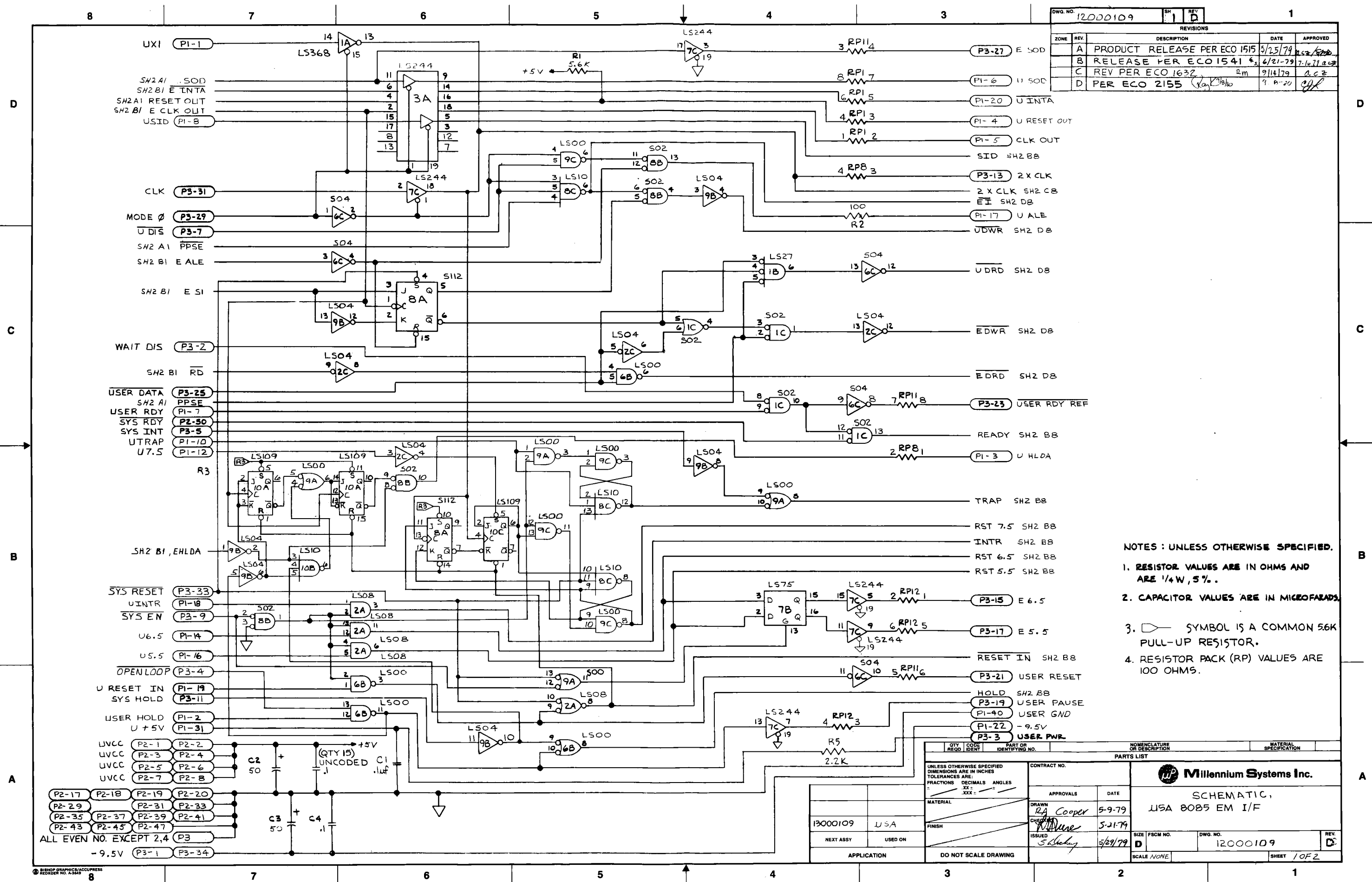
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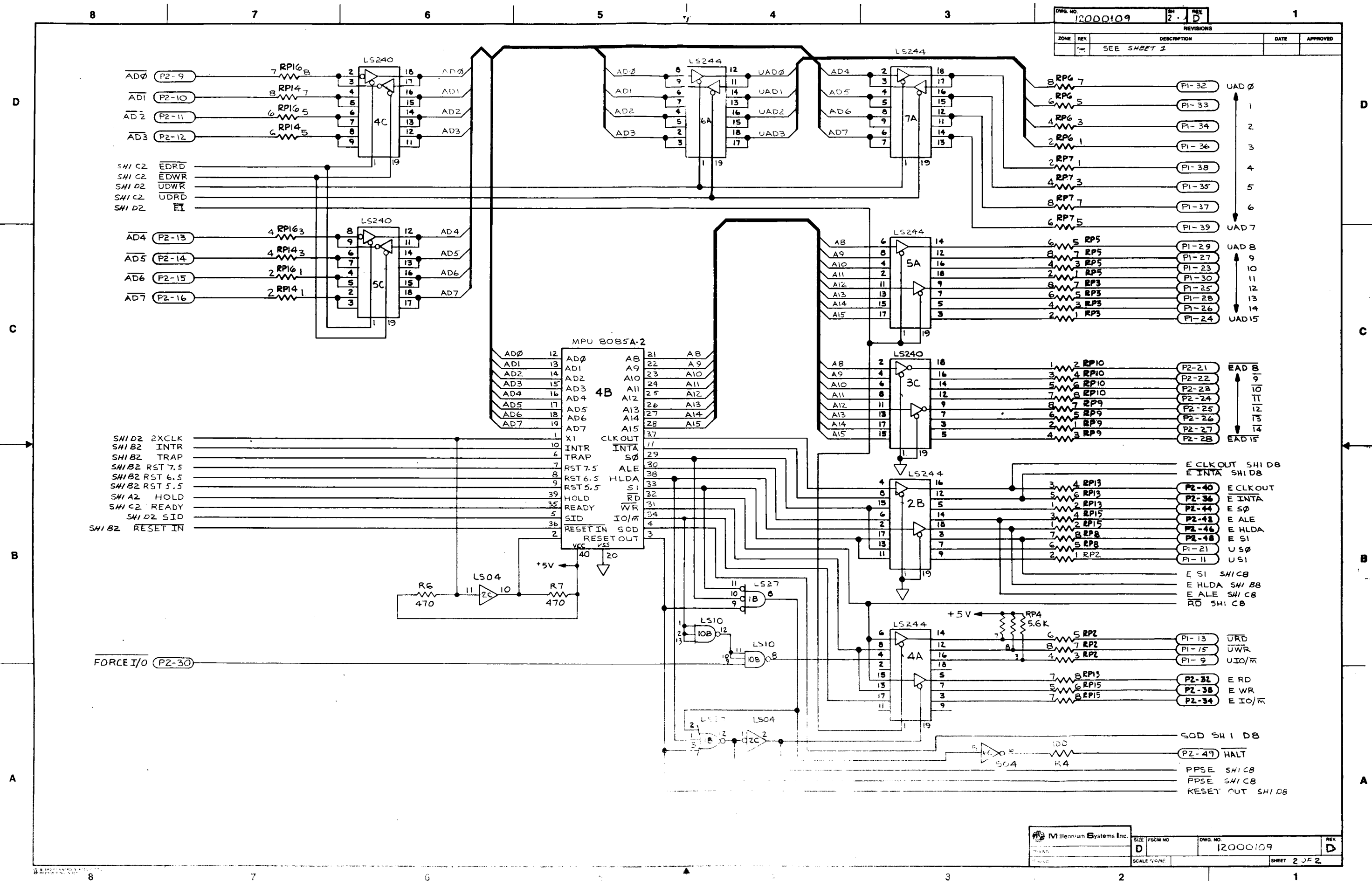
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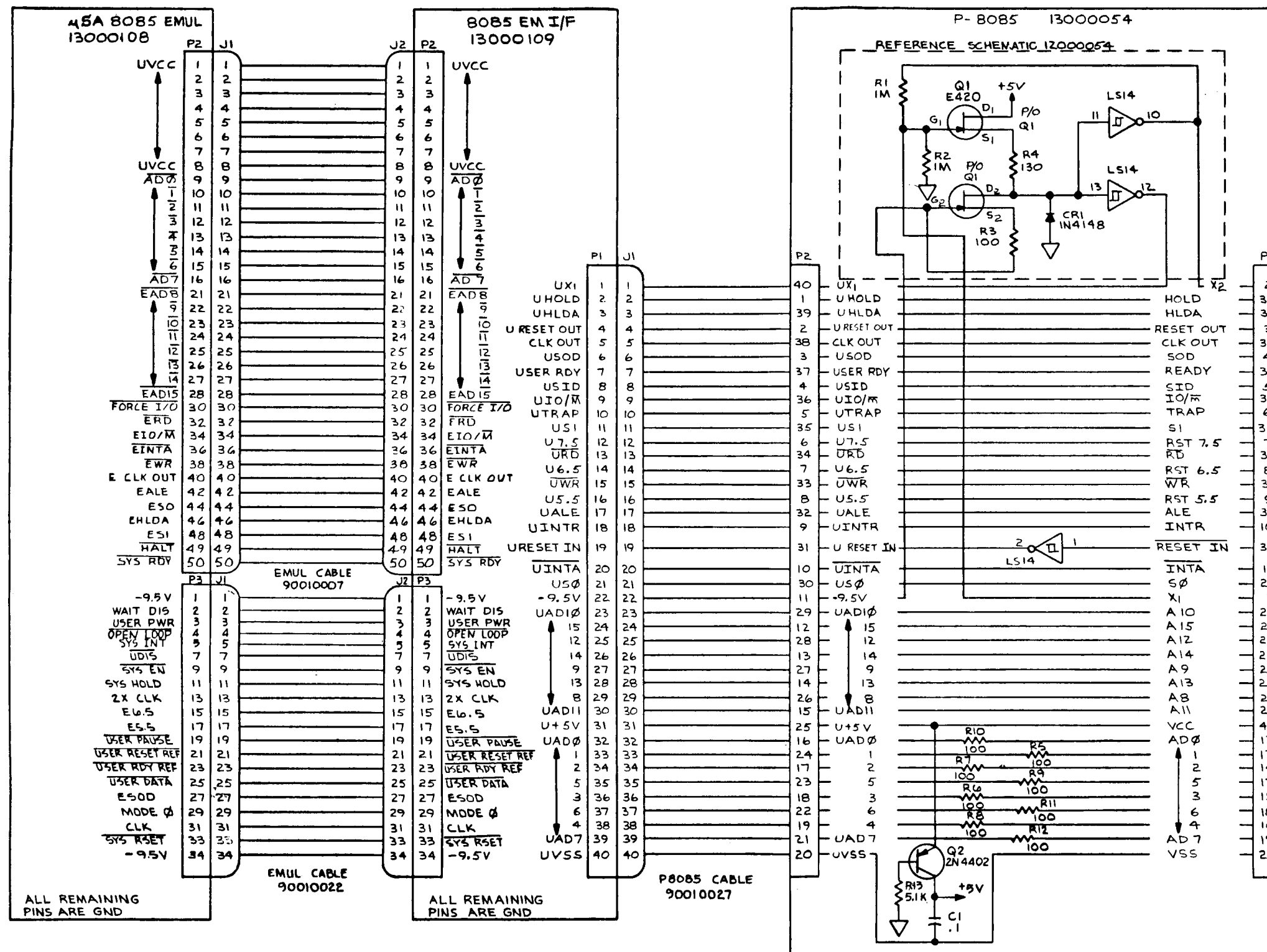
1












QTY REQD		CODE IDENT		PART ON IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION		MATERIAL SPECIFICATION	
PARTS LIST									
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XXX ±       XXX ±       XXX ±				CONTRACT NO.		 <b>Millennium Systems Inc.</b>			
MATERIAL				APPROVALS		DATE		WIRING SCHEMATIC, MSA 8085 OPTION	
				DRAWN <i>Rmcer</i>		5-24-79			
FINISH				CHECKED <i>G. Kelly</i>		5-30-79		SIZE PDSCH NO. DWG. NO. REV <b>D</b> <b>12000124</b> <b>8</b>	
				ISSUED <i>S. Kelly</i>		5-28-79			
APPLICATION				DO NOT SCALE DRAWING					
NEXT ASSY		USED ON		SCALE NONE					

9508 MICROSYSTEM EMULATOR  
USERS MANUAL ADDENDUM  
8085 EMULATOR OPTION

Publication No. 87000076  
June 1981  
Release 1.0

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SPECIFIC COMMENTS AND CORRECTIONS

Reference	Page
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_____	_____
_____	_____
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_____	_____
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Cupertino, Calif. 95014  
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MILLENNIUM SYSTEMS, INC.

---

SOFTWARE/SYSTEM PROBLEM REPORT

---

1. DATE

2. CUSTOMER INFORMATION

NAME OF COMPANY

NAME OF EMPLOYEE

ADDRESS

CITY/STATE/ZIP CODE

TELEPHONE #

EXTENSION

3. HARDWARE/SOFTWARE CONFIGURATION

9520

SERIAL #

VOLTAGE

HERTZ

MEMORY SIZE: 64K?

112K?

OPERATION SYSTEM

VERSION #

9508

SERIAL #

VERSION #

16K?

EMULATOR Z80

OTHER

8080

6800

8085

6801

8048/49

6802

8021

6809

8041

4. HOW ARE THE HOST, 9508, AND UNIT UNDER TEST CONNECTED? PLEASE INDICATE PORT NUMBERS

5. COMMAND OR PROGRAM WHERE PROBLEM OCCURS

NAME

VERSION #

6. AFTER POWER ON/RESET, WHAT COMMAND OR SERIES OF COMMANDS WILL REPRODUCE THE ERROR.

7. DESCRIPTION OF THE ERROR

8. PLEASE ATTACH AS MUCH OF THIS OTHER HELPFUL INFORMATION AS POSSIBLE

SOURCE FILES

OBJECT FILES

COMMAND FILES

LISTINGS

CONSOLE HARDCOPY

(ATTACH ADDITIONAL SHEETS AS REQUIRED)

MILLENNIUM SYSTEMS, INC.

---

PRODUCT ENHANCEMENT REQUEST

---

1. DATE

2. CUSTOMER INFORMATION

NAME OF COMPANY  
NAME OF EMPLOYEE  
ADDRESS  
PHONE # \_\_\_\_\_

EXT. \_\_\_\_\_

3. PRODUCT NAME (9508, 9520, 9516, 9580, ETC.)

4. DESCRIPTION OF ENHANCEMENT

5. DESCRIPTION OF HOW ENHANCEMENT WOULD BE USED

6. HOW LONG BEFORE YOU MUST HAVE THIS ENHANCEMENT?

NOW \_\_\_\_\_  
6 MONTHS \_\_\_\_\_  
1 YEAR \_\_\_\_\_  
2 YEARS \_\_\_\_\_

7. WHAT SHOULD BE THE COST OF THIS ENHANCEMENT?

(ATTACH ADDITIONAL SHEETS AS REQUIRED)