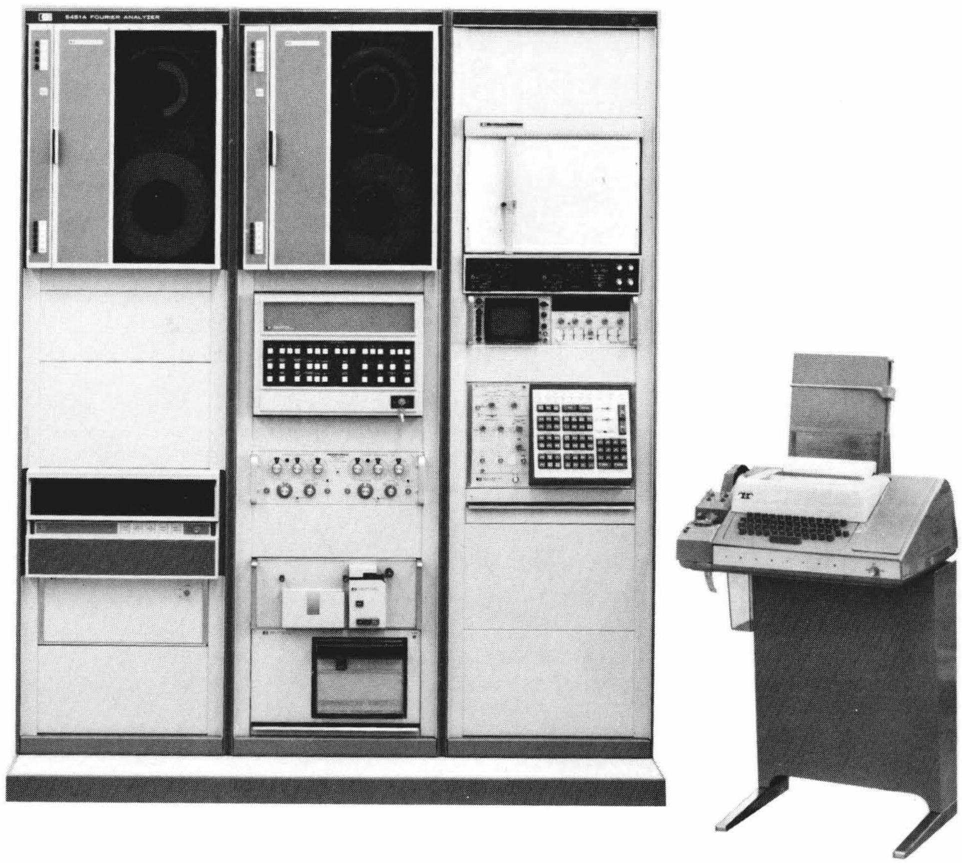
SYSTEM SERVICE MANUAL

FOURIER ANALYZER SYSTEM

5451A



NOTE:
Some units shown in this photograph are not part of the standard 5451A System, and are supplied as Options.

05451-90042

HEWLETT hp PACKARD

FOURIER ANALYZER SYSTEM

5451A

PRINTED: JUNE 1973

05451-90042 PRINTED IN USA

HEWLETT PACKARD

TABLE OF CONTENTS

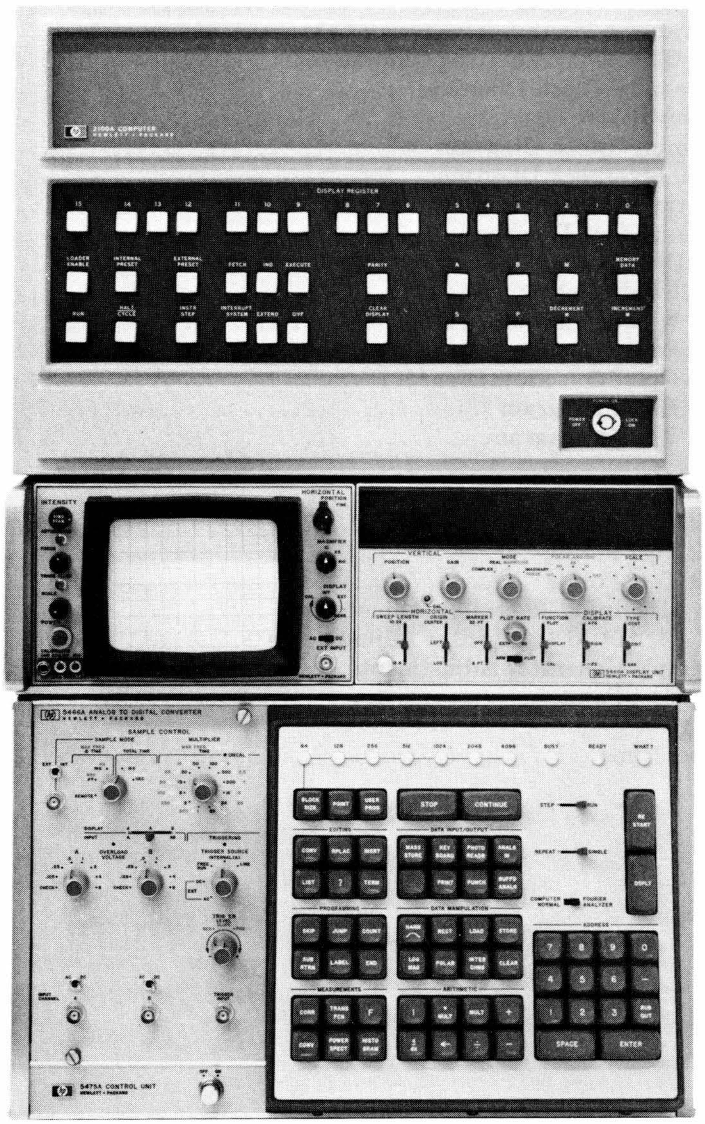
TABLE OF CONTENTS *(Cont'd)*

TABLE OF CONTENTS *(Cont'd)*

LIST OF TABLES

LIST OF FIGURES

Figure 1-1. Model 5451A Fourier Analyzer System



NOTE: Although not shown, a Teleprinter is a mandatory option for the 5451A System.

SECTION I
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides service information for the HP 5451A Fourier Analyzer System. It includes operating considerations, operational checkout procedures, circuit card adjustments, and troubleshooting information to the circuit card level. Applicable documents such as unit hardware manuals, computer and peripheral equipment instruction manuals are listed in the FOREWORD of this manual. Refer to the unit manuals for circuit card schematics and parts lists.

1.2 SYSTEM DESCRIPTION

The HP 5451A Fourier Analyzer System performs statistical analysis using Fourier analysis techniques. The system uses a computer for processing and storage of input data. The analyzer can take on a variety of configurations made up from a list of customer-selected add-on options. (See *Figure 1-1.*)

1.3 BASIC FOURIER ANALYZER SYSTEM AND REQUIRED OPTIONS

The specific units and required options to make up a minimum functional Fourier Analyzer System (5451A) are listed in *Table 1-1.* Additional information on available options can be obtained from any HP Sales or Service Office. Because of the wide variety of possible configurations, a System Configuration Notice is shipped with each system. The System Configuration Notice defines the equipment supplied, and the options and software included in each system. To perform the service and diagnostic routines described herein, the following minimum equipment is required:

5451A Basic Units (see *Table 1-1*)
2752A Teleprinter
2100A Computer with Switch Panel

1.4 INSTRUMENT IDENTIFICATION

1.4.1 Model Number and Name

Each unit in the standard Fourier Analyzer System is identified by model or specification number and name as a separate instrument; for example:

Specification H51-180AR Oscilloscope
Model 2100A Computer
Model 2748A Punched Tape Reader
Model 2752A Teleprinter
Model 5460A Display Plug-in Unit
Model 5466A ADC Plug-in Unit
Model 5475A Control Unit

1.4.2 Serial Numbers

Each Fourier Analyzer System is identified by a two-section system serial number (5451A-000). The number is found on a stick-on plate mounted on the inside rear of the system cabinet. The three-digit number is a serial number unique to each system, and the other portion provides the system model number.

Each unit including the computer and its peripherals, in the Fourier Analyzer System is identified by a two-section serial number on the rear panel of the unit. The serial number consists of nine

Table 1-1. 5451A Fourier Analyzer System Components

Description	HP Part Number	Quantity
BASIC UNITS		
Display Plug-in Unit	Model 5460A	1
Analog-to-Digital Converter (ADC) Plug-in	Model 5466A	1
2-channel, 10-bit	standard	
2-channel, 12-bit	5466A Opt. 001 (5451A Opt. 041)	
4-channel, 10-bit	5466A Opt. 002 (5451A Opt. 042)	
4-channel, 12-bit	5466A Opt. 003 (5451A Opt. 043)	
Control Unit (Keyboard and Power Supply)	Model 5475A	1
Oscilloscope Mainframe	Specif. H51-180	1
Microcircuit Interface Card Kit	HP 12566	3 (2-chan) or 2 (4-chan)
Computer (8K, EAU, DMA)	Model 2100A	1
Cable Assembly (Keyboard-Computer)	05451-60001	1
Cable Assembly (Display Unit-Computer)	05450-60002	1
Cable Assembly (ADC-Computer) (2-channel) (or) (4-channel)	05451-60002 05451-60004	1 1
Universal Interface Card (Replaces the HP 12566 Microcircuit Interface Card used for the ADC's interface, when an ADC with 4-channel capability is used; e.g., 5451A Options 042, 043, 044, and 045 are provided with two HP 12566's and one 12930.)	HP 12930	1
Cable Assembly (Control Unit-Computer)	05450-60004	1
REQUIRED OPTION		
Teleprinter and I/O Card	Model 2752A or 2754A and 12531 Kit	1
EXTENDED CAPABILITY OPTIONS		
Analog-to-Digital Converter (ADC) Plug-in	Model 5466A	(Replaces the "BASIC UNIT" above)
2-channel, 10-bit (wired and tested for future expansion to 4 channels—includes 4-channel interface card and cable)	5466A Opt. 006 (5451A Opt. 044)	

Table continues on next page.

Table 1-1. 5451A Fourier Analyzer System Components (Continued)

Description	HP Part Number	Quantity
EXTENDED CAPABILITY OPTIONS *(Continued)*		
Analog-to-Digital Converter (ADC) Plug-in *(Continued)*		(Replaces the "BASIC UNIT" above)
2-channel, 12-bit (wired and tested for future expansion to 4 channels—includes 4-channel interface card and cable).	5466A Opt. 007 (5451A Opt. 045)	
2-channel, 10- or 12-bit, Remote Programming (modifies 5475A Control Unit—ADC already wired to enable remote programming). Adds one HP 05466-60005 Cable Assembly, and one HP 12566 Microcircuit Interface Card.	5451A Opt. 060	1
4-channel, 10- or 12-bit, Remote Programming (modifies 5475A Control Unit—ADC already wired to enable remote programming). Adds one HP 05466-60006 Cable Assembly, and two HP 12566 Microcircuit Interface Cards.	5451A Opt. 061	1
Cabinet	2940B	1
Fast Processor	Model 5470A or 5471A	1
Photoreader	Model 2748A or 2758A	1
Tape Punch	Model 2753A, 2895A, or 8100A	1
Magnetic Tape Unit	Model 7970B	1
Cassette Tape I/O	Model 85001A	1
Magnetic Disc Unit	Model 7900A	1
Analog Plotter	Model 7004B or 7034A	1
Data Acquisition Multiplexer		1

1.4.2 Serial Numbers *(Continued)*

digits and an alpha character (0000A00000). The four-digit prefix portion is used to document changes. The alpha character denotes the country of origin; i.e., A = U.S.A., E = England, G = West Germany, J = Japan, and U = United Kingdom. The five-digit suffix of the serial number is unique to each instrument. Include complete serial number, model number and instrument name in correspondence about any unit in your Fourier Analyzer System.

1.5 CATHODE RAY TUBE WARRANTY

The Cathode Ray Tube (CRT) is covered by a warranty separate from the rest of the system. The CRT warranty and warranty claim form are located in the H51-180 Oscilloscope manual. Should CRT fail within time specified on warranty, return CRT with warranty form completed.

1.6 STORAGE AND SHIPMENT

1.6.1 Packaging

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Your Hewlett-Packard Sales and Service Office can provide packing material such as that used for original factory packaging. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

1.6.2 Environment

Conditions during storage and shipment should normally be limited as follows:

a. Maximum altitude: 25,000 ft.
b. Maximum temperature: +167°F (+75°C).
c. Minimum temperature: -40°F (-40°C).

1.7 SYSTEM INTERCONNECTION

Figures 1-2 and *1-3* show system interconnection and cable location for each of the computers used in the Fourier Analyzer System.

1.8 MICROCIRCUIT CARD STRAPPING

The Computer Subsystem uses Interface Cards, in the Computer's I/O slots, to interface the ADC, Display, and Keyboard units. These cards, and the required jumper or switch settings on them, are listed in Table 1-2.

Table 1-2. 5451A--Standard Interfaces

Unit Interfaced	ADC (data) (2-channel)	ADC (data) (4-channel)	Display	Keyboard	ADC (Remote programming)
Interface Card	12566 Microcircuit	12930 Universal	12566 Microcircuit	12566 Microcircuit	12566 Microcircuit
Jumper or Switch settings for this card	W1 = A W2 = B W3 = B W4 = B W5-W8 removed W9 = A	Position Number — S1 S2 S3 85 — 2 5 0 87 — 1 4 8 97 — 2 4 0 102 — 2 7 0 106 — 1 6 0	W1 = A W2 = C W3 = B W4 = B W5-W8 removed W9 = A	W1 = A W2 = C W3 = B W4 = B W5-W8 removed W9 = A	W1 = A W2 = B W3 = B W4 = B W5-W8 removed W9 = A

1.9 SERVICE AIDS

1.9.1 Service Kit

The service kit contains most-often-needed replaceable parts (see *Table 1-3*) for the following Fourier Analyzer system units:

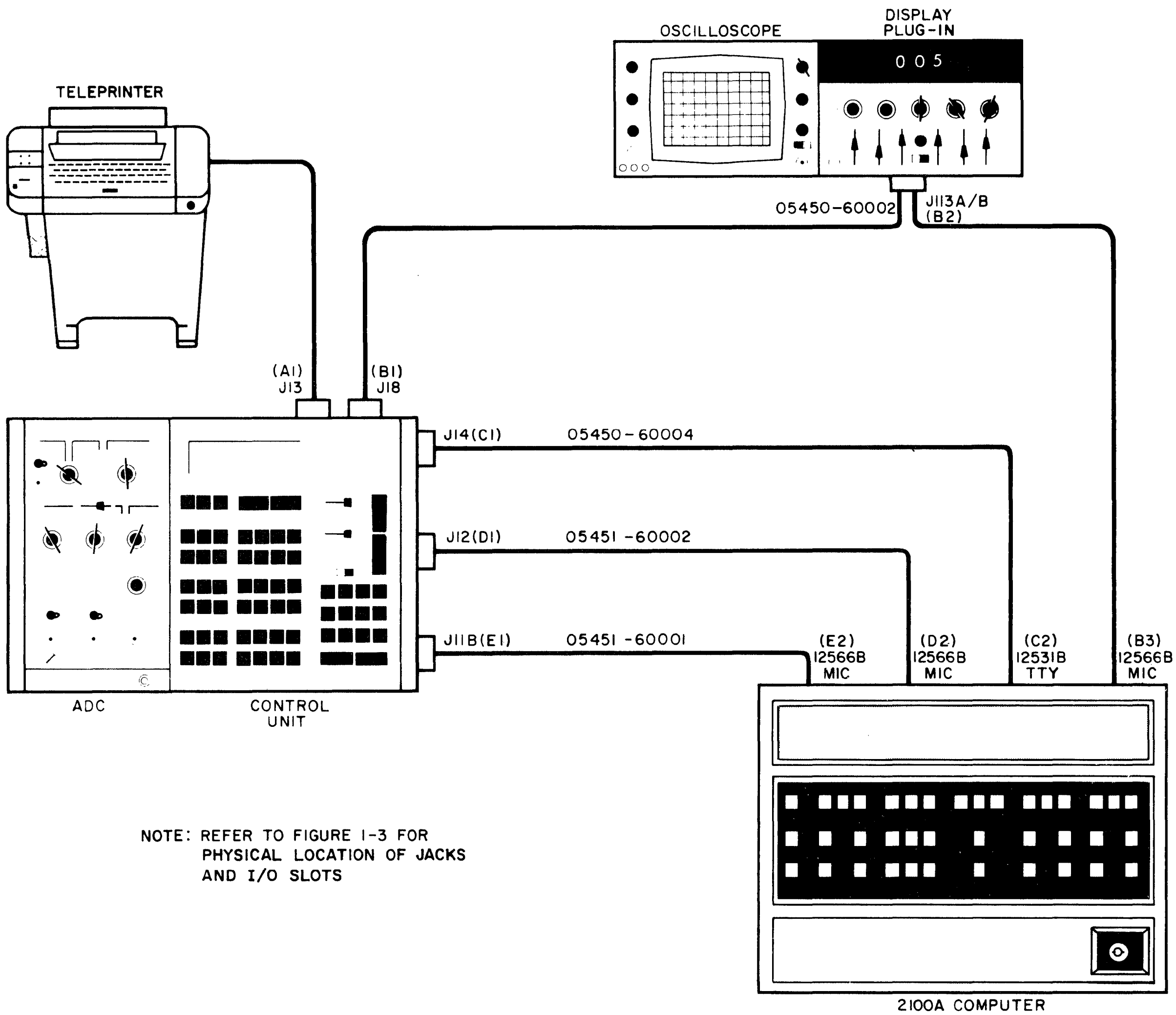
5460A Display Plug-in Unit
5466A, ADC Plug-in Unit
5475A Control Unit

For circuit card schematics and parts lists, refer to the applicable unit service manual. The H51-180 (or H51-181) Oscilloscope Mainframe is a standard 180-series oscilloscope with modifications to permit signal interface with the Display Plug-in. The oscilloscope may be serviced in the same manner as any other 180 series with the exception of the connectors added for the Display Plug-in. Information concerning these connectors is provided in the Display Unit Wiring Diagram in Section II of this manual.

1.9.1 Service Kit *(Continued)*

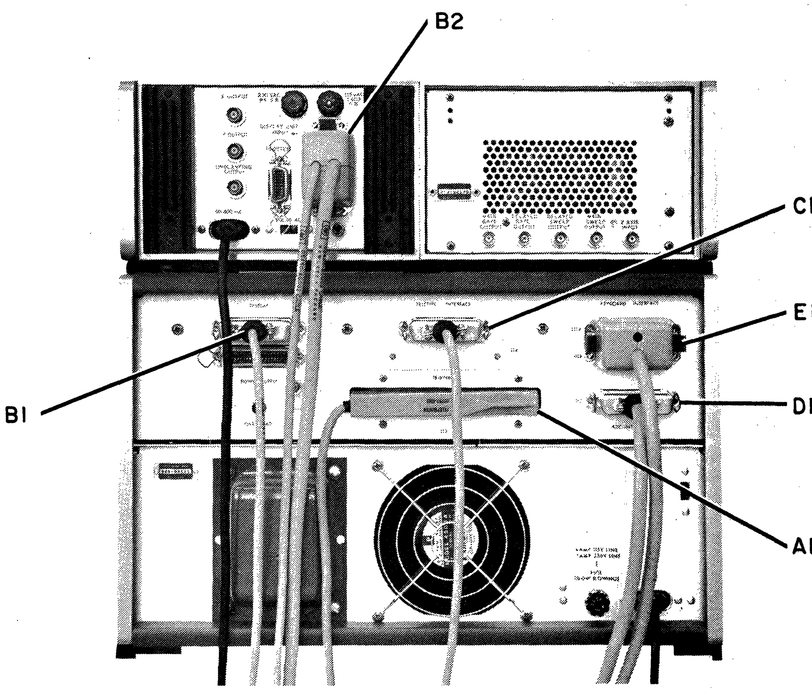
Contact your nearest Hewlett-Packard Sales and Service Office, listed in the back of this book, for information concerning on-site service utilizing the service kit, or purchase of such a kit for your facility.

Figure 1-2. System Interconnection Diagram



Label	Cable	Connection
A1	Teleprinter	Control Unit J13 to Teleprinter
B1, B2, B3	05450-60002	Control Unit J18 to Display Plug-in J112A/B to Computer MIC I/O Slot
C1, C2	05450-60004	Control Unit J14 to Computer TTY I/O Slot
D1, D2	05451-60002	Control Unit J12 to Computer MIC I/O Slot
E1, E2	05451-60001	Control Unit J11B to Computer MIC I/O Slot

Figure 1-3. System Cable Location



REFER TO OPPOSITE PAGE FOR CABLE LABEL TABLE

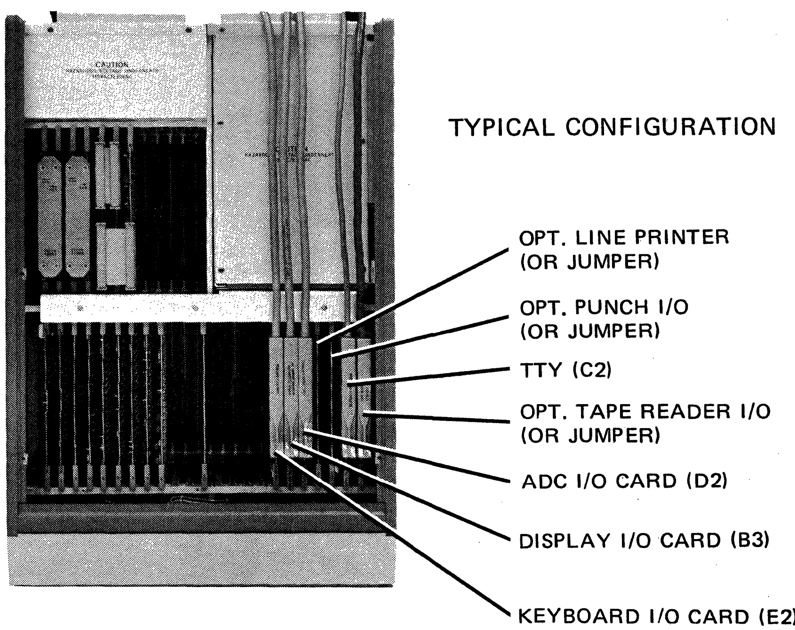


Table 1-3. Service Kit

GENERAL

A service kit should include the items listed below. The kit contents are ordered separately by using the HP Part or Assembly Numbers shown.

	HP ASSEMBLY NUMBER
Extender Kit. Includes 10603A Display Plug-in Extender Unit. Enables 5460A to be operated outside H51-180AR plug-in compartment. Extender Cards (1) 5060-0630 (2) 5060-0049	05450-60006
ADC Extender Cable. Enables 5466A to be operated outside 5475A plug-in compartment	10628A
Replacement Board Kits. Kits include boards listed below. Where both new and rebuilt boards are available, the kit may contain either type of board, but not both.	For 5460A: 10681A For 5466A: 10683A For 5475A: 10684A
Isolated Spares Kit. Includes replacement transistors, IC's, diodes, and lamps for one year's isolated service of 5451A	10685A
Service Kit Carrying Case	9211-1568

REPLACEMENT BOARD KITS

For 5460A Display Unit (Kit is HP Assembly Number 10681A)

Reference Designator	Description	HP Part Number
A1	Board Assembly: Vertical Amplifier	05460-60001 (new); 05460-60013 (rebuilt)
A2,A3	Board Assembly: DAC (Digital-to-Analog Converter)	05460-60002 (new); 05460-60014 (rebuilt)
A4	Board Assembly: Word Storage	05460-60003 (new); 05460-60015 (rebuilt)
A5	Board Assembly: Control	05460-60004 (new); 05460-60016 (rebuilt)
A6	Board Assembly: Reference Power Supply	05460-60005 (new); 05460-60017 (rebuilt)
A7	Board Assembly: Plot Control	05460-60020 (new); 05460-60520 (rebuilt)
A8	Board Assembly: Nixie® Display	05460-60006 (new); 05460-60018 (rebuilt)
A9	Board Assembly: Light Driver	05460-60007 (new); 05460-60019 (rebuilt)

For 5466A ADC Unit (Kit is HP Assembly Number 10683A)

Reference Designator	Description	HP Part Number
A1,A2	Board Assembly: Input	05466-60001 (new); 05466-60501 (rebuilt)

continued on next page

Table 1-3. Service Kit (Continued)

5466A ADC Unit *(Continued)*

Reference Designator	Description	HP Part Number
[1]A3,A4,A5,A6	[1]Board Assembly: Digitizer, 10-bit	[1]05466-60002 (new); 05466-60502 (rebuilt)
[1]A3,A4,A5,A6	[1]Board Assembly: Digitizer, 12-bit	[1]05466-60007 (new); 05466-60507 (rebuilt)
A7	Board Assembly: Error	05466-60003 (new); 05466-60503 (rebuilt)
A8	Board Assembly: Trigger	05466-60004 (new); 05466-60504 (rebuilt)
A9	Board Assembly: Control	05466-60008 (new); 05466-60508 (rebuilt)
A10	Board Assembly: Sample Generator	05466-60006 (new); 05466-60506 (rebuilt)
	[1]Subassembly: Digitizer, 10-bit	[1]1813-0011 (new); 1813-0025 (rebuilt)
	[1]Subassembly: Digitizer, 12-bit	[1]1813-0010 (new); 1813-0026 (rebuilt)
	Subassembly: Sample/Track-and-hold	1813-0009 (new); 1813-0028 (rebuilt)

For 5475A Control Unit (Kit is HP Assembly Number 10684A)

Reference Designator	Description	HP Part Number
A2	Board Assembly: Reference	05580-6002
A4—A6	Board Assembly: Regulator	05580-6004
A12	Board Assembly: Matrix A	05475-60045 (new); 05475 (rebuilt)
A13	Board Assembly: Matrix B	05475-60046 (new); 05475-60546 (rebuilt)
A14	Board Assembly: Shift Register	05475-60038 (new); 05475-60538 (rebuilt)
A15	Board Assembly: Function	05475-60012 (new); 05475-60512 (rebuilt)
A16	Board Assembly: Switch Register	05475-60041 (new); 05475-60541 (rebuilt)
A17	Board Assembly: Buffer	05475-60007 (new); 05475-60031 (rebuilt)

ISOLATED SPARES KIT (Includes replacement components as listed below):
(Kit is HP Assembly Number 10685A)

Resistors

Part Number	Quantity
0811-0436	1
0811-0233	1
0811-1397	1
0811-1398	1
0811-1517	1

Op Amps

Part Number	Quantity
0960-0025	1
0960-0049	1

SCR

Part Number	Quantity
1884-0063	1

[1] 10-bit Digitizer Assembly provided in standard 10683A Kit, 12-bit Digitizer provided in Option 001 10683A Kit.

continued on next page

Table 1-3. Service Kit (Continued)

ISOLATED SPARES KIT *(Continued)*

Transistors

Part Number	Quantity
1850-0099	1
1853-0015	1
1853-0020	4
1853-0027	1
1853-0034	1
1853-0036	2
1853-0088	2
1854-0003	2
1854-0005	1
1854-0019	2
1854-0020	1
1854-0022	1
1854-0039	2
1854-0071	6
1854-0092	2
1854-0094	2
1854-0215	2
1854-0326	2
1855-0020	2
1855-0049	1
1855-0051	1

Diodes

Part Number	Quantity
1901-0028	2
1901-0040	10
1901-0041	2
1901-0044	1
1901-0056	1
1901-0179	1
1901-0415	2
1902-0025	1
1902-0049	1
1902-0071	2
1902-0244	1
1902-0556	1
1902-3002	1
1902-3024	2
1902-3104	1
1902-3193	1
1902-3234	1
1902-3268	1

Digital Display Tubes

Part Number	Quantity
1970-0009	1
1970-0012	1

Lamps

Part Number	Quantity
1450-0745	2
2140-0300	1

Switches

Part Number	Quantity
3101-1238	2

Fuses

Part Number	Quantity
2110-0006	1
2110-0014	1
2110-0010	1

Integrated Circuits

Part Number	Quantity
1820-0054	4
1820-0055	2
1820-0068	2
1820-0069	1
1820-0070	2
1820-0071	2
1820-0077	4
1820-0092	1
1820-0116	2
1820-0174	1
1820-0201	1
1820-0327	2
1820-0328	1
1820-0539	1
1820-0956	2
1826-0105	1

end of table

1.9.2 Board Exchange

Hewlett-Packard provides exchange printed circuit boards for the following Fourier Analyzer system units:

5460A Display Plug-in Unit
5466A ADC Plug-in Unit
5475A Control Unit

The board exchange program may be used either to replenish boards used from the service kit or as a replacement for a known inoperative board in the Fourier Analyzer System. Rebuilt exchange boards are available at a cost reduced from that of a new board. The price of the board is dependent upon return of the defective board to Hewlett-Packard.

The procedure for participating in the board exchange program is as follows:

a. Repair Fourier Analyzer with the service kit. Replace faulty boards in the system with good boards from the kit. Tag bad boards with a description of trouble caused in system.

b. Order rebuilt boards(s) from your nearest Hewlett-Packard Sales and Service Office.

c. When replacement board ordered arrives, place it in the Service Kit. Save the box the board came in for return shipment of the faulty board.

d. The box in which you received your replacement board will also contain an address label to be used for returning the faulty board to the Central Repair Facility, a Module Repair Report to provide failure information, and a piece of tape to seal the box. Place the faulty board in the box, along with the completed Module Repair Report, and seal the box with the piece of tape provided. Stick the address label on the box and send the board to the Central Repair Facility.

1.10 ACCESS

The following paragraphs discuss the accessibility for repair and adjustments of the units that make up the 5451A Fourier Analyzer (see *Figure 1-4*). The discussion assumes cabinet mounting of the system. Always remove power before removing or replacing any system unit or circuit board.

1.10.1 Pozi-driv® Screwdrivers

Many screws in the instrument appear to be phillips, but are not. To avoid damage to the screw, Pozi-driv® screwdrivers must be used (HP Part No. 8710-0899 Small Pozi-driv®).

1.10.2 Pull-Out Table

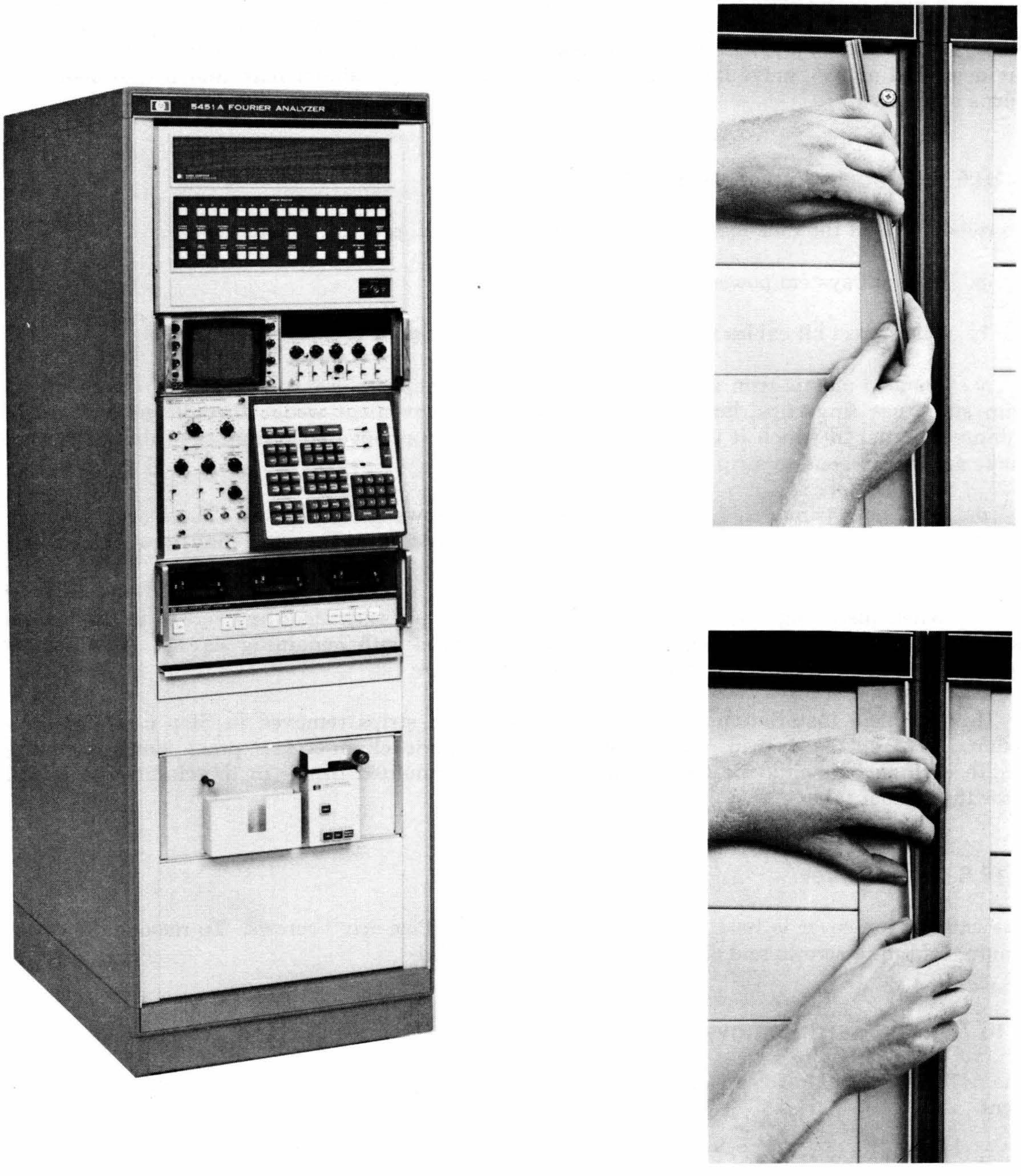
One unit in the 5451A cabinet is a pullout writing table. For access to the table, pull out on the trim strip/handle directly below the keyboard.

1.10.3 Plug-ins

The Fourier Analyzer system contains two plug-ins: the 5460A Display and the 5466A ADC. One plug-in is mounted in the H51-180 Oscilloscope Mainframe; the other is in the 5475A Control Unit Mainframe. To remove either plug-in, turn off power and loosen the one or two knurled mounting screws that connect through to the mainframe unit. Pull out gently on the screw(s) for initial separation of the plug-in from the mainframe unit connector. Now grasp the plug-in at one or more convenient points and pull out from the mainframe unit. To replace a plug-in, reverse the above procedure.

® National Screw and Mfg. Div. of Monogram Industry

Figure 1-4. Access Information



NOTES:
1. Some units shown are not part of the standard 5451A System.
2. 5465A ADC shown.

1.10.4 Rear Door

To prevent unauthorized access to connections at rear of system, the cabinet is fitted with a lockable rear door; two keys for the door are provided. To open the door, unlock it, turn latch handle 90° from locked position, and open the door.

To remove door, pull down on handle of "L"-shaped upper hinge pin and separate upper hinged corner of door from cabinet. The door can be lifted out of its lower mounting bracket. To install the door, reverse the above procedure. The cabinet design allows the door to be mounted as either a right-hand-opening or left-hand-opening door. To reverse door mounting, remove door (as described above), move latching bracket to other side of cabinet rear, and install door so it opens as desired.

1.10.5 Removing an Instrument

To remove one of the rack-mounted units from the cabinet, proceed as follows:

a. Turn off system power.

b. Disconnect all cables from rear of the instrument to be removed.

c. Remove plastic trim strips at each side of cabine from (see *Figure 1-4*). To remove trim trim strip, use fingertips, large coin, or some other convenient wedge to pull one end out of cabinet channel in which it is mounted. Then carefully remove strip from the cabinet. Do not make any sharp bend in strip.

d. With both trim strips removed, all mounting screws are accessible. These are Pozi-driv® screws and must be removed with a Pozi-driv® screwdriver. The unit may now be removed from the system and a new unit put in its place.

e. When installing a new unit in the cabinet, first put rack-mounting screws in the bottom holes of the rack-mounted brackets; then proceed upward with remaining screws. After attaching new unit to rack, connect cables as described in *Figure 1-2*.

f. Complete installation by replacing plastic trim strips removed in Step c. of this procedure. To replace a strip, place one end in the guide channel and press along its entire length. When replacing the trim strip, be sure it is mounted firmly in the channel so it will clear the pullout table.

1.10.6 Top Cover

The cabinet top cover is held in place by four flathead Pozi-driv® screws. To remove the cover, remove retaining screws and screw-in eyebolts, if installed.

1.10.7 Keyboard Removal

The 5475A Control Unit keyboard may be removed for maintenance (contact cleaning) or replacement.

a. Remove power.
b. Pull 5475A four to six inches forward from its normal rack-mounting position (see Removing an Instrument, paragraph 1.10.5).
c. Loosen three Pozi-driv® screws at top of keyboard unit.
d. Remove three Pozi-driv® screws at bottom of keyboard unit.

® National Screw and Mfg. Div. of Monogram Industry

please continue on next page

NOTE
Keyboard unit is connected to mainframe by two cables. When separating these two units, be careful to avoid straining cable or damaging connectors.

e. Gently separate keyboard unit from mainframe. Stop when you feel cable pull, reach behind keyboard unit and disconnect the two cables, then continue removing keyboard from mainframe.

To replace keyboard, perform the above procedure in reverse.

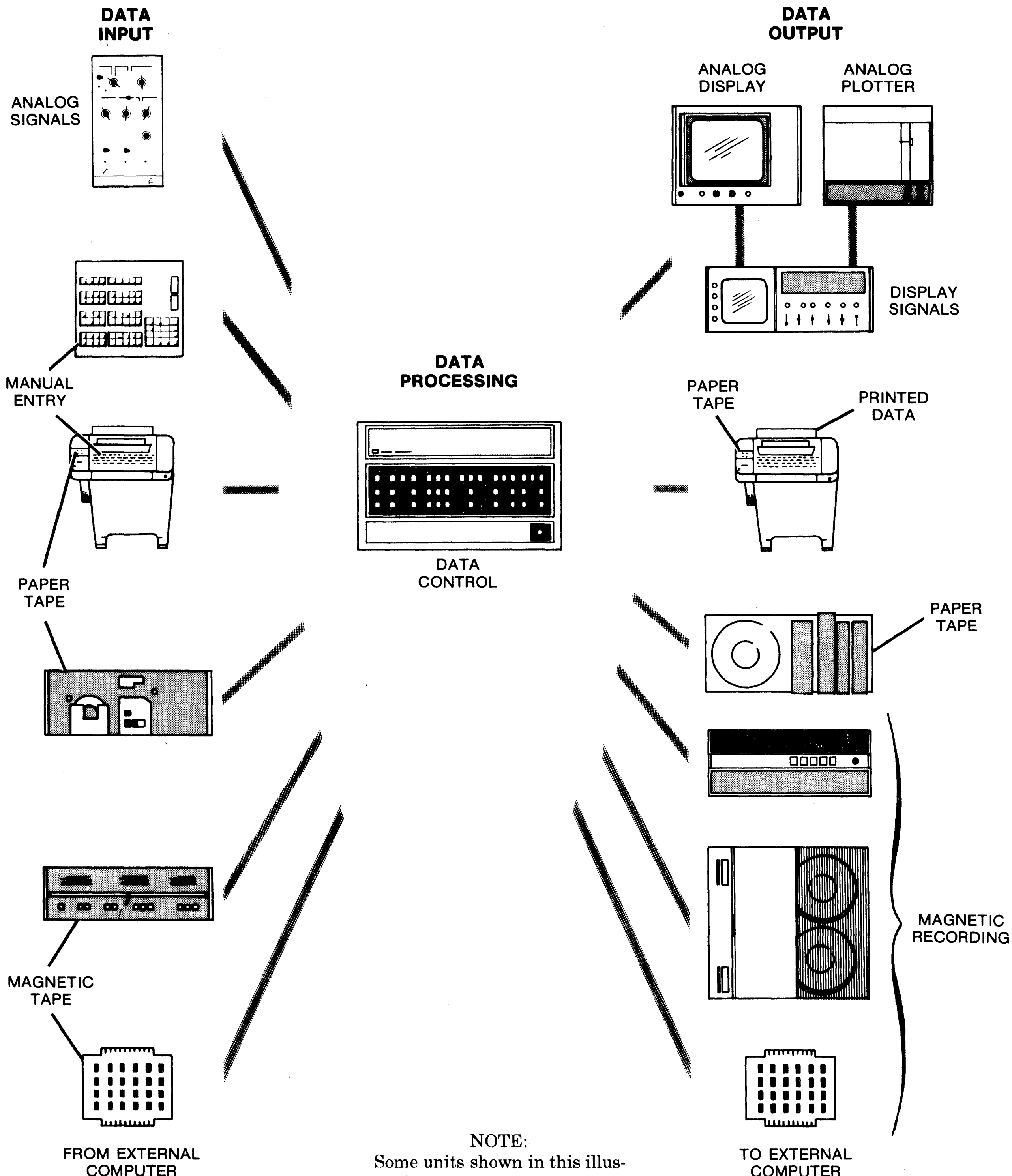
1.11 TEST EQUIPMENT

Table 1-4 provides the specifications and recommended test equipment required to maintain the 5460A, 5466A, and 5475A units of the Fourier Analyzer System.

Table 1-4. Test Equipment Specifications

Equipment Type and Critical Specifications	Recommended Instrument	Used For*
AC Voltmeter Voltage Range: 10 mV to 5V Frequency Range: 10 Hz to 1 MHz	HP Model 3470A	1, 2, 3
DC Voltmeter Voltage Range: 1 to 100V Resolution: .1 mV Accuracy: 0.03 of reading	HP Model 3470A	2
Oscilloscope Frequency Range: DC to 50 MHz Sensitivity Range: .005 V/div to 20 V/div Sweep Range: .05 μsec/div to 2 sec/div	HP Model 1707A	2, 3
Frequency Counter Frequency Range: DC to 50 MHz Accuracy: ±1 count Sensitivity: 0.1 Vrms Time Base Stability <±5 x 10^7, 0° to 50°C	HP Model 5300A, + Model 5303B, Option 001	2, 3
Function Generator	HP Model 3310B	2, 3
Precision Power Supply Output Range: 0 to 10V Resolution: 1 mV Accuracy: .025% +1 mV	HP Model 6115A	2, 3
		* 1 = Operational Check 2 = Adjustments 3 = Troubleshooting

Figure 2-1. Fourier Analyzer Data Flow Block Diagram



NOTE:
Some units shown in this illustration are not part of the standard 5451A System, and are offered as options.

SECTION II
PRINCIPLES OF OPERATION

2.1 INTRODUCTION

This section provides a brief theory of operation for the 5451A Fourier Analyzer System. Since specific Fourier Analyzer Systems will reflect individual requirements, the detailed theory of operation of the computer, oscilloscope mainframe, teleprinter, photoreader, I/O cards, and any additional peripherals supplied with each system are fully documented in separate manuals. On the other hand, specific unit theory of operation for the 5460A Display Unit plug-in, 5466A, A/D Converter plug-in, and 5475A Control Unit are provided in this manual since these units are unique to the Fourier Analyzer Systems.

2.2 SYSTEM DESCRIPTION

The 5451A Fourier Analyzer System performs statistical analysis using Fourier analysis techniques. Analysis control can be on an operation-by-operation basis or, using the six programming keys on the 5475A Control Unit, measurement routines can be automatically executed. All functions are performed under software control by means of the Fourier Analyzer System tape. Keyboard programming allows the system to perform the following operations automatically without additional special software:

Forward and inverse Fourier transform
Power Spectrum
Magnitude and phase spectrum
Auto and cross correlation
Cepstrum
Digital filtering
Convolution
Histogram
Scaling
Hanning and other weighting functions
Ensemble averaging (time and frequency)

Six editing keys on the control unit provide on-line editing so that user written automatically controlled measurement programs can be changed on-line, without the need of off-line compiling or testing.

The Fourier Analyzer is a completely calibrated system. All displays and data outputs are accompanied by a scale factor relating them to physical units. This calibration is the result of using digital techniques in all computations.

The systems can also be used as stand-alone computers by setting a switch on the 5475A Control Unit to COMPUTER NORMAL. Computer programming knowledge is not required for operation of the system as a Fourier Analyzer. All operations are controlled through the 5475A Control Unit keyboard.

The 5475A keyboard contains keys for input/output and basic analysis operations. Additional numeric address keys control data flow into and out of data block, and permit entry of numeric values into memory. All control and data entry operations use decimal numbers for data values and data identification.

Data can also be entered into the Fourier Analyzer as analog signals through the two-channel 5466A, A/D Converter, or as digital or binary information through the computer input channels (see *Figure 2-1*).

Data output is available through the oscilloscope, teleprinter and other peripheral devices depending on system configuration.

please continue on next page

2.3 FOURIER ANALYZER SYSTEM OPERATION

The operation of a Fourier Analyzer System (like most computing systems) can be separated into data input, data processing and control, and data output. This description will assume that the system is operating in the Fourier Analyzer mode and that an analog signal is applied to the 5466A A/D converter, digitized and stored in computer memory, manipulated under control of the 5475A Control Unit and system software, and displayed on the system oscilloscope. Other methods of input and output are possible as shown in *Figure 2-1* (i.e., photoreader input, punched tape output, etc.). However the choice of input and output devices does not change the basic operation of the Fourier Analyzer System. For a complete explanation of all controls and indicators on the 5460A, 5466A, and 5475A refer to the System Operating Manual. Refer to the mnemonic list (*Table 2-3*) placed at the end of this discussion for an explanation of signal names used in the system.

2.4 5466A A/D CONVERTER

The 5466A Fourier ADC produces two's-complement digital representation of sampled analog input signals, and transfers the resultant digital data words to the Computer. The ADC has three basic parts: input amplifiers, track/hold and digitizers, and control and sampling logic. Each of these parts is described in more detail below; a simplified block diagram of the ADC is given in *Figure 2-2.*

The input amplifier serves to provide sufficient gain so the input signal can drive the analog-to-digital converter; full-scale ADC output (positive or negative) requires plus or minus 10V at the output of the input amplifier. The track/hold and A-to-D converter module sample the analog input signal and convert its level to a digital word. The control and sampling logic serve to trigger the ADC, provide sampling signals to initiate conversions, transfer data words to the Computer, and detect erroneous sampling conditions and data patterns.

The 5466A is available in several different configurations. Some 5466A options, and the equivalent 5451A options, are listed in *Table 2-1.*

2.4.1 ADC Interface

Normally, the 5466A is installed in the plug-in compartment in the left-hand side of the 5475A Control Unit. One of the two rear-panel connectors (P15) mates with J15 in the 5475A, providing paths for all data, standard control, and power between these units. If one of the remote control options is ordered for the 5451A system, a second connector (J21) is added to the 5475A, to connect to P21 of the 5466A, to carry the signals that can be used to control the SAMPLE RATE and OVERLOAD VOLTAGE controls. The remote control signals interface via optional interface cables and microcircuit interface cards. *Figure 2-3* presents a simplified diagram of the interface connections.

text continues on page 2-5

Table 2-1. 5466A and 5451A Options

Description	5466A Option Number	5451A Option Number (See Configuration Notice)
10 bits, 2 channels	Standard	Standard
12 bits, 2 channels	001	041
10 bits, 4 channels	002	042
12 bits, 4 channels	003	043
10 bits, 2 channels (wired and tested for 4 channels)	006	044
12 bits, 2 channels (wired and tested for 4 channels)	007	045
2 channels (10-bit or 12-bit) remote control of ADC	No additional changes required	060
4-channels (10-bit or 12-bit) remote control of ADC	No additional changes required	061

Figure 2-2. ADC Block Diagram

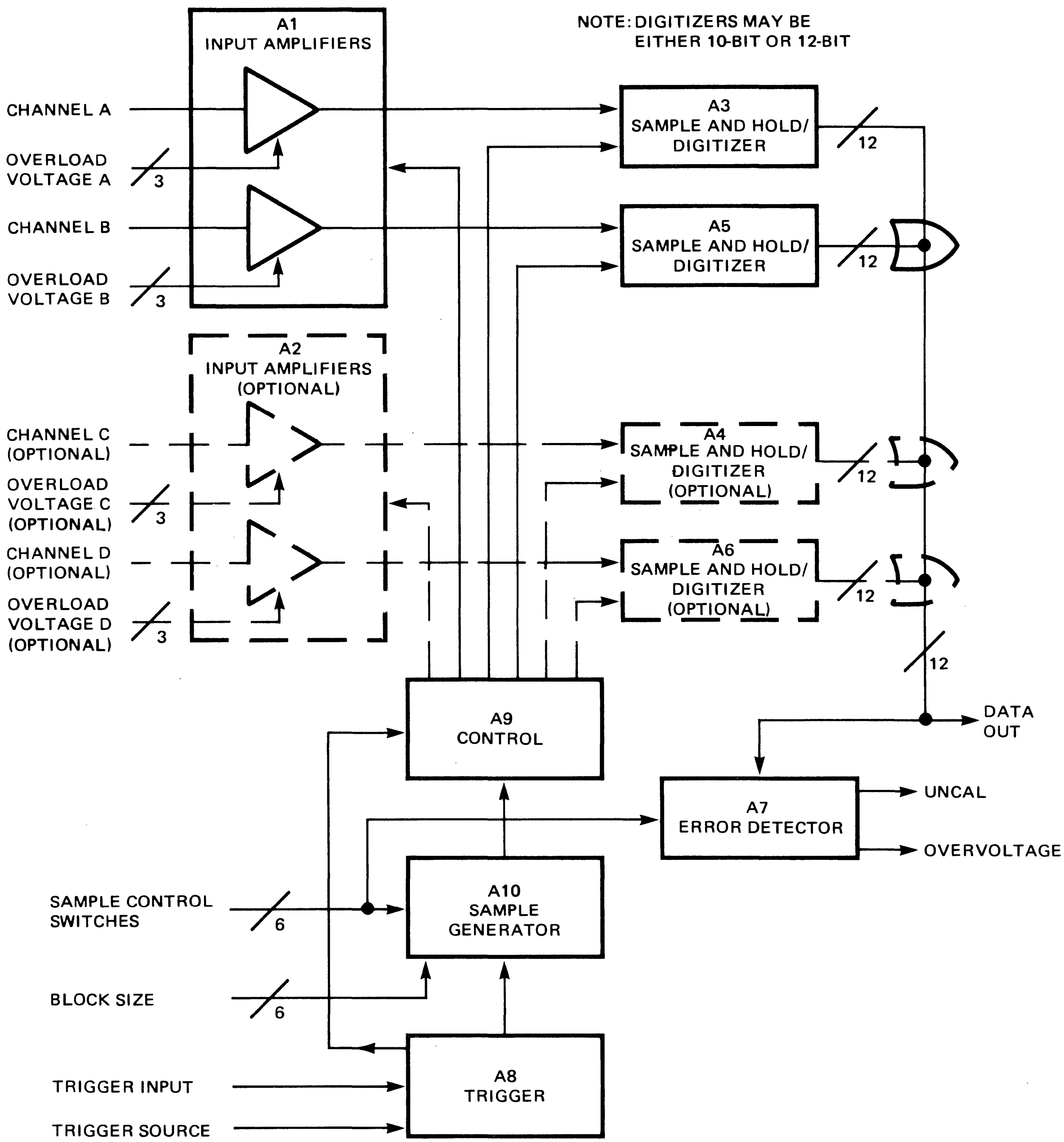
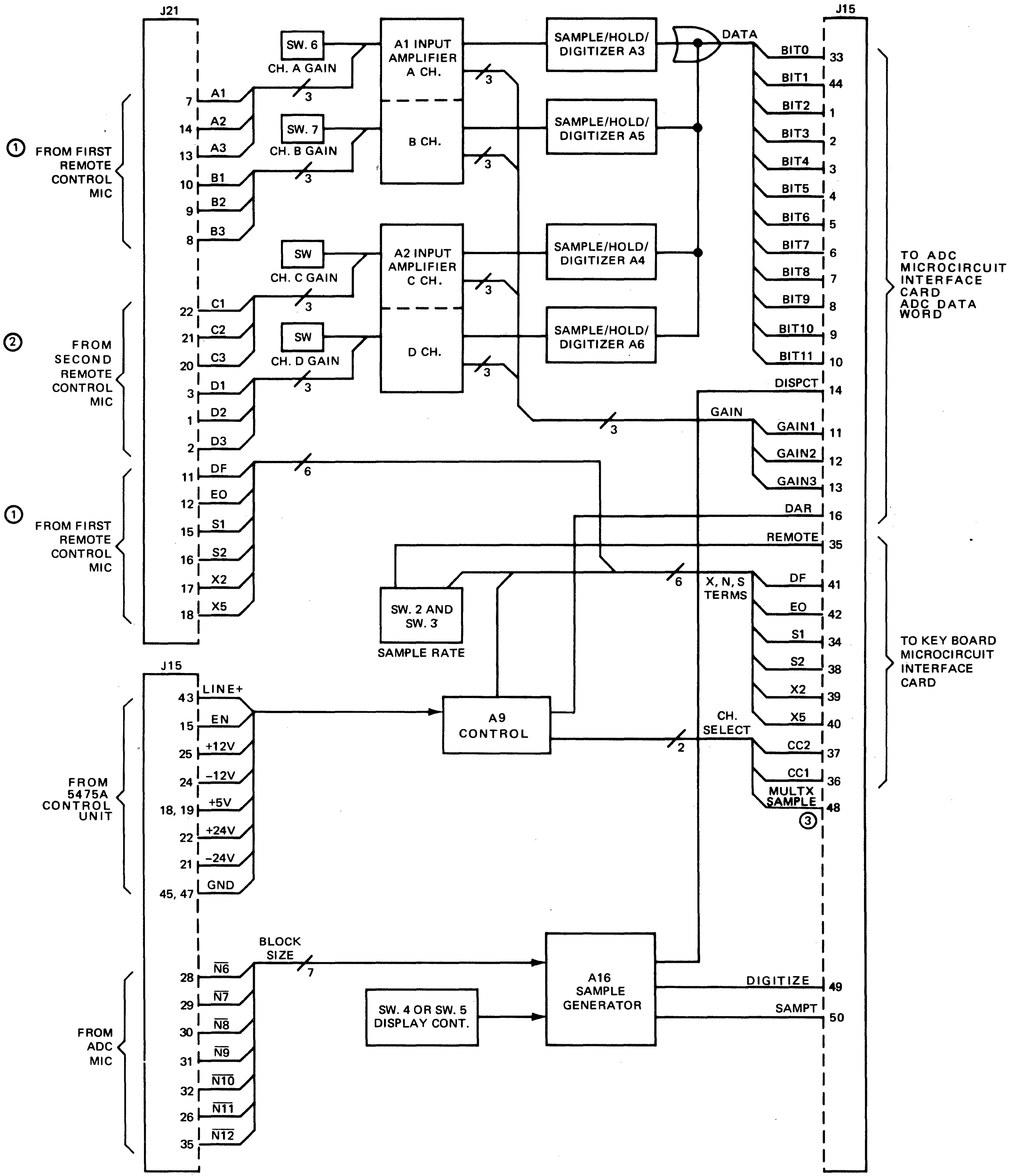


Figure 2-3. ADC Input/Output Signals

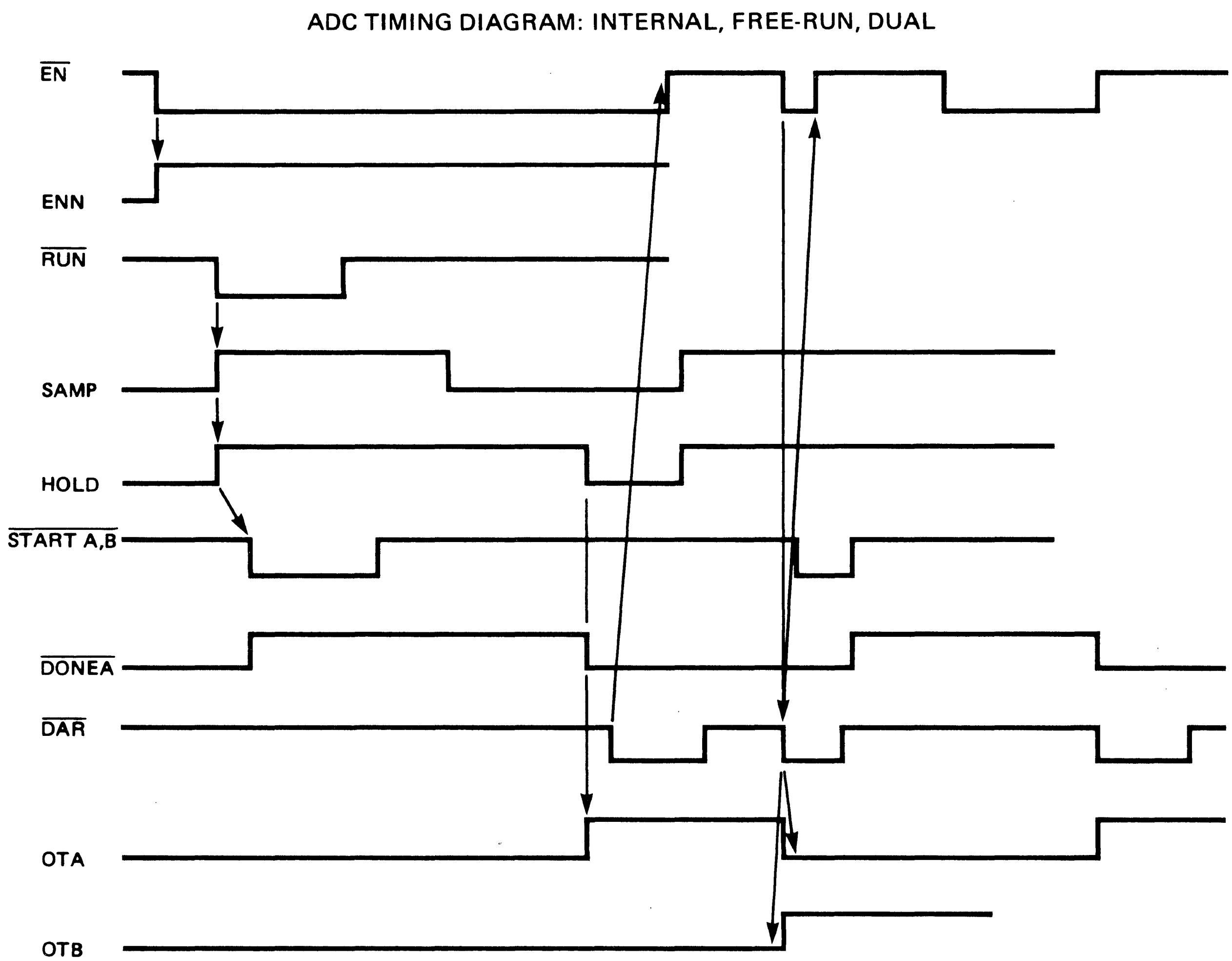


① Used for remote control of Channels A and B (2- channel or 4- channel ADC).
② Used for remote control of Channels C and D (4- channel ADC's only).
③ If installed.

2.4.2 ADC Data Transfer Sequence

The basic timing diagram for the 5466A, in two-channel operation, is given in *Figure 2-4*; arrows in the figure indicate causality between signals.

Figure 2-4. ADC Data Transfer Timing



The ADC is activated by the ENcode (or EN) signal from the Computer going "low". This causes the ADC's internal "off-on" signal, ENN, to be "high". If the ADC (TRIGGER SOURCE switch) is not in FREE RUN mode, the ADC waits for one of the triggering conditions (internal, external, or line) to be satisfied. When this occurs, the RUN signal goes "low", allowing the sample pulses to start. If the ADC (TRIGGER SOURCE switch) is in FREE RUN, the ENN signal itself will initiate the samples. In either case, the sample pulses are enabled to clock the ADC only after a positive-going transition of the sample pulse itself has been detected. This assures that no partial sample pulses will be generated.

The sample pulse causes the HOLD command to go to its "high" state. The HOLD signal disconnects the track-and-hold module from the analog input signal and stores the last analog value on a capacitor. This process requires about 100 nsec, so, 100 nsec after HOLD goes "high" ("true"), the START signals go "low", initiating action of the analog-to-digital converter modules.

please continue on next page

2.4.2 ADC Data Transfer Sequence *(Continued)*

A $\overline{\text{START}}$ signal is sent to the A-to-D converter module for each channel selected by the 5466A's INPUT (or DISPLAY/INPUT) switch. In the example shown in *Figure 2-4,* two channels are being used, so $\overline{\text{START A}}$ and $\overline{\text{START B}}$ are sent.

When the $\overline{\text{START}}$ commands are received by the digitizer modules, they respond by setting their $\overline{\text{DONE}}$ signals "high". Analog-to-digital conversion requires approximately 2.5 μsec for the 10-bit digitizers, or approximately 4 μsec for the 12-bit digitizers. When the digitization is completed, the digitizer modules send their $\overline{\text{DONE}}$ signals to the "low" state.

$\overline{\text{DONE A}}$, the $\overline{\text{DONE}}$ signal from the Channel A digitizer, initiates the data transfer to the Computer. This signal enables sending of the $\overline{\text{DAta Ready}}$ (or $\overline{\text{DAR}}$) signal to the Computer as OTA puts the Channel A data onto the data bus. When the Computer has accepted the data word, it returns $\overline{\text{EN}}$ to the ADC. If other data words (from Channel B, C, or D) are to be transmitted to the Computer, subsequent $\overline{\text{DAR}}$'s will be sent to the Computer and these words placed on the bus by the appropriate "OT" commands. The $\overline{\text{DONE}}$ signals also return HOLD to its "low" state, so the track-and-hold modules can prepare for another sampling of the input signal(s).

The ADC continues converting data points until it is stopped by the Computer when all the selected data blocks have been filled. The ADC "turn-off" method depends on the Control Board Assembly used as A9; in either case, the method is used because $\overline{\text{EN}}$ is used both to start the ADC and to transfer data.

If the 05466-60005 board assembly is used for A9, the ADC is turned "off", and ENN goes low, after two sample pulses have been generated without $\overline{\text{EN}}$ going "low".

If the 05466-60008 board assembly is used for A9, the ADC is turned "off", and ENN goes low, if a DAR (DAta Ready) is sent without $\overline{\text{EN}}$ being "low", or if approximately 50 μsec passes between the time a DAR is sent and an $\overline{\text{EN}}$ received from the Computer.

Control of ADC operation and data transfer to the Computer requires a Microcircuit Interface Card (MIC) for the ADC and a second MIC for the 5475A Keyboard; these cards are installed in Computer I/O slots, as indicated in Section I of this manual. The control words associated with these cards are "DATA" and "KEYBOARD", respectively.

A DATA word contains the digitized ADC output and the input range code. The ADC output is either 10-bits or 12-bits long, depending on the digitizers installed. The DATA word also contains the display code word, "DISPCT".

The KEYBOARD word transmits status signals concerning Sampling Rate, "EO", "DF", "X5", "X2", "S2", "S1", and the remote programming status word, "REMOTE", to the Computer. Block size information for the Sample Generator and for the 5475A indicator lamps is provided by lines $\overline{\text{N6}}$ through $\overline{\text{N12}}$ from the Keyboard MIC.

2.4.3 ADC Circuit Cards

The 5466A ADC unit contains seven or ten circuit cards, depending on whether it is to be able to digitize two or four channels. Major signal flow is shown functionally in the flow diagram, *Figure 2-3.* Internal wiring is shown in *Figure 2-12.*

2.4.3.1 A1 (AND A2) INPUT ASSEMBLY (05466-60001)

A two-channel ADC will have one of these assemblies (installed as "A1"); a four-channel ADC will have two of these assemblies (installed as "A1" and "A2").

The Input Board Assembly consists of two identical, independent, channels of amplification. Each channel consists of two amplifier stages; gains of these stages are controlled by decoding three binary signal lines, as indicated in *Table 2-2.*

please continue on next page

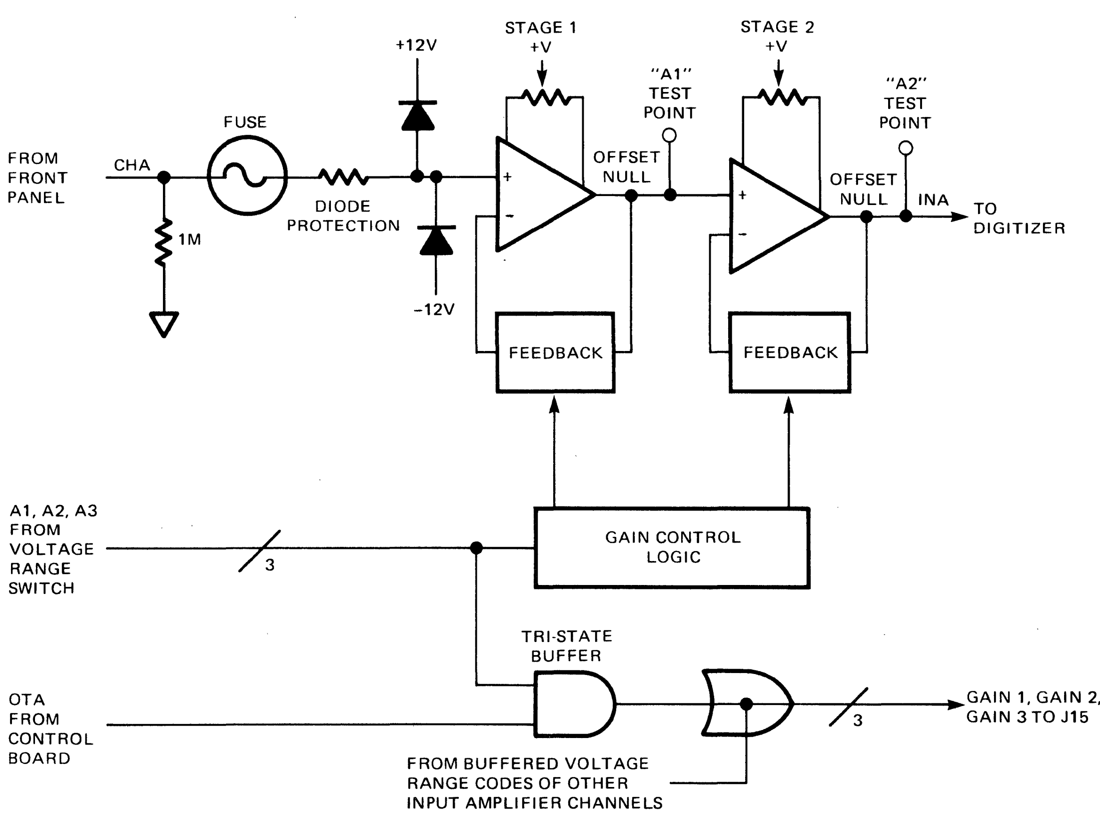
Table 2-2. Input Amplifier Gain Selection

INPUT RANGE	A1, B1 C1, D1	A2, B2 C2, D2	A3, B3 C3, D3	GAIN STAGE 1	GAIN STAGE 2	GAIN OVERALL
8.00 Volts	1	1	1	1	1.25	1.25
4.00 Volts	1	1	0	2	1.25	2.50
2.00 Volts	1	0	1	4	1.25	5.00
1.00 Volts	1	0	0	8	1.25	10.00
0.50 Volt	0	0	1	8	2.50	20.00
0.25 Volt	0	1	0	8	5.00	40.00
0.125 Volt	0	1	1	8	10.00	80.00
CHECK	0	1	1	8	10.00	80.00

A block diagram of one of the two input channels on the Input Board Assembly is given in *Figure 2-5*. Voltage gain is provided by two similar stages of feedback amplification. The first stage uses a FET hybrid operational amplifier for gain, and a MOSFET multiplexer to select the desired amount of feedback. Depending on the amount of feedback, the first stage provides gains of 1.25, 2.5, 5, or 10. The second stage is the same as the first, except that it uses a monolithic operational amplifier, and provides gains of 1, 2, 4, or 8.

The three least-significant bits in the data word sent from the ADC to the Computer represent the gain code for the input channel in which the word originated; for example, if the digitized word is from Channel A, then the three least significant bits are A1, A2, and A3. These bits are transmitted by wire-ORing the outputs of tri-state buffers on the Input Board. When Channel A is being sent to the Computer, the OTA signal will enable the outputs of these buffers onto the input voltage range bus, Gain 1, Gain 2, and Gain 3. This bus transmits these bits directly to the Computer.

Figure 2-5. Input Board--Block Diagram (One Channel)



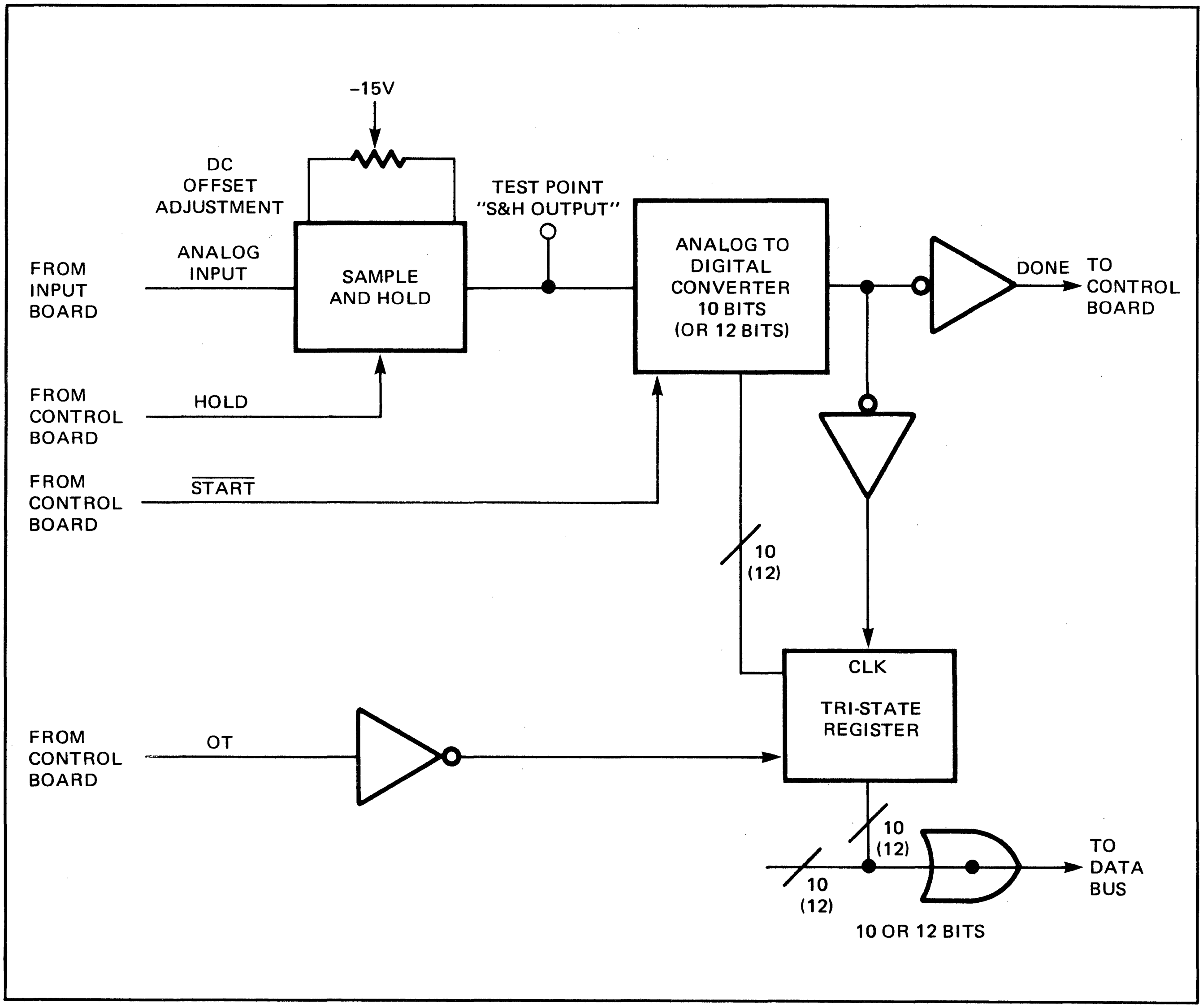
2.4.3.2 A3, A5 (AND A4, A6) DIGITIZER ASSEMBLY (10-bit Digitizer: 05466-60002)
(12-bit Digitizer: 05466-60007)

Each Digitizer Assembly handles one channel. For two-channel operation, only A3 and A5 are installed; for four-channel operation, all four digitizer slots are filled.

Either of the digitizers described in this manual subsection converts analog signal levels into corresponding digital data words; these data words are then transferred to the Computer for processing. The operation of the assembly is based on two major components: The track-and-hold module and a ten-bit or twelve-bit analog-to-digital converter. A block diagram of the digitizer board assembly is given in *Figure 2-6.*

When HOLD is "low", track-and-hold module's output is allowed to follow its input (which is the output of the input amplifier for that channel). The analog signal level at the instant HOLD goes "high" is stored on a capacitor, allowing analog-to-digital conversion of the input signal to be performed at definite points of time.

Figure 2-6. Digitizer Assembly--Block Diagram



2.4.3.2 A3, A5 (AND A4, A6) DIGITIZER ASSEMBLY (10-bit Digitizer: 05466-60002) (12-bit Digitizer: 05466-60007) *(Continued)*

Shortly after HOLD goes "high", $\overline{\text{START}}$ goes "low", initiating the a-to-d conversion. The converter module accepts the $\overline{\text{START}}$ command, starts its internal clock, and begins to digitize the analog value at its input, using the "successive approximation" technique. After a short time (approximately 2.5 μsec, for 10-bit conversion, or 4 μsec for 12-bit conversion) the conversion is completed, and a $\overline{\text{DONE}}$ signal is generated by the module. This signal is inverted on the Digitizer board and sent to the Control Board Assembly (A9); the $\overline{\text{DONE}}$ signal is also inverted and used to clock the digitized word onto the output register.

The output register consists of four four-bit tri-state flip-flop IC's that store the data word until it is put onto the data bus for transmission to the Computer. Depending on the 5466A configuration, one or three other digitizers will also output data to the Computer via this data bus.

2.4.3.3 A7 ERROR ASSEMBLY (05466-60003)

This assembly responds to two operating conditions which are outside the 5466A's specifications. These conditions are: digitized word equal to "full-scale" value (indicating that "overflow" has occurred); and Sampling Rate set too high. A block diagram of the Error Assembly is given in *Figure 2-7*.

The OVERLOAD VOLTAGE lamp is lighted whenever the digital output word is equal to the positive or negative full-scale value. Combinational logic, using exclusive-OR and conventional logic, detects when the word on the data bus is "full-scale". To avoid spurious signals from this combinational logic as the data is placed on the bus, the signal "OTEN" (from the Control Board) is used to strobe the output of the logic. This strobed output is used to activate a monostable flip-flop, which lights the OVERLOAD VOLTAGE LED (light-emitting diode) indicator on the 5466A's front panel. Jumpers on this board enable the user to set up the overload voltage detection logic for either 10-bit or 12-bit data words.

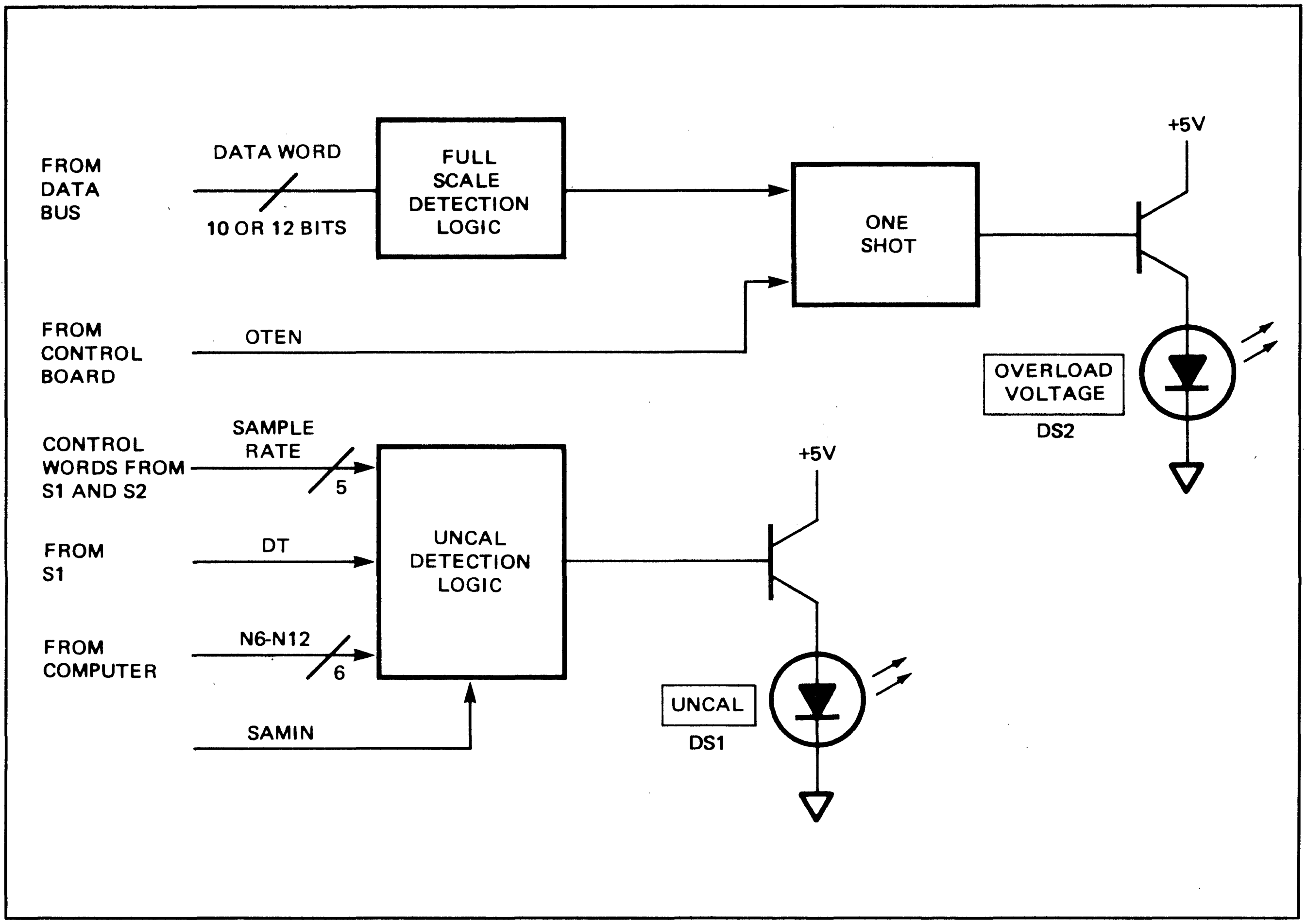
The UNCAL logic looks at the settings of the SAMPLE CONTROL switches, and the Block Size signals, and lights the UNCAL lamp if the sampling rate is too fast. The uncalibrated sample rates are listed in *Table 2-3*. The UNCAL condition is also indicated if the front-panel EXT/INT switch is set to EXT; in this case, the SAMIN signal will be "low".

Table 2-3. Uncalibrated Sample Rates/Block Sizes

SAMPLE MODE	MULTIPLIER	BLOCK SIZES
ΔTIME, kHz/μs	500/1K/1	ALL
ΔTIME, kHz/μs	250/500/2	ALL
ΔFREQ, Hz/ms	500/1K/1	256 ≤ ALL ≤ 4096
ΔFREQ, Hz/ms	250/500/2	512 ≤ ALL ≤ 4096
ΔFREQ, Hz/ms	100/250/5	1024, 2048, 4096
ΔFREQ, Hz/ms	50/100/10	2048, 4096
ΔFREQ, Hz/ms	25/50/20	4096 only

please continue on next page

Figure 2-7. Error Assembly--Block Diagram



2.4.3.4 A8 TRIGGER ASSEMBLY (05466-60004)

This assembly contains the signal conditioning and waveshaping circuitry to generate logic trigger pulses to start the ADC's operation. These pulses are generated from internal, external, and line trigger sources. The board also generates a self-CHECK calibrating signal for the ADC, and provides regulated plus-and-minus 15V power from plus-and-minus 24V inputs. A block diagram of the Trigger Board Assembly is given in *Figure 2-8*.

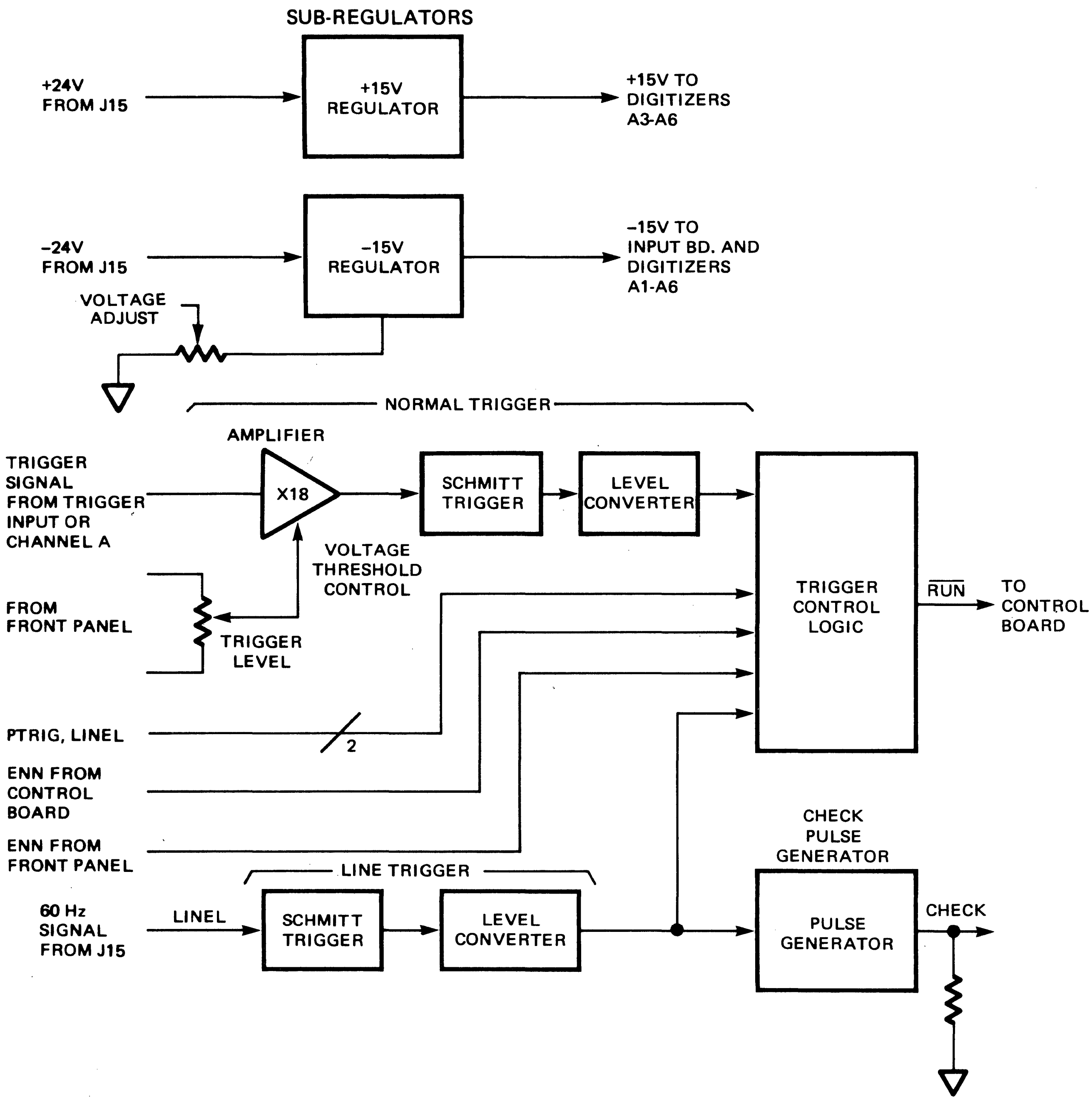
The "trigger" signal comes from the ADC's front-panel TRIGGER INPUT connector or from the output of Channel A's Input Amplifier. TRIGGER SOURCE selection is made by a switch on the ADC's front panel.

The "internal" or "external" trigger is amplified by a X18 amplifier. A level shifter associated with this amplifier allows its output to be shifted anywhere from approximately -10V to approximately +10V, so the following stage, a Schmitt Trigger, can trigger on any part of an ac waveform. The Schmitt trigger's output is passed through a level converter so it can be used by TTL control logic.

The "line" trigger circuitry operates from the 60-Hz sine wave signal available at the 5466A's rear-panel connector J15. A Schmitt trigger converts this signal to a 60-Hz square wave; this trigger's output is also passed through a level converter so it can be used by the TTL Trigger Control Logic circuit. The "line" "trigger" signal is also used to trigger a monostable pulse generator to produce the CHECK signal; this signal is a train of pulses approximately 51 mV high, 100 μsec wide, routed to each of the Input Amplifiers.

text continues on page 2-12

Figure 2-8. Trigger Assembly--Block Diagram



2.4.3.4 A8 TRIGGER ASSEMBLY (05466-60004) *(Continued)*

The Trigger Control Logic processes the logic transitions produced by the "normal" ("internal" or "external") trigger or the "line" trigger. If the signal "LINEL" is "low", the "normal" trigger will be used to produce the signals that start the ADC's operation, and $\overline{\text{PTRIG}}$ will determine the slope (or transition) that will be the triggering edge; "low" $\overline{\text{PTRIG}}$ = "positive-going" transition triggers, "high" $\overline{\text{PTRIG}}$ = "negative-going" transition triggers. If "LINEL" is "high", the "line" trigger is used, and $\overline{\text{PTRIG}}$ has no effect.

$\overline{\text{RUN}}$ is produced when the Trigger Control Logic is armed by the "ENN" signal, and then detects the correct logic transition in the output of the selected trigger source.

2.4.3.5 A9 CONTROL ASSEMBLY (05466-60005 or 05466-60008)

This assembly contains all the logic necessary to communicate with the Computer, start the digitizers, and transmit data words to the Computer. Since the Computer, the ADC's Sample Generator, and the ADC converter modules have independent clock rates, the control logic is (necessarily) asynchronous. A block diagram of this assembly is given in *Figure 2-9.*

The ADC passes data to the Computer in a "handshake" manner. In this way, whenever the ADC is ready to transmit a data word to the Computer, it sends the DAR (DAta Ready) signal to indicate this. Similarly, when the Computer is ready to accept a data word, it sends the EN (ENcode) signal to the ADC. EN is also used initially to turn on the ADC. Because of this dual usage, special Control Board logic (the "ENN Detection Logic) is required to handle it.

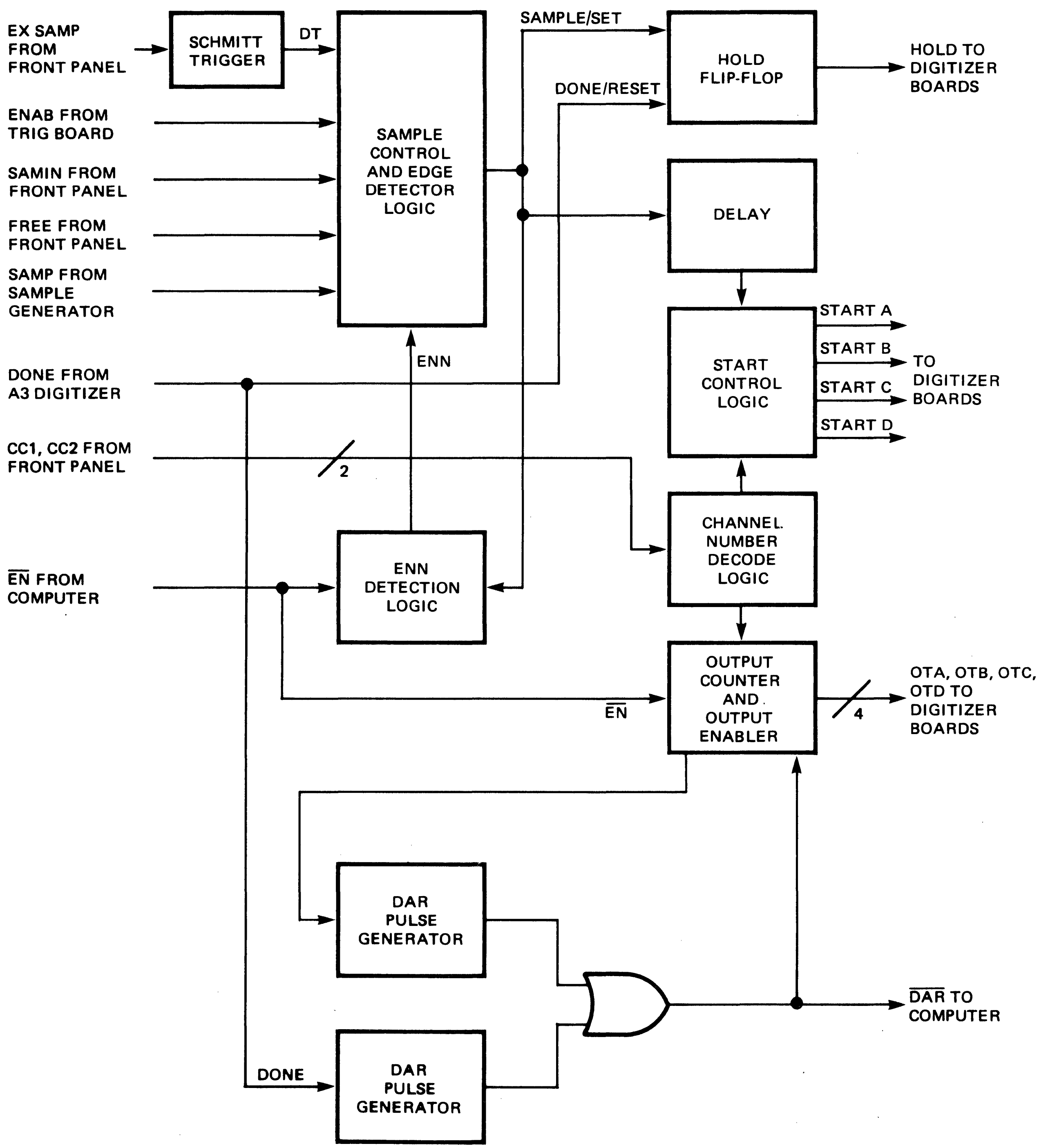
Whenever the ADC is turned "on", ENN is "high". Once ENN is "high", as a result of an EN signal, it is held high until two sample pulses are received without (meanwhile) receiving another EN signal. This condition occurs only when the Computer will accept no more data words, and wants to turn the ADC "off".

The ENN signal, when "high", enables the Sample Control and Edge Detector Logic. SAMIN and FREE define four conditions handled by this logic, as shown in *Table 2-4.* For the "free run" mode, with either "internal" or "external" sample control, the logic transmits samples starting with the first positive-going edge of the sample after ENN goes "high". For the "triggered" mode and "external" samples, the logic passes samples starting with the first positive-going edge of the sample after both ENN and the signal ENAB (from the Sample Generator Board) go "true". By waiting until the positive edges of pulses are received, the logic assures that no partial pulses are sent to other sections of the Control Board. For "triggered" mode and "internal" samples, the logic simply passes the pulses, because the Sample Generator Board will not send partial pulses.

Table 2-4. Sample Conditions

SAMPLE TYPE		TRIGGER MODE		SIGNALS	
INT.	**EXT.**	**FREE RUN**	**TRIGGERED**	**SAMIN**	**FREE**
X		X		H	H
X			X	H	L
	X	X		L	H
	X		X	L	L

Figure 2-9. Control Assembly--Block Diagram



2.4.3.5 A9 CONTROL ASSEMBLY (05466-60005 or 05466-60008) *(Continued)*

The sample pulses, after passing through the Sample Control and Edge Detector Logic, set the HOLD flip-flop. The HOLD command is sent to all digitizer boards. The sample pulses are delayed and used to send the START command to the appropriate digitizer board. Depending on the "number of input channels" information encoded on the lines "CC1" and "CC2", the START command is sent to 1, 2, 3, or 4 boards, as indicated in *Table 2-5*.

Table 2-5. Channel Number Encoding

CC1	CC2	NUMBER OF CHANNELS
0	1	1
1	1	2
0	0	3
1	0	4

When the Channel A digitizer accepts the START command, its DONE signal goes "low". When a conversion has been completed, DONE returns "high". This serves to reset the HOLD signal, allowing the track-and-hold modules to track the input signal again. It also triggers a monostable pulse generator which sends the $\overline{\text{DAR}}$ command to the Computer. When the Computer returns the ENcode signal, and if the Output Counter Enabling Logic indicates that other ADC channels have data words to be transferred, additional $\overline{\text{DAR}}$ signals are sent to the Computer. With each $\overline{\text{DAR}}$ signal, the appropriate "OT" command is generated, to place the correct A-to-D module data on the bus.

Jumper locations on either Control Board allow some flexibility to meet user operating requirements. The two Control Boards described in this section differ slightly in the jumper arrangements provided.

The two-position "ADC"/"MULTX" jumper (on either board) selects whether the ADC's sample rate or an external multiplexer command will be used to start the digitizer; normally the "ADC" connection is the one that is used.

The two-position "INT"/"EXT" jumper (on either board) selects the source of sample pulses that will be available at the 5475A's rear-panel SAMPLE OUT BNC connector. In the "EXT" position, the SAMPLE OUT pulses are those which are actually controlling the sampling; the 5466A's front-panel EXT/INT switch determines whether these pulses are to come from an external source, or from the ADC's Sample Generator assembly (controlled by the SAMPLE CONTROLs). When this jumper is in its "INT" position, the SAMPLE OUT pulses come only from the 5466A's Sample Generator assembly output, regardless of whether or not it has been selected as the sample control source by the 5466A's EXT/INT switch.

A single-position "2100" jumper (on the 05466-60005 board only) enables the slight change in timing required when the system that contains the 5466A is controlled by a HP 2100A Computer (the jumper is removed if some other model of the computer is used).

The single-position "MULTX" jumper (on the 05466-60005 board only) must be installed whenever the ADC containing this board is used with a multiplexer; normally this jumper is not installed.

The two-position "2CH"/"4CH" jumpers (on the 05466-60008 board only) enable the timing of the return of $\overline{\text{DAR}}$ to the Computer. If the ADC is interfaced via the HP 12930 Universal Interface Card (usually used for interfacing a four-channel ADC), then these jumpers should be in the "4CH" position. If the ADC is interfaced via the HP 12566 Microcircuit Interface Card, then these jumpers should be in the "2CH" position.

please continue on next page

2.4.3.6 A10 SAMPLE GENERATOR ASSEMBLY (05466-60006)

This assembly is the "master" timing source for the 5466A. It contains two crystal oscillators, several frequency dividers, sample inhibit logic, the trigger light driver, and the display flag generator. A block diagram of this assembly is given in *Figure 2-10.*

The 20 MHz oscillator's output is used to generate samples for the "Δt" sampling mode. This signal is divided down to 2 MHz before being passed into the divider chains.

The 8.192 MHz oscillator's output is used to generate samples for the "Δf" sampling mode. This signal is passed through a programmable frequency divider circuit (controlled by block size lines N6 through N12). Depending on the block size code, the 8.192 MHz signal is divided by "1", "2", "4", "8", "16", "32", or "64", as shown in *Table 2-6.*

Table 2-6. Programmable Divider Coding

For this BLOCK SIZE	This code line is "true"	So the Divider divides by
4096	N12	1
2048	N11	2
1024	N10	4
512	N9	8
256	N8	16
128	N7	32
64	N6	64

The signal "$\overline{DF}$" determines which oscillator's (divided) output is connected to the divider chains; "$\overline{DF}$" "high" = Δf (8.192 MHz oscillator), "$\overline{DF}$" "low" = Δt (20 MHz oscillator).

The first divider in the frequency divider chains is the X2, X5 Divider. Depending on the logic levels of the "X2" and "X5" bits, this circuit will divide by "1", "2", "4", or "10", as shown in *Table 2-7.* The next circuit, the S1, S2 divider, divides by "1", "10", "100", or "1000". The last divider, "EO", divides by "1" or "1000"; its output is the sample pulses that are sent to the Control Board Assembly.

Table 2-7. Coding of Divider Circuits

X2, X5 DIVIDER			S1, S2 DIVIDER			EO DIVIDER	
X2	X5	DIVIDE BY	S1	S2	DIVIDE BY	EO	DIVIDE BY
1	1	1	0	0	1	0	1000
0	1	2	1	1	10	1	1
1	0	4	0	1	100		
0	0	10	1	0	1000		

In the Sample Generator's composite form, sample pulses of a given frequency are generated for each combination of SAMPLE CONTROL switch settings, as shown in *Table 2-8* (for "Δt" sampling) or *Table 2-9* (for "Δf" sampling). Note that sampling rates which are too fast for proper ADC operation can be generated; these are indicated in the tables by an asterisk ("*"), and in actual 5466A operation by lighting of the front-panel "UNCAL" lamp.

The Sample Generator is allowed to operate at all times, when the ADC is in its "free run" mode. When not in FREE RUN the Sample Generator is turned "off" whenever the ADC, itself, is turned "off" by the Computer. This operation is controlled by the Sample Inhibit Logic, which also generates this signal which drives the 5466A's front-panel TRIGGERING lamp.

text continues on page 2-18

Figure 2-10. Sample Generator--Block Diagram

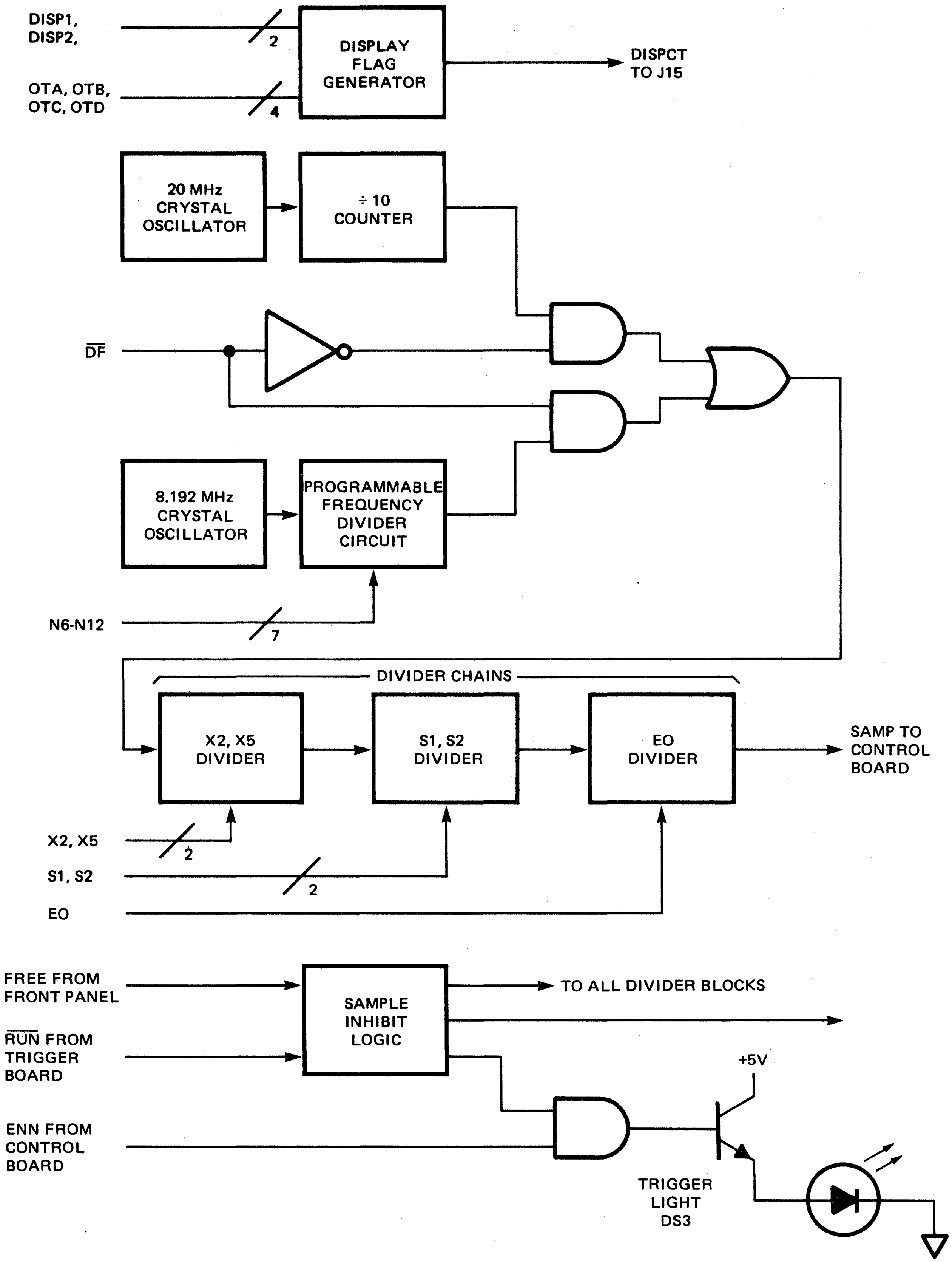


Table 2-8. Δt Sampling

$\overline{X2}$	$\overline{X5}$	$\overline{S1}$	$\overline{S2}$	EO	OUTPUT FREQ (Hz)	Δt	F_{MAX} (Hz)
0	1	0	0	1	1M	1 μs	500k*(UNCAL)
1	0	0	0	1	500k	2 μs	250k*(UNCAL)
1	1	1	1	1	200k	5 μs	100k
0	1	1	1	1	100k	10 μs	50k
1	0	1	1	1	50k	20 μs	25k
1	1	0	1	1	20k	50 μs	10k
0	1	0	1	1	10k	100 μs	5k
1	0	0	1	1	5k	200 μs	2.5k
1	1	1	0	1	2k	500 μs	1k
0	1	1	0	1	1k	1ms	500
0	1	0	0	0	1k	1 ms	500
1	0	1	0	1	500	2 ms	250
1	0	0	0	0	500	2 ms	250
0	0	1	0	1	200	5 ms	100
1	1	1	1	0	200	5 ms	100
0	1	1	1	0	100	10 ms	50
1	0	1	1	0	50	20 ms	25
1	1	0	1	0	20	50 ms	10
0	1	0	1	0	10	100 ms	5
1	0	0	1	0	5	200 ms	2.5
1	1	1	0	0	2	500 ms	1
0	1	1	0	0	1	1 sec	0.5
1	0	1	0	0	0.5	2 sec	0.25
0	0	1	0	0	0.2	5 sec	0.1

Table 2-9. Δf Sampling

						TOTAL	OUTPUT FREQ VS. BLOCK SIZE						
$\overline{X2}$	$\overline{X5}$	$\overline{S1}$	$\overline{S2}$	EO	ΔF	TIME	4096	2048	1024	512	256	128	64
0	1	0	0	1	1kHz	1ms	4.096MHz*	2.048MHz*	819.2kHz*	409.6kHz*	204.8kHz*	81.92kHz	40.96kHz
1	0	0	0	1	500Hz	2ms	2.048MHz*	8.192kHz*	409.6kHz*	204.8kHz*	81.92kHz	40.96kHz	20.48kHz
1	1	1	1	1	200Hz	5ms	8.192kHz*	409.6kHz*	204.8kHz*	81.92kHz	40.96kHz	20.48kHz	8.192kHz
0	1	1	1	1	100Hz	10ms	409.6kHz*	204.8kHz*	81.92kHz	40.96kHz	20.48kHz	8.192kHz	4.096kHz
1	0	1	1	1	50Hz	20ms	204.8kHz*	81.92kHz	40.96kHz	20.48kHz	8.192kHz	4.096kHz	2.048kHz
1	1	0	1	1	20Hz	50ms	81.92kHz	40.96kHz	20.48kHz	8.192kHz	4.096kHz	2.048kHz	819.2Hz
0	1	0	1	1	10Hz	100ms	40.96kHz	20.48kHz	8.192kHz	4.096kHz	2.048kHz	8192Hz	409.6Hz
1	0	0	1	1	5Hz	200ms	20.48kHz	8.192kHz	4.096kHz	2.048kHz	819.2Hz	409.6Hz	204.8Hz
1	1	1	0	1	2Hz	500ms	8.192kHz	4.096kHz	2.048kHz	819.2Hz	409.6Hz	204.8Hz	81.92Hz
0	1	1	0	1	1Hz	1sec	4.096kHz	2.048kHz	819.2Hz	409.6Hz	204.8Hz	81.92Hz	40.96Hz
0	1	0	0	0									
1	0	1	0	1	.5Hz	2sec	2.048kHz	819.2Hz	409.6Hz	204.8Hz	81.92Hz	40.96Hz	20.48Hz
1	0	0	0	0									
0	0	1	0	1	.2Hz	5sec	819.2Hz	409.6Hz	204.8Hz	81.92Hz	40.96Hz	20.48Hz	8.192Hz
1	1	1	1	0									
0	1	1	1	0	.1Hz	10sec	409.6Hz	204.8Hz	81.92Hz	40.96Hz	20.48Hz	8.192Hz	4.096Hz
1	0	1	1	0	50MHz	20sec	204.8Hz	81.92Hz	40.96Hz	20.48Hz	8.192Hz	4.096Hz	2.048Hz
1	1	0	1	0	20MHz	50sec	81.92Hz	40.96Hz	20.48Hz	8.192Hz	4.096Hz	2.048Hz	.8192Hz
0	1	0	1	0	10MHz	100sec	40.96Hz	20.48Hz	8.192Hz	4.096Hz	2.048Hz	.8192Hz	.4096Hz
1	0	0	1	0	5MHz	200sec	20.48Hz	8.192Hz	4.096Hz	2.048Hz	.8192Hz	.4096Hz	.2048Hz
1	1	1	0	0	2MHz	500sec	8.192Hz	4.096Hz	2.048Hz	.8192Hz	.4096Hz	.2048Hz	81.92mHz
0	1	1	0	0	1MHz	1ksec	4.096Hz	2.048Hz	.8192Hz	.4096Hz	.2048Hz	81.92mHz	40.96mHz
1	0	1	0	0	.5MHz	2ksec	2.048Hz	.8192Hz	.4096Hz	.2048Hz	81.92mHz	40.96mHz	20.48mHz
0	0	1	0	0	.2MHz	5ksec	.8192Hz	.4096Hz	.2048Hz	81.92mHz	40.96mHz	20.48mHz	8.192mHz

*UNCAL POSITIONS

2.4.3.6 A10 SAMPLE GENERATOR ASSEMBLY (05466-60006) *(Continued)*

The Display Control Logic on this board uses one bit of each data word passed to the Computer to indicate whether the channel associated with that word is to be displayed. The logic decodes the two words "DISP1" and "DISP2", as shown in *Table 2-10*, to detect which channel is to be displayed. It then checks the "OT" commands and generates the "DISPCT" signal at the same time the data word to be displayed is placed on the data bus.

Table 2-10. Display Coding

DISP 1	DISP 2	DISPLAY CHANNEL
1	1	A
0	1	B
1	0	C
0	0	D

2.5 5475A CONTROL UNIT

The 5475A Control Unit provides the necessary pushbuttons and switches to control and manipulate the input data during operation as a Fourier Analyzer System. The Control Unit also provides interfacing between the ADC and the Computer. A complete explanation of each control and the proper operating procedure to perform the required functions is contained in the System Operating Manual.

The 5475A Control Unit consists of a cabinet that houses the keyboard panel assembly, keyboard and control logic comprising seven circuit cards, a power supply consisting of six circuit cards, and a receptacle for the 5466A ADC plug-in. Refer to *Figure 2-13* and *Figure 2-14* for block diagrams and signal interconnection between the keyboard assembly and control unit circuit cards. The Control Unit cabinet can be mounted as one package in a standard rack cabinet.

2.5.1 Control Unit Connectors

The 5475A Control Unit contains three connectors within the cabinet for internal connection, and four connectors at the rear of the unit for cable hookup. The three internal connectors are shown on the left side of the wiring diagram (*Figure 2-14*). The J15 connector is a 50-pin ribbon-type female connector that mates with the male connector on the installed A/D Converter. The J16 and J19 connectors are mounted on the baseplate of the control unit directly behind the keyboard panel. J16 is a 24-pin ribbon-type female connector that mates with a cable from the keyboard front panel lights and switches. J19 (A and B) consists of dual 50-pin ribbon-type female connectors that mate with a cable from the keyboard panel pushbuttons. The four rear panel connectors are shown on the right side of the wiring diagram. The J11 (A and B) connector consists of dual 36-pin ribbon-type female connectors that mate with a double male connector and cable to the computer. The J11A connector is not used in the basic 5451A system. The J11B connector carries signals from front panel switches on the ADC and keyboard through to the computer interface card. The J12 connector is a 36-pin ribbon-type female connector that mates with a cable from the computer ADC/keyboard interface card. The J13 connector is a 48-pin etched-circuit male connector that mates with a cable from the 2752A Teleprinter I/O connector. The J14 connector is a 36-pin ribbon-type female connector that mates with a cable connected to the computer teleprinter interface card. Power connectors on the rear panel are described in Paragraph 2.5.4.8. "J21" is an optional 50-pin ribbon connector which carries the remote control signals between the ADC and the microcircuit interface cards.

please continue on next page

2.5.2 A11 Keyboard Assembly

The keyboard is a self-contained assembly with a front panel enclosing 63 pushbuttons, 2 lever switches, a slide switch, and 10 indicator lights. The keyboard pushbuttons are connected to the Control Unit by a cable terminating in dual 50-pin connectors (P19/J19). The switches and indicator lights are connected to the Control Unit by an additional cable terminated by a 24-pin connector (P16/J16).

The keyboard pushbuttons simulate the function of a teletypewriter. Sixty lines transfer signals from sixty pushbuttons on the keyboard to circuit cards A12 Matrix A and A13 Matrix B in the control unit. Three additional pushbuttons (RESTART, STOP, and CONTINUE) simulate functions of the computer front panel. These signals are transferred from the keyboard to the A15 Function card in the Control Unit.

The slide switch (S1) on the keyboard panel labeled COMPUTER NORMAL/FOURIER ANALYZER transfers an active (ground level) $\overline{\text{FOURIER}}$ signal to the A16 Switch Register, A15 Function Generator, and A14 Shift Register cards when the switch is in the Fourier Analyzer position. Lever switches RUN/STEP (S2) and SINGLE/REPEAT (S3) transfer ground level STEP and REPEAT signals to the A16 Switch Register card when placed in the $\overline{\text{STEP}}$ and $\overline{\text{REPEAT}}$ positions, respectively. Keyboard panel indicator lights (DS1-DS10) signifying block size of 64, 128, 256, 512, 1024, 2048, 4096 plus READY, BUSY, and WHAT? indications are activated by corresponding signals from the A17 Buffer card.

2.5.3 ADC/Control Unit Interface

The 5466A Analog-to-Digital Converter transfers nine signals, representing its front-panel switch settings, to the 5475A Control Unit's A16 Switch Register Card; these signals are "CC1", "CC2", "S1", "S2", "X2", "X5", "DF", and "EO". An additional 25 signals are transferred between the ADC and the Computer, passing from J15 directly through the 5475A to J12. For 5451A options 060 and 061, the remote programming signals are connected via 5475A connectors J23 and J21.

2.5.4 Control Unit Circuit Cards

2.5.4.1 A16 SWITCH REGISTER ASSEMBLY (05475-60041)

The switch register is inserted to provide continuity from the ADC and Control Unit keyboard to the microcircuit I/O card in the computer. All functions are straight wired through A16, except for the RESTART IN signal.

2.5.4.2 A15 FUNCTION ASSEMBLY (05475-60012)

The function card is used to generate a STOP OUT or CONTINUE OUT under control of the Control Unit keyboard during FOURIER operation and provide a POW ON signal to A14 each time power is turned on. The $\overline{\text{FOURIER}}$ signal is used to enable the STOP OUT and CONTINUE OUT flip-flops.

2.5.4.3 A17 BUFFER ASSEMBLY (05475-60199)

The buffer card contains 11 lamp drivers. The lamp drivers accept block size inputs ($\overline{\text{BSI}}$ $\overline{\text{64-4096}}$) for output to connector J16 to light the block size indicators on the keyboard panel. The block size inputs are also routed from connector J12 to J15 to permit computer control of block size dependent sample values in the ADC (refer to *Table 2-14*). A ground-level $\overline{\text{RDY I}}$ input signal results in a high level RDY O signal to light the keyboard panel READY light (DS9). A high-level RDY I input signal results in a high-level BUSY O signal to light the keyboard BUSY indicator (DS8). A high level STOP OUT signal from the A15 Function card

please continue on next page

2.5.4.3 A17 BUFFER ASSEMBLY (05475-60199) *(Continued)*

results in a high-level STOP LIGHT signal, which in turn is jumpered to the RDY O signal. This causes the READY indicator to light after the STOP button is depressed to interrupt a program. A ground level $\overline{\text{WHAT I}}$ input signal results in a high-level WHAT O output signal to light the keyboard WHAT? indicator.

2.5.4.4 A12 MATRIX A ASSEMBLY (05475-60045)

The matrix A card contains 29 diode arrays, with a possible 15 diodes in each array. The number and placement of diodes in each array is arranged to coincide with a specific code for two ASCII characters. Thus, an active ground-level input from a keyboard pushbutton over one of the 29 input lines activates a particular array and results in a ground-level coded output on the 15 signal lines $\overline{\text{M1}}$ through $\overline{\text{M15}}$ (two 7-bit ASCII words plus a start bit in parallel).

2.5.4.5 A13 MATRIX B ASSEMBLY (05475-60046)

The matrix B card functions as an extension of the matrix A card, by accepting the remaining 31 keyboard input lines to encompass a total of 60 keyboard pushbuttons (excepting the 3 command pushbuttons sensed by the function card). The combination of matrix A and B constitutes 60 different vertical diode arrays. Fifteen horizontal lines divide the vertical arrays into 15 segments. The presence or absence of a diode in each segment (diode connecting vertical and horizontal line) determines the ASCII format for each vertical array. A ground input applied to a vertical line pulls down the diodes in the array and results in ground-level outputs on those horizontal lines connected to a diode. Each of the 60 different ASCII combinations on the 15 output lines $\overline{\text{M1}}$ through $\overline{\text{M15}}$ is sensed as a unique character by the A14 Shift Register.

2.5.4.6 A14 SHIFT REGISTER (05475-60038)

The shift register card accepts the parallel ASCII double-character (representative of a Control Unit keyboard pushbutton) on input lines $\overline{\text{M1}}$ through $\overline{\text{M15}}$. The character is shifted through a 20-bit register and output serially on the TTY DATA OUT line to the computer via connector J14. An active $\overline{\text{FOURIER}}$ signal from the keyboard enables the data shift. The data is clocked out at a 110 Hz rate by an internal oscillator. The oscillator is enabled each time a data character enters the register and is disabled when the register is empty of information. Teleprinter character signals are accepted on the TTY DATA IN line and also transferred on the TTY DATA OUT line to the computer.

The shift register contains logic to eliminate pushbutton contact bounce, and to prevent redundant or simultaneous keyboard inputs. The read-only-memory enable (ROM ENAB) signal provides a 2V level to energize the matrix diodes when a pushbutton is depressed. This permits transfer of the character through matrix A and B to the shift register. The POW ON signal from the function card assures that the logic circuits are set to the proper state upon system turn-on.

2.5.4.7 A18 RELAY BOARD (05475-60010)

The relay and crowbar card contains a relay circuit to switch +12V on the TTY DATA IN line when the +12V sense line is opened. Opening of the sense line indicates that a teleprinter is not connected to the system; placing +12V on the TTY DATA IN line assures that the Control Unit keyboard data can be transferred through the A14 Shift Register on the TTY DATA OUT line. (Teleprinter when connected supplies a nominal +12V through J13 pin 4.) The crowbar circuit protects the +5V supply against overvoltage damage to the integrated circuits.

please continue on next page

2.5.4.8 POWER SUPPLY CIRCUIT (A1, A2, A3, A4, A5, A6)

The power supply (see *Figure 2-15*) is enclosed in the rear of the Control Unit cabinet and consists of the T1 transformer, a rectifier board (A1), and a motherboard (A3) with four plug-in cards (A2 and A4 through A6). The power supply generates plus and minus 24 volts, plus and minus 12 volts, and plus and minus 5 volts for distribution throughout the system. The supply voltages are provided through the rear panel connector J18 DISPLAY for distribution to the display subsystem and through connector J17 POWER SUPPLY for external distribution. Protection circuits are included to prevent damage to the instrument. In case of a voltage short to ground or another voltage, the OVERLOAD lamp DS2 on the rear panel of the Control Unit lights.

2.6 5460A DISPLAY UNIT

The 5460A Display Unit accepts 16-bit data words through the computer interface channel and displays the information in analog and digital form. The XY information is converted to analog for display on the system oscilloscope. Digital information is displayed on the 5460A front panel Nixie® tubes and indicator lights. Front panel switches control various modes of display on the oscilloscope.

2.6.1 Display Unit Interface and Connectors

The 5460A Display Unit plugs into the right side of the H51-180AR Oscilloscope Mainframe. Three rear panel connectors (P1, P3, P4) are aligned with three mating connectors (J1, J3, J4) at the rear of the mainframe. A fourth connector (P2) consists of a sliding PC contact on the upper left cabinet rail and mates with a spring contact (J2). This connector supplies a high voltage output to the oscilloscope vertical deflection plates. P1 consists of a 32-pin male ribbon connector that interfaces with the oscilloscope. P3 and P4 consist of 50-pin female ribbon connectors. P3 interfaces with the power supply and X-Y plotter device. P4 interfaces with the computer. See *Figure 2-18*, Wiring Diagram, for Display Unit interconnection with the system.

2.6.2 Data Transfer Sequence

The display unit accepts and processes one computer word (16 bits) at a time. The first two words in a data sequence always contain information for the front panel incandescent and Nixie® displays. The second two words (and subsequent pair of words) normally alternate one word of horizontal (X) data and one word of vertical (Y) data for the oscilloscope display. This transfer of XY data is continued until complete or interrupted by changing the front panel switch settings. See *Figure 2-10*, Operation Flow Diagram, during the ensuing discussion.

2.6.2.1 DATA WORD 1

If the data ready flag ($\overline{\text{DAR}}$ signal) in the Display Unit is active, a data transfer sequence is initiated with an encode command ($\overline{\text{EN}}$ signal) from the computer. The $\overline{\text{DAR}}$ flag is cleared and $\overline{\text{BIT 0}}$ of the first word is examined. $\overline{\text{BIT 0}}$ is low for the first data word and high for all subsequent words in a sequence. (The low level signal is the active level for computer interface cards and system devices.) Bit 0 set low causes the data word counter to be cleared (set to 0) upon receipt of the first word (see *Figure 2-16*, column 2). The remainder of word 1 (bits 1 through 15) contains part of the information required for the front panel display and is stored. A delay of 35 microseconds is encountered between each word time to allow processing of the CRT beam. If the DISPLAY FUNCTION SWITCH is set to PLOT, signifying external plotter operation, the display unit will lock up until the switch is placed at ARM. At this point the unblanking circuit is cleared (not significant until the third and fourth words when the CRT beam is turned on). The settings of the HORIZONTAL ORIGIN, VERTICAL MODE, VERTICAL POLAR ANG/DIV, and VERTICAL SCALE switches are clocked into the computer interface card when the data ready flag is set. Setting the data ready flag indicates completion of the first cycle and readiness to accept the second word.

® Burroughs Corporation

 please continue on next page

2.6.2.2 DATA WORD 2

In the second word of the data transfer sequence (and all other words until the start of a new sequence) $\overline{\text{BIT 0}}$ is high. The balance of the front panel display information is in bits 1 through 15 of the second word. The encode command precedes the second word and causes the data ready flag to be reset during processing of the second word. Since $\overline{\text{BIT 0}}$ of the second word is high and the data word counter was set to 0 for data word 1, the data word counter now advances to 1 (see *Figure 2-16*, column 3). Data word 2 is received and stored, completing the information needed for the front panel displays. After a 35-microsecond delay, the unblanking circuit is cleared (neither function applicable to first two words), and the front panel switches are again clocked in. The data ready flag is then set preparatory to receiving the next word.

2.6.2.3 DATA WORD 3

The third word in a data transfer sequence contains horizontal or X data for the oscilloscope (or plotter) display. An encode command precedes data word 3 and the data ready flag is cleared. $\overline{\text{BIT 0}}$ is high and with the data word counter left at a count of 1, internal logic advances the data word counter to 2 (see *Figure 2-16*, column 4). Bits 5 through 15 of the third word contain the X data and are temporarily stored. If the DISPLAY TYPE switch is set to CONT (X and Y data to be shown continuous) the X data remains stored until the following word containing Y data is received. With DISPLAY TYPE switch in any other position, the X data is transferred to the horizontal digital-to-analog converter. This transfer allows the X data to be positioned on the screen during the 35-microsecond delay. The beam is not turned on until the Y data in the next word completes the display; however, the unblanking circuit is cleared nonetheless. Front panel switch settings are again transferred to the computer, and the data ready flag is set for the receipt of the next word.

2.6.2.4 DATA WORD 4

The fourth word in a data transfer sequence contains vertical or Y data for the oscilloscope display. An encode command precedes arrival of the word and clears the data ready flag. BIT 0 is high and with the data word counter left at 2, the counter is advanced to 3 (see *Figure 2-16*, column 5). Data word 4 contains Y data in bits 5 through 15. These bits are not stored but sent directly to the vertical digital-to-analog (D/A) converter.

If the DISPLAY TYPE switch is set to CONT, the X data in the previous word is now transferred from word storage to the horizontal D/A converter. When the CRT beam is turned on, both X and Y information are displayed in continuous fashion during the 35-microsecond delay.

If the DISPLAY TYPE switch is set to POINT, a 25-microsecond delay is encountered before the beam is turned on, permitting the Y data to be positioned (X data positioned in previous cycle). The beam remains on for 10 microseconds to illuminate the X-Y point position.

If the VERTICAL MODE switch is set to COMPLEX, the X and Y data is displayed as described in the previous paragraph. This switch setting also overrides DISPLAY TYPE set to BAR position. If the switch is not set to COMPLEX, (and DISPLAY TYPE is not set to CONT or POINT) the BAR mode is indicated and the beam is turned on prior to the 35-microsecond delay. With input of subsequent Y data words, a vertical bar will be displayed (during the 35-microsecond delay after beam turn-on) from the mid-screen X position upward (or downward) to the Y position. In this mode the dot is reset each cycle to the midposition for the next bar display. After the Y data has been displayed on the oscilloscope, the unblanking circuit is cleared to turn off the beam.

During display, the position of the DISPLAY FUNCTION switch is tested. If the switch is in the PLOT position (after initially having been thrown to ARM), the word transfer sequence must wait until a completed plot signal (CP) is received from the external plotter accessory. After this pulse is received, signifying end of plotter arm movement, the front panel switch settings are sent to the computer as in previous word operation and the data ready flag is set.

please continue on next page

2.6.2.5 SUBSEQUENT DATA WORDS

Data transfer normally continues in word pairs alternating X and Y information until the display information is complete. Referring to *Figure 2-16,* top row, a data word subsequent to the fourth word (BIT 0 high) will decrement the data word counter from 3 to 2. This results in the processing of this data word for X information in a manner identical to data word 3. Similarly, the next data word (BIT 0 high and Y information in the remaining bits) advances the data word counter to 3 and is processed for Y data identical to data word 4. This alternating sequence continues until all X and Y data are displayed as required. Each new data sequence begins with data words 1 and 2 containing new front panel display information and BIT 0 low in word 1.

2.6.2.6 Z DATA BITS

Data words 3 and 4 also contain a provision to convey Z-axis information for modulating the intensity of the CRT beam under program direction. This type of control is not required under the present display unit configuration. The logic for digital Z-axis modulation is included for possible future options.

2.6.3 Display Unit Circuit Cards

The display unit contains nine printed circuit cards, mounted with discrete components and integrated circuits, that accomplish the display logic and control functions. The circuit card input/output functions are discussed in the following paragraphs. Refer to *Figures 2-17* and *2-18* during the discussion. Signal names with a bar (e.g., DAR) indicate that the active state of the signal is at ground level.

2.6.3.1 A1 VERTICAL AMPLIFIER ASSEMBLY (05460-60001)

The A1 Card converts the Y-axis - 2.0 to +2.0V output of the A2 Vertical DAC (via VERTICAL GAIN control R2) to +30 to +100V to drive the CRT deflection plates. The BEAM signal represents the input from the FIND BEAM switch (S102 via P1) on the oscilloscope. The VOUTA+ signal originates from the front panel GAIN control (R2) and the VPOSN1,2,3 signals originate from the POSITION control (R1). The VSIGP and VSIGM signals represent the output voltage to the vertical deflection plates in the oscilloscope (via P2).

2.6.3.2 A2 VERTICAL DAC ASSEMBLY (05460-60002)

The A2 card accepts vertical or Y-axis information in digital form and converts the binary value into an equivalent analog signal (VOUT 1+) for output to the A1 Vertical Amplifier (via R2) and A5 Control. Similar signals VOUT 2+ and PLOTY+ convey the analog Y information to connectors P4 (for external output) and to P3 (for plotter output). Vertical information is received in digital form from the computer via P4 over lines BIT 5 through BIT 15. The V LOAD input signal from A5 Control clocks the binary information into storage elements on the A2 card. The MID signal from A5 forces the vertical display to mid-scale after each point has been displayed in the DISPLAY TYPE BAR mode. Switch (S8) inputs DCORG, DCMFS, DCPFS represent switch positions DISPLAY CALIBRATE ORIGIN, DISPLAY CALIBRATE MINUS FULL SCALE, and DISPLAY CALIBRATE PLUS FULL SCALE respectively.

2.6.3.3 A3 HORIZONTAL DAC ASSEMBLY (05460-60002)

The A3 card accepts horizontal or X-axis information in digital form and converts the binary value into an equivalent analog signal (HSIG+, HSIGE+, PLOTX+) for respective output to connectors P1 (oscilloscope), P4 (external BNC) and P3 (plotter). Horizontal information is received in digital form over bit lines XDT0 through XDT10 from word storage in the A4 card. The same information is initially input to the A4 card over lines BIT 5 through BIT 15 from the computer. The HLOAD signal from A5 Control clocks the bits into A3 storage elements. Switch (S8) positions DCORG, DCMFS, and DCPFS apply equally to the horizontal information as referenced in the preceding paragraph for vertical data. Also applicable are switch (S4)

2.6.3.3 A3 HORIZONTAL DAC ASSEMBLY (05460-60002) *(Continued)*

positions representing HORIZONTAL SWEEP LENGTHS per centimeter of 12.8 (HS.8), 10.24 (HS.24), and 10 (HS10). With the VERTICAL MODE switch (S1) to COMPLEX, the HS8.0 signal is active, representing a horizontal sweep length of 8.0 centimeters.

2.6.3.4 A4 WORD STORAGE ASSEMBLY (05460-60003)

The A4 card maintains a count of the incoming data words from the computer, and directs the storage and distribution of the words according to the type of information involved. A data word counter on the A4 card counts the incoming words in a data transfer sequence (0-1-2-3, 2-3, 2-3, etc.) and outputs signals to A5 Control and A8 Nixie® Display representative of the word counter sequence (DWCO through DWC3). The data words are received in binary format over digital lines BIT 0 through BIT 15. Each word is preceded by an encode (EN) command from the computer that is recognized by A4 logic. Depending upon which data word counter signal (DWC0-DWC3) is active, the word is accepted by A3 Horizontal DAC (XDT0 through XDT10), A2 Vertical DAC (BIT 5 through BIT 15), A8 Nixie® Display (BIT 1 through BIT 10), or A9 Light Driver cards. Signals to A9 consist of decoded bits representing front panel incandescent lamp functions: Scale Factor Sign (SFS), Frequency (FREQ), Logarithmic (LOG) that also lights decibel (dB), Polar (PLAR), Rectangular (RECT) display, and scale factor multipliers ONE, TWO, FIVE (that also light X10). Signals to A5 Control consist of word counter outputs DWC0, DWC2, DWC3, a pulse from the encode signal (ENN), and Z-axis bit lines ZDT1 through ZDT5 (Z-axis not used in present configuration). Data word counter outputs (DWC0, DWC1) are also sent to A8 Nixie® Display. Refer to *Table 2-11*, Word Format, for bit configuration of each word.

Table 2-11. Data Word Format

BITS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA WORD 1	1	POLAR (0 = RECT)	LOG & dB	FREQ	8 Units	—	—	8 Tens	—	—	8 Hund.	—	—	—	—	SFS
DATA WORD 2		1 Units	2 Units	4 Units	1 Tens	2 Tens	4 Tens	1 Hund.	2 Hund.	4 Hund.	—	—	—	No. "1"	No. "2"	No. "5"
DATA WORD 3	0	ZDT5	—	—	—	XDT0	XDT1	XDT2	XDT3	XDT4	XDT5	XDT6	XDT7	XDT8	XDT9	XDT10
DATA WORD 4	0	ZDT1	ZDT2	ZDT3	ZDT4	YDT0	YDT1	YDT2	YDT3	YDT4	YDT5	YDT6	YDT7	YDT8	YDT9	YDT10

2.6.3.5 A5 CONTROL ASSEMBLY (05460-60004)

The A5 card contains timing and control logic to provide overall coordination of the front panel and oscilloscope displays. The DWC0 signal starts a marker clock on the A5 card; every eighth point or every thirty-second point is intensified according to HORIZONTAL MARKER switch (S6) setting 8 PT (HM8) or 32 PT (HM32). The DWC2 signal identifies the third or horizontal data word and enables the H LOAD clock signal to the A3 Horizontal DAC. The DWC3 signal identifies the fourth or vertical data word and enables the V LOAD clock signal to the A2 Vertical DAC. The MID signal sets the vertical DAC output to mid-scale when the DISPLAY TYPE switch (S9) is set to BAR (and VERTICAL MODE is not set to COMPLEX nor VERTICAL DISPLAY set to PLOT). These switch settings are determined in A5 logic circuits by switch inputs DTPNT, DTCNT, DFPLT, and VDMP2. The ENN signal from A4 Control represents an incoming computer encode command that clears the data ready flag (DAR), and triggers a delay circuit to set the data ready flag again after 35 microseconds. An unblanking circuit on A5

please continue on next page

2.6.3.5 A5 CONTROL ASSEMBLY (05460-60004) *(Continued)*

is activated by each DWC3 and sends a BLANK signal to P1 for unblanking the oscilloscope and an EBLANK+ signal to P4 for external unblanking. DWC3 can occur every other word when only X and Y data is being transferred.

When an X-Y plotter device is used, DISPLAY FUNCTION switch (S7) provides an active DFPLT signal. With the ARM/PLOT switch (S11) to ARM an inactive PLOT 1 signal is applied to A5, inhibiting the DAR signal after the fourth word and causing the plotter arm to stop after the first point has been plotted. Placing the ARM/PLOT switch to PLOT provides an active PLOT 1 signal that inhibits DAR after the first word, causing the plotter to stop after the last point has been plotted. Setting or resetting DAR also enables or disables the PLOT signal to A7 Plotter Control. Receipt of a complete plot pulse (CPP) from A7 sets DAR after the final fourth word. The PEN 1 or PEN 2 relay signal is active to control pen lift when PLOT 1 signal is active and DWC0 is inactive. The Z-AXIS signal provides a variable analog voltage output for modulating intensity of the CRT beam. An amplifier circuit on the A5 card controls Z-axis modulation by monitoring the rate of change of the A5 Vertical DAC output (VOUT 2+) with respect to time. This results in a stable intensity level regardless of length traveled. A digital-to-analog converter is included on the A5 card to accept digital information on ZDT1 through ZDT5 lines for Z-axis modulation; however, this form of Z-axis control is not used under the present configuration.

2.6.3.6 A6 REFERENCE POWER SUPPLY ASSEMBLY (05460-60005)

The A6 card uses the +15V supply voltage from P1 to produce a stable +10V reference output for the A2 Vertical DAC and A3 Horizontal DAC cards. The +5V input from P3 and –12.6V input from P1 are not connected.

2.6.3.7 A7 PLOTTER CONTROL BOARD (05460-60020)

The A7 card controls an external X-Y plotting device by providing an enabling signal (SEEK) to P3 in response to an input signal (PLOT) from A5. Plot rate is controlled by the RATE X input from the PLOT RATE switch (S10) when rotated from EXT to 20. A completed plot signal (CP) from the plotter (via P3) is relayed to A5 control as the completed plot pulse (CPP).

2.6.3.8 A8 NIXIE® DISPLAY ASSEMBLY (05460-60006)

The A8 card controls display of the front panel incandescent and Nixie® lights. Input lines BIT 1 through BIT 10 transfer binary numbers during data words 1 and 2. The DWC0 signal clocks in the most significant bits and DWC1 clocks in the least significant bits. This binary information is converted to BCD format and displayed on Nixie® tubes DS2, DS3, and DS4 and the end of word 2. Nine incandescent indicators are driven by the A9 Light Driver to display functional mode (as shown in *Figure 2-18*). The +170V supply voltage for the numerical Nixie® tubes and minus-sign neon tube is also supplied from the A9 card. The incandescent lamps are driven with +24V from P3.

2.6.3.9 A9 LIGHT DRIVER ASSEMBLY (05460-60007)

The A9 card converts incoming control signals from low voltage logic levels to levels sufficient to drive the front panel incandescent lamps. The A9 card also derives +70V from the 130V ac transformer T1, and adds this voltage to the +100V supply from P1 to provide +170V for the A8 neon and Nixie® tubes.

end of text

Table 2-12. List of Mnemonics: Fourier Analyzer System

SIGNAL	DEFINITION
A1, A2, A3	OVERLOAD VOLTAGE selector codes that indicate the input voltage position of the Channel A OVERLOAD VOLTAGE switch, S6.
ADJ1, ADJ3, ADJ4	Trigger level adjustment resistor R1 on S11.
B1, B2, B3	Code bits for Channel B input OVERLOAD VOLTAGE switch, S7, indicating setting of that switch.
$\overline{\text{BEAM}}$	FIND BEAM input from Oscilloscope mainframe.
$\overline{\text{BIT Ø}}$—$\overline{\text{11}}$	Ten-bit or twelve-bit digital word defining amplitude of analog input signal. Refer to the data bus signals for A, B, C, and D inputs.
$\overline{\text{BIT Ø}}$—$\overline{\text{15}}$	Sixteen-bit digital word defining display information from Computer to Display Unit.
BLANK	Unblanking signal to system oscilloscope from Display Unit's Control Card, A5.
BSO64—BSO4Ø96 (See N6—N12)	Signals to light BLOCK SIZE indication on Control Unit keyboard, and input block size to ADC.
BUSYØ	Signal to light BUSY indicator on Control Unit's keyboard.
C1, C2, C3	Code bits for Channel C OVERLOAD VOLTAGE switch, S9, indicating setting of that switch.
CC1, CC2	Code to indicate the position of input switch S4 or S5, which selects how many channels of analog data are to be analyzed.
CHA, CHB, CHC, CHD	Analog input signals to the input boards.
CHECK	Pulse (approximately 51 mV, 110 nsec wide) from Trigger Board Assembly. Serves as input test signal to ADC input channels.
CONT IN	Continue signal from keyboard to A15 (Function Generator) in Control Unit.
CONT OUT	Continue signal from A15 (Function Generator) to A16 (Switch Register) in Control Unit.
CP	Completed Plot signal from plotter to A7 (Plotter Control) in Display Unit.
CPP	Completed Plot Pulse from A7 (Plotter Control) to A5 (Control) in Display Unit.
D1, D2, D3	Code bits for Channel D OVERLOAD VOLTAGE switch, S10, indicating setting of that switch.
$\overline{\text{DAR}}$ (ADC)	Data Ready signal, from ADC to Computer. Indicates data is ready to be transferred to Computer.
$\overline{\text{DARENØ}}$, $\overline{\text{DAREN1}}$	Signals generated, but not used, by ADC.

continued on next page

Table 2-12. List of Mnemonics: Fourier Analyzer System (Continued)

SIGNAL	DEFINITION
$\overline{\text{DAR}}$ DISP KEY	Signal from Display Unit to Computer to indicate readiness to accept data word from Computer for Display.
$\overline{\text{DCMFS}}$	DISPLAY CALIBRATE MINUS FULL SCALE switch position (S8) to A2 Vertical DAC.
$\overline{\text{DCORG}}$	DISPLAY CALIBRATE ORIGIN switch position (S8) on Display Unit to A2 Vertical DAC.
$\overline{\text{DCPFS}}$	DISPLAY CALIBRATE PLUS FULL SCALE switch position (S8) on Display Unit to A2 Vertical DAC.
$\overline{\text{DFPLT}}$	"Low" level indicates DISPLAY FUNCTION switch S7 on Display Unit is in PLOT position.
DISP1, DISP2	Signals indicate position of the ADC DISPLAY switch. The channel selected for DISPLAY (A, B, C, or D) has bit "12" set for that ADC data word. Switch code is gated with OTA, OTB, OTC, or OTD, as selected on the A10 Sample Generator board in the ADC.
DISPCT	Indicates that the digital word being put onto the data bus should be displayed.
DONEA, DONEB, DONEC, DONED	Indicate that the analog-to-digital conversion in the indicated channel has been completed.
$\overline{\text{DSBL}}$	Provides an enable/disable signal from the DISPLAY FUNCTION switch on the Display Unit to the external X-Y Plotter.
DT	Indicates whether the SAMPLE MODE switch, S3, is in its "ΔFREQ" or "ΔTIME" position.
$\overline{\text{DTCNT}}$	"Low" level indicates DISPLAY TYPE switch (S9) on Display Unit is in its CONTinuous position.
$\overline{\text{DTPNT}}$	"Low" level indicates DISPLAY TYPE switch (S9) on Display Unit is in its POINT position.
$\overline{\text{DWCØ}}$—$\overline{\text{DWC3}}$	Contents of word counter on A4 board in Display Unit. If bit "15" of a data word sent to the Display Unit is set, the Data Word Counter is reset, indicating the first word of the display.
E BLANK+, E BLANK- (GND)	Unblanking signals from A5 (Control) in Display Unit to external oscilloscope.
$\overline{\text{EN}}$	Encode signal from Computer to ADC or Display Unit to start processing input signals.
ENAB	Indicates that triggering conditions have been satisfied in "external" sample mode.
ENN	Display Unit's internal "encode" signal.

continued on next page

Table 2-12. List of Mnemonics: Fourier Analyzer System (Continued)

SIGNAL	DEFINITION
ENN	ADC internal "on/off" signal.
$\overline{\text{EO}}$	SAMPLE MODE switch (S2) positions which enable "÷1000" on A10 Sample Generator Board. EO = "low" in Hz/ms (Δt/Fmax) and in the MHz/sec (ΔF/TOTAL TIME).
$\overline{\text{EXPNT}}$	Signal indicates command from Computer to light "X10" indicator on Display Unit.
EXSAMP	External Sample input from J1 to the ADC.
FIVE, $\overline{\text{FIVEX}}$	Signal indicates decoder command from Computer to light "5" indicator on Display Unit.
$\overline{\text{FOURIER}}$	"Low" level signal indicates system is operating as a Fourier Analyzer System. "High" level indicates system is operating as a stand-alone Computer. Determined by setting of FOURIER ANALYZER/COMPUTER NORMAL switch on Control Unit's keyboard.
FREE	Indicates that TRIGGER MODE switch, S6, is in FREE RUN position.
FREQ, $\overline{\text{FREQX}}$	Signal indicates decoded command from Computer to light "FREQ" indicator on Display Unit.
GAIN1, GAIN2, GAIN3	Signals indicate input OVERLOAD VOLTAGE switch setting of the digital word being put onto the data bus.
HLOAD	Clocks horizontal bits into A3 storage elements in Display Unit.
$\overline{\text{HM8}}$	"Low" level indicates HORIZONTAL MARKER switch (S6) on Display Unit is in the "8 PT" position, or "32 PT" position, and intensifies 8th or 32nd point on Oscilloscope display.
$\overline{\text{HOCTR}}$	Notifies Computer that HORIZONTAL ORIGIN switch (S5) on Display Unit is in the "CENTER" position, and display is to start at that point.
HOLD	Causes the sample-and-hold amplifier to disconnect from input signal and hold result on a capacitor
$\overline{\text{HOLFT}}$	Notifies the Computer that the HORIZONTAL ORIGIN switch (S5) on Display Unit is in the "LEFT" position, and display is to start at that point.
$\overline{\text{HOLOG}}$	Notifies the Computer that the HORIZONTAL ORIGIN switch (S5) is in the LOG position, and horizontal display is to be logarithmic.
HSIG+, HSIG- (GND)	Horizontal output voltage from A3 (Horizontal DAC) in Display Unit to the system oscilloscope.
HSIGE+, HSIGE- (GND)	Horizontal output voltage from A3 (Horizontal DAC) in Display Unit to the external oscilloscope.
$\overline{\text{HSSHLD}}$	Ground connection for VERTICAL MODE switch (S1) on Display Unit.

continued on next page

Table 2-12. List of Mnemonics: Fourier Analyzer System (Continued)

SIGNAL	DEFINITION
$\overline{\text{HS8.0}}$	"Low" level indicates Display Unit's VERTICAL MODE switch (S1) is in its "COMPLEX" position, and adjusts DAC gain for 8-cm sweep.
$\overline{\text{HS.8}}$, $\overline{\text{HS10}}$, $\overline{\text{HS.24}}$	"Low" level indicates Display Unit's HORIZONTAL SWEEP LENGTH switch (S4) is in its "12.8", "10", or "10.24" position (respectively), and adjusts Horizontal DAC gain. Also indicates VERTICAL MODE switch (S1) is not in its "COMPLEX" position.
INA, INB, INC, IND	Analog output signals from input board to digitizer board, in ADC.
LINE+, LINE- (GND)	50-Hz line source from Control unit to ADC clock generator.
$\overline{\text{LINE}}$	Input from Trigger Mode switch, S8.
LOG, $\overline{\text{LOGX}}$	Signal indicates decoded command from Computer to light the "LOG" and "dB" indicators on the Display Unit.
$\overline{\text{MID}}$	Signal from A5 (Control) in Display Unit for centering oscilloscope beaming bar display mode.
$\overline{\text{M1}}$—$\overline{\text{M15}}$	Outputs from the diode matrices to define the necessary ASCII characters for sixty Control Unit keyboard pushbuttons.
$\overline{\text{N6}}$—$\overline{\text{N12}}$	Seven signals used to indicate Block Size selected ("64" to "4096" words in binary increments). Same as BSO64-BSO4Ø96.
$\overline{\text{NEXT}}$, $\overline{\text{NEXT1}}$	Signals generated, but not used, by ADC.
ONE, $\overline{\text{ONEX}}$	Signal indicates decoded command from Computer to light the "1" indicator on the Display Unit.
OTA, OTB, OTC, OTD	Serve to output the digital data associated with the particular channel onto the data bus.
OTEN	Indicates that data is being enabled onto the data bus.
OVOLT	Signal which drives the OVERLOAD VOLTAGE indicator, DS2.
OVT	Signal sent to J16, indicating OVERLOAD VOLTAGE condition.
PEN1, PEN2 (GND)	Provides pen control from A5 (Control) in Display Unit to Plotter during "plot" mode.
$\overline{\text{PLAR}}$, $\overline{\text{PLARX}}$	Indicates decoded command from Computer to light "POLAR" indicator on Display Unit.
PLOT X+, PLOT X-	Horizontal output voltage from A3 (Horizontal DAC) in Display Unit to the Plotter.
PLOT Y+, PLOT Y-	Vertical output voltage from A2 (Vertical DAC) in Display Unit to the Plotter.

continued on next page

Table 2-12. List of Mnemonics: Fourier Analyzer System (Continued)

SIGNAL	DEFINITION
POW ON	Used to reset A14 (Shift Register) in Control Unit when power is first applied.
$\overline{\text{PTRIG}}$	Input from TRIGGER SLOPE switch, S11.
$\overline{\text{RATEX}}$	Input to A7 (Plotter Control) in Display Unit to determine plotting frequency.
RECT, $\overline{\text{RECTX}}$	Signal indicates decoded command from the Computer to light the "RECT" indicator on the Display Unit.
REMOTE	Indicates that the SAMPLE MODE switch (S2) is in its "REMOTE" position. Allows wired-OR signals from the remote control I/O card to control OVERLOAD VOLTAGE switch settings and SAMPLE MODE switch settings.
$\overline{\text{REPEAT}}$/(SINGLE)	"Low" level indicates that the REPEAT/SINGLE switch on the Control Unit's keyboard is in its "REPEAT" position. "High" level indicates the "SINGLE" position. Position information is routed to the Computer.
RESTART	Command from Control Unit's keyboard to restart the Fourier program
RESTART IN	Interrupt command from Control Unit's keyboard through A15 and A16 to the Computer.
$\overline{\text{RDYØ}}$	Lights "READY" indicator on Control Unit.
ROM ENAB	Read-only memory enable line from A14 (Shift Register) in Control Unit. Provides constant negative voltage to energize matrix diodes.
$\overline{\text{RUN}}$	ADC signal from A10 Board indicating that trigger conditions have been satisfied.
S1, S2	With X2 and X5, indicate position of MULTIPLIER switch S3 (see *Table 3-2*).
SAMP	Output of Sample Generator, A10, which serves to initiate a-to-d conversions and data transfers.
SAMIN	Indicates whether the External clock switch, S1, is in its EXT or INT position.
$\overline{\text{SAMPT}}$	Train of sample pulses from A10 (Sample Generator). Available at 5475A rear-panel BNC J21.
SEEK	Command from A7 (Plotter Control) in Display Unit enabling plotter to plot a specific point.
SFS, $\overline{\text{SFSX}}$	Signal indicates decoded command from the Computer to light the "–" indicator on the Display Unit.
STARTA, STARTB, STARTC, STARTD	Indicates digitizer is performing the analog-to-digital conversion on the indicated channel.
$\overline{\text{STEP}}$/(RUN)	"Low" level (STEP) causes program to proceed one step at a time. "High" level (RUN) causes program to proceed through steps automatically. From Control Unit keyboard switch position, to A16 (Switch Register) in Control Unit, to Computer.

continued on next page

Table 2-12. List of Mnemonics: Fourier Analyzer System (Continued)

SIGNAL	DEFINITION
STOP, STOP IN, STOP OUT	Keyboard command that relays a "halt" through the Control Unit to the Computer.
STOP LIGHT	Lights "READY" indicator on Control Unit's keyboard after STOP button has been pressed.
$\overline{\text{TRIG OUT}}$	Signal generated, but not used, by ADC.
TWO, $\overline{\text{TWOX}}$	Signal indicates decoded command from Computer to light "2" indicator on Display Unit.
UNCAL	Signal which drives the "UNCAL" LED, DS1. Derived on A7 (Error Board). Indicates that the selected combination of Block Size and SAMPLE CONTROL switch setting are beyond the range of the ADC.
$\overline{\text{VAS1}}$—$\overline{\text{VAS3}}$	Three-bit binary word defining position of VERTICAL POLAR ANG/DIV switch (S2) on Display Unit for Computer.
$\overline{\text{VDCMP1}}$	Notifies the Computer that the VERTICAL MODE switch (S1) on the Display Unit is in its "COMPLEX" position.
VDCMP2	Indicates to the Control Unit's A5 (Control) Board that the VERTICAL MODE switch is in its "COMPLEX" position.
$\overline{\text{VDI/P}}$	Notifies the Computer that the VERTICAL MODE switch (S1) on the Control Unit is in the "IMAGINARY/PHASE" position.
$\overline{\text{VDR/M}}$	Notifies the Computer that the VERTICAL MODE switch (S1) on the Control Unit is in the "REAL/MAGNITUDE" position.
V LOAD	Vertical load signal to A2 (Vertical DAC) in Display Unit.
VOUT A+	Input to Display Unit A1 (Vertical Amplifier) from GAIN control.
VOUT 1+	Output from Display Unit A2 (Vertical DAC) to GAIN control.
VOUT 2+	Vertical voltage output from Display Unit A2 (Vertical DAC) to external oscilloscope.
VPOSN1—VPOSN3	Inputs to Display Unit A1 (Vertical Amplifier) from POSITION control.
VSIGM, VSIGP	Output voltage to vertical deflection plates of system oscilloscope, from Display Unit A1 (Vertical Amplifier).
$\overline{\text{VS1}}$—$\overline{\text{VS5}}$	Five-bit binary word defining position of Display Unit's VERTICAL SCALE switch (S5) to Computer.
What Ø	Lights "WHAT?" indicator on Control Unit's keyboard.
$\overline{\text{XDTØ}}$—$\overline{\text{XDT1Ø}}$	Eleven-bit binary word defining horizontal display information to A3 (Horizontal DAC) in the Display Unit.
X2, X5	With S1 and S2, indicate position of MULTIPLIER switch S3 (see *Table 3-2*).
Z AXIS +, $\overline{\text{ZDT1}}$—$\overline{\text{ZDT5}}$	Z-axis CRT information (not used).

end of table

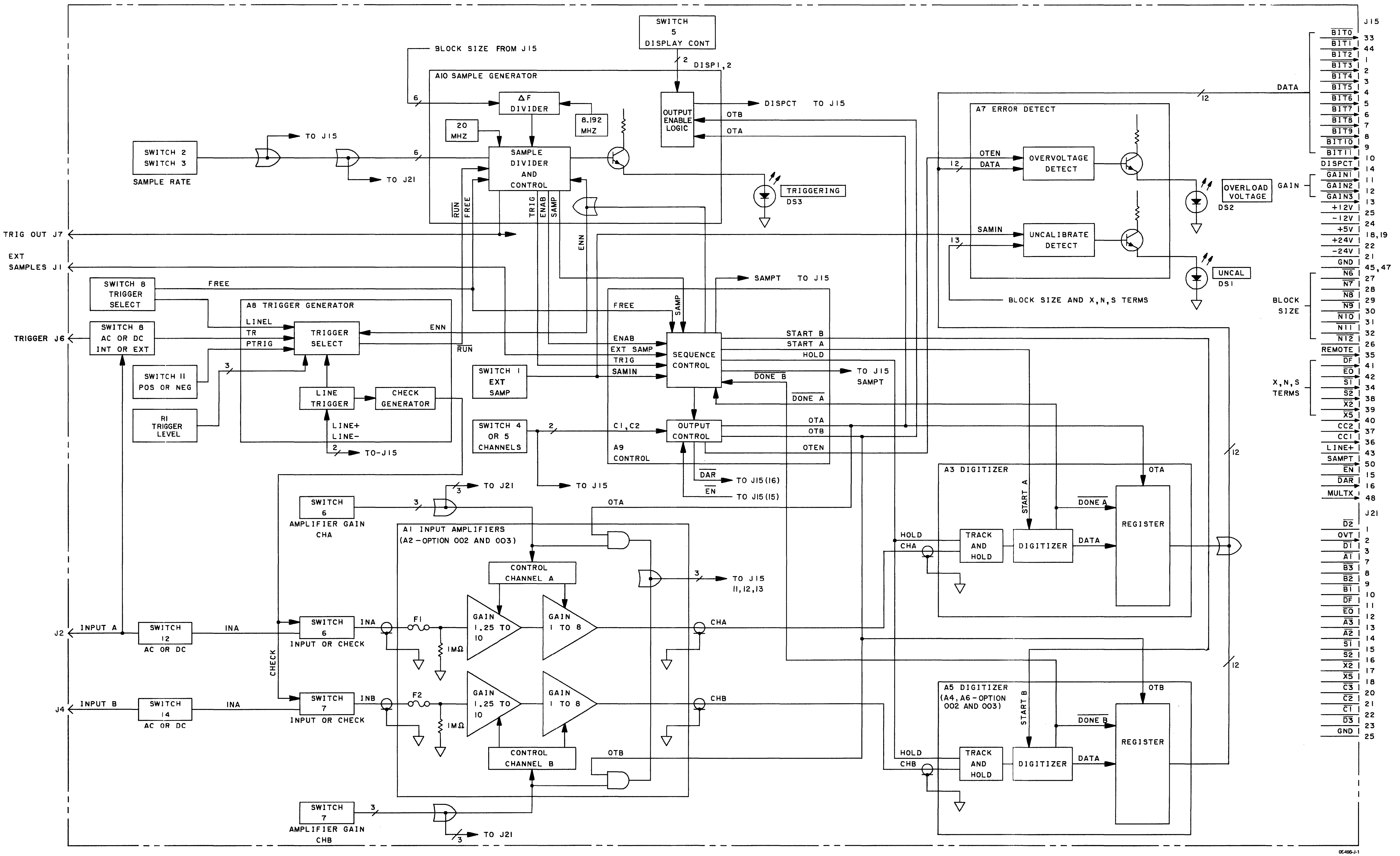


Figure 2-11
ADC FUNCTIONAL FLOW DIAGRAM

Table of Switches for Figure 2-12 (Continued)

Switch/Mnemonic	Switch Position	Connected To
EXT/INT (S1)		
SAMIN	(2)	XA9(13)
SAMPLE CONTROL SAMPLE MODE (S2)		
REMOTE	AFR(11)	S3AFR(3), P15(35)
GND	AF(7)	ground
DF	AF(3)	XA7(B)
EO	AF(8)	XA7(K)
SAMPLE CONTROL MULTIPLIER (S3)		
GND	AF(2),AR(2),BF(2),BR(2)	REMOTE S2AF(2), AR(2)
X2	AF(9)	XA10(6)
X5	AR(4)	XA10(7)
S1	BF(8)	XA10(3)
S2	BR(5)	XA10(4)
INPUT (S4) (4 channel only)		
GND	AF(1,2,3,10,11)	ground
CC1	AF(14)	XA9(21), J15(36)
CC2	AF(7)	XA9(20), J15(37)
DISPLAY INPUT (2 channel) (S5)		
CC1	AF(5)	XA9(2)
DISP1	AF(3)	XA10(J)
DISP2 (4 channel only)	AF(7)	XA10(H)
A OVERLOAD VOLTAGE (S6)		
INPUT A	BR(1)	S12(1)
IN A	BF(3)	XA1(20)
CHECK	B,FR(7)	XA8(15)[S9B, FR(7) 4 channel]
REMOTE	ARF(9)	S2AFR(11), S7AFR(9) [S9A,FR(9)]
GND	BF(2)	S7A, FR(9) [S7A, FR(9) 4 channel]
A1	AF(2,3)	XA1(16) P21(7)
A2	AF(5)	XA1(15) P21(14)
A3	AR(6)	XA1(T)
B OVERLOAD VOLTAGE (S7)		
INPUT B	BR(1)	S14(2) [S13(2) 4 channel]
IN B	BFR(3)	XA1(4)
CHECK	BFR(7)	XA8(15), S6BFR(7)
REMOTE	AFR(9)	S2A, FR(11), S6AFR(9)
GND	BF(2)	S14(5), XA1(3)

Table of Switches for Figure 2-12

Switch/Mnemonic	Switch Position	Connected To
B1	AF(2,3)	XA1(9) P21(3)
B2	AF(5)	XA1(8) P21(9)
B3	AR(6)	XA1(K) P21(8)
TRIGGER SOURCE (S8)		
CHA	BR(1)	XA3(20)
CHA	BR(7)	XA8(13)
TRIGGER INPUT	BR(3)	J6
FREE	AR(3)	XA9(P), XA10(13)
GND	AR(4)	ground
LINE	AR(5)	XA8(S)
C OVERLOAD VOLTAGE (S9) (4 channel only)		
INPUT C	BR(1)	S14(2) [S6B, FR(7) S10B, FR(7)]
IN C	BFR(3)	XA2(20)
CHECK	BFR(7)	XA8(15)
REMOTE	AFR(9)	S6AFR(9), S10AFR(9)
GND	BF(2)	J4, S14(5), ground
C1	AF(2,3)	XA2(16) P21(22)
C2	AF(5)	XA2(15) P21(21)
C3	AF(6)	XA2(T) P21(20)
D OVERLOAD VOLTAGE (S10) (4 channel ADC only)		
INPUT D	BR(1)	S15(2)
IN D	BR(3)	XA2(4)
CHECK	BFR(7)	XA8(15), S9BFR(7)
REMOTE	AFR(9)	S2A, FR(11), S9AFR(9)
GND	BF(2)	S14(5), XA2(13)
D1	AF(2,3)	XA2(9) P21(3)
D2	AF(5)	XA2(8) P21(1)
D3	AR(6)	XA2(K) P21(23)
TRIGGER SLOPE (S11/R1)		
P TRIG	S11R(4)	XA8(T)
ADJ2	R1(1)	XA8(19)
ADJ3	R1(2)	XA8(X)
ADJ1	R1(3)	XA8(W)
AC/DC SELECTORS		
INA (AC)	S12(1)	S6BR(1)
A INPUT	S12(2)	J3
INA	S12(3)	S6BR(1)
INB (AC)	S13(1)	S7BR(1)
B INPUT	S13(2)	J4
INB	S13(3)	S7BR(1)
INC (AC)	S14(1)	S9BR(1)
C INPUT	S14(2)	J5
INC	S14(3)	S9BR(1)
IND (AC)	S15(1)	S10BR(1)
D INPUT	S15(2)	J6
IND	S15(3)	S10BR(1)

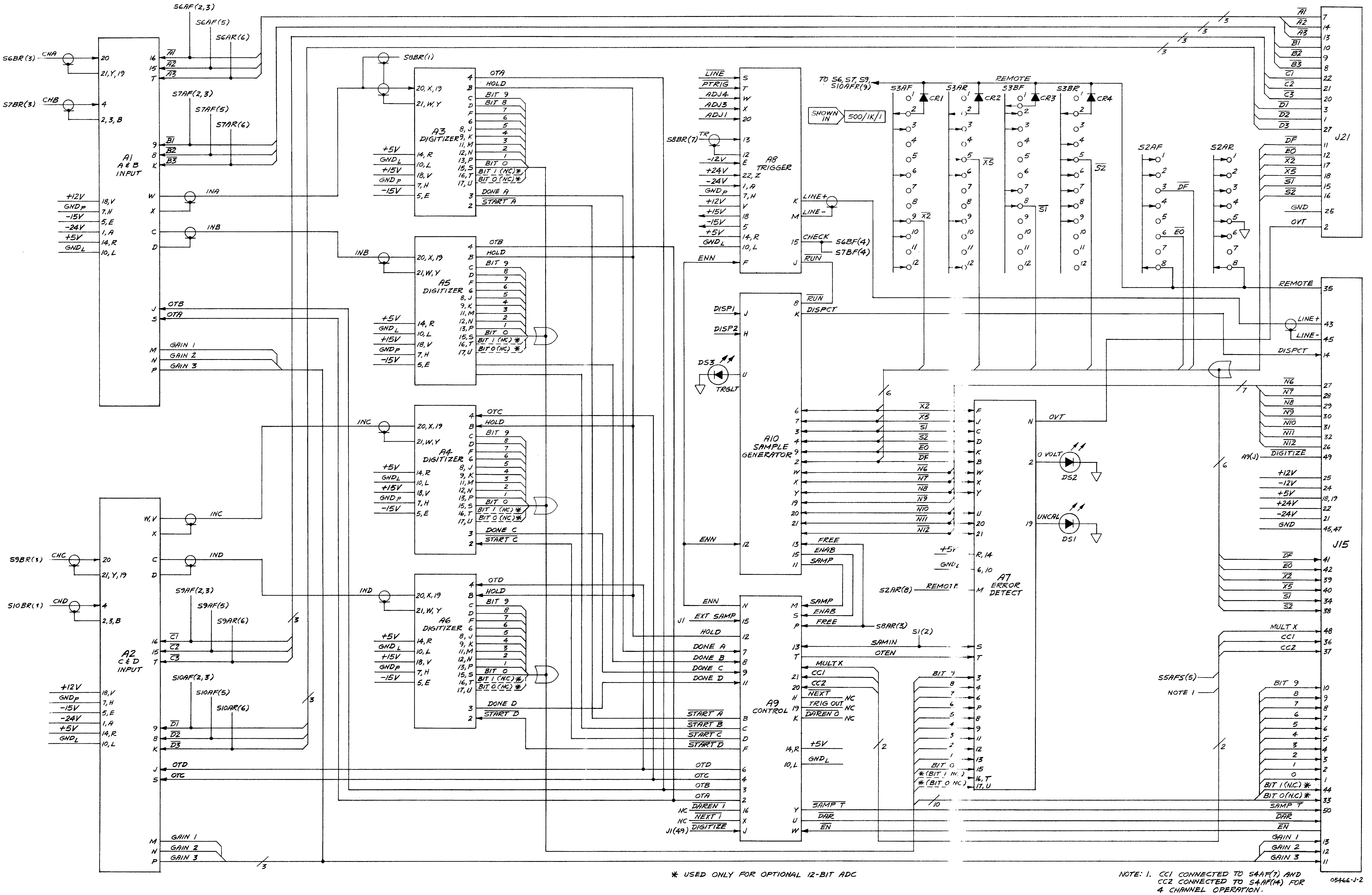


Figure 2-12
ADC WIRING DIAGRAM

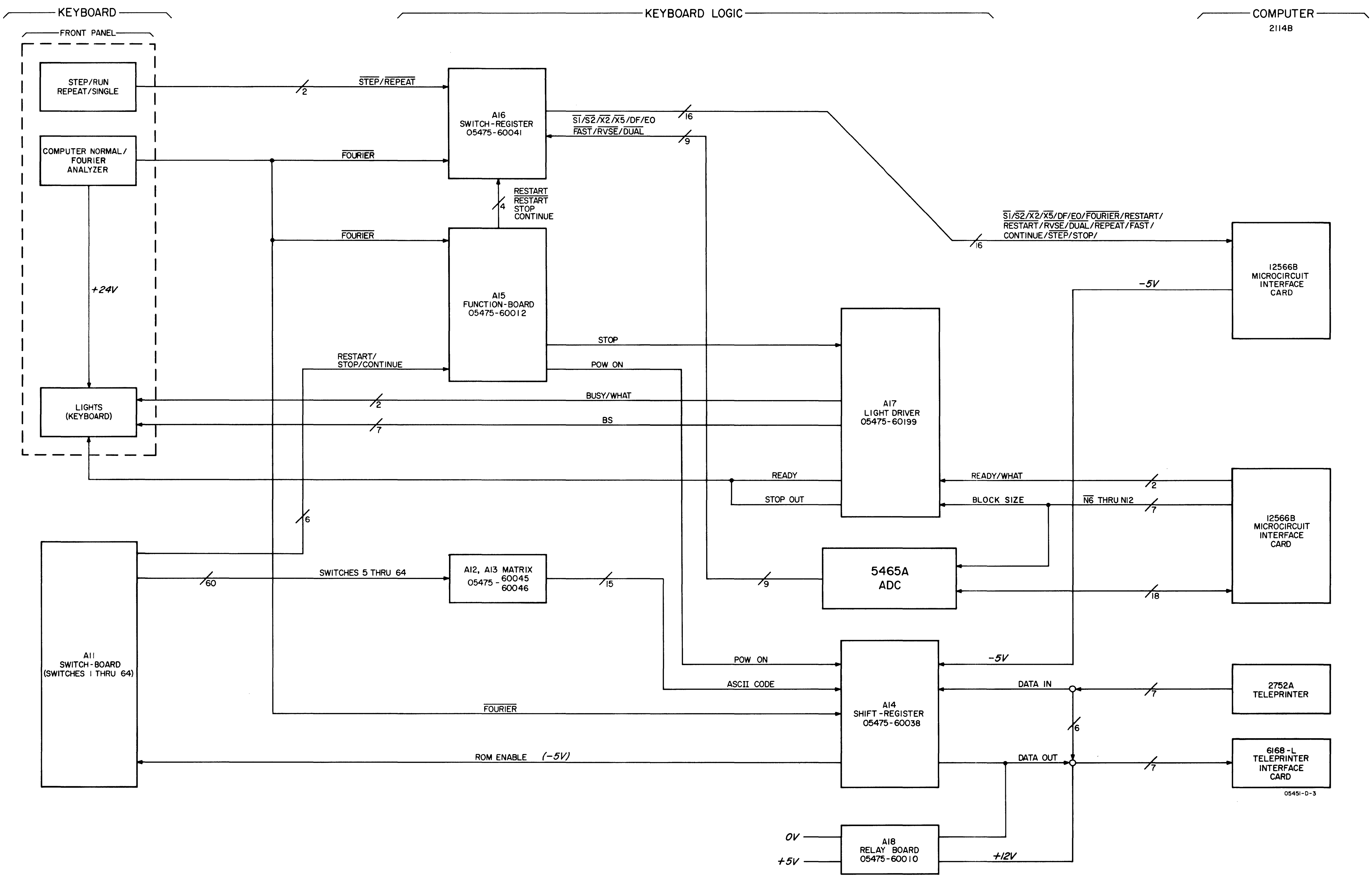


Figure 2-13
CONTROL UNIT BLOCK DIAGRAM

Table 2-13. Keyboard Signals to Matrix A and B

KEYBOARD CONNECTOR P19A/J19A	SIGNAL	MATRIX CONNECTOR	KEYBOARD CONNECTOR P19B/J19B	SIGNAL	MATRIX CONNECTOR
7	BLOCK SIZE	A12A(3)	11	SKIP	A12A(12)
8	POINT	A12A(4)	12	JUMP	A12A(13,P)
9	USER PROG	A12A(5)	13	COUNT	A12A(14,R)
11	DELET	A12A(6)	14	SUB RTRN	A12A(15)
12	RPLAC	A12A(7)	15	LABEL	A12A(S)
13	INSRT	A12A(8)	16	END	A12B(1,A)
14	LIST	A12A(9)	18	HISTOGRAM	A13A(C)
15	(?)	A12A(10)	19	RECT	A13A(D)
16	TERM	A12A(11)	20	LOAD	A13A(E)
18	MASS STORE	A12B(8,J)	21	STORE	A13A(F)
19	KEYBOARD	A12B(9,K)	22	LOG MAG	A13A(H)
20	PHOTO READR	A12B(10)	23	POLAR	A13A(J)
21	ANALG IN	A12B(11)	24	INTERCHNG	A13A(K)
22	ANALG OUT (OR BLANK)	A12B(12)	25	DSPLY	A13A(L)
23	PRINT	A12B(13)	36	(+)	A12B(2,B)
24	PUNCH	A12B(14)	37	(÷)	A12B(3,C)
25	BUFFD ANALG	A12B(15,S)	38	(←)	A12B(4,D)
35	ENTER	A13B(2)	39	(-)	A12B(5,E)
36	SPACE	A13B(3)	40	MULT	A12B(6,F)
37	CLEAR	A13B(4)	41	*MULT	A12B(7,H)
38	(-)	A13B(5)	43	(∫)	A13A(M)
39	RUB OUT	A13B(6)	44	HANN Ω	A13A(N)
41	(1)	A13B(8)	45	CONV	A13A(13)
42	(2)	A13B(9)	46	F	A13A(R)
43	(3)	A13B(L)	47	d/dx	A13A(S)
44	(4)	A13B(M)	48	TRANS FCN	A13A(14)
45	(5)	A13B(N)	49	CORR	A13A(15)
46	(6)	A13B(P)	50	POWER SPECT	A13B(1)
47	(7)	A13B(R)			
48	(8)	A13B(S)			
49	(9)	A13B(15)			
50	(0)	A13B(7)			

Table 2-14. Feedthru Signals — Computer to ADC

SIGNAL NAME	J15/P15 ADC CONNECTIONS	J12/P12 5475A CONNECTIONS	2 CH. 12566B I/O EDGE CONNECTIONS①	4 CH. 12930A I/O CONNECTIONS②
Signals from Computer:				
N6 (BSI 64)	27	20	H	10
N7 (BSI 128)	28	21	J	9
N8 (BSI 256)	29	22	K	18
N9 (BSI 512)	30	23	L	7
N10 (BSI 1024)	31	24	M	6
N11 (BSI 2048)	32	25	N	5
N12 (BSI 4096)	26	8	P	4
READY	NC	26	A	16
WHAT	NC	27	B	15
GND	NC	19,1	24,BB	50
Signals to Computer:				
BIT Ø③	33	33	5	37B
BIT 1③	44	35	6	36B
BIT 2③ (BIT Ø)④	1	18	7	35B
BIT 3③ (BIT 1)④	2	17	8	34B
BIT 4③ (BIT 2)④	3	16	9	33B
BIT 5③ (BIT 3)④	4	15	10	32B
BIT 6③ (BIT 4)④	5	14	11	31B
BIT 7③ (BIT 5)④	6	13	12	30B
BIT 8③ (BIT 6)④	7	12	13	29B
BIT 9③ (BIT 7)④	8	11	14	28B
BIT 10③ (BIT 8)④	9	10	15	27B
BIT 11③ (BIT 9)④	10	9	16	26B
GAIN 1	11	29	1	41B
GAIN 2	12	30	2	40B
GAIN 3	13	31	C,3	14B,39B
DISPCT	14	32	4	38B
EN	15	34	Z,22	24B
DAR	16	36	AA,23	49B

①Used with HP Cable No. 05451-60002.
②Used with HP Cable No. 05451-60004.
③Bit Ø—11 are used in 12-bit ADC.
④Bit Ø—9 are used in 10-bit ADC.

Table 2-15. Signal Outputs on Back of 5475A

SIGNAL	FROM	TO	5475A OPT.
SAMPLE OUT	J15(50)	J21	003, 004
EN OUT	J12(15)	J22	003, 004
DIGITIZE	J15(49)	J23	004
DAR	J15(16)	J24	004
MULTX SAMPLE	J15(48)	J25	006

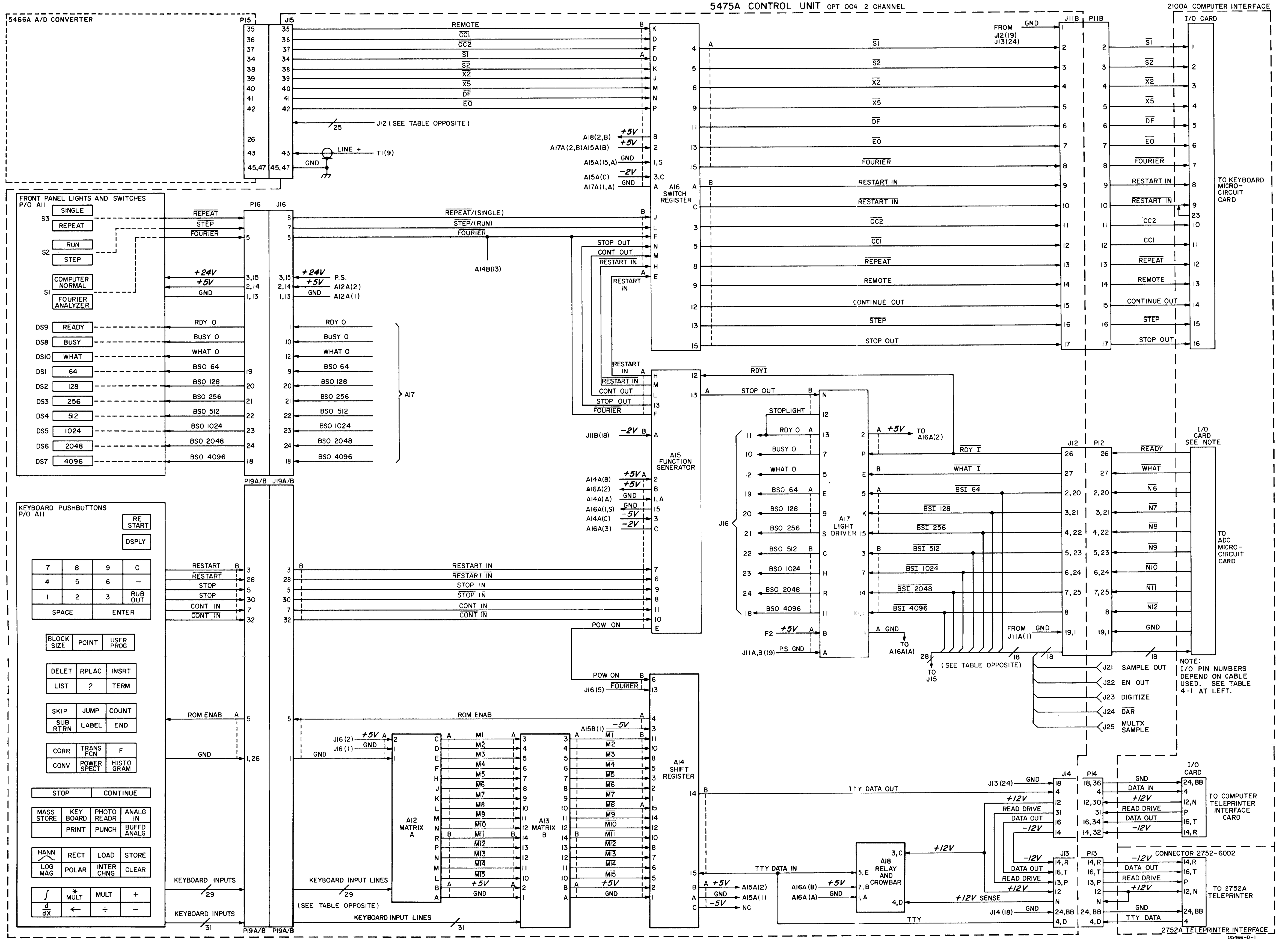


Figure 2-14
CONTROL UNIT WIRING DIAGRAM

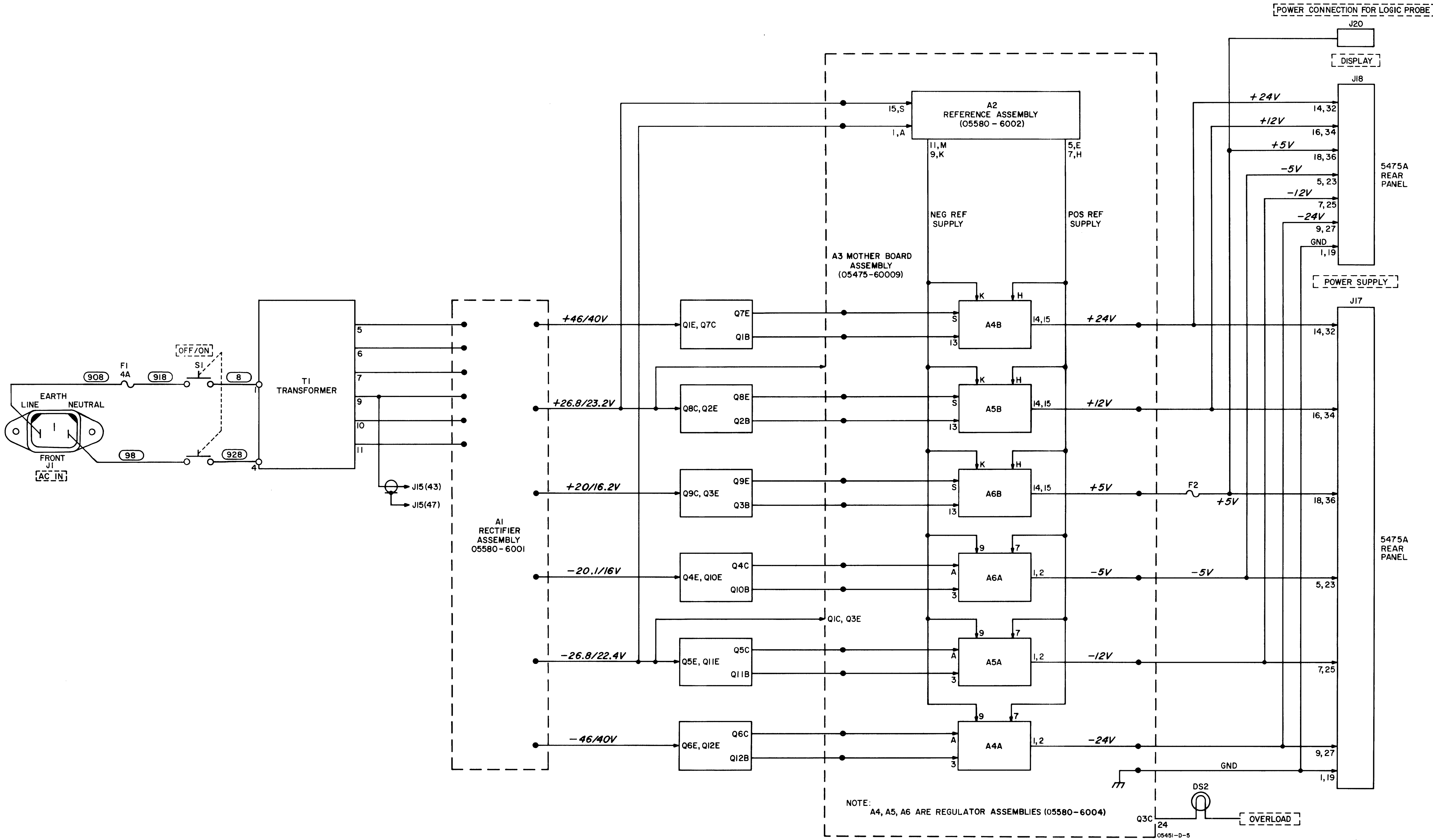


Figure 2-15
CONTROL UNIT POWER SUPPLY WIRING DIAGRAM

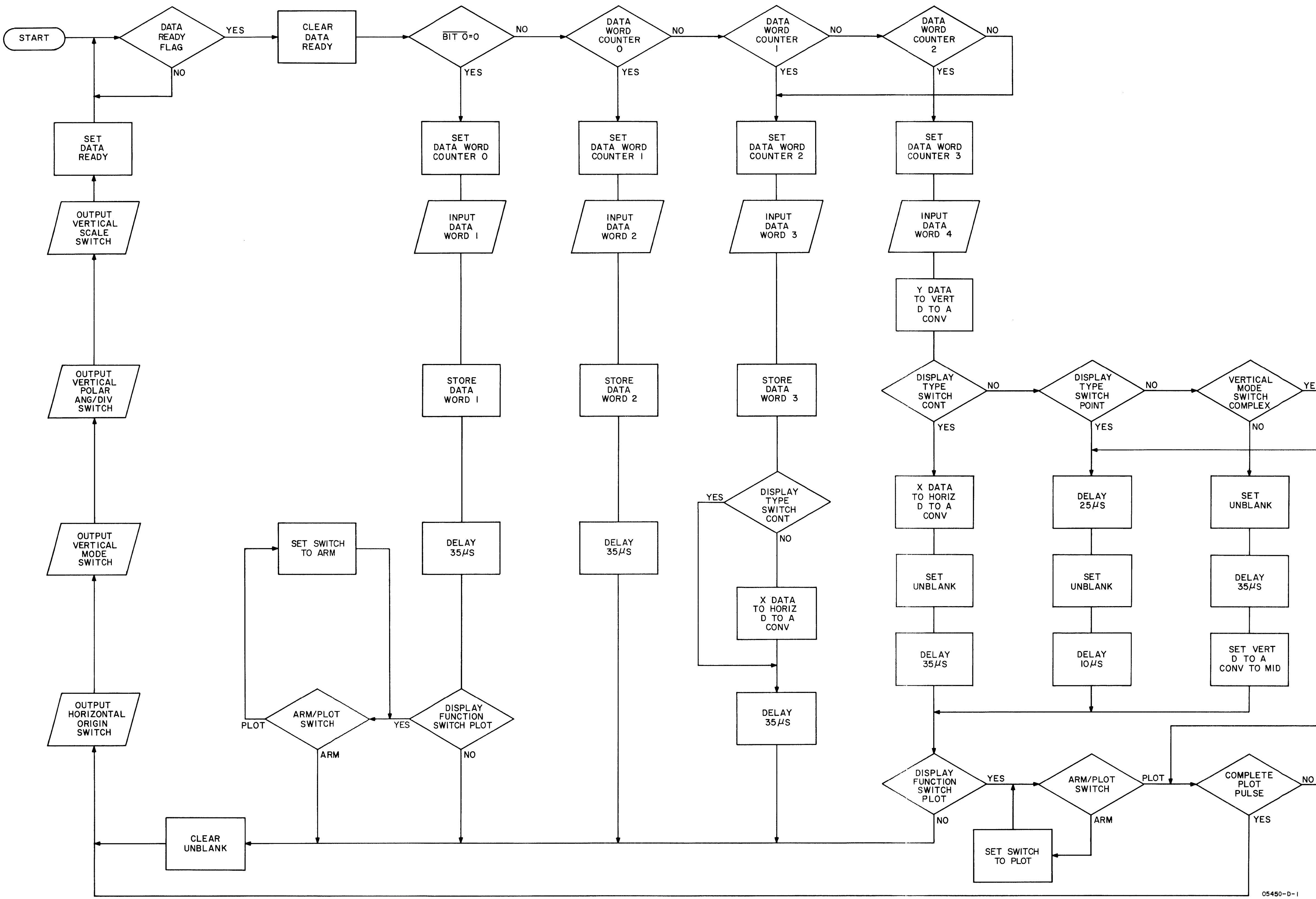


Figure 2-16
DISPLAY UNIT OPERATION FLOW DIAGRAM

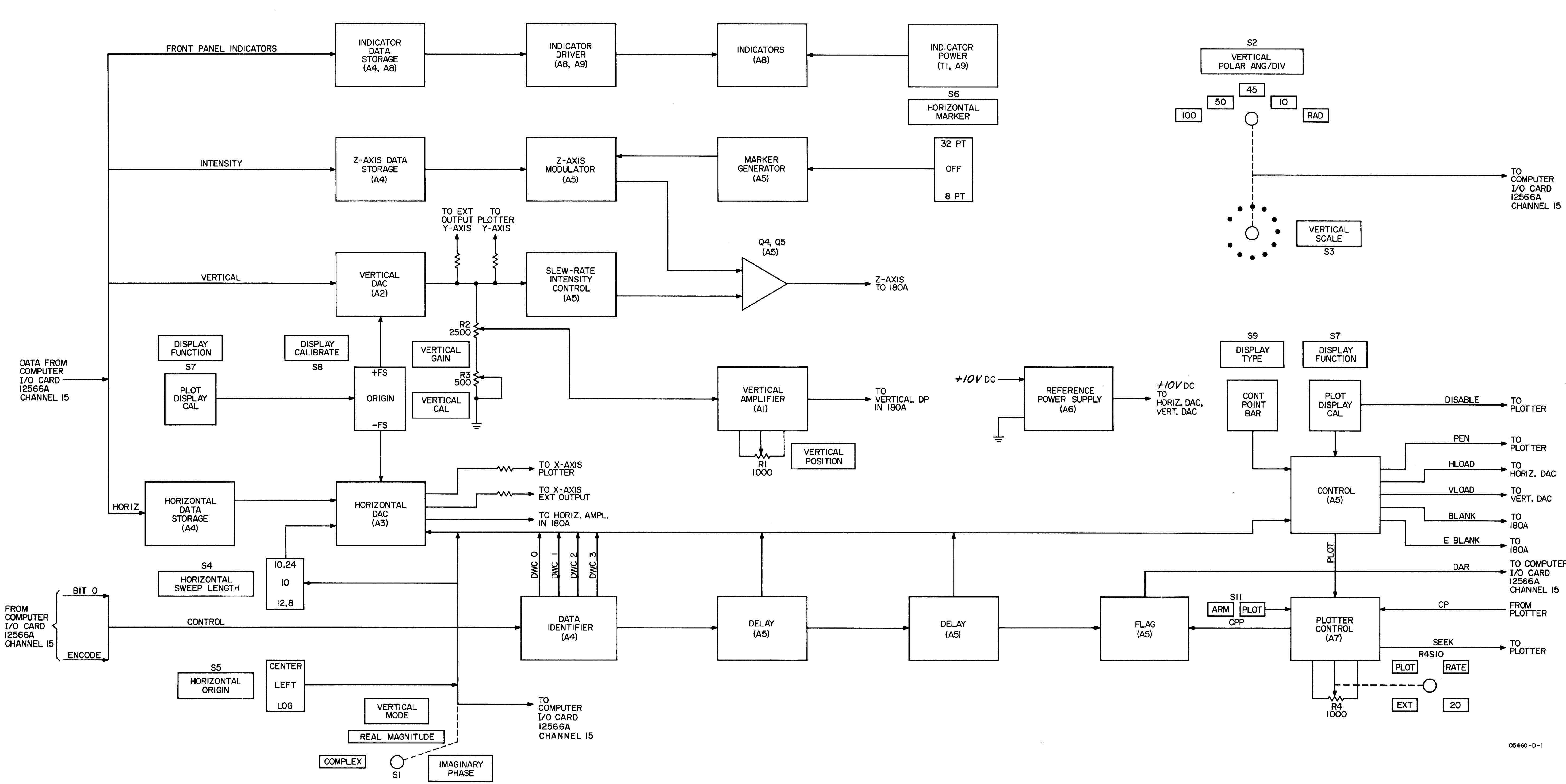


Figure 2-17
DISPLAY UNIT BLOCK DIAGRAM

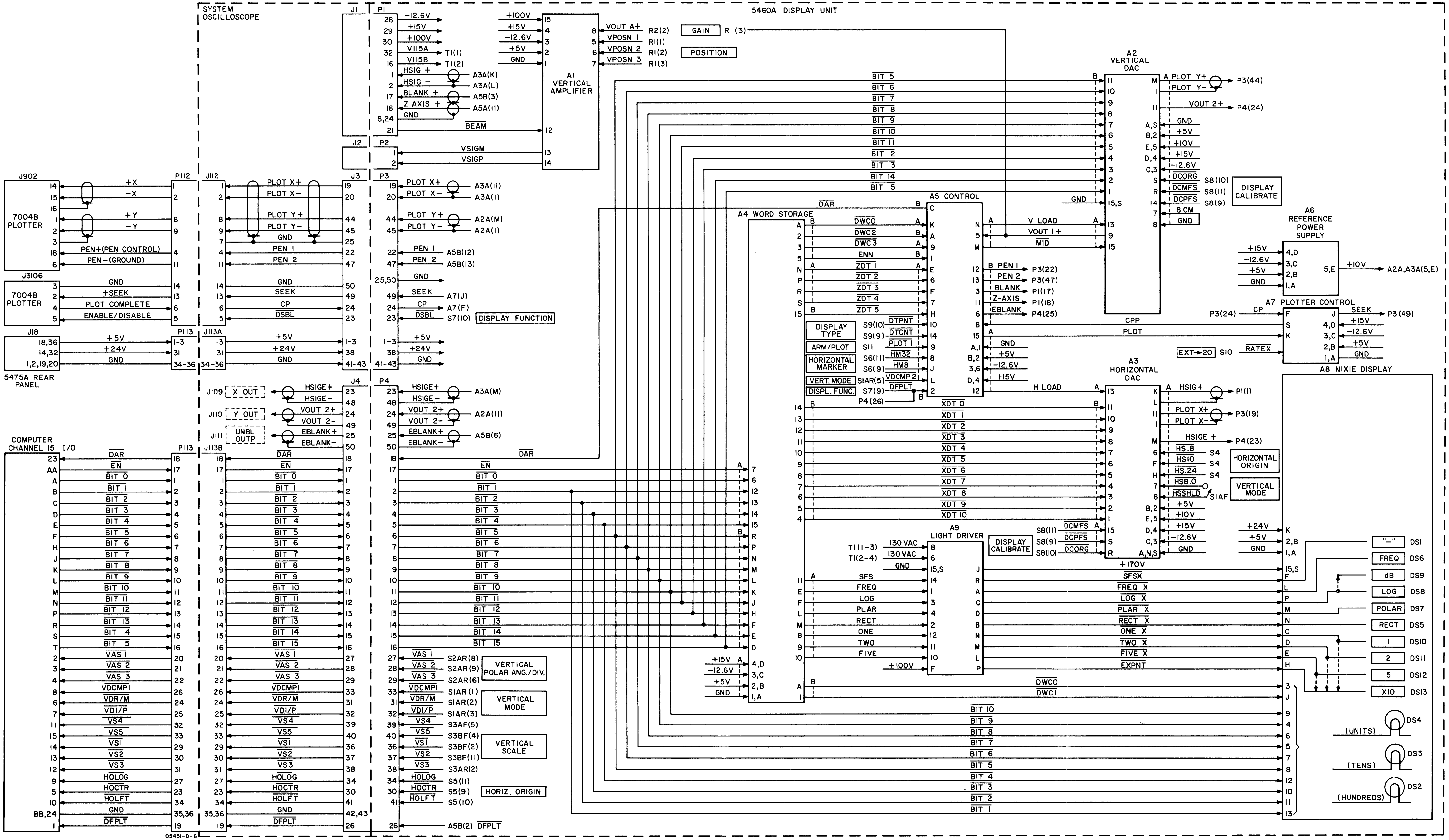


Figure 2-18
DISPLAY UNIT WIRING DIAGRAM

SECTION III

CHECKS AND ADJUSTMENTS

3.1 INTRODUCTION

This section provides a system checkout procedure for the 5451A Fourier Analyzer System. For additional operational checks of peripheral equipment supplied with the system or for checks as a stand-alone computer, refer to the applicable manuals. Adjustment procedures are provided for the 5460A Display Unit, 5466A ADC, and 5475A Control Unit. Refer to *Table 1-3* for a complete list of test equipment required.

3.2 SYSTEM TEST TAPE AND OPERATIONAL CHECK

The system test tape supplied with each Fourier Analyzer System provides an operational check of the Display Unit, the ADC, and the Control Unit Keyboard. System testing is arranged in subroutines to check out the computer input and output command and data transfer lines to the system. The system test tape writes over parts of the main Fourier program, and does not check the system software that performs the Fourier transform, or any of the other functions implemented by the systems software and called up via the keyboard; therefore, you must reload the main Fourier program to check these.

The system operational check verifies that the unique system units (5460A Display Unit, 5466A ADC, and 5475 Control Unit) are functioning properly. If a unit fails to perform a specific test, refer to the applicable troubleshooting procedure in Section IV.

3.2.1 Power Turn-on Procedure

a. If the system is rack-mounted, turn on rack power by pressing pushbutton in upper right corner, or moving switch inside rear to upper position.

b. Turn on power to oscilloscope by pressing green pushbutton. Green indicator lights.

c. Turn on power to Control Unit by pressing pushbutton. Indicator lights.

d. Turn on power to computer by turning key to POWER ON.

e. Auxiliary equipment should be left turned off until required in order to prevent unnecessary wear.

3.2.2 System Test Tape Loading

a. Load test tape (HP Part Number 05451-90021), using Photoreader or Teleprinter. Refer to Appendix A for instructions.

b. Set Computer's program register to 004000_8. (Press "P" button, CLEAR DISPLAY button, then button "11".)

c. Set Computer's switch register to Teleprinter interface channel address. (Press "S" button, enter channel number on display buttons; standard entry is "000011_8", refer to System Configuration Notice.)

d. Set Teleprinter switch to LINE.

e. Press Computer's INTERNAL PRESET, EXTERNAL PRESET, and RUN buttons.

3.2.2 System Test Tape Loading *(Continued)*

NOTE

Refer to HP 2100A Front Panel Procedures bulletin 5951-1371 for explanation of the Computer's front-panel pushbuttons.

f. Teleprinter prints out a series of statements requesting I/O channel locations. Answer each question by entering the appropriate channel number on the Teleprinter keyboard (press RETURN, LINEFEED, after each entry). If channel numbers are not known, refer to System Configuration Notice or 5475A rear panel. Standard configuration is:

Channel No.	Device
10	Photoreader
11	Teleprinter
12	Tape Punch
13	Jumper or Line Printer
14	ADC Data
15	Display
16	Control Unit Keyboard

Table 1-2 lists strapping requirements for the ADC Data, Display, and Keyboard interface cards.

3.2.3 Control Unit Tests and Subroutines

These checks test the Control Unit keyboard and functional operation. If a system fails any portion of these tests, refer to Control Unit troubleshooting in Section IV. The operational check troubleshooting is listed under the same heading as the test being performed. For example, troubleshooting for the preliminary keyboard test is contained in Section IV under preliminary keyboard test troubleshooting.

3.2.3.1 PRELIMINARY KEYBOARD TEST

a. Set COMPUTER NORMAL/FOURIER ANALYZER switch to COMPUTER NORMAL.

b. Press RESTART and BLOCK SIZE.

c. Verify that no characters are printed on the teleprinter.

d. Set switch to FOURIER ANALYZER.

e. Press keys as shown in *Table 3-1* and then press ENTER. (Press RESTART if not in READY mode.) Verify teleprinter prints correct characters.

NOTE

ASCII code for character appears in display register for each key depressed, should verification be necessary.

3.2.3.2 QK SUBROUTINE TEST

For this test, information is loaded through the keyboard interface card into the display register.

a. Type QK, (CR) Carriage Return (LF) Line Feed on the teleprinter.

NOTE

If BUSY is lighted perform step b then c. If READY is lighted perform step c then b.

Table 3-1. Preliminary Keyboard Test

Signal Name	Teleprint	Signal Name	Teleprint
BLOCK SIZE	BS	HANN	H1
POINT	/.	RECT	TR
USER PROG	Y ( ) †	LOAD	X<
DELET	/D	STORE	X>
RPLAC	/R	LOG MAG	TL
INSRT	/I	POLAR	TP
LIST	/L	INTER CHNG	X ( )
?	? ( )	CLEAR	CL
TERM	/ ( )	∫	$ ( )
SKIP	IF	*MULT	*-
JUMP	J ( )	MULT	* ( )
COUNT	# ( )	+	A+
SUB RTRN	< ( )	$\frac{d}{dx}$	% ( )
LABEL	L ( )	←	← ( )
END	. ( )	÷	: ( )
CORR	CR	—	A-
TRANS FCN	CH	1	1
F	F ( )	2	2
CONV	CV	3	3
POWER SPECT	SP	4	4
HISTOGRAM	RH	5	5
MASS STORE	MS	6	6
KEYBOARD	K ( )	7	7
PHOTOREADR	R ( )	8	8
ANALG IN	RA	9	9
(BLANK)	B ( )	0	0
PRINT	W ( )	-	-
PUNCH	P ( )	RUBOUT	(BELL)
BUFFD ANALG	RB	SPACE	( )
		ENTER	(CR) (LF)

† (   ) indicates one character space; to test this, press the key twice.

b. Press STOP. Verify bit 15 is on for 3 seconds, READY is on and BUSY is off after 3 seconds.

c. Press CONTINUE. Verify bit 13 is on for 3 seconds, READY is off and BUSY is on after 3 seconds. Press STOP again to return to READY mode for next test.

d. Set switches according to *Table 3-2* and verify bit lights.

text continues on page 3-5

Table 3-2. Switch Verification

Instrument	Switch and Setting	Computer Display Register Lamps
5475A	STEP/RUN = STEP	14 lighted
	STEP/RUN = RUN	14 off
	REPEAT/SINGLE = REPEAT	11 lighted
	REPEAT/SINGLE = SINGLE	11 off

Instrument	SAMPLE MODE SWITCH	Bit 12 (Remote)	Bit 5 (DF)	Bit 4 (EO)
5466A	REMOTE	on	on	on (bits 3,2,1, and Ø also "on" for REMOTE)
	kHz/μs	off	on	off
	ΔTIME Hz/ms	off	off	off
	ΔFREQ Hz/ms	off	on	on
	mHz/sec	off	off	on

Instrument	MULTIPLIER SWITCH	Bit 3 (X5)	Bit 2 (X2)	Bit 1 (S2)	Bit Ø (S1)
5466A	500/1K/1	on	off	off	off
	250/500/2	off	on	off	off
	100/200/5	on	on	on	on
	50/100/10	on	off	on	on
	25/50/20	off	on	on	on
	10/20/50	on	on	on	off
	100/10/5	on	off	on	off
	200/5/2.5	off	on	on	off
	500/2/1	on	on	off	on
	1K/1/.5	on	off	off	on
	2K/.5/.25	off	on	off	on
	5K/.2/.1	off	off	off	on

Instrument	DISPLAY/INPUT SWITCH (2-channel unit only)	Bit 10 (CC1)	Bit 9 (CC2)
5466A	A/A	off	on
	A/AB	on	on
	B/AB	on	on

Instrument	INPUT SELECTOR SWITCH (4-channel unit only)	Bit 10 (CC1)	Bit 9 (CC2)
5466A	A	off	on
	AB	on	on
	ABC	off	off
	ABCD	on	off

3.2.3.3 SK SUBROUTINE TEST

This subroutine tests the Control Unit response to its command lines sent from the computer through keyboard cable (J11).

a. Press RESTART. Verify teleprinter types START.

b. Type SK, (CR) , (LF) . Verify each keyboard front panel lights in a repetitive sequence. Note that BUSY goes off only when READY goes on.

c. Press RESTART. Verify teleprinter types START and program jumps out of light test loop.

3.2.4 Display Unit Tests and Subroutines

These checks test the Display Unit functional operation. If a system fails any portion of these tests, refer to Display Unit troubleshooting in Section IV. The operational check troubleshooting is listed under the same heading as the test being performed. For example, troubleshooting for the Display Unit SD subroutine test is contained in Section IV under SD subroutine test troubleshooting.

3.2.4.1 SD SUBROUTINE TEST

This subroutine controls the output to the Display Unit from the computer switch register.

a. Set COMPUTER NORMAL/FOURIER ANALYZER switch to COMPUTER NORMAL.

b. On the teleprinter type SD (CR) (LF) .

c. Set Display Unit FUNCTION switch to DISPLAY. Verify bit 15 light is off.

NOTE

If bit 15 light is on, the data ready flag (DAR) is not responding. Repeat procedure. If bit 15 light remains on, refer to troubleshooting.

d. Set switches according to *Table 3-3* and verify correct response. To enter computer switch register press S button; press MEMORY DATA after each bit.

text continues on page 3-7

Table 3-3. SD Subroutine Bit Test

Display Register	Pushbutton Light	Action
0	On	POLAR on. RECT off.
1	On	LOG on. dB on.
1	Off	Log off. dB off.
2	On	FREQ on.
2	Off	FREQ off.
3	On	Units counts 1—9, then blanks for 6 counts.
3	Off	Units readout of last count.
4	On	Tens, same as units
4	Off	Tens, same as units
5	On	Hundreds, same as units
5	Off	Hundreds, same as units
6	On	Minus (-) on
6	Off	Minus (-) off
7	On	5 on. X10 on.
7	Off	5 off. X10 off.

table continues on next page

Table 3-3. SD Subroutine Bit Test (Continued)

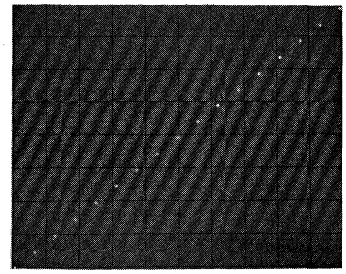
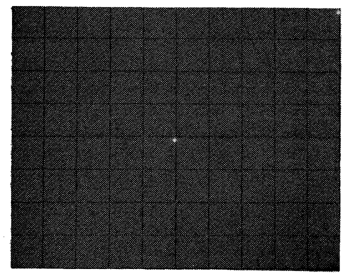
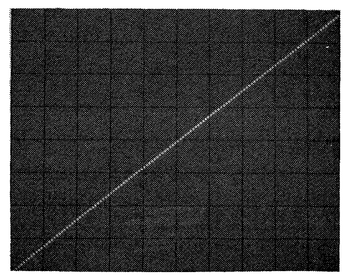
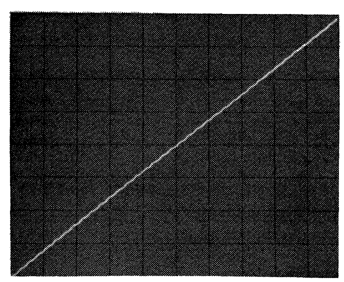
Display Register	Pushbutton Light	Action
8	On	2 on. X10 on.
8	Off	2 off. X10 off.
9	On	1 on. X10 on.
9	Off	1 off. X10 off.
10	On	17 points displayed: 
10	Off	3 points displayed: 
11	On	129 points displayed: 
11	Off	3 points displayed.
12	On	513 points displayed: 

table continues on next page

Table 3-3. SD Subroutine Bit Test (Continued)

Display Register	Pushbutton Light	Action
12	Off	3 points displayed.
13	On	1025 points displayed.
13	Off	3 points displayed.
14	On	2049 points displayed.
14	Off	3 points displayed.

NOTE

When using switches 10—14, the result of having the most significant bit switch on will be displayed. When using switches 12—14 it is difficult to determine the number of points displayed. However the length of time it takes to sweep can be used to determine if the correct number of points is displayed (i.e., it takes twice as long to sweep 2049 points as to sweep 1025 points).

end of table

e. Set up Display Unit controls as follows:

VERTICAL POSITION to center trace (knob at approximately 11 o'clock)

GAIN to CAL (switch engaged)

PLOT RATE to 20

ARM/PLOT to ARM

INTENSITY to approximately 4 o'clock

Place all other rotary switches to up position, and all slide switches to center position.

f. Press bit 11 on, all others off.

g. Set switches according to *Table 3-4* and verify correct response.

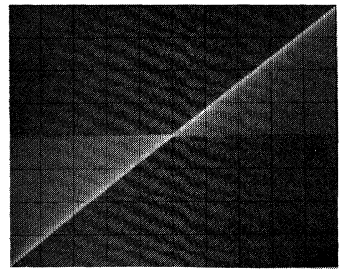
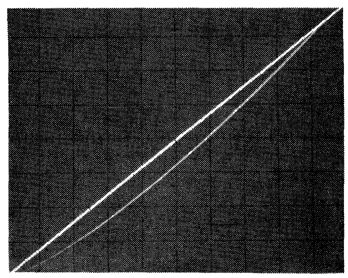
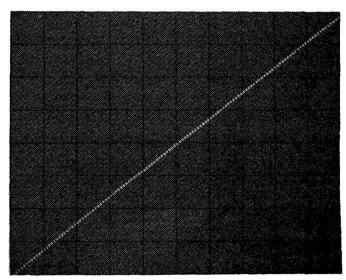
text continues on page 3-9

Table 3-4. SD Subroutine Display Test

5460A Switch Setting	Switch Effect
	Note: Adjust intensity to detect markers if necessary.
HORIZONTAL MARKER to:	
32 PT	Intensified trace every 32nd point.
8 PT	Intensified trace every 8th point.
OFF	No intensification of trace.
DISPLAY TYPE to BAR	Vertical bars on CRT from mid-scale to point being displayed. (Note: VERTICAL MODE switch in COMPLEX will disable vertical bar.)

table continues on next page

Table 3-4. SD Subroutine Display Test (Continued)

5460A Switch Setting	Switch Effect
DISPLAY TYPE to BAR	Vertical bars on CRT from mid-scale to point being displayed. (Note: VERTICAL MODE switch in COMPLEX will disable vertical bar.) 
CONT (Press bit 10 to on.)	Continuous line between each point being displayed. (Note: VERTICAL MODE must be set to REAL/MAGNITUDE.) 
POINT (Press bit 10 to on.)	Small dot at each point being displayed. 
(Set DISPLAY FUNCTION to CAL and DISPLAY CALIBRATE to -FS) HORIZONTAL SWEEP LENGTH to: (Press bit 10 to off.)	(Point displayed on CRT at horizontal position (cm).)
10.24	5.05 to 5.2
12.8	6.3 to 6.5
10	
VERTICAL MODE to:	
COMPLEX	3.95 to 4.05
REAL/MAGNITUDE	4.95 to 5.05
IMAGINARY/PHASE	4.95 to 5.05

end of table

3.2.4.2 QD SUBROUTINE TEST

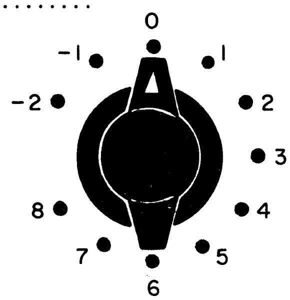
This test routine begins by sending out a display command word at all zeros. This word activates certain display indicators (e.g., RECT) then after 100 μsec, bit 15 should be cleared indicating an interrupt has been generated by the display through the computer interface card. A data word containing the display unit front panel switch setting (see *Table 3-5*) is then sent through the computer interface card and is displayed on the computer display register. Each time a display unit switch setting is changed an interrupt is generated and the displayed word is checked against the table.

a. Type QD, (CR), (LF).

b. Set switches according to *Table 3-5* and verify correct response.

Table 3-5. QD Subroutine Test

5460A Switch Setting	**Bits Affected and State: X = on, O = off**														
HORIZONTAL ORIGIN to:	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEFT						X	O				O				
LOG						O	X				O				
CENTER						O	O				X				
VERTICAL MODE to:															
COMPLEX								X	O	O					
REAL/MAGNITUDE								O	O	X					
IMAGINARY/PHASE								O	X	O					
VERTICAL SCALE to:															
-2 (Full CCW)	X	O	O	X	O										
-1	X	O	O	O	X										
0	O	O	O	O	O										
1	O	O	O	O	X										
2	O	O	O	X	O										
3	O	O	O	X	X										
4	O	O	X	O	O										
5	O	O	X	O	X										
6	O	O	X	X	O										
7	O	O	X	X	X										
8 (Full CW)	O	X	O	O	O										
POLAR ANG/DIV to:															
100												O	X	O	O
50												X	O	O	O
45												O	O	O	O
10												O	O	X	O
RAD												X	X	O	O



3.2.5 ADC Tests and Subroutines

These checks test the ADC functional operation. If a system fails any portion of these tests, refer to ADC troubleshooting in Section IV. The operational check troubleshooting is listed under the same heading as the test being performed. For example, troubleshooting for the SA subroutine test is contained in Section IV under the listing of SA subroutine test troubleshooting.

3.2.5.1 SA SUBROUTINE TEST

This subroutine sends the computer's switch register contents out through the ADC microcircuit I/O card to control ADC functions. Switch register bit "15" sets or clears the control to the I/O card.

3.2.5.1.1 Triggering Tests

This check tests that all ADC triggering modes are operating. Activating bit "15" enables an ENcode signal to the ADC, arming the triggering cycle.

a. Type SA (CR) (LF).

b. Set controls as follows:

   5466A:

   OVERLOAD VOLTAGE (A and B): ".125"

   TRIGGER LEVEL: "12 o'clock"

   SAMPLE MODE: INT., kHz/μs

   MULTIPLIER: 50/100/10

   DISPLAY/INPUT (2 channel): A/A
   DISPLAY (4 channel): A
   INPUT (4 channel): A

   Keyboard:

   COMPUTER NORMAL/FOURIER ANALYZER: FOURIER ANALYZER

   Computer:

   Bit "15": off ("0")

c. Set 5466A TRIGGER SOURCE to FREE RUN.

   TRIGGERING lamp should be "off".

d. Set Computer bit "15" "on" ("1").

   TRIGGERING lamp should light, indicating that the trigger circuit is armed.

e. Set Computer bit "15" "off" ("0").

   TRIGGERING lamp should turn "off".

f. Set 5466A TRIGGER SOURCE to LINE.

   Repeat steps "d" and "e" above.

please continue on next page

3.2.5.1.1 Triggering Tests *(Continued)*

g. Set 5466A TRIGGER SOURCE to INTERNAL (A). Set OVERLOAD VOLTAGE A to CHECK.

   Repeat steps "d" and "e". Slight TRIGGER LEVEL adjustment may be required.

h. Set controls as follows:

   5466A:

   TRIGGER SOURCE: EXT. DC

   Computer:

   Bit 15: "off"

i. Connect a 100 Hz, 100 mV rms sine wave from an external source through a 50-ohm feedthrough connector to the 5466A TRIGGER INPUT connector.

j. Repeat steps "d" and "e".

   Slight TRIGGER LEVEL adjustment may be necessary.

k. Change TRIGGER INPUT signal to 10 kHz, 100 mV rms (through the 51-ohm feedthrough termination).

l. Repeat steps "d" and "e".

   Slight TRIGGER LEVEL adjustment may be required.

3.2.5.1.2 UNCAL Test

Certain combinations of SAMPLE MODE and MULTIPLIER switch settings indicate a MAX FREQ or TOTAL TIME range that is beyond the sampling capability of the ADC. In these conditions, the analyzer is UNCALibrated. If you select one of these combinations, the UNCAL lamp lights. The UNCAL test is a part of the "SA" test.

a. Set switches according to *Table 3-6*.

b. Verify that the UNCAL lamp lights only at the appropriate switch settings.

3.2.5.2 QA SUBROUTINE TEST

The Query Analog subroutine transfers data from the ADC via the ADC's I/O channel. If bit "3" ("DISPCT") of the ADC's data word is "1", the word will be presented on the Computer's display unit. The binary word is converted to a BCD word which is sent to the display channel to be displayed on the NIXIE® display. A word in which bit "6" ("BLOCK SIZE 64") is "1" and all other bits are "0" is then sent to the ADC channel, and, after a 50 msec delay, the cycle is repeated.

3.2.5.2.1 Calibration Check

This test receives information from the 5466A, and displays it as a digital number on the 5460A Display Plug-in's readout tubes. This portion of the QA test also checks operation of the DISPLAY switch.

please continue on next page

Table 3-6. UNCAL Test

5466A		Set **Computer** Switch Register Bits (All switches off unless noted.)	5466A
SAMPLE MODE	MULTIPLIER		UNCAL Lamp Status
INT.ΔTIME, kHz/μs	500/1K/1 250/500/2 All other settings	All switches off	On On Off
INT.ΔTIME, Hz/ms	All Settings	All switches off	Off
INT.ΔFREQ, Hz/ms	500/1K/1 250/500/2 100/200/5 50/100/10 25/50/20 All other settings	12 on	On On On On On Off
	500/1K/1 250/500/2 100/200/5 50/100/10 All other settings	11 on	On On On On Off
	500/1K/1 250/500/2 100/200/5 All other settings	10 on	On On On Off
	500/1K/1 250/500/2 All other settings	9 on	On On Off
	500/1K/1 All other settings	8 on	On Off
	All Settings	7 on, then 6 on	Off
INT.Δf mHz/sec	All Settings	6 thru 12 on	Off
EXT All settings	All Settings		On

3.2.5.2.1 Calibration Check *(Continued)*

Depending on the options, if any, that were ordered, the ADC may have two or four digitizing channels, and these channels will have either 10-bit or 12-bit digitizers. This procedure can be used to check any version.

The digitizers operate like zero-center voltmeters. A "zero-volt" input gives a readout of the binary equivalent of zero counts. "Full-scale" positive or negative input voltage on any input rrange gives an output equivalent of ±512 counts for a 10-bit ADC, or ±2048 counts for a 12-bit ADC.

The procedure below determines the approximate accuracy of the 5466A ADC by using the CHECK pulse, supplied internally, and noting the ADC output. This 51 mV pulse is fed into the digitizer at the equivalent of the ".125" (volt) range. *Table 3-7* is provided as a convenient worksheet for determining the approximate accuracy of your ADC's channels.

3.2.5.2.1 Calibration Check *(Continued)*

a. Type QA (CR) (LF) to begin the test routine.

b. Set controls as follows:

Computer:

For 12-bit digitizers, set bit "15" to "1".

ADC:

SAMPLE MODE: INT, kHz/μs

MULTIPLIER: 10/20/50

DISPLAY/INPUT (2-channel): A/AB

DISPLAY (4-channel): A

INPUT (4-channel): ABCD

OVERLOAD VOLTAGE (all): CHECK

TRIGGER SOURCE: INTERNAL (A)

AC/DC (all): DC

SLOPE: NEG

TRIGGER LEVEL: approximately "2 o'clock" (verify that Display indicators flicker)

c. Adjust TRIGGER LEVEL control until ADC triggers, indicated by 5460A readout changing.

d. Measure the dc zero offset of the CHECK signal by reading the number in the 5460A Display Unit's readout; this number should be 000±8 counts for 10-bit ADC, or 000±16 for 12-bit ADC.

Record this "initial value" for the appropriate channel in the chart in *Table 3-7.*

please continue on next page

Table 3-7. Calibration Check — Worksheet

	CHANNEL A	CHANNEL B	CHANNEL C	CHANNEL D
Final Value	________	________	________	________
Initial Value[1]	________	________	________	________
Difference[2] (Final — Initial)	________	________	________	________

[1,2]

Specs:	Initial Value[1]	Difference[2]
10-bit	000±8	209±5 (204-214)
12-bit	000±16	836±10 (826-846)

3.2.5.2.1 Calibration Check *(Continued)*

e. Set 5466A SLOPE to POS.

f. If necessary, adjust TRIGGER LEVEL until ADC triggers.

g. Record the number now displayed on the 5460A as the "final value" in the chart in *Table 3-7.* The difference between this and the "initial value" must be 209 ±5 counts for a 10-bit ADC, or 836 ±10 counts for a 12-bit ADC.

h. Repeat steps "b" through "g" for the remaining ADC channels. For 2-channel unit, set DISPLAY/INPUT to B/AB to display channel B. For 4-channel unit, set DISPLAY successively to "B", "C", and "D".

3.2.5.2.2 OVERLOAD VOLTAGE Switch Tests

These tests are part of the "QA" test group. Each OVERLOAD VOLTAGE switch setting provides an output code to the Computer. These tests ensure that the OVERLOAD VOLTAGE gain codes are correct for all settings of all switches.

a. Type QA (CR) (LF)

b. Set controls as follows:

5466A:

SAMPLE MODE: kHz/μs

MULTIPLIER: 50/100/10

TRIGGER SOURCE: FREE RUN

Computer:

For 12-bit ADC, bit "15" to "1".

c. Set DISPLAY/INPUT to A/A or A/AB, or DISPLAY to A (depending on your ADC unit).

d. Check Computer display for each OVERLOAD VOLTAGE A position. It should be as shown in *Table 3-8.*

e. Repeat step "d" for OVERLOAD VOLTAGE switches B, C, and D. (Set DISPLAY/ INPUT or DISPLAY control to channel you want to check.)

Table 3-8. Attenuator Code Test

OVERLOAD VOLTAGE SETTING	COMPUTER DISPLAY REGISTER		
	Bit 2	Bit 1	Bit 0
CHECK	ON	OFF	OFF
.125	ON	OFF	OFF
.25	ON	OFF	ON
.5	ON	ON	OFF
1	OFF	ON	ON
2	OFF	ON	OFF
4	OFF	OFF	ON
8	OFF	OFF	OFF

please continue on next page

3.2.5.2.3 Attenuator Code "Bit 2" Test

This test is an extension of the OVERLOAD VOLTAGE Switch Tests given on the previous page. In this test, bit "2" must remain "high" for all OVERLOAD VOLTAGE attenuator settings.

a. Type QM (CR) (LF) .

b. Set controls as follows:

   5466A:

   SAMPLE MODE: MAX FREQ Hz/ms

   MULTIPLIER: 50/100/10

   TRIGGER SOURCE: FREE RUN

   Computer:

   For 12-bit ADC's, bit "15" to "1".

c. Set DISPLAY/INPUT or DISPLAY control to display channel A only.

d. Check Computer display for each position of OVERLOAD VOLTAGE A.

   Bit "2" must be "on" for each setting.

e. Repeat step "d" for the remaining ADC Channel(s), setting the DISPLAY/INPUT or DISPLAY control as required, and using the appropriate OVERLOAD VOLTAGE control.

3.2.5.2.4 ADC Gain Check

The gain check confirms that OVERLOAD VOLTAGE switch codes set up the corresponding gain in the input amplifiers.

a. Type QA (CR) (LF) .

b. Set controls as follows:

   Computer:

   Bit "10": "on" ("1")

   For 12-bit ADC, bit "15" to "1".

   5466A:

   SAMPLE MODE: INT.

   MULTIPLIER: 10/20/50

   ΔFREQ/TOTAL TIME: Hz/ms

   TRIGGERING: FREE RUN

   SLOPE: POS

   TRIGGER LEVEL: "12 o'clock"

please continue on next page

3.2.5.2.4 ADC Gain Check *(Continued)*

DISPLAY/INPUT (2-channel): A/AB

INPUT (4-channel): ABCD

DISPLAY (4-channel): A

c. Connect the HP 6115A Precision Power Supply to all 5466A Inputs (A, B, C, D), either simultaneously or consecutively.

d. Set Power Supply output and 5466A OVERLOAD VOLTAGE A according to *Table 3-9*, and conform readout.

For all combinations listed in *Table 3-9*, the readout should be:

"409±5" (405–413) for 10-bit digitizer

"1636±20" (1620–1652) for 12-bit digitizer

These numbers should be negative when the input voltages are negative.

Table 3-9. OVERLOAD VOLTAGE Gain Check

5466A OVERLOAD VOLTAGE SETTING	INPUT SIGNAL AMPLITUDE ("+" and "–")
8	6.400V
4	3.20V
2	1.60V
1	800 mV
.5	400 mV
.25	200 mV
.125	100 mV

e. Repeat steps "b" through "d" for Channels B, C, and D. Set DISPLAY/INPUT or DISPLAY switch to display channel with which you are working.

3.2.5.3 SAMPLE RATE TEST

This test checks the sample frequency set up by the SAMPLE CONTROL switches. The SAMPLE MODE codes have already been checked (3.2.3.2, QK Test).

3.2.5.3.1 Internal Sample Rate Tests

a. Type SA (CR) (LF) .

b. Set Controls as follows:

5466A:

TRIGGERING: FREE RUN

SAMPLE MODE: INT

Computer:

All "S" bits "off".

please continue on next page

3.2.5.3.1 Internal Sample Rate Tests *(Continued)*

c. Connect the Sample Out signal from 5475A rear-panel BNC connector to input of a HP 5300A/5303 Option 001 Counter. Set Counter's GATE TIME to 1 second. (As an alternate, the Counter's input could be connected to the "SAMP" test point on the 5465A's A10 Sample Generator Assembly.)

d. Set SAMPLE CONTROL switches according to *Table 3-10*. Observe results. Be sure to note that the sample frequency is divided down (see Calibration and Adjustments section for frequency adjustment).

Table 3-10. ΔTIME Sample Rate Test

5466A SAMPLE CONTROLS		FREQUENCY
kHz/μs	500/1K/1	1.000000 MHz ± .000005 MHz
	250/500/2	500.000 kHz ± .003 kHz
	100/200/5	200.000 kHz ± .002 kHz
	50/100/10	100.000 kHz ± .001 kHz
	25/50/20	50.000 kHz ± .001 kHz
	10/20/50	20.000 kHz ± .001 kHz
	100/10/5	10.000 kHz
	200/5/2.5	5.000 kHz
	500/2/1	2.000 kHz
	1K/1/.5	1.000 kHz
	2K/.5/.25	.500 kHz
	5K/.2/.1	.200 kHz
ms/Hz	500/1K/1	1.000 kHz
	250/500/2	.500 kHz
	100/200/5	.200 kHz

e. Set SAMPLE MODE to Δf, Hz/ms, and MULTIPLIER to 500/1K/1.

f. Set the Computer bit specified in *Table 3-11* "on", and all other bits "off".

Output frequency should correspond to that given in the Table.

Table 3-11. ΔFREQ Sample Rate Test

All Computer Bits "off", except:	FREQUENCY
12	4.096000 MHz ± .000010 MHz
11	2.048000 MHz ± .000005 MHz
10	1.024000 MHz ± .000003 MHz
9	512.000 kHz ± .002 kHz
8	256.000 kHz ± .001 kHz
7	128.000 kHz ± .001 kHz
6	64.000 kHz

please continue on next page

3.2.5.3.2 External Sample Test

This test runs the ADC at a very fast rate to "stress check" the ADC.

a. Set controls as follows:

   HP 3310B Function Generator:

   FUNCTION: Square Wave

   REP RATE: 100 kHz

   OUTPUT LEVEL: HIGH

   AMPLITUDE: 0 to 3 volts peak

   NOTE: You can measure this amplitude (p-p) by connecting the 3310B's output to the EXT. HORIZ. INPUT of the 5451A's oscilloscope.

   5466A:

   SAMPLE MODE: EXT

   TRIGGER MODE: FREE RUN

b. Connect the 3310B Pulse Output to a 5300/5303A Counter. Set Counter's GATE TIME to 1 second.

c. Connect the Function Generator's output to the 5466A's EXT. sample input connector.

d. Allow five minutes warm-up for the 3310B before observing frequency.

e. Type QA (CR) (LF) .

f. Observe that the 5466A's TRIGGERING lamp blinks dimly.

g. TYPE SA (CR) (LF) .

h. Set Computer bit "15" to "1" ("on").

i. Connect the 5300A/5303A Counter's input to the "START" test point on the 5466A's A9 Control Card assembly.

j. Observe that the measured frequency is 100 kHz ± 10 Hz.

3.2.5.4 REMOTE PROGRAMMING TEST

This test checks the Remote Programming codes that are transmitted between the Computer and the ADC. This test is required only when the 5475A is wired to enable remote control of the ADC (see *Table 2-1*).

a. Set 5466A controls as follows:

   SAMPLE MODE: REMOTE

   TRIGGER MODE: FREE RUN

   OVERLOAD VOLTAGE (all): 8V

please continue on next page

3.2.5.4 REMOTE PROGRAMMING TEST *(Continued)*

b. Type SM (CR) (LF) .

c. For four-channel ADC, only, set bit "14" to "1".

d. Set bit "15" to "1". The Remote Programming test routine will run, and then type "START" on the Teleprinter. If an error occurs, the Computer will HALT.

   In case of a Computer HALT during this test, refer to "SM" in the "Troubleshooting" section of this manual.

3.2.5.5 FOURIER SAMPLE RATE TEST

This test ensures correct operation of the ADC in the main Fourier program by setting certain sample rates and inserting corresponding known input signals.

a. Load the main Fourier Program, 05451-90011, using the standard TAPE LOADING procedure.

NOTE

Be sure that you have completed all procedures that use the test tape program. The main Fourier program writes over locations in which the test program is stored, destroying the test program.

b. To run the main Fourier Program, press "P", then "CLEAR DISPLAY", then "1" (to enter starting address "000002"), then both PRESETs, then "RUN".

c. Set controls as follows:

   5466A:

   OVERLOAD VOLTAGE (all) to "1".

   TRIGGER SOURCE: INTERNAL (A)

   TRIGGER LEVEL: 12 o'clock

   DISPLAY/INPUT (2-channel): A/AB

   DISPLAY (4-channel): A

   INPUT (4-channel): ABCD

   AC/DC (all): DC

   5460A:

   Lever switches (all): Centered

   SCALE: straight up

   VERTICAL POSITION: To center trace on CRT

   VERTICAL GAIN: CAL.

   MODE: REAL/MAGNITUDE

   ARM/PLOT: ARM

please continue on next page

3.2.5.5 FOURIER SAMPLE RATE TEST *(Continued)*

Keyboard:

REPEAT/SINGLE: REPEAT

COMPUTER NORMAL/FOURIER ANALYZER: FOURIER ANALYZER

d. Connect 3301B oscillator sinewave output through 51-ohm feedthrough to all 5466A INPUTs (A,B,C,D). Set DC OFFSET to 0V.

   Monitor the oscillator's amplitude, to maintain 0.6V rms output at all frequencies.

e. Enter a block size of 128 by pressing BLOCK SIZE, 1, 2, 8, and ENTER, in that order.

   ABLOCK SIZE 128 lamp should light.

f. Enter into the record-taking mode by pressing ANALG IN, and ENTER, in that order.

g. Observe the Display Unit's oscilloscope for each combination of 5466A control settings given in *Table 3-12*.

h. Set controls as follows:

   Keyboard:

   REPEAT/SINGLE: SINGLE

   5466A:

   SAMPLE MODE: ΔFREQ Hz/ms

   MULTIPLIER: 5/10/100

NOTE

In the ΔFREQ mode, changing a BLOCK SIZE does not affect the total time required to take a single record (make one complete sweep); therefore, no change in the period of the input will be noted when changing block sizes.

i. Set sine wave oscillator frequency to 10 Hz.

j. Enter sweeping mode by pressing ANALG IN, and ENTER, in that order.

   CRT displays one cycle of sine wave.

k. Repeat the above procedure for block sizes 64, 256, 512, and 1024.

   The CRT displays one cycle of sine wave at each block size.

l. If your system's Computer's memory is large enough to enable other block sizes (e.g., 2048, 4096), check those block sizes, too. If these sizes are not available, "WHAT" will light.

please continue on next page

Table 3-12. ADC Sample Rate Test

DISPLAY/INPUT		5466A Switches		Oscillator	CRT Display
Two Channel	Four Channel	SAMPLE MODE	MULTIPLIER	Frequency at .6V	(Sinewave May not be centered on Screen)
A/AB	A/ABCD B/ABCD	ΔFREQ/TOTAL TIME Hz/ms	10/20/50	20 Hz	1
B/AB	B/ABCD C/ABCD D/ABCD	ΔFREQ/TOTAL TIME Hz/ms	10/20/50	20 Hz	1
A/AB	A/ABCD B/ABCD C/ABCD D/ABCD	ΔFREQ/TOTAL TIME Hz/ms	2.5/5/200	10 Hz	2
A/AB B/AB	A/ABCD D/ABCD	ΔFREQ/TOTAL TIME Hz/ms	5/10/100	10 Hz	1
A/AB B/AB	A/ABCD D/ABCD	MAX FREQ/ΔTIME kHz/μs	1k/1.5	7.8 Hz	1
A/AB B/AB	A/ABCD D/ABCD	MAX FREQ/ΔTIME Hz/ms	50/100/10	7.8 Hz	10*

*NOTE: Set DISPLAY TYPE to CONT to view 10 cycles of waveform.

3.2.5.6 DUAL SPECTRUM SUBTRACT TEST

This test ensures that all channels in the ADC are matched, by subtracting one input from another.

a. Set controls as follows:

5466A:

SAMPLE MODE: kHz/μs

MULTIPLIER: 5/10/100

DISPLAY/INPUT (2-channel): A/AB

DISPLAY (4-channel): A

INPUT (4-channel): ABCD

TRIGGER SOURCE: FREE RUN

TRIGGER SLOPE: POS

OVERLOAD VOLTAGE (all): .125

AC/DC (all): AC

please continue on next page

3.2.5.6 DUAL SPECTRUM SUBTRACT TEST *(Continued)*

Keyboard:

FOURIER ANALYZER/COMPUTER NORMAL: FOURIER ANALYZER

5460A:

DISPLAY TYPE: POINT

Oscillator:

Frequency: 100 Hz

Amplitude: 30 mV, terminated in 51Ω

b. Connect Oscillator's output to 5466A's A,B,C,D INPUTs through "T" connectors and a 50-ohm termination.

c. Enter a BLOCK SIZE of 256 by pressing the BLOCK SIZE, 2, 5, 6, and ENTER keys in that order.

   BLOCK SIZE 256 lamp should light.

d. Enter into the record-taking mode by pressing ANALG IN, SPACE, 1, SPACE, and ENTER, in that order.

   Data will be accepted from the ADC as follows:

   Channel A to Block 1
   Channel B to Block 2
   Channel C* to Block 3
   Channel D* to Block 4

   *4-channel ADC only

   Following this data transfer, the Fourier Analyzer will automatically display the contents of Block 1.

e. Press F, 1, SPACE, 2, ENTER. (For 4-Channel ADC, also press F, 3, SPACE, 4, Enter.)

NOTE
Performing steps "f" and "g" subtracts block 1 (channel A's information) from block 2 (channel B's information).

f. On keyboard, press LOAD, 1, ENTER, arithmetic "–", 2, and ENTER.

g. Rotate the 5460A's DISPLAY SCALE switch clockwise, if required, until the readout section of the Display Unit shows a scale factor of 5×10^{-4}.

   The CRT display should be a group of random dots, representing the difference. The spread ("noise") of the pattern should not be greater than two major divisions, vertically. Check both REAL and IMAGINARY with the 5460A DISPLAY SELECTOR switch.

h. Repeat the above procedure from step "d" by setting MULTIPLIER switch for a sample rate of 2.5/5/200 (place DISPLAY SCALE switch in its "12 o'clock" position).

please continue on next page

3.2.5.6 DUAL SPECTRUM SUBTRACT TEST *(Continued)*

i. For 4-channel ADC, press LOAD, 1, ENTER, then arithmetic "–", 3, ENTER, to obtain "A–C". Observe results as in step "g" above.

j. For 4-channel ADC, press LOAD, 1, ENTER, then arithmetic "–", 4, ENTER, to obtain "A–D". Observe results as in step "g" above.

3.2.5.7 ADC DIGITIZER TEST

a. Connect the 3310A Function Generator Channel A to Channel A of the 5466A.

b. Connect the output of the 3310A Function Generator to the 5466A's EXT. TRIG input.

c. Set controls as follows:

Function Generator:

FREQUENCY: 800 Hz

FUNCTION: TRIANGLE

5466A:

SAMPLE MODE: INT, kHz/μs

MULTIPLIER: 100/200/5

DISPLAY/INPUT (2-channel): A/AB

DISPLAY (4-channel): A

INPUT (4-channel): ABCD

OVERLOAD VOLTAGE (all): 8

AC/DC (all): DC

TRIGGER MODE: EXT. DC

TRIGGER SLOPE: NEGATIVE

Keyboard:

SINGLE/REPEAT: REPEAT

d. Set block size of 256.

e. Press ANALG IN, ENTER.

f. The 5466A's TRIGGERING lamp should be blinking.

g. Approximately one cycle of a triangle wave should appear on the display oscilloscope.

h. Adjust the 3310A's Channel A AMPLITUDE control until the 5466A's OVERLOAD lamp just starts to blink.

i. Move the Keyboard's SINGLE/REPEAT switch to SINGLE.
All points of the waveform should be continuous, without missing levels or severe non-linearities. The waveform should appear approximately like the one represented in *Figure 3-1*.

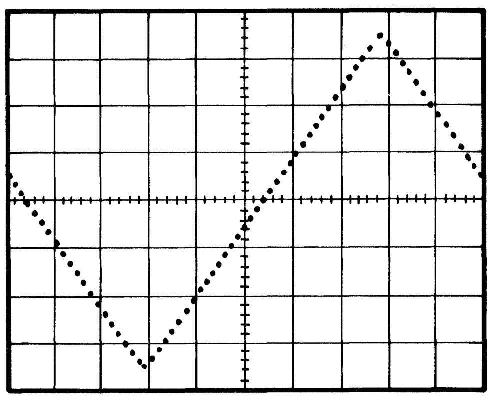
please continue on next page

3.2.5.7 ADC DIGITIZER TEST *(Continued)*

j. Repeat the above procedure for the remaining ADC channels as follows:

1) Disconnect the triangle signal from its current input, and connect it to the next higher channel.
2) Set the INPUT/DISPLAY or DISPLAY switch to the channel currently receiving the triangle input.
The triangle wave should be displayed.

Figure 3-1. Triangle Waveform



3.2.6 Power-on Test

This check ensures that when Fourier Analyzer System power is lost, the system goes to a HALT mode. There should be no loss of memory, and it should not be necessary to reload the system tape.

a. Verify that system test tape is loaded and operating.

b. Set FOURIER ANALYZER/COMPUTER NORMAL switch to FOURIER ANALYZER.

c. Turn off system power.

d. Wait 5 seconds then turn on system power.

e. Verify Computer comes up in the RUN mode, and that the Display Unit is sweeping, and that the READY light is "on".

3.3 ADJUSTMENTS AND CALIBRATION

Adjustment and calibration for the 5460A Display Unit, 5466A ADC, and the 5475A Control Unit are contained in the following paragraphs. *Table 3-13* summarizes the adjustments for each unit. Do not perform any adjustments not listed in the Table. Always remove power before removing or replacing any system units or circuit boards.

3.3.1 Display Unit Adjustment and Calibration

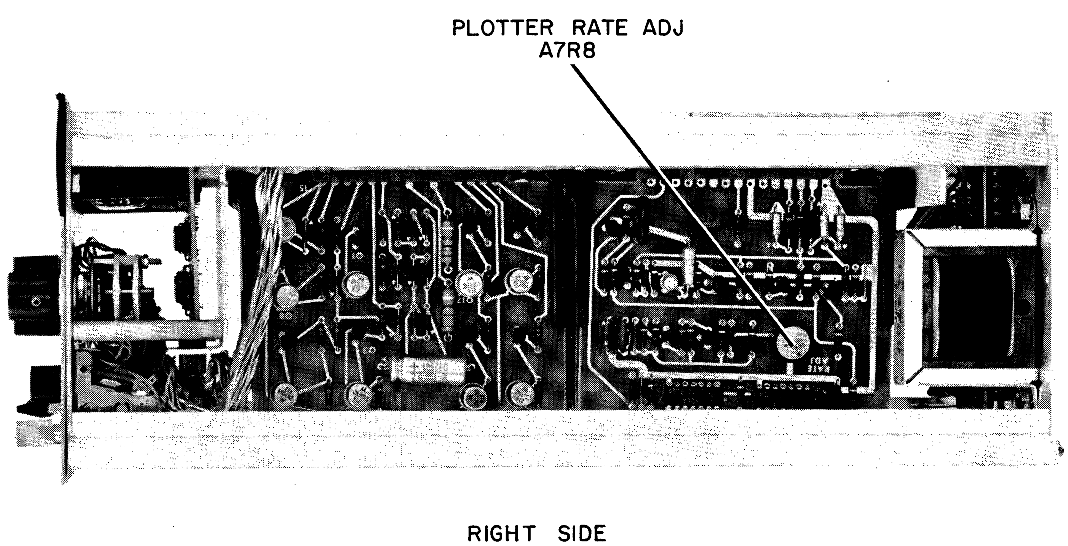
The procedures require that the 5460A plug-in be removed from the oscilloscope mainframe and its top and bottom covers removed. The 5460A is assumed connected to the oscilloscope through the 10603A Display Service Extender. Refer to Section I of this manual for detailed access information. See *Figure 3-2* for physical location of test points.

please continue on next page

Table 3-13. Adjustments and Calibration Procedures

UNIT	PROCEDURE
Display Unit	Bus Voltage Measurement Reference Voltage Adjustments Horizontal DAC Output Voltage Adjustments Horizontal CRT Gain Adjustments Vertical DAC Output Voltage Adjustments Vertical CRT Gain Calibration
ADC	A1 (and A2) Input Assembly Adjustments (DC Offset Adjustments) A3, A5 (and A4, A6) Digitizer Assembly Adjustments (DC Offset Adjustment) A10 Sample Generator Assembly Adjustments a. Adjust 20.00 MHz Crystal Oscillator. b. Adjust 8.192 MHz Crystal Oscillator.
Control Unit	Power Supply Adjustments a. Preliminary Instructions b. Voltage Adjustments c. Overcurrent Control Adjustment Oscillator Adjustment

Figure 3-2a. Display Unit Test Points



3.3.1.1 EQUIPMENT REQUIRED

The following equipment or the equivalent is required to perform these procedures:

HP Model 412A DC Vacuum Tube Voltmeter
HP Model 3460A Digital Voltmeter (6-digit readout)
Short Clip Lead
HP 10603A Service Extender Kit

please continue on next page

3.3.1.2 BUS VOLTAGE MEASUREMENTS

The voltage readings listed below are those for normally operating power supplies. There are no voltage adjustments for these supplies in the 5460A unit. Refer to Control Unit adjustments and oscilloscope manual for adjustments. See *Figure 3-2b* for test point location.

Test Point (all in 5460A)	Voltage (with respect to ground)
XA1(15)	+95V to +105V
XA8(15,S)	+165V to +180V
XA1(4)	+14.5V to +15.5V
XA1(3)	-12V to -13V
XA1(2)	+4.5V to +5.5V
XA8(2,B)	+4.5V to +5.5V
XA8(K)	+22V to +25V

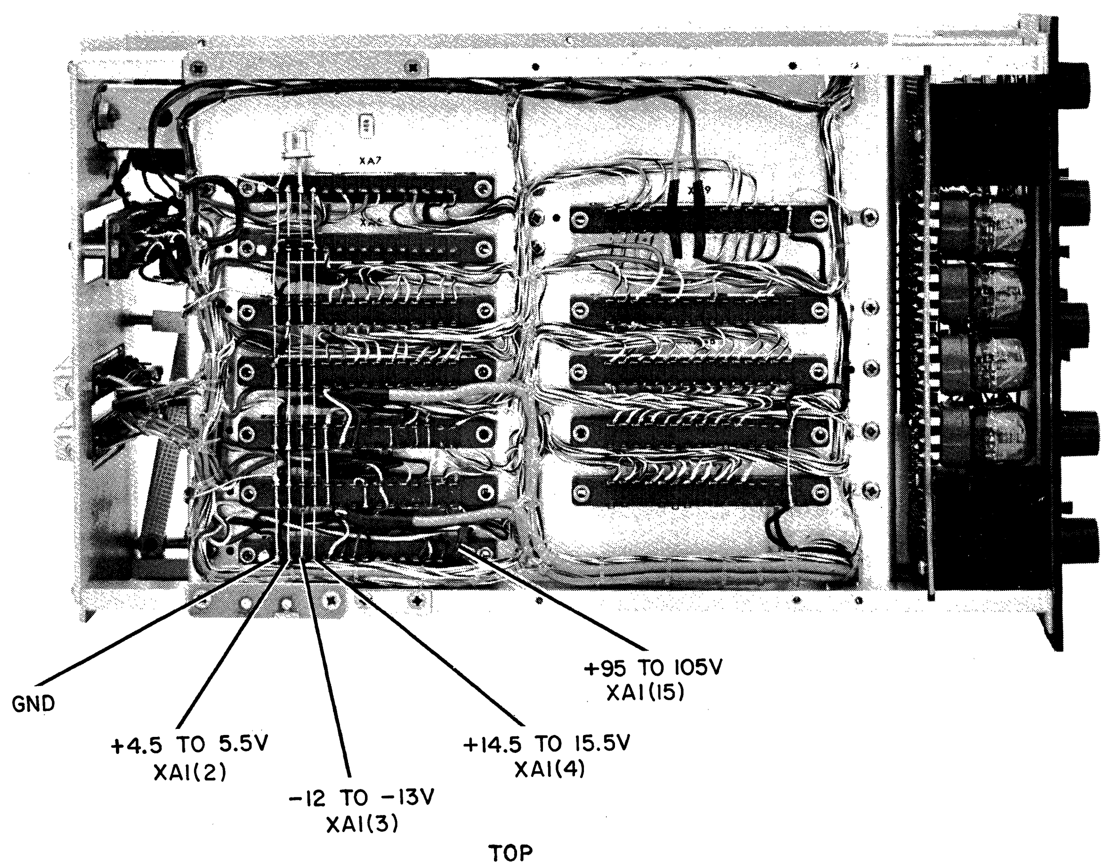
3.3.1.3 REFERENCE VOLTAGE ADJUSTMENT

a. Connect Digital Voltmeter (DVM) positive lead to XA6(5,E).

b. Voltage between XA6(5,E) and ground must be +9.9950V to +10.0050V.

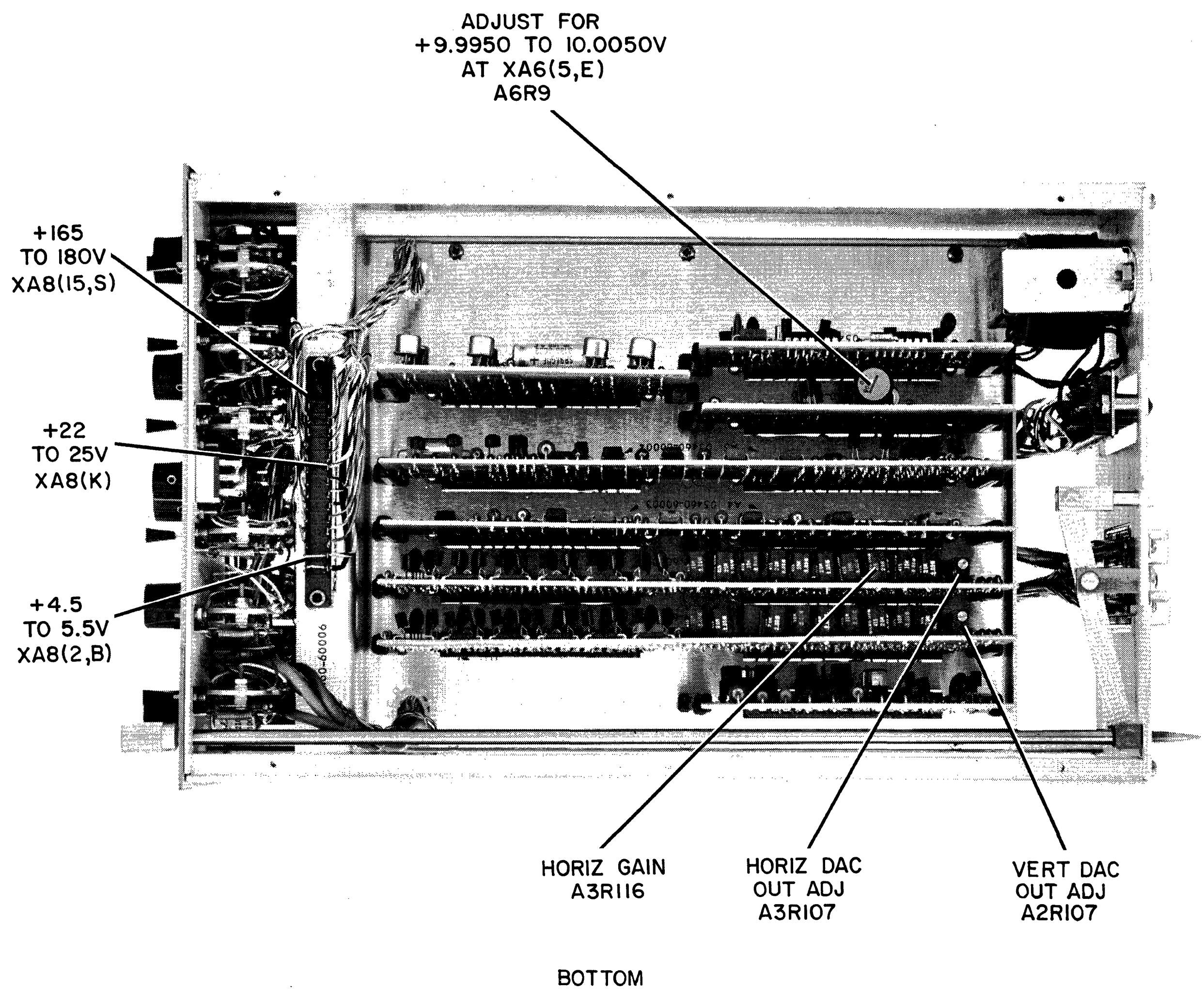
c. Adjust A6R9, if necessary, to bring voltage within specified range. See *Figure 3-2b* for test points.

Figure 3-2b. Display Unit Test Points (Continued)



please continue on next page

Figure 3-2c. Display Unit Test Points (Continued)



3.3.1.4 HORIZONTAL DAC OUTPUT VOLTAGE ADJUSTMENT

a. Connect DVM positive lead to oscilloscope rear-panel "X" output connector center conductor.

b. Set 5460A DISPLAY CALIBRATE to +FS.

c. Set 5460A DISPLAY FUNCTION to CAL.

d. DVM should read +2.5025V to +2.5050V.

e. If DVM reading is not correct, adjust 5460A A3R107 as required.

3.3.1.5 HORIZONTAL CRT GAIN ADJUSTMENT

a. Set 5460A DISPLAY CALIBRATE to ORIGIN, DISPLAY FUNCTION to CAL.

b. Adjust oscilloscope HORIZONTAL POSITION for dot on vertical line at left-hand edge of graticule.

please continue on next page

3.3.1.5 HORIZONTAL CRT GAIN ADJUSTMENT *(Continued)*

c. Set 5460A DISPLAY CALIBRATE to +FS.

d. Adjust 5460A A3R116 to place dot on center vertical line of graticule.

e. Repeat steps a. through d. above until A3R116 requires no further adjustment.

3.3.1.6 VERTICAL DAC OUTPUT VOLTAGE ADJUSTMENT

a. Connect DVM positive lead to oscilloscope rear-panel "Y" output connector center conductor.

b. Set 5460A DISPLAY FUNCTION to CAL.

c. Set 5460A DISPLAY CALIBRATE to +FS.

d. Connect 5460A XA2A(12) to chassis.

e. DVM must indicate +4.0060V to +4.0100V.

f. If DVM reading is not within specification, adjust 5460A A2R107.

g. Remove clip lead from XA2(12).

3.3.1.7 VERTICAL CRT GAIN CALIBRATION

a. Set 5460A DISPLAY CALIBRATE switch to ORIGIN and DISPLAY FUNCTION to CAL.

b. Adjust 5460A VERTICAL POSITION to center dot on vertical line at left-hand edge of CRT graticule.

c. Set 5460A DISPLAY CALIBRATE switch to +FS.

d. Adjust 5460A VERTICAL CAL (front panel) to position dot on upper horizontal line of CRT graticule.

e. Set 5460A DISPLAY CALIBRATE to -FS. Dot should appear on lower horizontal line of CRT graticule.

3.3.2 ADC Adjustments

Before adjusting any part of your 5466A, be very sure that adjustment is needed, and that you understand how to make the adjustment. Be sure the 5475A power supply adjustments have been completed before attempting adjustment of the ADC.

The adjustment procedures require that the 5466A plug-in be removed from the 5475A Control unit, and that its right-hand side cover be removed. The 5466A is assumed to be connected to the 5475A through the HP 10628A Service Extender Cable. Refer to Section I of this manual for detailed access information.

3.3.2.1 EQUIPMENT REQUIRED

The following equipment, or its equivalent, is required to perform these procedures:

HP Model 3470A Digital Voltmeter
HP Model 1707A Oscilloscope
HP Model 5300/5301 Electronic Counter

please continue on next page

3.3.2.1 EQUIPMENT REQUIRED

HP Model 3310B Function Generator
HP Model 6115A Precision Power Supply
HP Model 10628A Service Extender Cable

NOTE

These adjustments require use of the ADC Test Program. Enter the program by loading the System Diagnostic Tape as described in Subsection 3.2.2, and typing SA, (CR) , (LF) .

3.3.2.2 A1 (and A2) INPUT ASSEMBLY ADJUSTMENTS (05466-60001)

NOTE
Do 3.3.3.2 Power Supply Adjustments before proceeding.

3.3.2.2.1 Channel A DC Offset

a. Connect test lead from Digital Voltmeter to A1 Test Point A2 ("TP A2") (see *Figure 3-3*).

b. Connect a 50-ohm termination BNC to the Channel A INPUT. Set the Channel A OVERLOAD VOLTAGE switch to ".125".

c. DC offset, measure d with DVM connected at Test Point A2, should be less than ±1.5 mV for all Channel A OVERLOAD VOLTAGE switch settings from ".125" to "1", and less than ±5 mV for "2", "4", and "8". If all values are correct, go to 3.3.2.2.2; otherwise do "d" through "n" below.

d. Disconnect DVM from TP A2, and connect DVM to TP A1.

e. Adjust R12 (next to Test Point A1) for a DVM reading of 0.0 ± 10 mV.

f. Set the Channel A OVERLOAD VOLTAGE switch to "8".

g. Disconnect DVM from TP A1 and connect DVM to TP A2.

h. Adjust R18 (next to Test Point A2) for a DVM reading of 0.0 ± 5 mV.

i. Set Channel A OVERLOAD VOLTAGE to ".125".

j. Disconnect DVM from TP A2, and connect DVM to TP A1.

k. Adjust R12 for DVM reading of 0.0 ± 5 mV.

l. Disconnect DVM from TP A1 and connect DVM to TP A2.

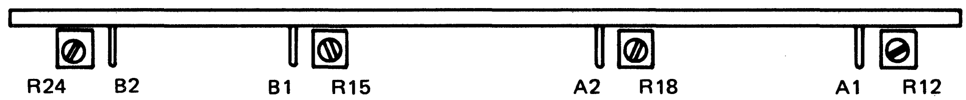
m. Adjust R18 for reading of 0.0 ± 1.5 mV.

n. Repeat step c.

This ends the Channel A Amplifier DC Offset Adjustments.

please continue on next page

Figure 3-3. A1 (and A2) ADC Input Assembly Adjustments



3.3.2.2.2 Channel B DC Offset

a. Connect test lead from Digital Voltmeter to A1 Test Point B2 ("TP B2").

b. Connect a 50-ohm termination BNC to the Channel B INPUT. Set the Channel B OVERLOAD VOLTAGE switch to ".125".

c. DC offset, measured with DVM connected at Test Point B2, should be less than ±1.5 mV for all Channel B OVERLOAD VOLTAGE switch settings from ".125" to "1", and less than ± 5 mV for "2", "4", and "8".

If all values are correct, and:

1) Yours is a 2-channel ADC: Go to 3.3.2.3.

2) Yours is a 4-channel ADC:

a) Repeat 3.3.2.2.1 on 5466A Board Assembly A2 for Channel C.
b) Perform this procedure on 5466A Board Assembly A2 for Channel D, then go to 3.3.2.3.

Otherwise, perform steps "d" through "n".

d. Disconnect the DVM from TP B2 and connect the DVM to TP B1.

e. Adjust R15 (next to TP B1) for a DC offset of 0.0 ±10 mV.

f. Set the Channel B OVERLOAD VOLTAGE switch to "8".

g. Disconnect the DVM from TP B1 and connect the DVM to TP B2.

h. Adjust R24 (next to Test Point B2) for a DVM reading of 0.0 ± 5 mV.

please continue on next page

3.3.2.2.2 Channel B DC Offset *(Continued)*

i. Set Channel B OVERLOAD VOLTAGE to ".125".

j. Disconnect the DVM from TP B2 and connect the DVM to TP B1.

k. Adjust R15 for DVM reading of 0.0 ± 5 mV.

l. Disconnect the DVM from TP B1 and connect the DVM to TP B2.

m. Adjust R18 for a reading of 0.0 ± 1 mV.

n. Repeat step "c".

This ends the Channel B DC Offset Adjustments.

3.3.2.3 A3, A5 (and A4, A6) DIGITIZER ADJUSTMENTS AND CALIBRATION

3.3.2.3.1 Sample-and-hold Module DC Offset Adjustment

a. Set all OVERLOAD VOLTAGE switches to ".125".

b. Connect the 50-ohm termination to the 5466A's Channel A INPUT.

c. Connect the test lead from the Digital Voltmeter to test point A2 on the A1 board. DVM should read the DC offset voltage, 0.0 ± 1.5 mV; if not, perform step 3.3.2.2.1 of this adjustment procedure.

d. Connect the DVM test lead to A3 test point "S AND H" (for "Sample and Hold"). (See *Figure 3-4.*)

e. Adjust A3R1 for a DVM reading of 0.0 ± 1.5 mV.

f. Perform steps "a" through "e" above for 5466A Board Assembly A5 (and A4 and A6, if installed).

NOTE

In step "c" above, use A1 test point B2 for Channel B, A2 test point A2 for Channel C, A2 test point B2 for Channel D.

In step "d" above, use A5 for Channel B, A4 for Channel C, A6 for Channel D.

3.3.2.3.2 Digitizer Module DC Offset Adjustment

a. Load the 5451A System Diagnostic Tape (HP Part Number 05451-90021), using the Basic Binary Loader (see Appendix A and procedure 3.2.2 for configuring the system diagnostic).

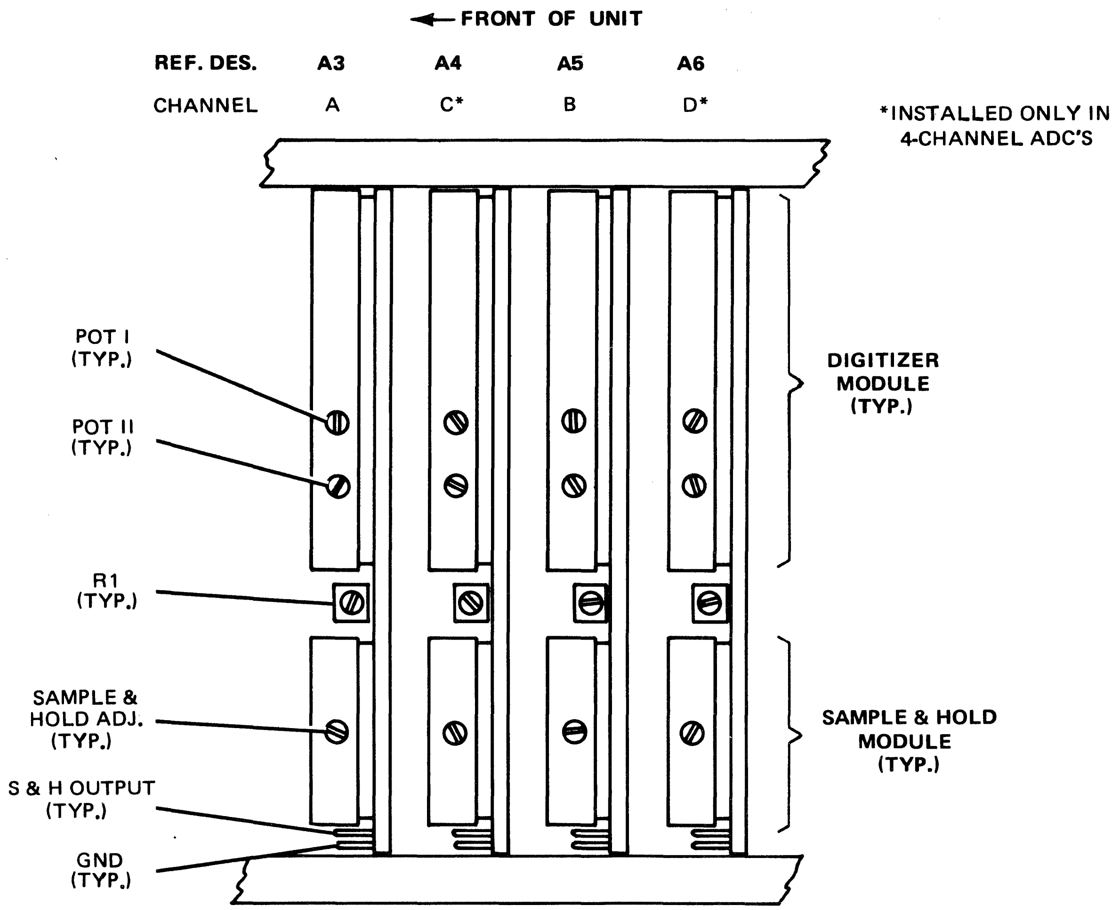
b. Type QA, (CR) , (LF) , on the Teleprinter, to enter the "Query ADC" routine.

c. Set ADC controls as follows:
SAMPLE MODE: INT, kHz
TRIGGER SOURCE: FREE RUN
OVERLOAD VOLTAGE (all): 8
DISPLAY/INPUT (2-channel): A/A
DISPLAY (4-channel): A

d. Connect 50-ohm load to Channel A INPUT.

please continue on next page

Figure 3-4. A3, A5 (and A4, A6) ADC Digitizer Adjustments (For 10-bit or 12-bit Digitizers)



3.3.2.3.2 Digitizer Module DC Offset Adjustment *(Continued)*

e. Set Computer's switch register bit "10" to "1". For a 12-bit ADC, also set bit "15" to "1".

f. Adjust A3's "POT I" (see *Figure 3-4*) for a reading of "000" ± "2" on the 5460A Display Unit's digital indicator tubes.

g. Remove the 50-ohm termination.

3.3.2.3.3 Digitizer Gain Calibration

NOTE

The DC Offset procedure above (subsection 3.3.2.3.2) should be performed for the Digitizer Board assembly before you perform this calibration procedure.

a. Set the HP 6115A Precision Power Supply for 7.0000V output.

b. Connect the 6115A's output to the 5466A's Channel A INPUT.

please continue on next page

3.3.2.3.3 Digitizer Gain Calibration *(Continued)*

c. Adjust A3's "POT II" for the correct 5460A indication, as given below for your digitizer.

   10-bit: "448" ± "2"
   12-bit: "1790" ± "2"

d. Check ADC Channel linearity by setting the 6115A's output level as indicated in *Table 3-14*, and checking the 5460A display for that voltage. The table includes a place for you to record the actual values you observe.

This completes the Digitizer Board Assembly adjustments for Channel A (Board Assembly A3). Perform the procedures of subsections 3.3.2.3.2 and 3.3.2.3.3 above for Channel B (Board Assembly A5) and, if yours is a four-channel ADC, for Channel C (Board Assembly A4) and Channel D (Board Assembly A6). For a two-channel plug-in, be sure to set the DISPLAY/INPUT switch to "B/AB" when you check Channel B. For a four-channel plug-in, set the INPUT switch to "ABCD", and the DISPLAY switch to "B", "C", or "D", corresponding to the channel you are adjusting.

Table 3-14. ADC Channel Linearity Check

CHANNEL INPUT VOLTAGE (VOLTS) (740A/B Output)	5460A Display					
	Specification (See Note)		Actual			
	10-bit	12-bit	Channel A	Channel B	Channel C	Channel D
0.0	000 ± 2	000 ± 4	________	________	________	________
1.0	064 ± 2	256 ± 4	________	________	________	________
2.0	128 ± 2	512 ± 4	________	________	________	________
3.0	192 ± 2	768 ± 4	________	________	________	________
4.0	256 ± 2	1024 ± 4	________	________	________	________
5.0	320 ± 2	1280 ± 4	________	________	________	________
6.0	384 ± 2	1536 ± 4	________	________	________	________
7.0	448 ± 2	1790 ± 4	________	________	________	________

NOTE:

In addition to the "Specifications" given above, the following linearity "spec" also applies:

For any one-volt *change* in INPUT signal level for any channel, the *change* in output (indicated on the 5460A Display Unit's tubes) must be:

   64 ± 1, for a 10-bit digitizer
   256 ± 2, for a 12-bit digitizer

please continue on next page

3.3.2.4 Oscillator Adjustment

a. Connect the Counter's AC Input to the Test point labelled "20 MHz". (See *Figure 3-5.*)

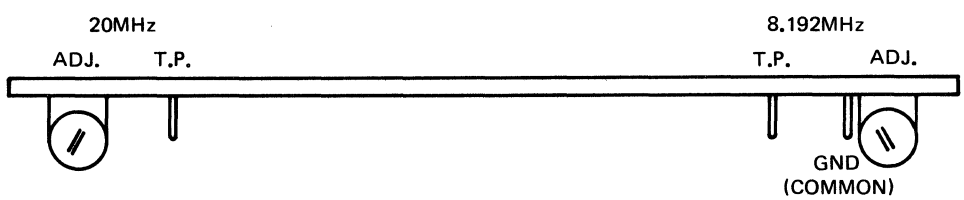
b. Set a one-second GATE time FREQUENCY measurement.

c. Adjust the capacitor next to the test point for a Counter reading of 20.000000 MHz ± .000050 MHz.

d. Connect the Counter's AC Input to the Test Point labelled "8.192 MHz".

e. Adjust the capacitor next to this test point for a reading of 8.192000 MHz ± .000020 MHz.

Figure 3-5. A10 ADC Sample Generator (05466-60006) Adjustments



3.3.3 Control Unit Adjustments

3.3.3.1 EQUIPMENT REQUIRED

The following equipment or equivalent is required to perform these procedures:

HP Model 412 DC Vacuum Tube Voltmeter
HP Model 3460B Digital Voltmeter (6-digit readout)
HP 5211A/B Counter
Short Clip Lead

3.3.3.2 POWER SUPPLY ADJUSTMENTS

The Model 5475A power supplies should not normally require adjustment. However, the replacement of a malfunctioning component or long-term component aging may cause the Model 5475A to become out-of-adjustment. All power supply adjustments are on the regulator board assemblies.

The dc output voltages from the power supply regulator board assemblies are independent of each other. Therefore, when you are adjusting any one supply, it is not necessary that you check or adjust any other supply.

please continue on next page

3.3.3.2 POWER SUPPLY ADJUSTMENTS *(Continued)*

When adjusting any supply, you must make the voltage adjustment before you make the overcurrent adjustment.

If you are adjusting more than one supply, you can make all voltage adjustments first, then go back and make all overcurrent adjustments.

NOTE

While performing adjustments, the regulator board assemblies must be seated in their respective connectors and not on an extender board assembly. Stray inductance can induce oscillations when the board assembly is extended.

3.3.3.2.1 Preliminary Instructions

The preliminary instructions are to be performed prior to any adjustments.

a. Remove 5466A plug-in from 5475A mainframe.

b. Adjust overcurrent control potentiometers associated with power supplies being adjusted to center of their travel (see *Figure 3-6*).

NOTE

The following list provides a quick-reference to locations of overcurrent control and voltage control potentiometers (see *Figure 3-6*).

1. **Overcurrent control adjustments:**
   Negative: Extreme left of board, extreme rear of instrument.
   Positive: Extreme right of board, extreme front of power supply section.

2. **Voltage adjustments:**
   Negative: Second from left on board, second from rear of instrument.
   Positive: Third from left on board, third from rear of instrument.

3. **Assemblies**
   + and -24V: A3A4
   + and -12V: A3A5
   + and -5V: A3A6

c. Connect load resistors listed below between designated pin on rear-panel connector J17 and chassis ground for the dc output voltages to be adjusted.

CAUTION

Do not exceed 120W total load capability of instrument. If possible, perform adjustment procedure with only part of the loads connected, then repeat this step for remaining dc voltages.

NOTE

Both pins should be used in parallel to check voltages.

+24V - 12Ω 50W between J17(14,32) and ground*
-24V - 12Ω 50W between J17(9,27) and ground*
+12V - 3Ω 50W between J17(16,34) and ground*
-12V - 3Ω 50W between J17(7,25) and ground*
+5V -1.2Ω 25W between J17(18,36) and ground*
-5V - 1.2Ω 25W between J17(5,23) and ground*
*ground connections are J17(1,2,19,20)

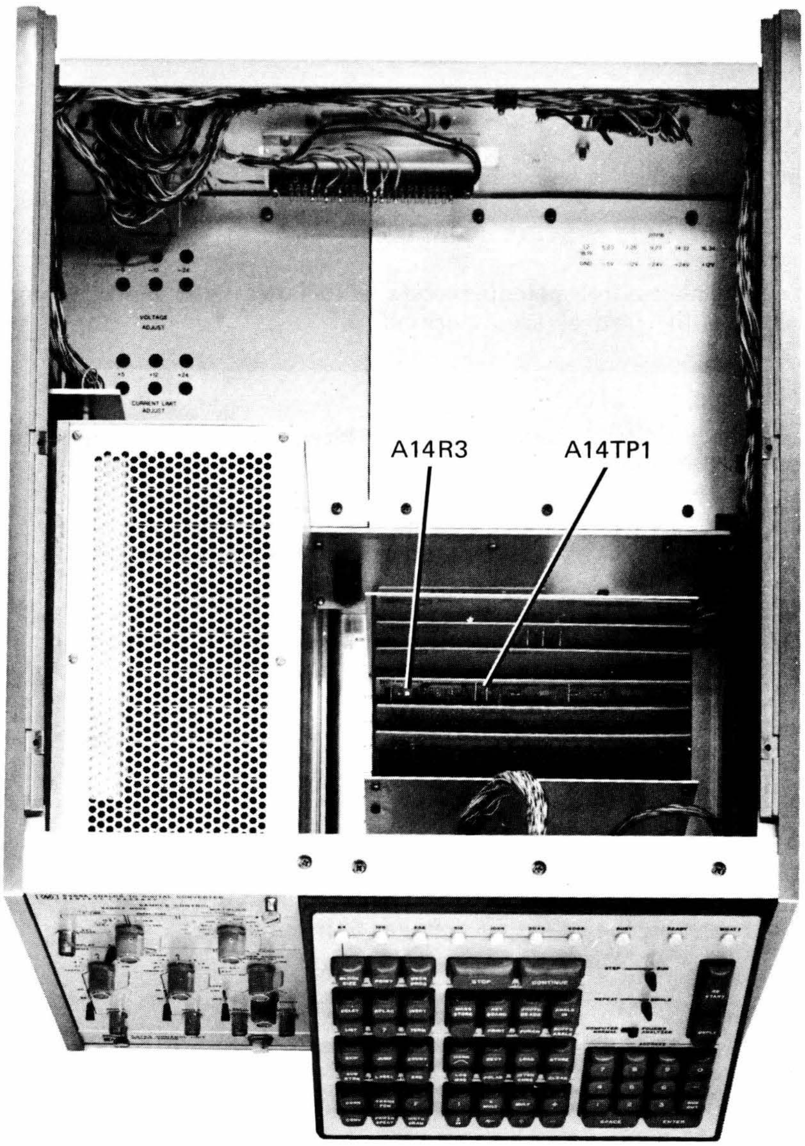
please continue on next page

3.3.3.2.1 Preliminary Instructions *(Continued)*

d. Connect Digital Voltmeter (DVM) across load resistor of first dc output voltage to be adjusted.

e. Turn on cabinet power and 5475A power.

Figure 3-6. Control Unit Test Points



please continue on next page

3.3.3.2.2 Voltage Adjustments

To adjust any of the dc output voltages, perform the following procedures for the associated supply:

a. Perform preliminary instructions listed in the preceding paragraph.

b. Adjust associated voltage potentiometer for nearest value displayed on DVM to designated magnitude. Value displayed shall be within ±0.5 percent of designated magnitude.

c. Repeat step b. for each additional dc output voltage to be adjusted, ensuring associated load resistor is connected and DVM is across the resistor.

d. Disconnect all test equipment.

3.3.3.2.3 Overcurrent Control Adjustment

To establish the point at which overcurrent from a supply is sensed, perform the following procedure:

a. Ensure voltage adjustment for the supply has been performed as described in the preceding paragraph.

b. Apply one of the following fixed load resistors, or a variable load resistor with an ammeter to produce given current condition between designated pin and chassis ground for first supply to be adjusted.

+24V - 10.1Ω 50W for 2.36 amps between J17(14,32) and ground*
-24V - 10.1Ω 50W for 2.36 amps between J17(9,27) and ground*
+12V - 2.5Ω 50W for 4.72 amps between J17(16,34) and ground*
-12V - 2.5Ω 50W for 4.72 amps between J17(7,25) and ground*
+5V - 1.0Ω 25W for 5.0 amps between J17(18,36) and ground*
-5V - 1.0Ω 25W for 5.0 amps between J17(5,23) and ground*

*ground is J17(1, 2, 19, 20)

c. Adjust associated overcurrent control potentiometer until 5475A rear-panel OVERLOAD indicator lights.

d. Disconnect load resistor presently connected.

e. Repeat steps a. through d. for each additional power supply that is to have the overcurrent control adjusted.

3.3.3.3 OSCILLATOR ADJUSTMENT

This procedure synchronizes the shift register clock rate with the clock rate of the teleprinter and the teletype I/O card in the computer. The oscillator is located on the shift register board A14 (05475-60038).

a. Connect Model 5300A/5303A Counter leads between A14 test pins TP1 and TP4 (ground). See *Figure 3-6*. (Connect 1 kΩ resistor in series with TP1 counter lead to reduce cable capacitance effect on oscillator frequency.)

b. Adjust A14R3 potentiometer (*Figure 3-6*) so period of signal at TP1 is 9.09 ± 0.04 msec (ambient temperature between 20-25°C).

end

SECTION IV

TROUBLESHOOTING

4.1 INTRODUCTION

This section provides system troubleshooting procedures for outline to the circuit card level in the 5460A Display Unit, 5466A ADC or 5475A Control Unit (see *Table 4-1*). This procedure determines as quickly as possible whether the trouble lies in the system hardware or the computer. Computer malfunction isolation, including all software and peripherals, is contained in separate manuals. Refer to the System Configuration Notice for a list of equipment and manuals supplied with your Fourier Analyzer System.

Table 4-1. System Troubleshooting Procedures

Title	Paragraph
NOTE *Read Troubleshooting Assumptions, paragraph 4.4 before using any troubleshooting procedures.*	
1. General Malfunction Indications Troubleshooting	4.5
2. Power Turn-On Troubleshooting	4.6
3. System Test Tape Loading Troubleshooting	4.7
4. Control Unit Troubleshooting a. Preliminary Keyboard Test b. QK Subroutine Test c. SK Subroutine Test	4.8
5. Display Unit Troubleshooting a. SD Subroutine Test b. QD Subroutine Test	4.9
6. ADC Troubleshooting a. SA Subroutine Test 1) Triggering Test 2) UNCAL Test b. QA Subroutine Test 1) Attenuator Code Test 2) Calibration Test c. Sample Rate Test d. External Clock Test e. Dual Input Subtract Test f. Histogram Test	4.10

4.2 TEST EQUIPMENT REQUIRED

Table 1-3 provides a list of equipment required to troubleshoot the Fourier Analyzer System.

please continue on next page

4.3 PREVENTIVE MAINTENANCE

No preventive maintenance is required for the ADC, for the Control Unit, and Display Unit. Clean and lubricate the keyboard switches and contacts using recommended cleaner (8500-1109) and lubricant (6040-0288). Recommended time interval during normal use is every six months. Refer to applicable manuals for preventive maintenance for the computer, teleprinter, and other peripherals.

4.4 TROUBLESHOOTING ASSUMPTIONS

The troubleshooting procedures make the following assumptions:

a. That, with the exception of general malfunction indications (e.g., teleprinter clatters when turned on, no CRT beam even with BEAM FIND depressed), the system test tape and operational check is used as a basis for the troubleshooting procedures. If it is obvious that the computer or a related peripheral is malfunctioning, refer to the applicable manual. The system test tape is configured to allow specific subroutines to be utilized as required. Always perform at least the unit operational check after repairing any unit.

b. That all system controls have been double checked to verify that they are in the proper positions. Also, that all cabling is correctly and firmly connected and that all computer interface cards are in the assigned I/O slots. The System Configuration Notice contains a record of the I/O slots for all of the computer peripherals.

c. That interconnect wiring will be checked and cabling replaced or repaired as required if the directed troubleshooting does not correct malfunction.

d. That all computer bit indicators are functioning. If any doubt exists, load the entire register to verify that indicators are functioning correctly.

e. That power is removed prior to replacing any units or circuit cards.

4.5 GENERAL MALFUNCTION INDICATIONS TROUBLESHOOTING

Table 4-2 provides troubleshooting for malfunctions that can be identified without being in the operational check. Where possible, the corrective action is given without going through the entire operational check. This list is not intended to cover all possible malfunctions.

4.6 POWER TURN-ON TROUBLESHOOTING

If the Fourier Analyzer System is rack-mounted, check continuity of rack wiring before individual units.

If power cannot be applied to the oscilloscope, refer to the oscilloscope manual.

If power cannot be applied to the Control Unit, refer to *Figure 2-9*. If the OVERLOAD lamp on the back of the Control Unit is lit, see *Table 4-2*.

4.7 SYSTEM TEST TAPE LOADING TROUBLESHOOTING

If the system test tape will not load, check the procedure in Appendix A. If the tape will still not load, check the basic binary loader (see Appendix B) and reload it if necessary. Refer to the System Operating Manual if the bootstrap tape is to be used.

please continue on next page

4.8 CONTROL UNIT TROUBLESHOOTING

These troubleshooting procedures are to be used if the Fourier Analyzer fails a portion of the Control Unit test in the operational check or if the Control Unit has performed correctly during the operational check but the keys fail to give correct operation in the Fourier Analyzer mode. Refer to one of the following tables for specific troubleshooting:

a. *Table 4-3*. Preliminary Keyboard Test Troubleshooting

b. *Table 4-4*. QK Subroutine Test Troubleshooting.

c. *Table 4-5*. SK Subroutine Test Troubleshooting.

4.9 DISPLAY UNIT TROUBLESHOOTING

These troubleshooting procedures are to be used only if the Fourier Analyzer fails a portion of the Display Unit test in the Operational check. If the Display Unit has performed correctly during the operational check but the plotter does not function properly or the display is jittery, refer to the general malfunction indications troubleshooting (*Table 4-2*). Refer to one of the following tables for specific troubleshooting:

a. *Table 4-6*. SD Subroutine Test Troubleshooting.

b. *Table 4-7*. QD Subroutine Test Troubleshooting.

4.10 ADC TROUBLESHOOTING

These troubleshooting procedures are to be used only if the Fourier Analyzer fails a portion of the ADC test in the operational checks.

Refer to one of the following tables for specific troubleshooting.

a. *Table 4-8*. SA Subroutine Test Troubleshooting

b. *Table 4-9*. QA Subroutine Test Troubleshooting

c. *Table 4-10*. QM Subroutine Test Troubleshooting

d. *Table 4-11*. SM Subroutine Test Troubleshooting

4.11 POWER-ON TEST TROUBLESHOOTING

If the system fails to return to the RUN mode, troubleshoot the computer. Refer to computer manuals.

Table 4-2. General Malfunction Indications Troubleshooting

Problem	Action
a. Can't get any input through the ADC.	a. 1. Check fuses on A1 (and/or A2) board(s) a) Turn off system power. b) Remove ADC from Control Unit. c) Remove ADC right-hand side cover. d) Remove A1 (and/or A2) board. e) Exchange "bad" fuse with spare fuse on board. 2. Check to see if proper voltages are being supplied to the ADC from the 5475A. See subsection 3.3.3.2. 3. Check ADC's front-panel controls. a) If TRIGGER MODE switch is in INT or EXT, is there actually a trigger signal? b) Are the sample rate switches on a calibrated range? c) If external samples are being generated, are they within the EXT. sample specifications? 4. Check to see that 5451A system tape is "ok". (Best method is to reload the tape) 5. Replace the following 5466A boards, in the order indicated, one at a time: a) A10, b) A9, c) A8, d) A3 — If ADC will not input, or inputs wrong data. e) A1 and/or A2, f) A4 through A6, g) A7 — If ADC inputs wrong data.
b. When turned on, the teleprinter clatters all the time.	b. 1. Verify cables are properly installed (see *Figure 1-2*). 2. Replace A14.
c. No action when RESTART is pressed.	c. 1. Replace keyboard microcircuit I/O card in computer. 2. Check computer, refer to computer manuals.
d. Control Unit keyboard does not perform correctly.	d. Refer to preliminary keyboard test troubleshooting for this problem.
e. No CRT display even with BEAM FIND pressed.	e. Refer to oscilloscope manual.

table continues on next page

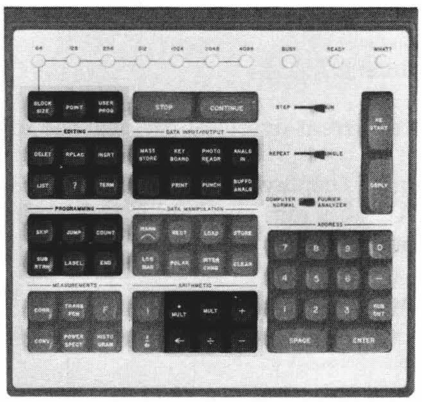
Table 4-2. General Malfunction Indications Troubleshooting (Continued)

Problem	Action
f. Plotter malfunctions	f.
1. No seek pulse to plotter (after plotter completes one plot it starts over).	1. a. Replace A7. b. Replace A5. c. Check completed plot pulse from plotter. d. Check plotter cable.
2. Plotter works on internal plot rate but does not work on external.	2. a. Replace A7. b. Check plotter.
3. No internal plotter rate control.	3. Replace A7.
g. OVERLOAD light on REAR of the Control Unit lights (indicates a power supply is overloaded.	g. To locate current overload perform the following: 1. Remove Display Unit plug-in. If OVERLOAD goes out, overload is in plug-in. Isolate and repair defective circuit. 2. Remove ADC plug-in. If OVERLOAD goes out, overload is in plug-in. Isolate and repair defective circuit. 3. One at a time, remove all cables from Control Unit rear panel. If disconnecting any cable causes the OVERLOAD indicator to go out, the problem is in the circuit served by that cable. Reconnect the cable. With a voltmeter and the Control Unit power supply adjustment procedure locate the supply being overloaded. If trouble is in the Control Unit, replace regulator board. If external, isolate and repair defective circuit.
h. COMPUTER NORMAL/FOURIER ANALYZER switch does not allow normal operation of computer in COMPUTER NORMAL position.	1. Replace keyboard microcircuit I/O card. 2. Check computer, refer to computer manuals.
i. Jittery display.	i. Check power supply voltages and clean board and plug contacts.
j. When System is turned on, the Teleprinter prints ".WHAT" repeatedly.	j. 1. Check +5V fuse inside 5475A Control Unit. 2. Replace Keyboard Microcircuit Interface Card.

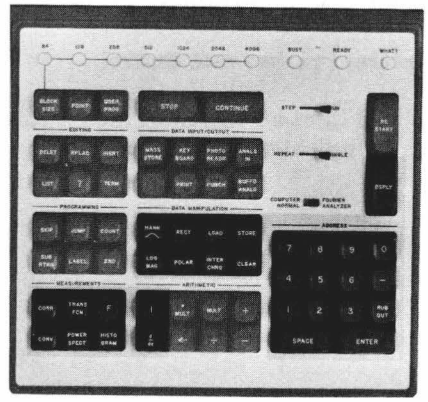
end of table

Table 4-3. Preliminary Keyboard Test Troubleshooting

Problem	Action
a. Teleprinter prints out with switch in COMPUTER NORMAL.	a. 1. Replace A14. 2. Replace A18.
b. Single teleprinter key is intermittent or locks out all other keys.	b. 1. Check switch (adjust, if necessary). 2. Check Wiring.



GROUP A



GROUP B

Problem	Action
c. No teleprinter output for either GROUP A or GROUP B switches.	c. 1. Check or replace A18. 2. Replace A14. 3. Replace TTY microcircuit I/O card in computer. 4. Check Teleprinter.
d. Wrong teleprinter output for GROUP A and GROUP B switches.	d. 1. Adjust A14 Oscillator (see Control Unit Adjustments). 2. Replace A14.
e. Wrong or no teleprinter output when a GROUP A switch is pressed. Teleprinter OK for GROUP B switches.	e. Replace A12.
f. Wrong or no teleprinter output when a GROUP B switch is pressed. Teleprinter OK for GROUP A switches.	f. Replace A13.
g. Correct letters print out when the keyboard buttons are pressed, but there is still a problem when returning to the main Fourier program (i.e., pushing a button does not perform the correct function), it is desirable to check the coding of the bits into the computer. In order to do this test, the test tape must be operating and the test subroutine entered by typing QK, (CR) , (LF) . Then press malfunctioning key. The octal code is displayed in the Display Register.	g. Observe octal code for ASCII character in Display Register (STOP, CONTINUE, & RESTART switches are uncoded and wired direct to A15).

table continues on next page

Table 4-3. Preliminary Keyboard Test Troubleshooting (Continued)

NOTE

Disregard bit 8 in binary count. That is, Block Size has a code of 102(3)23 but the computer may have 102(7)23.

Signal Name	Teleprint	ASCII Equivalent (Octal Code)
BLOCK SIZE	BS	102323
POINT	/.	057256
USER PROG	Y	131240
DELET	/D	057304
RPLAC	/R	057322
INSRT	/I	057311
LIST	/L	057314
?	?	077240
TERM	/	057240
SKIP	IF	111306
JUMP	J	112240
COUNT	#	043240
SUB RTRN	<	074240
LABEL	L	114240
END	.	056240
CORR	CR	103322
TRANS FLN	CH	103310
F	F	106240
CONV	CV	103326
POWER SPECT	SP	123320
HISTO GRAM	RH	122310
MASS STORE	MS	115323
KEY BOARD	K	113240
PHOTO READR	R	122240
ANALG IN	RA	122301
ANALG OUT (BLANK)	B	102240
PRINT	W	127240
PUNCH	P	120240
BUFFD ANALG	RB	120240
HANN Ω	H1	110261
RECT	TR	124322
LOAD	X<	130274
STORE	X>	130276
LOG MAG	TL	124314
POLAR	TP	124320
INTER CHNG	X	130240
CLEAR	CL	103314

table continues on next page

Table 4-3. Preliminary Keyboard Test Troubleshooting (Continued)

Signal Name	Teleprint	ASCII Equivalent (Octal Code)
*MULT	$	044240
MULT	*-	052255
+	*	052240
$\frac{d}{dx}$	A+	101253
	%	045240
←	←	137240
÷	:	072240
-	A-	101255
ENTER	(CR) (LF)	015212
SPACE		040000
DISPLAY	D	104240
RUBOUT	BELL	007377
1	1	061000
2	2	062000
3	3	063000
4	4	064000
5	5	065000
6	6	066000
7	7	067000
8	8	070000
9	9	071000
0	Ø	060000
-	-	055000

Problem	Action
h. Octal code as shown on computer register is incorrect but teleprinter had correct printout.	h. Adjust A14 Oscillator (see Control Unit Adjustments).
i. Octal code as shown on computer register is correct.	i. Troubleshoot computer, refer to computer manuals.

end of table

Table 4-4. QK Subroutine Test Troubleshooting

Problem	Action
a. Pressing STOP does not light READY or pressing CONTINUE does not light BUSY and the corresponding bit (15 or 13) is lit in the computer register.	a. 1. Replace A17. 2. Replace ADC microcircuit I/O card in computer. 3. Check indicator continuity.

table continues on next page

Table 4-4. QK Subroutine Test Troubleshooting (Continued)

Problem	Action
b. Pressing STOP does not light READY or pressing CONTINUE does not light BUSY and the corresponding bit (15 or 13) is not lit in the computer register.	b. 1. Replace A15. 2. Replace keyboard microcircuit I/O card in computer. 3. Check switch. 4. Check computer, refer to computer manuals.
c. STEP/RUN, REPEAT/SINGLE or any of the ADC switches called out in this test fail to light correct bits.	c. 1. Replace keyboard microcircuit I/O card in computer. 2. Check switch. 3. Check computer, refer to computer manuals.

Table 4-5. SK Subroutine Test Troubleshooting

Problem	Action
a. No action when RESTART is pressed.	a. Refer to general malfunction indication troubleshooting (*Table 4-2*).
b. A single indicator malfunctions.	b. 1. Check indicator. 2. Replace A17.
c. A group of indicators malfunction.	c. 1. Replace A17. 2. Replace ADC microcircuit I/O card in computer.

Table 4-6. SD Subroutine Test Troubleshooting

Problem	Action
1. a. Bit 15 remains on.	a. Replace A5. b. Replace display microcircuit I/O card in computer. c. Doublecheck switch settings.
2. LAMPS. Problem with one or more of the following 5460A lamps: POLAR, RECT, LOG, FREQ, 1, 2, 5, X10, dB.	
a. One or more of the lamps does not light.	a. Replace boards. 1. A8—lamps are mounted on this board. 2. A9—lamp drivers are on this board. 3. A4—T^2L driver lines are on this board. 4. Display microcircuit I/O card in computer.
b. None of the lamps light.	b. 1. Replace ±24V Regulator in 5475A Control Unit. 2. Check +24V line at A8(K).

Table 4-6. SD Subroutine Test Troubleshooting (Continued)

Problem	Action
3. READ-OUT TUBES. Problem with one or more Digital Display Tubes.	
a. No Digital Display Tube is lighted and no "—" sign displayed.	a. 1. Replace A9. 2. Check +170V line from A8(J) to A9(15,S). 3. Check 130V ac at A9(6,8).
b. All Digital Display Tubes function, but are dim.	b. Replace A9.
c. Any Digital Display Tube counts, but not in proper sequence (skips numbers or is dead for counts 0 through 9; or resets to 0 and recounts at the wrong time). Note: Normal operation includes blanking for 6 counts after "9", while the BCD counter counts back to "0".	c. Replace A8.
d. All Digital Display Tubes count, but sequence is bad.	d. 1. Replace A8. 2. Replace A4. 3. Replace display microcircuit I/O card in computer.
e. None of the tubes count.	e. 1. Replace A8. 2. Replace A4.
f. "—" Indicator does not light.	f. 1. Replace A9. 2. Replace A8. 3. Replace A4.
4. CRT Display problems:	
a. No sweep, but dot appears.	a. 1. Replace A3. 2. Replace A4. 3. Replace display microcircuit I/O card in computer. 4. Reload test tape. 5. Refer to Computer Service Manual for computer checkout procedure.
b. No sweep, but dot or vertical line appears at left side of screen.	b. Verify that DISPLAY switch on scope mainframe is in INT position.
c. No CRT sweep or vertical deflection, and no spot.	c. Press Beam FIND. 1. If dot appears, and computer register bit 15 is flashing, be sure 5460A FUNCTION switch is set to DISPLAY, not to PLOT.

table continues on next page

Table 4-6. SD Subroutine Test Troubleshooting (Continued)

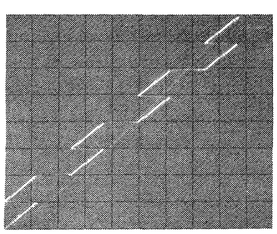
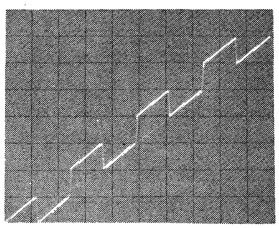
Problem	Action
	4.c. *Continued* 2. If dot appears, and computer register bit 15 is not flashing. a) Reload test tape. b) Replace display microcircuit I/O card in computer. c) Refer to computer checkout procedure computer service manual. 3. If dot does not appear. a) Replace A1. b) Check High Voltage to CRT—refer to oscilloscope manual.
d. Horizontal sweep, but VERTICAL GAIN, POSITION or CAL controls have no effect.	d. Replace A1.
e. Sweep nonlinear, either vertically or horizontally.	e. Interchange A2 and A3. 1. If problem changes. a) Replace A2 if problem is *now* Vertical nonlinearity. b) Replace A3 if problem is *now* Horizontal linearity. 2. If problem does not change. a) Replace A1 if problem is in Vertical deflection. b) Refer to oscilloscope manual if problem is in horizontal deflection.
f. If oscilloscope pattern resembles one shown below. HORIZONTAL PROBLEM 	f. Interchange A2 and A3. 1. If problem changes replace A2. 2. If problem doesn't change. a) Replace A4. b) Replace display microcircuit I/O card in computer. c) Check computer, refer to computer manuals.

table continues on next page

Table 4-6. SD Subroutine Test Troubleshooting (Continued)

Problem	**Action**
g. If oscilloscope pattern resembles one shown below: VERTICAL PROBLEM 	g. Interchange A2 and A3. 1. If pattern changes, replace A3. 2. If pattern doesn't change. a) Replace display microcircuit I/O card in computer. b) Check computer, refer to computer manuals.
h. Sweeps, but HORIZONTAL POSITION and X5, X10, MAGNIFICATION controls have no effect.	h. Refer to oscilloscope manual.
i. Display is Vertical line.	i. 1. Replace A4. 2. Replace A5. 3. Replace A3. 4. Refer to oscilloscope manual.
j. Display is only Horizontal line.	j. 1. Replace A1. 2. Replace A4. 3. Replace A5. 4. Replace A3. 5. Refer to oscilloscope manual.
k. Sweeps OK but problem with vertical bars.	k. Interchange A2, A3. If problem is corrected, replace the board NOW in A3. If problem is not corrected, replace A5.
5. SWITCH problems:	
a. HORIZONTAL MARKER switch causes no intensification of trace in either 8PT or 32PT position.	a. 1. Replace A5. 2. Replace A4. 3. Z-axis problem in oscilloscope mainframe, refer to oscilloscope manual.
b. HORIZONTAL MARKER switch causes intensificatin of trace only in 8 PT or 32 PT position, but not in both.	b. 1. Replace A5. 2. Check HORIZONTAL MARKER switch circuit for bad contacts or broken wires. 3. Check switch command lines A5(8) for $\overline{\text{HM32}}$ and A5(J) for HM8 signals.
c. DISPLAY TYPE "BAR" or "CONT" does not function.	c. 1. Replace A5. 2. Replace A2. 3. Check switch command lines A5A(14) for $\overline{\text{DTLNT}}$ and A5A(10) for $\overline{\text{DTPNT}}$ signals.
d. HORIZONTAL SWEEP LENGTH switch does not change sweep length.	d. 1. Be sure VERTICAL MODE switch is not in COMPLEX setting. 2. Replace A3. 3. Check switch command lines 12.8 (signal $\overline{\text{HS.8}}$) to A3A(6), 10 (signal $\overline{\text{HS10}}$) to A3A(F) and 10.24 (signal $\overline{\text{HS.24}}$) to A3A(H).

end of table

Table 4-7. QD Subroutine Test Troubleshooting

Problem	Action
a. Any Display Unit switch called out in this test that fails to light correct bits.	a. 1. Check switch wiring. 2. Reload test tape. 3. Possible problems with input portion of the display or with the computer.

Table 4-8. SA Subroutine Test Troubleshooting

Problem	Action
NOTE Set ADC controls as follows: SAMPLE MODE to kHz. MULTIPLIER to 2.5/5/200. TRIGGERING to FREE RUN	
a. TRIGGERING indicator lights when bit 15 is off.	a. 1. Replace A10, A9, A8. 2. Replace keyboard microcircuit I/O card in computer. 3. Check computer, refer to computer manuals.
b. TRIGGERING INDICATOR will not light in any position with bit 15 on.	b. 1. Check indicator. 2. Replace A8. 3. Replace A10. 4. Replace A9. 5. Check switch. 6. Replace ADC microcircuit I/O card in computer. 7. Check computer, refer to computer manuals.
c. TRIGGERING indicator will not light, in LINE position only.	c. 1. Replace A8. 2. Check Line plus signal from J15(43). 3. Check switch.
d. TRIGGERING indicator will not light, in INTERNAL (A) position only.	d. 1. Replace A8, A9. 2. Check TRIGGER SOURCE switch.
e. TRIGGERING indicator does not work in FREE RUN.	e. 1. Replace A8. 2. Replace A10. 3. Check TRIGGER SOURCE switch.
f. TRIGGERING indicator does not work, in EXTERNAL.	f. 1. Check EXTERNAL switch. 2. Replace A8.
g. UNCAL indicator does not light, in any position.	g. 1. Check indicator. 2. Replace A7.
h. UNCAL indicator does not light, in some positions.	h. 1. Replace A7. 2. Check SAMPLE MODE switch.
i. The frequency, or group of frequencies, are incorrect by a factor of 2, 10, etc.	i. 1. Check SAMPLE MODE switch codes in QK test. 2. Replace A10 Sample Generator board.

end of table

Table 4-9. QA Subroutine Test Troubleshooting

Problem	Action
a. ADC does not pass calibration check.	a. 1. Perform A1 (and/or A2) adjustments. 2. Perform A3, A5 (A4, A6) adjustments.
b. Wrong bit indications from OVERLOAD VOLTAGE attenuator switch(es).	b. 1. Check Switch(es) 2. Replace ADC microcircuit I/O card in Computer. 3. Check Computer, refer to Computer manuals. 4. Replace A1 (A2).
c. Check pulse did not appear, for one or more of the DISPLAY (or DISPLAY/INPUT) switch positions.	c. 1. Replace A7 board. 2. Check switch. 3. Check line plus signal from J15(43).
e. OVERLOAD VOLTAGE gain codes incorrect.	e. 1. Replace A7. 2. Replace A10. 3. Disconnect Remote Programming cable. 4. Check Switch. 5. Check Remote Programming and ADC I/O microcircuit (refer to appropriate manuals).
f. Incorrect codes for OVERLOAD VOLTAGE switch settings, for one or more DISPLAY/INPUT (or DISPLAY and INPUT) switch settings.	f. 1. Replace A7 board. 2. Disconnect Remote Programming cable. 3. Replace Remote Programming I/O microcircuit card.
g. ADC input gain test failed, for all input gain settings.	g. 1. Perform calibration procedure. 2. Check fuse on A1 (and/or A2) board. 3. Replace A1 (and/or A2) board. 4. Interchange A3, A5 (and/or A4, A6) Digitizer boards. If the fault is on the Digitizer, replace the Sample-and-Hold and/or Digitizer module as indicated. If the fault is on the data inverter and data buffers, plug "good" Sample-and-Hold and/or Digitizer module(s) from faulty board into replacement board.
h. Triangle wave input test failed.	h. 1. Interchange Digitizer boards (A3, A5, and/or A5, A6), as appropriate. 2. If the fault is on the Digitizer board, interchange Sample-and-Hold and/or Digitizer modules between "good" and "bad" boards. If fault indication is still present, load "good" Sample-and-Hold and/or Digitizer module(s) onto replacement board, and install board in the system.
i. ADC does not pass gain linearity part of adjustment and calibration procedure	i. 1. Replace A1 (or A2) Input board. 2. If the fault is on the Digitizer board, interchange Sample-and-Hold and/or Digitizer modules between "good" and "bad" boards. If fault indication is still present, load "good" Sample-and-Hold and/or Digitizer module(s) onto replacement board, and install board in the system.

table continues on next page

Table 4-9. QA Subroutine Test Troubleshooting (Continued)

Problem	Action
j. Does not pass EXTernal sample rate test.	j. 1. Check the INPUT signal for "noise" and overshoot. Be sure the levels are less than .3V and greater than 2V. 2. Replace A9 board. 3. Check Computer.
	end of table

Table 4-10. QM Subroutine Test Troubleshooting

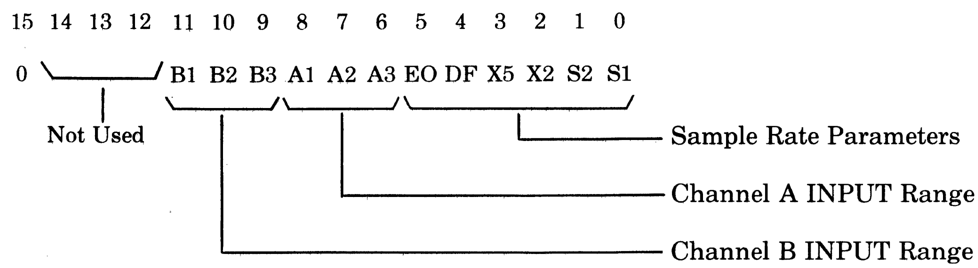
Problem	Action
Bit "2" does not light, or wrong bit pattern.	1. Confirm that proper cable is installed. (2-channel ADC uses 05451-60002; 4-channel ADC uses 05451-60004). Cable must have continuity between pin "C" and pin "3". 2. Check OVERLOAD VOLTAGE switches. 3. Replace ADC microcircuit I/O card in Computer. 4. Check Computer. Refer to Computer manuals.

Table 4-11. SM Subroutine Test Troubleshooting

Problem	Action
Computer HALTS during SM test.	1. Press the Computer's "S" button to see "SM" bit error. If bit "15" = "0", then bits "11" through "0" will indicate the signals which were in error. If bit "15" = "1", then bits "5" through "0" indicate signals associated with four-channel operation which were in error. Pressing RUN re-runs the program. Additional details are given below. 2. Confirm that proper cable is installed (2-channel ADC uses 05451-60005; 4-channel ADC uses 05451-60006). 3. Check OVERLOAD VOLTAGE switches. 4. Replace ADC microcircuit I/O card in Computer. 5. Check Computer. Refer to Computer manuals.
	table continues on next page

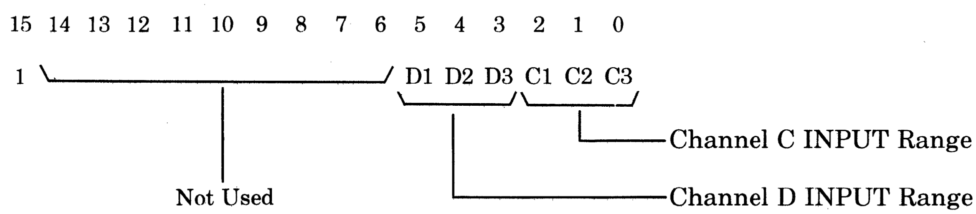
Table 4-11. SM Subroutine Test Troubleshooting (Continued)

Problem	Action
"SM" ERROR (BIT "15" "OFF")	



1. Check to be sure SAMPLE MODE switch is in its "REMOTE" position.
2. Check to see that all input range (OVERLOAD VOLTAGE) switches are in their "8" positions.
3. Replace Channel A and/or Channel B remote programming 12566 microcircuit interface card in Computer.
4. Check wiring.

"SM" ERROR (BIT "15" "ON")



1. Check to make sure SAMPLE MODE switch is in its "REMOTE" position.
2. Check to see that all input range (OVERLOAD VOLTAGE) switches are in their "8" positions.
3. Be sure 5466A four-channel capability exists, and is being used.

APPENDIX A

LOADING PAPER TAPE

This appendix contains the procedure for loading paper tape from the teleprinter tape reader and photoreader. *Table A-1* lists the procedure for loading tape from the teleprinter and *Table A-2* lists the procedure for loading tape from the photoreader. Refer to *Figure A-1* for inserting tape into the teleprinter and photoreader. Prior to performing the appropriate procedure, turn on all power to the computer, computer peripherals, and subsystems.

NOTE

If the DISPLAY REGISTER (step 8) does not contain 102077_8, the tape may have been loaded incorrectly and must be reloaded. A halt code of 102055 indicates an address error; check if tape is correct number or inserted backwards. A halt code of 102011 indicates a checksum error; check for bad tape or dirty reader. If the computer continues to halt with another number in the DISPLAY REGISTER, it is possible that the Basic Binary Loader program has been written over (erased). Refer to Appendix B for instructions on reloading the Basic Binary Loader.

TAPE PRINTOUT

To obtain a printout of any portion of the whole tape, perform steps of *Table A-1* except set the LINE-OFF-LOCAL switch in step 1 to LOCAL. The teleprinter will automatically print out the contents of the tape.

Figure A-1. Loading Paper Tape

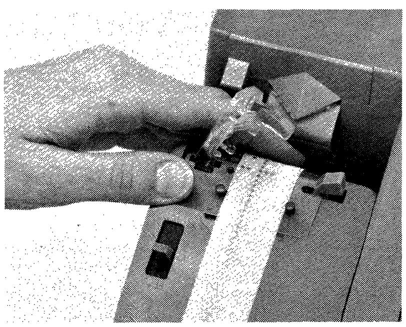
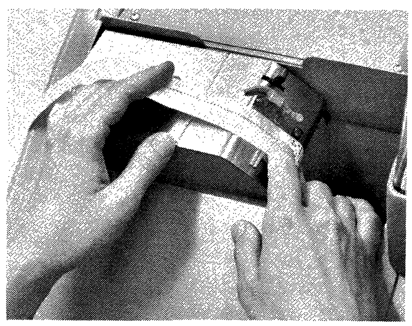
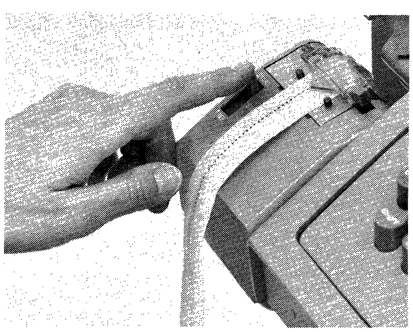
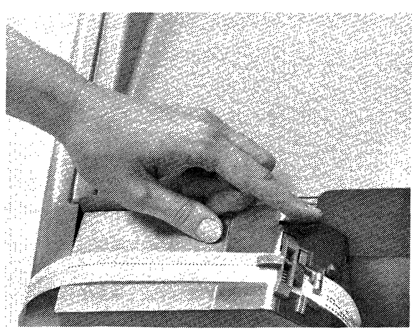
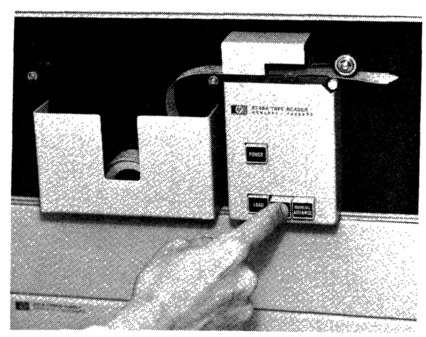
2752A	2754A	2748A
		
Load Tape into Reader	Load Tape into Reader	Load Tape into Reader
		
Set Reader Switch to START	Set Reader Switch to RUN	Press RUN

Table A-1. Teleprinter Tape Reader Load Procedure

Step	Unit	Operation	Remarks
1.	Teleprinter	Set LINE-OFF-LOCAL switch to LINE	Enables operation with computer
2.	Teleprinter	Load Tape per *Figure A-1* for 2752A or 2754A	
3.	Teleprinter	On 2752A, set switch to START. On 2754A, set switch to RUN.	Enables reader when commanded by computer.
4.	Computer	Set P (or M) register to 017700_8 (8K memory). Or 027700 (12K) or 037700 (16K) or 057700 (24K) or 077700 (32K).*	Octal code of starting address of basic binary loader.
5.	Computer	Press INTERNAL PRESET and EXTERNAL PRESET.	Sets Fetch phase and clears I/O channels.
6.	Computer	Press LOADER ENABLE.	Program register address entered in address register. Basic Binary Loader access enabled.
7.	Computer	Press RUN.	Computer accepts data from tape reader. Control of reader is maintained by computer. Tape takes about 30 min. to load average tape.
8.	Computer	HALT indicator lights and loader LOADER ENABLE darkens.	DISPLAY REGISTER shows 102077_8.
9.	Teleprinter	If teleprinter is not to be used, set set LINE-OFF-LOCAL switch to OFF.	Always turn off power to teleprinter when not in use to reduce mechanical wear.

*Press to light P button, press CLEAR DISPLAY button, enter starting address on DISPLAY REGISTER in octal code specified. (Press HALT button first if computer initially in RUN mode.)

Table A-2. Photoreader Load Procedure

Step	Unit	Operation	Remarks
1.	2748A	Press POWER switch to on.	Power applied to photoreader
2.	2748A	Press LOAD switch. Load paper tape into photoreader per *Figure A-1*, with the small feed holes nearest the panel. The first data frames must be to the left of the read element. The tape leader must pass under the hairpin on the read element and between the rollers on the right. Press READ switch.	
3.	2100A	Press HALT. Press P (or M) and enter starting address on DISPLAY REGISTER*	Octal code of starting address of basic binary loader
4.	2100A	Press INTERNAL PRESET and EXTERNAL PRESET.	Sets Fetch phase and clears I/O channels.
5.	2100A	Press LOADER ENABLE.	Program register address transferred to address register, access to Basic Binary Loader enabled.
6.		Press RUN.	Computer accepts data from tape reader. Control of reader is maintained by computer. Tape takes about 3 min. to load average tape.
7.		HALT indicator lights and LOADER ENABLE darkens.	DISPLAY REGISTER shows 102077_8.
8.	2748A	Press POWER switch to OFF.	
		*Octal code is 017700_8 for 8K memory; 027700 for 12K; 037700 for 16K; 057700 for 24K; 077700 for 32K.	

APPENDIX B

RELOADING THE BASIC BINARY LOADER

If the computer input device (2752A, 2754A Teleprinter tapereader or 2748A Photoreader) will not accept a program tape, or if incorrect HALT conditions are indicated by the DISPLAY REGISTER, it is possible that some or all of the loader program has been altered. Before assuming this is the case, check for dirt or other foreign material in the input device which may be causing incorrect operation. For systems using a disc loader or cassette loader, refer to applicable unit manual. To reload the loader program, proceed as follows:

Before reloading the loader, find out the channel number of the input device (teleprinter or photoreader) from the System Configuration Notice. The channel number is used when reloading the loader program.

NOTE

If your system contains a teleprinter and a photoreader, use the channel number of the photoreader when the channel number of the input device is called for in the loading procedure below.

To verify the Basic Binary Loader instructions in memory:

a. Press M button on computer front panel. Set the DISPLAY REGISTER to address of desired instruction. *Table B-1* illustrates the instructions and their addresses.
b. Press LOADER ENABLE to permit alteration of BBL contents.
c. Press MEMORY DATA. This displays the contents of address as listed in *Table B-1.*
d. Change the number displayed if necessary to agree with the corresponding number in *Table B-1.*
e. Press INCREMENT M. This displays the contents of the next consecutive memory locations.
f. Repeat steps d. and e. until satisfied that the program is correct.
g. Press LOADER ENABLE when all desired locations have been changed as necessary.

The M button can be pressed at any time to display the number of the current address, should you lose track. The DECREMENT M button can be used to reverse the BBL display. The CLEAR DISPLAY button can be used when preferable to enter a number from an all-zero display.

To reload the entire Basic Binary Loader using the bootstrap loader, refer to the System Operating Manual.

Table B-1. Instructions for Basic Binary Loader

Address	0	1	2	3	4	5	6	7
0m7700:	107700	063770	106501	004010	002400	006020	063771	073736
0m7710:	006401	067773	006006	027717	107700	102077	027700	017762
0m7720:	002003	027712	003104	073774	017762	017753	070001	073775
0m7730:	063775	043772	002040	027751	017753	044000	000000	002101
0m7740:	102000	037775	037774	027730	017753	054000	027711	102011
0m7750:	027700	102055	027700	000000	017762	001727	073776	017762
0m7760:	033776	127753	000000	1037cc	1023cc	027764	1025cc	027762
0m7770:	173775	153775	1n0100	177765	000000	000000	000000	000000

m = 1 for 8K memory
= 2 for 12K memory
= 3 for 16K memory
= 5 for 24K memory
= 7 for 32K memory

cc = channel number of punched tape reader

n = 6 for 8K memory
= 5 for 12K memory
= 4 for 16K memory
= 2 for 24K memory
= 0 for 32K memory

HEWLETT hp PACKARD

05451-90042

PRINTED IN USA