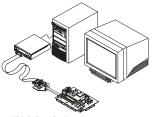


Emulation and Analysis Solutions for Motorola/IBM PowerPC 6XX Microprocessors

Product Overview



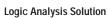
JTAG Emulation

- · Verify Interrupt Routines
- · Debug Assembly Code
- Optimize Code

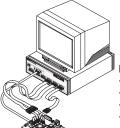
Emulation and Analysis Solutions for the Design Team







- Perform Basic Signal Measurements
- Profile Hardware Operation
- Verify Signal Integrity
- Verify Conformance to Specifications
- Exercise Microprocessor and Other Hardware
- Debug Boot Code



Emulation Solution with Real-Time Trace

- Debug Hardware/Software Interaction
- Profile Hardware/Software Interaction
- Optimize System Performance
- · Perform System Test

Quickly and accurately determine the root cause of your team's most difficult hardware, software, and system integration problems with Hewlett-Packard's powerful emulation and logic analysis solutions.

HP's emulation and analysis solutions for the Motorola/IBM PowerPC 6XX combine the powerful tools of run control, code download, debugger connections, and logic analysis for a complete, scalable system debug environment.

With a scalable solution from HP, design team members can customize HP's product offerings to meet their unique requirements. Solutions range from emulation probes combined with the industry's leading debuggers to emula-

Debug and Integrate Real-Time Embedded Systems

tion with real-time trace to solve today's most complex PowerPC 6XX design problems. HP's solutions are designed to meet your needs today and protect your investment as your needs change in the future.

With logic analysis providing timing and state analysis, you can monitor microprocessor activity in relation to other important system signals such as a PCI bus, other microprocessors, or I/O devices. Traditional emulation systems don't allow you to time-correlate events across your entire system using timing, analog, and state analysis for your most difficult integration problems.

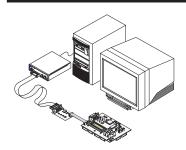
The logic analyzer is nonintrusive, allowing you to run your target system at full speed. A system trace, up to 2 M deep, can be combined with complex triggering to find the toughest problems. The microprocessor instruction set execution can be correlated to high-level source code with the HP source correlation tool set.

HP Scalable Solutions

HP emulation and logic analysis solutions are scalable for each member of the digital design team. The following are three typical configurations for firmware/software debug, hardware debug, and system integration.

Components of these solutions include a logic analyzer, emulation probe/module, analysis probe, inverse assembler, source correlation tool set, and optional system performance analysis tool set.

Information on each of these components is included in this document.



System Features

JTAG Emulation

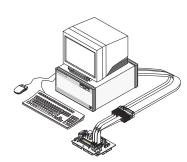
- Microprocessor run control on your target system
- · Debugger connection

System Components and Functionality

- Emulation Probe: (see p. 3)
 - Download code, view and modify memory, and view registers on your target system or evaluation board from the debugger interface
- Connect to industry-leading debuggers from Green Hills, Microtec, and SDS

Emulation Solution with Real-Time Trace

- Microprocessor run control on your target system
- Debugger connection
- Real-time logic analysis trace solution:
 - Assembly level trace
 - Source code trace
- QFP and PGA probing solutions
- HP 16600A or 16700A Series Logic Analysis System:
 - Capture and analyze code flow and data flow without halting the target system
 - Time-correlate analog, timing, and state events across your entire system
 - Monitor microprocessor activity in relation to system buses, other microprocessors, or I/O devices
- · Analysis Probe: (see p. 9)
 - Connect to PPC 603/603e target using 240 pin QFP probing solution
 - Connect to PPC 604/604e target using 289 pin PGA probing solution
 - Disassemble trace listing into PPC 6XX mnemonics
- Integrated Emulation Module: (see p. 3)
 - Download code, view and modify memory, and view registers on your target system or evaluation board from the debugger interface
 - Connect to industry-leading debuggers from Green Hills, Microtec, and SDS
- HP Source Correlation Tool Set: (see p. 11)
 - Time-correlate acquired logic analysis trace to highlevel source code
 - Step through in assembly or high-level code



Logic Analysis Solution

- Real-time logic analysis trace solution:
 Assembly level trace
- QFP and PGA probing solutions
- HP 16600A or 16700A Series Logic Analysis System:
 - Capture and analyze code flow and data flow without halting the target system
 - Time-correlate analog, timing, and state events across your entire system
 - Monitor microprocessor activity in relation to system buses, other microprocessors, or I/O devices
- Analysis Probe: (see p. 9)
 - Connect to PPC 603/603e target using 240 pin QFP probing solution
 - Connect to PPC 604/604e target using 289 pin PGA probing solution
 - Disassemble trace listing into PPC 6XX mnemonics

Microprocessor	Package Type	Microprocessor Clock Speed	JTAG Emulation	Emulation Solution with Real-Time Trace	Logic Analysis Solution
PPC 603	240-pin QFP	Up to 200 MHz	Х	Х	Х
PPC 603e	240-pin QFP	Up to 200 MHz	Х	Х	X
PPC 604	289-pin PGA	Up to 200 MHz	Х	Х	X
PPC 604e	289-pin PGA	Up to 200 MHz	Х	X	X

Table 1: Emulation and Analysis Solutions for Motorola/IBM PowerPC 6XX Microprocessors

Emulation Probe and Module

The emulation probe and module provide the same functionality. The emulation probe is a standalone product, as shown in figure 1. The emulation module is an integrated plug-in for the HP 16600A and 16700A Series logic analysis systems.

Both help you debug your code by providing run control, code download, and memory/register display and modification. You can control program execution through single stepping, start/stop, run/break, and set/modify breakpoints. You can also run code at full speed in the target.

The emulation probe can be controlled by an industry-leading debugger. The emulation module can either be controlled by an industry-leading debugger or the emulation control interface provided with the logic analyzer. These interfaces are described on page 4.

The HP emulation probe and module can be controlled over your local area network (LAN) by the debugger and connect to your target through a 16-pin Berg style connector, as shown in figure 4.

Unlike traditional emulators, the emulation probes and modules provide more stable operation by accessing only the debug pins of the microprocessor. You don't need a serial port on your target system to download code. Unlike ROM monitors, they don't require user memory.

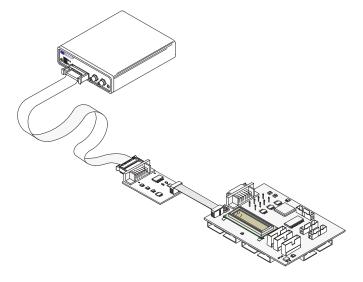


Figure 1: Standalone HP Emulation Probe

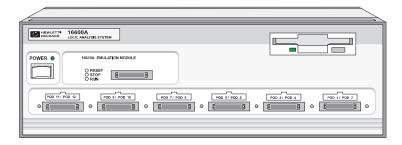


Figure 2: HP 16600A Logic Analysis System with Integrated Emulation Module

Debugger Interface

Industry-leading debuggers can control the HP emulation probe and module. You can set breakpoints, single-step through code, examine variables, and modify source code variables from the high-level source code debugger interface.

Debugger interfaces must be ordered directly from the debugger vendor.

Debugger Connections

Green Hills Software, Inc. 30 West Sola Street Santa Barbara, CA 93101 USA Phone: (805) 965-6044 http://www.ghs.com

Microtec, A Mentor Graphics Company 880 Ridder Park Drive San Jose, CA 95131 USA Phone: (800) 950-5554 Phone: (408) 487-7000 http://www.mri.com

Software Development Systems, Inc. 815 Commerce Drive, Suite 100 Oak Brook, Illinois 60523 USA Phone: (630) 368-0400 http://www.sdsi.com

Please check with your local HP Test and Measurement sales office or visit our web site at http://www.hp.com/go/las-data for the current list of debugger connections.

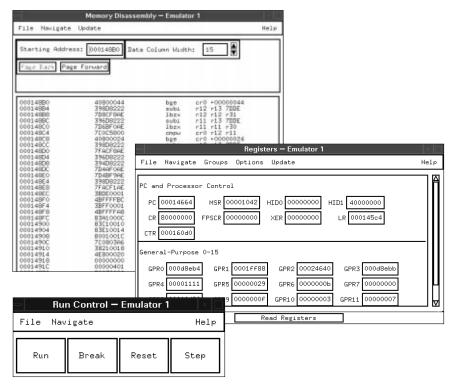


Figure 3: Emulation Control Interface

Emulation Control Interface

The emulation module integrated into the logic analysis system can be controlled directly by the emulation control interface. You can easily display and modify contents of microprocessor registers, system memory, and I/O. You can also view memory code segments disassembled into familiar Motorola/IBM PowerPC 6XX assembly instructions.

From the run control window you can instruct the microprocessor to run, break, reset, or single-step. You also can choose whether the memory, I/O, and register displays are updated for breaks and single steps.

Writing command files that set up registers, memory, and I/O in your system is easy with the command language. Once the command file is written, save it on the logic analyzer hard disk. When you want to initialize your hardware system to a particular state, simply recall and execute the command file. Unlike a debugger interface, the emulation control interface does not reference back to the high-level source code.

Emulation Module and Probe Migration

HP protects your current investment by providing a migration path for the emulation modules and probes as your needs change. To move from one processor family to another, simply order a migration kit for the emulation module or probe, which will provide all the necessary hardware, firmware, and cables to support your new processor family at a fraction of the cost of a new system.

This same migration path works for the emulation probes or emulation modules.

Emulation Module Triggering Integration with Logic Analyzer

With the emulation module, use the powerful triggering of the HP 16600A and 16700A Series logic analysis systems to halt on events such as microprocessor activity, system buses, or other external events. The emulation module also can trigger the logic analyzer when a breakpoint is hit. This provides powerful event correlation between the debugger interface environment and the logic analyzer.

Specification	Description		
Microprocessors	Motorola Part Numbers MPC 600AFExxxA, MPC 600AFExxxB		
Supported	IBM Part Numbers(f)	IBMxx EMPPC yyyyy, IBMxx EMPPC yyyyy,	
		IBMxx PPC yyyyy	
Physical Connections	Ethernet	10base2 or 10baseT Ethernet connections	
	RS-232	1200 through 115 Kbaud rates supported	
Number of Breakpoints	Virtually unlimited software breakpoints		
	or one hardware breakpoint		
Physical Size	155 mm width x 161 mm depth x 65 mm height		
Environmental			
Temperature	Operating: 5 °C to +40 °C (+41 °F to + 104 °F)		
	Nonoperating: -40 °C to +70 °C (-40 °F to +158 °F)		
Altitude	Operating: 4,600 m (15,000 ft)		
	Nonoperating: 4,600 m (15,000 ft)		
Humidity	15% to 80% @ 40 °C for 24 hours		
Regulatory Compliance	e EMC CISPR 11:1990/EN 55011:1991 Group 1, Class A		
	IEC 801-2:1991/EN 50082-1:1992 4 kV CD, 8 kV AD		
	IEC 801-3:1984/EN 50082-1:1992 3 V/m, (1 kHz 80% AM, 27-1 kMz)		
	IEC 801-4: 1988 / EN 50082	2-1:1992 0.RkV Sig lines, 1 kV Power lines	
Safety Approvals	IEC 1010-1:1990		
	AMD 1:1992		
	UL 1244		
	CSA-C22.2 No. 231		
	(Series M-89)		

Table 2: HP Emulation Probe and Module Specifications

Note f: where xx = frequency, where yyyyy = Processor

Emulation Probe and Module Target Connection Information

A 16-pin male 2X8 header Berg style connector is needed on the target development board to connect the PowerPC 6XX microprocessor interface assembly to the JTAG debug port of the microprocessor.

The header should be placed as close as possible to the processor to ensure signal integrity. TD0, TD1, TCK, TMS, and /TRST signal traces between the JTAG connector and the PowerPC 6XX must be less than three inches. If these signals are connected to other nodes, you must connect in a daisy chain between the JTAG debug connector and the PowerPC 6XX. These signals are sensitive to crosstalk and cannot be routed next to active signals, such as clock lines on the target board.

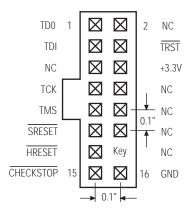


Figure 4: Target Development Board Header Connector (Top View)

Header	PPC 600	Board	5
Pin No.	1/0	600	Resistor
1	Out	TD0	
2		NC	
3	In	TDI	1KΩ pulldown
4	In	TRST	10KΩ pullup
5		NC	
6		Power*	1KΩ series
7	In	TCK	10KΩ pullup
8		NC	
9	In	TMS	10KΩ pullup
10		NC	
11	In	SRESET	10KΩ pullup
12		NC	
13	In	HRESET	10KΩ pullup
14		KEY	
15	Out	CHECKSTOP	1KΩ pullup
16		GND	

Table 3. JTAG Interface Connections

The +POWER signal is sourced from the development board and is used as a reference signal. It should be the power signal supplied to the processor (either +3.3V or +5V). It does not supply power to the HP emulation probe.

Note NC Refers to No Connect

Target System Requirements for PowerPC 603/e

(Please note the following is a partial list of requirements. Please refer to the users manuals, for more details.)

Mask Revision dd1

PPC603e silicon does not work in debug mode with either cache enabled.

Mask Revision dd3

PPC603 silicon can be used with the emulation probe and module.

/QACK Signal

If a target does not use the /QACK signal, the board must have a 1 KOhm pull down resistor to drive this signal low.

Reset Signal

The HRESET SRESET, and TRST signals from the JTAG connector must be logically ORed with the HREST, SRESET, and TRST signals that connect to the processor on the target system.

Unsupported Modes

The emulation probe and module do not support any target systems which:

- Enable caches (PPC603 and PPC604)
- · Use MMU for address translation
- Access devices that check parity (PPC603 and PC603e)
- · Try to access TLB entries

Motorola MVME 160X, Ultra, Atlas and Series E Target Boards

These boards have a unpopulated header location for installing the 16-pin connector. You must install a 16-pin connector as described earlier.

A resistor change is required to pull QACK low. The 1KOhm resistor that goes between the PPC603 and the PPC105 must be changed to 10 ohm.

For the MVME1603 series PM603 module this resistor is R27 on the 8018F, 8019F, 8100F and 8101F artwork.

For the Atlas it is R42 on the Rev B 8115F artwork. For the Ultra, it is R10 on the 8107D and later artwork.

These boards use DRTRY mode, so the configuration entry "cf drty=on" must be set on the emulation probe and module if cache is enabled.

The configuration entry "cf reset = runrom" also must be set.

Cogent CSB277

This board asserts AACK for more than one clock cycle. For proper disassembly, "Delayed-AACK" version of the inverse assembler must be used with the logic analyzer.

Target System Requirements for Other PowerPC Processors

For PowerPC processors other than the 603 and 603e, all target requirements are described in the "readme" files on the floppy disks provided with the emulation probe and module.

Real-Time Trace Analysis

Real-time trace analysis consists of a physical connection to signals on the Motorola/IBM PowerPC 603/e and 604/e microprocessors, acquisition of relevant data, and analysis of the captured bus information.

Physical connection to the microprocessor is provided by the probing solutions listed below. Either of the two probing solution alternatives will provide trace analysis on the PPC 603/e. Trace analysis is only possible with the analysis probe for the PPC 604/e.

The real-time trace analysis solutions are available for both probing alternatives. These include inverse assembly, source correlation, and optional system performance analysis.

For information on the data acquisition modules for the HP 16600A and 16700A Series logic analyzers, please refer to related HP literature on page 15.

MPC 8XX Microprocessor	Supported Speed	Probing Solutions	Real-Time Trace Solutions	
PPC 603/e	Processor Signals for logic analysis Up to 200 MHz Analysis Probe: PPC 603/603e 240-pin QFP probing solution PPC 604/604e 289-pin PGA probing solution Inverse assembler included Access to all microprocessor signals for logic analysis		Inverse Assembly: • Disassembly of bus information into PPC 6XX microprocessor mnemonics • PPC 6XX configuration files for logic analyzers Source Correlation: • Time-correlation of acquired trace to	
PPC 604/e	Up to 200 MHz	Optional Mictor Connector Solution for PPC 603/e: • Mictor connectors designed in target for access to critical signals for logic analysis	high-level source code Trigger and search through trace in high-level source code System Performance Analysis: Statistical performance measurements on trace data State overview, state interval, time interval, and time overview measurements	

Table 4: Real-Time Trace and Probing Alternatives

PowerPC 603/603e Analysis Probe

The analysis probe allows easy connection of an HP logic analyzer to your Motorola/IBM PowerPC 603/603e QFP target system for real-time analysis. With the analysis probe solution, you don't need to design special debug connectors into your target system.

The Motorola/IBM PowerPC 603/603e analysis probe consists of:

- · Analysis probe board
- Inverse assembler and configuration files
- 240-pin elastomeric probing solution
- Five HP E5346A high-density termination adapters
- · User's guide

Elastomeric Probing Solution

The elastomeric probing solution included in the analysis probe offers an inexpensive, rugged, and easy-to-use probing solution for the 240-pin QFP PowerPC 603/603e package. The probes require a minimal "keep out" area around the device, as shown in figure 13.

A retainer is glued to the top of the device, which ensures a solid connection to each pin of the device. Five retainers, a locator tool, and adhesive are included with each probe adapter.

Additional retainers and locator tools may be ordered. HP E5363A option 201 offers a kit of five additional retainers and adhesive. An additional locator tool is available as HP E5363A option 202.

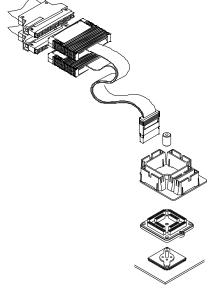


Figure 5: Analysis Probe for the PPC 603/603e

Modes of Operation

State Modes

In state-per-address or data-cycle modes, the logic analyzer records only those states in which one or more of the strobes AACK, ARTRY, TA, DRTRY, or TEA are asserted. This mode filters wait states and exposes the PowerPC 603/603e microprocessor's decoupled address and data buses.

In state-per-clock mode, address, data, and status are captured on each CPU clock. This mode is useful in hardware validation and analysis during system crashes.

Timing Mode

Timing analysis is supported. All microprocessor signals are presented to the logic analyzer unbuffered.

Pods Required

Eight, 16-channel logic analyzer pods are required for inverse assembly. These eight pods are connected to four HP E5346A high-density termination adapters included with the analysis probe. Five of these adapters are included with the analysis probe. One additional adapter is included for the other signals on the processor.

Probe Loading

- 10 pf on all signals
- 100 Kohms on all signals

HP Logic Analyzers Supported

- HP 1660A/D, 1670A/D
- HP 16550A
- HP 16554A/D, 16555A/D, 16556A/D
- HP 16600A, 16601A

Optional Accessories

The HP E2455-60002 is an optional analysis probe, which offers a connection directly to the 190-pin AMP Mictor connector on the Motorola Ultra and MVME1600-001 target boards. When using this optional analysis probe with the Motorola target boards, the complete PPC 603/e analysis probe is not needed. The inverse assembler is included with the HP E2455-60002 to provide assembly mnemonics for use with HP logic analyzers. The four HP E5346A high-density termination adapters needed must be ordered separately.

PowerPC 604/604e Analysis Probe

The analysis probe allows easy connection of an HP logic analyzer to your Motorola/IBM PowerPC 604/604e PGA target system for real-time analysis. With the analysis probe solution, you don't need to design special debug connectors into your target system.

The Motorola/IBM PowerPC 604/604e Analysis Probe consists of:

- Analysis probe
- Inverse assembler and configuration files
- 289 PGA probing solution
- Pin protector
- User's guide

The PPC 604/604e analysis probe has a Pin Grid Array (PGA) footprint. The connector on the analysis probe plugs directly into the PGA socket on the target system.

To connect the analysis probe, remove the PowerPC 604/604e microprocessor from the target system and plug it into the socket on the analysis probe. Then, plug the analysis probe into the target's socket.



Figure 6: Analysis Probe for the PPC 604/604e

Modes of Operation

State Modes

In the state-per-AACK mode the logic analyzer uses trigger-sequencer store qualifications to capture only address and data acknowledge cycles. The only states recorded are those in which one or more of the strobes (AACK, TS, ARTRY, TA, and DRTRY) are asserted. This default mode is set by the configuration files and provides the greatest information density to the logic analyzer acquisition memory.

In state-per-clock mode, the logic analyzer captures every clock cycle, including idle and wait states between and during tenures. Address, data, and status are captured on each CPU clock. This mode is useful in hardware validation and debugging system crashes.

Timing Modes

Timing analysis is supported. All microprocessor signals are presented to the logic analyzer unbuffered.

Target Signal Timing

The analysis probe requires that the AACK line have a 10.9 ns setup and 0s hold.

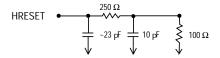
Pods Required

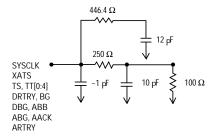
Eight, 16-channel logic analyzer pods are required for inverse assembly. There are three additional pod connections available to view other microprocessor signals.

HP Logic Analyzers Supported

- HP 1660A/D, 1661A/D, 1670A/D
- HP 16550A
- HP 16554A/D, 16555A/D, 16556A/D
- HP 16600A, 16601A, 16602A

Probe Loading





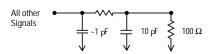


Figure 7: Signal Termination

Inverse Assembler

Software provided with the analysis probe quickly configures the logic analyzer by labeling address, data, and status signals for the PPC 6XX microprocessors. The software includes an inverse assembler, which gives you PPC 6XX mnemonics in the trace listing for easy correlation between captured data and target code. The inverse assembler also works with the HP B4620B source correlation tool set to provide time correlation between the assemblylevel trace and the high-level source code.

The inverse assembler provides filters and color coding to show and/or suppress different instructions such as data reads, data writes, unexecuted prefetches, and memory map regions.

The inverse assembler has several modes of operation, depending on your microprocessor configuration. The inverse assembler provides PPC 6XX mnemonics, but the cache must be off to see all cycles on the microprocessor.

HP B4620B Source Correlation Tool Set

The inverse assembler can be used with the HP B4620B source correlation tool set. This allows time correlation of an acquired trace to source code. The source correlation tool set uses the symbolic information provided in your object file to build a database of source files, line numbers and symbol information.

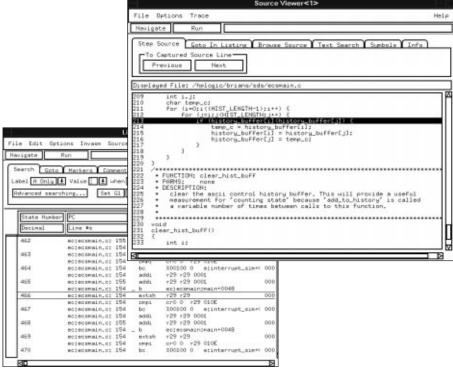


Figure 8: Inverse Assembled Trace Time-Correlated to Source Code Using the HP Source Correlation Tool Set

Once the logic analyzer acquires the real-time trace, you can step through the trace at assemblycode level or source-code level. You can also easily locate the cause of a problem by stepping backward to the root cause. With time-correlated analysis in both the digital and analog domains, HP provides powerful solutions for your most difficult hardware/software integration problems.

IEEE 695, Elf/Dwarf, and ASCII symbol files are supported.

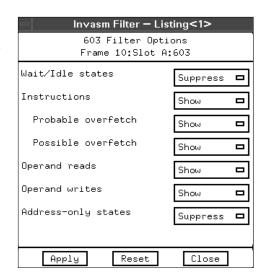


Figure 9: Inverse Assembler Filter Options

System Correlation

With the HP logic analysis systems, you can time-correlate bus information from other microprocessors or bus interfaces in your system, such as a PCI bus, with the PPC 603 or 604. Analysis probes are available for additional microprocessors. (Contact your local HP Test and Measurement sales office or visit our web site at http://www.hp.com/go/las-data for more information).

HP B4600B System Performance Analysis Tool Set

The system performance analysis (SPA) tool set is an optional software package for the HP 16600A and 16700A Series logic analysis systems. The SPA tool set provides such statistical performance measurements as state overview, state interval, time interval, and time overview. The same symbol file used with the source correlation tool set provides symbolic support for the system performance analysis tool set, as shown in figure 10.

Optional Mictor Connection Solution for the PowerPC 603/e

If system constraints won't allow use of the analysis probe, you can design high-density AMP Mictor connectors into your target system for connection to the microprocessor signals. The inverse assembler can be ordered separately to provide inverse assembly and configuration files to set up the logic analyzer.

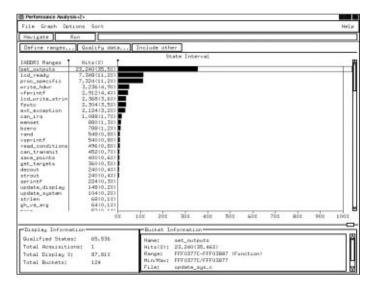


Figure 10: Statistical Performance Information from the HP System Performance Analysis Tool Set

All the necessary signals for inverse assembly can be routed to four Mictor connectors. Refer to the product note, "Passively Probing a Motorola/IBM PowerPC 603/e BGA Target System with HP E5346A High-Density Termination Adapters" (publication number 5966-4167E) for signal pin-out information. The AMP Mictor connectors can be located around the microprocessor, as shown in figure 11.

Four HP E5346A high-density termination adapters are required for connection to the logic analyzer pods. Mictor connectors can be purchased directly from AMP or from HP. Five Mictor connectors and recommended support shrouds are included in the HP E5346-68701 Mictor connector kit.

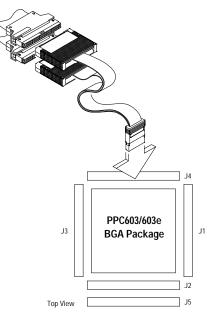


Figure 11: AMP Mictor Connector Layout

Analysis Probe Mechanical Specifications

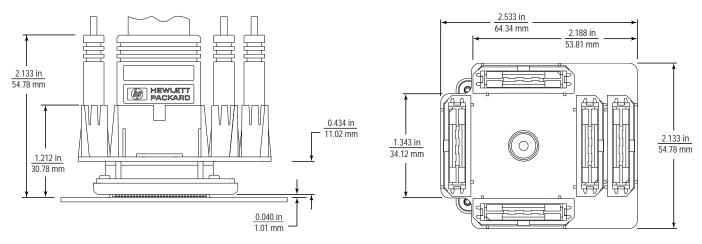


Figure 12: PPC 603/e Analysis Probe Specifications

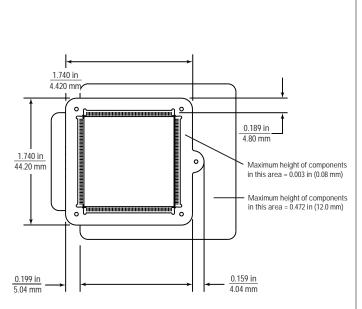


Figure 13: Elastomeric Keep-Out Information

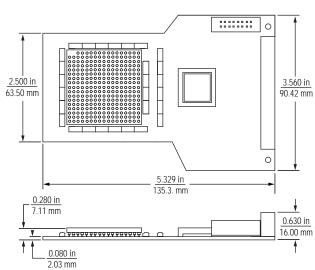
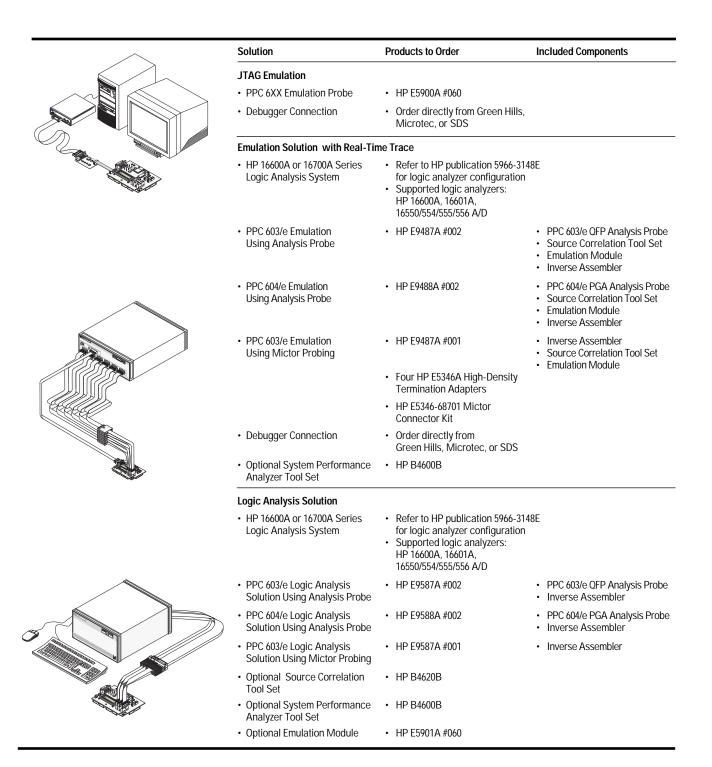


Figure 14: PPC 604/e Analysis Probe Specifications

System Configuration and Ordering Information

The table below shows the system components you need to order and what is included in each. For realtime trace, two alternatives are available to fit your needs. The solution product numbers do not include logic analysis. The HP 16600A and 16700A Series logic analysis systems must be ordered separately.

If you want to configure or upgrade your system with individual products, see page 15 for individual product number information.



Individual Components Ordering Information

Description	HP Product
PPC 6XX Emulation Probe	HP E5900A #060
PPC 6XX Emulation Module	HP E5901A #060
PPC 603/e Analysis Probe	HP E9587A #002
PPC 604/e Analysis Probe	HP E9588A #002
PPC 603/e Inverse Assembler Only	HP E9587A #001
Source Correlation Tool Set	HP B4620B
System Performance Analysis Tool Set	HP B4600B
High-Density Termination Adapter	HP E5346A
Mictor Connector Kit	HP E5346-68701

Training and Consulting

HP has experienced Digital Systems Consultants who can help you maximize the utilization of your emulation and analysis system through training and consulting. Digital Systems Consultants are peaked in debugging complex digital hardware/software problems and hardware/software integration.

HP training may be delivered through scheduled courses, on-site classes, or one-on-one consulting. HP has courses for the beginner as well as advanced users migrating from the 16500 Series system. Call 1-800-593-6632 in the U.S. for information about training schedules and location or to register. For training offered in other geographies and languages, consult the HP Test and Measurement education web site: http://www.hp.com/go/tmeducation.

For consulting services, contact your local HP Test and Measurement sales office. An HP Digital Systems Consultant can help you solve tough digital debug problems by showing you how to apply HP tools and debug best practices. Topics covered can include:

- System Installation
- Complex Triggering
- Multiple Bus Analysis
- Source-Line Referencing
- System Performance Analysis
- Instrumenting Code to Solve Specific Issues
- Bus Signal Timing Analysis
- Signal Integrity Analysis
- HP 16700A/HP1660XA Networking

Topics related to debug of PPC 6XX microprocessor-based targets can include:

- Instruction/Data Cache Related Issues
- Checkstop Analysis
- Single and Multiple Beat Bus Cycles
- · Pipelining and Bursts



Related HP Literature Pub. Number HP 16600A and 16700A Logic Analysis System Mainframes, Product Overview 5966-3107E HP Logic Analysis Systems Upgrade, **Product Overview** 5966-3059E System Configuration for the HP 16600A and 16700A Series Logic Analysis Systems, Configuration Guide 5966-3148E State and Timing Analyzers for the HP 16500C Logic Analysis System, Product Overview 5962-7245E Passively Probing a Motorola/IBM PowerPC 603/603e BGA Target System with HP E5346A High-Density Termination Adapters, **Product Note** 5966-4167E

Warranty Information

These Hewlett-Packard products have a warranty against defects in material and workmanship for a period of one year from date of shipment. During this warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For more information about the HP 16600A and 16700A Series logic analysis systems visit our web site, http://www.hp.com/go/las-data

For more information about Hewlett-Packard test & measurement products, applications, services, and for a current sales office listing, visit our web site, http://www.hp.com/go/tmdir

You can also contact one of the following centers and ask for a test and measurement sales representative.

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