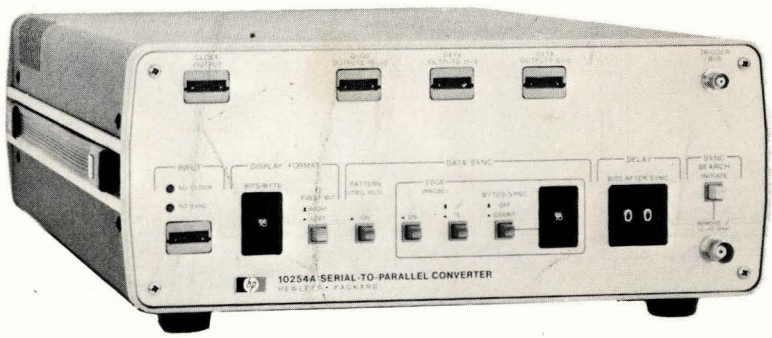
OPERATING NOTE

10254A

SERIAL-TO-PARALLEL CONVERTER



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SERIAL-TO-PARALLEL CONVERTER

Model 10254A

Serials Prefixed 1636A

OPERATING NOTE/MARCH 1977

Figure 1. Model 10254A Serial-To-Parallel Converter

1. GENERAL INFORMATION.

2. INTRODUCTION. This Operating Note contains information required to install, operate, test, and service the Hewlett-Packard Model 10254A Serial-To-Parallel Converter. Figure 1 shows the instrument and supplied accessories.

3. On the first page of this operating note is a microfiche part number. This number can be used to order 6- by 4-inch microfilm transparencies of the operating note. The microfiche package also includes the latest operating note changes supplement.

4. SPECIFICATIONS. Model 10254A specifications are listed in table 1. These specifications are the performance standards or limits against which the instrument is tested. Table 2 lists supplemental characteristics. Supplemental characteristics are not specifications but are typical characteristics included as additional information for the user.

5. INSTRUMENTS COVERED BY OPERATING NOTE. Attached to the instrument is a serial number plate. The serial number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. The suffix however, is assigned sequentially and is different for each instrument. The contents of this operating note apply to instruments with the serial number prefix(es) listed on the first page.

6. An instrument manufactured after the printing of this operating note may have a serial number prefix that is not listed on the first page. This unlisted serial number prefix indicates the instrument is different from those described in this operating note. The operating note for this newer instrument is accompanied by a yellow operating note changes supplement. This supplement contains "change information" that explains how to adapt the operating note to the newer instrument.

7. In addition to change information, the supplement may contain information for correcting errors in the operating note. To keep this operating note as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Operating Note Changes supplement. The supplement for this operating note is identified with the operating note print date and part number, both of which appear on the first page of the operating note. Complimentary copies of the supplement are available from Hewlett-Packard.

8. For information concerning a serial number prefix that is not listed on the first page or in the operating note changes supplement, contact your nearest Hewlett-Packard office.

9. DESCRIPTION. The HP Model 10254A is an accessory for Model 1600A and Model 1607A Logic State Analyzers. When used with an LSA, the 10254A provides up to 16 bytes of serial data with each byte

Operating Note Part No. 10254-90902
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displayed as one line on the table displayed by the LSA. Byte length is selectable from 1 to 16 bits with each byte right-justified on the display. The display can be formatted with first bit right or left. The instrument can synchronize to a sync signal from the system under test or on a serial data pattern up to 16-bits long. Data acquisition can be delayed up to 99 clock pulses after sync is established.

10. ACCESSORIES SUPPLIED. Figure 1 shows the Model 10254A, the Model 10236A Trigger Interface Cable, four interface cables (HP Part No. 10254-61601), and probe labels (HP Part Nos. 7120-5922 and 7120-5923).

11. EQUIPMENT REQUIRED BUT NOT SUPPLIED. To have a complete serial data analyzer, the Model 10254A must be interfaced with a Model 1600A Logic State Analyzer or with a Model 1607A Logic State Analyzer with display unit. A Six Bit Data Probe (supplied with the LSA) is required to interface the 10254A with the system under test.

12. INSTALLATION.

13. The following paragraphs provide installation instructions for the 10254A and its accessories. They also include information about initial inspection and damage claims, preparation for using the 10254A, and packing, storage and shipment.

14. INITIAL INSPECTION. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Contents of the shipment should be as shown in figure 1; procedures for checking electrical performance are given in the Performance Tests, para 43. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Tests, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

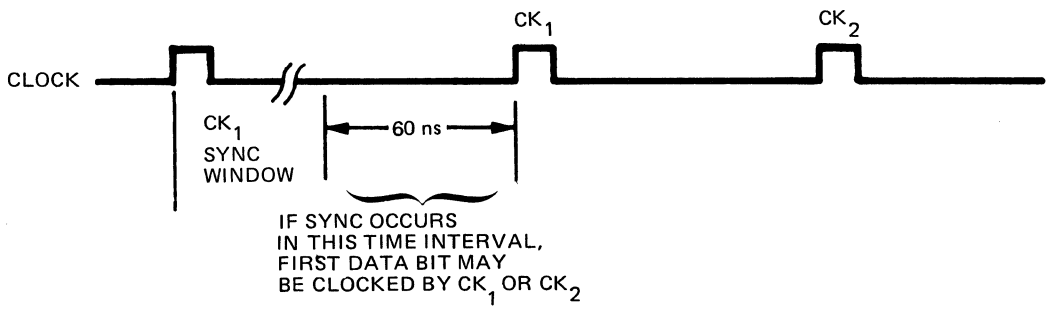
15. PREPARATION FOR USE.

16. Power Requirements. The 10254A requires power supplies of +5 Vdc, +12 Vdc, and -12 Vdc. Power is supplied by the LSA (Logic State Analyzer) through the interface cables.

Table 1. Specifications

PROBE INPUTS

REPETITION RATE: 7 MHz maximum in pattern sync mode, 10 MHz maximum in edge sync mode.
INPUT RC: 40 ±3 kΩ shunted by ≤14 pF.
INPUT BIAS CURRENT: ≤30 μA.
INPUT THRESHOLD: TTL, fixed at approx +1.5 V; variable, ±10 Vdc.
MAXIMUM INPUT
Level: ±15 Vdc.
Swing: 15 V peak from threshold.
MINIMUM INPUT
Swing: 0.5 V +5% of threshold voltage p-p.
Pulse Width: 40 ns at threshold.
Data Setup Time: time data must be present prior to clock transition, 50 ns.
Hold Time: time data must be present after clock transition, 0 ns.
Sync Occurrence: time sync edge must preceed clock transition corresponding to first data bit, 60 ns.



CLOCK AND DATA OUTPUTS

BITS/BYTE: 1 to 16 bits. (A byte is displayed as one line on the logic analyzer table display.)
BYTES/SYNC: 1 to 16 bytes. (Number of bytes of serial data acquired after each sync pulse.)

BNC AND TNC INPUTS/OUTPUTS

LEVEL: 0 to +5 V maximum.
DELAY AFTER SYNC
Number of clock pulses after sync before data acquisition, 0 to 99.

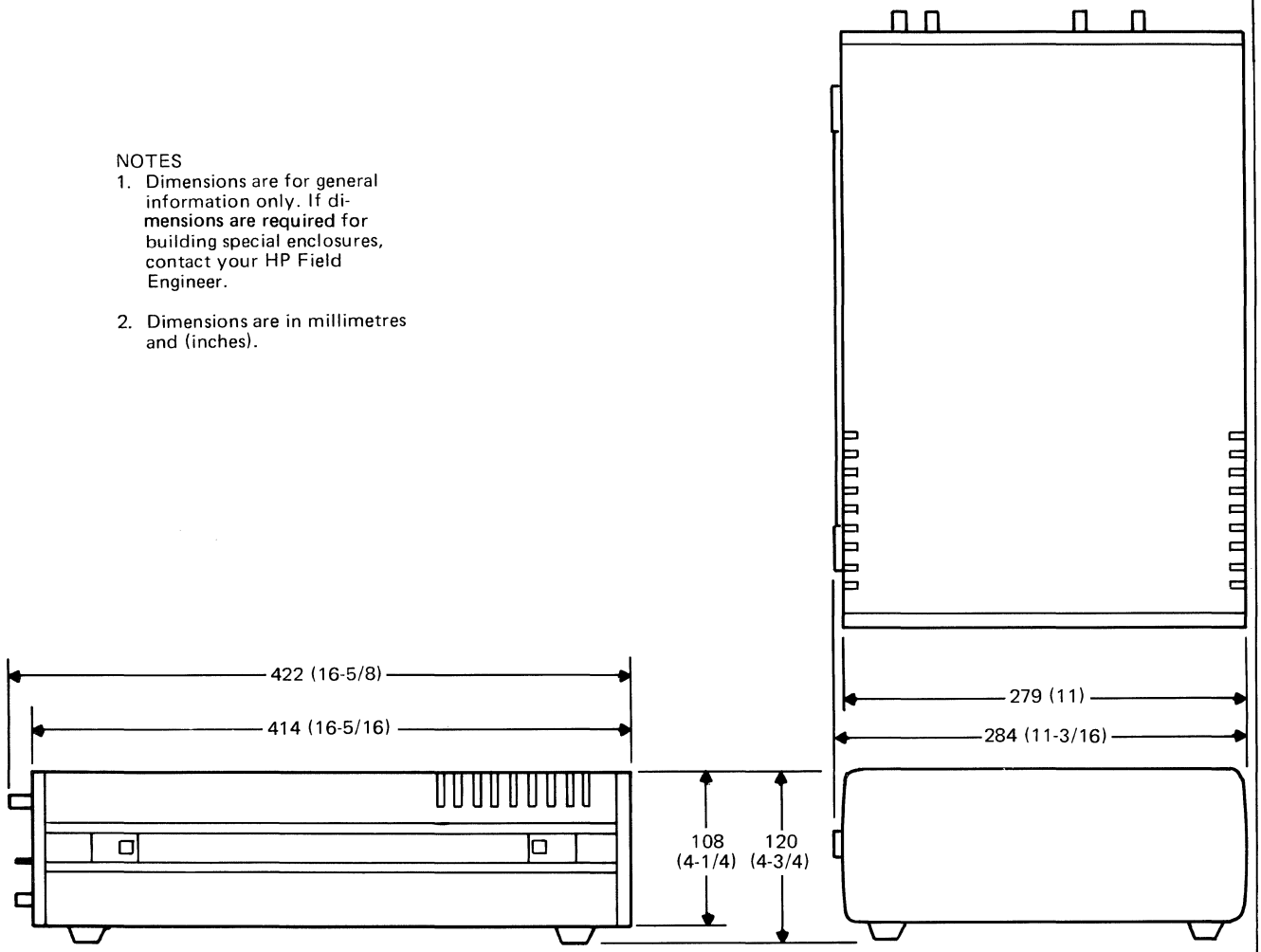
Table 2. Supplemental Characteristics

POWER REQUIREMENTS: +5 Vdc, +12 Vdc and -12 Vdc (supplied by the logic state analyzer). Power consumption is approximately 6 VA.

DIMENSIONS: see outline drawings.
WEIGHT: net, 3.2 kg (7 lb), shipping 5 kg (11 lb).
Temperature: 0°C to +55°C.
Humidity: to 95% relative humidity at +40°C.
Altitude: to 4600 m (15 000 ft).
Vibration: vibrated in three planes for 15 minutes each with 0.254 mm (0.010 in.) excursion, 10 to 55 Hz.

INSTRUMENT COMPATIBILITY
HP Model 1600A, Logic State Analyzer.
HP Model 1607A, Logic State Analyzer.
HP Model 10231B/C Six Data Probe.

NOTES
1. Dimensions are for general information only. If dimensions are required for building special enclosures, contact your HP Field Engineer.
2. Dimensions are in millimetres and (inches).



17. Interconnections. Before the instrument can be operated, the 10254A and Model 1600A or Model 1607A must be connected together with the four interface cables and trigger bus cable. Connect instruments together as follows:

10254A CLOCK OUTPUT to 1600A/1607A CLOCK INPUT
10254A Q1, Q0/OUTPUTS 15-12 to 1600A/1607A Q1, Q0/INPUTS 15-12
10254A DATA OUTPUTS 11-6 to 1600A/1607A DATA INPUTS 11-6
10254A DATA OUTPUTS 5-0 to 1600A/1607A DATA INPUTS 5-0
10254A TRIG BUS to 1600A/1607A TRIG BUS

18. REPACKING FOR SHIPMENT. If the Model 10254A is to be shipped to an HP Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required. Use the original shipping carton and packing material. If original packing material is not available, the HP Sales/Service Office will provide information and recommendations on materials to be used.

19. OPERATION.

20. The following paragraphs explain operating characteristics and the functions of controls and indicators on the 10254A.

21. PANEL FEATURES. Front panel features are described in figure 2. Description numbers match the numbers on the illustration.

22. OPERATING CHARACTERISTICS.

23. Inputs. Inputs to the 10254A from the system under test are provided through a Six Bit Data Probe. The data probe provides serial data, a synchronization signal, two clock signals, and two qualifier signals to the 10254A. The two clock signals are OR'ed together in the 10254A to provide the instrument clock. If only one clock signal is used, the other clock lead should be connected to ground. The two qualifier signals are routed through the 10254A to the LSA. See the LSA Operating and Service Manual for details on using the qualifier signals.

24. Data Synchronization. The 10254A has two synchronization modes: edge (probe) sync and pattern (trigger bus) sync. Edge sync is selected when a sync pulse is provided by the system under test through the data probe. The ⌐/¬ pushbutton selects the edge of the pulse that the 10254A synchronizes on. The ⌐ position selects the positive-going edge of the pulse as the sync, the ¬ position selects the negative-going edge of the pulse as the sync. When the sync pulse is detected, the 10254A starts acquiring data, beginning with the first clock following the sync pulse.

25. The Bytes/Sync Counter is enabled in the edge sync mode. With the OFF/COUNT switch set to COUNT, the 10254A acquires and transmits to the LSA only the number of bytes (1 to 16) selected by the BYTES/SYNC thumbwheel each time a sync signal occurs. With OFF/COUNT switch set to OFF, the Bytes/Sync Counter is disabled and the 10254A transmits all received bytes to the LSA.

26. When no sync pulse is available from the system under test, the 10254A can sync on a serial bit pattern up to 16 bits long. In the pattern sync mode, the pattern trigger recognition of the LSA is used to establish data sync. The LSA TRIGGER WORD switches are set to the desired sync pattern. When Sync Search is initiated, the 10254A clocks the LSA each time it receives a data bit from the sync under test. Since data is continuously clocked through shift registers whose outputs are applied to the 10254A data output connectors, the LSA sees every bit pattern in the serial data. When the 10254A output pattern matches the LSA trigger word, the LSA outputs a pulse (sync signal) on the trigger bus. The 10254A then formats the data into bytes referenced to the sync pattern and transmits it to the LSA. The LSA displays the sync pattern as its trigger word with subsequent bytes on the following lines.

27. Sync Search can be initiated by two methods. Pressing the SYNC SEARCH INITIATE pushbutton will start sync search. Alternately, applying a positive-going edge to the SYNC SEARCH REMOTE connector will initiate Sync Search. Once sync is established, the 10254A terminates Sync Search and repetitively outputs bytes.

NOTE

If the BITS AFTER SYNC or BITS/BYTE thumbwheel setting is changed, or if the serial input clock stops after sync is established, the 10254A may lose sync, causing the LSA display to blank. If this occurs, simply press the SYNC SEARCH INITIATE pushbutton to re-establish sync.

28. Delay. The BITS AFTER SYNC thumbwheels enable the 10254A to delay the first byte transmitted to the LSA up to 99 clock pulses after the sync signal. In the edge sync mode, the first displayed byte is that byte starting the selected number of clock pulses after the sync pulse. In the pattern sync mode, the sync pattern is displayed as the first line of the LSA display and the bytes starting after the selected delay as the subsequent lines.

29. Display Format. Display format is controlled by BITS/BYTE and FIRST BIT LEFT/RIGHT switches. The BITS/BYTE thumbwheel selects byte lengths from 1 to 16 bits. A byte is displayed as one line on the LSA table display. All bytes are right-justified on the display. When the selected byte length is less than 16 bits, the unused columns of the table display must be blanked using the LSA COLUMN BLANKING control.

30. The FIRST BIT LEFT/RIGHT pushbutton determines whether the first received serial data bit of a byte displayed as the rightmost bit (LSB) or leftmost bit (MSB) on the LSA display. The FIRST BIT LEFT/RIGHT pushbutton enables the 10254A to configure the display to match the data stream convention of the system under test.

31. LSA CONTROLS. Several logic state analyzer controls interact with the 10254A. The operation of these controls is described in the following paragraphs. For a full description of LSA controls, refer to the LSA Operating and Service Manual.

32. LOCAL/BUS and OFF/WORD Switches. Table 3 summerizes the operating modes available using the LOCAL/BUS and OFF/WORD switches. When LOCAL/BUS is set to BUS and the 10254A is in edge sync, the 10254A releases the trigger bus in time for the data byte immediately following the sync edge to be bus triggered in the LSA. If both BUS and WORD are selected on the LSA, the LSA triggers only when the first word following a sync matches the pattern

Table 3. Operating Modes

10254A SYNC MODE	LSA SWITCH SETTINGS		OPERATING MODE
	LOCAL/BUS	OFF/WORD	
EDGE	LOCAL	OFF	LSA acquires first 16 bytes of data transmitted by system under test, regardless of sync location.
EDGE	LOCAL	WORD	LSA acquires 16 bytes referenced to selected trigger word.
EDGE	BUS	OFF	LSA acquires 16 bytes referenced to sync.
EDGE	BUS	WORD	LSA acquires data only when the first byte following the sync pulse matches the selected trigger word.
PATTERN	X	OFF	10254A syncs on first serial byte received, LSA acquires sync byte and 15 following bytes.
PATTERN	X	WORD	10254A syncs on selected bit pattern. LSA acquires sync bit pattern and 15 following bytes.

selected on the TRIGGER WORD switches. If the LSA is set to LOCAL and WORD, the LSA triggers on the selected pattern whenever it occurs in the data stream.

33. When the 10254A is in the pattern sync mode, the LSA's pattern trigger performs a combing function on the serial data. With OFF/WORD set to WORD and a pattern set on the TRIGGER WORD switches, the first occurrence of the pattern generates a sync for the 10254A. The 10254A then transmits bytes to the LSA in the selected format. If OFF/WORD is set OFF or if TRIGGER WORD switches are all set to DON'T CARE, the 10254A syncs on the first byte of serial data received, since the bus trigger goes high on every clock.

34. Trigger Word. These switches select the serial data pattern in the pattern sync mode. In pattern sync, the LSA transmits a trigger pulse to the 10254A over the trigger bus when the sync pattern occurs. The trigger pulse syncs the 10254A with the serial data. TRIGGER WORD switches for unused data channels must be set to the OFF position; i.e., if the BITS/BYTE thumbwheel is set to 8, TRIGGER WORD switches 8 through 15 must be set to OFF. The switches are also used in the edge sync mode when it is desirable to trigger on a unique serial data byte.

35. Thld. The input threshold of the data probe is set to match the logic levels of the system under test with the LSA THLD switch. TTL position sets the input threshold to +1.5 V. VAR position allows the threshold to be varied from -10 Vdc to +10 Vdc using the LSA SET adjustment.

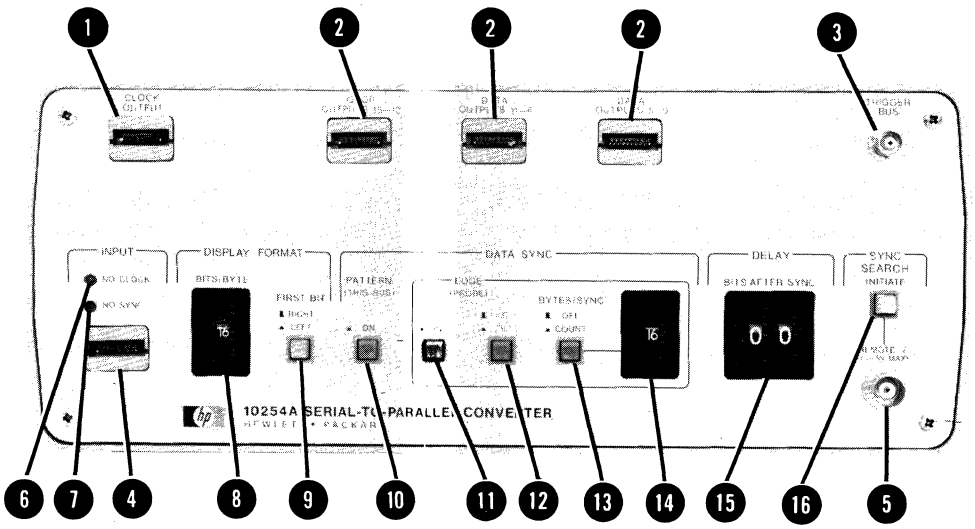
36. Clock. The LSA CLOCK switch setting determines which edge of the clock pulse from the system under test clocks the 10254A. The ⌐ position selects the positive-going edge and the ¬ position selects the negative-going edge.

37. Delay. The LSA DELAY thumbwheels set the number of bytes that displayed data is delayed from the sync or trigger when the LSA is used with a 10254A. Note that LSA DELAY differs from the 10254A BITS AFTER SYNC delay. The BITS AFTER SYNC thumbwheels select the number of bits (input clocks) delay from sync to when the 10254A sends data to the LSA.

38. LSA Display. Figure 3 shows typical LSA displays for both edge-sync and pattern-sync operation. In the edge-sync mode (figure 3A), the 10254A waits n number of bits (selected by the BITS AFTER SYNC thumbwheels) before transmitting bytes to the LSA for display. When the delay is complete, the 10254A transmits q number of bytes (selected by the BYTES/SYNC thumbwheel) to the LSA. The 10254A then waits for another sync signal and repeats the above cycle.

39. In the pattern-sync mode (figure 3B), the LSA displays the sync pattern when it is detected and, at the same time, transmits the sync signal to the 10254A. On receiving the sync signal, the 10254A waits the number of bits selected on the BITS AFTER SYNC thumbwheels and then begins transmitting subsequent bytes to the LSA for display.

40. OPERATOR'S CHECK. This check allows the operator to make a quick evaluation of the instrument's main functions prior to use. These checks assume the 10254A is connected to a 1600A or 1607A LSA. Therefore, if correct indications are not obtained, the trouble may possibly be the LSA. If the 10254A is suspected, follow the troubleshooting procedures in this operating note to isolate the problem.



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INPUTS/OUTPUTS

❶ **CLOCK OUTPUT.** Output connector for LSA (Logic State Analyzer) clock signals. Connector also supplies power to 10254A.

❷ **Q1, Q0, OUTPUTS 15-12; DATA OUTPUTS 11-6; DATA OUTPUTS 5-0.** Data output connectors. Each connector supplies six parallel data channels (bits) to the LSA. Connector also supplies power to 10254A.

❸ **TRIGGER BUS.** Trigger bus connector. In PATTERN (TRIG BUS) sync mode, LSA transmits sync pulse to 10254A over TRIG BUS. In EDGE (PROBE) sync mode, 10254A transmits trigger pulse to LSA over TRIG BUS.

❹ **INPUT.** Input connector for data probe. Supplies two qualifier channels, two clock channels, one sync channel, and one data channel from system under test.

❺ **REMOTE ⌐.** Input connector for remote sync search initiate signal.

INDICATORS

❻ **NO CLOCK.** When lit, LED indicates that 10254A has not received a clock pulse for more than 50 ms.

❼ **NO SYNC.** When lit, LED indicates that 10254A has not received a sync pulse for more than 50 ms.

❽ **BITS/BYTE.** Thumbwheel switch for selecting output byte length. Byte lengths are selectable from 1 to 16 bits. A byte is displayed as one line on the LSA table display.

❾ **FIRST BIT RIGHT/LEFT.** Configures output byte to input data stream convention. Out position configures byte with first bit received displayed on right side of table.

❿ **PATTERN (TRIG BUS).** ON position selects pattern sync mode. In pattern sync, the 10254A sync signal is supplied by the LSA on the trigger bus. The LSA provides a pulse on the trigger bus whenever incoming data matches the LSA trigger conditions.

⓫ **EDGE (PROBE) ON.** ON position selects edge sync mode. In edge sync, the 10254A accepts sync signals from the system under test through the probe.

⓬ ⌐ / ¬. Selects either leading or trailing edge of sync pulse as synchronization signal. This switch is disabled in pattern sync mode.

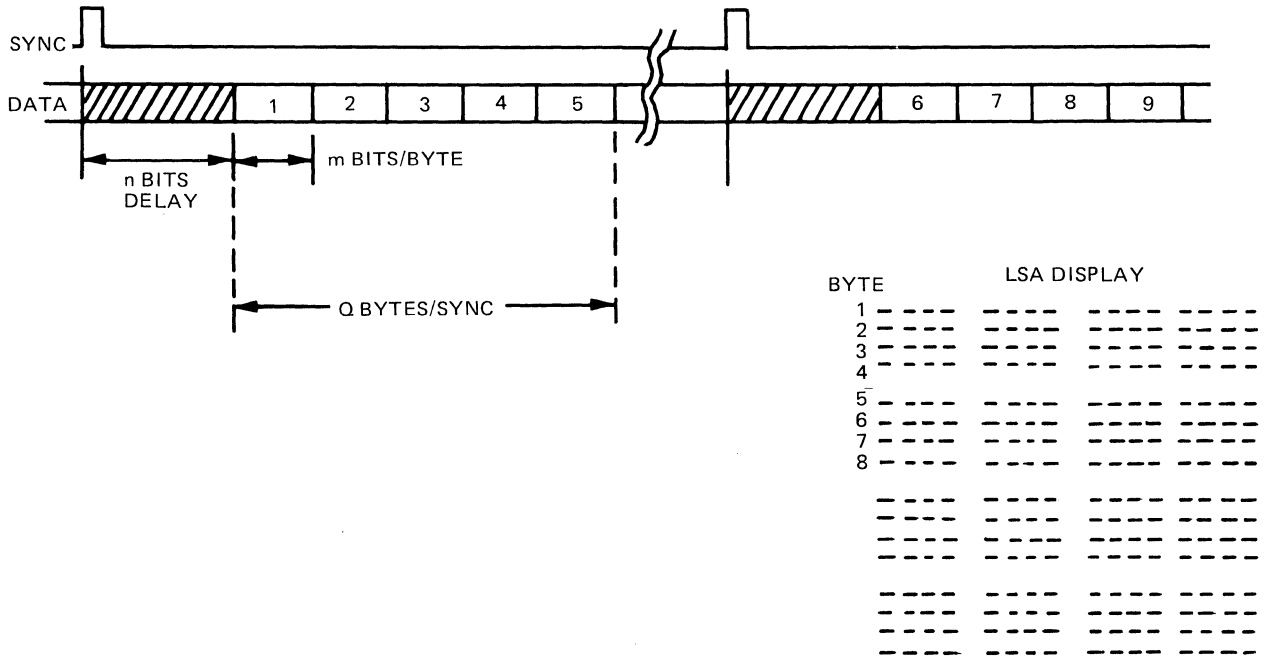
⓭ **BYTE/SYNC OFF/COUNT.** In OFF position, the 10254A outputs all bytes after sync signal. In COUNT position, the 10254A outputs only the number of bytes selected by the BYTES/SYNC thumbwheel each time a sync pulse occurs. This switch is disabled in pattern sync mode.

⓮ **BYTES/SYNC THUMBWHEEL.** Selects 1 to 16 bytes to be transmitted to the LSA each sync frame. This allows selective viewing of bytes in a serial word. This switch is disabled in pattern sync mode.

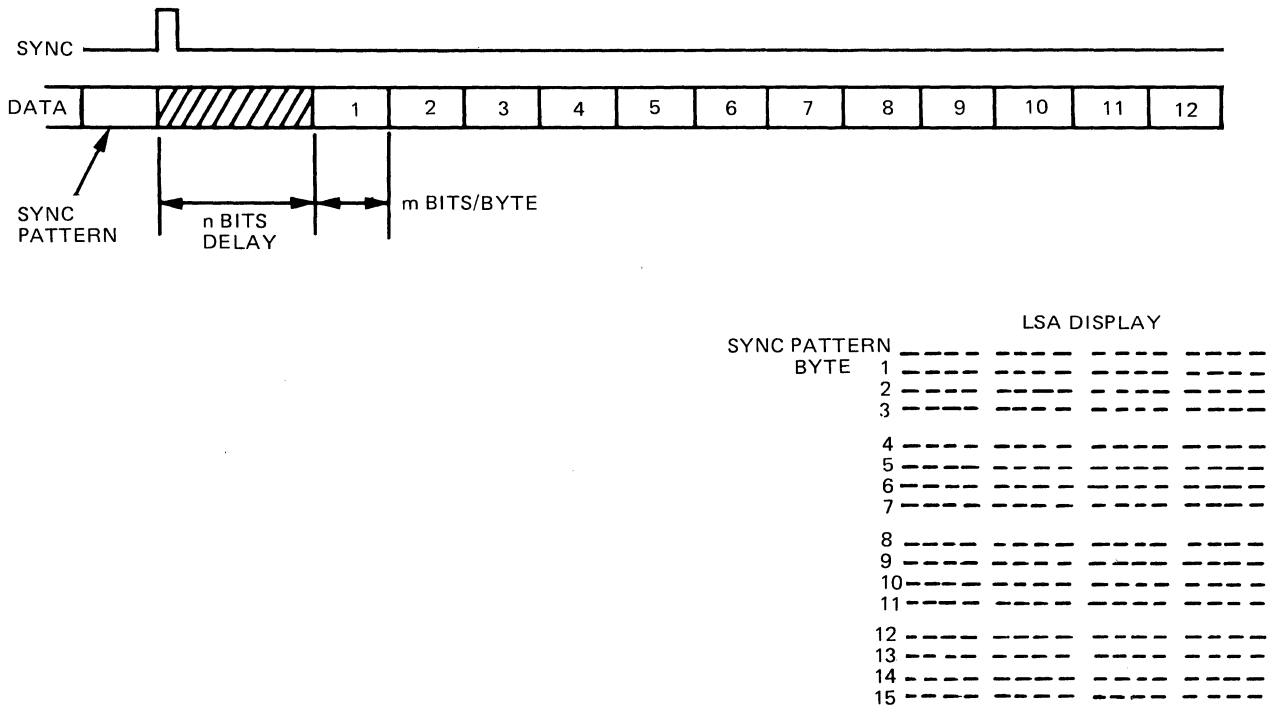
⓯ **BITS AFTER SYNC.** Thumbwheel switches select 1 to 99 clock pulses of delay after sync before data is divided into bytes and transmitted to the LSA.

⓰ **SYNC SEARCH INITIATE.** Pushing this button in pattern sync mode initiates sync search, i.e., enables 10254A to recognize next trigger pulse from LSA as sync pulse. Pushing button also clears out BITS AFTER SYNC delay and clears all data in the shift registers.

Figure 2.
Front Panel Controls, Connectors, and Indicators



A. EDGE SYNC MODE



B. PATTERN SYNC MODE

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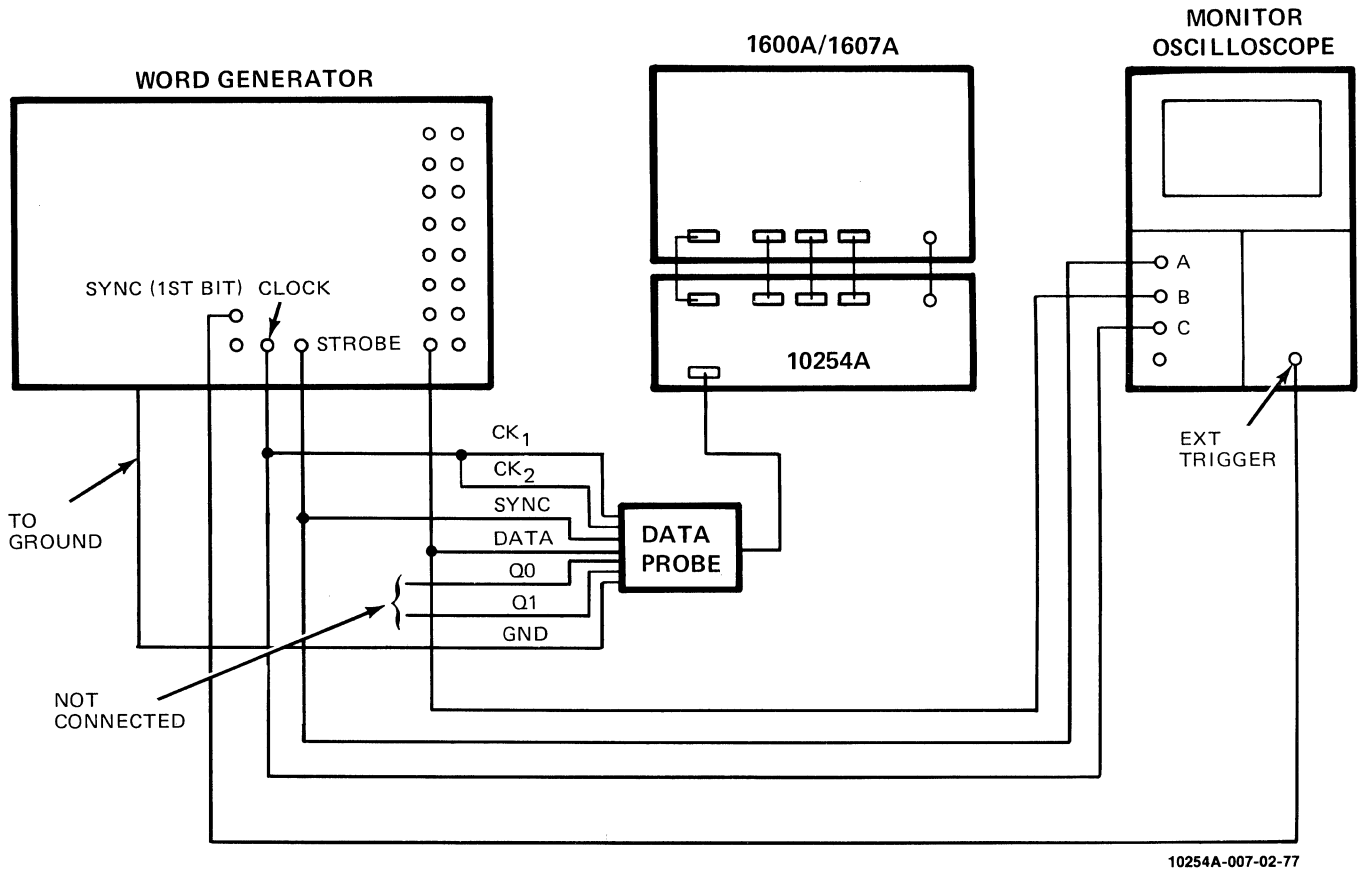
Figure 3. LSA Display Formats



OSCILLOSCOPE CONTROL SETTINGS

CHANNELS A, B, & C ..... 2 V/DIV
TIME/DIV ..... 0.05 ms
TRIGGER ..... A

NOTE: REFER TO TABLE 4 FOR TEST EQUIPMENT REQUIREMENTS

Figure 4. Operator's Checks and Performance Test Setup

a. Set up test equipment as shown in figure 4.

b. Connect BNC male-to-dual banana post adapters (3) to CLOCK, STROBE, and CHANNEL 8 outputs of word generator.

c. Connect Data Probe to word generator as follows:

10231B/C		Word Generator
CK_1 or CK_2, other CK to GND	to	CLOCK
SYNC	to	STROBE
SER DATA	to	DATA (CHANNEL 8)
GND	to	Ground
QUAL 1, QUAL 0	-	no connection

d. Set word generator controls as follows:

BIT RATE	5-50 MHz
BIT RATE VERNIER	2 o'clock
CHANNEL SERIALIZER	1 x 256
CYCLE MODE	AUTO
RZ WIDTH	10-100 ns
RZ WIDTH VERNIER	2 o'clock
WORD DELAY	0-100 ns
WORD DELAY VERNIER (Channel 8)	full CCW
WORD RZ/NRZ (Channel 8)	RZ
STROBE RZ/NRZ	RZ
OUTPUT	TTL

e. Program word generator DATA. For channels 1-8, set odd bits high, even bits low.

f. Program word generator STROBE. For channel 1, set bit 1 high, all other bits low. For channels 2-8, set all bits low.

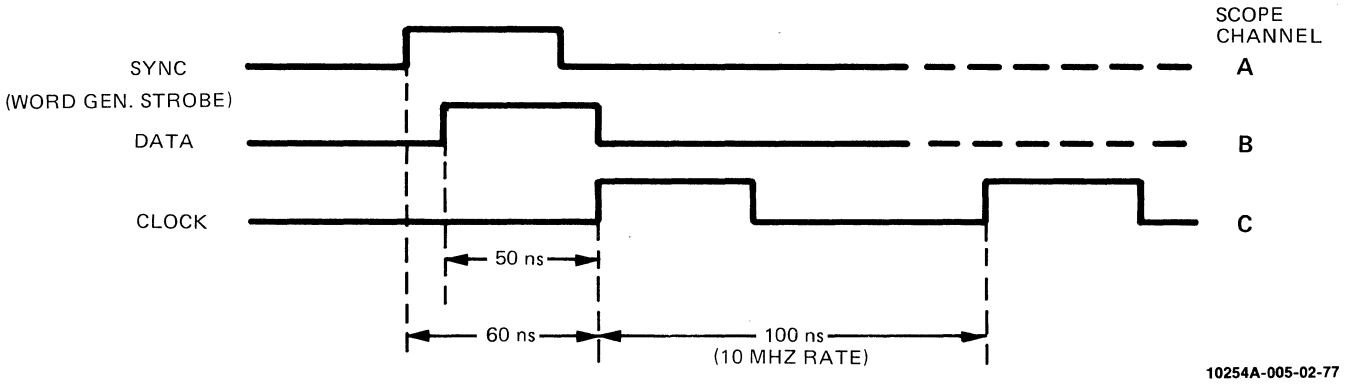


Figure 5. Performance Test Waveforms

g. Adjust word generator BIT RATE VERNIER, RZ WIDTH VERNIER. STROBE DELAY VERNIER, CLOCK DELAY VERNIER, WORD DELAY VERNIER for timing waveforms shown in figure 5.

h. Set 10254A controls as follows:

BITS/BYTE	16
FIRST BIT RIGHT/LEFT	RIGHT
EDGE (PROBE) ON	In position
⌐/¬	⌐
BYTE/SYNC OFF-COUNT	OFF
BITS AFTER SYNC	00

i. Set 1600A controls as follows:

THLD	TTL
CLOCK	⌐
TRIGGER WORD	Odd bits HI, even bits LO
OFF/WORD	WORD
SAMPLE MODE	REPET
DISPLAY MODE	TABLE A
Q0, Q1	OFF

j. Proper operation is verified by LSA display of 1's and 0's with all LED indicators off.

41. OPERATING INSTRUCTIONS.

42. Figure 6 shows a general operating setup for the 10254A. The following steps provide a general operating procedure for the 10254A.

a. Connect 10254A clock and data outputs to LSA clock and data inputs using 4 interface cables.

b. Connect 10254A TRIGGER BUS connector to LSA TRIG BUS connector using Trigger Interface Cable.

c. Connect Data Probe to 10254A INPUT connector.

d. Turn on and adjust LSA according to procedures in the LSA Operating and Service Manual.

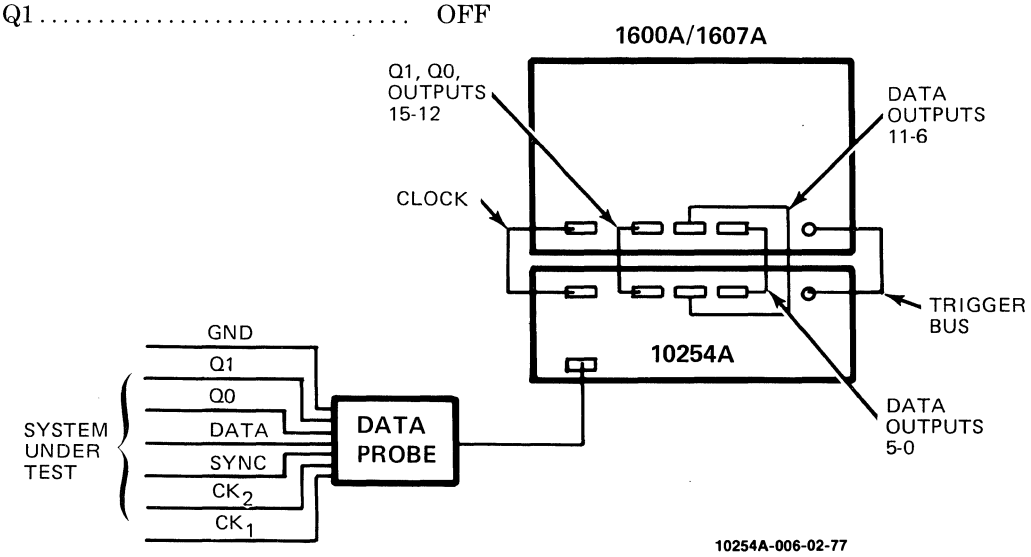


Figure 6. General Operating Setup

e. Connect data probe leads to circuitry under test (See figure 6).

f. Select clock slope. Set LSA CLOCK switch to match clock pulse slope requirements of system under test. OUT for positive-edge triggering, in for negative-edge triggering.

g. Select threshold. Set LSA THLD switch to TTL for threshold of 1.5 V. For other threshold levels, select VAR and adjust SET for threshold of system under test.

h. Select display format. Set BITS/BYTE thumbwheel for number of bits in each byte. A byte is displayed as one line on LSA table display. When less than 16 bits/byte are selected, use LSA COLUMN BLANKING control to blank unused columns on display. Display is always right justified.

i. Select first bit left or right. RIGHT position displays first serial bit of received byte as rightmost bit on display, LEFT position displays first bit received as leftmost bit on display with unused columns blanked by the LSA COLUMN BLANKING control.

j. Select delay. BITS AFTER SYNC thumbwheels select 0 to 99 bits of delay after sync before data is divided into bytes and transmitted to LSA.

k. Select LSA qualifier mode if qualification is desired. See LSA manual for details.

l. Select data sync mode. To synchronize on sync pulse supplied by system under test, select EDGE and perform steps m through o. To synchronize on serial data pattern up to 16 bits long, select PATTERN and proceed to step o.

m. Select sync edge. Set ⌐‾/‾¬ to ⌐‾ to sync on positive-edge of sync pulse or to ‾¬ to sync on negative-going edge of sync pulse.

n. Select number of bytes to be acquired each sync interval. To acquire and display from one to 16 bytes after sync, set OFF/COUNT switch to COUNT and BYTES/SYNC thumbwheel to desired number of bytes. To view all bytes after sync, set OFF/COUNT switch to OFF.

o. Set LSA LOCAL/BUS and OFF/WORD switches to desired positions. See table 3.

p. Select sync pattern. Set LSA TRIGGER WORD switches to desired serial data pattern. Set TRIGGER WORD switches for unused columns to OFF position.

q. In pattern sync, initiate SYNC SEARCH by pressing INITIATE pushbutton or by applying positive-going TTL-compatible, edge to REMOTE ⌐‾ connector.

43. PERFORMANCE TESTS.

44. The following procedures test electrical performance of the 10254A using the specifications of table 1 as the standard. All tests can be performed without removing instrument covers.

Equipment Required. Equipment required for the performance tests is listed in table 4. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended models.

Probe Input Specifications. Refer to the Performance Test Section of the logic state analyzer service manual for verification of the following specifications:

Input RC
Input Bias Current
Input Threshold
Maximum Input (Level and Swing)
Minimum Input (Swing)

45. Edge Sync Mode and Display Format Specifications. The following procedures verify the specifications and functions listed below:

Edge Sync Repetition Rate, 10 MHz Max
Sync Occurrence, >60 ns before clock
First Bit Left/Right Formats
Bits/Byte, 1 to 16 bits
Bytes/Sync, 1 to 16 bytes
Delay After Sync, 0 to 99 clocks

46. First Bit Left/Right.

a. Set up test equipment as shown in figure 4.

b. Connect BNC male-to-dual banana post adapters (3) to CLOCK, STROBE, and CHANNEL 8 outputs of word generator.

c. Connect Data Probe to word generator as follows:

10231B/C		Word Generator
CK_1 or CK_2 (other CK to GND)	to	CLOCK
SYNC	to	STROBE
SER DATA	to	DATA (CHAN 8)
GND	to	Ground
QUAL 1, QUAL 0	-	no connection

d. Set word generator controls as follows:

BITE RATE	5-50 MHz
BIT RATE VERNIER	2 o'clock
CHANNEL SERIALIZER	1 x 256
CYCLE MODE	AUTO
RZ WIDTH	10-100 ns

RZ WIDTH VERNIER ..... 2 o'clock
WORD DELAY ..... 0-100 ns
WORD DELAY VERNIER
(Channel 8) ..... fully CCW
WORD RZ/NRZ (Channel 8) ..... RZ
STROBE RZ/NRZ ..... RZ
OUTPUT ..... TTL
PROGRAM MODE ..... SERIAL

e. Program word generator DATA as follows:

CHANNEL	BITS HI
1	1, 2 and 18
2	3 and 20
3	5 and 22
4	7 and 24
5	9 and 26
6	11 and 28
7	13 and 30
8	15 and 32

f. Program word generator STROBE. For channel 1, set bit 1 high, all other bits low. For channels 2-8, set all bits low.

g. Adjust word generator BIT RATE VERNIER, RZ WIDTH VERNIER, STROBE DELAY VERNIER, CLOCK DELAY VERNIER, and WORD DELAY VERNIER for timing waveforms shown in figure 5.

h. Set 10254A controls as follows:

BITS/BYTE 16
FIRST BIT RIGHT/LEFT ..... RIGHT
EDGE (PROBE) ON ..... In position
⎍/⎏ ..... ⎍
BYTES/SYNC OFF-COUNT ..... OFF
BITS AFTER SYNC 00

i. Set 1600A TRIGGER WORD switches as follows:

Bit 0, 1 ..... HI
Bits 2 - 15 ..... LO
TRIGGER WORD ..... WORD

j. Verify that display matches figure 7A.

k. Set 10254A FIRST BIT LEFT/RIGHT switch to LEFT.

l. Set 1600A TRIGGER WORD switches as follows:

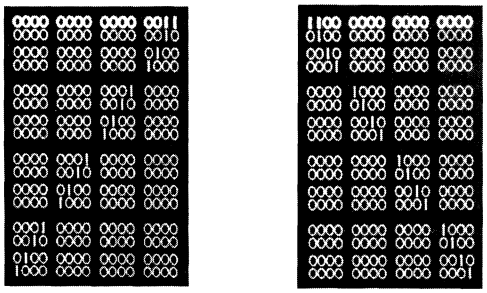
Bit 15, 14 ..... HI
Bits 13 - 0 ..... LO

m. Verify that display matches figure 7B. Correct displays indicate proper operation of FIRST BIT LEFT/RIGHT switch.

Table 4. Recommended Test Equipment

Instrument	Critical Specification	Recommended Model	Use*
Logic State Analyzer	No Substitute	1600A/1607A	P, T
Oscilloscope	3 channels, 50 MHz Sweep speed .1 μs x 10	180/1804A/1820C	P, T
Word Generator	1-by-256 word length	8016A	P, T
Interface Cable Assy (4)	No Substitute	(10254-61601)	P, T
Data Probe	No Substitute	10231B/C	P, T
Trigger Bus Cable	No Substitute	10236A	P, T
Probe	Scope vertical Bandwidth compatibility	10004B	P/T
BNC Male-to-Dual Banana Post Adapter (3)	Connection for 10231B/C Probe Tips	10110A	P/T

* P = Performance Test, T = Troubleshooting



A. B.

Figure 7. First Bit Left/Right Test Displays

47. Bits/Byte.

a. Set 10254A FIRST BIT LEFT/RIGHT switch to RIGHT.

b. Set LSA TRIGGER WORD switches as follows:

Bit 0, 1	HI
Bits 2 - 15	LO

c. Verify that display matches figure 7A.

d. Advance the bits/BYTE thumbwheel to 4, 8, and 12. Verify that displays match figures 8A through 8C for selected settings. Correct displays indicate proper operation of Bits/Byte function.

e. Set 10254A BITS/BYTE thumbwheel to 16 and vefity that LSA display matches figure 7A.

48. Bytes/Sync.

a. Set BYTES/SYNC OFF/COUNT switch to COUNT.

b. Advance BYTES/SYNC thumbwheel from 1 to 16 and verify that displays match figures 9A through 9D for selected settings. Correct displays indicate proper operation of the Byte/Sync function.

c. Return BYTES/SYNC thumbwheel to 16. 16 bytes/sync display will match figure 7A.

d. Set Bytes/Sync OFF/COUNT switch to OFF.

49. Delay After Sync.

a. Change LSA controls as follows:

OFF/WORD	OFF
LOCAL/BUS	BUS

b. Set BITS AFTER SYNC thumbwheels to 1 and verify that LSA display matches figure 10A.

c. Advance the BITS AFTER SYNC thumbwheels from 1 to 99 and verify that LSA displays match figures 10B through 10I for selected values. Correct displays indicate proper operation of delay function.

d. Return DELAY BITS AFTER SYNC thumbwheel to 00.

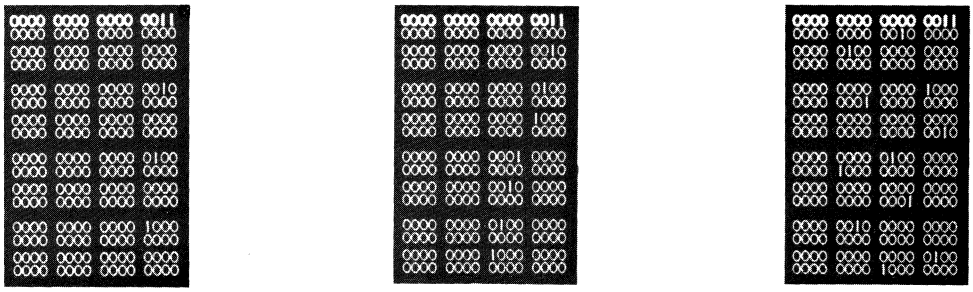
50. Pattern Sync Mode Specifications. This procedure verifies the following specifications and functions:

Pattern Sync Repetition Rate, 7 MHz max
Pattern Sync Search

a. Change clock period of clock pulse in figure 5 from 100 ns to 140 ns (7 MHz repetition rate).

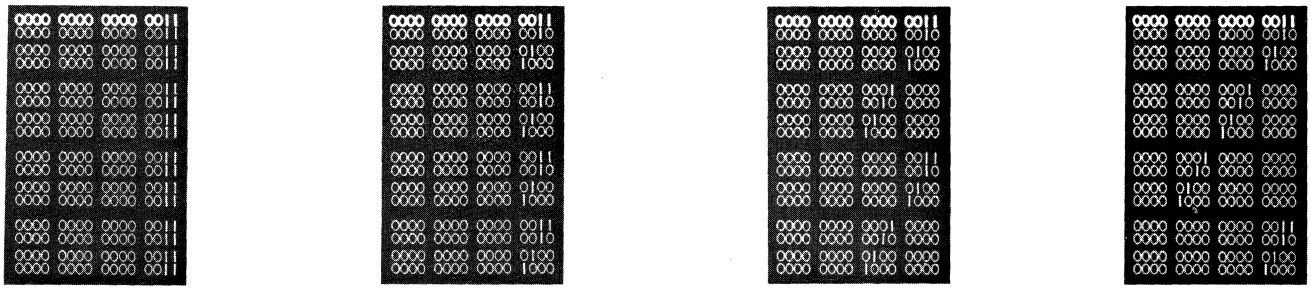
b. Program the word generator DATA as follows:

CHANNEL	BIT VALUES	
1	Bits 1, 3, 5, 7-10, 12, 14, 16-31 HI	Bits 2, 4, 6, 11, 13, 15, 32 LO
2	Bits 1-14 HI, Bits 15-16 LO	Bits 17-29 HI, Bits 30-32 LO
3	Bits 1-12 HI, Bits 13-16 LO	Bits 17-27 HI, Bits 28-32 LO
4	Bits 1-10 HI, Bits 11-16 LO	Bits 17-25 HI, Bits 26-32 LO
5	Bits 1-8 HI, Bits 9-16 LO	Bits 17-23 HI, Bits 24-32 LO
6	Bits 1-6 HI, Bits 7-16 LO	Bits 17-21 HI, Bits 22-32 LO
7	Bits 1-4 HI, Bits 5-16 LO	Bits 17-19 HI, Bits 20-32 LO
8	Bits 1-2 HI, Bits 3-16 LO	Bit 17 HI, Bits 18-32 LO



A. 4 BITS/BYTE B. 8 BITS/BYTE C. 12 BITS/BYTE

Figure 8. Bits/Byte Test Displays



A. 1 BYTE/SYNC B. 4 BYTES/SYNC C. 8 BYTES/SYNC D. 12 BYTES/SYNC

Figure 9. Bytes/Sync Test Displays

c. Set 10254A PATTERN (TRIG BUS) switch to ON position.

d. Connect Trigger Bus Cable between LSA and 10254A and disconnect sync input from data probe.

e. Set LSA switches as follows:

OFF/WORD ..... WORD
TRIGGER WORD..... 1010 1011 1101 0101

f. Press 10254A SYNC SEARCH INITIATE pushbutton and verify that LSA display matches figure 11. Correct display indicates proper operation of instrument in pattern sync mode.

51. Qualifier Check.

a. Set LSA switches as follows:

Q1, Q2..... HI
DSPLY/TRIG ..... DSPLY
OFF/WORD ..... OFF

b. Verify that NO QUAL indicator is on.

c. Connect Q0 and Q1 leads of data probe to data output (Channel 8) of word generator.

d. Verify that NO QUAL indicator is off.

52. REPLACEABLE PARTS.

53. INTRODUCTION. The following paragraphs contain information for ordering parts. Table 7 lists all replaceable parts in reference designator order.

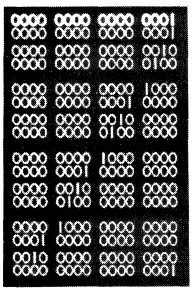
54. REPLACEABLE PARTS LIST. Table 7 is the list of replaceable parts and is organized as follows:

Electrical assemblies and their components in alphanumeric order by reference designation.
Chassis-mounted parts in alphanumerical order by reference designation.
Miscellaneous parts.
Illustrated parts breakdown.

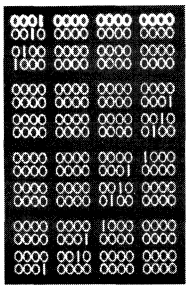
The information given for each part consists of the following:

Hewlett-Packard part number.
Total quantity (Qty) in the instrument.
Description of the part.
Typical manufacturer of the part in a five-digit code.
Manufacturers' number for the part.

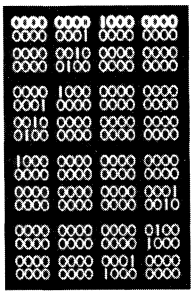
The total quantity for each part is given only once - at the first appearance of the part number in the list.



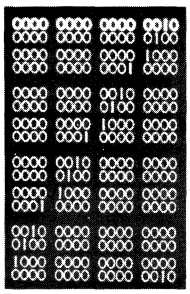
A. DELAY = 1



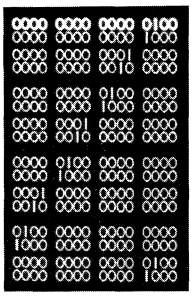
B. DELAY = 5



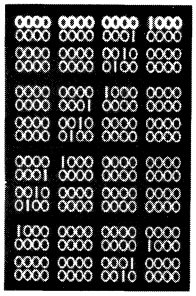
C. DELAY = 10



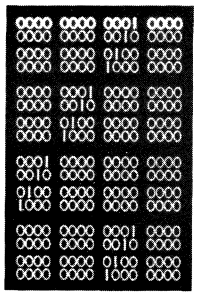
D. DELAY = 16



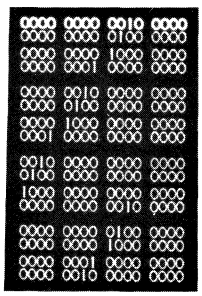
E. DELAY = 32



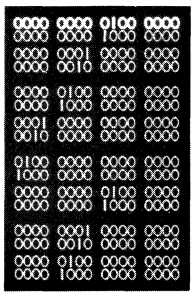
F. DELAY = 48



G. DELAY = 64



H. DELAY = 80



I. DELAY = 96

Figure 10. Delay Test Displays

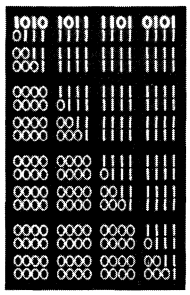


Figure 11. Pattern Sync Test Displays

55. ORDERING INFORMATION. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

56. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

57. DIRECT MAIL ORDER SYSTEM. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

Direct ordering and shipment from the HP Part Center in Mountain View, California.
No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).
Prepaid transportation (there is a small handling charge for each order).
No invoices - to provide these advantages, a check or money order must accompany each order.

58. Mail order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this operating note.

59. OLDER INSTRUMENTS.

60. This operating note applies directly to instruments which have a serial prefix number as shown on the title page of this operating note. Table 5 indicates changes required to adapt this operating note to an older instrument. Check table 5 for the proper instrument serial prefix and make the changes indicated.

Table 5. Operating Note Changes

Serial Prefix	Make Changes
No backdating changes are required at this time.	

61. PRINCIPLES OF OPERATION.

62. A functional description of 10254A circuitry is provided with the instrument block diagram in figure 12. Basic circuit descriptions giving stage-by-stage coverage are provided on service sheets at the rear of this operating note. Logic conventions used to describe the theory of operation are defined in the following paragraphs.

63. LOGIC CONVENTIONS. The positive logic convention is used in describing logic variables and circuits within the 10254A. Positive logic defines a logic "1" as the more positive voltage (high) and a logic "0" as the more negative voltage (low). The integrated circuits in the 10254A are transistor-transistor-logic (TTL).

64. MNEMONICS. Signals in the 10254A have been assigned mnemonics that describe the active state and function of the signal line. A prefix letter (H, L, P, or N) indicates the active state of the signal, and the remaining letters indicate its function. An H prefix indicates the function is active in the high state; an L prefix indicates the function is active in the low state. For edge-controlled devices, the prefix P indicates the function is active on the positive-going transition; prefix N indicates the function is active on the negative-going transition. Mnemonic functional definitions and points of origin are listed alphabetically in table 7.

65. TROUBLESHOOTING.

66. Figure 13 provides a fault isolation procedure in flowchart form. Malfunctions can be isolated to a specific circuit or component by following the step-by-step instructions. In addition to the troubleshooting tree, circuit descriptions, block diagrams, stage names, waveforms, and truth tables are included on the service sheets, when applicable, as troubleshooting aids.

Table 6. 10254A MNEMONICS

MNEMONIC	FUNCTION	ORIGIN
BITS 0-15	Parallel output bits to Logic State Analyzer.	Service Sheet 4, A1U1-U3
$\overline{CK}_1$, $\overline{CK}_2$	Complemented clock inputs from system under test.	Service Sheet 2, A1J7, PINS 15 & 16
$\overline{DATA}$	Complemented serial data input from system under test.	Service Sheet 4, A1J7, PIN 13
HBBCC	HI, Bits/Byte Count Complete. Enables Bytes/Sync Counter and Transmit Clock Gating.	Service Sheet 3, A1U35, PIN 15
HCBS	HI, Count Bytes/Sync. Enables CET input of Bytes/ Sync Counter. HCBS is DC level.	Service Sheet 3, BYTES/SYNC OFF COUNT SWITCH A1S2A
HCE	HI, Count Enable. Enables Bits/Byte Counter when Sync pulse is detected by Sync Search Latch.	Service Sheet 3, A1U21B, PIN 7
HCKE	HI, Clock Enable. Enables Transmit Clock Gating when Serial-To-Parallel Converter shift registers are loaded with good data.	Service Sheet 3, A1U31B, PIN 6
HDC	HI, Delay Complete. Signal goes high when Delay Counter has counted out delay set on BITS AFTER SYNC thumbwheels.	Service Sheet 3, A1U21D, PIN 11
HESYC/LPSYC	HI, Edge Sync/LO, Pattern Sync. DC Level. Sync Source Select and Trigger Generator control signal.	Service Sheet 3, PATTERN, (TRIG BUS) Switch A1S2D
HGD	HI, Good Data. Signal indicates Serial-To-Parallel Converter shift registers are loaded with good data.	Service Sheet 3, A1U25, PIN 15
HNORM/LSHIFT	HI, Normal/LO, Shift. High state enables Bits/Byte Counter. Low state causes Transmit Clock Gating to output PCLK and NCLK on every received system clock.	Service Sheet 3, A1U31D, PIN 11
LCKE	LO, Clock Enable. Transmit Clock Gating enable signal. LCKE goes low whenever HBBCC is true.	Service Sheet 3, A1U31C, PIN 8
LESYC	LO, Edge Sync. Control signal for Sync Search Latch and Shift Register Initialization Counter. LESYC is true when edge sync mode is selected.	Service Sheet 3, EDGE (PROBE) switch A1S2C
LSSC	LO, Sync Search Complete. LO state indicates sync signal has been received.	Service Sheet 3, A1U21B, PIN 9

Table 6. 10254A MNEMONICS (Cont'd)

MNEMONIC	FUNCTION	ORIGIN
LSSI	LO, Sync Search Initialize. Resets 10254A circuits to waiting for Sync mode in pattern sync.	Service Sheet 3, A1U29C, PIN 8
LSYNC	LO, Sync. Sync Latch Output. LSYNC drives Sync Generator.	Service Sheet 2, A1U24A, PIN 6
LSYNC*	LO, Sync*. 35 ns negative pulse output of Sync Generator. LSYNC* drives Trigger Generator.	Service Sheet 2, A1U24B, PIN 9
NCK*	Negative (Transition) Clock*. Clock signal for Trigger Generator and Shift Register Initialization Counter.	Service Sheet 2, A1U21A, PIN 5
NCLK	Negative (Transition) Clock. Clock signal output to LSA. Complement of PCLK.	Service Sheet 3, A1U19B, PIN 8
NOSC	Negative (Transition) OR'ed System Clock. OR of CK_1 and CK_2 from system under test.	Service Sheet 2, A1U33C, PIN 8
NSYNC	Negative (Transition) Sync. Delay Counter control signal derived from input sync signal.	Service Sheet 2, A1U32A, PIN 6
PCK*	Positive (Transition) Clock. Clocking signal for Transmit Clock Gating. Complement of NCK*.	Service Sheet 2, U21A, PIN 6
PCLK	Positive (Transition) Clock. Clock signal output to LSA. Complement of NCLK.	Service Sheet 3, A1U19A, PIN 6
POSC	Positive (Transition) OR'ed System Clock. OR of CK_1 and CK_2 from system under test. Complement of NOSC.	Service Sheet 2, A1U33B, PIN 6
PSYNC	Positive (Transition) Sync. Sync output of Sync slope select derived from $\overline{\text{SYNC}}$.	Service Sheet 2, A1U33A, PIN 3
QUAL 0, 1	Qualifier 0 and 1. Qualifier signals from system under test.	Service Sheet 4, A1J7, PINS 11 & 12
SI	Slope Invert. Clock slope command signal from LSA. SI=HI when LSA CLOCK switch is out (⌐), LO when LSA CLOCK switch is in (¬).	Service Sheet 2, A1J5, PIN 11
SS	Slope Switch. Clock Slope Command signal from LSA. Complement of SI. SS and SI control NOSC and POSC leading edge transitions in reference to clocking signals from system under test.	Service Sheet 2, A1J5, PIN 10
THRESHOLD	A dc level applied to the data probe that matches probe comparator switching threshold to the threshold of the systems under test.	Service Sheet 3, A1J2, PIN 8

BLOCK DIAGRAM DESCRIPTION

DATA PROBE. The 10254A monitors the system under test through a Six Bit Data Probe. The probe provides two clock channels, two qualifier channels, and sync and serial data channels.

CLOCK AND SYNC GENERATOR (Service Sheet 2). The clock and Sync generators provide clock and sync signals for the format control and serial-to-parallel converter sections of the 10254A.

Two clock signals, $\overline{CK}_1$ and $\overline{CK}_2$, from the data probe go to the Input Clock Gating and Slope Select Circuit. This circuit OR's the two input clocks together and provides two clocking signals, NOSC and POSC, to the 10254A on the selected input clock edge (determined by SS and SI). NOSC clocks the NO CLOCK indicator monostable, the delay counter, and the clock generator.

The Clock Generator derives two clock signals (NCK* and PCK*) from NOSC. NCK* and PCK* clock the Sync Generator and the Shift Register Initialization Counter, and Transmit clock Gating in the format control section.

$\overline{SYNC}$ input from the probe goes to the Sync Slope Select circuit. Sync Slope Select provides a positive-going transition (PSYNC) on the edge of the input sync pulse selected by the EDGE ⌐/¬ switch.

Sync Source Select chooses either PSYNC (edge sync mode) or the trigger bus input (pattern sync mode) as the sync signal for the 10254A. The output of Sync Source Select (NSYNC) goes to the Sync Latch and the Delay Counter.

LSYNC from the Sync Latch is clocked into the Sync Generator on the next NCK*. The Sync Generator provides LSYNC* to the Trigger Generator. The Trigger Generator provides a trigger pulse to the LSA (Logic State Analyzer) over the Trigger Bus. LSYNC presets the BITS/BYTE Counter and clears the Sync Search Latch.

FORMAT CONTROL (Service Sheet 3). Format control determines the bit length of a byte, the number of bits per sync, and the number of bits after sync that data formatting is delayed.

When a sync pulse is detected, NSYNC enables the Delay Counter. At the same time, LSYNC presets the Bits/Byte Counter. When the Delay Counter counts out the delay set on the BITS AFTER SYNC thumbwheels, HDC enables the Bits/Byte Counter. The Bits/Byte Counter counts the number of bits set on the BITS/BYTE thumbwheel and clocks the Bytes/Sync Counter when the count is complete (HBBCC). HBBCC increments the Bytes/Sync Counter and enables Transmit Clock Gating (LCKE).

When the Bytes/Sync Counter counts out the selected number of bytes per sync, it holds LCKE high, disabling Transmit Clock Gating until another sync pulse is detected.

Sync Search Initiate and the Sync Search Latch disable the counters and clock gating until the first sync pulse is received in the pattern sync mode. The Shift Register Initialization Counter disables the transmit clock output until a full data byte has been received by the Serial-To-Parallel Converter. This ensures that the first byte transmitted to the LSA contains good data, not residue from a previous cycle.

SERIAL-TO-PARALLEL CONVERTER AND QUALIFIER LATCHES. The Serial-To-Parallel Converter accepts Serial data from the system under test and converts it to a parallel format for transmission to the LSA. The Serial-To-Parallel Converter can format the parallel data with the first received serial data bit as the MSB or LSB to match the convention used by the system under test.

The qualifier Latches simply store the two qualifier signals until they are strobed into the LSA. Both the qualifiers and parallel data bytes are strobed into the LSA by NCLK and PCLK.

INTERFACE BOARD. The Interface Board routes signals between the 10254A and the LSA. The LSA provides a threshold signal, clock slope select signals, and power to the 10254A through the Interface Board. The 10254A supplies clock signals, qualifiers, and parallel data to the LSA through the Interface Board.

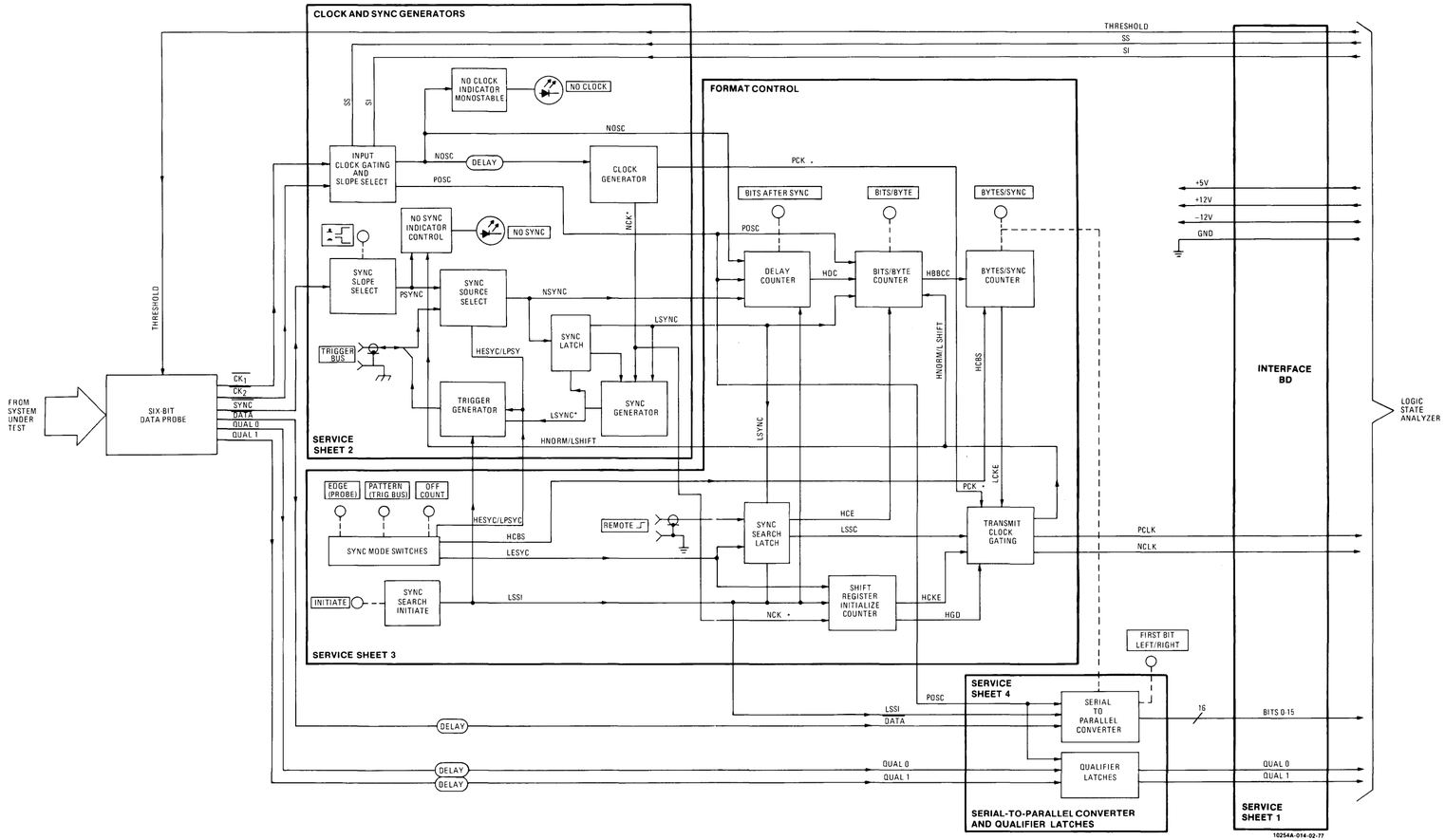


Figure 12.
Model 10254A Block Diagram
Page 17

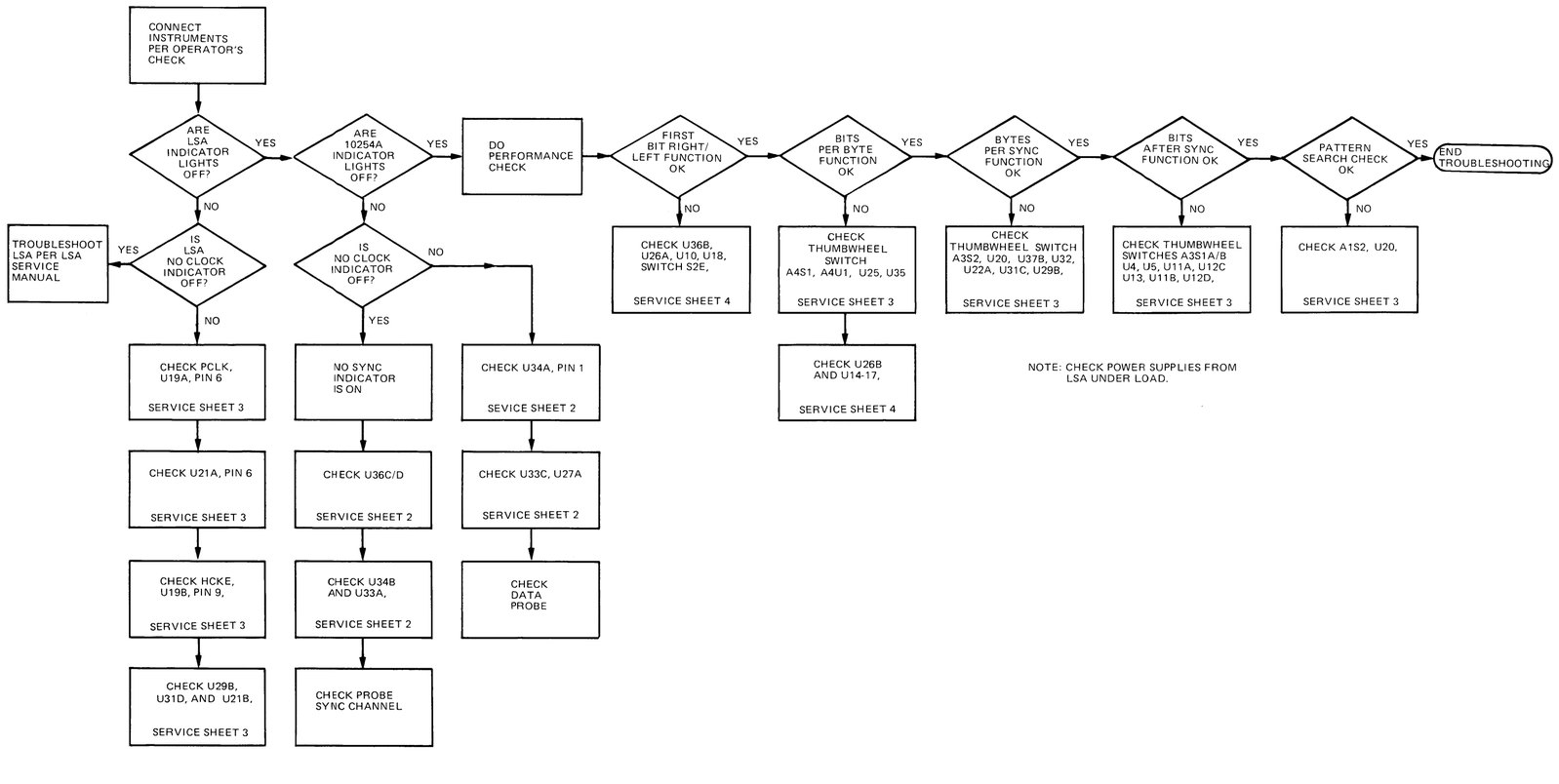


Figure 13. 10254A Troubleshooting Tree

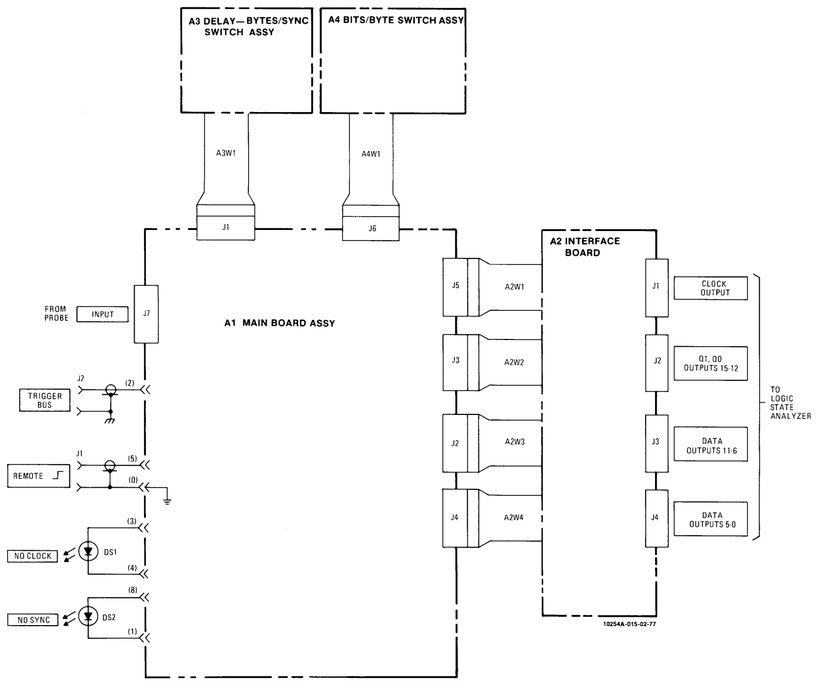


Figure 14. Model 10254A Interconnection Diagram

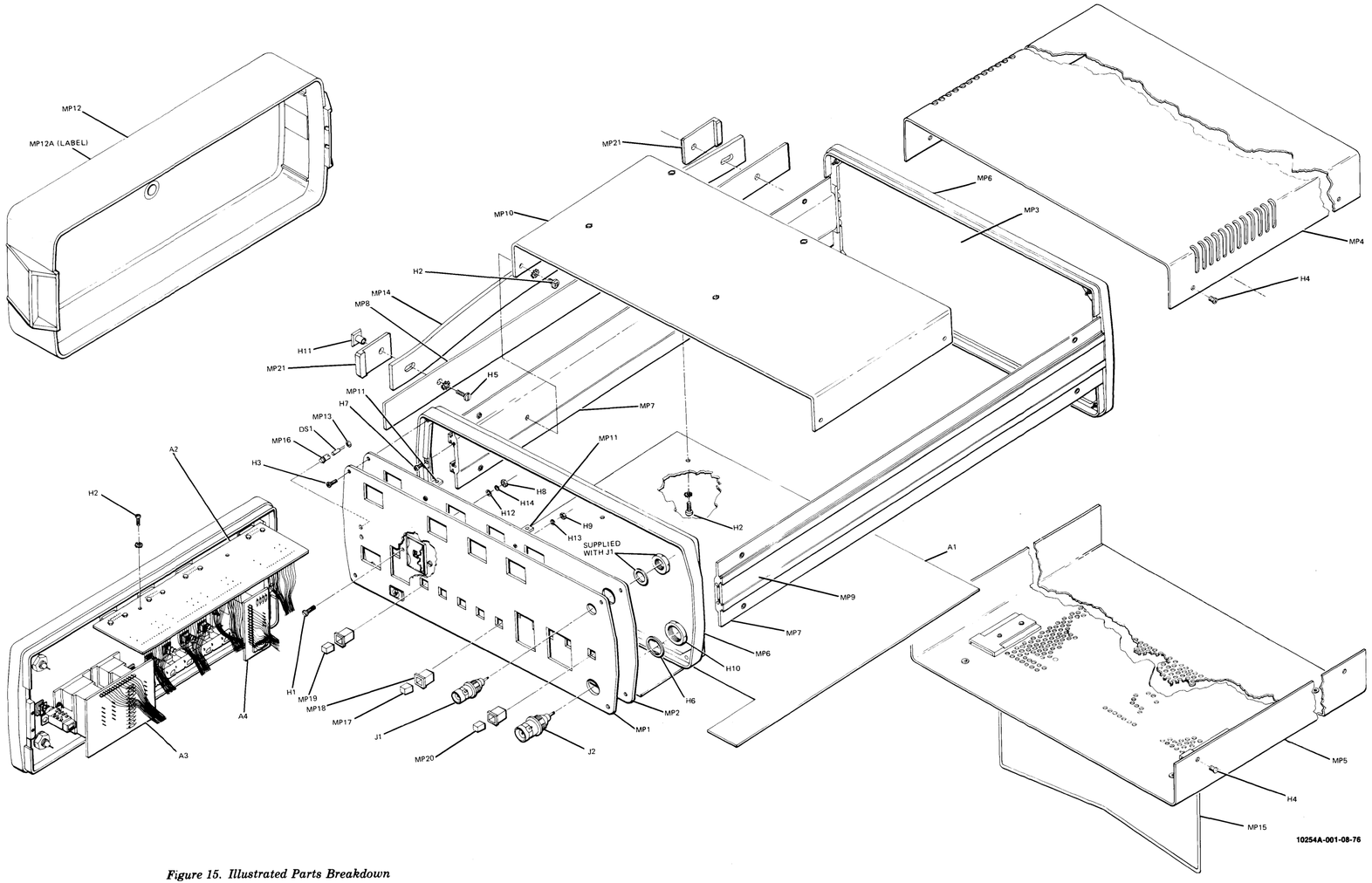


Figure 15. Illustrated Parts Breakdown

Table 7. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	10254-66501	1	BOARD ASSEMBLY, MAIN	28480	10254-66501
A2	10254-66502	1	BOARD ASSEMBLY, INTERFACE	28480	10254-66502
A3	10254-66503	1	BOARD ASSEMBLY, BITS AFTER SYNC, BYTES/SYNC	28480	10254-66503
A4	10254-66504	1	BOARD ASSEMBLY, BITS/BYTE	28480	10254-66504
DS1	1990-0486	2	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
DS2	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
H1	0520-0168	4	SCREW-MACH 2-56 .5-IN-LG 82 DEG	28480	0520-0168
H2	2200-0103	14	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	28480	2200-0103
H3	2200-0141	4	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	28480	2200-0141
H4	2200-0762	8	SCREW-MACH 4-40 .25-IN-LG TR-HD-POZI	28480	2200-0762
H5	2360-0113	2	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	28480	2360-0113
H6	0360-1632	1	TERMINAL-LUG-SLDR 3/8 SCR .375/.109 ID	79963	761-3/8
H7	0624-0279	8	SCREW-TPG 6-32 .75-IN-LG PAN-HD-POZI	28480	0624-0279
H8	0610-0001	4	NUT-HEX-DBL-CHAM 2-56-THD .062-THK	28480	0615-0002
H9	2260-0002	3	NUT-HEX-DBL-CHAM 4-40-THD .062-THK	28480	2260-0005
H10	2950-0043	1	NUT-HEX-DBL-CHAM 3/8-32-THD .094-THK	73743	2X 28200
H11	03580-24706	2	NUT-SPEC=6	28480	03580-24706
H12	3050-0098	4	WASHER-FL MTLC NO.=2 .094-IN-ID	80120	AN960 C2
H13	2190-0019	3	WASHER-LK HLCL NO.=6 .115-IN-ID	28480	2190-0019
H14	2190-0112	4	WASHER-LK HLCL NO.=2 .088-IN-ID	28480	2190-0112
H15	3050-0003	6	WASHER-FL NM NO.=6 .141-IN-ID .375-IN-OD	73734	1471
J1	1250-0659	1	CONNECTOR-RF TPS FEM SGL HOLE FR	28480	1250-0659
J2	1250-0083	1	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	24931	28JR-130-1
MP1	10254-00201	1	PANEL, FRONT	28480	10254-00201
MP2	10254-00202	1	PANEL, SUB	28480	10254-00202
MP3	10254-00203	1	PANEL, REAR	28480	10254-00203
MP4	01607-04101	1	COVER, TOP	28480	01607-04101
MP5	01607-04102	1	COVER, BOTTOM	28480	01607-04102
MP6	01620-20501	2	FRAME CASTING	28480	01620-20501
MP7	01607-23701	2	RAIL, SIDE	28480	01607-23701
MP8	01607-07201	1	TRIM, SIDE RAIL	28480	01607-07201
MP9	01607-07202	1	TRIM, SIDE RAIL	28480	01607-07202
MP10	10254-01201	1	BRACKET, CENTER	28480	10254-01201
MP11	10254-01202	3	BRACKET, ANGLE	28480	10254-01202
MP12	5040-0562	1	COVER, FRONT PANEL	28480	5040-0562
MP12A	7120-4184	1	LABEL, FRONT COVER	28480	7120-4184
MP13	00183-67701	2	BASE, PILOT LIGHT	28480	00183-67701
MP14	1440-0103	1	HANDLE; SPCL 12.5 L .12 THK	28480	1440-0103
MP15	1460-1451	1	TILT STAND 8.2 LG SST	28480	1460-1451
MP16	1450-0404	1	LENS CAP CLR-TL .125-DIA	28480	1450-0404
MP17	0370-0671	1	PUSHBUTTON, LEG BLU SQ	28480	0370-0671
MP18	0370-2626	6	BEZEL, PB GRAY	28480	0370-2626
MP19	0370-2630	4	PUSHBUTTON, WILLOW GRN SQ	28480	0370-2630
MP20	0370-2790	1	PUSHBUTTON, YEL GRN SQ	28480	0370-2790
MP21	5040-7042	2	CAP, PLASTIC	28480	5040-7042
MP22	7120-5922	1	LABEL, C PROBE	28480	7120-5922
MP23	7120-5923	1	LABLE, B PROBE	28480	7120-5923
W1	10254-61601	4	CABLE ASSEMBLY, INTERFACE	28480	10254-61601
W2	10254-61601		CABLE ASSEMBLY, INTERFACE	28480	10254-61601
W3	10254-61601		CABLE ASSEMBLY, INTERFACE	28480	10254-61601
W4	10254-61601		CABLE ASSEMBLY, INTERFACE	28480	10254-61601
W5	10236A	1	CABLE ASSEMBLY, TRIGGER BUS	28480	10236A

See introduction to this section for ordering information

Table 7. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	10254-66501		BOARD ASSEMBLY, MAIN	28480	10254-66501
A1C1	0140-0190	18	CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C2	0140-0190		CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C3	0140-0190		CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C4	0140-0190		CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C5	0140-0190		CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C6	0140-0190		CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C7	0160-3448	9	CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A1C8	0140-0190		CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C9	0140-0190		CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C10	0140-0190		CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C11	0140-0190		CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C12	0140-0190		CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C13	0140-0190		CAPACITOR-FXD 39PF +-5% 300VVDC MICA	72136	DM15E390J0300WV1CR
A1C14	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A1C15	0140-0204	7	CAPACITOR-FXD 47PF +-5% 500WVDC MICA	72136	DM15E470J0500WV1CR
A1C16	0140-0204		CAPACITOR-FXD 47PF +-5% 500WVDC MICA	72136	DM15E470J0500WV1CR
A1C17	0140-0204		CAPACITOR-FXD 47PF +-5% 500WVDC MICA	72136	DM15E470J0500WV1CR
A1C18	0140-0204		CAPACITOR-FXD 47PF +-5% 500WVDC MICA	72136	DM15E470J0500WV1CR
A1C19	0140-0204		CAPACITOR-FXD 47PF +-5% 500WVDC MICA	72136	DM15E470J0500WV1CR
A1C20	0140-0204		CAPACITOR-FXD 47PF +-5% 500WVDC MICA	72136	DM15E470J0500WV1CR
A1C21	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A1C22	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A1C23	0160-3443	2	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0160-3443
A1C24	0180-2255	27	C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C25	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C26	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C27	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C28	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C29	0160-3451	2	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C30	0160-0174	15	CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A1C31	0160-2204	1	CAPACITOR-FXD 100PF +-5% 300WVDC MICA	28480	0160-2204
A1C32	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C33	0160-3443		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0160-3443
A1C34	0160-3508	2	CAPACITOR-FXD 1UF +80-20% 50WVDC CER	28480	0160-3508
A1C35	0160-3451		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-3451
A1C36	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A1C37	0140-0204		CAPACITOR-FXD 47PF +-5% 500WVDC MICA	72136	DM15E470J0500WV1CR
A1C38	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C39	0160-3508		CAPACITOR-FXD 1UF +80-20% 50WVDC CER	28480	0160-3508
A1C40	0180-1746	3	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C41	0180-0159	1	CAPACITOR-FXD 220UF+-20% 10VDC TA	56289	150D227X0010B2
A1C42	0180-1746		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C43	0180-1746		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C44	0160-2250	2	CAPACITOR-FXD 5.1PF +-.25PF 500WVDC CER	28480	0160-2250
A1C45	0160-2250		CAPACITOR-FXD 5.1PF +-.25PF 500WVDC CER	28480	0160-2250
A1C46	0160-2253	1	CAPACITOR-FXD 6.8PF +-.25PF 500WVDC CER	28480	0160-2253
A1C47	0140-0190		CAPACITOR-FXD 39PF +-5% 300WVDC MICA	72136	DM15E390J0300WV1CR
A1C48	0140-0190		CAPACITOR-FXD 39PF +-5% 300WVDC MICA	72136	DM15E390J0300WV1CR
A1C49	0140-0190		CAPACITOR-FXD 39PF +-5% 300WVDC MICA	72136	DM15E390J0300WV1CR
A1C50	0140-0190		CAPACITOR-FXD 39PF +-5% 300WVDC MICA	72136	DM15E390J0300WV1CR
A1C51	0140-0190		CAPACITOR-FXD 39PF +-5% 300WVDC MICA	72136	DM15E390J0300WV1CR
A1C52	0140-0190		CAPACITOR-FXD 39PF +-5% 300WVDC MICA	72136	DM15E390J0300WV1CR
A1C53	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A1C54	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A1C55	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A1C56	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C57	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C58	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C59	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A1C60	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C61	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C62	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C63	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C64	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C65	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C66	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C67	0160-3448		CAPACITOR-FXD 1000PF +-10% 1000WVDC CER	28480	0160-3448
A1C68	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C69	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C70	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C

See introduction to this section for ordering information

Table 7. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1C71	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C72	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C73	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C74	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C75	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C76	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1C77	0180-2255		C1FXD TA ELECT 22 UF 20% 20VDCW	72982	301-000-C0M0-829C
A1CR1	1901-0040	3	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR2	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR3	1901-0535	1	DIODE-SCHOTTKY	28480	1901-0535
A1CR4	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1E1	0360-1653	7	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-1653
A1E2	0360-1653		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-1653
A1E3	0360-1653		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-1653
A1E4	0360-1653		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-1653
A1E5	0360-1653		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-1653
A1E6	0360-1653		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-1653
A1E7	0360-1653		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-1653
A1M1	0520-0137	10	SCREW-MACH 2-56 ,75-IN-LG PAN-HD-POZI	28480	0520-0137
A1M2	0610-0001	10	NUT-HEX-DBL-CHAM 2-56-THD ,062-THK	28480	0615-0002
A1M3	2190-0045	10	WASHER-LK HLCL NO.-2 ,088-IN-ID	28480	2190-0045
A1M4	3050-0098	10	WASHER-FL MTLC NO.-2 ,094-IN-ID	80120	AN960 C2
A1J1	1200-0768	6	SOCKET-IC 14-CONT DIP-SLDR	91506	314-AG5D-3R
A1J2	1200-0768		SOCKET-IC 14-CONT DIP-SLDR	91506	314-AG5D-3R
A1J3	1200-0768		SOCKET-IC 14-CONT DIP-SLDR	91506	314-AG5D-3R
A1J4	1200-0768		SOCKET-IC 14-CONT DIP-SLDR	91506	314-AG5D-3R
A1J5	1200-0768		SOCKET-IC 14-CONT DIP-SLDR	91506	314-AG5D-3R
A1J6	1200-0768		SOCKET-IC 14-CONT DIP-SLDR	91506	314-AG5D-3R
A1J7	1251-0699	5	CONNECTOR	28480	1251-0699
A1L1	9100-2254	18	COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L2	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L3	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L4	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L5	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L6	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L7	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L8	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L9	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L10	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L11	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L12	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L13	9100-2251	2	COIL-FXD MOLDED RF CHOKE ,22UH 10%	24226	10/220
A1L14	9100-2255	5	COIL-FXD MOLDED RF CHOKE ,47UH 10%	24226	10/470
A1L15	9100-2255		COIL-FXD MOLDED RF CHOKE ,47UH 10%	24226	10/470
A1L16	9100-2255		COIL-FXD MOLDED RF CHOKE ,47UH 10%	24226	10/470
A1L17	9100-2255		COIL-FXD MOLDED RF CHOKE ,47UH 10%	24226	10/470
A1L18	9100-2255		COIL-FXD MOLDED RF CHOKE ,47UH 10%	24226	10/470
A1L19	9100-2251		COIL-FXD MOLDED RF CHOKE ,22UH 10%	24226	10/220
A1L20	9100-2267	2	COIL-FXD MOLDED RF CHOKE 18UH 10%	24226	10/182
A1L21	9100-2267		COIL-FXD MOLDED RF CHOKE 18UH 10%	24226	10/182
A1L22	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L23	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L24	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L25	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L26	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1L27	9100-2254		COIL-FXD MOLDED RF CHOKE ,39UH 10%	24226	10/390
A1MP1	5040-7478	3	HOUSING, TOP	28480	5040-7478
A1MP2	5040-7478		HOUSING, TOP	28480	5040-7478
A1Q1	1854-0092	1	TRANSISTOR NPN SI PD=200MW FT=600MHZ	28480	1854-0092
A1Q2	1854-0009	1	TRANSISTOR NPN 2N709 SI TO-18 PD=300MW	28480	1854-0009
A1R1	0684-1011	8	RESISTOR 100 10% ,25W FC TC=-400/+500	01121	CB1011
A1R2	0684-1011		RESISTOR 100 10% ,25W FC TC=-400/+500	01121	CB1011
A1R3	0684-1011		RESISTOR 100 10% ,25W FC TC=-400/+500	01121	CB1011
A1R4	0684-1011		RESISTOR 100 10% ,25W FC TC=-400/+500	01121	CB1011
A1R5	0684-1031	22	RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R6	0698-3444	2	RESISTOR 316 1% ,125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A1R7	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R8	0684-1221	2	RESISTOR 1.2K 10% ,25W FC TC=-400/+700	01121	CB1221
A1R9	0684-3901	2	RESISTOR 39 10% ,25W FC TC=-400/+500	01121	CB3901
A1R10	0684-4721	2	RESISTOR 4.7K 10% ,25W FC TC=-400/+700	01121	CB4721
A1R11	0757-0434	1	RESISTOR 3.65K 1% ,125W F TC=0+-100	24546	C4-1/8-T0-3651-F
A1R12	0757-0426	1	RESISTOR 1.3K 1% ,125W F TC=0+-100	24546	C4-1/8-T0-1301-F
A1R13	0684-1541	2	RESISTOR 150K 10% ,25W FC TC=-800/+900	01121	CB1541
A1R14	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R15	0684-1811	2	RESISTOR 180 10% ,25W FC TC=-400/+600	01121	CB1811

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Table 7. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1R16	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R17	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R18	0757-0417	1	RESISTOR 562 1% ,125W F TC=0+-100	24546	C4-1/8-T0-562R-F
A1R19	0684-1011		RESISTOR 100 10% ,25W FC TC=-400/+500	01121	CB1011
A1R20	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R21	0698-3444		RESISTOR 316 1% ,125W F TC=0+-100	24546	C4-1/8-T0-316R-F
A1R22	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R23	0684-1221		RESISTOR 1.2K 10% ,25W FC TC=-400/+700	01121	CB1221
A1R24	0684-3901		RESISTOR 39 10% ,25W FC TC=-400/+500	01121	CB3901
A1R25	0684-1541		RESISTOR 150K 10% ,25W FC TC=-800/+900	01121	CB1541
A1R26	0684-1811		RESISTOR 180 10% ,25W FC TC=-400/+600	01121	CB1811
A1R27	0764-0033	1	RESISTOR 33 5% 2W MO TC=0+-200	11502	RG42
A1R28	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R29	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R30	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R31	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R32	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R33	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R34	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R35	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R36	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R37	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R38	0684-1021	4	RESISTOR 1K 10% ,25W FC TC=-400/+600	01121	CB1021
A1R39	0684-1011		RESISTOR 100 10% ,25W FC TC=-400/+500	01121	CB1011
A1R40	0684-1021		RESISTOR 1K 10% ,25W FC TC=-400/+600	01121	CB1021
A1R41	0684-4721		RESISTOR 4.7K 10% ,25W FC TC=-400/+700	01121	CB4721
A1R42	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R43	0684-1011		RESISTOR 100 10% ,25W FC TC=-400/+500	01121	CB1011
A1R44	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R45	0684-1021		RESISTOR 1K 10% ,25W FC TC=-400/+600	01121	CB1021
A1R46	0684-1021		RESISTOR 1K 10% ,25W FC TC=-400/+600	01121	CB1021
A1R47	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R48	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R49	0684-1001	1	RESISTOR 10 10% ,25W FC TC=-400/+500	01121	CB1001
A1R50	0684-1011		RESISTOR 100 10% ,25W FC TC=-400/+500	01121	CB1011
A1R51	0684-1031		RESISTOR 10K 10% ,25W FC TC=-400/+700	01121	CB1031
A1R52	0687-1011	1	RESISTOR 100 10% ,5W CC TC=0+529	01121	EB1011
A1S1	3101-1734	1	SWITCH ASSY	28480	3101-1734
A1S2	3101-2114	1	SWITCH-PB 5-STATION	28480	3101-2114
A1U1	1820-0683	4	IC-DIGITAL SN74804N TTL S HEX 1	01295	SN74804N
A1U2	1820-0683		IC-DIGITAL SN74804N TTL S HEX 1	01295	SN74804N
A1U3	1820-0683		IC-DIGITAL SN74804N TTL S HEX 1	01295	SN74804N
A1U4	1820-1426	2	IC-DIGITAL SN74LS145N TTL LS 4	01295	SN74LS145N
A1U5	1820-1426		IC-DIGITAL SN74LS145N TTL LS 4	01295	SN74LS145N
A1U6	1820-1304	4	IC-DIGITAL SN74S194N TTL S R=8	01295	SN74S194N
A1U7	1820-1304		IC-DIGITAL SN74S194N TTL S R=8	01295	SN74S194N
A1U8	1820-1304		IC-DIGITAL SN74S194N TTL S R=8	01295	SN74S194N
A1U9	1820-1304		IC-DIGITAL SN74S194N TTL S R=8	01295	SN74S194N
A1U10	1820-1197	4	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A1U11	1820-1204	1	IC-DIGITAL SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
A1U12	1820-0681	3	IC-DIGITAL SN74S00N TTL S QUAD 2 NAND	01295	SN74S00N
A1U13	1820-1212	2	IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN74LS112N
A1U14	1820-1470	4	IC-DIGITAL SN74LS157N TTL LS QUAD 2	01295	SN74LS157N
A1U15	1820-1470		IC-DIGITAL SN74LS157N TTL LS QUAD 2	01295	SN74LS157N
A1U16	1820-1470		IC-DIGITAL SN74LS157N TTL LS QUAD 2	01295	SN74LS157N
A1U17	1820-1470		IC-DIGITAL SN74LS157N TTL LS QUAD 2	01295	SN74LS157N
A1U18	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A1U19	1820-0697	1	IC-DIGITAL SN74S140N TTL S DUAL 4 NAND	01295	SN74S140N
A1U20	1820-1430	1	IC-DIGITAL SN74LS161N TTL LS BIN	01295	SN74LS161N
A1U21	1820-0629	2	IC-DIGITAL SN74S112N TTL S DUAL J-K	01295	SN74S112N
A1U22	1820-1112	1	IC-DIGITAL SN74L574N TTL LS DUAL	01295	SN74L574N
A1U23	1821-0002	1	IC CA3045 X8TR ARRAY	02735	CA3045
A1U24	1820-0629		IC-DIGITAL SN74S112N TTL S DUAL J-K	01295	SN74S112N
A1U25	1820-1278	1	IC-DIGITAL SN74LS191N TTL LS BIN	01295	SN74LS191N
A1U26	1820-1281	1	IC-DIGITAL SN74LS139N TTL LS DUAL 2	01295	SN74LS139N
A1U27	1820-0681		IC-DIGITAL SN74S00N TTL S QUAD 2 NAND	01295	SN74S00N
A1U28	1820-0693	1	IC-DIGITAL SN74S74N TTL S DUAL	01295	SN74S74N
A1U29	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A1U30	1820-1212		IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN74LS112N
A1U31	1820-0681		IC-DIGITAL SN74S00N TTL S QUAD 2 NAND	01295	SN74S00N
A1U32	1820-1158	1	IC-DIGITAL SN74S51N TTL S DUAL 2	01295	SN74S51N
A1U33	1820-0694	1	IC-DIGITAL SN74S86N TTL S QUAD 2 EXCL-OR	01295	SN74S86N
A1U34	1820-1423	1	IC-DIGITAL SN74LS123N TTL LS DUAL	01295	SN74LS123N
A1U35	1820-1453	1	IC-DIGITAL SN74S163N TTL S BIN	01295	SN74S163N

See introduction to this section for ordering information

Table 7. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1U36	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A1U37	1820-0686	1	IC-DIGITAL SN74S11N TTL S TPL 3 AND	01295	SN74S11N
A1U38	1820-0683		IC-DIGITAL SN74S04N TTL S HEX 1	01295	SN74S04N
A2	10254-66502	1	BOARD ASSEMBLY, INTERFACE	28480	10254-66502
A2C1	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C2	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C3	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C4	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C5	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C6	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C7	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C8	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C9	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C10	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C11	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C12	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2C13	0160-0174		CAPACITOR-FXD .47UF +80-20% 25WVDC CER	28480	0160-0174
A2H1	0520-0137		SCREW-MACH 2-56 .75-IN-LG PAN-HD-POZI	28480	0520-0137
A2H2	0610-0001		NUT-HEX-DBL-CHAM 2-56-THD .062-THK	28480	0615-0002
A2H3	2190-0045		WASHER-LK HLCL NO.-2 .088-IN-ID	28480	2190-0045
A2H4	3050-0098		WASHER-FL MTLC NO.-2 .094-IN-ID	80120	AN960 C2
A2J1	1251-0699		CONNECTOR	28480	1251-0699
A2J2	1251-0699		CONNECTOR	28480	1251-0699
A2J3	1251-0699		CONNECTOR	28480	1251-0699
A2J4	1251-0699		CONNECTOR	28480	1251-0699
A2MP1	5040-7478		HOUSING, TOP	28480	5040-7478
A2MP2	5040-7479	1	HOUSING, BOTTOM	28480	5040-7479
A2W1	8120-0621	6	CABLE ASSEMBLY, RIBBON	28480	8120-0621
A2W2	8120-0621		CABLE ASSEMBLY, RIBBON	28480	8120-0621
A2W3	8120-0621		CABLE ASSEMBLY, RIBBON	28480	8120-0621
A2W4	8120-0621		CABLE ASSEMBLY, RIBBON	28480	8120-0621
A3	10254-66503	1	BOARD ASSEMBLY, BITS AFTER SYNC, BYTES/SYNC	28480	10254-66503
A3R1	0684-1831	16	RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3R2	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3R3	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3R4	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3R5	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3R6	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3R7	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3R8	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3R9	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3R10	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3R11	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3R12	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A3S1	3100-3308	1	SWITCH, 2 SEC 10 POSITION THUMBWHEEL	28480	3100-3308
A3S2	3100-3391	2	SWITCH, 16 POSITION THUMBWHEEL	28480	3100-3391
A3W1	8120-0621		CABLE ASSEMBLY, RIBBON	28480	8120-0621
A4	10254-66504	1	BOARD ASSEMBLY, BITS/BYTE	28480	10254-66504
A4R1	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A4R2	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A4R3	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A4R4	0684-1831		RESISTOR 18K 10% .25W FC TC=-400/+800	01121	CB1831
A4S1	3100-3391		SWITCH, 16 POSITION THUMBWHEEL	28480	3100-3391
A4U1	1820-1199	1	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A4W1	8120-0621		CABLE ASSEMBLY, RIBBON	28480	8120-0621

See introduction to this section for ordering information

Table 8. List of Manufacturers' Codes

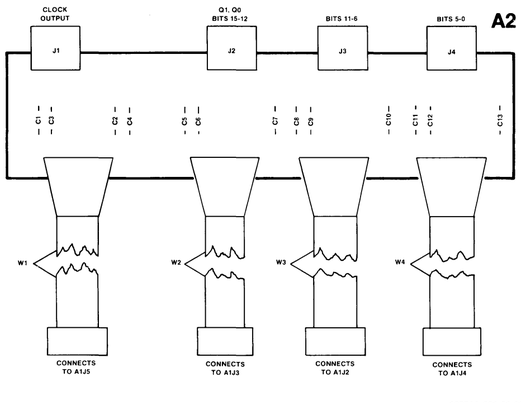
Mfr Code	Manufacturer Name	Address	Zip Code
01121	ALLEN-BRADLEY CO	MILWAUKEE WI	53212
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS TX	75231
02735	RCA CORP SOLID STATE DIV	SOMMERVILLE NJ	08876
11502	TRW INC BOONE DIV	BOONE NC	28607
24226	GOWANDA ELECTRONICS CORP	GOWANDA NY	14070
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
24931	SPECIALTY CONNECTOR CO INC	INDIANAPOLIS IN	46227
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC CT	06226
72982	ERIE TECHNOLOGICAL PRODUCTS INC	ERIE PA	16512
73734	FEDERAL SCREW PRODUCTS CO	CHICAGO IL	60618
73743	FISCHER SPECIAL MFG CO	CINCINNATI OH	45206
79963	ZIERICK MFG CO	MT KISCO NY	10549
80120	SCHNITZER ALLOY PRODUCTS CO	ELIZABETH NJ	07206
91506	AUGAT INC	ATTLEBORO MA	02703

SERVICE SHEET 1

PRINCIPLES OF OPERATION

Interface Board A2 provides interface connections between the 10254A and the LSA (Logic State Analyzer). The LSA provides threshold and clock slope select signals (SI and SS), and power supply voltages to the 10254A through the interface board. The 10254A provides the LSA with clock signals (NCLK and PCLK), two qualifier signals (QUAL 0 and QUAL 1), and up to 16 bits of parallel data (BIT 0 through BIT 15) through the interface board.

Capacitors C1 through C13 provide decoupling for the threshold signal and the +5 V, +12 V, -12 V power supplies.



Interface Board A2 Component Identification
(10254-66502)

NOTE: CONNECTORS A2J1-A2J4 CONSIST OF A CONNECTOR (HP PART NO. 1251-0699), AND TOP AND BOTTOM HOUSINGS (HP PART NOS. 5040-7478 AND 5040-7479).

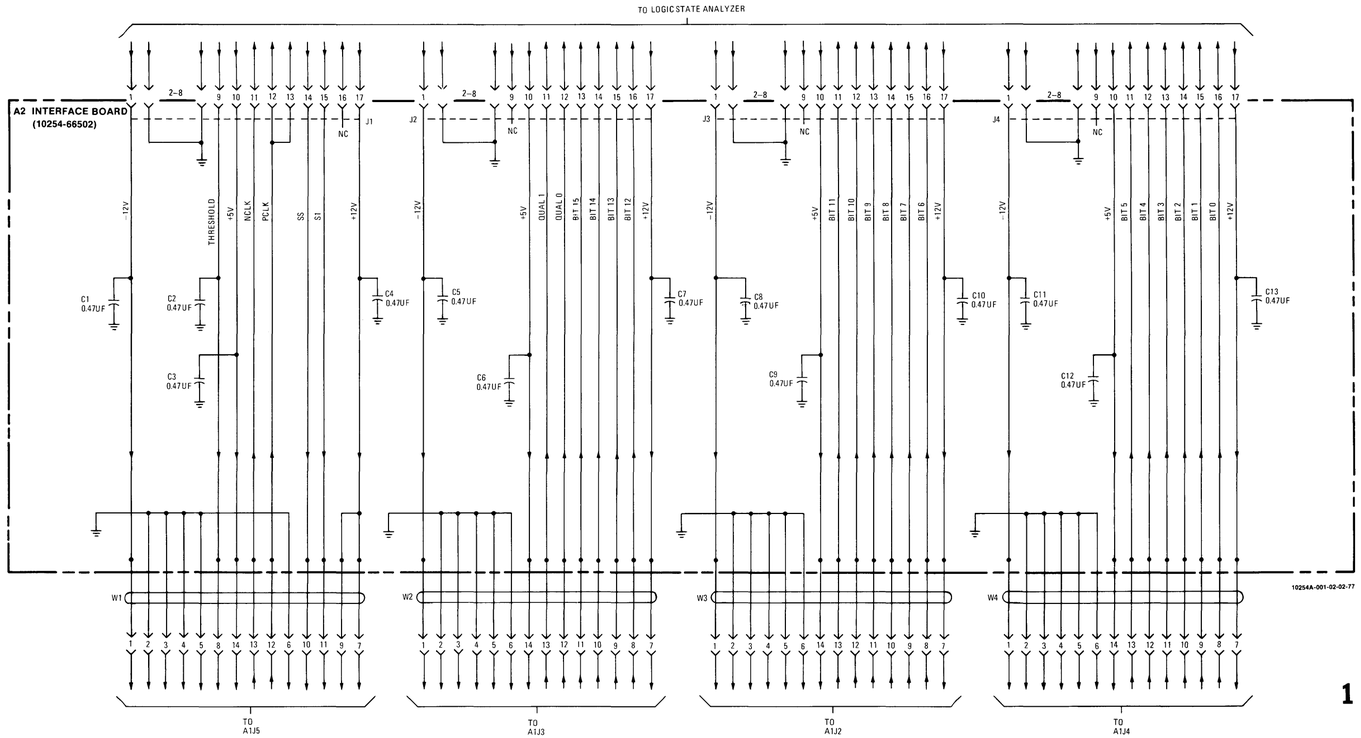


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Figure 16.
Service Sheet 1, Interface Baord A2

SERVICE SHEET 2

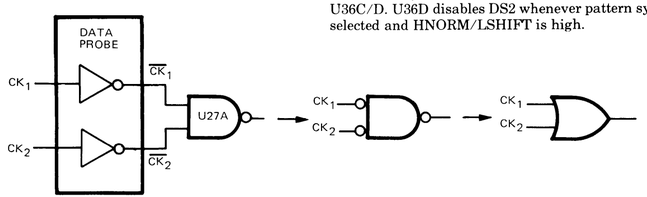
PRINCIPLES OF OPERATION

INPUT CLOCK GATING AND SLOPE SELECT. $\overline{CK}_1$ and $\overline{CK}_2$ from the data probe are routed to NAND gate U27A. U27A functions as an OR gate with respect to clock signals from the system under test (see figure below). U27A generates a positive-going pulse whenever $\overline{CK}_1$, $\overline{CK}_2$ or both go low. The output of U27A is combined with SS in XOR gate U33B and SI in XOR gate U33C. SS and SI are clock slope control signals from the logic state analyzer. SS is low when the logic analyzer CLOCK switch is set to ⌐ (positive edge transition), and high when the CLOCK switch is set to ¬ (negative edge transition). SI is the complement of SS. $\overline{CK}_1$ and $\overline{CK}_2$ are complements of the clock signals provided by the system under test.

If positive-edge clocking is selected (SS low), XOR U33B generates a positive-going edge (POSC) whenever a positive-going edge occurs at the output U27A. If negative-edge clocking is selected (SS high), XOR U33B generates POSC whenever a negative-going edge occurs at the output of U27A. POSC clocks qualifier latches U28A/B and shift registers U6-U9 (Service Sheet 4). POSC also clocks Bits/Byte Counter Counter U35, Bytes/Sync Counter U20, Delay Counter U4/U5, and U22A (Service Sheet 3).

XOR U33C functions in an opposite manner of U33B. It provides a negative-going transition (NOSC) at its output whenever the selected clock edge is detected by U27A. NOSC is routed to a one-shot multivibrator consisting of JK flip-flop U21A and transistor array U23A through a lumped-constant delay line consisting of C15 through C21, L13 through L18, and R3. The delay line provides a delay of 33 ns.

In addition to driving the one-shot, NOSC drives the NO CLOCK indicator circuit consisting of monostable U34A and LED DS1. If no clock signal occurs within 50 ms, the Q output of the monostable goes low, turning on NO CLOCK Indicator DS1.



Derivation of Clock Input OR Function

CLOCK GENERATOR. The clock generator provides two clock signals (NCK* and PCK*) used by the 10254A circuits. NOSC clocks U21A, generating a low level at Q output NCK* and a high level at $\overline{Q}$ output PCK*. When input NCK* to transistor array U23A goes low, its emitters ramp negative at a rate determined by the RC network tied to the emitters. The ramp continues until it reaches threshold voltage minus V_{be} of the second transistor in the pair. The threshold voltage is approximately 0.5 volt and is supplied by Q1. When the emitters reach threshold voltage minus V_{be}, the undriven transistor turns on. The collector of the undriven transistor then goes LO presetting JK flip-flop U21A.

As soon as the flip-flop is preset, NCK* goes HI, pulling the emitter up. When the emitters go up, the undriven transistor turns off and the clock generator waits for another clock signal from the system under test. The multivibrator provides a clock pulse 35 ns wide.

SYNC SLOPE SELECT. The probe sync signal $\overline{SYNC}$ is routed to XOR gate U33A. The second input to U33A comes from the sync edge select switch S2B. S2B determines whether U33A outputs a sync signal (PSYNC) to AOI gate U32 on the positive-going edge or negative-going edge of $\overline{SYNC}$.

SYNC SOURCE SELECT. AOI gate U32 selects the sync source that drives the sync generator. When edge sync is selected (HESYC=1), U32 gates the probe sync through to the sync generator. When pattern sync is selected (LPSYC=0), U32 gates the trigger bus input through to the sync generator.

SYNC LATCH AND GENERATOR. When a sync pulse is detected (NSYNC=0), the event is latched in JK flip-flop U24A. The next NOSC occurring after the sync pulse clocks the sync generator, providing LSYNC*. The sync generator consists of U24B and U23B and is identical to the clock generator in operation.

NO SYNC INDICATOR. In the edge (probe) sync mode, the NO SYNC indicator DS2 is turned on if no sync pulse occurs for 50 ms. The NO SYNC indicator is controlled by monostable U34B and NAND gates U36C/D. U36D disables DS2 whenever pattern sync is selected and HNORM/LSHIFT is high.

TRIGGER GENERATOR. In the edge sync mode (HESYC=1), the trigger generator provides a trigger for the logic state analyzer on the trigger bus every time a sync pulse is received from the system under test. When a sync pulse occurs, LSYNC* clears JK flip-flop U30A. The next NCK* clocks the $\overline{Q}$ output of U30B high. The circuit remains in this state until NCLK occurs. NCLK clocks the Q output of U30A high, generating a low level on the output of U31D. This turns off Q2, generating a trigger pulse (high level) on the trigger bus. The next NCK* after NCLK clocks the $\overline{Q}$ output of U30B low, turning off the trigger pulse. The circuit then waits for another LSYNC* and repeats the cycle described above. The trigger generator is disabled when pattern sync is selected (LPSYC=0).

IC'S ON SCHEMATIC 2

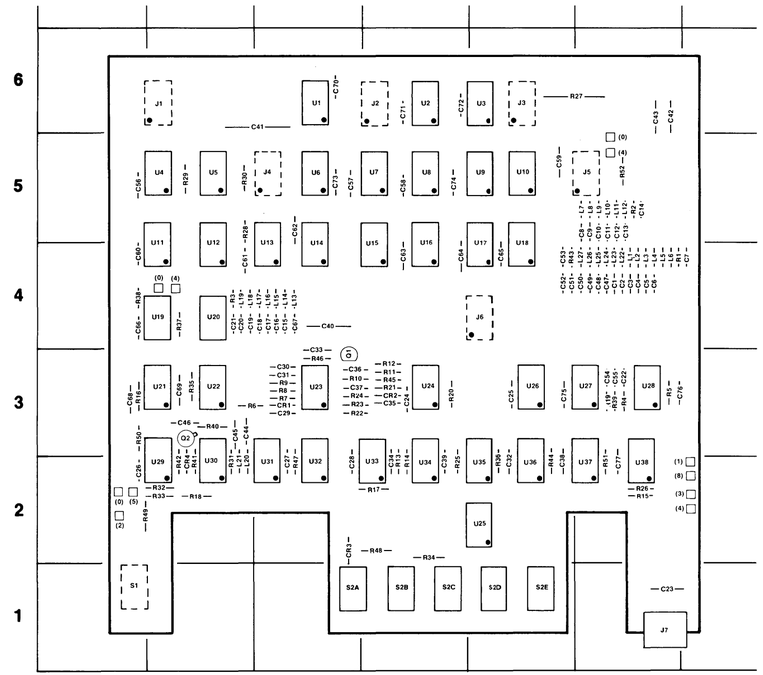
IC REF DES	HP PART NO.	MFR PART NO.
U21	1820-0629	74S112N
U23	1821-0002	CA3046
U24	1820-0629	74S112N
U27	1820-0681	74S00N
U30	1820-1212	74LS112N
U31	1820-0681	74S00N
U32	1820-1158	74S51N
U33	1820-0694	74S86N
U34	1820-1423	74LS123N
U36	1820-1197	74LS00N

U21/U24/U30 FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

U34A/B FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
H	L	↑	⌐	¬
H	↓	H	⌐	¬



Main Board A1 Component Identification (10254-66501)

10254A-002-01-02-77

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	F-4	C28	C-2	C55	F-3	J1	B-6	L21	B-2	R19	F-3	R45	D-3	U13	C-4
C2	F-4	C29	C-3	C56	A-5	J2	D-6	L22	F-4	R20	D-3	R46	C-3	U14	C-4
C3	F-4	C30	C-3	C57	C-5	J3	E-6	L23	F-4	R21	D-3	R47	C-2	U15	D-4
C4	F-4	C31	C-3	C58	D-5	J4	C-5	L24	F-4	R22	C-3	R48	D-2	U16	D-4
C5	F-4	C32	C-2	C59	E-5	J5	F-5	L25	F-4	R23	C-3	R49	B-2	U17	E-4
C6	F-4	C33	C-3	C60	A-4	J6	E-4	L26	F-4	R24	C-3	R50	A-3	U18	E-4
C7	F-4	C34	D-2	C61	D-4	J7	F-1	L27	F-4	R25	D-2	R51	F-2	U19	B-4
C8	F-5	C35	D-3	C62	C-5	L1	F-4	Q1	C-3	R26	F-2	R52	F-5	U20	B-4
C9	F-5	C36	C-3	C63	D-4	L2	F-4	Q2	B-3	R27	E-5	S1	A-1	U21	B-3
C10	F-5	C37	C-3	C64	D-4	L3	F-4	R1	F-4	R28	B-5	S2A	C-1	U22	B-3
C11	F-5	C38	E-2	C65	E-4	L4	F-4	R2	F-5	R29	B-5	S2B	D-1	U23	C-3
C12	F-5	C39	D-2	C66	A-4	L5	F-4	R3	B-4	R30	B-4	S2C	D-1	U24	D-3
C13	F-5	C40	C-4	C67	C-4	L6	F-4	R4	F-3	R31	B-2	S2D	E-1	U25	E-3
C14	F-5	C41	C-6	C68	A-3	L7	F-5	R5	F-3	R31	B-2	S2E	E-1	U26	E-3
C15	C-4	C42	F-6	C69	B-3	L8	F-5	R6	B-3	R33	B-2	U1	C-6	U27	F-3
C16	C-4	C43	F-6	C70	C-6	L9	F-5	R7	C-3	R34	D-2	U2	D-6	U28	F-3
C17	C-4	C44	B-3	C71	D-6	L10	F-5	R8	C-3	R35	B-3	U3	E-6	U29	B-2
C18	C-4	C45	B-3	C72	D-6	L11	F-5	R9	C-3	R36	E-2	U4	B-5	U30	B-2
C19	B-4	C46	B-3	C73	C-5	L12	F-5	R10	C-3	R37	B-5	U5	B-5	U31	C-2
C20	B-4	C47	F-4	C74	D-5	L13	C-4	R11	D-3	R38	A-4	U6	C-5	U32	C-2
C21	B-4	C48	F-4	C75	E-3	L14	C-4	R12	D-3	R39	F-3	U7	D-5	U33	D-2
C22	F-3	C49	F-3	C76	F-3	L15	C-4	R13	D-2	R40	B-3	U8	D-5	U34	D-2
C23	F-1	C50	F-4	C77	F-2	L16	C-4	R14	D-2	R41	B-2	U9	E-5	U35	E-2
C24	D-3	C51	E-4	CR1	C-3	L17	C-4	R15	F-2	R42	B-2	U10	E-5	U36	E-2
C25	E-3	C52	E-4	CR2	D-3	L18	B-4	R16	A-3	R43	E-4	U11	B-4	U37	F-2
C26	A-2	C53	E-4	CR3	C-2	L19	B-4	R17	F-3	R44	E-2	U12	B-4	U38	F-2
C27	C-2	C54	F-3	CR4	B-2	L20	B-2	R18	B-2						

P/O A1 MAIN BOARD (10254-66501)

INPUT CLOCK GATING AND SLOPE SELECT U27A/U33B, C

SYNC SLOPE SELECT S2B/U33A

SYNC SOURCE SELECT U32A/U33D

CLOCK GENERATOR U21A/U23A

SYNC GENERATOR U24B/U23B

SYNC LATCH U24A

NO CLOCK MONOSTABLE U34A

NO SYNC MONOSTABLE U34B

TRIGGER GENERATOR U30/U31D/Q2

NOTE: ALL SWITCHES ARE SHOWN IN OUT POSITION

NOTE: UNUSED PORTION OF U23

PARTS ON THIS SCHEMATIC

P/O A1	CHASSIS
C15-21, 28-31, 33-37, 39-46, 54, 55 CR1, 2, 4 P/O J2-5, 7 L13-21 Q1, 2 R3, 4, 6-19, 21-27, 31, 39, 40-42, 45, 46, 49 S2B U21, 23, 24, 27, 30-34, 36	DS1, 2 J2

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Figure 17.
Service Sheet 2, Clock and Sync Generators, P/O Main Board A1
Page 25

SERVICE SHEET 3

PRINCIPLES OF OPERATION

SYNC SEARCH INITIATE. The Sync Search Initiate circuit consists of INITIATE pushbutton S1 and debouncer U29C/D. Pressing S1 initializes the 10254A circuits and presets the Sync Search Latch so that it is waiting for a sync signal. In pattern sync mode (LESYC=1), Sync Search can also be initialized by a positive edge applied to the REMOTE input.

SYNC SEARCH LATCH. Sync Search Latch U21B controls the Bits/Byte and Bytes/Sync counters and Transmit Clock Gating. When a sync signal occurs, LSYNC clears U21B, driving LSSC and HCE to the true state. HCE releases three-input AND gate U37A allowing its output to go high. This enables the Bits/Byte and Bytes/Bit counters if HNORM/LSHIFT ($\overline{LSSC} \bullet \overline{HGD}$) is high.

SHIFT REGISTER INITIALIZATION COUNTER. In the pattern sync mode, binary counter U25 ensures that that shift registers in the serial-to-parallel converter are loaded with good data before clock signals are transmitted to the logic state analyzer. LSSI parallel loads U25 with the two's complement of the value set on BITS/BYTES thumbwheel A4S1. U25 then counts up until it reaches maximum count (HGD=1). HGD is inverted by U36A and applied to NAND gate U31B, gating HCKE high. HCKE enables the transmit Clock Gating. The second input to U31B is LESYC. LESYC holds HCKE high in the edge sync mode, overriding the Shift Register Initialization Counter.

DELAY GENERATOR. The delay generator consists of JK flip-flops U13A/B, decade counters U4 and U5, and some combinatorial logic. When a sync pulse is detected, the negative-going edge of NSYNC clocks the Q output of U31B high. On the next NOSC, the Q output of U31A goes high, parallel-load enabling the decade counters.

The counters are preset to the nines complement of the delay set on BITS AFTER SYNC thumbwheel A3S1. The counters then count POSC's until ten's decade counter U5 reaches a count of nine (1001 in BCD) and unit's decade counter reaches a count of eight (1000 in BCD). This represents a count of n-1 where n is the delay set on the thrmbwheels. The count of 98 is detected by 4 input NAND gate U11A. U11A applies a high level to the K input of JK flip-flop U13A through U12C. The next NOSC (Nth clock) clocks the Q output of U13A low, presetting the counters and forcing output HDC of NAND gate U12D high. When the BITS AFTER SYNC thumbwheels are set to zero, all four inputs to NAND gate U11B are high. This applies a low level to pin 13 of U12D, holding HDC high.

BITS/BYTE COUNTER. Bits/Byte counter U35 determines the length of bytes transmitted to the LSA. At the start of a data transmission sequence, LSYNC parallel loads binary counter U35 to the two's complement of the value set on the BITS/BYTE thumbwheel through three-input AND gate U37A. When HDC goes high, U35 counts POSC's. When U35 counts the selected number of bits/byte, HBBCC goes high, enabling BYTES/SYNC COUNTER U20 and the Transmit Clock Gating, and parallel loading the Bits/Byte counter with to the two's complement of the BITS/BYTE thumbwheel setting. This cycle repeats itself until the counter is disabled by HCE and HNORM/LSHIFT.

BYTES/SYNC COUNTER. Binary counter U20 determines the number of bytes transmitted to the LSA after each sync pulse when BYTES/SYNC OFF COUNT switch S2A is set to COUNT (HCBS=1). LSYNC pulses the PE input of the counter low, parallel loading the counter to the two's complement of the BYTES/SYNC thumbwheel setting. The counter then counts HBBCC's. When U20 reaches terminal count, i.e., U20 has the number of bytes selected on the BYTES/SYNC thumbwheel, the counter gates U32 low through 3-input AND gate U37B. The output of U32 is applied to D flip-flop U22A. The POSC clocks U22A, setting LBSCC low. LBSCC is gated with HBBCC in NAND gate U31C, forcing LCKE high. This disables Transmit Clock Gating until the next LSYNC pulse.

TRANSMIT CLOCK GATING. Transmit Clock Gating provides NCLK and PCLK used to clock the LSA. Transmit Clock Gating is controlled by HNORM/LSHIFT ($\overline{LSSC} \bullet \overline{HGD}$), HCKE, and LCKE. In the pattern sync mode, HCKE disables 4-input NAND gate U19A/B until the shift registers (Service Sheet 4) are filled with good data, i.e., one complete byte has been received from the system under test. When HCKE goes high U19A/B wait for the output of NAND gate U29B to go high. The inputs to U29B are HNORM/LSHIFT and LCKE. If HNORM/LSHIFT is low, PCLK and NCLK are generated on every PCK*. If HNORM/LSHIFT is high, PCLK and NCLK are generated only when LCKE is low.

U22A TRUTH TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

U13/U21B TRUTH TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

U25 COUNT SEQUENCE: CLOCK ⌐ • U/D └ • ENABLE └ • LOAD H = COUNTS UP

THUMBWHEEL CODED OUTPUTS

BYTES/SYNC A3S2, BITS/BYTE A4S1

THUMBWHEEL SETTING	OUTPUT* 8	4	2	1
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

*Output is two's complement of thumbwheel setting.

BITS AFTER SYNC A3S1A, B

THUMBWHEEL SETTING	OUTPUT** 8	4	2	1
0	1	0	0	1
1	1	0	0	0
2	0	1	1	1
3	0	1	1	0
4	0	1	0	1
5	0	1	0	0
6	0	0	1	1
7	0	0	1	0
8	0	0	0	1
9	0	0	0	0

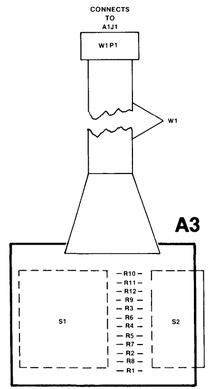
**Output is nine's complement of thumbwheel setting.

IC'S ON SCHEMATIC 3

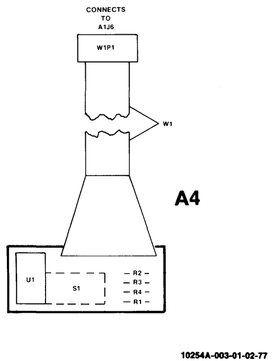
IC REF DEX	HP PART NUMBER	MFR PART NUMBER
U4	1820-1429	74LS160N
U5	1820-1429	74LS160N
U11	1820-1204	74LS20N
U12	1820-0681	74S00L
U13	1820-1212	74LS112N
U19	1820-0697	74S140N
U20	1820-1430	74LS161N
U21	1820-0629	74S112N
U22	1820-1112	74LS74N
U25	1820-1278	74LS191N
U29	1820-1197	74LS00N
U31	1820-0681	74S00N
U32	1820-1158	74S51N
U35	1820-1453	74S163N
U36	1820-1197	74LS00N
U37	1820-0686	74S11N
U38	1820-0683	74S04N

NOTE

See Service Sheet 2 for complete A1 Board Component Identifications.



Delay-Bytes/Sync Switch Board A3
Component Identification
(10254-66503)



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Bits/Byte Switch Board A4
Component Identification
(10254-66504)

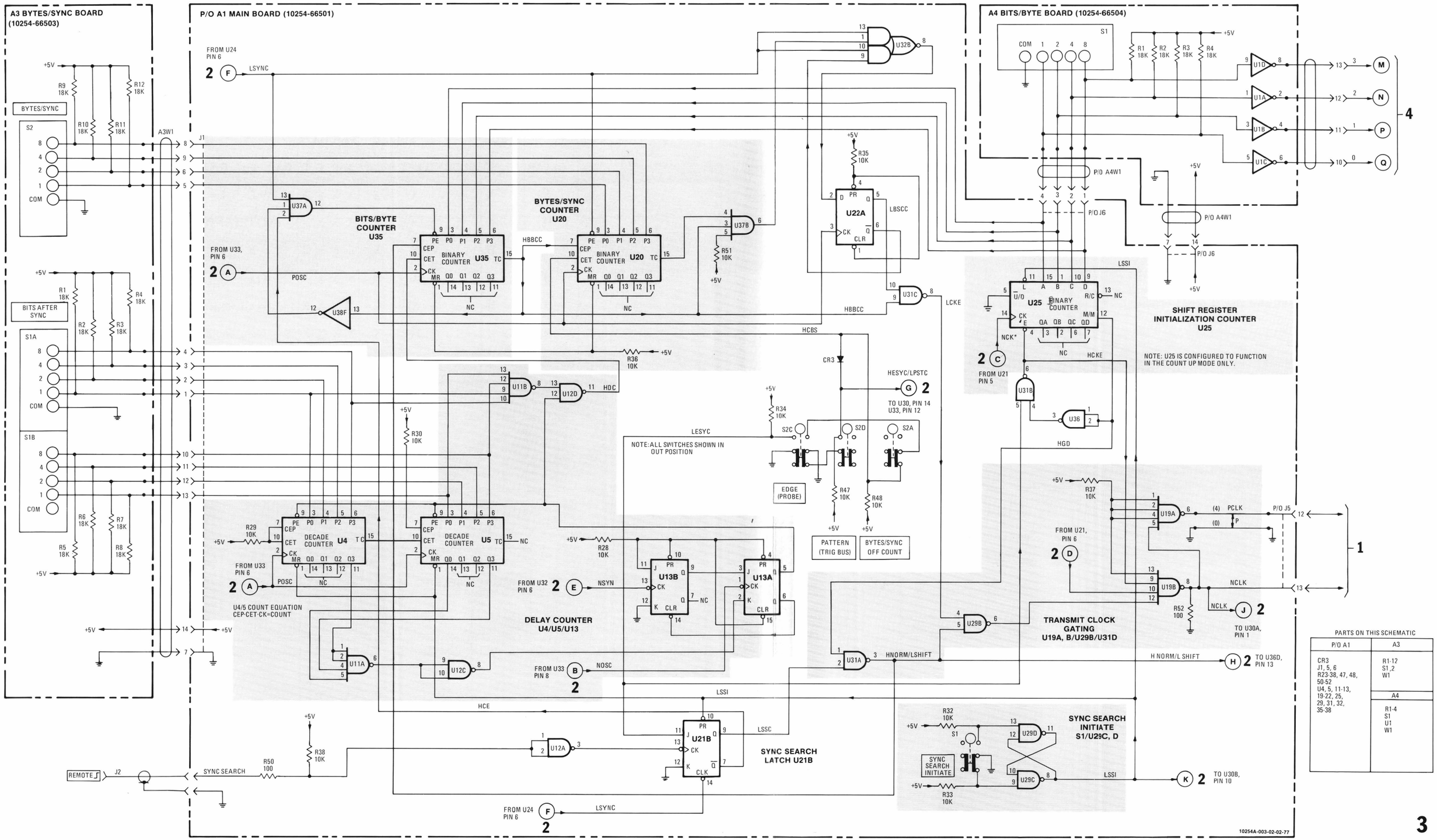

Figure 18. Service Sheet 3, Format Control, Bytes/Sync Bd A, Bits/Byte Bd A4, P/O Main Bd A1

SERVICE SHEET 4

PRINCIPLES OF OPERATION

SERIAL-TO-PARALLEL CONVERTER. The Serial-To-Parallel Converter converts serial data from the system under test to a parallel format for display on a LSA (Logic State Analyzer). The converter consists of decoders U26A/B, data selectors U14 through U17, and 4-bit bidirectional shift registers U6 through U9. The converter is designed to that output data can be formatted for first-bit right or first-bit left display with right justification.

The converter is controlled by FIRST BIT RIGHT/LEFT switch S2, NAND gate U36B, and the 4-bit code from BITS/BYTE Board A4 through decoders U26A/B and NAND gates U10 and U18. Serial data is routed through a lumped-constant delay line, buffered by inverter U38C, and applied to the A inputs of data selectors U14 through U17 and the R input of shift register U6.

In the first-bit left mode, all four shift registers are placed in the shift right operating mode (QA → QD). Note that the circuit is designed so that data is shifted left on the LSA display whenever the shift registers are in the shift-right mode. In the first-bit-left mode, U6 through U9 functions as a 16-bit shift-right shift register. $\overline{\text{DATA}}$ is applied to the R input (pin 2) of U6 and shifted right from QA to QD. The Bits/Byte counter divides the clock signal down and provides clocking signals (NCLK and PCLK) to the LSA when the selected number of bits have been shifted into the shift register. When less than 16 bits per byte are selected, the unused columns on the LSA can be blanked using the logic state analyzer COLUMN BLANKING control.

The Serial-To-Parallel Converter functions entirely different in the first-bit right mode. Assume that the BITS/BYTE switch is set to 16; lines 0 and 1 from the Bits/Byte board are then both high, setting the select line for U17 low and the select lines for U16 through U14 high. Thus U17 selects the A inputs (serial data from the probe) while U16 through U14 select the B inputs (feedback lines from the shift registers). Lines 2 and 3 from the Bits/Bytes board are also high, setting U9 to the parallel load mode and U8 through U6 to the shift-left mode

The first data bit from the probe is detected at pin 14 of U17, and routed to the D input of shift register U9. Since the shift register is in the parallel load mode, the next CK clocks the bit through to the QD output where it is routed around to the next MSB (C input) of U9. Thus the circuit is taking the Q_n output of the shift register and feeding it back to the P_{n-1} input through the data selector. The parallel-load shift register and data selector work as a synchronous load shift-left register. When the first bit reaches the QA output of U9, it is applied to the L input of U8. U8 and the subsequent shift registers function in the shift left mode. When all 16 bits are stored in the shift register, the bits/byte counter generates NCLK and PCLK, clocking the data to the logic analyzer.

If a 12 bit byte had been selected in the example above, the first bit would have been routed to the D input of U8. Regardless of selected byte length, the first shift register used is configured in the parallel-load mode and subsequent shift registers in the shift-left mode.

QUALIFIERS. Qualifier inputs QUAL 0 and QUAL 1 are applied to the 10254A through the data probe. The qualifier inputs are delayed 20 ns by lumped-constant delay lines and stored temporarily in "D" flip-flops U28A/B. QUAL 0 and QUAL 1 are then applied to the logic analyzer through Interface Board A2

U6-9 TRUTH TABLE

	INPUTS									OUTPUTS			
	MODE			SERIAL		PARALLEL							
CLEAR	S1	S0	CLOCK	LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	NO CHANGE			
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	NO CHANGE			

U14-17 TRUTH TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

U26 DECODER TRUTH TABLE

INPUTS			OUTPUTS			
ENABLE G	SELECT B	SELECT A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

IC'S ON SCHEMATIC 4

IC REF DES	HP PART NUMBER	MFR PART NO.
U1	1820-0683	74S04N
U2	1820-0683	74S04N
U3	1820-0683	74S04N
U6	1820-1304	74LS194N
U7	1820-1304	74LS194N
U8	1820-1304	74LS194N
U9	1820-1304	74LS194N
U10	1820-1197	74LS00N
U14	1820-1470	74LS157N
U15	1820-1470	74LS157N
U16	1820-1470	74LS157N
U17	1820-1470	74LS157N
U18	1820-1197	74LS00N
U26	1820-1281	74LS139N
U28	1820-0693	74LS74N
U36	1820-1197	74LS00N
U38	1820-0683	74S04N

NOTE

See Service Sheet 2 for complete A1 Board Component Identifications.

U26 LOGIC CLIP INDICATIONS

If U26 is functioning properly, monitoring the IC with a Model 10528A Logic Clip will yield the following indications.

BITS/BYTE THUMBWHEEL SETTING	LOGIC CLIP INDICATION* FIRST BIT LEFT MODE	LOGIC CLIP INDICATION* FIRST BIT RIGHT MODE
16	16 ●○●●●●●○ 1 ●●●●●●●○	16 ●○●●●●●○ 1 ○●●●●●○○
1	16 ●○○○○●●● 1 ●○○●●●●○	16 ●○○○○●●● 1 ○○○○●●●○
2	16 ●○●○●○●● 1 ●○○●●●●○	16 ●○●○●○●● 1 ○○○○●●●○
3	16 ●○○●●●○● 1 ●○○●●●●○	16 ●○○●●●○● 1 ○○○○●●●○
4	16 ●○●●●●●○ 1 ●○○●●●●○	16 ●○●●●●●○ 1 ○○○○●●●○
5	16 ○○○○○○○○ 1 ●●○●●●●○	16 ●○○○○●●● 1 ○●○●○●●○
6	16 ●○●○●○●● 1 ●●○●●●●○	16 ●○●○●○●● 1 ○●○●○●●○
7	16 ●○○●●●○● 1 ●●○●●●●○	16 ●○○●●●○● 1 ○●○●○●●○
8	16 ●○●●●●●○ 1 ●●○●●●●○	16 ●○●●●●●○ 1 ○●○●○●●○
9	16 ●○○○○●●● 1 ●○●●●●●○	16 ●○○○○●●● 1 ○○●●●○●○
10	16 ●○●○●○●● 1 ●○●●●●●○	16 ●○●○●○●● 1 ○○●●●○●○
11	16 ●○○●●●○● 1 ●○●●●●●○	16 ●○○●●●○● 1 ○○●●●○●○
12	16 ●○●●●●●○ 1 ●○●●●●●○	16 ●○●●●●●○ 1 ○○●●●○●○
13	16 ●○○○○●●● 1 ●●●●●●●○	16 ●○○○○●●● 1 ○●●●●●○○
14	16 ●○●○●○●● 1 ●●●●●●●○	16 ●○●○●○●● 1 ○●●●●●○○
15	16 ●○○●●●○● 1 ●●●●●●●○	16 ●○○●●●○● 1 ○●●●●●○○

* ● = LED ON

P/O A1 MAIN BOARD (10254-66501)

QUALIFIER LATCHES U28A/B

SERIAL-TO-PARALLEL CONVERTER

U6–U9 TRUTH TABLE

S1	S0	OPERATION
0	0	NO OPERATION
1	0	SHIFT L, QD ► QA
0	1	SHIFT R, QA ► QD
1	1	PARALLEL LOAD

PARTS ON THIS SCHEMATIC

P/O A1

C1-14, 47-53
P/O J2-4, 6, 7
L1-12, 22-27
R5, 43, 44
S2E
U1-3, 6-10, 14-18, 26, 28, 36, 38

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Figure 19. Service Sheet 4, Serial-To-Parallel Converter, P/O Main Bd A1

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