TELEVIDEO®
955 VIDEO DISPLAY TERMINAL
MAINTENANCE MANUAL

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TABLE OF CONTENTS

1.	Troubleshooting Guide	1-1
	Overview	1-1
	Description of the Modules	1-2
	Logic Board	1-2
	Power Supply	1-3
	Video Module (Video Monitor Board)	1-3
	Keyboard	1-3
	Removing the Modules	1-4
	Opening the Case	1-4
	Removing the Power Supply	1-6
	Replacing the Power Supply	1-6
	Removing the Video Module	1-8
	Replacing the Video Module	1-9
	Removing the Logic Board and Shroud	1-10
	Replacing the Logic Board and Shroud	1-10
	Closing the Case	1-11
	Opening the Keyboard Case	1-12
	Removing the Keyboard Circuit	1-12
	Visual Inspection	1-12
	Terminal and Keyboard Exterior	1-12
	Terminal and Keyboard Interior	1-13
	Fault Isolation at the Module Level	1-13
	Troubleshooting the Logic Board and Keyboard	1-17
	Troubleshooting the Video Module	1-22
	Visual Inspection	1-22
	Adjustments	1-22
2.	Schematics	2-1
3.	Ordering Spare Parts	3-1
	955 Terminal Spare Parts List	3-2
	955 Parts Reference List	3-5
4.	Theory of Operation	4-1
	Overview	4-1
	Gate Array Logic Board Theory of Operation	4-1
	Clock Circuit	4-1
	Clock Switching	4-3
	Clock Stretch Timing	4-4
	CPU System and Control	4-6
	Character Generation	4-9
	Display Generation	4-10
	Screen Data Storage	4-11
	Communications	4-12
	Enhanced Gate Array Logic Board Theory of Operation	4-13
	Clock Circuit	4-13
	CPU System and Control	4-15
	Character Generation	4-19
	Display Generation	4-20
	Screen Data Storage	4-21
	Communications	4-22

5. Service Information 5-1
Regional Sales Offices 5-1

6. Operator's Manual

7. Addenda
Specifications
Bulletins

LIST OF TABLES

1-1 Fault Isolation Guide 1-13
1-2 Gate Array Logic Board and Keyboard Troubleshooting Guide 1-17
1-3 Enhanced Gate Array Logic Board and Keyboard Troubleshooting Guide 1-20
2-1 IC Reference (Gate Array Logic Board) 2-1
2-2 IC Reference (Enhanced Gate Array Logic Board) 2-4
3-1 955 Terminal Spare Parts List 3-2
3-2 955 Parts Reference List 3-5
4-1 Memory Map 4-7
4-2 Memory Map 4-16

LIST OF FIGURES

1-1 955 Terminal, Front View 1-1
1-2 955 Terminal, Rear View 1-2
1-3 Discharging Voltages 1-4
1-4 Opening the Case 1-5
1-5 Removing the Power Supply 1-7
1-6 Removing the Video Module 1-9
1-7 Removing the Logic Board and Shroud 1-11
4-1 955 Block Diagram (Gate Array Logic Board) 4-2
4-2 Clock Switching 4-4
4-3 CPU Clock Stretch Timing 4-5
4-4 955 Block Diagram (Enhanced Gate Array Logic Board) 4-14

TROUBLESHOOTING GUIDE

This troubleshooting guide was designed for qualified repair personnel. Using this guide, the schematics in Section 2, and an Operator's Manual, you can repair most failures quickly. If difficulty arises, contact your dealer.

STOP! Do not open the case as described in this manual unless you are a qualified service technician. The components exposed during this procedure retain hazardous voltages that are present even after the power cord has been disconnected.

OVERVIEW

TeleVideo's 955, a general-purpose ASCII terminal, is fully code-compatible with our 925/950 family of terminals. The main element in the system is a 65C02 CMOS custom microprocessor. For CRT control, the 955 uses an advanced alphanumeric VLSI CRT controller chip.

Figures 1-1 and 1-2 show front and rear views of the terminal. Ports, switches and connectors are marked.

Figure 1-1
955 Terminal, Front View

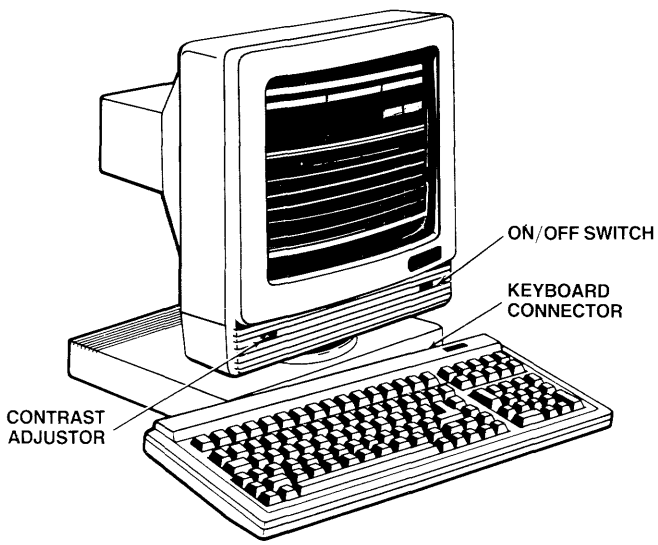
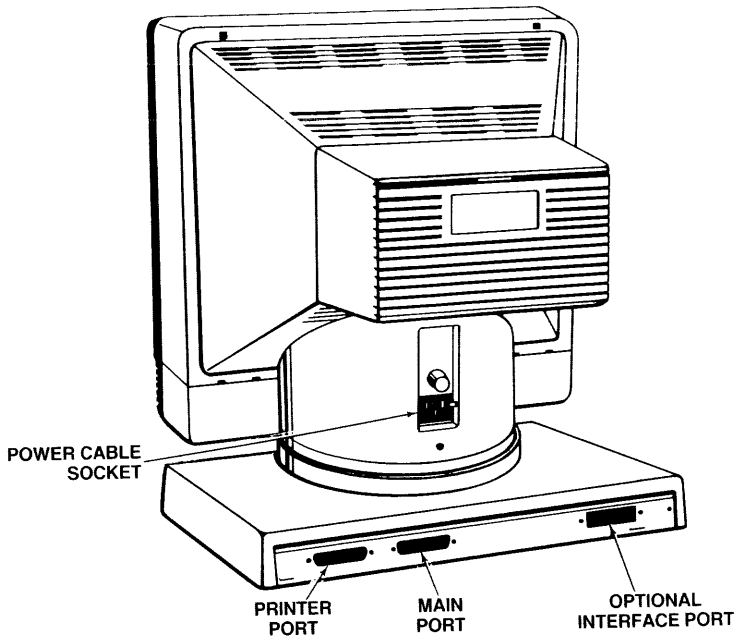


Figure 1-2
955 Terminal, Rear View



Terminal hardware is divided into four main modules:

Main logic board

Power supply

Video module (video monitor board)

Keyboard

This design permits fast fault isolation and keeps repair time to a minimum. To isolate a faulty module, swap a suspected module with a known-good one.

DESCRIPTION OF THE MODULES

Logic Board

The logic board fits inside a tray that slides into the base of the terminal. It is easily reached by removing two screws from the base.

The 65C02 microprocessor-based control circuitry on the logic board, acting on its own internal system program, stores and processes data received and data to be transmitted. The circuitry also generates the video and sync signals needed to display data on the screen.

The logic board has four distinct interconnected divisions that are discussed in this manual's Theory of Operation section. They are:

Main processor

Display circuitry-processor

Random Access Memory (RAM)

Interface for external input/output

Power Supply

A switching power supply is located in the pedestal below the CRT. It provides the following voltages for the terminal's electronic circuitry:

+ 5V for TTL logic

+12V for the video signals and RS-232C communications

-12V for RS-232C communications

- 5V for the optional modem

Two user-replaceable fuses--F1 on the power supply and a line fuse in back of the terminal--protect the circuitry.

Video Module (Video Monitor Board)

The video module is located behind the CRT. It contains horizontal and vertical sweep and video amplification circuitry. This circuitry produces a television-type noninterlaced raster display. The video signals generated by the display circuitry cause pixels to appear at designated positions across scan lines. These pixels form a character when selectively combined in a 7 x 9 dot matrix.

Keyboard

The 955 has a detachable keyboard connected to the terminal by a coiled keyboard cable.

The keyboard consists of an array of keyswitches mounted on a printed circuit board with an 8049 microcomputer and other IC's.

The 8049 microprocessor on the keyboard scans the keyboard matrix, encodes the data and transmits two bytes per character requested. Data is sent through a 6-wire coiled cable over an asynchronous serial channel at 9600 baud to the main logic board.

The keyboard microprocessor also activates an audio transducer for the bell and the simulated keyclick.

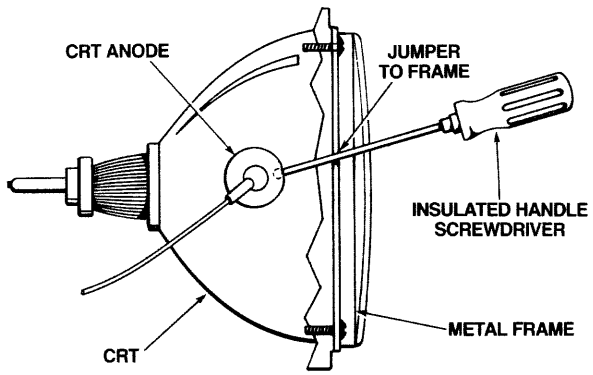
On the main logic board, the serial data is converted to parallel data and decoded by the main microprocessor and its firmware.

REMOVING THE MODULES

Opening the Case

STOP! The CRT and capacitors retain high voltages even after power has been turned off. As soon as you open the case, discharge the CRT by connecting one end of a grounding lead to the metal chassis and the other end to a screwdriver with an insulated handle. Slip the metal end of the screwdriver under the plastic cap of the anode, as shown in Figure 1-3. Be careful not to touch the metal portion of the screwdriver or the ground lead.

Figure 1-3
Discharging Voltages



Use Figure 1-4 as reference for opening the case.

1. Turn off the terminal.

2. Disconnect the power cord and data cable(s) from the back of the terminal; disconnect the keyboard cable from the front of the terminal.

3. Turn the terminal so the screen faces away from you.

4. Remove the three screws securing the monitor rear housing to the case (remove the screw under the power cord first, then remove the two screws near the top of the housing).

   NOTE: Remove the screws completely. If necessary, tip the unit backwards slightly.

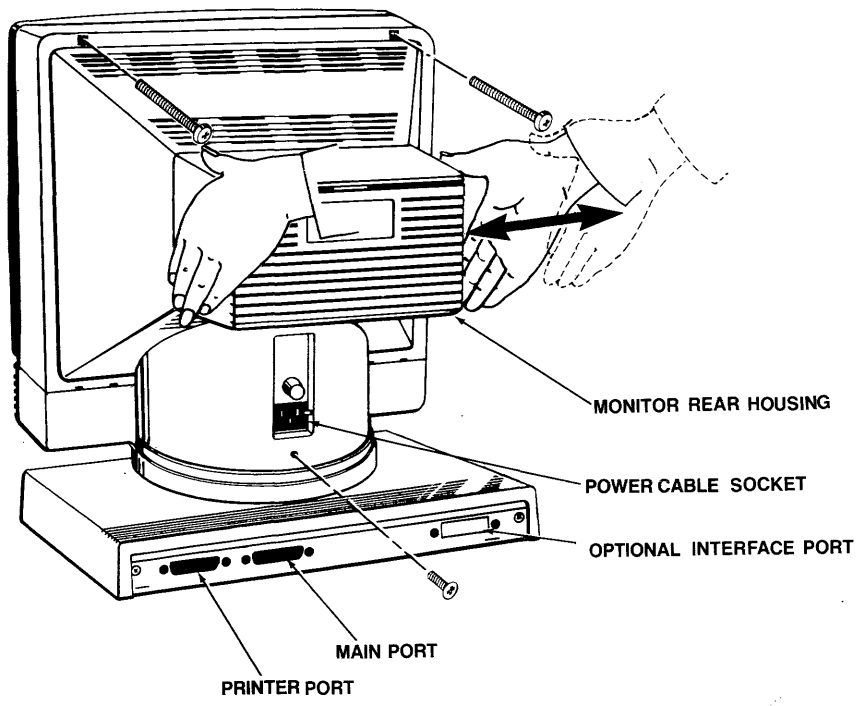
5. To release the clamp holding the bezel and monitor rear housing together (See Figure 1-4):

   a. Grasp the housing with your left hand.

   b. Sharply tap the right side of the housing with the heel of your right hand.

6. Lift off the monitor rear housing.

Figure 1-4
Opening the Case



Removing the Power Supply

STOP! The CRT retains high voltages, even after the power has been turned off, and poses a potential shock hazard. Follow the CRT discharge procedure on page 1-4 of this section before removing and replacing the power supply.

Use Figure 1-5 as reference for removing and replacing the power supply.

1. Turn off the terminal and open the case (See page 1-4).

2. Turn the terminal so the screen faces away from you.

3. Remove the two Phillips screws securing the bezel to the case (the screws are located inside the case, one on each side of the power supply).

4. Disconnect the Ground connector, the power connector (P4) and the DC connectors (P1, P2 and/or P3) from the power supply.

   NOTE: Only two connectors are attached at P1, P2 and P3. Pay close attention to the polarity for reference during reassembly.

5. Turn the unit so the screen faces you. Remove the two Phillips screws securing the power supply to the case.

6. Slide the power supply toward you to remove it from the case.

Replacing the Power Supply

1. Turn the unit so the screen faces you. Slide the power supply into the terminal until it locks into the plastic support bracket.

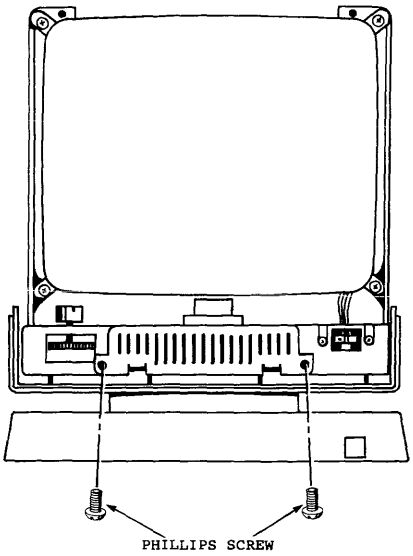
2. Reconnect the Ground connector, the power connector (P4) and the DC connectors (P1, P2 and P3).

   NOTE: Any of the three connectors may be used. For example, you may take the connectors off P1 and P2 and replace them on P2 and P3.

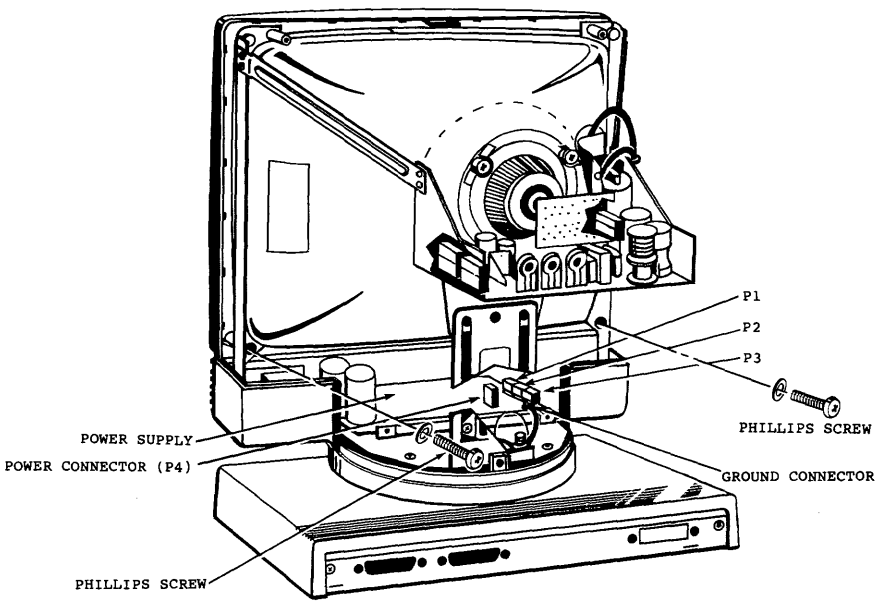
3. Insert and tighten the two Phillips screws securing the power supply to the case.

4. Replace the bezel and monitor rear housing and close the case (See page 1-11).

Figure 1-5
Removing the Power Supply



FRONT VIEW



BACK VIEW

Removing the Video Module

STOP! The CRT retains high voltages, even after the power has been turned off, and poses a potential shock hazard. Follow the CRT discharge procedure on page 1-4 of this section before removing and replacing the video module.

Use Figure 1-6 as reference for removing and replacing the video module.

1. Turn off the terminal and open the case (See page 1-4).

2. Turn the unit so the screen faces away from you.

3. Disconnect the voltage lead at the anode by gently lifting the rubber cap and unhinging the metal lead.

4. Carefully remove the CRT connector (small PC board at the back of the CRT).

5. Remove the power connector (red), the video connector (white) and the yoke connector (blue) from the video board.

6. **NOTE:** In some 955 terminals the video module is on a base that slides up and down; in others, the video module is on a hinged base.

   To determine which model you are working on, check below the video module. If there are three screws below the module, go on to the next step. If not, go to step 9.

7. Remove the two Phillips screws (one on each upper support bracket) holding the video module in place.

8. Remove the middle screw below the module and **loosen** the screw on each side of it. This allows the video module to slide down.

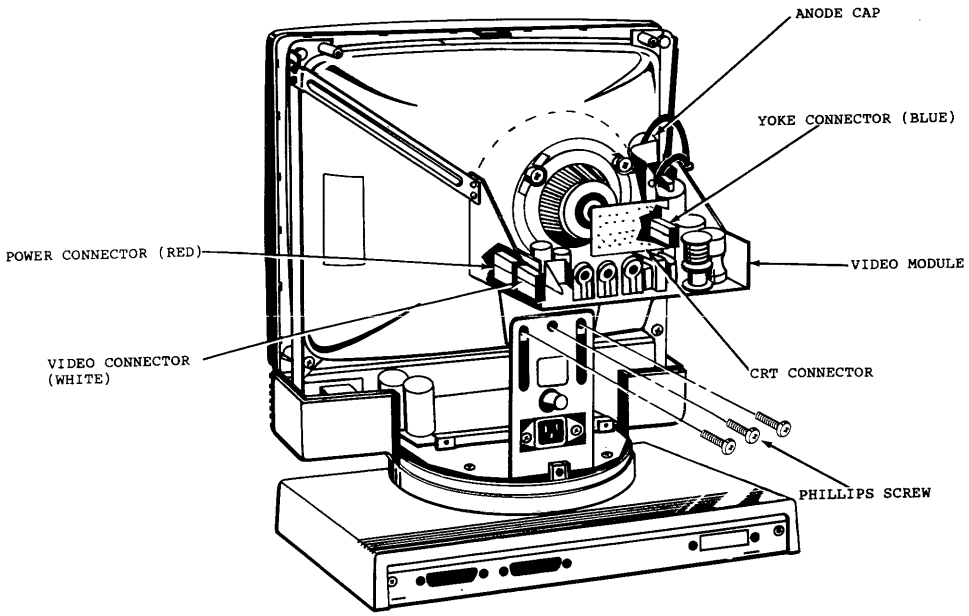
9. If the model you are working on is hinged, you must remove four screws.

   a. Remove the screw on each side of the plate holding the video module in place.

   b. Remove the two screws (one below the other) on the right side plate.

10. Remove the four Phillips screws holding the video board to its base; slide the board out of the terminal.

Figure 1-6
Removing the Video Module



Replacing the Video Module

1. Turn the terminal so the screen faces away from you.

2. Slide the video module onto its base (See Figure 1-6) until the four screw holes in the board line up with the four screw holes in the base.

3. Insert and tighten the four Phillips screws holding the video module to its base.

4. Reconnect the power connector (red), the video connector (white) and the yoke connector (blue) on the video module.

5. Carefully replace the CRT connector (small PCB at the back of the CRT).

6. Replace the anode cap:

   a. Pull back the rubber portion of the anode cap, exposing the metal leads.

b. Pinch the two leads together and insert them into the opening for the anode cap in the CRT. Release the leads.

c. Secure the rubber portion of the anode cap.

7. Insert and tighten the Phillips screws securing the module to the case. See step 6 (Removing the Video Module) if you are replacing the sliding module. See step 9 if you are replacing the hinged module.

8. Replace the bezel (if removed) and monitor rear housing; close the case (See page 1-11).

Removing the Logic Board and Shroud

Use Figure 1-7 as reference for removing and replacing the logic board and shroud.

1. Turn off the terminal. Disconnect the power cord and data cable(s) from the back of the terminal; disconnect the keyboard cable from the front of the terminal.

2. Rotate the complete unit so the back faces you. Remove the two Phillips screws (in the base) holding the logic board tray in place.

3. Grasp the logic board tray by its center tab; pull the tray toward you. Disconnect the red (P5) and white (P2) logic board connectors to slide the tray completely out of the terminal.

4. Remove the four brass screws securing the shroud to the logic board; remove the six Phillips screws securing the logic board to the tray.

5. Lift the logic board out of the tray.

Replacing the Logic Board and Shroud

1. Align the six screw holes in the logic board with the screw holes in the tray.

2. Loosely mount the six Phillips screws holding the logic board in place; insert and tighten the four brass screws holding the shroud to the logic board, then tighten the six Phillips screws securing the logic board.

3. Replace the logic board tray in the base:

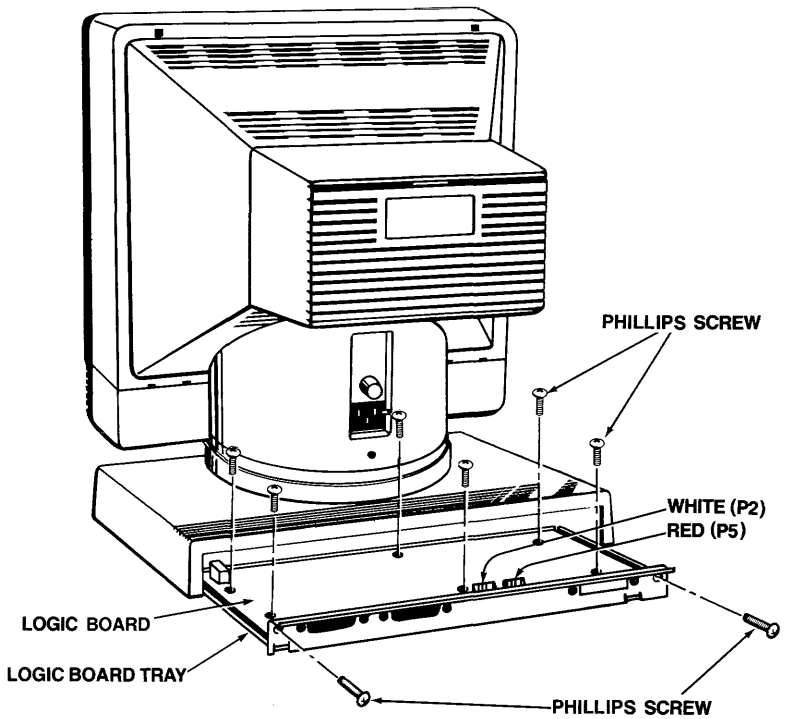
   a. Fit the metal flanges on the logic board tray into the guides at the back of the terminal. Hold the connector cables up so they do not interfere as you replace the tray.

b. Reattach the red connector (P5) and the white connector (P2) on the logic board.

c. Align the keyboard connector with the opening in the front of the terminal.

4. Insert and tighten the two Phillips screws holding the logic board tray in the base.

Figure 1-7
Removing the Logic Board and Shroud



Closing the Case

1. Replace the bezel:

a. Place the bezel face down in front of the terminal. Raise the bezel slightly and hook its two bottom tabs into the openings (one under the contrast adjustor; one under the ON/OFF switch) in the lower case.

b. Swing the bezel up to frame the screen, matching the ON/OFF switch and contrast adjustor with the openings in the bezel.

c. Carefully turn the screen away from you while holding the bezel in place. Insert and tighten the two Phillips screws securing the bezel to the case (these screws are located inside the case, on on each side of the power supply).

2. Replace the monitor rear housing:

   a. Position the monitor rear housing on the case, as shown in Figure 1-4.

   b. Align the screw hole under the power cord with the lower screw hole in the housing.

   c. Fit the four tabs in the housing over the edge of the lower case.

   d. Fit the tab in the top of the bezel into the slot in the top of the monitor rear housing. Squeeze the bezel and housing together.

   e. Insert and tighten the Phillips screw under the power cord and the two Phillips screws near the top of the housing.

Opening the Keyboard Case

1. Disconnect the coiled keyboard cable from the front of the terminal.

2. Turn the keyboard upside down and remove the six Phillips screws.

3. Turn the keyboard rightside up and remove the top cover.

Removing the Keyboard Circuit

1. Remove the four Phillips screws securing the keyboard circuit.

2. Lift the entire assembly out of the keyboard case.

VISUAL INSPECTION

A thorough visual inspection often makes the difference between success and failure in a repair attempt. Often a problem can be located just by close visual examination.

Terminal and Keyboard Exterior

Look for signs of accidental damage, abuse, or neglect. Keyboard failures are often caused by spilled liquids, sprayed cleaning solvents, staples, or paperclips.

Are there any dents or deep scratches on the exterior of the terminal or keyboard? If so, ask the user how and when the damage occurred. It may contribute to the problem with the unit.

Terminal and Keyboard Interior

Open the cases and inspect the keyboard and terminal interiors.

Keyboard: Check for signs of spilled liquids, foreign objects, unplugged devices, defective traces, and signs of overheating and burning. Check the telephone-style connectors (located on the back of the keyboard case and on the front of the terminal).

Wiring Harness: Check the condition of the wires and look for crushed insulation, exposed wires, and loose or broken connectors. Unplug the connectors and check that the pins are intact.

Logic Board: Check for loose chips, bent pins on chips, defective chip sockets, signs of overheating and burning, defective traces, and poor solder joints. Check that devices are properly installed.

Power Supply: Check for open fuses, defective components, and signs of overheating and burning.

Video Module: Check for defective components, signs of overheating, and defective traces.

Remove all defective modules for closer inspection and repair. When you finish the repairs, replace the module(s) and test them.

FAULT ISOLATION AT THE MODULE LEVEL

TeleVideo's modular terminal design makes isolating a problem to a particular module easy. You can either follow Table 1-1, Fault Isolation Guide, or replace each module in turn until the fault is corrected.

To use Table 1-1, find the description that resembles the problem in the terminal. Then, if applicable, refer to the troubleshooting guide for the suspected module.

Table 1-1
Fault Isolation Guide

Symptom	Suspected Module
No beep on power up	Logic board Line fuse Power supply Keyboard

Table 1-1 (Continued)
Fault Isolation Guide

Symptom	Suspected Module
No video, no cursor	Logic board Power supply Video module CRT
No external communication	Cable to host Logic board Power supply (-12V)
Incorrect characters	Logic board Keyboard
Incorrect attributes	Logic board
No keyboard communication	Logic board Keyboard cable
Fails to reset properly when CTRL RESET is pressed	Keyboard (See Service Bulletin number 65*
No baud-rate selection	Logic board
Power supply fuse blowing	Video module Power supply
Line fuse blowing	See Service Bulletin Number 63*
High-pitched whine	Video module
Distorted video	Video module Power supply Logic board
Characters missing dots	Logic board Defective CRT
Display too dim/can't adjust	Video module Power supply
Video fades	Check that video module has been modified as described in Service Bulletin Number 67*

*Section 7 (Addenda) contains Service Bulletins applicable to the 955 terminal.

Table 1-1 (Continued)
Fault Isolation Guide

Symptom	Suspected Module
Online communication problem	Logic board Cable to host Host
Garbled date, missing data, "P3ER" error message (revision C and D logic board only)	Logic Board (See Service Bulletin Number 64*)
False "P3ER" error when using main RS232 port (in block mode and half-duplex with pins 4 and 5 jumpered)	Logic board (See Service Bulletin Number 58*)
Jittery screen	Video module Hertz setting
Wavy screen	Video module Power supply External interference
Incorrect voltages	Power supply
No light at cathode filament	Video module Power supply Defective CRT
Display not equal to key entry	Logic board Keyboard cable Cable to host Host
Visible retrace scanlines	Brightness adjustment Video module Logic board
Keyboard locked up	Keyboard cable Keyboard Logic board Software command
Fails self test	Logic board Power supply (+5V) Keyboard
Some keys inoperative	Keyboard Logic board

*Section 7 (Addenda) contains Service Bulletins applicable to the 955 terminal.

Table 1-1 (Continued)
Fault Isolation Guide

Symptom	Suspected Module
Horizontal bar across screen	Logic board Video module
Poor linearity	Video module
Cursor moves, no characters	Logic board
Vertical line across screen	Logic board Video module Yoke
Crackling sound with distorted video	Video module

TROUBLESHOOTING THE LOGIC BOARD AND KEYBOARD

This section is a guide to component-level repair of the logic board and keyboard modules.

Determine the type of logic board in your terminal, then refer to Table 1-2 or Table 1-3 to locate the suspected defective component:

For Gate Array models (part number 132160-00 - Gate Array location U34), use Table 1-2.

For Enhanced Gate Array models (part number 132880-00 - Gate Array location U37), use Table 1-3.

NOTE: You can also determine the type of logic board by comparing the board to the illustrations in Section 2 of this manual.

If you are not sure that a component is satisfactory, replace it before proceeding to the next test point. Before replacing a chip or component, check its inputs and outputs for proper levels and signal quality.

Table 1-2
Gate Array Logic Board and Keyboard Troubleshooting Guide

Symptom	Component	Location	Page
Display/Video			
No display, no beep, fails self test	65C02	U1	2 of 6
	Gate Array	U34	4 of 6
	2674	U14	3 of 6
	Sys. Eprom	U4, U5	2 of 6
Distorted video	2674	U14	3 of 6
	2732	U45	4 of 6
	6116	U6	2 of 6
	74LS374	U33	4 of 6
	Gate Array	U34	4 of 6
Incorrect characters	2732	U45	4 of 6
	6551A	U9	6 of 6
	Gate Array	U34	4 of 6
	74LS374	U32	4 of 6
	6116	U6	2 of 6
	74AS194	U37, U42	4 of 6
	Sys. Eprom	U4, U5	2 of 6
	8049 (Kybd)	U2	KYBD

Table 1-2 (Continued)
Gate Array Logic Board and Keyboard Troubleshooting Guide

Symptom	Component	Location	Schematic Page
Display/Video			
Horizontal bar across screen	2674	U14	3 of 6
	Gate Array	U34	4 of 6
	74LS32	U43	3 of 6
	74LS08	U44	4 of 6
No vertical sync	2674	U14	3 of 6
	7406	U28	3 of 6
	Gate Array	U34	4 of 6
No cursor	2674	U14	3 of 6
	65C02	U1	2 of 6
Loss of attributes	2674	U14	3 of 6
	Gate Array	U34	4 of 6
	Sys. Eprom	U4, U5	2 of 6
	65C02	U1	2 of 6
Communications			
No full-duplex communication (FDX) at P3	6551A	U11	6 of 6
	1488	U3	6 of 6
	1489	U7	6 of 6
No full-duplex communication (FDX) at P4	6551A	U10	6 of 6
	1488	U3	6 of 6
	1489	U8	6 of 6
No status signal transmitted (DSR, DCD, CTS, DTR)	1488	U3, U12	6 of 6
	6551A	U11	6 of 6
No status signal received (DCD, CTS)	1489	U7, U8	6 of 6
	6551A	U11	6 of 6
Garbled data, missing data, "P3ER" error message (revision C and D logic board only)	See Service Bulletin Number 64*		
False "P3ER" error when using main RS232 port (in block mode and half-duplex with pins 4 and 5 jumpered)	See Service Bulletin Number 58*		

*Section 7 (Addenda) contains Service Bulletins applicable to the 955 terminal.

Table 1-2 (Continued)
Gate Array Logic Board and Keyboard Troubleshooting Guide

Symptom	Component	Location	Schematic Page
Keyboard			
All keys inoperative	6551A	U9	6 of 6
	74LS32	U23, U47	6 of 6
	Gate Array	U34	4 of 6
	8049 (Kybd)	U2	4 of 6
One or more row of keys inoperative	6551A	U9	6 of 6
	74LS32	U23, U47	6 of 6
One key inoperative	6551A	U9	6 of 6
	Keyswitch		
	8049 (Kybd)	U2	KYBD
	74LS145 (Kybd)	U3	KYBD
	74LS32	U23, U47	6 of 6
SHIFT, CTRL, ALPHA LOCK, and function keys inoperative	6551A	U9	6 of 6
	Sys Eprom	U4, U5	2 of 6
	74LS145 (Kybd)	U3	KYBD
No keyclick/no beep	Transducer (Kybd)		KYBD
	2N4401 (Kybd)	Q1	KYBD
	74LS32	U23	6 of 6
	6551A	U9	6 of 6
	8049 (Kybd)	U2	KYBD
Fails to reset properly when CTRL RESET is pressed	See Service Bulletin Number 65*		

*Section 7 (Addenda) contains Service Bulletins applicable to the 955 terminal.

Table 1-3
Enhanced Gate Array Logic Board and Keyboard Troubleshooting

Symptom	Component	Location	Page
Display/Video			
No display, no beep, fails self test	65C02	U4	2 of 5
	Gate Array	U37	4 of 5
	2674	U28	3 of 5
	Sys. Eprom	U14, U15	2 of 5
Distorted video	2674	U28	3 of 5
	2732	U46	4 of 5
	6116	U16	2 of 5
	74LS374	U33	4 of 5
	Gate Array	U37	4 of 5
Incorrect characters	2732	U46	4 of 5
	6551A	U20	5 of 5
	Gate Array	U37	4 of 5
	74LS374	U47	4 of 5
	6116	U16	2 of 5
	74F166	U38	4 of 5
	Sys. Eprom	U14, U15	2 of 5
	8049 (Kybd)	U2	KYBD
Horizontal bar across screen	2674	U28	3 of 5
	Gate Array	U37	4 of 5
	74LS32	U18	3 of 5
No vertical sync	2674	U28	3 of 5
	7406	U40	3 of 5
	Gate Array	U37	4 of 5
No cursor	2674	U28	3 of 5
	65C02	U4	2 of 5
Loss of attributes	2674	U28	3 of 5
	Gate Array	U37	4 of 5
	Sys. Eprom	U14, U15	2 of 5
	65C02	U4	2 of 5
Communications			
No full-duplex communication (FDX) at P3	6551A	U22	5 of 5
	1488	U17	5 of 5
	1489	U9	5 of 5
No full-duplex communication (FDX) at P4	6551A	U21	5 of 5
	1488	U17	5 of 5
	1489	U5	5 of 5

Table 1-3 (Continued)
Enhanced Gate Array Logic Board and Keyboard Troubleshooting

Symptom	Component	Location	Schematic Page
Communications			
No status signal transmitted (DSR, DCD, CTS, DTR)	1488	U13, U17	5 of 5
	6551A	U22	5 of 5
No status signal received (DCD, CTS)	1489	U5, U9	5 of 5
	6551A	U22	5 of 5
Keyboard			
All keys inoperative	6551A	U20	5 of 5
	74LS32	U11	5 of 5
	Gate Array	U37	4 of 5
	8049 (Kybd)	U2	KYBD
One or more row of keys inoperative	6551A	U20	5 of 5
	74LS32	U11	5 of 5
One key inoperative	6551A	U20	5 of 5
	Keyswitch		
	8049 (Kybd)	U2	KYBD
	74LS145 (Kybd)	U3	KYBD
	74LS32	U11	5 of 5
SHIFT, CTRL, ALPHA LOCK, and function keys inoperative	6551A	U20	5 of 5
	Sys Eprom	U14, U15	2 of 5
	74LS145 (Kybd)	U3	KYBD
No keyclick/no beep	Transducer (Kybd)		KYBD
	2N4401 (Kybd)	Q1	KYBD
	74LS32	U11	5 of 5
	6551A	U20	5 of 5
	8049 (Kybd)	U2	KYBD
Fails to reset properly when CTRL RESET is pressed	See Service Bulletin Number 65*		

*Section 7 (Addenda) contains Service Bulletins applicable to the 955 terminal.

TROUBLESHOOTING THE VIDEO MODULE

STOP! HIGH VOLTAGES ARE PRESENT ON THE VIDEO MODULE. USE EXTREME CARE DURING TROUBLESHOOTING.

Visual Inspection

Turn the terminal off and remove the monitor rear housing, as described in Section 1 of this manual (Removing the Modules). Check the following possible problem areas before removing the video module from the terminal.

a. Connectors: check for loose or damaged connectors, dirty contacts or bad crimps.

b. Wires: check for any broken, loose or frayed wires.

c. Components: check for any deformed, leaking or discolored components.

Correct any defects, then retest the terminal before continuing.

Remove the video module from the terminal, as described on page 1-8. Inspect the video module for:

a. Deformed, leaking, or discolored components.

b. Damaged components.

c. Cracked or lifted traces.

d. Poor solder joints (loose solder lumps, solder bridges, or cold solder joints).

Adjustments

Four adjustments can be made to the video module: height, linearity, brightness and focus (VR2). These controls are labeled on the video module. Use the following chart to determine the proper control to adjust.

Symptom	Control
Character intensity too bright or too dim	Brightness
Whole screen is too tall or too short	Height
Characters are not even in height from the top to the bottom of the screen	Linearity
Characters are not in focus	Focus

This section is a guide to component-level repair of the video module. When in doubt regarding the proper operation of a component, replace it before proceeding to the next test point. Before replacing a chip or component, check its inputs and outputs for proper levels and signal quality.

Symptom: No vertical deflection

1. Check IC-1 for vertical sync.

2. If the signal is improper or missing, trace back to P10 for vertical sync at pin 5.

3. If the signal is good, trace forward to IC-1, and related components up to the vertical yoke.

Symptom: No horizontal deflection

1. Check the base of Q301 for horizontal sync.

2. If the signal is improper or missing, trace back to P10 for horizontal sync at pin 1.

3. If the signal is good, check the output of the horizontal drive transformer T301 and the base of Q302. Trace for the presence of horizontal deflection through Q302, C306, L301, and L302 up to the horizontal yoke.

Symptom: Audible high-pitched whine

1. Check coils L301, L302, and flyback transformer.

Symptom: Video fades after a few minutes or after several hours.

Check that the video module has been modified as described in Service Bulletin Number 67*.

*Section 7 (Addenda) contains Service Bulletins applicable to the 955 terminal.

SCHEMATICS

This section contains schematics and silkscreens of the 955's major modules. For a brief description of the chip at each location on the logic board, determine the type of board in your terminal, then refer to Table 2-1 or Table 2-2.

For Gate Array models (part number 132160-00 - Gate Array location U34), use Table 2-1.

For Enhanced Gate Array models (part number 132880-00 - Gate Array location U37), use Table 2-2.

NOTE: You can also determine the type of logic board by comparing the board to the illustrations in Section 2 of this manual.

Refer to Section 3 of this manual for component part numbers.

Table 2-1
IC Reference (Gate Array Logic Board)

Location	Page	Type/Description
U1	2	MICROPROCESSOR 65C02 3MHZ
U2	2	74LS139 2X 1 OF 4 DECODER
U3	6	75188 4X LINE DRIVER
U4	2	SYSTEM EPROM 955
U5	2	SYSTEM EPROM 955
U6	2	2K x 8 CMOS STATIC RAM
U7	6	75189A 4X LINE RECEIVER
U8	6	75189A 4X LINE RECEIVER
U9	6	SY6551A/1 2MHZ SYN/AMI (KEYBOARD UART)
U10	6	SY6551A/1 2MHZ SYN/AMI (PRINTER UART)
U11	6	SY6551A/1 2MHZ SYN/AMI (HOST UART)
U12	6	75188 4X LINE DRIVER
U13	1,2,4	74LS00 4X 2-IN NAND GATE
U14	3	2674 ADVANCED VIDEO DISPLAY CONTROLLER (AVDC)
U15	2	74LS273 8X D-TYPE FLIP-FLOP

Table 2-1 (Continued)
IC Reference (Gate Array Logic Board)

Location	Page	Type/Description
U16	3	74LS157 4X 2-IN DATA SELECT MULTIPLEXER
U17	3	74LS157 4X 2-IN DATA SELECT MULTIPLEXER
U18	3	74LS245, N8T245N
U19	2,4	74HC04 HEX INVERTER
U20	3	74LS245, N8T245N
U21	3	74LS157 4X 2-IN DATA SELECT MULTIPLEXER
U22	3	74LS157 4X 2-IN DATA SELECT MULTIPLEXER
U23	2,5,6	74LS32 4X 2-IN OR GATE
U24	1,2,4,5	74LS02 4X 2-IN NOR GATE
U25	3	STATIC RAM 2K x 8 100ns.
U26	3	STATIC RAM 2K x 8 100ns.
U27	2	74LS32 4X 2-IN OR GATE
U28	1,2,3,4	7406 6X INVERTER BUFFER/DRIVER
U29	1	8211 PROG VOLTAGE REGULATOR
U30	3	STATIC RAM 2K x 8 100ns.
U31	3	STATIC RAM 2K x 8 100ns.
U32	4	74LS374 8X D-TYPE FLIP-FLOP
U33	4	74LS374 8X D-TYPE FLIP-FLOP
U34	4	GATE ARRAY TVI 16
U35	1,4	74LS374 8X D-TYPE FLIP-FLOP
U36	4	74AS194 4-BIT SHIFT REGISTER
U37	4	74AS194 4-BIT SHIFT REGISTER
U38	5	74LS74 2X D-TYPE E-TRIGGERED FLIP-FLOP
U39	5	74LS00 4X 2-IN NAND GATE

Table 2-1 (Continued)
IC Reference (Gate Array Logic Board)

Location	Page	Type/Description
U40	5	74AS163 SYNC 4-BIT COUNTER
U41	5	74S51 AND-OR INVERTER GATE
U42	4	74AS194 4-BIT SHIFT REGISTER
U43	3	74S32 4X 2-IN POS OR GATE
U44	3,4,6	74LS08 4X 2-IN AND GATE
U45	4	ROM 955 CHARACTER GENERATOR
U46	3	74LS32 4X 2-IN OR GATE
U47	1,6	74LS32 4X 2-IN OR GATE
U48	3,4,5	74S04 6X INVERTER

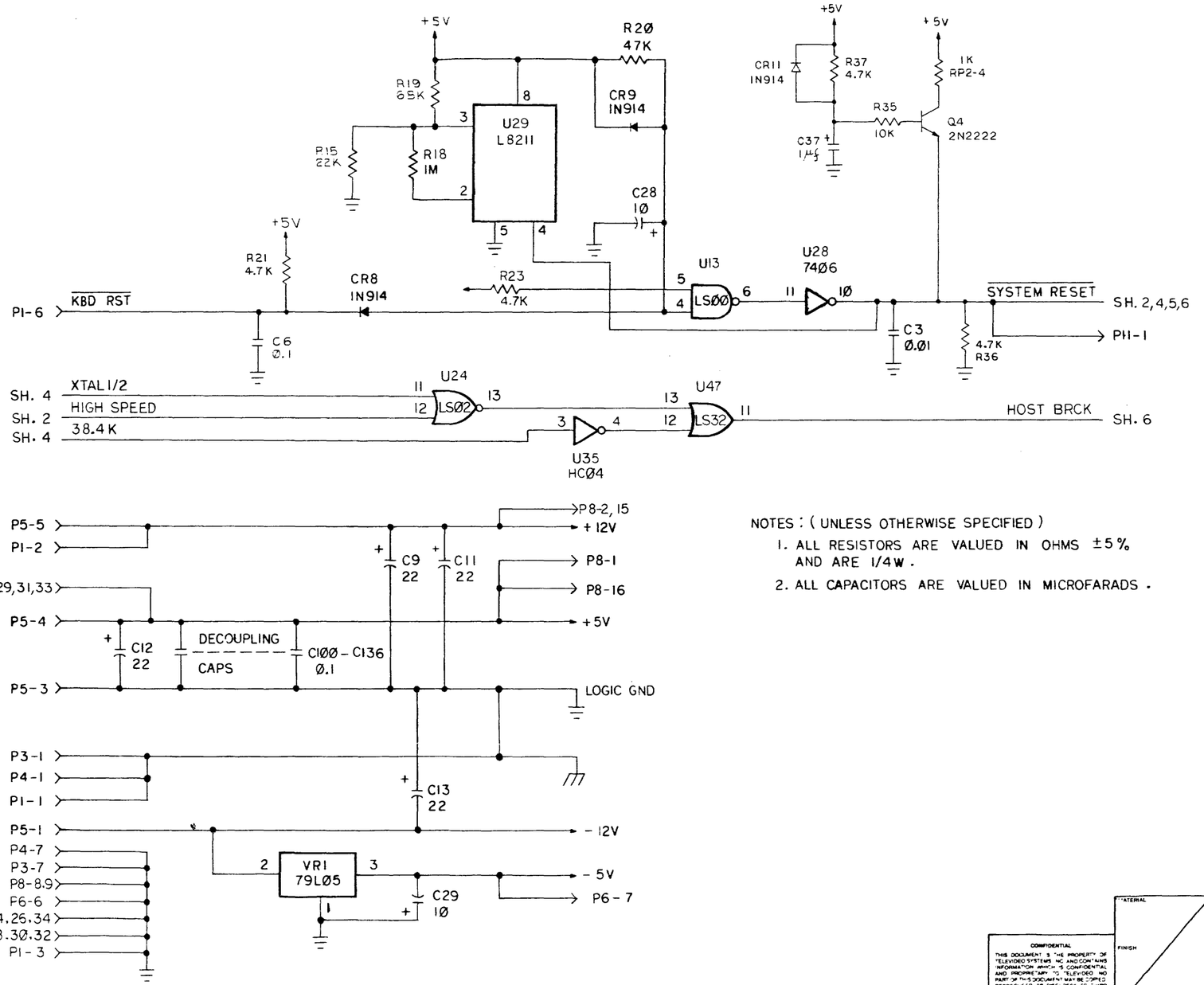
Table 2-2
IC Reference (Enhanced Gate Array Logic Board)

Location	Page	Type/Description
U2	1	8211 PROG VOLTAGE REGULATOR
U3	1,2	74LS132 4X 2-IN NAND SCHMITT
U4	2	65C02 MICROPROCESSOR 3 MHZ
U5	5	75189A 4X LINE RECEIVER
U7	1	7406 6X INVERTER BUFFER/DRIVER
U8	1,5	74LS08 4X 2-IN AND GATE
U9	5	75189A 4X LINE RECEIVER
U11	2,5	74LS32 4X 2-IN OR GATE
U13	5	75188 4X LINE DRIVER
U14	2	SYSTEM EPROM CO-FF
U15	2	CALCULATOR EPROM
U16	2	STATIC RAM 2K X 8 CMOS 150ns
U17	5	75188 4X LINE DRIVER
U18	3	74S32 4X 2-IN POS OR GATE
U19	2	74LS139 2X 1 OF 4 DECODER
U20	5	SY6551A/1 2 MHZ SYN/AMI (KYBD UART)
U21	5	SY6551A/1 2 MHZ SYN/AMI (PRINTER UART)
U22	5	SY6551A/1 2 MHZ SYN/AMI (HOST UART)
U23	1	74LS163 SYN 4-BIT COUNTER
U24	1,2,5	74LS32 4X 2-IN OR GATE
U25	3	74LS245, N8T245N 8X BUS TRANSCEIVER
U26	3	74LS157 4X 2-IN DATA SELECT MULTIPLEXER
U27	3	74LS157 4X 2-IN DATA SELECT MULTIPLEXER

Table 2-2 (Continued)
IC Reference (Enhanced Gate Array Logic Board)

Location	Page	Type/Description
U28	3	2674 ADVANCED VIDEO DISPLAY CONTROLLER (AVDC) 4 MHZ
U29	1,2,5	74HC04 HEX INVERTER
U30	3	74LS245, N8T245N 8X BUS TRANSCEIVER
U31	3	74LS157 4X 2-IN DATA SELECT MULTIPLEXER
U32	3	74LS157 4X 2-IN DATA SELECT MULTIPLEXER
U33	4	74LS374 8X D-TYPE FLIP-FLOP
U34	2	74LS32 4X 2-IN OR GATE
U36	3	STATIC RAM 8K X 8 100ns CMOS
U37	4	GATE ARRAY TSI-19
U38	4	74F166 8X SHIFT REGISTER
U39	2	74LS273 8X D-TYPE FLIP-FLOP
U40	3,4	7406 6X INVERTER BUFFER/DRIVER
U42	3,4	74LS08 4X 2-IN AND GATE
U43	3,5	74LS32 4X 2-IN OR GATE
U44	2,3,4	74LS04 6X INVERTER
U45	3	STATIC RAM 8K X 8 100ns CMOS
U46	4	CHARACTER GENERATOR
U47	4	74LS374 8X D-TYPE FLIP-FLOP
U48	3,4	74LS74 2X D-TYPE E-TRIGGERED FLIP-FLOP

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON	A	PROD RELEASE	266	1/14/85	
		B	REL REV B FAB PER ECO	2691T	3/4/85	
		C	REL REV C FAB SMALL BD	2820T	5/21/85	
		D	REV VALUES OF R16 & R17	2866T	5/22/85	



NOTES : (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4W .
2. ALL CAPACITORS ARE VALUED IN MICROFARADS .

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MATERIAL

FINISH

REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED

DIMENSION MM / INCH

X = ±

XX = ±

XXX = ±

ANGLES ±

CONTRACT NUMBER

DES		DATE
DR	D LY	DATE 11/17/84
CHK		DATE
ENGR		DATE

DESIGN ACTIVITY APPROVAL

CUSTOMER APPROVAL

TeleVideo Systems, Inc.

PCB SCHEMATIC DIAGRAM

955 CONTROL BOARD

SIZE	CODE IDENT		REV
D		132163-00	D

SCALE NONE SHEET 1 OF 6

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			

A0-15

+5V

U1 65C02

RP1(2) 4.7K

SH. 3 NMI
SH. 6 IRQ
SH. 1 SYSTEM RESET

C38 100PF

SH.5 Ø0

C31 47PF

R24 82

U2 LS139

U23 LS32

U28 7406

RP2(2) 1K

U19 HCØ4

A0-13 → SH. 3
A0 → P11-3
A1 → P11-5
A2 → P11-7
R/W → SH. 3,6
CRTC → SH. 3
CHAR RAM → SH. 3
ATT RAM → SH. 3
W11 → P11-4
COMM → SH. 5,6

U24 LSØ2
U13 LSØØ
CONT LATCH

U27 LS32
WR → P11-17
RD → P11-25
CRTC WR → SH. 3
Ø1 → SH. 4
Ø2 → SH. 6
CRTC RD → SH. 3
DØ-D7 → SH. 3,6

P11-10 DØ
P11-11 D1
P11-12 D2
P11-13 D3
P11-16 D4
P11-15 D5
P11-18 D6
P11-24 D7

U5 CO-DF 2764

U42 EO-FF 2764/27128

U4

RP1(3) 4.7K

W10

W9

W14

A13

A0-13

B1 3.2V

CR5 IN914

R29 680

CR3 IN914

C30 Ø.1

R14 1K

R17 10K

R12 1K

Q1 2N4264

Q2 2N4264

U6 6116LP4

R13 82

R16 4.7K

+12V

SYSTEM RESET → SH.1

RP1(4) 4.7

U15 LS273

DØ → DTR → SH. 6
D1 → HIGH SPEED → SH. 1,4
D2 → MODEM → SH. 6
D3 → 9
D4 → BOG/GOB → SH. 4
D5 → LINE/PAGE ATT → SH. 4
D6 → EMB/NONEMB → SH. 4
D7 → 80/132 → SH. 5
CK → 10

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DR DATE
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TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD
SIZE D | CODE IDENT | 32163-00 | REV C
SCALE NONE | SHEET 2 OF 6

8 7 6 5 4 3 2 1

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON		SEE SH 1			

A0'-A13'

CD0-CD7

AD0-AD7

U25 6116P-2 TC-5564 PL-10 — U30 6116P-2 TC-5564 PL-10 — U31 6116P-2 — U26 6116P-2

W8 W2 W1

R3

U28 7406

P11-23 VSYNC SH. 4

RP2(5) 1K VSYNC P2-5

SH. 2 D0 - D7
SH. 2 ATT RAM
SH. 2 CHAR RAM
SH. 5 QT
SH. 2 R/W
SH. 5 CCLK
SH. 2 CRTC RD
SH. 2 CRTC CE
SH. 2 CRTC WR
SH. 4 CURSOR
SH. 4 BLANK
SH. 2 NMI
SH. 2 A0 - A13

U14 SCN2674 AVDC

RP1(5) 4.7K

RP1(6) 4.7K

U46 LS32 — U44 LS08 — U43 S32 — U48 S04

U20 LS245 — U18 LS245

D0 - D7

A0'-A12'

U16 U17 U21 U22 LS157

R5 81

DADD0 DADD13

A0-A13

U43 S32

P2-1 HSYNCB

HSYNC SH. 4

DADD0-DADD13 SH. 4

P11-22

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PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD

SIZE	CODE IDENT		REV
D		132163-00	C
SCALE	NONE	SHEET 3 OF 6	

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			

SH. 3 AD0 - AD7
SH. 3 CD0 - CD7
SH. 5 CCLK
SH. 3 DADD0 - DADD13
SH. 3 BLANK
SH. 3 HSYNC
SH. 5 DCC
SH. 5 DOT CLK
SH. 3 CURSOR
SH. 3 VSYNC
SH. 2 HIGH SPEED
SH. 2 B0G / G0B
SH. 2 LINE / PAGE ATT
SH. 2 EMB / NONEMB
SH. 2 Ø1

U32 LS374 — U33 LS374 — U45 2732 — U28 7406 — U48 LS04 — U44 LS08 — U13 LS00 — U36 ASI94 / S194 — U37 ASI94 / S194 — U42 ASI94 / S194 — U35 LS374 — U24 LS02 — U28 7406 — RPI (7) 4.7K — RPI (8) 4.7K — RPI(9) 4.7K — RP2(7) 1K — RP2(6) 1K — R1 82 — R2 82 — R4 82 — R6 470 — R7 1K — R8 180 — R11 4.7 — C2 4.7 — CR6 — Q3 2N4264 — W12 — U19 HC04 — U12 HC04 — Y3 3.6864 — R27 47K — C5 0.001

P11-21
P2-3
P2-4
P11-20
DCC
SYSTEM RESET
SH. 5
SH. 1
+5V
-12V
38.4K
SH. 1
XTAL 1/2
SH 1,6

CUR= BLK
BLANK
DOT SER
RA0
RA2
RA3
BLINK CLK
DCC
DISPEN
CURSOR
H SYNC
V SYNC
SYS RESET
HALF INTENSITY
VIDEO
COMP VID
CHAD0
CHAD1
CHAD2
CHAD3
CHAD7
ATT
Ø2
BOW/WCB
LINE/PG ATT
910/925
ATT BNK INH 925/920
PG2
GND
SDR
40-7F
Ø2.W
DISPRAM
R/W
Ø1

MATERIAL
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TOLERANCES UNLESS NOTED
DIMENSION
ANGLES
CONTRACT NUMBER
DES — DATE
DR D LY — DATE 11/21/84
CHK — DATE
ENGR — DATE
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CUSTOMER APPROVAL

TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD
SIZE D | CODE IDENT | 132167-02 | REV L
SCALE NONE | SHEET 4 OF 6

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			

SH.2 $\overline{80}/132$

RP1 (10) 4.7K → +5V

U38 LS74

U39 LS00

U23 LS32

U41 LS51

U48 S04

+5V U41 S51 GND

DOT CLK SH. 4

Y1 19.3396 MHz

W13

R10 82

Y2 31.084 MHz

R9 82

U40 AS163

RP2 (3) 1K

DCC SH. 4

$\overline{DCC}$ SH. 4

$\overline{Q1}$ SH. 3

$\overline{CCLK}$ SH. 3

CCLK SH.4

SH. 2 $\overline{COMM}$

SH. 1 $\overline{SYSTEM\ RESET}$

U24 LS02

C33 47Pf

U39 LS00

00 SH. 2

DISTINCTIVE POST REORDER NO. 64482

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MATERIAL

FINISH

REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED

DIMENSION (THIS UNIT) (INCH)

X ± .

XX ± .

XXX ± .

ANGLES ±

CONTRACT NUMBER

DES		DATE
DR	D LY	DATE 2/6/84
CHK		DATE
ENGR		DATE

DESIGN ACTIVITY APPROVAL

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Televideo Systems, Inc.

PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD

SIZE	CODE IDENT		REV
D		132163-00	C

SCALE NONE SHEET 5 OF 6

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			

P6-1 RxD MOD
P8-12
P6-4
R25 4.7K +5V
SH.2 AIØ
SH.1 HOST BRCK
SH.2 DØ – D7
SH.1 SYS RESET
SH 2 AI
SH.2 MODEM
P8-14 RxC
P4-2 DATA FROM PNTR
P4-20 TEST
P3-18
P4-11 P BUSY
P4-19 P BUSY ALT
SH.2 R/W
SH.2 A9
SH.2 COMM
SH.4 XTAL 1/2
SH.2 AØ
P1-4 RxD KBD
SH.2 Ø2
SH.2 AII
P11-8
P8-13 DTR
P8-5
P3-5 CTS
P3-6 DSR
P3-8 DCD
P3-3 RxD
C14 C15 C16 C17 330 pF (4X)
U7 1489
U8 1489
U10 6551A
U9 6551A
U11 6551A
RP4 4.7 K(2X)
RP4 4.7K(3X)
R26 4.7K
CR10
CR7
1N914 (2X)
C18 330pF
C20 330pF
C19 330pF
C7
C21 100pF
C43 150pf
U23 LS32
U44 LS08
U33 LS32
R28 1K
W5
W6
W7
W3
RP4(2) 4.7K
R34 1K
RP4(8) 4.7K
U47 LS32
U19 HC04
U12 1488
U3 1488
C36 C24 330pF (2)
C35 330pf
C25 330PF
C26 330PF
C27 330PF
C34 330pf
C45 150pf
+5V
+12 V
-12 V
RTS P3-4
DSR P4-6
CTS P4-5
DTR W6-3
P8-3
TxD P3-2
HST DTR P3-20
W4 P3-11
DATA TO PRINTER P4-3
DCD P4-8
IRQ SH. 2
MOD P6-3
TxD MOD P6-2
P8-4
TxD KBD P1-5

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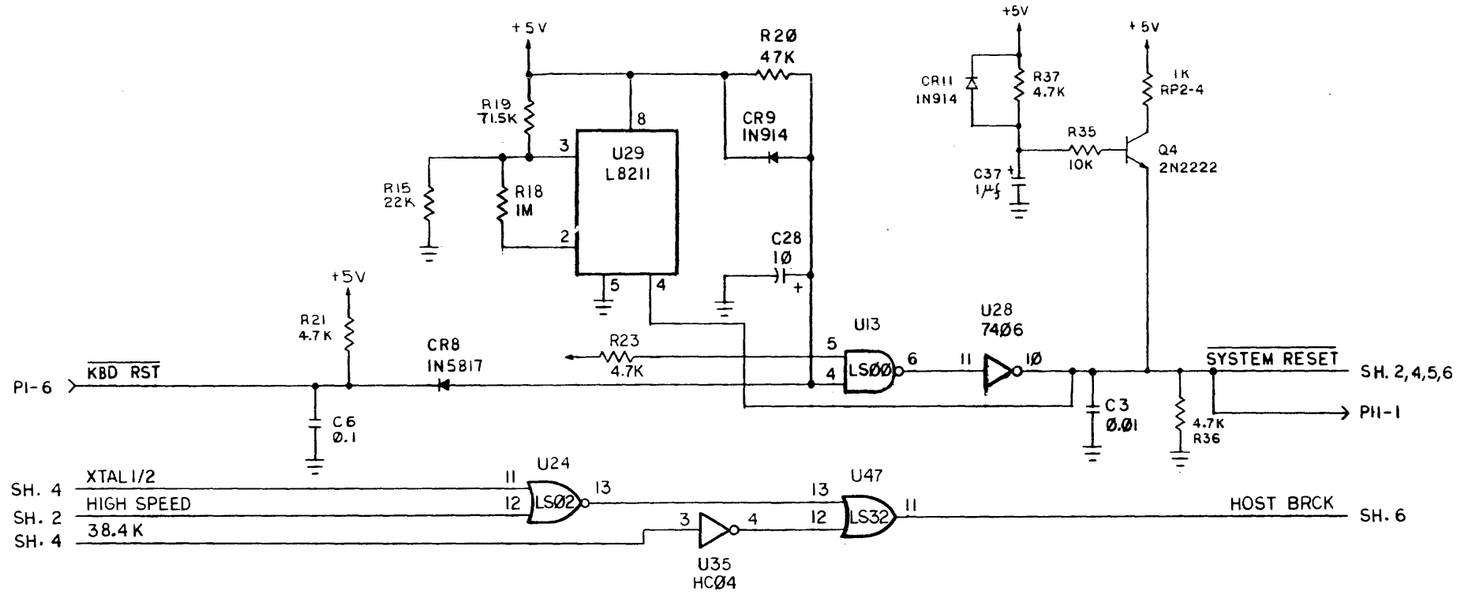
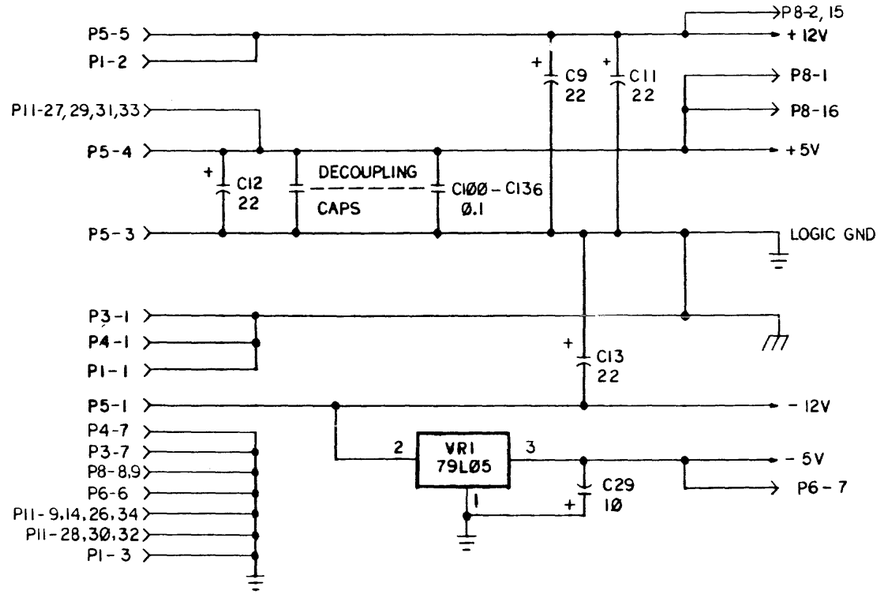
MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION mm / INCH
ANGLES

CONTRACT NUMBER
DES
DR D LY
CHK
ENGR
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL
DATE

TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD
SIZE D | CODE IDENT | 132163-00 | REV E
SCALE NONE | SHEET 6 OF 6

REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
A	PROD RELEASE	2661	1/5/85	
B	REL REV B FAB PER ECO	2691T	3/4/85	
C	REL REV C FAB SMALL BD	2820T	6/4/85	
D	REV VALUES OF R16 & R17	2866T	6/24/85	
E	REL REV D FAB PER ECO	2980T	8/6/85	
F	ADD C41 PER ECO	3035T	9/4/85	
G	REV R19 & JUMPERS	3133T	9/26/85	
H	DEL R25 PER ECO	3222T	1/9/86	





NOTES : (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4W .
2. ALL CAPACITORS ARE VALUED IN MICROFARADS .

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION — SEE INCH
ANGLES ±

CONTRACT NUMBER
DES.
DR. D LY 11/17/84 DATE
CHK. DATE
ENGR. DATE
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD
SIZE D | CODE IDENT | 132163-00 | REV H
SCALE NONE | SHEET 1 OF 6

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			

A0-15

+5V

U1 65C02

RP1(2) 4.7K

VDD, RDY, NMI, IRQ, SYNC, RESET, S.O., VSS, VSS, D7, D0, Ø0, R/W, Ø1, Ø2, A0, A15

SH. 3 NMI
SH. 6 IRQ
SH. 1 SYSTEM RESET
C38 100PF
SH.5 Ø0

R24 82

U2 LS139 — 1G, 1A, 1B, 2G, 2A, 2B, 1Y3, 1Y0, 2Y3, 2Y0

A8

W11

U28 7406

C31 47PF

U23 LS32

U24 LS02

U13 LS00

CONT LATCH

U27 LS32

RP2(2) 1K +5V

U19 HC04

C47 47PF

A0-13 → SH. 3
A0 → P11-3
A1 → P11-5
A2 → P11-7
R/W → SH. 3,6
CRTC → SH. 3
CHAR RAM → SH. 3
ATT RAM → SH. 3
COMM → P11-4, SH. 5,6
A7 → P11-6
WR → P11-17
RD → P11-25
CRTC WR → SH. 3
Ø1 → SH. 4
Ø2 → SH. 6
CRTC RD → SH. 3
D0-D7 → SH. 3,6

P11-10 D0
P11-11 D1
P11-12 D2
P11-13 D3
P11-16 D4
P11-15 D5
P11-18 D6
P11-24 D7

U5 2764 — A0, A12, CE, GND, OE, D0, D7

U4 CO-FF 27128 — VPP, VCC, A0, A13, CE, GND, OE, D0, D7

RP1(3) 4.7K

U19 HC04

A13

A0-13

W10

W9

W14

B1 3.2V

CR5 IN914

R29 680

CR3 IN914

C30 0.1

U6 6116LP4 — CE, A0, A10, WE, GND, OE, D0, D7

R14 1K

R17 10K

R12 1K

R13 82

Q1 2N4264

Q2 2N4264

R16 4.7K

+12V

SYSTEM RESET → SH.1

RP1(4) 4.7

U15 LS273 — VCC MR, D0, D1, D2, D3, D4, D5, D6, D7, CK, Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7

Q0 → DTR → SH. 6
Q1 → HIGH SPEED → SH. 1,4
Q2 → MODEM → SH. 6
Q3 → 80G/GOB → SH. 4
Q4 → LINE/PAGE ATT → SH. 4
Q5 → EMB/NONEMB → SH. 4
Q6 → 80/132 → SH. 5
Q7

MATERIAL — FINISH — REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED — DIMENSION | DECIMAL | INCH — X ± — XX ± — XXX ±

CONTRACT NUMBER

DSN	D LY	11/22/84 DATE
DR		DATE
CHK		DATE
ENGR		DATE

DESIGN ACTIVITY APPROVAL

CUSTOMER APPROVAL

Televideo Systems, Inc.

PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD

SIZE	CODE IDENT		REV
D		132163-00	H

SCALE NONE — SHEET 2 OF 6

8 7 6 5 4 3 2 1

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			

A0-A13

+5V

U25 6116P2 TC-5564 PL-10

U30 6116P2 TC-5564 PL-10

U31 6116P2

U26 6116P2

W8 W2 W1

CD0-CD7

AD0-AD7

A11'

R3

P11-23

VSYNC SH. 4

RP2(5) 1K VSYNC P2-5

U28 7406

SH. 2 D0-D7

SH. 2 ATT RAM

SH. 2 CHAR RAM

SH. 5 QT

SH. 2 R/W

SH. 5 CCLK

SH. 2 CRTC RD

SH. 2 CRTC CE

SH. 2 CRTC WR

SH. 4 CURSOR

SH. 4 BLANK

SH. 2 NMI

RP1(5) 4.7K

U14 SCN2674 AVDC

HSYNC DADDI3 CNTRL1

ACLL

RP1(6) 4.7K

U46 LS32

U44 LS08

U48 S04

U43 S32

U20 LS245

U18 LS245

D0-D7

A0-A12

U16 U17 U21 U22 LSI57

R5 81

DADD0 DADD13

A0-A13

U43 S32

HSYNCB P2-1

HSYNC SH. 4

DADD0-DADD13 SH. 4

P11-22

MATERIAL

FINISH

REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED

DIMENSION	DECIMAL INCH
X	±
.XX	±
.XXX	±
ANGLES	±

CONTRACT NUMBER

CUSTOMER APPROVAL

		DATE
DES.		
DR.	D LY	11/26/84 DATE
CHK.		DATE
ENGR.		DATE

DESIGN ACTIVITY APPROVAL

TeleVideo Systems, Inc.

PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD

SIZE	CODE IDENT		REV
D		132163-00	H

SCALE NONE

SHEET 3 OF 6

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			

SH. 3 AD0 - AD7
SH. 3 CD0 - CD7
SH. 5 CCLK
SH. 3 DADD0 - DADD13
SH. 3 BLANK
SH. 3 HSYNC
SH. 5 DCC
SH. 5 DOT CLK
SH. 3 CURSOR
SH. 3 VSYNC
SH. 2 HIGH SPEED
SH. 2 B0G/G0B
SH. 2 LINE/PAGE ATT
SH. 2 EMB/NONEMB
SH. 2 Ø1

U32 LS374
U33 LS374
U45 2732
U28 7406
RP2(7) 1K
R4 82
R1 82
U48 LS04
U44 LS08
U13 LS00
U36 ASI94/SI94
U37 ASI94/SI94
U42 ASI94/SI94
RP1(7) 4.7K
RP1(8) 4.7K
RP1(9) 4.7K
U28 7406
R11 4.7
C2 4.7
CR6
R8 180
Q3 2N4264
R7 1K
-12V
U24 LS02
RP2(6) 1K
R6 470
W12
P11-21
P2-3
P2-4
P11-20
DCC SH. 5
SYSTEM RESET SH. 1

U34
CUR=BLK
BLANK
DOT SER
RA0
RA2
RA3
BLINK CLK
DCC
DISPEN
CURSOR
H SYNC
V SYNC
SYS RESET
HALF INTENSITY
VIDEO
COMP VID
CHAD 0
CHAD 1
CHAD 2
CHAD 3
CHAD 7
ATT
Ø2.W
DISPRAM
R/W
Ø1
ATT BNKTNH 925/920
Ø2
BOW/WOB PG2
LINE/PG ATT GND
910/925 SDR 40-7F
38.4K SH. 1
XTAL 1/2 SH 1,6

U35 LS374
R2 82
U19 HC04
Y3 3.6864
R27 47K
C5 0.001

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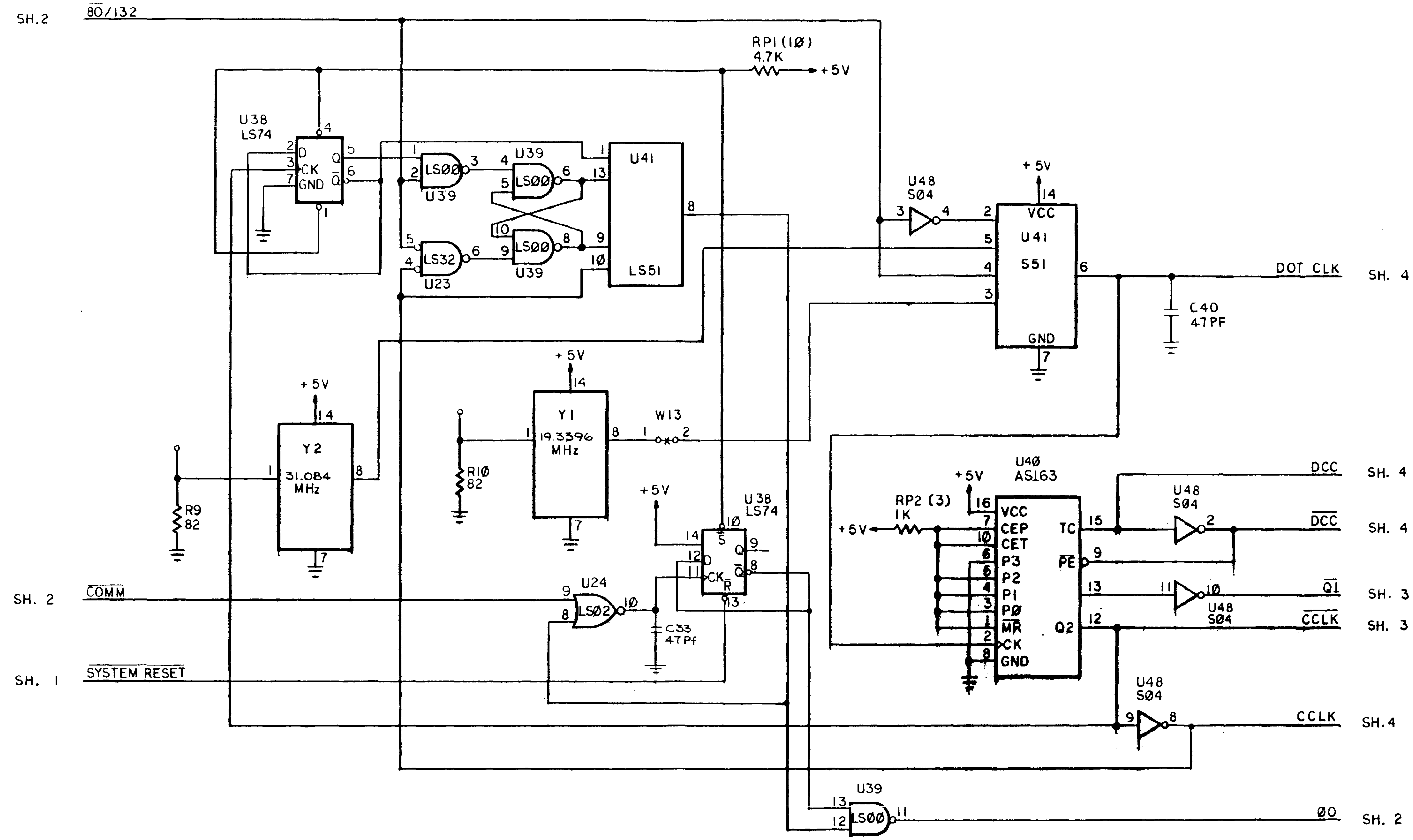
MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION | DECIMAL | INCH
CONTRACT NUMBER
DRS | DATE
DR. D LY | 11/21/84
CHK. | DATE
ENGR. | DATE
DESIGN ACTIVITY APPROVAL | DATE
CUSTOMER APPROVAL | DATE

TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD
SIZE D | CODE IDENT | 132163-00 | REV H
SCALE NONE | SHEET 4 OF 6

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON		SEE SH 1			



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MATERIAL | FINISH | REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED | DIMENSION MM/INCH | X = ± | XX = ± | XXX = ± | ANGLES ±

CONTRACT NUMBER | DES. | DR. D LY DATE 11/26/84 | CHK. DATE | ENGR. DATE | DESIGN ACTIVITY APPROVAL | CUSTOMER APPROVAL

TeleVideo Systems, Inc.

PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD

SIZE	CODE IDENT		REV
D		132163-00	H
SCALE NONE		SHEET 5 OF 6	

P6-1 R×D MOD
P8-12
P6-4

SH.2 A10
SH.1 HOST BRCK
SH.2 D0-D7

P3-5 CTS
P3-6 DSR
P3-8 DCD
P3-3 R×D

C14 C15 C16 C17 330 pF (4X)

SH.1 SYS RESET
SH 2 A1
SH.2 MODEM

P8-14 R×C

C18 330pF

P4-2 DATA FROM PNTR
P4-20 TEST
P3-18

C20 330pF C19 330pF C7

P4-11 P BUSY
P4-19 P BUSY ALT

SH.2 R/W
SH.2 A9
SH.2 COMM
SH.4 XTAL1/2
SH.2 A0

P1-4 R×D KBD
SH.2 Ø2

C43 150pf

C21 100pF

SH.2 A11
P11-8
P8-13
SH.2 DTR
P8-5

U7 1489
U8 1489
U10 6551A
U11 6551A
U9 6551A
U23 LS32
U44 LS08
U47 LS32
U19 HCØ4
U12 1488
U3 1488
U33 LS32

R26 4.7K
CR10 CR7 1N914 (2X)
RP4 4.7K(2X)
RP4 4.7K(3X)
R28 1K
R34 1K
RP4(2) 4.7K
RP4(8) 4.7K

C36 C24 330pF (2)
C35 330pf
C25 330pF
C26 330pF
C27 330pF
C34 330pf
C45 150pf

RTS P3-4
DSR P4-6
CTS P4-5
DTR W6-3
P8-3
MOD P6-3
TxD P3-2
HST DTR P3-20
W4 P3-11
DATA TO PRINTER P4-3
DCD P4-8
IRQ SH.2
TxD MOD P6-2
P8-4
TxD KBD P1-5

+5V +12V -12V

APPLICATION		REVISION	DESCRIPTION	BCO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			

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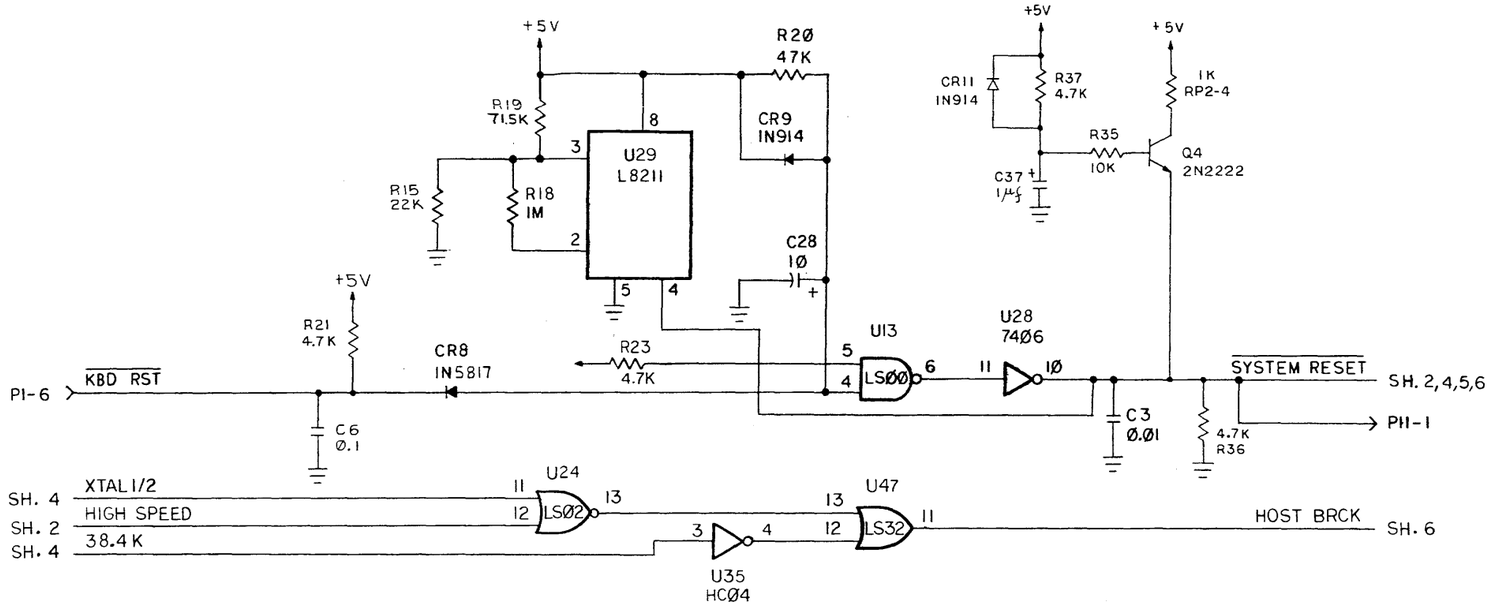
MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES

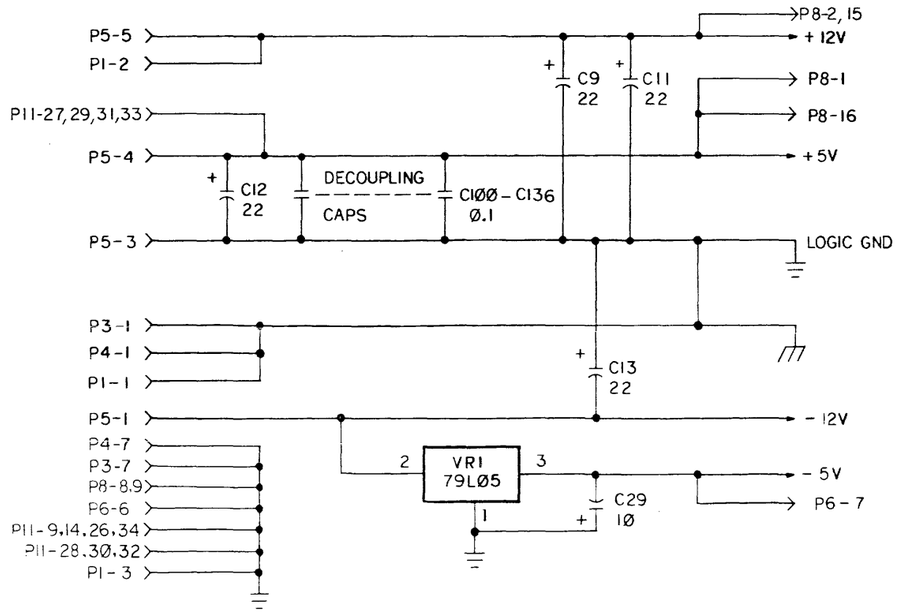
TOLERANCES UNLESS NOTED
DIMENSION ENGL. METRIC
.X ± .1 2.5
.XX ± .03 .8
.XXX ± .010 .25
ANGLES ±

CONTRACT NUMBER
DES.
DR. D LY DATE 11/21/84
CHK. DATE
ENGR. DATE
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD
SIZE D | CODE IDENT | 132163-00 | REV H
SCALE NONE | SHEET 6 OF 6

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON	A	PROD RELEASE	2661	11/4/85	
		B	REL REV B FAB PER ECO	2691T	3/4/86	
		C	REL REV C FAB SMALL BD	2820T	6/12/86	
		D	REV VALUES OF R16 & R17	2866T	5/24/86	
		E	REL REV D FAB PER ECO	2980T	9/8/86	
		F	ADD C41 PER ECO	3035T	9/18/86	
		G	REV R19 & JUMPERS	3133T	9/26/86	
		H	DEL R25 PER ECO	3222T	11/19/86	
		J	ON SH.4 ADD R38 1M	3602T	10/19/87	
		K	ON SH. 2 & 3 ADD SYS RAM-R/$\overline{W}$	3636T	11/23/87	





NOTES : (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4W .
2. ALL CAPACITORS ARE VALUED IN MICROFARADS .

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION
ANGLES
CONTRACT NUMBER
DES
DR D LY 11/17/86
CHK
ENGR
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD
SIZE D | CODE IDENT | 132163-00 | REV K
SCALE NONE | SHEET 1 OF 6

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			

A0-15

+5V

U1 65C02

VDD, RDY, NMI, IRQ, SYNC, RESET, S.O., D0, D7, VSS, VSS, Ø0, R/W, A0, A15, Ø1, Ø2

RP1(2) 4.7K

SH. 3 NMI
SH. 6 IRQ
SH. 1 SYSTEM RESET

C38 100PF

SH.5 Ø0

C31 47PF

R24 82

U2 LS139

U28 7406

U23 LS32

W11

A8

U24 LSØ2 · U13 LSØØ · CONT LATCH

U27 LS32 (WR, RD, CRTC WR)

RP2(2) 1K +5V

U19 HCØ4

C47 47PF

A0-13 → SH. 3
A0 → P11-3
A1 → P11-5
A2 → P11-7
R/W → SH. 3,6
CRTC → SH. 3
CHAR RAM → SH. 3
ATT RAM → SH. 3
COMM → SH. 5,6
A7 → P11-6
WR → P11-17
RD → P11-25
CRTC WR → SH. 3
Ø1 → SH. 4
Ø2 → SH. 6
CRTC RD → SH. 3
D0-D7 → SH. 3,6

P11-10 D0
P11-11 D1
P11-12 D2
P11-13 D3
P11-16 D4
P11-15 D5
P11-18 D6
P11-24 D7

U5 2764

U4 CO-FF 27128

RP1(3) 4.7K

U19 HCØ4

W10 · W9 · W14

A13

A0-13

SH.3 SYS RAM R/W

B1 3.2V · CR5 1N914 · R29 680 · CR3 1N914 · C30 0.1

U6 6116LP4

R14 1K · R17 10K · R12 1K · R13 82 · R16 4.7K

Q1 2N4264 · Q2 2N4264

+12V

RPI(4) 4.7

U15 LS273

DTR	SH. 6	
HIGH SPEED	SH. 1,4	
MODEM	SH. 6	
BOG/GOB	SH. 4	
LINE/PAGE ATT	SH. 4	
EMB/NONEMB	SH. 4	
80/132	SH. 5	

SYSTEM RESET SH.1

MATERIAL · FINISH · REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED: DIMENSION — X ± , XX ± , XXX ± , ANGLES ±

CONTRACT NUMBER

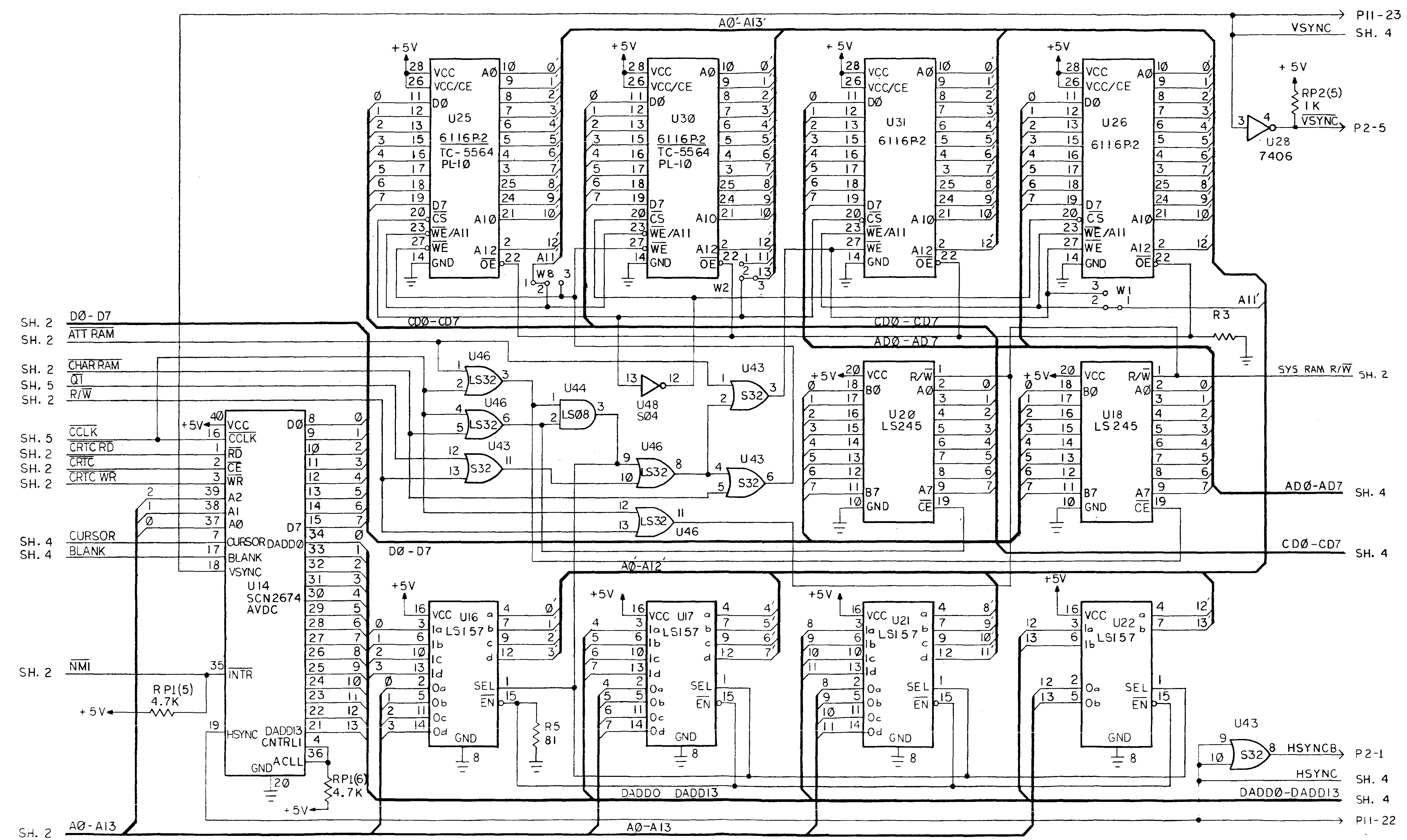
DES	D LY	11/22/84 DATE
DR		DATE
CHK		DATE
ENGR		DATE
DESIGN ACTIVITY APPROVAL		
CUSTOMER APPROVAL		

TeleVideo Systems, Inc.

PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD

SIZE	CODE IDENT		REV
D		132163-00	K
SCALE NONE		SHEET 2 OF 6	

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON		SEE SH 1			



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MATERIAL / FINISH / REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED — DIMENSION IN/INCH — X ±, XX ±, XXX ±, ANGLES ±

CONTRACT NUMBER — DES — DR D LY DATE 11/26/84 — CHK — ENGR — DESIGN ACTIVITY APPROVAL — CUSTOMER APPROVAL

TeleVideo Systems, Inc.

PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD

SIZE	CODE IDENT		REV
D		132163-00	K
SCALE NONE		SHEET 3 OF 6	

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON		SEE SH 1			

SH. 3 AD0 - AD7
SH. 3 CD0 - CD7
SH. 5 CCLK
SH. 3 DADD0 - DADD13
SH. 3 BLANK
SH. 3 HSYNC
SH. 5 DCC
SH. 5 DOT CLK
SH. 3 CURSOR
SH. 3 VSYNC
SH. 2 HIGH SPEED
SH. 2 B0G/G0B
SH. 2 LINE/PAGE ATT
SH. 2 EMB/NONEMB
SH. 2 01

U32 LS374
U33 LS374
U35 LS374
U45 2732
U36 ASI94/S194
U37 ASI94/S194
U42 ASI94/S194
U13 LS00
U44 LS08
U48 LS04
U28 7406
U24 LS02
RP1 (7) 4.7K
RP1 (8) 4.7K
RP1(9) 4.7K
RP2(6) 1K
RP2(7) 1K
R1 82
R2 82
R4 82
R6 470
R7 1K
R8 180
R11 4.7
C2 4.7
C5 0.001
CR6
Q3 2N4264
W12
Y3 3.6864
U19 HC04

P11-21
P2-3
P2-4
P11-20
DCC
SYSTEM RESET SH. 5 SH. 1
38.4K SH. 1
XTAL 1/2 SH 1,6

CUR= BLK
BLANK
DOT SER
RA0
RA2
RA3
BLINK CLK
DCC
DISPEN
CURSOR
H SYNC
V SYNC
SYS RESET
CHAD 0
CHAD 1
CHAD 2
CHAD 3
CHAD 7
ATT
Ø2
BOW/WOB
LINE/PG ATT
910/925
HALF INTENSITY
VIDEO
COMP VID
Ø2.W
DISPRAM
R/W
ATT BNK INH 925/920
PG 2
GND
SDR 40-7F

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION TOL. INCH
ANGLES
CONTRACT NUMBER
DES DATE
DR D LY 11/21/84
CHK DATE
ENGR DATE
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TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD
SIZE D | CODE IDENT | 132163-00 | REV K
SCALE NONE | SHEET 4 OF 6

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON		SEE SH 1			

SH.2 $\overline{80}/132$

RP1 (1Ø) 4.7K +5V

U38 LS74

U39 LSØØ

U23 LS32

U41 LS51

U48 SØ4

+5V

VCC U41 S51 GND

DOT CLK SH. 4

C40 47PF

Y2 31.084 MHz R9 82

Y1 19.3396 MHz W13 RIØ 82

U24 LSØ2 C33 47 Pf

SH. 2 $\overline{COMM}$

SH. 1 $\overline{SYSTEM\ RESET}$

U40 AS163 RP2 (3) 1K

VCC CEP CET P3 P2 P1 PØ $\overline{MR}$ CK GND TC $\overline{PE}$ Q2

DCC SH. 4

$\overline{DCC}$ SH. 4

$\overline{Q1}$ SH. 3

$\overline{CCLK}$ SH. 3

CCLK SH.4

ØO SH. 2

MATERIAL FINISH REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED DIMENSION mm/INCH X ± XX ± XXX ± ANGLES

CONTRACT NUMBER DES DR D LY 2/6/84 CHK ENGR DESIGN ACTIVITY APPROVAL CUSTOMER APPROVAL

TeleVideo Systems, Inc.

PCB SCHEMATIC DIAGRAM
955 CONTROL BOARD

SIZE D | CODE IDENT | 132163-ØØ | REV K

SCALE NONE | SHEET 5 OF 6

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			

P6-1 RxD MOD
P8-12
P6-4

SH.2 AIØ
SH.1 HOST BRCK
SH.2 DØ - D7

P3-5 CTS
P3-6 DSR
P3-8 DCD
P3-3 RxD

C14 C15 C16 C17 330 pF (4X)

SH.1 SYS RESET
SH 2 AI
SH.2 MODEM

P8-14 RxC

C18 330pF

P4-2 DATA FROM PNTR
P4-20 TEST
P3-18

C20 330pF C19 330pF

P4-11 P BUSY
P4-19 P BUSY ALT

C7

SH.2 R/W
SH.2 A9
SH.2 COMM
SH.4 XTAL1/2
SH.2 AØ

P1-4 RxD KBD
SH.2 Ø2

C43 150pf

C21 100pF

SH.2 A11
P11-8
P8-13
SH.2 DTR
P8-5

U7 1489 — VCC, AØ BØ CØ DØ, A1 B1 C1 D1, RCA RCB RCC RCD, GND; +5V; R26 4.7K; CR10 CR11 1N914 (2X)

RP4 4.7K(2X) (3) (4)

U8 1489 — VCC, AØ BØ CØ DØ, A1 B1 C1 D1, RCA RCB RCC RCD, GND; +5V

RP4 4.7K(3X) (6)(5)(7) +5V

U10 6551A — DØ VCC RTS IRQ TxD GND; D7 RES DCD R/W CSØ CS1 XTAL1 RSØ RS1 Ø2 RxD DSR CTS

U9 6551A — DØ VCC RTS IRQ TxD GND; D7 RES DCD R/W CSØ CS1 XTAL1 RSØ RS1 Ø2 RxD DSR CTS

U44 LSØ8

U11 6551A — DØ VCC RTS IRQ TxD GND; D7 RES DCD R/W CSØ CS1 XTAL1 RSØ RS1 Ø2 RxD DSR CTS RxC

U47 LS32; U44 LSØ8

U12 1488 — +12 V, -12 V

RTS → P3-4
C36 C24 330pF (2)
DSR → P4-6
CTS → P4-5
DTR → W6-3
C35 330 Pf

P8-3
MOD → P6-3

U19 HCØ4

U3 1488 — +12 V, -12 V

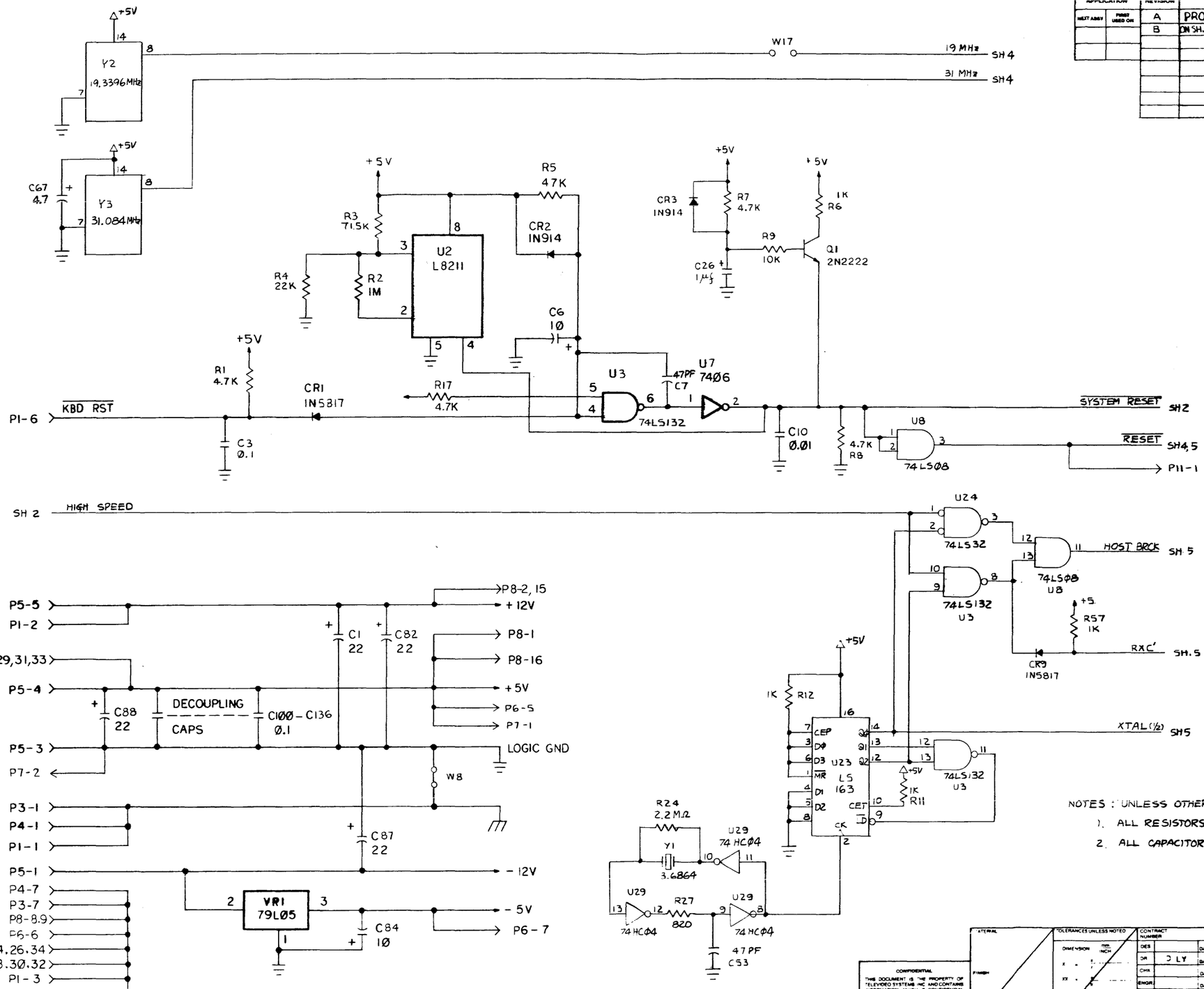
TxD → P3-2
C25 330PF
HST DTR → P3-20
C26 330PF W4 → P3-11
DATA TO PRINTER → P4-3
C27 330PF
C34 330pf
DCD → P4-8
IRQ → SH. 2
TxD MOD → P6-2, P8-4
TxD KBD → P1-5
C45 150Pf

U33 LS32
R28 1K
RP4(2) 4.7K
R34 1K
RP4(8) 4.7K +5V

U23 LS32

MATERIAL	TOLERANCES UNLESS NOTED	CONTRACT NUMBER	TeleVideo Systems, Inc.			
FINISH	DIMENSION mm INCH; X ± ±; XX ± ±; XXX ± ±; ANGLES ±	DES DATE; DR D LY 11/21/84; CHK DATE; ENGR DATE; DESIGN ACTIVITY APPROVAL; CUSTOMER APPROVAL	PCB SCHEMATIC DIAGRAM 955 CONTROL BOARD			
REMOVE ALL BURRS AND SHARP EDGES			SIZE D	CODE IDENT 132163-00	REV K	
			SCALE NONE	SHEET 6 OF 6		

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
		A	PROD RELEASE	3563T	4/8/86	
		B	ON SH. 1 CHG CR9 FR. IN914 TO IN587	3710T	12/8/87	



NOTES : UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE VALUED IN OHMS ±5%, ¼W.
2. ALL CAPACITORS ARE VALUED IN MICROFARADS.

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED
DIMENSION / TOL. INCH
ANGLES

CONTRACT NUMBER
DES
DR J LY 1/7/86
CHK
ENGR
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.

PCB SCHEMATIC
355 ENHANCED G/A

SIZE	CODE IDENT		REV
D		132383-00	B

SCALE NONE SHEET 1 OF 5

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			

A0-15

+5V

U4 65C02

RPI(2) 4.7K

SH. 3 NMI
SH. 5 IRQ
SH. 1 SYSTEM RESET

C11 100PF

SH.4 Ø0
SH.4 CCLK

P11-10 D0
P11-11 D1
P11-12 D2
P11-13 D3
P11-16 D4
P11-15 D5
P11-18 D6
P11-24 D7

U4 CO-FF 27123

U15 2764

U14

R18 4.7K

W7

W5

W6

A13
A0-13

U29 HC04

R21 82

U19 LS139

74LS04 U44

74LS32 U11

74LS32 U24

U44 74LS04 74LS132 U11 U3

CONT LATCH

U34 LS32

R58 1K +5V

U29 HC04

U34 LS32

C5 47PF

B1 3.2V CR6 IN914 R14 680

CR7 IN914 C38 10

R15 1K

Q2 2N4264

R16 10K OPTION

R13 1K

U16 EI16LP4

R19 82

Q3 2N4264

+12V

R20 4.7K OPTION

A0-13 SH. 3
A0 P11-3
A1 P11-5
A2 P11-7
R/W SH. 3,5
CRTC SH. 3
CHAR RAM SH. 3
ATT RAM SH. 3
P11-4
COMM SH. 4,5
A7 P11-6
WR P11-17
RD P11-25
CRTC WR SH. 3
Ø2 SH. 5
CRTC RD SH. 3
D0-D7 SH. 3,5

R45 4.7K

U39 LS273

DTR SH. 5
2 HIGH SPEED SH. 1
16 MODEM SH. 5
5 PROT MODE SH 4
15 LITE/DARK SH 4
6 LINE/PAGE ATT SH. 4
12 EMB/NONEMB SH. 4
9 80/132 SH. 4

TOLERANCES UNLESS NOTED

CONTRACT NUMBER	
DES	D LY
DR	
CHK	
ENGR	
DESIGN ACTIVITY APPROVAL	
CUSTOMER APPROVAL	

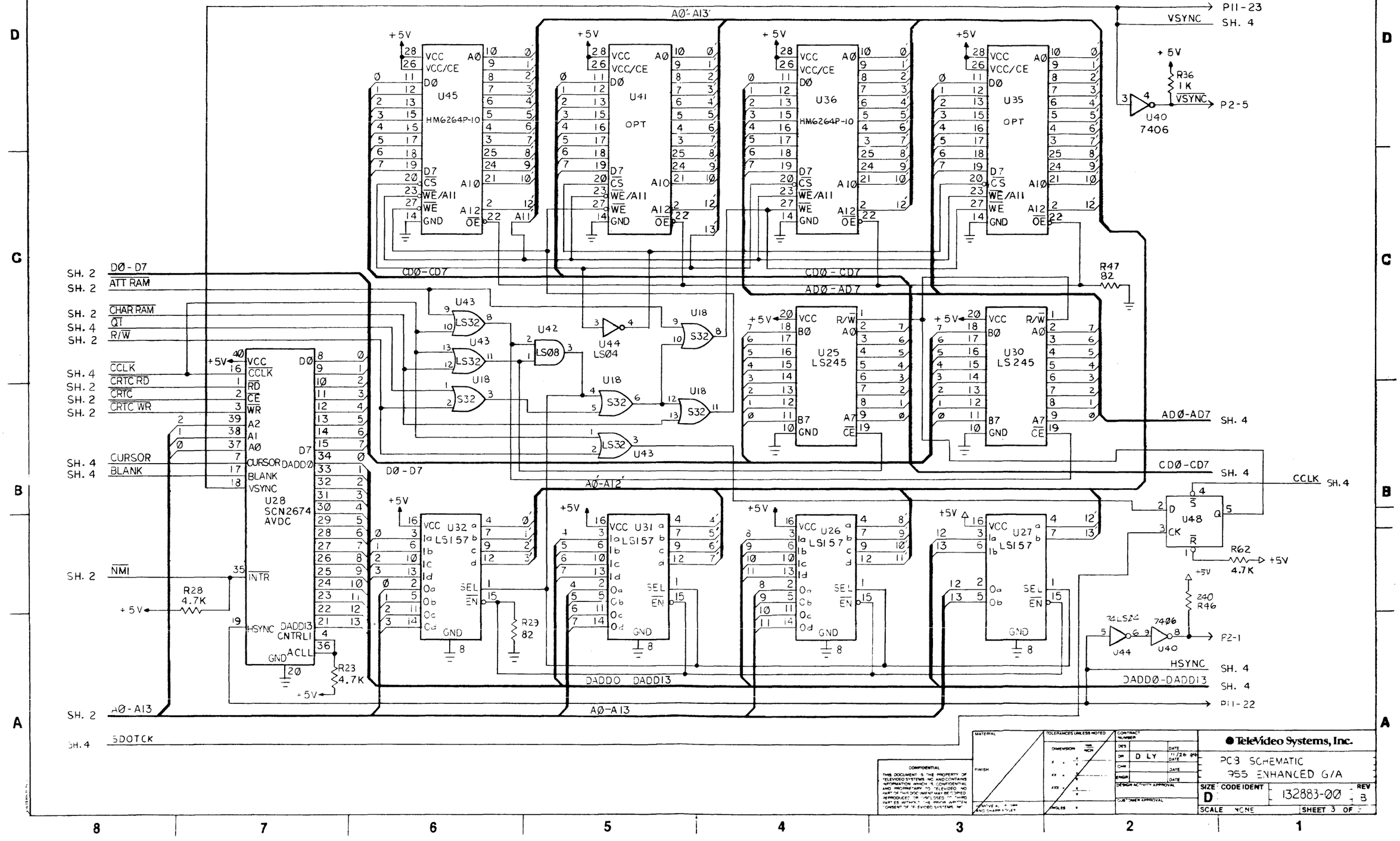
TeleVideo Systems, Inc.

PCB SCHEMATIC
955 ENHANCED G/A

SIZE	CODE IDENT	REV
D	132883-00	B

SCALE NONE SHEET 2 OF 5

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SH 1			



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MATERIAL

FINISH

REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED

DIMENSION | TOL. NON-CUM

X | ±

XX | ±

XXX | ±

ANGLES | °

CONTRACT NUMBER

		DATE
DES		
DR	D LY	11/26 84
CHK		
ENGR		

DESIGN ACTIVITY APPROVAL

CUSTOMER APPROVAL

● TeleVideo Systems, Inc.

PCB SCHEMATIC

955 ENHANCED G/A

SIZE	CODE IDENT	DWG NO	REV
D		132883-00	B

SCALE NONE SHEET 3 OF 5

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON		SEE SHT 1			

SH3 ADϕ - AD7
SH3 CDϕ - CD7
SH3 DADDϕ - DADD13
SH 3 BLANK
SH3 HSYNC
SH2 PROT MODE
SH2 80/132
SH1 RESET
SH1 19 MHz
SH1 31 MHz
SH3 CURSOR
SH3 VSYNC
SH2 COMM
SH2 LITE/DARK
SH2 LINE/PAGE ATT
SH2 EMB/NONEMB

U47 LS374 — U33 LS374 — U44 LS04 — U46 2732 — U48 74LS74 — U42 74L508 — U38 74F166 — U49 LS08 (OPTION) — U40 7406 — U42 — U40 7406

R56 4.7K, R54 1K, R53 1K, R61 4.7K, R48 82, R49 82, R43 82, R44 4.7K, R52 1K, R40 4.7, C78 4.7, R38 180, CR8, Q4 2N4264, R42 1K, R41 1K, R39 1K, R32 1K, R35 1K, R30 1K, R31 470, R34 1K, R33 1K, C73 33μ, R51 4.7K, W11, W12, W13, W14, W16, W10

74L508 AD7 AD6 AD5 AD4 AD3 AD2 AD1 ADϕ

U37 G/A 270947-00 — HSDLY, 901ϕB, DLYDE, PROT, FIB, ATT, HI, CHAD3, CHAD2, CHAD1, CHADϕ, LDSRB, SDOTCK, DOTSER, PROTHI, PROTRV, DW, BLANK, HORSYN, CCLK, ROW1ϕ, BLKCLK, 8ϕB132, SYSRES, 19MHz, 31MHz, CURSOR, VERTSY, COMMB, LBODK, LBOPAT, DBOATT, VDD, FI, HALF IN, VIDEO, COMSYC, N.C., DECBTV, DLY, PURB, FOCBHI, ATTSPHI, ATSPBK, Vss, QB, CCLKB, PHIϕ

P11-21
P2-3
P2-4
P11-2ϕ
$\overline{Q1}$ SH 3
$\overline{CCLK}$ SH 2,3
ϕ0 SH 2
CCLK SH. 3
SDOTCK SH. 3

MATERIAL — FINISH — REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED — DIMENSION — FRACTIONS — INCH — X = ± — XX = ± — XXX = ± — ANGLES ±
CONTRACT NUMBER — DES. — DR. — CHK. — ENGR. — DESIGN ACTIVITY APPROVAL — CUSTOMER APPROVAL — DATE

TeleVideo Systems, Inc.
PCB SCH
955 ENHANCED G/A
SIZE D | CODE IDENT |) 32883 -00 | REV B
SCALE | SHEET 4 OF 5

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON		SEE SH 1			

P6-1 RxD MOD
P8-12
P6-4
R55 +5V
R60 27K
SH.2 AIØ
SH.1 HOST BRCK
SH.2 DØ-D7

+5V
U9 1489
VCC 14
AØ 3
BØ 6
CØ 8
DØ 11
RCA 2
RCB 5
RCC 9
RCD 12
GND 7
A1 1
B1 4
C1 10
D1 13
R10 4.7K
CR5 CR4 1N5817 (2X)
RP1 4.7K(2X) +5V (8) (6)
P3-5 CTS
P3-6 DSR
P3-8 DCD
P3-3 RxD
C31 C30 C17 C18 330 pF (4X)
RESET
SH.1 AI
SH 2 MODEM
SH.2

SH.1 RxC'
P8-14 RxC
W15
C13 330pF
U5 1489
P4-2 DATA FROM PNTR
P4-20 TEST
P3-18
W1 W2
C4 330pF C15 330pF C16
P4-11 P BUSY
P4-19 P BUSY ALT
W3
RP1 4.7K(3X) +5V
SH.2 R/W
SH.2 A9
SH.2 COMM
SH.1 XTAL1/2
SH.2 AØ

U11 LS32
P1-4 RxD KBD
SH.2 Ø2
C20 150pF
C19 100pF
R59 4.7K +5V

SH.2 A11
P11-8
P8-13 DTR
SH.2
P8-5

U21 6551A
U20 6551A
DØ VCC
RTS
IRQ
TxD
GND
D7 RES DCD R/W CSØ CS1 XTAL1 RSØ RS1 Ø2 RxD DSR CTS RxC

U8 LSØ8
U24 LS32
R25 1K
R22 4.7K
R26 1K
R50 4.7K +5V
C4 150pF

U43 LS32
U8 LSØ8
U13 1488
U17 1488
+12V -12V
C33 C32 330PF (2)
C34 330pf
C46 330PF
C45 330PF
C44 330PF
C43 330pf
U29 HCØ4
RTS P3-4
DSR P4-6
CTS P4-5
DTR WI-3
P8-3
MOD P6-3
TxD P3-2
HST DTR P3-20
W9 P3-11
DATA TO PRINTER P4-3
DCD P4-8
IRQ SH. 2
TxD MOD P6-2
P8-4
TxD KBD P1-5

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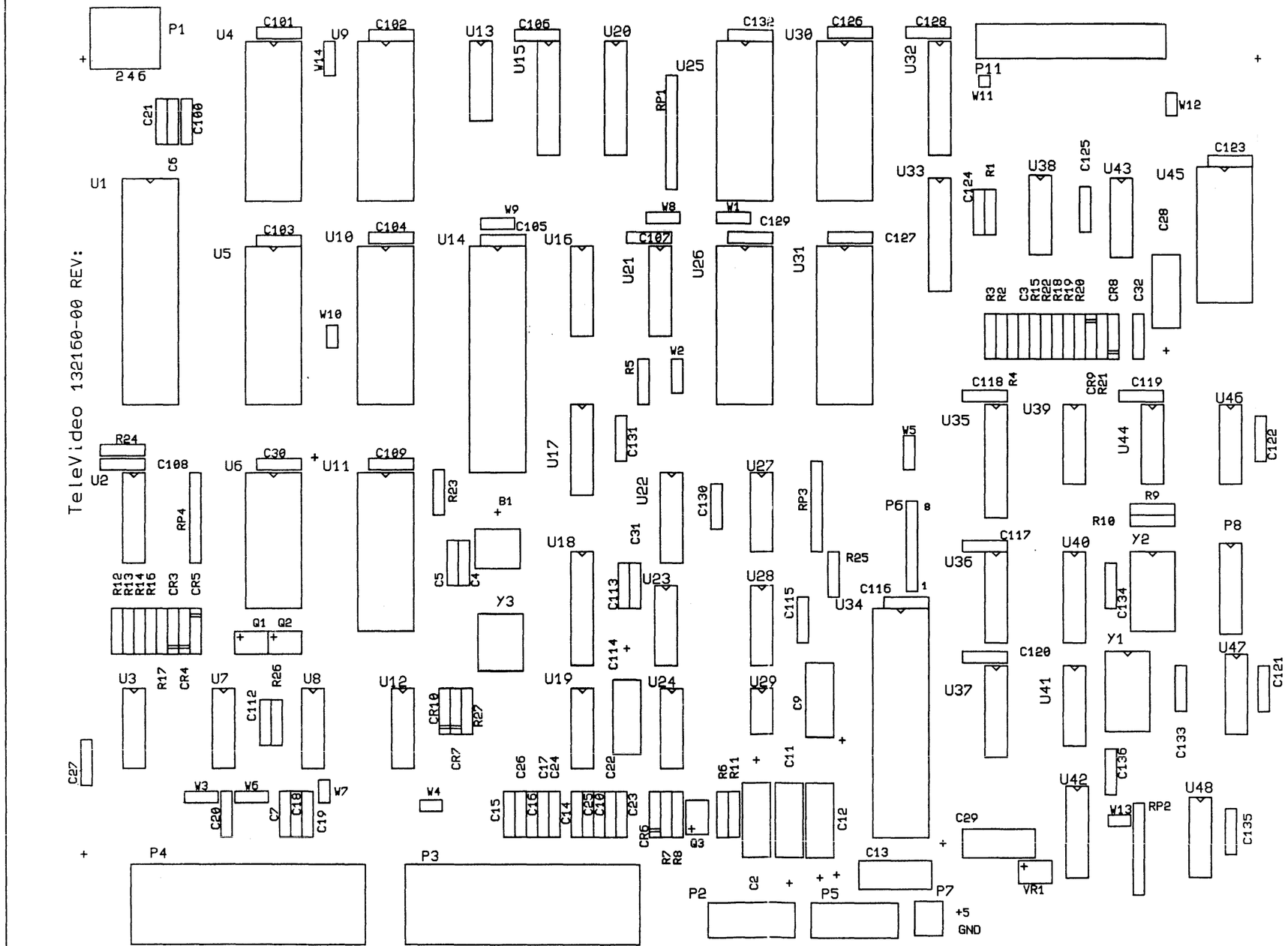
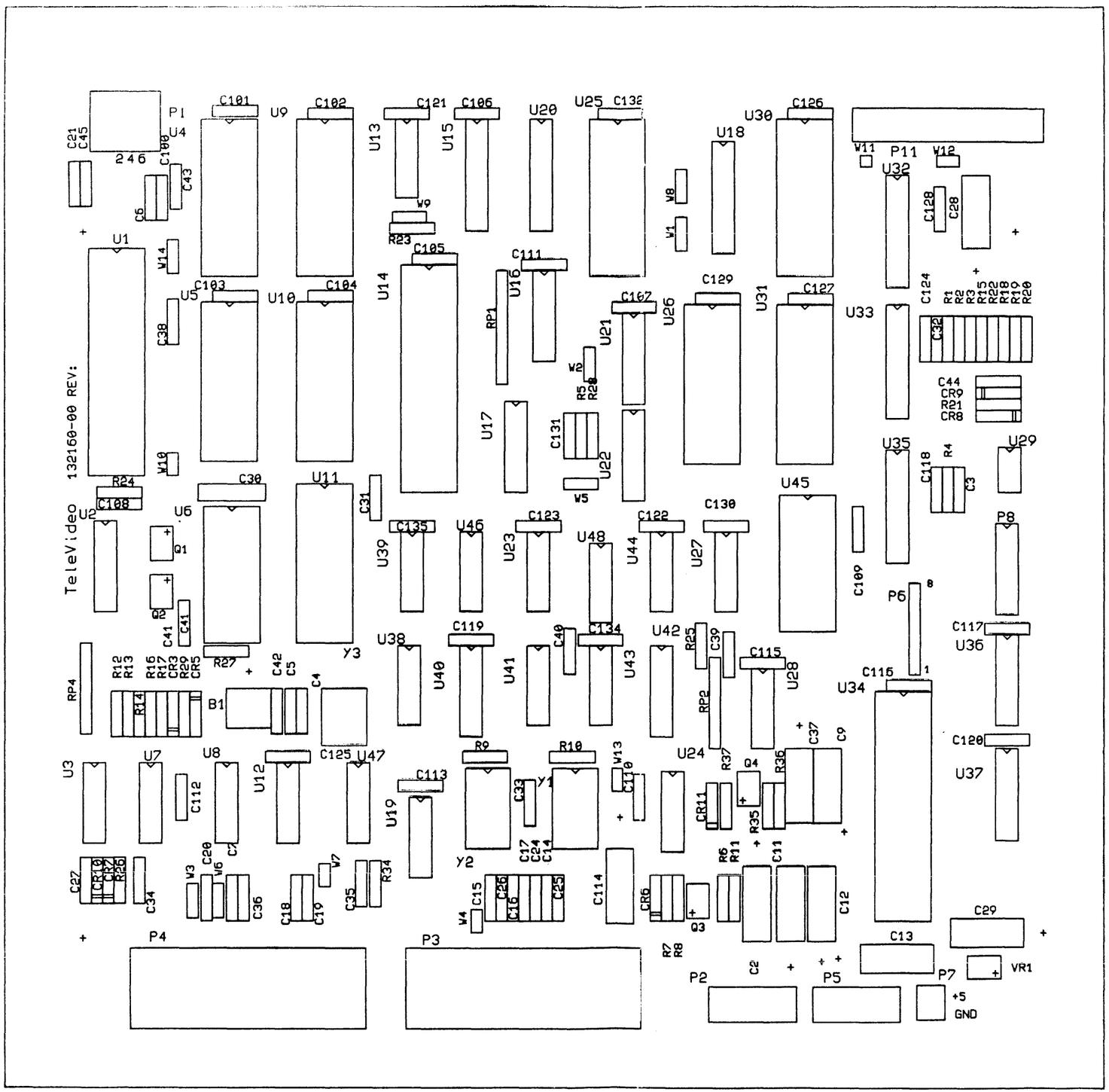
MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION mm INCH
ANGLES
CONTRACT NUMBER
DES DATE
DR D.LY DATE
CHK DATE
ENGR DATE
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

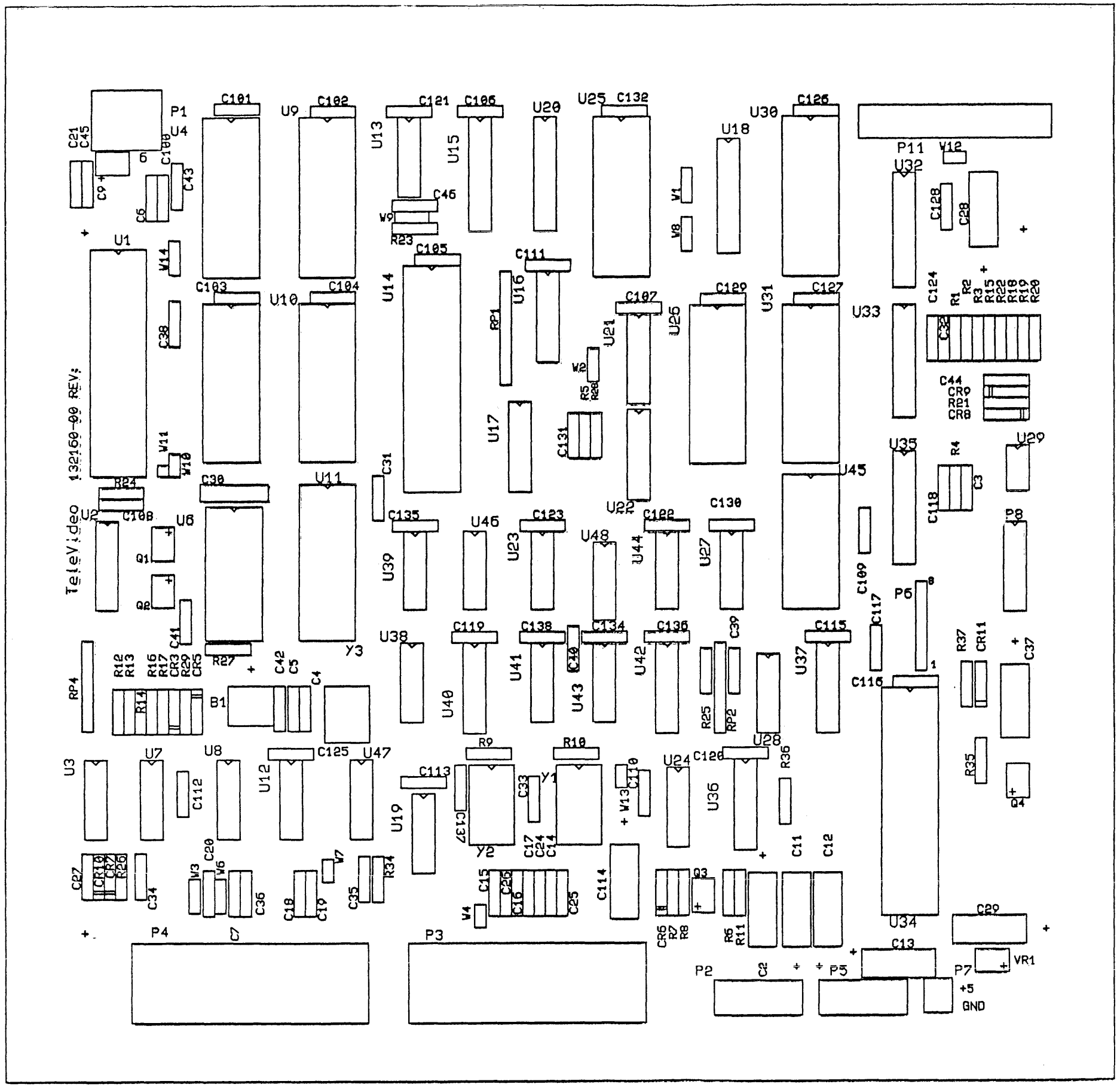
TeleVideo Systems, Inc.
PCB SCHEMATIC
955 ENHANCED G/A
SIZE D CODE IDENT
132883-00
REV B
SCALE NONE
SHEET OF



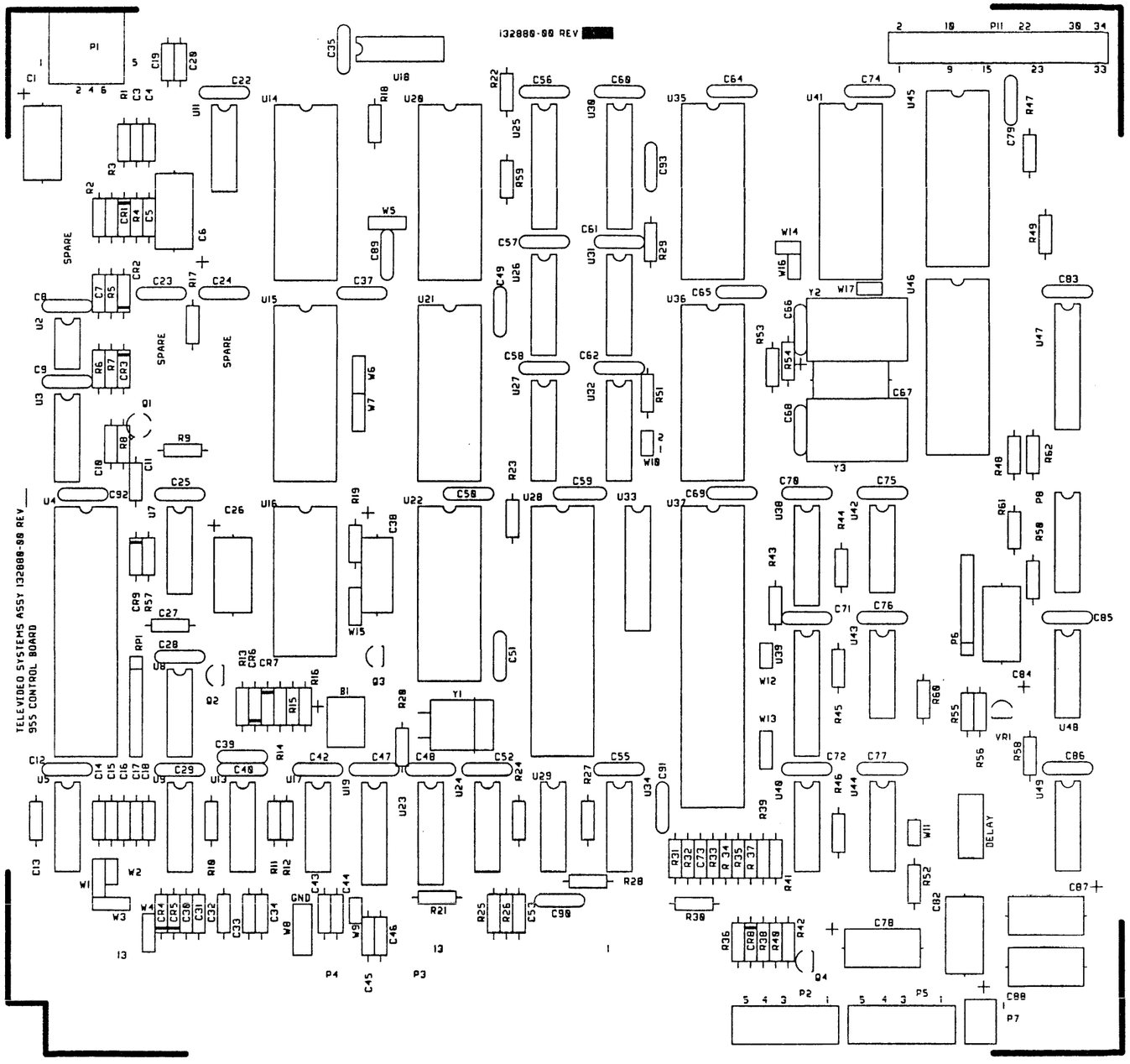
955 CONTROL BOARD
REV B



955 CONTROL BOARD
REV C



955 CONTROL BOARD
REV D



SILKSCREEN

955 LOGIC BOARD
(ENHANCED GATE ARRAY)

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON	A	PROD REL	2965T	7/18/85	
		B	ADD D505 AND R302	2927T	7/18/85	

V. HEIGHT

V. LINEARITY

R614 3.3 1/2W

16V/2200U C605

IN 4004 D601

25V/100U C606

R608 100K

C607 220P

R501 47

IN

V. YOKE

BLUE

C608 10V/2200U

R612 220

C610 .047U

H. YOKE

R309 390 1/2W

D305 BA159

BRIGHT

SG1

FOCUS

340CXB(31)N

V501

KTC1959(O) Q502

SK9041 2SC2441(F) Q501

R506 220 1/2W

R503 680 2W

C501 180P

R502 68

C508 50V 10U

R510 6.8K

R511 6.8K

R507 1.5K 1/2W

R508 10K 1/2W

S62

R509 1.5K 1/2W

SG3

BLK

RED

PINK

GRN

YLW

WHT

BLK

H3

H4

JP7

JP8

JP6

JP5

JP9

C503 .02U

VR2 2M

SFR4 100K

R504 10K 1/2W

D505 IN4757A

C504 630V/1U

D502 BA159

C507 400V/.033U

D503 BA159

P10

VI

R513 68

VR1 500B

CONTRAST

Vo

GND

Ho

C601 0.1U

IC1 TDA 1170N

R602 180K

C602 .15U

R603 180K

R604 390K

C603 0.1U

SFR1 100K

R605 47K

C604 .1U

R606 220K

R609 33K

R607 1.0/1W

R610 56K

R611 4.7K

R613 3.3

C609 25V/47U

C611 .1U

R601 4.7K

SFR2 500K

L-955

L-301

W-955

L-302

WIDTH

TO

CRT HEATER

C306 25V/6.8U NPHF

C305 25V/220U

D303 MR856

C303 400V/.001U

Q302 BU407

C301 16V/4.7U

R301 470

R302 22K

Q301 KTC200Y

T301 HDT-955

C307 50V/0.2

D504 BA159

C502 100V/100U

T302

LINEARITY

D301 IN4148

C302 50V/.01U

D307 MR856

C304 400V/.01U

5

4

3

1

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W, ±5%, RESISTANCE IS IN OHMS.

MATERIAL

FINISH

REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED

DIMENSION mm / INCH

ANGLES

CONTRACT NUMBER

DES

DR L. Dyer DATE 4/4/85

CHK DATE 7/18/85

ENGR DATE 7/18/85

DESIGN IDENTITY APPROVAL

CUSTOMER APPROVAL

TeleVideo Systems, Inc.

PCB SCHEMATIC

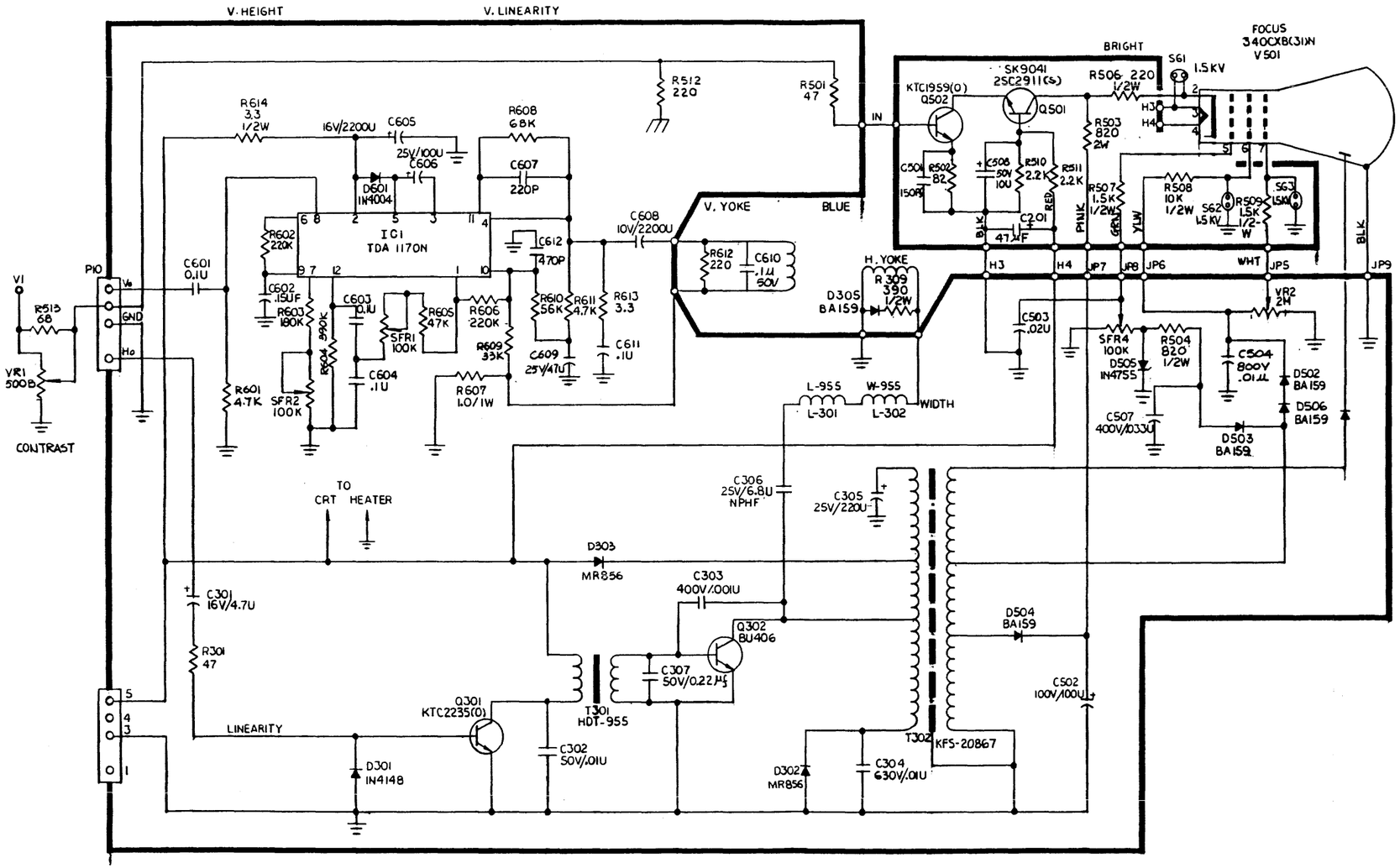
955 VIDEO MONITOR

SIZE D | CODE IDENT | 132326-00 | REV B

SCALE | SHEET 1 OF 1

DETERCH POST REORDER NO. 83067

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
		A	PROD REL	2965T	7/9/85	
		B	ADD D505 AND R302	2977T	7/19/85	
		C	CHG R602 FROM 180K TO 200K	3118T	9/24/85	
		D	UPDATE VIDEO MON. ADD NOTE 2	3408T	11/18/85	
		E	REV DOC ERROR	3454T	12/6/85	
		F	ADD C201 47μF	3503T	1/6/86	



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W, ±5%, RESISTANCE IS IN OHMS.
2. D502, D506 CONNECTED IN SERIES.

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION — DEC. INCH
ANGLES
CONTRACT NUMBER
DES.
DR. L. Yue DATE 4/4/86
CHK. DATE 7/4/85
ENGR. DATE 7/9/85
CUSTOMER APPROVAL

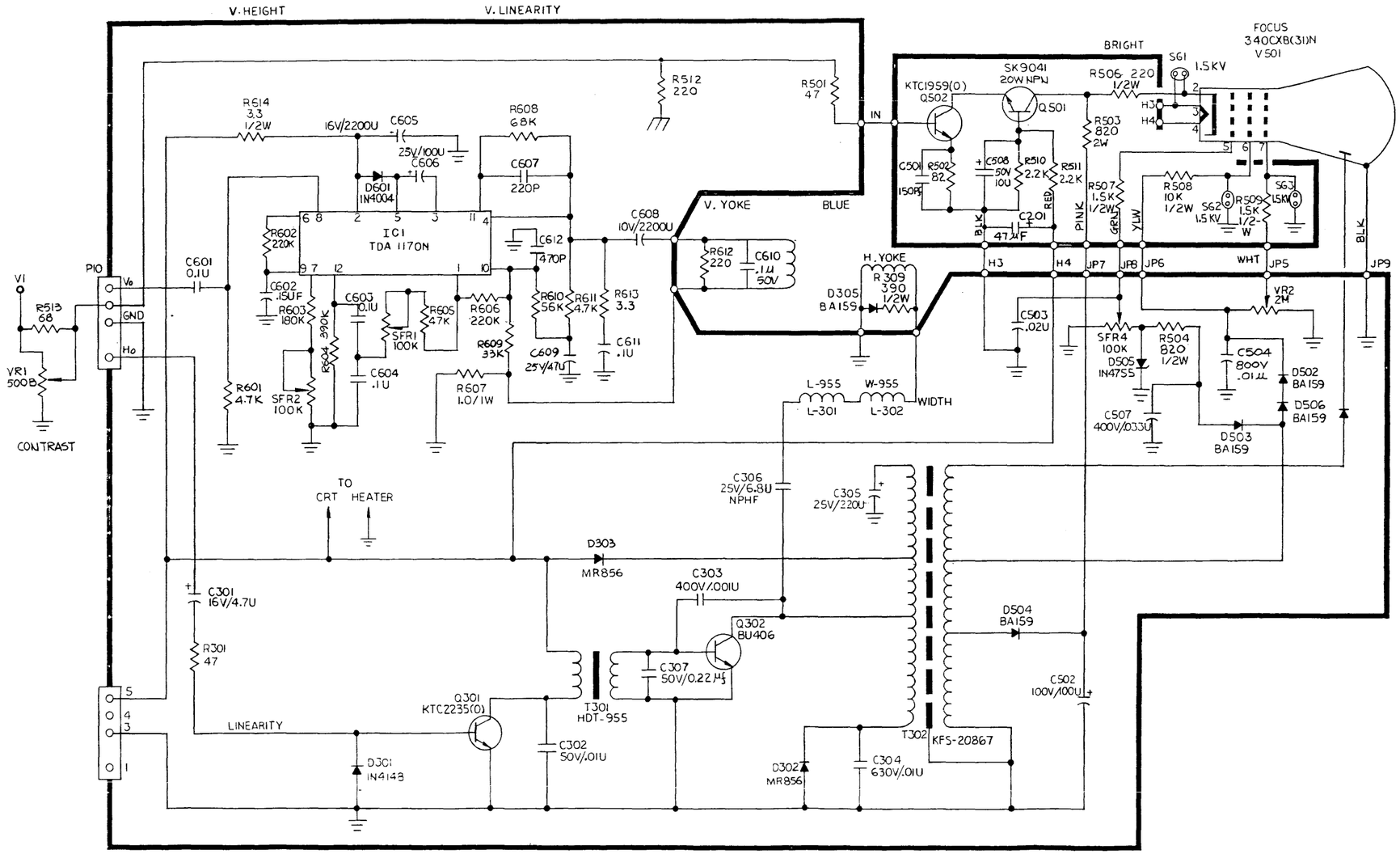
TeleVideo Systems, Inc.

PCB SCHEMATIC
955 VIDEO MONITOR

SIZE	CODE IDENT	REV
D	132326-00	F

SCALE — SHEET 1 OF 1

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
		A	PROD REL	2965T	7/18/85	
		B	ADD D505 AND R302	2927T	7/18/85	
		C	CHG R602 FROM 80K TO 200K	3118T	7/24/86	
		D	UPDATE VIDEO MON. ADD NOTE 2	3408T	9/17/86	
		E	REV DOC ERROR	3454T	11/6/86	
		F	ADD C201 47uF	3503T	1/12/87	
		F1	CHG DESCRIPTION	3568T	3/17/87	
		F2	Q501 WAS 2SC2911	3880	8/10/87	



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4 W ±5%. RESISTANCE IS IN OHMS.
2. D502, D506 CONNECTED IN SERIES.

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES

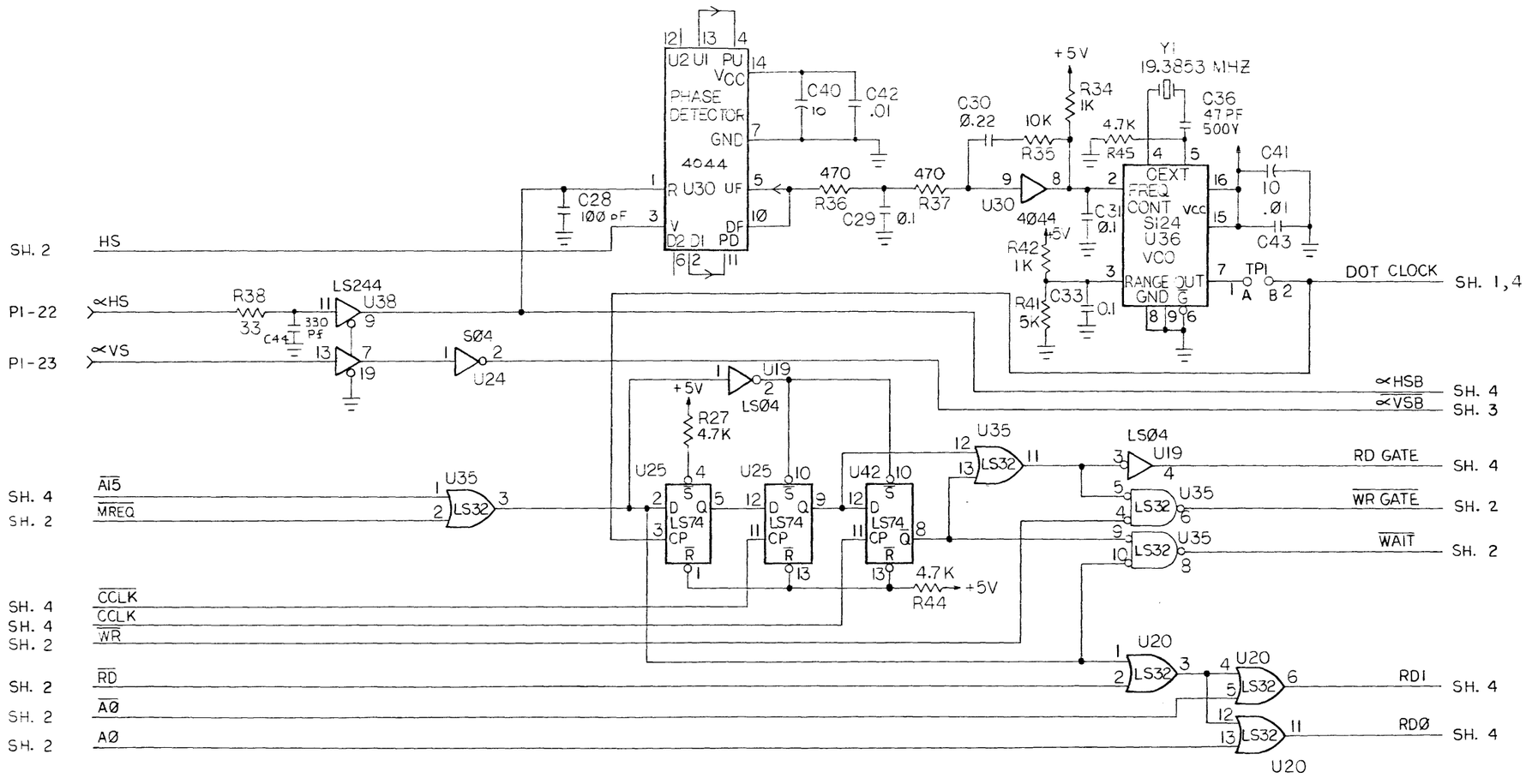
TOLERANCES UNLESS NOTED
DIMENSION IN INCH
ANGLES

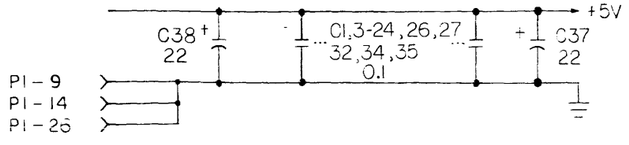
CONTRACT NUMBER
DES DATE
DR L Diaz DATE 7/9/85
CHK DATE 7/15/85
ENGR DATE 7/9/85
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.
PCB SCHEMATIC
VIDEO MONITOR 955/PCS1

SIZE	CODE IDENT		REV
D		132326-00	F2
SCALE		SHEET 1 OF 1	

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
		A	PRELIMINARY REL			
		A	PROD REL	3298T		
		B	ON SH.1, C36 47PF 500V WAS C36 20PF	3509T		





NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4W.
2. ALL CAPACITORS ARE VALUED IN MICROFARADS.
3. NOT USED: U39, C39, R46, R24, R40
4. HIGHEST DESIGNATIONS: U44, C43, R47

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION FRACT. DECIMAL
ANGLES
CONTRACT NUMBER
DES DATE
DR D LY 6-9-85
CHK DATE
ENGR DATE
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 GRAPHIC
SIZE D | CODE IDENT | 132123-00 | REV B
SCALE NONE | SHEET 1 OF 4

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASS'Y	FIRST USED ON					
			SEE SH. 1			

CPU/STI RST SH. 3
∝ READY SH. 3
DATINT SH. 3
A0 - A15 SH. 1,3,4
HS SH. 1
DISPEN SH. 4
DAT8-DAT15 SH. 4
DAT0 - DAT7 SH. 4
WR0 SH. 4
WR1 SH. 4
M1 SH. 3
RD SH. 1
IORQ SH. 3
MREQ SH. 1
D0-D7 SH. 3,4
RDINT SH. 3
A0 SH. 1

P1-24 ∝D7
P1-18 ∝D6
P1-15 ∝D5
P1-16 ∝D4
P1-13 ∝D3
P1-12 ∝D2
P1-11 ∝D1
P1-10 ∝D0

R25 100
U21 74LS374
U22 74LS374
U23 74LS374
U37 74LS05
U37 7406
U38
U31 74LS139
U32 LS74
U20 LS32
U19 LS04
U24 S04
U33 S32
U1 68B45
U3 Z80B GMHZ CPU
U9 LS157
U11 LS157
U10 LS157
U12 LS157
U13 2064P-10
U14 2064P-10
U15 2064P-10
U16 2064P-10

P1-17 ∝WR
P1-3 ∝A0
P1-25 ∝RD
SH. 3 Z8RD
SH. 3 CRTCS
SH. 3 CRTRST
SH. 4 CCLK
P1-4 GRAPH SEL
P1-6 ∝A7
SH. 3 Z8WR
P1-8 IRQ
SH. 3 PRNTR/MODM
SH. 1 WR
SH. 3 CPUINT
SH. 1 WAIT
SH. 4 Z8CLK
SH. 4 CCLK
SH. 1 WRGATE
SH. 3 Φ

+5V
R39 4.7K
R30 4.7K
R48 4.7K
R11 150
R3 4.7K
R2 4.7K
R13 4.7K
R4 10K
R9 22
R8
R29 1K
R10 220
C25 47pF
Q1 2N2907
R14 100
R15 100
R16 100
R17 100

W3

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION THIS IS INCH
X = ±
XX = ±
XXX = ±
ANGLES ±

CONTRACT NUMBER
DES
DR D LY 2-9-55 DATE
CHK DATE
ENGR DATE
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 GRAPHIC
SIZE D | CODE IDENT 132123-00 | REV B
SCALE NONE | SHEET 2 OF 4

DATARICH PRINT RECORDER NO. 44482

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON		SEE SH. 1			

+5V RP1 RP2 4.7K

SH. 2 A0 - A15
SH. 2 Φ
SH. 2 ∝VSB
SH. 1 DATINT
SH. 2 WR
SH. 2 RD
SH. 2 IORQ
SH. 2 M1
SH. 2 CPU/STI RST

SH. 4 H1
SH. 2 MREQ

U41 LS86 U43 LS32 U29 LS139 U40 LS08

U6 6116 R7 100

U5 27128 W1 W2

U4 2764

R1 100K CR1 IN914 C2 0.01 +5V R6 4.7K R5 4.7K

STICE

A0 - A15
Φ
∝VSB
DATINT
WR
RD
IORQ
M1

Z8WR SH. 2
Z8RD SH. 2
GI/O SEL SH. 4
CRTCS SH. 2

R12 10K

U2 STI

INT → CPUINT SH. 2
I5 ← CRTRST SH. 2
I4 ← RDINT SH. 2
I3 → GRDISPEN SH. 4
I2 ← PI-21
I1 ← ∝READY SH. 2
I0 → 8 PRNTR/MCDM SH. 2
SI ← 38
SO → 37
TAO → 1
TCO → 3
TDO → 4
IEO → 18
TBC ← 2

RP3 +5V

SH. 2 D0 - D7

P3-3 R47 4.7K P3-4 +5V MOUSE CONN. P3-5

U19 LS04 U19 LS04

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MATERIAL / FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION mm / INCH
ANGLES
CONTRACT NUMBER
DES
DR D LY 2-9-35
CHK
ENGR
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 GRAPHIC
SIZE D | CODE IDENT | 132123-00 | REV B
SCALE NONE | SHEET 3 OF 4

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON		SEE SH. 1			

SH. 2 D0 – D7

U7 LS373 U8 LS244 U18 LS373 U17 LS244

SH. 1 RDGATE
SH. 1 RD0
SH. 1 RDI
SH. 1 DAT 8 – 15
SH. 2 WR0
SH. 2 WRI
SH. 2 DAT0-7

+5V

U27 74166 (HIGH BYTE)
R22 47K
R23 330
R21 330
SI
INH
QH

HIGH BYTE

LOW BYTE

U26 74166
R20 4.7K
330 R19

U28
VCC
CRTCS 20
BUFF EN 17
CONTROL 22
GRPH CURS 4
HSYNC 16
GI/O SEL 19
A3 21
A2 23
A1 1
A0 GATE ARRAY IOA
BLINK CLK 6
GMEM SEL 18
DISPEN 7
DOT CLOCK 9
CCLK
GND 12

SH. 1 ≪HSB
SH. 3 GI/O SEL
SH. 2 A3
SH. 2 A2
SH. 2 A1
SH. 3 HI 5V R43 4.7K
SH. 2 A15
LS86 U41
SH. 1 DOT CLOCK

R26 4.7K
U44 74S163 TC
W5
U24 S04
R32 4.7K
U34 LS 74
U33 S32
R18 4.7K
U41 LS 86
U40 LS08
W4
U41 LS86
1K R28
U34 LS 74
4.7K R33
-5V

TTL VIDEO → P1-20
U24 S04
CCLK → SH. 1,2
CCLK → SH. 1,2
Z8CLK → SH. 2
A15 → SH. 1
SH. 2 DISPEN
SH. 3 GRDISPEN

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MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION THIS INCH
ANGLES

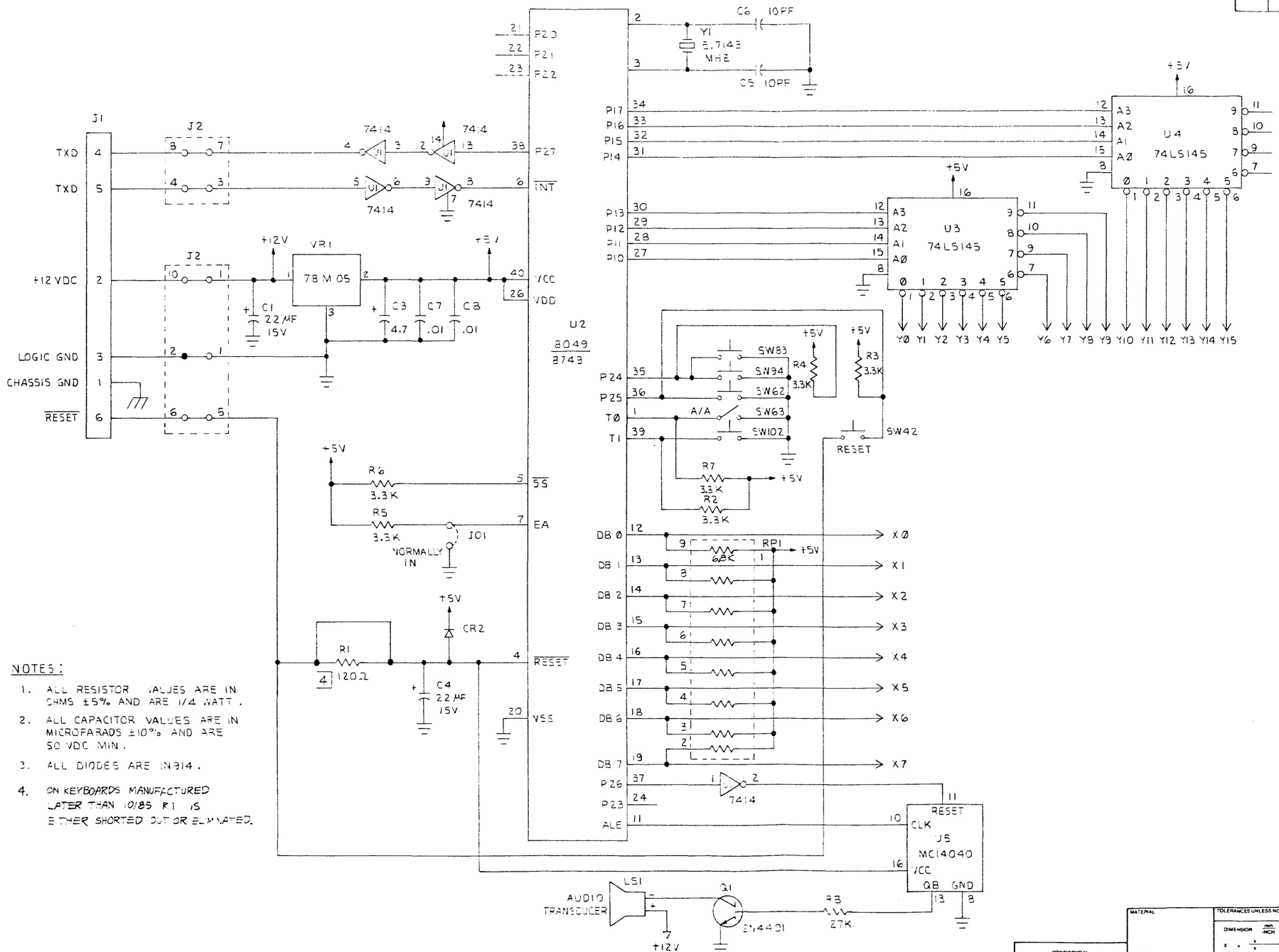
CONTRACT NUMBER
DES DATE
DR D LY 2-9-85 DATE
CHK DATE
ENGR DATE
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.
PCB SCHEMATIC DIAGRAM
955 GRAPHIC

SIZE	CODE IDENT		REV
D		132123-00	3
SCALE	NONE	SHEET 1 OF 1	

8 7 6 5 4 3 2 1
D C B A

APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
		A	PROD REL	B285	8/31	



NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS ±5% AND ARE 1/4 WATT.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS ±10% AND ARE 50 VDC MIN.
3. ALL DIODES ARE 1N914.
4. ON KEYBOARDS MANUFACTURED LATER THAN 10/85 R1 IS EITHER SHORTED OUT OR ELIMINATED.

DISTRIBUTION POST RELEASE NO 83887

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED
DIMENSION mm / INCH
X ± ±
XX ± ±
XXX ± ±
ANGLES ±

CONTRACT NUMBER
DES DATE
DR DATE 8/31/85
CHK DATE
ENGR DATE
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.

955 / 925 / 970 HI TEK.
KYBD PCB SCHEMATIC

SIZE	CODE IDENT	131438-00	REV
D			A

SCALE ~ SHEET 1 OF 2

APPLICATION		REVISION	DESCRIPTION	ECO NO	DATE	APPROVED
NEXT ASSY	FIRST USED ON					
			SEE SHT 1			

Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 Y9 Y10 Y11 Y12 Y13 Y14 Y15

X0 SW1 F1 | SW3 F3 | SW103 SPACE BAR | SW2 F2 | SW5 F5 | SW104 Home | SW74 " ' | SW31 < , | SW55 Line Feed | SW38 Char Delete | SW19 Line Erase | SW17 Char Insert | SW30 ó

X1 SW22 Loc Esc | SW24 @ 2 | SW66 D | SW25 # 3 | SW49 Y | SW53 P | SW50 U | SW106 ↓ | SW32 O | SW97 CE | SW57 Clear Space | SW60 9 | SW77 Tab

X2 SW82 back Tab | SW64 A | SW23 ^ 6 | SW23 ! 1 | SW67 F | SW88 B | SW89 N | SW34 + = | SW37 back Space | SW58 7 | SW96 Del | SW100 3 | SW109 Ø | SW61 —

X3 SW101 Print | SW85 X | SW68 G | SW65 5 | SW26 $ 4 | SW29 & 7 | SW92 > . | SW71 K | SW14 F14 | SW73 : ; | SW15 F15 | SW18 Line Insert | SW41 Page | SW78 4 | SW21 Send

X4 SW43 Tab | SW45 W | SW86 C | SW6 F6 | SW69 H | SW13 F13 | SW31 (9 | SW35 ~ ` | SW32) Ø | SW36 ! \ | SW98 1 | SW76 Break | SW111 · | SW39 Line Delete

X5 SW84 Z | SW48 T | SW46 E | SW27 % 5 | SW9 F9 | SW10 F11 | SW11 F10 | SW95 } { | SW40 Erase Page | SW105 ← | SW81 > | SW79 5

X6 SW44 Q | SW87 V | SW7 F7 | SW30 * 8 | SW12 F12 | SW51 I | SW107 ↑ | SW33 _ | SW39 2 | SW75 Return | SW20 Set UP / No Scroll | SW110 ØØ

X7 SW47 R | SW8 F8 | SW4 F4 | SW70 J | SW54] [| SW90 M | SW93 ? | SW72 L | SW16 F16 | SW108 → | SW112 Enter | SW59 8

SW XX

X

SWITCH ORIENTATION

MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES UNLESS NOTED
DIMENSION — INCH
X = ±
XX = ±
XXX = ±
ANGLES ±

CONTRACT NUMBER
DES DATE
DR DATE 2/14/
CHK DATE
ENGR DATE
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL

TeleVideo Systems, Inc.

955 / 965 / 970 HI TEK KYBD PCB SCHEMATIC

SIZE	CODE IDENT	DWG NO	REV
D		131438-00	A

SCALE ~ SHEET 2 OF 2

DRAWING POST REORDER NO 83067

ORDERING SPARE PARTS

You can order spare parts by telephone*, telex or by written purchase order. To place an order, contact the TeleVideo Regional Sales Office in your area, or contact our Corporate Spare Parts Order Entry Department at the following address:

TeleVideo Systems, Inc.
1170 Morse Avenue
P.O. Box 3568
Sunnyvale, CA 94088-3568

or call

Sunnyvale:	408-745-7760
Telex:	474-5041 TVISYS
Fax:	408-734-1927
TWX	910-338-7633

All orders are shipped F.O.B. our designated site.

*All telephone orders must be followed by a confirming purchase order clearly marked "Confirming Purchase Order".

Order parts by contacting the TeleVideo Regional Sales Office in your area, or contacting our Spare Parts Order Entry Department.

Table 3-1
955 Terminal Spare Parts List

MAJOR MODULES

Part Number	Description	List Price	Rec. Qty.
*132160-00	LOGIC BOARD	417.40	1
*132880-00	ENHANCED GATE ARRAY LOGIC BD.	250.00	1
*132325-00	VIDEO MONITOR BOARD	50.00	1
*132324-00	POWER SUPPLY	80.00	1
*130945-00	KEYBOARD ASSEMBLY	92.00	1
*122187-00	TUBE CRT 14" GREEN	85.00	1
*131747-00	TUBE CRT 14" AMBER	85.00	1

PCB ASSEMBLY LOGIC BOARD

NOTE: Determine whether you have a gate array logic board or an enhanced gate array board before ordering the shift register, gate array chip or static RAM chips. See page 3-3 for enhanced gate array part numbers.

Part Number	Description	List Price	Rec. Qty.
*130236-00	IC MICROPROCESSOR 65C02 3-MHZ	26.00	4
*121387-00	IC 2K x 8 CMOS STATIC RAM	14.00	4
*131405-00	IC GATE ARRAY TVI 16	42.31	5
131612-00	IC 74AS194 4-BIT SHIFT REG	5.00	
*180002-78**	IC SYSTEM EPROM 2764	35.00	4 sets
*180002-79**	IC SYSTEM EPROM 2764	32.00	4 sets
*180002-88**	IC SYSTEM EPROM 27128	32.00	4 sets
*180002-91**	IC SYSTEM EPROM	32.00	4 sets

*TeleVideo recommends dealers stock the quantity indicated per 100 units.

**Before ordering, check the part number on the EPROM(s). You must replace the EPROM(s) with the same type and combination you removed. The three possible combinations are:

1. Two 2764 EPROMs (P/N 180002-78; P/N 180002-79)
2. One 27128 EPROM - P/N 180002-88
3. P/N 180002-91; P/N 180002-88

Table 3-1 (Continued) - 955 Terminal Spare Parts List

PCB ASSEMBLY LOGIC BOARD

Part Number	Description	List Price	Rec. Qty.
*120530-00	IC SY6551A/1 2-MHZ SYN/AMI	6.00	2
*130234-00	IC 2674 AVDC 4-MHZ	28.00	4
*180002-26	IC ROM 955 CHAR GEN	35.00	2
*131154-00	CRY 19.3396-MHZ OSC	8.00	2 sets
*131155-00	CRY OSC 31.684-MHZ	17.00	2 sets
*131386-00	BATTERY LITHIUM CYLINDER	6.00	2

ENHANCED GATE ARRAY LOGIC BOARD

*270947-00	IC GATE ARRAY TSI-19	30.00	1

PCB ASSEMBLY VIDEO MONITOR BOARD

*242816-00	TRANS FLYBACK KFS-20867	14.00	1

*TeleVideo recommends dealers stock the quantity indicated per 100 units.

Table 3-1 (Continued) - 955 Terminal Spare Parts List

ADDITIONAL PARTS

Part Number	Description	List Price	Rec. Qty.
*131219-00	KEYCAP KIT	20.00	1
131158-00	KEYSWITCH NONLOCKING	3.00	
131159-00	KEYSWITCH NONLOCKING MAR	3.00	
131157-00	KEYSWITCH LOCKING	4.00	
122911-00	PWR CORD 3-COND SHLD 10A 125V	10.00	
122161-00	CBL ASY 6 CONDUCTOR RJ12	10.00	
132165-00	BEZEL	9.00	
132166-00	REAR HSG	19.60	
132155-00	BASE PEDESTAL	6.40	
132143-00	OUTER SHIPPING CARTON	15.00	
132144-00	SHIPPING CARTON STYROFOAM RT	15.00	
132145-00	SHIPPING CARTON STYROFOAM LEFT	15.00	
131969-00	OPERATOR'S MANUAL 955	20.00	
131968-00	MAINTENANCE MANUAL 955	50.00	

PRICES ARE SUBJECT TO CHANGE WITHOUT NOTICE

*TeleVideo recommends dealers stock the quantity indicated per 100 units.

Table 3-2
955 Parts Reference List

NOTE: NOT ALL PARTS LISTED IN TABLE 3-2 WILL BE STOCKED BY TELEVIDEO

MAJOR MODULES

Part Number	Description
132160-00	LOGIC BOARD
132880-00	ENHANCED GATE ARRAY LOGIC BOARD
132325-00	VIDEO MONITOR BOARD
132324-00	POWER SUPPLY
130945-00	KEYBOARD ASSEMBLY
122187-00	TUBE CRT 14" GREEN
131747-00	TUBE CRT 14" AMBER

PCB ASSEMBLY LOGIC BOARD

Determine whether you have a gate array logic board or an enhanced gate array logic board, then refer to the appropriate parts list (page 3-5 for the gate array; page 3-7 for the enhanced gate array.

PCB ASSEMBLY GATE ARRAY LOGIC BOARD - PART NUMBER 132160-00

Part Number	Description	Location
130236-00	IC MICROPROCESSOR 65C02 3-MHZ	U1
120272-00	IC 74LS139 2X 1 OF 4 DECODER	U2
120292-00	IC 75188N 4X LINE DRIVER	U3, 12
180002-78*	IC SYSTEM EPROM 2764	U4
180002-79*	IC SYSTEM EPROM 2764	U5
180002-88*	IC SYSTEM EPROM 27128	U4
180002-91*	IC SYSTEM EPROM	U5
121387-00	IC 2K x 8 CMOS STATIC RAM	U6
120294-00	IC 75189A 4X LINE RECEIVER	U7, 8
120530-00	IC SY6551A/1 2-MHZ SYN/AMI	U9, 10, 11
120242-00	IC 74LS00 4X 2-IN NAND GATE	U13, 39
130234-00	IC 2674 AVDC 4-MHZ	U14

*Before ordering, check the part number on the EPROM(s). You must replace the EPROM(s) with the same type and combination you removed. The three possible combinations are:

1. Two 2764 EPROMs (P/N 180002-78; P/N 180002-79)
2. One 27128 EPROM - P/N 180002-88
3. P/N 180002-91; P/N 180002-88

Table 3-2 (Continued) - 955 Parts Reference List

PCB ASSEMBLY GATE ARRAY LOGIC BOARD - PART NUMBER 132160-00

Part Number	Description	Location
120376-00	IC 74LS273 8X D-TYPE FF	U15
120274-00	IC 74LS157 4X2-IN DATA SEL/MLT	U16, 17, 21, 22
120362-00	IC 74LS245, N8T245N	U18, 20
131609-00	IC 74HC04 HEX INVERTER	U19
120258-00	IC 74LS32 4X 2-IN OR GATE	U23, 27, 46, 47
120416-00	IC 74LS02 4X 2-IN NOR GATE	U24
131634-00	IC STATIC RAM 8K x 8 100ns.	U25, 31
131615-00	IC STATIC RAM 2K x 8 100ns.	U25, 26, 30, 31
120348-00	IC 7406 6X INVTR BFR/DRVR	U28
131614-00	IC 8211 PROG VOLT REG	U29
120290-00	IC 74LS374 8X D-TYPE FF	U32, 33, 35
131405-00	IC GATE ARRAY TVI 16	U34
131612-00	IC 74AS194 4-BIT SHIFT REG	U36, 37, 42
120266-00	IC 74LS74 2X D-TYPE E-TRIG FF	U38
131611-00	IC 74AS163 SYNC 4-BIT COUNTER	U40
120456-00	IC 74S51 AND-OR INVTR GATE	U41
120388-00	IC 74S32 4X 2-IN POS OR GATE	U43
120252-00	IC 74LS08 4X 2-IN AND GATE	U44
180002-26	IC ROM 955 CHAR GEN	U45
120246-00	IC 74S04 6X INVTR	U48
131551-00	TRAN 2N4264 NPN	Q1-3
120469-00	TRAN 2N2222A NPN/SILICON	Q4
131154-00	CRY 19.3396-MHZ OSC	Y1
131155-00	CRY OSC 31.684-MHZ	Y2
122168-00	CRY 3.6864-MHZ	Y3
131386-00	BATTERY LITHIUM CYLINDER	B1
121440-00	RES CF 82 OHM 1/4W 5%	R1-5, 9, 10, 13, 24
120517-00	RES CF 470 OHM 1/4W 5%	R6
120521-00	RES CF 1000 OHM 1/4W 5%	R7, 12, 14, 28, 34
120533-00	RES CF 180 OHM 1/4W 5%	R8
120381-00	RES CF 4.7 OHM +/-5%	R11
126182-00	RES MF 22K OHM 1/4W +/-1%	R15
120531-00	RES CF 4700 OHM 1/4W 5%	R16, 21, 23, 25, 26, 36, 37
120341-00	RES CF 10K OHM 1/4W 5%	R17, 35
126184-00	RES MF 1M OHM 1/4W +/-1%	R18
131829-00	RES MF 71.5K OHM 1/4W 1%	R19
120337-00	RES CF 47K OHM 1/4W 5%	R20, 27
120371-00	RES CF 680 OHM 1/4W 5%	R29
120413-00	RES PK 4.7K OHM 10P SIP	RP1
120427-00	RES PK 1K OHM 8P SIP	RP2
120429-00	RES PK 4.7K OHM 8P SIP	RP4
130177-00	CAP TANT 4.7uF 16V +/-20%	C2, 114

Table 3-2 (Continued) - 955 Parts Reference List

PCB ASSEMBLY GATE ARRAY LOGIC BOARD - PART NUMBER 132160-00

Part Number	Description	Location
130172-00	CAP GL PK .1uF 25V +80%	C3, 6, 7, 100-105, 108-110, 112, 116, 118, 124, 126-129, 131, 132
130190-00	CAP GL PK .001uF 25V +80 -20	C5
130175-00	CAP ELEC 22uF 16V +80%	C9, 11-13
130173-00	CAP GL PK 330pF 25V +/-20%	C14-20, 24-27, 34-36
130183-00	CAP GL PK 100pF 50V +/-10%	C21, 38
130176-00	CAP ELEC 10uF 16V +80%	C28-30
130179-00	CAP GL PK 47pF 50V	C31, 33, 40, 47
120279-00	CAP ELEC 1uF 16V 10%	C37
120251-00	CAP MICA 150pF 500V 1%	C43, 45
120301-00	CAP CER .1uF 50V 10%	C106, 107, 111, 113, 115, 117, 119-123, 125, 130, 134, 135, 136, 137, 138
120475-00	DIODE 1N914	CR3, 5-7, 9-11
131746-00	DIODE 1N5817 SCHOT BAR RECT 1A	CR8

ENHANCED GATE ARRAY LOGIC BOARD - PART NUMBER 132880-00

Part Number	Description	Location
131614-00	IC 8211 PROG VOLT REG	U2
123620-00	IC 74LS132 4X 2-IN NAND SCHMITT	U3
130236-00	IC 65C02 MICROPROCESSOR 3 MHZ	U4
120294-00	IC 75189A 4X LINE RECEIVER	U5, 9
120348-00	IC 7406 INVERTER BFR/DRVR	U7, 40
120252-00	IC 74LS08 4X 2-IN AND GATE	U8, 42
120258-00	IC 74LS32 4X 2-IN OR GATE	U11, 24, 34, 43
120292-00	IC 75188 4X LINE DRIVER	U13, 17
180002-88	IC SYSTEM EPROM CO-FF	U14
180002-91	IC CALCULATOR EPROM	U15
270992-00	IC STATIC RAM 2K X 8 CMOS 150ns	U16
120388-00	IC 74S32 4X 2-IN POS OR GATE	U18
120272-00	IC 74LS139 2X 1 OF 4 DECODER	U19
120530-00	IC SY6551A/1 2 MHZ SYN/AMI	U20-22
120276-00	IC 74LS163 SYN 4-BIT COUNTER	U23
120362-00	IC 74LS245, N8T245N	U25, 30
120274-00	IC 74LS157 4X 2-IN DATA SEL/MLT	U26, 27, 31, 32
130234-00	IC 2674 AVDC 4 MHZ	U28
131609-00	IC 74HC04 HEX INVERTER	U29
120290-00	IC 74LS374 8X D-TYPE FLIP-FLOP	U33, 47

Table 3-2 (Continued) - 955 Parts Reference List

ENHANCED GATE ARRAY LOGIC BOARD - PART NUMBER 132880-00

Part Number	Description	Location
270958-00	IC STATIC RAM 8K X 8 100ns CMOS	U36, 45
270947-00	IC GATE ARRAY TSI-19	U37
270737-00	IC 74F166 8X SHIFT REGISTER	U38
120376-00	IC 74LS273 8X D-TYPE FF	U39
120248-00	IC 74LS04 6X INVERTER	U44
180002-26	IC CHARACTER GENERATOR	U46
120266-00	IC 74LS74 2X D-TYPE E-TRIGGERED FLIP-FLOP	U48
131386-00	BATTERY LITHIUM CYLINDER	B1
131746-00	DIODE 1N5817 SCHOT BAR RECT 1A	CR1, 4, 5, 9
120475-00	DIODE 1N914	CR2, 3, 6-8
120469-00	TRAN 2N2222A NPN/SILICON	Q1
131551-00	TRAN 2N4264 NPN	Q2, 4
122168-00	CRYSTAL 3.6864 MHZ	Y1
131154-00	CRYSTAL 19.3396 MHZ OSC	Y2
131155-00	CRYSTAL OSC 31.684 MHZ	Y3
120531-00	RES CF 4700 OHM 1/4W 5%	R1, 7, 8, 10 17, 18, 22, 23, 28, 44, 45, 50, 51, 55, 56, 59, 61, 62
126184-00	RES MF 1M OHM 1/4W +/- 1%	R2
131829-00	RES MF 71.5K OHM 1/4W 1%	R3
126182-00	RES MF 22K OHM 1/4W +/- 1%	R4
120337-00	RES CF 47K OHM 1/4W 5%	R5
120521-00	RES CF 1000 OHM 1/4W 5%	R6, 11-13, 15, 25, 26, 30, 32-37, 39, 41, 42, 52-54, 57
120341-00	RES CF 10K OHM 1/4W 5%	R9
120371-00	RES CF 680 OHM 1/4W 5%	R14
121440-00	RES CF 82 OHM 1/4W 5%	R19, 21, 43, 47, 48, 49, 29
270414-00	RES CF 2.2M OHM 1/4W	R24
121770-00	RES CF 820 OHM 1/2W 5%	R27
120517-00	RES CF 470 OHM 1/4W 5%	R31
120533-00	RES CF 180 OHM 1/4W 5%	R38
120381-00	RES CF 4.7 OHM +/- 5%	R40
120365-00	RES CF 240 OHM 1/4W 5%	R46
120373-00	RES CF 27K OHM 1/4W 5%	R60
120429-00	RES PK 4.7K OHM 8-PIN SIP	RP1
130175-00	CAP ELECT 22uF 16V +80%	C1, 82, 87, 88
130172-00	CAP GL PK .1uF 25V +80%	C3
120251-00	CAP MICA 150 pF 500V	C4, 20
130179-00	CAP GL PK 47pF 50V	C5, 7, 27, 53

Table 3-2 (Continued) - 955 Parts Reference List

ENHANCED GATE ARRAY LOGIC BOARD - PART NUMBER 132880-00

Part Number	Description	Location
130176-00	CAP ELECT 10uF 16V +80%	C6, 38
120301-00	CAP CER .1uF 50V 10%	C8, 9, 12, 22, 25, 28, 29, 35, 37, 39, 40, 42, 47-52, 55-62, 64-66, 68-72, 74-77, 79, 83, 85, 86, 89, 90, 92
130174-00	CAP GL PK .01uF 25V +80% -20%	C10
130183-00	CAP GL PK 100 pF 50V +/- 10%	C11, 19
130173-00	CAP GL PK 330pF 25V +/- 20%	C13-18, 30-34, 43-46, 73
120279-00	CAP ELEC 1uF 16V 10%	C26
130177-00	CAP TANT 4.7uF 16V +/- 20%	C67, 78

PCB ASSEMBLY VIDEO MONITOR BOARD - PART NUMBER 132325-00

270884-00	TRAN KTC 2235(0)	Q301
270883-00	TRAN BU406	Q302
120485-00	DIODE 1N4148 SWITCH	D301
241301-00	DIODE MR856	D302, 303
241300-00	DIODE BA159	D502-504, 506
270882-00	DIODE 1N4755	D505
122022-00	DIODE 1N4004 MOT	D601
242817-00	TRANS H DRIVE HDT-955	T301
242816-00	TRANS FLYBACK KFS-20867	T302
241020-00	COIL LINEARITY FIXED YEL DOT	L301
241021-00	COIL WIDTH W-955	L302
242000-00	IC VERT AMP TDA-117ON	IC1
120441-00	POT TRIM 100K OHM TOP-ADJ PCMT	SFR1, 2, 4
121801-00	POT FOCUS 2M OHM	VR2
120377-00	RES CF 47 OHM 1/4W +/-5%	R301, 501
131800-00	RES CF 22K OHM 1/4W 5%	R302
121770-00	RES CF 820 OHM 1/2W 5%	R504
120403-00	RES CF 220 OHM 1/4W 5%	R512
120531-00	RES CF 4700 OHM 1/4W 5%	R601, 611
240102-00	RES CF 180K OHM 1/4W	R603
240104-00	RES CF 220K OHM 1/4W	R602, 606
240103-00	RES CF 390K OHM 1/4W	R604
120337-00	RES CF 47K OHM 1/4W 5%	R605
240108-00	RES MF 1.0 OHM 1W	R607
131502-00	RES CF 68K OHM 1/4W +/- 5%	R608
249700-01	RES CF 33K OHM 1/4W	R609
240105-00	RES CF 56K OHM 1/4W	R610
240106-00	RES CF 3.3 OHM 1/4W	R613
240107-00	RES CF 3.3 OHM 1/2W	R614
121967-00	CAP ELEC 4.7uF 16V	C301

Table 3-2 (Continued) - 955 Parts Reference List

PCB ASSEMBLY VIDEO MONITOR BOARD - PART NUMBER 132325-00

Part Number	Description	Location
249017-00	CAP PF 0.01uF 50V	C302
240910-00	CAP PF 0.001uF 400V	C303
241124-00	CAP PP .01uF 630V	C304
130127-00	CAP ELEC 220uF 25V	C305
249032-00	CAP ELECT 6.8uF 25V NON-POL	C306
240909-00	CAP PF 0.22uF 50V	C307
130827-00	CAP ELEC 100uF 100V RADIAL LDS	C502
130186-00	CAP CER .02uF 50V	C503
270880-00	CAP MF .01uF 800V 10% RAD	C504
130126-00	CAP PF .033uF 400V	C507
240907-00	CAP PF 0.1uF 50V	C601, 603, 604, 611
240908-00	CAP PF 0.15uF 50V	C602
249015-00	CAP ELEC 2200uF 16V	C605
249003-00	CAP ELECT 100uF 25V	C606
121959-00	CAP CER 220pF 50V	C607
121962-00	CAP ELEC 2200uF 10V	C608
249027-00	CAP ELECT 47uF 25V	C609
240700-00	CAP CER 470pF 50V	C612

ADDITIONAL PARTS

131219-00	KEYCAP KIT
131158-00	KEYSWITCH NONLOCKING
131159-00	KEYSWITCH NONLOCKING MAR
131157-00	KEYSWITCH LOCKING
121700-00	IC 74LS145 (KYBD) (U3)
120455-00	TRANSISTOR 2N4401/2SC1166 (KYBD - Q1)
121390-00	KYBD CPU (8049) (U2)
122151-00	TRANSDUCER AUDIO (KYBD)
130948-00	HSG KEYBOARD TOP
130949-00	HSG KEYBOARD BOTTOM
132189-00	OVERLAY FUNCTION KEY 955 BLANK
123361-00	PWR CORD 3-COND SHLD 10A 125V
122161-00	CBL ASY 6 CONDUCTOR RJ12
132165-00	BEZEL
132166-00	HSG REAR
132155-00	BASE PEDESTAL
132143-00	OUTER SHIPPING CARTON
132144-00	SHIPPING CARTON STYROFOAM RT
132145-00	SHIPPING CARTON STYROFOAM LEFT
132195-00	FUSE HOLDER
122985-03	FUSE 1.5 AMP 250V SLOW BLOW (115V ONLY)
122985-01	FUSE .75 AMP 250V SLOW BLOW (230V ONLY)
132172-00	CONTRAST POT
132167-00	BRIGHTNESS KNOB
132158-00	PANEL REAR PEDESTAL
132441-00	CURRENT LOOP KIT
131969-00	OPERATOR'S MANUAL 955
131968-00	MAINTENANCE MANUAL 955

OVERVIEW

Determine the type of logic board in your terminal, then refer to the theory of operation that applies to your board.

For Gate Array models (part number 132160-00 - Gate Array location U34), read the information starting on page 4-1 .

For Enhanced Gate Array models (part number 132880-00 - Gate Array location U37), read the information starting on page 4-13 .

NOTE: You can determine the type of logic board by comparing the board to the illustrations in Section 2 of this manual.

GATE ARRAY LOGIC BOARD THEORY OF OPERATION

The terminal logic is based on a 65C02 8-bit microprocessor rated at 3 MHz, capable of addressing 65K bytes of memory.

Figure 4-1 shows a block diagram of the gate array logic board.

Refer to the schematic diagram in Section 2 while reading the Theory of Operation that follows.

Clock Circuit (See sheet 5 of the schematic)

The 955 has two display modes: 80-column and 132-column. Two clock oscillators (Y1 and Y2) accommodate the two modes. Y1 oscillates at 19.3396 MHz and serves as the basic clock in 80-column mode. Y2 oscillates at 31.084 MHz and serves as the basic clock in 132-column mode.

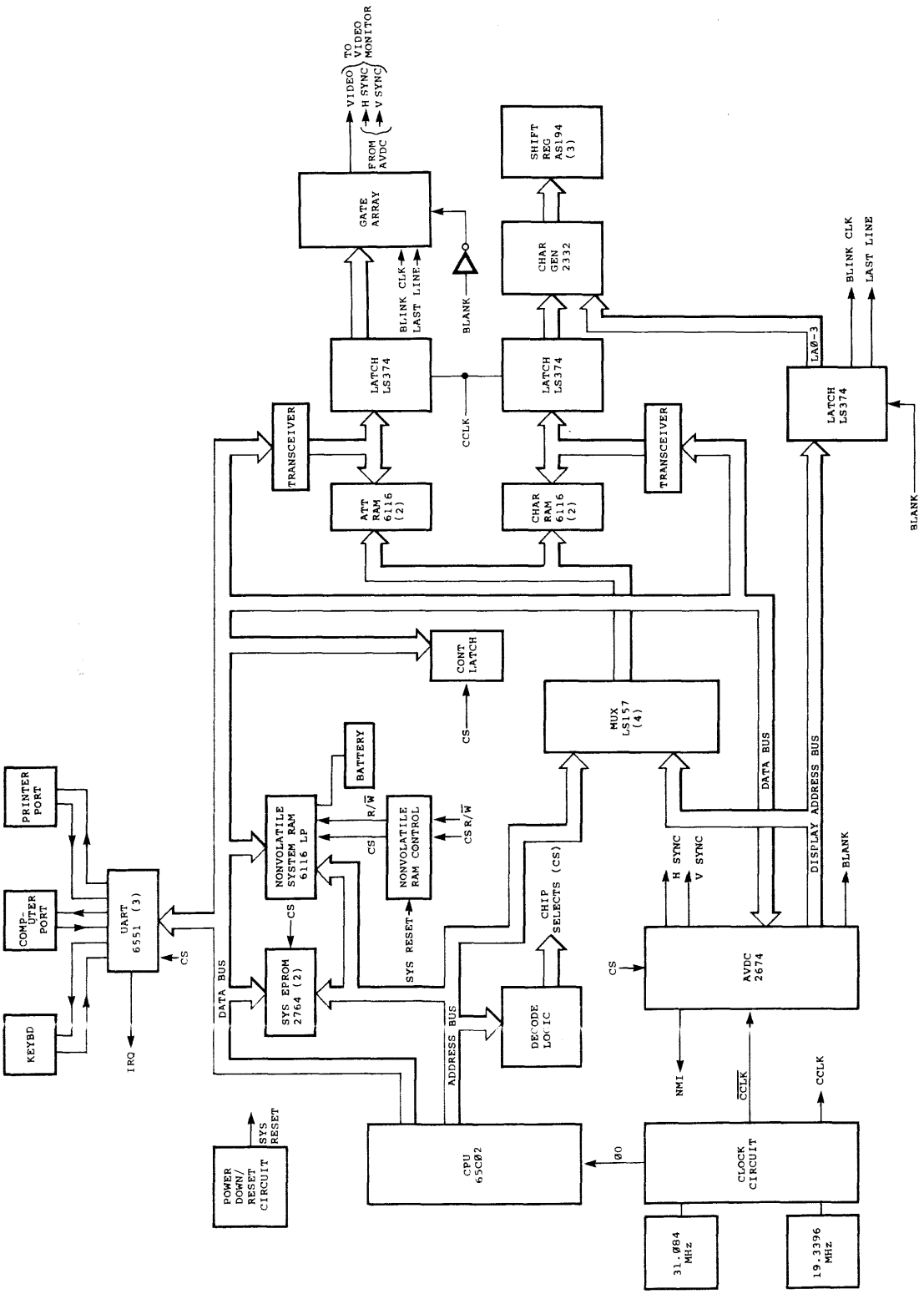
One half of U41 (a 74S51 AND/OR INVERT) selects Y1 or Y2. The level on the 80/132 line determines which oscillator's output appears at pin 6 of U41. This output, DOT CLOCK, serves two purposes: as a clock to shift video data through a shift register (see CHARACTER GENERATION, page 4-9) and as a clock for a divide-by-nine counter (U40). The 955's character cell is nine pixels wide; thus, the divide-by-nine counter.

U40 (74AS163) provides the basis for the CPU system clock and for the character clock used by the CRT controller (AVDC SCN2674 - U14).

The CRT controller uses the CCLK BAR* signal as the character clock. An inversion of this clock, CCLK, generates the CPU system clock or Phi zero (Ø0).

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

Figure 4-1
955 Block Diagram (Gate Array Logic Board)



The CPU system clock and character clock are synchronized and interleaved (see SCREEN DATA STORAGE, page 4-11). This allows the same clock to be used for system timing and for display generation.

Two considerations require CCLK to be modified for use as the system clock. They are: 1) the CPU's 3 MHz frequency limitation; and, 2) the requirement that any speed Universal Asynchronous Receiver Transmitter (UART) be used.

To overcome the CPU's speed limitation, CCLK is divided by 2 when in 132-column mode (see discussion in the next paragraph). To allow the use of any speed UART, the system clock is stretched out whenever the UARTs are accessed by the CPU (see discussion under Clock Stretch Timing).

In 132-column operation, the character clock is 31.084 MHz divided by 9, or 3.454 MHz. Dividing by 2 overcomes the CPU's 3 MHz frequency limitation while allowing the character and system clocks to be synchronized and interleaved. This is accomplished by half of U38 (a D-type flip-flop connected in toggle mode, thus dividing by 2). The Q BAR* output of U38 (pin 6) is connected to one input of the second section of U41 (74S51). The other input to U41 is CCLK.

In 132-column mode, the output of U38 is used for Phi zero; in 80-column mode, CCLK is used for Phi zero.

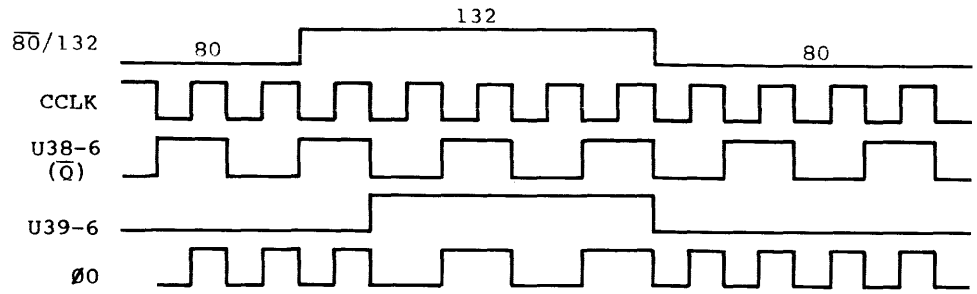
Clock Switching

Clock switching occurs in the following way. When the system clock is switched from 132-column mode (divide-by-2) to 80-column mode, or vice versa, the transition must occur during the inactive or low portion of the clock being switched to. Two gates of U39 are cross-connected to form a simple set/reset flip-flop. The outputs of the flip-flop control which clock is gated to the output of U41 (pin 8).

When the 80/132 line switches from low to high under system control (going to 132-column mode) the U39 flip-flop will not change state unless the Q output of U38 is high (Q BAR* is low). Conversely, when the 80/132 line switches from high to low, the U39 flip-flop will not change unless CCLK is low. This timing is illustrated in Figure 4-2.

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

Figure 4-2
Clock Switching



Clock Stretch Timing

Clock Stretch Timing occurs in the following sequence:

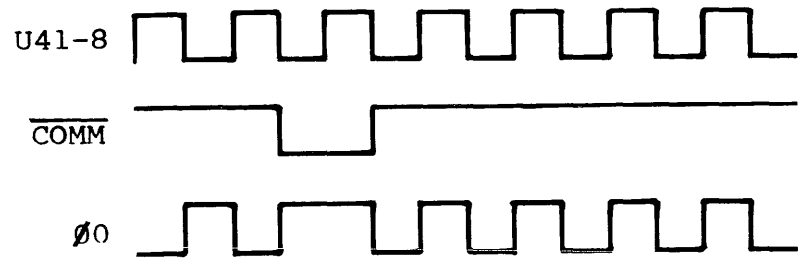
Using SYSTEM RESET BAR*, U38** is initialized with Q BAR* output high (pin 8). This gates the output of U41 directly through NAND gate U39 to be used for Phi zero. If the output of U41 is low and COMM BAR* (a CPU address bus decode that signifies a UART access) is low, a positive edge is provided to the clock input of U38. This causes the Q BAR* output to toggle low, which in turn holds Phi zero high.

COMM BAR* remains low as long as Phi zero is high, allowing the next negative transition of U41's output to toggle U38 again, which returns it to the initialized state. This timing is illustrated in Figure 4-3.

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

**The remaining half of U38 is connected in toggle mode.

Figure 4-3
CPU Clock Stretch Timing



The three other clocks provided by the clock circuitry are: DCC, DCC BAR* and Q1 BAR*.

DCC is used to load parallel character data into the video shift register (see Display Generation, page 4-10).

DCC BAR* is used to latch attribute data and display control signals into the gate array (see Display Generation, page 4-10).

Q1 BAR* is used to produce the signals necessary to properly write data into the character and attribute RAMs (see Screen Data Storage, page 4-11).

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

CPU System And Control (See sheets 1 and 2 of the schematic)

The CPU system consists of the CPU (65C02 - U1), the address bus decoder (74LS139 - U2, plus some gates), the system EPROMs (2764's - U4 and U5), system RAM (6116 LP4 - U6), the system reset circuit, and the control latch (74LS273 - U15).

The CPU is the controller for the entire board, initializing and controlling all of the UARTs, the CRT controller, the clock circuits and the video gate array. It also processes all of the data received from the keyboard, computer or printer, and updates the screen RAM accordingly.

Many of the display features, such as smooth scrolling and line lock, are controlled by the CPU in conjunction with the CRT controller.

Each device on the board has a specific address or range of addresses, as shown on the memory map (see Table 4-1).

The decoder chip (U2) provides the chip selects for all the devices on the memory map. Section one of this chip divides the 65K address range of the 65C02 into four 16K blocks.

The highest range block is used to select the system EPROMs, which contain the system firmware (a specialized operating system). The next lower 16K block is used for character RAM, which with attribute RAM (the next lower 16K block), is expandable to 16K bytes. The lowest 16K block is divided into four, 4K blocks by the second section of U2 and is allocated as follows.

The highest 4K block selects the optional system ROM, if it is installed. The next lower 4K block selects the CRT controller. The next lower 4K block selects the UARTs, graphics option board, and control latch. The lowest 4K block selects system RAM.

System RAM serves two purposes in the 955. Part of the RAM is used by the firmware as the stack and other temporary data stores, such as input and output buffers. In addition, the RAM is backed up by a battery, thus retaining the data even with power switched off. This allows portions of the RAM to be used for function key programming and to retain initialization parameters.

To retain data two things must occur: 1) the voltage to the RAM must not fall below 2 volts; and, 2) the RAM must be deselected as power from the power supply discharges.

Voltage is maintained by the battery (B1). Deselecting the RAM is accomplished by using a transistor (Q1) in series with the chip select signal from the decoder (see discussion in the next paragraph).

Table 4-1
Memory Map

FFFF F000	SYSTEM ROM
DFFF C000	SYSTEM ROM
BFFF 8000	CHARACTER RAM
7FFF 4000	ATTRIBUTE RAM
3FFF 3000	OPTION ROM
2FFF 2000	CRTC
18FF 1800	HOST UART
14FF 1400	PRINTER UART
12FF 1200	KEYBOARD UART
11FF 1100	CONTROL LATCH
10FF 1000	GRAPHICS OPTION
0FFF 0000	SYSTEM RAM

With power on, SYSTEM RESET BAR* is high, turning Q1 on and allowing the chip select signal to go to the RAM. When power goes away, the SYSTEM RESET BAR* signal goes low when +5 volts falls below 4.4 volts. This turns Q1 off, causing pin 18 of the RAM to follow the voltage at the junction of CR3 and R29. This voltage drops at the same rate as +5 volts until the battery voltage is reached (typically 2.8 to 3 volts), at which time the battery voltage takes over. As an added precaution, pin 21 of the RAM (WE BAR*) is also deselected during power down (Q2).

The CPU system uses the control latch to give the firmware control over some hardware devices that do not interface to the data bus. Starting with the Q0 output of U15, the control latch's output signals are:

DTR
Data Terminal Ready. A signal sent to the host computer telling it to stop transmitting data to the 955 (DTR high).

HIGH SPEED
Used to control the transmit and receive clock to the computer port UART. When this signal is high, the clock frequency is 3.6864 MHz; when it is low, the frequency is 1.8432 MHz. This allows for a maximum baud rate of 38.4 Kbaud in high-speed mode.

MODEM
Used only if an internal modem is installed in the 955. When this signal is low, the internal modem interfaces with the computer port UART; when it is high, the RS232 interface is used.

BOG/GOB
Connects to the video gate array and is used to control the normal background of the display. A low on this line provides a light background; a high produces a dark background.

LINE/PAGE ATT
Connects to the video gate array. Causes the selected attribute to carry to the end of the present character row (low) or to the end of the display (high).

EMB/NONEMB
Connects to the video gate array and controls the appearance of the attribute character. In embedded mode (space), the attribute character appears as a half-intensity space and prevents displaying data in the attribute character position. In nonembedded mode (no space) the attribute character does not appear and it is possible to display data at any location on the screen.

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

The reset circuit is shown on sheet 1 of the schematic. For the CPU to initialize properly, the RESET BAR* input (pin 40) must be held low for a minimum of six system clock cycles after voltage is at the operating level (4.75 volts minimum).

The node labeled SYSTEM RESET BAR* is controlled by the outputs of three devices: U29, U28 and Q4. Until the +5 volts reaches the operating level for these devices, their outputs are in a high-impedance state (not being driven to either a high or low state). During this period the node is held low by pull-down resistor R36.

When the voltage reaches the 1.6-volt level, U29 begins to drive the node low and continues to do so until the voltage gets above 4.6 volts. At the 2.2-volt level the output of U28 also begins to drive the node low and continues to do so until the level on pin 4 of U13 reaches the 2.2-volt level. This is delayed by the RC network consisting of R20 and C28. The result is that SYSTEM RESET BAR* is held low for 60 to 80 milliseconds after +5 volts reaches the 4.75-volt level.

When all the devices stop driving the node low, a high level is applied to the node through Q4, which serves as an active pull-up with a delayed response relative to +5 volts. This prevents the node from following +5 volts during the early stages of a power-up sequence (when +5 volts is lower than 1.6 volts).

At power-down the controlling device is U29. Its output is driven low when the supply goes below 4.4 volts. This is not necessary for proper operation of the CPU, but is critical for the integrity of the battery backed-up RAM.

Character Generation (See sheet 4 of the schematic)

The 955 uses character cells, rather than a full bit-mapped display, to produce characters on the screen. Each character cell is 9 pixels wide by 14 pixels high. The screen consists of either 3432 (132 x 26) character cells in 132-column mode, or 2080 (80 x 26) character cells in 80-column mode. Each of the 256 possible characters is pre-defined and resides in the character generator ROM (U45). The CPU changes the display by changing the code stored in the screen RAMs at the desired location(s).

The codes written into the screen RAMs are read out as the CRT controller refreshes the display (see Display Generation, page 4-10). As each code is read out, one per character clock cycle, it is latched into the character address latch (U32).

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

The outputs of the character address latch are used as the high-order address lines of the character generator ROM. The low-order addresses are provided by the scan line address latch (U33), which latches the line address outputs of the CRT controller. At the end of the character clock cycle, DCC (left side of sheet 4) goes high for one DOT CLK cycle.

With DCC high, the next rising edge of DOT CLK will load the D0 through D7 outputs of the character generator into a nine-bit shift register consisting of U36, U37 and U42 (74AS194 or 74S194). When DCC goes low again, the data is shifted out of the QC output of U42 (pin 13) until the complete byte has been shifted out. The output of the shift register (U42, pin 13) connects to the video gate array (U34), where it is combined with other signals to create the video signal to the video monitor board.

Under certain conditions, two of the shift register's inputs are connected to provide a character cell nine pixels wide without using a special 9-bit wide ROM. In normal text mode, D7 from the character generator is always a low (zero), creating a single dot space on the left side of each character cell. The DC input of U36 (pin 5), which becomes the dot on the right in the character cell, is loaded into the shift register as a low unless the D7 output of the character address latch (U32) is high.

If D7 is high, the DC input of U36 will be the same as the DD input of U36. This allows characters that need to use the entire width of the character cell, such as line drawing graphics, to do so.

Character address codes 00 through 7F cannot extend the entire width of the character cell; character codes 80 through FF can.

Display Generation (See sheets 3 and 4 of the schematic)

The video monitor board requires three signals from the logic board to produce a display on the CRT: vertical sync (VSYNC BAR*), horizontal sync (HSYNC), and video.

VSYNC BAR* and HSYNC originate from the CRT controller (U14). They are buffered and connect to the video board through pin 5 (VSYNC BAR*) and pin 1 (HSYNC) of P2. Video comes from the video gate array (U34). It goes through a NOR gate (U24) and a high-current open collector inverter (U28).

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

HSYNC and VSYNC BAR* are timed pulses derived by the CRT controller from internal programmable counters that count CCLK cycles. For example, HSYNC might be a positive-going pulse starting 80 CCLK cycles after the beginning of each scan line and lasting 16 CCLK cycles. The CRT controller's internal counter would reset at the beginning of each scan line, count to 80, set HSYNC high, count 16 more CCLKs and set HSYNC low.

VSYNC is a much slower signal based on scan lines. Another counter inside the CRT controller counts scan lines and toggles VSYNC according to the way the firmware has programmed the internal registers.

As the CRT controller (AVDC SCN2674 - U14) counts CCLKs, it is also putting out addresses on its display address lines (pins 21-34, DADD0-DADD13). These lines connect to four 74LS157 4-bit 2-way multiplexers (U16, U17, U21 and U22). The select inputs of the multiplexers are normally high, allowing the CRT controller's address line to access the data in the screen RAMs.

As data in the screen RAMs is read out, it is latched into the character address latch (U32) for the character data bus and into the video gate array for the attribute data bus.

The serialized character data (see Character Generation, page 4-9), is fed into the video gate array where it is combined with attribute data, the BLANK output of the CRT controller, the cursor output of the CRT controller, the screen background control (BOG/GOB) and other signals to produce a series of pulses that come out on the VIDEO output of the gate array.

If the VIDEO output is high, the electron beam in the CRT is turned on, producing a light dot or series of dots on the screen. If VIDEO is low, the screen is dark.

Screen Data Storage (See sheets 2 and 3 of the schematic)

If the CPU needs to access either the character or attribute RAMs, the corresponding signal, CHAR RAM BAR* or ATT RAM BAR* goes low for a full CPU cycle. Since the CPU clock can be running at half the speed of the character CCLK (see Clock Circuit, page 4-1), both of these signals are gated with CCLK BAR*.

When CCLK BAR* is low, the CRT controller is at the beginning of a character clock cycle and its address lines are not stable. However, during this period the CPU's address lines are stable and the CPU is either putting data on the data bus or is looking for data from the selected device.

Gating CHAR RAM BAR* and ATT RAM BAR* with CCLK BAR* and then ANDing the resulting signals produces a low on the select inputs

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

(pin 1) to the multiplexers during this period of the CPU cycle. This allows the CPU's address lines to drive the screen RAMs.

The outputs of the two gates used to gate CHAR RAM BAR* and ATT RAM BAR* with CCLK BAR* (74LS32, U46 pins 1-6) are connected to the CE BAR* inputs to U20 and U18. U20 and U18 are 8-bit transceivers used to isolate the CPU data bus from the character data bus and the attribute data bus (CD0-7 and AD0-7).

The direction control input to the transceivers (pin 1) is created by gating CCLK BAR* with R/W from the CPU (U46, pins 11-13). In this manner, the CPU can write data to or read data from the screen RAMs (either character or attribute) without interrupting or interfering with the CRT controller's process of refreshing the screen.

Communications (See sheet 6 of the schematic)

There are three serial communications channels. Each has its own dedicated UART and can send and receive data at speeds ranging from 50 to 19,200 bits per second (38,400 for the computer port).

U11 (6551A) is the UART used for communication to the host computer. It interfaces to a 25-pin D-subminiature connector (P3) via TTL to RS-232 level converters (U7 and U8, 1489's; U3 and U12, 1488's).

The baud rate is selectable under firmware control and is derived from the clock going in on pin 6 (XTAL 1). For the normal baud rate range of 50 to 19.2K, a 1.8432-MHz clock is used. When the 38.4K baud rate is selected, the firmware must also increase the clock input to 3.6864-MHz. It does this by using the HIGH-SPEED control line of the control latch (see CPU System and Control, page 4-6).

U10 is the UART dedicated to printer communications. It interfaces to a 25-pin D-subminiature connector (P4) via the same chips as U11. Its clock input is fixed at 1.8432 MHz, allowing the 50 to 19.2K baud range.

U9 is the UART used to communicate with the keyboard. Its clock input is also fixed at 1.8432 MHz and is capable of communicating at 50 to 19.2K baud. Since the keyboard's baud rate is 9600 baud, the firmware programs U9 to always communicate at this speed.

The IRQ BAR* outputs for all three UARTs are tied together in a wired OR configuration. When any of the UARTs generate an Interrupt Request (IRQ), the IRQ BAR* line goes low, signaling to the CPU that an interrupt has occurred. The CPU then polls the UARTs to determine which one generated the interrupt, and processes the interrupt as required.

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

ENHANCED GATE ARRAY LOGIC BOARD THEORY OF OPERATION

The terminal logic is based on a 65C02 8-bit microprocessor rated at 3 MHz, capable of addressing 65K bytes of memory.

Figure 4-4 shows a block diagram of the enhanced gate array logic board.

Refer to the schematic diagram in Section 2 while reading the Theory of Operation that follows.

Clock Circuit (see sheets 1, 2, 3, and 4 of the schematic)

The 955 has two display modes: 80-column and 132-column. Two clock oscillators (Y2 and Y3) accommodate the two modes. Y2 oscillates at 19.3396 MHz and serves as the basic clock in 80-column mode. Y3 oscillates at 31.084 MHz and serves as the basic clock in 132-column mode.

The gate array (U37) selects Y2 or Y3. The SDOTCK output from the gate array serves two purposes: as a clock to shift video data through a shift register (see Character Generation, page 4-19) and as a clock for a divide-by-nine counter within the gate array. The 955's character cell is nine pixels wide; thus, the divide-by-nine counter.

All system clocks are created inside the gate array. It provides the basis for the CPU system clock and for the character clock (CCLK BAR*) used by the CRT controller (2674 AVDC - U28). An inversion of this clock (CCLK) generates the CPU system clock or Phi zero (Ø0).

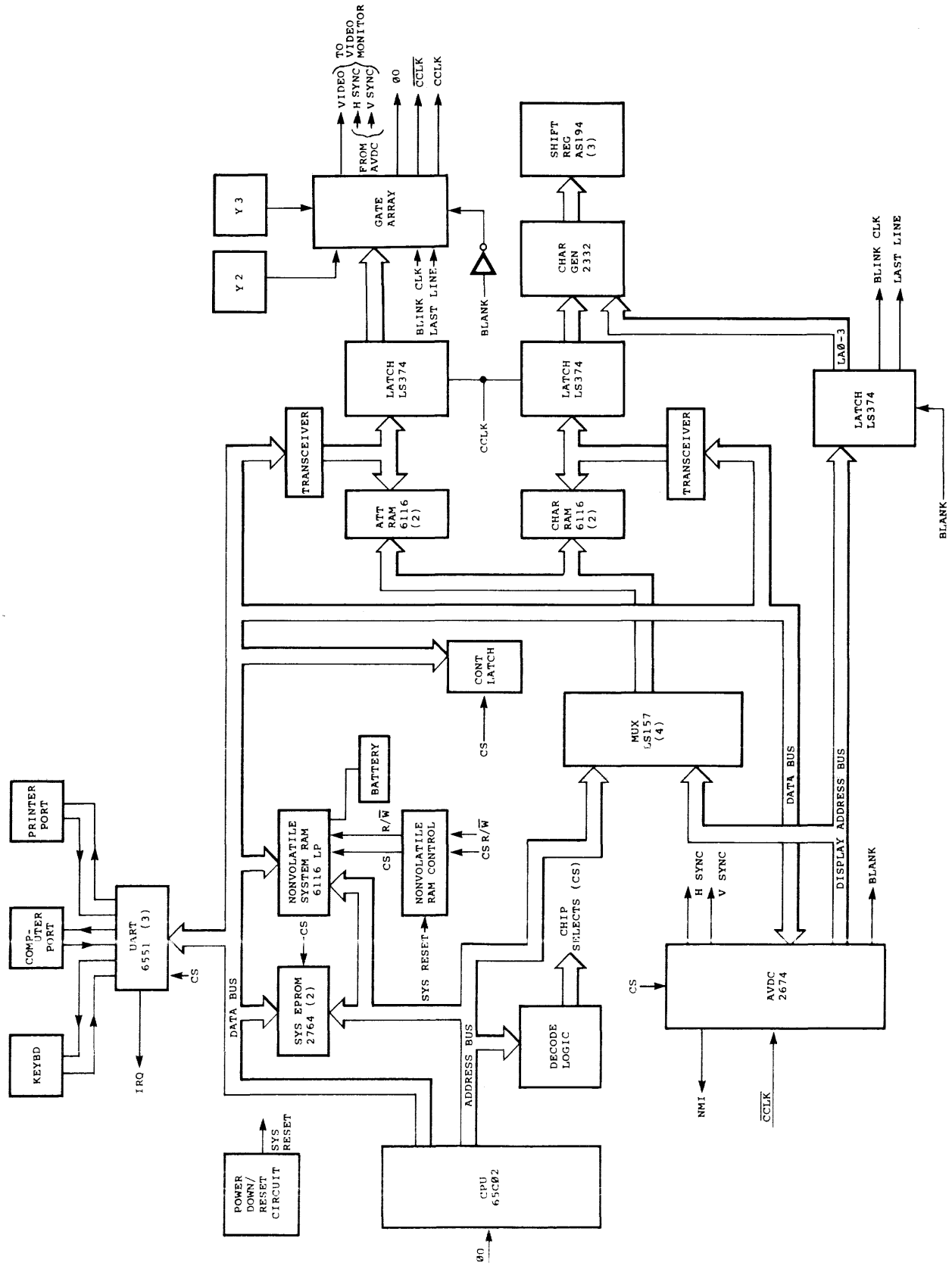
The CPU system clock and character clock are synchronized and interleaved (see Screen Data Storage, page 4-21). This allows the same clock to be used for system timing and for display generation.

Two considerations require CCLK to be modified for use as the system clock. They are: 1) the CPU's 3 MHz frequency limitation; and, 2) the requirement that any speed Universal Asynchronous Receiver Transmitter (UART) be used.

To overcome the CPU's speed limitation, CCLK is divided by 2 when in 132-column mode (see discussion in the next paragraph). To allow the use of any speed UART, the system clock is stretched out whenever the UARTs are accessed by the CPU.

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

Figure 4-4
955 Block Diagram (Enhanced Gate Array Logic Board)



In 132-column operation, the character clock is 31.084 MHz divided by 9, or 3.454 MHz. Dividing by 2 overcomes the CPU's 3 MHz frequency limitation while allowing the character and system clocks to be synchronized and interleaved. This is accomplished by the gate array.

The other clocks provided by the clock circuitry are: LDSRB and Q1 BAR*.

LDSRB is used to load parallel character data into the video shift register (see Display Generation, page 4-20).

Q1 BAR* is used to produce the signals necessary to properly write data into the character and attribute RAMs (see Screen Data Storage, page 4-21).

CPU System And Control (see sheets 1 and 2 of the schematic)

The CPU system consists of the CPU (65C02 - U4), the address bus decoder (74LS139 - U19, plus some gates), the system EPROMs (U14 and U15), system RAM (6116 LP4 - U16), the system reset circuit, and the control latch (74LS273 - U39).

The CPU is the controller for the entire board, initializing and controlling all of the UARTs, the CRT controller, the clock circuits and the video gate array. It also processes all of the data received from the keyboard, computer or printer, and updates the screen RAM accordingly.

Many of the display features, such as smooth scrolling and line lock, are controlled by the CPU in conjunction with the CRT controller.

Each device on the board has a specific address or range of addresses, as shown on the memory map (see Table 4-2).

The decoder chip (U19) provides the chip selects for all the devices on the memory map. Section one of this chip divides the 65K address range of the 65C02 into four 16K blocks.

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

The highest range block is used to select the system EPROMs, which contain the system firmware (a specialized operating system). The next lower 16K block is used for character RAM, which with attribute RAM (the next lower 16K block), is expandable to 16K bytes. The lowest 16K block is divided into four, 4K blocks by the second section of U19 and is allocated as follows.

The highest 4K block selects the optional system ROM, if it is installed. The next lower 4K block selects the CRT controller. The next lower 4K block selects the UARTs, graphics option board, and control latch. The lowest 4K block selects system RAM.

Table 4-2
Memory Map

FFFF F000	SYSTEM ROM
DFFF C000	SYSTEM ROM
BFFF 8000	CHARACTER RAM
7FFF 4000	ATTRIBUTE RAM
3FFF 3000	OPTION ROM
2FFF 2000	CRTC
18FF 1800	HOST UART
14FF 1400	PRINTER UART
12FF 1200	KEYBOARD UART
11FF 1100	CONTROL LATCH
10FF 1000	GRAPHICS OPTION
0FFF 0000	SYSTEM RAM

System RAM serves two purposes in the 955. Part of the RAM is used by the firmware as the stack and other temporary data stores, such as input and output buffers. In addition, the RAM is backed up by a battery, thus retaining the data even with power switched off. This allows portions of the RAM to be used for function key programming and to retain initialization parameters.

To retain data two things must occur: 1) the voltage to the RAM must not fall below 2 volts; and, 2) the RAM must be deselected as power from the power supply discharges.

Voltage is maintained by the battery (B1). Deselecting the RAM is accomplished by using a transistor (Q2) in series with the chip select signal from the decoder (see next paragraph).

With power on, SYSTEM RESET BAR* is high, turning Q2 on and allowing the chip select signal to go to the RAM. When power goes away, the SYSTEM RESET BAR* signal goes low when +5 volts falls below 4.4 volts. This turns Q2 off, causing pin 18 of the RAM to follow the voltage at the junction of CR6 and R14. This voltage drops at the same rate as +5 volts until the battery voltage is reached (typically 2.8 to 3 volts), at which time the battery voltage takes over.

The CPU system uses the control latch (U39) to give the firmware control over some hardware devices that do not interface to the data bus. The control latch's output signals are:

DTR
Data Terminal Ready. A signal sent to the host computer telling it to stop transmitting data to the 955 (DTR high).

HIGH SPEED
Used to control the transmit and receive clock to the computer port UART. A maximum baud rate of 38.4 Kbaud is provided when the signal is high. When it is low, the frequency is 1.8432 MHz.

MODEM
Used only if an internal modem is installed in the 955. When this signal is low, the internal modem interfaces with the computer port UART; when it is high, the RS232 interface is used.

PROT MODE
Protect Mode. A customer option determined by jumper W13. Identifies protect characters as half-intensity or reverse.

LITE/DARK
Selects whether the screen background is light or dark. When the signal is low, the screen background is light; when it is high, the screen background is dark.

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

LINE/PAGE ATT
Connects to the video gate array. Causes the selected attribute to carry to the end of the present character row (low) or to the end of the display (high).

EMB/NONEMB
Connects to the video gate array and controls the appearance of the attribute character. In embedded mode (space), the attribute character appears as a half-intensity space and prevents displaying data in the attribute character position. In nonembedded mode (no space) the attribute character does not appear and it is possible to display data at any location on the screen.

80/132
Selects between the 80-column mode and the 132-column mode. Clock frequencies are changed to correspond to the mode that is chosen.

The reset circuit is shown on sheets 1 and 2 of the schematic. For the CPU to initialize properly, the RESET BAR* input (pin 40) must be held low for a minimum of six system clock cycles after voltage is at the operating level (4.75 volts minimum).

The node labeled SYSTEM RESET BAR* is controlled by three devices: U2, the keyboard, and Q1. Until the +5 volts reaches the operating level for these devices, their outputs are in a high-impedance state (not being driven to either a high or low state). During this period the node is held low by pull-down resistor R8.

When the voltage reaches the 1.6-volt level, U2 begins to drive the node low and continues to do so until the voltage gets above 4.6 volts. At the 2.2-volt level the output of U7 also begins to drive the node low and continues to do so until the level on pin 4 of U3 reaches the 2.2-volt level. This is delayed by the RC network consisting of R5 and C6. The result is that SYSTEM RESET BAR* is held low for 60 to 80 milliseconds after +5 volts reaches the 4.75-volt level.

When all the devices stop driving the node low, a high level is applied to the node through Q1, which serves as an active pull-up with a delayed response relative to +5 volts. This prevents the node from following +5 volts during the early stages of a power-up sequence (when +5 volts is lower than 1.6 volts).

At power-down the controlling device is U2. Its output is driven low when the supply goes below 4.4 volts. This is not necessary for proper operation of the CPU, but is critical for the integrity of the battery backed-up RAM.

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

Character Generation (see sheet 4 of the schematic)

The 955 uses character cells, rather than a full bit-mapped display, to produce characters on the screen. Each character cell is 9 pixels wide by 14 pixels high. The screen consists of either 3432 (132 x 26) character cells in 132-column mode, or 2080 (80 x 26) character cells in 80-column mode. Each of the 256 possible characters is pre-defined and resides in the character generator ROM (U46). The CPU changes the display by changing the code stored in the screen RAMs at the desired location(s).

The codes written into the screen RAMs are read out as the CRT controller refreshes the display (see Display Generation, page 4-20). As each code is read out, one per character clock cycle, it is latched into the character address latch (U47).

The outputs of the character address latch are used as the high-order address lines of the character generator ROM (U46). The low-order addresses are provided by the scan line address latch (U33), which latches the line address outputs of the CRT controller. At the end of the character clock cycle, LDSRB goes low for one SDOTCK cycle.

With LDSRB low, the next rising edge of SDOTCK will load the D0 through D7 outputs of the character generator into an eight-bit wide shift register (U38 - 74F166). When LDSRB goes high, the data is shifted out of the Q7 output of U38 (pin 13) until the complete byte has been shifted out. The output of the shift register (U38, pin 13) connects to the video gate array (U37), where it is combined with other signals to create the video signal to the video monitor board.

The ninth bit is decoded when the logic (U42 and U48) detects a graphic character, which then is shifted in serial as the last dot.

In normal text mode, D7 and D0 from the character generator are always low (zero), creating a single dot space on the left (D7) and right (D0) of each character cell. The DS input of U38 (pin 1), which becomes the last dot on the right in the character cell, is loaded into the shift register as a low unless the Q7 output of the character address latch (U47) and D0 are high.

If Q7 is high, the DS input of U38 will be the same as the D0 input of U38. This allows nine-bit wide graphics characters that use the entire width of the character cell, such as line drawing graphics.

Character address codes 00 through 7F cannot extend the entire width of the character cell; graphics character codes 80 through FF can.

Display Generation (see sheets 3 and 4 of the schematic)

The video monitor board requires three signals from the logic board to produce a display on the CRT: vertical sync (VSYNC BAR*), horizontal sync (HSYNC), and video.

VSYNC BAR* and HSYNC originate from the CRT controller (2674 AVDC - U28). They are buffered and connect to the video board through pin 5 (VSYNC BAR*) and pin 1 (HSYNC) of P2. Video comes from the video gate array (U37). It goes through an AND gate (U42) and a high-current open collector inverter (U40).

HSYNC and VSYNC BAR* are timed pulses derived by the CRT controller from internal programmable counters that count CCLK cycles. For example, HSYNC might be a positive-going pulse starting 80 CCLK cycles after the beginning of each scan line and lasting 16 CCLK cycles. The CRT controller's internal counter would reset at the beginning of each scan line, count to 80, set HSYNC high, count 16 more CCLKs and set HSYNC low.

VSYNC is a much slower signal based on scan lines. Another counter inside the CRT controller counts scan lines and toggles VSYNC according to the way the firmware has programmed the internal registers.

As the CRT controller (2674 AVDC - U28) counts CCLKs, it is also putting out addresses on its display address lines (pins 21-34, DADD0-DADD13). These lines connect to four 74LS157 4-bit 2-way multiplexers (U26, U27, U31 and U32). The select inputs of the multiplexers are normally high, allowing the CRT controller's address line to access the data in the screen RAMs.

As data in the screen RAMs is read out, it is latched into the character address latch (U47) for the character data bus and into the video gate array for the attribute data bus.

The serialized character data (see Character Generation, page 4-19), is fed into the video gate array where it is combined with attribute data, the BLANK output of the CRT controller, the cursor output of the CRT controller, LITE/DARK and other signals to produce a series of pulses that come out on the VIDEO output of the gate array.

If the VIDEO output of P2-4 is high, the electron beam in the CRT is turned on, producing a light dot or series of dots on the screen. If the VIDEO is low, the screen is dark.

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

Screen Data Storage (see sheets 2 and 3 of the schematic)

If the CPU needs to access either the character or attribute RAMs, the corresponding signal, CHAR RAM BAR* or ATT RAM BAR* goes low for a full CPU cycle. Since the CPU clock can be running at half the speed of the character CCLK (see Clock Circuit, page 4-13), both of these signals are gated with CCLK BAR*.

When CCLK BAR* is low, the CRT controller is at the beginning of a character clock cycle and its address lines are not stable. However, during this period the CPU's address lines are stable and the CPU is either putting data on the data bus or is looking for data from the selected device.

Gating CHAR RAM BAR* and ATT RAM BAR* with CCLK BAR* and then ANDing the resulting signals produces a low on the select inputs (pin 1) to the multiplexers during this period of the CPU cycle. This allows the CPU's address lines to drive the screen RAMs.

The outputs of the two gates used to gate CHAR RAM BAR* and ATT RAM BAR* with CCLK BAR* (74LS32, U43 pins 8-13) are connected to the CE BAR* inputs to U25 and U30. U25 and U30 are 8-bit transceivers used to isolate the CPU data bus from the character data bus and the attribute data bus (CD0-7 and AD0-7).

The direction control input to the transceivers (pin 1) is created by gating CCLK BAR* with R/W from the CPU (U43, pins 1-3). In this manner, the CPU can write data to or read data from the screen RAMs (either character or attribute) without interrupting or interfering with the CRT controller's process of refreshing the screen.

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

Communications (see sheet 5 of the schematic)

There are three serial communications channels. Each has its own dedicated UART and can send and receive data at speeds ranging from 50 to 19,200 bits per second (38,400 for the computer port).

U22 (6551A) is the UART used for communication to the host computer. It interfaces to a 25-pin D-subminiature connector (P3) via TTL to RS-232 level converters (U9 and U5, 1489's; U13 and U17, 1488's).

The baud rate is selectable under firmware control and is derived from the clock going in on pin 6 (XTAL 1). For the normal baud rate range of 50 to 19.2K, a 1.8432-MHz clock is used. When the 38.4K baud rate is selected, the firmware selects a slower frequency of 460.8-KHz. It does this by using the HIGH-SPEED control line of the control latch (see CPU System and Control, page 4-15).

U21 is the UART dedicated to printer communications. It interfaces to a 25-pin D-subminiature connector (P4) via the same chips as U22. Its clock input is fixed at 1.8432 MHz, providing a 50 to 19.2K baud range.

U20 is the UART used to communicate with the keyboard. Its clock input is also fixed at 1.8432 MHz and is capable of communicating at 50 to 19.2K baud. Since the keyboard's baud rate is 9600 baud, the firmware programs U20 to always communicate at this speed.

The IRQ BAR* outputs for all three UARTs are tied together in a wired OR configuration. When any of the UARTs generate an Interrupt Request (IRQ), the IRQ BAR* line goes low, signaling to the CPU that an interrupt has occurred. The CPU then polls the UARTs to determine which one generated the interrupt, and processes the interrupt as required.

*Signals referred to as "SIGNAL BAR" appear on the schematic as $\overline{\text{SIGNAL}}$.

SERVICE INFORMATION

If your terminal has technical problems, contact your dealer. International customers may telex 474-5041 TVISYS or call the nearest regional sales office. TeleVideo sales offices are listed below.

REGIONAL SALES OFFICES

Eastern
6900 Jericho Turnpike
Suite 100LL
Syosset, NY 11791
(516) 496-4777

Northeast
1601 Trapelo Road
Reservoir Place
Waltham, MA 02154
(617) 890-3282/3284

Northwest
1170 Morse Avenue
P.O. Box 3568
Sunnyvale, CA 94088-3568
(408) 745-7760

Southeast
6075 The Corners Parkway
Suite 208
Norcross, GA 30092
(404) 447-1231

Southcentral
1431 Greenway Drive
Suite 110
Irving, TX 75038
(214) 550-1060

Midwest
1002 E. Algonquin Road
Suite 112
Schaumburg, IL 60173
(312) 397-5400

Central Europe
Saturnusstraat 25
2132 HB Hoofdorp
The Netherlands
Phone: 011-31-2503-35444
Telex: 74615 (TLVDO NL)

Northern Europe
Dorna House,
50 Guildford Rd., West End
Surrey GU24 9PW
England
Phone: 011-44-09905-6464
Telex: 858922

Southern Europe
3 rue Le Corbusier
Silic 244
94568 Rungis Cedex (Paris)
France
Phone: 011-33-1-4687-3440
Telex: 205191F

SPECIFICATIONS

I. Physical

VDT Dimension:

Height:	36.195 cm (14.25 in.)
Width :	32.385 cm (12.75 in.)
Depth :	31.75 cm (12.5 in.)

VDT Net Weight: 22 lbs.

Case Foot Print 12.5 in. by 11.5 in. max.

Case Features:

Tilt:	-5 to +15 degrees
Swivel:	270 degrees left to right
Cooling:	Convection system
Connectors:	One RS232 communication port One RS422 communication port (option) One RS232 printer port One RJ12 mouse port (option) One RJ12 keyboard port One AC receptacle-type quick disconnect

CRT:

Diagonal Measure:	35.56 cm (14 in.)
Phosphor:	Green
Fluorescence:	Green
Face-plate:	Filterglass
Screen:	Aluminized
Persistence:	Medium Short (300us decay time)

II. Electrical

AC Supply:

Frequency:	50/60 Hertz +/- 3Hz
Source Current:	
115V Line:	1.0 Amp. (Max.)
230V Line:	.5 Amp. (Max.)
Phase:	Single phase, 3-wire
Wattage:	40 VA Max.

DC Supply:

5V:	+/- .1 Volt at 3 Amp.
12V:	+/- .2 Volt at 2.0 Amp.
-12V:	+/- .5 Volt at 200 mA
Ripple and Spike Noise:	100mV peak to peak all DC outputs max. (Resistive Load)

III. Display	80	132
Horizontal Scanning Frequency:	22.86 Khz	22.86 Khz
Vertical Scanning Frequency:	60 Hertz	60 Hertz
Character Lines:	26	26
Columns Per Line:	80	132
Cell Size (Character Block):	Dot Matrix	Dot Matrix
Width:	9	9
Height:	14	14
High Voltage (At Dark Screen):	13.5 KV +/-500V	13.5 KV +/-500V
High Voltage Regulation (From Dark Screen to Full Bright):	500V +/-250V	500V +/-250V
Picture Brightness at Maximum Contrast:	40 Ft. Lambert	40 Ft. Lambert
Picture Size (Active Display)		
Format:	26 lines of 80	26 lines of 80
Width:	235 mm	235 mm
Height:	185 mm	185 mm
Levels of Gray:	Dark, Half Bright, Full Bright	

IV. Keyboard:

Style:	Low Profile (DIN std.)
Height:	4.699 cm (1.85 in.) Untilted
Home Row DIN std.	30 mm Untilted
Width:	45.2 cm (17.8 in.)
Depth:	18.415 cm (7.25 in.)
Net Weight:	1.81 kg (3 lbs.)
Microcontroller:	8049
Layout:	Included in this section, following specifications
Operating Life:	10 Million Keystrokes Min.

V. Environmental:

Operating:

Temperature:	0 to 45 Degrees C (32 to 113 Degrees F)
Humidity:	10% to 85% non-condensing
Altitude:	3,000 m / (10,000 ft.)

Non-operating:

Temperature:	-40 to 60 Degrees C
Humidity:	10% to 85%
Altitude:	5,000 m / (15,000 ft.)

MTBF:	10,000 Hours Min.
MTTR:	30 Minutes
Vibration:	0.3G, 5 to 100 Hz, operational
Shock:	20G, 11 ms, 18 shocks

Shipping:

Girth:	108 inches max.
Weight:	50 lbs. max.

VI. CRT Controller Format:

	80 x 26	132 x 26
1. Dot Frequency	19.3396 MHz	31.6840 MHz
2. Character Cell		
Number of Dots per Character:	9	9
Number of Scan Lines per Character	14	14
3. Character Frequency	2.14884 MHz	3.52044 MHz
4. Screen Format		
Number of Characters per Screen	80	132
Number of Rows per Screen	26	26
5. Total Characters per Line	94	154

VII. Control Board

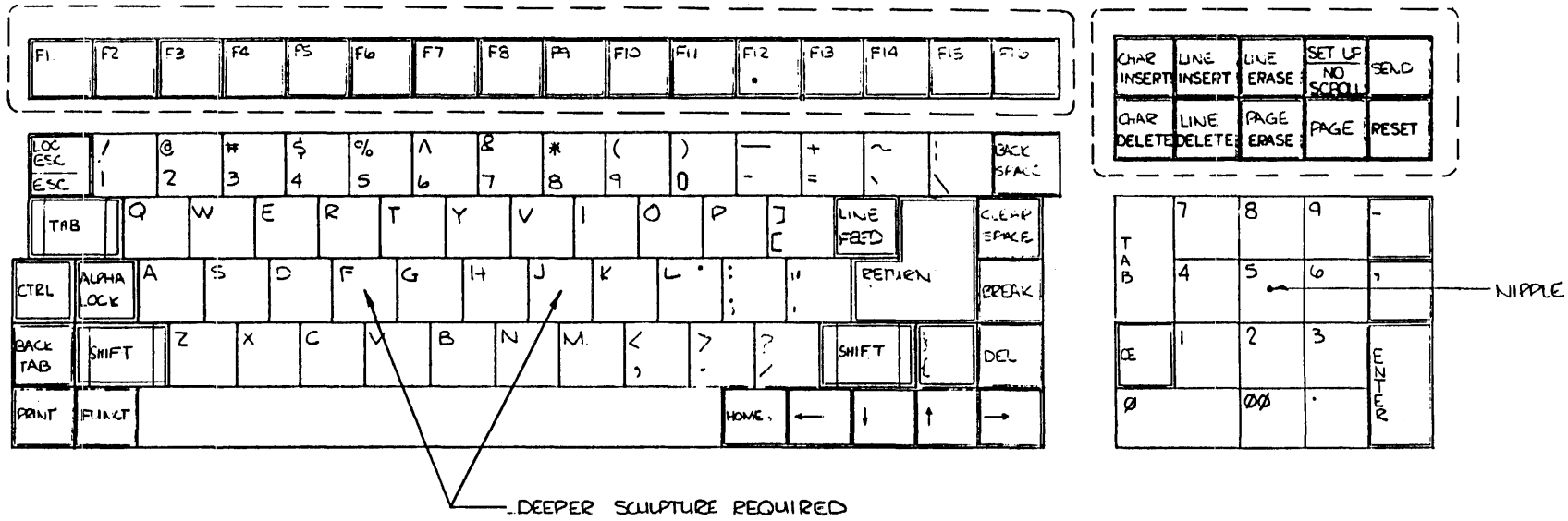
Type:	2-sided, includes power and ground
Microprocessor:	65C02-P3 (3 MHz)
CRT Controller:	2674
Battery:	3V min. Lithium
Current Loop:	Option Board (P6)
Graphics Board Connector:	26-pin
Current Load (std.)	1.3A (5V); 220ma (12V)
Current Load with Options	2.5A (5V) max.
Printer Port	RS232 (P4)
Main Port	RS232 (P3)
Baud Rate (Main): (Printer):	50-38.4K bit/sec. 50-19.2K bit/sec.
Parity:	No, Odd, Even, Mark, Space
Data Bits:	7 or 8
Handshaking:	No, X-on/X-off, DTR, Both
System ROM:	16K
System RAM:	2K
Display RAM:	4K to 16K max.

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	1	PROTO RELEASE	3-6-84	DDH
	2	CHANGED TAB & SHIFT TO STEPPED KEYS	3-8-84	N.G.
	A	PROD RELEASE PER ECO #2846T	5/7/85	

— LIGHT COLOR KEYCAPS.

— DARK COLOR KEYCAPS.

— KEYCAPS IN DESIGNATED AREA ARE 0° SLOPE.



NOTES:
1. KEYCAP COLORS MUST MATCH SHADES WITHIN EACH SET OF KEYCAPS

QTY REQD	ITEM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN	TeleVideo, Inc.
NEXT ASSY	USED ON		CHK	
		ANG ± PLCS ± PLC	ENGR	TITLE: KEY CAP LAYOUT LO PRO (Hi-Tek)
		x	APPD	
		SCALE x	APPD	
		MATERIAL x	FINISH x	SIZE C · SHT 1 OF 1 · DRAWING NO. 131102-00 · REV A

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