H-78-0408A

Graphic7™

COMPUTER GRAPHICS DISPLAY SYSTEM

MODELS 7702—7704
LARGE READ/WRITE MEMORY
TECHNICAL MANUAL

Information Products Division
Federal Systems Group
SANDERS
DANIEL WEBSTER HIGHWAY, SOUTH—NASHUA, NEW HAMPSHIRE 03061

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SECTION 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the optional large memory circuit card assembly used in the Sanders Associates, Inc., GRAPHIC 7 terminal controller when customer applications require large memory capacities. This manual covers the following versions of the large memory card:

Model	Part No.	Description
7704/5704	1089724G1	64K read/write memory cca
7703/5703	1089724G2	32K read/write memory cca
Special	1089724G4	32K read/write memory cca
7702	1089724G4	16K read/write memory cca
-	1089724G5	48K read/write memory cca

The G2 through G5 configurations are depopulated versions of the G1 configuration. The G2 and G3 configurations have the same capacity and the same features, but the depopulations are different.

1.2 EQUIPMENT DESCRIPTION

1.2.1 PHYSICAL DESCRIPTION

The large memory circuit card assembly is 7.75-inch by 12-inch long assembly, fitted with a 98-pin plug that matches the GRAPHIC 7 terminal controller card cage connectors XA1 through XA8, which are commonly wired. The preferred position for the large memory card is the lowest numbered slot available on the processor bus (i.e., slot 1A1A1), with a second card (if used) in the next higher slot. If a 32K, 48K or 16K memory card is used in conjunction with a 64K memory card, the 64K memory card must be in the lower numbered slot. Processor bus control priority is not a concern with these cards.

1.2.2 FUNCTIONAL DESCRIPTION

The large memory card is an optional replacement for the 8K memory card supplied as the nominal 1A1A1 card for the GRAPHIC 7 terminal controller. Each 64K memory card can store up to $65,536_{10}$ 16-bit words (or $131,072_{10}$ separately

addressable 8-bit bytes). The 32K memory card can store up to 32,768 16-bit words or 65,536 8-bit bytes. The 16K memory card can store up to 16,384 16-bit words or 32,768 8-bit bytes.

A maximum of two 64K memory cards can be installed in a GRAPHIC 7 system for a combined storage capacity of 131,072 16-bit words or 262,144 8-bit bytes. Each large memory card has its own local oscillator, memory controller, refresh controller, and memory mapping logic.

A large read/write memory card cannot be used in conjunction with the 8K memory cards normally supplied with the GRAPHIC 7 terminal controller.

SECTION 2

OPERATION

2.1 GENERAL

The large read/write memory cards connect to and are controlled by the processor bus, but do not control that bus. Any applicable circuit card connecting to the processor bus can write data into a specific memory location by seizing control of the bus, placing the desired address on the ADnn-B lines and the desired data on the DAnn-B lines, then placing a low logic level on the WRIT-B (write command) and ADRV-B (address valid) control lines.

Conversely, any applicable circuit card can seize control of the processor bus to read out stored data onto the DAnn-B lines by placing the specific address on the ADnn-B lines and placing a low logic level on the ADRV-B line while leaving WRIT-B high.

The large read/write memory cards can operate in any of card cage slots 1A1XA1 through 1A1XA7. Sanders recommends that they be installed at the lower end of the card cage. If two cards are used, they should be installed in consecutive slots. If one card is a 64K card and the other is not, the 64K card should be installed in the lower numbered slot.

2.2 MEMORY ORGANIZATION

The memory card is divided into 4K "pages". Each such page is a 4K word storage area: page 0 = addresses 0 through 4K-1; page 1 = addresses 4K through 8K-1, etc. The 64K memory card has 16 such pages, the 32K memory card has eight pages, and the 16K memory card has four pages.

The G2 configuration of the memory card contains only octal pages 0 through 7. The G3 configuration contains only pages 0 through 3 and 10 through 13. The G4 configuration contains only pages 0 through 3.

Figure 2-1 lists the 32 pages of a 2-card memory. The listing identifies octal-value page numbers and the corresponding octal-value addresses for each page. Note that page 0 is dedicated and cannot be used for general purpose applications. Page 0 contains all the vector trap addresses and certain other reserved functions.

Pages 6 and 7 are a special case. The addresses associated with page 6 are also the addresses associated with the GCP or GCP+ located in ROM on the ROM and status card. An address in the range from 140000_8 through 157776_8 accesses the GCP or GCP+. However, through a special mapping technique, the display processor can access page 6 of the large read/write memory card. The display processor is the only device that can access page 6.

OCTAL PAGE #		EFFECTIVE ADDRESSES
	MEMORY CARD 1	
0	RESERVED	000000:017776
1	MAP AREA 1	020000:037776
2	MAP AREA 2	040000:057776
3	MAP AREA 3	060000:077776
4		100000:117776
5		120000:137776
6	GCP (ROM)	140000:157776
7	DEVICE ADDRESSES	160000:177776
10		200000:217776
11		220000:237776
12		240000:257776
13		260000:277776
14		300000:317776
15		320000:337776
16		340000:357776
17		360000:377776
	MEMORY CARD 2	
20		400000:417776
21		420000:437776
22		440000:457776
23		460000:477776
24		500000:517776
25		520000:537776
26		540000:557776
27		560000:577776
30		600000:617776
31		620000:637776
32		640000:657776
33		660000:677776
34		700000:717776
35		720000:737776
36		740000:757776
37		760000:777776

Figure 2-1. Correspondence Between Octal Page Numbers and Their Associated Addresses

Similarly, the addresses associated with page 7 are also the addresses associated with devices (device addresses). An address in the range from 160000_8 through 177776_8 accesses a particular device. However, through a special mapping technique, the display processor can access page 7 of the large read/write memory card. The display processor is the only device that can access page 7.

2.3 MEMORY ADDRESSING

Typical devices that have access to the memory include the display processor, graphic controller, and parallel interface. Only the display processor can use the memory mapping technique and thus gain access to pages 6 and 7. All other devices address the memory directly.

The memory card can be addressed in either of two ways: by 18-bit addressing from any card capable of generating an 18-bit address, or by 16-bit addressing (plus page registers) by the display processor.

Figure 2-2 shows the structure of an 18-bit address. This mode of addressing is called direct addressing. Bit 17 (in conjunction with a switch on the memory card) determines whether card 1 or card 2 is addressed. Bits 15 and 16 select a 16K block (4 pages) on the card. Bits 1 through 14 determine the single address within the selected 16K block. Bit 0 is not really part of the address; it determines the word/byte status.

Direct addressing with an 18-bit address gives access to the total memory, except for pages 6 and 7.

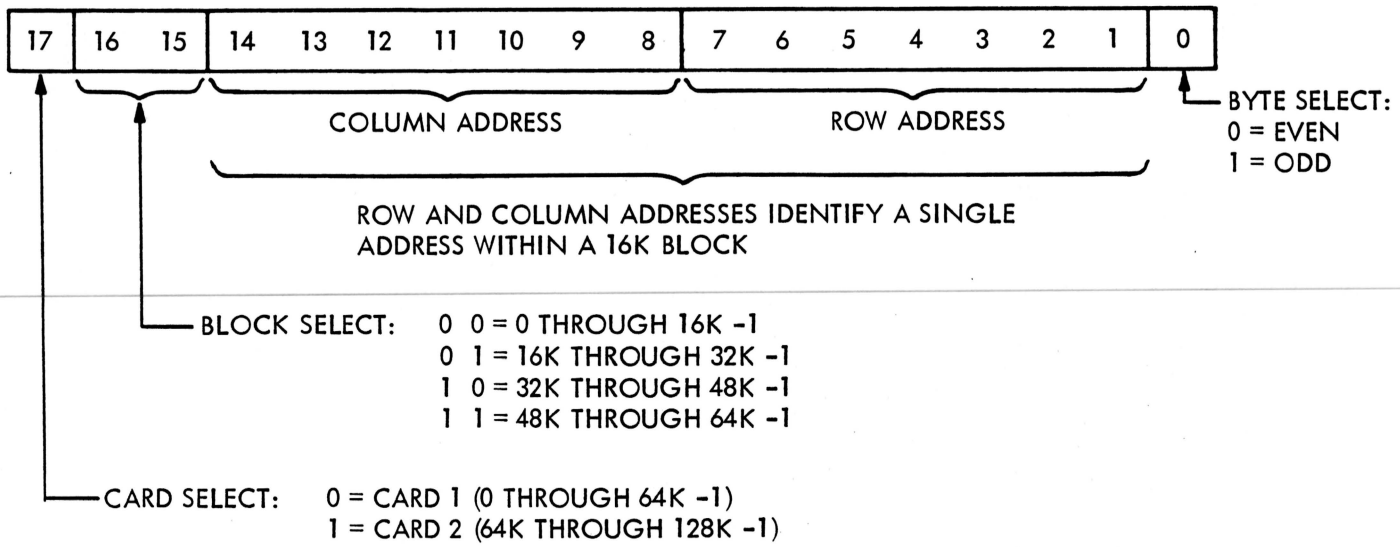

Figure 2-2. Structure of 18-Bit Address

The display processor is a 16-bit device, and thus has direct address to only 32K words of memory (8 pages). The display processor can gain access to memory locations above 32K-1 by memory mapping from memory locations in the range from 4K through 16K-1. This feature involves the use of three page registers.

The memory card contains three page registers, each of which can be preloaded with some particular value consisting of five bits. When the display processor addresses a page register, the five bits stored in that register becomes bits 13 through 17 of the address, as shown in figure 2-3. This feature allows mapping to 32 pages.

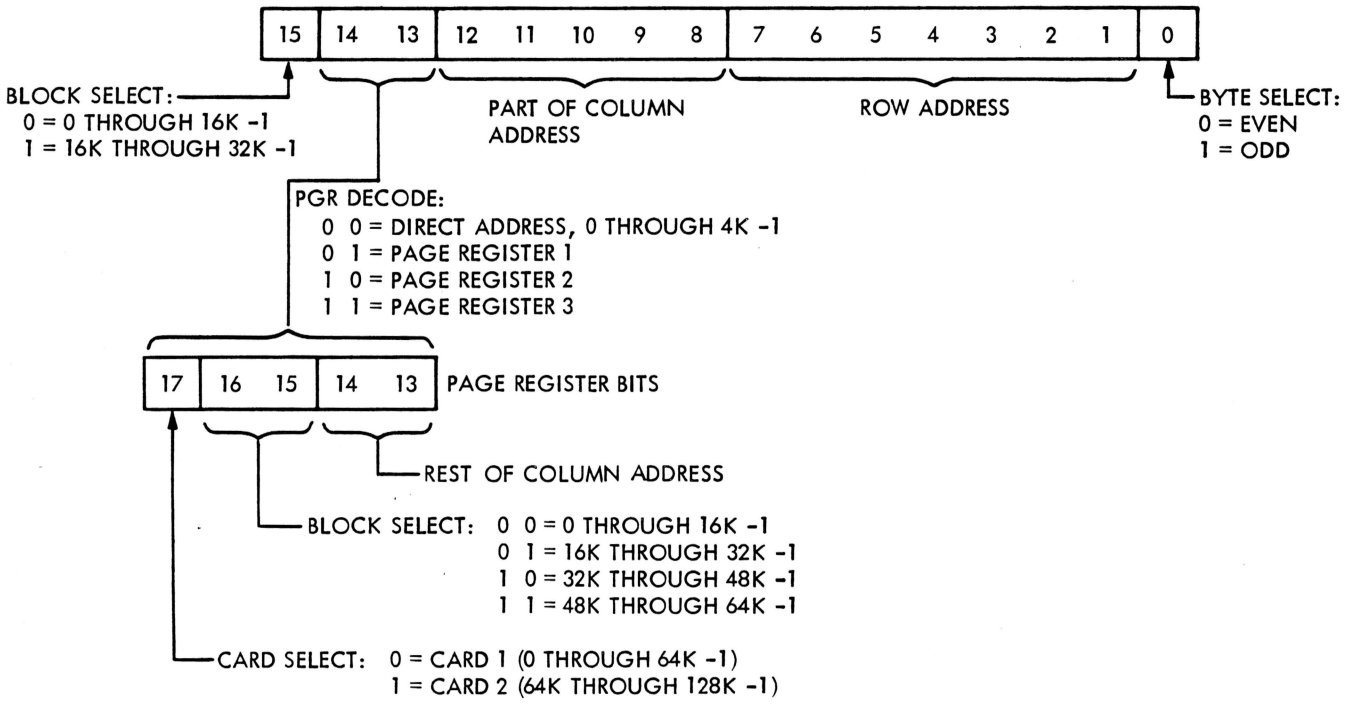

Figure 2-3. Structure of 16-Bit Address with Memory Mapping

Memory mapping is not invoked when bits 13 through 15 are all zeros; in this case the display processor has direct access to page 0 (memory locations 0 through 4K-1). Memory mapping is not invoked when bits 15 is true (low = logic 1); in this case the display processor has direct access to pages 4 and 5 (memory locations 16K through 24K-1). (In this case pages 6 and 7 are still locked out.)

Memory mapping is invoked only when the controlling device is the display processor, bit 15 is high (logic 0) and bits 13 and 14 are not both zeros. In this case, bits 13 and 14 select one of the three page registers, and bits 1 through 12 constitute part of the final address. The selected page register contributes five additional bits: bit 17 selects the memory card; bits 15 and 16 select a 16K block (4 pages) on the card; and bits 13 and 14 select a predetermined 4K block (1 page) within the 16K block. This is how the display processor gains access to pages 6 and 7 and to memory locations above 32K-1.

However, if the page register is loaded with all zeros, then memory mapping is disabled and the address defaults to the appropriate 4K page in the range from 4K through 16K-1.

2.3.1 EXAMPLE OF MEMORY MAPPING

Assume that the page registers are loaded as shown in figure 2-4. In this case, if the display processor addresses map area 1 or 3, it gains access to pages 1 or 3 because page registers 1 and 3 are loaded with all zeros. However, a read/write operation addressed to map area 2 actually reads or writes at the corresponding address on page 14, because page register 2 contains a value of 14.

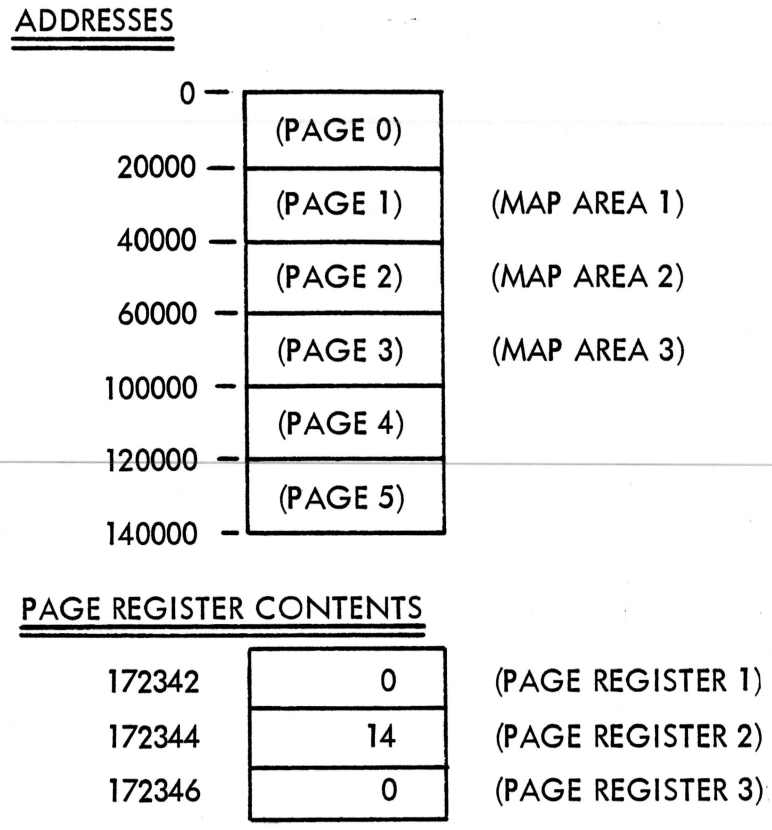

Figure 2-4. Mapping Action

2.4 SOFTWARE CONSIDERATIONS

2.4.1 USING MAPPING FUNCTION TO RELOCATE A REFRESH FILE

Figure 2-5 shows a programming technique for using the mapping function to relocate a refresh file. This assembly-language example assumes a refresh file that begins at the start of page 12_8 and is to be relocated on page 15_8.

```
START:  COUNT =  200.       ; 200 WORDS TO BE MOVED
        MOV     #20000,R1   ; R1 WILL BE SOURCE ADDRESS
        MOV     #60000,R2   ; R2 WILL BE DESTINATION ADDRESS
        MOV     #12 ,PR1    ; PAGE 12 IS SOURCE
        MOV     #15 ,PR3    ; PAGE 15 IS DESTINATION
        MOV     #COUNT,R3   ; WORD COUNT IN R3
WRITE:  MOV     (R1)+,(R2)+ ; 1 WORD COPIED
        SOB     R3,WRITE    ; CONTINUE UNTIL DONE
```

Figure 2-5. Use of Programmable Mapping Function to Relocate a File

In the above example, the instruction MOV # 20000,R1 selects address 000000 of a 16K block and the digit 2 of that instruction specifies page register 1. The instruction MOV # 60000,R2 selects address 000000 of a 16K block and the digit 6 of that instruction specifies page register 3.

2.4.2 PGR CONSIDERATIONS

The graphic controller card's PGR (page register) logic stores and outputs address bits AD16-B and AD17-B, which effectively select one of four 32K memory banks for read/write operations while the graphic controller card has control of the processor bus. The GCP can read or write this register (when the graphic controller card is halted) through data bits DA14-B and DA15-B at address 165014_8. Such access requires paying special attention to the handling of graphic controller interrupts and to starting and stopping the graphic controller.

First, note that the PGR page-register bits are accessed at the same address (165014_8) as the DPR (display parameter register) bits, normally accessed only during the processing of an LDDP graphic controller instruction. Inadvertent changing of other bits at this program address thus might alter display parameters.

Secondly, the PGR bits are not incremented by the display program counter (DPC) circuit on the graphic controller card. This fact means that a "wraparound" effect would occur if the graphic controller sequence were to encounter a 32K boundary -- which thus must not be allowed to happen. The housekeeping software must keep track of these boundaries and prevent the graphic controller code from crossing them.

Finally, all page registers (PGR, PR1, PR2, and PR3) are cleared (to zero value) by activation of a REST-B bus-reset signal following power turn-on, execution of a reset instruction, or receipt of a host-generated initialize command.

The following discussion provides further details concerning these considerations.

2.4.3 USING THE GRAPHIC CONTROLLER "ABOVE" 32K

a. To start the graphic controller, the page register (PGR) bits should be set up before loading the DPC, because loading the DPC starts the graphic controller.

Since a bus-reset (REST-B) signal clears the page register bits after power turn-on or after the display processor executes an initialization instruction, the graphic controller will initially run at "page zero" (0-32K) if the PGR bits remain unchanged.

b. The use of FUNS (FUNction Control Stop) and FUNC (FUNction Control Continue) instructions is not different with the use of the page register. A FUNS instruction stops the graphic controller if it is running, a FUNC instruction restarts it.

c. Handling PHOTOPEN® interrupts by checking the DPC is cumbersome, because the page register bits also need to be checked. A better approach is the use of the graphic controller general purpose registers DR0 through DR3 to act as labels for PHOTOPEN-sensitive areas of refresh files (see figures 2-6 and 2-7).

```
LDDI 1,1        ; SET LABEL TO "1"
(REFRESH        ; PHOTOPEN-SENSITIVE
 CODE FOR       ; REFRESH AREA #1
 FIRST AREA)    ;
LDDI 1,2        ; SET LABEL TO "2"
(REFRESH        ;
 CODE FOR       ; PHOTOPEN-SENSITIVE
 FIRST AREA)    ; REFRESH AREA #2
```

Figure 2-6. Labeling of PHOTOPEN-Sensitive Areas

d. LINK - All indirect addresses are accessed in the page defined by the page register. The direct instruction addresses pertain to page 0 regardless of the state of the PGR bits. A "LINK 170" is not allowed outside of page 0, because the display processor does not have a direct 18-bit addressing capability and must use memory mapping to access memory addresses greater than 32K.

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```
INTRPT: CMP @#DR1,#1 ; DID AREA 1 CAUSE INTERRUPT?
        BEQ AREA1    ; YES.PROCESS AREA 1 INTERRUPT.
        CMP @#DR1,#2 ; DID AREA 2 CAUSE INTERRUPT?
        BEQ AREA2    ; YES. PROCESS AREA 2 INTERRUPT.
RETURN: RTI          ; RETURN IF UNKNOWN INTERRUPT

AREA 1: (HANDLER FOR
         AREA1 INTERRUPT)
AREA 2: (HANDLER FOR
         AREA 2 INTERRUPT)
```

NOTE: HANDLER SUBROUTINES MUST END WITH RTI INSTRUCTION.

Figure 2-7. Representative Interrupt Handler for Processing the PHOTOPEN Data Refresh File

An approach to using LINK addresses in pages other than page 0 would be to define a location which corresponds to each of the four 32K blocks for LINKing (see figure 2-8).

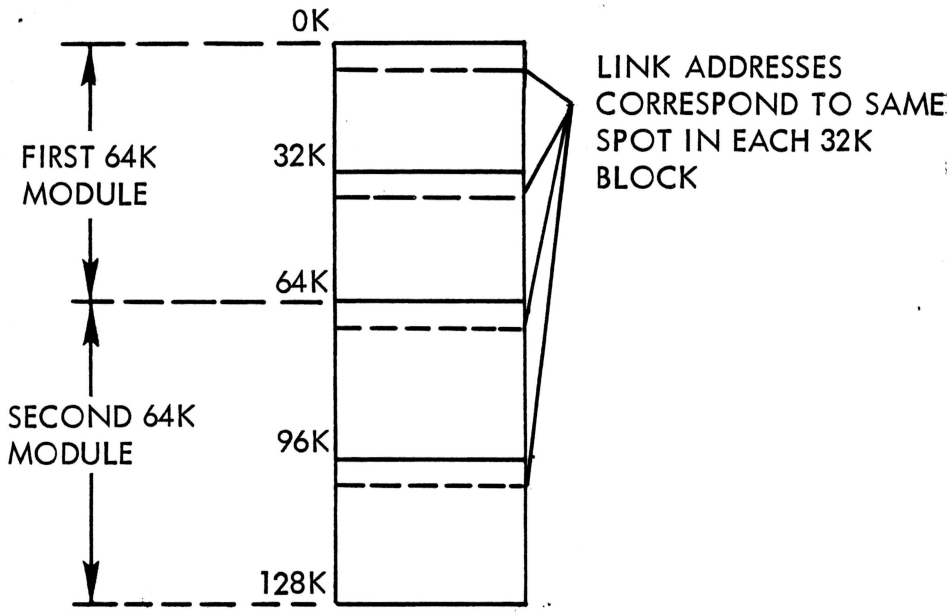


Figure 2-8. An Approach to LINKs

A LINK performs a "JUMP and MARK" to the subsequent LINK address, then halts the graphic controller and interrupts the display processor. The LINK interrupt trap vector is at address 170.

e. Stack-related instructions, such as CALL, RTRN, SAVD and RESD, require the definition of a stack pointer and a stack area in each 32K block. An approach similar to that used for LINK addressing would reserve some memory in each 32K block for stack, as shown in figure 2-9.

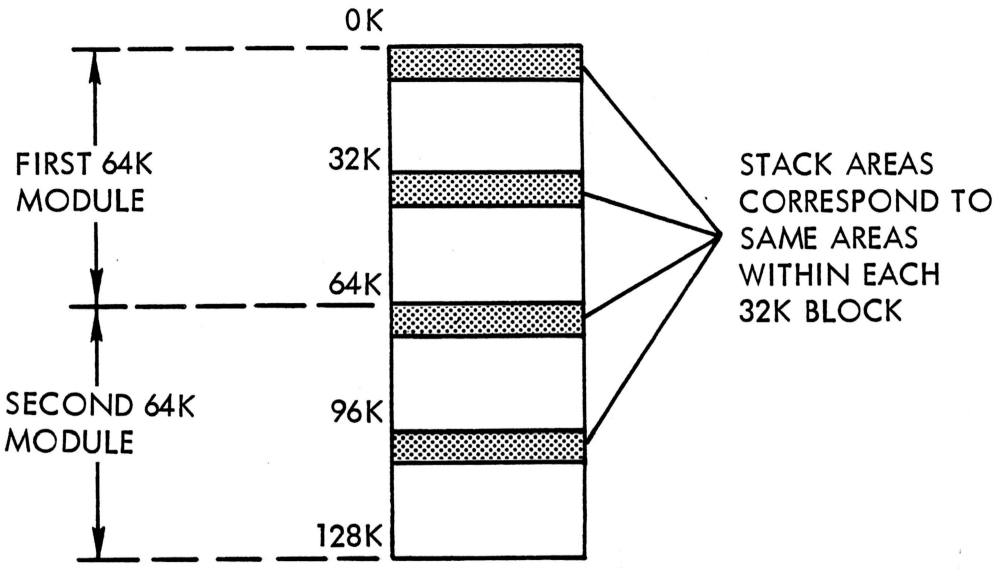


Figure 2-9. An Approach to the Use of the Graphic Controller's Stack

f. Graphic controller calls to specified banks may be incorporated by using coded graphic controller halt codes. This method is used by GCP+ after the host computer sends a LM (large memory) command.

The 'Q' register of the display processor is used as a private calling stack. The halt interrupt vector is set to interrupt to a special graphic controller banking routine. The halt interrupt is enabled. General register 3 (DR3) is used to pass the 'CALL' address from the graphic file to the display processor.

The coded graphic halts are:

OCTAL CODE	FUNCTION
000000	Return from subroutine
000001	Call bank 0
000002	Call bank 1
000003	Call bank 2
000004	Call bank 3

Refresh file CALLS would appear as follows:

```
LDDI   3,BOX1      ; LOAD THE CALL ADDRESS IN DR3
,WORD  2           ; CALL BANK #1
```

Refresh file SUBROUTINES would be similar to this:

```
BOX1    LDXR    -100        ; ENTRY FOR BOX1 SUBROUTINE
        DRYR    +100        ;
          .
          .
          .
        ,WORD   0           ; RETURN FROM SUBROUTINE
```

The graphic controller bank interrupt (HALT) routine is:

```
GCBANK:         EXCQ    R2              ; EXCHANGE R2 AND Q
                MOV     R0, -(SP)       ; SAVE R0
                MOV     @# DIR, R0      ; GET CODED HALT FROM INSTRUCTION
                                          REGISTER
                BEQ     GCB3            ; SKIP FOR A RETURN
                MOV     @# DPC, -(R2)   ; PUSH DISPLAY PC
                SUB     #2, (R2)        ; ADJUST DISPLAY RETURN ADDRESS
                MOV     @# PGR, -(R2)   ; PUSH DISPLAY PAGE REGISTER
                DEC     R0              ; CODE 1 = BANK 0, CODE 2 = BANK 1, etc
                ROR     R0              ; ALIGN LOW ORDER
                ROR     R0              ;   BITS TO
                ROR     R0              ;     MSB POSITIONS
                MOV     R0, @# PGR      ; SET NEW BANK
                MOV     @# DR3, @# DPC  ; START GRAPHIC SUBROUTINE
                BR      GCB5
GCB3:           MOV     (R2)+, @# PGR   ; RESTORE PAGE
                MOV     (R2)+, @$ DPC   ; RESTART GRAPHICS FOR RETURN
GCB5:           MOV     (SP)+, R0       ; RESTORE R0
                EXCQ    R2              ; EXCHANGE Q AND R2
                RTI                     ; RETURN FROM INTERRUPT
```

2.4.4 DISPLAY PROCESSOR LARGE MEMORY SOFTWARE

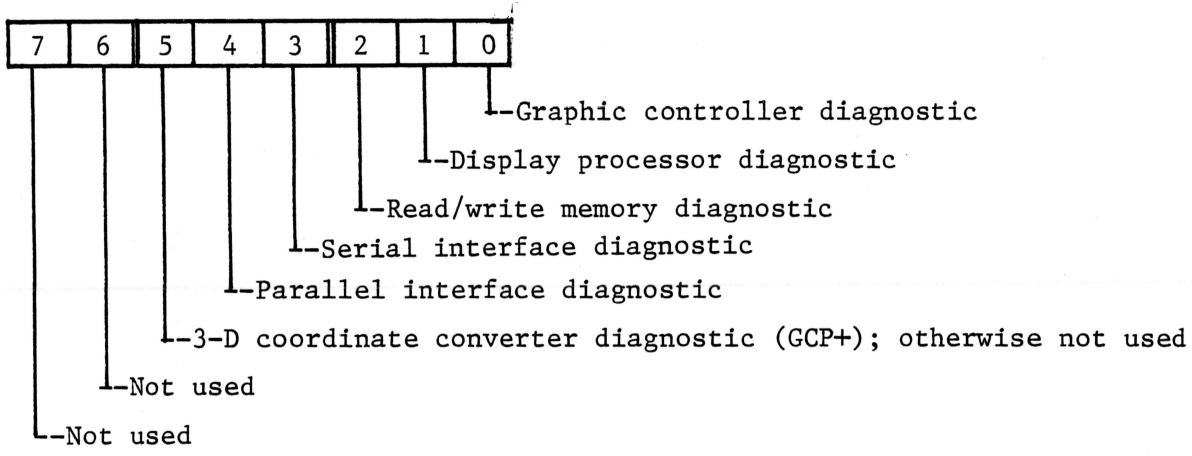
GCP+ firmware supports large memory systems as well as software options. For related programming information, see GRAPHIC 7 Options Reference Manual (H-79-0357) and GCP+ Programmer's Reference Manual (H-79-0348).

2.5 OPERATOR CHECKOUT PROCEDURE

Whenever the terminal controller is initialized in the LOCAL mode, the terminal controller performs its built-in diagnostic routines and presents the results of this self-test as part of the verification test pattern, as follows:

1. XX appears in the small box at the lower right portion of the verification test pattern. The presence of XX indicates that the 3-digit code at the lower left corner of the same box is the results of the built-in diagnostics.

The diagnostic code is a 3-digit octal representation of an 8-bit binary code whose bits are assigned as follows:



2. When a diagnostic routine detects a malfunction, the corresponding bit in the error code is set to 1; if no malfunction is detected, the bit is set to 0. The octal code displayed in the verification test pattern thus indicates the results of all diagnostic tests. For example, 000 indicates all tests passed; 077 (GCP+) or 037 indicates that all diagnostic tests failed. If the third digit is 4, 5, 6, or 7, the read/write memory diagnostic test failed.

(This paragraph applies to GCP+ only.) As part of the memory diagnostic test, you can examine the memory configuration. Address 000736 contains the RAM configuration word.

1. On keyboard, press RETURN 736/

2. The verification test pattern disappears and the display shows

000736 / nnnnnn

where nnnnnn is an octal code that describes the configuration of the installed read/write memory, as follows:

000400 = 16K	017400 = 80K
001400 = 32K	037400 = 96K
003400 = 48K	077400 = 112K
007400 = 64K	177400 = 128K

NOTE

The preceding paragraph does not apply to systems fitted with the G3 configuration of the 32K memory card.

SECTION 3

THEORY OF OPERATION

3.1 BASIC DESCRIPTION

The large read/write memory card allows the following operations to be performed:

1. Load five bits of data into the page registers.

2. Read a 16-bit word from memory.

3. Write a 16-bit word into memory.

4. Read eight least significant bits from memory.

5. Write eight least significant bits into memory.

6. Read eight most significant bits from memory onto the least significant bit lines of the processor data bus.

7. Write eight least significant bits from the processor data bus into eight most significant bit positions of memory.

When none of these operations is being performed, the memory runs through a continuing program of refreshing itself.

The major circuit blocks shown in figure 3-1 perform the following functions to support these operations.

a. Signal Inverters. The WRIT-B, ADRV-B, and ADnn-B signals are inverted and buffered to match the logic of the card and to allow multiple usage of the signals.

b. Page Register Control Circuits. The page register control circuits recognize when memory mapping is being invoked and which of the three page registers is being accessed. They also recognize whether the page registers are being accessed for a memory read/write operation, or whether new mapping information is being written into the page registers themselves. The inputs to the page register control circuits are those address bits that make up the address 17234X, the additional address bits that select a single page register, and a read/write instruction.

When new mapping information is being written into the page registers, these circuits also receive data bits DA00-B through DA04-B from the data control circuits.

The outputs from the page register control circuits are address bits P1-P5, which go to the address selection circuits and the data control circuits. Refer to figure 2-3 for the functions of these five bits.

The page registers are cleared by an active low REST-B.

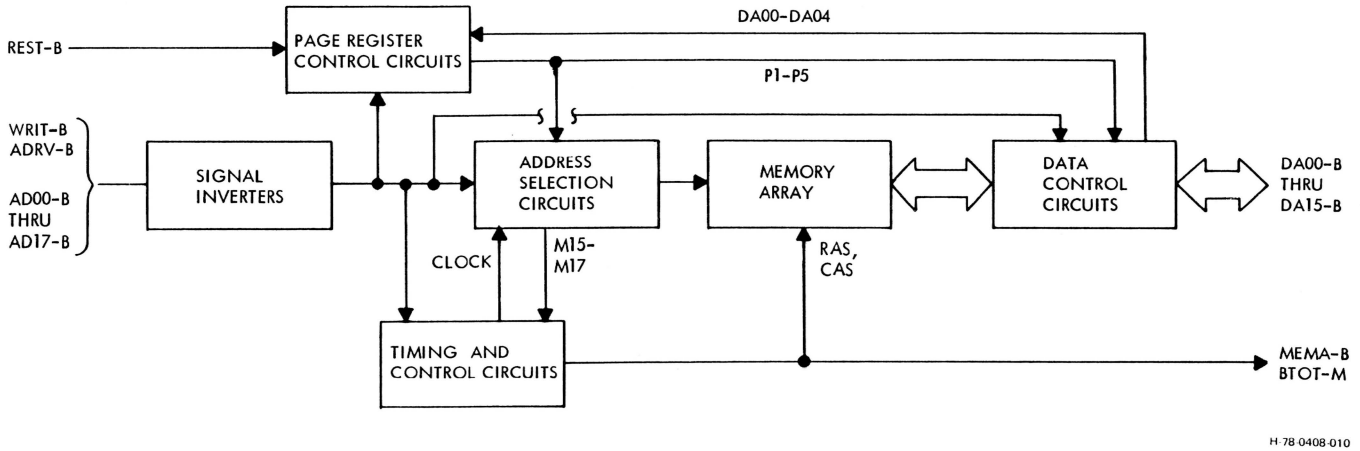


Figure 3-1. Large Read/Write Memory, Simplified Block Diagram

c. Address Selection Circuits. The address selection circuits address the memory array in a two-step operation: first the proper row in memory is selected, then all columns. The intersection of row and column is the location of the individual address.

When direct addressing is invoked, the address selection circuits compile the address from address bits AD01-B through AD17-B. When memory mapping is involved, the address selection circuits compile the address from address bits AD01-B through AD12-B plus bits P1 through P5 from the page register control circuits. When the memory is not being accessed by some external device, the address selection circuits perform the memory refresh operation. A counter in the address selection circuits generates sequential addresses for refresh.

The output from the address selection circuits consists of two groups of seven bits each, the first to select the row, the second the column. The timing of the address selection circuits is controlled by the timing and control circuits.

These row and column bits are applied to all 64 chips in the memory array. The appropriate signals from the timing and control circuits turn on only the appropriate chips to enable that address that was selected by the address selection circuits.

d. Timing and Control Circuits. The timing and control circuits produce the signals that turn on only the selected chips in the memory array that are selected by the address selection circuits. Two turn-on signals, RAS (row address strobe) and CAS (column address strobe), strobe in the row and column address information from the address selection circuits. RAS and CAS go only to selected chips in the memory array, as determined by bits M15 through M17 from the address selection circuits.

The timing and control circuits also generate clocking signals at 10 MHz and 20 MHz that regulate timing throughout the large read/write memory card.

The timing and control circuits also generate the memory acknowledge signal (MEMA-B) at the completion of a memory operation, and the time-out signal BTOT-M if for some reason a memory request does not get serviced.

e. Data Control Circuits. The data control circuits are the interface between the large read/write memory card and the DAnn-B lines on the processor bus. When data is to be written into either the memory array or the page registers, the data control circuits accept the information from the processor bus and pass it to its destination. When data is to be read from the memory array, the data control circuits accept the information from the memory array and pass it to the processor bus.

When the data to be read or written is an eight-bit byte, the data control circuits select the appropriate high/low byte of memory address for connection to the least significant bit lines of the processor data bus.

f. Memory Array. The memory array is organized as a matrix consisting of four rows and 16 columns. Each row represents a word, and each column represents a bit of that word. At the intersection of each row and column, there is a 16K x 1 bit dynamic random access memory device. Therefore, each row represents $16{,}384_{10}$ 16-bit

words. Total storage for the array (four rows) is $65{,}536_{10}$ 16-bit words. Each 16-bit word is divided into two 8-bit bytes by separate read/write control lines, allowing selection of the high or low byte when needed.

3.2 DETAILED DESCRIPTION.

Refer to figure 3-2 in this section and to engineering drawing 1089726 in Section 6.

3.2.1 CARD POWER

The large read/write memory card receives +5V (P05V+), +15V (P15+), and -15V (N15-) from the terminal controller power supply.

The +5V is filtered and distributed in four discrete fanouts, three of which go to logic devices and one goes to the memory array. The four fanouts are decoupled from each other.

Voltage regulator VR1 and its associated components reduce the +15V input to +12V for the devices in the memory array.

Voltage regulator VR2 and its associated components reduce the -15V input to -5V for the devices in the memory array.

3.2.2 PAGE REGISTER CONTROL CIRCUITS

a. Page Register Decoder. When ADDRESS VALID (ADRV-B) is true, the register decoder responds to address 17234X, where X has the value 2, 4, or 6. When WRIT-B is also true, one of the three page registers is to receive new data. When WRIT-B is not true, then the contents of the selected page register are to be made available to the address selection circuits.

b. Read/Write Page Register Control. When the register decoder responds to a page register address, a high at the output of U40D is applied to the A and B inputs of register U9. The 10 MHz clocking signals from the timing and control circuits make this high available at the register QB and QC outputs.

c. Write Selected Page Register. U48B is a 2-line to 3-line decoder. When the read/write page register control QB output is high and WRIT-B is also true, the output of U10B strobes address bits A1 and A2 into U48B. These two bits select one of the three page registers, as follows:

ADDRESS	A2	A1	PAGE REGISTER
172342	low	high	U22 (page register 1 on card 1 or page register 4 on card 2)
172344	high	low	U12 (page register 2 on card 1 or page register 5 on card 2)
172346	high	high	U2 (page register 3 on card 1 or page register 6 on card 2)

NOTE

Page register selection is the same on both cards of a two-card memory, but the memory control circuit on the card not being addressed is inhibited by the read/write inhibit circuit in the timing and control circuits.

The output of U48B clocks the new data into the selected page register. This is how a page register gets loaded with bits D0 through D4 from the data control circuits.

d. Read Selected Page Register. The 15 bits representing the outputs of the page registers are always applied to the page register output multiplexer. The read selected page register circuit, when enabled, determines which set of five bits pass through the multiplexer.

The read selected page register circuit is enabled when the register decoder recognizes a valid address 17234X. Then bits A1 and A2 form a code (as for the write selected page register circuit) through which U38A enables the page register output multiplexer to pass one set of five bits from the selected page register.

When direct addressing is invoked and bit AD15-B is high (bit A15 is low; the desired address is less than 16K), data selector U38A is also enabled. In this case bits A13 and A14 form the code that selects the output of one page register to pass through the multiplexer. However, in this case, the selected page register must have been loaded with all zeroes; otherwise the result will be inadvertent paging.

e. Page Registers. The page registers (U2, U12, U22) are hex D-type flip-flops. Each stores five bits of data (D0-D4) that correspond to memory page numbers, as explained in Section 2. They get loaded as described under Write Selected Page Register and are read as described under Read Selected Page Register.

f. Page Register Output Multiplexer. Devices U1, U11, and U21 constitute five 3-line to 1-line data selectors, one for each bit stored in the page registers. The selected input bits are connected to the outputs in response to the code from the read selected page register circuit.

3.2.3 ADDRESS SELECTION CIRCUITS

a. Refresh Address Counter. Devices U26 and U27 comprise a synchronous 7-bit counter that gets clocked every 15 microseconds (66.667 kHz rate). When the read/write memory card is not otherwise engaged, it continually refreshes itself. The refresh address counter steps through its 128 addresses in 2.0 milliseconds, then repeats. Its output consists of refresh address bits R0 - R6, which go to the memory address multiplexer.

b. Comparator. Comparator U4 continually monitors the output of the page register output multiplexer. If the five outputs of the page register output multiplexer (P1 - P5) are all zeroes, the comparator sends a high output to the address gate.

Similarly, gate U10C passes a high ADDRESS VALID signal, provided that the output of U17D is high and the output comparator U16 in the read/write inhibit circuit is also high.

Either a REFRESH REQUEST or an ADDRESS VALID, when the other signals are high, produces a high at the output of U29A, which starts the memory control circuit.

d. Memory Control. The memory control circuit generates the timing signals that trigger the RAS generator, memory address multiplexer, CAS generator, and busy/timeout circuit in the proper sequence. The heart of the memory control circuit is a fourstage ripple counter, U14 and U15.

A high output from U29A in the refresh request/inhibit cycle gates circuit clocks U19B, priming gates U30A and U10A. The same high output from U29A, inverted by U20B, presets flip-flop U18B. The high Q output of U18B passes through gate U17B (the other input to U17B is high at this time) and ripples successively through U14A, U14B, U15A, and U15B. Each of these flip-flops is clocked by the 20 MHz signal from the timing generator. When U15B clocks high, its low $\overline{Q}$ output disables U17B, so that a low level starts rippling through the counter.

When U14A receives the high input, its $\overline{Q}$ output goes low and triggers the RAS generator circuit through U17A. When U14B receives the high, its high Q output strobes the memory address multiplexer, selecting the CAS address. When U15A receives the high, its high Q output clocks the CAS generator.

Whether or not a CAS signal is generated depends on whether the cycle was started by a REFRESH REQUEST or an ADDRESS VALID signal. If the cycle was started by a REFRESH REQUEST signal, the ADDRESS VALID signal remains low throughout the cycle, keeping U25B in its clear state; further, the D input to U25B is low, thus preventing generation of a CAS signal. If the cycle was started by an ADDRESS VALID signal, the high ADDRESS VALID signal unblocks U25B and the D input to U25B is high, which gets clocked through by the Q output of U15A.

When flip-flop U18B is preset at the beginning of the cycle, its $\overline{Q}$ output is gated through U17D to disable the refresh request/inhibit cycle gates for the duration of the memory cycle. At the end of the cycle (after the high has passed through the ripple counter and been replaced by the rippling low), the $\overline{Q}$ output of U15B goes high and clocks U18B, removing the low from the input to U17D.

At that point in the cycle when the Q output of U15B is still high but the $\overline{Q}$ output of U15A has gone high, the output of U10A goes low to preset U19A. The Q output of U19A goes low, clearing U19B. This is the normal or static condition that prevails between memory cycles. A new REFRESH REQUEST changes the states of U19A and U19B; a new ADDRESS VALID signal does not change their states.

Figure 3-3 shows the timing signals associated with memory control.

e. RAS Generator. The function of the RAS generator is to produce either a single low $\overline{\text{RASn}}$ strobe in response to an ADDRESS VALID input or four low $\overline{\text{RASn}}$ strobes in response to a REFRESH REQUEST input.

In the ADDRESS VALID case, gate U30A is disabled by a low input from U19B. When the output of U17A in the memory control circuit goes low, it strobes 2-line to 4-line multiplexer U24. One output of the multiplexer goes low, as determined by the values of bits M15 and M16 from the address selection circuits. The selected low output is gated through U86 to the proper row in the memory array.

In the REFRESH REQUEST case, gate U30A is enabled. When the output of U17A goes low, the output of U30A also goes low and activates all four RAS signals to the memory array. The memory array cells that get refreshed in this case are a function of the output of the refresh address counter in the address selection circuits. If there is no interruption by an ADDRESS VALID input, the entire memory gets refreshed by 128 REFRESH REQUEST cycles in a 2-millisecond period.

___ f. CAS Generator. The function of the CAS generator is to produce four low CASn signals in response to an ADDRESS VALID input, and not to generate any CASn signal in response to a REFRESH REQUEST input. The CAS generator consists of flip-flop U25B and four inverters. The action of U25B is described under Memory Control. In the ADDRESS VALID case, the low $\overline{Q}$ output of U25B goes to U17D to disable any further inputs until the operation is complete. The high Q output of U25B also clocks U39A in the read/write lo/hi byte control circuit (part of the data control circuits).

g. MEMA/Timeout Circuit. The MEMA/timeout circuit consists of timer U28B, flip-flops U39B, U25A, and six inverters. The functions of the MEMA/timeout circuit are to generate the MEMA-B (MEMORY ACKNOWLEDGE) signal that indicates the completion of certain activities, and to generate the BTOT-M (BUS TIMEOUT) signal if the memory fails to complete a cycle in response to an ADDRESS VALID input.

When the page register address is detected, the read/write page register control generates the MEMA-B signal to indicate to the display processor that the page register decoder has recognized the page register address 17234X. The high QC output of register U9, inverted by U50B, becomes the MEMA-B signal.

In the ADDRESS VALID case, the high ADDRESS VALID signal starts timer U28B. The low $\overline{Q}$ output of U19B is applied to the D input of U25A. When (during the memory control cycle) the $\overline{Q}$ output of U15A goes high, it clocks U25A. The low $\overline{Q}$ output of U25A, twice inverted, becomes the MEMA-B signal.

When MEMA-B goes low, the device that generated the ADDRESS VALID signal clears that signal. The ADDRESS VALID clears timer U28B and flip-flops U39B and U25A.

If the timer times out (approximately 12 microseconds), the low-to-high transition of the timer $\overline{Q}$ output clocks flip-flop U39B. The low $\overline{Q}$ output of U39B, twice inverted, produces both the MEMA-B and BTOT-M signals. The MEMA-B signal terminates the ADDRESS VALID signal. The BTOT-M signal indicates that the memory cycle was not completed.

In the G1 and G3 configurations of the large read/write memory, a jumper is installed from E2 to E3 to disable the preset terminals of U25A and U39B. In the G2 and G4 configurations, the jumper is installed from E2 to E1. If address bit M16 goes high, indicating an address higher than 32K-1, the output of inverter U50F goes low; this low presets U39B and U25A and immediately produces both the MEMA-B and BTOT-M signals, indicating that the memory card does not contain the address specified.

3.2.5 DATA CONTROL CIRCUITS

a. Data Input/Output Multiplexer. Multiplexers U32, U33, U46, and U47 are tri-state devices. The multiplexers pass processor bus DAnn-B data to the memory banks as the Dnn data bits at all times. When so directed by LO BYTE/HI BYTE signals from the read/write lo/hi byte control circuit, the multiplexers pass the memory output bits Onn to the same processor bus. When the LO BYTE/HI BYTE signals are inactive, the connections between Onn and DAnn-B are at a high impedance level.

Each multiplexer acts as both an input and output register. Each register contains four bits of the 16-bit data word. Operation of the registers depends on the status of the read/write command and the status of the byte select signals.

b. Read/Write Lo/Hi Byte Control. The read/write lo/hi byte control circuit, in response to the levels of the BYTE-B, ADOO-B, and WRIT-B inputs, performs the following functions:

BYTE-B	ADOO-B	WRIT-B	FUNCTION
H	H	H	Read 16-bit word from memory
H	H	L	Write 16-bit word into memory
H	L	H	Illegal - no response
H	L	L	Illegal - no response
L	H	H	Read 8 LSBs from memory; MSBs on bus = 0
L	H	L	Write 8 LSBs into LSB locations in memory; MSB locations are not altered
L	L	H	Read 8 MSBs from memory onto bus LSB lines; bus MSB lines = 0
L	L	L	Write 8 LSBs from bus into MSB locations in memory; memory LSB locations are not altered

(1) Read/Write Decision. The memory write command is a low from U8A (lo byte) and/or U8B (hi byte). When WRIT-B is high (indicating a read operation), the output of U30B is high, and the outputs of U8A and U8B are both high.

Similarly, during a refresh operation, the $\overline{Q}$ output of U19B is low, the output of U30B is high, and the outputs of U8A and U8B are both high.

When WRIT-B is low (indicating a write operation), and the $\overline{Q}$ output of U19B is high (indicating an ADDRESS VALID case), then the output of U30B is low. If BYTE-B is high (indicating a 16-bit operation), then the outputs of U8A and U8B are both low, and 16 bits of data may be written into memory.

If WRIT-B is low (indicating a write operation), and the $\overline{Q}$ output of U19B is high (indicating an ADDRESS VALID case), and BYTE-B is low (indicating an 8-bit operation), then either U8A or U8B has a low output (but not both), depending on the state of the AD00-B signal. If AD00-B is high, the output of U8A is low, permitting writing into the LSB locations in memory. If AD00-B is low, the output of U8B is low, permitting writing into the MSB locations in memory.

(2) Lo/Hi Byte Decision. Figure 3-2 shows that, for data flow from the data bus to the memory array all 16 bits enter the data input/output multiplexer. However, only the eight LSBs go directly from the input/output multiplexer to the memory array. All 16 bits go from the input/output multiplexer through the byte swap multiplexer to the memory array. This arrangement allows the following three possibilities:

- Write 16-bit word into memory
- Write 8 LSBs into LSB locations in memory; MSB locations are not altered
- Write 8 LSBs from bus into MSB locations in memory; memory LSB locations are not altered

Similarly, for data flow from the memory array to the data bus, only the eight MSBs go directly from the memory array to the data input/output multiplexer. However, all 16 bits go through the byte select multiplexer to the input/output multiplexer. This arrangement allows the following three possibilities:

- Read 16-bit word from memory
- Read 8 LSBs from memory; MSBs on bus = 0
- Read 8 MSBs from memory onto bus LSB lines; bus MSB lines = 0

In the write case, when AD00-B is high, the byte swap multiplexer (U36, U37) passes the eight MSBs from the input/output multiplexer to the memory array. When AD00-B is low, the byte swap multiplexer passes the eight LSBs from the input/output multiplexer to the memory array. In either case, the outputs of the byte swap multiplexer go to the MSB locations in memory.

In the read case, the MSB bits from memory (bits D08 - D015) are always supplied to the MSB half of the data input/output multiplexer (U46, U47). All 16 bits from memory are applied to byte select multiplexer (U31, U41, U42, U43). The state of the AD00-B signal determines whether the MSB bits or the LSB bits get applied to the LSB half of the data input/output multiplexer (U32, U33). When AD00-B is high, the LSB bits are selected; when AD00-B is low, the MSB bits are selected.

Putting the bits applied to the data input/output multiplexer onto the data bus lines is a separate operation. When the LO BYTE or HI BYTE signals go low, the data is transferred to the data bus lines. When the LO BYTE or HI BYTE signals are high, the data input/output multiplexer is held in its high impedance state, and the lines are held at a logic high (logic 0) level.

The LO BYTE and HI BYTE signals are controlled by flip-flop U39A and gates U30C, U30D. In the REFRESH REQUEST case, the D input to U39A is high. As a result, both the LO BYTE and HI BYTE lines are high, and there is no output from the data input/output multiplexer.

In the ADDRESS VALID case, the D input to U39A is low; the trailing edge of $\overline{CAS}$ clocks U39A, making the LO BYTE line low. Whether the HI BYTE goes low or not then depends on the state of the BYTE-B input.

(3) Reading Page Register Contents. As a special case, an address of 17234X with WRIT-B, AD00-B, and BYTE-B held high reads the contents of the addressed page register. In this case, the low output of U29B applied to the byte select multiplexer puts bits P1 - P5 on the line to the data input/output multiplexer; the other three bits are hard-wired high (logic 0). The low output of U29B also clears flip-flop U39A; the LO BYTE line goes low, placing bits P1 - P5 on the data bus lines. The HI BYTE line also goes low, but because there is no CAS strobe, the memory is not accessed. The MSB bytes are all high (logic 0).

c. Byte Swap Multiplexer. The byte swap multiplexer (U36, U37) is involved only in a memory write operation. Its use is described under Read/Write Lo/Hi Byte Control. When AD00-B is high, the multiplexer passes the eight MSBs to the memory array. When AD00-B is low, the multiplexer passes the eight LSBs to the memory array.

d. Byte Select Multiplexer. The byte select multiplexer (U31, U41, U42, U43) is involved only in a memory read operation. Its use is described under Read/Write Lo/Hi Byte Control. When the B inputs are low, the multiplexer passes bits P1 - P5 (and the associated hard-wired bits) to the LSB portion of the data input/output multiplexer. When the B inputs are high, the output selected depends on the level of the A inputs. High A inputs select the most significant bits from memory; low A inputs select the least significant bits from memory.

3.2.6 MEMORY ARRAY

The individual memory device is a dynamic random access MOS memory circuit, organized as $16{,}384_{10}$ words by 1 bit. The device features multiplexed address inputs, permitting it to be packaged in a standard 16-pin chip. Other features are low power (less than 462 mW active) and fast access time (200 ns maximum).

Each memory chip is configured as a 128 bit by 128 bit cell for addressing purposes. Seven row addresses are latched onto the chip by a low-going $\overline{RAS}$ signal; then seven column addresses are latched onto the chip by a low-going $\overline{CAS}$ signal.

Whenever $\overline{CAS}$ is high, the memory data output lines are held floating in a high impedance state. The output contains a logic 0 or 1 only during the access time of a read cycle.

Chips that do not receive the $\overline{RAS}$ signal remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

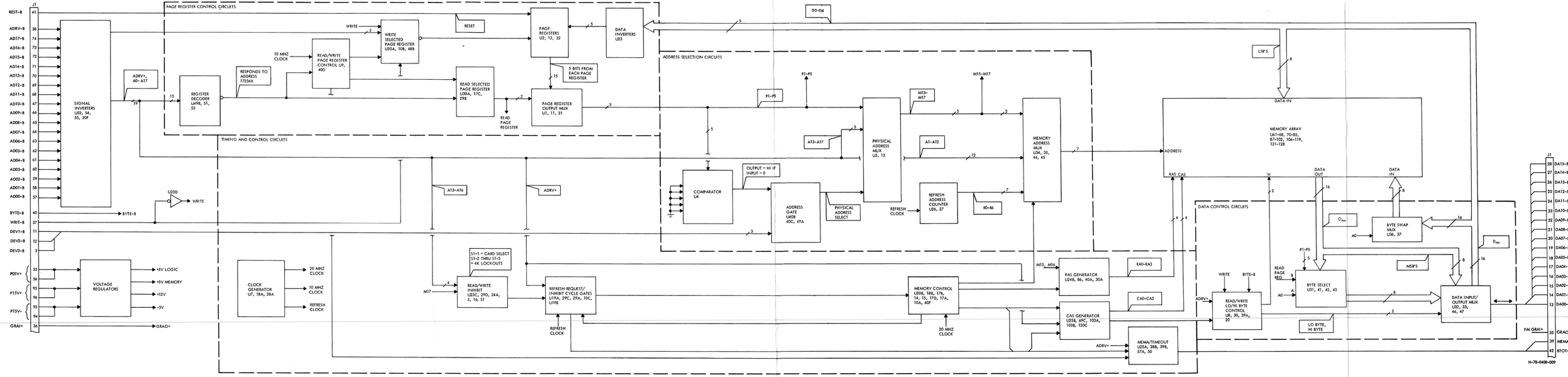


Figure 3-2. Functional Block Diagram

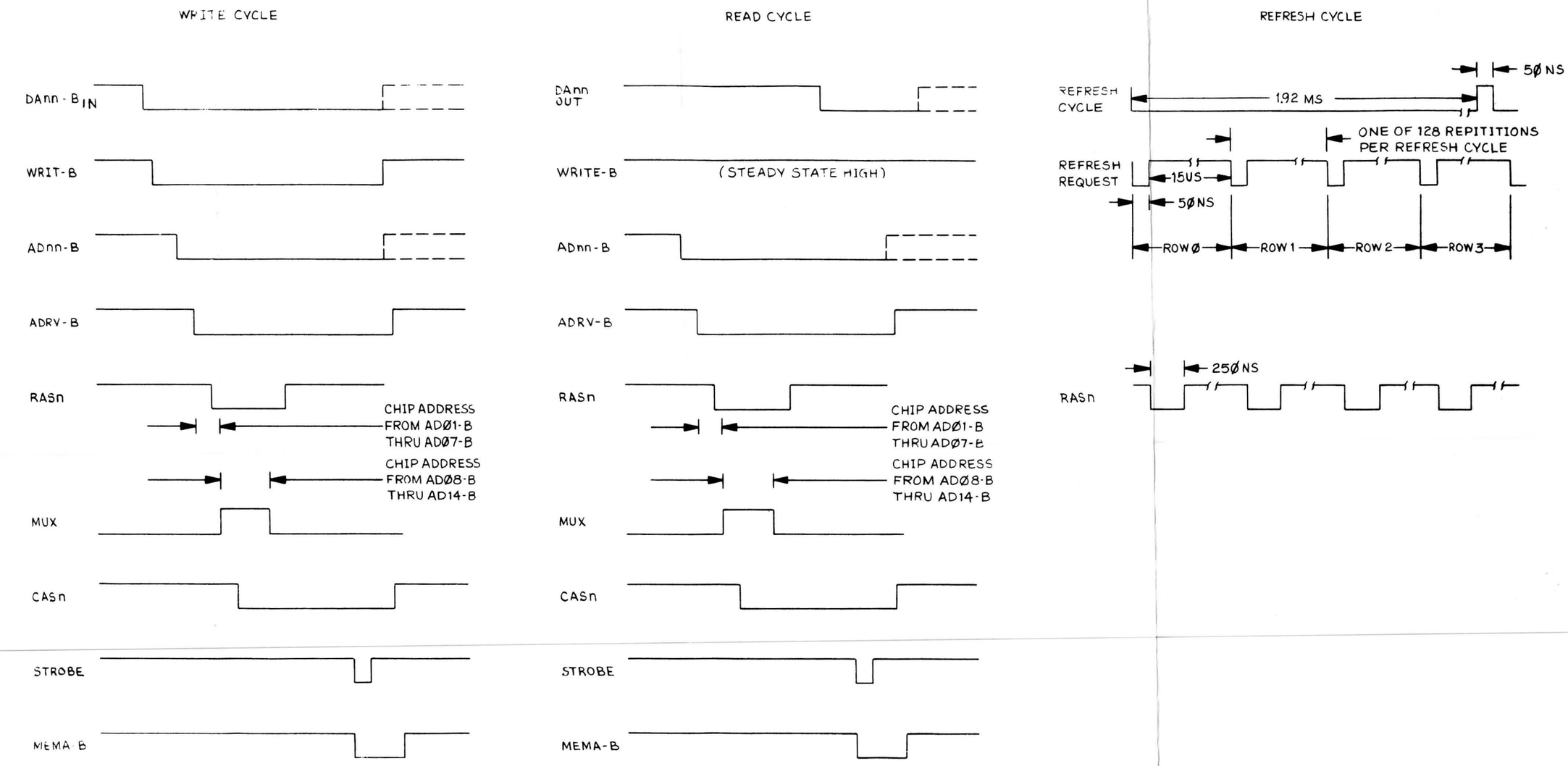


Figure 3-3. Write Cycle, Read Cycle, and Refresh Cycle Timing

SECTION 4

INSTALLATION

4.1 UNPACKING AND VISUAL INSPECTION

Inspect the shipping container carefully. If the container shows any evidence of rough handling or is sufficiently damaged to have affected the contents, notify Sanders Associates, Inc., and the carrier immediately.

After removing the large read/write memory card from the container, inspect the card assembly for any signs of damage. If the unit appears damaged in any way, notify Sanders Associates, Inc., immediately.

4.2 COMPATIBILITY WITH GRAPHIC CONTROLLER

Confirm that the graphic controller card in slot 1A1A10 in the terminal controller is part number 1089845. Do not use the large read/write memory card with a graphic controller card part number 1086758.

4.3 SWITCH SETTINGS AND JUMPER CONNECTIONS

Confirm that switches are set and jumpers installed as shown in table 4-1.

Table 4-1. Switch Settings and Jumper Connections

MEMORY CONFIGURATION	S1 SWITCH POSITIONS CARD #1	CARD #2	JUMPER CONNECTIONS CARD #1	CARD #2
16K	S1-1 thru S1-5 ON	N/A	E2-E3	N/A
32K (G2 configuration)	S1-1 ON S1-2 thru S1-5 OFF*	N/A	E2-E3	N/A
48K	S1-1 ON S1-2 thru S1-5 OFF*	N/A	E1-E2	N/A
64K	S1-1 ON S1-2 thru S1-5 OFF*	N/A	E1-E2	N/A
94K	S1-1 ON S1-2 thru S1-5 OFF*	S1-1 OFF S1-2 thru S1-5 OFF*	E1-E2	E2-E3
112K	S1-1 ON S1-2 thru S1-5 OFF*	S1-1 OFF S1-2 thru S1-5 OFF*	E1-E2	E1-E2

* - These switch positions allow access to all available memory and may be changed to mask out undesired memory blocks.

Table 4-1. Switch Settings and Jumper Connections (Cont)

MEMORY CONFIGURATION	S1 SWITCH POSITIONS CARD #1	CARD #2	JUMPER CONNECTIONS CARD #1	CARD #2
128K	S1-1 ON S1-2 thru S1-5 OFF*	S1-1 OFF S1-2 thru S1-5 OFF*	E1-E2	E1-E2
32K (G3 configuration)	S1-1 thru S1-5 ON	N/A	E2-E3	N/A

* - These switch positions allow access to all available memory and may be changed to mask out undesired memory blocks.

4.4 INSTALLATION

1. Turn off ac power at the terminal controller.

2. Remove any 8K memory cards present in the card cage (1A1A1, 1A1A2, 1A1A3).

3. Install the large read/write memory card in the applicable card cage slot (normally 1A1A1).

NOTES

If more than one large read/write memory card is to be installed, the card in the lowest numbered slot is card no. 1.

If two large read/write memory cards are to be installed, of which one is a 64K card and the other is a 32K or 16K card, then the 64K card must be in the lower numbered slot and must be card no. 1. The other card should be in the next higher slot.

If any slot between XA1 and XA8 is left vacant as a result of this installation, connect jumper assembly (Sanders part no. 47067) between pins 35 and 36 (the priority grant line) of the vacant slot. Connect jumper assembly at the back plane.

SECTION 5

MAINTENANCE

5.1 MAINTENANCE PHILOSOPHY

The overall maintenance approach is based on using the large read/write memory checkout procedure in paragraph 2.5. The large memory card is an off-the-shelf item and is not field repairable. Maintenance is limited to fault isolation at the circuit card level.

5.2 TEST POINT INFORMATION

There are six test points on the large read/write memory card, accessible when the memory card is mounted on a card extender. Table 5-1 describes the signals present at these test points.

Table 5-1. Test Point Information

TEST POINT	SIGNAL NAME	DESCRIPTION
1	--	Goes high when U18B is preset by either a read/write command or a REFRESH REQUEST command; goes low at the end of the ripple counter cycle (350 nanoseconds).
2	INHIBIT CYCLE	Goes low if the addressed card or 4K memory block has been locked out. If this point goes low, TP1 should not go high; TP4 should go low after approximately 10 microseconds.
3	REFRESH REQUEST	15 microseconds high, 50 nanoseconds low, continuous.
4	MEMA-B	Normally high, goes low on completion of a read/write cycle or at the end of timeout; remains low until ADRV-B goes high.
5	ADDRESS VALID	ADRV-B inverted. Goes high to initiate a read/write command. Remains high until MEMA-B goes low, then is reset by the device that accessed the memory.
6	READ/$\overline{\text{WRITE}}$	Same as WRIT-B. Normally high, goes low when accessing device issues a write command.

SECTION 6

DRAWINGS

This section contains the following drawings:

Large Read/Write Memory Assembly Parts List	PL1089724
Large Read/Write Memory Assembly	1089724
Large Read/Write Memory Logic	1089726

REVISION STATUS

PARTS LIST	SH	1	2	3	4	5	6	7	8	9	10	11	12
	REV	N	M	M	M	M	M	M	N	M	L		
	SH	13	14	15	16	17	18	19	20	21	22	23	24
	REV												

DWG REV	J
WL REV	N/A

4. ITEM NUMBERS WITH SUBSCRIPTS ARE ALTERNATE ITEMS. SELECT ONE ONLY.

3. FOR AUTHORIZED COMPONENT SUBSTITUTION LIST SEE DWG SA1088588.

2. PARTS LIST SHEET ONE IS THE CONTROLLING REVISION FOR THE COMBINED PARTS LIST, DRAWING AND WIRE LIST.

1. SHOP PRACTICE TOLERANCES AND DRAWING INTERPRETATION WITHIN 815002 SUPPLEMENT THIS DRAWING.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED	
—	REL FOR DEVELOPMENT	9 FEB 78	RT/AOT	
A	REV PER ENG	28 FEB 78	AB/	
B	CHANGED ITEM 30, 31, 35 PER ENG	13 APR 78	AB/	
C	REV PER ENG	4 MAY 78	WG/	
D	CHANGED ITEM 9 REL FOR PROD	6 JUN 78	RL/ RLB	M
E	REV PER ECO 76264	2 NOV 78	WG/ RLB	M
F	REV PER ECO 76316	11 APR 79	WG/WL	
G	REV PER ECO 76326			M
H	REV PER ECO 76474	31 OCT 79	WG/WL	
J	REV PER ECO 76480			M
K	REV PER ECO 96257A	2 JAN 80	ROM/WL	M
L	REV PER ECO 96388	9 MAY 80	MB/WL	M
M	ECO 96913A SEE DWG REV H	23 MAY 80	PNK/ OK	M
N	REV PER ECO 96990	16 OCT 80	WG/WL	M

PRODUCTION
CHANGE BY ECO ONLY

MFG Vpch 8-2-78

NEXT ASSY	USED ON
	GRA-7

APPLICATION

CONT NO.

DRFTG	DR W. Gurgowski	4 MAY 78
	APPD	18 JUL 78
	CHK	
ENGRG	DEV E. Roth	6-6-78
	E/M	
	PROJ	8/7/78

SANDERS ASSOCIATES, INC NASHUA, NEW HAMPSHIRE

CIRCUIT CARD ASSY, LARGE MEMORY

SIZE	CODE IDENT NO.	
A	94117	PL 1089724

SHEET 1 OF 10

OP—1039 REV B

DWG SIZE E

PARTS LIST

ITEM NO.	QTY PER ASSY G1	G2	G3	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
1	1	1	1			1089725G1	CIRCUIT CARD SUBASSY 64K MEMORY	
2	64	—	—		12881	MK4116P-3	MED, U61,62,63,64,65,66,67,68,70,71, 72,73,74,75,76,77,78,79,80,81,82,83,84,85, 87,88,89,90,91,92,93,94,95,96,97,98,99, 100,101,102,104,105,106,107,108,109,110, 111,112,113,114,115,116,117,118,119,121,122,123, 124,125,126,127,128 (MOSTEX)	
2A	REF	REF	REF			UPD416C-2	MED, (NEC) (SEE NOTE 4)	
2B	REF	REF	REF		07263	F16K3DC	MED (SEE NOTE 4) (FAIRCHILD)	
3	2	2	2		07263	F93S46PC	MED, U4,16 (FAIRCHILD)	
4	1	1	1		07263	F96S02PC	MED, U28 (FAIRCHILD)	
5	1	1	1		07263	F9S42PC	MED, U8 (FAIRCHILD)	
6	4	4	4		27014	DS8833N	MED, U32,33,46,47 (NATIONAL)	
7	2	2	2			SN7400N	MED, U29,30	
8	1	1	1			SN74S02N	MED, U5	
9	11	11	11			SN74S04N	MED, U3,20,23,40,52,54,55,57,69,103,120	
10	1	1	1			SN74S05N	MED, U50	
11	2	2	2			SN74S08N	MED, U17,86	
12	1	1	1			SN7410N	MED, U10	
13	1	1	1			SN74S20N	MED, U49	
14	1	1	1			SN7421N	MED, U53	
15	1	1	1			SN7425N	MED, U51	

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1089724

REV M | SHEET 2

OP—277 REV C

PARTS LIST

ITEM NO.	QTY PER ASSY G1	G2	G3	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
16	5	5	5			SN74S74N	MED. U14.15.18.19.25	
17	1	1	1			JKPT080-1330071	CRYSTAL OSCILLATOR 20.0 MHZ U7(SEE NOTE 4)CTS KNIGHT	
18	2	2	2			SN74S139N	MED, U24,48	
19	11	11	11			SN74S153N	MED, U1,11,21,31,34,35,41,42,43,44,45	
20	5	5	5			SN74S157N	MED, U13,36,37,38,56	
21	2	2	2			SN74LS163N	MED, U26,27	
22	1	1	1			SN74LS164N	MED, U9	
23	3	3	3			SN74LS174N	MED, U2,12,22	
24	1	1	1		07263	UA7812UC	VOLTAGE REGULATOR +12 VDC, VR1 (FAIRCHILD)	
25	1	1	1		07263	UA79M05AHC	VOLTAGE REGULATOR -5 VDC, VR2 (FAIRCHILD)	
~~26~~	~~1~~	~~1~~	~~1~~			~~RNC55H3161FS~~	~~RES, MIL-R-55182/1, 3.16K, ±1%, .10W, R1~~	
~~27~~	~~1~~	~~1~~	~~1~~			~~RNC55H2151FS~~	~~RES, MIL-R-55182/1, 2.15K, ±1%, .10W, R2~~	
28	1	1	1			RCR07G223JS	RES, 22K OHMS, ±5%, .25W, R3	
29	1	1	1			RCR07G243JS	RES, 24K OHMS, ±5%, .25W, R4	
30	22	22	22			RCR07G200JS	RES, 20 OHMS, ±5%, .25W, R5,6,7,8,9,10, 11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26	
31	2	2	2			RCR07G360JS	RES, 36 OHMS, ±5%, .25W, R33,34	
32	1	1	1			RCR07G302JS	RES, 3K OHMS, ±5%, .25W, R27	
33	5	5	5			RCR07G512JS	RES, 5.1K OHMS, ±5%, .25W, R28,29,30,31,32	
34	2	2	2			RCR07G102JS	RES, 1K OHMS, ±5%, .25W, R35,36	
~~35~~	~~1~~	~~1~~	~~1~~			~~CM05ED240JP3~~	~~CAP, 24PF, ±5%, 500 WVDC, C1~~	
36	2	2	2			CK05BX102K	CAP, 1000PF, ±10%, 200 WVDC, C2,3	

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1089724

REV M | SHEET 3

OP—277 REV C

PARTS LIST

ITEM NO.	QTY PER ASSY G1	G2	G3	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
37	9	9	9			M39003/01-2304	CAP, 6.8 UF, ±10%, 35 WVDC, C4,5,10,11, 12,13,14,15,16	
38	1	1	1			M39003/01-2347	CAP, .33 UF, ±10%, 50 WVDC, C6	
39	10	10	10			M39003/01-2356	CAP, 1.0 UF, ±10%, 50 WVDC, C7, 9, 17, 18, 19, 20, 21, 22, 23, 24	
40	1	1	1			M39003/01-2362	CAP, 2.2 UF, ±10%, 50 WVDC, C8	
41	110	—	—			CK05BX104K	CAP, 0.1 UF, ±10%, 50 WVDC, C25 - C134	
	—	78	—			CK05BX104K	CAP, 0.1 UF, ±10%, 50 WVDC, C25-C77, C82, C87-C94, C103-C118, C25	
	—		78			CK05BX104K	CAP, 0.1 UF, ±10%, 50 WVDC, C25-C69, C82, C87-C110, C119-C126	
42	4	4	4			7011935P1	INDUCTOR L1, 2, 3, 4	
43	1	1	1		31514	1008-692	SWITCH, S1 (SAE)	
44	1	1	1		13103	6073B	HEAT SINK (THERMALLOY)	
45	1	1	1			1086608P18	CONN, ELEC, PC BOARD	
46	2	2	2		07707	6010	EYELET	
47	2	2	2	A		600107P1	EJECTOR, CARD	
48	2	2	2	A		630003P14	EYELET, METALLIC	
49	1	1	1	A		640049P1	TRANSIPAD	
								≠ ≠ ≠

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1089724
	REV M	SHEET 4

OP—277 REV C

PARTS LIST

ITEM NO.	QTY PER ASSY G1	G2	G3	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
50	1	1	1			MS51957-14	SCREW, MACH, PAN HD, .112-40 x .31 LG	
51	1	1	1			MS15795-803	WASHER, FLAT-METAL, .125 ID x .25 OD	
52	1	1	1			MS21083C04	NUT, SLFLKG, HEX, .112-40	
53	REF	REF	REF	J		1089726	LOGIC DIAGRAM, 64K MEMORY	
54	6	6	6	A		165046P1	TEST POINT, TP1-TP6	≠
55	AR	AR	AR	A		93002P1	SOLDER	
56	1	1	1			SN74LS74N	MED, U39	
57								
58	3	3	3			RCR07G331JS	RES, 330 OHMS, ±5%, .25W, R37,38,39	
59	AR	AR	AR			270006P5	INSULATION TUBING, ELEC.	
60	AR	AR	AR	A		278002P13	WIRE, ELEC, UNINSUL, 22 AWG	≠
61	REF	REF	REF	A		815003	PW AND CKT BD, REQT FOR	
62	—	32	—		12881	MK4116P-3	MED, U61,62,63,64,65,66,67,68,70,71,72,73, 74,75,76,77,78,79,80,81,82,83,84,85,87,88, 89,90,91,92,93,94 (MOSTEX)	
63	—	—	32		12881	MK4116P-3	MED, U61,62,63,64,65,66,67,68,70,71,72, 73,74,75,76,77,95,96,97,98,99,100,101, 102,104,105,106,107,108,109,110,111	
64								
65	AR	AR	AR			276000P26	WIRE, ELEC INSUL, 22 AWG	
62A	—	REF	—			UPD416C-2	MED, (NEC) (SEE NOTE 4)	
63A	—	—	REF			UPD416C-2	MED, (NEC) (SEE NOTE 4	
17A	REF	REF	REF			MX040-20MHZ	CRYSTAL OSCILLATOR 20.0MHZ. U7 (SEE NOTE 4) CTS KNIGHT	

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	PL 1089724
A	94117	
	REV M	SHEET 5

PARTS LIST

ITEM NO.	QTY PER ASSY G4	QTY PER ASSY G5	QTY PER ASSY G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
1	1	1				1089725G1	CIRCUIT CARD SUBASSY 64K MEMORY	
2	–	48			12881	MK4116P-3	MED, U61,62,63,64,65,66,67,68,70,71, 72,73,74,75,76,77,78,79,80,81,82,83,84,85, 87,88,89,90,91,92,93,94,95,96,97,98,99, 100,101,102,104,105,106,107,108,109,110, 111,~~112,113,114,115,116,117,118,119,121,122,123,~~ ~~124,125,126,127,128~~ (MOSTEX)	
2A	REF	REF				UPD416C-2	MED (NEC) (SEE NOTE 4)	
2B	REF	REF			07263	F16K3DC	MED (SEE NOTE 4) (FAIRCHILD)	
3	2	2			07263	F93S46PC	MED, U4,16 (FAIRCHILD)	
4	1	1			07263	F96S02PC	MED, U28 (FAIRCHILD)	
5	1	1			07263	F9S42PC	MED, U8 (FAIRCHILD)	
6	4	4			27014	DS8833N	MED, U32,33,46,47 (NATIONAL)	
7	2	2				SN7400N	MED, U29,30	
8	1	1				SN74S02N	MED, U5	
9	11	11				SN74S04N	MED, U3,20,23,40,52,54,55,57,69,103,120	
10	1	1				SN74S05N	MED, U50	
11	2	2				SN74S08N	MED, U17,86	
12	1	1				SN7410N	MED, U10	
13	1	1				SN74S20N	MED, U49	
14	1	1				SN7421N	MED, U53	
15	1	1				SN7425N	MED, U51	

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1089724

REV M SHEET 6

OP—277 REV C

PARTS LIST

ITEM NO.	QTY PER ASSY G4	QTY PER ASSY G5	QTY PER ASSY G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
16	5	5				SN74S74N	MED. U14.15.18.19.25	
17	1	1				JKPT080-1330071	CRYSTAL OSCILLATOR 20.0 MHZ U7 (SEE NOTE 4) CTS KNIGHT	
18	2	2				SN74S139N	MED, U24,48	
19	11	11				SN74S153N	MED, U1,11,21,31,34,35,41,42,43,44,45	
20	5	5				SN74S157N	MED, U13,36,37,38,56	
21	2	2				SN74LS163N	MED, U26,27	
22	1	1				SN74LS164N	MED, U9	
23	3	3				SN74LS174N	MED, U2,12,22	
24	1	1			07263	UA7812UC	VOLTAGE REGULATOR +12 VDC, VR1 (FAIRCHILD)	
25	1	1			07263	UA79M05AHC	VOLTAGE REGULATOR -5 VDC, VR2 (FAIRCHILD)	
~~26~~	~~1~~	~~1~~				~~RNC55H3161FS~~	~~RES, MIL-R-55182/11, 3.16K, ±1%, .10W, R1~~	
~~27~~	~~1~~	~~1~~				~~RNC55H2151FS~~	~~RES, MIL-R-55182/11, 2.15K, ±1%, .10W, R2~~	
28	1	1				RCR07G223JS	RES, 22K OHMS, ±5%, .25W, R3	
29	1	1				RCR07G243JS	RES, 24K OHMS, ±5%, .25W, R4	
30	22	22				RCR07G200JS	RES, 20 OHMS, ±5%, .25W, R5,6,7,8,9,10, 11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26	
31	2	2				RCR07G360JS	RES, 36 OHMS, ±5%, .25W, R33,34	
32	1	1				RCR07G302JS	RES, 3K OHMS, ±5%, .25W, R27	
33	5	5				RCR07G512JS	RES, 5.1K OHMS, ±5%, .25W, R28,29,30,31,32	
34	2	2				RCR07G102JS	RES, 1K OHMS, ±5%, .25W, R35,36	
~~35~~	~~1~~	~~1~~				~~CM05ED240JP3~~	~~CAP, 24PF, ±5%, 500 WVDC, C1~~	
36	2	2				CK05BX102K	CAP, 1000PF, ±10%, 200 WVDC, C2,3	

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1089724

REV M | SHEET 7

PARTS LIST

ITEM NO.	QTY PER ASSY G4	QTY PER ASSY G5	QTY PER ASSY G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
37	9	9				M39003/01-2304	CAP, 6.8 UF, ±10%, 35 WVDC, C4,5,10,11, 12,13,14,15,16	
38	1	1				M39003/01-2347	CAP, .33 UF, ±10%, 50 WVDC, C6	
39	10	10				M39003/01-2356	CAP, 1.0 UF, ±10%, 50 WVDC, C7, 9, 17, 18, 19, 20, 21, 22, 23, 24	
40	1	1				M39003/01-2362	CAP, 2.2 UF, ±10%, 50 WVDC, C8	
41	62	—				CK05BX104K	CAP, 0.1 UF, ±10%, 50 WVDC, C25-C69, C82, C87-C94, C103-C110	
	—	94				CK05BX104K	CAP, 0.1 UF ±10%, 50 WVDC, C25, C77 C82, C87-C126	
42	4	4				7011935P1	INDUCTOR, L1,2,3,4	
43	1	1			31514	1008-692	SWITCH, S1 (SAE)	
44	1	1			13103	6073B	HEAT SINK, (THERMALLOY)	
45	1	1				1086608P18	CONN, ELEC, PC BOARD	
46	2	2				6010	EYELET	
47	2	2		A		600107P1	EJECTOR, CARD	≠
48	2	2		A		630003P14	EYELET, METALLIC	≠
49	1	1		A		640049P1	TRANSIPAD,	≠

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS ≠ INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1089724

REV N SHEET 8

PARTS LIST

ITEM NO.	QTY PER ASSY G4	QTY PER ASSY G5	QTY PER ASSY G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
50	1	1				MS51957-14	SCREW, MACH, PAN HD, .112-40 X .31 LG	
51	1	1				MS15795-803	WASHER, FLAT-METAL, .125 ID X .25 OD	
52	1	1				MS21083C04	NUT, SLFLKG, HEX, .112-40	
53	REF	REF		J		1089726	LOGIC DIAGRAM, 64K MEMORY	
54	6	6		A		165046P1	TEST POINT, TP1-TP6	≠
55	AR	AR		A		93002P1	SOLDER	
56	1	1				SN74LS74N	MED, U39	
57								
58	3	3				RCR07G331JS	RES, 330 OHMS, ±5%, .25W, R37,38,39	
59	AR	AR				270006P5	INSULATION TUBING, ELEC.	
60	AR	AR		A		278002P13	WIRE, ELEC, UNINSUL, 22 AWG	≠
61	REF	REF		A		815003	PW AND CKT BD, REQT FOR	
62	—	—			12881	MK4116P-3	MED, U61,62,63,64,65,66,67,68,70,71,72,73, 74,75,76,77,78,79,80,81,82,83,84,85,87, 88, 89,90,91,92,93,94 (MOSTEK)	
63	—	—			12881	MK4116P-3	MED, U61,62,63,64,65,66,67,68,70,71,72, 73,74,75,76,77,95,96,97,98,99,100,101, 102,104,105,106,107,108,109.110,111	
64	16	—			12881	MK4116P-3	MED, U61, 62, 63, 64, 66, 66, 67, 68, 70, 71, 72, 73, 74, 75, 76 77	
65	AR	AR				276000P26	WIRE, ELEC INSUL, 22 AWG	
64A	REF	—				UPD416C-2	MED, (NEC) (SEE NOTE 4)	
17A	REF	REF				MX040-20MHZ	CRYSTAL OSCILLATOR 20.0 MHZ (SEE NOTE 4) U7 CTS KNIGHT	

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS ≠ INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	PL
A	94117	1089724

REV M SHEET 9

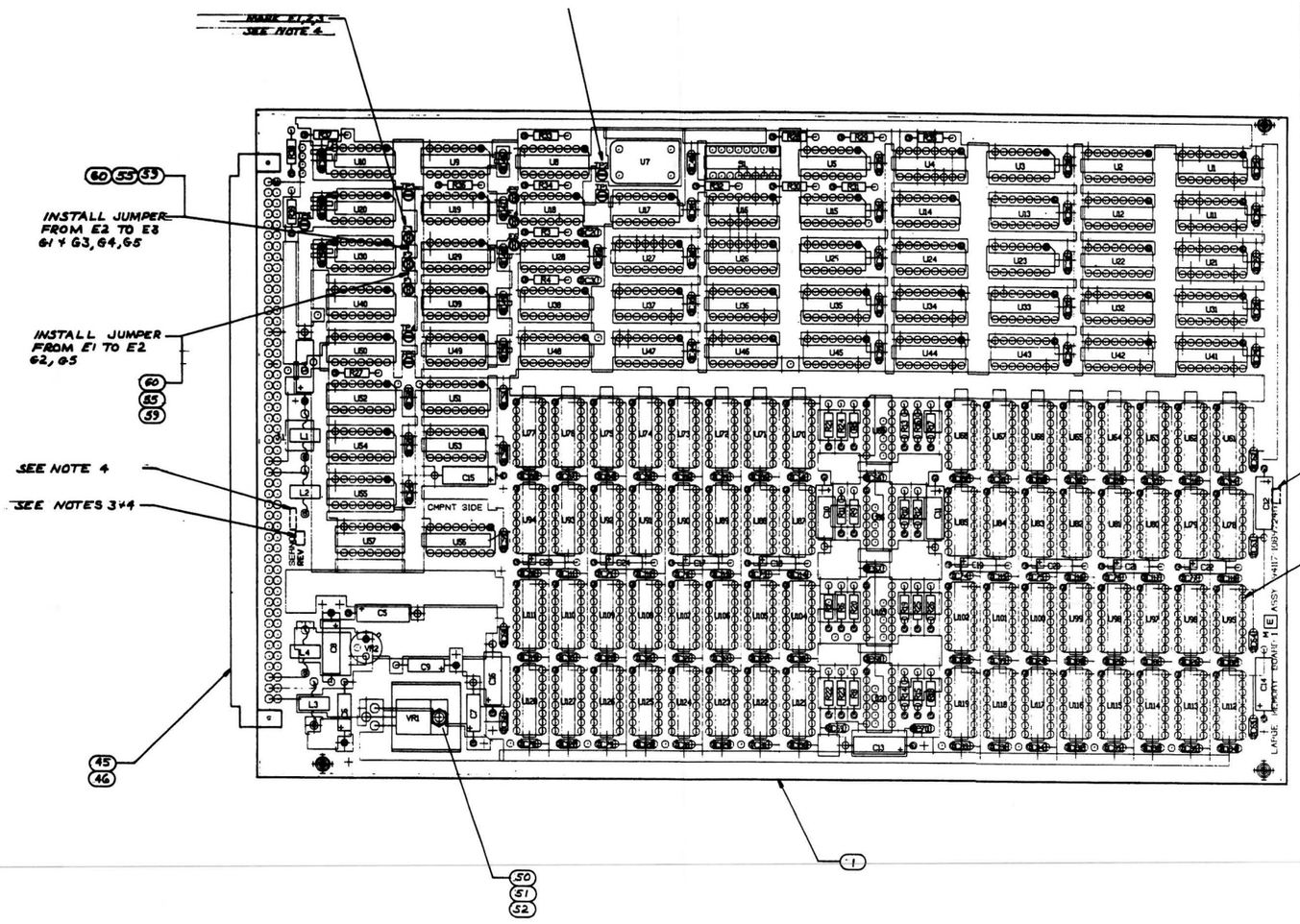
PARTS LIST

ITEM NO.	QTY PER ASSY G 5	QTY PER ASSY G	QTY PER ASSY G	DWG SIZE	CODE IDENT	PART OR IDENTIFYING NO.	DESCRIPTION	SYM
66	48	—	—		12881	MK4116P-3	MED U61-68, 70-85, 87-102, 104-111	
66A	REF	—	—			UPD 416C-2	MED, (NEC) (SEE NOTE 4)	

SHEET ONE REVISION LETTER IS THE IDENTIFYING REVISION FOR THIS MULTISHEET DWG
SEE SHEET ONE FOR REVISION DESCRIPTIONS
SYMBOLS : INDICATES VENDOR ITEM - SEE SPEC/SOURCE CONTROL DWG.

SIZE	CODE IDENT NO.	
A	94117	PL 1089724

REV L | SHEET 10



CUT		JUMPER		
FROM	TO	FROM	TO	USING ITEM
U15-11	U15-3	U15-3	U57-5	65
		U57-6	U15-11	65

SWITCH / JUMPER TABLE

MEMORY CONFIGURATION	NO OF BOARDS	BOARD NO.2 S1 SWITCH POS'N.	JUMPER BOARD 1	JUMPER BOARD 2
16K	1	N/A	E2-E1	N/A
32K	1	N/A	E2-E1	N/A
32K (HUGHES) + 48K	1	N/A	E3-E2	N/A
64K	1	N/A	E3-E2	N/A
80K	2	S1-1 THRU S1-5 OFF	E3-E2	E3-E2
96K	2	S1-1 THRU S1-5 OFF	E3-E2	E3-E2

9. NORMAL CONFIGURATION JUMPER E4-E5.
8. MARK APPROPRIATE SERIAL REV & CONDITION AT ASSY.
7. SOLDER TIPS OR WIRE TO BE .05 MAX FROM BOARD
6. MAX COMPONENT HEIGHT TO BE .44
5. OTHER THAN SPECIFICALLY NOTED, CHARACTERS ARE REFERENCE AND NOT TO BE MARKED.
4. MARK CHARACTERS .04-.16 HIGH, IN ACCORDANCE WITH MIL-STD-130.

G5 G4 G3 G2 G1 **FOR PARTS LIST** SEE PL 7089724

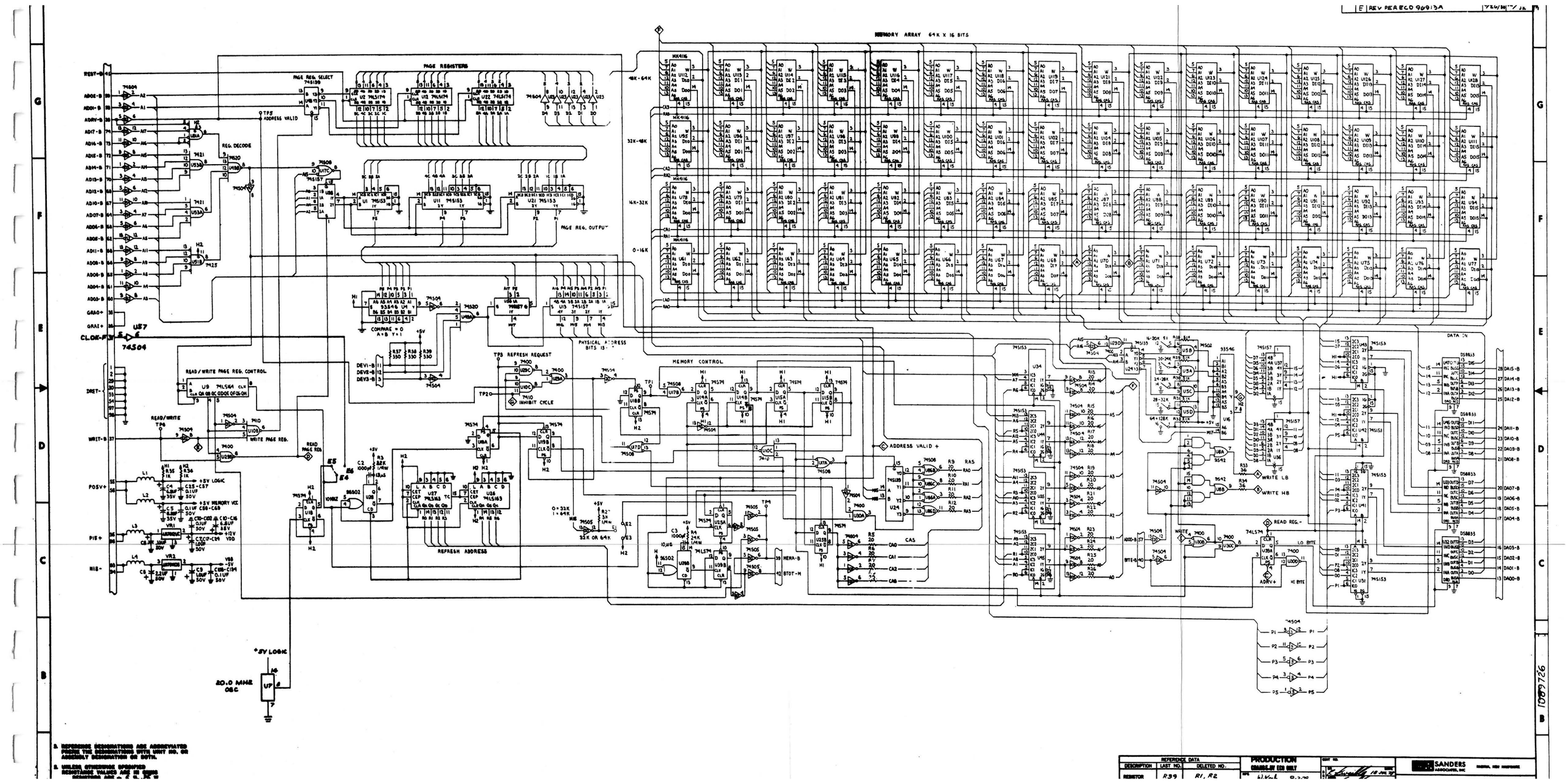
G5	G4	G3	G2	G1	ITEM	SIZE	PART OR IDENTIFYING NO.	DESCRIPTION
QTY PER ASSY								PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES

CONT NO.

SANDERS ASSOCIATES, INC. NASHUA, NEW HAMPSHIRE

1089724 B



1. REFERENCE DESIGNATIONS ARE ABBREVIATED WHERE THE DESIGNATIONS WITH UNIT NO. OR ASSEMBLY DESIGNATION ON BOTH.
2. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS

REFERENCE DATA			PRODUCTION
DESCRIPTION	LAST NO.	DELETED NO.	STANDARD ECO ONLY
RESISTOR	R39	R1, R2	

SANDERS ASSOCIATES, INC

F REV PER ECO 96913A

9216801 B

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firmware ☐ manual ☐

Description of problem (or suggestion for improvement):

Related tech manual number _____