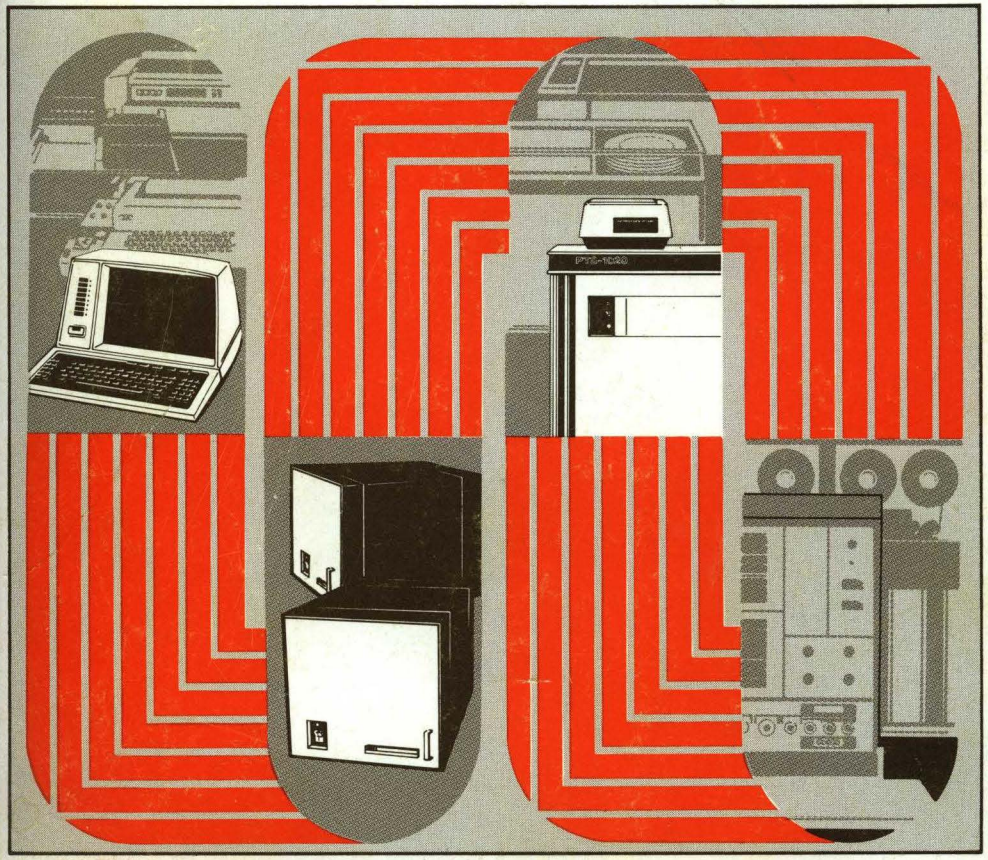
RAYTHEON

MAINTENANCE MANUAL

PTS-100

RAYTHEON DATA SYSTEMS



RAYTHEON

MAINTENANCE MANUAL

PTS-100

44-7650

PROGRAMMABLE TERMINAL SYSTEM
PTS-100
MAINTENANCE MANUAL

For
RAYTHEON ENGINEERS

Revised
October 1978

PREPARED BY

RAYTHEON DATA SYSTEMS
1415 BOSTON-PROVIDENCE TURNPIKE
NORWOOD, MASSACHUSETTS 02062

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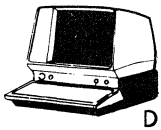
1001
STANDALONE
AGENT SET



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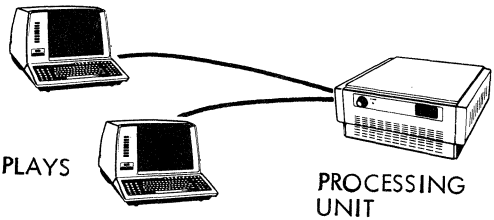
AGENT SET
QUAD



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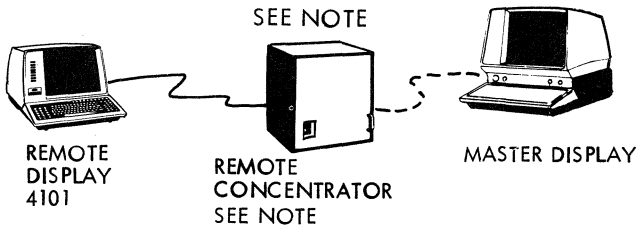
STANDALONE
SYSTEM



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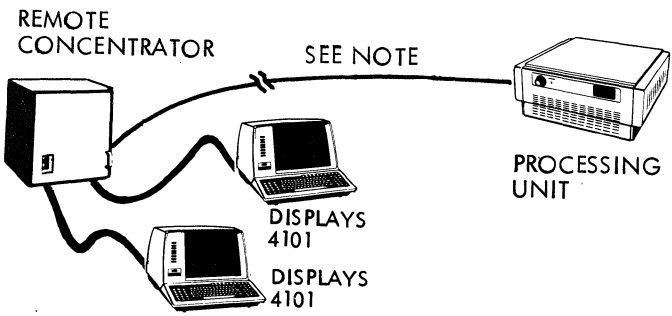
SYSTEM



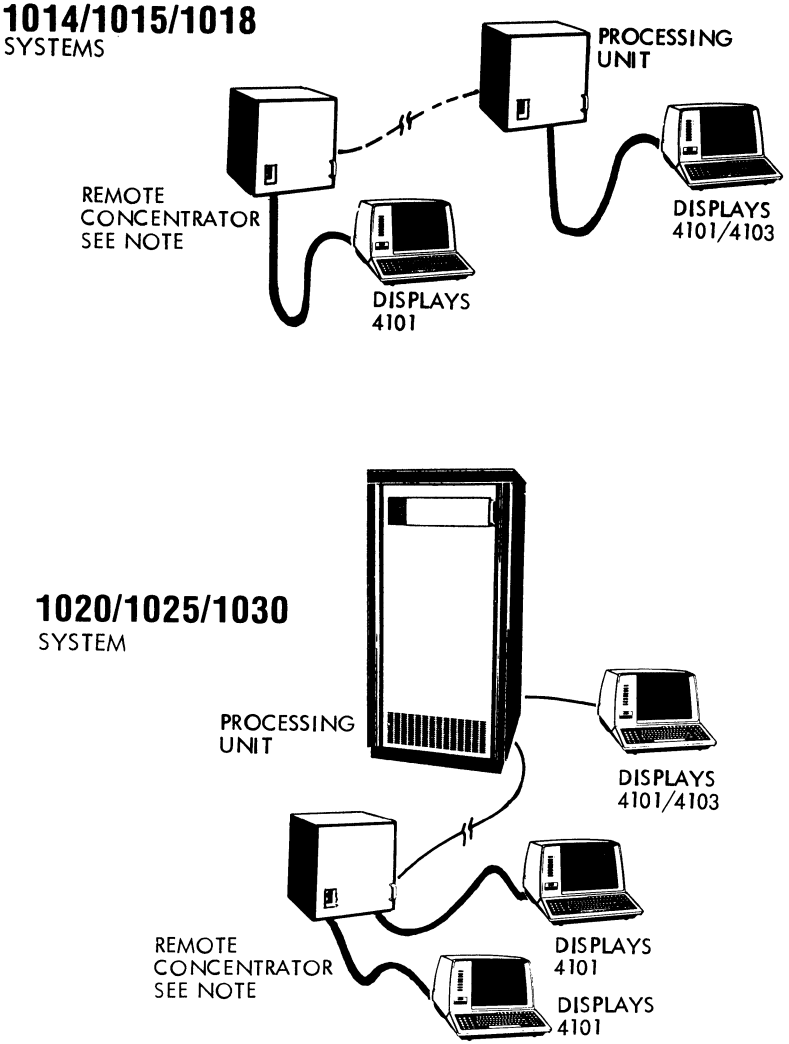


Figure 1-1 PTS-100 System Configurations

CHAPTER 1. GENERAL SYSTEM DESCRIPTION

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1.1 Introduction

The Raytheon Programmable Terminal System 100 (PTS-100) is a modularized programmable data display terminal system designed for alphanumeric data display applications. It can operate with various central processing systems, including IBM 360/370 systems. It is easily integrated into existing systems and can be tailored to suit individual data display system requirements. The PTS-100 system is expandable and can accommodate from 1 to 96 data display terminals.

There are twelve models of six basic PTS-100 system configurations (Figure 1-1). The models differ mainly in number of display terminals and number of peripheral I/O devices accommodated. The maximum number of displays and I/O devices that can be attached to each of the PTS-100 models is:

PTS-100 Model	No. Local Displays	No. Remote Displays	No. Low Speed Half Duplex I/O Device Channels	No. High Speed I/O Device Channels	Max Memory Size
1001	1	-	3	-	28K**
1001A	-	4	3	-	28K*
1005	1	1	6	1	16K
1008	-	32	3	-	64K
1014	1	1	12	3	32K
1015	4	32	12	3	32K
1015-1	4	32	12	3	32K
1015M	4	32	12	3	32K
1018	4	128	12	3	128K
1020†	8*	192	23	10	65K
1025	8*	128	15	10	128K
1030†	8*	224	15	10	128K

The low speed channels accommodate peripheral I/O devices that are used to load and assemble programs, connect the PTS-100 to other systems output error messages, etc. These devices operate at 9600 bits per second (bps) or less. The high speed channels accommodate devices that operate up to 1 Mbps. These devices are interfaces to other system disc and tape memories, customer engineer console, etc. The actual number of high and low speed channels that can be used depends upon the particular system configuration since these channels share board slots in the processing unit with other system components. Refer to Section 1-6 for the PTS-100 configuration.

1.2 System Hardware Features

The major components of the PTS-100 system are: processor, memory, high and low speed peripherals, display terminals, keyboards, and associated interfaces. The important features of these components are listed in Table 1-1.

*Actual number determined by 5 volt power supply loading, which depends on the number of memory boards and I/O controller boards installed.

**Plus 9K Display/Printer Ram Buffer.

† Interim models 1020M and 1030M are the same as 1020 and 1030 except they use DAM boards.

Table 1-1. Equipment Feature

Processor

- 16-bit word length (two 8-bit bytes)
- single and double word instructions
- 4 program addressable registers
- 29 executable instructions
- automatic priority interrupt with 8 external and 3 internal interrupts
- DMA transfer rate of 1 Mbps
- optional remote program load
- optional watchdog timer
- instruction execution time: 1.6 to 4.0 μs
- DMA request time: 1.76 to 4.32 μs
- DMA service time: 0.64 to 2.88 μs
- enter interrupt time: 4.8 μs
- exit interrupt time: 4.0 μs

Memory

- type: MOS RAM consisting of: 4K, 8K, 16K, 32K, and 65K byte modules
- 16-bit word (two 8-bit bytes)
- expandable to 131,072 bytes
- word and byte addressing
- 2-port
- refresh time: 64.1 μs
- read time: 0.8 μs
- write time: 1.28 μs
- three servicing priorities: 1. memory refresh, 2. display data refresh, and 3. processor requests.

Display Terminal

- 15 inch screen
- P31 phosphor
- two alphanumeric and symbol character sets:
  64 characters (upper case)
  96 characters (upper and lower case)
- number of characters displayed: 480, 960, 1024, or 1920

Table 1-1. Equipment Features (cont)

- seven character/line formats:

  12 lines of 40 characters each
  12 lines of 80 characters each
  24 lines of 40 characters each
  24 lines of 80 characters each
  15 lines of 64 characters each
  16 lines of 64 characters each
  30 lines of 64 characters each

- character generation dot matrix:

  64 character set - 7 x 7 dots enhanced, equivalent to 13 x 7 dots

  96 character set - 7 x 9 dots enhanced, equivalent to 13 x 9 dots

- data refresh rate: 60 Hz
- optional 8 programmable status indicators
- up to 192 display terminals (480 character) can be attached to the PTS-100

Keyboards

- eight basic keyboards: 67, 69, 75, 81, 82, 87, 89, and 91 key
- all keys programmable except REPEAT, SHIFT
- n-key rollover prevents simultaneous key depression from causing keyboard lockout
- detachable, permits remoting from the display.

Peripheral Equipment

Low speed I/O devices:

- speed to 9600 bps
- half/full duplex channels
- expandable to 28 half-duplex devices
- devices: (for model numbers see Chapter 2)
  - ASR/KSR/RO teletype
  - serial printers
  - card reader, 300/1000 cards/minute
  - cassette tape drive 10 ips, 360K byte capacity
  - asynchronous and synchronous modem interfaces
  - paper tape reader/punch
  - ticket printer
  - boarding pass printer
  - line printer
  - matrix printer

Table 1-1. Equipment Features (cont)

High Speed I/O devices:

- optional asynchronous data processor
- speed to 1 Mbps
- 16-bit I/O bus
- direct memory access
- expandable from 3 to 10 channels
- 80 Mb disc
- channel interface controller (CIC)
- magnetic tape

1.3 Hardware Description

The PTS-100 system hardware configurations are shown in Figure 1-2. Each block in the diagrams is a standard plug-in board or assembly that is interchangeable in the different PTS-100 models. The configurations shown are composites; some of the features are not found in all systems. The PTS-100 systems are made up of three major hardware assemblies and various optional I/O devices and associated interfaces. The three basic assemblies are:

- Processing Unit
- Remote Concentrator
- Display/Keyboard Terminals

1.3.1 Processing Unit

The processing unit contains the processor, memory, I/O device and display/keyboard interfaces, and a power supply. The processor is a general purpose 16-bit machine that controls the PTS-100 system. Except for Model 1001/A the processor is contained on one plug-in-board, with various fixed and switch selectable options mounted on an associated feature board or, in the case of the Model 1005 and 1014 on the combined DA/MC/FB. On the 1001/A all of the electronics and memory are mounted on a single plug-in pc board. The memory is either on separate boards or combined with the circuits on the display adapter boards (DAM). The memory stores system programs and data for the displays. It has two ports to allow access by both the processor and the display adapter(s). The memory is expandable from 8K bytes to 131K bytes by plugging in additional up to 65K byte memory or DAM boards.

The data stored in this type of memory must be refreshed periodically or it will be lost. This function is performed either on the DAMs or by the display adapters, which also multiplex the data received from the keyboards and send refresh data to the displays. When DAMs are not used, one display adapter is required for every two 4K or 8K memory modules or for every 16K memory module.

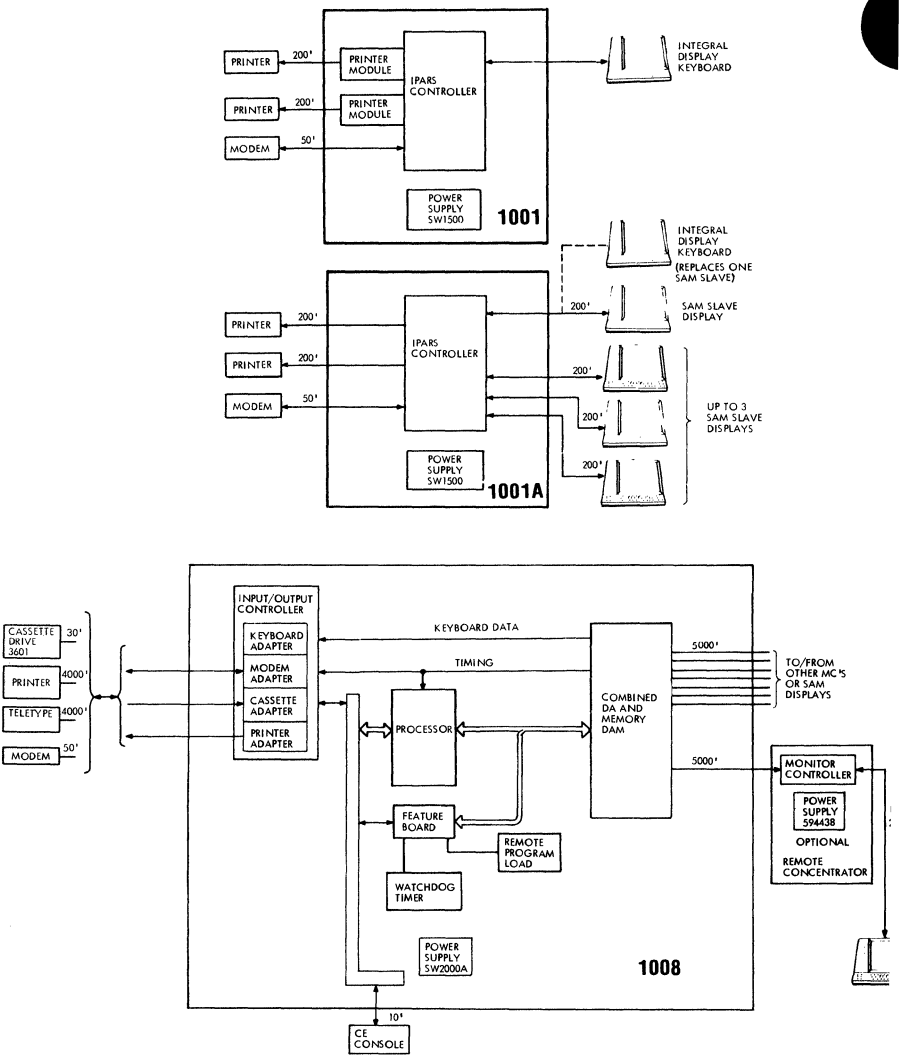
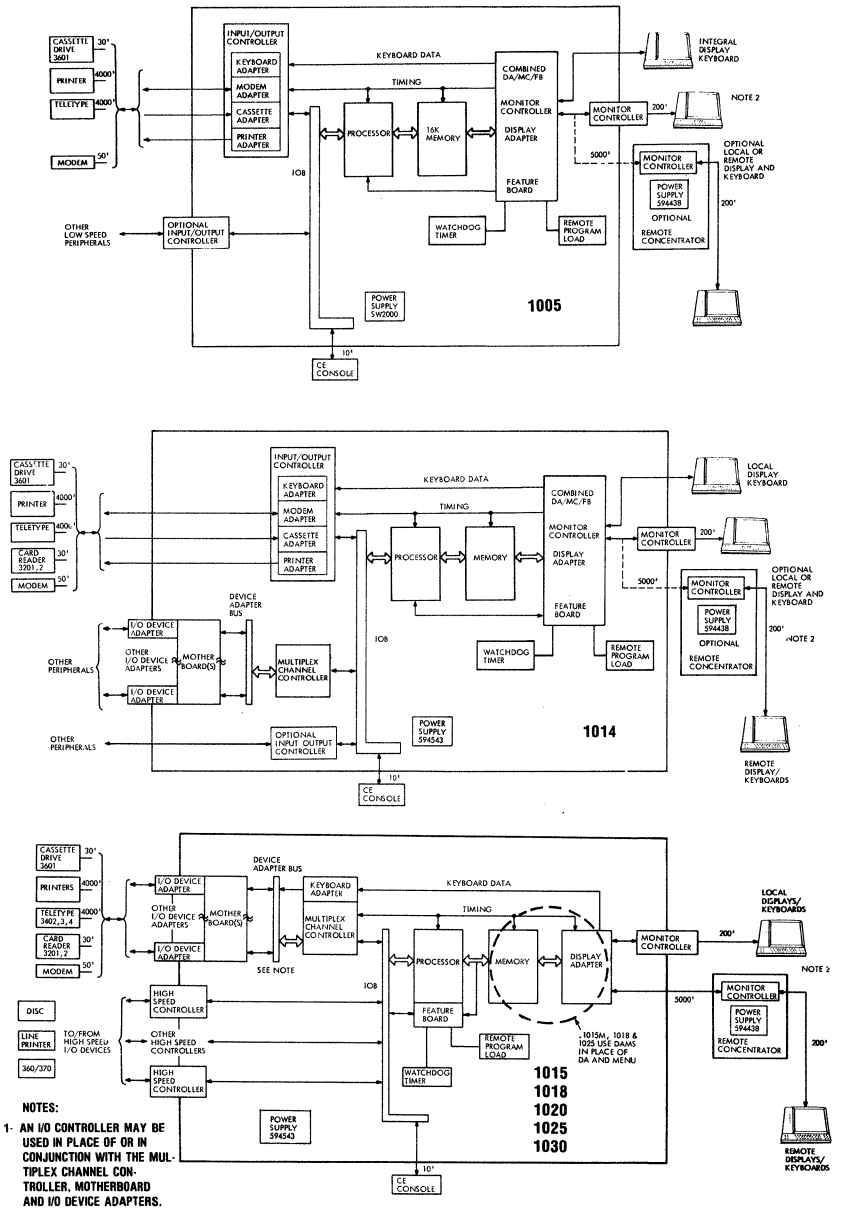


Figure 1-2. PTS-100 Block Diagram (Sheet 1)



NOTES:

1- **AN I/O CONTROLLER MAY BE USED IN PLACE OF OR IN CONJUNCTION WITH THE MULTIPLEX CHANNEL CONTROLLER, MOTHERBOARD AND I/O DEVICE ADAPTERS.**

2- **A SAM DISPLAY CAN BE USED IN PLACE OF A STANDARD DISPLAY AND MONITOR CONTROLLER.**

Figure 1-2. PTS-100 Block Diagram (Sheet 2)

The data to and from the displays/keyboards is processed by monitor controllers that decode the character codes from the memory and provide character generation, power, and sweep signals to the attached display(s). Generally, two 1920 character displays, four 480, or two 960 or 1024 character displays and keyboards can be attached to each monitor controller. The monitor controllers are installed in either the processing unit or the remote concentrator(s), depending upon whether the displays/keyboards are located within 200 feet of the processing unit or located more remotely from it. PTS-100 Models 1005 and 1014 use a combined display adapter/monitor controller/feature board that performs the same functions as the display adapter, monitor controller and feature board except that it accommodates fewer display/keyboard terminals. PTS-100 Models 1008, 1015M, 1018, and 1025 use combined display adapter/memories (DAMs) that perform the same functions as the display adapter and memory boards.

Data from all the keyboards is multiplexed and serialized in the display adapter(s) and applied to a keyboard adapter in the multiplex channel controller or in the input/output controller (IOC). The low speed (9600 bps) peripheral devices also attach to these controllers (for the multiplex channel controller - via I/O device adapters, one for each I/O device attached and motherboards which hold the adapters). The multiplex channel controller and IOC interface the processor over the processor direct memory access I/O bus (IOB) and control the data transfer operations to and from the I/O devices and from the keyboard, under program initiation. Optional high speed controllers (1 Mbps maximum) are used to connect high speed I/O devices to the PTS-100 system. They connect directly to the IOB.

1.3.2 Remote Concentrator

There are two remote concentrator models, 4301 and 4302. The remote concentrators house the monitor controller boards and power supplies that drive the remote displays. The monitor controllers are the same as those used in the processing unit. The Model 4301 remote concentrator can accommodate up to eight monitor controller boards, which could drive sixteen 480, 960, or 1024 character, or fourteen 1920 character, display terminals. The number of monitor controllers permitted depends on the PTS-100 model. The model 4301 remote concentrator uses the same type of cabinet as the 1015 processing unit. The model 4302 remote concentrator has only one monitor controller which can drive any two display terminals.

1.3.3 Display/Keyboard Terminals

The keyboards are used to enter information into the processing unit memory, and the associated displays display the data stored at these memory locations. The data to the displays is refreshed 60 times per second. Each display is capable of displaying 1920, 1024, 960, or 480 characters on 12, 15, 16, 24, or 30 lines. The number of characters, number of lines, character

font, etc., are determined by the monitor controllers, which provide power and sweep voltages to the displays and interface the displays with the display adapters in the processing unit. There are two types of displays: SAM and standard. The SAM displays have integral monitor controller circuits. The standard displays have separate monitor controllers. The only other circuits in the displays are the high voltage CRT power supplies, video amplifiers, and an optional eight status indicator assembly, which displays system status information.

1.4 Physical Characteristics and Power Requirements

PTS-100 physical characteristics and power requirements are listed in Chapter 2.

1.5 Equipment Configuration

Most PTS-100 configurations use the same plug-in component boards and accommodate the same type of peripheral equipment. They differ mainly in size and I/O device handling capability. The PTS-100 equipment configurations are shown in Figure 1-3. The reference designations correspond to the board locations in the cabinets. Some of the locations are used for several different types of boards, depending upon the PTS-100 configuration. Refer to Chapter 3 for pictures of the boards. Some of the high speed controllers mount in separate card cages, which are not shown. Refer to the controller description in Chapter 3 for these. Also not shown are the board compliment and board locations in the displays. Refer to Chapter 3, Section 3 for these.

1.6 PTS Model Feature Code Description

1.6.1 PTS-100 Processor Model Feature Code Configurations

A. M/FC Format

Model	Mode	Emulator	-	Memory Size KB
1005	R-Remote	1 = 2260		16 (Kilobytes)
1008	L-Local	2 = 3270		32
1014		3 = IPARS		40
1015		4 = SITA		48
1018		5 = ALPHA		96
1020		7 = U100		128
1025		12 = SDLC		
1030		22 = SDLC/3270		

B. Examples No. 1 1014 R3-32 No. 2 1030 L2-128

Model	Mode	Emulator		Memory Size
1014	R	3	-	32

Model - 1014 Processor
Mode - Remote
Emulator - IPARS
Memory Size - 32KB of Memory

Model	Mode	Emulator		Memory Size
1030	L	2	-	128

Model - 1030 Processor
Mode - Local
Emulator - 3270
Memory Size - 128KB of Memory

C.

Model	Description
1001	Single Display Fixed Memory (1001 Processor does not require Mode, Emulator, or Memory Size M/FC)
1001 Q-1	(No. of Displays) Fixed Memory
-2	" " "
-3	" " "
-4	" " "

1.6.2 PTS/1200 Processor Hardware Model Feature Code Configurations

A. M/FC Format

Model	Memory Size		Disc Storage
1200	48	A	2.5 mb (Megabytes)
	64	B	5.0 mb
	80	C	7.5 mb
	96	D	10.0 mb 1 Diablo 31/33 Disc Drives=2.5 mb
	112	E	12.5 mb
	128	F	15.0 mb
		G	17.5 mb
		H	20.0 mb
		I	10.0 mb
		J	20.0 mb 1 Diablo 44B Disc Drives=10.0 mb
		K	30.0 mb
		L	40.0 mb
		M	80.0 mb 1 CDC Storage Module=80.0 mb

B. Examples No. 1 1200-641 No. 2 1200 = 128D

Model		Memory	Disc Storage
1200	-	64	1

Model - 1200 Processor
Memory - 64KB of Memory
Disc Storage - 10.0 mb (1 Diablo 44B Disc Drive)

Model		Memory	Disc Storage
1200	-	128	D

Model - 1200 Processor
Memory - 128KB of Memory
Disc Storage - 10.0 mb (4 Diablo 33/31 Disc Drive)

PTS/1200 MARK I, MARK II, Processor Hardware Model Feature Codes

C. M/FC Format

Model	-	Memory Size	Disc Storage
MKI		64	1-10 mb
MKI		128	1-10 mb
MKII		64	1-10 mb (Note 1)
MKII		128	1-10 mb
MKII		64	M-80 mb (Note 1)
MKII		128	M-80 mb

D. Examples

No. 1 MKI-64

Model	-	Memory	Disc Storage
MKI		64	1

Model - MKI Processor
Memory - 64KB of Memory
Disc Storage - 10.0 mb (1 Diablo 44B Disc Drive)

No. 2 MKII-128M

Model	-	Memory	Disc Storage
MKII		128	M

Model - MKII Processor
Memory - 128KB of Memory
Disc Storage - 80 mb (1 CDC Storage Module)

NOTE 1

More than one drive is permitted on a MKII system, therefore the following M/FC's define disc expansion.

M/FC	Description
3810-02	2nd 10.0 mb Diablo 44B Disc Drive
3810-03	3rd " " " " " "
3810-04	4th " " " " " "
3820-02	2nd 80.0 mb CDC Storage Module
3820-03	3rd " " " " " "

1.6.3 Display Drive Model Feature Code Configurations

A. M/FC Format

4	Type of Drive	Type of Cables*	Screen Format	-	No. of Displays Driven
4-Direct	Direct Drive			1 - 480	01
3-Remote	1 - Twisted Pair			2 - 960	.
	3 - Coaxial RG-62U			3 -1920	. up to 16
	* 5 - Used only wity U-100 Application for Protected Field Display Option				
	Remote Concentrators				. 16
	1 - R. C. Twisted Pair				
	2 - L. P. R. C. Twisted Pair				
	3 - R. C. Coaxial				
	4 - L. P. R. C. Coaxial				
	* 5 - Used only with U-100 Application for Protected Field Display				

NOTE

L. P. R. C. - Low Profile Remote Concentrator, R. C. - Large Remote Concentrator

B. Model Feature Code Examples

1. Model 4413 - 08

   — Direct Drive
   — Twisted Pair Cable
   — 1920 Character Screen Format
   — Capable of Driving 8 Displays

2. Model 4332 - 16

   — Remote Concentrator Drive
   — Coaxial Cables
   — 960 Character Screen Format
   — Capable of Driving 16 Displays

3. Model 4323 - 02

   — Low Profile R. C. Drive
   — Twisted Pair Cables
   — 1920 Character Screen Format
   — Capable of Driving 2 Displays

4. Model 4451 - 04

   — Direct Drive
   — Protected Field Option
   — 480 Character Screen Format
   — Capable of Driving 4 Displays

Display Model Feature Codes

A.

M/FC		Description
4101	Display Monitor	Interfaces to Remote Concentrator and/or Low Profile Remote Concentrator via Coax or Twisted Pair Cables

M/FC		Description
4103 - XX	Stand Alone Monitor	SAM interfaces directly to Processor via Twisted Pair or Coaxial Cables.
12 - 3270	Emulator, 960 Screen Format	
13 - "	Emulator, 1920 Screen Format	
14 IPARS	Emulator, 960 Screen Format	
15 - IPARS	Emulator, 1920 Screen Format	
4104	Stand Alone Monitor (slave)	Interfaces to a 4103 SAM Master via Coaxial Cable. Supports only 960 (80 x 12) character formats.

1.6.4 Peripheral Model Feature Code Configurations

A. Printers

M/FC	Description	
3301	Data Products 2230	300 lpm
3306	Data Products 2260	600 lpm
3401	GE TermiNet 300	30 cps
3405	Extel 15	15 cps
3406-01	Centronics 306	120 cps
3406-02	Centronics 306C	100/165 cps
3407	Extel 30	30 cps
3408	Hyterm/Diablo	45 cps
3411	GE TermiNet 1200	120 cps
3412	Centronics 101A	165 cps
3472	Centronics 702	120 cps
3414	GE TermiNet 30 (Ticket/Serial)	
3421	DiAn Ticket Printer	
3422-01	Vogue Ticket Printer	
3423	DiAn Boarding Pass Printer	
3424	Vogue Boarding Pass Printer	
3430	Raytheon Boarding Pass Printer	
3440	Raytheon Ticker Printer (Tugboat)	

B. Disc Equipment

M/FC	Description
3800	Diablo Series 30
3810	Diablo 44B
3820	CDC Storage Module

C. Mag Tape Equipment

M/FC	Description
3900	800 bpi, Drive and Controller
3901	800 bpi, Drive
3910-1	1600 bpi, Drive and Controller
3910-2	1600 bpi, Drive

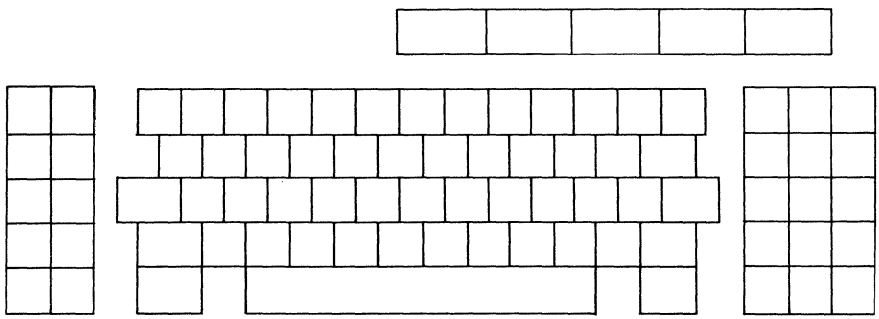
D. Special Peripheral

M/FC	Description
6140-01	Badge Reader
6150-01	Magnetic Card Reader
LC-50	Documation Card Reader/Punch
HFR-1	Documation Hand Feed Card Reader
3201	Documation Card Reader 300 cpm

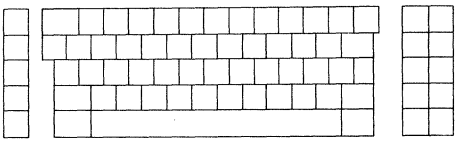
1.6.5 Keyboard Model Feature Codes

M/FC	Description
6102-XX (Note 2)	82 Key
6103-XX	69 Key
6104-XX	81 Key
6105-XX	89 Key
6106-XX	91 Key
6107	75 Key
6108	87 Key

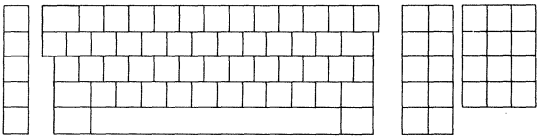
XX defines the customer's options, such as special key functions, LED panel, unique key cap configurations, etc. For purposes of the asset control inventory, these options are not required.



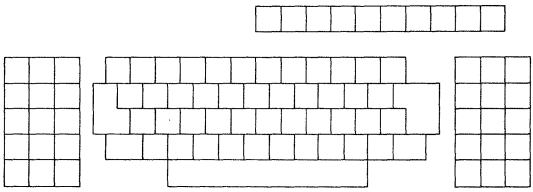
Model 6102, 82 Key



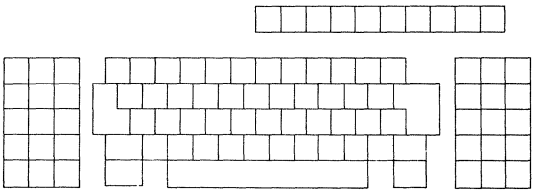
Model 6103, 69 Key



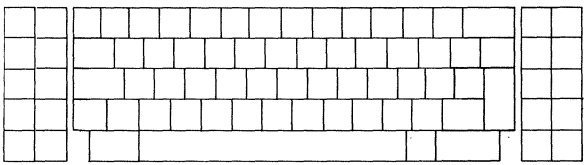
Model 6104, 81 Key



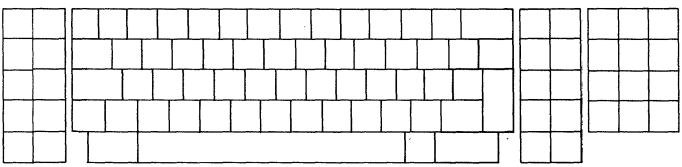
Model 6105, 89 Key



Model 6106, 91 Key



Model 6107, 75 Key



Model 6108, 87 Key

1.7 Major Component Descriptions

1.7.1 Processor

The processor is a general purpose 16-bit minicomputer with 29 single and double word instructions and six byte and word addressing modes. It has an eight level external hardware priority interrupt system and an interval timer. The same processor is used in all PTS-100 models except the 1001/A (the processor is part of the IPARS controller).

1.7.2 Feature Board

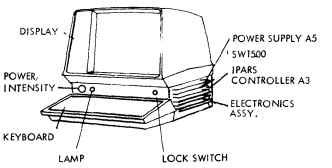
The feature board contains various fixed and switch selectable options and features for the processor. It includes an alternate program load device address switch, 64 miniature chip switches for configuration control, a standard interval timer, a standard initial program load (IPL), an optional watchdog timer 2421 (WDT), and an optional remote program load 2420 (RPL). On the 1005 and 1014 the feature board circuits are on the DA/MC/FB. On the 1001(A) these circuits are on the IPARS controller.

1.7.3 Memory

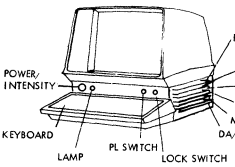
The memory stores the system programs and the data for the displays. It employs random access semiconductor MOS devices and is expandable from 8,192 to 131,072 bytes in increments of 8,192, 16,384, 32,768, and 65,536 bytes. It is organized in 16-bit words (2 bytes per word) and has an average cycle time of 1 microsecond. The memory modules are dual ported, permitting access by both the processor and the display adapters. There are two standard types of memory boards, 8K and 16K, which cannot be mixed in a system because they use different power supply voltages, and there are three types of DAMs, 16K, 32K, and 64K which can be mixed. The memory on the 1001/A is part of the IPARS controller.

1.7.4 Multiplex Channel Controller

Up to three multiplex channel controllers can be attached to the processor (1020) I/O bus. They interface low speed peripherals that operate at rates up to 9600 bits per second. The interface is actually made through I/O device adapters that plug into motherboards connected to the multiplex controller channels. The multiplex channels automatically execute control operations for the I/O devices under program initiation. Block transfer of data between memory and the I/O devices is handled by these channels, including code translation and code recognition without program intervention. The multiplex channel controllers can each handle up to eight half duplex I/O devices. However, in this case one multiplex controller subchannel is reserved for data from the display terminal keyboards. This subchannel is interfaced by a keyboard adapter, which is part of the first multiplex channel controller.



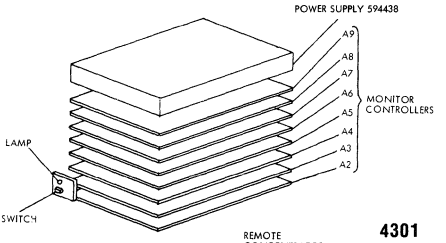
1001/1001A



1008
POWER SUPPLY A6
SW 2000A
PROCESSOR A5
FEATUREBOARD B
A3 A4
DAM A2
IO/CONTROLLER A1

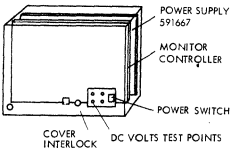
NOTE: 1008 HAS NO LOCAL DISPLAY

1005/1008



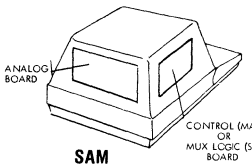
REMOTE CONCENTRATOR MODEL 4301

4301

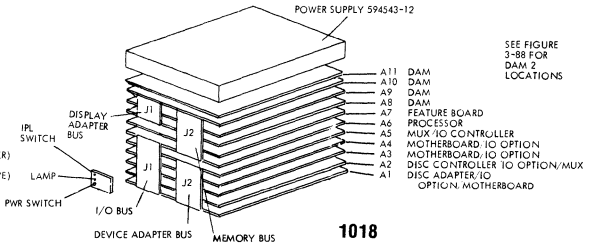


LOW PROFILE REMOTE CONCENTRATOR MODEL 4302

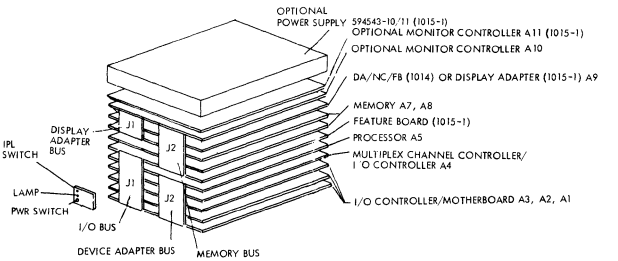
4302



SAM

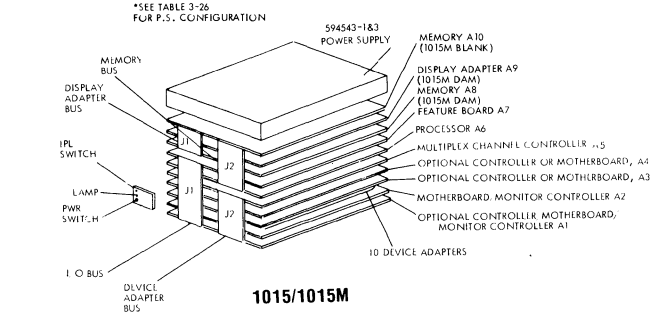


1018

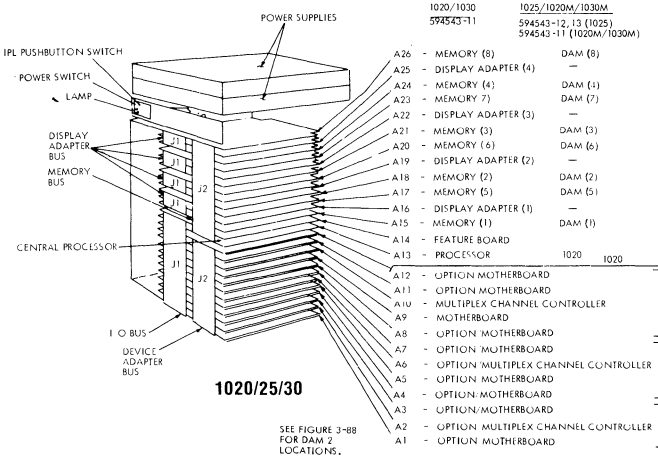


MODELS 1014 & 1015-1

1014/1015-1



1015/1015M



1020/25/30

	1020/1030 594543-11	1025/1020M/1030M 594543-12,13 (1025) 594543-11 (1020M/1030M)
A26 -	MEMORY (8)	DAM (8)
A25 -	DISPLAY ADAPTER (4)	—
A24 -	MEMORY (4)	DAM (4)
A23 -	MEMORY 7)	DAM (7)
A22 -	DISPLAY ADAPTER (3)	—
A21 -	MEMORY (3)	DAM (3)
A20 -	MEMORY (6)	DAM (6)
A19 -	DISPLAY ADAPTER (2)	—
A18 -	MEMORY (2)	DAM (2)
A17 -	MEMORY (5)	DAM (5)
A16 -	DISPLAY ADAPTER (1)	—
A15 -	MEMORY (1)	DAM (1)
A14 -	FEATURE BOARD	
A13 -	PROCESSOR	

SEE NOTE BELOW FOR 1020M/1030M BOARD LOCATIONS.

SEE FIGURE 3-88 FOR DAM 2 LOCATIONS

	1020	1025/30/20M/30M	
A12 -	OPTION MOTHERBOARD	- OPTION MOTHERBOARD	
A11 -	OPTION MOTHERBOARD	- OPTION MOTHERBOARD	
A10 -	MULTIPLEX CHANNEL CONTROLLER	- MULTIPLEXER CHANNEL CONTROLLER	1
A9 -	MOTHERBOARD	- MOTHERBOARD	
A8 -	OPTION MOTHERBOARD	- OPTION ADAPTER/MOTHERBOARD/DISC	
A7 -	OPTION MOTHERBOARD	- OPTION/ADAPTER/MOTHERBOARD/DISC	
A6 -	OPTION MULTIPLEX CHANNEL CONTROLLER	- OPTION MULTIPLEXER CHANNEL CONTROLL	2
A5 -	OPTION MOTHERBOARD	- OPTION MOTHERBOARD	
A4 -	OPTION MOTHERBOARD	- OPTION MOTHERBOARD	
A3 -	OPTION MOTHERBOARD	- OPTION	
A2 -	OPTION MULTIPLEX CHANNEL CONTROLLER	- OPTION	3
A1 -	OPTION MOTHERBOARD	- OPTION	

SEE FIGURE 3-88 FOR DAM 2 LOCATIONS.

NOTE: FOR 1020 : MONITOR CONTROLLERS ARE INSTALLED IN SLOTS A2, A3, A4 & A5 WHEN ONLY 2 MULTIPLEX CONTROLLERS ARE USED. MONITOR CONTROLLERS COULD BE INSTALLED IN A7, A8 & A9 WHEN 3 MULTIPLEX CONTROLLERS ARE USED. BRACKETS (1,2,3) SHOW BOARD SLOTS WITH SEPARATE J2 BUSES.

NOTE: 1020 HAS NO LOCAL DISPLAY, CAPABILITY, FOR 1025 M.C.S. CAN BE INSTALLED IN BOARD SLOTS A2,A3,A4&A5.

NOTE

LOCATION(X) OF 16K DAM BDS IN 1020M/1030M

	1020M 1 PS		1020M 2 PS		1030M 3 PS	1030M 4 PS
	64K	128K	64K	128K	128K	128K
A26	-	-	X	-	-	X
A25	-	-	-	-	-	-
A24	-	-	-	-	-	X
A23	-	-	X	-	X	X
A22	-	-	-	-	-	-
A21	-	-	-	X	X	X
A20	X	-	X	X	X	X
A19	-	-	-	-	-	-
A18	-	-	-	X	X	X
A17	X	X	X	X	X	X
A16	-	-	-	-	-	-
A15	-	X	-	X	X	X

Figure 1-3 Board Locations

The number of I/O devices that can be accommodated is a function of the physical adapter size and the desired operation (full duplex capability requires two multiplex channels; half duplex or simplex capability requires one channel). Peripherals may be attached in any combination.

1.7.5 I/O Device Adapters and Motherboards

One I/O device adapter is required for each low speed I/O device attached to the multiplex channel controller(s). The I/O device adapters are mounted either on the I/O device adapter motherboards or (in the case of the general purpose communication adapter) in place of a motherboard. The I/O device adapters come in three physical sizes: quarterboard, halfboard and board size. Four quarterboard and two halfboard (or combinations of) adapters can be mounted on one motherboard. The number of I/O device adapters that can be electrically accommodated by each PTS-100 model is limited by the number of multiplex controller subchannels available. Each subchannel can accommodate one half-duplex I/O device adapter. The physical size of each I/O device adapter (occupies 1/4 or 1/2 of the motherboard) and the number of multiplex controller subchannels required by each are shown in Table 1-2. The maximum number of motherboards permitted and the number of multiplex controller subchannels available (exclusive of the one used for the keyboard adapter) for each PTS-100 model are as follows:

PTS-100 Model	No. of Multiplex Channel Controller Subchannels Available	Maximum No. of Motherboards Permitted
1014	7	3
1015-1	7	3
1015	7	4
1020, 1025, 1030 (with 1 multiplex controller)	7	4
(with 2 multiplex controllers)	15	7
(with 3 multiplex controllers)	23	9

The total number of multiplex controller subchannels required for the I/O device adapters can never exceed the number of subchannels available. Also, the total number of motherboards required to mount the I/O device adapters can never exceed the total number of motherboards permitted.

1.7.6 Input/Output Controller

The Input/Output Controller (IOC) is a microprogrammed I/O controller that is used to interface the PTS-100 to five I/O devices: a magnetic tape cassette, a printer, a send and a receive modem, and the display keyboards. In applications where only these five I/O devices are used the IOC replaces

Table 1-2. I/O Device Adapter Mux Channel and M'board Requirements

I/O Device Adapter	Amount of M'Board Used by Adapters*	Mux Subchannels Required by Adapter
Card Reader Adapter	1/4	1
Line Printer, Parallel Adapter	1/4	1
Serial Printer Adapter:		
1. MISA	1/4	1
2. Serial Adapter	1/4	
Half duplex		1
Full duplex		2
Magnetic Tape Cassette Adapter (handles 1 to 4 drives)	1/2	1
Modem adapter 2331, 2K to 9.6K bps, 6 bits/char, sync modem sup. clk		
Half duplex	1/2	1
Full duplex	1/2	2
Modem adapter, CTMC, 2848 & 3270, 2K to 9.6K bps		
Half duplex	1/2	1
Full duplex	1/2	2
Modem adapter asynchronous, 2341 to 9.6K bps 5, 6, 7 or 8 bits/char, async adapter supplied clock		
Half duplex	1/2	1
Full duplex	1/2	2
General Purpose Communications adapter .GPCA (accommodates up to 4 half duplex or 2 full duplex 50-4800 baud modems)	1**	
Half duplex		1
Full duplex		2
Synchronous Data link communications SDLC Adapter		
Full duplex	1**	2

*Four 1/4 board or two 1/2 board I/O device adapters can be mounted on a single motherboard.

**Replaces motherboard.

the Multiplex Channel Controller, motherboard, and I/O device adapters. When additional I/O devices are employed the IOC can be used in conjunction with the Multiplex Channel Controller.

The IOC only requires one board slot. However, it is slower than the multiplex channel controller and its application is limited to the five devices listed above. In addition, when more than one IOC is installed most of the circuits on the second IOC are not used.

1.7.7 Display Adapter

The display adapters attach to the memory bus. They transmit serial display refresh data from memory to the displays. They also serialize the data received from the keyboards and control the refresh of the memory. Each display adapter is used to refresh the data in two 8K or one 16K memory module: therefore, one display adapter is required for every two 8K memory modules or one 16K memory module. All displays connected to a display adapter must use the same number of characters per line and the same number of lines per screen.

1.7.8 Display Adapter/Monitor Controller/Feature Board

The display adapter/monitor controller/feature board (DA/MC/FB) is a single circuit board that provides the combined display adapter, monitor controller, and feature board functions for models 1005 and 1014. The DA/MC/FB can accommodate one local display terminal, two keyboards, two LED status indicator panels, and the monitor controller for one remote display terminal.

1.7.9 Display Adapter-Memory

The DAM is a single board that provides the combined functions of a display adapter and its memory modules. The DAMs come in 16K, 32K, and 65K byte memory sizes.

1.7.10 Monitor Controller

The monitor controller (MC) provides character generation, power, and sweep signals for the CRT displays. Each monitor controller connects to a separate channel of the associated display adapter via a single twisted pair or coaxial cable. The monitor controllers handle up to 3840 characters of displayable information (3840 bytes of memory storage) which may be allocated to two 1920, four 960 (or 1024), or four 480 character display terminals. The standard monitor controller uses a 64 character upper case symbol set. Optional 96 and 128 character symbol set features

Table 1-3. Monitor Controller and Remote Concentrator Capacity

Monitor Controller (MC) Model	Screen Format	Max No. Displays/ MC	Max No. Keyboards/ MC	Max No. LEDs/ MC	Max No. MCs/Remote Concentrator
B Mod	1920 80/64 Ch	1	2	2	8
	960 80/64 Ch	2	2	2	8
	960 40 Ch	2	2	2	8
	480 40 Ch	4	4	4	4
B Mod 16th Line	1920 80/64 Ch	1	2	2	8
	1024 64 Ch	2	2	2	8
	960 80/64 Ch	2	2	2	8
	960 40 Ch	2	2	2	8
	480 40 Ch	4	4	4	4
C	1920 80/64 Ch	1	2	2	7
	960 80/64 Ch	2	2	2	7
	960 40 Ch	2	2	2	7
	480 40 Ch	4	4	4	4
D	1920 80 Ch	2	2	2	6
	960 80 Ch	4	4	4	4
	960 40 Ch	2	2	2	6
	480 40 Ch	4	4	4	4
F and K	1920 80/64 Ch	2	2	2	7 /6**
	1024 64 Ch	4	4	4	4
	960 80/64 Ch	4	4	4	4
	960 40 Ch	2	2	2	7 /6**
	480 40 Ch	4	4	4	4
DA/MC/FB	1920 80/64 Ch	1 /1*	2 /2*	2 /2*	-
	960 40/64/ 80 Ch	1 /1*	1 /1*	1 /1*	-
	480 40 Ch	1 /1*	1 /1*	1 /1*	

*DA/MC/FB Monitor Controller (See Figure 2-4 for cable connections), Local/Remote

**With/without Character Generator Module

Table 1-4. Monitor Controller Options

Option	Monitor Controller Model							
Screen Format	MC-B MOD	MC-B MOD-16	MC-C	MC-C1 MOD	MC-D	MC-D MOD	MC-F	MC-K
40 CH/LN 12 LN 480 CH	X	X	X	X	X	X	X	X
40 CH/LN 24 LN 960 CH	X	X	X	X	X	X	X	X
80 CH/LN 12 LN 960 CH	X	X	X	X	X	X	X	X
80 CH/LN 24 LN 1920 CH	X	X	X	X	X	X	X	X
64 CH/LN 15 LN 960 CH	X	X	X	X			X	X
64 CH/LN 30 LN 1920 CH	X	X	X	X			X	X
64 CH/LN 16 LN 1024 CH		X					X	
Controlled Data Fields								
High Intensity Field			X		X	X	X	X
Low Intensity Field					X	X	X	X
Blinking Data Field				X	X	X	X	X
Blank Data Field			X	X	X	X	X	X
8th Bit Control of Data Fields								X
Audible Tone Control								
Single Transition of Bit 4			X	X	X	X	X	X
Both Transitions of Bit 4					X	X	X	X
Display Power On Indication Cont								
+5V to LED Panel			X	X				
LED Bit No. 9		X	X	X	X	X	X	X
Keylock Video Blanking			X	X	X	X	X	X
Blinking Cursor @ 30 Hz			X	X	X	X	X	X
Blinking Cursor @ 1 of 5 Rates							X	X
Low Intensity Cursor	X	X					X	X

Table 1-4. Monitor Controller Options (cont)

Option	Monitor Controller Model							
Screen Format	MC-B MOD	MC-B MOD-16	MC-C	MC-C1 MOD	MC-D	MC-D MOD	MC-F	MC-K
Cursor Register								X
Underline Cursor	X						X	X
Dual DA Channel Input					X	X	X	X
4-960 or 2-1920 80 Ch Format					X	X	X	X
4-960 or 2-1920 64 Ch Format							X	X
4-1024 64 Ch Format							X	
External/Internal Oscillator							X	X
128 Displayable Char Types							X	X
Half or Full Duplex Data Trans						X	X	X
12 x 8 PROMS (594542-4) as Ch Gen							X	X
Split Screen 1920 Ch Format w/o Cursor Register	X	X	X	X	X	X	X	X
Split Screen 960 Ch Format w/o Cursor Register							X	X

are available with both upper and lower case characters; however, they are only used with displays that employ 40 or 80 characters per line. The monitor controller also provides the interface for up to four keyboards and four optional status LED indicator assemblies on the displays. Refer to Tables 1-3 and 1-4 for the monitor controller capacity and options provided by each monitor controller model.

1.7.11 Remote Concentrator

The Remote Concentrators (Figure 1-3) contain the monitor controller boards that drive the remote displays located up to 4000 feet from the processor. There are two models of remote concentrator. One can accommodate eight monitor controllers. The other contains only one. Each monitor controller can drive four 480 character, four 960 (or 1024) character, or two 1920 character displays. Each monitor controller connects to a separate I/O channel on a display adapter in the processing unit via a single shielded twisted pair cable. The remote concentrator contains a standard power supply, which is designed to drive four displays. When more than four displays (16 maximum) are connected to a remote concentrator, a display expansion module (35 vdc, 7 ampere) must be installed in the power supply to increase its capacity. Refer to Table 1-3 for the number of monitor controllers that can be used in a remote concentrator.

1.7.12 Display

Data Display Model 4101 has a 15 inch rectangular CRT. It is capable of displaying 480, 960, 1024, or 1920 characters on 12, 15, 16, 24, or 30 lines with 40, 64, or 80 characters per line. Each display uses the memory to store its refresh data. A 1920 character display uses 1920 bytes of memory; a 480 character display uses 480 bytes of memory, etc. The characters on the displays are refreshed at a 60 hertz rate.

The display uses the power supply in the processing unit or in the remote concentrator. It is controlled by its associated monitor controller, which converts the character codes from memory into horizontal and vertical voltages and applies them to the display. There are two character sets: the standard enhanced 7 x 7 dot matrix, upper case only, 64 character set; and the optional enhanced 7 x 9 dot matrix, upper/lower case, 96 character set. The displays may have an optional eight red indicators, Feature 6121, that are set or reset to define system status, message transmission status, and terminal operating modes. These red indicators are mounted vertically on the left of the CRT and are controlled by the user program. The indicators are updated automatically each display refresh period.

1.7.13 IPARS Controller and PTS 1001/A

The PTS 1001/A is a standalone display system that uses a 4101 display mounted on a base that contains an SW1500 power supply and an IPARS controller. It uses a 960 character 64 x 15 format, and can interface a modem and two serial printers. Its program is contained in PROM so there is no IPL. The IPARS controller contains all of the electronics (processor, memory, I/O interfaces, etc.) for the system.

The 1001 has one integral 4101 display. The 1001A can accommodate either one integral 4101 display and 3 SAM slave displays, or 4 SAM displays.

1.7.14 SAM Display

The Stand Alone Monitor (SAM) Display is a 15-inch CRT display and associated keyboard interfaced directly to one DA channel. The SAM display can operate alone or with a second SAM display (slave) and keyboard, connected to the master SAM via coax cable. One SAM can display a maximum of either 960 or 1920 characters. In the SAM and slave SAM configuration, each screen can display 960 characters maximum.

The master SAM consists of a control logic board, analog board, CRT, status display LEDs, keyboard, and keyboard display LEDs. A self-contained power supply on the analog board receives ac line power from any convenient source and generates all ac and dc operating power for the circuits in the master SAM. The control logic board provides the interface between the master SAM and the DA channel.

The slave SAM is similar to the master SAM except that it contains a MUX logic board which executes all control and signal processing functions. The MUX logic board is an abbreviated version of the control logic board since the majority of slave SAM control is performed by the control logic board.

1.7.15 Keyboards

The keyboard contains keys for entry of alphanumeric characters and symbols, text editing, cursor control, and system defined functions. All key functions except SHIFT, REPEAT, and SHIFT LOCK are interpreted and acted upon by the processor software. There are 10 versions of four keyboards: 67, 81, 82, and 89 key. Refer to Section 3 of Chapter 3 for the standard keyboard layouts.

1.7.16 Power Supplies

The SW1500 power supply in the 1001 can support one local display and up to 28K bytes of memory. The SW2000 power supply in the 1005 and 1014 processing units is capable of driving two displays and two 16K memory modules. The SW2000A in the 1008 cannot support a local display, but it can support up to 65K bytes of memory. The other processing units use variations of power supply 594543 (See Section 3.4).

The standard power supply in the remote concentrator is capable of driving four displays. When more than four displays are connected, a remote concentrator display expansion module (±35vdc, 7 ampere) is added to the power supply. This permits the remote concentrator to drive a maximum of 16 displays. See Table 1-3 for the maximum of monitors controllers per remote concentrator.

1.7.17 High Speed Controllers

Various high speed controllers may be attached directly to the processor I/O bus. Data can be transferred over the bus at a rate of 1 megabyte per second. All PTS-100 models except the 1020, 1025, and 1030 will accommodate a maximum of three high speed controllers; models 1020, 1025, and 1030 will accommodate ten. This is in addition to one multiplex controller, and one motherboard, which also attach to the I/O bus. The high speed controllers share board slots in the processing unit with the multiplex channel controller motherboards, monitor controllers, CE console, and multiplex channel controllers. Therefore, the number of high speed controllers that can actually be accommodated is limited by the number of these boards that are installed. Also, available dc power is a limiting factor. The high speed controllers attach the following devices to the PTS-100:

- Disc Memories
- Magnetic Tape Units
- Host Processor Channel Interface Controllers (CIC)
- Async Data Processor (ADP)
- Other Special High Speed Interfaces

1.7.18 Customer Engineer Console

The customer engineer (CE) console is an optional maintenance and programming aid. It connects directly to the processor I/O bus and takes priority over all other controllers. It permits machine language instructions and data to be entered manually into memory, and it displays the contents of the ACC,

PC, X1, and X2 registers or addressed memory locations. In PTS-100 Models 1010 and 1015, the CE console can be connected to board slots A1, A3, or A4. In PTS-100 Model 1020, 1025, and 1030, it can be connected to board slots A1 through A8, A11, or A12. Since one multiplex channel controller is necessary to provide system clocks, the CE console cannot be connected to the slot occupied by that multiplex channel controller. Also, the CE console cannot be connected to slot A2 (Model 1010/1015) or slot A9 (Model 1020) since these slots have no J1 connector. Connection is made to either the front board slot or the rear backplane wiring.

1.8 Related Publications

1.8.1 Raytheon Manuals

PTS-100 Operators Manual	44-7645
PTS-100 Programmers Handbook	44-7644
PTS-100 IODC Diagnostic Functional Specifications Magnetic Tape and Listing	593951
PTS-100 Facilities Planning	44-10214
Installation Procedure	44-8021

1.8.2 PTS-100 Equipment Vendor Manuals

Card Reader, Documation Manuals M-200, M-400, and M-1000

Teletype Printer Models 3402, 3403, 3404

Teletype Corp. Bulletin 310B Vol. I & II

Teletype Corp. Bulletin 1184B

Teletype Corp. Wiring Diagram Package WDP-316

Cassette Drive, MFE Model 250 M3601

Cartridge Disc Drive, Diablo Disk Series 30

Maintenance Manual D3140-171 and Model 029 Power Supply Product Data Description PS 029-172

Serial Printer Models 3401 and 3411, G. E. TermiNet Operation and Service Literature 44A410543-G10 and GEH 2185A, 36105, 36122, 36100, 36123

Serial Matrix Printer Model 3412, Centronics Model 101A Technical Manual, Interface, and Operators Manual

Ticket Printer Model 3421 DI/AN Maintenance Manual

Ticket Printer Model 3422 Maintenance Manual 44-7672

Boarding Pass Printer Model 3423 DI/AN Maintenance and Operation Manuals

Boarding Pass Printer Model 3424 Maintenance Manual 44-7670

High Speed Paper Tape Punch, Teletype Corp., Manuals 215B and 1154B and Lambda Power Supply Manual LM D-Package

Paper Tape Reader Remex RR105/305

Paper Tape Punch, Teletype Corp., Technical Manual 215B, Parts 1154B

Teleprinter, Extel Instruction Manual AE & AF

Serial Matrix Printer Centronics Model 306 & 300; also PTS-100 Interface Technical Manual

ICC Modem 2200 Installation Manual

PERTEC Mod 6 x 40 & 6 x 60 Transport Manual	5-9019
Diablo Mod. 44B Disc Drive Maintenance Manual	5-9198
CDC 8K 5XX Inst & Chk Out Maintenance Manual	5-9186
CDC DIAS, Maintenance Manual for 300 mb	5-9202
Extel AH-11 (B) 30 cps PTR I & Op Manual	5-9180
Centronics Technical Manual for 702-PTR	5-9211

CHAPTER 2. INSTALLATION

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

2.1 General

This chapter contains installation information for the various PTS-100 equipment. It provides all the physical, electrical, and environmental data required to plan and complete an installation.

2.2 Equipment Characteristics

The electrical, environmental, and physical characteristics of the PTS-100 are shown in Table 2-1.

2.3 Air Flow and Equipment Mounting Dimensions

Each PTS-100 equipment has an air moving system that provides the cooling necessary for safe, reliable operation over the specified range of equipment operating temperatures. The recommended air flow clearances are shown in Figure 2-1. It is important that installations be planned to avoid blocking or restricting the air flow to or from the equipment.

It is also important that installation planning consider the air flow systems of adjacent equipment to ensure that the exhaust air of one equipment is not directed at the intake of an adjacent equipment. Operating and nonoperating temperatures for each equipment must be maintained within the limits specified in Table 2-1. Since the operating temperature of the equipment depends largely on air flow, nothing should be done at installation to alter this factor appreciably.

The tops of the equipment should not be used for storage or for mounting other equipment.

2.4 Static Electricity

Since electrostatic discharges may affect MOS semiconductor and memory circuits, site and installation planning should include consideration of floor covering materials that will minimize the buildup of static electricity. If carpeting is to be used, it is recommended that special carpeting be installed with a percentage of metallic fibers that will limit the electrostatic potential.

If standard carpeting has been installed previously, static electricity buildup may be controlled through the use of an antistatic spray and by maintaining adequate humidity.

Table 2-1. Physical and Environmental Characteristics

	Unpacked				Packed				Ambient Temp. Range			Altitude	
Equipment	Height inch/cm	Width inch/cm	Depth inch/cm	Weight lbs/kg	Height inch/cm	Width inch/cm	Depth inch/cm	Weight lbs/kg	Operating °F/C	Nonoperating °F/C	Relative Humidity %	Operating ft/m	Nonoperating ft/m
Mark I Processor	63.5/162	25.75/65	33.5/85	500/227	75/191	32/82	46/117	600/272	60/15 - 90/32	-25/-32 - 140/60	35 - 60	6,000/1,800	10,000/3,048
1020/1025/1030** 5 ft cabinet * Mark II Processor	63.5/162	24.5/63	27.5/70	450/203**	75/191	32/82	35/89	550/250**	40/4 - 110/43	-40/-40 - 150/66	20-95	10,000/3,048	50,000/15,240
	63.5/162	24.5/63	27.5/70	450/203**	75/191	32/82	35/89	550/250	60/15 - 90/32	-25/-32 - 140/60	35 - 60	6,000/1,800	10,000/3,048
1014/1015/1015M/ 1018 Processor	18/46	19.5/50	22/56	130/59	25/64	26/66	28/71	150/68	50/10 - 104/40	-25/-32 - 140/60	20 - 90	8,000/2,400	10,000/3,048
1020 Processor 4 ft Cabinet	51.5/131	24.5/63	27.5/70	400/181	63/160	32/82	35/89	500/230	↓	↓	↓	↓	50,000/15,240
1001A/1005/1008 Processor w/o Display and Keyboard	8.0/20	18/46	16.6/42.2	20/9	***	***	***	***	↓	↓	↓	↓	40,000/12,000
1001/1001A/1005 Processor with Display and Keyboard	18.75/47	18/46	25.75/65	55/25	25/65	26/66	28/72	75/34	50/10 - 104/40	-25/-32 - 140/60	20 - 90	8,000/2,400	10,000/3,048
1030B (3800) Disc Cabinet	63.5/162	24.5/63	27.5/70	590/251	75/191	32/82	35/89	690/288	60/15 - 90/32	-25/-32 - 140/60	35 - 60	6,000/1,800	10,000/3,048
Magnetic Tape Cabinet 3900, 3910	63.5/160	25.75/65	27.5/70	350/159	75/191	32/82	35/89	450/204	60/15 - 90/32	-25/-32 - 140/60	35 - 60	6,000/1,800	10,000/3,048
Diablo 44B Disc Cabinet (3810-02F)	37.5/95.3	24.5/62.3	33.5/85	800/363	52/132	37/94	46/117	900/409	60/15 - 90/32	-25/-32 - 140/60	35 - 60	6,000/1,800	10,000/3,048
4301 Remote Concentrator	18/46	19.5/50	22/56	140/64	25/65	26/66	28/72	160/73	50/10 - 104/40	-25/-32 - 140/60	20 - 90	8,000/2,400	10,000/3,048
4302 Remote Concentrator	16.3/42	16.8/43	7.3/19	15/7	24/61	24/61	14/36	30/14	↓	↓	↓	↓	↓
4101 Display w/Keyboard	14/36	18/46	22.5/65	35/16	26/66	25/64	25/64	67/31					
4101 Display w/o Keyboard	14/36	18/46	18/46	28/13	26/66	25/64	25/64	60/78					
Keyboard (4101)	4/10	18/46	8.75/23	7/3	N/A	N/A	N/A	N/A					

Table 2-1. Physical and Environmental Characteristics (cont)

	Unpacked				Packed				Ambient Temp. Range			Altitude		
4103/4104 Display (SAM) w/ Keyboard (Master & Slave)	14/36	18/46	25.5/65	50/21	26/66	25/64	25/64	67/31						
4103/4104 Display (SAM) w/o Keyboard (Master & Slave)	14/36	18/46	18/46	40/18	26/66	25/64	25/64	60/26						
Keyboard (4103)	4/10	18/46	8.75/23	10/5	N/A	N/A	N/A	N/A						
2201 Printer Controller	5.3/13.5	10.9/27.7	13.3/33.8	10/4.5	***	***	***	***						
3201 Card Reader	11.5/29	19.8/50	14.8/38	60/27	18/46	26/66	21/54	80/36						
3301 Line Printer	45/115	33/84	22/56	340/155	52.8/135	41/105	31.5/80	386/180						
3306 Line Printer	40/115	33/84	26/66	370/168	53.5/136	41.5/105.4	33/84	425/193						
3401 Char. Printer	7.5/19	19/48	22/56	65/30	14/36	27/69	34/87	84/38						
3402 RO TTY	33/84	18.7/48	18.5/47	52/23	39/100	27.5/70	23/59	125/56						
3404 ASR TTY	33/84	22/56	18.5/47	56/25	39/100	27.5/70	23/59	129/58						
3405, 3407 Char. Printer	5/13	12.6/32	17.8/35	25/11.5	13/33	19.5/50	22/56	30/14						
3406 Char. Printer	13/33.02	23.2/59	19.48	66/30	22/55.8	28/71	27/68.5	80/36.4						
3408 Char. Printer	8.25/21	23.3/59.1	15.7/39.9	48/21.8	16/40.6	26/66	28/71	58/26						
3412 Char. Printer	11.5/29	27.8/71	20/51	118/53	20/51	31/79	24/61	145/70						
Stand for 3412	25/64	19.7/50	35/89	52/24	27/69	24/62	20/51	62/29						
3414 Char. Printer	34.3/87	26.6/57.7	15.4/39.1	91/41	30/91.5	39/99	27/68.6	111/50.4						
3421 Ticket Printer	36.8/94	18.8/48	24.2/62	130/59	39.5/100	21.5/55	28.3/72	140/64						
3422 Ticket Printer	26/66	25/64	25/64	270/122	29/74	29/74	26/66	350/160						

Table 2-1. Physical and Environmental Characteristics (cont)

	Unpacked				Packed				Ambient Temp. Range			Altitude	
3423 Boarding Pass Printer	12/31	10.5/27	23.5/60	70/32	16.5/42	15/38	28/72	80/36					
3424 Boarding Pass Printer	See Fig. 2-1, M	See Fig. 2-1, M	See Fig. 2-1, M	See Fig. 2-1, M	29.5/75	22/56	32.5/83	110/50					
3430 Boarding Pass Printer	12/31	10.8/27	24/62	55/25	15.5/38	14/36	27.5/70	80/36					
3440 Ticket Printer	24/61	12/30.5	24/61	90/40.8	△	△	△	△					
3445 Ticket Printer	24/61	12/30.5	24/61	90/40.8	△	△	△	△					
3472 Char. Printer	9/22.9	25/63.5	19.5/49.5	75/34	15/38	31/79	16/66	90/41					
6140 Badge Reader	6.25/17	6.5/17	90/23	6/2.6	***	***	***	***					
6150-1 Mag. Stripe Reader	4/10	5/12.7	8.5/21.6	5/2.3	***	***	***	***					
9101 CE Console	17/43	20.5/5.2	7/18	20/9	24/61	24/61	14/36	35/16					
3601 Cassette Drive	4.3/11	7.3/18.5	5.8/14.8	4/1.8	***	***	***	***	50/10 - 104/40	-25/-32 - 140/60	20 - 90	8,000/2,400	10,000/3,048
Diablo 44B (3810-02) Disc Drive w/o Cabinet	10.3/26.2	18.8/48	30.2/76.5	135/61.3	22/55.8	40/100	30/76.2	150/68	60/15 - 90/32	-25/-32 - 140/60	35 - 60	6,000/1,800	10,000/3,048
3820 Storage Module Drive	34/86.4	19/48.3	34/86.4						60/15 - 90/32	-25/-32 - 140/60	35 - 60	6,000/1,800	10,000/3,048

*Required for 1020 with CIC and Cabinet mounted modem

**When more than two power supplies are installed, add 100 pounds (45.5 Kg) per power supply

***Shipped in containers with additional equipment

+CIC and Cabinet mounted modem not available on 1030

△ Units packed in two cartons. Dimensions of individual cartons: Height 14/35.6, Width 14/35.6, Depth 26/66, Weight of individual carton 45/20.4

All values are approximate.

2.5 Power Cables and Power Requirements

The power requirements for each equipment in the PTS-100 system are given in Table 2-1, and the power cables are described in Table 2-2. PTS-100 system equipment requiring primary power has been designed to operate from a single phase alternating current power source. It is recommended that dedicated power circuits be made available for all PTS-100 equipment.

The branch circuit and plug receptacles supplying PTS equipments must meet the following conditions:

a. An insulated grounding conductor that is identical in size and insulation to the grounded and ungrounded branch-circuit supply conductors except that it is green or green with one or more yellow stripes is to be installed as part of the branch circuit that supplies the unit or system.

b. The grounding conductor mentioned in item a is to be grounded at the service equipment.

c. The plug receptacles in the vicinity of the unit or system are all to be of a grounding type, and the grounding conductors serving these receptacles are to be connected to the grounding conductor that serves the unit or system.

In the event that a two-wire system is used and there is no ac ground line, equipment chassis ground must be connected directly to the building ground system. This should be accomplished by using a separate insulated conductor which is equivalent in wire guage to that used in the power cord for that equipment as specified in Table 2-2.

When a three-wire system is used, the chassis grounds are connected to the third wire AC grounds within the equipment. If the AC grounds are all connected to the building ground and the building AC ground conductor is sufficient to carry the ground current, no additional ground is required.

Table 2-2. Electrical Characteristics

	Power Requirements†† International Sites			Power Requirements U.S. Sites									
Equipment	Voltage	Current (amps) Nominal Unless Otherwise Noted	Hz	Voltage	Current (amps) Nominal Unless Otherwise Noted	Hz	Req'd Supply Branch Circuit	BTU/Hr Nominal Unless Otherwise Noted	Watts Nominal Unless Otherwise Noted	Power Cord Length ft./m	Power Cord Dia inch/mm	Number of Conductors /AWG	Plug Type (115 vac only)
Mark I Processor	220-260	6.5	47-53	103-127	13.0	57-63	20	4880	1430	10/3	.65/17	3/#12	2 Pole 3 Wire Locking
1020/1025 Processor***†	207-253	8.0	47-53	103-127	16.0 max.	57-63	20	6800 max.	2000 max.	10/3	.65/17	3/#12	2 Pole 3 Wire Locking*
Mark II/1030 Processor***†	207-253	10.0	47-53	103-127	20.0 max.	57-63	30	8500 max.	2500 max.	10/3	.65/17	3/#12	2 Pole 3 Wire Locking††
1014/1015/1015M/ 1018 Processor***†	207-253	4.3	47-53	103-127	10.0 max.	57-63	15	3900 max.	1150 max.		.35/9	3/#16	2 Pole 3 Wire Grounding Non-Locking
1001A/1005/1008 Processor w/o Display and Keyboard	184-276	1.6	47-53	92-138	3.2	54-66	15	1000	300	8/2.5	.25/7	3/#18	2 Pole 3 Wire Grounding Non-Locking
1001A/1001/1005 Processor with Display Keyboard	184-276	1.6	47-53	92-138	3.2	54-66	15	1100	340	8/2.5	.25/7	3/#18	2 Pole 3 Wire Grounding Non-Locking
1030B (3800) Disc Cabinet	220-260	7.0 max.	47-53	100-130	14.0 max.	57-63	20	5600 max.	1600 max.	10/3	.65/17	3/#12	2 Pole 3 Wire Locking*
Magnetic Tape Cabinet	220-260	2.6	47-53	100-130	5.2	57-63	20	1904	560	10/3	.65/7	3/#12	2 Pole 3 Wire Locking
Diablo 44B Disc Cabinet (3810-02F)	220-260	2.6	47-53	100-130	5.2	57-63	20	1917	562	10/3	.65/7	3/#12	2 Pole 3 Wire Locking
4301 Remote Concentrator***†	207-253	6.0 max.	47-53	103-127	12.0 max.	57-63	15	3750 max.	1100	10/3	.35/9	3/#16	2 Pole 3 Wire Grounding Non-Locking
4302 Remote Concentrator***	207-253	1.0 max.	47-53	103-127	2.0 max.	57-63	15	360	100	10/3	.35/9	3/#16	2 Pole 3 Wire Grounding Non-Locking
4101 Display	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
4103 Display (Master)	210-230	0.4	47-63	105-125	0.8	47-63	1.5 Slow Blow	240	70	8/2.5	.35/9	3/#16	2 Pole 3 Wire Non-Locking
4103 Display (Slave)	210-230	0.3	47-63	105-125	0.6	47-63	1.5 Slow Blow	205	60	8/2.5	.35/9	3/#16	2 Pole 3 Wire Non-Locking

Table 2-2. Electrical Characteristics (cont)

	Power Requirements†† International Sites			Power Requirements U.S. Sites									
Equipment	Voltage	Current (amps) Nominal Unless Otherwise Noted	Hz	Voltage	Current (amps) Nominal Unless Otherwise Noted	Hz	Req'd Supply Branch Circuit	BTU/Hr Nominal Unless Otherwise Noted	Watts Nominal Unless Otherwise Noted	Power Cord Length ft. /m	Power Cord Dia inch/mm	Number of Conductors /AWG	Plug Type (115 vac only)
2201 Printer Controller	210-230	0.11	47-63	105-125	0.22	47-63	1.5	86	25	8/2.5	.35/9	3/#16	2 Pole 3 Wire Non-Locking
3201 Card Reader	198-242	2.1	47-53	103-127	4.2	57-63	15	1700	500	9/2.8	.35/9	3/#16	2 Pole 3Wire Grounding Non-Locking
3301 Line Printer	198-242	2.5	47-53	103-127	5.0	57-63	15	1800	525	12/3.6	.38/10	3/#16	2 Pole 3 Wire Non-Locking
3306 Line Printer	210-230	3.1	49-61	105-125	6.2	59-61	15	2319	680	12/3.6	.35/9	3/#16	2 Pole 3 Wire Non-Locking
3401 Char. Printer	211-257	0.5	48.5-51	105-129	1.0	58.5-61	15	400	120	6/1.7	.25/7	3/#18	2 Pole 3 Wire Non-Locking
3402 RO TTY	198-242	1.0	47-53	103-127	2.0	57-63	15	800	250	7/2.1	.25/7	3/#16	2 Pole 3 Wire Non-Locking
3404 RO TTY	198-242	1.0	47-53	103-127	2.0	57-63	15	800	250	7/2.1	.25/7	3/#16	2 Pole 3 Wire Non-Locking
3405, 3407 Char. Printer	207-253	0.25	47-53	103-127	0.5	57-63	15	200	60	8/2.5	.3/8	3/#18	2 Pole 3 Wire Non-Locking
3406 Char. Printer	211-257	1.6	47-53	105-129	3.2	57-63	15	1275	375	8/2.5	.3/8	3/#16	2 Pole 3 Wire Non-Locking
3408 Char. Printer	210-230	0.9	47-53	105-125	1.8	57-63	15	750	200	12/3.8	.35/9	3/#16	2 Pole 3 Wire Non-Locking
3412 Char. Printer	211-257	2.0	47-53	105-129	4.0	57-63	15	1500	450	8/2.5	.25/7	3/#16	2 Pole 3 Wire Non-Locking
3414 Char. Printer	210-230	0.8	49-51	107-127	1.6	59-61	15	60	175	9/2.8	.35/9	3/#16	2 Pole 3 Wire Non-Locking
3421 Ticket Printer	210-240	2.2	48-52	105-125	4.3	58-62	15	1700	500	5/1.5	.35/9	3/#16	2 Pole 3 Wire Non-Locking
3422 Ticket Printer	207-253	1.6	47-53	103-127	3.3	57-63	15	1400	400	8/2.5	.35/9	3/#16	2 Pole 3 Wire Locking**
3423 Boarding Pass Printer	210-240	1.3	48-52	105-125	2.6	58-62	15	1000	300	5/1.5	.25/7	3/#18	2 Pole 3 Wire Non-Locking

Table 2-2. Electrical Characteristics (cont)

Equipment	Power Requirements†† International Sites			Power Requirements U.S. Sites			Req'd Supply Branch Circuit	BTU/Hr Nominal Unless Otherwise Noted	Watts Nominal Unless Otherwise Noted	Power Cord Length ft./m	Power Cord Dia inch/mm	Number of Conductors /AWG	Plug Type (115 vac only)
	Voltage	Current (amps) Nominal Unless Otherwise Noted	Hz	Voltage	Current (amps) Nominal Unless Otherwise Noted	Hz							
3424 Boarding Pass Printer	198-242	1.5	48-52	103-127	3.0	58-62	15	1700	500	6/1.7	.25/7	3/#16	2 Pole 3 Wire Locking**
3430 Boarding Pass Printer	198-242	0.67	48-52	99-121	1.3	58-62	15	561	165	5/1.5	.25/7	3/#18	2 Pole 3 Wire Grounding Non-Locking
3440 Ticket Printer	210-230	0.75	48-52	100-120	1.5	58-62	15	563	165	8/2.5	.35/9	3/#16	2 Pole 3 Wire Non-Locking
3445 Ticket Printer	210-230	0.75	48-52	100-120	1.5	58-62	15	563	165	8/2.5	.35/9	3/#16	2 Pole 3 Wire Non-Locking
3472 Char. Printer	215-240	1.70	49-51	100-125	3.40	59-61	15	1280	375	12/3.8	.35/9	3/#16	2 Pole 3 Wire Non-Locking
6140 Badge Reader	207-253	0.10	47-53	103-127	0.20	57-63	15	68	20	7/2.1	.38/10	3/#18	2 Pole 3 Wire Grounding Non-Locking
6150-01 Mag. Stripe Reader	210-230	0.10	47-63	105-125	0.20	47-63	0.5	68	20	8/2.5	.35/9	3/#16	2 Pole 3 Wire Grounding Non-Locking
Diablo 44B (3810-02) Disc Drive w/o Cabinet	210-230	1.3	49-61	110-130	2.6	49-61	N/A	N/A	281	N/A	N/A	N/A	N/A
3820 Storage Module Drive	195-235	4.9	48-53	102-128	6.6	59-66	15	2500	725	8/2.5	.35/9	3/#16	2 Pole 3 Wire Non-Locking

*Mates with Hubbell 2310 Outlet or 2313 Cable Receptacle, NEMA L5-20 R

**Mates with Hubbell 4700 Outlet or 4730 Cable Receptacle, NEMA L5-15 R

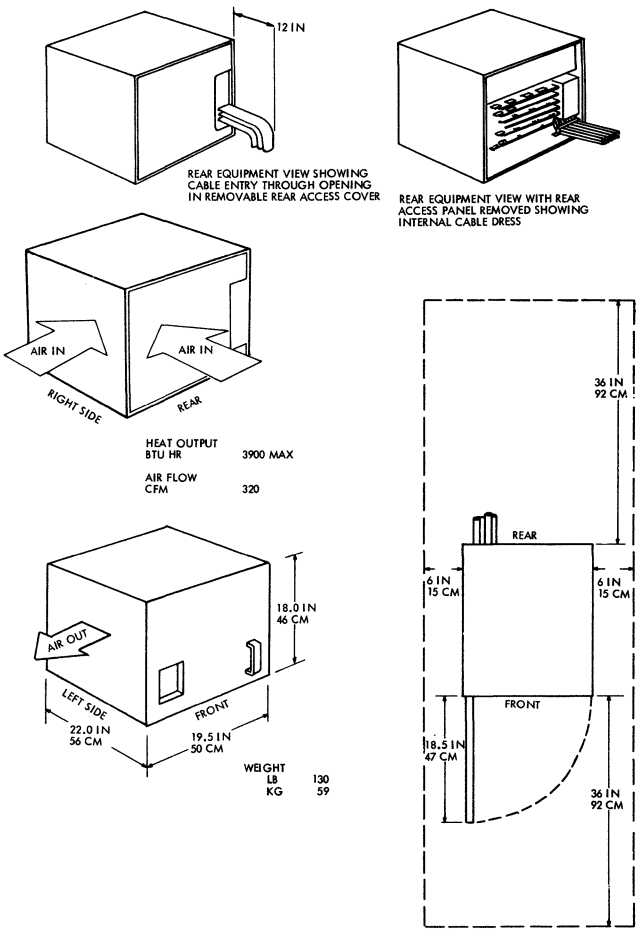
All non-locking plugs mate with Hubbell 5252 Outlet on 5269C Cable Receptacle, NEMA L5-15R

***Equipment grounding is required

†Power requirements indicated are for maximum equipment configurations.

††Non-standard power requirements must be defined at time of order.

†††Mates with Hubbell 2610 Outlet or Hubbell 2613 Cable Receptacle, NEMA L5-30R



A. PROCESSING UNIT MODELS 1014 AND 1015

Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 1 of 17)

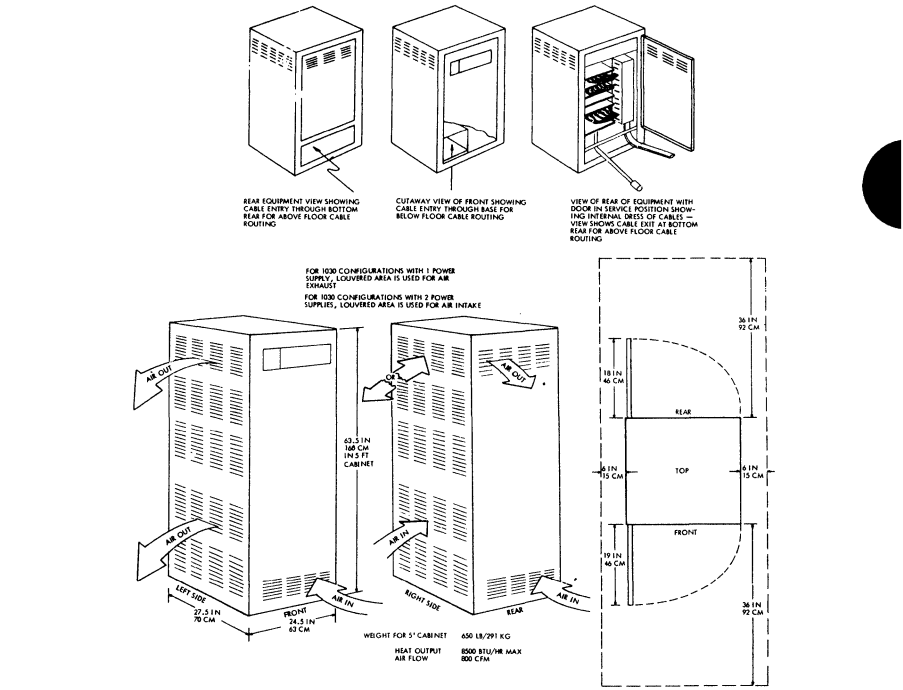
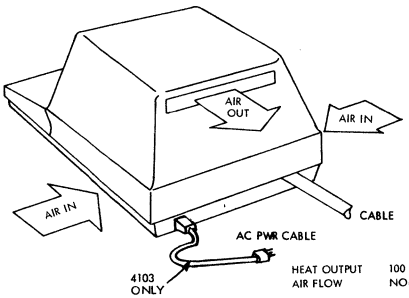


Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 2 of 17)

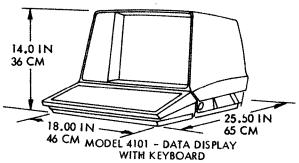


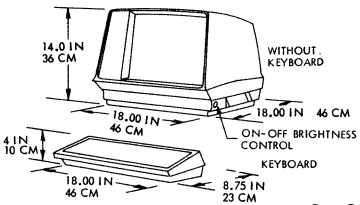
WEIGHT (4101):

DATA DISPLAY WITH KEYBOARD	35 LB/16 KG
DATA DISPLAY WITHOUT KEYBOARD	28 LB/13 KG
KEYBOARD	7 LB/3 KG

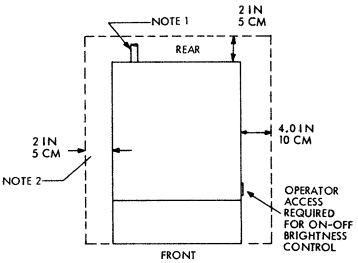
WEIGHT (4103):

DATA DISPLAY WITH KEYBOARD	50 LB/21 KG
DATA DISPLAY WITHOUT KEYBOARD	40 LB/18 KG
KEYBOARD	10 LB/5 KG





THE DATA DISPLAY AND KEYBOARD ARE SEPARATE UNITS WHICH APPEAR TO BE A SINGLE UNIT WHEN NESTED.

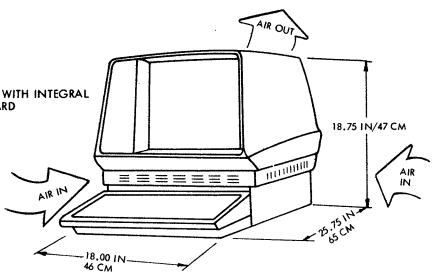


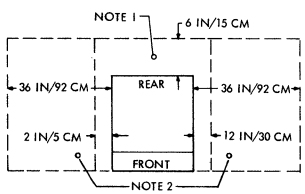
NOTE 1 IF REAR ACCESS IS NOT CONVENIENT A SHORT SERVICE CABLE LOOP WILL BE REQUIRED SO THAT SET CAN BE PULLED FORWARD FOR DETACHING SIGNAL CABLE

NOTE 2 A 2" MINIMUM CLEARANCE MUST BE MAINTAINED AS SHOWN, TO AVOID RESTRICTING EQUIPMENT AIR FLOW.

D. DISPLAY TERMINAL MODELS 4101, 4103 (SAM)

WEIGHT	55 LB/25 KG FOR 1005 WITH INTEGRAL DISPLAY AND KEYBOARD
HEAT OUTPUT BTU/HR	1100 MAX
AIR FLOW CFM	100



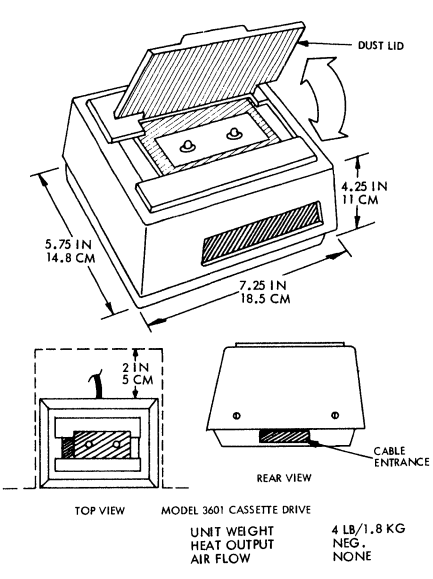


NOTE 1. INSTALLATIONS USING THIS DIMENSION MUST PROVIDE CABLE SLACK TO ALLOW UNIT TO BE MOVED FOR MAINTENANCE CLEARANCE

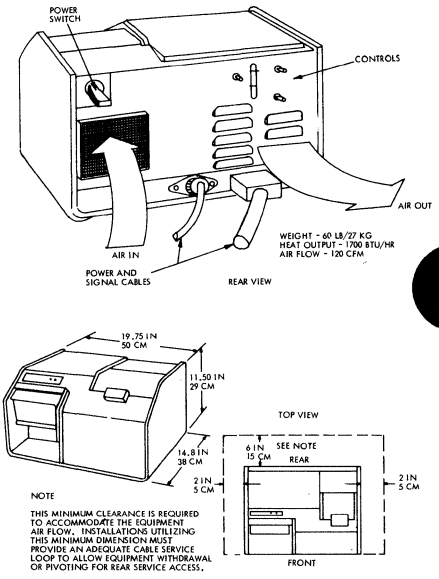
NOTE 2. REFER TO APPENDIX B FOR LARGER CLEARANCES BETWEEN THE DISPLAY TERMINAL AND ELECTROMAGNETIC DEVICES.

E. 1005 STANDALONE PROCESSING SYSTEM

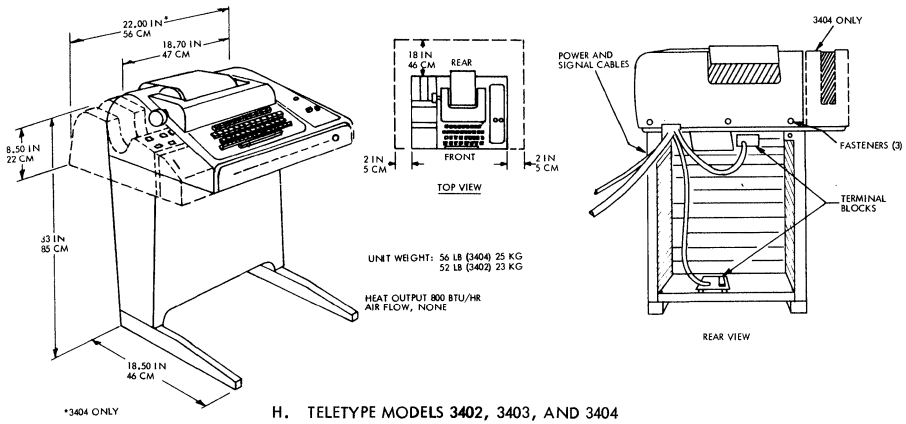
Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 3 of 17)



F. MAGNETIC TAPE CASSETTE MODEL 3601

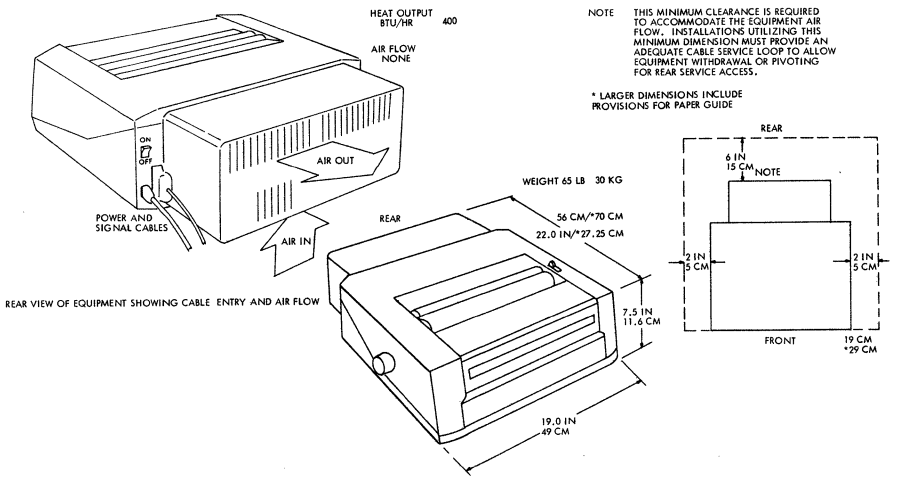


G. CARD READER MODEL 3201

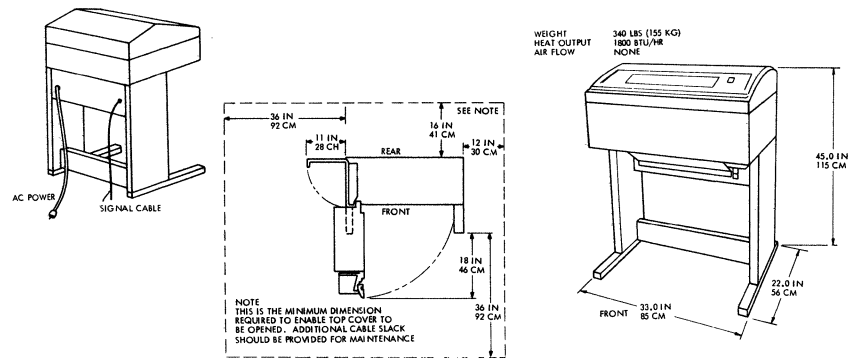


H. TELETYPE MODELS 3402, 3403, AND 3404

Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 4 of 17)

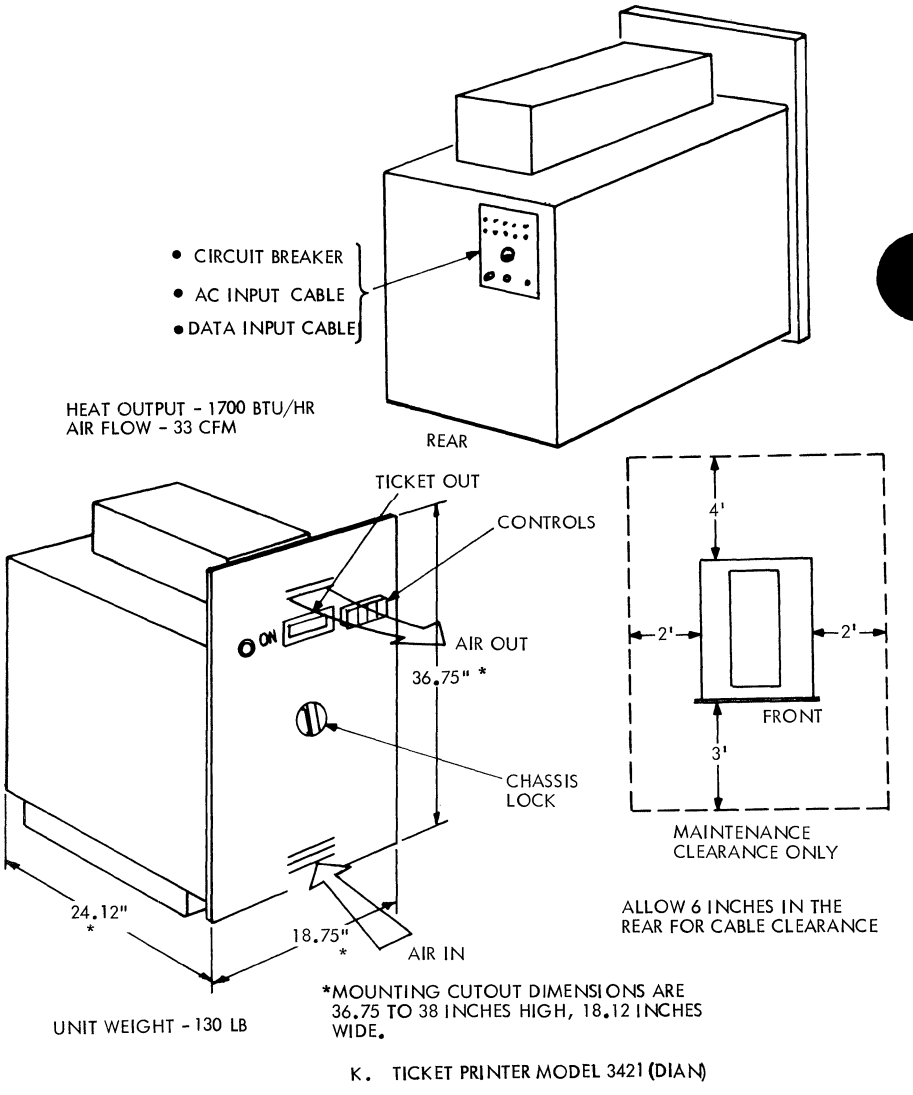


I. SERIAL PRINTER MODEL 3401



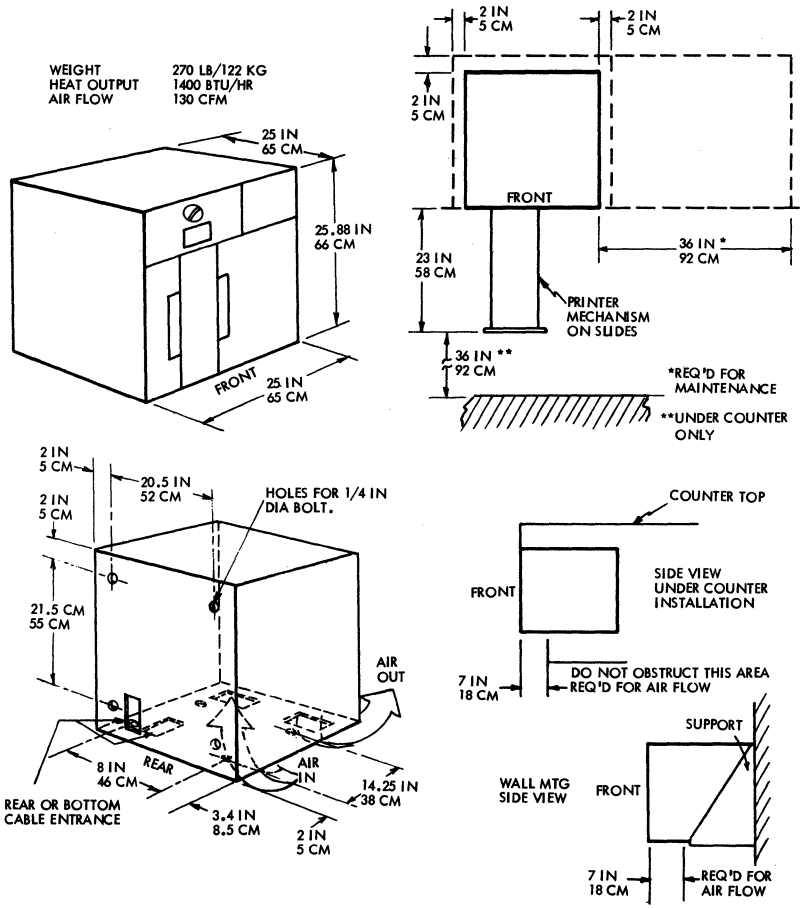
J. LINE PRINTER MODEL 3301

Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 5 of 17)



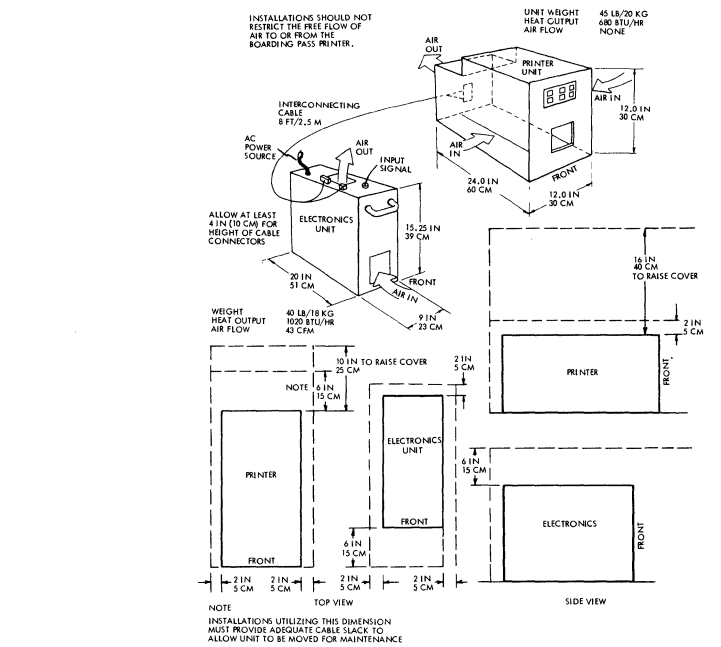
K. TICKET PRINTER MODEL 3421 (DIAN)

Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 6 of 17)

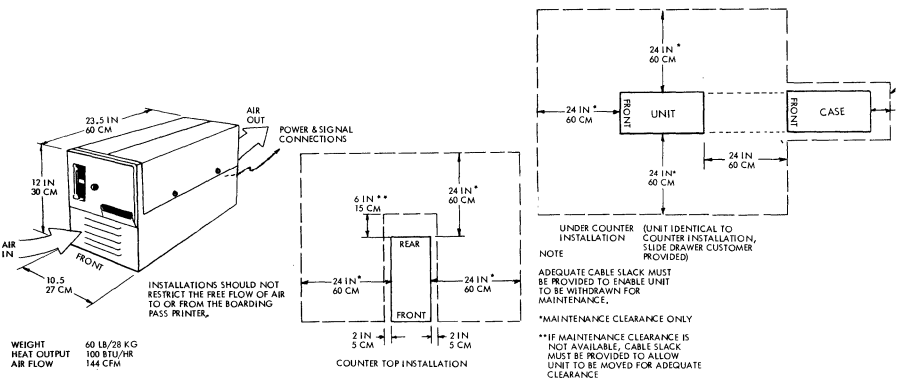


L. TICKET PRINTER MODEL 3422 VOGUE

Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 7 of 17)

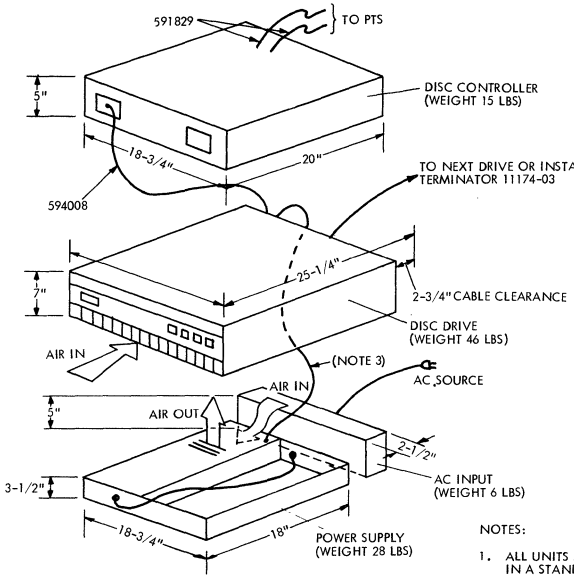


M. BOARDING PASS PRINTER MODEL 3424 (VOGUE)



N. 3423 BOARDING PASS PRINTER (DIAN)

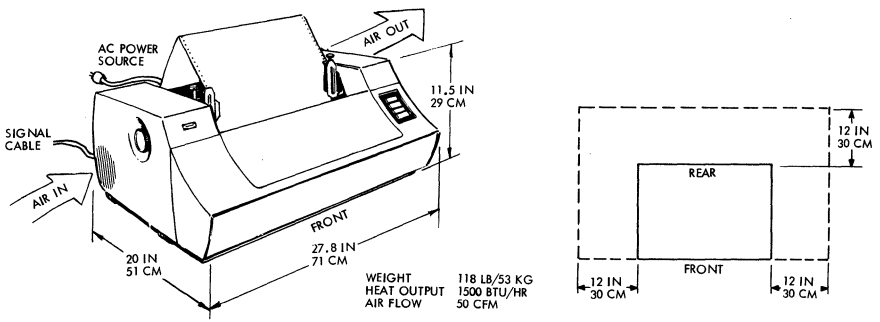
Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 8 of 17)



NOTES:

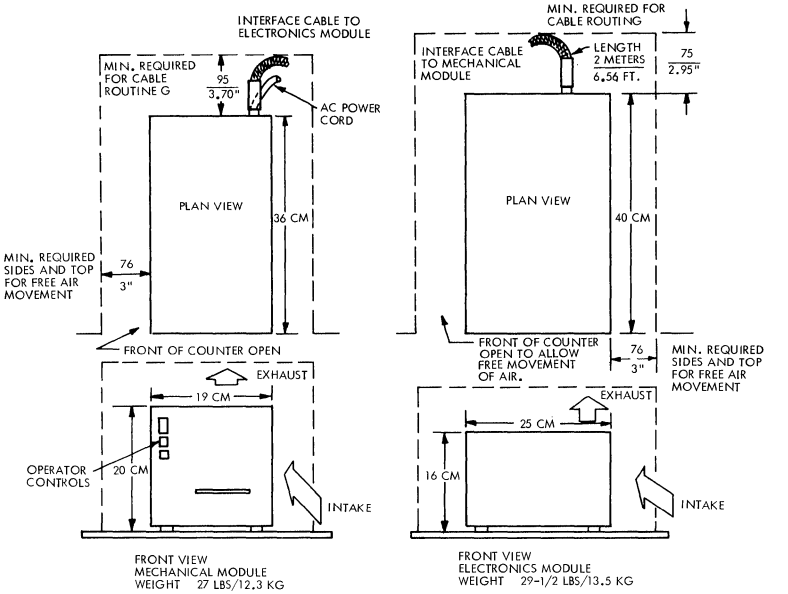
1. ALL UNITS ARE DESIGNED TO MOUNT IN A STANDARD 19 INCH RACK.
2. ONE POWER SUPPLY CAN DRIVE TWO DISC DRIVES.
3. CONNECTOR TO DISC DRIVE. RED WIRES CONNECT TO PS +15V. BLUE WIRES CONNECT TO PS -15V.

Q. CARTRIDGE DISC SYSTEM: INNER CABINET CABLING

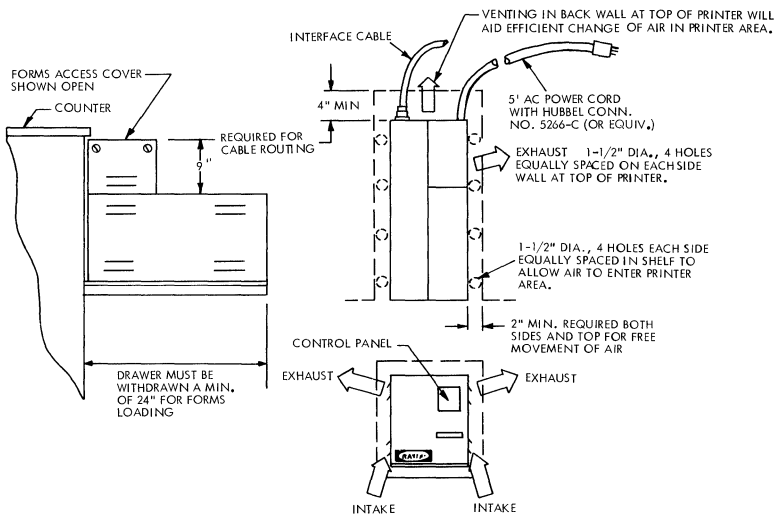


R. MATRIX PRINTER MODEL 3412

Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 9 of 17)

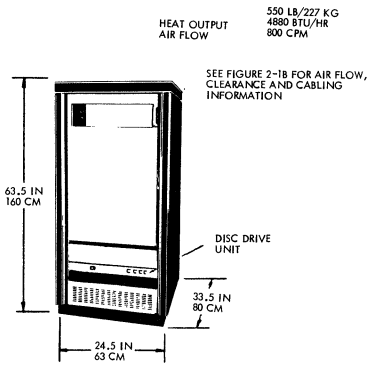


S. IER BOARDING PASS PRINTER

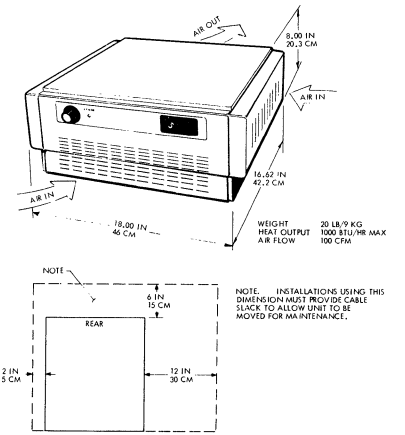


T. RAYTHEON BOARDING PASS PRINTER (CANOE)

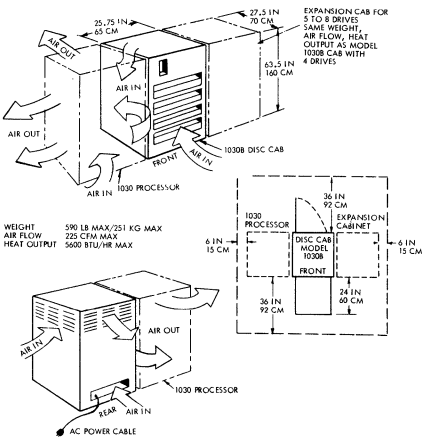
Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 10 of 17)



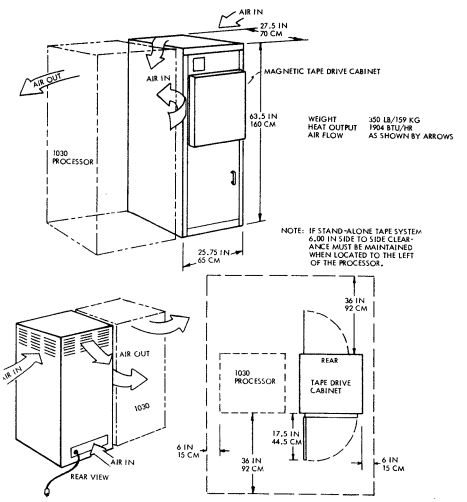
U. PROCESSING UNIT MODEL MARK I



V. PROCESSING UNIT, MODELS 1001A, 1005, 1008 (WITHOUT DISPLAY AND KEYBOARD)

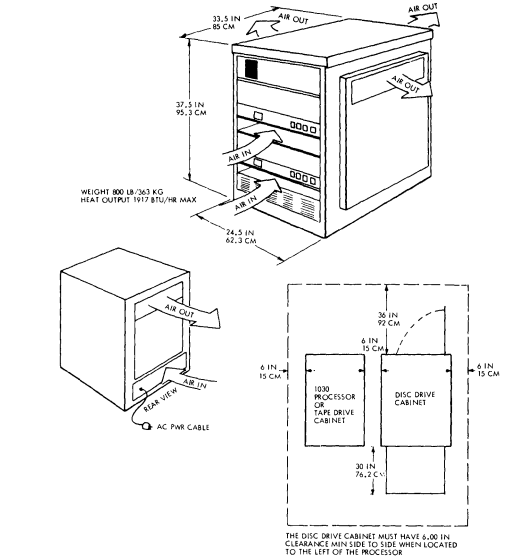


W. DISC DRIVE CABINET MODEL 1030B

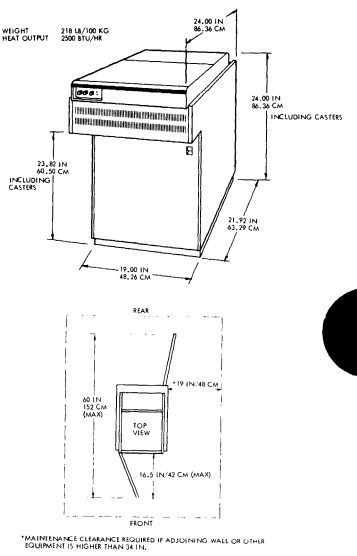


X. MAGNETIC TAPE DRIVE CABINET

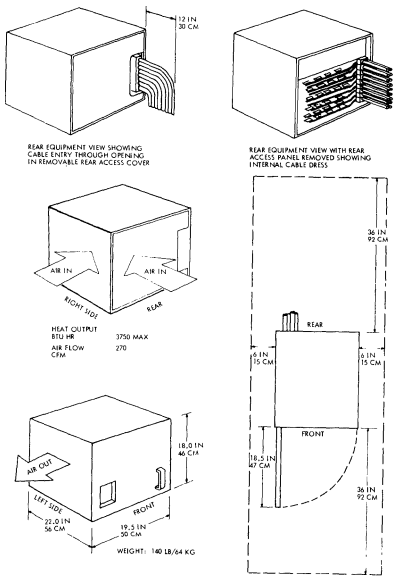
Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 11 of 17)



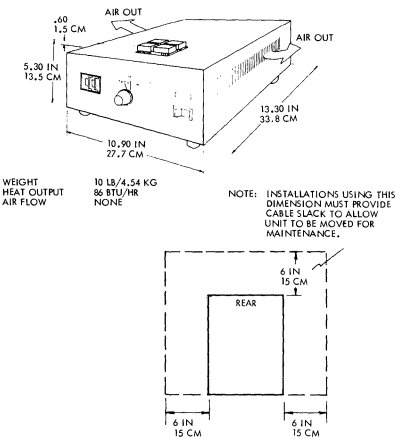
Y. DISC DRIVE CABINET MODEL 3810



Z. STORAGE MODULE DRIVE

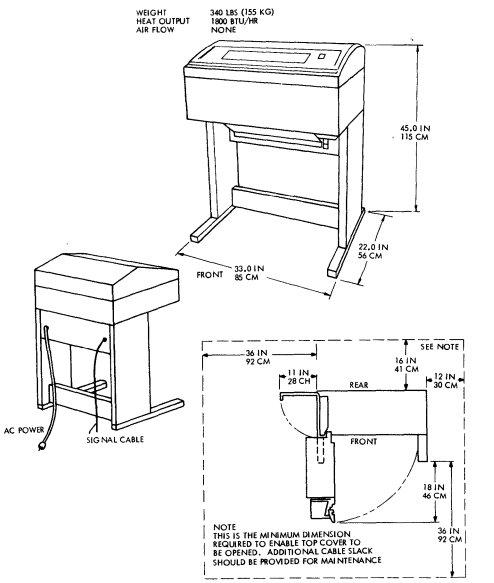


AA. REMOTE CONCENTRATOR MODEL 4301

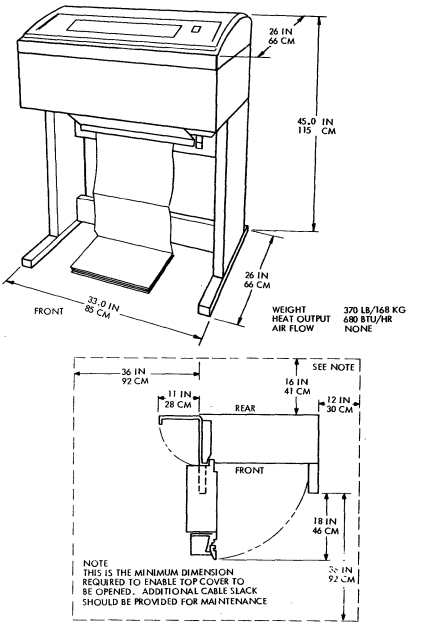


AB. PRINTER CONTROLLER MODEL 2201

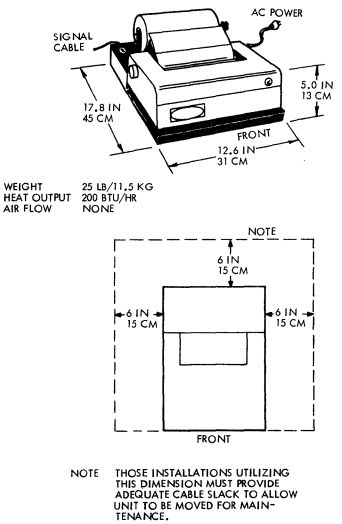
Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 12 of 17)



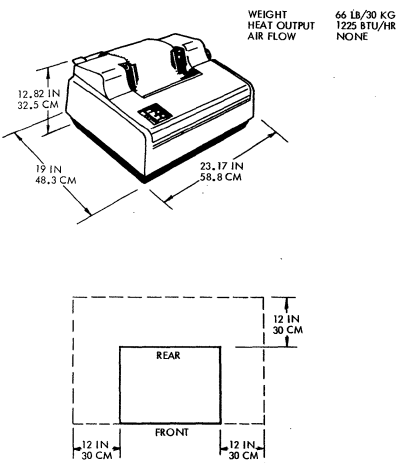
AC. LINE PRINTER MODEL 3301



AD. LINE PRINTER MODEL 3306

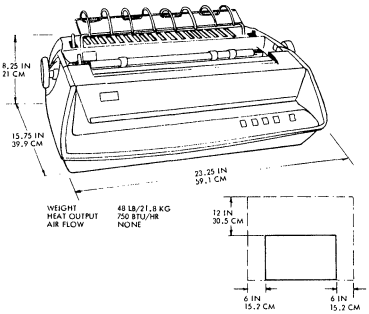


AE. IMPACT PRINTER MODELS 3405 AND 3407

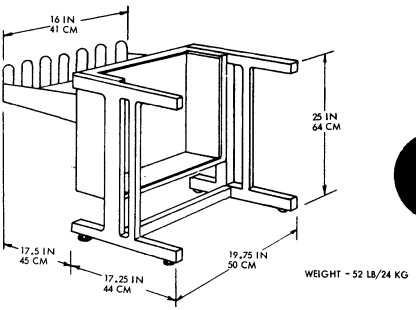


AF. MATRIX PRINTER MODEL 3406

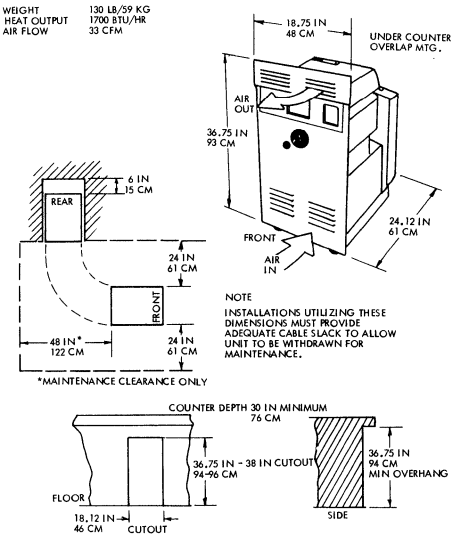
Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 13 of 17)



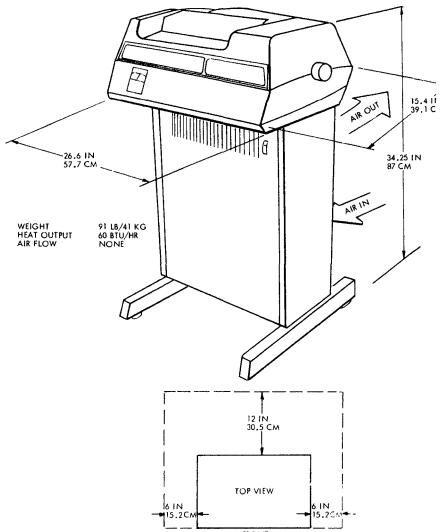
AG. PRINTER MODEL 3408



AH. STAND FOR MATRIX PRINTER MODEL 3412

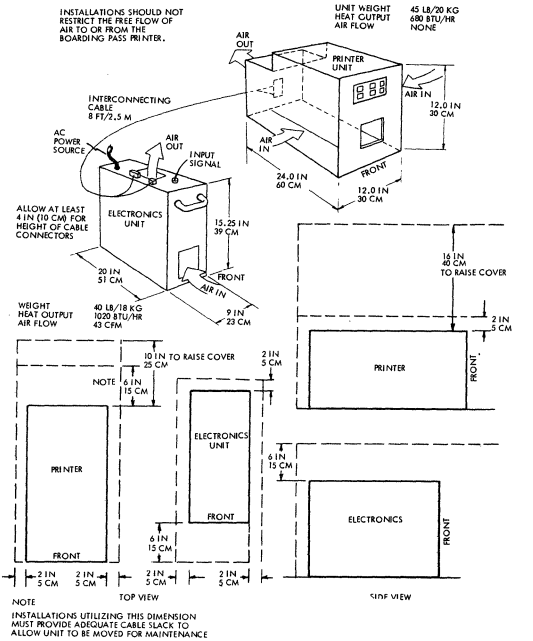


AI. PRINTER MODEL 3414

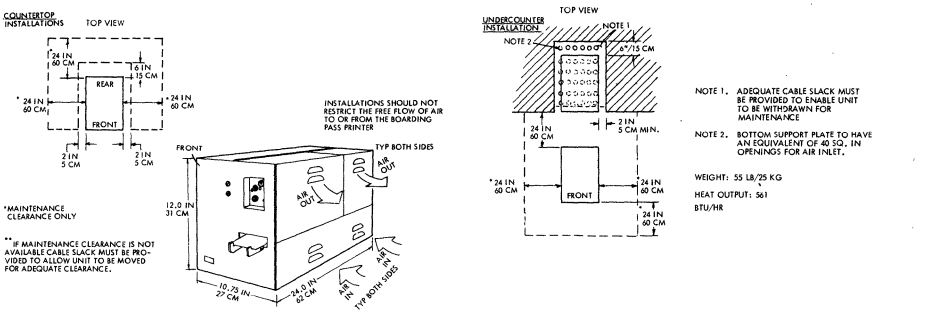


AJ. TICKET/SERIAL PRINTER MODEL 3414

Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 14 of 17)

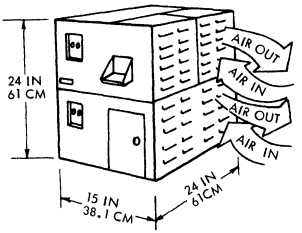


AK. BOARDING PASS PRINTER MODEL 3424

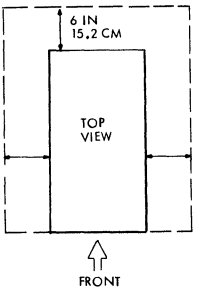


AL. BOARDING PASS PRINTER MODEL 3430

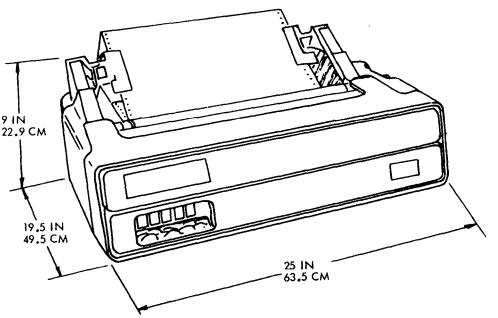
Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 15 of 17)



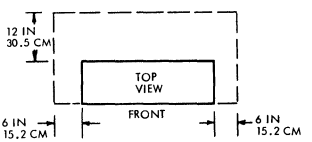
WEIGHT 90 LB/40.8 KG
HEAT OUTPUT 563 BTU/HR
AIR FLOW NONE



AM. TICKET PRINTER MODELS 3440 AND 3445

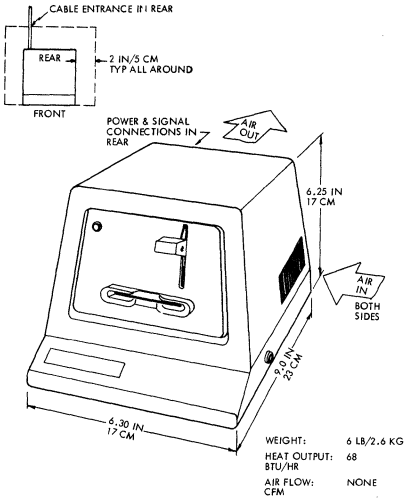


WEIGHT 75 LB/34 KG
HEAT OUTPUT 1280 BTU/HR
AIR FLOW NONE

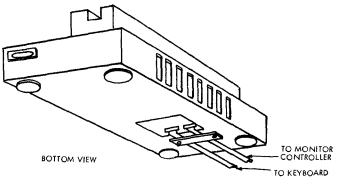


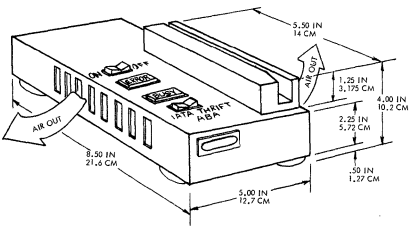
AN. PRINTER MODEL 3472

Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 16 of 17)

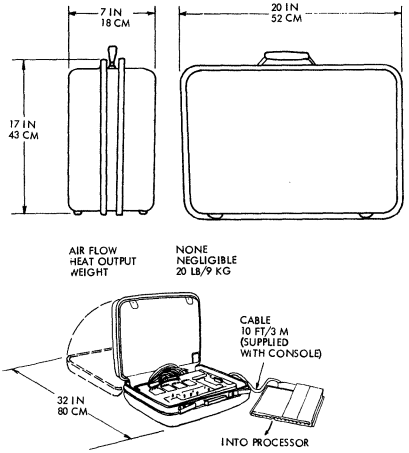


AO. BADGE READER MODEL 6140

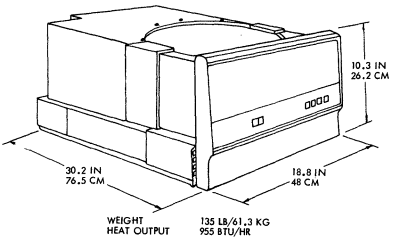




AP. MAGNETIC STRIPE CARD READER MODEL 6150-01



AQ. CUSTOMER ENGINEER CONSOLE MODEL 9101



AR. DIABLO DISC DRIVE WITHOUT CABINET

Figure 2-1. Cabling, Dimensions, Weight, Mounting Clearances, and Air Flow (Sheet 17 of 17)

2.6 System Cabling

The PTS-100 system cables are shown in Figure 2-2 and the cable specifications are listed in Table 2-3. The cable connections to the equipment are shown in Figure 2-1 and the connectors are shown in Figure 2-3.

If applicable, cables connecting peripheral devices and terminals to the PTS-100 processing system are supplied with the devices, factory precut and terminated.

It is imperative that no changes be made to the cabling installation, relative to grounding and placement, after the equipment has been accepted by the user.

Cathode ray tube (CRT) display devices can be susceptible to electrical transients that may be conducted into the displays on their signal cables. The RDS display design utilizes techniques that will alleviate the effect of transients. Nevertheless, it is desirable to take all reasonable precautions to reduce pickup of transients in the input/output signal cables. In extreme cases the Raytheon signal cables may have to be placed in conduits or shielded troughs to ensure adequate isolation.

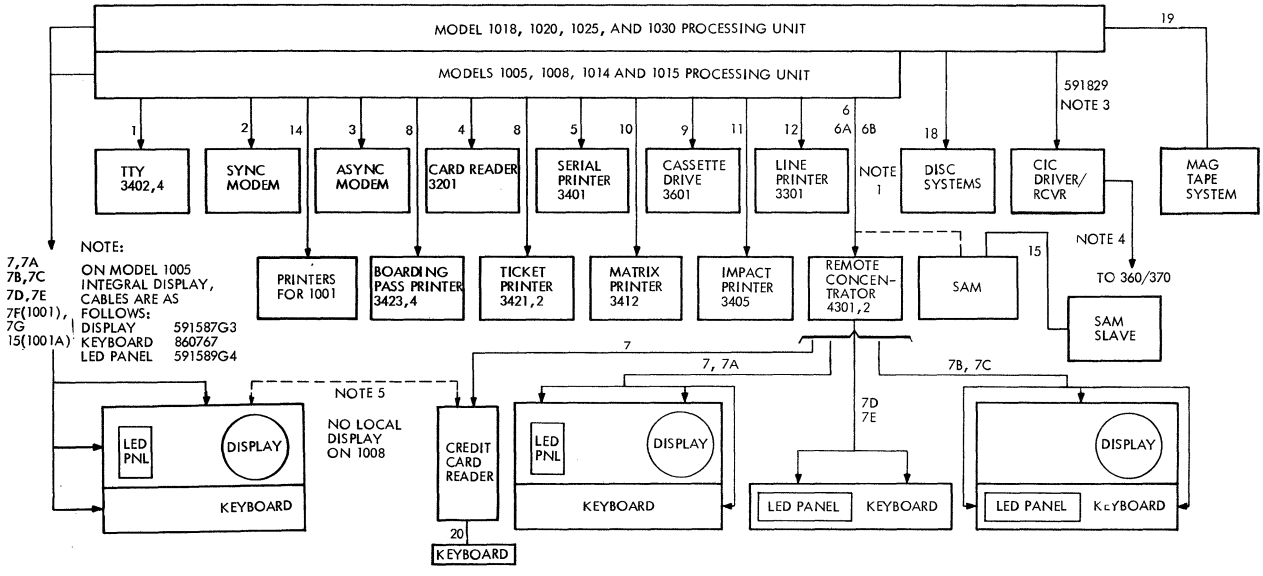
Every precaution should be taken to ensure that the installation of the equipment is far removed from industrial machinery and large power transformers. Signal cables must be kept separate from ac power telephone and teletype cables. However, where required, the signal cables may cross these cables, but the angle of crossing should be as close as possible to 90 degrees. The Raytheon signal cables and station power or telephone/teletype cables should be kept at least 12 inches apart. Closer separations are permitted for limited runs.

If the Raytheon signal cables are contained in a separate steel conduit and the other cables are contained in another similar conduit, a one inch separation will be satisfactory over any distance, provided the conduits are properly grounded.

Signal cables should be installed over the shortest possible route within these restrictions since noise pickup increases with distance.

2.7 Installation Procedure

a. Unpack equipment. Check the equipment against the Raytheon Sales Order Summary to see if the shipment is complete. If any item is missing inform Raytheon Data Systems immediately.



NOTES:

1. ONE OR TWO CABLES REQUIRED PER MONITOR CONTROLLER DEPENDING UPON MONITOR CONTROLLER TYPE AND SYSTEM REQUIREMENTS.
2. INTERNAL CABLE INCLUDED WITH DISC SYSTEM.
3. INTERNAL CABLE INCLUDED WITH CIC.
4. TWO CABLES REQUIRED.
5. CCR CONNECTS INTO MC KEYBOARD CHANNEL

Figure 2-2. PTS-100 Peripheral Cables

Table 2-3. PTS-100 System Cable Specifications

Cable	From (See Ref. For Conn.	To Figure Details)	Part Number of Precut Terminated Cable	Part Number of Field Termination Kit	Bulk Cable Type	Cable Size (Inches)	Cable Weight Per Foot (Ounces)	Max Allowable Pull (lbs)	Maximum Length (feet)	Maximum Length (inches)	Std Length (feet)	Std Length (meters)
1	Processing Unit (Fig 2-3, A)	TTY (Fig 2-3, D)	591584	593431 G1	594436-1 2 Twisted Shielded Pairs	0.30 Dia	0.5	20	4000	1200	25	7.5
2	Processing Unit (Fig 2-3, A)	Sync Modem (Fig 2-3, E)	590815		594435-2 12 Conductor	0.43 Dia	1.0	30	50	15	20	6
			SDLC 860889/ IOC 860952 1001 930600 RFI 932446 932447		594097-1 14 Conductor	0.45 Dia	1.0	30	50	15	20	6
3	Processing Unit (Fig 2-3, A)	Async Modem (Fig 2-3, E)	930840 RFI 932445		594097-1 14 Conductor	0.45 Dia	1.0	30	50	15	20	6
4	Processing Unit (Fig 2-3, B)	Card Reader (Fig 2-3, F)	591581		594443-1 19 Twisted Pairs	2.00 x 0.25 Flat Bonded	1.5	50	30	9	10	3
5	Processing Unit (Fig 2-3, A)	Serial Printer (Fig 2-3, E)	591582	591765 G1	594319-1 1 Twisted Shielded Pair	0.30 Dia	0.5	20	4000	1200	25	7.5
6	Processing Unit (Fig 2-3, A, T)	Remote Concentrator & SAM (Fig 2-3, A, T)	591586 Note 1 932398	591763 G1 RFI	594319-1 1 Twisted Shielded Pair	0.30 Dia	0.5	20	2000	600	--	--
6A	Processing Unit (Fig 2-3, A)	Remote Concentrator (Fig 2-3, A)	593349 Note 1	593406 G1	594818-1 1 Coax 1 Twisted Shielded Pair	0.5 Dia	1.5	35	4000	1200	--	--
6B	Processing Unit (Fig 2-3, V)	Coax Cable (Fig 2-3, V)	860673	--	RG62A/U	.25	0.5	20	10	3	10	3
	Coax Cable (Fig 2-3, U)	Remote Concentrator (Fig 2-3, U)	860672	--	RG62A/U	.25	0.5	20	10	3	10	3
	Coax Cable (Processor End) (Fig 2-3, W)	Coax Cable (Remote Concentrator or SAM End) (Fig 2-3, W)	860905	--	RG62A/U	.25	.05	20	5000	1500	--	
			860914 Note 3	--	594092	.28						

Table 2-3. PTS-100 System Cable Specifications (cont)

Cable	From (See Ref. For Conn. Details)	To Figure	Part Number of Precut Terminated Cable	Part Number of Field Termination Kit	Bulk Cable Type	Cable Size (Inches)	Cable Weight Per Foot (Ounces)	Max Allowable Pull (lbs)	Maximum Length (feet)	Maximum Length (inches)	Std Length (feet)	Std Length (meters)
6C	Internal Cable											
	Display Adapter	Monitor Controller	890906		594319-1 1 Twisted Shielded Pair	.30			100	30	6	1.8
	(Fig 2-3, T)	(Fig 2-3, T)										
7	Processing Unit or Remote Concentrator	Credit Card Reader Display LED Panel Keyboard	593348 Note 2	593404 G1	594814-1 1 Coax 5 Twisted Pairs 5 Twisted Pairs 5 Twisted Pairs	0.88 Dia	6.0	200	200	60	25	7.5
	(Fig 2-3, C)	(Fig 2-3, C)										
7A	Processing Unit or Remote Concentrator	Display LED Keyboard	593346 Note 2	593405 G1	594813-1 1 Coax 5 Twisted Pairs 5 Twisted Pairs 5 Twisted Pairs	0.75 Dia	4.0	100	75	23	25	7.5
	(Fig 2-3, C)	(Fig 2-3, C)										
7B	Processing Unit or Remote Concentrator	Display LED Panel Keyboard	593450 Note 2	593433 G1	594814-1 1 Coax 5 Twisted Pairs 5 Twisted Pairs 5 Twisted Pairs	0.88 Dia	6.0	200	200	60	25	7.5
	(Fig 2-3, C)	(Fig 2-3, C) For applications where LED panel is in keyboard										
7C	Processing Unit or Remote Concentrator	Display LED Panel Keyboard	860376 Note 2		594813-1 1 Coax 5 Twisted Pairs 5 Twisted Pairs 5 Twisted Pairs	0.75 Dia	4.0	100	75	23	25	7.5
	(Fig 2-3, C)	(Fig 2-3, C) For applications where LED panel is in keyboard										
7D	Processing Unit or Remote Concentrator	LED Panel Keyboard	593432 Note 2	593451 G1	594814-1 5 Twisted Pairs 5 Twisted Pairs	0.88 Dia	6.0	200	200	60	25	7.5
	(Fig 2-3, J)	(Fig 2-3, J) For split screen applications										
7E	Processing Unit or Remote Concentrator	LED Panel Keyboard	860377 Note 2		594813-1 5 Twisted Pairs 5 Twisted Pairs	0.75	4.0	100	75	23	25	7.5
	(Fig 2-3, J)	(Fig 2-3, J) For split screen applications										

Table 2-3. PTS-100 System Cable Specifications (cont)

Cable	From (See Ref. For Conn. Details)	To Figure	Part Number or Precut Terminated Cable	Part Number of Field Termination Kit	Bulk Cable Type	Cable Size (inches)	Cable Weight Per Foot (ounces)	Max Allowable Pull (lbs)	Maximum Length (feet)	Maximum Length (inches)	Std Length (feet)	Std Length (meters)
7F	Processing Unit 1001 (Fig 2-3, AA, Z)	Keyboard with LED Keyboard without LED	930603 930644		594813-2 Twisted Pair	0.75	4.0	100	10	3		
7G	Processing Unit or Remote Concentrator (Fig 2-3, C)	Display LED Panel Keyboard (Fig 2-3, C)	932451 RFI	--	864213-1 1 Coaxial 3/5 Twisted Pair Groups with overall shield and Drain-wire	.90	6.0	200	200	60	25	7.5
8	Processing Unit (Fig 2-3, A)	Boarding Pass Printer or Ticket Printer (Fig 2-3, G)	593366	593445 G1	594436-1 2 Twisted Shielded Pairs	0.3 Dia	0.5	20	4000	1200	25	7.5
9	Processing Unit (Fig 2-3, H)	Cassette Drive (Fig 2-3, I)	591583		594311-3 9 Twisted Pairs 2 Twisted Shielded Pairs	1.50 x 0.20 Flat Bonded	1.5	50	30	9	10	3
	Processing Unit (Fig 2-3, H)	Cassette Drive (Fig 2-3, I)	932452 RFI	--	864275-1 9 Twisted Pairs 2 Twisted Shielded Pairs with overall shield	.48	1.5	50	30	9	10	3
10	Processing Unit (Fig 2-3, A)	Matrix Printer (Fig 2-3, G)	593366	593445 G1	594436-1 2 Twisted Shielded Pairs	0.3 Dia	0.5	20	4000	1200	25	7.5
11	Processing Unit (Fig 2-3, A)	Impact Printer (Fig 2-3, K)	860268	860320 G1	594319-1 1 Twisted Shielded Pair	0.3 Dia	0.5	20	4000	1200	25	7.5
12	Processing Unit (Fig 2-3, B)	Line Printer (Fig 2-3, L)	861067		531420-309 Twisted Pair	0.5 Dia	1.5	50	50	15	25	7.5
13	CIC Driver Receiver (Fig 2-3, M)	IBM 360/370 (Fig 2-3, M)	594564 2 Cables Required	Refer to IBM Manual		1.10 Dia	8.0	200	As Specified by IBM		20	6

Table 2-3. PTS-100 System Cable Specifications (cont)

Cable	From (See Ref. For Conn. Figure Details)	To	Part Number or Precut Terminated Cable	Part Number of Field Termination Kit	Bulk Cable Type	Cable Size (inches)	Cable Weight Per Foot (ounces)	Max Allowable Pull (lbs)	Maximum Length (feet)	Maximum Length (inches)	Std Length (feet)	Std Length (meters)
14	Processing Unit 1001	Printers Current Loop	930601		594436-1 2 Twisted Pairs	0.3 Dia	0.5	20	200	60	25	7.5
		Extel	930908		594319-1 1 Twisted Pair	0.3 Dia	0.5	20	4000	1200	25	7.5
	(Fig 2-3, X, Y, AB)	RS-232	930602		594097-1	0.45 Dia	1.0	30	50	15	20	6
15	SAM or 1001A (Fig 2-3, W) (See Figure 4-11)	SAM Slave	860914 U/L		594092-1 Coax	.28			200	60		
16	Badge Reader (Fig 2-3, A)	Keyboard (Fig 2-3, A)	593416	--	594158-1	.46 x .20 Flat Bonded	1.0	20	4	1.3	4	1.2
17	(Fig 2-3, A)	Printer Cont	932595	--	15 Twisted Pairs # 26 AWG	.50	1.0	20	10	3	10	3
18	Processing Unit	Storage Module Drive	864147-4 (80 Mb, Daisy)	--	Flat Cable	3.0 x .15	1.2	20	20	6	20	6
			864208-4 (300 Mb, Daisy)		Flat Cable						50	15
			864147-5 (80 Mb, Star)		Flat Cable						20	6
			864208-5 (300 Mb, Star)		Flat Cable						50	15
			930082 (Fig 2-3, AD)		Flat Cable						8	2.4
		Diablo 44B Drive	930837 (Fig 2-3, AF)	--	594793-1	2.25 x .045					15	4.5
	Disc Drive #1	Disc Drive #2	864168-3 (Daisy Chain)	--							5	1.5
	Processing Unit	Diablo 30 (Controller in Separate Cabinet)	591829	--					20	6	10	3
	Disc Adapter	Disc Drive	860935G10 (Up to 4dr)	--							10	3
			860935G15 (Up to 8dr)								15	4.5
	Disc Drive #1	Disc Drive #2	594008-006	--							7	2.1

Table 2-3. PTS-100 System Cable Specifications (cont)

Cable	From (See Ref. For Conn.	To Figure Details)	Part Number of Precut Terminated Cable	Part Number of Field Termination Kit	Bulk Cable Type	Cable Size (inches)	Cable Weight Per Foot (ounces)	Max Allowable Pull (lbs)	Maximum Length (feet)	Maximum Length (inches)	Std Length (feet)	Std Length (meters)
19	Processing Unit	Magnetic Tape	932238 (Fig 2-3, AC)	--	531420-209						5.5	1.66
			594518-7								7	2.1
		(See Fig 3-98)	864227-4 (2 Units)								4	1.2
			864227-6 (3 Units)								6	1.8
20	Keyboard	Credit Card Reader	930520G3 (Fig 2-3, AE)	--	594813-2 5 Twisted Pair #22 AWG	.74			Combined Length of Cables 7 & 20 Not to Exceed 200 Feet		3	.9
	The following cables are used when interfacing with the referenced IBM system cables											
	Processing Unit (Fig 2-3, A)	IBM 3270 Cable (Fig 2-3, N)	860222		594319-1 1 Twisted Shielded Pair	.30	0.5	20	10	3	10	3
	IBM 3270 Cable (Fig 2-3, N)	Remote Concentrator (Fig 2-3, A)	860223		594319-1 1 Twisted Shielded Pair	.30	0.5	20	10	3	10	3
	Processing Unit (Fig 2-3, A)	IBM 2260 Cable #5213814 (Fig 2-3, O)	593493		594436-1 2 Twisted Shielded Pairs	.30	0.5	20	10	3	10	3
	IBM 2848 Cable #5213814 (Fig 2-3, P)	Remote Concentrator (Fig 2-3, A)	593494		594436-1 2 Twisted Shielded Pairs	.30 Dia	0.5	20	10	3	10	3
	Processing Unit (Fig 2-3, A)	IBM 2848 Cable #5213821 (Fig 2-3, Q)	591841		594319-1 1 Twisted Shielded Pair	.30	0.5	20	10	3	10	3
	IBM 2848 Cable #5213821 (Fig 2-3, R)	Serial Printer (Fig 2-3, E)	591840		594319-1 1 Twisted Shielded Pair	.30	0.5	20	10	3	10	3
	Processing Unit (Fig 2-3, A)	IBM 2948 Cable (Fig 2-3, S)	591838		594436-1 2 Twisted Shielded Pairs	.30	0.5	20	10	3	10	3
	IBM 2948 Cable (Fig 2-3, S)	Remote Concentrator (Fig 2-3, E)	591839		594436-1 2 Twisted Shielded Pairs	.30	0.5	20	10	3	10	3

NOTES

1. One or two cables per monitor controller depending upon monitor controller type and system requirements. Minimum cable bend radius = cable dia. x 10. Also see Figure 2-4 for dual mode cable lengths and restrictions. When M.C. is in processing unit use 593349-G6.
2. See Figure 2-4 for connections.
3. Two umbilical cables (860672 & 860673) are also used (only one for SAM).

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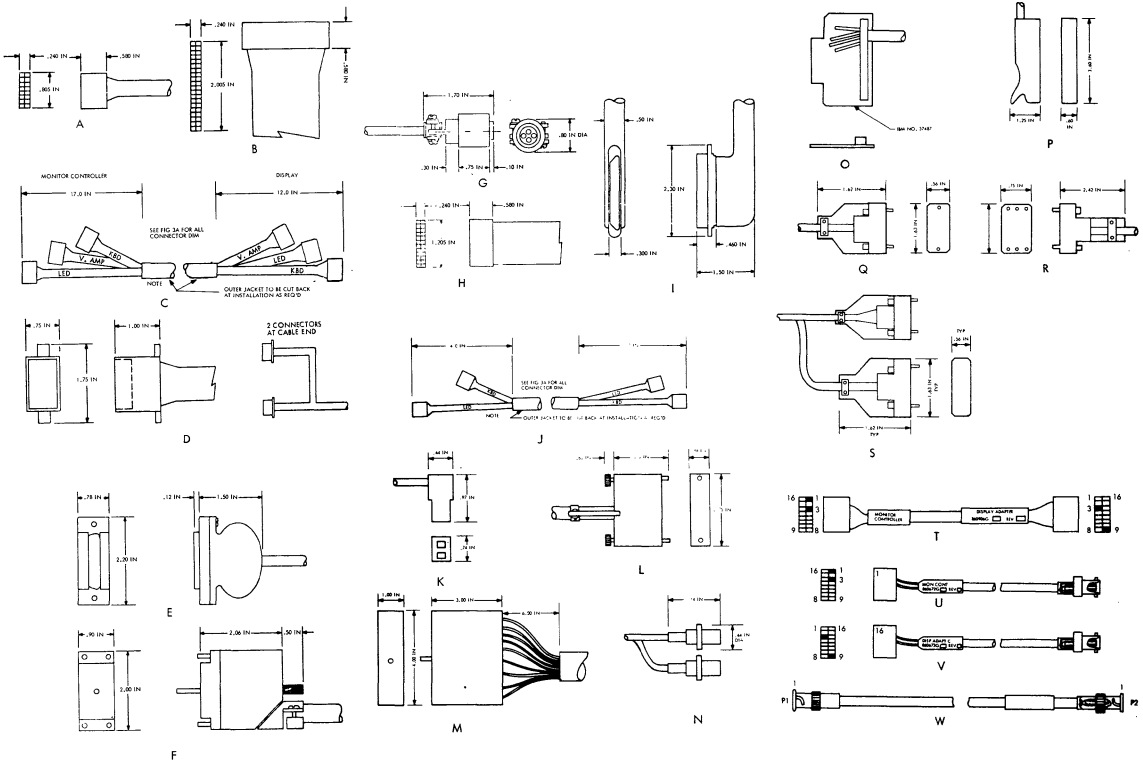
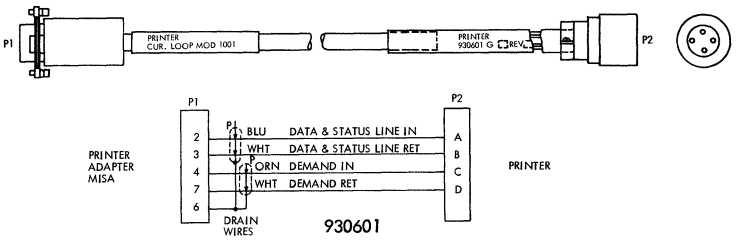


Figure 2-3. PTS-100 Cable Connectors and Diagrams (Sheet 1 of 6)



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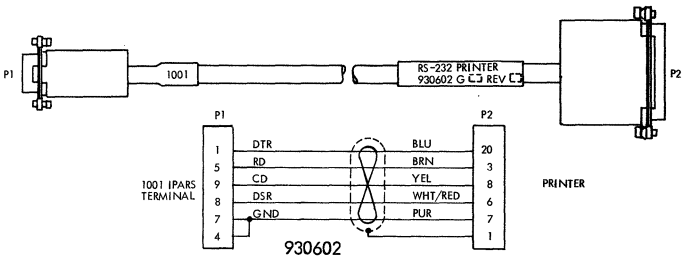

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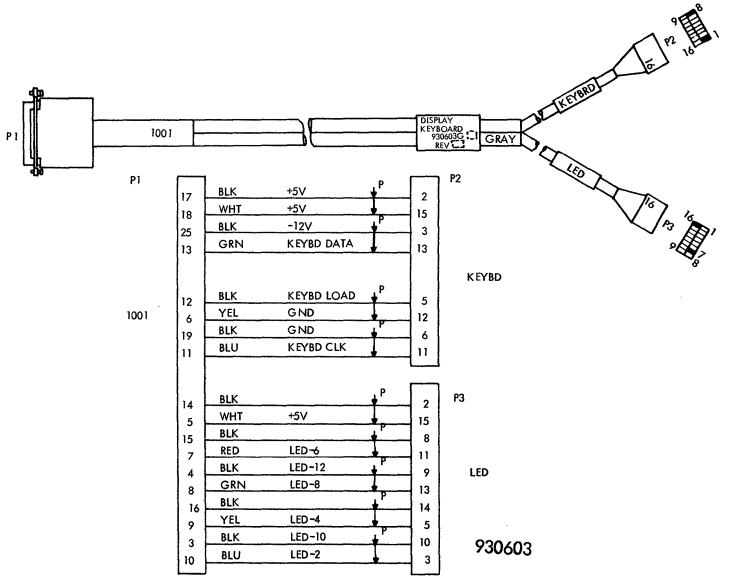

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Figure 2-3. PTS-100 Cable Connectors and Diagrams (Sheet 2 of 6)

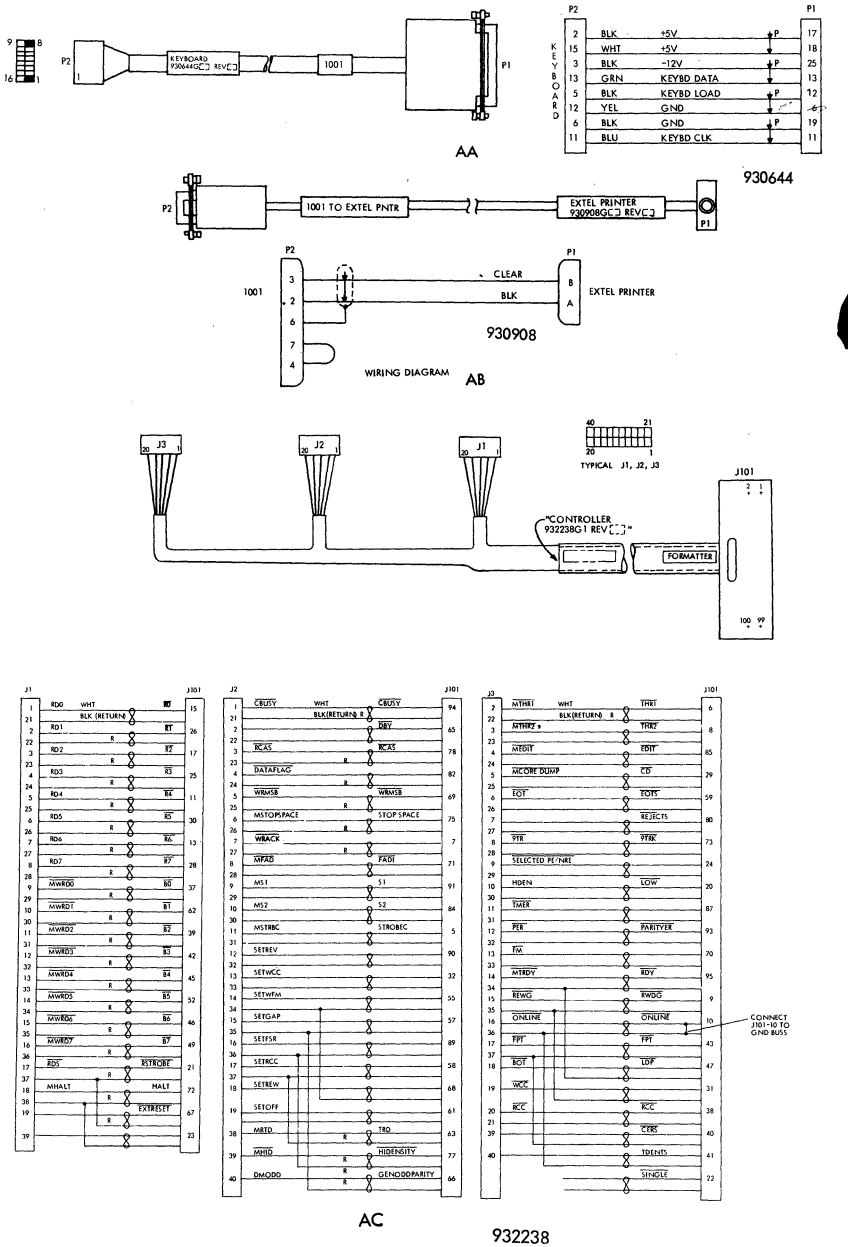


Figure 2-3. PTS-100 Cable Connectors and Diagrams (Sheet 3 of 6)

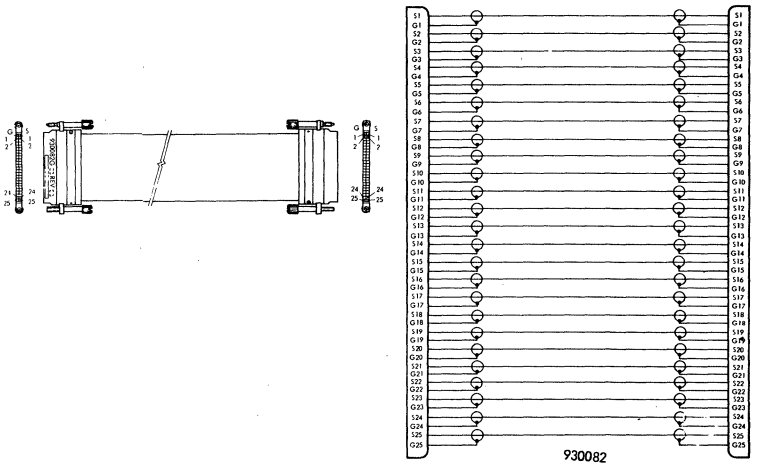


Figure 2-3. PTS-100 Cable Connectors and Diagrams (Sheet 4 of 6)

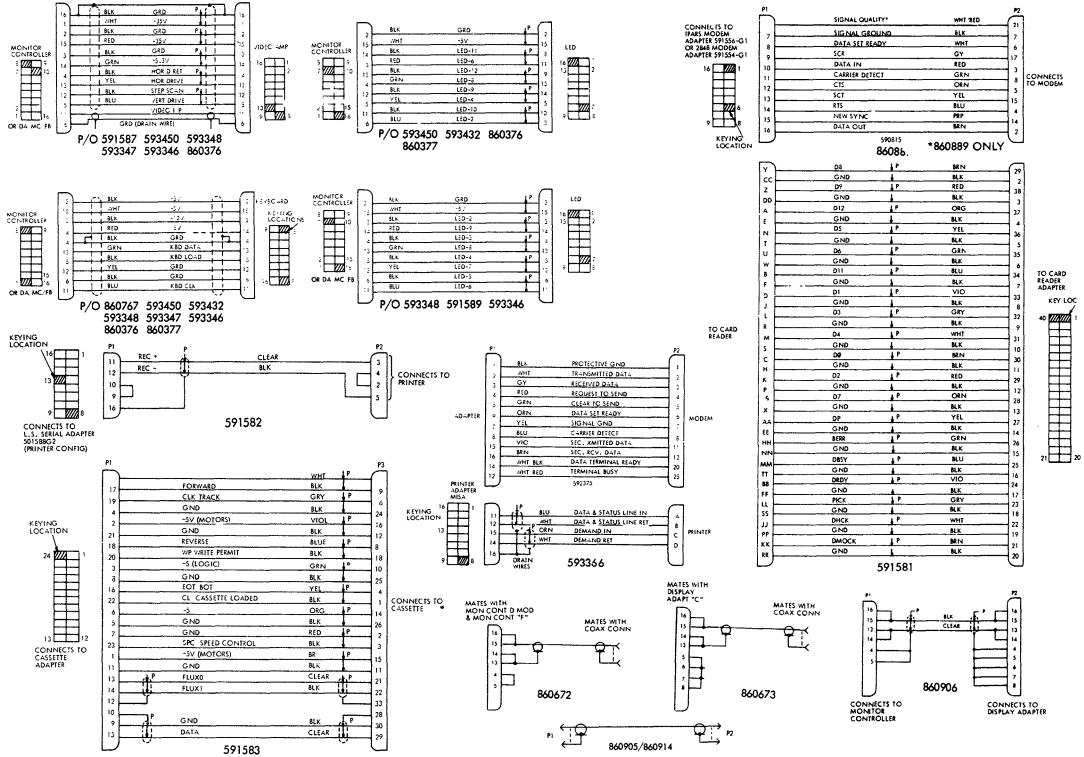


Figure 2-3. PTS-100 Cable Connectors and Diagrams (Sheet 5 of 6)

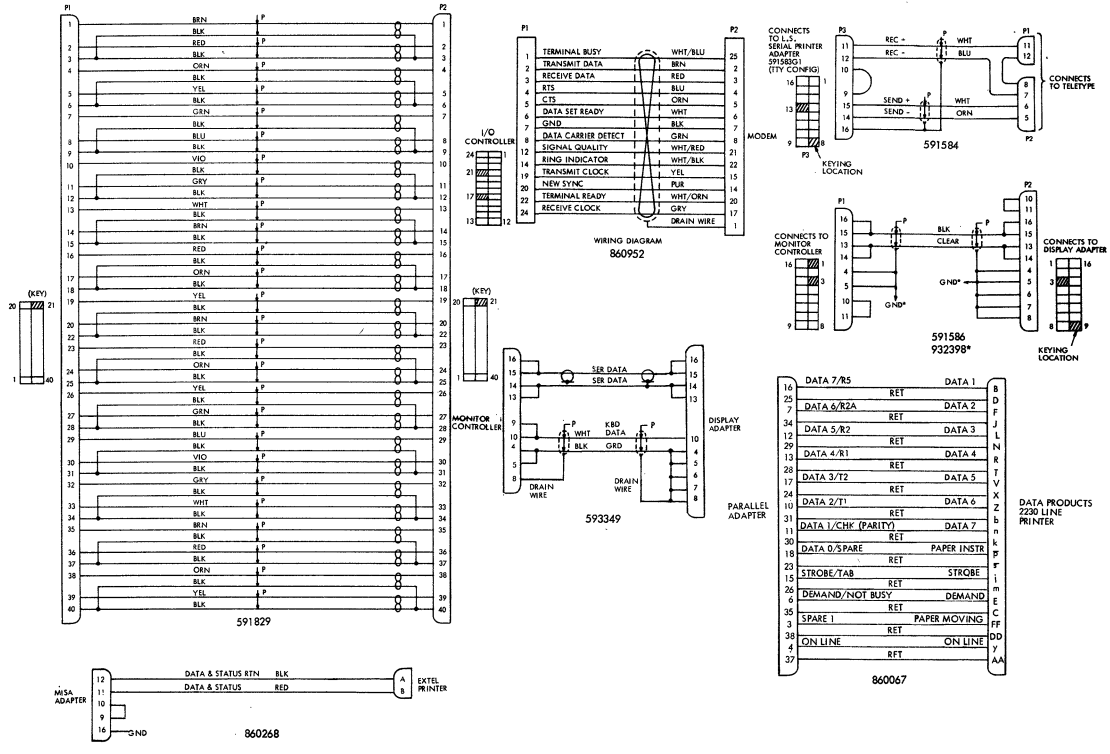
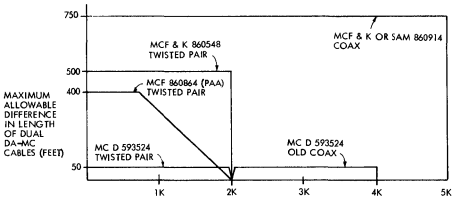


Figure 2-3. PTS-100 Cable Connectors and Diagrams (Sheet 6 of 6)



MC D&F DUAL MODE ALLOWABLE DA-MC CABLE LENGTH DIFFERENCES

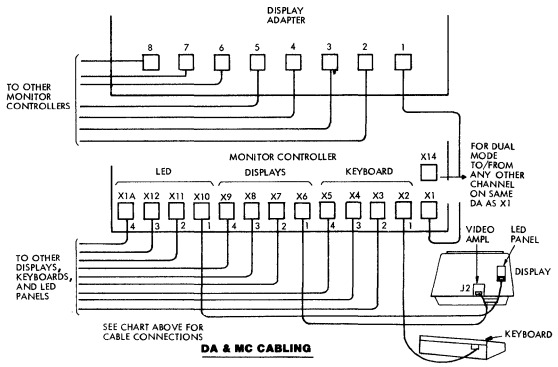
DISPLAY FORMAT		MC MODEL	MONITOR CONTROLLER KEYBOARD X2	X3	X4	X5	DISPLAY X6	X7	X8	X9	LED X10	X11	X12	X13	DA INPUT
SPLIT* SCREEN	1920	ALL	1	2			1				1	2			
	960	ALL	1A	2A	1B	2B	1		2		1A	2A	1B	2B	
STD	40X12	ALL	1	2	3	4	1	2	3	4	1	2	3	4	X1
	40X24	B-16, D, F, K	1	2			1	2			1	2			
	64X15	ALL EXC D	1		2		1		2		1		2		
	64X16	B-16 & F	1	2			1	2			1	2			
	80X12	ALL	1		2		1		2		1		2		
	64X30	ALL EXC D	1				1				1				
	80X24	ALL	1				1				1				
DUAL ** MODE	64X15	F, K	1	2	3	4	1	2	3	4	1	2	3	4	X1 & X14
	64X16	F	(X1)	(X14)	(X1)	(X14)	(X1)	(X14)	(X1)	(X14)	(X1)	(X14)	(X1)	(X19)	
	80X12	D , F, K													
	64X30	F, K	1	2			1	2			1	2			
	80X24	D , F, K	(X1)	(X14)			(X1)	(X14)			(X1)	(X14)			

1-1st, 2-2nd, 3-3rd, 4-4th DISPLAY, KYBD OR LED PNL

** IN DUAL MODE KEEP DIFFERENCE BETWEEN THE TWO CABLES TO 750 FT FOR COAX AND 500 FT FOR TWISTED PAIR

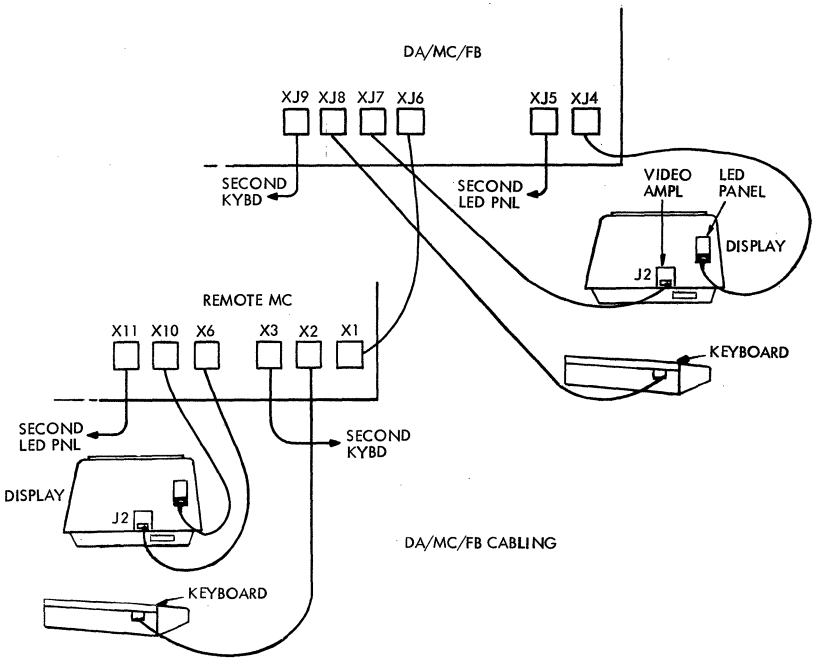
FOR 1920 CHARACTER SPLIT SCREENS, CONNECT CABLE 593458G1 BETWEEN X7 AND X12. FOR 960 CHARACTER SPLIT SCREENS, CONNECT CABLE 860675 BETWEEN X7 AND X9.

MC TO DISPLAY, KEYBOARD AND LED PANEL CABLING MATRIX



DA & MC CABLING

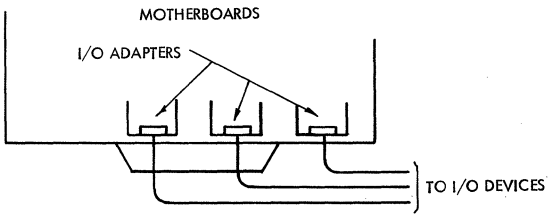
Figure 2-4. Cabling to DA/MC/FB, Display Adapter, Monitor Controller, and Motherboards (Sheet 1 of 2)



DA/MC/FB CABLING

DISPLAY SIZE	DA/MC/FB						REMOTE MC				
	KYBD2 XJ9	KYBD1 XJ8	DISPLAY XJ7	DA OUT XJ6	LED2 XJ5	LED1 XJ4	LED2 X11	LED1 X10	DISPLAY X6	KYBD2 X3	KYBD1 X1
1920 CH	1B	1A	1	TO MC X1	1B	1A	2B	2A	2	2B	2A
960 CH OR 480 CH	–	1	1		–	1	–	2	2	–	2

DA/MC/FB AND REMOTE MC TO DISPLAY, KEYBOARD AND LED PANEL CABLING MATRIX



I/O DEVICE TO ADAPTER CABLING

Figure 2-4. Cabling to DA/MC/FB, Display Adapter, Monitor Controller, and Motherboards (Sheet 2 of 2)

b. Visually inspect the equipment for possible damage incurred during shipment. Look for marred surface finish, loose or broken wires and hardware, and loose modules or subassemblies. Check the PC boards for cracks, loose or broken components, loose cables (motherboards), etc. Inspect cables for broken wires and cracked or broken connectors.

Remove top cover from power supply(s) and visually inspect the components and wiring. Replace top cover.

Remove the top covers from the displays and keyboards and visually inspect the components and wiring. Replace covers.

Immediately inform Raytheon Data Systems of any damage.

c. Move the equipment to its intended positions. Figure 2-1 shows the necessary maintenance, air flow, and cabling clearances.

d. Prepare the peripheral equipment for operation using the installation procedures given in the Manufacturers manuals.

e. On PTS-100 Models 1015, and 4301, install power supply chassis in the cabinet(s) (when packed separately) using the procedure below. (When the cabinets are shipped with power supplies mounted, check power supply wiring and mountings.)

1. Open cabinet front door and remove four panel-retaining screws from cabinet rear panel. Remove rear cabinet panel.

2. Slide power supply chassis into top front of cabinet.

3. Fasten power supply to cabinet chassis using four screws in front and four screws in rear of power supply.

4. Connect wires from rear of cabinet to terminal board(s) on rear of power supply. Wires are marked with terminal board and terminal numbers.

5. Connect output cable from front of power supply to spade lugs on printed wiring board just below left side of power supply. Connect each wire to its associated lug.

CAUTION

Double check connections to prevent damage to equipment

Before installing the printed circuit boards check the power supply voltages. Apply power to the cabinet by connecting the cabinet ac input cable to an ac power source, and turn the cabinet power switch on. Measure each dc output voltage. They all must be within ±3% of the marked values. Adjust the voltages as required (refer to Chapter 4 for the procedure). Disconnect power.

f. Inspect the patch plugs, jumpers, switches and outboard plug-in modules on each plug-in printed circuit board. Make sure they are set according to the associated diagram given in Figures 2-5 through 2-21, Table 2-4, and the Raytheon Installation Documentation Package.

g. Make any wiring modifications to the 1020/1030 backplane to accommodate additional monitor controller boards. The wiring is shown in Figures 2-22 and 2-23.

h. Remove processing unit cabinet back cover as in step e and install each plug-in printed circuit board in the cabinet in the locations shown in the Raytheon Sales Order Summary. Slide each board (component side up) into its assigned board slot from the rear of the cabinet. Use Insertion/Extraction tool 591800 to insert the boards. Carefully seat the board (on the old model boards close the board retaining locks). Make sure that the I/O device adapters on the motherboards are installed properly before inserting the motherboards. The adapters are mounted on top of the motherboards.

WARNING

Do not insert any other boards into slots wired for monitor controllers or the ±35 vdc will damage the boards.

NOTE

This note applies to steps i through m. Exercise caution when laying cables. Don't strain the cables when pulling them. Protect the connectors at all times. Don't pull cables by the connectors. Don't lay cables on suspended ceilings. Observe local codes. Label cables before laying. Clamp cables with care.

i. Connect the signal cables from the I/O devices (refer to Table 2-3) to their associated I/O device adapters. The cables plug into the bottom rear of the I/O device adapters. Route the cables into the rack, up through the right side cable duct and out through the slots in the duct to the connectors on the printed circuit boards. Remove the plastic cable duct cover to install the cables.

j. Refer to Section 2.8 if coax cable adapters are used. If not connect cables from the channel 1-8 connectors on the Display Adapter board(s) to connectors X1 on the Monitor Controller boards (see Figure 2-4). For Monitor Controllers mounted in remote concentrators route the cables as in step i. Refer to the display connections and memory assignments diagram on the feature board chip switch setting procedures (Appendix A) to determine the correct monitor controller display adapter and display channel connections. Keep in mind that the displays are assigned from the uppermost memory address down.

k. Connect the cables from the monitor controller boards (Figure 2-4) to the display (J2 on the video amplifiers), the display LED panels, and the keyboards. Route the cables as in step j, and secure the cables to the displays and keyboards using the cable clamps at the cable entrances and at the cable connectors. After stripping back the outside cable jacket approximately 3 feet, clamp the video amplifier cable near the point where the cable branches; this provides strain relief for the whole cable.

l. Display hardware and connectors are sometime loosened during shipment. After removing the display housing, the following should be checked for security:

1. The four screws which mount the chassis to the base.

2. Connectors, particularly the interconnection of the video and H. & V. assemblies, and the connector at the top of the H. & V. assembly.

3. Yoke, to ensure that it has not loosened on the CRT neck.

m. When a CIC is used, insert the CIC plug-in printed circuit boards as shown in the Sales Order Summary. Check that the interrupt and 360 device address patch plugs are wired correctly before installing the boards (see Figure 2-6). Interconnect the two boards as shown in Figures 2-16 and 3-73. Connect the cables from the 360 to the connectors on the separate driver receiver chassis as shown. Always connect IBM light colored cable connectors to dark colored receptacles and vice versa. Install terminators in J5 and J7 if tag out and bus out cables are not used.

n. When a disc or CIC is used, insert the controller printed circuit boards as shown in the Sales Order Summary. Check that the interrupt and address patch plugs are wired correctly (Figures 2-6 and 2-9) before installing the boards. Connect and cable the boards as shown in Figure 3-67 (DISC) or Figure 3-72 (CIC). For the disc controller, connect the daisy chain cables from the plug(s) on the disc controller chassis to the disc drives. Install a terminator on the last drive in the daisy chain. For the CIC connect BUS and TAG connectors J5 and J7 to the next controller or install terminators.

o. Connect the cabinet and peripheral device ac power cables to a main power source, double check cabling and printed circuit board seating. If the unit uses SW2000/A, install and check out using FIB PO483 and the procedure in Section 4.4.5 of this manual. Turn on the PTS-100 system using the procedures in the Raytheon PTS-100 Operator Manual, Raytheon document 44-7645.

p. Check power supply dc output voltages and readjust as required.

q. Display Checks

1. Processors or remote concentrators to which displays are attached should be energized first with all displays turned off. Displays should then be turned on one at a time to identify problem displays.

2. If turn on is done with housing in place and display does not come up, check to ensure interlock is adjusted so that it is activated by the housing.

3. Refer to trouble shooting procedure for fault isolation if monitor does not come on (Figure 4-8). Lack of CRT filament voltage usually indicates either a fault on the H. & V. board (SAM analog board) or no ±35v input.

4. Let monitor run for several hours if possible before attempting quality alignments.

r. 4103 SAM Display Alignments — See Section 4.12.5.

s. 4101 Display Alignments — A complete display alignment procedure is given in Section 4.4.2; however, only the following is normally necessary.

1. Turn brightness control fully clockwise.
2. Adjust prebrightness control (R25 on video amplifier) until background sweep is visible.
3. Load emulator tape and fill screen with data.
4. Adjust horizontal shift control (R14 on H. & V. amplifier) until data pattern is centered within raster.

NOTE

This adjustment may change whenever monitor is attached to a different cable or connected to a different monitor controller port.

5. Decrease prebrightness until background sweep is barely visible.
6. Adjust vertical linearity (R38 on H. & V. amplifier) until character height is uniform on all rows.

7. Set contrast control (R6 on video amplifier) for sufficient brightness. On 3270 systems with dual brightness allow for low brightness level.

8. Adjust static and/or dynamic focus controls as required. These two controls interact so that some repetition is usually necessary. Adjust static control (R51 on video amplifier) for optimum spot size at about 1/4 and 3/4 points of the middle character line. Then adjust dynamic correction (R12) for corners and center. Always ensure that upper left corner of screen has good presentation.

9. If character rows are not horizontal, rotate yoke as necessary. If barrel distortion (convex curvature of raster outline) is evident, yoke may have slipped back from flare of tube. Make sure clamp is tight at completion.

10. If any portion of presentation is obscured by bezel, rotate centering tabs on rear of yoke.

2.8 Coaxial Cable Adapter Installation

The coaxial cable adapter is an option that permits monitor controllers (model F) to be connected to the display adapters (model C) using RG62A/U coaxial cables instead of the normal shielded twisted pair. Coaxial cable runs of up to 4000 feet are permitted. The coax adapter consists of four piggyback plug in circuit boards. Three of the boards — two high speed receiver modules (860631) and a control module (860634) — plug into the display adapters (J9, J10, and J11, respectively); the fourth, a high speed transmitter module (860635), plugs into the monitor controllers (J15).

When any DA-MC run uses RG62A/U all display adapters and monitor controllers must have the cable adapter modules installed. The only exception to this is when a display adapter, display adapters, or part of a display adapter is used for memory refresh only. In this case, the high speed receiver module or modules associated with that portion of memory does not have to be installed. The receiver module nearest the channel number 1 connector is for channels 1, 3, 5, and 7; the other receiver module is for channels 2, 4, 6, and 8.

When coax is used to interconnect the display adapters and monitor controllers coax-to-berg transition cables are used, to interface the coaxial cables with the berg connectors. The transition cable for the display adapter is part no. 860673, and that for the monitor controller is part no. 860672.

Table 2-4. IOC, DA/MC/FB and FB 'B' Outboard Module PROM Locations

PROM Location	G8	G7	G6	G5	G4	G3	G2	G1	PROM Part No.
U8			-	-	-	1	-	-	A860518-8B
U4			-	-	-	1	-	-	A860418-7B
U7			-	-	-	1	-	-	A860418-6B
U3			-	-	-	1	-	-	A860418-5B
U6			-	-	-	1	-	-	A860418-4B
U2			-	-	-	1	-	-	A860418-3B
U5			-	-	-	1	-	-	A860418-2B
U1			-	-	-	1	-	-	A860418-1B
U8			-	-	-	-	1	-	A591810-8A
U4			-	-	-	-	1	-	A591810-7A
U7			-	-	-	-	1	-	A591810-6A
U3			-	-	-	-	1	-	A591810-5A
U6			-	-	-	-	1	-	A591810-4A
U2			-	-	-	-	1	-	A591810-3A
U5			-	-	-	-	1	-	A591810-2A
U1			-	-	-	-	1	-	A591810-1A
U8			-	-	-	-	-	1	A592646-8C
U4			-	-	-	-	-	1	A592646-7C
U7			-	-	-	-	-	1	A592646-6C
U3			-	-	-	-	-	1	A592646-5C
U6			-	-	-	-	-	1	A592646-4C
U2			-	-	-	-	-	1	A592646-3C
U5			-	-	-	-	-	1	A592646-2C
U1			-	-	-	-	-	1	A592646-1C
U8			1	-	-	-	-	-	A860808-8A
U7			1	-	-	-	-	-	A860808-7A
U6			1	-	-	-	-	-	A860808-6A
U5			1	-	-	-	-	-	A860808-5A
U4			1	-	-	-	-	-	A860808-4A
U3			1	-	-	-	-	-	A860808-3A
U2			1	-	-	-	-	-	A860808-2A
U1			1	-	-	-	-	-	A860808-1A
U8			-	1	-	-	-	-	A860806-8A
U6			-	1	-	-	-	-	A860806-6A
U4			-	1	-	-	-	-	A860806-4A
U2			-	1	-	-	-	-	A860806-2A
U7			-	1	-	-	-	-	A860805-7A
U5			-	1	-	-	-	-	A860805-5A
U3			-	1	-	-	-	-	A860805-3A
U1			-	1	-	-	-	-	A860805-1A
U7			-	-	1	-	-	-	A860657-7A
U5			-	-	1	-	-	-	A860657-5A
U3			-	-	1	-	-	-	A860657-3A
U1			-	-	1	-	-	-	A860657-1A

G1 = 2848/2260 Emulator RPL
G2 = Midwest RPL & Dump RPL
G3 = TWA RPL
G4 = Disc IPL
G5 = IOC ROM, IPARS
G6 = IOC ROM, 3270 EBCDIC

SYNCHRONOUS - ASYNCHRONOUS PATCH*

WIREWRAP BOARDS (WW) - G7
PRINTED CIRCUIT BOARDS (PC) - E5

GPCA CHANNEL NO.	PATCH PLUGPINS CONNECTED TOGETHER	
	ASYNC	SYNC
0	7-5	7-4
1	8-5	8-4
2	9-5	9-4
3	10-5	10-4

NOTE: FOR ALL CHAN ASYNC OPERATION INSERT PATCH 593192G121 INTO LOC: WW-G7; PC-E5 AND INSERT PATCH 593192G122 INTO LOCATIONS: WW-D15 & D18; PC-B12 & C7.

STOP BIT (ISR BIT 6) PATCH*

WW BOARDS - G7
PC BOARDS - E5

GPCA CHANNEL NO.	TWO STOP BITS	ONE STOP BIT
0	1-5	1-4
1	2-5	2-4
2	3-5	3-4
3	6-5	6-4

NOTE: PATCH 593192G121 IS FOR TWO STOP BITS ON ALL CHANNELS (SEE ABOVE)

FULL DUPLEX/HALF DUPLEX PATCHES*

FOR CHAN	MODE HALF DUPLEX FULL DUPLEX	INSERT PATCH* 593192	INTO LOCATIONS PC BOARD	INTO LOCATIONS WW BOARD
0,1,2 & 3	HD	G115	B5, A14	A12, B17
		G114	A6, A13	B16, B19
0 & 1	HD	G115	B5, A13	A12, B16
2 & 3	FD	G114	A6, A14	B19, B17
0 & 1	FD	G115	A6, A14	B19, B17
2 & 3	HD	G114	B5, A13	A12, A16
0,1,2 & 3	FD	G114	B5, A14	A12, B17
		G115	A6, A13	B19, B16

MUX INTERRUPT PATCHES — MUX INTERRUPT PATCHES (THESE PATCHES ASSIGN THE GPCA CHAN REQUEST, ENABLE, AND ACKNOWLEDGE SIGNALS TO A MUX PORT.

ACKNOWLEDGE: WW BOARD N9, PC BOARD N9 — ENABLE: WW BOARD N8, PC BOARD M11 — REQUEST: WW BOARD N13, PC BOARD N13

CONNECT PINS OF N9, N8/M11 AS INDICATED FOR DESIRED GPCA CHAN/MUX PORT CONNECTION

FOR GPCA CHAN NO.	MUX PORT NO. 0	1	2	3	4	5	6	7
0	9-8	9-7	9-6	9-5	9-4	9-3	9-2	9-1
1	10-8	10-7	10-6	10-5	10-4	10-3	10-2	10-1
2	11-8	11-7	11-6	11-5	11-4	11-3	11-2	11-1
3	12-8	12-7	12-6	12-5	12-4	12-3	12-2	12-1

CONNECT PINS OF N13 AS INDICATED FOR DESIRED GPCA CHAN/MUX PORT CONNECTION

FOR GPCA CHAN NO.	MUX PORT NO. 0	1	2	3	4	5	6	7
0	1-16	1-15	1-14	1-13	1-12	1-11	1-10	1-9
1	2-16	2-15	2-14	2-13	2-12	2-11	2-10	2-9
2	3-16	3-15	3-14	3-13	3-12	3-11	3-10	3-9
3	4-16	4-15	4-14	4-13	4-12	4-11	4-10	4-9

BAUD RATE PATCHES

WW BOARDS - M8
PC BOARDS - L7

FOR BAUD RATE:	CONNECT PINS 15 AND 16 TO PIN:
4800	1
2400	2
1200	3
600	4
300	5
150	6
**NONSTANDARD	7
75	8

**NONSTANDARD RATES — M1/K1 IS PATCHED FOR THE NONSTANDARD BAUD RATE

WW BOARDS - K1
PC BOARDS - M1

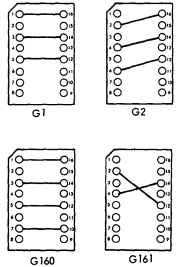
FOR BAUD RATE	ALSO CONNECT PINS
110 (ONLY NONSTD RATE PRESENTLY AVAILABLE)	1-5-12-8 TOGETHER AND CONNECT ALL OTHER PINS BUT 15, 16 TOGETHER

*SEE FIGURE 2-24 FOR PATCH PLUG WIRING

GPCA's 593469, 593579

Figure 2-5. GPCA Patching (Sheet 1 of 2)

FULL DUPLEX/HALF DUPLEX PATCHES			
FOR GPCA PORT	MODE HALF DUPLEX FULL DUPLEX	INSERT PATCH 593192	INTO LOCATIONS
0,1,2 & 3	HD	G1	B2,A14
		G2	A4,A12
0 & 1	HD	G1	B2,A12
2 & 3	FD	G2	A4,A14
0 & 1	FD	G1	A4,A14
2 & 3	HD	G2	B2,A12
0,1,2 & 3	FD	G2	B2,A14
		G1	A4,A12



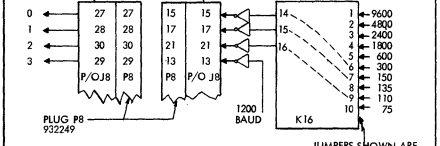
BAUD RATE SELECTION

TO SELECT THE BAUD RATE FOR A PORT.

JUMPER THE ASSOCIATED PIN ON P8 TO THE OTHER PIN ON P8 (15, 17, 21, 13) THAT HAS THE DESIRED CLOCK.

THE CLOCKS TO J8-15, 17 & 21 ARE SET ON PATCH K-16. THE 1200 BAUD CLOCK IS HARDWIRED TO J8-13.

MAKE THE JUMPERS ON PATCH K16 TO CONNECT THE DESIRED FREQUENCY(S) TO J8-15, 17 & 21.



NOTE

EACH PORT CAN BE CONNECTED TO ANY BAUD RATE CLOCK AND ALL PORTS CAN USE THE SAME BAUD RATE. MAKE CLOCK DISTRIBUTION TO PORTS ON P8

*WHEN THE AUTO SPEED SENSING MODULE 932032 IS USED, K16 MUST BE 592153-G245 AS SHOWN.

A SYNCHRONOUS OPTION PATCH

1. FOR SYNCHRONOUS OPERATION, INSERT PATCH 593192G161 INTO LOCATIONS B11 & C5.
2. FOR ASYNCHRONOUS OPERATION, INSERT PATCH 592153G160 INTO LOCATIONS B11 & C5.
3. ALSO JUMPER E4 AS SHOWN BELOW

FOR THIS OPTION ON THIS GPCA PORT, JUMPER THESE PINS ON E4	NO. OF STOP BITS		FIXED RATE OR AUTO SPEED		SYNC/ASYNC	
	1	2	FIXED	AUTO	SYNC	ASYNC
PORT 0	1-4	1-5	11-4	11-5	7-4	7-5
1	2-4	2-5	12-4	12-5	8-4	8-5
2	3-4	3-5	13-4	13-5	9-4	9-5
3	6-4	6-5	14-4	14-5	10-4	10-5

MUX INTERRUPT PATCHES

MUX INTERRUPT PATCHES (THESE PATCHES ASSIGN THE GPCA CHAN REQUEST, ENABLE, AND ACKNOWLEDGE SIGNALS TO A MUX PORT).

ACKNOWLEDGE: M10 ENABLE: N9 REQUEST: N11

FOR GPCA PORT NO.	CONNECT PINS OF N9 AND M10 AS INDICATED FOR DESIRED GPCA CHAN/MUX PORT CONNECTION MUX PORT NO. 0	1	2	3	4	5	6	7	FOR GPCA PORT NO.	CONNECT PINS OF N11 AS INDICATED FOR DESIRED GPCA CHAN/MUX PORT CONNECTION MUX PORT NO. 0	1	2	3	4	5	6	7
0	9-8	9-7	9-6	9-5	9-4	9-3	9-2	9-1	0	1-16	1-15	1-14	1-13	1-12	1-11	1-10	1-9
1	10-8	10-7	10-6	10-5	10-4	10-3	10-2	10-1	1	2-16	2-15	2-14	2-13	2-12	2-11	2-10	2-9
2	11-8	11-7	11-6	11-5	11-4	11-3	11-2	11-1	2	3-16	3-15	3-14	3-13	3-12	3-11	3-10	3-9
3	12-8	12-7	12-6	12-5	12-4	12-3	12-2	12-1	3	4-16	4-15	4-14	4-13	4-12	4-11	4-10	4-9

GPCA 930646

Figure 2-5. GPCA Patching (Sheet 2 of 2)

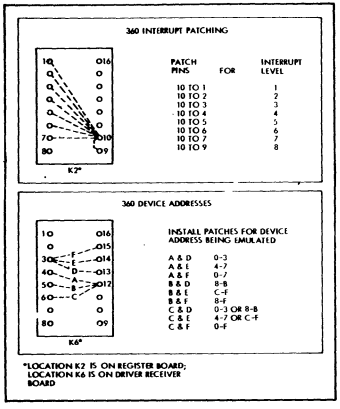


Figure 2-6. CIC Patching

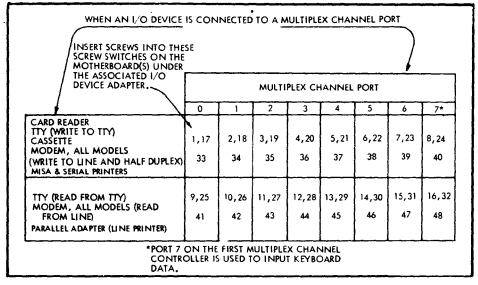


Figure 2-7. Motherboard Screw Switch Settings

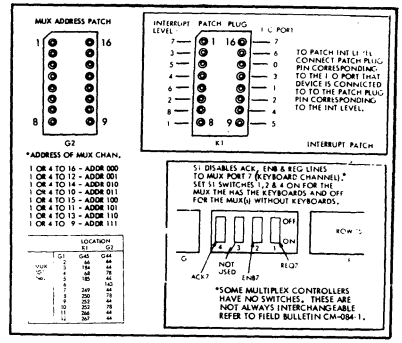


Figure 2-8. Multiplex Channel Controller Patches and Switches

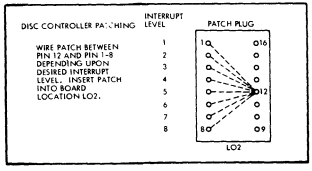


Figure 2-9. Disc Controller Patching

MISA 593296-	PATCH 592153G- & LOCATION M5	B2
G1 TERMINET 300 BAUD W/EOR	98	100
G2	98	101
G3 TERMINET 1200 BAUD W/EOR	99	100
G4	99	101
G5 TTY 110 BAUD W/EOR	106	105
G6	106	04
G7 TTY 50 BAUD W/O EOR	102	104
G8	102	105
G9 TTY 75 BAUD W/O EOR	103	104
G10	103	105
G11 TKT & BP PTR	107	108
G12	107	124
G13 EXTEL AR11	128	101
G14 VAST SIEMANS TTY	102	129
G15 COSSOR RS232	130	131
G16 BRAATHENS, TTY, FDX	103	132
G17 EXTEL PTR 165 BAUD	139	140
G18 TTY FDX	106	154
G19 CENTRONICS 1200 BAUD	99	156
G20 IER BP PTR	107	217
G21 QUME PTR	99	124
G22 DIABLO RS 232 PTR	98	229
G23 PTS 1200 - ACOUSTIC COUP	98	233
G24 TERMINET 30 W/DEMAND LINE	98	124

Figure 2-10. Multiinterface Serial Adapter Patching

ON THIS MODEL CASSETTE ADAPTER C	MAKE THESE JUMPERS	TO CONNECT THIS CASSETTE DRIVE
860566G1	E1-E2, E4-E5, E8-E9, E10-E11	594968 (5V)
860566G2	E2-E3, E5-E6, E7-E8, E10-E11	594132 (7V) (OLD DRIVE)

Figure 2-11. Cassette Adapter C Jumpers

G1 **FULL DUPLEX-TTY**

INSERT PATCH PLUGS* 592153-G11 INTO LOCATION Z1, G10 INTO LOCATION Z2, AND G9 INTO LOCATION Z3 OF SERIAL ADAPTER 591558.

G2 **HALF DUPLEX-TTY & SERIAL PRINTER** (300 BAUD)

INSERT PATCH PLUGS* 592153-G13 INTO LOCATION Z1, G14 INTO LOCATION Z2 AND G12 INTO LOCATION Z3 OF SERIAL ADAPTER 591558.

G 3 **HALF DUPLEX-TTY & SERIAL PRINTER** (1200 BAUD)

INSERT PATCH PLUGS* 592153-G47 INTO LOCATION Z1, G14 INTO LOCATION Z2 AND G46 INTO LOCATION Z3 OF SERIAL ADAPTER 591558.

* SEE FIGURE 2-24 FOR PATCH PLUG WIRING

Figure 2-12. Serial Adapter Patching for TTY and Serial Printer (TermiNet)

AMA 591707-		DISCIPLINE	FULL/HALF DUPLEX	MARK/SPACE IDLE	PARITY INT YES/NO	LOCATION A1	D7	J8	Z1	Z3	Z4
	G1	CTMC	FULL	MARK	YES	G73	G31	G30	G113	G71	G72
	G2	CTMC	FULL	MARK	NO	G73	G31	G32	↑	↑	↑
	G3	CTMC	FULL		YES	G73	G33	G30	↑	↑	↑
	G4	CTMC	FULL	SPACE	NO	G73	G33	G32	↑	↑	↑
	G5	CTMC	HALF	—	YES	G74	G34	G36	↓	↓	↓
	G6	CTMC	HALF	—	NO	G74	G34	G37	G113		
	G7	2848	FULL	MARK	YES	G73	G39	G38	G70		
	G8	2848	FULL	MARK	NO	G73	G39	G40	↑		
	G9	2848	FULL	SPACE	YES	G73	G41	G38	↑		
	G10	2848	FULL	SPACE	NO	G73	G41	G40	↑		
	G11	2848	HALF	—	YES	G75	G43	G42	↓		
	G12	2848	HALF	—	NO	G75	G43	G7	G70	G71	G72
	G13	3270	FULL			G93	G31	G32	G90	G95	G94
	G14	3270	HALF			G75	G31	G37	G90	G95	G94
	G15	RIMS	FULL			G218	G31	G32	G90	G95	G94
	G16	3270 ASCII				G169	G31	G32	G113	G71	G72
	G17	2780				G169	G91	G92	G90	G95	G94

Figure 2-14. Modem Adapter CTMC (2332), 2848 (2333), and 3270 (2334) Patching

PATCH 'G' NO.	L2	G4	F8	E8	M7	M2
G1	65	50	51	52	53	54
2	65	55	56	57	60	61
3	65	55	56	57	58	59
4	62	63	56	64	58	59
AMA 5	65	55	125	57	126	127
G + 6	65	225	226	227	223	222
7	62	236	234	235	58	59
8	62	236	234	235	126	127
9	65	225	238	227	240	239
10	65	225	238	227	244	239
G11	65	225	238	227	58	59

NOT USED, ALWAYS CUT OR LEAVE UP

PORT

PATCH

* LEAVE DOWN THE ONE PIN FOR THE ASSIGNED PORT

ALWAYS LEAVE DOWN

SDLC

MAKE ALL PATCHES FOR LOCATIONS N9, N10, N11, N12, M9 AND M10 THE SAME

M2 AND M7 PATCHING

FOR THIS BAUD RATE SHORT THESE PINS TO THESE PINS*	ON THESE PATCH PLUGS M2 9	10	11	12	13	14	15	16	M7 9	10	11	12	13	14	15	16
75	7	7	7	6	3	4	3	1	7	8	7	6	3	4	2	2
150	7	7	7	5	4	3	2	1	7	7	6	5	4	3	2	2
300	7	7	7	5	5	4	3	2	7	7	7	6	5	4	3	2
600	7	7	7	5	3	5	2	1	8	7	7	5	4	3	2	1
1200	7	7	7	5	5	5	3	2	7	8	7	6	3	2	3	2
1800	7	7	7	5	3	5	3	3	8	8	7	6	4	3	1	1
2400	7	7	7	5	5	5	3	3	8	7	6	5	3	3	2	1
3200	7	7	7	5	5	5	3	3	7	8	6	6	4	3	3	2
4800	7	7	7	5	5	5	3	3	7	8	7	6	3	3	1	1

*NOTE: PINS 1,3,5, & 7 ARE COMMON AND PINS 2,4,6, & 8 ARE COMMON.

F8 PATCHING

NO. DATA BITS	PARITY ODD-EVEN	STOP BITS	ON PATCH PLUG #8 TIE THESE PINS TO LOGIC 1 OR 0* 11	12	13	14	15
8	NONE	2	0	1	1	0	1
8	NONE	2	0	1	1	1	0
8	ODD	2	0	1	1	0	0
8	ODD	2	0	1	1	1	1
8	EVEN	2	1	1	1	0	0
8	EVEN	2	1	1	1	1	1
7	NONE	2	1	0	1	0	1
7	NONE	2	0	0	1	1	0
7	ODD	2	0	0	1	0	1
7	ODD	2	0	0	1	1	0
7	EVEN	2	1	0	1	0	0
7	EVEN	2	1	0	1	1	1
6	NONE	2	1	1	0	0	1
6	NONE	2	0	1	0	1	0
6	ODD	2	0	1	0	0	0
6	ODD	2	0	1	0	1	1
6	EVEN	2	1	1	0	0	0
6	EVEN	2	1	1	0	1	1
5	NONE	2	1	0	0	0	1
5	NONE	2	0	0	0	1	0
5	ODD	2	0	0	0	0	0
5	ODD	2	0	0	0	1	1
5	EVEN	2	1	0	0	0	0
5	EVEN	2	1	0	0	1	1

* FOR LOGIC 1 TIE TO PINS 1,3,5 OR 7
FOR LOGIC 0 TIE TO PINS 2,4,6 OR 8

L2 PATCHING

FOR THIS MODE OF OPERATION	TIE THESE PINS TOGETHER
FULL DUPLEX	2-14, 4-13, 7-9, 6-10
HALF DUPLEX	6-11, 8-9, 11-15
INTERRUPT ON PARITY ERROR	3-12
NO INTERRUPT ON PARITY	4-12
NORMAL CH BREAK	1-15

G4 PATCHING

FOR THIS MODE OF OPERATION	TIE THESE PINS TOGETHER
FULL DUPLEX	1-15, 2-16, 5-12, 6-11
HALF DUPLEX	1-15, 3-14, 4-13, 11-12
8 DATA BITS	7-9
7 DATA BITS OR LESS	7-10

E8 PATCHING

FOR THIS MODE OF OPERATION	TIE THESE PINS TOGETHER
HALF DUPLEX	6-11
FULL DUPLEX	7-11
PARITY ERROR CHAR	8-9
REVERSE CH BREAK	1-15, 3-13
NORMAL CH BREAK	2-15, 3-14
REVERSE CH OR HALF-DUPLEX 4 WIRE	5-12
NO REVERSE CH OR FULL DUPLEX	4-12
NULL CHARACTER	9-10

NOTE: SEE FIGURE 2-24 FOR PATCH PLUG WIRING

Figure 2-15. Modem Adapter, Asynchronous AMA (2341) Patching

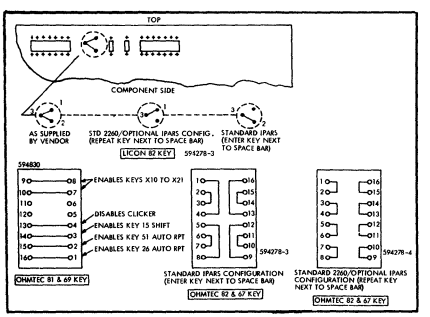


Figure 2-16. Keyboard Patching

PARALLEL ADAPTER PATCHING AND SWITCHING FOR DATA PRODUCTS 2230 LINE PRINTER

IN THESE LOCATIONS	INSERT PATCHES 591572-	ALSO SET DIP SWITCH F1 AS FOLLOWS:
A2	G148	8 — NOT USED
D3	G148	ON 7
B2	G149	6
		OFF 5
CONTROL ASSOCIATED STATUS BIT: WHEN SWITCH 15 OFF STATUS BIT IS '1': TESTED BY IODC.		ON 4 — STATUS BITS 6 5 4 3
		OFF 3
		OFF 2
		OFF 1

Figure 2-13. Parallel Adapter Patching and Switching for Line Printer D. P. Model 2230

	FOR THIS MODEM	INSERT THESE PATCHES INTO THESE LOCATIONS K6	A2
ADAPTER 860820	G1 FDX PAIN AM	G163	G147
	G2 HUB POLLING	G170	G162
	G3 FDX STD IPARS		G147
	UP/DOWNLINE IPARS		G220
ADAPTER 591556	ADAPTER 591556 FOR FULL DUPLEX MODE INSERT PATCH PLUG 592153-G25 INTO LOCATIONS E5 AND G27 INTO LOCATION J3 OF THE IPARS MODEM ADAPTER. SEE FIGURE 2-24 FOR THE PATCH PLUG WIRING.		

Figure 2-17. IPARS Modem Adapter 2331 Patching

SWITCH	40X12 (24)	80 X 12	(24)	64 X 15	(30)	OPTIONS
1	—	—	—	—	—	NOTE 1
2	—	—	—	—	—	NOTE 2
3	OPEN *	OPEN	CLOSED	OPEN	CLOSED	—
4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
5	CLOSED	CLOSED	CLOSED	OPEN	OPEN	—
6	CLOSED	OPEN	OPEN	OPEN	OPEN	—
7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
8	—	—	—	—	—	NOTE 3

NOTES:

*CLOSE FOR 40 X 24

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

MONITOR CONTROLLER B MODIFIED AND C CHARACTER/LINE FORMAT E6 SWITCH SETTINGS

E6 CHIP SWITCH SETTING	40 CHAR. 12 LINES	80 CHAR. 12 LINES	64 CHAR. 15/16 LINES	80 CHAR. 24 LINES	64 CHAR. 30 LINES	40 CHAR. 24 LINES	STEP SCAN*
E6-1	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	CLOSED
E6-2	OPEN	OPEN	OPEN†	OPEN	OPEN	OPEN	OPEN
E6-3	OPEN	OPEN	OPEN	CLOSED	CLOSED	CLOSED	CLOSED
E6-4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
E6-5	CLOSED	CLOSED	OPEN	CLOSED	OPEN	CLOSED	**
E6-6	CLOSED	OPEN	OPEN	OPEN	OPEN	CLOSED	OPEN
E6-7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
E6-8††	OPEN	OPEN	OPEN†	OPEN	OPEN	OPEN	OPEN

*USABLE ONLY ON 24 OR 30 LINE FORMAT. SPACING BETWEEN LINES IS ADJUSTABLE BY SETTING R35.

**SET AS INDICATED FOR 24 OR 30 LINE FORMAT.

†CLOSED FOR 16 LINE FORMAT

††E6-8 IS USED ON SOME MC'S (IT IS USED ON ALL 16 LINE MC'S).

NOTE: WHEN MC IS USED WITH SPLIT SCREEN DISPLAYS A JUMPER IS CONNECTED BETWEEN X12 PIN 15 AND X7 PIN 14.

MONITOR CONTROLLER B-16 CHARACTER/LINE FORMAT E6 SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT 40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5				
6		See Below		
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.
When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

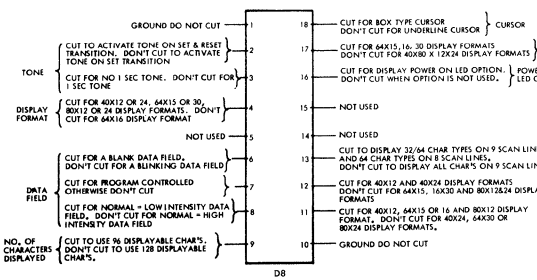
Switch Chip — D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.
for LOW Intensity - close even numbered switches and open all others.

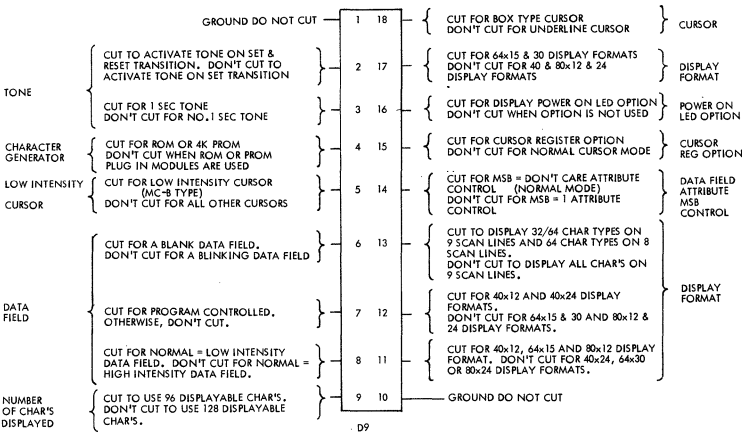
Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1; Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS



MONITOR CONTROLLER F CONFIGURATION CONTROL MANUAL DATA CHIP D8 SETTINGS

Figure 2-18. Monitor Controller Switch and Data Chip Settings (Sheet 1 of 2)



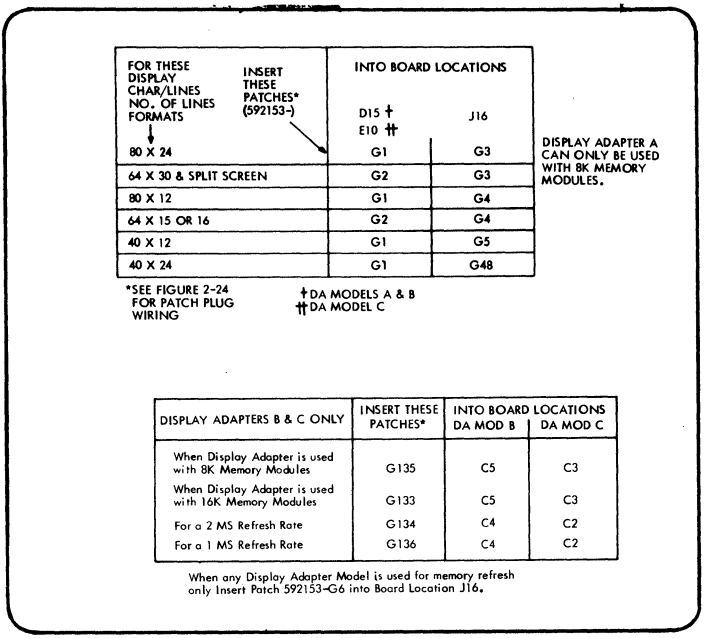
DIP SWITCH BETWEEN A1 & A2 — SET ALL TO OFF WHEN USING TWISTED PAIR TO DA.
SET ALL TO ON WHEN USING COAX.

DIP SWITCH E17/F17

1	ON - 9 LINE LC CHARACTERS OFF - # OF CHAR LINES DETERMINED BY D9-13
2	ON - 128 7 x 7 CHARACTERS OFF - WHEN 3 BELOW IS ON
3	ON - 96 CHAR (32 7 x 9 LC CHARACTERS) OFF - WHEN 2 ABOVE IS ON
4	NOT USED

MONITOR CONTROLLER SWITCH & DATA CHIP D9 SETTINGS

Figure 2-18. Monitor Controller Switch and Data Chip Settings (Sheet 2 of 2)



FOR THESE DISPLAY CHAR/LINES NO. OF LINES FORMATS ↓	INSERT THESE PATCHES* (592153-)	INTO BOARD LOCATIONS D15 † E10 ††	J16
80 X 24		G1	G3
64 X 30 & SPLIT SCREEN		G2	G3
80 X 12		G1	G4
64 X 15 OR 16		G2	G4
40 X 12		G1	G5
40 X 24		G1	G48

DISPLAY ADAPTER A CAN ONLY BE USED WITH 8K MEMORY MODULES.

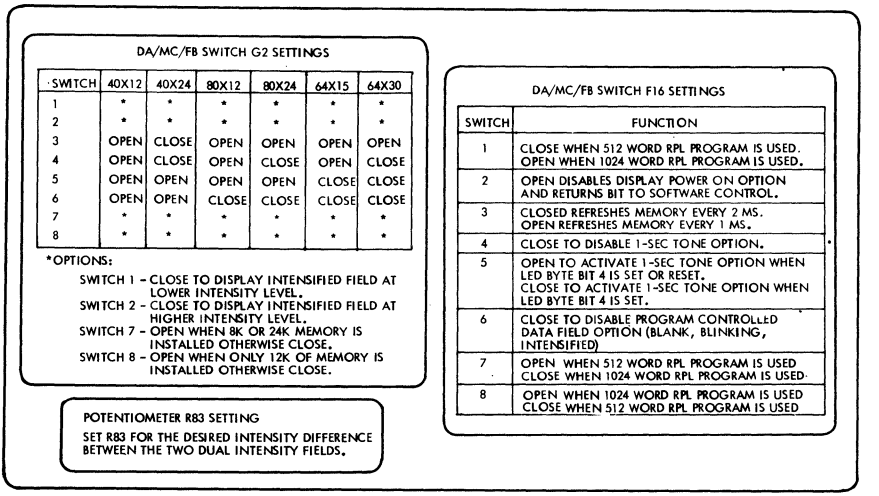
*SEE FIGURE 2-24 FOR PATCH PLUG WIRING

†DA MODELS A & B
††DA MODEL C

DISPLAY ADAPTERS B & C ONLY	INSERT THESE PATCHES*	INTO BOARD LOCATIONS DA MOD B	DA MOD C
When Display Adapter is used with 8K Memory Modules	G135	C5	C3
When Display Adapter is used with 16K Memory Modules	G133	C5	C3
For a 2 MS Refresh Rate	G134	C4	C2
For a 1 MS Refresh Rate	G136	C4	C2

When any Display Adapter Model is used for memory refresh only Insert Patch 592153-G6 into Board Location J16.

Figure 2-19. Display Adapter Character/Line Format Patch Plugs



DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40X12	40X24	80X12	80X24	64X15	64X30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL.
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL.
SWITCH 7 - OPEN WHEN 8K OR 24K MEMORY IS INSTALLED OTHERWISE CLOSE.
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE.

POTENTIOMETER R83 SETTING

SET R83 FOR THE DESIRED INTENSITY DIFFERENCE BETWEEN THE TWO DUAL INTENSITY FIELDS.

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL.
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE TO DISABLE PROGRAM CONTROLLED DATA FIELD OPTION (BLANK, BLINKING, INTENSIFIED)
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED CLOSE WHEN 1024 WORD RPL PROGRAM IS USED
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED CLOSE WHEN 512 WORD RPL PROGRAM IS USED

Figure 2-20. DA/MC/FB Switch and Intensity Potentiometer Settings

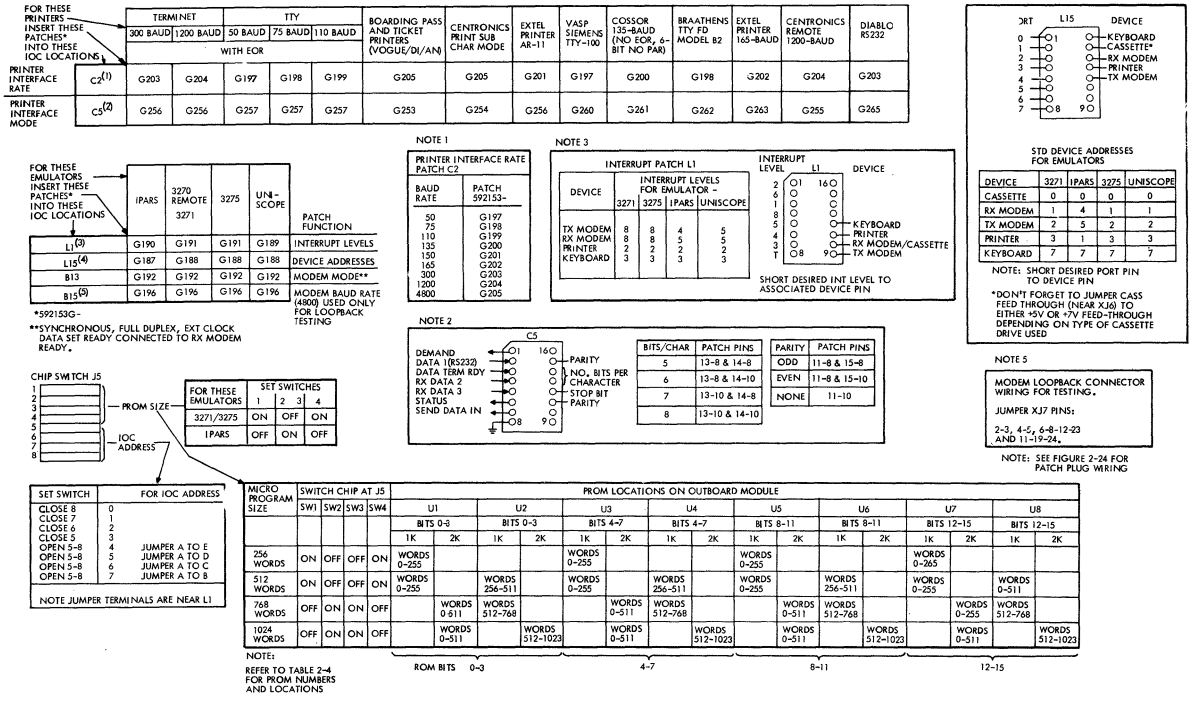


Figure 2-21. IOC Patching and Switching.

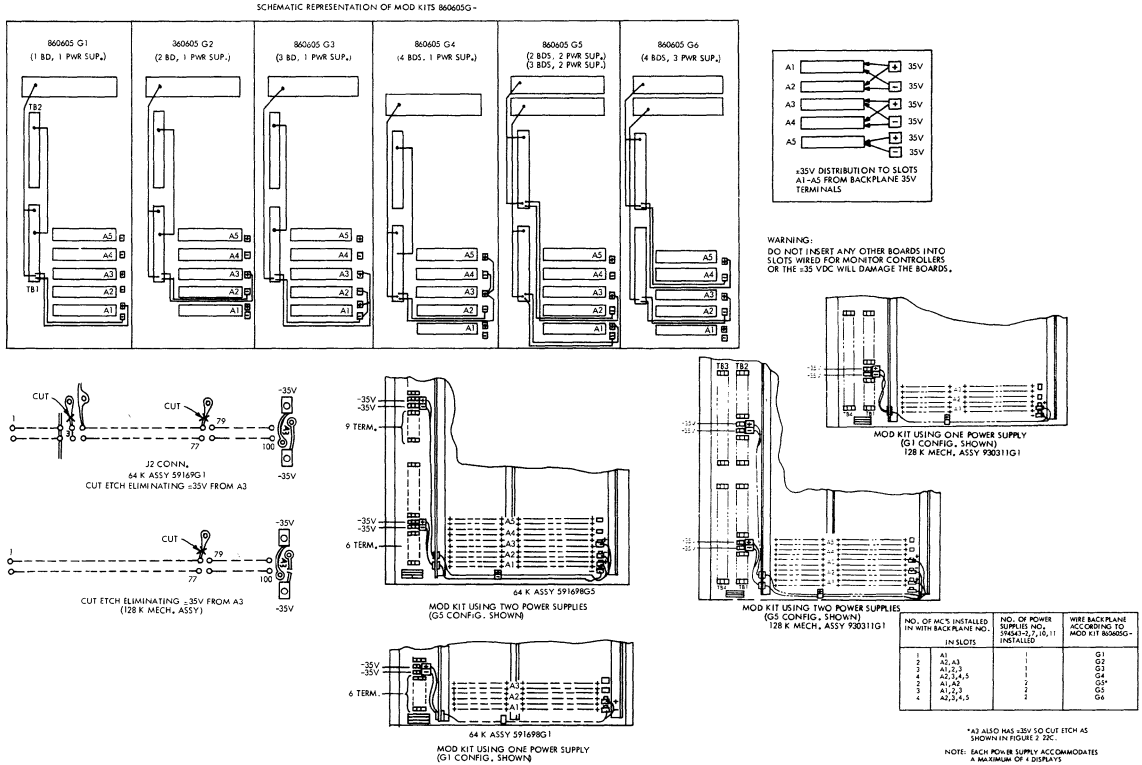
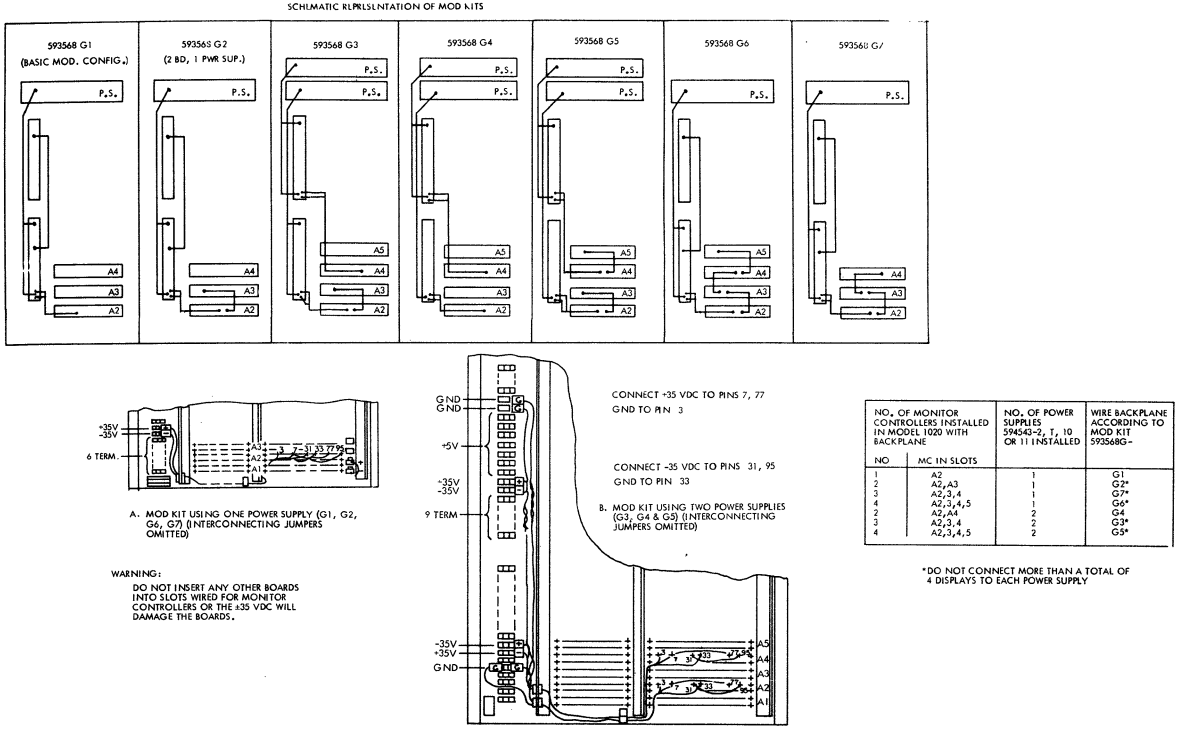


Figure 2-22. New 1020, 1020M, 1030 and 1030M Backplane Wiring Modifications for Different Numbers of Monitor Controllers



NO. OF MONITOR CONTROLLERS INSTALLED IN MODEL 1020 WITH BACKPLANE		NO. OF POWER SUPPLIES 594543-2, T, 10 OR 11 INSTALLED	WIRE BACKPLANE ACCORDING TO MOD KIT 593568G-
NO	MC IN SLOTS		
1	A2	1	G1
2	A2,A3	1	G2*
3	A2,3,4	1	G7*
4	A2,3,4,5	1	G6*
2	A2,A4	2	G4
3	A2,3,4	2	G3*
4	A2,3,4,5	2	G5*

*DO NOT CONNECT MORE THAN A TOTAL OF 4 DISPLAYS TO EACH POWER SUPPLY

Figure 2-23. Old 1020 Backplane Wiring Modifications for Different Numbers of Monitor Controllers

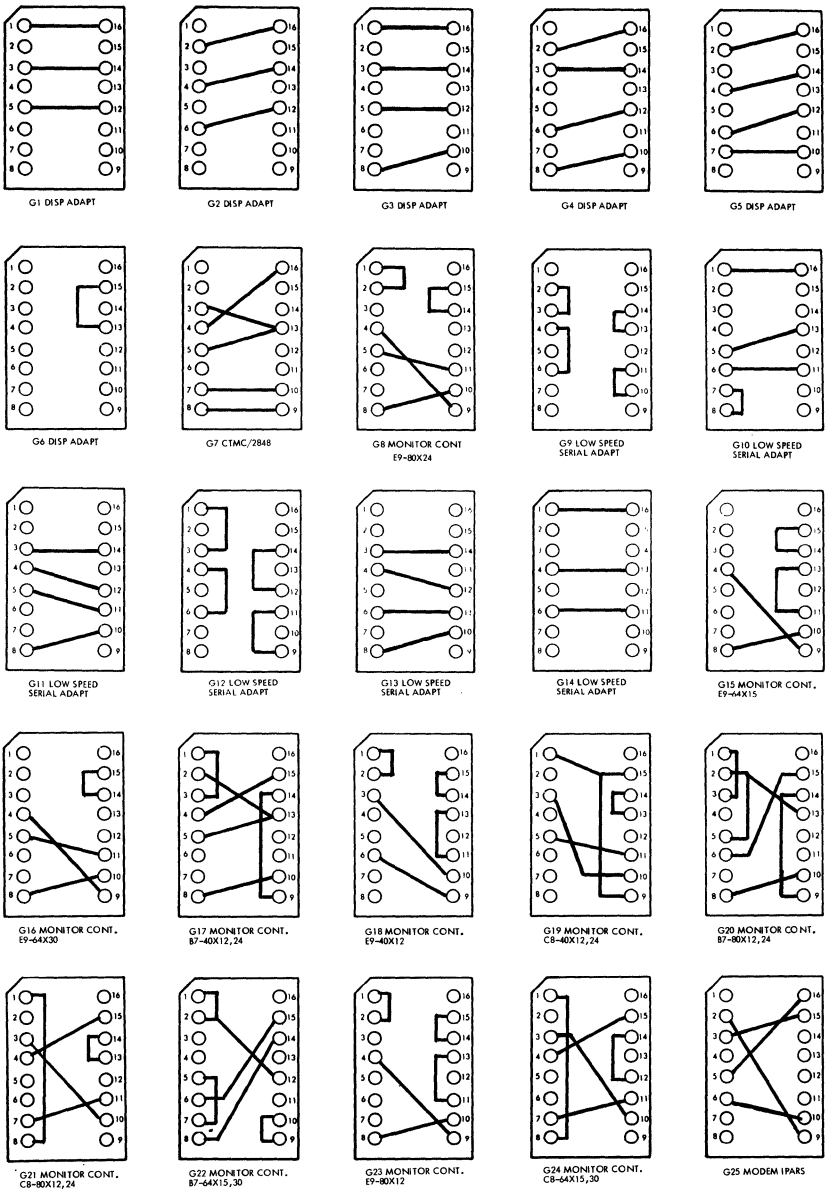


Figure 2-24. Patch Plug Wiring (Sheet 1 of 12)

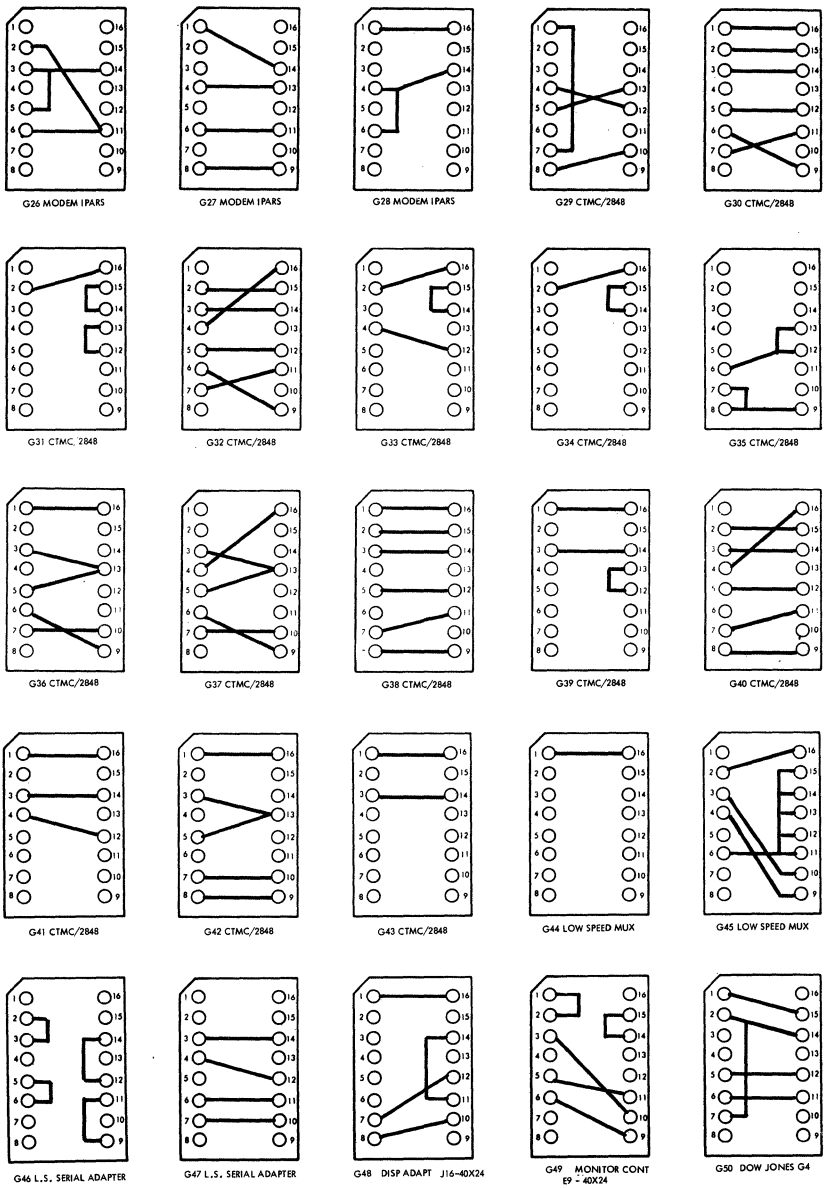


Figure 2-24. Patch Plug Wiring (Sheet 2 of 12)

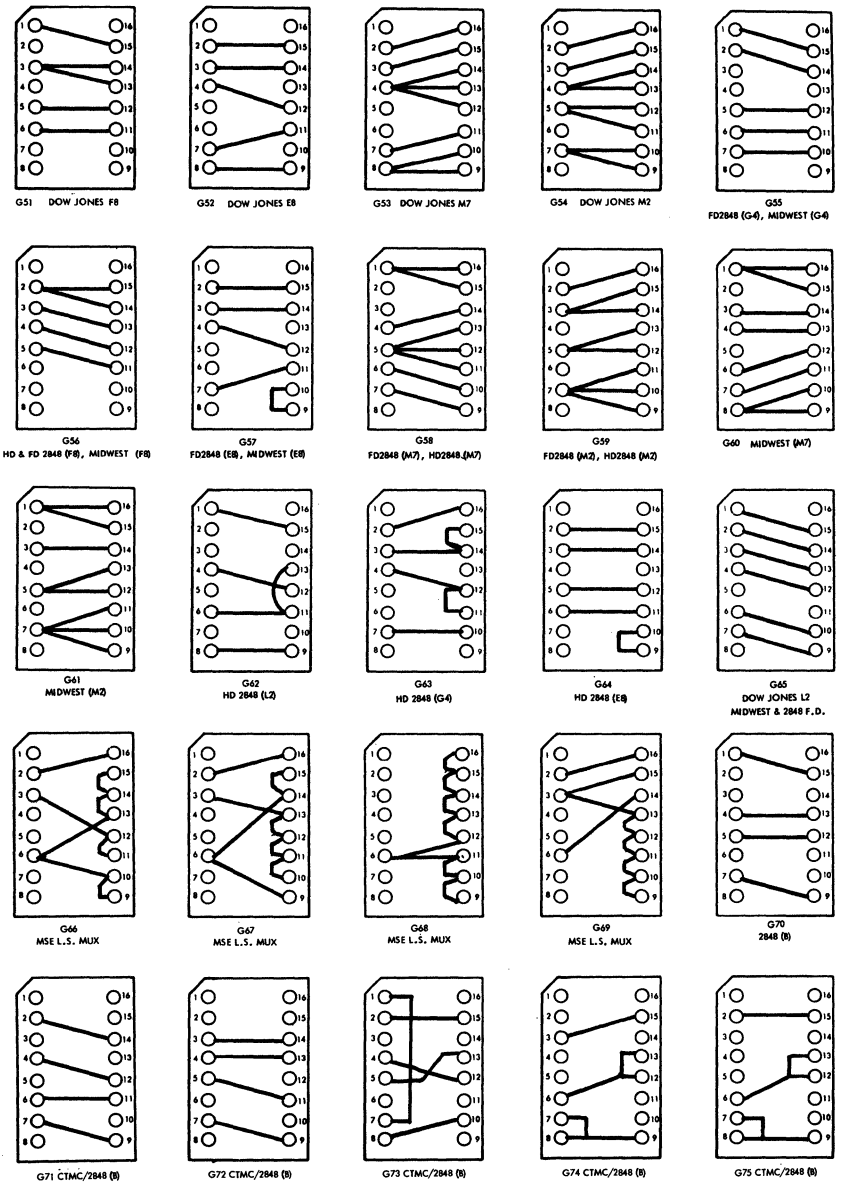


Figure 2-24. Patch Plug Wiring (Sheet 3 of 12)

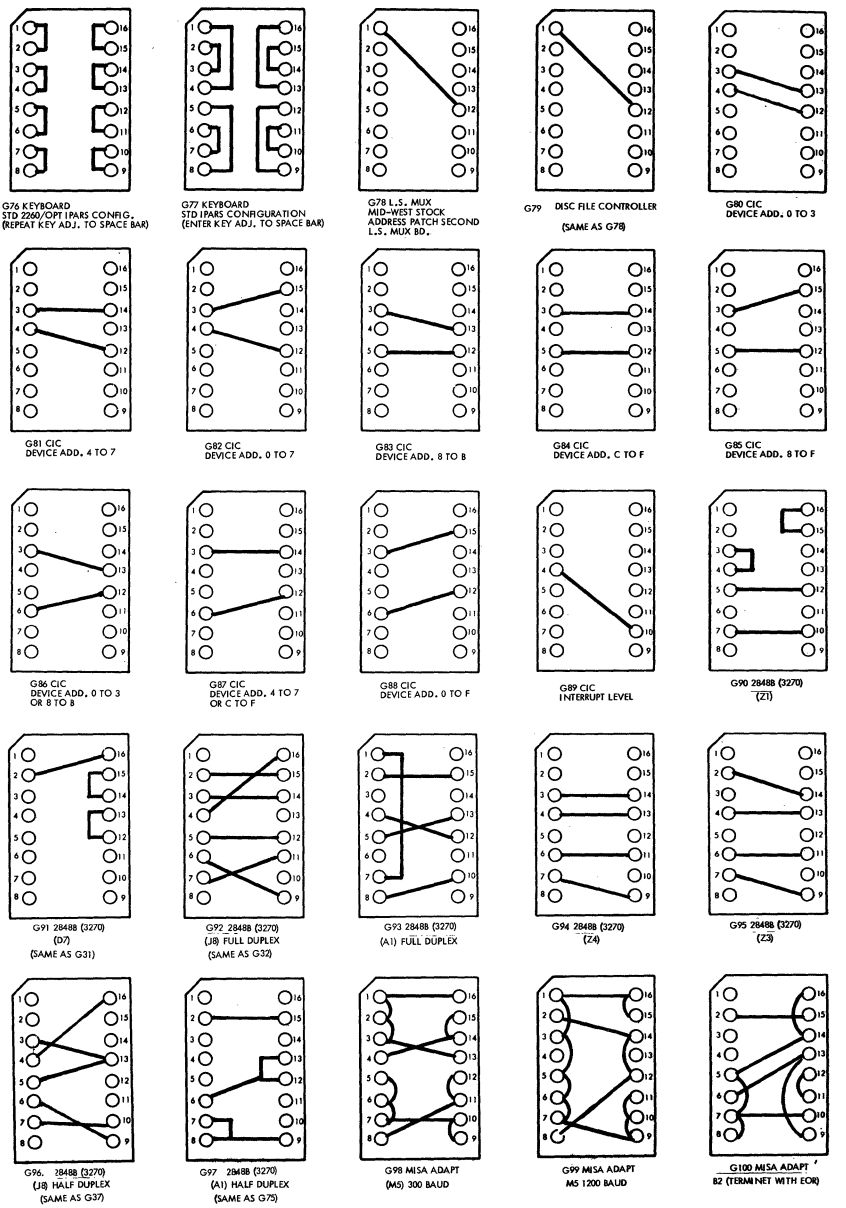


Figure 2-24. Patch Plug Wiring (Sheet 4 of 12)

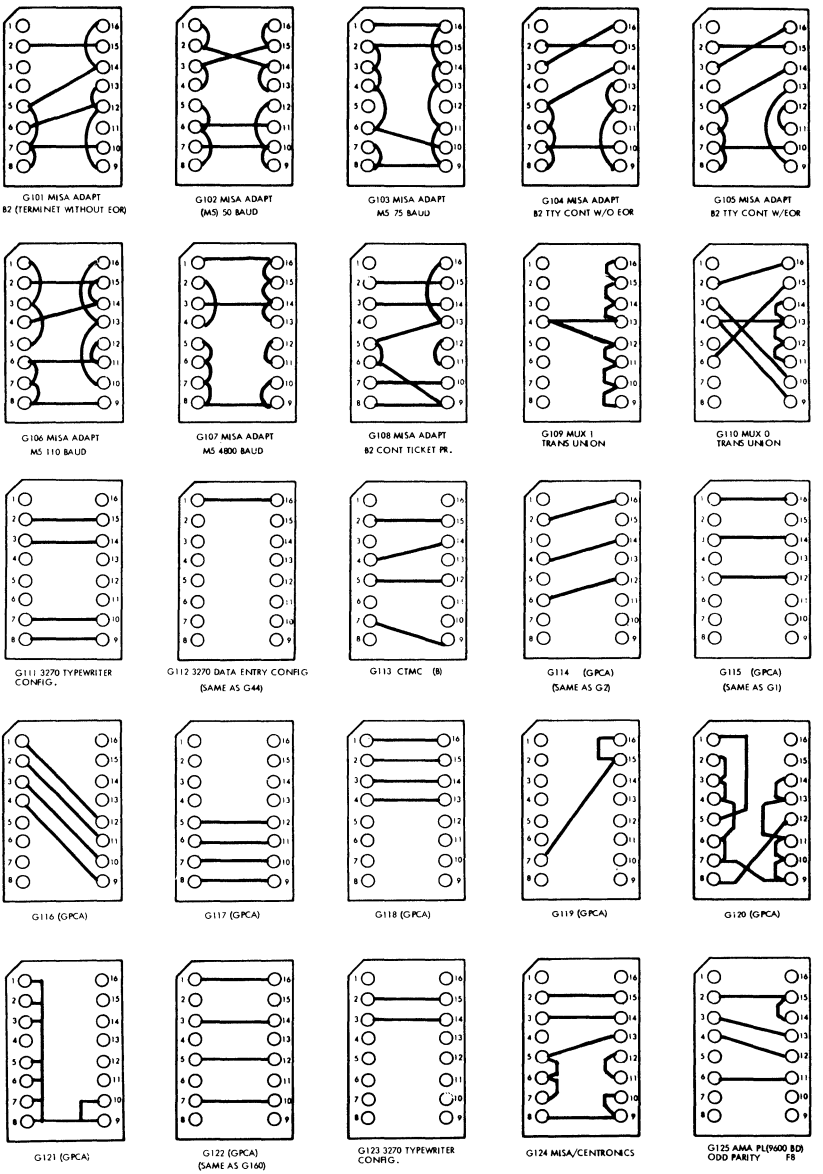


Figure 2-24. Patch Plug Wiring (Sheet 5 of 12)

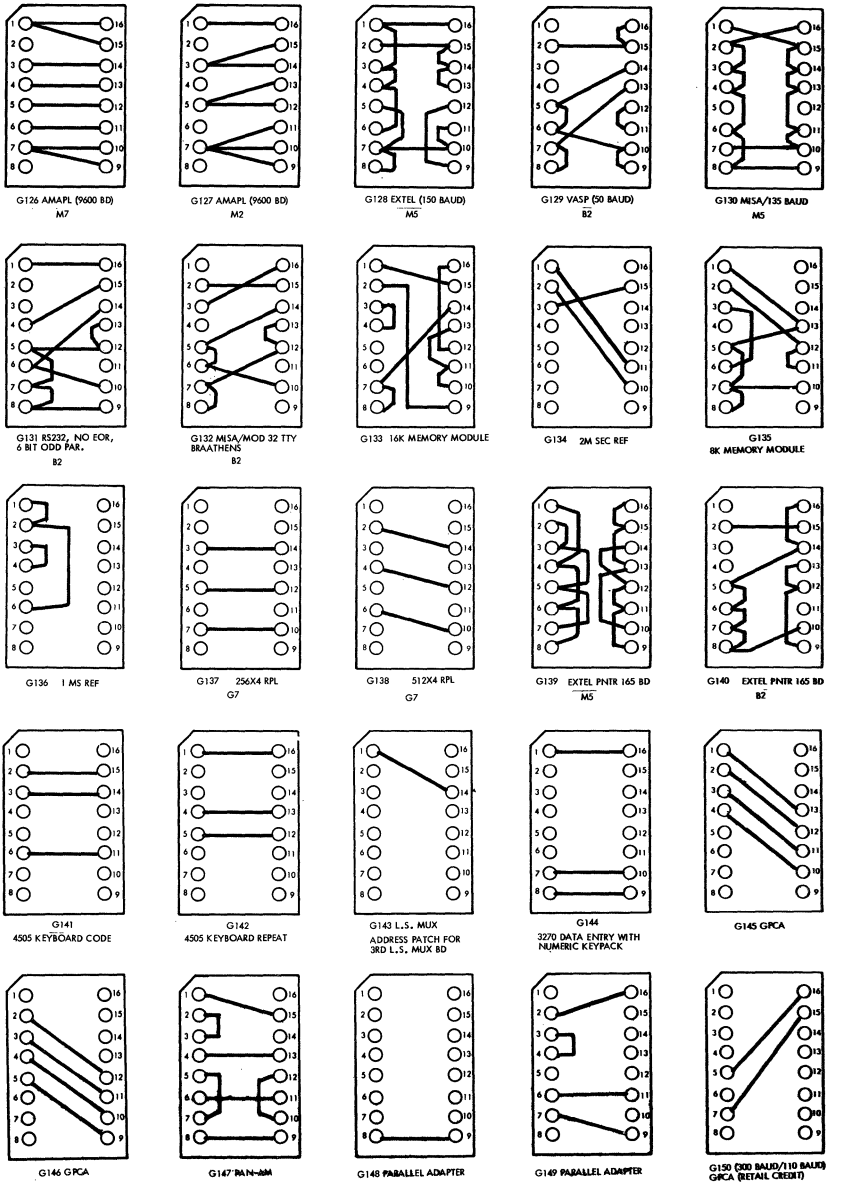


Figure 2-24. Patch Plug Wiring (Sheet 6 of 12)

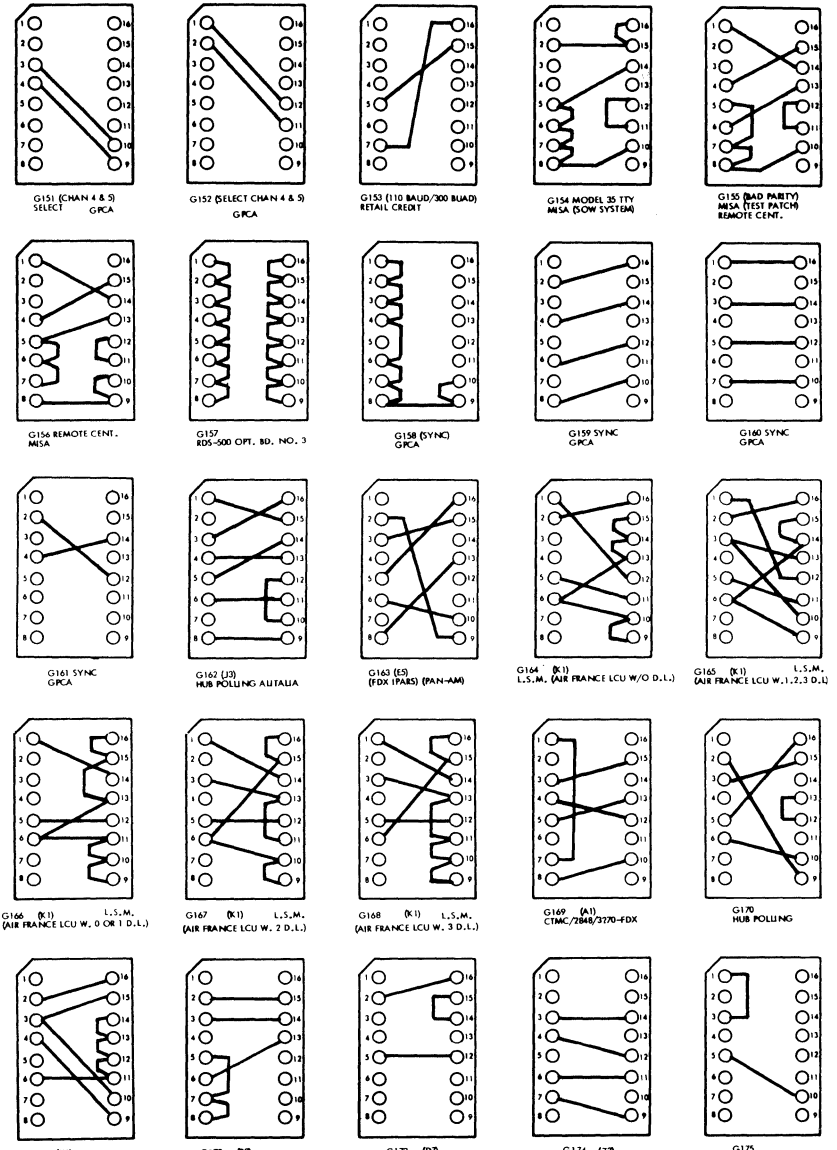


Figure 2-24. Patch Plug Wiring (Sheet 7 of 12)

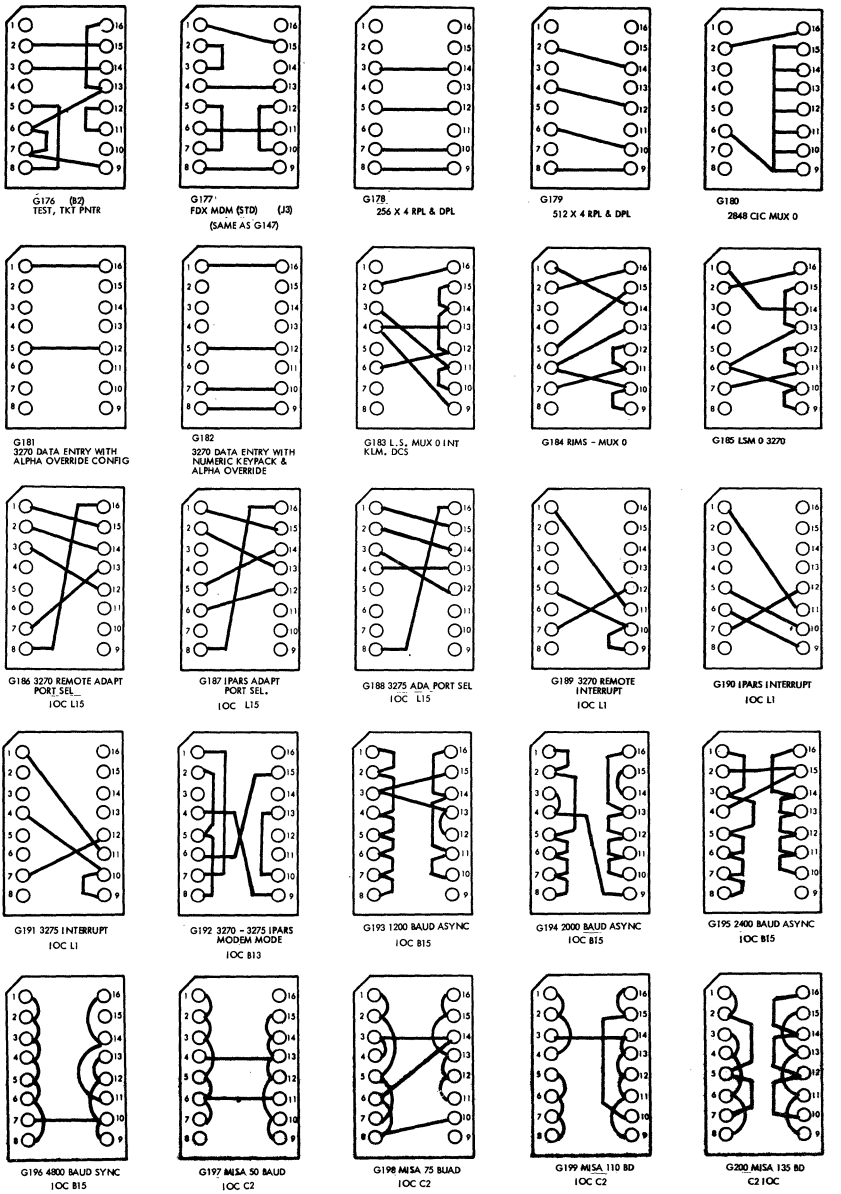


Figure 2-24. Patch Plug Wiring (Sheet 8 of 12)

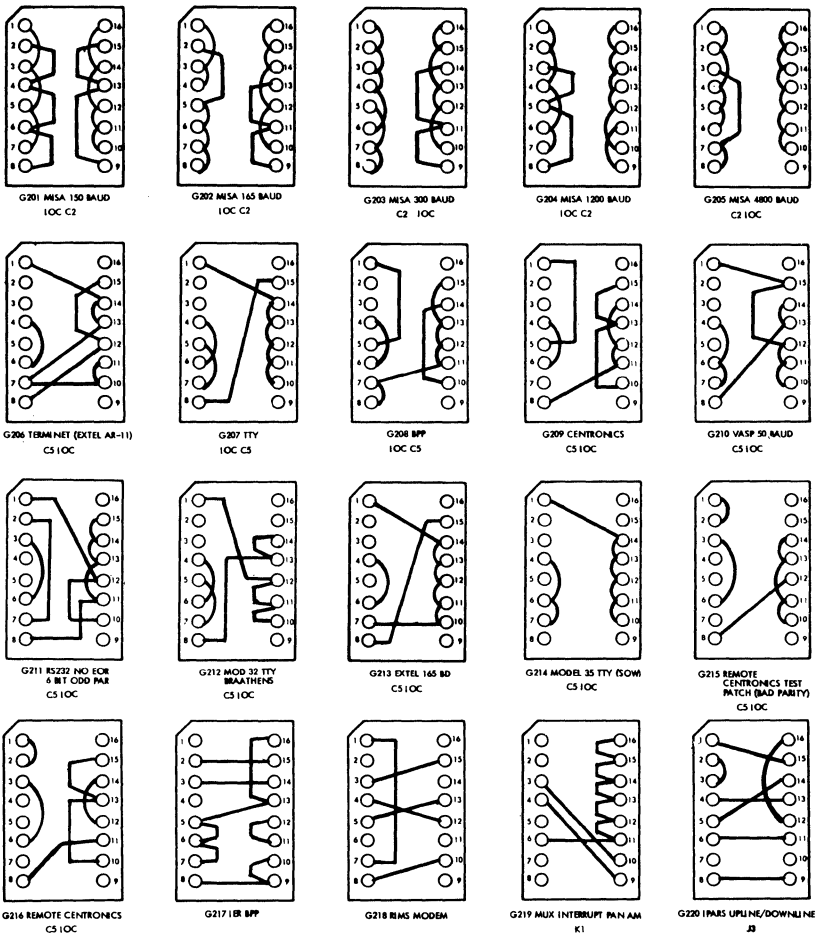


Figure 2-24. Patch Plug Wiring (Sheet 9 of 12)

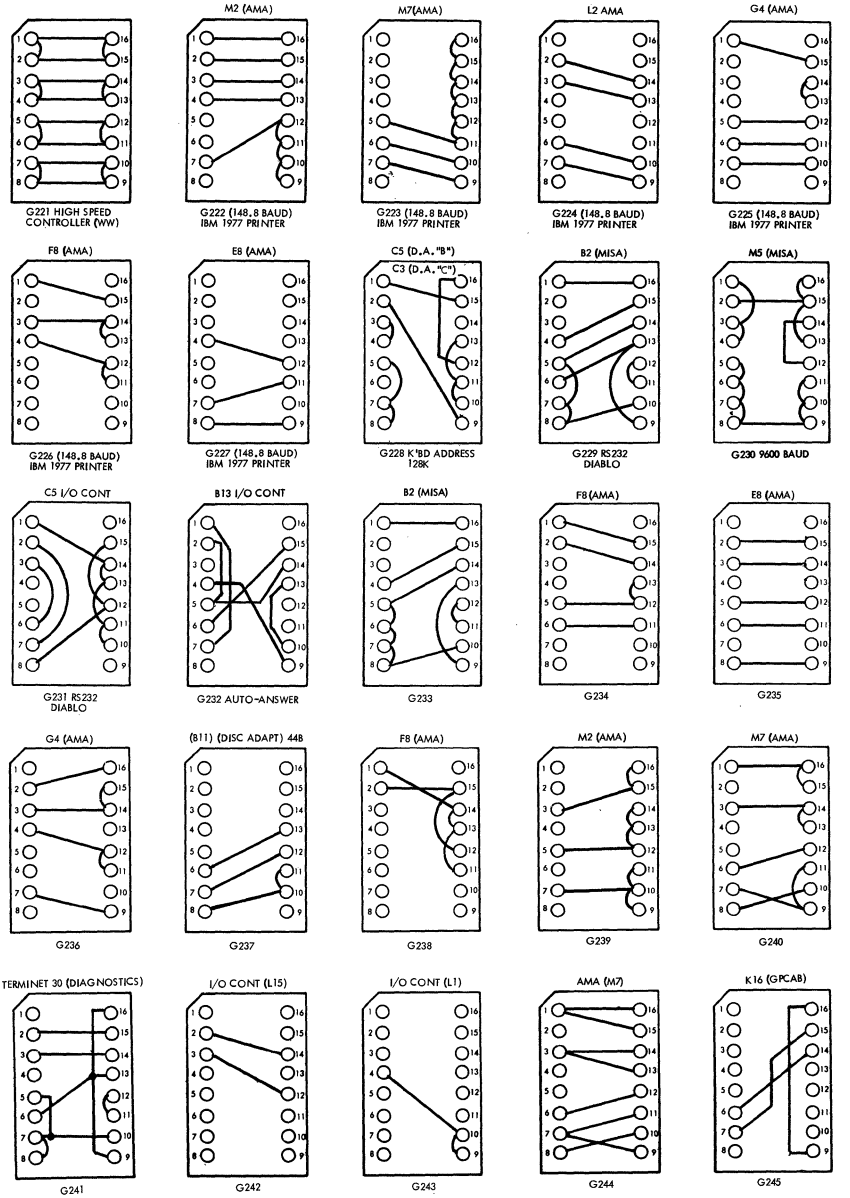


Figure 2-24. Patch Plug Wiring (Sheet 10 of 12)

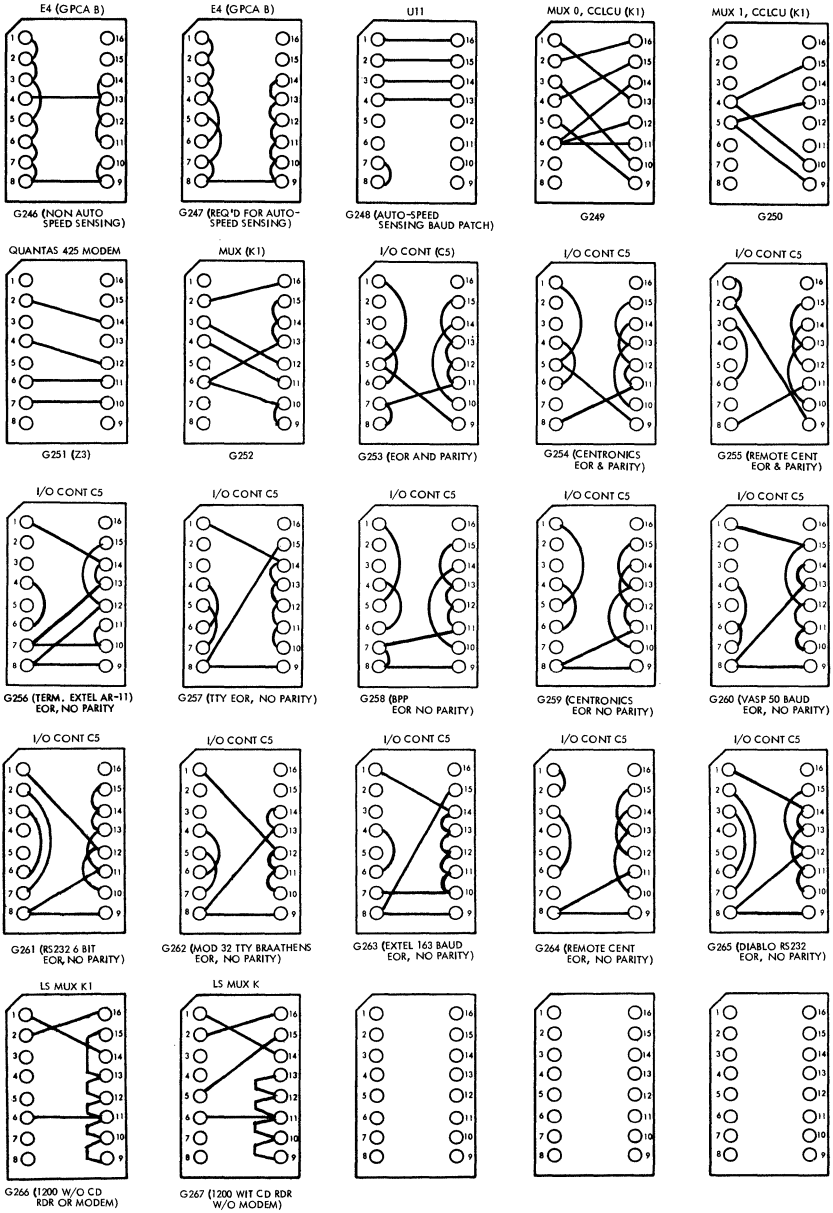


Figure 2-24. Patch Plug Wiring (Sheet 11 of 12)

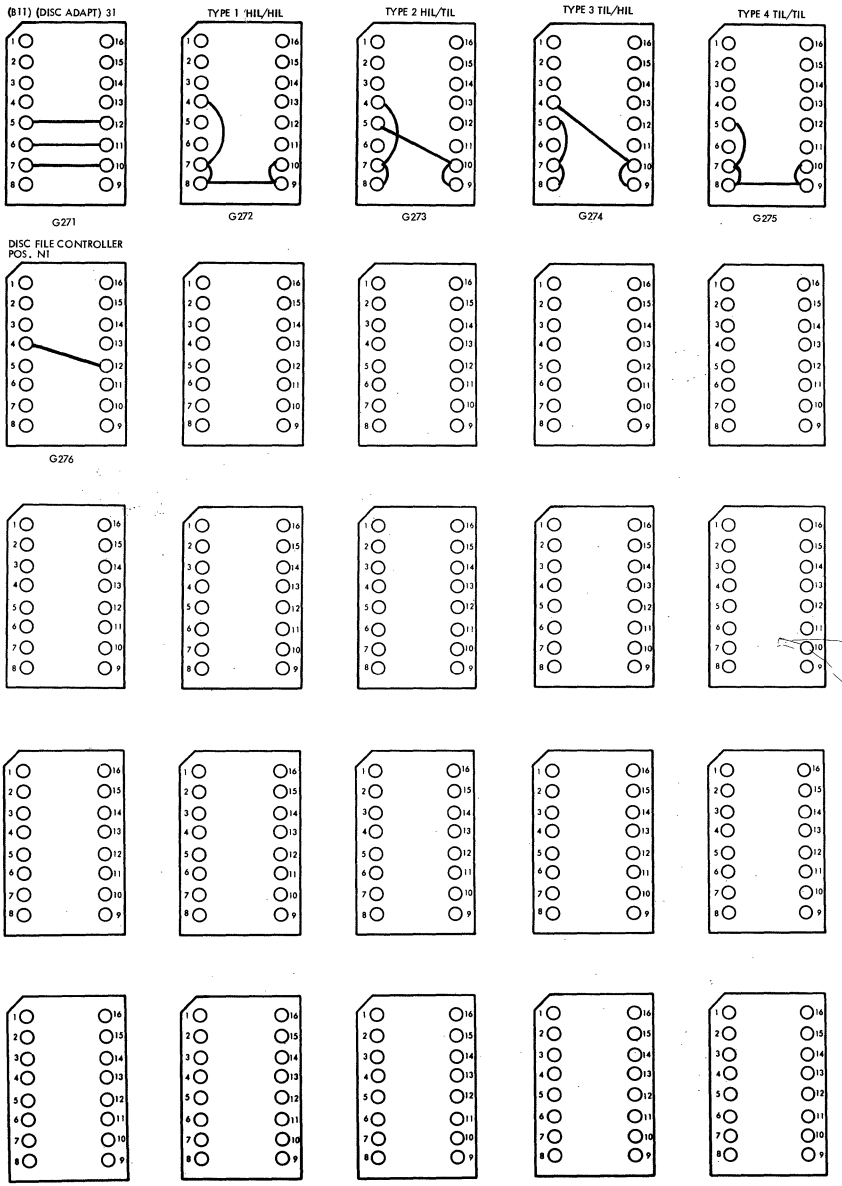


Figure 2-24. Patch Plug Wiring (Sheet 12 of 12)

CHAPTER 3. THEORY OF OPERATION

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LIST OF TABLES

3.1 Processing Unit Interfaces and Input/Output Facilities

3.1.1 General

The PTS-100 has four types of I/O operations: keyboard data input, display refresh data output, high speed device I/O, and low speed device I/O (multiplex channel). All I/O operations except the display refresh are performed over the processor direct memory access input/output bus (IOB). Data to refresh the displays is sent out to the displays directly from memory via display adapters and monitor controllers. The input/output system is shown in Figure 3-1.

Controller servicing on the IOB is on a fixed dual priority basis, with each controller having two levels of priority. The controller that is plugged in electrically nearest to the processor has the highest and lowest priorities. The next controller in line has the second highest and second lowest priorities, etc. These interrupt priorities are separate from those for the processor priority interrupt facility (paragraph 3.1.8) which is used to alert the processor to interrupt conditions in the controllers. I/O device servicing and the multiplex channel controller / I/O device adapter bus is also on a fixed priority basis, with device adapter 7 having the highest priority and adapter 0 having the lowest priority. In either case, the interrupts are serviced in ascending priorities, with all higher priority interrupts serviced before a lower priority interrupt can be serviced.

3.1.2 Input/Output Bus

All processor I/O transfers take place over the input/output bus (IOB), initiated by the processor and under control of the attached controllers. A data transfer rate of approximately one megabyte per second can be transferred over the I/O bus. The controllers permit attachment of disc memories, magnetic tape transports, and host processor channel interfaces, as well as other special interfaces. Up to ten high speed controllers and one to three low speed multiplexer channel controllers may be attached to the IOB, depending upon the PTS-100 system configuration. However, all controllers cannot be connected at the same time. Data is transferred to and from memory over a bidirectional 16 bit data bus in the IOB. The processor also uses this bus to address and control the I/O devices through their respective controllers. The CE console and feature board also attach to the IOB. The feature board contains the IPL and RPL programs, watchdog and interval timers, and the program load configuration controls. It communicates with the processor over the IOB and sends the program load information to the processor over the CPU/memory bus.

The timing of the signals on the IOB is shown in Figure 3-2, and the signal functions are described in Table 3-1. I/O device memory requests have priority over processor memory requests. Data transferred between processor and controllers is held valid for one or two processor arithmetic logic (ALU) cycles. Data transferred from a controller to the processor is put on the bus only when a device is selected and only for the amount of time that the data requesting control line is active. Control lines requesting data (status-in, address-in, data-in) are valid for two processor ALU cycles. Two processor instructions are used for all input/output operations, Do I/O and Read I/O. Both instructions have two arguments, the accumulator (ACC) and the memory effective address (EA). The Do I/O instruction initiates all I/O operations, and the Read I/O is used to read and reset I/O device status.

3.1.2.1 Do I/O. The Do I/O (DIO) instruction (2 in Figure 3-2) is issued to initiate either a start or a stop operation. The stop DIO instruction stops the I/O operation. It is initially used to clear all memory requests, reset the ICB and interrupts, and place the I/O device adapter in a ready not busy state. It requires no reply from the addressed controller. The start DIO instruction initiates an I/O operation. It consists of two 16 bit words: one contains the instruction and the other contains the effective address (EA) in memory of word 0 of a Physical Input Output Table (PIOT), which has all the information required to execute a particular input or output operation (see Figure 3-12 for the PIOT and Section 3.1.9 for the start Do I/O instruction). The controller stores the EA and replies to a start DIO instruction (3 in Figure 3-2) by raising the CYC Request line, putting the memory address of the first PIOT word back on the processor data bus, and putting a function code 7 (4 in Figure 3-2) on the function code bus. The processor reads the function code and sends the first PIOT word to the controller, where the controller and device order codes are extracted, stored in a stack and the device order code also sent to the associated I/O device adapter. The order codes specify search and translate functions to the controller and the functions to be performed by the I/O device adapter. This completes the I/O initialization sequence for the multiplexer (other I/O controllers fetch and store the entire I/O packet at this time (see Figure 3-12). When an I/O device requests a read, write or ICB operation, depending on the device order code the associated controller responds to the request for service by sending instructions to the processor over the function code bus (4 of Figure 3-2). These instructions cause the processor to perform the desired operation. I/O controllers other than the IOC and multiplexer also send to the processor the address in memory where the data is to be read from or written into. These controllers maintain the packets until they are complete, whereupon they return all or part to the program.

In the case of the IOC and multiplexer, the packets are maintained in memory by the processor. They are updated by the processor under the direction of the IOC or multiplexer.

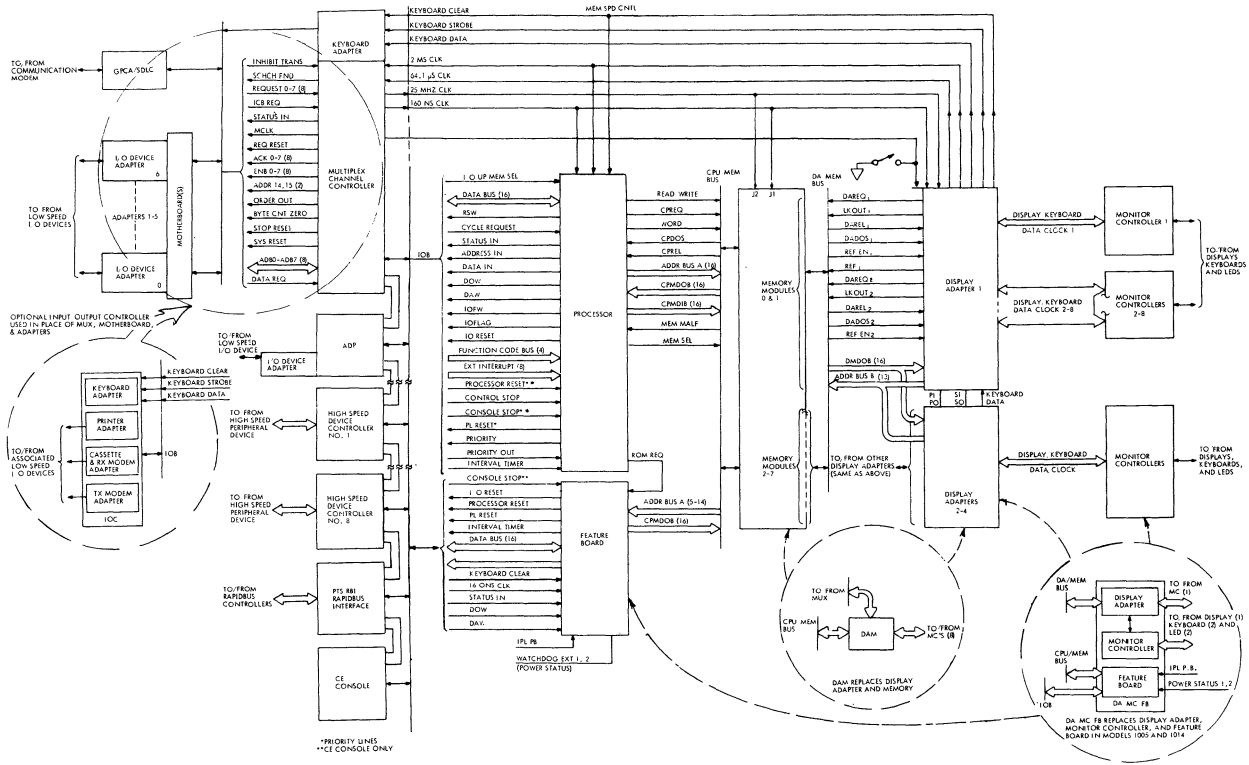

Figure 3-1. PTS-100 Input/Output System

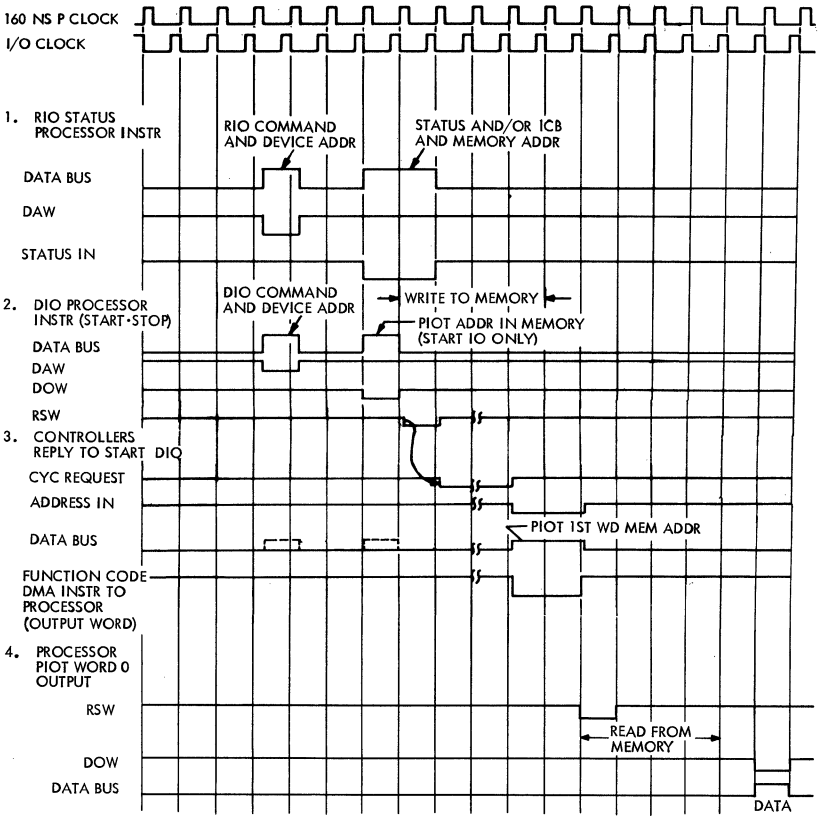

Figure 3-2. Processor Input/Output Interface Timing Diagram (Sheet 1 of 2)

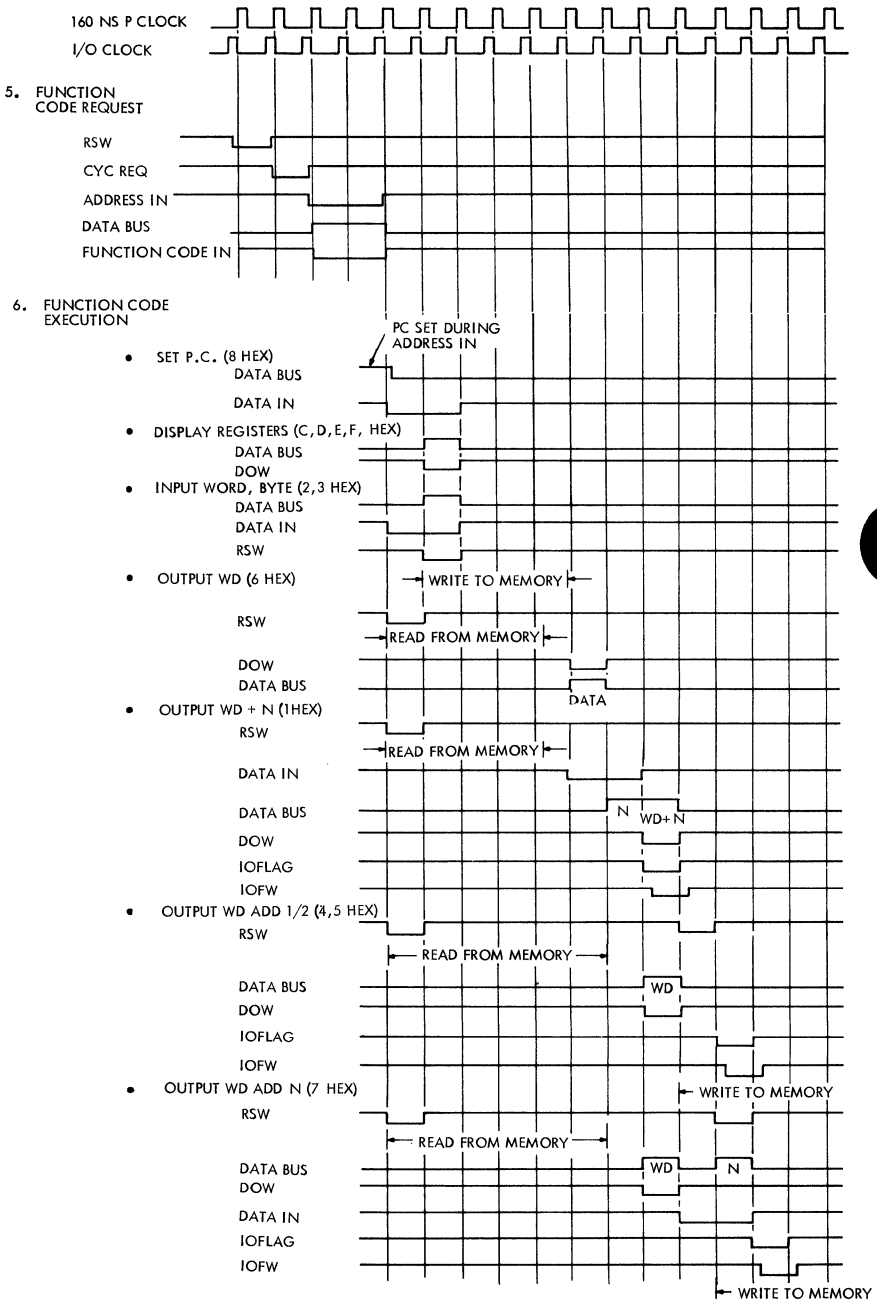

Figure 3-2. Processor Input/Output Interface Timing Diagram (Sheet 2 of 2)

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Table 3-1. Processor DMA Input/Output Bus Signals

SIGNAL (No. of Lines)	FUNCTION
DATA BUS (16)	A 16-bit bidirectional bus with bit 15 the LSB. It is used to transfer address and data between the processor and the controllers and feature board. When data is put onto the bus to be transferred to a controller, it is valid for one processor ALU cycle, or 160 ns. The data is accompanied by the DOW or DAW control signals. The controllers only put data on the bus for transfer to the processor when the data requesting control line (Status In, Address In, Data In) is active. These lines are active for two ALU cycles, or 320 ns.
FUNCTION CODE BUS (4)	A 4-bit bus used to carry controller instructions to the processor, with bit 0 the MSB of the function code. The function code is gated onto the bus when a device is selected and the Address-In control line is active. The various function codes are as follows:

Hexadecimal Function Code	Name	Function
1	Output Word 1N	Add the contents of memory to the value of word N sent to the processor by the controller. Output result to the controller. Do not disturb the value stored in memory. Output the ALU carry out for the addition.
2	Input Word	Input a word to memory.
3	Input Byte	Input a byte to the memory address specified by the controller during the address in.
4	Output Word, Add 1 to Memory	Output a word from memory to the data bus, then increment the word by 1 and put the new value back into memory. Output the ALU carry out for the addition.
5	Output Word, Add 2 to Memory	Same as 4 above except increment by 2.
6	Output Word	Output a word from memory.

Table 3-1. Processor DMA Input/Output Bus Signals (cont)

SIGNAL (No. of Lines)	FUNCTION

FUNCTION CODE (cont)

Hexidecimal Function Code	Name	Function
7	Output Word, Add N to Memory	Output a word from memory to the data bus, then increment the word by N (subsequently sent from the controller). Put the new value back into memory. Output the ALU carry out for the addition.
8	Set PC	Input a word to the program counter.
C	Display ACC	Output the contents of the accumulator register.
D	Display PC	Output the contents of the program counter.
E	Display X1	Output the contents of index register 1.
F	Display X2	Output the contents of index register 2.

CYCLE CONTROL

RSW — Request Start Window. Used by the processor to interrogate the controllers. Issued once during each memory access cycle.

CYCLE REQUEST — Used by the controllers to request service. This is the controllers reply to RSW when it desires service.

DATA IN CONTROL

STATUS IN — Issued by the processor during Read I/O status to instruct the addressed controller to put its status on the data bus to the processor.

ADDRESS IN — Issued by the processor. Instructs the controller to gate the function code onto the function code bus, and when appropriate to gate the memory location address or new program counter value onto the data bus.

DATA IN — Issued by the processor to gate the data from the controller onto the data bus to the processor.

Table 3-1. Processor DMA Input/Output Bus Signals (cont)

SIGNAL (No. of Lines)	Function
DATA OUT CONTROL	
DOW	Data Out Window. Notifies the controller that data is on the data bus waiting to be transferred to the controller.
DAW	Device Address Window. Notifies the controller that the device address is on the data bus.
IOFW	I/O Flag Window. Indicates to the controller that the I/O flag is valid for the arithmetic operation that the controller function code indicated.
IO FLAG	The IO Flag is the ALU carry out for the arithmetic operation performed by the processor for function codes 1, 4, 5 and 7.
2 MS CLK	Interval Timer. When enabled by feature board switches permits the processor to take a level 0 interrupt every 2 ms provided it is processing at level 0.
INTERRUPT BUS (8)	Eight lines from the controllers that alert the processor to controller events. They are part of the processor priority interrupt facility.
CONTROL STOP	From controllers that are not designed to respond to STATUS IN. Allows these controllers to stop the processor to input status via normal DMA operation.
PROCESSOR RESET	Resets processor under control of the CE console.
CONSOLE STOR	Stops the processor under control of CE console.
PL RESET	Program Load Reset. Initializes CE console concurrent with program load (IPL/RPL).
IPL PB OPEN/CLOS	Manual program load pushbutton on the operator panel.
KEYBOARD CLEAR	67 ms timing pulse used to clock optional watchdog timing interval, which is 512 67 ms pulses.
I/O UP MEM SEL	Not used by multiplexer or IOC. Used only by I/O controllers that transfer data a word at a time. When word address bit 15 is set, controller sets this line. Tells the CPU to raise either the upper or lower memory select line to the memory.

Table 3-1. Processor DMA Input/Output Bus Signals (cont)

SIGNAL (No. of Lines)	FUNCTION
WATCHDOG EXT 1, 2 (Power Status 1, 2)	Informs the processor via status bits 0 and 1 from the feature board of system power changeover to/ from battery pack.
INTERVAL TIMER	Generated on the feature board by Console Stop, Keyboard Clear, and the Interval Timer switch, sent to the processor 15 times per second for program control.
ROM REQuest	Sent to the feature board by the processor to initiate program load from the feature board IPL/RPL ROMs and configuration control switches(FB. A)or manual data chips (FB. B).
IO RESET	Generated from the processor under program load or from the CE console. Completely resets all I/O controllers.
PRIORITY (line)	Connected to all controllers in turn to determine their servicing priorities. Each controller has two priorities.

3.1.2.2 Read I/O Status (RIO). The Read I/O status instruction (1 in Figure 3-2) is issued to permit the program to determine the status of an I/O device. It can be issued at any time and it is followed by a write to memory operation, which writes the I/O device status and/or interrupt condition byte (ICB) into memory. Refer to paragraph 3.1.10 for the Read I/O instruction format.

3.1.3 Processor/Memory Bus

The PTS-100 memory is a two port dynamic MOS memory composed of 8,192 or 16,384 kilobyte modules. It must be refreshed every 2 milliseconds to maintain the data. The memory refresh, which is initiated by the display adapter, has priority over processor memory requests and display data refresh memory requests. All write to memory operations are performed over the processor/memory bus. The display adapter/memory bus is used only to read the display data from memory and to initiate memory refresh. The timing of the signals on the processor/memory bus in shown in Figures 3-3 and 3-4 and the signal functions are described in Table 3-2.

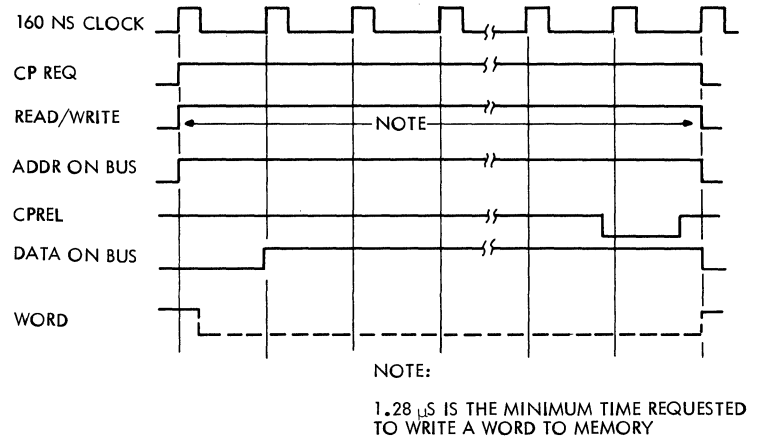


Figure 3-3. Processor Write to Memory Timing Diagram

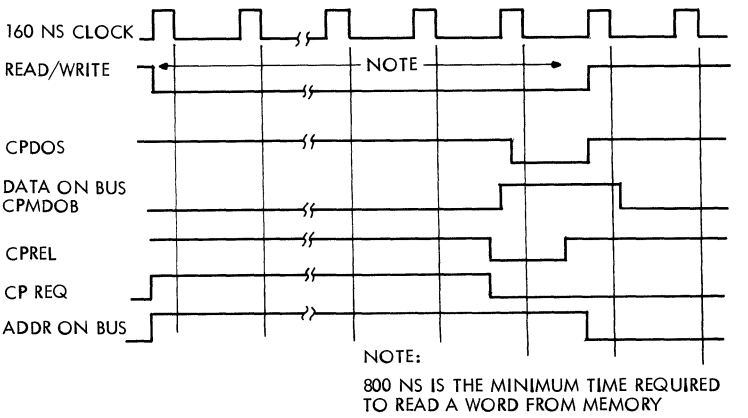


Figure 3-4. Processor Read From Memory Timing Diagram

Table 3-2. Processor/Memory Bus Signals

SIGNAL (No. of Lines)	FUNCTION
CPMDOB (16)	Processor memory data output bus. A 16 bit bus that carries the data read from the memory and the feature board program load memory to the processor. The memory location is specified by the address bus (ADDR BUS A).
CPMDIB (16)	Processor memory data input bus. A 16 bit bus that carries the data to be stored in memory from the processor to the memory.
ADDR BUS A (16)	Memory address bus A. A 16 bit bus that carries the memory address to be read from or written into from the processor to the memory and to the feature board. Line 15 specifies the right or left byte.
CPDOS	Processor data output strobe. Informs the processor that the requested data is on the memory data output bus (CPMDOB).
CPREL	Processor release. Informs the processor that the memory request operation has been implemented.
CPREQ	Processor memory request. Informs the memory that the processor desires a memory operation.
READ/WRITE	Tells the memory which type of memory operation (read or write) the processor desires.
WORD	Word store flag. Used to direct the memory to execute a word rather than a byte write operation. For a word operation address line 15 is ignored.
H0, H1	Hardwired memory board address assignments. Compared to address bits 0 and 1 to see if memory board in a particular slot is being addressed.
MEM SEL LOW MEM SEL UP MEM SEL	Memory select (J1-30). 16th memory address line. Generated by the processor to select either the upper or lower 64K bytes of memory. Comes from the processor LOW MEM SEL line (J1-62)

	for lower memory and from the processor UP MEM SEL line (J2-56) for upper memory. Initiated by I/O UP MEM SEL from the I/O controllers or by a backplane switch on 1018 and 1025.
MEM MALF	Memory malfunction. When active indicates that the memory detected a parity error (1018 and 1025 only). Generates an interrupt on level 10.

3.1.4 Display Adapter/Memory Bus

The display adapters attach directly to the memory. They transmit refresh data directly from memory to the external displays. They also initiate and control the memory refresh operation, serialize the keyboard data and couple it to the multiplexer channel controller via a keyboard adapter, and generate various clocks to synchronize the system. The timing for a display adapter read from memory operation is shown in Figure 3-5. The functions of signals on the bus are described in Table 3-3. The memory refresh timing is the same as that shown, except that the refresh line is active and there is no data output strobe (DADOS); therefore, no data is put on the DMDOB bus.

Table 3-3. Display Adapter/Mux/Memory Bus Signal

SIGNAL (No. of Lines)	FUNCTION
DMDOB0-DMDOB15 (16)	Display adapter memory data output bus. A 16 bit bus from the memory to the display adapter that carries the data from the memory location specified by the address bus. The data bus is common to all display adapters and memory modules. The data sent over the bus refreshes the data on the data display.
ADDR BUS B (2-14)	Memory address bus B. A 13-bit bus that carries the address of the memory location to be read from (refresh display data) or refreshed. The bus is common to all display adapters and memory modules. Lines 0 and 1 are hardwired on the backplane to define the memory module.
REF EN (1-8)	Refresh enable. An interlock line that informs the display adapter that the associated memory module is installed. It enables the display adapter to initiate memory refresh for the attached memory module.
REF (1-8)	Refresh. Activates the refresh circuits in the associated memory module and refreshes the memory words addressed by the address bus (ADDR BUS B).
DADOS (1-8)	Display adapter data output strobe. Informs the display adapter that the requested display refresh data word is on the memory output bus (DMDOB). There is one strobe line from each memory module.
DAREL (1-8)	Display adapter release. Informs the display adapter that the read from memory or refresh memory request has been implemented. There is one release line from each memory module.
DAREQ (1-8)	Display adapter request. Informs the memory that the display adapter wants a memory operation at the address on the address bus. The operation is either a memory refresh or a display data refresh. There is a request line to each memory module.

Table 3-3. Display Adapter/MUX/Memory Bus Signal (cont)

SIGNAL (No. of Lines)	FUNCTION
LKOUT (1-8)	Lockout. Inhibits the associated memory module circuits to the processor when the display adapter is using that memory module for either memory refresh or display data refresh. The 16K memory boards use LKOUT in place of DAREQ.
Other Lines to/from the Display Adapter	
PI, PO	Program in, program out and sync in, sync out.
SI, SO	These are interlock lines between each display adapter that determine which display adapter will provide the system clock and synchronize the display and keyboard timing.
2 MS CLK	2 millisecond clock. Used to time certain I/O devices. Used in the CE console for auto display.
64.1 μs CLK	64.1 microsecond clock. Used to time certain I/O devices.
160 NS CLK	Synchronizes the processor, memory, and display adapter to the low speed multiplexer.
KEYBOARD DATA	Serialized keyboard data from all attached keyboards.
KEYBOARD CLEAR	Synchronizes the keyboard adapter with active keyboards. Occurs every 67 ms.
KEYBOARD STROBE	Strobes the keyboard data bits into the keyboard adapter. Occurs every 64.1 μs.
DISPLAY/KEYBOARD DATA/CLOCK 1-8	Eight shielded twisted pair lines (per display adapter) that carry display refresh data and timing (frequency modulated) to the monitor controllers and keyboard data (amplitude modulated) to the display adapters. There is a twisted pair to each monitor controller.
MEM SPD CNTL	Memory speed control. Used on DAM. From a switch on the backplane and from the multiplexer. Low for 800 ns memories; when high memory speed is set by a switch on the DAM board that selects either 480 ns or 640 ns memory cycle times.

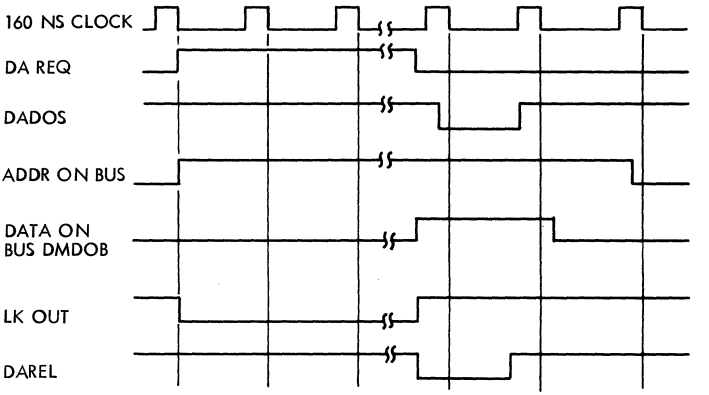


Figure 3-5. Display Adapter Read from Memory Timing Diagram

3.1.5 Multiplex Channel Controller / I/O Device Adapter Bus

All low speed I/O devices connected to I/O device adapters communicate with the processor over the multiplexer channel controller / I/O device adapter bus through I/O device adapters on subchannels of the multiplex channel controller. Each type of I/O device uses a different I/O device adapter. A keyboard adapter is connected to dedicated subchannel 7. It is used to enter the keyboard data, serialized by the display adapters, from all attached keyboards. The multiplexer subchannels are all half duplex. Two subchannels are used for full duplex I/O devices. The multiplex channels automatically execute control operations for the I/O devices under program initiation. They transfer data between the devices and memory, and perform code translation and code recognition under program intervention. The functions of signals on the multiplex channel controller / I/O device adapter bus are described in Table 3-4.

All input/output operations are initiated by the DIO and RIO status instructions from the processor. The multiplex channel controller-I/O device adapter timing for these operations is shown in Figure 3-6. The timing for a data transfer over the bus is shown in Figure 3-7, and the timing for an interrupt condition byte (ICB) transfer from the adapter to the multiplex channel controller is shown in Figure 3-8 (refer to Figure 4-10 for the data flow diagram).

Table 3-4. Multiplex Controller/I/O Device Adapter Bus Signals

SIGNAL (No. of Lines)	FUNCTION
ADB (8)	Adapter data bus. A bidirectional 8 bit bus that carries data between the multiplexer and the IO device adapters.
REQUEST 0-7 (8)	Request service. One line from each IO device adapter to the multiplexer. Informs the multiplexer that the associated adapter desires service. Each request is serviced on a priority basis with subchannel 0 having the highest priority. The request is either to set the interrupt control byte (ICB) or to transfer data.
CONTROL IN LINES	
DATA REQ	A single line to all IO adapters that informs the multiplexer that the current REQUEST is a data service operation (read or write). Gated out by ACK.
ICB REQ	Interrupt condition byte request. A single line to all IO adapters that informs the multiplexer that the current REQUEST is a set ICB, gated out by ACK.
INHIBIT TRANS	Inhibit translate. Inhibits the translating of the current data byte during translate orders.
ACK 0-7 (8)	Adapter acknowledge. One line to each IO device adapter to inform it that the multiplexer is servicing its REQUEST. Remains active all during the time the adapter is being serviced.
ENB 0-7 (8)	Adapter enable. One line for each IO device adapter that directs it to sample the control out lines.
CONTROL OUT LINES	
STATUS IN	A single line to all IO adapters that directs the adapter to put its device status byte onto the data bus (ADB). It is coincident with the ENB signal.

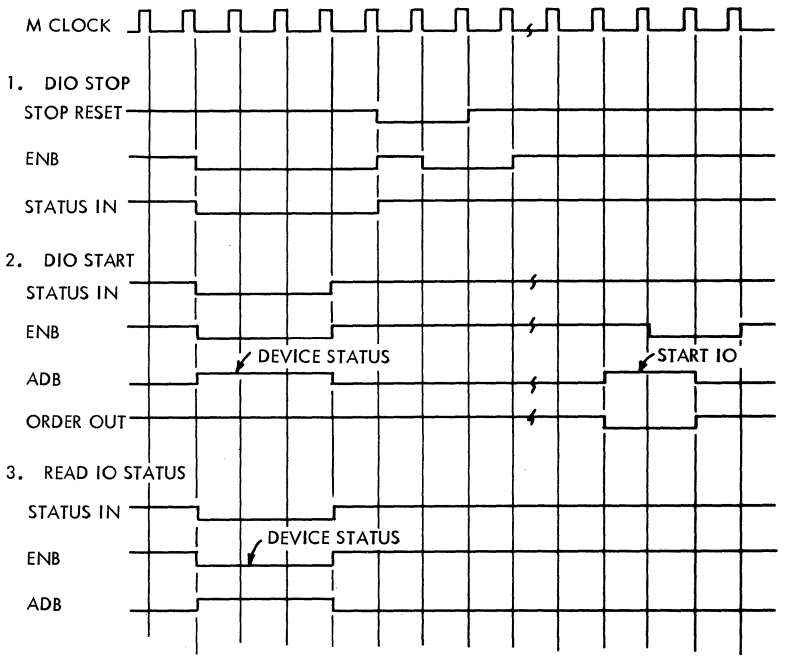


Figure 3-6. Multiplex Channel Controller - Input/Output Device Adapter DIO and RIO Status Timing

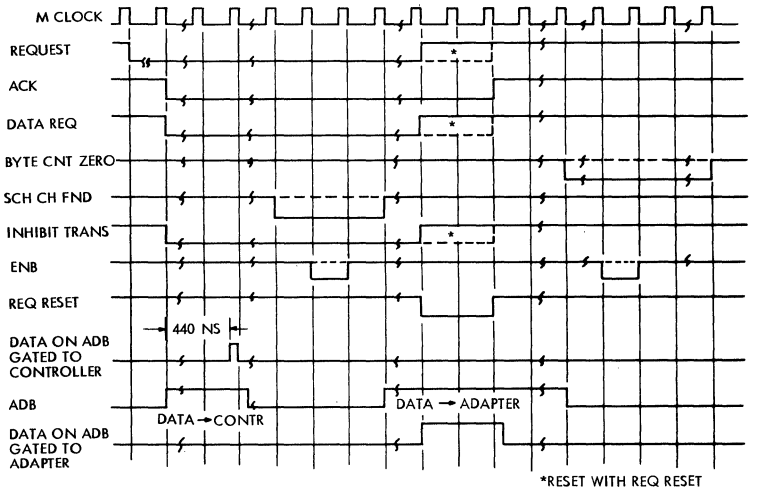


Figure 3-7. Multiplex Channel Controller - Input/Output Device Adapter Data Transfer Timing

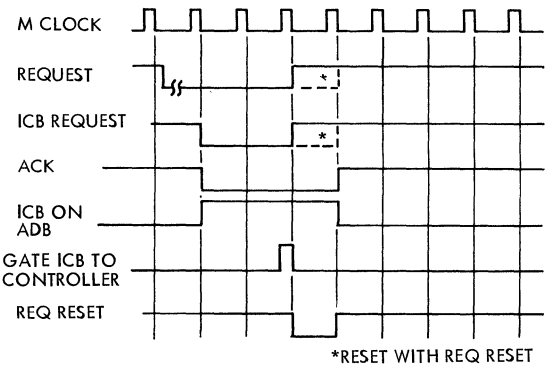


Figure 3-8. Multiplex Channel Controller — Input/Output Device Adapter ICB Transfer Timing

3.1.6 Rapidbus

Refer to Raytheon documents 44-10147 and 44-7669 for a description of this bus.

3.1.7 Channel Interface Controller/360 Bus

Refer to channel Interface Controller circuit description in Chapter 3, Section 2.

3.1.8 Priority Interrupt Facility

The priority interrupt facility of the PTS-100 is composed of the following:

- A multilevel interrupt system permitting user-assigned interrupt handling priorities.
- A set of machine instructions to enable and disable interrupts, trap to higher interrupt levels, and return to prior levels when pending interrupts are serviced.
- Either the Input/Output Control System (IOCS) monitor, an RDS-supplied software system to service external interrupts from I/O devices and trap calls from executing programs; or two machine instructions (Do I/O and Read I/O Status) which may be employed by users who wish to design and implement special systems programs in which input/output control capabilities are incorporated.

The components of the priority interrupt facility are described in the following paragraphs.

3.1.8.1 Interrupt Levels. There are eleven interrupt levels, eight of which are external (device) interrupt levels, and three of which are internal (processor) interrupt levels. The processor operates at a given level and may be interrupted when a higher priority interrupt condition is detected. The interrupt priority levels are illustrated in Figure 3-9, with the highest numbered level having the highest priority.

10	PARITY
9	TRAP
8	EXTERNAL 8
7	EXTERNAL 7
6	EXTERNAL 6
5	EXTERNAL 5
4	EXTERNAL 4
3	EXTERNAL 3
2	EXTERNAL 2
1	EXTERNAL 1
0	PROCESSOR/INTERVAL TIMER

Figure 3-9. Interrupt Priority Levels in the PTS-100

For each interrupt level, an associated four-word interrupt packet must be set up in the format shown in Figure 3-10. When the processor is operating at one interrupt level and an interrupt of a higher priority is detected, the processor completes the execution of the current instruction, then saves the current (old) counter value, the current (old) interrupt level and condition bit (CB), and the new program counter value in the interrupt packet. When this is accomplished, the new interrupt level is entered and the interrupt is serviced. If an interrupt of a higher priority occurs during the above saving procedure, its servicing is deferred until one processor instruction is executed at the interrupt level that caused the saving procedure to be entered. A second saving procedure is then performed, and the new higher priority interrupt is serviced. Specific processor actions for interrupts occurring at the eleven levels are described in the following paragraphs.

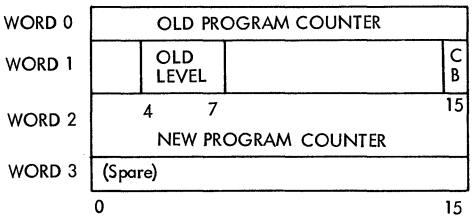


Figure 3-10. Interrupt Packet Format

The Parity Interrupt is optional. It occurs when the processor hardware detects invalid parity on the data return from memory. When the current instruction being executed is completed, the interrupt is serviced and level 10 is entered.

The Trap Interrupt is a synchronous interrupt which occurs when the Monitor Service Call (MSC) machine instruction is executed. A trap interrupt may be issued at any interrupt level. It is not maskable. When a trap interrupt occurs, the present processor status is stored, the program counter from the level 9 interrupt packet is loaded, and execution begins at level 9.

The eight External Interrupt levels (levels 1 through 8) may be assigned to any configuration of input/output devices. Interrupt level assignments are specified to the System Generator program, which is used to create uniquely tailored IOCS monitors for specific users. Typical interrupt level assignments of various types of devices used on the PTS-100 are as follows:

Interrupt Level	Device Type(s) Assigned
1	(unassigned)
2	Card Readers, Cassette Tape Devices, ASR Teletype Devices, Paper Tape Readers and Punches, Serial Printers
3	Display/Keyboard Devices
4	Communication Transmission Devices
5	Communication Receive Devices
6	(unassigned)
7	(unassigned)
8	(unassigned)
9	(unassigned)
10	Memory Parity Error

The Processor Interrupt level 0 does not have the ability to interrupt execution at any other level. That is, level 0 may be entered only by the execution of the Interrupt Return machine instruction with no higher interrupts pending. Applications object programs operate at level 0.

The Interval Timer Interrupt is an optional external interrupt condition which occurs once every 67 milliseconds. The interrupt may be taken only when the processor is already operating at level 0 with the external interrupts enabled. The interrupt causes present status to be stored, the program counter to be loaded, and processing to continue at level 0.

The processor may be operating at any of the eleven interrupt levels and is normally enabled for external interrupts that occur at a higher priority level than the current operating level. The trap and parity interrupts are always enabled. Interrupts of the same or lower priority than the current operating level remain pending. All external interrupts may be disabled

(held pending) by the execution of the Disable Interrupts machine instruction. The processor returns to the enabled state when the Enabled Interrupts machine instruction is executed.

3.1.8.2 Interrupt Handling Instructions. Machine instructions are provided to enable and disable interrupts, trap to a higher interrupt level, and return to a prior level after the current interrupt is serviced. These instructions are:

- Disable Interrupts (DIN) instruction causes all interrupts from level 0 through 8 to be disabled, or held pending, so that current instruction execution cannot be interrupted.
- Enable Interrupts (ENB) instruction causes all interrupts at levels higher than the current operating level to be enabled, or serviced, when they occur.
- Interrupt Return (INR) instruction causes the processor to return to the interrupt level at which it was operating just prior to the occurrence of the most recent interrupt.
- Monitor Service Call (MSC) instruction causes a software initiated trap interrupt at level 9, which is typically serviced by the IOCS monitor in response to user program requests for I/O operations.

3.1.8.3 Interrupt Servicing. PTS-100 interrupt servicing uses software routines to queue interrupts for priority processing; switch from one processing level to another; issue hardware commands to the I/O devices; receive, interpret, and process external device interrupts; etc. For the standard PTS-100 equipment configuration, RDS supplies a modular software Input/Output Control System (IOCS) that is specifically designed to service the interrupts and provide the necessary interface between the standard external I/O devices, the processor, and executing object programs requiring external device input/output.

For PTS-100 systems with standard I/O devices, a hardware-specialized IOCS monitor is created via the System Generator program. That is, physical device addresses, interrupt level assignments, and copies of the required portions of the IOCS monitor are combined to form a unique monitoring system for the user.

For PTS-100 installations in which nonstandard device types are combined with standard types, the user may alter the monitor by defining and incorporating it in the necessary special physical I/O and control routines to accommodate the nonstandard devices. That is, for nonstandard devices the user may define macro routines into the IOCS monitor being generated for his installation.

For PTS-100 installations that have mostly or only nonstandard devices, the user may develop his own IOCS monitor by using the interrupt handling instructions and the Do IO (DIO) and Read IO status (RIO) machine instructions.

3.1.9 Do I/O - Initiating Activity on the Input/Output Bus

PTS-100 input/output operations occur via direct access channels. Data, addresses, and status information are exchanged between the processor and various device controllers across a 16 bit bidirectional data bus. The I/O controllers may initiate data transfers between their attached devices and memory, and they may also initiate limited arithmetic operations to be performed by the processor. These actions are multiplexed with processor instruction executions, with I/O memory requests taking precedence over processor memory requests.

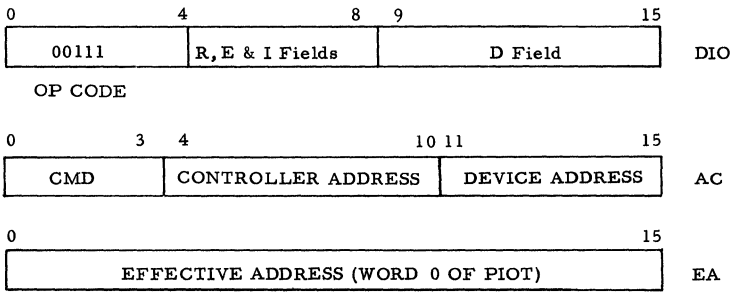
All I/O activity is initiated by execution of the Start Do I/O instruction. This instruction is usually preceded by a Load Word (LDW) instruction to bring the desired device address into the accumulator register. Once this address is in the accumulator, the three-step Do I/O instruction is executed.

In the first step, the device address and command (CMD) in the accumulator are placed on the data I/O bus, and the device address window (DAW) control line is raised, telling all controllers to sample this information to see if they are being addressed.

After this, the processor computes the effective address of the first word of the PIOT table for the addressed device. It does this in the same manner as it would for any effective address; however, instead of the computed address being used to fetch a word from memory, it is placed on the I/O bus for use by the addressed controller.

Effective addresses are computed within the processor by taking the Operand of the Do I/O instruction, and using it as a base address to which the value of the PC register or index register 1 or 2 is added to create the desired memory address directly; or it may be used as an indirect address to tell where in memory the desired address may be found. When these computations and/or memory access operations are completed, the processor places the computed EA on the data bus, and raises the DOW line. At that point, the previously addressed controller accepts the EA while all other controllers ignore it.

The format of the DIO instruction is shown below.



Refer to paragraphs 3.2.1.4 through 3.2.1.6 for an explanation of the DIO format.

AC bits 4-15 specify the physical address of the device and AC bits 0- 3 specify one of the following:

CMD = 0_{16} specifies that an IO operation is to start

CMD = 1_{16} specifies that the IO operation is to stop

If CMD = 1_{16} when the DIO instruction is executed, the addressed device will be stopped as soon as possible and all pending or active memory requests from the device will be cleared. The I/O controller for the device will left in the Not Busy state.

If CMD = 0_{16}, the DIO instruction specifies the starting address of an I/O packet containing all information necessary for executing the I/O operation.

Controller Address

Bits 4 through 10 address the specific controller on the I/O channel to which the DIO action is directed.

Subchannel Address

Bits 11 through 13 select a specific subchannel of the controller.

Device Address

Bits 14 and 15 select a specific peripheral if the subchannel drives more than one (used in GPCA, disc, and cassette tape adapters).

After the addressed controller receives the EA, it waits for the next opportunity to gain access to memory and request the first word of the PIOT table. This opportunity will occur when the processor next raises its RSW line (Request Start Window), at which time the controller(s) desiring service will answer by raising its (their) Cycle Request line, requesting access to memory. If no other higher priority controller has also raised its cycle request line, the controller will be able to gate its memory address (the EA previously received) into the processor upon receipt of the Address In control signal. This normally immediately follows the cycle request response.

At the same time that the controller places its EA on the data I/O bus, it must also place a function code on a function code bus to direct the processor in the action to be taken with respect to the designated memory address. In this case the function code would be to "output word." The processor would then prepare to output the requested word.

Three steps are required. First, the processor raises the RSW window again, to see if any other controller is waiting for memory (or to see if this controller has another request). If other controllers are waiting, they will be given access immediately after the completion of this operation. If there are none waiting, the processor will be free to resume internal processing operations after completion of this I/O action.

After the RSW line has been raised and lowered (and response to it noted), the processor will extract the desired word from its memory and perform any necessary arithmetic operation on the word (in this case none). Finally, the processor will output the desired word (first word of the PIOT table) to the controller, and at the same time raise its DOW line.

After receiving this word, the controller extracts the order code from it, and sends instructions (based upon the order) to the input/output device. No further operations will occur across the data bus until the device itself requests action by stating that it is ready to start the desired operation (e.g., ready to receive). At that point the operations described in the following paragraphs will occur.

3.1.9.1 Input Word Operations. The following steps describe the sequence of events necessary for the multiplex channel controller to input a word to the PTS-100 memory. The sequence is illustrated in Figure 3-11. It does not consider search and/or translate operations which, if required, are performed before and in addition to these operations.

1. Processor raises RSW line (to see if a controller wants service)

2. Multiplex controller responds by raising its cycle request line (requests service)

3. Processor raises Address In line (tells controller to put memory address on bus)

4. Controller places address of word 1 of PIOT table on bus, and function code 4 on function code bus (requests word from specified memory location).

5. In preparation for complying, processor raises RSW line again (will there be another memory request following this one?).

6. Controller has cycle request line still raised, since this is a multi-step operation.

7. Processor places address of requested word in its memory address register (which it fetched from PIOT), reads out selected word through memory output register and processor ALU circuitry, and places word on data I/O bus, at the same time raising the DOW control line.

8. Since a function code 4 had been requested, processor also places word in accumulator register and adds '1' to it, thus increasing buffer byte address by one.

9. Data overflow, if any, from this operation is read out of accumulator and placed on IO flag control line, followed by IO flag window control signal, stating that there is a bit on the IO flag line.

10. Processor raises Address In line again (since there was another cycle request).

11. Controller responds by sending back to processor the buffer address word it just received, and placing function code 3 on function code bus.

12. Since function code 3 specifies that a word is to be written into memory, processor responds by raising Data In.

13. Controller responds by placing input data byte on bus.

14. In preparation for complying with write memory request, processor raises RSW line again.

15. Controller raises cycle request line again, since this operation has more steps.

16. Processor now places input data byte into memory location specified by buffer address.

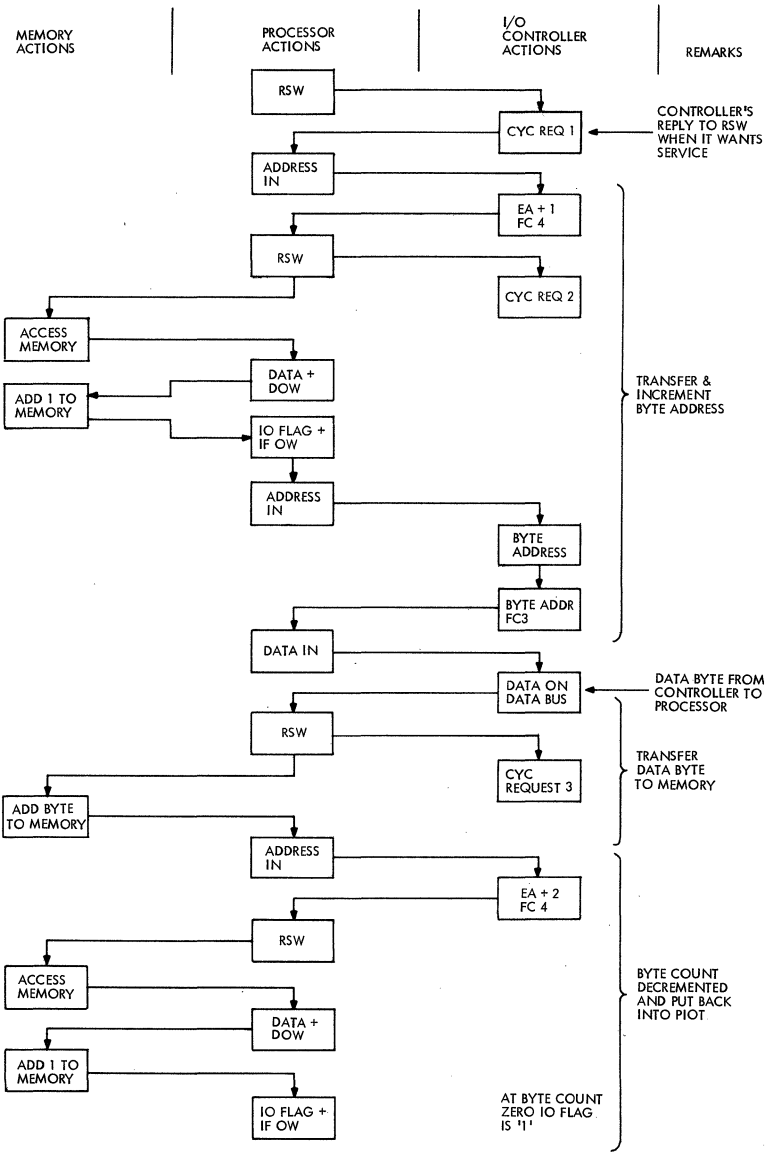


Figure 3-11. Typical Byte Transfer from Controller to Memory

17. Processor follows this with another Address In (requests next memory address).

18. Controller responds by placing address of word 2 of PIOT table (byte count) on bus, and function code 4 on function code bus.

19. In preparation for complying with another memory access request, processor once again raises RSW line.

20. Since this is last step of sequence, controller has cycle request line down.

21. Processor enters memory for desired word, and reads it out on data input/output bus, with DOW control signal.

22. Processor also places word in accumulator register and adds '1' to it (function code 4), thus in effect decrementing byte count.

23. Data overflow (caused by byte count zero), if any, from this operation is read out of accumulator and placed on I/O flag control line, followed by an I/O flag window control signal, stating that there is a bit on the line.

24. Controller checks for I/O flag (signifying byte count zero) and, if present, checks for chaining operations.

3.1.9.2 I/O Packet. When I/O operations are being performed independently of the IOCS monitor, the I/O packet specifies the input/output function to be performed on the device, the data storage area to or from which data is to be transferred, the total number of bytes of data involved in the transfer, and the base addresses of any Search or Translate tables to be used in the operation. A typical I/O packet format is shown in Figure 3-12.

Different devices (such as CIC and disc) use different I/O packet formats. The discussion below is based upon the typical PIOT format of Figure 3-12.

Order Byte

The Order Byte field of the I/O packet contains the device controller order code (COC) in bits 0 through 2, and the device order code (DOC) in bits 3 through 7.

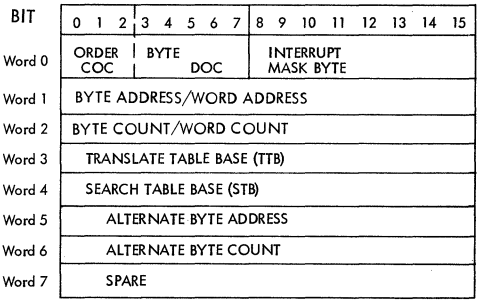


Figure 3-12. I/O Packet (PIOT) Format

The controller order code specifies the Search and Translate function performed by the I/O controller, using the current input/output character passing through the controller as an offset from corresponding byte table base addresses specified in words 3 and 4 of the I/O packet. The controller order codes are defined in Table 3-5.

The device order code (DOC) in bits 3-7 of the Order Byte specifies the desired I/O function to be performed on the specific device. Bit 3 specifies chaining. The device order codes vary with each I/O device. Refer to Table 3-6 for the order codes.

Table 3-5. Controller Order Codes

Code Bits 0, 1, 2 Octal	Operation
0	No search or translate
1	Translate with no interrupt condition when MSB is on. Use Translate Table Base (TTB)
2, 3, 4	Unassigned
5	Translate with interrupt condition when MSB is on, i.e., Search and Translate through a common table. Use only Translate Table Base (TTB) specified in I/O packet.
6	Search and set interrupt condition when MSB is on; i.e., Search only and use the Search Table Base (STB) specified in the I/O packet.
7	(6) above followed by (1) above using separate table base for each (STB then TTB). Use current character for offset on both.

Interrupt Mask

The Interrupt Mask in the right-hand byte of Word 0 of the I/O packet is used to allow or inhibit interrupts; that is, the bits of the Mask Byte correspond one-for-one with the bits in the Interrupt Condition Byte (ICB) in the device controller. Hence, a one bit may be set in each position of the Interrupt Mask Byte where the corresponding interrupt is to be allowed, and a zero bit may be set in each bit position where the corresponding interrupt is to be inhibited. When an interrupt condition occurs in the device controller, the Interrupt Mask is fetched and ANDed with the ICB to determine whether an interrupt should be generated. The ICB and interrupt condition will remain on until Read and Reset Interrupt Status RIO instruction is executed, whereupon both the ICB and interrupt condition are reset (only if an interrupt condition is pending). The Interrupt Mask and ICB bytes are listed below:

Interrupt Mask

Bit 0 = Search requested and MSB = 1

Bit 1 = Byte count incremented to zero

Bit 2 = Start issued while not ready (see device status below)

Bit 3 = Device "End of Record" (EOR)

Bit 4 = Attention

Bit 5 = Error (data overrun, data error, or unit check generated by device)

Bit 6 = Carrier lost (modems); top-of-form (printer) other devices unassigned

Bit 7 = Unassigned

Byte Address/Word Address

Word 1 of the I/O control packet specifies the address of the first byte or word of memory storage area into or from which input/output data is to be transferred. Bit 15 of the address specifies upper (64K - 128K) or lower (0 - 64K) memory.

Byte Count/Word Count

Word 2 of the I/O packet specifies the two's complement of the total number of bytes or words of I/O data to be transferred. The count is incremented each time a byte or word of data is transferred by the I/O controller. When the count reaches zero, the data transfer is complete.

Search and Translate

The search table in memory consists of one byte location associated with each possible character code being processed by the controller. As each data byte passes through the controller, the address of that character's associated byte in the search table is calculated. The controller looks at the character's associated byte in the search table in memory to determine if the current character byte is being sought. It is used in the GPCA, for example, to detect that an end of message (EOM) character has been received.

The most significant bit (MSB) of the search table byte associated with a character code being sought will be set to a one. If the controller finds that the MSB of the search table byte associated with the current character code is set, the controller will attempt to generate an interrupt. The interrupt mask will determine if the interrupt is generated or inhibited. The controller calculates the search table address of any character code being transferred by summing the binary value of the actual character code with a search table base address value. The sum of the character code and table base will be the memory byte address of the search table byte associated with that specific character.

Example: A seven bit character code can have a maximum of $128_{(10)}$ different binary values (0000000 through 1111111). Assume that the specified search table base is byte address $0500_{(10)}$. The search table for the seven bit code would occupy all byte locations between locations $0500_{(10)}$ and location $0627_{(10)}$. The summation of any possible seven bit code plus $0500_{(10)}$ will result in a sum between $0500_{(10)}$ and $0627_{(10)}$. The MSB being set in any byte location of the search table will cause the controller to attempt to generate an interrupt when the character code associated with that byte location is transferred to or from memory if the search function is specified in the Controller Order Code field of word 0 of the I/O control packet.

Translate is an operation performed by the controller using a translate table contained in memory. It may be used to convert one set of character codes to another. Specifying the translate operation in the Controller Order Code field of the I/O control packet causes the controller to process a sequence that will translate each character code being transferred to or from memory.

Table 3-6. I/O Device Order Codes

Device	Function	Device Order Code
		Bit 3 4 5 6 7
Card Reader	Read Hollerith	C 0 1 0 0
	Read Binary	C 0 0 0 0
Teletype and Printers	Read	0 0 0 0 0
	Write	0 0 0 0 1
Cassette	Read	0 0 0 0 0
	Write	0 0 0 0 1
	Backspace	0 0 0 1 0
	Rewind	0 0 0 1 1
	Erase	0 0 1 0 1
Paper Tape Punch	Output Data	0 0 0 0 1
Paper Tape Reader	Input Data	C 0 0 0 0
Display Keyboard	Read	C 0 0 0 0
Model 2331 Modem Adapter	Start Receive (look for sync)	C 0 0 1 0
	Continue Inputting Received Data	C 0 1 1 0
	Check CRC Character	C 0 1 0 0
	Start Transmit - No CRC Transmitted at Byte Count Zero	C 0 0 0 1
	Start Transmit - CRC Transmitted at Byte Count Zero	C 0 1 0 1
	Continue Transmit - No CRC Transmitted at Byte Count Zero	C 1 0 0 1
	Continue Transmit with CRC Transmitted at Byte Count Zero	C 0 1 1 1
	Transmit Idles	C 0 0 1 1
	Send New Sync Pulse	C 0 0 0 0
Models 2332, 2333, 2334* Modem Adapters	Start Receive (look for sync)	C 0 0 1 0
	Continue Inputting Received Data	C 0 1 1 0
	Stop Receive	C 0 1 1 1
	Start Transmit	C 0 0 0 1
	Transmit Idles	C 0 0 1 1
	Stop Transmit	C 0 1 0 1
	Send New Sync Pulse	C 0 0 0 0
Model 2341* Modem Adapter	Prepare	C X 1 0 0
	Receive	C X X 1 0
	Stop Receive	C X 1 1 1
	Transmit	X X 0 0 1
	Break	X X 0 0 0
	Stop Transmit	C X 1 0 1
	Transmit Idles	C X 0 1 1

(C = chaining; X = immaterial; - = not used)

*Also used with Modem Adapter Model GPCA as applicable.

Table 3-6. I/O Device Order Codes (cont)

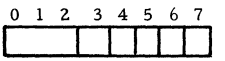
Device	Function	Device Order Code
Channel Interface Controller	Transmit Status	-1000
	Translate & Transmit to 360	-0110
	Transmit to 360	-0010
	Receive from 360	-0001
	Receive from 360 & Translate	-0101
Disc Controller Diablo	Write Data	00001
	Read Order	00010
	Seek	00011
	Compare Data	00100
	Write Address	00101
	Read Address	00110
	Recalibrate	00111
Disc Controller SMD	See Raytheon document 44-10141 with supplement	
Parallel	Write Data	00001
Adapter	Write Control	10001
SDLC	Continue Receive	-0000
	Search for Flag	-0010
	Search for Flag and Address	-0100
	Continue Transmit	-0001
	Transmit Frame	-0011
	Transmit Frame Check Sequence	-0101
	Transmit Flags	-1001
	Transmit Abort	-1011
	Clear Request to Send	-1101
	Load Microcode	-1111

(C = chaining; X = immaterial; - = not used)

Table 3-6. I/O Device Order Codes (cont)

ADP ORDER CODES

ORDER CODE BYTE



CODE BITS 0, 1, 2 (Octal)	OPERATION
0	Move
1	Translate with NO interrupt condition when MSB is on. Use Translate Table Base (TTB).
5	Translate with interrupt condition when MSB is on, i.e., Search and Translate through a common table. Use only Translate Table Base (TTB) specified in I/O Packet.
6	Search and set interrupt condition when MSB is on, i.e., Search only and use the Search Table Base (STB) specified in the I/O Packet.
7	(6) above followed by (1) above using separate table base for each (STB then TTB). Use current character for offset on both.
3, 4	
00	Move data from lower memory to lower memory
01	Move data from lower memory to upper memory
10	Move data from upper memory to lower memory
11	Move data from upper memory to upper memory
5	0-Increment both read and write byte addresses 1-Decrement both read and write byte addresses
6	0-Normal Move 1-Diagnostic ADP Stack Transfer
7	0-Normal Interrupts 1-Inhibit Interrupts

Table 3-6. I/O Device Order Codes (cont)

EXTENDED ORDER CODE BYTE

PKT WD4	0	1	2	3	4	5	6	7

CODE BITS	OPERATION
0	0-TTB in lower memory 1-TTB in upper memory
1	0-STB in lower memory 1-STB in upper memory
2	0-CRC before Translate 1-CRC after Translate
3	0-Normal move 1-Calculate CRC, put result in 7th word of I/O Packet (overwrites the test/mask word).
4	0-Normal move 1-Move with Mask and Test

5, 6, 7 (Octal)

0	Normal move
1	Read data, or with test byte, result in memory
2	Not defined
3	Read data, and with test byte, result in memory
4	Not defined
5	Read data, XOR with test byte, result in memory

Magnetic Tape Controller

Read Mode	000
Rewind	001
Drive Off Line	010
Space Forward One Record	011
Space Back One Record	100
Write	101
Write File Mark	110
Erase Gap Forward	111

The translate table in memory consists of one byte location associated with each possible character code being processed by the controller. As each data byte passes through the controller the address of that character's associated byte in the translate table is calculated. Each byte location in the translate table will contain the translated data code for its associated character code being processed by the controller. The controller reads the contents of the calculated address in the translate table and inputs or outputs this data in place of the original data transferred to the controller. The associated byte address in the translate table for each character code is calculated in the same manner as that described for determining addresses in the search table.

If the translated codes in the translate table are 7 bits or less in length, the same table can be used for both search and translate. The search table uses only the MSB and does not use the least significant 7 bits. Refer to Table 3-5 for the Controller Order Codes.

Alternate Address and Byte Count

Words 5 and 6 of the I/O packet are used to specify the alternate data storage address and byte count when I/O orders are chained. Order chaining is specified by a one in bit 3 of the Device Order code. When chaining is specified, the I/O controller executes the first order specified by the DOC and uses the byte address and count located in words 1 and 2 of the I/O packet. Data transfer is halted when the byte count in word 2 reaches (is incremented to) zero. When the next I/O order is executed, the I/O controller uses the alternate address and byte count specified in words 5 and 6 of the packet. Subsequent sets of chained orders may be issued by resetting the byte addresses and counts in the I/O packet. As chained orders are subsequently received, the controller again alternates between the byte addresses and counts. Odd numbered orders use words 1 and 2 of the packet, and even numbered orders use words 5 and 6 of the packet. Order chaining continues until a device order with bit 3 set to zero is executed or until a Stop I/O is issued. Chaining is not provided in some controllers (e.g., the disc).

3.1.10 Testing I/O Device Status on the IOB

The Read I/O Status (RIO) machine instruction is used to test the operational status (see Table 3-7) of the I/O devices attached to the PTS-100. It is used in conjunction with the accumulator which specifies the command code and the physical address of the device whose status is to be checked. The format of the RIO instruction is shown below.

Table 3-7. Status and ICB Bit Assignment

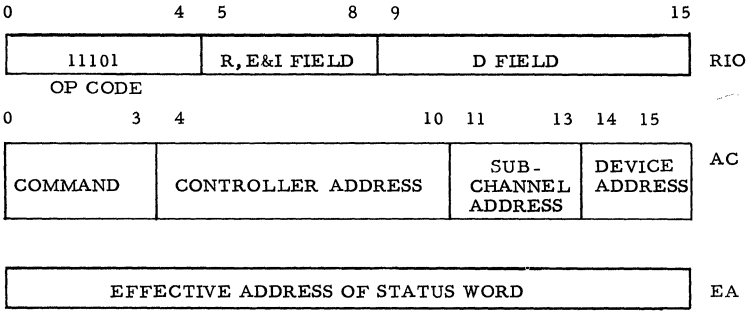
Device	Bit Number	Status Bit Function	ICB Bit Function
Card Reader Adapter	0	Ready	
	1	Busy	
	2	Hopper Check	
	3	Error	EOR
	4	Motion Check	Attention
	5	Data Overrun	Error
	6	Unassigned	
	7	Unassigned	
IPARS Modem Adapter	0	Ready	
Transmit	1	Busy	
Status Word	3		EOR or Data Rate Error
	5	Idles	Overrun
Receive	0	Ready	
Status Word	1	Busy	
	3	CRC Error	EOR or CRC Error
	4	Data Rate Error	Data Rate Error
	5		CRC Error/Overrun
Low Speed Serial	0	Ready	BCZ
Adapter	1	Busy	Invalid OP
	2	Framing Error	
	3	Overrun	
Cassette Adapter	0	Ready	
	1	Busy	
	2	Write Not Permitted	Start While Busy
	3	EOT/BOT	EOR
	4	Cassette Not Loaded	Attention
	5	CRC Error	CRC/Data Overrun Error
	6	Data Overrun	
	7	Not Used	
Channel Interface	0	Ready	Invalid Command
Controller	1	Busy	Command While Busy
	2	-	Parity Error
	3	-	Halt I/O
	4	-	Selective Reset
	5	-	EOR
	6	-	BCZ
	7	-	Command While Off Line
	11	Initialization Complete	-
	12	Turnble Table Interrupt	-
	15	System Reset	-
MISA Adapter	0	Ready	Search Hit
	1	Busy	BCZ
	2	Demand	Start While Busy
	3	-	TX EOR
	4	-	Malfunction
	5	-	TX Error
CTMC/2848	0	Ready	
Modem Adapter	1	Busy	
Transmit	3	-	EOR
Status Word	5	Idles	Overrun
Receive	0	Ready	
Status Word	1	Busy	
	2	Parity Error	Parity Error
	4	Data Rate Error	Data Rate Error
	5	-	Parity Error/Overrun
	6	-	No Carrier
Disc File Controller	0	Ready	Drive 0 Attention
Diablo	1	Busy	Drive 1 Attenation
	2	Operator Intervention Required	Drive 2 Attention
	3	Seek Incomplete	Drive 3 Attention
	4	Format Error	Drive 4 Attention
	5	CRC Error	Drive 5 Attention
	6	Rate Error	Drive 6 Attention
	7	Spare	Drive 7 Attention
	8	Spare	Attention Controller Ready
	9	Spare	Spare
	10	Start I/O While Busy	Start I/O While Busy
	11	Seek Complete	Seek Complete
	12	Byte Count Zero	BCZ
	13	End of Track	EOT
	14	Non-Compare	Non-Compare
	15	Summary Error	Summary Error
Disc Controller SMD		See Raytheon document 44-10147 with supplement	

Table 3-7. Status and ICB Bit Assignment (cont)

Device	Bit Number	Status Bit Function	ICB Bit Function
High Speed Paper Punch Adapter	0	Ready	
	1	Busy	
	2	Error	
	3	Tape Out	
Paper Tape Reader Adapter	0	Ready	
	1	Busy	
	2	Error	
Asynchronous Modem (AMAPL)	0	Ready	
	1	Busy	
	2	Parity Error	Parity Error
Receive Status Bits	3	Framing Error	EOR/Framing Error
	4	Overrun	Attention/Data Rate Error
	5	Wake Up Character	Data Error
	6	Receive Spacing Signal	No Carrier
Transmit Status Bits	0	Ready	
	1	Busy	
	3		EOR
Parallel Adapter	0	Ready	
	1	Busy	
			EOR
	3	Manually entered	
	4	Program Flags	Malfunction
	5	That Identify the I/O	
	6	Device Type (e.g., 0001 for Printer 2230)	Parity Error TOF
ADP	0	Ready	Search requested and MSB - 1
	1	Busy	Byte Count incremented to 0
	2		Start issued while not ready
	3		Move mask and test requested and one or more, but not all of the unmasked bits compare
	4		Move mask and test requested and all of the unmasked bits are equal
	7		Diagnostic ADP stack transfer complete
SDLC (REC)	0	Ready	Search Hit
	1	Busy	BCZ
	2	No Data	Start and Not Ready
	3	FCS Error	End Of Frame
	4	Carrier	Maintenance Or Carrier Lost (STOP) Or Overrun
	5	Maintenance	---

Table 3-7. Status and ICB Bit Assignment (cont)

Device	Bit Number	Status Bit Function	ICB Bit Function
	6	Sig. Quality	Abort Received
SDLC (TX)	0	Ready	Search Hit
	1	Busy	BCZ
	2	---	Start and Not Ready
	3	---	Frame Check Seq.
	4	---	---
	5	Xmittings Flags	Underflow
	6	---	RTS Cleared Or Abort
	7	Load Microcode Error	Load Microcode
Magnetic Tape Controller	0	Ready	-
	1	Busy	-
	2	PE(1600 BPI) SEL	-
	3	HD(NRZI Only)	-
	4	File Protect	-
	5	Rewinding	-
	6	9 Track Drive	-
	7	Odd Length Record	-
	8	-	Transfer Timing Error
	9	-	Parity Error
	10	-	Start While Busy
	11	-	File Mark
	12	-	BCZ
	13	-	EOT
	14	-	BOT
	15	-	Bad Tape



Refer to paragraphs 3.2.1.4 through 3.2.1.6 for an explanation of the RIO format.

AC bits 0 through 3 of this field specifies Read and Reset Interrupts or Read Device Status, as follows:

0000 = CMD 0_{16} specifies that the ICB register is to be read, and interrupts are to be reset.

0001 = CMD 1_{16} specifies that the ICB register is to be read, and interrupt conditions are not to be altered.

*0010 = CMD 2_{16} specifies that the ICB register is to be read, and interrupts are to be reset.

*0011 = CMD 3_{16} specifies that the ICB register is to be read, and interrupt conditions are not to be altered.

Controller Address

Bits 4 through 10 address the specific controller on the I/O channel to which the RIO action is directed.

Subchannel Address

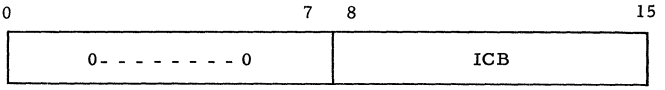
Bits 11 through 13 select a specific subchannel of the controller.

Device Address

Bits 14 and 15 select a specific peripheral if the subchannel drives more than one (used in GPCA, and disc, and cassette tape adapter).

*These two commands are used by disc only; all other devices transmit device status and ICB status in the same word, using the first two commands.

Execution of RIO instruction 0_{16} or 2_{16} cause the device status to be read and any pending interrupts to be cleared. If an interrupt was pending the following will appear in the addressed memory word after the RIO is executed.



Execution of RIO instruction 1_{16} or 3_{16} only causes the device status to be read; any interrupts remain pending. After execution of this RIO the following will appear in the address memory word:

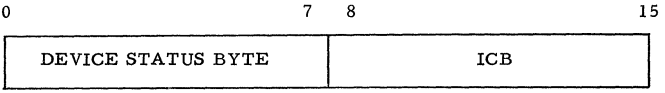


Table 3-7 lists the status bit assignments for the different peripheral devices.

3.2 Processing Unit Circuit Board Descriptions

3.2.1 Processor Operation

This section describes the functional operation of the Processor Unit. The processor is a general purpose 16 bit parallel machine with four program-addressable registers: program counter (PC), accumulator (AC), and two index registers (IX1 and IX2). The processor has direct memory access to the memory modules (maximum eight) and sends and receives data from I/O devices through device adapters and/or controllers. Addressing modes include absolute addressing, PC relative addressing, indexing, and indirect addressing.

Instructions may be either 16 or 32 bits in length. Sixteen bit instructions include a short displacement field which allows addressing ±128 words relative to the current program counter value or +128 words relative to zero or the value contained in one of the index registers.

Word boundaries in memory are fixed. References to memory for words ignore the least significant bit (LSB) of the effective address. Byte addressing uses the LSB to select either the left hand byte (LSB = 0) or the right hand byte (LSB = 1).

A hardware condition bit (CB) is provided to record status as the result of arithmetic or logical operations.

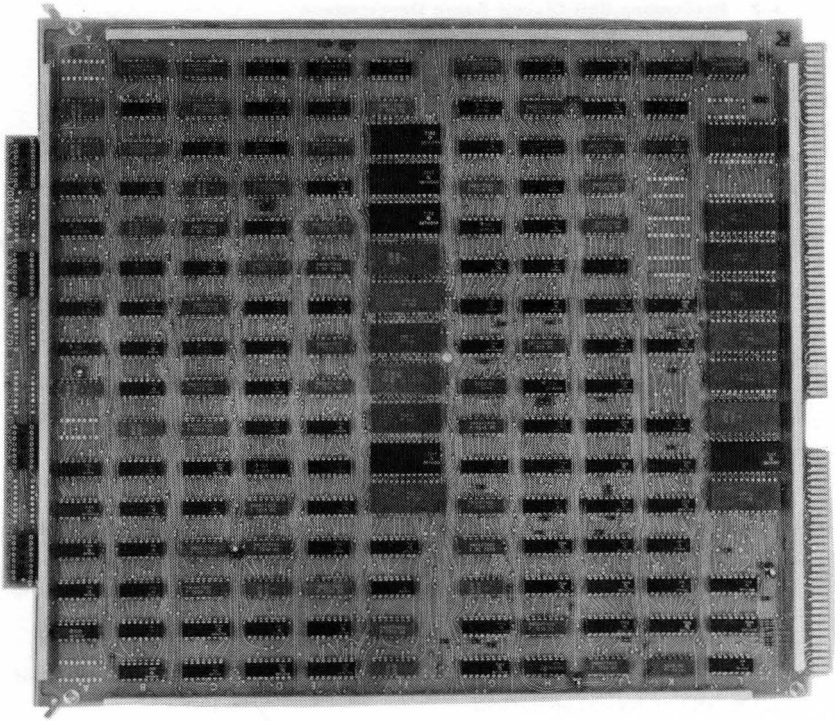
A multilevel interrupt system provides eight external interrupt levels and three internal (CPU) levels.

Input/Output operations occur via a DMA channel initiated by the processor and under the control of the attached controllers.

The processor is physically packaged on one board (Figure 3-13), but works in conjunction with a second feature board for a number of standard and optional features.

3.2.1.1 Processor Circuit Description. Figure 3-14 shows a simplified block diagram of the processor. The functional use of each element is described in the following paragraphs.

The accumulator (AC) is a 16 bit program addressable register, which is the principal data handling register for the processor. It is involved in the execution of most instructions. The most significant bit (bit 0) of the AC is



C73-569

Figure 3-13. PTS-100 Processor

used as the sign bit (0 for positive, 1 for negative) for arithmetic operations, leaving the other 15 bits for fixed point data representation in the following range:

$$2^{15}\ (+32,768)_{10}$$

$$2^{15}\ -1(32,767)_{10}$$

The program counter (PC) is a 16 bit program addressable register that supplies the memory address register with the addresses for the fetching of instruction words from memory and therefore directs the program sequence. Normally, the PC contents are incremented by two for a singel word instruction or by four for a double word instruction to advance the byte-oriented address to that of the next instruction word. This sequencing is disrupted only by the occurrence of a branch (jump) instruction or the processor's servicing a priority interrupt. In the case of a branch instruction, its effective address will replace the current program counter contents and thus initiate a change in program sequence if the branch conditions are met. For interrupts,

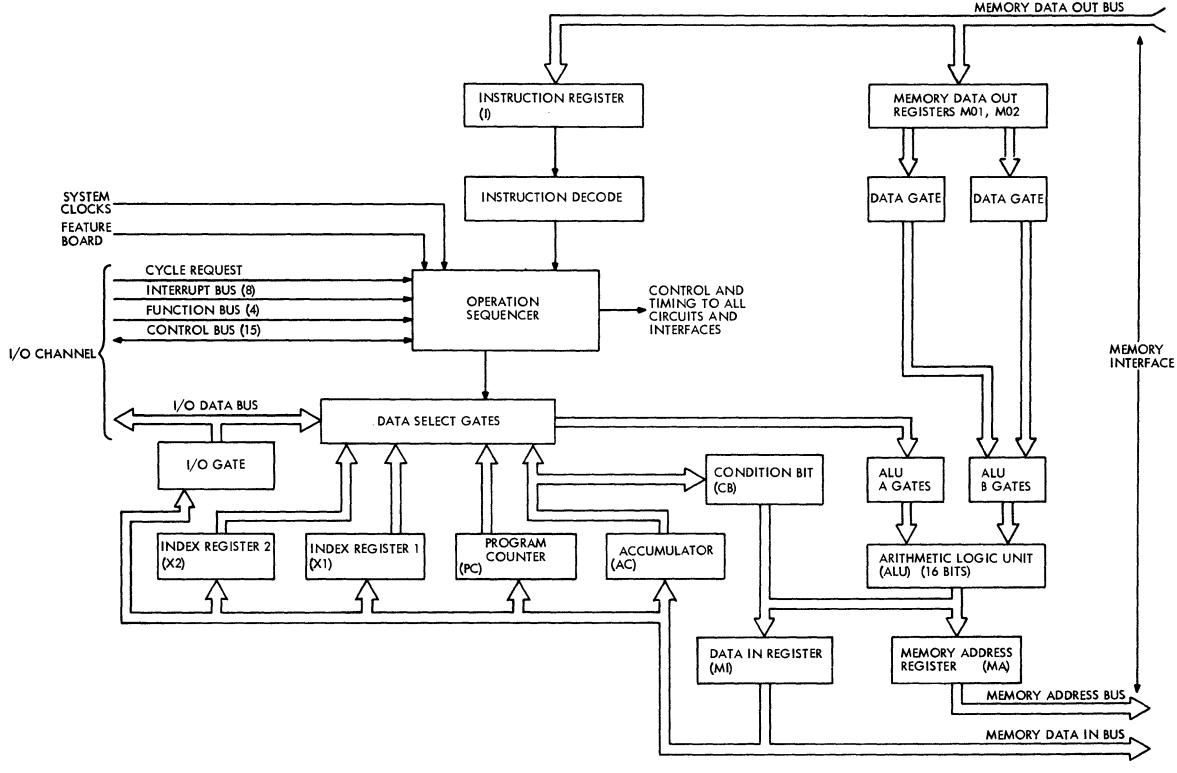


Figure 3-14. PTS-100 Processor, Block Diagram

the processor hardware saves the contents of the program counter (as well as the contents of several other registers) to facilitate restoration of the interrupted program sequence. After the PC contents have been stored, the hardware enters the effective address for the start of the interrupt service routine into the PC. The last instruction of the interrupt service routine is an INR (interrupt return) instruction which restores the previous contents of the program counter.

Index registers 1 and 2 (X1 and X2) are both 16 bit program addressable registers that are used primarily to provide address components for the computation of effective addresses. They may also be used as temporary storage registers for data and address references.

The Memory Address register (MA) is a 16 bit non program addressable register, It temporarily holds the effective memory address until the processor has obtained access to the memory. At this time this address is decoded in memory to select the word location desired.

The Memory Data Out Registers (M01 and M02) are 16 bit non program addressable registers that temporarily hold data received from memory. M01 stores data which will be input to the processor; M02 stores data for output on the I/O bus.

The Memory Data In Register (M1) is a 16 bit non program addressable register. It temporarily stores data from the arithmetic logic unit prior to its being strobed into memory, sent to a peripheral device, or loaded into one of the other machine registers.

The Arithmetic Logic Unit (ALU) functions with the shift hardware controls to accomplish the arithmetic or logical manipulation of data called for by an instruction.

The Instruction register (I) decodes an instruction word read from memory to determine the requested action and method of addressing.

The Condition Bit (CB) is a 1 bit non program addressable register that functions with arithmetic, logical, and compare instruction to simplify program checking of the result. Its state (1 or 0) can only be tested by the Branch-on-CB-Set instruction to indicate results such as arithmetic "carry" occurred, non zero AC contents detected, or true comparison found. The CB state is maintained until execution on a subsequent instruction calls for a different indication. The CB state is automatically saved by the processor hardware when a priority interrupt is serviced. Execution of the interrupt return (INR) instruction at the completion of interrupt servicing automatically restores the CB to the state existing at the time of the interrupt. Table 3-8 shows the instructions that set the condition bit.

Table 3-8. Condition Bit Setting

Instruction	Sets CB If
Add Immediate, R = 0	Arithmetic Overflow
Add Immediate, R ≠ 0	No Carry Out
Add	Arithmetic Overflow
And	Result Not Zero
Subtract	Arithmetic Overflow
Compare for Not Equal	Accumulator ≠ Memory Word
Compare for ACC <	Accumulator < Memory Word
Add ACC to Memory	No Carry Out
Add One to Memory	No Carry Out

3.2.1.2 Processor-Memory Transfers. The processor accepts data from memory and writes data into memory through the use of several control lines, in addition to the registers already described. Under normal conditions, the processor raises a memory request control line (CPREQ) when it wants memory access. At the same time it activates the read/write control line to tell the memory what type of operation is desired, and places the memory address on a 16 bit address bus (ADDR BUS A). For memory write operation, it also places the selected data word on the processor/memory data input bus (CPMDIB). After the memory has accepted the new word, it will provide a processor release (CPREL). Similarly, a data output strobe (CPDOS) will be sent when the requested data has been put on the data output bus. Either operation may be delayed due to memory busy conditions, since the memory will service a display memory request first.

When DAM boards are used and they detect a memory parity error the memory malfunction line informs the processor, which then completes the current instruction and enters the interrupt sequence. Level 10 is set, status is saved, and the PC is loaded from the level 10 interrupt packet. In level 10 no external interrupts can be serviced, however, traps and other parity error interrupts can be serviced.

This transfer is modified slightly under initial program load conditions. When the IPL pushbutton is activated (or the watchdog timer overflows) the processor is reset to zero and the operation sequencer is placed in an initial program load condition. This condition causes the processor to read data from the ROMs (read only memories) located on the feature board instead of from the main memory. This is accomplished by causing a ROM request line to be raised instead of the memory request line. Under these conditions data enters the processor from the bootstrap program stored in the ROM memory and is stored back in the main memory via the normal memory write instructions. Once this transfer of data from ROM to main memory is accomplished, an INR (interrupt return) instruction is used to reset the IPL load flip-flop of the operation sequencer, and normal operation is resumed.

3.2.1.3 Processor I/O Transfers. All input/output operations except display refresh are performed over the processor direct memory access input/output bus (IOB). Display refresh is performed independently of the processor through the display adapters and monitor controllers and is discussed later in this section.

Two types of instructions are used for I/O operations: DIO and RIO. DIO is a Do I/O instruction and is used to start or stop I/O operations. RIO is a read I/O status instruction, and is used to test the status of an I/O device and/or reset status.

Under a DIO start instruction, an initialization sequence is required prior to actual read or write operations. A different initialization sequence is needed for each I/O device, and therefore the program instructions necessary to perform the initialization are stored in different instruction tables located in memory. These instruction tables, known as PIOT (Physical Input/Output Table), are addressed via the effective address of the start DIO instruction. As the PIOT table (7 words) is read out for the selected I/O device, the controller extracts, stores, and utilizes the necessary information. Once the instructions have been performed by the I/O device and/or I/O controller, the I/O initialization sequence has been completed and the appropriate read or write operation can begin. The exact operation to be performed is specified by a controller through the use of a 4 bit function code which is decoded by the operation sequencer within the processor.

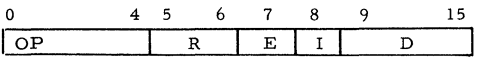
Under a DIO stop instruction, the controller is cleared of all memory requests, interrupts are reset, and the I/O device is placed in a ready/not busy condition.

RIO instructions are used to permit the program to determine the status of an I/O device. For example, if a tape rewind had been ordered, the processor tests to see if it has been completed. The RIO instruction is always followed by a write to memory operation, so that the status of the device can be written into memory. If the device cannot respond to the status request immediately, a control stop line is raised which temporarily halts all processor operations until the status information is available. An RIO instruction may also be used to reset the status bits.

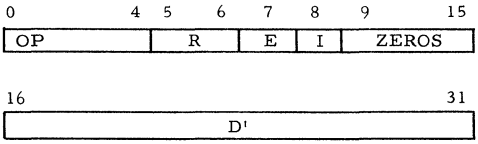
3.2.1.4 Instruction Formats. The PTS-100 has these general classes of machine instructions: Memory reference, immediate instructions, and extended OP code instructions (for interrupt servicing). The formats and functions of each are described below.

Memory reference instructions use base-plus-displacement addressing in single word (16 bit) and double word (32 bit) formats. The latter permit larger displacements for greater memory address ranges. The formats and field definitions for both are as follows.

Single-Word Instruction Format:



Double-Word Instruction Format:



Field Definitions:

OP (Bits 0-4) — five bits which select one of the processor instructions

R (Bits 5, 6) — specify which base the displacement is to be combined with to form the effective address

0 = Zero
1 = Contents of PC
2 = Contents of X1
3 = Contents of X2

E (Bit 7) — specifies the instruction length

0 = Single Word (16 bits)
1 = Double Word (32 bits)

I (Bit 8) — specifies direct or indirect addressing except when R = 1 (PC relative) and E = 0 (16 bit instruction).

0 = direct
1 = indirect

When R = 1 and E = 0, the I bit specifies the sign of the 7 bit displacement field (D)

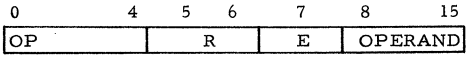
0 = positive
1 = negative

D (Bits 9 to 15) — a 7 bit positive word displacement, of up to 128 words, to be combined with the base in forming the effective address when E = 0. (The D field is shifted left one position prior to address computation to provide word displacement with respect to byte addresses.)

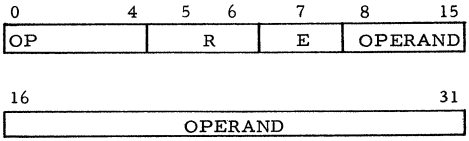
D' (Bits 16 to 31) — a 16 bit byte displacement to be combined with the base in forming the effective address when E = 1. Negative displacements are made possible by the placing of a negative number in two's complement form in the D' field.

The immediate instructions, ADI (Add Immediate) and LDI (Load Immediate), function with single word (16 bit) and double word (32 bit) lengths to provide byte- and word-stored literal values. The formats and field definitions are as follows.

Single-Word Instruction Format:



Double-Word Instruction Format:



Field Definitions:

OP (Bits 0-4) — specifies ADI or LDI instruction

R (Bits 5, 6) — specifies addressable processor register to be involved in immediate instruction operation.

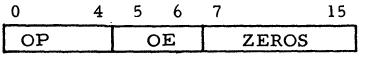
0 = Accumulator
1 = Program Counter
2 = Index Register 1
3 = Index Register 2

E (Bit 7) — specifies instruction length

0 = Single Word (16 bits)
1 = Double Word (32 bits)

Operand — See immediate instruction descriptions (paragraph 3.2.1.6) for operand characteristics.

Extended op code instructions relate to the servicing of priority interrupts. They have a single-word format as follows:



OP (Bits 0-4) — Op code of 1 specifies extended op code instruction

OE (Bits 5, 6) — Specifies which of four extended op code instructions is called for:

0 = Enable external priority interrupt
1 = Disable external priority interrupt
2 = Interrupt return
3 = Trap to interrupt level 9

Refer to Interrupt Servicing Instructions, paragraph 3.2.1.6.

3.2.1.5 Effective Address Computation. Processor computation of the effective address for a memory reference instruction is done in accordance with the appropriate rule of the following set. The notation conventions used are:

( ) means contents of.

(( )) means contents of (addressed by) the contents of.

Single Word Instructions, Effective Addresses

	Direct	Indirect
No Base	2D	(2D)
PC Relative*	(PC) + 2D	(PC) - 2D
X1 Relative	(X1) + 2D	((X1) + 2D)
X2 Relative	(X2) + 2D	((X2) + 2D)

*Indirect addressing is not permitted for single word PC relative addresses.

Double Word Instructions, Effective Address

	Direct	Indirect
No Base	D'	(D')
PC Relative	(PC) + D'	((PC) + D')
X1 Relative	(X1) + D'	((X1) + D')
X2 Relative	(X2) + D'	((X2) + D')

3.2.1.6 Instruction Set. Table 3-9 describes the hardware-implemented instruction set for the processor. The set has nine subgroups: arithmetic, logical, compare, load, store, branch, I/O, interrupt servicing, and trap. The descriptions of each instruction include its name, assembler mnemonic, machine-recognizable op code (hexadecimal), execution time, and functional result. Descriptions are arranged alphabetically by mnemonic for each subgroup.

Table 3-9. Processor Instructions

Instruction Name	Op Code (Hex)	Exec. Time* (μs)	Description of Operation
Arithmetic Instructions** ACM	F000	3.20	Adds contents of accumulator to contents of effectively addressed memory word in two's complement arithmetic. Result is stored at effective address, AC contents remain unchanged. CB is 1 if no carry occurs, or 0 for carry.
Add Memory to AC ADD	5000	2.08	Adds contents of effectively addressed memory word to AC contents in two's complement arithmetic. Result is stored in AC. Contents of effectively addressed memory word are unchanged. CB is 1 if an arithmetic overflow occurs.
Add Immediate ADI	2800	1.60	Adds algebraically the contents of the instruction's operand field to the contents of the instruction-selected register (AC, PC, X1, or X2). Result is stored in the register. The operand value is unchanged. For a single-word instruction, the operand byte contents are taken as sign-and-magnitude representation.

*Execution time is increased by 0.96 microsecond if either indirect or byte displacement addressing (double word instructions) is used, and by 1.92 microseconds if both are used.

**The term "carry" in the following arithmetic instruction descriptions refers to the condition where, upon completion of the operation, the resulting value is $< -2^{15}$ or $> 2^{15}-1$.

Table 3-9. Processor Instructions (cont)

Instruction Name	Op Code (Hex)	Exec. Time* (μs)	Description of Operation
Add Immediate (cont)			The seven least significant bits are added to the selected register's seven least significant bits if the sign bit is 0 or subtracted if it is 1. For a double-word instruction, the 16-bit operand is added to the selected register's 16-bit value in two's complement arithmetic. When the AC is the selected register, the CB is 1 if carry occurs or 0 for no carry. For all other selectable registers, the CB is 1 if no carry occurs, or 0 for a carry.
Add One to Memory AOM	F800	3.20	Increments by one the contents of the effectively addressed memory word. The CB is 1 if no carry occurs, or 0 for a carry.
Shift Right One, Arithmetic SRO	3000	1.60	Shifts the AC contents one bit position to the right. The sign bit (left-most bit) is retained.
Subtract SUB	7000	2.08	Subtracts the contents of the effectively addressed memory word from the AC contents in two's complement. Stores result in AC. The CB is 1 if arithmetic overflow occurs.
Logical Instructions			
AND	6000	2.08	Logically ANDs the contents of the AC on a bit-by-bit basis with the contents of the effectively addressed memory word. Result is stored in AC; contents of the memory word are unchanged. The CB is 1 if the result is not zero; for a zero result the CB is 0. The logical significance of the AND operation can be illustrated by the following, which indicates the result arising from ANDing each of the four possible states for two bits.

Table 3-9. Processor Instructions (cont)

Instruction Name	Op Code (Hex)	Exec. Time* (μs)	Description of Operation
Logical Instructions	6000		
AND (cont)			

Bit A	Bit B	AND Result
0	0	0
0	1	0
1	0	0
1	1	1

Note that one result is based on uniquely known bit states; i.e., the "1" result when both bits are "1".

Exclusive OR
XOR — 5800 — 2.08

Logically exclusive ORs the contents of the AC on a a bit-by-bit basis with the contents of the effectively addressed memory word. Result is stored in the AC; contents of the memory word are unchanged. The logical significance of the exclusive OR operation can be illustrated by the following, which indicates the result arising from exclusive OR of each of the four possible states for two bits.

Bit A	Bit B	Exclusive OR Result
0	0	0
0	1	1
1	0	1
1	1	0

Note that unlike the AND instruction (see above), the exclusive OR produces a 0 result when the bits have the same state (0 or 1) and a 1 result when the bits are in differing states.

Compare Instructions:

Compare for AC Less
CAL — 8800 — 2.08

Compares contents of effectively addressed memory word with contents of AC. If AC is less, CB is 1; CB is 0 for greater than or equal AC value. Contents of AC and memory word are unchanged.

Table 3-9. Processor Instructions (cont)

Instruction Name	Op Code (Hex)	Exec. Time* (μs)	Description of Operation
Compare for AC Not Equal CNE	8000	2.08	Compares contents of effectively addressed memory word with contents of AC. If AC is not equal, CB is 1; CB is 0 for equal value in AC. Contents of AC and memory word are unchanged.
Load Instructions:			
Load Address in Index Register 2 LAX2	4000	2.08	Loads the effective address value in Index Register 2.
Load Byte LDB	9800	2.08	Clears the AC; loads the contents of the effectively addressed memory byte in the right-hand byte (AC8-AC15) of AC. Contents of the memory-resident byte are unchanged.
Load Immediate LDI	2000	1.60	Loads contents of the instruction's operand field in the selected register (AC, PC, X1, or X2). For single-word instructions, LDI clears the register and enters the operand byte contents in the register's right-hand byte (R8-R15). For double-word instructions, LDI enters the operand word contents in the selected register. For either case, the contents of the operand field are unchanged.
Load Word LDW	9000	2.08	Loads the contents of the effectively addressed memory word into the AC. Contents of memory-resident word are unchanged.
Load Index Register 1 LX1	A000	2.08	Loads contents of the effectively addressed memory word in Index Register 1. Contents of memory-resident word are unchanged.
Load Index Register 2 LX2	A800	2.08	Loads contents of the effectively addressed memory word in Index Register 2. Contents of the memory-resident word are unchanged.

Table 3-9. Processor Instructions (cont)

Instruction Name	Op Code (Hex)	Exec. Times* (μs)	Description of Operation
Store Instructions			
Store Byte STB	E000	2.40	Stores the contents of the AC right-hand byte (AC8-AC15) in the effectively addressed memory byte. AC contents are unchanged.
Store Word STW	C000	2.40	Stores the AC contents in the effectively addressed memory word. The AC contents are unchanged.
Store Index Register SX1	D000	2.40	Stores the contents of Index Register 1 in the effectively addressed memory word. The register contents are unchanged.
Store Index Register 2 SX2	D800	2.40	Stores the contents of Index Register 2 in the effectively addressed memory word. The register contents are unchanged.
Branch on Set Condition Bit BCB	1000	1.60	If condition bit (CB) is 1, replace the contents of the PC with the effective memory address. This action effects a conditional change in program sequence. If CB is 0, BCB functions as a "no-op" and does not alter the program sequence.
Branch on AC Minus BRM	1800	1.60	If AC sign bit (ACO) is 1 (typically signifying a negative value in AC), replaces contents of PC with the effective memory address. This action effects a conditional change in program sequence. If ACO is 0, BRM functions as a "no-op" and does not alter the program sequence.
Branch Unconditionally (Jump) JMP	0000	1.60	Effects an unconditional program sequence change or jump by replacing the PC contents with the effective memory address. Memory contents are not changed.
Set Expanded BT SEB			Sets Upper Memory Select bit and causes following memory reference instruction to be executed to upper memory (top 64K of 128K).

Table 3-9. Processor Instructions (cont)

Instruction Name	Op Code (Hex)	Exec. Times* (μs)	Description of Operation
Do I/O Operation DIO	3800	2.24	Selectively initiates or halts addressed peripheral device asynchronous activity. AC contents indicate mode, start or stop I/O, and device address. The effectively addressed memory word is word 0 of the Physical I/O Table, which fully specifies the parameters for a data transfer. DIO in stop mode does not use an effective address. Refer to Section 3.1 for DIO details.
Read I/O Status RIO	E800	3.36	Reads selected status information from addressed peripheral device and/or its adapter or multiplexer channel into the effectively addressed memory word. Refer to Section 3.1 for RIO details.
Interrupt Servicing Instructions***			
Disable External Priority Interrupts DIN	0A00	1.60	Inhibits the suspension of current program activity by subsequent external interrupts, i.e., those initiated by peripheral I/O activity or peripheral error conditions. External interrupts occurring during the disabled interval remain pending for later servicing. DIN is typically used to inhibit disruption of interrupt servicing routines.
Enable External Priority Interrupts ENB	0800	1.60	Permits a pending or subsequent external interrupt of higher priority to suspend current program activity. During the enable interval, external interrupts are recognized by the processor in order of priority (highest to lowest). Interrupts of equal or lower priority to the current operating level remain pending. Upon recognition of an interrupt, the current PC contents, CB state, and

***The following briefly describes the function of each priority interrupt servicing instruction. For greater detail on their use, refer to Section 3.1.

Table 3-9. Processor Instructions (cont)

Instruction Name	Op Code (Hex)	Exec. Times* (μs)	Description of Operation
Enable External Priority Interrupts ENB (cont)			interrupt level are saved by the hardware. The interrupt servicing software must provide for the saving of the contents of the AC, and Index Registers 1 and 2.
Interrupt Return INR	0C00	4.00	Processor replaces the current PC contents, CB state, and operating level with their counterparts saved at the time of the previous interrupt, thereby returning the processor to the previously interrupted state. INR should be the last instruction of the interrupt servicing software, which should prior to INR replace the current contents of the AC and Index Registers 1 and 2 with the previously software-saved contents.
Trap Instruction			
Software-Initiated Interrupt (Monitor Service Call) MSC	0E00	1.60	Processor recognition of the MSC instruction through hardware decode suspends current activity and implements priority interrupt servicing at level 9 after saving the current PC contents, CB state, and operating level. MSC may be issued at any operating level. It cannot be inhibited by the disable interrupts (DIN) instruction. MSC is typically used with the PTS-100 IOCS software to facilitate the unimpeded servicing of user calls to the monitor routine.

3.2.2 Feature Board Operation

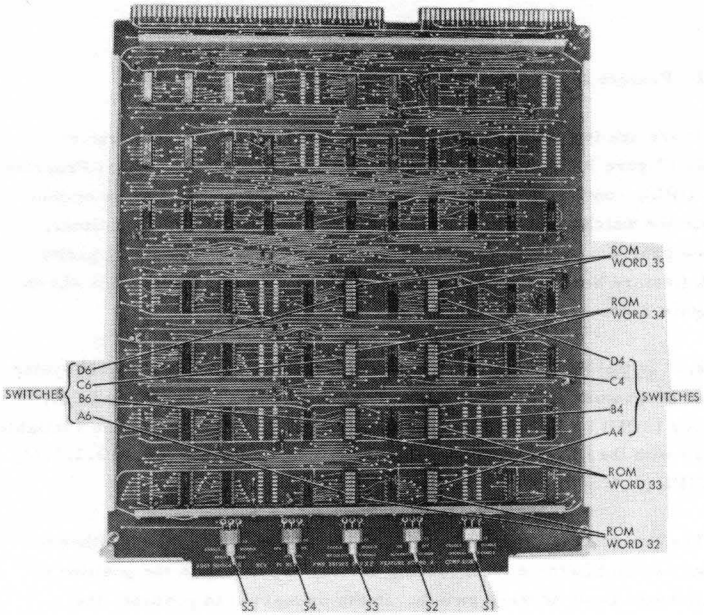
There are two models of the feature board: A and B. The feature boards (Figure 3-15) contain the necessary circuitry for the Initial Program Load (IPL), configuration control, and six system options. These options include the watchdog timer (WDT), power status change, interval timer, remote program load (RPL), alternate load address, and memory parity check (feature board A only). A functional diagram of this board is shown in Figure 3-16.

3.2.2.1 Initial Program Load. The IPL feature permits the PTS-100 system to load programs using a bootstrap loader stored in a 64 word Read Only Memory (ROM) located on the feature board. Other ROMs are also available for use with the RPL (remote program load option, see paragraph 3.2.2.6), and DIPL (disc program load).

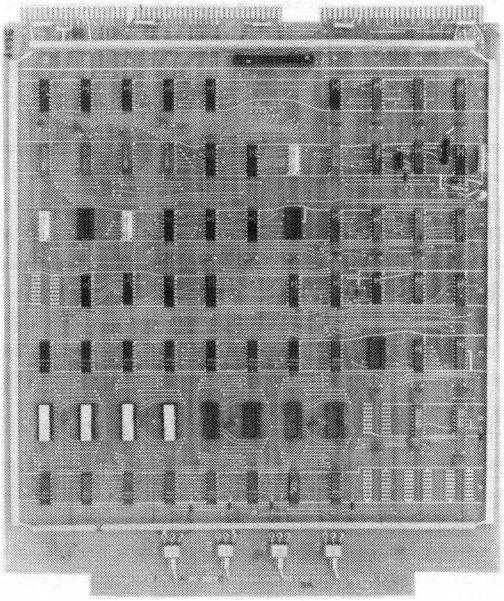
The program being loaded during IPL mode may come from either a primary or an alternate local loading device, depending on the position of the alternate Load Address switch. In the primary load position, the selected device address will be multiplex channel 0. When the switch is placed in the alternate load position, a flag is set in bit position 0 of byte 40 to alert the bootstrap program to utilize the address location specified in byte 40. This location is manually entered into the PTS-100 system through the use of configuration control chip switches (Feature Board A) or manual data chips (Feature Board B).

There are two IPL programs: the old and the new. Both are shown in Figure 3-17. The discussion below is for the old IPL program. The new program is similar except that it uses subroutines for rewind and for the transfer of the configuration data, which is eight words instead of four. When the IPL pushbutton is depressed, the I/O system and processor are cleared, and the program load control is reset. Next, program load is initialized and a portion of the bootstrap program from the IPL ROM is loaded into main memory beginning at location zero. The manually entered configuration control data (bytes 40-47) is read into main memory at hex locations 2A, 2C, 2E, and 30.

After ROM loading, an interrupt return instruction (INR) is executed to begin program loading operations. The first configuration control word in main memory (location 2A) is transferred to main memory location 4, and its high order bit is tested to determine whether it contains the address of the loading device. If the bit is set, the word contains the loading device address; if not, the device address is zero. The loading device address now in the accumulator is then transferred to main memory location 2, and the manual data from memory locations 2C, 2E, and 30 are transferred to memory



C72-8543



C75-1853

Figure 3-15. Feature Boards

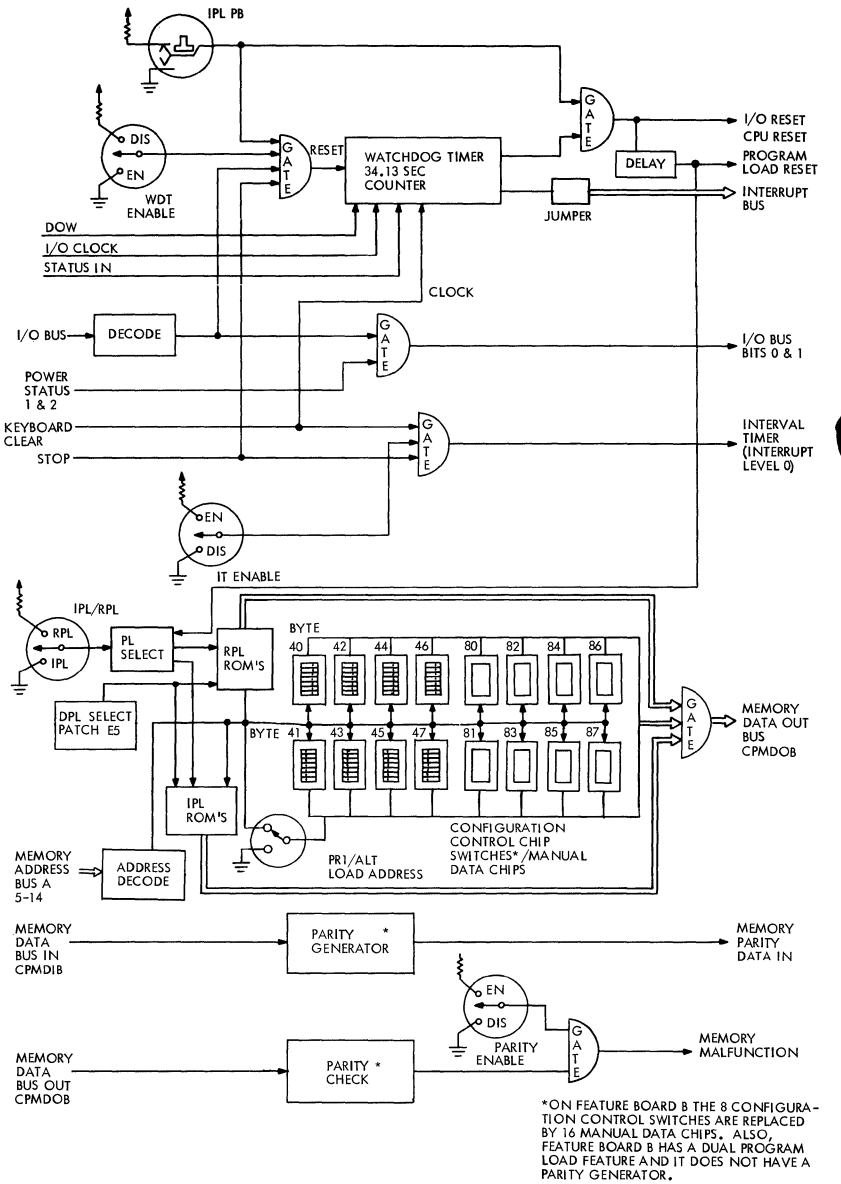


Figure 3-16. Feature Board, Simplified Circuit Diagram

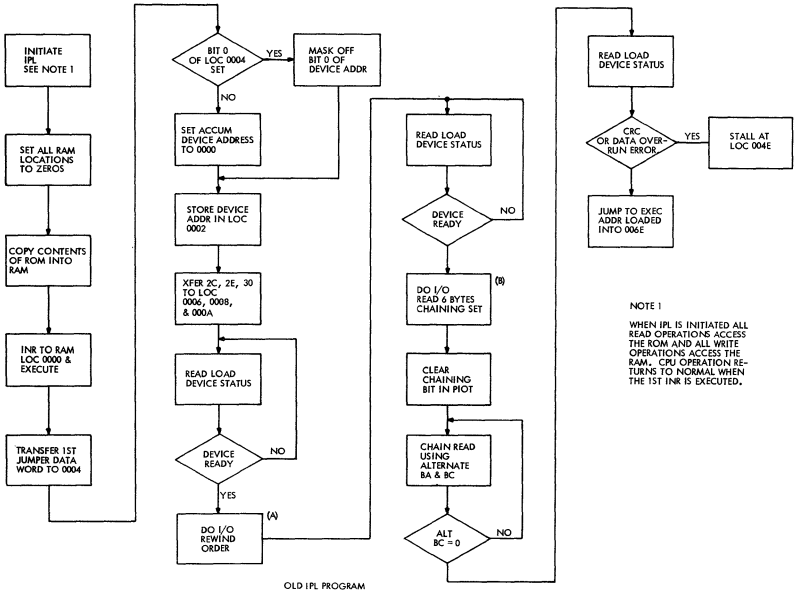


Figure 3-17. IPL Program Functional Sequence (Sheet 1 of 2)

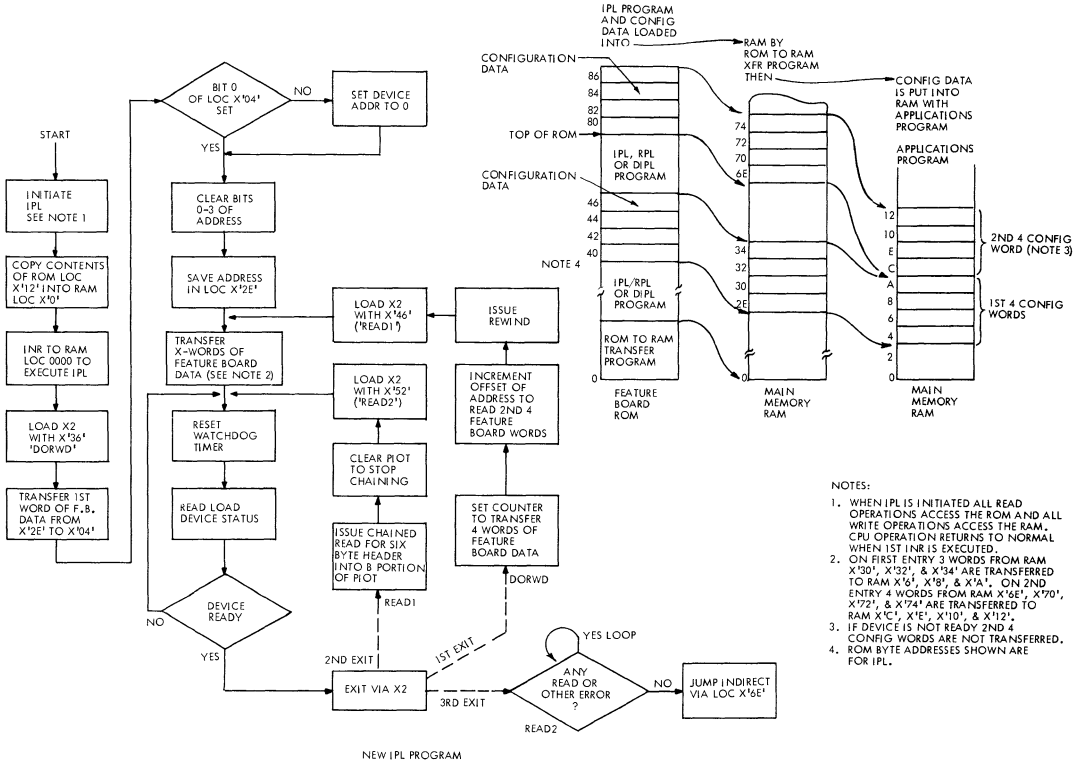


Figure 3-17. IPL Program Functional Sequence (Sheet 2 of 2)

locations 6, 8, and A, respectively. Index register 2 (X2) is set to return address C, and the status of the loading device is read to ensure that it is ready with the input program. A six instruction subroutine in the bootstrap loader is used to read the status of the loading device. When the device status word has its high order bit set, signifying that it is ready, control is transferred to the return address (C) in index register 2, where a rewind command is issued.

In the IPL boostrap loader there are two Physical Input/Output Tables (PIOT). One contains instructions to initialize the load device, and the other contains instructions to load the input program. The first PIOT contains a rewind order that is used for magnetic tape cassette, paper tape, and card reader load devices. The cassette responds to the rewind order by rewinding the tape. The card and paper tape readers respond to the rewind order by physically moving a record forward the number of bytes indicated in the PIOT. The card reader will read one card, and the paper tape reader will read two bytes, although no data will be transferred in either case.

After the rewind order has been issued, index register 2 is set to return address D and the loading device status is again read to ensure completion of the rewind. When the device is ready, the program proceeds to address D, where it uses the second PIOT table, which contains a read order code with the data chaining bit set, to read in the program. The first six program input data bytes are leader information (start loading address, byte count, and program execution address) that is read into the fifth, sixth, and seventh words in the PIOT. Words five and six provide a second byte count and load address which, since the chaining bit is set, cause loading to continue at the new address using the second byte count. One record of the program load data is read consecutively into memory, starting at the location given as the program load address, and continuing until the specified number of bytes have been loaded. After this, return address F is set into index register 2, the device status is read and control proceeds to address F.

At this time the IPL program loops until the input device status word is ready. This word is read to determine whether an error occurred during the loading period. If it did, the program halts. If no errors are detected, control is transferred to the loaded program.

A complete listing of the IPL instructions is given in Figure 3-18.

3.2.2.2 Configuration Control. Feature board A contains eight 8-bit chip switches and feature board B contains eight 16-bit manual data chips for the manual insertion of data for configuration control. As the IPL (DPL or RPL) ROM is being loaded into main memory, bytes 40-47 are read from the eight 8-bit chip switches instead of the ROM. The bootstrap programs

```
IPL LOAD                                                    PAGE  0001
ERRORS  LOC  CONTENTS   OP R F I S OPERAND  SEQ #  SOURCE

                                            0001  *                                                        IP 00010
                                            0002  *                    INITIAL PROGRAM LOAD                IP 00020
                                            0003  *                      (IPL)                             IP 00030
                                            0004  *                                                        IP 00040
                                            0005  *                    VERSION  6                          IP 00050
                                            0006  *                                                        IP 00060
                                            0007  *                                                        IP 00070
                                            0008  *                                                        IP 00080
                                            0009        ORG   0                                            IP 00090
        0000  2100   04 0 1 0              0010        LDI   AC,-64,L    NEGATIVE WORD COUNT MOVE TO      IP 00100
        0002  FFC0                 -  0040
        0004  2400   04 2 0 0 +     00     0011        LDI   X1,0        STARTING ADDRESS                 IP 00110
        0006  AC08   15 2 0 0 +     08     0012        LX2,X1 X'16'      MOVE                             IP 00120
        0008  DC00   1A 2 0 0 +     00     0013        SX2,X1 0            DATA                           IP 00130
        000A  2801   05 0 0 0 +     01     0014        ADI   AC,1        ADD TO COUNT                     IP 00140
        000C  2C02   05 2 0 0 +     02     0015        ADI   X1,2        BUMP ADDRESS                     IP 00150
        000E  1485   03 1 0 0 -     05     0016        BRM   *-8         BRANCH TO MOVE MORE              IP 00160
        0010  C277                         0017        HEX   C277        STW X'100' CLEAR 100 AND 102     IP 00170
        0012  C277                         0018        HEX   C277        STW X'102'  FOR INR              IP 00180
        0014  0C00                         0019        INR               INTERRUPT RETURN TO RAM          IP 00190
                                            0020  *                                                        IP 00200
        0016  0201   00 1 0 0 +     01     0021  #00   JMP   *+4          GO TO START OF LOAD              IP 00210
        0018  0FFF                         0022  #02   HEX   0FFF        MASK/DEVICE ADR STORAGE          IP 00220
        001A  9212   12 1 0 0 +     12     0023  #04   LDW   #42         TRANSFER JUMPER DATA TO          IP 00230
        001C  C282   18 1 0 0 -     02     0024  #06   STW   #04           LOCATIONS 4 - 10               IP 00240
        001E  1401   03 1 0 0 +     01     0025  #08   BRM   *+4          IS 1ST WORD = DEVICE ADR         IP 00250
        0020  2000   04 0 0 0 +     00     0026  #10   LDI   AC,0        NO, ASSUME DEVICE ADR 0          IP 00260
        0022  6286   0C 1 0 0 -     06     0027  #12   AND   #02         YES, MASK OFF HIGH BIT           IP 00270
        0024  C287   18 1 0 0 -     07     0028  #14   STW   #02         SAVE DEVICE ADR                  IP 00280
        0026  920D   12 1 0 0 +     0D     0029  #16   LDW   #44         CONTINUE TRANSFERRING            IP 00290
        0028  C287   18 1 0 0 -     07     0030  #18   STW   #06           JUMPER DATA TO                 IP 00300
        002A  920C   12 1 0 0 +     0C     0031  #20   LDW   #45           STORAGE AREA                   IP 00310
        002C  C288   18 1 0 0 -     08     0032  #22   STW   #08                                          IP 00320
        002E  9208   12 1 0 0 +     08     0033  #24   LDW   #48                                          IP 00330
        0030  C289   18 1 0 0 -     09     0034  #26   STW   #10                                          IP 00340
12      0032  420A   08 1 0 0 +     0A     0035  #28   LAX2  #50         SET RETURN ADR                   IP 00350
        0034  928F   12 1 0 0 -     0F     0036  #30   LDW   #02         READ STATUS ROUTINE              IP 00360
11      0036  5A19   08 1 0 0 +     19     0037  #32   XOR   #84                                          IP 00370
        0038  EA03   1D 1 0 0 +     03     0038  #34   RIO   #42         CHECK STATUS                     IP 00380
10      003A  9202   12 1 0 0 +     02     0039  #36   LDW   #42                                          IP 00390
        003C  1F00   03 3 0 0 +     00     0040  #38   BRM,X2 0          RETURN TO CALLER IF READY        IP 00400
9       003E  0286   00 1 0 0 -     06     0041  #40   JMP   *-10        LOOP BACK IF BUSY                IP 00410
        0040  0000                         0042  #42   HEX   0          JUMPER DATA                      IP 00420
8       0042  0000                         0043  #44   HEX   0          JUMPER DATA                      IP 00430
        0044  0000                         0044  #46   HEX   0          JUMPER DATA                      IP 00440
7       0046  0000                         0045  #48   HEX   0          JUMPER DATA                      IP 00450
        0048  9999   12 1 0 0 -     19     0046  #50   LDW   #02                                          IP 00460
6       004A  3A11   07 1 0 0 +     11     0047  #52   DIO   #88         ISSUE REWIND COMMAND             IP 00470
        004C  4201   08 1 0 0 +     01     0048  #54   LAX2  #58         SET RETURN ADR                   IP 00480
5       004E  228E   00 1 0 0 -     0E     0049  #56   JMP   #30         GO CHECK STATUS                  IP 00490
        0050  DA18   1B 1 0 0 +     18     0050  #58   SX2   #138        SET BYTE COUNT TO NON-ZERO       IP 00500
4       0052  929E   12 1 0 0 -     1E     0051  #60   LDW   #02                                          IP 00510
        0054  3A10   07 1 0 0 +     10     0052  #62   DIO   #96         ISSUE READ COMMAND               IP 00520
3       0056  2000   04 0 0 0 +     00     0053  #64   LDI   AC,0                                        IP 00530
        0058  C28F   18 1 0 0 +     0F     0054  #66   STW   #96         CLEAR CHAINING BIT IN PIOT       IP 00540
2       005A  8213   10 1 0 0 +     13     0055  #68   CNE   #108        DOES BYTE COUNT = 0              IP 00550
```

Figure 3-18. IPL Program 593614 (Sheet 1 of 4)

```
        IPL LOAD                                             PAGE  0002
ERRORS  LOC  CONTENTS  OP R E I S OPERAND SEQ #  SOURCE

        005C  1282     02 1 0 0 -   02    0056  #70    BCR    *-2     NO, LOOP BACK                  IP 00560
        005E  4201     08 1 0 0 +   01    0057  #72    LAX2   #76     SET RETURN ADR                 IP 00570
        0060  0297     00 1 0 0 -   17    0058  #74    JMP    #30     GO CHECK STATUS                IP 00580
        0062  6204     0C 1 0 0 +   04    0059  #76    AND    #86     CRC OR DATA OVERRUN ERROR      IP 00590
        0064  1281     02 1 0 0 -   01    0060  #78    BCR    *       YES, LOOP ON SELF              IP 00600
        0066  0380     00 1 1 1           0061  #80    JMP,N  #110    NO, JUMP TO PROGRAM START      IP 00610
        0068  001A             +  001A
                                          0062  *                     (LONG INSTRUCTION)             IP 00620
        006A  1000                        0063  #84    HEX    1000    CONSTANT                       IP 00630
        006C  0600                        0064  #86    HEX    0600    MASK                           IP 00640
        006E  0300                        0065  #88    HEX    0300    REWIND ORDER PACKET            IP 00650
        0070  0000                        0066  #90    HEX    0000                                   IP 00660
        0072  FFFE                        0067  #92    HEX    FFFE                                   IP 00670
        0074  0000                        0068  #94    HEX    0                                      IP 00680
        0076  1000                        0069  #96    HEX    1000    READ CMD WITH CHAINING         IP 00690
        0078  006A                        0070. #98    HEX    6A      START ADR OF HEADER            IP 00700
        007A  FFFA                        0071  #100   HEX    FFFA    HEADER BYTE COUNT (-6)         IP 00710
        007C  FFFF                        0072  #102   HEX    FFFF    STOP TRANSFER SIGNAL           IP 00720
        007E  0000                        0073  #104   HEX    0                                      IP 00730
        0080  0000                        0074  #106   HEX    0                                      IP 00740
        0082  0000                        0075  #108   HEX    0                                      IP 00750
        0084  0000                        0076  #110   HEX    0                                      IP 00760
                                          0077         END    #00                                    IP 00770

        THERE ARE   NO ERRORS IN THIS ASSEMBLY
```

Figure 3-18. IPL Program 593614 (Sheet 2 of 4)

```
       IPLLOAD7                                             PAGE  0001
ERRORS  LOC CONTENTS   OP R F I S OPERAND SEQ # SOURCE

                                          0001  *     DRAWING NUMBER  863075                                  HYA00010
                                          0002  *                                                             HYA00020
                                          0003  *         IPL  (INITIAL PROGRAM LOAD) PROGRAM - VERSION 7     HYA00030
                                          0004  *                                                             HYA00040
                                          0005  *    THIS IPL IS WRITTEN TO OPERATE WITH FEATURE BOARD VERSION 'B'     HYA00050
                                          0006  *    THE FIRST FOUR WORDS OF CONFIGURATION DATA ARE STORED IN LOCATION  HYA00060
                                          0007  *                0004, 0006, 0008, 000A                       HYA00070
                                          0008  *                                                             HYA00080
                                          0009  *    THE SECOND FOUR WORDS OF CONFIGURATION DATA ARE STORED IN LOCATIONSHYA00090
                                          0010  *                000C, 000E, 0010, 0012                       HYA00100
                                          0011  *                                                             HYA00110
                                          0012  *    THIS IS A NON-CLEAR IPL.                                 HYA00120
                                          0013  *                                                             HYA00130
                                          0014  *    THE WATCHDOG TIMER WILL BE RESET CONTINUOUSLY DURING STATUS LOOP   HYA00140
                                          0015  *                                                             HYA00150
                                          0016  *                                                             HYA00160
                                          0017        ORG                                                     HYA00170
                                          0018  *                                                             HYA00180
        0000   0012                       0019  OFFSET  EQU     X'12'       SIZE OF ROM-RAM TRANSFER PROGRAM  HYA00190
                                          0020  *                                                             HYA00200
                                          0021  *       THIS PORTION PROVIDES FOR ROM TO RAM TRANSFER         HYA00210
                                          0022  *                                                             HYA00220
        0000   2500   04 2 1 0            0023          LDI     X1,-118     COMPLIMENT OF XFER AMOUNT IN BYTES HYA00230
        0002   FFBA             -  0076
        0004   9444   12 2 0 0 +    44    0024  ROMRAM  LDW,X1  118+OFFSET  FROM ROM X'12'                    HYA00240
        0006   C43B   18 2 0 0 +    3B    0025          STW,X1  118         TO RAM X'0'                       HYA00250
        0008   2C02   05 2 0 0 +    02    0026          ADI     X1,2                                          HYA00260
        000A   1284   02 1 0 0 -    04    0027          BCB     ROMRAM      LOOP FOR FULL TRANSFER AMOUNT     HYA00270
        000C   D279                       0028          HEX     D279        CLEAR INTERRUPT PACKET PC         HYA00280
        000E   D279                       0029          HEX     D279        CLEAR INTERRUPT PACKET LEVEL, CB  HYA00290
        0010   0C00                       0030          INR                 TO RAM PROGRAM                    HYA00300
                                          0031  *                                                             HYA00310
                                          0032  *       THE FOLLOWING IS THE ACTUAL RAM PROGRAM               HYA00320
                                          0033  *                                                             HYA00330
                                          0034  *       UPON EXECUTION IT WILL BE BASED AT LOCATION X'0000'   HYA00340
                                          0035  *                                                             HYA00350
                                          0036  *                                                          RAMHYA00360
                                          0037  *                                                          LOCHYA00370
                                          0038  *                                                             HYA00380
        0012   0202   00 1 0 0 +    02    0039          JMP     START                                       00HYA00390
        0014   0000                       0040          RESV    4           FILLER                          02HYA00400
        0018   4217   08 1 0 0 +    17    0041  START   LAX2    DORWND                                      06HYA00410
        001A   9212   12 1 0 0 +    12    0042          LDW     FB1         FIRST WORD OF FEATURE BOARD DATA 08HYA00420
        001C   C002   18 0 0 0 +    02    0043          STW     X'04'       STASH IT                        0AHYA00430
        001E   1A01   03 1 0 0 +    01    0044          BBM     ALTDEV      IF HIGH-ORDER BIT ON - ALT. LOAD DEVICE  0CHYA00440
        0020   2000   04 0 0 0 +    00    0045          LDI     AC,0        NOT ALT. DEV. - USE MUX/PORT ZERO 0EHYA00450
        0022   622C   0C 1 0 0 +    2C    0046  ALTDEV  AND     X0FFF       EXTRACT ADDRESS PORTION         10HYA00460
        0024   C20D   18 1 0 0 +    0D    0047          STW     FB1         TEMP STORE FOR REST OF IPL      12HYA00470
        0026   9418   12 2 0 0 +    18    0048  FBLOOP  LDW,X1  X'30'       TRANSFER FEATURE BOARD DATA     14HYA00480
        0028   C403   18 2 0 0 +    03    0049          STW,X1  6                                           16HYA00490
        002A   2C02   05 2 0 0 +    02    0050          ADI     X1,2                                        18HYA00500
        002C   FA1F   1F 1 0 0 +    1F    0051          ADM     FBCNT       3 ITERATIONS ON FIRST ENTRANCE, 4 LATER  1AHYA00510
        002E   1285   02 1 0 0 -    05    0052          BCB     FBLOOP                                      1CHYA00520
        0030   921D   12 1 0 0 +    1D    0053  STATUS  LDW     X'DF0                                       1EHYA00530
        0032   FA08   1D 1 0 0 +    08    0054          RIO     FB3         RESET WATCHDOG TIMER            20HYA00540
        0034   9205   12 1 0 0 +    05    0055          LDW     FB1         DEVICE ADDRESS                  22HYA00550
```

Figure 3-18.   IPL Program 593614 (Sheet 3 of 4)

```
            IPLLOAD7                                                          PAGE  0002
   ERRORS    LOC CONTENTS   OP R F I S OPERAND SEQ # SOURCE

             0036    5A20     08 1 0 0 +    20     0056              XOR     X1000                                              24HYA00560
             0038    EA04     1D 1 0 0 +    04     0057              RIO     FB2         CHECK STATUS OF LOAD DEVICE            26HYA00570
             003A    9203     12 1 0 0 +    03     0058              LDW     FB2                                                28HYA00580
             003C    1E00     03 3 0 0 +    00     0059              BRM,X2  0           DEVICE READY - BACK TO CALLER          2AHYA00590
             003E    0288     00 1 0 0 -    08     0060              JMP     STATUS      LOOP UNTIL READY                       2CHYA00600
             0040    0000                          0061    FB1       HEX     0           WORD 1 OF FEATURE BOARD BEFORE XFER TO 4 2EHYA00610
             0042    0000                          0062    FB2       HEX     0           WORD 2 OF FEATURE BOARD BEFORE XFER TO 6 30HYA00620
             0044    0000                          0063    FB3       HEX     0           WORD 3 OF FEATURE BOARD BEFORE XFER TO 8 32HYA00630
             0046    0000                          0064    FB4       HEX     0           WORD 4 OF FEATURE BOARD BEFORE XFER TO A 34HYA00640
             0048    921A     12 1 0 0 +    1A     0065    DORWND    LDW     MINUS4      SET TO MOVE FB 5 - 8                   36HYA00650
             004A    C20F     18 1 0 0 +    0F     0066              STW     FBCNT                                              38HYA00660
             004C    201C     04 0 0 0 +    1C     0067              LDT     AC,X'1C'    OFFSET TO GET FB 5-8 IN RAM            3AHYA00670
             004E    F295     1F 1 0 0 -    15     0068              ACM     FBLOOP                                             3CHYA00680
             0050    9289     12 1 0 0 -    09     0069              LDW     FB1         DEVICE ADDRESS                         3EHYA00690
             0052    3A0F     07 1 0 0 +    0F     0070              DIO     RWDORD      ISSUE REWIND ORDER                     40HYA00700
             0054    4201     08 1 0 0 +    01     0071              LAX2    READ1                                              42HYA00710
             0056    0299     00 1 0 0 -    19     0072              JMP     FBLOOP      GET REST OF FB, AND WAIT FOR REWIND    44HYA00720
             0058    928D     12 1 0 0 -    0D     0073    READ1     LDW     FB1         DEVICE ADDRESS                         46HYA00730
             005A    3A0B     07 1 0 0 +    0B     0074              DIO     RPIOT0      ISSUE CHAINED READ TO GET HEADER       48HYA00740
             005C    2000     04 0 0 0 +    00     0075              LDT     AC,0                                               4AHYA00750
             005E    C209     18 1 0 0 +    09     0076              STW     RPIOT0      STOP CHAINING                          4CHYA00760
             0060    4201     08 1 0 0 +    01     0077              LAX2    READ2                                              4EHYA00770
             0062    029A     00 1 0 0 -    1A     0078              JMP     STATUS      WAIT FOR READ TO COMPLETE              50HYA00780
             0064    620A     0C 1 0 0 +    0A     0079    READ2     AND     X1F00       CHECK CRC, DATA O'RUN, BOT/EOT         52HYA00790
             0066    1281     02 1 0 0 -    01     0080              BCB     *           ERROR                                  54HYA00800
             0068    00B7                          0081              HEX     00B7        JMP,N   RPIOT+14   TO PROGRAM          56HYA00810
             006A    FFFD                          0082    FBCNT     DEC     -3          BECOMES -4 ON SECOND TIME AROUND       58HYA00820
             006C    1DF0                          0083    X1DF0     HEX     1DF0        ADDRESS OF WATCHDOG TIMER              5AHYA00830
             006E    0000                          0084              RESV    2           FILLER SO RPIOT0 FALLS ON MOD 16 BOUND 5CHYA00840
             0070    0300                          0085    RWDORD    HEX     0300        REWIND ORDER                           5EHYA00850
             0072    1000                          0086    RPIOT0    HEX     1000        READ ORDER WITH CHAINING               60HYA00860
             0074    006A                          0087              HEX     6A          READ HEADER INTO X'6A'                 62HYA00870
             0076    FFFA                          0088              DEC     -6          FOR 6-BYTES                            64HYA00880
             0078    1000                          0089    X1000     HEX     1000        CONSTANT                               66HYA00890
             007A    1F00                          0090    X1F00     HEX     1F00        CONSTANT                               68HYA00900
             007C    0FFF                          0091    X0FFF     HEX     0FFF        MASK - HEADER READ INTO HERE           6AHYA00910
             007E    FFFC                          0092    MINUS4    DEC     -4          HEADER WILL ALSO BE READ HERE          6CHYA00920
                                                   0093              END     0                                                    HYA00930

             THERE ARE   NO ERRORS IN THIS ASSEMBLY
   !EOJ
```

Figure 3-18. IPL Program 593614 (Sheet 4 of 4)

stored in the ROM are all hardwired, thus only bytes 40-47 can be manually programmed. The first few bytes are used for entering the address of the alternate load device. Bit 0 of the first byte serves as a flag bit to indicate which position the primary/alternate switch (S2) is set in. The functions of the remaining bytes are controlled by system software, and vary with the configuration. In general, they indicate the number and types of displays connected to control units and monitor controllers.

The ROM bytes controlled by the chip switches on feature board A are illustrated in Figure 3-19. For the bytes controlled by the manual data chips on feature board B refer to the figures given in Appendix A.

3.2.2.3 Watchdog Timer, Feature 2421. The watchdog timer (WDT) provides an automatic program restart after a program hangup or when power is initially applied to the PTS-100 system. The program restart may occur locally or remotely via a communications modem to a host computer. The latter capability requires the Remote Program Load feature (paragraph 3.2.2.6).

The watchdog timer is basically a 34.13 second counter with provision for the operating program to reset the counter to zero. Under normal operating conditions, resets are periodically issued well within the 34.13 second timeout period. If a reset is not issued, the watchdog timer initializes the system and initiates a program load operation. This action is similar to that caused by depressing the IPL pushbutton.

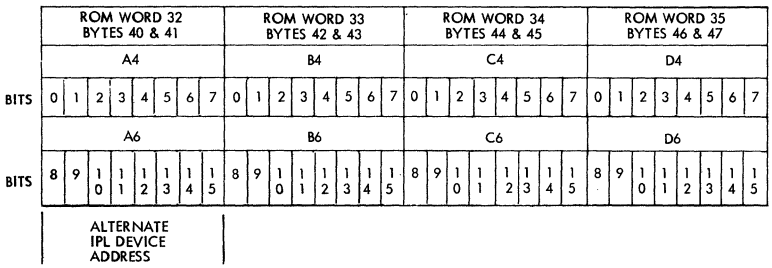


Figure 3-19. Feature Board A Chip Switches

The watchdog timer counts keyboard clear pulses from a display adapter board. These pulses, occuring 15 times a second, provide the triggers to step the counter. After 2^9 counts (34.13 seconds), the counter puts out a signal to the I/O and processor which causes them to reset and begin an initial program load. While no warning interrupt is issued prior to these actions in the standard timer, a warning interrupt capability is available. It is implemented by the addition of a patch between the WDT interrupt signal and one of the eight external interrupt lines. This interrupt will occur after 2^8 counts (17.07 seconds). It can be used by the program to take special actions, such as storing key data from the memory onto a peripheral storage device, or providing a memory dump.

Five conditions will reset the watchdog timer and prevent it from initializing the system. Three of these, a program disable, the stop line, and the WDT disable switch, will reset it and stop the counter. The other two, a program reset and an IPL signal, reset it and start the counter. The stop line is an automatic disable provided whenever the processor is placed in either the stop or single instruction mode by an attached CE console. When the run mode is resumed, the watchdog timer function starts again.

A switch on the rear of the feature board is provided to disable the watchdog timer function manually, if desired. It may also be turned on and off under program control. This is normally reserved for diagnostics and special cases since the automatic restart capability is disabled when the WDT is turned off. Control of the WDT by programming is accomplished by the use of the Do I/O stop instruction with the WDT addressed by means of its assigned address, DFO_{16}. Do I/O in start mode will reset and start the counter. The effective address in the Do I/O instruction is unused for this function.

The WDT is usually reset by the operating program. The program can reset the timer to zero by issuing a Read I/O status instruction to the watchdog timer circuitry. This circuitry has been assigned device address DFO_{16}. This instruction is normally issued in ample time to prevent the WDT from initializing the system. However, if a program hangup occurs, the timer will overflow 34.13 seconds after its last reset and automatically restart the system.

3.2.2.4 Power Status Change. A battery pack option is available to the PTS-100 system to allow continued system operation during periods of limited power outages. If this option is included in the system, the program may want to know when the system is operating from the battery pack. Notification of this changeover can be provided to the program through the use of power status bits. Each time a read I/O instruction is issued for device address DFO_{16}, the status of two power status lines are read into the computer. Since this instruction is the same one which is used to reset the WDT, implementation of this option provides automatic notification of any power changeover. If the WDT option was not selected, or disabled by program or manual means, the operating program would have to provide the read I/O status instruction periodically to determine the status of external power.

3.2.2.5 Interval Timer, Feature 2422. This option provides the processor with a signal generated every 67 milliseconds (15 times a second). The signal can be used as a timing signal or delay signal for program control purposes. In operation, the interval timer generates a processor interrupt at priority level zero. The signal uses the keyboard clear signal from a display adapter board for its source, and if enabled it will flag the processor. The flag is recognized by the processor only if the external interrupts are enabled and only when the processor is operating at level zero. If the above conditions are not satisfied, the interrupt remains pending. Should the program fail to respond prior to the next interrupt, the current interrupt remains pending and the second interrupt is lost. (Refer to Section 3.1.8 for information regarding the servicing of interrupts.)

The control gate will disable the interval timer function whenever the interval timer switch has been put in the disable position. In addition, an automatic disable is provided whenever the processor is placed in Stop mode by the CE console. Timer interrupts resume after Run mode is resumed.

3.2.2.6 Remote Program Load. The remote program load (RPL) option permits the PTS-100 system to receive system programs from a host computer via a communications modem or channel interface controller. Its operation is similar to the operation of the initial program load sequence described in paragraph 3.2.2.1. However, the instruction sequence is longer and varies with the application. To hold this longer instruction sequence, a 512 word ROM (feature board A) or a 512/1024 word ROM (feature board B) is provided on the feature board (compared to a 64 word ROM for the IPL). The RPL ROM on feature board B is mounted on a piggyback plug-in module. Refer to Table 2-4 for the RPL PROM locations on the module.

Selection of the remote program load feature is effected through the IPL/RPL switch which controls whether the IPL or RPL ROM's are read out when a bootstrap operation is begun. The configuration control chips or chip switches are utilized for either IPL or RPL operation.

3.2.2.7 Alternate Load. The alternate load feature is included in each PTS-100 system. It is used to specify the exact external address of a program load device when the primary address (multiplex channel 0) is not to be used. This allows an initial program load to occur from any external load device. Selection of the alternate loading device is made through the alternate load address switch on the rear of the feature board. The switch has two positions, one for primary and one for alternate load address.

On feature board A, manual insertion of the alternate load address is made via the word 32 configuration control ship switches A4, A6 and on feature board B it is made using data chip B4.

The alternate program load address assignments are illustrated in Figure 3-20.

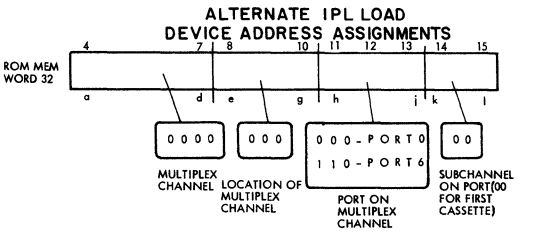


Figure 3-20. Alternate IPL Load Device Address Assignments

3.2.2.8 Memory Parity Check. On feature board A, switch S5 enables a memory parity check circuit that may be developed in the future. Until that time S5 should always be set to the disabled position. There is no parity circuit on feature board B.

3.2.2.9 Disc Program Load. The disc program load (DIPL) option permits the PTS-100 system to receive system programs from a disc. Its operation is similar to that for the RPL described in paragraph 3.2.2.6. In fact the disc program load is stored in ROMs which are controlled by the IPL/RPL switch. When the switch is in the RPL position the disc load program is read out.

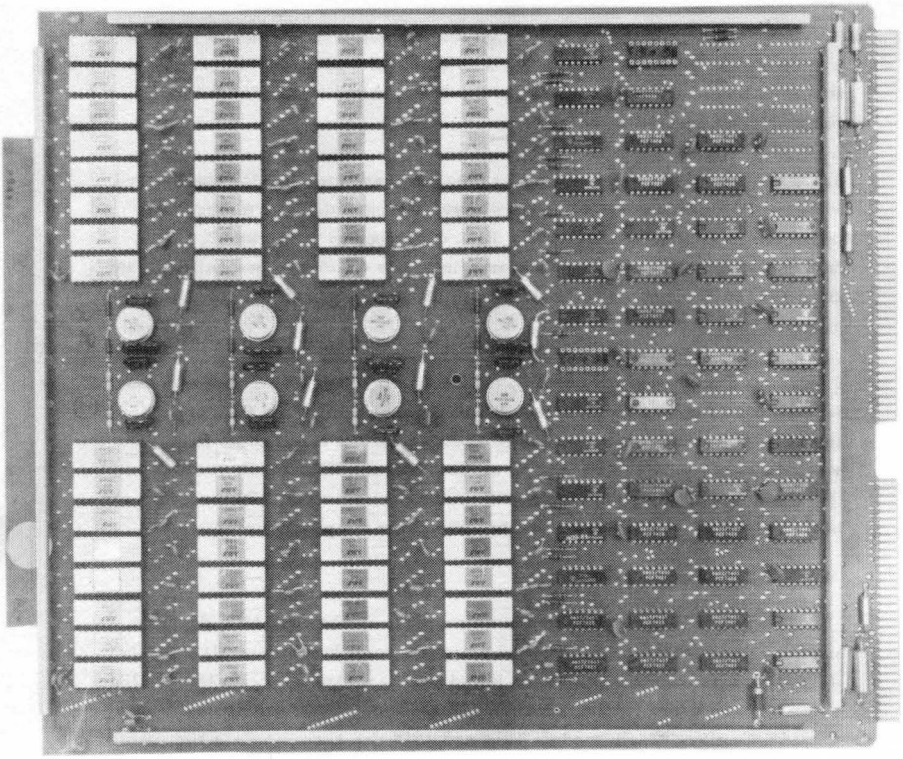
3.2.2.10 Dual Program Load. Feature board B has a dual program load feature (DPL) that is patch selectable with patch E5. When DPL is selected the DO I/O instruction to the watchdog timer always initiates an RPL, regardless of the IPL/RPL switch setting, and the IPL pushbutton and watchdog timer are under control of the IPL/RPL switch. The RPL program can be 512 or 1024 words. Refer to Appendix A for the patch wiring.

3.2.3 Memory Operation

The PTS-100 main memory is a two-port, P-channel, MOS dynamic memory composed of from one to 8 printed circuit boards containing either 4096/8192 bytes of storage on each board (8K boards) or 8192/12,288/16,384 bytes on each board (16K boards). PTS-100 model 1005 can accommodate one 16K memory board; models 1014 and 1015 can accommodate two memory boards; model 1020 can accommodate up to eight boards. The power supplies are strapped differently for the 8K and 16K boards (refer to Section 3.4) since the 8K boards require +24 vdc and +28 vdc whereas the 16K boards require -15 vdc and +8.5 vdc.

Figure 3-21 shows a 8192 word or 16,384 byte memory module, with its 4 rows of 16 memory chips and the associated timing, logic, control, and interface circuitry. The older 4096 word module looks much the same. The modules require only power, external instructions, and clock signals (25 MHz and 160 ns) to store, retrieve, and refresh data.

One memory port connects to the processor, and the other connects to a display adapter. One display adapter can service two different memory modules. The processor reads from and writes to memory; the display adapter initiates memory refresh and reads data from memory to refresh the data on the displays. Memory refresh and display refresh operations take place independently of the processor. However, when a display adapter and the processor require simultaneous service the display adapter is given priority.



C75-1854

Figure 3-21. 16K Memory Module

Memory refresh is necessary because the data stored in the MOS memory elements decays with time. The display adapter(s) initiates a refresh cycle every 64.1 μs, during the time that the line sync (LS) and display (DA) characters are sent to the monitor controllers (refer to display adapter operation). Each refresh cycle takes 1.28 μs, with a total of 32 cycles needed to refresh the entire memory; refresh thus consumes 2 percent of the total memory available time. Read from memory operations from both the processor and display adapters take 800 ns, and processor write to memory operations take 1.28 μs. All write operations are performed by the processor. (Refer to Table 3-13 for the memory buffer assignments.)

3.2.3.1 Memory Organization. Each 8K memory module (see Figure 3-22) is composed of 64 32 x 32 bit chips (or 64 32 x 64 chips for the 16K modules) arranged in four 1024 (2048*) 16-bit word groups. Each module, therefore, contains 4096 (8192*) words of storage. There are two sets of address lines. The A set come from the processor and the B lines come from the display adapter. They both perform the same function. Address lines 0, 1, and 2 (0 and 1*) select one of the modules. Address lines 3 and 4 (2 and 3*) select one of the four word groups (A, B, C, or D). Address lines 5 through 9 (4 - 9*) and 10 through 14 point to the word location by selecting its X and Y coordinates, respectively. Thus each of the 16 1024 or 2048* bit chips in a selected group contain one bit of each of the 1024 or 2048* words stored in the group.

Within each chip is a 32 x 32 (32 x 64*) MOS memory matrix, plus gating, temporary storage, and addressing circuitry (see Figure 3-23). The 32 bit columns selected by address lines 10 through 14 for all memory chips in the 4 groups are read out into 32 bit temporary storage registers during the first phase of the memory cycle (Ø1). There is a temporary storage register for each memory chip. During the second phase of the cycle (Ø2), the data is read back into the same memory locations, thus providing the necessary refresh for the selected 32 bit columns of data in each of the 4 groups in the memory module.

During write operations, while the 32 bit columns are in the temporary storage registers, the appropriate row of bits is selected, from the selected group's sixteen 32-bit columns by decoding address lines 5 through 9 (4 through 9*). Only the selected group may be written into. Writing occurs during phase 1 of the memory cycle. Phase 2 is identical with the refresh operation described above.

For read operations, there is no phase 2 of the memory cycle, so all reads occur in a shorter time period (800 ns) than all refreshes or writes (1.2 μs). The chip select (CS) gate gates out the selected bits from the temporary storage register onto the data output lines. Address bits 2 through 9 select the bit row to output.

3.2.3.2 Basic Memory Timing. See Figure 3-23. Each memory module remains in the standby mode until it has been selected by the activation of the associated Display Adapter Request line, DAREQ (or LKOUT*) or selected by the processor through appropriate coding of address bus lines A0, A1, A2. Once selected, the memory module goes into a busy state to prevent interference from any subsequent memory request until this memory cycle has been completed. The busy state also initiates an internal counter that serves as timing control during the memory cycle.

*16K memory

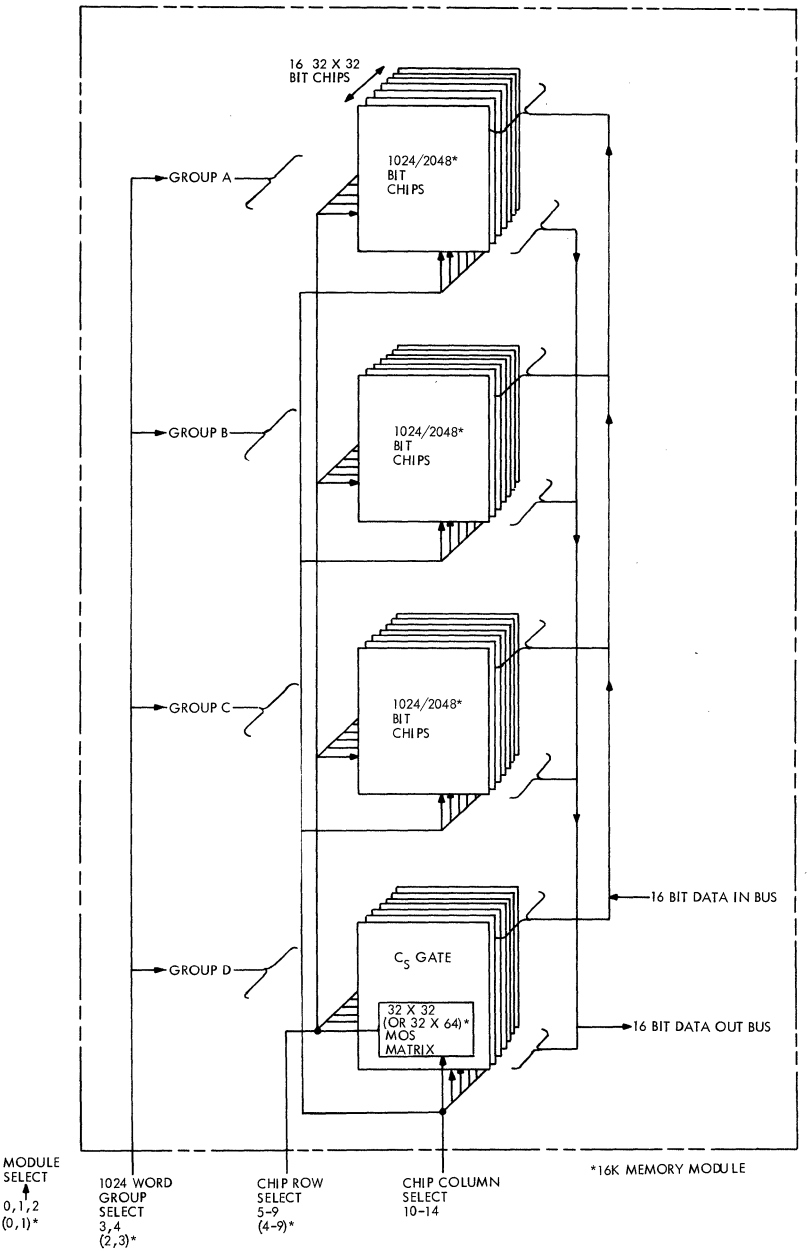


Figure 3-22. Module Memory Organization

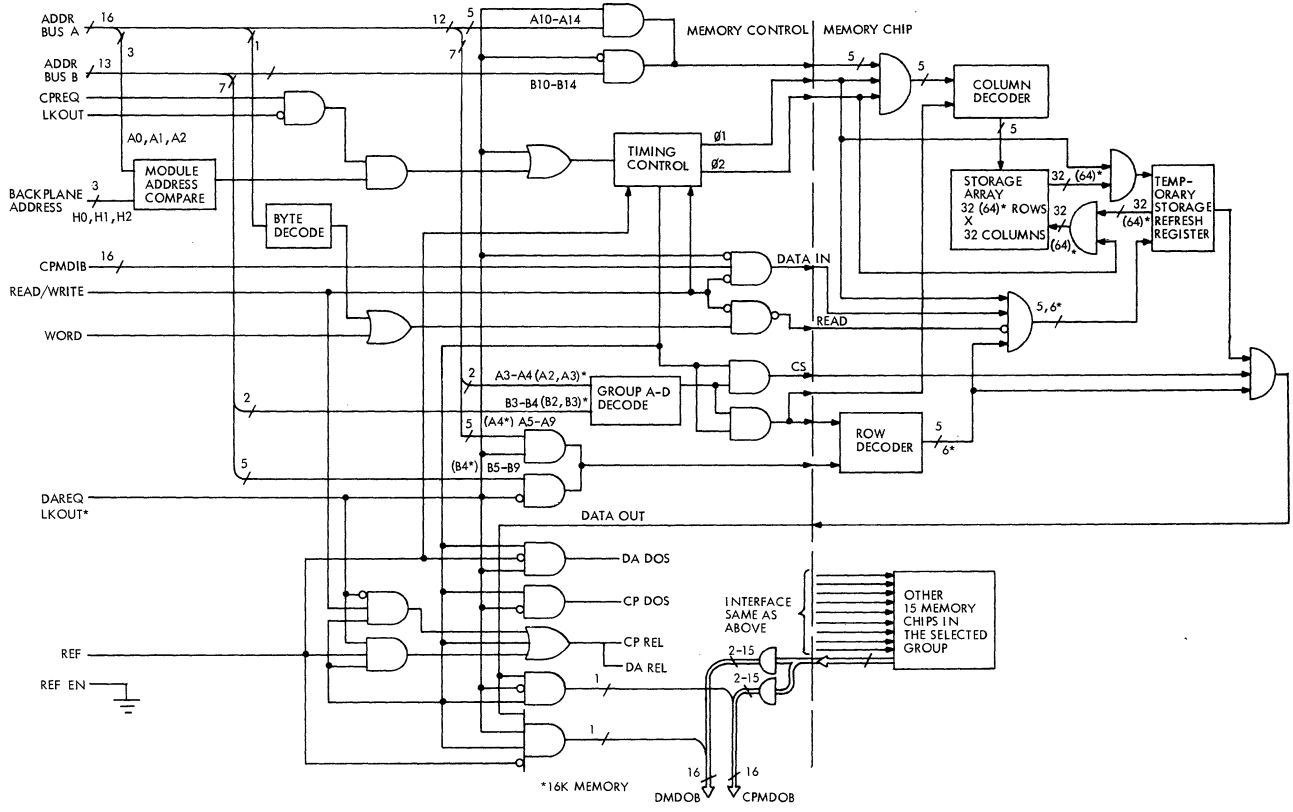


Figure 3-23. Memory, Functional Block Diagram

After the addressing, a phase 1 (Ø1) gate signal is sent to the memory chips to read out the column of data addressed by the column address lines from the storage array into the temporary storage refresh registers. The next step depends upon the requested operation. In the read mode, one data bit from each of the 16 addressed memory chips storage registers is read out to the appropriate data output line — DMDOB for display data out (DAREQ high) and CPMDOB for processor data out (DAREQ low). A data output strobe is also generated (DADOS or CPDOS) to signal that valid data is now on the output bus. In the write mode, each of the 16 data bits is read from the data input bus (CPMDIB) into its associated addressed temporary storage register refresh cell. In the refresh mode, only the columns are addressed and the associated column in each of the four groups is read into the temporary storage storage refresh registers. After this no action occurs for the balance of the phase 1 gate signal.

At the completion of phase 1, the timing control circuit either returns the system to a not busy state (if a read has been performed) or initiates a phase 2 (Ø2) gate signal (if write or refresh is being accomplished). Memory chip circuit action is similar for write and refresh during phase 2. For write, the information contained in the 32 (or 64*) refresh register cells is read back into the addressed column of the memory chips. For refresh, the information contained in all the refresh storage registers for the four groups is read back into the addressed memory chip columns. In memory refresh mode, the display adapter addresses (B10-B14) and refreshes each memory column in turn.

3.2.3.3 Interface Signals. This section describes the memory interface lines shown in Figure 3-23. Address bus A from the processor (ADDR Bus A) contains the selected module address on lines A0, A1, and A2, and the selected word address within that module on lines A3 through A14. In addition, A15 is provided to select either left or right byte during a write operation.

Address bus B from the associated display adapter (ADDR Bus B) contains the selected word address within the module on lines B3 (B2)* through B14. No byte operation capability is provided to the displays and the module select is hardwired through a dedicated DAREQ (LKOUT)* line, one for each module.

CPREQ indicates that the processor is requesting a memory operation. If the memory is not busy and a lockout signal has not been sent from the display adapter, presence of this signal will start a memory cycle in the requested module. If the memory is busy, or lockout is present, the processor (CP) memory cycle will not start until these two lines are both clear.

*16K memory

Display lockout (LKOUT) is a signal line from the display adapter notifying the memory module that a display request is imminent, and it prevents the implementation of a processor memory request at this time, thus giving priority to the display adapter. In the 16K memory LKOUT is used in place of DAREQ.

Backplane address lines H0, H1, and H2 designate the proper bit coding for the module address. By having this address hardwired on the backplane instead of in the memory module, all memory modules are kept identical and interchangeable.

The data in bus (CPMDIB) is a 16 line parallel bus that allows complete memory words to be written into memory.

The read/write line indicates whether a processor read or write operation should be performed.

The word line is utilized by the processor to distinguish between byte and word operations during a write cycle.

The display adapter request line, DAREQ (LKOUT)* is a separate line for each memory module from its associated display adapter. It notifies the memory module that a display memory cycle is requested. The module, unless already busy, will immediately initiate the requested cycle.

The refresh line (REF) is used by the display adapter to tell the memory whether a read or refresh operation should be performed.

Refresh enable (REFEN) is a ground signal used to notify the display adapter that the memory module is connected to the system.

The display adapter data output strobe (DADOS) is used as a timing signal by the memory module to tell the display adapter when valid data is present on the corresponding data output bus. The CP data output strobe (CPDOS) performs a similar function for the processor.

* 16K memory

Processor release (CPREL) and display adapter release (DAREL) are signals sent to either the processor or the display adapter depending on the memory operation being performed to indicate that the selected memory cycle is almost complete.

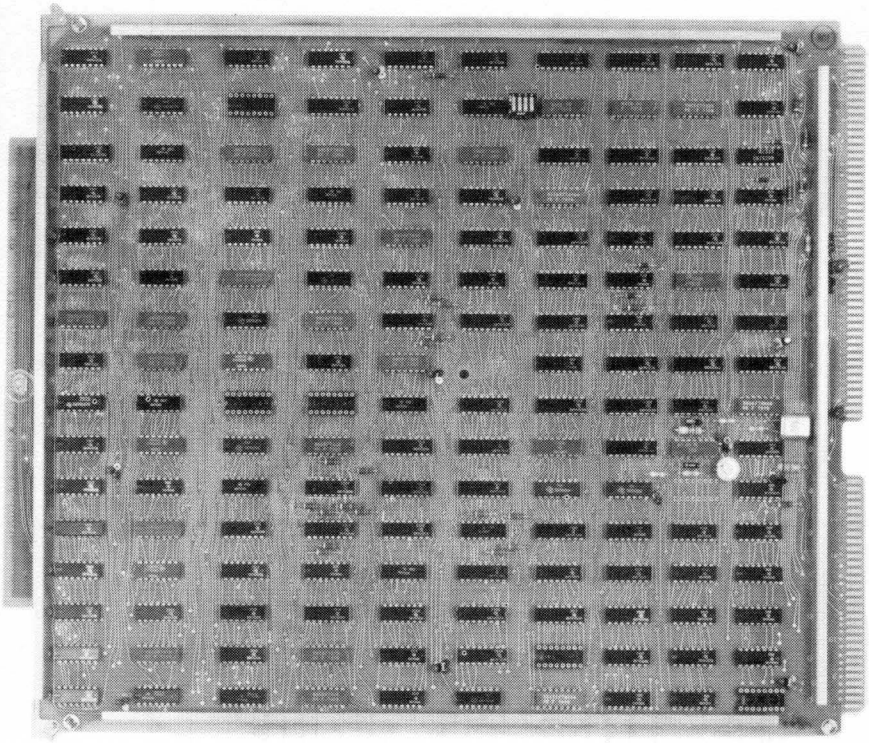
There are two sets of data output lines — CPMDOB and DMDOB — serving the processor and display adapter, respectively. Both are 16 bits, and are only valid during the associated output strobe. There are separate sets of display data output lines for each memory module. However, the processor output lines are connected in parallel between all memory modules.

3.2.4 Multiplex Channel Controller

The multiplex channel controller with its associated I/O device adapters provides an interface between the processor and the various low speed I/O devices. As an interface unit, the controller receives and executes instructions from both the processor and the I/O devices, performs necessary data buffering between them, and reports on the status of the I/O devices to the processor. The controller is mounted on a single plug-in board, as shown in Figure 3-24. Also physically located on this board is the keyboard adapter which is described in Section 3.2.9.

3.2.4.1 Multiplex Channel Controller Circuit Description. Figure 3-25 is a simplified block diagram of the multiplex channel controller. The controller contains various buffer registers, logic gates, a 16 word memory stack, and sequence control circuits. The controller interfaces with the processor over a 16-bit bidirectional data bus, three control buses and a clock bus. It supplies two system clocks, the 160 ns and the 25 MHz clocks. One of the three control buses, the interrupt bus, allows the low speed devices, or device adapters, to interrupt the processor through the controller. A second control bus, the function code bus, is used by the controller to give instructions to the arithmetic logic unit (ALU) within the processor. The available function code instructions are shown in Table 3-10. The third control bus provides the necessary timing and response signals to transfer data and address information across the data bus.

The controller interfaces with a maximum of eight I/O device adapters through an 8 bit adapter data bus, two control buses, and three individual control lines per adapter. These lines are adapter request (REQ), processor acknowledge (ACK), and processor enable (ENB). The control buses include the control out bus, with 10 control lines from the controller to all device adapters, and the control in bus, with 3 control lines in common from all device adapters to the controller. (A detailed description of all interface lines with the multiplex channel controller was given in Section 3.1.)



C74-1315

Figure 3-24. Multiplex Channel Controller

Table 3-10. Function Code Instructions

Hexadecimal Function Code	Name	Function
1	Output Word +N	Add contents of memory to the value of word N sent to processor by controller. Send result to controller. DO NOT disturb the value stored in memory. Output the ALU, carry out for addition.
2	Input Word	Input a word to memory.
3	Input Byte	Input a byte to memory address specified by controller during address in.
4	Output Word Add 1 to memory	Output a word from memory to data bus; then increment the word by 1 and put new value back into memory. Output ALU; carry out for addition.
5	Out Word Add 2 to memory	Same as 4 above except increment by 2.

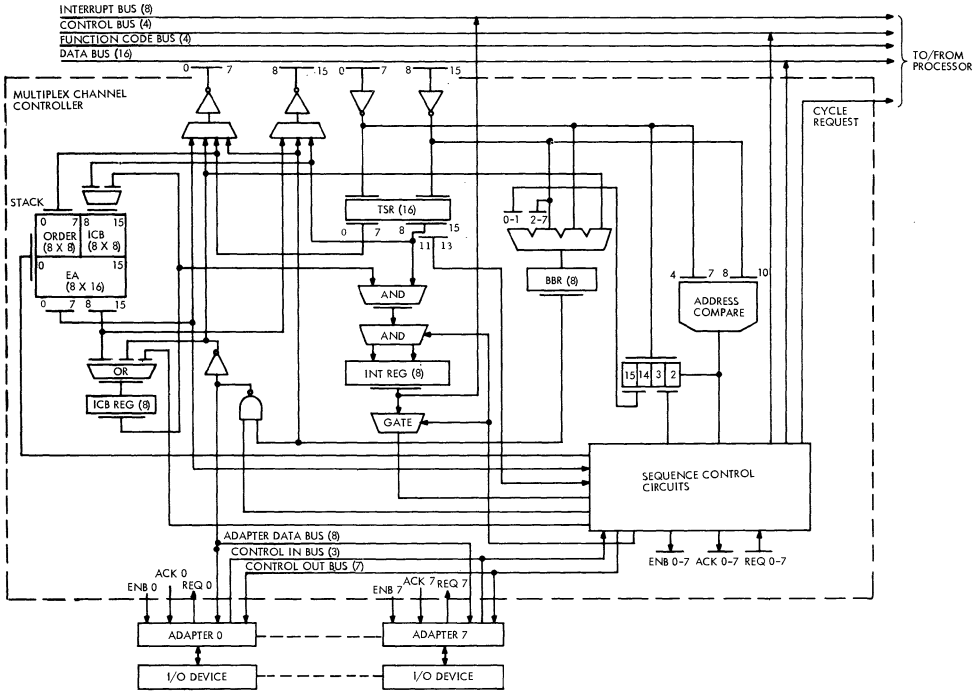
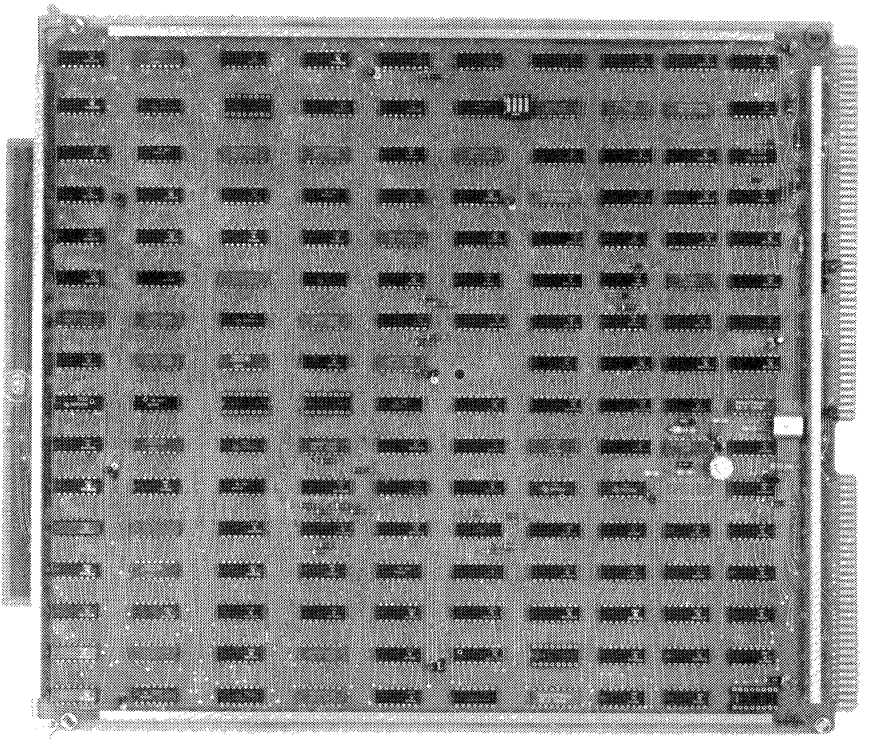


Figure 3-25. Multiplex Channel Controller, Simplified Block Diagram



C74-1315

Figure 3-24. Multiplex Channel Controller

Table 3-10. Function Code Instructions

Hexadecimal Function Code	Name	Function
1	Output Word +N	Add contents of memory to the value of word N sent to processor by controller. Send result to controller. DO NOT disturb the value stored in memory. Output the ALU, carry out for addition.
2	Input Word	Input a word to memory.
3	Input Byte	Input a byte to memory address specified by controller during address in.
4	Output Word Add 1 to memory	Output a word from memory to data bus; then increment the word by 1 and put new value back into memory. Output ALU; carry out for addition.
5	Out Word Add 2 to memory	Same as 4 above except increment by 2.

Table 3-10. Function Code Instructions (cont)

Hexadecimal Function Code	Name	Function
6	Output Word	Output a word from memory.
7	Output Word Add N to memory	Output a word from memory to data bus, then increment the word by N (subsequently sent from controller). Put new value back into memory. Output ALU, carry out for addition.
8	Set PC	Input a word to program counter.
C, D, E, F	Used by CE Console Only	

The controller responds to two basic instructions from the processor: Do I/O (either start or stop an I/O operation) and Read I/O (either read status or read and reset status). The processor places these instructions on the data bus in addition to the address code for the selected controller and device. The processor then raises the device address window (DAW) control line to identify this data as address information to the controller. For a start DIO instruction, the processor immediately places the effective address of the PIOT table for the addressed device on the data bus. The controller takes this data word and stores it in the effective address portion of its memory stack. From this point on, the controller takes control of the I/O operation, requesting information from the PIOT table, using the arithmetic unit in the processor as necessary through operation of the 4 bit function code bus, and writing data into, or reading data from, the designated portion of memory.

The controller can also pass on a request from an I/O device to start an I/O operation, by raising its cycle request line to the processor. This line is enabled by the processor each memory cycle by means of the request start window (RSW) control line.

Major circuits within the multiplex channel controller are the address compare circuits, the temporary store register, the byte buffer register, the ICB register, the interrupt register, a memory stack, and sequence control circuitry.

The address compare circuits monitor the addresses presented on the processor data bus during a DIO or RIO instruction to determine the start of an input-output operation. When the correct controller address is decoded, the control sequencer starts (or stops) the appropriate I/O device, or reads its status from the ICB portion of the memory stack. After reading status, the processor can reset the ICB bits. To start an operation, the sequencer enables the addressed I/O adapter, stores the effective address (EA) and order code in the memory stack, and sends the appropriate order to the addressed I/O adapter.

The 16 bit temporary storage register (TSR) holds all data and instructions from the processor while the controller is responding to them.

The 8 bit byte buffer register (BBR) holds all data transferred between the processor and the I/O device. During write mode, the BBR receives one byte of data at a time and transfers it to the I/O device data bus. In the read mode, the BBR receives the data from this bus and transfers it to the processor data bus.

The 8 bit ICB register holds the interrupt condition bits (ICB) when writing into or reading out of the memory stack. The interrupt condition byte, associated with each I/O device, contains within its 8 bits the reasons for the interrupt. These reasons are listed in Table 3-11.

Table 3-11. Interrupt Condition Byte

Interrupt Condition Bit	Function
0	Search Found
1	Byte Count = 0
2	Start Issued While Not Ready
3	Device End of Record (EOR)
4	Attention
5	Error (CRC & Data Overrun)
6	Not Used
7	Not Used

The interrupt register holds the interrupt bits associated with each I/O device after these have been compared to the interrupt mask stored in the PIOT table. This mask is brought into the temporary storage register during a Fetch Interrupt Mask instruction issued by the sequencer through the function code bus. It is compared to the bits stored in the ICB stack for the device being interrogated. If a match occurs (that is, if the processor is looking for the interrupt condition found), an interrupt line will be raised to the processor. A patchboard is supplied with the controller to specify the lines raised by each external device. (The processor will only respond to the interrupt if the external interrupts have been enabled by the program.)

The memory stack stores 256 bits of data through flip-flop storage. It holds eight 16-bit effective addresses, eight 8-bit order codes, and eight 8-bit interrupt condition bytes. All eight associated I/O device adapters have their own assigned areas within the memory stack. The order code and the effective address is loaded during a Do I/O start instruction; the ICB data comes from the addressed I/O device or its adapter.

Sequence control circuits contain the necessary timing logic and control circuitry to allow the multiplexer to perform each of its eight major functions: read I/O status, read/reset status, stop I/O, read, write, search, translate, and interrupt. The operation of each of these functions is shown in the functional flow diagrams, Figure 3-26.

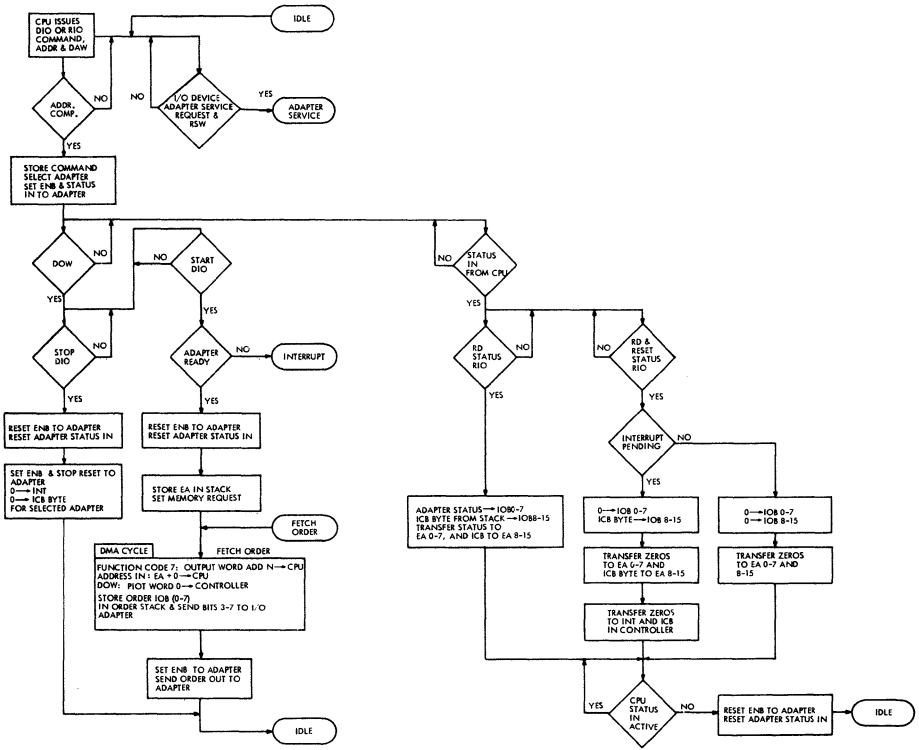


Figure 3-26. Multiplex Channel Controller, Flow Diagram (Sheet 1 of 4)

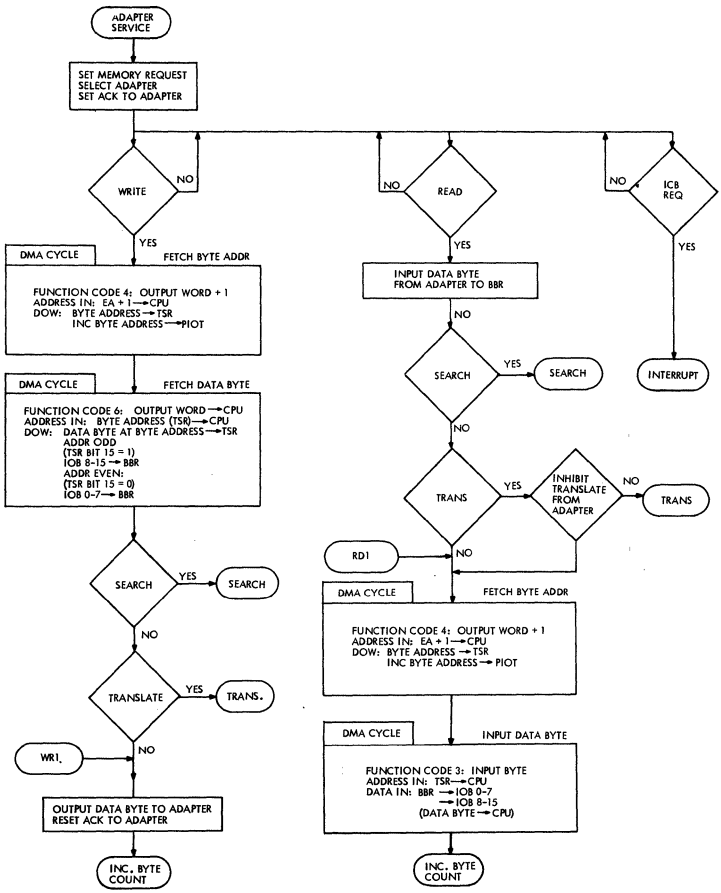


Figure 3-26. Multiplex Channel Controller, Flow Diagram (Sheet 2 of 4)

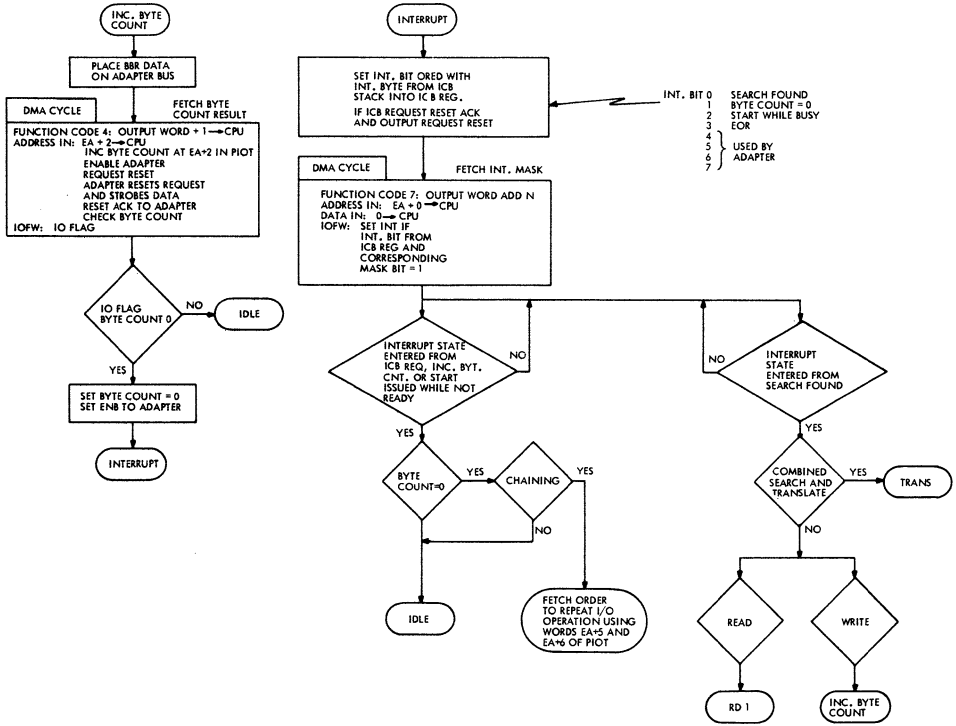


Figure 3-26. Multiplex Channel Controller, Flow Diagram (Sheet 3 of 4)

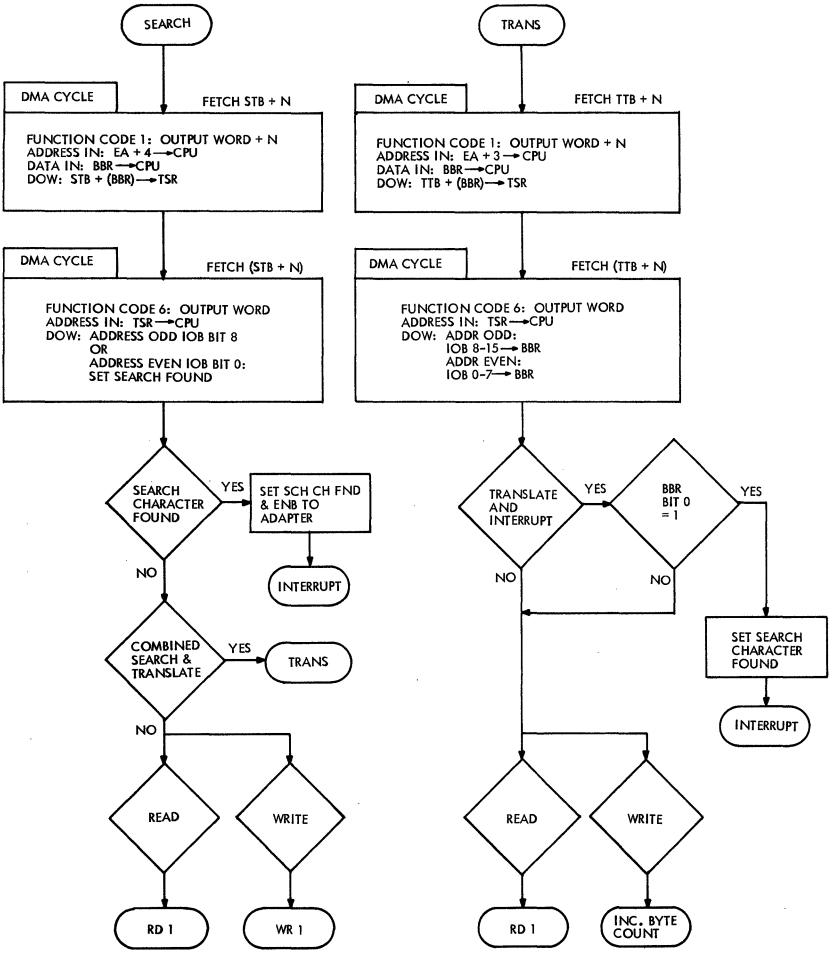
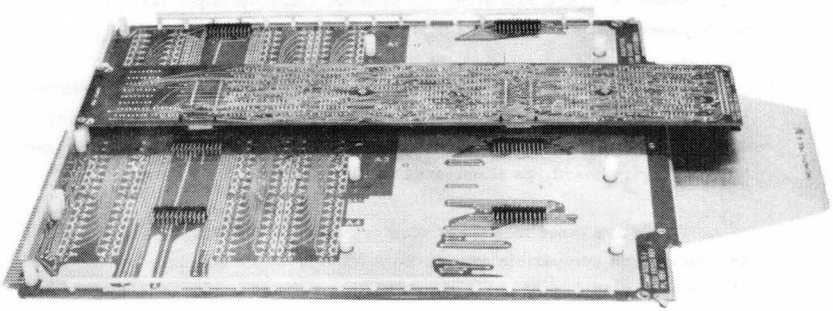


Figure 3-26. Multiplex Channel Controller, Flow Diagram (Sheet 4 of 4)

3.2.5 Motherboard Description

The motherboard, Figure 3-27, holds the various adapters used with the PTS-100 system. It provides the interconnection wiring between these adapters and the multiplex channel controller. Table 1-2 (Chapter 1) indicates the amount of space occupied by each I/O device adapter on the motherboard, and the number of multiplex subchannels required. Each motherboard, then, can support from one to four I/O adapters, depending upon the adapter's size. Since each multiplex controller has either seven or eight subchannels available (one subchannel is assigned to the keyboard adapter), the required number of multiplex controllers and motherboards required in a system, after the number and type of I/O devices have been specified, can be determined (refer to Table 1-2).

The motherboards also contain a series of 48 screw switches to specify to the multiplex controller which low speed device is attached to each data port (Figure 3-28). Specifically, they connect the request, acknowledge, and enable lines to a specific device adapter. For those adapters having both transmit and receive functions, screw switches are provided for both transmit and receive signals.



C-73-565

Figure 3-27. Motherboard with I/O Adapter

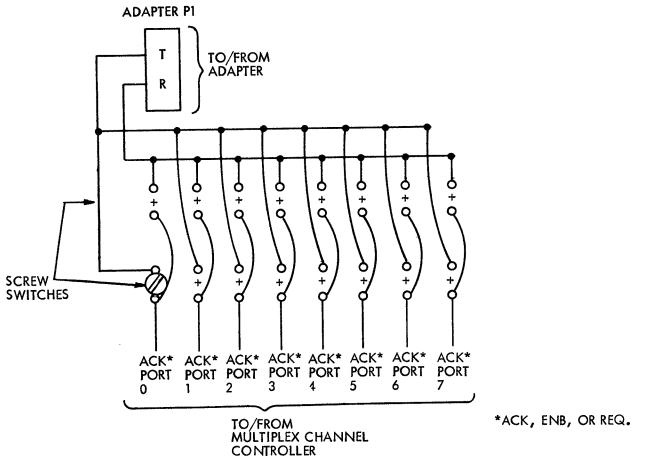


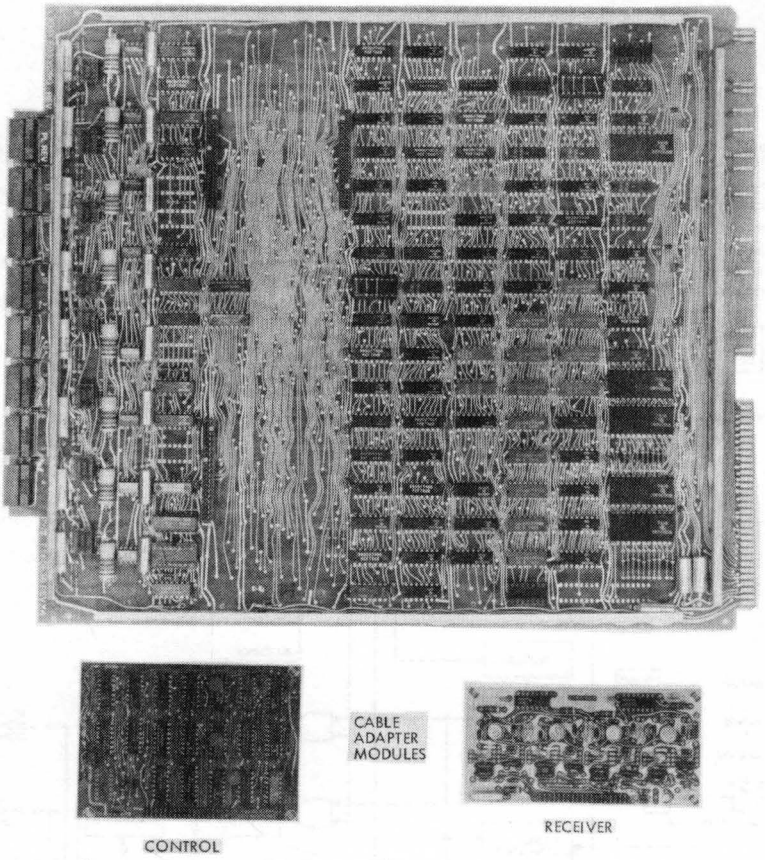
Figure 3-28. Motherboard Simplified Screw Switch, Wiring Diagram

3.2.6 Display Adapter

The display adapter (DA) provides the interface between the monitor controllers (which drive the displays) and the memory modules. The DA also multiplexes keyboard data from the monitor controllers for transmission to the keyboard adapter in the multiplex channel controller.

Each display adapter can handle a maximum of eight monitor controllers, and there is a maximum of four display adapters in a PTS system, depending upon system configuration. Each adapter is physically packaged on one plug-in board, as illustrated in Figure 3-29.

There are three models of display adapter: A, B, and C. All models are backwards compatible except the A model, which can only be used with 8K memory modules; it has a standard 2ms refresh period; the B and C models can be used with either the 8K or 16K memory modules using 1 or 2ms refresh; only the C model can be used with coaxial cable to the monitor controllers, in which case optional control and receiver modules are plugged into the display adapter(s).



C75-1848/1850

Figure 3-29. Display Adapter

Figure 3-30 is a simplified block diagram of the display adapter. The adapter performs four functions: generates 2 ms and 64.1 μs system clocks; time multiplexes keyboard data; initiates memory refresh; and formats of display data.

3.2.6.1 System Clocks. The display adapter uses the 25 MHz clock from the multiplex channel controller as the master clock for its own timing circuits. These circuits synchronize internal adapter operations, and produce 67 ms, 2 ms and 64.1 μs clocks. The 67 ms clock synchronizes the keyboard adapter, and the 2 ms and 64.1 μs clocks are used both internally and as system clocks (64.1 μs is the time of one horizontal display sweep line).

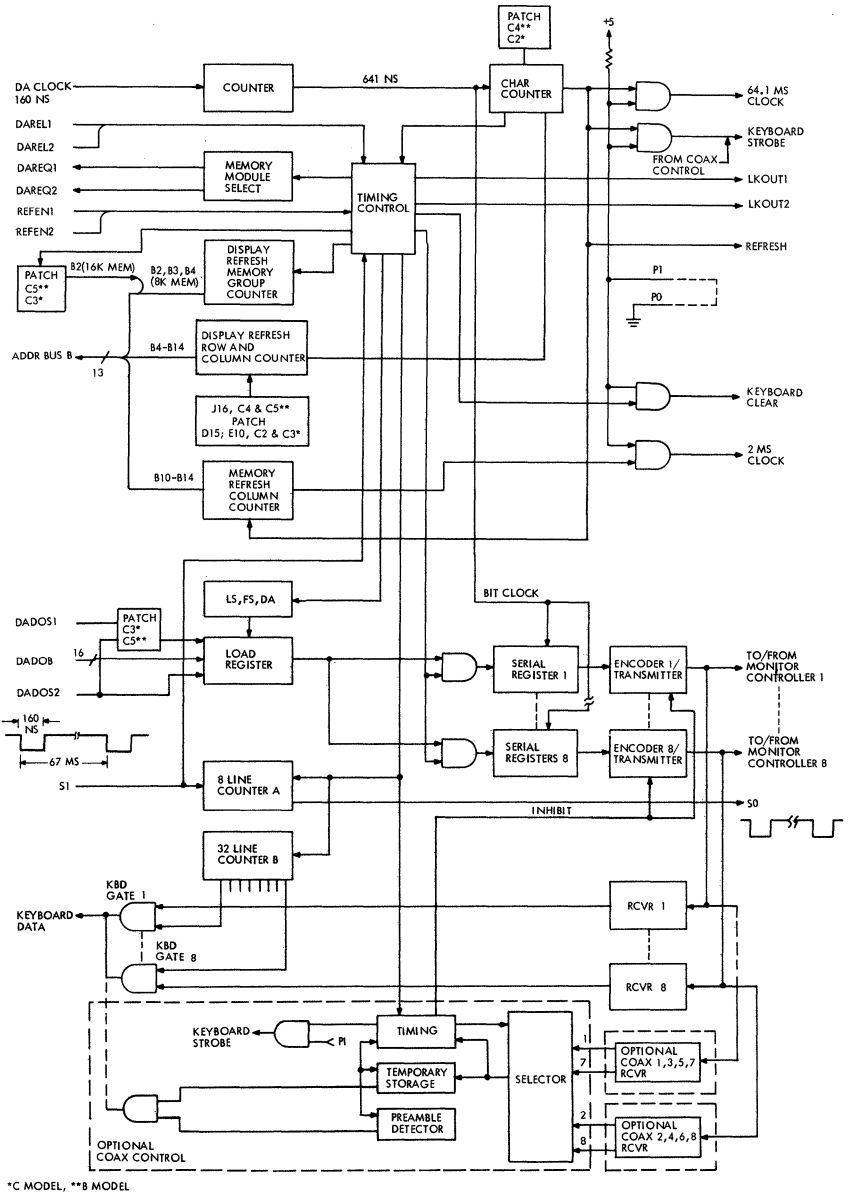


Figure 3-30. Display Adapter Simplified Block Diagram

Sync in (SI) and sync out (SO) lines are provided to interlock all display adapters in the PTS-100 model 1020 so that the display adapter installed in board slot A16 provides the master timing for all adapters. The SO signal is the SI signal delayed by eight horizontal display line times or 512.8 μs. This staggers the display adapter timing and keeps the returned keyboard data separate. Only the first display adapter produces the keyboard adapter master timing signals; all other display adapters are synchronized to the first.

3.2.6.2 Memory Refresh Circuits. Each display adapter initiates memory refresh for its associated two memory modules every 64.1 μs. Memory refresh takes place during the time that line sync (LS) characters are sent to the monitor controllers. All the even numbered modules are refreshed first, followed by all the odd numbered modules, both being completed during the same line sync time period (5.12 μs). Even though the other display adapters are offset in time, all refresh occurs during the same time, since the offset is an even multiple of line sync character times.

Refresh is accomplished by the display adapter which raises its refresh (REF) and appropriate display request (DAREQ1 or DAREQ2) lines, and cycles through all of the 32 memory column addresses. The memory is organized so that a column of data in each of the 16 chips in all 4 groups on the memory board is refreshed at the same time, thus completing refresh for each memory board (either 8K or 16K) in 32 refresh cycles. Since a refresh cycle is completed every 64.1 μs, complete memory refresh takes 2.05 ms. When two memory boards are installed they are refreshed alternately. Memory refresh circuitry is located on the memory modules, with only the timing, column address counter, and refresh initiation circuitry located on the display adapter. No data can be sent to the display adapter during memory refresh, so refresh occurs during display line sync time periods, when no data is required by the display.

3.2.6.3 Keyboard Data Circuits. The data from the keyboards (maximum of four per monitor controller) is carried from the monitor controller to the display adapters over the same lines used for sending display data to the monitor controllers. The display data uses balanced lines, and the keyboard data uses unbalanced lines, thus ensuring separation of the data (except for coax; refer to Section 3.2.6.6). The received data is applied to keyboard data gates in the display adapter. These gates multiplex the data from each keyboard into a single data stream (at a 15.6 kHz bit rate) and send it to the keyboard adapter (See Section 3.2.9).

An 8 bit data character is gated out from each keyboard once every four display refresh frames, or 15 times a second. The keyboard gating sequence is shown in Table 3-12, and it occurs regardless of the number of keyboards in actual use.

Table 3-12. Keyboard Sequencing

Display Adapter	Display Adapter Channel to Monitor Controllers	Data Transferred During Display Horizontal Line Number	Keyboard Numbers & Addresses			
			Frame 1	Frame 2	Frame 3	Frame 4
			MC Port 0	MC Port 1	MC Port 2	MC Port 3
1	1	1- 8	K1 (81)	K33 (A1)	K65 (C1)	K97 (E1)
2	1	9- 16	K2	K34	K66	K98
3	1	17- 24	K3	K35	K67	K99
4	1	25- 32	K4	K36	K68	K100
1	2	33- 40	K5	K37	K69	K101
2	2	41- 48	K6	K38	K70	K102
3	2	49- 56	K7	K39	K71	K103
4	2	57- 64	K8	K40	K72	K104
1	3	65- 72	K9 (89)	K41 (A9)	K73 (C9)	K105 (E9)
2	3	73- 80	K10	K42	K74	K106
3	3	81- 88	K11	K43	K75	K107
4	3	89- 96	K12	K44	K76	K108
1	4	97-104	K13	K45	K77	K109
2	4	105-112	K14	K46	K78	K110
3	4	113-120	K15	K47	K79	K111
4	4	121-128	K16(90)	K48 (B0)	K80 (D0)	K112 (F0)
1	5	129-136	K17	K49	K81	K113
2	5	137-144	K18	K50	K82	K114
3	5	145-152	K19	K51	K83	K115
4	5	153-160	K20	K52	K84	K116
1	6	161-168	K21	K53	K85	K117
2	6	169-176	K22	K54	K86	K118
3	6	177-184	K23	K55	K87	K119
4	6	185-192	K24	K56	K88	K120
1	7	193-200	K25 (99)	K57 (B9)	K89 (D9)	K121 (F9)
2	7	201-208	K26	K58	K90	K122
3	7	209-216	K27	K59	K91	K123
4	7	217-224	K28	K60	K92	K124
1	8	225-232	K29	K61	K93	K125
2	8	233-240	K30	K62	K94	K126
3	8	241-248	K31	K63	K95	K127
4	8	249-256	K32 (A0)	K64 (C0)	K96 (E0)	K128 (80)

A keyboard load occurs under control of bit 8 in the display address character. When this bit is a one (once every display frame) an 8 bit character from one of the four associated keyboards is allowed to pass through the monitor controller and display adapter to the keyboard adapter. The keyboard which is selected in any given frame is controlled by bits 1 and 2 of the display address character. These bits change once each frame counting to four for the four attached keyboards. Hence, any given keyboard's data is accepted every four frames (15 times a second).

To understand the keyboard timing, refer to Table 3-12. There can be up to four display adapters. Each display adapter requests keyboard data every 32 horizontal line times, from its eight associated monitor controllers. Each monitor controller alternates between its associated keyboards every fourth frame. Each display adapter is offset by eight horizontal line times from the preceding display adapter, and each requests keyboard data from its associated monitor controllers every 32 line times. It takes eight horizontal line times to transmit the keyboard character serially (eight bits at 64.1 μs per bit). Thus, with the exception of the final four line times in any display frame, all available time is multiplexed among all keyboards when a full complement (128) of keyboards is attached to the system. The time slots are still provided, even if fewer keyboards are attached.

The monitor controller is discussed in more detail later in this section, and a listing of all keyboard codes is presented in Section 3.3.

3.2.6.4 Display Format Control. The data for each display is stored in memory at the locations shown in Tables 3-13 and 3-14. The data for all displays attached to a display adapter (via the monitor controllers) is stored in the two 8K memory modules or the top 16K memory module connected to that adapter. The display adapter automatically reads the data alternately from the 8K memory modules or alternately from the upper and lower halves of the top 16K memory module under control of the display refresh address counters, formats it into eight data streams, and sends each data stream to a monitor controller. For 16K memories an additional memory address line (B2) is used to address the extra 32 rows of memory data. (Refer to Section 3.2.3.) This extra line is patched on patch C3 or C5. Prior to transmission each data train is encoded in a Manchester code to provide clock information for the monitor controller (refer to Section 3.2.7.1). The following paragraphs describe the format of the transmitted data in general. Refer to Section 3.2.6.5 for details of variations of this data transmission as a function of the number and character formats of the attached displays. Note when the display adapter is used with 16K memory boards it refreshes all 32K of memory but it can only read data for display refresh from the top 16K memory board.

Table 3-13. Display Data Memory Buffer Locations and Keyboard Addresses

Display Adaptor	Channel	Monitor	1920 Char/Display 80 Ch X 24 Lines 64 Ch X 30 Lines		960 Char/Display 80 Ch X 12 Lines 64 Ch X 15 or 16 Lines		960 Char/Display 40 Ch X 24 Lines		480 Char/Display 40 Ch X 12 Lines	
			Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address
1	1	0	0000-07FF	81	0000-03FF	81	0000-03FF	81	0000-01FF	81
		1					0400-07FF	A1	0200-03FF	A1
		2			0400-07FF	C1			0400-05FF	C1
		3							0600-07FF	E1
	3	0	0800-0FFF	89	0800-0BFF	89	0800-0BFF	89	0800-09FF	89
		1					0C00-0FFF	A9	0A00-0BFF	A9
		2			0C00-0FFF	C9			0C00-0DFF	C9
		3							0E00-0FFF	E9
	5	0	1000-17FF	91	1000-13FF	91	1000-13FF	91	1000-11FF	91
		1					1400-17FF	B1	1200-13FF	B1
		2			1400-17FF	D1			1400-15FF	D1
		3							1600-17FF	F1
	7	0	1800-1FFF	99	1800-1BFF	99	1800-1BFF	99	1800-19FF	99
		1					1C00-1FFF	B9	1A00-1BFF	B9
		2			1C00-1FFF	D9			1C00-1DFF	D9
		3							1E00-1FFF	F9
	2	0	0200-27FF	85	2000-23FF	85	2000-23FF	85	2000-21FF	85
		1					2400-27FF	A5	2200-23FF	A5
		2			2400-27FF	C5			2400-25FF	C5
		3							2600-27FF	E5
	4	0	2800-2FFF	8D	2800-2BFF	8D	2800-2BFF	8D	2800-29FF	8D
		1					2C00-2FFF	AD	2A00-2BFF	AD
		2			2C00-2FFF	CD			2C00-2DFF	CD
		3							2E00-2FFF	ED
	6	0	2000-37FF	95	3000-33FF	95	3000-33FF	95	3000-31FF	95
		1					3400-37FF	B5	3200-33FF	B5
		2			3400-37FF	D5			3400-35FF	D5
		3							3600-37FF	F5
	8	0	3800-3FFF	9D	3800-3BFF	9D	3800-3BFF	9D	3800-39FF	9D
		1					3C00-3FFF	BD	3A00-38FF	BD
		2			3C00-3FFF	DD			3C00-3DFF	DD
		3							3E00-3FFF	FD
2	1	0	4000-47FF	82	4000-43FF	82	4000-43FF	82	4000-41FF	82
		1					4400-47FF	A2	4200-43FF	A2
		2			4400-47FF	C2			4400-45FF	C2
		3							4600-47FF	E2
	3	0	4800-4FFF	8A	4800-4BFF	8A	4800-4BFF	8A	4800-49FF	8A
		1					4C00-4FFF	AA	4A00-4BFF	AA
		2			4C00-4FFF	CA			4C00-4DFF	CA
		3							4E00-4FFF	EA
	5	0	5000-57FF	92	5000-53FF	92	5000-53FF	92	5000-51FF	92
		1					5400-57FF	B2	5200-53FF	B2
		2			5400-57FF	D2			5400-55FF	D2
		3							5600-57FF	F2
	7	0	5800-5FFF	9A	5800-5BFF	9A	5800-5BFF	9A	5800-59FF	9A
		1					5C00-5FFF	BA	5A00-5BFF	BA
		2			5C00-5FFF	DA			5C00-5DFF	DA
		3							5E00-5FFF	FA
	2	0	6000-67FF	86	6000-63FF	86	6000-63FF	86	6000-61FF	86
		1					6400-67FF	A6	6200-63FF	A6
		2			6400-67FF	C6			6400-65FF	C6
		3							6600-67FF	E6
	4	0	6800-6FFF	8E	6800-6BFF	8E	6800-6BFF	8E	6800-69FF	8E
		1					6C00-6FFF	AE	6A00-6BFF	AE
		2			6C00-6FFF	CE			6C00-6DFF	CE
		3							6E00-6FFF	EE
	6	0	7000-77FF	96	7000-73FF	96	7000-73FF	96	7000-71FF	96
		1					7400-77FF	B6	7200-73FF	B6
		2			7400-77FF	D6			7400-75FF	D6
		3							7600-77FF	F6
	8	0	7800-7FFF	9E	7800-7BFF	9E	7800-79FF	9E	7800-79FF	9E
		1					7C00-7FFF	BE	7A00-7BFF	BE
		2			7C00-7FFF	DE			7C00-7DFF	DE
		3							7E00-7FFF	FE

Table 3-13. Display Data Memory Buffer Locations and Keyboard Addresses (cont)

Display Adaptor	Channel	Monitor	1920 Char/Display 80 Ch X 24 Lines 64 Ch X 30 Lines		960 Char/Display 80 Ch X 12 Lines 64 Ch X 15 or 16 Lines		960 Char/Display 40 Ch X 24 Lines		480 Char/Display 40 Ch X 12 Lines	
			Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address
3	1	0	8000-87FF	83	8000-83FF	83	8000-83FF	83	8000-81FF	83
		1					8400-87FF	A3	8200-83FF	A3
		2			8400-87FF	C3			8400-85FF	C3
		3							8600-87FF	E3
	3	0	8800-8FFF	8B	8800-8BFF	8B	8800-8BFF	8B	8800-89FF	8B
		1					8C00-8FFF	AB	8A00-8BFF	CB
		2			8C00-8FFF	CB			8C00-8DFF	EB
		3							8E00-8FFF	EB
	5	0	9000-97FF	93	9000-93FF	93	9000-93FF	93	9000-91FF	93
		1					9400-97FF	B3	9200-93FF	B3
		2			9400-97FF	D3			9400-95FF	D3
		3							9600-97FF	F3
	7	0	9800-9FFF	9B	9800-9BFF	9B	9800-9BFF	9B	9800-99FF	9B
		1					9C00-9FFF	BB	9A00-9BFF	BB
		2			9C00-9FFF	DB			9C00-9DFF	DB
		3							9E00-9FFF	FB
	2	0	A000-A7FF	87	A000-A3FF	87	A000-A3FF	87	A000-A1FF	87
		1					A400-A7FF	A7	A200-A3FF	A7
		2			A400-A7FF	C7			A400-A5FF	C7
		3							A600-A7FF	E7
	4	0	A800-AFFF	8F	A800-ABFF	8F	A800-ABFF	8F	A800-A9FF	8F
		1					AC00-AFFF	AF	AA00-ABFF	AF
		2			AC00-AFFF	CF			AC00-ADFF	CF
		3							AE00-AFFF	FF
	6	0	B000-B7FF	97	B000-B3FF	97	B000-B3FF	97	B000-B1FF	97
		1					B400-B7FF	B7	B200-B3FF	B7
		2			B400-B7FF	D7			B400-B5FF	D7
		3							B600-B7FF	F7
	8	0	B800-BFFF	9F	B800-BBFF	9F	B800-BBFF	9F	B800-B9FF	9F
		1					BC00-BFFF	BF	BA00-BBFF	BF
		2			BC00-BFFF	DF			BC00-BDFF	DF
		3							BE00-BFFF	FF
4	1	0	C000-C7FF	84	C000-C3FF	84	C000-C3FF	84	C000-C1FF	84
		1					C400-C7FF	A4	C200-C3FF	A4
		2			C400-C7FF	C4			C400-C5FF	C4
		3							C600-C7FF	E4
	3	0	C800-CFFF	8C	C800-CBFF	8C	C800-CBFF	8C	C800-C9FF	8C
		1					CC00-CFFF	AC	CA00-CBFF	AC
		2			CC00-CFFF	CC			CC00-CDFF	CC
		3							CE00-CFFF	EC
	5	0	D000-D7FF	94	D000-D3FF	94	D000-D3FF	94	D000-D1FF	94
		1					D400-D7FF	B4	D200-D3FF	B4
		2			D400-D7FF	D4			D400-D5FF	D4
		3							D600-D7FF	F4
	7	0	D800-DFFF	9C	D800-DBFF	9C	D800-DBFF	9C	D800-D9FF	9C
		1					DC00-DFFF	BC	DA00-DBFF	BC
		2			DC00-DFFF	DC			DC00-DDFF	DC
		3							DE00-DFFF	FC
	2	0	E000-E7FF	88	E000-E3FF	88	E000-E3FF	88	E000-E1FF	88
		1					E400-E7FF	A8	E200-E3FF	A8
		2			E400-E7FF	C8			E400-E5FF	C8
		3							E600-E7FF	E8
	4	0	E800-EFFF	90	E800-E8FF	90	E800-EBFF	90	E800-E9FF	90
		1					EC00-EFFF	B0	EA00-EBFF	B0
		2			EC00-EFFF	D0			EC00-EDFF	D0
		3							EE00-EFFF	F0
	6	0	F000-F7FF	98	F000-F3FF	98	F000-F3FF	98	FF00-F1FF	98
		1					F400-F7FF	B8	F200-F3FF	B8
		2			F400-F7FF	D8			F400-F5FF	D8
		3							F600-F7FF	F8
	8	0	F800-FFFF	A0	F800-FBFF	A0	F800-FBFF	A0	F800-FBFF	A0
		1					FC00-FFFF	C0	FA00-FBFF	C0
		2			FC00-FFFF	E0			FC00-FDFF	E0
		3							FE00-FFFF	80

Table 3-14. LED Memory Buffer Assignments

Display Adapter	Channel	1920 Character Display	960 Character Display		480 Character Display			
			Mon. 0	Mon. 1	Mon. 0	Mon. 1	Mon. 2	Mon. 3
1	1	0780	03C0	07C0	01E0	03E0	05E0	07E0
	2	2780	23C0	27C0	21E0	23E0	25E0	27E0
	3	0F80	0BC0	0FC0	09E0	0BE0	0DE0	0FE0
	4	2F80	2BC0	2FC0	29E0	2BE0	2DE0	2FE0
	5	1780	13C0	17C0	11E0	13E0	15E0	17E0
	6	3780	33C0	37C0	31E0	33E0	35E0	37E0
	7	1F80	1BC0	1FC0	19D0	1BE0	1DE0	1FE0
	8	3F80	3BC0	3FC0	39E0	3BE0	3DE0	3FE0
2	1	4780	43C0	47C0	41E0	43E0	45E0	47E0
	2	6780	63C0	67C0	61E0	63E0	65E0	67E0
	3	4F80	43C0	4FC0	49E0	4BE0	4DE0	4FE0
	4	6F80	6BC0	6FC0	69E0	6BE0	6DE0	6FE0
	5	5780	53C0	57C0	51E0	53E0	55E0	57E0
	6	7780	73C0	77C0	71E0	73E0	75E0	77E0
	7	5F80	5BC0	5FC0	59E0	5BE0	5DE0	5FE0
	8	7F80	7BC0	7FC0	79E0	7BE0	7DE0	7FE0
3	1	8780	83C0	87C0	81E0	83E0	85E0	87E0
	2	A780	A3C0	A7C0	A1E0	A3E0	A5E0	A7E0
	3	8F80	8BC0	8FC0	89E0	8BE0	8DE0	8FE0
	4	AF80	ABC0	AFC0	A9E0	ABE0	ADE0	AFE0
	5	9780	93C0	97C0	91E0	93E0	95E0	97E0
	6	B780	B3C0	B7C0	B1E0	B3E0	B5E0	B7E0
	7	9F80	9BC0	9FC0	99E0	9BE0	9DE0	9FE0
	8	BF80	BBC0	BFC0	B9E0	BBE0	8DC0	BFE0
4	1	C780	C3C0	C7C0	C1E0	C3E0	C5E0	C7E0
	2	E780	E3C0	E7C0	E1E0	E3E0	E5E0	E7E0
	3	CF80	CBC0	CFC0	C9E0	CBE0	CDE0	CFE0
	4	EF80	EBC0	EFC0	E9E0	EBE0	EDE0	EFE0
	5	D780	D3C0	D7C0	D1E0	D3E0	D5E0	D7E0
	6	F780	F3C0	F7C0	F1E0	F3E0	F5E0	F7E0
	7	DF80	DBC0	D7C0	D9E0	DBE0	DDE0	DFE0
	8	FF80	FBC0	FFC0	F9E0	FBE0	FDE0	FFE0

Figure 3-31 shows the composite signal from the memory modules to the display adapter and the serial data transmission between the display adapter and the monitor controller for the 1920 character, 80 characters/line, 24 line format. Information from the two associated memory modules is received one word at a time (two characters) for each of the eight monitor controllers in sequence. The first word is from memory module 1, board row D, word address 0, and is for monitor controller 1. While this word is being processed by the display adapter, a word from memory module 2, board row D, word address 0 is received for monitor controller 2, followed by a word from memory module 1, board row C, word address 0 for monitor controller 3. In similar fashion, words are received for all eight monitor controllers before a second word is received for monitor controller 1. This sequence is continued until all 1024 words in each board row and memory module are transmitted. Some formats utilize all 1024 words for displaying characters. However, most only require a maximum of 960 words. In these formats, the remaining 64 words are not used, except for words 960 and 970 which are utilized for status information.

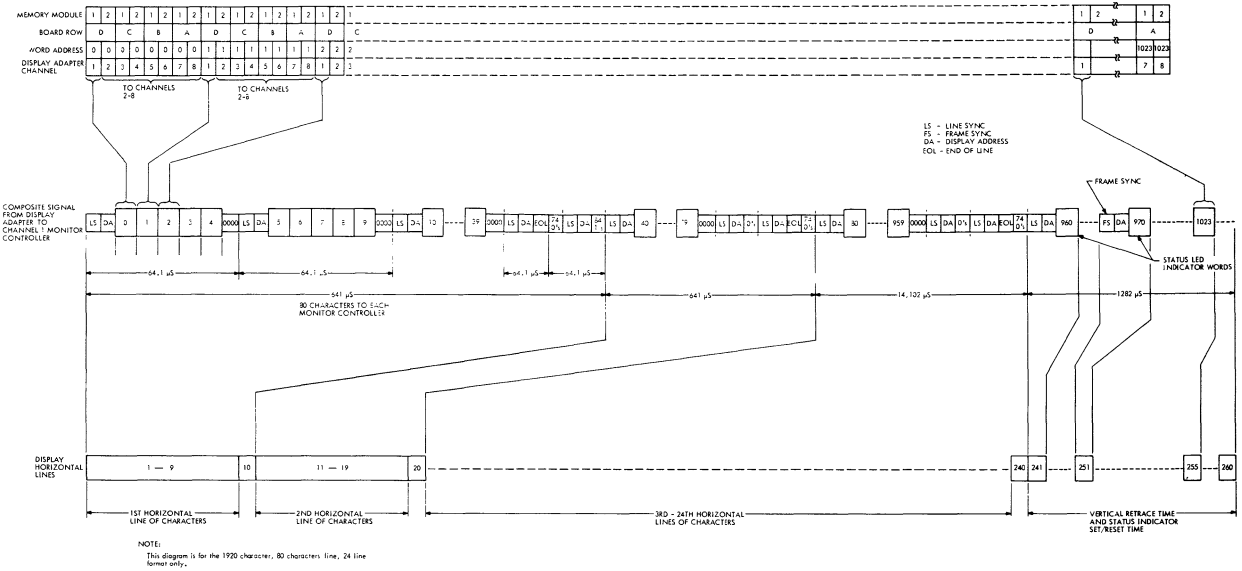


Figure 3-31. 80 Character By 24 Line Composite Signal from Display Adapter to Monitor Controller

As each word is received by the display adapter, it is stored in a separate serial shift register, one for each monitor controller. As the next seven words are being loaded into seven other shift registers, the first register is shifting its data out in a prescribed format. This serial data is encoded using FM for transmission to the monitor controllers over a shielded, twisted wire pair.

The format of the data shifted out is as follows: A line sync character (LS) and a display address character (DA) are inserted by the display adapter, followed by 10 display characters and four zeros to round out the timing to an even 64.1 μs per ten character grouping. This is followed by another LS, DA, and ten display characters with the four zeros for the second ten character grouping. This transmission is continued until a complete horizontal line of characters has been transferred (80 characters in the format shown in Figure 3-31). At this time an EOL character (end of line) is sent, followed by a series of zeros, a final LS and DA, and 84 ones. This completes transmission of one horizontal line of characters to this monitor controller, and is followed by a second and remaining lines of characters (24 lines in the format shown). After all horizontal lines of characters have been transmitted, the remaining time is used for the transmission of status information to the LEDs (word 960 and occasionally 970) while the displays are going through vertical retrace. Just prior to the transmission of word 970, a frame sync character is sent instead of the customary line sync character, thus ensuring that the displays stay in sync each frame.

The display address (DA) character tells the monitor controller which display the information is for, and which keyboard is being interrogated.

Each horizontal line of characters is vertically sliced by the character generator in the monitor controller into eight or ten display lines for character generation purposes. Eight lines are used with the 32 and 64 character/line formats and ten lines are used for the 40 and 80 character formats.

3.2.6.5 Alternate Display Formats. Display formats available include 80 and 40 characters/line in either 24 or 12 line configurations and 64 characters/line in either 30 or 15 lines. Selection among various formats is made by patch connections of the display adapter and screw switches on the monitor controller. When a 1920 character format is selected (either 80 chars/line, 24 lines or 64 chars/line, 30 lines), only two display terminals may be attached to a monitor controller. When a 960 character format is selected (40 chars/line, 24 lines; 80 chars/line, 12 lines; or 64 chars/line, 15 lines), a maximum of four (identical format) displays may be attached to a monitor controller. Finally, if a 480 character format (40 characters/line, 12 lines) is selected, four displays may be attached. The display adapter patches control the area of memory from which each display receives its data and control some format timing changes.

Figure 3-32 shows the composite signal utilized in the 64 characters/line, 30 line display formats. The diagram is similar to Figure 3-31, except that only 32 words (64 characters) are read from memory for each line. Thus, the EOL character follows the thirty-first character, and only 44 zeros are used to complete that character grouping. The entire line is transferred in 512.8 μs, instead of 641 μs. The display only has eight horizontal lines during this time period instead of ten lines for the 80 character format. Since the same number of total characters are transferred in both cases (1920), and the same number of total display horizontal lines employed (240), both formats complete their final display line at the same time. However, the location of the frame sync character is changed from horizontal line 250 to horizontal line 248.

Figure 3-33 shows the composite signal utilized in the 40 character/line 24 line format. This is similar to Figure 3-31, except that the 80 characters per horizontal line are distributed between two display terminals. The first two characters (first memory word) are sent to the first display and the second two characters sent to the second display, alternating for the entire 80 characters. Since the output alternates between displays, memory locations must alternate as the data is transferred in. This is accomplished through a patch, which alternately adds a bit in position 8 of the memory address word counter as the two different display memory locations are being utilized.

Figure 3-34 shows the composite signal utilized in the 80 character/line, 12 line format. This is also similar to Figure 3-31, except that every other line of data goes to alternate display terminals, and the internal patch forces the memory counter to alternate between 0 - 511 and 512 - 1063 memory locations through control over bit 9. Each display still goes through all 260 horizontal scanning lines; however, data is only presented on every other set of 10 lines.

Figure 3-35 shows the composite signal used in the 40 character/line, 12 line format. This combines the alternation of displays and memory locations described under the last two format descriptions.

Finally, Figure 3-36 shows the composite signal employed in the 64 character/line, 15 line formats. It is similar to the 64 character 30 line format, with the alternate line sequencing system employed.

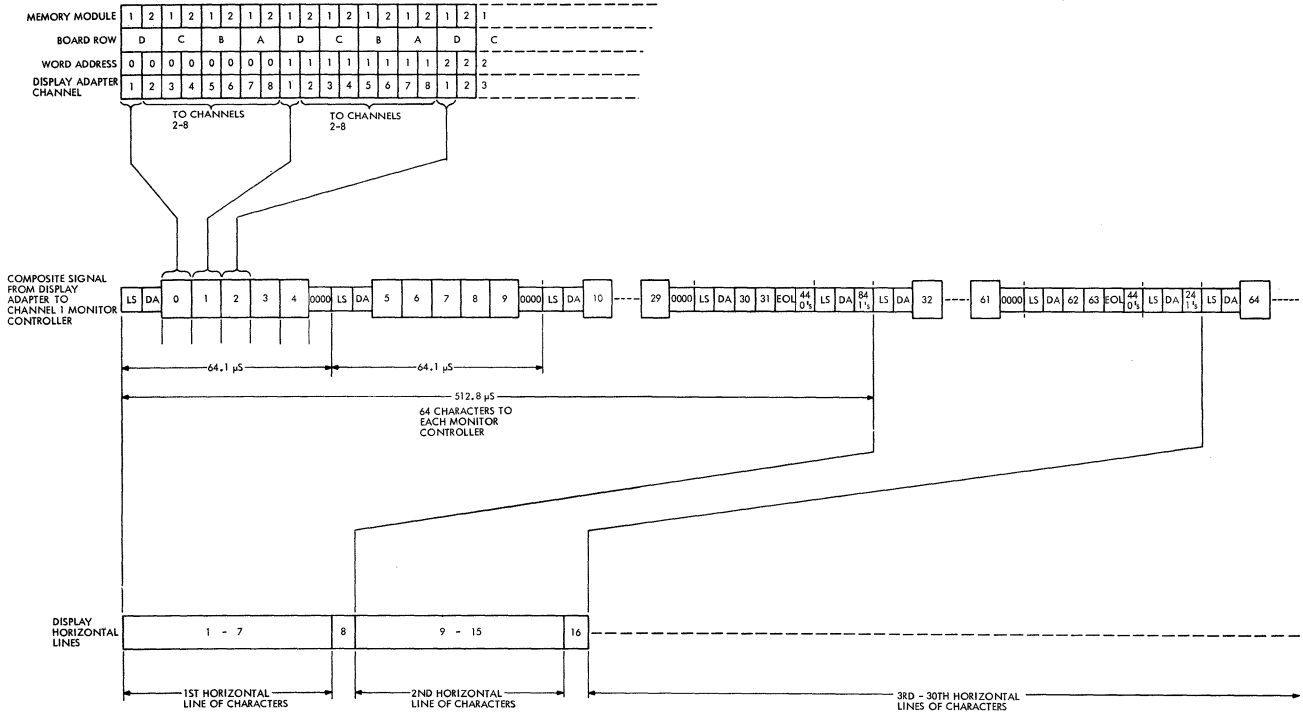


Figure 3-32. 64 Character By 30 Line Composite Signal from Display Adapter to Monitor Controller

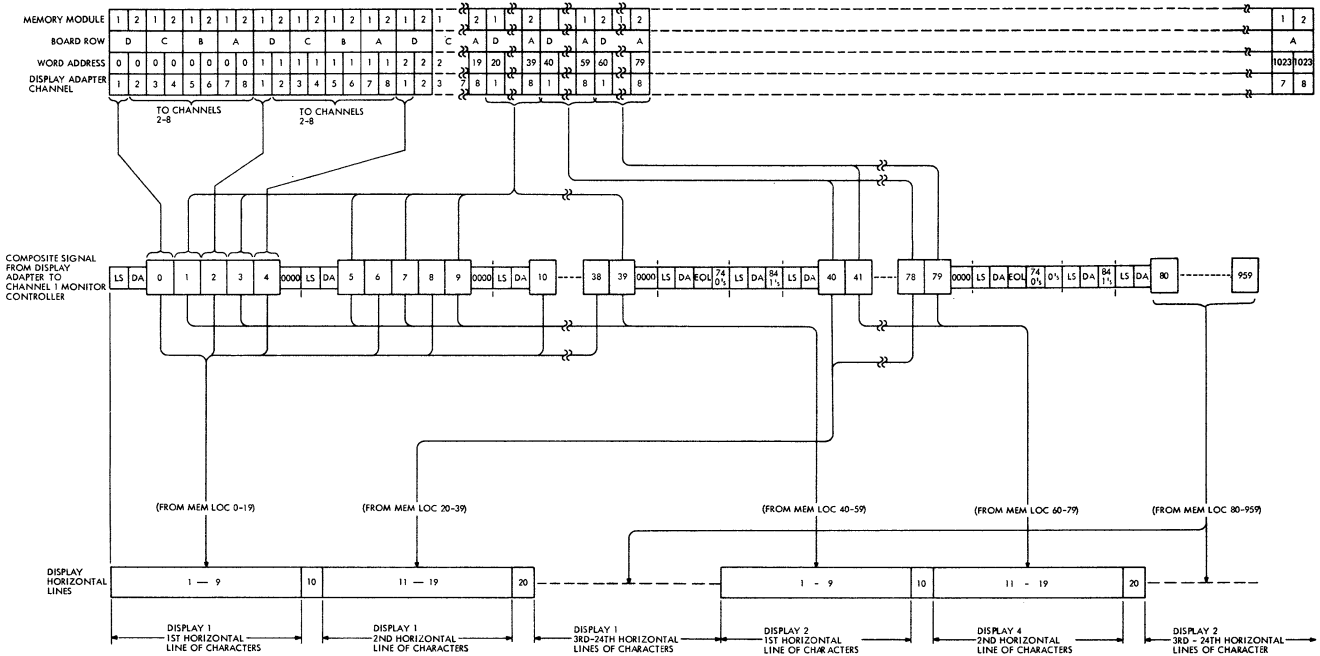


Figure 3-33. 40 Character By 24 Line Composite Signal from Display Adapter to Monitor Controller

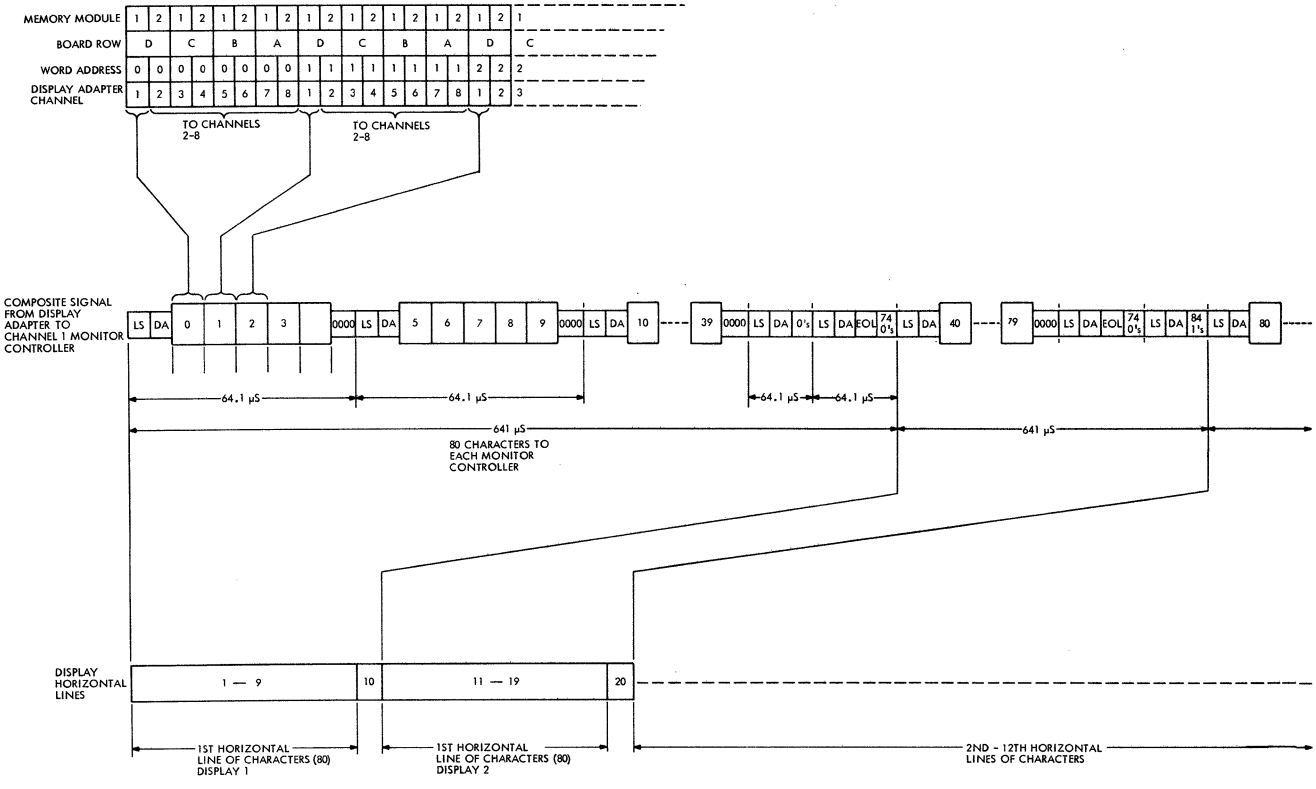


Figure 3-34. 80 Character By 12 Line Composite Signal from Display Adapter to Monitor Controller

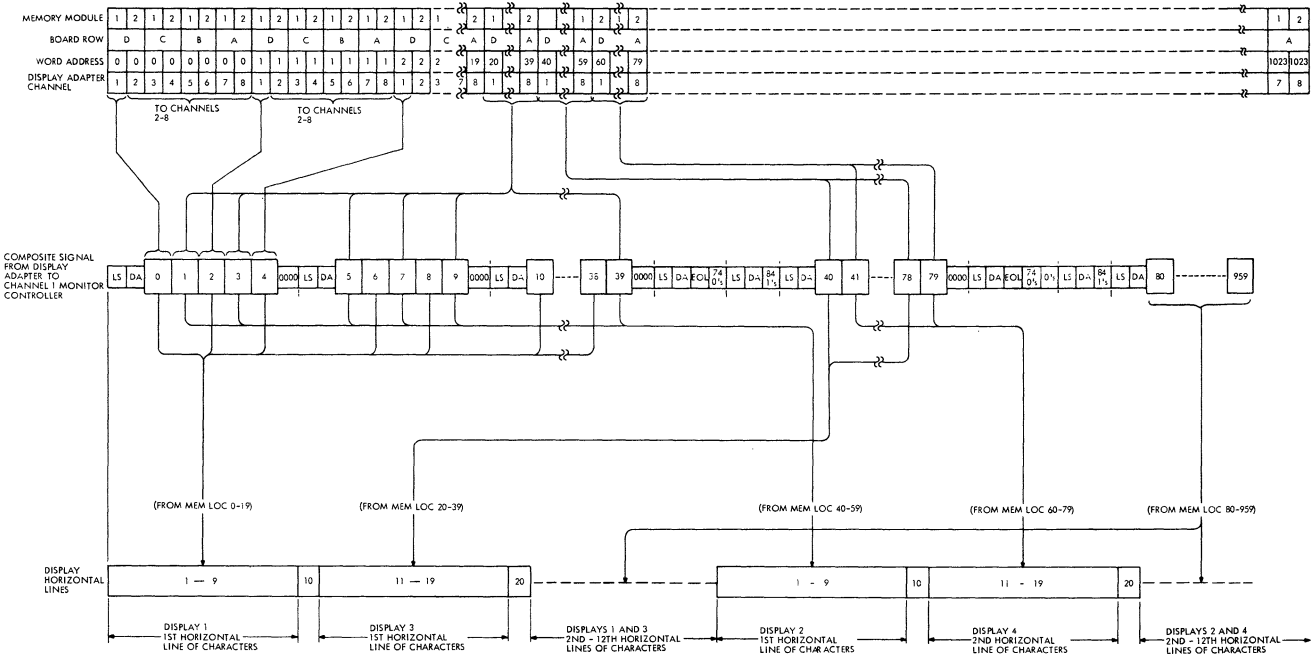


Figure 3-35. 40 Character By 12 Line Composite Signal from Display Adapter to Monitor Controller

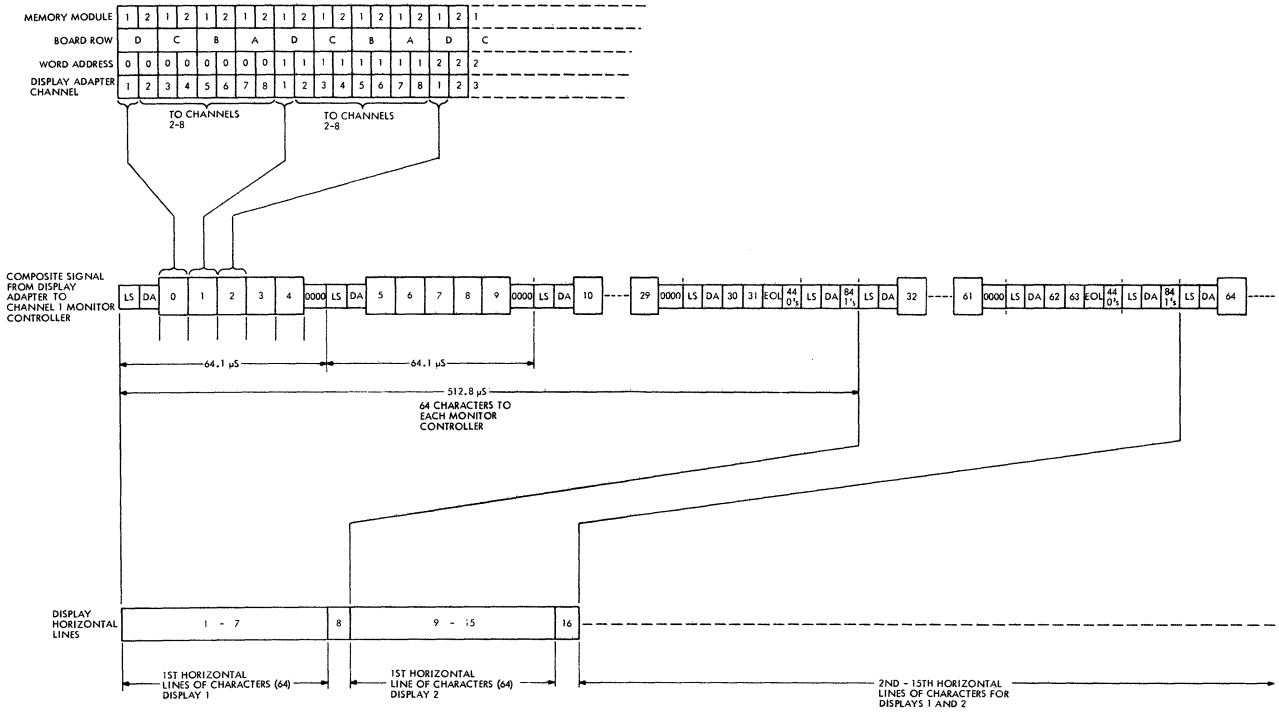
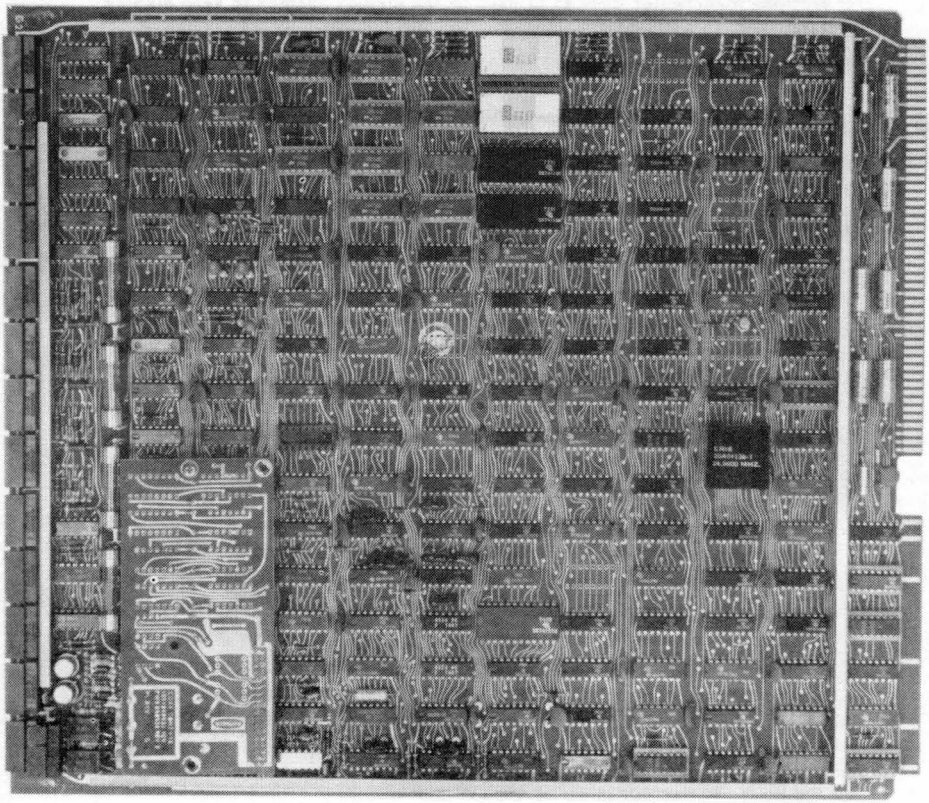


Figure 3-36. 64 Character By 15 Line Composite Signal from Display Adapter to Monitor Controller

3.2.6.6 Coaxial Cable Adapter. The coaxial cable adapter is an option that permits the monitor controllers (Model F) to be connected to the display adapters (Model C) using RG62A/U coaxial cable instead of shielded twisted pair. When using coax, the display data sent from the display adapter to the monitor controller and the keyboard data sent from the monitor controller to the display adapter both use the same coax cable on a time-shared basis. The coax adapter consists of four piggyback plug-in circuit boards. Three of the boards — two identical high speed receiver modules, and a control module (see Figure 3-29) — plug into each display adapter. The fourth board plugs into each monitor controller; it is a dual high speed transmitter module (shown mounted in Figure 3-37).



C75-1849

Figure 3-37. Monitor Controller F PC Board (with Cable Adapter Transmitter Module)

The transmitter module contains two storage shift registers, timing and preamble circuits and two high speed transmitters, one for each 1920 character screen. The keyboard data is generated in the same way as before, except that instead of being transmitted directly to the display adapter it is temporarily stored in the shift registers. Then during the seventh line for 64 character formats or during the ninth line for 40 and 80 character formats the transmitters on the display adapters are inhibited and the keyboard character is sent to the display adapter in one short burst. The keyboard characters are preceded by a unique preamble (01011110) which is also generated by the transmitter module. The keyboard character is sent during the time that zeros would have been transmitted by the display adapter so no display data is lost. The monitor controller clock "free runs" during this period. The keyboard data is sent over the cable at 1.56 MHz using the same self-clocking Manchester code as is used by the display adapter to send display data.

After the keyboard data has been sent, the display adapter transmitters are turned on and the next lines of data from the display adapter are sent to the monitor controller. The next line is 84 ones, followed by $1C_{16}$ or $1E_{16}$ which resynchronizes the monitor controller to receive the display data.

When the cable adapter is installed, the normal receivers on the display adapter are not connected and the cable adapter receivers take their place. The received keyboard characters are amplified by the associated transformer-coupled high speed cable adapter receivers. The cable adapter control module selects the receive keyboard channel, temporarily stores the keyboard character, detects the preamble, and synchronizes its timing to the received character. Then if the preamble is correct at the end of the 64.1 μs line time, it shifts the keyboard character at a 390 kHz rate out to the keyboard adapter on the multiplex channel controller. The control module also produces the keyboard strobe signal, which gates the keyboard character into the keyboard adapter. The PI signal interlocks the cable adapters so that the cable adapter on the lowest display adapter in the backplane produces the keyboard strobe for all the cable adapters. The keyboard strobe is four bursts of eight pulses 128 μs apart, repeated every 2 milliseconds. The following chart gives keyboard timing.

See Figure 2-4 for DA-MC cable connections and dual mode cable restrictions.

Cable Adapter
Keyboard Timing

DA Channel No.	DA Sends Keyboard Load to MC During Line No.	Keyboard Data From MC Sent to DA During Line No.		Keyboard Character Sent From DA to Mux During Line No.			
		64 Char.	80 Char.	DA1	DA2	DA3	DA4
1	0	6	8	9	11	13	15
2	32	38	38	41	43	45	47
3	64	70	68	73	75	77	79
4	96	102	98	105	107	109	111
5	128	134	128	137	139	141	143
6	160	166	168	169	171	173	175
7	192	198	208	201	203	205	207
8	224	230	228	233	235	237	239

3.2.7 Monitor Controller Operation

The monitor controller printed circuit boards (Figure 3-37) provide the interface between the data display and keyboards and the display adapters in the PTS-100 processing system. There are five versions of monitor controllers: B modified, C, D, F, K, and a special B-16 controller. Monitor controllers B modified, B16, and C can accommodate one 1920 character, two 960 character, or four 480 character display terminals. Monitor controllers D, F, and K have an option to accept two 1920 character or four 960 or 480 character displays. The differences between monitor controller types are discussed in Section 3.2.7.3.

During keyboard data entry, the monitor controllers send the keyboard data from the keyboards to the display adapters where it is sent to the multiplex channel controller, where the codes are translated to ASCII and stored in the memory. During display refresh, the monitor controllers convert the ASCII coded data characters from memory via the display adapter into dot patterns, and send them to the displays along with horizontal and vertical sweep signals. In systems where the displays/keyboards are located within 200 feet of the processing unit, the monitor controllers are mounted inside the processing unit cabinet. In systems where the displays/keyboards are located remotely, the monitor controllers are mounted in the remote concentrator cabinets.

3.2.7.1 Monitor Controller Functional Description. Figure 3-38 is a simplified block diagram of the monitor controller circuits. Data from the DA is encoded using the Manchester system where the data is exclusive ORed with the 1.56 MHz clock. This ensures that there is at least one transition per bit in the data stream. The resulting data stream contains 780 kHz and

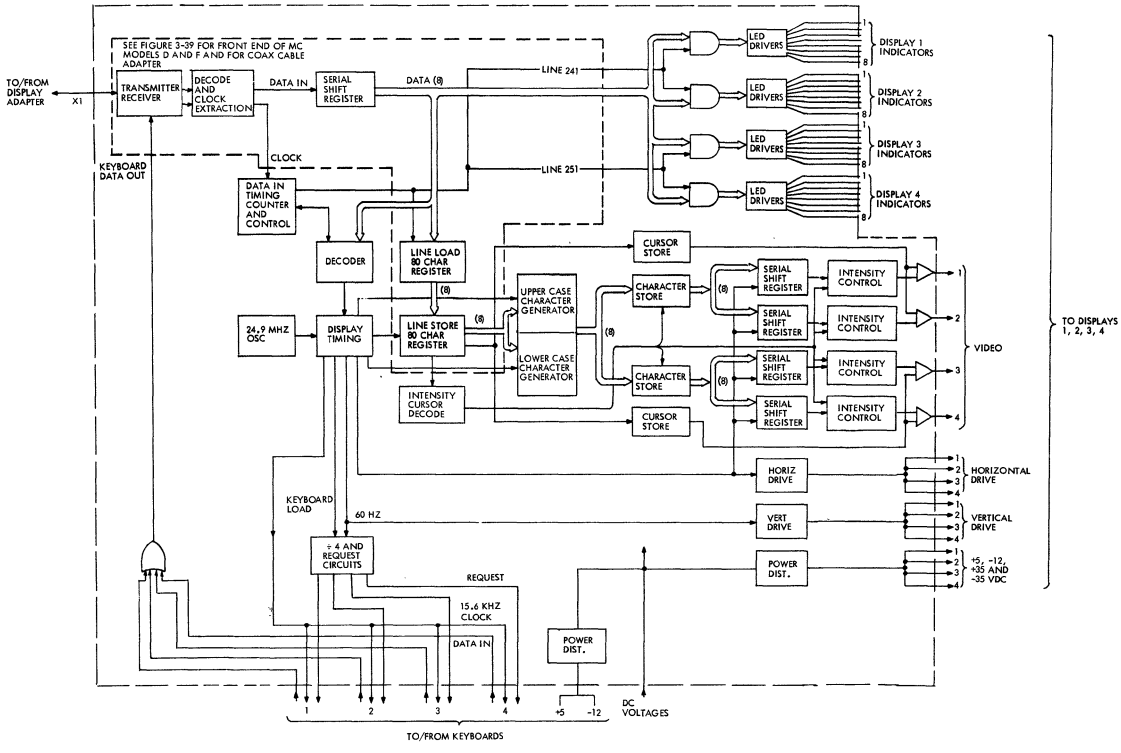


Figure 3-38. Monitor Controller, Simplified Block Diagram

1.56 MHz frequency components, which allow the MC to use bandpass filters with transformer coupling to improve noise rejection and eliminate ground potential differences. The Manchester encoded serial character data from the display adapter is decoded to restore the zero crossings, the clock extracted, and the data entered into a serial shift register, where it is read out in 8 bit parallel bytes. The extracted 1.56 MHz clock drives the data-in timing circuits, which count the incoming bits to determine the time of occurrence of data characters, line sync, frame sync, display address, and other signals. These circuits then gate the input data into the appropriate decoder, line load, or LED registers.

During the time of horizontal display line 241 (see Figure 3-31), the two 8-bit bytes from memory location 960 are gated through the LED drivers to the LED status indicators on displays 1 and 2. During the time of horizontal display line 251, the two 8-bit bytes from memory location 970 are gated through the LED drivers to the LED status indicators on displays 3 and 4. Each bit in the bytes controls one indicator. Some of the available options affect the LED status indicators. These are discussed in Section 3.2.7.3.

The decoder decodes the sync, keyboard load, and display address characters and gates the display timing circuits which clock the displays, keyboards, and data output circuits. The line load register loads complete lines of data characters (80 for 80 character/line formats) and transfers them one line at a time to the line store register. The line of characters circulates in the line store register for a period of nine horizontal display line times (seven for certain formats). During the following line time, the line store register is reloaded with a new line of characters. The line store register presents each character in the circulating character line to the character generator once during each horizontal line time.

Two character generators are provided, one supplying 64 numerical and upper case characters, and the other, 32 lower case characters. Each character generator contains a 7 x 7 or 7 x 9 dot matrix for every character or symbol to be displayed*. The character codes address the applicable dot matrixes. The first time a line of characters is presented to the character generator, the generator outputs the dot matrix pattern for the first slice of each character in the line. The second time the line is presented, the character generator outputs the dot pattern for the second slice, and so on through slice 9, whereupon a new line of characters is loaded into the line store register and read out starting with line 11. Certain configurations, notably 15, 16, and 30 line formats only utilize 7 slices for sending the characters. The deletion of the last two slices prevents use of the lower case characters.

*Some monitor controllers use character generators that are composed of PROMs instead of monolithic ICs. In these cases the PROMs are mounted on a piggyback plug-in module that plugs into the character generator chip socket.

The slice dot patterns are temporarily stored in character store registers and shifted out serially to the displays by serial shift registers. Gating signals from the display timing circuit selectively enable the shift registers to the displays. The gating signals are derived from bits 1 and 2 of the display address characters that accompany each line of characters.

The cursor, which is the eighth bit in each character code, is picked off in the line store register and sent to the output circuits to intensity modulate the associated character slices.

The display horizontal and vertical sweep signals are produced by horizontal and vertical drive circuits under control of the display timing circuit and in synchronism with the video to the displays.

The keyboards are clocked with a 15.6 kHz signal from the display timing circuit and polled by the Request signal 15 times per second when the keyboard load pulses occur. The keyboard load pulses are initiated by bit 8 of the display address characters. They are detected by the decoder and applied through the display timing circuit to the request circuit. The appropriate display address code with bit 8 set occurs once every four display frames as discussed in Section 3.2.6. The keyboard data are then transmitted to the display adapter at a 15.6 kHz bit rate or if a coax cable adapter is used, at a 1.56 MHz rate. The keyboard signal to the display adapter is a gated 40 ma +12V signal with approx imately 2.5V developed across the DA 62 ohm load.

3.2.7.2 Display Line /Character Format Selection. Chip switches or manual data chips (model F) on the controller boards modify the circuits to interface with the different displays. The chip switches or data chips control the number of characters (480, 960, or 1920), number of character lines (12, 15, 16, 24, or 30), and number of characters per line (40, 64, or 80). The switch and data chip settings are made at system installation to reflect the system character and line configuration. The settings, made at location E6, L8 or D8 are shown in Chapter 2.

3.2.7.3 Monitor Controller Variations. Several different types of monitor controllers are available, providing various system options (see Table 1-4 for the options). Monitor controller B Modified is the standard module, providing the basic system, without options. Monitor controller C provides identical functions as B Modified, but in addition offers two LED options and an intensity field option. When selected, one LED option shows display power on, and the other provides an audio tone signal instead of the LED indication. The intensity field option allows control over character intensity. Two intensity levels are provided, besides blank field. Under program control, a special character representing high, low, or blank field is transmitted with the normal data stream of characters. This changes the intensity level of all

characters after that time until a second special intensity field character is transmitted. By sending one special character followed by a regular data character, or data word, or data line(s) and then a second special character, the programmer has control over the intensity of a single character, word or line(s) as desired. By using the blank field, the program can prevent certain data from being displayed on a given terminal. This option is implemented by a decoding network that recognizes the special characters and changes the intensity level of the characters prior to transmitting them to the terminal. A blank space will occur on the display for each special character.

Monitor controller D is similar to monitor controller C, offering the two LED options and the intensity field option. In addition, it provides the capability of driving two 1920 or four 960 or 480 character displays. However, monitor controller D cannot be used with a 64 character format. Monitor controllers F and K have all the options of the D model as well as several others: they can handle all display formats (model K does not use 64 x 16); they have an optional blank and blinking data field; they can display 96 and 128 characters in 8 or 9 lines (32 char on 9 lines and 64 char on 8 lines); they have optional blinking, box or underline cursors, and they can use the coax cable adapter (refer to Section 3.2.2.6 for the description). Like model D the models F and K monitor controllers can also accommodate two 1920, four 960, or 480 character displays. All of these monitor controllers have dual front ends to handle the second display adapter data channel, which provides the data for the added display(s). The simplified block diagram of the front end circuits is shown in Figure 3-39. The two input cables must be connected to the same display adapter to provide proper timing.

The front ends of monitor controllers D, F, and K are similar. They have dual transmitter/receivers and dual serial shift, line load, and line store registers. Model D has a single decode and clock extraction circuit whereas models F and K have dual circuits. The cable delay equalizer electronically delays the faster data stream and lines it up with the slower. This corrects for any delay introduced by different length cables and puts the two data streams back in sync. The selector alternately selects the data stream to feed the character generator. In model D, the LED signals are taken off after the serial shift registers; on models F and K they are taken off at the selector. All other circuits are shared by the displays. Model F offers a sixteenth line of characters in the 64 ch/line 960 character format. Thus, it offers 1024 characters instead of 960.

Monitor controller B-16 is very similar to controller B modified. It offers one LED option (power on) only, and no intensity field option. However, it also offers a sixteenth line of characters in the 64 x 15 line

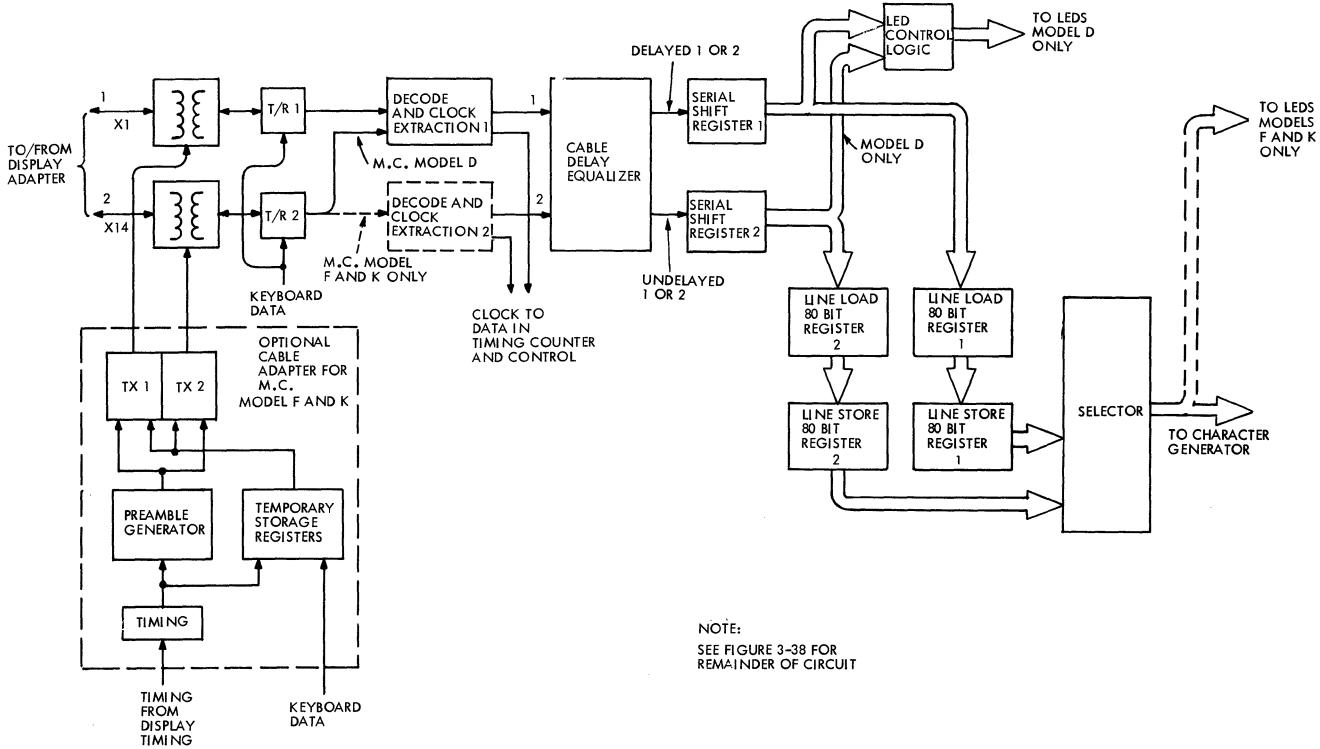


Figure 3-39. Monitor Controller Models D, F and K Front End and Cable Adapter Simplified Block Diagram

configuration (1024 characters instead of 960). The sixteenth line is flashed on and off at a 3 Hertz rate to attract attention. In this option, all the available memory spaces assigned to the display are utilized.

Monitor controller K also has the option of using a cursor word in memory to provide the cursor location instead of bit 8 of the character. Bit 8 of the characters can then be optionally used to turn the selected data field option on or off. When the cursor register option is implemented, a count that indicates the position of the cursor is maintained in memory by the program. There is one cursor count for each display and it is stored in the memory area assigned to the display. The program changes the count whenever keyboard data is received from the associated display.

The cursor count is sent to the monitor controller and stored in its cursor register during the word immediately following the LED word. There is only one cursor register on a monitor controller. When loaded, it is counted up to zero at which point the cursor is displayed on the associated display. Then the register is loaded with the count for the next display and the process repeats until a cursor has been displayed on each of the four displays on that monitor controller, whereupon it starts over again. Thus, in this mode a cursor is displayed on every fourth raster.

3.2.8 Cabinet Backplane Wiring

The PTS-100 is configured around a number of plug-in printed circuit boards and power supplies in the Central Processing Unit cabinet. These boards plug into an equipment cabinet, and utilize backplane wiring for interconnections. The arrangement of the boards is illustrated in Chapter 1 and Figure 6-1.

In addition to connector wiring, the backplane circuitry also includes four sets of bus wires, hardwired address circuitry, configuration connections, and miscellaneous components. The four sets of bus lines are the memory bus, display adapter bus, device adapter bus, and I/O bus.

To make the boards interchangable, all addressing is on the backplane. Thus, each memory and DAM board picks its address through three backplane connections (H0, H1, and H2) that provide the necessary address code information for the address compare circuits. Similarly, the display adapter boards are hardwired to the proper memory modules through the backplane wiring and, in addition, are interconnected together through the sync in (SI) and sync out (SO) lines. A jumper is provided at all display adapter locations except for the board plugged into location A16 (models 1020 and 1030). This jumper interconnects lines PI and PO (program in and program out), preventing all display adapters except A16 from

supplying system clock information. See Figure 3-88 for the DAM board locations in the backplane.

One connection on the backplane is configuration sensitive. DMA priority in is standardly jumpered to DMA priority out on all I/O J1 connectors. Whenever a multiplex channel controller is plugged into any board location, the associated priority in and priority out connection must be cut. All other connections are not configuration sensitive, and the pin connections for the motherboard, I/O adapters and multiplex channel controllers are identical, although certain pins may not be used on a given type of board.

In addition to the interconnection wiring on the backplane, components are mounted there. These components include pull-up resistors, which tie the various signal lines to the 5 volt power bus. These lines are identified to the wiring lists in Chapter 6 as open collector (OC). Also mounted on the backplane are the IPL pushbutton, the on/off switch, a power on indicator lamp, and a fuse.

See Figure 6-12 for the DC power distribution to the 20B backplane slots and see Figure 3-92 for the DC power distribution to the old 1020 backplane. The 20B backplane has four terminal boards that are used to connect the DC power supplies. These terminal boards have additional terminals other than those for the DC voltages. The purpose of each terminal is:

Terminal	
ST1, 2	Power sense status lines from the feature board. Used to cause switchover to battery backup.
SYNC	Power supply sync. Used to synchronize a switching power supply to the display horizontal line frequency from a monitor controller in the cabinet.
EXT IPL	External IPL. Carries an IPL signal to the processor to cause it to the IPL when the IPL switch on a disc unit is depressed.
SP	Spares.

The remote concentrator cabinet, when used, contains monitor controller boards to drive remote displays located up to 5000 feet from the processor. These require no interconnections (except for power). However, the remote concentrator has all the I/O bus connections wired in for future system expansion.

3.2.9 Keyboard Adapter Operation

The keyboard adapter provides the interface between the keyboards and badge reader and the processor, through the multiplex channel controller. Refer to Section 3.2.10 for badge reader operation. The keyboard adapter can service a maximum of 128 keyboards, with 32 keyboards assigned to each of 4 display adapters. Each keyboard is associated with one display terminal except for 1920 character split screen terminals which accommodate two keyboards. A maximum of four keyboards may be connected to one monitor controller, a maximum of eight monitor controllers to each display adapter, and a maximum of four display adapters in each PTS-100 processing system. Refer to Chapter 1 for the overall configuration.

The keyboard adapter is physically located on the multiplex channel controller board. (For a description of the multiplex channel controller, refer to Section 3.2.4.) Since only one keyboard adapter may be utilized in any system configuration, if a system has more than one multiplex channel controller, the associated keyboard adapter circuits on the additional controller units must be disconnected from channel 7 through the use of four DIP switches on the controller board. These switches disconnect Request, Enable, Acknowledge, and a spare line to the keyboard adapter circuits.

Keyboard data is sent from the display adapters to the keyboard adapter over a single time-shared bus at a rate of 16.5K bits/sec. The keyboard adapter strips out any all-zero characters and appends keyboard addresses (assigned in the sequence in which the keyboards are scanned for data) to the valid keyboard characters. The addressing sequence is listed in Table 3-12. Keyboard address numbers are assigned modulo 4 at each display controller and modulo 32 at each monitor controller. Each 16-bit word of keyboard information contains 7 bits of keyboard addressing, and 7 bits of keyboard data. In addition, bit 0 is always a 1, and bit 8 is a 0 for keyboards or badge readers. This format is illustrated below:

	0	1 2 3 4 5 6 7	8	9 10 11 12 13 14 15
1	1	KEYBOARD ADDRESS 1	0	CHARACTER DATA
2	1	KEYBOARD ADDRESS 2	0	CHARACTER DATA
128	1	KEYBOARD ADDRESS 128	0	CHARACTER DATA

Since all keyboard data is multiplexed on the same multiplex channel controller port, there is only one I/O control packet and one buffer area for all keyboard data. For this reason, all keyboard data has the keyboard address as part of the same word. Bit 0 is used by software control to

indicate keyboards which have new information associated with them. The keyboard address information (first eight bits) is inserted by the keyboard adapter onto the data word.

The keyboard characters (with addresses) are sent to the CPU just like any other I/O data. The CPU software puts the keyboard data into the memory screen area associated with the keyboard address and into the character location specified by the cursor address counter, which is maintained in the undisplayable portion of memory for that display. (The software also detects cursor movement and updates the cursor address as necessary.)

3.2.9.1 Keyboard Adapter Circuit Description. Figure 3-40 is a functional block diagram of the keyboard adapter circuit. Keyboard data comes in from the display adapters in a serial data stream. It is converted to parallel data, and stored in an 8-bit data register. At the same time, the keyboard strobe pulses are used to clock in the serial data and drive an address counter. The address counter counts bits and characters, with each new character corresponding to a different keyboard address. The character count (keyboard address) is alternately sent out on the adapter data bus with the data from the data register via output select gates. Status data is also available for output, and if the multiplex channel controller requests status information from the adapter, this status (e.g., is the adapter busy?) is also sent out on the output lines. Status data may be requested through the use of the enable signal.

The status flip-flop is set upon receipt of an order out command, and this circuit controls the initiation of a request signal to the controller. The status flip-flop is reset upon receipt of a BCZ or stop/reset signal, which will stop all adapter transfers of data until a new order is received.

The controller clock is used to clock several of the control circuits. Keyboard clear is used as a reset pulse to ensure that the address information is in synchronism with the keyboard data, since it resyncs every complete cycle.

Four bit switches are provided with the keyboard adapter to disconnet it if it is not being used. These switches disconnect the acknowledge, enable, request (and a spare) lines.

3.2.10 Badge Reader Operation

The badge reader (Figure 3-41) can be used with any system to provide user access control. Depending upon the user identification, access to different levels of the system can be provided under program control. The badge reader is connected into the system in series with a keyboard. This is accomplished by connecting the badge reader through a cable to a monitor controller keyboard port. The displaced keyboard is then plugged into the badge reader. A simplified badge reader circuit diagram is shown in Figure 3-42.

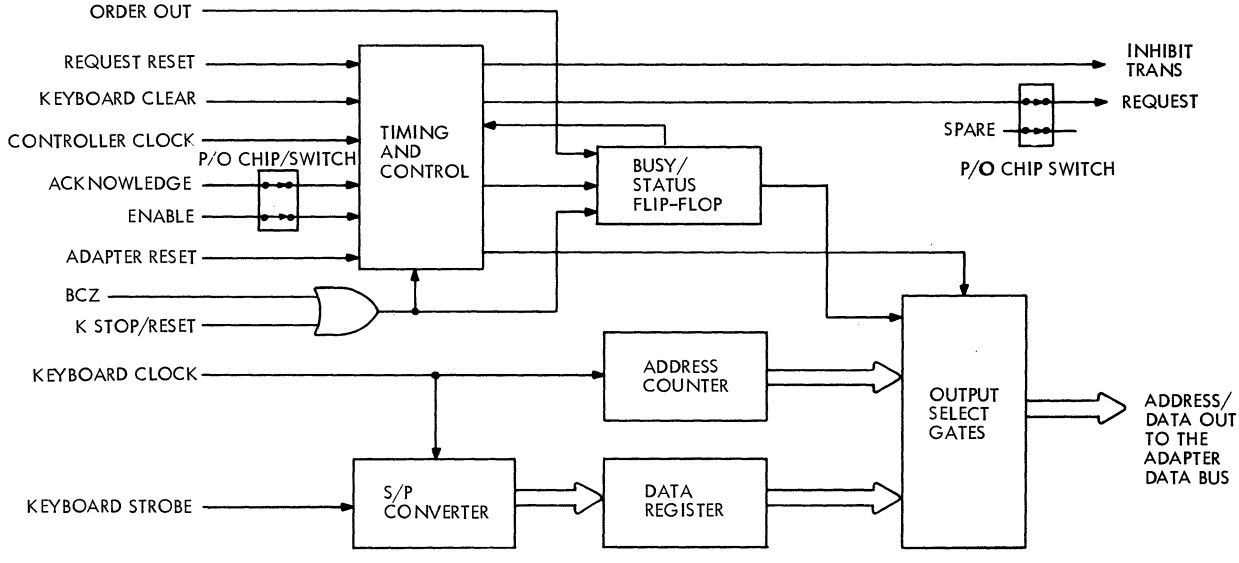
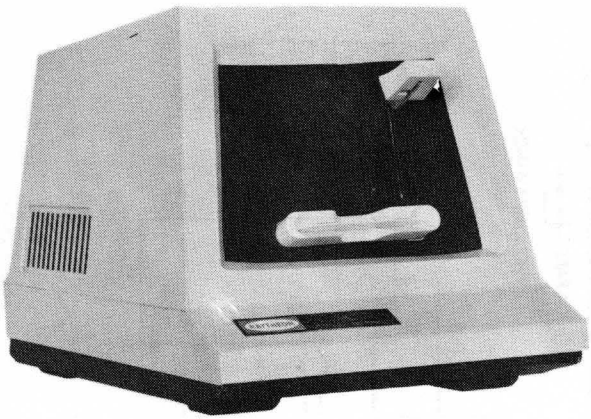


Figure 3-40. Keyboard Adapter



C73-653

Figure 3-41. Badge Reader

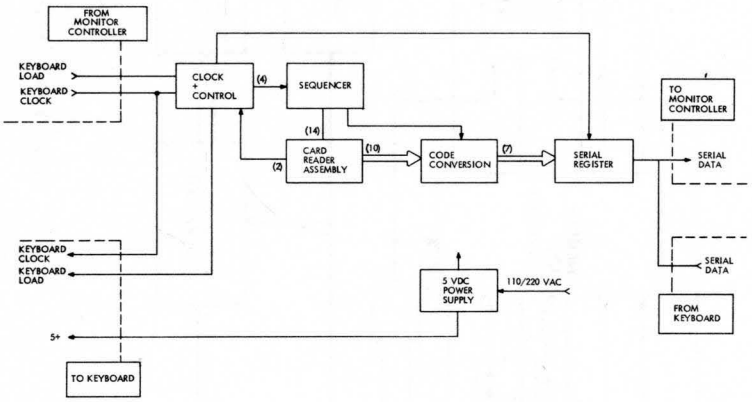


Figure 3-42. Badge Reader, Simplified Block Diagram

3.2.10.1 Badge Reader Circuit Description. The system uses a small plastic card which contains a matrix of 15 columns by 12 rows. A user identification code is punched in using only the numbers 0-9 on rows 1-14. The fifteenth column, in connection with the last two rows is used by the circuitry to detect when a card has been inserted and when it is withdrawn.

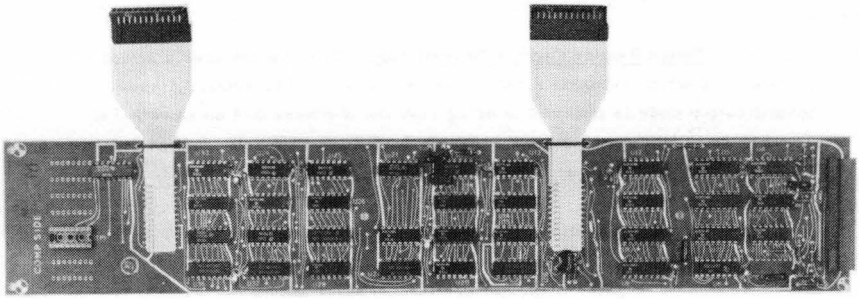
When a card is inserted, a hole punched in row 11, column 15, is detected by the circuitry, setting the card in flip-flop in the clock and control circuit. This also gates a special prefix character onto a serial data register. On the next keyboard load pulse that comes across the interface, the sequence control circuitry is advanced to position 2, while the data in the serial register is read out serially onto the data out bus under control of the keyboard clock signals. In position 2, the first data character is transferred from the matrix circuits to the serial register, and subsequently read out onto the data out bus. This process is continued, with one character readout following each keyboard load pulse until the fourteenth, or final, data character has been read out. No further transmission from the badge reader occurs until the card is removed. At this time a final character, representing card withdrawal, is sent at the next keyboard load pulse. The first and last character codes (prefix and withdrawal) are unique to the badge reader, and are utilized by the program. The data characters are identical to the keyboard characters 0-9, and are distinguishable only by their position immediately following the prefix code.

The keyboard is allowed system access any time the badge reader is not busy. This is accomplished via control of the keyboard load pulse. This pulse is inhibited from being sent to the keyboard by a gate while the badge reader is transmitting data. Without the keyboard load pulse, the keyboard will not send data back to the processor.

The badge reader includes its own 5 volt power supply. The keyboard attached to it also shares this 5 volt supply. Because of this supply, the badge reader may be positioned up to 200 feet from a monitor controller.

3.2.11 Card Reader Adapter Operation

The card reader adapter (Figure 3-43) is the PTS-100 interface, via the multiplex channel controller, for card reader models 3201 and 3202. The card reader is started and stopped by the adapter acting in response to orders and commands from the processor. The adapter reads Hollerith or binary data. The card reader and the adapter generate status and interrupts to the program. The adapter operates in the receive simplex mode only.



C73-566

Figure 3-43. Card Reader Adapter

3.2.11.1 Interfaces. The interface between card reader and adapter consists of a 12 bit data bus and seven status and command lines. The status lines (Ready, Busy, Hopper Check, Error, Motion Check, and Device Present) produce the status byte to the multiplexer. The command line is the pick command.

The signals between multiplexer and card reader adapter are described in Section 1 of this chapter.

3.2.11.2 Status and ICB. Status and the reasons for generating interrupts (ICB) are reported to the multiplexer over bits 0 through 5 of the data bus. All status conditions except bit 5, Data Overrun, originate in the card reader (Figure 3-44). Each status condition lights an associated indicator lamp on the card reader. After one of the status conditions stops the card reader and the condition is cleared the reset switch or the card reader must be activated to restart operation. The switch sets the ready flip-flop, which raises Device Ready to the adapter. ICB Bits 1 (BC = 0) and 2 ($\overline{\text{Ready}}$) are generated by the multiplexer. The adapter status and ICB bits are generated as follows:

Data Bus Bit	Status Bit Name	Status Bit Description
0	READY	This bit is lowered when any of the following conditions occur: device busy, hopper check, error, motion check, power disconnect. If the processor issues a new order before the reader has returned to a ready condition, the new order is not processed. An ICB is set and the order being processed is executed. The exception to this is the issuance of a Stop Reset, whereupon the present order is terminated, Busy is lowered after the card is stacked and the ready state is determined by the status conditions.

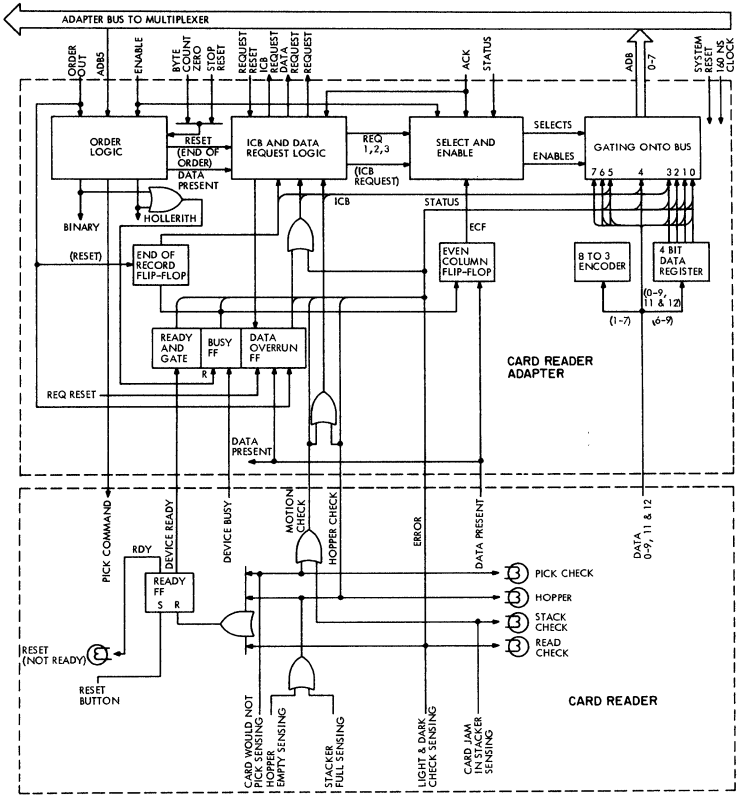


Figure 3-44. Card Reader Adapter, Block Diagram

Data Bus Bit	Status Bit Name	Status Bit Description
		Device Ready from the card reader is gated by the Busy flip-flop output. When Busy is not set, Ready is gated out to ABDO to the multiplexer.
1	BUSY	This bit is raised when a new order is received and it is lowered when the reader has stacked a card. When the card reader sends a Device Busy to the adapter, it sets the Busy flip-flop, which raised the Busy bit on ABD1. The flip-flop is cleared by Order Out. Busy is also used to clear the End of Record flip-flop and reset the ECF flip-flop.
2	HOPPER CHECK	If the card reader input hopper becomes empty or the output stacker becomes full of cards, the card reader HOPPER CHECK lamp will illuminate and a Hopper Check status signal will be sent to the adapter. The Hopper Check signal is put on ADB2 to the multiplexer. It is also ORed with Motion Check to generate an ICB interrupt and set the interrupt condition into ADB4.
3	ERROR	This bit is set on ADB3 when the card reader has a light or dark check failure. When this occurs the READ CHECK lamp illuminates on the card reader. This bit usually indicates that a card has a tear at the leading or trailing edge (dark check). If the card reader read station should experience an emitter sensor failure while reading a card, the light check will pick it up. This bit is also ORed with DOR to generate an ICB interrupt and set the interrupt condition into ADB5.
4	MOTION CHECK	This bit is raised when the card reader issues a Stack Check or a Pick Check. If the card being read does not stack fully, the Stack Check alarm is activated and the STACK CHECK lamp on the front panel illuminates. If the picker fails to engage a card, the reader logic will try to pick the card six more times. If the six attempts are unsuccessful, the PICK CHECK indicator illuminates. If either of these status conditions occurs, the motion check signal is sent to the adapter where it is put on ADB4. This signal is also used with Hopper Check to generate an interrupt.
5	DATA OVERRUN	This bit is set if the data sent by the card reader is not sensed by the processor before the holes in the card being read move beyond the sensing point. It is reset when a new order is received. The overrun condition is sensed in the adapter by the data overrun flip-flop. The D input is derived from REQ RESET, and the unit is clocked by a signal derived from the Data Present status from the card reader. Since REQ RESET occurs at the end of the transfer sequence between adapter and multiplexer, if it comes in while the Data Present status is active, an error condition results. The error is reported by sending the error overrun signal through ADB5 to the multiplexer. The overrun flip-flop is cleared by Order Out.

Data Bus Bit	ICB Bit Name	ICB Bit Description
3	EOR	This bit is raised when the adapter becomes not busy, which occurs when the cards are stacked and the reader can accept a new order. If the order has not been terminated, it will terminate at EOR. The Not Busy signal clocks the EOR flip-flop. EOR becomes one of the activating signals to the ICB. It is also gated onto ADB3.
4	HOPPER CHECK or MOTION CHECK (ATTENTION)	This bit is set by either Hopper Check or Motion Check.
5	ERROR	This bit is set by either Data Overrun or Error.

3.2.11.3 Circuit Description. The card reader and adapter are initialized by execution of the DIO Stop and Start instructions. The Stop instruction stops the reader, clears all pending or active requests for memory access, resets the ICB and any pending interrupts, and places the adapter in the ready and not busy state. The Start instruction transfers starting information and a Read Hollerith (00100) or Read Binary (00000) order to the multiplexer and adapter. The multiplexer samples the adapter status and when it senses that the card reader is ready and not busy it sends Order Out to the adapter and informs the adapter of the order (Read binary or Hollerith) by raising or lowering bit 5 on the adapter data bus (Figure 3-45). If bit 5 is high, it sets a binary flip-flop in the order logic circuits; if it is low, it sets a Hollerith flip-flop. The outputs of the two flip-flops are ORed and sent out as the Pick command to the card reader. (The Pick command is terminated when the byte count has reached zero (BCZ); the End of Record (EOR) condition has occurred; or a Stop Reset or System Reset is issued.) When the Pick command is raised, the card reader moves the first card from the input hopper to the read station where 80 twelve-row columns of punched data are read and put on the data bus to the adapter one column at a time.

When the card reader reads a card, it sends Data Present to the adapter for each column read. Data Present toggles the Even Column flip-flop and controls the request flip-flops in the ICB and Data Request Logic circuits, which send a REQUEST signal to the multiplexer. The multiplexer responds by sending the acknowledge signal (ACK) to the adapter. ACK is then gated with REQ3 from the request flip-flops and sent to the multiplexer as DATA REQ to signify that the request is for data service. The multiplexer responds by sending a REQ RESET signal to the request flip-flops. The flip-flops produce three request signals that control circuit operation and cause the select and enable circuit to produce select and enable signals to gate the data bytes onto the adapter data bus (ADB). There are three enable (G1 ENB, G2 ENB, and G3 ENB) and three select (G1 SEL, G2 SEL, and G3 SEL) signals, which

DATA						
HOLLERITH	BINARY			STATUS	ICB	AD B BIT NO.
12	12	6 DR	2	READY	—	0
11	11	7 DR	3	BUSY	BC = 0*	1
0	0	8 DR	4	HOPPER CHECK	READY*	2
8	1	9 DR	5	ERROR	EOR	3
9	2	12	6	MOTION CHECK	HOPPER CHECK MOTION CHECK	4
ENCODER 1	3	11	7	DATA OVERRUN	DATA OVERRUN ERROR	5
ENCODER 2	4	0	8	—	—	6
ENCODER 3	5	1	9	—	—	7
I	II	III	IV	V	VI	

EQUATIONS:

		SELECT		ENABLE	SOURCE
I	=	G1 SEL	+	G1 ENB	READ HOLLERITH
II	=			G1 ENB	READ BINARY + $\overline{ECF}$
III	=	G2 SEL	+	G2 ENB	READ BINARY + ECF + REQ 1
IV	=			G2 ENB	READ BINARY + ECF + $\overline{REQ\ 1}$
V	=	G3 SEL	+	G3 ENB	STATUS IN
VI	=			G3 ENB	ICB REQUEST

*PRODUCED BY THE MULTIPLEXER

Figure 3-45. Data Bus Bit Format

are primarily controlled by the order: even column flip-flop (ECF), request signals (REQ), status in, and ICB request. The primary source signals that produce the select and enable signals are shown in Figure 3-45 along with the select and enable signal gating for the ADB. The card reader data, status, and ICB bytes are gated onto ADB0-7 as shown in the equations.

When directed to read Hollerith data, the adapter automatically converts the 12 bit Hollerith character from each card column into 8 bit extended code bytes. Hollerith bits 1 through 7 are converted into three bits which are combined with Hollerith bits 8, 9, 0, 11, and 12 and sent to the multiplexer over ADB0-7.

When directed to read binary data, the adapter reads the data directly without altering the column contents. Since the adapter can handle only 8 bits at a time, the first odd column ($\overline{ECF}$) 12 bit character, bits 0 through 5, 11, and 12 is sent out on ADB0-7 while bits 6 through 9 are stored in the 4 bit Data Register (DR). Then during the next even column character the 4 bits from the Data Register are put on the data bus (ADB) and transferred to the multiplexer with bits 1, 0, 11, and 12 of the even column character. The rest of the even column character (bits 2 through 9) is transferred as the next 8 bit byte.

Timing for the adapter is derived from the 160 ns clock (MCLK) from the multiplexer.

3.2.11.4 Interrupts. The interrupt state is entered when any of the status bits (see table above) indicate an error condition. The status bits are ORed, when an error occurs the gate activates the ICB request, which is sent to multiplexer. The type of interrupt is indicated by the ICB byte.

3.2.12 Serial Adapter Operation

The serial adapter (Figure 3-46) is a PTS-100 interface, via the multiplexer channel, for simplex send and full duplex serial devices (TTY and TermiNet). The adapter executes orders received through the multiplexer, and provides status and interrupt information to the multiplexer. In the receive mode it converts serial data from the device to parallel data which it sends to the multiplexer. In the transmit mode it converts parallel data from the multiplexer to serial data and sends it to the device. When used in full duplex the data formats must be the same in both transmit and receive modes. Different baud rates (95 to 1200), number of stop bits (1 or 2), and type of operation (simplex-duplex) are selectable by patch plugs.

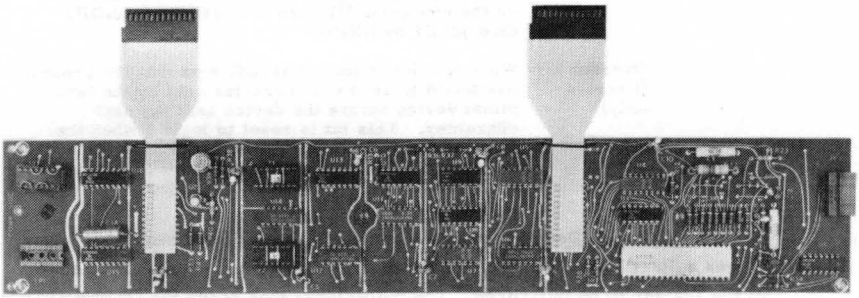


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Figure 3-46. Serial Adapter

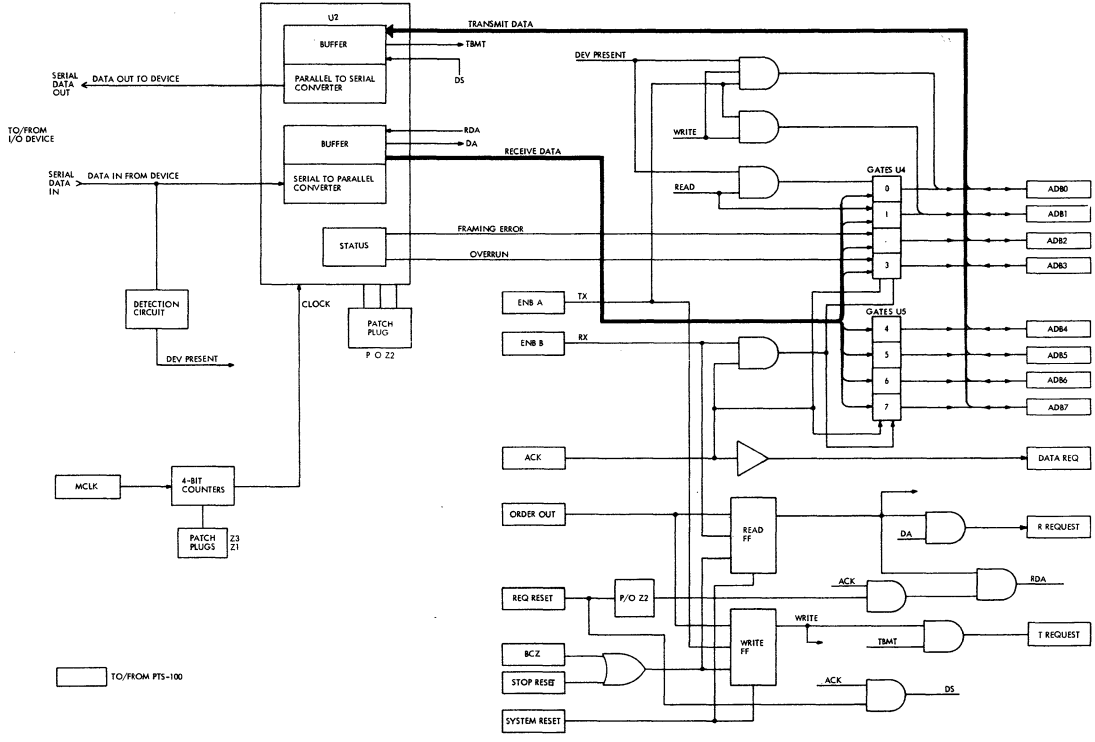


Figure 3-47. Serial Adapter, Simplified Circuit Diagram

the enable pulses (ENB) from the multiplexer. See Figures 3-47 and 3-48. The multiplexer sends only one ENB to the adapter. It is distributed by screw switches on the motherboard to the ENBA (transmit) or ENBB (receive) lines. If the adapter is to operate in the receive mode, ENBB clocks the read flip-flop, and if it is to operate in the transmit mode, ENBA clocks the write flip-flop; if the adapter operates full duplex, the enable commands clock both flip-flops. In this case the PTS software controls the operating mode. After the flip-flops have been clocked, the outputs (and the ENB signal) set the ready and busy bits as previously described.

The flip-flops remain latched until they are reset by SYSTEM RESET, STOP RESET, or BCZ. In the meantime the adapter is in a waiting state until data transmission begins.

The DEV PRESENT signal is produced by a detector circuit attached to the adapter/device interface line. It senses the current in the receive line and indicates that an output device is attached to the adapter and is working. Some older devices do not have the device present circuit; in these cases the adapter circuit is strapped to a true voltage level. New devices having this circuit can be identified as follows: TTYs will have model number 33XX, where X is any number. On TermiNets the DAT card at the rear of the unit will be stamped DATI Group II.

a. Timing Circuit

Adapter timing is generated by counting down the MCLK (160 ns) from the multiplexer in three 4 bit counters (Figure 3-48). The frequency of the resulting clock is determined by the preset count on patch plugs Z1 and Z3. The clock is applied to converter U2 where it times the data transfer operations.

b. Receive Circuit Operation

When the terminal device is ready to send data it sends the first character to converter U2 where it is clocked into a serial-to-parallel converter buffer. This causes the buffer to raise Data Available (DA) which is ANDed with READ from the read flip-flop to produce the R REQUEST to the multiplexer. (The read flip-flop was previously set by ORDER OUT and ENBB.) The multiplexer responds with ACK which is sent back to the multiplexer as DATA REQ to signify that the request is for data service. Then the multiplexer responds to DATA REQ with REQ RESET.

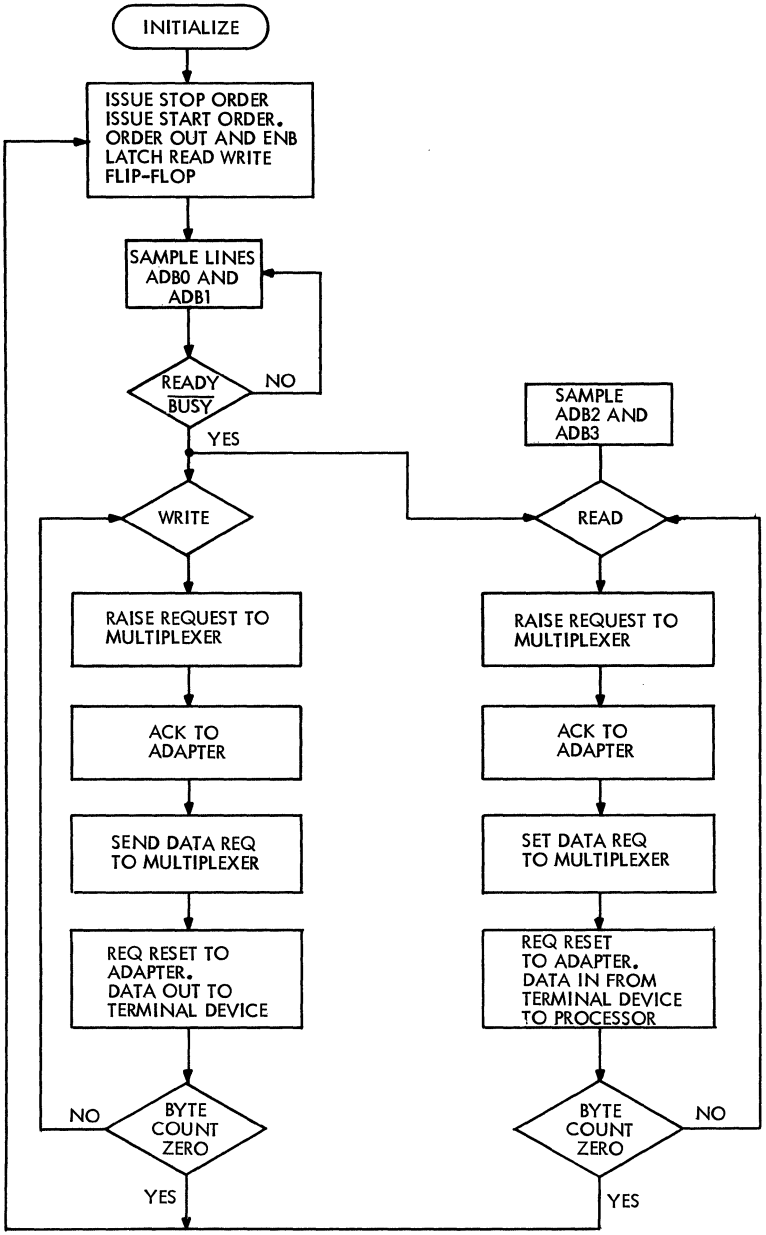


Figure 3-48. Serial Adapter, Functional Flow Diagram

ACK and READ are combined with REQ RESET to produce Reset Data Available (RDA), which gates the character from the buffer to gates U4 and U5, where ACK gates it onto the data bus (ADB). The data transfers continue with the R REQUEST-ACK-DATA REQ - REQ RESET cycle repeated for each character transferred until the read flip-flop is reset by byte-count-zero (BCZ) or a stop or system reset is received from the multiplexer. The start and stop bits are stripped off the characters in converter U2 before they are gated to the multiplexer.

c. Transmit Circuit Operation

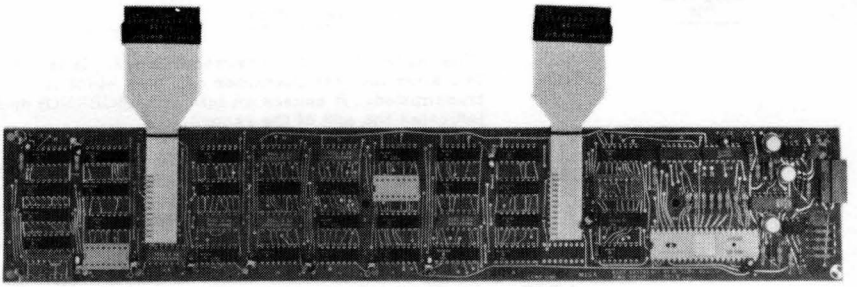
When the program is ready to transmit to the terminal device, it sends ORDER OUT and ENB A to the adapter to set the write flip-flop. The flip-flop WRITE output is ANDed with TBMT (Transmit Buffer Empty - when the buffer is empty) and sent to the multiplexer as T REQUEST. The multiplexer responds with ACK, which, as before, is sent to the multiplexer as DATA REQ to signify that the request is for data service. The multiplexer then responds by putting data on the ADB bus and sending REQ RESET. REQ RESET is ANDed with ACK to produce Data Strobe (DS). DS gates the data character from the data bus, now in the transmit buffer, into the transmit parallel-to-serial converter where it is shifted out to the terminal device by the clock. Data transfers continue with the T REQUEST-ACK -DATA REQ-REQ RESET cycle repeated for each character transferred until the Write flip-flop is reset by Byte Count Zero (BCZ), System Reset, or Stop Reset. Start and stop bits are added to the characters in converter U2 before they are sent to the I/O device.

When the adapter is operated in the simplex transmit mode, a patch (Z2) is removed at installation that opens the REQ RESET line to the receive circuits.

3.2.13 Multiple Interface Serial Adapter Operation

The multiple interface serial adapter (MISA) is a PTS-100 interface, via the multiplexer channel, for 50 to 4800 baud serial devices. The MISA (Figure 3-49) executes orders received via the multiplexer and provides status and interrupt information to the multiplexer. In the receive mode it converts serial data to parallel data. In the send mode it converts parallel data to serial data. Serial data characters transferred between adapter and device are formatted with start and stop bits. Different baud rates, stop bit (1 or 2), and parity (odd, even or none) formats are selectable by patch plugs.

3.2.13.1 Interfaces. The MISA interfaces with devices using either RS232 (asynchronous) or current loop (with or without demand control).



C74-1316

Figure 3-49. Multiple Interface Serial Adapter

The adapter is modified to accommodate either interface by strap connections on patch plug B2. (For patching information refer to Chapter 2.)

The control and data signals between the multiplexer channel and adapter are described in Section 1 of this Chapter.

3.2.13.2 Status and ICB. Status and the reasons for generating interrupts are reported to the multiplexer over bits 0 through 5 of the data bus. Bits 0 through 2 represent normal status conditions and bits 3 through 5 represent interrupt conditions. The multiplex channel controller sets six ICB bits for this adapter: Search Hit (bit 0); BC = 0 (bit 1); Start Issued While Busy (bit 2); EOR, TX (bit 3); Malfunction (bit 4); and ERROR, TX (bit 5). Bits 0, 1, and 2 are generated by the multiplexer. See Figure 3-50. The status bits are generated as follows:

Data Bus Bit	Name	Description
0	Ready	The adapter raises this bit (1) when it and the I/O device are ready to process a message. It is set to 1 during a read order when there is no parity or framing error ($\overline{PE + FE}$) and DATA REQ is sent to the multiplexer. It is set to 0 before the order is issued when the I/O device is not present or not operating ($\overline{DEV\ PRESENT}$).
1	Busy	This bit is set to 1 by ORDER. It indicates that the adapter is actively transferring a message. During this time the adapter does not accept a new ORDER OUT.
2	Demand Present	This bit is only used in transmit mode. It indicates the status of the DEMAND line to the I/O device. When the I/O device is ready to receive data it is raised (1).

Data Bus Bit	Name	Description
3	EOR* (ICB)	This bit is only used in transmit mode. It is set to 1 after the last character of a data block is transmitted. It causes an interrupt (ICBREQ) and indicates the end of the record.
4	MALF (ICB)	This bit is set (1) when the I/O device is not operating or present. The condition must exist for at least 16 to 32 bits before the adapter will indicate the malfunction. The setting of this bit causes an interrupt (ICBREQ).
5	Demand* and EOR (ICB)	This bit is only used in transmit mode. When set (1), it indicates that a parity error occurred in the data block just transmitted. It is an interrupt condition (ICBREQ) and it is set by EOR when a DEMAND still exists from the I/O device.

3.2.13.3 Circuit Description. The adapter is initialized when the program issues a Start I/O order to the multiplexer. The start order contains the address of the adapter to be initialized. It causes the multiplexer to fetch and send to the adapter the order to be performed. The order is either a read or a write. The multiplexer informs the MISA of the order over bit 7 of the adapter data bus (ADB). See Figure 3-50.

When bit 7 is a 1, it is a write order, and when bit 7 is a 0 it is a read order. ADB7 and $\overline{\text{ADB7}}$ are applied to gates that control the read and write flip-flops. Following the start command the multiplexer issues ORDER OUT which enables both gates. If the order is a read order the read flip-flop is set. If it is a write order the write flip-flop is set. The flip-flops are clocked by the ENB (enable) signal from the multiplexer. The set flip-flop will remain set awaiting a data or ICB transfer, until BCZ (byte-count-zero) or until a STOP RESET, SYSTEM RESET, or interrupt clears it. While in the waiting state, the I/O device loop current activates the device present circuit which produces the DEV PRESENT signal that is inverted and applied to ADB0 through output selector gate D4. Therefore, when the device is ready to process data, ADB0 is a logic 1.

Also in the waiting state, when the order is issued the MALF flip-flop is set if the I/O device is not present. The resulting MALF ICB produces a REQUEST to the multiplexer and with $\overline{\text{DATA REQ}}$ produces ICB REQ to the multiplexer when ACK occurs. If the I/O device is present and operating MALF is not set and REQUEST is generated by $\overline{\text{DATA REQ}}$. The multiplexer response to REQUEST is ACK. When the adapter is ready for a data transfer operation the data request flip-flop is set and ACK gates DATA REQ out to the multiplexer.

*Options

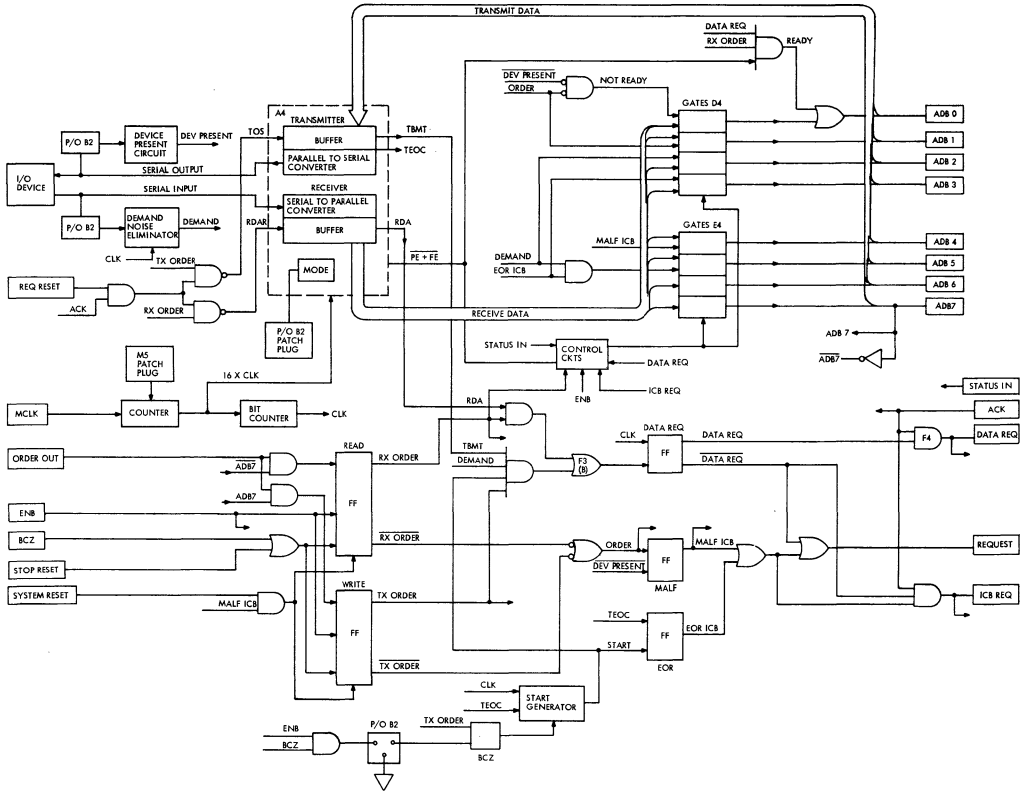


Figure 3-50. MISA Simplified Circuit Diagram

a. Timing

The MCLK is used to synchronize the adapter to the PTS system clock. It clocks a countdown circuit that is controlled (preset) by patch plug M5, which is strapped for the different baud rates. The patch plug connections are shown in Chapter 2.

The output of the countdown circuit (16X) clocks converter A4 and drives a bit counter. The timing outputs of the bit counter clock the other adapter circuits.

b. Receive Circuit Operation

When data has entered the serial-to-parallel converter in A4 and has been shifted to the buffer, the Receive Data Available (RDA) signal is raised. It is gated by the RX ORDER from the read flip-flop and it sets the data request flip-flop. The ACK signal, which was the multiplexer's response to the previous request, gates DATA REQ to the multiplexer. This instructs the multiplexer that the service requested is for data, not an interrupt. The multiplexer now replies with REQ RESET. REQ RESET with ACK and the RX ORDER produce Reset Data Available Receive (RDAR), which gates the data character out of the buffer onto the data bus and resets RDA. Selector gates D4 and E4 gate the data out onto the adapter data bus (ADB). Gating is performed by the control circuits during ENB, DATA REQ, RX ORDER, no parity or framing error, $(\overline{PE + FE})$, no STATUS IN and no ICB REQ. When RDA is lowered it resets the Data Request flip-flop, which lowers DATA REQ. Then when the receive buffer again contains a character of data RDA sets the flip-flop and sends DATA REQ to the multiplexer, which once more responds with REQ RESET to gate the character onto the data bus. The process continues until the multiplexer sends byte-count-zero (BCZ) and resets the read flip-flop to terminate the order. Start and stop bits are stripped off the characters in converter A4 before they are sent to the multiplexer.

c. Transmit Circuit Operation

In the transmit mode the write flip-flop is set when ADB7 is a logic 1 and ORDER OUT is present. As in the receive mode REQUEST and DATA REQ are sent to the multiplexer. However, in the transmit mode the data request flip-flop is set by TX ORDER, DEMAND, TBMT and START. TX ORDER is raised when the write flip-flop is set. DEMAND is high (when patched for TTY or TermiNet and for certain conditions of operation of the ticket printer) when the I/O device wants service. TBMT (transmit buffer empty) is high when the transmit buffer of the converter A4 is empty. START is high during the data transfer. The multiplexer responds to DATA REQ by placing a data character on the adapter data bus and sending REQ RESET

to the adapter. REQ RESET and TX ORDER are ANDed to produce the transmit data strobe (TDS). TDS gates the character out of the transmit buffer into the serial-to-parallel converter where it is clocked out to the I/O device. Start and stop bits are added to the character in converter A4 before it is sent to the I/O device. When the transmit buffer is full TBMT resets the data request flip-flop and lowers DATA REQ, whereupon the multiplexer sends another character over the data bus into the transmit buffer. This character is sent to the I/O device as before. Character transfers continue until the multiplexer sends Byte Count Zero (BCZ); then the write flip-flop is reset and the order is terminated.

The start generator gates each transmit character transfer by controlling the data request flip-flop. It also controls the end of record (EOR) flip-flop, which is set after each record has been transferred to the I/O device, provided the BCZ flip-flop is enabled by patch B2. The Transmit End of Character (TEOC) starts the start generator, which initiates START. The clock (CLK) terminates START at the end of each character transfer. However, after the last character in the data block is transferred, TEOC initiates START and remains high. Then when START is terminated by the clock (BCZ flip-flop enabled) the EOR flip-flop is set. When the BCZ flip-flop is disabled by the patch the EOR flip-flop is not set after the last character. When set, EOR ICB generates ICB REQ, sets bit ADB3 and if DEMAND is high, sets bit ADB5. DEMAND is only high after a block of data has been transferred and the data block had a parity error.

3.2.14 Modem Adapter 2331 Operation

Modem adapter model 2331 (IPARS) is the PTS-100 interface to a commercial modem for serial data interchange via common carrier or privately owned communication facilities. The modem adapter (Figure 3-51) is for use with a 6 level character code, two-sync-character pattern recognition, and error detection by 6 bit CRC characters. It is synchronous, full duplex, and operates up to 9600 baud. Parity checking is not implemented. The adapter operation, except for sync character detection, is unaffected by the composition of the data being sent or received. (Refer to Chapter 2 for patch plug options.) There are two versions of this adapter: the old, 591556, and the new, 860820 (also called modem adapter B). They are both the same except for layout and patches.

3.2.14.1 Interfaces. The interface lines between the adapter and the multiplexer are described in Section 1 of this chapter. The function of the interface lines between the adapter and the modem are listed below and further defined in Appendix C.

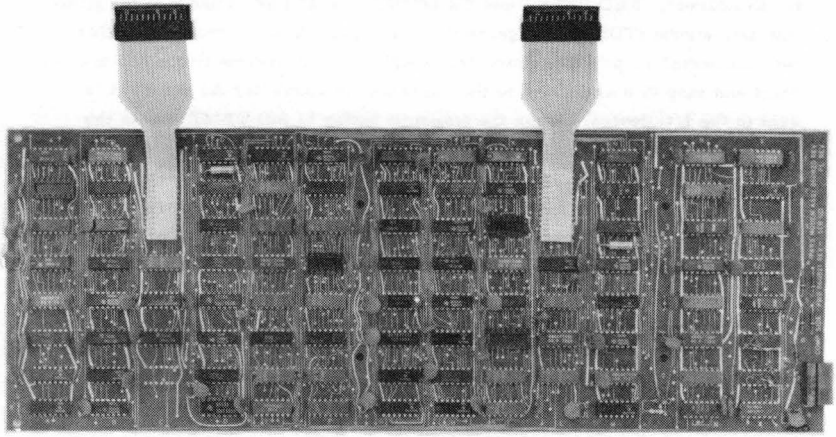


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Figure 3-51. Modem Adapter 860820

Signal	Function
RDATA	Serial Receive Data from the modem to the adapter (±3 v to ±25 v).
CARRIER	A positive voltage from the modem to the adapter when a carrier is received by the modem from the distant modem (> +3 v).
SCR	Serial Clock Receive. A clock from the modem to the adapter to clock its receive circuits (±3 v to ±25 v).
NEW SYNC	A sync signal from the adapter to the modem to synchronize the modem. A positive pulse at the end of the message quenches the existing sync signal (> +3 v).
TDATA	Serial data from the adapter to the modem (±3 v to ±25 v).
RTS	Request to send. A positive voltage sent to the modem when the processor has a message to send. It is held positive during transmission (> +3 v).
CTS	Clear to send. Raised in response to RTS when the modem is ready to accept transmission (> +3 v).
DSETREADY	Data Set Ready. Indicates that the modem is ready to operate. A positive voltage exists at all times when the modem is prepared to send or receive data (> +3 v).
SCT	Serial Clock Transmit. A clock from the modem to the adapter to clock its transmit circuits (±3 v to ±25 v).

3.2.14.2 Status and ICB. Status and interrupt condition bits are reported to the multiplexer on bits 0 through 6 of the data bus (ADB). Bits 0, 1, 3, and 4 are used to report receive status conditions and bits 0, 1, and 5 are used to report transmit status conditions. The interrupt condition bits (ICB) are described later in this section. Figures 3-52 (Receive) and 3-53 (Transmit) are simplified diagrams of the interrupt and status circuits. The status bits are generated as follows:

Receive Status Word

Data Bus Bit	Name	Description
0	Ready	When this bit is 0, it indicates that the modem is not connected or has power off. It is also 0 when the adapter is busy or when the modem has not set data set ready. This bit is controlled by the flip-flop which is set by ANDing DSETREADY with CARRIER and the reset output of the busy flip-flop. DSETREADY and CARRIER are high when the modem is ready, and the reset output of the busy flip-flop is high whenever the adapter is not busy.
1	Busy	This bit is controlled by the busy flip-flop. It is 1 when the adapter is in the look-for-sync state or is actively transferring a message from the modem to the multiplexer. During this time the adapter will not accept a new ORDER OUT without causing an error.
3	CRC Error	When this bit is 1, it indicates that a CRC error has been detected at the end of the message just received. The bit is reset when the status word is read into the multiplexer or when a new look-for-sync order is issued.
4	Data Rate Error	When this bit is 1 it indicates that the multiplexer was unable to accept an assembled character before the first bit of the next character was received over the data line from the modem. As a result, one or more of the bits from the character being assembled was lost. The bit is set by receive state count 101.

Transmit Status Word

0	Ready	When this bit is 0, it indicates that the modem is not connected or has power off. It is also 0 when the adapter is busy or when the modem has not set data set ready. This bit is controlled by the ready flip-flop, which is set by ANDing DSETREADY and the reset output of the busy flip-flop. DSETREADY is high when the modem is ready to send, and the reset output of the busy flip-flop is high when the adapter is not busy.
1	Busy	When this bit is 1, it indicates that the adapter is actively transmitting a message to the modem. During this time the adapter will not accept a new ORDEROUT without causing an error. The busy flip-flop is set by ORDEROUT when the start transmit order is issued and a transmit order other than transmit idles (TSTRTIDLE) is decoded.

Data Bus Bit	Name	Description
5	Idles	When this bit is 1, it indicates that the adapter is transmitting idle characters (continuous 1's) to the modem. IDLES is generated by the idles flip-flop under control of the Transmit Idles order (TSTRTIDLE). During the idles state, the busy flip-flop is reset, the busy bit on the data bus is 0, the ready flip-flop is set and the ready bit on the data bus is 1.

3.2.14.3 Receive Circuit Description (Figure 3-52).

a. Timing

MCLK and SCR are used by the timing circuits to produce timing signals synchronized to both the PTS-100 and the modem. The timing circuits clock the adapter circuits and also drive a state counter, which is stepped through various states that control the phases of operation of the adapter receive circuits.

b. Data Transfer

Serial data from the modem is loaded into a serial-to-parallel converter and transferred to the multiplexer over data bus (ADB) lines 2 through 7. The adapter transfers the data to the multiplex channel controller under control of the program which directs the adapter by sending orders on the data bus bits ADB 5, 6, and 7. Adapter status and interrupt conditions are reported to the program via the multiplexer on data bus bits 3 through 6.

c. Initializing

The adapter is initialized when STOP RESET is sent by the multiplexer. When ANDed with RENB, it resets the check flag, request busy, state counter, interrupt, and status flip-flops. When the busy flip-flop is cleared, ADB1 is low indicating to the processor that the adapter is not busy. When the modem is not ready, the ready flip-flop is reset and ADB0 is low indicating to the multiplexer that the adapter is not ready to process a message. The multiplexer continues to monitor ADB0 and ADB1 while the adapter is in the waiting state.

d. Start Receive Order

When the modem is ready it raises the CARRIER and DSETREADY lines. $\overline{\text{RBUSY}}$ is now ANDed with CARRIER and DSETREADY to set the ready flip-flop. READY is gated out to ADB0, through patch plug E5. The program responds to ready by sending the start receive order on the data bus. When

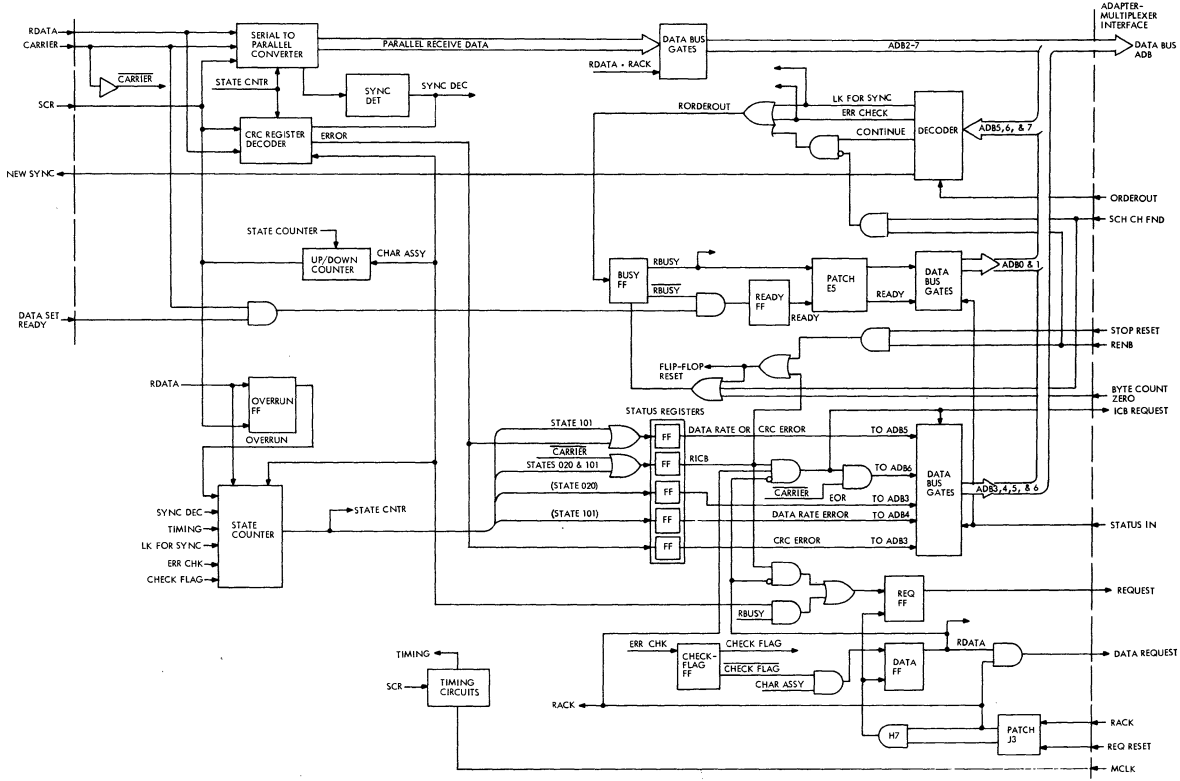

Figure 3-52. Modem Adapter Model 2331, Receive Circuits, Simplified Diagram

the multiplexer detects the ready signal, it also sends ORDER OUT which gates the start receive order through the decoder. The decoder converts the start receive order into a look for sync (LKFORSYNC) signal. This signal initiates the receive state counter, resets the receive status registers, and becomes RORDEROUT. RORDEROUT sets the busy flip-flop. BUSY, now high, is sent out through patch plug E5 to ADB1 to indicate to the multiplexer that the adapter is busy and cannot accept additional orders until the present sequence has been completed.

Serial sync characters from the modem are clocked by SCR and gated into the serial-to-parallel converter by CARRIER. The sync characters are applied to the sync detector circuit, which advances the state counter and resets the CRC register with CHARASSEM when the two sync characters are detected. The modem follows the sync character with data characters, which are clocked into the serial-to-parallel converter. Each data character is gated directly onto data bus lines ADB2-ADB7 by RDATA and RACK. The up/down counter keeps track of the data characters being clocked in by counting SCR. After each character is loaded it produces CHAR ASSEM to generate REQUEST and advance the state counter, which clears the serial-to-parallel converter for the next character. CHAR ASSEM with RBUSY sets the REQuest flip-flop, which raises REQUEST to the multiplexer to inform it that the adapter desires service. The multiplexer responds by sending Acknowledge (RACK) which is ANDed with RDATA and sent back to the multiplexer as DATA REQ to indicate that the request is for data service, not interrupt service. RACK and RDATA gate the assembled character in the serial-to-parallel converter out to the multiplexer. In response to the DATA REQ signal the multiplexer sends REQ RESET, which is ANDed with RAK, to reset the REQuest and DATA flip-flops. When the next character is received CHAR ASSEM again initiates the REQUEST-RACK-DATA-REQUEST RESET cycle and transfers this character to the multiplexer as before. This process continues until the program sends Byte Count Zero or Search Character Found (SCH CH FND), whereupon the adapter circuits are reset.

e. The Continue Receive Order

All orders for the modem adapter use the chaining option. Chaining assures continued character processing to the end of the message. During a start receive order when the PIOT byte count goes to zero, BCZ (byte count zero) clears the busy flip-flop, preparing the adapter for another processing sequence, then a continue receive order is sent to the adapter. Just as with start receive, continue receive is decoded and produces RORDEROUT, except that RLKFORSYNC is not produced and RORDEROUT is disabled by SCH CH FND when an end of message character is detected.

f. The Check CRC Order

The Check CRC order is issued when an EOM character is detected. It directs the adapter to compare the next assembled character, assumed to be the message's CRC character, with the CRC character developed by the adapter as the message is received. This order advances the state counter to 020 which clears the serial to parallel converter and sets the EOR bit on ADB3. The check CRC order is decoded and it produces ERRCHK and RORDEROUT. ERRCHK sets the check flag flip-flop and advances the state counter. In the set state the check flag flip-flop disables the data flip-flop. This inhibits the data bus gates and the next input character is fed to the 6 bit CRC register decoder. Here the CRC character is compared to the computed CRC. When no difference is detected, the message is valid, the EOR interrupt is set, and the adapter enters a look-for-sync state. When sync is detected another start receive order will be issued to transfer the next message. If a CRC error is detected the CRC decoder sets the data rate or CRC error and CRC error flip-flops. This sets interrupt bits 3 and 5. When ERRCHK disabled the data flip-flop, REQUEST was raised to the multiplexer, which responded with RACK. $\overline{\text{RDATA}}$ ANDed with RACK, and RICB next produces ICB REQUEST indicating to the multiplexer that interrupt service, not data service, is desired.

g. The Send New Sync Order

Sequential messages received by the modem may have different bit synchronizations. When this condition occurs, a Send New Sync order is issued by the program. When the order is decoded it is sent directly out of the decoder to the modem as New Sync.

h. Receive Interrupts

There are four receive interrupt conditions: loss of carrier, CRC error, data rate error (failure of multiplexer to accept the assembled character); and EOR (end of record). The ICB request gates the interrupt bits onto the data bus. The ICB request is produced by $\overline{\text{RDATA}}$ and RACK when states 101 or 020 occur or when there is no carrier ($\overline{\text{CARRIER}}$). When there is no RDATA, RICB raises the REQUEST line to the multiplexer.

There are two bit 3 interrupts, which may occur simultaneously. One is EOR, which signifies that the message is complete and the CRC has been checked, whereupon the adapter is ready to process a new message. The EOR flip-flop is set by state 020 at the end of the state counter sequence. State 020 is generated by ERR CHK, which occurs when the adapter receives the check CRC order. The other bit 3 interrupt condition is the CRC error. It is initiated by a CRC error detector in the CRC register and decoder circuit. It occurs when a CRC error occurs.

The bit 4 interrupt is the data rate error. It originates from the overrun flip-flop whose inputs, RDATA and SCR, set the flip-flop and flag a data overrun condition if a data character is not transferred during the SCR pulse. The adapter and multiplexer transfer a data character between the beginning of REQUEST and the beginning of REQ RESET. If RDATA is still high when SCR changes, the next character has been introduced before the last one was transferred, in which case the overrun flip-flop is set and it in turn sets state 101, which produces the data rate error to ADB4.

The bit 5 interrupt signifies that either a CRC error or an overrun condition (state 101) has occurred. The CRC register sets the data rate or CRC error flip-flop when a CRC error occurs. State 101, which also sets the flip-flop, is entered in an overrun condition, or when the check CRC order (ERR CHK) is issued. To determine which error has occurred, the multiplexer examines the other bits on the data bus.

3.2.14.4 Transmit Circuit Description (Figure 3-53).

a. Timing

MCLK and SCT are used by the timing circuits to produce timing signals synchronized to both the PTS-100 and the modem. The timing circuits clock the adapter circuits and also drive a state counter, which is stepped through various states that control the phases of operation of the adapter transmit circuits.

b. Data Transfer

Parallel data from the multiplex channel controller (data bus ADB 2-7) is loaded into a parallel-to-serial converter where it is transferred serially to the modem. Data transfers are under control of the program which directs the adapter by sending orders on data bus bits ADB 4 through 7. The data may be transferred with or without CRC characters. Adapter status and interrupt conditions are reported to the program via the multiplexer on data bus bits ADB 0, 1, 3, and 5.

c. Initialization

The adapter is initialized when STOP RESET is sent by the multiplexer. When ANDed with TENB, it resets the state counter and the request and busy flip-flops. When the modem is ready to receive it raises DSETREADY, which

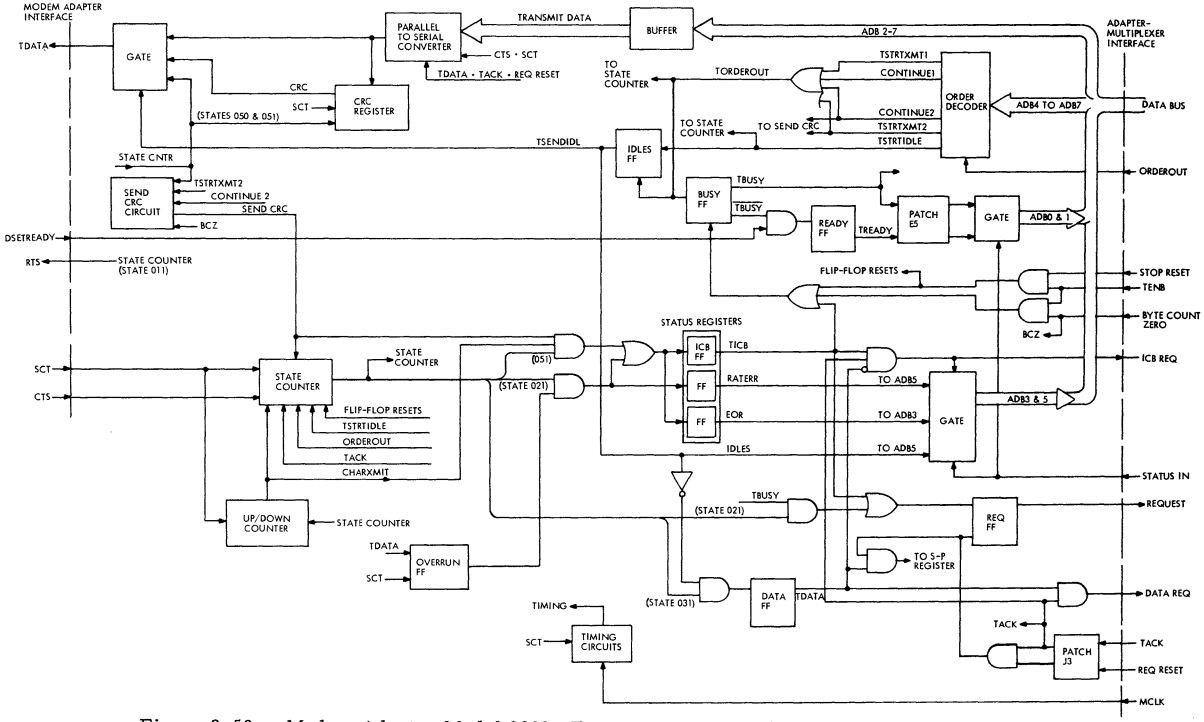

Figure 3-53. Modem Adapter Model 2331, Transmit Circuits, Simplified Diagram

with $\overline{\text{TBUSY}}$ sets the ready flip-flop. TREADY is then gated onto ADB0 indicating to the multiplexer that the adapter and modem are ready to begin data transmission.

d. Start Transmit Without CRC

This order is issued to the adapter when the program wants to transfer the initial buffer of a multibuffer message. It is decoded (TSTRTXMT1) in the decoder and ORed to produce TORDEROUT, which sets the busy flip-flop. TBUSY, now high, is applied through patch plug E5 to ADB0 to indicate to the multiplexer that the adapter is busy.

TORDEROUT also advances the state counter to state 011, which is sent to the modem as RTS (request to send). If the modem is ready to begin data transfer, it replies with CTS (clear to send). CTS advances the state counter to state 021. State 021 and TBUSY set the request (REQ) flip-flop that sends REQUEST to the multiplexer, which responds with TACK. TACK advances the state counter to state 031, which sets the data flip-flop. Then TDATA and TACK raise DATA REQ to the multiplexer, signifying that data service is requested. The multiplexer replies with REQ RESET and puts the first sync character on the data bus.

REQ RESET, SCT, CTS, TDATA, TACK, and MCLK clock the sync character into the parallel-to-serial converter. Then the state counter gates the character out serially to the modem. The next sync character is sent in the same way followed by byte count zero. The processor then sends another start transmit command followed by the data to be transmitted. If the entire message is in one buffer a start transmit with CRC will follow; if not, a start transmit without CRC will be sent followed by continue send command(s) until byte count zero. The last continue Send will be with CRC.

e. Start Transmit with CRC

This order is issued to the adapter when the program wants to transfer one buffer of data. It is decoded as TSTRTXMT2 and causes the same sequence of events as TSTRTXMT1 except that it also sets the send CRC circuit. The send CRC circuit produces SEND CRC at byte count zero, which advances the state counter to state 051. State 051 enables the CRC register output circuits. During the time when data characters are being sent to the modem, the serial output of the parallel-to-serial converter is also being clocked into the CRC shift register. When state 051 becomes active, it gates the previously calculated CRC character out to the modem serial data line. State 051 also generates

an ICB request and an EOR interrupt when the up/down counter produces CHARXMIT. The up/down counter keeps track of the characters being clocked out of the modem by the counting SCT. After each character is sent out it produces CHARXMIT, which resets the state counter and after the CRC produces EOR.

f. The Continue Send Orders

These commands are issued to the adapter to continue transmitting data from new buffers. There are two types of Continue Send orders, one that causes a CRC to be sent after the data buffer is sent, and one that does not cause the CRC character to be sent. The order without CRC is issued when the data buffer is not the final buffer to be transmitted, or is the final buffer in a message not requiring a CRC character. The Continue order with CRC is used to send the final buffer.

The Continue Send orders are decoded to TCONTINUE1 and TCONTINUE2. TCONTINUE1 causes the same sequence of events as TSTRTXMT1, and TCONTINUE2 causes the same sequence of events as TSTRTXMT2. The difference is that the state counter state 011 is not entered because the RTS line to the modem does not need to be raised.

g. The Transmit Idles Order

The multiplexer may respond to an EOR interrupt by sending a stop command, by initiating another message, or by sending a transmit idles order. Assuming the latter, the transmit idles order is decoded and the resulting TSTRTIDLE is applied to the Idles flip-flop. TSENDIDL from the Idles flip-flop inhibits the data flip-flop, is put on ADB5, is sent to the state counter, and is sent directly over the serial data line to the modem. Being a series of 1's, it maintains synchronization with the modem while waiting for further data transmission. TSTRTIDLE also initiates state counter state 031. This state disables the up/down counter and CRC register to prevent the generation of the CRC character while idle characters are being sent. It also is inhibited from setting the data flip-flop by TSENDIDL during this time.

h. Transmit Interrupts

There are two transmit interrupt conditions: device end of record (EOR) and data rate error (RATERR). The ICB REQuest gates the interrupt bits onto the data bus. ICB REQ is produced by $\overline{\text{TDATA}}$ and TACK when the ICB flip-flop is set (TICB).

The ICB flip-flop is set by any of the interrupt conditions. Its output also sets the request flip-flop, which raises the REQUEST line to the multiplexer.

The bit 3 interrupt is set when the entire message including the CRC character has been transmitted or when a data rate error occurs. It is normally set during state 051 by CHARXMIT from the up/down counter and SEND CRC from the send CRC circuit after the complete message and associated CRC character have been sent. Bits 3 and 5 are set in state 021 when an overrun condition occurs. This indicates that the next data character was not received in time to prevent a gap in the outgoing data. OVERRUN is produced by the overrun flip-flop when SCT occurs before the data flip-flop (TDATA) is set. When an interrupt occurs the multiplexer determines whether the interrupt is a data rate error or an end of record by monitoring both ADB bits 3 and 5.

3.2.15 Modem Adapters 2332, 2333, 2334 Operation

Modem adapters models 2332 (CTMC), 2333 (2848), and 2334 (3270) (Figure 3-54) are the PTS-100 interface to commercial modems for serial data interchange via common carrier or privately owned communications facilities. The modem adapters are either full or half duplex synchronous with modem supplied clocks and data rates to 9600 baud. Adapter 2332 processes 8-level characters, 8 bits with or without parity, with two-sync-character pattern recognition. Error detection is by VRC and LRC checking. Adapter 2333 processes 10-level characters (start bit, 7 data bits, parity bit, stop bit). Error detection is by VRC parity per character and LRC checking per block. Adapter operation for both, except for the character synchronizing capability, is unaffected by composition of the character code being sent or received. (Refer to Chapter 2 for the patching options.)

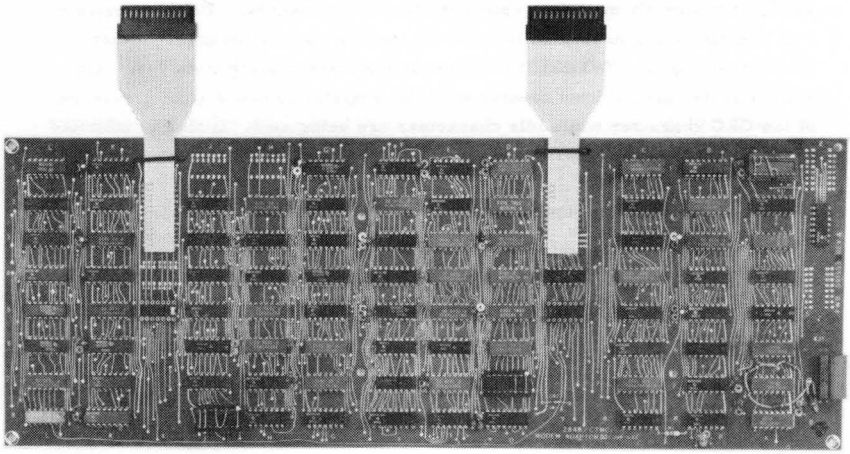

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Figure 3-54. Modem Adapters 2332, 2333, and 2334

3.2.15.1 Interfaces. Refer to Section 3.2.14.1 and Appendix C.

3.2.15.2 Status and ICB. Status and interrupt condition bits are reported to the multiplexer on bits 0 through 6 of the data bus (ADB). Bits 0, 1, 2, and 4 are used to report receive status conditions and bits 0, 1, and 5 are used to report transmit status conditions. The interrupt condition bits (ICB) are described later in this section. Figures 3-55 (Receive) and 3-56 (Transmit) are simplified diagrams of the interrupt and status circuits. The status bits are generated as follows:

Receive Status Word

Signal		Function
0, 1, & 4		Refer to Section 3.2.14.2 for a description of these bits.
2	Parity Error	When this bit is a 1 it indicates that a parity error has been detected on the character being received. The PARERROR flip-flop is set during state 140 by PARITY ERROR from the parity detector circuit.

Transmit Status Word

Signal	Function
0, 1, & 5	Refer to Section 3.2.14.2 for a description of these bits. The only difference between that adapter and this adapter is that in this adapter the busy flip-flop is set directly by the decoded start transmit command (TSTRTXMIT).

3.2.15.3 Receive Circuit Description. The receive circuit operation (Figure 3-55) is basically the same as that for the receive circuits in the modem adapter model 2331 (refer to Section 3.2.14.3) except for the following:

1. The cyclic redundancy check (CRC) circuits and associated CRC orders are not used.

2. A new Stop Data order is employed.

3. Parity and start bit detectors are used. The parity detector Parity Error output sets a bit in the status word.

4. Additional patch plugs are installed (refer to Chapter 2) for options.

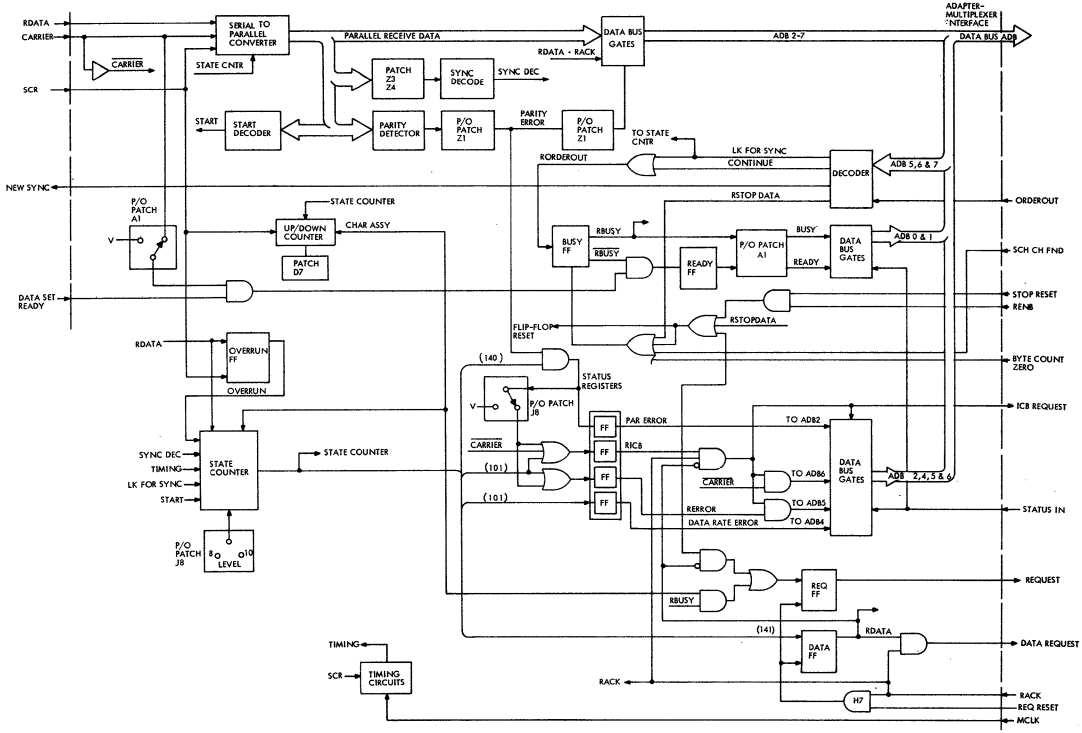


Figure 3-55. Modem Adapter 2332, 2333, 2334 Receive Circuits, Simplified Diagram

a. Initialization

Initialization is basically the same as that described in Section 3.2.14.3, except that parity is used and model 2333 does not use sync characters but uses start and stop bits. In normal operation when the sync pattern (models 2332 and 2334) or start bit (model 2333) is detected the state counter is advanced and the adapter assembles the incoming data characters and strips off the parity, start and stop bits before sending the data to the multiplexer controller. If a parity error is detected the data byte will either be sent with the error with the MSB set or an 80 Hex character will be sent to the multiplexer. This is a patch option.

b. Orders

The orders are decoded and perform the same functions as described in Section 3.2.14.3, except that the CRC order is not employed and a Stop Data order is used. The Stop Data order is issued to terminate the receive function after an entire message has been transferred to the processor.

c. Receive Interrupts

There are three receive interrupt conditions: loss of carrier, parity error, and data rate error (failure of multiplexer to accept the assembled character). The ICB request gates the interrupt bits onto the data bus. The ICB request is produced by $\overline{\text{RDATA}}$ and RACK when state 101 occurs, when a parity error occurs, or when there is no carrier ($\overline{\text{CARRIER}}$). When there is no RDATA, RICB raises the REQUEST line to the multiplexer.

The bit 2 interrupt is a parity error. It occurs during state 140 whenever the parity detector detects a parity error on the incoming data.

The bit 4 interrupt is the data rate error. It originates from the overrun flip-flop whose inputs, RDATA and SCR, set the flip-flop and flag a data overrun condition if a data character is not transferred during the SCR pulse. The adapter and multiplexer transfer a data character between the beginning of REQUEST and the beginning of REQ RESET. If RDATA is still high when SCR changes, the next character has been introduced before the last one was transferred. In this case the overrun flip-flop is set and it in turn sets state 101, which produces the data rate error to ADB4.

The bit 5 interrupt signifies that either a parity error or an overrun condition has occurred. The RERROR flip-flop is set when a parity error occurs or state 101 is entered in an overrun condition. To determine which error has occurred, the multiplexer examines the other bits on the data bus.

Interrupt bit 6 is set by $\overline{\text{CARRIER}}$ when there is no carrier received from the modem.

3.2.15.4 Transmit Circuit Description. The transmit circuit operation (Figure 3-56) is basically the same as that for the transmit circuits in the modem adapter model 2331 (refer to Section 3.2.14.4) except for the following:

1. The cyclic redundancy check (CRC) register is not used.

2. Only one start transmit order is employed. The start idles order is still used, and a new stop data transmit order is used.

3. A parity generator is installed, which produces parity bits for the transmitted characters. The parity bits are put on the data characters in the parallel-to-serial converter that also generates start and stop bits for the data characters.

4. Additional patch plugs are installed (refer to Chapter 2 for the patches) for options.

a. Initialization

Initialization is basically the same as that described in Section 3.2.14.4.

b. Orders

Three orders are used to control the adapter: start transmit (TSTRTXMIT), stop transmit (TSTOP DATA), and transmit idles (TSTRTIDLE).

c. Start Transmit

This order is issued when the program wants to transmit data to the modem. It is decoded to TSTRTXMIT in the order decoder. It performs the same basic function as the start transmit without CRC order described in Section 3.2.14.4. The main difference is that the parity generator generates an odd or an even (patch option - Z1) parity bit for each character assembled in the parallel-to-serial converter. The parity bits are sent out to the modem with the data characters. Also in the 2848 version (model 2333) the parallel-to-serial converter puts start and stop bits on the characters. Only one buffer is sent when the start transmit order is issued. Each subsequent buffer requires a start transmit order.

d. Transmit Idles

This order is decoded to start Idles (TSTRTIDLE), which sets the idles flip-flop. TSENDIDL, the idles flip-flop output, is sent out to the modem as a series of 1's or 0's depending on patch plug D7. TSENDIDL also sets status bit 5, interrupt condition bit 3 (EOR), and advances the state counter. The purpose of sending idle characters to the modem is to avoid the RTS-CTS starting delay.

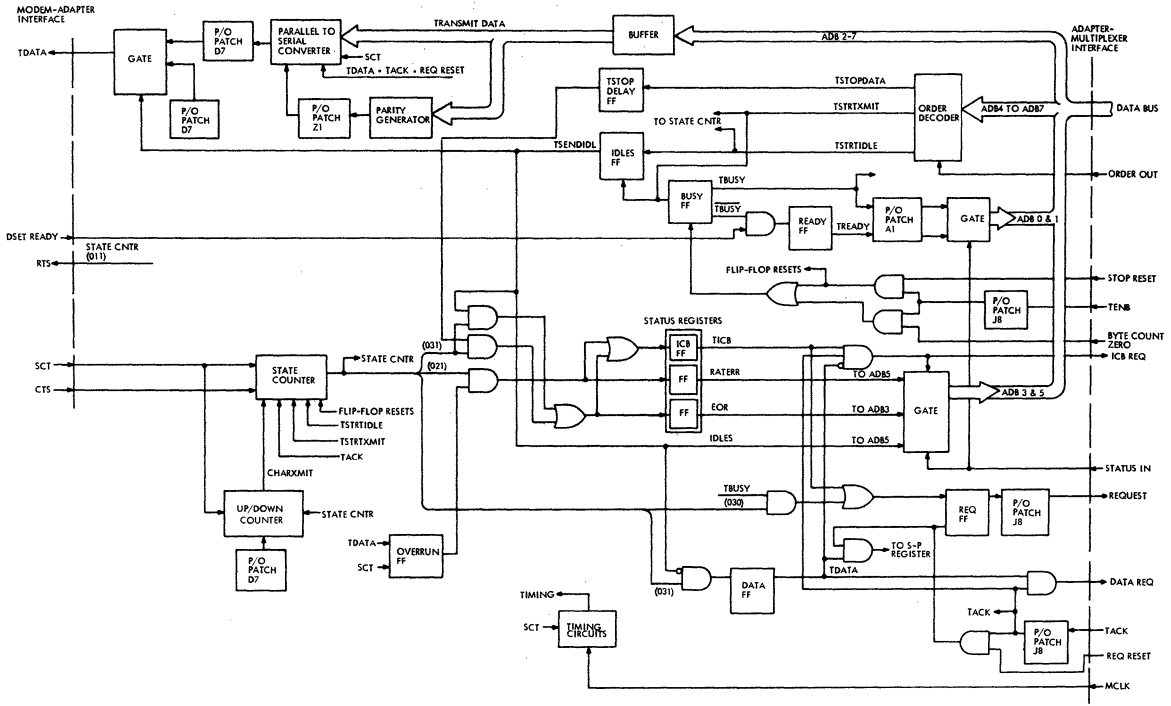


Figure 3-56. Modem Adapters 2332, 2333, 2334 Transmit Circuits, Simplified Diagram

e. Stop Transmit

This order is issued at byte count zero. It is decoded as TSTOPDATA and sets the TSTOP DELAY flip-flop. The flip-flop delays the signal for one modem character and then sets the EOR interrupt condition bit.

f. Transmit Interrupts

There are two transmit interrupt conditions: end of record (EOR) and data rate error (RATERR). The ICB Request gates the interrupt bits onto the data bus. The ICB request is produced by $\overline{\text{T DATA}}$ and TACK when a data rate error (overrun) occurs or when an end of record occurs. TICB also sets the request flip-flop, which raises REQUEST to the multiplexer.

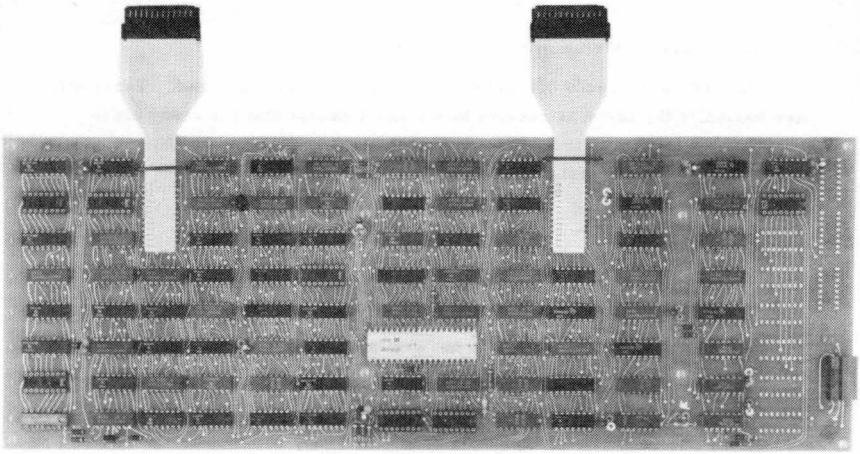
The bit 3 interrupt (EOR) occurs when the entire message has been transmitted. It is set by the output of the TSTOP DELAY flip-flop in state 031. It also is set by TSENDIDL or receipt of a transmit idles order.

The bit 5 interrupt (RATERR) is set in state 021 when an overrun condition exists. Overrun is when the next data character was not received in time to prevent a gap in the outgoing data. Overrun is produced by the overrun flip-flop when SCT occurs before the data flip-flop (TDATA) is set.

3.2.16 Modem Adapter 2341 Operation

The asynchronous modem adapter model 2341 (Figure 3-57) is the PTS-100 interface with commercial modems that do not provide clock signals for serial data interchange. The modem interface is EIA and CCITT recommendation V.24. The adapter operates at data rates from 50-9600 baud, half or full duplex with 5, 6, 7, or 8-level character codes. It has optional parity detection, (odd, even, or none selectable by a patch plug), optional stop bit length (number of stop bits selectable by patch plugs), optional reverse channel line break detection and generation, and the number of data bits per character are selectable by patch plugs. Refer to Chapter 2 for the patch plug configurations.

3.2.16.1 Interfaces. The interface between the adapter and the modem is described in Appendix C and Section 3.2.14.1 with the addition of the following lines:



C73-567

Figure 3-57. Modem Adapter 2341

Signal	Function
SECondary RDATA and TDATA lines	The 202D modems have a reverse channel (also called supervisory or secondary channel) that provides a means for simultaneous communications from the receiving station to the transmitting station while on half duplex 2-wire communication lines. This optional feature is a means of circuit assurance, provides a break signal, and facilitates certain forms of error control. Refer to Section 1 of Chapter 3 for the adapter-multiplexer interface.
Data Terminal Ready (DTR) and Terminal Busy (TB)	Two lines from the adapter to the modem that cause the modem to perform the following functions depending upon their states.

DTR	TB
0	0 - Ring
0	1 - Busy
1	0 - Answer
1	1 - Undefined

3.2.16.2 Status and ICB. Status and interrupt condition bits are reported to the multiplexer on bits 0-6 of the data bus (ADB). Bits 0 through 6 are used to report receive status conditions and bits 0 and 1 are used to report transmit status conditions. The interrupt condition bits (ICB) are described later in this section. Figures 3-58 (Receive) and 3-59 (Transmit) are simplified diagrams of the interrupt and status circuits. The status bits are generated as follows:

a. Transmit Status Bits

Only two bits, ready bit ADB0, and busy bit ADB1, are used. These bits are basically the same as receive bits 0 and 1 except that the ready bit is reset by the transmit, transmit mark, and break orders and the busy bit is reset when the order terminates.

Receive Status Bits

Data Bus Bit	Name	Description
0	Ready	When this bit is a 1, it indicates that the adapter is not processing an order and is ready to accept a message. When it is a 0, it indicates that the adapter is not available, or it may mean that the modem is not operational due to a power off or a disconnect condition. The ready flip-flop is set by the busy flip-flop and DSETREADY from the modem. When the adapter is not processing an order and the modem is ready the ready flip-flop is set by $\overline{\text{BUSY}}$ and DSETREADY. Then when a carrier is detected (CARRIER) the ready flip-flop output, READY, is gated through patch plug G4 to ADB0. The ready bit is reset when a prepare or receive order is issued.
1	Busy	When this bit is a 1, it indicates that a prepare or receive order is being processed. When it is 0, it indicates that the adapter is not busy and can accept an order. The busy flip-flop is set by the decoded prepare or receive order. The flip-flop output taken through patch plug G4 is the busy bit. The flip-flop is reset when the order terminates.
2	Parity Error	When this bit is a 1, it indicates that a parity error has been detected on the received character. The parity error signal is generated by the serial-to-parallel converter status register, which sets the parity flip-flop whose output is gated through the data bus logic gate onto ADB2. The parity bit is controlled by patch plug G4.
3	Framing Error	When this bit is a 1, it indicates that no stop bit was detected on the previous character. The bit is set by RCVDATA and FRAMERR from the serial-to-parallel converter status register during a prepare or receive order.
4	Overrun	When this bit is a 1, it indicates that the multiplexer was unable to accept the present character before the next character was sent to the adapter. The overrun status flip-flop is set by ROVERRUN, RCVDATA, CARRIER and state 05.
5	Wake up	When this bit is a 1, it indicates that a character with a correct stop bit was received during a prepare order. It is set by state 02 when there is RCV DATA.

Data Bus Bit	Name	Description
6	Break	When this bit is a 1, it indicates that the data being received changed to a spacing condition. The receive data (RDATA) or the secondary receive data (SECRDATA) (determined by patch plug E8) is gated by the no transmit order to a break detector. When there is no transmit order the break detector monitors the incoming data and produces an RBREAK output whenever a gap occurs in the incoming data.

3.2.16.3 Receive Circuit Description (Figure 3-58).

a. Timing

MCLK from the multiplexer is used by the timing circuits to generate timing for the adapter. Patch plugs M2 and M7 are used to adjust the timing to the different baud rates. Since the modem is asynchronous no modem clock is necessary. The timing circuits clock the serial-to-parallel converter and the state counter. The state counter is stepped through various states to control the phases of operation of the adapter receive circuits.

b. Data Transfer

Serial data RDATA from the modem is put into the serial-to-parallel converter shift register and clocked by the timing and control circuits into the buffer where it is gated out to the multiplexer. The adapter transfers the data to the multiplex channel controller under control of the program, which directs the adapter by sending orders on data bus bits 5, 6, and 7. Adapter status and interrupt conditions are reported to the program via the multiplexer on data bus bits 0 through 6. Status information is assembled by the control and status circuits in the serial-to-parallel converter and gated out through the adapter status registers. When a data character is in the receive shift register, the status circuit reports that fact to the other adapter circuits by raising the RCVDATA signal. If a parity error, framing error, or overrun is detected, the condition is also reported to the adapter circuits from the converter status circuit.

c. Initialization

The adapter is initialized when STOP RESET is sent by the multiplexer. When ANDed with RENB, it resets the request, busy, data, state counter, interrupt, and status flip-flops. When the busy flip-flop is cleared, ADB1 is low, indicating to the processor that the adapter is not busy. When the modem is not ready to send, the ready flip-flop is reset, and ADB0 is low indicating to the multiplexer that the adapter is not ready to process a message. The multiplexer continues to monitor ADB0 and ADB1 while the adapter is in the waiting state. When the modem is ready it raises DATA SET READY which with $\overline{\text{BUSY}}$ sets the ready flip-flop. Then when the modem sends a message to the adapter it raises the CARRIER line, which gates Ready onto ADB0.

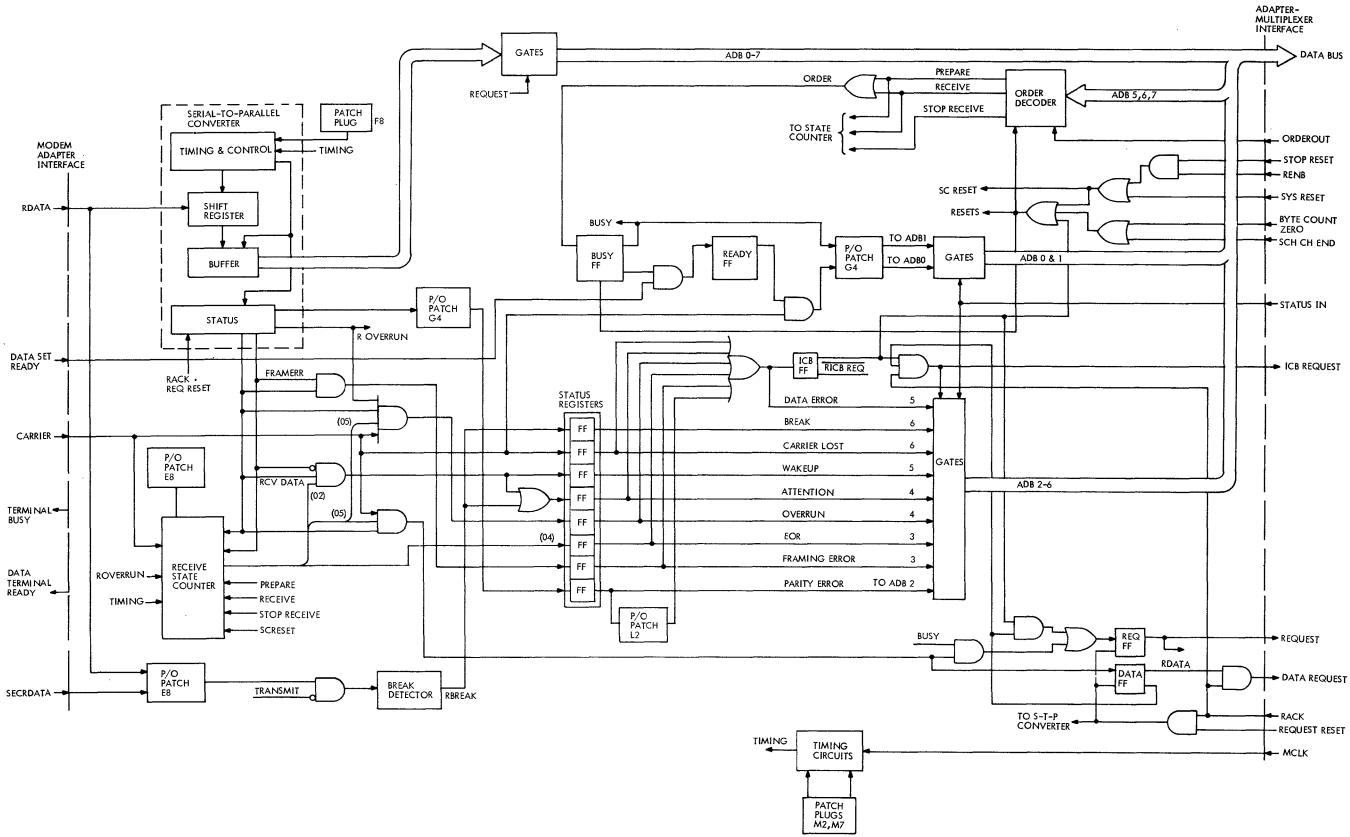


Figure 3-58. Modem Adapter 2341 Receive Circuits, Simplified Diagram

d. Prepare Order

When the processor is ready to begin operation it sends the Prepare order to the adapter to put it in the waiting state. This enables the adapter to monitor the communications line and signal the multiplexer when the modem becomes active. No data transfer occurs as a result of this order. The order is terminated as the first character is received.

The Prepare order is gated onto the decoder by ORDER OUT. Here it is decoded, and PREPARE sets the busy flip-flop and advances the receive state counter to state 02. When the first character of data from the modem arrives in the buffer the serial-to-parallel converter status circuit reports the presence of the character by raising RCVDATA. State 02 and RCVDATA are ANDed to set the wake up flip-flop and put WAKEUP on ADB5. When the multiplexer detects WAKEUP on ADB5 the program normally responds with a Receive order.

e. Receive Order

This order enables the adapter to assemble characters from the modem and send the characters over the parallel data bus to the multiplexer. Characters assembled prior to the order are ignored. If the adapter is in the process of assembling a character when this order arrives, that character will be the first sent. If the command is given while the adapter is busy and not ready the command is ignored, and the multiplexer sets an ICB bit. Except for the parity, stop, and start bits the adapter is transparent to all characters received. The stop and start bits are stripped off the received character by the serial-to-parallel converter circuit. The parity bit is selected by patching options. Termination of this order normally occurs when a search condition has been satisfied or by the byte count equal zero (BCZ).

The Receive order is gated into the decoder by ORDER OUT. The Receive order sets the busy flip-flop which raises BUSY, on ADB1. The Receive order also advances the state counter to state 05. When there is a character in the serial-to-parallel converter, RCV DATA, state 05, CARRIER and BUSY set the request and data flip-flops. The output of the request flip-flop is sent to the multiplexer as REQUEST. The multiplexer responds with RACK. RACK gates RDATA from the data flip-flop to the multiplexer as DATA REQUEST. REQUEST also enables the data bus gates, which gate the data character onto the data bus. The multiplexer responds to DATA REQUEST with REQ RESET. REQ RESET and RACK reset the request and data flip-flops and the status register circuit in the serial-to-parallel converter. When the next character is received RCV DATA again initiates the REQUEST-RACK-DATA-REQUEST-REQUEST RESET cycle and transfers this character to the multiplexer as before. This process continues until the program sends byte count zero or search character found, whereupon the adapter circuits are reset.

f. Stop Receive Order

Normally this order is sent to the adapter after a receive order has terminated because of byte-count-zero or search character found. It advances the state counter to state 04, which sets the EOR ICB bit.

g. Receive Interrupts

There are six receive interrupt conditions: loss of carrier, overrun (failure of multiplexer to accept the assembled character); EOR (end of record), framing error, parity error, and wake up or break. The ICB request gates the interrupt bits onto the data bus. The ICB request is produced by $\overline{\text{RDATA}}$ and RACK when any interrupt condition occurs. When there is no RDATA, ICB request raises the REQUEST line to the multiplexer.

The bit 2 interrupt, which is optional (patches L2 and G4), is the parity error. It is initiated by the serial-to-parallel converter status circuit when incorrect parity is detected on the received character.

There are two bit 3 interrupts: EOR, which signifies that the message is complete, whereupon the adapter is ready to process a new message (EOR is set by state 04 at the end of a data transfer sequence); and Framing Error, which is initiated by the serial-to-converter status circuit when no stop bit is detected on the previous character.

The bit 4 interrupt is either an ATTENTION or a data rate error (overrun). Overrun originates from ROVERRUN in the serial-to-parallel converter status circuit whenever a data character is not transferred to the multiplexer before the next character is assembled in the converter.

Attention is set when either WAKEUP status bit 5 or BREAK status bit 6 is set.

The bit 5 interrupt, DATA ERROR, is set when any of the ICB conditions occur.

The bit 6 interrupt is CARRIER LOST. It is set if the received carrier is lost during the execution of a Receive order.

3.2.16.4 Transmit Circuit Description (Figure 3-59).

a. Timing

The timing is the same as the receive circuits except that the timing signals clock a parallel-to-serial converter and the transmit state counter, which drives the transmit circuits.

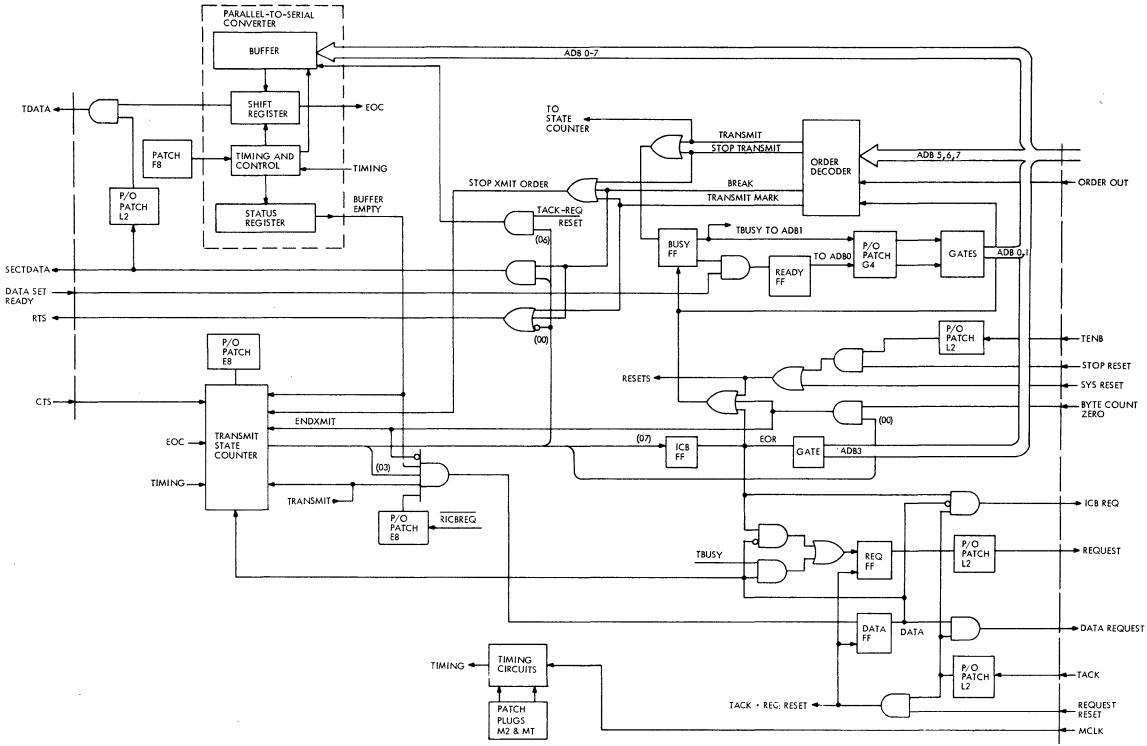


Figure 3-59. Modem Adapter 2341 Transmit Circuits, Simplified Diagram

b. Data Transfer

Parallel data from the multiplex channel controller (data bus ADB 0 through 7) is loaded into a buffer in the parallel-to-serial converter where it is transferred to a shift register by TACK, REQ RESET, and state 06, and clocked out serially to the modem. Data transfers are under control of the program, which directs the adapter by sending orders on the data bus bits ADB 5, 6, and 7. Adapter status and interrupt conditions are reported to the program via the multiplexer on data bus bits ADB 0, 1, and 3.

When the transmit shift register has been emptied, the transmit control circuit reports the end of character signal (EOC) to the adapter. When there is no character present in the transmit circuit, the status register reports an empty buffer (BUFFER EMPTY) to the adapter.

c. Initialization

The adapter is initialized when STOP RESET is sent by the multiplexer. When ANDed with TENB, it resets the state counter and the busy flip-flop. When the modem is ready to receive it raises DSETREADY, which with BUSY sets the ready flip-flop. TREADY is then gated onto ADB0 indicating to the multiplexer that the adapter and modem are ready to begin data transmission.

d. Transmit Order

This order is issued to the adapter when the program wants to transfer data to the modem. It is gated into the decoder by ORDER OUT. The decoder decodes the order to TRANSMIT, which sets the busy flip-flop. TBUSY, now high, is applied through patch plug G4 to ADB0 to indicate to the multiplexer that the adapter is busy.

TRANSMIT also advances the state counter out of state 00, which raises RTS (request to send) to the modem. If the modem is ready to begin data transfer, it replies with CTS (clear to send). CTS advances the state counter to state 03. State 03, TRANSMIT, BUFFER EMPTY, no receive interrupt ($\overline{\text{RICBREQ}}$) and no end transmit ($\overline{\text{ENDXMIT}}$) set the data flip-flop. Then DATA and TBUSY set the request (REQ) flip-flop that sends REQUEST to the multiplexer, which responds with TACK. TACK gates DATA REQUEST from the data flip-flop to the multiplexer, signifying that data service is requested. The multiplexer replies with REQ RESET and puts the first character on the data bus. DATA also advances the state counter to state 06, which, with REQ RESET and TACK, gate the character into the parallel-to-serial converter. Then TIMING clocks the character out serially to the modem. The next characters are sent in the same way until byte count zero (BCZ).

At BCZ, while transmitting the last character sent by the program, the Transmit order is terminated and the busy flip-flop is reset. The adapter enters the ready and not busy state and another Transmit order, a Break order, a Transmit Mark order, or a Stop Transmit order may be sent to the adapter. If a Break, Transmit Mark, or Stop Transmit order is sent before the present character has been transmitted, after the last bit of the character has been transmitted, the state counter is advanced to state 07, which sets the end of record (EOR) ICB bit.

e. Break Order

The Break order causes a continuous space to be sent to the modem until a Stop Transmit order is received, whereupon the end of record bit is set. The adapter remains in the ready and not busy state (ADB0 = 1) while performing this order. Any order except Transmit Mark may be sent to the adapter while it is performing the Break order.

The Break order is gated into the decoder by ORDEROUT. The decoded order, BREAK, puts the state counter into state 00, raises RTS to the modem, and puts continuous spaces on the TDATA and SEC TDATA output lines. Patch L2 controls the connection to the TDATA line. If the connection is closed the output gate is inhibited by the break order and TDATA is continuous spaces.

f. Transmit Mark Order

This order is the same as Break, except that a continuous mark is transmitted on the communication line until a Stop order is issued. The purpose of this order is to cause the modem to keep its carrier high without transmitting data. The Transmit Mark order performs the same function as the Break order except that the TDATA and SEC TDATA lines are not inhibited so a continuous mark is transmitted.

g. Stop Transmit Order

This order causes the end of record (EOR) bit to be set. The adapter remains in the ready and not busy state. If the order is received after BCZ of a Transmit order, the (EOR) bit is set after the last character has been transmitted.

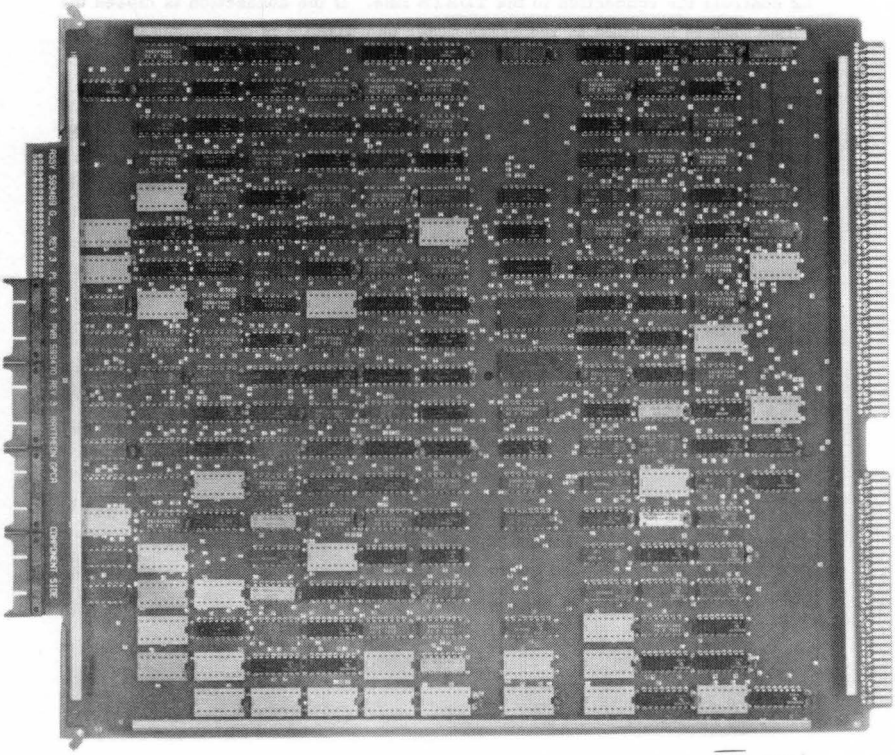
This order is gated into the decoder by ORDEROUT and decoded. The decoded order, STOP TRANSMIT, sets the state counter to state 07 after BUFFER EMPTY is issued by the parallel-to-serial converter. State 07 sets the ICB Request, puts the EOR bit on ADB3 and sets REQUEST.

h. Transmit Interrupts

The Break, Transmit Mark, and Stop Transmit orders advance the state counter to state 07. State 07 is also set at BCZ by ENDXMIT. State 07 sets the ICB flip-flop, which initiates REQUEST and ICB REQUEST when no data is being transmitted ($\overline{\text{DATA}}$). The multiplexer responds to REQUEST with TACK, which gates ICB REQUEST to the multiplexer. The ICB flip-flop generates the EOR bit that is put on data bus ADB3.

3.2.17 General Purpose Communication Adapter Operation

The general purpose communication adapter (GPCA) is a microprogrammable communications adapter that interfaces the PTS-100 multiplex channel controller with up to four 50 to 4800 baud serial communication line modems. With the GPCA, the PTS-100 system can communicate with four half-duplex/simplex or two full duplex communications lines. The GPCA can be microprogrammed to communicate on private or switched network lines with any combination(s) of communications protocols presently in common use. The GPCA is contained on one full printed circuit board (illustrated in Figure 3-60), and may be installed in any PTS-100 motherboard slot.



$\overline{\text{C74}}$-1236

Figure 3-60. General Purpose Communication Adapter

The GPCA provides all the interface control functions necessary for the various types of communications modems. These include character assembly/disassembly, redundancy generation and checking, odd or even parity, control character recognition, and insertion of start/stop bits for asynchronous operation. (Refer to Chapter 2 for the patch plug configurations.)

The interface with the multiplexer requires from one to four multiplexer ports, depending on the number and types of communication channels in use. Table 3-15 shows the various configurations possible. Figure 3-61 illustrates a typical configuration for the IPARS system application.

Table 3-15. Communication Line Configurations

Port 1	Port 2	Port 3	Port 4	No. of Ports
FDX	Not Used	FDX	Not Used	4
FDX	Not Used	HDX	HDX	4
FDX	Not Used	HDX	Spare	3
FDX	Not Used	Spare	Spare	2
HDX	Spare	Spare	Spare	1
HDX	HDX	Spare	Spare	2
HDX	HDX	HDX	Spare	3
HDX	HDX	HDX	HDX	4

FDX = Full Duplex
HDX = Half Duplex or Simplex

3.2.17.1 Interfaces. The block diagram of the GPCA (Figure 3-62) relates the interface lines to the various functional blocks making up the unit. The GPCA utilizes the standard multiplexer interface, as discussed in Section 3.2.4. In addition, the GPCA provides four sets of lines to up to four communications modems. Each set contains two serial data lines (one transmit and one receive) two timing lines (also one transmit and one receive) and five control lines (DSR, DCD, CTS, RTS, and DTR). The functions of each of these lines was discussed in Sections 3.2.14.1 and 3.2.16.1. In addition, there are three control lines for use with the autocall system. Two (ASDSR and ASDTR) are signals from the modems (DSR and DTR) sent to the autocall unit adapter (ACUA) via the GPCA. The third (ABT) is an abort signal from the ACUA which tells the GPCA that the autocall system has not been able to obtain the desired connection. (Also see Appendix C for a description of the lines.)

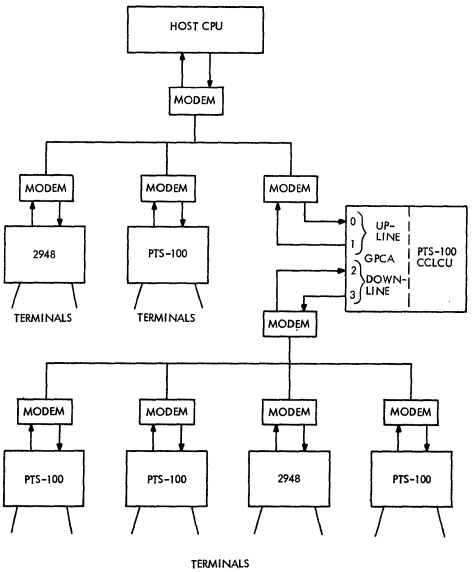


Figure 3-61 . IPARS CCLCU Typical Configuration

3.2.17.2 General Circuit Description. Figure 3-62 illustrates the various functional blocks of the GPCA. It is composed of an arithmetic logic unit (ALU), with its associated input and output registers; a read-only memory (ROM) with program counter, hold register and instruction decode circuits; a 32 register working stack, containing eight different types of registers for each of the four communications channels; multiplexer interfacing and timing circuits; communications interfacing and timing circuits; order registers, and internal status registers.

The arithmetic logic unit and associated input and output registers perform all the necessary serial/parallel conversion, error checking, parity and CRC generation, stop and start bit insertion, and other functions necessary to convert information from the PTS-100 format into required modem formats (and vice versa) under control of the microprogram.

The ROM holds the microprogram which provides the necessary communications protocols for the specific application, and allows multiplex control over the four sets of communications channels. Each communications modem operates independently of the others, and therefore may have different types of data on it, utilize different control codes, or have different data rates.

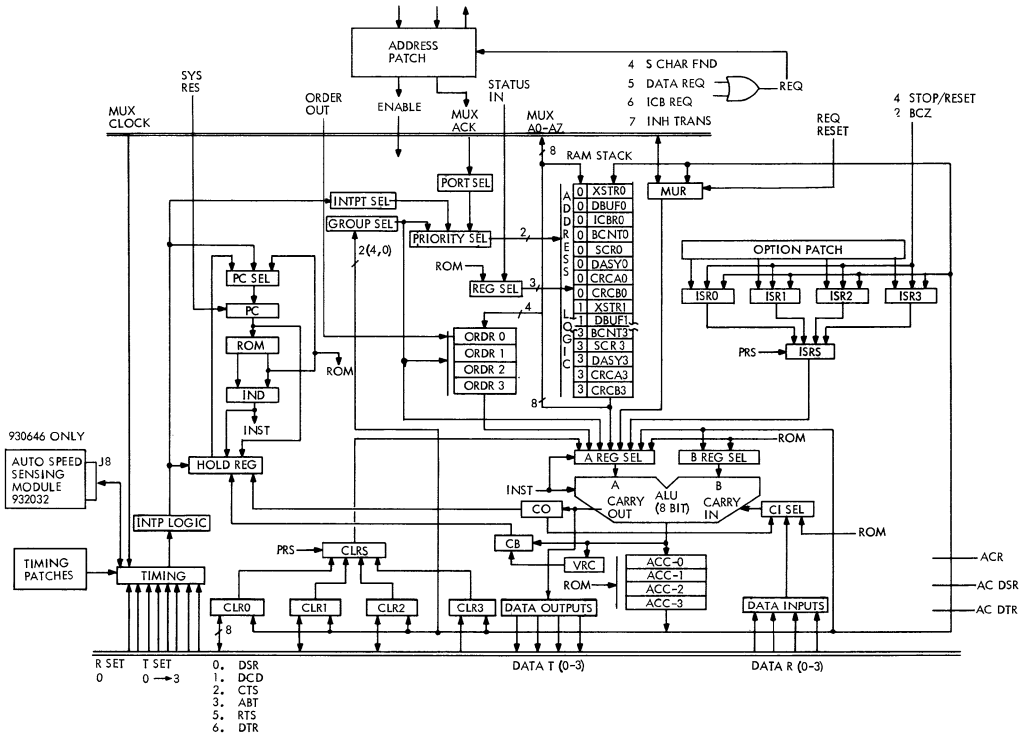


Figure 3-62. General Purpose Communication Adapter, Block Diagram

The working register stack includes registers for the storage of status data (XSTR), data ready for (or from) the multiplexer (DBUF), status of the ICB conditions (ICBR), registers for CRC generation or checking (CRCA and CRCB), registers for data transfers to (or from) the modems (DASY), scratch pad registers (SCR), and registers to keep track of the number of bits assembled into characters (BCNT).

The multiplex register (MUR) provides four signals to the multiplexer as required for system operation. These are search character found (SCF, bit 4 of the MUR), Data Request (bit 5), ICB Request (bit 6), and Inhibit Translate (bit 7). In addition, data request and ICB request are ORed to provide the REQUEST signal. The actual REQUEST line raised is under control of the priority select logic, thus requesting any one of four ports from the multiplexer. MUR is reset by the REQUEST RESET line from the multiplexer.

The communication line registers (CLR) hold the interface control signals for the modems. These signals include data set ready (DSR, bit 0 of CLR), data carrier detected (DCD, bit 1), clear to send (CTS, bit 2), abort (ABT, bit 3), request to send (RTS, bit 5), and data terminal ready (DTR, bit 6). In addition, there are serial data output and data input lines to each modem (Data T and Data R). The GPCA operates over a data rate of 50 to 9600 baud synchronous and 50 to 4800, asynchronous.

Orders for each communication channel are received from the multiplexer and stored in the appropriate order register. They are interpreted by the microprogram (different applications have different meanings for the same order code).

The internal status registers keep track of the status of each order as it is being processed, and flag certain options and control conditions. They are utilized in conjunction with an option patch panel which defines the options being implemented in the system. Bit 7 is the asynchronous flag (defines synchronous or asynchronous operation). Bit 6 is the option patch flag (has several meanings, usually odd or even parity). Bit 5 is an enable flag. Bit 4 is the stop I/O flag (set by stop/reset line). Bit 3 is the asynchronous start flag. Bit 2 is the byte count zero flag (set by BCZ line).

The priority select register specifies the sets of registers that are currently being operated on. It is under control of interrupt circuitry (from the modems), port selection circuitry (from the multiplexer) and group selection (from the ALU).

3.2.17.3 Autospeed Sensing. GPCA 930646 has the capability of automatically sensing the modem baud rate and adjusting the GPCA timing to interface channel. Only four baud rates can be recognized, they are: 1200, 300, 150 and 110. When the auto speed sensing option is used, module 932032 is plugged into J8 on the GPCA.

3.2.17.4 Initialization and Timing. The GPCA may be initialized through either the STOP RESET or SYSTEM RESET lines. SYSTEM RESET is used to reset the entire GPCA, including all four channels and the program counter. STOP RESET is used when only one channel is to be reset, and it will have no effect on any of the other channels. When this line becomes true, it sets a flag in the appropriate internal status register (ISR bit 4). The presence of this flag is detected by the microprogram, causing it to reset specific registers associated with the selected channel. The registers reset include ICBR, CLR, ISR, XSTR, SCR, ORDR, and BCNT. However, XSTR is reset to a "ready, not busy" condition. The STOP RESET microprogram subroutine takes 3.5 microseconds to execute.

SYSTEM RESET is hardwired to reset the program counter and several other registers. When the program counter is reset, it causes an initialization subroutine to reset all registers in all four channels.

Basic timing is derived from the multiplexer I/O clock (160 nanosecond period). All other timing (GPCA and modems) is slaved to be synchronous with it. In the transmit mode, timing signal TSET is used by both the GPCA and the modems (synchronous only) in sending data out. TSET and the multiplexer clock, which is divided down to the desired baud rate (selectable through a timing patch) produce an interrupt clock that drives the interrupt circuits. The interrupt circuits generate a signal that interrupts the microprogram long enough to send out the desired data bit, at which time the microprogram is returned to its previous activity. For received synchronous data, a similar interrupt is generated by RSET, which comes from the modem with data. Nonsynchronous data causes the counter to be resynchronized with each start bit. Each modem has equal priority in interrupts.

3.2.17.5 Receive Circuit Description. The microprogram resident in the ROM specifies whether parity, CRC, or LRC checking is to be employed on the incoming data, and, if parity, whether it is odd or even parity. The option patch network associated with the internal status register specifies whether synchronous or asynchronous operations are being performed, and if the latter, whether one or two stop bits are being used.

The arrival of received data in the modem causes the issuance of a timing signal (RSET) to the GPCA. This signal in turn interrupts the microprogram and causes the received data bit to be clocked into the carry in circuits of the ALU. After each bit is received, it is stored in the data assembly register (DASY) of the working stack, and the microprogram is released to return to other tasks. The BCNT register keeps track of the number of bits received, and when a complete character has been assembled it is moved to the data buffer register (DBUF) for transmission to the multiplexer. This is accomplished through the raising of the REQUEST and DATA REQUEST lines, which

tell the multiplexer that a character is ready. Upon receipt of the acknowledge signal from the multiplexer, the character is placed on the adapter data bus for transmission.

Special characters (start of message, end of transmission, CRC) as well as start and stop bits (if utilized) are not sent to the multiplexer, but are used within the GPCA.

3.2.17.6 Transmit Circuit Description. Data that is to be sent out to the modems is received from the multiplexer over the adapter data bus, and loaded into the appropriate data buffer. When the timing circuits generate TSET, this data word is taken from the DBUF and placed into the ALU, where any necessary start and stop bits are added to it. The data is then shifted left one bit position, and the carry out bit is sent to the modem over the data output circuits. The remainder of the data character is then restored in the working register stack until a new TSET is received, at which point another data bit is shifted out. When BCZ is received, or transmission has been completed (depending upon the order), a CRC character is added if required, and the end of transmission is signaled to the multiplexer.

3.2.17.7 Order Codes. Order codes are received by the GPCA over the adapter data bus, bits 3 through 7. Bit 3 is a chaining bit; the other bits specify the order to be performed. The meaning of the order codes is under microprogram control, and depends upon the system application. For example, 1001 is used in the IPARS application to continue a transmission with no CRC character after receipt of BCZ. The same order code in the AMASN application is used to disable the Mark order (stop transmission of continuous mark bits). A complete listing of the order codes available in the GPCA for each application appears in Section 3.1. This section will discuss the implementation of these orders in the GPCA.

The first set of orders is applicable to the AMASN application.

a. Enable Call - Disable Call

These two orders are used by the PTS-100 system to enable/disable the modem from answering an incoming telephone call. It is implemented in the GPCA by raising/lowering the DTR line to the modem. The order code is read from the appropriate order register by the microprogram, which subsequently sets/resets bit 6 in the communication line register, which in turn controls the DTR line. The enable order can be terminated by either the processor (through the disable order) or the modem (through its DSR line) indicating that it has received an incoming call.

b. Prepare - Receive

These two orders are quite similar. Both cause the GPCA to assemble and send received data to the multiplexer. The only difference is in the handling of a space in the stop bit position. If this occurs, Prepare will notify the processor of the receipt of a Break order, while Receive will indicate that a framing error has occurred. The former order is useful in systems in which the communications protocol starts all messages with a Break order. In either case, if no space is received in the stop bit position, the message will be received and sent to the processor through the multiplexer. If the space occurs, Prepare will cause a bit to appear in status bit 4, while Receive will cause a bit to appear in status bit 3. Both will then terminate the order. The operation of the GPCA in receive modes is discussed in Section 3.2.17.4.

c. Transmit - Transmit Complete

These two orders are quite similar. The Transmit order causes the GPCA to request characters from the processor and send them to the modem, with BCZ used to terminate the transmission. Transmit Complete also requests characters and sends them to the modem, but it does not terminate until the last bit of the last character has been sent. The operation of the GPCA in transmit modes is discussed in Section 3.2.17.5.

d. Mark - Disable Mark

Mark causes the GPCA to transmit a continuous series of Mark bits. This will occur in the modem as soon as the RTS (request to send) line is raised to the modem, and it sends back the CTS (clear to send) signal. No characters are transmitted, and no further action need be taken by the GPCA to keep the modem transmitting. Disable Mark may be used for termination, or any of the transmit orders may be used to change the transmission from Marks to characters.

e. Break

This order may be used after any of the transmit (or Mark) orders to cause the GPCA to send a continuous space signal to the modem. The length of the Break signal is under the control of BCZ.

f. Dial

This order is an optional order which causes the auto call unit to originate a call over the switched network. Dial digits are transferred from the processor to the ACU via the GPCA and the ACUA under control of BCZ. After BCZ is received, the GPCA waits for a response from the ACUA to indicate that the call has either been completed or abandoned. Call completion causes ICB bit 3 to be set; abandonment causes ICB bit 4 (and status bit 7) to be set.

The following orders are used in the IPARS applications.

g. Start Receive - Continue Receive

Start Receive causes the GPCA to enable its receive circuitry and look for a start sync pattern in the modem data stream. After receipt of the start sync pattern, normal receive operations commence until a BCZ or SCF (search character found, indicating end of transmission character has been received). If chaining is to be implemented, Continue Receive must be sent after BCZ has been received by the GPCA. Continue Receive is ignored if the adapter is not already receiving data. A detailed discussion of Receive operations is covered in Section 3.2.17.5.

h. Check CRC

If a CRC character is expected, this command must be sent after receipt of the EOM character by the GPCA. It causes the GPCA to check the next received character against the computed CRC character. If no CRC check is to be performed, a STOP RESET command must be sent after receipt of the EOM character.

i. Start Transmit 1 - Start Transmit 2

These transmit orders are similar except for the transmission of a CRC character. With Start Transmit 1, no CRC character is transmitted at BCZ. With Start Transmit 2, a CRC character is transmitted at BCZ. Note that if chaining is in use during transmission, no CRC character should be sent until the final chained message. A detailed discussion of the transmit modes is covered in Section 3.2.17.6.

j. Continue Transmit 1 - Continue Transmit 2

These orders are similar to the two listed above, but are used during chaining when a transmit has already begun and was terminated at BCZ.

k. Transmit Idles

This order causes the GPCA and modem to send out idles continuously, thus keeping the transmission line active.

l. Send New Sync

This order may be used between received messages to request a new sync signal for the following message.

3.2.17.8 Status and ICB. The GPCA has an 8 bit status register and an 8 bit ICB register to store the status and ICB information for each of the four communications channels. All eight of these registers are a part of the working stack of registers, a group of 32 8 bit registers. Other registers in this stack are used for data buffering to the MUX, character assembly, redundancy checking, and for scratch pads.

In addition to the external status register in the stack, there is also an internal status register for use by the microprogram. This register contains flag bit positions for character assembly, option patch, enable, stop, start, and BCZ.

The first two bits in the (external) status register define Adapter Ready and Adapter Busy conditions, with a zero in the first two bits specifying that the referenced modem is not available. The remaining status bits are defined by the microprogram for the specific application. For example, status bit 5 in an IPARS transmit condition indicates that the transmit circuitry is sending idles. In IPARS receive operations, bit 3 indicates the presence of a CRC error, and bit 4 the presence of a data rate error.

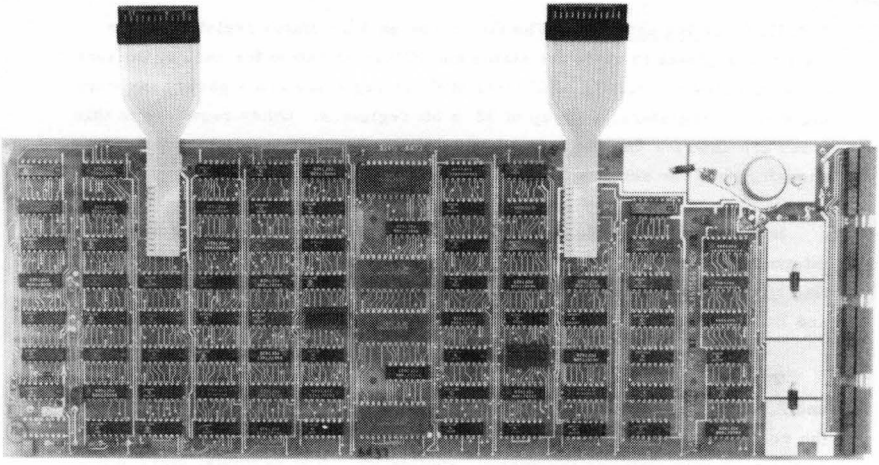
In AMASN applications, transmit status bits include disconnected (bit 5), and abandoned call (bit 7). Receive status bits include: no carrier (bit 2); framing error (bit 3); reception break (bit 4); disconnected (bit 5); and parity error (bit 6).

The ICB register has five bit positions available for ICB data. Bit positions 0, 1, and 2 are not used for ICB purposes by the GPCA. Bit positions 3 through 7 are read by the multiplexer after an ICB request has been generated, and are assigned different meanings for each application. In IPARS, bit 2 refers to an invalid start, bit 3 to an EOR condition, bit 5 to a data rate error under transmit, and to a data error during receive. In addition, in the receive mode only, bit 6 refers to carrier lost, and bit 7 indicates that a new sync order is terminated.

The ICB bits have the following meanings in the AMASN application: For receive, bit 3 is order complete, and bit 5, data error. In transmit, bit 3 is also order complete, bit 4 is attention, and bit 5 is a data error.

3.2.18 Cassette Adapter Operation

The cassette adapter (Figure 3-63) serves as the interface between the tape cassette drives and the multiplex channel controller. Each cassette adapter can drive a maximum of four tape drives; however, only one drive may be in operation at any one time.



C75-1856

Figure 3-63. Cassette Adapter C

3.2.18.1 Circuit Description. A simplified circuit diagram of the cassette adapter is shown in Figure 3-64. Data from the processor is transmitted to the cassette adapter through the multiplexer, and is received on the adapter data bus, in 8 bit parallel bytes. This parallel data is converted to a serial bit stream in the cassette adapter by a parallel to serial converter. It is then encoded using biphase data encoding, and written on the tape by the FLUX 0 and FLUX 1 data lines. Biphase encoding uses a transition in the middle of all bits to represent a one, and no transition to represent a zero. See Figure 3-65.

In addition to the data being recorded, a preamble is written at the beginning of each record, and a CRC word (cyclic redundancy code) is added at the end of each record for checking, as shown in Figure 3-65. As the data is read off the tape, the preamble is detected to ensure that the beginning of the tape record has been selected, and at the end of the record the CRC word is checked to ensure that the data is read out errorfree. Data read from the tape is received via the data line, decoded, converted to parallel bits, and read to the multiplexer over the adapter data bus.

To control tape motion, five commands are utilized. These commands are also sent across the adapter data bus, and are identified by the use of the Order Out control line from the multiplexer. The commands are: Read, Write, Backspace Record, Rewind, and Erase. Read, Write, and Erase

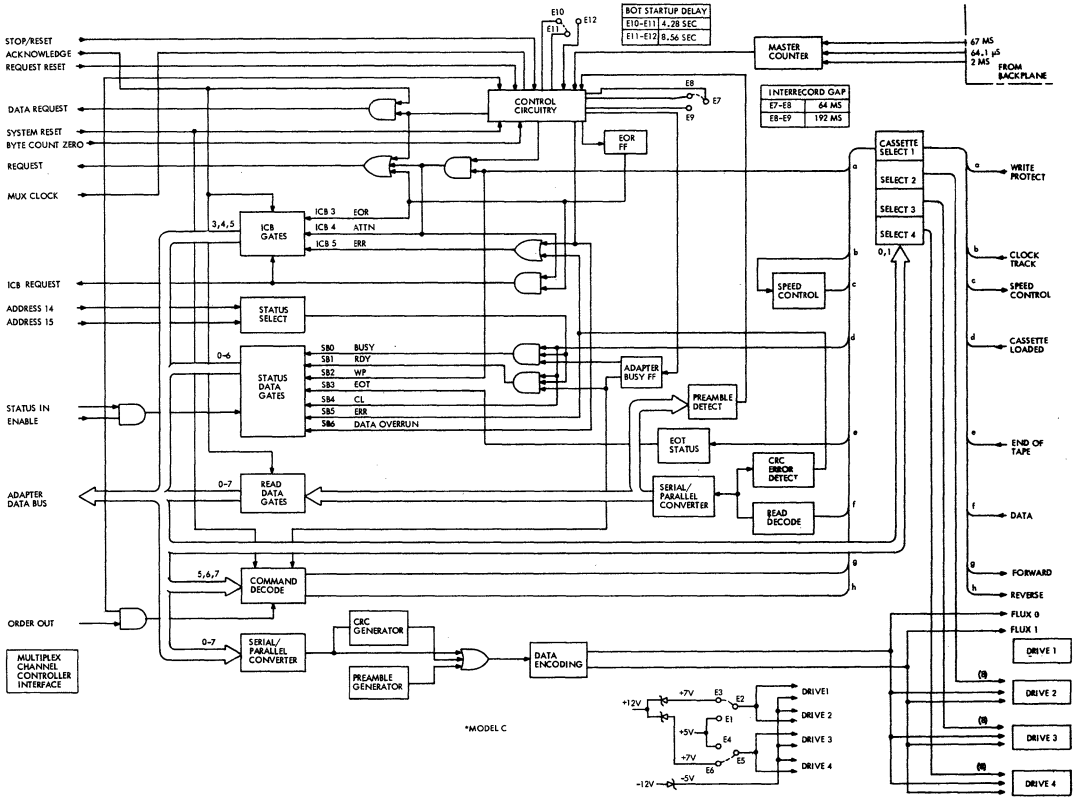
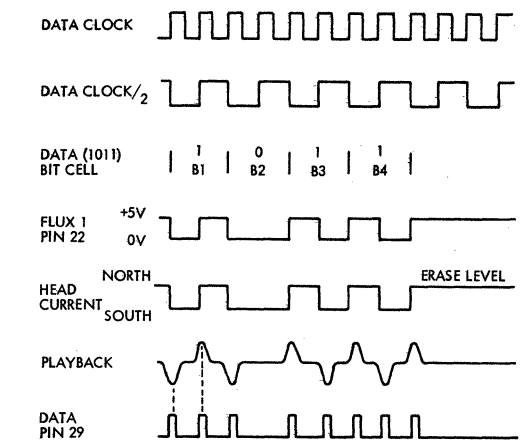
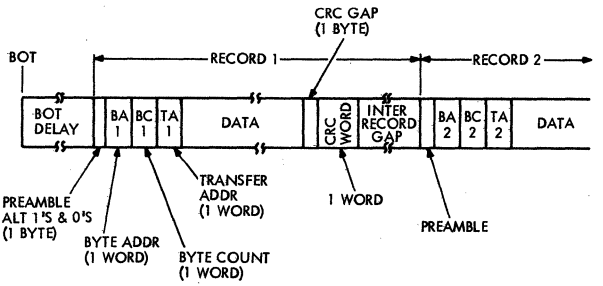


Figure 3-64. Cassette Adapter, Simplified Circuit Diagram



A. BIPHASE DATA ENCODING



B. CASSETTE TAPE FORMAT

Figure 3-65. Biphase Data Encoding and Cassette Tape Format

commands are decoded to control forward tape motion, as well as to route the data to the appropriate circuits. Backspace Record and Rewind (backspace to the beginning of the tape) are decoded to control reverse tape motion. A rewind command must be issued before the tape can be read when starting at the beginning of the tape.

Seven status bits are available for the adapter and its associated tape drives to report their status to the multiplexer: adapter busy, adapter ready, write permit tab removed, end of tape, cassette loaded, CRC error, and data overrun. This status information is sent to the multiplexer (and then to the processor) after the receipt of a Status In control signal from the multiplexer.

Status bit 0 defines adapter ready (i.e., a "1" indicates Ready). Bit 1 defines adapter busy (i.e., a 1 indicates that the adapter is busy). Both bits 0 indicates that the selected cassette is not ready (for example, cassette not loaded or not connected). Both bits 1 is an undefined condition.

Status bit 2 indicates that a write or erase order has been directed against a tape that has its write permit tab in the write protect position. Since this tab must be in place to allow writing on the tape, an attempt to write on a tape with the tab in the wrong position (or missing) will result in the setting of this status bit. It will also cause interrupt bit 4 to be set and will prevent writing on the tape.

Status bit 3 indicates either a beginning of tape or an end of tape condition, thus requiring a rewind or backspace record order before write, read, or erase may be accomplished. Status bit 4 indicates whether the cassette has been loaded with a tape. The use of this bit, in conjunction with bits Zero and One will tell the processor whether the addressed cassette drive is disconnected, or missing a tape.

Status bit 5 indicates that a CRC error has been detected on the last data record read out, and therefore the validity of the data transmitted to the processor is open to question. Status bit 6 indicates that a data overrun condition has occurred. That is, some data has been lost during transmission between the multiplexer and the cassette.

In addition to status information, three interrupt condition bits (ICB) are sent from the adapter to the multiplexer. ICB 3 indicates that an EOR (end of record) has been reached, thus signifying to the multiplexer that its backspace record, rewind, or read order has been carried out. (Write and erase orders are controlled by the byte count zero line although new orders will not be accepted until after an EOR.) ICB 4 indicates that operator attention is required. This occurs if a write order has been attempted on a cassette without the write permit tab in place, or an order has been directed to a cassette drive without a cassette being loaded. These ICB's cause an immediate notification of the condition to the multiplexer. ICB 5, and all status bits are only transmitted to the multiplexer after an EOR has been generated. ICB 5 is the error indication. It indicates that either a data overrun or a CRC error has occurred. Ambiguities in ICB's 4 and 5 may be resolved by looking at the appropriate status bits (2, 4, 5, and 6).

Other circuits present in the cassette adapter control the speed of the tape drive (40 ips is used for rewind and 10 ips for the other four commands) and control the interface circuitry. To control tape speed, a clock track that has been permanently recorded on the tape is used. This track is recorded at 800 bpi (bits per inch). The rate of receipt of the clock track is used by speed control circuitry to adjust the speed of the tape drive motors.

Signals such as acknowledge, request, request reset, multiplexer clock, and enable are used at the multiplexer interface to control the flow of data, status information, and control signals between the multiplexer and the cassette adapter. A description of their operation is covered in Section 3.1. The following section discusses some of these lines as they relate particularly to the cassette adapter.

All input/output activity is initiated through the execution of a Do I/O instruction from the processor. Neither the tape drive nor the adapter may initiate activity. Each Do I/O instruction executing an order must include as its argument the effective address of the PIOT table specifying the I/O operation. Word 0 of the PIOT is set to one of the following values (orders) for the required action:

Operation	Hex Value
Read	0 0 3 C
Write	0 1 3 C
Backspace	0 2 3 C
Rewind	0 3 3 C
Erase	0 5 3 C

The final 8 bits of the PIOT word specify the interrupt mask. For the cassette, interrupt mask 3 C permits the following four interrupt bits to pass:

Start issued when not ready
End of record
Attention
Error

3.2.18.2 Cassette Adapter to Multiplexer Interface. The cassette adapter receives three timing signals directly from the backplane (67 ms, 2 ms, and 64.1 μs), and a clock signal from the multiplexer (MUX CLOCK). The three timing signals are used by a master counter circuit to provide various time-out signals to detect EOR and other conditions. The MUX clock gates data across the interface. The multiplexer interface control lines perform the standard functions except that byte count zero is used to stop write or erase, and address lines 14 and 15 are used to address the four cassette drives when status information is requested. Normal operation of the four cassettes is under the control of bits 0 and 1 of the order code. This allows the processor to request status information on a different tape drive from the one that is currently in operation.

3.2.18.3 Cassette Adapter to Cassette Drive Interface. Ten lines are sent to each cassette drive. Two of the ten (Flux 0 and Flux 1) contain data to be recorded on the tape. These are sent to all drives. (All inactive tape drives stop in the EOR gap on the tape.)

The other eight lines are separate signal lines to the tape drives. They carry data from the tape, control tape motion, and report status. Forward motion of the tape is controlled by one line; reverse motion is controlled by another. A clock track on the tape and a speed control line to the tape drive control tape motion. A data line carries the read data from the tape drive to the adapter.

Other signal lines include write permit (telling the adapter the status of the write permit tabs); cassette loaded (indicating that a tape is on the tape drive); and end of tape. This signal indicates that the tape has reached the end of its travel and all motion has stopped. The end of tape signal also signifies a beginning of tape condition, depending on the direction of tape travel.

There are two types of cassette drives that differ mainly in head configuration and drive voltages. Drive 594968 requires ±5 vdc; drive 594132 requires -5 vdc and +7 vdc. Also, the two drives require different interrecord gap timing. Jumpers on the model C adapter are used to set the voltages and adjust the interrecord gap timing for the particular drive used. See Figure 2-11 for the connections.

3.2.19 Disc Controller/Adapter Operation

The disc controller/adapter interfaces disc drive units with the PTS-100 processing system. It is composed of two boards — disc controller and disc adapter — with two interconnecting cables (Figure 3-66). The disc controller board is installed in the processor cabinet and the disc adapter board is installed in the disc drive cabinet. The interconnecting cables attach to the rear of the boards.

The disc adapter interfaces with Diablo series 31 and 33 disc drives. Other types of drives require a new disc adapter, as well as changes to the microprogram stored in the disc controller ROM.

The disc controller can drive up to eight series 31 disc drives and up to four series 33 double drives. The controller provides four basic functions: control over disc drive motion, conversion of parallel data from the processor to serial data for the disc and vice versa, synchronizing data and control signals from the disc clock to the controller clock, and control between the asynchronous operations of the disc and the processor. The disc adapter

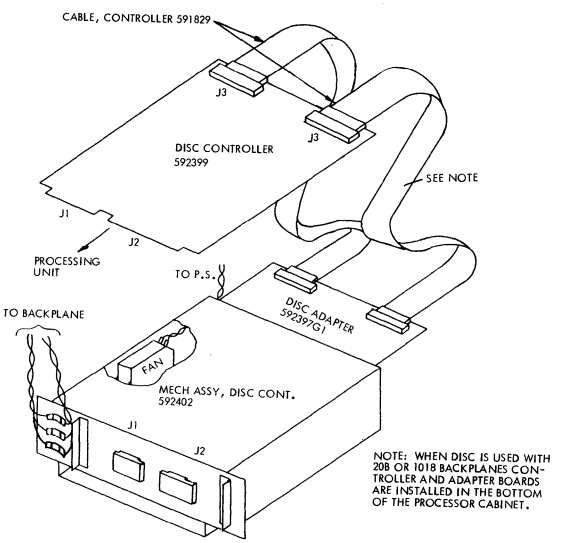


Figure 3-66. Disc Controller

converts address information into appropriate signals on four sets of address lines (unit, head, track, and sector), provides necessary timing control and compare functions, and provides for the interchange of data and status information with the disc.

Refer to Chapter 2 for controller interrupt patching.

3.2.19.1 Disc Adapter Circuit Description. The disc adapter interfaces the disc drive with the control circuitry located on the disc controller board. With the exception of unit (or disc drive) select, all address information is received from the disc controller over a serial data link, which is also used to carry data to be written on the disc. The address information is identified as such and routed to the appropriate address registers through separate control lines. Figure 3-67 is a functional block diagram of the disc adapter.

Sector address (defining one of twenty sectors around the disc) is stored in a 5 bit sector address register. Sector information is available on a time-multiplex basis only, since the disc must be in the correct physical position for the selected sector. To determine the position of the disc, the stored address is constantly compared to the sector address information coming from the disc. When an address match occurs, this information is sent back

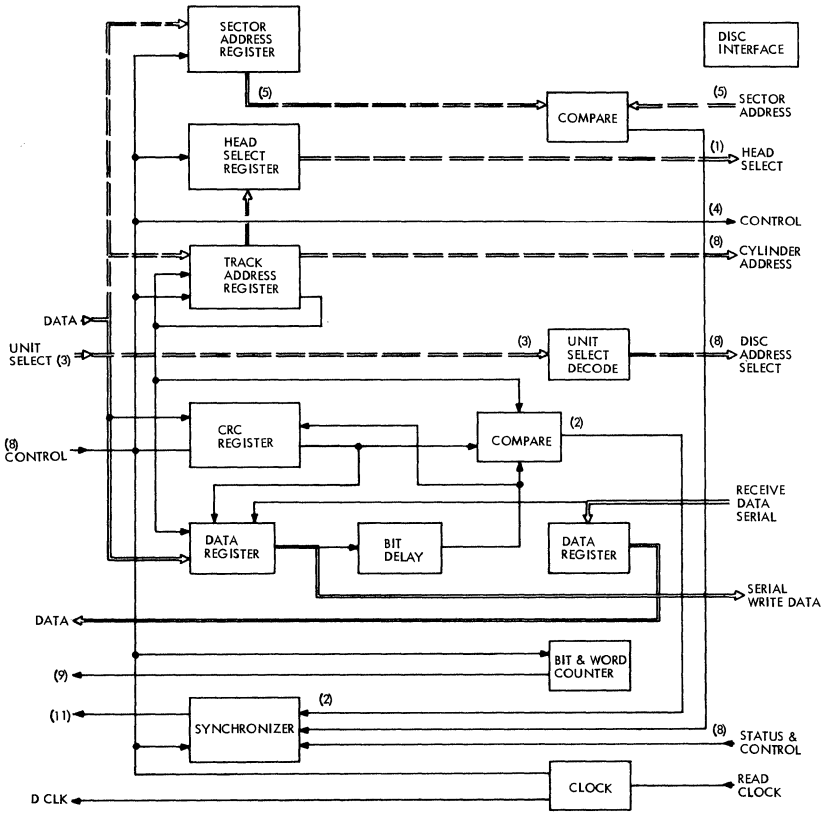


Figure 3-67. Disc Adapter, Block Diagram

to the logic control circuitry on the disc controller board and appropriate information is then either read onto or off of the disc. It should be noted that an address match is not absolutely required to read or write. Under control of the microprogram in the ROM, the controller may decide to ignore address match information. (For example, this might be done when information spills over into a second sector, or when new sector addresses are to be written.)

The track address register stores 9 bits of address information. One of these bits is sent to the head select register where it is used to select the appropriate head, and therefore the appropriate side of the disc. The other 8 track address register bits are sent to the disc drive as cylinder address bits. They are used to control the physical placement of the head along the disc radius, thus selecting the recording area to be used. There are 203 areas, or cylinders, on these discs. During read and write operations, the selected track address is written onto or read from the disc as the first word after the sync byte.

Three bits of unit select address are received from the disc controller over three separate lines. These bits are stored in the unit select register within the disc controller, and therefore the unit select address lines stay true during the entire time that a disc is selected. The disc adapter takes these three signal lines and decodes them so that the appropriate line (out of eight) is kept energized, thus selecting the appropriate disc drive. Until the disc is ready to accept commands, the status line READY from the disc stays false. When this line goes true, it indicates that the drive is ready to seek, read, or write.

There are twenty sector marks spaced around the disc, and one index mark located between sector marks 19 and 0. The index mark defines sector position 0, since the next sector mark occurring after an index mark is sector 0. The sector marks are counted by circuitry in the disc drive to send the current sector address back to the adapter.

Data to be written on the disc is received over the serial data line between the disc controller and the disc adapter. It is then stored in a data register in the adapter, and subsequently written on the disc with the appropriate control lines. The purpose of the data register in the disc adapter is to match the timing of the disc with the timing of the controller. Data is written on the disc under control of the write clock, which is not always in precise synchronism with the 320 ns clock in the controller.

Serial data read from the disc is loaded into a second data register, for a similar synchronizing function, prior to its being sent to the disc controller.

In addition to the address, data, and control information discussed above, there are additional interface signals between the adapter and the disc drive, and between the adapter and the disc controller. Table 3-16 lists the entire interface with the disc drives. Eighteen lines are used for address, three lines for data and clock (read data, write data and clock, read clock), and twelve control and status lines. Four of these lines are control lines to the disc drive (write gate, read gate, restore, and address strobe), four are status signals from the disc drive (ready, file ready, address acknowledge, and seek incomplete),and four are control signals from the disc (sector mark, index mark, write check, and logical address interlock). All twelve control and status lines are also sent back to the disc controller.

Another function performed by the adapter is to compare CRC. Each file of data written on the disc has a cyclic redundancy code (CRC) written as the last bit of data to provide a built in method of determining whether certain types of errors have occurred. During reading of data, the data is examined

and a new CRC is computed from this data by circuitry located on the controller board. This new CRC is compared to the CRC that was recorded on the disc in compare circuits located on the adapter board. If the CRC signals match, the data is assumed to be good. If they do not match, a warning is sent to the computer that some or all of the data may be faulty.

Table 3-16. Disc Drive Interface Signals

Sector Address	0	Read Data
	1	Write Data & Clock
	2	Read Clock
	3	
	4	Control Out
Head Select		write gate
		read gate
Track (cylinder)	0	restore
Address	1	Strobe
	2	
	3	Control & Status In
	4	File ready
	5	Ready to seek, read, write
	6	Address Acknowledge
	7	Seek Incomplete
		Sector Mark
Unit Select	1,5	Index Mark
	2,6	Write Check
	3,7	Logical Address Interlock
	4,8	

The adapter uses a synchronizer that adjusts the timing of various signals to account for differences in the clocks employed. The basic clock on the disc is written under control of the write oscillator. This is read off as the Read clock, and minor errors in clock timing or phase will occur due to minor changes in disc speed. The information gated into the synchronizer is under control of the read, or DS, clock. Information gated out of the synchronizer is under control of the S clock. The S clock is a 320 ns clock generated in the controller and derived from the I/O system clock (160 ns). An independent 320 ns clock is generated to provide the write clock signal. A third clock signal is also found across the disc controller/adapter interface. This is the SDS clock. This clock is simply the DS clock from the controller returned to it. Since the two boards are physically separated, there are some phase differences between the D (or DS) clock generated in the adapter, and the SDS clock received from the controller. These minor phase differences are important for certain functions within the adapter.

3.2.19.2 Adapter - Disc Timing. Information is written on the disc in the format shown in Figure 3-68. A preamble is written containing 31 bytes of zeros (15-1/2 words), followed by a one byte sync signal. This is followed by one word specifying the track address, 160 data words, a CRC check word, and a postamble of all zeros (the remaining 17 words). Each track starts in

coincidence with the trailing edge of the sector pulse. During write operations, a clock is written on the disc in addition to the data. During read operations, this clock is read off and becomes the DS clock.

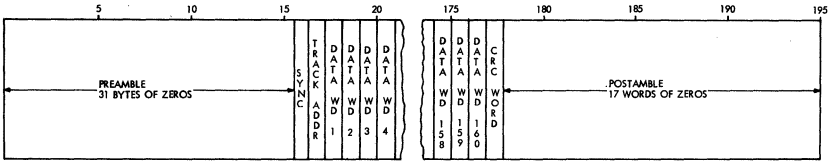


Figure 3-68. Disc Data Format

Data is written on the disc in serial fashion, with each bit written every 640 ns. Therefore, a byte of data (8 bits) is written in 5.12 μs, and a word (16 bits) every 10.24 μs. Since new words are produced about every 10 μs during read, or are required about every 10 μs during write, provision must be made in the disc controller for data buffering to ensure that the data which travels in bursts over the DMA bus from the processor is matched to the data from the disc. This is accomplished through a four word data buffer. Under some conditions of system overload or malfunction, this buffering may not be sufficient, and in that case data would be lost.

3.2.19.3 Disc Controller Circuit Description. The disc controller board, Figure 3-69, contains a 256 word ROM memory. This ROM memory contains the microprogram instructions to perform all the basic functions of the controller. The controller generates and checks the preamble, sync byte, CRC character, and postamble. In addition, it verifies track and cylinder address during write operations. The controller also interfaces with the processor, and accepts order codes from it.

To accomplish these functions, four 4 bit by 256 word ROMs are used. These ROMs store a microprogram for control of the disc controller and the disc adapter. This microprogram scans the status of all disc drives and controls the actions of the system as necessary with changing disc status. It also periodically scans the status of the processor initiated Do I/O instruction. Whenever the microprogram determines that the processor has requested a Do I/O, the microprogram branches to an appropriate microprogram subroutine to perform the requested order.

Seven basic orders can be performed by the controller: Write Data, Read Data, Seek, Compare Data, Write Address, Read Address, and Recalibrate. This order code is stored in the device packet as shown in Table 3-17. A

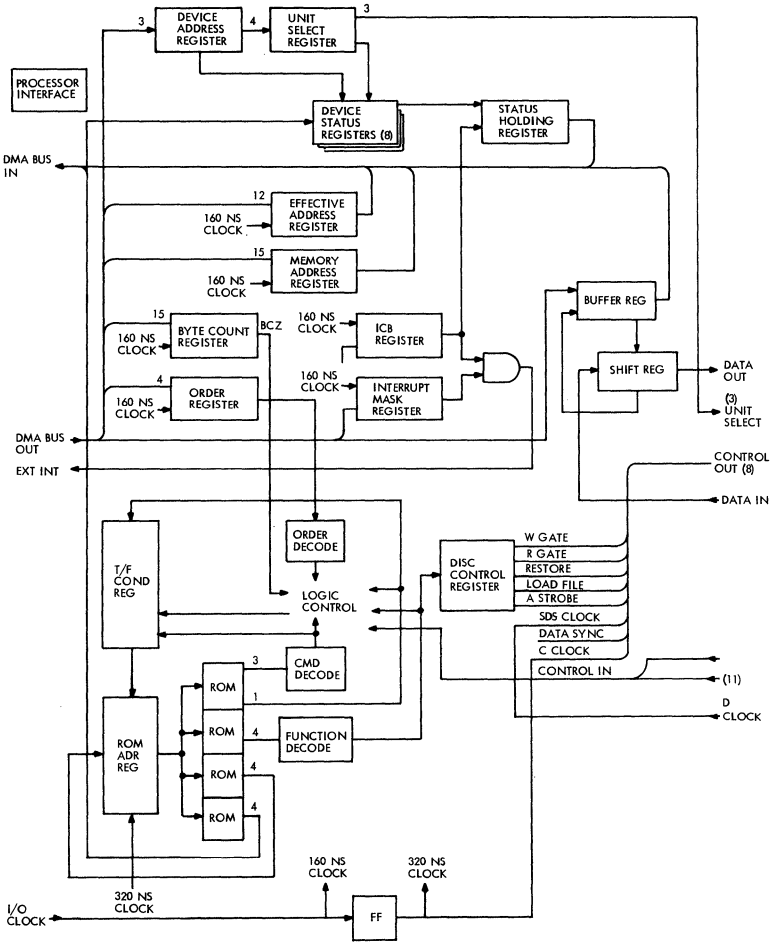


Figure 3-69. Disc Controller, Block Diagram

seek order causes the controller to logically connect to the selected drive only long enough to send the desired address to the drive. Then the controller is free to perform other tasks. When the drive completes its seek, and the controller is in the non-busy state, the seek complete indicator is set. The program is now free to perform write, read, or compare operations. Although a separate seek order is not essential (since each write, read, and compare starts with its own seek order), time is saved in the typical system by having the seek performed while the controller is busy doing other operations.

Table 3-17. Order Byte Codes

0	1	2	3	4	5	6	7	
X	X	X	X	X	0	0	1	Write Data
X	X	X	X	X	0	1	0	Read Data
X	X	X	X	X	0	1	1	Seek
X	X	X	X	X	1	0	0	Compare Data
X	X	X	X	X	1	0	1	Write Address
X	X	X	X	X	1	1	0	Read Address
X	X	X	X	X	1	1	1	Recalibrate

(X indicates don't care bits)

Write Data is the basic order for writing data on the disc. It requires that track addresses have been previously written. Write Address is used to format the drive, and to write the track address information. No data is written with this order. Read Data will read all data from a track, but will not read address information. In addition, Read Data will terminate under any error condition. Read Address will read the track address as well as all data recorded, and will not terminate under error conditions. It is primarily used for maintenance purposes.

Compare Data operates as both a read from disc, and a write from memory order. The data area of the disc is compared word by word with words stored in memory. A non-compare will terminate this order, as well as the existence of error conditions, or the presence of BCZ.

Recalibrate is used to clear the disc whenever a seek incomplete indicator has been set, or after certain types of format errors. This order causes the disc to seek to a Cylinder 0 Track 0 position.

The controller contains a ROM with stored program that controls all operations of the disc, disc adapter, and disc controller. Various built in error conditions cause the existing order to be terminated. These include incorrect address, track not written, incorrect sector, sector location hardware malfunction, and end of track.

The ROM instruction word format is illustrated in Figure 3-70. The first three bits are an OP code defining the type of operation to be performed. OP code 1_8 contains the memory commands, with bit 3 of the instruction word indicating whether it is an input or an output from memory operation. Bits 4 through 7 are function code bits, further defining the type of operation to be performed. Bits 8 through 15 specify the address of the data word being described.

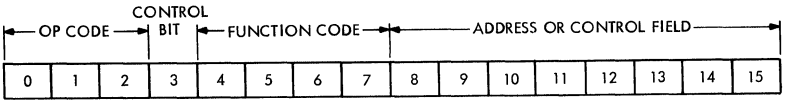


Figure 3-70. ROM Word Format

OP Code 2_8 is a Test True command, and OP code 3_8 is a Test False (TF) command. These commands cause a conditional jump to the address specified in bits 8 through 15. The condition being tested for is defined in bits 3 through 7.

OP Code 4_8 is the unconditional jump command. This command performs certain functions prior to the jump instruction. The functions performed are defined by bits 4 through 7. After the function is performed, the ROM jumps to the instruction location specified in address locations 8 through 15.

OP Code 5_8 is a status command. Bits 4 through 7 define the affected status, and bits 8 and 9 of the address field indicate whether the attention bit and/or the summary error bit in the status register should also be set. Bit 3 is used as a control bit. When set, all other bits are ignored, and the status information is read out.

OP codes 0_8, 6_8, and 7_8 are spares.

The controller includes a four word buffer register and a parallel/serial conversion register that work together to accept the data from the PTS-100 DMA bus to write on the disc, or supply the data to the DMA bus from the disc. The four words of buffering ensure that no words will be lost during the transfer, since access to the bus may be delayed due to higher priority users. Within four word times (40.96 μs) access to the bus is guaranteed. Since data is transferred over the DMA bus in 16 bit parallel words, and stored on the disc serially, a parallel/serial shift register is used for data conversion.

The controller also contains an ICB register and eight status registers. In addition, there is an interrupt mask register to hold interrupt validity data, and a status holding register that accepts data from either the ICB register

or one of the device status registers prior to the transmission of the status on the DMA bus. The ICB register uses its first 8 bits to indicate which of the disc drives requires attention, and the second 8 bits to indicate the type of attention required. The status registers, one for each of the disc drives, indicate the operational status of each of the drives. Tables 3-18 and 3-19 illustrate the format of data within these registers.

Table 3-18. ICB Register Format

Bit 0	Drive 0 Attention
Bit 1	Drive 1 Attention
Bit 2	Drive 2 Attention
Bit 3	Drive 3 Attention
Bit 4	Drive 4 Attention
Bit 5	Drive 5 Attention
Bit 6	Drive 6 Attention
Bit 7	Drive 7 Attention
Bit 8	Attention - Controller Ready
Bit 9	Spare - Zero
Bit 10	Start I/O While Busy
Bit 11	Seek Complete
Bit 12	Byte Count Zero
Bit 13	End of Track
Bit 14	Non-Compare
Bit 15	Summary Error

Table 3-19. Status Register Format

Bit 0	Ready
Bit 1	Busy
Bit 2	Operator Intervention Required
Bit 3	Seek Incomplete
Bit 4	Format Error
Bit 5	CRC Error
Bit 6	Rate Error
Bit 7	Spare
Bit 8	Spare
Bit 9	Spare
Bit 10	Start I/O While Busy
Bit 11	Seek Complete
Bit 12	Byte Count Zero
Bit 13	End of Track
Bit 14	Non-Compare
Bit 15	Summary Error

3.2.19.4 Disc Controller - Processor Interface. The disc controller starts operations when the PTS processor places a Do I/O start command on the input/output bus (with the disc controller address). This is followed by a word containing the EA of the PIOT table and the address of the selected drive (unit). If the disc controller, adapter, and selected drive are not busy, the disc controller requests the PIOT information from memory by using the effective address which had just been sent to it. If the controller, adapter, or drive is busy or not ready, the start I/O command will not be performed, and the start I/O while busy flag will be set.

The controller requests the first word of the PIOT table by sending a function code (output word) to the processor, as well as the address of this word (EA). The processor responds by sending the first word of the PIOT table. This word, containing the order code (previously defined in Table 3-17) and the interrupt mask, is stored in the appropriate registers in the disc controller. These steps are then repeated for the remaining words of the PIOT table. Figure 3-71 illustrates the format of the PIOT table.

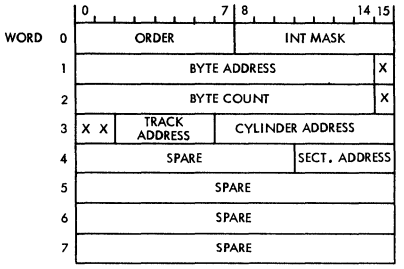


Figure 3-71. Disc Controller PIOT Table

Other commands that are sent to the controller include the stop I/O command, a reset command, and four read I/O commands. A stop I/O command terminates immediately all read and compare data orders. A write data order will terminate at the end of the current disc sector, after the remainder of the sector has been filled with zeros and the correct CRC.

Reset causes the controller to reset immediately. If it was in a write order mode, an incorrect CRC might be written in that sector.

The four read I/O commands that are responded to are numbered 0 through 3. Read I/O command 0 causes the addressed device's status register to be read back to the processor and reset. Read I/O command 1 performs the same read without the reset. Read I/O command 2 reads and resets the ICB register, and command 3 reads this register without the reset.

3.2.20 Channel Interface Controller

The channel interface controller (CIC) permits the PTS-100 to communicate with an IBM 360/370 computer. It translates the PTS-100 and IBM 360/370 languages so that the two systems can communicate and transfer data to one another. The CIC attaches to the PTS-100 I/O bus and the 360/370 selector or multiplexer channel I/O cables. The CIC consists of two plug-in circuit boards: driver receiver, and register (see Figure 3-72). The driver receiver board contains the 360/370 interface circuits, and the register board contains the PTS-100 interface circuits. The register board is mounted in any J1 slot below the processor not dedicated to monitor controllers in the PTS-100 cabinet (Model 1020B), and the driver receiver board is mounted in a separate chassis fastened underneath the cabinet rack. When the CIC is used with a Model 1015 the separate chassis is mounted in an external cabinet.

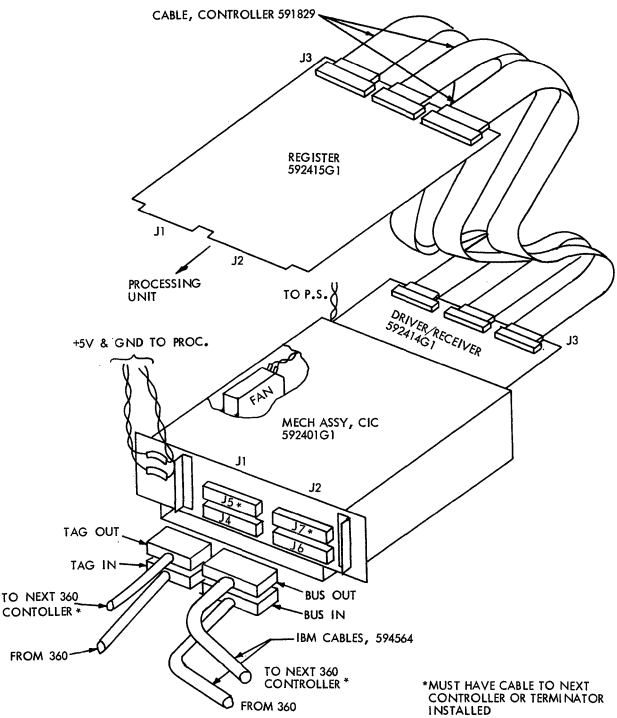


Figure 3-72. Channel Interface Controller

The CIC is transparent to data and 360 commands, except Test I/O, Halt, Selective Reset, System Reset, and Sense, although it can translate data by hardware table lookup. Both the PTS-100 and the IBM 360/370 programs can initiate communications. The CIC operations are controlled by an internal microprogram that is stored in a read only memory (ROM). The microprogram changes for each different CIC application. The 2848 version is described here. The 3270 version is much the same but it uses a different I/O device packet and recognizes different 360/370 commands. The CIC contains an OFF LINE/ON LINE switch that disables the CIC drivers and receivers to and from the 360/370. The OFF LINE position is used for CIC testing.

NOTE

The CIC driver/receiver board must not be unplugged when the 360/370 is connected and operating or the 360/370 channel will be disabled.

3.2.20.1 Interfaces. Refer to Section 1 of this chapter for the CIC - PTS-100 interface. The CIC - 360/370 interface is described below and shown in Figure 3-73. The timing of the basic signals between the CIC and 360/370 for the data and command transfer sequences is shown in Figure 3-74. Refer to Chapter 2 for interface cabling and CIC patches.

a. In Tags

These lines carry signals that identify to the 360/370 the nature of the EBCDIC characters placed on the bus in lines by the CIC.

1. Address In - identifies the character as an address.

2. Status In - identifies the character as status information. The status byte has the following format:

Bit	Status
P	Parity
O	Attention
1	Status Modifier
2	Control Unit End
3	Busy
4	Channel End
5	Device End
6	Unit Check
7	Unit Exception

3. Service In - sent to the 360/370 whenever the CIC wants to transmit or receive a character of information on the Bus In or Bus Out lines.

b. Out Tags

The lines identify the nature of the character placed on the Bus Out lines.

1. Address Out - normally identifies the character on the Bus Out as an I/O device address; however, for an interface disconnect sequence (Halt I/O) it causes the CIC to disconnect from the 360/370.

2. Command Out - this signal can be raised in reply to an Address In (proceed), Status In (status stacked) or Service In (end of record) from the CIC. During the command issue sequence it indicates that a command character is on the Bus Out line. During a control unit (CIC) initiated or data transfer sequence it indicates "proceed" to the CIC. The command character has the following format:

Bit	Test I/O	Read Backwards	Sense	Write	Read	Control
P	1	P	P	O	P	P
0	0	M	M	M	M	M
1	0	M	M	M	M	M
2	0	M	M	M	M	M
3	0	1	M	M	M	M
4	0	1	O	M	M	M
5	0	0	1	M	M	M
6	0	0	0	0	1	1
7	0	0	0	1	0	1

M - Modifier Bit; P - Parity Bit

1. Service Out - this signal is sent to the CIC in response to a Service In or Status In signal. It informs the CIC that the 360/370 has accepted the character from the CIC presently on the Bus In lines.

c. Bus In and Bus Out

Two groups of lines (8 + parity) that transfer information (EBCDIC) between the CIC and 360/370.

d. Scan Control Lines

Four lines that enable the 360/370 to establish initial communication with the CIC.

1. Select Out and Select In lines - these signals provide a scan loop that allows the 360/370 to interrogate the CIC during the initial selection and control unit initiated sequences. The Select In (outbound) is the return path for the Select In (inbound) line. The Select In lines are normally open. They are shorted when the CIC is not able to enter into a transaction with the 360/370. The Select Out lines are always shorted together.

2. Hold Out - this signal enables the Select Out signal.

3. Request In - the CIC sends this signal to the 360/370 when it has a service requirement. The 360/370 responds with Select Out.

e. Interlock Lines

These lines are used to interlock the CIC and 360/370.

1. Operational Out - this signal enables the CIC to communicate with the 360/370. It gates all the I/O interface signals and provides a reset.

2. Operational In - the CIC sends and holds up this signal to the 360/370 when it has been selected during an initial selection and control unit initiated sequence.

f. Special Control Lines

1. Clock - sent to the CIC to inform it that the 360/370 channel is not active.

2. Meter Out - this signal is normally sent to a device to start its clock. In the CIC it is not used.

3. Metering In - normally this signal is the device's replay to Meter Out when its meter is running. However, in the CIC it is generated by Operational In.

4. Suppress Out - this signal is sent from the 360/370 to the CIC to inhibit data transfer, suppress status, indicate chaining, and during selective reset sequences.

3.2.20.2 Status Bits and ICB. The CIC sends status information to both the PTS-100 and the 360/370. It also sends interrupt bits to the PTS-100. The status and interrupt bits and their functions are listed below.

a. PTS-100 ICB Bits (CIC to PTS-100)

Bit	Name	Function
0	Invalid Command	This bit is set when the command received from the 360 was incorrect or had a parity error in which case the parity bit is also set.
1	Command While Busy	A command was received for another device while the CIC was busy with this device.
2	Parity Error	A parity error was detected in a data or command byte.
3	Halt I/O	All operations to that device are terminated and the Do register for that device is cleared.
4	Selective Reset	Same as Halt I/O.
5	End of Record	The 360/370 has stopped data transfer or the Send Status ordered has been completed.

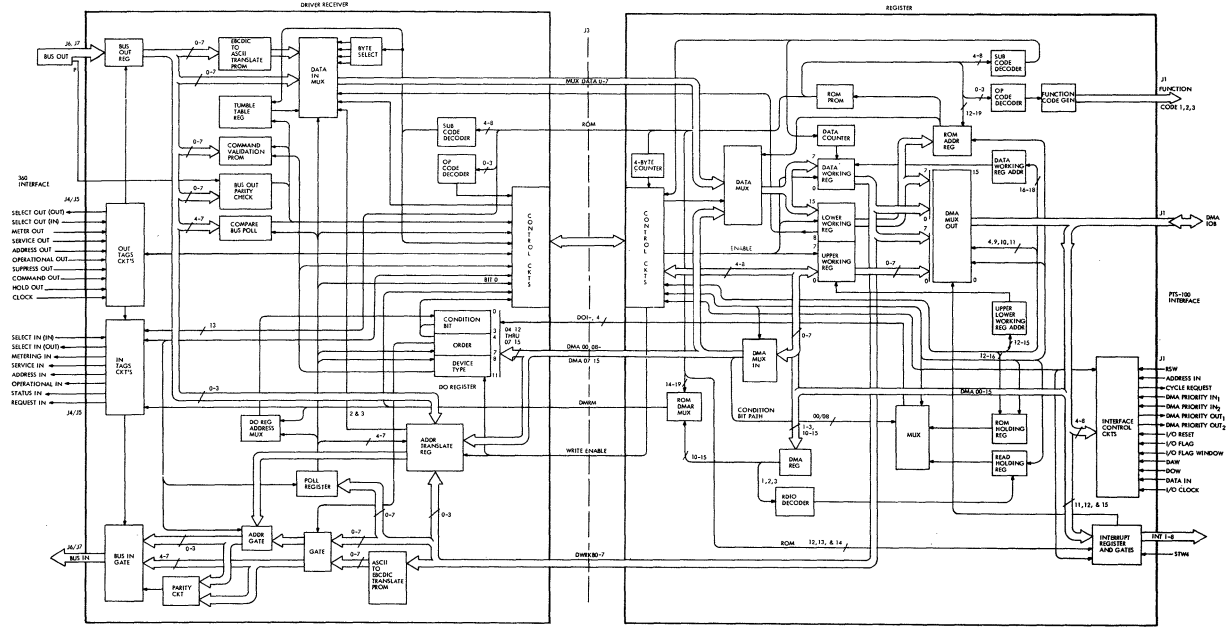


Figure 3-73. CIC Simplified Circuit Block Diagram

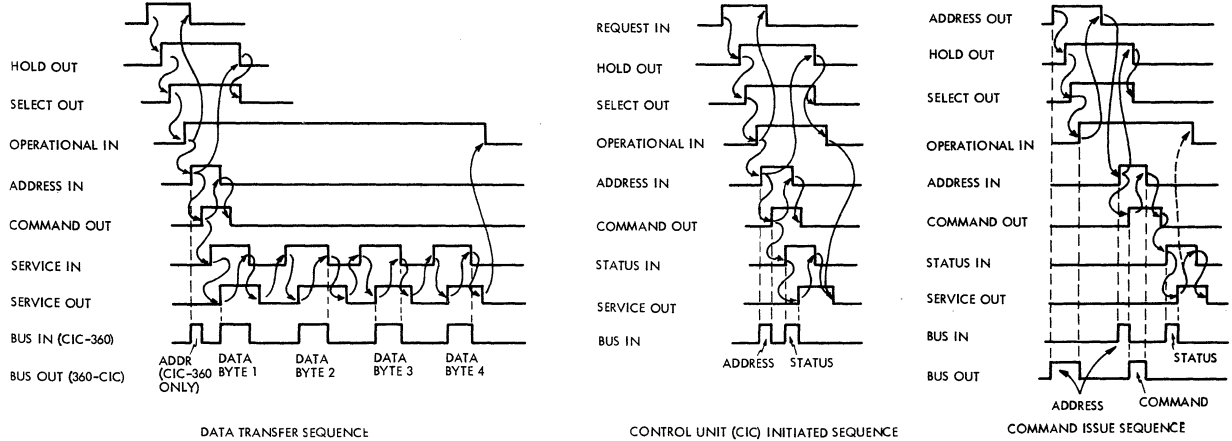


Figure 3-74. CIC - 360/370 Timing

Bit	Name	Function
6	Byte Count Zero	The byte count stored in the device packet has reached 0.
7	Command While Off Line	Indicates that a 360/370 command was issued to an off line PTS-100 device.

b. PTS-100 ICB Bits (CIC to PTS-100)

Bit	Name	Function
0	Ready	Indicates to the PTS-100 that the 360/370 is connected (Operational Out is raised) and the CIC is not being initialized.
1	Busy	When this bit is raised to the PTS-100 it indicates that the CIC is performing the initialization sequence.
11	Initialization Complete	Informs the PTS-100 that the initialization has been completed.
12	Tumble Table Interrupt	Sent to the PTS-100 to inform the program that an entry in the tumble table has been made.
15	System Reset	Sent to the PTS-100 to inform the program that a system reset has been received from the 360/370. (Program must then perform another initialization sequence.)

c. 360/370 Status Bits (CIC to 360/370)

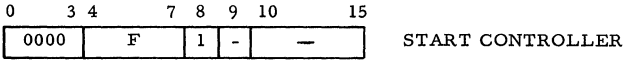
Bit	Name	Function
0	Attention	This bit is generated when the enter key is depressed on one of the PTS-100 displays that is not presently communicating with the 360/370.
1	Status Modifier	The status modifier bit is sent to the 360/370 with the busy status bit (3) when initial status is stacked and the 360/370 wants to communicate with an I/O device other than the one for which the status is stacked.
2	Control Unit End	This bit is sent to the 360/370 in the initial status byte when a status modifier bit was previously sent. This bit indicates to the 360/370 that the CIC is no longer busy.
3	Busy	This bit is sent to the 360/370 to indicate that the addressed I/O device is busy or it is sent with the status modifier, bit 1.
4	Channel End	This is sent to the 360/370 to inform it that the CIC has completed the transfer (360 to/from CIC) of data or control information.

Bit	Name	Function
5	Device End	This bit is sent to the 360/370 to inform it that the CIC has completed transfer of data or control information to the addressed I/O device, except for printers (2260 applications) in which case this bit is sent before all of the data has been sent to the I/O device. If the 360/370 tries to communicate with the printer before the operation is complete the busy bit is sent; then, after the printer has completed printing, this bit is again sent.
6	Unit Check	This bit is sent to the 360/370 with initial status when a command is sent to the CIC for an off-line I/O device, the command had a parity error, or the command is invalid for the I/O device. The bit is also sent with Channel End and Device End to indicate that a parity error was detected in the data transferred.

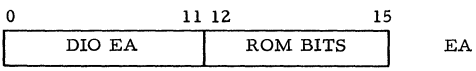
3.2.20.3 Initialization PTS-100 - CIC Sequence (Figure 3-73).

a. Loading the Start Controller Table

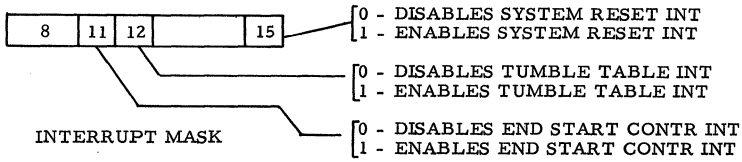
The CIC is started when the PTS-100 processor places a DIO start command with the CIC address on the Input Output Bus (IOB).



Bits 4 through 8 are applied to the interface circuits where bit 8 sets a start controller flip-flop when bits 4 through 7 contain the CIC address (F) and bit 8 is set. The control circuits gate the following EA from the processor directly into address C (hex) of the upper working register (bits 0 through 7) and through the DMA Mux In and Data Mux into address C of the lower working register (bits 8 through 15) (bits 13 through 15 of the EA must be zeros). The upper, lower, and data working registers are each 8 bit, 16 word registers. The word locations are addressed by the upper, lower, and data working register address circuits. All CIC operations are under microprogram control. When the CIC detects that the start controller flip-flop is set the microprogram initiates the start controller sequence. Bits 0 through 11 of the upper and lower working registers are then sent through the DMA Mux Out to the processor IOB. Bits 12 through 15 of the word are supplied by microprogram ROM bits 4, 9, 10 and 11 through the DMA Mux Out.



A function code (Output Word) is also sent to the processor. It causes the processor to output the word located at the memory address (EA) on the bus. This is the first word (Interrupt Mask) of the start controller packet (Figure 3-75). Bits 11, 12, and 15 of the interrupt mask are received and put into an interrupt mask register in the interrupt register and gate circuits.



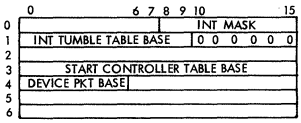


Figure 3-75. Start Controller Packet

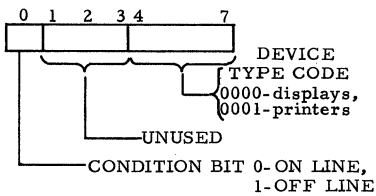
Next the CIC changes the portion of the memory address represented by the ROM bits and sends this address and another output word function code to the processor, which responds by sending the second word (interrupt tumble table base) of the start controller packet. This word is put into the upper and lower working registers at address 8 (hex). The CIC brings in the next two words of the start controller packet in the same way. It puts them into the upper and lower working registers with the start controller table base put into location A and the device packet base put into location 4. At this point the microprogram clears both the tumble table counter and the poll register. When this is accomplished the CIC puts the start controller table base from the upper and lower working registers onto the IOB and sends an output word +1 function code to the processor. The processor responds by sending the 80 byte start controller table through the CIC DMA mux in circuit to the address translate register and the Do register. The first 16 bytes (address translate table) are put into the 8 bit, 16 word address translate register.

ADDRESS TRANSLATE TABLE			
		ADDR TRANS REG	
360 ADDRESS	PTS-100 ADDR	PTS ADDR 0123	360 ADDR 0123
0	0	1000	0000
1	1	1000	0000
2	2 =	1000	0011
3 =	3	0010	0000
4		1000	0000
-			
-			
-			
F		1000	0000

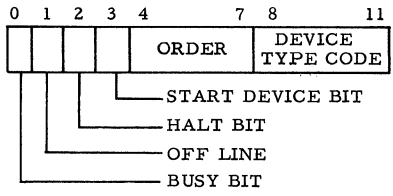
EXAMPLE:
360 ADDRESS-3
PTS-100 ADDRESS-2

The next 64 bytes are put into the device type and condition bit portions of the 12 bit, 64 word Do register. The device type codes are put into bits 8 through 11 and the condition bit is put into bit 1 (see below).

Format of Bytes to Do Register



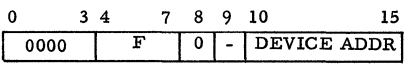
Format of Bytes in Do Register



The path of the condition bit is from the DMA mux in through the holding register mux to the Do register. The poll register increments the address of the address translate register and the device type portion of the Do register as the bytes are loaded. It also increments the address of the condition bit portion to the Do register through the Do register address mux. The order portion of the Do register is then cleared, the Initialization Complete ICB bit is set in the interrupt register and gates circuit to inform the PTS that the CIC is initialized, and a relay is set in the In Tags circuit to initialize the Select In (in/out) circuits to the 360/370. The 360/370 is now able to communicate with the PTS-100 I/O devices.

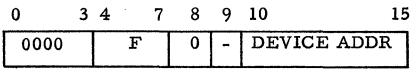
b. Loading the Start Device Packet Order

The start I/O device packets in PTS memory (one for each order for each I/O device) are not used until either the 360/370 or a PTS I/O device wants service. When the service is requested by an I/O device the processor issues an RIO Test and Set Busy command to the CIC.



RIO Test & Set Busy

The CIC DMA register receives the RIO command. Bits 10 through 15 (the device address) are applied through the ROM DMAR mux to the Do register address mux, and bits 1, 2, and 3 are decoded in the RDIO decoder. Bit 0 of the word at the device address in the Do register is sent to the processor via the control circuits, interrupt register and gates circuit, and the DMA mux out. When bit 0 is a zero the associated I/O device is not busy. (If it is a 1 the device is busy.) When Bit 0 is found to be zero it is set to 1 (busy) by the read holding register through the holding register mux. The processor now issues a DIO start device command to the CIC, which sets condition bit 3 of the associated word in the Do register.



DIO START DEVICE

Do register addressing is through the DMA register, ROM DMAR mux and Do register address mux. The setting of bit 3 is through the RDIO decoder, read holding register, and holding register mux, as before. When a condition bit is set, the whole condition bit byte is read out by the control circuits and written back into the Do register via the ROM holding register and holding register mux.

When the poll register, which normally cycles through all the Do register addresses (polls), cycles to the address with condition bit 3 set it stops and initiates the start device routine. The microprogram loads the poll address (6 bits) into the lower working register through the data in mux and the data mux. Here the poll address is combined with the device packet base previously put in from the start controller packet. The device packet base and the poll address are sent to the DMA mux out where they are combined with ROM bits 4, 9, 10, and 11 to form a word that points to the order in the start device packet for that particular I/O device (Figure 3-76). The composite address word is sent to the processor along with an Output Word function code. The processor sends the order byte (bits 4 through 7) from the device packet.

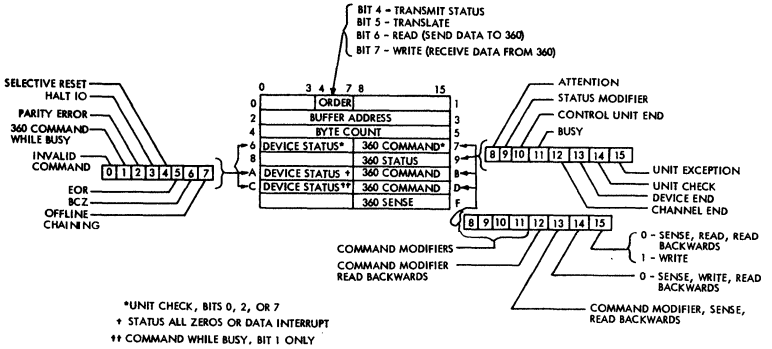
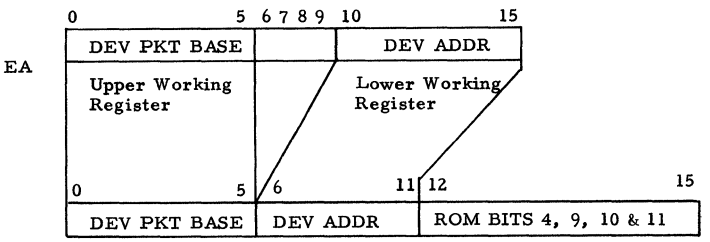


Figure 3-76. I/O Device Packet

In this case the order will be Transmit Status (1000), since an I/O device wanted service. The order is sent through the DMA mux in to the order portion of the Do register. It is checked by the CIC control circuits, which recognize it as a transmit status order (refer to Section of this chapter for the other orders), and therefore initiate action to bring in the status byte from the device packet (byte 9). The microprogram again loads the poll address into the lower working register where it is combined with the device packet base and sent to the data mux. Here, as before, it is combined with ROM bits 4, 9, 10, and 11 put on the IOB and sent to the processor along with an output word function code. This time this address points to the 360 status byte, which is polled and sent to the CIC where it is put into the data working register address E (via the DMA mux in and the data mux). In this case the status byte is Attention.



3.2.20.4 Control Unit Initiated CIC-360 Sequence (Figure 3-73). Once the status byte is in the data working register the control circuits raise Request In to the 360/370, which responds with SELECT OUT. When the SELECT OUT is

detected it sets OPERATIONAL IN. When the microprogram detects OPERATIONAL IN it enables the address gate in the Bus In circuits. It also loads the poll (device address) into the data (address D) and lower working (address 6) registers (through data in and data muxes). The device address is then sent from the data working register to the address translate register (bits 2 and 3) and to Bus In (bits 4 through 7). The address translate register translates the address to a 360 address and applies it through the address gate to bits 0 through 3 of Bus In. Then the microprogram raises ADDRESS IN to the 360/370, which responds by reading the address and raising COMMAND OUT. COMMAND OUT causes the CIC to drop ADDRESS IN and disable the Bus In address gating circuits. At this point either data or status can be transferred. The status transfer is described in "a" below, the send data to 360/370 is described in "b", and receive data from 360/370 is described in "c."

a. Send Status Sequence

When status is being transferred, the status byte from the data working register is sent to the Bus In circuits where it is gated onto Bus In when the microprogram raises STATUS IN to the 360/370. The 360/370 accepts the status byte and raises SERVICE OUT (if the 360/370 stacks status it raises COMMAND OUT and the CIC continues to try to send status until the 360/370 accepts it). In this case the status sent to the 360/370 was "attention" so on receipt of SERVICE OUT the microprogram loads condition bits 0 through 3 from the Do register into the ROM holding register (via the control circuits). Here condition bit 0 is reset and bits 1, 2, and 3 are written back into the condition bit portion of the Do register, via the holding register mux. Now OPERATIONAL IN is reset and the microprogram goes to a data interrupt sequence.

b. Send Data Sequence

When data is being transferred to the 360/370 the data counter is reset to zero. Then if the 360/370 does not raise SUPPRESS OUT the byte of data in the data working register addressed by the data counter is gated into the Bus In circuits. If the translate bit in the order (from the PTS-100) was set, the data byte is first routed through the ASCII to EBCDIC Translate PROM where the ASCII coded data byte is converted to EBCDIC. The CIC microprogram raises SERVICE IN to the 360/370 and puts the data byte on Bus In. The 360/370 replies with SERVICE OUT, which resets SERVICE IN. (If the 360/370 does not want to accept the data it raises COMMAND OUT, which causes the CIC to set the EOR bit in the control circuits, reset OPERATIONAL IN and SERVICE IN, and go into a data interrupt sequence [discussed in Section 3.2.20.5].) Each time a data byte is transferred from the data working

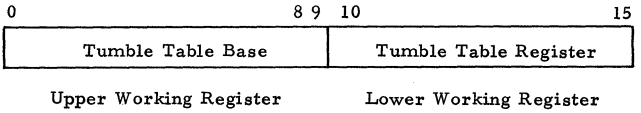
register to the 360/370 the CIC microprogram sends an output word +1 function code to the PTS-100 processor along with the byte count EA (stored in the upper and lower registers) to increment the byte count. Also as each data byte is transferred when SERVICE OUT falls the 4-byte counter is decremented and the data counter is incremented. The data byte transfers continue until a byte count zero is received or until the 4-byte counter reaches zero. When byte count zero is received the CIC resets OPERATIONAL IN and performs a data interrupt sequence (Section 3.2.20.5). When the 4-byte counter reaches zero the CIC resets OPERATIONAL IN and cycles through the poll addresses. It services all other I/O devices requiring service until it again finds the read order in the Do register for this device, at which point it repeats this read data to 360/370 sequence except that it does not refetch the order.

c. Receive Data Sequence

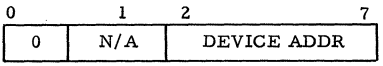
When data is being transferred from the 360/370 to the CIC the data counter is reset to zero. Then if the 360/370 does not raise SUPPRESS OUT the CIC microprogram raises SERVICE IN to the 360/370, which puts the data byte on Bus Out. The 360/370 then raises SERVICE OUT, which resets SERVICE IN. (If the 360/370 does not want to send the data it raises COMMAND OUT, which causes the CIC to set the EOR bit in the control circuits, reset OPERATIONAL IN and SERVICE IN, and go into a data interrupt sequence.) When SERVICE OUT is raised the byte of data from Bus Out is transferred to the data working register addressed by the data counter. If the translate bit in the order (from the PTS-100) was set, the data byte is first routed through the EBCDIC to ASCII Translate PROM where the EBCDIC coded data byte is converted to ASCII. Each time the 360/370 raises SERVICE OUT and transfers a byte of data to the data working register the CIC microprogram sends an output word +1 function code to the PTS-100 processor along with the byte count EA (stored in the upper and lower registers) to increment the byte count. Also as each byte is transferred when SERVICE OUT falls the 4-byte counter is incremented and the data counter is incremented. The data byte transfers continue until a byte count zero is received or until the 4-byte counter reaches three. When byte count zero is received the CIC resets OPERATIONAL IN and performs a data interrupt sequence. When the 4-byte counter reaches three, the CIC resets OPERATIONAL IN, resets the data counter, and sends an output word +1 function code to the processor. This causes the processor to increment the buffer address and put it back into the packet. The CIC then sends an input byte function code to the processor, which responds by accepting and storing the first data byte from the CIC at the buffer address. The data byte transferred to the PTS-100 is stored in the data working register at the address set into the data counter. The data counter is incremented, the 4-byte counter is decremented, and the process is repeated four times, transferring four data bytes from the data working register, whereupon the 4-byte counter contains a count of zero. Then the CIC cycles through

the poll addresses. It services all other I/O devices requiring service until it again finds the write order in the Do register for this device. When it does it repeats this Write Data from 360/370 sequence except it does not refetch the order.

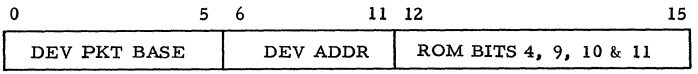
3.2.20.5 Data Interrupt CIC-PTS-100 Sequence (see Figure 3-73). The contents of the upper and lower working registers are sent out to the processor on the IOB (via DMA mux out). This is the tumble table address in memory where the device address will be stored.



The contents of the poll register (the device address) are loaded into the lower and data working registers via the data in and data muxes. The device address from the data working register is put on the IOB through the DMA mux out and sent to the processor along with an input byte function code.

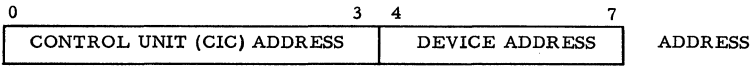


(A zero in bit 0 of the byte indicates a data interrupt rather than a 360/370 initiated interrupt.) The processor puts this byte in the tumble table in memory at the specified address. The microprogram then increments the CIC tumble table register and transfers its contents to the lower working register via the Data In and Data muxes. It also puts an EOR bit in the data working register and zeros the order in the Do register at the poll address. The device packet base and the device address from the upper and lower working registers are combined with ROM bits 4, 9, 10 and 11 and sent to the processor. This word points to byte A in the device packet.



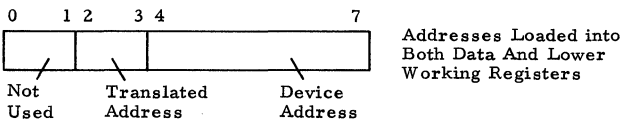
Next the status byte (EOR) from the data working register is sent to the processor where it is put into byte A of the packet. Then the microprogram sets a tumble table interrupt in the interrupt register circuit and returns to an idle condition.

3.2.20.6 360/370 Command Issue 360-CIC Sequence (see Figure 3-73). After "Attention" has been sent to the 360/370 during the initial selection sequence, the 360/370 requests service from the CIC by sending a command (read, write, etc.) and the CIC and device addresses. The operation of the CIC on receipt of the address and command is the same regardless of the command except for Sense and Test I/O. When the 360/370 puts the address on Bus Out it raises ADDRESS OUT, which gates bits 0-3 (CIC address) to the address translate register.



In the translate register the address is checked against the addresses stored in the address translate table. If the address compares to one stored in the table (if bit 0 is a zero it is a CIC address) the control circuit raises OPERATIONAL IN and blocks SELECT IN (SELECT IN [in] and SELECT IN [out] remain open circuited) to the 360/370. If the address is not in the table the control circuits short SELECT IN (in) to SELECT IN (out) to pass on the address.

When the address is a CIC address the CIC has 32 microseconds in which to interrupt the CIC microprogram, connect to the 360/370, and complete the 360/370 initiated sequence. When interrupted, the microprogram stores the contents of the ROM address register in the lower working register via the data mux. The program then loads the ROM starting address of the initial select program sequence into the ROM address register. The first instruction at the address is decoded by the Op code and Sub code decoders. It causes the address to be loaded into the lower and data working registers via the data in and data muxes. The translated address, bits 2 and 3 come from the address translate register. Bits 4-7 come from the Bus Out register where they were being held.



The microprogram advances and loads the contents of the poll register into the data and lower working registers. This saves the poll. Next the microprogram transfers the translated address from bits 0 through 3 of the data working register (DWRK 0-3) to the address translate register. Here the address is translated back into the original form and gated out through the address gate (ADDR GATE) to the Bus In circuits. At the same time the contents of the data working register is stored in the poll register.

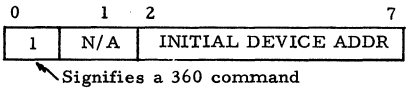
In response to OPERATIONAL IN the 360/370 lowers ADDRESS OUT when it is ready to communicate with the CIC. When this occurs the CIC raises ADDRESS IN and enables the Bus In gate so that the translated address is gated out to the 360/370. The 360/370 replies by putting a coded command (see Section 3.2.20.1b) on Bus Out and raising the COMMAND OUT TAG line. The CIC Bus Out parity check circuit checks the command for correct parity.

If a parity error is detected the parity check circuit sets a Unit Check Status bit in the control circuits. In any case the command is applied through the data in and data muxes and stored in the data working register. Then the microprogram resets ADDRESS IN and disables the address gate circuit. The command, which is still in the Bus Out register, is checked for validity by the command validation PROM circuit. The device type information from the Do register (addressed by the poll register) gates the PROM so that the command is checked against the valid commands stored in the applicable portions of the preprogrammed PROM. If the command is not the same as one of those stored in the PROM a unit check status bit is set in the control circuits. The microprogram next instructs the control circuits (through the Sub and Op code decoders) to check the condition bit of the addressed device in the Do register to see if the device is busy (bit 0) or off line (bit 1). Off line is not used with sense commands. If the command is valid and the device is busy a status bit is set in the control circuits. If the device is not busy the microprogram sets the busy bit (1) and resets the halt bit (2) in the ROM holding register and clears the order portion of the Do register. If the device is off line a unit check status bit is set in the control circuits. The status bits from the control circuits are then loaded into the data working register via the data in and data muxes.

The exception to this is when the command is Test I/O and the PTS-100 is trying to send status for this device to the 360/370, in which case the pending status in the device packet is loaded into the data working register instead of being held in the control circuits. After the Data Working Register is loaded its contents are applied to the Bus In circuits to the 360/370. When COMMAND OUT falls, STATUS IN is sent to the 360/370 and the status byte is gated through the Bus In gate onto Bus In. If the command is a Test I/O in response to STATUS IN, the 360/370 may raise COMMAND OUT causing the CIC microprogram to stack the status and perform a control unit initiated sequence, which again tries to send the status byte to the 360/370. If in response to STATUS IN the 360/370 raises SERVICE OUT, the CIC microprogram checks the device type in the Do register and when the device is a printer or display that is not busy the CIC goes into a command interrupt sequence. If the device is a display that is busy and the command is a Test I/O the CIC also goes into a command interrupt sequence. If the command is not a Test I/O the microprogram resets STATUS IN and OPERATIONAL IN, restores the poll by transferring the old poll stored in the data working register to the poll register

(DWRKB-), and transfers the original ROM address stored in the lower working register back to the ROM address register.

3.2.20.7 Command Interrupt CIC-PTS-100 Sequence (Figure 3-73). After the 360/370 issues a command and accepts status from the CIC, the CIC microprogram sends an Input Word function code to the PTS-100 processor and puts the tumble table address stored in the upper and lower working registers onto the IOB through the DMA MUX OUT. The tumble table base and the contents of the tumble table register make up the tumble table address (having been previously put into the upper and lower working registers during the data interrupt sequence). Following the transfer of the tumble table address the CIC microprogram puts the initial device address stored in the data working register (address C) onto the IOB to the PTS-100 processor. Next it sends an input byte function code to the PTS-100, which causes the initial device address byte to be stored in memory at the tumble table address.



Then the microprogram increments the tumble table register and transfers its contents to the lower working register via the data in and data muxes. It also resets STATUS IN and OPERATIONAL IN and disconnects from the 360/370. The original command from the 360/370, stored in the data working register, is now transferred to the PTS-100 by the microprogram. The microprogram loads the poll address from the poll register into the lower working register through the data in and data muxes. The poll address is combined in the DMA MUX OUT with the previously loaded device packet base stored in the upper working register and with ROM bits 4, 9, 10, and 11 to form an effective address. The effective address points to byte locations 6 and 7, A and B, or C and D of the device packet, depending on the particular CIC status conditions. (See Figure 3-76.) It is sent to the processor with an input word function code. The command stored in the data working register is now sent over the IOB to the processor accompanied by an input byte function code. The command is stored at the effective address in the device packet. The ROM holding register, which has the busy bit set and the halt bit reset, is now loaded into the Do register condition bit at the poll address via the holding register mux. Then the poll register is restored to its previous address by reading into it the address stored in the data working register. The program next sets a tumble table interrupt in the interrupt register and gates circuit. This interrupt flags the processor to look at the tumble table in memory and perform the operation requested by the command on the addressed device. The ROM address stored in the lower working register at the start of this sequence is then put back into the ROM address register.

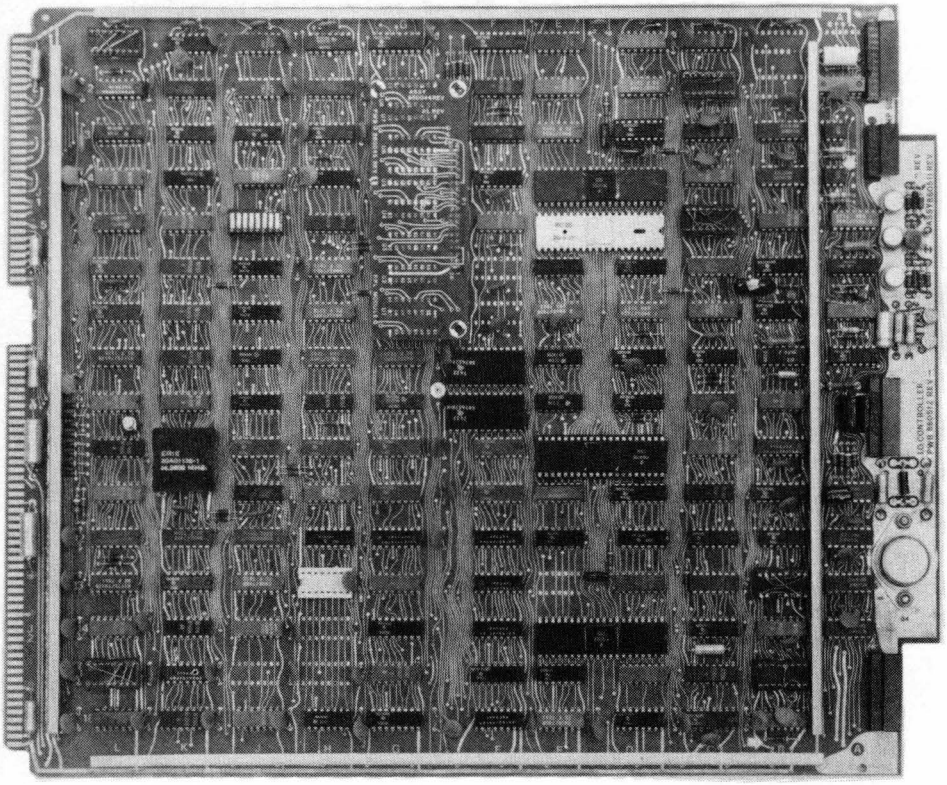
3.2.20.8 Send Data to 360/370 Sequence (Figure 3-73). When the PTS-100 program detects a device address with the MSB set in the interrupt tumble table, it reads the 360 command previously stored in the associated I/O device packet. If the command is a Read (transmit to 360) command the program puts the order, buffer address, and byte count into the packet; then it issues a Start Device DIO instruction to the CIC and sends the order, byte count, and buffer address in the manner described in Section 3.2.20.3b. On receipt of the order, byte count, and buffer address, the CIC resets the data and 4-byte counters and sends an output word +1 function code to the processor. This causes the processor to increment the buffer address and put it back into the packet. The CIC then sends an output word function code to the processor, which responds by sending the first data byte to the CIC. Here it is stored in the data working register at the address set into the data counter. The data counter and 4-byte counter are incremented and the process is repeated four times transferring four data bytes to the data working register, whereupon the 4-byte counter contains a count of 3. When this occurs the CIC performs a "control unit initiated send data" sequence as described in Section 3.2.20.4b.

3.2.20.9 Receive Data from 360/370 Sequence (Figure 3-73). When the PTS-100 program detects a device address with the MSB set in the interrupt tumble table, it reads the 360 command previously stored in the associated I/O device packet. If the command is a Write (receive from 360) command the program puts the order, buffer address, and byte count into the packet; then it issues a Start Device DIO instruction to the CIC and sends the order, byte count, and buffer address in the manner described in Section 3.2.20.3c. On receipt of the order, byte count, and buffer address, the CIC performs a "control unit initiated receive data" sequence, Section 3.2.20.4c.

3.2.21 Input-Output Controller (IOC) Operation

The IOC (Figure 3-77) is a microprogrammable controller that provides the interfaces between the PTS-100 processor and the display keyboard channel, a printer with or without keyboard, a transmit modem, a receive modem, and a single receive only cassette. The IOC is software compatible with the multiplex channel controller, which it replaces along with the motherboard(s) and I/O adapters.

The IOC receives and executes instructions from the processor, performs the necessary data buffering, and reports the status of the I/O device to the processor. The IOC is mounted on a single full size plug-in PC board.



C75-1847

Figure 3-77. Input/Output Controller (IOC)

3.2.21.1 Interfaces. The IOC patching and microprogram can be changed to provide the interface for any of the standard modems (IPARS, CTMC, 2848, 3270, AMAPL, and Switched Network), all the standard printers, TTYs, etc., presently used with the MISA adapter, the receive only cassette, and the keyboard channel. The interfaces between the IOC and these devices are exactly the same as those described for the individual modem, MISA, cassette, and keyboard adapters. The only exception is for the read only cassette, which only uses the read interface since the IOC does not have a cassette record capability.

The IOC MISA interface, which is described in Section 3.2.13, is RS232 asynchronous or current loop with a data rate of up to 4800 baud, half duplex, start and one or two stop bits, 5 to 8 bits per data character, and odd, even, or no parity. The modem interface is the same as that described in Sections 3.2.14 through 3.2.17, and Appendix C. The keyboard interface is the same as that described in Section 3.2.9. The read only cassette interface is the same as that described in Section 3.2.18.

The IOC patch plug wiring for the different interface configurations is shown in Figure 2-22.

3.2.21.2 Status and ICB. The IOC has an 8 bit status register and an 8 bit ICB register for each I/O device. The status and ICB registers are part of the RAM and they are used to store status and ICB information for each of the four I/O devices.

The first two bits in each status register define adapter ready and adapter busy conditions with a zero in both of these bits indicating that the associated device is not available. The remaining status bits are defined by the microprogram for the particular I/O device. They are the same as those for the counterpart I/O adapters. The adapter descriptions in Sections 3.2.9 through 3.2.18 give the status bit meanings; refer to Table 3-7 for the status bit listing.

The ICB bits (interrupt condition bits) inform the program of interrupt conditions. The ICB bytes (8 bits) are also the same as for the counterpart I/O adapters. The ICB bits are set by the I/O devices and their interfaces. When an ICB bit is set the microprogram fetches the interrupt mask from the associated PIOT using the function code bus. The mask is ANDed in the ALU with the ICB byte on a bit by bit basis to determine whether an interrupt should be generated. Patch plug L1 is used to specify the interrupt line raised by each device. See Figure 2-22 for the patch plug wiring. The processor will only respond to an interrupt if the interrupts have been enabled by the program. The ICB byte and mask format is shown and described in Section 3.1.9.2. Refer to Table 3-7 for the ICB bit listings.

3.2.21.3 Circuit Description.

a. Initialization

The IOC simplified block circuit diagram is shown in Figure 3-78. The IOC responds to the two basic instructions from the processor: Do I/O, to start or stop an I/O operation; and Read I/O, to read or read and reset status. The processor places these instructions on the IOB data bus in addition to the address code for the selected controller and I/O device (Sections 3.1.9 and 3.1.10). The processor then raises the device address window (DAW) control line to identify this data as address information to the controllers. For a start DIO instruction, the processor next places the effective address (EA) of the PIOT table for the addressed device on the data bus and raises the Data Out Window (DOW). The IOC address decoder detects the IOC address and queues the DMA control circuits through IOC address chip switch J5. The device address latch holds the device address. On a start DIO instructions, this latch sets a condition bit to the microprogram (via the ALU and P.C.) that tells the microprogram that a start DIO command has been received, since bit 3 of the instruction is found to be on. Another condition bit from the DMA control circuit then flags the microprogram to begin operation.

Once started, the microprogram directs the IOC to accept the EA on the IOB and store it in the effective address portion of the RAM at the EA location for the addressed device. The RAM has a dedicated location for the EA for each of the four I/O devices. It also has dedicated locations for status bytes, orders, and ICBs for each of the four I/O devices.

The RAM is addressed by the ROM and the decoded output of the scan counter, which has four states, one for each I/O device. The scan counter can either continuously scan the RAM locations for each I/O device (used to poll each I/O device after initialization) or it can be jammed to the I/O device address. It is jammed to the device address set into the device a address latch modified by patch L15 and jammed to the address of a device requesting service by the ROM instruction decode. The device address patch L15 allows the device addresses to be assigned to any I/O device (see Figure 2-22 for the patch wiring).

The scan counter output is also applied to the program counter where it is used to jump to the appropriate microprogram sequence in ROM to direct the initialization or servicing for the addressed device.

After the EA is in the RAM the IOC takes control of the I/O operation, requesting the order from the PIOT table (see Section 3.1.9) and storing it in the RAM, using the arithmetic unit in the processor as necessary through

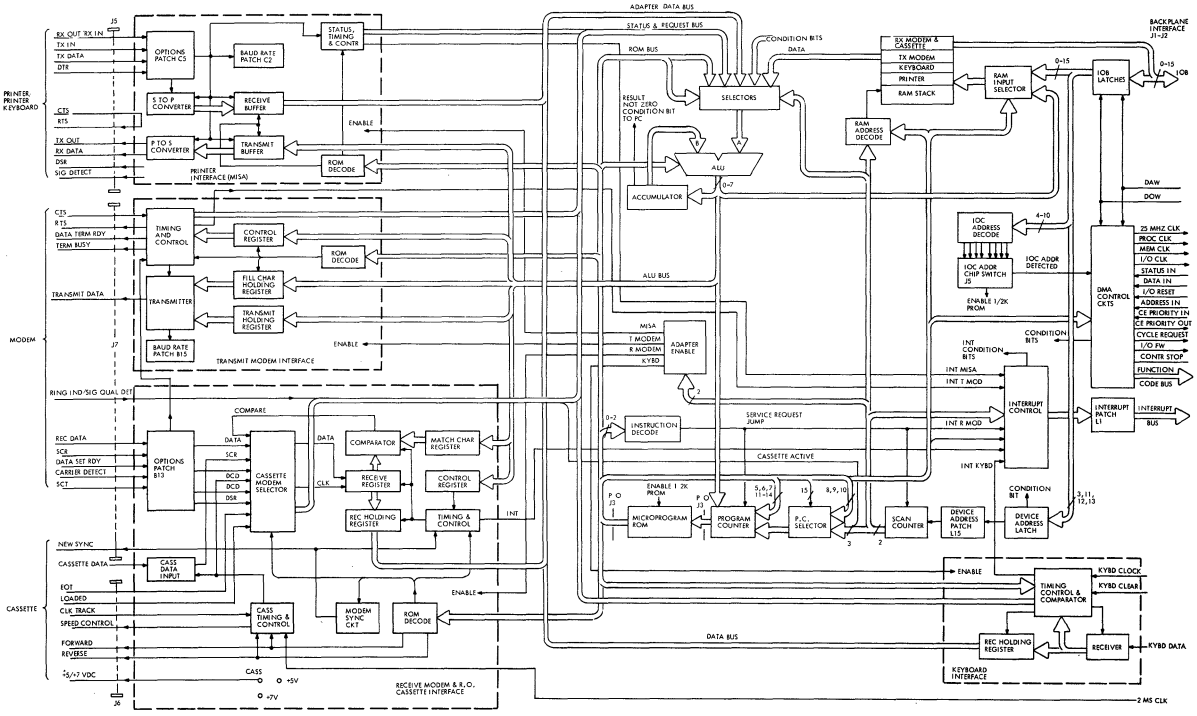


Figure 3-78. IOC Simplified Circuit Blôck Diagram

the operation of the 4 bit function code bus, and writing data into, or reading data from, the designated portions of memory.

Each device on the IOC, keyboard, printer, transmit modem, and receiver modem or cassette is initialized in the same way, the only difference being the device addresses and the storage locations in RAM.

b. Microprogram ROM

The microprogram that directs the operation of the IOC resides in the ROM. Each different application of the IOC uses a different ROM, which can have 256, 512, 768, or 1024 16 bit words. The ROM chips are mounted on a separate piggyback module that plugs into receptacle J3. The module accommodates up to eight 1024 or 2048 bit memory chips (256 or 512 4 bit words). Chip switch J5 selects the ROM addressing for the 1K and 2K chips. The ROM chip locations, allocations, and associated switch J5 settings are shown in Table 2-4 and Figure 2-22.

The program counter addresses the microinstructions in the ROM. It is driven by the ROM bits, the output of the ALU, the instruction decode, and the P. C. selector. The instruction decode is used to jump to the service request routines. The P. C. selector selects either the two scan counter outputs and the cassette active signal or ROM bits 8, 9, and 10 to supplement the other ROM bits to address the ROM. The cassette active signal flags the microprogram that the cassette interface is used. The ROM bits address each succeeding microinstruction in the microprogram routines, and the scan counter outputs provide the device addresses that further select the applicable routines for each I/O device.

c. RAM Stack

The RAM is an 8 bit, 32 word, read and write memory. It stores the four effective addresses (16 bits each), the four 8 bit order codes, the four 8 bit ICB bytes, the four 8 bit status bytes, the keyboard address, and four CRC characters. The remainder is temporary storage, scratch and data registers. All data passing into or out of the IOC passes through the RAM. RAM addressing is performed by the RAM address decode, which is driven by the ROM bits in conjunction with the scan counter. The RAM input selector, which is also under ROM control, connects either the ALU output or the IOB to the RAM input. All data out of the RAM processes through the ALU except that which is sent out directly to the processor on the IOB.

d. ALU

The ALU is an 8 bit arithmetic unit that is used for both arithmetical and logical operations (for example, to see if a bit is set, or to check ICB

bits against the mask). It operates on the data, status, etc., selected by the ALU selectors that are under control of the ROM. The ALU output is applied to the I/O device interface circuits, to the RAM, and to the program counter where it causes ROM program branches. The accumulator provides the B operand input to the ALU. In addition, it produces a result not zero condition bit, which is also used for program branches. All data sent to or received from the I/O devices is carried on the adapter data bus, and data sent to the I/O devices is carried on the ALU bus.

e. Interface Circuits

The interface circuits provide the same functions as their counterpart device adapters. They send and/or receive data and interface signals to/from their associated devices and they monitor device status and generate interrupt condition bits. The IOC accommodates five interfaces: MISA, transmit modem, keyboard channel, receive modem, and receive only cassette.

The interface circuits are individually enabled by the adapter enable circuit, which decodes the scan counter outputs. Whenever the scan counter is at a device address, the associated interface circuit is enabled. When the scan counter is polling, each of the interfaces is enabled in turn. The microprogram controls each interface through its ROM decode. Whenever an interface circuit requests service it raises a request line on the request bus to the ALU selectors. Then when the scan counter polls that interface circuit the request is processed (through the ALU and P.C. where it is used to select the ROM routine to carry out the request).

When an interface circuit wants to interrupt the PTS program it raises an interrupt line to the interrupt control circuit, which informs the ROM microprogram of the interrupt and sends the interrupt to the processor over the interrupt bus (but only after the ICB bits have been checked against the interrupt mask). Patch L1 is used to patch the I/O device interface interrupts to any processor interrupt level.

(1) Printer Interface (MISA).

This interface is the same as the MISA (Section 3.2.13). It operates in half duplex to send data to a printer or receive data from a printer keyboard. Data characters sent to a printer are received from the RAM via the ALU as parallel characters, buffered, converted to serial data by the parallel-to-serial converter, and sent out to the printer. The character rate and options (parity, number of bits/character stop bit) are determined by patches C2 and C5 (see Figure 2-22). Data received from a printer keyboard is converted from serial to parallel, buffered, and sent to the ALU over the adapter data bus. All data transfers are under ROM control.

(2) Transmit Modem Interface

This interface can be patched and programmed to be the same as that for any one of the transmit modem adapters described in Sections 3.2.14 through 3.2.17. The data to be transmitted is transferred from RAM through the ALU and loaded into the transmit holding register. Fill or idle characters are loaded into the fill character holding register and a coded control character describing the word length, parity, clock rate, number of stop bits, synchronous or asynchronous operation, etc., is loaded into the control register. All data transfers are under ROM control. The parallel data characters from the holding registers are converted to serial in the transmitter and sent out to the modem. The transmitter is under the control of the timing and control circuit, which decodes the character in the control register and directs the transmitter accordingly. Patch B15 selects the transmitted baud rate. See Figure 2-22 for the patch configuration.

(3) Receive Modem and Receive Only Cassette Interface

This interface is used for a receive modem and for the receive only cassette. It is microprogram controlled and it is used for both interfaces, but not at the same time. A start DIO instruction must be reissued each time the interface is switched between the two devices.

The receive modem interface can be patched and programmed to be the same as that for any one of the receive modem adapters described in Sections 3.2.14 through 3.2.17. The cassette interface is the same as the receive portion of the cassette adapter described in Section 3.2.18.

The cassette connects to receptacle J6 and the modem connects to J7. The cassette/modem selector, which is controlled by the microprogram, selects either the cassette or the modem data, clock, and control inputs. The selector connects the selected serial data and clock to the receive register and the selected device status and request signals to the ALU selectors. The receive register assembles the incoming serial characters, changes them to parallel characters, and applies them to a comparator and to the receive holding register. The holding register retains the data character until the ROM microprogram directs that it be transferred out. The comparator compares the received data character with a sync character put into the match character register by the ROM microprogram. The comparator generates a compare signal that is sent back to the microprogram when a comparison is detected. This

enables the program to look for sync or any other special character in the data received from the modem.

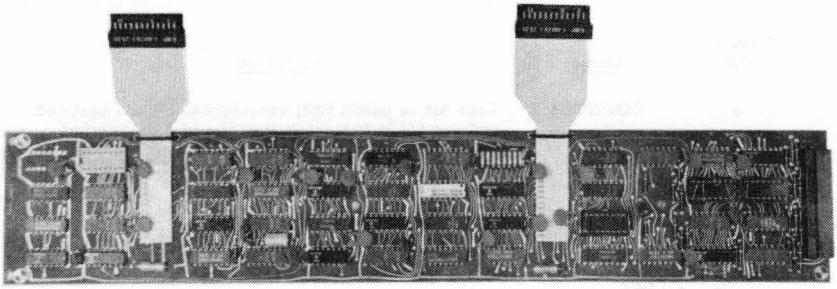
The microprogram also loads the control register with a coded character that describes the number of bits/character, parity, synchronous or asynchronous, number of stop bits, etc., to be received. The timing and control circuit decodes the control character and directs the receive circuits accordingly.

(4) Keyboard Interface

The keyboard interface performs the same overall function as the keyboard adapter on the multiplex channel controller described in Section 3.2.9. The serial keyboard data from the display adapter is assembled into 8 bit characters in the receiver, checked for non-zero by the comparator, and loaded into the receive holding register. The keyboard clock pulses are counted, and after eight have occurred (the complete character is assumed to be in the receiver at this time) a service request is sent to the ROM. When the ROM microprogram services the request it increments a keyboard address character stored in the RAM. Then it checks the comparator to see if the character is not zero; if it is not, the microprogram transfers both the incremented keyboard address from RAM and the keyboarddata character from the keyboard holding register to the processor. The keyboard address in RAM is incremented by one for each keyboard data character received until the count reaches 128 (maximum of keyboards), whereupon it repeats, starting over again. Only non-zero keyboard characters are transferred. Zero characters indicate that no data has been entered on the associated keyboard.

3.2.22 Parallel Adapter Operation

The parallel adapter provides the interface between one port on the multiplex channel controller and a receive only printer or other receive I/O device that requires data in parallel format. The adapter (Figure 3-79) receives the data from the multiplexer in 8 bit bytes. It can accumulate two 8 bit bytes and transfer them together to the I/O device. However, in this mode one byte is used for control. It can optionally hold an 8 bit control character while transferring other 8 bit data bytes or it can transfer alternate data and control bytes. The adapter executes write orders via the multiplex channel controller and provides status and interrupt condition bits to the multiplexer. The output signal polarities, control bits, status bits, and interrupt condition bits are patch and switch selectable. The output level to the I/O device is TTL with 100 ohm resistors in series with the outputs.



C75-1859

Figure 3-79. Parallel Adapter

3.2.22.1 Interfaces. The interface between the parallel adapter and the I/O device is shown in Figure 2-3.

3.2.22.2 Status and ICB. The parallel adapter reports status and ICB bits to the multiplex controller over bits 0 through 6 of the adapter data bus. Bits 0 and 1 are ready and busy status; the remaining bits 3 through 6 (bit 2 is not used) are used for both I/O device status and interrupt conditions. Chip switches F1-1 through F1-4 are used for the manual entering of a code on status bits 3 through 6 that describes the I/O device type to the program. This information supplements the feature board configuration data.

Data Bus Bit	Name	Description
0	Ready	The adapter raises this bit (1) when it and the I/O device are ready to process data. The bit is set when there is no existing order and the device is available.
1	Busy	This bit is set (1) by ORDER OUT and DEVICE AVAILABLE. It indicates that the adapter is actively transferring data.
3-6	-	These bits are set manually with switches F1-1 through F1-4. They identify the I/O device type to the program.
3	EOR(ICB)	This bit is set (1) after the last character of a data block has been transmitted. It causes an ICB REQUEST and indicates the end of the record.
4	MALF(ICB)	This bit is set (1) when the I/O device is not operating or present when an ORDER OUT is received. It causes an ICB REQUEST.
5	ERR(ICB)	This bit is patch (B2) selectable. When patched and set (1) it indicates that a parity error has been detected in the last character sent to the I/O device. When that occurs it also causes an ICB REQUEST.

Data Bus Bit	Name	Description
6	TOF(ICB)	This bit is patch (B2) selectable. When patched and set (1) it indicates that the I/O device has reached the top-of-form position. When that occurs the bit also causes an ICB REQUEST.

3.2.22.3 Circuit Description (Figure 3-80).

a. Timing

The 160 nanosecond MUX CLOCK clocks all circuits on the parallel adapter except the data and control output flip-flops, which are clocked by: ACK, Request Reset, ADB0, ADB3, Order and Switch F1-7. The 2 ms CLOCK clocks the demand antibounce circuit.

b. Initialization.

The adapter is initialized when the program issues a start I/O order to the multiplexer. The start order contains the address of the adapter to be initialized. It causes the multiplexer to fetch and send to the adapter the order to be performed. The only order used for the parallel adapter is the write order. The multiplexer informs the adapter of the order by raising ORDER OUT.

Prior to receipt of the order the I/O device activates ON LINE (normally patched B2) to DEVICE AVAILABLE, which is applied to ADB0 to tell the multiplexer that the device is ready to process data. The multiplexer then sends ORDER OUT, which sets the order flip-flop. Order terminates READY (ADB0) and raises BUSY. However, if the I/O device is not available at this time the MALF flip-flop will be set instead of BUSY. MALF then generates REQUEST to the multiplexer, which replies with ACK, causing the ICB REQUEST to be sent to the multiplexer and gating the MALF ICB bit out on ADB4.

c. Data Transfer

When the I/O device is ready to accept data it raises DEMAND to the adapter. Patch B2 selects the demand signal and applies it to the Request flip-flop input circuit. The demand signal can be the direct or inverted demand input or a positive or negative polarity 32 ms signal. The latter is produced by the antibounce circuit, which is initiated by demand and timed out after counting eight 2 ms clock pulses. Demand along with $\overline{\text{BUSY}}$ and $\overline{\text{STROBE}}$ sets the Request flip-flop, which generates REQUEST to the multiplexer. When the multiplexer sends ACKnowledge, the adapter replies with DATA REQUEST, telling the multiplexer that the I/O device is ready for service. The multiplexer responds to DATA REQUEST by placing a data

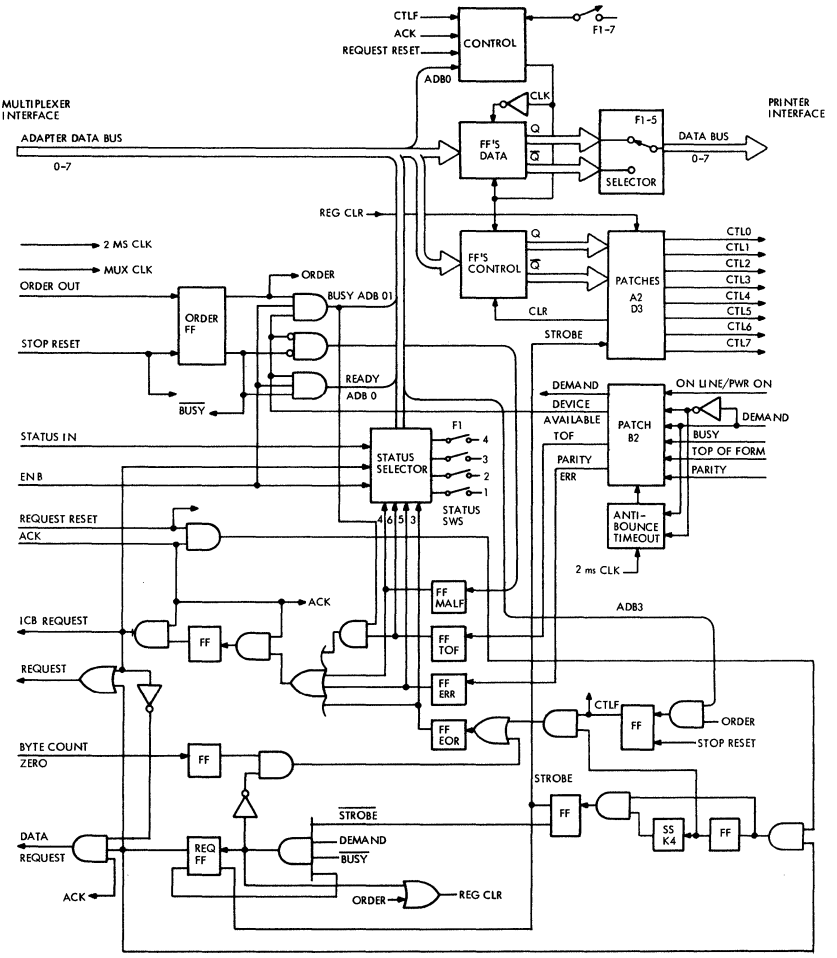


Figure 3-80. Parallel Adapter Simplified Circuit Diagram

character on the adapter data bus and sending REQUEST RESET to the adapter. The data character is clocked into either the data or control flip-flops, which have been previously cleared by Order or DATA REQUEST. The character is clocked into the data flip-flops by ACK, REQUEST RESET, and no CTLF or the signal from switch F1-7. The character is clocked into the control flip-flops and not the data flip-flops when CTLF occurs or switch F1-7 is set and ADB0, now acting as a control bit, is high. CTLF is generated by ORDER and ADB3, which in this case also acts as a control bit. Thus the character on the ADB can be put into the control flip-flops in one of two ways, using ADB bits 0 or 3 as control. The control flip-flops can be used to extend the number of bits in the output data character or they can hold or transfer control information for the I/O device. The polarity of the data outputs is selected by switch F1-5, which controls the output selectors that select the direct or inverted outputs of the data flip-flops. The control (CTL) outputs can be patched to either the direct or the inverted control flip-flop outputs on patch plugs A2 and D3. The output flip-flops can all be cleared together, when ORDER OUT is received or when a data request is generated, or the control flip-flops can be cleared separately, depending upon a patch on D3.

REQUEST RESET, ACK and REQUEST (data) also produce a data strobe, which resets the request flip-flop and which can also be sent out to the I/O device via patch plug A2. The data strobe indicates that the data character is in the output flip-flops awaiting transfer to the I/O device. Single-shot K4 delays the occurrence of the strobe for 30 microseconds. This limits the character transfer rate to one character every 30 microseconds and prevents the parallel adapter from tying up the IOB, since it could operate at the IOB speed.

d. Status and ICB

ENB, STATUS, and ICB REQUEST select and gate out at the status and ICB bits onto the adapter data bus. The status selector selects either status bits 3-6 from switches F1-1 through F1-4 or the ICB bits. When the multiplexer wants to read status it sends ENB and STATUS IN to gate out the status bits. The ICB bits are gated out by ICB REQUEST. The ICB bits initiate ICB REQUEST when any one of them is active. The TOF (Top-of-Form) ICB bit will only initiate an ICB REQUEST if it occurs while the device is busy. The TOF and ERR ICB bits are both patch selectable on patch plug B2. The EOR (End Of Record) ICB bit is set by BYTE COUNT ZERO after the last character has been transferred, or by CTLF at the beginning of the data output strobe.

3.2.23 Display Adapter/Monitor Controller/Feature Board (DA/MC/FB) Operation

The DA/MC/FB (Figure 3-81) provides the combined features of the display adapter, monitor controller, and feature board on a single board for the 1005 and 1014 processing units. The DA portion supports one or two 16K memory boards, the integral MC (with one display) and one remote display, two keyboards, and two LED panels. The FB portion has all the features of standard feature board A except the WDT interrupt option. See the DA/MC/FB simplified circuit diagram, Figure 3-82, and refer to the circuit descriptions in Sections 3.2.2, 6 and 7.

3.2.23.1 Display Adapter Circuits. The DA portion of the DA/MC/FB provides the same basic functions in the same way as the standard display adapter. It refreshes memory, reads data out of memory for display refresh, assembles data from the keyboards and sends it to the IOC or multiplex channel controller.

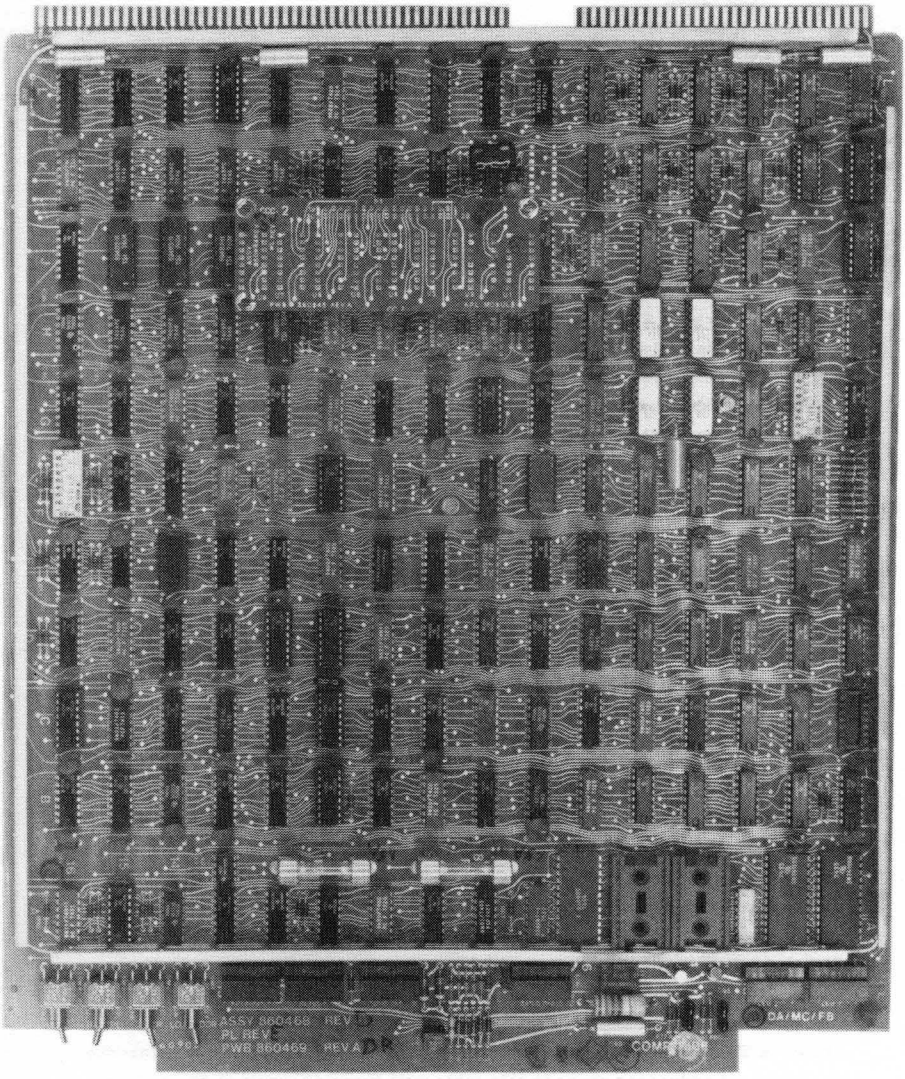
a. Clocks

The 25 MHz and 160 ns clocks from the IOC or multiplex controller clock the DA and MC Timing circuits that produce KEYBOARD CLEAR, KEYBOARD STROBE, and the 2 ms and 64.1 μs clocks. See Figure 3-83. The timing circuit also produces PS SYNC that synchronizes the switching power supply to the DA and MC timing to prevent power supply generated switching transients from interfering with the display.

b. Keyboards

The two keyboards connected to the remote monitor controller are loaded when the DA/MC/FB sets bit 15 of the DA character (see Figures 3-31 through 3-36) in the same way as in the standard DA - MC system except that only two of the keyboards are addressed. The clocks and load pulses for the keyboards connected to DA/MC/FB J8 and J9 are generated by the keyboard address circuit, which is driven by the DA/MC/FB timing circuits and controlled by the memory size switches of option switch G2. One load pulse is sent to each keyboard every 66.64 ms, and the keyboard clock pulses occur every 64.1 μs. The keyboard addressing sequences are shown in Table 3-20. To determine the keyboard load timing cross reference the keyboard addresses given in this table with those shown in Table 3-12 in Section 3.2.6.3.

The incoming keyboard data from J6, J8, and J9 is ORed and either passes directly out to the keyboard adapter in the multiplex controller or IOC when only one memory board is installed, or it first has its timing changed by the shift register when two memory boards are installed



C76-1987

Figure 3-81. DA/MC/FB

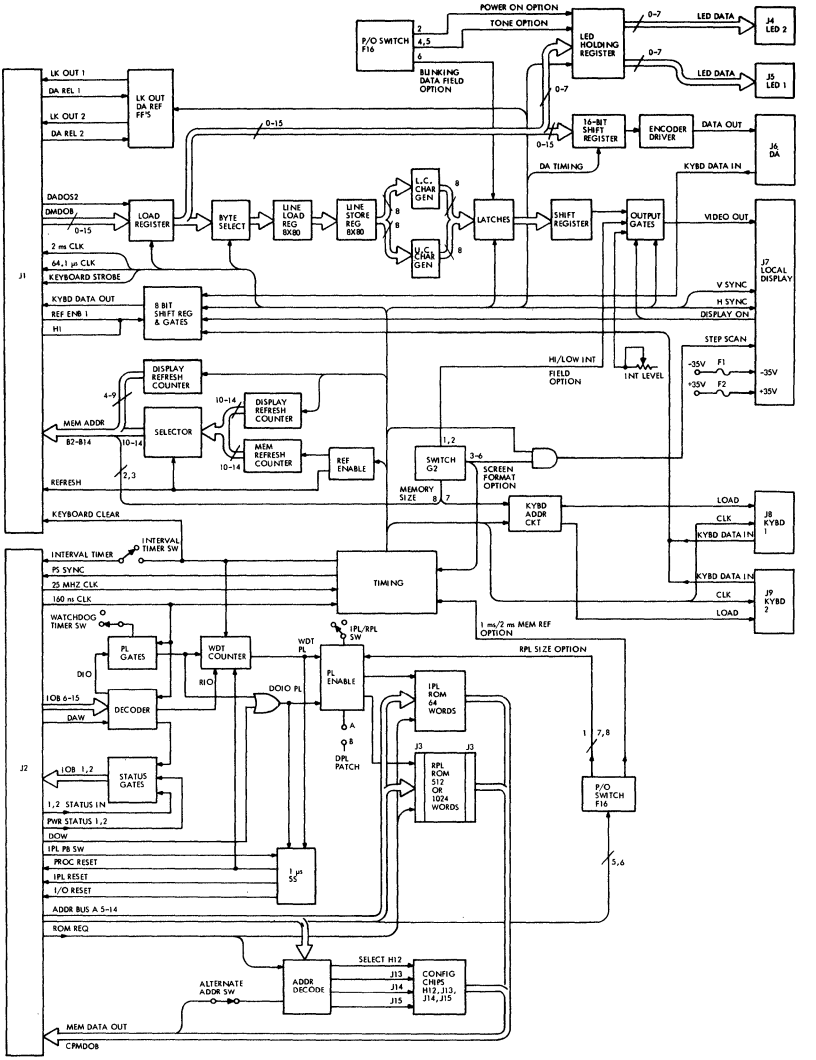


Figure 3-82. DA/MC/FB Simplified Circuit Diagram

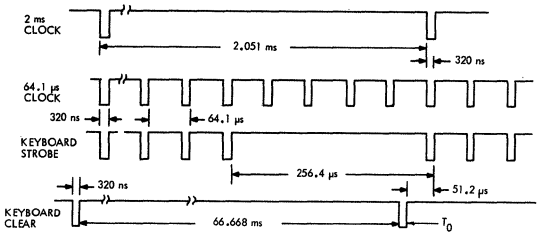


Figure 3-83. DA/MC/FB Clock Outputs

(REF ENB1 present). The shift register delays the keyboard data and effectively changes the keyboard addresses for memories above 16K. The DISPLAY ON signal from the local display inhibits data from the local keyboards when the display is off or when the keylock is on.

c. Memory Refresh

The DA/MC/FB refreshes memory during the LS-DA time (see Figure 3-31) in exactly the same way as for the standard display adapter (Section 3.2.6.2) except that the LKOUT 1, 2 signals are used instead of DAREQ1,2 signals and they are both raised together so the columns on both memory boards are refreshed simultaneously. REFRESH is generated by the refresh enable circuit, which increments the memory address counter whose output is selected to provide memory address lines B10-B14. When the 2 ms refresh option is selected by switch F16, REFRESH is produced every 64.1 µs during the LS-DA time and it remains active for 10.24 µs. The refresh memory address counter is incremented once for each refresh cycle. When the 1 ms refresh option is selected two refresh cycles are performed during every LS-DA period.

d. Display Refresh

During display refresh the memory address selector selects the display refresh counter output to provide address lines B10-B14. The other display refresh counter provides address lines B4-B9 and option switch G2 provides lines B2 and B3. Address lines B2 and B3 select a 4192 byte group in the top 16K memory board and LKOUT2 flags the top memory board to the display refresh operation. Data for display cannot be stored in the bottom board. Regardless of the size of memory installed and regardless of the display format used, the display data is always stored in one of the top three 4192 byte groups in the top 16K memory board. Refer to Table 3-20 for the memory buffer assignments.

Table 3-20. DA/MC/FB LED and Display Data Memory Buffer Assignments and Keyboard Addresses

Memory in Bytes	Monitor	Connected To:	1920 Char/Display 80 Ch x 24 Lines 64 Ch x 30 Lines Memory Buffer Area	1920 Char/Display 80 Ch x 24 Lines 64 Ch x 30 Lines Keyboard Address	960 Char/Display 80 Ch x 12 Lines 64 Ch x 15 Lines Memory Buffer Area	960 Char/Display 80 Ch x 12 Lines 64 Ch x 15 Lines Keyboard Address	960 Char/Display 40 Ch x 24 Lines Memory Buffer Area	960 Char/Display 40 Ch x 24 Lines Keyboard Address	480 Char/Display 40 Ch x 24 Lines Memory Buffer Area	480 Char/Display 40 Ch x 24 Lines Keyboard Address
8K	0 Disp.		1000-17FF	91(X2)* B1(X3)*	1800-1BFF	99	1800-1BFF	99	1C00-1DFF	D9
12K	0 Disp.		2000-27FF	85(X2)* A5(X3)*	2800-2BFF	8D	2800-2BFF	8D	2C00-2DFF	CD
16K	0 Disp.	XJ6	3000-37FF	95(X2)* B5(X3)*	3800-3BFF	9D	3800-3BFF	9D	3C00-3DFF	DD
24K	0 Disp.		5000-57FF	92(X2)* B2(X3)*	5800-5BFF	9A	5800-5BFF	9A	5C00-5DFF	DA
32K	0 Disp.		7000-77FF	96(X2)* B6(X3)*	7800-7BFF	9E	7800-7BFF	9E	7C00-7DFF	DE
8K	LED 0 LED 1	MC X10 MC X11	1780 1782		1BC0		1BC0		1DE0	
12K	LED 0 LED 1	MC X10 MC X11	2780 2782		2BC0		2BC0		2DE0	
16K	LED 0 LED 1	MC X10 MC X11	3780 3782		3BC0		3BC0		3DE0	
24K	LED 0 LED 1	MC X10 MC X11	5780 5782		5BC0		5BC0		5DE0	
32K	LED 0 LED 1	MC X10 MC X11	7780 7782		7BC0		7BC0		7DE0	
8K	Local		1800-1FFF	99(J8)** B9(J9)**	1C00-1FFF	D9	1C00-1FFF	B9(J9)**	1E00-1FFF	F9
12K	Local		2800-2FFF	8D(J8)** AD(J9)**	2C00-2FFF	CD	2C00-2FFF	AD(J9)**	2E00-2FFF	ED
16K	Local	XJ7	3800-3FFF	9D(J8)** BD(J9)**	3C00-3FFF	DD	3C00-3FFF	BD(J9)**	3E00-3FFF	FD
24K	Local		5800-5FFF	9A(J8)** BA(J9)**	5C00-5FFF	DA	5C00-5FFF	BA(J9)**	5E00-5FFF	FA
32K	Local		7800-7FFF	9E(J8)** BE(J9)**	7C00-7FFF	DE	7C00-7FFF	BE(J9)**	7E00-7FFF	FE
8K	LED Byte 1 LED Byte 2	XJ4 XJ5	1F80 1F82		1FC0		1FC0		1FE0	
12K	LED Byte 1 LED Byte 2	XJ4 XJ5	2F80 2F82		2FC0		2FC0		2FE0	
16K	LED Byte 1 LED Byte 2	XJ4 XJ5	3F80 3F82		3FC0		3FC0		3FE0	
24K	LED Byte 1 LED Byte 2	XJ4 XJ5	5F80 5F82		5FC0		5FC0		5FE0	
32K	LED Byte 1 LED Byte 2	XJ4 XJ5	7F80 7F82		7FC0		7FC0		7FE0	

*Connectors on Monitor Controller

**Connectors on DA/MC/FB

The data for display refresh is read from memory in the same way as for the standard display adapter. The data words for the remote and local displays are read alternately from their associated memory buffer areas and loaded into the load register. The data for the remote display is routed out of the load register to a shift register, where the hardwired DA, LS, FS, EOL, and sync characters are added. See Figures 3-31 through 3-36. (The DA/MC/FB puts zeros in for the LS and EOL characters.) The data stream from the shift register is encoded in the Manchester system and sent to a remote monitor controller via connector J6.

3.2.23.2 Monitor Controller Circuits. The data for the local display is line assembled in the line load register, line stored in the line store register, converted to character line slices and sent out to the local display through the latches, shift register and output gates. The process is the same as that which takes place in the standard monitor controller (see Section 3.2.7). The blinking data field option from switch F16 gates the output of the latches, and the HI/LOW intensity option control from switch G2 gates the intensity level control in the output gates. The resulting video signal, vertical sync, horizontal sync, and step scan signals are sent to the local display. STEP SCAN which is controlled by display format selected by option switch G2, increases the vertical spacing between the rows of characters on the display.

The LED bytes (see Table 3-20 for memory buffer locations) for the local display LED panels are gated into the LED holding register. The power on and tone option control signals from switch F16 are also brought in, and the resulting LED data is applied to the associated LED panel through connectors J4 and J5. The LED bits set the LED indicators on the display and keyboard as shown below:

LED Byte Bit	0	1	2	3	4	5	6	7
Controls On Display	9*	8	7	6	5	4	3	2
LED No. On Kybd		12		10	8	6	4	2

*Controlled by Display Power On Option

3.2.23.3 Feature Board Circuits. The feature board portion of the DA/MC/FB provides the same functions as standard feature board B,, except that there is no watchdog timer interrupt and only four configuration switches are used. Refer to Section 3.2.2 for the standard feature board.

The watchdog timer program load works in the same way as for feature board B. The watchdog timer PL, DO I/O PL, and IPL pushbutton switch generate system resets and initiate program load from either the IPL or RPL

ROMs depending on the setting of the IPL/RPL switch. When the DPL (Dual Program Load) jumper A to B is made, a DO I/O instruction to the watchdog timer always initiates an RPL regardless of the setting of the IPL/RPL switch, and the WDT and IPL pushbutton program load are under control of the IPL/RPL switch.

The RPL ROM is mounted on a separate piggyback plug-in module. It is either a 512 or a 1024 word program selected by switches 1, 7, and 8 of switch chip F16. The locations of the individual PROMs on the piggyback module are shown in Table 2-4. The processor addresses the load program words via the address bus, and the loading program is read out of the selected ROM onto the memory data bus a word at a time. The four words set into the configuration chips are read out in the same way.

The alternate load address switch determines the address of the load device. When the switch is off device address zero is used. When the switch is on (sets bit 0 of word 32) the first configuration word determines the load device.

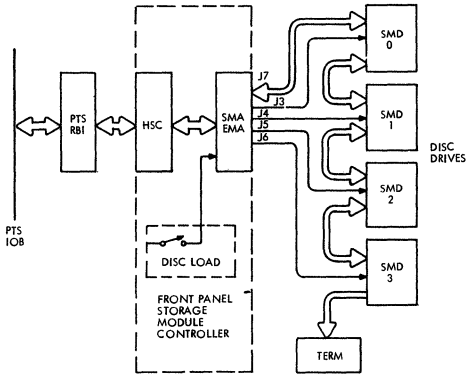


Figure 3-84. PTS RBI

3.2.24 PTS Rapidbus Interface (PTSRBI) Operation

The PTSRBI (see Figure 3-84) is used to connect high speed rapidbus controllers to the PTS. It can accommodate up to seven controllers. The PTSRBI provides the interface between the rapidbus and the PTS I/O bus (IOB). It converts PTS interface discipline to rapidbus interface discipline and vice versa. The PTSRBI is shown in simplified form in Figure 3-85.

The PROMs on the PTSRBI are preprogrammed to control its operation. The PROMs are addressed by the various interface signals and they output corresponding control signals to drive the interfaces. They also coordinate the transfer of data, addresses, status, commands, packets, and interrupts from one interface to the other.

The PTSRBI has two stack registers (CMD stack and Data/Addr stack), which temporarily store commands (requests) from rapidbus, along with their associated data (and address), until they can be operated on. The commands are then executed in the order of their arrival. Up to four commands can be stacked.

Every CPU interface on rapidbus is assigned a CPUID number. The CPUID number used by the PTSRBI is optional except when it is the only CPU interface on the rapidbus, in which case it must be zero. The CPUID is set into chip switch B26 (bits 2-4), and the request and acknowledge levels that correspond to the CPUID number (zero for zero, one for one, etc.) are set into patches B6 and B7.

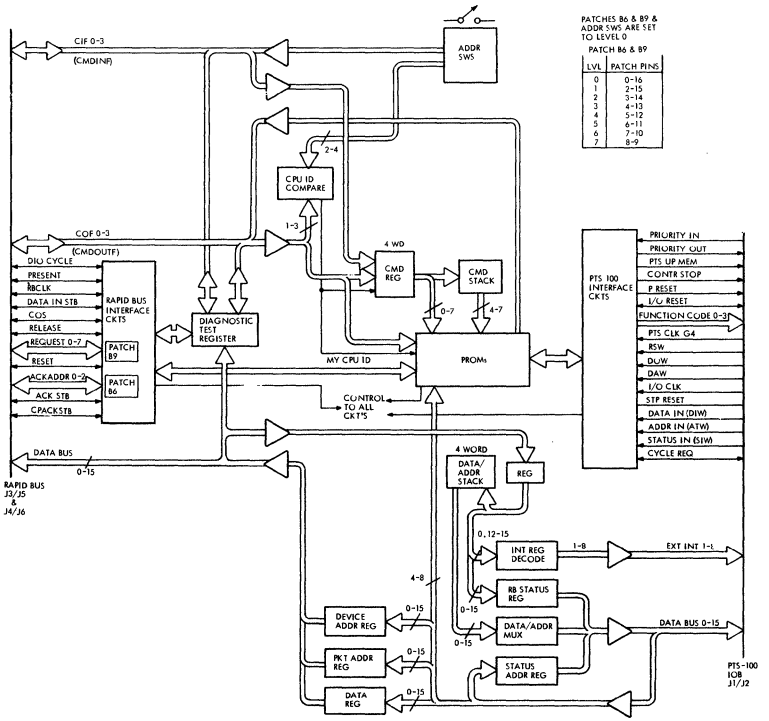


Figure 3-85. PTS-100 Rapidbus Interface Simplified Circuit Block Diagram

The device address, packet address, and data registers temporarily store their respective data from the PTS while it is awaiting transfer to rapidbus. The device and packet address registers handle the device and packet addresses during DIO and RIO instructions, and the data register handles the data and packet words.

The status address register stores the address from the PTS where the status will be stored during an RIO instruction. The RB status register stores the status received from the addressed rapidbus device during an RIO instruction. The data and address mux selects the data or addresses temporarily stored, one after the other, in the data and address stack (address 1, data 1; address 2, data 2; etc.) to ouptut to the PTS IOB. The interrupt register decodes, stores, and raises to the PTS any interrupts received from the rapidbus controllers until they are serviced, whereupon the interrupts are reset.

The COF and CIF circuits perform the same functions as for any other rapidbus interface. They inform the rapidbus controllers of DIO and RIO instructions and DMA read operations.

They inform the PTS RBI of DMA store, set/reset interrupt, and ready to receive DIO or RIO instruction operations.

The interface circuits receive the incoming interface signals, inform the PROMs of their arrival, and upon direction from the PROMs, initiate replies or requests to the interfaces.

The rapidbus interface signals are described in the RDS-500 Maintenance Manual 44-7669. The PTS interface signals are described in Section 1 of this chapter. Refer to the RDS Storage Module Controller Operation and Maintenance Manual, Raytheon Document Number 44-10147 for a description of the storage module controller and for a more detailed description of the PTS RBI.

The PTS RBI also contains a diagnostic register that permits the PTS RBI to be tested using the DIOC without a rapidbus controller connected (in which case terminators 930814G1 must be installed on the PTS RBI).

The following commands are used by the DIOC to access the test register. The address of the PTS RBI test circuit is 40_{16}.

1. READ WORD (1_{16})

   This command causes the RBI board to read the first word of the packet address, specified by this command, and store it in the test register.

2. WRITE WORD (2_{16})

This command causes the RBI board to write the word stored in the test register during CMD 1_{16} into the first word of the packet address specified by this command. If a different packet address is used, a comparison between both words can be made.

3. SET OR RESET INTERRUPT (3_{16})

This command causes the RBI board to set or reset interrupts depending on what bits are set in the packet address associated with this command. Bits 11-14 specify the interrupt level. If Bit 15 is a "1," the interrupt will be set. If Bit 15 is a "0," the interrupt will be reset.

3.2.25 Display Adapter Memory (DAM) Operation

The DAM (Figure 3-86) provides all the combined functions of the display adapter and memory boards. In addition, the DAM provides byte parity checking and optional 4K display memory buffers.

The DAMs come with 16K, 32K, or 65K byte memories, depending upon the model and type. There are two DAM models: DAM 1, which has a 16K memory, and DAM 2 which has a 16K, 32K, or 65K memory. DAM 1 and the 16K DAM 2 are interchangeable. See Figure 3-87 for the DAM simplified circuit block diagram.

3.2.25.1 Memory. The DAM memory has two ports; one for the processor and one for display refresh. It uses either 4K or 16K by 1 N-channel MOS RAMS. A DAM board can hold a maximum of 16K using 4K chips, or 65K using 16K chips. Since a DAM can contain more than 16K of memory, the board addressing is switch selectable. The DAM looks at combinations of address lines AO, HO, and MEMSEL to determine address selection. Byte parity is generated and checked on the board. This option can be disabled by a switch on the DAM. Since the memory is MOS, it requires refresh every 2 ms to maintain the data.

The memory is organized as two columns by 18 rows of 4K or 16K storage locations. To conserve power, the column not addressed during an operation other than refresh remains in a low power standby mode. Also, when not busy, the memory remains in the standby mode.

The memory accesses either or both bytes during write operations, but only a complete word during read operations.

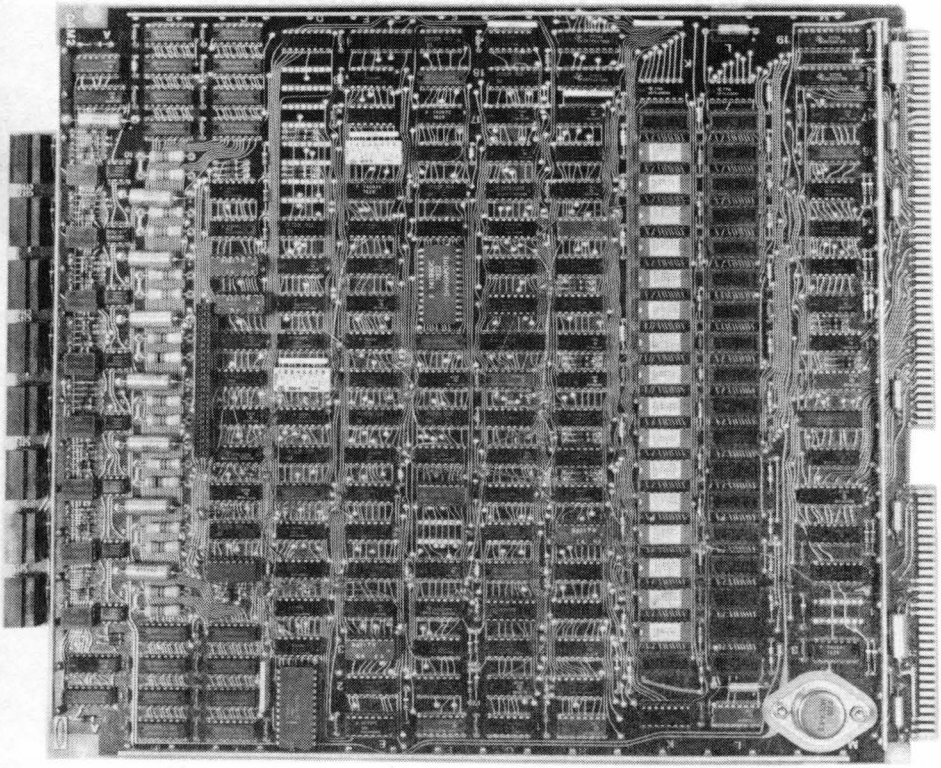


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Figure 3-86. DAM 2

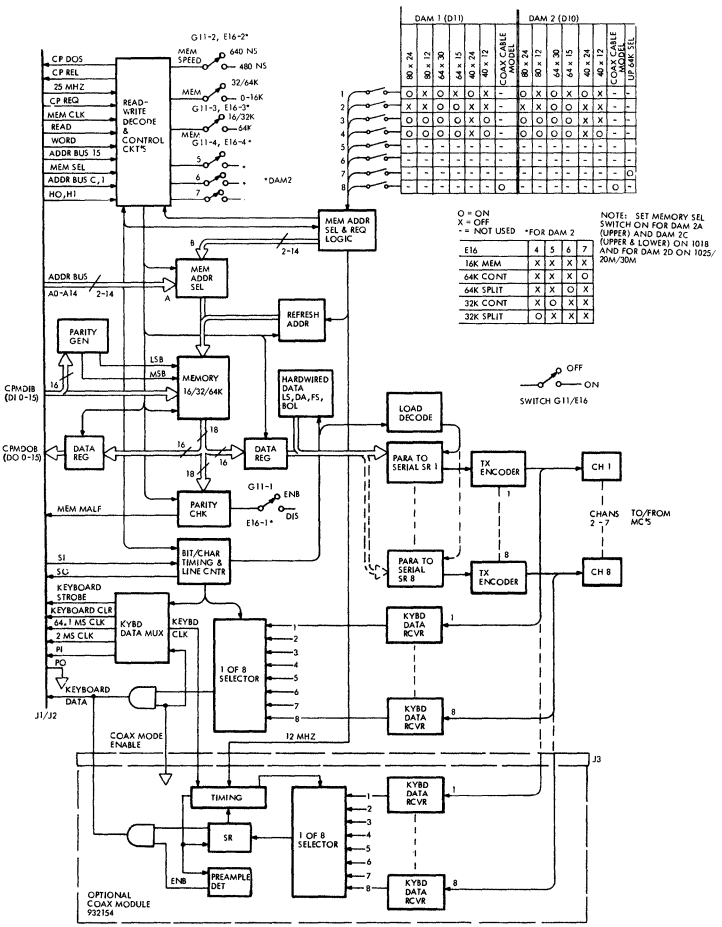


Figure 3-87. DAM Simplified Circuit Block Diagram

Memory refresh is performed entirely on the DAM. A refresh cycle, which takes 480 ns, is executed twice every 64.1 μs for 4K chips and four times every 64.1 μs for 16K chips. The memory addressing, refresh, etc., is basically the same as for the standard memory boards. Refer to Section 3.2.3 for a description of the memory operation.

The memory cycle time of the processor is switch selectable on the DAM for either 480 or 640 ns. However, the processor memory cycle time can be forced to 800 ns by a switch on the 1018 backplane or by the multiplexer.

The memory to processor interface is the same as that for the standard memory boards except that a memory malfunction and memory select address lines have been added. The memory select line is used in systems with memories greater than 65K bytes. It permits either the upper or the lower 65K bytes of memory to be addressed. A DIP switch on the DAM 2 is set or reset to indicate whether or not the DAM is in upper or lower memory. The memory malfunction line is used by the DAM to inform the processor of parity errors. When a parity error is detected, the processor completes the current instruction and enters the interrupt sequence. Level 10 is set, status saved, and the PC is loaded from the level 10 interrupt packet. In level 10 no external interrupts can be serviced; however, traps and other parity error interrupts can be serviced.

3.2.25.2 Display Refresh. Data to refresh the displays is only stored in the upper 16K bytes of the DAM memory. This upper area (all of memory on 16K DAMs) is proportioned to each monitor controller port, with either 2K or 4K (DAM 2 only) assigned to each of the eight ports. The 2K or 4K buffer assignments are made with DIP switches on the DAM 2 board. The display buffer assignments are shown in Table 3-21. A further breakdown of the 2K buffers is shown in Tables 3-13 and 3-14.

The circuits that move the display data from DAM memory to the monitor controllers are similar to those used on the standard display adapter. Bytes of display data are read out of memory and are sent to eight parallel-to-serial shift registers, one for each port to the MCs. The shift registers are loaded one at a time under control of the timing circuits. The timing circuits also load hardwired data into the shift registers to insert line and frame sync, device address, and end of line characters into the data stream.

The characters in the shift registers are then serially shifted out to their respective MCs. Refer to Figures 3-31 through 3-36 for the data stream formats. The formats are controlled by DIP switches on the DAMs. See Figure 3-87 for the switch settings.

Table 3-21. DAM Display Buffer and Keyboard Address Assignments

DISPLAY BUFFER AND KEYBOARD ADDRESS
DAM 2K SCREEN BUFFERS

DA CHANNEL	DAM #1 BUFFER ADDRESS	DAM #1 KEYBOARD ADDRESS	DAM #2 BUFFER ADDRESS	DAM #2 KEYBOARD ADDRESS	DAM #3 BUFFER ADDRESS	DAM #3 KEYBOARD ADDRESS	DAM #4 BUFFER ADDRESS	DAM #4 KEYBOARD ADDRESS
1	0000-07FF	81	4000-47FF	82	8000-87FF	83	C000-C700	84
2	2000-27FF	85	6000-67FF	86	A000-AFFF	87	E000-E7FF	88
3	0800-0FFF	89	4800-4FFF	8A	8800-8FFF	8B	C800-CFFF	8C
4	2800-2FFF	8D	6800-6FFF	8E	A800-AFFF	8F	E800-EFFF	90
5	1000-17FF	91	5000-57FF	92	9000-97FF	93	D000-D7FF	94
6	3000-37FF	95	7000-77FF	96	B000-B7FF	97	F000-F7FF	98
7	1800-1FFF	99	5800-5FFF	9A	9800-9FFF	9B	D800-DFFF	9C
8	3800-3FFF	9D	7800-7FFF	9E	B800-BFFF	9F	F800-FFFF	A0

DAM- 16K OR 32K SPLIT (16K UPPER 16K LOWER MEMORY)
WITH 4K SCREEN BUFFERS

1	0000-0FFF	81	4000-4FFF	82	8000-8FFF	83	C000-CFFF	84
2	N/A		N/A		N/A		N/A	
3	2000-2FFF	85	6000-6FFF	86	A000-AFFF	87	E000-EFFF	88
4	N/A		N/A		N/A		N/A	
5	1000-1FFF	91	5000-5FFF	92	9000-9FFF	93	D000-DFFF	94
6	N/A		N/A		N/A		N/A	
7	3000-3FFF	95	7000-7FFF	96	B000-BFFF	97	F000-FFFF	98
8	N/A		N/A		N/A		N/A	

DA CHANNEL	DAM 32K CONTINUOUS OR 64K SPLIT (32K UPPER 32K LOWER MEMORY) WITH 4K SCREEN BUFFERS: BUFFER ADDRESS	KEYBOARD ADDRESS	DAM 64K CONTINUOUS WITH 4K SCREEN BUFFERS: BUFFER ADDRESS	KEYBOARD ADDRESS
1	0000-0FFF	81	8000-8FFF	83
2	4000-4FFF	82	C000-CFFF	84
3	2000-2FFF	85	A000-AFFF	87
4	6000-6FFF	86	E000-EFFF	88
5	1000-1FFF	91	9000-9FFF	93
6	5000-5FFF	92	D000-DFFF	94
7	3000-3FFF	95	B000-BFFF	97
8	7000-7FFF	96	F000-FFFF	98

1018

CONFIGURATION	1	2	3	4	5	6	7	8*	9	10	11	12	13	14	15
MEMORY MODE	64K								128K						
MEMORY SIZE (K)	16	32	48	64	32	48	64		80		96		112	128	
DAM A11				1/2			1/2		3		3		3	7	
BOARD A10			1/2	1/2		1/2	1/2		3	3	3	7	7	7	
LOC A9		1/2	1/2	1/2	4	4	4	6	3	7	7	7	7	7	5
A8	1/2	1/2	1/2	1/2					7	7	7	7	7	7	6
DISPLAY MEM (K)	16-	32-	48-	64-	16	32	48	16	64	48	64	48	64	64	64
PROGRAM MEM (K)					16	16	16	48	16	32	32	48	48	64	64

1015M

	1	2	5
	32K		
	16	32	32
A11			
A10			
A9		1/2	4
A8	1/2	1/2	
	16-	32-	16
			16

1008

	30	31	32
	64K		
	16	32	64
A4			
A3			
A2	1/2	4	5
A1			
	16-	16	16
		16	48

1025/1020M/1030M

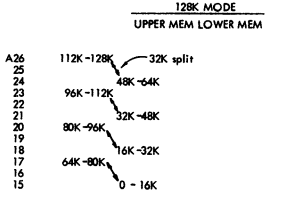
CONFIGURATION	16	17	18	19	20	21	22	23	24	25	26	27	28	29
MEMORY MODE	64K				128K			128K			128K		128K	
MEMORY SIZE (K)	32	48	64		80			96			112		128	
A26			1/2		2					1/2			1/2	7
A25														
A24									1/2					
A23		1/2	1/2		2	2			1/2	1/2	1/2		1/2	7
DAM A22														
BOARD A21														
LOC A20	1/2	1/2	1/2		2	7		1/2	7	7	1/2		1/2	7
A19														
A18												5		
A17	1/2	1/2	1/2	5	7	7	1/2	1/2	7	7	1/2	5	1/2	7
A16														
A15							5	5			5		5	
DISPLAY MEM (K)	16	32	48	32	64	48	16	32	48	64	64	64	64	64
PROGRAM MEM (K)	16	16	16	32	16	32	64	64	48	32	48	64	64	64

KEY

1. DAM I 932102 16K Continuous Lower†
2. DAM IIA 932316G1/G3 16K Continuous Lower †
** 3. DAM IIA 932316G1/G3 16K Continuous Upper †
4. DAM IIB 932316G4/G6 32K Continuous Lower †
5. DAM IIC 932316G7/G9 64K Continuous Lower †
** 6. DAM IIC 932316G7/G9 64K Continuous Upper †
7. DAM IID 932316G4/G6 32K 16K Upper/16K Lower (split)†

NOTES:

DAM2 MEMORY SLOT ASSIGNMENTS 1025/1020M/1030M



1. A DAM2 board must always be in A20 or A17 for clocks.
2. 16K DAM. Provides 16K to installed slot.
3. 32K split. Provides 16K to installed upper memory slot and 16K to associated lower memory area indicated by diagonal arrow.
4. 64K continuous. Provides 16K to installed slot and the remaining 48K to the next 3 lower continuous memory areas.

ON CONFIGURATION 8 SET BACKPLANE SWITCH S3 TO THE 64K POSITION. SET SWITCH TO 128K POSITION FOR ALL

** SWITCH D10-7 ON

†UPPER — SEB INSTRUCTION IS USED FOR ACCESS
LOWER — NO SEB INSTRUCTION NECESSARY

Figure 3-88. DAM 2 Backplane Locations

3.2.25.3 Keyboard Data Circuits. These circuits are the same as those for the standard display adapter described in Section 3.2.6.3.

3.2.25.4 Coaxial Cable Adapter. The coaxial cable adapter operates in the same way as the coax adapter for the standard display adapter except that the receiver and control circuits are on one board instead of two. Refer to Section 3.2.6.6 for the adapter operation.

3.2.25.5 DAM 2 Backplane Locations. The DAM 2 boards are installed into the backplanes as shown in Figure 3-88.

3.2.26 Asynchronous Data Processor (ADP) Operation

The ADP (Figure 3-89) is a microprogrammed high speed specialized processor that is presently used with the PTS/1200 for 3270 concurrency where it performs CRC generation and search and translate functions. The ADP moves and/or operates on the data in memory. It can move; move and modify; search; translate and calculate CRCs, and in general, it can perform these functions faster than the PTS-100 processor, since it does them in hardware rather than with software.

The ADP receives instructions from the program via I/O packets (PIOT), executes the packets, and returns status and results to the program.

The ADP is mounted on one half of a single full size plug-in PC board. The remaining half is a motherboard, which can accommodate one quarter or half board I/O adapter.

3.2.26.1 Interfaces. The ADP interfaces with the IOB, and the motherboard portion interfaces with the multiplexer I/O bus. Both of these interfaces are described in Section 1 of this chapter.

3.2.26.2 Status and ICB. The ADP has an 8-bit ICB register and a 2-bit status register. Both registers are in the RAM. The two status bits define ready (bit 0-1) and busy (bit 1-1) conditions with a '0' in both indicating that the ADP is not available.

The ICB bits (Interrupt Condition Bits) inform the program of interrupt conditions. The ICB bits are defined in Table 3-7. Whenever a bit is set, the interrupt mask from the PIOT, which is stored in the ADP, is ANDed with the ICB to determine if the present order (operation) should be terminated and an interrupt generated.

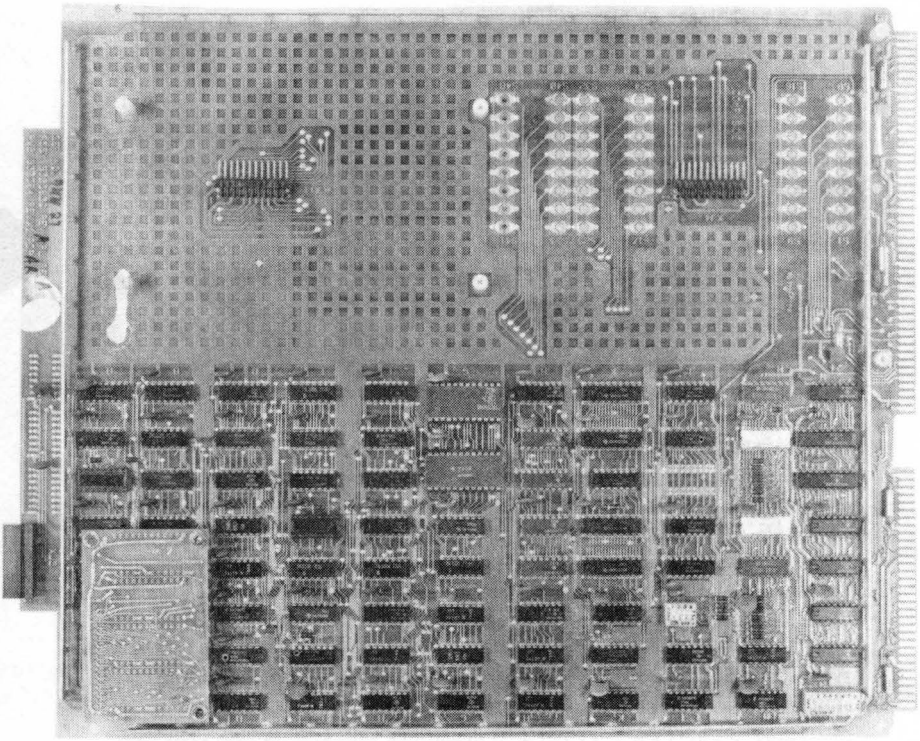


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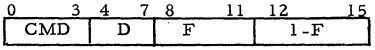
Figure 3-89. Asynchronous Data Processor

3.2.26.3 Circuit Description

A. Initialization

The ADP simplified block diagram is shown in Figure 3-90. The ADP responds to two basic instructions from the processor: DO I/O, to start or stop an I/O operation; and Read I/O, to read or read and reset status. (See Section 1 of this chapter.) The processor places these instructions on the IOB data bus in addition to the address code for the ADP. The address recognized by the ADP is switch selectable. The AC word of the instruction has the following format:



The other instruction words are the same as those shown in Section 3.1.9.

After putting the instruction word on the IOB, the processor raises DAW to identify the word as address information. For a start DIO instruction, the processor next puts the effective address (EA) of the Instruction packet (PIOT) on the data bus and raises DOW. The ADP decodes the ADP address and queues the interface circuits to accept the EA. Condition bits DOIO and IOB03 are sent to the microprogram in PROM (via the ALU and PC) to tell it that a start DIO command has been received (bit 3 is '1'). The microprogram then directs the ADP to accept the EA and store it in RAM. The RAM has dedicated locations for the EA, status, ICB, packet words, data, etc.

After the EA is in the RAM the ADP takes control of the I/O operation, requesting the packet words and storing them in RAM. The packet format is shown in Figure 3-91.

B. Microprogram PROM, PROM Decode, Program Counter, & Test Branch Mux.

The microprogram that directs the operation of the ADP circuits resides in the PROM. The PROM consists of two 512 x 8 word chips that are mounted on a piggyback module plugged into connector J6.

The program counter addresses the microinstructions in the PROM. It is loaded from PROM bits 5-15 during a test branch instruction when one of the ALU bits is set (selected by test branch mux) or during a branch when the ALU outputs are either all 0's or all 1's (C Bit).

The bits in the addressed microinstruction are decoded by the PROM Decode, which directs the various ADP circuits to perform their assigned tasks when the associated microinstruction bits are set.

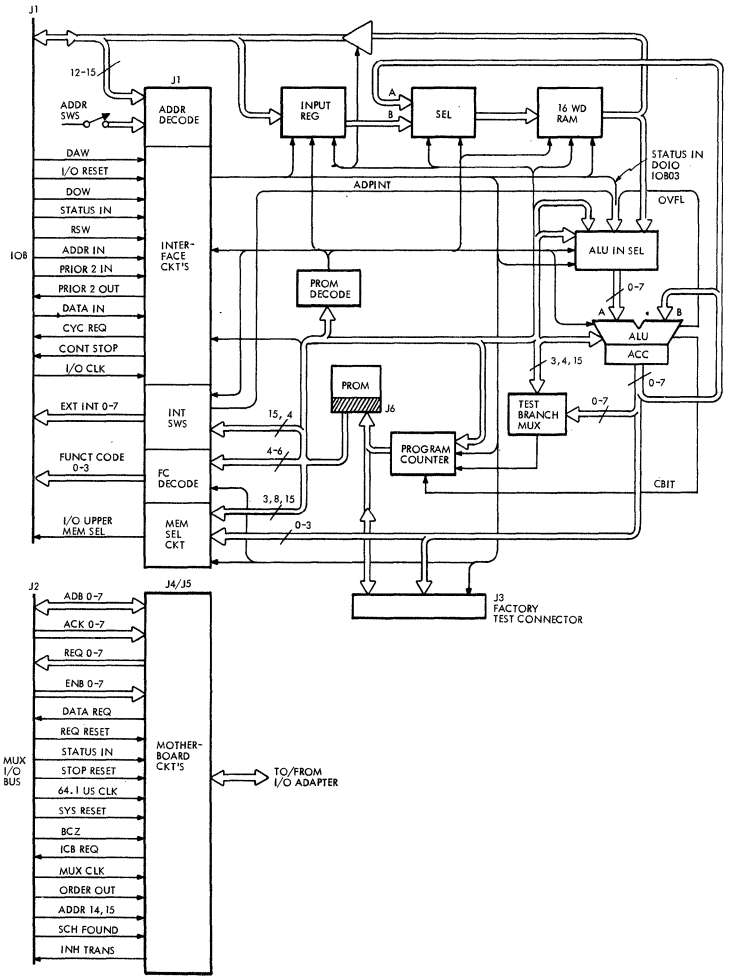


Figure 3-90. ADP Simplified Circuit Block Diagram

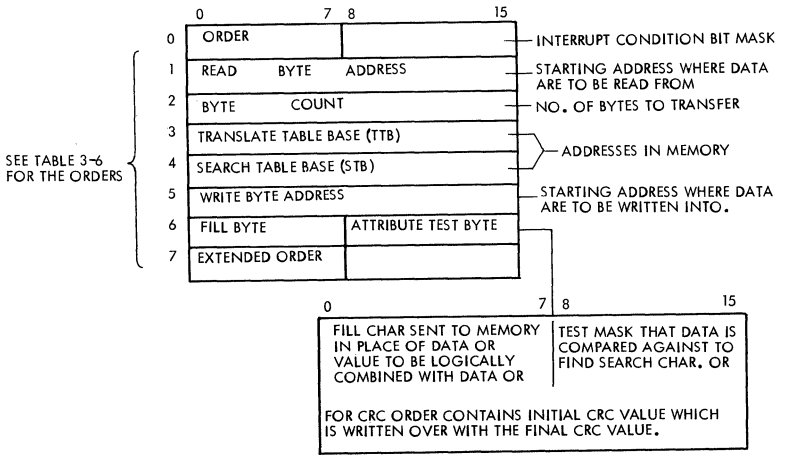


Figure 3-91. ADP Instruction Packet

C. RAM Circuits

All the data to and from the ADP passes through the RAM. The RAM can store up to 16 words. It stores the packet, status, ICB, data, etc. It is loaded either from the ALU or from the IOB via the input register, and it can write to either the IOB or ALU.

D. ALU and Upper Memory Select Circuits

The ALU performs logical and move operations under control of the microprogram. The ALU A operand is selected by the ALU input selector and the B operand is from the accumulator register, which is part of the ALU chip. The accumulator termporarily stores the ALU output. The accumulator output is applied to the ALU input selector, the RAM, test branch mux, test connector J3, and the upper memory select decode circuit.

The memory select circuits decode ALU bits 0-3 and ROM bits 3, 8, and 15 to determine when the microprogram wants to do a DMA access to upper memory.

E. Interrupt, Function Code and Interface Circuits

The level on which the processor is interrupted is switch selectable. Tne interrupt is controlled by bits 15 and 4 of the microinstructions and by

the output of the PROM decode. When an interrupt is activated, ADPINT is sent to the ALU to flag the microprogram and at RSW the interrupt is gated out to the IOB.

Also at RSW the function code generated by decoding microinstruction bits 4-6 is gated out to the IOB.

The remainder of the interface circuits coordinate the transfer of data across the IOB interface. They are under control of the microprogram, and they flag the microprogram to events on the interface with STATUS IN, DOIO, and IOB03.

3.2.27 Synchronous Data Link Control (SDLC) Adapter Operation

The SDLC adapter (Figure 3-92) is a microprogrammed I/O adapter that interfaces the PTS low speed multiplexer to a 3270 SDLC communication link. It is mounted on a single full size plug-in PC board and it connects to two PTS multiplexer ports, one send and one receive. The SDLC link is RS-232, synchronous up to 9600 baud, full duplex, NRZ, or NRZI (modem provided clock) with 8-bit characters.

The SDLC adapter receives its microprogram and its instructions via I/O packets (PIOT) from the program (for the PIOT see Figure 3-12). It loads its microprogram, executes the instruction packets, and returns status to the program.

3.2.27.1 Interfaces. The SDLC uses the low speed multiplexer interface, which is described in Section 1 of this chapter. Refer to Figure 2-3 for the modem cable and to Appendic C for a description of the modem lines.

3.2.27.2 Status and ICB. The SDLC has 8-bit status and ICB registers for both the transmit and receive ports. The registers are in RAM. The meanings of the status and ICB bits are given in Table 3-22.

3.2.27.3 Orders. Each of the orders used by the SDLC are described below. The SDLC data frame format to/from the modem is shown in Figure 3-93.

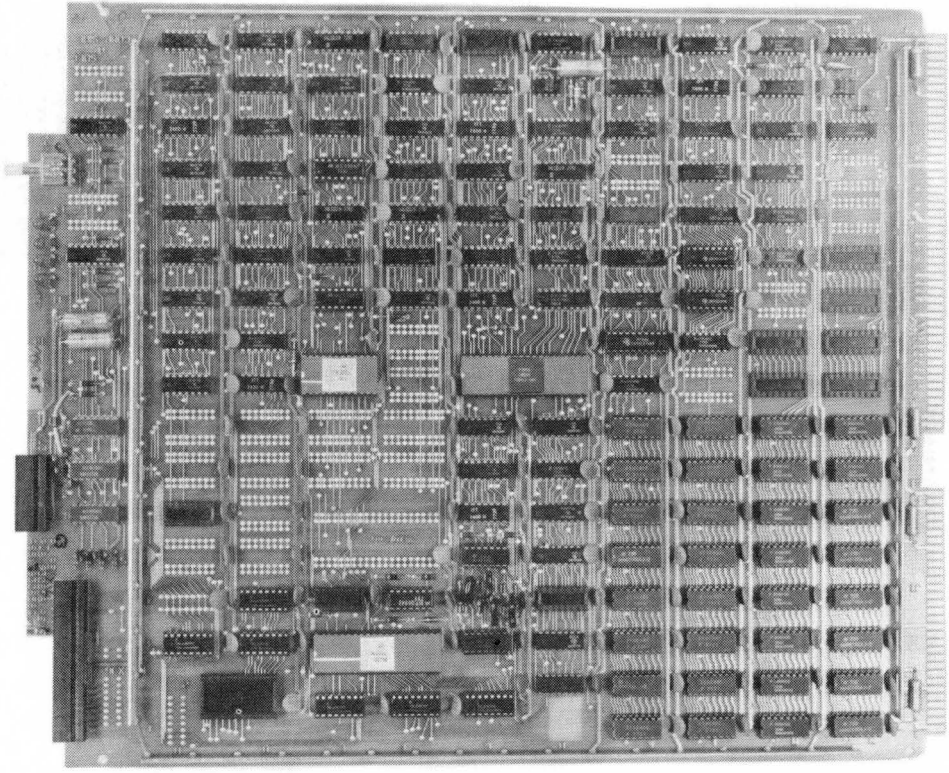


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Figure 3-92. SDLC Adapter

Table 3-22. SDLC Status & ICB

Transmit Status		Transmit ICB	
BIT	Meaning When Bit = Logic "1"	BIT	Meaning When Bit = Logic
0	Adapter is ready for a new transmit order.	0 1 2	These bits have the same meaning as their receive counterparts.
1	Adapter is busy processing a transmit order	3	The transmit frame check sequence order is being processed and another order can be sent to this adapter.
2	--		
3	--		
4	--	4	--
5	The adapter has received a Transmit Flags order.	5	An underflow occurred because there was no character to transmit.
6	--	6	The clear RTS or Transmit abort order has terminated. Termination means the last bit of the frame has been transmitted.
7	An error occurred during execution of the load microcode.	7	The load microcode order has terminated.

Read Status		Read ICB	
BIT	Meaning When Bit = Logic "1"	BIT	Meaning When Bit = Logic "1"
0	Adapter is ready for a new receive order.	0 1 2	Generated by the MUX " " " "
1	Adapter is busy processing a receive order.	3	The ending flag of the frame has been detected.
2	The last continue transmit order ended after NO DATA character had been inputted.	4	The receiving of data has been terminated because: 1. Lack of a receive order prevents inputting of characters to main memory and this adapter receive data registers are full. 2. The order being processed was terminated because the maintenance pushbutton was pressed. 3. The receive carrier has been lost. The adapter will accept search for flag or flag address order after carrier lost. After receipt of one of these orders, the adapter waits for carrier to change from a no carrier to carrier
3	The Frame Check Sequence character did not compare with the computed value indicating one or more of the fields checked is in error.		
4	The modem Data Carrier Detect line indicates carrier is being received.		

Table 3-22. SDLC Status & ICB (cont)

Read Status		Read ICB	
BIT	Meaning When Bit = Logic "1"	BIT	Meaning When Bit = Logic "1"
			present condition and then starts looking for frame sync.
5	The present order terminated because the adapter entered the maintenance mode.	5	--
6	A one indicates there is a high probability that the data contains errors.	6	Abort character was received.
7	--	7	--

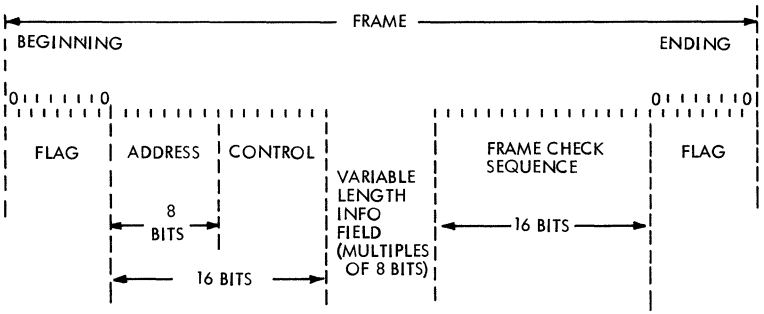

Figure 3-93. SDLC Frame Format

A. Receive Orders

SFG - SEARCH FOR FLAG

Adapter searches for frame sink then transfers Address, Control, and Information fields to the processor. The Frame Check Sequence character is checked and ICB and Status Bits report on the validity of the frame.

SFA - SEARCH FOR FLAG AND ADDRESS

Same as the SFG command except the Flag and Address (Station) characters are found before the adapter transfers any characters to the MUX. The received address character is compared against 8 address characters sent to the adapter from the program during an LMC command.

CONR - CONTINUE RECEIVE

After the receive logic is started using the SFG or SFA command and after any ICB conditions which do not terminate receive, this command is used to continue the receive operation.

B. Transmit Orders

XFR - TRANSMIT FRAME

Used to start transmitting a frame. When RTS is raised to the modem and the modem returns CTS, transmission begins with a flag character. The address character becomes the first character requested from the MUX and these requests continue until the XFCS command follows a BCZ condition. Only a CONX can be used between the XFR and XFCS commands.

XFCS - TRANSMIT FRAME CHECK SEQUENCE

Used to stop the adapter from requesting data and to terminate the frame. This order terminates with an End of Frame ICB condition, when the Frame Check Sequence and Flag Character are being generated and transmitted. If no other order is sent to this adapter between the End of Frame termination and the transmission of the last bit of the Flag character, Flag characters will continue to be transmitted until the next order.

XFLG - TRANSMIT FLAGS

Causes the adapter to transmit continuous flags. Each time an 8-bit flag is transmitted, a request is made to the MUX. The requests will stop at BCZ, but RTS will remain high and the 8-bit flag characters will continue to be transmitted. This order is used to generate program timeouts and none of the data characters requested are transmitted.

CRTS - CLEAR REQUEST TO SEND

Used to remove the carrier from the communication line after one or more frames have been transmitted.

CONX - CONTINUE TRANSMIT

After the frame is started with an XFR command, this command is used to continue transmitting data characters.

XABT - TRANSMIT ABORT

Causes the special, all ones abort/character to be transmitted and the frame to be terminated.

C. Receive and Transmit

Stop Order

This command stops both the transmit and receive sections of the adapter. It is sent to the receive port address in the DIO STOP IO instruction.

D. Load Microcode Order (LMC)

Refer to Section 3.2.27.4A for a description of this order.

3.2.27.4 Circuit Description

A. Initialization

The SDLC adapter simplified block diagram is shown in Figure 3-94. The SDLC contains two types of microprogram memory: a RAM and a PROM. The RAM is used to store the microprogram that controls the SDLC operation, while the PROM contains a bootstrap loader program. When any reset occurs the PROM program examines the contents of the RAM to see if it has been previously loaded. If it has, the microprogram in RAM is allowed to begin execution. If the RAM is found to be not loaded, the bootstrap loader waits for an LMC order, whereupon it directs the loading of the microcode into the RAM.

All orders are initiated by DIO instructions and I/O packets as described in Section 3.1.9. When an LMC order is received, the microcode is loaded into RAM from main memory.

The LMC order permits any amount of microcode to be loaded from any memory address. This is accomplished by preceding the microcode with a 5-byte header, which contains a longitudinal redundancy check character, the starting memory address of the microcode in main memory, and the address where execution will start in the microcode.

During microcode loading the PROM program calculates its own LRC and compares it to the LRC from the header to determine if the microcode is error free. The program to send the LMC order and the RAM microcode are loaded into main memory from cassette prior to loading the application program.

When the microcode is correctly loaded, the application program from cassette is loaded over the LMC program in main memory. The application program then uses the SDLC microcode to transmit and receive over the SDLC communication line.

B. 16 Byte RAM

All the data to and from the SDLC adapter passes through this RAM. The RAM can store up to 16 bytes of data, and it temporarily stores the packet, status, ICB, and data. It is loaded from the microprogram RAM, the bootload PROM with receive data from the 6852, or from the IOB. It can write to the IOB, the 6800 microprocessor, or the 6852 synchronous serial adapter.

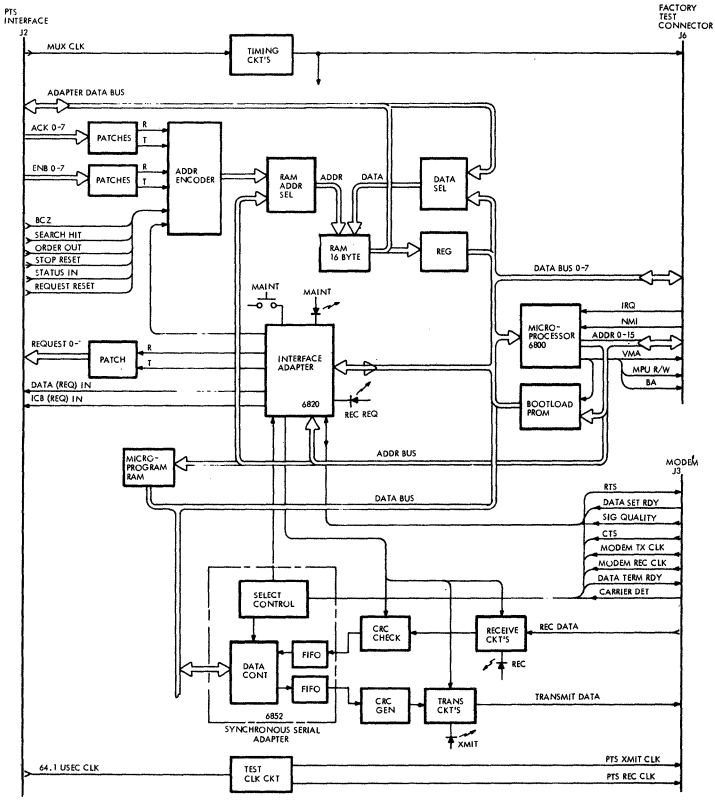

Figure 3-94. SDLC Simplified Circuit Block Diagram

C. RAM Address Selector

The RAM address selector selects either the microprocessor or the address encoder to address the RAM. The configuration of the active signals applied to the encoder determine the RAM address. (Two ACK and ENB signals are selected by the patches and applied to the encoder because the SDLC uses both a transmit and a receive port.)

D. Bootload PROM, Microprogram RAM, and Microprocessor

The bootload PROM (512 x 8) contains the program to bootload the microprogram RAM. The microprogram RAM (4Kx8) holds the microprogram that controls the SDLC adapter. An executive routine in the microprogram looks for tasks and branches to subroutines to perform the tasks. The microinstructions in the RAM are addressed by the microprocessor which provides the program counter function. The microinstructions are applied to the microprocessor, the 6820 interface adapter, and the 6852 synchronous serial adapter. The microprocessor operates on the microinstruction from both the RAM and PROM to produce various addresses (PC, RAM, 6820 and memory) and flags (to the 6820). It also monitors various flags (via the data bus) from the 6820 and notifies the microprogram of their occurrences.

E. Interface Adapter 6820

The interface adapter provides two general functions: it decodes the microinstructions to set various control signals (Request, Data In, ICB in, CRC, and Input/Output Control) and it monitors various flags. Both the control signals to be set and the flags to be monitored are selected by the bit configuration on address bus.

F. Synchronous Serial Adapter 6852, CRC

The 6852 is a bidirectional serial interface for simultaneous synchronous data transmission and reception. It performs serial-to-parallel (receive) conversion; parallel-to-serial (transmit) conversion; zeros insertion and deletion; frame check sequence generation and checking; start of frame detection; abort detection and generation; and NRZ/NRZI reception and generation. The functional configuration of the 6852 is programmed via the data bus during adapter initialization.

CRC generation and checking is performed by the CRC circuits on the transmitted and received data. LEDs in the transmit and receive input/output circuits illuminate to indicate the movement of data.

G. SDLC Maintenance Aids

The SDLC adapter has four LEDs and a maintenance switch that are used to check the operation of the SDLC microcode and hardware. The

diagnostic does not have to be loaded to use this facility nor does the application program have to be loaded after the checks are made.

During on-line operation the four LEDs are automatically switched on once every 30 seconds. Then they individually extinguish as their associated signals occur. The REC LED extinguishes when data is received from the modem; the REC REQ LED extinguishes when any request is made to the PTS main program; and the XMIT LED extinguishes when data is sent out to the modem. If the REC LED fails to extinguish it indicates that:

1. the modem is not connected or
2. the receive data is not changing state.

If the REC REQ LED fails to extinguish it indicates that the

1. microcode is not loaded
2. no polling from modem
3. PTS program is not sending receive orders, or
4. no receive data is being sent to the PTS program

If the XMIT LED fails to extinguish, it indicates that

1. no transmit order from PTS program
2. no CTS or
3. the transmit data to the modem is not changing state.

When the MAINT pushbutton switch is depressed all LEDs light, on-line operation is terminated with ICB bits set, the SDLC status goes ready and not busy until the maintenance period is over (all LEDs extinguished), and the SDLC adapter sends no data to the PTS and the modem. The switch may have to be held down for a short period of time to get the LEDs to light and start the maintenance period. When the maintenance period is started, the SDLC adapter issues pseudo receive and transmit orders to itself. It executes the orders just as if they were from the PTS main program. If the host is polling on the modem line, the receive data is handled as usual except that it is not sent over the interface to the PTS main program. Instead the data is looped back to the transmit circuits to the modem, but it is not sent out to the modem. In this mode the LEDs extinguish to indicate proper operation just as they did in the on-line mode. The only difference is that in this case the MAINT LED is lighted while the unit is in the maintenance (off-line) mode.

After the maintenance mode is terminated, the PTS application program will issue orders to restart SDLC adapter.

3.2.28 IPARS Controller (1001/A) Operation

The IPARS Controller is a microprogrammed, standalone, single board controller that contains all the electronics, except the power supplies, for the PTS 1001/A display system.

There are two versions of IPARS controller; one for the PTS 1001 (930452) and one for the PTS 1001A (932363). Both versions support a modem, two printers, and either a single display (1001) or up to four displays (1001A).

IPARS Controller 930452 is shown in Figure 3-95. Refer to Section 4.11 for PTS 1001/A testing.

3.2.28.1 Circuit Description The IPARS controller contains a microprocessor, RAM and PROM memories, modem and printer interfaces, and monitor controller circuits. Refer to Figures 3-96 and 3-97 for the simplified block circuit diagrams.

Note that the addresses for RAM and PROM memories and data and control registers are shown on the diagram. When the processor or other circuit puts one of these addresses on the address bus, that associated memory location or register is read from or written into.

A. Microprocessor, Interrupts, and Address Decoder

The processor is a 6800 LSI single chip microprocessor that contains an ALU, PC, and various other registers. It controls the operation of the display system under direction of the program stored in PROM. The processor has access to all the device interfaces including the keyboard and cursor registers and to the PROM and RAM memories (on the 1001A the PROM uses a separate bus). The processor does not get directly involved in the transfer of display refresh data.

The device interfaces (modem, printer, cursor-1001 only-and keyboard) all interrupt the processor when they want service. When interrupted the processor completes the current instruction, stores all internal registers, reads the interface registers to see which one has the interrupt bit set, and fetches the interrupt routine from PROM for that interrupt. This routine makes the appropriate response to service the device.

The address decoder decodes the address from the processor and enables the addressed device interface (including RAM and PROM) to communicate with the processor. After the device is serviced, the processor reloads its registers and continues operation where it previously left off before the interrupt.

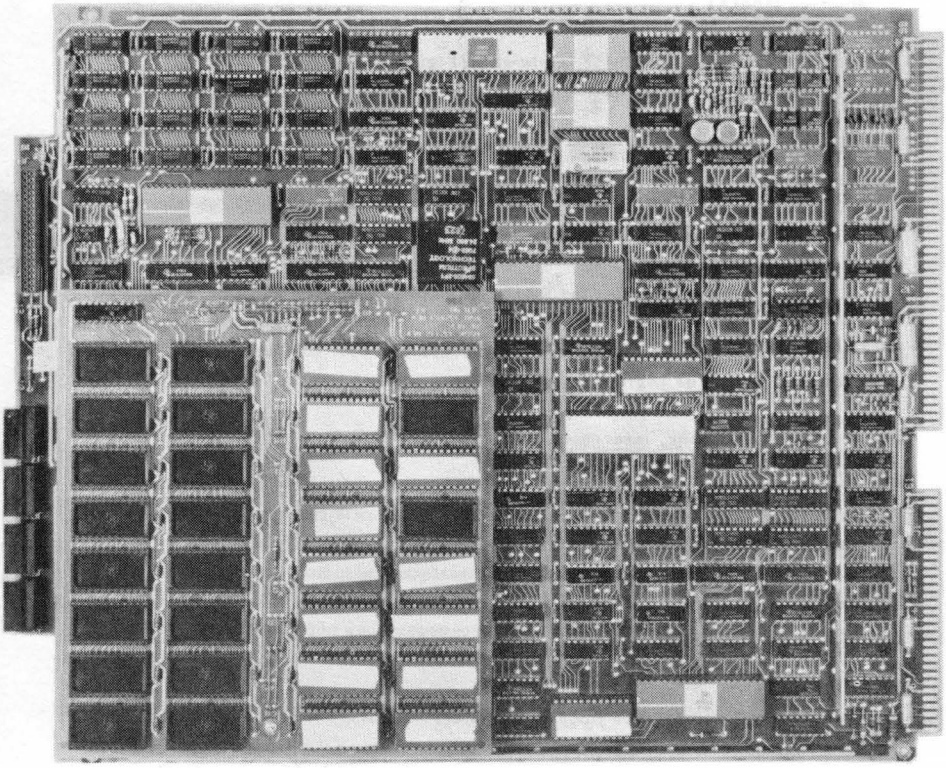

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Figure 3-95. IPARS Controller 930452

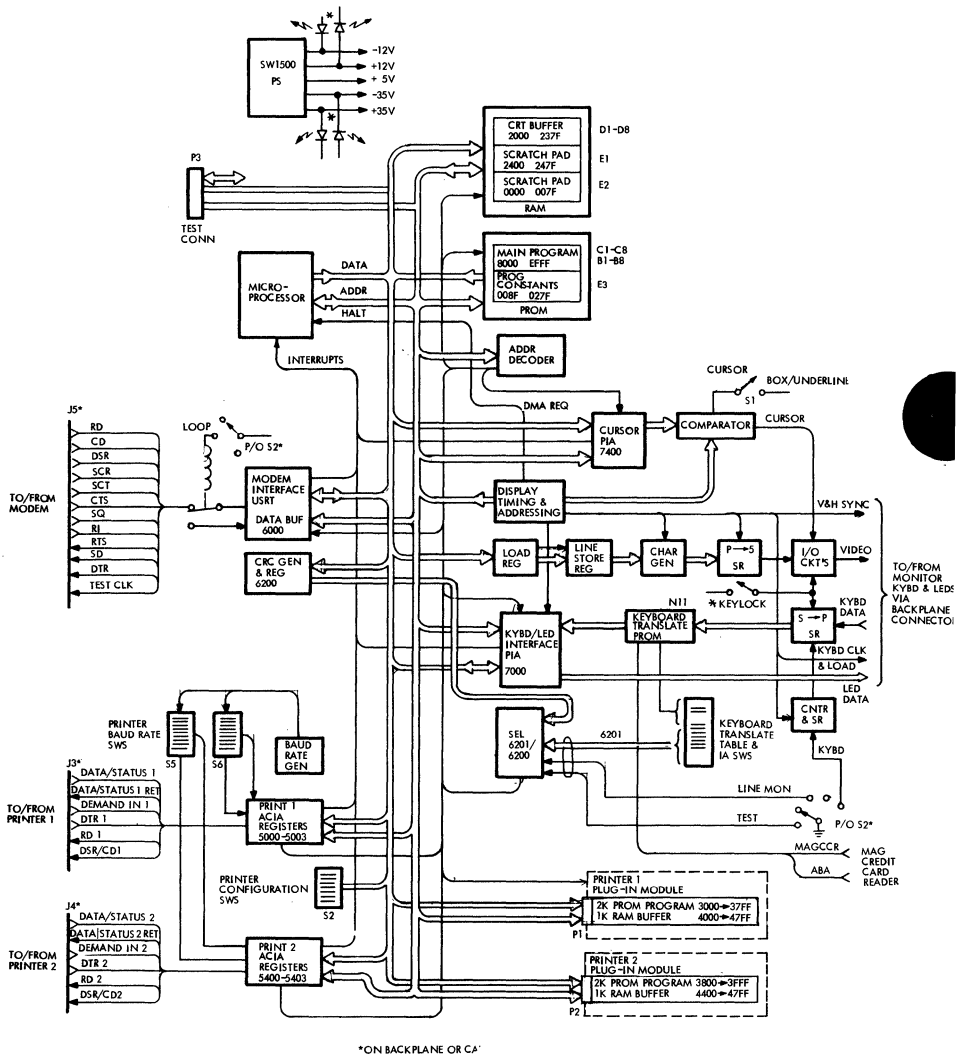


Figure 3-96. IPARS Controller (1001) Simplified Circuit Diagram

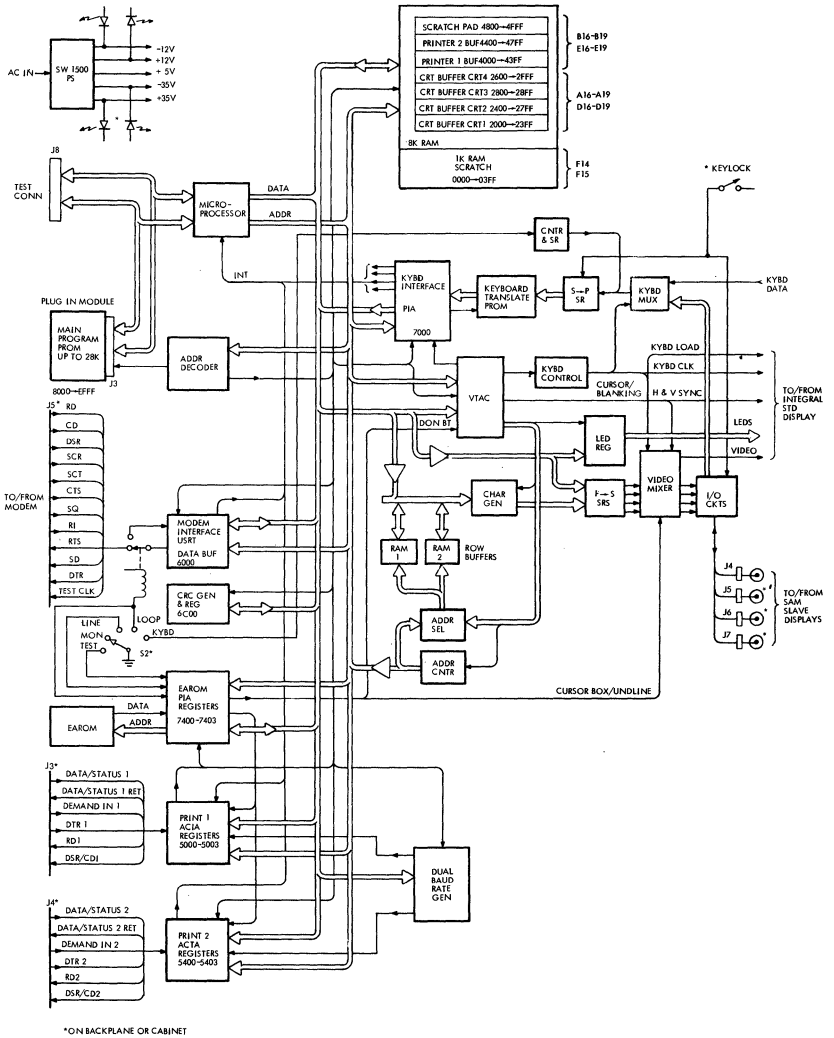


Figure 3-97. IPARS Controller (1001A) Simplified Circuit Diagram

When the monitor controller circuits in the 1001 want to fetch display refresh data from RAM, they raise DMA REQ to halt the processor. Then they read a full line of characters in a burst from the RAM CRT buffer before allowing the processor to continue.

On the 1001A the address decoder flags the monitor controller circuits whenever the processor is addressing PROM or an internal register. During this time the monitor controller circuits are allowed to fetch a single character of display refresh data from the RAM CRT buffers. Thus display refresh does not effect the processor overhead.

B. PROM

The PROM memory contains the main program. It is permanent storage and cannot be changed without changing the PROM chips. Up to 28K bytes of PROM can be installed in the locations assigned to main program, 8000-EFFF; however, the standard IPARS program only occupies the top 8K (DOOO-EFFF). The remainder of the PROM locations are not used in the IPARS application. In the IPARS controller for the 1001, there are three other PROMS: one stores program constants (008F - 027F), and the other two store the printer programs for their associated printer interfaces. These last two PROMs are located on separate printer interface plug-in modules. In the IPARS controller for the 1001A, the printer programs are in the main program PROM. Also, the 1001A uses a separate bus to access the PROM. This allows the processor to fetch instructions from PROM without interfering with display refresh data transfers from the RAM CRT buffers to the monitor controller circuits.

C. RAM

The RAM is used to store the CRT display data, with a 1K byte area assigned to each display. A portion of RAM is also used as a scratchpad memory for the processor, and in the case of the IPARS controller for the 1001A, it also contains two 1K printer data buffers.

D. EAROM (1001A only)

The EAROM is a 1400 bit electrically alterable ROM that is non-volatile when power is removed. It is used to store system configuration data. This is the same type of data that is entered into the DIP switches on the 1001 (see below). The EAROM provides permanent storage until it is altered. This is accomplished by operating switch S2 to TEST mode and entering the new data from any keyboard on the system.

The following configuration options are programmed into EAROM:

Cursor Option - Box/Underline

Printer Baud Rate (Sixteen different Baud Rates)

Printer Interface - Current Loop/RS-232

Keyboard Type to Select Translate Table

Terminal Address

Interchange Address

Number and types of printers

The EAROM PIA is a programmable interface adapter that allows the processor to: write data to and read data from EAROM; input the test signals from test switch S2; select the type of cursor; load the VTAC control register (DONBT) with configuration data; and select the type of printer interface, either current loop or RS-232.

An interval timer causes the program to read the EAROM PIA input register every 67 ms. If the test switch is operated to test, loop, or line monitor, an interrupt bit is set in the input register. When the interrupt bit is set the processor reads the PIA registers to determine the cause of the interrupt. The program then branches to the associated routine to perform the requested function.

E. Printer Interfaces

The printer interfaces are programmable Asynchronous Communications Interface Adapters (ACIA). The ACIAs are serial-to-parallel and parallel-to-serial converters. They have four registers (TXDATA, RXDATA, Control, and Status) each of which has a separate memory address (500X and 540X). The program at initialization configures the ACIA to interface the printer type. It reads the configuration data from EAROM (1001A) or from DIP switch S2 (1001). Then it writes the configuration data into the ACIAs control register. On the 1001, one bit of DIP switches S5 and S6 selects either a current loop or an RS-232 interface. On the 1001A this is accomplished by the program through the EAROM PIA.

DIP switches S5 and S6 on the 1001 select the baud rate (110-4800 baud) from a crystal controlled multiple-output baud rate generator and apply it to the ACIAs. On the 1001A the baud rate generator is programmable and the program selects the baud rates (50-19,200 baud).

The 1001 also uses two plug-in printer modules, one for each printer interface. These modules provide the specialized program in PROM for the printer interface and a 1K RAM buffer for the printer data.

When the ACIA wants service, it interrupts the processor and sets an interrupt bit in the ACIA, which is read by the processor to determine who caused the interrupt. The processor then branches to the interrupt routine and services the interrupt.

Refer to Section 4.11 for testing the printer interface.

F. Modem Interface

The modem interface is a programmable Universal Synchronous Receiver, transmitter (USRT) LSI chip with separate CRC generate and check, sync detector, and status registers. The data buffer in the USRT has memory address 6000 and the CRC register has address 6200 (1001) or 6C00 (1001A). The processor can read from or write to either register. The USRT is configured for 6-bit character with no parity. It is basically a parallel-to-serial and serial-to-parallel converter that interfaces an RS-232 modem.

When the USRT wants service or when a malfunction occurs, it interrupts the processor and sets an interrupt in its internal register. The processor services the interrupt in the same way as for the printer interface. The processor can read the status, receive data, or the CRC registers when it services the interrupt.

When test switch S2 is operated to LOOP, the modem transmit output lines are looped back through relays (on the backplane) to the receive input lines for testing. Refer to Section 4.11 for modem testing.

On the 1001A the CRC data is output directly to the data bus, whereas on the 1001 it first goes through a selector, which can also select the test switch outputs and the IA from switch S4 to put on the data bus.

G. Keyboard Circuits

The keyboard clock and load signals are generated by the display timing circuits and sent to the local (integral) keyboard (for the 1001A they are sent through the video mixer). The received serial keyboard data from the local keyboard and from the I/O circuit via the keyboard MUX (1001A) is assembled in the serial-to-parallel shift register and applied to the keyboard translate PROM. Here the keyboard data is translated into 6-bit SABRE code, which is sent to the keyboard PIA. The SABRE code is used in the 1001/A and on the comm line. The translate PROM contains four separate tables for the different types of keyboards. The table used is selected by the program via the keyboard PIA (1001A) or by DIP switch S4 (1001). When a Credit Card Reader (CCR) is attached to a keyboard channel, a special translate PROM is required.

The keyboard PIA stores the keyboard character, sets an interrupt bit in an internal register, and raises an interrupt to the processor. The processor services the interrupt in the same way as for the other interfaces, except that in this case the keyboard data is put into the associated CRT buffer in RAM at the cursor address. The cursor address (one for each CRT for the 1001A), which is maintained by the program, is updated as the keyboard data is received. The keyboard PIA for the 1001A has four interrupt lines, one for each CRT. The processor determines which CRT the keyboard data is from by determining which interrupt bit is set in the keyboard PIA.

When test switch S2 is set to the keyboard position, it starts a counter-shift register combination which inputs a continuous series of characters into the keyboard serial-to-parallel shift register. These characters are stored in the CRT buffers and are displayed on all screens.

The keylock switch prevents any keyboard data from being entered when it is on. On the 1001, the keyboard PIA also handles the LED data. When the LED data is addressed, it is loaded into the keyboard PIA and then it is sent out to the LEDs.

H. Monitor Controller Circuits

1001

Refer to Figure 3-96. The display timing and addressing circuits generate the display H and V sync signals and all monitor controller timing and addressing. They are independent of the processor, and they refresh the display one character line at a time. When they want to fetch display refresh data, they raise DMA REQ to halt the processor. Then they address and read a line of characters in the RAM CRT buffer, and load them into the line store register. Here the characters circulate for a period of 7 horizontal display line times. Once during each line time each character is presented to the character generator. The first time the line of characters is presented to the character generator, the generator outputs the dot matrix pattern for the first slice of each character in the line. The second time the line of characters is presented, it outputs the dot pattern for the second slice, and so on through slice 7, whereupon a new line of characters is fetched and loaded into the line store register and read out starting with line 9.

The slice dot patterns are temporarily stored in a shift register and shifted out serially to the display over the video line via the I/O circuit.

The cursor address, which is maintained by the program, is written into the cursor PIA by the processor during the previous vertical retrace

time. It is compared to the screen character addresses, and when a comparison occurs, the cursor is put onto the video line. Switch S1 determines the type of cursor, and the keylock switch blocks the video to the display.

1001A

Refer to Figure 3-97. The VTAC is a programmable CRT controller that generates all the timing for the monitor controller circuits and the H and V sync signals for the displays. It is configured (control register enabled by DONBT and loaded) by the program at initialization, after which it operates independently of the processor for display refresh.

The VTAC is flagged by the address decoder whenever the processor accesses an internal register or the PROM. During this time the monitor controller circuits use the data and address buses to fetch refresh data. Refresh is accomplished by fetching a character at a time from the CRT buffer RAM, storing the characters in one of the RAM row buffers, presenting the final assembled row of characters to the character generator, generating the character DOT matrix slices, and sending them to the displays. Character generation and transmittal to the displays is similar to that for the 1001. In this case, however, there are four displays so there are four shift registers, video mixers, and I/O circuits. Also a row of characters is sent to each display in turn, and the LED data from the data bus is loaded into the shift registers instead of being sent directly to the display. All the shift registers are loaded with LED data at the same time at the end of the frame, and the LED bytes are shifted out to the displays during vertical retrace.

The address counter produces the refresh memory addresses, and the address selector selects either the addresses from the address counter to store the characters in the row buffer RAM, or it selects the addresses from the VTAC to read the row of characters.

Each succeeding row of characters is fetched and stored in the second row buffer RAM while the previous character row in the other row buffer is being presented to the character generator.

The cursor address for each display is loaded into the VTAC once every four frames. It is gated out at the proper time and mixed with the video to the associated display in the video mixer. Thus, each display receives a cursor once every four frames. The type of cursor is controlled by a bit in the EAROM. The cursor address for each display is stored at the end of the display refresh memory in two consecutive locations (e.g., 23C0 and 23C1-CRT1, 27C0 and 27C1-CRT2, etc).

3.2.29 Magnetic Tape Controller Operation

3.2.29.1 General. The Magnetic Tape System uses 9-track magnetic tape in either of two recording formats, depending upon the configuration. Tapes prepared on this system in either format are generated in a format which is IBM and USASCII compatible. Tapes generated elsewhere in IBM or USASCII formats can also be read by this system.

The Mag Tape System consists of a cabinet (932115), the Magnetic Tape Controller (932289), a Tape Formatter (594518), and up to three tape drives. (See Figure 3-98 for the system components and cabling.) The Magnetic Tape Controller (MTC) is a single full-size board designed to be installed in any I/O controller slot in the processor card cage. It receives I/O control from the processor and transfers data to and from memory in word (16-bit) units via the PTS IOB bus. It can access all 128K bytes of memory.

Data is transferred between the MTC and Formatter in byte (8-bit) units. The data, as well as various control and status signals, is carried on a single cable (932238 G1). The formatter controls the write and read functions of the tape drive and all tape motion functions. The formatter also controls whether the data exchange with the drive is in NRZI or PE format. (These formats are shown in Figure 3-99.)

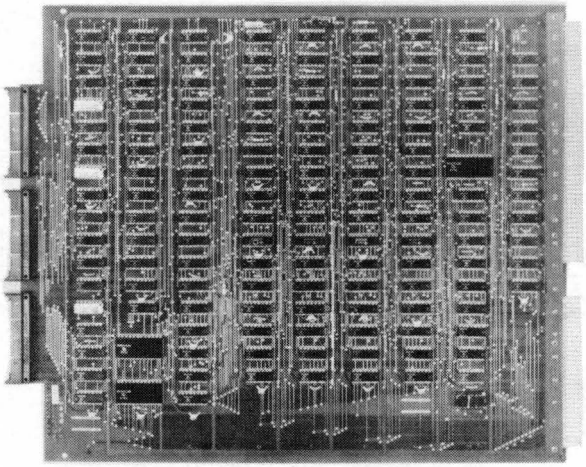
Data is written or read by the drive one byte at a time in blocks known as records; each time a write data function is executed, a record is created on the tape. The data, was well as drive control and status signals, is conveyed between formatter and drive by a three section cable, one for the drive read logic, one for the write logic, and one for the control logic.

A daisy chain of three-part cables is similar to that between the formatter and drive interconnect drives in a multidrive configuration. A maximum of three tape drives can be accommodated.

The MTC is assigned a fixed controller address = XAXX (HEX); i.e., bits 4-7 of the device address word must be 1010.

The MTC generates an interrupt to the processor when one or more of the eight ICB interrupt conditions occur. The level on which the interrupt is generated is determined by a patch plug at location H1 on the MTC. A connection between pin 12 and any one of pins 1-8 assigns the corresponding interrupt level 1-8 to the MT (Example: Pin 12- Pin 5 = level 5).

Dipswitch 117 is used for testing. For normal operation set it to "ON." If set to the "OFF," the Word Address and the Byte Count registers



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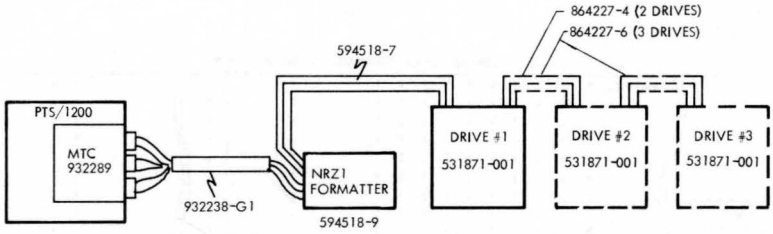
MAGNETIC TAPE CONTROLLER



NPZI PTS/1200 MAG TAPE SYSTEM CONFIGURATION AND CABLING

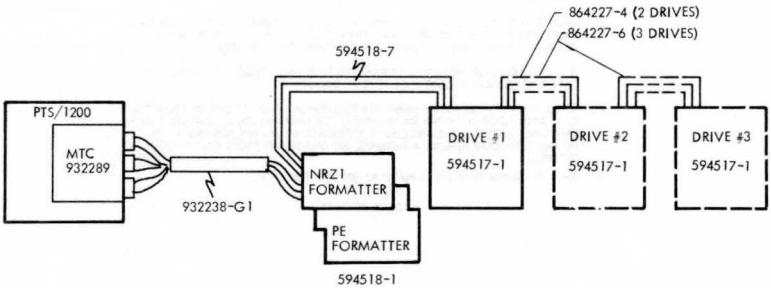
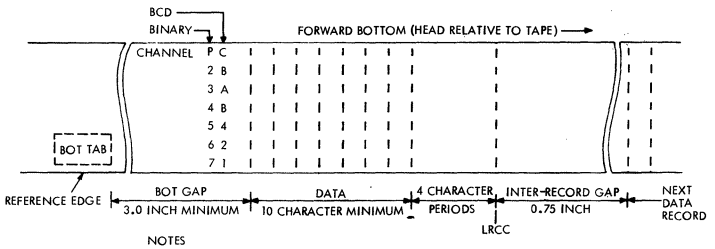


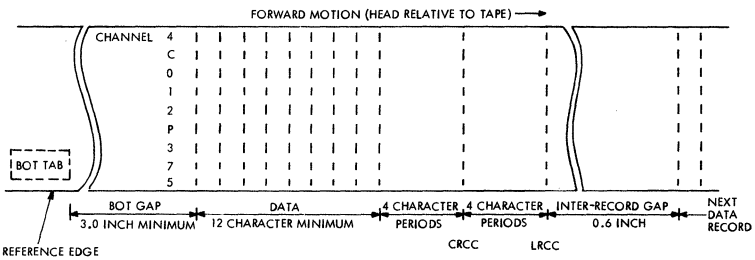
Figure 3-98. Magnetic Tape Controller and System Cabling



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 2 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) CONTAINS ODD DATA PARITY FOR BINARY TAPES, OR EVEN PARITY FOR BCD TAPES.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE LRCC) IS EVEN. IT IS POSSIBLE IN THE 7-TRACK FORMAT FOR THIS CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
5. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 4, 5, 6 AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL IRG (0.75 INCH) FROM THE FOLLOWING RECORD.
6. DATA PACKING DENSITY MAY BE 200, 556, OR 800 BITS PER INCH.

7-TRACK FORMAT



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. EACH BIT OF THE LRCC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE CRCC AND THE LRCC) IS EVEN. IN THE 9-TRACK FORMAT THE LRCC WILL NEVER BE AN ALL-ZEROES CHARACTER.
5. IT IS POSSIBLE FOR THIS CRCC CHARACTER TO BE ALL ZEROES, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED
6. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 3, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRCC. THE CRCC CONTAINS ALL ZEROES. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL IRG (0.6 INCH) FROM THE FOLLOWING RECORD.
7. DATA PACKING DENSITY IS FIXED AT 800 BITS PER INCH.

9-TRACK FORMAT

Figure 3-99. Magnetic Tape Formats

will both be inhibited from incrementing. This mode of operation should only be used for special testing applications.

3.2.29.2 Formats. There are two major formats and configurations of the PTS Mag Tape system. (Recording density and parity are not selectable in the 9 track format, either by program control or formatter switches.)

NRZI Configuration

The NRZI Formatter and Pertec Model 6840 tension arm drives use the 9 track NRZI format at a recording density of 800 bpi and tape speed of 37.5 ips.

A nominal, 6 inch interrecord gap separates records in the 9-track NRZI format. The record begins with data characters, 8 bits and P bit for odd character parity. An 8 bit CRCC character follows the last data character of the record by four character periods; four character periods after the CRCC, an LRCC character is written making the number of "1"s in each track even and ending the record.

A file mark is a record composed of a single data character (tracks 3, 6, and 7=1), in all Ø CRCC, and an LRCC identical to the data character.

NRZI/PE Configuration

The NRZI and PE formatters and Wangco Mod 11 PE/NRZI vacuum-column drives use the 9 track NRZI and PE formats at a tape speed of 75 ips and recording density of 800 bpi, NRZI and 1600 bpi, PE.

The NRZI/PE switch on the tape drive selects the format. PE is selected when the switch is lighted; NRZI is selected when it is not. The NRZI format is the same as described above.

In PE mode each data record begins with a 41 character preamble, followed by the data characters, followed by a 41 character postamble which completes the record. The data characters contain 8 bits plus a bit for odd parity. A nominal 0.6 in interrecord gap separates adjacent records. IBM/USASCII-compatible file marks are written and recognized.

3.2.29.3 DIO and RIO Instructions. Refer to the simplified circuit diagram shown in Figure 3-100. The MTC is initialized in the same way as the other high speed controllers on the IOB, except that the accumulator is as shown in Figure 3-101 and the packet is as shown in Figure 3-102.

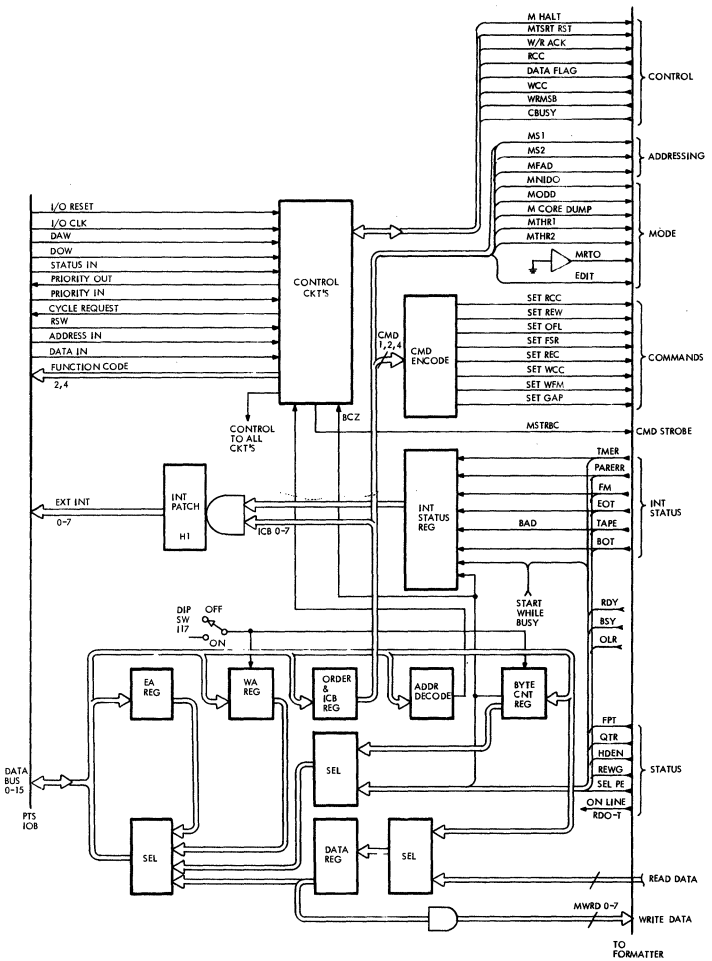
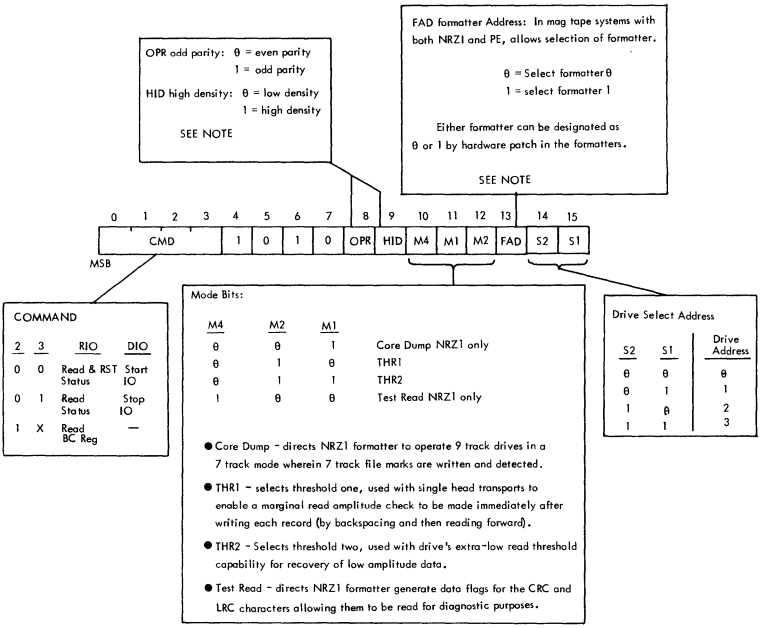


Figure 3-100. Magnetic Tape Controller Simplified Circuit Diagram



NOTE

Program selection of Formatter Address, Density, and Parity is possible only if hardware patching of formatter (s) is set to allow it. Also, density and parity selection is possible only with 7 track operation (not supported by PTS Mag Tape System); on 9 track operation density and parity are always fixed.

Figure 3-101. Magnetic Tape Controller DIO and RIO Instruction Format

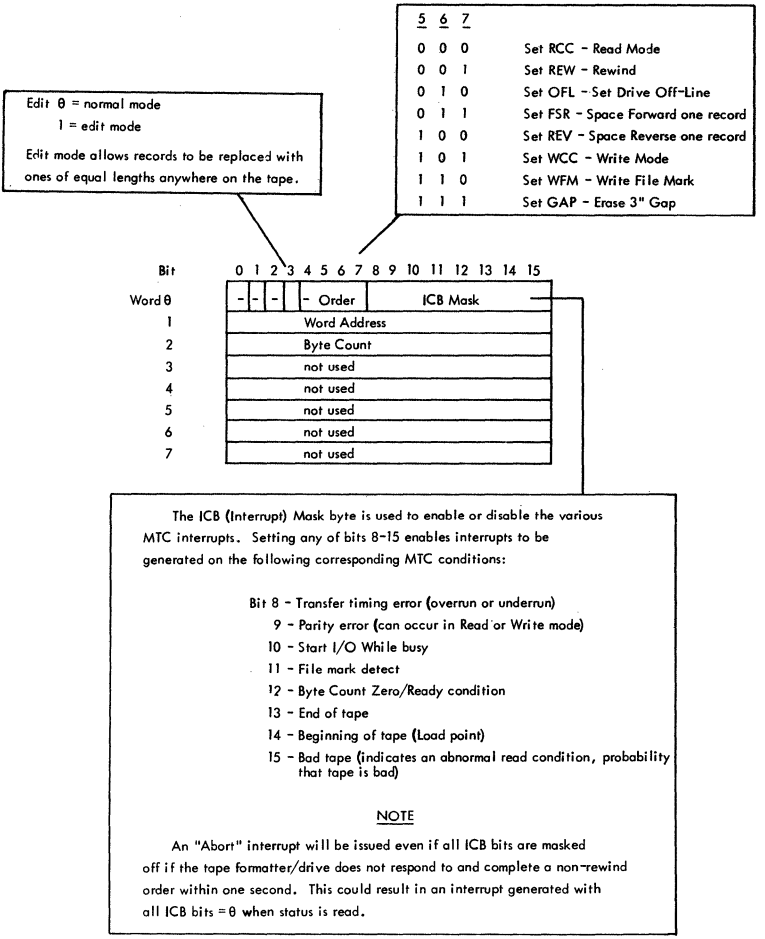


Figure 3-102. MTC Packet Format

In the case of a start I/O instruction, the first word of the packet is loaded into the Order and ICB register. The second word (in the case of a data transfer order) is loaded into the Word Address register, and the third word is stored into the Byte Count register.

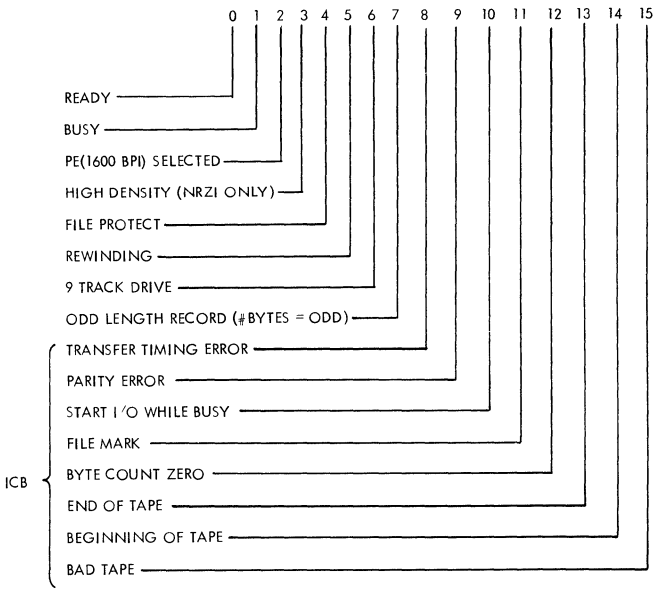
In the case of a Stop I/O, no packet words are loaded into the MTC, but a general reset is generated in the MTC, formatter and drive, halting execution of the instruction in progress.

The R I/O instruction references a single memory location into which the MTC status word is to be put; as with the DIO, the accumulator is loaded when the R I/O is issued. The FAD and S2, S1 bits determine which formatter and drive is to respond with status. The effective memory address determines where the status word will be stored.

NOTE

The status word location in memory is in the lower 64K bytes. As described in Figure 3-101, bit 2 of the accumulator word determines whether the status word or the contents of the byte count register are returned. And bit 3 determines whether the ICB bits are reset at the time status is read.

The status word bit assignments are shown below. Refer to the Formatter Maintenance Manual (Wangco 200250-001 and 201348-001) for a description of those status bits that are not self-explanatory.



3.2.29.4 MTC Operational Description. On receipt of a valid order, the formatter goes busy, and its status goes to busy, not ready. (Exceptions to this are the Set Off-Line order, and the Rewind Order, if so patched in the formatter.) The formatter then issues the appropriate signals to the drive.

In the case of data transfer orders, the formatter issues a data flag whenever it is ready to transfer a byte of data to or from the tape. When writing data onto tape, the MTC generates a DMA request for the first word to be transferred and then waits for the first data flag. When received, the MTC responds by sending the formatter the most significant data byte and an acknowledge. The second data flag causes the least significant data byte to be transferred to the formatter with the acknowledge, and a DMA request to be made for the next word. Each DMA request increments the Word Address counter to address the next data buffer word and increments the Byte Count register. The data transfer continues until the byte count register overflows, creating a byte count zero status/interrupt condition.

When reading data from the tape, the MTC waits for the first data flag from the formatter, whereupon it reads the most significant byte of data. It responds with an acknowledge and waits for the second data flag. It receives the least significant byte of data with the second data flag, returns an acknowledge, and transfers the first word to memory with a DMA request. As in the write case, each DMA transfer increments the Word Address counter, and the Byte Count register. At byte count register overflow, the byte count zero interrupt is issued and no further DMA requests are made.

If the record being read has a byte count greater than that which was specified by the I/O packet, the formatter/drive will continue to read the entire record, unless halted by a STOP I/O command. In any case, DMA transfers will stop at byte count zero.

If the record's byte count is equal to or less than that specified by the packet, the tape read operation will stop at the end of the record. If the number of bytes in any completely read record is odd, the odd length record status will be posted.

Two words of buffer register storage are used for DMA transfer of both read and write data.

Data transfer to and from memory locations above 64K bytes is implemented by returning bit 15 (the LSB) of the packet word address to the "I/O Upper Memory Select" signal to the processor. Also, memory access by the MTC will cross the 64K boundary if the record length causes the word address register to increment above 64K.

3.2.30 Magnetic Stripe Credit Card Reader Operation

The credit card reader (CCR) is self contained. It has its own power supply, controller, read preamplifier and card reader assy, refer to Figure 3-103. The CCR interfaces the PTS over the keyboard line. It is daisy-chained with the keyboard, and shares the line with the keyboard.

When a credit card is read by the reader, the data from the keyboard is inhibited and the CCR data is sent to the PTS over the keyboard line. The header in the CCR data notifies the program that the data is from the CCR.

Only credit cards complying with American Banking Association (ABA), International Air Travel Association (IATA), and Thrift Institutions (THRIFT) can be read at the present time. There are three read heads, one for each type of card. A switch on the CCR selects one of the read heads to read the credit card and notifies the controller as to the type of card to be read. When a credit card is read, data from the selected read head is amplified and peak detected by the preamplifier, decoded by the controller, and stored in the controller's memory. After the entire card is read the controller, which is microprogrammed, adds the appropriate control characters and sends the data to the PTS a character at a time. One character is sent each time a keyboard load pulse is received (15 characters/second).

While the CCR is transmitting data to the PTS, the keyboard is locked out and any characters entered during this time are lost. The transfer time to the PTS for an 80 character message is approximately 6 seconds.

The CCR has two indicators: It has a Busy indicator which is lighted when a card is read and extinguished when the entire message has been sent to the PTS, and it has an Error indicator which is lighted for two seconds when any of the following occurs:

a. Parity error on credit card

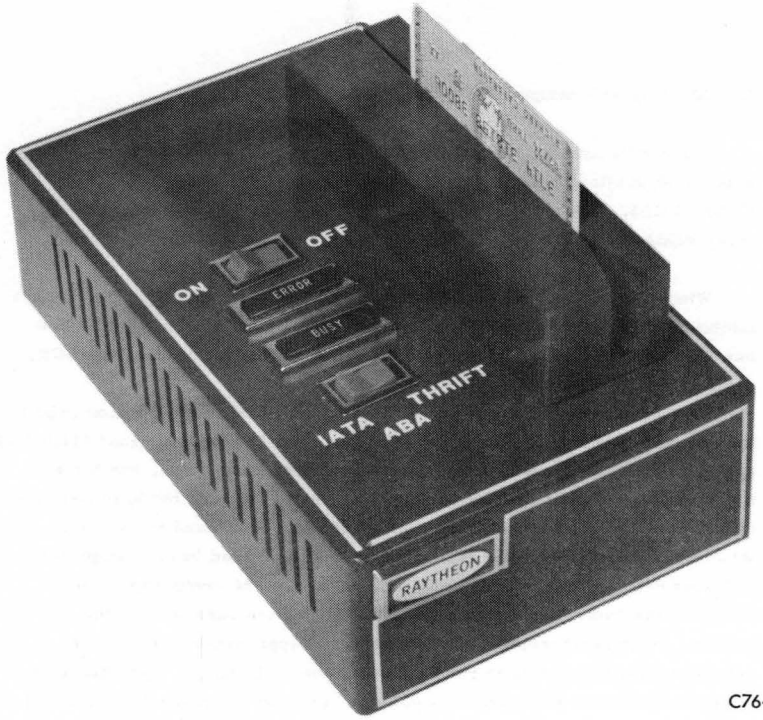
b. Failure to detect start and/or stop sentinel character

c. Card speed was not within 2.5 to 15 inch/sec.

In case of a parity error, the data will still be sent to the PTS. Other errors will cause a reset. The card may be reread when the error indicator is extinguished.

Read Head

Three separate center tapped differential output read heads are used, one for each application (ABA, IATA, and THRIFT). Head selection is



C76-2117

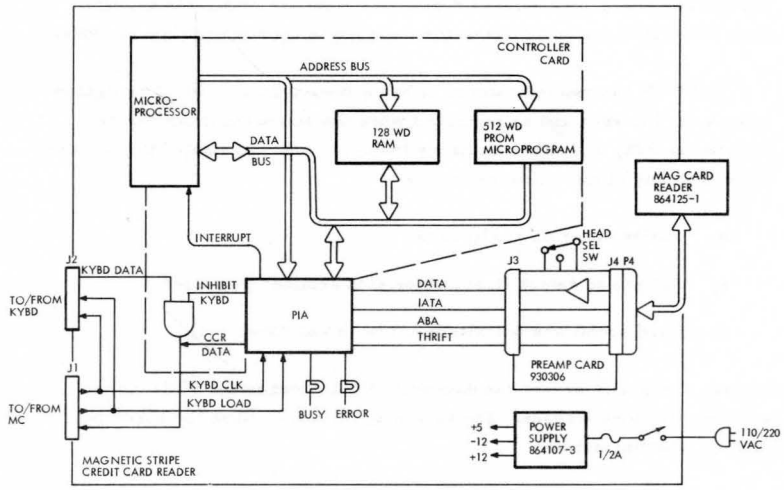


Figure 3-103. Magnetic Stripe Credit Card Reader

made by a swtich on the CCR which applies a dc TTL logic level to the center tap of the selected head. The level goes low when the head is selected.

Read Preamplifier

The read preamp is a differential amplifier that corrects for differences between heads and the degradation in credit card quality.

Controller

The Controller is a microprocessor system based on the Motorola 6800 chip set. The M6800 μP chip executes instructions stored in PROM (512 x 8, expandable to 1024 x 8), using the RAM (128 x 8) for temporary data storage. The Peripheral Interface Adapter (PIA) provides 16 bidirectional I/O ports, 7 of which are used in the CCR application. Three of the PIA inputs specify which track of the credit card is being read. The fourth input, also tied to an Interrupt line, is data from the Read Amplifier; this arrangement provides an interrupt whenever there is a data line transition.

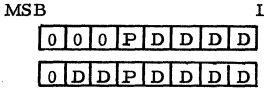
Two outputs control the keyboard channel. The first inhibits the keyboard when the CCR has data to send the PTS. The second acts as a data line feeding a flip-flop which is clocked on each keyboard clock pulse.

Data Message

The data encoded on the credit card is biphase, double frequency, coherent phase recording, where the data and clock are both recorded on a single track. To decode the data, the controller determines whether a bit is "0" or "1" by determining whether or not there was a transition in the middle of a bit-cell. It does this by calculating the duration of each bit cell. When a data transition occurs, the time between the last two transitions is compared with three-fourths of the previous bit cell length. The result of this comparison determines whether the present transition represents a "1" or a bit cell boundary. The microprogram ignores the first sixteen transitions when a card is read, and then synchronizes on the "0"s pattern prior to the Start Sentinel character.

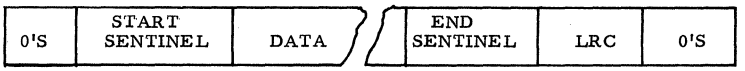
The microprogram examines the data stream for the correct Start Sentinel character. When this character is found, the CCR is "in sync," and characters are entered into the RAM until the End Sentinel character is detected. If no End Sentinel is found, the Error Indicator is lighted and the CCR is reset. The LRC character immediately following the End Sentinel is also input.

Once the data characters are in memory, the CCR checks parity and repacks each byte into the following formats:

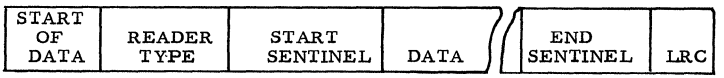


If a parity error is detected, the Error Indicator is lighted, but the data will still be sent to the PTS.

The Magnetic Strip encoded information on the card has the following format:



Data sent to the PTS is rearranged as shown below:



Start of Data - $(21)_{16}$ - A unique character informing the PTS that a reader is using the keyboard channel.

NOTE

PTS Badge Reader uses the same code.

Reader Type - - A character $(10)_{16}$ to $(1F)_{16}$ denoting the reader type. Any other code should be considered as Badge Reader data.

$(10)_{16}$ Magnetic Credit Card Reader

Start Sentinel - $(0B)_{16}$ - ABA

$(45)_{16}$ - IATA

Data ABA - Variable up to 37 characters
IATA - Variable up to 76 characters

End Sentinel - $(1F)_{16}$ - ABA

$(1F)_{16}$ - IATA

LRC - $(XX)_{16}$ - Longitudinal redundancy check character. The parity bit of this character reflects the parity of the LRC only.

NOTE

The above definition includes the parity bit.

Once a data message for the PTS is completely formatted, the CCR waits for a keyboard load pulse; then it locks out the keyboard. When the next load pulse is received, the MSB of the data byte is placed on the keyboard data line. The LSB of the data byte is placed on the PIA output line and clocked onto the data line on the next keyboard clock. The rest of the byte is transmitted LSB first on the following clocks. This cycle continues until the entire message is sent, and then the keyboard is unlocked.

Two additional signals have been added to unused pins on the keyboard cable connector in order to allow the Magnetic Card Reader to be used with the 1001/A. The signals are:

Pin 10 - CCRACTIVE (lo Truth)

Pin 7 - ABA (lo Truth)

These signals are used to select the CCR translate table. When the CCR is connected to a monitor controller, the message header characters inform the program that the CCR is sending data.

3.3 Data Display/SAM Display Circuit Description

3.3.1 General

This Section describes the PTS-100 Data Display (data display) and the Stand Alone Monitor (SAM) display. The SAM display can also operate with a slave SAM display attached via coax cable up to 200 feet. Figure 3-104 shows a data display/SAM display terminal along with its associated keyboard. General specifications for the data display/SAM display are listed in Table 3-23. The data display is a 15-inch rectangular CRT capable of displaying 480, 960, 1024, or 1920 characters. The SAM can display either 960 or 1920 characters. In the SAM and slave SAM configuration, each screen can display 960 characters maximum.

C73-12837

Figure 3-104. Data Display Terminal

Table 3-23. Data Display/SAM Display Specifications

Dimensions:	Height 13.5 in. Width 18 in. Depth 25.5 in.
Input Power:	
Data Display:	±35 vdc at 0.5 ampere
SAM Display:	240 vac ±10% 220 vac +10% -15% } 47 to 63 Hz 115 vac ±10%
Maximum Signal Cable Length:	
Data Display:	200 feet (data display to remote concentrator)
SAM Display:	SAM to CPU: 5000 ft. (coax) SAM to CPU: 2000 ft. (tw pr) SAM to SAM slave: 200 ft. (coax)
Screen:	Horizontally mounted rectangular CRT Height 8.5 in. Width 11 in. (15 in. diagonal)
Viewing Area:	Width 10 in. Height 7 in.
Screen Formats:	
Data Display:	40 char/line; 12 lines 80 char/line; 12, 24 lines 64 char/line; 15, 16, 30 lines (upper case only)
SAM Display:	80 char/line; 12, 24 lines 64 char/line; 15, 30 lines
Displayable Character Formats:	
Data Display:	480, 960, 1024, 1920
SAM Display:	960, 1920
Refresh rate:	60 Hertz
Character Generation:	Enhanced dot matrix 7 x 7 upper case 7 x 9 upper/lower case
Character Size:	0.11 inch wide x 0.14 inch high (64 or 80 characters/line), or 0.15 inch wide x 0.17 inch high (40 characters/line)
Phosphor:	P31 green

a. The operator generates the characters on the keyboard associated with the data display. The character codes produced by pressing keyboard keys are entered into dedicated memory blocks in the PTS-100 processing unit. Once entered into memory, the characters are sent back to the data display through the monitor controller. They are displayed on the data display and refreshed 60 times per second. In a SAM display, the Monitor Controller circuit is located on the control logic board mounted within the display cabinet.

b. In certain applications where the PTS-100 is used with central site processors, system generated messages are entered directly into the PTS-100 processing unit memory and then sent to the display and refreshed as before. These messages usually demand specific operator responses as part of a system-wide operating discipline.

A brightness control on the display permits adjustment of the viewing intensity of the characters. The focus and position of the characters do not require operator adjustment.

The characters presented on the CRT display screen are made up of a series of intensified dots, although they appear to have a solid printed font. Figure 3-105 shows a display screen presentation. Each character uses a 7 x 9 enhanced dot matrix as shown in Figure 3-106. However, for displays with upper case characters only, the 7 x 7 enhanced dot matrix is utilized.

3.3.2 Data Display Operation

Figure 3-107 is a simplified block diagram of the data display and keyboard circuits. The display receives dc power, video, and horizontal and vertical drive sweep signals from the monitor controller. The sweep signals are amplified and applied to the CRT deflection coil to produce a 260 line display repeated 60 times a second, with vertical retrace occurring during the last 20 lines, which are blanked. (See Figure 3-108.)

Ten horizontal sweep lines are used to display one line of characters. Nine lines are used to display the characters, while the tenth is for vertical spacing. Each horizontal line is divided into 800 dot times (400 for the 40 character/line format), with the last 60 dot times (80 for the 40 character/line format) used for horizontal retrace. The video signals from the monitor controller are composed of dot patterns from the character slices. Each character slice corresponds to a horizontal line. The character slices are amplified by the video amplifier and applied to the CRT, where they appear as intensified dots on the screen (see Figure 3-106). The dot size is controlled by the monitor controller and is determined by the screen character/line format. The 80 and 64 character/line formats use a 12.48 MHz dot

C72-7969

Figure 3-105. CRT Display Character Presentation

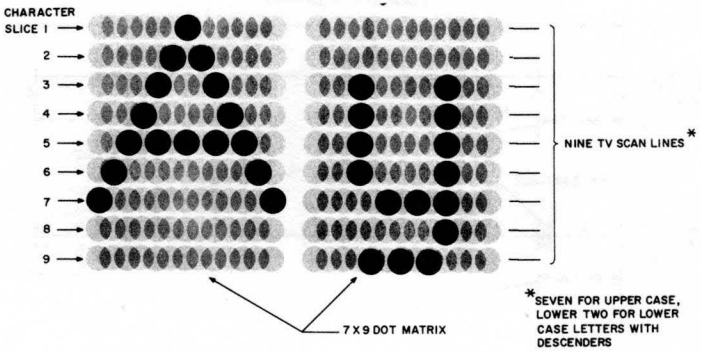


Figure 3-106. Character Format

frequency. The 40 character/line format uses a dot frequency of 6.24 MHz, which results in half as many dots, but the dots are twice as large. The horizontal sweep is also used to drive the display high voltage circuits.

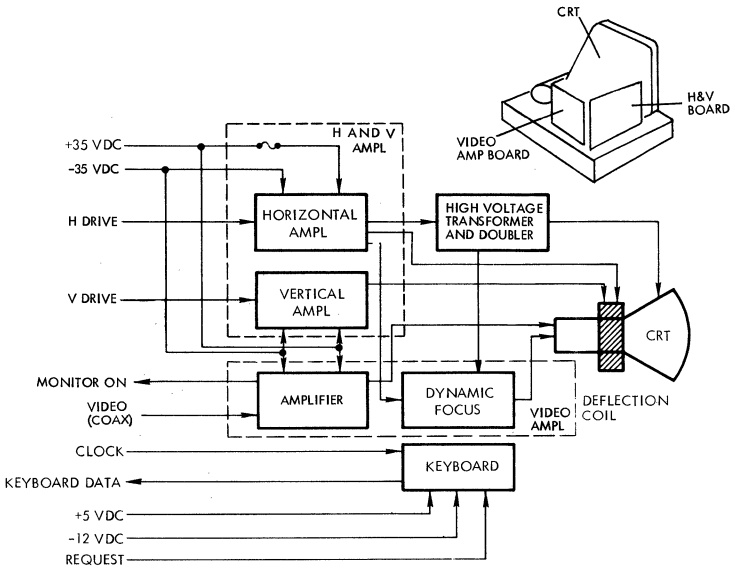
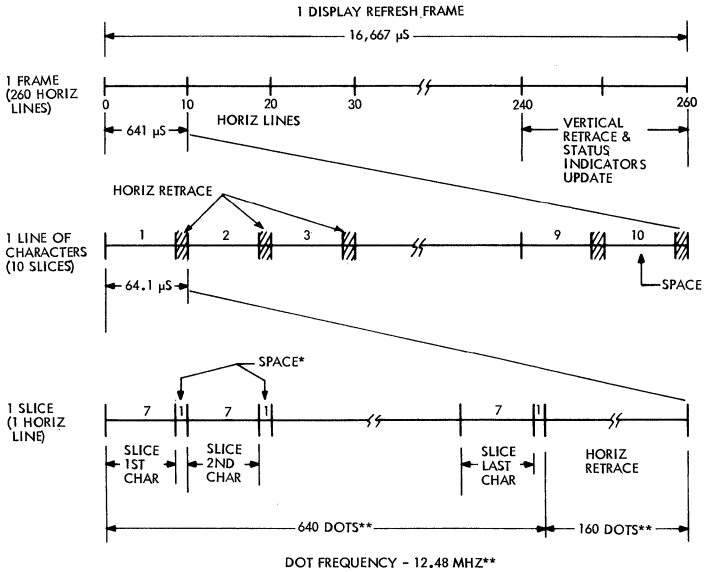


Figure 3-107. Data Display, Simplified Block Diagram



*1 DOT FOR 40 & 80 CHARACTER/LINE FORMATS;
3 DOTS FOR 64 CHARACTER/LINE FORMAT.

**FOR 40 CHARACTERS/LINE DOT FREQUENCY IS 6.24 MHZ WITH 400 DOT LINES (320 + 80).

Figure 3-108. Display Timing Diagram

3.3.3 SAM Display Operation

Figure 3-109 is a simplified block diagram of the SAM display showing a master SAM and slave SAM. The master SAM consists of a control logic board, analog board, CRT, status display LEDs, keyboard, and keyboard display LEDs. A self-contained power supply on the analog board receives ac line power from any convenient source and generates all ac and dc operating power for the circuits in the master SAM.

During keyboard data entry, the control logic board sends data from the SAM and slave SAM keyboards to the DA where it is sent to the multiplex channel controller. This controller translates the keyboard codes into ASCII and stores them in memory. During display refresh, the control logic board converts the ASCII coded data characters from memory via the DA into dot patterns, and alternately sends them one at a time to the master SAM and to the slave SAM along with horizontal and vertical sweep signals.

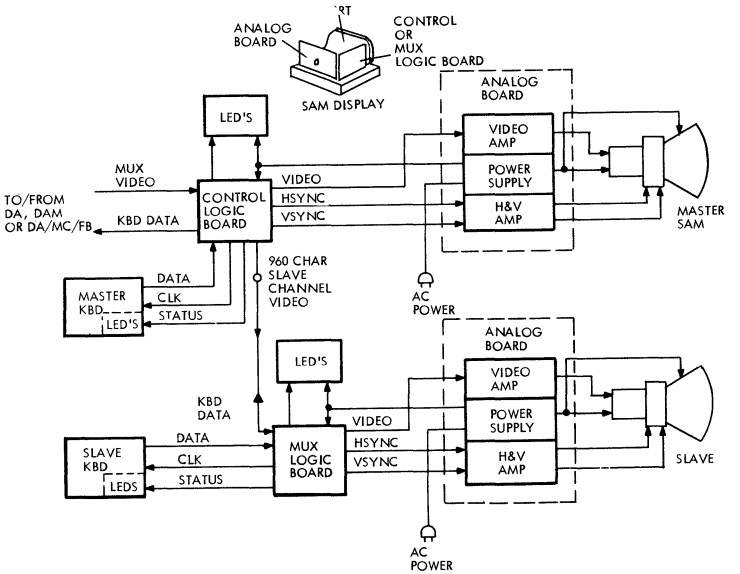


Figure 3-109. SAM Display, Simplified Block Diagram

The slave SAM is similar to the master SAM with the exception that it contains a MUX logic board which handles all control and signal processing functions. The MUX logic board is an abbreviated version of the control logic board since the majority of slave SAM control is performed by the control logic board. Both boards are interconnected with coax cable. Slave MUX video is received and slave keyboard data is sent out via the coax cable under control of the control logic board. The remainder of general overall circuit operation is similar to that described for the data display in Section 3.3.2.

3.3.3.1 Analog Board Circuit Description. The analog board is identical for both the master SAM and slave SAM. Figure 3-110 is a simplified functional block diagram of the analog board. When used in the master SAM, the analog board receives inputs from the control logic board and generates the operating and drive signals for the CRT in the master SAM cabinet. DC operating power for SAM circuits is produced by the analog board. When used inthe slave SAM, the analog board operates in a similar manner between the MUX logic board and the CRT in the slave SAM. The basic functional circuits of the analog board include: horizontal scan drive, video amplification, vertical scan drive, and low voltage power generation.

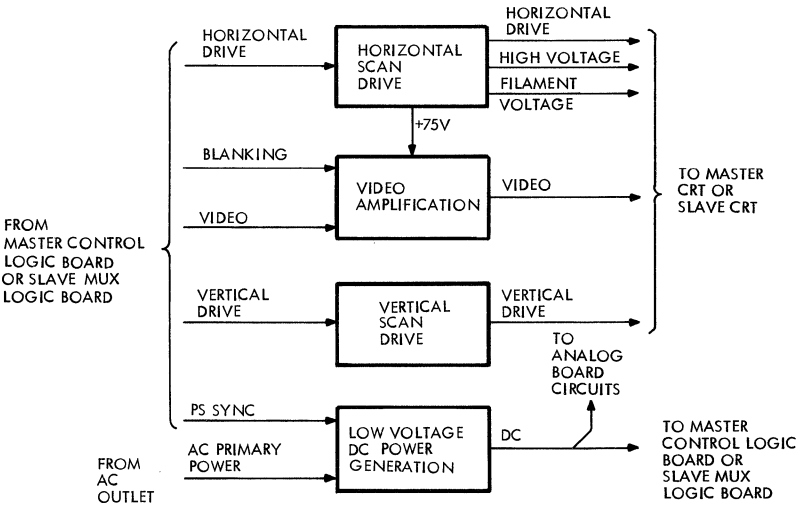


Figure 3-110. SAM Display Analog Board Simplified Block Diagram

The horizontal scan drive circuit produces drive pulses for the horizontal yoke of the CRT. These pulses are synchronized to the horizontal drive, pluses received from the MUX, or control logic boards. A +75V dc level, derived by rectifying the pulses, is also sent to the video amplifier to ensure a maximized video presentation on the CRT. The horizontal scan drive circuit also sends focus voltage, heater voltage, and high voltage to the CRT.

The video amplification circuit amplifies video pulses received from the MUX or control logic boards. It also provides facilities for black level setting and video blanking to allow slave keyboard and LED data to be processed during flyback.

The vertical scan drive circuit generates drive pulses for the vertical yoke of the CRT. These are synchronized with the vertical drive pulses from the control or MUX boards.

DC operating voltages for the entire display are generated by the low voltage power generation circuit. This switching power supply is frequency synchronized by PS SYNC pulses to prevent transients from affecting the CRT display. Various levels of ac input primary power can be accepted by the power supply.

3.3.3.2 Control Logic Board Functional Description. Figure 3-111 is a simplified block diagram of the control logic board circuits. Data from the DA is encoded using the Manchester system where the data is exclusive ORed with the 1.56 MHz clock. This ensures that there is at least one transition per bit in the data stream. The resulting data stream contains 780 kHz and 1.56 MHz frequency components, which allow bandpass filters with transformer coupling to improve noise rejection and eliminate ground potential differences. The Manchester encoded serial character data from the display adapter is decoded to restore the zero crossings, the clock extracted, and the data entered into a serial shift register, where it is read out in 8-bit parallel bytes. The extracted 1.56 MHz clock drives the data-in timing circuits, which count the incoming bits to determine the time of occurrence of data characters, line sync, frame sync, display address, and other signals for both the master SAM and slave SAM. These circuits then gate the input data into the appropriate decoder, line load, or LED registers.

During the time of horizontal display line 241 (see Figures 3-31, 3-32, 3-34, and 3-36), the two 8-bit bytes from memory location 960 are gated through the LED drivers to the LED status indicators on displays 1(master SAM) and 2 (slave SAM). Each bit in the byte controls one indicator.

The decoder decodes the sync, keyboard load, and display address characters and gates the display timing circuits which clock the displays,

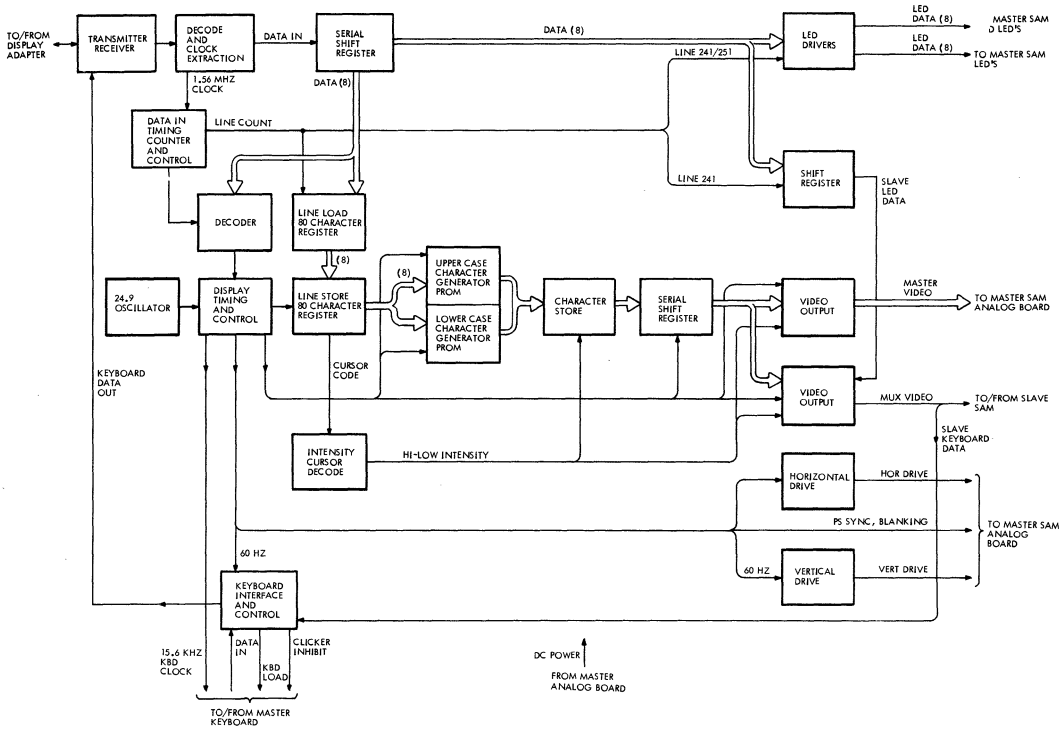


Figure 3-111. SAM Display Control Logic Board, Simplified Block Diagram

keyboards, and data output circuits. The line load register loads complete lines of data characters (80 for 80 character/line formats) and transfers them one line at a time to the line store register. The line of characters circulates in the line store register for a period of nine horizontal display line times (seven for the 64 char/line format). During the following line time, the line store register is reloaded with a new line of characters. The line store register presents each character in the circulating character line to the character generator once during each horizontal line time.

Two PROM character generators are provided, one supplying 64 numerical and upper case characters, and the other, 32 lower case characters. Each character generator contains a 7 x 7 or 7 x 9 dot matrix for every character or symbol to be displayed (see Figure 3-106). The character codes address the applicable dot matrixes. The first time a line of characters is presented to the character generator, the generator outputs the dot matrix pattern for the first slice of each character in the line. The second time the line is presented, the character generator outputs the dot pattern for the second slice, and so on through slice 9, whereupon a new line of characters is loaded into the line store register and read out starting with line 11. Certain configurations, notably 15 and 30 line formats only utilize 7 slices for sending the characters. The deletion of the last two slices prevents use of the lower case characters.

The slice dot patterns are temporarily stored in character store registers and shifted out serially to the displays by serial shift registers. Gating signals from the display timing and control circuit selectively enable the shift registers to the displays. The gating signals are derived from bits 1 and 2 of the display address characters that accompany each line of characters.

The cursor, which is the eighth bit in each character code, is picked off in the line store register and sent to the output circuits to intensity modulate the associated character slices.

Horizontal and vertical sweep signals for the master SAM display are produced by horizontal and vertical drive circuits under control of the display timing and control circuit and in synchronism with the video to the displays.

The master keyboard is clocked with a 15.6 kHz signal from the display timing and control circuit and polled by keyboard load pulses. The keyboard load pulses are initiated by bit 8 of the display address characters. They are detected by the decoder and applied through the display timing and control circuit to the keyboard interface and control circuit. The appropriate display address code with bit 8 set occurs once every four display frames as discussed in Section 3.2.6. Keyboard data is transmitted to the display adapter

at a 15.6 kHz bit rate or if a coax cable adapter is used, at a 1.56 MHz rate. The keyboard signal to the display adapter is a gated 40 ma +12V signal with approximately 2.5V developed across the DA 62 ohm load.

3.3.3.2.1 Control Logic Board Function Select. Chip switches S1, S2, and S3 on the control logic board modify the circuits for the desired operation. The chip switches control the number of characters (960 or 1920), number of character lines (12, 15, 24, or 30), and number of characters per line (64 or 80), in addition to other function selections described in Chapter 2. The switch and data chip settings are made at system installation to reflect the system character and line configuration.

3.3.3.3 Slave SAM MUX Logic Board Circuit Description. The MUX logic board in the slave SAM display is an abbreviated version of the master SAM control logic board described in section 3.3.3.2. The MUX logic board cannot operate alone; it only operates in conjunction with a master SAM board. As shown in Figure 3-112, the functional circuits comprising the MUX logic board include: slave keyboard control, frame sync detection, line sync detection, and video blanking. Each of these functional circuits is controlled by decoding circuits which examine the incoming serial pulse train from the master SAM control logic board. Each of the circuits is then sequentially enabled at the proper time to respond to the slave video pulse sequence, or to provide slave keyboard data to the master SAM display.

Line sync detection initiates data transfer to the slave display screen and also generates internal synchronizing pulses which are sent to the slave analog board and to the slave keyboard to interlace the transfer of CRT display data, LED data, and keyboard data. At the end of a data frame, the frame sync (FS) pulse causes the frame sync detection circuit to convert the subsequent serial LED information to parallel data for presentation on the LED displays. Upon receipt of every fourth frame sync pulse, the frame sync detection circuit strobes the slave keyboard data back to the CPU via the master SAM.

The slave video input to the MUX board consists of video and LED display information. The video blanking circuit generates the video blanking signal which goes to the slave analog board to blank the video during LED display and keyboard data transfer (during the retrace period).

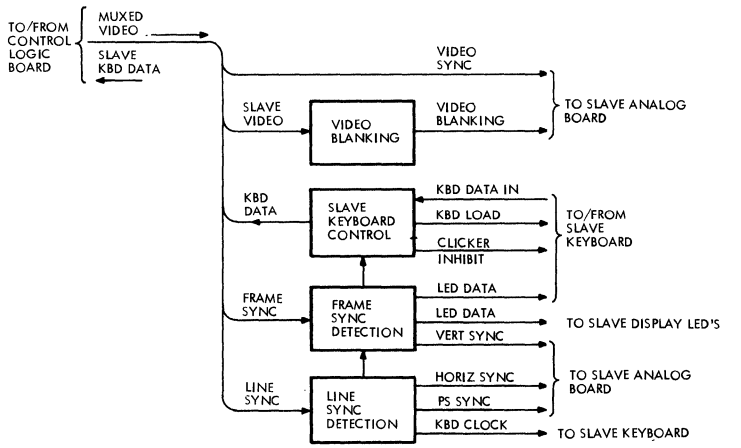


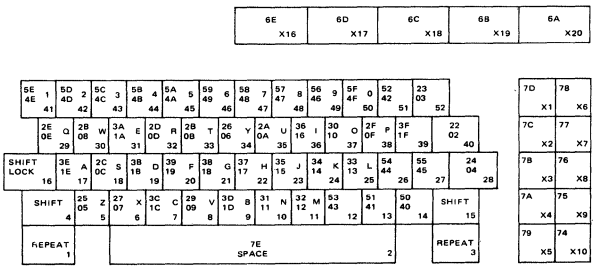
Figure 3-112. SAM Slave Display Mux Logic Board, Simplified Block Diagram

3.3.4 Display Indicators

Some displays contain eight light emitting diode (LED) red indicators, which are used to define system status, message transmission status, and terminal operating modes. The indicators are arranged in a vertical row on the left side of the CRT. (See Figure 3-104.) The eight indicators on each display are controlled by a single 8-bit byte in memory (locations 960 and 970), with each indicator controlled by one bit. The user program controls the indicators by controlling the bits in memory. Automatic update of the indicator status is made during each display refresh period through the monitor controller and display adapter associated with the particular display. Refer to Table 3-13 for the LED memory buffer assignments.

3.3.5 Keyboard

The keyboard for the data display terminals contains keys for entry of alphanumeric characters and symbols, text editing, cursor manipulation, and system defined functions. All key functions except SHIFT, REPEAT, and SHIFT LOCK are interpreted and acted upon according to the software application program. Four standard keyboard configurations are available. see Figure 3-113.) The key functions are programmable, and the legends on the key caps can be different for each customer. Standard editing cursor and intrasystem controls are provided for the most commonly desired entry functions for all versions of the keyboard. Some keyboards have light emitting diode indicators similar to those described above.



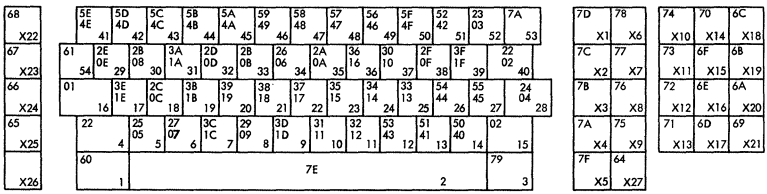
—KEYS SHOWING TWO CODES ENTER THE UPPER CODE WHEN DEPRESSED WITH SHIFT KEY, AND THE LOWER CODE WHEN DEPRESSED WITHOUT THE SHIFT KEY

– SINGLE CODE KEYS ARE SHIFT INDEPENDENT

– THE SMALL NUMBERS IN THE LOWER RIGHT HAND CORNER OF EACH KEY BLOCK ARE KEY REFERENCE (OR POSITION) NUMBERS.

– SOFTWARE TRANSLATE TABLE EXAMPLE: (b = translate table base)
Key 17 Hit unshifted – Add 1E and b to determine memory byte address at which desired code is located.

67 KEY KEYBOARD



– KEYS SHOWING TWO CODES ENTER THE UPPER CODE WHEN DEPRESSED WITH SHIFT KEY, AND THE LOWER CODE WHEN DEPRESSED WITHOUT THE SHIFT KEY

– SINGLE CODE KEYS ARE SHIFT INDEPENDENT

– THE SMALL NUMBERS IN THE LOWER RIGHT HAND CORNER OF EACH KEY BLOCK ARE KEY REFERENCE (OR POSITION) NUMBERS

– KEYS 4, 15, AND 16 PRODUCE CODE 63 (HEX) WHEN DEPRESSED AND CODE 62 (HEX) WHEN RELEASED

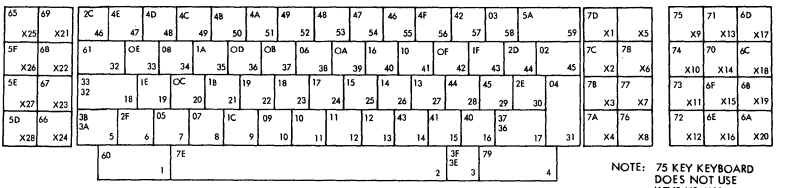
– KEYS 4 AND 16 PRODUCE SHIFT AND SHIFT LOCK, RESPECTIVELY. KEY 15 IS STRAPPABLE TO PRODUCE SHIFT.

– KEYS X10 THROUGH X21 ARE ENABLED BY STRAPPING

NOTE: 69 KEY KEYBOARD DOES NOT USE KEYS X10-X21

62/81 KEY KEYBOARD (3270)

Figure 3-113. Keyboard Key Code (Sheet 1 of 2)



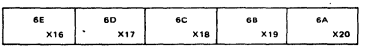
75/87 KEYBOARD

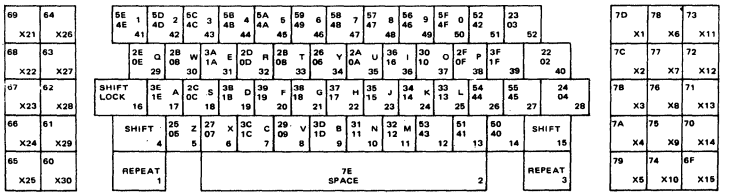
KEYS SHOWING TWO CODES ENTER THE UPPER CODE WHEN DEPRESSED AND THE LOWER CODE WHEN RELEASED

THE SMALL NUMBERS IN THE LOWER RIGHT OF EACH KEY BLOCK ARE KEY REFERENCE (OR POSITION) NUMBERS

KEYS X10-X21 ARE ENABLED BY STRAPPING

THE FOLLOWING KEYS UTILIZE AUTO REPEAT: 2, 4, 6-16, 19-59, X3, X8, and X9





– KEYS SHOWING TWO CODES ENTER THE UPPER CODE WHEN DEPRESSED WITH SHIFT KEY, AND THE LOWER CODE WHEN DEPRESSED WITHOUT THE SHIFT KEY

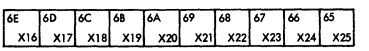
– SINGLE CODE KEYS ARE SHIFT INDEPENDENT

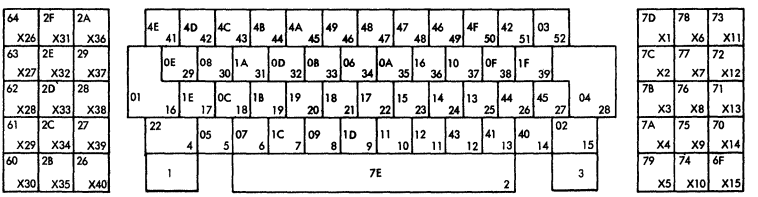
– THE SMALL NUMBERS IN THE LOWER RIGHT HAND CORNER OF EACH KEY BLOCK ARE KEY REFERENCE (OR POSITION) NUMBERS.

– SOFTWARE TRANSLATE TABLE EXAMPLE: (b = translate table base)
Key 17 Hit unshifted – Add 1E and b to determine memory byte address at which desired code is located.

82 KEY KEYBOARD

NOTE: 89 KEY KEYBOARD DOES NOT USE KEYS 1 AND 3.





– KEYS SHOWING TWO CODES ENTER THE UPPER CODE WHEN DEPRESSED WITH SHIFT KEY, AND THE LOWER CODE WHEN DEPRESSED WITHOUT THE SHIFT KEY

– SINGLE CODE KEYS ARE SHIFT INDEPENDENT

– THE SMALL NUMBERS IN THE LOWER RIGHT HAND CORNER OF EACH KEY BLOCK ARE KEY REFERENCE (OR POSITION) NUMBERS

NOTE: 89 KEY KEYBOARD DOES NOT USE KEYS 1 AND 3

89/91 KEY KEYBOARD (4505)

Figure 3-113. Keyboard Key Code (Sheet 2 of 2)

Data is entered when a key is depressed. Multiple key depression does not result in data loss. The transmission code of the depressed key defines the key location. The key code is sent through the monitor controller to the display adapter, where it is demodulated, coupled through the keyboard adapter and multiplex channel controller, translated to ASCII, and stored in memory (see Figure 3-113 for key codes and refer to Table 3-13 for the memory buffer assignments). During display refresh, the ASCII coded characters are read from memory by the display adapters and sent to the monitor controllers, where they are converted to display characters. Thus the keyboard is not restricted to a given code set such as USASCII or EBCDIC. The key functions can be translated into any code set by the monitor controllers.

3.3.5.1 Keyboard Circuit Description. Although there are a number of different keyboard configurations, there are only two basic keyboard circuits — Ohmtec, and Licon. Ohmtec keyboards use mechanical switches for keys; Licon uses magnetic sensing switches. Because of this difference, and changes in the method of implementing N-key rollover, the circuit configurations are not alike. (Refer to Chapter 2 for keyboard patching.)

The Ohmtec 3270 keyboard simplified circuit (Figure 3-114) uses bit counters driven by the system 64 μs clock to sequentially scan each key position. Recently, keyboards have been modified to use the clock divided by two, to reduce sensitivity to switch bounce. Key depressions, sensed by contact closures, produce output pulses when the keys are scanned. The output pulses gate the associated code combinations from the counters into the holding register, one at a time. Then the keyboard load pulses gate the holding register contents to a parallel-to-serial converter where it is shifted out serially by the 46 μs clock.

Three MOS 80 bit shift registers are used to prevent accidental repeating of the same key character code in the output, and to ensure that an output will occur for each key, even if the key is released prior to receipt of a keyboard load pulse.

The first of these registers (Repeat Prevent) prevents accidental repeating of the same character by blocking the input to the holding register for the second and each succeeding scan of the keyboard circuits while a key is held depressed. Each keyboard output gate pulse is loaded into the shift register where it circulates in synchronism with the keyboard scanning signals. The shift register output inhibits the holding register load gate if the pulse out of the shift register occurs in coincidence with the next keyboard output gate, signifying that a key was held depressed. The shift register is cleared when the key is released. The repeat prevent circuit can be disabled by the repeat key.

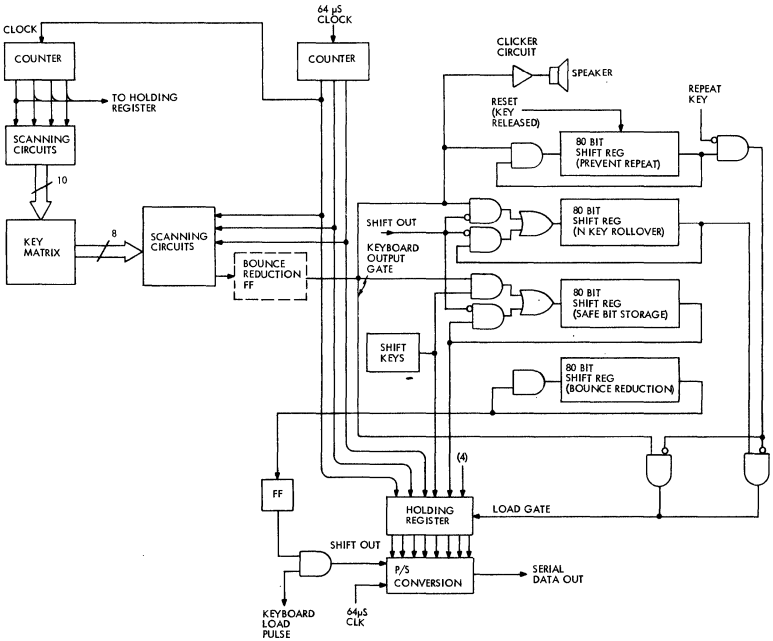


Figure 3-114. Ohmtec Keyboard, Simplified Circuit Diagram

The second 80 bit shift register (N-Key Rollover) provides an N-key roll-over function that ensures that each key depressed is sent, even if the key is depressed and released between keyboard load pulses. It accomplishes this by remembering which keys have been depressed, and supplying this information every keyboard scanning cycle to the holding register until an output of that key occurs. The repeat prevent circuit also ensures that each key code stored in the N-key rollover shift register is only transmitted once. As each character is transmitted, SHIFT OUT removes the associated character pulse from the shift register.

The third shift register provides the same N-key rollover function for the shifted characters. Since the shift key can be activated with any other key this shift register stores the shifted characters. As the characters associated with the pulses held in the shift registers are transmitted, SHIFT OUT removes the corresponding pulses by not allowing them to recirculate.

A few keyboards have been modified to use a fourth shift register and flip-flop to reduce the contact bounce problems by ensuring that the same key can only be transmitted by every other keyboard load pulse, thus providing sufficient time for bounce to settle. In addition, the most recent versions do not use this approach, but utilize a bounce reduction flip-flop in the output of the scanning circuits.

Some configurations have a "clicker circuit" added, providing an audible output to the operator each time a key is depressed.

Patches are supplied to identify those keys that are designated as control keys; i.e., keys that do not generate an output character code, but are used as control functions only. Typical among these is the repeat key. Most keyboards have one or two keys designated as repeat keys, which provide the capability of repeating the output continuously, as long as both the repeat key and the desired key are held down. This is accomplished through the use of contacts on the repeat key which disable the repeat prevent shift register output.

Some models provide an auto-repeat feature that allows a repeat function for selected keys by holding down that key only. (Activation of the repeat key is not required.) A time delay circuit is provided to prevent inadvertent repeat. A key must be held down for at least one second before the repeat function begins. This auto-repeat function is implemented by using a second set of contacts on the selected keys, with the second set acting as a standard repeat key.

One keyboard configuration (4504) provides a 96 position shift register instead of the 80 bit registers previously described. These keyboards do not provide a shift function, since each character is on a separate key. Repeat prevent and N-key rollover are provided in a manner similar to that of the standard systems, but instead of using one 80 bit register, three 32 bit registers are employed.

The Licon keyboards use a magnetic sensing system on the sequential circuitry, and hence are not bothered with contact bounce. The Licon circuit is shown in Figure 3-115. An LSI chip provides the necessary scanning functions, character coding, N-key rollover, repeat prevent/enable, and related functions.

Both keyboard configurations provide the same character coding — basically a modified inverted ASCII.

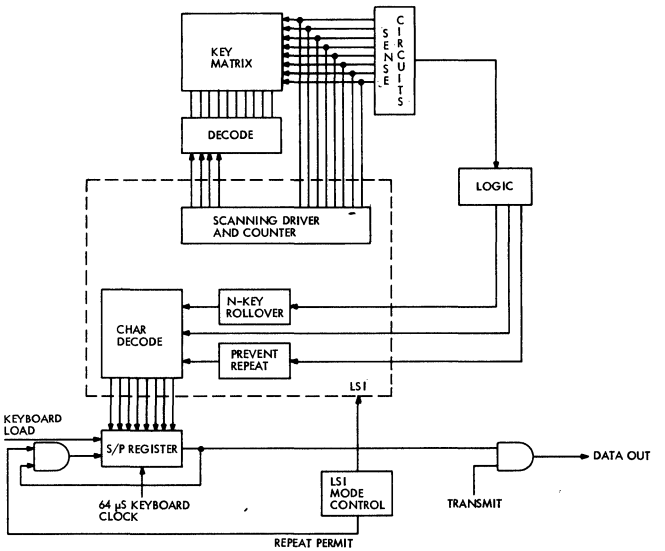


Figure 3-115. Licon Keyboard, Simplified Circuit Diagram

3.4 Power Supplies

3.4.1 General

The dc power supplies used with the PTS-100 system are regulated, solid state, chassis or plug-in board mounted units. They operate from either 115 vac or 230 vac power at 50/60 Hz, and provide almost all the dc voltages required to operate the PTS-100 system. The output voltages are individually adjustable with potentiometers.

3.4.2 Processing Unit Power Supply Circuit Description

a. Processing Units Models 1005, 1008, and 1014

A single plug-in board power supply (SW-2000), 593306, is used in the 1005 or 1014 processing units. The power supply delivers +5, ±12, ±35, and either +24, +28 or +8.5, -15 vdc depending upon the strapping. The Model 1008 processing unit uses a depopulated version of the power supply called SW-2000A. It delivers only +5, +12, and -12 vdc.

b. Processing Units Models 1015, 1020, 1025, and 1030

Two basic power supplies, each available from different procurement sources, are used in the processing unit. Both types have the same basic part number, but have different dash numbers (-1, -2, 3 -10, -11, -12, and -13 are produced by Acme. And -6, -7 and -8 are produced by Faratron). Power Supply 594543-1 (Acme model 61363) and Power Supply 594543-6 (Faratron model FR1183) produce +5, ±12, +24, and +28 output voltages. Power Supply 594543-2 (Acme model 61370) and Power Supply 594543-7 (Faratron model FR1462) are similar to these but with the addition of a ±35 vdc, 2 ampere power supply module. The added module drives local display units (if any). Remote display units are driven by the supply located in the remote concentrator cabinet. Power supplies 594543-11 and 594543-10 are the same as power supplies 594543-1 and 594543-2 except that they have a strapping option to produce +8.6 vdc and -15 vdc for the 16K memory modules. Power supplies -594543-12 and -13 produce only +5 and ±12 vdc. Table 3-24 lists the characteristics of each type of supply.

Table 3-25 shows the power supply voltage outputs for the different configurations. Each PTS-100 processing unit cabinet requires from one to four of either type, depending on the system configuration. Figure 3-116 shows the connections made between each power supply and the 26 board location slots when two power supplies are used in one cabinet. When only one

Table 3-24. Power Supply Specifications

Normal Output Voltage	Output Voltage	Static Current Range (amps)	Dynamic Load (% of Static)	Regulation Band	Noise & Ripple (p-p)
BASIC SUPPLY 594543					
+5	4.9 to 5.4	0 to 35.0 (50)**	5%	±3%	100 MV
+12	-11.4 to -12.6	0 to 1.5 (4.0)*	30%	±3%	100 MV
-12	-11.4 to -12.6	0 to 1.0	30%	±3%	100 MV
+19/-15	18 to 20/-14 to -16	0 to 1.0	50%	±3%	100 MV
+4/+9	3.4 to 4.5/ +8.5 to 9.5	0 to .25	50%	±3%	50 MV
+34.5	34.0 to 35.2	0 to 2.0	10%	±1%	600 MV
-34.5	-34.0 to -35.2	0 to 2.0	10%	±1%	600 MV
115 vac 50/60 Hz		0 to 1.5 amps	(External Fan Power)		
BASIC SUPPLY SW 1000 591667					
+5		4.0			
+12		0.25			
-12		0.25			
+35		1.0			
-35		1.0			
BASIC SUPPLY SW 2000 593306					
+4	2 - 5	0.4	15%	0.2%	100 MV
+5	4.5 - 5.5	22.0	20%	2%	100 MV
+8.5	7.8 - 9.5	0.4	15%	1%	100 MV
+12	11 - 13	0.8 (2.0)†	100%	0.2%	300 MV
-12	11 - 13	0.8	100%	0.2%	300 MV
-15	14 - 16	1.5	50%	2%	150 MV
+20	18 - 21	1.0	50%	2%	150 MV
+24	23 - 25	1.0			150 MV
+28	27 - 29	0.4			150 MV
+35	34.75 ±0.75	0.5	100-	2%	500 MV
-35	34.75 ±0.75	0.5	200%	2%	500 MV
115vac 50/60 Hz	92-138 vac				

*-12 & -13 versions

**-13 version

†Only voltages used on SW 2000A. Also on SW2000A +12V is 2.0 amps.

NEW 1020 & 1025/1030

SEE FIGURE 6-12 FOR THE DC POWER DISTRIBUTION. WHEN TWO POWER SUPPLIES ARE USED, TB1 & 4 AND TB2 & 3 ARE STRAPPED TOGETHER. WHEN ONE POWER SUPPLY IS USED, ALL FOUR TERMINAL BOARDS ARE STRAPPED TOGETHER.

OLD 1020

BOARD LOCATIONS		+5V	+12V	-12V	$V_{SS}V_{DD}$ -15V OR +24V	V_{SX} +8.5V OR +28V
A26	Memory Address 7	▒			▒	▒
A25	Display/Refresh Adapter	▒	▒	▒		
A24	Memory Address 6	▒			▒	▒
A23	Memory Address 5	▒			▒	▒
A22	Display/Refresh Adapter	▒	▒	▒		
A21	Memory Address 4	▒			▒	▒
A20	Memory Address 3	▒			◢	◢
A19	Display/Refresh Adapter	▒	▒	▒		
A18	Memory Address 2	▒			◢	◢
A17	Memory Address 1	▒			◢	◢
A16	Display/Refresh Adapter	▒	▒	▒		
A15	Memory Address 0	▒			◢	◢
A14	Feature Board	▒				
A13	CPU	▒				
A12	I/O Option/Adapter Motherboard	◢	▒	▒		
A11	I/O Option/Adapter Motherboard	◢	▒	▒		
A10	Low Speed Multiplexer	◢	▒	▒		
A9	Adapter Motherboard	◢	▒	▒		
A8	I/O Option Adapter Motherboard	◢	▒	▒		
A7	I/O Option/Adapter Motherboard	◢	◢	◢		
A6	I/O Option/Low Speed Multiplexer	◢	◢	◢		
A5	I/O Option/Adapter Motherboard	◢	◢	◢		
A4	I/O Option/Adapter Motherboard	◢	◢	◢		
A3	I/O Option	◢	◢	◢		
A2	I/O Option	◢	◢	◢		
A1	I/O Option	◢	◢	◢		

NOTE: ±35 VOLTS IS USED ONLY BY THE DISPLAYS THROUGH THE MONITOR CONTROLLERS WHICH MAY BE PLUGGED INTO LOCATIONS A1-A5 (OLD BACKPLANE) OR A2-A5 (NEW BACKPLANE). SEE FIGURES 2-22 AND 2-23. EACH POWER SUPPLY CAN DRIVE UP TO 4 DISPLAYS.

▒ POWERED BY POWER SUPPLY 1 CONNECTED TO UPPER TERMINALS

◢ POWERED BY POWER SUPPLY 2 CONNECTED TO LOWER TERMINALS

NO CONNECTION

Figure 3-116. Model 1020/1025 and 1030 DC Power Distribution to Board Slots

Table 3-25. Processing Unit Power Supply Output Voltages and Configurations

Unit	MEM Type	Power Supply Type	P.S. Qty	Local Display Capability
1020	STD	-11	1/2	Yes
1020M	DAM	-11	1/2	Yes
1025	DAM	-12/-13	1	No
1030	STD	-11	3/4	Yes
1030M	DAM	-11	3/4	Yes

1020/1025/1030 P.S. CONFIGURATION

Output Voltages	+5, ±12, +24, +28, +8.5*, -15*	+5, ±12, +24, +28, +8.5*, -15*, ±35	+5, ±12
Power Supply 594543-	-1, -6 -10*	-2 -7 -11*	-12** -13**

NOTE

See Figure 1-3 for other processing unit configurations.

*Used with 16K memory modules.

**Used with DAM Modules

supply is used, its outputs are connected to the lower terminal strip on the backplane and a jumper cable is used to interconnect the lower and upper terminals to distribute power to the top cabinet card slots.

Functional block diagrams of the power supplies are shown in Figures 3-117 and 3-118. Figure 3-117 shows the Acme model 61370 power supply (594543-2). Acme model 61363 (594543-1) is similar but without the 35 volt model; Acme model 61584 (594543-11) is similar but it has an added regulator bias supply for the 12 vdc regulator and it has a strapping option to produce +8.6 vdc and -15 vdc. Power supply 594543-10 is the same as 594543-11 except for the 35 volt module. Power supply 594543-12 is the same as 594543-10 except it only produces +5vdc @ 35A and +12V @ 4A. Power supply 594543-13 is the same as 594543-11 except the +5 vdc capacity is increased to 50A. In either case, ac input power is fused and strapped for either a 115 or 230 volt source. The input power is then applied to a transformer to supply regulator circuits for all voltages except the ±35 volts, which has its own transformer and regulator self-contained in the module. The transformer secondary voltages are rectified by diodes located on the diode board assembly for all supplies except the higher current 5 volt supply, which has

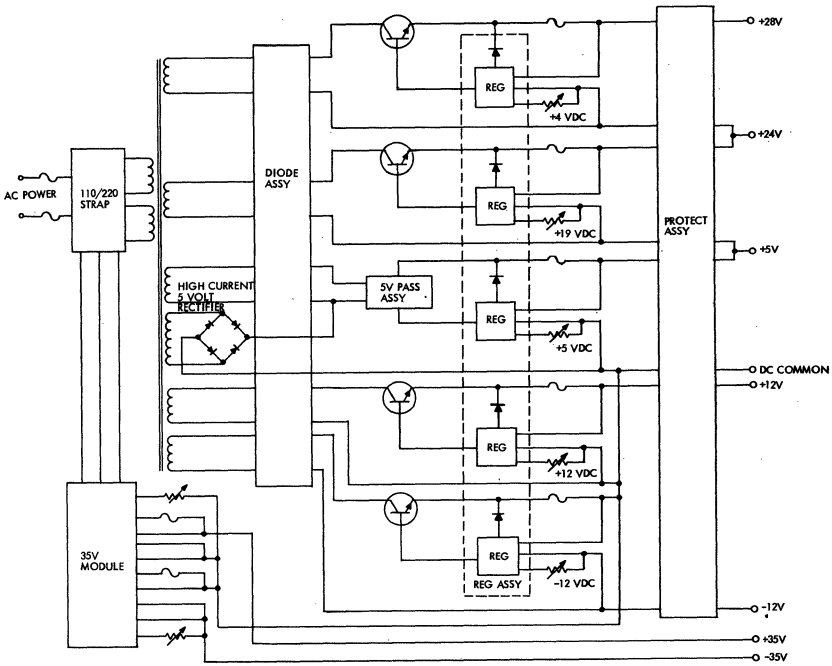


Figure 3-117. Acme 61370 Power Supply for Processor Cabinet

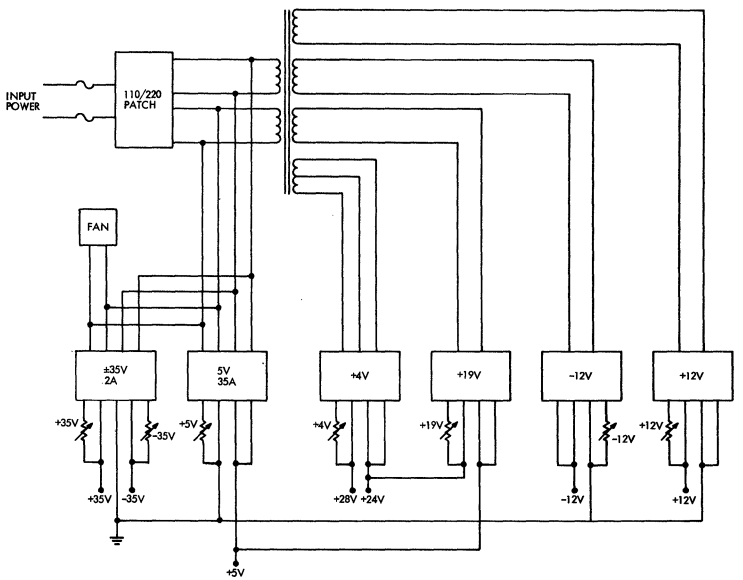


Figure 3-118. Faratron FR1462 Power Supply for Processor Cabinet

its own bridge rectifiers located separately. The rectified outputs are routed through series pass regulators and fuses. (The series regulator for the 5 volt supply contains six transistors in parallel, mounted on a separate pass assembly board.) Each pass regulator is controlled by integrated circuits located on a regulator assembly board. Potentiometers are mounted on these boards to provide adjustment of the regulated output voltage. Holes in the front panel allow screwdriver access to the potentiometers. Finally, overvoltage and reverse voltage protection circuits for most supplies, located on one printed circuit board, provide protection against out of tolerance voltages by making the output crowbar. Voltage regulation and protection circuitry for the 35 volt supply is similar, but it is located in the self-contained module.

Figure 3-118 shows the Faratron model FR1462 power supply (594543-7). Faratron model FR1183 (594543-6) is similar, but without the 35 volt module. In either case, ac input power is fused and strapped for either a 115 or 230 volt source. The input power is then applied to the transformer which supplies low voltages to the -12, +12, +19, and +4 volt power supplies and 115 vac to the ±35 and +5 volt supplies. These two units are completely self-contained with their own step down transformers. Voltage control potentiometers, mounted on the front panel, are wired to each power supply board. All the necessary voltage rectification, regulation, and protection circuits are located on the individual boards. The 4 volt, 5 volt, and 19 volt supplies are used to produce the +24 and +28 volt outputs. This is accomplished by wiring the individual supplies in series.

3.4.3 Remote Concentrator Model 4301 Power Supply Circuit Description

Two basic power supplies are used in the remote concentrator. Power Supply 594438-1 (Acme model 61243 without the high current drop-in module) produces +5, ±12, and ±35 volts output voltages. Power Supply 594438-3 (Acme model 61243 with high current module) produces the same voltages, but has the capability of providing more current at 35 volts (7 amps instead of 2 amps). With the higher current capacity, the latter model is used to drive systems with more than four displays per remote concentrator. The higher current unit can supply up to 16 display terminals.

Figure 3-119 shows the Acme model 61243 (594438-1) without the higher current capability. AC input power is fused and strapped for either 115 or 230 volt operation and applied to a power transformer. The secondary of the transformer is connected to either full wave or bridge rectifiers, applied to a series pass transistor (multiple transistors in parallel for the higher current supplies), fused, and the output voltages applied to an overvoltage and

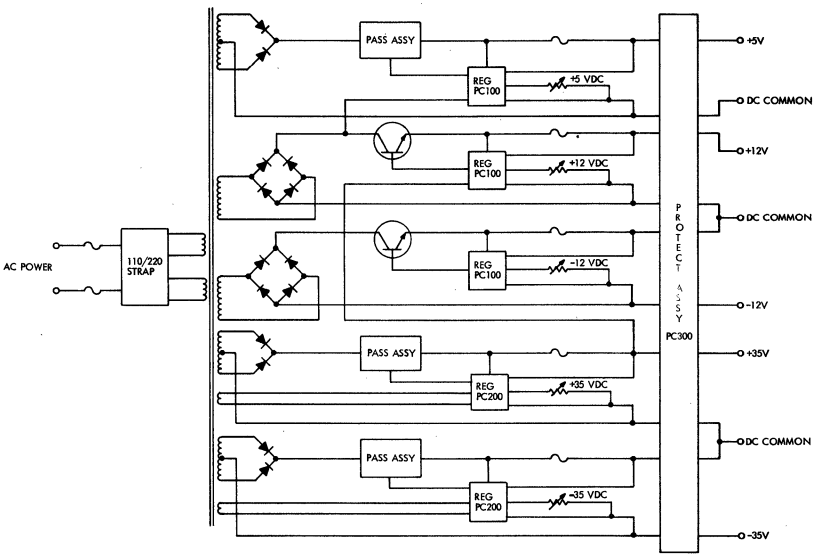


Figure 3-119. Acme 61243 Power Supply for Remote Concentrator Cabinet

reverse voltage protect assembly (PC300). Each series pass transistor assembly is controlled by separate regulator assemblies located on individual printed circuit boards (PC100 and PC200). Output voltage levels are adjustable from the front panel through a screwdriver adjustment slot.

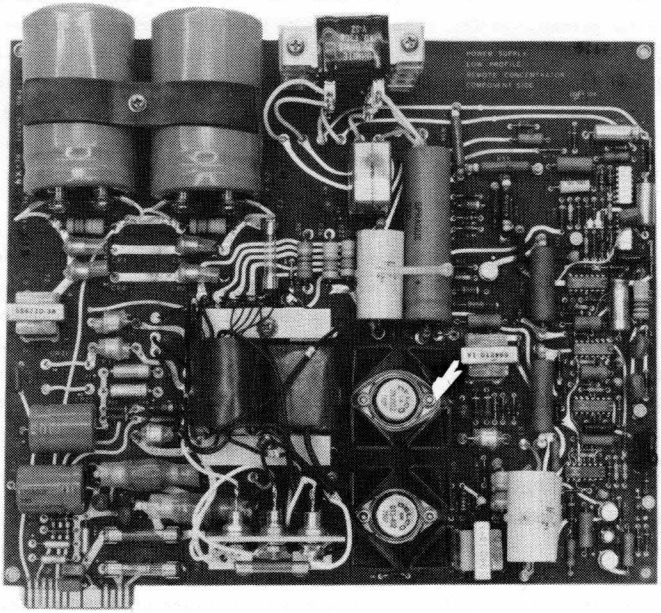
To increase the ±35 vdc to a 7 amp capacity, an extra transformer with added series pass transistors is added to the ±35 vdc power supplies.

3.4.4 Remote Concentrator Model 4302 (Low Profile) Power Supply SW1000 Circuit Description

The low profile remote concentrator uses power supply 591667, which produces +5 vdc, ±12 vdc, and ±35 vdc output voltages at sufficient power to drive two display terminals.

Figure 3-120 shows the power supply and the simplified circuit block diagram. The power supply is a frequency insensitive, high efficiency, switching power supply. It operates at 15 kHz phase locked to the display terminal horizontal line frequency by the PS SYNC signal from the monitor controller.

The input ac line voltage is rectified and applied through the switching regulator and filter to transformer T4. A 230 vac input is applied directly to the rectifier, whereas a 115 vac input is first doubled before being applied to the rectifier.



C75-1851

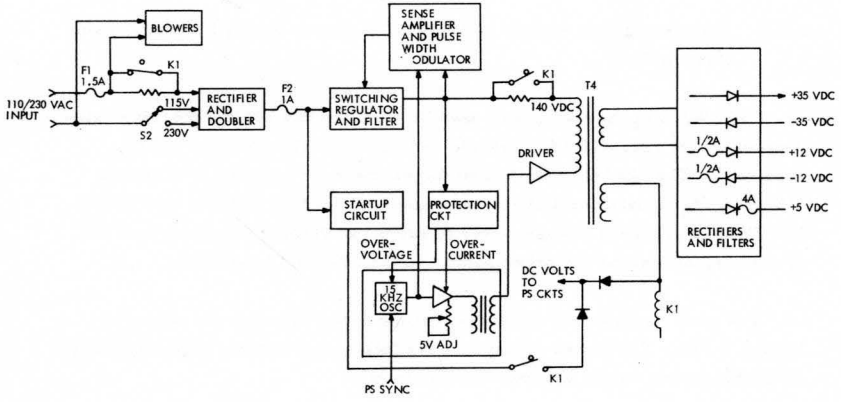


Figure 3-120. Low Profile Remote Concentrator Power Supply

The switching regulator is driven at the 15 kHz switching frequency. The sense amplifier and pulse width modulator sense the regulator output voltage and apply varying width 15 kHz pulses to the regulator to maintain a 140 vdc potential at T4. (The pulse width is directly proportional to the output current.) The driver switches the 140 vdc through T4 at the rate determined by the oscillator (15.6 kHz). The 5V ADJ potentiometer sets the width of the 15 kHz pulses and thereby sets the amplitude of the 140 vdc and output dc voltage levels, which are taken off separate T4 secondary windings, then rectified and filtered.

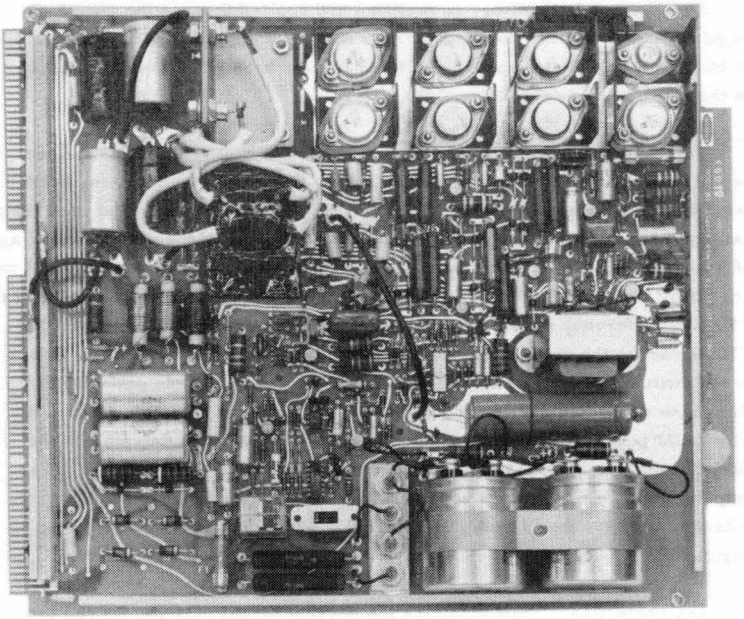
Power for the power supply circuits is obtained by rectifying the output of a separate secondary winding. In this case the rectifier only passes current during the flyback time of T4, which occurs during the display horizontal retrace periods, so the resulting EMI does not affect the display. The same secondary winding also drives relay K1. When K1 is energized its contacts shunt current limiting resistors in the input line and in the 140 vdc line, applying full voltage to the power supply outputs in two steps to prevent shocking the output circuits. Another K1 contact provides dc voltage to the power supply circuits during startup. This is necessary because at startup there is no current flow through the switching regulator and therefore no voltage output to energize the power supply circuits.

The protection circuit monitors the dc voltage amplitude to T4 and the current through T4. When the voltage is too high the protection circuit shuts down the oscillator until the overvoltage condition is corrected. When too much current is drawn through T4 the protection circuit temporarily inhibits the input to the driver and then recycles continuously until the overcurrent condition is removed.

3.4.5 Processing Unit Models 1005 and 1014 Power Supply SW2000 Circuit Description

The SW2000 power supply is used by the 1005 and 1014 processing units. It produces +5 vdc, ±12 vdc, ±35 vdc and +24 vdc, +28 vdc (or -15 vdc, +8.5 vdc). The +24/+28 vdc is used for 8K memory modules 590162; the -15/+8.5 vdc is used for 16K memory modules 593310, 594866, and 594764. The SW2000 produces enough power to drive two display terminals and 32K of memory as well as the other boards in the 1005/1014 systems.

The power supply and simplified circuit block diagram are shown in Figure 3-121. The power supply is a frequency insensitive, high efficiency, switching power supply that operates at 15 kHz.



C75-1857

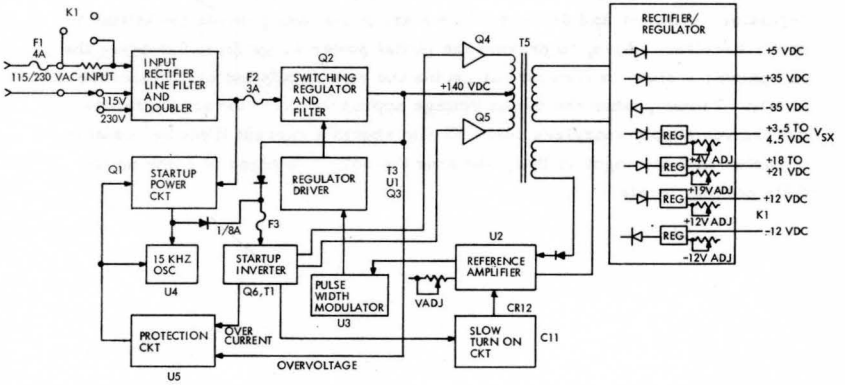


Figure 3-121. Processing Unit Models 1005 and 1014 Power Supply

The input ac line voltage is rectified and applied through the switching regulator and filter to transformer T5. A 230 vac input is applied directly to the rectifier, whereas a 115 vac input is first doubled before being applied to the rectifier.

The switching regulator is driven by the pulse width modulator and the regulator driver, which are in turn driven by the 15 kHz free running oscillator via the startup inverter. The regulator switches on and off at the 15kHz rate applying approximately +140 vdc to the center tap of the primary winding of T5. Class C driver transistors Q4 and Q5 are also alternately switched on and off by the 15 kHz, generating a pulsed 140 volt signal across transformer T5. The reference amplifier senses the voltage at the secondary winding of T5 and causes the pulse width modulator to apply varying width 15kHz pulses to the switching regulator to maintain an approximate 140 vdc potential at T5. The pulse width is directly proportional to the power supply output current. The VADJ potentiometer sets the initial pulse width, which determines the initial amplitude of the 140 vdc and the initial output dc voltage levels. The output voltages are taken off separate T5 secondary windings, rectified, filtered, and, for the ±12 vdc, 18 to 21 vdc, and 3.5 to 4.5 supplies, also regulated.

The protection circuit monitors the current through Q4 and Q5 and the 140 vdc. If either an overcurrent or an overvoltage condition is detected the protection circuit shuts down the oscillator and inhibits the drive to Q4 and Q5.

Switching power supplies require special circuits to provide startup power since at startup there are not dc voltages to operate the switching regulator oscillator and drivers. The startup circuits provide the initial dc power required. Also, to prevent the initial power surge from damaging the equipment, a slow turn-on circuit makes the voltage applied to T5 increase slowly. Finally, when the output voltage approaches its correct amplitude the +12 vdc supply energizes relay K1 and shunts a current limiting resistor in series with the input ac line, allowing the output voltages to come up to their correct levels.

CHAPTER 4. MAINTENANCE

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CHAPTER 4. MAINTENANCE

4.1 General

The PTS-100 Maintenance Concept has two echelons of maintenance: Field maintenance, which takes place on site where modules and selected piece parts are quickly replaced to get the failed unit back into operation, and Depot maintenance, which takes place at area depots where the failed modules are repaired to piece part and returned to stock. This chapter deals primarily with field maintenance.

4.1.1 Field Maintenance

All plug-in boards in the processing unit and remote concentrator and the display terminal CRTs, LED panels, PC boards, and keyboards are replaced on site as required. The processing unit and remote concentrator power supplies, the peripherals, and the fixed circuits mounted on the PTS-100 cabinets are repaired to selected component level on site (selected components being those modules and piece parts that have the highest failure rates). The cassette drive is a replaceable item that is piece part repaired at depot level. Cables are also repaired on-site. Preventive maintenance is performed on site on the peripheral devices and on the PTS-100 power supplies. On-site maintenance is covered by: diagnostic test programs, vendor peripheral maintenance manuals, and the PTS-100 maintenance manual.

4.1.2 Depot Maintenance

Depots located in various geographical areas throughout the world service all the sites in their respective areas. At the depots the failed modules returned from the sites are repaired to piece part level using special test equipment, test jigs, and test procedures provided by Raytheon Data Systems. In general, all procedures and test equipment used in the manufacturing plant board test area are provided to the depots. Peripheral device vendor manuals are used to repair the returned peripheral device modules. Depot maintenance procedures are not covered in this manual.

4.2 Scope

This chapter contains alignment procedures and diagnostic test procedures. The diagnostic tests are structured around troubleshooting flow diagrams, the diagnostic IODC cassette tape and various CE console diagnostic test procedures.

4.3 Test Equipment Required for Field Maintenance

Multimeter with 3% dc voltage accuracy or Fluke 800A

CE console

Oscilloscope*

CIC low speed channel simulator

CIC high speed channel simulator*

Special modem loopback cable

PC board insertion/extraction tool 591800

2-5 inch Daisy chain. Push on insulated terminals, Berg 47843 or 47067.

4.4 Alignment Procedures

4.4.1 Power Supply Output Voltage Adjustments

a. Power Supplies 594543 (except for 1020M and 1030M)

NOTES

This procedure is intended to be performed at installation. If power supply output voltages are known to be reasonably correct, perform only Steps 3 through 5.

The 594543-10, -11 power supplies have the same outputs as the basic supply plus optional +8.5 vdc and -15 vdc selected by external strapping on terminal board TB2 located on the rear of the power supply. If the optional +8.5/-15 volt outputs are selected, the +24/+28 volt outputs will be disabled.

For 8K memory boards that use +24/+28 volts, strap TB2 terminals 1 and 2 together and 3 and 4 together.

For 16K memory boards that use +8.5/-15 volts, strap TB2 terminals 2 and 3 together and 4 and 5 together.

1. Remove ac power from cabinet.

2. Unplug all PC boards from cabinet backplane.

3. Apply power to cabinet and power supply.

*Optional test equipment

4. Using ±3% dc voltmeter measure dc voltages where power supply wiring connects to backplane. Adjust voltages by turning potentiometers on power supply front panel. Make adjustments in order shown as the 24 vdc, 28 vdc and optional 8.5 vdc outputs are made up of other voltage outputs.

Adjust this potentiometer	For this voltage	As measured at this backplane terminal
-12 vdc	-12 vdc	-12 volts
+12 vdc	+12 vdc	+12 volts
-35 vdc	-34.5 vdc	-35 volts
+35 vdc	+34.5 vdc	+35 volts
+5 vdc	+ 5.15 vdc	+5 volts
+19 vdc	+24.15 vdc or -15.0*	+24 volts or VSS/VDD
+4 vdc	+28.15 vdc or +8.65*	+28 volts or VSX

*outputs when strapped for 16K memory modules.

5. When more than one power supply is installed also adjust voltage outputs of second supply.

6. Remove ac power from cabinet.

7. Insert all PC boards into cabinet and connect and turn on any displays.

8. Apply power to the cabinet and power supply.

9. Recheck all dc voltage outputs. If they are not exact, adjust potentiometers. Perform this adjustment in same order as before.

10. Repeat Step 9 for second supply if installed.

b. Power Supplies 594543-11 for 1020M and 1030M

ADJUSTMENT PROCEDURE FOR 1 POWER SUPPLY SYSTEM

Voltage	Test Points (-)	(+)	Adjust Power Supply	Adjust Voltage To	Notes
+5	A17-J2-97	A17-J2-99	1	+5.15	Attach a daisy chain. Push on insulated terminal to (1) meter lead
-12	A17-J2-97	A17-J2-93	1	-12.1	Attach a daisy chain. Push on insulated to both (-) and (+) meter leads.
+12	TB1 (gnd)	TB1 (+12V term)	1	+12.1	Use meter leads with alligator clips.
+35	TB1 (gnd)	TP10*	1	+35.0	Measure voltages at ±35V terminals near A3 on backplane.
-35	TB1 (gnd)	TP11*	1	-35.0	±35V terminals near A3 on backplane

ADJUSTMENT PROCEDURE FOR 2 POWER SUPPLY SYSTEMS

Voltage	Test Points (-)	(+)	Adjust Power Supply	Adjust Voltage To	Notes
+5	A14-J2-97	TP4*	1	+5.15	Attach a daisy chain. Push on insulated terminal to (-) meter lead.
+5	A20-J2-97	TP3*	2	+5.15	Same as above.
-12	A17-J2-97	A17-J2-93	1	-12.10	Attach a daisy chain. Push on insulated to both (-) and (+) meter leads.
-12	A20-J2-97	A20-J2-93	2	-12.10	Same as above.
+12	TB1 (gnd)	TB (+12V term)	1	+12.1	Use meter leads with alligator clips.
+12	TB2 (gnd)	TB2 (+12V term)	2	+12.1	Same as above.
+35	TB1 (gnd)	TP10*	1	+35.0	Same as above.
+35	TB2 (gnd)	TP8*	2	+35.0	Same as above.
-35	TB1 (gnd)	TP11*	1	-35.0	Same as above.
-35	TB2 (gnd)	TP9*	2	-35.0	Same as above.

*See Figure 6-12 for location.

ADJUSTMENT PROCEDURE FOR 3 POWER SUPPLY SYSTEMS

Voltage	Test Points (-)	(+)	Adjust Power Supply	Adjust Voltage To	Notes
+5	A14-J2-97	TP4*	1	+5.15	Attach a daisy chain push on insulated terminal to (-) meter lead.
+5	A20-J2-97	TP3*	2	+5.15	Same as above.
+5	A23-J2-97	TP2*	3	+5.15	Same as above.
-12	A17-J2-97	A17-J2-93	1	-12.1	Attach a daisy chain. Push on insulated terminal to both (-) and (+) meter leads.
-12	A20-J2-97	A20-J2-93	2	-12.1	Same as above.
-12	A23-J2-97	A23-J2-93	3	-12.1	Same as above.
+12	TB1 (gnd)	TB1 (+12V term)	1	+12.2	Use meter leads with alligator clips.
+12	TB2 (gnd)	TB2 (+12V term)	2	+12.2	Same as above.
+12	TB3 (gnd)	TB3 (+12V term)	3	+12.2	Same as above.
+35	TB1 (gnd)	TP10*	1	+35.0	Same as above.
+35	TB2 (gnd)	TP8*	2	+35.0	Same as above.
-35	TB1 (gnd)	TP11*	1	-35.0	Same as above.
-35	TB2 (gnd)	TP9*	2	-35.0	Same as above.

*See Figure 6-12 for location.

ADJUSTMENT PROCEDURE FOR 4 POWER SUPPLY SYSTEMS

Voltage	Test Points (-)	(+)	Adjust Power Supply	Adjust Voltage To	Notes
+5	A14-J2-97	TP4*	1	+5.15	Attach a daisy chain push on insulated terminal to (-) meter lead.
+5	A20-J2-97	TP3*	2	+5.15	Same as above.
+5	A23-J2-97	TP2*	3	+5.15	Same as above.
+5	A26-J2-97	TP1*	4	+5.15	Same as above.
-12	A17-J2-97	A17-J2-93	1	-12.1	Attach a daisy chain. Push on insulated terminal to both (-) and (+) meter leads.
-12	A20-J2-97	A20-J2-93	2	-12.1	Same as above.
-12	A23-J2-97	A23-J2-93	3	-12.1	Same as above.
-12	A26-J2-97	A26-J2-93	4	-12.1	Same as above.
+12	TB1 (gnd)	TB1 (+12V term)	1	+12.2	Use meter leads with alligator clips
+12	TB2 (gnd)	TB2 (+12V term)	2	+12.2	Same as above.
+12	TB3 (gnd)	TB3 (+12V term)	3	+12.2	Same as above.
+12	TB4 (gnd)	TB4 (+12V term)	4	+12.2	Same as above.
+35	TB1 (gnd)	TP10*	1	+35.0	Same as above.
+35	TB2 (gnd)	TP8*	2	+35.0	Same as above.
-35	TB1 (gnd)	TP11*	1	-35.0	Same as above.
-35	TB2 (gnd)	TP9*	2	-35.0	Same as above.

*See Figure 6-12 for location.

c. Power Supplies 594438

Follow the same procedure as that for power supplies 594543 except that the order of adjustment is not critical and only one supply is installed. Also, for the final adjustment ensure that displays are connected and turned on.

4.4.2 Remote Concentrator 4301 Acme Power Supply 594438-3 Rev. A-F 35 Volt Crowbar Adjustment

NOTE

This adjustment should be performed on all Acme Power Supplies 594438-3, Rev. F and lower; Rev. G and higher have been set at the factory. This adjustment reduces the frequency of overvoltage crowbar in the ±35 volt power circuit by increasing the overvoltage "Trip Point" to 37.0 volts.

1. Turn off Power On switch.

2. Remove +35V and -35V connectors from backplane.

3. On power supply, remove cover plate and PC 300; see Figure 4-1.

4. On PC-300 locate +35V and -35V overvoltage adjusting potentiometers; see Figure 4-1.

CAUTION

Adjusting any other overvoltage adjusting potentiometer may cause damage to the equipment.

5. With pencil, mark +35V and -35V overvoltage adjusting potentiometers opposite screwdriver slot on side closest to edge connector.

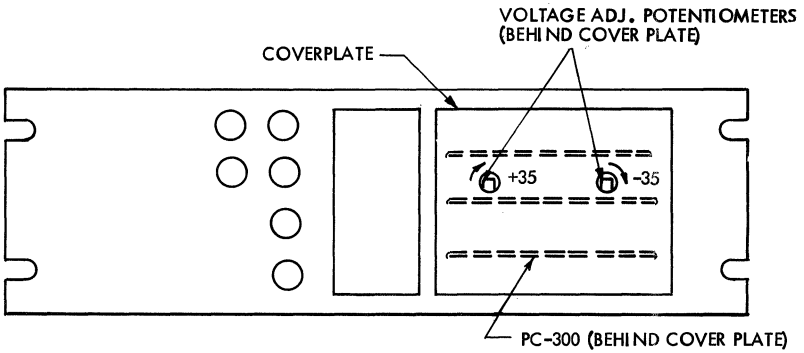
6. Rotate potentiometers to break seal.

7. Return screwdriver slot to position approximately 1/32 inch clockwise from pencil mark.

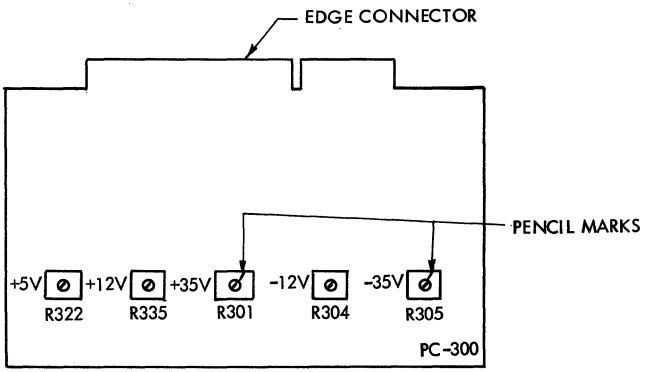
8. Plug PC-300 into power supply.

9. Connect digital voltmeter to +35V output.

10. Turn on Power On switch.



FRONT VIEW ACME 594438-3



PC-300 COMPONENT SIDE

Figure 4-1. Power Supply 594438-3 35V Crowbar Adjustment Potentiometer Locations

11. Using voltage adjusting potentiometers, adjust +35V until meter reading drops. Remember maximum reading on meter. If maximum reading is higher or lower than 37.0 ±0.2 volts, turn off Power On switch, remove PC-300, and repeat Steps 7 through 9 until 37.0 ±0.2 voltage level is obtained.

12. When overvoltage is successfully adjusted to 37.0V ±0.2 on +35V level, readjust output voltage to +34.5V.

13. Repeat Steps 11 and 12 for -35V output.

14. Turn off Power On switch, reconnect +35V and -35V leads to backplane, and reassemble cover plate.

15. Add sticker 310796-1, "±35V OVERVOLTAGE MOD."

4.4.3 Display Alignments

Figure 4-2 shows the location of the display adjustment controls used in the following procedures. Prior to performing an alignment procedure remove the display cover, turn on power on the display and associated processing unit cabinet or remote concentrator. Then adjust the display brightness control until a raster is visible on the display screen. If raster is not bright enough, adjust pre-brightness control R25 on the video amplifier. If excessive blooming, out-of-focus, or too large or too small raster conditions are encountered and no apparent trouble can be isolated, the flyback capacitor, located on terminal board TB1 on the flyback transformer, may be the wrong size. In this case perform the flyback transformer capacitor selection procedure, then repeat the other display alignment procedures. Use care in making all adjustments; perform the adjustments with an insulated screwdriver wherever possible.

4.4.3.1 Raster Centering and Size Adjustments.

1. Adjust Vertical Size control R5 until raster is 6-1/2 inches high.

2. Adjust Horizontal Width control L1 until raster is 9 inches wide.

3. Turn yoke coil on CRT neck and ensure that top and bottom edges of raster are exactly horizontal.

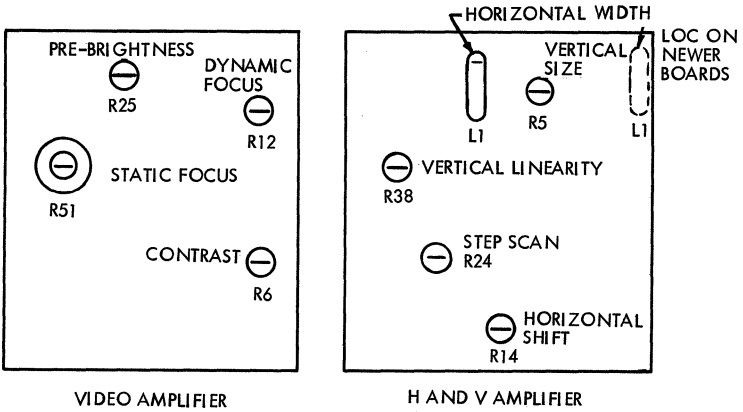


Figure 4-2. Display Adjustments

CAUTION

Avoid contact with the CRT leads since the CRT has 17,000 volts on it.

4. Adjust magnetic centering tabs on deflection coil until raster sides are perpendicular.

5. Repeat Steps 1 through 4 until proper 6-1/2 x 9 inch raster is obtained.

4.4.3.2 Brightness Adjustment.

1. Turn ON/OFF brightness control fully CW.

2. Adjust pre-brightness control R25 until raster just appears on screen. (If raster is too bright, leave R25 fully CCW and perform focus and contrast adjustments; then repeat brightness adjustment.)

4.4.3.3 Focus Adjustment.

1. Adjust Static Focus control R51 so that dots that make up characters in center of screen are round and sharp and show a definite separation.

2. Adjust Dynamic Focus control R12 so that dots that make up characters on edges of screen are round and sharp and show a definite separation.

3. Repeat Steps 1 and 2 to obtain uniformly sharp focus on all parts of screen.

4.4.3.4 Contrast Adjustment.

1. Attach oscilloscope vertical input lead to resistor R2 on video amplifier board.

2. Adjust Contrast Control R6 for a 30 volt ±5 volt p-p signal amplitude of waveform at R2 as viewed on oscilloscope.

3. Perform brightness and focus adjustment.

4.4.3.5 Character Line Centering Adjustment. Adjust Horizontal Shift control R14 so that leading edge of first character on a line is about 1/4 inch to right of raster left-hand edge.

4.4.3.6 Vertical Linearity Adjustment.

1. Measure height of characters on first, middle, and bottom lines.

2. Adjust Vertical Linearity control R38 until characters on these lines are all same height.

4.4.3.7 Flyback Transformer Capacitor Selection Procedure.

1. Turn display interlock switch off.

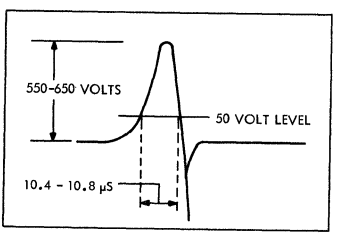
2. Connect scope vertical input to positive side of capacitor C11 on H and V amplifier. Connect scope ground lead to chassis ground.

3. Turn display interlock switch on.

4. Observe waveform at C11 displayed on oscilloscope. It should be as shown below. If it is wider at 50 volt point than 10.4 to 10.8 μs, capacitor across flyback transformer is too large. If waveform is too narrow, capacitor is too small.

5. If waveform is incorrect, turn off interlock switch and substitute the capacitor (typical values between 0.001 μf-0.0047 μf).

6. Repeat Steps 4 and 5 until waveform is within specifications.



4.4.3.8 Step Scan Adjustment. The step scan potentiometer on the old H and V amplifier boards has no effect. On the new boards, set the step scan adjustment for the desired spacing between the horizontal rows of characters. Readjust the vertical height and linearity as necessary.

4.4.4 Power Supply SW1000 Adjustment Procedure

WARNING

Do not make any measurements on the power supply circuits or the test equipment and/or power supply may be damaged. The power supply is not isolated from the input ac line.

NOTE

Do not adjust R33. It is set by the factory.

1. Turn off power.
2. Remove the remote concentrator cover.
3. Remove the two retaining screws from the monitor controller board and swing the board up out of the way.
4. Turn on power and pull up the interlock switch.
5. Connect a ±3% dc voltmeter to the +35V test point near the power on off switch and connect the other voltmeter lead to ground.
6. Adjust potentiometer R25 on the SW1000 for a reading of +34.5 vdc on the voltmeter. Check the -35 vdc at the other test point; it should be -34.5 vdc.
7. Connect the voltmeter to the +5V test point and adjust potentiometer R70 for a reading of +5.15 vdc.
8. Recheck the 35 vdc outputs and readjust as required.
9. Remove the voltmeter, turn off power, and button up the remote concentrator.

4.4.5 Power Supply SW2000/A Adjustment Procedure

WARNING

Do not make any measurements on the power supply circuits or the test equipment and/or power supply may be damaged. The power supply is not isolated from the input ac line.

NOTE

Only use this procedure for power supplies (SW2000) used in systems with 16K memory boards.

Use this procedure only to adjust the power supply output voltage levels (R24, R85, R90, R94, and R98). The remaining adjustments R36, R56 and R116 are factory set. DO NOT readjust these potentiometers.

1. Check and install SW2000/A (also install all other boards).

2. Turn on power.

3. With digital voltmeter (or any ±3% dc voltmeter), measure dc voltages listed below at backplane terminals indicated. Make all measurements in reference to chassis ground. If a voltage is out of tolerance, and +5.15 vdc is out of tolerance adjust potentiometer R24. After +5.15 vdc is correct, note which of the other voltages are out of tolerance. The ±35 vdc outputs are not adjustable.

Adjust This Potentiometer	For This Voltage Reading	As Measured at Backplane For 1005 at J1 Connector Slot A6	Direction of Pot Rotation to Increase Voltage
R24*	+5.15 vdc	Pin 1	CW
	+34.5 vdc** -34.5 vdc** (+35 vdc tracks 5 vdc - no other adjustment is required	Pin 37 Pin 39	
R85	+8.6 vdc**	Pin 7	CCW
R90	-15 vdc**	Pin 5	CW
R94	+12 vdc	Pin 13	CW
R98	-12 vdc	Pin 15	CW

*Adjust R24 first; it controls all voltages.

**Not used on SW2000A

4. Turn off power.

5. Remove power supply.

6. Adjust associated potentiometer(s) in the direction to correct the out of tolerance condition (2 degrees of rotation is equal to 0.1 v change).

7. Reinstall the power supply and repeat Steps 1-6 until all voltages are in tolerance.

4.5 Patch Plug Wiring and Switch Settings

Refer to Chapter 2 and Appendix A.

4.6 Preventive Maintenance

Preventive maintenance procedures for the PTS-100 equipment are given in the PTS-100 Operators Manual (document 44-7645), and in the associated peripheral device vendor manuals. The procedures in the Operators Manual are for operator maintenance. The P.M. intervals and actions are listed in Table 4-1. The preventive maintenance actions, time intervals, and references for the PTS-100 peripheral equipment are given in Raytheon Data Systems Document 44-8046.

Table 4-1. Preventive Maintenance Action Listing

Equipment	P.M. Action	Time Interval	Reference Document
Processing Unit	Clean	3 mos.	PTS-100 Op. Manual
Remote Concentrator	Clean	3 mos.	PTS-100 Op. Manual
Display Terminal	Clean Display Pres.	2 wks. 3 mos.	PTS-100 Op. Manual

4.7 Customer Engineer Console

4.7.1 General

The customer engineer console (Figure 4-3) is used to test and troubleshoot the PTS-100 software and hardware. Its capabilities are:

- Displays contents, statically or dynamically, of the selected processor register (AC, PC, X1, or X2) or absolutely addressed memory location.

C73-244

Figure 4-3. Customer Engineer Console

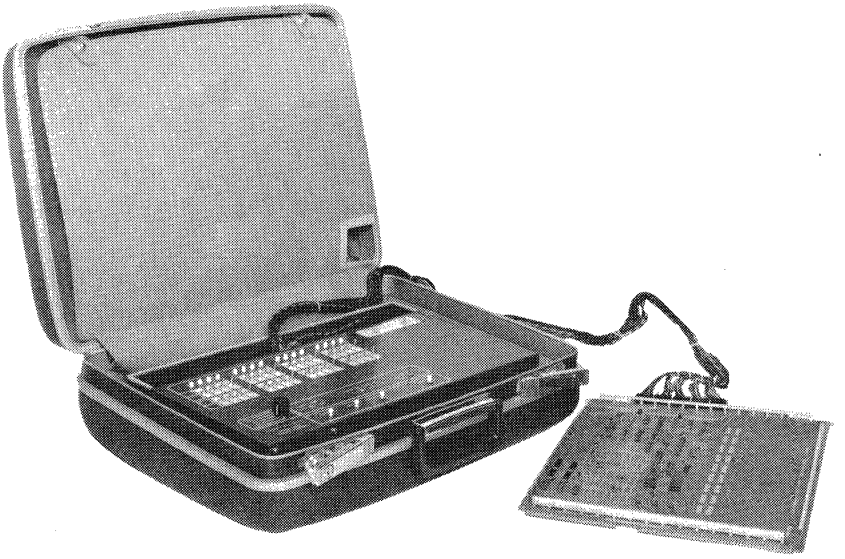
- Provides for entry in absolutely addressed memory location via 16 dual-position switches of instruction or data word in machine (binary) language.

- Controls program execution mode to be single instruction, continuous, or "auto start," i.e., program starts at regular intervals.

The CE console is packaged with an extender card fixture and interface cable in the portable carrying case. It is connected to the PTS-100 system by plugging the cable terminating connector into the system chassis via the extender card (Figure 4-3). The extender card may be inserted in any I/O position having a J1 connector located physically below the central processor.

4.7.2 Operation of CE Console Controls

The CE console controls are shown in Figure 4-4 and described in Table 4-2.



C73-8252

Figure 4-4. CE Console Controls and Indicators

4.8 Troubleshooting Procedures

PTS-100 troubleshooting procedures given in this section are based on the flow charts shown in Figure 4-8. The flow charts describe a general troubleshooting procedure beginning at installation and continuing through loading and operation of the application program. The charts are arranged in order with letters of the alphabet designating convenient entry points for troubleshooting individual devices. These entry points are useful when a trouble has been previously isolated to a particular area. In general, the troubleshooting philosophy used in the flow charts is to locate the fault by 1) visual inspection, 2) voltage checks, 3) CE console tests, and 4) diagnostic tests using the cassette version of the Diagnostic Input-Output Control program. Once the fault is isolated to a replaceable board or module the board or module is replaced. To run the diagnostic tests the Diagnostic Functional Specifications manual is required.

4.9 Diagnostic Programs

4.9.1 General

PTS-100 Diagnostic Programs are available in various forms. However, only the cassette tape versions are covered in this manual. The diagnostic cassette tape contains a processor test program, Diagnostic Input-Output

Table 4-2. Customer Engineer (CE) Console, Controls and Indicators

Control or Indicator	Function
0 through 15 (data indicators)	Display the machine (binary) language contents of a selected register or memory location. Lighted indicators represent the presence of logical 1's. The indicators are grouped in clusters of four to facilitate the determining of hexadecimal equivalents. (Status bits 0-7 are displayed on indicators 0-7. ICB bits are displayed on indicators 8-15.)
ADRS (address switches)	Dual position switches specify absolute address of memory location for use with START, STORE, or DISPLAY functions. Up position (toward indicators) is a logical 1; down is a logical 0. The switches are grouped in clusters of four to facilitate the setting of binary equivalents of hexadecimal addresses.
DATA (switches)	Dual position switches specify machine (binary) language value to be entered by the STORE function in the ADRS addressed memory location. Up position (toward indicators) is a logical 1; down is a logical 0. The switches are grouped in clusters of four to facilitate the setting of binary equivalents of hexadecimal values.
START (switch)	Momentary depression of switch initializes the PTS-100 processor (without resetting I/O), places ADRS set value in the program counter, and begins instruction sequence from this address. Duration of sequence is controlled by STOP, RESET, or MODE functions.
STOP (switch)	Momentary depression of switch halts the PTS-100 processor operation following completion of the in-progress instruction. In-progress I/O activity is not affected. The PTS-100 processor is not reset, i.e., register contents remain current.
CONTINUE (switch)	Momentary depression of switch resumes PTS-100 processor execution of the previously halted (by STOP or MODE) instruction sequence. After release of this switch, the indicators display the contents of the memory absolutely addressed by the ADRS switches. Duration of the instruction sequence is controlled by the STOP, RESET, or MODE functions.

Table 4-2. Customer Engineer (CE) Console, Controls and Indicators (cont)

Control or Indicator	Function
MODE (switch)	This dual position switch controls the number of instructions executed by the PTS-100 processor following depression of START or CONTINUE. The SINGLE INSTR position allows one instruction to be completed. The RUN position allows continuous instruction execution until STOP or RESET is depressed.
RESET (switch)	Momentary depression of switch halts the PTS-100 processor and all I/O activity, and resets the processor and all I/O devices. This switch should be depressed before the start of each operation.
STORE (switch)	Momentary depression of switch deposits the value represented by the DATA switches in the memory location absolutely addressed by the ADRS switches. The Display Select Switch must be in the MEM (memory) position. Note that for the entry of data in sequential memory locations (e.g., loading a diagnostic test sequence of instructions), the ADRS value as well as the DATA value must be altered prior to each depression of STORE. The address does not increment of its own accord.
DISPLAY (switch)	Momentary depression of switch displays the current contents of the selected register or absolutely ADRS (addressed) memory location on indicators 0 through 15. Note that to display the contents of sequential memory locations, the ADRS value (switch positions) must be incremented prior to each depression of DISPLAY.
Display Select Switch	This five-position rotary switch is used to select for display the contents of one of four PTS-100 processor registers (ACC, PC, X1, or X2). The contents of the selected register is displayed when the DISPLAY switch is depressed. In the MEM position of the display select switch, the data at the addressed (ADRS) memory location is displayed.
AUTO START (switch)	In ON position, causes the PTS-100 processor to function as if START were depressed at regular intervals of 2 milliseconds. OFF position disables the automatic starts.
AUTO DISPLAY (switch)	In ON position, dynamically displays the contents of the selected PTS-100 processor register or memory location at regular intervals of 2 milliseconds. OFF position disables the automatic display.

Control (DIOC) program, and the individual diagnostic programs. The processor test program is automatically loaded and executed 100 times at IPL (providing the Interval Timer is not on). If the processor test is successful it loads DIOC. The DIOC sets up the interrupt packets to handle unexpected interrupts and coordinates the input of variables, which determine the input and output devices and diagnostic program selection. The DIOC sets up each interrupt packet to go to a Load Immediate instruction relating to that particular interrupt (i. e., Interrupt level 5 is Load Immediate 5-LDI AC, 5). This is done initially and every time DIOC resumes control. Each individual diagnostic sets up its own interrupt packet(s) upon execution. Packets not set up by the diagnostic remain preset to handle any unexpected interrupts. When an unexpected interrupt not associated with the executing diagnostic occurs, DIOC, which contains a standard printout routine, prints "INT XX UNEXPECTED." (XX is the level.) After that the DIOC executes an Interrupt Return, INR. Once the DIOC program is entered the operator selects the input device to enter the variables. This device may be either a keyboard or the CE console. Using the selected input device the operator enters variables and the name of the diagnostic to be run (Table 4-3). DIOC then loads the diagnostic. The operator controls the execution of the diagnostic by changing various constants in the diagnostic program.

4.9.2 Modes of Operation

4.9.2.1 Equipment Modes of Operation. Three modes of Input/Output device operation can be selected by the operator to run the diagnostic. The operating procedure for each mode is given in Figures 4-5, 4-6, and 4-7. Only mode 1 (Keyboard Input) is automatically allowed by DIOC. Any other input device must be selected manually using the CE console.

4.9.2.2 DIOC Menu. Two types of menus are displayed or printed: the DIOC menu and the diagnostic menu. They both contain facts about a program.

a. DIOC Menu

The DIOC menu is displayed/printed immediately after a hard copy selection is made:

Table 4-3. DIOC PTS-100 Diagnostics on Cassette 933012

Revision E - June, 1978

Module #	Name	Part #	ID	PBC Rev & Last Rel	SCO Number	PFS Rev & Last Rel
01	DIOCCLR	593964	FP	E-12/77	32538	E-12/77
02	PROCTEST	590068	AN	G-09/76	32382	E-06/76
03	DIOCASSA	863458-1	NH	B-09/76	32383	B-09/76
04	DIOCASSB	863458-2	NH	B-09/76	32383	B-09/76
05	RAMBIT	593849	DT	G-09/76	32384	G-09/76
06	MEMTST	933118	MQ	C-03/78	32561	B-03/78
07	MODEMTST	593827	DK	G-06/76		G-06/76
08	PRINTERS	593805	AO	H-03/78	32561	G-03/78
09	PRNTERS2	933488	ZB	A-03/78	32561	A-03/78
10	TICKPASS	593961	FM	F-03/77	32437	F-03/77
11	KEYDISP	593950	FA	E-06/76		D-06/76
12	DISC1	593937	EM	G-06/78	32621	E-12/77
13	DISC2	933317	TY	A-03/77	32437	A-03/77
14	MAGTAPE	933456	YA	B-06/78	32621	B-06/78
15	CIC001TS	863065	HN	C-06/76		A-01/75
16	CIC002TS	863066	HP	C-09/76	32400	A-01/75
-	CIC001/2TS	863064	-	-	32388	C-09/76
17	AMATEST	593850	DU	D-06/76		C-06/76
18	AMASN	593962	FL	F-03/77	32437	E-03/77
19	ADP3270	933290	SW	A-09/76	32389	A-09/76
20	FEATRPL1	863086	JG	D-09/76	32390	B-09/76
21	FEATRPL2	863088	JJ	D-09/76	32391	B-09/76
22	FEATRPL3	863089	JK	D-09/76	32392	B-09/76
23	FEATDIPL	863167	LS	C-09/76	32393	A-06/76
24	FEATRPL5	933157	PG	D-03/78	32561	B-03/77
25	FEATRPL6	933158	PH	C-03/77	32437	B-03/77
26	CCLCUTST	863087	JH	B-06/76		B-06/76
27	CASSETTE	593923	DX	F-09/76	32396	E-09/76
28	PAPERT	593851	DV	D-06/76		C-06/76
29	CARDTST	593823	DE	C-09/76	32397	C-09/76
30	LC50TEST	933402	WE	A-03/77	32437	A-03/77
31	MULTITIC	593960	FU	C-06/76		B-01/75
32	DIOCUTIL	863407	MA	D-06/78	32621	C-12/77
33	MODEMLI	593848	DS	D-09/76	32398	D-09/76

```
"THE FOLLOWING PARAMETERS HAVE BEEN
 SELECTED: - 1.  DISPLAY BUFFER = AA00
             2.  KEYBOARD ADDRESS = BB
             3.  # OF CHAR PER LINE = CC
         *   4.  HARD COPY = MUX D CHAN E
         *       FFFFFF.....................
             5.  FEATURE BOARD DATA -- LOC 04-12
                 GGGG HHHH IIII JJJJ KKKK LLLL MMMM NNNN
                 NOTE:  LOC 00B2 IS HARD COPY DEVICE ADD.
         **      **TYPE <Y> IF ALL OK OR <N> FOR RETRY*
         ***     ATTENTION!!! - PROCTEST NOT RUN!
         ***     INTERVAL TIMER ON-TURN OFF FOR PROCTEST!"
                 AA  = 38 - F8 ———————————— N/A if no display
                 BB  = 9D - 80 ———————————— N/A if no keyboard
                 CC  = 40, 64, or 80 ————————— N/A if no display
                 D   = 0-7
                 E   = 0-7
                 FFFFF..... = TELETYPE, TERMINET, EXTEL..
                      or      CENTRONICS PRINTER
                      or      LINE PRINTER
                 GGGG-NNNN = data in loc 0004(16)-0012(16)
```

---

* If no hard copy, these two lines will be printed as follows:

```
"4.  NO HARD COPY (LOC B2 POS)"
"                              "
```

** In the case of CE console input, this line will be printed as follows:

"CE CONSOLE INPUT-SET LOC B6 TO 0 TO CONT"

*** These two lines will not be printed if the interval timer is off when the initial "PROCTEST" is run.

b. Diagnostic Menu

The diagnostic menu is printed when the control character "D" is typed; the program is restarted at location 0172_{16} (modes 1 and 2, Figures 4-5 and 4-6), or location 0164_{16} (mode 3, Figure 4-7); or when a diagnostic has completed its normal cycle:

```
NAME LOC VALUE XX NAME LOC VALUE ENTER
SUPP 0D06 0000    DELY 0D0C  0004
LOER 0D12 0000    LINE 0D18  000B
LOOP 0D1E 0000    LOPD 0D24  0000
      ↓                    ↓
maximum of 11     maximum of 11
```

The first six constants are common to all diagnostics. The remaining constants are applicable only to the individual diagnostics. Refer to Section 4.9.2.3 for the constants.

4.9.2.3 Constants. The following six constants are part of every diagnostic:

SUPP - Set to 8000 to suppress printouts in diagnostic, or to 1 to suppress start and end of messages.

DELY - Amount of time (approx decimal seconds) to view printouts on display.

LOER - Set to 8000 to loop on any error or to 1 to stall on any error. This is related to a location "#TSUB" set up by diagnostic to which DIOC will return after error printout.

LINE - Display line count minus one (Hex).

LOOP - This is a two function constant. The right two digits indicate the particular subtest to run and if 80 is set in the left byte, to loop on that subtest; i.e., in 80 01, 80 indicates loop on subtest 01.

LOPD - Set to 8000 to loop entire diagnostic.

Refer to the PTS-100 DIOC Diagnostic Function Specifications manual for the other constants, which are different for each diagnostic. Each constant occupies three memory words (i.e., two for the constant name and one for the value).

The word ENTER is displayed after the last constant. If a display is used, a cursor will appear on the next line below the E in Enter.

The operator can display and change the constant at any locations as follows:

a. Enter the 1 to 4 digit (hex) memory location (LOC) of the constant followed by a slash (/). DIOC will display (or print) its contents on the next line.

b. To change the constant at that location enter the changes as follows:

entering single digit 1	goes to memory as 0001
entering two digits 12	goes to memory as 0012
entering three digits 123	goes to memory as 0123
entering four digits 1234	goes to memory as 1234

c. When a change has been made, type a period or a comma to enter the change. If no changes are made, just enter a period or a comma. A period clears the enter area. A comma clears the enter area and causes DIOC to automatically display (or print) the next succeeding memory location.

d. After all the variables are entered, enter R for Run to execute the selected program(s).

4.9.2.4 Memory Copy to Cassette (M1). The DIOC contains a routine that dumps memory to cassette starting at memory location 0080 (the start of DIOC) and continuing through the memory location specified by location 00D4 (TEMP1). The copy memory routine is called by entering :QU, M1 followed by a slash (/) when in the enter diagnostic mode.

4.9.2.5 Memory Dump. When the diagnostic menu is displayed and constants can be entered, the memory can be dumped to the screen or printer 44 locations at a time. To dump memory, enter the starting memory location under ENTER (see diagnostic menu). Then enter a period (.). The contents of the 44 memory locations beginning at the starting memory location will then be dumped to the screen or printer. To dump the next successive 44 memory locations, type a comma. To return to the diagnostic menu, type a slash (/).

4.9.2.6 Conclusion of Diagnostic Test.

a. After the program has been run (assuming no looping), DIOC will resume control. If a display is used, it will display the diagnostic menu again and wait for input as above. If no display is used, only ENTER will be printed on hard copy. If no hard copy, DIOC will stall waiting for LOC 00B6 to be set to 0 to execute diagnostic.

b. When in the change constants mode the operator may select another diagnostic by typing S.

c. If any looping function is chosen by the operator, D (for display diagnostic menu) will have to be entered to stop the looping and return to DIOC control. Also, any test may be stopped by typing D whereupon DIOC will return to displaying the diagnostic menu.

MODE 1 - KEYBOARD INPUT

1. IPL CASSETTE AND WAIT FOR KEYBOARD MESSAGE. "KEYBOARD? S (STD) OR ENTER , . / 0123456789:"
2. ENTER S IF STANDARD KEYBOARD (SEE BELOW) IS USED. OTHERWISE, DEPRESS KEYS IN SEQUENCE, ONE AT A TIME, THAT CORRESPOND TO SYMBOLS AND NUMBERS SHOWN IN STEP 1 FROM THE , THROUGH THE : . FOLLOW THE : BY A SPACE.
3. ENTER NUMBER OF CHARACTERS PER LINE (2 DIGITS).
4. IF NO HARD COPY, ENTER N . IF HARD COPY DESIRED, ENTER FOLLOWING THREE CHARACTERS:
   A. MUX NUMBER - 0-7 (1 DIGIT)
   B. MUX PORT NUMBER - 0-7 (1 DIGIT)
   C. PRINTER DESIRED - T=TTY/TERMINET/EXTEL. C=CENTRONICS, OR L=LINE PRINTER.
5. IF DISPLAYED INFORMATION IS DESIRED, ENTER Y . OTHERWISE, TYPE N TO RESTART.
6. SELECT PROGRAM TO LOAD BY NAME PRECEEDED BY :QU, AND FOLLOWED BY A SLASH (/); (REFER TO TABLE 4-3).
7. WAIT FOR CASSETTE TO START REWINDING.
8. WHEN DIAGNOSTIC MENU IS DISPLAYED, MAKE ANY CHANGES USING SPACE BAR AS A RUBOUT.
9. TYPE R FOR RUN TO EXECUTE DIAGNOSTIC.
10. TYPE D ONCE OR TWICE TO RETURN TO DIAGNOSTIC MENU.
11. TO SELECT ANOTHER DIAGNOSTIC, TYPE S WHEN DIAGNOSTIC MENU IS DISPLAYED.

STANDARD KEYBOARD

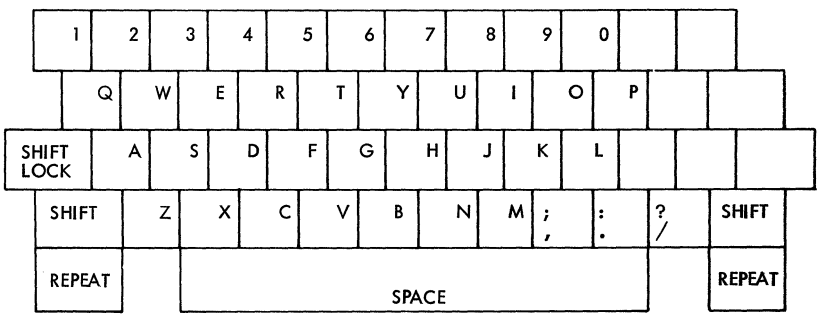


Figure 4-5. Keyboard Input Cassette, Diagnostic Operating Procedures

MODE 2 - TELETYPE INPUT

1. IPL CASSETTE AND WAIT FOR TAPE TO STOP.
2. SET FOLLOWING LOCATIONS IN ORDER, USING CE CONSOLE:
   A. 0084 - SET MUX PORT ADDRESS OF TTY KEYBOARD.
   B. 00B4 - SET TO 0 IF NO DISPLAY OR TO 80XX IF DISPLAY DESIRED; WHERE XX IS NUMBER OF HEX CHARACTERS PER LINE.
   C. 00A8 - IF DISPLAY, SET TO LOCATION OF DISPLAY BUFFER - 3800, 7800, ETC.
   D. 00B6 - SET TO 0000.
3. IF NO HARD COPY, ENTER N. IF HARD COPY DESIRED, ENTER FOLLOWING THREE CHARACTERS:
   A. MUX NUMBER - 0-7 (1 DIGIT).
   B. MUX PORT NUMBER - 0-7 (1 DIGIT).
   C. PRINTER DESIRED - T=TTY/TERMINET/EXTEL, C=CENTRONICS, OR L=LINE PRINTER.
4. IF DISPLAYED INFORMATION IS AS DESIRED, ENTER Y. OTHERWISE TYPE N TO RESTART.
5. SELECT PROGRAM TO LOAD BY NAME PRECEEDED BY :QU, AND FOLLOWED BY A SLASH (/)(REFER TO TABLE 4-3).
6. WAIT FOR CASSETTE TO START REWINDING TO TYPE D AND DISPLAY DIAGNOSTIC MENU.
7. WHEN DISPLAY CONSTANTS ARE DISPLAYED, MAKE ANY CHANGES USING SPACE BAR AS A RUBOUT.
8. TYPE R FOR RUN TO EXECUTE DIAGNOSTIC.
9. TYPE D FOR DISPLAY ONCE OR TWICE TO RETURN TO DIAGNOSTIC MENU MODE.
10. TO SELECT ANOTHER DIAGNOSTIC, TYPE S WHEN IN DIAGNOSTIC MENU MODE.

Figure 4-6. Teletype Input Cassette, Diagnostic Operating Procedures

MODE 3 - CE CONSOLE INPUT

1. IPL CASSETTE AND WAIT FOR CASSETTE TO STOP.
2. SET FOLLOWING LOCATIONS IN ORDER, USING CE CONSOLE:
   A. 00B4 - SET TO 0 IF NO DISPLAY OR TO 80XX WHERE XX IS NUMBER OF CHARACTERS PER LINE.
   B. 00A8 - IF DISPLAY, SET TO LOCATION OF DISPLAY BUFFER - 3800, 7800, ETC.
   C. 008A - IF HARD COPY, ENTER XYZZ WHERE X = MUX NUMBER 0-7, Y = CH NUMBER 0-7, AND ZZ = ASCII CODE FOR PRINTER DESIRED (T, C, OR L). SEE TABLE BELOW.
   D. 00B6 - SET TO 0000.
3. WHEN READY TO ENTER DIAGNOSTIC NAME (REFER TO TABLE 4-3), SET 00B6 TO 0.
4. WHEN CASSETTE STOPS, ENTER ASCII CODE LETTERS IN LOCATION "INPUTI" (ADDRESS AT LOC D2) FOR DIAGNOSTIC DESIRED - 8 CHARACTERS MAXIMUM; CONSULT TABLE BELOW FOR ASCII CODES.
5. SET LOCATION 00B6 TO 0000.
6. WHEN CASSETTE STOPS, SET LOC 00A4 TO 0000.
7. IF HARD COPY AND/OR DISPLAY, WAIT FOR DIAGNOSTIC MENU TO BE PRINTED.
8. MAKE ANY CHANGES VIA CE CONSOLE.
9. SET LOCATION 00B6 TO 0 AGAIN.
10. TO RETURN TO DIAGNOSTIC MENU:
    A. DEPRESS STOP AND RESET ON CE CONSOLE.
    B. RESTART AT LOCATION 0164.
    C. REPEAT STEPS 7 THROUGH 9 ABOVE.
11. TO SELECT ANOTHER DIAGNOSTIC:
    A. DEPRESS STOP AND RESET ON CE CONSOLE.
    B. RESTART AT LOCATION SPECIFIED IN LOC 0176.
    C. ENTER DIAGNOSTIC NAME AS IN STEP 4 ABOVE.
    D. REPEAT STEPS 5 THROUGH 9 ABOVE.

ASCII CODES FOR MODE 3

SPACE = A0	0 = B0	0 = C0	P = D0
! = A1	1 = B1	A = C1	Q = D1
" = A2	2 = B2	B = C2	R = D2
# = A3	3 = B3	C = C3	S = D3
$ = A4	4 = B4	D = C4	T = D4
% = A5	5 = B5	E = C5	U = D5
& = A6	6 = B6	F = C6	V = D6
' = A7	7 = B7	G = C7	W = D7
(= A8	8 = B8	H = C8	X = D8
) = A9	9 = B9	I = C9	Y = D9
* = AA	: = BA	J = CA	Z = DA
+ = AB	; = BB	K = CB	[= DB
, = AC	< = BC	L = CC	\ = DC
- = AD	= = BD	M = CD	] = DD
. = AE	> = BE	N = CE	↑ = DE
/ = AF	? = BF	O = CF	← = DF

NOTE: ALL ABOVE IS IN RIGHT BYTE - EXA. - A = 00C1

Figure 4-7. CE Console Input Cassette, Diagnostic Operating Procedures

4.10 Miscellaneous CE Console Programs

4.10.1 CE Console Program to Load and Execute an Order to any Low Speed I/O Device

1. Connect CE Console to PTS-100 Processing Unit and turn on power.

2. Load the following program:

LOC	CONTENTS	
0020	2100	
0022	3800	BYTE ADDRESS
0024	C009	STORE BYTE ADDR IN LOC 0012
0026	2100	
0028	FFF0	BYTE COUNT (16 BYTES)
002A	C00A	STORE BC IN LOC 0014
002C	20XX	XX = DEVICE ADDRESS (00 FOR CASSETTE)
002E	3808	DIO TO LOC 0010
0030	2100	
0032	10XX	XX = DEVICE ADDRESS (00 FOR CASSETTE)
0034	E800	LOAD STATUS* INTO LOC 0000
0036	0284	JMP BACK TO 0030 TO READ STATUS
0010	XXXX	XXXX - DEVICE ORDER CODE

Set in desired device address and order code. *

3. Execute program by setting CE Console ADRS switches to Location 0020 and depressing CE Console RESET and START buttons.

4.10.2 CE Console Single Record Tape-to-Tape Transfer Procedure

1. Perform Steps 1-3 in Section 4.10.1 with Rewind order (0300) into Location 0010.

2. Check Location 0000 for BOT status before proceeding.

*Refer to Tables 3-6 and 3-7 for order codes and status bit assignments. ICB bit assignments are shown in Section 3.1.9.2.

3. Set Read order (0000) into 0010 and execute (Step 3 of 4.10.1).

4. Read Byte Address (BA) in location 3800. Subtract 6 from BA and enter result into Location 0022.

5. Read Byte Count (BC) in location 3802. Subtract 6 from BC and enter result into Location 0028. (This increases BC by 6 since it is in 2's complement.)

NOTE

(For Information Only)
The transfer address is in location 3804.

6. Set Rewind order (0300) into location 0010 and execute (Step 3 of 4.10.1).

7. Check location 0000 for BOT status before proceeding.

8. Set Read order (0000) into location 0010 and execute (Step 3 of 4.10.1).

9. Check that byte count in location 0014 is zero and status in location 0000 is correct before proceeding.

10. Replace cassette with blank cassette with Write tab on.

11. Set Rewind order (0300) into location 0010 and execute (Step 3 of 4.10.1).

12. Check location 0000 for BOT status before proceeding.

13. Set Write order (0100) into location 0010 and execute (Step 3 of 4.10.1). Transfer is complete when byte count in location 0014 goes to zero. If status in location 0000 is not correct at byte count zero, repeat Steps 11 through 13.

4.10.3 CE Console Multirecord Tape-to-Tape Transfer Procedure

1. Perform Steps 1 through 3 of 4.10.2.

2. Read and record byte address in location 3800 and byte count in location 3802.

3. Depress CE Console RESET.

4. Execute previously entered Read order (0000) (Step 3 of 4.10.1).

5. Repeat Steps 2, 3, and 4 and record byte address and byte count for each record on tape.

6. Depress CE Console RESET.

7. Set Rewind order (0300) into location 0010 and execute (Step 3 of 4.10.1). Check for BOT status in location 0000 before proceeding.

8. Subtract 6 from each recorded byte address and byte counts (Steps 4 and 5 of 4.10.2). Record results.

9. Set new computed byte address and byte count for first record into locations 0022 and 0028, respectively (Steps 4 and 5 of 4.10.2).

10. Set Read order (0000) into location 0010 and execute (Step 3 of 4.10.1).

11. Check that byte count goes to zero in location 0014 and that status in location 0000 is correct before proceeding.

12. Remove tape cassette.

13. Set Rewind order (0300) into location 0010 and execute (Step 3 of 4.10.1).

14. Install blank tape cassette on drive.

15. Set Write order (0100) into location 0010 and execute (Step 3 of 4.10.1).

16. Check that byte count goes to zero in location 0014 and that status in location 0000 is correct before proceeding. If status indicates a CRC error (bit 5) put Backspace order (0200) into location 0010 and execute (Step 3 of 4.10.1). Tape will rewind to beginning of record. Then repeat Step 15.

17. Remove cassette from drive.

18. Put original cassette back onto drive.

19. Repeat Steps 9 through 18 setting in byte address and byte count for each successive record.

20. After last record has been transferred to new tape, remove tape cassette.

4.10.4 CE Console Read I/O Device Status Program

1. Connect CE Console to PTS-100 Processing Unit.

2. Load following program:

LOC	CONTENTS	
0000	2100	LOAD STATUS TO AC
0002	10 (XX)	XX = DEVICE ADDRESS
0004	E808	READ STATUS INTO LOC 0010
0006	0000	JMP TO LOC 0000

3. Set ADRS switches to Location 0000.

4. Depress RESET and then START.

5. Set ADRS switches to Location 0010.

6. Read I/O device status in Location 0010 (refer to Table 3-7).

4.10.5 CE Console Disc Test Procedure

See Figure 4-8, G1.

4.10.6 CE Console Memory Test Procedures

See Figure 4-8, A1 and A3.

4.10.7 CE Console Processor Test Procedure

See Figure 4-8, A4.

4.10.8 CE Console Display Test Procedure

See Figure 4-8, E2.

4.10.9 CE Console Check for Interchange Address

See Figure 4-8, H.

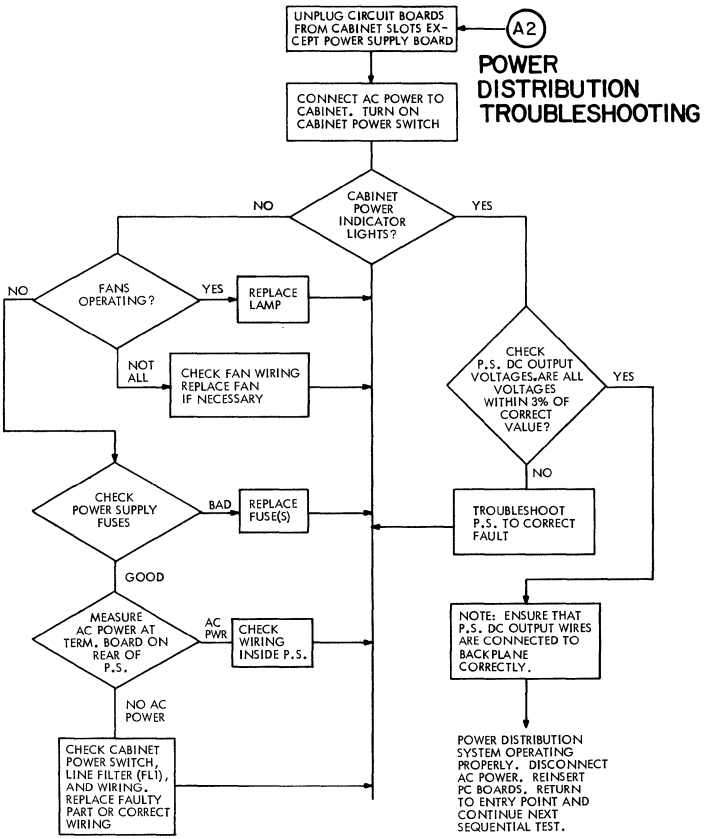


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 1 of 17)

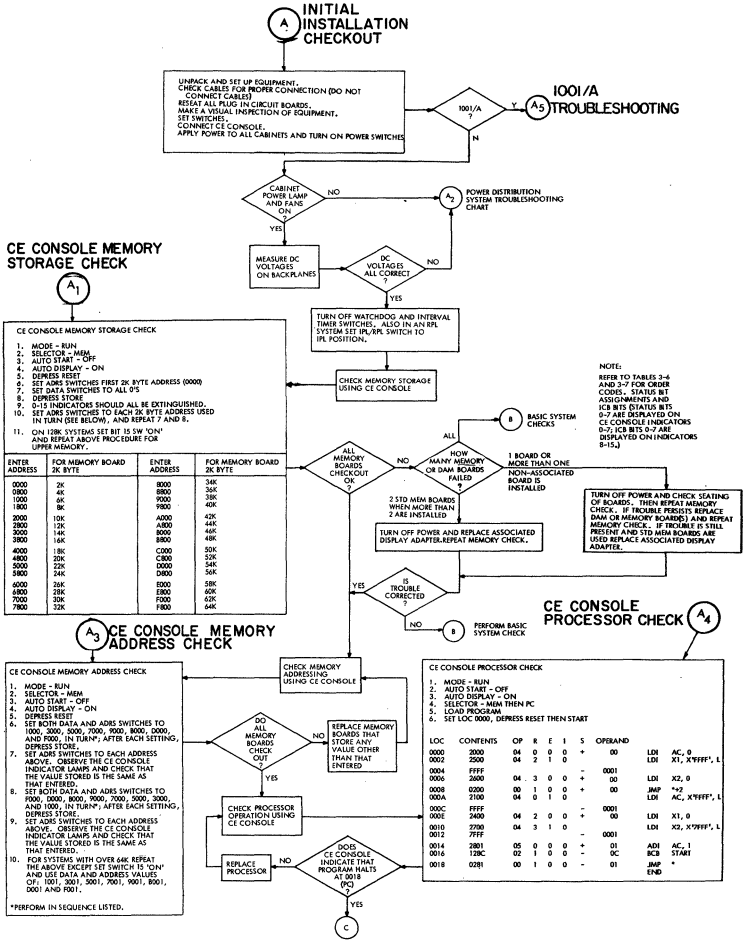


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 2 of 17)

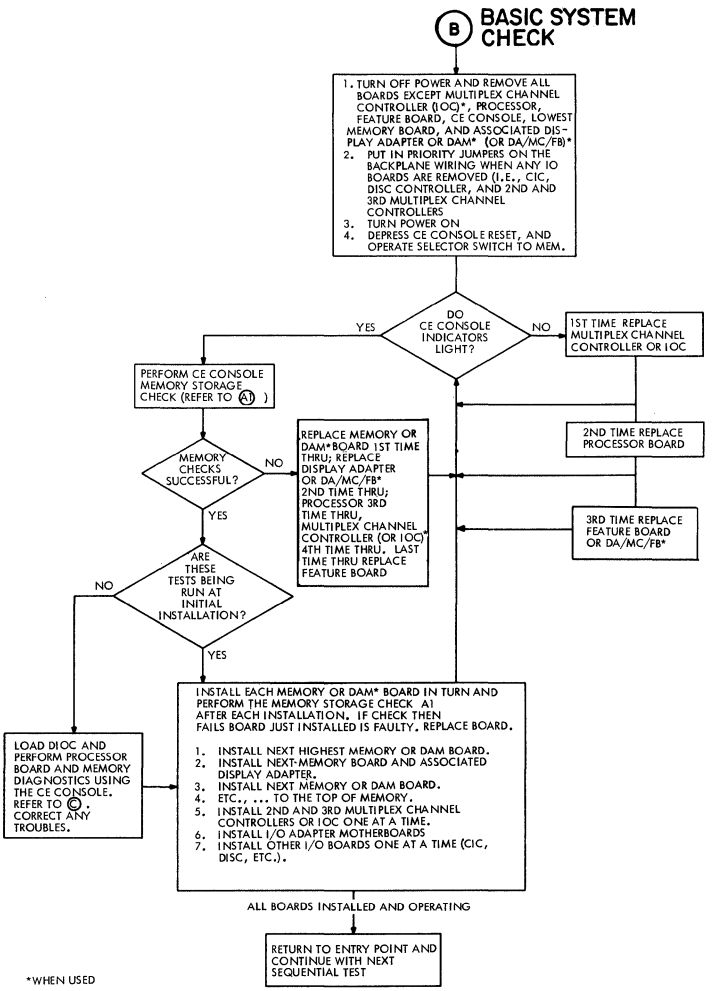


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 3 of 17)

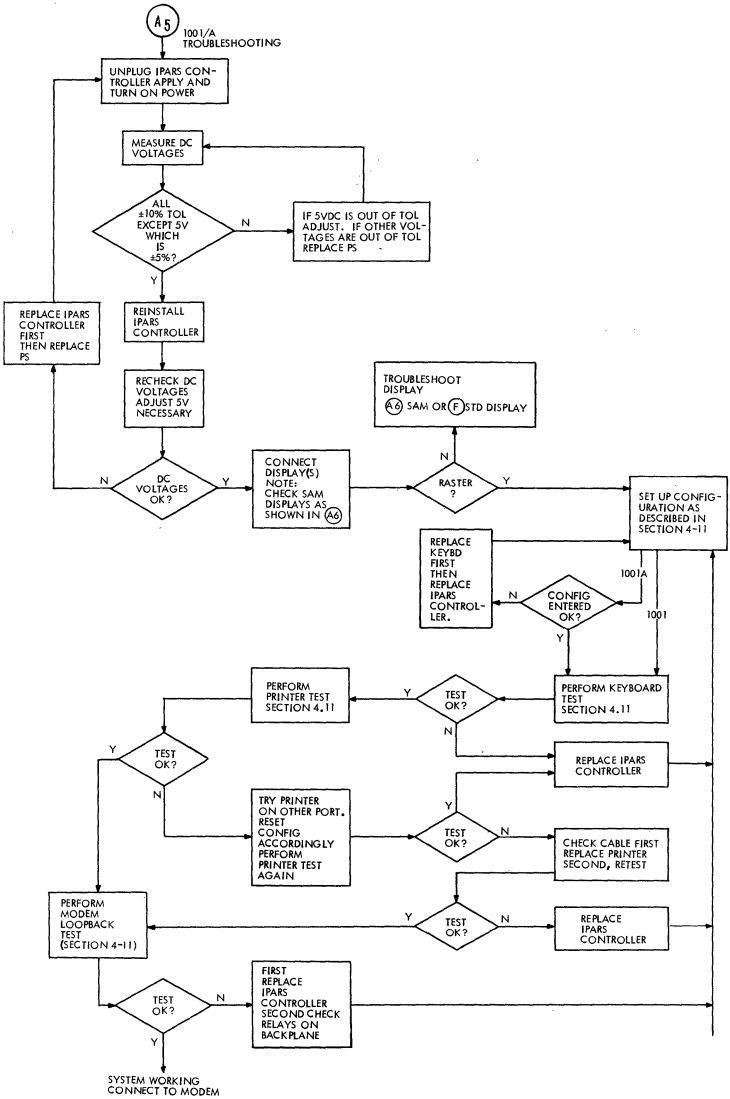


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 4 of 17)

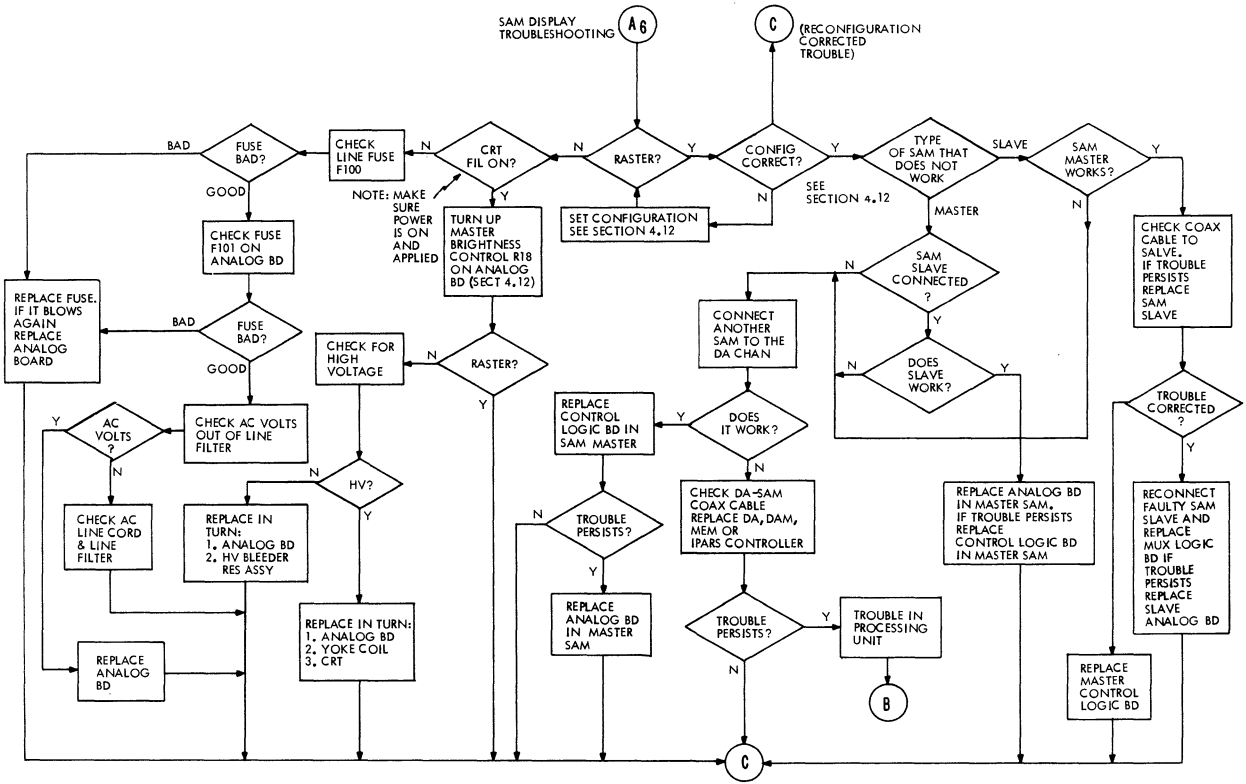


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 5 of 17)

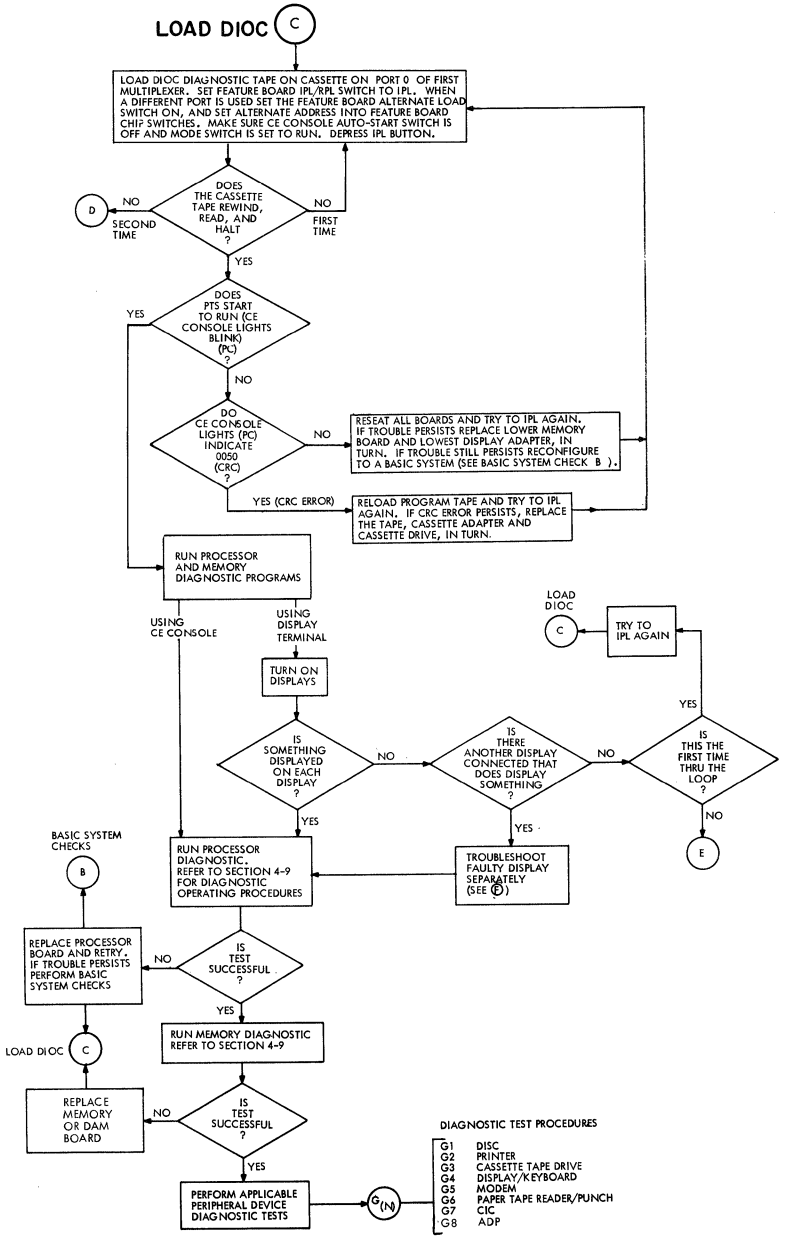


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 6 of 17)

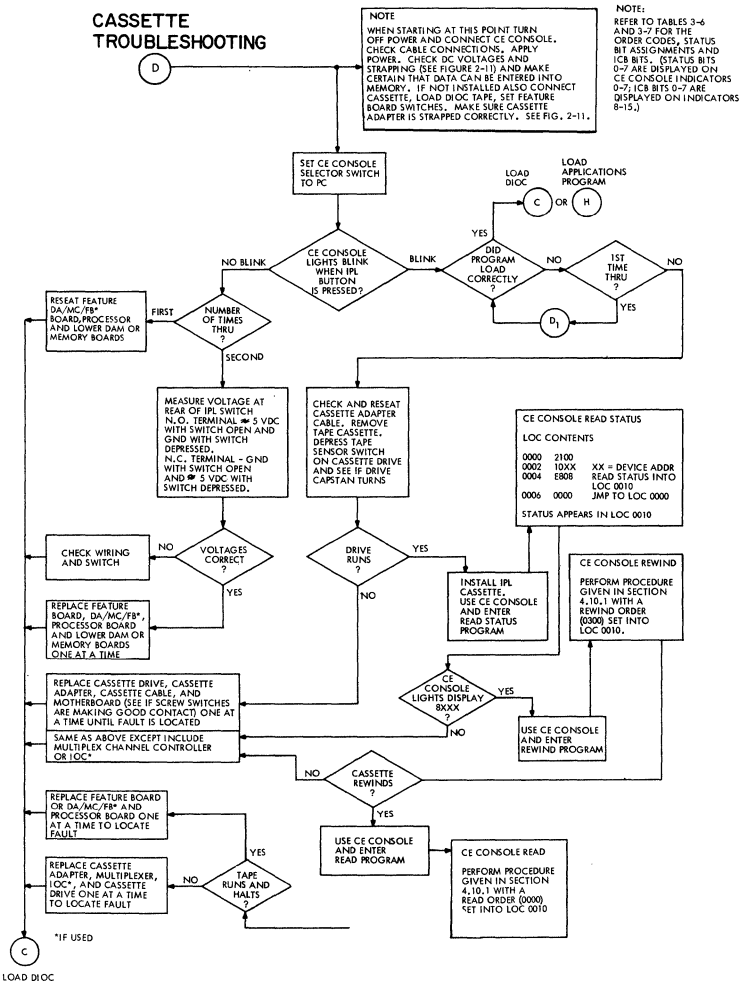


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 7 of 17)

D_1 CASSETTE CHECKS

VISUAL IPL PROBLEM		CE PANEL INDICATION	PROBABLE REASONS	PROBABLE CAUSES	CORRECTIVE ACTIONS
WDT DISABLED	WDT ENABLED				
1. TAPE MOVES FORWARD INDEFINITELY ON FIRST IPL. NORMAL VISUAL IPL CYCLE ON SECOND IPL. (NOTE 1)			TAPE WORN AT "END OF RECORD" AREA AND/OR HEADS ARE DIRTY RESULTING IN TAPE STICKING TO HEAD.	1) ROUGHNESS OF TAPE HEADS 2) EXCESSIVE USE OF THIS TAPE.	1) CLEAN HEADS.
2. NORMAL VISUAL IPL CYCLE EXCEPT TAPE DOES NOT STOP FORWARD MOTION UNTIL "END OF TAPE" IS REACHED ($\approx$ 6 MINUTES)	NOTE 2		1) CASSETTE DATA TRACK IS BLANK. 2) DATA PREAMBLE IS NOT RECOGNIZED. 3) CRC GAP IS NOT RECOGNIZED.	1) BLANK TAPE SHIPPED IN ERROR. 2) EXCESSIVE WEAR ON TAPE. 3) DUST/DIRT ON TAPE/HEAD. 4) CASSETTE DRIVE/ADAPTER MALFUNCTION.	1) RETRY TAPE 2) RUN CASSETTE DIAGNOSTIC 3) USE A NEW TAPE.
3. NORMAL VISUAL IPL CYCLE EXCEPT TAPE DOES NOT STOP FORWARD MOTION WITHIN 34 SECONDS BUT DOES STOP BEFORE "END OF TAPE" IS REACHED.	NOTE 2		BEGINNING OF EMULATOR PROGRAM BEGINS TOO FAR DOWN THE TAPE.	BAD STOP IN EARLY SECTION OF TAPE. TAPE WAS NOT CHECKED FOR 34 SECOND LOAD TIME REQUIREMENT.	OBTAIN NEW TAPE IF SYSTEM OPERATION WITH WDT IS REQUIRED; OTHERWISE USE AS IS.
4. NORMAL VISUAL IPL CYCLE, BUT SYSTEM DOES NOT ACTIVATE, I.E., NO CURSOR ON SCREEN.	NOTE 3	(MEM.LOC) $0064_{16} \neq 0$ OR (MEM.LOC) $006C_{16} \neq 0$ $0040_{16} < (P.C.) < 0050_{16}$ (ACC.) = 0000	ONE OR MORE DATA BITS MISSED DURING READ OF TAPE. FALSE CRC GAP OR FALSE E.O.T. SENSED IN EXTREME CASE.	1) EXCESSIVE WEAR ON TAPE 2) DUST/DIRT ON TAPE/HEAD 3) PORTIONS OF DATA AND/OR CLOCK TRACK MAGNETICALLY ALTERED/ERASED 4) CASSETTE DRIVE/ADAPTER MALFUNCTION.	1) RETRY TAPE 2) RUN CASSETTE DIAGNOSTIC 3) USE A NEW TAPE.
5. SAME AS 4 ABOVE	NOTE 3	(MEM.LOC) $0064_{16} = 0$ AND (MEM.LOC) $006C_{16} = 0$ $(P.C.) = 0050_{16}$ (ERROR CONDITION) $(ACC.) = 0400_{16}$ (CRC ERROR)	ALL DATA BITS READ. ONE OR MORE BITS ARE IN ERROR. ∴ CRC ERROR	1) EXCESSIVE WEAR ON TAPE 2) DUST/DIRT ON TAPE/HEAD 3) CASSETTE DRIVE/ADAPTER MALFUNCTION.	1) RETRY TAPE 2) RUN CASSETTE DIAGNOSTIC 3) USE A NEW TAPE.
6. SAME AS 4 ABOVE	NOTE 3	(MEM.LOC) $0064_{16} = 0$ AND (MEM.LOC) $006C_{16} = 0$ $3000_{16} \leq (P.C.) \leq 4000_{16}$ (MEM.LOC) WHOSE ADDRESS IS EQUAL TO $(P.C.)$ IS 0281_{16}	FEATURE BOARD CONFIG. SWITCH SETTINGS ARE INCORRECT. PROGRAM STALL AT MEM. LOC. EQUAL TO (P.C.) NOTE: CASSETTE SYSTEM IS WORKING PROPERLY.	1) FEATURE BD CONFIG. SWITCHES DO NOT REFLECT SYSTEM CONFIG. AND/OR ADDRESSING. 2) MALFUNCTIONING CONFIG. SWITCH OR A CONFIG. SWITCH NOT FULLY DEPRESSED.	RECHECK FEATURE BOARD SWITCH SETTINGS.
7. NORMAL VISUAL IPL SYSTEM ACTIVATES; I.E., CURSOR ON SCREEN - BUT SYSTEM HANGS AFTER A SHORT TIME	NOTE 4		ERROR IN PROGRAM OPERATION NOTE: CASSETTE SYSTEM IS WORKING PROPERLY.	1) HARDWARE MALFUNCTION IN OTHER THAN CASSETTE SYSTEM 2) IMPROPER GENERATION OF ORIGINAL PROGRAM TAPE 3) PROGRAMMING ERROR 4) SYSTEM PROBLEM.	1) RUN SYSTEM DIAGNOSTICS.

NOTES:
1. NORMAL VISUAL IPL CYCLE WITH WDT DISABLED: REWIND TO B.O.T. - STOP - IMMEDIATE FORWARD - STOP (ALL WITHIN 34 SECONDS)
2. NORMAL VISUAL IPL CYCLE - STOP IS FOR LESS THAN A SECOND. - THEN OPERATION REPEATS AGAIN BEGINNING WITH REWIND TO B.O.T. - THIS LOOP WILL CONTINUE INDEFINITELY.
3. NORMAL VISUAL IPL CYCLE - STOP IS FOR A PERIOD OF SECONDS - THEN OPERATION REPEATS AGAIN BEGINNING WITH REWIND TO B.O.T. - THIS LOOP WILL CONTINUE INDEFINITELY.
4. NORMAL VISUAL IPL CYCLE - STOP IS FOR A PERIOD OF SECONDS TO MINUTES UNTIL PROGRAM HANGS. - THEN THE OPERATION REPEATS AGAIN BEGINNING WITH REWIND TO B.O.T.

Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 8 of 17)

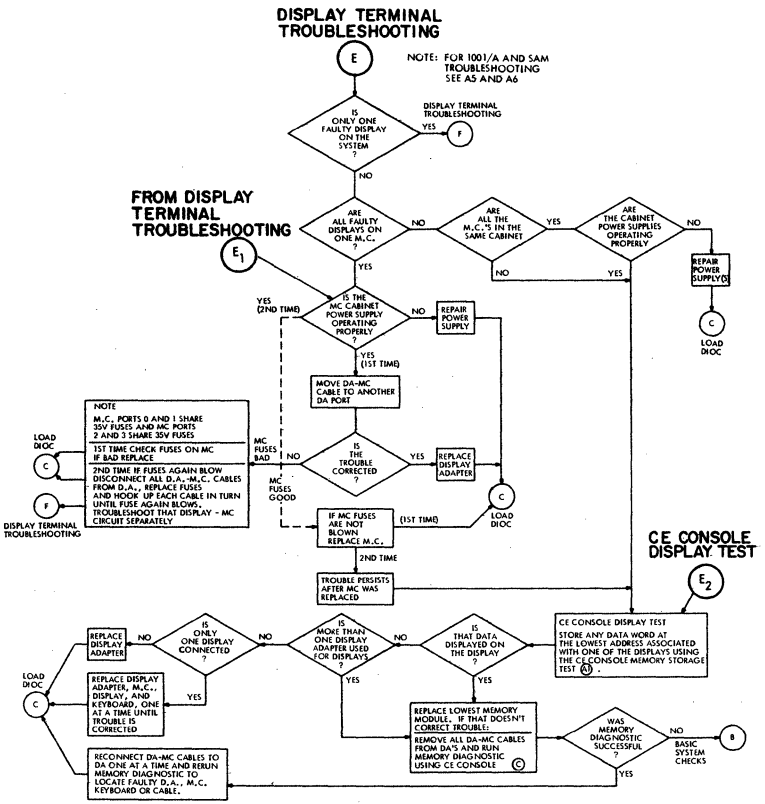


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 9 of 17)

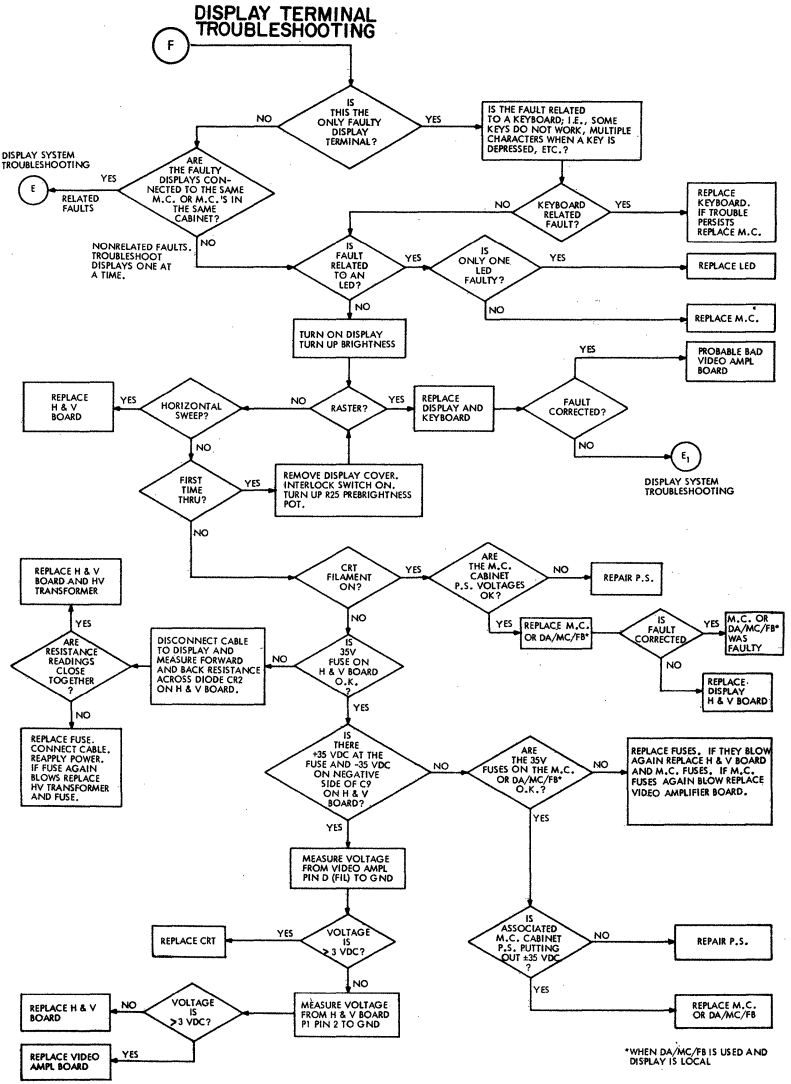


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 10 of 17)

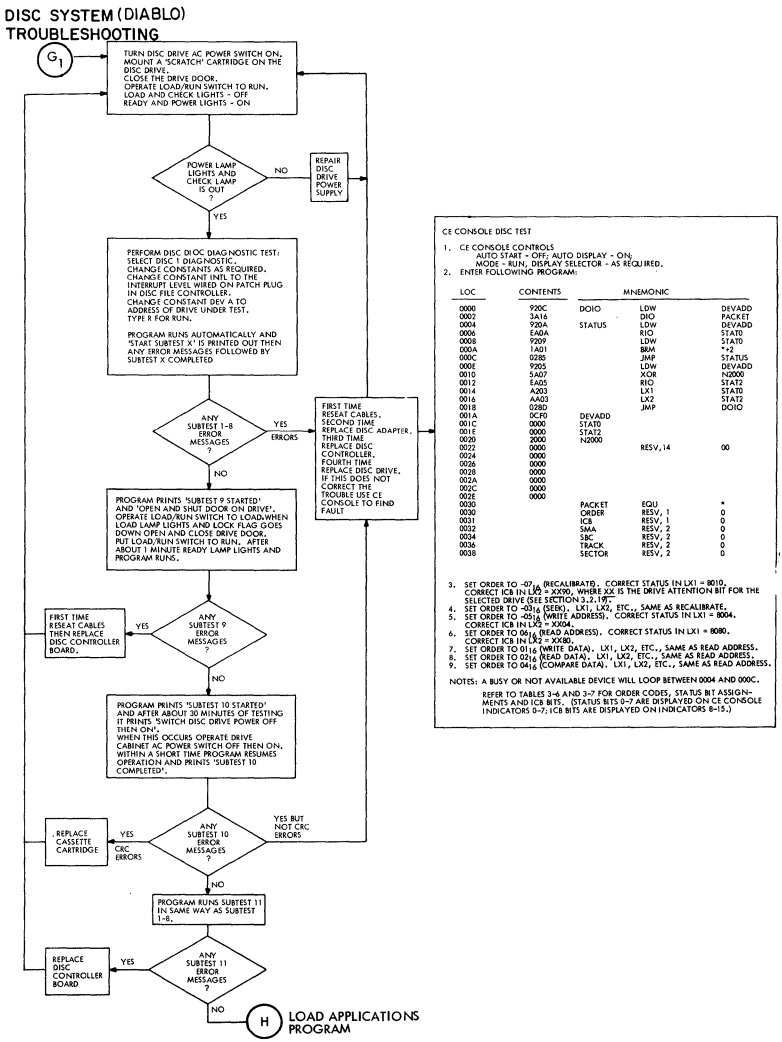


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 1 of 17)

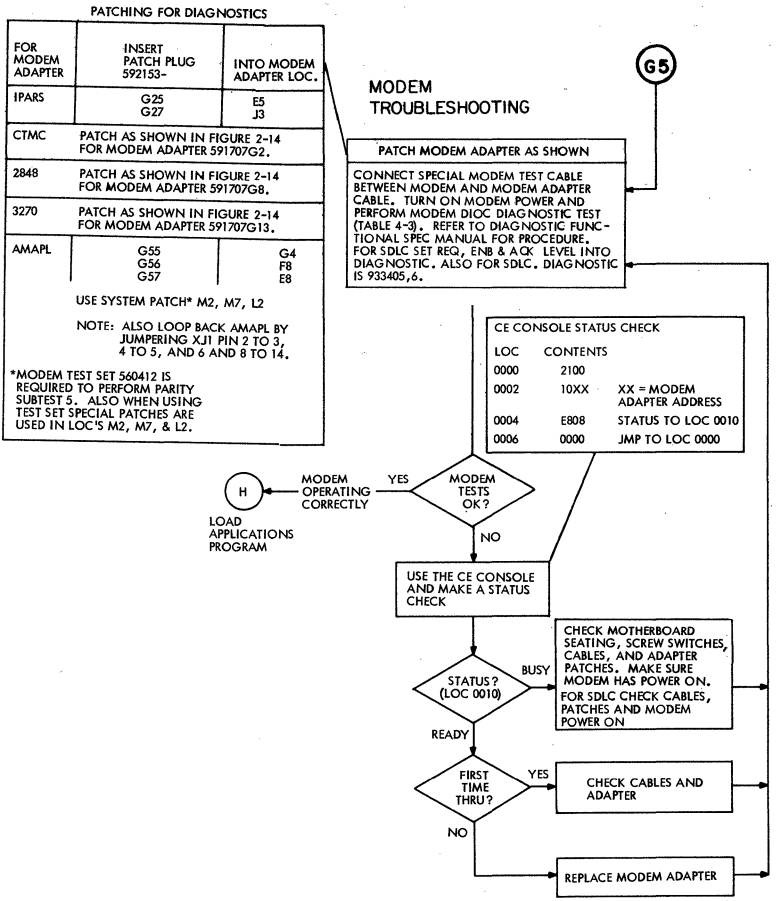


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 12 of 17)

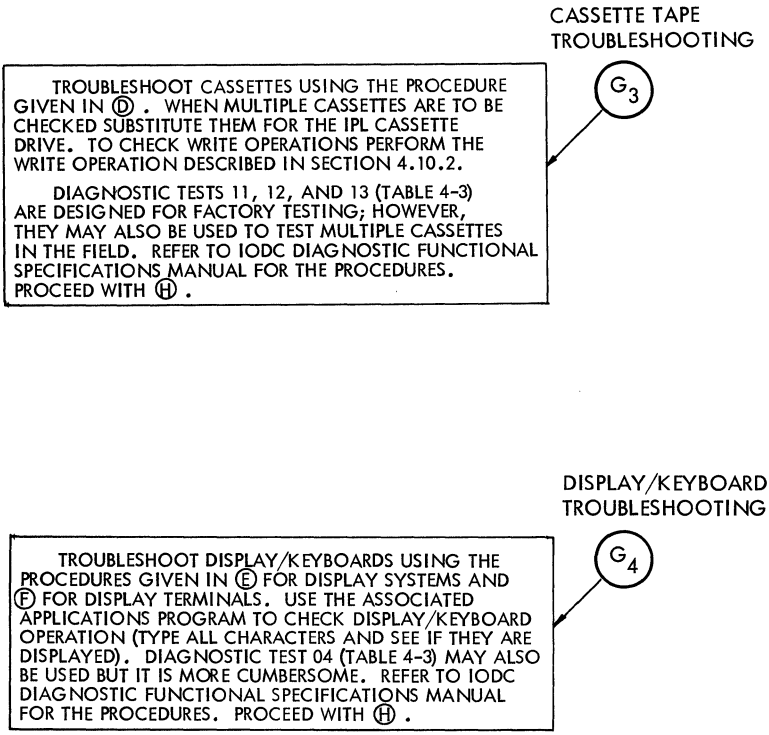


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 13 of 17)

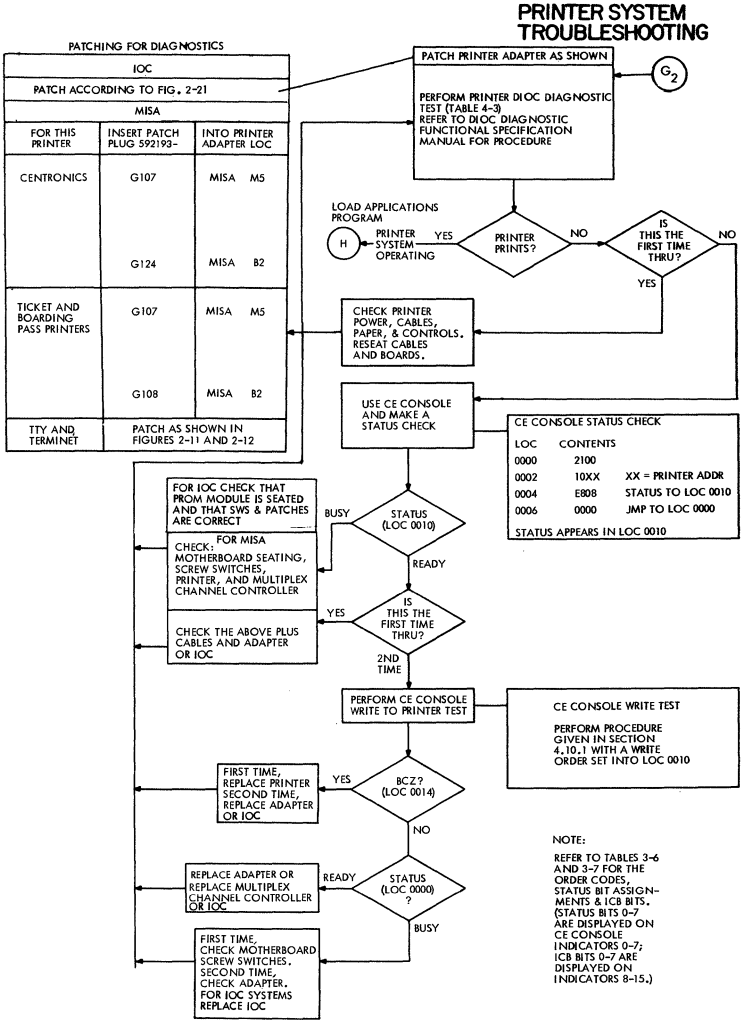


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 14 of 17)

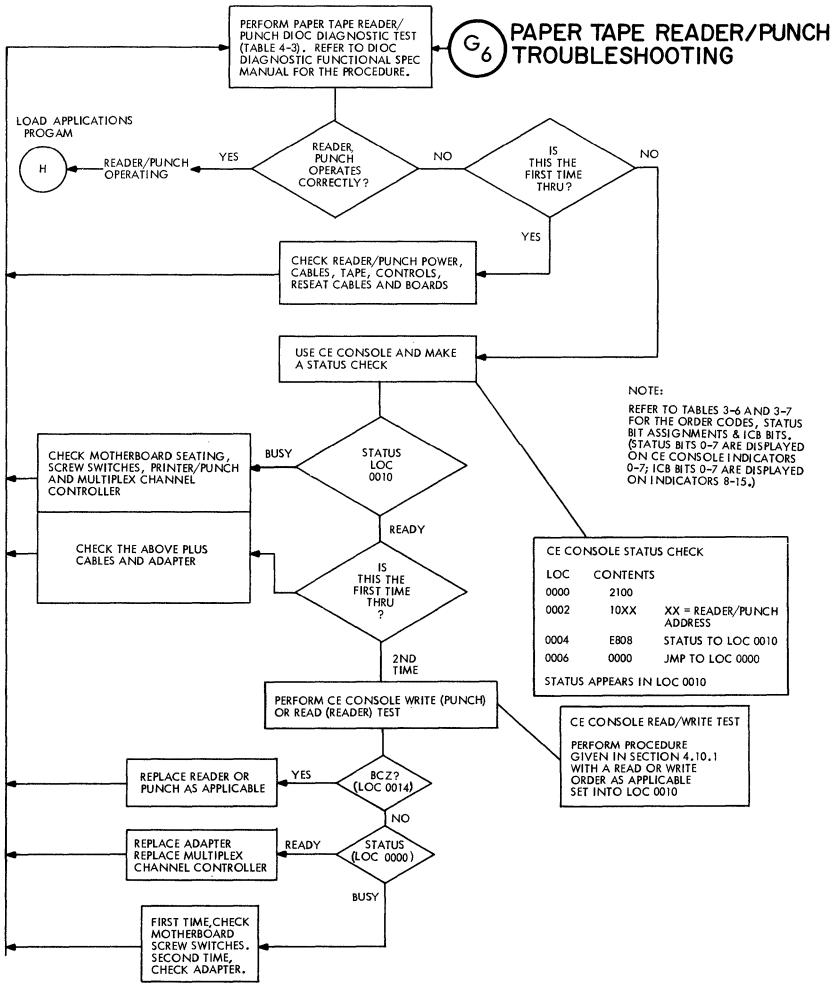


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 15 of 17)

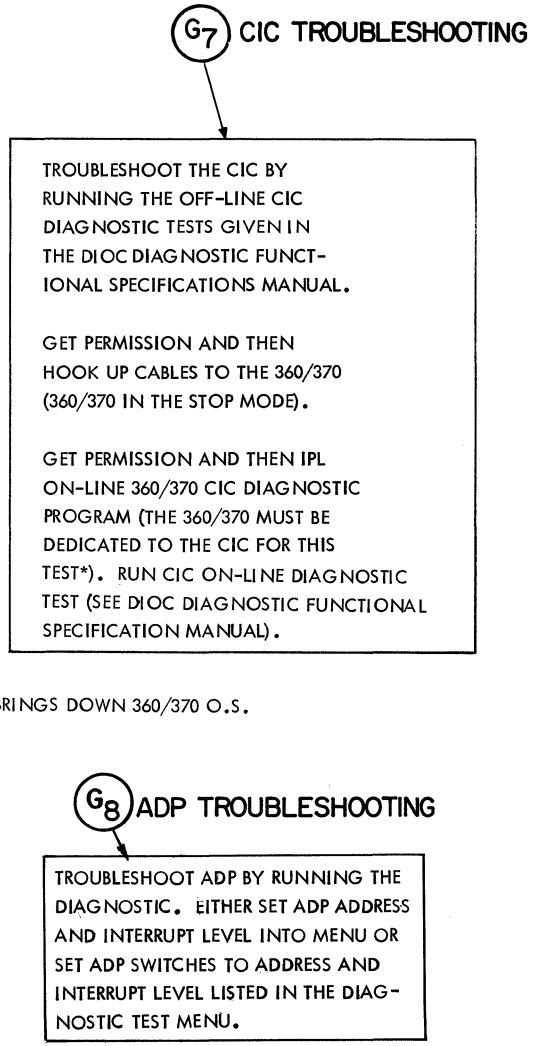


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 16 of 17)

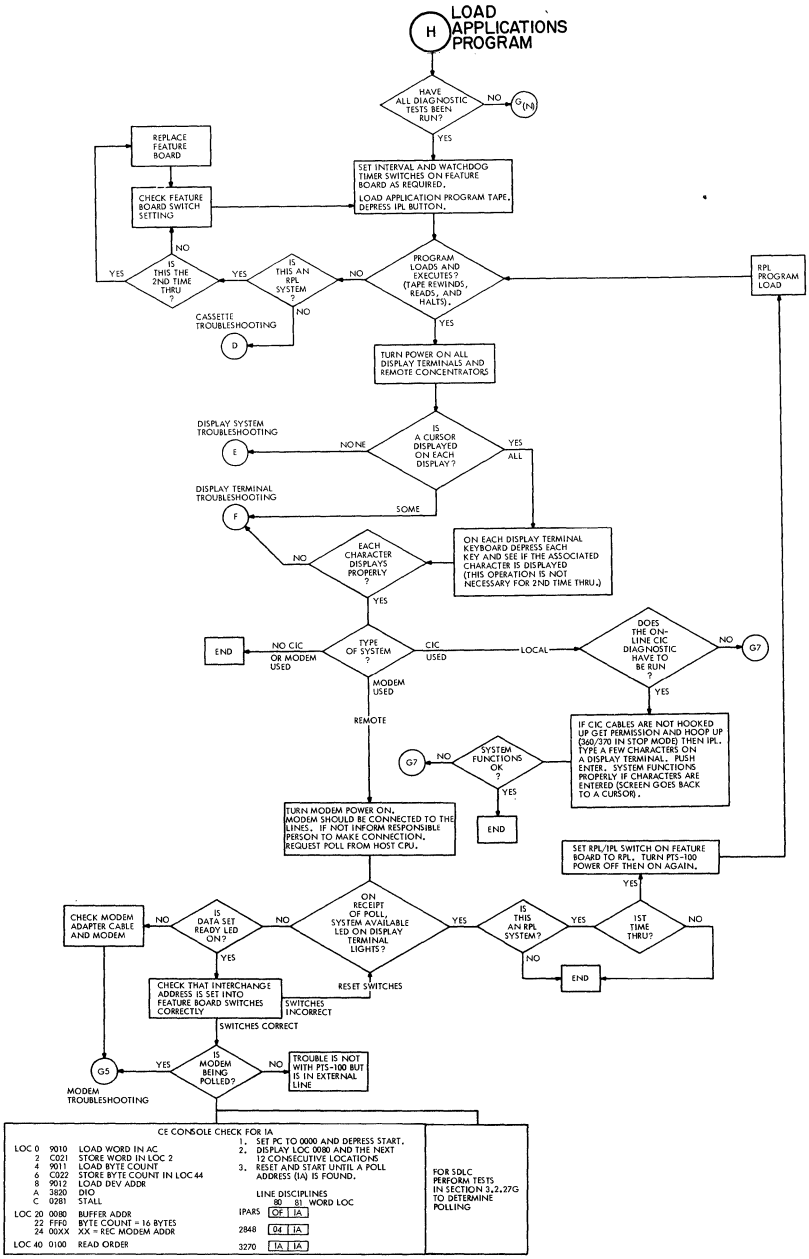


Figure 4-8. PTS-100 Troubleshooting Flow Diagram (Sheet 17 of 17)

4.11 PTS 1001/A Tests and Adjustments

4.11.1 115V/230V Conversion

1. Unplug power cord and remove wall plug end of cord and replace with applicable 230V wall plug.

2. Remove power supply board and change switch setting on power supply board from 115V to 230V. Reinstall power supply board.

3. Remove lead marked "E3 for 110V - E2 for 230V" from E3 terminal on backplane and attach to adjacent E2 terminal.

4. Remove lead marked "E4 for 110V - E2 for 220V" from E4 terminal on backplane and attach to E2 terminal.

4.11.2 Power Supply Adjustments

The power supply has been adjusted at the factory and should not require adjustment in the field.

±35V This voltage should be set to a voltage between 31.5V and 38.5V. No adjustment is required if the voltage is within the above range.

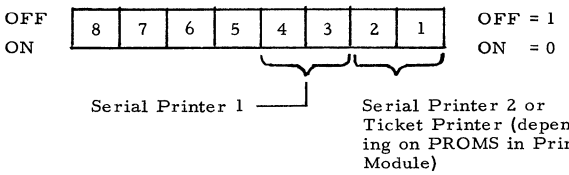
±12V This voltage should be set to a voltage between 11.6V and 12.4V. No adjustment is required if the voltage is within the above range.

+5V This voltage should be set to a voltage between 5.0V and 5.1V. No adjustment is required if the voltage is within the above range.

4.11.3 PTS 1001 Switch Settings

A toggle switch on the edge of the board selects either an underline or block type cursor. Depressing the local print key will cause all data from the top of the screen to the cursor position to be printed on serial printer 1.

Switch 2 - Printer Selection



Serial Printer - 00 = Centronics
01 = Extel

Ticket Printer - 00 = Eastern
(P2 only) 01 = Allegheny
10 = TWA

Switch 6 - Printer 1 Options

SW1 - ON = 4800 baud
SW2 - ON = 2400 baud
SW3 - ON = 1200 baud
SW4 - ON = 600 baud
SW5 - ON = 300 baud
SW6 - ON = 150 baud
SW7 - ON = 110 baud

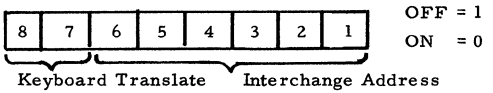
Only one of these switches may be on at any given time.

SW8 - OFF = Current loop
ON = RS-232

Switch 5 - Printer 2 Options

Same as Switch 6.

Switch 4 - IA/Keyboard Selection



IA - In Binary

Keyboard - 00 = Eastern
01 = Allegheny
10 = TWA
11 = Standard

4.11.4 PTS 1001/A Test Features

The diagnostic features incorporated into the 1001/A are controlled by using a five-position rotary switch located on the rear of the unit.

Switch Position

Run

This is the normal operation mode. Return the switch to this position when testing is complete.

Test

This mode will allow the operator to verify the correct operation of both printers, the modem logic if a loopback cable is used, and will also allow any area of 1001/A memory to be displayed on the screen. To use these tests, place the switch in the test position and:

1. Depress the CLEAR key

2. Type one of the following function codes and depress ENTER. (Type a space before the function code if American Airlines.)

   Code

   a. T1 - A void ticket will be printed on the ticket printer.

   b. T2A - Four eighty character lines of the selected character will be printed on the serial printer.

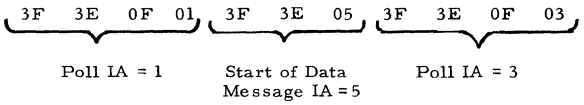
   c. T3 - Local Print - any data on the screen will be printed on the serial printer.

   d. T4 - Loopback - a modem loopback cable must be installed before performing this test! After entering T4, type any text desired and depress ENTER. The test will be transmitted and received and placed on the screen. Depress RESET to leave loopback mode.

   e. TC - EAROM configuration (1001A only) see 4.11.5 below.

Line Mon

With the switch in this position data from the telephone line is displayed on the screen in a hexadecimal format. A typical data stream follows:



Loop Test

This position is the same as 'test' except that the modem signals are automatically looped back on the backplane. Therefore, T4 may be used without a special loopback cable.

Keyboard

The normal PTS keyboard is disconnected and simulated keyboard data is continually sent to the screen.

NOTE

The 1001 will continue to respond to polls in the 'test' and 'line mon' positions. The test LED will be lighted when the test switch is in the test, line mon or loop position.

4.11.5 Procedure to Enter or Read Configuration Data Into EAROM

1. Operate test switch on rear of 1001A to test.

2. Depress CLEAR key

3. Type TC and depress ENTER (type a space before TC for American Airlines.)

4. Program replies with "KBTYPE" (A, B, C, OR D/). Type in the appropriate translate table code and depress ENTER.

   A - Eastern/Continental
   B - Allegheny/American
   C - TWA/Swissair
   D - Standard

NOTE

When entering data in the remaining steps of this procedure, preceed all single digits with a 0.

5. Program replies with IA/. Type in interchange address and depress ENTER.

6. Program replies with TA1/. Type in terminal address of CRT1 and depress ENTER.

7. Program replies with TA2/, the second time, TA3/, the third time, etc., through TA6/ the sixth time. TA1-TA4 are the terminal addresses of the displays. TA5 and TA6 are the terminal addresses of the printers. Each time the program replies with TA-/ type in the associated terminal address and depress ENTER. If no display or printer terminal is attached, type FF.

   The TA assignments are checked for duplication by the program. In case of error an INVALID TA ASSIGNMENT is displayed when operator depresses RESET and exits from the configuration mode. In which case, repeat this entire procedure.

8. Program replies with CURS TYPE/. Type 00 for an underline cursor or FF for a box cursor then depress ENTER.

9. Program replies with PRTR1 OPTION/. Type 00 for Centronics or GE Printer, or 01 for Extel printer and depress ENTER.

10. Program replies with PRTR1 TYPE/. Type 01 for serial, 02 for ticket printer, or FF for no printer. Then depress ENTER.

11. Program replies with PRTR1 BAUD RATE/. TYPE code for printer baud rate and depress ENTER.

Code	Baud Rate	Code	Baud Rate	Code	Baud Rate
00	50	06	600	0C	4800
01	75	07	1200	0D	7200
02	110	08	1800	0E	9600
03	134.5	09	2000	0F	19.2K
04	150	0A	2400		
05	300	0B	3600		

12. Program replies with PRTR1 INTERFACE/. Type 00 for RS232, or 01 for current loop and depress ENTER.

13. Program replies in the same way as in Steps 9-12 except for Printer 2.

14. Program replies with LOCAL PRTR FOR CRT1/ followed by the same thing for CRT2, 3 and 4. In each case, type 01 if the associated display is to have a local print capability to printer 1 (cabled to center connector J3), or type 02 if the display is to have a local print capability to printer 2 (cabled to the top connector J4). Depress ENTER for each entry.

15. Depress RESET to enter data into EAROM.

16. Turn off power.

17. Turn on power (EAROM is only read at initialization).

4.12 SAM Display Alignment

This section presents initial checkout, patching, cabling, and adjustment information for the SAM and Slave SAM displays. The following procedures should be performed in the order given to patch, switch, cable, and align the displays.

4.12.1 AC Input Power Patching

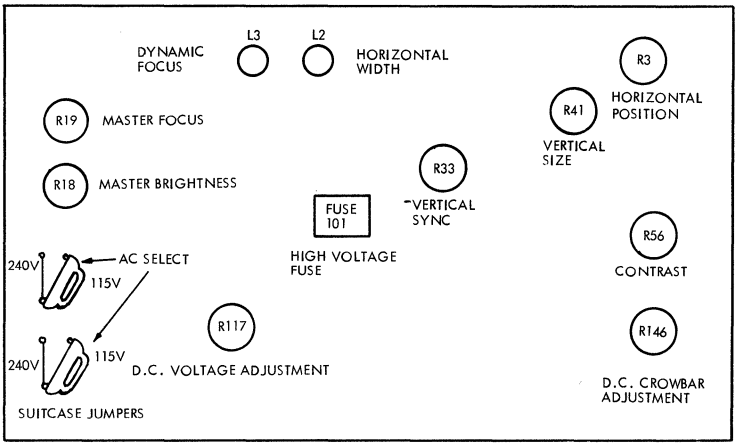
1. Refer to Figure 4-9 to locate the two suitcase jumpers on the analog board of the master SAM (and slave SAM, if used).

2. Insert the jumpers as shown in Figure 4-9A for 115 vac, 60 Hz operation.

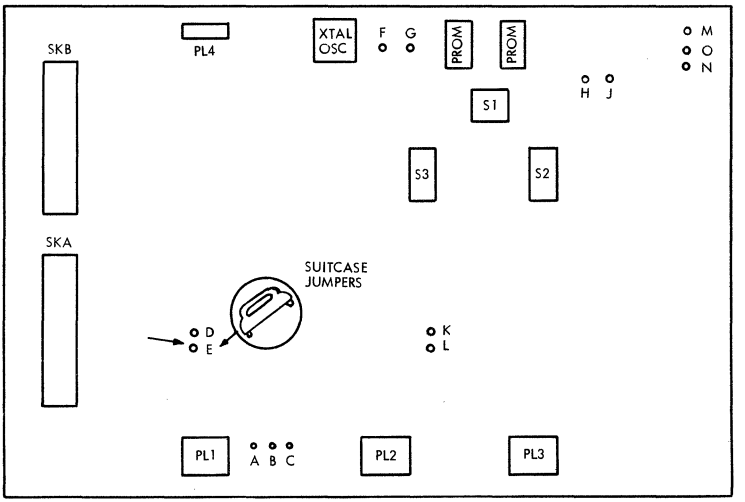
3. Locate primary power ac line fuse FS100 on the top of the SAM chassis assembly. Check that the rating of FS100 is correct for the specified ac line voltage (115 vac, 1.5 amps, P/N 503118-010 or 240 vac, 0.8 amp). Repeat step for slave SAM (if used).

4.12.2 CSA Modification Kit

Each master SAM and slave SAM display installed in Canada must be equipped with modification kit 860410G1 which removes the two thumbscrews used to secure the SAM cabinet cover to the base. These thumbscrews are replaced with two captive fillister head screws which necessitates the use of a special tool to remove the cover.



A. ANALOG BOARD



B. CONTROL LOGIC BOARD

Figure 4-9. SAM Display Boards — Control and Patch Location

4.12.3 System Configuration Patching and Switching

The master SAM mode of operation is selected by inserting or removing suitcase jumpers and by programming switches S1, S2, and S3 as shown on the control logic board layout of Figure 4-9B. Table 4-4 specifies the options selected by the suitcase jumpers, while Table 4-5 indicates the modes of operation selected by programming switches S1, S2, and S3.

The MUX logic board in the slave SAM only utilizes one programming switch (S1). The different modes of operation selected by S1 are listed in Table 4-6.

Table 4-4. Master SAM Display Jumper Patching Configuration

Jumper	Function
A, B, C	Selects full or half duplex operation in the data receiver circuit.
A to B	Half duplex (coax mode)
B to C	Full duplex (twisted pair mode)
D, E	Link in signal path from the data received to the remaining logic. Should be linked.
F, G	Link between crystal oscillator and the remaining logic. Should be linked.
H, J	Keylock option. If there is no keylock, install link.
K, L	Link in timing; normally linked.
M, N, O	Cursor register load select
M to O	1920 Screen size
N to O	960 Screen size

Table 4-5. Master SAM Programming Switch Functions

Function	Option Switches	
	On	Off
Character Generation		
Upper Case Only (7 x 7) 4K Proms 64 Char. (One Prom at Loc. IC6 Only)	S2-7 S3-2	S2-5 S3-5 S2-6 S3-6
128 Char. (7 x 7) 8K Prom (One Prom at Loc IC6 Only)	S2-7	S2-5 S3-2 S2-6 S3-5 S3-6
128 Char. (7 x 7 4K Prom at Locs. IC6 and IC7	S2-5 S2-7	S2-6 S3-5 S3-2 S3-6
Upper Case (7 x 7) and Lower Case (9 x 7) 96 Char. 4K Prom at Loc IC6 4K Prom at Loc IC7	S1-2 S3-2 S2-5 S3-5 S2-6	S2-7 S3-6
128 Char. Upper Case (7 x7) and Lower Case and Control Code (9 x 7) 4K Prom Loc. IC7 8K Prom Loc. IC6	S1-2 S3-5 S2-5 S2-6	S2-7 S3-6 S3-2
Upper and Lower Case (9 x 7) 8K Prom Loc. IC7 4K Prom Loc. IC6	S1-2 S3-6 S2-5 S2-6 S3-2	S2-7
128 Char. (9 x 7) 8K Prom at Locs IC6 and IC7	S1-2 S3-6 S2-5 S2-6	S2-7 S3-2
LED 9		
Controlled by LED Bit 0	S2-1	
Display Enable Indication		S2-1
ALARM		
Continuous	S1-1	S3-7
Momentary (set)	S3-7 S1-1	
Momentary (Set and Reset, Retrig)	S3-7	S1-1
Momentary (Set and Reset, Non Retrig)		S3-7 S1-1
TRANSMISSION MODE		
Full Duplex		S3-8
Half Duplex	S3-8	
FORMATS		
1920 Character		S3-4
960 Character	S3-4	
80 Character	S1-2	
64 Character		S1-2

Table 4-5. Master SAM Programming Switch Functions (cont)

Function	Option Switches On	Off
CURSOR		
Cursor Register Mode	S2-4	
MSB Mode	S2-3	S2-4
Block	S3-1	S2-4
Underline		S3-1
Flashing	S1-4	
Non-Flashing		S2-4 S1-4
ATTRIBUTES		
Enabled	S2-2	
Disabled		S2-2
MSB Mode	S2-2 S2-4	S2-3
Control Code Mode	S2-2 S2-3	
Normal Fields Brighter	S2-2 S3-3	
Alternative Intensity Brighter	S2-2	S3-3
Blinking Fields	S1-3 S2-2	
Blank Fields	S2-2	S1-3

Table 4-6. Slave SAM Programming Switch Functions

LED Control	Option Switches On	Off
LED 9		
Off Status Controlled by Key SW		S1-1 S1-2
On Status Controlled by Key SW	S1-1	S1-2
Controlled by LED Bit 0	S1-1 S1-2	
ALARM		
Continuous	S1-3	S1-4
Momentary (Set)	S1-3 S1-4	
Momentary (Set & Reset, Retrig)	S1-4	S1-3
Momentray (Set & Reset, Non Retrig)		S1-3 S1-4

4.12.3.1 Configuration Example for 3270 (1920, Box, MSB Cursor).

1. Install the suitcase jumpers on the control logic board as follows:

   a. A to B with Coax
      B to C Twisted Pair

   NOTE

   When using Coax, (S-3) Switch 8 must be ON.

   b. D to E

   c. F to G

   d. H to J, except when key lock option is used.

   e. K to L

   f. M to O — 1920 Screen Size

2. Program switches S1, S2, and S3 on the control logic board as follows:

SWITCH (S-1)			
1	2	3	4
ON	ON	OFF	OFF

SWITCH (S-2)							
1	2	3	4	5	6	7	8
OFF	OFF	OFF	OFF	ON	ON	OFF	OFF

SWITCH (S-3)							
1	2	3	4	5	6	7	8
ON	ON	OFF	OFF	ON	OFF	ON	OFF

4.12.3.2 Configuration Example Form 3270 (960, Box, MSB Cursor).

1. Install suitcase jumpers on the control logic board as follows:

   a. A to B with Coax
      B to C Twister Pair

   NOTE

   When using Coax, (S-3) Switch 8 must be ON.

b. D to E

c. F to G

d. H to J, except when key lock option is used.

e. K to L

f. N to O — 960 Screen Size

2. Program switches S1, S2, and S3 on the control logic board as follows:

SWITCH (S-1)			
1	2	3	4
ON	ON	OFF	OFF

SWITCH (S-2)							
1	2	3	4	5	6	7	8
OFF	OFF	OFF	OFF	ON	ON	OFF	OFF

SWITCH (S-3)							
1	2	3	4	5	6	7	8
ON	ON	OFF	ON	ON	OFF	ON	OFF

4.12.3.2 Configuration Example For IPARS (64 x 15, Box, MSB Cursor).

1. Install the suitcase jumpers on the control logic board as follows:

a. A to B with Coax
B to C Twisted

NOTE

When using Coax, (S-3) Switch 8 must be ON.

b. D to E

c. F to G

d. H to J, except when key lock option is used.

e. K to L

f. N to O — 960 Screen Size

2. Program switches S1, S2, and S3 on the control logic board as follows:

SWITCH (S-1)			
1	2	3	4
ON	OFF	OFF	OFF

SWITCH (S-2)							
1	2	3	4	5	6	7	8
OFF	OFF	OFF	OFF	ON	ON	OFF	OFF

SWITCH (S-3)							
1	2	3	4	5	6	7	8
ON	ON	OFF	ON	ON	OFF	ON	OFF

4.12.4 System Cabling

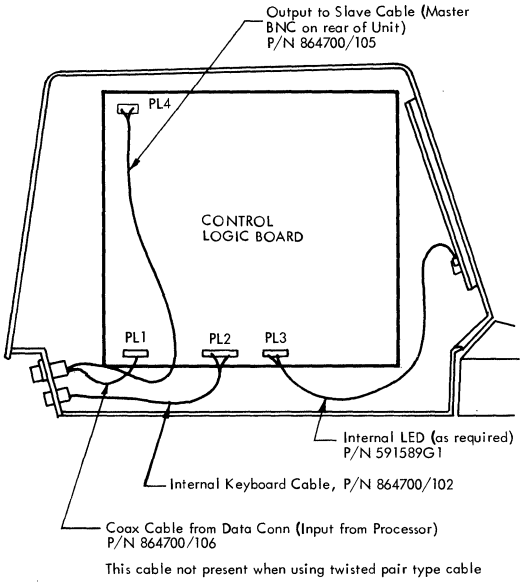
Figures 4-10 and 4-11 show all cabling used for the SAM display system. Figure 4-10 shows the internal cabling for both the master SAM and slave SAM displays. The external signal cabling between the master SAM, slave SAM, and the DA/MC/FB or DAM board in the CPU is illustrated on Figure 4-11. The general guidelines presented below should be followed when installing system cables.

1. When using twisted pair cabling, first remove caox cable plug PL1 from its connector on the master SAM control logic board (Figure 4-10, illustration A). Insert new connector PL1 from twisted pair cable. Verify correct jumper patching and programming switch settings per Table 4-4 and 4-5.

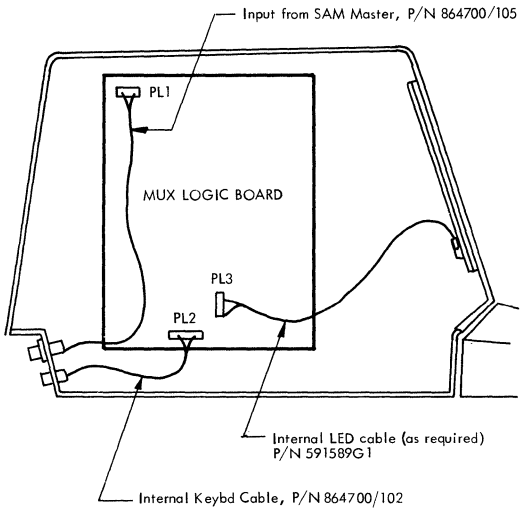
2. For installation purposes, type 860914 coax cable is fabricated in maximum lengths of 1000 feet only. If an installation requires a 1500 foot cable, the site will receive two cables. one at 1000 feet and one at 500 feet. Installation kit 930890G1 contains an adapter to attach the two cables together.

NOTE

Installation kit 930890G1 is provided as part of the coax cable accessories kit (APL860914) supplied with each 1000-foot length of coax cable.



A. MASTER SAM INTERNAL CABLING



B. SLAVE SAM INTERNAL CABLING

Figure 4-10. SAM Display Terminal Cabling

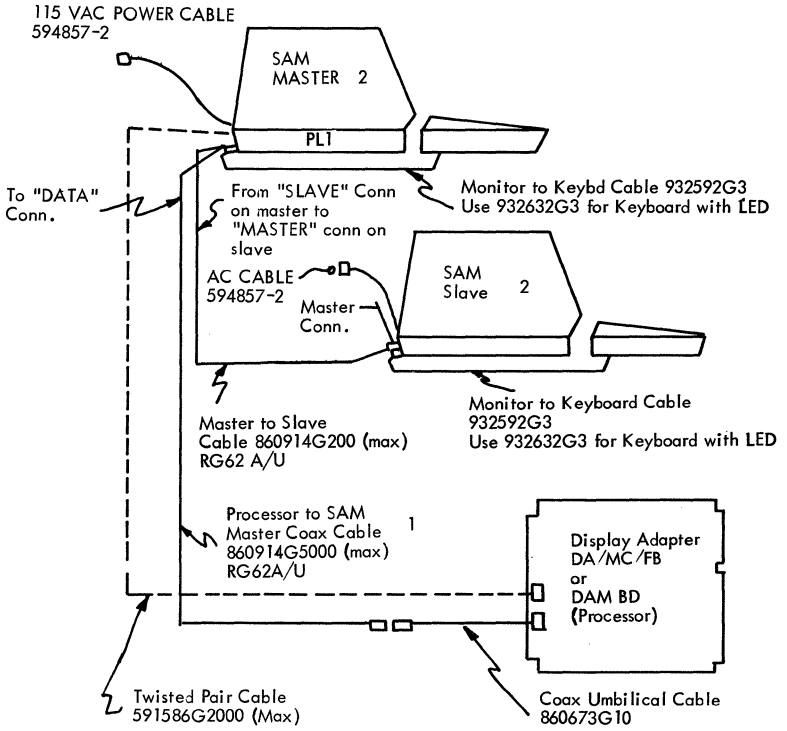


Figure 4-11. SAM Display System Cabling

4.12.5 SAM Display Adjustments

The adjustments presented in this section should only be performed as required. The majority of adjustment controls are located on the analog board (Figure 4-9, illustration A) which is identical for both the master SAM and slave SAM displays. Perform Steps 1 and 2 below before proceeding with any of the remaining procedures.

WARNING

Lethal voltage is present at the CRT anode connector, the high voltage lead, and the high voltage circuit on the analog board. Use extreme caution when performing any adjustments. Use insulated tools for all adjustments.

1. Remove the display cover, engage the interlock switch, and apply ac power to the SAM display.

2. Turn the on/off/brightness control clockwise until the raster is visible. If the raster is still not visible, adjust R18.

4.12.5.1 Raster Centering and Size Adjustment

1. Adjust vertical size control R41 until raster is 6 1/2-inches high.

2. Adjust horizontal width control L2 until raster is 9 inches wide.

3. If the edges of the raster are not horizontal, loosen the brass screw that holds the yoke coil tightening bracket. Turn the yoke coil as required, and retighten the holding screw.

4. Adjust the magnetic centering tabs on the deflection coil until the raster is centered on the screen.

5. Adjust the pin-cushion magnets on the sides of the deflection coil until the raster sides are perpendicular.

4.12.5.2 Focus Adjustment

1. Execute DIOC utility KEYDISP Subtest 3 to produce the full-screen display required for this test.

2. Adjust static focus control R19 until the dots that make up the characters in the center of the CRT display are round and sharp and show definite separation.

3. If the results in Step 2 cannot be obtained, adjust dynamic focus control L3 in addition to R19 for the desired result. Alternate between the two adjustments to optimize the CRT display.

4.12.5.3 Contrast Adjustment. Adjust R56 until the desired contrast is obtained.

4.12.5.4 Character Line Centering Adjustment. Adjust the horizontal position control R3 so that the leading edge of the first character on a line is about 1/4 inch to the right of the raster's left hand edge.

4.12.5.5 Vertical Sync

1. Turn R33 two turns fully clockwise or until sync is lost, and then counterclockwise until sync is lost again.

2. Note the position that produces a loss of sync in both directions and set the pot mid way.

CHAPTER 5. PARTS LISTS

TABLE OF CONTENTS

The part numbers for field maintenance and repair of the PTS-100 are listed in this chapter. The part numbers of the PTS-100 cable assemblies and power plugs are listed in Chapter 2 in Tables 2-2 and 2-3. Only the parts listed are considered to be replaceable within the scope of allowed field maintenance. Refer to the applicable vendor manuals for peripheral device repair parts.

5.1 Cabinets* and Cabinet Parts

Part	Part No.
1020 Cabinet	
4 ft.	594440
5 ft.	594524
1010/1015 Cabinet	592163
Remote Concentrator Cabinet	592163
Remote Concentrator Cabinet (A)	591694
Remote Concentrator Cabinet Low Profile (Swissair)	591666
Remote Concentrator Cabinet (Finnair)	592229
1020 Backplane Assembly	591567
1020 (A) Backplane Assembly	591697
1020 (B) Backplane Assembly	930309
1010/1015 Backplane Assembly	591660
1014/1015-1 Backplane Assembly	860619-1
1001 Backplane Assembly	930439
1001A Backplane Assembly	932379
1005 Backplane Assembly	860542
1008 Backplane Assembly	932302
1018 Backplane Assembly	932145
Remote Concentrator Backplane Assembly	591620
Remote Concentrator (A) Backplane Assembly	591693

*Cabinet part numbers are listed for reference only.

Part	1001/A Part No.	1005/1008 Part No.	1010/1015 Part No.	1014/1015-1/ 1018 Part No.	1020/1025/ 1030 Part No.	Remote Concentrator Part No.
Power Switch	468446-2	468446-2	594761-1	594761-1	594760-1	594860-1
IPL Switch	-	594863-4 (1005) 864105-3 (1008)	594361-1	594361-1	594361-1	-
IPL Switch Shield	-	-	594362-1	594361-2	594362-1	-
Switch Lock	864105-4	393541-001	-	-	-	-
EMI Filter FL1	594853-1	594853-1	594389-1	594389-2	594389-1	594389-1
Indicator Lamp	530297-004	530297-004	594456-4	594456-4	594456-4	594456-4
Fan	563358-1	563358-1	530461-005	530461-006 530461-004*	530461-005	530461-006
Fuse						
15A 115 volt	-	-	594461-1	594461-1	594461-1	594461-1
20A 115 volt	-	-	594461-2	594461-2	594461-2	594461-2
7A 250 volt	-	-	530438-003	530438-003	530438-003	530438-003
4A 115 volt	-	-	-	-	-	-
2A 230 volt	503118-6	-	-	-	-	-
3A 115 volt	503118-3					
Fuse Holder	-	503118-3	594462-1	594462-1	594462-1	594462-1
Test Switch S2	864178-2	-	-	-	-	-
Disc IPL SW	-	-	-	-	594710-3 (1025)	-
Power Cable	594857-5 1001	594857-5	591737G2	594982-1	930555 G10 30A 591781 G10 20A	591737 G2

5.2 Plug In Circuit Boards

Part	Part No.	Remarks
8K Memory	590162	G1: 8K with parity; G2: 8K without parity; G3: 4K with parity; G4: 4K without parity
16K Memory	593310 594866 594764	G1: 16K; G2: 12K; G3: 8K
Display Adapter (A)	591546	G0: Basic G6: Refresh
Display Adapter (C)	860629	
Display Adapter/ Monitor Controller	591695	Replaced by DAMC E591731
Display Adapter/ Monitor Controller (A) (2201)	591731	
Processor	591548	Without remote peripheral read I/O status (cannot be used with GPCA); replaced by processor A.
Asynchronous Data Processor	930383	PROM MOD 930579G1

Part	Part No.	Remarks
Feature Board A	591564	G1: Includes Watchdog Timer IPL and parity; G2: Basic
Feature Board B	860438	
Processor A	591700	With Read I/O status (can be used with GPCA); replaces 591548
Power Supply SW1000		
Power Supply SW2000	593306	
I/O Controller	860511	
Motherboard	591552	
Multiplex Channel Controller (B)	591735	Includes data overrun on chaining
Multiplex Channel Controller (A)	591550	G1: one mux only in system; G2: required when more than one mux in system
Monitor Controller (B)	591574	With vertical linearity drive. G1: upper case; G2: upper and lower case.
Monitor Controller (B) Modified	591716	Without vertical linearity. G1: upper case; G2: upper and lower case.
Monitor Controller (C)	591714	Compatible with 591705 Display Terminal only (intensified field).
Monitor Controller (B) Modified 16 Line	593732	G1: upper case G2: lower case package G3: upper case oscillator circuit G4: lower case discrete
Monitor Controller (D)	593524	Dual G1: upper case G2: upper and lower case
Monitor Controller (F)	860864 860548	PAA version Standard version
RPL Module	860044	
Coax Cable Adapter	860633	
DA/MC/FB	860468	—
Display Adapter, B	860237	G1: 480 char, 40 x 12/16K G2: 960 char, 80 x 12/16K G3: 960 char, 64 x 15/16K G4: 1920 char, 80 x 24/16K G5: 1920 char, 64 x 30/16K G7: 960 char, 40 x 24/16K
Display Adapter, C	860629	
Display Adapter/Memory	932102	
	932352	
IPARS Controller	1001	930452 Print Mod 930457
	1001A	932363 PROM Mod 932442 G1 - KLM G2 - AA G3 - STD IPARS

5.3 Adapter Circuit Boards

Part	Part No.	Remarks
Card Reader Adapter	591562	
Low Speed Serial Adapter	591558	G1: TTY G2: PRT 30 char/sec G3: PRT 120, 1200 char/sec
Parallel Adapter	860499	
Multiple Interface Serial Adapter MISA	593296	G1-G4: TermiNet Serial Printer G5-G11: TTY G11: Boarding Pass and Ticket Printers G12: Matrix Printer G13: EXTEL Printer G14: VASP/SEIMENS TTY G15: COSSOR 135 baud G16: Braathens TTY
Modem Adapter (Synchronous)	591556 (old)	G1: Model 2331 IPARS
	860820 (new)	G1: Pan Am G2: Hub polling G3: FDX std IPARS G4: Upline/downline IPARS
Modem Adapter (Synchronous)	591554	Obsolete. Replaced by 591707.
Modem Adapter	591707	G1-G6: Model 2332 CMTC G7-G12: Model 2333. 2848. G13-G14: Model 2334. 3270.
Modem Adapter	591695	Replaced by 591725
Modem Adapter B	860820	
Modem Adapter (Asynchronous)	591725	G1-G4: Model 2341 G1: Dow Jones G2: Midwest Stock Exchange G3: Full Duplex G4: Half Duplex
General Purpose Communications Adapter, GPCA	593469	Wirewrap version. Can be used only with processor 591700.
General Purpose Circuit Adapter (GPCA)	593579	PC board version replaces 593469 G1: mux ports 0-3 G2: mux ports 4-7
Cassette Adapter (A) with preamble	592512	Replaces Cassette Adapter (B) 591572. Replaced by 860566.
Cassette Adapter (B) with preamble	591572	Replaced by 592512
General Purpose Communications Adapter GPCA	930646	Replaces 593469 & 593579 G1: PORTS 0-3 G2: PORTS 4-7 G3: PORTS 3-6 G4: PORTS 3-6 (CCLCU) Autospeed sensing module 932032.

Part	Part No.	Remarks
Cassette Adapter (A) without preamble	591560	
Cassette Adapter (C)	860566	

5.4 High Speed Controller Assemblies

Part	Part No.	Remarks
Disc Drive Controller	593343	
Disc Drive Controller Mechanical Assembly	592402	
Disc Drive Controller Backplane Assembly	592419	
Disc Drive Controller Circuit Card Assembly	592399	
Disc Drive Controller Adapter Circuit Card Assembly	592397	
Fan	530461	
Connector Receptacle	561908	
Channel Interface Controller (CIC)	592421	G1: Version 1 -2260 G2: Version 2 -2260 G3: Version 2 -3270
CIC Mechanical Assembly	592401	
CIC Backplane Assembly	592528	
Driver/Receiver Circuit Card Assembly	592414	G1: Version 1 -2260 G2: Version 2 -2260/3270
Register Circuit Card Assembly	592415	G1: Version 1 -2260 G2: Version 2 -2260/3270
Capacitor, 1 μf 35v	594461	
Fan	530461	
Connector Receptacle	561908	
Magnetic Tape Controller	932289	

5.5 Display

A.4101

Part	Part No.	Remarks
Display Terminal Assembly	591705	Metal enclosure G1: with blank LED panel G2: with LED panel G3: with CRT etched face plate G4: combined G2 and G3
Display Terminal Assembly	592755	Plastic enclosure G1: with PWR ON ind G2: with LED panel G3: with PWR ON ind and bonded etched face plate G4: with LED panel and bonded etched face plate G5: with blank LED panel G6: with LED panel
CRT	594140-2	
Video Amplifier PC Board	591628G1	
Horizontal and Vertical PC Board	591703G1	
Deflection Coil	594192-1	
High Voltage Transformer	594190-5	
High Voltage Doubler	594601-1	
Switch ON/OFF	468-446-1	
Knob, Switch	594194-1	
Fuse (H&V board)	3AG 0.6 ampere 250 volt	
Capacitor(s) (.0022, .0033, .0047, .0015, .001 mfd) ±10%, 1000 volt tubular	593261G-	
Circuit Card Assembly LED	590654	
Diode, Light Emitting (LED)	594054-1	

B.4103, 4104

Control Logic Board (4103 only)	864700/200
Mux Logic Board (4104 only)	864701/200
Analog Board	864700/401
CRT	864221-1
Deflection Coil	916302/000
Interlock Switch	594200-2
Mains Fuse, 1.5A, 250V	503118-010
HV Fuse, 1A, 250V	864249-1
Knob	594594-2
Bleeder Resistor Assembly	916457/000
Upper Case PROM	594393-1
Lower Case PROM	594393-2

5.6 Keyboards

Part	Part No.	Remarks
Keyboard, 67 key, metal housing	592044	G0: without key caps G1: 2260
Keyboard, 67 key, compression molded housing	592757	G0: without key caps: G1: with numeric keys, 2260
Keyboard, 81 key, 3270	593474	G0: without key caps G1: typewriter G2: Data Entry G3: ASCII
Keyboard, 82 key, metal housing	591924	G0: basic without key caps G1: 2260 with numeric keys G2: PARS/IPARS
Keyboard, 82 key, strappable; metal housing	592389	G0: without key caps G1: 2260 with numeric keys G2: PARS/IPARS G4: PARS/IPARS with alt action shift
Keyboard, 82 key, strappable; compression molded housing	592756	G0: without key caps G1: 2260 G2: PARS/IPARS G3: PARS/IPARS with alt shift lock
Keyboard, 89/91 key, 4505	593455	G0: with LED assembly, without key caps
Keyboard, 75/87 Key	864607-1	G1: with LED assembly, and key caps (When ordering with key caps, stipulate customer).

5.7 Cassette Drive, Credit Card Reader and Customer Engineer (CE) Console (Test Set)

Part	Part No.	Remarks
CE Test Set Assembly	591398 G1 591398 G2 591398 G3 591398 G4	(Old card extender (demo)) (No cassette capability) (Test set with cassette) (Blank panel in place of cassette)
Front Panel Assembly	590061 G1	For CE Test Set 591398 G1, G2
Front Panel Assembly	590061 G2	For CE Test Set 591398 G3, G4
Toggle switch	594303-1	
Pushbutton switch	594180-4	
Rotary switch	594300-1	
Indicator lights	398503 P1	
Incandescent lamps	398504 P9	
Knob, knurled	594318	
Resistor Board Assembly	591455 G1	
Resistor, 1K 1/4W ±5%	RL075102G	

Part	Part No.	Remarks
Test panel circuit card assembly	590063G2	For CE Test Set 591398 G1, G2
Test panel circuit card assembly	593269G2	For CE Test Set 591398 G3, G4
Cassette drive	594132-2 590146 (2 head) 594968 (1 head)	
Cable assembly Cassette A	591583G20	For CE Test Set 591398 G3
Cassette circuit card assembly, adapter B	591572G1	
Card extender assembly	591400 G1	For CE Test Set 591398 G1
Card extender assembly	591988 G1	For CE Test Set 591398 G2, G3, G4
Credit Card Reader	930312	
Power Supply	864107-3	
Controller Board	930290	
Preamp Board	930306	
Reader	864125-1	
Fuse 1/2A	503118-002	

5.8 Power Supplies

Part	Part No.	Remarks
Processing Unit Power Supplies		—
without 35 volt module	594543	-1 (ACME), -6(Faratron)
and with -15 & +8.5 volts	594543	-10 (ACME)
or with no -15, +19 or +4 vdc	594543	-12 (ACME)
or same as -12 except more current	594543	-13 (ACME)
with 35 volt module	594543	-2 (ACME), -7 (Faratron)
and with -15 & 8.5 vdc	594543	-11 (ACME)
Drop in 35 volt module	594543	-3 (ACME), -8 (Faratron)
SW2000	593306G1	1005
SW2000A	593306G2	1008
SW1500	930450	1001(A)
Remote Concentrator Power Supplies		
with 2A, ± 35 volt	594438	-1 (ACME)
with 7A, ± 35 volt	594438	-3 (ACME)
Drop in 35 volt module	594438	-5 (ACME)
SW1000	591667	Low Profile

CHAPTER 6. SCHEMATIC AND WIRING DIAGRAMS

This chapter contains the following diagrams:

NOTE 1 All signals marked O.C. (Open Collector) are pulled up on back panel. See Note 10 for OCX and Note 11 for OC #.

NOTE 2 Display Adapter Signal noted with 1 and 2 suffix (REF. EN., LKOUT, DAREQ, DADOS, DAREL) are connected to associated memories as follows:

1020/30	1015	1014 1015-1
A16 suffix 2 to A17	A9 suffix 2 to A10	A9 suffix 2 to A8
A16 suffix 1 to A15	A9 suffix 1 to A8	A9 suffix 1 to A7
A19 suffix 2 to A20		
A19 suffix 1 to A18		
A22 suffix 2 to A23		
A22 suffix 1 to A21		
A25 suffix 2 to A26		
A25 suffix 1 to A24		

NOTE 3 Hard-wired memory addresses are as follows:

1020/25/30

A15 H_0	ADDR. TIED UP	A8 H_0	ADDR. TIED UP
H_0^1	ADDR. TIED UP	H_1^1	ADDR. TIED UP
H_2^1	ADDR. TIED UP	H_2^1	ADDR. TIED UP
A17 H_0	ADDR. TIED UP	A10 H_0	ADDR. TIED UP
H_0^1	ADDR. TIED UP	H_1^1	UNDER DISPLAY
H_2^1	GROUND	H_2^1	ADAPTER CONTROL
A18 H_0	ADDR. TIED UP		
H_0^1	GROUND	1014	1015-1
H_2^1	ADDR. TIED UP	A7 H_0	ADDR. TIED UP
A20 H_0	ADDR. TIED UP	H_1	ADDR. TIED UP
H_0^1	GROUND	H_2^1	ADDR. TIED UP
H_2^1	GROUND	A8 H_0^1	ADDR. TIED UP
A21 H_0	GROUND	H_1	UNDER DA CONTROL
H_0^1	ADDR. TIED UP	H_2^1	GROUND
A H_2^1	ADDR. TIED UP		
A23 H_0	GROUND		
H_0^1	ADDR. TIED UP	1005	1008
H_1^1	GROUND		
A24 H_0	GROUND	A2 H_0	ADDR. TIED UP
H_0^1	GROUND		
H_2^1	ADDR TIED UP	H_1	ADDR. TIED UP
A26 H_0	GROUND		
H_0^1	GROUND		
H_2^1	GROUND		

NOTE 4 External Watchdog lines are those generated outside the processing unit.

NOTE 5 Keyboard Data, Strobe and Clear are not connected to A5, A4, A3, A2, or A1 on Model 1020/25/30 backplane (J1-26, 29, 62).

NOTE 6 DMA Priority 1 (In) (J1-32) connects to DMA Priority 1 (Out) (J1-33) on all I/O J1 connectors. On Location A12 (1020/25/30), A5 (1015) Priority 1 (Out) (J1-33) connects to DMA Priority 2 (In) (J1-25) which then connects to DMA Priority 2 (Out) (J1-24). The Priority 2 (In) and Priority 2 (Out) are connected on each location. When a controller is inserted into a system, the appropriate Priority In and Out connection must be cut. Highest priority is given to the CE Console, followed by A1 to A12 (1020/25/30), A5 (1015) A4 (1014 & 1015-1) on Priority 1 (In) (J1-32) signal lines, then A12 (1020/25/30). A5 (1015) A4 (1014 & 1015-1) to A1 on Priority 2 (In) (J1-25) signal lines. When a controller board is removed from the cabinet the associated backplane J1-32 must be jumpered to J1-33.

NOTE 7 Program In and Out lines on the Display Adapters and DAMS are connected as follows:

1020/1030	1025
PI — A16, PO - A16, A19, A22, A25 open;	PI-A17 open;
PI — A19, A22, and A25 ground	PO-A17 to PI-A20;
	PO-A20 to PI-A23;
	PO-A23 to PI-A26.

1018

PI-A8 OPEN
PO-A8 TO PI-A9
PO-A9 TO PI-A10
PO-A10 to PI-A11.

NOTE 8 SI and SO on Display Adapters are connected as follows:

1025	1020/1030	1018
A17 SI -- open	A16 SI -- open	A8 SI -- open
A17 SO to A20 -- SI	A16 SO to A19 -- SI	A8 SO to AI -- SI
A20 SO to A23 -- SI	A19 SO to A22 -- SI	A9 SO to A10 -- SI
A23 SO to A26 -- SI	A22 SO to A25 -- SI	A10 SO to A11 -- SI
A26 SO -- open	A25 SO -- open	A11 SO -- open

NOTE 9 Signals marked OCX are open collector terminated on associated Multiplex Channel Controller.

NOTE 10 Signals marked OC# are open collector terminated on associated display adapter.

NOTE 11 On 1025 the memory select lines are connected as follows: A13-J1-62 to J1-A15, A18, A21, A24, pin 30; & A13-J2-56 to J2, A17, A20, A23, A26 pin 30.

NOTE 12 There is no J1 connection to slot A2 (1015) and A9 (1020/25/30). On connector J2 signals on pin 5, 6, 34 and 51 are only connected to the first multiplex channel controller slot. For models 1020/25/30 the I/O Adapter signals Acknowledge, Enable, Request, Status In, Mux Clk, etc., come from the associated Multiplexer.

Figure 6-1. Processing Unit Backplane Wiring (Sheet 1 of 9)

SIGNAL	CONNECTOR J1 PIN NUMBER		SIGNAL
+5V	1	2	+5V
Ext. Inter Sig 7 (O.C.)	3	4	Ext. Inter Sig 3 (O.C.)
Ext. Inter Sig 5 (O.C.)	5	6	Ext. Inter Sig 4 (O.C.)
Ext. Inter Sig 1 (O.C.)	7	8	Ext. Inter Sig 8 (O.C.)
Ext. Inter Sig 2 (O.C.)	9	10	Ext. Inter Sig 6 (O.C.)
Ground	11	12	Ground
Status In	13	14	I/O Flag Window
Address In	15	16	Data In
Reg. Start Window	17	18	Data Out Window
I/O Reset (O.C.)	19	20	Device Addr. Window
Cycle Request (O.C.)	21	22	I/O Bus Bit 3 (O.C.)
I/O Bus Bit 2 (O.C.)	23	24	Watchdog Ext. 1
	25	26	Keyboard Clear (O.C.)
Ground	27	28	Ground
Run	29	30	I/O Bus Bit 0 (O.C.)
I/O Bus Bit 1 (O.C.)	31	32	
Interval Timer	33	34	I/O Bus Bit 7 (O.C.)
I/O Bus Bit 6 (O.C.)	35	36	Watchdog Ext. 2
Processor Reset (O.C.)	37	38	Console Stop (O.C.)
Controller Stop	39	40	Run Light (EXT IPL)
I/O Bus Bit 4 (O.C.)	41	42	I/O Bus Bit 5 (O.C.)
	43	44	PL Reset
I/O Bus Bit 11 (O.C.)	45	46	I/O Bus Bit 10 (O.C.)
Ground	47	48	I/O CLK (Pos. True)
I/O Bus Bit 12 (O.C.)	49	50	I/O Function Bit 0 (O.C.)
I/O Function Bit 1 (O.C.)	51	52	I/O Bus Bit 8 (O.C.)
I/O Bus Bit 9 (O.C.)	53	54	I/O Function Bit 2 (O.C.)
I/O Function Bit 3 (O.C.)	55	56	I/O Bus Bit 15 (O.C.)
Ground	57	58	I/O Bus Bit 14 (O.C.)
I/O Flag	59	60	I/O Bus Bit 13 (O.C.)
+5V	61	62	Low Mem Sel

All lines are negative true unless noted otherwise.

*1018

PROCESSOR AND FEATURE BOARD BACKPLANE CONNECTIONS

SIGNAL	CONNECTOR J2 PIN NUMBER		SIGNAL
+5V	1	2	Data In Bit 2
Data In Bit 6	3	4	Data In Bit 3
Data In Bit P0-7 *	5	6	Data In Bit 7
Ground	7	8	Data In Bit 0
Data In Bit 1	9	10	Data In Bit 4
Data In Bit 5	11	12	Data In Bit 10
Data In Bit 11	13	14	Data In Bit 14
Data In Bit 15	15	16	Data In Bit 8
Data In Bit 9	17	18	Data In Bit 12
Data In Bit 13	19	20	Data In Bit P8-15 *
Proc. Clock	21	22	Read Cycle
Word Store Flag	23	24	Mem. Request (Pos. true)
Ground	25	26	Ground
Addr. In Bit 14	27	28	Addr. In Bit 15
Addr. In Bit 10	29	30	Addr. In Bit 11
Addr. In Bit 8	31	32	Addr In Bit 9
Addr. In Bit 12	33	34	Addr. In Bit 13
Ground	35	36	
H1 *†	37	38	
Addr. In Bit 6	39	40	Addr. In Bit 7
Addr. In Bit 2	41	42	Addr. In Bit 3
Addr. In Bit 0	43	44	Addr. In Bit 1
Addr. In Bit 4	45	46	Addr. In Bit 5
H0 *†	47	48	+5V
Ground	49	50	Ground
25 MHz Clock *†	51	52	Data Out Bit 0 (O.C.)
Data Out Bit 1 (O.C.)	53	54	Data Out Bit 2 (O.C.)
Data Out Bit 3 (O.C.)	55	56	Up Mem Sel*
+5V	57	58	IPL PB Norm Open
+5V	59	60	IPL PB Norm Closed
Ground *†	61	62	
Data Out Bit P0-7 (O.C.)*	63	64	Data Out Bit 4 (O.C.)
Data Out Bit 5 (O.C.)	65	66	Data Out Bit 6 (O.C.)
Data Out Bit 7 (O.C.)	67	68	CPU Enhancement #1
+5V	69	70	+5V
Mem. Data Out Strobe (O.C.)	71	72	Mem. Release (O.C.)
Rom Request	73	74	
Ground	75	76	CPU Enhancement #3*† (I/O Up Mem Sel)
Data Out Bit 9 (O.C.)	77	78	Data Out Bit 8 (O.C.)
Data Out Bit 11 (O.C.)	79	80	Data Out Bit 10 (O.C.)
Ground	81	82	Ground
+5V	83	84	+5V
CPU Enhancement #4	85	86	Data Out Bit P8-15 (O.C.)*
Data Out Bit 12 (O.C.)	87	88	Data Out Bit 13 (O.C.)
Data Out Bit 14 (O.C.)	89	90	Data Out Bit 15 (O.C.)
	91	92	
+28V *†	93	94	
CPU Enhancement #2	95	96	Mem. Mal. Fnct.
Ground	97	98	Ground
+5V	99	100	+5V

*Not used on 1005/1008/1018 †Not used on 1025 and 1030

Figure 6-1. Processing Unit Backplane Wiring (Sheet 2 of 9)

SIGNAL	CONNECTOR J1 PIN NUMBER		SIGNAL
Ground	1	2	Ground
+5V	3	4	+5V
+24V (VSS/VDD)	5	6	+24V (VSS/VDD)
Ref EN	7	8	+28V (VSX)
REF	9	10	B05
B06	11	12	B04
B14	13	14	B10
B11	15	16	B08
B13	17	18	B07
B12	19	20	B09
LKOUT	21	22	
DA REQ (B2)	23	24	
B03	25	26	
DADOS (OC #)	27	28	
DAREL (OC #)	29	30	Mem Sel.
Ground	31	32	Ground
+5V	33	34	+5V
	35	36	
	37	38	
	39	40	
DMDOB 00 (OC#)	41	42	DMDOB 01 (OC#)
DMDOB 02 (OC#)	43	44	DMDOB 03 (OC#)
DMDOB 07 (OC#)	45	46	DMDOB 06 (OC#)
DMDOB 05 (OC#)	47	48	DMDOB 04 (OC#)
DMDOB 09 (OC#)	49	50	DMDOB 11 (OC#)
DMDOB 08 (OC#)	51	52	DMDOB 10 (OC#)
DMDOB 12 (OC#)	53	54	DMDOB 13 (OC#)
DMBOB 14 (OC#)	55	56	DMDOB 15 (OC#)
	57	58	
	59	60	
Ground	61	62	Ground

All lines are negative true unless noted otherwise.

Note: See Display Adapter for DAM J1

MEMORY & DAM BOARD BACKPLANE CONNECTIONS

SIGNAL	CONNECTOR J2 PIN NUMBER		SIGNAL
+5V	1	2	Data In Bit 2
Data In Bit 6	3	4	Data In Bit 3
PO-7 (Unused)*	5	6	Data In Bit 7
Ground	7	8	Data In Bit 0
Data In Bit 1	9	10	Data In Bit 4
Data In Bit 5	11	12	Data In Bit 10
Data In Bit 11	13	14	Data In Bit 14
Data In Bit 15	15	16	Data In Bit 8
Data In Bit 9	17	18	Data In Bit 12
Data In Bit 13	19	20	Data In Bit P8-15 (Unused)*
	21	22	Read Cycle
Word Store Flag	23	24	Mem. Request (POS TRUE)
Ground	25	26	Ground
Addr. In Bit 14	27	28	Addr. In Bit 15
Addr. In Bit 10	29	30	Addr. In Bit 11
Addr. In Bit 8	31	32	Addr. In Bit 9
Addr. In Bit 12	33	34	Addr. In Bit 13
Ground	35	36	Mem. Clk (160 μs) (POS TRUE)
H_1	37	38	H_2 (Unused)*
Addr. In Bit 6	39	40	Addr. In Bit 7
Addr. In Bit 2	41	42	Addr. In Bit 3
Addr. In Bit 0	43	44	Addr. In Bit 1
Addr. In Bit 4	45	46	Addr. In Bit 5
H_0	47	48	
Ground	49	50	Ground
25 MHZ CLK	51	52	Data Out Bit 0 (O.C.)
Data Out Bit 1 (O.C.)	53	54	Data Out Bit 2 (O.C.)
Data Out Bit 3	55	56	
+5V	57	58	+5V
	59	60	
Ground	61	62	Ground
Data Out Bit PO-7 (O.C.)	63	64	Data Out Bit 4 (O.C.)
Data Out Bit 5	65	66	Data Out Bit 6
Data Out Bit 7	67	68	
+5	69	70	+5
Mem Data Out Strobe (O.C.)	71	72	Mem Release (O.C.)
	73	74	
Ground	75	76	
Data Out Bit 9 (O.C.)	77	78	Data Out Bit 8 (O.C.)
Data Out Bit 11	79	80	Data Out Bit 10
Ground	81	82	Ground
+5V	83	84	+5V
	85	86	Data Out Bit P8-15 (O.C.) (Mem Spd Cntl O.C.)*
Data Out Bit 12 (O.C.)	87	88	Data Out Bit 13
Data Out Bit 14	89	90	Data Out Bit 15
	91	92	Not Used
+28V (VSX) (-12V)*	93	94	+28V (VSX) (Mem Mal Fnct)* (-12V)*
+24V (VSS/VDD) (+12V)*	95	96	+24V (VSS/VDD (+12V)*
Ground	97	98	Ground
+5V	99	100	+5V

*Changes for DAM board only

Figure 6-1. Processing Unit Backplane Wiring (Sheet 3 of 9)

SIGNAL	CONNECTOR J1 PIN NUMBER		SIGNAL
† Ground	1	2	† Ground
† +5V	3	4	† +5V
† +12V	5	6	† -12V
Ref. EN 1	7	8	† Ref. EN 2 (-12V†)
REF (POS TRUE)	9	10	B05
B06	11	12	B04
B14	13	14	B10
B11	15	16	B08
B13	17	18	B07
B12	19	20	B09
LKOUT 1	21	22	LKOUT 2
DA REQ 1 (Pos. True)	23	24	DA MEM REQ 2 (Pos. True) (B02)
B03	25	26	† Keyboard Clear (O.C.)
DADOS 1 (OC #)	27	28	† DADOS 2 (OC #) (Mem Sel 2†)
DAREL 1 (OC #)	29	30	† DAREL 2 (OC #) (Mem Sel 1†)
† Ground	31	32	† Ground
† +5V	33	34	† +5V
† SI (Note 9)	35	36	† Keyboard Data (O.C.)
† SO (Note 9)	37	38	PI (Note 8)
PO (Note 8)	39	40	† 2 ms Clk (O.C.)
DMDOB 00 (OC#)	41	42	DMDOB 01 (OC#)
DMDOB 02 (OC#)	43	44	DMDOB 03 (OC#)
DMDOB 07 (OC#)	45	46	DMDOB 06 (OC#)
DMDOB 05 (OC#)	47	48	DMDOB 04 (OC#)
DMDOB 09 (OC#)	49	50	DMDOB 11 (OC#)
DMDOB 08 (OC#)	51	52	DMDOB 10 (OC#)
DMDOB 12 (OC#)	53	54	DMDOB 13 (OC#)
DMDOB 14 (OC#)	55	56	DMDOB 15 (OC#)
H1	57	58	† 64.1 μs (O.C.)
† Mem Clk (160 ns)	59	60	† Keyboard Strobe (O.C.)
† Ground	61	62	† Ground

All lines are negative true unless otherwise noted.

† Only lines used on DAM (See Memory connections for DAM J2.)

DISPLAY ADAPTER AND DAM BACKPLANE CONNECTIONS

Figure 6-1. Processing Unit Backplane Wiring (Sheet 4 of 9)

SIGNAL	CONNECTOR J1 PIN NUMBER		SIGNAL
GROUND	1	2	GROUND
+5V	3	4	+5V
+12V	5	6	-12V
REF. EN 1	7	8	REF. EN 2
REF (POS TRUE)	9	10	B05
B06	11	12	B04
B14	13	14	B10
B11	15	16	B08
B13	17	18	B07
B12	19	20	B09
LKOUT 1	21	22	LKOUT 2
DA REQ 1 (POS. TRUE)	23	24	DA MEM REQ 2 (POS. TRUE)
B03	25	26	KEYBOARD CLEAR (O.C.)
DADOS 1 (OC)	27	28	DADOS 2 (OC)
DAREL 1 (OC)	29	30	DAREL 2 (OC)
GROUND	31	32	GROUND
+5V	33	34	+5V
	35	36	KEYBOARD DATA (O.C.)
	37	38	
	39	40	2 MS CLK (O.C.)
DMDOB 00 (OC)	41	42	DMDOB 01 (OC)
DMDOB 02 (OC)	43	44	DMDOB 03 (OC)
DMDOB 07 (OC)	45	46	DMDOB 06 (OC)
DMDOB 05 (OC)	47	48	DMDOB 04 (OC)
DMDOB 09 (OC)	49	50	DMDOB 11 (OC)
DMDOB 08 (OC)	51	52	DMDOB 10 (OC)
DMDOB 12 (OC)	53	54	DMDOB 13 (OC)
DMDOB 14 (OC)	55	56	DMDOB 15 (OC)
H1 (UPPER MEM ONLY)	57	58	64.1 µS (OC)
MEM CLK (160 NS)	59	60	KEYBOARD STROBE (OC)
GROUND	61	62	GROUND

ALL LINES ARE NEGATIVE TRUE UNLESS OTHERWISE NOTED

MODELS 1014 & 1005 DA/MC/FB BACKPLANE CONNECTIONS

SIGNAL	CONNECTOR J2 PIN NUMBER		SIGNAL
+5V	1	2	I/O BUS BIT 11
	3	4	I/O BUS BIT 10
	5	6	I/O BUS BIT 9
GROUND	7	8	I/O BUS BIT 8
PL RESET	9	10	I/O BUS BIT 4
I/O BUS BIT 5	11	12	I/O BUS BIT 7
PWR STATUS 1	13	14	I/O BUS BIT 0
PWR STATUS 2	15	16	I/O BUS BIT 1
	17	18	I/O RESET
	19	20	
+35V	21	22	PROC. RESET
I/O BUS BIT 6	23	24	I/O BUS BIT 12
GROUND	25	26	GROUND
ADDR IN BIT 14	27	28	STATUS IN
ADDR IN BIT 10	29	30	ADDR IN BIT 11
ADDR IN BIT 8	31	32	ADDR IN BIT 9
ADDR IN BIT 12	33	34	ADDR IN BIT 13
GROUND	35	36	I/O BUS BIT 15
I/O BUS BIT 14	37	38	I/O BUS BIT 13
ADDR IN BIT 6	39	40	ADDR IN BIT 7
	41	42	
	43	44	INTERVAL TIMER
	45	46	ADDR IN BIT 5
	47	48	-35V
GROUND	49	50	GROUND
25 MHZ	51	52	DATA OUT BIT 0 (O.C.)
DATA OUT BIT 1 (O.C.)	53	54	DATA OUT BIT 2 (O.C.)
DATA OUT BIT 3 (O.C.)	55	56	
+5V	57	58	+5V
+35V	59	60	+35V
GROUND	61	62	GROUND
	63	64	DATA OUT BIT 4 (O.C.)
DATA OUT BIT 5 (O.C.)	65	66	DATA OUT BIT 6 (O.C.)
DATA OUT BIT 7 (O.C.)	67	68	IPL PB (NO)
+5V	69	70	+5V
DATA OUT WINDOW (DOW)	71	72	
ROM REQ	73	74	IPL PB (NC)
GROUND	75	76	-35V
DATA OUT BIT 9 (O.C.)	77	78	DATA OUT BIT 8 (O.C.)
DATA OUT BIT 11 (O.C.)	79	80	DATA OUT BIT 10 (O.C.)
GROUND	81	82	GROUND
+5V	83	84	+5V
+35V	85	86	I/O CLOCK
DATA OUT BIT 12 (O.C.)	87	88	DATA OUT BIT 13 (O.C.)
DATA OUT BIT 14 (O.C.)	89	90	DATA OUT BIT 15 (O.C.)
-35V	91	92	-35V
	93	94	
PS SYNC	95	96	DEVICE ADDR WINDOW (DAW)
GROUND	97	98	GROUND
+5V	99	100	+5V

Figure 6-1. Processing Unit Backplane Wiring (Sheet 5 of 9)

SIGNAL	CONNECTOR J2 PIN NUMBER		SIGNAL
+5V	1	2	+5V
+5V	3	4	+5V
* VSS	5	6	* VSS
* VSX	7	8	* VSX
GND	9	10	GND
GND	11	12	GND
+12V	13	14	+12V
-12V	15	16	-12V
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
GND	27	28	GND
	29	30	
GND	31	32	GND
+5V	33	34	+5V
	35	36	
+35V	37	38	+35V
-35V	39	40	-35V
+5V	41	42	+5V
+5V	43	44	+5V
	45	46	
GND	47	48	GND
	49	50	
	51	52	
	53	54	
	55	56	
GND	57	58	GND
GND	59	60	GND
+5V	61	62	+5V

MODELS 1005, 1008 & 1014 POWER SUPPLY SW2000 BACKPLANE CONNECTIONS

*NOT ON 1008

SIGNAL	CONNECTOR J2 PIN NUMBER		SIGNAL
+5V	1	2	+5V
GND	3	4	GND
	5	6	
+35V	7	8	+35V
	9	10	
+5V	11	12	+5V
	13	14	
AC IN (W)	15	16	AC IN (W)
	17	18	
AC IN (B)	19	20	AC IN (B)
	21	22	
	23	24	
GND	25	26	GND
	27	28	
+12	29	30	+12V
-35	31	32	-35V
GND	33	34	GND
GND	35	36	GND
	37	38	
-12	39	40	-12V
	41	42	
	43	44	
	45	46	
+5V	47	48	+5V
GND	49	50	GND
	51	52	
GND	53	54	GND
	55	56	
+5V	57	58	+5V
+5V	59	60	+5V
GND	61	62	GND
PS SYNC	63	64	
	65	66	
GND	67	68	GND
+5V	69	70	+5V
	71	72	
	73	74	
GND	75	76	GND
+35V	77	78	+35V
	79	80	
GND	81	82	GND
+5V	83	84	+5V
GND	85	86	GND
	87	88	
	89	90	
(4V) VSX	91	92	VSX
(20V) VSS/VDD	93	94	VSS/VDD
-35V	95	96	-35V
GND	97	98	GND
+5V	99	100	+5V

Figure 6-1. Processing Unit Backplane Wiring (Sheet 6 of 9)

SIGNAL	CONNECTOR J2 PIN NUMBER		SIGNAL
+5V	1	2	+5V
GND	3	4	GND
	5	6	
+35V	7	8	
	9	10	
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
	27	28	
+12V	29	30	+12V
-35V	31	32	
GND	33	34	
	35	36	
	37	38	
-12V	39	40	-12V
	41	42	
	43	44	
	45	46	
	47	48	
	49	50	
	51	52	
GND	53	54	GND
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
GND	67	68	
	69	70	
	71	72	
	73	74	
	75	76	
+35V	77	78	
	79	80	
	81	82	
	83	84	
GND	85	86	
	87	88	
	89	90	
	91	92	
	93	94	
-35V	95	96	
GND	97	98	GND
+5V	99	100	+5V

MONITOR CONTROLLER BACKPLANE CONNECTIONS

Figure 6-1. Processing Unit Backplane Wiring
(Sheet 7 of 9)

SIGNAL	CONNECTOR J1 PIN NUMBER		SIGNAL
+5V	1	2	+5V
Ext. Inter Sig 7 (O.C.)	3	4	Ext. Inter Sig 3 (O.C.)
Ext. Inter Sig 5 (O.C.)	5	6	Ext. Inter Sig 4 (O.C.)
Ext. Inter Sig 1 (O.C.)	7	8	Ext. Inter Sig 8 (O.C.)
Ext. Inter Sig 2 (O.C.)	9	10	Ext. Inter Sig 6 (O.C.)
Ground	11	12	Ground
Status In	13	14	I/O Flag Window
Address In	15	16	Data In
Req. Start Window	17	18	Data Out Window
I/O Reset (O.C.)	19	20	Device Addr. Window
Cycle Request (O.C.)	21	22	I/O Bus Bit 3 (O.C.)
I/O Bus Bit 2 (O.C.)	23	24	† DMA Priority 2 (OUT) (Note 7)
† DMA Priority 2 (IN) (Note 7)	25	26	Keyboard Clear (O.C.) (Note 5)
Ground	27	28	Ground
Keyboard Data (O.C.) (Note 5)	29	30	I/O Bus Bit 0 (O.C.)
I/O Bus Bit 1 (O.C.)	31	32	DMA Priority 1 (In) (Note 7)
DMA Priority 1 (Out) (Note 7)	33	34	I/O Bus Bit 7 (O.C.)
I/O Bus Bit 6 (O.C.)	35	36	CE Priority (Out)
Processor Reset (O.C.)	37	38	Console Stop (OC)
Controller Stop	39	40	2 ms Clk (O.C.)
I/O Bus Bit 4 (O.C.)	41	42	I/O Bus Bit 5 (O.C.)
† CE Priority (In)	43	44	PL Reset
I/O Bus Bit 11 (O.C.)	45	46	I/O Bus Bit 10 (O.C.)
Ground	47	48	I/O Clk In (160 ns) (Pos. True)
I/O Bus Bit 12 (O.C.)	49	50	I/O Function Bit 0 (O.C.)
I/O Function Bit 1 (O.C)	51	52	I/O Bus Bit 8 (O.C.)
I/O Bus Bit 9 (O.C.)	53	54	I/O Function Bit 2 (O.C.)
I/O Function Bit 3 (O.C.)	55	56	I/O Bus Bit 15 (O.C.)
Ground	57	58	I/O Bus Bit 14 (O.C.)
I/O Flag	59	60	I/O Bus Bit 13 (O.C.)
+5V	61	62	Keyboard Strobe (O.C.) (Note 5)

All lines are negative true unless noted otherwise.

† Not On 1008

MULTIPLEX CHANNEL CONTROLLER, I/O CONTROLLER AND MOTHERBOARD BACKPLANE CONNECTIONS

**1018/1025/1030

†Only signals used on 1005 & 1008 also on 1005 CPU Enhancement #3 is used and Pin 86 is unused.

††Used on 1005 only.

SIGNAL	CONNECTOR J2 PIN NUMBER		SIGNAL
† +5V	1	2	† +5V
† Ground	3	4	† Ground
† Proc. Clk	5	6	† Mem. Clk (160 ns)
†† +35V	7	8	† I/O Clk (160 ns) (Pos. true)
Enable 0	9	10	Enable 1
Enable 2	11	12	Enable 3
Enable 4	13	14	Enable 5
Enable 6	15	16	Acknowledge 0
Acknowledge 6	17	18	Acknowledge 5
Acknowledge 4	19	20	Acknowledge 3
Acknowledge 2	21	22	Acknowledge 1
Enable 7	23	24	Acknowledge 7
Adapter Data Bus 4 (OCX)	25	26	Adapter Data Bus 5 (OCX)
Adapter Data Bus 6 (OCX)	27	28	Adapter Data Bus 7 (OCX)
† +12V	29	30	†+12V
†† -35V	31	32	TP(J11-7)*
† Ground	33	34	† Mem Clk (160 ns) (Pos. true)
Request 1	35	36	Request 0
Request 3	37	38	Request 2
† -12V	39	40	† -12V
	41	42	TP(J11-9)*
Search Char. Found	43	44	Status In
TP(J11-14)*	45	46	ICB REQUEST(OCX)
Request 4	47	48	Request 5
Request 7	49	50	Request 6
† 25 MHz Clk	51	52	Addr. 14
† Ground	53	54	† GND
TP(B3-4)*	55	56	TP(J8-1)*
Adapter Data Bus 1 (OCX)	57	58	Adapter Data Bus 0 (OCX)
TP(D9-10)*	59	60	TP(F12-7)*
Adapter Data Bus 2 (OCX)	61	62	Adapter Data Bus 3 (OCX)
	63	64	TP(C10-6)*
TP(J8-4)*	65	66	Addr. 15
† Ground	67	68	† CPU Enhancement #1
System Reset	69	70	† 2 MS CLK (O.C.)
	71	72	† Keyboard Clear (O.C.)
	73	74	
CPU Enhancement #3	75	76	† 64.1 μs Clk (O.C.)
†(I/O Up Mem Sel)**	77	78	TP(F11-5)*
	79	80	Inh. Trans. On This Byte (OCX)
TP(E15-2)*	81	82	TP(F16-5)*
	83	84	Data Request (OC*)
† Ground	85	86	† Mem Speed Cntl*
TP(F13-3)*	87	88	
† CPU Enhancement #4	89	90	Order Out
Request Reset	91	92	Mux Clk
Stop Reset	93	94	Byte Count Zero
†† -35V	95	96	† CPU Enhancement #2
† Ground	97	98	† Ground
† +5V	99	100	† +5V

Refer to NOTE 12

*1018 Only (TP(XX-X) only on Mux).

Figure 6-1. Processing Unit Backplane Wiring (Sheet 8 of 9)

SIGNAL	CONNECTOR J1 PIN NUMBER		SIGNAL
+5V	1	2	+5V
	3	4	KB CLK
V SYNC DRIVE	5	6	
VIDEO	7	8	
	9	10	
GND	11	12	GND
H SYNC DRIVE	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
GND	27	28	GND
KB TEST	29	30	
	31	32	
+5V	33	34	+5V
	35	36	KB LOAD
	37	38	
	39	40	
	41	42	
	43	44	
	45	46	KB DATA
GND	47	48	GND
	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
KEYLOCK GND	59	60	KEYLOCK
+5V	61	62	+5V

1001/A

SIGNAL	CONNECTOR J1 PIN NUMBER		SIGNAL
+5V	1	2	+5V
GND	3	4	GND
	5	6	
+35V	7	8	+35V
	9	10	
+5V	11	12	+5V
	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
	27	28	
+12V	29	30	+12V
-35V	31	32	-35V
GND	33	34	GND
	35	36	
	37	38	
-12V	39	40	-12V
MAGCCRL	41	42	ABAL
TEST MODE	43	44	LINE MONITOR
	45	46	
+5V	47	48	+5V
LED 5	49	50	LED 6
LED 7	51	52	LED 4
GND	53	54	GND
	55	56	
LED 3	57	58	LED 2
LED 0	59	60	LED 1
RD	61	62	CD
SCR	63	64	DSR
RI	65	66	SQ
GND	67	68	GND
+5V	69	70	+5V
SCT	71	72	CTS
DTRL	73	74	DTR 2
DATA/STATUS 1	75	76	DATA/STATUS 2
+35V	77	78	+35V
DATA/STATUS 1 RET	79	80	DATA/STATUS 2 RET
DEMAND IN 1	81	82	DEMAND IN 2
+5V	83	84	+5V
GND	85	86	GND
RD1	87	88	RD2
DSR/CD1	89	90	DSR/CD2
SD	91	92	RTS
TEST CLK	93	94	DTR
-35V	95	96	-35V
GND	97	98	GND
+5V	99	100	+5V

1001/A

Figure 6-1. Processing Unit Backplane Wiring (Sheet 9 of 9)

SIGNAL	CONNECTOR P1 PIN NUMBER	SIGNAL	CONNECTOR P2 PIN NUMBER
DATA REQUEST	1	GROUND	1
+5V	2	GROUND	2
KEYBOARD CLEAR (67 MS)	3	-12V	3
GROUND	4	GROUND	4
REQUEST*	5		5
GROUND	6	ADDRESS 14	6
GROUND	7	ADAPTER DATA BUS 1	7
GROUND	8	SEARCH CHARACTER FOUND	8
ACKNOWLEDGE**	9	ADAPTER DATA BUS 4	9
ACKNOWLEDGE*	10	ADAPTER DATA BUS 5	10
STOP RESET	11	ADAPTER DATA BUS 2	11
64.1 μS CLK	12	GROUND	12
SYSTEM RESET	13	+12V	13
BYTE COUNT ZERO	14	ADAPTER DATA BUS 0	14
ICB REQUEST	15	ADAPTER DATA BUS 7	15
MUX CLK	16	ADAPTER DATA BUS 6	16
REQUEST**	17	ADDRESS 15	17
STATUS IN	18	2 MS CLK	18
REQUEST RESET	19	ADAPTER DATA BUS 3	19
+5V	20	INH TRANS ON THIS BYTE	20
ORDER OUT	21		21
ENABLE**	22	+5V	22
ENABLE*	23	+5V	23
+5V	24	+5V	24

Figure 6-2. Motherboard Adapter Interface, Wiring

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+5V	34		67	GROUND
2	+5V	35		68	
3	GROUND	36		69	
4	GROUND	37		70	
5		38		71	
6		39	-12V	72	
7	+35V	40	-12V	73	
8		41		74	
9		42		75	
10		43		76	
11		44		77	+35V
12		45		78	
13		46		79	
14		47		80	
15		48		81	
16		49		82	
17		50		83	
18		51		84	
19		52		85	GROUND
20		53	GROUND	86	
21		54	GROUND	87	
22		55		88	
23		56		89	
24		57		90	
25		58		91	
26		59		92	
27		60		93	
28		61		94	
29	+12V	62		95	-35V
30	+12V	63		96	
31	-35V	64		97	GROUND
32		65		98	GROUND
33	GROUND	66		99	+5V
				100	+5V

NOTE

ALL PINS IN ALL BOARD SLOTS
ARE BUSED TOGETHER.

Figure 6-3. Remote Concentrator Backplane Wiring

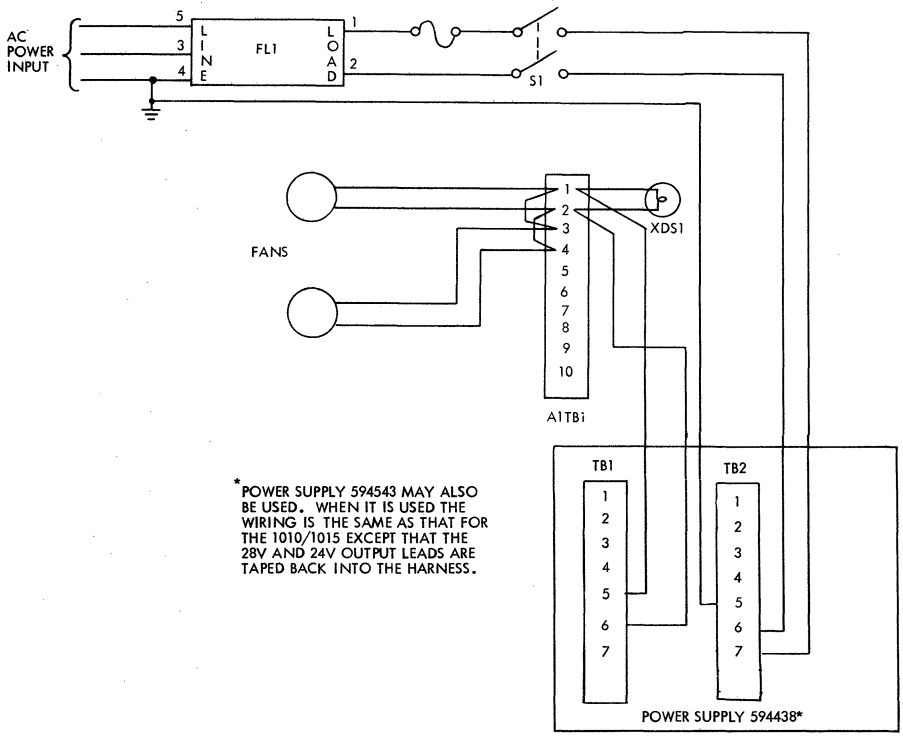


Figure 6-4. Remote Concentrator Cabinet AC Wiring Diagram

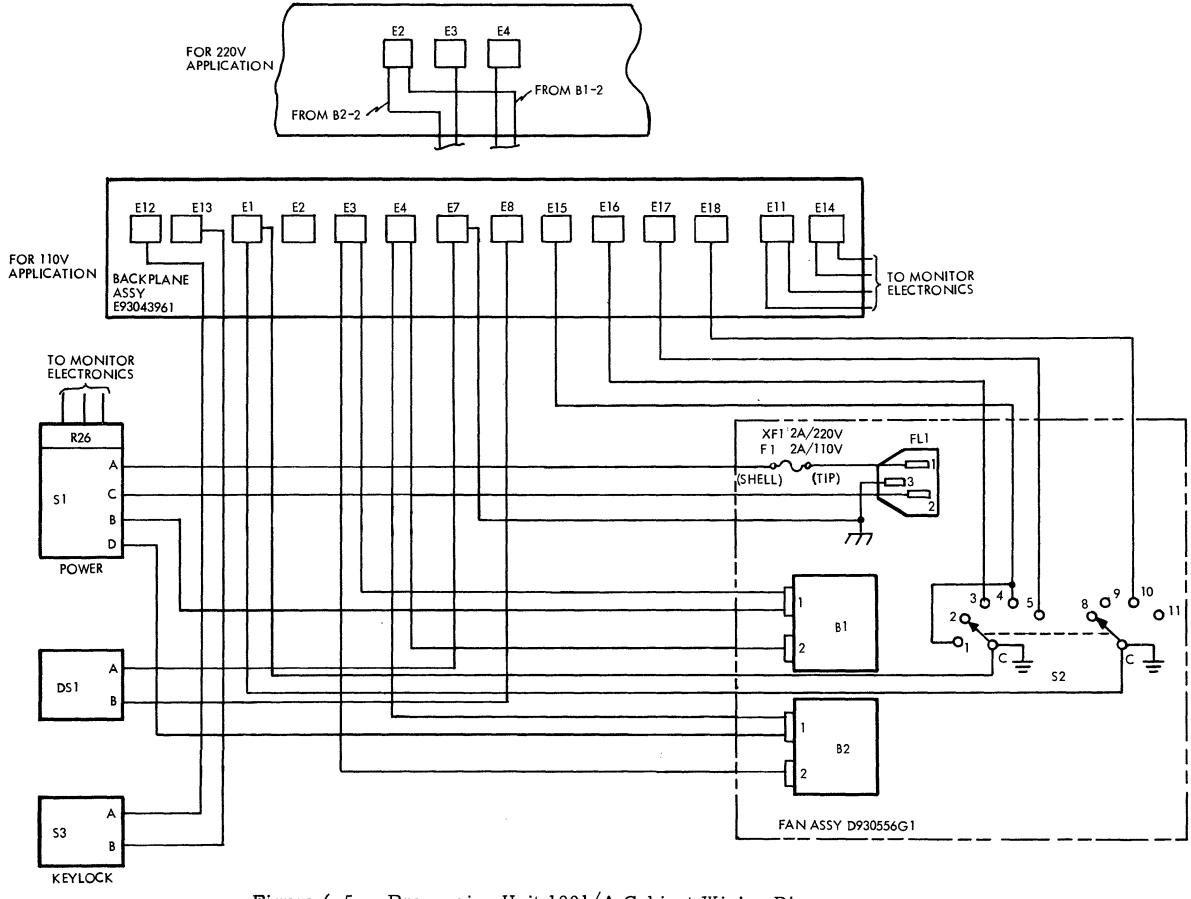


Figure 6-5. Processing Unit 1001/A Cabinet Wiring Diagram

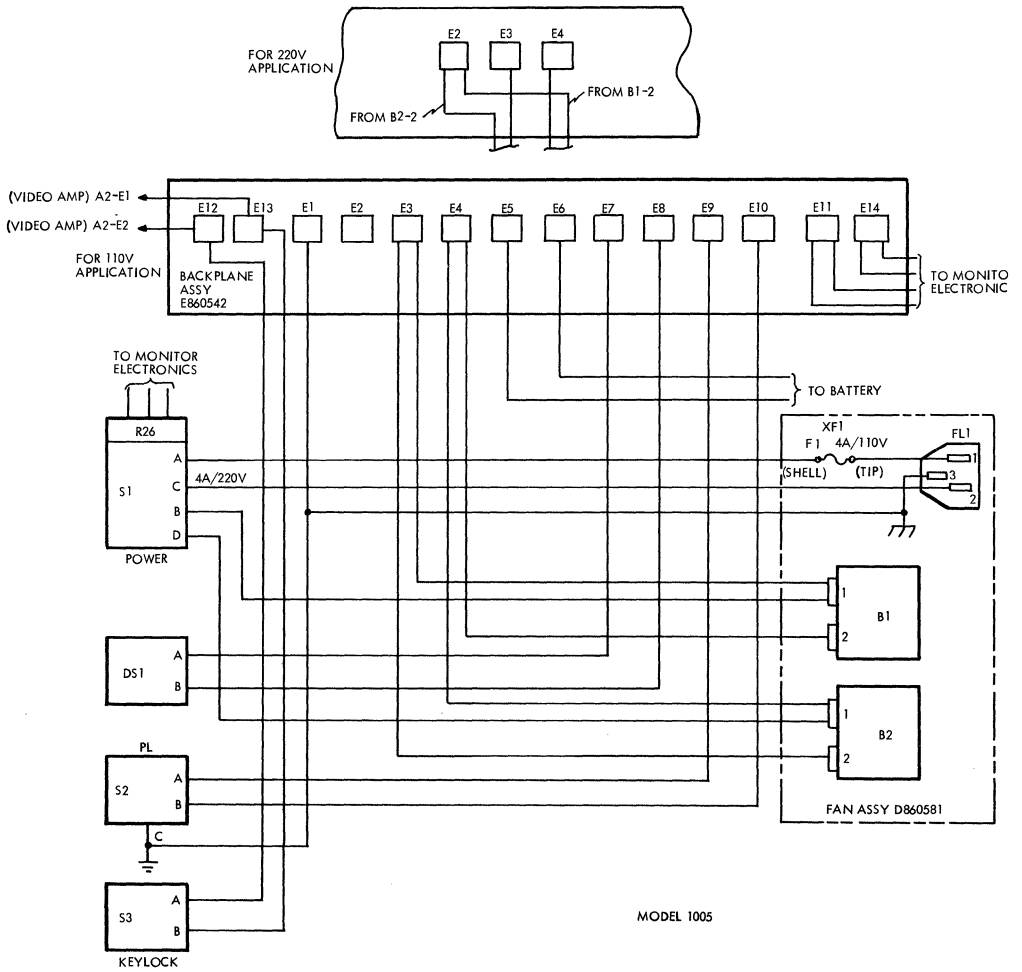


Figure 6-6. Processing Unit Model 1005 Cabinet Wiring Diagram

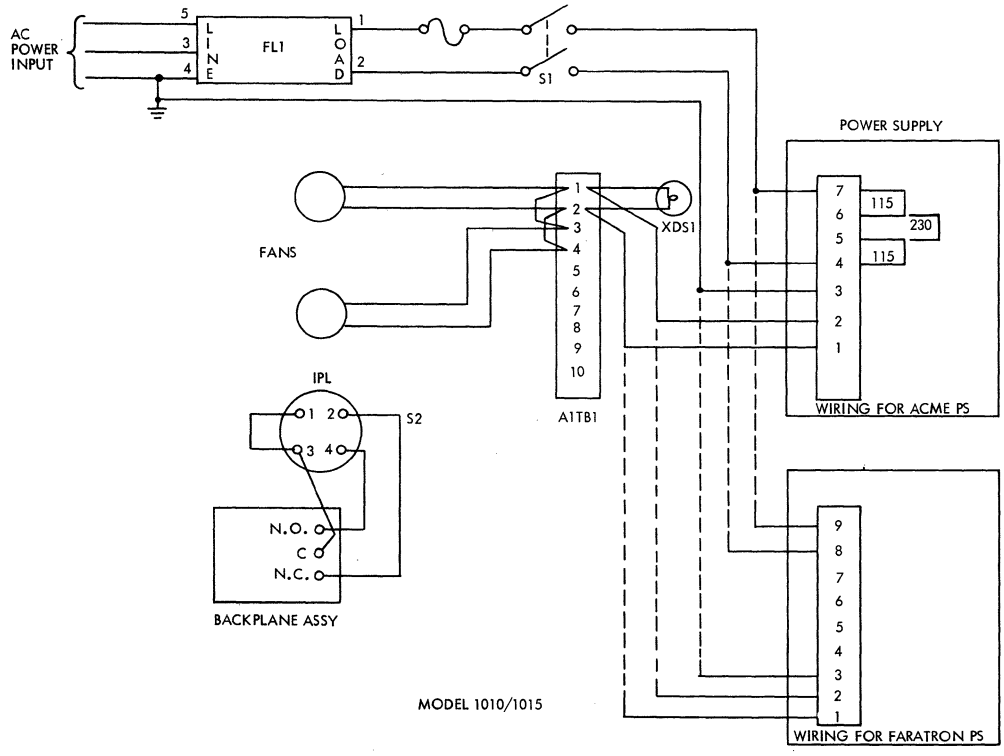


Figure 6-7. Processing Unit Model 1010/1015 Cabinet Wiring Diagram (Sheet 1 of 2)

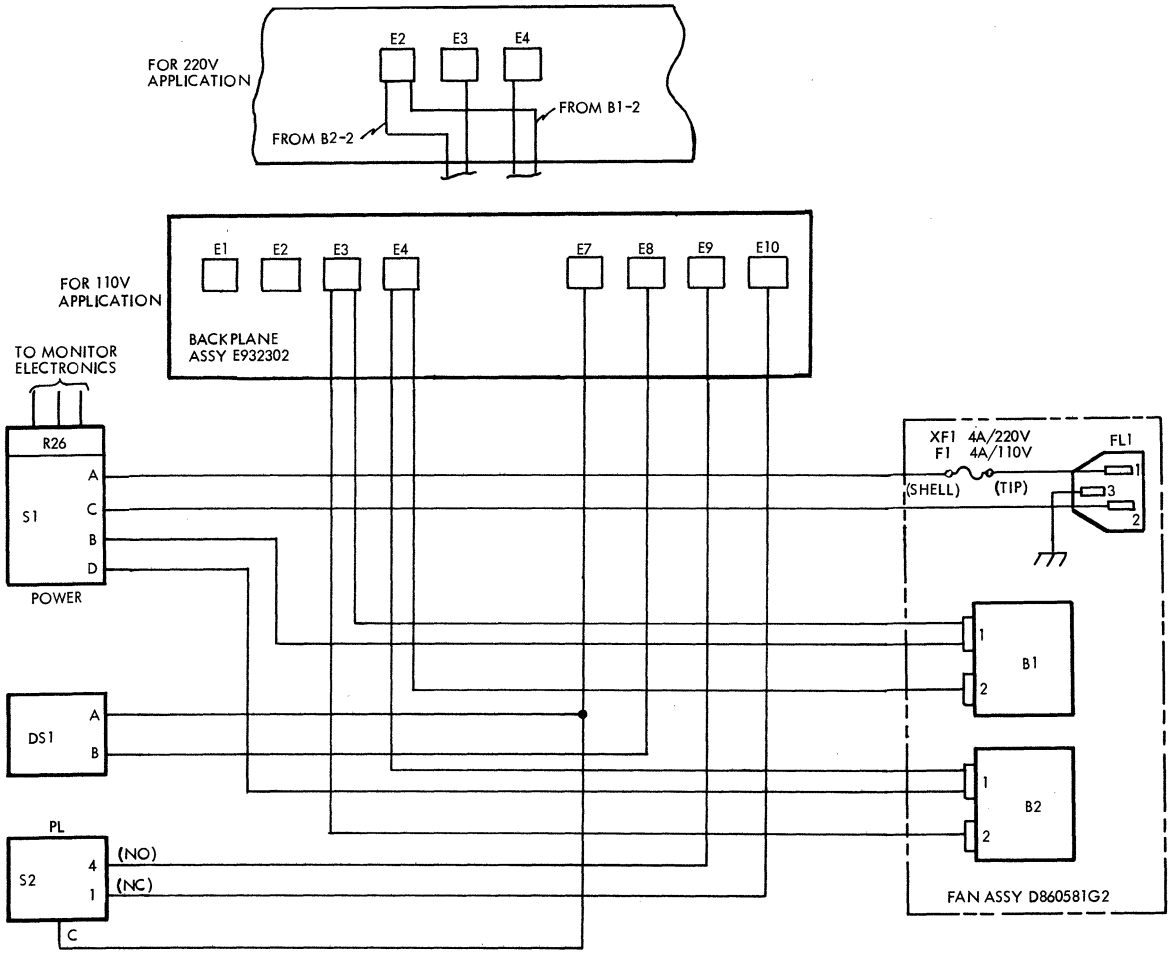


Figure 6-7. Processing Unit Model 1010/1015 Cabinet Wiring Diagram
(Sheet 2 of 2)

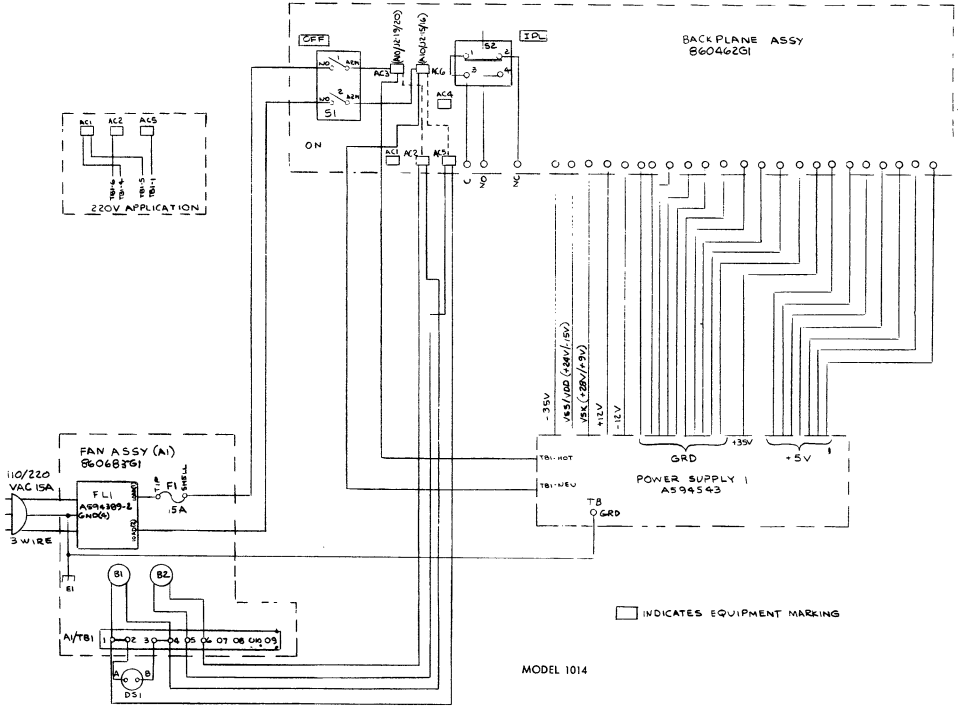


Figure 6-8. Processing Unit Model 1014 Cabinet Wiring Diagram

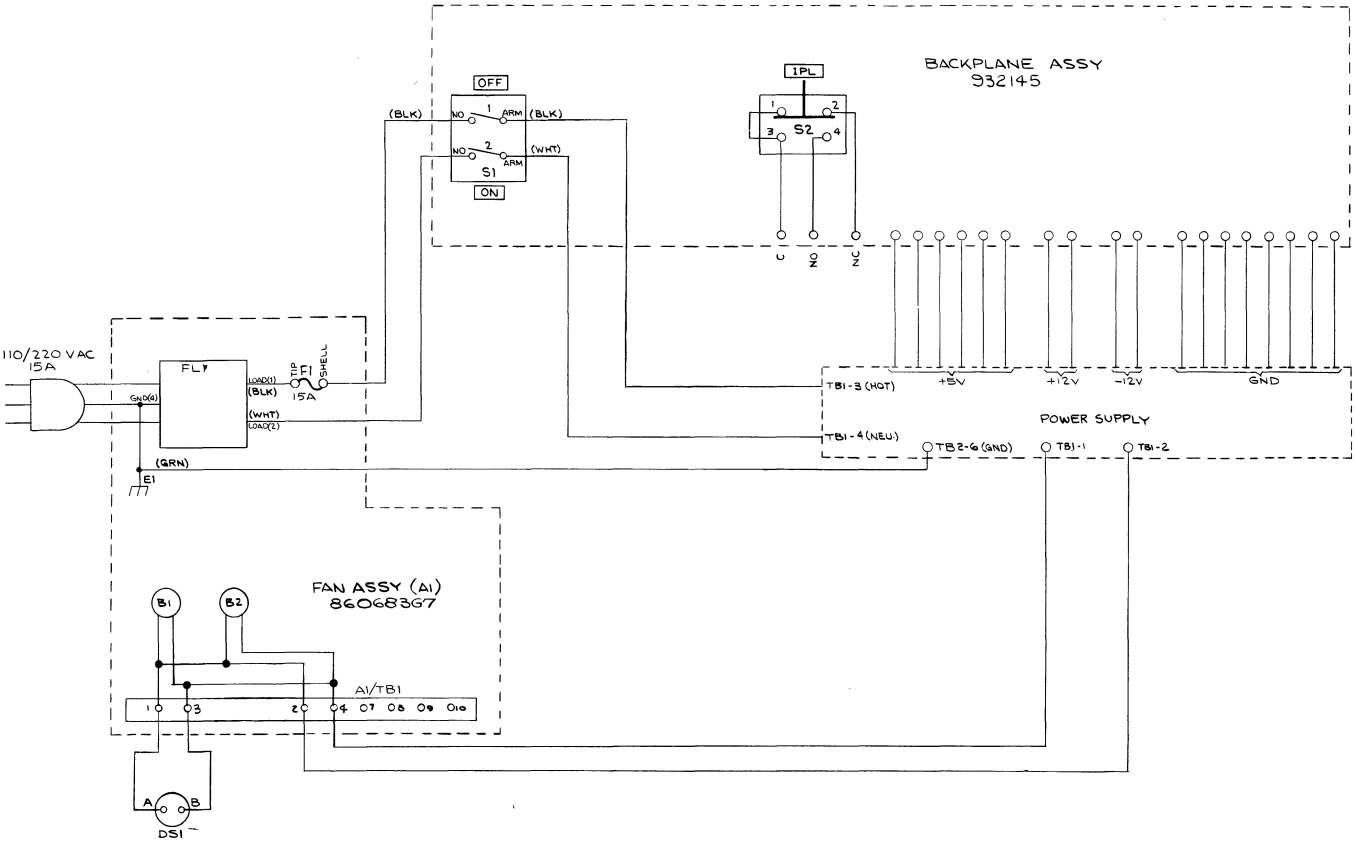


Figure 6-9. Processing Unit 1018 Cabinet Wiring Diagram

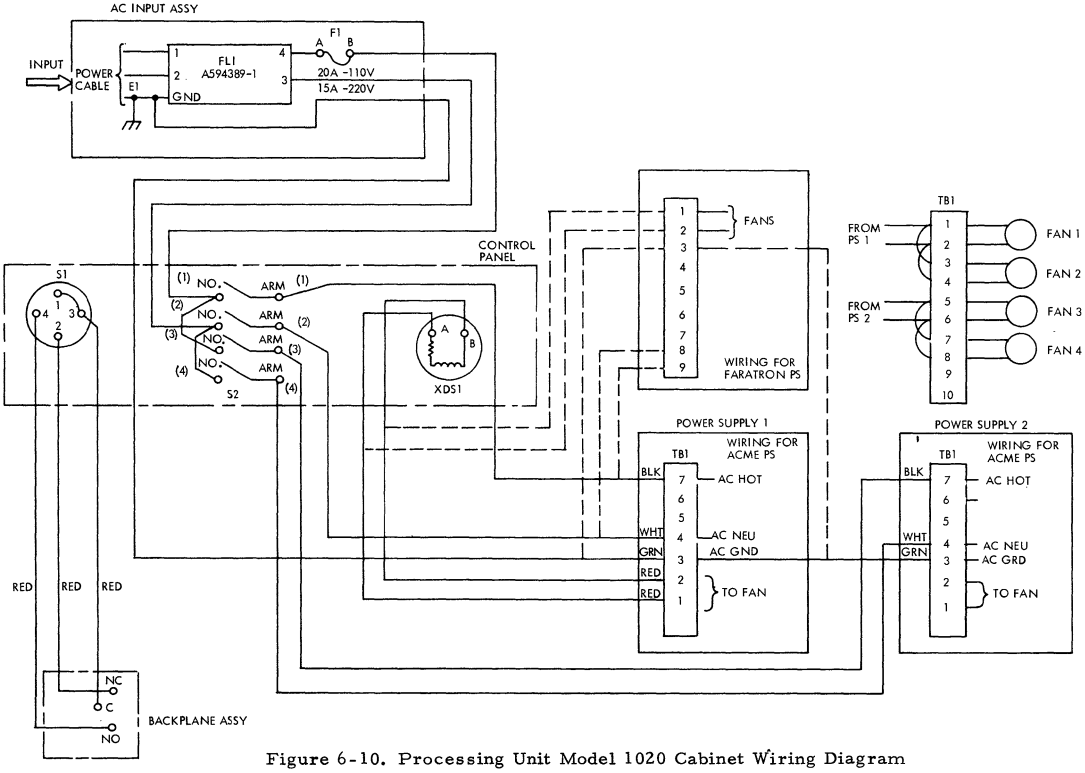


Figure 6-10. Processing Unit Model 1020 Cabinet Wiring Diagram

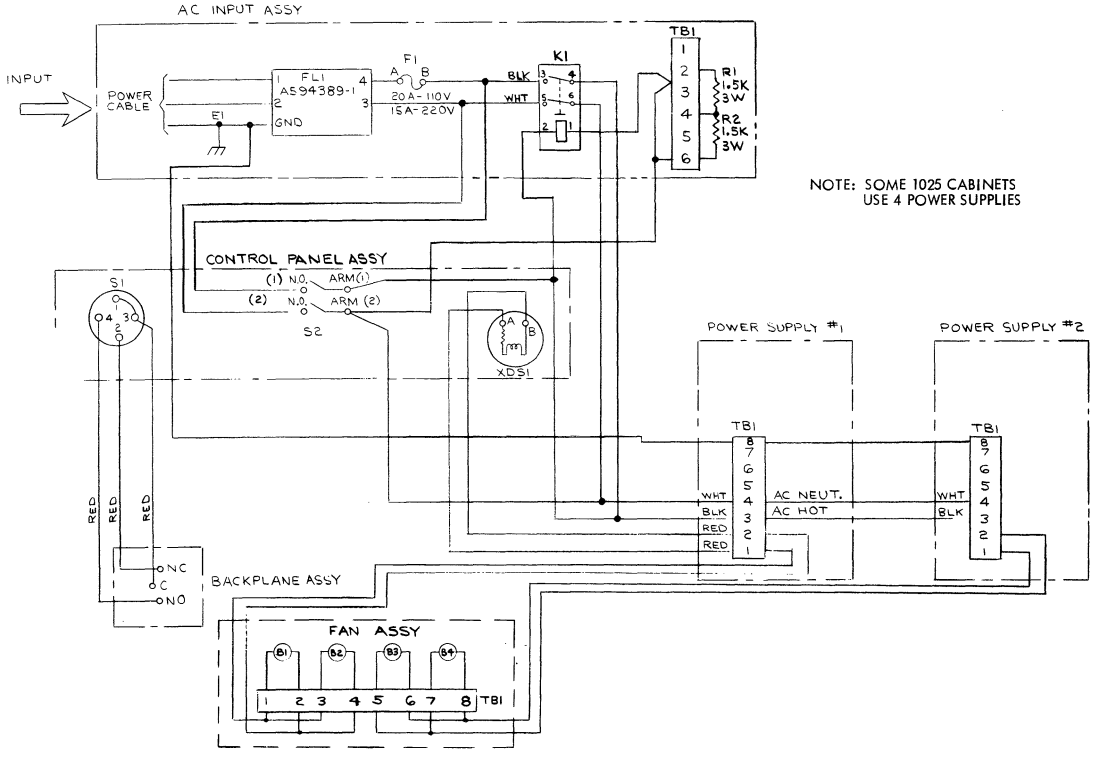


Figure 6-11. Processing Unit 1025 Cabinet Wiring Diagram

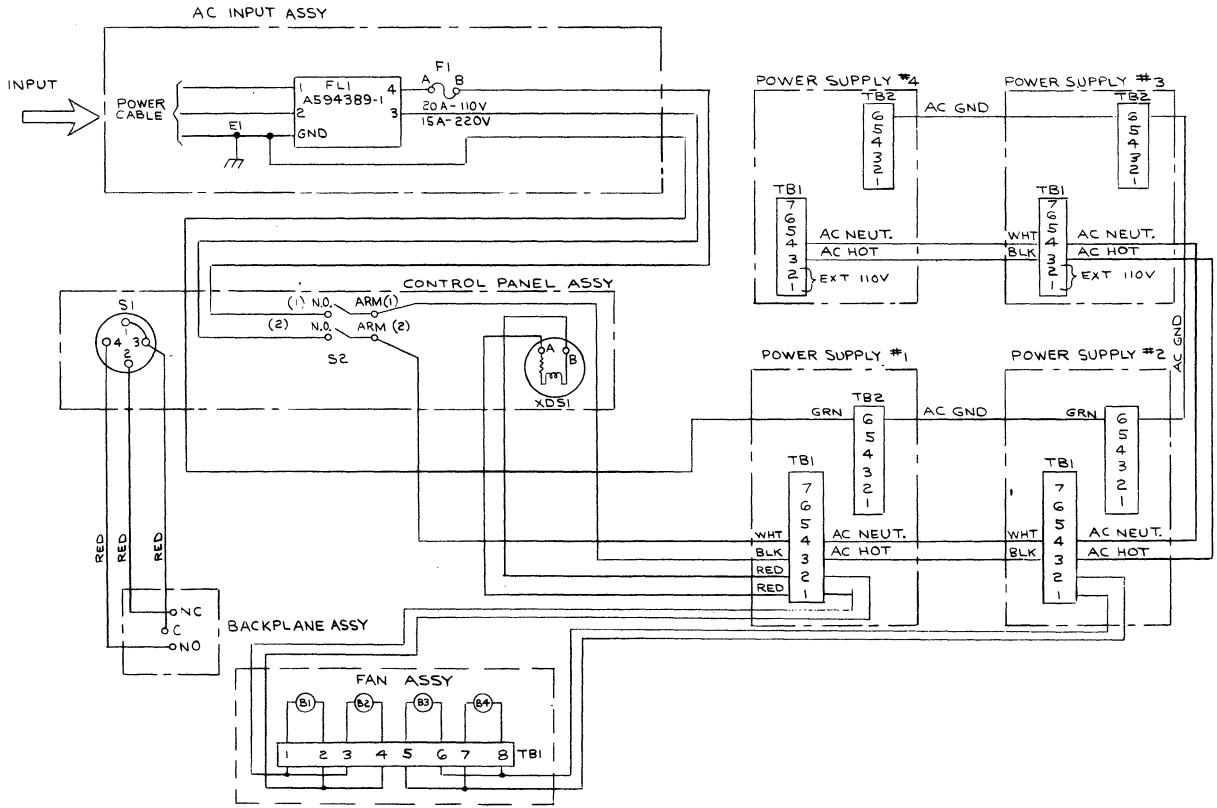


Figure 6-12. Processing Unit 1030 Cabinet Wiring Diagram (Sheet 1 of 4)

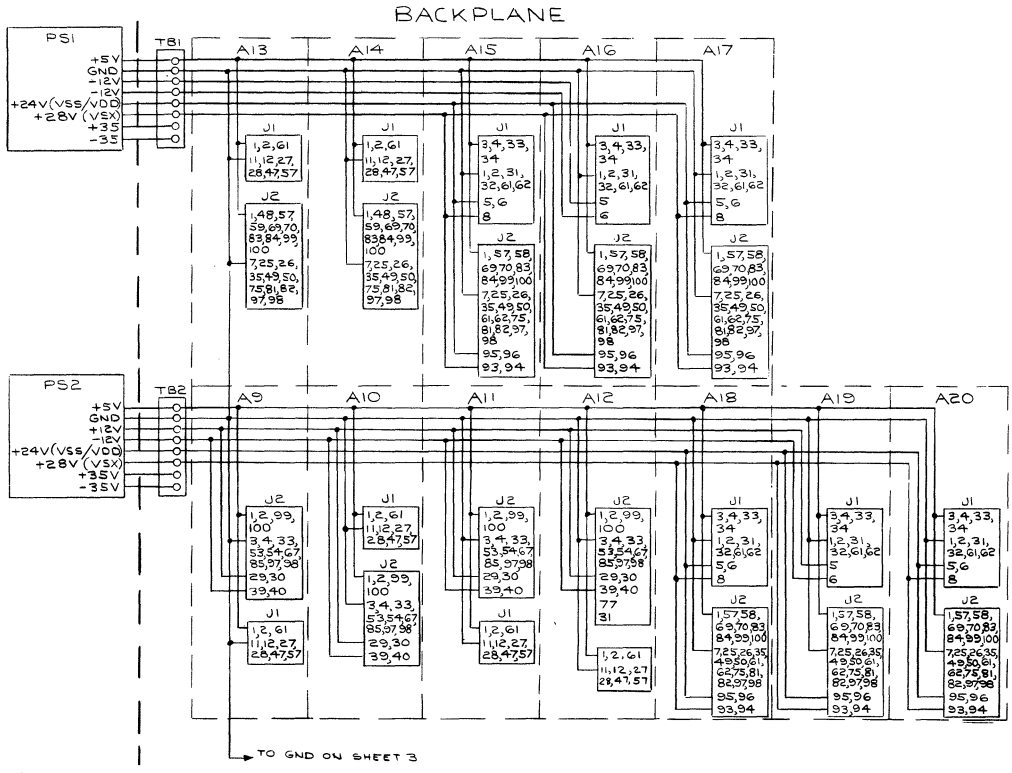


Figure 6-12. Processing Unit 1030 Cabinet Wiring Diagram (Sheet 2 of 4)

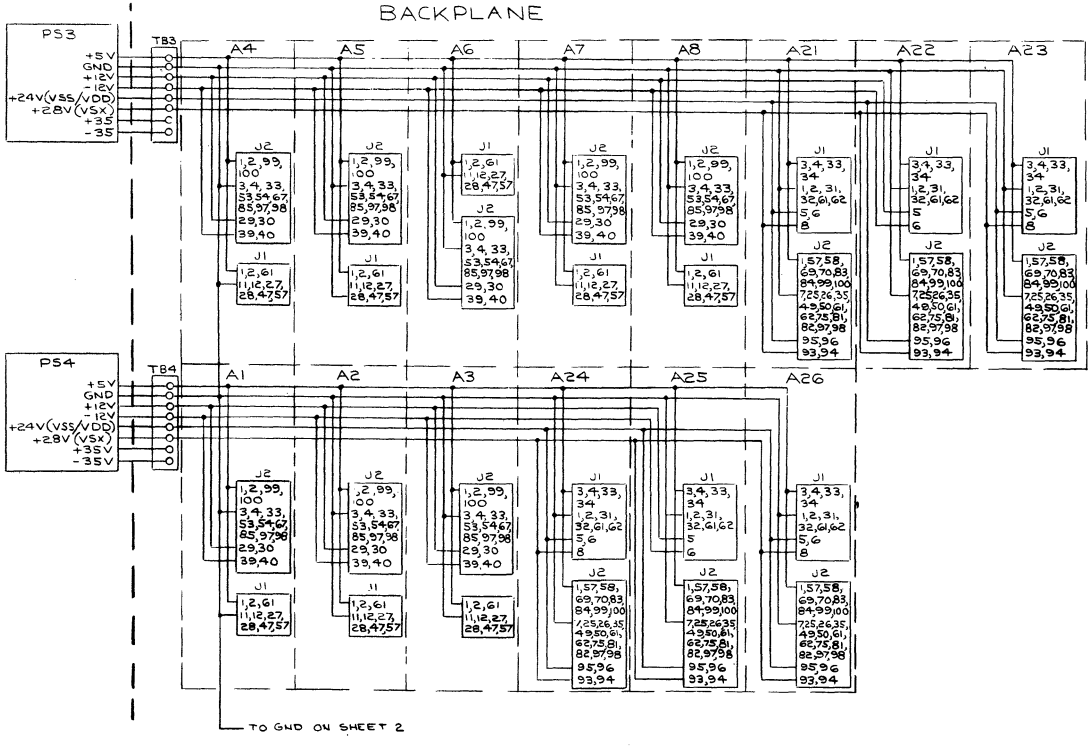


Figure 6-12. Processing Unit 1030 Cabinet Wiring Diagram (Sheet 3 of 4)

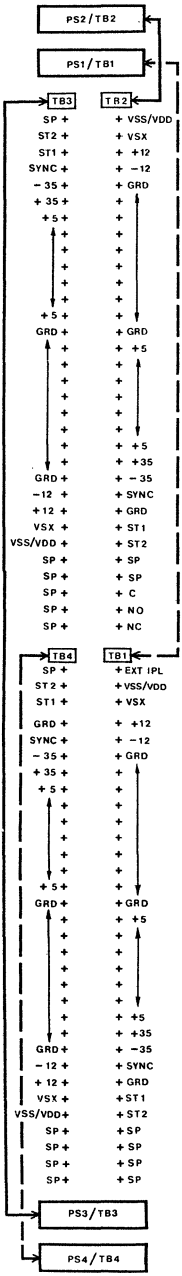


Figure 6-12. Processing Unit 1030 Cabinet Wiring Diagram (Sheet 4 of 4)

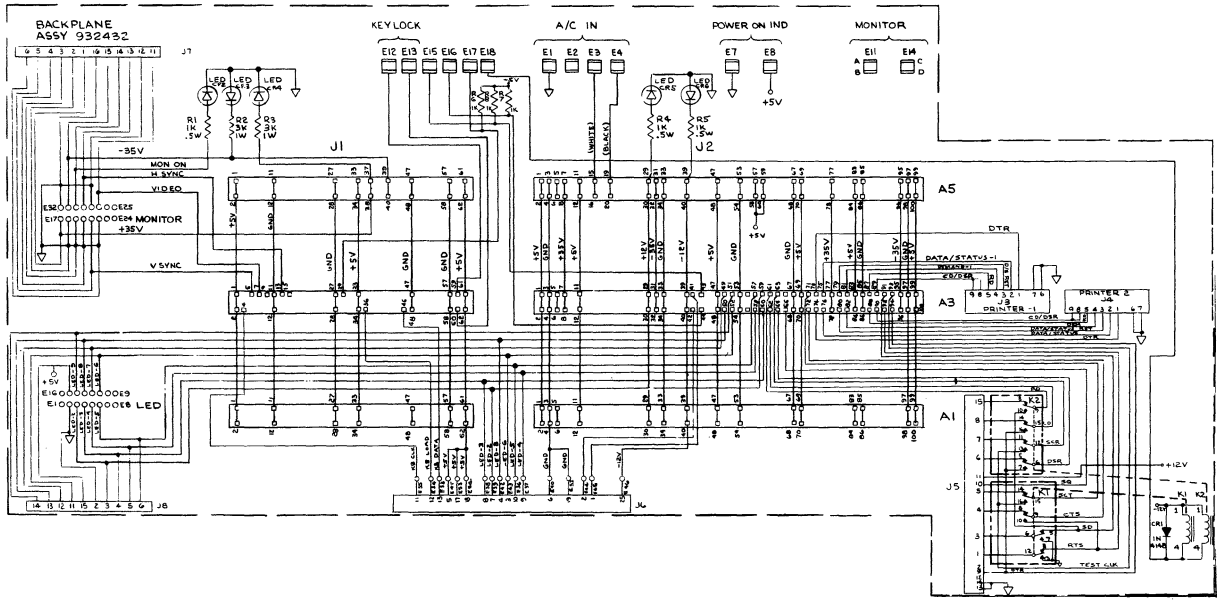


Figure 6-13. 1001/A Backplane Schematic Diagram

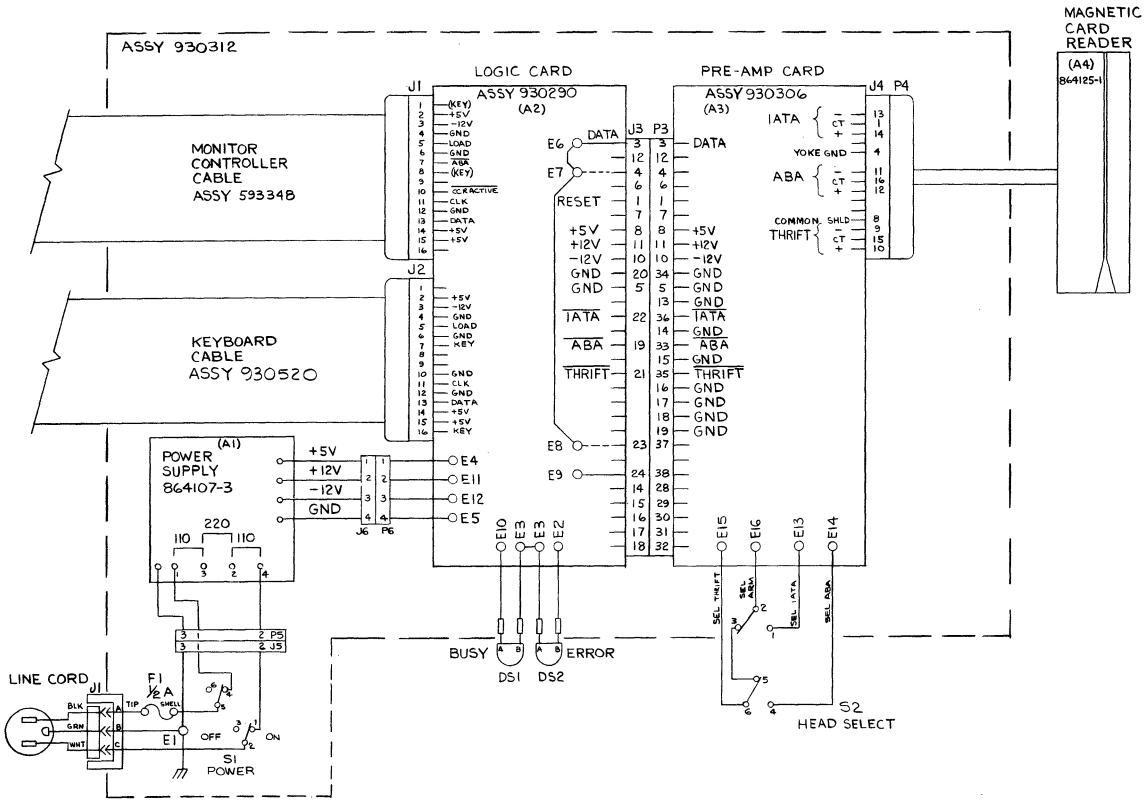


Figure 6-14. Magnetic Stripe Credit Card Reader Wiring Diagram

APPENDIX A

FEATURE BOARDS

APPENDIX A. FEATURE BOARDS

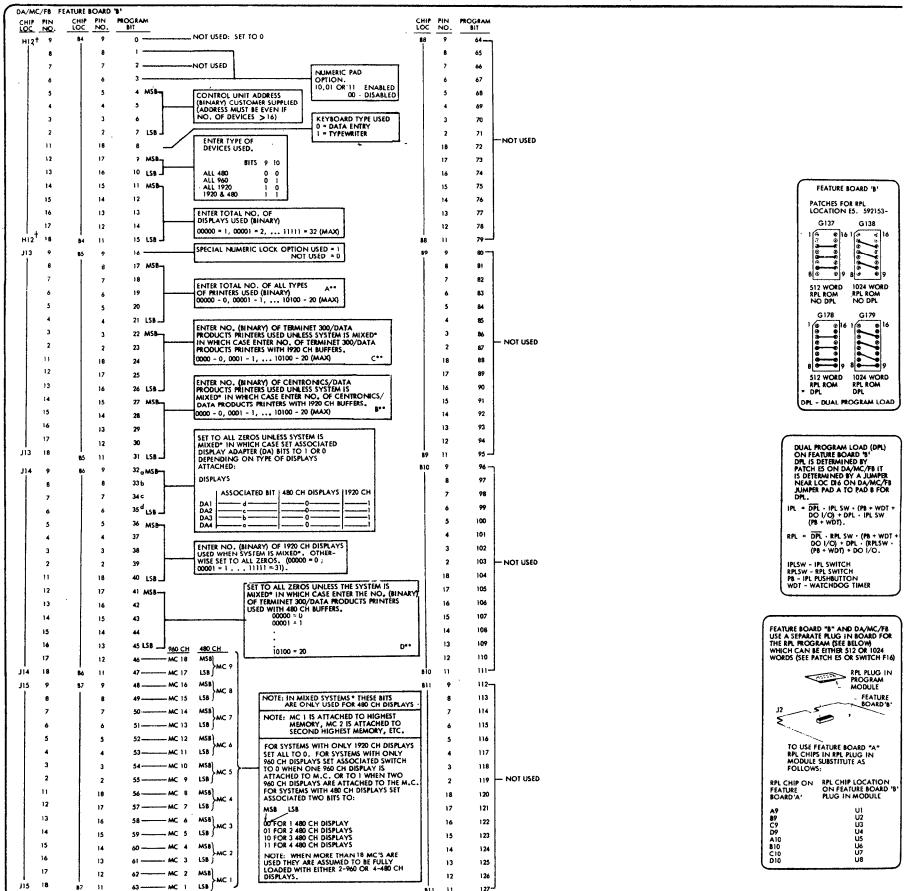
TABLE OF CONTENTS

TABLE OF CONTENTS (cont)

FEATURE BOARD A TO B CONVERSION

A		B			A		B		
Chip Loc	Switch	Chip Loc	Pin No.	Prog Bit	Chip Loc	Switch	Chip Loc	Pin No.	Prog Bit
A4	8	B4	9	0	D4	8	B7	9	48
	7		8	1		7		8	49
	6		7	2		6		7	50
	5		6	3		5		6	51
	4		5	4		4		5	52
	3		4	5		3		4	53
	2		3	6		2		3	54
	1		2	7		1		2	55
A6	8		18	8	D6	8		18	56
	7		17	9		7		17	57
	6		16	10		6		16	58
	5		15	11		5		15	59
	4		14	12		4		14	60
	3		13	13		3		13	61
	2		12	14		2		12	62
	1		11	15		1		11	63
B4	8	B5	9	16					
	7		8	17					
	6		7	18					
	5		6	19					
	4		5	20					
	3		4	21					
	2		3	22					
	1		2	23					
B6	8		18	24					
	7		17	25					
	6		16	26					
	5		15	27					
	4		14	28					
	3		13	29					
	2		12	30					
	1		11	31					
C4	8	B6	9	32					
	7		8	33					
	6		7	34					
	5		6	35					
	4		5	36					
	3		4	37					
	2		3	38					
	1		2	39					
C6	8		18	40					
	7		17	41					
	6		16	42					
	5		15	43					
	4		14	44					
	3		13	45					
	2		12	46					
	1		11	47					

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR 3272 LOCAL EMULATOR



* A MIXED SYSTEM IS A SYSTEM THAT UTILIZES BOTH 480 CH AND 1920 CH DEVICES.

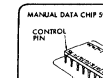
960 CH DEVICES ARE NOT ALLOWED ON MIXED SYSTEMS.

† J12 ON SOME OLDER BOARDS

**WHEN DATA PRODUCTS LINE PRINTERS ARE USED THE STATUS SWITCHES (F1) ON THE PARALLEL ADAPTER MUST BE SET TO 0001011X SEE NOTE ON REVERSE FOR A,B,C & D.

MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA/MC/FB	FEATURE BOARD B	IPL	512 RPL	1024 RPL
J12 †	B4	40,41	40,41	40,41
J13	B5	42,43	42,43	42,43
J14	B6	44,45	44,45	44,45
J15	B7	46,47	46,47	46,47
	B8	80,81	400,401	800,801
	B9	82,83	402,403	802,803
	B10	84,85	404,405	804,805
	B11	86,87	406,407	806,807

MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THIS LEG.

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:

SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)

SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)

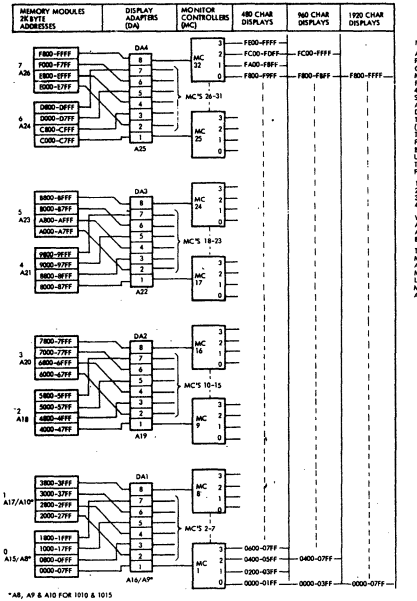
SWITCH 7 - OPEN WHEN IN OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE

SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, A9 & A10 FOR 1010 & 1015

NOTES

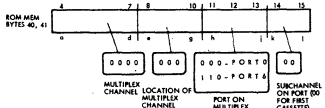
ALL DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. IN A MIXED SYSTEM 1920 CH DISPLAYS ARE ASSIGNED BEFORE 480 CH DISPLAYS. ALSO THE STARTING MEMORY ADDRESSES ARE DETERMINED BY WHICH DISPLAY ADAPTERS ARE ASSIGNED TO 1920 CH AND 480 CH DISPLAYS (SEE C4 ON F.B.'A'). IF A SYSTEM IS MIXED OR DOES NOT FULLY LOAD ALL M.C.'s, PRINTER BUFFERS WILL BE ASSIGNED TO THE UNUSED AREAS. IN A MIXED SYSTEM PRINTERS ARE ASSIGNED AS FOLLOWS:

1 CENTRONICS - 1920 CH BUFFER (B)
2 TERMINET - 1920 CH BUFFER(C)
3 CENTRONICS - 480 CH BUFFER (A)-(B+C+D)
4 TERMINET - 480 CH BUFFER (D)

WHEN DATA PRODUCTS LINE PRINTERS ARE USED THEY MAY BE ASSIGNED TO ANY OR ALL OF THE ABOVE PRINTER BUFFER AREAS.

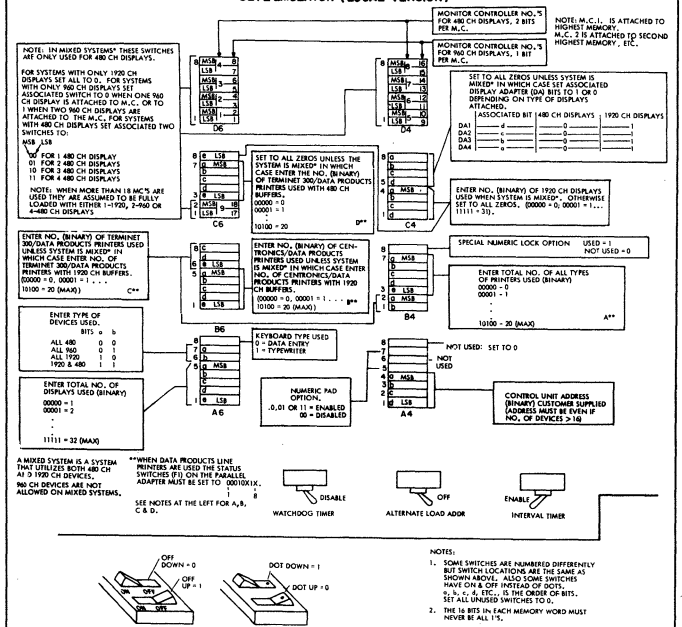
THE PROGRAM RESIDES IN LOWER MEMORY. NORMALLY IN MODULES A17/A10* AND A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 0000 THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR 3272 EMULATOR (LOCAL VERSION)



MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO AND HALF DUPLEX) PRINTERS	MULTIPLEX CHANNEL PORT 0	1	2	3	4	5	6	7*
	1,17	2,18	3,19	4,20	5,21	6,22	7,23	8,24
	33	34	35	36	37	38	39	40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25	10,26	11,27	12,28	13,29	14,30	15,31	16,32
	41	42	43	44	45	46	47	48

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PORT 1 AND 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER ARE NOT USED

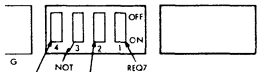
FIRST PRINTER IS ASSIGNED TO PORT 3 OF FIRST MULTIPLEX CHANNEL CONTROLLER

ADDITIONAL PRINTERS ARE ASSIGNED TO ALL OTHER PORTS (SEE "PRINTER" DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS).

MULTIPLEX CHANNEL CONTROLLER

DISABLE/ENABLE PORT 7 SWITCH*

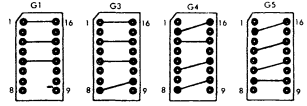
S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS 592153-



FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-) INTO BOARD LOCATIONS D15 AND J16	
80 X 24	G1	G3
80 X 12	G1	G4
40 X 12	G1	G5

MONITOR CONTROLLER* CHARACTER/LINE FORMAT E6 SWITCH SETTINGS

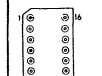
SWITCH	40 X 12	80 X 12	(24)	OPTIONS
1	——	——	——	NOTE 1
2	——	——	——	NOTE 2
3	OPEN	OPEN	CLOSED	——
4	OPEN	CLOSED	CLOSED	——
5	CLOSED	CLOSED	CLOSED	——
6	CLOSED	OPEN	OPEN	——
7	OPEN	CLOSED	CLOSED	——
8	——	——	——	NOTE 3

*C BOARD ONLY

NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

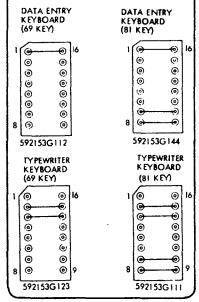


G2 BOARD LOCATION

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

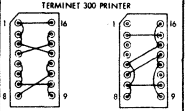
KEYBOARD PATCHES

MAKE THE FOLLOWING PATCH CONNECTIONS ON THE PATCH PLUG LOCATED ON THE RIGHT REAR OF THE KEYBOARD.



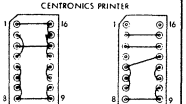
MISA PATCHES

TERMINET 300 PRINTER



MS - BOARD LOCATION - B2

CENTRONICS PRINTER

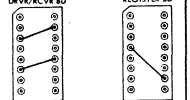


MS - BOARD LOCATION - B2

NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

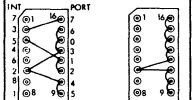
CIC PATCHES



THIS PATCH ALLOWS MORE THAN 16 DEVICES TO BE ADDRESSED (592153G88)

INTERRUPT LEVEL 4 (592153G89)

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



FIRST MULTIPLEX CHANNEL CONTROLLER

2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

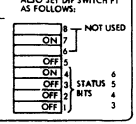
DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
CIC	N/A	N/A	4
PRINTERS 1-4	0	3-6	2
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2

PARALLEL ADAPTER PATCHING AND SWITCHING FOR DATA PRODUCTS 2200 LINE PRINTER

IN THESE LOCATIONS	INSERT PATCHES 592152-
A2	G148
D3	G148
B2	G149

ALSO SET DIP SWITCH F1 AS FOLLOWS:



MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT 40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5				
6		See Below		
7				
8				

Options:

Switch 5	Set to closed to disable the controlled data field feature.
Switch 6	Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)
Switch 7	When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset. When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.
Switch 8	Closing disables the Display Power On option and returns this bit to software control.
Switch Chip	D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.

for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

AUGUST 1975
44-10030
Sheet 3 of 4

PATCH AND SWITCH SETTINGS FOR 3272 LOCAL EMULATOR

COMMUNICATIONS REGION DEFINITION (POINTED TO BY LOC 000C)

DISPLACEMENT	DEFINITION
0	REVISION LEVEL (ASCII) ↑ REVISION SUB-LEVEL (ASCII)
2	ADDRESS OF CIC DEVICE PACKETS
4	ADDRESS OF CIC TUMBLE TABLE
6	ADDRESS OF CIC ADDRESS TRANSLATE TABLE
8	ADDRESS OF CIC OFF LINE TABLE
A	ADDRESS OF CHANNEL I/O BUFFER*
C	ADDRESS OF DUMMY WORK BUFFER
E	ADDRESS OF KEYBOARD IOCQ
10	ADDRESS OF CIC CONTROLLER IOCQ
12	ADDRESS OF CIC DEVICE IOCQ
14	ADDRESS OF KEYBOARD TUMBLE TABLE
16	ADDRESS OF KEYBOARD TRANSLATE TABLE
18	LOAD ADDRESS OF K/PSVC MODULE
1A	LOAD ADDRESS OF CSVC MODULE
1C	LOAD ADDRESS OF ISVC MODULE
1E	ADDRESS OF SRM PARAMETER LIST
20	ADDRESS OF DCQ ADDRESS TABLE

*CONSISTS OF 2 BUFFERS OF EQUAL SIZE. SIZE DETERMINED BY SUBTRACTING THIS ADDRESS FROM DUMMY WORK BUFFER ADDRESS.

DCQ DEFINITION

0	LED BYTE*	CONFIG 1*
2+	NO. CHAR/LINE	NO. LINES
4	STATUS*	AID (ASCII)**
6	BASE BUFFER ADDRESS	
8	CURRENT BUFFER ADDRESS	
A	CURSOR ADDRESS	
C	ATTRIBUTE ADDRESS	
E	NEXT DCQ ADDRESS	
14	DEVICE ADDRESS (BINARY)	
16	KYBD ADDR OR PRINTER AUX/PORT - LUN ID	
1A	DEBUG*	CONFIG 2*

NOTES: DCQ'S ARE LOCATED AT THE END OF EACH DEVICE'S BUFFER AREA.
*REFER TO DCQ BIT DEFINITION TABLE BELOW FOR DEFINITIONS.
**REFER TO 3270 SPECIFICATION
+ NOT VALID FOR PRINTERS

DCQ BIT DEFINITIONS

BYTE / BIT	LED BYTE	CONFIGURATION 1	CONFIGURATION 2	STATUS	DEBUG
0	POWER	0=DISPLAY 1=PRINTER	PRINTER/KYBD TYPE*	NOT USED	DEBUG ENABLED-FULL SCREEN DUMP
1	SYSTEM AVAILABLE	DEVICE ON LINE		NOT USED	1 LINE DUMP
2	INPUT INHIBIT	FORMATTED SCREEN		NOT USED	
3	INSERT	NOT USED		IR PENDING	
4	ALARM	0=DATA ENTRY OR TERMINET/DATA PRODUCTS 1=TYPEWRITER OR CENTRONICS	NOT USED	DEVICE BUSY	NOT USED
5	DSR (NOT USED)	OVERRIDE ON KEYBOARD		NOT USED	
6	XMIT/RCV	LOCAL PRINT REQUEST		DE PENDING	
7	DEBUG MODE	ALARM REQUEST		NOT USED	

*1 0 = DATA PRODUCTS PRINTER

CASSETTE PROGRAM PATCH PROCEDURE

1. IPL OLD CASSETTE.
2. DURING IPL STORE X'80XX' INTO LOCATION 0 (WHERE XXX = DEVICE ADDRESS OF TARGET DRIVE).
3. WHEN IPL IS COMPLETE LOCATION 0 WILL CONTAIN X'0100'. IF NOT RETRY.
4. ENTER PATCHES. DO NOT PRESS STOP OR RESET.
5. PUT A NEW CASSETTE IN TARGET DRIVE.
6. STORE X'80XX' INTO LOCATION 0 AS ABOVE. LOCATION 0 WILL CHANGE TO X'0300' TO INDICATE THAT THE DUMP IS IN PROGRESS.
7. THE TAPE WILL REWIND AND STOP WHEN COMPLETE AND LOCATION 0 WILL CONTAIN X'0100'. IF MORE COPIES ARE DESIRED RETURN TO STEP 5.
8. IF AN ERROR OCCURS, THE TAPE WILL TRY TO REWRITE CONTINUOUSLY. TO START OVER INSERT A NEW CASSETTE AND STORE X'80XX' INTO LOCATION 0.

NOTE: FOR ADDITIONAL INFORMATION REFER TO FIB NO. PS-0018.

INITIALIZER ERROR MESSAGES

NOTE: INITIALIZER WILL DISPLAY THE FOLLOWING ERROR MESSAGES IN THE TOP 1920 BYTES OF REFRESH MEMORY.

ERROR MESSAGE	MEANING
ADAP	INSUFFICIENT ADAPTERS
MEM	INSUFFICIENT MEMORY
PTRS	MORE THAN 30 PRINTERS
DEV	MORE THAN 32 DEVICES
1920	MORE THAN 24 1920 CH DEVICES

LOCATION PARAMETER

0004	FIRST DCQ
0008	DCQ OF DEVICE BEING SERVICED
000A	CIC PACKET OF DEVICE BEING SERVICED
000C	COMMUNICATIONS REGION ADDRESS
0018	FIRST PRINTER DCQ (IF ANY)

SRM NODE DEFINITION

SRM	NODE DEFINITION
+0	LINK TO NEXT (0=END OF LIST)
+2	ADDRESS TO START TRACE (LSB ON = INDIRECT)
+4	NUMBER OF BYTES TO TRACE
+6	DEVICE ID (BINARY) — DISPLAYED ON TRACE TO IDENTIFY ENTRY
+7	NODE ID (ASCII)
+8	TRACE MASK*
*A to A+n	SCRATCH AREA WHERE n = NO. OF BYTES TO TRACE

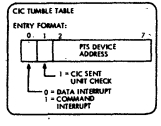
*MASK - BIT 0 = 1 SKIP THIS NODE.
BITS 1-15 = 1 SKIP CORRESPONDING WORD (i.e., bit 15 = word 0, bit 14 = word 1)

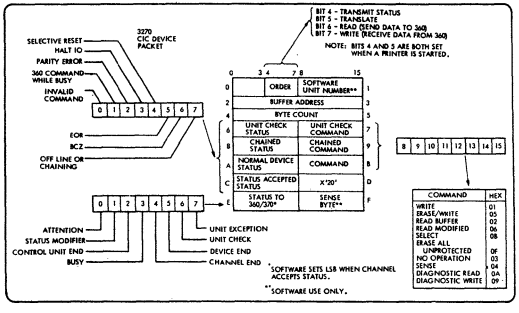
SRM PARAMETER LIST DEFINITION

SRM	PARAMETER LIST DEFINITION
+0	SRM SWITCH; 0 = ENABLE, 8000 = DISABLE
+2	ADDRESS OF NODE LIST
+4	WIDTH OF DISPLAY AREA
+6	NO. OF LINES IN DISPLAY AREA
+8	BASE ADDRESS OF DISPLAY AREA
+A	CURRENT DISPLAY ADDRESS (INITIALLY = BASE)
+C	CURRENT LINE POSITION (INITIALLY = 0)
+E	CURRENT COLUMN POSITION (INITIALLY = 0)

CIC TUMBLE TABLE

ENTRY FORMAT:





COMMAND	HEX
WRITE	01
ERASE/WRITE	05
READ BUFFER	02
READ MODIFIED	06
SELECT	0B
ERASE ALL UNPROTECTED	0F
NO OPERATION	03
SENSE	04
DIAGNOSTIC READ	0A
DIAGNOSTIC WRITE	09

DEBUG PROGRAM OPERATING PROCEDURE

TO ENTER DEBUG:
TYPE <CAN>, PRESS PA1
ENTER COMMANDS AT HOME; CURSOR ENDS LINE
ALL NUMBERS ARE HEX

COMMANDS:

HA, A, B	-	ADD A+B
HS, A, B	-	A-B
DM	-	SET DUMP=FULL SCREEN
DL	-	SET DUMP=TOP LINE ONLY
C.P, D1, D2, D3...	-	COPY FROM DEVICE 1 TO DEVICE 2, 3, ETC.
TR, LOC, AC, X1, X2, C8	-	TRANSFER TO LOCATION, DEFINE REGISTERS
SI, DEV	-	INITIALIZE SRM INTO DEVICES BUFFER.
PA, LOC, VAL, VAL...	-	PATCH MEMORY
SY	-	SRM ENABLE
SN	-	SRM DISABLE
ID	-	DISPLAY DEVICE ADDRESS BITS 0-7 CONTROL UNIT ADDRESS BITS 8-15 PTS DEVICE ADDRESS
XX	-	EXIT DEBUG MODE (CLEARS SCREEN AND SETS CLEAR AID)
ML, BC	-	MONITOR LOCATIONS, BC=NO. OF BYTES MAX = X'1E'
MO	-	DISABLE LOCATION MONITOR
DK	-	DISABLE ALL KYBDS EXCEPT OURS
EK	-	ENABLE KYBDS
MS, DEV, OP CODE	-	ISSUE CIC MSC DISPLAY RESULT

OP CODES:
0 T = S CUB, SEND ATTN.
1 SET DVB
2 RESET DVB
3 SET OFF LINE
4 RESET OFF LINE
5 T = S CUB, SEND STATUS
6 RESET CUB

RESULTS:
BIT 0 = CONTROL UNIT BUSY
BIT 1 = CONTROLLER BUSY
BIT 2 = DEVICE BUSY
BIT 3 = DEVICE OFF LINE

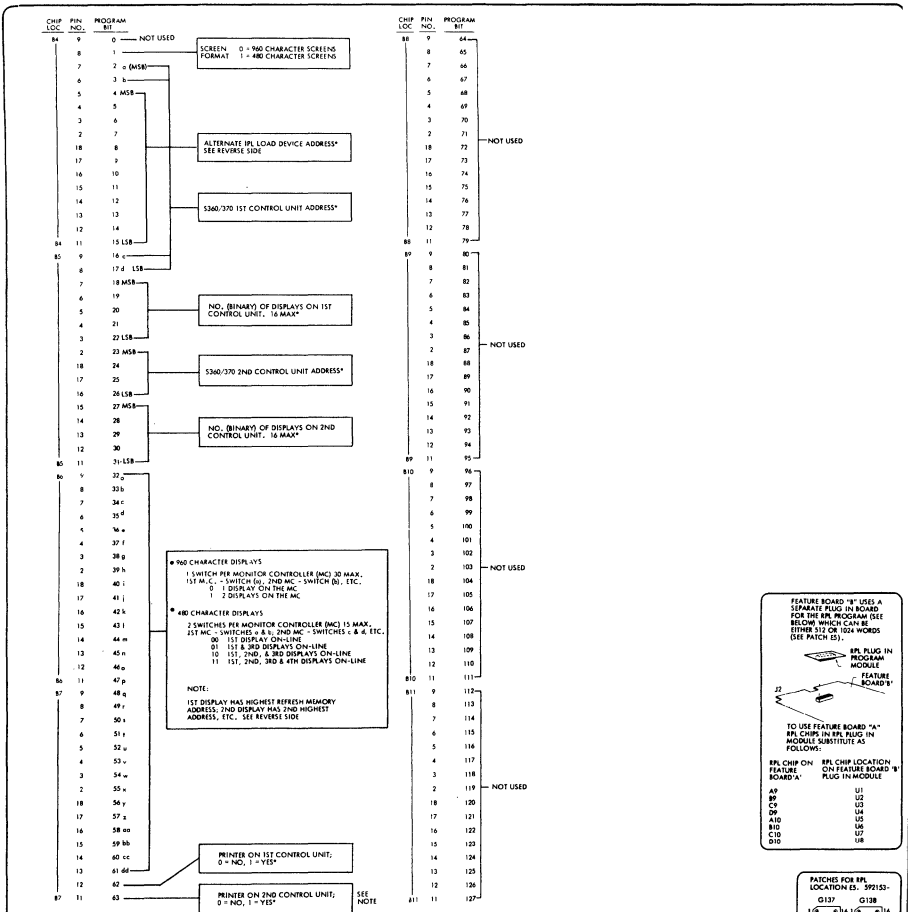
MEMORY DUMP AND ALTER:
IF CURSOR = HOME OR IF NO COMMAND IS DETECTED, MEMORY DUMP IS PERFORMED. IF THE 5TH CHARACTER = 'A', THE DIGITS FOLLOWING THE 'A' UP TO THE CURSOR WILL BE STORED IN THE LOCATION DEFINED BY THE 4 DIGITS PRECEDING THE 'A'. A DUMP IS ALSO PERFORMED.
IF PA1 IS DEPRESSED THE MEMORY DUMP IS SCROLLED UP 16 BYTES. PA2 SCROLLS IT DOWN 16 BYTES.

NOTES: 1. LOCAL PRINT IS PERFORMED BY ENTERING 'Pn' (WHERE n = PRINTER NUMBER) AND DEPRESSING TEST REQUEST.
2. DEV = PTS DEVICE ADDRESS (0'20'-X'3F')
3. LEADING ZEROS NOT REQUIRED

AUGUST 1975
44-10030

SOFTWARE NOTES FOR 3272 LOCAL EMULATOR

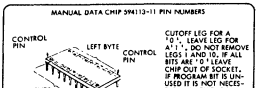
PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR LOCAL 2848/2260 EMULATOR**



NOTE: BITS 62 AND 63 CANNOT BOTH BE 1'S.

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY.

**FOR PROGRAM 592955



MANUAL DATA CHIP LOC	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX) IPL	512 RPL	1024 RPL
B4	40,41	40,41	40,41
B5	42,43	42,43	42,43
B6	44,45	44,45	44,45
B7	46,47	46,47	46,48
B8	80,81	400,401	800, 801
B9	82,83	402,403	802, 803
B10	84,85	404,405	804, 805
B11	86,87	406,407	806, 807

DUAL PROGRAM LOAD (DPL)

DPL IS DETERMINED BY PATCH E5.

IPL = $\overline{DPL}$ · IPL SW · (PB + WDT + DO I/O) + DPL · IPL SW (PB + WDT).

RPL = $\overline{DPL}$ · RPL SW · (PB + WDT + DO I/O) + DPL · (RPLSW + (PB + WDT) + DO I/O.

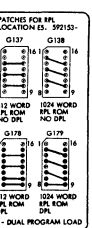
IPLSW = IPL SWITCH
RPLSW = RPL SWITCH
PB = IPL PUSHBUTTON
WDT = WATCHDOG TIMER

FEATURE BOARD "B" USES A SEPARATE PLUG IN BOARD FOR THE RPL PROGRAM (SEE BELOW) WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5).

TO USE FEATURE BOARD "A" RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATION ON FEATURE BOARD 'B' PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

PATCHES FOR RPL LOCATION E5. 592153-



JANUARY 1975
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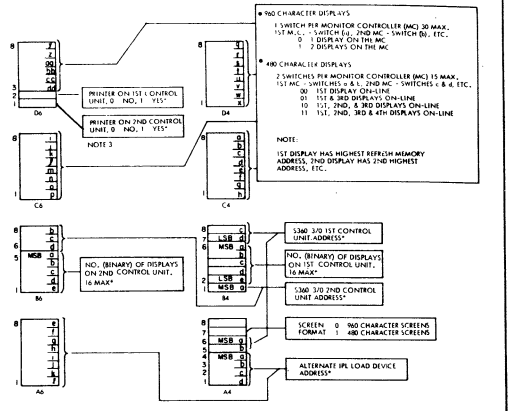
Sheet 1 of 2

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR LOCAL 2848/2260 EMULATOR**

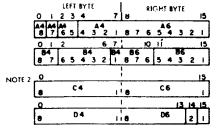


NOTES:

1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC. IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE all 1's.
3. SWITCHES D6 1 & 2 CANNOT BOTH BE 1's.

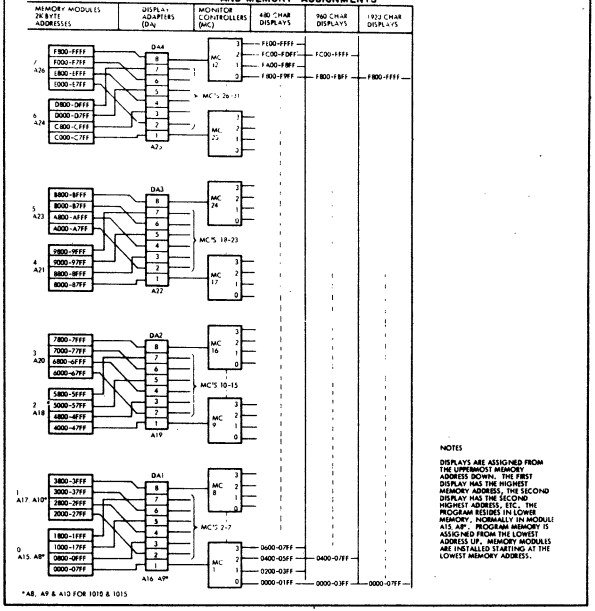
*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY.

**FOR PROGRAM 593955



FOR XORD FUNCTIONS AND SWITCHES SEE ABOVE

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS

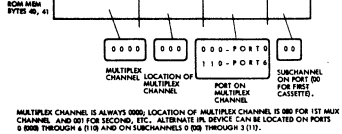


*A8, A9 & A10 FOR 1015 & 1015

NOTES

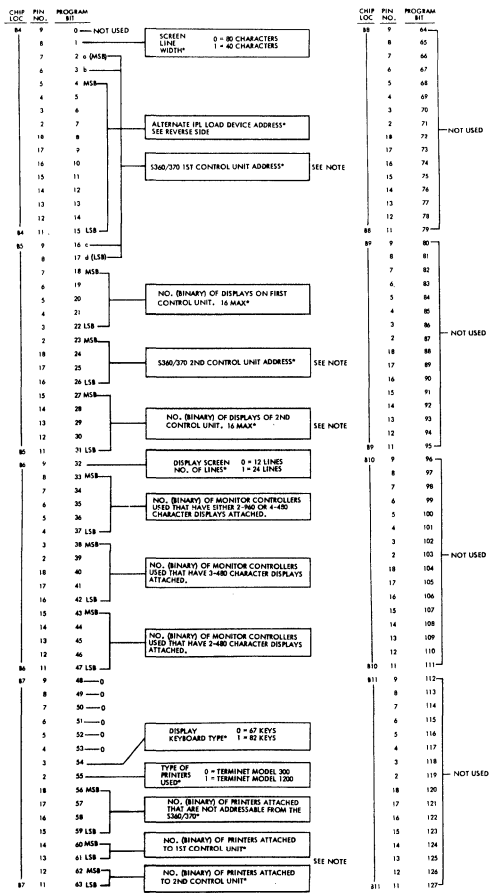
DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY. NORMALLY IN MODULE A15, A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 080 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR 2848/2260 LOCAL EMULATOR (VERSION 1) WITH MULTIPLE PRINTERS

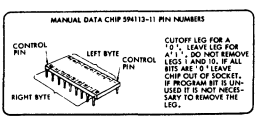


NOTE:

THE CONTROL UNITS ARE THOSE BEING EMULATED BY THE PTS SYSTEM. (C.I.C. RECOGNIZES 2 ADDRESSES).

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY

**EMULATOR 592955



MANUAL DATA CHIP LOC	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX) IPL	512 RPL	1024 RPL
B4	40,41	40,41	40,41
B5	42,43	42,43	42,43
B6	44,45	44,45	44,45
B7	46,47	46,47	46,48
B8	80,81	400,401	800,801
B9	82,83	402,403	802,803
B10	84,85	404,405	804,805
B11	86,87	406,407	806,807

DUAL PROGRAM LOAD (DPL)

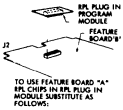
DPL IS DETERMINED BY PATCH E5.

IPL = $\overline{DPL}$ • IPL SW • (PB + WDT + DO I/O) + DPL • IPL SW (PB + WDT)

RPL = $\overline{DPL}$ • RPL SW • (PB + WDT + DO I/O) + DPL • (RPLSW • (PB + WDT) + DO I/O.

IPLSW - IPL SWITCH
RPLSW - RPL SWITCH
PB - IPL PUSHBUTTON
WDT - WATCHDOG TIMER

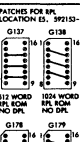
FEATURE BOARD "B" USES A SEPARATE PLUG IN BOARD FOR THE RPL PROGRAM (SEE BELOW) WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5).



TO USE FEATURE BOARD "A" RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATION ON FEATURE BOARD 'B' PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

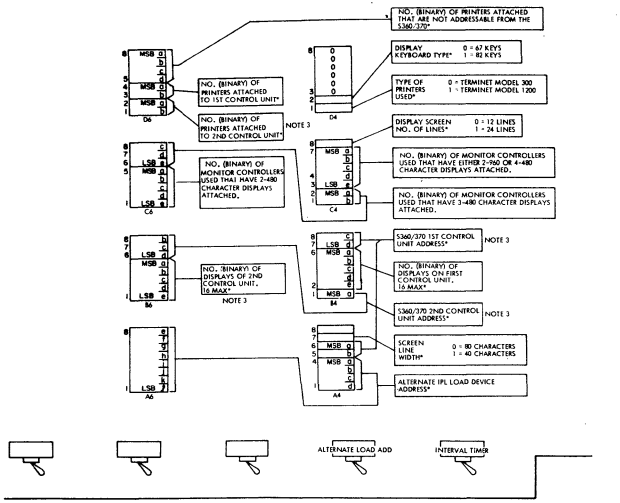
PATCHES FOR RPL LOCATION E5. 592153-



DPL - DUAL PROGRAM LOAD

FEBRUARY 197
44-8067
Sheet 1 of 2

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR LOCAL 2848/2260 EMULATOR (VERSION I)** WITH MULTIPLE PRINTERS

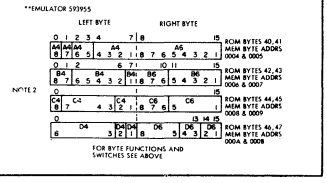


NOTES:

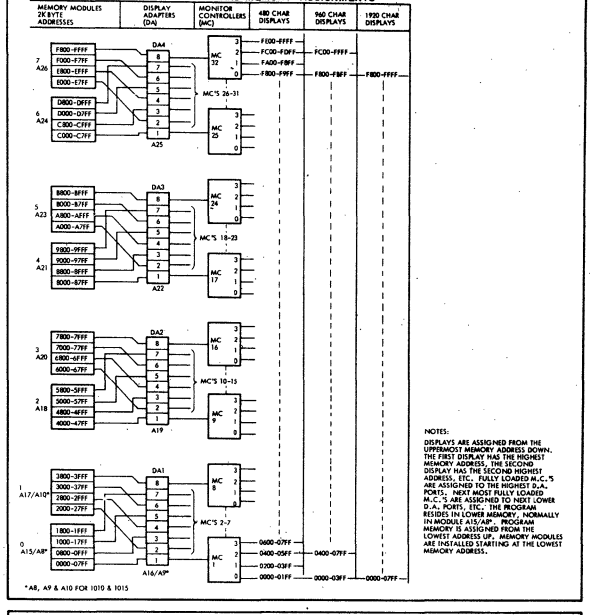
1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1'S.
3. THE CONTROL UNITS ARE THOSE BEING EMULATED BY THE PTS SYSTEM. (C.I.C. RECOGNIZES 2 ADDRESSES).

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY

**EMULATOR 597955



DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS

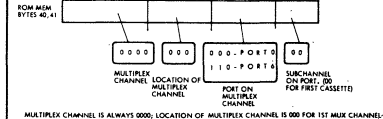


*A8, A9 & A10 FOR 1010 & 1015

NOTES:

DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. FULLY LOADED M.C.'S ARE ASSIGNED TO THE HIGHEST D.A. PORTS; NEXT MOST FULLY LOADED M.C.'S ARE ASSIGNED TO NEXT LOWER D.A. PORTS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000, LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

MULTIPLEX CHANNEL PRINTER PORT ASSIGNMENTS

PRINTER NO.	MUX NO.	PORT NO.
1 - 6	0	1-6
7 - 14	1	0-7
15 - 22	2	0-7

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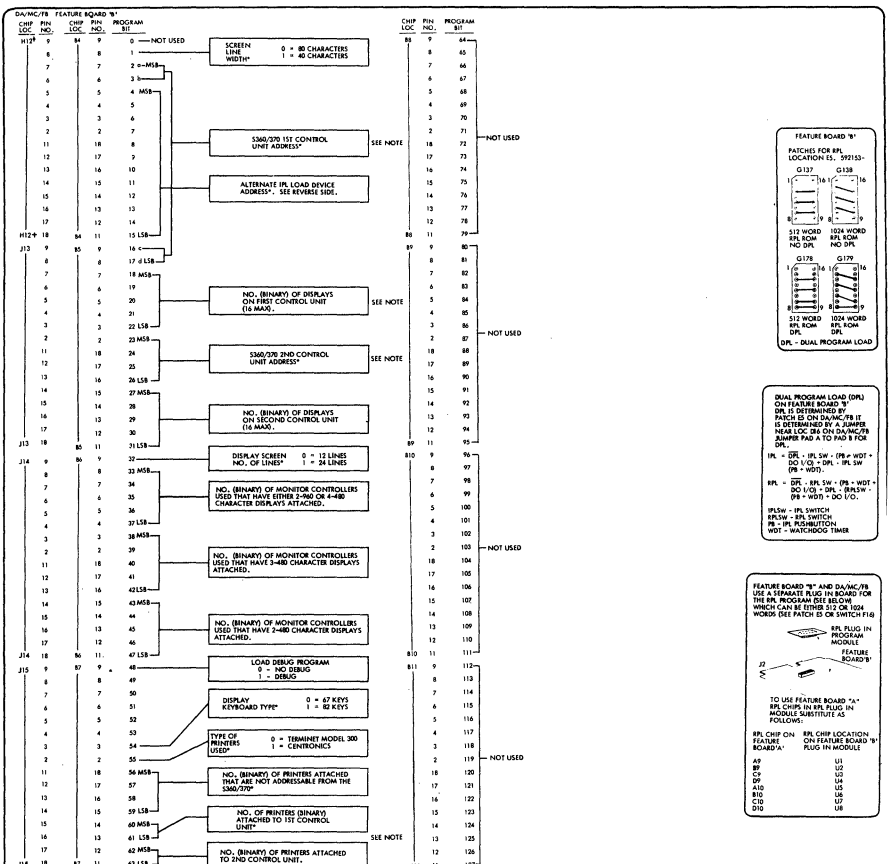
PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR LOCAL 2848/2260 EMULATOR FOR VERSION 2 C.I.C. 863034



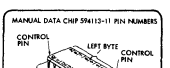
THE CONTROL UNITS ARE THOSE BEING EMULATED BY THE PTS SYSTEM. (C.I.C. RECOGNIZES 2 ADDRESS).

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY.

↑ J12 ON SOME OLDER BOARDS

MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA/MC/FB	FEATURE BOARD 'B'	IPL	512 RPL	1024 RPL
H12 ↑	B4	40,41	40,41	40,41
J13	B5	42,43	42,43	42,43
J14	B6	44,45	44,45	44,45
J15	B7	46,47	46,47	46,47
	B8	B0,B1	400,401	B00,B01
	B9	B2,B3	402,403	B02,B03
	B10	B4,B5	404,405	B04,B05
	B11	B6,B7	406,407	B06,B07

MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

FEATURE BOARD 'B'

PATCHES FOR RPL LOCATION E5, 592153-

DPL - DUAL PROGRAM LOAD

DUAL PROGRAM LOAD (DPL) ON FEATURE BOARD 'B' DPL IS DETERMINED BY PATCH (S) ON DA/MC/FB IF IS DETERMINED BY A JUMPER NEAR LOC D86 ON DA/MC/FB JUMPER PAD A TO PAD B FOR DPL.

IPL = $\overline{DPL}$ • IPL SW - (PB ≠ WDT + DO I/O) + DPL • IPL SW (PB = WDT).

RPL = $\overline{DPL}$ • RPL SW - (PB = WDT + DO I/O) + DPL • (RPLSW - (PB = WDT) + DO I/O).

IPLSW - IPL SWITCH
RPLSW - RPL SWITCH
PB - IPL PUSHBUTTON
WDT - WATCHDOG TIMER

FEATURE BOARD 'B' AND DA/MC/FB USE A SEPARATE PLUG IN BOARD FOR THE RPL PROGRAM (SEE BELOW WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5 OR SWITCH F16)

TO USE FEATURE BOARD 'A' RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS

RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATION ON FEATURE BOARD 'B' PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:

SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)

SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)

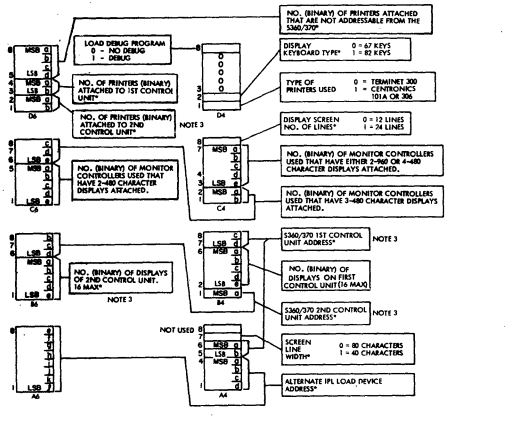
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE

SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL.
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR LOCAL 2848/2260 EMULATOR FOR VERSION 2 C.I.C. 863034



NOTES:

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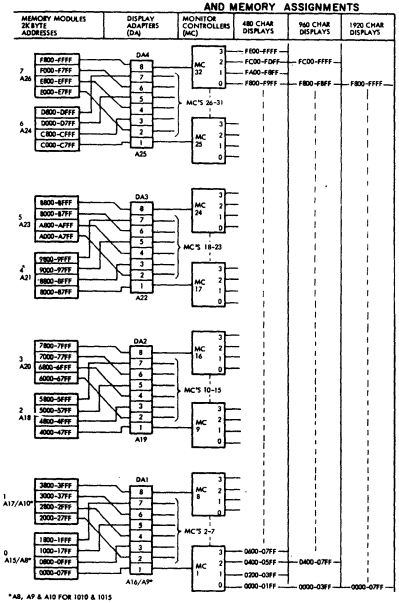
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1'S.
3. THE CONTROL UNITS ARE THOSE BEING EMULATED BY THE PTS SYSTEM. (C.I.C. RECOGNIZES 2 ADDRESSES).

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS

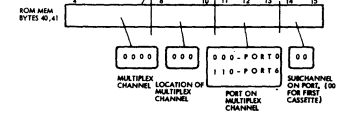


*A8, A9 & A10 FOR 1010 & 1015

NOTES

DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. FULLY LOADED M.C.'S ARE ASSIGNED TO THE HIGHEST D.A. PORTS. NEXT MOST FULLY LOADED M.C.'S ARE ASSIGNED TO THE NEXT LOWER D.A. PORTS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A9*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS (0000). LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110). AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

MONITOR CONTROLLER B AND C CHARACTER/LINE FORMAT E6 SWITCH SETTINGS

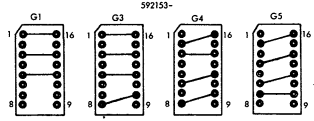
SWITCH	40 X 12	80 X 12	(24)	OPTIONS
1	——	—	—	NOTE 1
2	——	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	——
4	OPEN	CLOSED	CLOSED	——
5	CLOSED	CLOSED	CLOSED	——
6	CLOSED	OPEN	OPEN	——
7	OPEN	CLOSED	CLOSED	——
8	——	—	—	NOTE 3

NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS 592153-



FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-) INTO BOARD LOCATIONS D15 AND J16	
80 X 24	G1	G3
80 X 12	G1	G4
40 X 12	G1	G5

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT 0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM. ALL MODELS (WRITE TO PRINT	1,17	2,18	3,19	4,20	5,21	6,22	7,23	8,24
	33	34	35	36	37	38	39	40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25	10,26	11,27	12,28	13,29	14,30	15,31	16,32
	41	42	43	44	45	46	47	48

NOTE:
CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT 40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5	See Below			
6				
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.
When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.

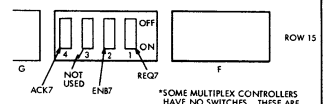
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MULTIPLEX CHANNEL CONTROLLER

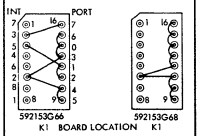
DISABLE/ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



FIRST MULTIPLEX CHANNEL CONTROLLER

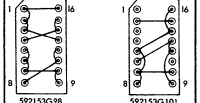
2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
CIC	N/A	N/A	4
PRINTERS 1 - 6	0	1 - 6	2
PRINTERS 7 - 14	1	0 - 7	2
PRINTERS 15 - 22	2	0 - 7	2

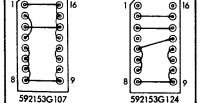
MISA PATCHES

TERMINET 300 PRINTER



M5 - BOARD LOCATION - B2

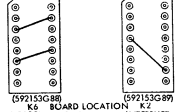
CENTRONICS PRINTER



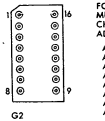
M5 - BOARD LOCATION - B2

NOTE:
SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

CIC PATCHES



MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

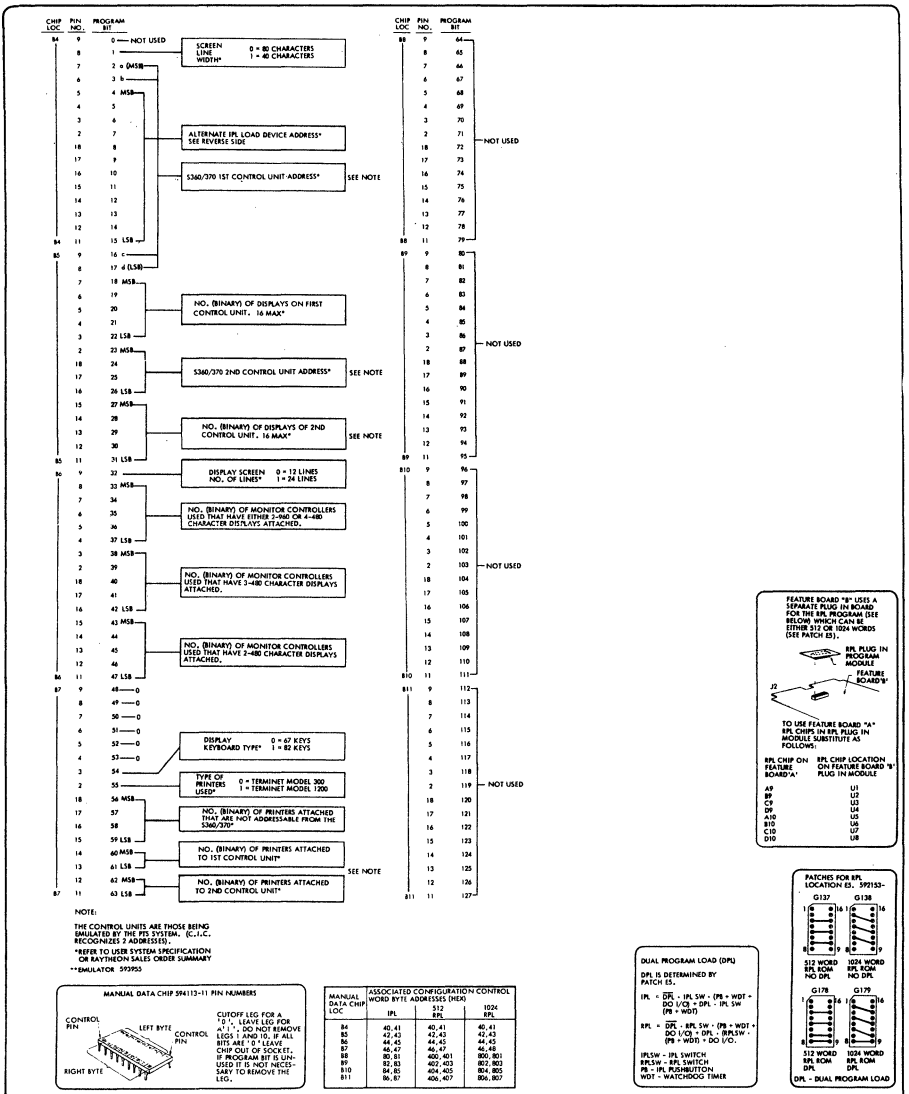


FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

PATCH AND SWITCH SETTINGS FOR LOCAL 2848/2260 EMULATOR FOR VERSION 2 C.I.C. 863034

MARCH 1976
44-8063
Sheet 3 of 3

PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR 2848/2260 LOCAL EMULATOR ** FOR EASTERN AIRLINES–TSO



NOTE:

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*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY

**EMULATOR 593955

MANUAL DATA CHIP 594113-11 PIN NUMBERS

CUTOFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

MANUAL DATA CHIP LOC	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
	IPL	512 RPL	1024 RPL
B4	40,41	40,41	40, 41
B5	42,43	42,43	42,43
B6	44,45	44,45	44,45
B7	46,47	46,47	46,48
B8	80,81	400,401	800, 801
B9	82,83	402,403	802, 803
B10	84,85	404,405	804, 805
B11	86, 87	406,407	806, 807

DUAL PROGRAM LOAD (DPL)

DPL IS DETERMINED BY PATCH E5.

IPL = $\overline{DPL}$ · IPL SW · (PB + WDT + DO I/O) + DPL · IPL SW (PB + WDT)

RPL = $\overline{DPL}$ · RPL SW · (PB + WDT + DO I/O) + DPL · (RPLSW · (PB + WDT) + DO I/O.

IPLSW = IPL SWITCH
RPLSW = RPL SWITCH
PB = IPL PUSHBUTTON
WDT = WATCHDOG TIMER

FEATURE BOARD 'B' USES A SEPARATE PLUG IN BOARD FOR THE RPL PROGRAM (SEE BELOW WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5).

TO USE FEATURE BOARD 'A' RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

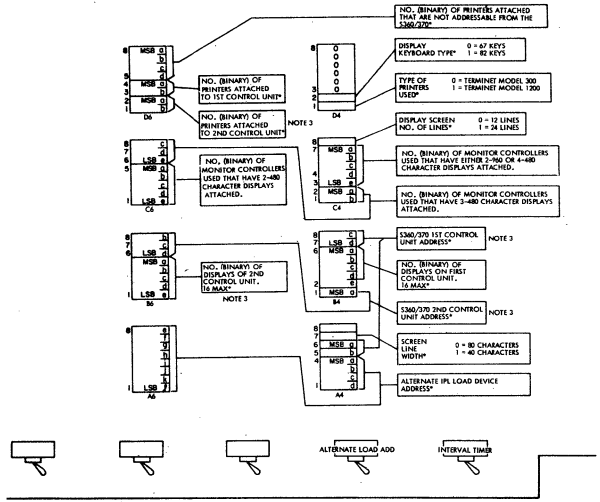
RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATION ON FEATURE BOARD 'B' PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

PATCHES FOR RPL LOCATION E5. 592153-

DPL - DUAL PROGRAM LOAD

FEBRUARY 1975
44-A056
Sheet 1 of 2

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR LOCAL 2848/2260 EMULATOR** FOR EASTERN AIRLINES-TSO



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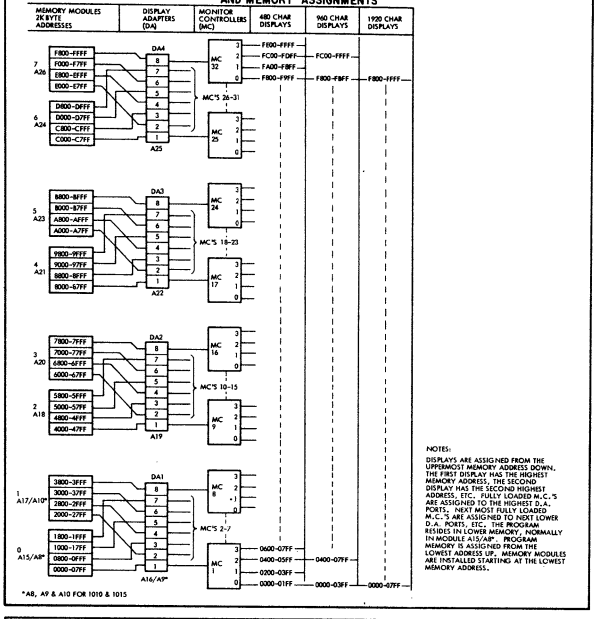
1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1'S.
3. THE CONTROL UNITS ARE THOSE BEING EMULATED BY THE PTS SYSTEM. (C.U.C. RECOGNIZES 2 ADDRESSES).

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY

**EMULATOR 593958

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS

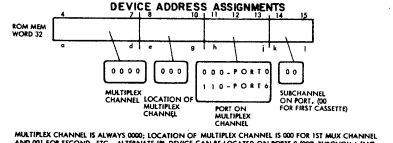


*A8, A9 & A10 FOR 1010 & 1015

NOTES:

DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. FULLY LOADED M.C.'S ARE ASSIGNED TO THE HIGHEST D.A. PORTS; NEXT MOST FULLY LOADED M.C.'S ARE ASSIGNED TO NEXT LOWER D.A. PORTS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A8* PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS

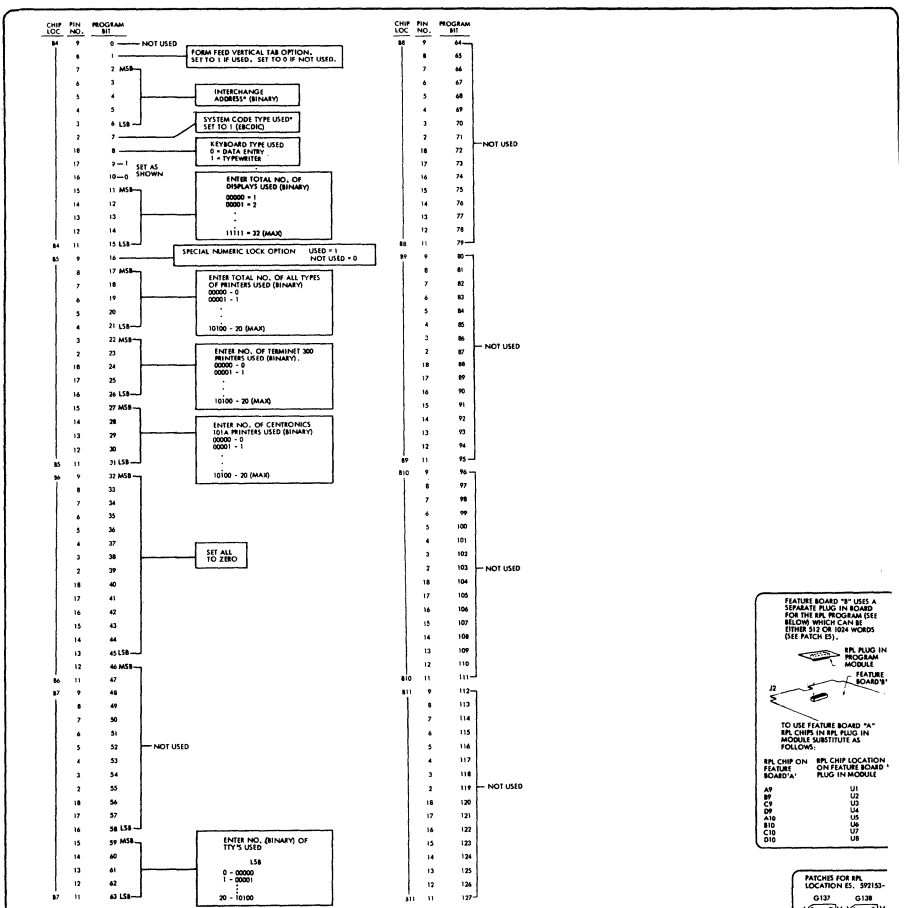


MULTIPLEX CHANNEL PRINTER PORT ASSIGNMENTS

PRINTER NO.	MUX NO.	PORT NO.
1 - 6	0	1-6
7 - 14	1	0-7
15 - 22	2	0-7

MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR CBI RETAIL CREDIT SYSTEM 3270 REMOTE EMULATOR WITH TELETYPE CONCENTRATOR 863008

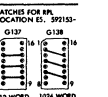


FEATURE BOARD "B" USES A SEPARATE PLUG IN BOARD FOR THIS RPL PROGRAM (SEE BELOW) WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5).

TO USE FEATURE BOARD "A" RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

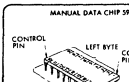
RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATION ON FEATURE BOARD 'B' PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

PATCHES FOR RPL LOCATION E5, 592153-



DPL - DUAL PROGRAM LOA

MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUTOFF LEG FOR A "0", LEAVE LEG FOR A "1". DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE "0" LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

MANUAL DATA CHIP LOC	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX) IPL	512 RPL	1024 RPL
B4	40, 41	40, 41	40, 41
B5	42, 43	42, 43	42, 43
B6	44, 45	44, 45	44, 45
B7	46, 47	46, 47	46, 48
B8	80, 81	400, 401	800, 801
B9	82, 83	402, 403	802, 803
B10	84, 85	404, 405	804, 805
B11	86, 87	406, 407	806, 807

DUAL PROGRAM LOAD (DPL)

DPL IS DETERMINED BY PATCH E5.

IPL = DPL · IPL SW · (PB + WDT + DO I/O) + DPL · IPL SW (PB + WDT).

RPL = DPL · RPL SW · (PB + WDT + DO I/O) + DPL · (RPLSW + (PB + WDT) + DO I/O.

IPLSW - IPL SWITCH
RPLSW - RPL SWITCH
PB - IPL PUSHBUTTON
WDT - WATCHDOG TIMER

OCTOBER

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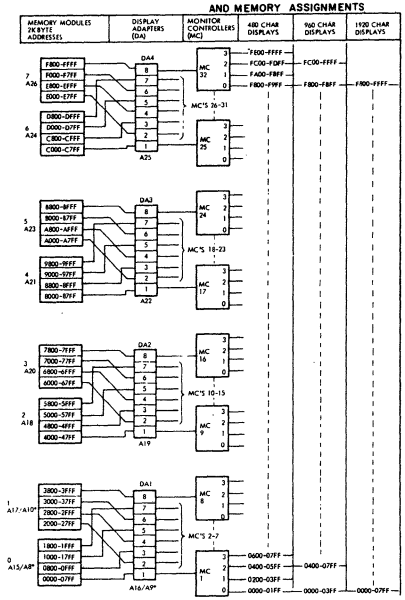
REVISI
Sheet 1

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS

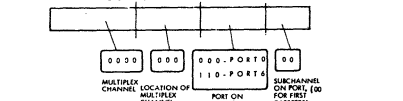


*A8, A9 & A10 FOR 1015 & 1015

NOTES

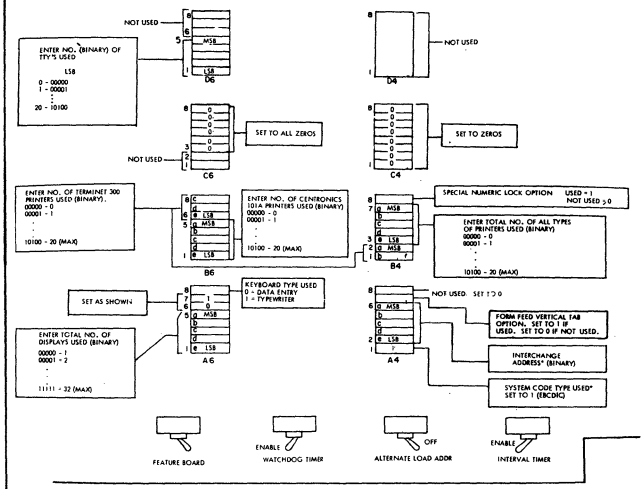
DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. FULLY LOADED M.C.'S ARE ASSIGNED TO THE HIGHEST D.A. PORTS. NEXT MOST FULLY LOADED M.C.'S ARE ASSIGNED TO THE NEXT LOWER D.A. PORTS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULES A17/A10* AND A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

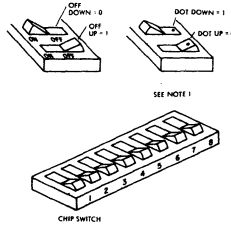
DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000 THROUGH 4 (110) A 'O' ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR CBI RETAIL CREDIT SYSTEM 3270 REMOTE EMULATOR WITH TELETYPE CONCENTRATOR 863008

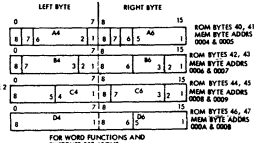




NOTES:

1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1'S.

*REFER TO USER SYSTEM SPECIFICATION OR FOR INTERCHANGE ADDRESS TO PROCESSING UNIT AND TERMINAL ADDRESS ASSIGNMENT TABLE.



MONITOR CONTROLLER C CHARACTER/LINE FORMAT E6 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12	(74)	OPTIONS
1	——	——	——	NOTE 1
2		——	——	NOTE 2
3	OPEN	OPEN	CLOSED	——
4	OPEN	CLOSED	CLOSED	——
5	CLOSED	CLOSED	CLOSED	——
6	CLOSED	OPEN	OPEN	——
7	OPEN	CLOSED	CLOSED	——
8	——	——	——	NOTE 3

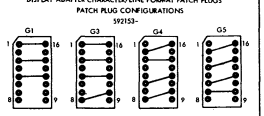
NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS

592153-



FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-) INTO BOARD LOCATIONS D15 AND J16	
80 X 24	G1	G3
80 X 12	G1	G4
40 X 12	G1	G5

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT 0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (READ FROM) IS ASSIGNED TO PORT 1 OF FIRST MULTIPLEX CHANNEL CONTROLLER

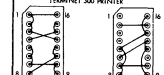
MODEM (WRITE TO) IS ASSIGNED TO PORT 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS.

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MI5-A PATCHES

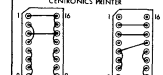
TERMINET 300 PRINTER



592153G98 592153G101

MI5 - BOARD LOCATION - B2

CENTRONICS PRINTER



592153G107 592153G124

MI5 - BOARD LOCATION - B2

NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT 40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5				
6	See Below			
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.

When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.

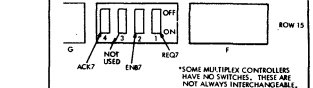
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MULTIPLEX CHANNEL CONTROLLER

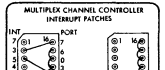
DISABLE/ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



592153G66 592153G68

K1 BOARD LOCATION K1

FIRST MULTIPLEX CHANNEL CONTROLLER

2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEMS SEND	0	2	5
REC	0	1	5
PRINTERS AND TTY'S	0	3-6	2
	1	0-7	2
	2	0-7	2

NOTE: TTY'S ARE ASSIGNED TO THE LOWEST MUX PORTS STARTING WITH MUX 0 PORT 3 AND CONTINUING UNTIL ALL TTY'S HAVE BEEN ASSIGNED. THEN THE PRINTERS ARE ASSIGNED TO THE FOLLOWING MUX PORTS.

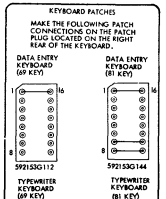
MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 11
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

G2 BOARD LOCATION

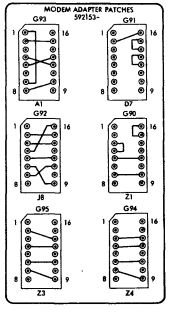
KEYBOARD PATCHES

MAKE THE FOLLOWING PATCH CONNECTIONS ON THE PATCH PLUG LOCATED ON THE RIGHT REAR OF THE KEYBOARD.



MODEM ADAPTER PATCHES

592153-

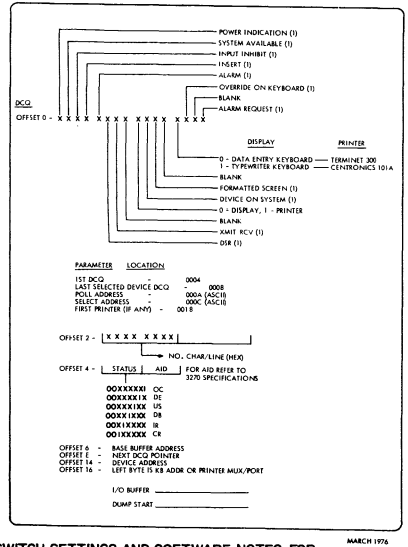


Processing Unit and Terminal Address Assignments

Encode on Feature Board / Processing Unit or Device Number	Column 1 Use this column to find: • Device Selection, • Specific Poll, • General Poll, and • Fixed Return Addresses — EBCDIC Hex	ASCII Hex	Column 2 Use this column to find: • PTS Selection Addresses — EBCDIC Hex	ASCII Hex
D0	40	20	60	2D
D1	C1	41	61	2F
D2	C2	42	E2	53
D3	C3	43	E3	54
D4	C4	44	E4	55
D5	C5	45	E5	56
D6	C6	46	E6	57
D7	C7	47	E7	58
D8	C8	48	E8	59
D9	C9	49	E9	5A
DA	4A	58	6A	2C
DB	4B	68	4B	25
DC	4C	3C	6C	5F
DD	4D	28	6D	3E
DE	4E	2B	6E	3F
DF	4F	21	6F	3A
E0	50	26	F0	30
E1	51	4A	F1	31
E2	52	4B	F2	32
E3	53	4C	F3	33
E4	54	4D	F4	34
E5	55	4E	F5	35
E6	56	4F	F6	36
E7	57	50	F7	37
E8	58	51	F8	38
E9	59	52	F9	39
EA	5A	5D	7A	3A
EB	5B	24	7B	23
EC	5C	2A	7C	40
ED	5D	29	7D	27
EE	5E	3B	7E	3D
EF	5F	5E	7F	22

NOTE

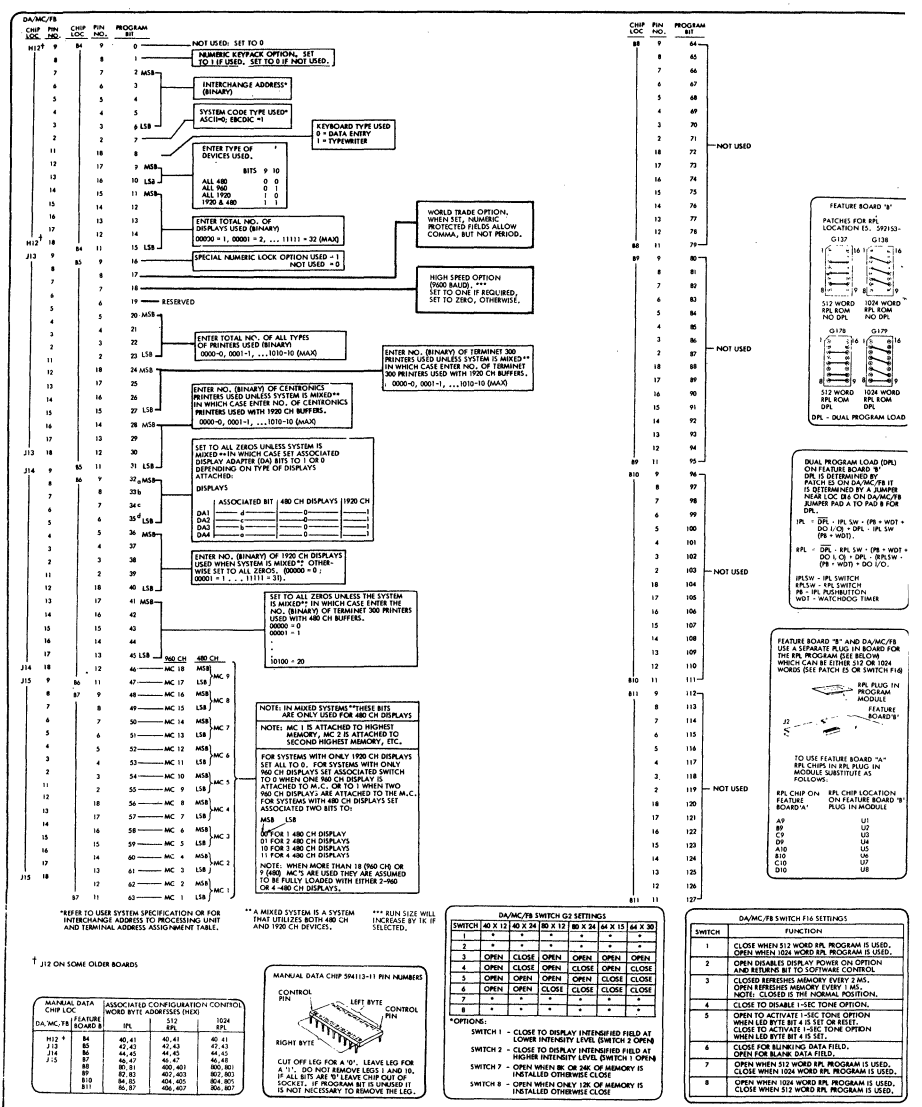
I/O character address 7F is used as the device address to specify a General Poll operation.



PATCH AND SWITCH SETTINGS AND SOFTWARE NOTES FOR CBI RETAIL CREDIT SYSTEM 3270 REMOTE EMULATOR WITH TELEVIDEO CONCENTRATOR

MARCH 1976
44-9065
Sheet 3 of 3

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR 3271 REMOTE EMULATOR 863373



MONITOR CONTROLLER C CHARACTER LINE FORMAT 66 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12	(24)	OPTIONS
1	——	——	——	NOTE 1
2	——	——	——	NOTE 2
3	OPEN	OPEN	CLOSED	——
4	OPEN	CLOSED	CLOSED	——
5	CLOSED	CLOSED	CLOSED	——
6	CLOSED	OPEN	OPEN	——
7	OPEN	CLOSED	CLOSED	——
8	——	——	——	NOTE 3

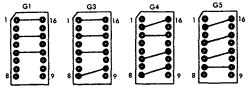
NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS

592153-



FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-) INTO BOARD LOCATIONS D15 AND J16	
80 X 24	G1	G3
80 X 12	G1	G4
40 X 12	G1	G5

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (READ FROM) IS ASSIGNED TO PORT 1 OF FIRST MULTIPLEX CHANNEL CONTROLLER

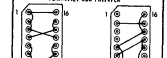
MODEM (WRITE TO) IS ASSIGNED TO PORT 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS.

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MISA PATCHES

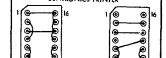
TERMINET 300 PRINTER



592153G98 592153G101

M5 - BOARD LOCATION - B2

CENTRONICS PRINTER



592153G107 592153G124

M5 - BOARD LOCATION - B2

NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E5, E4-E6, E7-E9, E10-E11.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT			
	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5	See Below			
6				
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.

When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip — D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.

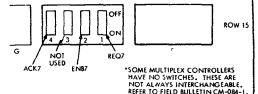
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1; Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MULTIPLEX CHANNEL CONTROLLER

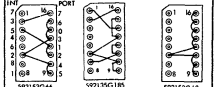
DISABLE ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS K'BOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE K'BOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



592153G66 FOR MODEM INT LEVELS

592153G185 FOR MODEM INT LEVEL 8

FIRST MULTIPLEX CHANNEL CONTROLLER

592153G68 2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEMS			
SEND	0	2	5 OR 8
REC	0	1	5 OR 8
PRINTERS 1-4	0	3-6	2
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2

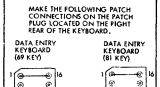
MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

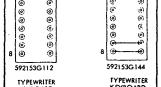
G2 BOARD LOCATION

KEYBOARD PATCHES

MAKE THE FOLLOWING PATCH CONNECTIONS ON THE PATCH PLUG LOCATED ON THE RIGHT REAR OF THE KEYBOARD.



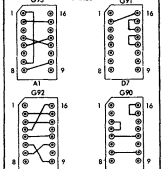
592153G112 592153G144



592153G123 592153G111

MODEM ADAPTER PATCHES

592153-

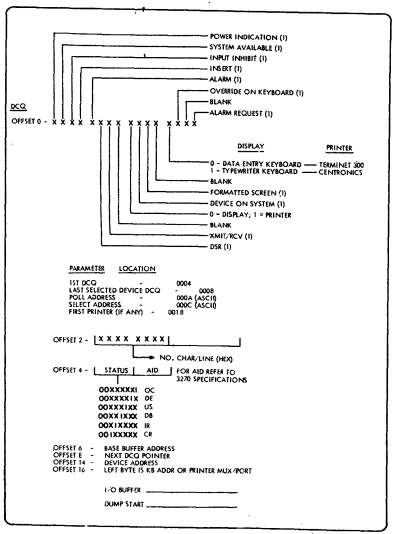


Processing Unit and Terminal Address Assignments

Encode as Feature Board	Column 1 Use this column to find: • Device Selection, • Specific Poll, • General Poll, and • Fixed Return Addresses		Column 2 Use this column to find: • PTS Selection Addresses	
Processing Unit or Device Number	EBCDIC Hex	ASCII Hex	EBCDIC Hex	ASCII Hex
0	40	20	60	2D
1	C1	41	61	2F
2	C2	42	E2	53
3	C3	43	E3	54
4	C4	44	E4	55
5	C5	45	E5	56
6	C6	46	E6	57
7	C7	47	E7	58
8	C8	48	E8	59
9	C9	49	E9	5A
10	4A	5B	6A	5C
11	4B	2E	6B	2C
12	4C	3C	6C	25
13	4D	28	6D	5F
14	4E	2B	6E	3E
15	4F	21	6F	3F
16	50	26	F0	30
17	D1	D1	F1	31
18	D2	48	F2	32
19	D3	4C	F3	33
20	D4	4D	F4	34
21	D5	4E	F5	35
22	D6	4F	F6	36
23	D7	50	F7	37
24	D8	51	F8	38
25	D9	52	F9	39
26	5A	5D	7A	3A
27	5B	24	7B	23
28	5C	2A	7C	40
29	5D	29	7D	27
30	5E	3B	7E	3D
31	5F	5E	7F	22

NOTE

I/O character address 7F is used on the device address to specify a General Poll operation.

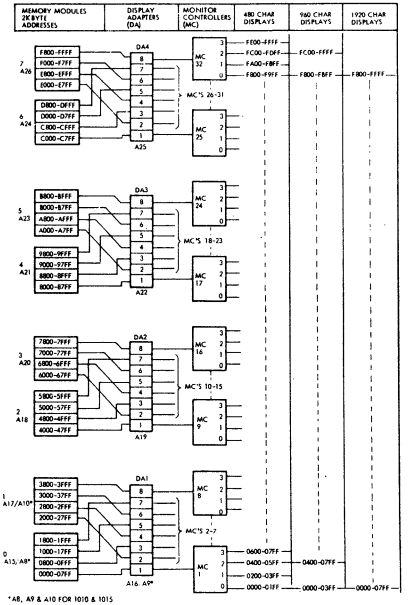


REV. MARCH 1978

64-8099

PATCH AND SWITCH SETTINGS AND SOFTWARE NOTES FOR 3271 REMOTE EMULATOR

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, A9 & A10 FOR 1010 & 1015

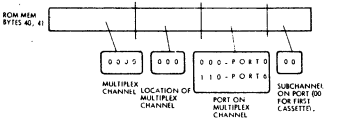
NOTES

ALL DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. IN A MIXED SYSTEM 1920 CH DISPLAYS ARE ASSIGNED BEFORE 480 CH DISPLAYS. ALSO THE STARTING MEMORY ADDRESSES ARE DETERMINED BY WHICH DISPLAY ADAPTERS ARE ASSIGNED TO 1920 CH AND 480 CH DISPLAYS (SEE C4 ON F.B.'A'). IF A SYSTEM IS MIXED OR DOES NOT FULLY LOAD ALL M.C.'s, PRINTER BUFFERS WILL BE ASSIGNED TO THE UNUSED AREAS. IN A MIXED ** SYSTEM PRINTERS ARE ASSIGNED AS FOLLOWS:

1 CENTRONICS - 1920 CH BUFFER
2 TERMINET - 1920 CH BUFFER
3 CENTRONICS - 480 CH BUFFER
4 TERMINET - 480 CH BUFFER

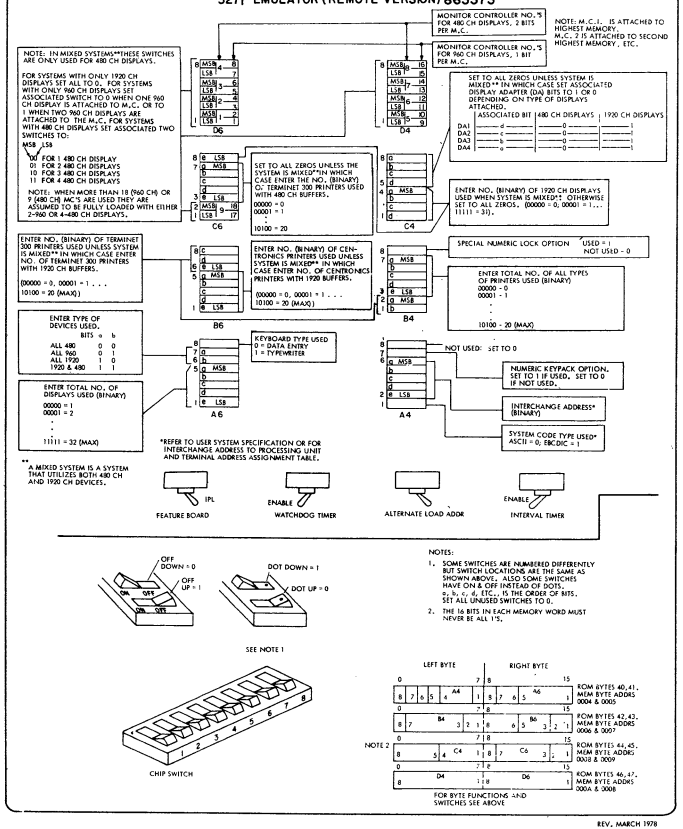
THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULES A17/A10* AND A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

DEVICE ADDRESS ASSIGNMENTS



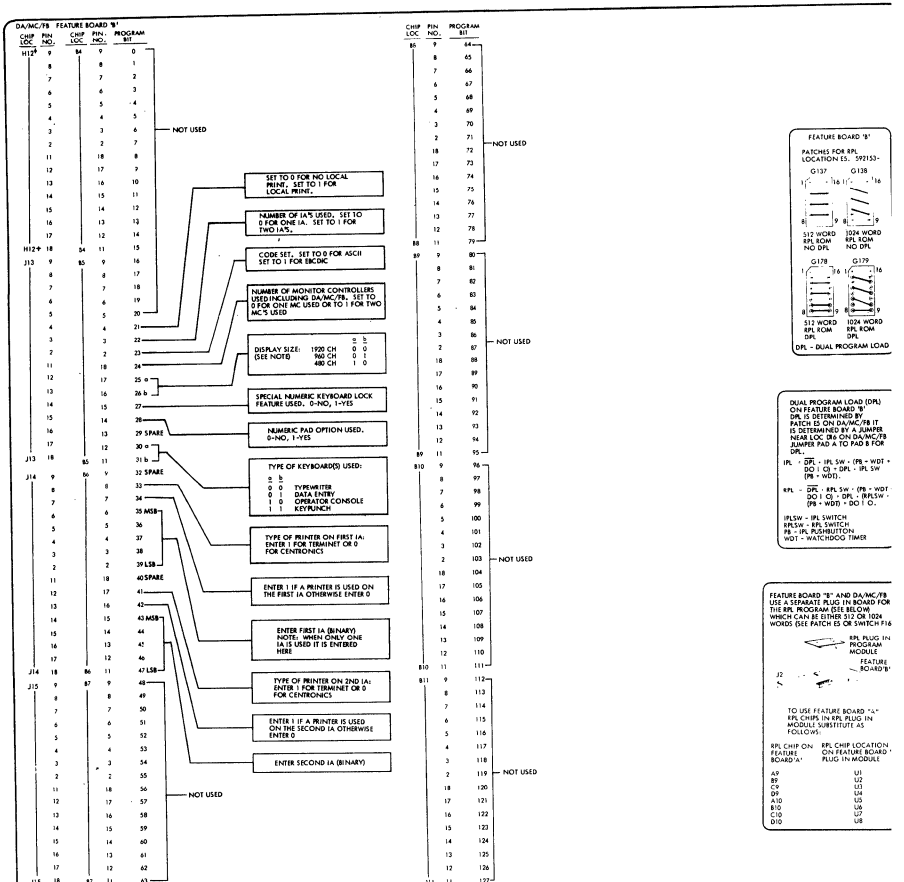
MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC., ALTERNATE I/O DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR 3271 EMULATOR (REMOTE VERSION) 863373



REV. MARCH 1978

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR THE 3275 REMOTE EMULATOR 863177



MARCH 1
44-809
Sheet 1

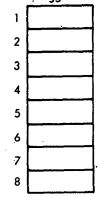
FOR THESE PRINTERS INSERT THESE PATCHES* INTO THESE IOC LOCATIONS		TERMINET 300 BAUD	TERMINET 1200 BAUD	TTY 50 BAUD	TTY 75 BAUD	TTY 110 BAUD	BOARDING PASS AND TICKET PRINTERS (VOGUE/DI/AN)	CENTRONICS PRINT SUB CHAR MODE	EXTEL PRINTER AR-11	VASP SIEMENS TTY-100	COSSOR 135 BAUD (NO EOR, 6-BIT NO PAR)	BRAATHENS TTY FD MODEL B2	EXTEL PRINTER 165 BAUD	CENTRONICS REMOTE 1200 BAUD
		WITH EOR												
PRINTER INTERFACE RATE	C2	G203	G204	G197	G198	G199	G205	G205	G201	G197	G200	G198	G202	G204
PRINTER INTERFACE MODE	C5	G206	G206	G207	G207	G207	G208	G209	G206	G210	G211	G212	G213	G216

FOR THESE EMULATORS INSERT THESE PATCHES* INTO THESE IOC LOCATIONS	3270 REMOTE 3271	IPARS	3275	UNI-SCOPE	PATCH FUNCTION
L1	G191	G190	G191	G189	INTERRUPT LEVELS
L15	G188	G187	G188	G188	DEVICE ADDRESSES
B13	G192	G192	G192	G192	MODEM MODE**
B15	G196	G196	G196	G196	MODEM BAUD RATE (4800) USED ONLY FOR LOOPBACK TESTING

*592153G-

**SYNCHRONOUS, FULL DUPLEX, EXT CLOCK
DATA SET READY CONNECTED TO RX
MODEM READY.

CHIP SWITCH J5



FOR THESE EMULATORS	SET SWITCHES 1	2	3	4
3271/3275	CLOSE	OPEN	CLOSE	
IPARS	OPEN	CLOSE	OPEN	

SET SWITCH	FOR IOC ADDRESS
CLOSE 8	0
CLOSE 7	1
CLOSE 6	2
CLOSE 5	3

IOC PATCH AND SWITCH SETTINGS

DEVICE	INTERRUPT LEVELS FOR EMULATOR – 3271	IPARS	3275	UNISCOPE
TX MODEM	8	4	8	5
RX MODEM	8	5	8	5
PRINTER	2	2	2	2
KEYBOARD	3	3	3	3

STD DEVICE ADDRESSES FOR EMULATORS

DEVICE	3271	IPARS	3275	UNISCOPE
CASSETTE	0	0	0	0
RX MODEM	1	4	1	1
TX MODEM	2	5	2	2
PRINTER	3	1	3	3
KEYBOARD	7	7	7	7

NOTE:

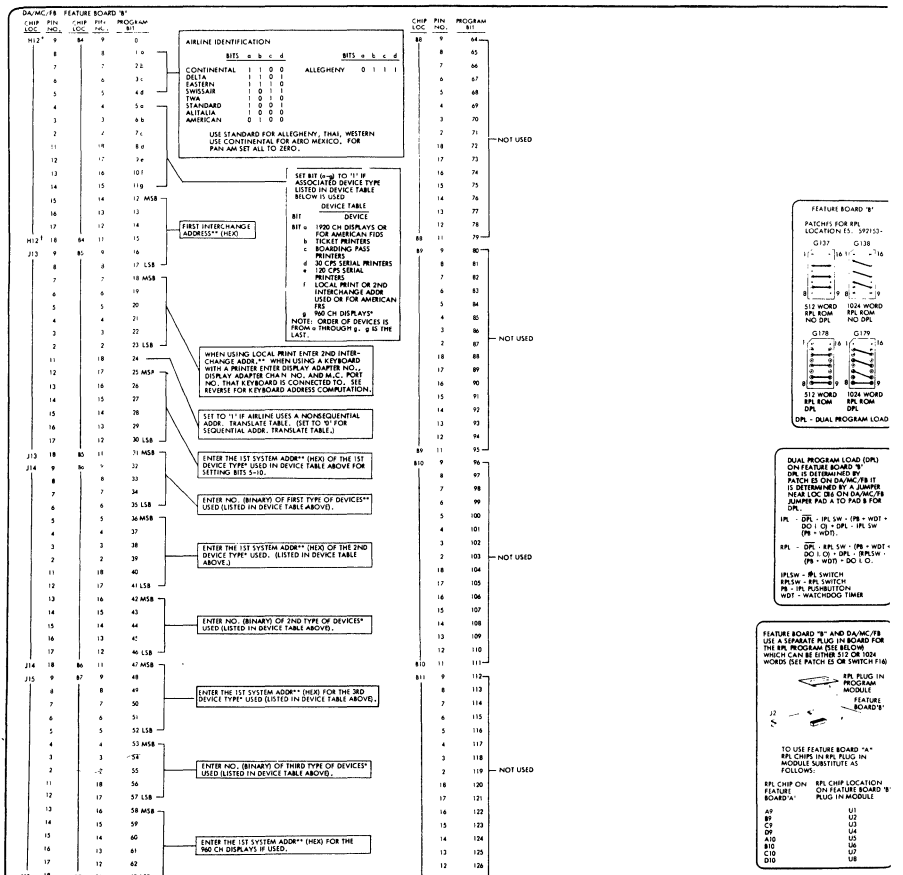
FOR OTHER PATCH AND SWITCH SETTINGS AND SOFTWARE NOTES REFER TO 3271 EMULATOR 44-8098

AUGUST 1975

44-8099
Sheet 2 of 2

PATCH AND SWITCH SETTINGS FOR 3275 REMOTE EMULATOR

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR PARS/IPARS EMULATOR USING THE INITIALIZATION PROGRAM ***



*960 CH DISPLAY ADDR IS ALWAYS ONLY ENTERED IN BITS 58-63.

**REFER TO USER SYSTEM SPECIFICATION OR CONFIGURATION EXAMPLE FOR ADDR (4 HEX) ENTER MSB 01 0100

***FOR PROGRAM 593822 AND FOR AMERICAN AIRLINES 863028 ALSO FOR PAN AM 863081

† J12 IS ON SOME OLDER BOARDS

MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA/MC/FB	FEATURE BOARD 'B'	IPL	512 RPL	1024 RPL
H12 †	B4	40, 41	40, 41	40, 41
J13	B5	42, 43	42, 43	42, 43
J14	B6	44, 45	44, 45	44, 45
J15	B7	46, 47	46, 47	46, 48
	B8	80, 81	400, 401	800, 801
	B9	82, 83	402, 403	802, 803
	B10	84, 85	404, 405	804, 805
	B11	86, 87	406, 407	806, 807

MANUAL DATA CHIP 594113-11 PIN NUMBERS

CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

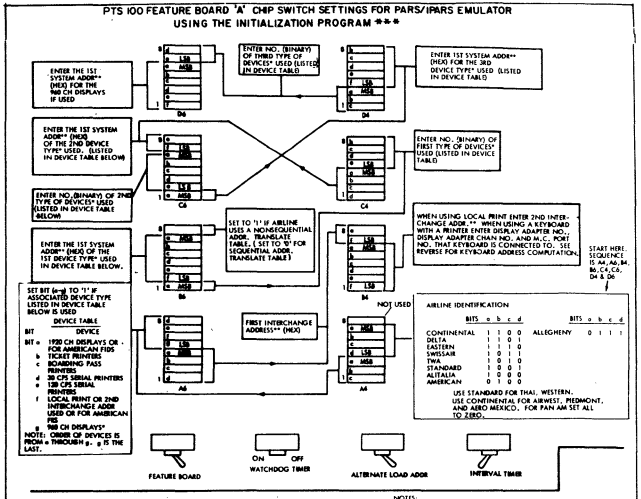
SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

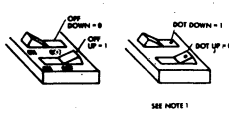
*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

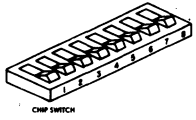
DA/MC FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT # 15 SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT # 15 SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

PTS 100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR PARS/IPARS EMULATOR USING THE INITIALIZATION PROGRAM ***



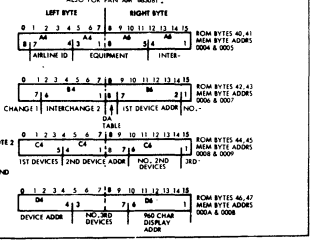


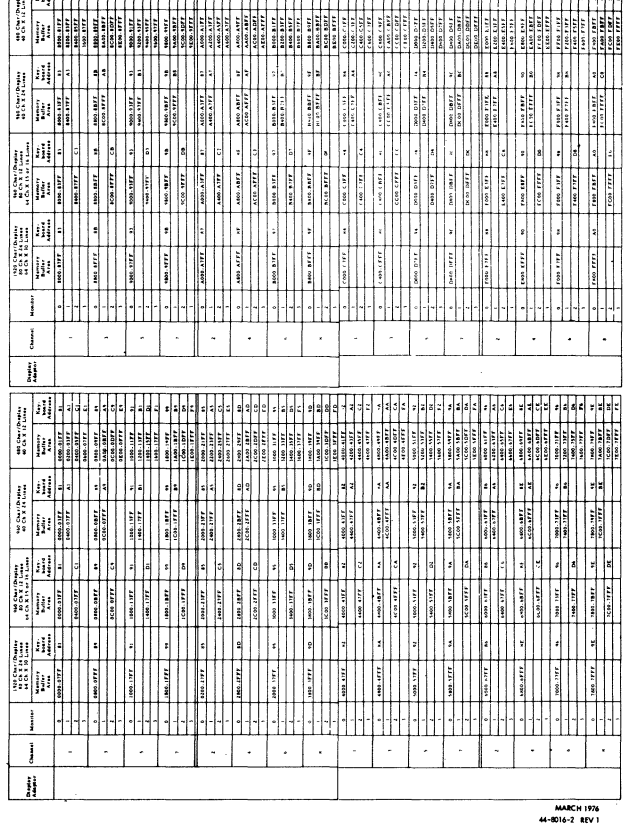


NOTES:

1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. **THE L6 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1'S.**960 CH DISPLAY ADDR IS ALWAYS ONLY ENTERED IN SWITCH D6 1-6.**REFER TO USER SYSTEM SPECIFICATION OR CONFIGURATION EXAMPLE FOR ADDR 14 (HEX) ENTER 01 0100 ab cdef

*** FOR 593822 AND FOR AMERICAN AIRLINES 863028. ALSO FOR PAN AM 863081 .





MARCH 1976
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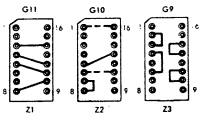
Sheet 2 of 4

SERIAL ADAPTER PATCHING

PATCH PLUGS 592153-

FULL DUPLEX - TTY

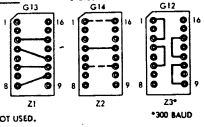
INSERT THESE PATCH PLUGS INTO LOCATIONS Z1, Z2 & Z3 ON THE SERIAL ADAPTER 591558-



PATCH PLUGS 592153-

HALF-DUPLEX - TTY & SERIAL PRINTER

INSERT THESE PATCH PLUGS INTO LOCATIONS Z1, Z2 & Z3 ON THE SERIAL ADAPTER 591558-



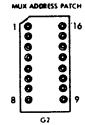
*300 BAUD

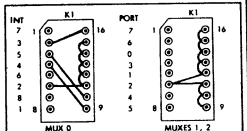
---- INSTALLED BUT NOT USED.

MULTIPLEX CHANNEL CONTROLLER KEYBOARD, INTERRUPT AND ADDRESS PATCHES

INTERRUPT PATCHES

MUX ADDRESS PATCH

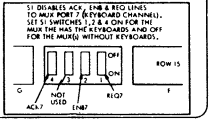




*ADDRESS OF MUX CHAN.

1 OR 4 TO 16 - ADDR 000
1 OR 4 TO 12 - ADDR 001
1 OR 4 TO 14 - ADDR 010
1 OR 4 TO 10 - ADDR 011
1 OR 4 TO 15 - ADDR 100
1 OR 4 TO 11 - ADDR 101
1 OR 4 TO 13 - ADDR 110
1 OR 4 TO 9 - ADDR 111

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 & 4 ON FOR THE MUX THE HAS THE KEYBOARDS AND OFF FOR THE MUX(S) WITHOUT KEYBOARDS.



WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT INSERT SCREW(S) INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT						
	0	1	2	3	4	5	6 7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1, 17 33	2, 18 34	3, 19 35	4, 20 36	5, 21 37	6, 22 38	7, 23 39 8, 24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9, 25 41	10, 26 42	11, 27 43	12, 28 44	13, 29 45	14, 30 46	15, 31 16, 32 47 48

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MOTHERBOARD SCREW SWITCH SETTINGS

MONITOR CONTROLLER* CHARACTER/LINE FORMAT E6 SWITCH SETTINGS**

E6 CHIP SWITCH SETTING	64 CHAR. 15 LINES	64 CHAR. 16 LINES	64 CHAR. 30 LINES
E6-1	OPEN	OPEN	OPEN
E6-2	OPEN	CLOSED	OPEN
E6-3	OPEN	OPEN	CLOSED
E6-4	CLOSED	CLOSED	CLOSED
E6-5	OPEN	OPEN	OPEN
E6-6	OPEN	OPEN	OPEN
E6-7	CLOSED	CLOSED	CLOSED
E6-8*	OPEN	CLOSED	OPEN

*8 MODIFIED BOARD,

**CLOSED = 1; OPEN = 0, SEE FEATURE BOARD SWITCH SETTING PROCEDURE

+ USED ON SOME M.C.'S (USED ON ALL 16 LINE M.C.'S)

IPARS MODEM ADAPTER PATCHES

INSERT THESE PATCH PLUGS INTO BOARD LOCATIONS E5 AND J3

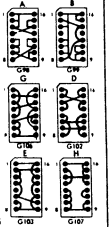
592153G25 592153G27

IPARS SYSTEM CONFIGURATION VARIABLE PATCHES, SWITCHES AND REMOTE PRINTER ADDRESSES

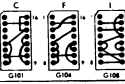
MULTI-INTERFACE SERIAL ADAPTER (MISA) PATCHING (592153-)

INSERT THESE FOR THIS MODEL MISA 59329A-	PLUGS INTO A5	PLUGS INTO B2
G1 TERMINET 300 BAUD	A	C
G3 TERMINET 1200 BAUD	B	C
G5 TTY 110 BAUD	G	F
G7 TTY 50 BAUD	D	F
G9 TTY 75 BAUD	E	F
G11 TICKET & BOARDING PASS PRINTER	H	I

A5 PATCH CONFIGURATIONS (BAUD RATES)



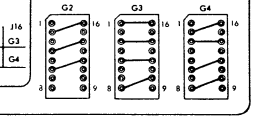
B2 PATCH CONFIGURATIONS (CONTROL)



DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

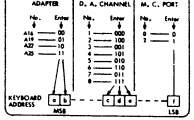
FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-) D15	J16
64 X 30 SPLIT SCREEN	G2	G3
64 X 15 OR 16	G2	G4

PATCH PLUG CONFIGURATIONS 592153-



KEYBOARD ADDRESS COMPUTATION

KEYBOARD CONNECTED:



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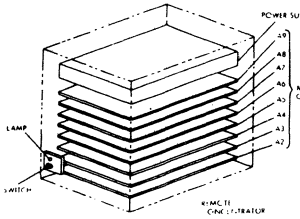
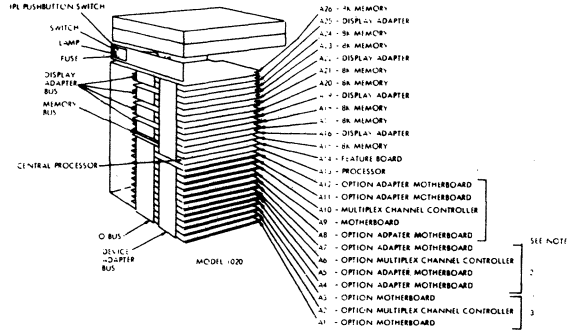
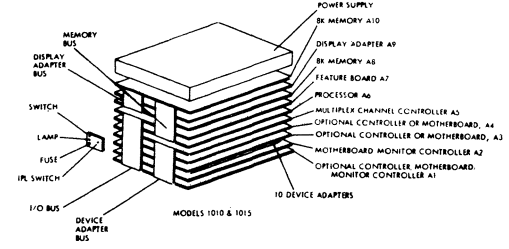


POWER SUPPLIES





NOTE:
MONITOR CONTROLLERS ARE INSTALLED IN SLOTS A1, A2, A3 & A4 WHEN ONLY 2 MULTIPLEX CONTROLLERS ARE USED. MONITOR CONTROLLERS ARE INSTALLED IN A7, A8 & A9 WHEN 3 MULTIPLEX CONTROLLERS ARE USED.

COMMUNICATIONS REGION TABLE

LOAD SIZE OF PROGRAM
KEYBOARD MODULE
SECOND HALF OF INITIALIZER
TASK SUPERVISOR
PRINTER INITIALIZER
SERIAL PRINTER ROUTINE
TICKET & BOARDING PASS PRINTERS INITIALIZER
PRINTER STATUS TABLES
DISPLAY STATUS TABLES
NUMBER OF DISPLAYS
NUMBER OF PRINTERS
CCC COUNTER
NUMBER OF MESSAGES RECEIVED
NUMBER OF MESSAGES TRANSMITTED
EOMC'S IN TKT AND BOARDING PASS MESSAGES
DATA LOST COUNTER
CARRIER LOST COUNTER
IOCQ'S FOR DISPLAYS
IOCQ'S FOR PRINTERS
OUTPUT - TO HOST - BUFFER
VALID TERMINAL ADDRESSES
VALID PRINTER ADDRESSES
AIRLINE ID
INTERCHANGE 1
INTERCHANGE 2
LOCATION 0010 CONTAINS THE ADDRESS OF THIS TABLE

LED MEMORY BUFFER ASSIGNMENTS

Adapter	Channel	1920 Character Display	960 Character Display		480 Character Display			
			Mon. 0	Mon. 1	Mon. 0	Mon.	Mon.	Mon. 3
1	1	07B0	03C0	07C0	01E0	03E0	05E0	07E0
	2	27B0	23C0	27C0	21E0	23E0	25E0	27E0
	3	0FB0	0BC0	0FC0	09E0	0BE0	0DE0	0FE0
	4	2FB0	2BC0	2FC0	29E0	2BE0	2DE0	2FE0
	5	17B0	13C0	17C0	11E0	13E0	15E0	17E0
	6	37B0	33C0	37C0	31E0	33E0	35E0	37E0
	7	1FB0	1BC0	1FC0	19D0	1BE0	1DE0	1FE0
	8	3FB0	3BC0	3FC0	39E0	3BE0	3DE0	3FE0
2	1	47B0	43C0	47C0	41E0	43E0	45E0	47E0
	2	67B0	63C0	67C0	61E0	63E0	65E0	67E0
	3	4FB0	43C0	4FC0	49E0	4BE0	4DE0	4FE0
	4	6FB0	6BC0	6FC0	69E0	6BE0	6DE0	6FE0
	5	57B0	53C0	57C0	51E0	53E0	55E0	57E0
	6	77B0	73C0	77C0	71E0	73E0	75E0	77E0
	7	5FB0	5BC0	5FC0	59E0	5BE0	5DE0	5FE0
	8	7FB0	7BC0	7FC0	79E0	7BE0	7DE0	7FE0
3	1	87B0	83C0	87C0	81E0	83E0	85E0	87E0
	2	A7B0	A3C0	A7C0	A1E0	A3E0	A5E0	A7E0
	3	8FB0	8BC0	8FC0	89E0	8BE0	8DE0	8FE0
	4	AFB0	ABC0	AFC0	A9E0	ABE0	ADE0	AFE0
	5	97B0	93C0	97C0	91E0	93E0	95E0	97E0
	6	B7B0	B3C0	B7C0	B1E0	B3E0	B5E0	B7E0
	7	9FB0	9BC0	9FC0	99E0	9BE0	9DE0	9FE0
	8	BFB0	BBC0	BFC0	B9E0	BBE0	BDC0	BFE0
4	1	C7B0	C3C0	C7C0	C1E0	C3E0	C5E0	C7E0
	2	E7B0	E3C0	E7C0	E1E0	E3E0	E5E0	E7E0
	3	CFB0	CBC0	CFC0	C9E0	CBE0	CDE0	CFE0
	4	EFB0	EBC0	EFC0	E9E0	EBE0	EDE0	EFE0
	5	D7B0	D3C0	D7C0	D1E0	D3E0	D5E0	D7E0
	6	F7B0	F3C0	F7C0	F1E0	F3E0	F5E0	F7E0
	7	DFB0	DBC0	D7C0	D9E0	DBE0	DDE0	DFE0
	8	FFB0	FBC0	FFC0	F9E0	FBE0	FDE0	FFE0

IPARS SYSTEM CONFIGURATION

CUSTOMER _____ LOCATION _____ LINE ADDRESS _____ INTERCHANGE ADDRESS _____ RDS SYSTEM NO. _____

DEVICE LOCATION NO.	TYPE (1)	SYS ADDR	INT LEVEL (2)	CABLE LENGTH (FEET)	MOTHERBOARD DEVICE ADAPTER	MOTHERBOARD SCREW SWITCH SETTING	MOTHERBOARD SLOT
	CASSETTE		2			1,17,33	0
	MODEM RX		5			13,29,45	4
	MODEM TX		4			6,22,38	5
	KEYBOARDS			NOTE 7	N/A	N/A	N/A 7

CONTROLLERS: PORT / SLOT / I/O BUS ADDR (4)

- #0 MULTIPLEX CHANNEL CONTROLLER A10 A5* — 0000 000
- #1 MULTIPLEX CHANNEL CONTROLLER A6** — 0000 001
- #2 MULTIPLEX CHANNEL CONTROLLER A2** — 0000 010

MEMORY MODULE 2K BYTE ADDRS / DISPLAY ADAPTER / CABLE LENGTH (FEET)

- 7 A26** / 6 A24** / 5 A23** — SEE SUPPLEMENTAL SHEET 44-8017-2 WHEN MORE THAN 48K MEMORY
- 4 A21**: B800-BFFF, B000-B7FF, A800-AFFF, A000-A7FF; 9800-9FFF, 9000-97FF, 8800-8FFF, 8000-87FF — A22
- 3 A20**: 7800-7FFF, 7000-77FF, 6800-6FFF, 6000-67FF; 5800-5FFF, 5000-57FF, 4800-4FFF, 4000-47FF — A19
- 2 A18: 3800-3FFF, 3000-37FF, 2800-2FFF, 2000-27FF, 1800-1FFF, 1000-17FF, 0800-0FFF, 0000-07FF
- 1 A17/A10* — 0 A15/A8* — A16/A9*

MONITOR CONTROLLER: LOCATION REMOTE CONCENTRATOR OR PROCESSING UNIT / SLOT / M.C. PORT (5,6) / CABLE LENGTH (FEET)

DISPLAY (6): SYS ADDR / RELATED DEVICE NO. / LOCATION

SIMPLIFIED MEMORY MAP

- (6) — DISPLAY DATA
- UNUSED
- PRINTER PROGRAM — PRINTER BUFFERS
- 1FFF 8K 0000 — BASIC PROGRAM

NOTES

1. DEVICES AND THEIR SYSTEM ADDRESSES ARE ASSIGNED SEQUENTIALLY FROM THE TOP OF THE PAGE DOWN. ALL UPPER PORTS MUST BE OCCUPIED BEFORE ADDING OTHER DEVICES. THE CASSETTE, MODEM AND KEYBOARD ASSIGNMENTS ARE FIXED. THE ORDER OF OTHER DEVICE ASSIGNMENTS MUST ALWAYS BE: ALL TICKET PRINTERS FIRST; ALL BOARDING PASS PRINTERS SECOND; ALL 30 CPS SERIAL PRINTERS THIRD; AND ALL 120 CPS SERIAL PRINTERS LAST.
2. REFER TO THE INTERRUPT LEVEL PATCHING. ALL PRINTERS ARE CONNECTED TO INTERRUPT LEVEL 2.
3. REFER TO THE MOTHERBOARD SCREW SWITCH SETTINGS FOR EACH MUX CHANNEL PORT.
4. DEVICE ADDRESS ASSIGNMENTS

MULTIPLEX CHANNEL	LOC. OF MULTIPLEX CHANNEL CONT.	PORT ON MUX CH. (000-1st; 111-Last)	SUB CHANNEL ON PORT (00-1st; 11-Last)
0000	000	XXX	XX

5. FOR MONITOR CONTROLLER PORT 0 USE CONNECTORS X2 (KEYBOARD), X6 (DISPLAY) & X10 (LED PANEL). FOR MONITOR CONTROLLER PORT 2 USE CONNECTORS X4 (KEYBOARD), X8 (DISPLAY) & X12 (LED PANEL). FOR 1920 CHARACTER SPLIT SCREEN DISPLAY USE CONNECTORS X6 (DISPLAY) X2 & X3 (KEYBOARDS) AND X10 AND X11 (LEDS) (ALSO ON MC A JUMPER IS MADE BETWEEN X12 AND X7.
6. DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS. 960 CHARACTER DISPLAYS USE M.C. PORTS 2 AND 0. 1920 CHARACTER DISPLAYS USE ONLY PORTS 0. SPLIT SCREEN 1920 CHARACTER DISPLAYS USE BOTH PORTS. ALL MONITOR CONTROLLER PORTS (0 AND 2) MUST BE ASSIGNED SYSTEM ADDRESSES WHETHER USED OR NOT, EXCEPT FOR PORT 0 OF LOWEST NUMBERED MONITOR CONTROLLER USED.
7. SAME AS ASSOCIATED DISPLAY CABLE.

† REMOTE CONCENTRATOR USED WITH MORE THAN ONE PTS SYSTEM, ⊕ REQUIRES A DISPLAY EXPANSION MODULE.

* 1010 & 1015

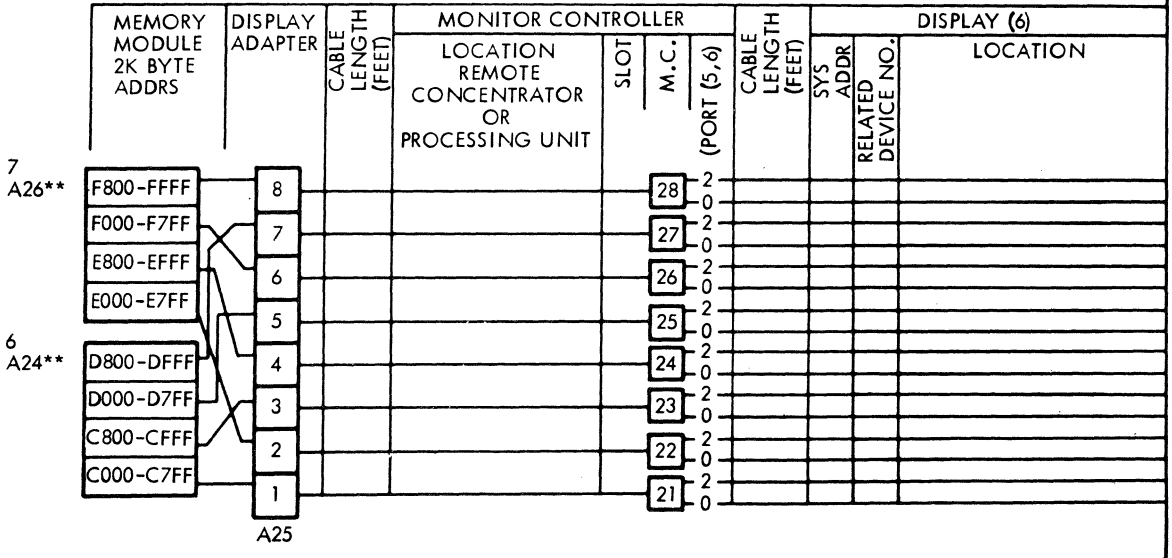
** A MEMORY EXPANSION P.S. MODULE REQUIRED WHEN ITEM IS USED.

IPARS SYSTEM CONFIGURATION

SUPPLEMENTAL SHEET

CUSTOMER _____ LOCATION _____

INTERCHANGE ADDRESS _____ RDS SYSTEM NO. _____ LINE ADDRESS _____



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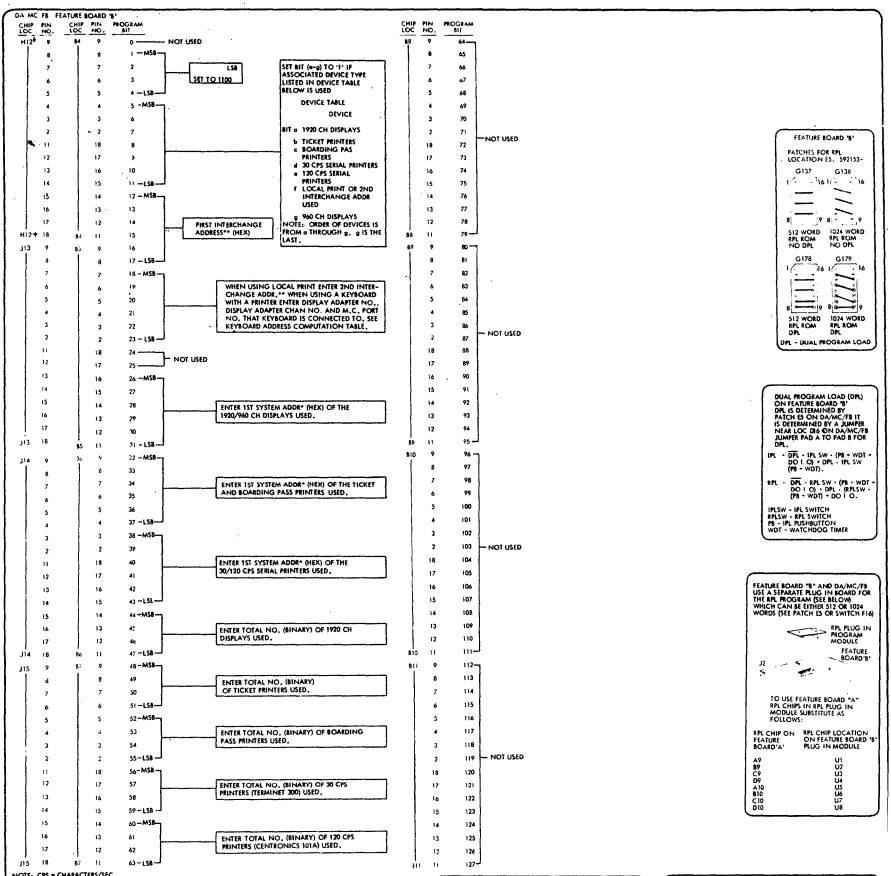
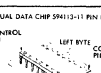
Sheet 2 of 2

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR CONTINENTAL AIRLINES SPECIAL EMULATOR 593822-19



MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA MC/FB	FEATURE BOARD B	IPL	512 RPL	1024 RPL
H12 *	B4	40, 41	40, 41	40, 41
J12	B5	42, 43	42, 43	42, 43
J14	B6	44, 45	44, 45	44, 45
J15	B7	46, 47	46, 47	46, 47
	B8	3C, 3I	400, 401	800, 801
	B9	3E, 3J	402, 403	802, 803
	B10	B4, B5	404, 405	804, 805
	B11	B6, B7	406, 407	806, 807

MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

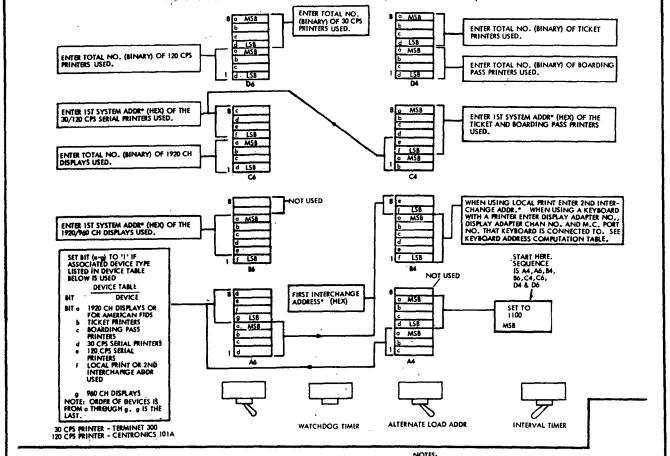
SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED, OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLANKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED, CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED, CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR CONTINENTAL AIRLINES SPECIAL EMULATOR 593822-19

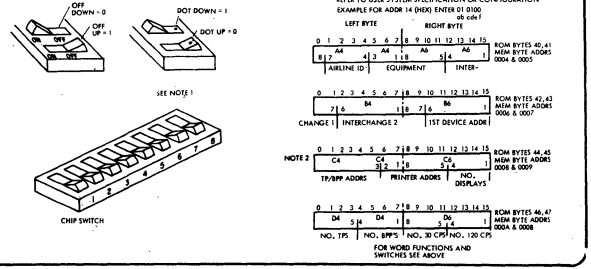


NOTES:

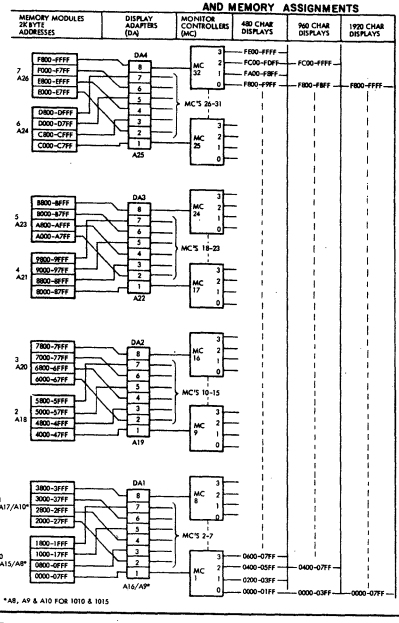
1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1's.
3. FOR OTHER SWITCH SETTING AND PATCHES USE STANDARD IPARS /PARS (44-8016).

*REFER TO USER SYSTEM SPECIFICATION OR CONFIGURATION

EXAMPLE FOR ADDR 14 (HEX) ENTER 01 0100 on side f



DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS

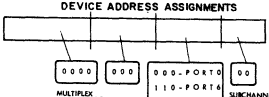


*A8, A9 & A10 FOR 1010 & 1015

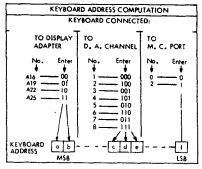
NOTES

DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A9*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110), AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).



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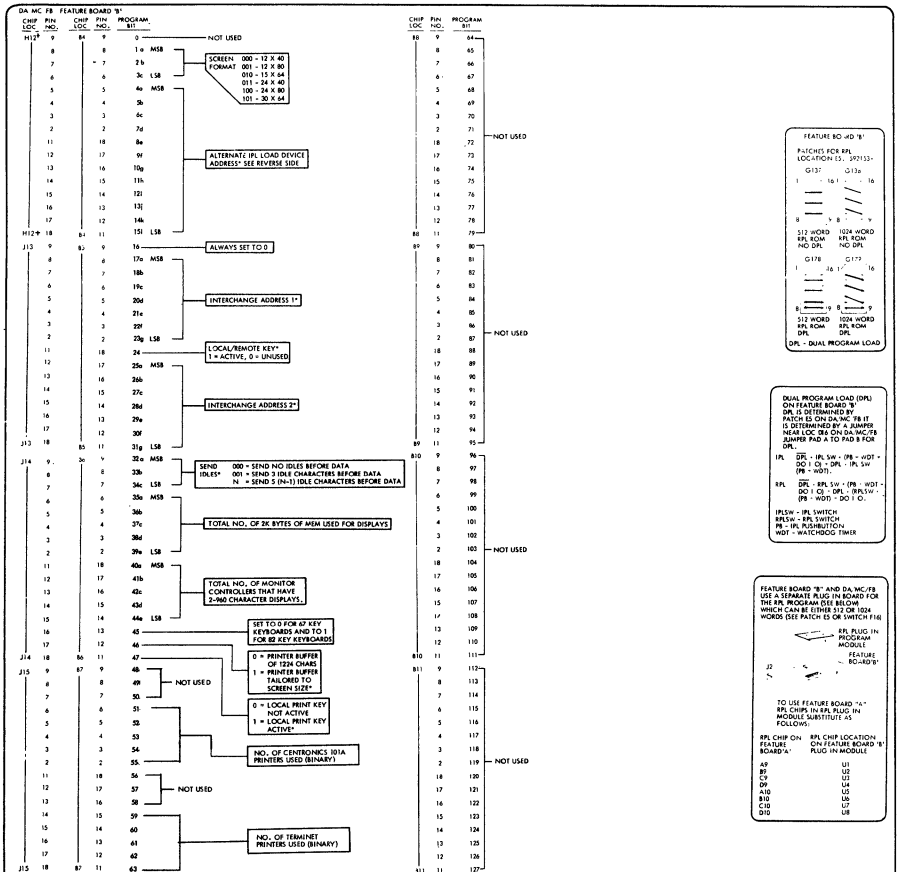
PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR REMOTE 2848/2260 EMULATOR 933057 FOR CONTINENTAL AIRLINES (SUPPORTS 20 PRINTERS)



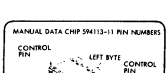
*REFER TO USER SYSTEM SPECIFICATION OR BAYTHEON SALES ORDER SUMMARY

**THE TOTAL NUMBER OF BOTH TYPES OF PRINTERS CANNOT EXCEED 12.

† J12 ON SOME OLDER BOARDS

MANUAL DATA CHIP LOC DA/MC/FB	FEATURE BOARD B	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX) IPL	512 RPL	1024 RPL
H12 †	B4	40,41	40,41	40,41
J13	B5	42,43	42,43	42,43
J14	B6	44,45	44,45	44,45
J15	B7	46,47	46,47	46,48
	B8	80, B1	400, 401	B00, B01
	B9	B2, B3	402, 403	B03, B03
	B10	B4, B5	404, 405	B04, B05
	B11	B6, B7	406, 407	B06, B07

MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

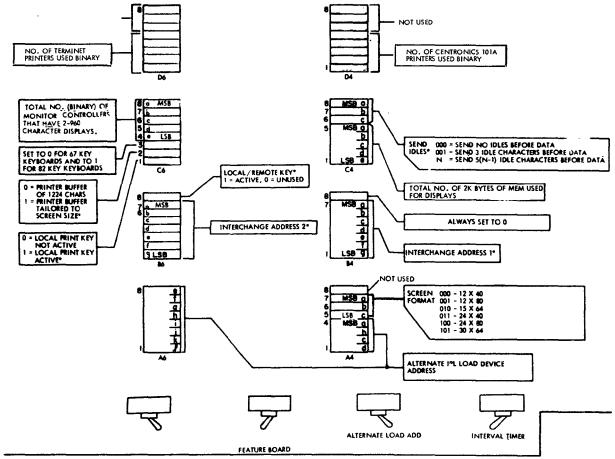
SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

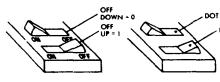
*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

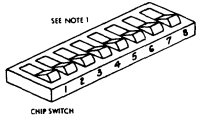
DA/MC FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RESTARTS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT #15 SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT #15 SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR REMOTE 2848/2260 EMULATOR 933057 FOR CONTINETAL AIRLINES (SUPPORTS 20 PRINTERS)





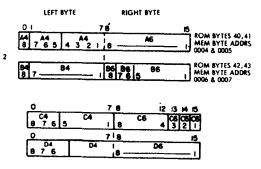


NOTES:

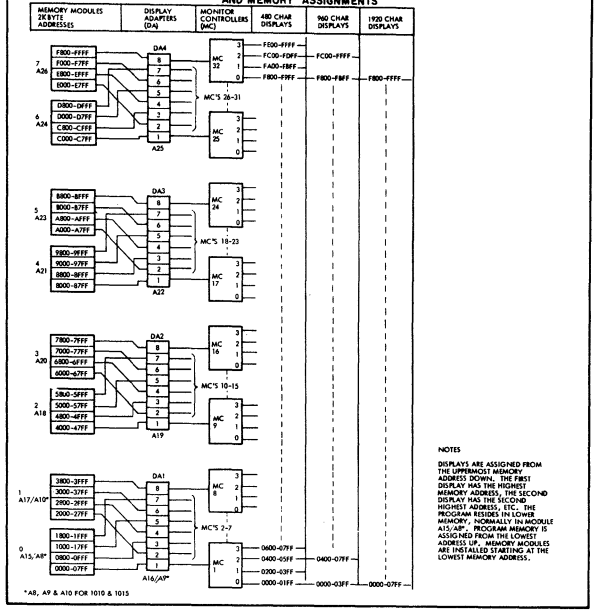
1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1'S.

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY

**THE TOTAL NUMBER OF BOTH TYPES OF PRINTERS CANNOT EXCEED 12



DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS

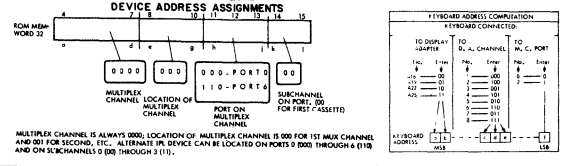


*A8, A9 & A10 FOR 1010 & 1015

NOTES

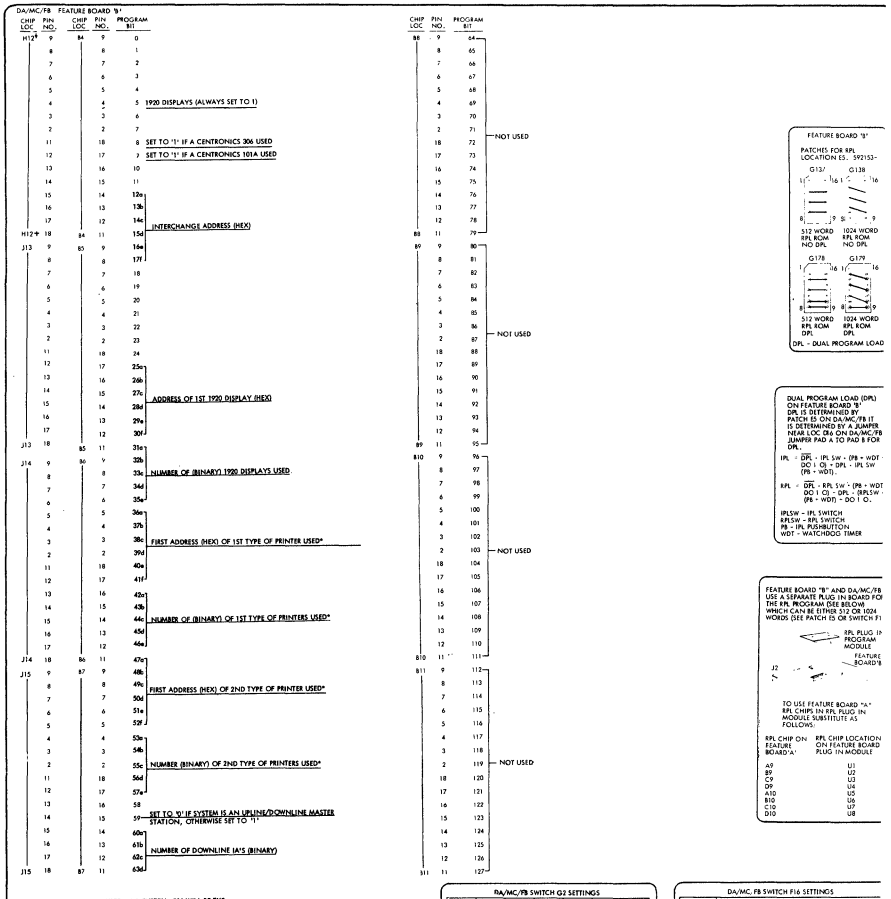
DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY. NORMALLY IN MODULE A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC., ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR PANAMAC EMULATOR USING INITIALIZATION PROGRAM 863081

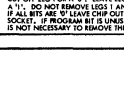


*IF 20I/S AND 101A'S ARE USED IN A SYSTEM, 20I WILL BE THE 1ST PRINTER TYPE; 101A WILL BE THE 2ND PRINTER TYPE. WHEN ASSOCIATED PRINTER IS NOT USED SET TO ZERO.

† J12 ON SOME OLDER BOARDS

MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA/MC/FB	FEATURE BOARD 'B'	IPL	512 RPL	1024 RPL
H12 †	84	40,41	40,41	40,41
J13	85	42,43	42,43	42,43
J14	86	44,45	44,45	44,45
J15	87	46,47	46,47	46,47
	88	80,81	400,401	800,801
	89	82,83	402,403	802,803
	B10	84,85	404,405	804,805
	B11	86,87	406,407	806,807

MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC, FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

MUX PORT ASSIGNMENTS

MUX 0

PORT 0 CASSETTE
- 1 MISA PRINTER #1 (G12)
- 2 MISA PRINTER #2 (G12)
- 3 MISA PRINTER #3 (G12)
- 4 MAIN IPARS MODEM ADAPT RX (G2)
- 5 MAIN IPARS MODEM ADAPT TX (G2)
- 6 HUB POLLING IPARS MODEM ADAPT (MONITOR) RX (G1)
- 7 KEYBOARD (ENABLED)

MUX 1

PORT 0 MISA PRINTER #4 (G12)
- 1 MISA PRINTER #5 (G12)
- 2 MISA PRINTER #6 (G12)
- 3 MISA PRINTER #7 (G12)
- 4 UPLINE/DOWNLINE IPARS MODEM ADAPTER RX
- 5 UPLINE/DOWNLINE IPARS MODEM ADAPTER TX
- 6 NOT USED
- 7 NOT USED

INTERRUPT LEVELS

DEVICE TYPE	INT LVL
CASSETTE	2
PRINTERS	2
KEYBOARDS	3
MAIN IPARS MODEM ADAPTER TX	4
MAIN IPARS MODEM ADAPTER RX	5
UPLINE/DOWNLINE MODEM ADAPTER TX	4
UPLINE/DOWNLINE MODEM ADAPTER RX	5
HUB POLLING MODEM ADAPTER RX	5

MONITOR CONTROLLER "F" DATACHIP CONFIGURATION
(PAN AM PATCH - A860890-10)
CUT PINS 4, 7, 8, 9, 13, 16, 17 AND 18.

MUX PATCHPLUGS

MUX 0

ADDRESS PATCH LOC G2 = G44
INTERRUPT PATCH LOC K1 = G171

NOTE: SYSTEMS IN THE FIELD THAT DO NOT USE HUB POLLING MAY USE INTERRUPT PATCH G45.

MUX 1

ADDRESS PATCH LOC G2 = G78
INTERRUPT PATCH LOC K1 = G219

MODEM ADAPTER PATCHPLUGS

UPLINE/DOWNLINE IPARS FOR MOD ADPT ON SECOND MUX OF MASTER PTS ONLY (CARRIER DETECT INTERRUPT IS DISCONNECTED)

OLD MODEM ADAPTER P.N. 860533G2		NEW MODEM ADAPTER P.N. 860820G2
LOC E5 = G170	———	LOC K6 = G170
LOC J3 = G220	———	LOC A2 = G220

MAIN IPARS - (DATA SET READY IS PATCHED HIGH)

OLD MODEM ADAPTER P.N. 860533G2		NEW MODEM ADAPTER P.N. 860820
LOC E5 = G163	———	LOC K6 = G163
LOC J3 = G147	———	LOC A2 = G147

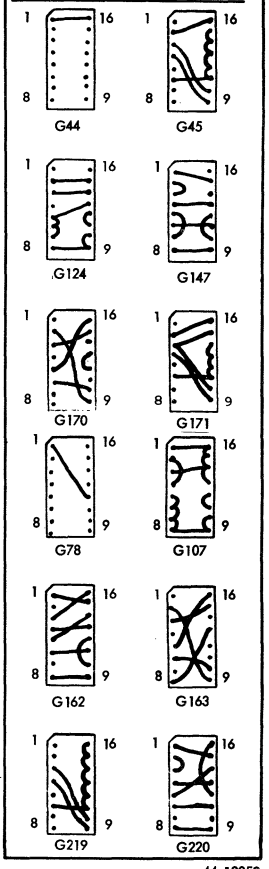
HUB POLLING IPARS

OLD MODEM ADAPTER P.N. 860533G2		NEW MODEM ADAPTER P.N. 860820G2
LOC E5 = G170	———	LOC K6 = G170
LOC J3 = G162	———	LOC A2 = G162

MISA PATCHPLUGS

LOC M5 = G107
LOC B2 = G142

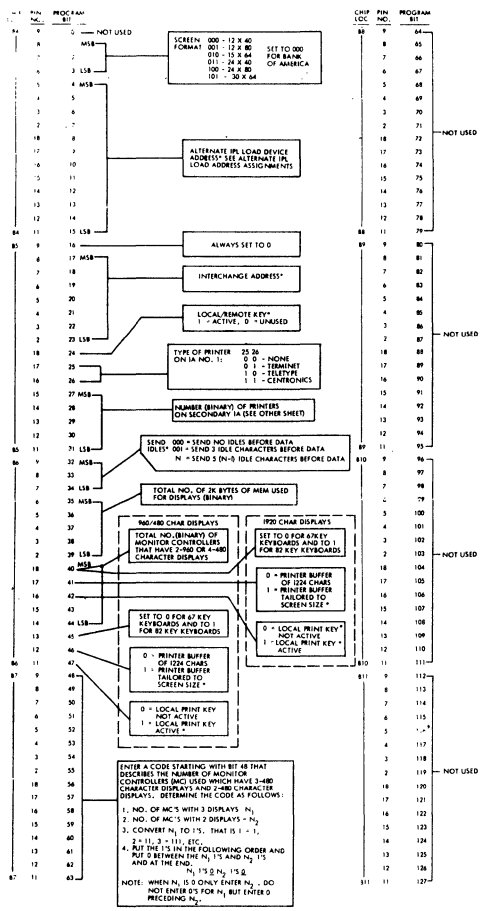
PATCHES USED IN PAN AM SYSTEM



PATCH AND SWITCH SETTINGS FOR PANAMAC EMULATOR 863081

44-10052
Sheet 2 of 2

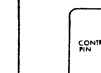
PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR 2848/2260 REMOTE EMULATOR**



* REFER TO USER SYSTEM SPECIFICATION OR FOR INTERCHANGE ADDRESS TO PROCESSING UNIT AND TERMINAL ADDRESS ASSIGNMENT TABLE.

**FOR EMULATOR 593800 REV D AND LATER

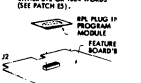
MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUTOFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE EGGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

MANUAL DATA CHIP LOC	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
	IPL	512 RPL	1024 RPL
84	40,41	40,41	40,41
85	42,43	42,43	42,43
86	44,45	44,45	44,45
87	46,47	46,47	46,48
88	80, 81	400, 401	800, 801
89	82, 83	402, 403	802, 803
810	84, 85	404, 405	804, 805
811	86, 87	406, 407	806, 807

FEATURE BOARD "B" USES A SEPARATE PLUG IN BOARD FOR THE RPL PROGRAM (SEE BELOW) WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5).



TO USE FEATURE BOARD "A" RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATION ON FEATURE BOARD PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

DUAL PROGRAM LOAD (DPL)

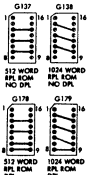
DPL IS DETERMINED BY PATCH E5.

IPL = $\overline{DPL}$ · IPL SW · (PB + WDT + DO I/O) + DPL · IPL SW · (PB + WDT).

RPL = $\overline{DPL}$ · RPL SW + (PB + WDT + DO I/O) + DPL · $\overline{IPL}$SW · (PB + WDT) + DO I/O.

IPLSW - IPL SWITCH
RPLSW - RPL SWITCH
PB - IPL PUSHBUTTON
WDT - WATCHDOG TIMER

PATCHES FOR RPL LOCATION E5. 592153-

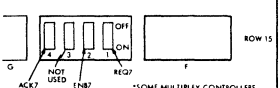


DPL - DUAL PROGRAM LOAD

MULTIPLEX CHANNEL CONTROLLER

DISABLE/ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-684-1.

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

ADDITIONAL PRINTERS ARE ASSIGNED TO ALL OTHER PORTS (SEE "PRINTER" DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS).

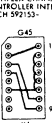
*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

G3 BOARD LOCATION

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCH 592153-



MONITOR CONTROLLER* CHARACTER/LINE FORMAT E6 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12	(24)	OPTIONS
1	——	—	—	NOTE 1
2	——	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	——
4	OPEN	CLOSED	CLOSED	——
5	CLOSED	CLOSED	CLOSED	——
6	CLOSED	OPEN	OPEN	——
7	OPEN	CLOSED	CLOSED	——
8	——	—	—	NOTE 3

*B AND C BOARDS ONLY

NOTES:

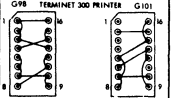
1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER. IN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
CLC	N/A	N/A	4
PRINTERS 1-4	0	3-6	2
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2
MODEM:			
SEND/REC	0	4	5
PRINTER			
IA1	0	0	2
IA2	0	3	2
IA3	0	2	2
IA4	0	1	2

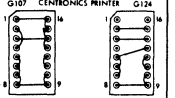
M5A PATCHES 592153-

G98 TERMINET 300 PRINTER G101



M5 - BOARD LOCATION - B2

G107 CENTRONICS PRINTER G124



M5 - BOARD LOCATION - B2

NOTE:

SPECIAL BAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT			
	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Open	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5				
6		See Below		
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.

When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

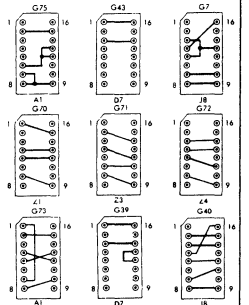
These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.

for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

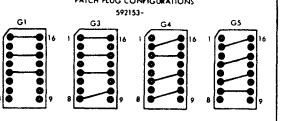
MODEM ADAPTER PATCHES 592153-



FOR DIAGNOSTIC TESTING USE PATCHES G73, G39, AND G40 IN LOCATIONS A1, D7 AND J8.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS 592153-



FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-) INTO BOARD LOCATIONS D15 AND J16	
80 X 24	G1	G3
80 X 12	G1	G4
40 X 12	G1	G5

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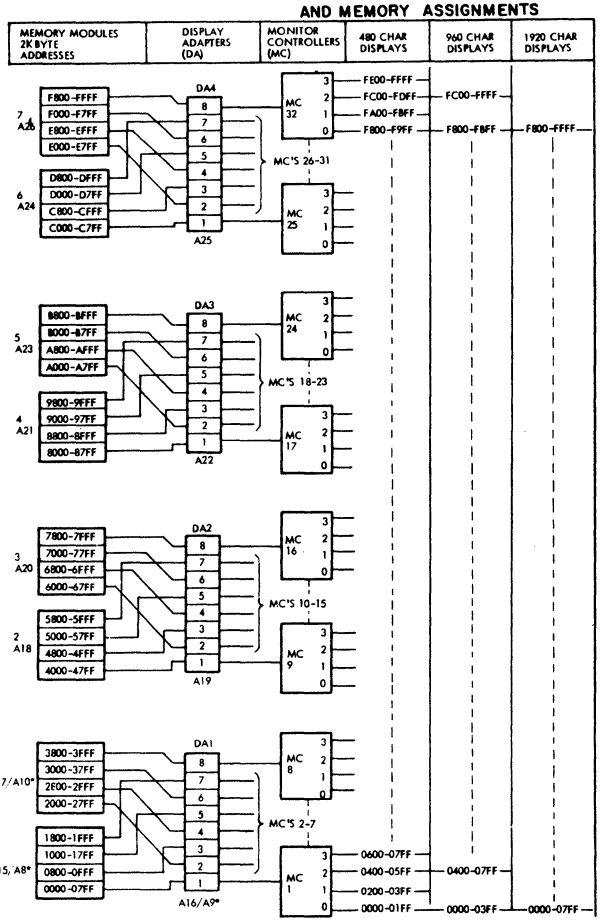
PATCH AND SWITCH SETTINGS FOR REMOTE 2248/2260 EMULATOR

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, A9 & A10 FOR 1010 & 1015

NUMBER OF PRINTERS ON SECONDARY IA'S

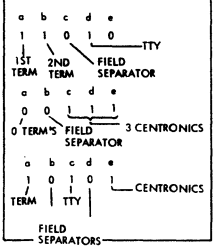
ENTER A WORD INTO B6 BITS 5-1 THAT DESCRIBES THE NUMBER AND TYPES OF PRINTERS ON SECONDARY IA'S. COMPOSE THE WORD BY LISTING THE NO. OF PRINTERS USED IN THE FOLLOWING ORDER:

FIRST - NO. OF TERMINETS USED.
SECOND - NO. OF TTY'S USED.
LAST - NO. OF CENTRONICS USED.

ENTER 1 FOR 1 PRINTER, 11 FOR 2 PRINTERS AND 111 FOR 3 PRINTERS (A MAX OF 3 PRINTERS IS ALLOWED.)

ENTER 0 IF A PRINTER IS NOT USED AND PUT A 0 BETWEEN FIELDS WHEN MORE THAN ONE PRINTER IS USED

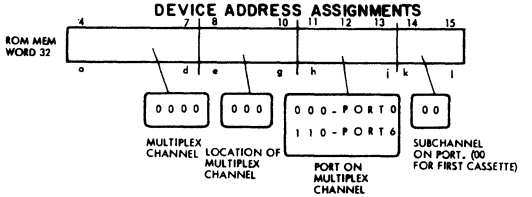
EXAMPLES:



NOTES

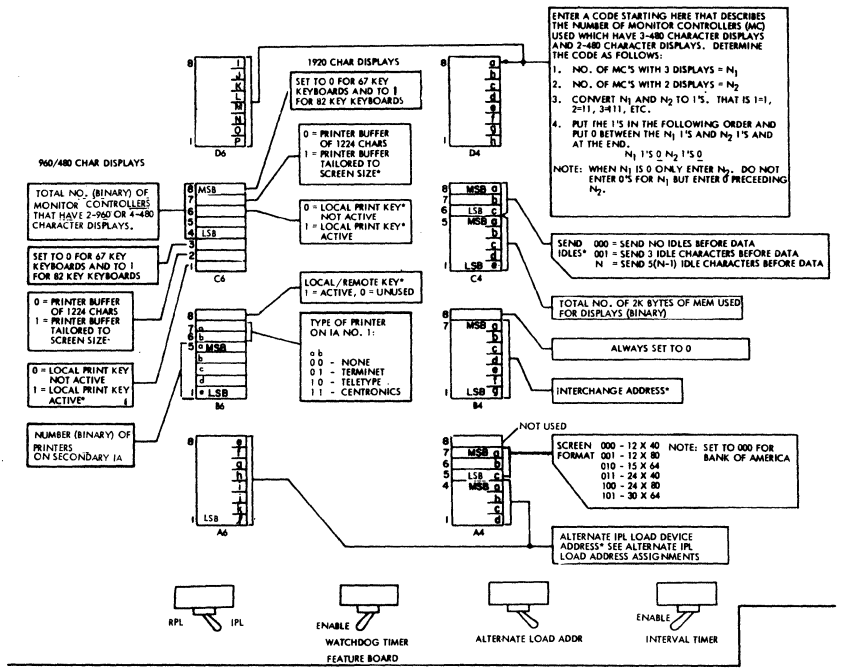
DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

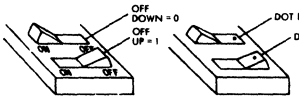
ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR REMOTE 2848/2260 EMULATOR **



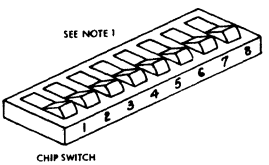


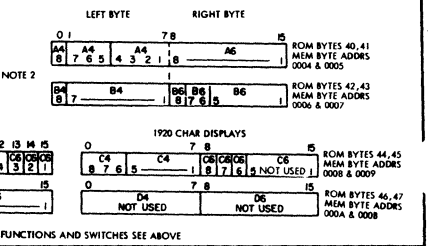
NOTES:

1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1'S.

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY

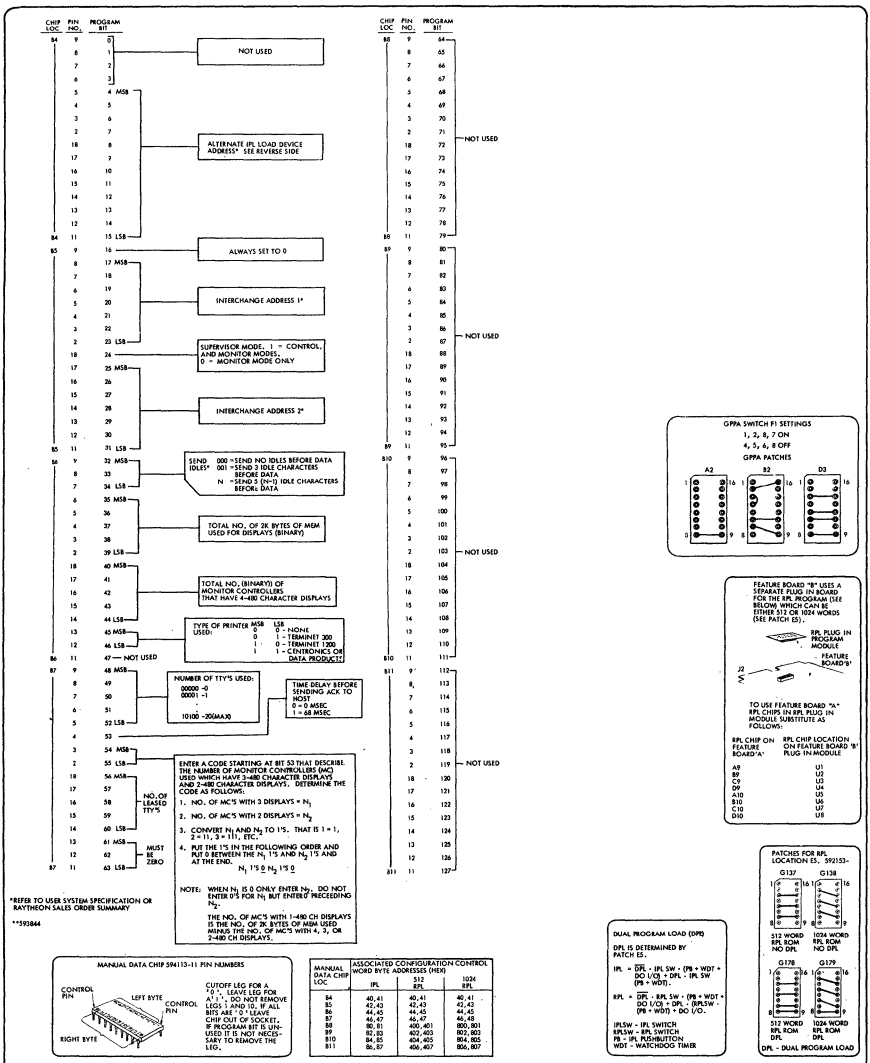
**FOR EMULATOR 593830 REV D AND LATER



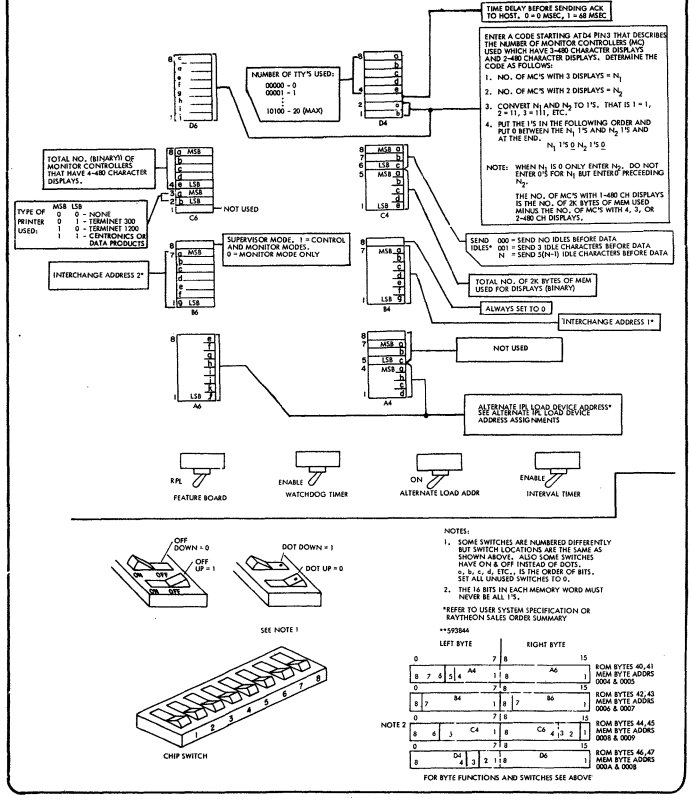


FOR BYTE FUNCTIONS AND SWITCHES SEE ABOVE

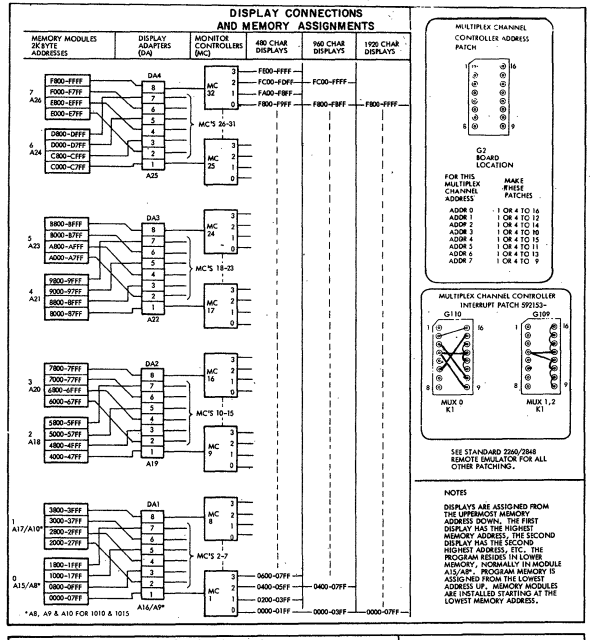
PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR TRANS UNION REMOTE 2848/2260 EMULATOR** AND TELETYPE CONCENTRATOR



PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR TRANS UNION REMOTE 2848/2260 EMULATOR** AND TELETYPE CONCENTRATOR



DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

G2 BOARD LOCATION

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

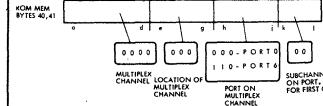
MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCH 592153-

SEE STANDARD 2260/2848 REMOTE EMULATOR FOR ALL OTHER PATCHING.

NOTES

DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

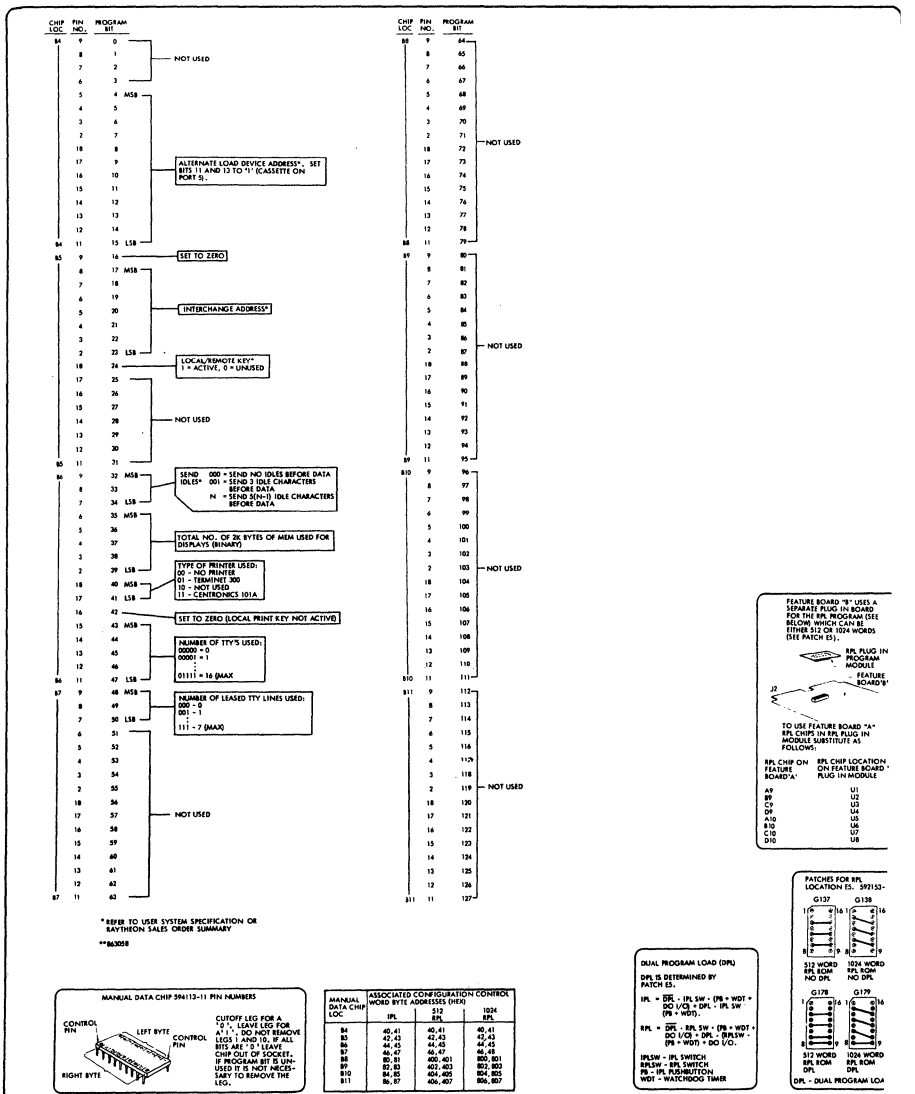
DEVICE ADDRESS AND INTERRUPT LEVEL ASSIGNMENTS

	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	5	4
KEYBOARDS	0	7	3
MODEM	0	4	5
PRINTER	0	6	2
GPCA'S	0,1&2	*	4

*ALL GPCA BOARDS USE INTERRUPT LEVEL 4 FOR ADDRESSING.

REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY FOR PORT ASSIGNMENTS.

PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR TRW CREDIT DATA SYSTEM REMOTE 2848/2260 EMULATOR AND TELETYPE CONCENTRATOR**



MANUAL DATA CHIP LOC*	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX) IPL	512 RPL	1024 RPL
B4	40, 41	40, 41	40, 41
B5	42, 43	42, 43	42, 43
B6	44, 45	44, 45	44, 45
B7	46, 47	46, 47	46, 47
B8	80, 81	400, 401	800, 801
B9	82, 83	402, 403	802, 803
B10	84, 85	404, 405	804, 805
B11	86, 87	406, 407	806, 807

DUAL PROGRAM LOAD (DPL)

DPL IS DETERMINED BY PATCH E5.

IPL = $\overline{DPL}$ · IPL SW · (PB + WDT + DO I/O) + DPL · IPL SW (PB + WDT).

RPL = $\overline{DPL}$ · RPL SW · (PB + WDT + DO I/O) + DPL · (RPLSW + (PB + WDT) + DO I/O).

IPLSW - IPL SWITCH
RPLSW - RPL SWITCH
PB - IPL PUSHBUTTON
WDT - WATCHDOG TIMER

FEATURE BOARD "B" USES A SEPARATE PLUG IN BOARD FOR THE RPL PROGRAM (SEE BELOW) WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5).

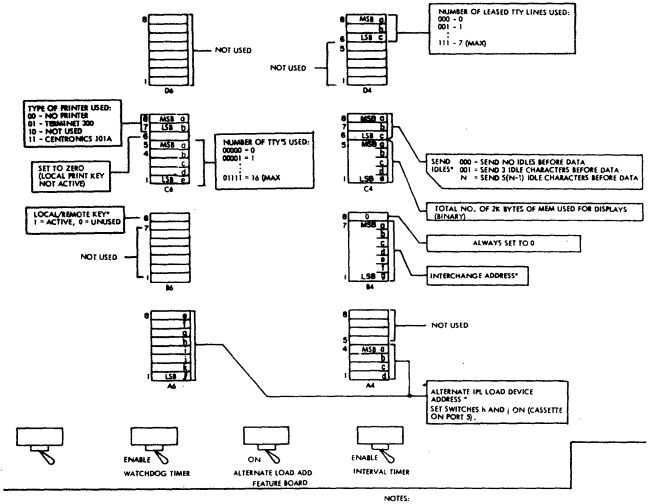
TO USE FEATURE BOARD "A" RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

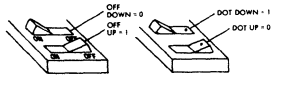
RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATION ON FEATURE BOARD 'B' PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

PATCHES FOR RPL LOCATION E5. 592153-

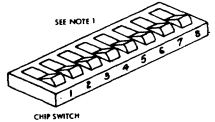
DPL - DUAL PROGRAM LOA

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR TRW CREDIT DATA SYSTEM REMOTE 2848/2260 EMULATOR** AND TELETYPE CONCENTRATOR





SEE NOTE 1



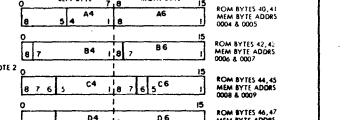
CHIP SWITCH

NOTES:

1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1'S.

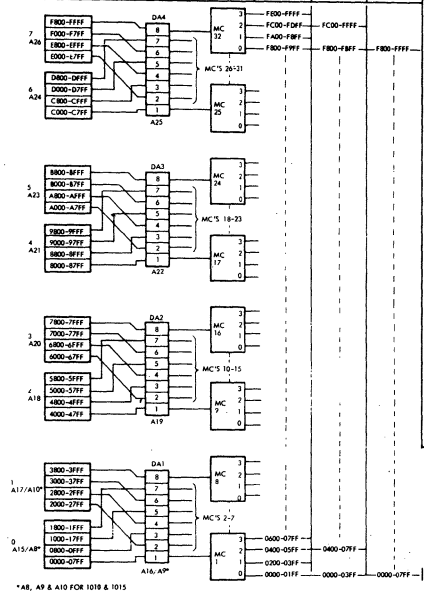
*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY

**863058

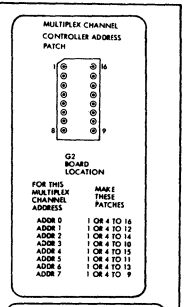


FOR BYTE FUNCTIONS AND SWITCHES SEE ABOVE

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, A9 & A10 FOR 1010 & 1015

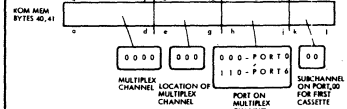


SEE STANDARD 2260/2848 REMOTE EMULATOR FOR ALL OTHER PATCHING.

NOTES

DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

DEVICE ADDRESS AND INTERRUPT LEVEL ASSIGNMENTS *

	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	5	4
KEYBOARDS	0	7	3
MODEM	0	4	5
PRINTER	0	6	7
GPCA'S	0,1&2	*	4

*ALL GPCA BOARDS USE INTERRUPT LEVEL 4 FOR ADDRESSING.

REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY FOR PORT ASSIGNMENTS.

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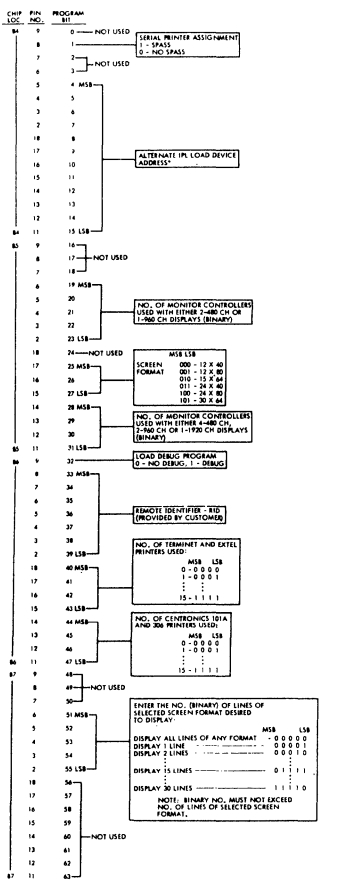
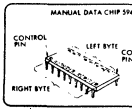
PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR UNISCOPE EMULATOR 863165



*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY

MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUTOFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 3 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

MANUAL DATA CHIP LOC	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
	IPL	512 RPL	1024 RPL
B4	40, 41	40, 41	40, 41
B5	42, 43	42, 43	42, 43
B6	44, 45	44, 45	44, 45
B7	46, 47	46, 47	46, 48
B8	80, 81	400, 401	800, 801
B9	82, 83	402, 403	802, 803
B10	84, 85	404, 405	804, 805
B11	86, 87	406, 407	806, 807

DUAL PROGRAM LOAD (DPL)

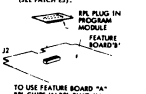
DPL IS DETERMINED BY PATCH E5.

IPL = $\overline{DPL}$ · IPLSW · (PB + WDT + DO I/O) + DPL · IPLSW · (PB + WDT).

RPL = $\overline{DPL}$ · RPLSW · (PB + WDT + DO I/O) + DPL · (RPLSW · (PB + WDT) + DO I/O.

IPLSW - IPL SWITCH
RPLSW - RPL SWITCH
PB - IPL PUSHBUTTON
WDT - WATCHDOG TIMER

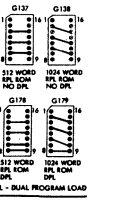
FEATURE BOARD "B" USES A SEPARATE PLUG IN BOARD FOR THE RPL PROGRAM (SEE BELOW) WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5).



TO USE FEATURE BOARD "A" RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

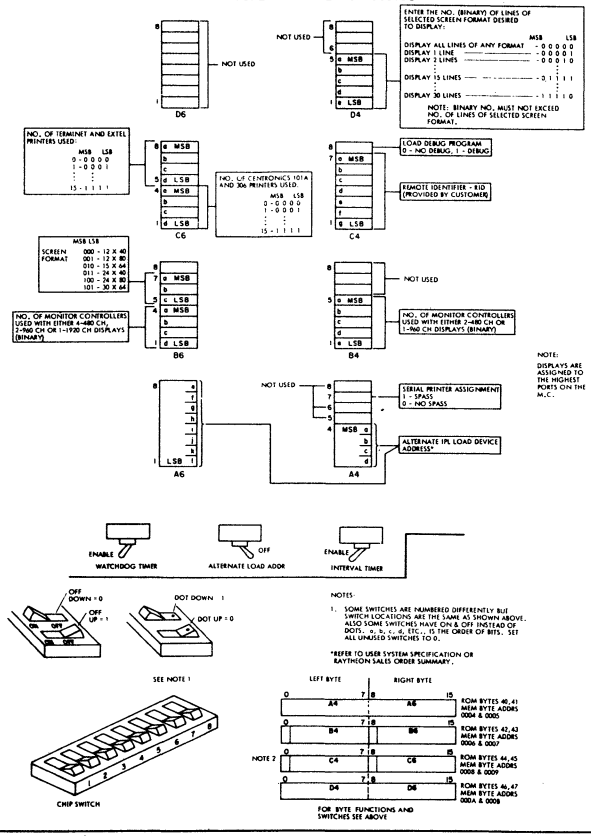
RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATION ON FEATURE BOARD 'B' PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

PATCHES FOR RPL LOCATION E5. 592153-

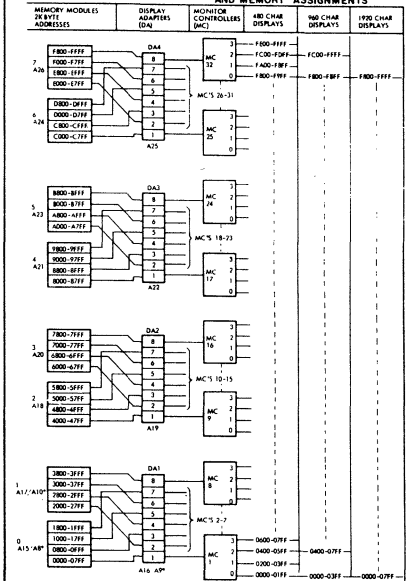


DPL - DUAL PROGRAM LOAD

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR UNISCOPE 100 EMULATOR 863165



DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, AP & A10 FOR 1010 & 1015

NOTES

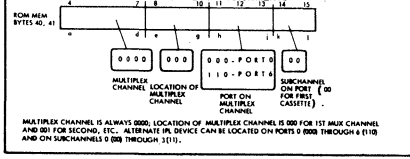
DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC., FULLY LOADED MC'S ARE ASSIGNED TO HIGHEST MEMORY, NEXT MOST FULLY LOADED MC'S ARE ASSIGNED TO NEXT HIGHEST MEMORY, ETC. PRINTER BUFFERS ARE ASSIGNED TO THE MEMORY GAPS LEFT BETWEEN DISPLAY REFRESH AREAS IN DESCENDING ORDER

EXAMPLE FOR 960 CH DISPLAYS:

DISPLAY 1 } MC
DISPLAY 2 }
DISPLAY 3 } MC
PRINTER 1 }
DISPLAY 4 } MC
PRINTER 2 }
PRINTER 3 } MC
PRINTER 4 }

THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3(11).

JANUARY 1975
64-18862
Sheet 2 of 4

MONITOR CONTROLLER B AND C

CHARACTER LINE FORMAT E6 SWITCH SETTINGS

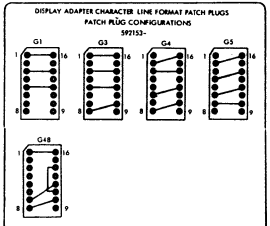
SWITCH	40 X 12	80 X 12	1240	64 X 15	1280	OPTIONS
1	—	—	—	—	—	NOTE 1
2	—	—	—	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	OPEN	CLOSED	—
4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
5	CLOSED	CLOSED	CLOSED	OPEN	OPEN	—
6	CLOSED	OPEN	OPEN	OPEN	OPEN	—
7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
8	—	—	—	—	—	NOTE 3

NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LEN 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS 592153-



FOR THESE DISPLAY CHARACTERISTICS NO. OF LINES FORMATS	INSERT THESE PATCHES* (592153-)	INTO BOARD LOCATIONS D15 AND J16	
80 X 24		G1	G3
64 X 30 & SPLIT SCREEN		G2	G3
80 X 12		G1	G4
64 X 15 OR 16		G2	G4
40 X 12		G1	G5
40 X 24		G1	G48

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSIGNED I O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO CASSETTE MODEM, ALL MODELS (WRITE TO PRINTER)	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 6 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PORT 1 AND 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER ARE NOT USED

FIRST PRINTER IS ASSIGNED TO PORT 3 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
-MODEM:			
SEND	0	2	5
REC	0	1	5
PRINTERS:			
1-4	0	3-6	2
5-12	1	0-7	2
13-15	2	0-7	2

NOTE: TERMINET AND EXTEL PRINTERS MUST BE ASSIGNED FIRST

MONITOR CONTROLLER D CHARACTER LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

	FORMAT			
Switch	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5	See Below			
6				
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.

When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.

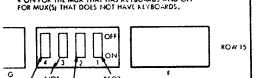
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for part 0; switches 3 and 4 are for part 1; Switches 5 and 6 are for part 2 and switches 7 and 8 are for part 3.

MULTIPLEX CHANNEL CONTROLLER

DISABLE ENABLE PORT 7 SWITCH*

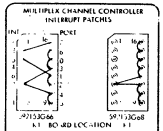
S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2, AND 4 ON FOR THE MUX THAT HAS KEYBOARD AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



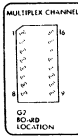
*SOME MULTIPLEX CONTROLLERS HAVE TWO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

MULTIPLEX CHANNEL CONTROLLER

INTERRUPT PATCHES



MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH



FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

8A CHIP SWITCH SETTING	40 CHAR., 12 LINES	80 CHAR., 12 LINES	64 CHAR., 15/16 LINES	80 CHAR., 24 LINES	64 CHAR., 30 LINES	48 CHAR., 24 LINES	STEP SCAN*
8A-	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	CLOSED
8A-2	OPEN	OPEN	OPEN†	OPEN	OPEN	OPEN	OPEN
8A-3	OPEN	OPEN	OPEN	CLOSED	CLOSED	CLOSED	CLOSED
8A-4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
8A-5	CLOSED	OPEN	OPEN	CLOSED	OPEN	CLOSED	**
8A-6	CLOSED	OPEN	OPEN	OPEN	OPEN	CLOSED	OPEN
8A-7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
8A-8***	OPEN	OPEN	OPEN†	OPEN	OPEN	OPEN	OPEN

*USABLE ONLY ON 24 OR 30 LINE FORMAT. SPACING BETWEEN LINES IS ADJUSTABLE BY SETTING 8B.

**SET AS INDICATED FOR 24 OR 30 LINE FORMAT.

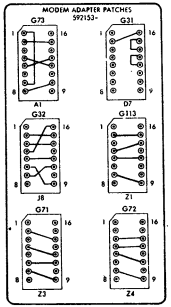
†CLOSED FOR 16 LINE FORMAT

***8A-8 IS USED ON SOME MC'S BUT IS USED ON ALL 16 LINE MC'S.

NOTE: WHEN MC IS USED WITH SPLIT SCREEN DISPLAYS A JUMPER IS CONNECTED BETWEEN X12 PIN 15 AND X7 PIN 14.

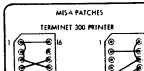
MODEM ADAPTER PATCHES

592153-



MISA PATCHES

TERMINET 300 PRINTER



592153G98
MS - BOARD LOCATION - B2

592153G101

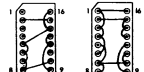
NOTE:
SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

CENTRONICS PRINTER

592153G107
MS - BOARD LOCATION - B2

592153G124

EXTEL PRINTER



592153G139
MS BOARD LOCATION B2

592153G140

592153G128

EXTEL MODEL	BAUD RATE	PATCHES MS	PATCHES B2
15,30	165	G139	G140
30	150	G128	G101*
30	300	GND*	G101*

*SEE TERMINET 300

PATCH AND SWITCH SETTING FOR UNISCOPE 100 EMULATOR

MARCH 1976
44-1067

DEBUG PROGRAM DIRECTIVES

(DEBUG FEATURE BOARD SWITCH MUST BE SET "ON" TO USE DIRECTIVE)

.DEBUG	ENABLE DEBUG MODE
XX	DISABLE DEBUG MODE
HA(A), (B)	ADD A + B
HS(A), (B)	SUBTRACT A-B
TR(LOC), (AC), (X1), (X2), (CB)	LOAD REGISTER AND TRANSFER
PA(LOC), (VAL1), (VAL2), . . .	PATCH LOC TO VAL1, LOC+2 TO VAL2, ETC.
CK(VAL), (VAL), . . .	COMPUTE CHECKSUM
WI	DISPLAY RID, SID, HOME ADDRESS, AND DST NUMBER
IS	INITIALIZE STATISTICS TABLE AND ERROR TABLE
CT (UNIT)	CREATE TAPE ON SPECIFIED MUX/PORT/ XPORT (DEFAULT IS 0/0/0)
CS (DST1), (DST2), . . .	CONNECT SCREENS FOR SRM
SL (LEVEL 1), (LEVEL 2), . . .	LEVEL 5: 1 MAIN LOOP 2 .OMPRC ENTRANCE 3 .OMPRC TEXT ROUTINE 4 .IMPRC IOACT RETURN 5 MODEM RECEIVE IOACT RETURN 7 .IMPRC TASK BRANCH 8 MODEM RECEIVE LINE RESTART 10 RECEIVE ERROR 11 TRANSMIT ERROR 12 SOH IN TEXT ERROR 13 ADDRESSING ERROR 14 CHARACTER ERROR 15 ESCAPE SEQUENCE ERROR 17 BCC ERROR 18 SET CURSOR ERROR
SY	SRM ON
SN	SRM OFF
AY	MONITOR ALL RECORDS
AN	IGNORE ALL RECORDS
TY (X)	MONITOR ALL RECORDS OF TYPE (X)
TN (X)	IGNORE ALL RECORDS OF TYPE (X)
WY (X) (W)	MONITOR WORD (W) OF ALL RECORDS OF TYPE (X)
WN (X) (W)	IGNORE WORD (W) OF ALL RECORDS OF TYPE (X)
DY (ZZ)	MONITOR ALL RECORDS FOR DEVICE (ZZ)
DN (ZZ)	IGNORE ALL RECORDS FOR DEVICE (ZZ)
ML (LOC)	MONITOR LOCATION SPECIFIED BY LOC
1Y	ONE SHOT MODE ON
1N	ONE SHOT MODE OFF
PS	PRINT ALL CONNECTED SCREENS
PX	STOP ALL PRINT OPERATIONS
RS	CLEAR ALL SRM SCREENS

CASSETTE PROGRAM PATCH PROCEDURE

1. IPL OLD CASSETTE.
2. DURING IPL STORE X'BKXX' INTO LOCATION 0 (WHERE XXX = DEVICE ADDRESS OF TARGET DRIVE).
3. WHEN IPL IS COMPLETE LOCATION 0 WILL CONTAIN X'0100'. IF NOT RETRY.
4. ENTER PATCHES. DO NOT PRESS STOP OR RESET.
5. PUT A NEW CASSETTE IN TARGET DRIVE.
6. STORE X'BKXX' INTO LOCATION 0 AS ABOVE. LOCATION 0 WILL CHANGE TO X'0300' TO INDICATE THAT THE DUMP IS IN PROGRESS.
7. THE TAPE WILL REWIND AND STOP WHEN COMPLETE AND LOCATION 0 WILL CONTAIN X'0100'. IF MORE COPIES ARE DESIRED RETURN TO STEP 5.
8. IF AN ERROR OCCURS, THE TAPE WILL TRY TO REWRITE CONTINUOUSLY. TO START OVER INSERT A NEW CASSETTE AND STORE X'BKXX' INTO LOCATION 0.

NOTE: FOR ADDITIONAL INFORMATION REFER TO FIB NO. PS-0018.

COMMUNICATIONS REGION (ADDRESS AT LOCATION X'C')

WORD DISPLACEMENT	DEFINITION	
0	REVISION LEVEL (ASCII)	REVISION SUBLEVEL (ASCII)
1	STATISTICS TABLE ADDRESS	
2	ERROR TABLE ADDRESS	
3	LINE CONTROL BLOCK ADDRESS	
4	ADDRESS OF TABLE CONTAINING DST ADDRESSES	
5	RECEIVE BUFFER ADDRESS	
6	ADDRESS OF FIRST XMIT BUFFER	
7	ADDRESS OF SOFTWARE TIMER CELL	

PRINTER STATUS TABLE (PST ADDR IN DST)

WORD DISPLACEMENT	DEFINITION	
0	STATUS	LUN
1	CURRENT PRINT ADDRESS	
2	PRINTER BUFFER ADDRESS	
3	PRINTER TIMER ADDRESS	
4	PRINTER IOCQ ADDRESS	
5	PRINTER STATUS FOR HOST	

ERROR TABLE (ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION
0	MODEM RECEIVE ERROR COUNTER
1	MODEM TRANSMIT ERROR COUNTER
2	SOH IN TEXT ERROR COUNTER
3	ADDRESSING ERROR COUNTER
4	ILLEGAL CHARACTER ERROR COUNTER
5	ESCAPE SEQUENCE ERROR COUNTER
6	CHARACTER PARITY ERROR COUNTER
7	BCC ERROR COUNTER
8	CURSOR ADDRESSING ERROR COUNTERS
9	MODEM RECEIVE IO ACTION ERROR COUNTER

LINE CONTROL BLOCK (LCB ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION	
0	RECEIVE CHANNEL UP/DOWN	
1	CURRENT RECEIVE IOCQ ADDRESS	
2	FIRST RECEIVE IOCQ ADDRESS	
3	.OMPRC RE-ENTRANCE ADDRESS	
4	FIRST MODEM RECEIVE BUFFER ADDRESS	
5	FIRST DST ADDRESS	
6	NUMBER OF DST'S	
7	MODEM RECEIVE TIMER ADDRESS	
8	MODEM RECEIVE LUN	
9	NUMBER OF XMIT BUFFERS AVAILABLE	
A	MODEM XMIT CHANNEL UP/DOWN	
B	MODEM XMIT ERROR FLAG	
C	CURRENT MODEM XMIT IOCQ ADDRESS	
D	FIRST XMIT IOCQ ADDRESS	
E	MODEM XMIT TIMER ADDRESS	
F	INPUT MESSAGE COLLECTION ACTIVE FLAG	
10	MODEM XMIT LUN	
11	MODEM XMIT BUFFER ADDRESS	
12	NOT USED	
13	CURRENT OUTPUT MSG PROCESSOR DST	
14	POLL TIMER ADDRESS	
15	ACK CONTROL BYTE	OUTPUT MESSAGE TYPE
16	SID FROM LAST OUTPUT MSG	DID FROM LAST OUTPUT MESSAGE
17	RID FROM FEATURE BOARD	SID OF LAST INPUT TERMINAL
18	TERMINAL STATUS OF LAST INPUT DEVICE	

DISPLAY STATUS TABLE (FIRST DST ADDR IN LCB)

WORD DISPLACEMENT	DEFINITION	
0	LINK TO NEXT DST	
1	KEYBOARD NUMBER	STATUS
2	CURSOR ADDRESS	
3	HOME ADDRESS	
4	NOT USED	XMIT LUN
5	HOME FOR DEBUG	
6	LED BYTE ADDRESS	
7	CURSOR ADDRESS DURING MESSAGE COLLECTION	
8	PRINTER STATUS TABLE ADDRESS	
9	SOE ADDRESS	
A	SID	PRINTER STATUS
B	DISPLAY END ADDRESS	
C	NUMBER OF CHAR LEFT ON LINE	

STATISTICS TABLE (ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION
0	OUTPUT MESSAGE FROM HOST
1	INPUT MESSAGE TO HOST
2	BROADCAST MESSAGE FROM HOST
3	PRINTER MESSAGE FROM HOST
4	PRINTER STATUS REQUEST FROM HOST
5	MESSAGE WAITING FROM HOST
6	REPLY REQUEST TO HOST
7	RETRANSMIT REQUEST FROM HOST
8	GENERAL POLL FROM HOST
9	SPECIFIC POLL FROM HOST
A	OUTPUT FROM HOST TO ANOTHER RID
B	NO BUSINESS RESPONSE SENT TO HOST
C	MESSAGE WAITING SENT TO HOST
D	PRINTER STATUS SENT TO HOST
E	LOOK-FOR SYNC ISSUED TO MODEM RECEIVE

SRM	NODE DEFINITION	
+0	LINK TO NEXT (0=END OF LIST)	
+2	ADDRESS TO START TRACE (LSB ON = INDIRECT)	
+4	NUMBER OF BYTES TO TRACE	
+6	DEVICE ID (BINARY)	DISPLAYED ON TRACE TO IDENTIFY ENTRY
+7	NODE ID (ASCII)	
+8	TRACE MASK*	
+A to A+n	SCRATCH AREA WHERE n = NO. OF BYTES TO TRACE	

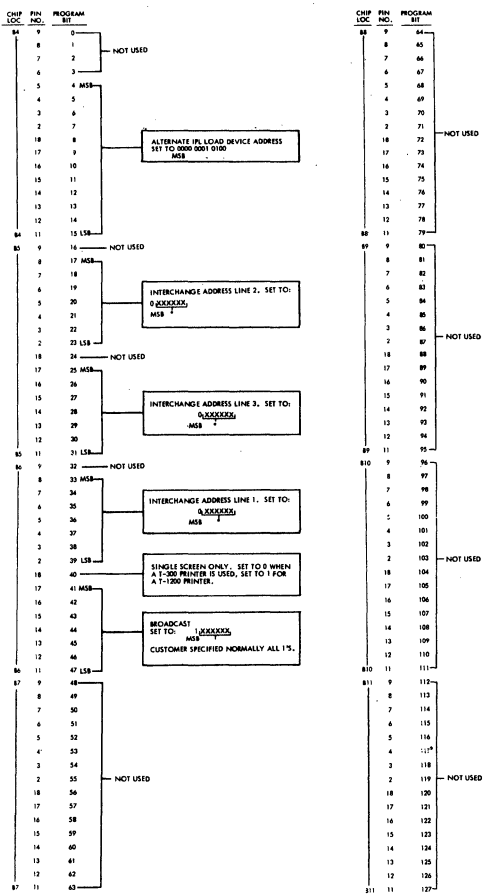
*MASK - BIT 0 = 1 SKIP THIS NODE.
BITS 1-15 = 1 SKIP CORRESPONDING WORD (i.e., bit 15 - word 0, bit 14 - word 1)

SRM NODE TYPES

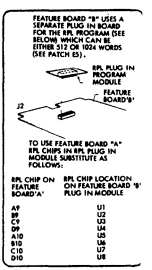
A	MODEM XMIT BUFFER
B	MODEM RECEIVE BUFFER
C	MODEM XMIT PCB
D	MODEM RCV PCB
E	MODEM XMIT PIOT
F	MODEM RECEIVE PIOT
G	MODEM RECEIVE FIOB
H	MODEM XMIT FIOB
I	PRINTER FIOB
J	PRINT BUFFER
K	DISPLAY STATUS TABLE
L	FIRST 16 WORDS OF LCB
M	LAST 9 WORDS OF LCB
P	PRINTER STATUS TABLE
Q	PRINTER IOCQ
R	MODEM RECEIVE IOCQ
S	STATISTICS TABLE
T	MODEM XMIT IOCQ
X	ERROR TABLE
Z	DEFINE BY 'ML' DIRECTIVE

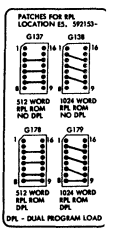
UNISCOPE 100 EMULATOR SOFTWARE NOTES

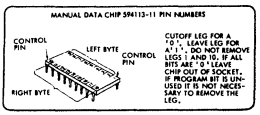
PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR MIDWEST STOCK EXCHANGE (MSE)



*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY.







MANUAL DATA CHIP LOC	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
	IPL	512 RPL	1024 RPL
B4	40,41	40,41	40,41
B5	42,43	42,43	42,43
B6	44,45	44,45	44,45
B7	46,47	46,47	46,48
B8	B0,B1	400,401	B00,B01
B9	B2,B3	402,403	B02,B03
B10	B4,B5	404,405	B04,B05
B11	B6,B7	406,407	B06,B07

DUAL PROGRAM LOAD (DPL)

DPL IS DETERMINED BY PATCH E5.

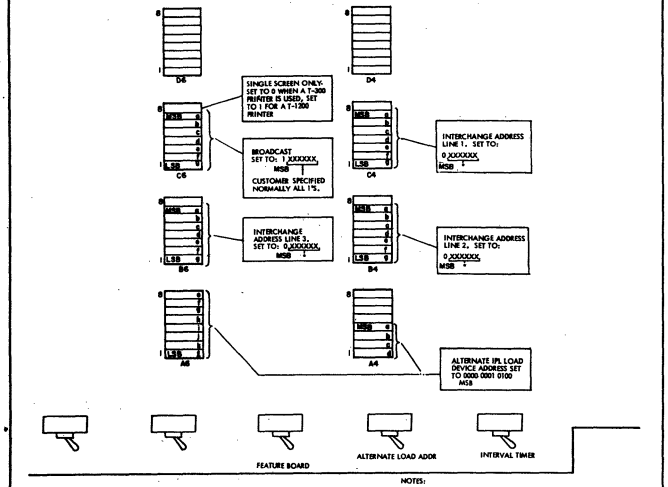
IPL = DPL • IPL SW • (PB + WDT + DO I/O + DPL • IPL SW (PB + WDT).

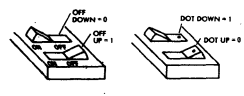
RPL = DPL • RPL SW • (PB + WDT + DO I/O + DPL • RPLSW • (PB + WDT) + DO I/O.

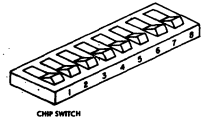
IPLSW - IPL SWITCH
RPLSW - RPL SWITCH
PB - IPL PUSHBUTTON
WDT - WATCHDOG TIMER

FEBRUARY 19
44-8054
Sheet 1 of

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR MIDWEST STOCK EXCHANGE (MSE)



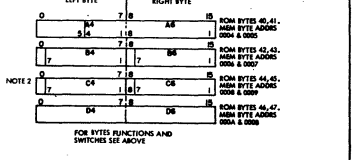




NOTES:

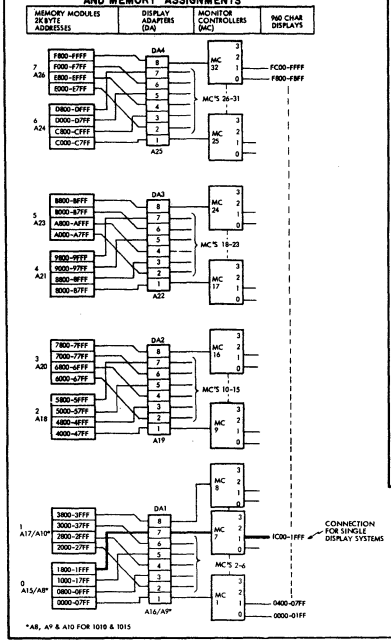
1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1'S.

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY.



FOR BYTES FUNCTIONS AND SWITCHES SEE ABOVE

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, A9 & A10 FOR 1010 & 1015

ORDER OF I/O DEVICE ASSIGNMENT

DEVICE	QTY
HOST MODEM	1-3
VOGUE PRINTERS	0-3
CARD READERS	0-2
T1200 PRINTERS	0-8
T300 PRINTERS	0-8

I/O DEVICE PORT ASSIGNMENTS*

MUX CHAN CONTROLLER	PORT	DEVICES
0	0	RESERVED (M-UNIT)
	1	HOST MODEM
	2	HOST MODEM
	3	PRINTER** OR ANY DEVICE
	4	ANY DEVICE
	5	ANY DEVICE
	6	ANY DEVICE
0	7	KEYBOARD
1	0	ANY DEVICE
1	1	ANY DEVICE
1	2	ANY DEVICE
1	3	ANY DEVICE
1	4	ANY DEVICE
1	5	ANY DEVICE
1	6	ANY DEVICE
1	7	ANY DEVICE

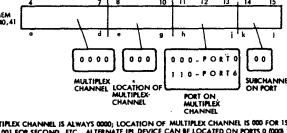
*CONNECT DEVICES TO FIRST AVAILABLE PORT LISTED

**SINGLE DISPLAY SYSTEM

NOTES

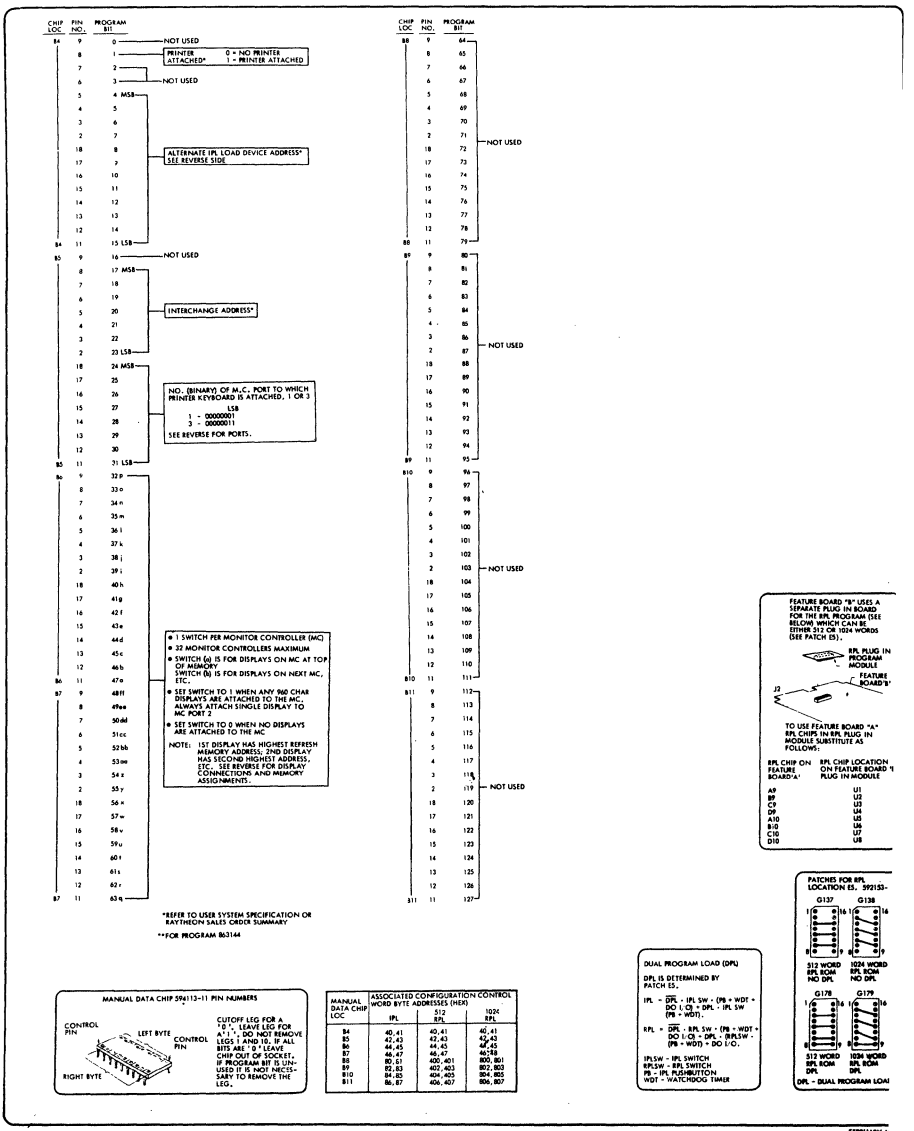
DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY. NORMALLY IN MODULE A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR QANTAS EUROPE PARS/IPARS EMULATOR **



FEATURE BOARD "B" USES A SEPARATE PLUG IN BOARD FOR THE RPL PROGRAM (SEE BELOW) WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5).

TO USE FEATURE BOARD "A" RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

RPL CHIP ON FEATURE BOARD "A"	RPL CHIP LOCATION ON FEATURE BOARD "B" PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

PATCHES FOR RPL LOCATION E5, 592153-

DPL = DUAL PROGRAM LOAD

MANUAL DATA CHIP 594113-11 PIN NUMBERS

CUTOFF LEG FOR A "0", LEAVE LEG FOR A "1"; DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE "0" LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

MANUAL DATA CHIP LOC	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
	IPL	512 RPL	1024 RPL
B4	40,41	40,41	40,41
B5	42,43	42,43	42,43
B6	44,45	44,45	44,45
B7	46,47	46,47	46745
B8	80,81	400, 401	800, 801
B9	82,83	402, 403	802, 803
B10	84,85	404, 405	804, 805
B11	86, 87	406, 407	806, 807

DUAL PROGRAM LOAD (DPL)

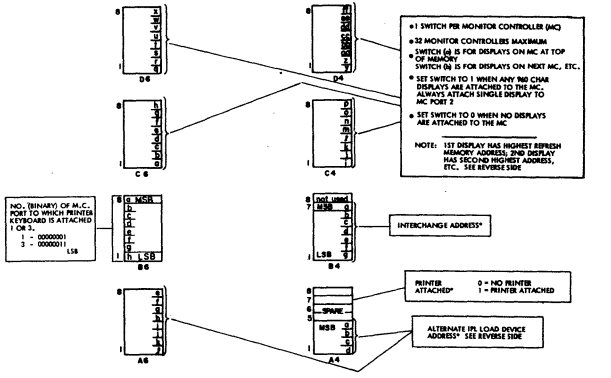
DPL IS DETERMINED BY PATCH E5.

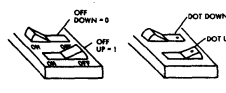
IPL = $\overline{DPL}$ · IPL SW · (PB + WDT + DO I/O) + DPL · IPL SW (PB + WDT).

RPL = $\overline{DPL}$ · RPL SW · (PB + WDT + DO I/O) + DPL · (RPLSW · (PB + WDT) + DO I/O).

IPLSW - IPL SWITCH
RPLSW - RPL SWITCH
PB - IPL PUSHBUTTON
WDT - WATCHDOG TIMER

PTS-100 FEATURE BOARD CHIP SWITCH SETTINGS FOR QANTAS EUROPE PARS/IPARS EMULATOR**



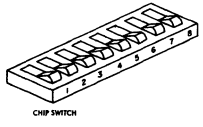


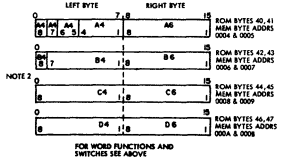
SEE NOTE 1

NOTE
1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, etc., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS TN EACH MEMORY WORD MUST NEVER BE ALL 1'S.

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY

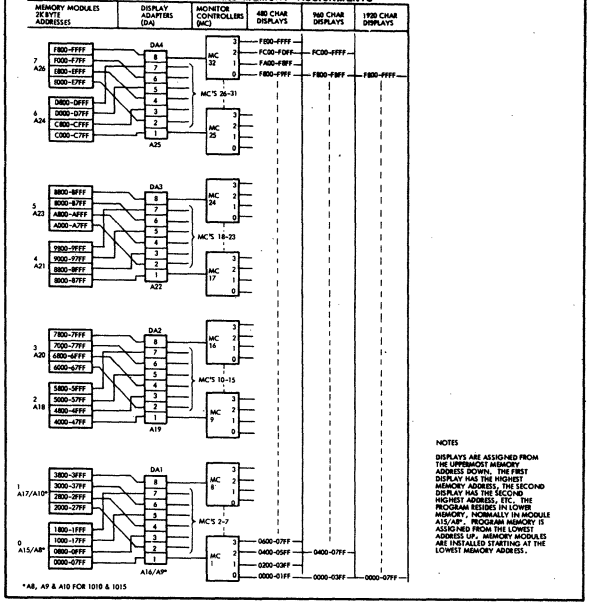
**PROGRAM 8631#4





FOR WORD FUNCTIONS AND SWITCHES SEE ABOVE

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS

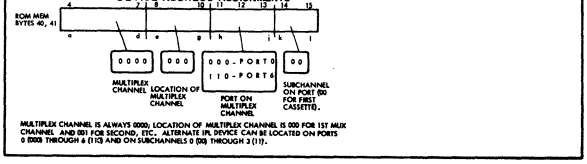


*A8, A9 & A10 FOR 1010 & 1015

NOTES

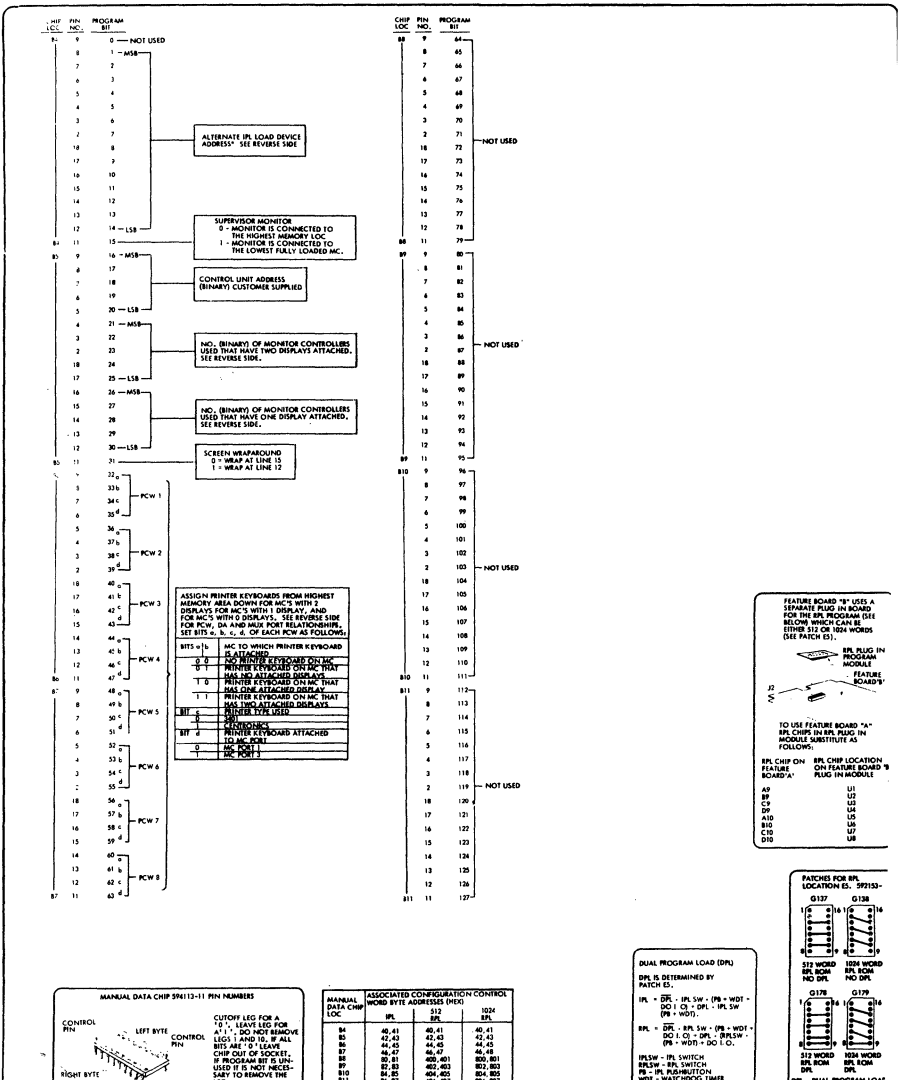
DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY; NORMALLY IN MODULE A15/A9*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR QANTAS AUSTRALIAN 425 EMULATOR



FEATURE BOARD "B" USES A SEPARATE PLUG IN BOARD FOR THE RPL PROGRAM (SEE BELOW) WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5).

TO USE FEATURE BOARD "A" RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATION ON FEATURE BOARD 'B' PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

PATCHES FOR RPL LOCATION E5. 592153-

DUAL PROGRAM LOAD (DPL)

DPL IS DETERMINED BY PATCH E5.

IPL = $\overline{DPL}$ · IPL SW · (P8 + WDT · DO I. C) + DPL · IPL SW (P8 + WDT).

RPL = DPL · RPL SW · (P8 + WDT · DO I. C) + DPL · (RPLSW · (P8 + WDT) + DO I. C).

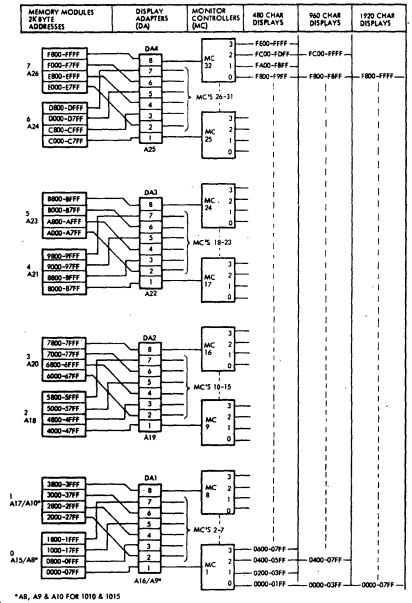
IPLSW - IPL SWITCH
RPLSW - RPL SWITCH
P8 - IPL PUSHBUTTON
WDT - WATCHDOG TIMER

MANUAL DATA CHIP 594113-11 PIN NUMBERS

CUTOFF LEG FOR A '0', LEAVE LEG FOR A '1', DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

MANUAL DATA CHIP LOC	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
	IPL	512 RPL	1024 RPL
B4	40,41	40,41	40,41
B5	42,43	42,43	42,43
B6	44,45	44,45	44,45
B7	46,47	46,47	46,45
B8	80,81	400,401	800,801
B9	82,83	402,403	802,803
B10	84,85	404,405	804,805
B11	86,87	406,407	806,807

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS

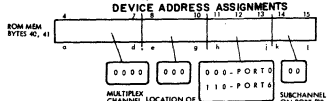


*A8, A9 & A10 FOR 1010 & 1015

NOTES

DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY, BELOW 3000 HEX. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

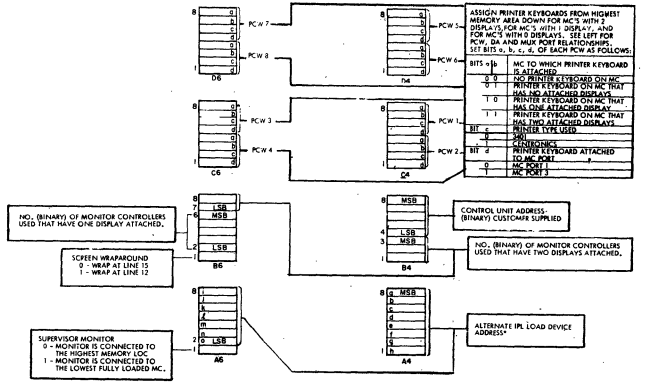
ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS

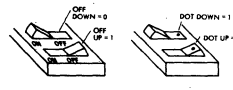


MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PRINTER MUX PORT		SOFTWARE DA	PCW
0	6	00	1
0	3	01	2
0	2	02	3
0	1	03	4
1	0	04	5
1	1	05	6
1	2	06	7
1	3	07	8

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR QANTAS AUSTRALIAN 425 EMULATOR

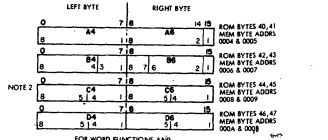




NOTES:

1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1'S.

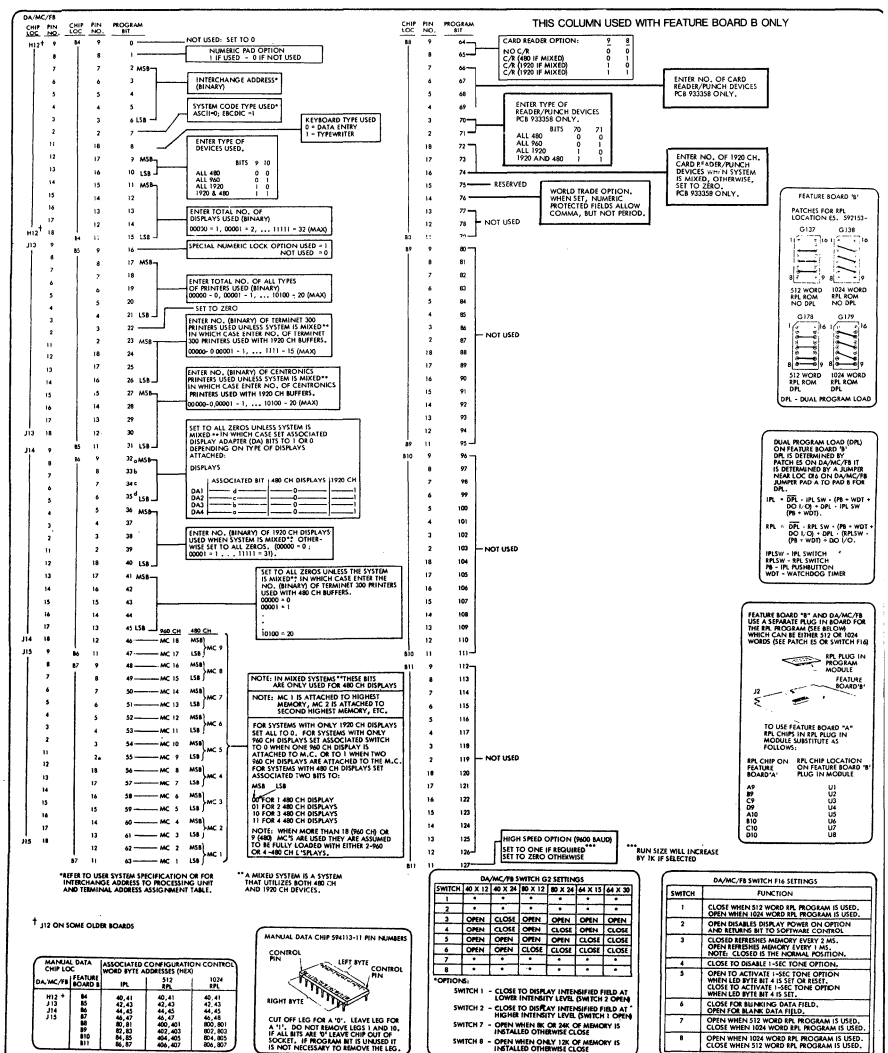
*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY.



FOR WORD FUNCTIONS AND SWITCHES SEE ABOVE

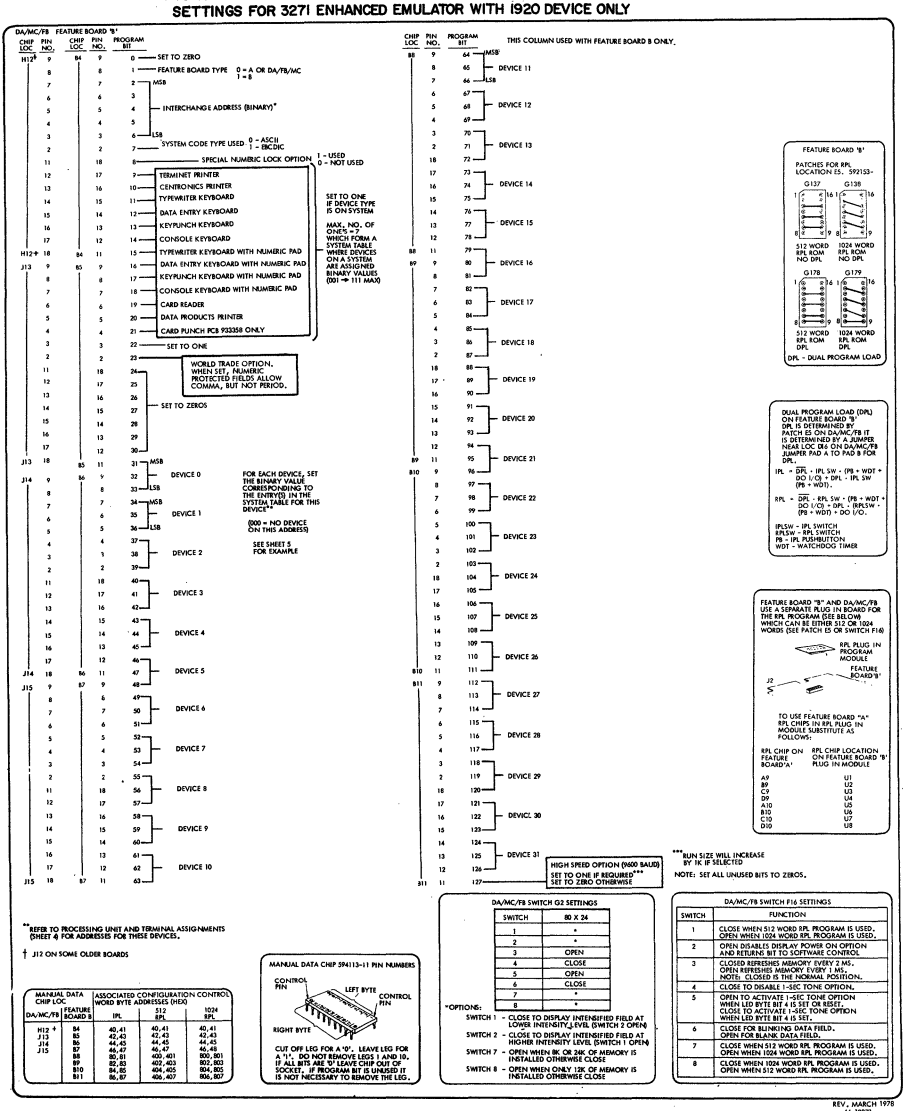
JANUARY 1975
44-1068
Sheet 2 of 2

PTS 100 FEATURE BOARD CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR 3271 ENHANCED EMULATOR



REV., MARCH 1978
44-10071
SHEET 1 OF 5.

PTS-100 FEATURE BOARD CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR 3271 ENHANCED EMULATOR WITH 1920 DEVICE ONLY



**REFER TO PROCESSING UNIT AND TERMINAL ASSIGNMENTS (SHEET 4 FOR ADDRESSES FOR THESE DEVICES.

† J12 ON SOME OLDER BOARDS

MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA/MC/FB	FEATURE BOARD B	IPL	512 RPL	1024 RPL
H12 †	B4	40,41	40,41	40,41
J13	B5	42,43	42,43	42,43
J14	B6	44,45	44,45	44,45
J15	B7	46,47	46,47	46,48
	B8	80,81	400,401	800,801
	B9	82,83	402,403	802,803
	B10	84,85	404,405	804,805
	B11	86,87	406,407	806,807

CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

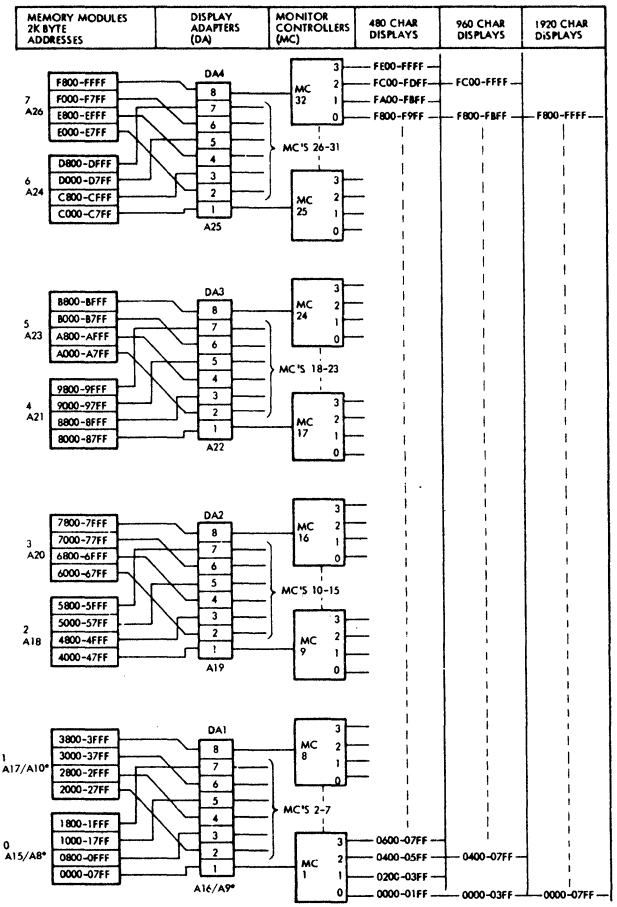
SWITCH	80 X 24
1	*
2	*
3	OPEN
4	CLOSE
5	OPEN
6	CLOSE
7	*
8	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
8	CLOSE WHEN 1024 WORD RPL PROGRAM IS USED. OPEN WHEN 512 WORD RPL PROGRAM IS USED.

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, A9 & A10 FOR 1010 & 1015

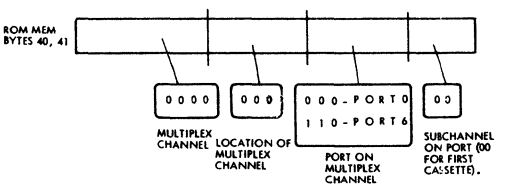
NOTES

ALL DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. IN A MIXED SYSTEM 1920 CH DISPLAYS ARE ASSIGNED BEFORE 480 CH DISPLAYS. ALSO THE STARTING MEMORY ADDRESSES ARE DETERMINED BY WHICH DISPLAY ADAPTERS ARE ASSIGNED TO 1920 CH AND 480 CH DISPLAYS (SEE C4 ON F.B.'A'). IF A SYSTEM IS MIXED OR DOES NOT FULLY LOAD ALL M.C.'s, PRINTER BUFFERS WILL BE ASSIGNED TO THE UNUSED AREAS. IN A MIXED ** SYSTEM PRINTERS ARE ASSIGNED AS FOLLOWS:

1 CENTRONICS - 1920 CH BUFFER
2 TERMINET - 1920 CH BUFFER
3 CENTRONICS - 480 CH BUFFER
4 TERMINET - 480 CH BUFFER

THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULES A17/A10* AND A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

MONITOR CONTROLLER C CHARACTER/LINE FORMAT & SWITCH SETTINGS

SWITCH	40 X 12	80 X 12	(24)	OPTIONS
1	——	—	—	NOTE 1
2	——	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	——
4	OPEN	CLOSED	CLOSED	——
5	CLOSED	CLOSED	CLOSED	——
6	CLOSED	OPEN	OPEN	——
7	OPEN	CLOSED	CLOSED	——
8	—	—	—	NOTE 3

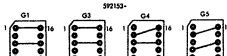
NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS

5921530-



FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (5921530-)	INTO BOARD LOCATIONS D15 AND J16	
80 X 24		G1	G3
80 X 12		G1	G4
40 X 12		G1	G5

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER (TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (READ FROM) IS ASSIGNED TO PORT 1 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (WRITE TO) IS ASSIGNED TO PORT 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS.

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

4415A PATCHES

TERMINET 300 PRINTER

CENTRONICS PRINTER

NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

COMMUNICATIONS REGION DEFINITION (POINTED TO BY LOC 0026)

DISPLACEMENT	DEFINITION
0	REV AND SUB REV IN ASCII
2	LOAD ADDRESS OF KSVC
4	CSVC LOAD ADDRESS
6	PSVC LOAD ADDRESS
8	ISVC LOAD ADDRESS
A	CRSVC LOAD ADDRESS
C	POINTER TO I/O BUFFER ADDRESS
E	POINTER TO DUMMY BUFFER ADDRESS
10	FIRST PIOT ADDRESS
12	KEYBOARD IOCQ ADDRESS
14	KEYBOARD TUMBLE TABLE ADDRESS
16	POINTER TO DATA ENTRY XLATE TABLE
18	POINTER TO TYPEWRITER XLATE TABLE
1A	POINTER TO DEAUXILIARY TABLE
1C	POINTER TO TYPE AUXILIARY TABLE
1E	POINTER TO NUMERIC PAD TABLE
20	ADDRESS OF SIM PARAMETER LIST
22	ADDRESS OF ERROR COUNTER TABLE
24	FIRST COMMUNICATION IOCQ
26	ADDRESS OF FEATURE TABLE FOR SYSGEN

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

	FORMAT			
Switch	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5		See Below		
6				
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.
When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

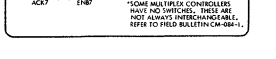
for HI Intensity - close ODD numbered switches and open others.
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MULTIPLEX CHANNEL CONTROLLER

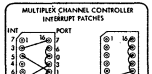
DISABLE ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). THIS SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES, THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-058-1.

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



FIRST MULTIPLEX CHANNEL CONTROLLER

2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

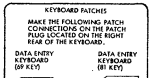
DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	2	
KEYBOARDS	0	7	3
MODEMS SEND	0	2	5
REC	0	1	5
PRINTERS 1-4	0	3-6	3
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

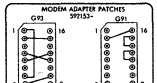
KEYBOARD PATCHES

MAKE THE FOLLOWING PATCH CONNECTIONS ON THE PATCH PLUG LOCATED ON THE RIGHT REAR OF THE KEYBOARD.



MODEM ADAPTER PATCHES

5921530-

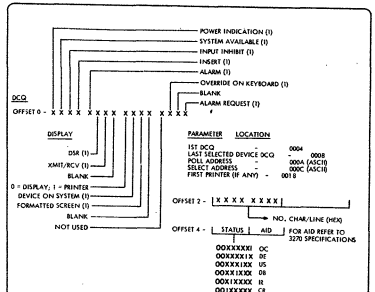


Processing Unit and Terminal Addressing Assignments

Encode on Feature Board: Processing Unit or Device Number	Column 1 Use this column to find: • Device Selection, • Specific Poll, • General Poll, and • Fixed Return Addresses — EBCDIC Hex	ASCII Hex	Column 2 Use this column to find: • PES Selection Addresses — EBCDIC Hex	ASCII Hex
0	40	20	60	20
1	C1	41	61	2F
2	C2	42	E2	53
3	C3	43	E3	54
4	C4	44	E4	55
5	C5	45	E5	56
6	C6	46	E6	57
7	C7	47	E7	58
8	C8	48	E8	59
9	C9	49	E9	5A
10	4A	5B	6A	5C
11	4B	2E	6B	2C
12	4C	3C	6C	25
13	4D	28	6D	5F
14	4E	2B	6E	3E
15	4F	21	6F	3F
16	50	26	F0	30
17	D1	4A	F1	31
18	D2	4B	F2	32
19	D3	4C	F3	33
20	D4	4D	F4	34
21	D5	4E	F5	35
22	D6	4F	F6	36
23	D7	50	F7	37
24	D8	51	F8	38
25	D9	52	F9	39
26	5A	5D	7A	3A
27	5B	24	7B	23
28	5C	2A	7C	40
29	5D	29	7D	27
30	5E	3B	7E	3D
31	5F	5E	7F	22

NOTE

I/O character address 7F is used as the device address to specify a General Poll operation.



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PATCH AND SWITCH SETTINGS AND SOFTWARE NOTES FOR 3271 ENHANCED EMULATOR

MONITOR CONTROLLER F - (P/N 860548) - EXCEPT FIRST 250 BOARDS P/N 860864, PAM ONLY)

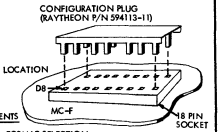
CONFIGURATION PLUG (D8)

THE MC-F HAS ONE SOCKET WHICH REQUIRES A CONFIGURATION PLUG TO SELECT MOST OF THE AVAILABLE OPTIONS. ANY POSSIBLE COMBINATION OF OPTIONS CAN BE SELECTED BY CUTTING OFF APPROPRIATE LEGS OF THE PLUG.

NOTE: 1. WITHOUT TRANSMITTER MODULE, THE MC-F IS COMPLETELY BACKWARDS COMPATIBLE WITH THE PRESENT D.A.

2. WITH TRANSMITTER MODULE, MC-F HAS THE ADDED COAX CABLE OPTION USED WITH D.A. "C".

CONFIGURATION SOCKET LOCATION



OPTION PIN ASSIGNMENTS

FORMAT SELECTION

CONFIG. PLUG PIN NO.	DISPLAY FORMATS						
	40X12	40X24	64X15	64X16	64X30	80X12	80X24
4	CUT	CUT	CUT	IN	CUT	CUT	CUT
11	CUT	IN	CUT	CUT	IN	CUT	IN
12	CUT	CUT	IN	IN	IN	IN	IN
17	IN	IN	CUT	CUT	CUT	IN	IN

DISPLAY ADAPTER "C"

P/N 860629

8K AND 16K MEMORIES

DISPLAY ADAPTER "C" HAS A PROVISION FOR THREE AUXILLIARY MODULES TO USE IBM COAX CABLE: TWO RECEIVER BOARDS AND ONE COAX CONTROL LOGIC BOARD.

CHARACTER/LINE FORMAT AND MEMORY REFRESH TIMING PATCH PLUGS

FOR THESE DISPLAYS CHAR/LINES NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-)	INTO BOARD LOCATIONS				
		E10	J16	C2 (Norm)	C2 (Opt)	C3 16K / 8K
80 X 24	G1	G3	G134 OR G136		G133 OR G135	
64 X 30 & SPLIT SCREEN	G2	G3	G134 OR G136		G133 OR G135	
80 X 12	G1	G4	G134 OR G136		G133 OR G135	
64 X 15 OR 16	G2	G4	G134 OR G136		G133 OR G135	
40 X 12	G1	G5	G134 OR G136		G133 OR G135	
40 X 24	G1	G48	G134 OR G136		G133 OR G135	

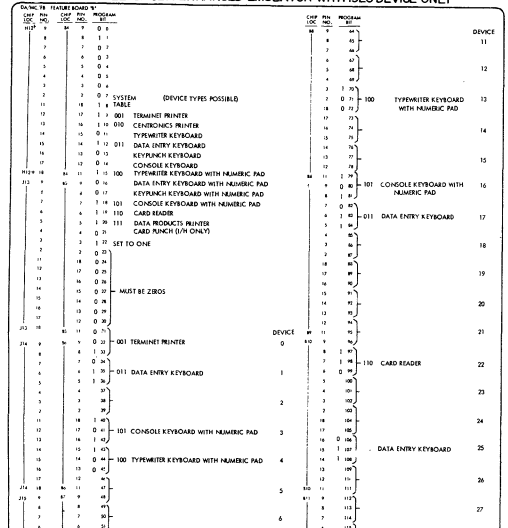
E10 NUMBER OF CHARACTERS PER LINE

J16 NUMBER OF LINES PER FORMAT

C2 MEMORY REFRESH
- G134 - 2 MS (NORMAL TIMING)
- G136 - 1 MS (OPTION TIMING)

C3 TYPE OF MEMORY MODULE
- G135 - 8K MEMORY MODULE
- G133 - 16K MEMORY MODULE

EXAMPLE OF 3271 ENHANCED EMULATOR WITH 1920 DEVICE ONLY



NOTE: SET ALL UNUSED BITS TO ZEROS.

FROM THE LIST OF 15 POSSIBLE DEVICE TYPES, UP TO 7 MAY BE SELECTED. THESE FORM THE SYSTEM TABLE AND ARE NUMBERED CONSECUTIVELY IN THE ORDER IN WHICH THEY OCCUR IN THE POSSIBLE DEVICE TYPES TABLE.

FOR THIS EXAMPLE THE SYSTEM TABLE WOULD BE:

DECIMAL	BINARY	
(1)	001	TERMINET PRINTER
(2)	010	CENTRONICS PRINTER
(3)	011	DATA ENTRY KEYBOARD
(4)	100	TYPEWRITER KEYBOARD WITH NUMERIC PAD
(5)	101	CONSOLE KEYBOARD WITH NUMERIC PAD
(6)	110	CARD READER (ONE ONLY)
(7)	111	DATA PRODUCTS PRINTER

THE THREE NUMBERS IN THE BINARY COLUMN INDICATE WHICH DEVICE TYPE IS TO BE AT THAT ADDRESS.

FOR EXAMPLE:

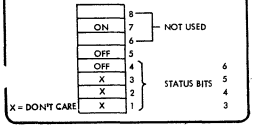
DEVICE LOCATION 0 (BITS 31, 32, 33) SHOW 001 WHICH STANDS FOR THE FIRST DEVICE TYPE OF THE SYSTEM TABLE WHICH IS A TERMINET PRINTER, THEREFORE, DEVICE 0 IS A TERMINET PRINTER AT ADDRESS 40 (28CDIC).

DEVICE LOCATION 25 (BITS 106, 107, 108) SHOW 011 WHICH IS THE THIRD TYPE WHICH IS DATA ENTRY KEYBOARD, THEREFORE, A DISPLAY WITH A DATA ENTRY KEYBOARD IS DEVICE 25 AT ADDRESS 09 (8CDIC).

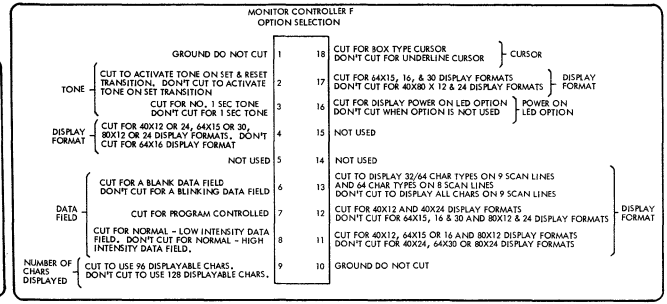
PARALLEL ADAPTER PATCHING AND SWITCHING FOR DATA PRODUCTS 2230 LINE PRINTER

IN LOCATIONS	INSERT PATCHES 593192-
A2	G148
D3	G148
B2	G149

ALSO SET DIP SWITCH AT LOCATION F1 AS FOLLOWS FOR 3270



MONITOR CONTROLLER F
OPTION SELECTION



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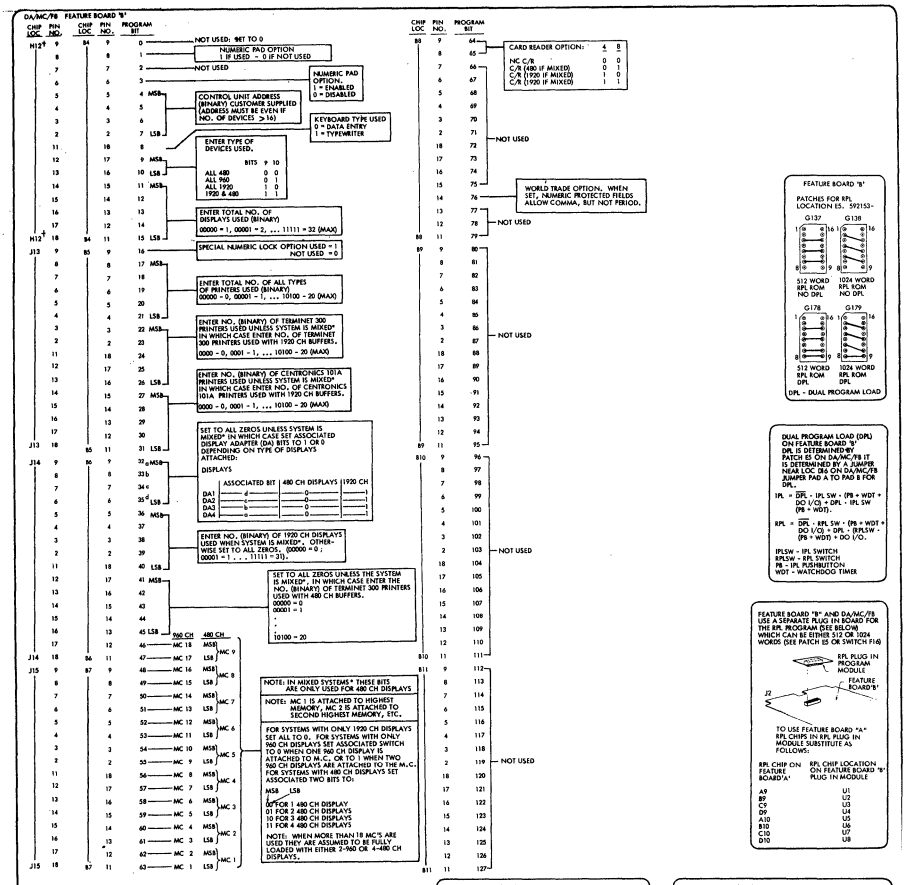
PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR 3272-ENHANCED EMULATOR

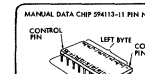


* A MIXED SYSTEM IS A SYSTEM THAT UTILIZES BOTH 480 CH AND 1920 CH DEVICES.

† J12 ON SOME OLDER BOARDS

MANUAL DATA CHIP LOC DA/MC/FB	FEATURE BOARD 'B'	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX) IPL	512 RPL	1024 RPL
H12 †	B4	40,41	40,41	40,41
J12	B5	42,43	42,43	42,43
J14	B6	44,45	44,45	44,45
J15	B7	46,47	46,47	46,48
	B8	80,81	400,401	800,801
	B9	82,83	402,403	802,803
	B10	84,85	404,405	804,805
	B11	86,87	406,407	806,807

MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:

SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)

SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)

SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE

SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/78 SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS., OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO AND HALF DUPLEX) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PORT 1 AND 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER ARE NOT USED

FIRST PRINTER IS ASSIGNED TO PORT 3 OF FIRST MULTIPLEX CHANNEL CONTROLLER

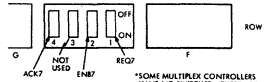
ADDITIONAL PRINTERS ARE ASSIGNED TO ALL OTHER PORTS (SEE "PRINTER" DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS).

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MULTIPLEX CHANNEL CONTROLLER

DISABLE/ENABLE PORT 7 SWITCH*

S1 DISABLES ACK7, ENB 8 REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.

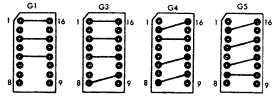


*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS

592153-



FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS

INSERT THESE PATCHES (592153-) INTO BOARD LOCATIONS D15 AND J16

80 X 24	G1	G3
80 X 12	G1	G4
40 X 12	G1	G5

MONITOR CONTROLLER* CHARACTER/LINE FORMAT E6 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12	(24)	OPTIONS
1	——	——	——	NOTE 1
2	——	——	——	NOTE 2
3	OPEN	OPEN	CLOSED	——
4	OPEN	CLOSED	CLOSED	——
5	CLOSED	CLOSED	CLOSED	——
6	CLOSED	OPEN	OPEN	——
7	OPEN	CLOSED	CLOSED	——
8	——	——	——	NOTE 3

*C BOARD ONLY

NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

G2 BOARD LOCATION

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

	FORMAT			
Switch	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5				
6		See Below		
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.

When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

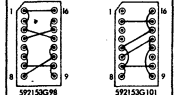
for HI Intensity - close ODD numbered switches and open others.

for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MISA PATCHES

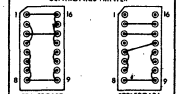
TERMINET 300 PRINTER



592150G98 592153G101

MS - BOARD LOCATION - B2

CENTRONICS PRINTER



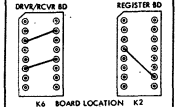
592153G107 592153G124

MS - BOARD LOCATION - B2

NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

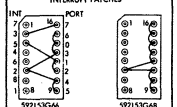
CIC PATCHES



THIS PATCH ALLOWS MORE THAN 16 DEVICES TO BE ADDRESSED (592153G88)

INTERRUPT LEVEL 4 (592153G89)

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



592153G66 592153G68

FIRST MULTIPLEX CHANNEL CONTROLLER

2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
CIC	N/A	N/A	4
PRINTERS 1-4	0	3-6	2
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2

KEYBOARD PATCHES

MAKE THE FOLLOWING PATCH CONNECTIONS ON THE PATCH PLUG LOCATED ON THE RIGHT REAR OF THE KEYBOARD.

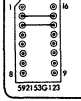
DATA ENTRY KEYBOARD (69 KEY)

592153G112

DATA ENTRY KEYBOARD (81 KEY)

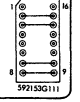
592153G144

TYPEWRITER KEYBOARD (69 KEY)



592153G123

TYPEWRITER KEYBOARD (81 KEY)



592153G111

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PATCH AND SWITCH SETTINGS FOR 3272 ENHANCED EMULATOR

COMMUNICATIONS REGION DEFINITION (POINTED TO BY LOC 0026)

DISPLACEMENT	DEFINITION
0	REVISION LEVEL (ASCII) ‡ REVISION SUB-LEVEL (ASCII)
2	ADDRESS OF CIC DEVICE PACKETS
4	ADDRESS OF CIC TUMBLE TABLE
6	ADDRESS OF CIC ADDRESS TRANSLATE TABLE
8	ADDRESS OF CIC OFF LINE TABLE
A	ADDRESS OF CHANNEL I/O BUFFER*
C	ADDRESS OF DUMMY WORK BUFFER
E	ADDRESS OF KEYBOARD IOCQ
10	ADDRESS OF CIC CONTROLLER IOCQ
12	ADDRESS OF CIC DEVICE IOCQ
14	ADDRESS OF KEYBOARD TUMBLE TABLE
16	ADDRESS OF KEYBOARD TRANSLATE TABLE
18	LOAD ADDRESS OF K/PSVC MODULE
1A	LOAD ADDRESS OF CSVC MODULE
1C	LOAD ADDRESS OF ISVC MODULE
1E	ADDRESS OF SRM PARAMETER LIST
20	ADDRESS OF DCQ ADDRESS TABLE
22	ADDRESS OF ERROR COUNTER TABLE
24	CIC CONTROLLER IOCQ
26	CIC DEVICE IOCQ
28	CIC DEVICE PACKET BASE
2A	CIC INTERRUPT TUMBLE TABLE
2C	CIC START CONTROLLER TABLE
2E	CIC ONLINE/OFFLINE TABLE
30	DCQ ADDRESS TABLE
32	FEATURE TABLE FOR SYSGEN

*CONSISTS OF 2 BUFFERS OF EQUAL SIZE. SIZE DETERMINED BY SUBTRACTING THIS ADDRESS FROM DUMMY WORK BUFFER ADDRESS.

DCQ DEFINITION

0	LED BYTE+	CONFIG*
2+	NO. CHAR/LINE	NO. LINES
4	STATUS*	AID (ASCII)**
6	BASE BUFFER ADDRESS	
8	CURRENT BUFFER ADDRESS	
A	CURSOR ADDRESS	
C	ATTRIBUTE ADDRESS	
E	NEXT DCQ ADDRESS	
14	DEVICE ADDRESS (BINARY)	
16	KYBD ADDR OR PRINTER MUX/PORT - LUN ID	
1A	DEBUG FLAG	ENHANCEMENT BYTE

NOTES: DCQ'S ARE LOCATED AT THE END OF EACH DEVICE'S BUFFER AREA.
*REFER TO DCQ BIT DEFINITION TABLE BELOW FOR DEFINITIONS.
**REFER TO 3270 SPECIFICATION
+ NOT VALID FOR PRINTERS

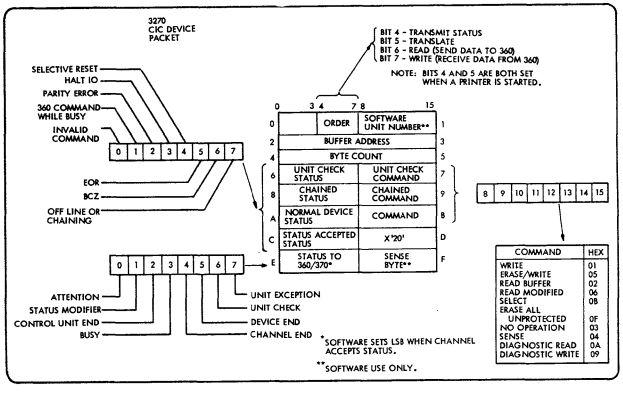
DCQ BIT DEFINITIONS

BYTE / BIT	LED BYTE	CONFIGURATION	STATUS
0	POWER	0=DISPLAY 1=PRINTER	DEBUG - FULL SCREEN DUMP
1	SYSTEM AVAILABLE	DEVICE ON LINE	DEBUG - ONE LINE DUMP
2	INPUT INHIBIT	FORMATTED SCREEN	NOT USED
3	INSERT	NOT USED	IR PENDING
4	ALARM	NOT USED	DEVICE BUSY (PRINTER)
5	DSR (NOT USED)	OVERRIDE ON KEYBOARD	NOT USED
6	XMIT/RCV	NOT USED	DE PENDING
7	DEBUG MODE	ALARM REQUEST	NOT USED

ENHANCEMENT BYTE

8	9	10	11	12 - 15
				N/U

	DISPLAY	OTHER DEVICE
11	1 = NUMERIC PAD	1 = LOCAL ONLY LOCAL PRINTER
10	1 = SPECIAL NUMERIC LOCK	1 = LOCAL PRINTER
00	TYPEWRITER KBD	TERMINET
01	DATA ENTRY KBD	CENTRONICS
10	CONSOLE KBD	DATA PRODUCTS
11	KEYPUNCH KBD	CARD READER



COMMAND	HEX
WRITE	01
ERASE/WRITE	05
READ BUFFER	02
READ MODIFIED	06
SELECT	0B
ERASE ALL UNPROTECTED	0F
NO OPERATION	03
SENSE	04
DIAGNOSTIC READ	0A
DIAGNOSTIC WRITE	09

DEBUG PROGRAM OPERATING PROCEDURE

TO ENTER DEBUG:
TYPE <DM> PRESS PA1
ENTER ALL COMMANDS AT HOME; CURSOR ENDS LINE

COMMANDS:

HA, A, B	-	ADD A+B
HS, A, B	-	A-B
DM	-	SET DUMP = FULL SCREEN
DL	-	SET DUMP = TOP LINE ONLY
PR, DEV	-	PRINT, DEV MUST BE PRINTER
CP, D1, D2, D3...	-	COPY FROM DEVICE 1 TO DEVICE 2, 3, ETC.
TR, LOC, AC, X1, X2, CB	-	TRANSFER TO LOCATION, DEFINE REGISTERS
SI, DEV	-	INITIALIZE SRM INTO DEVICE'S BUFFER.
PA, LOC, VAL, VAL...	-	PATCH MEMORY
SY	-	SRM ON
SN	-	SRM OFF
ID	-	DISPLAY DEVICE ADDRESS
XX	-	EXIT DEBUG MODE
MS, DEV, OP CODE	-	ISSUE CIC MSC FOR DEVICE

OP CODES:
0 T + S CUB, SEND ATTN.
1 SET DVB
2 RESET DVB
3 SET OFF LINE
4 RESET OFF LINE
5 T + S CUB, SEND STATUS
6 RESET CUB

NOTES: 1. ALL OTHER ENTRIES PERFORM MEMORY DUMP, FIRST FOUR CHARACTERS TAKEN AS STARTING ADDRESS.
2. DEV = PTS DEVICE ADDRESS (X'20' - X'3F').
3. LEADING ZEROS NOT REQUIRED.

LOCATION	PARAMETER
0004	FIRST DCQ
0008	DCQ OF DEVICE BEING SERVICED
000A	CIC PACKET OF DEVICE BEING SERVICED
000C	COMMUNICATIONS REGION ADDRESS
0018	FIRST PRINTER DCQ (IF ANY)

SRM	PARAMETER LIST DEFINITION
+0	SRM SWITCH; 0 = ENABLE, 8000 = DISABLE
+2	ADDRESS OF NODE LIST
+4	WIDTH OF DISPLAY AREA
+6	NO. OF LINES IN DISPLAY AREA
+8	BASE ADDRESS OF DISPLAY AREA
+A	CURRENT DISPLAY ADDRESS (INITIALLY = BASE)
+C	CURRENT LINE POSITION (INITIALLY = 0)
+E	CURRENT COLUMN POSITION (INITIALLY = 0)

SRM	NODE DEFINITION
+0	LINK TO NEXT (0=END OF LIST)
+2	ADDRESS TO START TRACE (LSB ON = INDIRECT)
+4	NUMBER OF BYTES TO TRACE
+6	DEVICE ID (BINARY) — DISPLAYED ON TRACE TO IDENTIFY ENTRY
+7	NODE ID (ASCII)
+8	TRACE MASK*
+A to A+n	SCRATCH AREA WHERE n = NO. OF BYTES TO TRACE

*MASK - BIT 0 = 1 SKIP THIS NODE.
BITS 1-15 = 1 SKIP CORRESPONDING WORD (i.e., bit 15 - word 0, bit 14 - word 1)

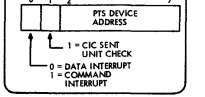
CASSETTE PROGRAM PATCH PROCEDURE

1. IPL OLD CASSETTE.
2. DURING IPL STORE X'80XX' INTO LOCATION 0 (WHERE XXX = DEVICE ADDRESS OF TARGET DRIVE).
3. WHEN IPL IS COMPLETE LOCATION 0 WILL CONTAIN X'0100'. IF NOT RETRY.
4. ENTER PATCHES. DO NOT PRESS STOP OR RESET.
5. PUT A NEW CASSETTE IN TARGET DRIVE.
6. STORE X'80XX' INTO LOCATION 0 AS ABOVE. LOCATION 0 WILL CHANGE TO X'0300' TO INDICATE THAT THE DUMP IS IN PROGRESS.
7. THE TAPE WILL REWIND AND STOP WHEN COMPLETE AND LOCATION 0 WILL CONTAIN X'0100'. IF MORE COPIES ARE DESIRED RETURN TO STEP 5.
8. IF AN ERROR OCCURS, THE TAPE WILL TRY TO REWRITE CONTINUOUSLY. TO START OVER INSERT A NEW CASSETTE AND STORE X'80XX' INTO LOCATION 0.

NOTE: FOR ADDITIONAL INFORMATION REFER TO FIB NO. PS-0018.

CIC TUMBLE TABLE

ENTRY FORMAT:



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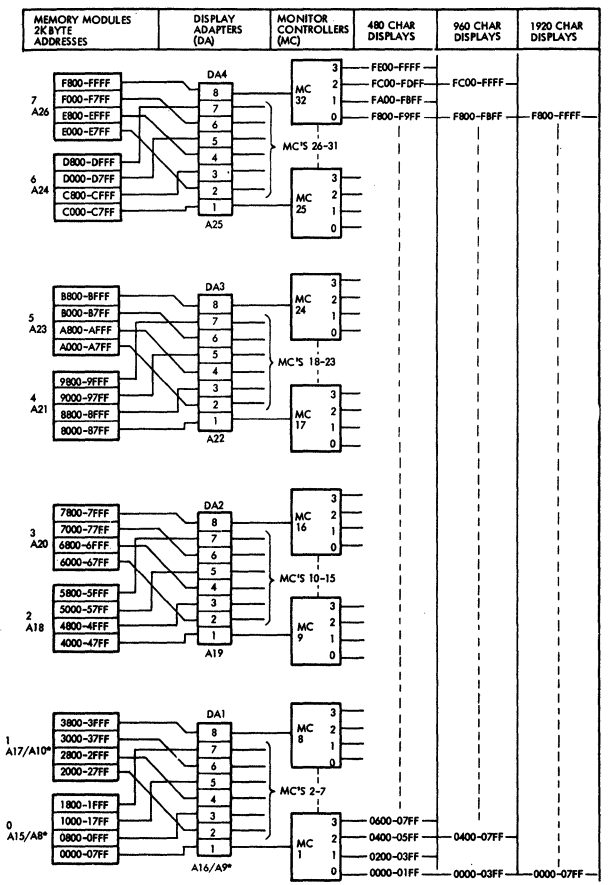
SOFTWARE NOTES FOR 3272 ENHANCED EMULATOR

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, A9 & A10 FOR 1010 & 1015

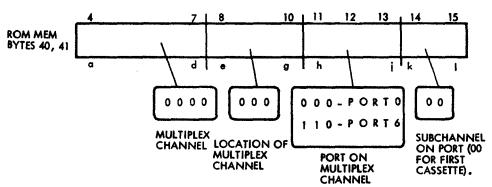
NOTES

ALL DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. IN A MIXED SYSTEM 1920 CH DISPLAYS ARE ASSIGNED BEFORE 480 CH DISPLAYS. ALSO THE STARTING MEMORY ADDRESSES ARE DETERMINED BY WHICH DISPLAY ADAPTERS ARE ASSIGNED TO 1920 CH AND 480 CH DISPLAYS (SEE C4 ON F.B.'A'). IF A SYSTEM IS MIXED OR DOES NOT FULLY LOAD ALL M.C.'s, PRINTER BUFFERS WILL BE ASSIGNED TO THE UNUSED AREAS. IN A MIXED SYSTEM PRINTERS ARE ASSIGNED AS FOLLOWS:

1 CENTRONICS - 1920 CH BUFFER
2 TERMINET - 1920 CH BUFFER
3 CENTRONICS - 480 CH BUFFER
4 TERMINET - 480 CH BUFFER

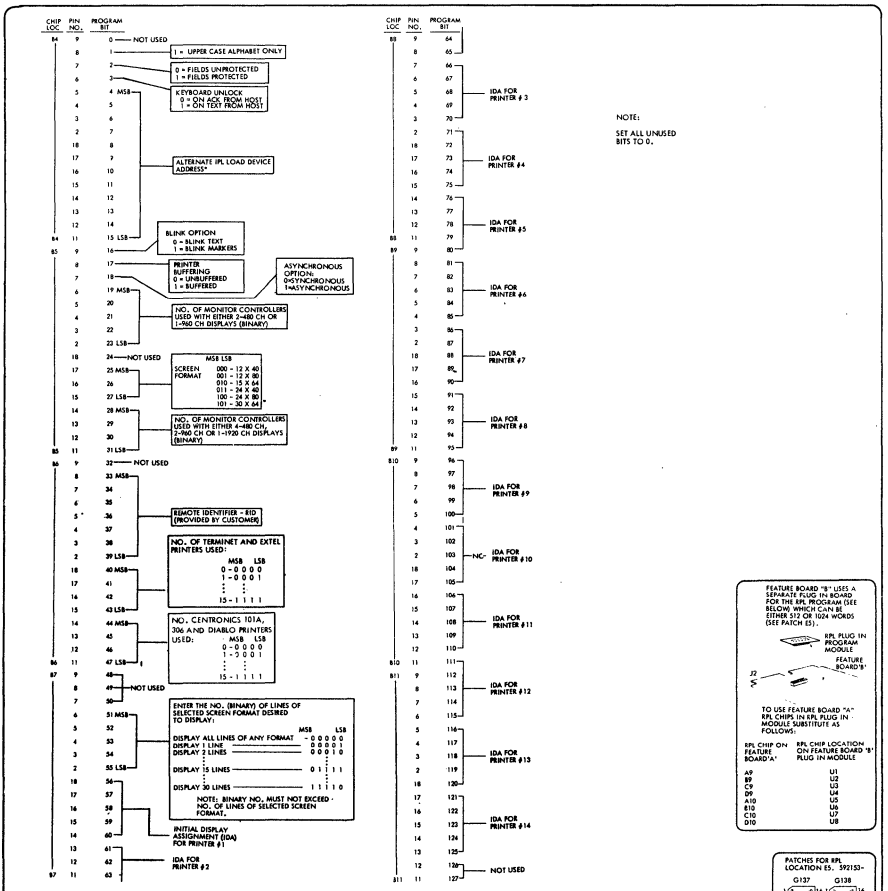
THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULES A17/A10* AND A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

DEVICE ADDRESS ASSIGNMENTS



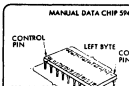
MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR UNISCOPE EMULATOR 933259



*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY

MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUTOFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

MANUAL DATA CHIP LOC.	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
	IPL	512 RPL	1024 RPL
B4	40,41	40,41	40,41
B5	42,43	42,43	42,43
B6	44,45	44,45	44,45
B7	46,47	46,47	46,48
B8	80,81	400,401	800,801
B9	82,83	402,403	802,803
B10	84,85	404,405	804,805
B11	86,87	406,407	806,807

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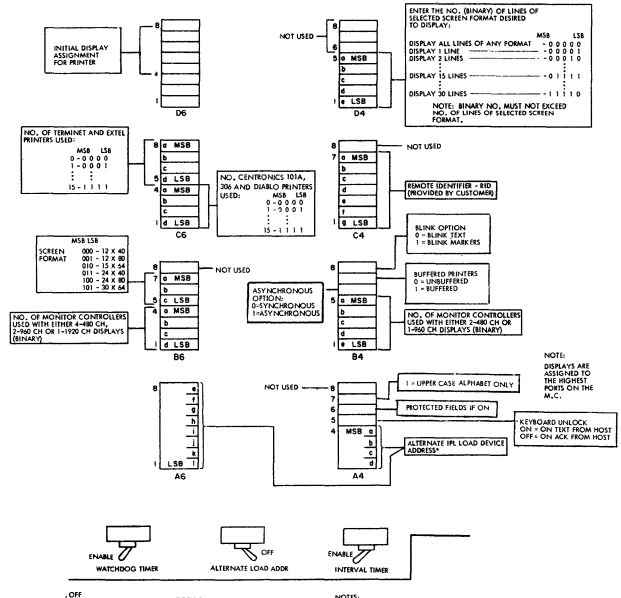
PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR UNISCOPE 100 EMULATOR 933259

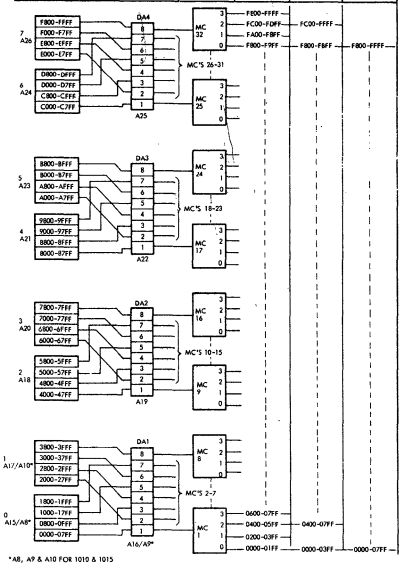


NOTES:

1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY.

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



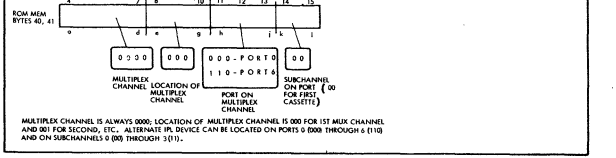
NOTES

DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. FULLY LOADED MC'S ARE ASSIGNED TO HIGHER MEMORY. NEXT MOST FULLY LOADED MC'S ARE ASSIGNED TO NEXT HIGHEST MEMORY, ETC. PRINTER BUFFERS ARE ASSIGNED TO THE MEMORY GAPS LEFT BETWEEN DISPLAY REFRESH AREAS IN DESCENDING ORDER EXAMPLE FOR NO CH DISPLAYS:

DISPLAY 1 } MC
DISPLAY 2 } MC
DISPLAY 3 } MC
PRINTER 1 } MC
DISPLAY 4 } MC
PRINTER 2 } MC
PRINTER 3 } MC
PRINTER 4 } MC

THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

MONITOR CONTROLLER B AND C

CHARACTER/ LINE FORMAT 86 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12	(24)	64 X 15	(30)	OPTIONS
1	—	—	—	—	—	NOTE 1
2	—	—	—	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	OPEN	CLOSED	—
4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
5	CLOSED	CLOSED	CLOSED	OPEN	OPEN	—
6	CLOSED	OPEN	OPEN	OPEN	OPEN	—
7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
8	—	—	—	—	—	NOTE 3

NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER. EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 OUT, A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT			
	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5				
6		See Below		
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.
When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

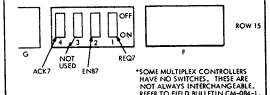
for HI Intensity - close ODD numbered switches and open others.
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MULTIPLEX CHANNEL CONTROLLER

DISABLE/ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.

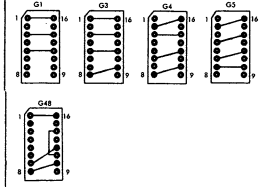


*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-086-11.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS

592153-



FOR THESE DISPLAY CHARACTER/LINE FORMATS	INSERT THESE PATCHES* (592153-)	INTO BOARD LOCATIONS D10 AND J16	
80 X 24		G1	G3
64 X 30 & SPLIT SCREEN		G2	G3
80 X 12		G1	G4
64 X 15 OR 16		G3	G4
40 X 12		G1	G5
40 X 24		G1	G48

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO PRINTER)	1,17	2,18	3,19	4,20	5,21	6,22	7,23	8,24
	33	34	35	36	37	38	39	40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25	10,26	11,27	12,28	13,29	14,30	15,31	16,32
	41	42	43	44	45	46	47	48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PORT 1 AND 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER ARE NOT USED

FIRST PRINTER IS ASSIGNED TO PORT 3 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS

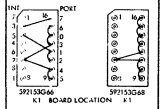
*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEM:			
SEND	0	2	5
REC	0	1	5
PRINTERS:			
1-4	0	3-6	2
5-12	1	0-7	2
13-15	2	0-7	2

NOTE: TERMINET AND EXTEL PRINTERS MUST BE ASSIGNED FIRST

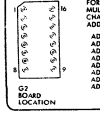
MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



FIRST MULTIPLEX CHANNEL CONTROLLER

2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH



FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

MONITOR CONTROLLER B-16

86 CHIP SWITCH SETTINGS	40 CHAR. 12 LINES	80 CHAR. 12 LINES	64 CHAR. 15/16 LINES	80 CHAR. 24 LINES	64 CHAR. 30 LINES	40 CHAR. 24 LINES	STEP SCAN*
86-1	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	CLOSED
86-2	OPEN	OPEN	OPEN+	OPEN	OPEN	OPEN	OPEN
86-3	OPEN	OPEN	OPEN	CLOSED	CLOSED	CLOSED	CLOSED
86-4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
86-5	CLOSED	OPEN	OPEN	CLOSED	OPEN	CLOSED	**
86-6	CLOSED	OPEN	OPEN	OPEN	OPEN	CLOSED	OPEN
86-7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
86-8***	OPEN	OPEN	OPEN+	OPEN	OPEN	OPEN	OPEN

*USABLE ONLY ON 24 OR 30 LINE FORMAT. SPACING BETWEEN LINES IS ADJUSTABLE BY SETTING R30.

**SET AS INDICATED FOR 24 OR 30 LINE FORMAT.

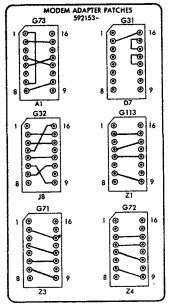
+CLOSED FOR 16 LINE FORMAT

***86-8 IS USED ON SOME MC'S (IT IS USED ON ALL 16 LINE MC'S).

NOTE: WHEN MC IS USED WITH SPLIT SCREEN DISPLAYS A JUMPER IS CONNECTED BETWEEN X12 PIN 15 AND X7 PIN 14.

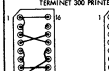
MODEM ADAPTER PATCHES

592153-



MISA PATCHES

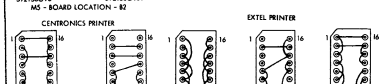
TERMINET 300 PRINTER



NOTE:
SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

CENTRONICS PRINTER

EXTEL PRINTER



EXTEL MODEL	BAUD RATE	PATCHES MS	PATCHES B2
15,30	165	G139	G140
30	150	G128	G101*
30	300	G98*	G101*

*SEE TERMINET 300

PATCH AND SWITCH SETTING FOR UNISCOPE 933259 EMULATOR

CASSETTE PROGRAM PATCH PROCEDURE

1. IPL OLD CASSETTE.
2. DURING IPL STORE X'8XXX' INTO LOCATION 0 (WHERE XXX = DEVICE ADDRESS OF TARGET DRIVE).
3. WHEN IPL IS COMPLETE LOCATION 0 WILL CONTAIN X'0100'. IF NOT RETRY.
4. ENTER PATCHES. DO NOT PRESS STOP OR RESET.
5. PUT A NEW CASSETTE IN TARGET DRIVE.
6. STORE X'8XXX' INTO LOCATION 0 AS ABOVE. LOCATION 0 WILL CHANGE TO X'0300' TO INDICATE THAT THE DUMP IS IN PROGRESS.
7. THE TAPE WILL REWIND AND STOP WHEN COMPLETE AND LOCATION 0 WILL CONTAIN X'0100'. IF MORE COPIES ARE DESIRED RETURN TO STEP 5.
8. IF AN ERROR OCCURS, THE TAPE WILL TRY TO REWRITE CONTINUOUSLY. TO START OVER INSERT A NEW CASSETTE AND STORE X'8XXX' INTO LOCATION 0.

NOTE: FOR ADDITIONAL INFORMATION REFER TO FIB NO. PS-0018.

COMMUNICATIONS REGION (ADDRESS AT LOCATION X'14')

WORD DISPLACEMENT	DEFINITION	
0	REVISION LEVEL (ASCII)	REVISION SUBLEVEL (ASCII)
1	STATISTICS TABLE ADDRESS	
2	ERROR TABLE ADDRESS	
3	LINE CONTROL BLOCK ADDRESS	
4	ADDRESS OF TABLE CONTAINING DST ADDRESSES	
5	RECEIVE BUFFER ADDRESS	
6	ADDRESS OF FIRST XMIT BUFFER	
7	ADDRESS OF SOFTWARE TIMER CELL	

PRINTER STATUS TABLE (PST ADDR IN DST)

WORD DISPLACEMENT	DEFINITION	
0	STATUS	LUN
1	CURRENT PRINT ADDRESS	
2	PRINTER BUFFER ADDRESS	
3	PRINTER TIMER ADDRESS	
4	PRINTER IOCQ ADDRESS	
5	PRINTER STATUS FOR HOST	

ERROR TABLE (ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION
0	MODEM RECEIVE ERROR COUNTER
1	MODEM TRANSMIT ERROR COUNTER
2	SOH IN TEXT ERROR COUNTER
3	ADDRESSING ERROR COUNTER
4	ILLEGAL CHARACTER ERROR COUNTER
5	ESCAPE SEQUENCE ERROR COUNTER
6	CHARACTER PARITY ERROR COUNTER
7	BCC ERROR COUNTER
8	CURSOR ADDRESSING ERROR COUNTERS
9	MODEM RECEIVE IO ACTION ERROR COUNTER

LINE CONTROL BLOCK (LCB ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION	
0	RECEIVE CHANNEL UP/DOWN	
1	CURRENT RECEIVE IOCQ ADDRESS	
2	FIRST RECEIVE IOCQ ADDRESS	
3	.OMPRC RE-ENTRANCE ADDRESS	
4	FIRST MODEM RECEIVE BUFFER ADDRESS	
5	FIRST DST ADDRESS	
6	NUMBER OF DST'S	
7	MODEM RECEIVE TIMER ADDRESS	
8	MODEM RECEIVE LUN	
9	NUMBER OF XMIT BUFFERS AVAILABLE	
A	MODEM XMIT CHANNEL UP/DOWN	
B	MODEM XMIT ERROR FLAG	
C	CURRENT MODEM XMIT IOCQ ADDRESS	
D	FIRST XMIT IOCQ ADDRESS	
E	MODEM XMIT TIMER ADDRESS	
F	INPUT MESSAGE COLLECTION ACTIVE FLAG	
10	MODEM XMIT LUN	
11	MODEM XMIT BUFFER ADDRESS	
12	NOT USED	
13	CURRENT OUTPUT MSG PROCESSOR DST	
14	POLL TIMER ADDRESS	
15	ACK CONTROL BYTE	OUTPUT MESSAGE TYPE
16	SID FROM LAST OUTPUT MSG	DID FROM LAST OUTPUT MESSAGE
17	RID FROM FEATURE BOARD	SID OF LAST INPUT TERMINAL
18	TERMINAL STATUS OF LAST INPUT DEVICE	
19	LAST DST TO RECEIVE INPUT	

DISPLAY STATUS TABLE (FIRST DST ADDR IN LCB)

WORD DISPLACEMENT	DEFINITION	
0	CURSOR ADDRESS	
1	KEYBOARD NUMBER	STATUS
2	LINK TO NEXT DST	
3	HOME ADDRESS	
4	NOT USED	XMIT LUN
5	HOME FOR DEBUG	
6	LED BYTE ADDRESS	
7	CURSOR ADDRESS DURING MESSAGE COLLECTION	
8	PRINTER STATUS TABLE ADDRESS	
9	SOE ADDRESS	
A	SID	PRINTER STATUS
B	DISPLAY END ADDRESS	
C	NUMBER OF CHAR LEFT ON LINE	
	SPECIAL MESSAGE CODE STORAGE FOR RETRANSMIT	NEW U-100 STATUS

STATISTICS TABLE (ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION
0	OUTPUT MESSAGE FROM HOST
1	INPUT MESSAGE TO HOST
2	BROADCAST MESSAGE FROM HOST
3	PRINTER MESSAGE FROM HOST
4	PRINTER STATUS REQUEST FROM HOST
5	MESSAGE WAITING FROM HOST
6	REPLY REQUEST TO HOST
7	RETRANSMIT REQUEST FROM HOST
8	GENERAL POLL FROM HOST
9	SPECIFIC POLL FROM HOST
A	OUTPUT FROM HOST TO ANOTHER RID
B	NO BUSINESS RESPONSE SENT TO HOST
C	MESSAGE WAITING SENT TO HOST
D	PRINTER STATUS SENT TO HOST
E	LOOK-FOR SYNC ISSUED TO MODEM RECEIVE
F	TRAFFIC POLLS W/O ACK
10	TRAFFIC POLLS W/ACK
11	STATUS POLLS W/O ACK
12	STATUS POLLS W/ACK

UNISCOPE EMULATOR 933259 SOFTWARE NOTES

100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR EASTERN AIRLINES UNISCOPE EMULATOR 933325

DA/MC/FB FEATURE BOARD 'B'

CHIP LOC	PIN NO.	CHIP LOC	PIN NO.	PROGRAM BIT
H12†	9	B4	9	0 NOT USED
	8		8	1a MSB
	7		7	2b
	6		6	3c
	5		5	4d
	4		4	5e
	3		3	6f
	2		2	7g
	11		18	8 NOT USED
	12		17	9a MSB
	13		16	10b
	14		15	11c
	15		14	12d
	16		13	13e
	17		12	14f
H12+	18	B4	11	15g
J13	9	B5	9	16*
	8		8	17
	7		7	18
	6		6	19a MSB
	5		5	20b
	4		4	21c
	3		3	22d
	2		2	23e
	11		18	24
	12		17	25 a AIRLINE CODE
	13		16	26b
	14		15	27c
	15		14	28a
	16		13	29b
	17		12	30c
J13	18	B5	11	31d
J14	9	B6	9	32e
	8		8	33a
	7		6	34b
	6		6	35c
	5		5	36d
	4		4	37e
	3		3	38a
	2		2	39b
	11		18	40c
	12		17	41d
	13		16	42e
	14		15	43a
	15		14	44b
	16		13	45c
	17		12	46d
J14	18	B6	11	47e
J15	9	B7	9	48a
	8		8	49b
	7		7	50c
	6		6	51d
	5		5	52e
	4		4	53a
	3		3	54b
	2		2	55c
	11		18	56d
	12		17	57e
	13		16	58a
	14		15	59b
	15		14	60c
	16		13	61d
	17		12	62e
J15	18	B7	11	63a

CHIP LOC	PIN NO.	PROGRAM BIT
B8	9	64b
	8	65c
	7	66d
	6	67e
	5	68a
	4	69b
	3	70c
	2	71d
	18	72e
	17	73a
	16	74b
	15	75c
	14	76d
	13	77e
	12	78a
B8	11	79b
B9	9	80c
	8	81d
	7	82e
	6	83a
	5	84b
	4	85c
	3	86d
	2	87e
	18	88a
	17	89b
	16	90c
	15	91d
	14	92e
	13	93a
	12	94b
B9	11	95c
B10	9	96d
	8	97e
	7	98a
	6	99b
	5	100c
	4	101d
	3	102e
	2	103a
	18	104b
	17	105c
	16	106d
	15	107e
	14	108a
	13	109b
	12	110c
B10	11	111d
B11	9	112e
	8	113a
	7	114b
	6	115c
	5	116d
	4	117e
	3	118a
	2	119b
	18	120c
	17	121d
	16	122e
	15	123a
	14	124b
	13	125c
	12	126d
B11	11	127e

* 8TH DEVICE SID = X'58', 0'130'

* 9TH DEVICE SID = X'59', 0'131'

* 10TH DEVICE SID = X'5A', 0'132'

* 11TH DEVICE SID = X'5B', 0'133'

* 12TH DEVICE SID = X'5C', 0'134'

* 13TH DEVICE SID = X'5D', 0'135'

* 14TH DEVICE SID = X'5E', 0'136'

* 15TH DEVICE SID = X'5F', 0'137'

* 16TH DEVICE SID = X'60', 0'140'

* 17TH DEVICE SID = X'61', 0'141'

* 18TH DEVICE SID = X'62', 0'142'

* 19TH DEVICE SID = X'63', 0'143'

* 20TH DEVICE SID = X'64', 0'144'

REMOTE IDENTIFIER - RID

SET TO X'22' IF PRINTERS, 0 IF NO PRINTERS

ALWAYS 01

DEBUG MODE 1 - LOAD DEBUG

NUMBER OF DEVICES DEFINED AS: 00001 = 1 DEVICE, 00010 = 2, ETC.

a b c	
0 0 0	EASTERN
0 0 1	PIEDMONT
0 1 0	OZARK
0 1 1	HUGHES AIR WEST
1 0 0	SOUTHERN
1 0 1	TEXAS INT.
1 1 0	NATIONAL

1ST DEVICE SID = X'51', 0'121'

2ND DEVICE, SID = X'52', 0'122'

3RD DEVICE SID = X'53', 0'123'

4TH DEVICE SID = X'54', 0'124'

5TH DEVICE SID = X'55', 0'125'

6TH DEVICE SID = X'56', 0'126'

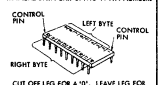
7TH DEVICE SID = X'57', 0'127'

† J12 ON SOME OLDER BOARDS

*SEE NOTES ON BACK SIDE OF THIS SHEET TO CONFIGURE THESE DEVICE FIELDS.

MANUAL DATA CHIP LOC	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)			
DA/MC/FB	FEATURE BOARD B	IPL	512 RPL	1024 RPL
H12 †	B4	40,41	40,41	40,41
J13	B5	42,43	42,43	42,43
J14	B6	44,45	44,45	44,45
J15	B7	46,47	46,47	46,48
	B8	80,81	400,401	800,801
	B9	82,83	402,403	802,882
	B10	84,85	404,405	804,805
	B11	86,87	406,407	806,807

MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:

SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)

SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)

SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE

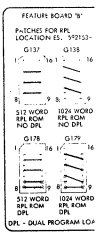
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED
2 CLOSE	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4 OPEN	CLOSE TO DISABLE 1-SEC TONE OPTION.
5 CLOSE	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6 CLOSE	CLOSE FOR BLANKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED
8	CLOSE WHEN 1024 WORD RPL PROGRAM IS USED OPEN WHEN 512 WORD RPL PROGRAM IS USED.

FEATURE BOARD 'B'

PATCHES FOR RPL LOCATION ES - 592153-



DPL - DUAL PROGRAM LOA

DUAL PROGRAM LOAD (DPL) ON FEATURE BOARD 'B' DPL IS DETERMINED BY PATCH ES ON DA/MC/FB IT IS DETERMINED BY A JUMPER NEAR LOC. D6 ON DA/MC/F JUMPER PAD A TO PAD B FOR DPL.

IPL - $\overline{DR}$ • IPL SW + (PB • WDT DO 1 C) - DPL - IPL SW (PB • WDT)

RPL - $\overline{DR}$ • RPLSW + (PB • WD DO 1 C) - DPL - (RPLSW (PB • WDT) - DO 1 C.

IPLSW - IPL SWITCH
RPLSW - RPL SWITCH
PB - IPL PUSHBUTTON
WDT - WATCHDOG TIMER

FEATURE BOARD 'B' AND DA/MC/F USE A SEPARATE PLUG IN BOARD FE THE RPL PROGRAM (SEE BELOW) WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH ES OR SWITCH F

TO USE FEATURE BOARD "A" RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATIO ON FEATURE BOARI PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

PROCEDURE TO SET 5-BIT DEVICE FIELDS

THERE IS ONE FIELD FOR EACH DEVICE.

EACH DEVICE CAN HAVE EITHER A DISPLAY OR PRINTER OR BOTH ATTACHED. EACH PRINTER HAS THE OPTION OF PROVIDING THE LOCAL PRINT FUNCTION FOR OTHER DISPLAYS. THE PROGRAM ASSIGNS THE PRINTERS USED AS LOCAL PRINTERS ASCENDING SEQUENTIAL NUMBERS (1-7) STARTING WITH THE FIRST DEVICE FIELD THAT HAS THE LOCAL PRINT BIT (a) SET TO '1'. THESE NUMBERS ALLOW THE OTHER DISPLAYS TO ADDRESS THE PRINTER FOR LOCAL PRINT.

BIT

a — SET TO '1' WHEN A DISPLAY IS ATTACHED OTHERWISE SET TO '0'.

b — SET TO '1' WHEN A PRINTER IS ATTACHED OTHERWISE SET TO '0'.

BIT

c, d, e (MSB) — ENTER SEQUENTIAL NUMBER OF PRINTER THAT IS TO PROVIDE LOCAL PRINT FUNCTION (SEE EXAMPLE BELOW). WHEN NO LOCAL PRINT FUNCTION IS REQUIRED SET BITS TO 000.

BIT

c — SET TO '1' IF THIS PRINTER IS TO PROVIDE A LOCAL PRINT FUNCTION FOR OTHER DISPLAYS. OTHERWISE SET TO '0'.

PRINTER TYPE

d	0	0	1	1
e	0	1	0	1

- 0 1 — CENTRONICS
- 1 1 — EXTEL, TERMINET

} 80 CHAR LOGICAL LINE LENGTH

- 0 0 — CENTRONICS
- 1 0 — EXTEL, TERMINET

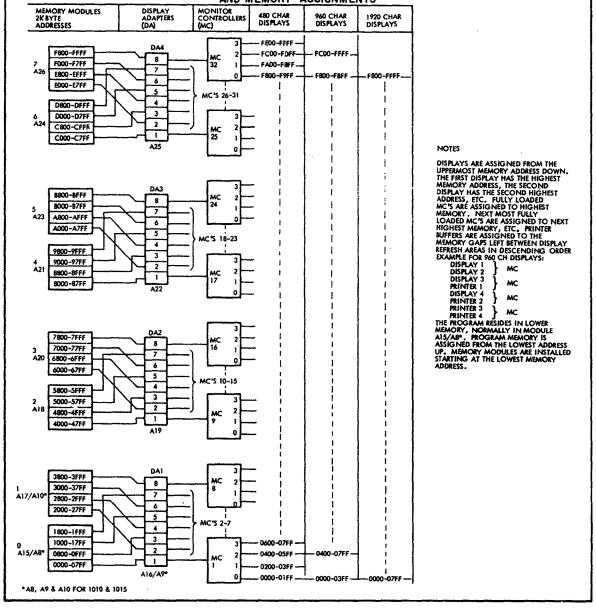
EXAMPLE:

Number of devices = 5

Devices 1 & 2 are displays with printers
Devices 3 & 4 are displays without printers
Device 5 1 printer with no display

	Program Bits		Set to	
	28	a	1	Display
	29	b	1	Printer
DEVICE 1	30	c	1	Used as local printer (first local printer so it is assigned sequential #1).
	31	d	0	EXTEL
	32	e	0	
	33	a	1	Display
	34	b	1	Printer
DEVICE 2	35	c	0	Printer not used for local print (therefore it does not have a sequential #).
	36	d	0	CENTRONICS
	37	e	1	
	38	a	1	Display
	39	b	0	No printer
DEVICE 3	40	c	0	This display uses printer assigned sequential #1 for local print.
	41	d	0	
	42	e	1	
	43	a	1	Display
	44	b	0	No printer
DEVICE 4	45	c	0	This display uses printer assigned sequential #2 for local print.
	46	d	1	
	47	e	0	
	48	a	0	No Display
	49	b	1	Printer
DEVICE 5	50	c	1	Used as local printer (second local printer so it is assigned sequential #2)
	51	d	0	CENTRONICS
	52	e	1	

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, A9 & A10 FOR 1010 & 1015

NOTES

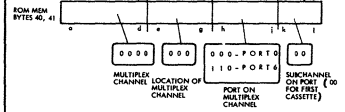
DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. FULLY LOADED MC'S ARE ASSIGNED TO HIGHEST MEMORY. NEXT MOST FULLY LOADED MC'S ARE ASSIGNED TO NEXT HIGHEST MEMORY, ETC. PRINTER BUFFERS ARE ASSIGNED TO THE MEMORY GAPS LEFT BETWEEN DISPLAY REFRESH AREAS IN DESCENDING ORDER

EXAMPLE FOR 960 CH DISPLAYS:

DISPLAY 1 } MC
DISPLAY 2 }
DISPLAY 3 } MC
PRINTER 1 }
DISPLAY 4 } MC
PRINTER 2 }
PRINTER 3 } MC
PRINTER 4 }

THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

MONITOR CONTROLLER B AND C

CHARACTER/ LINE FORMAT E6 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12	(24)	64 X 15	(30)	OPTIONS
1	—	—	—	—	—	NOTE 1
2	—	—	—	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	OPEN	CLOSED	—
4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
5	CLOSED	CLOSED	CLOSED	OPEN	OPEN	—
6	CLOSED	OPEN	OPEN	OPEN	OPEN	—
7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
8	—	—	—	—	—	NOTE 3

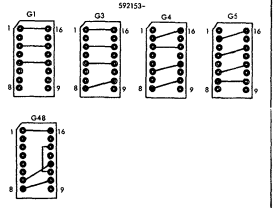
NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER. EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 EXT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS

592153-



FOR THESE DISPLAY CHAR/LINES NO. OF LINES FORMATS	INSERT THESE PATCHES* (SYSTEM 4	INTO BOARD LOCATIONS D15 AND J16	
80 X 24		G1	G3
64 X 30 & SPLIT SCREEN		G2	G4
80 X 12		G1	G4
64 X 15 OR 16		G2	G4
40 X 12		G1	G5
40 X 24		G1	G48

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(D) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO PRINTER)	1,17	2,18	3,19	4,20	5,21	6,22	7,23	8,24
	33	34	35	36	37	38	39	40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25	10,26	11,27	12,28	13,29	14,30	15,31	16,32
	41	42	43	44	45	46	47	48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PORT 1 AND 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER ARE NOT USED

FIRST PRINTER IS ASSIGNED TO PORT 3 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.,	PORT NO.,	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEM:			
SEND	0	2	5
REC	0	1	5
PRINTERS:			
1–4	0	3–6	2
5–12	1	0–7	2
13–15	2	0–7	2

NOTE: TERMINET AND EXTEL PRINTERS MUST BE ASSIGNED FIRST

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT			
	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5	See Below			
6				
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.

When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

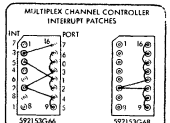
These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.

for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1; Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

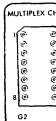
MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



FIRST MULTIPLEX CHANNEL CONTROLLER

2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH



FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

MONITOR CONTROLLER I CONFIGURATION CONTROL MANUAL DATA

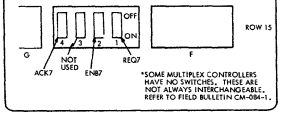
CHIP OR SETTINGS

	GROUND DO NOT CUT	1	18	CUT FOR BOX TYPE CURSOR DON'T CUT FOR UNDERLINE CURSOR ? CURSOR
TONE	CUT TO ACTIVATE TONE ON SET & RESET TRANSITION. DON'T CUT TO ACTIVATE TONE ON SET TRANSITION.	2	17	CUT FOR 64 × 15, 16, 30 DISPLAY FORMATS DON'T CUT FOR 40 & 80 × 12 & 24 DISPLAY FORMATS
	CUT FOR HDL, 1 SEC TONE. DON'T CUT FOR 1 SEC TONE.	3	16	CUT FOR DISPLAY POWER ON LED OPTION. DON'T CUT WHEN OPTION IS NOT USED.
DISPLAY FORMAT	CUT FOR 40 × 12 OR 24, 64 × 15 OR 30, 80 × 12 OR 24 DISPLAY FORMATS. DON'T CUT FOR 64 × 16 DISPLAY FORMAT.	4	15	NOT USED
	NOT USED	5	14	NOT USED
DATA FIELD	CUT FOR A BLANK DATA FIELD. DON'T CUT FOR A BLINKING DATA FIELD.	6	13	CUT TO DISPLAY 32-64 CHAR TYPES ON 9 SCAN LINES AND 64 CHAR TYPES ON 8 SCAN LINES. DON'T CUT TO DISPLAY ALL CHAR'S ON 9 SCAN LINES.
	CUT FOR PROGRAM CONTROLLED UNDERLINE DON'T CUT.	7	12	CUT FOR 40 × 12 AND 40 × 24 DISPLAY FORMATS DON'T CUT FOR 64 × 15, 16, 30 AND 80 × 12, 24 DISPLAY FORMATS.
	CUT FOR NORMAL - LOW INTENSITY DATA FIELD. DON'T CUT FOR NORMAL - HIGH INTENSITY DATA FIELD.	8	11	CUT FOR 40 × 12, 64 × 15 OR 16 AND 80 × 12 DISPLAY FORMATS. DON'T CUT FOR 40 × 24, 64 × 30 OR 80 × 24 DISPLAY FORMATS.
NO. OF CHARACTERS DISPLAYED	CUT TO USE 96 DISPLAYABLE CHAR'S. DON'T CUT TO USE 128 DISPLAYABLE CHAR'S.	9	10	GROUND DO NOT CUT

MULTIPLEX CHANNEL CONTROLLER

DISABLE/ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

MONITOR CONTROLLER B-16

16 CHIP SWITCH SETTING	40 CHAR. 12 LINES	80 CHAR. 12 LINES	64 CHAR. 15/16 LINES	80 CHAR. 24 LINES	64 CHAR. 30 LINES	40 CHAR. 24 LINES	STEP SCAN*
16-1	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	CLOSED
16-2	OPEN	OPEN	OPEN'	OPEN	OPEN	OPEN	OPEN
16-3	OPEN	OPEN	OPEN	CLOSED	CLOSED	CLOSED	CLOSED
16-4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
16-5	CLOSED	OPEN	OPEN	CLOSED	OPEN	CLOSED	**
16-6	CLOSED	OPEN	OPEN	OPEN	OPEN	CLOSED	OPEN
16-7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
16-8#	OPEN	OPEN	OPEN'	OPEN	OPEN	OPEN	OPEN

*USABLE ONLY ON 24 OR 30 LINE FORMAT. SPACING BETWEEN LINES IS ADJUSTABLE BY SETTING R25.

** SET AS INDICATED FOR 24 OR 30 LINE FORMAT.

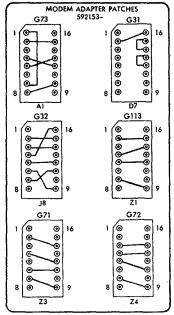
' CLOSED FOR 16 LINE FORMAT

#16-8 IS USED ON SOME MC'S (IT IS USED ON ALL 16 LINE MC'S.

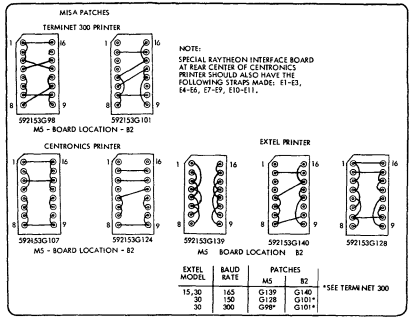
NOTE: WHEN MC IS USED WITH SPLIT SCREEN DISPLAYS A JUMPER IS CONNECTED BETWEEN K12 PIN 15 AND K7 PIN 14.

MODEM ADAPTER PATCHES

592153-



MISA PATCHES



NOTE:
SPECIAL BAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

EXTEL MODEL	BAUD RATE	PATCHES MS	PATCHES B2
15,30	165	G139	G140
30	150	G128	G101*
30	300	G98*	G101*

*SEE TERMINET 300

PATCH AND SWITCH SETTING FOR EASTERN AIRLINES UNISCOPE 933325 EMULATOR

JANUARY 1977
44-10118
SHEET 3 OF 4

DEBUG PROGRAM DIRECTIVES

(DEBUG FEATURE BOARD SWITCH MUST BE SET "ON" TO USE DIRECTIVE)

.DEBUG	ENABLE DEBUG MODE
XX	DISABLE DEBUG MODE
HA(A), (B)	ADD A + B
HS(A), (B)	SUBTRACT A-B
TR(LOC), (AC), (X1), (X2), (CB)	LOAD REGISTER AND TRANSFER
PA(LOC), (VAL1), (VAL2), . . .	PATCH LOC TO VAL1, LOC+2 TO VAL2, ETC.
CK(VAL), (VAL), . . .	COMPUTE CHECKSUM
WI	DISPLAY RID, SID, HOME ADDRESS, AND DST NUMBER
IS	INITIALIZE STATISTICS TABLE AND ERROR TABLE
CT (UNIT)	CREATE TAPE ON SPECIFIED MUX/PORT/ XPORT (DEFAULT IS 0/0/0)
CS (DST1), (DST2), . . .	CONNECT SCREENS FOR SRM
SL (LEVEL 1), (LEVEL 2), . . .	LEVEL 5: 1 MAIN LOOP 2 .OMPRC ENTRANCE 3 .OMPRC TEXT ROUTINE 4 .IMPRC IOACT RETURN 5 MODEM RECEIVE IOACT RETURN 7 .IMPRC TASK BRANCH 8 MODEM RECEIVE LINE RESTART 10 RECEIVE ERROR 11 TRANSMIT ERROR 12 SOH IN TEXT ERROR 13 ADDRESSING ERROR 14 CHARACTER ERROR 15 ESCAPE SEQUENCE ERROR 17 BCC ERROR 18 SET CURSOR ERROR
SY	SRM ON
SN	SRM OFF
AY	MONITOR ALL RECORDS
AN	IGNORE ALL RECORDS
TY (X)	MONITOR ALL RECORDS OF TYPE (X)
TN (X)	IGNORE ALL RECORDS OF TYPE (X)
WY (X) (W)	MONITOR WORD (W) OF ALL RECORDS OF TYPE (X)
WN (X) (W)	IGNORE WORD (W) OF ALL RECORDS OF TYPE (X)
DY (ZZ)	MONITOR ALL RECORDS FOR DEVICE (ZZ)
DN (ZZ)	IGNORE ALL RECORDS FOR DEVICE (ZZ)
ML (LOC)	MONITOR LOCATION SPECIFIED BY LOC (TYPE IS 'Z')
1Y	ONE SHOT MODE ON
1N	ONE SHOT MODE OFF
PS	PRINT ALL CONNECTED SCREENS
PX	STOP ALL PRINT OPERATIONS
RS	CLEAR ALL SRM SCREENS

CASSETTE PROGRAM PATCH PROCEDURE

1. IPL OLD CASSETTE.
2. DURING IPL STORE X'8XXX' INTO LOCATION 0 (WHERE XXX = DEVICE ADDRESS OF TARGET DRIVE).
3. WHEN IPL IS COMPLETE LOCATION 0 WILL CONTAIN X'0100'. IF NOT RETRY.
4. ENTER PATCHES. DO NOT PRESS STOP OR RESET.
5. PUT A NEW CASSETTE IN TARGET DRIVE.
6. STORE X'8XXX' INTO LOCATION 0 AS ABOVE. LOCATION 0 WILL CHANGE TO X'0300' TO INDICATE THAT THE DUMP IS IN PROGRESS.
7. THE TAPE WILL REWIND AND STOP WHEN COMPLETE AND LOCATION 0 WILL CONTAIN X'0100'. IF MORE COPIES ARE DESIRED RETURN TO STEP 5.
8. IF AN ERROR OCCURS, THE TAPE WILL TRY TO REWRITE CONTINUOUSLY. TO START OVER INSERT A NEW CASSETTE AND STORE X'8XXX' INTO LOCATION 0.

NOTE: FOR ADDITIONAL INFORMATION REFER TO FIB NO. PS-0018.

COMMUNICATIONS REGION (ADDRESS AT LOCATION X'C')

WORD DISPLACEMENT	DEFINITION
0	REVISION LEVEL (ASCII) | REVISION SUBLEVEL (ASCII)
1	STATISTICS TABLE ADDRESS
2	ERROR TABLE ADDRESS
3	LINE CONTROL BLOCK ADDRESS
4	ADDRESS OF TABLE CONTAINING DST ADDRESSES
5	RECEIVE BUFFER ADDRESS
6	ADDRESS OF FIRST XMIT BUFFER
7	ADDRESS OF SOFTWARE TIMER CELL

PRINTER STATUS TABLE (PST ADDR IN DST)

WORD DISPLACEMENT	DEFINITION
0	STATUS | LUN
1	CURRENT PRINT ADDRESS
2	PRINTER BUFFER ADDRESS
3	PRINTER TIMER ADDRESS
4	PRINTER IOCQ ADDRESS
5	PRINTER STATUS FOR HOST

ERROR TABLE (ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION
0	MODEM RECEIVE ERROR COUNTER
1	MODEM TRANSMIT ERROR COUNTER
2	SOH IN TEXT ERROR COUNTER
3	ADDRESSING ERROR COUNTER
4	ILLEGAL CHARACTER ERROR COUNTER
5	ESCAPE SEQUENCE ERROR COUNTER
6	CHARACTER PARITY ERROR COUNTER
7	BCC ERROR COUNTER
8	CURSOR ADDRESSING ERROR COUNTERS
9	MODEM RECEIVE IO ACTION ERROR COUNTER

LINE CONTROL BLOCK (LCB ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION
0	RECEIVE CHANNEL UP/DOWN
1	CURRENT RECEIVE IOCQ ADDRESS
2	FIRST RECEIVE IOCQ ADDRESS
3	.OMPRC RE-ENTRANCE ADDRESS
4	FIRST MODEM RECEIVE BUFFER ADDRESS
5	FIRST DST ADDRESS
6	NUMBER OF DST'S
7	MODEM RECEIVE TIMER ADDRESS
8	MODEM RECEIVE LUN
9	NUMBER OF XMIT BUFFERS AVAILABLE
A	MODEM XMIT CHANNEL UP/DOWN
B	MODEM XMIT ERROR FLAG
C	CURRENT MODEM XMIT IOCQ ADDRESS
D	FIRST XMIT IOCQ ADDRESS
E	MODEM XMIT TIMER ADDRESS
F	INPUT MESSAGE COLLECTION ACTIVE FLAG
10	MODEM XMIT LUN
11	MODEM XMIT BUFFER ADDRESS
12	NOT USED
13	CURRENT OUTPUT MSG PROCESSOR DST
14	POLL TIMER ADDRESS
15	ACK CONTROL BYTE | OUTPUT MESSAGE TYPE
16	SID FROM LAST OUTPUT MSG | DID FROM LAST OUTPUT MESSAGE
17	RID FROM FEATURE BOARD | SID OF LAST INPUT TERMINAL
18	TERMINAL STATUS OF LAST INPUT DEVICE

DISPLAY STATUS TABLE (FIRST DST ADDR IN LCB)

WORD DISPLACEMENT	DEFINITION
0	LINK TO NEXT DST
1	KEYBOARD NUMBER | STATUS
2	CURSOR ADDRESS
3	HOME ADDRESS
4	NOT USED | XMIT LUN
5	HOME FOR DEBUG
6	LED BYTE ADDRESS
7	CURSOR ADDRESS DURING MESSAGE COLLECTION
8	PRINTER STATUS TABLE ADDRESS
9	SOE ADDRESS
A	SID | PRINTER STATUS
B	DISPLAY END ADDRESS
C	NUMBER OF CHAR LEFT ON LINE

STATISTICS TABLE (ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION
0	OUTPUT MESSAGE FROM HOST
1	INPUT MESSAGE TO HOST
2	BROADCAST MESSAGE FROM HOST
3	PRINTER MESSAGE FROM HOST
4	PRINTER STATUS REQUEST FROM HOST
5	MESSAGE WAITING FROM HOST
6	REPLY REQUEST TO HOST
7	RETRANSMIT REQUEST FROM HOST
8	GENERAL POLL FROM HOST
9	SPECIFIC POLL FROM HOST
A	OUTPUT FROM HOST TO ANOTHER RID
B	NO BUSINESS RESPONSE SENT TO HOST
C	MESSAGE WAITING SENT TO HOST
D	PRINTER STATUS SENT TO HOST
E	LOOK-FOR SYNC ISSUED TO MODEM RECEIVE

SRM	NODE DEFINITION
+0	LINK TO NEXT (0=END OF LIST)
+2	ADDRESS TO START TRACE (LSB ON = INDIRECT)
+4	NUMBER OF BYTES TO TRACE
+6	DEVICE ID (BINARY)
+7	NODE ID (ASCII) — DISPLAYED ON TRACE TO IDENTIFY ENTRY
+8	TRACE MASK*
+A to A+n	SCRATCH AREA WHERE n = NO. OF BYTES TO TRACE

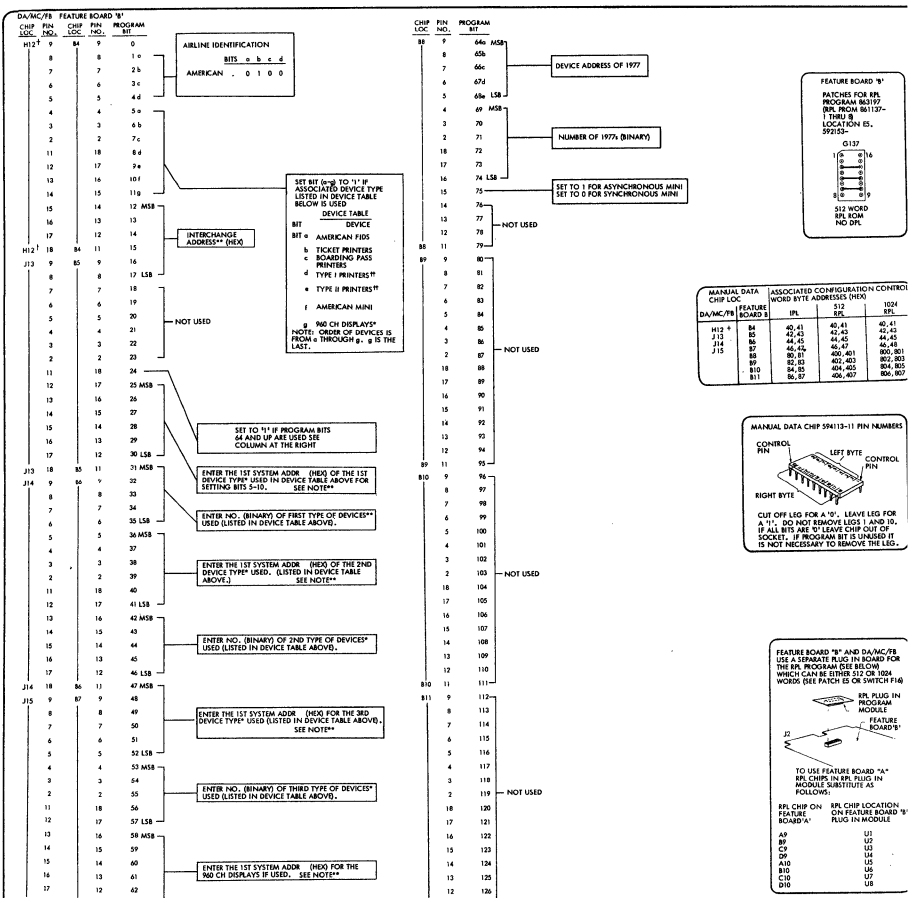
*MASK - BIT 0 = 1 SKIP THIS NODE.
BITS 1-15 = 1 SKIP CORRESPONDING WORD (i.e., bit 15 = word 0, bit 14 = word 1)

SRM NODE TYPES

A	MODEM XMIT BUFFER
B	MODEM RECEIVE BUFFER
C	MODEM XMIT PCB
D	MODEM RCV PCB
E	MODEM XMIT PIOT
F	MODEM RECEIVE PIOT
G	MODEM RECEIVE FIOB
H	MODEM XMIT FIOB
I	PRINTER FIOB
J	PRINT BUFFER
K	DISPLAY STATUS TABLE
L	FIRST 16 WORDS OF LCB
M	LAST 9 WORDS OF LCB
P	PRINTER STATUS TABLE
Q	PRINTER IOCQ
R	MODEM RECEIVE IOCQ
S	STATISTICS TABLE
T	MODEM XMIT IOCQ
X	ERROR TABLE
Z	DEFINE BY 'ML' DIRECTIVE

EASTERN AIRLINES UNISCOPE EMULATOR 933325
SOFTWARE NOTES

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR AMERICAN EMULATOR USING THE INITIALIZATION PROGRAM ***



*960 CH DISPLAY ADDR IS ALWAYS ONLY ENTERED IN BITS 58-63.

**REFER TO USER SYSTEM SPECIFICATION OR CONFIGURATION MULTIPLY HOST SYSTEM ADDRESS BY 2 BEFORE ENTERING. SEE EXAMPLES BELOW.

EXAMPLE 1: FOR HOST ADDRESS 01_{16}
21000001 = 000010
ENTER 000010 (02_{16})
LSB

EXAMPLE 2: FOR HOST ADDRESS $0F_{16}$
22001001 = 010010
ENTER 010010 (12_{16})
LSB

†J12 IS ON SOME OLDER BOARDS

††TYPE I PRINTERS ARE: EXTEL 15/30, TERMINET 300/1200, TTY
TYPE II PRINTERS ARE: CENTRONICS 101A/306, TERMINET 30 (W/INTERFACE CARD #)

***

FOR EMULATORS	WHICH SUPPORT:			
TRAVEL AGENT (AXC)	SP (INCL TERM 30)	TP BP	1977	MINI
933284-1	✓	—	—	—
-2	✓	✓	✓	—
-3	✓	—	—	✓
-4	✓	✓	✓	✓
RES (AXA) 863028-1	—	—	—	—
-2 (FIDS)	—	—	—	—
-3	✓	✓	—	—
-4	✓	✓	✓	—
FRS 863401-1	—	—	—	—

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:

SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)

SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)

SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE

SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

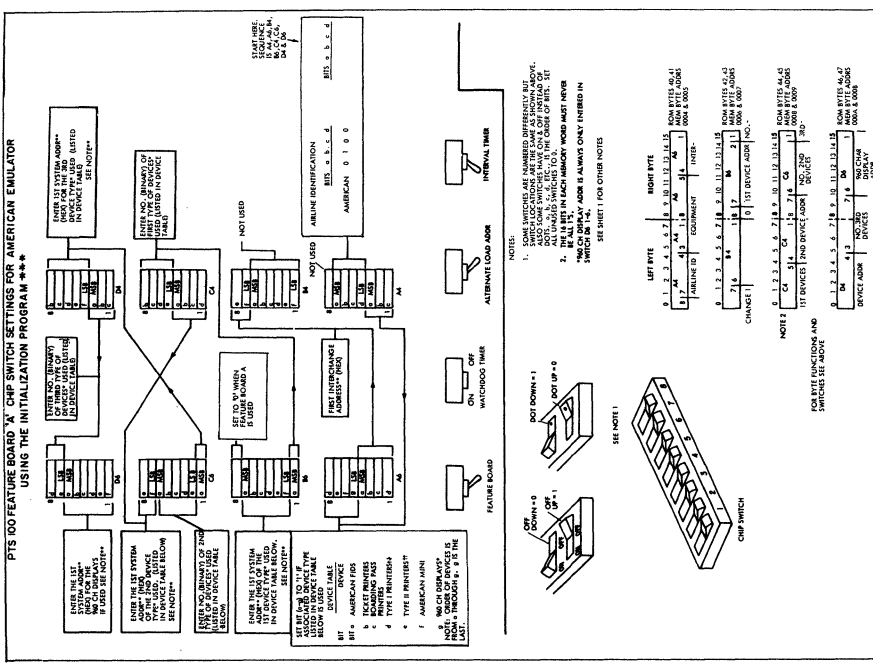
DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

Display Adaptor	Channel	Monitor	1920 Char/Display 80 Ch X 24 Lines 64 Ch X 30 Lines		960 Char/Display 80 Ch X 12 Lines 64 Ch X 15 or 16 Lines		960 Char/Display 40 Ch X 24 Lines		480 Char/Display 40 Ch X 12 Lines	
			Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address
1	1	0	0000-07FF	81	0000-03FF	81	0000-03FF	81	0000-01FF	81
		1					0400-07FF	A1	0200-03FF	A1
		2			0400-07FF	C1			0400-05FF	C1
		3							0600-07FF	E1
	3	0	0800-0FFF	89	0800-0BFF	89	0800-0BFF	89	0800-09FF	89
		1					0C00-0FFF	A9	0A00-0BFF	A9
		2			0C00-0FFF	C9			0C00-0DFF	C9
		3							0E00-0FFF	E9
	5	0	1000-17FF	91	1000-13FF	91	1000-13FF	91	1000-11FF	91
		1					1400-17FF	B1	1200-13FF	B1
		2			1400-17FF	D1			1400-15FF	D1
		3							1600-17FF	F1
	7	0	1800-1FFF	99	1800-1BFF	99	1800-1BFF	99	1800-19FF	99
		1					1C00-1FFF	B9	1A00-1BFF	B9
		2			1C00-1FFF	D9			1C00-1DFF	D9
		3							1E00-1FFF	F9
	2	0	0200-27FF	85	2000-23FF	85	2000-23FF	85	2000-21FF	85
		1					2400-27FF	A5	2200-23FF	A5
		2			2400-27FF	C5			2400-25FF	C5
		3							2600-27FF	E5
	4	0	2800-2FFF	8D	2800-2BFF	8D	2800-2BFF	8D	2800-29FF	8D
		1					2C00-2FFF	AD	2A00-2BFF	AD
		2			2C00-2FFF	CD			2C00-2DFF	CD
		3							2E00-2FFF	ED
	6	0	2000-37FF	95	3000-33FF	95	3000-33FF	95	3000-31FF	95
		1					3400-37FF	B5	3200-33FF	B5
		2			3400-37FF	D5			3400-35FF	D5
		3							3600-37FF	F5
	8	0	3800-3FFF	9D	3800-3BFF	9D	3800-3BFF	9D	3800-39FF	9D
		1					3C00-3FFF	BD	3A00-39FF	BD
		2			3C00-3FFF	DD			3C00-3DFF	DD
		3							3E00-3FFF	FD
2	1	0	4000-47FF	82	4000-43FF	82	4000-43FF	82	4000-41FF	42
		1					4400-47FF	A2	4200-43FF	A2
		2			4400-47FF	C2			4400-45FF	C2
		3							4600-47FF	E2
	3	0	4800-4FFF	8A	4800-4BFF	8A	4800-4BFF	8A	4800-49FF	8A
		1					4C00-4FFF	AA	4A00-4BFF	AA
		2			4C00-4FFF	CA			4C00-4DFF	CA
		3							4E00-4FFF	EA
	5	0	5000-57FF	92	5000-53FF	92	5000-53FF	92	5000-51FF	92
		1					5400-57FF	B2	5200-53FF	B2
		2			5400-57FF	D2			5400-55FF	D2
		3							5600-57FF	F2
	7	0	5800-5FFF	9A	5800-5BFF	9A	5800-5BFF	9A	5800-59FF	9A
		1					5C00-5FFF	BA	5A00-5BFF	BA
		2			5C00-5FFF	DA			5C00-5DFF	DA
		3							5E00-5FFF	FA
	2	0	6000-67FF	86	6000-63FF	86	6000-63FF	86	6000-61FF	86
		1					6400-67FF	A6	6200-63FF	A6
		2			6400-67FF	C6			6400-65FF	C6
		3							6600-67FF	E6
	4	0	6800-6FFF	8E	6800-6BFF	8E	6800-6BFF	8E	6800-69FF	8E
		1					6C00-6FFF	AE	6A00-6BFF	AE
		2			6C00-6FFF	CE			6C00-6DFF	CE
		3							6E00-6FFF	EE
	6	0	7000-77FF	96	7000-73FF	96	7000-73FF	96	7000-71FF	96
		1					7400-77FF	B6	7200-73FF	B6
		2			7400-77FF	D6			7400-75FF	D6
		3							7600-77FF	F6
	8	0	7800-7FFF	9E	7800-7BFF	9E	7800-79FF	9E	7800-79FF	9E
		1					7C00-7FFF	BE	7A00-7BFF	BE
		2			7C00-7FFF	DE			7C00-7DFF	DE
		3							7E00-7FFF	FE
3	1	0	8000-87FF	83	8000-83FF	83	8000-83FF	83	8000-81FF	83
		1					8400-87FF	A3	8200-83FF	A3
		2			8400-87FF	C3			8400-85FF	C3
		3							3600-87FF	E3
	3	0	8800-8FFF	8B	8800-8BFF	8B	8800-8BFF	8B	8800-89FF	8B
		1					8C00-8FFF	AB	8A00-8BFF	CB
		2			8C00-8FFF	CB			8C00-8DFF	EB
		3							8E00-8FFF	EB
	5	0	9000-97FF	93	9000-93FF	93	9000-93FF	93	9000-91FF	93
		1					9400-97FF	B3	9200-93FF	B3
		2			9400-97FF	D3			9400-95FF	D3
		3							9600-97FF	F3
	7	0	9800-9FFF	9B	9800-9BFF	9B	9800-9BFF	9B	9800-99FF	9B
		1					9C00-9FFF	B8	9A00-9BFF	BB
		2			9C00-9FFF	DB			9C00-9DFF	DB
		3							9E00-9FFF	FB
	2	0	A000-A7FF	87	A000-A3FF	87	A000-A3FF	87	A000-A1FF	87
		1					A400-A7FF	A7	A200-A3FF	A7
		2			A400-A7FF	C7			A400-A5FF	C7
		3							A600-A7FF	E7
	4	0	A800-AFFF	8F	A800-ABFF	8F	A800-ABFF	8F	A800-A9FF	8F
		1					AC00-AFFF	AF	AA00-ABFF	AF
		2			AC00-AFFF	CF			AC00-ADFF	CF
		3							AE00-AFFF	FF
	6	0	B000-B7FF	97	B000-B3FF	97	B000-B3FF	97	B000-B1FF	97
		1					B400-B7FF	B7	B200-B3FF	B7
		2			B400-B7FF	D7			B400-B5FF	D7
		3							B600-B7FF	F7
	8	0	B800-BFFF	9F	B800	9F	B800-BBFF	9F	B800-B9FF	9F
		1					BC00-BFFF	BF	BA00-BBFF	BF
		2			BC00-BFFF	DF			BC00-BDFF	DF
		3							BE00-BFFF	FF
4	1	0	C000-C7FF	84	C000-C3FF	84	C000-C3FF	84	C000-C1FF	84
		1					C400-C7FF	A4	C200-C3FF	A4
		2			C400-C7FF	C4			C400-C5FF	C4
		3							C600-C7FF	E4
	3	0	C800-CFFF	8C	C800-CBFF	8C	C800-CBFF	8C	C800-C9FF	8C
		1					CC00-CFFF	AC	CA00-CBFF	AC
		2			CC00-CFFF	CC			CC00-CDFF	CC
		3							CE00-CFFF	EC
	5	0	D000-D7FF	94	D000-D3FF	94	D000-D3FF	94	D000-D1FF	94
		1					D400-D7FF	B4	D200-D3FF	B4
		2			D400-D7FF	D4			D400-D5FF	D4
		3							D600-D7FF	F4
	7	0	D800-DFFF	9C	D800-DBFF	9C	D800-DBFF	9C	D800-D9FF	9C
		1					DC00-DFFF	BC	DA00-DBFF	BC
		2			DC00-DFFF	DC			DC00-DDFF	DC
		3							DE00-DFFF	FC
	2	0	E000-E7FF	88	E000-E3FF	88	E000-E3FF	88	E000-E1FF	88
		1					E400-E7FF	A8	E200-E3FF	A8
		2			E400-E7FF	C8			E400-E5FF	C8
		3							E600-E7FF	E8
	4	0	E800-EFFF	90	E800-E8FF	90	E800-EBFF	90	E800-E9FF	90
		1					EC00-EFFF	B0	EA00-EBFF	B0
		2			EC00-EFFF	D0			EC00-EDFF	D0
		3							EE00-EFFF	F0
	6	0	F000-F7FF	98	F000-F3FF	98	F000-F3FF	98	FF00-F1FF	98
		1					F400-F7FF	B8	F200-F3FF	B8
		2			F400-F7FF	D8			F400-F5FF	D8
		3							F600-F7FF	F8
	8	0	F800-FFFF	A0	F800-FBFF	A0	F800-FBFF	A0	F800-FBFF	A0
		1					FC00-FFFF	C0	FA00-FBFF	C0
		2			FC00-FFFF	E0			FC00-FDFF	E0
		3							FE00-FFFF	80

DISPLAY DATA MEMORY BUFFER ASSIGNMENTS

JANUARY 1977
44-10119
SHEET 2 OF 4



DEVICE ADDRESS & INTERRUPT ASSIGNMENTS

DEVICE	MUX	MUX PORT	INT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEM ADAPTERS			
2331 PARS RX	0	4	5
PARS TX	0	5	4
2341 MINI RX	0	1	2 } TAPE 933284
MINI TX	0	2	2 } -3 OR -4 ONLY
PRINTERS	0 1 2	1-3,6 0-7 0-7	
1977	0 1 2	USED WITH TAPE 933284-2,-4 SEE NOTE BELOW (PRINTER ASSIGNED FIRST)	

NOTE: THE 1977 REQUIRES AN AMA MODEM ADAPTER THAT IS CONNECTED TO 2 PORTS ON THE SAME MUX, STARTING WITH THE LOWEST NUMBERED PORT AVAILABLE SEE EXAMPLES BELOW.

XAMPLE 1:

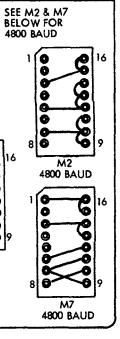
		CASSETTE		MODEM				
MUX 0	PORTS	0	1 2 3	4 5	6	7		
			SP TP	1ST 1977		KYBD		
MUX 1	PORTS	0 1	2 3	4 5	6 7			
		2ND 1977	3RD 1977	4TH 1977	5TH 1977			

XAMPLE 2:

		CASSETTE	1ST 1977			UNUSED	
MUX 0	PORTS	0	1 2 3	4 5	6 7		
			TP	MODEM			
MUX 1	PORTS	0 1	2 3	4 5	6 7		
		2ND 1977	3RD 1977	4TH 1977	5TH 1977		

PTS/MINI PATCHES

FOR THIS MINI MODEM ADAPTER	INSERT THESE PATCHES (592153-) INTO THE LOCATIONS SHOWN
ASYNCH AMA 2341 591725	M2-G59, M7-G58 } 1200 BAUD — SEE M2 & M7 BELOW FOR 4800 BAUD L2-G65 G4-G225 E8-G227 F8-TBR (7 BITS, EVEN PARITY, 2 STOP BITS)
SYNCH CTMC 2332 591707	A1-G73 D7-G31 J8-G32 Z1-G113 Z3-G71 Z4-G72



PTS/1977 PATCHES

INSERT PATCHES (592153-) INTO THE LOCATIONS SHOWN

G223-M7
G222-M2
G65-L2
G225-G4
G226-F8
G227-E8

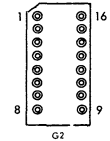
IPARS MODEM ADAPTER PATCHES

INSERT THESE PATCH PLUGS INTO BOARD LOCATIONS K6 AND A2

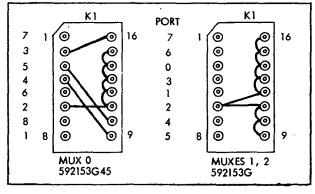
592153G170 592153G147

MULTIPLEX CHANNEL CONTROLLER KEYBOARD, INTERRUPT AND ADDRESS PATCHES

MUX ADDRESS PATCH



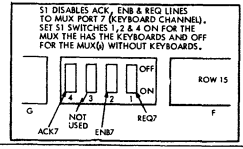
INTERRUPT PATCHES



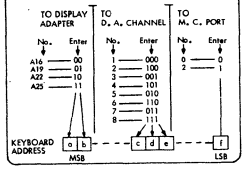
*ADDRESS OF MUX CHAN.

1 OR 4 TO 16 - ADDR 000
1 OR 4 TO 12 - ADDR 001
1 OR 4 TO 14 - ADDR 010
1 OR 4 TO 10 - ADDR 011
1 OR 4 TO 15 - ADDR 100
1 OR 4 TO 11 - ADDR 101
1 OR 4 TO 13 - ADDR 110
1 OR 4 TO 9 - ADDR 111

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1,2 & 4 ON FOR THE MUX THAT HAS THE KEYBOARDS AND OFF FOR THE MUX(s) WITHOUT KEYBOARDS.



KEYBOARD ADDRESS COMPUTATION

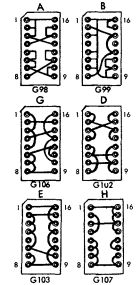


IPARS SYSTEM CONFIGURATION VARIABLE PATCHES, SWITCHES AND REMOTE PRINTER ADDRESSES

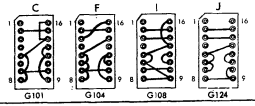
MULTI-INTERFACE SERIAL ADAPTER (MISA) PATCHING (592153-)

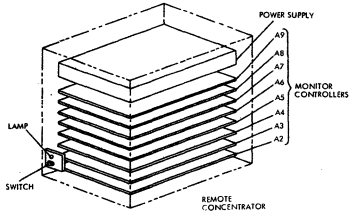
INSERT THESE PATCHES FOR THIS MODEL MISA 593296-	M5	B2
G1 TERMINET 300 BAUD	A	C
G3 TERMINET 1200 BAUD	B	C
G5 TTY 110 BAUD	G	F
G7 TTY 50 BAUD	D	F
G9 TTY 75 BAUD	E	F
G11 TICKET & BOARDING PASS PRINTER	H	I
CENTRONICS	H	J
TERMINET 30	A	J

M5 PATCH CONFIGURATIONS (BAUD RATES)

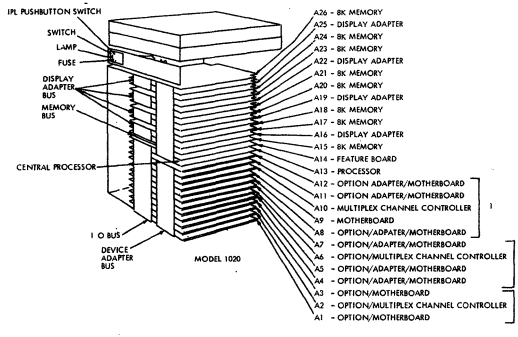


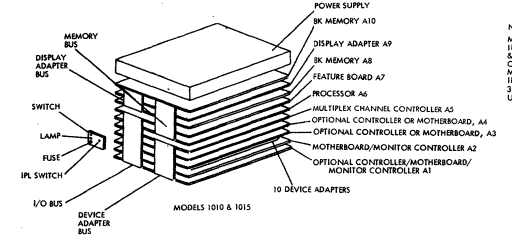
B2 PATCH CONFIGURATIONS (CONTROL)





POWER SUPPLIES





NOTE:
MONITOR CONTROLLERS ARE INSTALLED IN SLOTS A1, A2, A3 & A4 WHEN ONLY 2 MULTIPLEX CONTROLLERS ARE USED. MONITOR CONTROLLERS ARE INSTALLED IN A7, A8 & A9 WHEN 3 MULTIPLEX CONTROLLERS ARE USED.

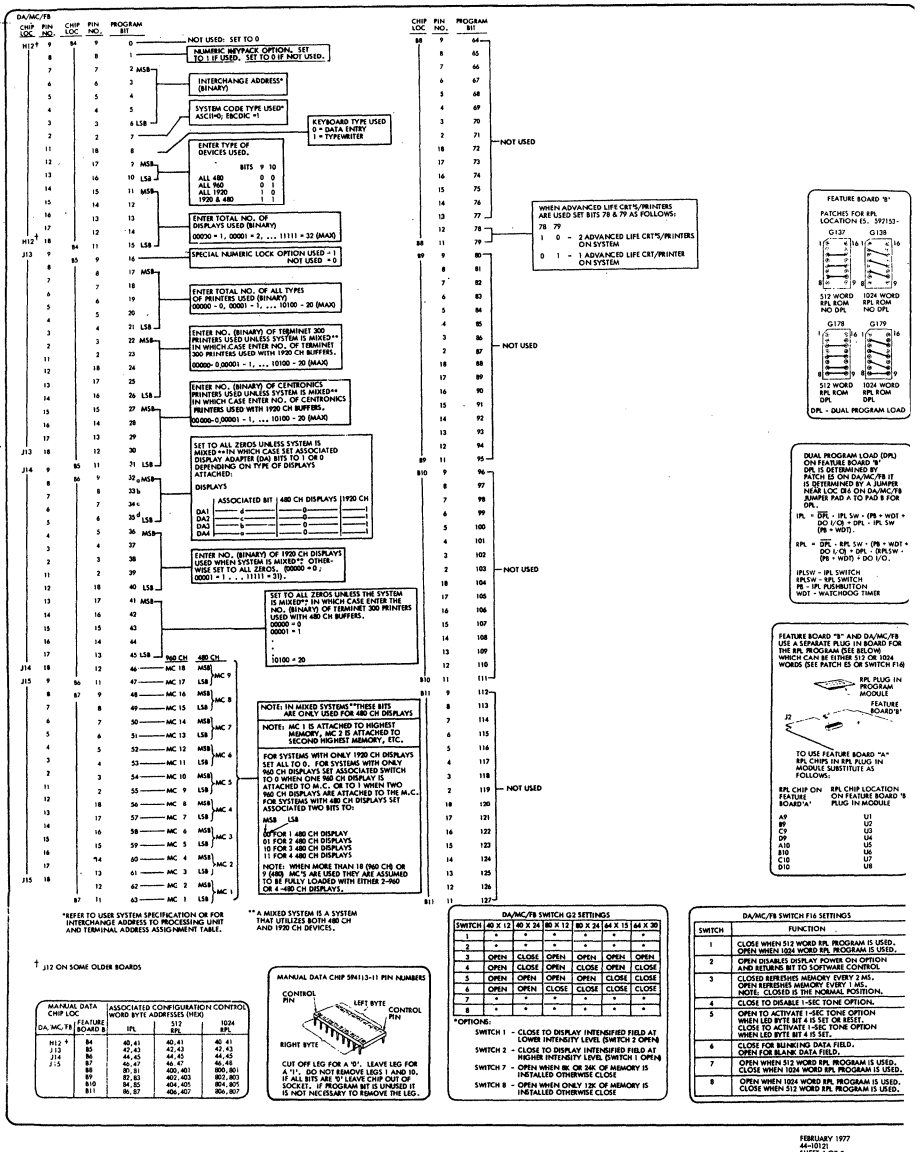
COMMUNICATIONS REGION TABLE

LOAD SIZE OF PROGRAM
KEYBOARD MODULE
SECOND HALF OF INITIALIZER
TASK SUPERVISOR
PRINTER INITIALIZER
SERIAL PRINTER ROUTINE
TICKET & BOARDING PASS PRINTERS
INITIALIZER
PRINTER STATUS TABLES
DISPLAY STATUS TABLES
NUMBER OF DISPLAYS
NUMBER OF PRINTERS
CCC COUNTER
NUMBER OF MESSAGES RECEIVED
NUMBER OF MESSAGES TRANSMITTED
EOMC'S IN TKT AND BOARDING PASS MESSAGES
DATA LOST COUNTER
CARRIER LOST COUNTER
IOCQ'S FOR DISPLAYS
IOCQ'S FOR PRINTERS
OUTPUT - TO HOST - BUFFER
VALID TERMINAL ADDRESSES
VALID PRINTER ADDRESSES
AIRLINE ID
INTERCHANGE 1
INTERCHANGE 2
LOCATION 0010 CONTAINS THE ADDRESS OF THIS TABLE

LED MEMORY BUFFER ASSIGNMENTS

Adaptor	Channel	1920 Character Display	960 Character Display		480 Character Display			
			Mon. 0	Mon. 1	Mon. 0	Mon. 1	Mon. 2	Mon. 3
1	1	07B0	03C0	07C0	01E0	03E0	05E0	07E0
	2	27B0	23C0	27C0	21E0	23E0	25E0	27E0
	3	0FB0	0BC0	0FC0	09E0	0BE0	0DE0	0FE0
	4	2FB0	28C0	2FC0	29E0	2BE0	2DE0	2FE0
	5	17B0	13C0	17C0	11E0	13E0	15E0	17E0
	6	37B0	33C0	37C0	31E0	33E0	35E0	37E0
	7	1FB0	1BC0	1FC0	19D0	1BE0	1DE0	1FE0
	8	3FB0	3BC0	3FC0	39E0	3BE0	3DE0	3FE0
2	1	47B0	43C0	47C0	41E0	43E0	45E0	47E0
	2	67B0	63C0	67C0	61E0	63E0	65E0	67E0
	3	4FB0	4BC0	4FC0	49E0	4BE0	4DE0	4FE0
	4	6FB0	68C0	6FC0	69E0	6BE0	6DE0	6FE0
	5	57B0	53C0	57C0	51E0	53E0	55E0	57E0
	6	77B0	73C0	77C0	71E0	73E0	75E0	77E0
	7	5FB0	5BC0	5FC0	59E0	5BE0	5DE0	5FE0
	8	7FB0	7BC0	7FC0	79E0	7BE0	7DE0	7FE0
3	1	87B0	83C0	87C0	81E0	83E0	85E0	87E0
	2	A7B0	A3C0	A7C0	A1E0	A3E0	A5E0	A7E0
	3	8FB0	8BC0	8FC0	89E0	8BE0	8DE0	8FE0
	4	AFB0	A8C0	AFC0	A9E0	ABE0	ADE0	AFE0
	5	97B0	93C0	97C0	91E0	93E0	95E0	97E0
	6	B7B0	B3C0	B7C0	B1E0	B3E0	B5E0	B7E0
	7	9FB0	9BC0	9FC0	99E0	9BE0	9DB0	9FE0
	8	BFB0	BBC0	BFC0	B9E0	BBE0	BDC0	BFE0
4	1	C7B0	C3C0	C7C0	C1E0	C3E0	C5E0	C7E0
	2	E7B0	E3C0	E7C0	E1E0	E3E0	E5E0	E7E0
	3	CFB0	CBC0	CFC0	C9E0	CBE0	CDE0	CFE0
	4	EFB0	EBC0	EFC0	E9E0	EBE0	EDE0	EFE0
	5	D7B0	D3C0	D7C0	D1E0	D3E0	D5E0	D7E0
	6	F7B0	F3C0	F7C0	F1E0	F3E0	F5E0	F7E0
	7	DFB0	DBC0	D7C0	D9E0	DBE0	DDE0	DFE0
	8	FFB0	FBC0	FFC0	F9E0	FBE0	FDE0	FFE0

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR 3271 REMOTE EMULATOR 933388



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44-10121
SHEET 1 OF 2

MONITOR CONTROLLER C CHARACTER, LINE FORMAT E6 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12 (24)		OPTIONS
1	——	—	—	NOTE 1
2	——	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	——
4	OPEN	CLOSED	CLOSED	——
5	CLOSED	CLOSED	CLOSED	——
6	CLOSED	OPEN	OPEN	——
7	OPEN	CLOSED	CLOSED	——
8	——	—	—	NOTE 3

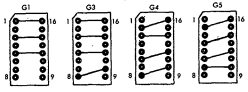
NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS

59213-



FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (59213-) INTO BOARD LOCATIONS D15 AND J16	
80 X 24	G1	G3
80 X 12	G1	G4
40 X 12	G1	G5

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (READ FROM) IS ASSIGNED TO PORT 1 OF FIRST MULTIPLEX CHANNEL CONTROLLER

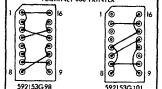
MODEM (WRITE TO) IS ASSIGNED TO PORT 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS.

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MISA PATCHES

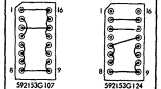
TERMINET 300 PRINTER



592153G98 592153G101

M5 - BOARD LOCATION - B2

CENTRONICS PRINTER



592153G107 592153G124

M5 - BOARD LOCATION - B2

NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

	FORMAT			
Switch	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5		See Below		
6				
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.

When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

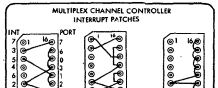
These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.

for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



592153G66 592135G185 592153G68

FOR MODEM INT LEVEL 8 — FOR MODEM INT LEVEL 8

FIRST MULTIPLEX CHANNEL CONTROLLER — 2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEMS			
SEND	0	2	5 OR 8
REC	0	1	5 OR 8
PRINTERS 1-4	0	3-6	2
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

G2 BOARD LOCATION

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

MULTIPLEX CHANNEL CONTROLLER

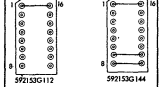
DISABLE/ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.

*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

KEYBOARD PATCHES

MAKE THE FOLLOWING PATCH CONNECTIONS ON THE PATCH PLUG LOCATED ON THE FIGHT REAR OF THE KEYBOARD.

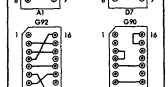


592153G112 592153G144

592153G123 592153G111

MODEM ADAPTER PATCHES

592153-

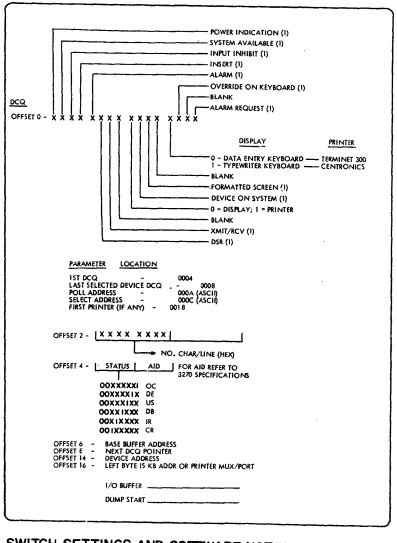


Processing Unit and Terminal Address Assignments

Encode on Feature Board — Processing Unit or Device Number	Column 1 Use this column to find: • Device Selection, • Specific Poll, • General Poll, and • Fixed Return Addresses — EBCDIC Hex	ASCII Hex	Column 2 Use this column to find: • PTS Selection Addresses — EBCDIC Hex	ASCII Hex
0	40	20	60	20
1	C1	41	61	2F
2	C2	42	E2	53
3	C3	43	E3	54
4	C4	44	E4	55
5	C5	45	E5	56
6	C6	46	E6	57
7	C7	47	E7	58
8	C8	48	E8	59
9	C9	49	E9	5A
10	4A	58	6A	5C
11	4B	2E	6B	2C
12	4C	3C	6C	25
13	4D	28	6D	5F
14	4E	2B	6E	3E
15	4F	21	6F	3F
16	50	26	F0	30
17	D1	4A	F1	31
18	D2	4B	F2	32
19	D3	4C	F3	33
20	D4	4D	F4	34
21	D5	4E	F5	35
22	D6	4F	F6	36
23	D7	50	F7	37
24	D8	51	F8	38
25	D9	52	F9	39
26	5A	5D	7A	3A
27	5B	24	7B	23
28	5C	2A	7C	40
29	5D	29	7D	27
30	5E	3B	7E	3D
31	5F	5E	7F	22

NOTE

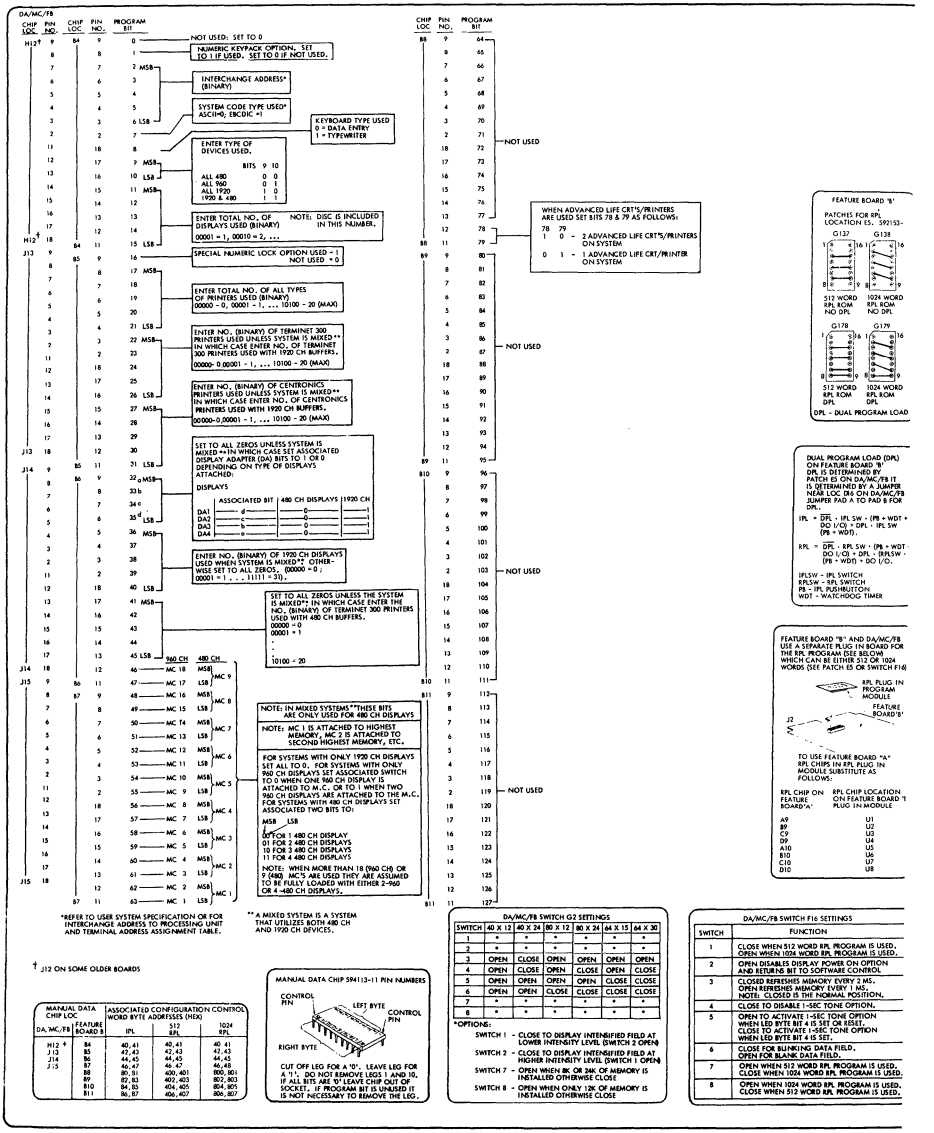
I/O character address 7F is used as the device address to specify a General Poll operation.



PATCH AND SWITCH SETTINGS AND SOFTWARE NOTES FOR 3271 REMOTE EMULATOR 933388

FEBRUARY 1977
44-10121
SHEET 2 OF 2

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR 3271 REMOTE EMULATOR 933306



MONITOR CONTROLLER C CHARACTER/LINE FORMAT E6 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12	24	OPTIONS
1	——	—	—	NOTE 1
2	——	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	——
4	OPEN	CLOSED	CLOSED	——
5	CLOSED	CLOSED	CLOSED	——
6	CLOSED	OPEN	OPEN	——
7	OPEN	CLOSED	CLOSED	——
8	—	—	—	NOTE 3

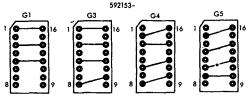
NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS

592153-



FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-)	INTO BOARD LOCATIONS D15 AND J16	
80 X 24	G1	G3	
80 X 12	G1	G4	
40 X 12	G1	G5	

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (READ FROM) IS ASSIGNED TO PORT 1 OF FIRST MULTIPLEX CHANNEL CONTROLLER

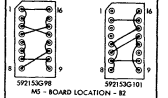
MODEM (WRITE TO) IS ASSIGNED TO PORT 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS.

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MISA PATCHES

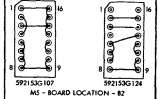
TERMINET 300 PRINTER



592153G98 592153G101

M5 - BOARD LOCATION - B2

CENTRONICS PRINTER



592153G107 592153G124

M5 - BOARD LOCATION - B2

NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT			
	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5	——			——
6	——	See Below		——
7	——			——
8	——			——

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.

When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

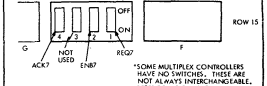
for HI Intensity - close ODD numbered switches and open others.
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1; Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MULTIPLEX CHANNEL CONTROLLER

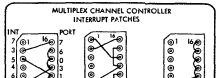
DISABLE ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

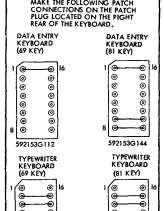
DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEMS			
SEND	0	2	5 OR 8
REC	0	1	5 OR 8
PRINTERS 1-4	0	3-6	2
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

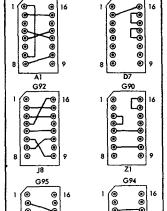
KEYBOARD PATCHES

MAKE THE FOLLOWING PATCH CONNECTIONS ON THE PATCH PLUG LOCATED ON THE RIGHT REAR OF THE KEYBOARD.



MODEM ADAPTER PATCHES

592153-

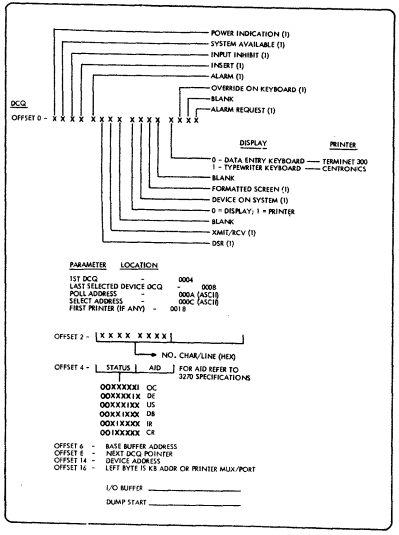


Processing Unit and Terminal Address Assignments

Encode on Feature Board	Column 1 Use this column to find: • Device Selection, • Specific Poll, • General Poll, and • Fixed Return Addresses		Column 2 Use this column to find: • PTS Selection Addresses	
Processing Unit or Device Number	EBCDIC Hex	ASCII Hex	EBCDIC Hex	ASCII Hex
0	40	20	60	2D
1	C1	41	61	2F
2	C2	42	E2	53
3	C3	43	E3	54
4	C4	44	E4	55
5	C5	45	E5	56
6	C6	46	E6	57
7	C7	47	E7	58
8	C8	48	E8	59
9	C9	49	E9	5A
10	4A	5B	6A	5C
11	4B	2E	6B	2C
12	4C	3C	6C	25
13	4D	28	6D	5F
14	4E	2B	6E	3E
15	4F	21	6F	3F
16	50	26	F0	30
17	D1	4A	F1	31
18	D2	4B	F2	32
19	D3	4C	F3	33
20	D4	4D	F4	34
21	D5	4E	F5	35
22	D6	4F	F6	36
23	D7	50	F7	37
24	D8	51	F8	38
25	D9	52	F9	39
26	5A	5D	7A	3A
27	5B	24	7B	23
28	5C	2A	7C	40
29	5D	29	7D	27
30	5E	3B	7E	3D
31	5F	5E	7F	22

NOTE

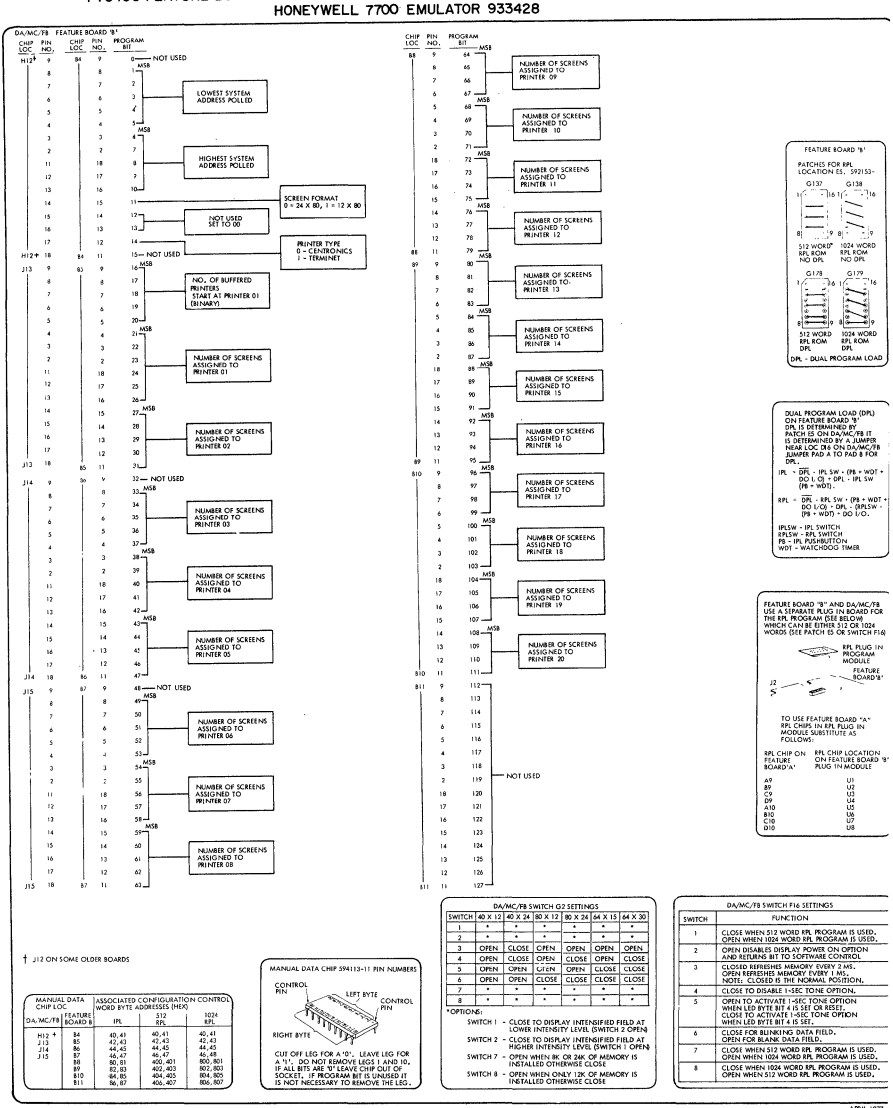
I/O character address 7F is used as the device address to specify a General Poll operation.



PATCH AND SWITCH SETTINGS AND SOFTWARE NOTES FOR 3271 REMOTE EMULATOR 933306

FEBRUARY 1977
44-10122

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR HONEYWELL 7700 EMULATOR 933428



† J12 ON SOME OLDER BOARDS

MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA/MC/FB	FEATURE BOARD B	IPL	512 RPL	1024 RPL
H12 †	B4	40, 41	40, 41	40, 41
J13	B5	42, 43	42, 43	42, 43
J14	B6	44, 45	44, 45	44, 45
J15	B7	46, 47	46, 47	46, 48
	B8	80, 81	400, 401	800, 801
	B9	82, 83	402, 403	802, 803
	B10	84, 85	404, 405	804, 805
	B11	86, 87	406, 407	806, 807

MANUAL DATA CHIP 594113-11 PIN NUMBERS

CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
8	CLOSE WHEN 1024 WORD RPL PROGRAM IS USED. OPEN WHEN 512 WORD RPL PROGRAM IS USED.

FEATURE BOARD 'B'

PATCHES FOR RPL LOCATION ES. 592153-

DPL - DUAL PROGRAM LOAD

DUAL PROGRAM LOAD (DPL) ON FEATURE BOARD 'B' DPL IS DETERMINED BY PATCH IS ON DA/MC/FB IT IS DETERMINED BY A JUMPER NEAR LOC P4 ON DA/MC/FB JUMPER PAD A TO PAD B FOR DPL.

IPL = $\overline{DPL}$ · IPL SW · (PB + WDT + DO I/O + DPL · IPL SW (PB + WDT).

RPL = DPL · RPL SW · (PB + WDT + DO I/O) + DPL · (IPLSW · (PB + WDT) + DO I/O.

IPLSW - IPL SWITCH
RPLSW - RPL SWITCH
PB - IPL PUSHBUTTON
WDT - WATCHDOG TIMER

FEATURE BOARD 'B' AND DA/MC/FB USE A SEPARATE PLUG IN BOARD FOR THE RPL PROGRAM (SEE BELOW) WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5 OR SWITCH F16)

TO USE FEATURE BOARD "A" RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATION ON FEATURE BOARD 'B' PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8

MONITOR CONTROLLER B AND C

CHARACTER/ LINE FORMAT E6 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12	D26	64 X 15	D28	OPTIONS
1	—	—	—	—	—	NOTE 1
2						NOTE 2
3	OPEN	OPEN	CLOSED	OPEN	CLOSED	—
4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
5	CLOSED	CLOSED	CLOSED	OPEN	OPEN	—
6	CLOSED	OPEN	OPEN	OPEN	OPEN	—
7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
8	—	—	—	—	—	NOTE 3

NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT			
	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5	See Below			
6				
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.

When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level then normal:

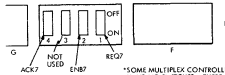
for HI Intensity - close ODD numbered switches and open others.
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MULTIPLEX CHANNEL CONTROLLER

DISABLE/ENABLE PORT 7 SWITCH*

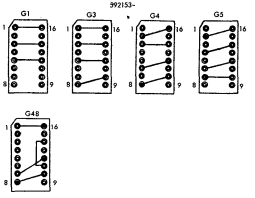
S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS



FOR THESE CHAR./LINE/LINES OF LINES FORMATS	INSERT THESE PATCHES* (592153-)	INFO BOARD LOCATIONS D15 AND J16	
80 X 24		G1	G3
64 X 30 & SPLIT SCREEN		G2	G3
80 X 12		G1	G4
64 X 15 OR 16		G2	G4
40 X 12		G1	G5
40 X 24		G1	G48

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE THE MOTHERBOARD UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY SHIFTED TO CASSETTE INDOSM, ALL MODELS (WRITE TO PRINTER)	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY READ FROM MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:
CASSETTE IS ASSIGNED TO PORTS 0 & 3 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PORT 1 AND 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER ARE ASSIGNED TO MODEM RECEIVE & TRANSMIT

FIRST PRINTER IS ASSIGNED TO PORT 3 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS

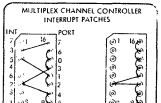
*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

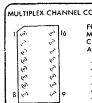
DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0,3	2
KEYBOARDS	0	7	3
MODEM:			
SEND	0	2	5
REC	0	1	5
PRINTERS:			
1-4	0	4-6	2
5-12	1	0-7	2
13-15	2	0-7	2

NOTE: TERMINET AND EXTEL PRINTERS MUST BE ASSIGNED FIRST

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH



FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 13 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

MONITOR CONTROLLER B-16

56 CHR SWITCH SETTING	40 CHAR. 12 LINES	80 CHAR. 12 LINES	64 CHAR. 15/16 LINES	80 CHAR. 24 LINES	64 CHAR. 30 LINES	40 CHAR. 24 LINES	STEP SCAN#
E6-1	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	CLOSED
E6-2	OPEN	OPEN	OPEN*	OPEN	OPEN	OPEN	OPEN
E6-3	OPEN	OPEN	OPEN	CLOSED	CLOSED	CLOSED	CLOSED
E6-4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
E6-5	CLOSED	OPEN	OPEN	CLOSED	OPEN	CLOSED	**
E6-6	CLOSED	OPEN	OPEN	OPEN	OPEN	CLOSED	OPEN
E6-7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
E6-8***	OPEN	OPEN	OPEN*	OPEN	OPEN	OPEN	OPEN

*USABLE ONLY ON 24 OR 30 LINE FORMAT. SPACING BETWEEN LINES IS ADJUSTABLE BY SETTING R35.

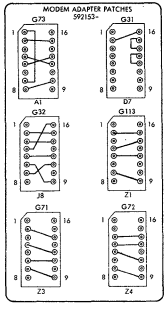
**SET AS INDICATED FOR 24 OR 30 LINE FORMAT.

+ CLOSED FOR 16 LINE FORMAT

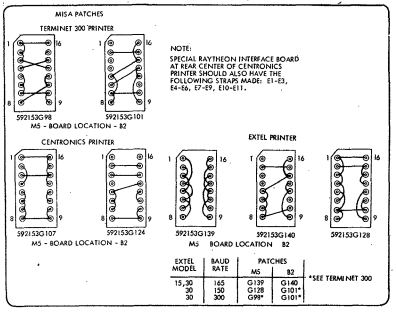
***E6-8 IS USED ON SOME MC'S (IT IS USED ON ALL 16 LINE MC'S).

NOTE: WHEN MC IS USED WITH SPLIT SCREEN DISPLAYS A JUMPER IS CONNECTED BETWEEN XT2 PIN 15 AND XT PIN 14.

MODEM ADAPTER PATCHES



MISA PATCHES



NOTE:
SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

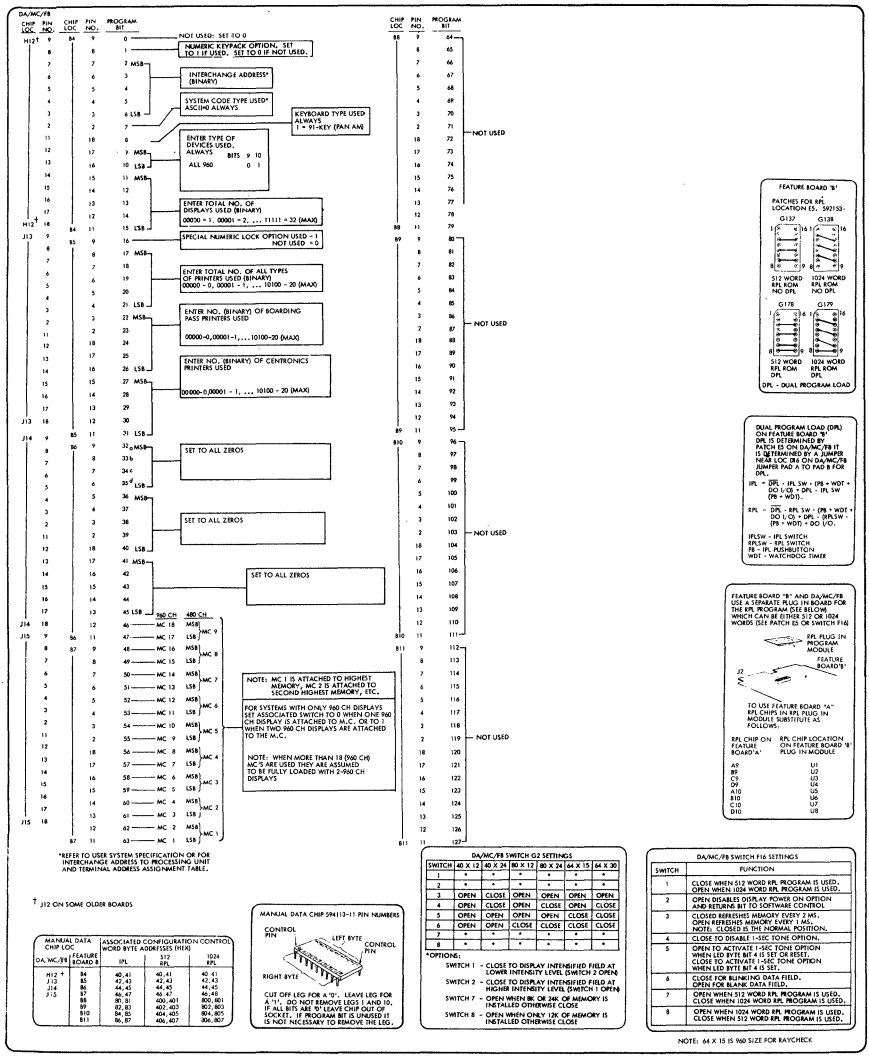
EXTEL MODEL	BAUD RATE	PATCHES M5	PATCHES B2	
15,30	165	G139	G140	*SEE TERMINET 300
30	150	G128	G101*	
30	300	G98*	G101*	

NOTE: UNDERLINES DENOTE REQUIREMENTS FOR THIS EMULATOR

PATCH AND SWITCH SETTING FOR HONEYWELL 7700 EMULATOR 933428

APRIL 1977
44-10143
SHEET 2 OF 2

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR DOWNLINE 3271 REMOTE EMULATOR FOR RAYCHECK 933494



MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA, MC/FB	FEATURE BOARD B	IPL	512 RPL	1024 RPL
H12 †	84	40, 41	40, 41	40 41
J12	85	42, 43	42, 43	42, 43
J14	86	44, 45	44, 45	44, 45
J15	87	46, 47	46, 47	46, 47
	88	00, 01	400, 401	800, 801
	89	02, 03	402, 403	802, 803
	B10	04, 05	404, 405	804, 805
	B11	06, 07	406, 407	806, 807

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT # 15 SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT # 15 SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

NOTE: 64 X 15 IS 960 SIZE FOR RAYCHECK

MONITOR CONTROLLER F – (P/N 860548 – EXCEPT FIRST 250 BOARDS P/N 860864, PAM ONLY)

CONFIGURATION PLUG (D8)

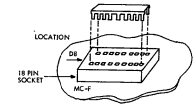
THE MC-F HAS ONE SOCKET WHICH REQUIRES A CONFIGURATION PLUG TO SELECT MOST OF THE AVAILABLE OPTIONS. ANY POSSIBLE COMBINATION OF OPTIONS CAN BE SELECTED BY CUTTING OFF APPROPRIATE LEGS OF THE PLUG.

NOTE: 1. WITHOUT TRANSMITTER MODULE, THE MC-F IS COMPLETELY BACKWARDS COMPATIBLE WITH THE PRESENT D.A.

2. WITH TRANSMITTER MODULE, M-FC HAS THE ADDED COAX CABLE OPTION USED WITH D.A. "C".

CONFIGURATION SOCKET LOCATION

CONFIGURATION PLUG (RAYTHEON P/N 594113-11)



OPTION PIN ASSIGNMENTS

FORMAT SELECTION

Config. Plug Pin No.	DISPLAY FORMATS						
	40X12	40X24	64X15	64X16	64X30	80X12	80X24
4	Cut	Cut	Cut	In	Cut	Cut	Cut
11	Cut	In	Cut	Cut	In	Cut	In
12	Cut	Cut	In	In	In	In	In
17	In	In	Cut	Cut	Cut	In	In

DISPLAY ADAPTER "C"

P/N 860629

8K AND 16K MEMORIES

DISPLAY ADAPTER "C" HAS A PROVISION FOR THREE AUXILIARY MODULES TO USE IBM COAX CABLE. TWO RECEIVER BOARDS AND ONE COAX CONTROL LOGIC BOARD.

CHARACTER/LINE FORMAT AND MEMORY REFRESH TIMING PATCH PLUGS

For These Displays Char/Lines No. of Lines Formats (592153-)	Insert These Patches (592153-)	INTO BOARD LOCATIONS				
		E10	J16	C2 (Norm)	C2 (Opt)	C3 16K	C3 8K
80 X 24		G1	G3	G134 OR G136		G133 OR G135
64 X 30		G2	G3	G134 OR G136		G133 OR G135
80 X 12		G1	G4	G134 OR G136		G133 OR G135
64 X 15 OR 16		G2	G4	G134 OR G136		G133 OR G135
40 X 12		G1	G5	G134 OR G136		G133 OR G135
40 X 24		G1	G48	G134 OR G136		G133 OR G135

E10 – NUMBER OF CHARACTERS PER LINE

J16 – NUMBER OF LINES PER FORMAT

C2 – MEMORY REFRESH
G134 – 2 MS (NORMAL TIMING)
G136 – 1 MS (OPTION TIMING)

C3 – TYPE OF MEMORY MODULE
G135 – 8K MEMORY MODULE
G133 – 16K MEMORY MODULE

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (READ FROM) IS ASSIGNED TO PORT 1 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (WRITE TO) IS ASSIGNED TO PORT 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS.

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MI5A PATCHES

BOARD PASS PRINTER

G107 G108

MS-BOARD LOCATION – B2
CENTRONICS PRINTER

592153G107 592153G124

MS – BOARD LOCATION – B2

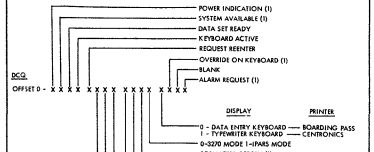
NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

G2 BOARD LOCATION

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9



PARAMETER	LOCATION	
1ST DCQ	-	0004
LAST SELECTED DEVICE DCQ	-	0008
POLL ADDRESS	-	000A (ASCII)
SELECT ADDRESS	-	000C (ASCII)
FIRST PRINTER (IF ANY)	-	0018

OFFSET 2 - X X X X X X X X

NO. CHAR/LINE (HEX)

OFFSET 4 - STATUS | AID — FOR AID REFER TO 3270 SPECIFICATIONS

00XXXXXI OC
00XXXIXX DE
00XXIXXX US
00XXIXXX D8
00XIXXXX IR
00IXXXXX CR

OFFSET 6 - BASE BUFFER ADDRESS
OFFSET E - NEXT DCQ POINTER
OFFSET 14 - DEVICE ADDRESS
OFFSET 16 - LEFT BYTE IS KB ADDR OR PRINTER MUX/PORT

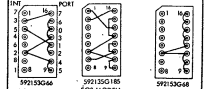
I/O BUFFER _____

DUMP START _____

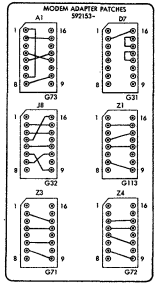
DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	2	3
KEYBOARDS	0	7	3
MODEMS			
SEND	0	2	5 OR 8
REC	0	1	5 OR 8
PRINTERS 1-4	0	3-6	2
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



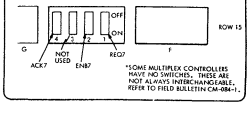
MODEM ADAPTER PATCHES 592153-



MULTIPLEX CHANNEL CONTROLLER

DISABLE, ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

Processing Unit and Terminal Address Assignments

Encode on Feature Board	Column 1 Use this column to find: • Device Selection, • Specific Poll, • General Poll, and • Fixed Return Addresses	Column 2 Use this column to find: • PIS Selection Addresses
Control Unit or Device Number	ASCII HEX	ASCII Hex
0	24	54
1	25	55
2	26	56
3	27	57
4	28	58
5	29	59
6	2A	5A
7	2B	5B
8	2C	5C
9	2D	5D
10	2E	5E
11	2F	5F
12	30	60
13	31	61
14	32	62
15	33	63
16	34	64
17	35	65
18	36	66
19	37	67
20	38	68
21	39	69
22	3A	6A
23	3B	6B
24	3C	6C
25	3D	6D
26	3E	6E
27	3F	6F
28	40	70
29	41	71
30	42	72
31	43	73
32	44	74
33	45	75
34	46	76
35	47	77
36	48	78
37	49	79
38	4A	7A
39	4B	7B

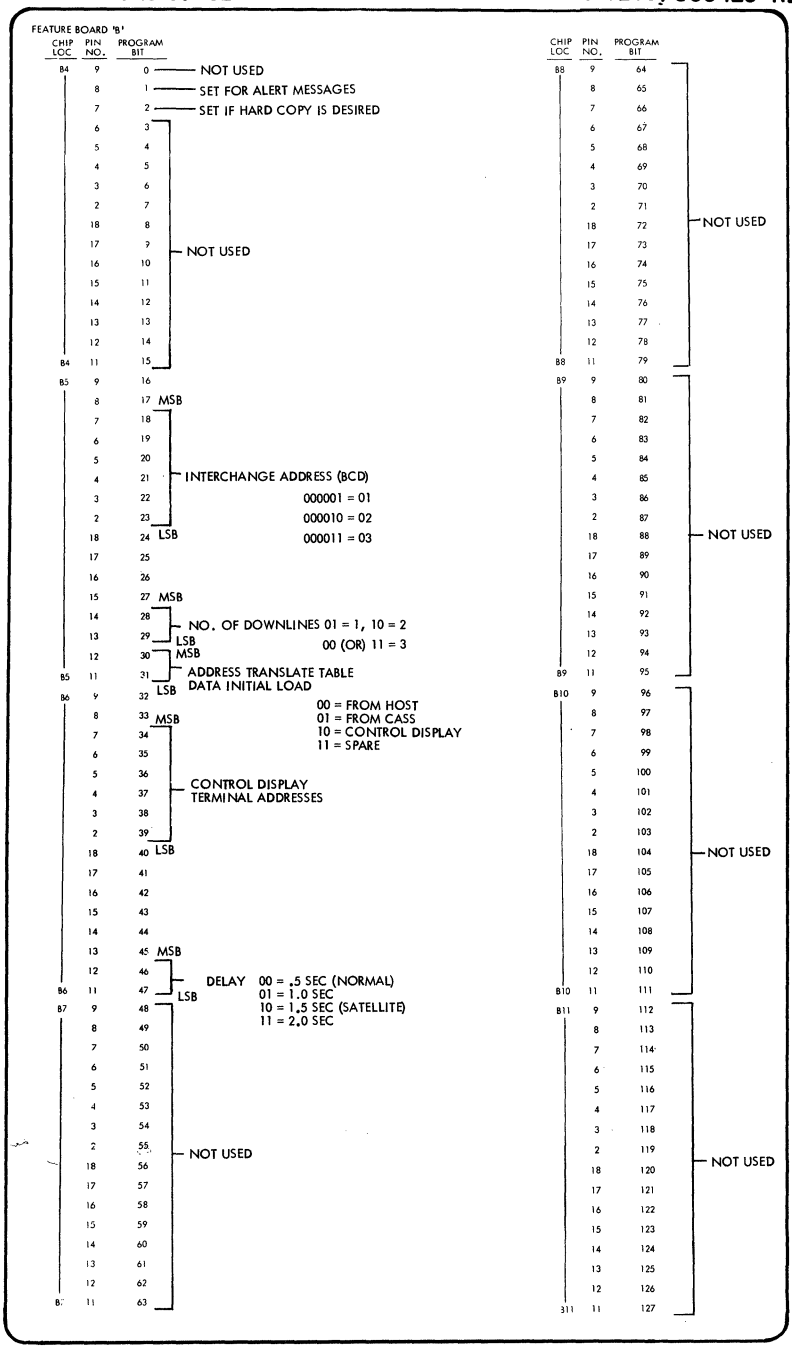
NOTE

I/O character address 7F is used as the device address to specify a General Poll operation.

44-10152
Sheet 2 of 2

PATCH AND SWITCH SETTINGS AND SOFTWARE NOTES FOR DOWNLINE 3271 REMOTE EMULATOR FOR RAYCHECK

PTS-100 FEATURE BOARD
'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR COMMUNICATIONS CONCENTRATOR AND LINE CONTROL UNIT (CCLCU) 863426-REV. C



SET ALL UNUSED BITS = 0

MUX PORT AND INTERRUPT ASSIGNMENT

MUX 0

DEVICE	MUX PORT ASSIGNMENT	INTERRUPT LEVEL
CASSETTE	0	2
PRINTER	1	2
UPLINE RECEIVE	3	7
UPLINE TRANSMIT	4	5
DOWNLINE RECEIVE 1	5	6
DOWNLINE TRANSMIT 1	6	4
KEYBOARD	7	3

MUX 1

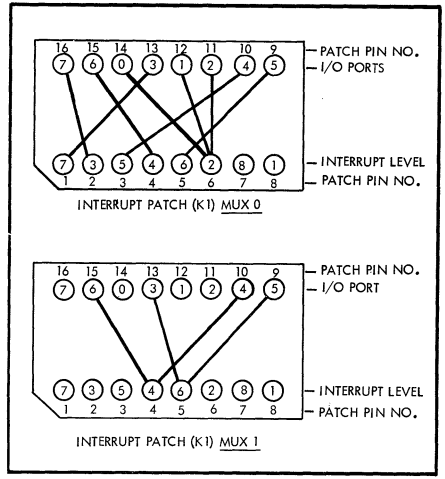
DOWNLINE RECEIVE 2	3	6
DOWNLINE TRANSMIT 2	4	4
DOWNLINE RECEIVE 3	5	6
DOWNLINE TRANSMIT 3	6	4

GPCA CONFIGURATION

PATCHES	LOCATION	PATCH NO.	CCLCU ROMS	LOCATION	PART NO.
	A6	592153G160		K1	860832-1
	A13	592153G160		G1	860832-2
	A14	592153G159		B2	860832-3
	B5	592153G159		K3	860832-4
	B12	592153G161		H1	860832-5
	C7	592153G161		C4	860832-6
	E5	592153G158		H2	860832-7
	M11	592153G146		K2	860832-8
	N9	592153G146		F2	860832-9
	N13	592153G145		C2	860832-10
				B4	860832-11
				D1	860832-12

CABLES

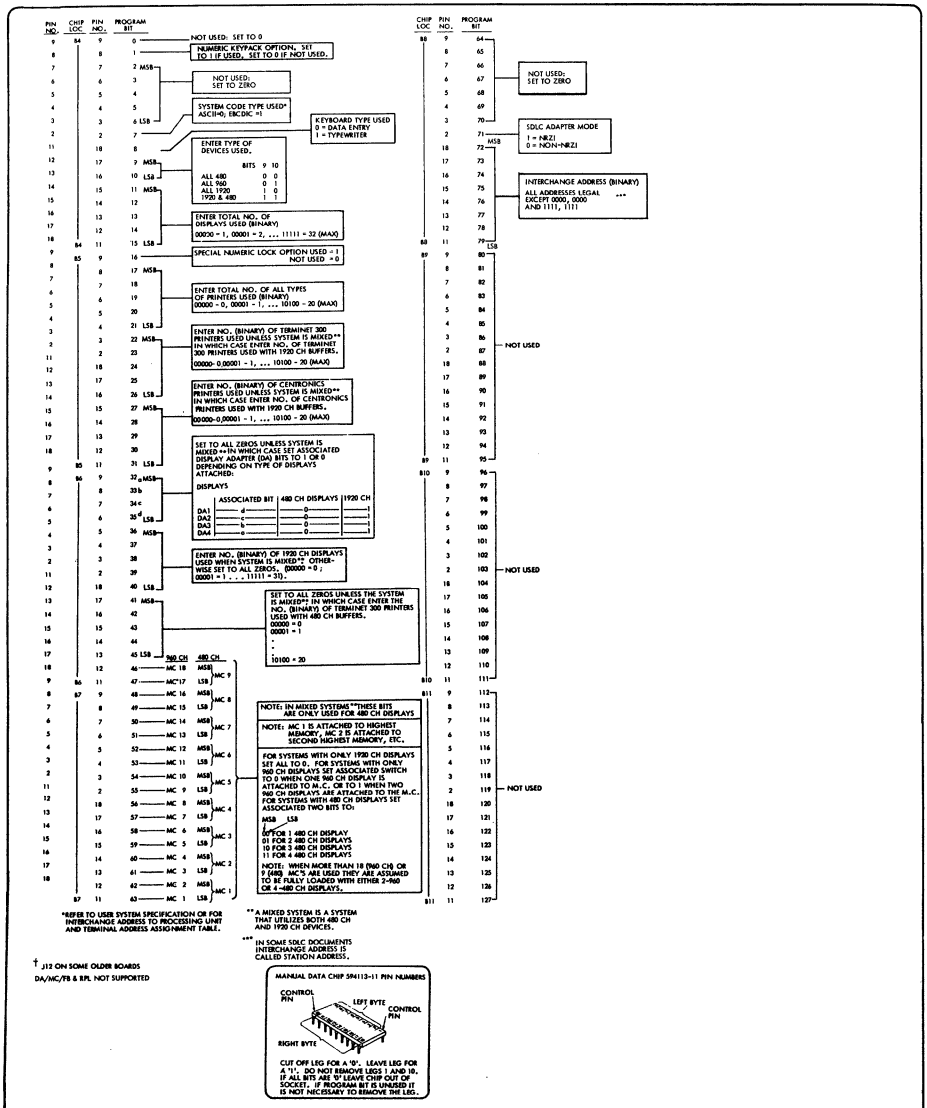
GPCA TO MODEM CABLE PART NUMBER 860538.



INTERRUPT PATCH (K1) MUX 0

INTERRUPT PATCH (K1) MUX 1

PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR SDLC 3271 REMOTE EMULATOR 933457



*REFER TO USER SYSTEM SPECIFICATION OR FOR INTERCHANGE ADDRESS TO PROCESSING UNIT AND TERMINAL ADDRESS ASSIGNMENT TABLE.

**A MIXED SYSTEM IS A SYSTEM THAT UTILIZES BOTH 480 CH AND 1920 CH DEVICES.

*** IN SOME SDLC DOCUMENTS INTERCHANGE ADDRESS IS CALLED STATION ADDRESS.

† J12 ON SOME OLDER BOARDS
DA/MC/FB & RPL NOT SUPPORTED

MONITOR CONTROLLER C CHARACTER/LINE FORMAT E6 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12 (24)		OPTIONS
1	——	—	—	NOTE 1
2	——	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	——
4	OPEN	CLOSED	CLOSED	——
5	CLOSED	CLOSED	CLOSED	——
6	CLOSED	OPEN	OPEN	——
7	OPEN	CLOSED	CLOSED	——
8	——	—	—	NOTE 3

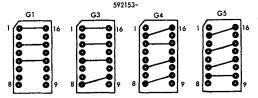
NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER. EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS

592153-



FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-) INTO BOARD LOCATIONS D15 AND J16	
80 X 24	G1	G3
80 X 12	G1	G4
40 X 12	G1	G5

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (READ FROM) IS ASSIGNED TO PORT 1 OF FIRST MULTIPLEX CHANNEL CONTROLLER

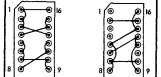
MODEM (WRITE TO) IS ASSIGNED TO PORT 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS.

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MISA PATCHES

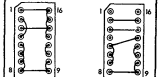
TERMINET 300 PRINTER



592153G98 — MS - BOARD LOCATION - B2

592153G101

CENTRONICS PRINTER



592153G107 — MS - BOARD LOCATION - B2

592153G124

NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT			
	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Close	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5	See Below			
6				
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.
When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level then normal:

for HI Intensity - close ODD numbered switches and open others.

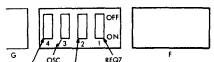
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MULTIPLEX CHANNEL CONTROLLER

DISABLE/ENABLE PORT 7 SWITCH

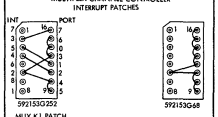
S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



FIRST MUX "OFF"
2ND AND 3RD MUX "ON"

*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-004-1.

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



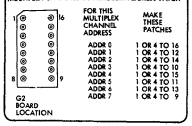
592153G252 — MUX K1 PATCH — FIRST MULTIPLEX CHANNEL CONTROLLER

592153G68 — 2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEMS SEND REC	0 0	2 1	5 OR 8 5 OR 8
PRINTERS 1-4	0	3-6	2
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2

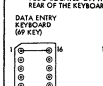
MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH



KEYBOARD PATCHES

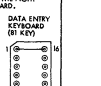
MAKE THE FOLLOWING PATCH CONNECTIONS ON THE PATCH PLUG LOCATED ON THE FIGHT REAR OF THE KEYBOARD.

DATA ENTRY KEYBOARD (69 KEY)



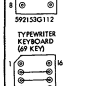
592153G112

DATA ENTRY KEYBOARD (81 KEY)



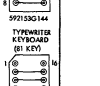
592153G144

TYPEWRITER KEYBOARD (69 KEY)



592153G123

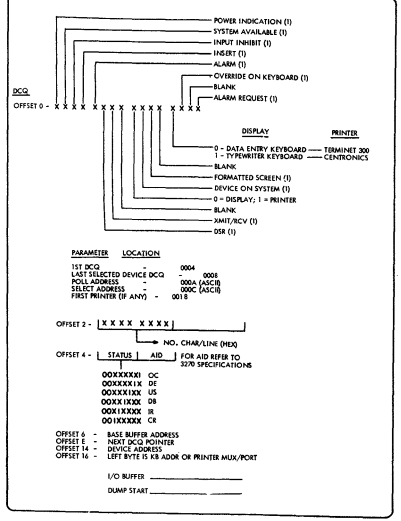
TYPEWRITER KEYBOARD (81 KEY)



592153G111

DEVICE ADDRESSING FOR 3271 CONTROL UNIT

DEVICE NUMBER	TH ADDRESS FIELD BITS: 1 2 3 4 5 6 7
0	1 0 0 0 0 0 0
1	1 0 0 0 0 0 1
2	1 0 0 0 0 1 0
3	1 0 0 0 0 1 1
4	1 0 0 0 1 0 0
5	1 0 0 0 1 0 1
6	1 0 0 0 1 1 0
7	1 0 0 0 1 1 1
8	1 0 0 1 0 0 0
9	1 0 0 1 0 0 1
10	1 0 0 1 0 1 0
11	1 0 0 1 0 1 1
12	1 0 0 1 1 0 0
13	1 0 0 1 1 0 1
14	1 0 0 1 1 1 0
15	1 0 0 1 1 1 1
16	1 0 1 0 0 0 0
17	1 0 1 0 0 0 1
18	1 0 1 0 0 1 0
19	1 0 1 0 0 1 1
20	1 0 1 0 1 0 0
21	1 0 1 0 1 0 1
22	1 0 1 0 1 1 0
23	1 0 1 0 1 1 1
24	1 0 1 1 0 0 0
25	1 0 1 1 0 0 1
26	1 0 1 1 0 1 0
27	1 0 1 1 0 1 1
28	1 0 1 1 1 0 0
29	1 0 1 1 1 0 1
30	1 0 1 1 1 1 0
31	1 0 1 1 1 1 1

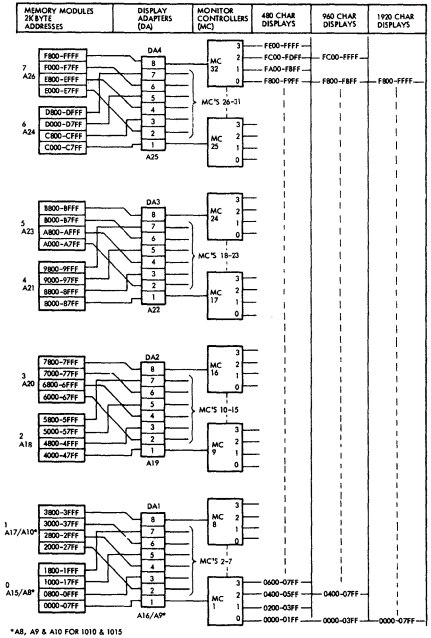


PATCH AND SWITCH SETTINGS AND SOFTWARE NOTES FOR SDLC 3271 REMOTE EMULATOR

OCTOBER 1977
44-10162
SHEET 2 OF 3

A-92

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, A9 & A10 FOR 1010 & 1015

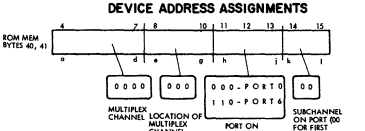
NOTES

ALL DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. IN A MIXED SYSTEM 1920 CH DISPLAYS ARE ASSIGNED BEFORE 480 CH DISPLAYS. ALSO THE STARTING MEMORY ADDRESSES ARE DETERMINED BY WHICH DISPLAY ADAPTERS ARE ASSIGNED TO 1920 CH AND 480 CH DISPLAYS (SEE C4 ON F.B.'A3). IF A SYSTEM IS MIXED OR DOES NOT FULLY LOAD ALL M.C.'s, PRINTER BUFFERS WILL BE ASSIGNED TO THE UNUSED AREAS. IN A MIXED SYSTEM PRINTERS ARE ASSIGNED AS FOLLOWS:

1 CENTRONICS - 1920 CH BUFFER
2 TERMINET - 1920 CH BUFFER
3 CENTRONICS - 480 CH BUFFER
4 TERMINET - 480 CH BUFFER

THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULES A17/A10* AND A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

MONITOR CONTROLLER F - (P/N 860548 - EXCEPT FIRST 250 BOARDS P/N 860864, PAM ONLY)

CONFIGURATION PLUG (D8)

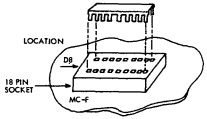
THE MC-F HAS ONE SOCKET WHICH REQUIRES A CONFIGURATION PLUG TO SELECT MOST OF THE AVAILABLE OPTIONS. ANY POSSIBLE COMBINATION OF OPTIONS CAN BE SELECTED BY CUTTING OFF APPROPRIATE LEGS OF THE PLUG.

NOTE: 1. WITHOUT TRANSMITTER MODULE, THE MC-F IS COMPLETELY BACKWARDS COMPATIBLE WITH THE PRESENT D.A.

2. WITH TRANSMITTER MODULE, M-FC HAS THE ADDED COAX CABLE OPTION USED WITH D.A. "C".

CONFIGURATION SOCKET LOCATION

CONFIGURATION PLUG (RAYTHEON P/N 594113-11)



OPTION PIN ASSIGNMENTS — FORMAT SELECTION

Config. Plug Pin No.	DISPLAY FORMATS 40X12	40X24	64X15	64X16	64X30	80X12	80X24
4	Cut	Cut	Cut	In	Cut	Cut	Cut
11	Cut	In	Cut	Cut	In	Cut	In
12	Cut	Cut	In	In	In	In	In
17	In	In	Cut	Cut	Cut	In	In

DISPLAY ADAPTER "C"

P/N 860629

8K AND 16K MEMORIES

DISPLAY ADAPTER "C" HAS A PROVISION FOR THREE AUXILIARY MODULES TO USE IBM COAX CABLE: TWO RECEIVER BOARDS AND ONE COAX CONTROL LOGIC BOARD.

CHARACTER/LINE FORMAT AND MEMORY REFRESH TIMING PATCH PLUGS

For These Displays Char/Linen No.: of Lines Formats	Insert These Patches (5951253-1)	INTO BOARD LOCATIONS E10	J16	C2 (Norm)	C2 (Opt)	C3 16K	C3 8K
80 X 24		G1	G3	G134 OR G136		G133 OR G135	
64 X 30		G2	G3	G134 OR G136		G133 OR G135	
80 X 12		G1	G4	G134 OR G136		G133 OR G135	
64 X 16 OR 16		G2	G4	G134 OR G136		G133 OR G135	
40 X 12		G1	G5	G134 OR G136		G133 OR G135	
40 X 24		G1	G48	G134 OR G136		G133 OR G135	

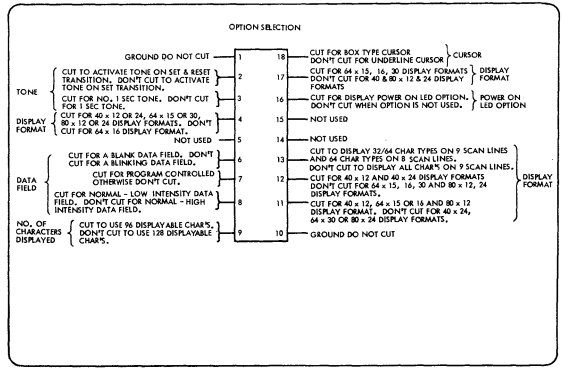
E10 — NUMBER OF CHARACTERS PER LINE

J16 — NUMBER OF LINES PER FORMAT

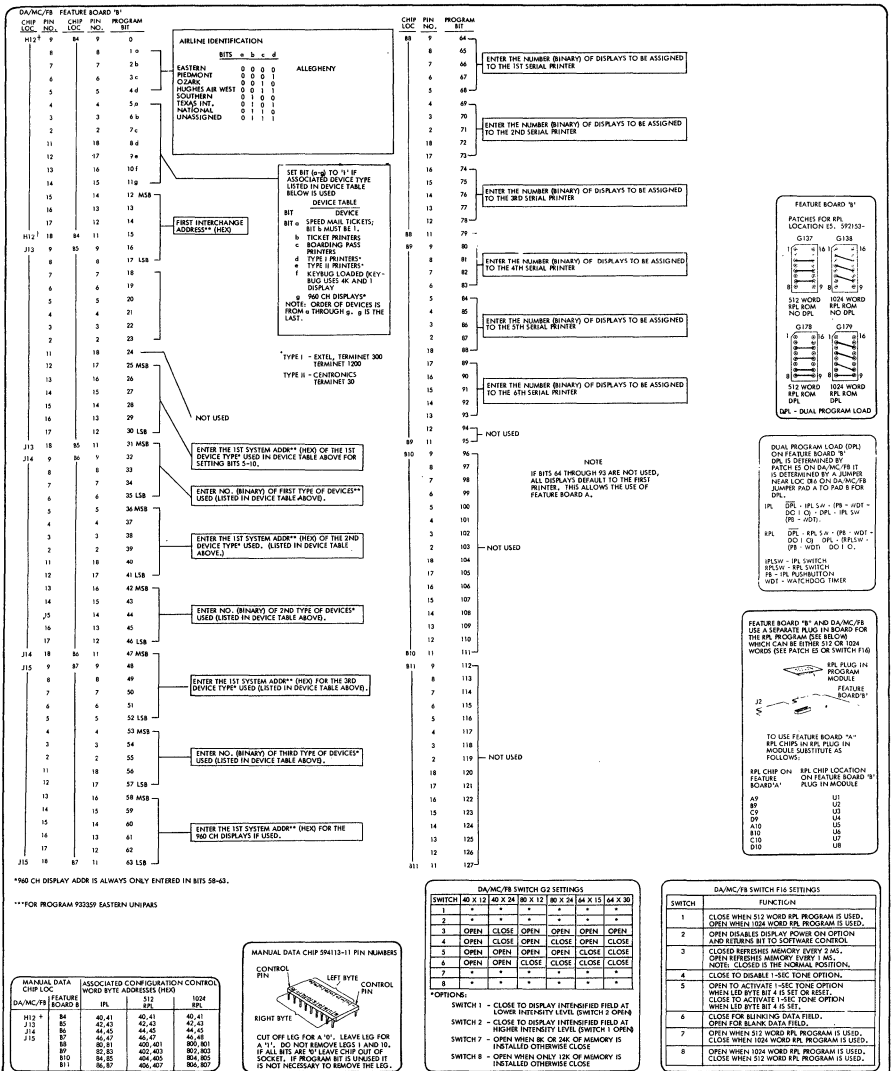
C2 — MEMORY REFRESH
G134 - 2 MS (NORMAL TIMING)
G136 - 1 MS (OPTION TIMING)

C3 — TYPE OF MEMORY MODULE
G135 - 8K MEMORY MODULE
G133 - 16K MEMORY MODULE

OPTION SELECTION



PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR EASTERN UNIPARS (933359) EMULATOR USING THE INITIALIZATION PROGRAM ***



*960 CH DISPLAY ADDR IS ALWAYS ONLY ENTERED IN BITS 58-63.

***FOR PROGRAM 933359 EASTERN UNIPARS

MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA/MC/FB	FEATURE BOARD B	IPL	512 RPL	1024 RPL
H12 †	84	40,41	40,41	40,41
J13	85	42,43	42,43	42,43
J14	86	44,45	44,45	44,45
J15	87	46,47	46,47	46,48
	88	80,81	400,401	800,801
	89	82,83	402,403	802,803
	B10	84,85	404,405	804,805
	B11	86,87	406,407	806,807

MANUAL DATA CHIP 594113-11 PIN NUMBERS

CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

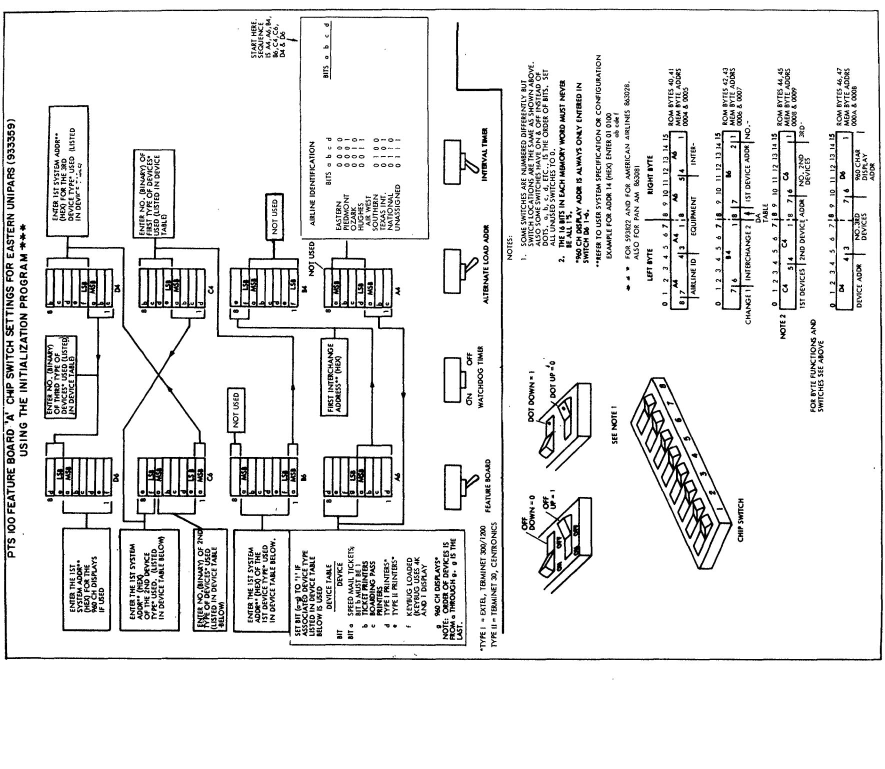
*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

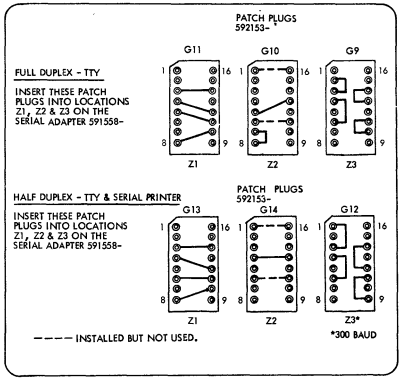
SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

Display Adaptor	Channel	Monitor	1920 Char/Display 80 Ch X 24 Lines 64 Ch X 30 Lines: Memory Buffer Area	Keyboard Address	960 Char/Display 80 Ch X 12 Lines 64 Ch X 15 or 16 Lines: Memory Buffer Area	Keyboard Address	960 Char/Display 40 Ch X 24 Lines: Memory Buffer Area	Keyboard Address	480 Char/Display 40 Ch X 12 Lines: Memory Buffer Area	Keyboard Address
1	1	0	0000-07FF	81	0000-03FF	81	0000-03FF	81	0000-01FF	81
		1					0400-07FF	A1	0200-03FF	A1
		2			0400-07FF	C1			0400-05FF	C1
		3							0600-07FF	E1
	3	0	0800-0FFF	89	0800-0BFF	89	0800-0BFF	89	0800-09FF	89
		1					0C00-0FFF	A9	0A00-0BFF	A9
		2			0C00-0FFF	C9			0C00-0DFF	C9
		3							0E00-0FFF	E9
	5	0	1000-17FF	91	1000-13FF	91	1000-13FF	91	1000-11FF	91
		1					1400-17FF	B1	1200-13FF	B1
		2			1400-17FF	D1			1400-15FF	D1
		3							1600-17FF	F1
	7	0	1800-1FFF	99	1800-1BFF	99	1800-1BFF	99	1800-19FF	99
		1					1C00-1FFF	B9	1A00-1BFF	B9
		2			1C00-1FFF	D9			1C00-1DFF	D9
		3							1E00-1FFF	F9
	2	0	0200-27FF	85	2000-23FF	85	2000-23FF	85	2000-21FF	85
		1					2400-27FF	A5	2200-23FF	A5
		2			2400-27FF	C5			2400-25FF	C5
		3							2600-27FF	E5
	4	0	2800-2FFF	8D	2800-2BFF	8D	2800-2BFF	8D	2800-29FF	8D
		1					2C00-2FFF	AD	2A00-2BFF	AD
		2			2C00-2FFF	CD			2C00-2DFF	CD
		3							2E00-2FFF	ED
	6	0	2000-37FF	95	3000-33FF	95	3000-33FF	95	3000-31FF	95
		1					3400-37FF	B5	3200-33FF	B5
		2			3400-37FF	D5			3400-35FF	D5
		3							3600-37FF	F5
	8	0	3800-3FFF	9D	3800-3BFF	9D	3800-3BFF	9D	3800-39FF	9D
		1					3C00-3FFF	BD	3A00-3BFF	BD
		2			3C00-3FFF	0D			3C00-3DFF	DD
		3							3E00-3FFF	FD
2	1	0	4000-47FF	82	4000-43FF	82	4000-43FF	82	4000-41FF	82
		1					4400-47FF	A2	4200-43FF	A2
		2			4400-47FF	C2			4400-45FF	C2
		3							4600-47FF	F2
	3	0	4800-4FFF	8A	4800-4BFF	8A	4800-4BFF	8A	4800-49FF	8A
		1					4C00-4FFF	AA	4A00-4BFF	AA
		2			4C00-4FFF	CA			4C00-4DFF	CA
		3							4E00-4FFF	EA
	5	0	5000-57FF	92	5000-53FF	92	5000-53FF	92	5000-51FF	92
		1					5400-57FF	B2	5200-53FF	B2
		2			5400-57FF	D2			5400-55FF	D2
		3							5600-57FF	F2
	7	0	5800-5FFF	9A	5800-5BFF	9A	5800-5BFF	9A	5800-59FF	9A
		1					5C00-5FFF	BA	5A00-5BFF	BA
		2			5C00-5FFF	DA			5C00-5DFF	DA
		3							5E00-5FFF	FA
	2	0	6000-67FF	86	6000-63FF	86	6000-63FF	86	6000-61FF	86
		1					6400-67FF	A6	6200-63FF	A6
		2			6400-67FF	C6			6400-65FF	C6
		3							6600-67FF	E6
	4	0	6800-6FFF	8E	6800-6BFF	8E	6800-6BFF	8E	6800-69FF	8E
		1					6C00-6FFF	AE	6A00-6BFF	AE
		2			6C00-6FFF	CE			6C00-6DFF	CE
		3							6E00-6FFF	EE
	6	0	7000-77FF	96	7000-73FF	96	7000-73FF	96	7000-71FF	96
		1					7400-77FF	B6	7200-73FF	B6
		2			7400-77FF	D6			7400-75FF	D6
		3							7600-77FF	F6
	8	0	7800-7FFF	9E	7800-7BFF	9E	7800-79FF	9E	7800-79FF	9E
		1					7C00-7FFF	BE	7A00-7BFF	BE
		2			7C00-7FFF	DE			7C00-7DFF	DE
		3							7E00-7FFF	FE
3	1	0	8000-87FF	83	8000-83FF	83	8000-83FF	83	8000-81FF	83
		1					8400-87FF	A3	8200-83FF	A3
		2			8400-87FF	C3			8400-85FF	C3
		3							3600-87FF	E3
	3	0	8800-8FFF	8B	8800-8BFF	8B	8800-8BFF	8B	8800-89FF	8B
		1					8C00-8FFF	AB	8A00-8BFF	CB
		2			8C00-8FFF	CB			8C00-8DFF	EB
		3							8E00-8FFF	EB
	5	0	9000-97FF	93	9000-93FF	93	9000-93FF	93	9000-91FF	93
		1					9400-97FF	B3	9200-93FF	B3
		2			9400-97FF	D3			9400-95FF	D3
		3							9600-97FF	F3
	7	0	9800-9FFF	9B	9800-9BFF	9B	9800-9BFF	9B	9800-99FF	9B
		1					9C00-9FFF	B8	9A00-9BFF	BB
		2			9C00-9FFF	DB			9C00-9DFF	DB
		3							9E00-9FFF	FB
	2	0	A000-A7FF	87	A000-A3FF	87	A000-A3FF	87	A000-A1FF	87
		1					A400-A7FF	A7	A200-A3FF	A7
		2			A400-A7FF	C7			A400-A5FF	C7
		3							A600-A7FF	E7
	4	0	A800-AFFF	8F	A800-ABFF	8F	A800-ABFF	8F	A800-A9FF	8F
		1					AC00-AFFF	AF	AA00-ABFF	AF
		2			AC00-AFFF	CF			AC00-ADFF	CF
		3							AE00-AFFF	FF
	6	0	B000-B7FF	97	B000-B3FF	97	B000-B3FF	97	B000-B1FF	97
		1					B400-B7FF	B7	B200-B3FF	B7
		2			B400-B7FF	D7			B400-B5FF	D7
		3							B600-B7FF	F7
	8	0	B800-BFFF	9F	B800-BBFF	9F	B800-BBFF	9F	B800-B9FF	9F
		1					BC00-BFFF	BF	BA00-BBFF	BF
		2			BC00-BFFF	DF			BC00-BDFF	DF
		3							BE00-BFFF	FF
4	1	0	C000-C7FF	84	C000-C3FF	84	C000-C3FF	84	C000-C1FF	84
		1					C400-C7FF	A4	C200-C3FF	A4
		2			C400-C7FF	C4			C400-C5FF	C4
		3							C600-C7FF	E4
	3	0	C800-CFFF	8C	C800-CBFF	8C	C800-CBFF	8C	C800-C9FF	8C
		1					CC00-CFFF	AC	CA00-CBFF	AC
		2			CC00-CFFF	CC			CC00-CDFF	CC
		3							CE00-CFFF	EC
	5	0	D000-D7FF	94	D000-D3FF	94	D000-D3FF	94	D000-D1FF	94
		1					D400-D7FF	B4	D200-D3FF	B4
		2			D400-D7FF	D4			D400-D5FF	D4
		3							D600-D7FF	F4
	7	0	D800-DFFF	9C	D800-DBFF	9C	D800-DBFF	9C	D800-D9FF	9C
		1					DC00-DFFF	BC	DA00-DBFF	BC
		2			DC00-DFFF	DC			DC00-DDFF	DC
		3							DE00-DFFF	FC
	2	0	E000-E7FF	88	E000-E3FF	88	E000-E3FF	88	E000-E1FF	88
		1					E400-E7FF	A8	E200-E3FF	A8
		2			E400-E7FF	C8			E400-E5FF	C8
		3							E600-E7FF	E8
	4	0	E800-EFFF	90	E800-E8FF	90	E800-EBFF	90	E800-E9FF	90
		1					EC00-EFFF	B0	EA00-EBFF	B0
		2			EC00-EFFF	D0			EC00-EDFF	D0
		3							EE00-EFFF	F0
	6	0	F000-F7FF	98	F000-F3FF	98	F000-F3FF	98	FF00-F1FF	98
		1					F400-F7FF	B8	F200-F3FF	B8
		2			F400-F7FF	D8			F400-F5FF	D8
		3							F600-F7FF	F8
	8	0	F800-FFFF	A0	F800-FBFF	A0	F800-FBFF	A0	F800-FBFF	A0
		1					FC00-FFFF	C0	FA00-FBFF	C0
		2			FC00-FFFF	E0			FC00-FDFF	E0
		3							FE00-FFFF	80

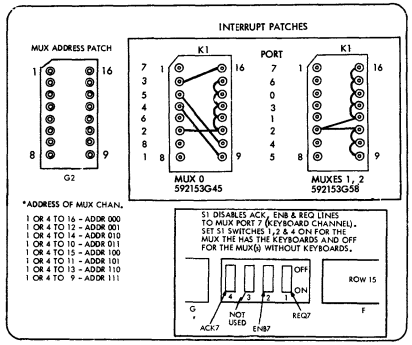
DISPLAY DATA MEMORY BUFFER ASSIGNMENTS

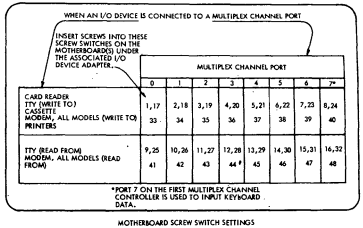


SERIAL ADAPTER PATCHING



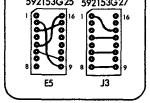
MULTIPLEX CHANNEL CONTROLLER KEYBOARD, INTERRUPT AND ADDRESS PATCHES





IPARS MODEM ADAPTER PATCHES

INSERT THESE PATCH PLUGS INTO BOARD LOCATIONS E5 AND J3



MONITOR CONTROLLER* CHARACTER/LINE FORMAT E6 SWITCH SETTINGS**

E6 CHIP SWITCH SETTING	64 CHAR. 15 LINES	64 CHAR. 16 LINES	64 CHAR. 30 LINES
E6-1	OPEN	OPEN	OPEN
E6-2	OPEN	CLOSED	OPEN
E6-3	OPEN	OPEN	CLOSED
E6-4	CLOSED	CLOSED	CLOSED
E6-5	OPEN	OPEN	OPEN
E6-6	OPEN	OPEN	CLOSED
E6-7	CLOSED	CLOSED	CLOSED
E6-8+	OPEN	CLOSED	OPEN

*B MODIFIED BOARD,

**CLOSED = 1; OPEN = 0. SEE FEATURE BOARD SWITCH SETTING PROCEDURE

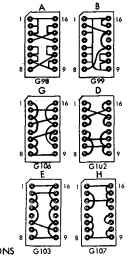
+ USED ON SOME M.C.'S (USED ON ALL 16 LINE M.C.'S)

IPARS SYSTEM CONFIGURATION VARIABLE PATCHES, SWITCHES AND REMOTE PRINTER ADDRESSES

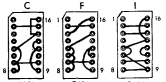
MULTI-INTERFACE SERIAL ADAPTER (MISA) PATCHING (592153-)

INSERT THESE FOR THIS MODEL MISA 593296-	PLUGS INTO M5	PLUGS INTO B2
G1 TERMINET 300 BAUD	A	C
G3 TERMINET 1200 BAUD	B	C
G5 TTY 110 BAUD	G	F
G7 TTY 50 BAUD	D	F
G9 TTY 75 BAUD	E	F
G11 TICKET & BOARDING PASS PRINTER	H	I

M5 PATCH CONFIGURATIONS (BAUD RATES)



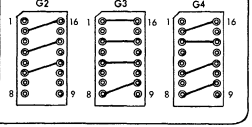
B2 PATCH CONFIGURATIONS (CONTROL)



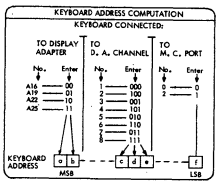
DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

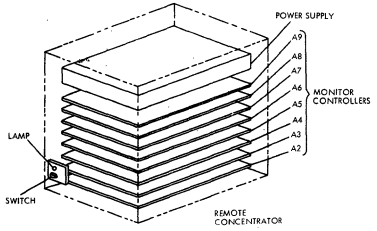
FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-) D15	J16
64 X 30 SPLIT SCREEN	G2	G3
64 X 15 OR 16	G2	G4

PATCH PLUG CONFIGURATIONS 592153-

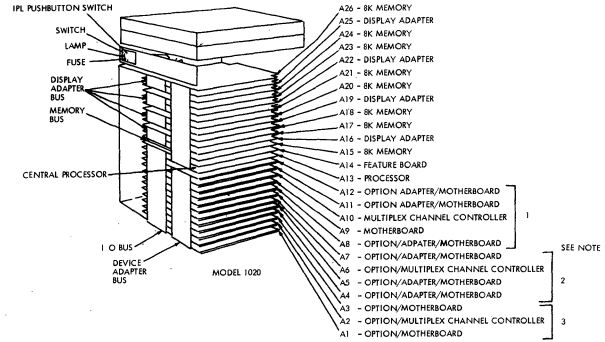


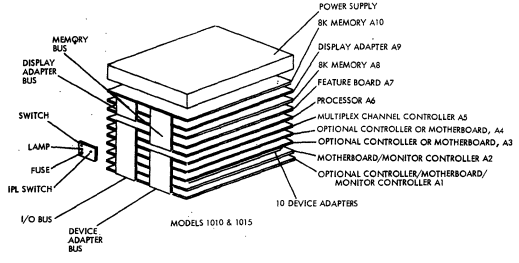
KEYBOARD ADDRESS COMPUTATION





POWER SUPPLIES





NOTE:
MONITOR CONTROLLERS ARE INSTALLED IN SLOTS A1, A2, A3 & A4 WHEN ONLY 2 MULTIPLEX CONTROLLERS ARE USED. MONITOR CONTROLLERS ARE INSTALLED IN A7, A8 & A9 WHEN 3 MULTIPLEX CONTROLLERS ARE USED.

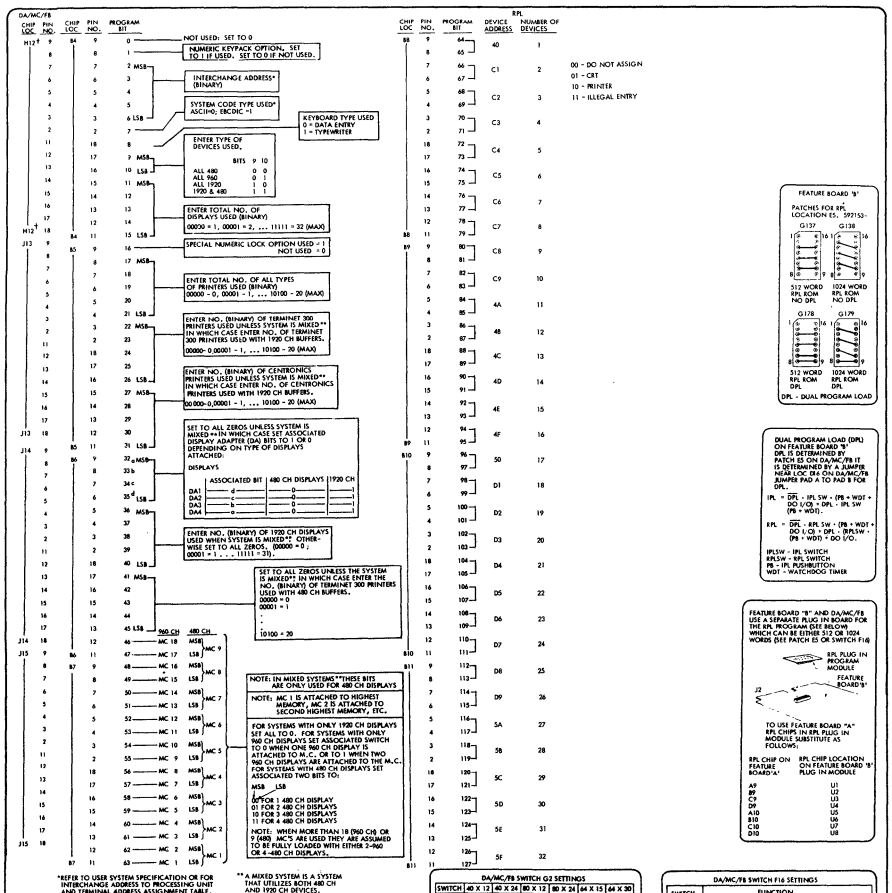
COMMUNICATIONS REGION TABLE

LOAD SIZE OF PROGRAM
KEYBOARD MODULE
SECOND HALF OF INITIALIZER
TASK SUPERVISOR
PRINTER INITIALIZER
SERIAL PRINTER ROUTINE
TICKET & BOARDING PASS PRINTERS
INITIALIZER
PRINTER STATUS TABLES
DISPLAY STATUS TABLES
NUMBER OF DISPLAYS
NUMBER OF PRINTERS
CCC COUNTER
NUMBER OF MESSAGES RECEIVED
NUMBER OF MESSAGES TRANSMITTED
EOMC'S IN TKT AND BOARDING PASS MESSAGES
DATA LOST COUNTER
CARRIER LOST COUNTER
IOCQ'S FOR DISPLAYS
IOCQ'S FOR PRINTERS
OUTPUT - TO HOST - BUFFER
VALID TERMINAL ADDRESSES
VALID PRINTER ADDRESSES
AIRLINE ID
INTERCHANGE 1
INTERCHANGE 2
LOCATION 0010 CONTAINS THE ADDRESS OF THIS TABLE

LED MEMORY BUFFER ASSIGNMENTS

Adaptor	Channel	1920 Character Display	960 Character Display		480 Character Display			
			Mon. 0	Mon. 1	Mon. 0	Mon. 1	Mon. 2	Mon. 3
1	1	0780	03C0	07C0	01E0	03E0	05E0	07E0
	2	2780	23C0	27C0	21E0	23E0	25E0	27E0
	3	0F80	0BC0	0FC0	09E0	0BE0	0DE0	0FE0
	4	2F80	2BC0	2FC0	29E0	2BE0	2DE0	2FE0
	5	1780	13C0	17C0	11E0	13E0	15E0	17E0
	6	3780	33C0	37C0	31E0	33E0	35E0	37E0
	7	1F80	1BC0	1FC0	19D0	1BE0	1DE0	1FE0
	8	3F80	3BC0	3FC0	39E0	3BE0	3DE0	3FE0
2	1	4780	43C0	47C0	41E0	43E0	45E0	47E0
	2	6780	63C0	67C0	61E0	63E0	65E0	67E0
	3	4F80	43C0	4FC0	49E0	4BE0	4DE0	4FE0
	4	6F80	6BC0	6FC0	69E0	6BE0	6DE0	6FE0
	5	5780	53C0	57C0	51E0	53E0	55E0	57E0
	6	7780	73C0	77C0	71E0	73E0	75E0	77E0
	7	5F80	5BC0	5FC0	59E0	5BE0	5DE0	5FE0
	8	7F80	7BC0	7FC0	79E0	7BE0	7DE0	7FE0
3	1	8780	83C0	87C0	81E0	83E0	85E0	87E0
	2	A780	A3C0	A7C0	A1E0	A3E0	A5E0	A7E0
	3	8F80	8BC0	8FC0	89E0	8BE0	8DE0	8FE0
	4	AF80	ABC0	AFC0	A9E0	ABE0	ADE0	AFE0
	5	9780	93C0	97C0	91E0	93E0	95E0	97E0
	6	B780	B3C0	B7C0	B1E0	B3E0	B5E0	B7E0
	7	9F80	9BC0	9FC0	99E0	9BE0	9DE0	9FE0
	8	BF80	BBC0	BFC0	B9E0	BBE0	8DC0	BFE0
4	1	C780	C3C0	C7C0	C1E0	C3E0	C5E0	C7E0
	2	E780	E3C0	E7C0	E1E0	E3E0	E5E0	E7E0
	3	CF80	C3C0	CFC0	C9E0	CBE0	CDE0	CFE0
	4	EF80	EBC0	EFC0	E9E0	EBE0	EDE0	EFE0
	5	D780	D3C0	D7C0	D1E0	D3E0	D5E0	D7E0
	6	F780	F3C0	F7C0	F1E0	F3E0	F5E0	F7E0
	7	DF80	D8C0	D7C0	D9E0	DBE0	DDE0	DFE0
	8	FF80	FBC0	FFC0	F9E0	FBE0	FDE0	FFE0

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR SEARS 3271 REMOTE EMULATOR 933172



*REFER TO USER SYSTEM SPECIFICATION OR FOR INTERCHANGE ADDRESS TO PROCESSING UNIT AND TERMINAL ADDRESS ASSIGNMENT TABLE.

** A MIXED SYSTEM IS A SYSTEM THAT UTILIZES BOTH 480 CH AND 1920 CH DEVICES.

† J12 ON SOME OLDER BOARDS

MANUAL DATA CHIP LOC

DA/MC/FB	FEATURE BOARD B	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX) IPL	512 RPL	1024 RPL
H12 †	B4	40, 41	40, 41	40, 41
J13	B5	42, 43	42, 43	42, 43
J14	B6	44, 45	44, 45	44, 45
J15	B7	46, 47	46, 47	46, 45
	B8	80, 81	400, 401	800, 801
	B9	82, 83	402, 403	802, 803
	B10	84, 85	404, 405	804, 805
	B11	86, 87	406, 407	806, 807

MANUAL DATA CHIP 594113-11 PIN NUMBERS

CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN BK OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

MONITOR CONTROLLER C CHARACTER/LINE FORMAT I6 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12	24	OPTIONS
1	——	—	—	NOTE 1
2	——	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	——
4	OPEN	CLOSED	CLOSED	——
5	CLOSED	CLOSED	CLOSED	——
6	CLOSED	OPEN	CLOSED	——
7	OPEN	CLOSED	CLOSED	——
8	——	—	—	NOTE 3

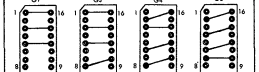
NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS

592153-



FOR THIS DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-)	INTO BOARD LOCATIONS D15 AND J16
80 X 24	G1	G3
80 X 12	G1	G4
40 X 12	G1	G5

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17	2,18	3,19	4,20	5,21	6,22	7,23	8,24
	33	34	35	36	37	38	39	40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25	10,26	11,27	12,28	13,29	14,30	15,31	16,32
	41	42	43	44	45	46	47	48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (READ FROM) IS ASSIGNED TO PORT 1 OF FIRST MULTIPLEX CHANNEL CONTROLLER

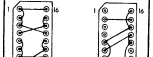
MODEM (WRITE TO) IS ASSIGNED TO PORT 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS.

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MISA PATCHES

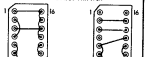
TERMINET 300 PRINTER



592153G98 — MS - BOARD LOCATION = B2

592153G101

CENTRONICS PRINTER



592153G107 — MS - BOARD LOCATION = B2

592153G124

NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT			
	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5	See Below			
6				
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.

When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.

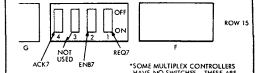
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1; Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MULTIPLEX CHANNEL CONTROLLER

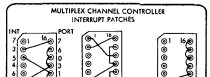
DISABLE, ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES, THESE ARE NOT ALWAYS INTERCHANGEABLE, REFER TO FIELD BULLETIN CM-084-1.

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



FOR MODEM INT LEVELS

FIRST MULTIPLEX CHANNEL CONTROLLER

FOR MODEM INT LEVEL 8

2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEMS			
SEND	0	2	5 OR 8
REC	0	1	5 OR 8
PRINTERS 1-4	0	3-6	2
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2

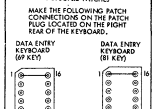
MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

G2 BOARD LOCATION

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	I OR 4 TO 16
ADDR 1	I OR 4 TO 12
ADDR 2	I OR 4 TO 14
ADDR 3	I OR 4 TO 10
ADDR 4	I OR 4 TO 15
ADDR 5	I OR 4 TO 11
ADDR 6	I OR 4 TO 13
ADDR 7	I OR 4 TO 9

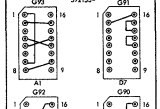
KEYBOARD PATCHES

MAKE THE FOLLOWING PATCH CONNECTIONS ON THE PATCH PLUG LOCATED ON THE RIGHT REAR OF THE KEYBOARD.



MODEM ADAPTER PATCHES

592153-

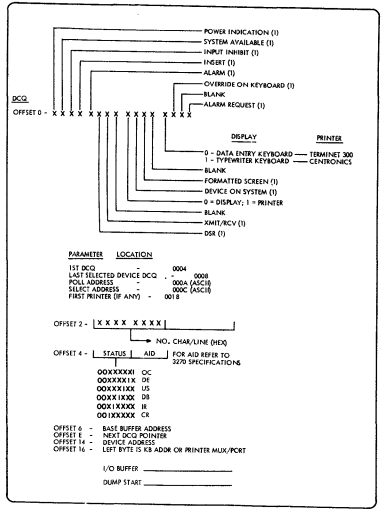


PROCESSING UNIT AND TERMINAL ADDRESS ASSIGNMENTS

Encode on Feature Board	Column 1 Use this column to find: • Device Selection, • Specific Poll, • General Poll, and • Fixed Return Addresses		Column 2 Use this column to find: • PTS Selection Addresses	
Processing Unit or Device Number	EBCDIC Hex	ASCII Hex	EBCDIC Hex	ASCII Hex
0	40	20	60	2D
1	C1	41	61	2F
2	C2	42	E2	53
3	C3	43	E3	54
4	C4	44	E4	55
5	C5	45	E5	56
6	C6	46	E6	57
7	C7	47	E7	58
8	C8	48	E8	59
9	C9	49	E9	5A
10	4A	58	6A	5C
11	4B	2E	6B	2C
12	4C	3C	6C	25
13	4D	28	6D	5F
14	4E	2B	6E	3E
15	4F	21	6F	3F
16	D0	26	F0	30
17	D1	4A	F1	31
18	D2	4B	F2	32
19	D3	4C	F3	33
20	D4	4D	F4	34
21	D5	4E	F5	35
22	D6	4F	F6	36
23	D7	50	F7	37
24	D8	51	F8	38
25	D9	52	F9	39
26	5A	5D	7A	3A
27	5B	24	7B	23
28	5C	2A	7C	40
29	5D	29	7D	27
30	5E	3B	7E	3D
31	5F	5E	7F	22

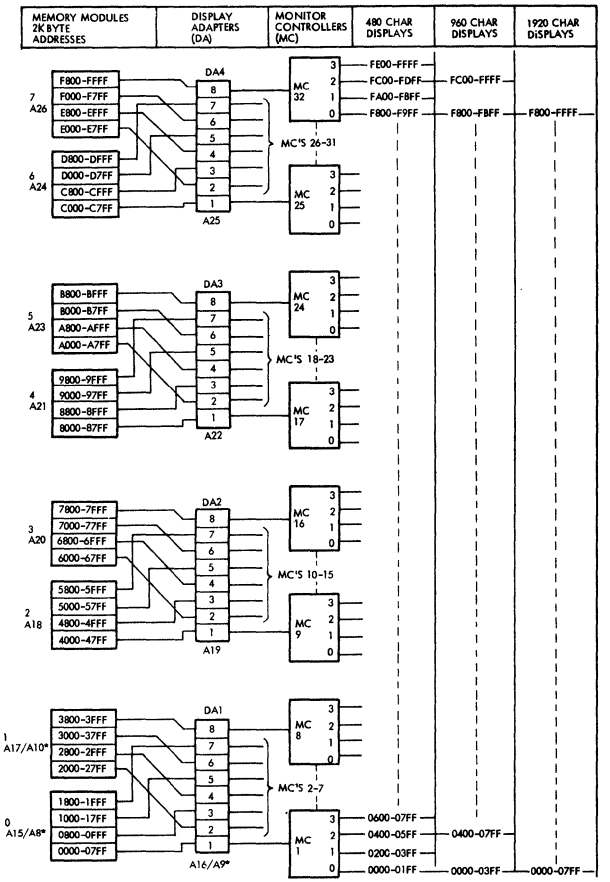
NOTE

I/O channcter address 7F is used as the device address to specify a General Poll operation.



PATCH AND SWITCH SETTINGS AND SOFTWARE NOTES FOR SEARS 3271 REMOTE EMULATOR 933172

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, A9 & A10 FOR 1010 & 1015

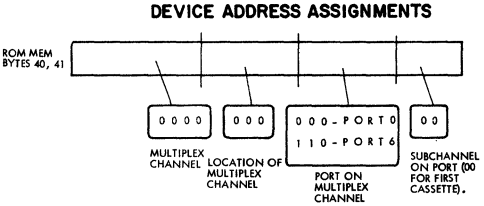
NOTES

ALL DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. IN A MIXED SYSTEM 1920 CH DISPLAYS ARE ASSIGNED BEFORE 480 CH DISPLAYS. ALSO THE STARTING MEMORY ADDRESSES ARE DETERMINED BY WHICH DISPLAY ADAPTERS ARE ASSIGNED TO 1920 CH AND 480 CH DISPLAYS (SEE C4 ON F.B.'A9'). IF A SYSTEM IS MIXED OR DOES NOT FULLY LOAD ALL M.C.'s, PRINTER BUFFERS WILL BE ASSIGNED TO THE UNUSED AREAS. IN A MIXED ** SYSTEM PRINTERS ARE ASSIGNED AS FOLLOWS:

1 CENTRONICS - 1920 CH BUFFER
2 TERMINET - 1920 CH BUFFER
3 CENTRONICS - 480 CH BUFFER
4 TERMINET - 480 CH BUFFER

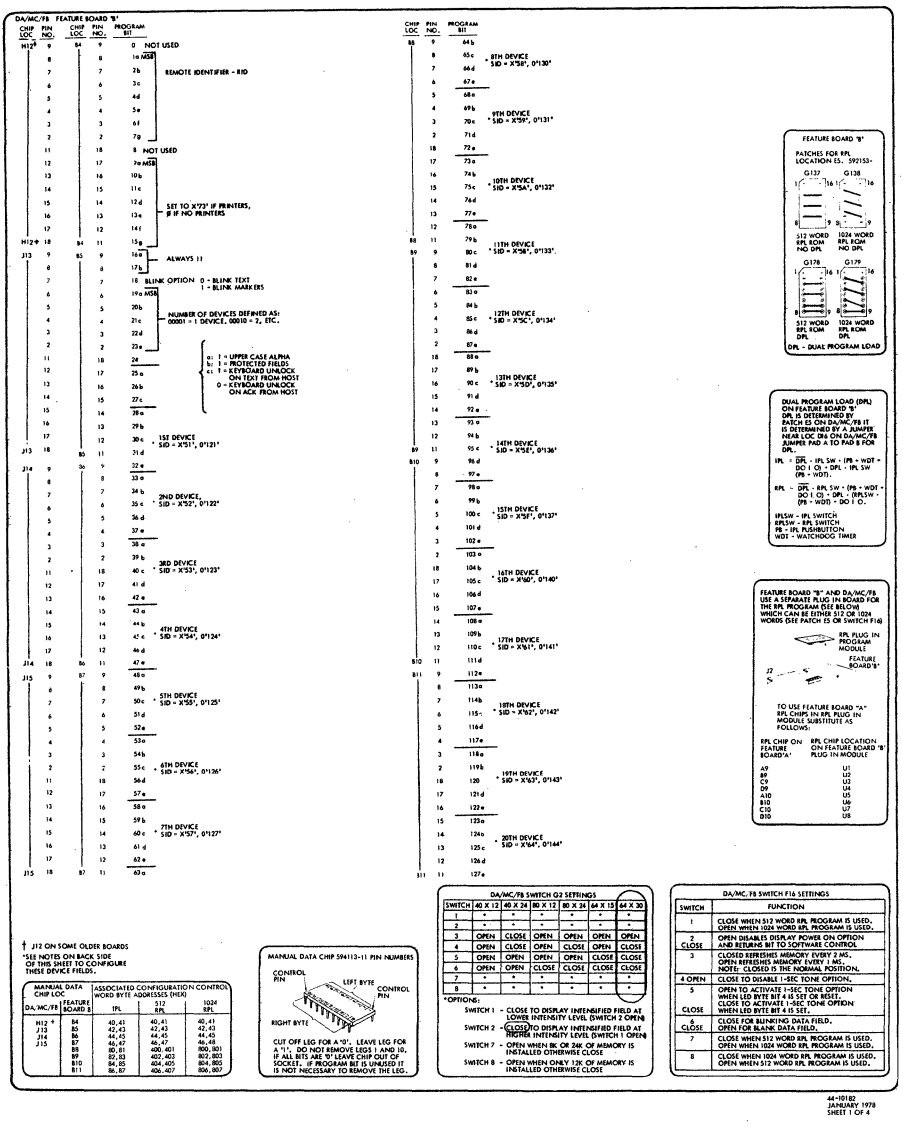
THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULES A17/A10* AND A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

STATE OF NEW YORK U250 933742



† J12 ON SOME OLDER BOARDS

*SEE NOTES ON BACK SIDE OF THIS SHEET TO CONFIGURE THESE DEVICE FIELDS.

MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA/MC/FB	FEATURE BOARD B	IPL	512 RPL	1024 RPL
J12 †	B4	40,41	40,41	40,41
J13	B5	42,43	42,43	42,43
J14	B6	44,45	44,45	44,45
J15	B7	46,47	46,47	46,48
	B8	80,81	400,401	800,801
	B9	82,83	402,403	802,803
	B10	84,85	404,405	804,805
	B11	86,87	406,407	806,807

MANUAL DATA CHIP 594113-11 PIN NUMBERS

CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH Q2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	OPEN	CLOSE	OPEN	CLOSE	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT BRIGHTER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2 CLOSE	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4 OPEN	CLOSE TO DISABLE 1-SEC TONE OPTION.
5 CLOSE	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6 CLOSE	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	CLOSED WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
8	CLOSE WHEN 1024 WORD RPL PROGRAM IS USED. OPEN WHEN 512 WORD RPL PROGRAM IS USED.

PROCEDURE TO SET 5-BIT DEVICE FIELDS

THERE IS ONE FIELD FOR EACH DEVICE.

EACH DEVICE CAN HAVE EITHER A DISPLAY OR PRINTER OR BOTH ATTACHED. EACH PRINTER HAS THE OPTION OF PROVIDING THE LOCAL PRINT FUNCTION FOR OTHER DISPLAYS. THE PROGRAM ASSIGNS THE PRINTERS USED AS LOCAL PRINTERS ASCENDING SEQUENTIAL NUMBERS (1-7) STARTING WITH THE FIRST DEVICE FIELD THAT HAS THE LOCAL PRINT BIT (c) SET TO '1'. THESE NUMBERS ALLOW THE OTHER DISPLAYS TO ADDRESS THE PRINTER FOR LOCAL PRINT.

BIT

a — SET TO '1' WHEN A DISPLAY IS ATTACHED OTHERWISE SET TO '0'.

b — SET TO '1' WHEN A PRINTER IS ATTACHED OTHERWISE SET TO '0'.

BIT

c MSB
d
e

ENTER SEQUENTIAL NUMBER OF PRINTER THAT IS TO PROVIDE LOCAL PRINT FUNCTION (SEE EXAMPLE BELOW). WHEN NO LOCAL PRINT FUNCTION IS REQUIRED SET BITS TO 000.

BIT

c — SET TO '1' IF THIS PRINTER IS TO PROVIDE A LOCAL PRINT FUNCTION FOR OTHER DISPLAYS. OTHERWISE SET TO '0'.

PRINTER TYPE

d 0 0 1 1
e 0 1 0 1

- CENTRONICS, EXTEL, TERMINET — 80 CHAR LOGICAL LINE LENGTH
- CENTRONICS, 120 CHAR LINE LENGTH
- EXTEL, TERMINET, 40 CHAR LINE LENGTH

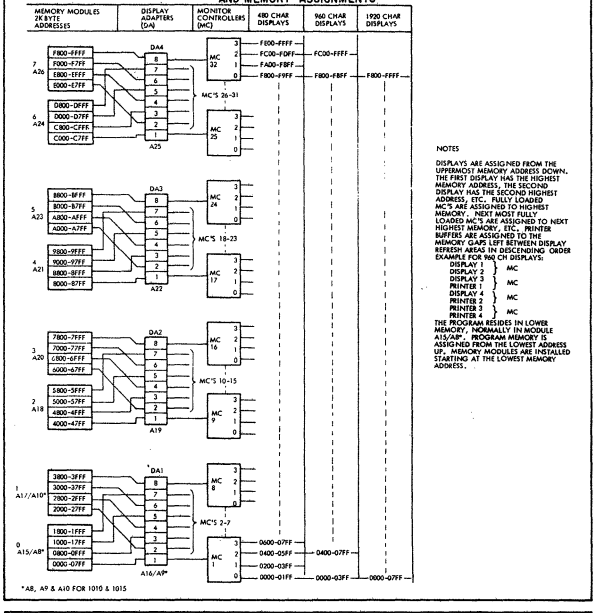
EXAMPLE:

Number of devices = 5

Devices 1 & 2 are displays with printers
Devices 3 & 4 are displays without printers
Device 5 — 1 printer with no display

	Program Bits		Set to	
	28	a	1	Display
	29	b	1	Printer
DEVICE 1	30	c	1	Used as local printer (first local printer so it is assigned
	31	d	0	EXTEL sequential #1).
	32	e	0	
	33	a	1	Display
	34	b	1	Printer
DEVICE 2	35	c	0	Printer not used for local print (therefore it does not have
	36	d	0	CENTRONICS a sequential #).
	37	e	1	
	38	a	1	Display
	39	b	0	No printer
DEVICE 3	40	c	0	This display uses printer assigned sequential #1 for
	41	d	0	local print.
	42	e	1	
	43	a	1	Display
	44	b	0	No printer
DEVICE 4	45	c	0	This display uses printer assigned sequential #2 for
	46	d	1	local print.
	47	e	0	
	48	a	0	No
	49	b	1	Printer
DEVICE 5	50	c	1	Used as local printer (second local printer so it is
	51	d	0	CENTRONICS assigned sequential #2)
	52	e	1	

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



*A8, A9 & A10 FOR 1010 & 1015

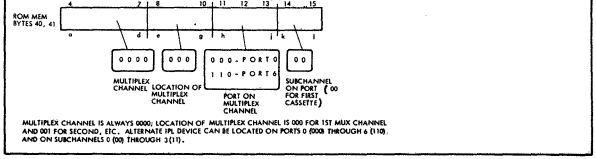
NOTES

DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. FULLY LOADED MC'S ARE ASSIGNED TO HIGHEST MEMORY. NEXT MOST FULLY LOADED MC'S ARE ASSIGNED TO NEXT HIGHEST MEMORY, ETC. PRINTER BUFFERS ARE ASSIGNED TO THE MEMORY GAPS LEFT BETWEEN DISPLAY REFRESH AREAS IN DESCENDING ORDER EXAMPLE FOR 960 CH DISPLAYS:

DISPLAY 1 } MC
DISPLAY 2
DISPLAY 3 } MC
PRINTER 1
DISPLAY 4 } MC
PRINTER 2
PRINTER 3 } MC
PRINTER 4

THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC., ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

MONITOR CONTROLLER B AND C

CHARACTER/ LINE FORMAT E6 SWITCH SETTINGS

SWITCH	40 X 12	80 X 12	1/24	64 X 15	128	OPTIONS
1	—	—	—	—	—	NOTE 1
2	—	—	—	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	OPEN	CLOSED	—
4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
5	CLOSED	CLOSED	CLOSED	OPEN	OPEN	—
6	CLOSED	OPEN	OPEN	OPEN	OPEN	—
7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	—
8	—	—	—	—	—	NOTE 3

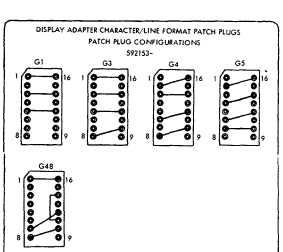
NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CRT, A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS

592153-



FOR THIS DISPLAY CHAR/LINES NO. OF LINES FORMATS	INSERT THESE PATCHES* (592153-)	INTO BOARD LOCATIONS D15 AND J16	
		G1	G3
80 X 24			
64 X 30 & SPLIT SCREEN		G2	G3
80 X 12		G7	G4
64 X 15 OR 16		G2	G4
40 X 12		G5	G5
40 X 24		G1	G48

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD, UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM: ALL MODELS (WRITE TO PRINTER)	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PORT 1 AND 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER ARE NOT USED

FIRST PRINTER IS ASSIGNED TO PORT 3 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEM:			
SEND	0	2	5
REC	0	1	5
PRINTERS:			
1-4	0	3-6	2
5-12	1	0-7	2
13-15	2	0-7	2

NOTE: TERMINET AND EXTEL PRINTERS MUST BE ASSIGNED FIRST

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

	FORMAT			
Switch	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5				
6		See Below		
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.
When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip — D9

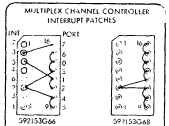
These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.

for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

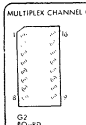
MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



FIRST MULTIPLEX CHANNEL CONTROLLER

2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH



FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

MONITOR CONTROLLER B-16

E6 CHIP SWITCH SETTING	40 CHAR. 12 LINES	80 CHAR. 12 LINES	64 CHAR. 15/16 LINES	80 CHAR. 24 LINES	64 CHAR. 30 LINES	40 CHAR. 24 LINES	STEP SCAN*
E6-1	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	CLOSED
E6-2	OPEN	OPEN	OPEN*	OPEN	OPEN	OPEN	OPEN
E6-3	OPEN	OPEN	OPEN	CLOSED	CLOSED	CLOSED	CLOSED
E6-4	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
E6-5	CLOSED	OPEN	OPEN	CLOSED	OPEN	CLOSED	**
E6-6	CLOSED	OPEN	OPEN	OPEN	OPEN	CLOSED	OPEN
E6-7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
E6-8**	OPEN	OPEN	OPEN*	OPEN	OPEN	OPEN	OPEN

*USABLE ONLY ON 24 OR 30 LINE FORMAT. SPACING BETWEEN LINES IS ADJUSTABLE BY SETTING K85.

**SET AS INDICATED FOR 24 OR 30 LINE FORMAT.

*CLOSED FOR 16 LINE FORMAT

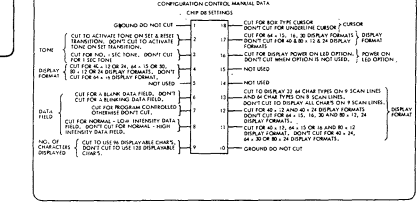
**E6-8 IS USED ON SOME MC'S (IT IS USED ON ALL 16 LINE MC'S).

NOTE: WHEN MC IS USED WITH SPLIT SCREEN DISPLAYS A JUMPER IS CONNECTED BETWEEN X12 PIN 15 AND X7 PIN 14.

MONITOR CONTROLLER F

CONFIGURATION CONTROL MANUAL DATA

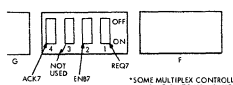
CHIP D6 SETTINGS



MULTIPLEX CHANNEL CONTROLLER

DISABLE/ENABLE PORT 7 SWITCH*

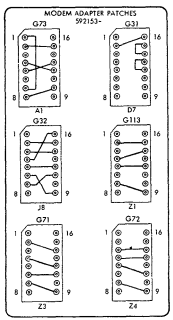
S1 DISABLES +OK, EN8 & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

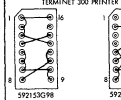
MODEM ADAPTER PATCHES

592153-



MISA PATCHES

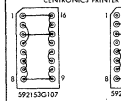
TERMINET 300 PRINTER



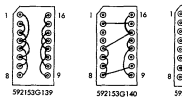
NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

CENTRONICS PRINTER



EXTEL PRINTER



EXTEL MODEL	BAUD RATE	PATCHES M5	PATCHES B2
15,30	165	G139	G140
30	150	G128	G101*
30	300	G98*	G101*

*SEE TERMINET 300

CASSETTE PROGRAM PATCH PROCEDURE

1. IPL OLD CASSETTE.
2. DURING IPL STORE X'8XXX' INTO LOCATION 0 (WHERE XXX = DEVICE ADDRESS OF TARGET DRIVE).
3. WHEN IPL IS COMPLETE LOCATION 0 WILL CONTAIN X'0100'. IF NOT RETRY.
4. ENTER PATCHES. DO NOT PRESS STOP OR RESET.
5. PUT A NEW CASSETTE IN TARGET DRIVE.
6. STORE X'8XXX' INTO LOCATION 0 AS ABOVE. LOCATION 0 WILL CHANGE TO X'0300' TO INDICATE THAT THE DUMP IS IN PROGRESS.
7. THE TAPE WILL REWIND AND STOP WHEN COMPLETE AND LOCATION 0 WILL CONTAIN X'0100'. IF MORE COPIES ARE DESIRED RETURN TO STEP 5.
8. IF AN ERROR OCCURS, THE TAPE WILL TRY TO REWRITE CONTINUOUSLY. TO START OVER INSERT A NEW CASSETTE AND STORE X'8XXX' INTO LOCATION 0.

NOTE: FOR ADDITIONAL INFORMATION REFER TO FIB NO. PS-0018.

COMMUNICATIONS REGION (ADDRESS AT LOCATION X'C')

WORD DISPLACEMENT	DEFINITION	
0	REVISION LEVEL (ASCII)	REVISION SUBLEVEL (ASCII)
1	STATISTICS TABLE ADDRESS	
2	ERROR TABLE ADDRESS	
3	LINE CONTROL BLOCK ADDRESS	
4	ADDRESS OF TABLE CONTAINING DST ADDRESSES	
5	RECEIVE BUFFER ADDRESS	
6	ADDRESS OF FIRST XMIT BUFFER	
7	ADDRESS OF SOFTWARE TIMER CELL	

PRINTER STATUS TABLE (PST ADDR IN DST)

WORD DISPLACEMENT	DEFINITION
0	STATUS | LUN
1	CURRENT PRINT ADDRESS
2	PRINTER BUFFER ADDRESS
3	PRINTER TIMER ADDRESS
4	PRINTER IOCQ ADDRESS
5	PRINTER STATUS FOR HOST
6	LAST PRINTER STATUS FOR HOST

ERROR TABLE (ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION
0	MODEM RECEIVE ERROR COUNTER
1	MODEM TRANSMIT ERROR COUNTER
2	ADDRESSING ERROR COUNTER
3	ILLEGAL CHARACTER ERROR COUNTER
4	CHARACTER PARITY ERROR COUNTER
5	BCC ERROR COUNTER
6	CURSOR ADDRESSING ERROR COUNTERS
7	MODEM RECEIVE IO ACTION ERROR COUNTER
8	XMIT - CARRIER LOST
9	XMIT - DEVICE NOT READY
10	XMIT - DATA LOST

LINE CONTROL BLOCK (LCB ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION	
0	RECEIVE CHANNEL UP/DOWN	
1	CURRENT RECEIVE IOCQ ADDRESS	
2	FIRST RECEIVE IOCQ ADDRESS	
3	.OMPRC RE-ENTRANCE ADDRESS	
4	FIRST MODEM RECEIVE BUFFER ADDRESS	
5	FIRST DST ADDRESS	
6	NUMBER OF DST'S	
7	MODEM RECEIVE TIMER ADDRESS	
8	MODEM RECEIVE LUN	
9	NUMBER OF XMIT BUFFERS AVAILABLE	
A	MODEM XMIT CHANNEL UP/DOWN	
B	MODEM XMIT ERROR FLAG	
C	CURRENT MODEM XMIT IOCQ ADDRESS	
D	FIRST XMIT IOCQ ADDRESS	
E	MODEM XMIT TIMER ADDRESS	
F	INPUT MESSAGE COLLECTION ACTIVE FLAG	
10	MODEM XMIT LUN	
11	MODEM XMIT BUFFER ADDRESS	
12	NOT USED	
13	CURRENT OUTPUT MSG PROCESSOR DST	
14	POLL TIMER ADDRESS	
15	ACK CONTROL BYTE	OUTPUT MESSAGE TYPE
16	SID FROM LAST OUTPUT MSG	DID FROM LAST OUTPUT MESSAGE
17	RID FROM FEATURE BOARD	SID OF LAST INPUT TERMINAL
18	TERMINAL STATUS OF LAST INPUT DEVICE	
19	DST OF LAST DEVICE TO RECEIVE INPUT	

DISPLAY STATUS TABLE (FIRST DST ADDR IN LCB)

WORD DISPLACEMENT	DEFINITION	
0	CURSOR ADDRESS	
1	KEYBOARD NUMBER	STATUS
2	LINK TO NEXT DST	
3	HOME ADDRESS	
4	NOT USED	XMIT LUN
5	HOME FOR DEBUG	
6	LED BYTE ADDRESS	
7	CURSOR ADDRESS DURING MESSAGE COLLECTION	
8	PRINTER STATUS TABLE ADDRESS	
9	SOE ADDRESS	
A	SID	PRINTER STATUS
B	DISPLAY END ADDRESS	
C	NUMBER OF CHAR LEFT ON LINE	
D	MORE STATUS BITS	
E	ATTRIBUTE CHAR POINTER	

STATISTICS TABLE (ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION
0	OUTPUT MESSAGE FROM HOST
1	INPUT MESSAGE TO HOST
2	BROADCAST MESSAGE FROM HOST
3	PRINTER MESSAGE FROM HOST
4	PRINTER STATUS REQUEST FROM HOST
5	MESSAGE WAITING FROM HOST
6	REPLY REQUEST TO HOST
7	RETRANSMIT REQUEST FROM HOST
8	GENERAL POLL FROM HOST
9	SPECIFIC POLL FROM HOST
A	OUTPUT FROM HOST TO ANOTHER RID
B	NO BUSINESS RESPONSE SENT TO HOST
C	MESSAGE WAITING SENT TO HOST
D	PRINTER STATUS SENT TO HOST
E	LOOK-FOR SYNC ISSUED TO MODEM RECEIVE

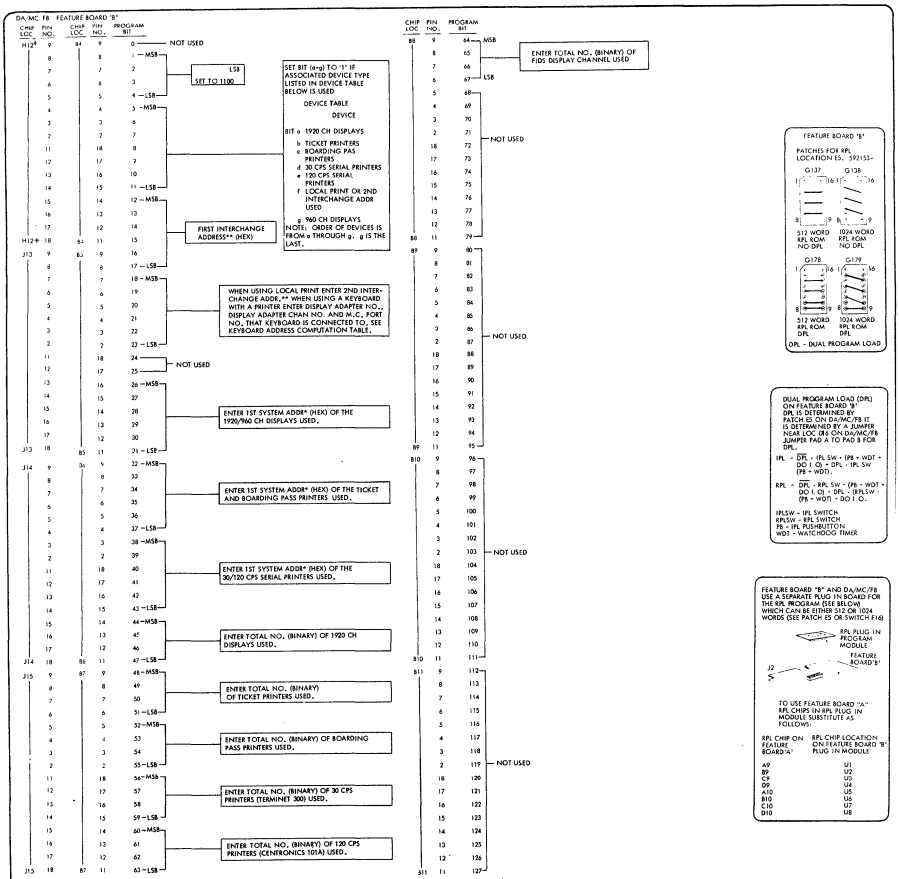
SRM	NODE DEFINITION	
+0	LINK TO NEXT (0=END OF LIST)	
+2	ADDRESS TO START TRACE (LSB ON = INDIRECT)	
+4	NUMBER OF BYTES TO TRACE	
+6	DEVICE ID (BINARY)	DISPLAYED ON TRACE TO IDENTIFY ENTRY
+7	NODE ID (ASCII)	
+8	TRACE MASK*	
+A to A+n	SCRATCH AREA WHERE n = NO. OF BYTES TO TRACE	

*MASK - BIT 0 = 1 SKIP THIS NODE.
BITS 1-15 = 1 SKIP CORRESPONDING WORD (i.e., bit 15 = word 0, bit 14 = word 1)

SRM NODE TYPES

A	MODEM XMIT BUFFER
B	MODEM RECEIVE BUFFER
C	MODEM XMIT PCB
D	MODEM RCV PCB
E	MODEM XMIT PIOT
F	MODEM RECEIVE PIOT
G	MODEM RECEIVE FIOB
H	MODEM XMIT FIOB
I	PRINTER FIOB
J	PRINT BUFFER
K	DISPLAY STATUS TABLE
L	FIRST 16 WORDS OF LCB
M	LAST 9 WORDS OF LCB
P	PRINTER STATUS TABLE
Q	PRINTER IOCQ
R	MODEM RECEIVE IOCQ
S	STATISTICS TABLE
T	MODEM XMIT IOCQ
X	ERROR TABLE
Z	DEFINE BY 'ML' DIRECTIVE

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR FIDS/CONTINENTAL AIRLINES SPECIAL EMULATOR 933927-19



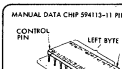
NOTE: CPS = CHARACTERS/SEC.
FOR PATCHING AND SWITCH SETTINGS REFER TO STANDARD PAR/IPARS (44-8016)

*REFER TO USER SYSTEM SPECIFICATION OR CONFIGURATION
EXAMPLE FOR ADDR 14 (HEX) ENTER 01 0100
ab cde f

*J12 ON SOME OLDER BOARDS

MANUAL DATA CHIP LOC DA/MC/FB	FEATURE BOARD 'B'	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX) IPL	512 RPL	1024 RPL
H12 *	B4	40, 41	40, 41	40, 41
J13	B5	42, 43	42, 43	42, 43
J14	B6	44, 45	44, 45	44, 45
J15	B7	46, 47	46, 47	46, 48
	B8	B0, B1	400, 401	800, B0
	B9	B2, B3	402, 403	B02, B03
	B10	B4, B5	404, 405	B04, B05
	B11	B6, B7	406, 407	B06, B07

MANUAL DATA CHIP 594113-11 PIN NUMBERS



CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

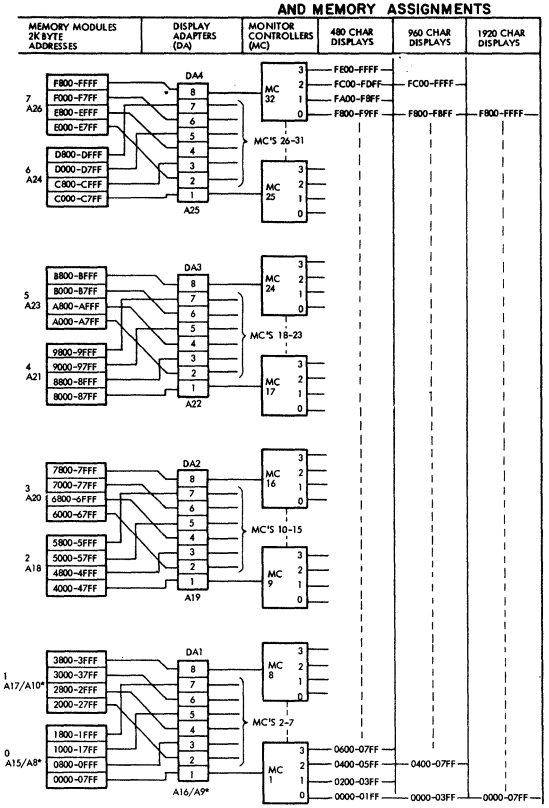
SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS

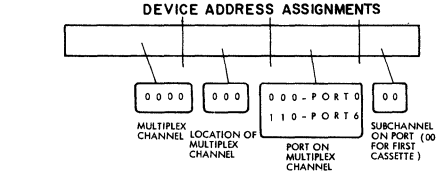


*A8, A9 & A10 FOR 1010 & 1015

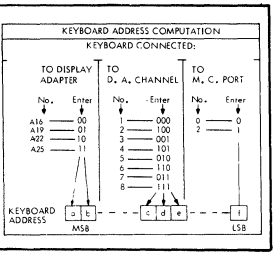
NOTES

DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. THE FIRST DISPLAY HAS THE HIGHEST MEMORY ADDRESS, THE SECOND DISPLAY HAS THE SECOND HIGHEST ADDRESS, ETC. THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULE A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

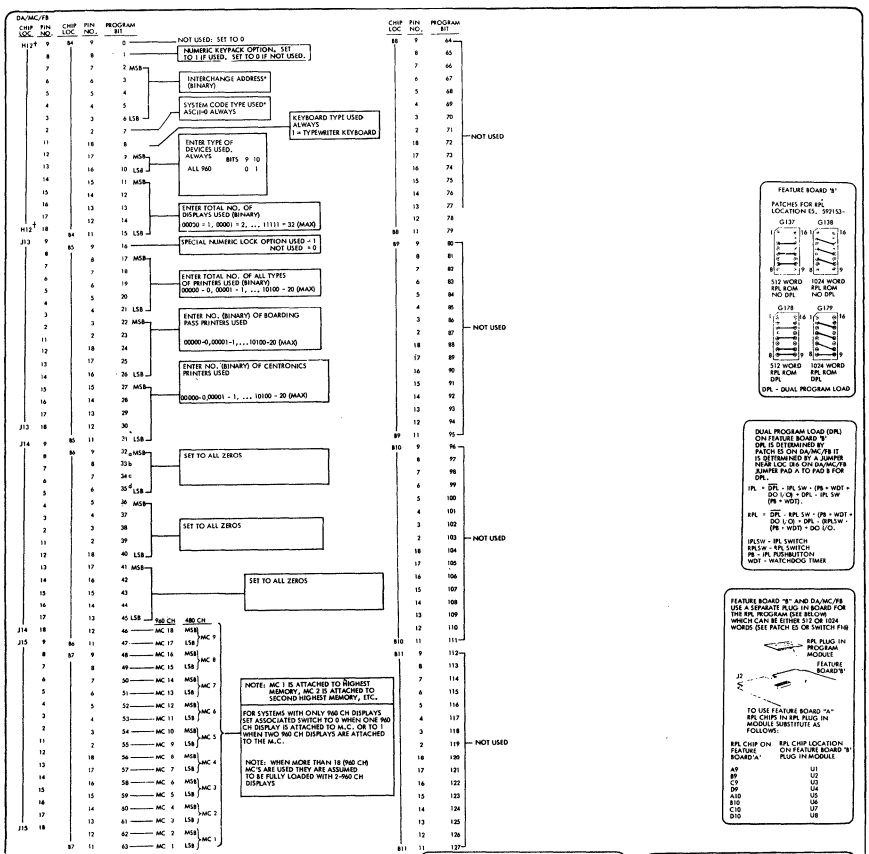
ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110), AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).



PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR DOWNLINE 3271 REMOTE EMULATOR FOR RAYCARGO 933949



MAINMAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA, MC, FB	FEATURE BOARD B	IPL	512 RPL	1024 RPL
H12 †	84	40, 41	40, 41	40, 41
J13	85	42, 43	42, 43	42, 43
J14	86	44, 45	44, 45	44, 45
J15	87	46, 47	46, 47	46, 48
	88	80, 81	400, 401	800, 801
	89	82, 83	402, 403	802, 803
	B10	84, 85	404, 405	804, 805
	B11	86, 87	406, 407	806, 807

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED, OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

NOTE: 64 X 15 IS 960 SIZE FOR RAYCARGO

MONITOR CONTROLLER F - (P/N 860548 - EXCEPT FIRST 250 BOARDS P/N 860864, RAM ONLY)

CONFIGURATION PLUG (D8)

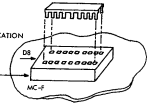
THE MC-F HAS ONE SOCKET WHICH REQUIRES A CONFIGURATION PLUG TO SELECT MOST OF THE AVAILABLE OPTIONS. ANY POSSIBLE COMBINATION OF OPTIONS CAN BE SELECTED BY CUTTING OFF APPROPRIATE LEGS OF THE PLUG.

NOTE: 1. WITHOUT TRANSMITTER MODULE, THE MC-F IS COMPLETELY BACKWARDS COMPATIBLE WITH THE PRESENT D.A. "C".

2. WITH TRANSMITTER MODULE, M-FC HAS THE ADDED COAX CABLE OPTION USED WITH D.A. "C".

CONFIGURATION SOCKET LOCATION

CONFIGURATION PLUG (RAYTHEON P/N 594113-11)



OPTION PIN ASSIGNMENTS — FORMAT SELECTION

Config. Plug Pin No.	DISPLAY FORMATS						
	40X12	40X24	64X15	64X16	64X30	80X12	80X24
4	Cut	Cut	Cut	In	Cut	Cut	Cut
11	Cut	In	Cut	Cut	In	Cut	In
12	Cut	Cut	In	In	In	In	In
17	In	In	Cut	Cut	Cut	In	In

DISPLAY ADAPTER "C"

P/N 860629

8K AND 16K MEMORIES

DISPLAY ADAPTER "C" HAS A PROVISION FOR THREE AUXILIARY MODULES TO USE IBM COAX CABLE. TWO RECEIVER BOARDS AND ONE COAX CONTROL LOGIC BOARD.

CHARACTER/LINE FORMAT AND MEMORY REFRESH TIMING PATCH PLUGS

For These Displays Char/Lines No. of Lines Formats	Insert These Patches (5921553-)	INTO BOARD LOCATIONS				
		E10	J16	C2 (Norm)	C2 (Opt)	C3 16K / 8K
80 X 24		G1	G3	G134 OR G136	G133 OR G135	
64 X 30		C1	G3	G134 OR G136	G133 OR G135	
80 X 12		G1	G4	G134 OR G136	G133 OR G135	
64 X 15 OR 16		G2	G4	G134 OR G136	G133 OR G135	
40 X 12		C-	G5	G134 OR G136	G133 OR G135	
40 X 24		G1	G48	G134 OR G136	G133 OR G135	

E10 — NUMBER OF CHARACTERS PER LINE

J16 — NUMBER OF LINES PER FORMAT

C2 — MEMORY REFRESH
G134 = 2 MS (NORMAL TIMING)
G136 = 1 MS (OPTION TIMING)

C3 — TYPE OF MEMORY MODULE
G135 = 8K MEMORY MODULE
G133 = 16K MEMORY MODULE

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER (TTY (WRITE TO) CASSETTE (WRITE TO), ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (READ FROM) IS ASSIGNED TO PORT 1 OF FIRST MULTIPLEX CHANNEL CONTROLLER

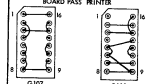
MODEM (WRITE TO) IS ASSIGNED TO PORT 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS.

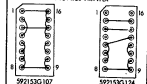
*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MI5-A PATCHES

BOARD PASS PRINTER



MS-BOARD LOCATION - B2
CENTRONICS PRINTER

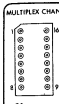


MS - BOARD LOCATION - B2

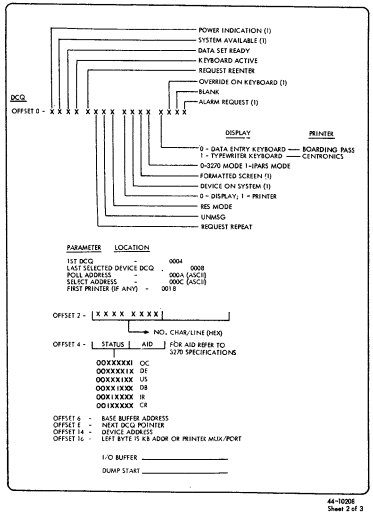
NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH



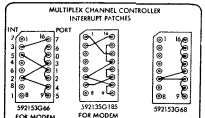
FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9



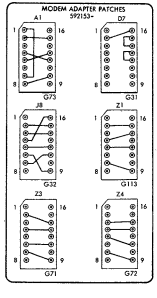
DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEMS			
SEND	0	2	5 OR 8
REC	0	1	5 OR 8
PRINTERS 1-4	0	3-6	2
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



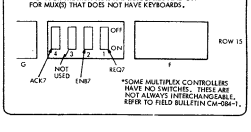
MODEM ADAPTER PATCHES



MULTIPLEX CHANNEL CONTROLLER

DISABLE/ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

Processing Unit and Terminal Address Assignments

Encode on Feature Board / Control Unit or Device Number	Column 1 Use this column to find: • Device Selection, • Specific Poll, • General Poll, and • Fixed Return Addresses — ASCII HEX	Column 2 Use this column to find: • PTS Selection Addresses — ASCII Hex
0	20	54
1	21	55
2	22	56
3	23	57
4	24	58
5	25	59
6	26	5A
7	27	5B
8	28	5C
9	29	5D
10	2A	5E
11	2B	5F
12	2C	60
13	2D	61
14	2E	62
15	2F	63
16	30	64
17	31	65
18	32	66
19	33	67
20	34	68
21	35	69
22	36	6A
23	37	6B
24	38	6C
25	39	6D
26	3A	6E
27	3B	6F
28	3C	70
29	3D	71
30	3E	72
31	3F	73
32	40	74
33	41	75
34	42	76
35	43	77
36	44	78
37	45	79
38	46	7A
39	47	7B
	48	7B

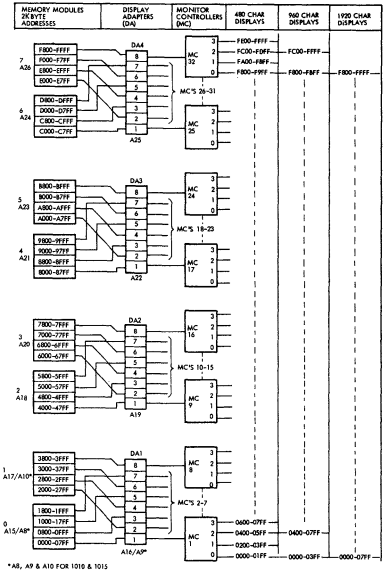
NOTE

I/O character address 7B is used on the device address to specify a General Poll operation.

44-10206
Sheet 2 of 3
JUNE 1978

PATCH AND SWITCH SETTINGS AND SOFTWARE NOTES FOR DOWNLINE 3271 REMOTE EMULATOR FOR RAYCARGO

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



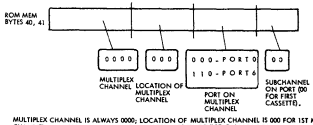
NOTES

ALL DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. IN A MIXED SYSTEM 1920 CH DISPLAYS ARE ASSIGNED BEFORE 480 CH DISPLAYS. ALSO THE STARTING MEMORY ADDRESSES ARE DETERMINED BY WHICH DISPLAY ADAPTERS ARE ASSIGNED TO 1920 CH AND 480 CH DISPLAYS (SEE C4 CH F, B, %). IF A SYSTEM IS MIXED OR DOES NOT FULLY LOAD ALL M.C.'s, PRINTER BUFFERS WILL BE ASSIGNED TO THE UNUSED AREAS. IN A MIXED ** SYSTEM PRINTERS ARE ASSIGNED AS FOLLOWS:

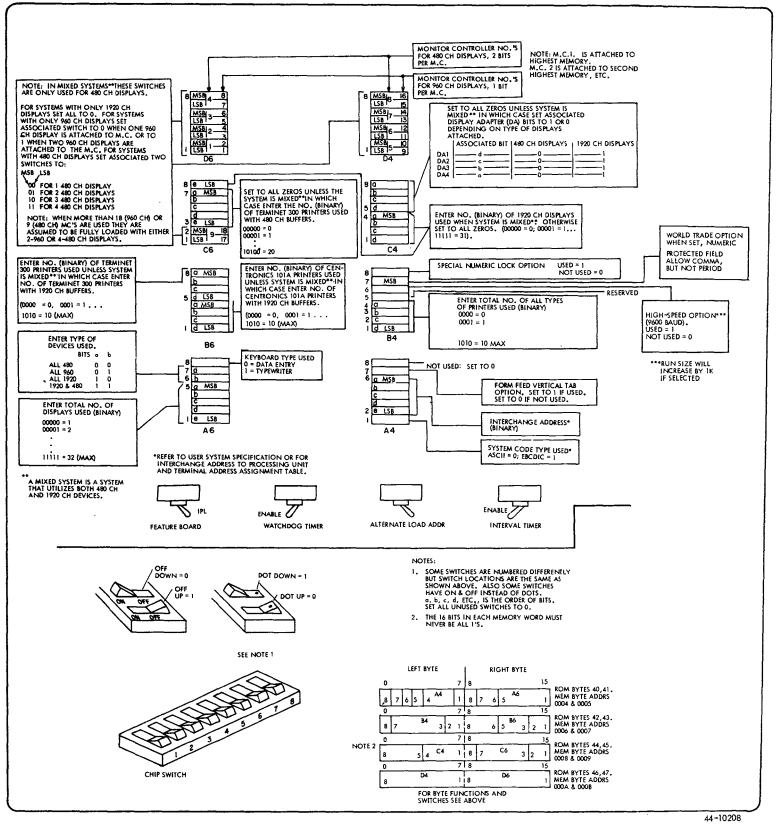
1 CENTRONICS - 1920 CH BUFFER
2 TERMINET - 1920 CH BUFFER
3 CENTRONICS - 480 CH BUFFER
4 TERMINET - 480 CH BUFFER

THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULES A17/A10* AND A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

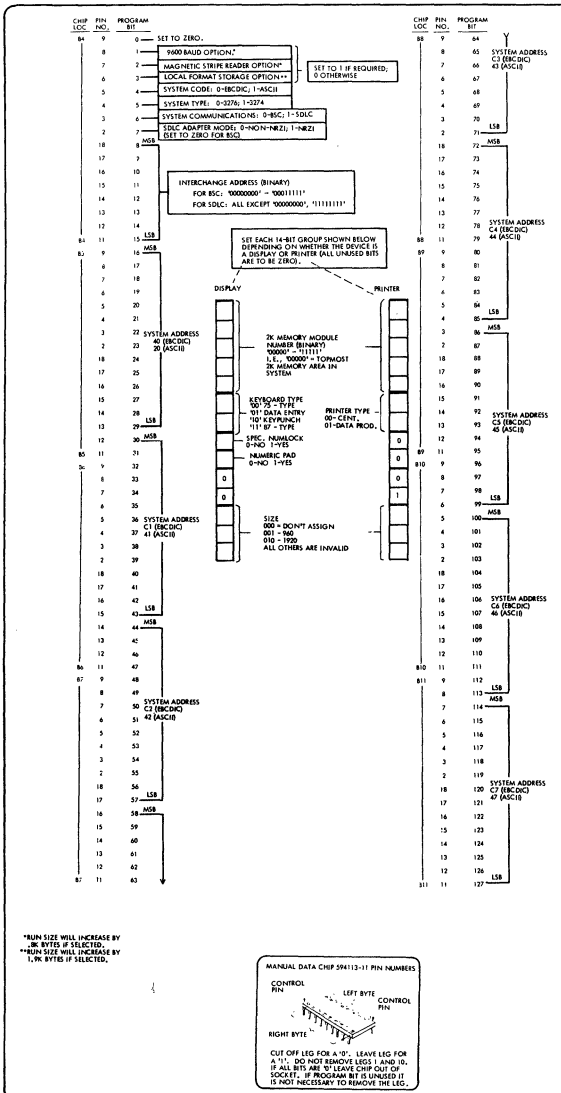
DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS 0000; LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).



PTS-100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR 3274/3276 REMOTE EMULATOR



THE INTERACTIVE CONFIGURATOR MAY BE USED TO CONFIGURE BOTH 3274'S AND 3276'S. THE FEATURE BOARD CAN ONLY CONFIGURE A 3276 AND A 3274 WITH LESS THAN 8 DEVICES AND DOES NOT PERMIT AS MANY SYSTEM OPTIONS AS THE INTERACTIVE CONFIGURATOR (SEE SHEET 4 FOR DIRECTIONS ON ENTERING THE INTERACTIVE CONFIGURATOR).

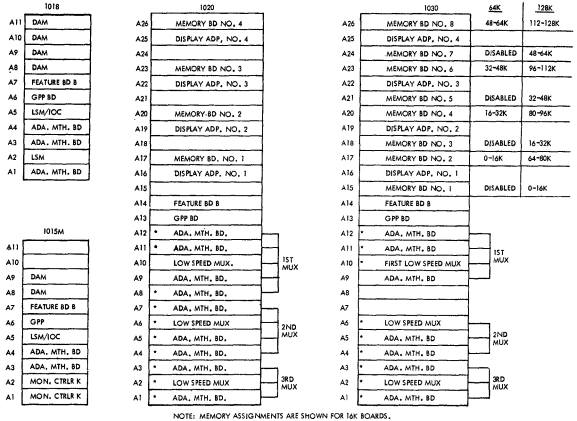
*RUN SIZE WILL INCREASE BY .5K BYTES IF SELECTED.
**RUN SIZE WILL INCREASE BY 1.9K BYTES IF SELECTED.

Processing Unit and Terminal Address Assignments

Encode on Feature Board	Column 1 Use this column to find: • Device Selection, • Specific Poll, • General Poll, and • Fixed Return Addresses		Column 2 Use this column to find: • PTS Selection Addresses	
Processing Unit or Device Number	EBCDIC Hex	ASCII Hex	EBCDIC Hex	ASCII Hex
0	40	20	60	2D
1	C1	41	61	2F
2	C2	42	E2	53
3	C3	43	E3	54
4	C4	44	E4	55
5	C5	45	E5	56
6	C6	46	E6	57
7	C7	47	E7	58
8	C8	48	E8	59
9	C9	49	E9	5A
10	4A	58	6A	5C
11	4B	7E	6B	2C
12	4C	3C	6C	25
13	4D	28	6D	5F
14	4E	2B	6E	3E
15	4F	21	6F	3F
16	50	26	F0	30
17	D1	4A	F1	31
18	D2	4B	F2	32
19	D3	4C	F3	33
20	D4	4D	F4	34
21	D5	4E	F5	35
22	D6	4F	F6	36
23	D7	50	F7	37
24	D8	51	F8	38
25	D9	52	F9	39
26	5A	5D	7A	3A
27	5B	24	7B	23
28	5C	2A	7C	40
29	5D	29	7D	27
30	5E	3B	7E	3D
31	5F	5E	7F	22

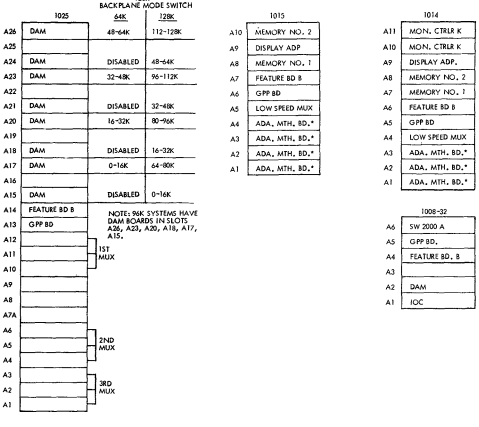
NOTE
I/O character address 7F is used as the device address to specify a General Poll operation.

PTS-100 PROCESSING UNIT BOARD LOCATIONS

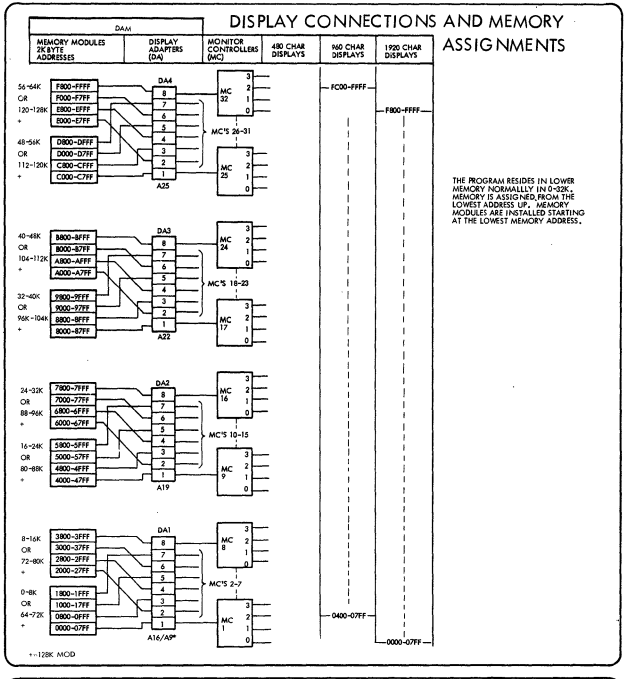


NOTE: MEMORY ASSIGNMENTS ARE SHOWN FOR 16K BOARDS.

*SLOT CAN ALSO ACCOMMODATE OTHER OPTION BOARDS.

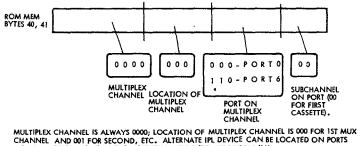


DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



THE PROGRAM RESIDES IN LOWER MEMORY NORMALLY IN 0-32K. MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

DEVICE ADDRESS ASSIGNMENTS



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MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

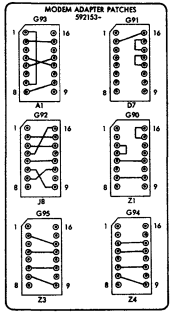
MODEM (READ FROM) IS ASSIGNED TO PORT 1 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (WRITE TO) IS ASSIGNED TO PORT 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS.

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MODEM ADAPTER PATCHES 592153-



SAM I

LOGIC OPTION SWITCHES (ON=CLOSED, OFF=OPEN)

S1	ON	ON	OFF	OFF					
	1	2	3	4					
S2	OFF	ON	OFF	ON	ON	ON	OFF	ON	
	1	2	3	4	5	6	7	8	
S3	ON=BLOCK OFF=UNDERLINE		OFF	OFF	ON=960 OFF=1920	ON	OFF	ON	ON=CX OFF=TP
	1		2	3	4	5	6	7	8

NOTE: USE CHARACTER GENERATOR PROMS 7639?/003 IN IC7 76441/001 IN IC6.

CX=COAX CABLE (HALF-DUPLEX)

TP=TWISTED PAIR CABLE (FULL-DUPLEX)

LINKS

D=E, F=G, K=L

A=B IF COAX; B=C IF TWISTED PAIR

H=J IF NO SECURITY KEYLOCK

CAUTION!!!

THE DAM I REQUIRES DIFFERENT VOLTAGES THAN THE PRESENT 16K MEMORIES. THEREFORE, IF A PROCESSOR HAS DAM I'S, ONLY DAM I BOARDS CAN BE USED IN THAT SYSTEM. CONVERSELY, IF A PROCESSOR DOES NOT HAVE DAM I'S, DO NOT PLUG ANY DAM I BOARDS IN THAT SYSTEM.

DAM I D11 - DISPLAY FORMATS

SWITCH					
FORMAT	1	2	3	4	8
80 X 24	ON	OFF	ON	ON	-
80 X 12	OFF	OFF	ON	ON	-
COAX MODE	-	-	-	-	*

*TWISTED PAIR: OFF FOR ALL DAM'S

COAX: ON FOR ALL DAM'S EXCEPT FOR ONE WITH COAX, THEN OFF. USE COAX MODULE 932155.

SWITCH SETTINGS G11

ON	S1 PARITY INT. DISABLE
ON	S2 480 NS MEMORY CYCLE
ON	S3 16K MEMORY SIZE
ON	S4 16K MEMORY SIZE

DISPLAY ADAPTER "C"

P/N 860629

8K AND 16K MEMORIES

DISPLAY ADAPTER "C" HAS A PROVISION FOR THREE AUXILIARY MODULES TO USE IBM COAX CABLE: TWO RECEIVER BOARDS AND ONE COAX CONTROL LOGIC BOARD.

CHARACTER/LINE FORMAT AND MEMORY REFRESH TIMING PATCH PLUGS

For These Displays Char/Lines No. of Lines Formats	Insert These Patches (592153-)	INTO BOARD LOCATIONS					
		E10	J16	C2 (Norm)	C2 (Opt)	C3 16K	C3 8K
80 X 24		G1	G3	G134 OR G136		G133 OR G135	
80 X 12		G1	G4	G134 OR G136		G133 OR G135	

E10 – NUMBER OF CHARACTERS PER LINE

J16 – NUMBER OF LINES PER FORMAT

C2 – MEMORY REFRESH
G134 - 2 MS (NORMAL TIMING)
G136 - 1 MS (OPTION TIMING)

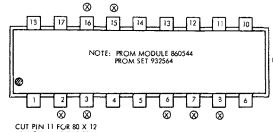
C3 – TYPE OF MEMORY MODULE
G135 - 8K MEMORY MODULE
G133 - 16K MEMORY MODULE

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEMS SEND	0	2	5 or 8
REC	0	1	5 or 8

NOTE: Use Prom Module No. 860544
Use Character Proms 932564

MONITOR CONTROLLER K (P/N 860963)

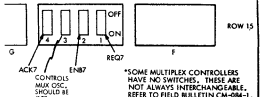


CUT PIN 11 FOR 80 X 12
LEAVE AS-LINE FOR 80 X 24

MULTIPLEX CHANNEL CONTROLLER

DISABLE/ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



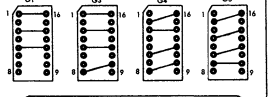
CONTROLS MUX OSC. SHOULD BE OFF

*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

KEYBOARD PATCH
10——02
ENABLES 87 KEYS
CUT FOR 75 KEYS

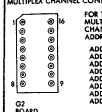
DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS 592153-



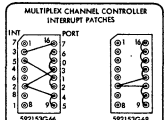
FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-)	INTO BOARD LOCATIONS D15 AND J16	
80 X 24		G1	G3
80 X 12		G1	G4

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH



FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



NOTE: G185 MAY BE SUBSTITUTED FOR G66.

FIRST MULTIPLEX CHANNEL CONTROLLER

2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

OPTION SELECTION

	GROUND DO NOT CUT	1	18	CUT FOR BOX TYPE CURSOR DON'T CUT FOR UNDERLINE CURSOR } CURSOR
TONE	CUT TO ACTIVATE TONE ON SET & RESET TRANS. DON'T CUT TO ACTIVATE TONE ON SET TRANS.	2	17	CUT FOR 64X16&30 DISPLAY FORMATS DON'T CUT FOR 40&80X12&24 DISPLAY FORMATS } DISPLAY FORMAT
	CUT FOR 1 SEC TONE DON'T CUT FOR NO 1 SEC TONE	3	16	CUT FOR DISPLAY POWER ON LED OPTION DON'T CUT WHEN OPTION IS NOT USED } POWER ON LED OPTION
CHARACTER GENERATOR	CUT FOR ROM OR 4K PROM DON'T CUT FOR ROM OR PROM MODULES	4	15	CUT FOR CURSOR REGISTER OPTION DON'T CUT FOR NORMAL CURSOR MODE
LOW INTENSITY CURSOR	CUT FOR LOW INTENSITY CURSOR (MC-9 TYPE) DON'T CUT FOR ALL OTHER CURSORS	5	14	CUT FOR MSB= DON'T CARE ATTRIBUTE CONTROL-NORMAL MODE DON'T CUT FOR MSB= 1 ATTRIBUTE CONTROL } ATTRIBUTE MSB CONTROL
DATA FIELD	CUT FOR A BLANK DATA FIELD DON'T CUT FOR A BLINKING DATA FIELD	6	13	CUT TO DISPLAY 32/64 CHAR TYPES ON 8 SCAN LINES DON'T CUT TO DISPLAY ALL CHARS ON 9 SCAN LINES
	CUT FOR PROGRAM CONTROLLED OTHERWISE, DON'T CUT	7	12	CUT FOR 40X12&24 DISPLAY FORMATS DON'T CUT FOR 64X15&30 AND 80X12&24 DISPLAY FORMATS } DISPLAY FORMAT
	CUT FOR NORMAL= LOW INTENSITY DATA FIELD DON'T CUT FOR NORMAL= HIGH INTENSITY FIELD	8	11	CUT FOR 40X12, 64X15 AND 80X12 DISPLAY FORMATS DON'T CUT FOR 40X24, 64X30 OR 80X24 FORMATS
NUMBER OF CHARACTERS DISPLAYED	CUT TO USE 96 DISPLAYABLE CHARS DON'T CUT TO USE 128 DISPLAYABLE CHARS	9	10	GROUND DO NOT CUT

SWITCHES: CABLE TYPE (NEAR X1, X14)
TWISTED PAIR - ALL OFF
COAX - ALL ON

CHARACTER GENERATOR (NEAR E17, F17)
1 - ON 3 - ON
2 - OFF 4 - ON

FOR COAX: USE TX MODULE 860954

SYSTEM CONFIGURATION

The system may be configured in three ways:

1. Feature board (up to 8 devices)
2. Interactive configurator (set alternate load switch, remove patch plug or 84 for up to 32 devices
3. Configuration information written on the tape by previous use of Method 2

Refer to PFI 933892 for further details.

DCQ DEFINITION

DISPLACEMENT (HEX)	DISPLAYS	PRINTER
0	LED byte, Misc. byte	Same
2	Cursor register	Same
4	KB misc. word	WCC, LRC
6	Status byte, Aid byte	Same
8	Buffer address	Same
A	Buffer pointer	Same
C	No. char/line, no. lines	Same
E	Attribute address	Same
10	Next DCQ address	Same
12	MAGSTP LRC	WCC byte address
14	MAGSTP flag, MAGSTP byte count	Printer class word
16	ASCII device address	Same
18	KB address, KB shift byte	KB address, --
1A	LED byte address	Same
1C	Local print printer's DCQ	Local print display's DCQ
1E	Cursor register address	Same
20	Saved cursor address	Same
22	Word 1 of last line	Timer cell
24	Word 2 of last line	Ptr status, PTR misc. bytes
26	Word 3 of last line	--
28	Last byte of last line, Ptr ident byte	--
2A	Print matrix word 1	--
2C	Print matrix word 2	--

NOTE: DCQ's reside in low core on GT 64K systems (all except for bytes 0, 2, 3 (all devices), and 4, 5 (printers only); and immediately following the device buffers on LE 64K systems.

LOW CORE CONSTANTS AND VARIABLES

DISPLACEMENT (HEX)	DEFINITION
0	DIN
2	HALT
4	First DCQ address
6	Current DCQ address
8	Last selected DCQ address
A	Control unit polling address (ASCII)
C	Control unit selection address (ASCII)
E	First printer (if any) or first display DCQ address
10	Dummy DCQ address
12	PSVC's next searched display DCQ address
14	X'0000'
16	X'0001'
18	X'0011'
1A	X'0007'
1C	X'0080'
1E	X'FFFF'
20	0:LE.64K; 1:GT .64K
22	0:3276; X'8000':3274
24	Run size of emulator
26	COMREG's address
28	Start of local format library
2A	End of local format library
2C	Next available space in local format library
2E	LOFRMT KB retrieval flag
30	LOFRMT downline load flag
32	LOFRMT filing status flag
34	LOFRMT format not found flag

Breakdown of several DCQ bytes.

Offset 0- LED BITS BYTE
- BIT 0 - POWER ON INDICATION
- 1 - SYSTEM AVAILABLE
- 2 - INPUT INHIBIT
- 3 - INSERT MODE
- 4 - ALARM
- 5 - DATA SET READY
- 6 - TRANSMIT / RECEIVE
- 7 - IDENT MODE

Offset 1- MISC. BITS BYTE
- BIT 8 - 0-DISPLAY 1-PRINTER
- 9 - DEVICE ON SYSTEM; 0-NO, 1-YES
- A - FORMATTED SCREEN; 0-NO, 1-YES
- B -
- C - LOCAL PRINT IN PROGRESS; 0-NO, 1-YES
- D, E - PRINTER DCQ ONLY
  - 10-SYSTEM
  - 01-LOCAL
  - 11-SHARED
- F - ALARM REQUEST

Offset 4- KEYBOARD MISC. WORD(DISPLAY DCQS ONLY)
- BIT 0 -
- 1 -
- 2 - REQ. IDENT STATUS LINE; 0-NO, 1-YES
- 3 - REQUEST FOR LOCAL PRINT; 0-NO, 1-YES
- 4 - REQ. FOR IDENT OPERATION; 0-NO, 1-YES
- 5 - REQ. DISPLAY OF IDENT NO; 0-NO, 1-YES
- 6 - REQ. FOR MATRIX LOAD; 0-NO, 1-YES
- 7 - DEVICE NO.0 AT INIT.; 0-NO, 1-YES

- 8 - STATUS LINE ON DISP 0-NO, 1-YES
- 9 - 1-ONLY DEVICE CANCEL IS OPERABLE
- A - K/B HAS NUMERIC PAD; 0-NO, 1-YES
- B - NO. OF K/B KEYS; 0-75, 1-87
- C
- D
- E - K/B SHIFT; 0-OFF, 1-ON
- F - ALTERNATE MODE; 0-OFF, 1-ON

Offset 4- WRITE CONTROL CHARACTER (PRINTER DCQ ONLY)
- BIT 0
- 1 - 0:REMOTE PRINT, 1:LOCAL PRINT
- 2,3 - 00 - NL, EM, CR DEFINE PRT LINE LEN
  - 01 - 40 CHAR PRT LINE LENGTH
  - 10 - 64 CHAR PRT LINE LENGTH
  - 11 - 80 CHAR PRT LINE LENGTH
- 4 - START PRINT BIT WHEN 1
- 5 - SOUND ALARM BIT WHEN 1
- 6 - KEYBOARD RESTORE BIT WHEN 1
- 7 - RESET MDT BIT WHEN 1

Offset 6- DEVICE STATUS BYTE
- BIT 0 - WAITING FOR PRINTER TO ANSWER
- 1 - DATA CHECK
- 2 - COMMAND REJECT
- 3 - INTERVENTION REQUIRED
- 4 - DEVICE BUSY
- 5 - UNIT SPECIFY
- 6 - DEVICE END
- 7 - OPERATION CHECK

Offset 19- KEYBOARD SHIFT BYTE
- BIT 8,9 - K/B TYPE
  - 11 - TYPEWRITER
  - 10 - DATA ENTRY
  - 01 - KEYPUNCH
- A - CASE: 0-U/L CASE, 1-UPPERCASE ONLY
- B - NUMERIC LOCK OPTION; 0-NO, 1-YES
- C - LEFT SHIFT; 0-OFF, 1-ON
- D - ALPHA (DE, KP ONLY); 0-OFF, 1-ON
- E - RIGHT SHIFT; 0-OFF, 1-ON
- F - SHIFT LOCK; 0-OFF, 1-ON

ATTRIBUTE STRUCTURE ------
- BIT 0 - 1=ATTRIBUTE CHARACTER
- 1 - IF PSVC, THERE WAS AN ATT. ON LAST LINE WHEN ONE; IF CSVC, THIS IS A NEW ATTRIBUTE TO PROCESS
- 2 - SELECTOR PEN DETECTABLE; 0-NO, 1-YES
- 3 - 0-NORMAL; 1-HIGH INTENSITY OR BLANK <SEE BIT 7>
- 4 - 0-UNPROTECTED; 1-PROTECTED SCREEN
- 5 - MDT 0-UNMODIFIED, 1-MODIFIED
- 6 - 0-ALPHANUMERIC, 1-NUMERIC
- 7 - 0:HIGH INTENSITY; 1:BLANK/BLINK IF BIT 3 ON <MUST BE 1 IF BIT 3 OFF>

3274/76 COMMUNICATIONS REGION (POINTED TO BY LOCATION 26)

	DISPLACEMENT (HEX)	DEFINITION	
Addresses	0	CSVC run time address	
	2	CPRO run time address	
	4	GBSBTB run time address	
	6	KSVC run time address	
	8	PSVC run time address	(if present)
	A	MAGSTP run time address	(if present)
	C	LOFRMT run time address	(if present)
	E	PSVC load time address	
	10	MAGSTP load time address	
	12	LOFRMT load time address	
	14	TRANT B load time address	
	16	COMBUF load time address	
	18	ISVC load time address	
	1A	IACONF load time address	
	1C	START load time address	
	1E	Table of run time KB translate table addresses	
	20	Pointer to I/O comm buffer at run time.	
	22	Pointer to dummy comm buffer at run time	
	24	First plar address	
	26	Keyboard IOCQ address	
	28	Keyboard tumble table address	
	2A	EBCDIC to ASCII translate table address	
	2C	ASCII to EBCDIC translate table address	
	2E	First comm IOCQ address	
	30	Configuration table address	
Error counters	32	KB char hardware errors	
	34	Tumble table address errors	
	36	KB entry errors	
	38	Printer starts	
	3A	Printer errors - bad LRC	
	3C	Printer errors - bad status	
	3E	Messages sent	
	40	NAK's sent	
	42	ENQ's sent	
	44	WACK's sent	
	46	RVI's sent	
	48	Messages received	
	4A	RVI's received	
	4C	NAK's received	
	4E	ENQ's received	
	50	WACK's received	
	52	Messages with bad CRC	
	54	Carrier lost count	
	56	Input overrun count	
	58	Reject command count	
	5A	Wrong ACK count	

CASSETTE PROGRAM PATCH PROCEDURE

1. IPL OLD CASSETTE.
2. DURING IPL STORE X'8XXX' INTO LOCATION 0 (WHERE XXX = DEVICE ADDRESS OF TARGET DRIVE).
3. WHEN IPL IS COMPLETE LOCATION 0 WILL CONTAIN X'0100'. IF NOT RETRY.
4. ENTER PATCHES. DO NOT PRESS STOP OR RESET.
5. PUT A NEW CASSETTE IN TARGET DRIVE.
6. STORE X'8XXX' INTO LOCATION 0 AS ABOVE. LOCATION 0 WILL CHANGE TO X'0300' TO INDICATE THAT THE DUMP IS IN PROGRESS.
7. THE TAPE WILL REWIND AND STOP WHEN COMPLETE AND LOCATION 0 WILL CONTAIN X'0100'. IF MORE COPIES ARE DESIRED RETURN TO STEP 5.
8. IF AN ERROR OCCURS, THE TAPE WILL TRY TO REWRITE CONTINUOUSLY. TO START OVER INSERT A NEW CASSETTE AND STORE X'8XXX' INTO LOCATION 0.

NOTE: FOR ADDITIONAL INFORMATION REFER TO FIB NO. PS-0018.

PRINTER CONTROLLER

LED VALUE DEFINITIONS

- 0 = RUN MODE
- 1 = RUN/MONO MODE
- 2 = TEST MODE
- 3 = PRINTER OFFLINE
- 4 = PRINTER BUSY
- 5 = OUT OF PAPER (CENTRONICS)
- 6 = PARITY ERROR (DP 8-300)
- 7 = LRC ERROR (PTS - PRINTER CONTROLLER TRANSMISSION)
- 8 = INTERVENTION REQUIRED
- 9 = KEYBOARD LOAD INTERRUPT MISSING
- A = MEMORY ERRORS DETECTED
- B = PRINTER INTERRUPT ERROR
- C = CANCEL PRINT DEPRESSED
- D = BUFFER REPRINT BEING PROCESSED
- E = FUNCTION KEY CODE ERROR
- F = N/A

STATUS PIA -

DDRA/PA	X'7000'
DDRB/PB	X'2001'
CRA	X'7002'
CRB	X'7003'

PRINTER PIA -

		STACK	X'20' → X'00'
DDRA/PA	X'5400'	PA BUFFER	X'4000'
DDRB/PB	X'5401'		
CRA	X'5402'		
CRB	X'5403'		

THUMBWHEEL SWITCHES -

X'5003'

8-BIT SWITCH X'5000'

PRINTER CONTROLLER OPTION SWITCH - B2

1	2	3	4	5	6	7	8
ON-TWISTED PAIR OFF-COAX	ON (1 OR 2K BUFFER)	X	X	X	X	X	X

X = DON'T CARE

PRINTER INTERFACE MODULE OPTION SWITCH - C4 ON ASSY 932371 IN J2

1	2	3	4	5	6	7	8
X	ON=DATA PRODUCT OFF=CENTRONIC	OFF (80 CHAR)	ON	X	X	X	ON=960 OFF=1920

THUMBWHEEL SWITCHES -

USED TO SET THE DECIMAL NUMBER OF LINES PER PAGE (A SETTING OF 00 INDICATES THE DEFAULT VALUE OF 66 LINES PER PAGE)

ROTARY SWITCH -

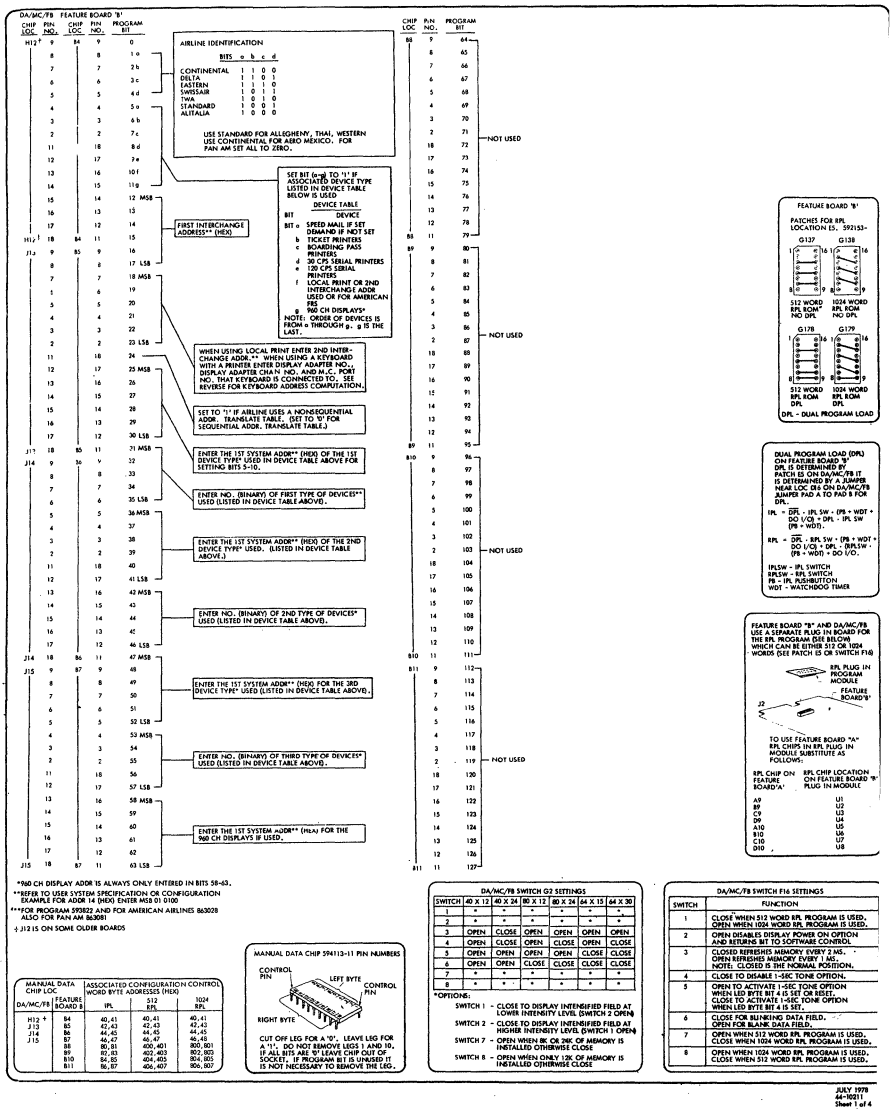
'TEST' - RUNS RAM AND PRINTER DIAGNOSTICS UNTIL THE SWITCH IS MOVED TO THE 'RUN' OR 'RUN/MONO' POSITIONS

'RUN' - ONLINE; PRINTER WILL PRINT UPPER AND LOWER CASE CHARACTERS

'RUN/MONO' - ONLINE; PRINTER WILL PRINT UPPER CASE ONLY.

USE PROMS: 932636 - 1A, 2A, 3A, 4A

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR EASTERN SPEED MAIL/DEMAND 593822-20



MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA/MC/FB	FEATURE BOARD B	IPL	512 RPL	1024 RPL
H12 †	B4	40,41	40,41	40,41
J13	B5	42,43	42,43	42,43
J14	B6	44,45	44,45	44,45
J15	B7	46,47	46,47	46,46
	B8	80,81	800,401	800,801
	B9	82,83	402,403	802,803
	B10	84,85	404,405	804,805
	B11	86,87	406,407	806,807

DA/MC/FB SWITCH G2 SETTINGS

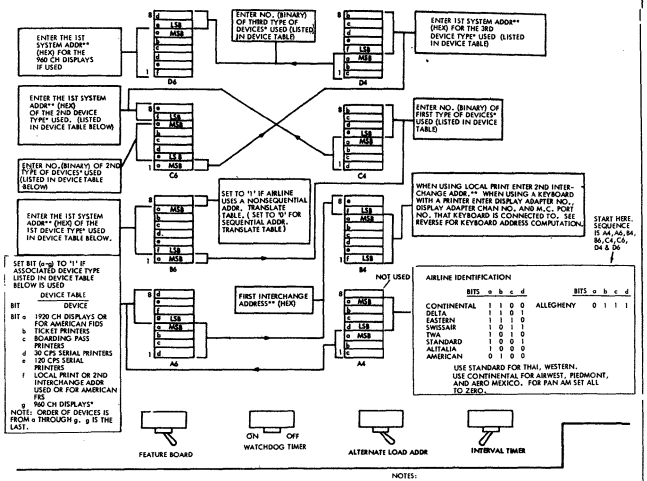
SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	CLOSE	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 28K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

PTS 100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR PARS/IPARS EMULATOR USING THE INITIALIZATION PROGRAM ***



DISPLAY DATA MEMORY BUFFER ASSIGNMENTS

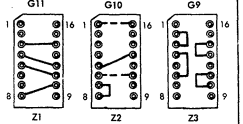
Display Adapter	Channel	Monitor	1920 Char/Display 64 Ch X 30 Lines 960 Char/Display 64 Ch X 15 Lines	Buffer Area	Status Address	960 Char/Display 64 Ch X 15 Lines	Buffer Area	Status Address	480 Char/Display 40 Ch X 12 Lines	Buffer Area	Status Address
a	0	0		8000-83FF	A0		8000-83FF	C0		8000-83FF	E0
	1	1		8400-87FF	A1		8400-87FF	C1		8400-87FF	E1
	2	2		8800-8BFF	A2		8800-8BFF	C2		8800-8BFF	E2
	3	3		8C00-8FFF	A3		8C00-8FFF	C3		8C00-8FFF	E3
	4	4		9000-93FF	A4		9000-93FF	C4		9000-93FF	E4
	5	5		9400-97FF	A5		9400-97FF	C5		9400-97FF	E5
	6	6		9800-9BFF	A6		9800-9BFF	C6		9800-9BFF	E6
	7	7		9C00-9FFF	A7		9C00-9FFF	C7		9C00-9FFF	E7
b	0	8		A000-A3FF	A8		A000-A3FF	C8		A000-A3FF	E8
	1	9		A400-A7FF	A9		A400-A7FF	C9		A400-A7FF	E9
	2	10		A800-ABFF	AA		A800-ABFF	CA		A800-ABFF	EA
	3	11		AC00-AFFF	AB		AC00-AFFF	CB		AC00-AFFF	EB
	4	12		B000-B3FF	AC		B000-B3FF	CC		B000-B3FF	EC
	5	13		B400-B7FF	AD		B400-B7FF	CD		B400-B7FF	ED
	6	14		B800-BBFF	AE		B800-BBFF	CE		B800-BBFF	EE
	7	15		BC00-BFFF	AF		BC00-BFFF	CF		BC00-BFFF	EF
c	0	16		C000-C3FF	B0		C000-C3FF	D0		C000-C3FF	F0
	1	17		C400-C7FF	B1		C400-C7FF	D1		C400-C7FF	F1
	2	18		C800-CBFF	B2		C800-CBFF	D2		C800-CBFF	F2
	3	19		CC00-CFFF	B3		CC00-CFFF	D3		CC00-CFFF	F3
	4	20		D000-D3FF	B4		D000-D3FF	D4		D000-D3FF	F4
	5	21		D400-D7FF	B5		D400-D7FF	D5		D400-D7FF	F5
	6	22		D800-DBFF	B6		D800-DBFF	D6		D800-DBFF	F6
	7	23		DC00-DFFF	B7		DC00-DFFF	D7		DC00-DFFF	F7
d	0	24		E000-E3FF	B8		E000-E3FF	D8		E000-E3FF	F8
	1	25		E400-E7FF	B9		E400-E7FF	D9		E400-E7FF	F9
	2	26		E800-EBFF	BA		E800-EBFF	DA		E800-EBFF	FA
	3	27		EC00-EFFF	BB		EC00-EFFF	DB		EC00-EFFF	FB
	4	28		F000-F3FF	BC		F000-F3FF	DC		F000-F3FF	FC
	5	29		F400-F7FF	BD		F400-F7FF	DD		F400-F7FF	FD
	6	30		F800-FBFF	BE		F800-FBFF	DE		F800-FBFF	FE
	7	31		FC00-FFFF	BF		FC00-FFFF	DF		FC00-FFFF	FF

SERIAL ADAPTER PATCHING

PATCH PLUGS 592153-

FULL DUPLEX - TTY

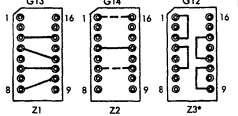
INSERT THESE PATCH PLUGS INTO LOCATIONS Z1, Z2 & Z3 ON THE SERIAL ADAPTER 591558-



HALF DUPLEX - TTY & SERIAL PRINTER

PATCH PLUGS 592153-

INSERT THESE PATCH PLUGS INTO LOCATIONS Z1, Z2 & Z3 ON THE SERIAL ADAPTER 591558-

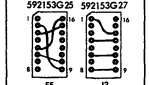


---- INSTALLED BUT NOT USED.

*300 BAUD

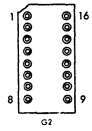
IPARS MODEM ADAPTER PATCHES

INSERT THESE PATCH PLUGS INTO BOARD LOCATIONS E5 AND J3



MULTIPLEX CHANNEL CONTROLLER KEYBOARD, INTERRUPT AND ADDRESS PATCHES

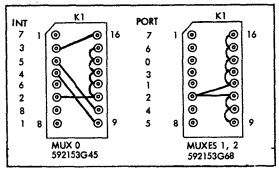
MUX ADDRESS PATCH



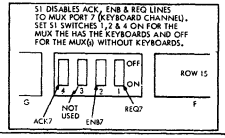
*ADDRESS OF MUX CHAN.

1 OR 4 TO 16 - ADDR 000
1 OR 4 TO 12 - ADDR 001
1 OR 4 TO 14 - ADDR 010
1 OR 4 TO 10 - ADDR 011
1 OR 4 TO 15 - ADDR 100
1 OR 4 TO 11 - ADDR 101
1 OR 4 TO 13 - ADDR 110
1 OR 4 TO 9 - ADDR 111

INTERRUPT PATCHES



S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1,2 & 4 ON FOR THE MUX THE HAS THE KEYBOARDS AND OFF FOR THE MUX(I) WITHOUT KEYBOARDS.



WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

MOTHERBOARD SCREW SWITCH SETTINGS

MONITOR CONTROLLER* CHARACTER/LINE FORMAT E6 SWITCH SETTINGS**

E6 CHIP SWITCH SETTING	64 CHAR. 15 LINES	64 CHAR. 16 LINES	64 CHAR. 30 LINES
E6-1	OPEN	OPEN	OPEN
E6-2	OPEN	CLOSED	OPEN
E6-3	OPEN	OPEN	CLOSED
E6-4	CLOSED	CLOSED	CLOSED
E6-5	OPEN	OPEN	OPEN
E6-6	OPEN	OPEN	OPEN
E6-7	CLOSED	CLOSED	CLOSED
E6-8+	OPEN	CLOSED	OPEN

*8 MODIFIED BOARD,

**CLOSED = 1; OPEN = 0. SEE FEATURE BOARD SWITCH SETTING PROCEDURE

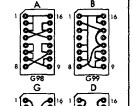
+ USED ON SOME M.C.'S (USED ON ALL 16 LINE M.C.'S)

IPARS SYSTEM CONFIGURATION VARIABLE PATCHES, SWITCHES AND REMOTE PRINTER ADDRESSES

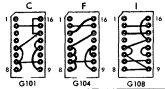
MULTI-INTERFACE SERIAL ADAPTER (MISA) PATCHING (592153-)

INSERT THESE FOR THIS MODEL MISA 593296-	PLUGS INTO B1	PLUGS INTO B2
G1 TERMINET 300 BAUD	A	C
G3 TERMINET 1200 BAUD	B	C
G5 TTY 110 BAUD	G	F
G7 TTY 50 BAUD	D	F
G9 TTY 75 BAUD	E	F
G11 TICKET & BOARDING PASS PRINTER	H	I

M5 PATCH CONFIGURATIONS (BAUD RATES)



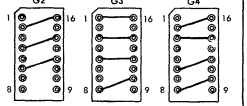
B2 PATCH CONFIGURATIONS (CONTROL)



DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

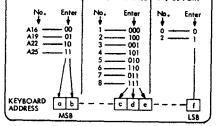
FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (592153-) D15	J16
64 X 30 SPLIT SCREEN	G2	G3
64 X 15 OR 16	G2	G4

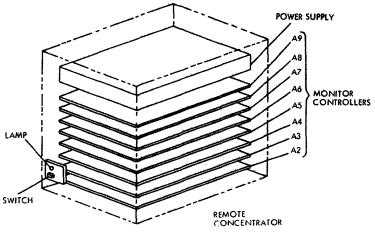
PATCH PLUG CONFIGURATIONS 592153-



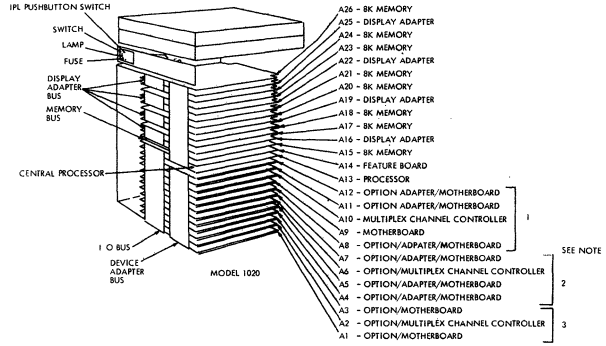
KEYBOARD ADDRESS COMPUTATION

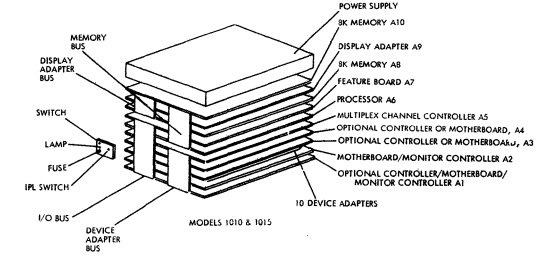
KEYBOARD CONNECTED:





POWER SUPPLIES





NOTE:
MONITOR CONTROLLERS ARE INSTALLED IN SLOTS A1, A2, A3 & A4 WHEN ONLY 2 MULTIPLEX CONTROLLERS ARE USED. MONITOR CONTROLLERS ARE INSTALLED IN A7, A8 & A9 WHEN 3 MULTIPLEX CONTROLLERS ARE USED.

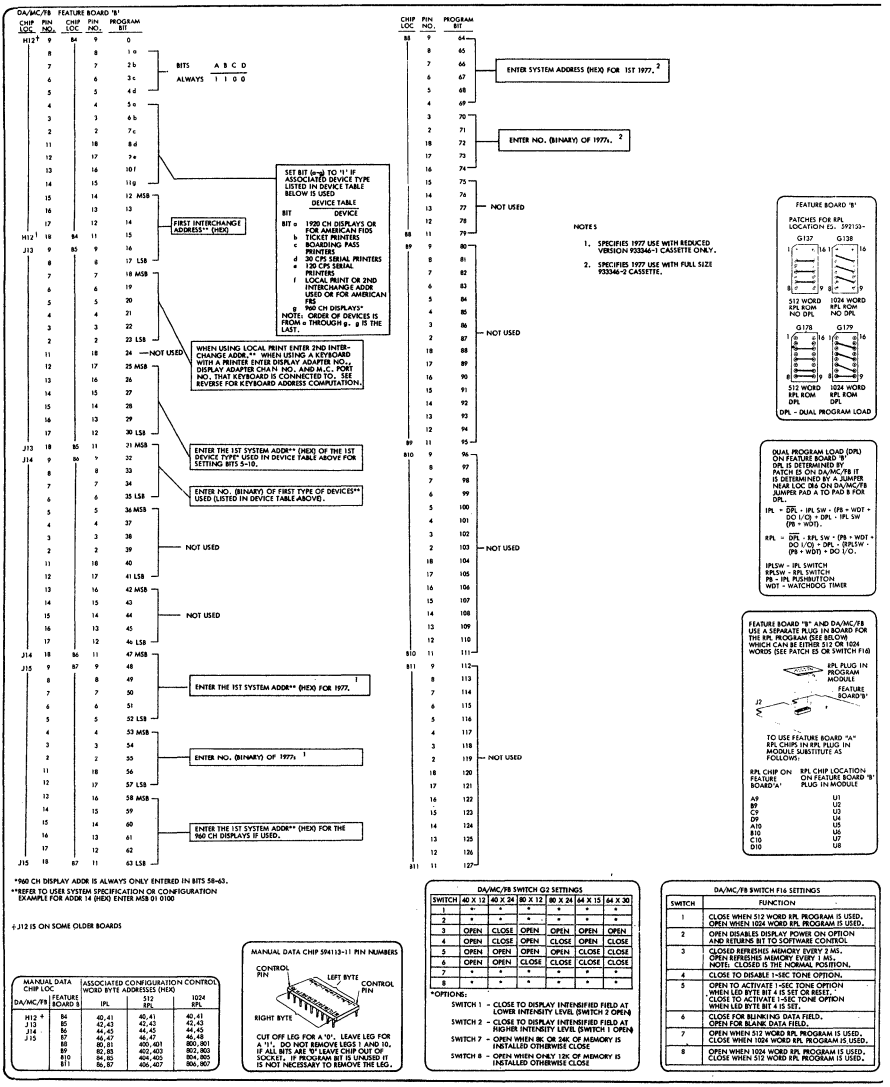
COMMUNICATIONS REGION TABLE

LOAD SIZE OF PROGRAM
KEYBOARD MODULE
SECOND HALF OF INITIALIZER
TASK SUPERVISOR
PRINTER INITIALIZER
SERIAL PRINTER ROUTINE
TICKET & BOARDING PASS PRINTERS INITIALIZER
PRINTER STATUS TABLES
DISPLAY STATUS TABLES
NUMBER OF DISPLAYS
NUMBER OF PRINTERS
CCC COUNTER
NUMBER OF MESSAGES RECEIVED
NUMBER OF MESSAGES TRANSMITTED
EOMC'S IN TKT AND BOARDING PASS MESSAGES
DATA LOST COUNTER
CARRIER LOST COUNTER
IOCQ'S FOR DISPLAYS
IOCQ'S FOR PRINTERS
OUTPUT - TO HOST - BUFFER
VALID TERMINAL ADDRESSES
VALID PRINTER ADDRESSES
AIRLINE ID
INTERCHANGE 1
INTERCHANGE 2
LOCATION 0010 CONTAINS THE ADDRESS OF THIS TABLE

LED MEMORY BUFFER ASSIGNMENTS

Adaptor	Channel	1920 Character Display	960 Character Display		480 Character Display			
			Mon. 0	Mon. 1	Mon. 0	Mon. 1	Mon. 2	Mon. 3
1	1	07B0	03C0	07C0	01E0	03E0	05E0	07E0
	2	27B0	23C0	27C0	21E0	23E0	25E0	27E0
	3	0FB0	0BC0	0FC0	09E0	0BE0	0DE0	0FE0
	4	2FB0	2BC0	2FC0	29E0	2BE0	2DE0	2FE0
	5	17B0	13C0	17C0	11E0	13E0	15E0	17E0
	6	37B0	33C0	37C0	31E0	33E0	35E0	37E0
	7	1FB0	1BC0	1FC0	19D0	1BE0	1DE0	1FE0
	8	3FB0	3BC0	3FC0	39E0	3BE0	3DE0	3FE0
2	1	47B0	43C0	47C0	41E0	43E0	45E0	47E0
	2	67B0	63C0	67C0	61E0	63E0	65E0	67E0
	3	4FB0	43C0	4FC0	49E0	4BE0	4DE0	4FE0
	4	6FB0	6BC0	6FC0	69E0	6BE0	6DE0	6FE0
	5	57B0	53C0	57C0	51E0	53E0	55E0	57E0
	6	77B0	73C0	77C0	71E0	73E0	75E0	77E0
	7	5FB0	5BC0	5FC0	59E0	5BE0	5DE0	5FE0
	8	7FB0	7BC0	7FC0	79E0	7BE0	7DE0	7FE0
3	1	87B0	83C0	87C0	81E0	83E0	85E0	87E0
	2	A7B0	A3C0	A7C0	A1E0	A3E0	A5E0	A7E0
	3	8FB0	8BC0	8FC0	89E0	8BE0	8DE0	8FE0
	4	AFB0	ABC0	AFC0	A9E0	ABE0	ADE0	AFE0
	5	97B0	93C0	97C0	91E0	93E0	95E0	97E0
	6	B7B0	B3C0	B7C0	B1E0	B3E0	B5E0	B7E0
	7	9FB0	9BC0	9FC0	99E0	9BE0	9DE0	9FE0
	8	BFB0	BBC0	BFC0	B9E0	BBE0	BDC0	BFE0
4	1	C7B0	C3C0	C7C0	C1E0	C3E0	C5E0	C7E0
	2	E7B0	E3C0	E7C0	E1E0	E3E0	E5E0	E7E0
	3	CFB0	CBC0	CFC0	C9E0	CBE0	CDE0	CFE0
	4	EFB0	EBC0	EFC0	E9E0	EBE0	EDE0	EFE0
	5	D7B0	D3C0	D7C0	D1E0	D3E0	D5E0	D7E0
	6	F7B0	F3C0	F7C0	F1E0	F3E0	F5E0	F7E0
	7	DFB0	DBC0	D7C0	D9E0	DBE0	DDE0	DFE0
	8	FFB0	FBC0	FFC0	F9E0	FBE0	FDE0	FFE0

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR FRONTIER PARS/IPARS EMULATOR USING 1977 DEVICES (FOR USE WITH CASSETTES 933346-1 AND -2)



MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)			
DA/MC/FB	FEATURE BOARD 'B'	IPL	512 RPL	1024 RPL
H12 †	B4	40,41	40,41	40,41
J13	B5	42,43	42,43	42,43
J14	B6	44,45	44,45	44,45
J15	B7	46,47	46,47	46,48
	B8	B0, B1	400,401	800, 801
	B9	B2, B3	402,403	802, 803
	B10	B4, B5	404,405	804, 805
	B11	B6, B7	406,407	806, 807

DA/MC/FB SWITCH G2 SETTINGS

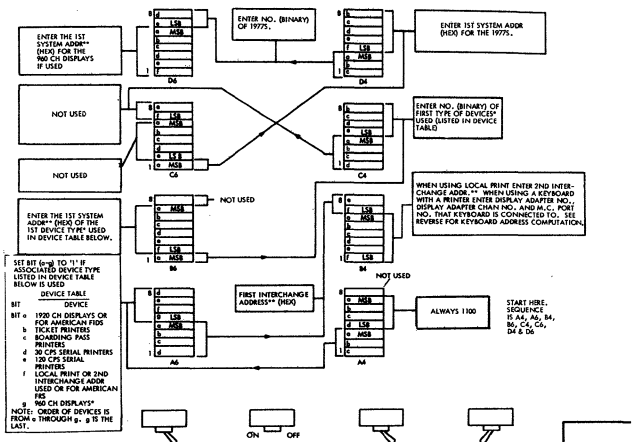
SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

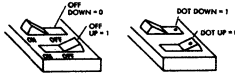
*OPTIONS -
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

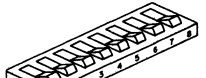
SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED, OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS., OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT #15 SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT #15 SET.
6	CLOSE FOR BLINKING DATA FIELD, OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED, CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED, CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

PTS 100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR PARS/IPARS EMULATOR USING THE INITIALIZATION PROGRAM ***





SEE NOTE 1



CHIP SWITCH

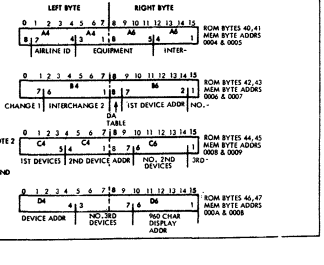
NOTES:

1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1's.

*960 CH DISPLAY ADDR IS ALWAYS ONLY ENTERED IN SWITCH D6 1-6.

**REFER TO USER SYSTEM SPECIFICATION OR CONFIGURATION EXAMPLE FOR ADDR 14 (HEX) ENTER 01 0100
ab cde f

* * * FOR 593822 AND FOR AMERICAN AIRLINES 863028. ALSO FOR PAN AM 863081.



DISPLAY DATA MEMORY BUFFER ASSIGNMENTS

Display Adapter	Channel	Monitor	192 CH/1 DISPLAY 64 CH X 3 LINES Display Buffer Address (Hex)	384 CH/2 DISPLAYS 64 CH X 6 LINES Display Buffer Address (Hex)	960 CH/1 DISPLAY 64 CH X 15 LINES Display Buffer Address (Hex)	480 CH/1 DISPLAY 80 CH X 6 LINES Display Buffer Address (Hex)	1920 CH/1 DISPLAY 64 CH X 30 LINES Display Buffer Address (Hex)	960 CH/1 DISPLAY 80 CH X 12 LINES Display Buffer Address (Hex)	3840 CH/2 DISPLAYS 80 CH X 24 LINES Display Buffer Address (Hex)	Display Adapter
A	0	0	8000-803F	8000-807F	8000-81DF	8000-82FF	8000-87BF	8000-85DF	8000-8BBF	A
		1	8040-807F	8080-80FF	8200-83DF	8300-84FF	8800-8BBF	8600-89DF	9000-93BF	
	1	0	8080-80BF	8100-813F	8400-85DF	8500-86FF	8C00-8FBF	8800-8DDF	9400-9DBF	
		1	80C0-80FF	8180-81FF	8600-87DF	8700-88FF	9000-93BF	8A00-91DF	9800-A7BF	
	2	0	8100-813F	8200-823F	8800-89DF	8900-8AFF	9400-9BBF	8C00-95DF	9C00-B1BF	
		1	8140-817F	8280-82FF	8A00-8BDF	8B00-8CFF	9800-A3BF	8E00-99DF	A000-BBBF	
	3	0	8180-81BF	8300-833F	8C00-8DDF	8D00-8EFF	9C00-ABBF	9000-9DDF	A400-C5BF	
		1	81C0-81FF	8380-83FF	8E00-8FDF	8F00-90FF	A000-B3BF	9200-A1DF	A800-CFBF	
	4	0	8200-823F	8400-843F	9000-91DF	9100-92FF	A400-ABBF	9400-A5DF	AC00-D9BF	
		1	8240-827F	8480-84FF	9200-93DF	9300-94FF	A800-C3BF	9600-A9DF	B000-E3BF	
	5	0	8280-82BF	8500-853F	9400-95DF	9500-96FF	AC00-DBBF	9800-ADDF	B400-EDBF	
		1	82C0-82FF	8580-85FF	9600-97DF	9700-98FF	B000-F3BF	9A00-B1DF	B800-F7BF	
	6	0	8300-833F	8600-863F	9800-99DF	9900-9AFF	B400-BBBF	9C00-B5DF	BC00-FFBF	
		1	8340-837F	8680-86FF	9A00-9BDF	9B00-9CFF	B800-C3BF	9E00-B9DF	C000-07BF	
	7	0	8380-83BF	8700-873F	9C00-9DDF	9D00-9EFF	BC00-CBBF	A000-BDDF	C400-0FBF	
		1	83C0-83FF	8780-87FF	9E00-9FDF	9F00-A0FF	C000-D3BF	A200-C1DF	C800-17BF	
	8	0	8400-843F	8800-883F	A000-A1DF	A100-A2FF	C400-DBBF	A400-C5DF	CC00-1FBF	
		1	8440-847F	8880-88FF	A200-A3DF	A300-A4FF	C800-E3BF	A600-C9DF	D000-27BF	
	9	0	8480-84BF	8900-893F	A400-A5DF	A500-A6FF	CC00-EBBF	A800-CDDF	D400-2FBF	
		1	84C0-84FF	8980-89FF	A600-A7DF	A700-A8FF	D000-F3BF	AA00-D1DF	D800-37BF	
	A	0	8500-853F	8A00-8A3F	A800-A9DF	A900-AAFF	D400-FBBF	AC00-D5DF	DC00-3FBF	
		1	8540-857F	8A80-8AFF	AA00-ABDF	AB00-ACFF	D800-03BF	AE00-D9DF	E000-47BF	
	B	0	8580-85BF	8B00-8B3F	AC00-ADDF	AD00-AEFF	DC00-0BBF	B000-DDDF	E400-4FBF	
		1	85C0-85FF	8B80-8BFF	AE00-AFDF	AF00-B0FF	E000-13BF	B200-E1DF	E800-57BF	
	C	0	8600-863F	8C00-8C3F	B000-B1DF	B100-B2FF	E400-1BBF	B400-E5DF	EC00-5FBF	
		1	8640-867F	8C80-8CFF	B200-B3DF	B300-B4FF	E800-23BF	B600-E9DF	F000-67BF	
	D	0	8680-86BF	8D00-8D3F	B400-B5DF	B500-B6FF	EC00-2BBF	B800-EDDF	F400-6FBF	
		1	86C0-86FF	8D80-8DFF	B600-B7DF	B700-B8FF	F000-33BF	BA00-F1DF	F800-77BF	
	E	0	8700-873F	8E00-8E3F	B800-B9DF	B900-BAFF	F400-3BBF	BC00-F5DF	FC00-7FBF	
		1	8740-877F	8E80-8EFF	BA00-BBDF	BB00-BCFF	F800-43BF	BE00-F9DF		
	F	0	8780-87BF	8F00-8F3F	BC00-BDDF	BD00-BEFF	FC00-4BBF	C000-FDDF		
		1	87C0-87FF	8F80-8FFF	BE00-BFDF	BF00-C0FF				

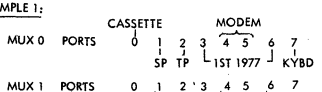
Display Adapter	Channel	Monitor	192 CH/1 DISPLAY 64 CH X 3 LINES Display Buffer Address (Hex)	384 CH/2 DISPLAYS 64 CH X 6 LINES Display Buffer Address (Hex)	960 CH/1 DISPLAY 64 CH X 15 LINES Display Buffer Address (Hex)	480 CH/1 DISPLAY 80 CH X 6 LINES Display Buffer Address (Hex)	1920 CH/1 DISPLAY 64 CH X 30 LINES Display Buffer Address (Hex)	960 CH/1 DISPLAY 80 CH X 12 LINES Display Buffer Address (Hex)	3840 CH/2 DISPLAYS 80 CH X 24 LINES Display Buffer Address (Hex)	Display Adapter
B	0	0	8800-883F	9000-903F	8000-81DF	8000-82FF	8000-87BF	8000-85DF	8000-8BBF	B
		1	8840-887F	9080-90FF	8200-83DF	8300-84FF	8800-8BBF	8600-89DF	9000-93BF	
	1	0	8880-88BF	9100-913F	8400-85DF	8500-86FF	8C00-8FBF	8800-8DDF	9400-9DBF	
		1	88C0-88FF	9180-91FF	8600-87DF	8700-88FF	9000-93BF	8A00-91DF	9800-A7BF	
	2	0	8900-893F	9200-923F	8800-89DF	8900-8AFF	9400-9BBF	8C00-95DF	9C00-B1BF	
		1	8940-897F	9280-92FF	8A00-8BDF	8B00-8CFF	9800-A3BF	8E00-99DF	A000-BBBF	
	3	0	8980-89BF	9300-933F	8C00-8DDF	8D00-8EFF	9C00-ABBF	9000-9DDF	A400-C5BF	
		1	89C0-89FF	9380-93FF	8E00-8FDF	8F00-90FF	A000-B3BF	9200-A1DF	A800-CFBF	
	4	0	8A00-8A3F	9400-943F	9000-91DF	9100-92FF	A400-ABBF	9400-A5DF	AC00-D9BF	
		1	8A40-8A7F	9480-94FF	9200-93DF	9300-94FF	A800-C3BF	9600-A9DF	B000-E3BF	
	5	0	8A80-8ABF	9500-953F	9400-95DF	9500-96FF	AC00-DBBF	9800-ADDF	B400-EDBF	
		1	8AC0-8AFF	9580-95FF	9600-97DF	9700-98FF	B000-F3BF	9A00-B1DF	B800-F7BF	
	6	0	8B00-8B3F	9600-963F	9800-99DF	9900-9AFF	B400-BBBF	9C00-B5DF	BC00-FFBF	
		1	8B40-8B7F	9680-96FF	9A00-9BDF	9B00-9CFF	B800-C3BF	9E00-B9DF	C000-07BF	
	7	0	8B80-8BBF	9700-973F	9C00-9DDF	9D00-9EFF	BC00-CBBF	A000-BDDF	C400-0FBF	
		1	8BC0-8BFF	9780-97FF	9E00-9FDF	9F00-A0FF	C000-D3BF	A200-C1DF	C800-17BF	
	8	0	8C00-8C3F	9800-983F	A000-A1DF	A100-A2FF	C400-DBBF	A400-C5DF	CC00-1FBF	
		1	8C40-8C7F	9880-98FF	A200-A3DF	A300-A4FF	C800-E3BF	A600-C9DF	D000-27BF	
	9	0	8C80-8CBF	9900-993F	A400-A5DF	A500-A6FF	CC00-EBBF	A800-CDDF	D400-2FBF	
		1	8CC0-8CFF	9980-99FF	A600-A7DF	A700-A8FF	D000-F3BF	AA00-D1DF	D800-37BF	
	A	0	8D00-8D3F	9A00-9A3F	A800-A9DF	A900-AAFF	D400-FBBF	AC00-D5DF	DC00-3FBF	
		1	8D40-8D7F	9A80-9AFF	AA00-ABDF	AB00-ACFF	D800-03BF	AE00-D9DF	E000-47BF	
	B	0	8D80-8DBF	9B00-9B3F	AC00-ADDF	AD00-AEFF	DC00-0BBF	B000-DDDF	E400-4FBF	
		1	8DC0-8DFF	9B80-9BFF	AE00-AFDF	AF00-B0FF	E000-13BF	B200-E1DF	E800-57BF	
	C	0	8E00-8E3F	9C00-9C3F	B000-B1DF	B100-B2FF	E400-1BBF	B400-E5DF	EC00-5FBF	
		1	8E40-8E7F	9C80-9CFF	B200-B3DF	B300-B4FF	E800-23BF	B600-E9DF	F000-67BF	
	D	0	8E80-8EBF	9D00-9D3F	B400-B5DF	B500-B6FF	EC00-2BBF	B800-EDDF	F400-6FBF	
		1	8EC0-8EFF	9D80-9DFF	B600-B7DF	B700-B8FF	F000-33BF	BA00-F1DF	F800-77BF	
	E	0	8F00-8F3F	9E00-9E3F	B800-B9DF	B900-BAFF	F400-3BBF	BC00-F5DF	FC00-7FBF	
		1	8F40-8F7F	9E80-9EFF	BA00-BBDF	BB00-BCFF	F800-43BF	BE00-F9DF		
	F	0	8F80-8FBF	9F00-9F3F	BC00-BDDF	BD00-BEFF	FC00-4BBF	C000-FDDF		
		1	8FC0-8FFF	9F80-9FFF	BE00-BFDF	BF00-C0FF				

DEVICE ADDRESS & INTERRUPT ASSIGNMENTS

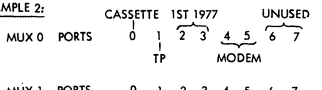
DEVICE	MUX	MUX PORT	INT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEM ADAPTERS			
2331 PARS RX	0	4	5
PARS TX	0	5	4
PRINTERS	0 1 2	1-3,6 0-7 0-7	
1977	0 1 2	SEE NOTE BELOW (PRINTER ASSIGNED FIRST)	

NOTE: THE 1977 REQUIRES AN AMA MODEM ADAPTER THAT IS CONNECTED TO 2 PORTS ON THE SAME MUX, STARTING WITH THE LOWEST NUMBERED PORT AVAILABLE SEE EXAMPLES BELOW.

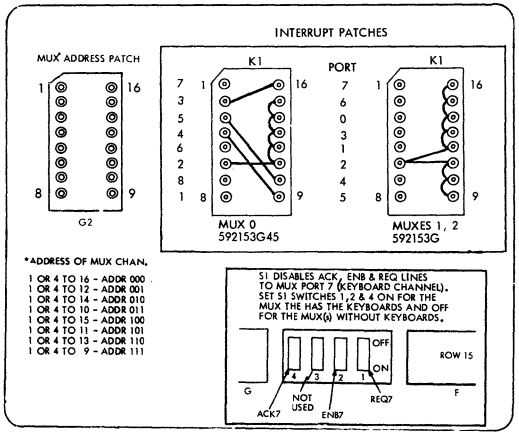
EXAMPLE 1:



EXAMPLE 2:



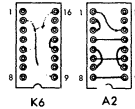
MULTIPLEX CHANNEL CONTROLLER KEYBOARD, INTERRUPT AND ADDRESS PATCHES



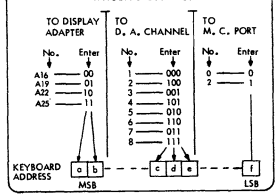
IPARS MODEM ADAPTER PATCHES

INSERT THESE PATCH PLUGS INTO BOARD LOCATIONS K6 AND A2

592153G170 592153G147



KEYBOARD ADDRESS COMPUTATION



PTS/1977 PATCHES

INSERT PATCHES (592153-) INTO THE LOCATIONS SHOWN

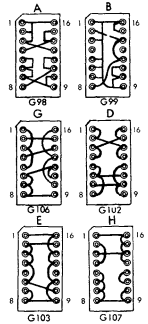
G223-M7
G222-M2
G65-L2
G225-G4
G226-F8
G227-E8

IPARS SYSTEM CONFIGURATION VARIABLE PATCHES, SWITCHES AND REMOTE PRINTER ADDRESSES

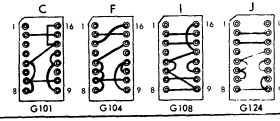
MULTI-INTERFACE SERIAL ADAPTER (MISA) PATCHING (592153-)

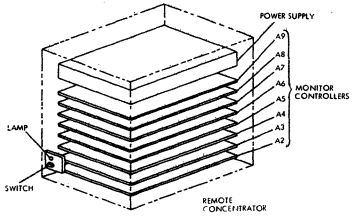
INSERT THESE PATCHES FOR THIS MODEL MISA 593296-	M5	B2
G1 TERMINET 300 BAUD	A	C
G3 TERMINET 1200 BAUD	B	C
G5 TTY 110 BAUD	G	F
G7 TTY 50 BAUD	D	F
G9 TTY 75 BAUD	E	F
G11 TICKET & BOARDING PASS PRINTER	H	I
CENTRONICS	H	J
TERMINET 30	A	J

M5 PATCH CONFIGURATIONS (BAUD RATES)

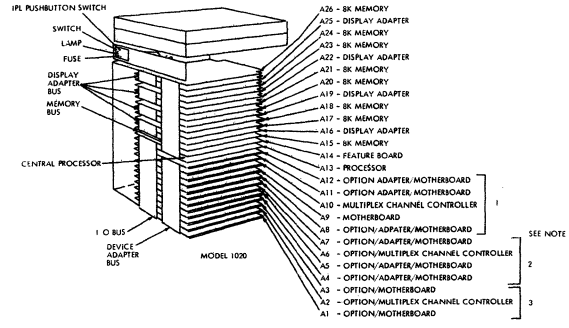


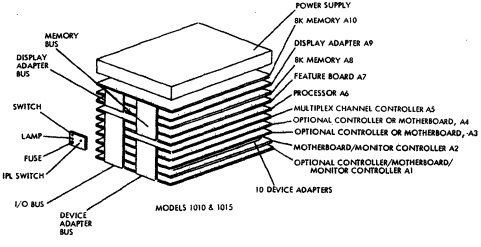
B2 PATCH CONFIGURATIONS (CONTROL)





POWER SUPPLIES





NOTE:
MONITOR CONTROLLERS ARE INSTALLED IN SLOTS A1, A2, A3 & A4 WHEN ONLY 2 MULTIPLEX CONTROLLERS ARE USED. MONITOR CONTROLLERS ARE INSTALLED IN A7, A8 & A9 WHEN 3 MULTIPLEX CONTROLLERS ARE USED.

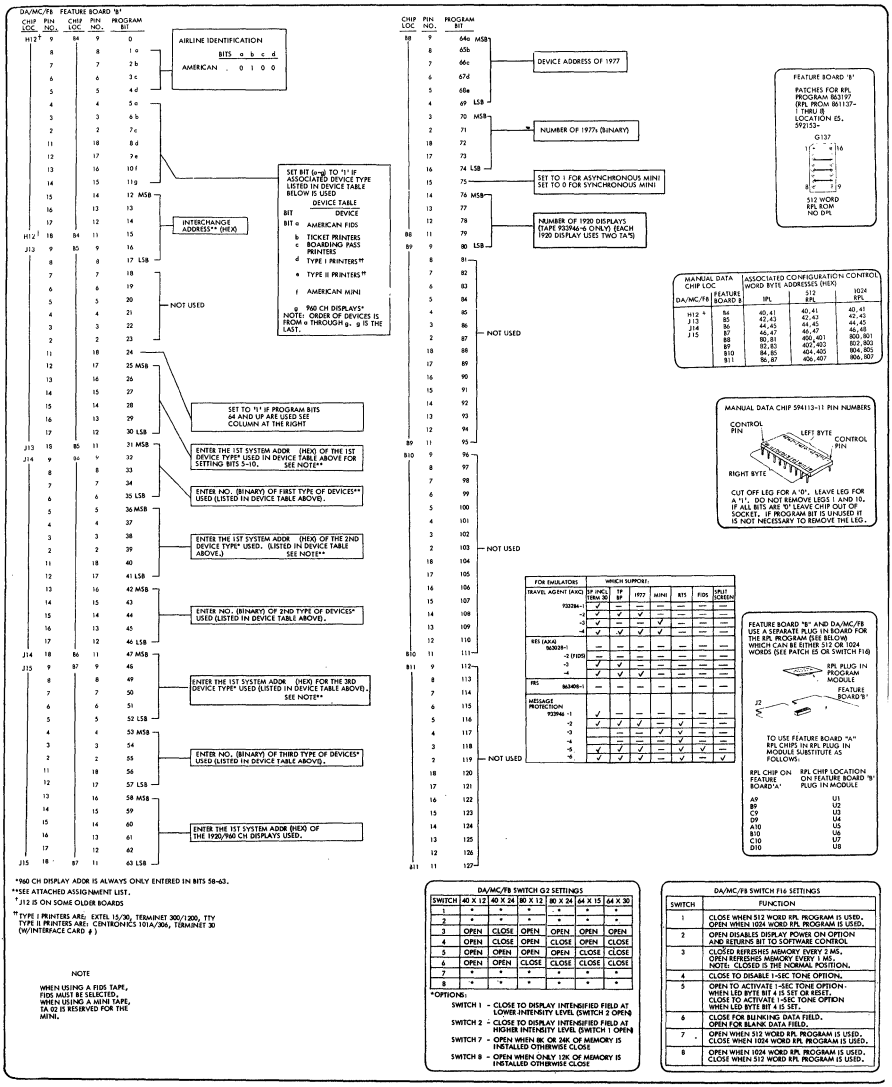
COMMUNICATIONS REGION TABLE

LOAD SIZE OF PROGRAM
KEYBOARD MODULE
SECOND HALF OF INITIALIZER
TASK SUPERVISOR
PRINTER INITIALIZER
SERIAL PRINTER ROUTINE
TICKET & BOARDING PASS PRINTERS INITIALIZER
PRINTER STATUS TABLES
DISPLAY STATUS TABLES
NUMBER OF DISPLAYS
NUMBER OF PRINTERS
CCC COUNTER
NUMBER OF MESSAGES RECEIVED
NUMBER OF MESSAGES TRANSMITTED
EOMC'S IN TKT AND BOARDING PASS MESSAGES
DATA LOST COUNTER
CARRIER LOST COUNTER
IOCQ'S FOR DISPLAYS
IOCQ'S FOR PRINTERS
OUTPUT - TO HOST - BUFFER
VALID TERMINAL ADDRESSES
VALID PRINTER ADDRESSES
AIRLINE ID
INTERCHANGE 1
INTERCHANGE 2
LOCATION 0010 CONTAINS THE ADDRESS OF THIS TABLE

LED MEMORY BUFFER ASSIGNMENTS

Adaptor	Channel	1920 Character Display	960 Character Display		480 Character Display			
			Mon. 0	Mon. 1	Mon. 0	Mon. 1	Mon. 2	Mon. 3
1	1	07B0	03C0	07C0	01E0	03E0	05E0	07E0
	2	27B0	23C0	27C0	21E0	23E0	25E0	27E0
	3	0FB0	0BC0	0FC0	09E0	0BE0	0DE0	0FE0
	4	2FB0	2BC0	2FC0	29E0	2BE0	2DE0	2FE0
	5	17B0	13C0	17C0	11E0	13E0	15E0	17E0
	6	37B0	33C0	37C0	31E0	33E0	35E0	37E0
	7	1FB0	1BC0	1FC0	19D0	1BE0	1DE0	1FE0
	8	3FB0	3BC0	3FC0	39E0	3BE0	3DE0	3FE0
2	1	47B0	43C0	47C0	41E0	43E0	45E0	47E0
	2	67B0	63C0	67C0	61E0	63E0	65E0	67E0
	3	4FB0	43C0	4FC0	49E0	4BE0	4DE0	4FE0
	4	6FB0	6BC0	6FC0	69E0	6BE0	6DE0	6FE0
	5	57B0	53C0	57C0	51E0	53E0	55E0	57E0
	6	77B0	73C0	77C0	71E0	73E0	75E0	77E0
	7	5FB0	5BC0	5FC0	59E0	5BE0	5DE0	5FE0
	8	7FB0	7BC0	7FC0	79E0	7BE0	7DE0	7FE0
3	1	87B0	83C0	87C0	81E0	83E0	85E0	87E0
	2	A7B0	A3C0	A7C0	A1E0	A3E0	A5E0	A7E0
	3	8FB0	8BC0	8FC0	89E0	8BE0	8DE0	8FE0
	4	AFB0	ABC0	AFC0	A9E0	ABE0	ADE0	AFE0
	5	97B0	93C0	97C0	91E0	93E0	95E0	97E0
	6	B7B0	B3C0	B7C0	B1E0	B3E0	B5E0	B7E0
	7	9FB0	9BC0	9FC0	99E0	9BE0	9DE0	9FE0
	8	BFB0	BBC0	BFC0	B9E0	BBE0	BDE0	BFE0
4	1	C7B0	C3C0	C7C0	C1E0	C3E0	C5E0	C7E0
	2	E7B0	E3C0	E7C0	E1E0	E3E0	E5E0	E7E0
	3	CFB0	CBC0	CFC0	C9E0	CBE0	CDE0	CFE0
	4	EFB0	EBC0	EFC0	E9E0	EBE0	EDE0	EFE0
	5	D7B0	D3C0	D7C0	D1E0	D3E0	D5E0	D7E0
	6	F7B0	F3C0	F7C0	F1E0	F3E0	F5E0	F7E0
	7	DFB0	DBC0	D7C0	D9E0	DBE0	DDE0	DFE0
	8	FFB0	FBC0	FFC0	F9E0	FBE0	FDE0	FFE0

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR AMERICAN EMULATORS



*960 CH DISPLAY ADDR IS ALWAYS ONLY ENTERED IN BITS 58-63.

**SEE ATTACHED ASSIGNMENT LIST.

†J12 IS ON SOME OLDER BOARDS

††TYPE I PRINTERS ARE: EXTEL 15/30, TERMINET 300/1200, TTY TYPE II PRINTERS ARE: CENTRONICS 101A/306, TERMINET 30 (W/INTERFACE CARD #)

NOTE

WHEN USING A FIDS TAPE, FIDS MUST BE SELECTED. WHEN USING A MINI TAPE, TA 02 IS RESERVED FOR THE MINI.

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:

SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)

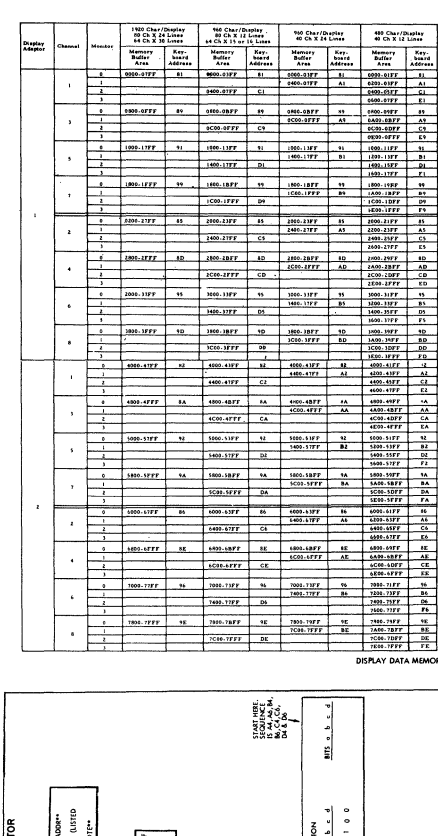
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)

SWITCH 7 - OPEN WHEN 8K OR 24K OF MEMORY IS INSTALLED OTHERWISE CLOSE

SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY POWER ON OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION. WHEN LED BYTE BIT 4 IS SET OR RESET. CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.



Display Adaptor	Channel	Monitor	1920 Char/Display 80 Ch X 24 Lines 64 Ch X 30 Lines		960 Char/Display 80 Ch X 12 Lines - 64 Ch X 15 or 16 Lines		960 Char/Display 40 Ch X 24 Lines		480 Char/Display 40 Ch X 12 Lines	
			Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address
1	1	0	0000-07FF	B1	8000-83FF	E1	0000-03FF	A1	0000-01FF	F1
		1					0400-07FF	A1	0200-03FF	A1
		2			8400-87FF	C1			0400-05FF	C1
		3							0600-07FF	E1
	3	0	0800-0FFF	B9	0800-08FF	99	0800-09FF	99	0800-09FF	B9
		1					0C00-0FFF	A9	0A00-0BFF	A9
		2			8C00-8FFF	C9			0C00-0DFF	C9
		3							0E00-0FFF	E9
	5	0	1000-17FF	B1	1000-13FF	B1	1000-13FF	B1	1000-11FF	B1
		1					1400-17FF	D1	1200-13FF	B1
		2			9400-97FF	D1			1400-15FF	D1
		3							1600-17FF	F1
	7	0	1800-1FFF	99	1800-18FF	99	1800-19FF	99	1800-19FF	99
		1					1C00-1FFF	B9	1A00-1BFF	BB
		2			9C00-9FFF	D9			1C00-1DFF	D9
		3							1E00-1FFF	F9
2	0	0	2000-27FF	B5	2000-23FF	B5	2000-21FF	B5	2000-21FF	B5
		1			2400-27FF	A5	2200-23FF	A5	2200-23FF	A5
		2			A400-A7FF	C5			2400-25FF	C5
		3							2600-27FF	E5
	4	0	2800-2FFF	BD	2800-28FF	BD	2800-29FF	BD	2800-29FF	BD
		1					2C00-2FFF	AD	2A00-2BFF	AD
		2			AC00-AFFF	CD	-		2C00-2DFF	CD
		3							2E00-2FFF	ED
	6	0	3000-37FF	95	3000-33FF	95	3000-31FF	95	3000-31FF	95
		1					3400-37FF	B5	3200-33FF	B5
		2			3400-37FF	D5			3400-35FF	D5
		3							3600-37FF	F5
	8	0	3800-3FFF	9D	3800-38FF	9D	3800-39FF	9D	3800-39FF	9D
		1					3C00-3FFF	BD	3A00-3BFF	BD
		2			9C00-9FFF	DD			3C00-3DFF	DD
		3							3E00-3FFF	FD
1	0	0	4000-47FF	B2	4000-43FF	B2	4000-41FF	B2	4000-41FF	B2
		1					4400-47FF	A2	4200-43FF	A2
		2			4400-47FF	C2			4400-45FF	C2
		3							4600-47FF	E2
	3	0	4800-4FFF	BA	4800-48FF	BA	4800-49FF	BA	4800-49FF	BA
		1					4C00-4FFF	AA	4A00-4BFF	AA
		2			4C00-4FFF	CA			CC00-CDFF	CC
		3							4E00-4FFF	EA
	5	0	5000-57FF	B2	5000-53FF	B2	5000-51FF	B2	5000-51FF	B2
		1					5400-57FF	D2	5200-53FF	B2
		2			5400-57FF	D2			5400-55FF	D2
		3							5600-57FF	F2
	7	0	5800-5FFF	BA	5800-58FF	BA	5800-59FF	BA	5800-59FF	BA
		1					5C00-5FFF	DA	5A00-5BFF	BA
		2			5C00-5FFF	DA			5C00-5DFF	DA
		3							5E00-5FFF	FA
	2	0	6000-67FF	B6	6000-63FF	B6	6000-61FF	B6	6000-61FF	B6
		1					6400-67FF	A6	6200-63FF	A6
		2			6400-67FF	C6			6400-65FF	C6
		3							6600-67FF	E6
	4	0	6800-6FFF	BE	6800-68FF	BE	6800-69FF	BE	6800-69FF	BE
		1					6C00-6FFF	AE	6A00-6BFF	AE
		2			6C00-6FFF	CE			6C00-6DFF	CE
		3							6E00-6FFF	EE
	6	0	7000-77FF	96	7000-73FF	96	7000-71FF	96	7000-71FF	96
		1					7400-77FF	B6	7200-73FF	B6
		2			7400-77FF	D6			7400-75FF	D6
		3							7600-77FF	F6
	8	0	7800-7FFF	9E	7800-78FF	9E	7800-79FF	9E	7800-79FF	9E
		1					7C00-7FFF	BE	7A00-7BFF	BE
		2			7C00-7FFF	DE			7C00-7DFF	DE
		3							7E00-7FFF	FE

Display Adaptor	Channel	Monitor	1920 Char/Display 80 Ch X 24 Lines 64 Ch X 30 Lines		960 Char/Display 80 Ch X 12 Lines - 64 Ch X 15 or 16 Lines		960 Char/Display 40 Ch X 24 Lines		480 Char/Display 40 Ch X 12 Lines	
			Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address	Memory Buffer Area	Key-board Address
4	1	0	8000-87FF	B3	8000-83FF	B3	8000-81FF	B3	8000-81FF	B3
		1							8200-83FF	A3
		2			8400-87FF	C3			8400-85FF	C3
		3							8600-87FF	E3
	3	0	8800-8FFF	BB	8800-88FF	BB	8800-89FF	BB	8800-89FF	BB
		1					8C00-8FFF	AB	8A00-8BFF	AB
		2			8C00-8FFF	CB			8C00-8DFF	CB
		3							8E00-8FFF	EB
	5	0	9000-97FF	93	9000-93FF	93	9000-91FF	93	9000-91FF	93
		1					9400-97FF	B3	9200-93FF	B3
		2			9400-97FF	D3			9400-95FF	D3
		3							9600-97FF	F3
	7	0	9800-9FFF	9B	9800-98FF	9B	9800-99FF	9B	9800-99FF	9B
		1					9C00-9FFF	BB	9A00-9BFF	BB
		2			9C00-9FFF	DB			9C00-9DFF	DB
		3							9E00-9FFF	FB
3	0	0	A000-A7FF	B7	A000-A3FF	B7	A000-A1FF	B7	A000-A1FF	B7
		1			A400-A7FF	A7	A200-A3FF	A7	A200-A3FF	A7
		2			A400-A7FF	C7			A400-A5FF	C7
		3							A600-A7FF	E7
	4	0	A800-AFFF	BF	A800-ABFF	BF	A800-A9FF	BF	A800-A9FF	BF
		1			AC00-AFFF	AF	AA00-ABFF	AF	AA00-ABFF	AF
		2			AC00-AFFF	CF			AC00-ADFF	CF
		3							AE00-AFFF	EF
	6	0	B000-B7FF	97	B000-B3FF	97	B000-B1FF	97	B000-B1FF	97
		1			B400-B7FF	B7	B200-B3FF	B7	B200-B3FF	B7
		2			B400-B7FF	D7			B400-B5FF	D7
		3							B600-B7FF	F7
	8	0	B800-BFFF	9F	B800	9F	B400-B5FF	9F	B800-B9FF	9F
		1			BC00-BFFF	BF	BC00-BDFF	BF	BA00-BBFF	BF
		2			BC00-BFFF	DF			BC00-BDFF	DF
		3							BE00-BFFF	FF
4	1	0	C000-C7FF	B4	C000-C3FF	B4	C000-C1FF	B4	C000-C1FF	B4
		1					C400-C7FF	A4	C200-C3FF	A4
		2			C400-C7FF	C4			C400-C5FF	C4
		3							C600-C7FF	E4
	3	0	C800-CFFF	BC	C800-CBFF	BC	C800-C9FF	BC	C800-C9FF	BC
		1					CC00-CFFF	AC	CA00-CBFF	AC
		2			CC00-CFFF	CC			CC00-CDFF	CC
		3							CE00-CFFF	EC
	5	0	D000-D7FF	B4	D000-D3FF	B4	D000-D1FF	B4	D000-D1FF	B4
		1					D400-D7FF	B4	D200-D3FF	B4
		2			D400-D7FF	D4			D400-D5FF	D4
		3							D600-D7FF	F4
	7	0	D800-DFFF	9C	D800-DBFF	9C	D800-D9FF	9C	D800-D9FF	9C
		1					DC00-DFFF	BC	DA00-DBFF	BC
		2			DC00-DFFF	DC			DC00-DDFF	DC
		3							DE00-DFFF	FC
	2	0	E000-E7FF	B8	E000-E3FF	B8	E000-E1FF	B8	E000-E1FF	B8
		1					E400-E7FF	A8	E200-E3FF	A8
		2			E400-E7FF	C8			E400-E5FF	C8
		3							E600-E7FF	E8
	4	0	E800-EFFF	90	E800-EBFF	90	E800-E9FF	90	E800-E9FF	90
		1					EC00-EFFF	B0	EA00-EBFF	B0
		2			EC00-EFFF	D0			EC00-EDFF	D0
		3							EE00-EFFF	F0
	6	0	F000-F7FF	98	F000-F3FF	98	F000-F1FF	98	F200-F1FF	98
		1					F400-F7FF	B8	F200-F3FF	B8
		2			F400-F7FF	D8			F400-F5FF	D8
		3							F600-F7FF	F8
	8	0	F800-FFFF	A0	F800-FBFF	A0	F800-F9FF	A0	F800-F9FF	A0
		1					FC00-FFFF	C0	FA00-FBFF	C0
		2			FC00-FFFF	E0			FC00-FDFF	E0
		3							FE00-FFFF	F0

DISPLAY DATA MEMORY BUFFER ASSIGNMENTS

DEVICE ADDRESS & INTERRUPT ASSIGNMENTS

DEVICE	MUX	MUX PORT	INT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEM ADAPTERS			
† 2331 PARS RX	0	4	5
PARS TX	0	5	4
† 2341 MINI RX	0	1	2
MINI TX	0	2	2
† 2332 FIDS RX	0	1	2
FIDS TX	0	2	2
PRINTERS	0 1 2	1-3,6 0-7 0-7	
† ≠ 1977	0 1 2	TAPE 933946-2, -5, -6 OR 933284-2, -4. (PRINTERS ARE ASSIGNED FIRST)	

TAPE 933946-3 OR 933284-3, -4

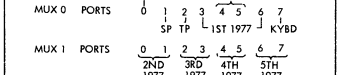
TAPE 933946-5 OR 863028-2

NOTES:

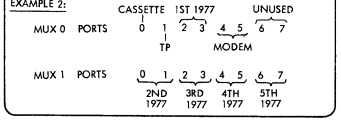
†ALL MODEM ADAPTERS RECEIVE ON THE LOWEST NUMBERED PART OF THE PAIR AND TRANSMIT ON THE HIGHEST.

THE 1977 REQUIRES AN AMA MODEM ADAPTER THAT IS CONNECTED TO 2 PORTS ON THE SAME MUX, STARTING WITH THE LOWEST NUMBERED PORT AVAILABLE SEE EXAMPLES BELOW.

EXAMPLE 1:

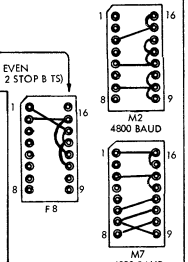


EXAMPLE 2:



PTS/MINI PATCHES

FOR THIS MINI MODEM ADAPTER	INSERT THESE PATCHES (592153-) INTO THE LOCATIONS SHOWN
ASYNC AMA 2341 591725	M2-G59, M7-G58 } 1200 BAUD — SEE M2 & M7 BELOW FOR 4800 BAUD L2-G65 G4-G225 E8-G227 F8-TBR (7 BITS, EVEN PARITY, 2 STOP B TS)
SYNC CTMC 2332 591707G2	A1-G73 D7-G31 J8-G32 Z1-G113 Z3-G71 Z4-G72



PTS/1977 PATCHES

INSERT PATCHES (592153-) INTO THE LOCATIONS SHOWN

G223-M7
G222-M2
G65-L2
G225-G4
G226-F8
G227-E8

PTS/FIDS PATCHES

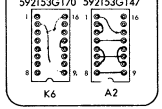
CTMC 591707G2
INSERT PATCHES (592153-) INTO LOCATIONS SHOWN

G73 - A1 G113 - 21
G31 - D7 G71 - 23
G32 - J8 G72 -24

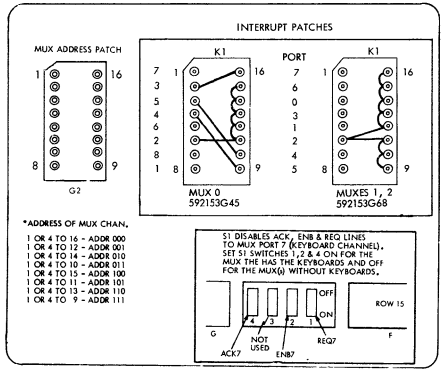
IPARS MODEM ADAPTER PATCHES

INSERT THESE PATCH PLUGS INTO BOARD LOCATIONS K6 AND A2

592153G170 592153G147



MULTIPLEX CHANNEL CONTROLLER KEYBOARD, INTERRUPT AND ADDRESS PATCHES



AA/PTS-100 IA/TA ADDRESS ASSIGNMENTS

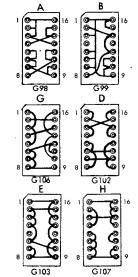
VALUE PROVIDED BY AMERICAN	IA TO BE SET ON F,B, IN HEX	TA TO BE SET ON F,B, IN HEX
DEVICE OR INTERCHANGE	01	02
	02	04
	03	06
	04	08
	05	0A
	06	0C
	07	0E
	08	10
	09	12
	0A	14
	0B	16
	0C	18
	0D	1A
	0E	1C
	0F	1E
	10	20
	11	22
	12	24
	13	26
	14	28
	15	2A
	16	2C
	17	2E
	18	30
	19	32
	1A	34
	1B	36
	1C	38
	1D	3A
	1E	3C

IPARS SYSTEM CONFIGURATION VARIABLE PATCHES, SWITCHES AND REMOTE PRINTER ADDRESSES

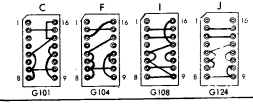
MULTI-INTERFACE SERIAL ADAPTER (MISA) PATCHING (592153-)

INSERT THESE PATCHES FOR THIS MODEL MISA 593296-	M5	B2
G1 TERMINET 300 BAUD	A	C
G3 TERMINET 1200 BAUD	B	C
G5 TTY 110 BAUD	G	F
G7 TTY 50 BAUD	D	F
G9 TTY 75 BAUD	E	F
G11 TICKET & BOARDING PASS PRINTER	H	I
CENTRONICS	H	J
TERMINET 30	A	J

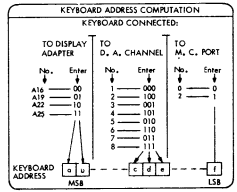
M5 PATCH CONFIGURATIONS (BAUD RATES)

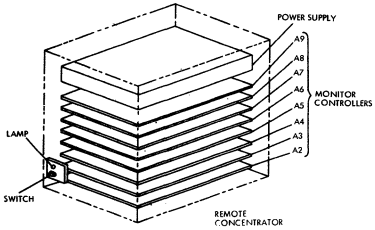


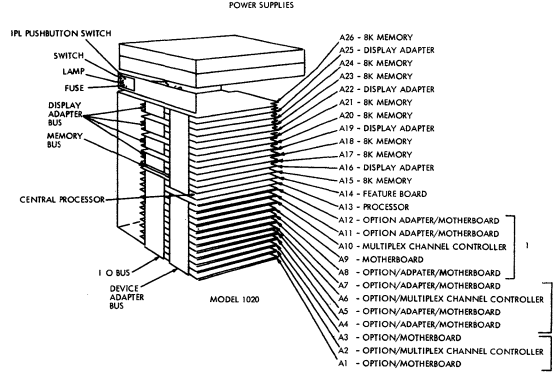
B2 PATCH CONFIGURATIONS (CONTROL)

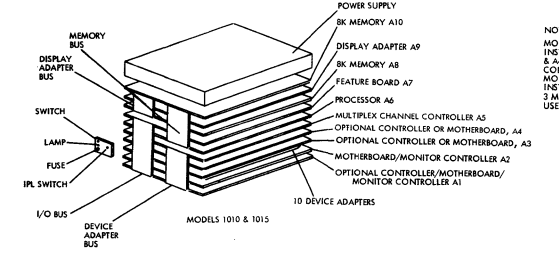


KEYBOARD ADDRESS COMPUTATION









NOTE:

MONITOR CONTROLLERS ARE INSTALLED IN SLOTS A1, A2, A3 & A4 WHEN ONLY 2 MULTIPLEX CONTROLLERS ARE USED. MONITOR CONTROLLERS ARE INSTALLED IN A7, A8 & A9 WHEN 3 MULTIPLEX CONTROLLERS ARE USED.

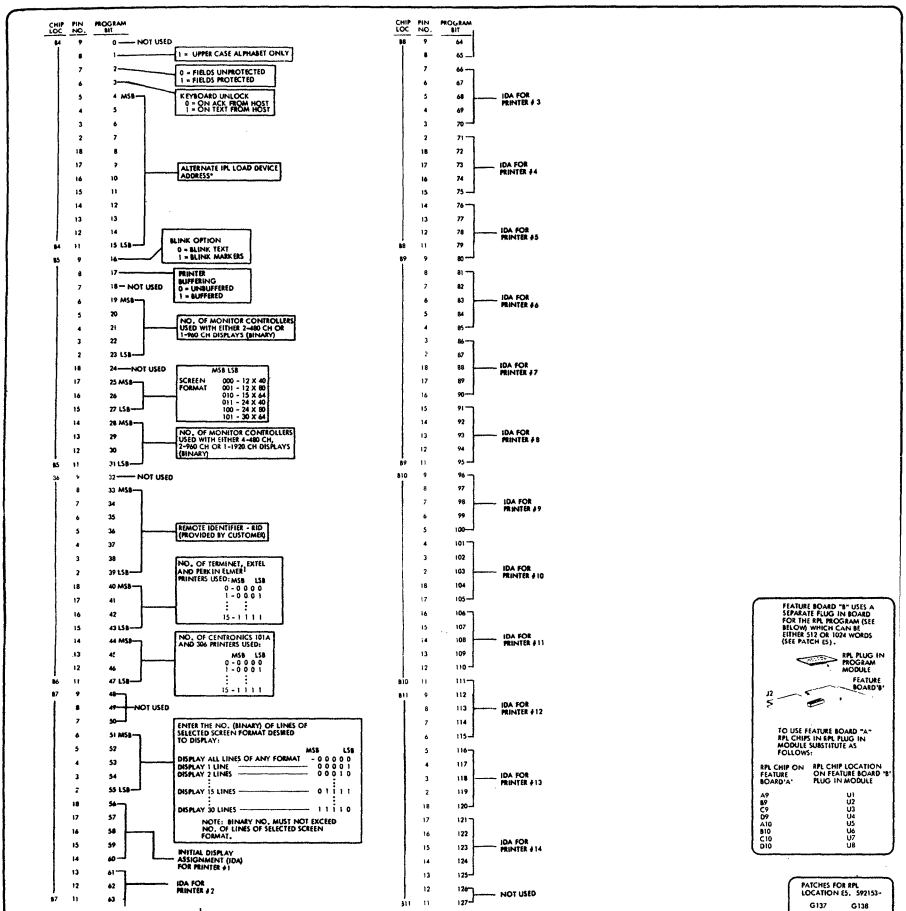
COMMUNICATIONS REGION TABLE

LOAD SIZE OF PROGRAM
KEYBOARD MODULE
SECOND HALF OF INITIALIZER
TASK SUPERVISOR
PRINTER INITIALIZER
SERIAL PRINTER ROUTINE
TICKET & BOARDING PASS PRINTERS INITIALIZER
PRINTER STATUS TABLES
DISPLAY STATUS TABLES
NUMBER OF DISPLAYS
NUMBER OF PRINTERS
CCC COUNTER
NUMBER OF MESSAGES RECEIVED
NUMBER OF MESSAGES TRANSMITTED
EOMC'S IN TKT AND BOARDING PASS MESSAGES
DATA LOST COUNTER
CARRIER LOST COUNTER
IOCQ'S FOR DISPLAYS
IOCQ'S FOR PRINTERS
OUTPUT - TO HOST - BUFFER
VALID TERMINAL ADDRESSES
VALID PRINTER ADDRESSES
AIRLINE ID
INTERCHANGE 1
INTERCHANGE 2
LOCATION 0010 CONTAINS THE ADDRESS OF THIS TABLE

LED MEMORY BUFFER ASSIGNMENTS

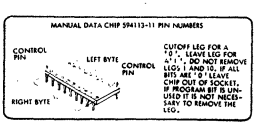
Adaptor	Channel	1920 Character Display	960 Character Display		480 Character Display			
			Mon. 0	Mon. 1	Mon. 0	Mon. 1	Mon. 2	Mon. 3
1	1	07B0	03C0	07C0	01E0	03E0	05E0	07E0
	2	27B0	23C0	27C0	21E0	23E0	25E0	27E0
	3	0FB0	0BC0	0FC0	09E0	0BE0	0DE0	0FE0
	4	2FB0	2BC0	2FC0	29E0	2BE0	2DE0	2FE0
	5	17B0	13C0	17C0	11E0	13E0	15E0	17E0
	6	37B0	33C0	37C0	31E0	33E0	35E0	37E0
	7	1FB0	1BC0	1FC0	19D0	1BE0	1DE0	1FE0
	8	3FB0	3BC0	3FC0	39E0	3BE0	3DE0	3FE0
2	1	47B0	43C0	47C0	41E0	43E0	45E0	47E0
	2	67B0	63C0	67C0	61E0	63E0	65E0	67E0
	3	4FB0	43C0	4FC0	49E0	4BE0	4DE0	4FE0
	4	6FB0	68C0	6FC0	69E0	6BE0	6DE0	6FE0
	5	57B0	53C0	57C0	51E0	53E0	55E0	57E0
	6	77B0	73C0	77C0	71E0	73E0	75E0	77E0
	7	5FB0	58C0	5FC0	59E0	5BE0	5DE0	5FE0
	8	7FB0	78C0	7FC0	79E0	7BE0	7DE0	7FE0
3	1	87B0	83C0	87C0	81E0	83E0	85E0	87E0
	2	A7B0	A3C0	A7C0	A1E0	A3E0	A5E0	A7E0
	3	8FB0	88C0	8FC0	89E0	8BE0	8DE0	8FE0
	4	AFB0	ABC0	AFC0	A9E0	ABE0	ADE0	AFE0
	5	97B0	93C0	97C0	91E0	93E0	95E0	97E0
	6	B7B0	B3C0	B7C0	B1E0	B3E0	B5E0	B7E0
	7	9FB0	98C0	9FC0	99E0	9BE0	9DE0	9FE0
	8	BFB0	BBC0	BFC0	B9E0	BBE0	BDC0	BFE0
4	1	C7B0	C3C0	C7C0	C1E0	C3E0	C5E0	C7E0
	2	E7B0	E3C0	E7C0	E1E0	E3E0	E5E0	E7E0
	3	CFB0	CBC0	CFC0	C9E0	CBE0	CDE0	CFE0
	4	EFB0	EBC0	EFC0	E9E0	EBE0	EDE0	EFE0
	5	D7B0	D3C0	D7C0	D1E0	D3E0	D5E0	D7E0
	6	F7B0	F3C0	F7C0	F1E0	F3E0	F5E0	F7E0
	7	DFB0	DBC0	D7C0	D9E0	DBE0	DDE0	DFE0
	8	FFB0	FBC0	FFC0	F9E0	FBE0	FDE0	FFE0

PTS 100 FEATURE BOARD 'B' CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR PITNEY BOWES EMULATOR 933259-3



[1] IF PERKIN ELMER PRINTER IS USED, IT MUST BE SET UP AS A TERMINET PRINTER.

*REFER TO USER SYSTEM SPECIFICATION OR RAYTHEON SALES ORDER SUMMARY



MANUAL DATA CHIP LOC	ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
	IPL	512 RPL	1024 RPL
B4	40,41	40,41	40,41
B5	42,43	42,43	42,43
B6	44,45	44,45	44,45
B7	46,47	46,47	46,48
B8	80,81	400,401	800,801
B9	82,83	402,403	802,803
B10	84,85	404,405	804,805
B11	86,87	406,407	806,807

DUAL PROGRAM LOAD (DPL)

DPL IS DETERMINED BY PATCH E5.

IPL = $\overline{DR}$ • IPL SW • (PB + WDT + DO I/O) + DPL • IPL SW (PB + WDT).

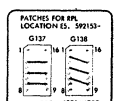
RPL = $\overline{DR}$ • RPL SW • (PB + WDT + DO I/O) + DPL • (RPLSW • (PB + WDT) + DO I/O.

IPLSW = IPL SWITCH
RPLSW = RPL SWITCH
PB = IPL PUSHBUTTON
WDT = WATCHDOG TIMER

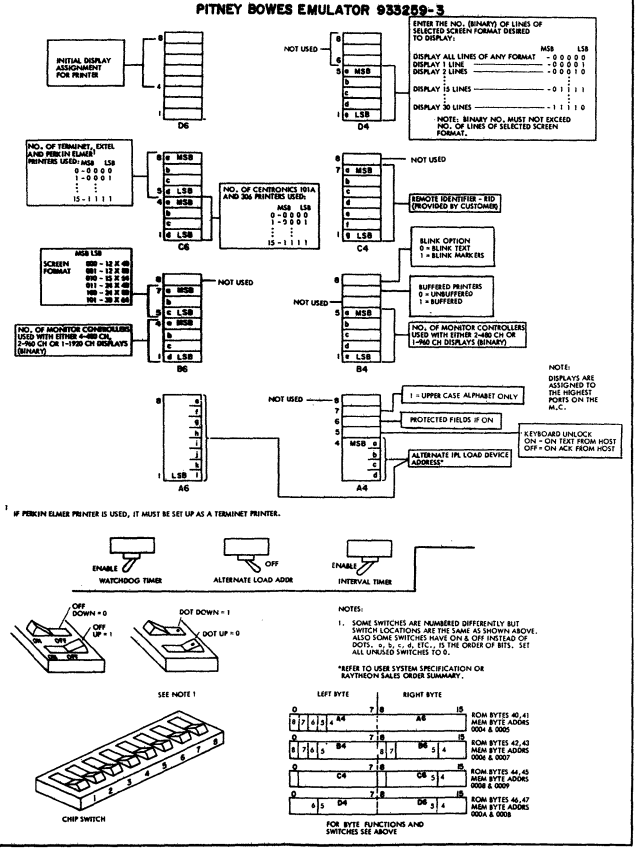
FEATURE BOARD "B" USES A SEPARATE PLUG IN BOARD FOR THE RPL PROGRAM (SEE BELOW WHICH CAN BE EITHER 512 OR 1024 WORDS (SEE PATCH E5).

TO USE FEATURE BOARD "A" RPL CHIPS IN RPL PLUG IN MODULE SUBSTITUTE AS FOLLOWS:

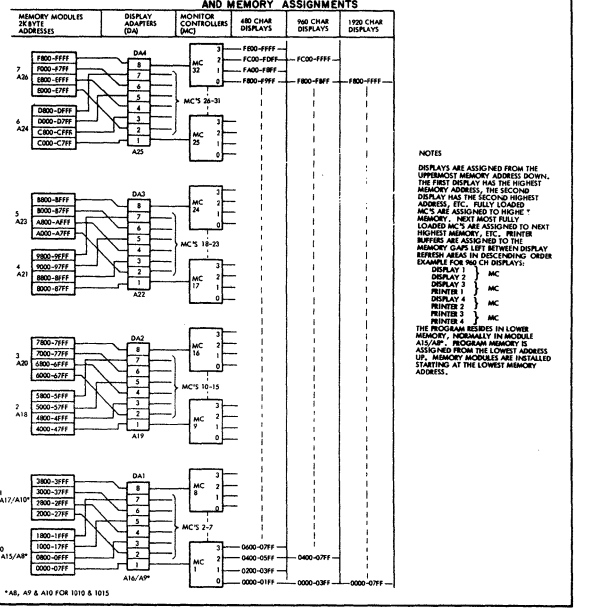
RPL CHIP ON FEATURE BOARD 'A'	RPL CHIP LOCATION ON FEATURE BOARD 'B' PLUG IN MODULE
A9	U1
B9	U2
C9	U3
D9	U4
A10	U5
B10	U6
C10	U7
D10	U8



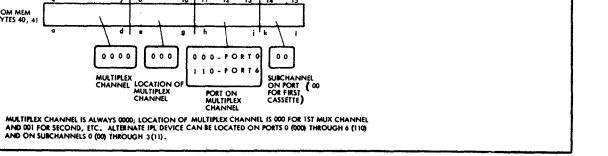
PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR PITNEY BOWES EMULATOR 933259-3



DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



ALTERNATE IPL LOAD DEVICE ADDRESS ASSIGNMENTS



MULTIPLEX CHANNEL IS ALWAYS (000). LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

DISPLAY ADAPTER "C"

Character/Line Format and Memory Refresh Timing Patch Plugs

For These Displays Char/Lines No.of Lines Formats	Insert These Patches (592153-)	INTO BOARD LOCATIONS E10	J16	C2 (Norm)	C2 (Opt)	C3 16K	C3 8K
80 X 24		G1	G3	G134 or G136		G133 or G135	
→ 64 X 30 & Split Screen		G2	G3	G134 or G136		G133 or G135	
80 X 12		G1	G4	G134 or G136		G133 or G135	
64 X 15 or 16		G2	G4	G134 or G136		G133 or G135	
40 X 12		G1	G5	G134 or G136		G133 or G135	
40 X 24		G1	G48	G134 or G136		G133 or G135	

E10 - Number of characters per line

J16 - Number of lines per format

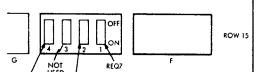
C2 - Memory refresh
- G134 - 2 ms (Normal timing)
- G136 - 1 ms (Option timing)

C3 - Type of memory module
- G135 - 8K memory module
- G133 - 16K memory module

MULTIPLEX CHANNEL CONTROLLER

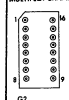
DISABLE/ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, ENB & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-0584-1.

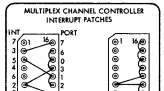
MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH



G2 BOARD LOCATION

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	3 OR 4 TO 12
ADDR 2	2 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	0 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT 0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO CASSETTE MODEM, ALL MODELS (WRITE TO PRINTER)	1,17	2,18	3,19	4,20	5,21	6,22	7,23	8,24
	33	34	35	36	37	38	39	40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25	10,26	11,27	12,28	13,29	14,30	15,31	16,32
	41	42	43	44	45	46	47	48

NOTE:
- CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER
- PORT 1 AND 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER ARE NOT USED
- FIRST PRINTER IS ASSIGNED TO PORT 3 OF FIRST MULTIPLEX CHANNEL CONTROLLER
- PRINTERS ARE ASSIGNED TO ALL OTHER PORTS

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	3
MODEM:			
SEND	0	2	5
REC	0	1	5
PRINTERS:			
1-4	0	3-6	2
5-12	1	0-7	2
13-15	2	0-7	2

NOTE: TERMINET AND EXTEL PRINTERS MUST BE ASSIGNED FIRST

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT 40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5	See Below			
6				
7				
8				

Options:

Switch 5 — Set to closed to disable the controlled data field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.
When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

for HI Intensity - close ODD numbered switches and open others.
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MONITOR CONTROLLER K (P/N 860963)

Option Pin Assignments

FORMAT SELECTION

Config. Plug Pin #	DISPLAY FORMATS 40X12	40X24	64X15	64X30	80X12	80X24
11	Cut	In	Cut	In	Cut	In
12	Cut	Cut	In	In	In	In
17	In	In	Cut	Cut	In	In

MONITOR CONTROLLER B-16

16 CHIP SWITCH SETTING	40 CHAR. 12 LINES	80 CHAR. 12 LINES	64 CHAR. 15/16 LINES	80 CHAR. 24 LINES	64 CHAR. 30 LINES	40 CHAR. 24 LINES	STEP SCAN*
66-1	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	CLOSED
66-2	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
66-3	OPEN	OPEN	OPEN	CLOSED	CLOSED	CLOSED	CLOSED
66-4	OPEN	CLOSED	OPEN	CLOSED	CLOSED	OPEN	CLOSED
66-5	CLOSED	OPEN	OPEN	CLOSED	OPEN	CLOSED	**
66-6	CLOSED	OPEN	OPEN	OPEN	OPEN	CLOSED	OPEN
66-7	OPEN	CLOSED	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
66-8**	OPEN	OPEN	OPEN*	OPEN	OPEN	OPEN	OPEN

*USABLE ONLY ON 24 OR 30 LINE FORMAT. SPACING BETWEEN LINES IS ADJUSTABLE BY SETTING R30.

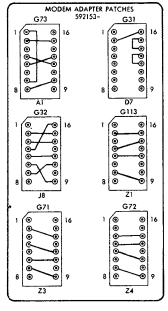
**SET AS INDICATED FOR 24 OR 30 LINE FORMAT.

* CLOSED FOR 16 LINE FORMAT

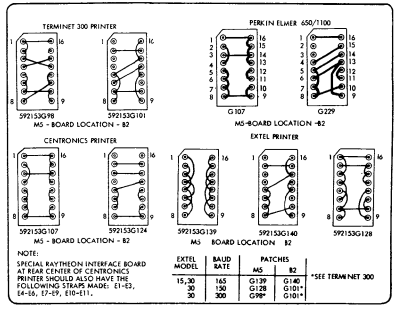
**66-8 IS USED ON SOME MC'S (IT IS USED ON ALL 16 LINE MC'S.

NOTE: WHEN MC IS USED WITH SPLIT SCREEN DISPLAYS A JUMPER IS CONNECTED BETWEEN X73 PIN 15 AND X7 PIN 14.

MODEM ADAPTER PATCHES



MISA PATCHES



NOTE:
SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

EXTEL MODEL	BAUD RATE	PATCHES MS	PATCHES B2
15,30	165	G139	G140
30	150	G128	G101*
30	300	G98*	G101*

*SEE TERMINET 300

AUGUST 1978
44-10220
SHEET 3 OF 4

PATCH AND SWITCH SETTING FOR PITNEY BOWES 933259-3 EMULATOR

CASSETTE PROGRAM PATCH PROCEDURE

1. IPL OLD CASSETTE.
2. DURING IPL STORE X'8XXX' INTO LOCATION 0 (WHERE XXX = DEVICE ADDRESS OF TARGET DRIVE).
3. WHEN IPL IS COMPLETE LOCATION 0 WILL CONTAIN X'0100'. IF NOT RETRY.
4. ENTER PATCHES. DO NOT PRESS STOP OR RESET.
5. PUT A NEW CASSETTE IN TARGET DRIVE.
6. STORE X'8XXX' INTO LOCATION 0 AS ABOVE. LOCATION 0 WILL CHANGE TO X'0300' TO INDICATE THAT THE DUMP IS IN PROGRESS.
7. THE TAPE WILL REWIND AND STOP WHEN COMPLETE AND LOCATION 0 WILL CONTAIN X'0100'. IF MORE COPIES ARE DESIRED RETURN TO STEP 5.
8. IF AN ERROR OCCURS, THE TAPE WILL TRY TO REWRITE CONTINUOUSLY. TO START OVER INSERT A NEW CASSETTE AND STORE X'8XXX' INTO LOCATION 0.

NOTE: FOR ADDITIONAL INFORMATION REFER TO FIB NO. PS-0018.

COMMUNICATIONS REGION (ADDRESS AT LOCATION X'14')

WORD DISPLACEMENT	DEFINITION	
0	REVISION LEVEL (ASCII)	REVISION SUBLEVEL (ASCII)
1	STATISTICS TABLE ADDRESS	
2	ERROR TABLE ADDRESS	
3	LINE CONTROL BLOCK ADDRESS	
4	ADDRESS OF TABLE CONTAINING DST ADDRESSES	
5	RECEIVE BUFFER ADDRESS	
6	ADDRESS OF FIRST XMIT BUFFER	
7	ADDRESS OF SOFTWARE TIMER CELL	

PRINTER STATUS TABLE (PST ADDR IN DST)

WORD DISPLACEMENT	DEFINITION	
0	STATUS	LUN
1	CURRENT PRINT ADDRESS	
2	PRINTER BUFFER ADDRESS	
3	PRINTER TIMER ADDRESS	
4	PRINTER IOCQ ADDRESS	
5	PRINTER STATUS FOR HOST	

ERROR TABLE (ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION
0	MODEM RECEIVE ERROR COUNTER
1	MODEM TRANSMIT ERROR COUNTER
2	SOH IN TEXT ERROR COUNTER
3	ADDRESSING ERROR COUNTER
4	ILLEGAL CHARACTER ERROR COUNTER
5	ESCAPE SEQUENCE ERROR COUNTER
6	CHARACTER PARITY ERROR COUNTER
7	BCC ERROR COUNTER
8	CURSOR ADDRESSING ERROR COUNTERS
9	MODEM RECEIVE IO ACTION ERROR COUNTER

LINE CONTROL BLOCK (LCB ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION	
0	RECEIVE CHANNEL UP/DOWN	
1	CURRENT RECEIVE IOCQ ADDRESS	
2	FIRST RECEIVE IOCQ ADDRESS	
3	.OMPRC RE-ENTRANCE ADDRESS	
4	FIRST MODEM RECEIVE BUFFER ADDRESS	
5	FIRST DST ADDRESS	
6	NUMBER OF DST'S	
7	MODEM RECEIVE TIMER ADDRESS	
8	MODEM RECEIVE LUN	
9	NUMBER OF XMIT BUFFERS AVAILABLE	
A	MODEM XMIT CHANNEL UP/DOWN	
B	MODEM XMIT ERROR FLAG	
C	CURRENT MODEM XMIT IOCQ ADDRESS	
D	FIRST XMIT IOCQ ADDRESS	
E	MODEM XMIT TIMER ADDRESS	
F	INPUT MESSAGE COLLECTION ACTIVE FLAG	
10	MODEM XMIT LUN	
11	MODEM XMIT BUFFER ADDRESS	
12	NOT USED	
13	CURRENT OUTPUT MSG PROCESSOR DST	
14	POLL TIMER ADDRESS	
15	ACK CONTROL BYTE	OUTPUT MESSAGE TYPE
16	SID FROM LAST OUTPUT MSG	DID FROM LAST OUTPUT MESSAGE
17	RID FROM FEATURE BOARD	SID OF LAST INPUT TERMINAL
18	TERMINAL STATUS OF LAST INPUT DEVICE	
19	LAST DST TO RECEIVE INPUT	

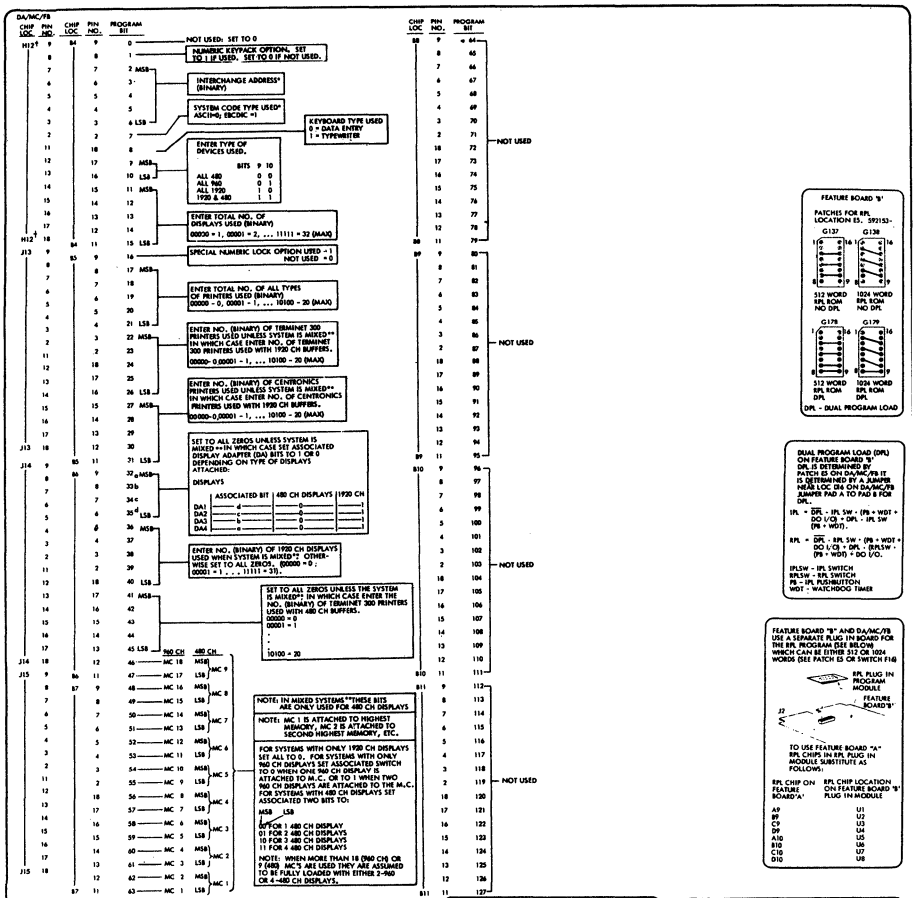
DISPLAY STATUS TABLE (FIRST DST ADDR IN LCB)

WORD DISPLACEMENT	DEFINITION	
0	CURSOR ADDRESS	
1	KEYBOARD NUMBER	STATUS
2	LINK TO NEXT DST	
3	HOME ADDRESS	
4	NOT USED	XMIT LUN
5	HOME FOR DEBUG	
6	LED BYTE ADDRESS	
7	CURSOR ADDRESS DURING MESSAGE COLLECTION	
8	PRINTER STATUS TABLE ADDRESS	
9	SOE ADDRESS	
A	SID	PRINTER STATUS
B	DISPLAY END ADDRESS	
C	NUMBER OF CHAR LEFT ON LINE	
	SPECIAL MESSAGE CODE STORAGE FOR RETRANSMIT	NEW U-100 STATUS

STATISTICS TABLE (ADDR IN COMMUNICATIONS REGION)

WORD DISPLACEMENT	DEFINITION
0	OUTPUT MESSAGE FROM HOST
1	INPUT MESSAGE TO HOST
2	BROADCAST MESSAGE FROM HOST
3	PRINTER MESSAGE FROM HOST
4	PRINTER STATUS REQUEST FROM HOST
5	MESSAGE WAITING FROM HOST
6	REPLY REQUEST TO HOST
7	RETRANSMIT REQUEST FROM HOST
8	GENERAL POLL FROM HOST
9	SPECIFIC POLL FROM HOST
A	OUTPUT FROM HOST TO ANOTHER RID
B	NO BUSINESS RESPONSE SENT TO HOST
C	MESSAGE WAITING SENT TO HOST
D	PRINTER STATUS SENT TO HOST
E	LOOK-FOR SYNC ISSUED TO MODEM RECEIVE
F	TRAFFIC POLLS W/O ACK
10	TRAFFIC POLLS W/ACK
11	STATUS POLLS W/O ACK
12	STATUS POLLS W/ACK

PTS 100 FEATURE BOARD 'B' AND DA/MC/FB CONFIGURATION CONTROL MANUAL DATA CHIP SETTINGS FOR TRAVELERS DISC BACKUP 933403



† J12 ON SOME OLDER BOARDS

MANUAL DATA CHIP LOC		ASSOCIATED CONFIGURATION CONTROL WORD BYTE ADDRESSES (HEX)		
DA, MC, FB	FEATURE BOARD B	IPL	512 RPL	1024 RPL
J12 †	B4	40, 41	40, 41	40, 41
J13	B5	42, 43	42, 43	42, 43
J14	B6	44, 45	44, 45	44, 45
J15	B7	46, 47	46, 47	46, 48
	B8	80, 81	400, 401	800, 801
	B9	82, 83	402, 403	802, 803
	B10	84, 85	404, 405	804, 805
	B11	86, 87	406, 407	806, 807

MANUAL DATA CHIP 594113-11 PIN NUMBERS

CUT OFF LEG FOR A '0'. LEAVE LEG FOR A '1'. DO NOT REMOVE LEGS 1 AND 10. IF ALL BITS ARE '0' LEAVE CHIP OUT OF SOCKET. IF PROGRAM BIT IS UNUSED IT IS NOT NECESSARY TO REMOVE THE LEG.

DA/MC/FB SWITCH G2 SETTINGS

SWITCH	40 X 12	40 X 24	80 X 12	80 X 24	64 X 15	64 X 30
1	*	*	*	*	*	*
2	*	*	*	*	*	*
3	OPEN	CLOSE	OPEN	OPEN	OPEN	OPEN
4	OPEN	CLOSE	OPEN	CLOSE	OPEN	CLOSE
5	OPEN	OPEN	OPEN	OPEN	CLOSE	CLOSE
6	OPEN	OPEN	CLOSE	CLOSE	CLOSE	CLOSE
7	*	*	*	*	*	*
8	*	*	*	*	*	*

*OPTIONS:
SWITCH 1 - CLOSE TO DISPLAY INTENSIFIED FIELD AT LOWER INTENSITY LEVEL (SWITCH 2 OPEN)
SWITCH 2 - CLOSE TO DISPLAY INTENSIFIED FIELD AT HIGHER INTENSITY LEVEL (SWITCH 1 OPEN)
SWITCH 7 - OPEN WHEN 8K OR 28K OF MEMORY IS INSTALLED OTHERWISE CLOSE
SWITCH 8 - OPEN WHEN ONLY 12K OF MEMORY IS INSTALLED OTHERWISE CLOSE

DA/MC/FB SWITCH F16 SETTINGS

SWITCH	FUNCTION
1	CLOSE WHEN 512 WORD RPL PROGRAM IS USED. OPEN WHEN 1024 WORD RPL PROGRAM IS USED.
2	OPEN DISABLES DISPLAY TIMEOUT OPTION AND RETURNS BIT TO SOFTWARE CONTROL
3	CLOSED REFRESHES MEMORY EVERY 2 MS. OPEN REFRESHES MEMORY EVERY 1 MS. NOTE: CLOSED IS THE NORMAL POSITION.
4	CLOSE TO DISABLE 1-SEC TONE OPTION.
5	OPEN TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET OR RESET; CLOSE TO ACTIVATE 1-SEC TONE OPTION WHEN LED BYTE BIT 4 IS SET.
6	CLOSE FOR BLINKING DATA FIELD. OPEN FOR BLANK DATA FIELD.
7	OPEN WHEN 512 WORD RPL PROGRAM IS USED. CLOSE WHEN 1024 WORD RPL PROGRAM IS USED.
8	OPEN WHEN 1024 WORD RPL PROGRAM IS USED. CLOSE WHEN 512 WORD RPL PROGRAM IS USED.

MONITOR CONTROLLER C CHARACTER LINE FORMAT 6s SWITCH SETTINGS

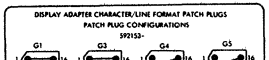
SWITCH	40 X 12	80 X 12	(24)	OPTIONS
1	———	—	—	NOTE 1
2	———	—	—	NOTE 2
3	OPEN	OPEN	CLOSED	———
4	OPEN	CLOSED	CLOSED	———
5	CLOSED	CLOSED	CLOSED	———
6	CLOSED	OPEN	OPEN	———
7	OPEN	CLOSED	CLOSED	———
8	———	—	—	NOTE 3

NOTES:

1. CONTROLS THE POWER TO THE LED PANEL. IF OPEN, THE PANEL HAS POWER, EVEN IF THE DISPLAY IS TURNED OFF. WHEN CLOSED THE LED PANEL HAS POWER ONLY WHEN THE DISPLAY IS TURNED ON.
2. CONTROLS LED BIT 7. IF OPEN THE MONITOR POWER CONTROLS LED 7. IF CLOSED THE LED 7 OPERATES NORMALLY.
3. SWITCH CONTROLS TONE OPTION. IF OPEN AND A TONE DEVICE IS CONNECTED TO LED 4 CKT. A ONE SECOND TONE OCCURS WHEN LED BIT 4 IS SET. IF CLOSED LED 4 OPERATES NORMALLY.

DISPLAY ADAPTER CHARACTER/LINE FORMAT PATCH PLUGS

PATCH PLUG CONFIGURATIONS
5921S3-



FOR THESE DISPLAY CHAR/LINE & NO. OF LINES FORMATS	INSERT THESE PATCHES (5921S3-)	INTO BOARD LOCATIONS D15 AND J16	
80 X 24		G1	G3
80 X 12		G1	G4
40 X 12		G1	G5

MOTHERBOARD SCREW SWITCH SETTINGS

WHEN AN I/O DEVICE IS CONNECTED TO A MULTIPLEX CHANNEL PORT

INSERT SCREWS INTO THESE SCREW SWITCHES ON THE MOTHERBOARD(S) UNDER THE ASSOCIATED I/O DEVICE ADAPTER.

	MULTIPLEX CHANNEL PORT							
	0	1	2	3	4	5	6	7*
CARD READER TTY (WRITE TO) CASSETTE MODEM, ALL MODELS (WRITE TO) PRINTERS	1,17 33	2,18 34	3,19 35	4,20 36	5,21 37	6,22 38	7,23 39	8,24 40
TTY (READ FROM) MODEM, ALL MODELS (READ FROM)	9,25 41	10,26 42	11,27 43	12,28 44	13,29 45	14,30 46	15,31 47	16,32 48

NOTE:

CASSETTE IS ASSIGNED TO PORT 0 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (READ FROM) IS ASSIGNED TO PORT 1 OF FIRST MULTIPLEX CHANNEL CONTROLLER

MODEM (WRITE TO) IS ASSIGNED TO PORT 2 OF FIRST MULTIPLEX CHANNEL CONTROLLER

PRINTERS ARE ASSIGNED TO ALL OTHER PORTS.

*PORT 7 ON THE FIRST MULTIPLEX CHANNEL CONTROLLER IS USED TO INPUT KEYBOARD DATA.

M15A PATCHES

TERMINET 300 PRINTER

5921S3G98 — M5 - BOARD LOCATION - B2

5921S3G101

CENTRONICS PRINTER

5921S3G107 — M5 - BOARD LOCATION - B2

5921S3G124

NOTE:

SPECIAL RAYTHEON INTERFACE BOARD AT REAR CENTER OF CENTRONICS PRINTER SHOULD ALSO HAVE THE FOLLOWING STRAPS MADE: E1-E3, E4-E6, E7-E9, E10-E11.

MONITOR CONTROLLER D CHARACTER/LINE FORMAT AND CHARACTER INTENSITY LEVEL SWITCH SETTINGS

Switch Chip L-8

Switch	FORMAT			
	40 X 12	40 X 24	80 X 12	80 X 24
1	Close	Close	Open	Open
2	Open	Open	Close	Close
3	Open	Open	Close	Close
4	Open	Close	Open	Close
5	———	See Below	———	———
6	———		———	———
7	———		———	———
8	———		———	———

Options:

Switch 5 — Set to closed to disable the controlled dote field feature.

Switch 6 — Set to closed to disable the 1-second tone option. (Tone will remain on as long as the corresponding bit in the LED byte is set.)

Switch 7 — When open the 1-second tone option will be triggered when bit 4 of the LED byte is either set or reset.
When closed, the tone will only respond to bit 4 being set. Note - switch 6 must also be open.

Switch 8 — Closing disables the Display Power On option and returns this bit to software control.

Switch Chip D9

These switches determine whether an intensified field will be displayed at a higher or lower intensity level than normal:

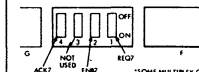
for HI Intensity - close ODD numbered switches and open others.
for LOW Intensity - close even numbered switches and open all others.

Switches 1 and 2 are for port 0; switches 3 and 4 are for port 1;
Switches 5 and 6 are for port 2 and switches 7 and 8 are for port 3.

MULTIPLEX CHANNEL CONTROLLER

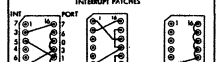
DISABLE ENABLE PORT 7 SWITCH*

S1 DISABLES ACK, END & REQ LINES TO MUX PORT 7 (KEYBOARD CHANNEL). SET S1 SWITCHES 1, 2 AND 4 ON FOR THE MUX THAT HAS KEYBOARDS AND OFF FOR MUX(S) THAT DOES NOT HAVE KEYBOARDS.



*SOME MULTIPLEX CONTROLLERS HAVE NO SWITCHES. THESE ARE NOT ALWAYS INTERCHANGEABLE. REFER TO FIELD BULLETIN CM-084-1.

MULTIPLEX CHANNEL CONTROLLER INTERRUPT PATCHES



5921S3G66 — FOR MODEM INT LEVELS — FIRST MULTIPLEX CHANNEL CONTROLLER

5921S3G185 — FOR MODEM INT LEVEL 8

5921S3G68 — 2ND AND 3RD MULTIPLEX CHANNEL CONTROLLER

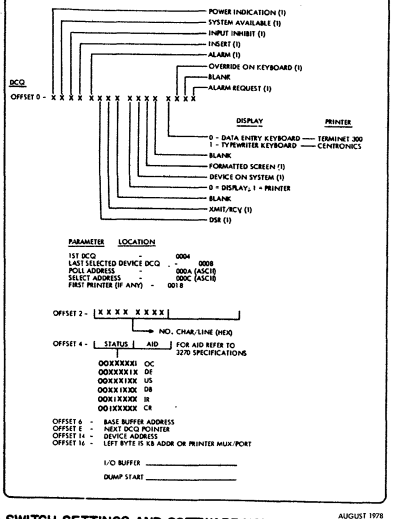
DEVICE ADDRESS AND INTERRUPT ASSIGNMENTS

DEVICE	MUX NO.	PORT NO.	INTERRUPT LEVEL
CASSETTE	0	0	2
KEYBOARDS	0	7	5
MODEMS SEND REC	0 0	2 1	5 OR 8 5 OR 8
PRINTERS 1-4	0	3-6	2
PRINTERS 5-12	1	0-7	2
PRINTERS 13-20	2	0-7	2

MULTIPLEX CHANNEL CONTROLLER ADDRESS PATCH

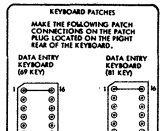
G2 BOARD LOCATION

FOR THIS MULTIPLEX CHANNEL ADDRESS	MAKE THESE PATCHES
ADDR 0	1 OR 4 TO 16
ADDR 1	1 OR 4 TO 12
ADDR 2	1 OR 4 TO 14
ADDR 3	1 OR 4 TO 10
ADDR 4	1 OR 4 TO 15
ADDR 5	1 OR 4 TO 11
ADDR 6	1 OR 4 TO 13
ADDR 7	1 OR 4 TO 9



KEYBOARD PATCHES

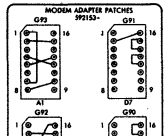
MAKE THE FOLLOWING PATCH CONNECTIONS ON THE PATCH PLUG LOCATED ON THE RIGHT REAR OF THE KEYBOARD.



5921S3G112 — 5921S3G144 — 5921S3G129 — 5921S3G111

MODEM ADAPTER PATCHES

5921S3-



Processing Unit and Terminal Address Assignments

Encode on Feature Board

Column 1
Use this column to find:
- Device Selection,
- Specific Poll,
- General Poll; and
- Fixed Return Addresses

Column 2
Use this column to find:
- PTS Selection Addresses

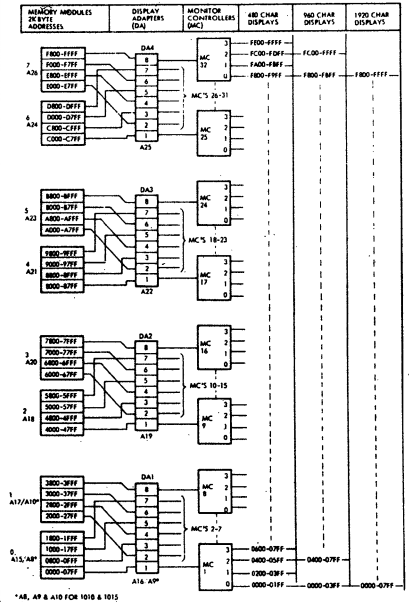
Processing Unit or Device Number	EBCDIC Hex	ASCII Hex	EBCDIC Hex	ASCII Hex
0	40	20	60	2D
1	C1	41	61	2F
2	C2	42	E2	53
3	C3	43	E3	54
4	C4	44	E4	55
5	C5	45	E5	56
6	C6	46	E6	57
7	C7	47	E7	58
8	C8	48	E8	59
9	C9	49	E9	5A
10	4A	5B	6A	5C
11	4B	2E	6B	2C
12	4C	3C	6C	25
13	4D	28	6D	5F
14	4E	2B	6E	3E
15	4F	21	6F	3F
16	50	26	F0	30
17	D1	4A	F1	31
18	D2	4B	F2	32
19	D3	4C	F3	33
20	D4	4D	F4	34
21	D5	4E	F5	35
22	D6	4F	F6	36
23	D7	50	F7	37
24	D8	51	F8	38
25	D9	52	F9	39
26	5A	5D	7A	3A
27	5B	24	7B	23
28	5C	2A	7C	40
29	5D	29	7D	27
30	5E	3B	7E	3D
31	5F	5E	7F	22

NOTE

I/O character address 79 is used as the device address to specify a General Poll operation.

PATCH AND SWITCH SETTINGS AND SOFTWARE NOTES FOR TRAVELERS DISC BACKUP 933403

DISPLAY CONNECTIONS AND MEMORY ASSIGNMENTS



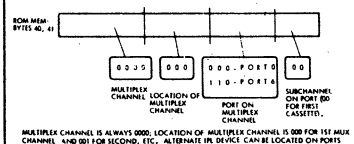
NOTES

ALL DISPLAYS ARE ASSIGNED FROM THE UPPERMOST MEMORY ADDRESS DOWN. IN A MIXED SYSTEM 1920 CH DISPLAYS ARE ASSIGNED BEFORE 480 CH DISPLAYS. ALSO THE STARTING MEMORY ADDRESSES ARE DETERMINED BY WHICH DISPLAY ADAPTERS ARE ASSIGNED TO 1920 CH AND 480 CH DISPLAYS (SEE C4 CONF. B, A). IF A SYSTEM IS MIXED OR DOES NOT FULLY LOAD ALL M.C.'s, PRINTER BUFFERS WILL BE ASSIGNED TO THE UNUSED AREAS. IN A MIXED ** SYSTEM PRINTERS ARE ASSIGNED AS FOLLOWS:

1 CENTRONICS - 1920 CH BUFFER
2 TERMINET - 1920 CH BUFFER
3 CENTRONICS - 480 CH BUFFER
4 TERMINET - 480 CH BUFFER

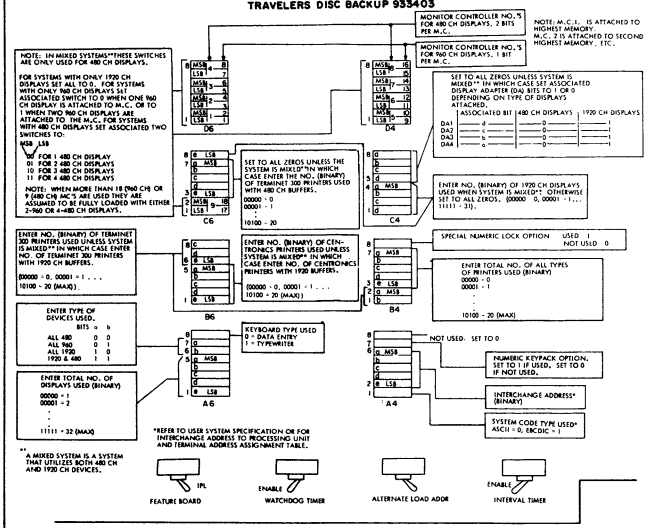
THE PROGRAM RESIDES IN LOWER MEMORY, NORMALLY IN MODULES A17/A16*, AND A15/A8*. PROGRAM MEMORY IS ASSIGNED FROM THE LOWEST ADDRESS UP. MEMORY MODULES ARE INSTALLED STARTING AT THE LOWEST MEMORY ADDRESS.

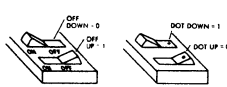
DEVICE ADDRESS ASSIGNMENTS

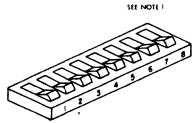


MULTIPLEX CHANNEL IS ALWAYS 0000. LOCATION OF MULTIPLEX CHANNEL IS 000 FOR 1ST MUX CHANNEL AND 001 FOR SECOND, ETC. ALTERNATE IPL DEVICE CAN BE LOCATED ON PORTS 0 (000) THROUGH 6 (110) AND ON SUBCHANNELS 0 (00) THROUGH 3 (11).

PTS-100 FEATURE BOARD 'A' CHIP SWITCH SETTINGS FOR TRAVELERS DISC BACKUP 933403

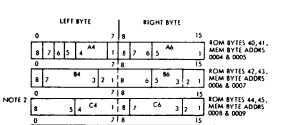






NOTES:

1. SOME SWITCHES ARE NUMBERED DIFFERENTLY BUT SWITCH LOCATIONS ARE THE SAME AS SHOWN ABOVE. ALSO SOME SWITCHES HAVE ON & OFF INSTEAD OF DOTS. a, b, c, d, ETC., IS THE ORDER OF BITS. SET ALL UNUSED SWITCHES TO 0.
2. THE 16 BITS IN EACH MEMORY WORD MUST NEVER BE ALL 1'S.



FOR BYTE FUNCTIONS AND SWITCHES SEE ABOVE

APPENDIX B

PTS-100 CHARACTER SET

APPENDIX B

PTS-100 CHARACTER SET

Symbol	Hollerith	Extended Code$_{10}$	ASCII$_8$	ASCII HEX 8 Bit	ASCII HEX 7 Bit
@	0-2-8	50	300	C0	40
A	12-1	132	301	C1	41
B	12-2	130	302	C2	42
C	12-3	134	303	C3	43
D	12-4	129	304	C4	44
E	12-5	133	305	C5	45
F	12-6	131	306	C6	46
G	12-7	135	307	C7	47
H	12-8	144	310	C8	48
I	12-9	136	311	C9	49
J	11-1	68	312	CA	4A
K	11-2	66	313	CB	4B
L	11-3	70	314	CC	4C
M	11-4	65	315	CD	4D
N	11-5	69	316	CE	4E
O	11-6	67	317	CF	4F
P	11-7	71	320	D0	50
Q	11-8	80	321	D1	51
R	11-9	72	322	D2	52
S	0-2	34	323	D3	53
T	0-3	38	324	D4	54
U	0-4	33	325	D5	55
V	0-5	37	326	D6	56
W	0-6	35	327	D7	57
X	0-7	39	330	D8	58
Y	0-8	48	331	D9	59
Z	0-9	40	332	DA	5A
[	12-5-8	149	333	DB	5B
	0-6-8	51	334	DC	5C
]	11-5-8	85	335	DD	5D
	7-8	23	336	DE	5E
	2-8	18	337	DF	5F
blank	No punch	00	240	A0	20
!	11-2-8	82	241	A1	21
"	0-5-8	53	242	A2	22
#	0-7-8	55	243	A3	23
$	11-3-8	86	244	A4	24
%	11-7-8	87	245	A5	25
&	12-7-8	151	246	A6	26
'	4-8	17	247	A7	27
(	0-4-8	49	250	A8	28
)	12-4-8	145	251	A9	29
*	11-4-8	81	252	AA	2A
+	12	128	253	AB	2B
,	0-3-8	54	254	AC	2C
-	11	64	255	AD	2D
.	12-3-8	150	256	AE	2E
/	0-1	36	257	AF	2F
0	0	32	260	B0	30
1	1	4	261	B1	31
2	2	2	262	B2	32
3	3	6	263	B3	33
4	4	1	264	B4	34
5	5	5	265	B5	35
6	6	3	266	B6	36
7	7	7	267	B7	37
8	8	16	270	B8	38
9	9	8	271	B9	39

PTS-100 CHARACTER SET (cont)

Symbol	Hollerith	Extended Code$_{10}$	ASCII$_8$	ASCII HEX 8 Bit	ASCII HEX 7 Bit
:	5-8	21	272	BA	3A
;	11-6-8	83	273	BB	3B
<	12-6-8	147	274	BC	3C
=	3-8	22	275	BD	3D
>	6-8	19	276	BE	3E
?	12-2-8	146	277	BF	3F
NUL	12-9-1	140	200	80	00
SOH	12-9-2	138	201	81	01
STX	12-9-3	142	202	82	02
ETX	12-9-4	137	203	83	03
EOT	12-9-5	141	204	84	04
ENQ	12-9-6	139	205	85	05
ACK	12-9-7	143	206	86	06
BEL	11-9-1	76	207	87	07
BS	11-9-2	74	210	88	08
HT	11-9-3	78	211	89	09
LF	11-9-4	73	212	8A	0A
VT	11-9-5	77	213	8B	0B
FF	11-9-6	75	214	8C	0C
CR	11-9-7	79	215	8D	0D
SO	0-9-1	44	216	8E	0E
SI	0-9-2	42	217	8F	0F
DLE	0-9-3	46	220	90	10
DC1	0-9-4	41	221	91	11
DC2	0-9-5	45	222	92	12
DC3	0-9-6	43	223	93	13
DC4	0-9-7	47	224	94	14
NAK	12-0-8	176	225	95	15
SYN	12-1-8	148	226	96	16
ETB	11-0-8	112	227	97	17
CAN	11-1-8	84	230	98	18
EM	0-1-8	52	231	99	19
SUB	12-8-9	152	232	9A	1A
ESC	11-8-9	88	233	9B	1B
FS	0-8-9	56	234	9C	1C
CS	8-9	24	235	9D	1D
RS	9-1	12	236	9E	1E
US	9-2	10	237	9F	1F
DEL	1-8	20	377	FF	7F

APPENDIX C
MODEM EIA STANDARD
RS-232-C
CIRCUIT LINE DESCRIPTIONS

APPENDIX C

MODEM EIA STANDARD RS-232-C CIRCUIT LINE DESCRIPTIONS

C-1. GENERAL INTERCHANGE SIGNAL CHARACTERISTICS

1. During the transmission of data, the marking condition is used to denote the binary state ONE and the spacing condition is used to denote the binary state ZERO.

2. For timing and control interchange circuits, a function is considered ON when the voltage on the interchange circuit is more positive than plus three volts with respect to circuit AB, and is considered OFF when the voltage is more negative than minus three volts with respect to circuit AB.

Notation	Interchange Voltage	
	Negative 3 v	Positive 3 v
Binary State	1	0
Signal Condition	Marking	Spacing
Function	OFF	ON

3. Interchange circuits transferring timing signals across the interface point hold ON and OFF conditions for nominally equal periods of time. During periods when timing information is not provided on a timing interchange circuit, this interchange circuit is clamped in the OFF condition.

C-2. INTERCHANGE CIRCUITS

The interchange circuits are listed Figure C-1 and defined in the following paragraphs.

C-3. INTERFACE CIRCUIT DEFINITIONS

1. Circuit AA - Protective Ground

   This conductor is electrically bonded to the machine or equipment frame. It may be further connected to external grounds as required by applicable regulations.

2. Circuit AB - Signal Ground or Common Return

   This conductor establishes the common ground reference potential for all interchange circuits except Circuit AA (Protective Ground).

Pin Number	Interchange Circuit	C.C.I.T.T. Equivalent	Description	Gnd	Data		Control		Timing	
					From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
1	AA	101	Protective Ground	X						
7	AB	102	Signal Ground/Common Return	X						
2	BA	103	Transmitted Data	-		X				
3	BB	104	Received Data		X					
4	CA	105	Request to Send					X		
5	CB	106	Clear to Send				X			
6	CC	107	Data Set Ready				X			
20	CD	108.2	Data Terminal Ready					X		
22	CE	125	Ring Indicator				X			
8	CF	109	Received Line Signal Detector				X			
21	CG	110	Signal Quality Detector				X			
23	CH	111	Data Signal Rate Selector (DTE)					X		
	CI	112	Data Signal Rate Selector (DCE)				X			
24	DA	113	Transmitter Signal Element Timing (DTE)							X
15	DB	114	Transmitter Signal Element Timing (DCE)						X	
17	DD	115	Receiver Signal Element Timing (DCE)						X	
14	SBA	118	Secondary Transmitted Data			X				
16	SBB	119	Secondary Received Data		X					
19	SCA	120	Secondary Request to Send					X		
13	SCB	121	Secondary Clear to Send				X			
12	SCF	122	Secondary Rec'd Line Signal Detector				X			

DCE - Data Communications Equipment

Figure C-1. Interchange Circuit Listing

Within the data communication equipment, this circuit is brought to one point, and it is possible to connect this point to Circuit AA by means of a wire strap inside the equipment. This wire strap can be connected or removed at installation, as may be required to meet applicable regulations or to minimize the introduction of noise into electronic circuitry.

3. Circuit BA - Transmitted Data

Signals on this circuit are generated by the data terminal equipment and are transferred to the local transmitting signal converter for transmission of data to remote data terminal equipment.

The data terminal equipment will hold Circuit BA (Transmitted Data) in marking condition during intervals between characters or words, and at all times when no data are being transmitted.

In all systems, the data terminal equipment will not transmit data unless an ON condition is present on all the following four circuits, where implemented.

Circuit CA (Request to Send)
Circuit CB (Clear to Send)
Circuit CC (Data Set Ready)
Circuit CD (Data Terminal Ready)

All data signals are transmitted across the interface on interchange circuit BA (Transmitted Data) during the time an ON condition is maintained on all the above four circuits, where implemented.

4. Circuit BB - Received Data

Signals on this circuit are generated by the receiving signal converter in response to data signals received from remote data terminal equipment via the remote transmitting signal converter. Circuit BB (Received Data) is held in the binary ONE (Marking) condition at all times when Circuit CF (Received Line Signal Detector) is in the OFF condition.

On a half duplex channel, Circuit BB is held in the Binary One (Marking) condition when Circuit CA (Request to Send) is in the ON condition and for a brief interval following the ON to OFF transition of Circuit CA to allow for the completion of transmission (see Circuit BA - Transmitted Data) and the decay of line reflections.

5. Circuit CA - Request to Send

This circuit is used to condition the local data communication equipment for data transmission and, on a half duplex channel, to control the direction of data transmission of the local data communication equipment.

On one way only channels or duplex channels, the ON condition maintains the data communication equipment in the transmit mode. The OFF condition maintains the data communication equipment in a non-transmit mode.

On a half duplex channel, the ON condition maintains the data communication equipment in the transmit mode and inhibits the receive mode. The OFF condition maintains the data communication equipment in the receive mode.

A transition from OFF to ON instructs the data communication equipment to enter the transmit mode. The data communication equipment responds by taking such action as may be necessary and indicates completion of such actions by turning ON Circuit CB (Clear to Send), thereby indicating to the data terminal equipment that data may be transferred across the interface point on interchange Circuit BA (Transmitted Data).

A transition from ON to OFF instructs the data communication equipment to complete the transmission of all data which was previously transferred across the interface point on interchange Circuit BA and then assume a non-transmit mode or a receive mode as appropriate. The data communication equipment responds to this instruction by turning OFF Circuit CB (Clear to Send) when it is prepared to again respond to a subsequent ON condition of Circuit CA.

NOTE

A non-transmit mode does not imply that all line signals have been removed from the communication channel.

When Circuit CA is turned OFF, it is not to be turned ON again until Circuit CB has been turned OFF by the data communication equipment.

An ON condition is required on Circuit CA as well as on Circuit CB, Circuit CC (Data Set Ready) and, where implemented,

Circuit CD (Data Terminal Ready) whenever the data terminal equipment transfers data across the interface on interchange Circuit BA.

It is permissible to turn Circuit CA ON at any time when Circuit CB is OFF regardless of the condition of any other interchange circuit.

6. Circuit CB - Clear to Send

Signals on this circuit are generated by the data communication equipment to indicate whether or not the data set is ready to transmit data.

The ON condition together with the ON condition on interchange circuits CA, CC and, where implemented, CD, is an indication to the data terminal equipment that signals presented on Circuit BA (Transmitted Data) will be transmitted to the communication channel.

The OFF condition is an indication to the data terminal equipment that it should not transfer data across the interface on interchange Circuit BA.

The ON condition of Circuit CB is a response to the occurrence of a simultaneous ON condition on Circuits CC (Data Set Ready) and Circuit CA (Request to Send), delayed as may be appropriate to the data communication equipment for establishing a data communication channel (including the removal of the MARK HOLD clamp from the Received Data interchange circuit of the remote data set) to a remote data terminal equipment.

Where Circuit CA (Request to Send) is not implemented in the data communication equipment with transmitting capability, Circuit CA is assumed to be in the ON condition at all times, and Circuit CB responds accordingly.

7. Circuit CC - Data Set Ready

Signals on this circuit are used to indicate the status of the local data set.

The ON condition on this circuit is presented to indicate that -

a. the local data communication equipment is connected to a communication channel ("OFF HOOK" in switched service),

b. the local data communication equipment is not in test (local or remote), talk (alternate voice), or dial mode,

c. the local data communication equipment has completed, where applicable: any timing functions required by the switching system to complete call establishment, and; the transmission of any discreet answer tone, the duration of which is controlled solely by the local data set.

Where the local data communication equipment does not transmit an answer tone, or where the duration of the answer tone is controlled by some action of the remote data set, the ON condition is presented as soon as the other above conditions are satisfied.

This circuit is used only to indicate the status of the local data set. The ON condition should not be interpreted as either an indication that a communication channel has been established to a remote data station or the status of any remote station equipment.

The OFF condition appears at all other times and is an indication that the data terminal equipment is to disregard signals appearing on any other interchange circuit with the exception of Circuit CE (Ring Indicator). The OFF condition does not impair the operation of Circuit CE or Circuit CD (Data Terminal Ready).

When the OFF condition occurs during the progress of a call before Circuit CD is turned OFF, the data terminal equipment interprets this as a lost or aborted connection and takes action to terminate the call. Any subsequent ON condition on Circuit CC is considered a new call.

When the data set is used in conjunction with Automatic Calling Equipment (ACE), the OFF to ON transition of Circuit CC is not an indication that the ACE has relinquished control of the communication channel to the data set.

NOTE

If a data call is interrupted by alternate voice communication, Circuit CC will be in the OFF condition during the time that voice communication is in progress. The transmission or reception of the signals required to condition the communication channel or data communication equipment in response to the ON condition of interchange Circuit CA (Request to Send) of the transmitting data terminal equipment will take place after Circuit CC comes ON, but prior to the ON condition on Circuit CB (Clear to Send) or Circuit CF (Received Line Signal Detector).

8. Circuit CD - Data Terminal Ready

Signals on this circuit are used to control switching of the data communication equipment to the communication channel. The ON condition prepares the data communication equipment to be connected to the communication channel and maintains the connection established by external means (e.g., manual call origination, manual answering or automatic call origination).

When the station is equipped for automatic answering of received calls and is in the automatic answering mode, connection to the line occurs only in response to a combination of a ringing signal and the ON condition of Circuit CD (Data Terminal Ready): however, the data terminal equipment is normally permitted to present the ON condition on Circuit CD whenever it is ready to transmit or receive data, except as indicated below.

The OFF condition causes the data communication equipment to be removed from the communication channel following the completion of any "in process" transmission. See Circuit BA (Transmitted Data). The OFF condition will not disable the operation of Circuit CE (Ring Indicator).

In switched network applications, when circuit CD is turned OFF, it is not turned ON again until Circuit CC (Data Set Ready) is turned OFF by the data communication equipment.

9. Circuit CE - Ring Indicator

The ON condition of this circuit indicates that a ringing signal is being received on the communication channel.

The ON condition appears approximately coincident with the ON segment of the ringing cycle (during rings) on the communication channel.

The OFF condition is maintained during the OFF segment of the ringing cycle (between "rings") and at all other times when ringing is not being received. The operation of this circuit is not disabled by the OFF condition on Circuit CD (Data Terminal Ready).

10. Circuit CF - Received Line Signal Detector

The ON condition on this circuit is presented when the data communication equipment is receiving a signal which meets its

suitability criteria. These criteria are established by the data communication equipment manufacturer.

The OFF condition indicates that no signal is being received or that the received signal is unsuitable for demodulation.

The OFF condition of Circuit CF (Received Line Signal Detector) causes Circuit BB (Received Data) to be clamped to the Binary One (Marking) condition.

The indications on this circuit follow the actual onset or loss of signal by appropriate guard delays.

On half duplex channels, Circuit CF is held in the OFF condition whenever Circuit CA (Request to Send) is in the ON condition and for a brief interval of time following the ON to OFF transition of Circuit CA. (See Circuit BB.)

11. Circuit CG - Signal Quality Detector

Signals on this circuit are used to indicate whether or not there is a high probability of an error in the received data.

An ON condition is maintained whenever there is no reason to believe that an error has occurred.

An OFF condition indicates that there is a high probability of an error. It may, in some instances, be used to call automatically for the retransmission of the previously transmitted data signal. Preferably the response of this circuit is such as to permit identification of individual questionable signal elements on Circuit BB (Received Data).

12. Circuit CH - Data Signal Rate Selector (DTE Source)

Signals on this circuit are used to select between the two data signaling rates in the case of dual rate synchronous data sets or the two ranges of data signaling rates in the case of dual range non-synchronous data sets.

An ON condition selects the higher data signaling rate or range of rates.

The rate of timing signals, if included in the interface, is controlled by this circuit as may be appropriate.

13. Circuit CI - Data Signal Rate Selector (DCE Source)

Signals on this circuit are used to select between the two data signaling rates in the case of dual rate synchronous data sets or the two ranges of data signaling rates in the case of dual range non-synchronous data sets.

An ON condition selects the higher data signaling rate or range of rates.

The rate of timing signals, if included in the interface, is controlled by this circuit as may be appropriate.

14. Circuit DA - Transmitter Signal Element Timing (DTE Source)

Signals on this circuit are used to provide the transmitting signal converter with signal element timing information.

The ON to OFF transition nominally indicates the center of each signal element on Circuit BA (Transmitted Data). When Circuit DA is implemented in the DTE, the DTE normally provides timing information on this circuit whenever the DTE is in a POWER ON condition. It is permissible for the DTE to withhold timing information on this circuit for short periods provided Circuit CA (Request to Send) is in the OFF condition. (For example, the temporary withholding of timing information may be necessary in performing maintenance tests within the DTE.)

15. Circuit DB - Transmitter Signal Element Timing (DCE Source)

Signals on this circuit are used to provide the data terminal equipment with signal element timing information. The data terminal equipment provides a data signal on Circuit BA (Transmitted Data) in which the transitions between signal elements nominally occur at the time of the transitions from OFF to ON condition of the signal on Circuit DB. When Circuit DB is implemented in the DCE, the DCE normally provides timing information on this circuit whenever the DCE is in a POWER ON condition. It is permissible for the DCE to withhold timing information on this circuit for short periods provided Circuit CC (Data Set Ready) is in the OFF condition. (For example, the withholding of timing information may be necessary in performing maintenance tests within the DCE.)

16. Circuit DD - Receiver Signal Element Timing (DCE Source)

Signals on this circuit are used to provide the data terminal equipment with received signal element timing information. The transition from ON to OFF condition nominally indicates the center of each signal element on Circuit BB (Received Data). Timing information on Circuit DD is provided at all times when Circuit CF (Received Line Signal Detector) is in the ON condition. It may, but need not, be present following the ON to OFF transition of Circuit CF (see C-1, subsection 3).

17. Circuit SBA - Secondary Transmitted Data

This circuit is equivalent to Circuit BA (Transmitted Data) except that it is used to transmit data via the secondary channel.

Signals on this circuit are generated by the data terminal equipment and are connected to the local secondary channel transmitting signal converter for transmission of data to remote data terminal equipment.

The data terminal equipment holds Circuit SBA (Secondary Transmitted Data) in marking condition during intervals between characters or words and at all times when no data are being transmitted.

In all systems, the data terminal equipment does not transmit data on the secondary channel unless an ON condition is present on all the following four circuits, where implemented:

Circuit SCA - Secondary Request to Send
Circuit SCB - Secondary Clear to Send
Circuit CC - Data Set Ready
Circuit CD - Data Terminal Ready

All data signals that are transmitted across the interface on interchange Circuit SBA during the time when the above conditions are satisfied are transmitted to the communication channel.

When the secondary channel is usable only for circuit assurance or to interrupt the flow of data in the primary channel (less than 10 baud capability), Circuit SBA (Secondary Transmitted Data) is normally not provided, and the channel carrier is turned ON or OFF by means of Circuit SCA (Secondary Request to Send). Carrier OFF is interpreted as an "Interrupt" condition.

18. Circuit SBB - Secondary Received Data

This circuit is equivalent to Circuit BB (Received Data) except that it is used to receive data on the secondary channel.

When the secondary channel is usable only for circuit assurance or to interrupt the flow of data in the primary channel, Circuit SBB is normally not provided. See interchange Circuit SCF (Secondary Received Line Signal Detector).

19. Circuit SCA - Secondary Request to Send

This circuit is equivalent to Circuit CA (Request to Send) except that it requests the establishment of the secondary channel instead of requesting the establishment of the primary data channel.

Where the secondary channel is used as a backward channel, the ON condition of Circuit CA (Request to Send) disables Circuit SCA and it is not possible to condition the secondary channel transmitting signal converter to transmit during any time interval when the primary channel transmitting signal converter is so conditioned. Where system considerations dictate that one or the other of the two channels be in transmit mode at all times but never both simultaneously, this can be accomplished by permanently applying an ON condition to Circuit SCA (Secondary Request to Send) and controlling both the primary and secondary channels, in complementary fashion, by means of Circuit CA (Request to Send). Alternatively, in this case, Circuit SCB need not be implemented in the interface.

When the secondary channel is usable only for circuit assurance or to interrupt the flow of data in the primary data channel, Circuit SCA serves to turn ON the secondary channel unmodulated carrier. The OFF condition of Circuit SCA turns OFF the secondary channel carrier and thereby signals an interrupt condition at the remote end of the communication channel.

20. Circuit SCB - Secondary Clear to Send

This circuit is equivalent to Circuit CB (Clear to Send), except that it indicates the availability of the secondary channel instead of indicating the availability of the primary channel. This circuit is not provided where the secondary channel is usable only as a circuit assurance or an interrupt channel.

21. Circuit SCF - Secondary Received Line Signal Detector

This circuit is equivalent to Circuit CF (Received Line Signal Detector) except that it indicates the proper reception of the secondary channel line signal instead of indicating the proper reception of a primary channel received line signal.

Where the secondary channel is usable only as a circuit assurance or an interrupt channel (see Circuit SCA, Secondary Request to Send), Circuit SCF is used to indicate the circuit assurance status or to signal the interrupt. The ON condition indicates circuit assurance or a non-interrupt condition. The OFF condition indicates circuit failure (no assurance) or the interrupt condition.

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