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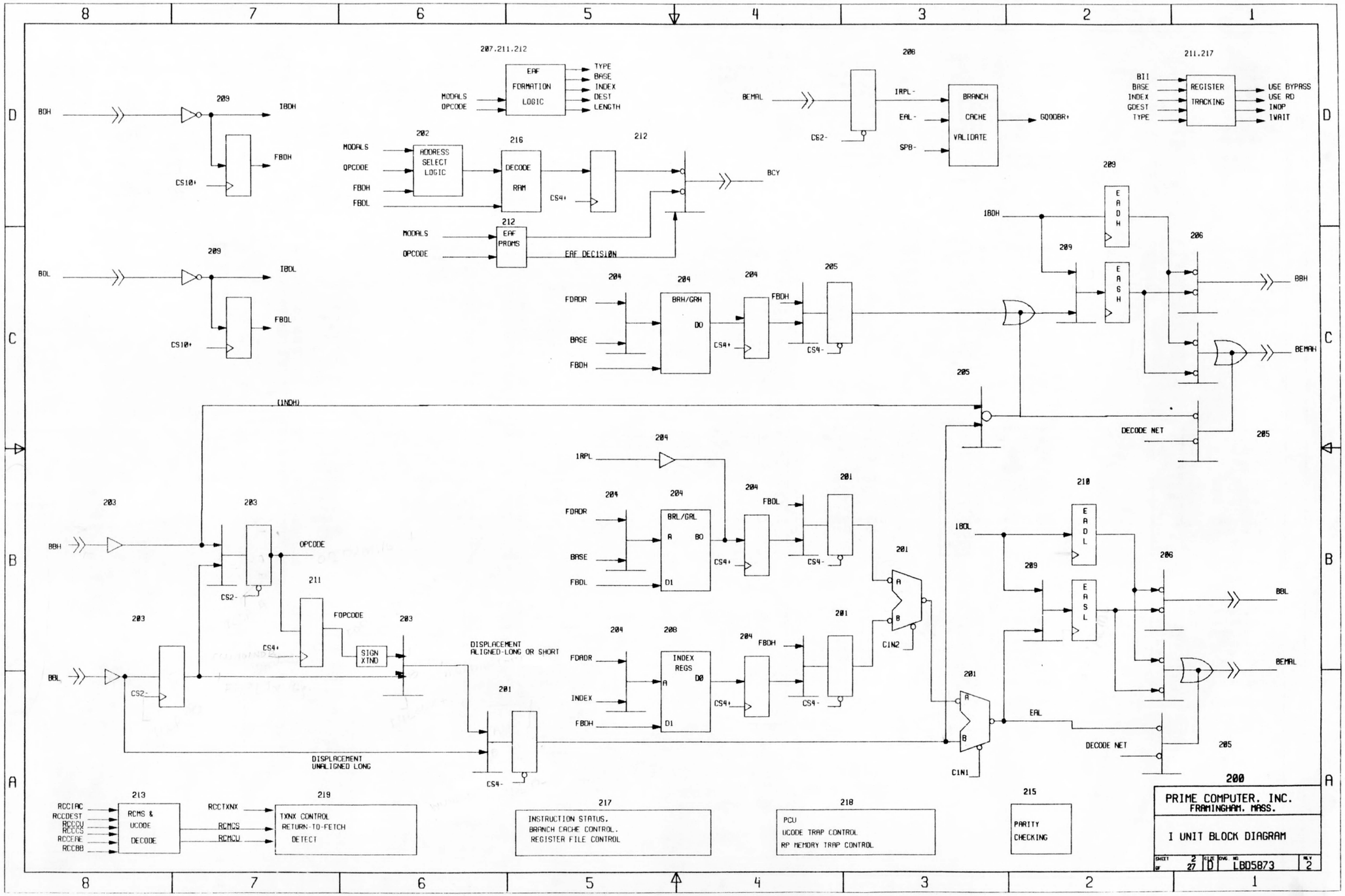
300-CS
400-C
500-FI
600-FR
700-

PRIME COMPUTER, INC.
9950 LBD SET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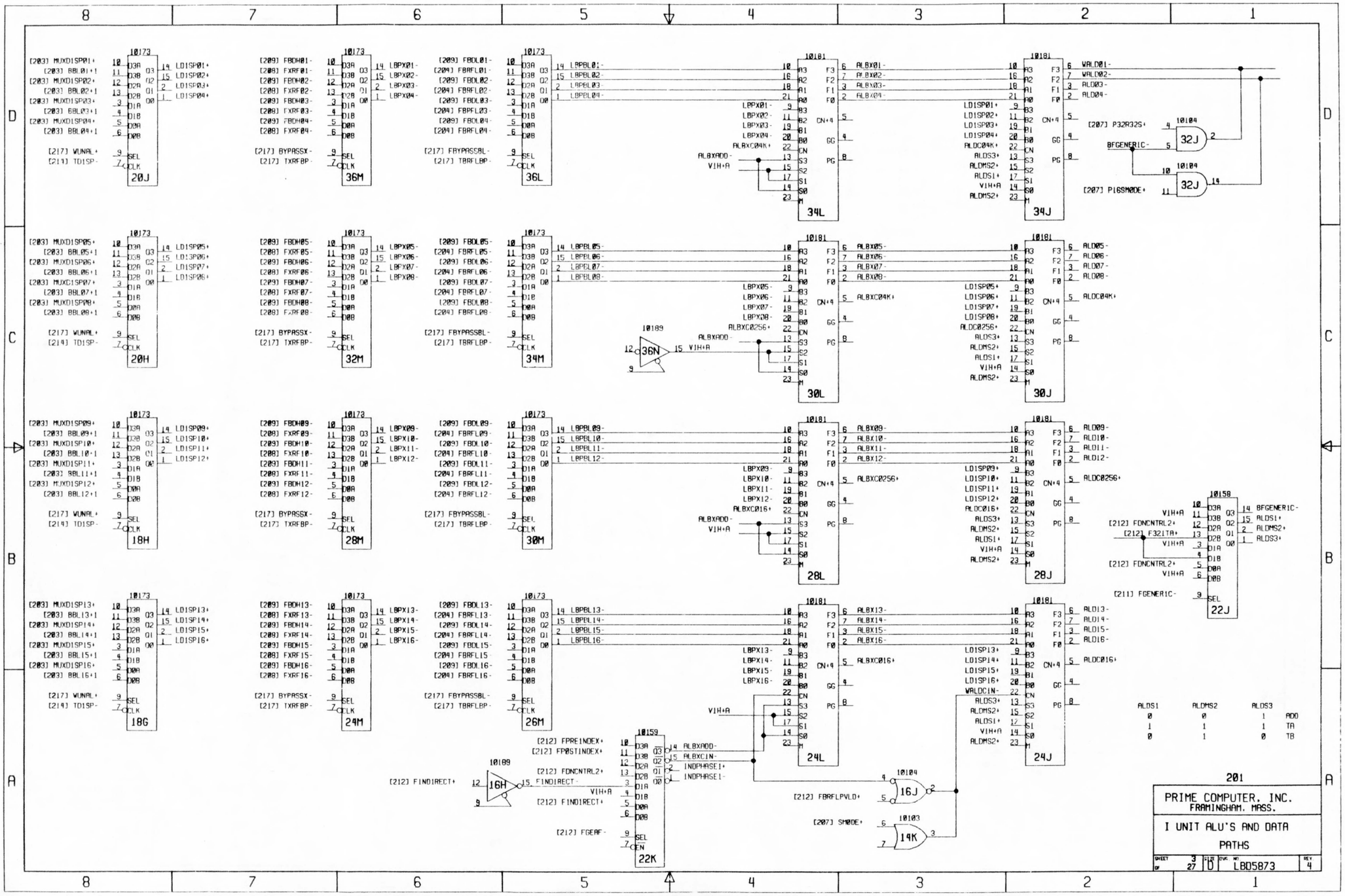
EAF FORMATION LOGIC
MODALS
OPCODE
TYPE
BASE
INDEX
DEST
LENGTH
208
BEMRL
C62-
IRPL-
EAL-
SPB-
BRANCH CACHE VALIDATE
GOODBR+
211.217
BII
BASE
INDEX
GDEST
TYPE
REGISTER TRACKING
USE BYPASS
USE RD
INDP
IWAIT
209
BDH
IBDH
FBDH
CS10+
202
ADDRESS SELECT LOGIC
216
DECODE RAM
212
CS4+
BCY
FBDH
FBDL
212
EAF PROMS
EAF DECISION
BDL
IBDL
FBDL
CS10+
204
FDADR
BASE
FBDH
BRH/GRH
DO
CS4+
CS4-
205
206
EADH
EAGH
IBDH
BBH
BEMAH
(INDH)
DECODE NET
IRPL
BRL/GRL
A
B0
D1
FBDL
201
EADL
EASL
IBDL
BBL
BEMRL
203
BBH
OPCODE
CS2-
211
FOPCODE
SIGN XTND
BBL
CS2-
CS4+
DISPLACEMENT ALIGNED-LONG OR SHORT
DISPLACEMENT UNALIGNED LONG
INDEX REGS
D0
INDEX
CIN2
CIN1
EAL
213
RCCIAC
RCCDEST
RCCCV
RCCCS
RCCEAE
RCCBB
RCMS & UCODE DECODE
RCCTXNX
RCMCS
RCMCV
219
TXNX CONTROL
RETURN-TO-FETCH
DETECT
217
INSTRUCTION STATUS,
BRANCH CACHE CONTROL,
REGISTER FILE CONTROL
218
PCU
UCODE TRAP CONTROL
RP MEMORY TRAP CONTROL
215
PARITY
CHECKING
200
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT BLOCK DIAGRAM
SHEET 2 OF 27
SIZE D
DWG NO LBD5873
REV 2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36M
36L
34L
34J
20H
32M
34M
30L
30J
18H
28M
30M
28L
28J
18G
24M
26M
24L
24J
22J
22K
16J
14K
36N
16H
32J
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT ALU'S AND DATA PATHS
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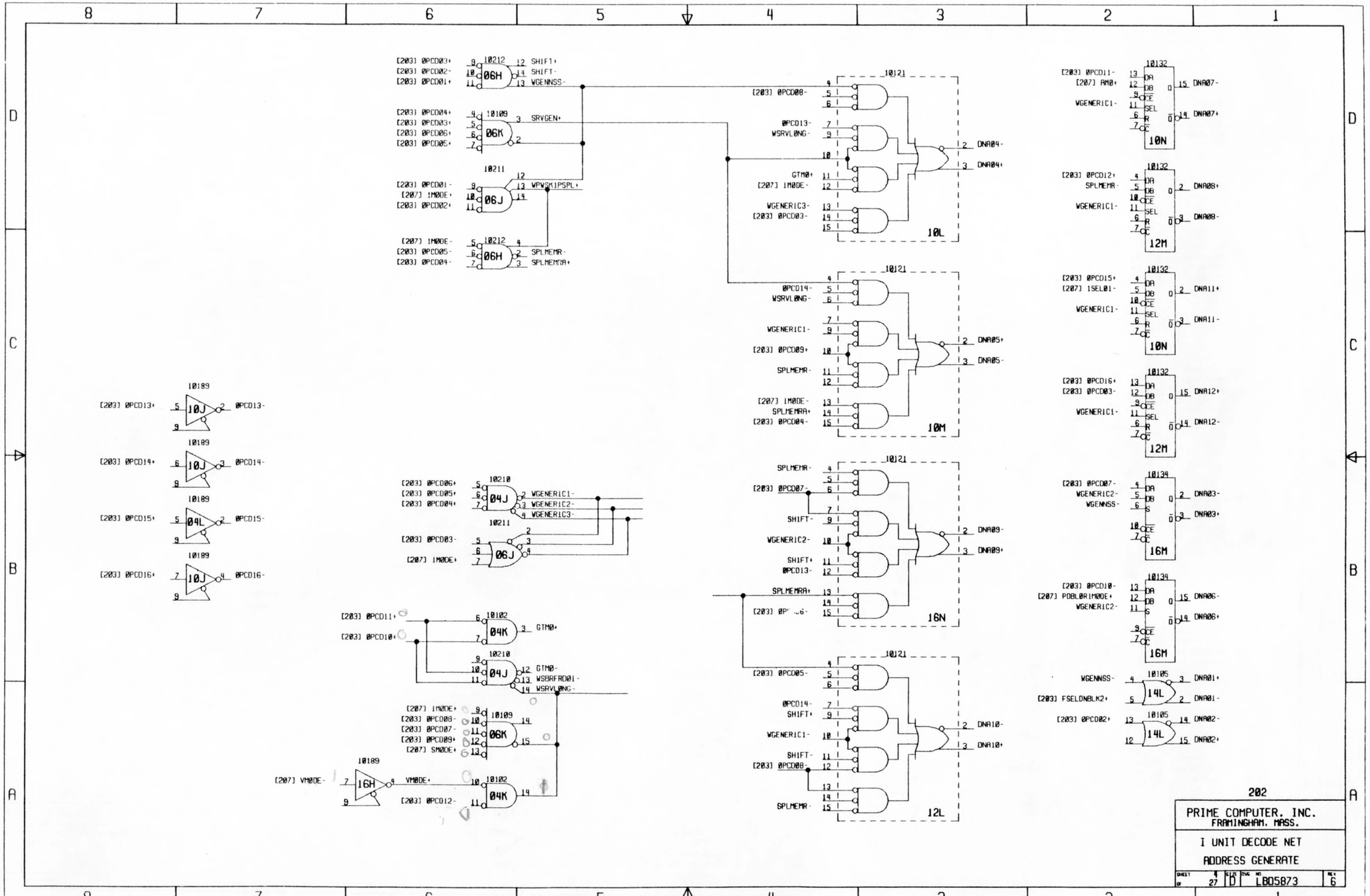
LBD5873
ALDS1 ALDMS2 ALDS3
0 0 1 ADD
1 1 1 TA
0 1 0 TB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4
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C
B
A
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06H
SHIFT+
SHIFT-
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10109
06K
SRVGEN+
10211
06J
WPWSK1PSPL+
SPLMEMR-
SPLMEMRA+
10121
10L
10M
16N
12L
DNA04-
DNA04+
DNA05+
DNA05-
DNA09-
DNA09+
DNA10-
DNA10+
10132
10N
12M
DNA07-
DNA07+
DNA08+
DNA08-
DNA11+
DNA11-
DNA12+
DNA12-
10134
16M
DNA03-
DNA03+
DNA06-
DNA06+
10105
14L
DNA01+
DNA01-
DNA02-
DNA02+
10189
10J
04L
16H
10210
04J
WGENERIC1-
WGENERIC2-
WGENERIC3-
10102
04K
GTM0+
GTM0-
WSBRFR001-
WSRVL0NG-
VM0DE+
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PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
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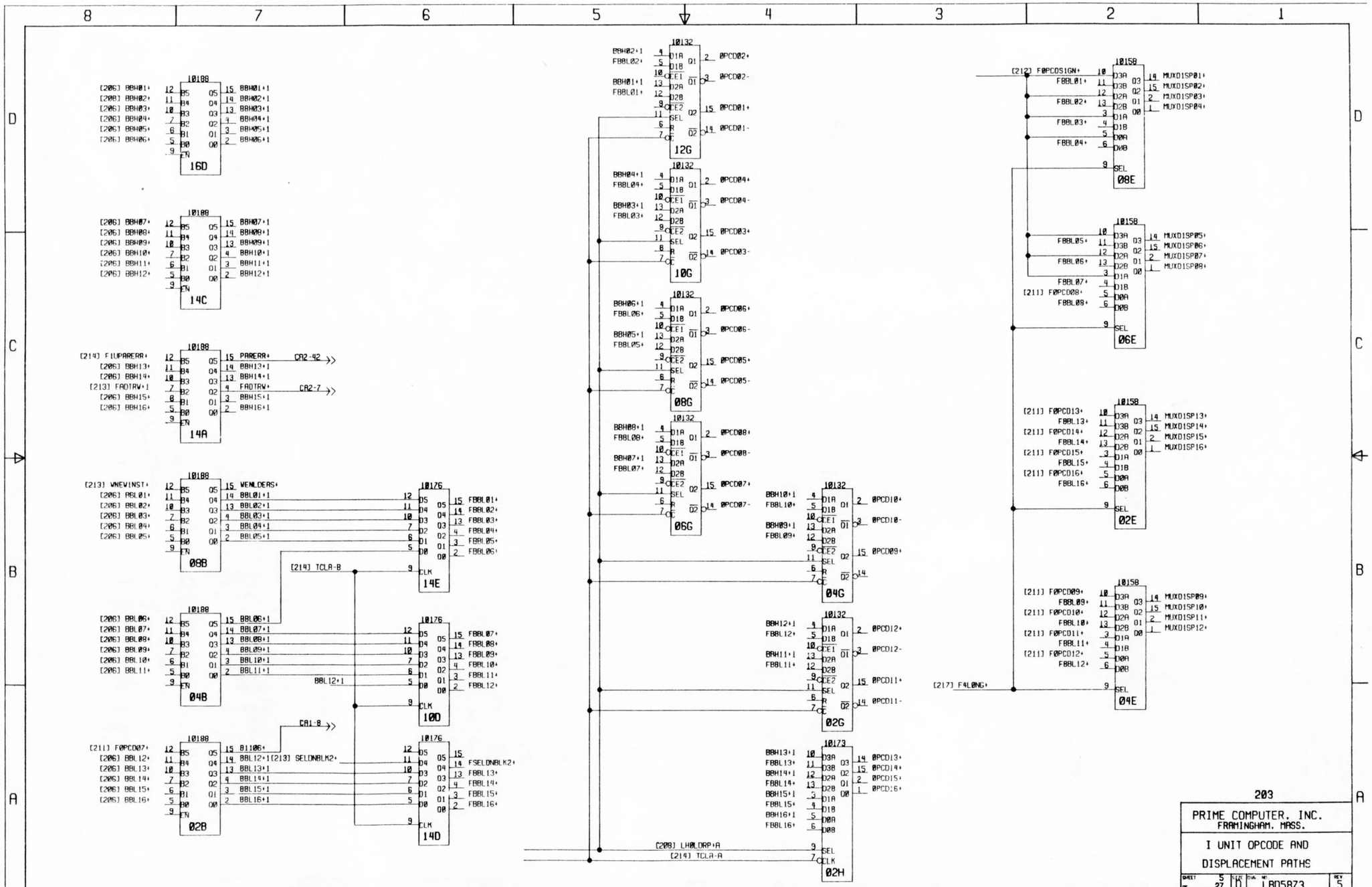
ADDRESS GENERATE
SHEET 27 OF
SIZE D
DWG NO LBD5873
REV 6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08B
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12G
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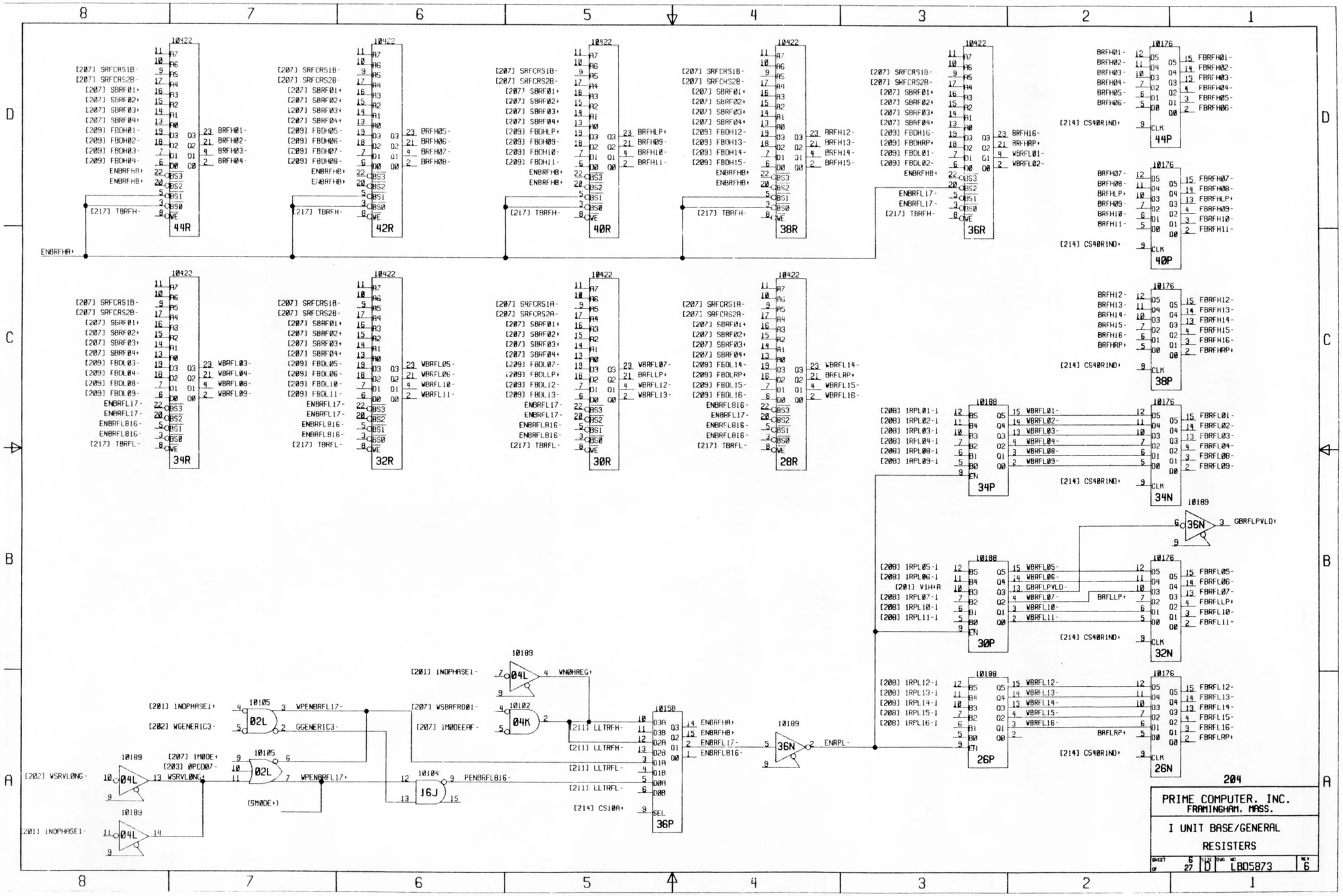
04G
02G
02H
08E
06E
02E
04E
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT OPCODE AND
DISPLACEMENT PATHS
203
SHEET 5 OF 27
SIZE D
DWG NO LBD5873
REV 5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34R
32R
30R
28R
10176
44P
40P
38P
34P
32P
30P
28P
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26N
32N
34N
36N
10188
10189
10105
10102
10104
10158
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BRFH03-
BRFH04-
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BRFH08-
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BRFHLP+
BRFH09-
BRFH10-
BRFH11-
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[209] FBDH15-
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BRFH13-
BRFH14-
BRFH15-
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BRFHRP+
WBRFL01-
WBRFL02-
ENBRFL17-
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BRFH14-
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BRFH16-
BRFHRP+
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WBRFL04-
WBRFL08-
WBRFL09-
WBRFL05-
WBRFL06-
WBRFL10-
WBRFL11-
WBRFL07-
BRFLLP+
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WBRFL15-
WBRFL16-
BRFLRP+
WBRFL18-
ENBRFL816-
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GBRFLPVLD+
GBRFLPVLD-
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WN0HREG+
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WPENBRFL17-
GGENERIC3-
[207] WSBRFRD01-
[207] IM0DEEAF-
[211] LLTRFH-
[211] LLTRFL-
ENBRFL17-
ENBRFL816-
ENRPL-
[202] WSRVL0NG-
WSRVL0NG+
[207] IM0DE+
[203] 0PCD07-
(SM0DE+)
WPENBRFL17+
PENBRFL816-
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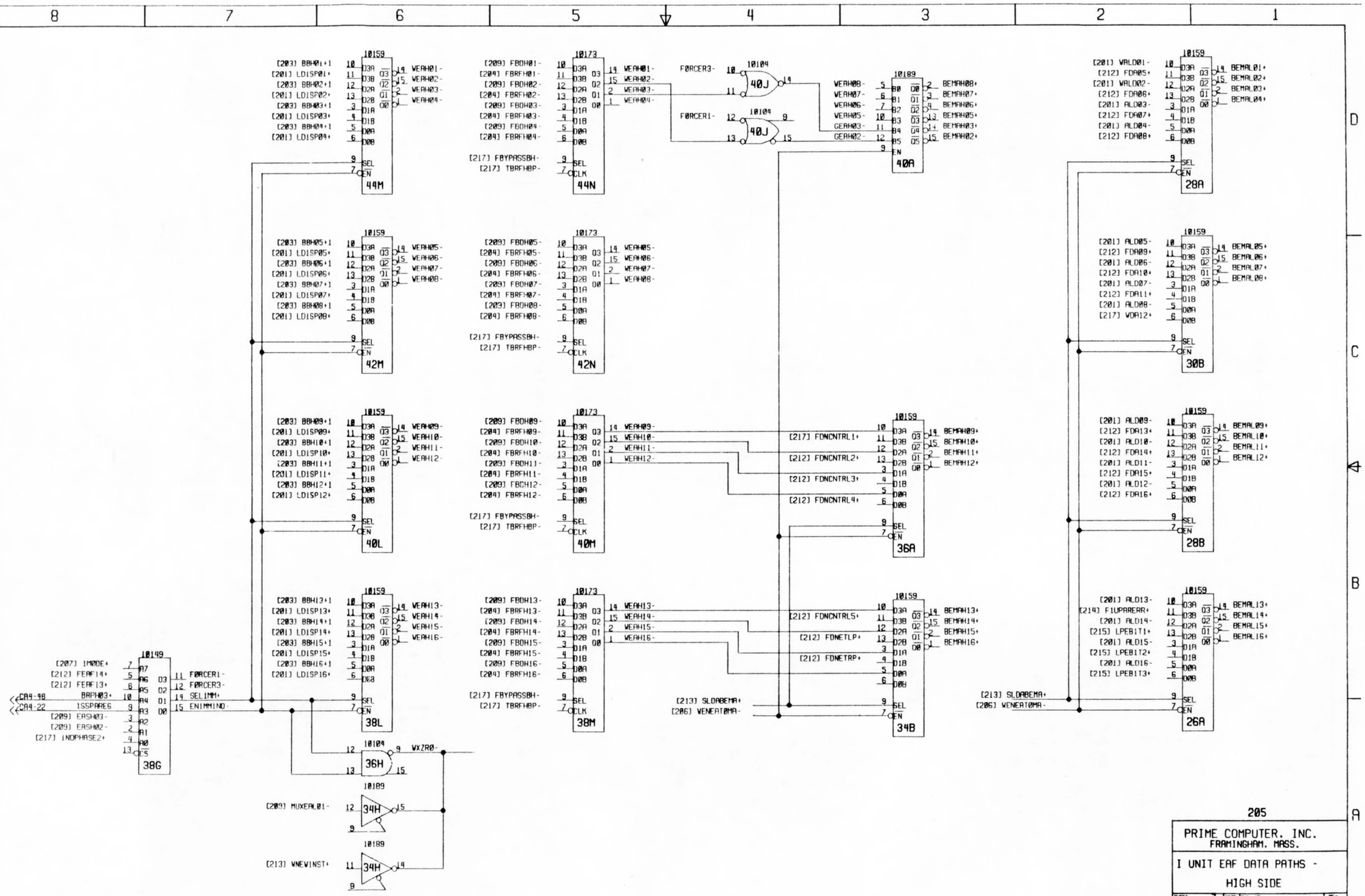
204
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT BASE/GENERAL
RESISTERS
SHEET OF 6 27
SIZE D
DWG NO LB05873
REV 6


205
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT EAF DATA PATHS -
HIGH SIDE
SHEET 7 OF 27
SIZE D
DWG NO LBD5873
REV 5
44M
44N
42M
42N
40L
40M
38L
38M
38G
40J
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36H
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34H
30B
28A
28B
26A
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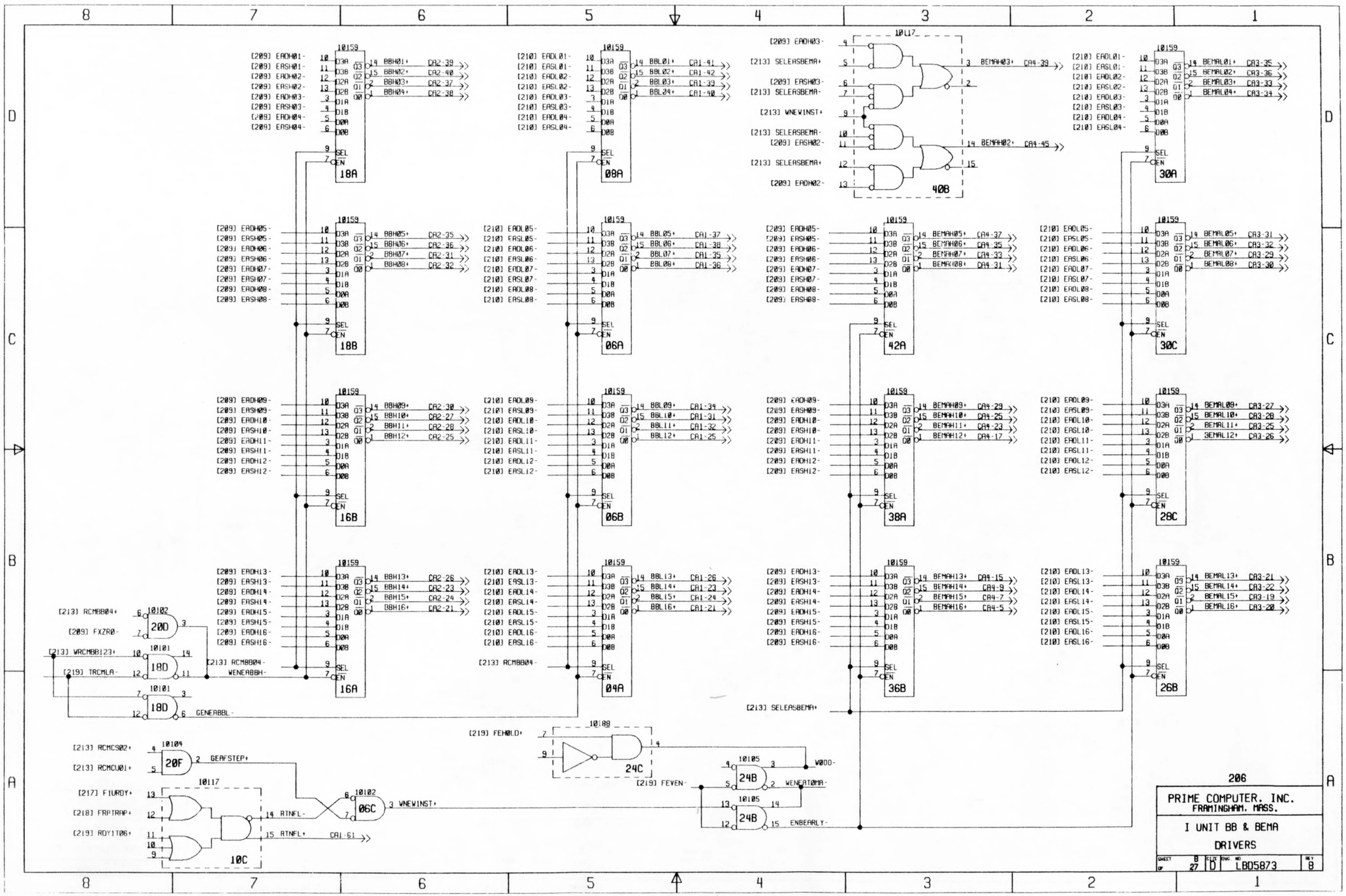
34B


206
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT BB & BEMA
DRIVERS
SHEET 27 OF 27
SIZE D
DWG NO LBD5873
REV B
18A
08A
40B
30A
18B
06A
42A
30C
16B
06B
38A
28C
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04A
36B
26B
20D
18D
18D
06C
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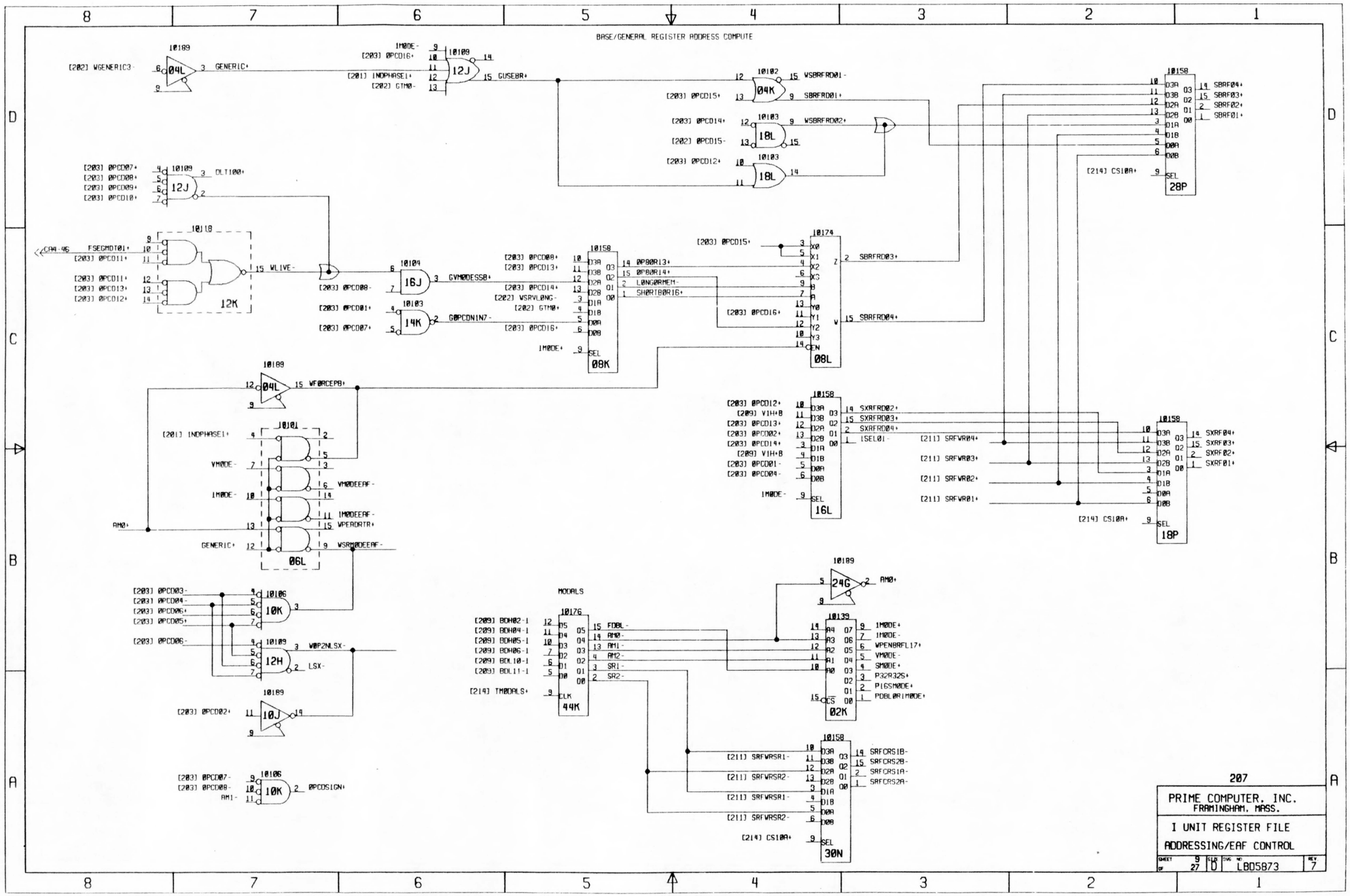
24B
24B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GENERIC+
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WSBRFRD01+
WSBRFRD02+
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DLT100+
CAA-06
FSEGMDT01+
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WLIVE-
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GVMØDESSB+
GØPCDN1N7-
[203] ØPCD08+
[203] ØPCD13+
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[202] VSRVLØNG-
[202] GTM0+
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IMØDE+
ØPBØR13+
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LØNGØRMEM-
SHØRTBØR16+
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SBRFRD04+
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WF0RCEPB+
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AMØ+
GENERIC+
VMØDEEAF-
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VSRMØDEEAF-
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SXRF01+
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LSX-
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MODALS
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AM2-
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SR2-
AM0+
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VMØDE-
SMØDE+
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PDBLØR1MØDE+
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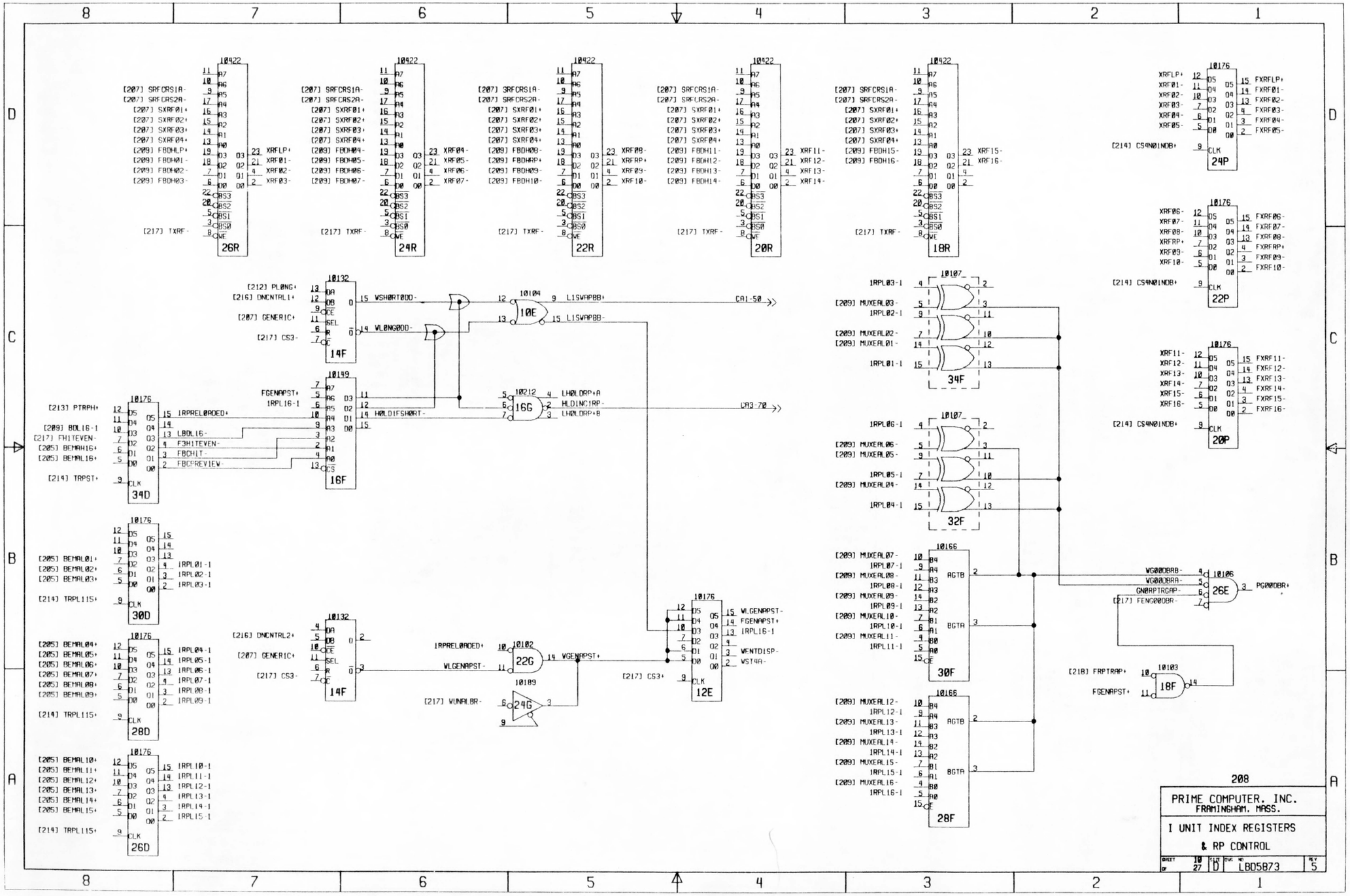
SRFCRS1A-
SRFCRS2A-
207
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT REGISTER FILE
ADDRESSING/EAF CONTROL
SHEET 9 OF 27
SIZE D
DWG NO LBD5873
REV 7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22R
20R
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[207] SXRF03+
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XRF02-
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XRF05-
XRF06-
XRF07-
XRF08-
XRFRP+
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14F
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[207] GENERIC+
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WL0NG0DD-
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L1SWAPBB-
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CA3-70
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FGENAPST+
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16G
H0LD1FSH0RT-
LH0LDRP+A
HLD1NC1RP-
LH0LDRP+B
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30D
28D
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FBDH1T-
FBCPREVIEV-
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1RPL02-1
1RPL03-1
1RPL04-1
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1RPL06-1
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FGENAPST+
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WST4A-
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WG00DBRA-
GN0BAPTRGAP-
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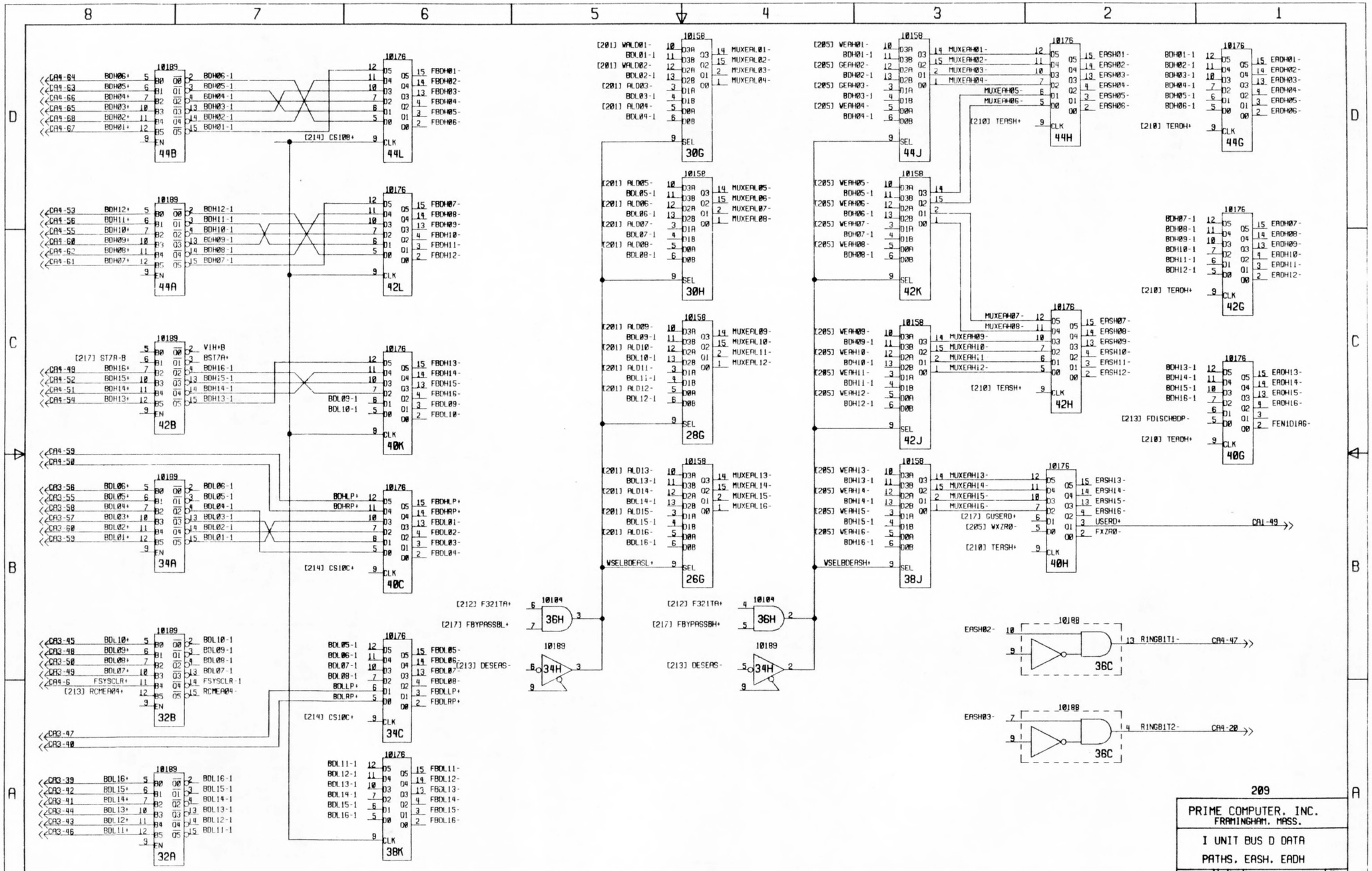
PG00DBR+
[218] FRPTRAP+
10103
18F
FGENAPST+
208
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT INDEX REGISTERS
& RP CONTROL
SHEET 10 OF 27
CLK D
DWG NO LBD5873
REV 5


8
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D
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209
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT BUS D DATA
PATHS, EASH, EADH
SHEET 11 OF 27
SIZE D
DWG. NO LBD5873
REV 6
44B
44A
42B
34A
32B
32A
44L
42L
40K
40C
34C
38K
30G
30H
28G
26G
44J
42K
42J
38J
44H
42H
40H
36C
44G
42G
40G
36H
34H
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[214] CS1ØA+
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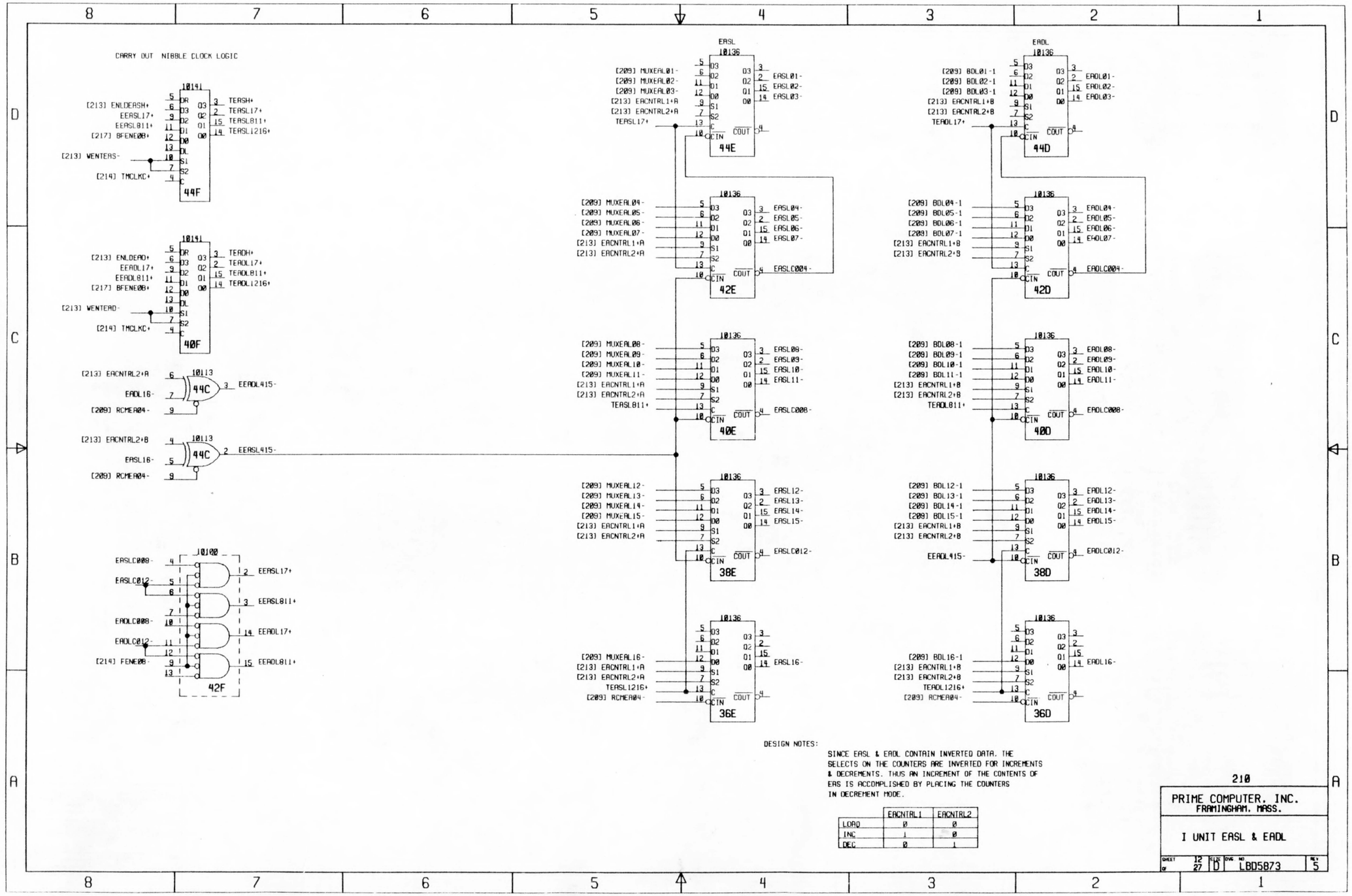
VSELBDEASH+
BDLHLP+
BDHRP+
BDLLP+
BDLRP+
CA1-49
CA9-47
CA9-20
RINGBIT1-
RINGBIT2-
FSYSCLR+
RCMEAØ4-
VIH+B
BST7A+
ST7A-B


CARRY OUT NIBBLE CLOCK LOGIC
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EEASL17+
EEASL811+
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[214] TMCLKC+
TEASH+
TEASL17+
TEASL811+
TEASL1216+
44F
10141
[213] ENLDEAD+
EEADL17+
EEADL811+
[217] BFENE08+
[213] WENTEAD-
[214] TMCLKC+
TEADH+
TEADL17+
TEADL811+
TEADL1216+
40F
10113
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EADL16-
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44C
EEADL415-
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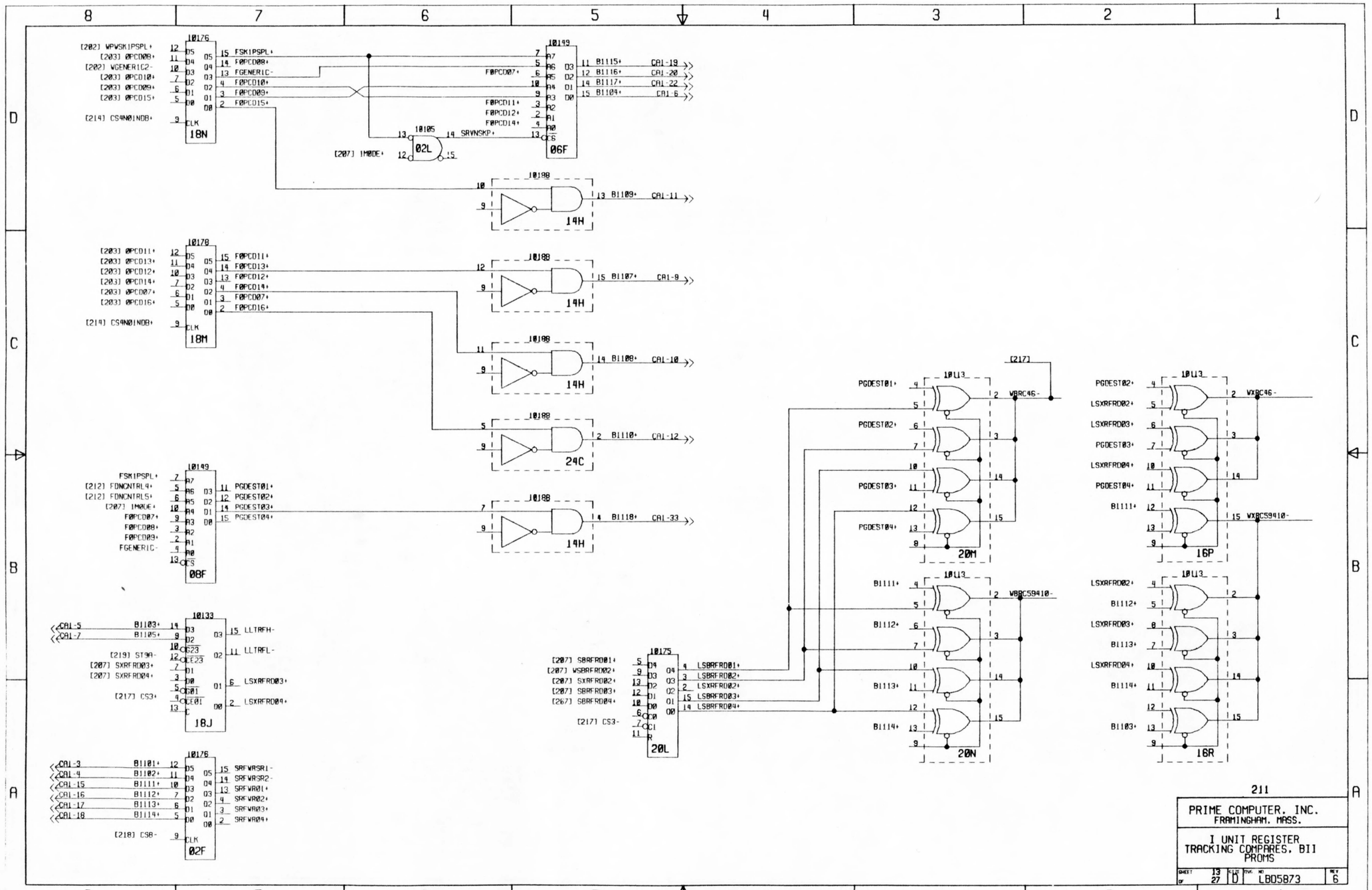
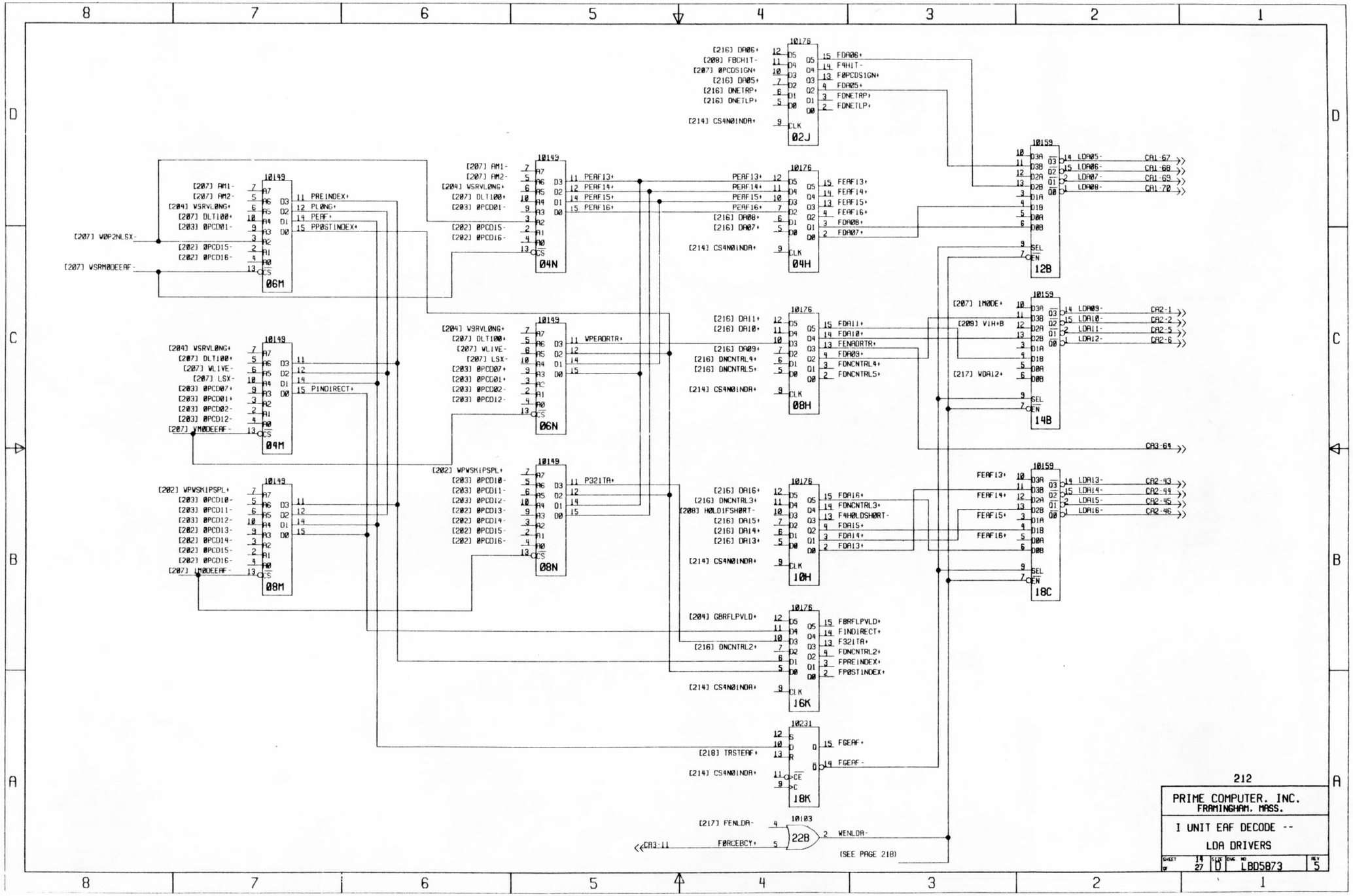
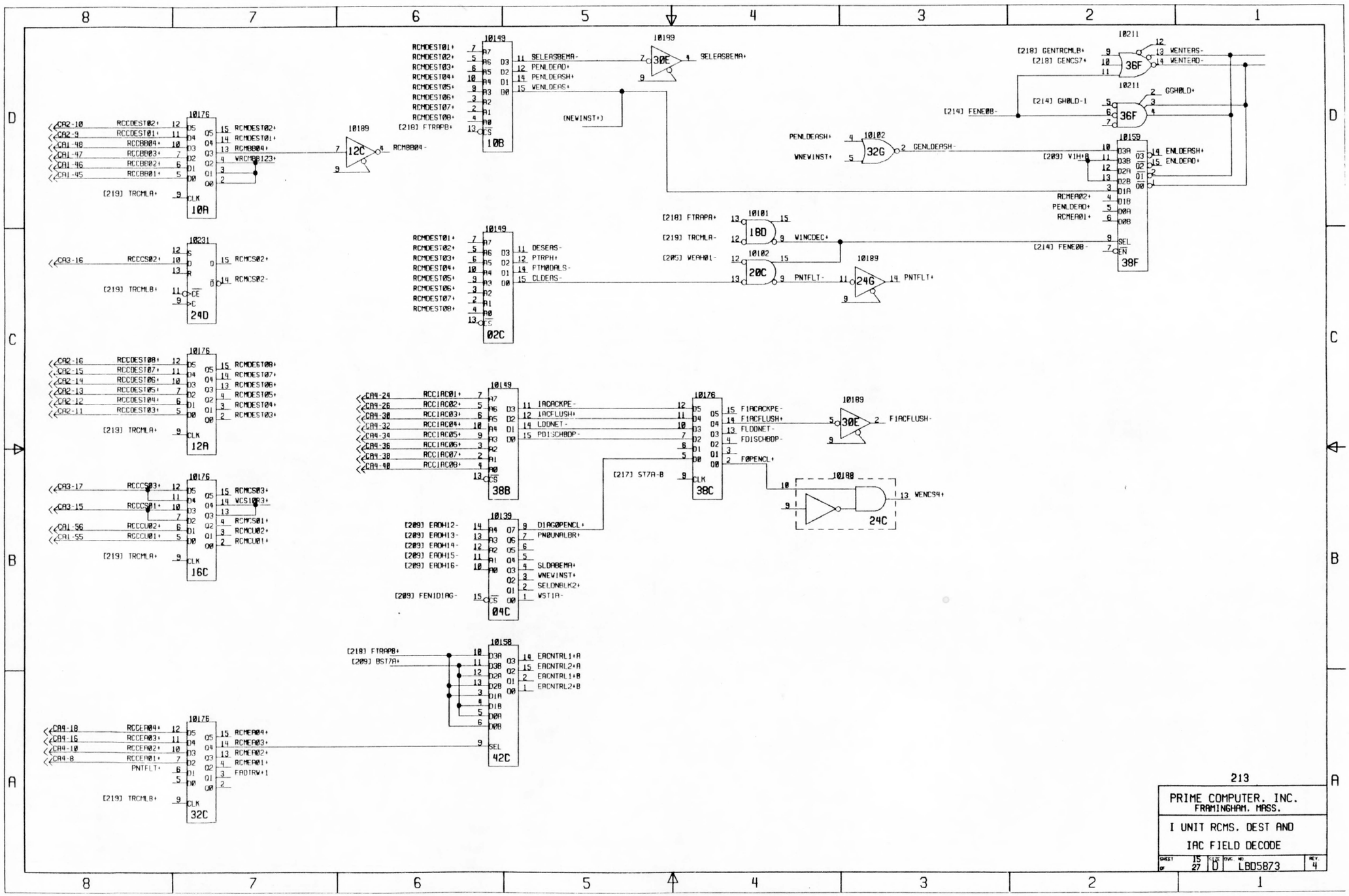
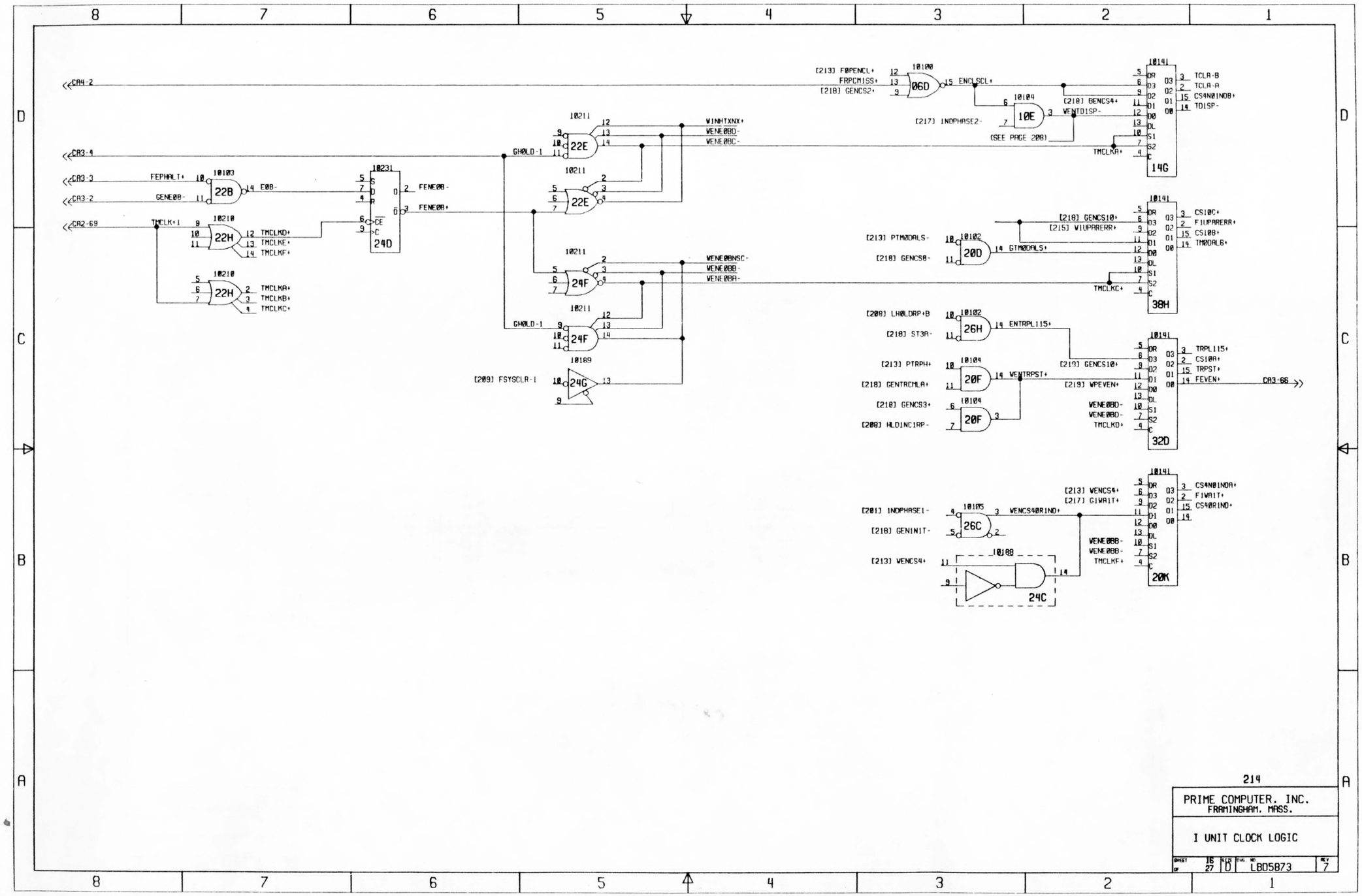
EASL16-
[209] RCMEA04-
44C
EEASL415-
10100
EASLC008-
EASLC012-
EADLC008-
EADLC012-
[214] FENE08-
EEASL17+
EEASL811+
EEADL17+
EEADL811+
42F
EASL
10136
[209] MUXEAL01-
[209] MUXEAL02-
[209] MUXEAL03-
[213] EACNTRL1+A
[213] EACNTRL2+A
TEASL17+
EASL01-
EASL02-
EASL03-
44E
[209] MUXEAL04-
[209] MUXEAL05-
[209] MUXEAL06-
[209] MUXEAL07-
[213] EACNTRL1+A
[213] EACNTRL2+A
EASL04-
EASL05-
EASL06-
EASL07-
EASLC004-
42E
[209] MUXEAL08-
[209] MUXEAL09-
[209] MUXEAL10-
[209] MUXEAL11-
[213] EACNTRL1+A
[213] EACNTRL2+A
TEASL811+
EASL08-
EASL09-
EASL10-
EASL11-
EASLC008-
40E
[209] MUXEAL12-
[209] MUXEAL13-
[209] MUXEAL14-
[209] MUXEAL15-
[213] EACNTRL1+A
[213] EACNTRL2+A
EASL12-
EASL13-
EASL14-
EASL15-
EASLC012-
38E
[209] MUXEAL16-
[213] EACNTRL1+A
[213] EACNTRL2+A
TEASL1216+
[209] RCMEA04-
EASL16-
36E
EADL
10136
[209] BDL01-1
[209] BDL02-1
[209] BDL03-1
[213] EACNTRL1+B
[213] EACNTRL2+B
TEADL17+
EADL01-
EADL02-
EADL03-
44D
[209] BDL04-1
[209] BDL05-1
[209] BDL06-1
[209] BDL07-1
[213] EACNTRL1+B
[213] EACNTRL2+B
EADL04-
EADL05-
EADL06-
EADL07-
EADLC004-
42D
[209] BDL08-1
[209] BDL09-1
[209] BDL10-1
[209] BDL11-1
[213] EACNTRL1+B
[213] EACNTRL2+B
TEADL811+
EADL08-
EADL09-
EADL10-
EADL11-
EADLC008-
40D
[209] BDL12-1
[209] BDL13-1
[209] BDL14-1
[209] BDL15-1
[213] EACNTRL1+B
[213] EACNTRL2+B
EEADL415-
EADL12-
EADL13-
EADL14-
EADL15-
EADLC012-
38D
[209] BDL16-1
[213] EACNTRL1+B
[213] EACNTRL2+B
TEADL1216+
[209] RCMEA04-
EADL16-
36D
DESIGN NOTES:
SINCE EASL & EADL CONTAIN INVERTED DATA, THE SELECTS ON THE COUNTERS ARE INVERTED FOR INCREMENTS & DECREMENTS. THUS AN INCREMENT OF THE CONTENTS OF EAS IS ACCOMPLISHED BY PLACING THE COUNTERS IN DECREMENT MODE.
EACNTRL1
EACNTRL2
LOAD
INC
DEC
210
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT EASL & EADL
SHEET 12 OF 27
SIZE D
DWG NO LBD5873
REV 5


18N
06F
02L
14H
18M
24C
08F
18J
02F
20M
20N
20L
16P
16R
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT REGISTER
TRACKING COMPARES, BII
PROMS
LBD5873


06M
04N
02J
04H
12B
04M
06N
08H
14B
08M
08N
10H
18C
16K
18K
22B
(SEE PAGE 218)
212
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT EAF DECODE --
LDA DRIVERS
LBD5873
5


10A
12A
16C
32C
24D
12C
10B
02C
42C
04C
38B
38C
36F
38F
30E
32G
20C
18D
24G
24C
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT RCMS. DEST AND
IAC FIELD DECODE
213
LBD5873
REV 4

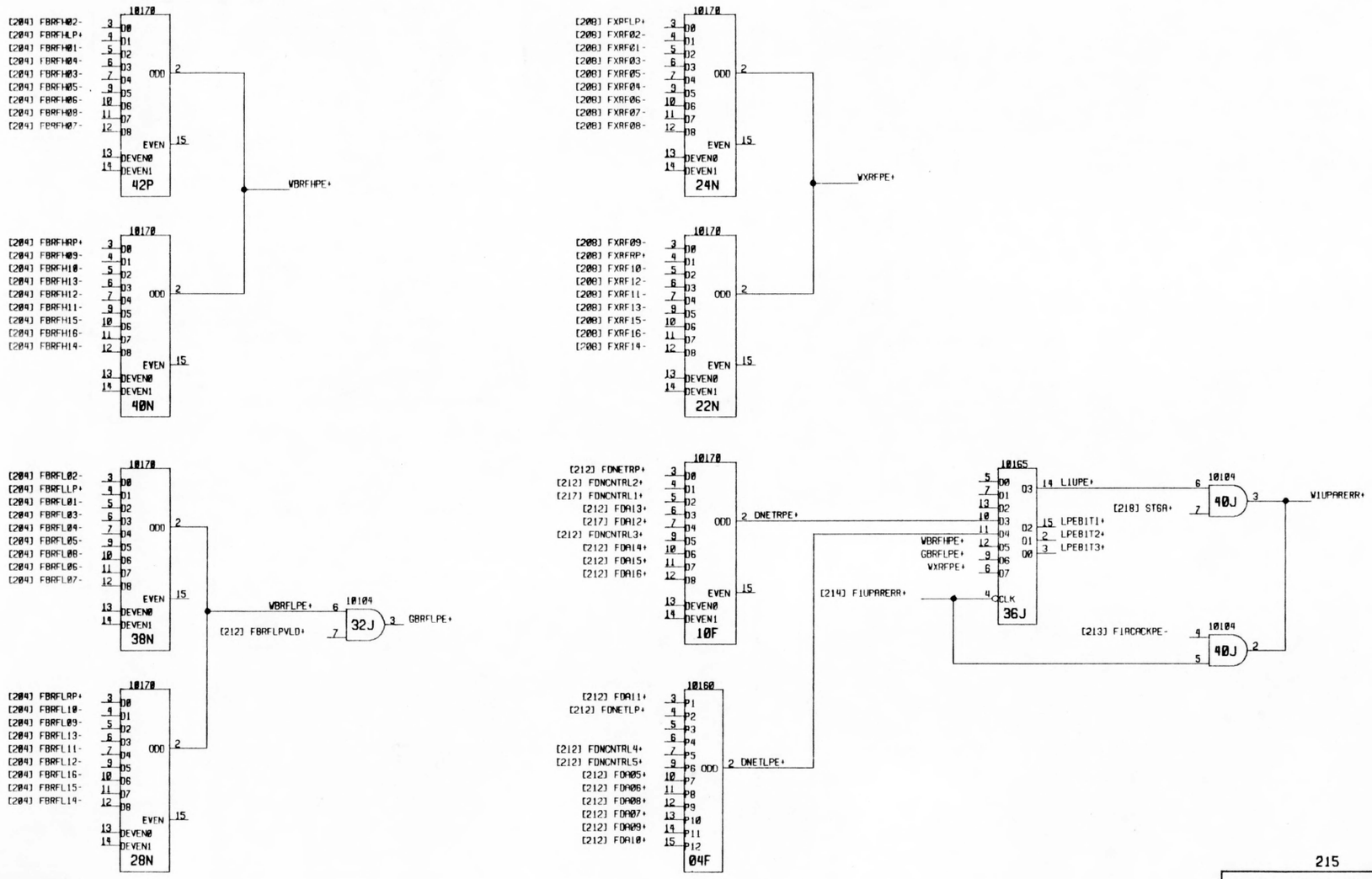


214

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

I UNIT CLOCK LOGIC

SHEET OF	SIZE	DWG NO	REV
16 27	D	LBD5873	7



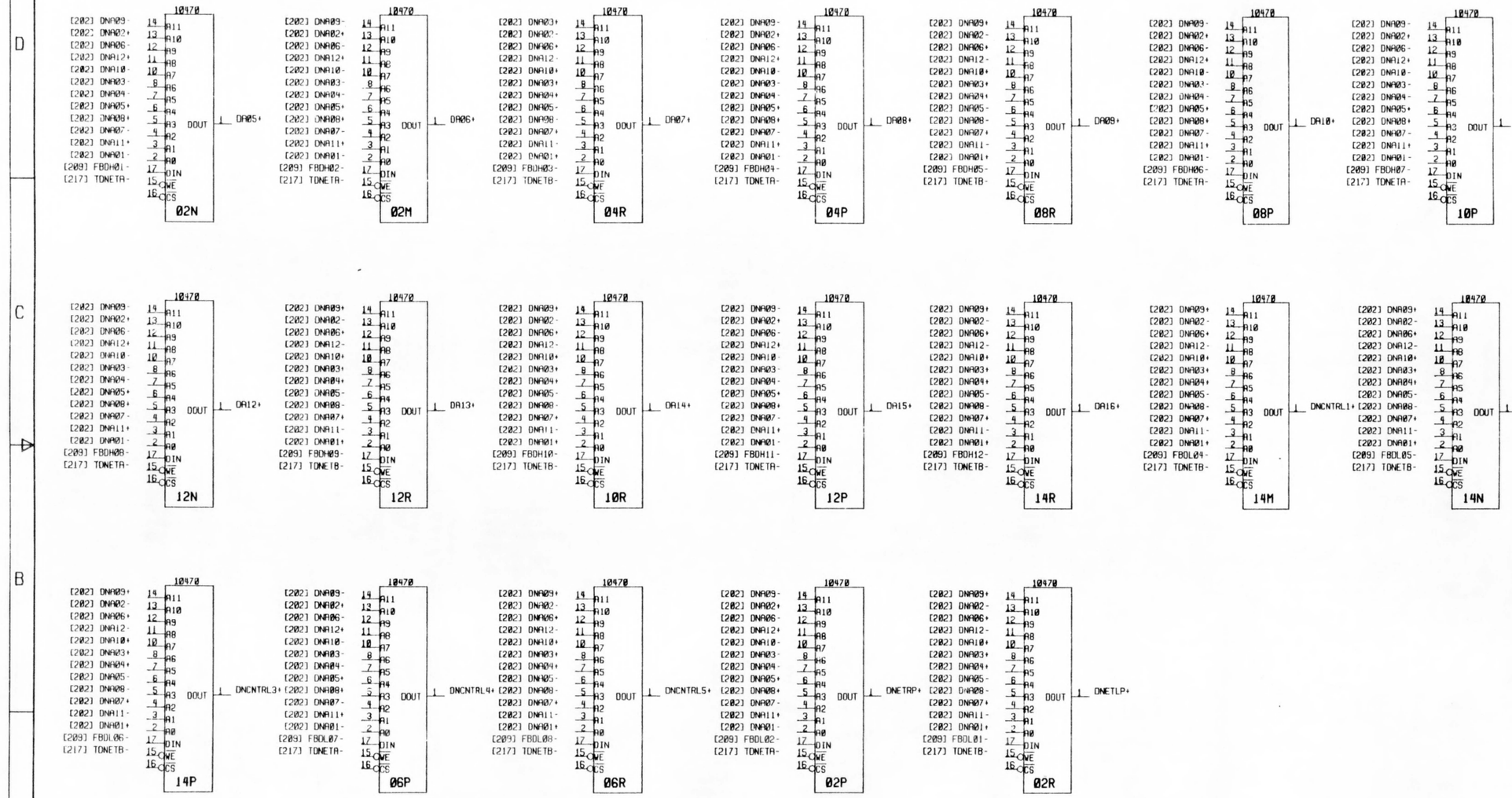
NOTE: EVEN PARITY IS USED ON THE I-UNIT.
THAT IS, A BYTE OF ZEROS PLUS A PARITY
BIT OF ZERO IS CORRECT PARITY.

215

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

I UNIT PARITY CHECKING

SHEET 17 OF 27 | SIZE D | DWG NO LBD5873 | REV 5

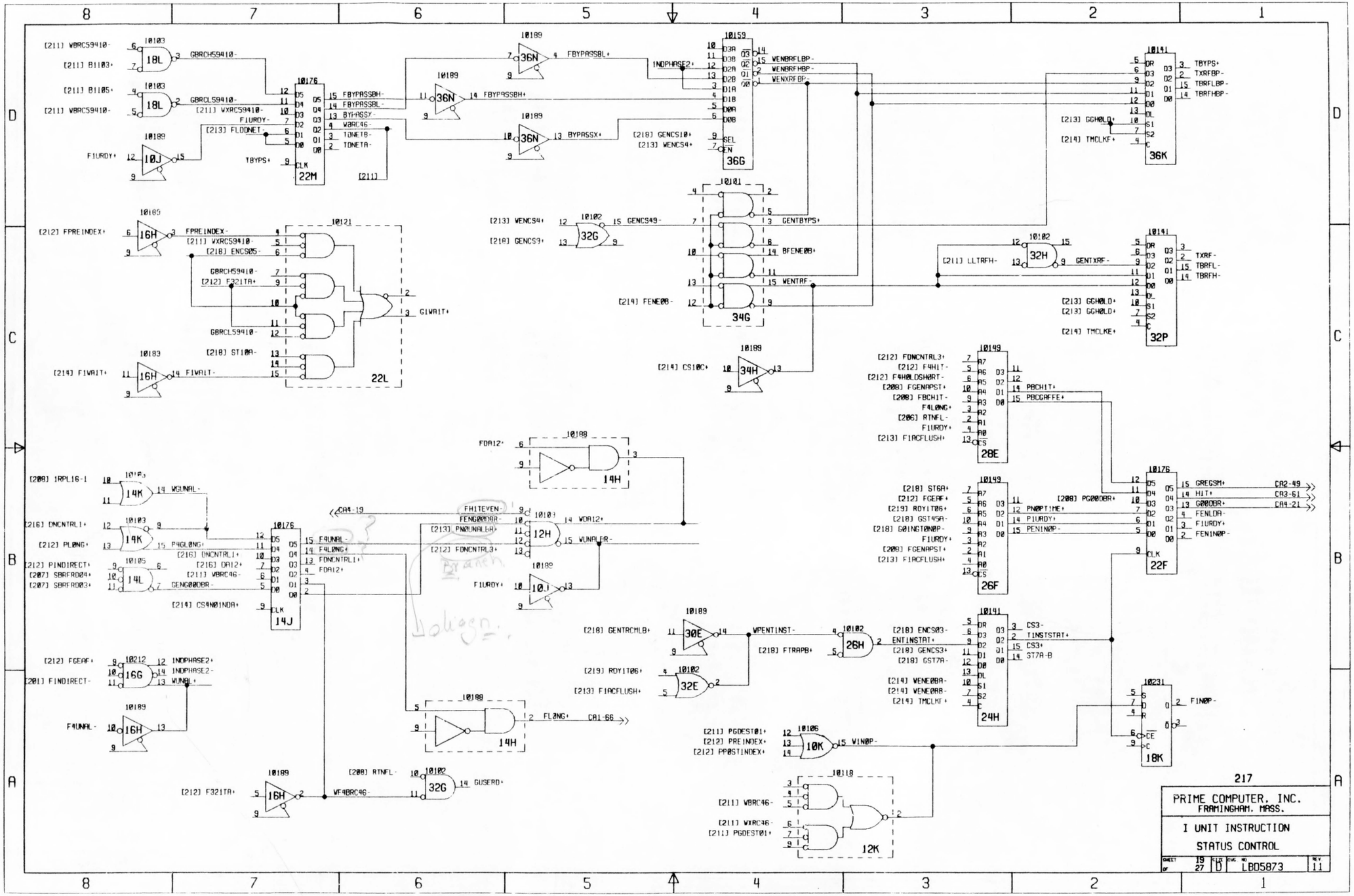


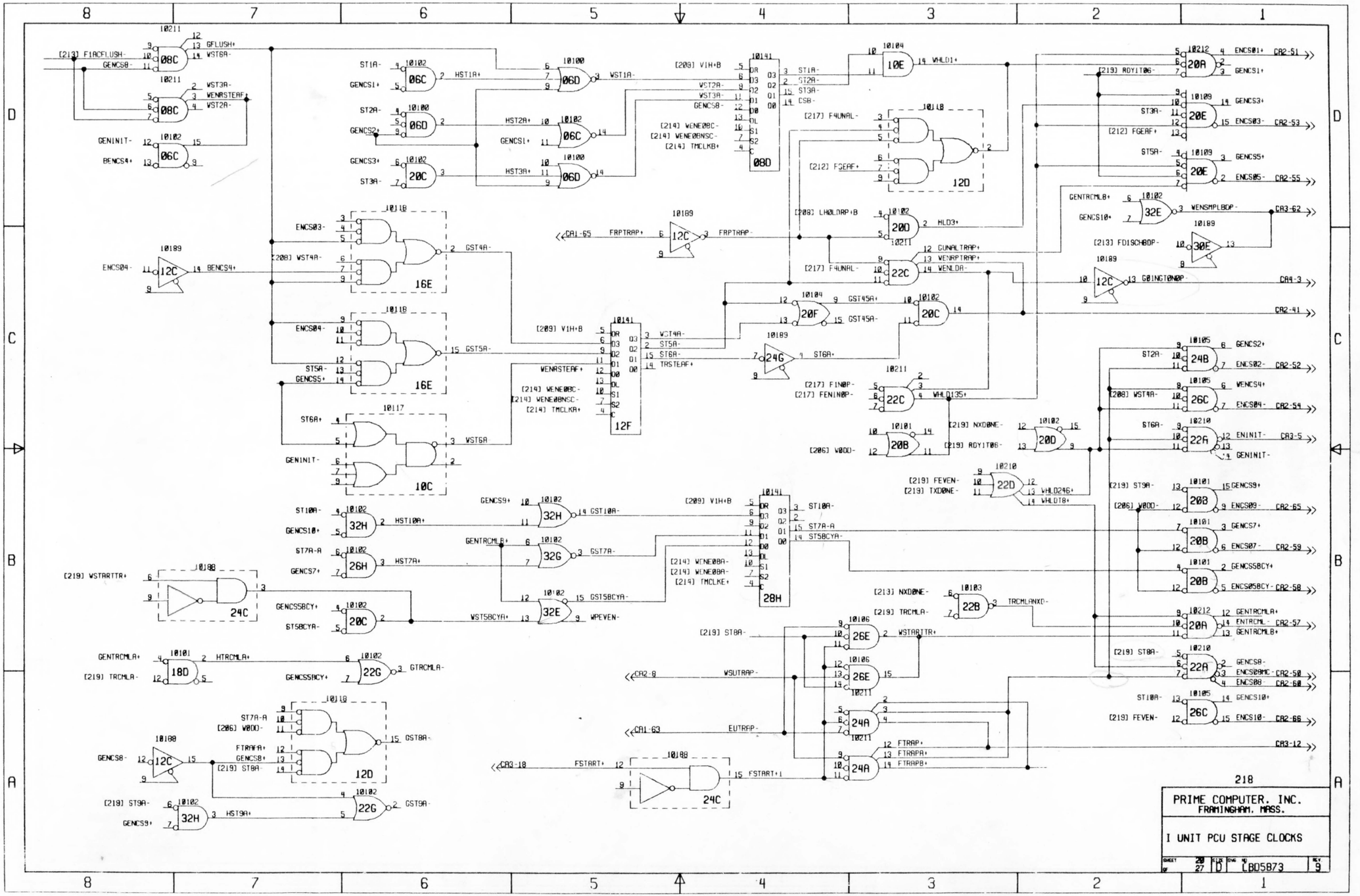
216

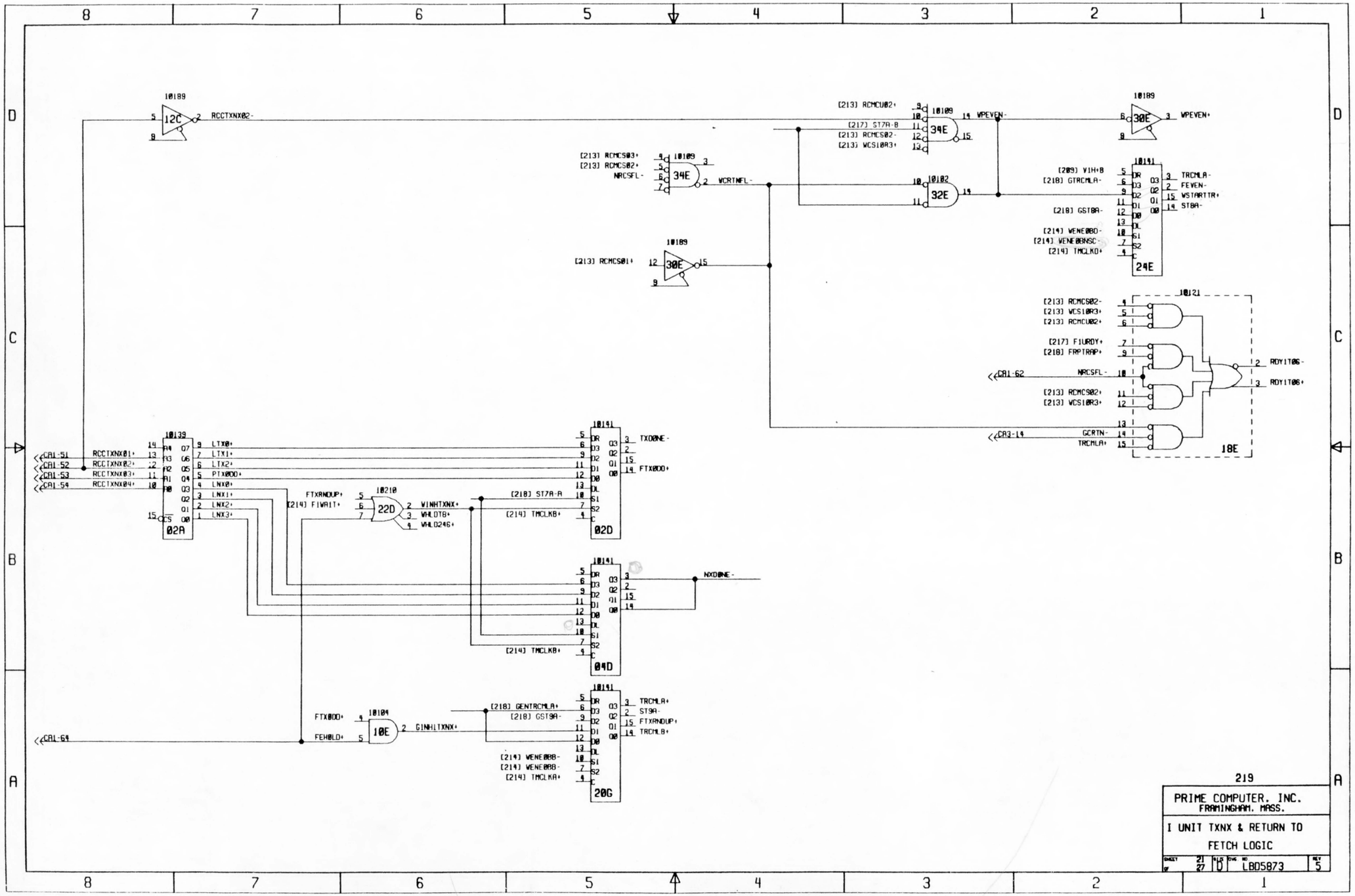
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

I UNIT DECODE NET

SHEET OF	SIZE	DWG NO	REV
18 27	D	LBD5873	3


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT INSTRUCTION
STATUS CONTROL
217
LBD5873
REV 11


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I UNIT PCU STAGE CLOCKS
218
SHEET 20 27
SIZE D
ENG NO LBD5873
REV 9



219

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

I UNIT TXNX & RETURN TO FETCH LOGIC

SHEET	OF	SIZE	DWG NO	REV
21	27	D	LBD5873	5

CA1-13 >>GND

CA1-14 >>GND

CA1-27 >>-5.2V

CA1-28 >>-5.2V

CA1-29 >>-5.2V

CA1-30 >>-5.2V

CA1-43 >>-2V

CA1-44 >>-2V

CA1-57 >>GND

CA1-58 >>GND

CA1-59 >>GND

CA1-60 >>GND

CA2-17 >>-5.2V

CA2-18 >>-5.2V

CA2-19 >>-5.2V

CA2-20 >>-5.2V

CA2-3 >>GND

CA2-33 >>-2V

CA2-34 >>-2V

CA2-4 >>GND

CA2-47 >>GND

CA2-48 >>GND

CA2-61 >>GND

CA2-62 >>GND

CA2-63 >>GND

CA2-64 >>GND

CA2-67 >>GND

CA2-78 >>GND

CA3-1 >>GND

CA3-10 >>GND

CA3-23 >>GND

CA3-24 >>GND

CA3-37 >>-2V

CA3-38 >>-2V

CA3-51 >>-5.2V

CA3-52 >>-5.2V

CA3-53 >>-5.2V

CA3-54 >>-5.2V

CA3-67 >>GND

CA3-68 >>GND

CA3-7 >>GND

CA3-8 >>GND

CA3-9 >>GND

CA4-11 >>GND

CA4-12 >>GND

CA4-13 >>GND

CA4-14 >>GND

CA4-27 >>-2V

CA4-28 >>-2V

CA4-41 >>-5.2V

CA4-42 >>-5.2V

CA4-43 >>-5.2V

CA4-44 >>-5.2V

CA4-57 >>GND

CA4-58 >>GND

C176
22
15V.10%
GND 1 + 2 -2V

C177
22
15V.10%
GND 1 + 2 -5.2V

C179
22
15V.10%
GND 1 + 2 -5.2V

C178
22
15V.10%
GND 1 + 2 -2V

NOTE :

1. .01 UF AXIAL LEAD CAPACITORS ARE NOT SHOWN BUT ARE INSTALLED ABOVE THE DIPS IN THE FOLLOWING COLUMNS : A.C.E.G.J.L.N.R EXCEPT AT 02L.12L.14L

2. UNLESS OTHERWISE SPECIFIED :
RESISTANCE VALUES ARE IN OHMS
CAPACITANCE VALUES ARE IN MICROFARADS

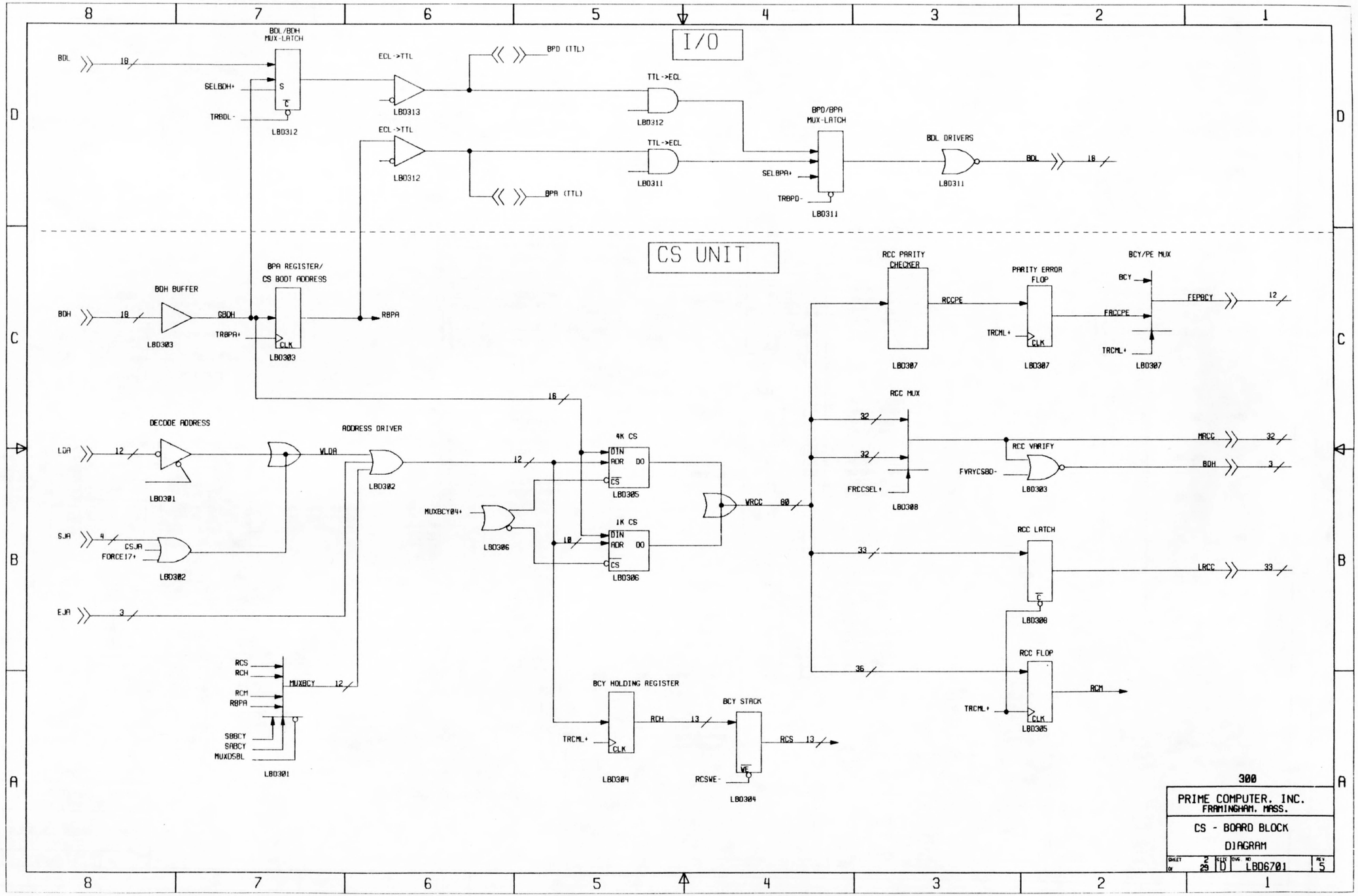
220

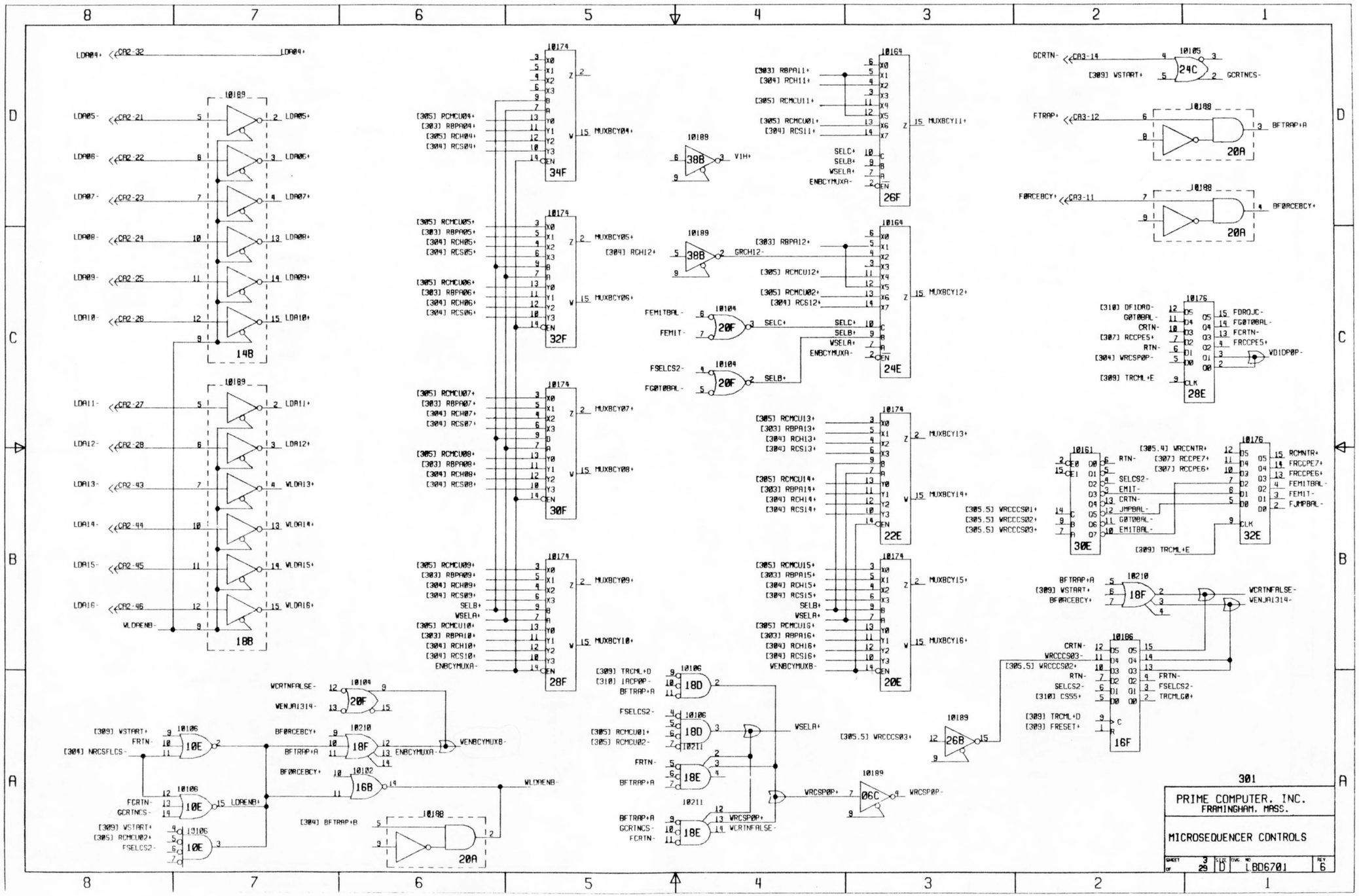
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

I UNIT POWER CONNS.

BYPASS CAPS

SHEET 22 OF 27 | SIZE D | DWG NO L805873 | REV 5


I/O
BDL/BDH MUX-LATCH
BDL
16
SELBDH+
TRBDL-
LBD312
ECL->TTL
LBD313
BPD (TTL)
TTL->ECL
LBD312
BPD/BPA MUX-LATCH
SELBPA+
TRBPD-
LBD311
BDL DRIVERS
LBD311
BPA (TTL)
CS UNIT
BPA REGISTER/ CS BOOT ADDRESS
BDH BUFFER
BDH
GBDH
TRBPA+
RBPA
LBD303
RCC PARITY CHECKER
RCCPE
PARITY ERROR FLOP
TRCML+
BCY/PE MUX
BCY
FEPBCY
12
FRCCPE
LBD307
DECODE ADDRESS
LOA
VLDA
LBD301
ADDRESS DRIVER
LBD302
4K CS
1K CS
DIN
ADR
DO
CS
LBD305
LBD306
MUXBCY04+
LBD306
RCC MUX
32
FRCCSEL+
LBD308
RCC VARIFY
FVRYCS8D-
MRCC
BDH
SJA
CSJA
FORCE17+
EJA
WRCC
80
RCC LATCH
33
LRCC
LBD308
RCC FLOP
36
RCM
LBD305
RCS
RCH
RCM
RBPA
MUXBCY
SBBCY
SABCY
MUXDSBL
LBD301
BCY HOLDING REGISTER
BCY STACK
13
RCSWE-
LBD304
300
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
CS - BOARD BLOCK DIAGRAM
SHEET 2 OF 29
SIZE D
DWG NO LBD6701
REV 5


LDA04+
CA2-32
LDA04+
LDA05-
CA2-21
LDA05+
LDA06-
CA2-22
LDA06+
LDA07-
CA2-23
LDA07+
LDA08-
CA2-24
LDA08+
LDA09-
CA2-25
LDA09+
LDA10-
CA2-26
LDA10+
14B
LDA11-
CA2-27
LDA11+
LDA12-
CA2-28
LDA12+
LDA13-
CA2-43
VLDA13+
LDA14-
CA2-44
VLDA14+
LDA15-
CA2-45
VLDA15+
LDA16-
CA2-46
VLDA16+
WLDRENB-
18B
[305] RCMCU04+
[303] RBPA04+
[305] RCH04+
[304] RCS04+
34F
MUXBCY04+
[305] RCMCU05+
[303] RBPA05+
[304] RCH05+
[304] RCS05+
32F
MUXBCY05+
[304] RCH12+
[305] RCMCU06+
[303] RBPA06+
[304] RCH06+
[304] RCS06+
MUXBCY06+
[305] RCMCU07+
[303] RBPA07+
[304] RCH07+
[304] RCS07+
30F
MUXBCY07+
[305] RCMCU08+
[303] RBPA08+
[304] RCH08+
[304] RCS08+
MUXBCY08+
[305] RCMCU09+
[303] RBPA09+
[304] RCH09+
[304] RCS09+
SELB+
WSELA+
[305] RCMCU10+
[303] RBPA10+
[304] RCH10+
[304] RCS10+
ENBCYMUXA-
28F
MUXBCY09+
MUXBCY10+
38B
V1H+
[303] RBPA11+
[304] RCH11+
[305] RCMCU11+
[305] RCMCU01+
[304] RCS11+
SELC+
SELB+
WSELA+
ENBCYMUXA-
26F
MUXBCY11+
GRCH12-
[303] RBPA12+
[305] RCMCU12+
[305] RCMCU02+
[304] RCS12+
24E
MUXBCY12+
FEMITBAL-
FEMIT-
20F
FSELCS2-
FG0T0BAL-
[305] RCMCU13+
[303] RBPA13+
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22E
MUXBCY13+
[305] RCMCU14+
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[304] RCH14+
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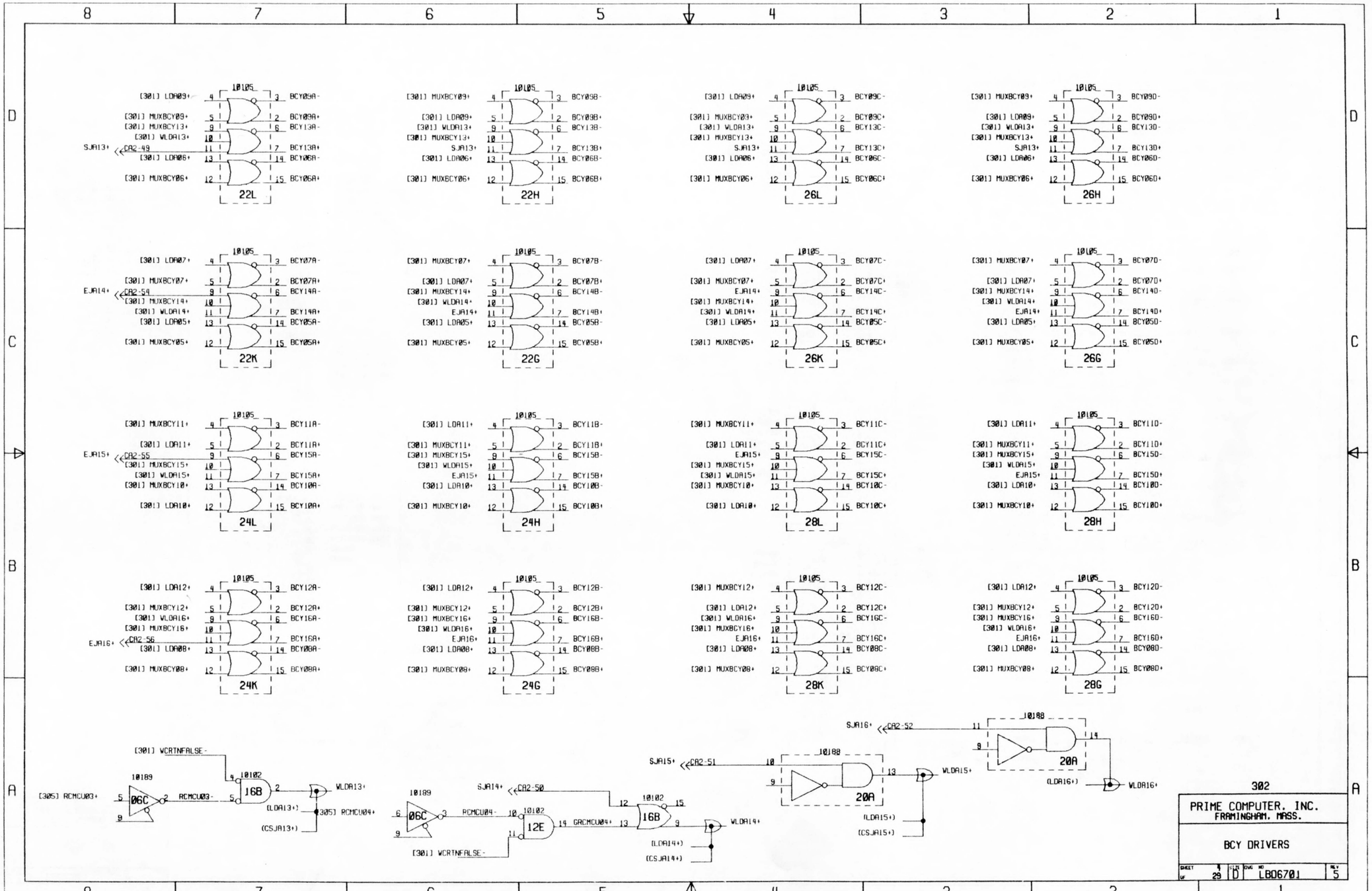
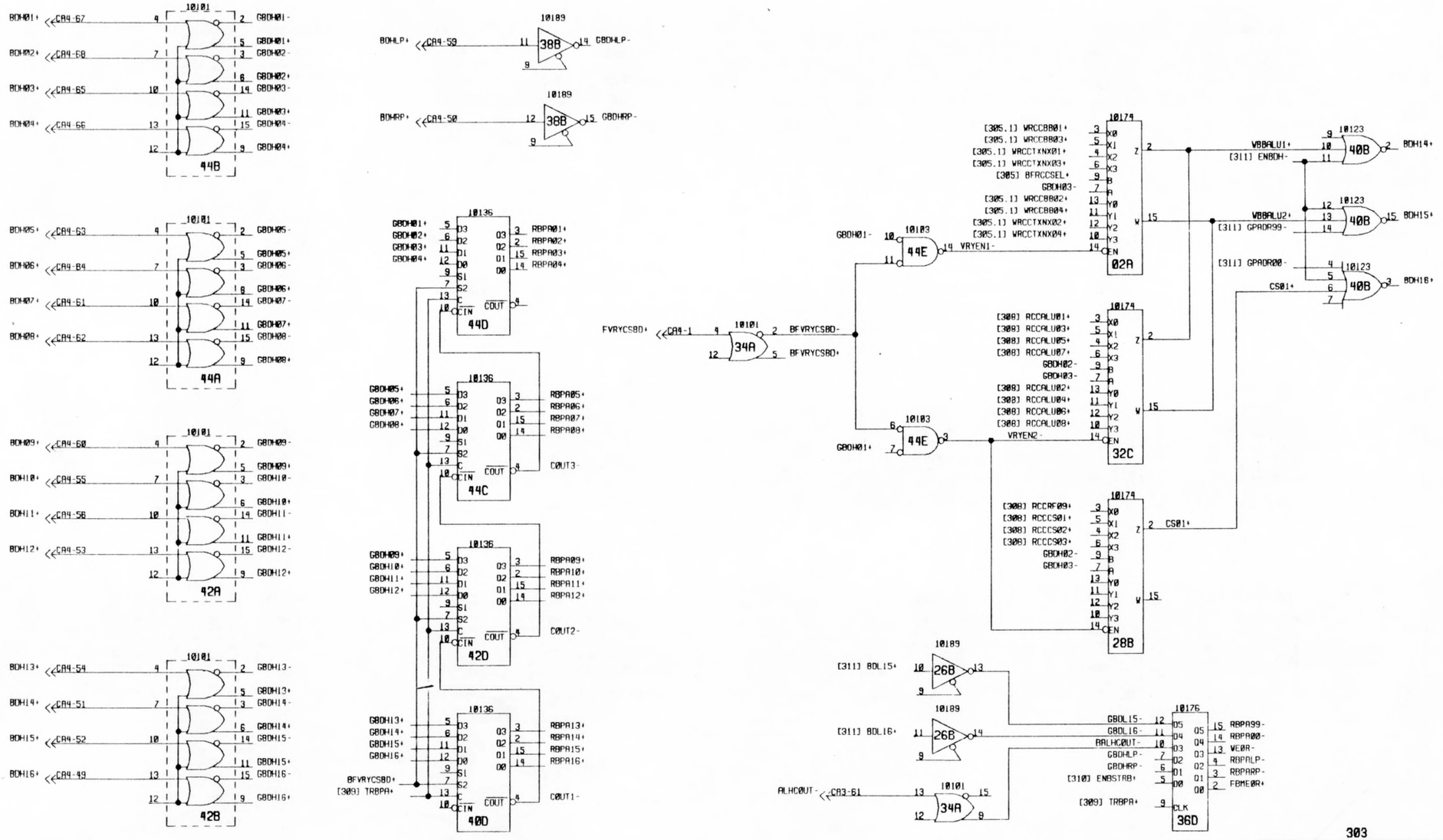
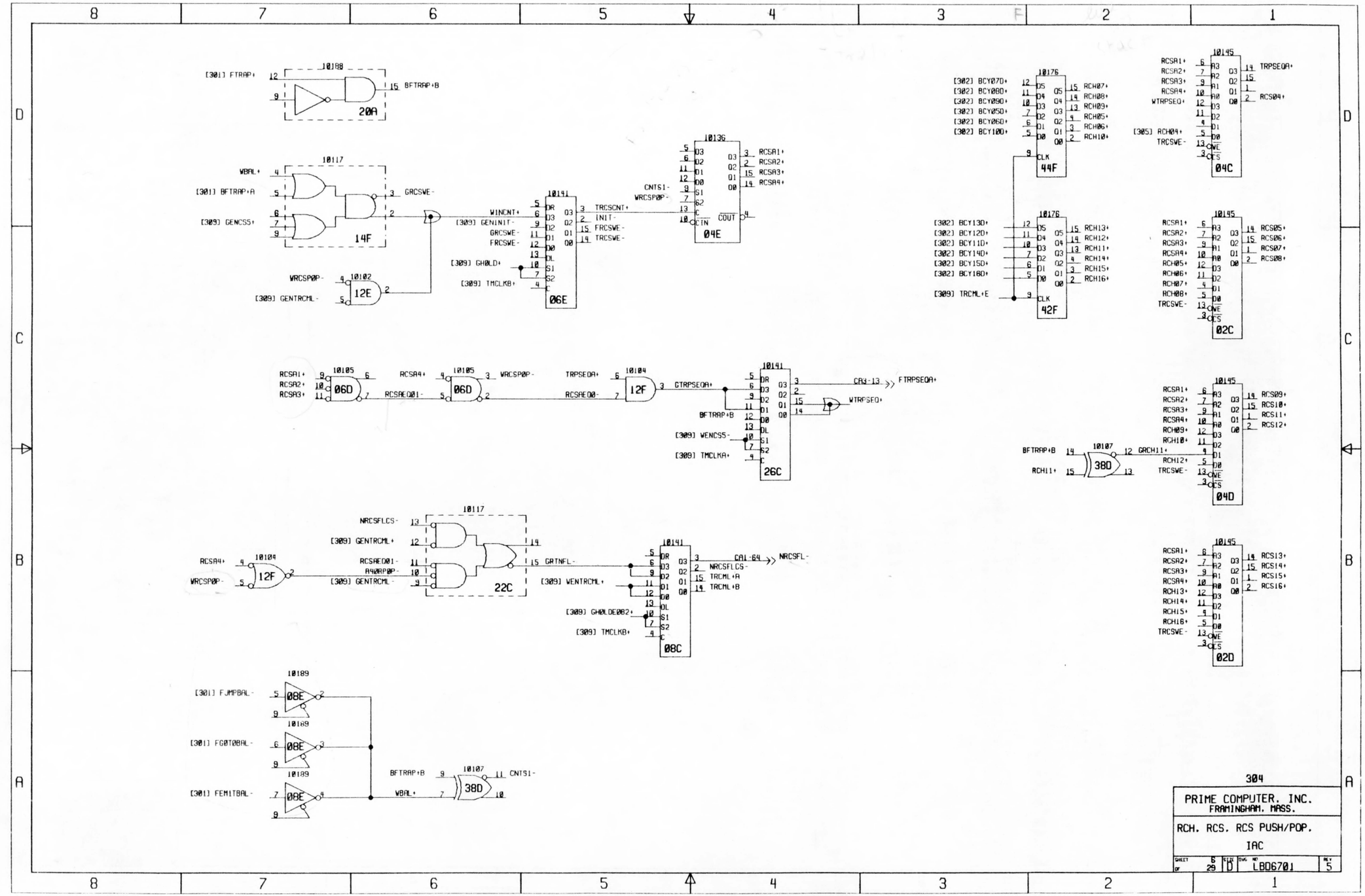
MUXBCY14+
[305] RCMCU15+
[303] RBPA15+
[304] RCH15+
[304] RCS15+
[305] RCMCU16+
[303] RBPA16+
[304] RCH16+
[304] RCS16+
VENBCYMUXB-
20E
MUXBCY15+
MUXBCY16+
GCRTN-
CA3-14
24C
[309] WSTART+
GCRTNCS-
FTRAP+
CA3-12
20A
BFTRAP+A
F0RCEBCY+
CA3-11
BF0RCEBCY+
[310] DF1DRD-
G0T0BAL-
CRTN-
[307] RCCPE5+
RTN-
[304] WRCSP0P-
[309] TRCML+E
28E
FDRQJC-
FG0T0BAL-
FCRTN-
FRCCPE5+
VDIDP0P-
[305.4] WRCCNTR+
[307] RCCPE7+
[307] RCCPE6+
RTN-
SELCS2-
EMIT-
CRTN-
JMPBAL-
G0T0BAL-
EMITBAL-
30E
[305.5] WRCCCS01+
[305.5] WRCCCS02+
[305.5] WRCCCS03+
[309] TRCML+E
32E
RCMNTR+
FRCCPE7+
FRCCPE6+
FEMITBAL+
FEMIT-
FJMPBAL-
BFTRAP+A
[309] VSTART+
BF0RCEBCY+
18F
WCRTNFALSE-
VENJA1314-
CRTN-
WRCCCS03-
[305.5] WRCCCS02+
RTN-
SELCS2-
[310] CS55+
[309] TRCML+D
[309] FRESET+
16F
FRTN-
FSELCS2-
TRCMLG0+
[309] VSTART+
FRTN-
[304] NRCSFLCS-
10E
FCRTN-
GCRTNCS-
LDRENB+
[309] VSTART+
[305] RCMCU02+
FSELCS2-
WCRTNFALSE-
VENJA1314-
20F
BF0RCEBCY+
BFTRAP+A
ENBCYMUXA-
VENBCYMUXB-
16B
WLDRENB-
[304] BFTRAP+B
20A
[309] TRCML+D
[310] IACP0P-
BFTRAP+A
18D
FSELCS2-
[305] RCMCU01+
[305] RCMCU02-
18E
WSELA+
FRTN-
BFTRAP+A
VRCSP0P+
BFTRAP+A
GCRTNCS-
FCRTN-
WCRTNFALSE-
06C
WRCSP0P-
[305.5] WRCCCS03+
26B
301
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MICROSEQUENCER CONTROLS
SHEET 3 OF 29
SIZE D
DWG NO LBD6701
REV 6


22L
22H
26L
26H
22K
22G
26K
26G
24L
24H
28L
28H
24K
24G
28K
28G
20A
20A
16B
16B
06C
06C
12E
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
BCY DRIVERS
302
LBD6701


44B
44A
42A
42B
44D
44C
42D
40D
38B
34A
44E
26B
02A
32C
28B
36D
40B
BDH01+
BDH02+
BDH03+
BDH04+
BDH05+
BDH06+
BDH07+
BDH08+
BDH09+
BDH10+
BDH11+
BDH12+
BDH13+
BDH14+
BDH15+
BDH16+
BDHLP+
BDHRP+
FVRYCSBD+
BFVRYCSBD+
BFVRYCSBD-
ALHC0UT-
VRYEN1-
VRYEN2-
VBBALU1+
VBBALU2+
CS01+
C0UT3-
C0UT2-
C0UT1-
RBPA99-
RBPA00-
VE0R-
RBPALP-
RBPARP-
FBME0R+
303
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
BDH, RBPA
LBD6701
REV 6



304

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

RCH. RCS. RCS PUSH/POP.

IAC

SHEET 6 OF 29 | SIZE D | DWG NO LBD6701 | REV 5

10470 WIRE-OR OUTPUT	DIP SITE	ADDRESS	INPUT	CHIP SELECT	WRITE ENABLE
WRCCBB01+	02L	BCY**A-	GBDH01-	MCSENB1-	MCSWE1A-
WRCCBB02+	02K	BCY**A+	GBDH02-	MCSENB2-	MCSWE1A-
WRCCBB03+	02H	BCY**B-	GBDH03-	MCSENB3-	MCSWE1A-
WRCCBB04+	02G	BCY**B+	GBDH04-	MCSENB4-	MCSWE1A-
WRCCTXNX01+	04L	BCY**A-	GBDH05-	MCSENB1-	MCSWE1A-
WRCCTXNX02+	04K	BCY**A+	GBDH06-	MCSENB2-	MCSWE1A-
WRCCTXNX03+	04H	BCY**B-	GBDH07-	MCSENB3-	MCSWE1A-
WRCCTXNX04+	04G	BCY**B+	GBDH08-	MCSENB4-	MCSWE1A-
WRCCPAR01+	06L	BCY**A-	GBDH09-	MCSENB1-	MCSWE1B-
WRCCCU01+	06K	BCY**A+	GBDH10-	MCSENB2-	MCSWE1B-
WRCCCU02+	06H	BCY**B-	GBDH11-	MCSENB3-	MCSWE1B-
WRCCCU03+	06G	BCY**B+	GBDH12-	MCSENB4-	MCSWE1B-
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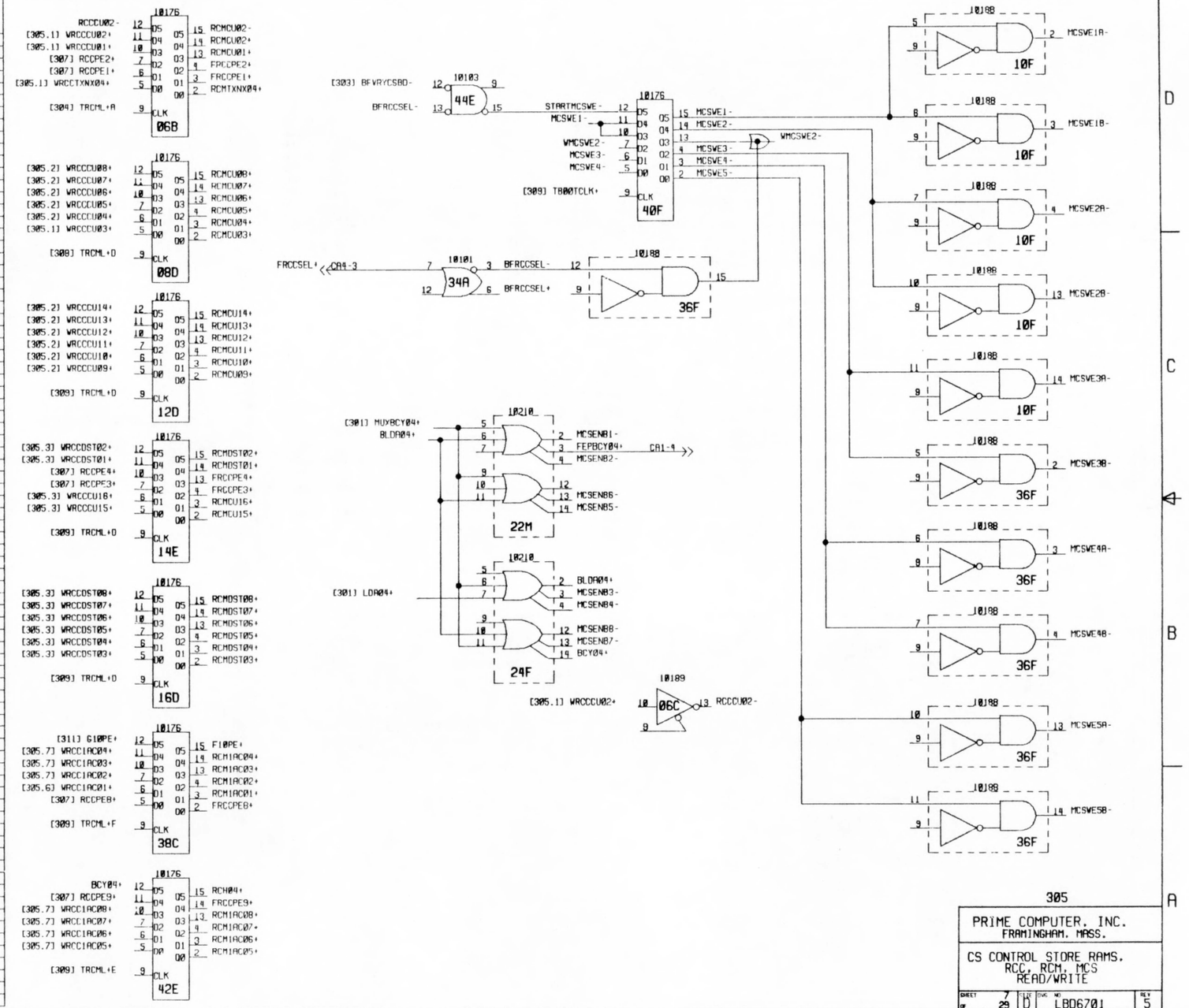
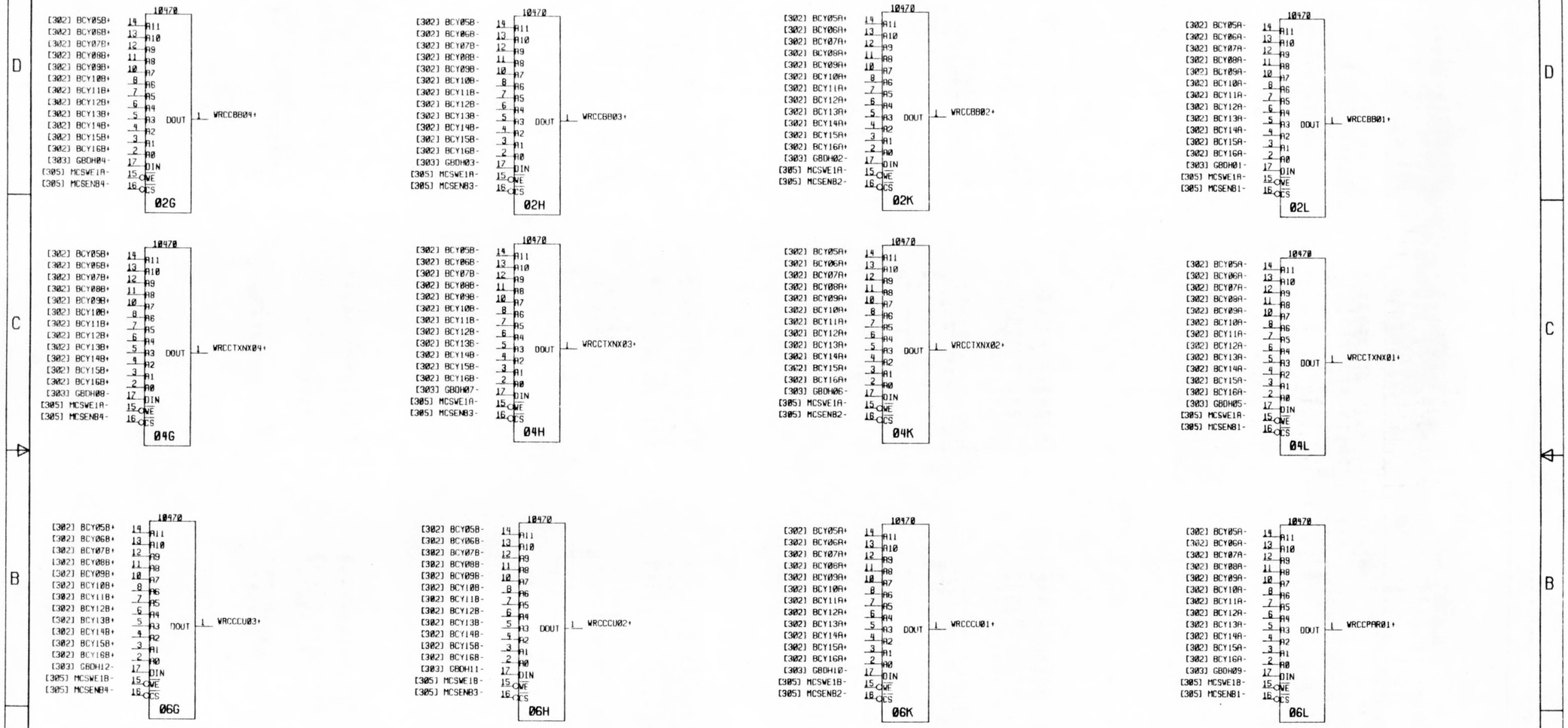


305

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

CS CONTROL STORE RAMS.
RCC, RCM, MCS
READ/WRITE

SHEET 7 OF 29 | SIZE D | DWG NO LBD6701 | REV 5



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PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

1ST 4K OF CONTROL STORE

SHEET	SIZE	DWG NO	REV
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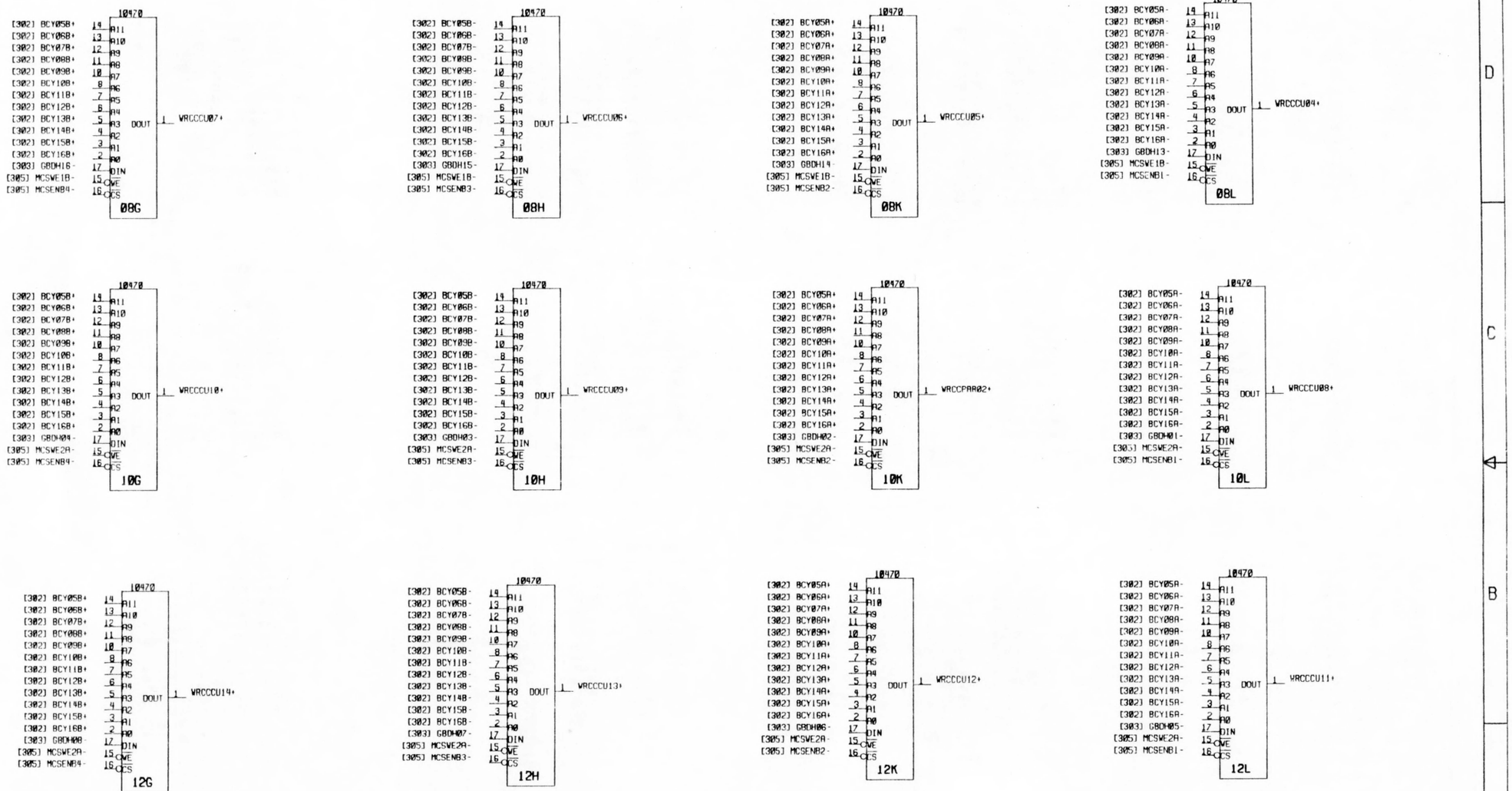
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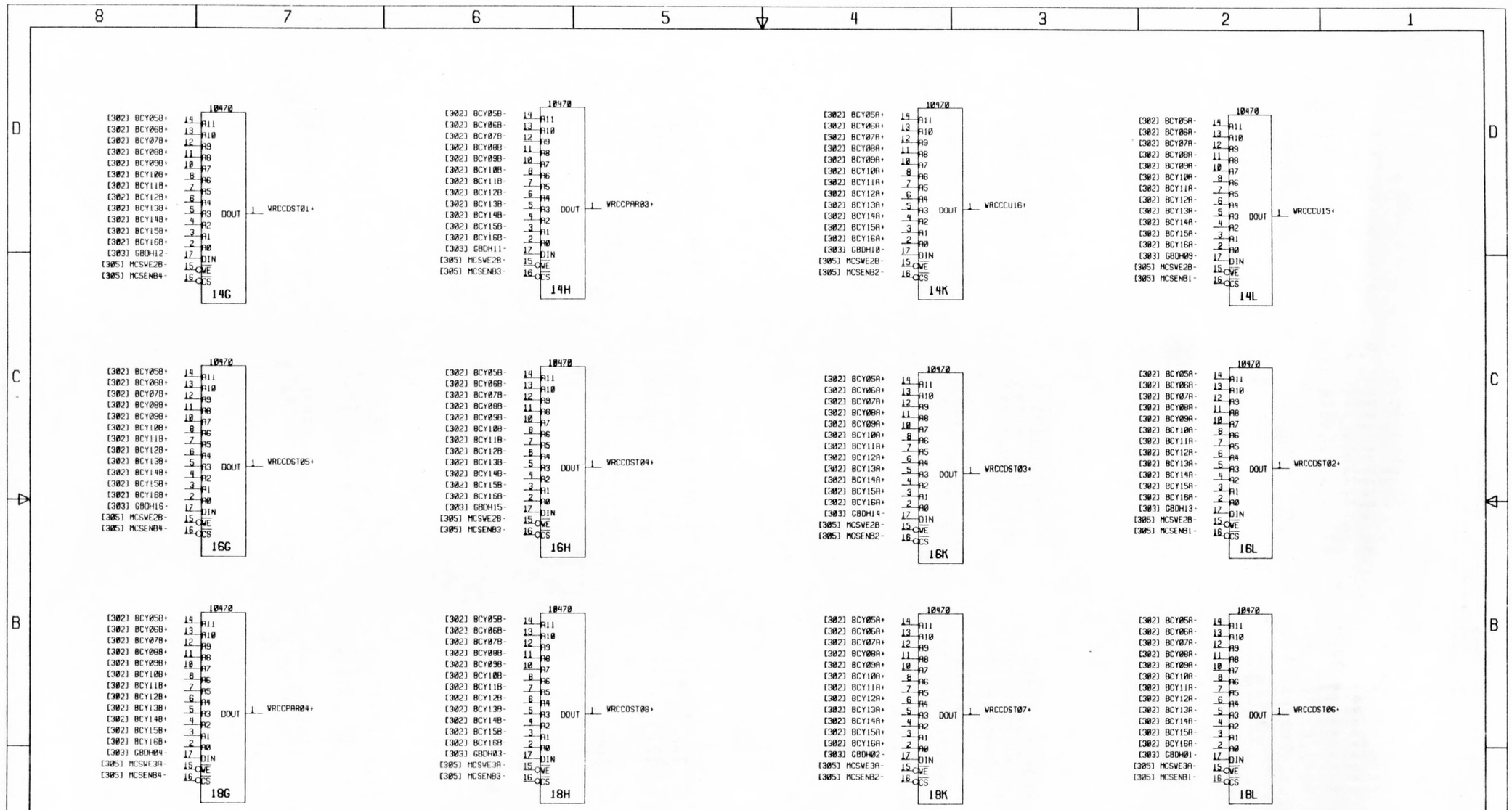
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
1ST 4K OF CONTROL STORE
SHEET 9 OF 29
SIZE D
DWG NO LBD6701
REV 5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PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
1ST 4K OF CONTROL STORE
SHEET 10 29
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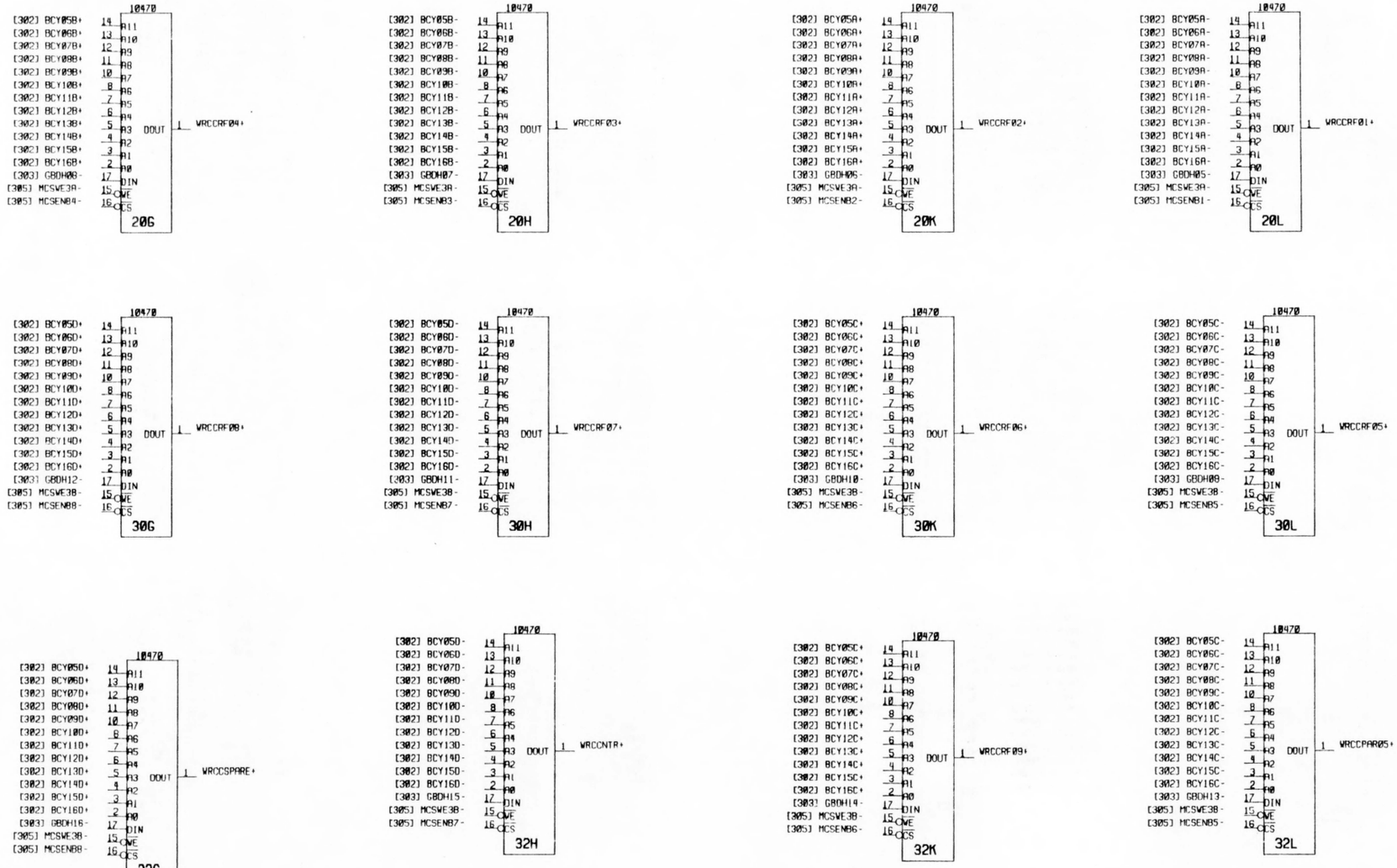
DWG NO LBD6701
REV 5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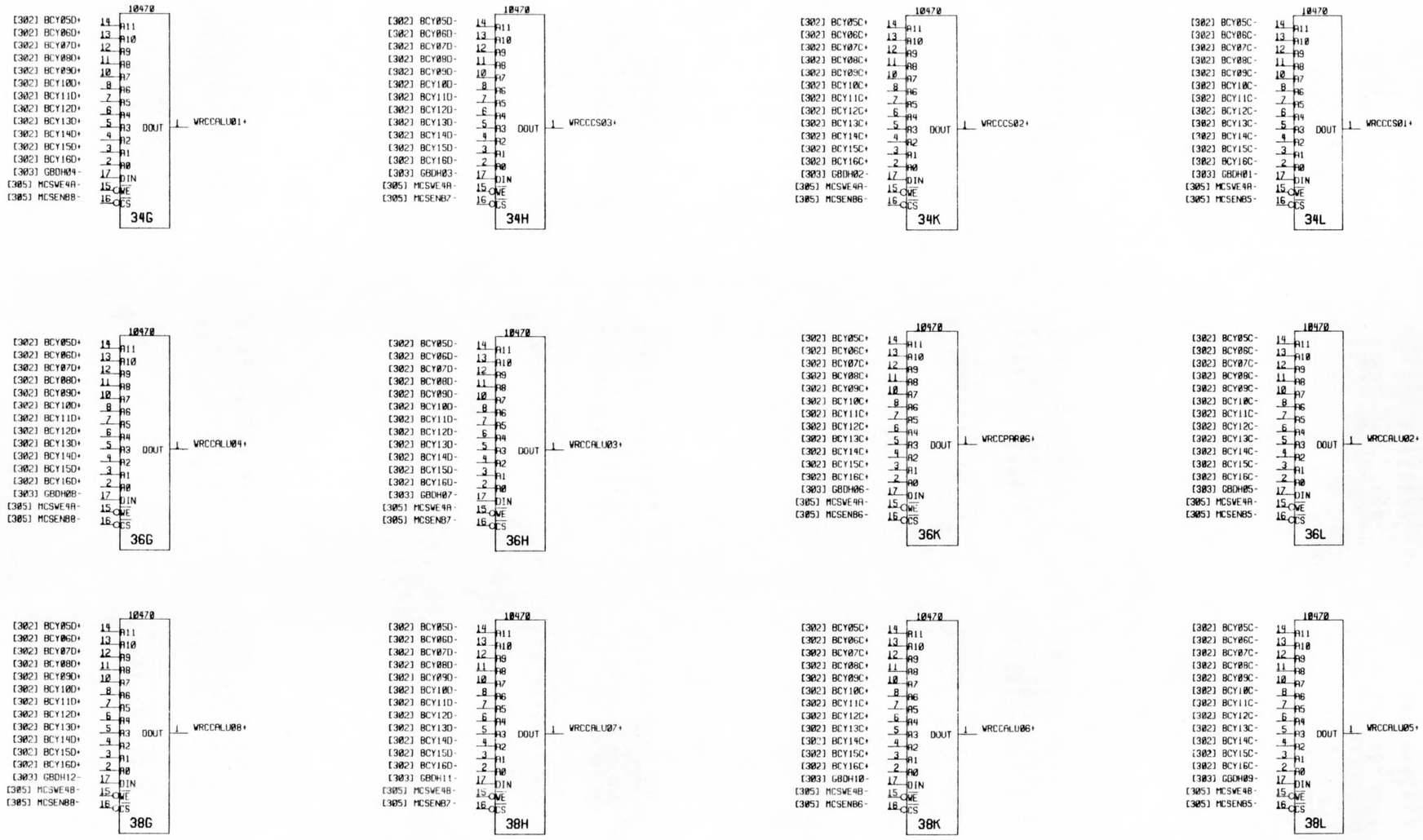
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
1ST 4K OF CONTROL STORE
SHEET 11 OF 29
SIZE D
DWG. NO. LBD6701
REV 4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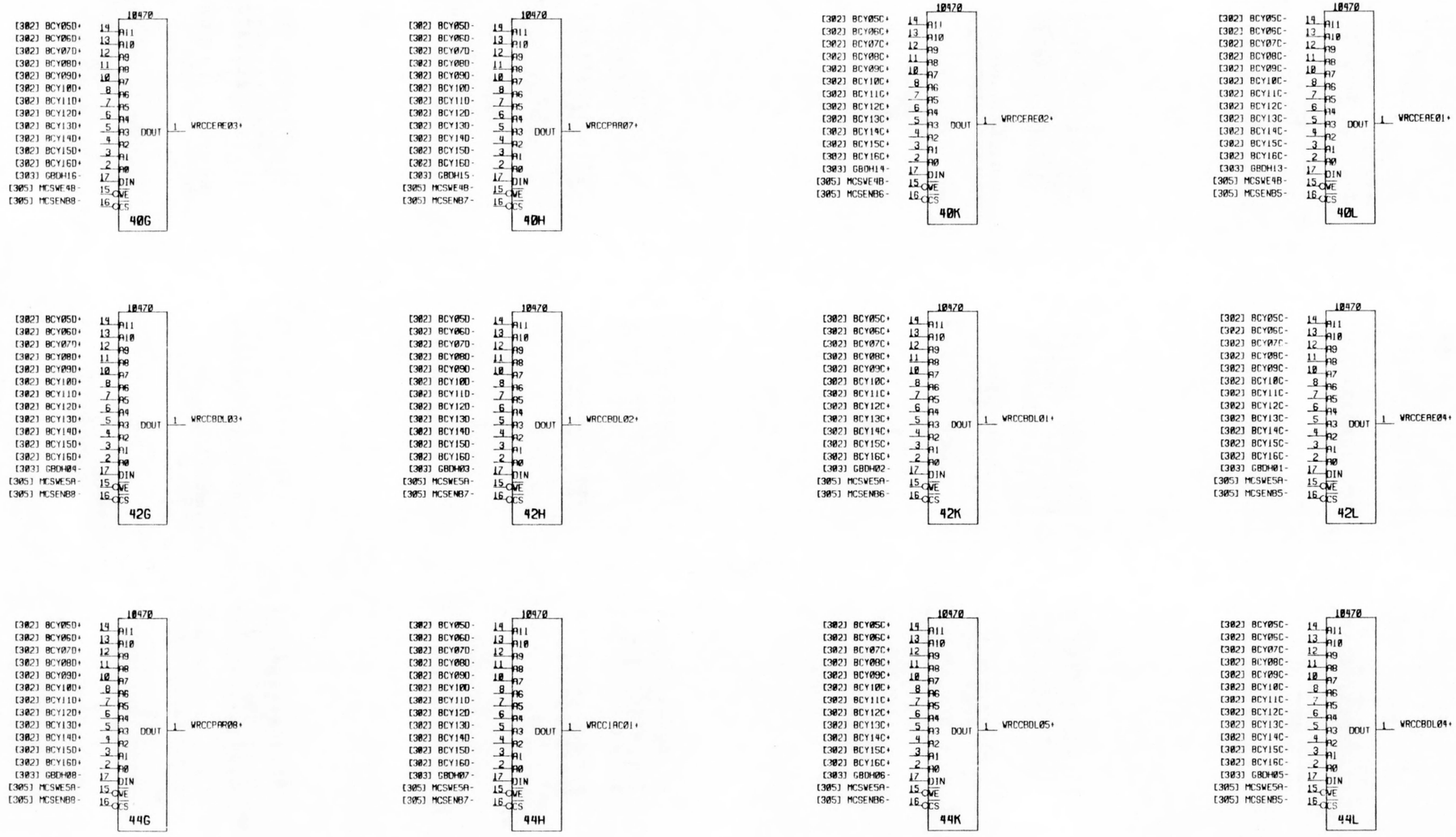
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
16T 4K OF CONTROL STORE
SHEET 12 OF 29
SIZE D
DWG NO LBD6701
REV 4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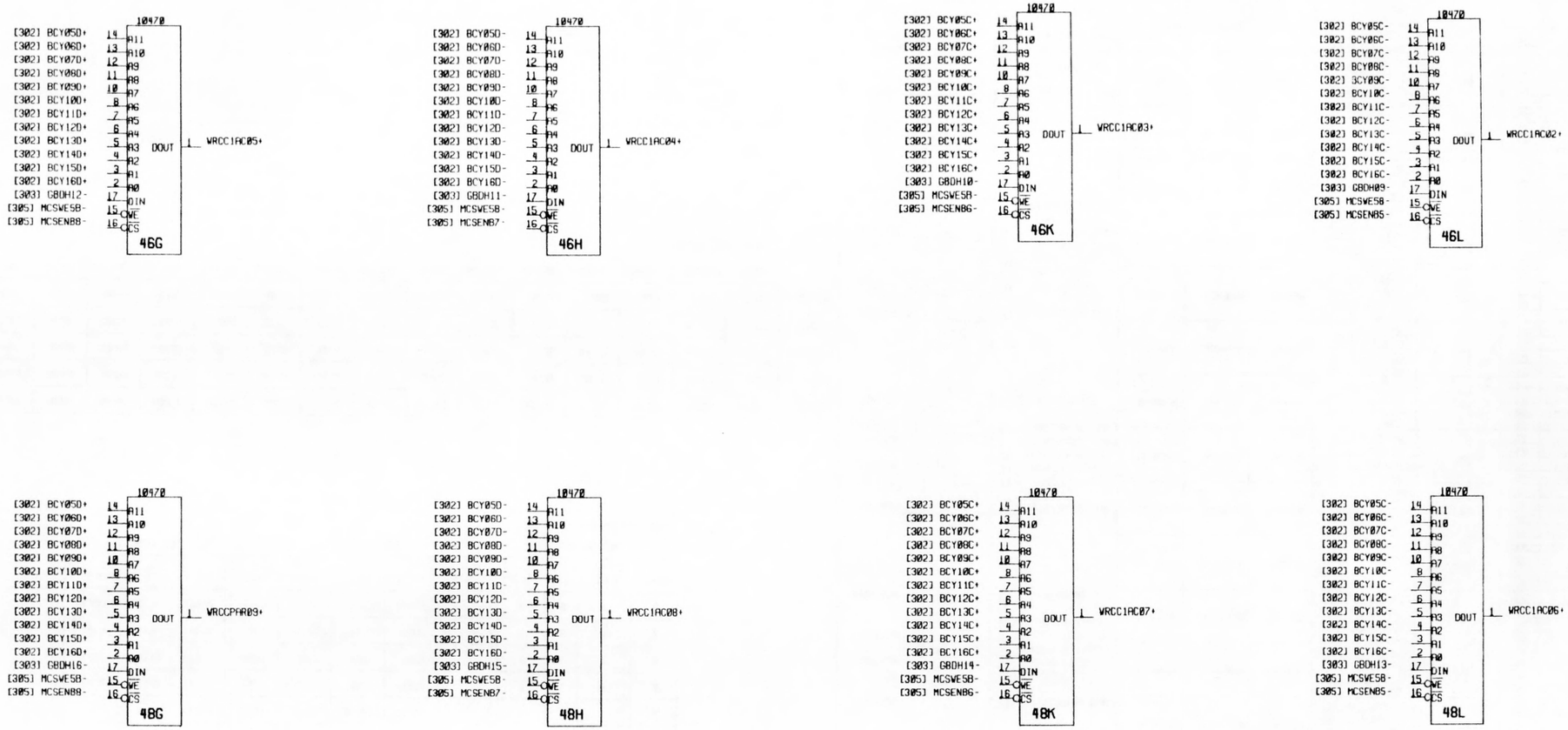
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
1ST 4K OF CONTROL STORE
SHEET 13 OF 29
SIZE D
DWG NO LBD6701
REV 4



305.7

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

1ST 4K OF CONTROL STORE

SHEET	OF	SIZE	DWG NO	REV
14	29	D	LBD6701	4

WIRE-OR OUTPUT	DO PIN	10474 DIP SITE	INPUT DATA	DO PIN	ADDRESS DRIVER	CHIP SELECT	WRITE ENABLE
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WRCCB02↑	03	02J	GBDH02-	21	BCY**E-	MCSENB9-	MCSWE1A-
WRCCB03↑	02		GBDH03-	20			
WRCCB04↑	23		GBDH04-	19			
WRCCTXNX01↑	22		GBDH05-	18			
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WRCCPAR01↑	22		GBDH09-	18			
WRCCCU01↑	03	06J	GBDH10-	21	BCY**E-	MCSENB9-	MCSWE1B-
WRCCCU02↑	02		GBDH11-	20			
WRCCCU03↑	23		GBDH12-	19			
WRCCCU04↑	22		GBDH13-	18			
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WRCCCU07↑	23		GBDH16-	19			
WRCCCU08↑	22		GBDH01-	18			
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WRCCCU15↑	22		GBDH03-	18			
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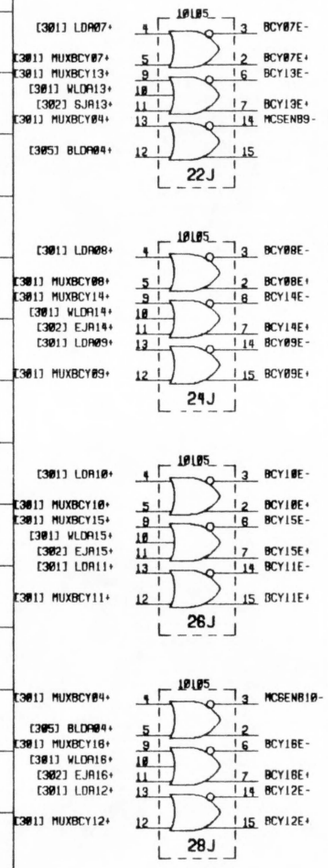

WRITE DATA FORMAT:

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SECTOR 1	BB01	BB02	BB03	BB04	TXNX01	TXNX02	TXNX03	TXNX04	PAR01	CU01	CU02	CU03	CU04	CU05	CU06	CU07
SECTOR 2	CU08	PAR02	CU09	CU10	CU11	CU12	CU13	CU14	CU15	CU16	PAR03	DST01	DST02	DST03	DST04	DST05
SECTOR 3	DST06	DST07	DST08	PAR04	RF01	RF02	RF03	RF04	RF05	RF06	RF07	RF08	PAR05	RF09	TRAP	SPARE
SECTOR 4	CS01	CS02	CS03	ALU01	ALU02	PAR06	ALU03	ALU04	ALU05	ALU06	ALU07	ALU08	EAE01	EAE02	PAR07	EAE03
SECTOR 5	EAE04	BDL01	BDL02	BDL03	BDL04	BDL05	IAC01	PAR08	IAC02	IAC03	IAC04	IAC05	IAC06	IAC07	IAC08	PAR09

READ DATA FORMAT:

RCC SELECT				RCC FROM E2					RCC FROM CS		
FRCCSEL	BDH01	BDH02	BDH03	BDH09	BDH10	BDH11	BDH12	BDH13	BDH14	BDH15	BDH16
0	0	0	0		CU13	CU14	CU15	CU16	ALU07	ALU08	CS03
0	0	0	1		CU09	CU10	CU11	CU12	ALU05	ALU06	CS02
0	0	1	0		CU05	CU06	CU07	CU08	ALU03	ALU04	CS01
0	0	1	1		CU01	CU02	CU03	CU04	ALU01	ALU02	RF09
0	1	X	0		IAC05	IAC06	IAC07	IAC08	BB03	BB04	
0	1	X	1		IAC01	IAC02	IAC03	IAC04	BB01	BB02	
1	0	0	0		RF04	DST06	DST07	DST08	EAE02	EAE03	RF08
1	0	0	1		PAR04	RF01	RF02	RF03	PAR07	EAE01	RF07
1	0	1	0		DST02	DST03	DST04	DST05	PAR05	PAR06	RF06
1	0	1	1		PAR01	PAR02	PAR03	DST01	TRAP	SPARE	RF05
1	1	X	0		BDL04	BDL05	PAR08	PAR09	TXNX03	TXNX04	
1	1	X	1		EAE04	BDL01	BDL02	BDL03	TXNX01	TXNX02	

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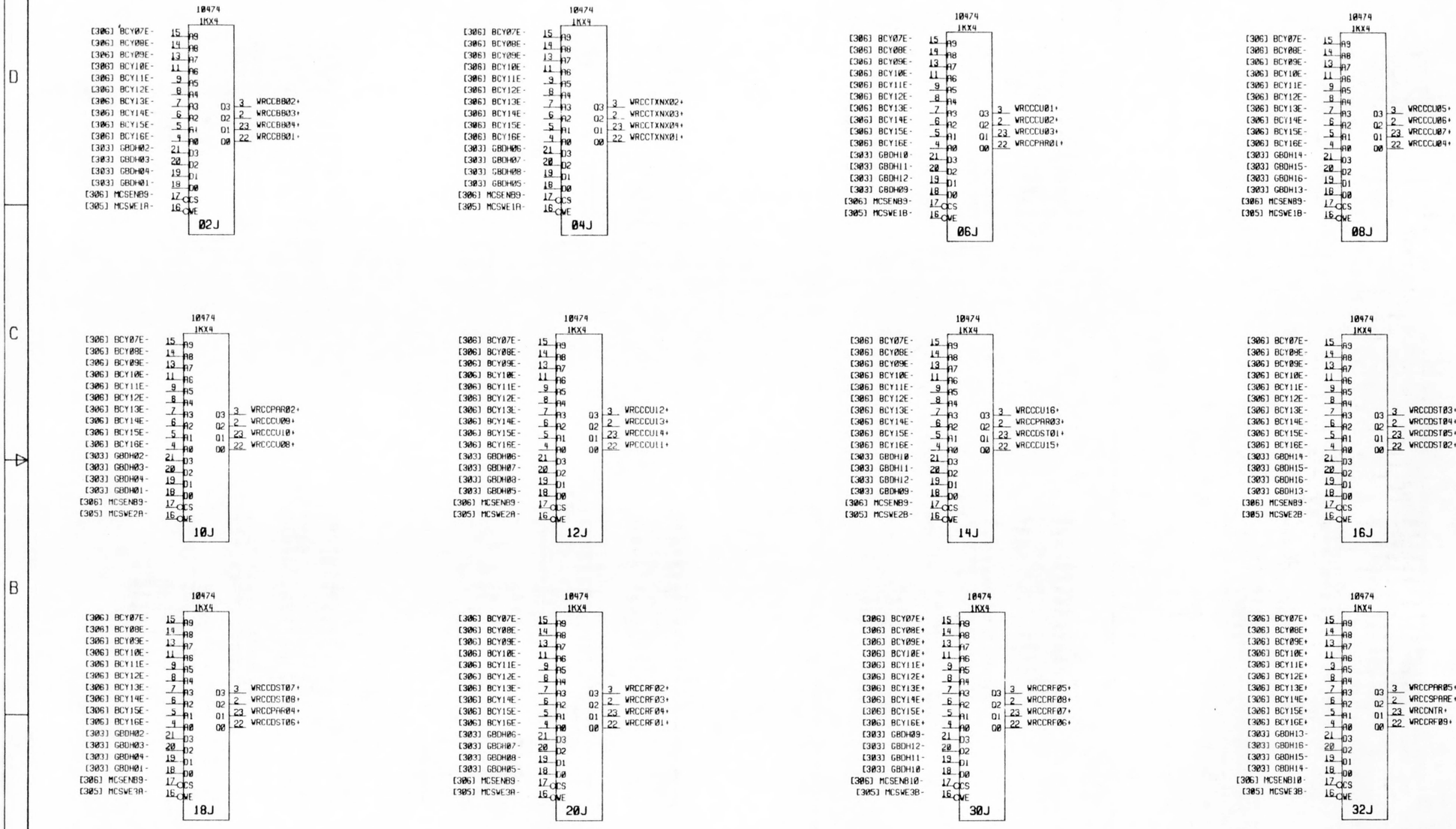
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

BCY DRIVERS. 5TH K OF CONTROL STORE

SHEET 15 OF 29 | SIZE D | DWG NO LBD6701 | REV 6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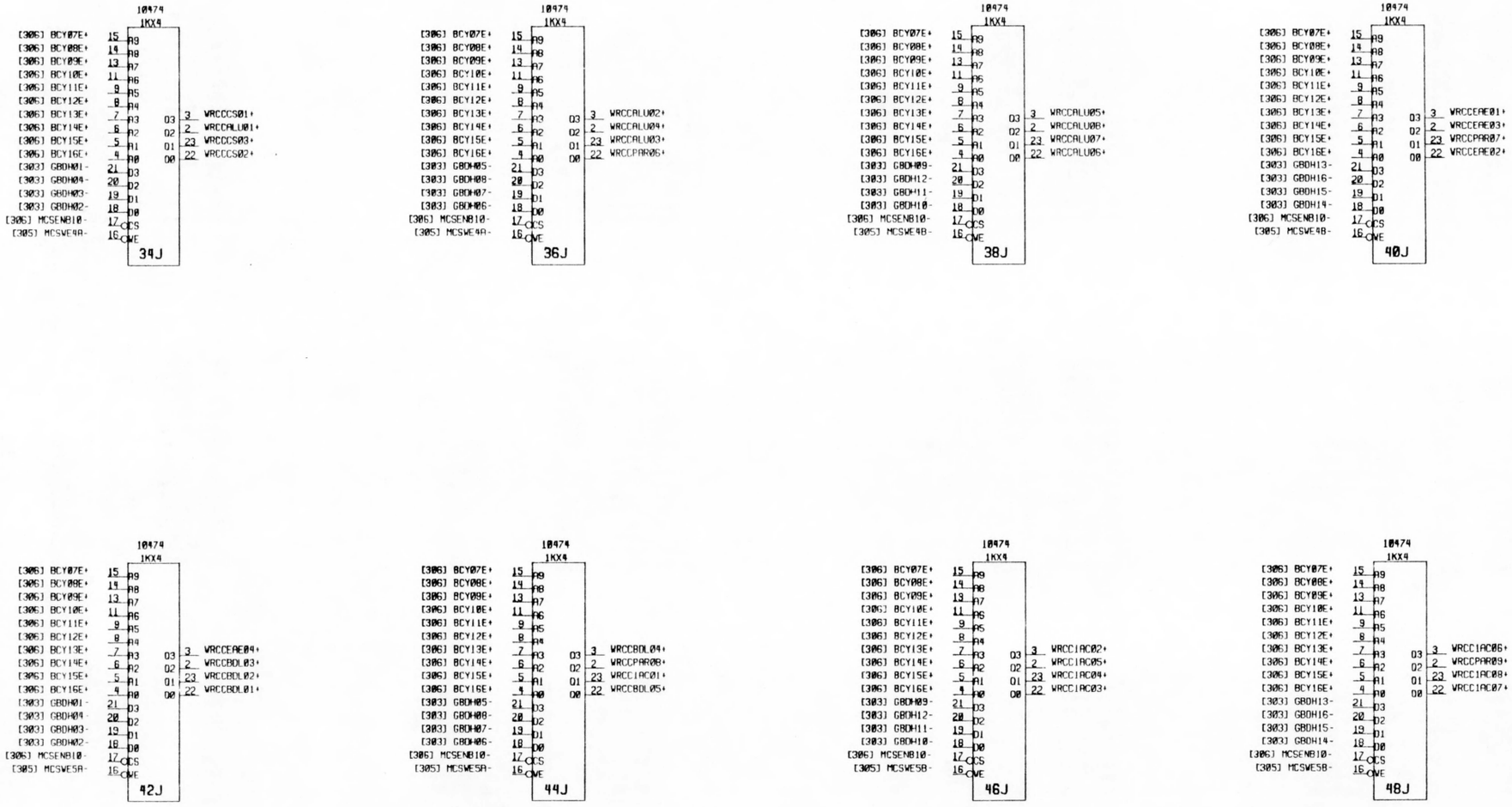
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
5TH K OF CONTROL STORE
SHEET 16 OF 29
SIZE D
DWG NO L8D6701
REV 4



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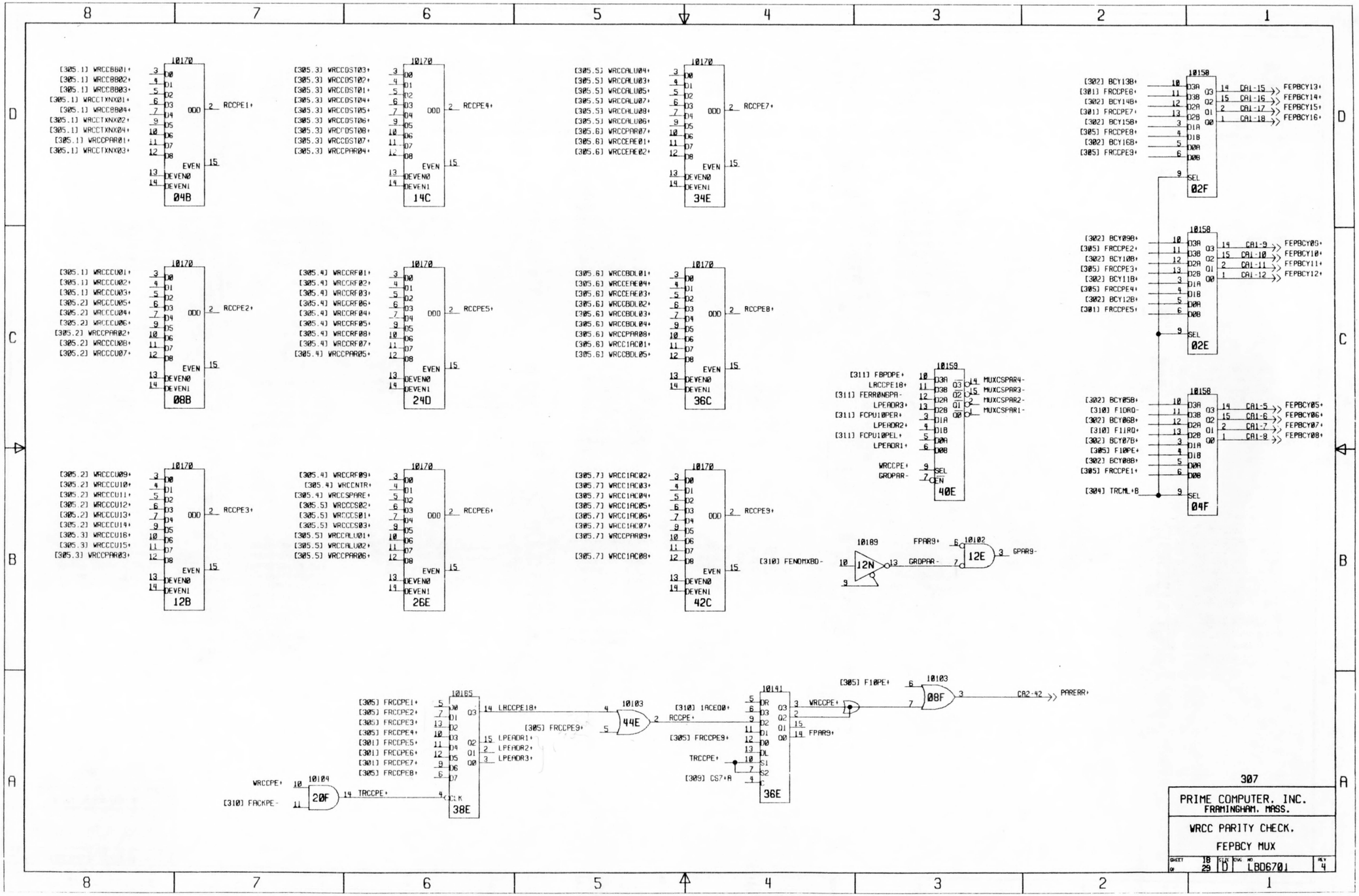
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

5TH K OF CONTROL STORE

SHEET 17 OF 29 | SIZE D | DWG. NO LBD6701 | REV 4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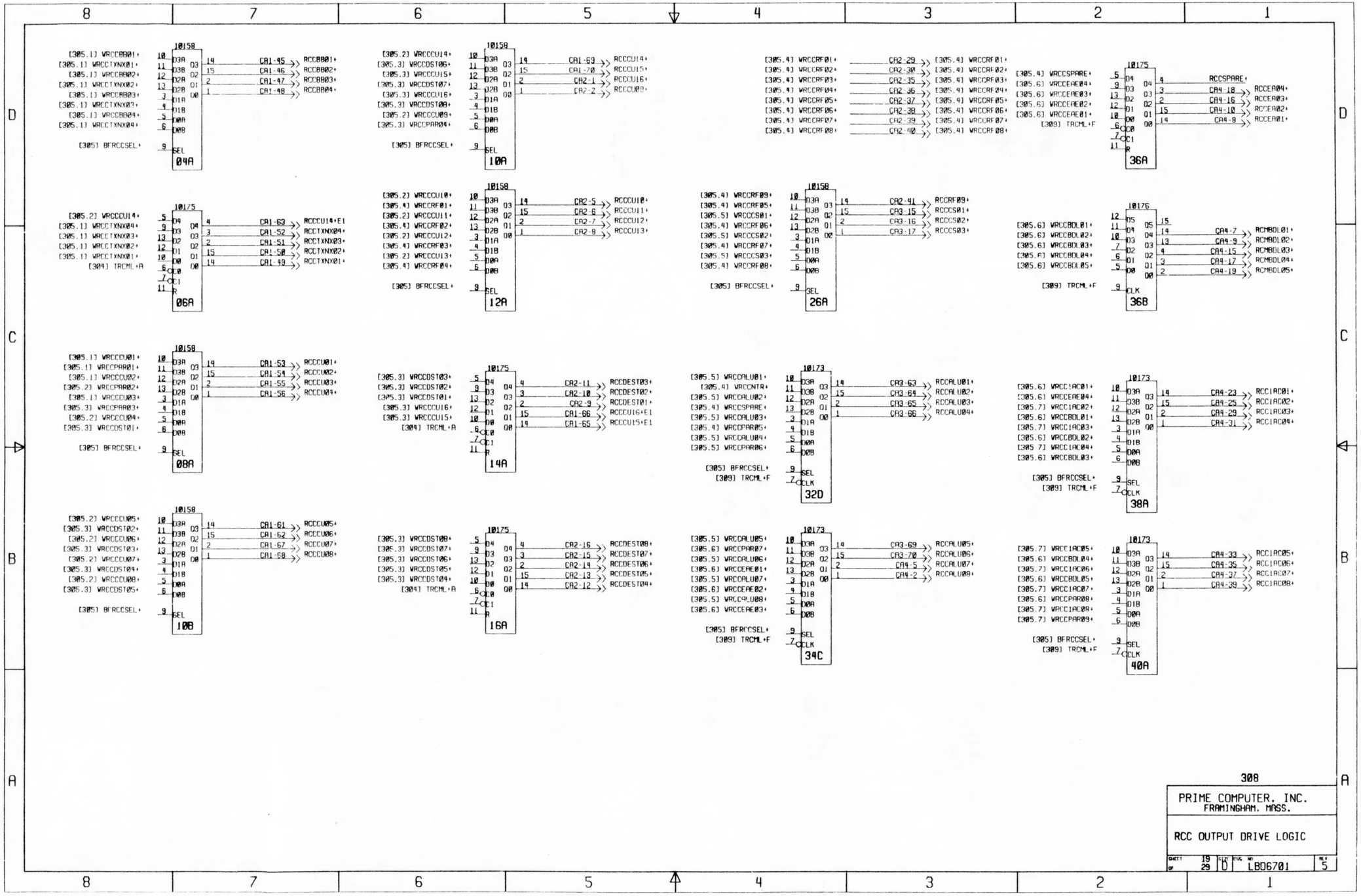
307
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
WRCC PARITY CHECK.
FEPBCY MUX
SHEET 18 OF 29
SIZE D
DWG NO LBD6701
REV 4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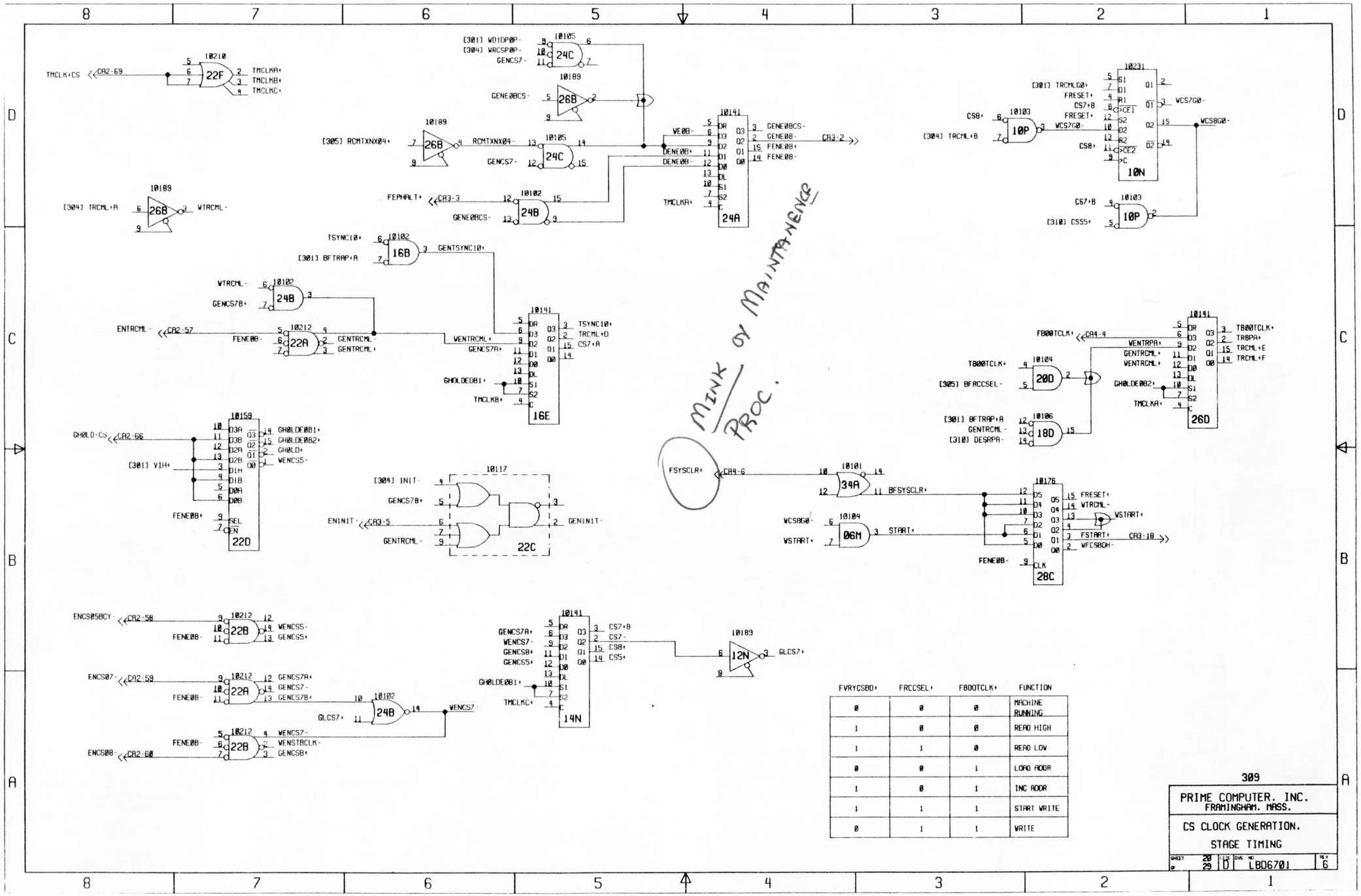
308
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
RCC OUTPUT DRIVE LOGIC
SHEET OF 19 29
SIZE D
DWG NO LBD6701
REV 5



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1	0	0	READ HIGH
1	1	0	READ LOW
0	0	1	LOAD ADDR
1	0	1	INC ADDR
1	1	1	START WRITE
0	1	1	WRITE

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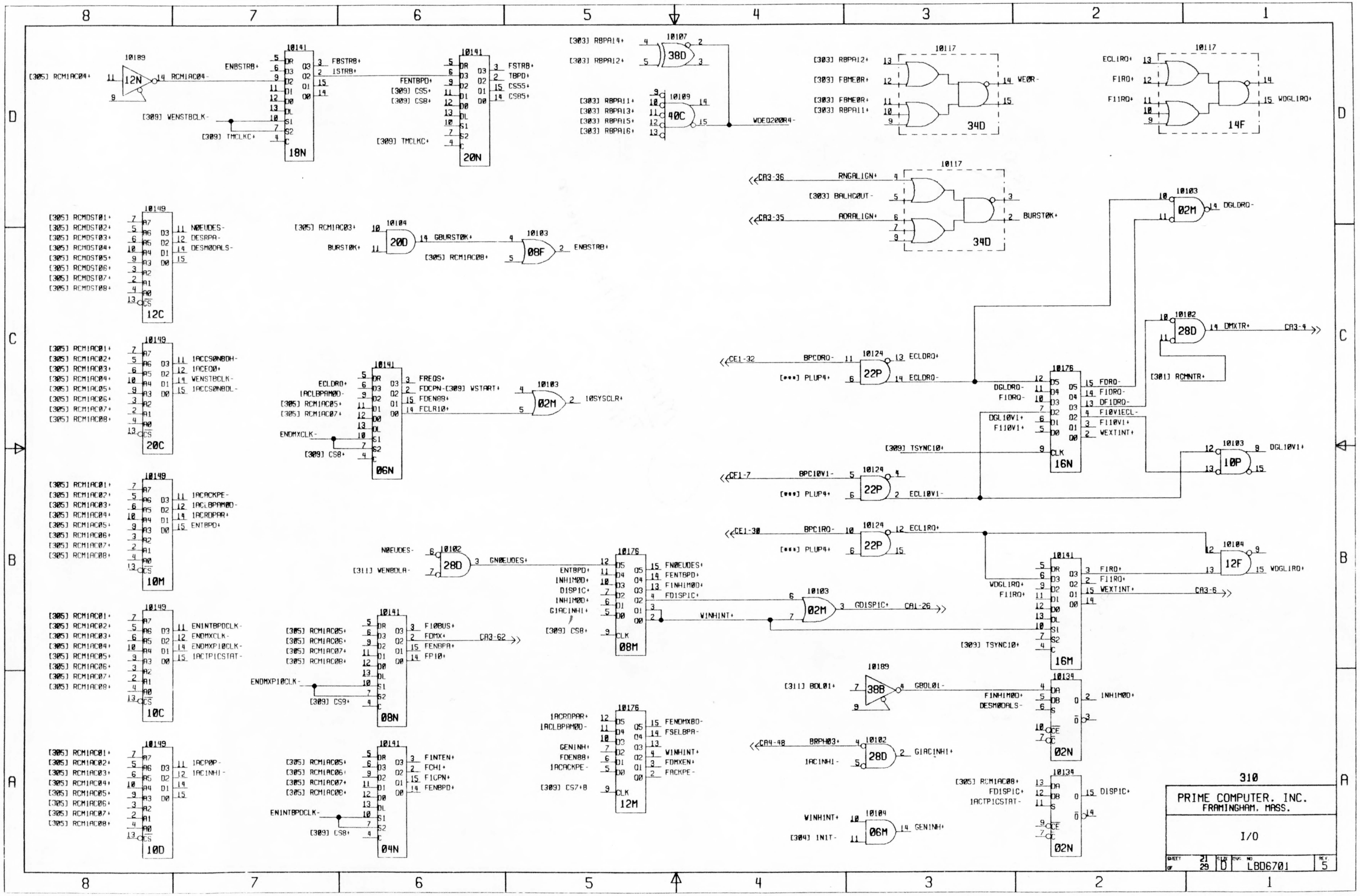
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

CS CLOCK GENERATION.
STAGE TIMING

SHEET OF	SIZE	DWG. NO	REV
20 29	D	LBD6701	6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PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I/O
21
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LBD6701
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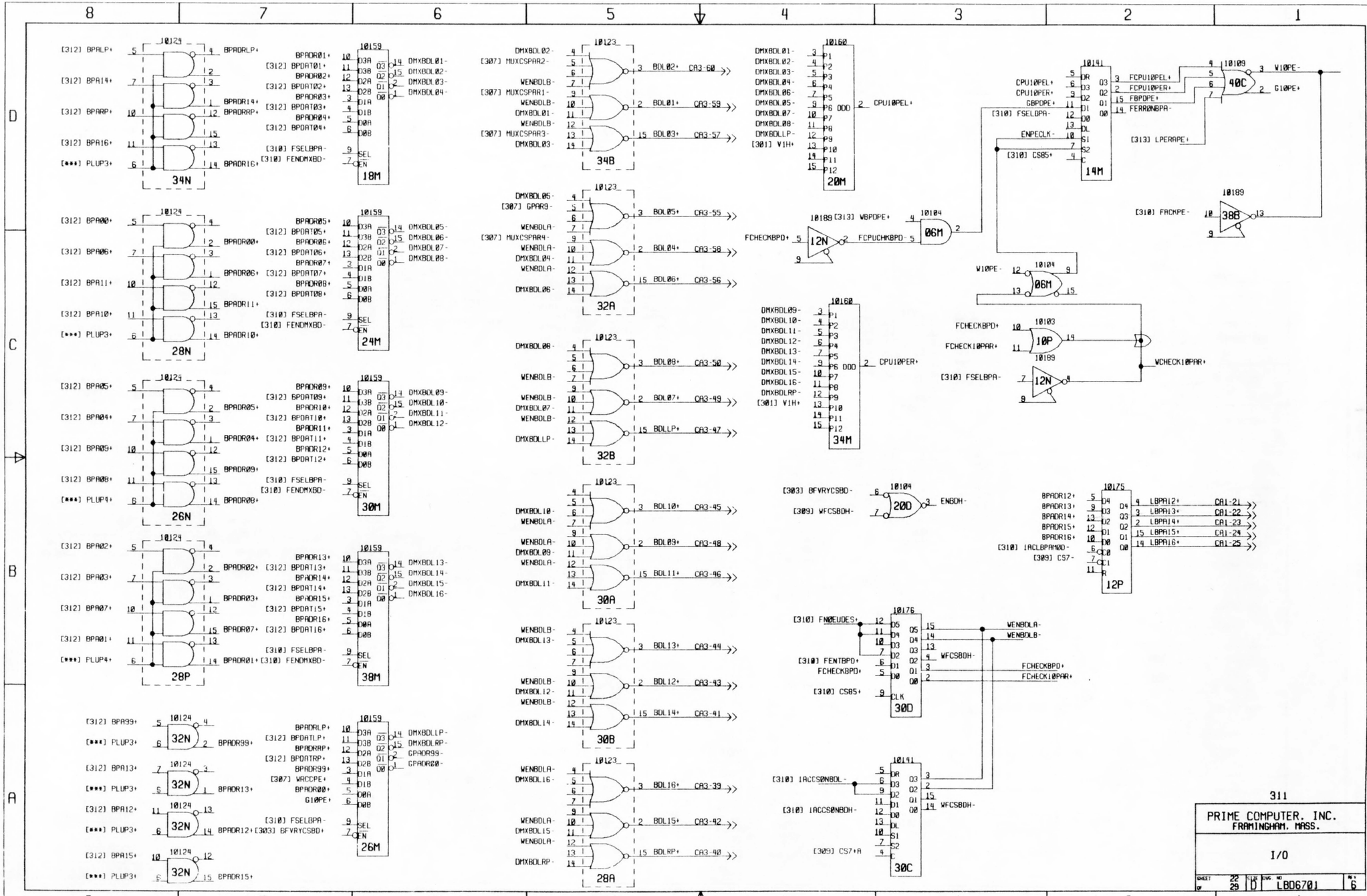
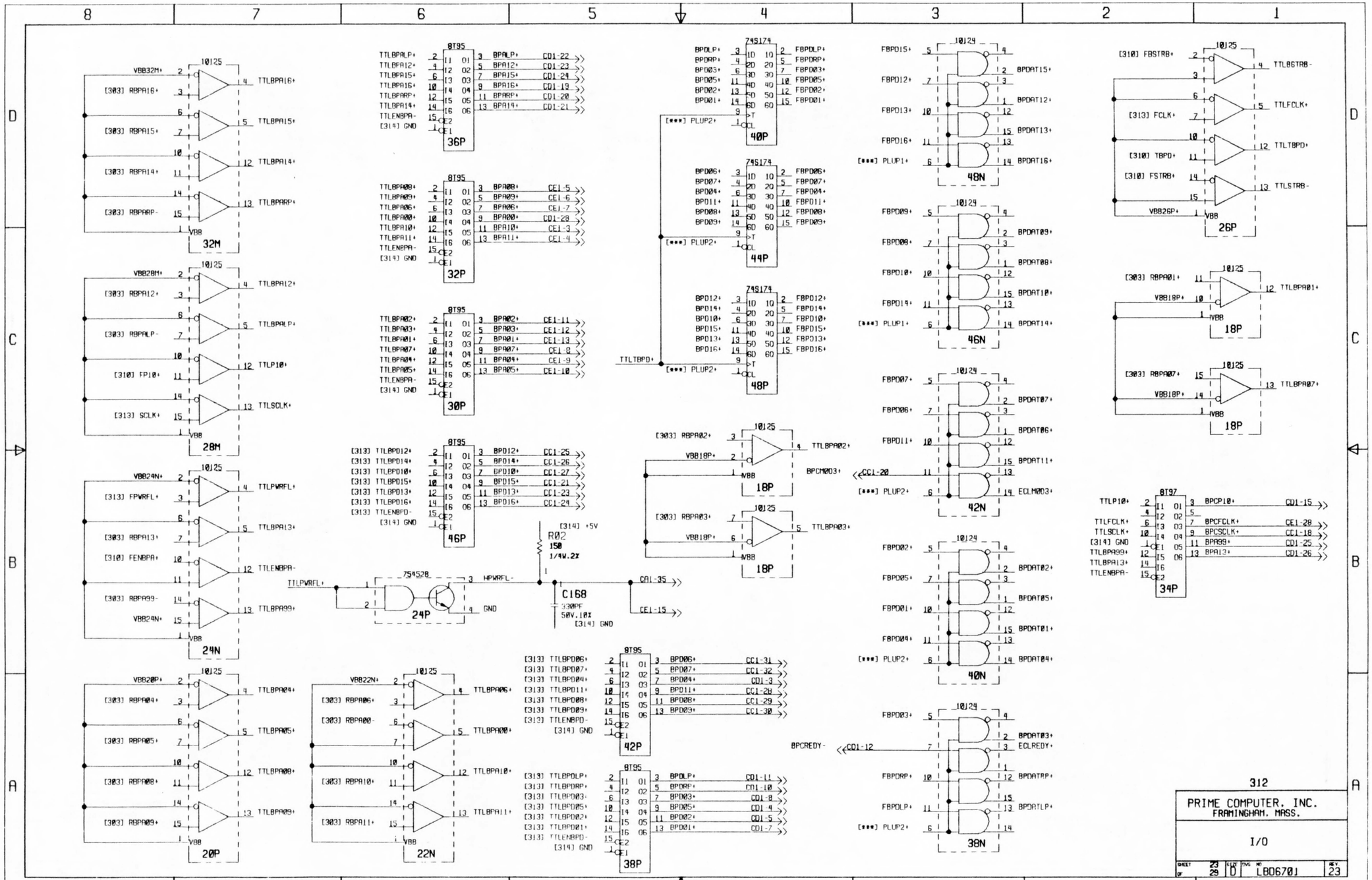
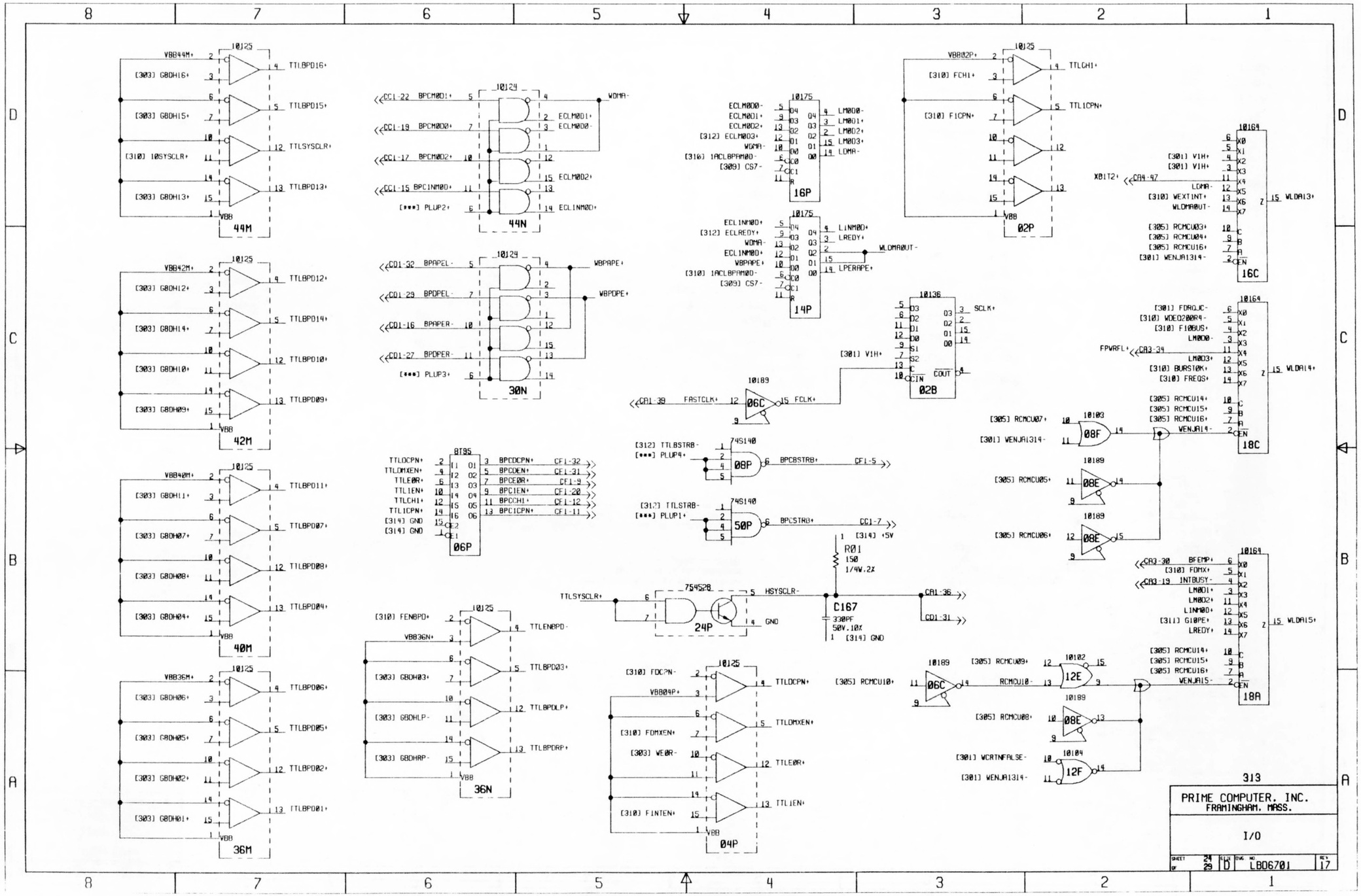

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I/O
LBD6701
311


8T95
36P
8T95
32P
8T95
30P
8T95
46P
74S174
40P
74S174
44P
74S174
48P
10125
32M
28M
24N
20P
22N
18P
18P
18P
10124
48N
46N
42N
40N
38N
8T97
34P
10125
26P
18P
18P
754528
24P
C168
330PF
50V.1%
R02
150
1/4W.2%
8T95
42P
8T95
38P
312
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I/O
LBD6701


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
I/O
313
LBD6701
SHEET 24 OF 29
SIZE D
REV 17
44M
44N
42M
30N
40M
06P
36M
36N
04P
16P
14P
02P
16C
02B
06C
08P
50P
C167
08F
08E
12E
12F
18C
18A
24P

CA1-1	+5V
CA1-2	+5V
CA1-13	GND
CA1-14	GND
CA1-27	-5.2V
CA1-28	-5.2V
CA1-29	-5.2V
CA1-30	-5.2V
CA1-43	-2V
CA1-44	-2V
CA1-57	GND
CA1-58	GND
CA1-59	GND
CA1-60	GND

CA2-3	GND
CA2-4	GND
CA2-17	-5.2V
CA2-18	-5.2V
CA2-19	-5.2V
CA2-20	-5.2V
CA2-33	-2V
CA2-34	-2V
CA2-47	GND
CA2-48	GND
CA2-61	GND
CA2-62	GND
CA2-63	GND
CA2-64	GND
CA2-67	GND
CA2-70	GND

CA3-1	GND
CA3-7	GND
CA3-8	GND
CA3-9	GND
CA3-10	GND
CA3-23	GND
CA3-24	GND
CA3-37	-2V
CA3-38	-2V
CA3-51	-5.2V
CA3-52	-5.2V
CA3-53	-5.2V
CA3-54	-5.2V
CA3-67	GND
CA3-68	GND

CA4-11	GND
CA4-12	GND
CA4-13	GND
CA4-14	GND
CA4-27	-2V
CA4-28	-2V
CA4-41	-5.2V
CA4-42	-5.2V
CA4-43	-5.2V
CA4-44	-5.2V
CA4-57	GND
CA4-58	GND
CA4-69	+5V
CA4-70	+5V

CC1-1	GND
CC1-2	GND
CC1-33	GND
CC1-34	GND

CD1-1	GND
CD1-2	GND
CD1-33	GND
CD1-34	GND

CE1-1	GND
CE1-2	GND
CE1-33	GND
CE1-34	GND

CF1-1	GND
CF1-2	GND
CF1-33	GND
CF1-34	GND

C161 22 15V 10% : +5V — 1 — 2 — GND

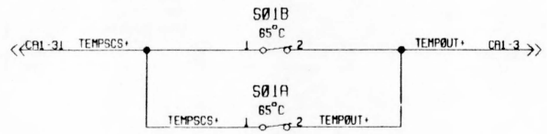
C162 22 15V 10% : GND — 1 — 2 — -2V

C163 22 15V 10% : GND — 1 — 2 — -5.2V

C164 22 15V 10% : GND — 1 — 2 — -2V

C165 22 15V 10% : GND — 1 — 2 — -5.2V

C166 22 15V 10% : +5V — 1 — 2 — GND



ONLY ONE TEMPERATURE SENSOR WILL BE IN THE BOARD

NOTES :

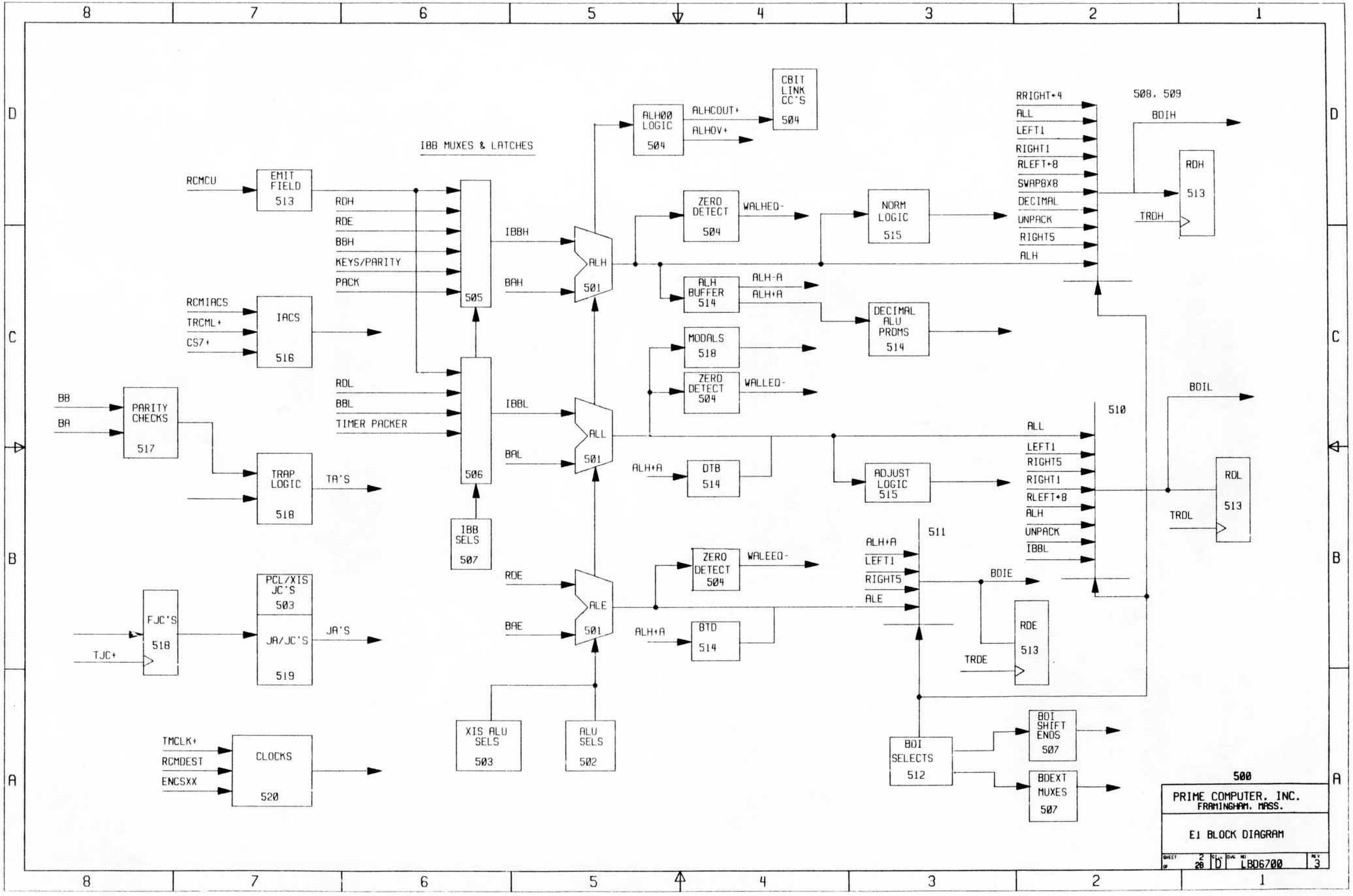
1. .01 UF AXIAL LEAD CAPACITORS ARE NOT SHOWN BUT ARE INSTALLED ADJACENT TO ALL DIPS IN THE FOLLOWING COLUMNS : A.C.E.G.J EXCEPT 16J AND TOOLING HOLE AT 38J. L. AND N.

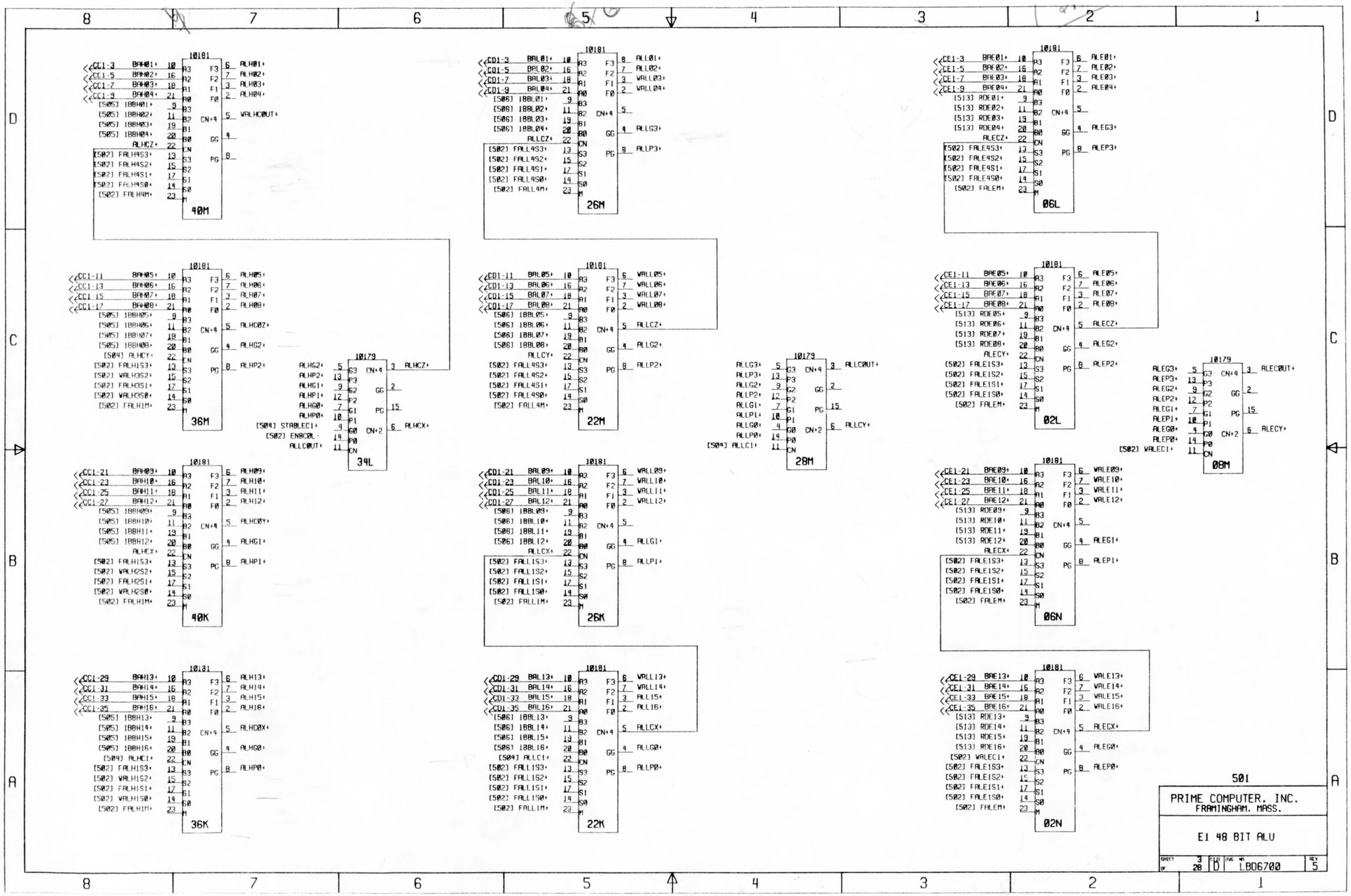
2. UNLESS OTHERWISE SPECIFIED : RESISTANCE VALUES ARE IN OHMS CAPACITANCE VALUES ARE IN MICROFARADS.

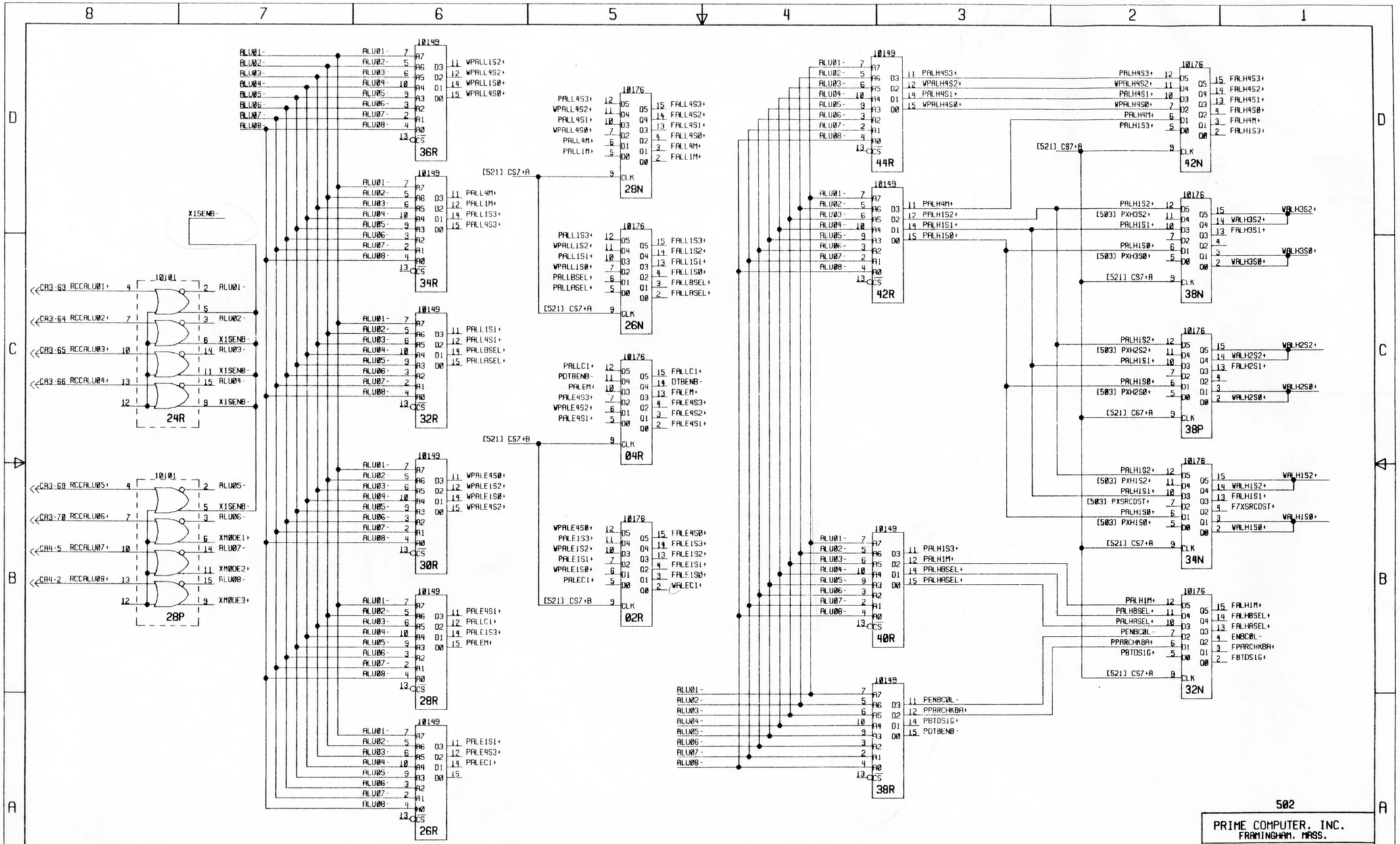
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

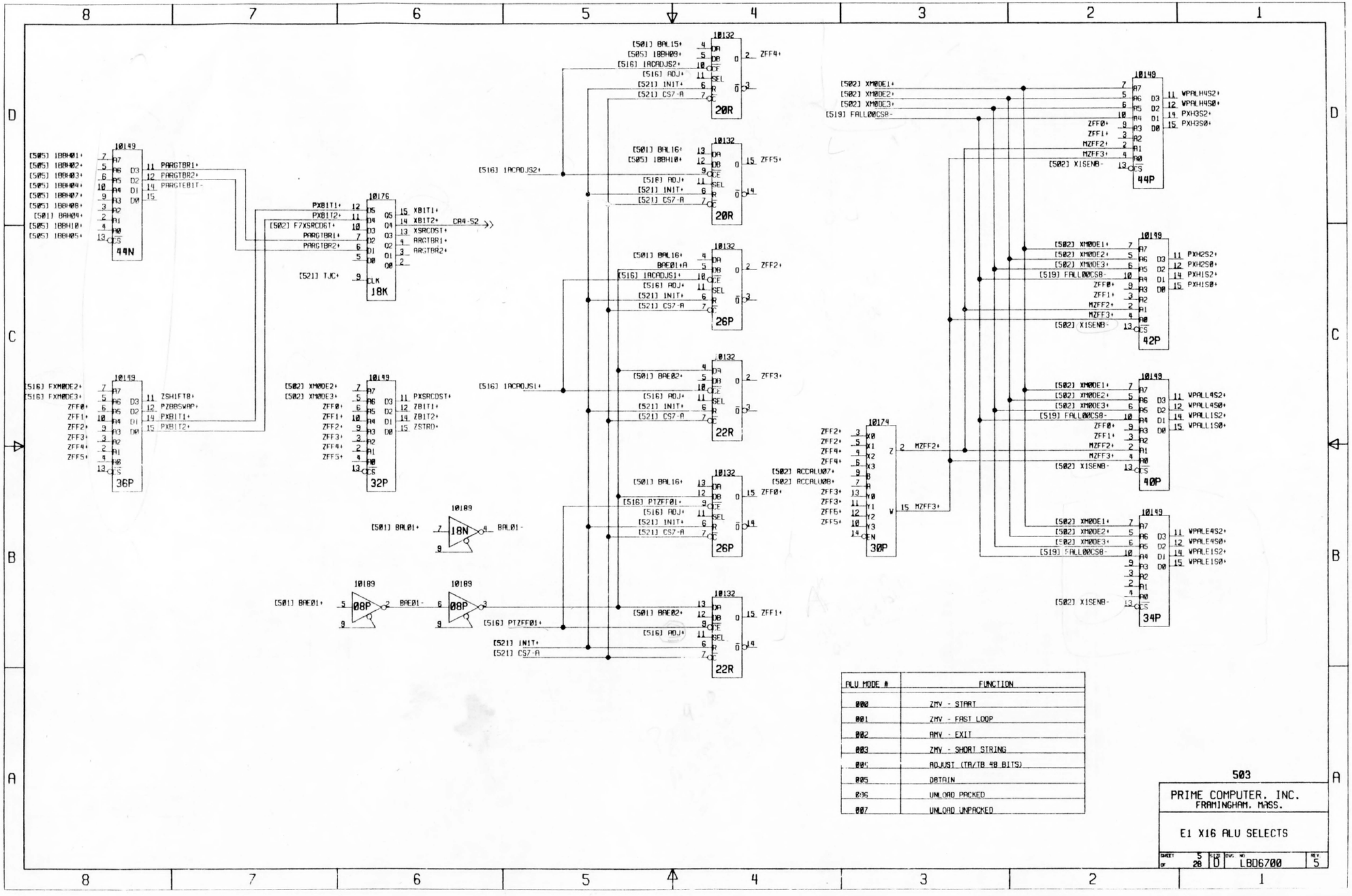
MISC. CONNECTOR ASSIGNMENTS

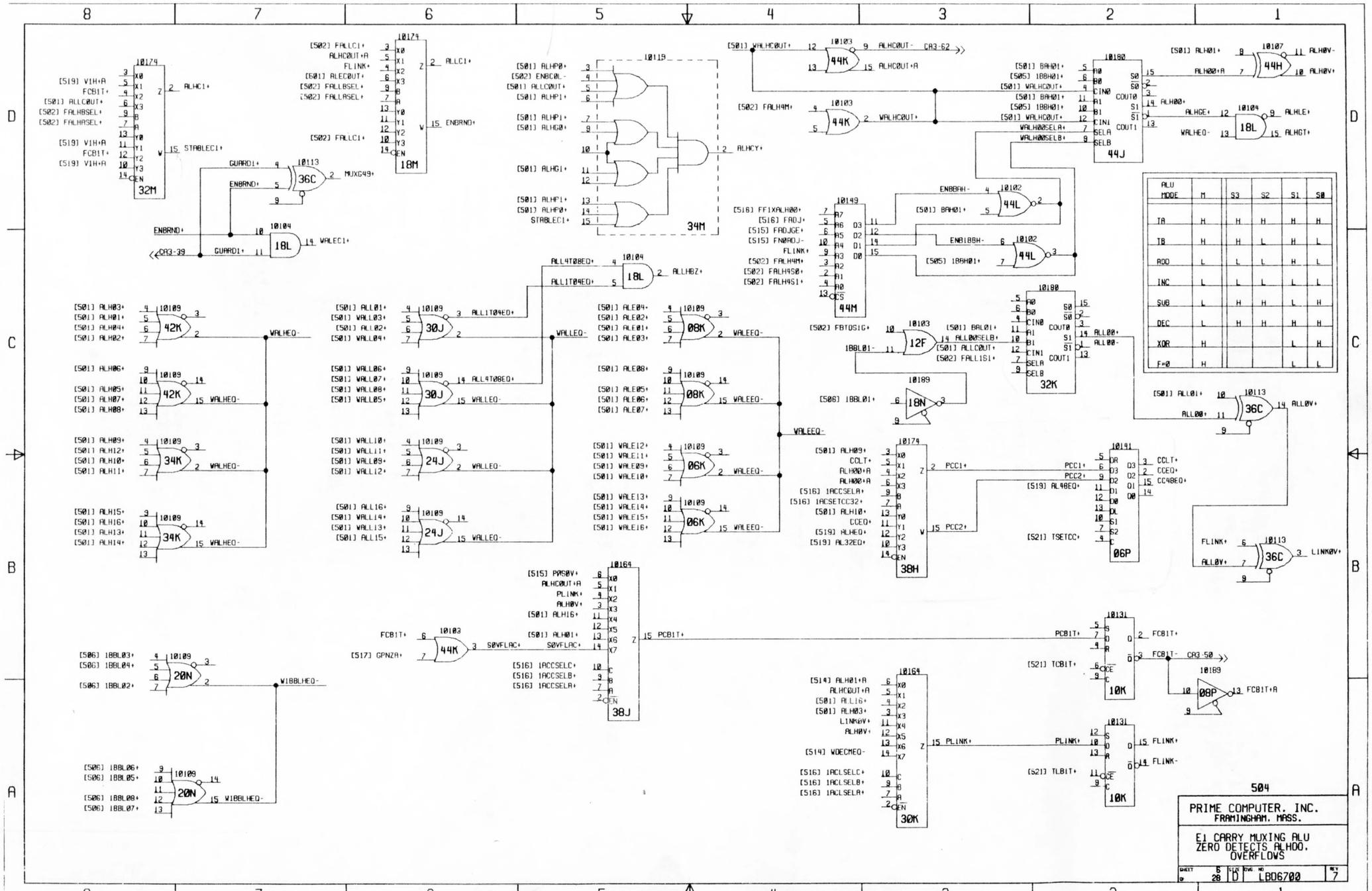
SHEET OF	SIZE	DWG NO	REV
25 29	D	LBD6701	10

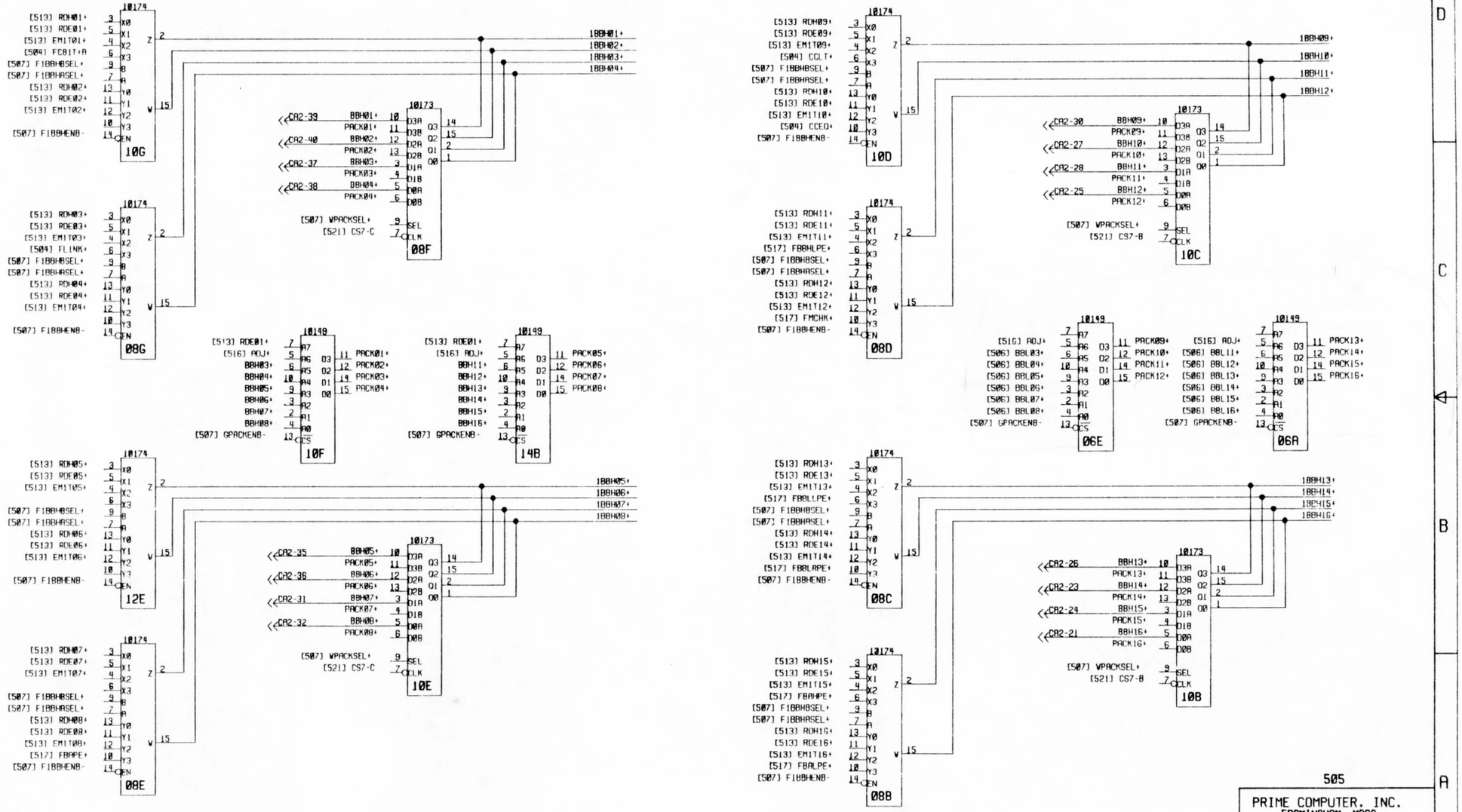

IBB MUXES & LATCHES
RCMCU
EMIT FIELD 513
RDH
RDE
BBH
KEYS/PARITY
PACK
505
IBBH
BAH
ALH 501
ALH00 LOGIC 504
ALHCOUT+
ALHOV+
CBIT LINK CC'S 504
ZERO DETECT 504
WALHEQ-
NORM LOGIC 515
RRIGHT+4
ALL
LEFT1
RIGHT1
RLEFT+8
SWAP8X8
DECIMAL
UNPACK
RIGHT5
ALH
508, 509
BDIH
RDH 513
TRDH
ALH BUFFER 514
ALH-A
ALH+A
DECIMAL ALU PROMS 514
RCM1ACS
TRCML+
CS7+
IACS 516
MODALS 518
ZERO DETECT 504
WALLEQ-
RDL
BBL
TIMER PACKER
506
IBBL
BAL
ALL 501
BB
BA
PARITY CHECKS 517
TRAP LOGIC 518
TA'S
IBB SELS 507
ALH+A
DTB 514
ADJUST LOGIC 515
510
BDIL
RDL 513
TRDL
ALL
LEFT1
RIGHT5
RIGHT1
RLEFT+8
ALH
UNPACK
IBBL
RDE
BAE
ALE 501
ZERO DETECT 504
WALEEQ-
ALH+A
BTD 514
511
ALH+A
LEFT1
RIGHT5
ALE
BDIE
RDE 513
TRDE
FJC'S 518
TJC+
PCL/XIS JC'S 503
JA/JC'S 519
JA'S
XIS ALU SELS 503
ALU SELS 502
TMCLK+
RCMDEST
ENCSXX
CLOCKS 520
BDI SELECTS 512
BDI SHIFT ENDS 507
BDEXT MUXES 507
500
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 BLOCK DIAGRAM
SHEET 2 OF 28
SIZE D
DWG NO LBD6700
REV 3

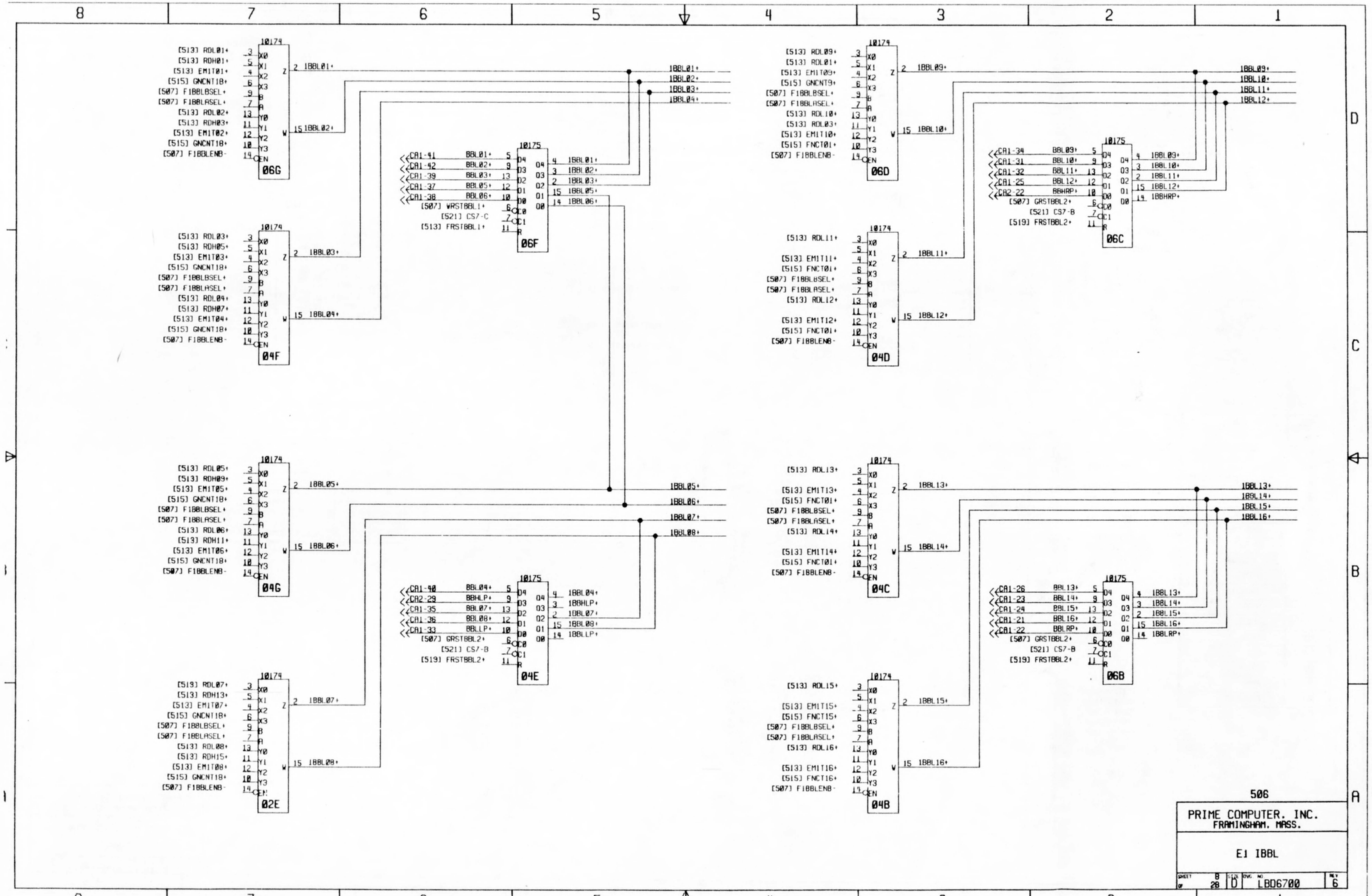

10181
40M
36M
34L
40K
36K
26M
22M
26K
22K
10179
28M
06L
02L
08M
06N
02N
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 48 BIT ALU
501
SHEET 3 OF 28
SIZE D
DWG NO L.BD6700
REV 5

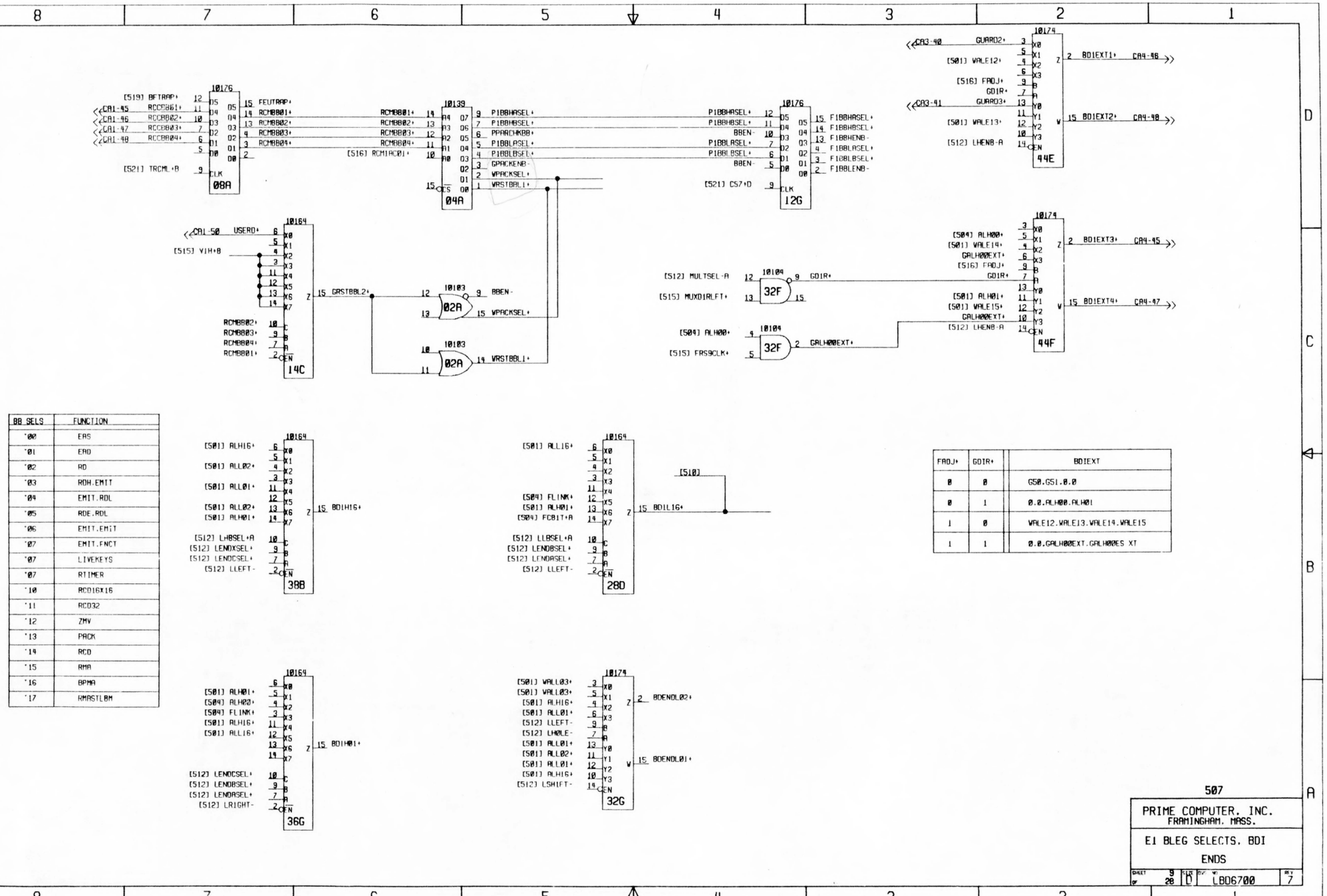

10149
36R
34R
32R
30R
28R
26R
10101
24R
28P
10176
28N
26N
04R
02R
44R
42R
40R
38R
42N
38N
38P
34N
32N
X1SENB-
[521] CS7+A
[521] CS7+B
[521] C97+A
[521] C67+A
[521] CS7+A
[503] PXH3S2+
[503] PXH3S0+
[503] PXH2S2+
[503] PXH2S0+
[503] PXH1S2+
[503] PXH1S0+
[503] PXSRCDST+
502
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 ALU SELECTS
SHEET 4 OF 28
SIZE D
DWG NO LBD6700
REV 7


49N
36P
18K
32P
18N
08P
08P
20R
20R
26P
22R
26P
22R
44P
42P
40P
34P
30P
CR4-52
ALU MODE #
FUNCTION
000 ZMV - START
001 ZMV - FAST LOOP
002 AMV - EXIT
003 ZMV - SHORT STRING
004 ADJUST (TA/TB 48 BITS)
005 OBTAIN
006 UNLOAD PACKED
007 UNLOAD UNPACKED
503
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 X16 ALU SELECTS
SHEET 5 OF 28
SIZE D
DWG NO LBD6700
REV 5


32M
18M
36C
18L
34M
44K
44H
44J
44L
12F
18N
44M
32K
42K
30J
08K
34K
24J
06K
38H
06P
20N
38J
10K
08P
30K
PRIME COMPUTER. INC.
FRAMINGHAM. MASS.
E1 CARRY MUXING ALU
ZERO DETECTS ALH00.
OVERFLOWS
LBD6700
504


10G
08G
10F
08F
10E
08E
12E
10D
08D
10C
06E
06A
08C
10B
08B
14B
505
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
EI IBBH
LBD6700
REV 4


06G
06F
06D
06C
04F
04D
04G
04C
04E
06B
02E
04B
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 IBBL
506
LBD6700



BB SELS	FUNCTION
'00	EAS
'01	EAD
'02	RD
'03	RDH.EMIT
'04	EMIT.RDL
'05	RDE.RDL
'06	EMIT.EMIT
'07	EMIT.FNCT
'07	LIVEKEYS
'07	RTIMER
'10	RCD16X16
'11	RCD32
'12	ZMV
'13	PACK
'14	RCD
'15	RMA
'16	BPMA
'17	RMASTLBM

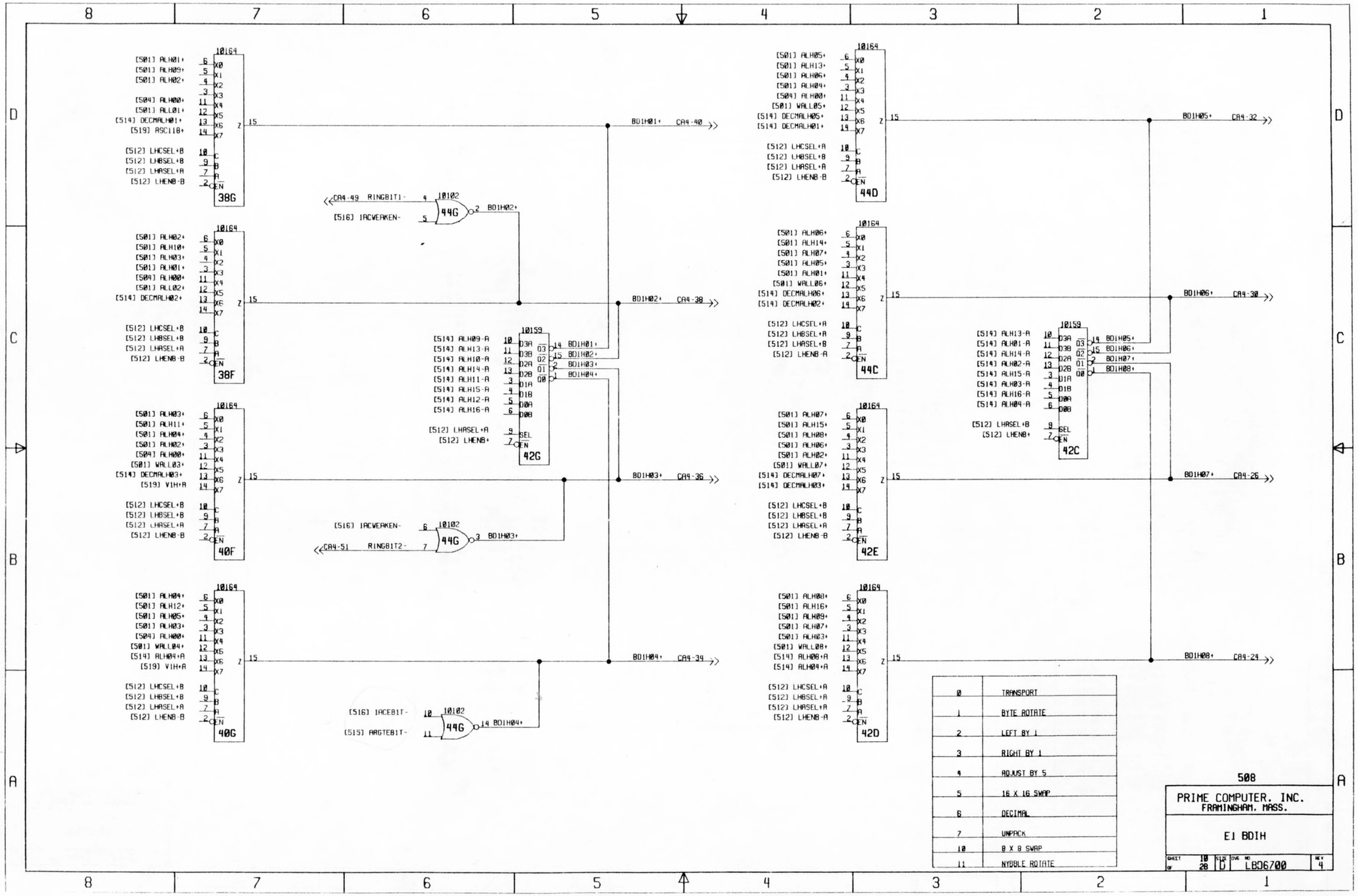
FADJ+	GDIR+	BDIEXT
0	0	G50.G51.0.0
0	1	0.0.ALH00.ALH01
1	0	VALE12.VALE13.VALE14.VALE15
1	1	0.0.GALH00EXT.GALH00ES XT

507

PRIME COMPUTER. INC.
FRAMINGHAM. MASS.

E1 BLEG SELECTS. BDI
ENDS

SHEET 9 OF 28 | SIZE D | DWG LBD6700 | REV 7


8
7
6
5
4
3
2
1
D
C
B
A
10164
38G
[501] ALH01+
[501] ALH09+
[501] ALH02+
[504] ALH00+
[501] ALL01+
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[519] ASCII8+
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[512] LHBSEL+B
[512] LHASEL+A
[512] LHENB-B
BD1H01+
CA4-40
38F
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[501] ALH10+
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[504] ALH00+
[501] ALL02+
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BD1H02+
CA4-38
40F
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[501] ALH11+
[501] ALH04+
[501] ALH02+
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BD1H03+
CA4-36
40G
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BD1H04+
CA4-34
10102
44G
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[CA4-51] RINGBIT2-
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10159
42G
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44D
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BD1H05+
CA4-32
44C
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BD1H06+
CA4-30
42C
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42E
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BD1H07+
CA4-26
42D
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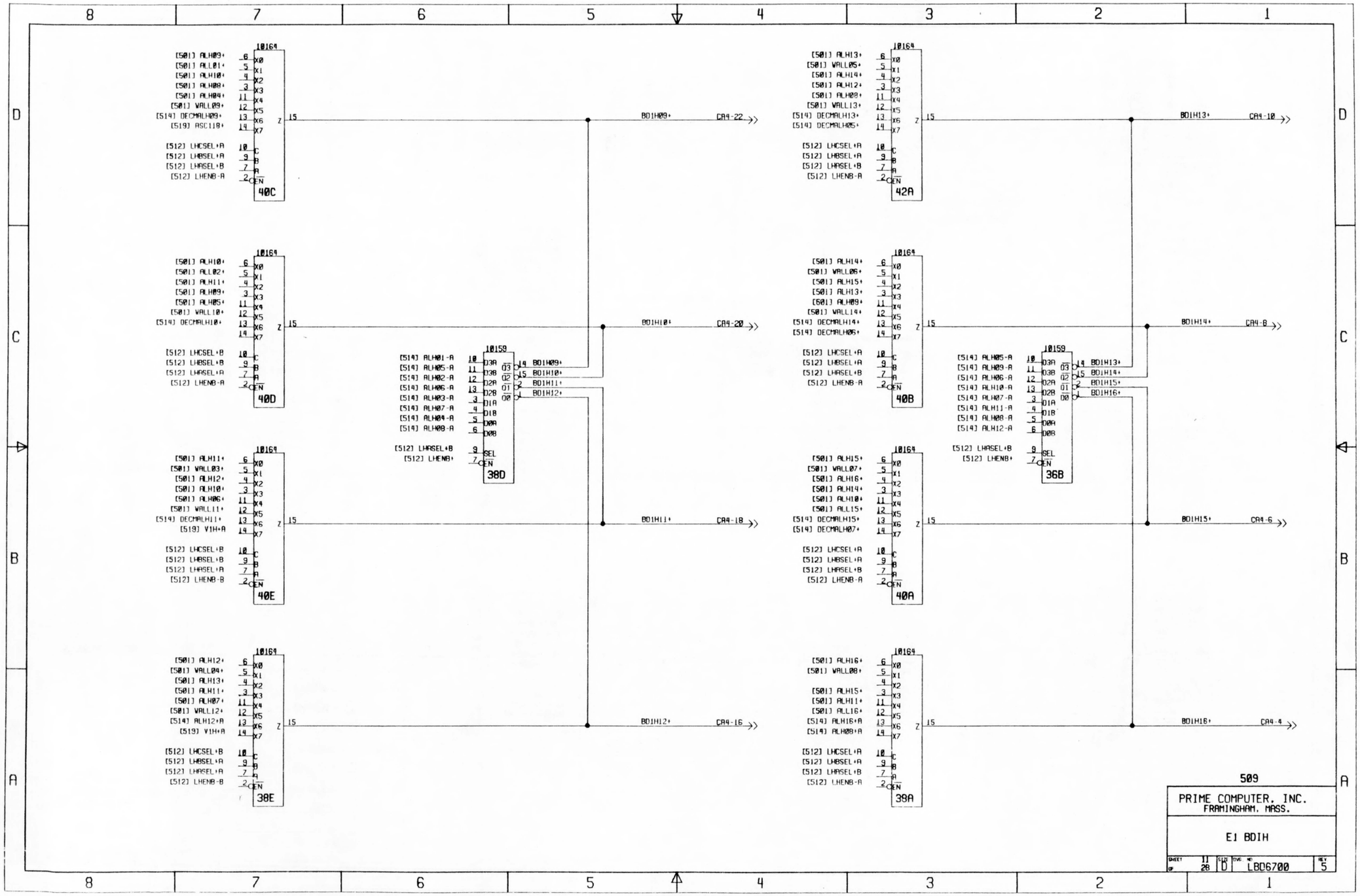
BD1H08+
CA4-24
0 TRANSPORT
1 BYTE ROTATE
2 LEFT BY 1
3 RIGHT BY 1
4 ADJUST BY 5
5 16 X 16 SWAP
6 DECIMAL
7 UNPACK
10 8 X 8 SWAP
11 NYBBLE ROTATE
508
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 BDIH
SHEET 10 OF 28
SIZE D
DWG NO LBD6700
REV 4


8
7
6
5
4
3
2
1
D
C
B
A
10164
40C
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BD1H09+
CA9-22
10164
42A
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BD1H13+
CA9-10
10164
40D
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BD1H10+
CA9-20
10159
38D
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[514] ALH08-A
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BD1H09+
BD1H10+
BD1H11+
BD1H12+
10164
40B
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BD1H14+
CA9-8
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36B
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BD1H13+
BD1H14+
BD1H15+
BD1H16+
10164
40E
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BD1H11+
CA9-18
10164
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BD1H15+
CA9-6
10164
38E
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[501] ALH13+
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BD1H12+
CA9-16
10164
39A
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[501] VALL08+
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[501] ALH11+
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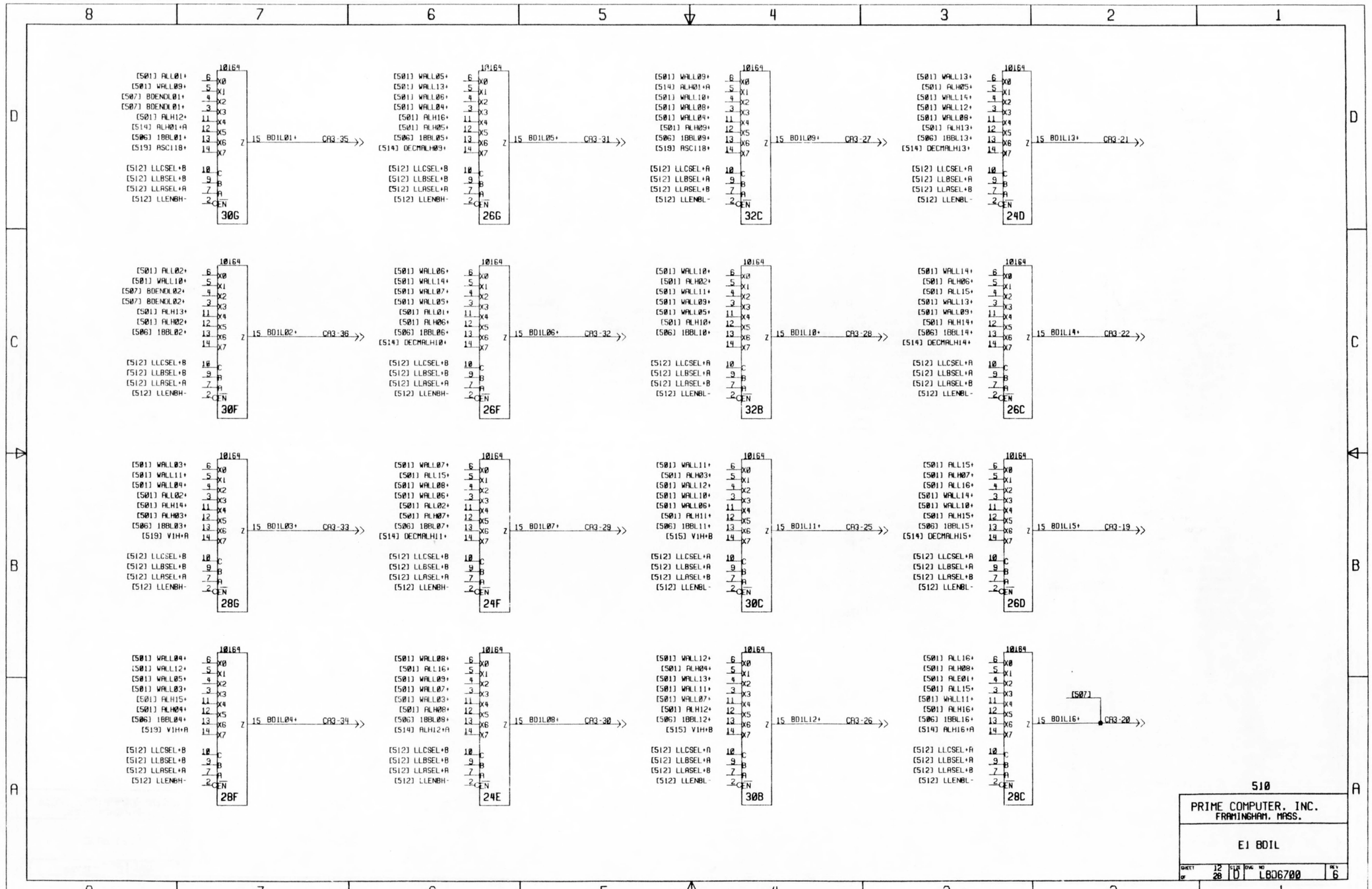
BD1H16+
CA9-4
509
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
EI BDIH
SHEET 11 OF 28
SIZE D
DWG NO LBD6700
REV 5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[519] ASCII8+
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[512] LLBSEL+B
[512] LLASEL+A
[512] LLENBH-
10164
30G
15 BD1L01+
CA3-35
[501] WALL05+
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[501] WALL06+
[501] WALL04+
[501] ALH16+
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[506] 1BBL05+
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10164
26G
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CA3-31
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28G
15 BD1L03+
CA3-33
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24F
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CA3-29
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26D
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28F
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CA3-30
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30B
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28C
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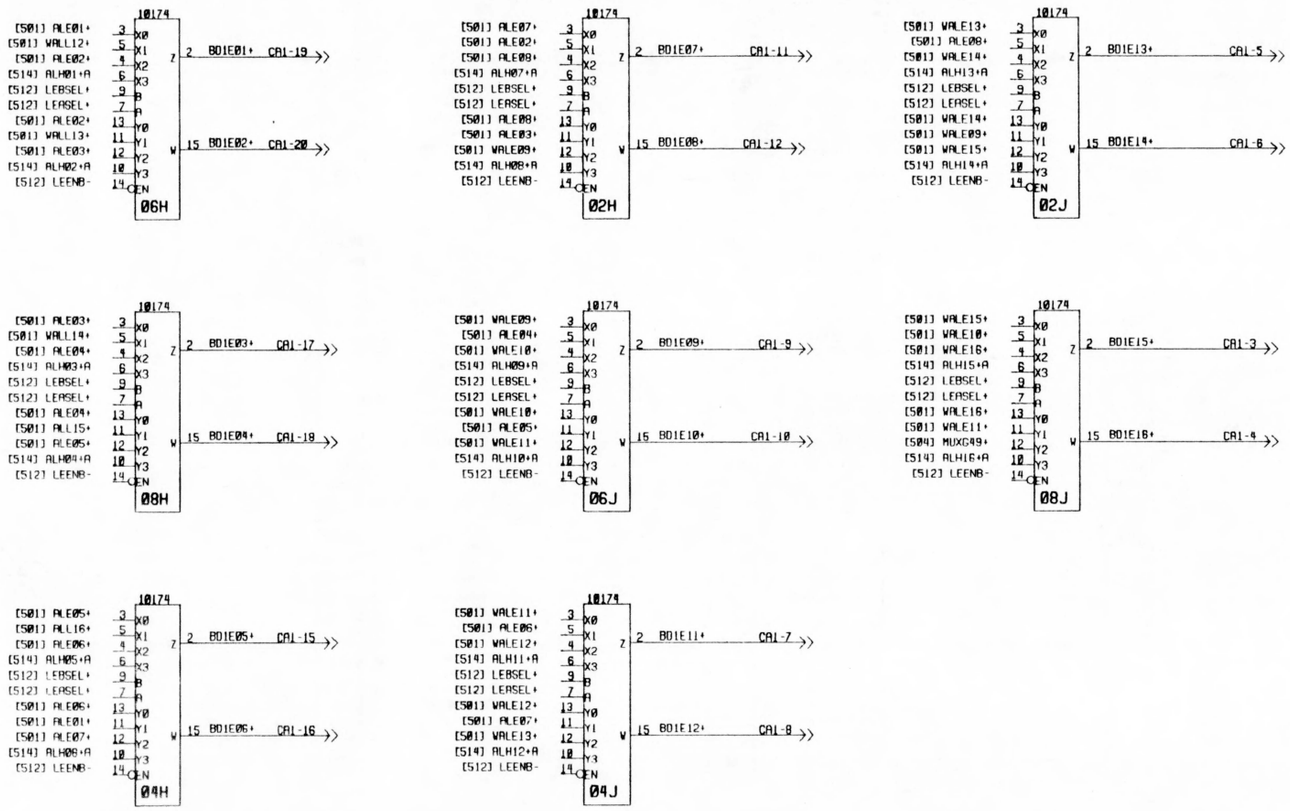
15 BD1L16+
CA3-20
510
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
EI BDIL
SHEET 12 OF 28
SIZE D
DWG NO LBD6700
REV 6

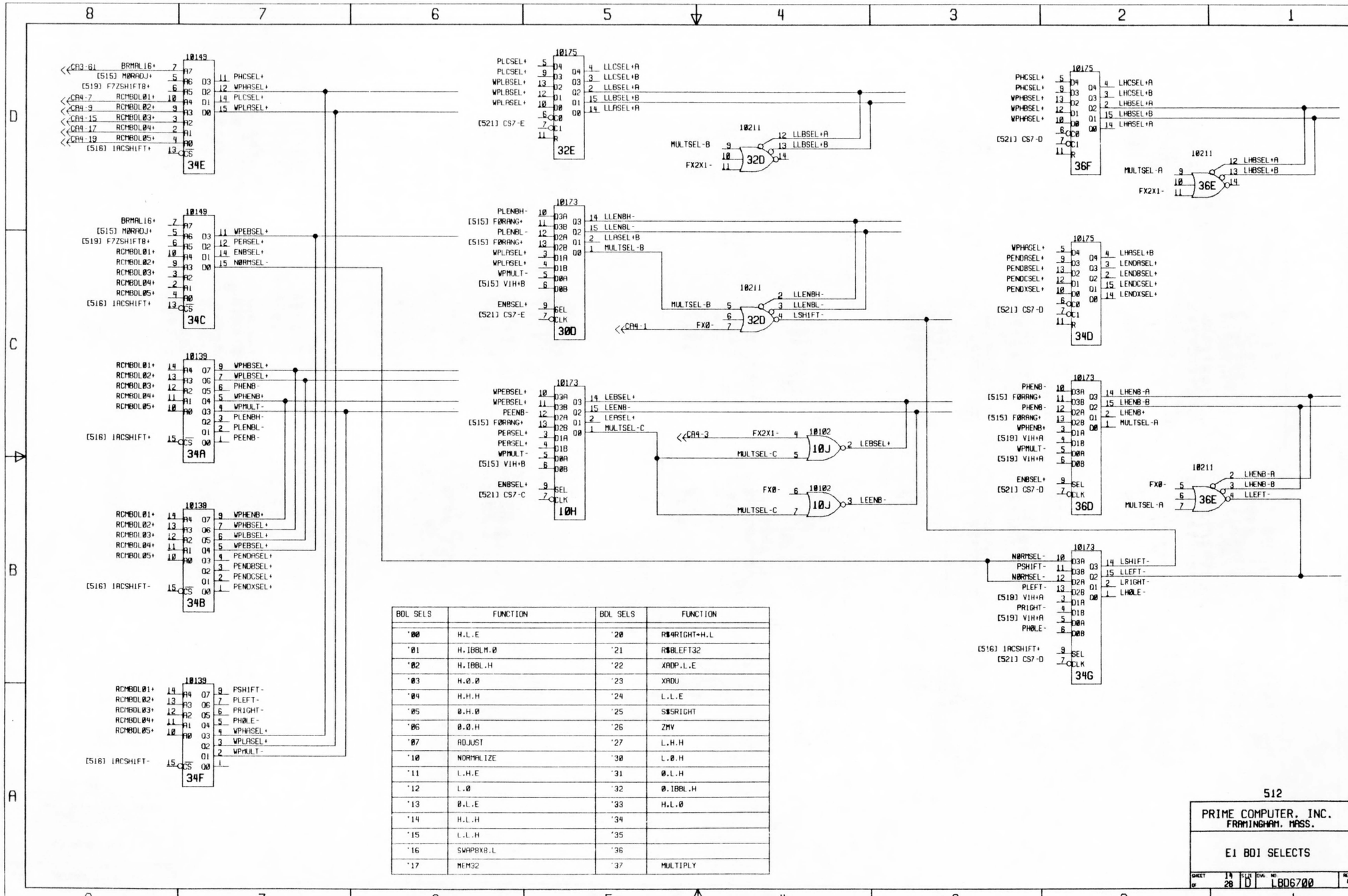


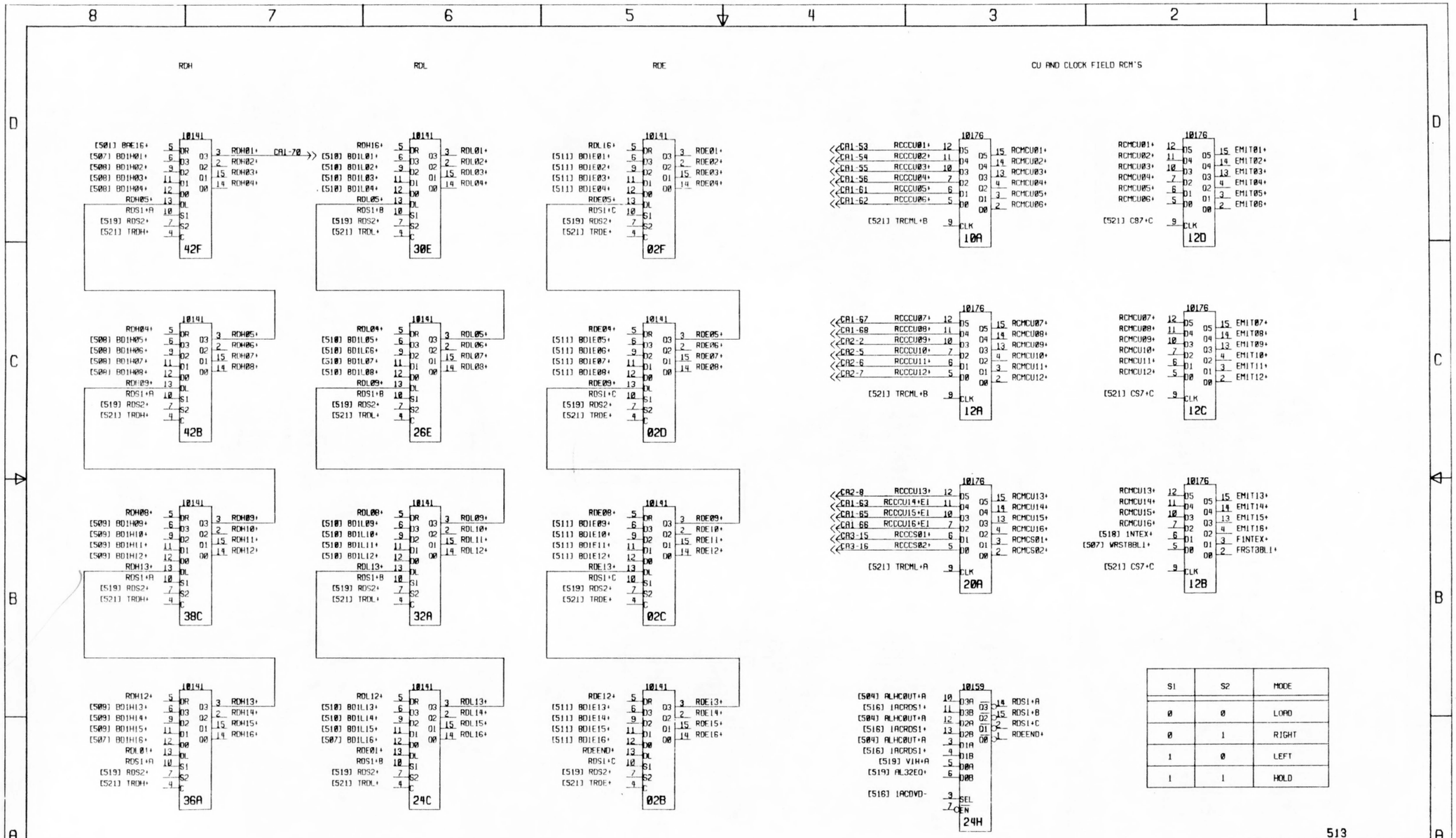
511

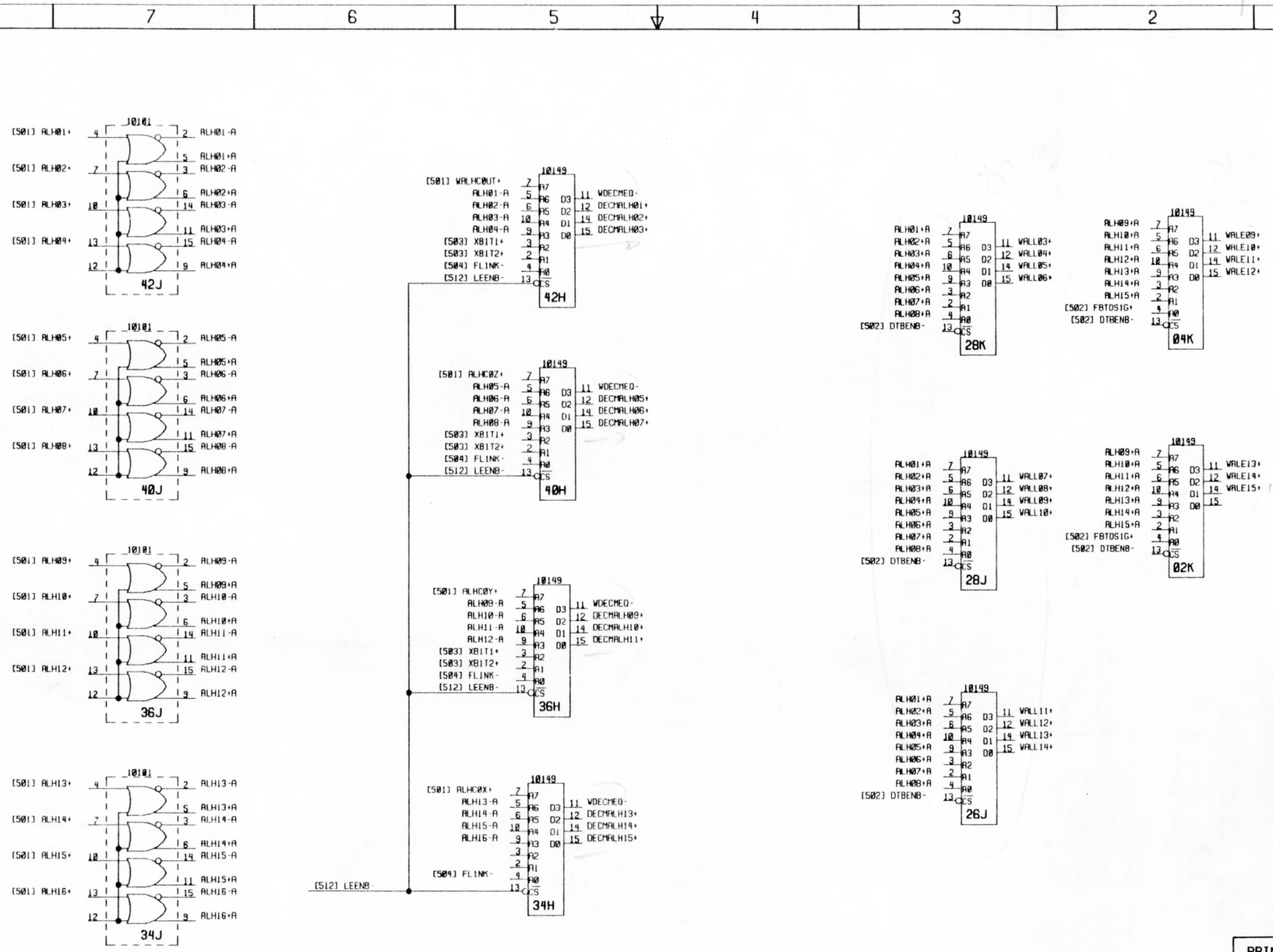
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E1 BDIE

SHEET OF	SIZE	DWG. NO	REV
13 28	D	LBD6700	4


34E
34C
34A
34B
34F
30D
32E
32D
36F
34D
36D
36E
34G
10H
10J
BDL SELS
FUNCTION
'00 H.L.E
'01 H.IBBLM.0
'02 H.IBBL.H
'03 H.0.0
'04 H.H.H
'05 0.H.0
'06 0.0.H
'07 ADJUST
'10 NORMALIZE
'11 L.H.E
'12 L.0
'13 0.L.E
'14 H.L.H
'15 L.L.H
'16 SWAP8X8.L
'17 MEM32
'20 R$4RIGHT+H.L
'21 R$8LEFT32
'22 XADP.L.E
'23 XADU
'24 L.L.E
'25 S$5RIGHT
'26 ZMV
'27 L.H.H
'30 L.0.H
'31 0.L.H
'32 0.IBBL.H
'33 H.L.0
'34
'35
'36
'37 MULTIPLY
512
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 BDI SELECTS
SHEET 19 OF 28
SIZE D
DWG NO L8D6700
REV 4


RDH
RDL
RDE
CU AND CLOCK FIELD RCM'S
42F
30E
02F
42B
26E
02D
38C
32A
02C
36A
24C
02B
10A
12D
12A
12C
20A
12B
24H
CA1-70
S1 S2 MODE
0 0 LOAD
0 1 RIGHT
1 0 LEFT
1 1 HOLD
513
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 RD, CU RCM'S
SHEET 15 OF 28
SIZE D
DWG NO LBD6700
REV 4

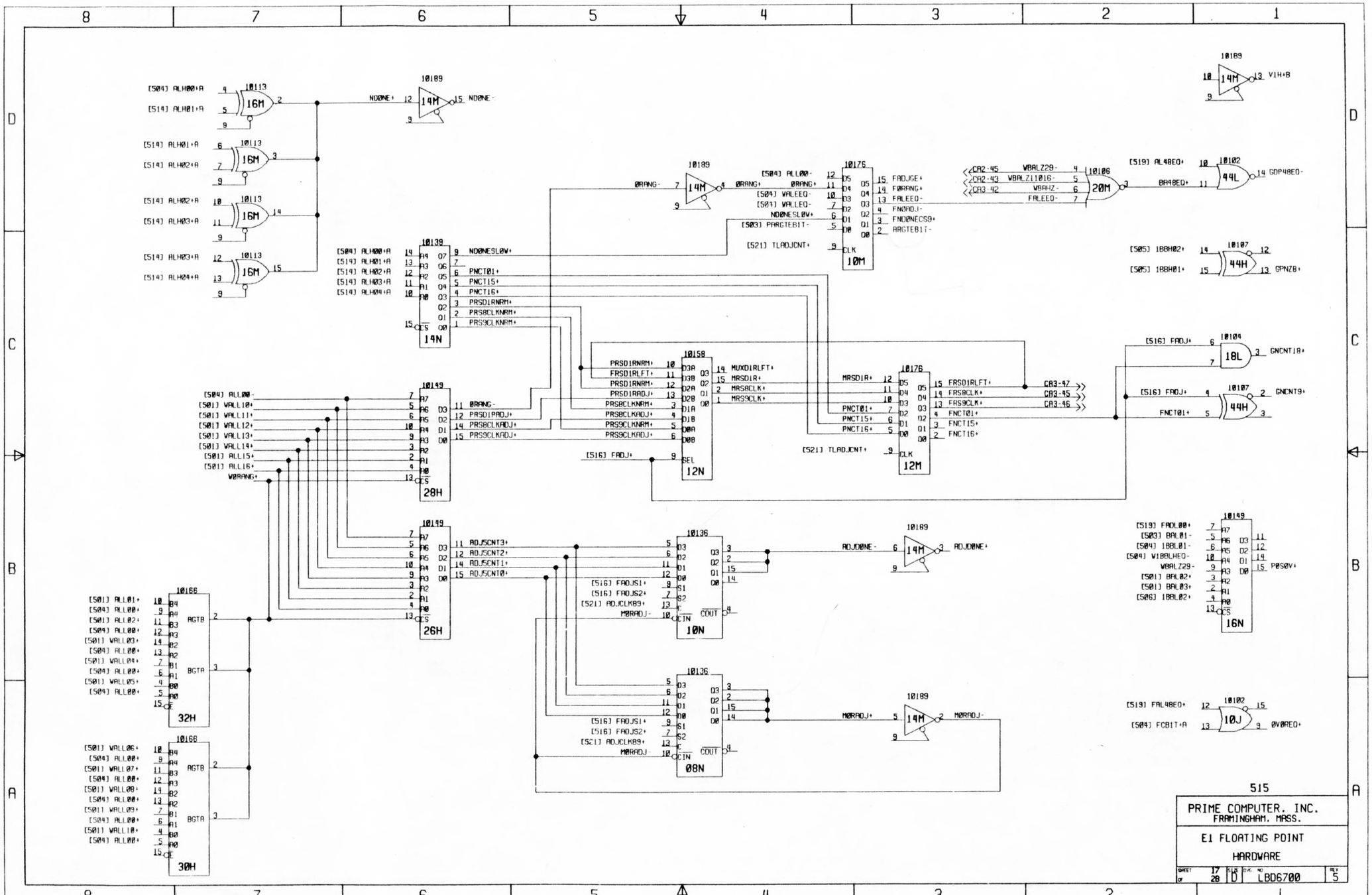


514

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E1 DECIMAL HARDWARE

SHEET 16 OF 28 | SIZE D | DWG NO LBD6700 | REV 4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VIH+B
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10113
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ND0NE+
ND0NE-
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[514] ALH03+A
[514] ALH03+A
[514] ALH04+A
10139
14N
[504] ALH00+A
[514] ALH01+A
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[514] ALH04+A
ND0NESL0V+
PNCT01+
PNCT15+
PNCT16+
PRSD1RNRM+
PRS8CLKNRM+
PRS9CLKNRM+
10189
14M
0RANG-
0RANG+
10176
10M
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[504] VALL07+
FADJGE+
F0RANG+
FALEEQ-
FN0ADJ-
FND0NECS9+
ARGTEBIT-
[521] TLADJCNT+
10106
20M
CA2-45
CA2-43
CA3-42
VBALZ29-
VBALZ11016-
VBAHZ-
FALEEQ-
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BA48EQ+
10102
44L
GDP48EQ-
[505] IBBH02+
[505] IBBH01+
10107
44H
GPNZB+
10149
28H
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W0RANG+
0RANG-
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PRS8CLKADJ+
PRS9CLKADJ+
10158
12N
PRSD1RNRM+
FRSD1RLFT+
PRSD1RNRM+
PRSD1RADJ+
PRS8CLKNRM+
PRS8CLKADJ+
PRS9CLKNRM+
PRS9CLKADJ+
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MRS8CLK+
MRS9CLK+
10176
12M
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PNCT15+
PNCT16+
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FRS8CLK+
FRS9CLK+
FNCT01+
FNCT15+
FNCT16+
CA3-47
CA3-45
CA3-46
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10104
18L
GNCNT18+
[516] FADJ+
FNCT01+
10107
44H
GNCNT9+
10149
26H
ADJ5CNT3+
ADJ5CNT2+
ADJ5CNT1+
ADJ5CNT0+
10136
10N
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M0RADJ-
COUT
CTN
10189
14M
ADJD0NE-
ADJD0NE+
10149
16N
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VBALZ29-
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P0S0V+
10166
32H
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AGTB
BGTA
10166
30H
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BGTA
10136
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M0RADJ-
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14M
M0RADJ-
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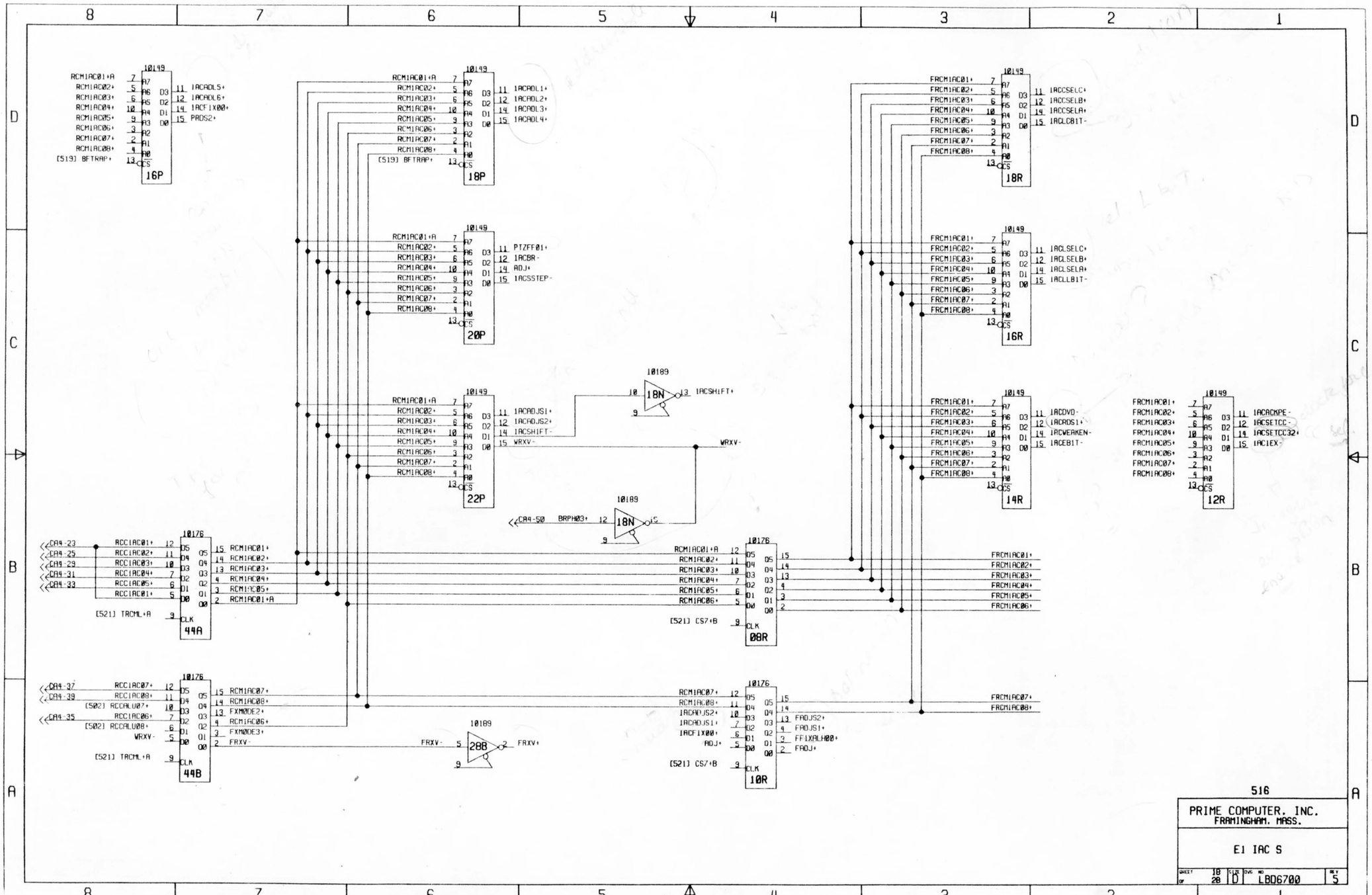
10102
10J
0V0REQ+
515
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 FLOATING POINT
HARDWARE
SHEET 17 OF 28
SIZE D
DWG. NO LBD6700
REV 5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18P
20P
22P
18R
16R
14R
12R
44A
44B
08R
10R
18N
28B
RCM1AC01+A
RCM1AC02+
RCM1AC03+
RCM1AC04+
RCM1AC05+
RCM1AC06+
RCM1AC07+
RCM1AC08+
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IACADL5+
IACADL6+
IACFIX00+
PROS2+
IACADL1+
IACADL2+
IACADL3+
IACADL4+
PTZFF01+
IACBR-
ADJ+
IACSSTEP-
IACADJS1+
IACADJS2+
IACSHIFT-
WRXV-
IACSHIFT+
FRCM1AC01+
FRCM1AC02+
FRCM1AC03+
FRCM1AC04+
FRCM1AC05+
FRCM1AC06+
FRCM1AC07+
FRCM1AC08+
IACCSELC+
IACCSELB+
IACCSELA+
IACLCB1T-
IACLSELC+
IACLSELB+
IACLSELA+
IACLLB1T-
IACDVD-
IACRDS1+
IACWERKEN-
IACEB1T-
IACACKPE-
IACSETCC-
IACSETCC32+
IACIEX-
CA9-23
CA9-25
CA9-29
CA9-31
CA9-33
RCC1AC01+
RCC1AC02+
RCC1AC03+
RCC1AC04+
RCC1AC05+
RCC1AC01+
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RCM1AC02+
RCM1AC03+
RCM1AC04+
RCM1AC05+
RCM1AC01+A
[521] CS7+B
CA9-37
CA9-39
CA9-35
RCC1AC07+
RCC1AC08+
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RCC1AC06+
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WRXV-
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FXM00E2+
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FRXV-
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IACADJS1+
IACFIX00+
ADJ+
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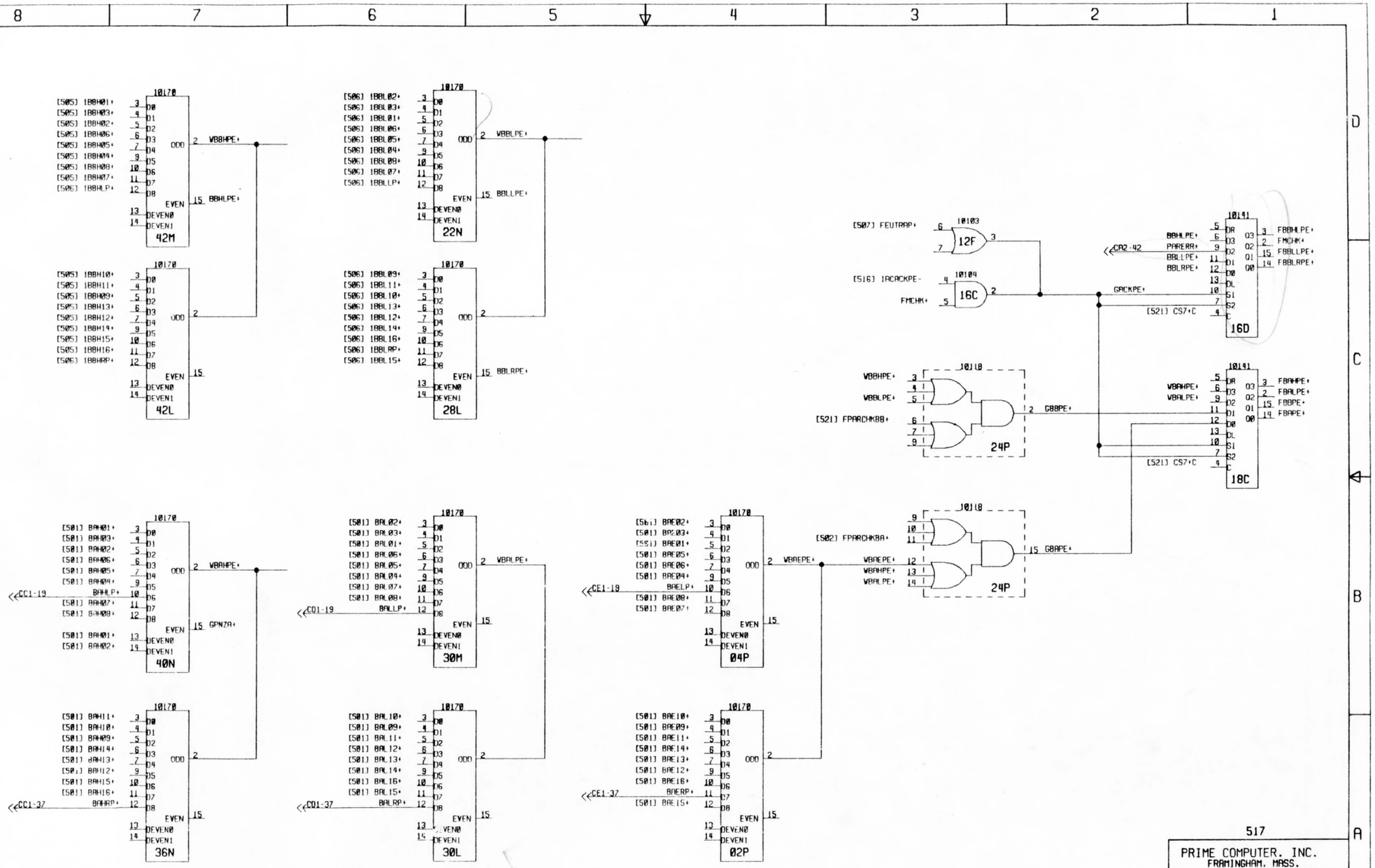
FADJS2+
FADJS1+
FFIXALH00+
FADJ+
CA9-50
BRPH03+
FRXV+
516
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 IAC S
SHEET 18 OF 28
SIZE D
DWG NO LBD6700
REV 5


42M
22N
42L
28L
40N
30M
36N
30L
04P
02P
12F
16C
16D
18C
24P
24P
VBBHPE+
VBBLPE+
BBHLPE+
BBLLPE+
VBBLPE+
BBLRPE+
VBAHPE+
GPNZA+
VBALPE+
VBAEPE+
VBAHPE+
VBALPE+
FEUTRAP+
IACACKPE-
FMCHK+
GACKPE+
CS7+C
FBBHLPE+
FMCHK+
FBBLLPE+
FBBLRPE+
FBAHPE+
FBALPE+
FBBPE+
FBAPE+
FPARCHKBB+
GBBPE+
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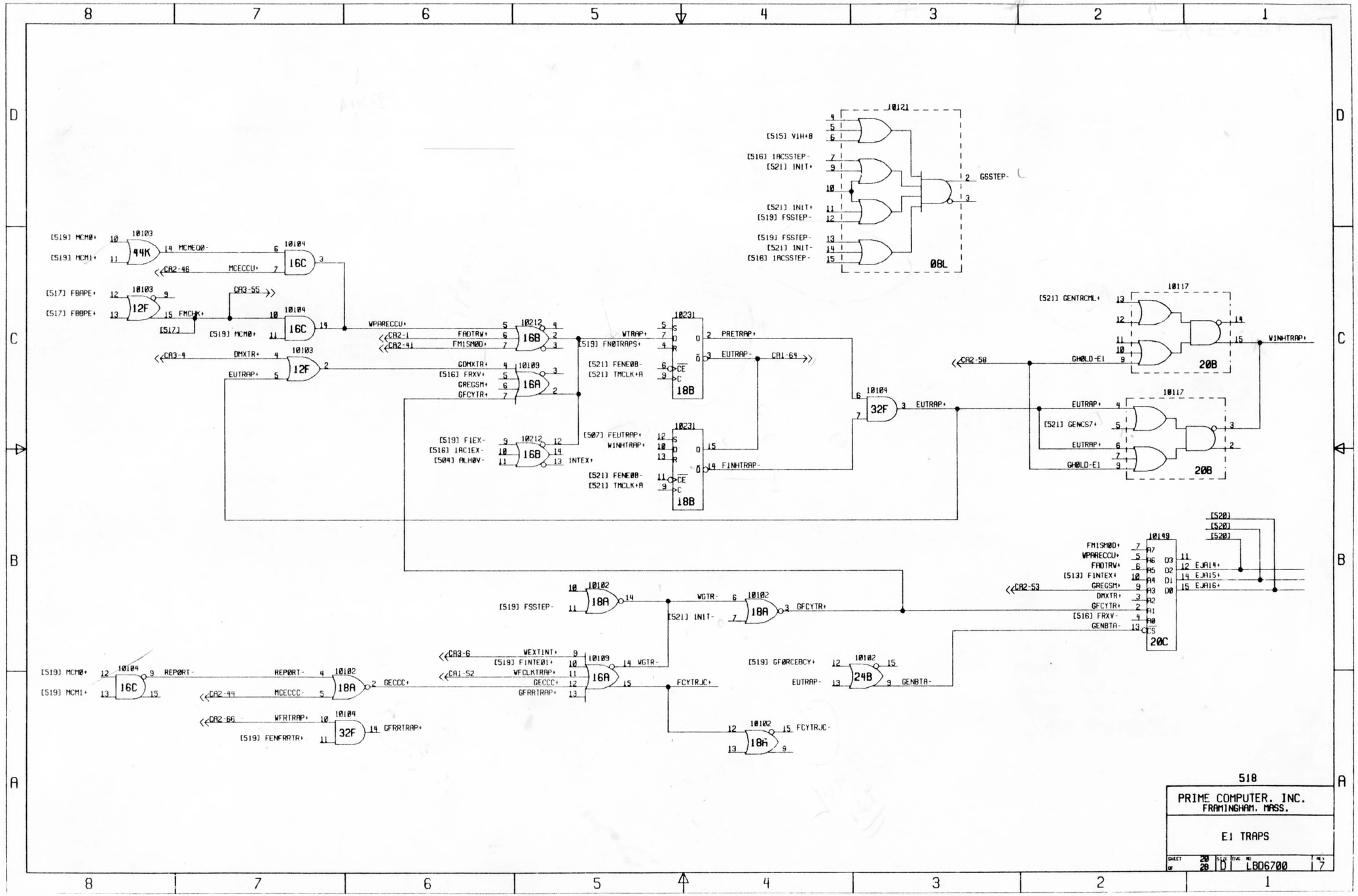
GBAPE+
517
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 PARITY
LBD6700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MCMEØØ-
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MCECCU+
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FM1SMØD+
10212
16B
WTRAP+
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18B
PRETRAP+
EUTRAP-
CA1-64
CA3-9
DMXTR+
EUTRAP+
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GDMXTR+
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GFCYTR+
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INTEX+
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WINHTRAP+
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FINHTRAP-
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32F
EUTRAP+
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10117
20B
WINHTRAP+
CA2-58
GHØLD-E1
EUTRAP+
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EUTRAP+
GHØLD-E1
20B
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WGTR-
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GFCYTR+
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WPARECCU+
FADTRV+
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GREGSM+
DMXTR+
GFCYTR+
[516] FRXV-
GENBTA-
CA2-53
D3
D2
D1
D0
EJA14+
EJA15+
EJA16+
20C
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16C
REPØRT-
CA2-44
MCECCC-
18A
GECCC+
CA3-6
WEXTINT+
[519] FINTEØ1+
CA1-52
WFCLKTRAP+
GECCC+
GFRRTRAP+
16A
WGTR-
FCYTRJC+
[519] GFØRCEBCY+
EUTRAP-
24B
GENBTA-
CA2-66
WFRTRAP+
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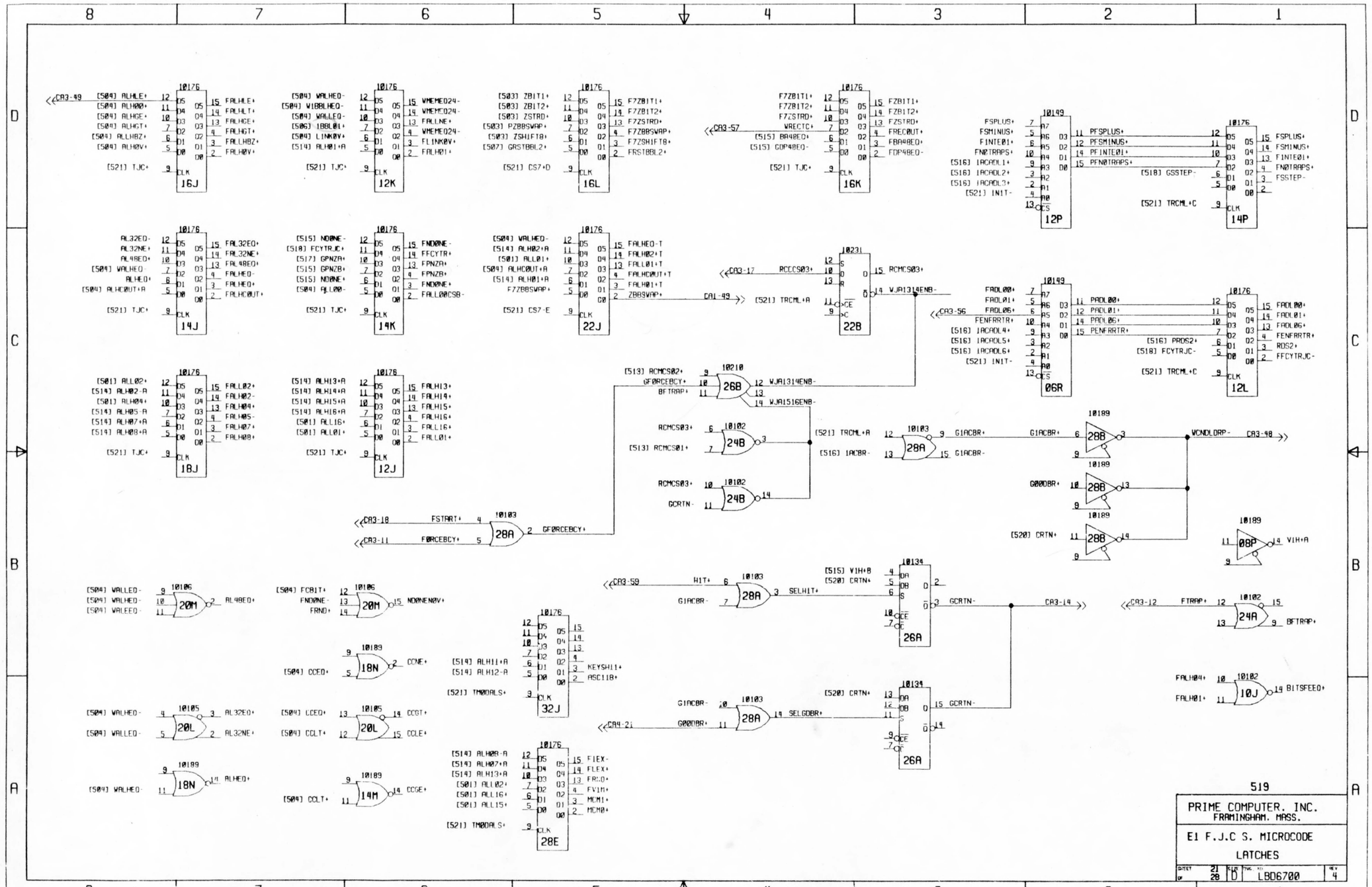
32F
GFRRTRAP+
FCYTRJC-
18A
518
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 TRAPS
SHEET 20 OF 20
SIZE D
DWG NO LBD6700
REV 7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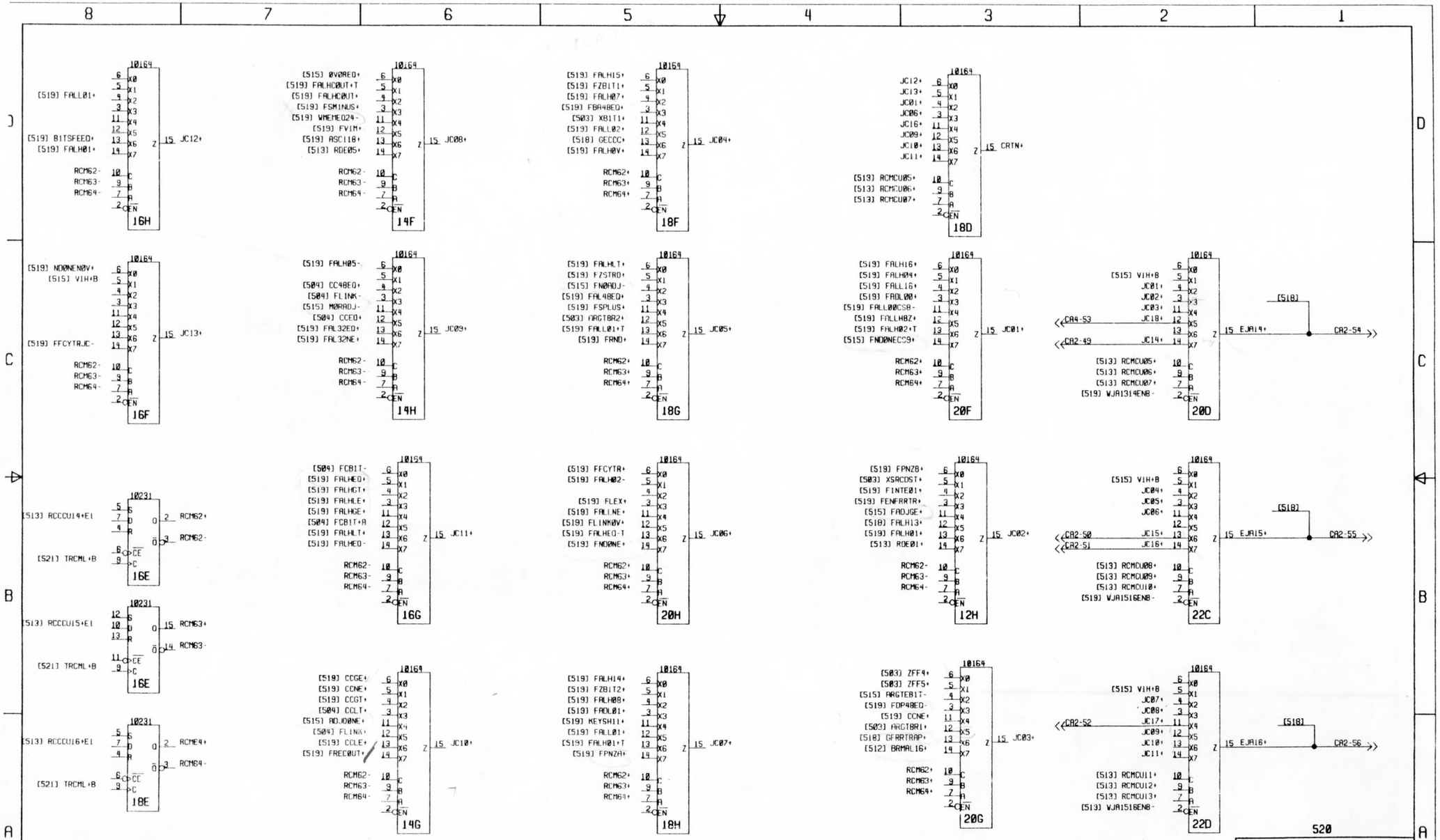
FRAMINGHAM, MASS.
E1 F.J.C S. MICROCODE
LATCHES
519
LBD6700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RCM62-
RCM63-
RCM64-
JC12+
14F
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JC08+
18F
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JC12+
JC13+
JC01+
JC06+
JC16+
JC09+
JC10+
JC11+
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[513] RCMCU06+
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CRTN+
16F
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JC13+
14H
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JC09+
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JC05+
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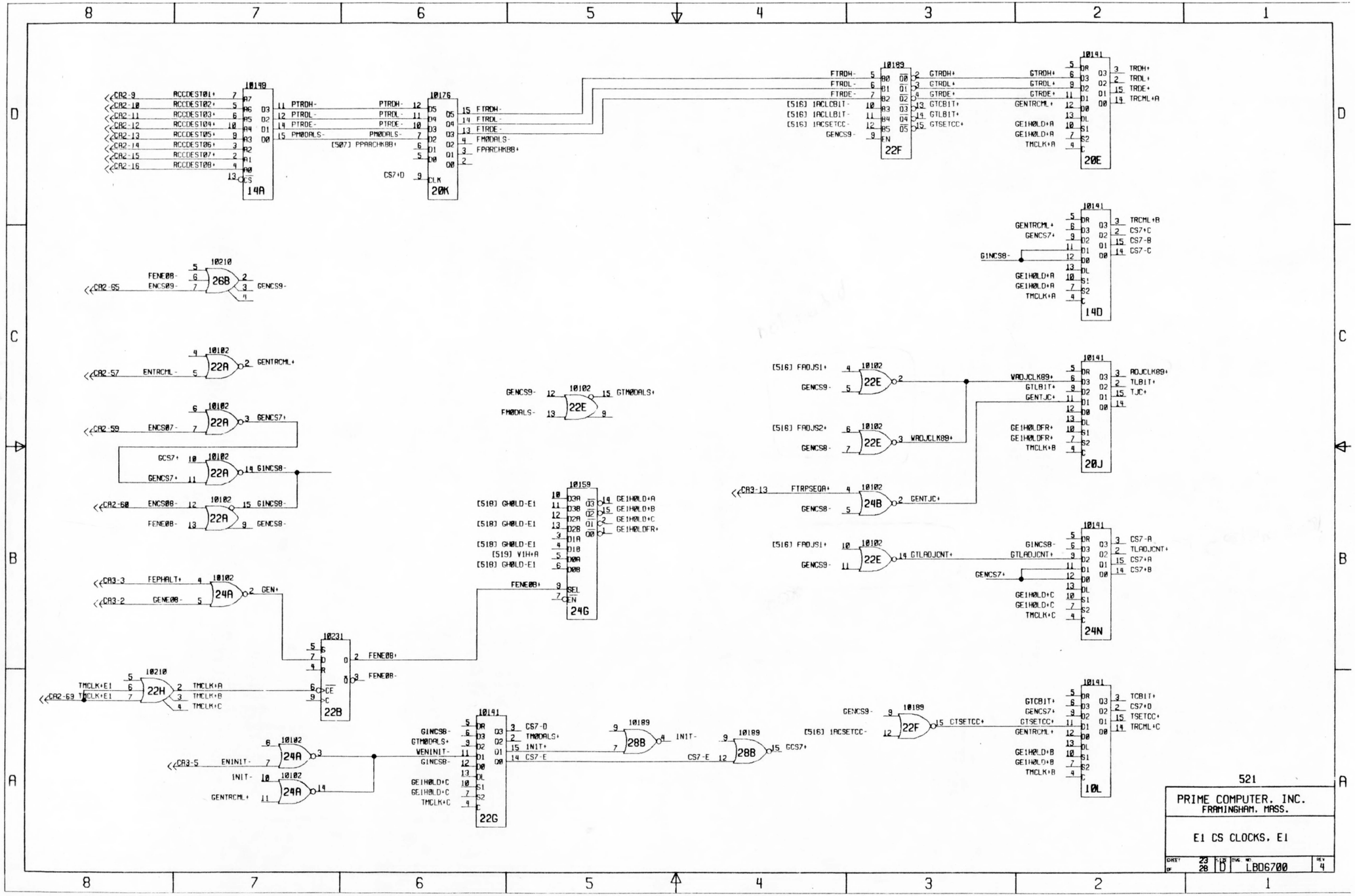
[519] FALL16+
[519] FR0L00+
[519] FALL00CSB-
[519] FALLHBZ+
[519] FALH02+T
[515] FN00NECC9+
JC01+
20D
[515] VIH+B
JC01+
JC02+
JC03+
JC18+
JC14+
CA4-53
CA2-49
[518]
15 EJA19+
CA2-54
[513] RCMCU05+
[513] RCMCU06+
[513] RCMCU07+
[519] WJA1314ENB-
16E
[513] RCCCU14+E1
[521] TRCML+B
RCM62+
RCM62-
16G
[504] FCBIT-
[519] FALHE0+
[519] FALHGT+
[519] FALHLE+
[519] FALHGE+
[504] FCBIT+A
[519] FALHLT+
[519] FALHE0-
JC11+
20H
[519] FFCYTR+
[519] FALH02-
[519] FLEX+
[519] FALINE+
[519] FLINK0V+
[519] FALHE0-T
[519] FN00NE+
JC06+
12H
[519] FPNZB+
[503] XSRCDST+
[519] FINTE01+
[519] FENFRRTR+
[515] FA0JGE+
[518] FALH13+
[519] FALH01+
[513] RDE01+
JC02+
22C
[515] VIH+B
JC04+
JC05+
JC06+
CA2-50
CA2-51
JC15+
JC16+
[518]
15 EJA15+
CA2-55
[513] RCMCU08+
[513] RCMCU09+
[513] RCMCU10+
[519] WJA1516ENB-
16E
[513] RCCCU15+E1
[521] TRCML+B
RCM63+
RCM63-
14G
[519] CCGE+
[519] CCNE+
[519] CCGT+
[504] CCLT+
[515] A0.00NE+
[504] FLINA+
[519] CCLE+
[519] FREC0UT+
JC10+
18H
[519] FALH14+
[519] FZBIT2+
[519] FALH08+
[519] FR0L01+
[519] KEYSH11+
[519] FALL01+
[519] FALH01+T
[519] FPNZA+
JC07+
20G
[503] ZFF4+
[503] ZFF5+
[515] ARGTEBIT-
[519] FDP4BED-
[519] CCNE+
[503] ARGTBR1+
[518] GFARTRAP+
[512] BRMAL16+
JC03+
22D
[515] VIH+B
JC07+
JC08+
JC17+
JC09+
JC10+
JC11+
CA2-52
[518]
15 EJA16+
CA2-56
[513] RCMCU11+
[513] RCMCU12+
[513] RCMCU13+
[513] WJA1516ENB-
16E
[513] RCCCU16+E1
[521] TRCML+B
RCM64+
RCM64-
T SUFFIX ON THE NAME MEANS J.C. IS FOR TRAP UCODE.
OTHER J.C.'S STOP STATICIZING ON TRAPS.
520
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
EI J.A.'S, J.C.'S
SHEET OF 22 28
SIZE D
DWG NO LBD6700
REV 6


14A
20K
22F
20E
14D
26B
22A
22E
20J
24B
24N
24A
22H
22B
24G
22G
28B
10L
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E1 CS CLOCKS, E1
521
LBD6700
D

CA1-13 >>GND

CA1-14 >>GND

CA1-27 >>-5.2V

CA1-28 >>-5.2V

CA1-29 >>-5.2V

CA1-30 >>-5.2V

CA1-43 >>-2V

CA1-44 >>-2V

CA1-57 >>GND

CA1-58 >>GND

CA1-59 >>GND

CA1-60 >>GND

CA2-3 >>GND

CA2-4 >>GND

CA2-17 >>-5.2V

CA2-18 >>-5.2V

CA2-19 >>-5.2V

CA2-20 >>-5.2V

CA2-33 >>-2V

CA2-34 >>-2V

CA2-47 >>GND

CA2-48 >>GND

CA2-61 >>GND

CA2-62 >>GND

CA2-63 >>GND

CA2-64 >>GND

CA2-67 >>GND

CA2-70 >>GND

CA3-1 >>GND

CA3-7 >>GND

CA3-8 >>GND

CA3-9 >>GND

CA3-10 >>GND

CA3-23 >>GND

CA3-24 >>GND

CA3-37 >>-2V

CA3-38 >>-2V

CA3-51 >>-5.2V

CA3-52 >>-5.2V

CA3-53 >>-5.2V

CA3-54 >>-5.2V

CA3-67 >>GND

CA3-68 >>GND

CA4-11 >>GND

CA4-12 >>GND

CA4-13 >>GND

CA4-14 >>GND

CA4-27 >>-2V

CA4-28 >>-2V

CA4-41 >>-5.2V

CA4-42 >>-5.2V

CA4-43 >>-5.2V

CA4-44 >>-5.2V

CA4-57 >>GND

CA4-58 >>GND

C164
22
15V 10%
GND 1 || 2 -5.2V
+

C165
22
15V 10%
GND 1 || 2 [***] -2V
+

C166
22
15V 10%
GND 1 || 2 [***] -2V
+

C167
22
15V 10%
GND 1 || 2 -5.2V
+

CC1-1 >>GND

CC1-10 >>GND

CC1-12 >>GND

CC1-14 >>GND

CC1-16 >>GND

CC1-18 >>GND

CC1-2 >>GND

CC1-20 >>GND

CC1-22 >>GND

CC1-24 >>GND

CC1-26 >>GND

CC1-28 >>GND

CC1-30 >>GND

CC1-32 >>GND

CC1-34 >>GND

CC1-36 >>GND

CC1-38 >>GND

CC1-4 >>GND

CC1-6 >>GND

CC1-8 >>GND

CD1-1 >>GND

CD1-2 >>GND

CD1-4 >>GND

CD1-6 >>GND

CD1-8 >>GND

CD1-10 >>GND

CD1-12 >>GND

CD1-14 >>GND

CD1-16 >>GND

CD1-18 >>GND

CD1-20 >>GND

CD1-22 >>GND

CD1-24 >>GND

CD1-26 >>GND

CD1-28 >>GND

CD1-30 >>GND

CD1-32 >>GND

CD1-34 >>GND

CD1-36 >>GND

CD1-38 >>GND

CE1-1 >>GND

CE1-2 >>GND

CE1-4 >>GND

CE1-6 >>GND

CE1-8 >>GND

CE1-10 >>GND

CE1-12 >>GND

CE1-14 >>GND

CE1-16 >>GND

CE1-18 >>GND

CE1-20 >>GND

CE1-22 >>GND

CE1-24 >>GND

CE1-26 >>GND

CE1-28 >>GND

CE1-30 >>GND

CE1-32 >>GND

CE1-34 >>GND

CE1-36 >>GND

CE1-38 >>GND

NOTES :

1. .01 UF AXIAL LEAD CAPACITORS ARE NOT SHOWN BUT ARE INSTALLED IN ALL COLUMNS BELOW ROWS A.C.E.G.J.R EXCEPT 38A & 14E. AND ABOVE ROW K COLUMNS 2.6.8.10.12.16.18. 20.28.30.32.34.42 & 44. AND ROW N COLUMNS 08 - 44

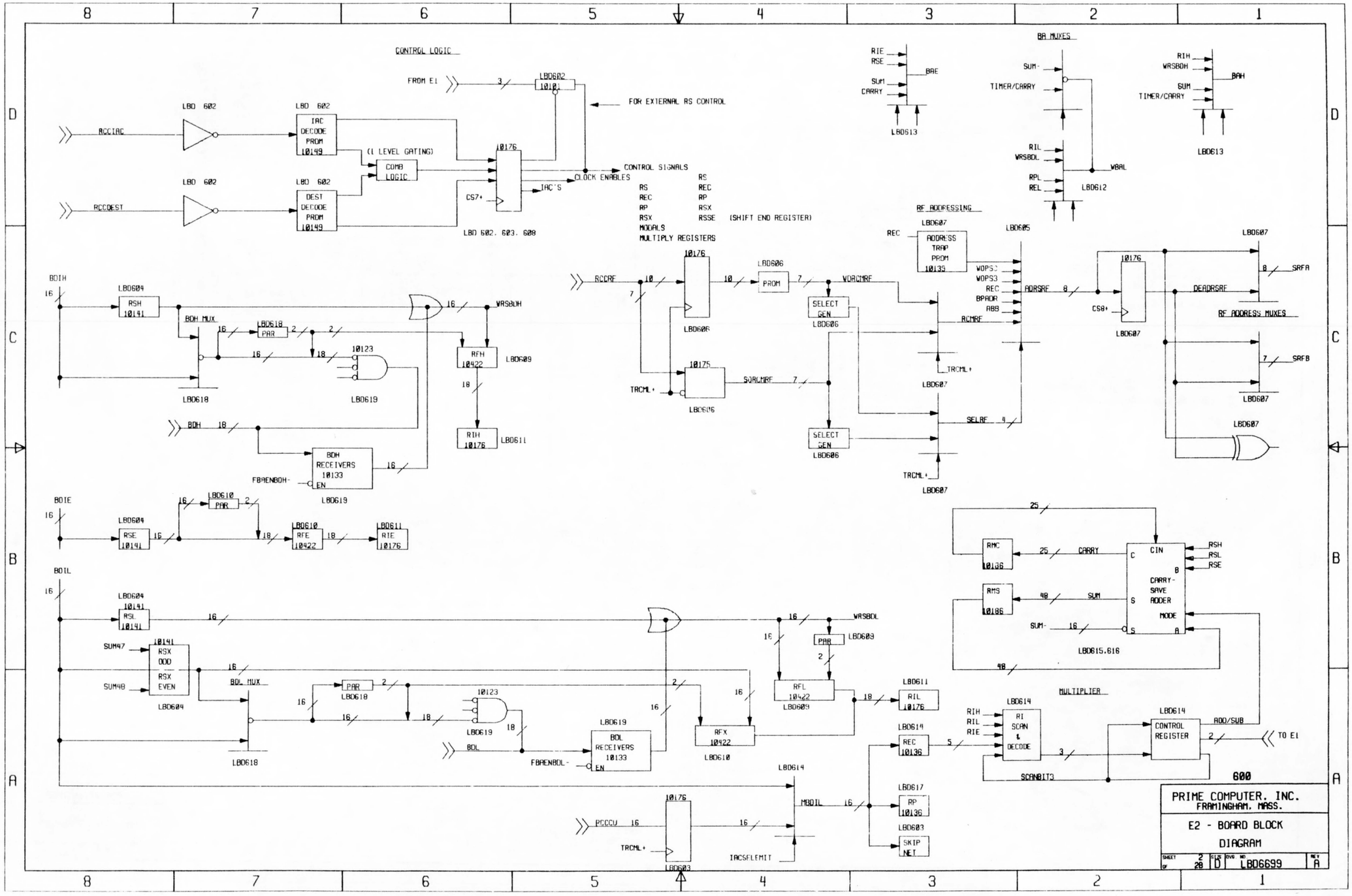
2. UNLESS OTHERVISE SPECIFIED : RESISTANCE VALUES ARE IN OHMS CAPACITANCE VALUES ARE IN MICROFARADS.

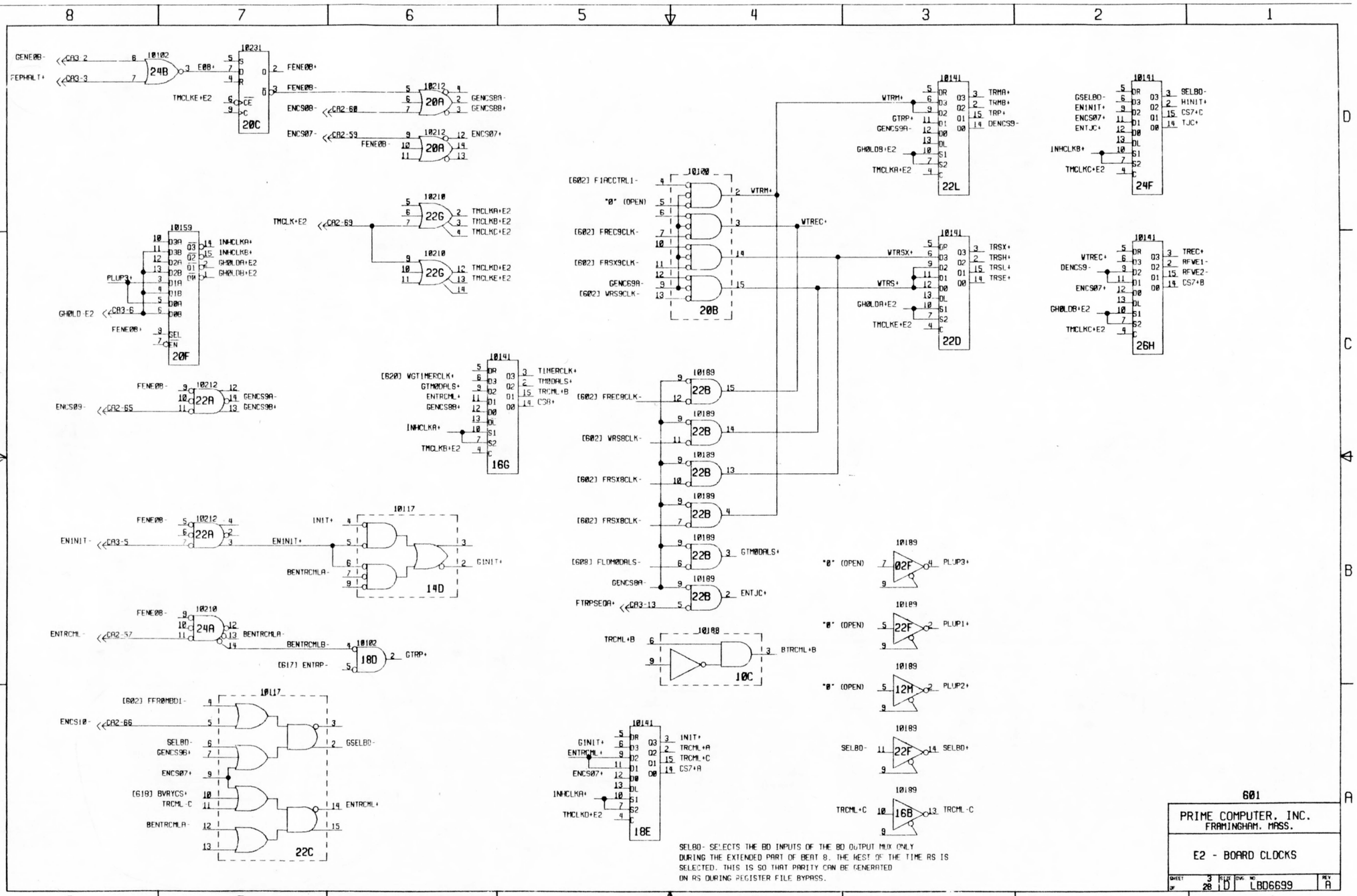
522

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E1 - BOARD POWER PINS

SHEET 20 OF 20 | SIZE D | DWG. NO LBD6700 | REV. 119


CONTROL LOGIC
FROM EI
LBD602
10101
FOR EXTERNAL RS CONTROL
LBD 602
ACCIAC
IAC DECODE PROM 10149
(1 LEVEL GATING)
COMB LOGIC
10176
CONTROL SIGNALS
CLOCK ENABLES
IAC'S
CS7+
ACCDEST
DEST DECODE PROM 10149
LBD 602, 603, 608
RS
REC
RP
RSX
MODALS
MULTIPLY REGISTERS
RS
REC
RP
RSX
RSSE
(SHIFT END REGISTER)
BA MUXES
RIE
RSE
SUM
CARRY
BAE
LBD613
SUM-
TIMER/CARRY
RIL
WRSBDL
WBAL
RPL
REL
LBD612
RIH
WRSBDH
BAH
LBD613
RF ADDRESSING
LBD607
REC
ADDRESS TRAP PROM 10135
LBD605
WOPS2
WOPS3
REC
BPADR
ABS
RCMRF
ADRSRF
8
CS8+
LBD607
DEADRSRF
SAFA
RF ADDRESS MUXES
SAFB
RCCRF
10
PROM
LBD606
VQRCMRF
SELECT GEN
LBD606
10175
TRCML+
SQRCMRF
7
LBD606
SELRF
4
BDIH
16
LBD604
RSH 10141
BDH MUX
LBD618
PAR
2
10123
LBD619
RFH 10422
LBD609
RIH 10176
LBD611
VRSBDH
BDH
18
BDH RECEIVERS 10133
EN
FBAENBDH-
LBD619
BDIE
RSE 10141
LBD610
PAR
RFE 10422
RIE 10176
BDIL
RSL 10141
SUM47
SUM48
RSX ODD
RSX EVEN
10141
BDL MUX
LBD618
BDL
FBAENBDL-
BDL RECEIVERS 10133
LBD619
RFX 10422
LBD610
WRSBDL
PAR
LBD609
RFL 10422
LBD611
RIL 10176
RMC 10136
RMS 10136
CARRY-SAVE ADDER
CIN
CARRY
SUM
SUM-
MODE
RSH
RSL
RSE
LBD615.616
MULTIPLIER
LBD614
RI SCAN & DECODE
REC 10136
CONTROL REGISTER
ADD/SUB
TO EI
SCANBIT3
LBD617
RP 10136
LBD603
SKIP NET
MBDIL
PCCCU
TRCML+
IACSFLEMIT
LBD603
600
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E2 - BOARD BLOCK DIAGRAM
SHEET 2 OF 28
SIZE D
DWG NO LBD6699
REV A



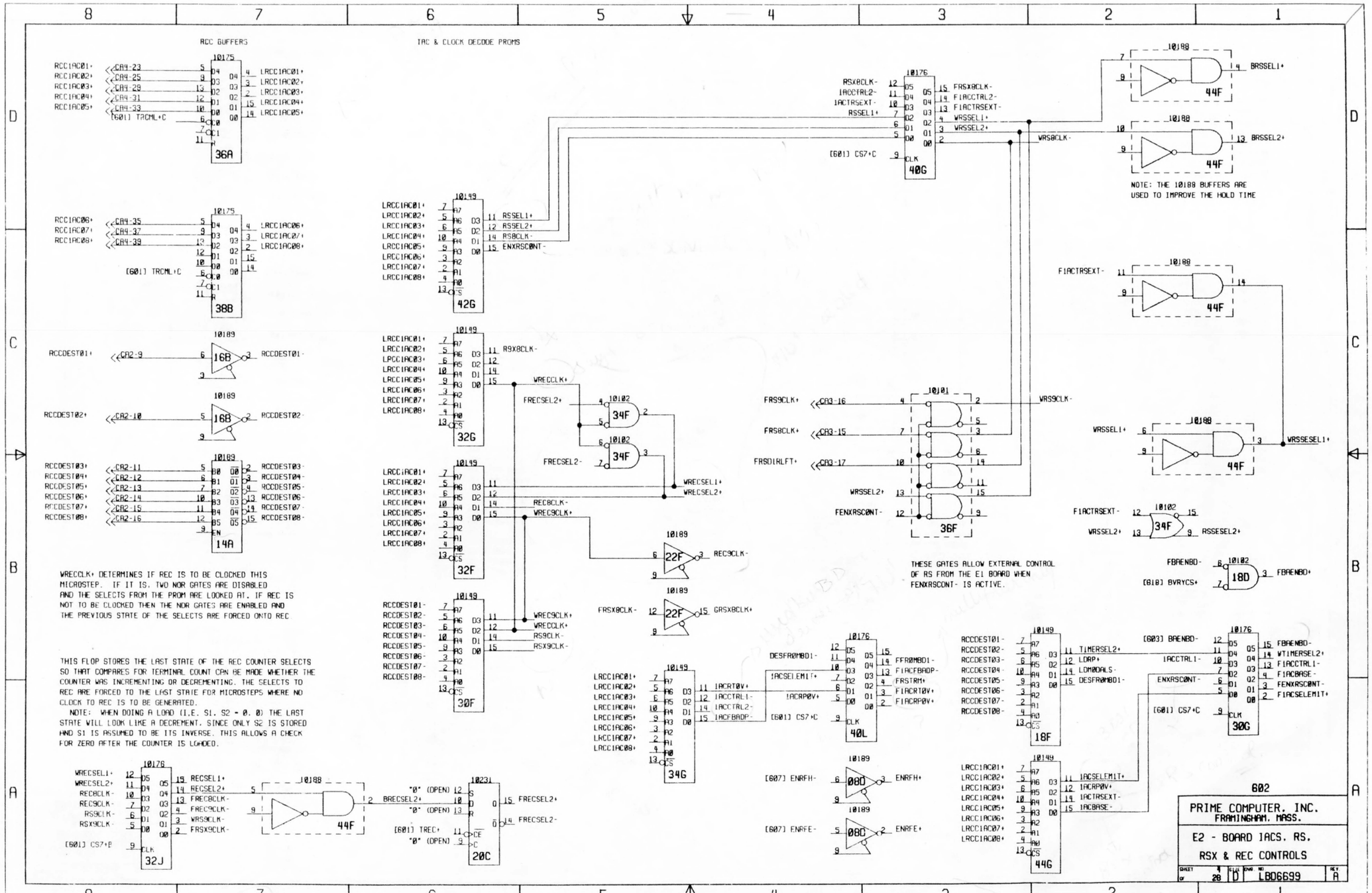
SELBD- SELECTS THE BD INPUTS OF THE BD OUTPUT MUX ONLY DURING THE EXTENDED PART OF BEAT 8. THE REST OF THE TIME RS IS SELECTED. THIS IS SO THAT PARITY CAN BE GENERATED ON RS DURING REGISTER FILE BYPASS.

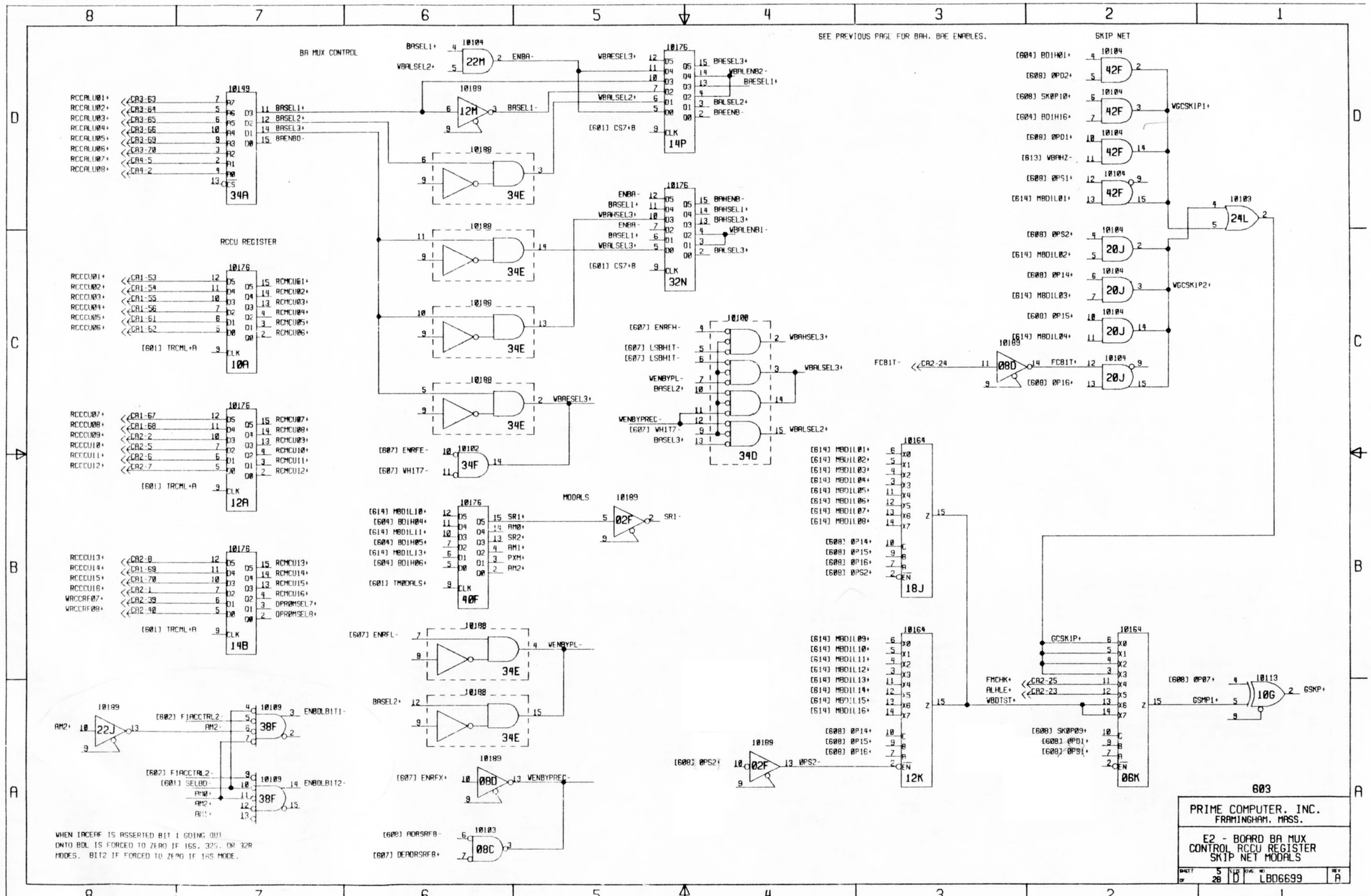
601

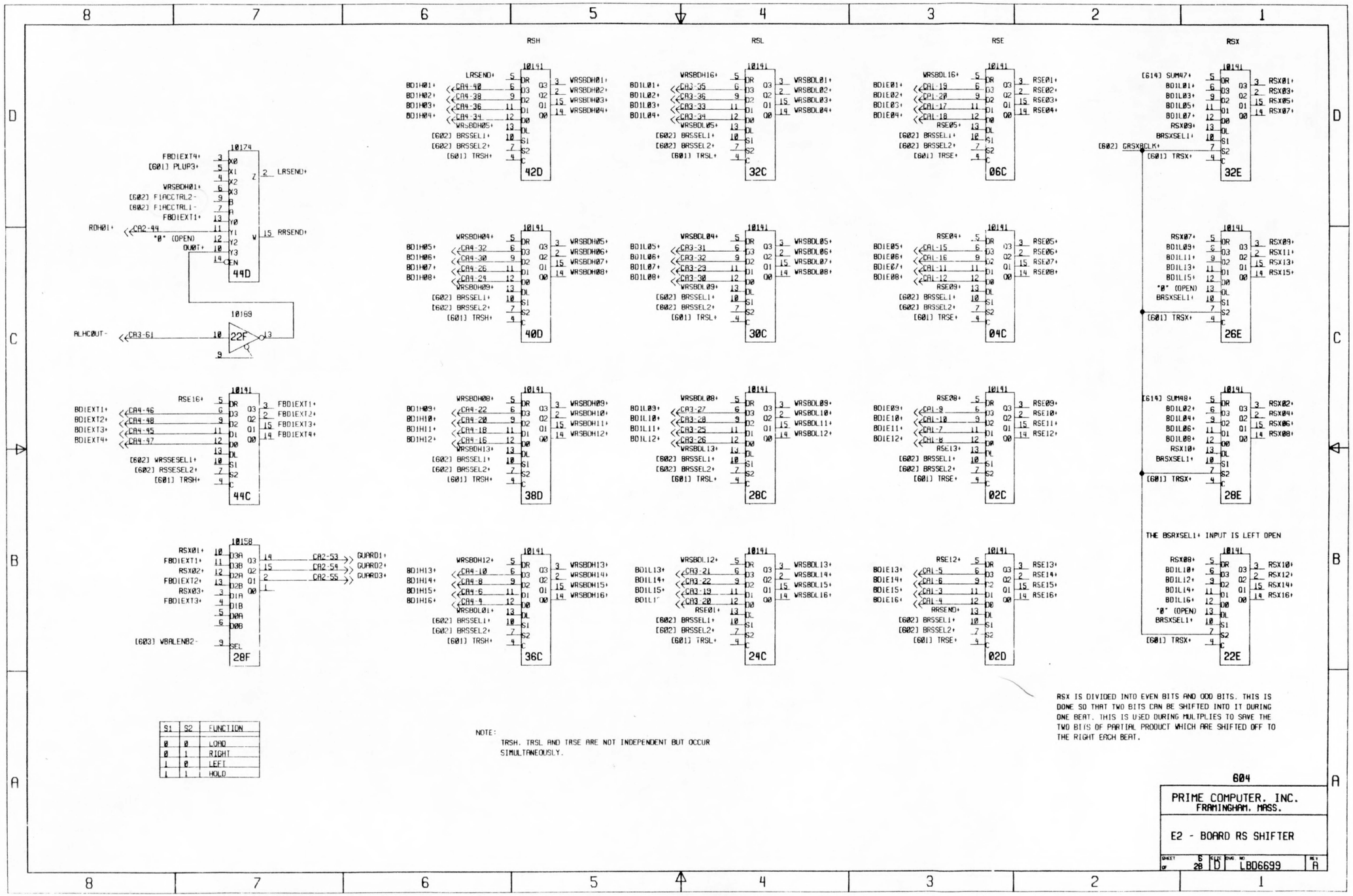
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

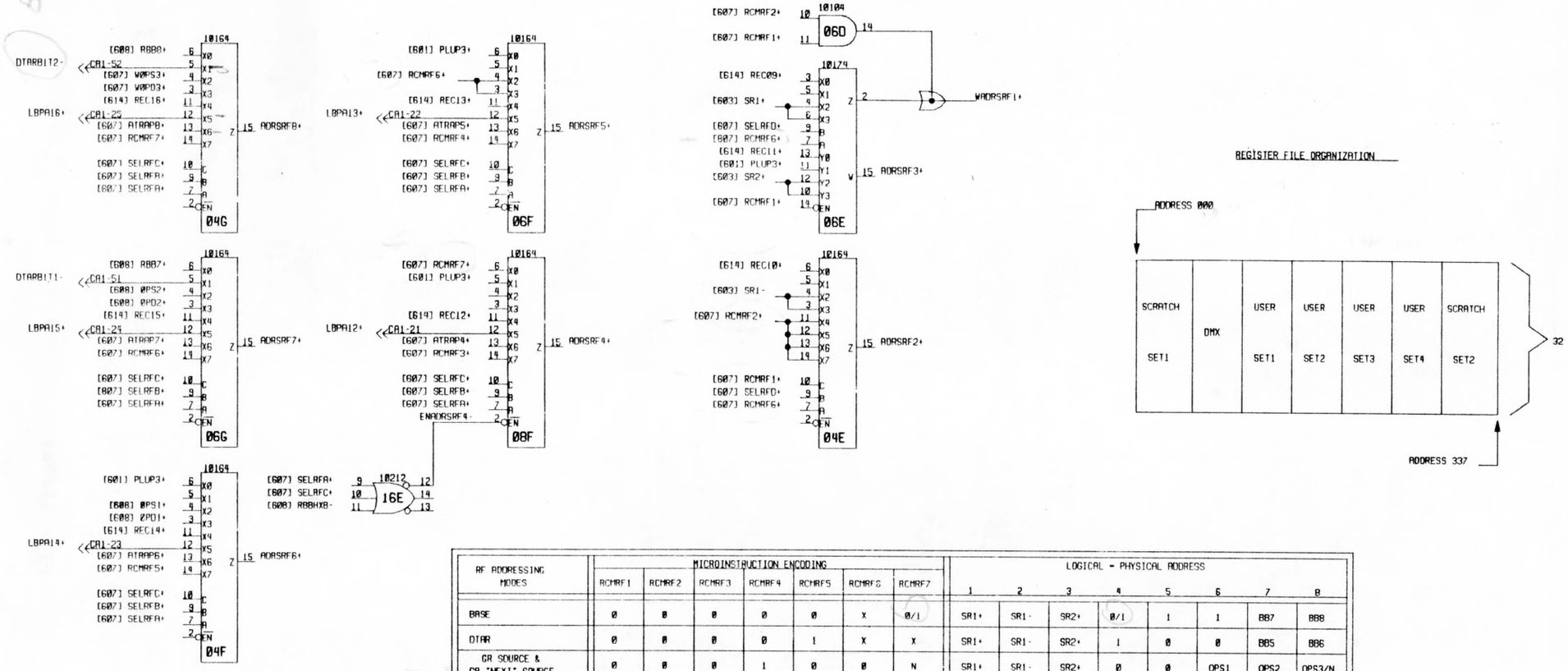
E2 - BOARD CLOCKS

SHEET 3 OF 28 | DWG NO LBD6699 | REV A


RCC BUFFERS
IAC & CLOCK DECODE PROMS
WRECCLK+ DETERMINES IF REC IS TO BE CLOCKED THIS MICROSTEP. IF IT IS, TWO NOR GATES ARE DISABLED AND THE SELECTS FROM THE PROM ARE LOOKED AT. IF REC IS NOT TO BE CLOCKED THEN THE NOR GATES ARE ENABLED AND THE PREVIOUS STATE OF THE SELECTS ARE FORCED ONTO REC
THIS FLOP STORES THE LAST STATE OF THE REC COUNTER SELECTS SO THAT COMPARES FOR TERMINAL COUNT CAN BE MADE WHETHER THE COUNTER WAS INCREMENTING OR DECREMENTING. THE SELECTS TO REC ARE FORCED TO THE LAST STATE FOR MICROSTEPS WHERE NO CLOCK TO REC IS TO BE GENERATED.
NOTE: WHEN DOING A LOAD (I.E. S1, S2 = 0, 0) THE LAST STATE WILL LOOK LIKE A DECREMENT. SINCE ONLY S2 IS STORED AND S1 IS ASSUMED TO BE ITS INVERSE. THIS ALLOWS A CHECK FOR ZERO AFTER THE COUNTER IS LOADED.
NOTE: THE 10188 BUFFERS ARE USED TO IMPROVE THE HOLD TIME
THESE GATES ALLOW EXTERNAL CONTROL OF RS FROM THE E1 BOARD WHEN FENXRSCONT- IS ACTIVE.
602
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E2 - BOARD IACS, RS, RSX & REC CONTROLS
SHEET 28
SIZE D
DWG NO LBD6699
REV A


SEE PREVIOUS PAGE FOR BAH, BAE ENABLES.
BA MUX CONTROL
RCCU REGISTER
SKIP NET
34A
34E
14P
32N
10A
12A
14B
34F
34D
18J
12K
06K
22J
38F
42F
20J
24L
08D
02F
10G
40F
08C
WHEN IACERF IS ASSERTED BIT 1 GOING OUT ONTO BDL IS FORCED TO ZERO IF 16S, 32S, OR 32R MODES. BIT2 IF FORCED TO ZERO IF 16S MODE.
603
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E2 - BOARD BA MUX CONTROL RCCU REGISTER SKIP NET MODALS
SHEET 5 OF 28
SIZE D
DWG NO LBD6699
REV A


RSH
RSL
RSE
RSX
10174
FBDIEXT4+
[601] PLUP3+
WRSBDH01+
[602] FIACCTRL2-
[602] FIACCTRL1-
FBDIEXT1+
RDH01+
CA2-44
"0" (OPEN)
OUT+
LRSEND+
RRSEND+
44D
10169
ALHC0UT-
CA3-61
22F
10141
LRSEND+
BD1H01+
BD1H02+
BD1H03+
BD1H04+
CA4-40
CA4-38
CA4-36
CA4-34
WRSBDH05+
[602] BRSSEL1+
[602] BRSSEL2+
[601] TRSH+
WRSBDH01+
WRSBDH02+
WRSBDH03+
WRSBDH04+
42D
WRSBDL16+
BD1L01+
BD1L02+
BD1L03+
BD1L04+
CA3-35
CA3-36
CA3-33
CA3-34
WRSBDL05+
[601] TRSL+
WRSBDL01+
WRSBDL02+
WRSBDL03+
WRSBDL04+
32C
BD1E01+
BD1E02+
BD1E03+
BD1E04+
CA1-19
CA1-20
CA1-17
CA1-18
RSE05+
[601] TRSE+
RSE01+
RSE02+
RSE03+
RSE04+
06C
[614] SUM47+
BD1L01+
BD1L03+
BD1L05+
BD1L07+
RSX09+
BRSXSEL1+
[602] GRSXCLK+
[601] TRSX+
RSX01+
RSX03+
RSX05+
RSX07+
32E
WRSBDH04+
BD1H05+
BD1H06+
BD1H07+
BD1H08+
CA4-32
CA4-30
CA4-26
CA4-24
WRSBDH09+
WRSBDH05+
WRSBDH06+
WRSBDH07+
WRSBDH08+
40D
WRSBDL04+
BD1L05+
BD1L06+
BD1L07+
BD1L08+
CA3-31
CA3-32
CA3-23
CA3-30
WRSBDL09+
WRSBDL05+
WRSBDL06+
WRSBDL07+
WRSBDL08+
30C
RSE04+
BD1E05+
BD1E06+
BD1E07+
BD1E08+
CA1-15
CA1-16
CA1-11
CA1-12
RSE09+
RSE05+
RSE06+
RSE07+
RSE08+
04C
RSX07+
BD1L09+
BD1L11+
BD1L13+
BD1L15+
"0" (OPEN)
BRSXSEL1+
[601] TRSX+
RSX09+
RSX11+
RSX13+
RSX15+
26E
BD1EXT1+
BD1EXT2+
BD1EXT3+
BD1EXT4+
CA4-46
CA4-48
CA4-45
CA4-47
[602] WRSSESEL1+
[602] RSSESEL2+
[601] TRSH+
RSE16+
FBDIEXT1+
FBDIEXT2+
FBDIEXT3+
FBDIEXT4+
44C
WRSBDH08+
BD1H09+
BD1H10+
BD1H11+
BD1H12+
CA4-22
CA4-20
CA4-18
CA4-16
WRSBDH13+
WRSBDH09+
WRSBDH10+
WRSBDH11+
WRSBDH12+
38D
WRSBDL08+
BD1L09+
BD1L10+
BD1L11+
BD1L12+
CA3-27
CA3-28
CA3-25
CA3-26
WRSBDL13+
WRSBDL09+
WRSBDL10+
WRSBDL11+
WRSBDL12+
28C
RSE08+
BD1E09+
BD1E10+
BD1E11+
BD1E12+
CA1-9
CA1-10
CA1-7
CA1-8
RSE13+
RSE09+
RSE10+
RSE11+
RSE12+
02C
[614] SUM48+
BD1L02+
BD1L04+
BD1L06+
BD1L08+
RSX10+
BRSXSEL1+
[601] TRSX+
RSX02+
RSX04+
RSX06+
RSX08+
28E
THE BSRXSEL1+ INPUT IS LEFT OPEN
RSX01+
FBDIEXT1+
RSX02+
FBDIEXT2+
RSX03+
FBDIEXT3+
[603] VBALEN82-
CA2-53
CA2-54
CA2-55
GUARD1+
GUARD2+
GUARD3+
28F
WRSBDH12+
BD1H13+
BD1H14+
BD1H15+
BD1H16+
CA4-10
CA4-8
CA4-6
CA4-4
WRSBDL01+
WRSBDH13+
WRSBDH14+
WRSBDH15+
WRSBDH16+
36C
WRSBDL12+
BD1L13+
BD1L14+
BD1L15+
BD1L1?
CA3-21
CA3-22
CA3-19
CA3-20
RSE01+
WRSBDL13+
WRSBDL14+
WRSBDL15+
WRSBDL16+
24C
RSE12+
BD1E13+
BD1E14+
BD1E15+
BD1E16+
CA1-5
CA1-6
CA1-3
CA1-4
RRSEND+
RSE13+
RSE14+
RSE15+
RSE16+
02D
RSX08+
BD1L10+
BD1L12+
BD1L14+
BD1L16+
"0" (OPEN)
BRSXSEL1+
[601] TRSX+
RSX10+
RSX12+
RSX14+
RSX16+
22E
S1 S2 FUNCTION
0 0 LOAD
0 1 RIGHT
1 0 LEFT
1 1 HOLD
NOTE:
TRSH, TRSL AND TRSE ARE NOT INDEPENDENT BUT OCCUR SIMULTANEOUSLY.
RSX IS DIVIDED INTO EVEN BITS AND ODD BITS. THIS IS DONE SO THAT TWO BITS CAN BE SHIFTED INTO IT DURING ONE BEAT. THIS IS USED DURING MULTPLIES TO SAVE THE TWO BITS OF PARTIAL PRODUCT WHICH ARE SHIFTED OFF TO THE RIGHT EACH BEAT.
604
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E2 - BOARD RS SHIFTER
SHEET 6 OF 28
SIZE D
DWG NO LBD6699
REV A



REGISTER FILE ORGANIZATION

RF ADDRESSING MODES	MICROINSTRUCTION ENCODING							LOGICAL - PHYSICAL ADDRESS							
	RCMRF1	RCMRF2	RCMRF3	RCMRF4	RCMRF5	RCMRF6	RCMRF7	1	2	3	4	5	6	7	8
BASE	0	0	0	0	0	X	0/1	SR1+	SR1-	SR2+	0/1	1	1	BB7	BB8
DTAR	0	0	0	0	1	X	X	SR1+	SR1-	SR2+	1	0	0	BB5	BB6
GR SOURCE & GR "NEXT" SOURCE	0	0	0	1	0	0	N	SR1+	SR1-	SR2+	0	0	OPS1	OPS2	OPS3/N
FR SOURCE & FR "NEXT" SOURCE	0	0	0	1	0	1	N	SR1+	SR1-	SR2+	0	1	*OPS1=0	OPS2	N
GR DESTINATION & GR "NEXT" DESTIN	0	0	0	1	1	0	N	SR1+	SR1-	SR2+	0	0	OPD1	OPD2	OPD3/N
FR DESTINATION & FR "NEXT" DESTIN	0	0	0	1	1	1	N	SR1+	SR1-	SR2+	0	1	*OPD1=0	OPD2	N
INDIRECT	0	0	1	0	0	0	X	REC9	REC10	REC11	REC12	REC13	REC14	REC15	REC16
DMX	0	0	1	0	1	1	X	0	0	1	BPADR4	BPADR5	BPADR6	BPADR7	BPADR8
ADR TRAP	0	0	1	1	0	1	X	SR1+/0	SR1-/0	SR2/1	ATRAP4	ATRAP5	ATRAP6	ATRAP7	ATRAP8
USER REG SET	0	1	X	X	X	X	X	SR1+	SR1-	SR2	RCMRF3	RCMRF4	RCMRF5	RCMRF6	RCMRF7
SCRATCH SET 1	1	0	X	X	X	X	X	0	0	0	RCMRF3	RCMRF4	RCMRF5	RCMRF6	RCMRF7
SCRATCH SET 2	1	1	X	X	X	X	X	1	1	0	RCMRF3	RCMRF4	RCMRF5	RCMRF6	RCMRF7

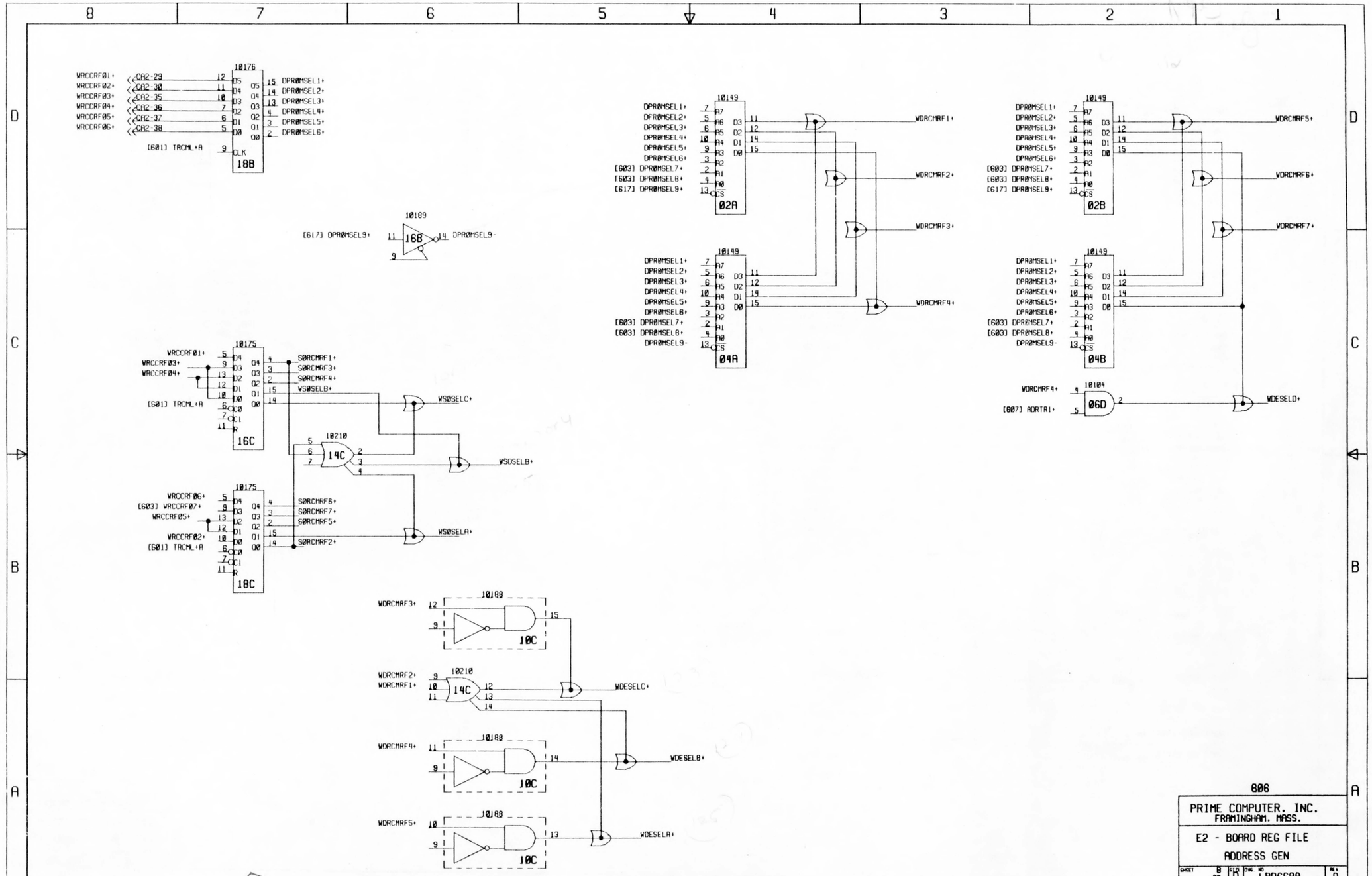
* ZERO GUARANTEED BY HARDWARE (I-UNIT)

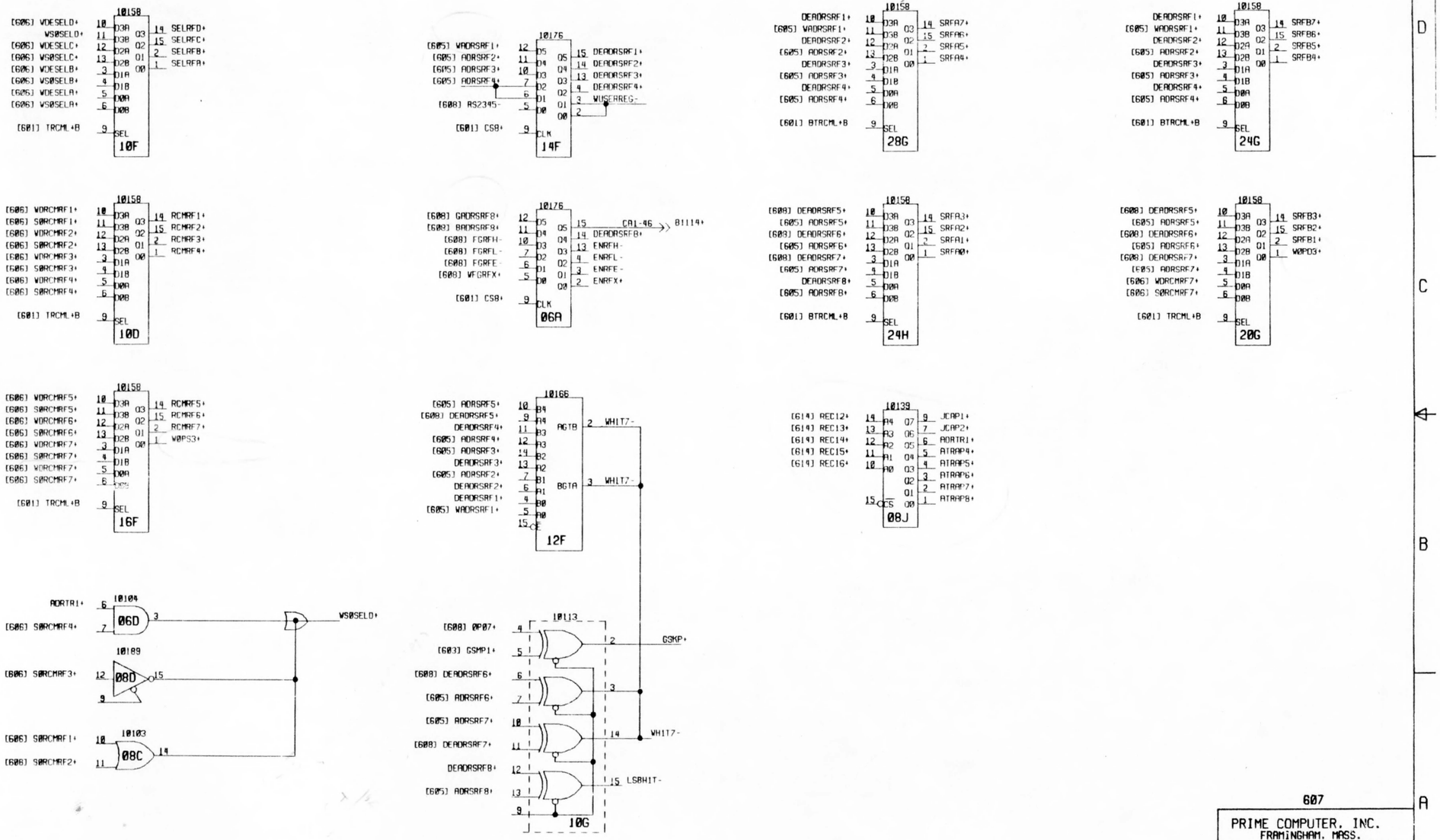
605

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E2 - BOARD RF ADDRESS GEN

SHEET 7 OF 28 | SIZE D | DWG NO LBD6699 | REV A1


10176
WRCCRF01+
WRCCRF02+
WRCCRF03+
WRCCRF04+
WRCCRF05+
WRCCRF06+
CA2:29
CA2:30
CA2:35
CA2:36
CA2:37
CA2:38
DPR0MSEL1+
DPR0MSEL2+
DPR0MSEL3+
DPR0MSEL4+
DPR0MSEL5+
DPR0MSEL6+
[601] TRCML+A
CLK
18B
10109
[617] DPR0MSEL9+
16B
DPR0MSEL9-
10149
DPR0MSEL1+
DPR0MSEL2+
DPR0MSEL3+
DPR0MSEL4+
DPR0MSEL5+
DPR0MSEL6+
[603] DPR0MSEL7+
[603] DPR0MSEL8+
[617] DPR0MSEL9+
02A
WDRCMRF1+
WDRCMRF2+
WDRCMRF3+
WDRCMRF4+
04A
02B
WDRCMRF5+
WDRCMRF6+
WDRCMRF7+
04B
10175
WRCCRF01+
WRCCRF03+
WRCCRF04+
[601] TRCML+A
16C
SØRCMRF1+
SØRCMRF3+
SØRCMRF4+
VSØSELB+
VSØSELC+
10210
14C
VSOSELB+
WRCCRF06+
[603] WRCCRF07+
WRCCRF05+
WRCCRF02+
[601] TRCML+A
18C
SØRCMRF6+
SØRCMRF7+
SØRCMRF5+
SØRCMRF2+
VSØSELA+
10188
WDRCMRF3+
10C
WDRCMRF2+
WDRCMRF1+
WDESELC+
WDRCMRF4+
WDESELB+
WDRCMRF5+
WDESELA+
10104
WDRCMRF4+
[607] ADRTR1+
06D
WDESELD+
606
PRIME COMPUTER. INC.
FRAMINGHAM. MASS.
E2 - BOARD REG FILE
ADDRESS GEN
SHEET 8 OF 20
SIZE D
DWG NO LBD6699
REV A



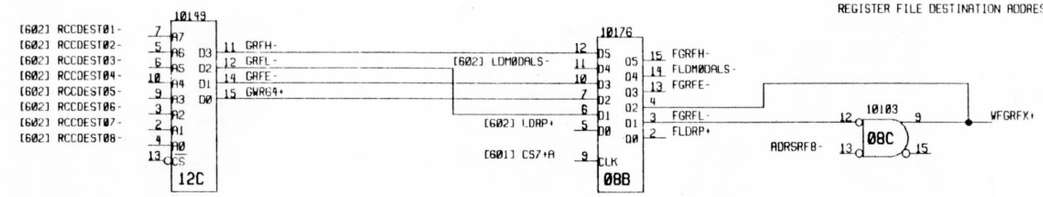
607

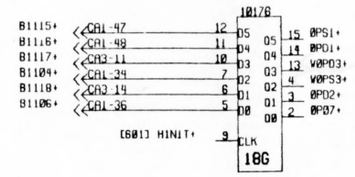
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

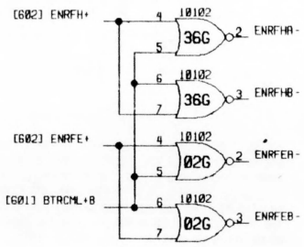
E2 - BOARD REGISTER,
FILE ADDRESS GENERATION

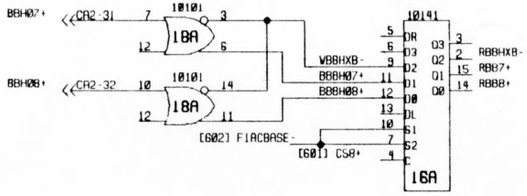
SHEET OF	SIZE	DWG NO	REV
9 28	D	LBD6699	A1

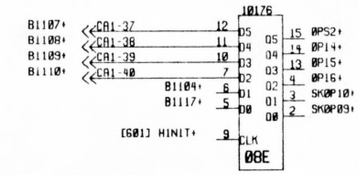
RFX IS CLOCKED IF A 64 BIT WRITE IS SPECIFIED BY THE DESTINATION FIELD, OR IF RFL IS BEING CLOCKED AND THE REGISTER FILE DESTINATION ADDRESS IS ODD.



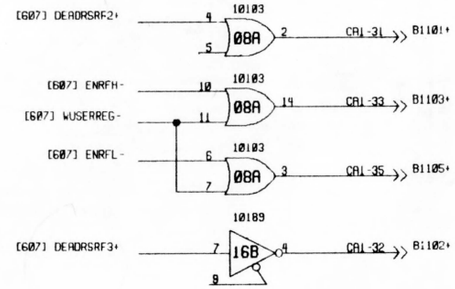


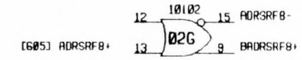


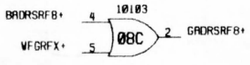


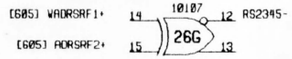


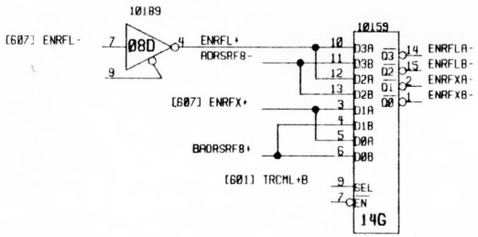
THE LSB OF THE REGISTER FILE ADDRESS, SENT TO THE I-UNIT, IS FORCED TO A ONE IF RFX IS BEING WRITTEN.

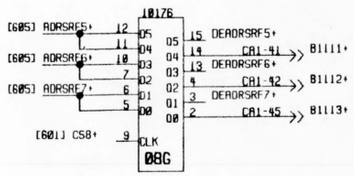










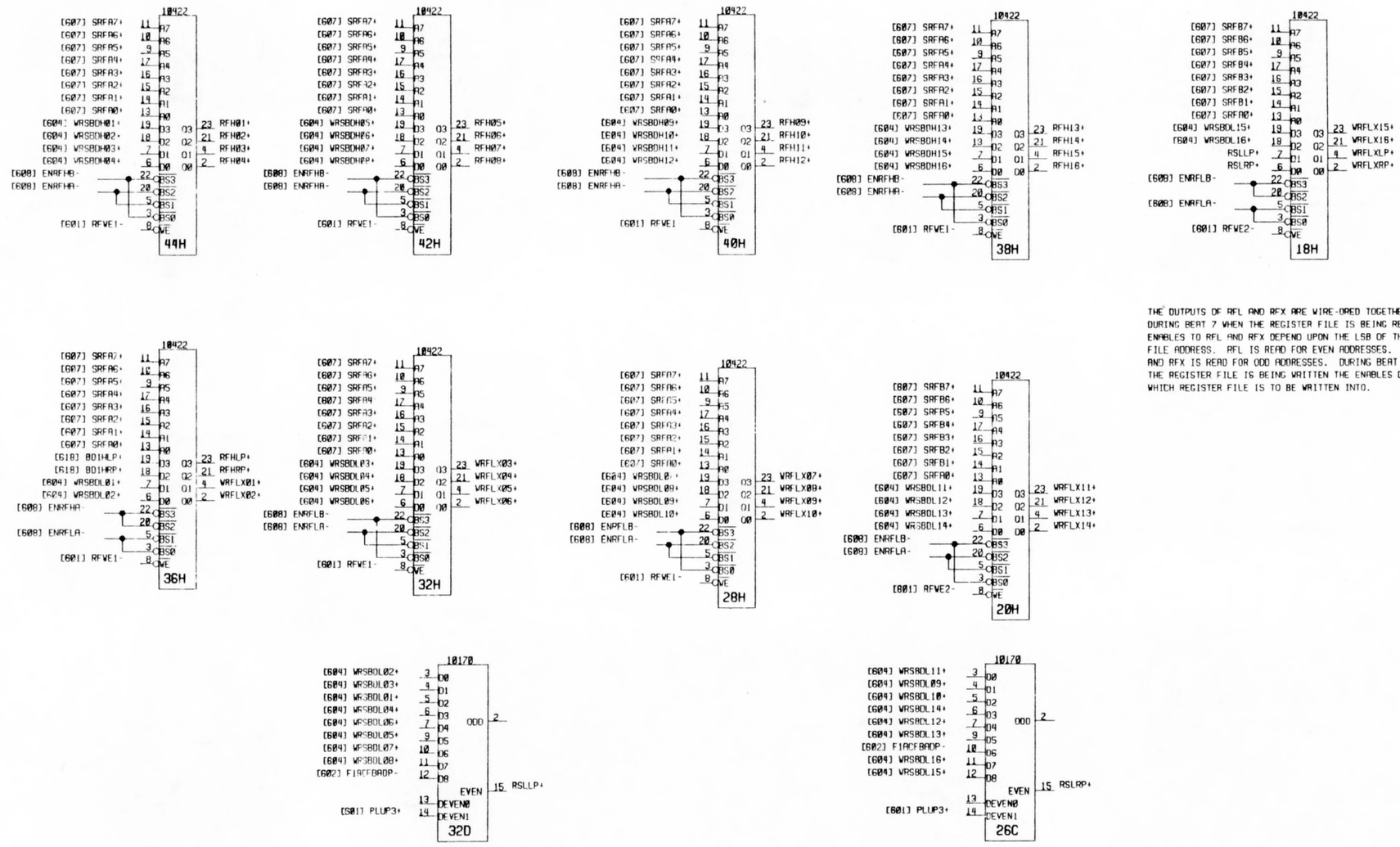


608

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E2 - BOARD REGISTER FILE ADDRESS GENERATION ENABLES. BIT BUS

SHEET 10 OF 28 | SIZE D | DWG NO LBD6699 | REV A



THE OUTPUTS OF RFL AND RFX ARE WIRE-ORED TOGETHER. DURING BEAT 7 WHEN THE REGISTER FILE IS BEING READ THE ENABLES TO RFL AND RFX DEPEND UPON THE LSB OF THE REGISTER FILE ADDRESS. RFL IS READ FOR EVEN ADDRESSES. AND RFX IS READ FOR ODD ADDRESSES. DURING BEAT 10 WHEN THE REGISTER FILE IS BEING WRITTEN THE ENABLES DEPEND UPON WHICH REGISTER FILE IS TO BE WRITTEN INTO.

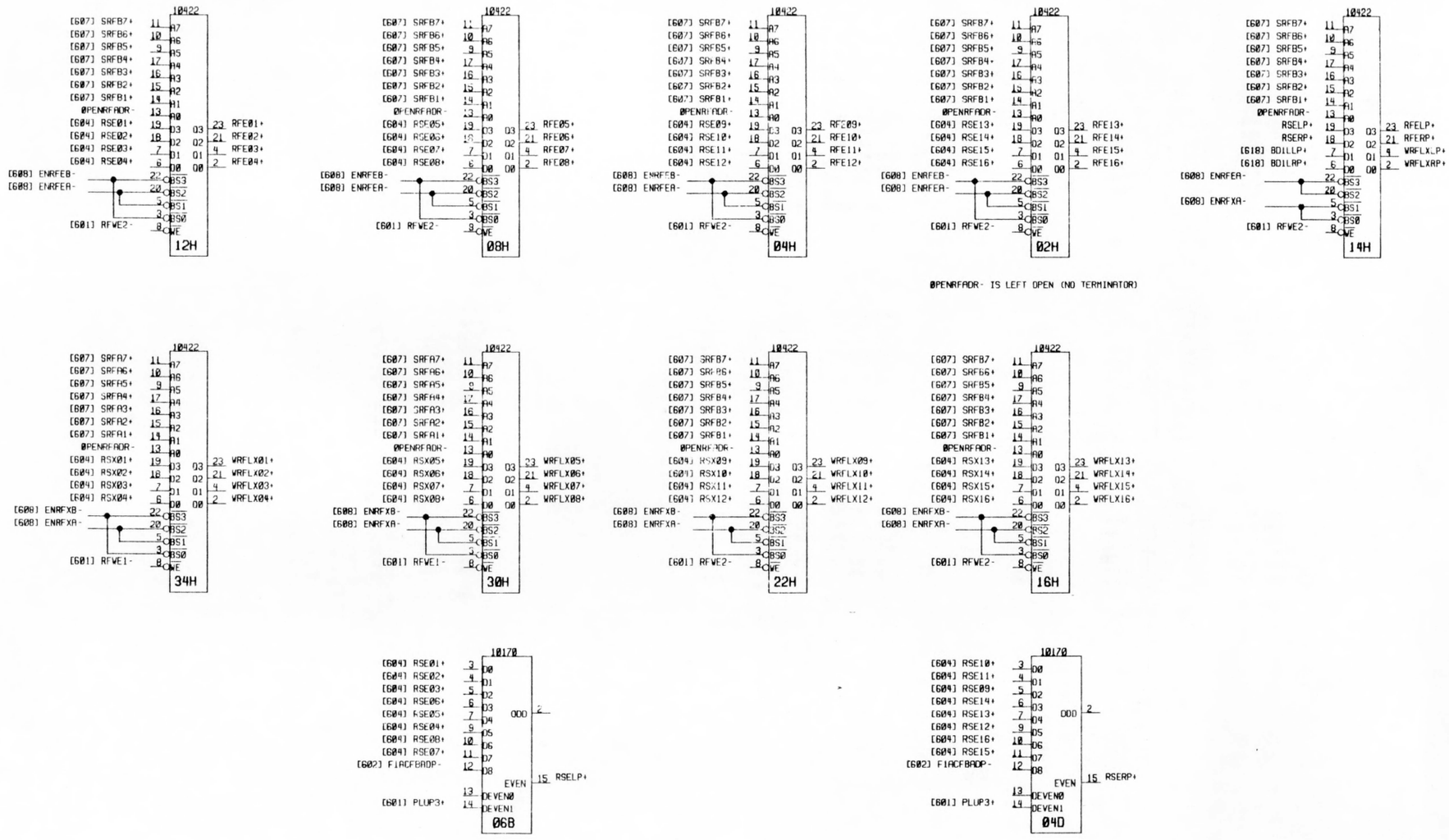
609

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E2 - BOARD REG FILE

RFH, RL

SHEET 11 OF 28 | SIZE D | DWG NO LBD6699 | REV A



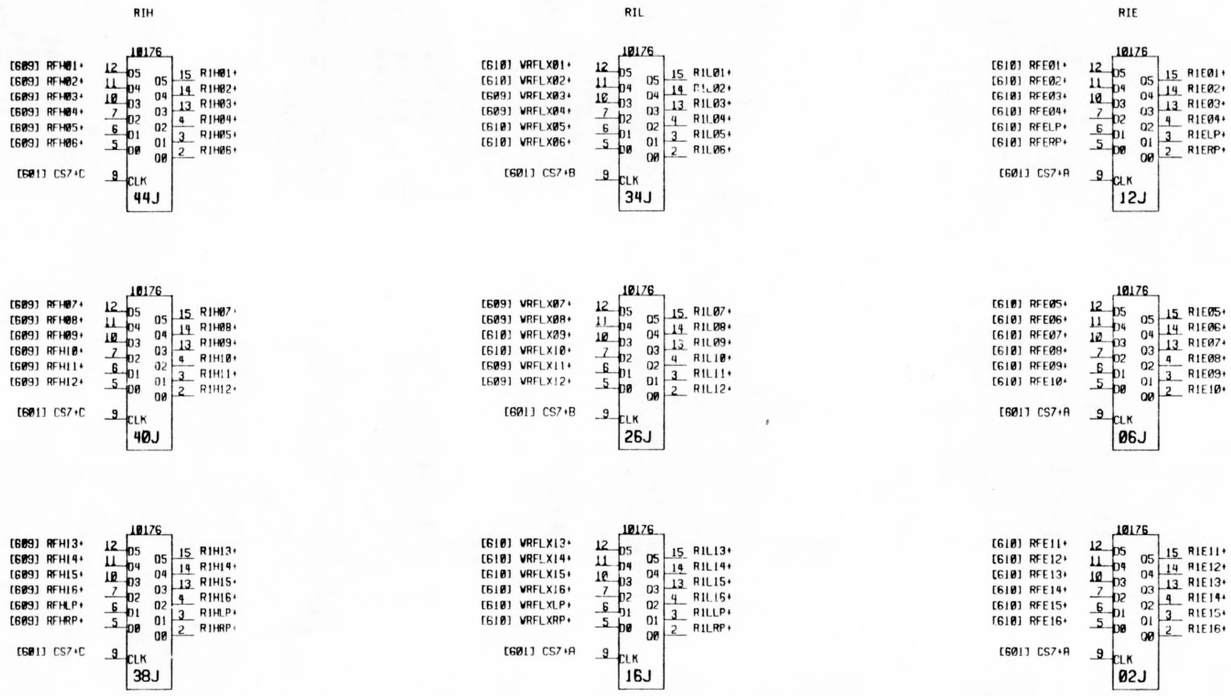
610

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E2 - BOARD REG FILE

RFE. RFX

SHEET 12 OF 28 | SIZE D | DWG NO LBD6699 | REV A

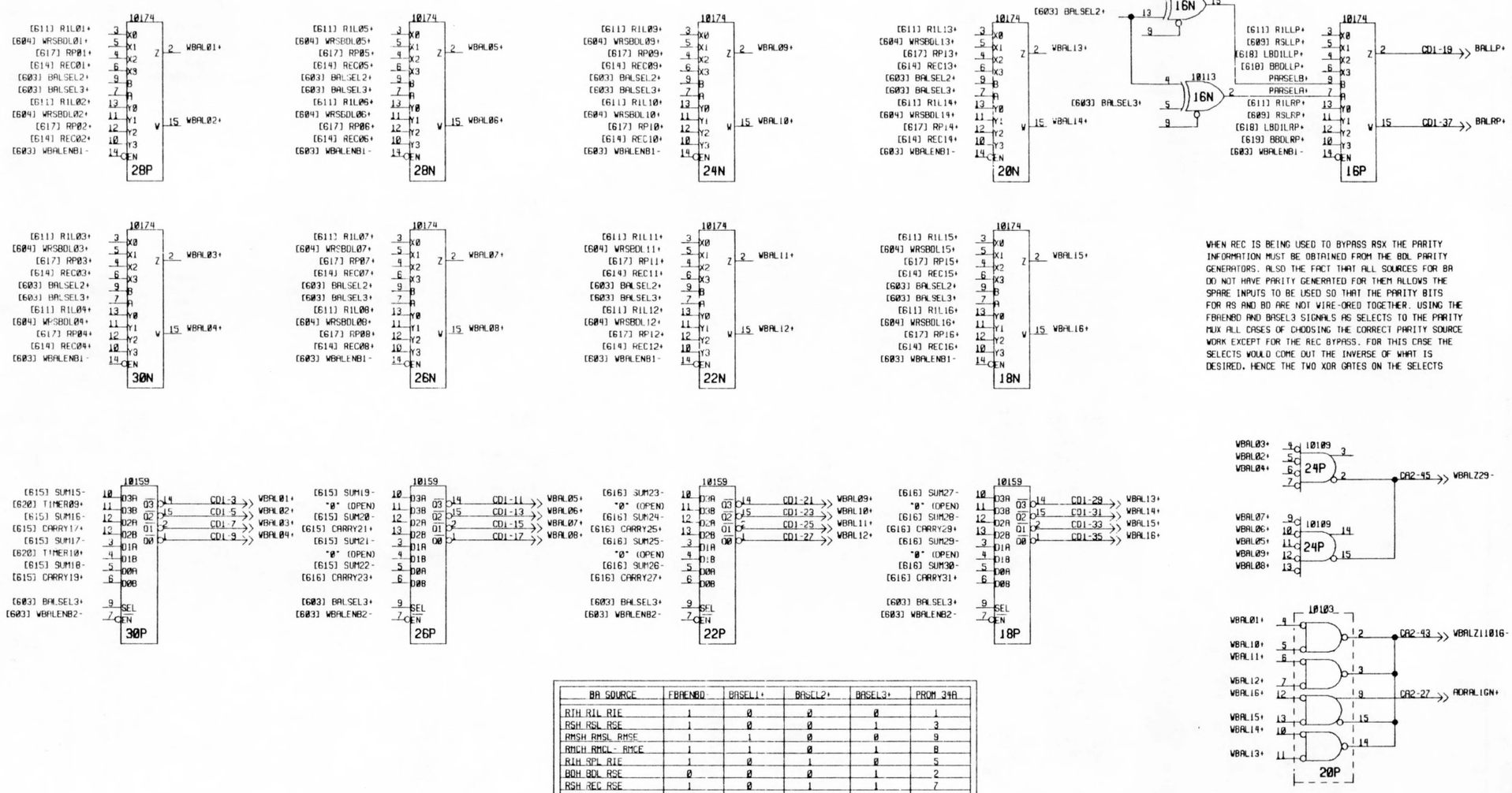


611

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E2 - BOARD RI

SHEET OF	SIZE	DWG NO	REV
13 28	D	LBD6699	A



BA SOURCE	FBAENBD-	BASEL1+	BASEL2+	BASEL3+	PROM 39A
RTH RIL RIE	1	0	0	0	1
RSH RBL RSE	1	0	0	1	3
RMSH RMSL RMSE	1	1	0	0	9
RMCH RMCL- RMCE	1	1	0	1	B
RTH RPL RIE	1	0	1	0	5
BDH BDL RSE	0	0	0	1	2
RSH REC RSE	1	0	1	1	7
0 0 0	1	1	1	X	F

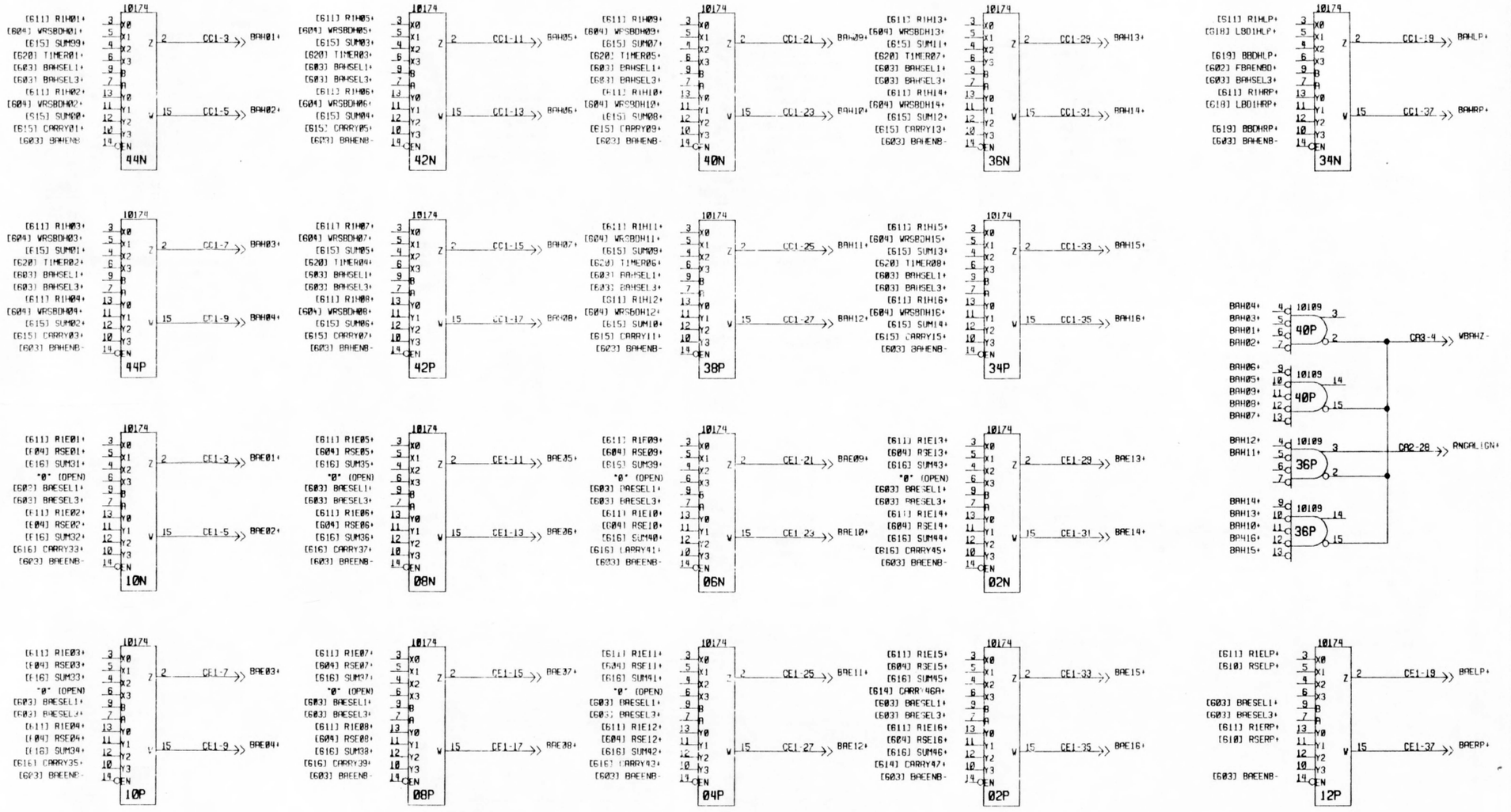
THIS TABLE SHOWS THE CONTROL SIGNALS FOR EACH OF THE POSSIBLE BA SOURCES. NOTE THAT IF A REGISTER COLLISION OCCURS BASEL3+ IS FORCED TO A ONE AND IF REC IS TO BE BYPASSED BASEL2+ IS ALSO FORCED TO A ONE

612

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E2 - BOARD BAL MUX

SHEET 14 OF 28 | SIZE D | DWG NO LBD6699 | REV A1

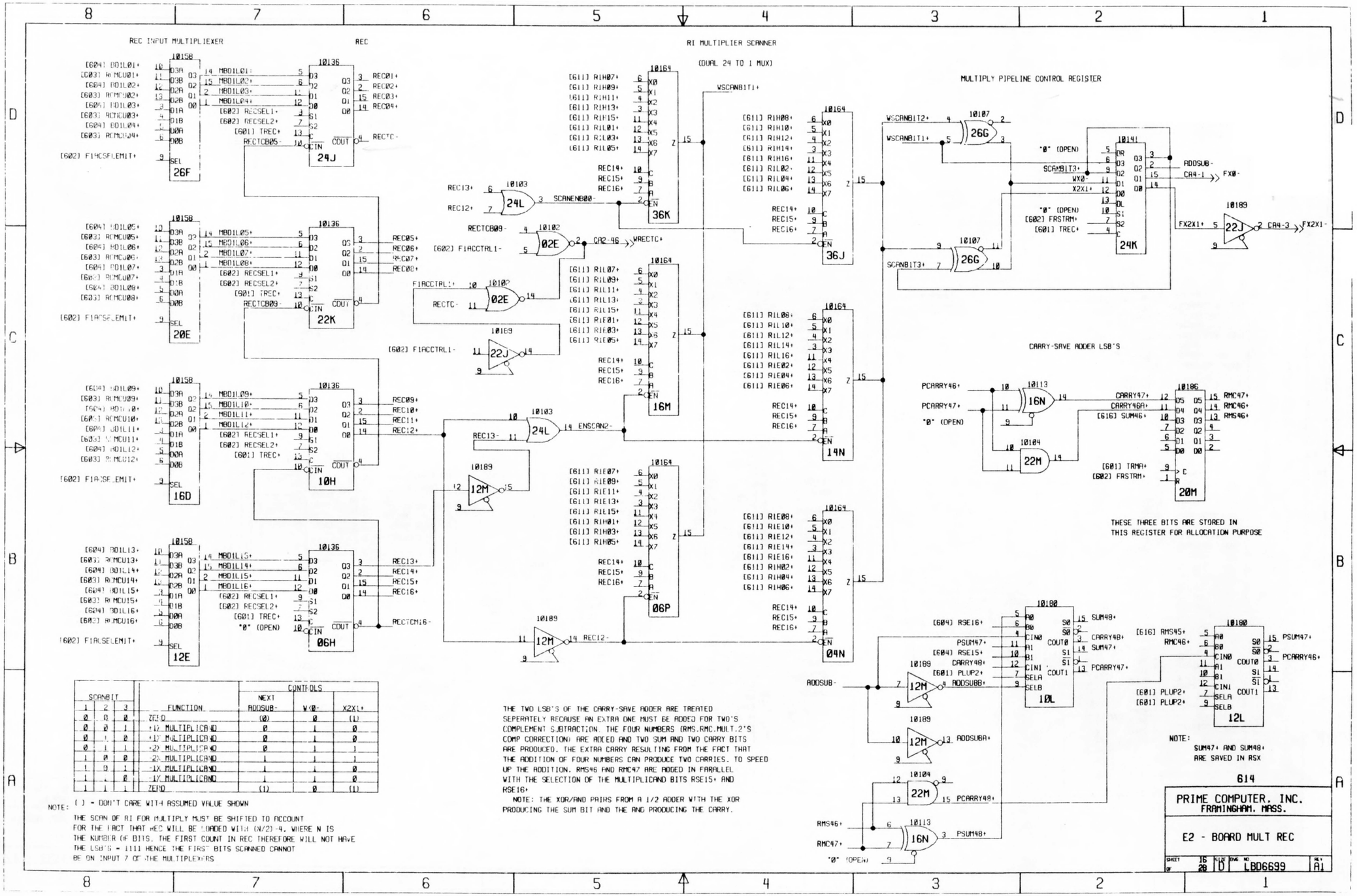


613

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E2 - BOARD BAH MUX &
BAE MUX

SHEET 15 OF 28 | SIZE D | DWG NO LBD5699 | REV A



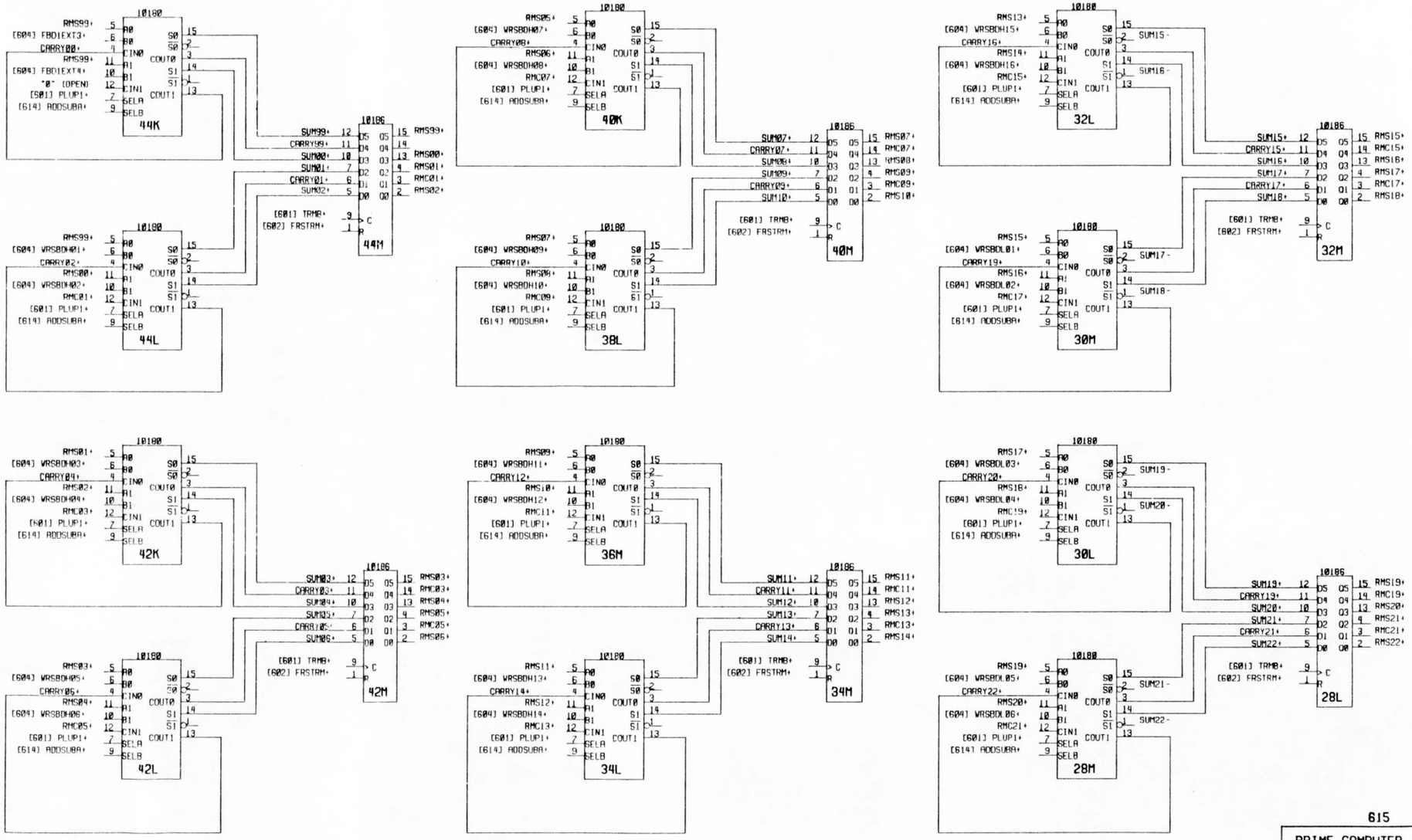
SCANBIT 1	2	3	FUNCTION	CONTROLS NEXT ADDSUB-	W(0)-	X2X1+
0	0	0	ZERO	(0)	0	(1)
0	0	1	+1*2 MULTIPLICAND	0	1	0
0	1	0	+1*1 MULTIPLICAND	0	1	0
0	1	1	+2*2 MULTIPLICAND	0	1	1
1	0	0	-2*2 MULTIPLICAND	1	1	1
1	0	1	-1*1 MULTIPLICAND	1	1	0
1	1	0	-1*1 MULTIPLICAND	1	1	0
1	1	1	ZERO	(1)	0	(1)

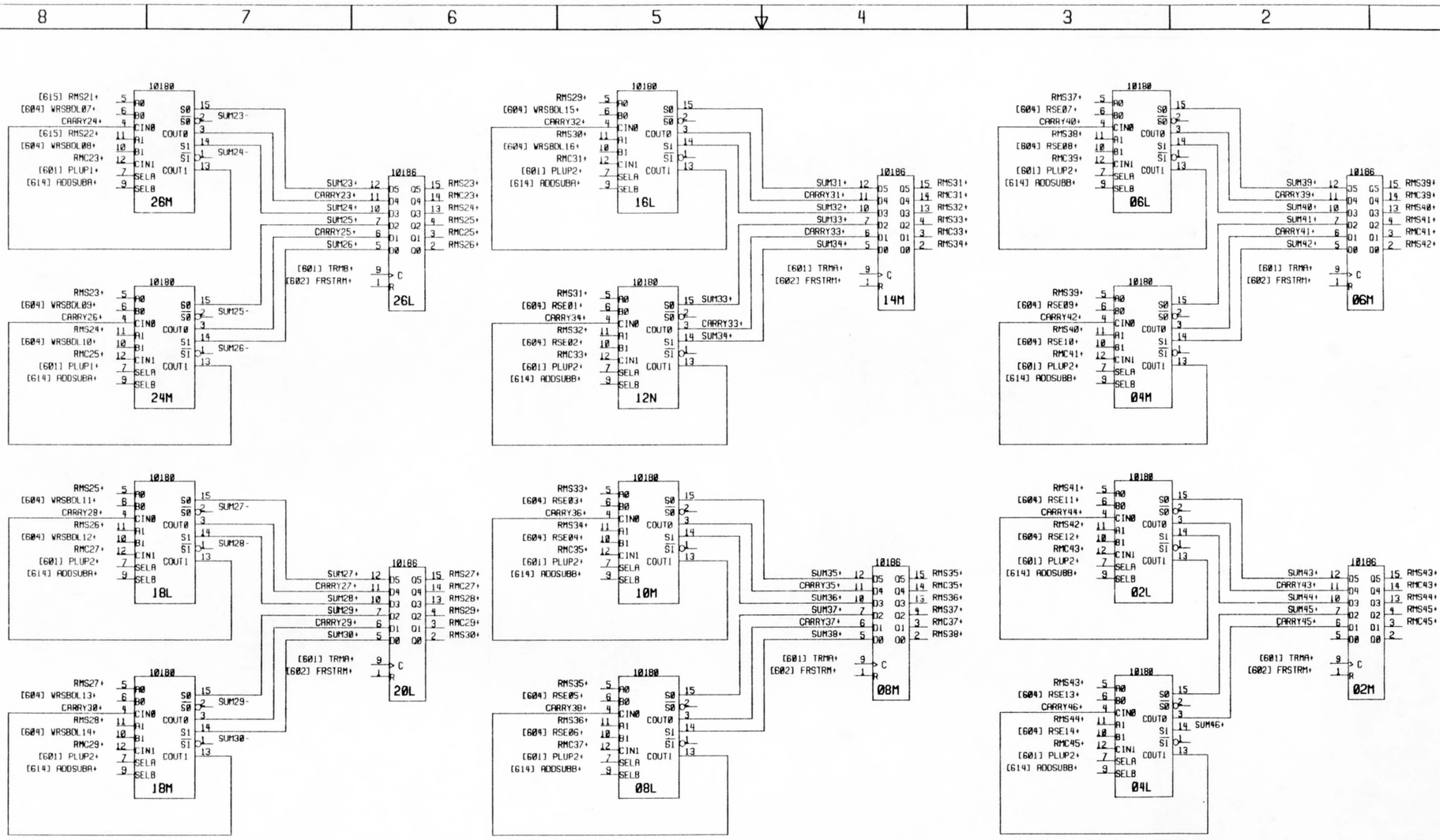
NOTE: ( ) = DON'T CARE WITH ASSUMED VALUE SHOWN

THE SCAN OF RI FOR MULTIPLY MUST BE SHIFTED TO ACCOUNT FOR THE FACT THAT REC WILL BE LOADED WITH (N/2)-4, WHERE N IS THE NUMBER OF BITS. THE FIRST COUNT IN REC THEREFORE WILL NOT HAVE THE LSB'S = 1111 HENCE THE FIRST BITS SCANNED CANNOT BE ON INPUT 7 OF THE MULTIPLEXERS

THE TWO LSB'S OF THE CARRY-SAVE ADDER ARE TREATED SEPERATELY BECAUSE AN EXTRA ONE MUST BE ADDED FOR TWO'S COMPLEMENT SUBTRACTION. THE FOUR NUMBERS (RMS,RMC,MULT,2'S COMP CORRECTION) ARE ADDED AND TWO SUM AND TWO CARRY BITS ARE PRODUCED. THE EXTRA CARRY RESULTING FROM THE FACT THAT THE ADDITION OF FOUR NUMBERS CAN PRODUCE TWO CARRIES. TO SPEED UP THE ADDITION, RMS46 AND RMC47 ARE ADDED IN FARALLEL WITH THE SELECTION OF THE MULTIPLICAND BITS RSE15+ AND RSE16+

NOTE: THE XOR/AND PAIRS FROM A 1/2 ADDER WITH THE XOR PRODUCING THE SUM BIT AND THE AND PRODUCING THE CARRY.


44K
44M
44L
40K
40M
38L
32L
32M
30M
42K
42M
42L
36M
34M
34L
30L
28L
28M
615
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E2 - BOARD MULTIPLIER
99 TO 22
LBD6699
A



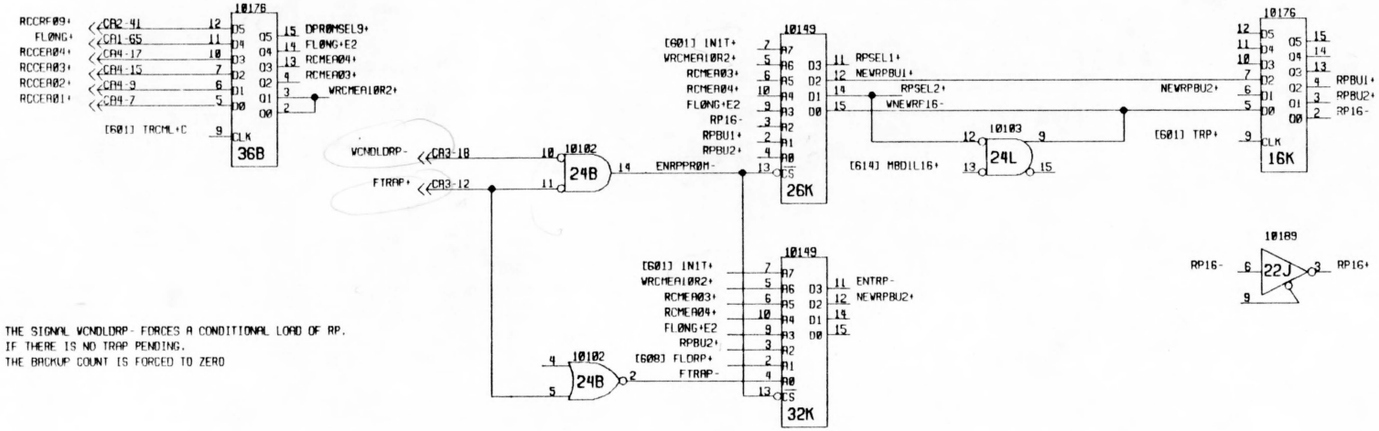
616

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E2 - BOARD MULTIPLIER

23 TO 46

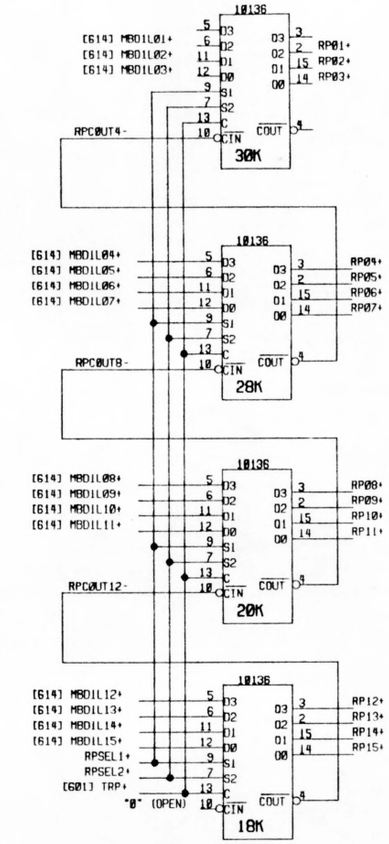
SHEET OF	SIZE	DWG NO	REV
18 20	D	LBD6699	A



THE SIGNAL WCNDLDRP- FORCES A CONDITIONAL LOAD OF RP.
IF THERE IS NO TRAP PENDING.
THE BACKUP COUNT IS FORCED TO ZERO

S1	S2	MODE
0	0	LOAD
0	1	INC
1	0	DEC (NOT USED)
1	1	HOLD

RP COUNTER

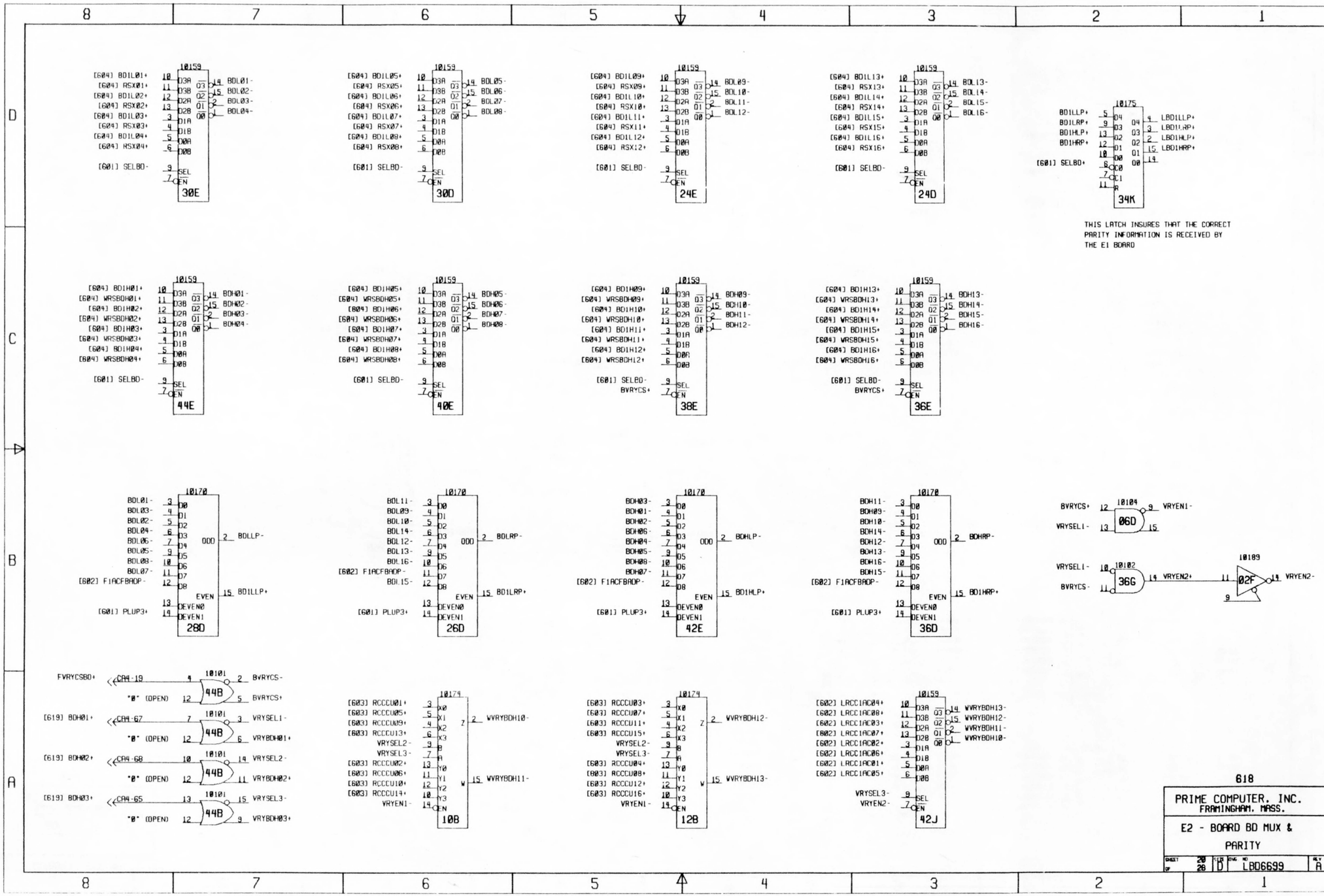


617

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E2 - BOARD RP COUNTER

SHEET 19 OF 20 | SIZE D | DWG NO LBD6699 | REV A1


[604] BDIL01+
[604] RSX01+
[604] BDIL02+
[604] RSX02+
[604] BDIL03+
[604] RSX03+
[604] BDIL04+
[604] RSX04+
[601] SELBD-
10159
30E
BDL01-
BDL02-
BDL03-
BDL04-
[604] BDIL05+
[604] RSX05+
[604] BDIL06+
[604] RSX06+
[604] BDIL07+
[604] RSX07+
[604] BDIL08+
[604] RSX08+
[601] SELBD-
10159
30D
BDL05-
BDL06-
BDL07-
BDL08-
[604] BDIL09+
[604] RSX09+
[604] BDIL10+
[604] RSX10+
[604] BDIL11+
[604] RSX11+
[604] BDIL12+
[604] RSX12+
[601] SELBD-
10159
24E
BDL09-
BDL10-
BDL11-
BDL12-
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[604] RSX13+
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[604] BDIL15+
[604] RSX15+
[604] BDIL16+
[604] RSX16+
[601] SELBD-
10159
24D
BDL13-
BDL14-
BDL15-
BDL16-
BDILLP+
BDILRP+
BDIHLP+
BDIHRP+
[601] SELBD+
10175
34K
LBDILLP+
LBDILRP+
LBDIHLP+
LBDIHRP+
THIS LATCH INSURES THAT THE CORRECT
PARITY INFORMATION IS RECEIVED BY
THE E1 BOARD
[604] BDIH01+
[604] WRSBDH01+
[604] BDIH02+
[604] WRSBDH02+
[604] BDIH03+
[604] WRSBDH03+
[604] BDIH04+
[604] WRSBDH04+
[601] SELBD-
10159
44E
BDH01-
BDH02-
BDH03-
BDH04-
[604] BDIH05+
[604] WRSBDH05+
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[604] WRSBDH06+
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[604] WRSBDH07+
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[604] WRSBDH08+
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10159
40E
BDH05-
BDH06-
BDH07-
BDH08-
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[604] WRSBDH09+
[604] BDIH10+
[604] WRSBDH10+
[604] BDIH11+
[604] WRSBDH11+
[604] BDIH12+
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BVRYCS+
10159
38E
BDH09-
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BDH11-
BDH12-
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BVRYCS+
10159
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BDH14-
BDH15-
BDH16-
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BDL03-
BDL02-
BDL04-
BDL06-
BDL05-
BDL08-
BDL07-
[602] F1ACFBADP-
[601] PLUP3+
10170
28D
ODD
EVEN
DEVEN0
DEVEN1
BDLLP-
BDILLP+
BDL11-
BDL09-
BDL10-
BDL14-
BDL12-
BDL13-
BDL16-
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BDL15-
[601] PLUP3+
10170
26D
ODD
EVEN
DEVEN0
DEVEN1
BDLRP-
BDILRP+
BDH03-
BDH01-
BDH02-
BDH06-
BDH04-
BDH05-
BDH08-
BDH07-
[602] F1ACFBADP-
[601] PLUP3+
10170
42E
ODD
EVEN
DEVEN0
DEVEN1
BDHLP-
BDIHLP+
BDH11-
BDH09-
BDH10-
BDH14-
BDH12-
BDH13-
BDH16-
BDH15-
[602] F1ACFBADP-
[601] PLUP3+
10170
36D
ODD
EVEN
DEVEN0
DEVEN1
BDHRP-
BDIHRP+
BVRYCS+
VRYSEL1-
10104
06D
VRYEN1-
VRYSEL1-
BVRYCS-
10102
36G
VRYEN2+
10189
02F
VRYEN2-
FVRYCSBD+
CA4-19
"0" (OPEN)
10101
44B
BVRYCS-
BVRYCS+
[619] BDH01+
CA4-67
"0" (OPEN)
10101
44B
VRYSEL1-
VRYBDH01+
[619] BDH02+
CA4-68
"0" (OPEN)
10101
44B
VRYSEL2-
VRYBDH02+
[619] BDH03+
CA4-65
"0" (OPEN)
10101
44B
VRYSEL3-
VRYBDH03+
[603] RCCCU01+
[603] RCCCU05+
[603] RCCCU09+
[603] RCCCU13+
VRYSEL2-
VRYSEL3-
[603] RCCCU02+
[603] RCCCU06+
[603] RCCCU10+
[603] RCCCU14+
VRYEN1-
10179
10B
WVRYBDH10-
WVRYBDH11-
[603] RCCCU03+
[603] RCCCU07+
[603] RCCCU11+
[603] RCCCU15+
VRYSEL2-
VRYSEL3-
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[603] RCCCU12+
[603] RCCCU16+
VRYEN1-
10179
12B
WVRYBDH12-
WVRYBDH13-
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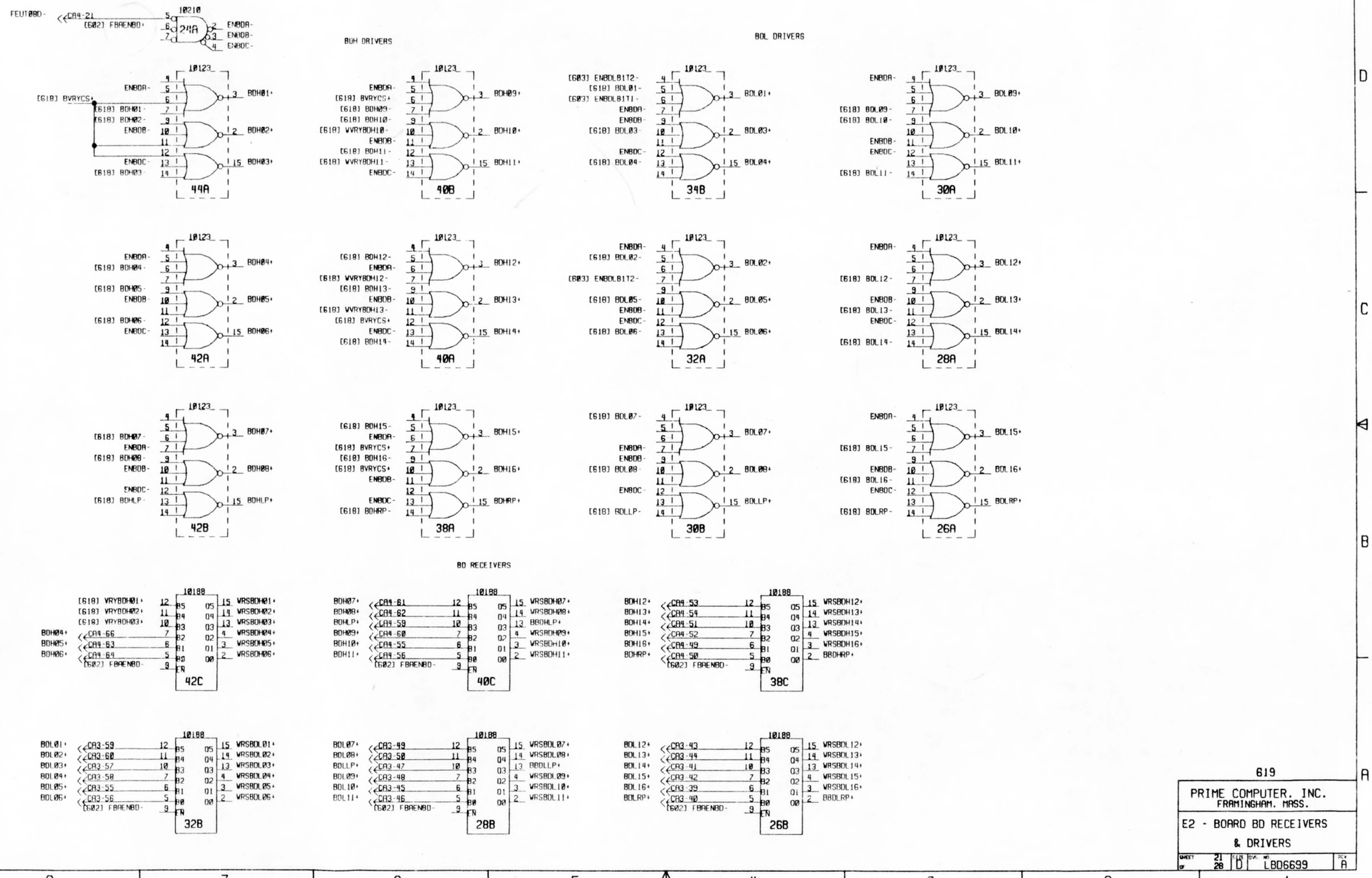
[602] LRCC1AC08+
[602] LRCC1AC03+
[602] LRCC1AC07+
[602] LRCC1AC02+
[602] LRCC1AC06+
[602] LRCC1AC01+
[602] LRCC1AC05+
VRYSEL3-
VRYEN2-
10159
42J
WVRYBDH13-
WVRYBDH12-
WVRYBDH11-
WVRYBDH10-
618
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E2 - BOARD BD MUX &
PARITY
SHEET OF 20 28
SIZE D
DWG NO LBD6699
REV A

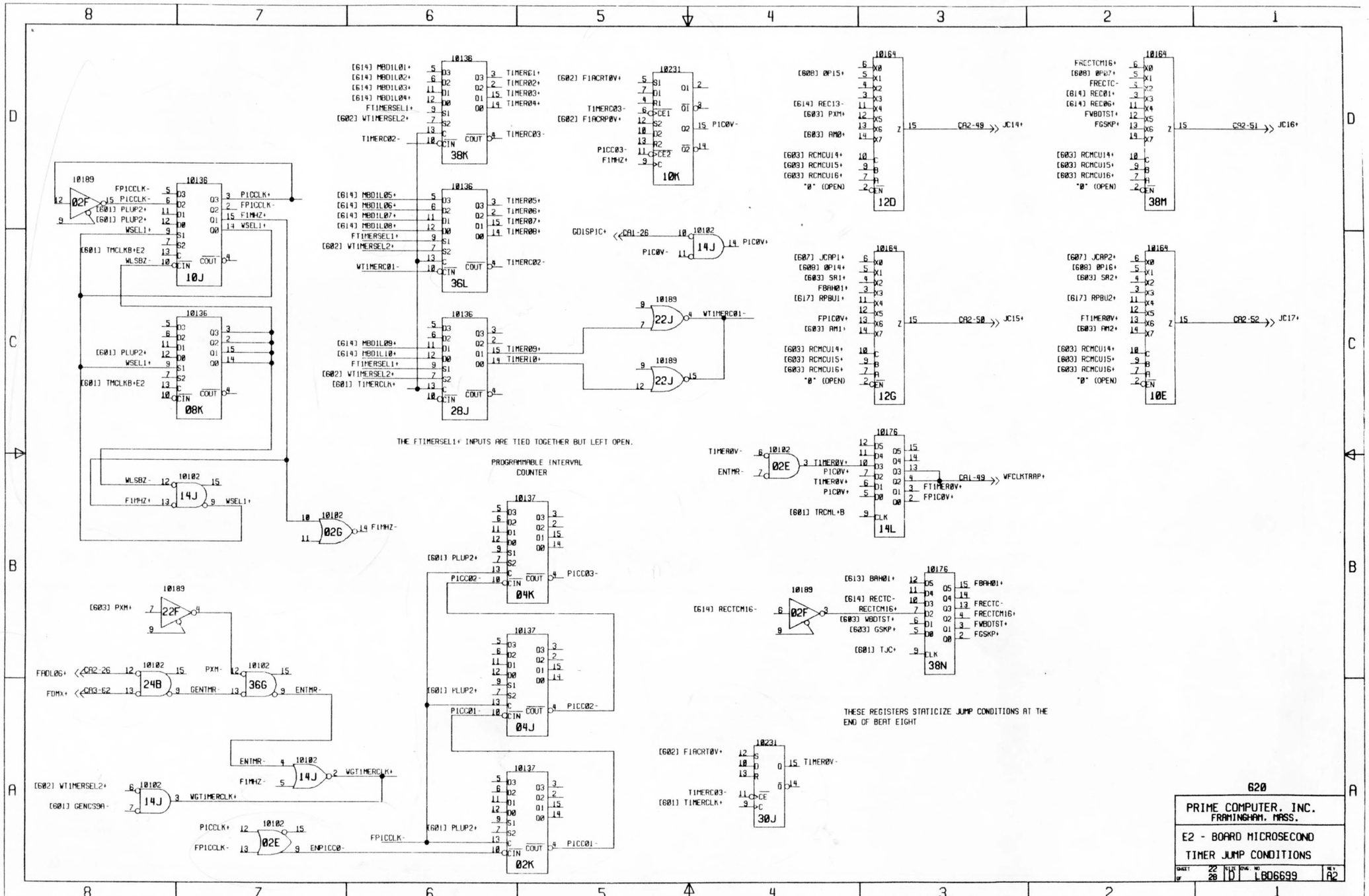


619

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E2 - BOARD BD RECEIVERS & DRIVERS

SHEET 21 OF 28 | SIZE D | DWG NO LBD6699 | REV A


10136 38K
10231 10K
10164 12D
10164 38M
10136 36L
10136 10J
10136 08K
10164 12G
10164 10E
10189 02F
10102 14J
10102 02G
10189 22J
10189 22J
10176 14L
10102 02E
10189 22F
10102 24B
10102 36G
10137 04K
10137 04J
10137 02K
10231 30J
10176 38N
10102 14J
10102 14J
10102 02E
[614] MBD1L01+
[614] MBD1L02+
[614] MBD1L03+
[614] MBD1L04+
FTIMERSEL1+
[602] WTIMERSEL2+
TIMERC02-
TIMERC03-
TIMER01+
TIMER02+
TIMER03+
TIMER04+
[614] MBD1L05+
[614] MBD1L06+
[614] MBD1L07+
[614] MBD1L08+
WTIMERC01-
TIMERC02-
TIMER05+
TIMER06+
TIMER07+
TIMER08+
[614] MBD1L09+
[614] MBD1L10+
[602] WTIMERSEL2+
[601] TIMERCLK+
TIMER09+
TIMER10+
WTIMERC01-
[602] F1ACRT0V+
TIMERC03-
[602] F1ACRP0V+
P1CC03-
F1MHZ+
P1C0V-
GDISP1C+
P1C0V-
P1C0V+
[608] 0P15+
[614] REC13-
[603] PXM+
[603] AM0+
[603] RCMCU14+
[603] RCMCU15+
[603] RCMCU16+
"0" (OPEN)
CA2-49
JC14+
FRECTCM16+
[608] 0P07+
FRECTC-
[614] REC01+
[614] REC06+
FWBDTST+
FGSKP+
CA2-51
JC16+
[607] JCAP1+
[608] 0P14+
[603] SR1+
FBAH01+
[617] RPBU1+
FP1C0V+
[603] AM1+
CA2-50
JC15+
[607] JCAP2+
[608] 0P16+
[603] SR2+
[617] RPBU2+
FTIMER0V+
[603] AM2+
CA2-52
JC17+
THE FTIMERSEL1+ INPUTS ARE TIED TOGETHER BUT LEFT OPEN.
PROGRAMMABLE INTERVAL COUNTER
P1CCLK+
FP1CCLK-
[601] PLUP2+
[601] PLUP2+
WSEL1+
[601] TMCLKB+E2
WLSBZ-
F1MHZ+
WSEL1+
[601] PLUP2+
WSEL1+
[601] TMCLKB+E2
WLSBZ-
F1MHZ+
WSEL1+
F1MHZ-
[603] PXM+
FADL06+
FDMx+
PXM-
GENTMR-
ENTMR-
F1MHZ-
WGTIMERCLK+
[602] WTIMERSEL2+
[601] GENCS9A-
WGTIMERCLK+
P1CCLK+
FP1CCLK-
ENP1CC0-
[601] PLUP2+
P1CC02-
P1CC03-
[601] PLUP2+
P1CC01-
P1CC02-
[601] PLUP2+
FP1CCLK-
P1CC01-
TIMER0V-
ENTMR-
TIMER0V+
P1C0V+
TIMER0V+
P1C0V+
[601] TRCML+B
CA1-49
WFCLKTRAP+
FTIMER0V+
FP1C0V+
[614] RECTCM16-
[613] BAH01+
[614] RECTC-
RECTCM16+
[603] WBDTST+
[603] GSKP+
[601] TJC+
FBAH01+
FRECTC-
FRECTCM16+
FWBDTST+
FGSKP+
THESE REGISTERS STATICIZE JUMP CONDITIONS AT THE END OF BEAT EIGHT
[602] F1ACRT0V+
TIMERC03-
[601] TIMERCLK+
TIMER0V-
620
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
E2 - BOARD MICROSECOND
TIMER JUMP CONDITIONS
SHEET 22 OF 28
SIZE D
DWG. NO. LBD6699
REV. A2

CA1-13 >>GND

CA1-14 >>GND

CA1-27 >>-5.2V

CA1-28 >>-5.2V

CA1-29 >>-5.2V

CA1-30 >>-5.2V

CA1-43 >>-2V

CA1-44 >>-2V

CA1-57 >>GND

CA1-58 >>GND

CA1-59 >>GND

CA1-60 >>GND

CA2-3 >>GND

CA2-4 >>GND

CA2-17 >>-5.2V

CA2-18 >>-5.2V

CA2-19 >>-5.2V

CA2-20 >>-5.2V

CA2-33 >>-2V

CA2-34 >>-2V

CA2-47 >>GND

CA2-48 >>GND

CA2-61 >>GND

CA2-62 >>GND

CA2-63 >>GND

CA2-64 >>GND

CA2-67 >>GND

CA2-70 >>GND

CA3-1 >>GND

CA3-7 >>GND

CA3-8 >>GND

CA3-9 >>GND

CA3-10 >>GND

CA3-23 >>GND

CA3-24 >>GND

CA3-37 >>-2V

CA3-38 >>-2V

CA3-51 >>-5.2V

CA3-52 >>-5.2V

CA3-53 >>-5.2V

CA3-54 >>-5.2V

CA3-67 >>GND

CA3-68 >>GND

CA4-11 >>GND

CA4-12 >>GND

CA4-13 >>GND

CA4-14 >>GND

CA4-27 >>-2V

CA4-28 >>-2V

CA4-41 >>-5.2V

CA4-42 >>-5.2V

CA4-43 >>-5.2V

CA4-44 >>-5.2V

CA4-57 >>GND

CA4-58 >>GND

CC1-1 >>GND

CC1-2 >>GND

CC1-4 >>GND

CC1-6 >>GND

CC1-8 >>GND

CC1-10 >>GND

CC1-12 >>GND

CC1-14 >>GND

CC1-16 >>GND

CC1-18 >>GND

CC1-20 >>GND

CC1-22 >>GND

CC1-24 >>GND

CC1-26 >>GND

CC1-28 >>GND

CC1-30 >>GND

CC1-32 >>GND

CC1-34 >>GND

CC1-36 >>GND

CC1-38 >>GND

CD1-1 >>GND

CD1-2 >>GND

CD1-4 >>GND

CD1-6 >>GND

CD1-8 >>GND

CD1-10 >>GND

CD1-12 >>GND

CD1-14 >>GND

CD1-16 >>GND

CD1-18 >>GND

CD1-20 >>GND

CD1-22 >>GND

CD1-24 >>GND

CD1-26 >>GND

CD1-28 >>GND

CD1-30 >>GND

CD1-32 >>GND

CD1-34 >>GND

CD1-36 >>GND

CD1-38 >>GND

CE1-1 >>GND

CE1-2 >>GND

CE1-4 >>GND

CE1-6 >>GND

CE1-8 >>GND

CE1-10 >>GND

CE1-12 >>GND

CE1-14 >>GND

CE1-16 >>GND

CE1-18 >>GND

CE1-20 >>GND

CE1-22 >>GND

CE1-24 >>GND

CE1-26 >>GND

CE1-28 >>GND

CE1-30 >>GND

CE1-32 >>GND

CE1-34 >>GND

CE1-36 >>GND

CE1-38 >>GND

C177
22
15V 10%
GND 1 + 2 -5.2V

C178
22
15V 10%
GND 1 + 2 -2V

C179
22
15V 10%
GND 1 + 2 -2V

C180
22
15V 10%
GND 1 + 2 -5.2V

NOTES

1. .01 UF AXIAL LEAD CAPACITORS ARE NOT SHOWN BUT
   ARE INSTALLED ABOVE IC'S COLUMNS 4.8.12.16.20.24.28.32.36
   40 & 44 OF ROWS A.C.E.G.J.L & N AND COLUMNS 2.6.10.14.18
   22.26.30.34.38 & 42 OF ROWS B.D.F.H.K.M & P.

2. UNLESS OTHERWISE SPECIFIED :
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS

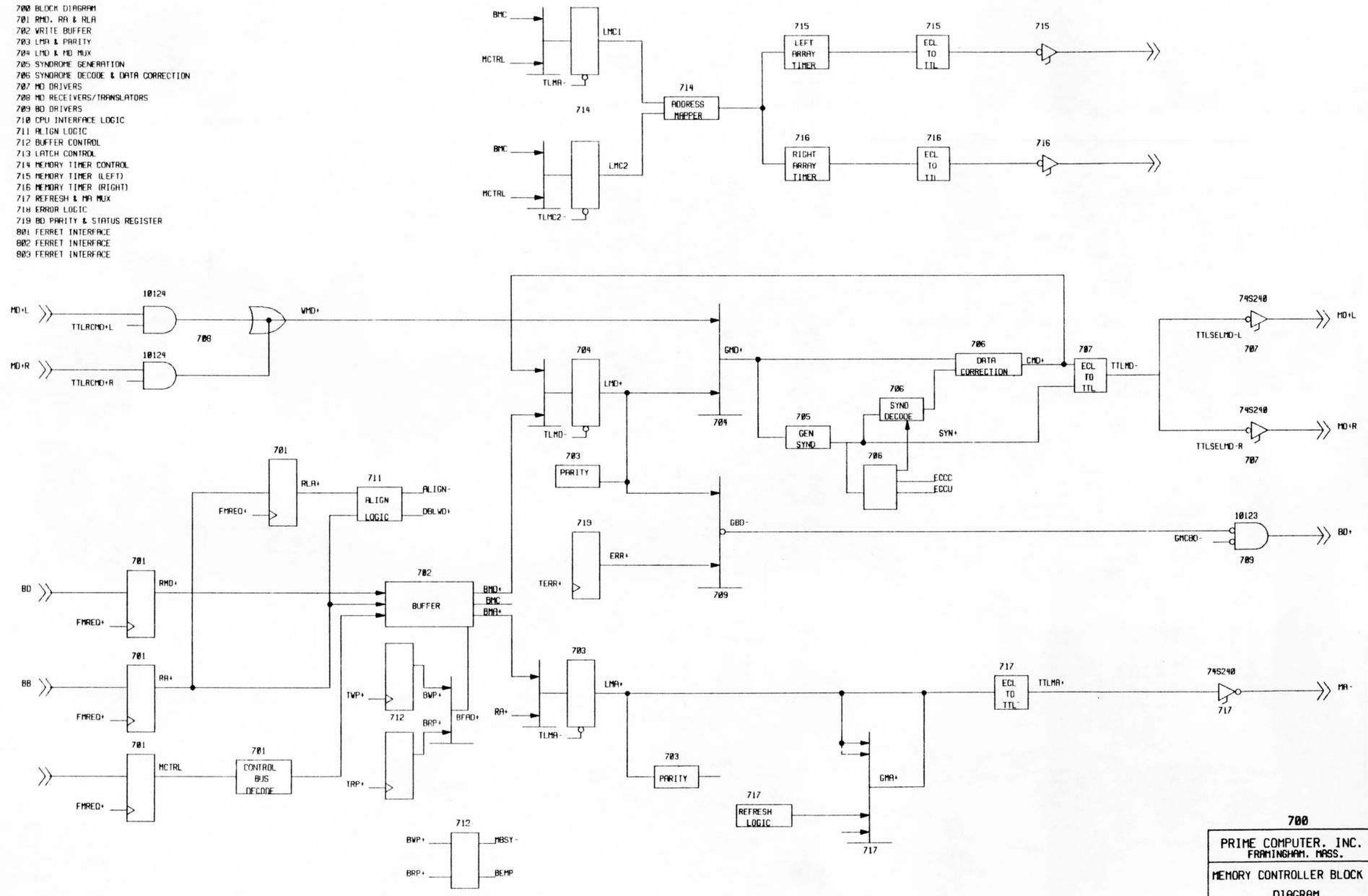
621

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

E2 - BOARD POWER PINS

SHEET OF	SIZE	DWG NO	REV
23 28	D	LBD6699	A

700 BLOCK DIAGRAM
701 RMD, RA & RLA
702 WRITE BUFFER
703 LMA & PARITY
704 LMD & MD MUX
705 SYNDROME GENERATION
706 SYNDROME DECODE & DATA CORRECTION
707 MD DRIVERS
708 MD RECEIVERS/TRANSLATORS
709 BD DRIVERS
710 CPU INTERFACE LOGIC
711 ALIGN LOGIC
712 BUFFER CONTROL
713 LATCH CONTROL
714 MEMORY TIMER CONTROL
715 MEMORY TIMER (LEFT)
716 MEMORY TIMER (RIGHT)
717 REFRESH & MA MUX
718 ERROR LOGIC
719 BD PARITY & STATUS REGISTER
801 FERRET INTERFACE
802 FERRET INTERFACE
803 FERRET INTERFACE

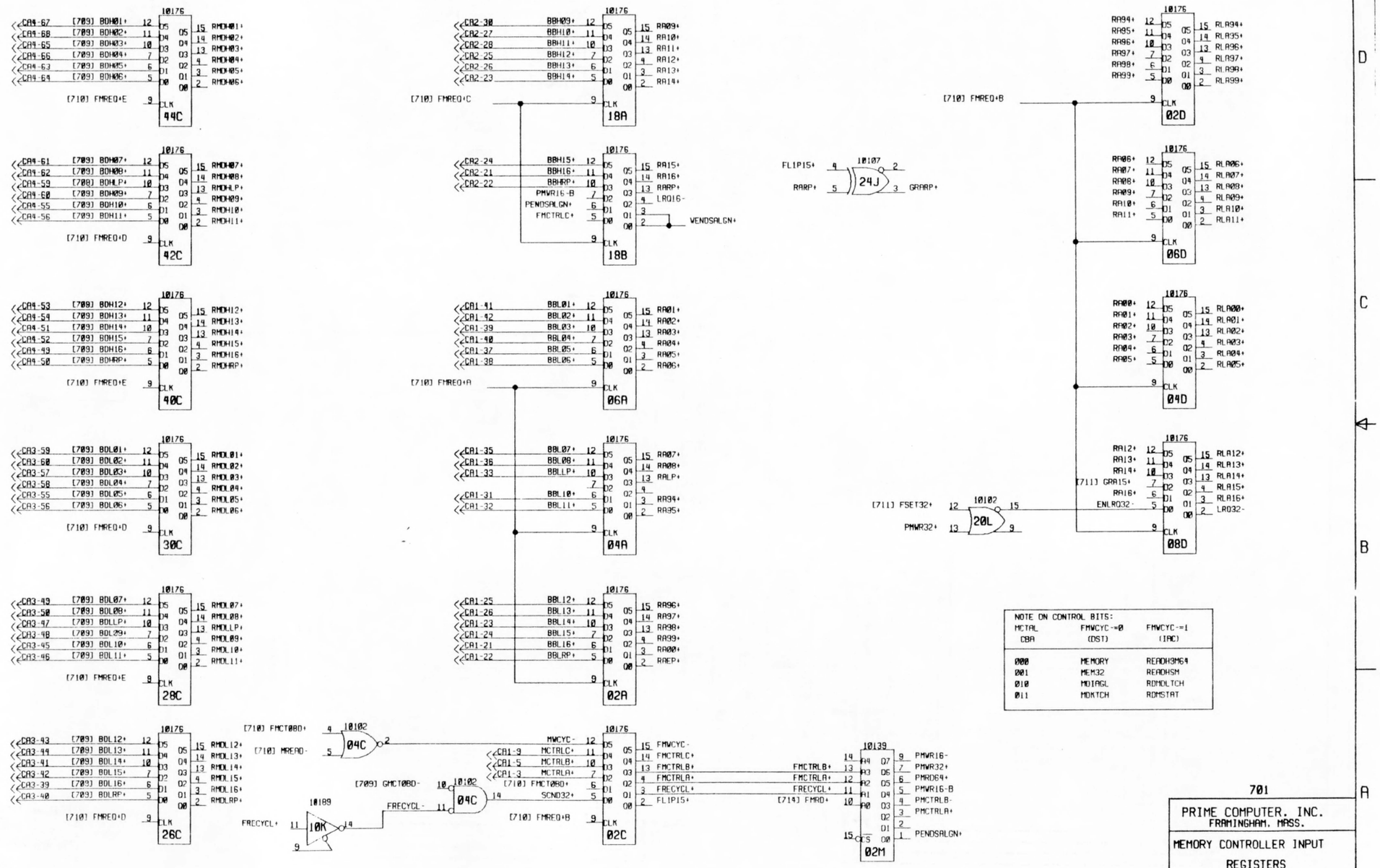


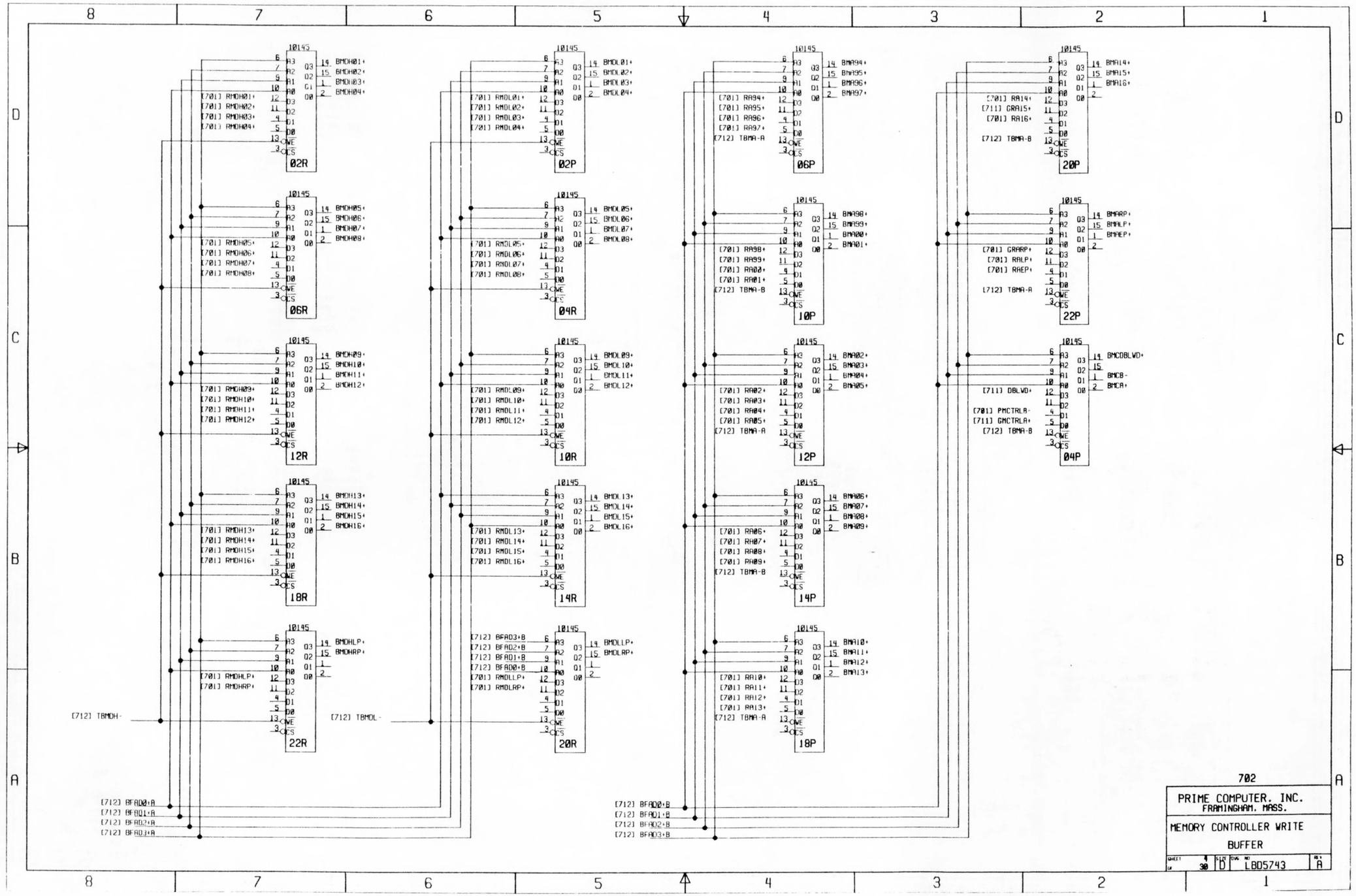
700

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY CONTROLLER BLOCK DIAGRAM

SHEET 2 OF 30 | SIZE D | DWG NO LBD5743 | REV A


10176
44C
42C
40C
30C
28C
26C
18A
18B
06A
04A
02A
02C
02D
06D
04D
08D
10107
24J
10102
20L
10102
04C
10102
04C
10189
10K
10139
02M
[710] FMREQ+E
[710] FMREQ+D
[710] FMREQ+C
[710] FMREQ+A
[710] FMREQ+B
[710] FMCT0B0+
[710] MREAD-
[709] GMCT0B0-
[710] FMCT0B0-
[710] FMREQ+B
FLIP15+
RARP+
GRARP+
[711] FSET32+
PMWR32+
ENLRQ32-
[711] GRA15+
[714] FMRD+
FRECYCL+
FRECYCL-
VENDSALGN+
NOTE ON CONTROL BITS:
MCTRL CBA | FMWCYC-=0 (DST) | FMWCYC-=1 (IAC)
000 | MEMORY | READH3M64
001 | MEM32 | READHSM
010 | MDIAGL | RDMDLTCH
011 | MDXTCH | RDMSTAT
701
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MEMORY CONTROLLER INPUT REGISTERS
SHEET 3 OF 30
SIZE D
DWG NO LBD5743
REV A

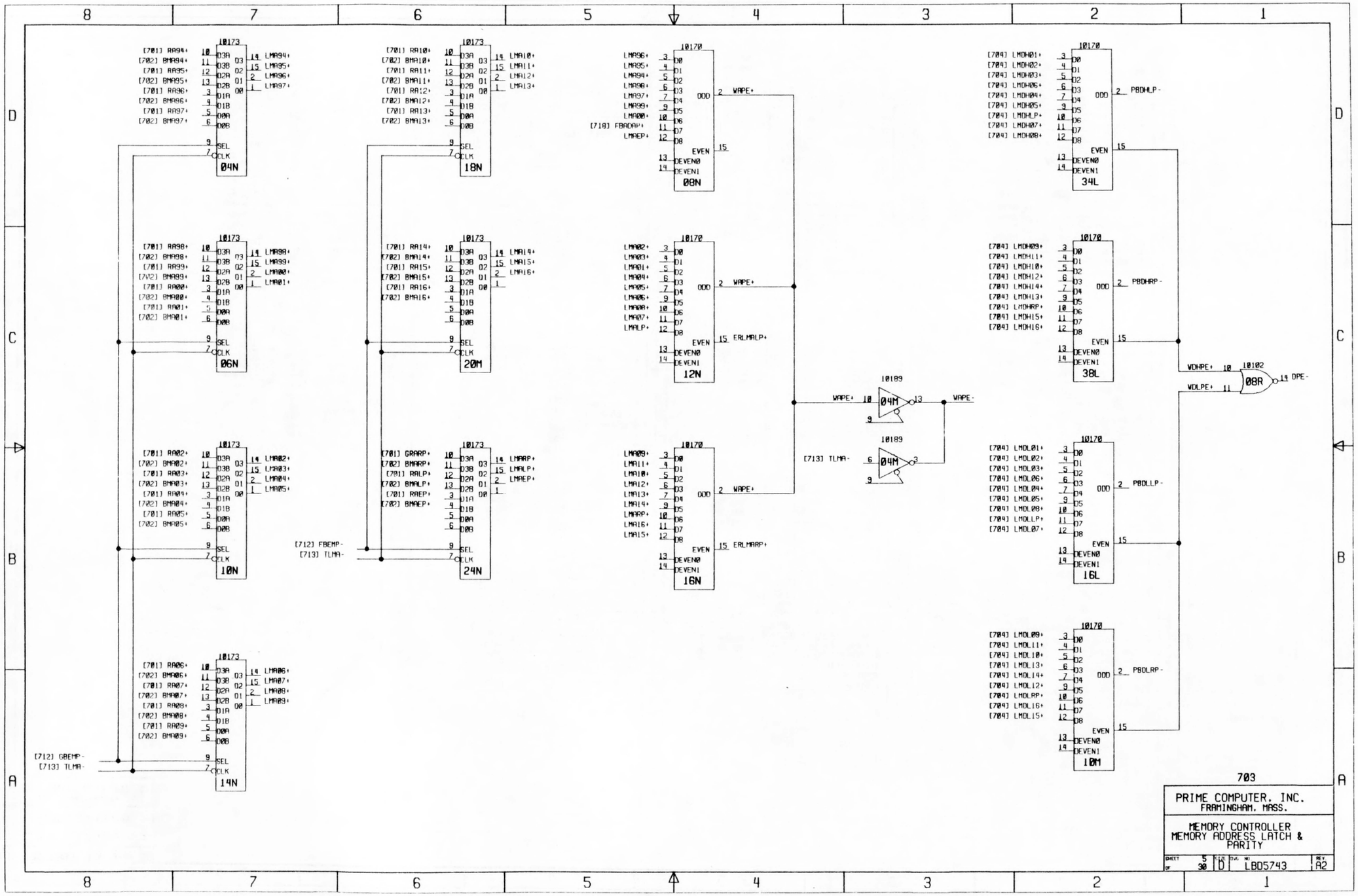


702

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY CONTROLLER WRITE BUFFER

SHEET 30 | SIZE D | DWG NO LBD5743 | REV A


8
7
6
5
4
3
2
1
D
C
B
A
10173
04N
18N
06N
20M
10N
24N
14N
10170
08N
12N
16N
34L
38L
16L
10M
10189
04M
10102
08R
[701] RA94+
[702] BMA94+
[701] RA95+
[702] BMA95+
[701] RA96+
[702] BMA96+
[701] RA97+
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LMA94+
LMA95+
LMA96+
LMA97+
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LMA95+
LMA94+
LMA98+
LMA97+
LMA99+
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LMA16+
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LMA03+
LMA01+
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LMA05+
LMA06+
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LMA07+
LMALP+
ERLMALP+
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ERLMARP+
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LMA09+
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PBDHLP-
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PBDHRP-
WDHPE+
WDLPE+
DPE-
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[704] LMDL07+
PBDLLP-
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[704] LMDL14+
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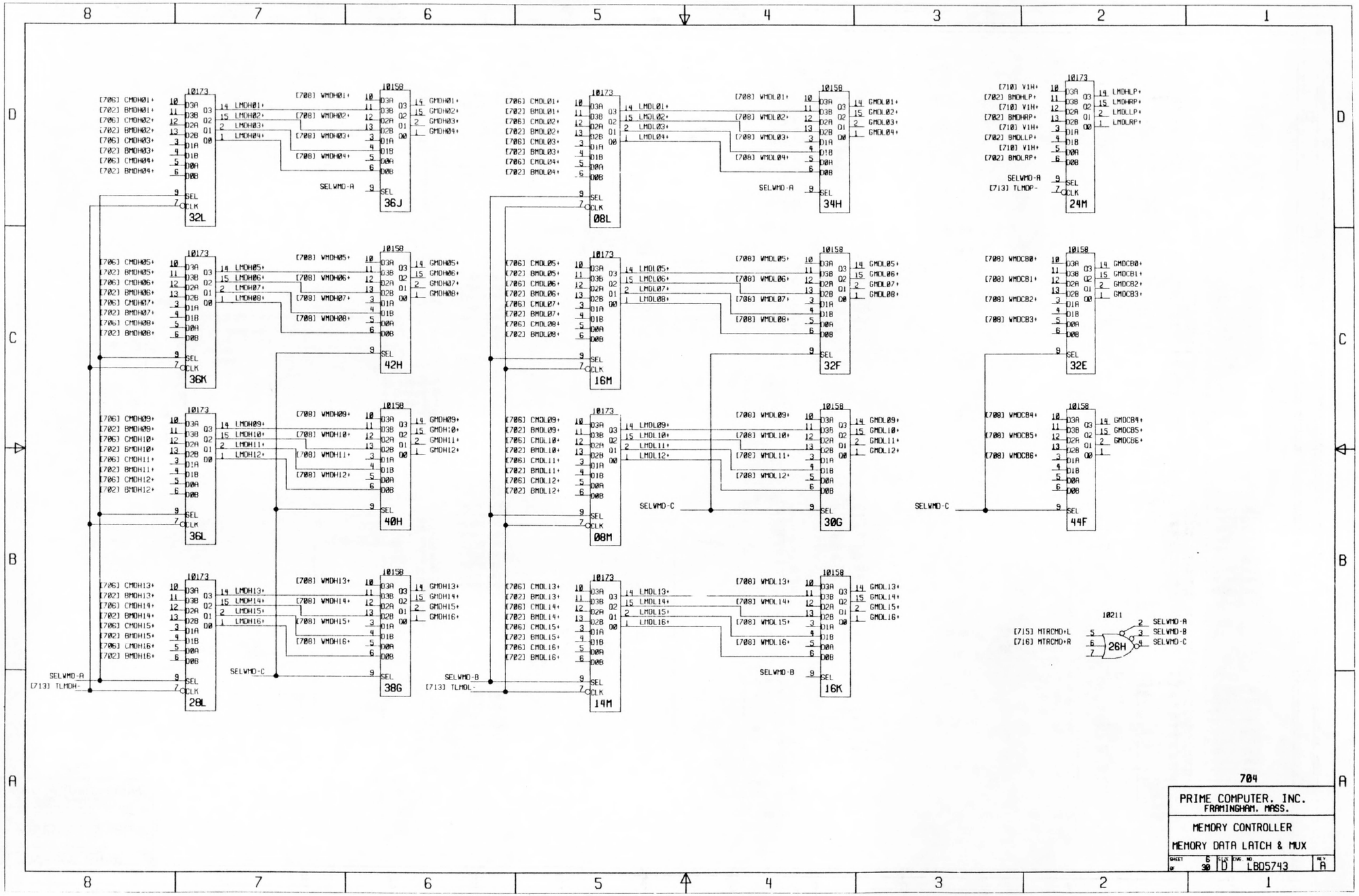
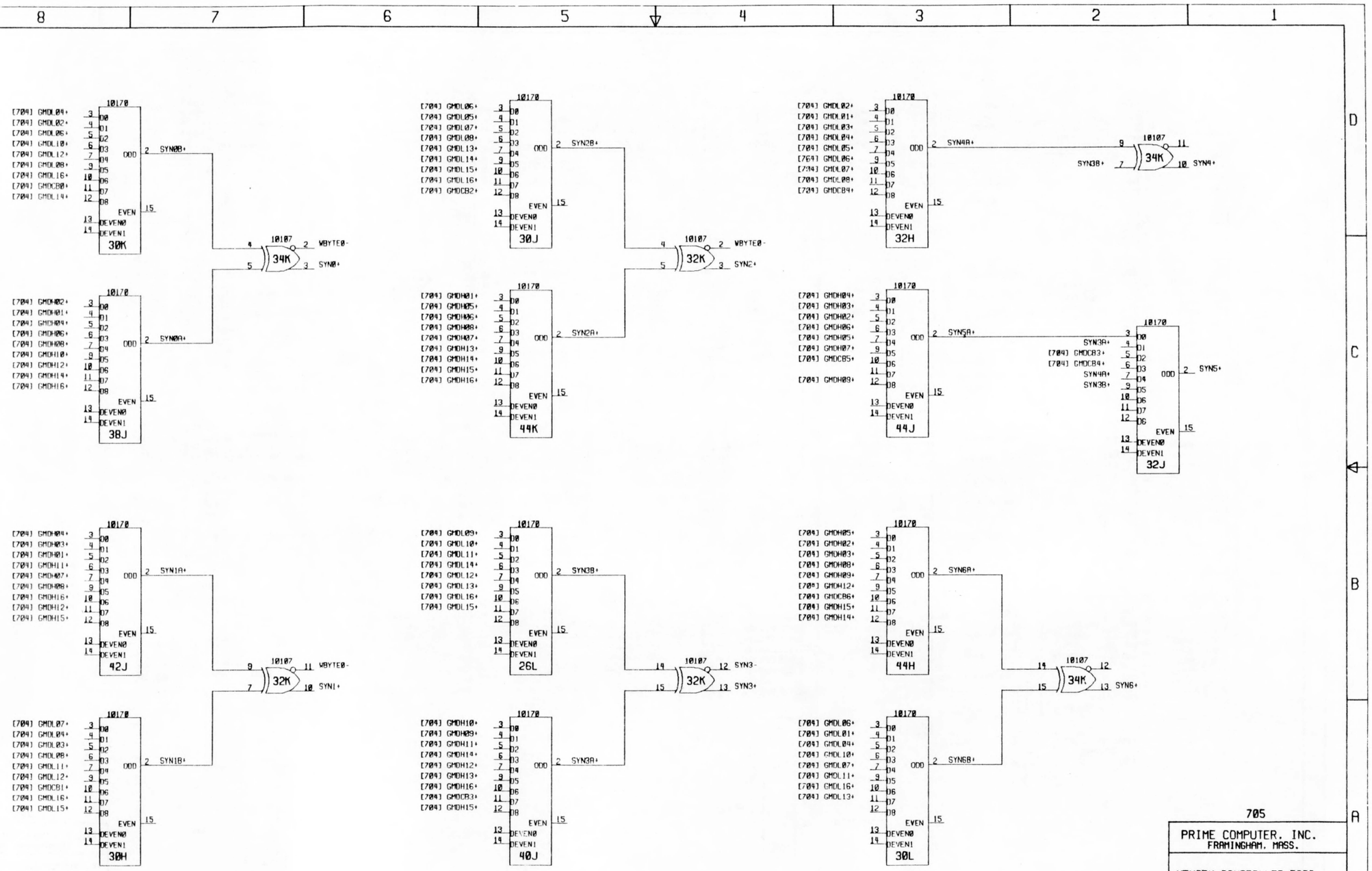
[704] LMDLRP+
[704] LMDL16+
[704] LMDL15+
PBDLRP-
703
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MEMORY CONTROLLER
MEMORY ADDRESS LATCH &
PARITY
SHEET 5 OF 30
SIZE D
DWG. NO LBD5743
REV A2


704
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MEMORY CONTROLLER
MEMORY DATA LATCH & MUX
SHEET 5 OF 30
SIZE D
DWG. NO LBD5743
REV A
32L
36K
36L
28L
36J
42H
40H
38G
08L
16M
08M
14M
34H
32F
30G
16K
24M
32E
44F
26H
SELWMD-A
SELWMD-B
SELWMD-C
[713] TLMDH-
[713] TLMDL-
[713] TLMDP-
[715] MTRCMD+L
[716] MTRCMD+R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[704] GMDCB0+
[704] GMDL14+
10170
ODD
EVEN
DEVEN0
DEVEN1
30K
SYN0B+
10107
34K
WBYTE0-
SYN0+
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[704] GMDH01+
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[704] GMDH16+
38J
SYN0A+
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30J
SYN2B+
32K
WBYTE0-
SYN2+
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SYN3A+
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SYN3B+
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WBYTE0-
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30H
SYN1B+
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SYN3B+
32K
SYN3-
SYN3+
[704] GMDH10+
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[704] GMDCB6+
[704] GMDH15+
[704] GMDH14+
44H
SYN6A+
34K
SYN6+
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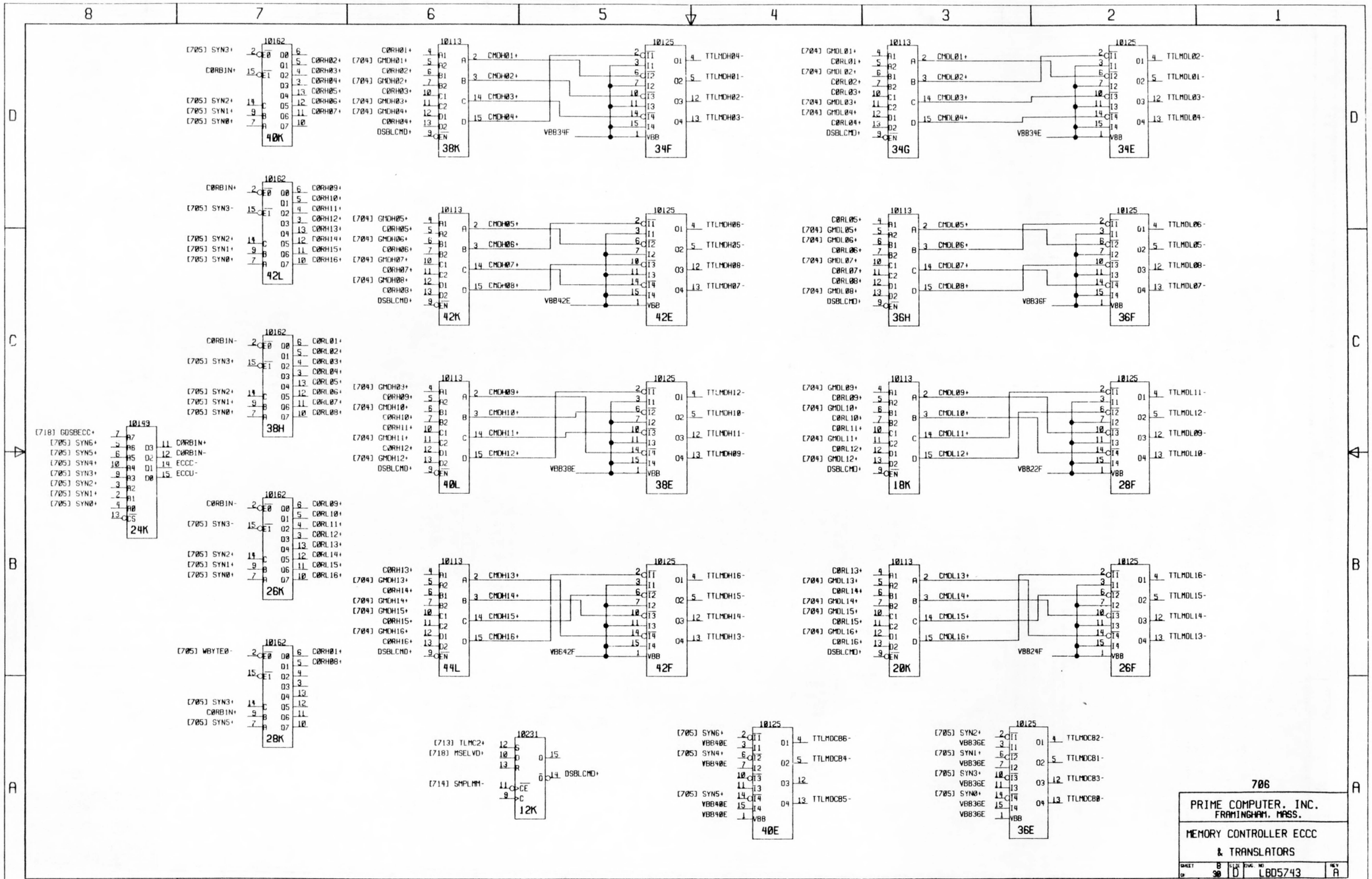
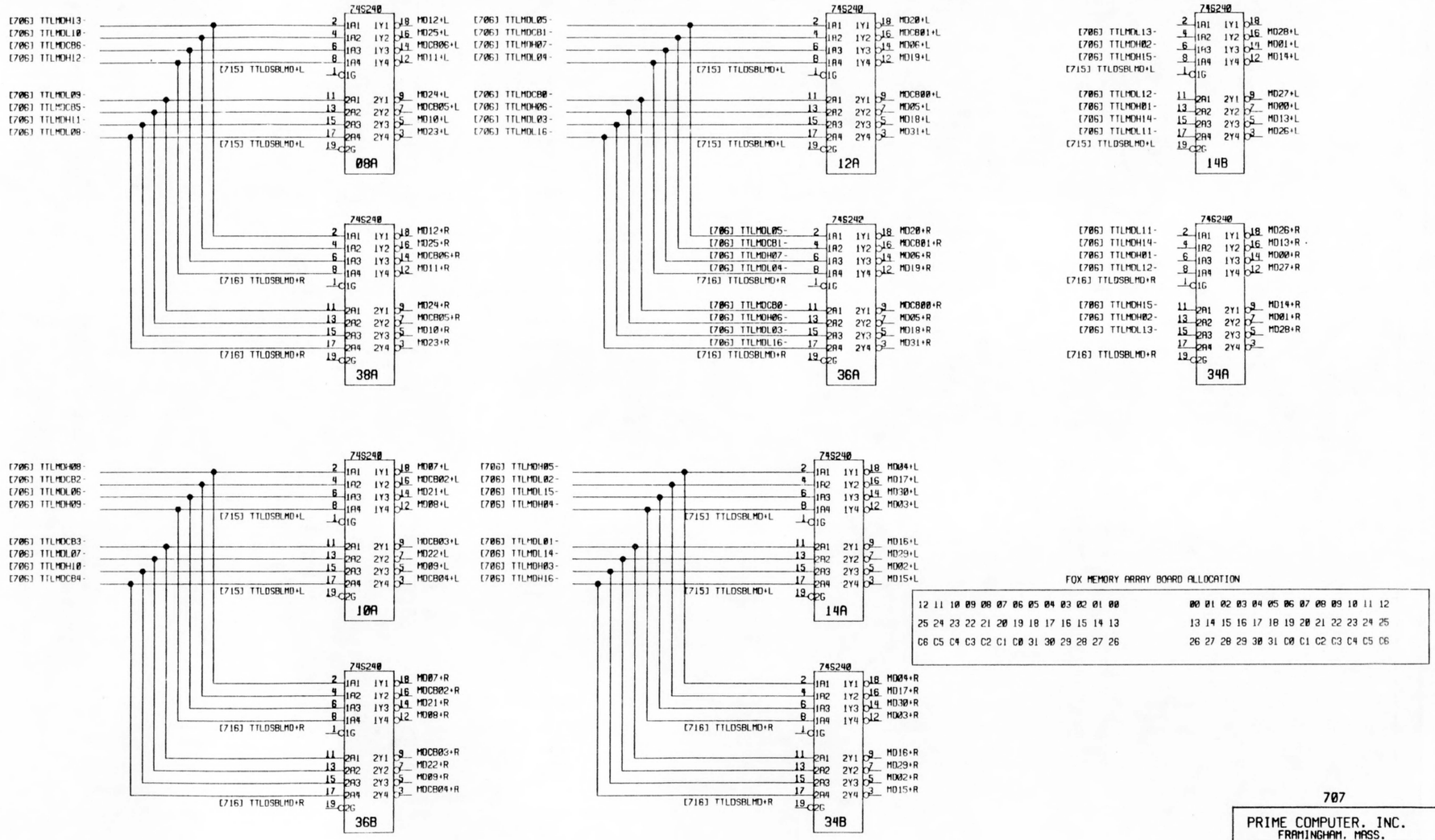
30L
SYN6B+
705
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MEMORY CONTROLLER ECCC
SHEET 7 OF 30
SIZE D
DWG NO LBD5743
REV A


706
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MEMORY CONTROLLER ECCC
& TRANSLATORS
SHEET 30 OF 30
SIZE D
DWG NO LBD5743
REV A



FOX MEMORY ARRAY BOARD ALLOCATION

12 11 10 09 08 07 06 05 04 03 02 01 00	00 01 02 03 04 05 06 07 08 09 10 11 12
25 24 23 22 21 20 19 18 17 16 15 14 13	13 14 15 16 17 18 19 20 21 22 23 24 25
C6 C5 C4 C3 C2 C1 C0 31 30 29 28 27 26	26 27 28 29 30 31 00 C1 C2 C3 C4 C5 C6

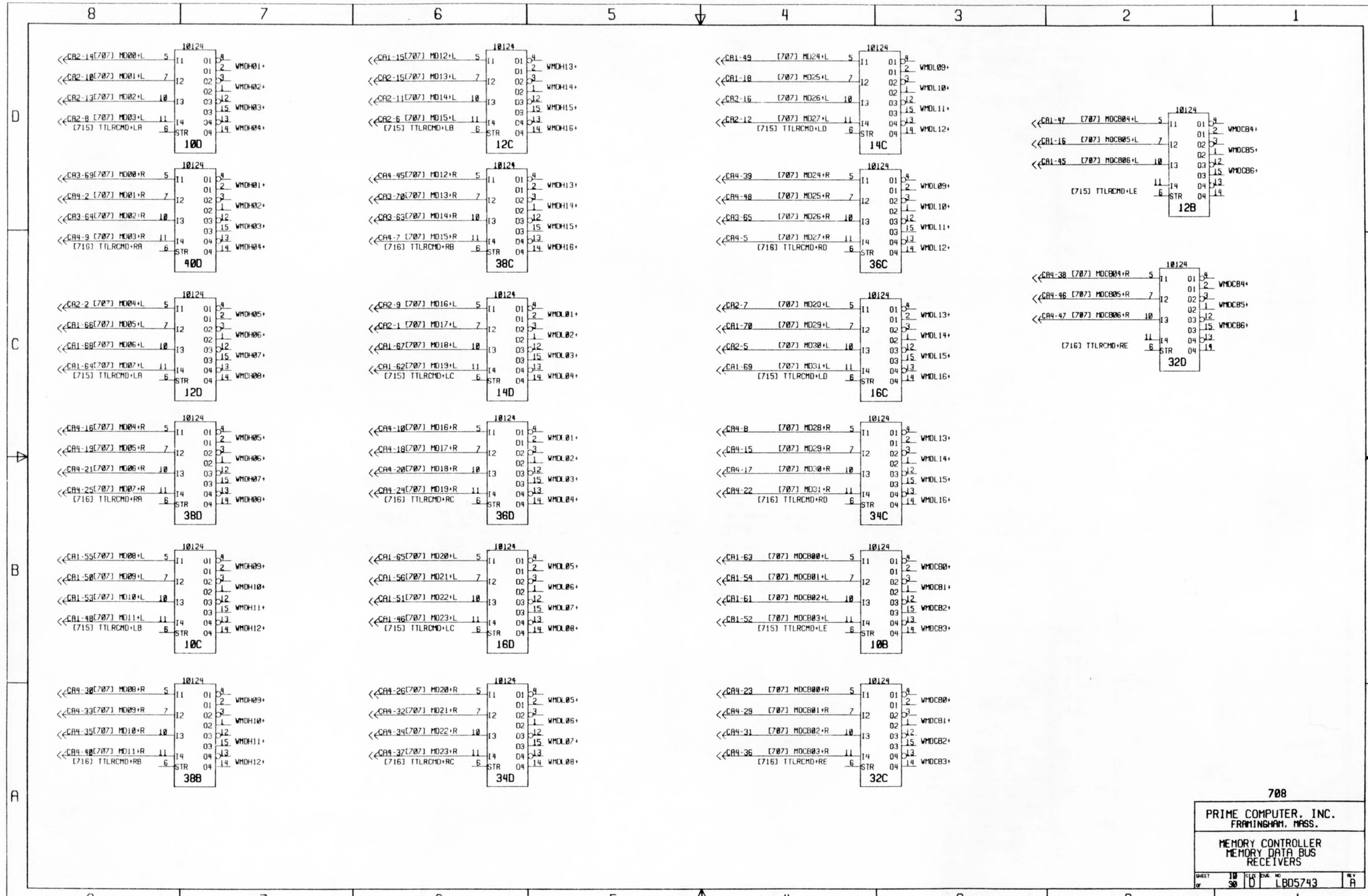
707

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY CONTROLLER

MEMORY DATA BUS DRIVERS

SHEET 9 OF 30 | SIZE D | DWG NO LBD5743 | REV A

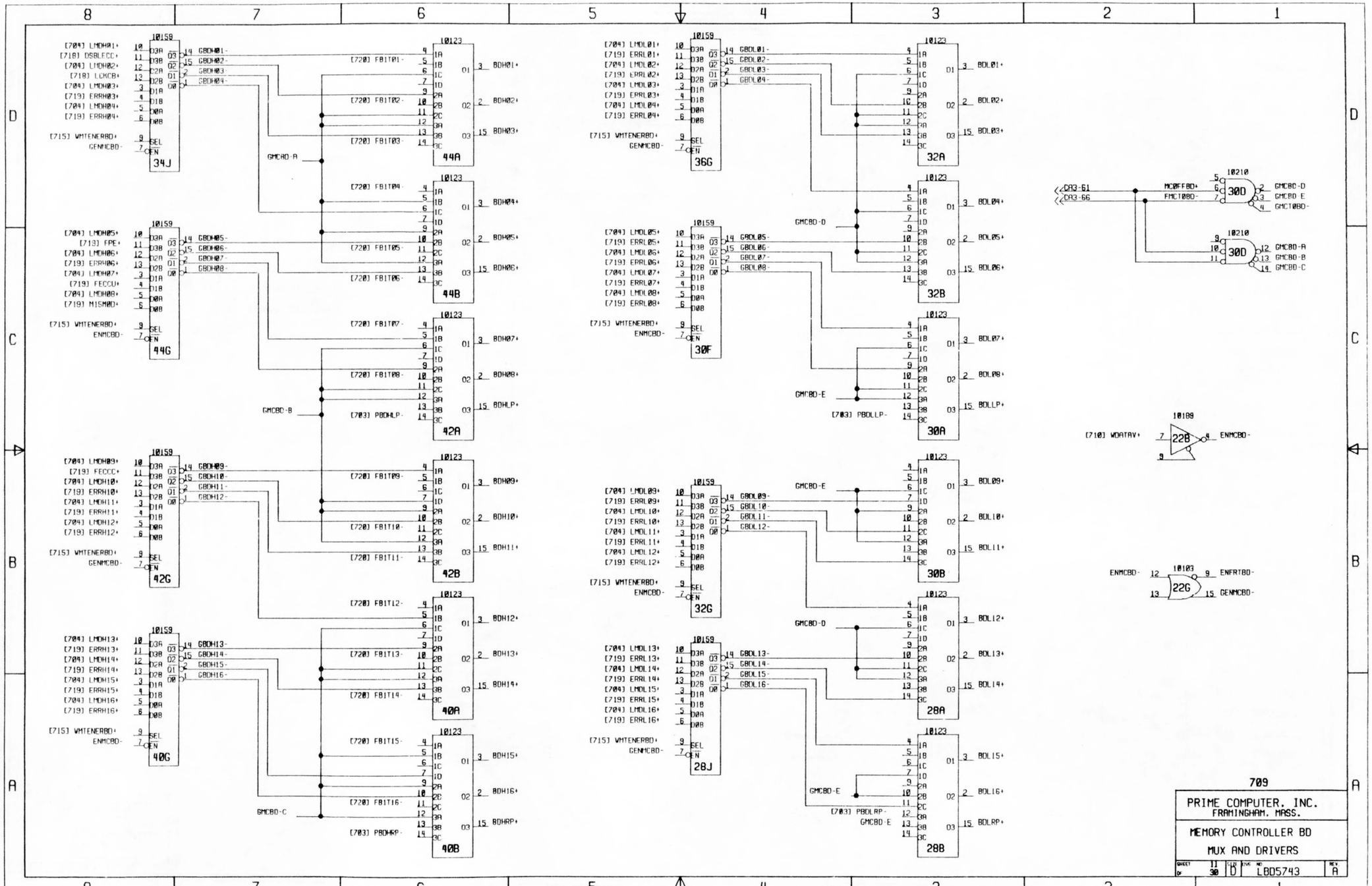


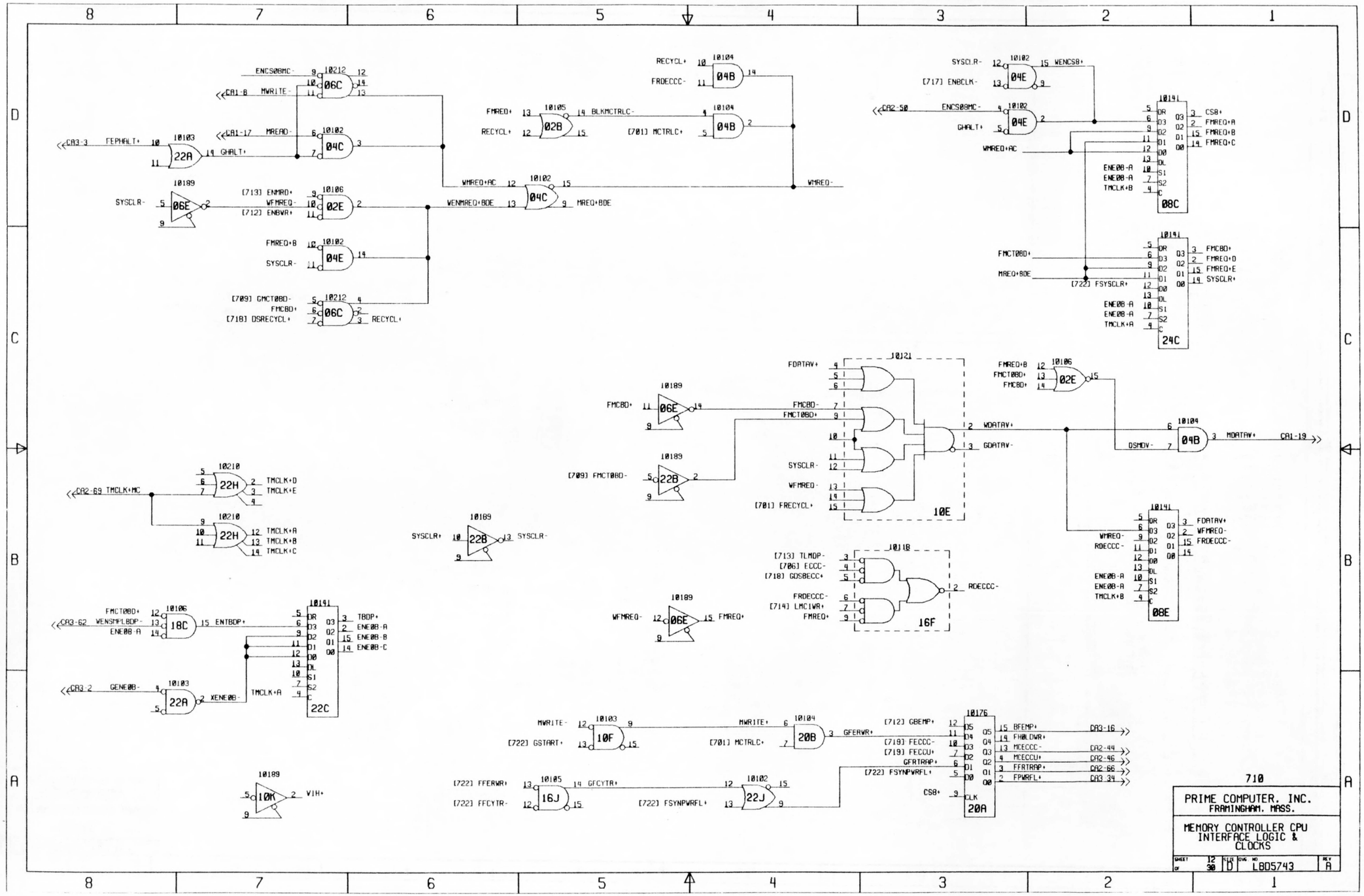
708

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY CONTROLLER
MEMORY DATA BUS
RECEIVERS

SHEET 10 OF 30 | SIZE D | DWG NO LBD5743 | REV A


34J
44A
44B
44G
42A
42B
42G
40A
40B
40G
36G
32A
32B
30F
30A
30B
32G
28A
28B
28J
30D
30D
22B
22G
GMCBD-A
GMCBD-B
GMCBD-C
GMCBD-D
GMCBD-E
709
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MEMORY CONTROLLER BD
MUX AND DRIVERS
LBD5743
A

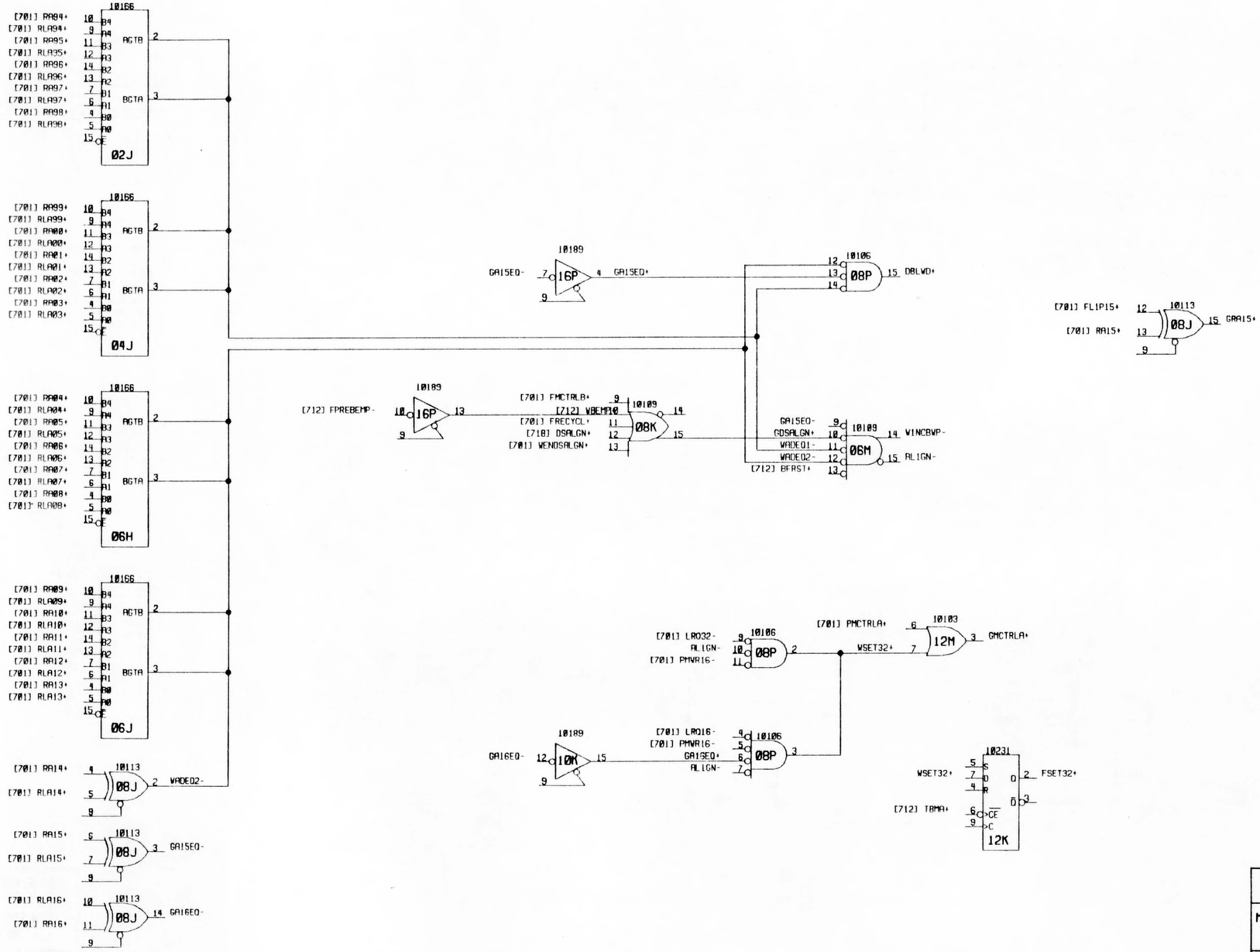


710

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY CONTROLLER CPU INTERFACE LOGIC & CLOCKS

SHEET	OF	SIZE	DWG NO	REV
12	30	D	LBD5743	A

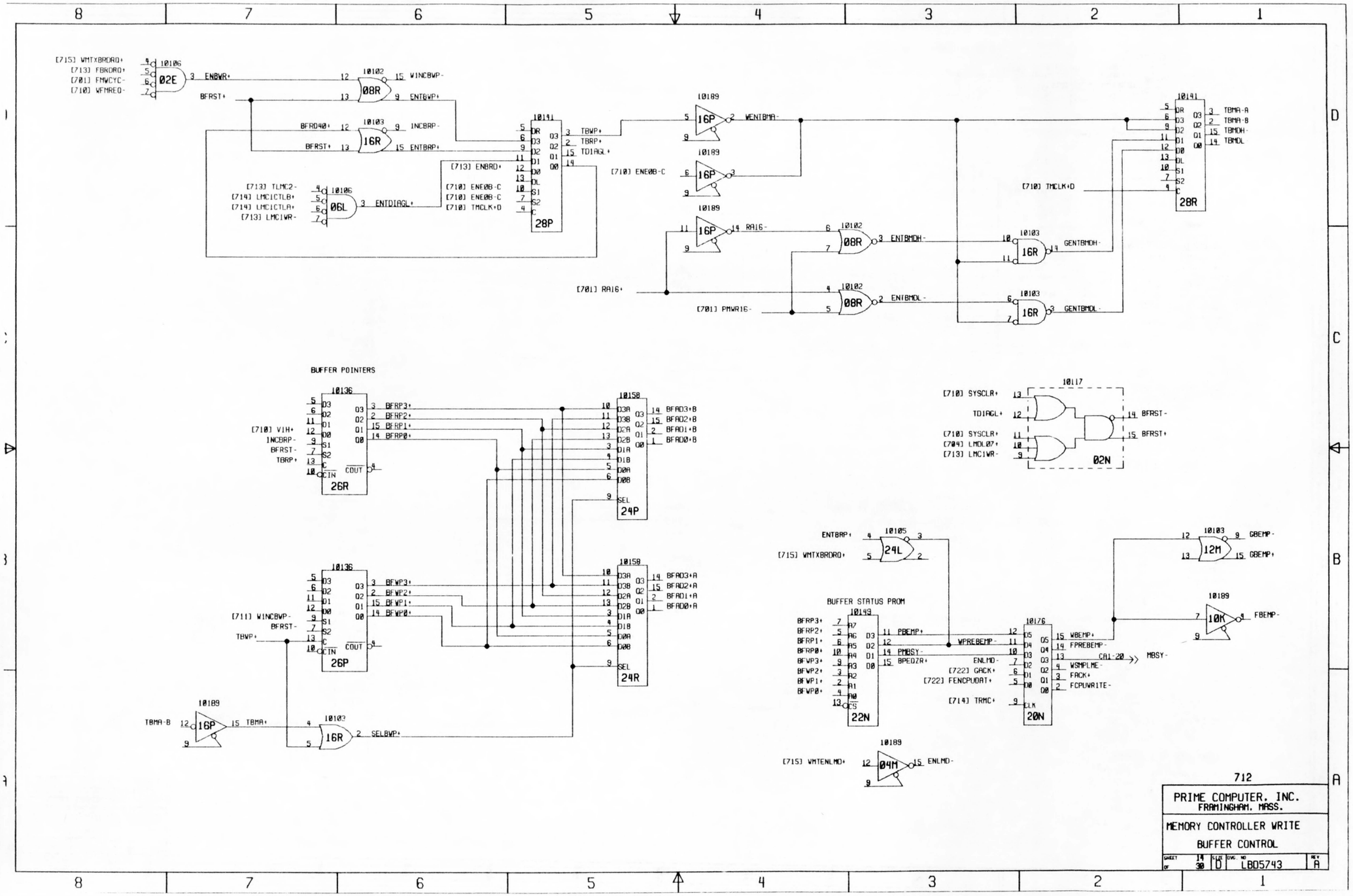


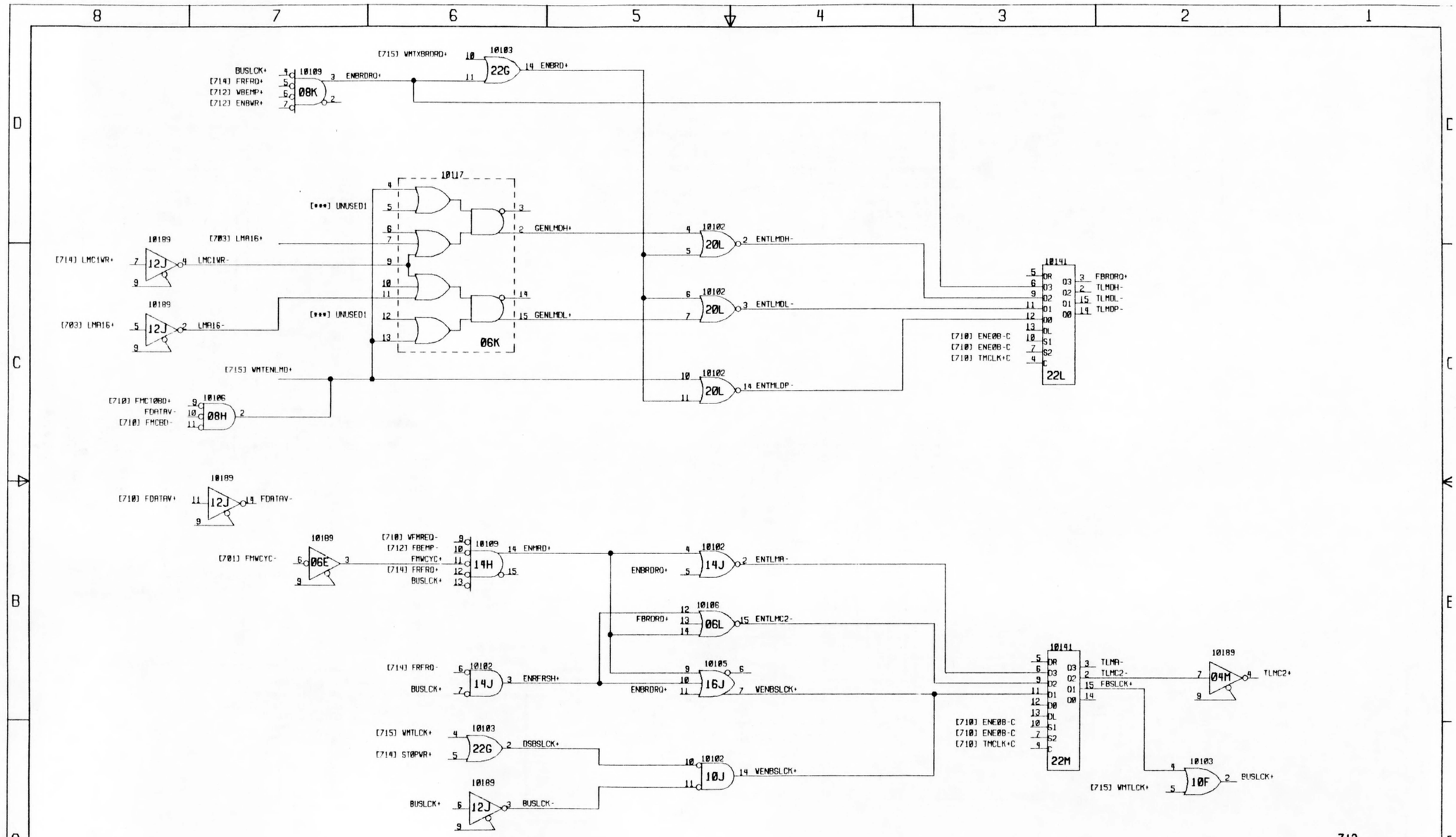
711

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY CONTROLLER ALIGN LOGIC

SHEET OF	SIZE	DWG. NO	REV
13 30	D	LBD5743	A


[715] WMTXBRDRQ+
[713] FBRDRQ+
[701] FMWCYC-
[710] WFMREQ-
ENBWR+
BFRST+
BFRD40+
BFRST+
INCBRP-
ENTBRP+
WINCBWP-
ENTGWP+
[713] ENBRD+
[710] ENE0B-C
[710] ENE0B-C
[710] TMCLK+D
TBWP+
TBRP+
TDIAGL+
[713] TLMC2-
[714] LMCICTLB+
[714] LMCICTLA+
[713] LMCIWR-
ENTDIAGL+
[710] ENE0B-C
WENTBMA-
[710] TMCLK+D
TBMA-A
TBMA-B
TBMDH-
TBMDL
[701] RA16+
[701] PMWR16-
RA16-
ENTBMDH-
ENTBMDL-
GENTBMDH-
GENTBMDL-
BUFFER POINTERS
[710] VIH+
INCBRP-
BFRST-
TBRP+
BFRP3+
BFRP2+
BFRP1+
BFRP0+
BFAD3+B
BFAD2+B
BFAD1+B
BFAD0+B
[711] WINCBWP-
BFRST-
TBWP+
BFWP3+
BFWP2+
BFWP1+
BFWP0+
BFAD3+A
BFAD2+A
BFAD1+A
BFAD0+A
TBMA-B
TBMA+
SELBWP+
[710] SYSCLR+
TDIAGL+
[710] SYSCLR+
[704] LMDL07+
[713] LMCIWR-
BFRST-
BFRST+
ENTBRP+
[715] WMTXBRDRQ+
BUFFER STATUS PROM
BFRP3+
BFRP2+
BFRP1+
BFRP0+
BFWP3+
BFWP2+
BFWP1+
BFWP0+
PBEMP+
WPREBEMP-
PMBSY-
BPEOZR+
ENLMD-
[722] GACK+
[722] FENCPUDAT+
[714] TRMC+
WBEMP+
FPREBEMP-
CA1-20
MBSY-
WSMPLME-
FACK+
FCPUWRITE-
GBEMP-
GBEMP+
FBEMP-
[715] WMTENLMD+
ENLMD-
10102
10103
10105
10106
10108
10117
10136
10141
10149
10158
10176
10189
02E
08R
16R
06L
28P
26R
26P
24P
24R
02N
24L
22N
12M
10K
04M
20N
28R
712
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MEMORY CONTROLLER WRITE
BUFFER CONTROL
SHEET 14 OF 30
SIZE D
DWG NO LBD5743
REV A

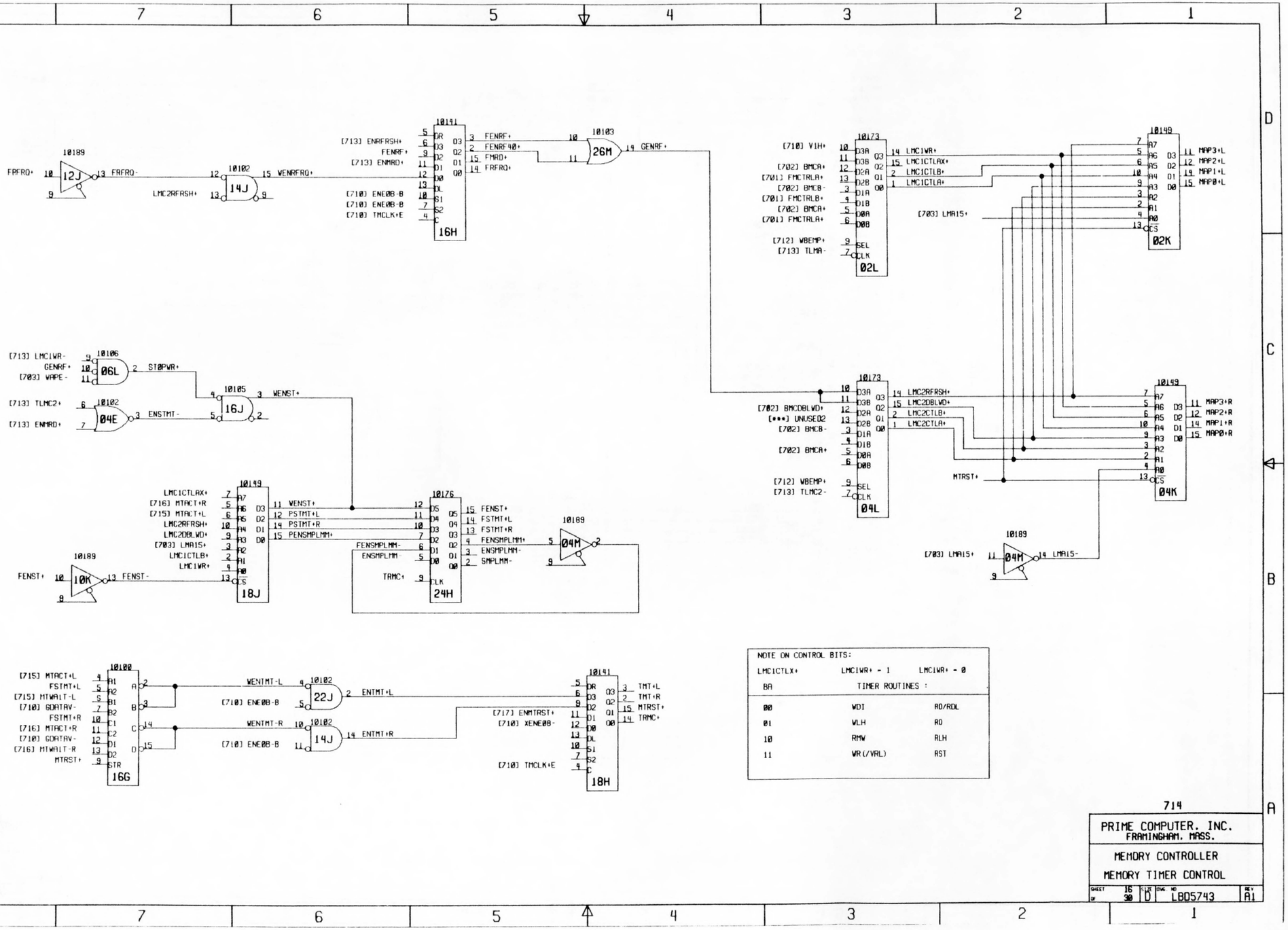


713

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY CONTROLLER LATCH CONTROL

SHEET 15 OF 30 | SIZ D | DWG NO LBD5743 | REV A



NOTE ON CONTROL BITS:

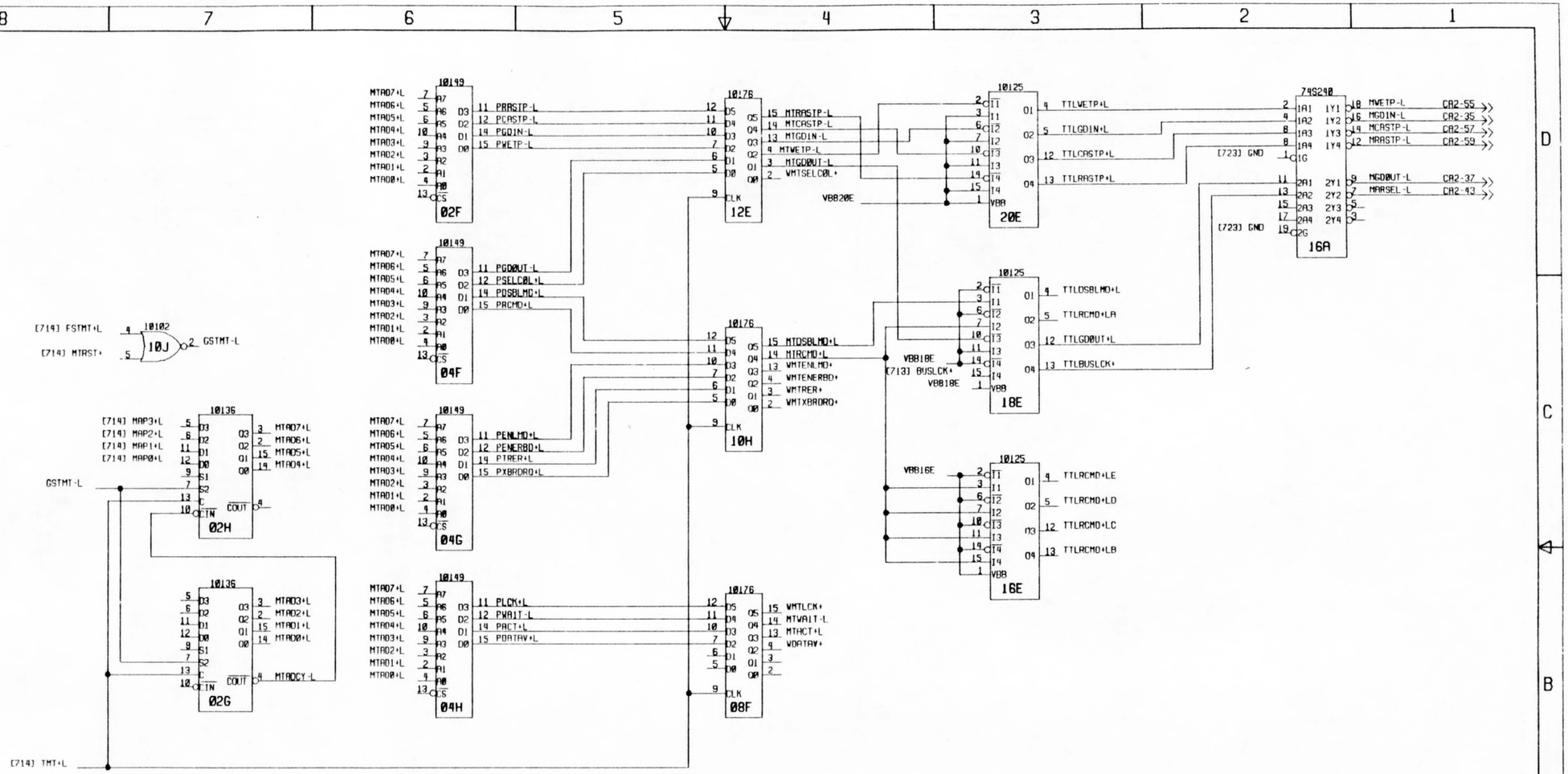
LMC1CTLX+ BA	LMC1WR+ = 1 TIMER ROUTINES :	LMC1WR+ = 0
00	WDI	RD/RDL
01	WLH	RD
10	RMW	RLH
11	WR(/VRL)	RST

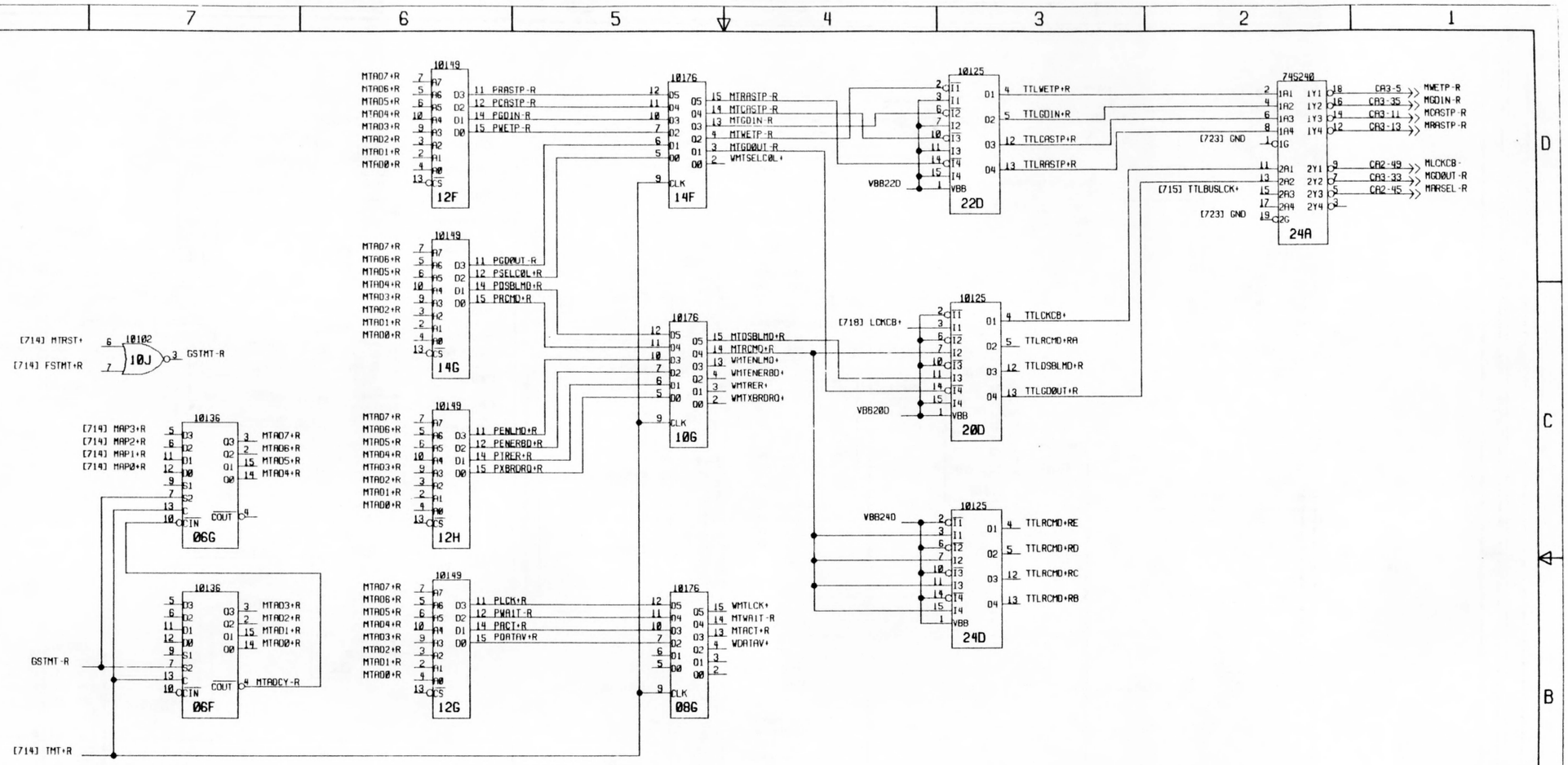
714

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY CONTROLLER
MEMORY TIMER CONTROL

SHEET 16 OF 30 | SIZE D | DWG NO LBD5743 | REV A1


10J
02F
12E
20E
16A
04F
10H
18E
04G
16E
02H
02G
04H
08F
715
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MEMORY CONTROLLER LEFT
MEMORY TIMER
LBD5743

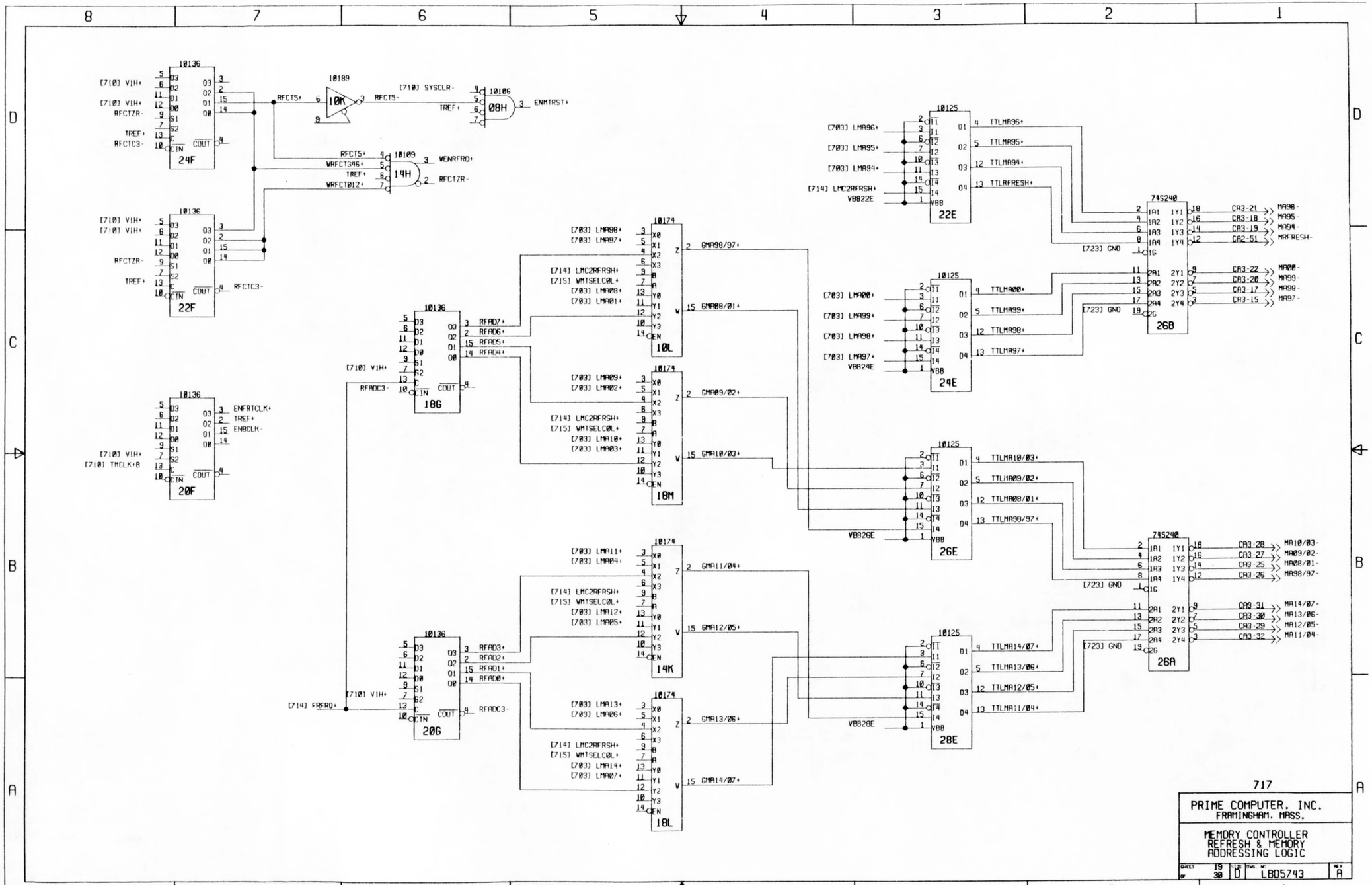


716

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY CONTROLLER RIGHT
MEMORY TIMER

SHEET 18 OF 30 | SIZE D | DWG NO LBD5743 | REV A

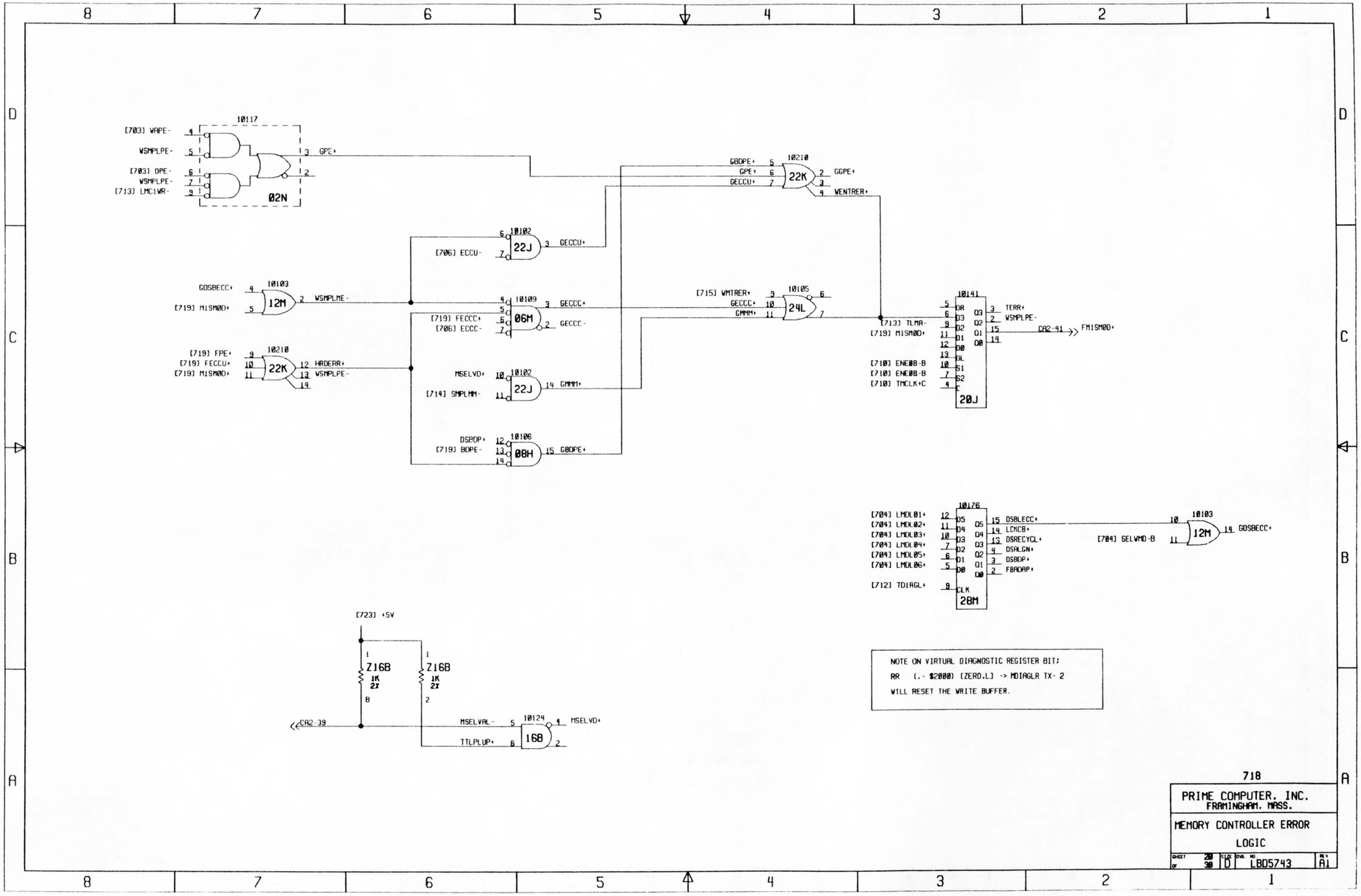


717

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY CONTROLLER
REFRESH & MEMORY
ADDRESSING LOGIC

SHEET 19 OF 30 | SIZE D | DWG NO LBD5743 | REV A



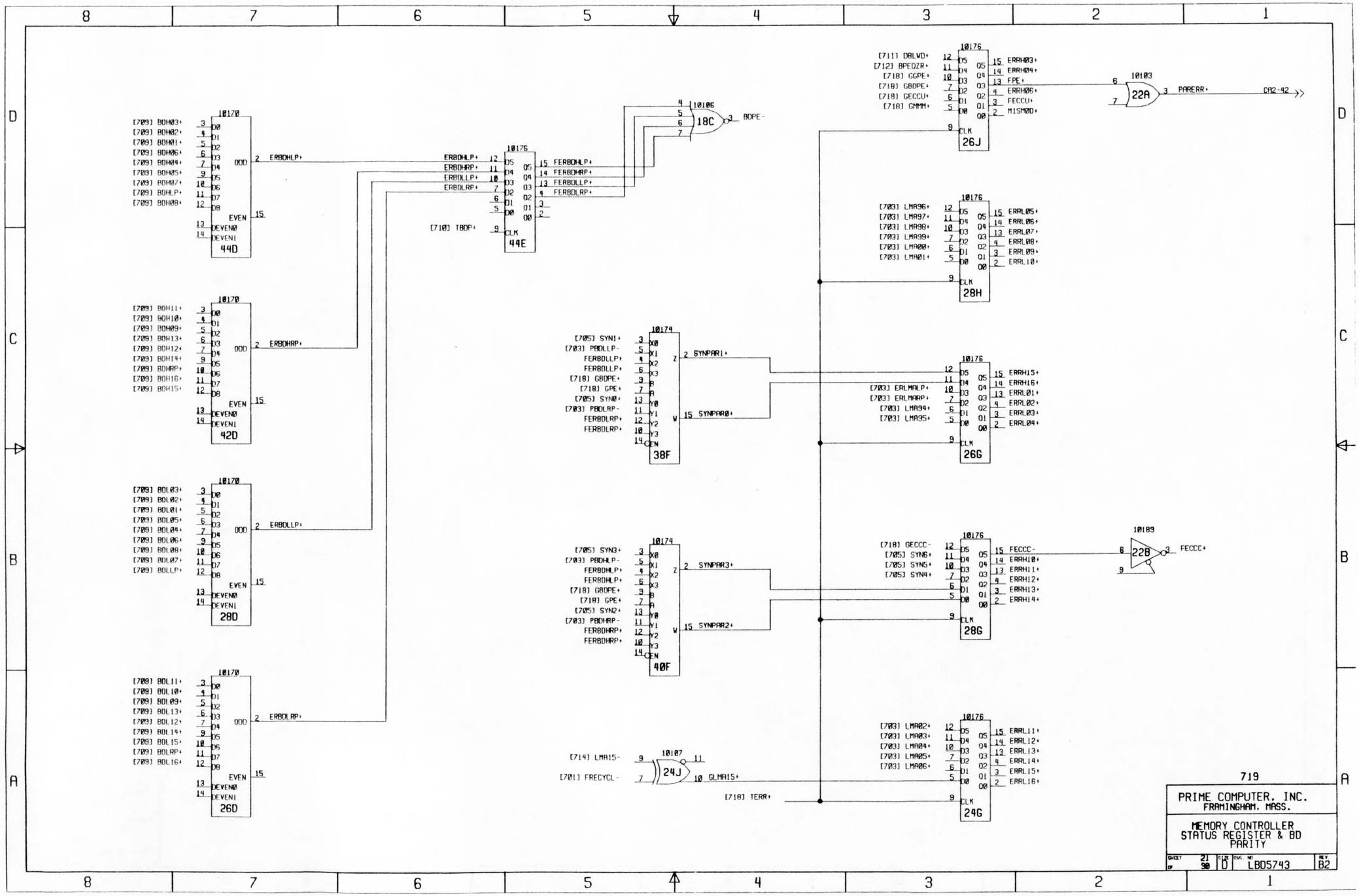
NOTE ON VIRTUAL DIAGNOSTIC REGISTER BIT:
RR (,- $2000) [ZERO.L] -> MDIAGLR TX- 2
WILL RESET THE WRITE BUFFER.

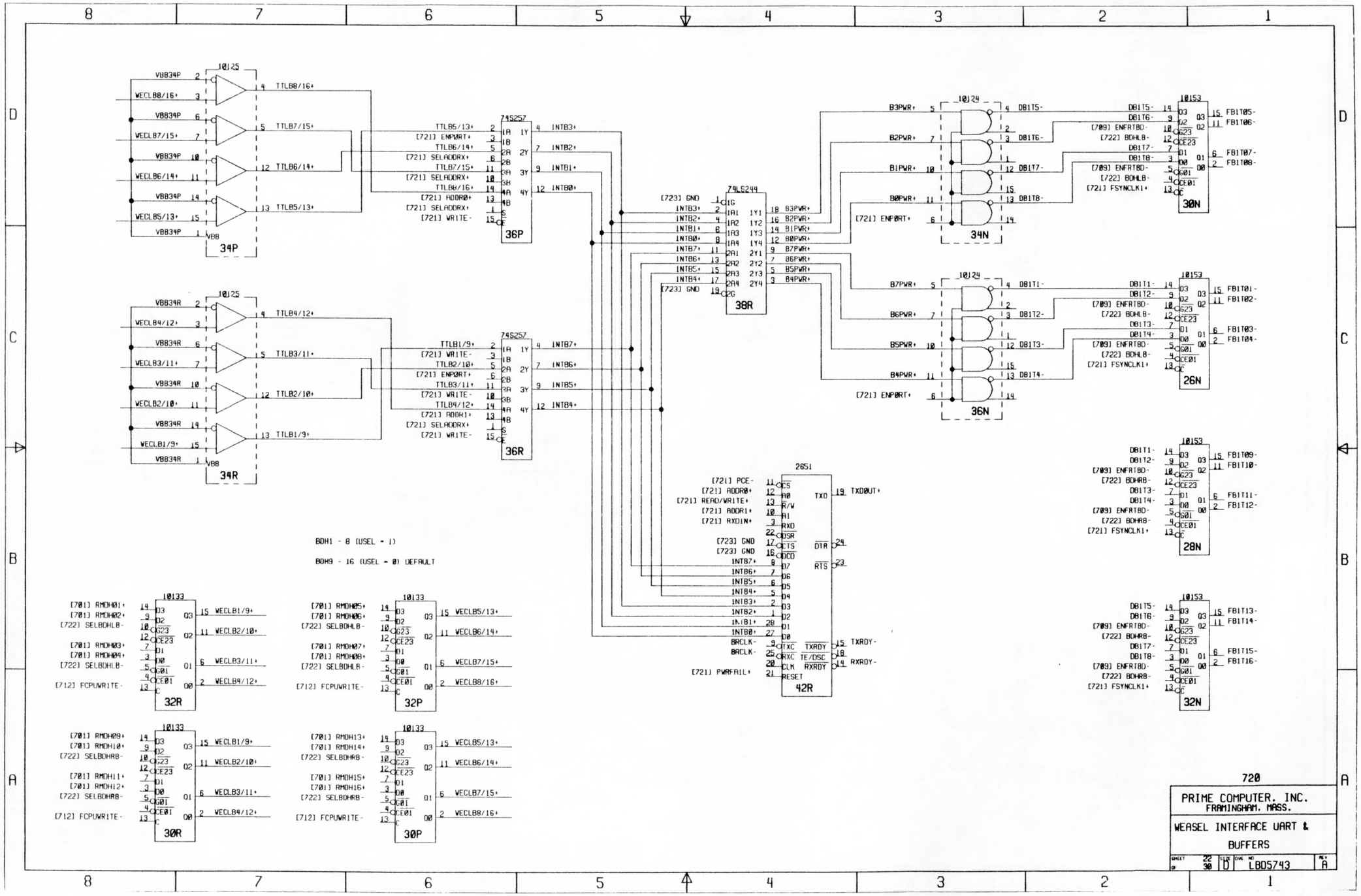
718

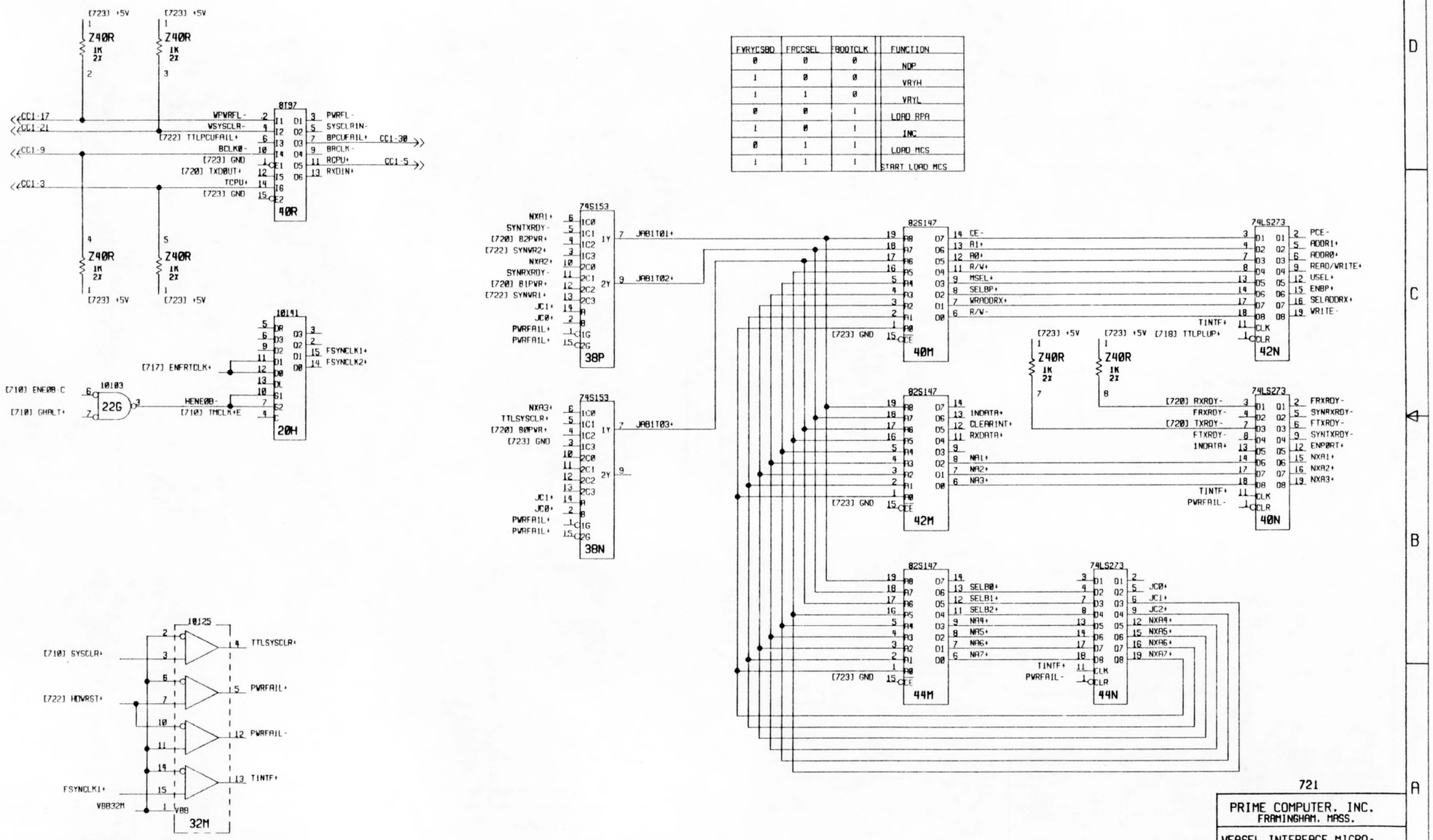
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY CONTROLLER ERROR LOGIC

SHEET 29 OF 30 | SIZE D | DWG NO LBD5743 | REV A1


719
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MEMORY CONTROLLER
STATUS REGISTER & BD
PARITY
SHEET 21 OF 90
SIZE D
DWG NO LBD5743
REV B2
44D
44E
42D
28D
26D
18C
22A
26J
28H
26G
38F
28G
40F
24G
24J
22B


10125
VBB34P
WECLB8/16+
VBB34P
WECLB7/15+
VBB34P
WECLB6/14+
VBB34P
WECLB5/13+
VBB34P
VBB
TTLB8/16+
TTLB7/15+
TTLB6/14+
TTLB5/13+
34P
74S257
TTLB5/13+
[721] ENP0RT+
TTLB6/14+
[721] SELADDRX+
TTLB7/15+
[721] SELADDRX+
TTLB8/16+
[721] ADDR0+
[721] SELADDRX+
[721] WRITE-
1A 1B 2A 2B 3A 3B 4A 4B 1Y 2Y 3Y 4Y S E
INTB3+
INTB2+
INTB1+
INTB0+
36P
10125
VBB34R
WECLB4/12+
VBB34R
WECLB3/11+
VBB34R
WECLB2/10+
VBB34R
WECLB1/9+
VBB34R
VBB
TTLB4/12+
TTLB3/11+
TTLB2/10+
TTLB1/9+
34R
74S257
TTLB1/9+
[721] WRITE-
TTLB2/10+
[721] ENP0RT+
TTLB3/11+
[721] WRITE-
TTLB4/12+
[721] ADDR1+
[721] SELADDRX+
[721] WRITE-
1A 1B 2A 2B 3A 3B 4A 4B 1Y 2Y 3Y 4Y S E
INTB7+
INTB6+
INTB5+
INTB4+
36R
74LS244
[723] GND
INTB3+
INTB2+
INTB1+
INTB0+
INTB7+
INTB6+
INTB5+
INTB4+
[723] GND
1G 2G 1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4 1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4
B3PWR+
B2PWR+
B1PWR+
B0PWR+
B7PWR+
B6PWR+
B5PWR+
B4PWR+
38R
10124
B3PWR+
B2PWR+
B1PWR+
B0PWR+
[721] ENP0RT+
DB1T5-
DB1T6-
DB1T7-
DB1T8-
34N
10153
DB1T5-
DB1T6-
[709] ENFRTBD-
[722] BDHLB-
DB1T7-
DB1T8-
[709] ENFRTBD-
[722] BDHLB-
[721] FSYNCLK1+
G23 CE23 D1 D0 G01 CE01 C
FB1T05-
FB1T06-
FB1T07-
FB1T08-
30N
10124
B7PWR+
B6PWR+
B5PWR+
B4PWR+
[721] ENP0RT+
DB1T1-
DB1T2-
DB1T3-
DB1T4-
36N
10153
DB1T1-
DB1T2-
[709] ENFRTBD-
[722] BDHLB-
DB1T3-
DB1T4-
[709] ENFRTBD-
[722] BDHLB-
[721] FSYNCLK1+
G23 CE23 D1 D0 G01 CE01 C
FB1T01-
FB1T02-
FB1T03-
FB1T04-
26N
10153
DB1T1-
DB1T2-
[709] ENFRTBD-
[722] BDHRB-
DB1T3-
DB1T4-
[709] ENFRTBD-
[722] BDHRB-
[721] FSYNCLK1+
G23 CE23 D1 D0 G01 CE01 C
FB1T09-
FB1T10-
FB1T11-
FB1T12-
28N
10153
DB1T5-
DB1T6-
[709] ENFRTBD-
[722] BDHRB-
DB1T7-
DB1T8-
[709] ENFRTBD-
[722] BDHRB-
[721] FSYNCLK1+
G23 CE23 D1 D0 G01 CE01 C
FB1T13-
FB1T14-
FB1T15-
FB1T16-
32N
2651
[721] PCE-
[721] ADDR0+
[721] READ/WRITE+
[721] ADDR1+
[721] RXDIN+
[723] GND
[723] GND
INTB7+
INTB6+
INTB5+
INTB4+
INTB3+
INTB2+
INTB1+
INTB0+
BRCLK-
BRCLK-
[721] PWRFAIL+
CS A0 R/W A1 RXD DSR CTS DCD D7 D6 D5 D4 D3 D2 D1 D0 TXC RXC CLK RESET TXD DTR RTS TXRDY TE/DSC RXRDY
TXD0UT+
TXRDY-
RXRDY-
42R
BDH1 - 8 (USEL - 1)
BDH9 - 16 (USEL - 0) DEFAULT
10133
[701] RMDH01+
[701] RMDH02+
[722] SELBDHLB-
[701] RMDH03+
[701] RMDH04+
[722] SELBDHLB-
[712] FCPUWRITE-
VECLB1/9+
VECLB2/10+
VECLB3/11+
VECLB4/12+
32R
10133
[701] RMDH05+
[701] RMDH06+
[722] SELBDHLB-
[701] RMDH07+
[701] RMDH08+
[722] SELBDHLB-
[712] FCPUWRITE-
VECLB5/13+
VECLB6/14+
VECLB7/15+
VECLB8/16+
32P
10133
[701] RMDH09+
[701] RMDH10+
[722] SELBDHRB-
[701] RMDH11+
[701] RMDH12+
[722] SELBDHRB-
[712] FCPUWRITE-
VECLB1/9+
VECLB2/10+
VECLB3/11+
VECLB4/12+
30R
10133
[701] RMDH13+
[701] RMDH14+
[722] SELBDHRB-
[701] RMDH15+
[701] RMDH16+
[722] SELBDHRB-
[712] FCPUWRITE-
VECLB5/13+
VECLB6/14+
VECLB7/15+
VECLB8/16+
30P
720
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
WEASEL INTERFACE UART & BUFFERS
SHEET 22 OF 30
SIZE D
DWG NO LBD5743
REV A



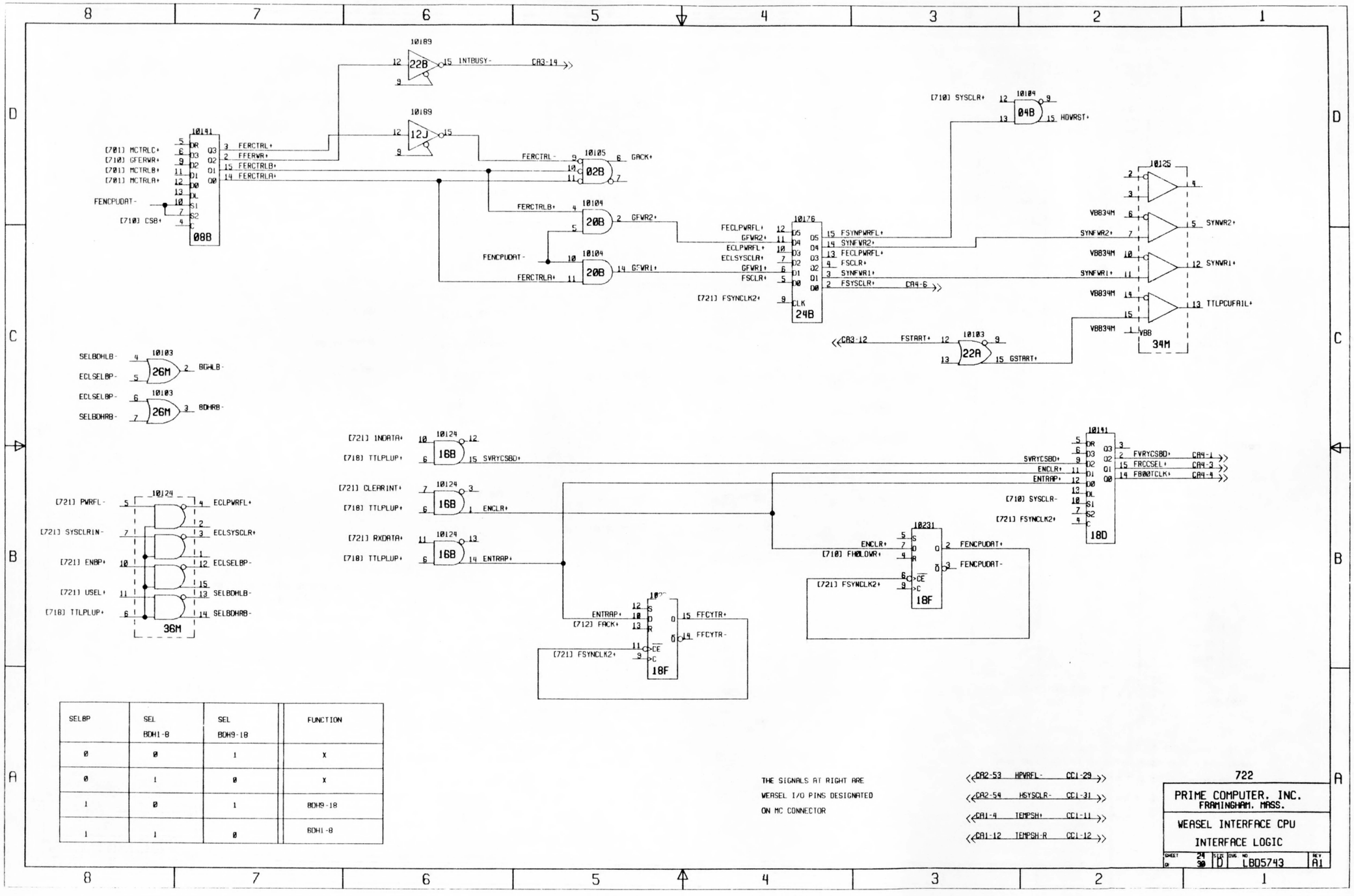
FVRYCSB0	FRCCSEL	FB0OTCLK	FUNCTION
0	0	0	NOP
1	0	0	VRYH
1	1	0	VRYL
0	0	1	LOAD RPA
1	0	1	INC
0	1	1	LOAD MCS
1	1	1	START LOAD MCS

721

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

WEASEL INTERFACE MICRO-SEQUENCER & CLOCKS

SHEET 23 OF 30 | SIZE D | DWG NO LBD5743 | REV A



SELBP	SEL BDH1-8	SEL BDH9-18	FUNCTION
0	0	1	X
0	1	0	X
1	0	1	BDH9-18
1	1	0	BDH1-8

THE SIGNALS AT RIGHT ARE WEASEL I/O PINS DESIGNATED ON MC CONNECTOR

CA2-53 HPVRFL- CC1-29
CA2-54 HSYSCLR- CC1-31
CA1-4 TEMPSH+ CC1-11
CA1-12 TEMPSH-R CC1-12

722

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

WEASEL INTERFACE CPU
INTERFACE LOGIC

SHEET 24 OF 30 | SIZE D | DWG NO LBD5743 | REV A1

X-REF TABLE

SIGNAL NAME	DIAG. PROC. PIN #	CPU PIN #
[5]GND	01	33
[5]GND	02	34
HSYSCLR-	03	31
	04	*
HPWRFL-	05	29
BPCCUFAIL+	06	30
[9]CNTRL2+	07	*
[5]GND	08	28
[5]GND	09	25
[9]BCLCPUART-	10	*
	11	*
	12	*
[5]VSYSCLR-	13	21
[5]GND	14	22
	15	*
[5]GND	16	20
[5]WPWRFL-	17	17
	18	*
	19	*
	20	*
	21	*
	22	*
TEMPSH+	23	11
[9]TEMPSH-R	24	12
[7]BCLK0	25	09
[5]GND	26	10
	27	*
[5]GND	28	08
RCPU	29	05
[5]GND	30	06
[7]TCPU	31	03
[5]GND	32	04
[5]GND	33	01
[5]GND	34	02

NOTE : * MEANS DON'T CARE

THE TABLE ABOVE EQUATES THE DIAGNOSTIC PROCESSOR CONNECTOR PINS WITH THE MC BOARD CONNECTOR PINS FOR THIS CABLE. THE BOARD CONNECTOR ENDS DIFFER IN PIN DESIGNATION.

CA1-1 >>+5VA
CA1-2 >>+5VA
CA1-13 >>GND
CA1-14 >>GND
CA1-27 >>-5.2V
CA1-28 >>-5.2V
CA1-29 >>-5.2V
CA1-30 >>-5.2V
CA1-43 >>-2V
CA1-44 >>-2V
CA1-57 >>GND
CA1-58 >>GND
CA1-59 >>GND
CA1-60 >>GND

CA2-3 >>GND
CA2-4 >>GND
CA2-17 >>-5.2V
CA2-18 >>-5.2V
CA2-19 >>-5.2V
CA2-20 >>-5.2V
CA2-33 >>-2V
CA2-34 >>-2V
CA2-47 >>GND
CA2-48 >>GND
CA2-61 >>GND
CA2-62 >>GND
CA2-63 >>GND
CA2-64 >>GND
CA2-67 >>GND
CA2-70 >>GND

CA3-1 >>GND
CA3-7 >>GND
CA3-8 >>GND
CA3-9 >>GND
CA3-10 >>GND
CA3-23 >>GND
CA3-24 >>GND
CA3-37 >>-2V
CA3-38 >>-2V
CA3-51 >>-5.2V
CA3-52 >>-5.2V
CA3-53 >>-5.2V
CA3-54 >>-5.2V
CA3-67 >>GND
CA3-68 >>GND

CA4-11 >>GND
CA4-12 >>GND
CA4-13 >>GND
CA4-14 >>GND
CA4-27 >>-2V
CA4-28 >>-2V
CA4-41 >>-5.2V
CA4-42 >>-5.2V
CA4-43 >>-5.2V
CA4-44 >>-5.2V
CA4-57 >>GND
CA4-58 >>GND
CA4-69 >>+5V
CA4-70 >>+5V

CC1-1 >>GND
CC1-2 >>GND
CC1-4 >>GND
CC1-6 >>GND
CC1-8 >>GND
CC1-10 >>GND
CC1-20 >>GND
CC1-22 >>GND
CC1-25 >>GND
CC1-28 >>GND
CC1-33 >>GND
CC1-34 >>GND

C500
22
15V.10%
+5VA 1 2 GND

C501
22
15V.10%
GND 1 2 [***] -2V

C502
22
15V.10%
GND 1 2 -5.2V

C503
22
15V.10%
GND 1 2 [***] -2V

C504
22
15V.10%
GND 1 2 -5.2V

C505
22
15V.10%
+5V 1 2 GND

NOTE :

1. .01 UF AXIAL LEAD CAPACITORS ARE NOT SHOWN BUT ARE INSTALLED ABOVE THE DIPS IN THE FOLLOWING COLUMNS : A.C.E.G.J.L.N.P AND WHEREVER NECESSARY

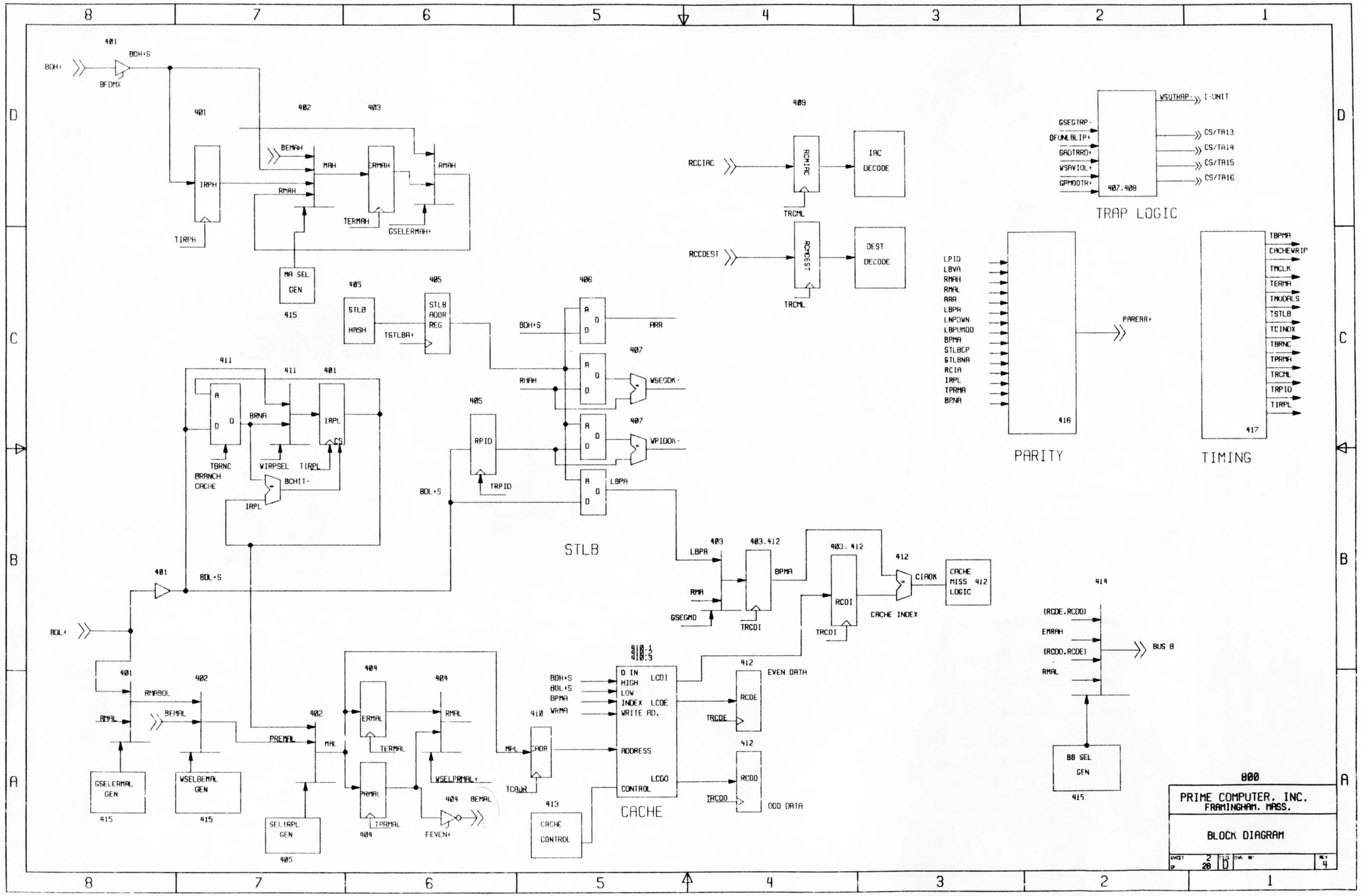
2. UNLESS OTHERWISE SPECIFIED :
RESISTANCE VALUES ARE IN OHMS
CAPACITANCE VALUES ARE IN MICROFARADS

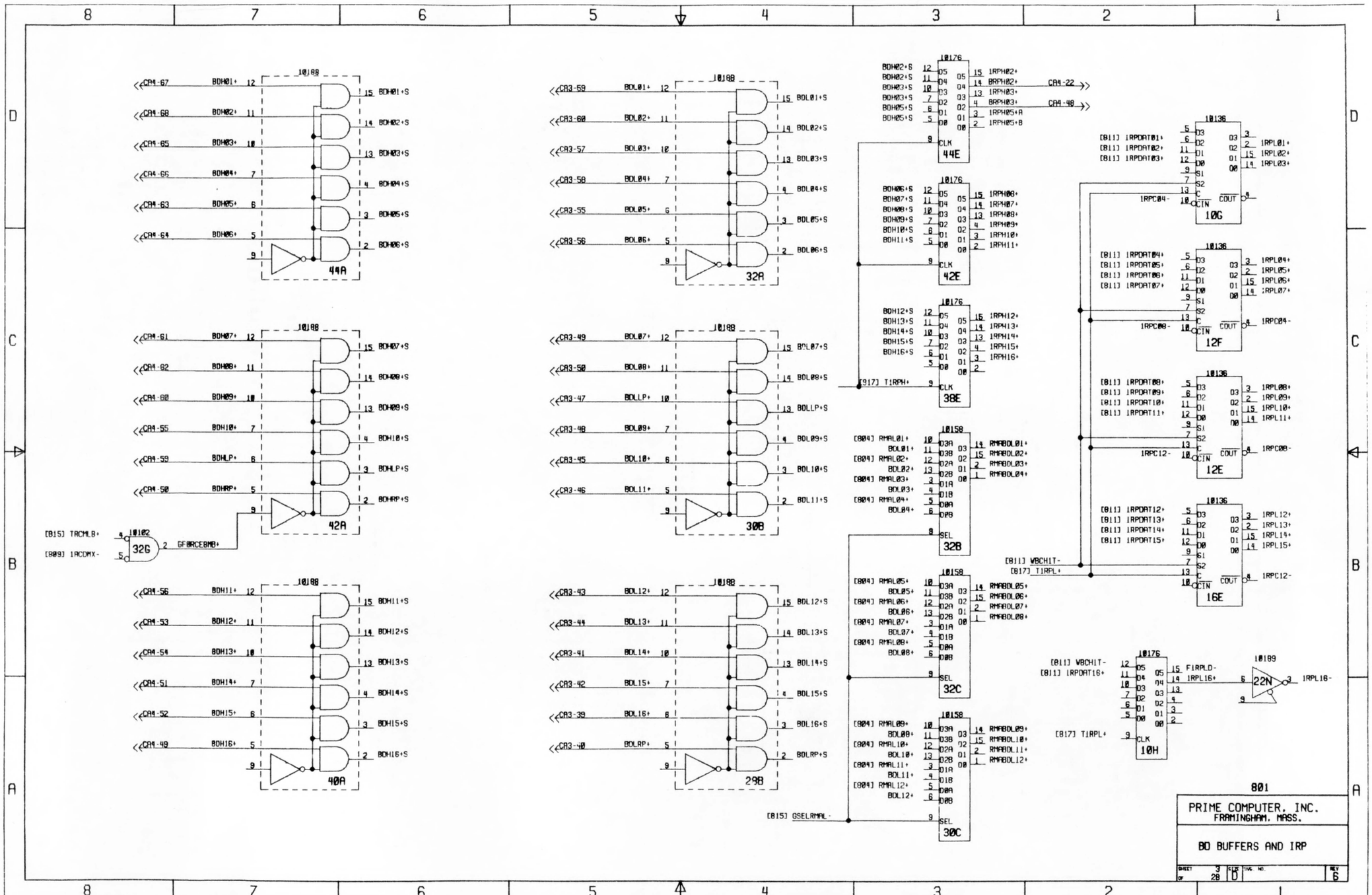
723

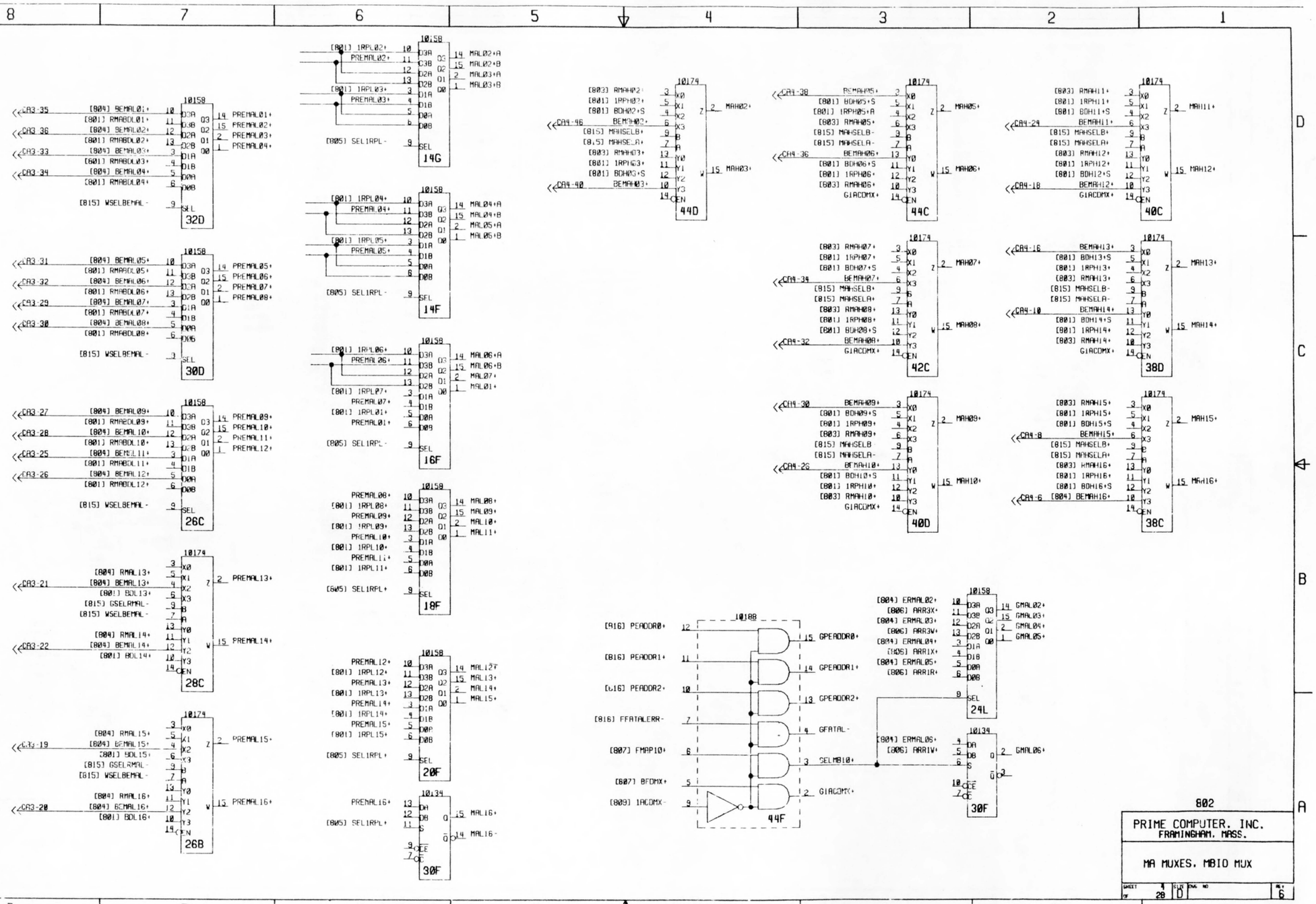
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

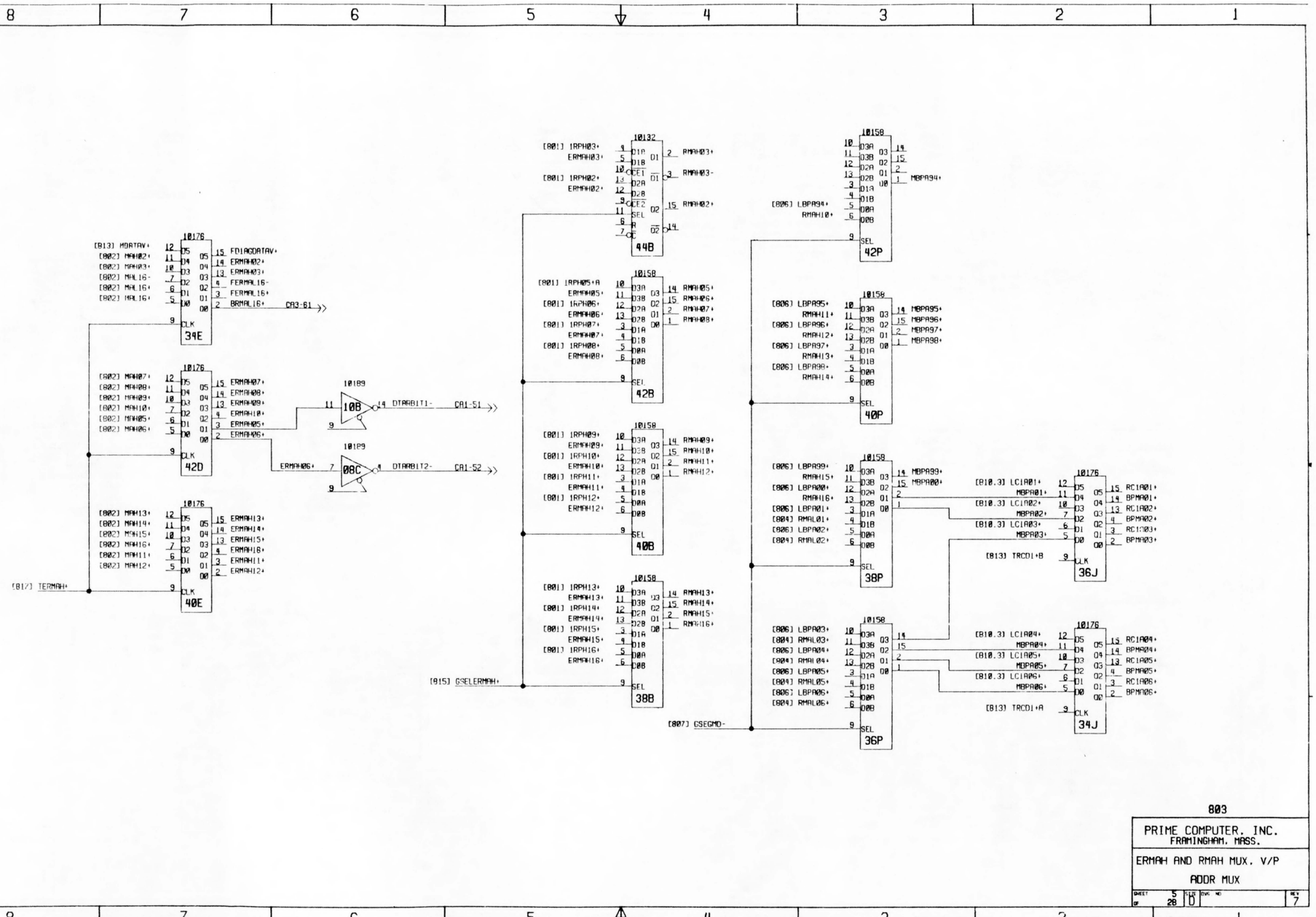
MEMORY CONTROLLER POWER CONNECTORS

SHEET OF	SIZE	DWG. NO	REV
25 30	D	LBD5743	A2


BDH+
BDH+S
BFDMX
IRPH
TIRPH
BEMAH
MAH
RMAH
ERMAH
TERMAH
GSELERMAH+
MA SEL GEN
STLB HASH
TSTLBA+
STLB ADDR REG
BDH+S
ARR
RMAH
WSEGDK-
WPIDOK-
LBPA
RPID
TRPID
BDL+S
STLB
BRNA
IRPL
TBRNC
BRANCH CACHE
WIRPSEL
TIRPL
BCHIT-
RCCIAC
RCMIAC
TRCML
IAC DECODE
RCCDEST
RCMDEST
DEST DECODE
GSEGTRP-
DFUNLBLIP+
GADTRRD+
WSAVIOL+
GPMODTR+
VSVTRAP-
I-UNIT
CS/TA13
CS/TA14
CS/TA15
CS/TA16
407,408
TRAP LOGIC
LPID
LBVA
RMAH
RMAL
ARR
LBPA
LNPOWN
LBPUMOD
BPMA
STLBCP
STLBNA
RCIA
IRPL
TPRMA
BRNA
PAREER+
416
PARITY
TBPMA
CACHEWRIP
TMCLK
TERMA
TMODALS
TSTLB
TCINDX
TBRNC
TPRMA
TRCML
TRPID
TIRPL
417
TIMING
RMA
GSEGMD
TRCDI
BPMA
CIAOK
CACHE MISS 412 LOGIC
CACHE INDEX
RCDI
BDL+
RMABDL
RMAL
BEMAL
PREMAL
MAL
GSELERMAL GEN
WSELBEMAL GEN
SELIRPL GEN
ERMAL
TERMAL
PRMAL
TPRMAL
WSELPRMAL+
FEVEN+
MAL
CADR
TCAWR
BDH+S
BDL+S
BPMA
VRMA
D IN HIGH LOW
INDEX WRITE AD.
ADDRESS
CONTROL
LCDI
LCDE
LCDO
CACHE
CACHE CONTROL
RCDE
RCDO
TRCDE
TRCDO
EVEN DATA
ODD DATA
(RCDE,RCDO)
EMRAH
(RCDO,RCDE)
RMAL
BUS B
BB SEL GEN
800
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
BLOCK DIAGRAM
SHEET 2 OF 20
D
REV 4


44A
32A
42A
30B
40A
29B
32G
32B
32C
30C
38E
44E
42E
10G
12F
12E
16E
10H
22N
801
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
BD BUFFERS AND IRP
SHEET 3 OF 28
FILE 0
REV 6


32D
30D
26C
28C
26B
19G
19F
16F
18F
20F
30F
44D
44C
42C
40D
40C
38D
38C
44F
24L
30F
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MA MUXES, MBIO MUX
802
SHEET 4 OF 28
SIZE D
REV 6



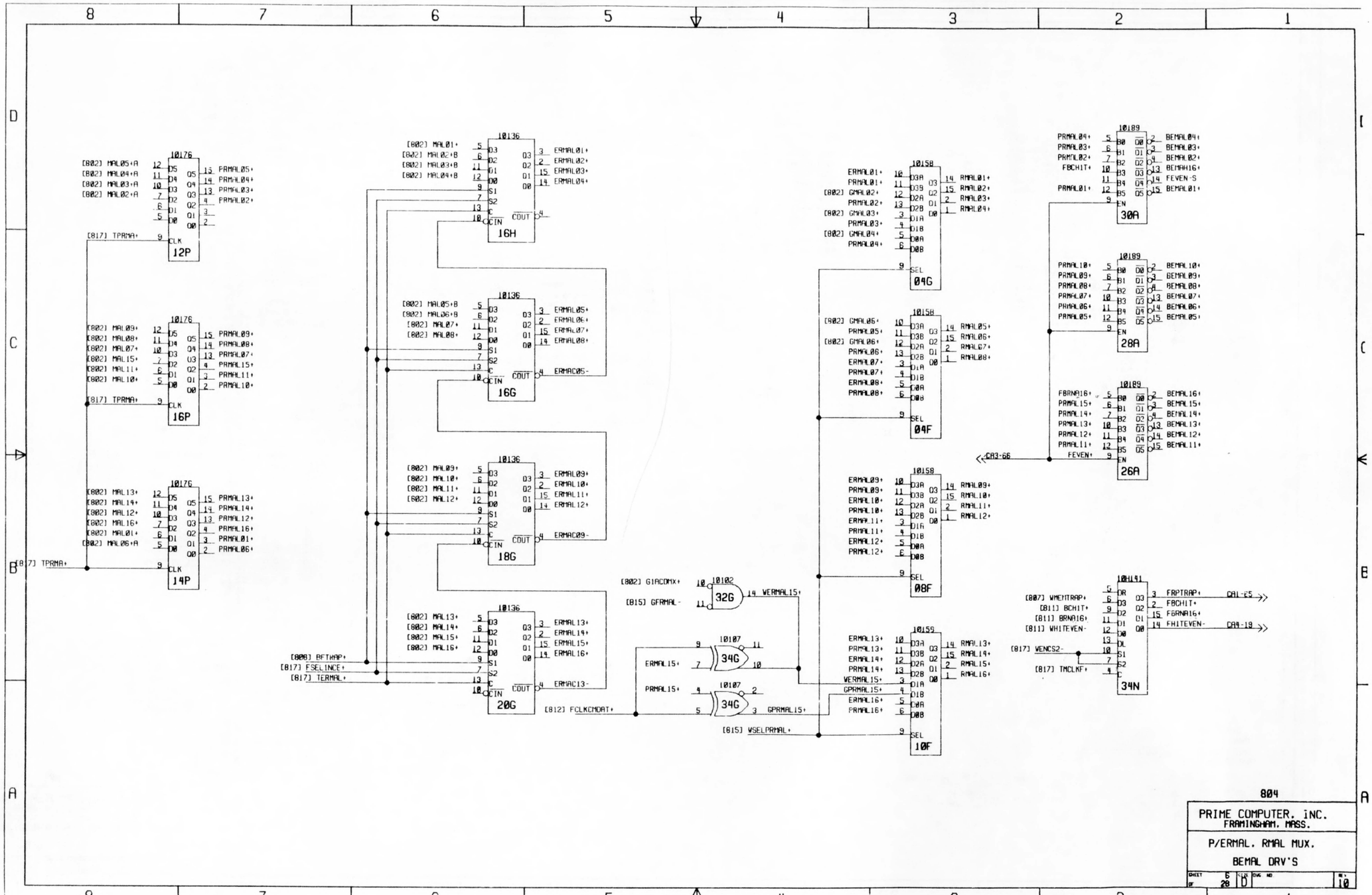
803

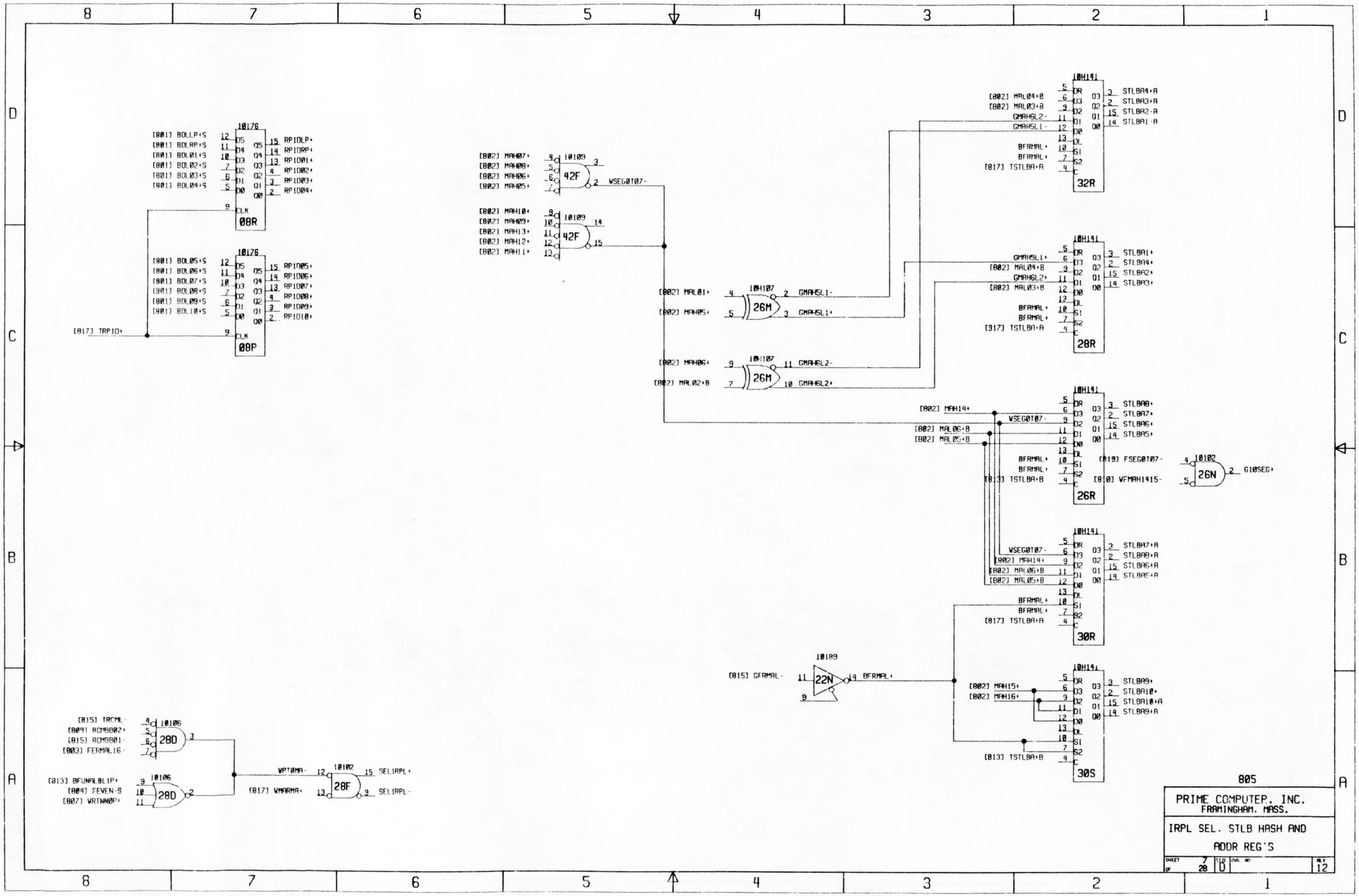
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

ERMAH AND RMAH MUX. V/P

ADDR MUX

SHEET 5 OF 28 | SIZE D | DWG NO | REV 7


12P
16P
14P
16H
16G
18G
20G
32G
34G
34G
04G
04F
08F
10F
30A
28A
26A
34N
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
P/ERMAL, RMAL MUX,
BEMAL DRV'S
804


10L76
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[801] BDLRP+S
[801] BDL01+S
[801] BDL02+S
[801] BDL03+S
[801] BDL04+S
RP1DLP+
RP1DRP+
RP1D01+
RP1D02+
RP1D03+
RP1D04+
08R
[801] BDL05+S
[801] BDL06+S
[801] BDL07+S
[801] BDL08+S
[801] BDL09+S
[801] BDL10+S
RP1D05+
RP1D06+
RP1D07+
RP1D08+
RP1D09+
RP1D10+
[817] TRP1D+
08P
10109
42F
[802] MAH07+
[802] MAH08+
[802] MAH06+
[802] MAH05+
WSEG0T07-
[802] MAH10+
[802] MAH09+
[802] MAH13+
[802] MAH12+
[802] MAH11+
10107
26M
[802] MAL01+
[802] MAH05+
GMAH5L1-
GMAH5L1+
[802] MAH06+
[802] MAL02+B
GMAH6L2-
GMAH6L2+
10H14
32R
[802] MAL04+B
[802] MAL03+B
GMAH6L2-
GMAH5L1-
BFRMAL+
BFRMAL+
[817] TSTLBA+A
STLBA4+A
STLBA3+A
STLBA2-A
STLBA1-A
28R
GMAH5L1+
[802] MAL04+B
GMAH6L2+
[802] MAL03+B
BFRMAL+
BFRMAL+
[817] TSTLBA+A
STLBA1+
STLBA4+
STLBA2+
STLBA3+
26R
[802] MAH14+
WSEG0T07-
[802] MAL06+B
[802] MAL05+B
BFRMAL+
BFRMAL+
[813] TSTLBA+B
STLBA8+
STLBA7+
STLBA6+
STLBA5+
[819] FSEG0T07-
[810] WFMAH1415-
10102
26N
G10SEG+
30R
WSEG0T07-
[802] MAH14+
[802] MAL06+B
[802] MAL05+B
BFRMAL+
BFRMAL+
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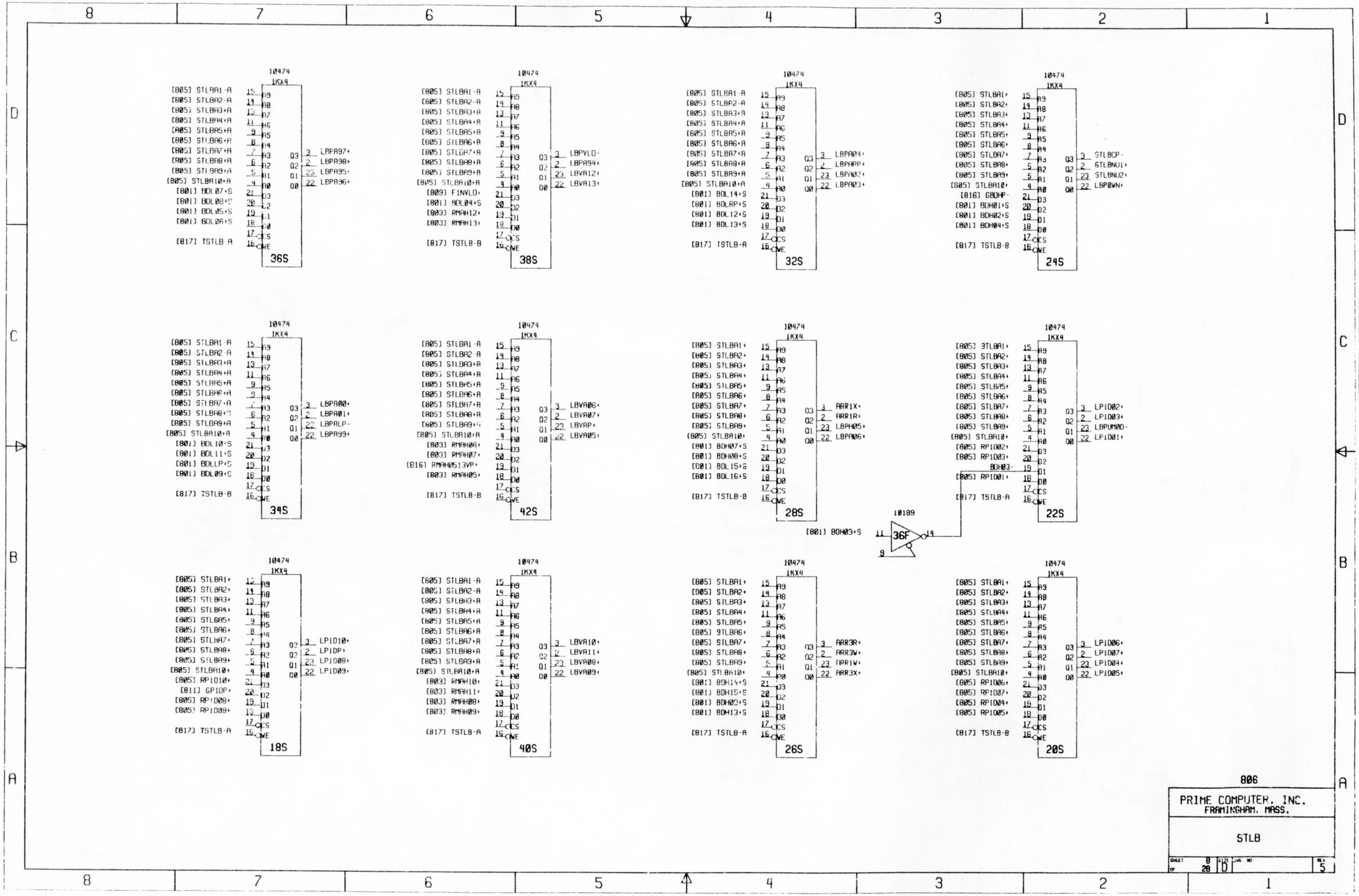
STLBA7+A
STLBA8+A
STLBA6+A
STLBA5+A
10189
22N
[815] GFRMAL-
BFRMAL+
30S
[802] MAH15+
[802] MAH16+
[813] TSTLBA+B
STLBA9+
STLBA10+
STLBA10+A
STLBA9+A
10106
28D
[815] TRCML-
[809] RCMSB02+
[815] RCMSB01-
[803] FERMAL16-
[813] BFUNALBL1P+
[809] FEVEN-S
[807] WRTNW0P+
WPT0MA-
[817] WMARMA+
10102
28F
SELIRPL+
SELIRPL-
805
PRIME COMPUTEP. INC.
FRAMINGHAM. MASS.
IRPL SEL. STLB HASH AND
ADDR REG'S
SHEET 7 OF 28
SIZE D
REV 12

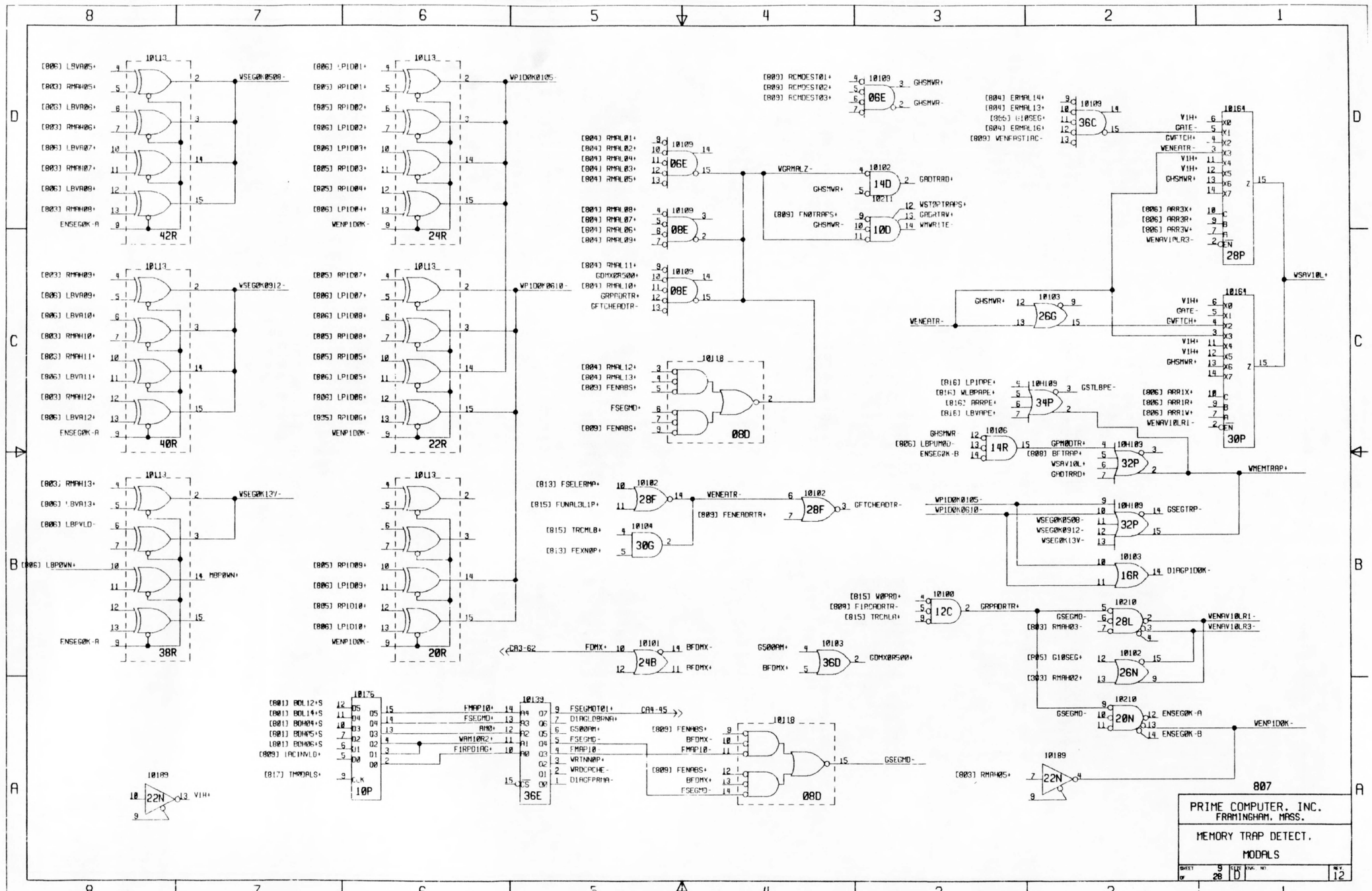


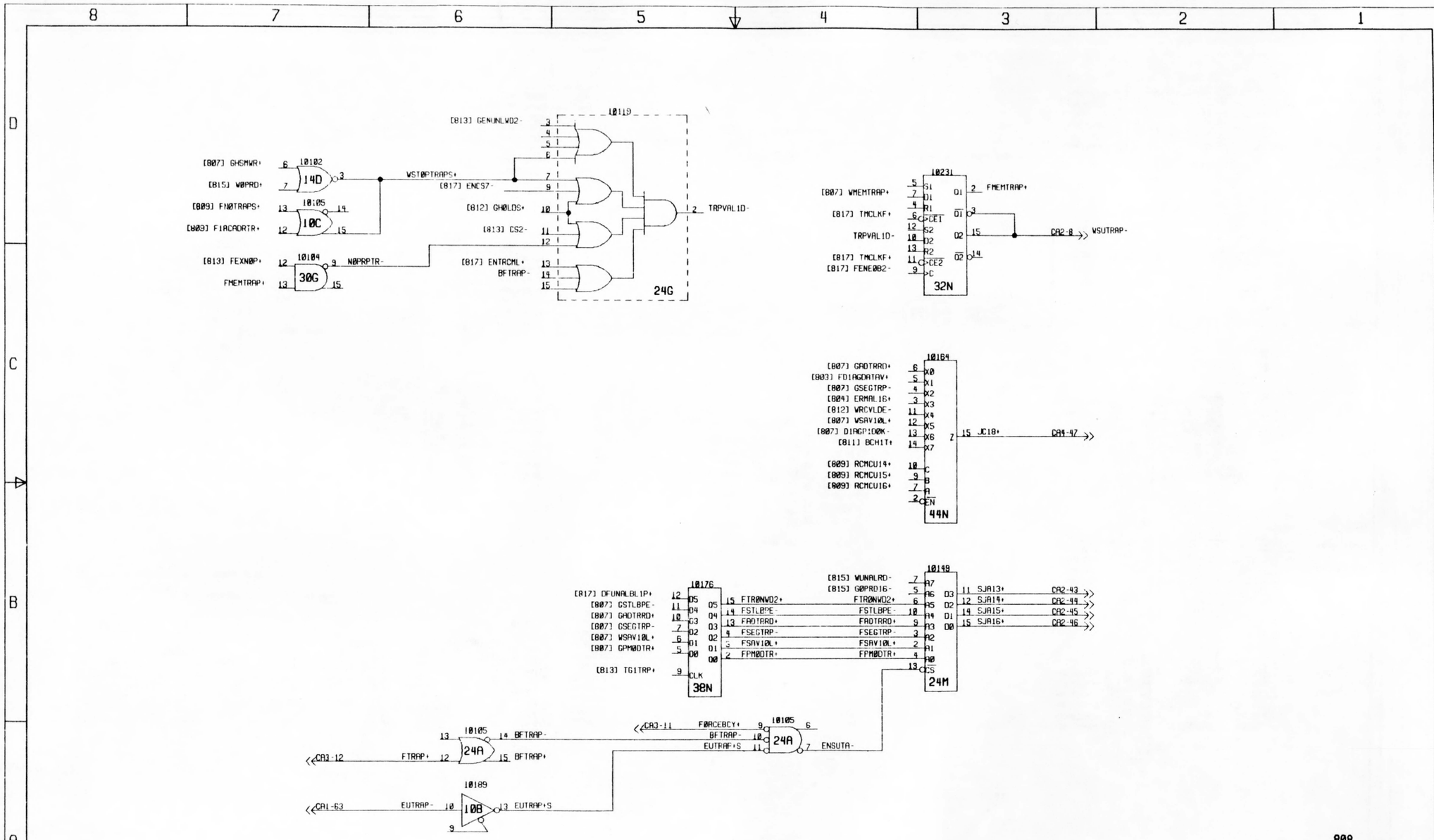
806

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

STLB

SHEET 8 OF 28 | SIZE D | REV 5


42R
24R
40R
22R
38R
20R
06E
08E
14D
10D
08D
36C
28P
26G
30P
34P
14R
32P
16R
12C
28L
26N
20N
22N
24B
30G
36D
28F
10P
36E
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
MEMORY TRAP DETECT,
MODALS
807

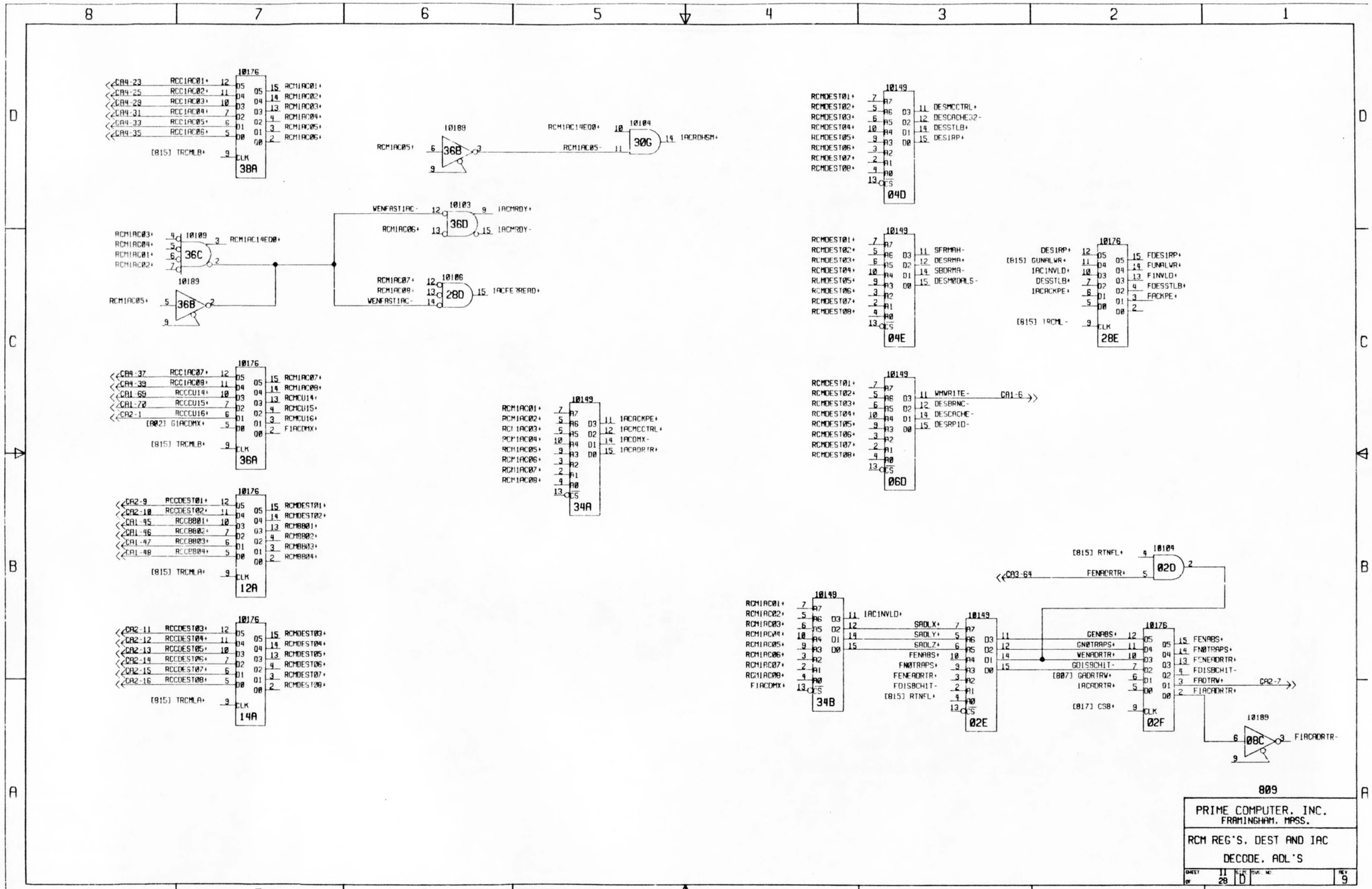


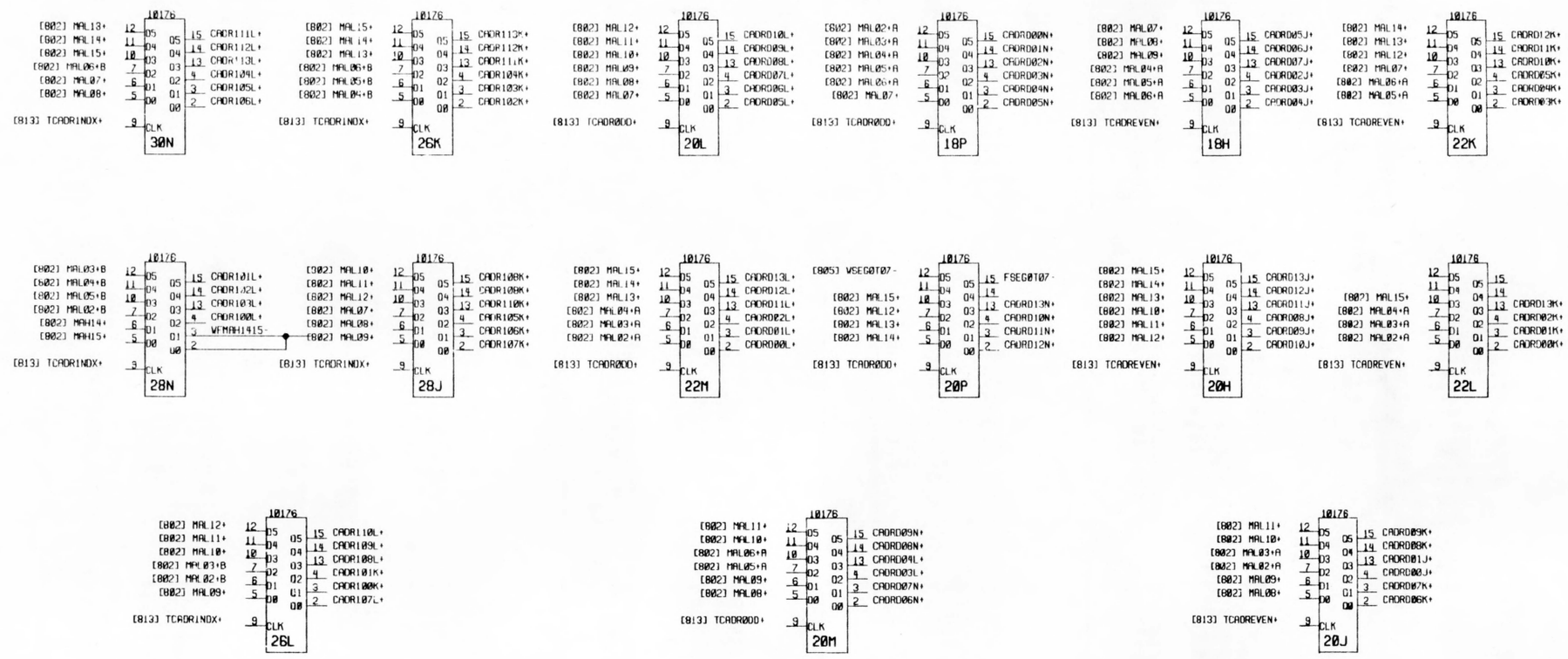
808

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MEMORY TRAP GENERATION

SHEET 10 OF 28 | SIZE D | DWG. NO | REV 10


809
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
RCM REG'S, DEST AND IAC
DECODE, ADL'S
SHEET 11 OF 28
SIZE D
REV 9

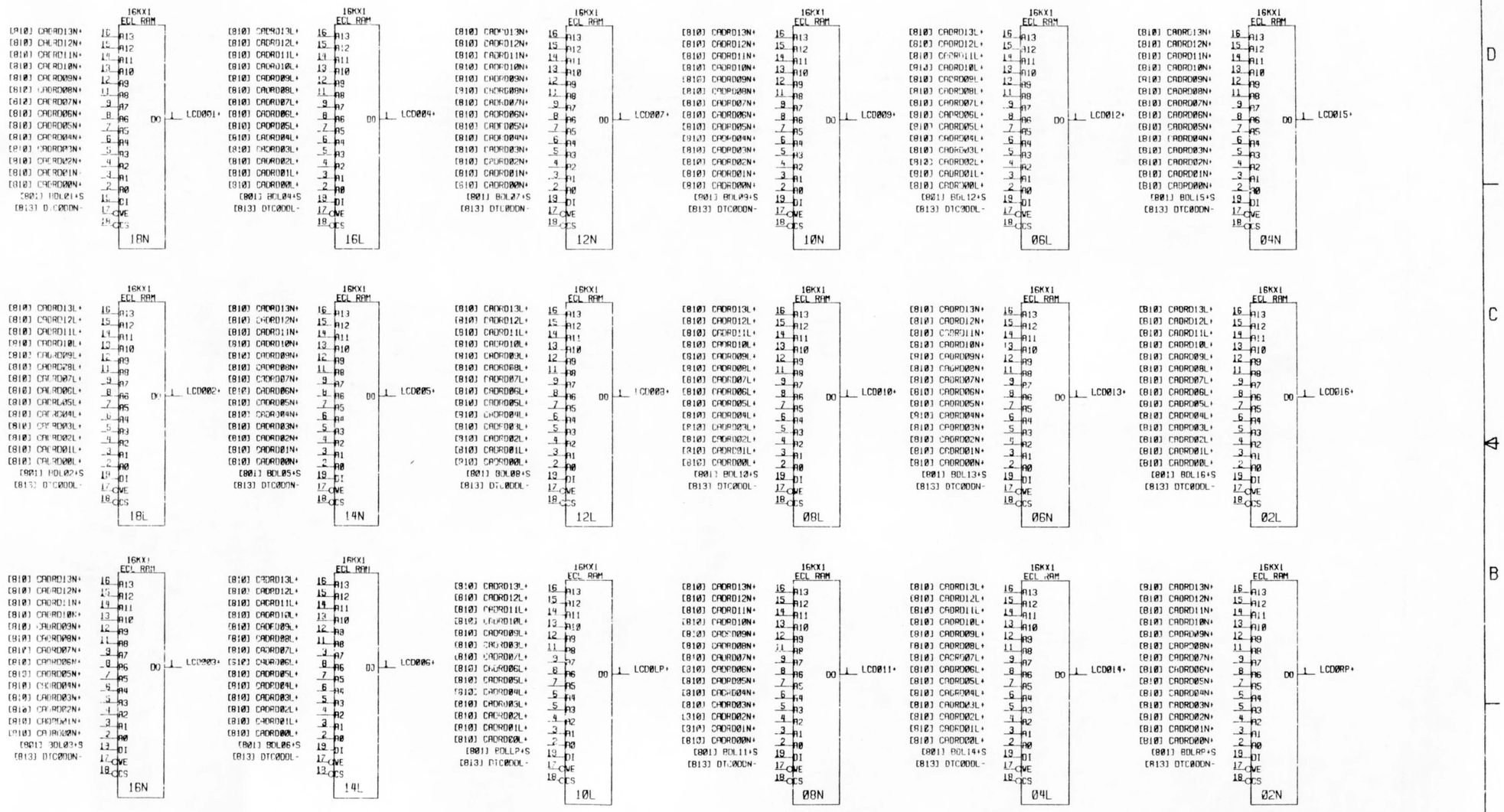


810

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

CACHE, CACHE ADDR FLOPS

SHEET 12 OF 28 | SIZE D | DWG NO | REV 5

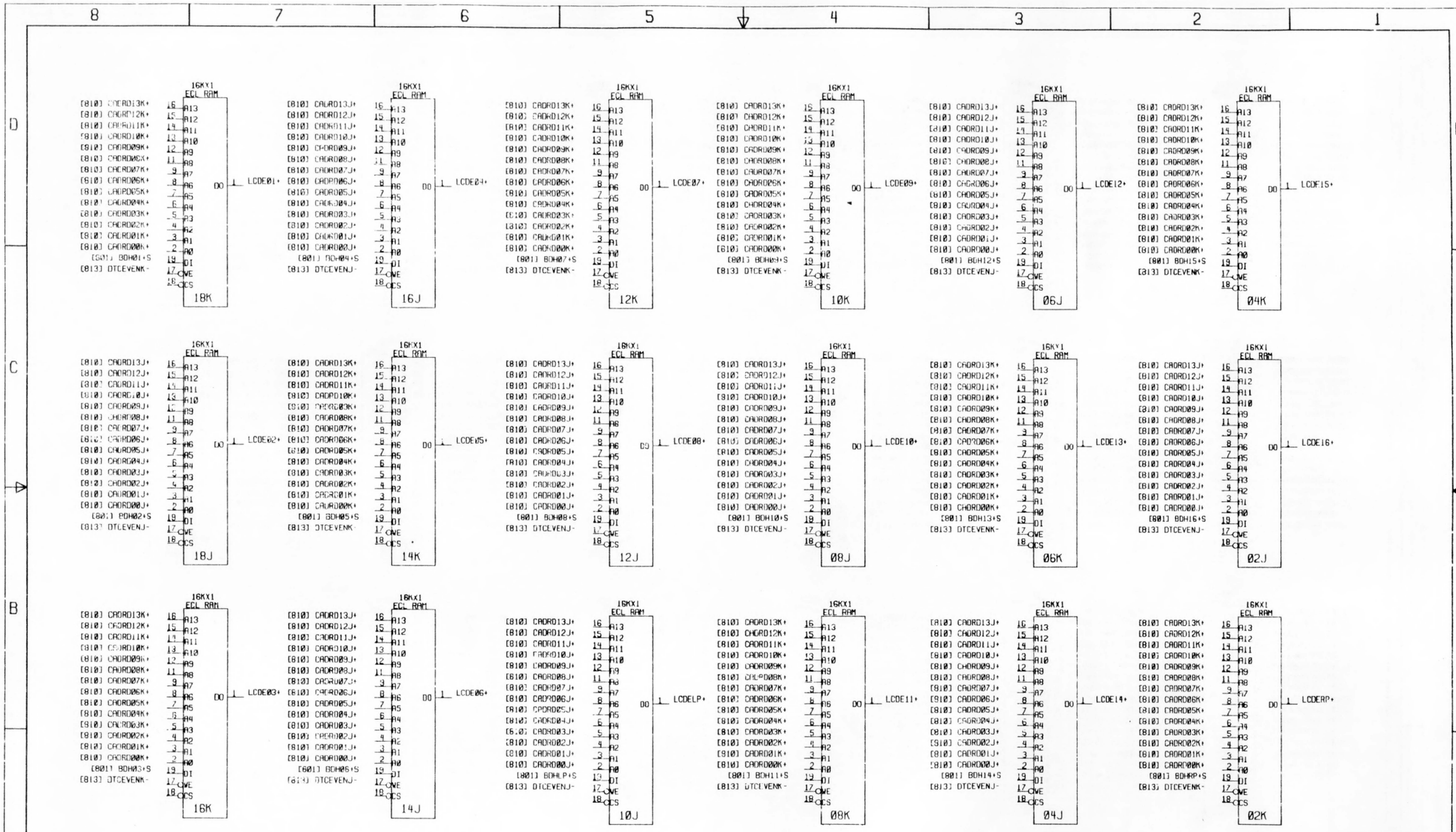


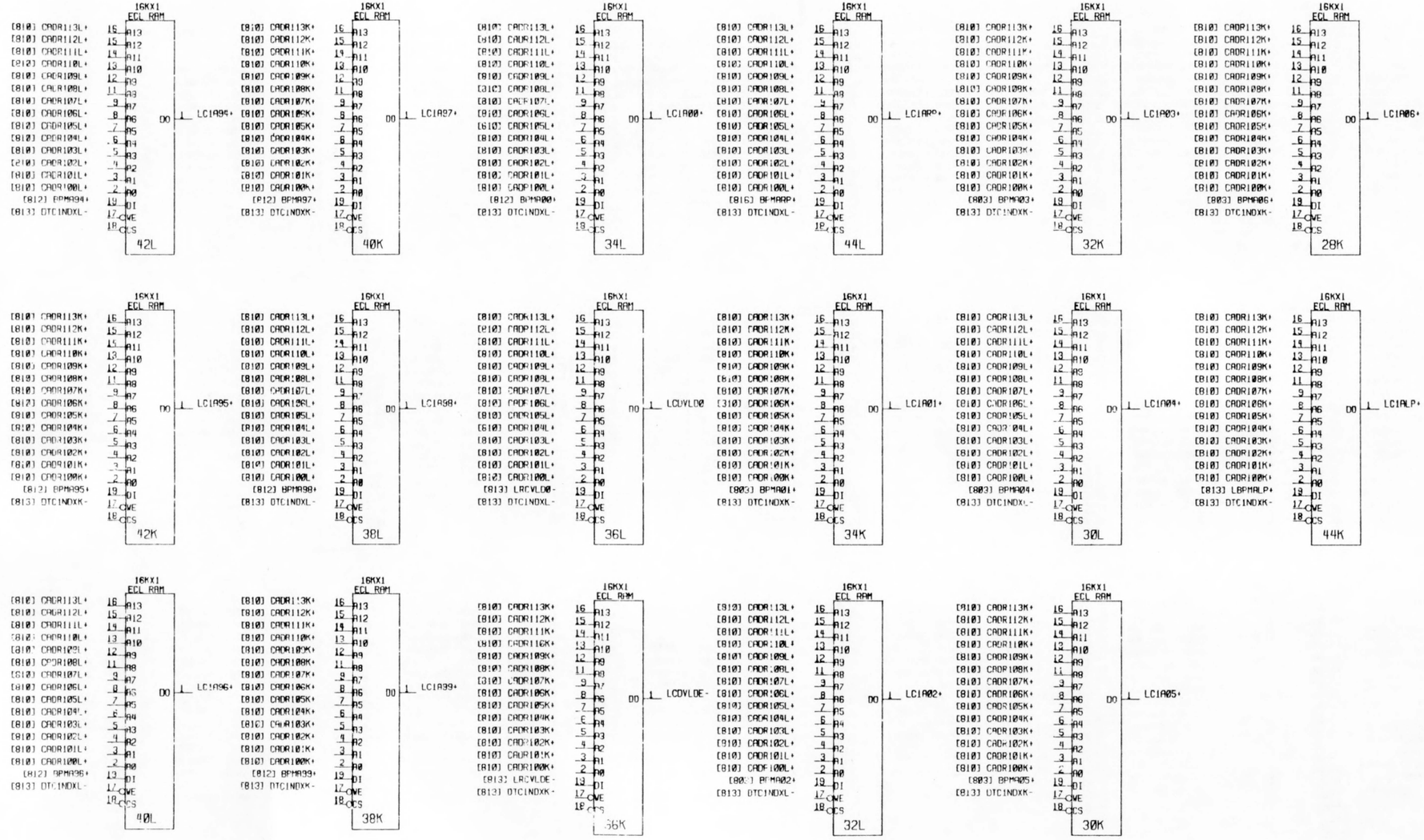
810.1

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

CACHE DATA ODD

SHEET 13 OF 28 | SIZE D | DWG NO | REV 9


16KX1 ECL RAM
18K
16J
12K
10K
06J
04K
18J
14K
12J
08J
06K
02J
16K
14J
10J
08K
04J
02K
LCDE01+
LCDE04+
LCDE07+
LCDE09+
LCDE12+
LCDF15+
LCDE02+
LCDE05+
LCDE08+
LCDE10+
LCDE13+
LCDE16+
LCDE03+
LCDE06+
LCDELP+
LCDE11+
LCDE14+
LCDERP+
B10.2
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
CACHE DATA EVEN
SHEET 14 OF 28
SIZE U
REV 9

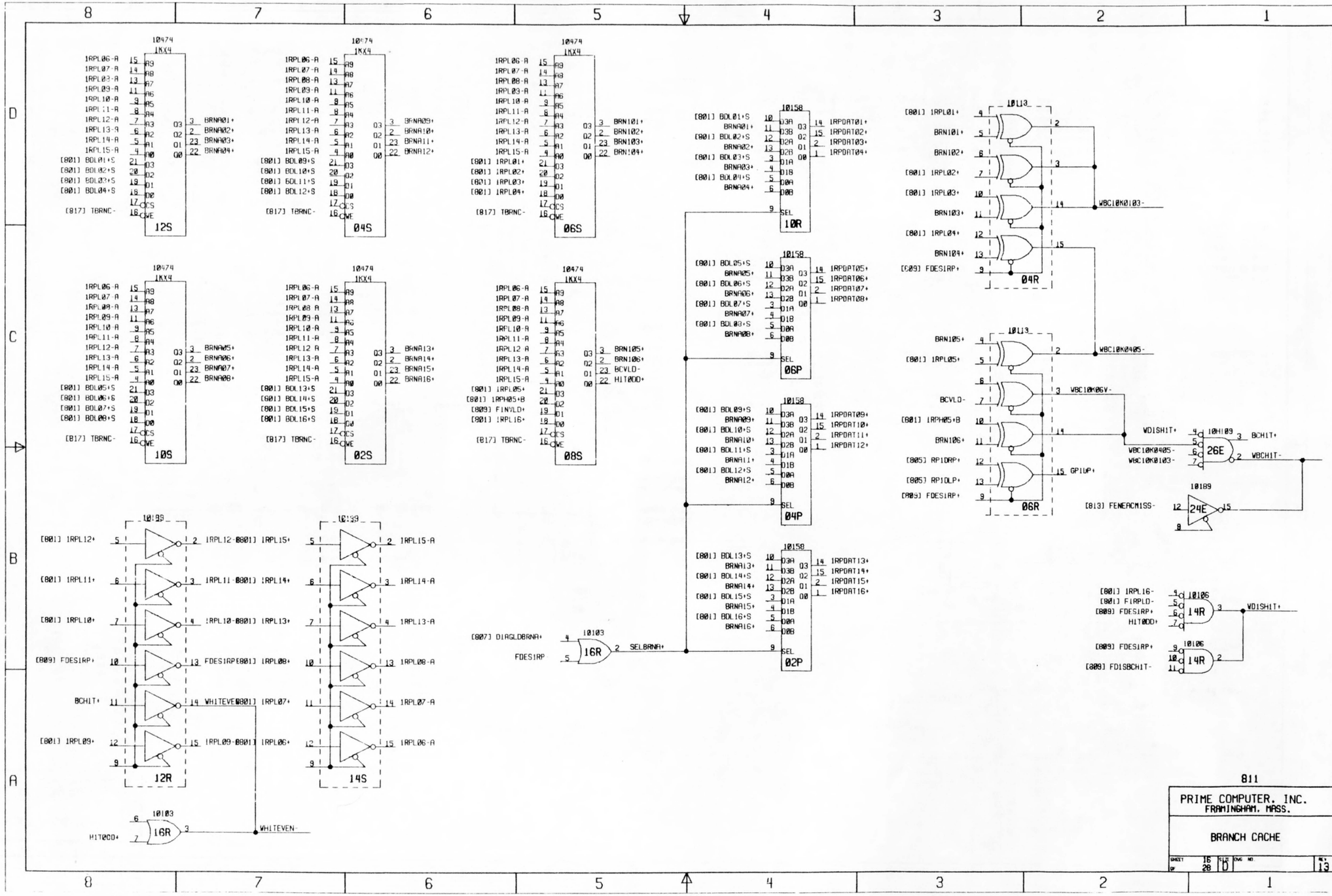


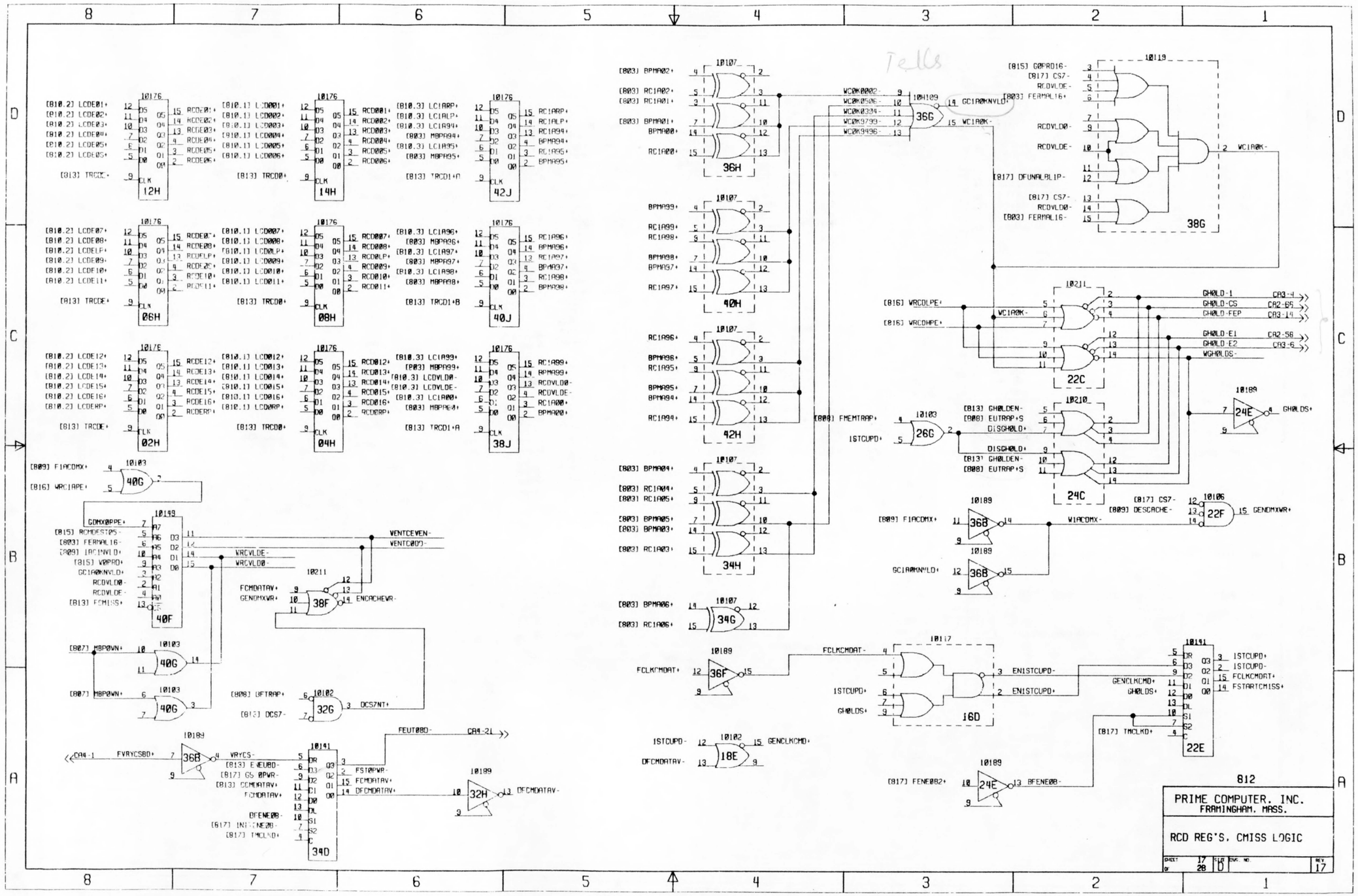
810.3

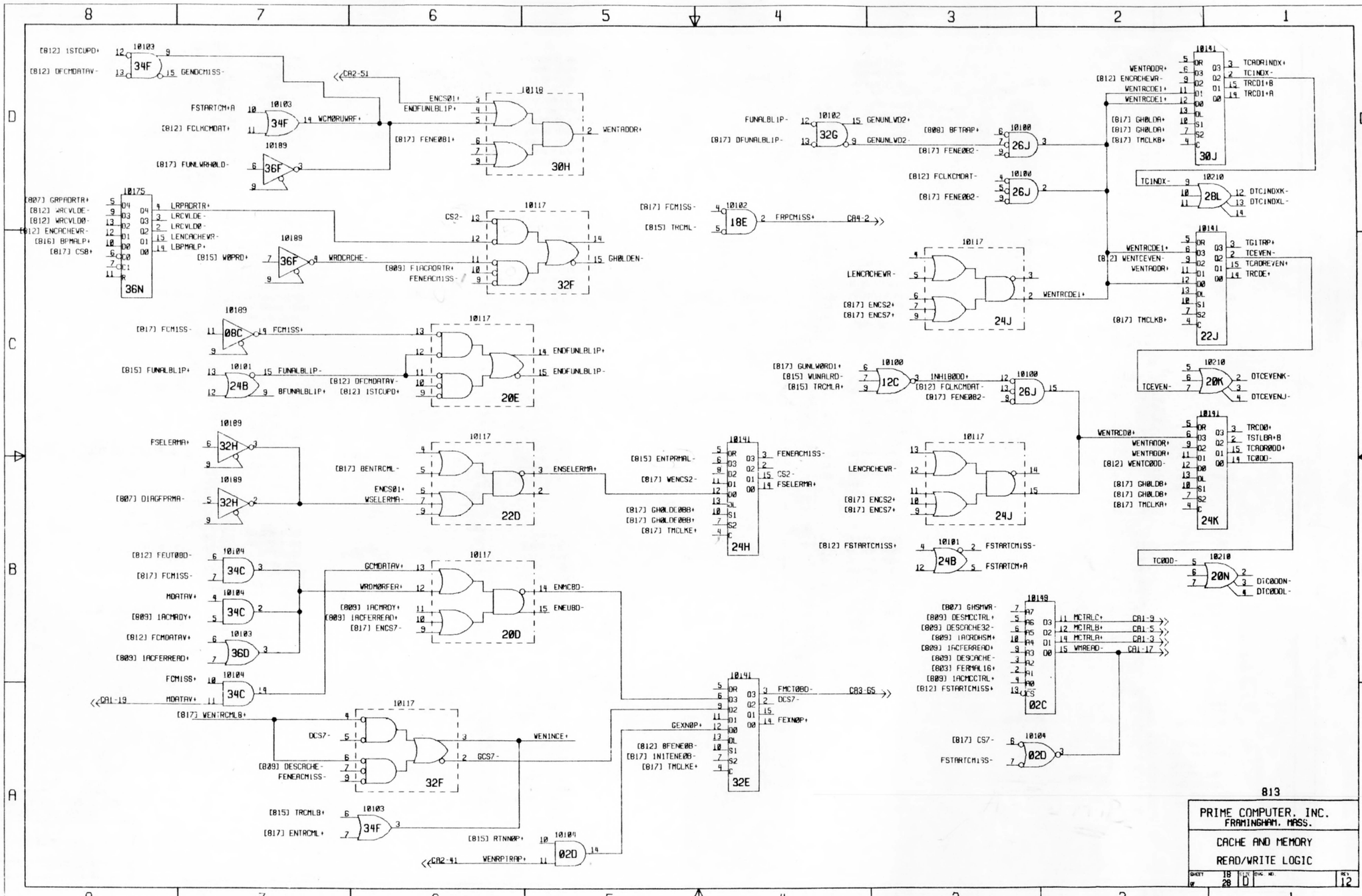
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

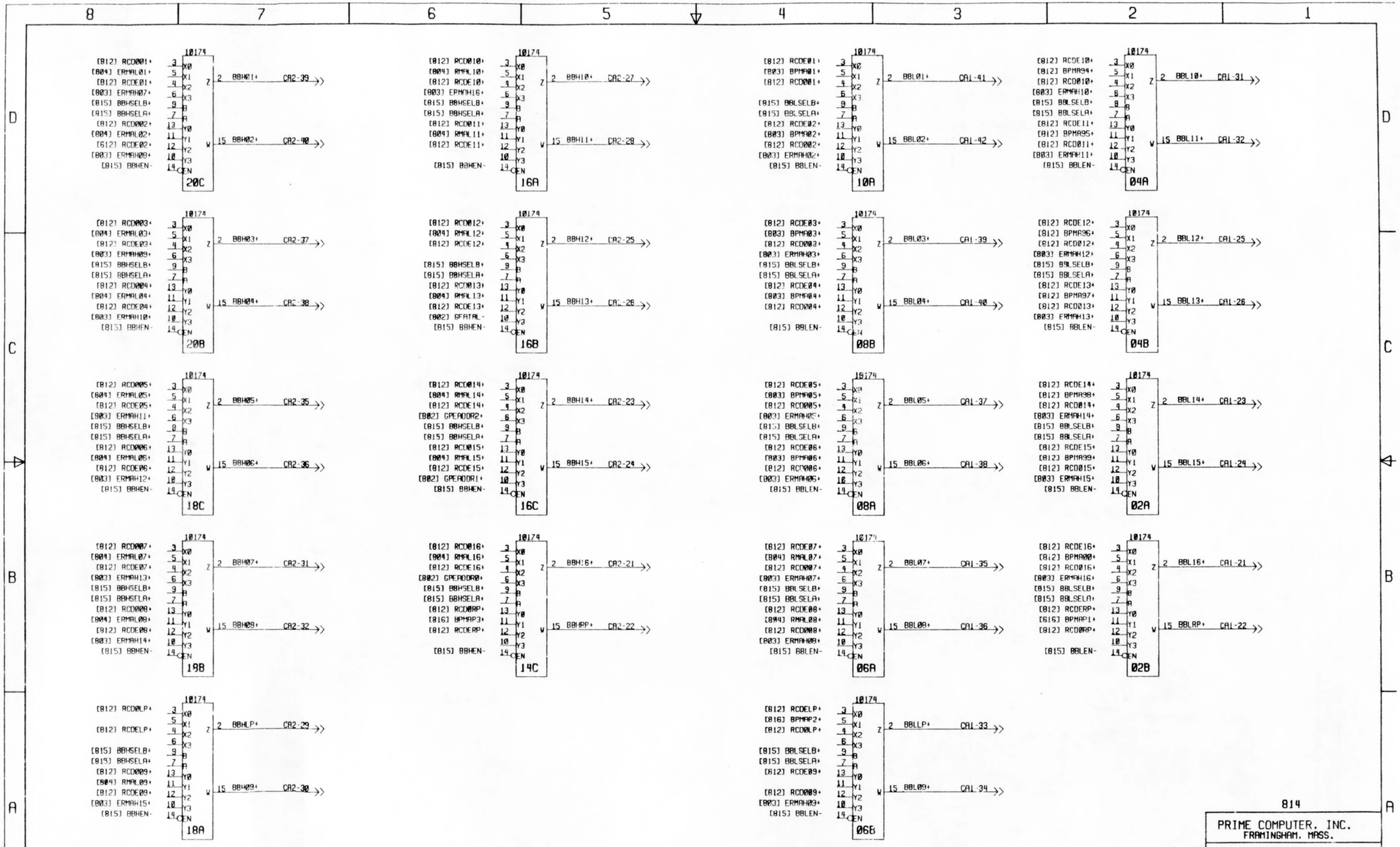
CACHE INDEX, VALID BITS

SHEET 15 OF 28 | SIZE D | DWG NO | REV 34


12S
04S
06S
10S
02S
08S
10R
06P
04P
02P
04R
06R
12R
14S
16R
26E
24E
14R
811
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
BRANCH CACHE


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
RCD REG'S, CMISS LOGIC
812
SHEET 17 OF 20
FILE DWG NO D
REV 17


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
CACHE AND MEMORY
READ/WRITE LOGIC
813
SHEET 18 OF 28
SIZE D
REV 12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[B15] BBHSELA+
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[B04] ERMAL02+
[B12] RCDE02+
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[B15] BBHEN-
10174
BBH01+ CA2-39
BBH02+ CA2-40
20C
[B12] RCD003+
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[B12] RCD004+
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[B12] RCDE04+
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[B15] BBHEN-
10174
BBH03+ CA2-37
BBH04+ CA2-38
20B
[B12] RCD005+
[B04] ERMAL05+
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[B12] RCD006+
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[B15] BBHEN-
10174
BBH05+ CA2-35
BBH06+ CA2-36
18C
[B12] RCD007+
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[B03] ERMAH13+
[B15] BBHSELB+
[B15] BBHSELA+
[B12] RCD008+
[B04] ERMAL08+
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[B15] BBHEN-
10174
BBH07+ CA2-31
BBH09+ CA2-32
19B
[B12] RCD0LP+
[B12] RCDELP+
[B15] BBHSELB+
[B15] BBHSELA+
[B12] RCD009+
[B04] RMAL09+
[B12] RCDE09+
[B03] ERMAH15+
[B15] BBHEN-
10174
BBHLP+ CA2-29
BBH09+ CA2-30
18A
[B12] RCD010+
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[B12] RCDE10+
[B03] ERMAH16+
[B15] BBHSELB+
[B15] BBHSELA+
[B12] RCD011+
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[B12] RCDE11+
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10174
BBH10+ CA2-27
BBH11+ CA2-28
16A
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10174
BBH12+ CA2-25
BBH13+ CA2-26
16B
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[B12] RCDE14+
[B02] GPEADDR2+
[B15] BBHSELB+
[B15] BBHSELA+
[B12] RCD015+
[B04] RMAL15+
[B12] RCDE15+
[B02] GPEADDR1+
[B15] BBHEN-
10174
BBH14+ CA2-23
BBH15+ CA2-24
16C
[B12] RCD016+
[B04] RMAL16+
[B12] RCDE16+
[B02] GPEADDR0+
[B15] BBHSELB+
[B15] BBHSELA+
[B12] RCD0RP+
[B16] BPMAP3+
[B12] RCDERP+
[B15] BBHEN-
10174
BBH16+ CA2-21
BBHPP+ CA2-22
14C
[B12] RCDE01+
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[B15] BBLSELB+
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[B03] BPMA02+
[B12] RCD002+
[B03] ERMAH02+
[B15] BBLEN-
10174
BBL01+ CAL-41
BBL02+ CAL-42
10A
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[B03] BPMA03+
[B12] RCD003+
[B03] ERMAH03+
[B15] BBLSELB+
[B15] BBLSELA+
[B12] RCDE04+
[B03] BPMA04+
[B12] RCD004+
[B15] BBLEN-
10174
BBL03+ CAL-39
BBL04+ CAL-40
08B
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[B12] RCD005+
[B03] ERMAH05+
[B15] BBLSELB+
[B15] BBLSELA+
[B12] RCDE06+
[B03] BPMA06+
[B12] RCD006+
[B03] ERMAH06+
[B15] BBLEN-
10174
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BBL06+ CAL-38
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[B12] RCD008+
[B03] ERMAH08+
[B15] BBLEN-
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BBL07+ CAL-35
BBL08+ CAL-36
06A
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[B16] BPMAP2+
[B12] RCD0LP+
[B15] BBLSELB+
[B15] BBLSELA+
[B12] RCDE09+
[B12] RCD009+
[B03] ERMAH09+
[B15] BBLEN-
10174
BBLLP+ CAL-33
BBL09+ CAL-34
06B
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[B12] RCD010+
[B03] ERMAH10+
[B15] BBLSELB+
[B15] BBLSELA+
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BBL10+ CAL-31
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[B15] BBLSELA+
[B12] RCDE13+
[B12] BPMA97+
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[B15] BBLEN-
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BBL13+ CAL-26
04B
[B12] RCDE14+
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[B12] RCD014+
[B03] ERMAH14+
[B15] BBLSELB+
[B15] BBLSELA+
[B12] RCDE15+
[B12] BPMA99+
[B12] RCD015+
[B03] ERMAH15+
[B15] BBLEN-
10174
BBL14+ CAL-23
BBL15+ CAL-24
02A
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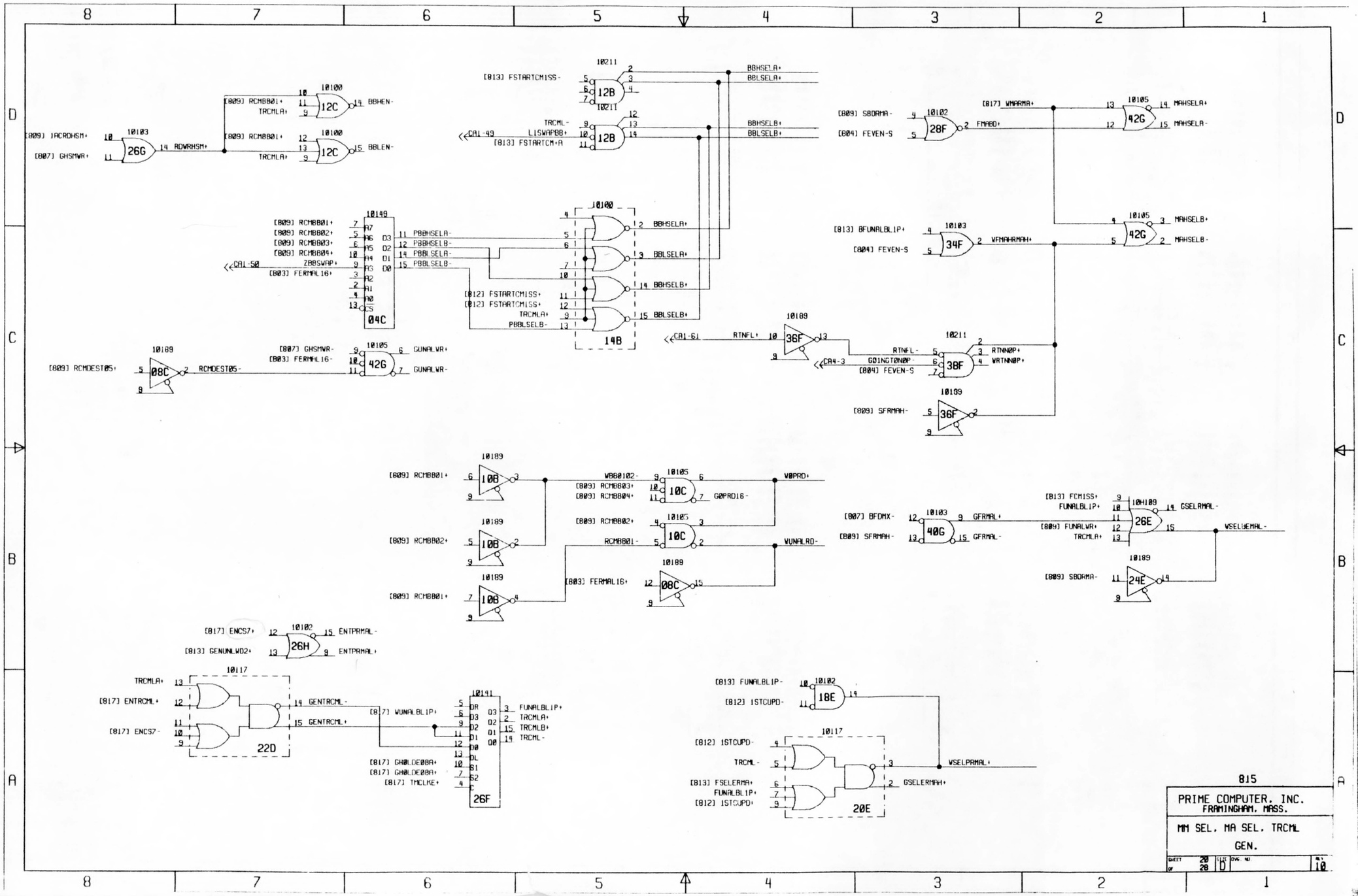
10174
BBL16+ CAL-21
BBLRP+ CAL-22
02B
814
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
BB MUXES
SHEET 19 OF 28
FILE
ENG. NO
REV 4

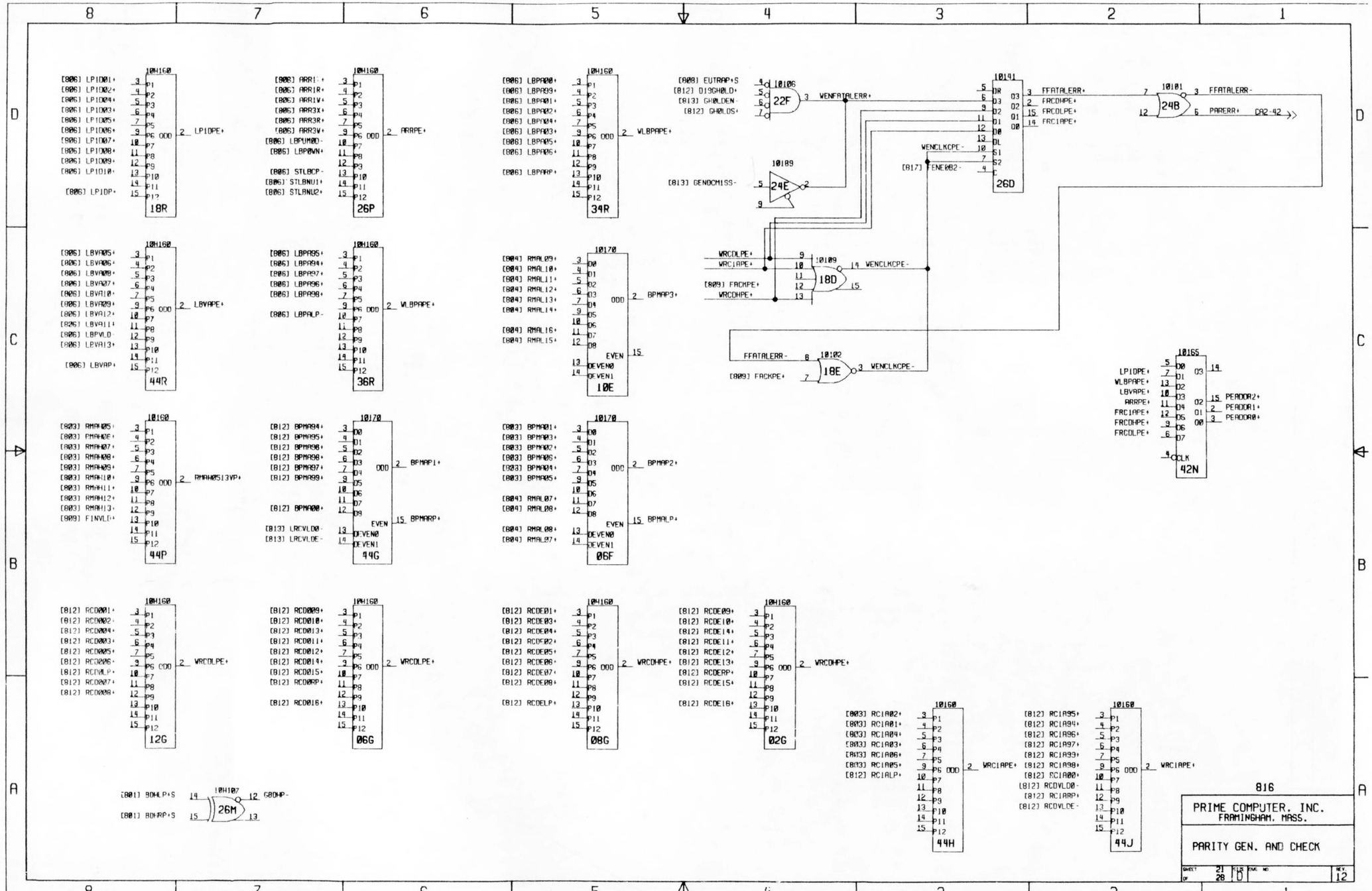


815

PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

MM SEL. MA SEL. TRCML GEN.

SHEET 20 OF 28 SIZE D REV. NO. 10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ARRPE+
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WLBPAPE+
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WENFATALERR+
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WENCLKCPE-
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26D
FFATALERR+
FRCDHPE+
FRCDLPE+
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PARERR+
CA2-42
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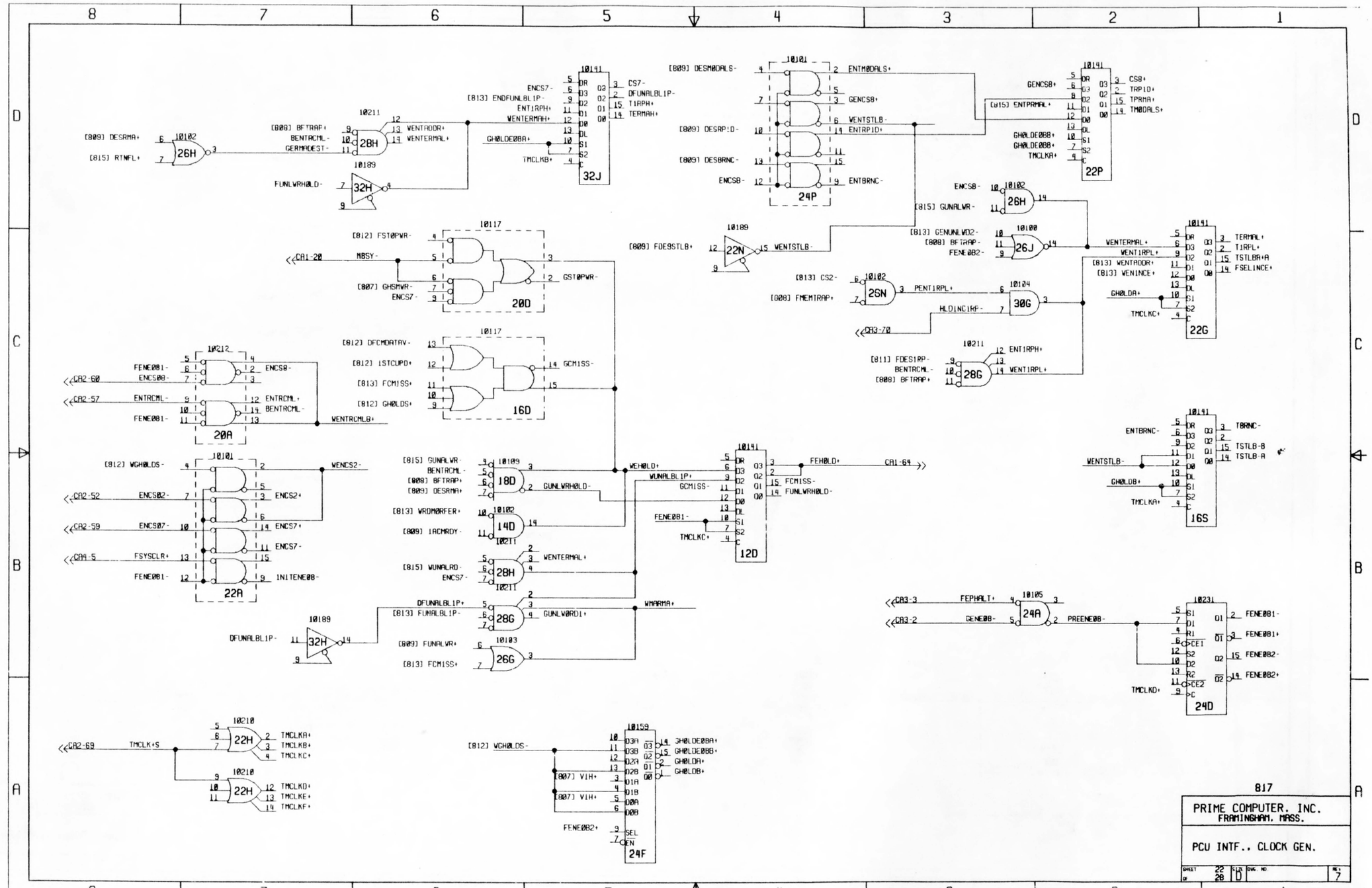
WRCIAPE+
816
PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
PARITY GEN. AND CHECK
SHEET 21 OF 28
FILE 10
ENG NO.
REV. 12


PRIME COMPUTER, INC.
FRAMINGHAM, MASS.
PCU INTF.. CLOCK GEN.
817
SHEET 22 OF 28
SIZE D
DWG NO
REV 7
20D
16D
20A
22A
18D
14D
28H
28G
26G
32H
22H
26H
28H
28N
26J
30G
28G
24P
22P
22G
16S
12D
24A
24D
24F
32J

CA1-13 >>GND

CA1-14 >>GND

CA1-27 >>-5.2V

CA1-28 >>-5.2V

CA1-29 >>-5.2V

CA1-30 >>-5.2V

CA1-43 >>-2V

CA1-44 >>-2V

CA1-57 >>GND

CA1-58 >>GND

CA1-59 >>GND

CA1-60 >>GND

CA2-3 >>GND

CA2-4 >>GND

CA2-17 >>-5.2V

CA2-18 >>-5.2V

CA2-19 >>-5.2V

CA2-20 >>-5.2V

CA2-33 >>-2V

CA2-34 >>-2V

CA2-47 >>GND

CA2-48 >>GND

CA2-61 >>GND

CA2-62 >>GND

CA2-63 >>GND

CA2-64 >>GND

CA2-67 >>GND

CA2-70 >>GND

CA3-1 >>GND

CA3-7 >>GND

CA3-8 >>GND

CA3-9 >>GND

CA3-10 >>GND

CA3-23 >>GND

CA3-24 >>GND

CA3-37 >>-2V

CA3-38 >>-2V

CA3-51 >>-5.2V

CA3-52 >>-5.2V

CA3-53 >>-5.2V

CA3-54 >>-5.2V

CA3-67 >>GND

CA3-68 >>GND

CA4-11 >>GND

CA4-12 >>GND

CA4-13 >>GND

CA4-14 >>GND

CA4-27 >>-2V

CA4-28 >>-2V

CA4-41 >>-5.2V

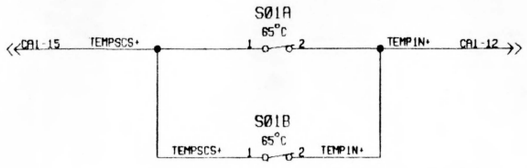
CA4-42 >>-5.2V

CA4-43 >>-5.2V

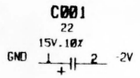
CA4-44 >>-5.2V

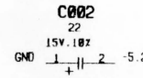
CA4-57 >>GND

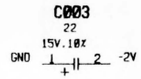
CA4-58 >>GND

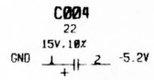


ONLY ONE TEMPERATURE SENSOR WILL BE MOUNTED IN THE BOARD









NOTES :

1. .01 UF AXIAL LEAD CAPACITORS ARE NOT SHOWN BUT ARE INSTALLED ADJACENT TO ALL DIPS IN THE FOLLOWING COLUMNS : A.C.E.G.J.L.N EXCEPT AT 14L.

2. UNLESS OTHERVISE SPECIFIED :
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS.

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PRIME COMPUTER, INC.
FRAMINGHAM, MASS.

POWER CONN. TEMP SEN

SHEET 23 OF 28 | SIZE D | DWG. NO | REV 3