LOGICON 2+2

DRUM PROCESSOR

MANUAL

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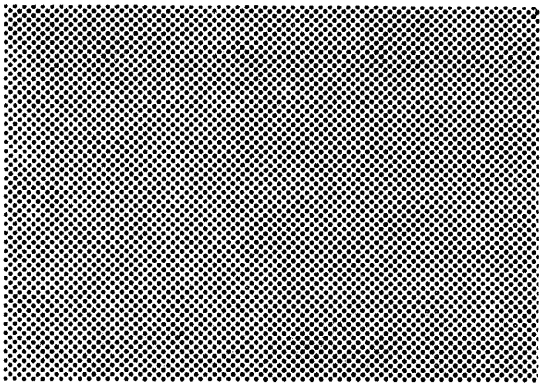


I...

Equipment Description

GENERAL

The LOGICON 2+2 Drum Processor (DP), Figure 1-1, is designed to control data exchanges between main memory (core) and an auxiliary memory (drum) efficiently and with a high degree of information integrity. Emphasis has also been placed on command flexibility and minimum real-time processor burden.

All data transfers are effected in groups of 512_{10} data words known as pages. Associated with each page is a pre-recorded drum address word (verified before write), a programmable code word (checked during read), and an efficient integrity word (generated by DP or program, always checked by DP).

Information integrity of each data page is preserved by three DP methods: address verification, code word verification, and integrity word generation/verification.

Proven TTL logic and MSI elements are used to achieve performance and high reliability. Extensive maintenance features are provided. High density packaging minimizes space requirements. Replacement modules are the integrated circuits themselves.

The DP will operate at data transfer rates up to 4 million bytes per second and with a variety of fixed head drums with capacities ranging from 1/2 to 8 million 8 bit bytes. Single or dual core memory access is available. The two memories may be addressed simultaneously or sequentially.

The DP features direct memory access for control words, thus requiring a minimum of real time processor response for efficient operation. Control word look-ahead is employed to combine a contiguous drum sector

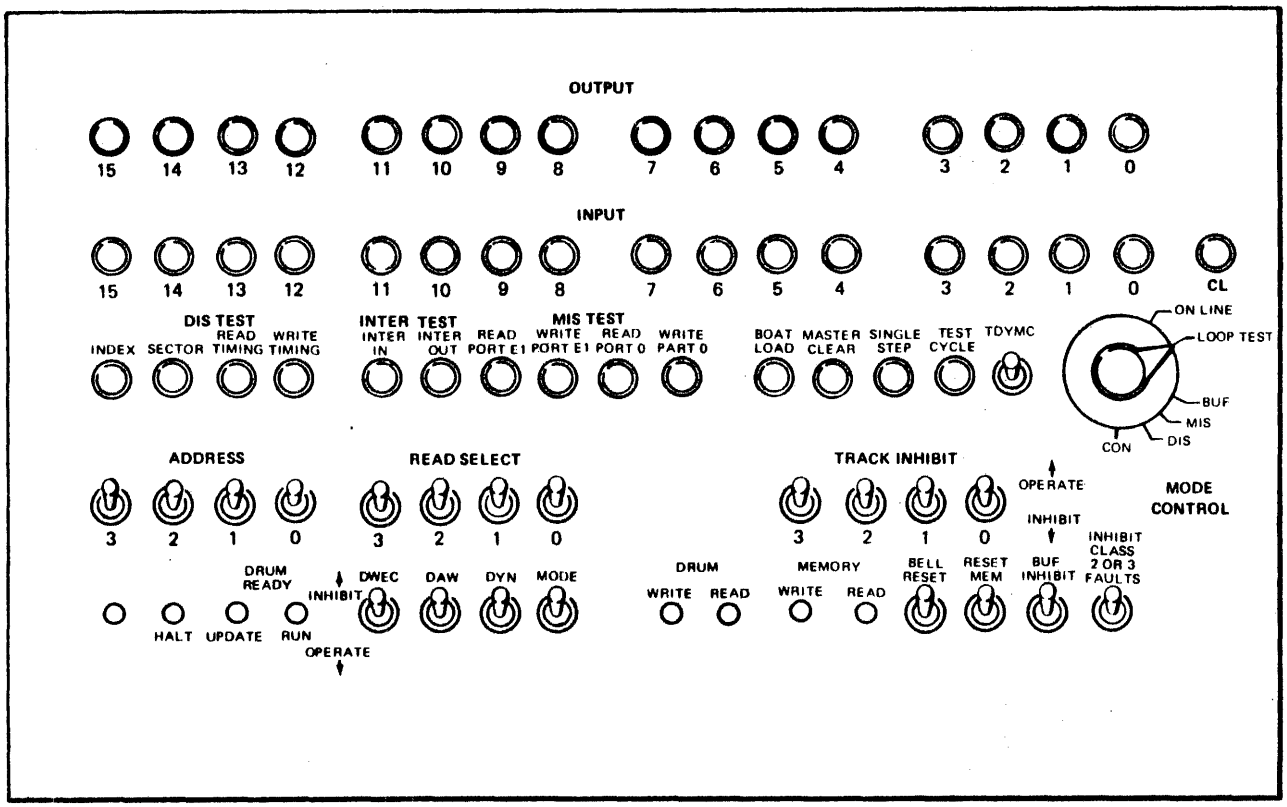


Figure 1-1. LOGICON 2+2 Drum Processor (DP)

transfer capability with a list driven command word chaining structure. Both mode (read/write) and address (TK/TK) changes may occur between contiguous sectors.

LEADING PARTICULARS

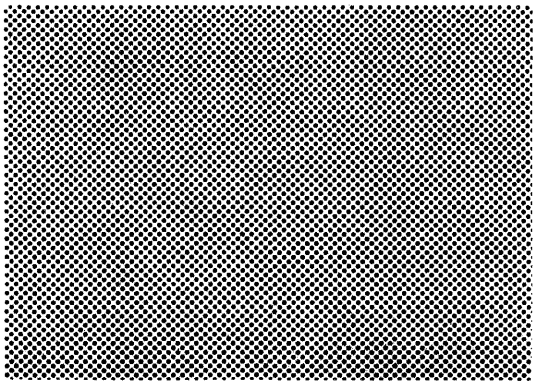
Table 1-1 provides a list of leading particulars on the LOGICON 2+2 Drum Processor.

TABLE 1-1. DRUM PROCESSOR LEADING PARTICULARS

Characteristic	Particulars
• Size (logic module) (maintenance panel)	19" wide x 18" deep x 3 1/2" high 19" wide x 3" deep x 12" high
• Weight	50 #

TABLE 1-1. DRUM PROCESSOR LEADING PARTICULARS (Contd)

Characteristic	Particulars
• Power	115 VAC, 5 amp.
• Interfaces	16 bit parallel digital interface to core memory(s) (One or two memory ports) 1, 2, 4, or 8 bit parallel digital interface to drum memory 2 interrupts/acknowledgement signals to/from processor
• Addressing	Core memory - up to 128 K - directly Drum - 8M bytes in 512_{10} word sectors
• Speed	Memory - 2 MHZ word rate Drum - 2 MHZ/byte rate
• Commands	Read - 3, Write - 4 Interrupt Enable Conditions - 3 Command Linkage Conditions - 3
• Status Words	Current LDC mode. Current sector. Last Command Word Pointer 14 unique error conditions
• Integrity Functions	Address verification before read or write. Code word verification before read. Integrity word generation/verification for write/read.
• Circuitry	TTL integrated circuits - Functional and MSI elements. High Speed LSI scratch pad memory.
• Other	Local and external bootload feature. Simple change for various drum sizes. Extensive test and maintenance features built-in.



II...

System Tie-In Description

GENERAL

The LOGICON 2+2 time-sharing system is configured around four mini-computers; one of these is the Drum Processor (DP), the heart of the Extended Memory Subsystem.

The DP is designed to control the exchange (swapping) of data between main memory (core) and auxiliary memory (drum). All data transfers are effected in blocks of 512_{10} 16-bit words, called pages. Associated with each page of data is a pre-recorded drum address word, a programmable code word, and an integrity word. The appropriate generation, comparison, and/or verification of these three words preserves the integrity of all information transferred.

The DP is the only one of the four mini-computers in the LOGICON 2+2 System that is not microprogrammed. Its logic is hardwired and functionally organized into five sections; memory (main) interface; drum interface; buffer, which acts as an intermediary between memory and drum interfaces; and test, which handles the input/output requirements of the external test panel. Inter-processor communication with the Control Processor (CP) is accomplished through the control section. Proven TTL logic and MSI elements are used to achieve performance and high reliability. Extensive maintenance features are provided. High density packaging minimizes space requirements. Replacement modules are integrated circuits themselves.

The DP features direct main memory access for control words, thus requiring a minimum of real-time processor response for efficient operation. Control word look-ahead is employed to provide a contiguous drum sector transfer capability. Both mode (read/write) and track-to-track address changes may occur between contiguous sectors.

The DP will operate at a sustained transfer rate in and out of main memory of 1 million words per second; a burst rate of 2 million words per second is attainable. Single or dual memory access is available, and the two memories may be addressed simultaneously or sequentially. Operation with a variety of fixed-head drums is possible with capacities from one-half million to 16 million 8-bit bytes.

DP operation is initiated by receipt of an interrupt from the CP, causing the DP to access a 2-word Current State Cell (CSC) in main memory. The DP receives its operating instructions from the CP, and in turn, maintains a record of the current operating status, in this cell.

The DP may be directed to operate in any one of the four following states:

- INACTIVE --DP idle with all registers master-cleared.
- HALT --DP suspends all memory accesses until CP generates next interrupt; if DP detects error condition in its own operation, it will also go to this state.
- UPDATE --drum sector count mained in CSC, is updated as sector marks are physically encountered; DP goes automatically to this state at conclusion of RUN state (see below) or when interrupted by the CP while in RUN.
- RUN --DP processes first Drum Control Block (DCB) in main memory, pointed to by word two of the CSC; a DCB is a group of four words associated with each page of data to be transferred, and contains the address, integrity, and instructional information necessary to accomplish the transfer; the DCBs may be listed sequentially (up to 128 max) linked by pointer to the next; as each DCB is processed, the DP maintains in CSC an indication of its current operating state, the current drum sector count, a pointer to the last DCB serviced, and the retrieval fault status of that DCB. The DP interrupts the CP when the last DCB has been processed or when a data transfer

error is encountered for which the associated DCB directed that an interrupt be enabled.

Associated with each page of data that is transferred between main memory and the drum are two special-purpose words that are fundamental to the error detection process:

- Code Word — a software-defined "label" that may be used for page identification or linkage, or as a file key or check word. Word (2) in the DCB is devoted to the Code Word.

- Integrity Word — the 513th word stored with every page on the drum; it represents a computed check-sum over the 1024 half-words (8-bit bytes) of data; in the read mode, it is compared to an internally-generated check-sum; in the write mode, it may be either generated on-line or optionally pre-specified in word (3) of the DCB.

The information content of each DCB processed by the DP may be summarized as follows:

1. track and sector drum address coordinates

2. the seven (7) most significant bits of the core memory address; the low-order nine bits correspond sequentially to each of the 512 words in the page to be transferred.

3. a function code defining one of the eight possible read (R)/ write (W) operations to be performed in the RUN state; these codes, their meanings and functional implications, are summarized in Table 2-1.

4. interrupt enables — specifies for which class (u) of errors the DP is to generate an interrupt to the CP. Errors are of three classes: (1) Code Word compare errors, for which DP remains in RUN state, (2) non-code word errors requiring only an interrupt, (3) non-code word errors severe enough to require an interrupt and DP going into the HALT state.

5. DCB linkage — indicates last DCB or whether next DCB is listed sequentially or is pointed to in word 3 of current DCB.

TABLE 2-1. FUNCTION CODES

Function Code		Code Word			Integrity Word			Data Page		Comment
		R	Store	W	R	Store	W	R	W	
0	Bootload									Automatic HALT states
1	Read Code Word Only	•	DCB (word 3)							Compare with Code Word in DCB 2
2	Read Data & Code Words	•	DCB 3 if in error		Check			•		Compare with Code Word in DCB 2
3	Read Data, Code & Integrity Words	•	DCB 2		Check	DCB 3		•		Compare with Code Word in DCB 2
4	Write Code Word Only			from DCB 2			"0" data		"0" data	
5	Write Data & Code Word			from DCB 2			gener-ates		•	
6	Write Data & Code Word			from DCB 2			gener-ates		•	HALT on Class 2 or 3 error
7	Write Data, Code & Integrity Words			from DCB 2			from DCB 3		•	(1) As above (2) generate and check integ. word

When the DP concludes processing of a particular DCB it sets the status flags in word (0) of the DCB indicating that the DCB has been serviced and whether Code Word or other error conditions have occurred. Where "other" (non-code word) errors have been detected, indicators are set in word 3 of the DCB specifying the particular class 2 or class 3 error condition encountered.

DP INTERFACE SECTIONS

The DP is functionally divided into sections (Figure 2-1). The following paragraphs discuss each section separately.

Memory Section (MIS)

The MIS interfaces directly with the (core) memory (ies) of the computer system. The initial design accommodates the 2+2 System memory interface. The basic design considerations include a simple interface with the Buffer and Central Control sections of the DP. Thus, other MIS's may be designed to accommodate other computer systems with minimal redesign of other sections of the DP. All MIS's will satisfy the following requirements.

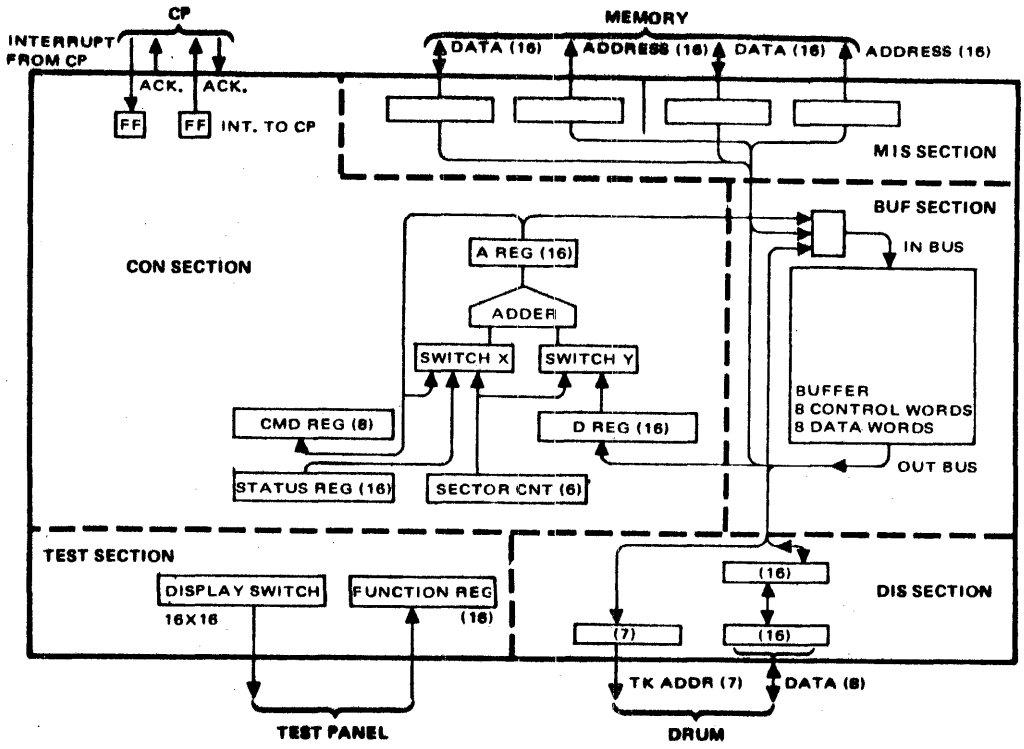


Figure 2-1. Drum Processor Functional Interface

1. The MIS is informed of the type memory access required and the information direction (to/from) the Buffer.

2. Where appropriate, memory address is provided from the Buffer. When no address is provided, the MIS uses the internally stored memory address specified.

3. The MIS must buffer the data word being transmitted/ received to/from the memory.

4. The MIS must request data transfer to/from the Buffer Section. Also, it must control all memory access requests to obtain maximum efficiency for data transfer. Request is made via CON.

5. All address and data are supplied via a single (parallel) bus to the MIS from the Buffer. All data is sent from the MIS to the Buffer via a single (paralleled) bus.

6. The MIS interfaces with two asynchronous sections. The Memory interface must operate ≥ 2 MHZ word rate. The Buffer interface at ≥ 10MHZ byte rate.

Control Section (CON)

The CON section interfaces with all other sections (MIS, DIS, BUF, and CPI). The purpose of the CON is to direct control information retrieval, interrogation, and update. Once data transfer is initiated between the MIS and DIS the CON basically monitors the operation for purposes of integrity, checking and BUF address selection until:

1. the data transfer activity completes,

2. an abnormal condition occurs, or

3. a halt is received via the CPI

The CON section design is based on the DCB & CSC formats for the 2+2 System. It is basically independent of the drum type used.

The CON is designed to satisfy the following requirements.

1. To command MIS regarding type of memory access required and initial address to be used. The MIS assumes the same type access and sequential address access until another command is received.

2. To command DIS regarding type of drum access required.

3. To receive and respond to control sequence requests from the DIS (formulate status words, set BUF access location, etc.).

4. To respond to CPI to initiate, suspend, or halt LDC operations. Also, formulate interrupt, when required for CPI execution.

Buffer Section (BUF)

The BUF interfaces with the MIS, DIS, and CON sections. Its obvious purpose is to buffer control and general data information. The initial design accommodates sixteen 16-bit words and includes a simple interface between the sections mentioned. Basic design considerations include modularity concepts for an 8-, 16-, 24-, and 32-bit word (or byte) format. The BUF is designed to satisfy the following requirements.

1. The BUF must operate at a rate $\geq$ 5 MHZ (request received to transfer complete cycle). A design objective is about 10 MHZ.

2. All access requests shall be from CON. Input data source (MIS, DIS, CON) selection are provided by CON. Output data may be placed on a common bus.

3. Control data locations are provided by CON. General data buffer locations are accessed by internal BUF control using a FIFO algorithm. Detection logic must be provided for both empty and full buffer (general data) cases.

Drum Interface Section (DIS)

The DIS interfaces directly with the digital interface of the drum device. The initial design accommodates the VRC-1016, VRC-1032, and VRC-2032 drum devices. The basic design considerations include a simple interface with the BUF and CON sections of the DP. Thus, other DIS's may be designed to accommodate other drum devices, or multiple drums, with minimal redesign of other sections of the DP. All DIS's will satisfy the following requirements.

1. The DIS is informed of the type drum access required by the CON.

2. The appropriate drum (track) address is provided from the Buffer.

3. The DIS must buffer data being transmitted to the drum.

4. The DIS must request data transfer to/from the Buffer. Also its control must be designed to allow for maximum delays between request and completion of data transfer with the Buffer. Data transfer requests are made via the CON.

5. All address and data is supplied via a single (parallel) bus to the DIS from the Buffer. All data is sent from the DIS to the Buffer via a single (paralleled) bus.

6. The DIS must be format sensitive in that it can detect when an event will occur relative to the recorded clock track count (e.g., address and code word location, integrity word location).

7. The DIS must respond to the drum as a synchronous device, which is controlling the system. Therefore, particular attention is required to assure that the DIS (and rest of the DP) can maintain data and control information at the established synchronous rate. The maximum synchronous rate for the DIS design is ≥4.0 MHZ clock rate.

8. All preambles and postambles are generated within the DIS.

9. The DIS requests track address according to its needs.

10. The DIS detects if the control information received (transfer, address, access mode) has been made available at the required time. If not, the DIS protects the recorded information (on drum) from being disturbed.

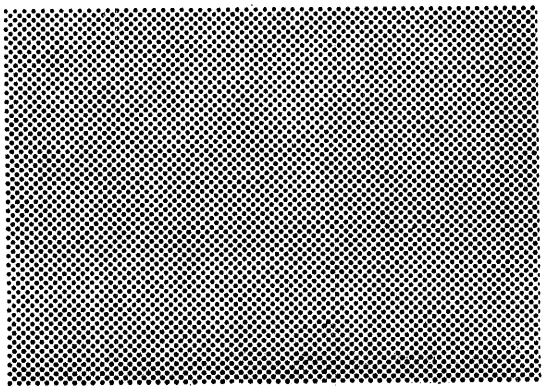
DRUM SUBSYSTEM

The drum subsystem consists of a Vermont Research drum of 1, 2, 4, or 8 million words, and a Logicon designed and built drum controller. The drum sizes are as follows:

	Model Number			
	1016	1032	2032	2064
Sectors	32	32	64	64
Track Sets	64	128	128	256
Total Pages	2048	4096	8192	16384
Rotation time	17 ms	17 ms	35 ms	35 ms

SWAPPING STORAGE

Swapping Storage consists of a drum built by Vermont Research Corporation, and a drum controller designed and built by Logicon. The drum holds 2^{20}, 2^{21}, 2^{22}, or 2^{23} words (approximately 1, 2, 4, or 8 million words) of 16 bits each, organized in 512 word pages, with an average access time of 8.7 milliseconds (1 and 2 million word drums) or 17.4 milliseconds (4 and 8 million word drums) and a transfer rate in or out of CP memory of approximately 1 million words per second.



III...

Operational Characteristics

GENERAL

The DP functions that require program preparation and have programming implications when using the DP are discussed in this section. The programmer is considered as a "System Programmer"; meaning one thoroughly knowledgeable about the 2+2 System executive functions and interactions. The system programmer is also one who is authorized to develop and perform modifications to portions of the 2+2 System executive functions.

The DP functions requiring program preparation are:

- DP State Commands
- CP interrupt generation
- DP Data Control Blocks (DCB's)

Implied for 2+2 System operation, but not required by the DP, are the programs to service the DP generated interrupts.

Other functions particular to the DP and drum subsystem are used by diagnostic programs. Design details of the DP operating characteristics are required to develop such programs.

DP CONTROL COMMANDS

The DP recognizes four operating states. Of these only three are considered available to the system programmer. The fourth is used by the diagnostic programs.

The basic DP design concept is that all current information will be preserved until forced to change, either by normal sequence of

operation or by programmed commands. Thus two levels of information interrogation are available:

1. Core resident control information

2. Internal DP buffered information

The former (1) is directly accessible by program. The latter (2) is visually observable through the DP test panel.

The DP's four operating states are:

1. RUN

2. UPDATE

3. HALT

Ø INACTIVE

The DP state is established by the program as follows:

- Insertion of the required state into CSCØ
- Generation of an interrupt to the DP from the CP

The DP responds to the interrupt by:

- interrogating the CSCØ and the associated control command.
- acknowledging the CP generated interrupt after attempting to establish the requested state.
- proceeding to operate in the resultant state.

RUN State

This command will start the DP. The DP will access CSC 1 for pointer (address) of first DCB in memory. This DCB will be read from memory and initiated. Further DCB's will be controlled by DCB linkage of each individual DCB.

NOTE: For a guaranteed start on this revolution of the drum, a RUN command must be given for drum address ≥ current drum address plus 3 sectors. Also note that the DP will MASTER CLEAR all internal registers upon receiving the CP interrupt whose action subsequently results in the RUN state.

UPDATE State

The DP shall update CSCØ with the current (physical) drum sector count as each sector is encountered. No data transfer occurs except the single word update of CSCØ. Normally when the DP terminates a RUN state it will automatically establish the UPDATE state mode of operation.

HALT State

The DP shall cease all memory accesses until an interrupt is received from the CP. The contents of the DP internal registers will not be disturbed when this state is achieved by DP internal action (i.e. fault detected). When the CP generates an interrupt the DP resets all internal registers. Any CP generated interrupt may be lost if presented during the first 10 μs after the DP starts an internal MASTER CLEAR function. Upon completion the DP assumes the HALT state and will respond to a CP generated interrupt.

INACTIVE State

The DP is not presently active. The cell may have been cleared by the program without a HALT function.

CURRENT STATE CELL (CSC) STRUCTURE

Through the CSC the program can determine the current state of the DP. The following information is presented:

- Current drum sector (physical rotational position)
- Current DP operating state (run, update, halt, master clear, or inactive).
- Current DCB state
- Pointer to last DCB serviced

The drum rotation shall result in contiguously incrementing sector address within the current configuration limits. In the RUN and UPDATE state, the sector number will be automatically updated by the DP. The

DP never reads the sector number from CSCØ. The current DP operating state is updated by the DP.

- Every sector - RUN or UPDATE state
- Once - HALT state

Program access to the current DP state field is required in all but one case when a change of state is planned. When the DP is in RUN mode and an interrupt is received from the CP, the DP will always assume an UPDATE state. The DP will not access CSCØ in this case but will generate an interrupt to the CIOP.

For all other cases it is recommended that CSCØ be examined by program after the DP responds (via interrupt acknowledge sent to the CP). It is possible in the UPDATE state for the DP to update CSCØ after a new state has been sent by program but before the DP receives the CP interrupt causing a Store then Interrupt sequence. The DP may respond to an interrupt immediately (e.g., $< 1\ \mu s$) thus there is no guaranteed delay on the DP's part before it accesses memory for CSCØ.

The current CSCØ state reflects access to the current DCB. When the DCB is successfully retrieved, the respective status bit will be set at the time of normal CSCØ and 1 update. If the DCB access is unsuccessful, the nature of the fault encountered will be indicated and the DP will terminate operation with a HALT state; and an interrupt will be sent to the CP. The DP internally stored information will not be disturbed and is accessible through the DP test panel.

The address of the last DCBØ serviced is identified via the contents of CSC1. However, during initiation of the RUN state, the pointer will be set to zero during the first CSC1 update.

INTEGRITY WORD

The purpose of the integrity word is to provide a method for verification of data integrity during data transfer between storage media. Each 512 word page written on the drum has an integrity word written with it as the 513th word. The integrity word is the sum of the 1024 half-words of data. (Appendix A7 integrity word algorithm.)

The integrity word is normally generated and written into the drum by the DP for write function codes 4, 5, and 6. (Code 4 write code word only, Code 5 write data and code word, Code 6 write data and code word halt on error.)

An integrity word is generated and compared against the one read/ provided by the DP for function codes 2, 3, and 7 (Code 2 read data and code word, Code 2 read data code word and integrity word, Code 7 write data, code word and integrity word halt on error provided).

The capability of transferring the integrity word with a page is possible with function Code 3 (read data, code word and integrity word) and function Code 7 (write data, code word and integrity word halt on error).

One usage of the integrity word in file storage manipulation is to transfer a 512_{10} word data page with integrity word to other storage media, such as a disk file storage unit, without recomputing the integrity word. This page could then be read from the disk file and written on the drum with the related integrity word for this page still in tact. Thus, any loss of information during transfer will have an automatic check proceeding with it. When this data page is written onto the drum, the computer would get an integrity word compare error from the DP, if one exists.

CODE WORD

The code word is a software header or label for each page. Its meaning is a software function and can be defined by the system programmer. It is provided in the DP to allow an extra check on DP drum and software operation. It might be used, for example, to label each page by the user number to which the page is assigned.

The code word can be read or written without a data page being transferred to/from core memory.

SPECIAL PROGRAMMING PRECAUTIONS

Last DCB List Termination

If the programmer wishes to terminate a list of DCB's which are in continual operation, without generating an interrupt, he may inspect CSC1 for a pointer to the last completed DCB (n). A last DCB flag may be inserted in DCB (n + 2) or greater.

Initiated DCB With Serviced Flag Set

If the DP receives a DCB with the serviced flag set, the DP will halt and send an interrupt to the CP. Status information will be set into CSCØ bit 2.

Interrupt Timing

A special note about interrupt timing. It is possible for an interrupt to occur every 456 μ seconds from the DP. The interrupt will occur at the end of the sector generating the interrupt condition.

Contiguous Sectors

The DP is capable of switching modes (read vs write) between contiguous sectors. The DP can also address contiguous sectors independent of track address.

Contiguous sectors operation can only be employed in chaining of DCB's in a list driven structure. Conditions which cause the DP to assume UPDATE or HALT mode for each sector will result in at least one sector of inactivity between UPDATE/HALT and RUN mode.

Boot Mode Precaution

Boot mode will use track Ø sector Ø. This function may be used for manual or automatic recovery of the system. When the BOOT MODE switch is activated, track Ø sector Ø (512 words of data) will be transferred to memory addresses Ø through 511_{10}. Upon completion, an interrupt will be sent to the CP.

CP Interrupt Precaution

When the DP is in the RUN mode, a CP generated interrupt will cause the DP to automatically assume the UPDATE state upon completion of its current DCB activity.

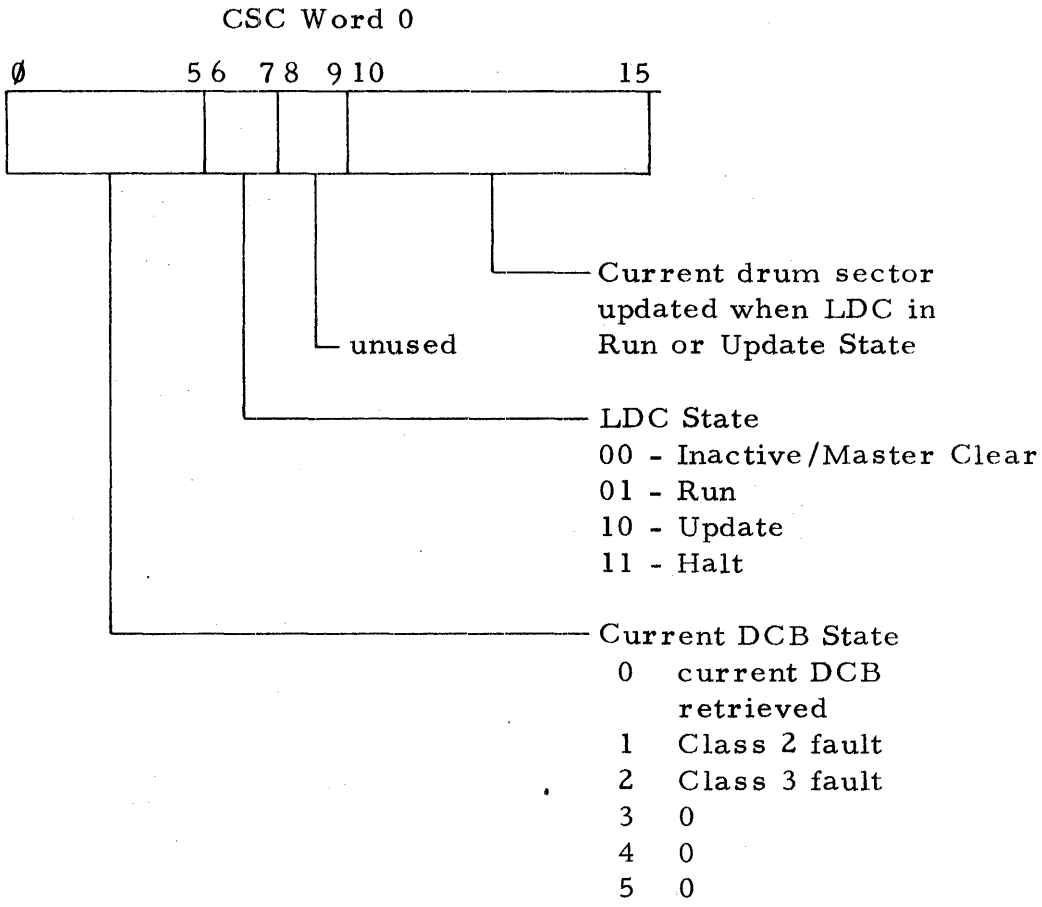
DCB List Structure

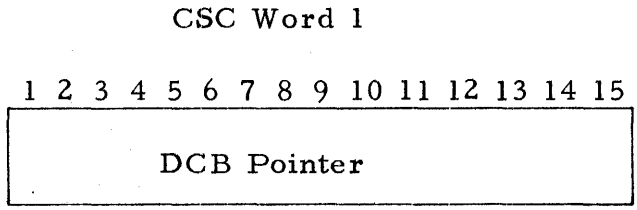
When the DP is operating from a list of DCB's, the software must take care that it stays ahead of the DP. One example would be to have a done interrupt enabled from the DP at a known location in the list of DCB's. The programmer would then check to make sure that the next group of DCB's is ready for the DP to process.

DCB Memory Location Error

Since the DP will not access sequentially beyond the 511 cell of any Ø modulo 512 block, the valid range of addresses to start a DCB (four words) are addresses ØØØ through $5Ø8_{10}$ of any 512_{10} word page in memory. A DCB cannot overlap two pages in memory. If the DCB is placed in core where it will overlap two pages of memory an interrupt will be generated as a result of the improper DCB command.

DESCRIPTION OF CURRENT STATE CELLS (CSC)





The CSC are two fixed memory locations in the first 0 - 511_{10} memory cells, the location of the CSC is manually selectable by hardware switches.

The CSC is used to provide the program with the following:

1. DP state

   - 00 - Inactive - DP master cleared
   - 01 - Run - DP processing DCB's
   - 10 - Update - DP is updating current drum sector in CSC word 0 bits 10 - 15 (for sector count $\leq 63_8$ max.)
   - 11 - Halt - LDC stopped

2. Current drum sector position

   For the initial configuration (Section 3.1) each addressable track location is divided into 32 physical sectors. The sectors are identified by 32 sector clocks recorded on a special track. During each revolution of the drum, each of the 32 sectors are in a position to be accessed once. The current drum sector position of CSCØ tells the program which sector the drum is at at any given time. CSC + 3 sector would give the program best access time, CSC + 31 to CSC + 2 could give the program the worst access, 17.4 to 19.1 milliseconds.

3. The current DCB state indicators are set as follows by the DP.

   - Bit Ø - When a new DCB has been retrieved successfully by the DP.
   - Bit 1 - A class 2 type fault (Section 3.3.5.1) occurred during access to the current DCB.
   - Bit 2 - A class 3 type fault (Section 3.3.5) occurred during access to the current DCB. This includes the following DCB Ø if the current DCB is not the last one.

   NOTE: If bit 0 and bits 1 or 2 are set, the problem has occurred while trying to update the last DCB retrieved after servicing it or getting the next DCB Ø.

4. CSC 1 DCB Pointer (pointer to last DCB completed).

   This tells the program which DCB is the latest one completed by the DP.

CSC 1 is also used to provide the DP with a pointer to the first DCB to be initiated for the start command.

CSC 1 pointer to DCB has different meaning depending upon the CSC Ø current state designator present code and its previous code. The following is a list of the different meanings.

- When CSC Ø in UPDATE or HALT state (1Ø, 11) and was previously in the RUN (Ø1) mode CSC 1 contains pointer to the last DCB serviced.
- CSCØ in RUN state (Ø1) and when the DP was previously in another mode, CSC 1 is set to Ø until the first DCB is serviced. (See Appendix A9.)

NOTE (1)

Any interrupts to the processor will be generated after CSC 1 is updated by the DP.

NOTE (2)

The interrupt routine by looking at the DCB pointed to by CSC 1 can determine which page of data or what activity was occurring when the interrupt occurred.

DESCRIPTION OF DRUM CONTROL BLOCK (DCB)

The DCB contains all command information needed by the DP to process any one of the six function codes.

The DP will access core directly for the command information stored in the DCB.

The DCB will also, after being serviced by the DP, contain all status information resulting from errors. Each DCB command will be for one sector only.

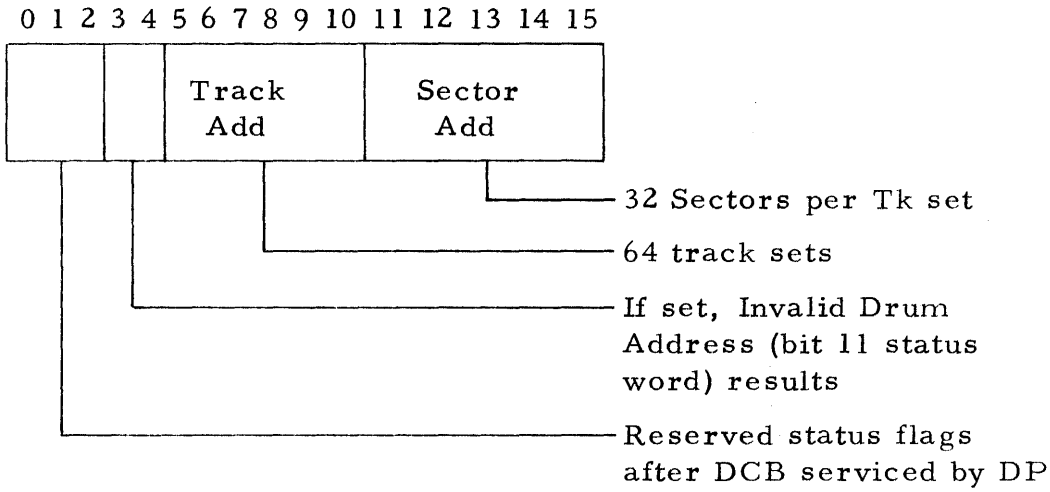
DCB 0 Bits 4 through 15 (Drum Addresses)

DCB word 0 contains the drum address. It will be compared with a pre-recorded address on the drum prior to commencing execution of the

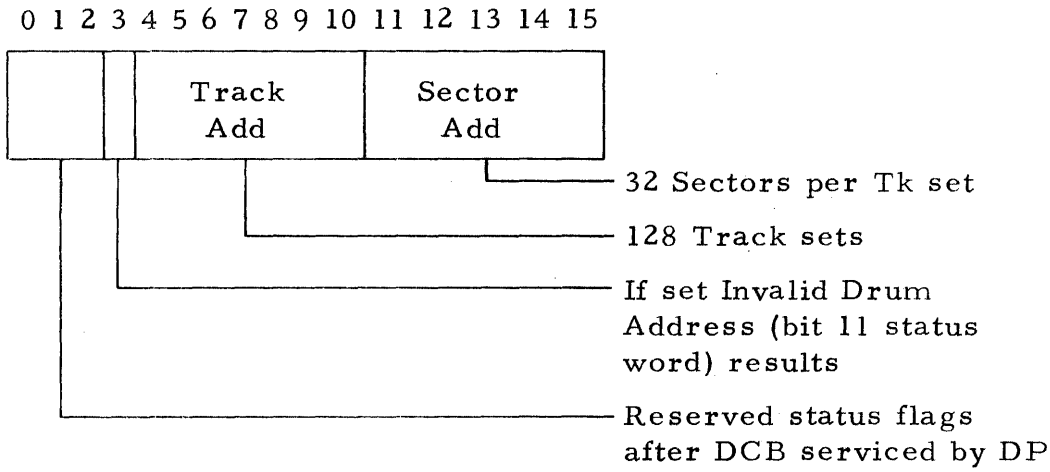
function code activity specified. For the initial configuration (Drum 1016) bits 11 through 15 contain the sector address 0 through 31. The sector is a physical location on the drum. Each revolution of the drum will pass by each of the 32 sectors.

DCB word 0 (Drum 1016) bit 5 through 10 contain the track address (0-63). As a sector becomes physically available, any track of the 64 can be accessed for that sector. Drums 1032 and 2032 follow the same pattern with larger address fields as shown below.

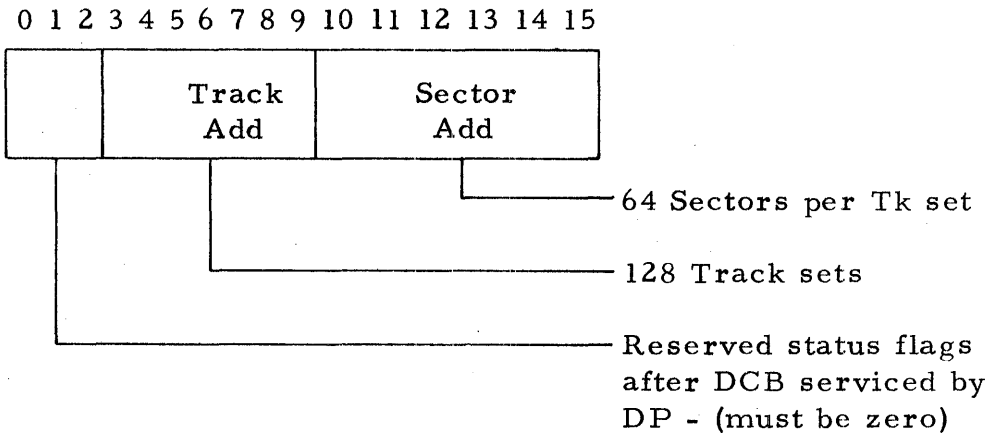
DCB Word Ø for Drum 1016



DCB Word Ø for Drum 1032

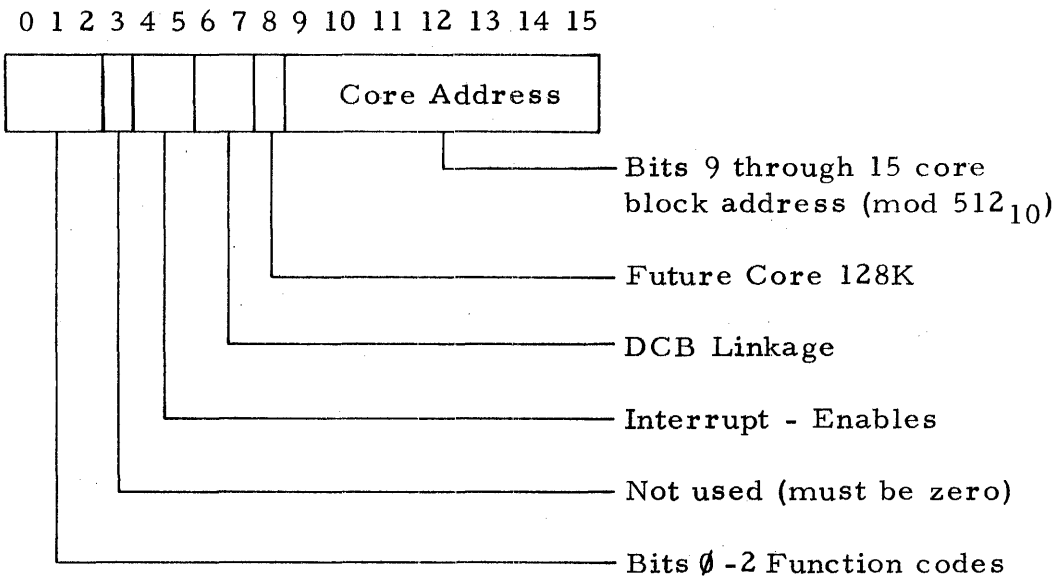


DCB Word Ø for Drum 2032



DCB 1 bits Ø Through 2 Function Codes

DCB Word 1



Function Code. Ø Bootload (not programmable). If supplied improper DCB error flag is set in DP causing class 3 fault bit (2) of CSC Ø to be set. DP assumes HALT state when initiated via Bootload action. The DCB is serviced as the last DCB with an interrupt to the CP resulting.

Function Code 1. Read Code Word Only (Compare Code Word)

1. Track and sector address read off of drum. Drum address read from drum compared to DCB drum address requested.

- Address Compare OK: Proceed to (2).

- No address Compare Error: Set invalid drum address status bit 11, proceed to (3).

2. Read Code Word: Code word read from drum placed into DCB 3 (within LDC). DCB 2 (drum control block code word) compared with DCB 3 (code word read from drum).

   - Code Word Compare OK: Proceed to (3).

   - Code Word Compare Error: Set code word check error status bit 1 and DCB Ø bit 1 of serviced DCB, then proceed to (3).

3. DCB Linkage: Bit Ø of DCB Ø of serviced DCB set to indicate this DCB complete. Also upon completion, the code word is in the DCB 3 (read mode only) unless other faults (class 2 or 3) have occurred. In latter case DCB 3 contains status word.

NOTE

No data is transferred and the integrity word is not checked for read code word only function.

Function Code 2. Read Data and Code Word. (Compare Code Word and Check Integrity Word):

1. Read Track and Sector - Read off of drum. Drum address read from drum compared to DCB drum address requested.

   - Address Compare OK: Proceed to (2).

   - No Address Compare Error: Set invalid drum address status bit 11, proceed to (4).

2. Read Code Word: Code word read from drum placed into DCB 3 (within DP). DCB 2 (drum control block code word) compared with DCB 3 (code word read from drum).

   - Code Word Compare OK: Proceed to (3).

   - Code Word Compare Error: Set code word check error status bit 1 and DCB Ø bit 1 of serviced DCB, then proceed to (3).

3. Read Data: Read 512_{10} data words from drum to computer memory. As the 512_{10} words are read from the drum, each byte of data is added to form a full word check-sum. If at any time during the reading of the 512_{10} data words, the drum transfer rate exceeds the rate computer memory will accept the data a transfer timing error occurs. The transfer timing error bit 3 of status word will be set. If a timing error occurs, zeros will be transferred to memory for all remaining words. Further generation of the integrity will be stopped.

   The integrity word read from the drum is then compared to the integrity word generated by the DP during read.

   - Integrity Word Compare OK: Proceed to (4).

   - Integrity Word Compare Error: Set integrity word compare error (bit 4) of status word, then proceed to (4).

4. DCB Linkage: Bit Ø of DCB Ø of serviced DCB set to indicate this DCB complete. Also upon completion, the code word is in the DCB 3 (read mode only) unless other faults (class 2 or 3) have occurred. In latter case DCB 3 contains status word.

NOTE

No data is transferred and the integrity word is not checked for read code word only function.

Function Code 3. Read Data, Code Word, and Integrity Word (Compare Code Word and Check Integrity).

1. Read Track and Sector: Read off of drum. Drum address read from drum compared to DCB drum address requested.

   - Address Compare OK: Proceed to (2).

   - No Address Compare Error: Set invalid drum address status bit 11, proceed to (5).

2. Read Code Word: Code word read from drum placed into DCB 3 (within DP). DCB 2 (drum control block code word) compared with DCB 3 (code word read from drum).

   - Code Word Compare OK: Proceed to (3).

   - Code Word Compare Error: Set code word check error status bit 1 and DCB Ø bit 1 of serviced DCB, then proceed to (3).

3. Read Data: Read 512_{10} data words from drum to computer memory. As the 512_{10} words are read from the drum, each byte of data as added to form a full word check-sum. If at any time during the reading of the 512_{10} data words, the drum transfer rate exceeds the rate computer memory will accept the data a transfer timing error occurs. The transfer timing error bit 3 of status word will be set. If a timing error occurs, zeros will be transferred to memory for all remaining words. Further generation of the integrity will be stopped.

   The integrity word read from the drum is then compared to the integrity word generated by the DP during read.

4. Save Code Word and Integrity Word: DCB 2 equals code word read from drum. DCB 3 equals integrity word read from drum provided it does compare with the integrity word generated (see NOTE in 5).

5. DCB Linkage: Bit Ø of DCB Ø of serviced DCB set indicate this DCB complete. Also upon completion, the integrity word is in the DCB 3 (read mode only) unless other faults (class 2 or 3) have occurred. In latter case DCB 3 contains status word.

NOTE

DCB 3 equal to integrity word only if DCB Ø bit 2 (other condition flag) clear.

DCB 3 equal to status word if DCB Ø bit 2 (other condition flag) set.

DCB 2 is normally equal to code word supplied (functions 1, 2, 4, 5, 6, 7). However, with function code 3, after code words have been compared, the code word read from the drum is placed into DCB 2 whether they match or not.

Function Code 4. Write Code Word Only

1. Read Track and Sector: Read off of drum. Drum address read from drum compared to DCB drum address requested.

   - Address Compare OK: Proceed to (2).

   - No Address Compare Error: Set invalid drum address status bit 11, proceed to (5).

2. Write code word on drum as received from DCB 2 being serviced.

3. Write 512_{10} words of zeros on drum with no memory accesses made.

4. Write LDC generated integrity word onto drum.

5. DCB Linkage: Set bit Ø, DCB Ø of serviced DCB to indicate this DCB is complete.

Function Code 5. Write Data and Code Word

1. Read Track and Sector: Read off of drum. Drum address read from drum compared to DCB drum address requested.

   - Address Compare OK: Proceed to (2).

   - No Address Compare Error: Set invalid drum address status bit 11, proceed to (4).

2. Write Code Word: Write code word on drum as received from DCB 2 being serviced.

3. Write Data: Write 512_{10} words of data onto the drum as received from memory.

   If at any time during the writing of the 512_{10} data words the drum transfer rate exceeds the rate the computer memory can supply the data, a transfer timing error occurs. The transfer timing error bit (3) of the status word will be set to one. At the point of writing a page that a timing error occurs the DP writes zero's onto the drum for the remaining words, no further memory accesses are required after a timing error. After all 512_{10} words have been written an DP generated integrity word is written on the drum. If a timing error occurred the integrity word written will be invalid.

4. DCB Linkage: Same as Function Code 4 (5).

Function Code 6. Write Data and Code Word (Halt on Error).

This function code same as Function Code 5 except that this function will halt on all class 2 and 3 errors.

Function Code 7. Write Data, Code Word, and Integrity Word (Halt on Error).

1. Read Track and Sector: Read off of drum. Drum address read from drum compared to DCB drum address requested.

   - Address Compare OK: Proceed to (2).

   - No Address Compare Error: Set invalid drum address status bit 11, proceed to (5).

2. Write Code Word: Write code word on drum as received from DCB 2 being serviced.

3. Write Data: Write 512_{10} words of data onto the drum as received from memory.

4. Write Integrity Word: After all 512_{10} data words have been written, the integrity word received from DCB 3 is always written on the drum.

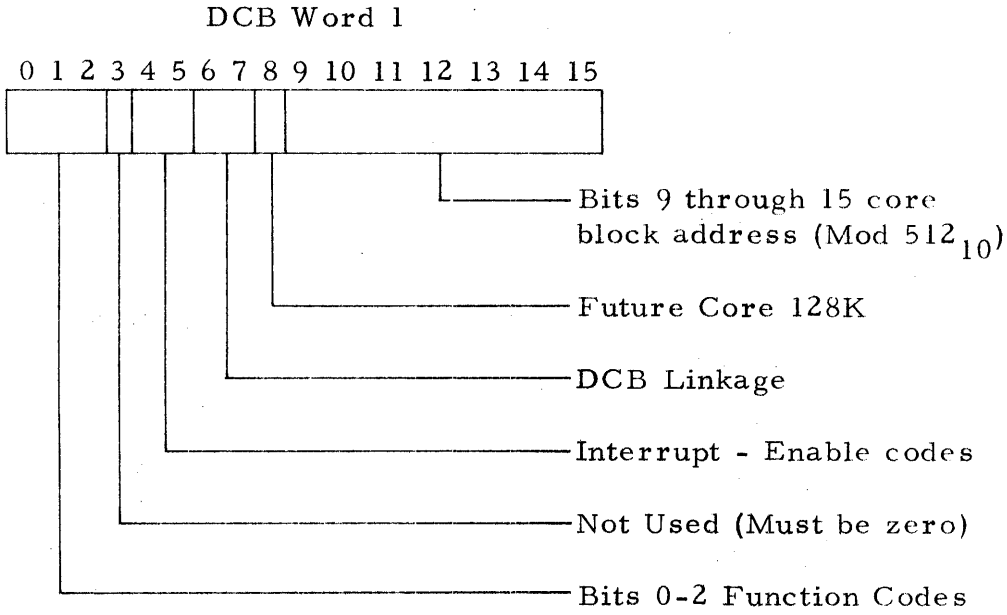
   The DP computes an integrity word during data write and compares it with the integrity word in DCB 3.

   INTEGRITY Word Compare OK: Proceed to (5).

   INTEGRITY Word Compare Error: Set integrity word compare error Bit (4) status word, then proceed to (5).

5. DCB Linkage: Set bit Ø, DCB Ø of serviced DCB to indicate this DCB is complete.

DCB 1 Bits 4 and 5. Interrupt Enables



Interrupt enables are used to inform the DP on how to handle interrupts for each individual DCB.

Interrupt Enable 0. Interrupt on all errors (class 1, 2, 3)

- Interrupt on data errors
- Interrupt on control errors
- Code word check error

Interrupt Enable 1. Interrupt on all errors or when done (class 1, 2, 3)

- Interrupt on data errors.
- Interrupt on control errors
- Code word check error
- Interrupt when this DCB is done

Interrupt Enable 2. Interrupt only on non-code word check error (class 2, 3).

- Interrupt on all status errors except code word check error.

DCB 1 DCB Linkage (Bits 6 and 7)

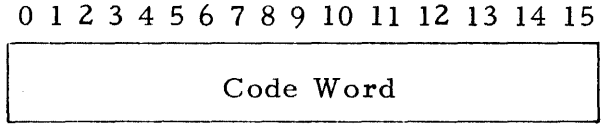
- DCB Linkage (0): Last DCB.
  Halt when done.
- DCB Linkage 1: Sequence DCB's:
  Proceed with next DCB in sequence.
- DCB Linkage 2: Link DCB:
  Next DCB Pointer in DCB 3.
- DCB Linkage 3: Not used:
  Decoded as illegal DCB.

DCB 1 Core Address (Bits 9 through 15)

The core address specifies the core page address (512_{10} contiguous words) to be read from or written into. The DP uses these 7 bits as the most significant bits of a 16-bit address. The DP initially puts zeros into the lower nine bits and starts transferring 512 words to/from the first word of the addressed page.

DCB 2 Code Word (Bits 0 through 15)

DCB Word 2

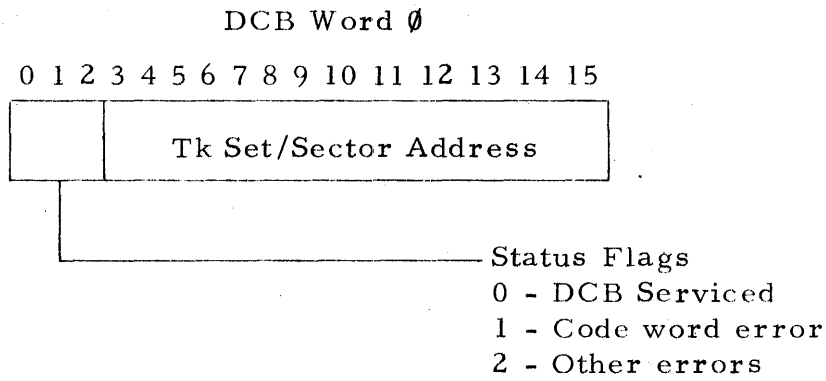


Code Word. The code word is a software function. The programmer may use it as a page identifier, page linkage, check word, file key, etc. During a write function, this word will be written on the drum with the associated page of data. During a read function, this word will be compared with that recorded with the addressed track and sector.

DCB 3 Special Information (Bits 0 through 15)

Function Code ≠ 7 and DCB 1, DCB Linkage = 2. Bits 0 through 15 contain pointer to next DCB.

DESCRIPTION OF DRUM CONTROL BLOCK (DCB) AFTER COMPLETION (Serviced by DP)



DCB Word Ø Serviced (Status Flags)

- Bit Ø DCB Serviced: DP has completed this DCB.
- Bit 1 Code Word Check Error: The DCB code word did not compare with the code word read from the drum.
- Bit 2: Other Error Conditions: This bit when set informs software that this DCB has some class 2 or 3 error conditions as identified in the status word (DCB 3).

  NOTE: When bits 1 and 2 are zeros, this DCB has been processed without error.

Drum Address

DCB Ø bits 3 through 15: Drum Address Track and Sector as Supplied.

DCB Word 1 Serviced (Function Code):

DCB Word 1

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Function Code	Core Address

Unchanged - As Supplied

DCB Word 2 Serviced (Code Word)

DCB Word 2

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Code Word

Write mode - As Supplied

Read mode function $\neq 3$ - as supplied. Read mode function = 3 - as read from drum.

DCB Word 3 Serviced (Status Word)

DCB Word 3

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Code, Integrity or Status Word

- DCB 3 normally loaded with code word read from drum during read functions.
- DCB 3 normally unchanged during write functions.
- DCB 3 equal to status only if DCB Ø bit 2 (other condition) flag set.
- DCB 3 equals integrity word read from drum if DCB Ø bit 2 (other condition flag) is clear and function code equal 3.

Interrupt Classes. The interrupt Classes are:

1. Class 1 Errors: Code word check error

   - Interrupt only on interrupt enable codes (DCB 1; bits 4, 5) equal to zero or one. Never changes DP state (RUN).

2. Class 2 Errors: Always generates interrupt to CP-7. DP assumes Halt state only if function code equals 6 or 7.

   - Transfer timing error
   - Integrity word compare error
   - Memory parity/write protect error
   - Data available late

3. Class 3 Errors: Always generates CP interrupt and assumes Halt state.

   - Improper DCB command
   - Memory time out
   - Invalid drum address
   - Drum not available
   - No drum response
   - Write inhibit set
   - Late control sequence

Other Conditions Flag Set (Bit 2, DCB 0)

NOTE

DCB 3 bits 0, 1 and 2 of status word have same meaning as bits 0, 1, and 2 of DCB 0 serviced DCB.

DCB 3 Status Bit 3 Transfer Timing Error. When, during transfer of data to or from the drum, the drums transfer rate exceeds the memory's transfer rate (plus buffer capacity) a loss of data has occurred.

DCB 3 Status Bit 4 Integrity Word Compare Error. The integrity word computed during data transfer did not compare with the integrity word accompanying the data (Function Codes Ø, 2, 3, 7).

DCB 3 Status Bit 5 Data Available Late Sequence. This error is received when data communications between the LDC and drum have failed. When this error occurs during write mode, there is no way of knowing what is written on the drum at the address of the failure. (Not to be confused with a Transfer Timing Error.)

DCB 3 Status Bit 6 Memory Parity/Write Protect Error. Data read from memory has a parity check. If data being read from memory by the DP has a parity error, this information is passed to the DP which sets this bit of the status word. The memory has a write protect option. If an attempt is made to write into a protected cell this bit will be set.

DCB 3 Status Bit 7, 8 Memory Error. Designates which memory has the error. Bits 7, 8 represents low order address bits (2^1, 2^0 respectively).

DCB 3 Status Bit 9 Memory Timeout. This error indicates communications between the DP and memory have failed or the DP has terminated memory accesses prematurely (i.e., next DCB address greater than current page).

DCB 3 Status Bit 10 Improper DCB Command. This error indicates that the DP could not translate this DCB into a legal instruction. Example: Function code 0 is translated in an improper DCB command, except during Bootland activity.

Function code 7 and DCB linkage equal 2 is an improper DCB command since DCB 3 cannot logically contain both the integrity word and a DCB link.

DCB 3 Status Bit 11 Invalid Drum Address (DCB Ø, Bits 3 - 15 Drum Address). No match for drum address found (DCB 0 Bits 3 - 15). Either a hardware failure has occurred, prohibiting the match or the given address is too large for the attached drum.

Drum Address Too Large:

Drum 1016 = Any addressing greater than track 63.

Drum 1032 = Any addressing greater than track 127.

Drum 2032 = No invalid drum address.

DCB 3 Status Bit 12 Drum Not Available. This status bit indicates the drum power may be off or the drum may be switched off line, rotation below speed limit, etc.

DCB 3 Status Bit 13 No Drum Response. Drum is available but does not respond to LDC commands (i.e., missing clocks, no response to internal commands, etc.).

DCB 3 Status Bit 14 Write Inhibit Set. This status bit indicates the write inhibit switch was set when a write function was initiated to the addressed track set.

DCB 3 Status Bit 15 Late Control Sequence. This status bit indicates the DP was late during a control sequence (i.e., late with the control function to switch to the write mode, did not complete Tk selection/ compare sequence in time).

INTEGRITY WORD ALGORITHM

DP Integrity Word (IW)

Basic equation: Checksum with end-around carry.

$$IW = \sum_{n=0}^{m} Bn + IV = \sum C^{x}$$

where

Bn = byte (n) value

m = max byte number

IV = initial value

C^{x} = carry out from bit x

For DP Configuration:

$m = (2W-1) = 1023_{10}$, W = words/sector = 512_{10}

$IV = 000377_{8}$ (for 16 bit IW)

x = bit '16

$C^{x} \geq 2^{16}$

Undetected errors occur only if $\sum$ Bn in error total $\pm (2^x - 1)$ of true value.

Repeating pattern errors require 2^x cycles in order to remain undetected. Since $2^x > 2^m$ no single repeating pattern error will go undetected (e.g., stuck "1" or "0" in byte data, logic).

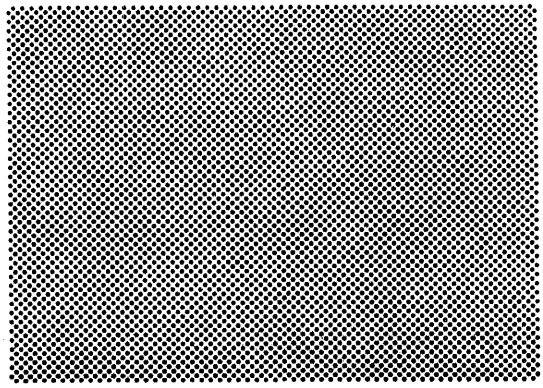
Range of IW values

$\sum$Bn (18 bits)	IV	$\sum C^x$	IW (16 bits)
-	-	-	000000*
000000_8	377_8	0	000377_8**
177400	377	0	177777
177401	377	1	000001
377377	377	1	177777
377400	377	2	000001
577376	377	2	177777
577377	377	3	000001
776000	377	3	776402***

*Invalid, cannot generate

**Min $\sum$ Bn : all 0's

***Max $\sum$ Bn : all 1's



Appendix **A. . .**

LOGICON 2+2 Drum Specification

Several sizes of drums are of interest. This Specification covers specifically the VRC 1016. By suitable changes of rotation speed, sectors/track, addressable track sets, and other figures derived from these, this Specification covers many of the drums in the VRC product line.

Mechanical and Electrical Interface	VRC Model 1016 (In accordance with VRC Bulletin DB-6808)
Options Required	• Eight track parallel read/write and address electronics. • Deskewing buffer for read operations. • Ability to pre-record addresses in guard band.
Rotation Speed (Nominal)	3450 RPM ± 2%
Sectors/Track	32
Addressable Track Sets (Eight Tracks Each)	64

Pre-Recorded Tracks

- Two bit clocks, ØA and ØB, 180° apart, width 1/3 bit time.
- Sector clock spans ØA symmetrically ± 24 ns, at intervals of 1104 ØA clock periods.
- Index clock spans ØA symmetrically ± 25 ns, once per revolution, coincident with a sector clock.

Read Clock:

During a read function when all tracks (8) have been synchronized (e.g., all preambles detected) and the first byte of information is available, a read clock will be generated. In the read mode there will be read clocks generated by the diskewing buffer for prerecorded track and sector address, the recorded code word, and all data bytes. There will be 1028 read clocks for the transfer of one 512_{10} word page. Each byte of information will be output from the diskewing buffer as parallel bits with the read clock entered within the data available period.

Data to be recorded in each sector in each track set (8 bits/byte)

- 48 byte guard band (allows for worst case skew, track address change, and read/write or write/read transition).
- 8 byte preamble
- 2 byte address
- 2 byte postamble

  } File Address Block

- 6 byte guard band (allows for worst case skew, plus read/write or write/off transition).
- 8 byte preamble
- 2 byte code word
- 1024 byte data page
- 2 byte integrity word
- 2 byte postamble

  } Data Block

Total Bytes/Sector in each track set	1104 bytes
Total Bytes/Drum	2,260,992
Total Data Page Bytes/Drum	2,097,152
Data Pages/Drum	2048
Total Bits/Track	35,328
Switching Times	Track address change plus read/write or write/read mode switching in less than 20 μ seconds. Read/write or write/off switching in less than 1 bit time.
Digital Interface	Drives 10 feet of interface cable (twisted pair or coax)
Write to read back relationship	Five bit times maximum shift (phase shift plus worst case combination of allowable +2 bit skew).
Modes of Operation	• Write file address block without disturbing data block. • Read file address block [Tk(t), sector (n)], read or write next contiguous position data block [Tk(t), sector (n + 1)]. Must be able to switch track after reading/writing data block [Tk(x) Sector (n)] before reading next address block [Tk(t), Sector (n + 1)].
Maximum Preamble/Postamble required by drum system	• 8 bit preamble 2 bit postamble
Bit Frequency (nominal)	2.03136 megahertz

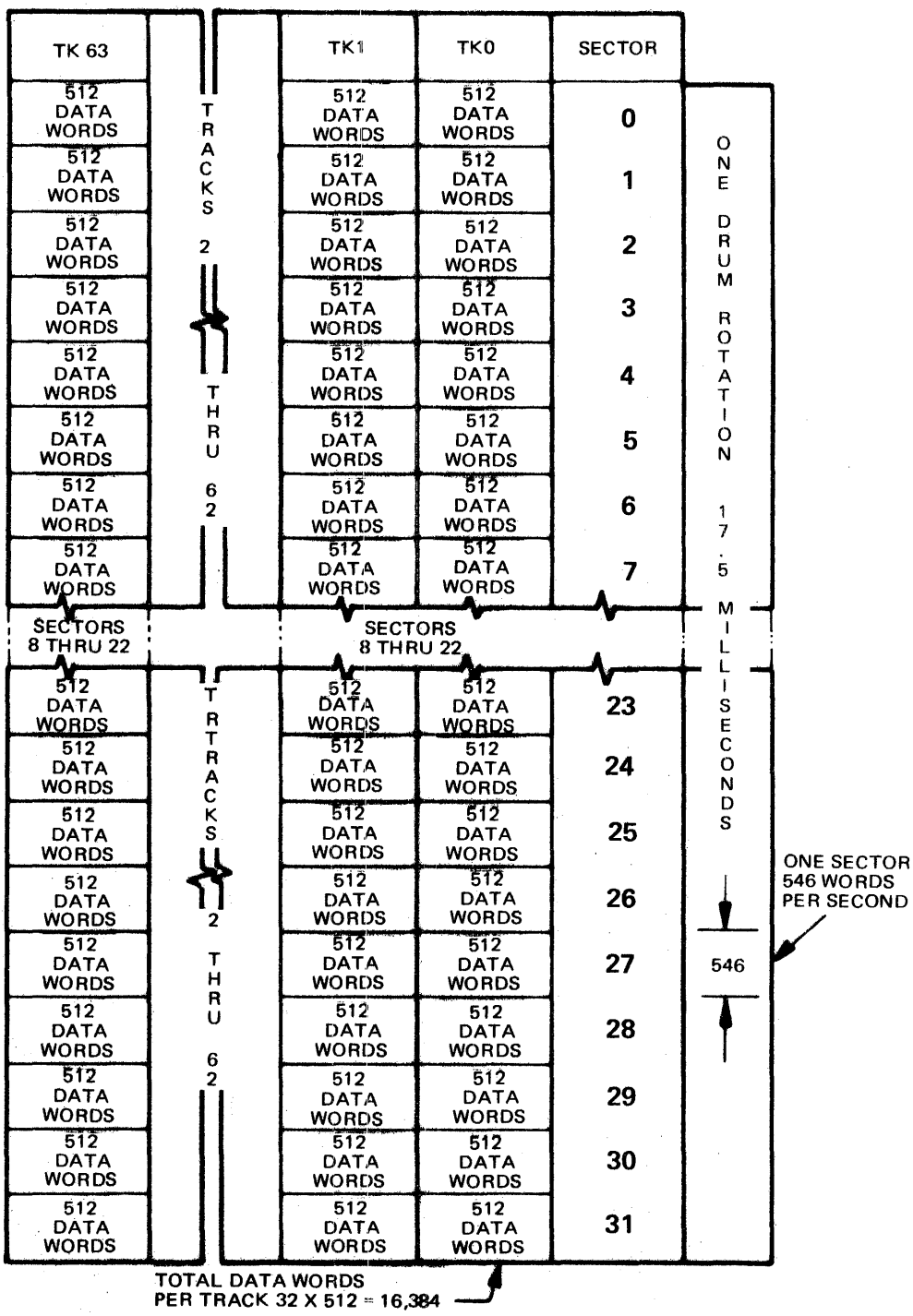
Byte Transfer Rate (nominal)	2.03136 megabytes/second during data page. 1.88416 bytes/second average/ sector.
Maximum Acceptable Recoverable (by single re-read) Error Rate	1 in 10^{11} bits transferred.
Maximum Tolerable Non-Recoverable Error Rate	1 in 10^{13} bits transferred.

APPENDIX B OVERALL DRUM IMAGE

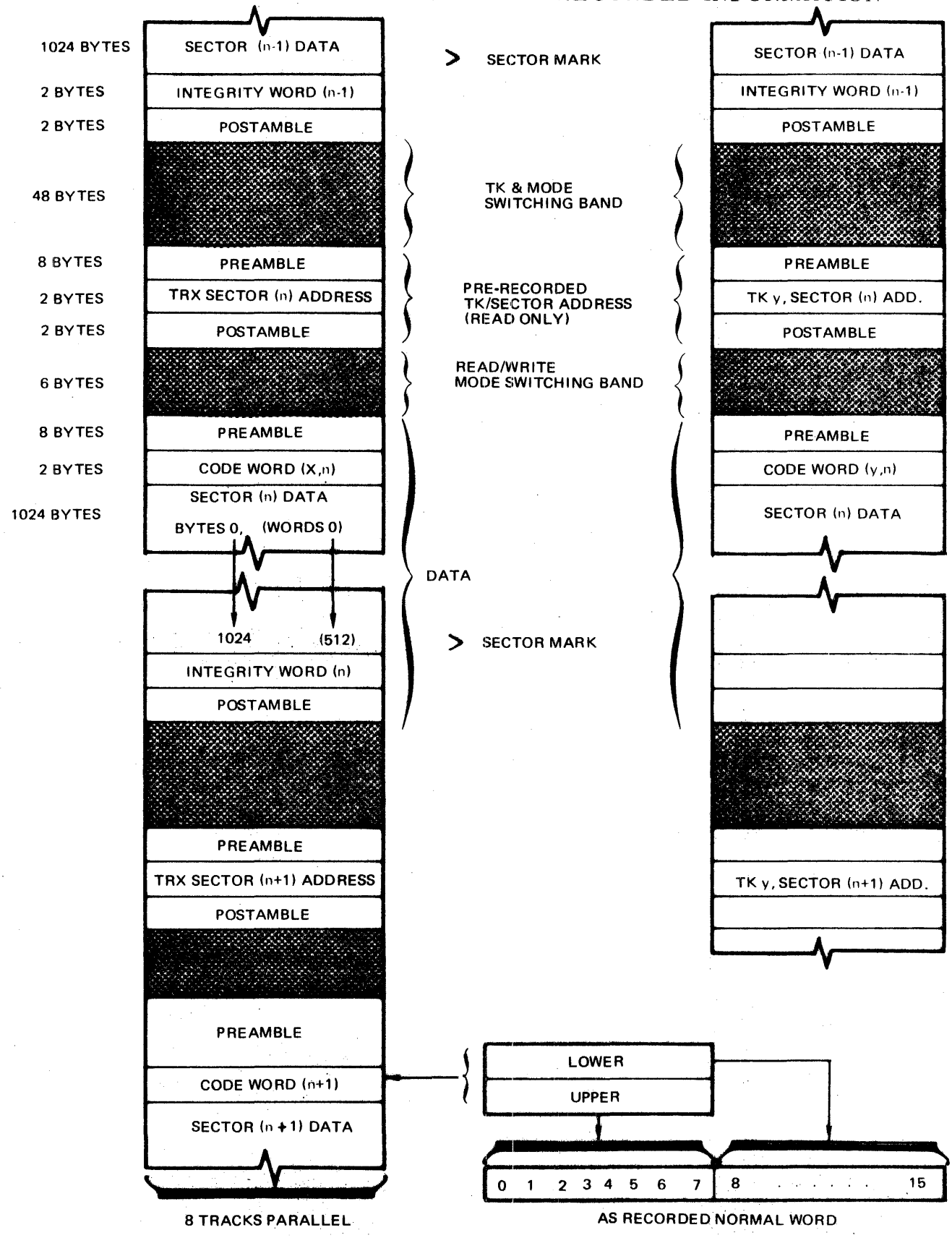
NOTE: Each 512 WORD BLOCK EQUALS 1 PAGE.

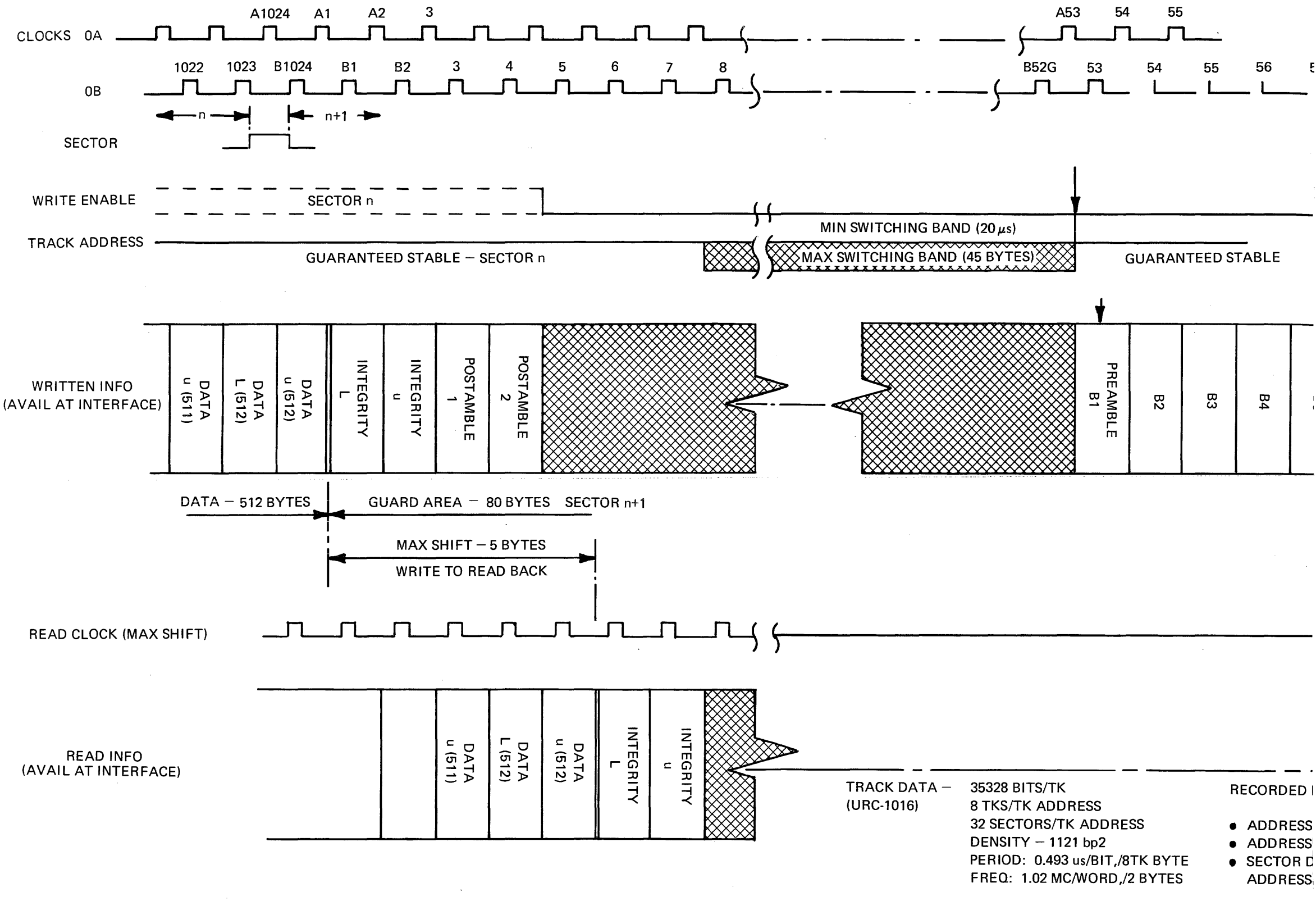
32 PAGES PER TK
64TK X 32 PAGES =
2048 PAGES PER
DRUM.

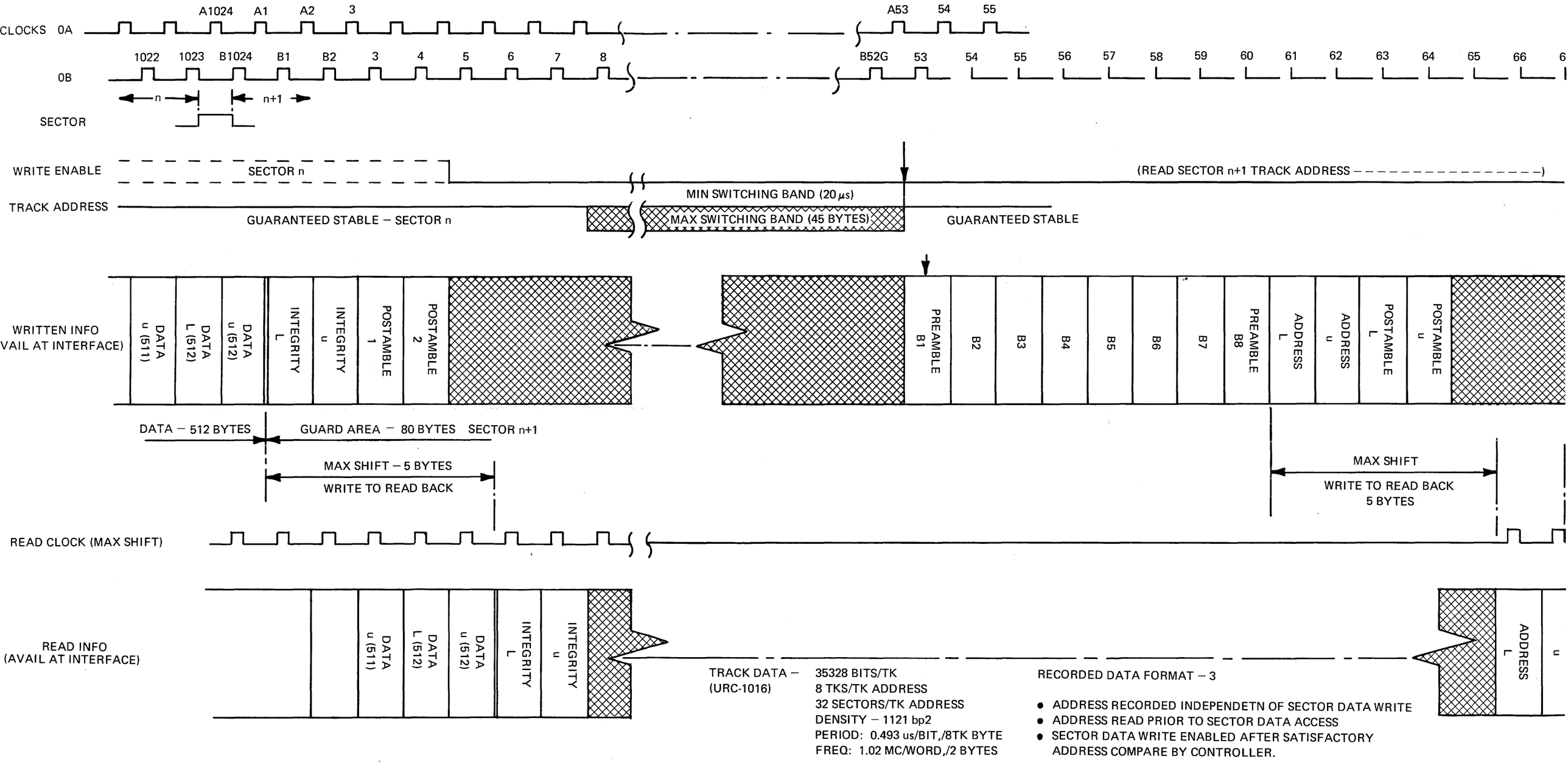
2048 PAGES X 512
DATA WORDS =
1,048,576
16BIT DATA WORDS
TOTAL DRUM
CAPACITY



APPENDIX C DRUM FORMAT -- RECORDED INFORMATION




CLOCKS 0A
A1024 A1 A2 3 A53 54 55
0B
1022 1023 B1024 B1 B2 3 4 5 6 7 8 B52G 53 54 55 56
n
n+1
SECTOR
WRITE ENABLE
SECTOR n
TRACK ADDRESS
MIN SWITCHING BAND (20 μs)
GUARANTEED STABLE – SECTOR n
MAX SWITCHING BAND (45 BYTES)
GUARANTEED STABLE
WRITTEN INFO
(AVAIL AT INTERFACE)
DATA u (511)
DATA L (512)
DATA u (512)
INTEGRITY L
INTEGRITY u
POSTAMBLE 1
POSTAMBLE 2
PREAMBLE B1
B2
B3
B4
DATA – 512 BYTES
GUARD AREA – 80 BYTES SECTOR n+1
MAX SHIFT – 5 BYTES
WRITE TO READ BACK
READ CLOCK (MAX SHIFT)
READ INFO
(AVAIL AT INTERFACE)
DATA u (511)
DATA L (512)
DATA u (512)
INTEGRITY L
INTEGRITY u
TRACK DATA –
(URC-1016)
35328 BITS/TK
8 TKS/TK ADDRESS
32 SECTORS/TK ADDRESS
DENSITY – 1121 bp2
PERIOD: 0.493 us/BIT,/8TK BYTE
FREQ: 1.02 MC/WORD,/2 BYTES
RECORDED
• ADDRESS
• ADDRESS
• SECTOR D
ADDRESS

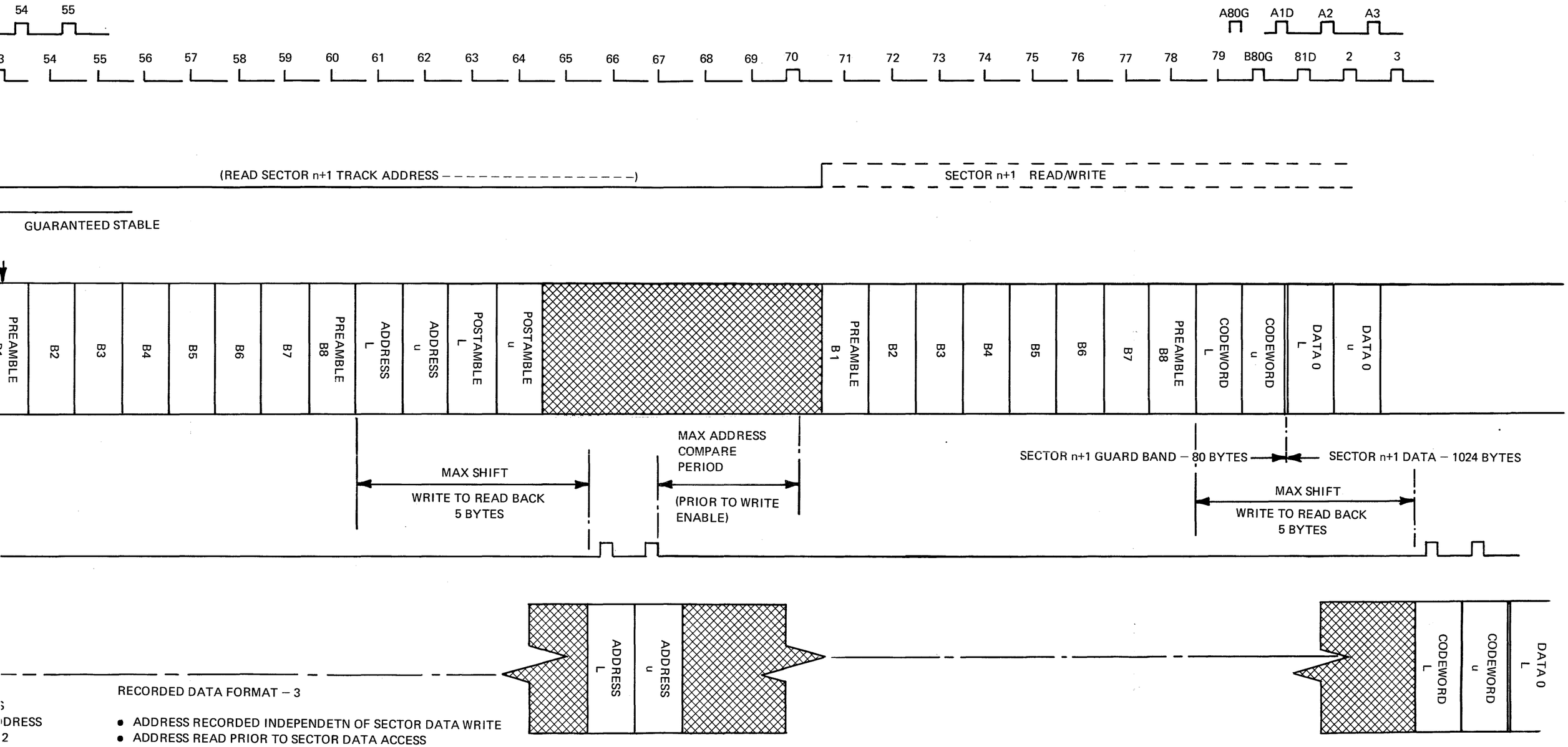


TRACK DATA – (URC-1016)

35328 BITS/TK
8 TKS/TK ADDRESS
32 SECTORS/TK ADDRESS
DENSITY – 1121 bp2
PERIOD: 0.493 us/BIT,/8TK BYTE
FREQ: 1.02 MC/WORD,/2 BYTES

RECORDED DATA FORMAT – 3

- ADDRESS RECORDED INDEPENDETN OF SECTOR DATA WRITE
- ADDRESS READ PRIOR TO SECTOR DATA ACCESS
- SECTOR DATA WRITE ENABLED AFTER SATISFACTORY ADDRESS COMPARE BY CONTROLLER.



RECORDED DATA FORMAT – 3

- ADDRESS RECORDED INDEPENDETN OF SECTOR DATA WRITE
- ADDRESS READ PRIOR TO SECTOR DATA ACCESS
- SECTOR DATA WRITE ENABLED AFTER SATISFACTORY ADDRESS COMPARE BY CONTROLLER.

APPENDIX D DRUM TIMING DIAGRAM