F
L

IBM **Maintenance Information**

INDEX
MLX
LGND
START
FSI
MSG
SENSE
MICRO

VOL. R01

OLT
OPER
PANEL
CTL-I

VOL. R02

DEV-I
DATA

VOL. R03

HDA
ACC

VOL. R04

R/W
RPI
PWR
LOC
INST

VOL. R05

MICFL

VOL. R06

Volumes R01 through R06 accompany each Control Module and support all 3350s attached.

3350 Disk Storage

3350	CA0000 Seq. 1 of 2	2358630 Part No.	441300 31 Mar 76					

PREFACE

MAINTENANCE INFORMATION MANUAL ORDERING PROCEDURE (IBM Internal)

Individual pages of the 3350 Maintenance Information Manual can be ordered from the San Jose plant by using the Wiring Diagram/Logic Page Request (Order No. 120-1679). In the columns headed "Logic Page" enter the page identifier information: sequence number, sheet number, part number, and EC number. Groups of pages can be ordered by including a description (section, volume, etc.) and the machine serial number.

This manual was prepared by the IBM General Products Division, Technical Publishing, Department G26, San Jose, California 95193.

SAFETY

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it; for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment - eliminate unsafe acts.

ARTIFICIAL RESPIRATION

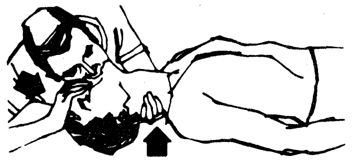
General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects.
3. After victim is breathing by himself or when help is available:
   a. Loosen clothing.
   b. Place victim on his side.
   c. Keep victim warm.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

1. Place victim on back; lift neck and tilt head way back. (Quickly remove any noticeable food or objects from mouth.)

2. Pinch nose closed; make airtight seal around victim's mouth with your mouth; and forcefully breathe into victim until chest rises (expands).

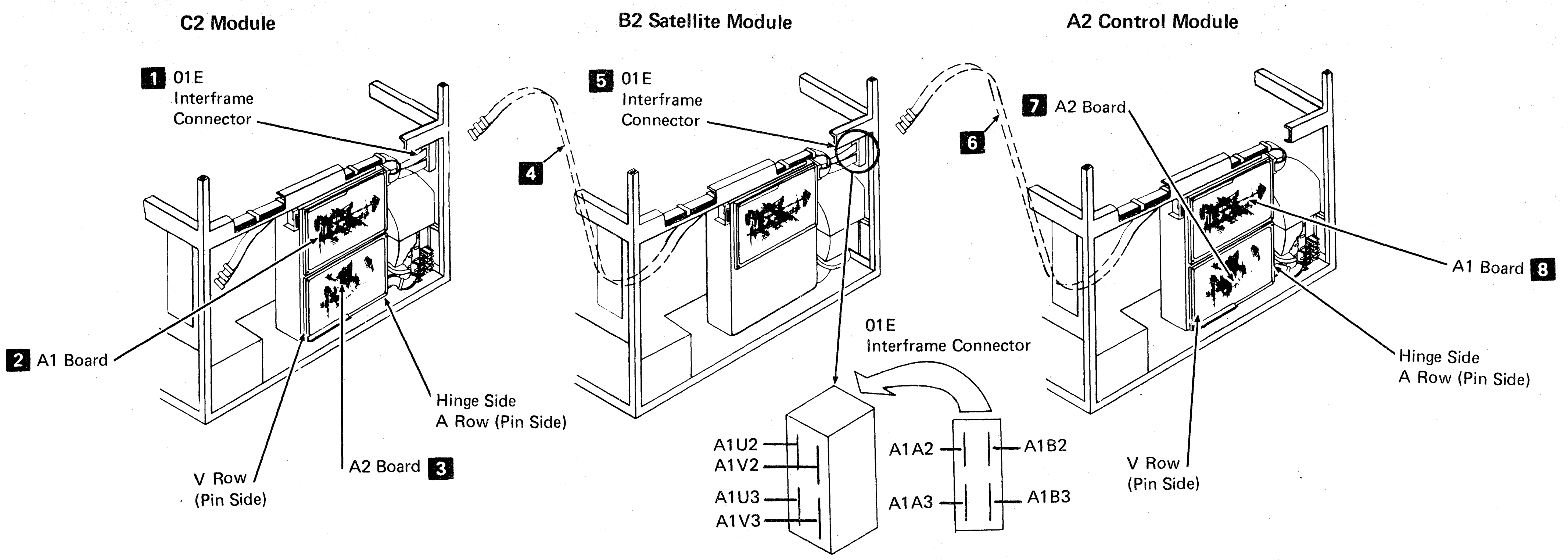


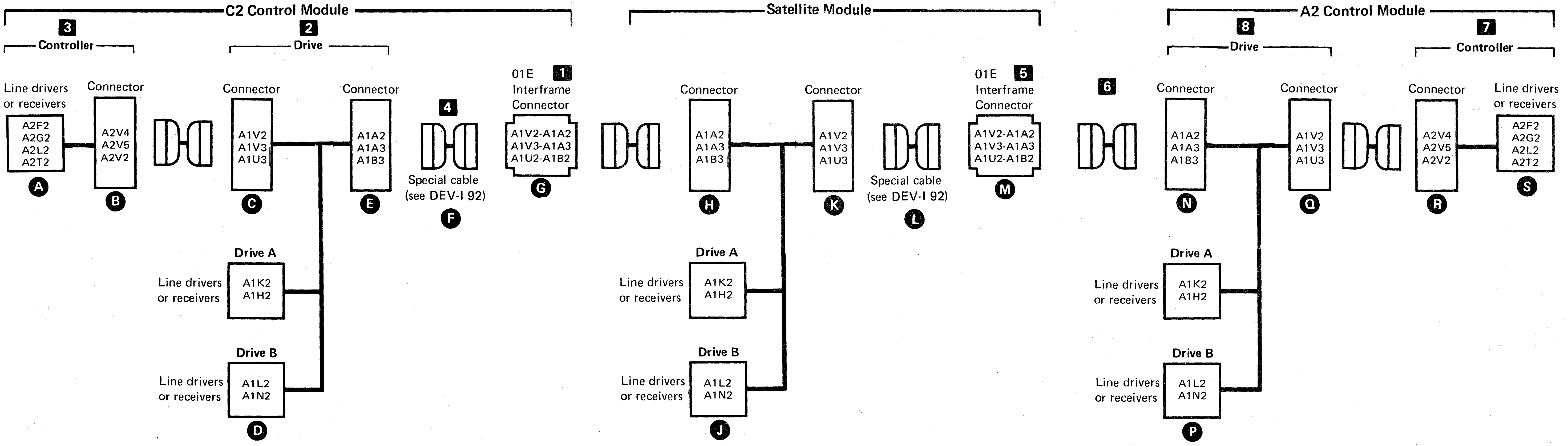
3. Continue breathing for the victim 12 times per minute WITHOUT STOPPING.
4. If chest does not rise (expand), roll victim onto side and pound firmly between shoulder blades to remove blocking material. Also, try lifting jaw higher with your fingers. Resume rescue breathing.

DEV-I CONTENTS

DEVICE INTERFRAME CABLES (C2 MODULE)

See DEV-I 100 for 3350 without C2 Module.





3350

CC0001 Side 2 of 2	2358185 Part No.	441300 31 Mar 76	441301 1 Jun 76	441303 30 Jul 76		

DEVICE INTERFACE CABLES

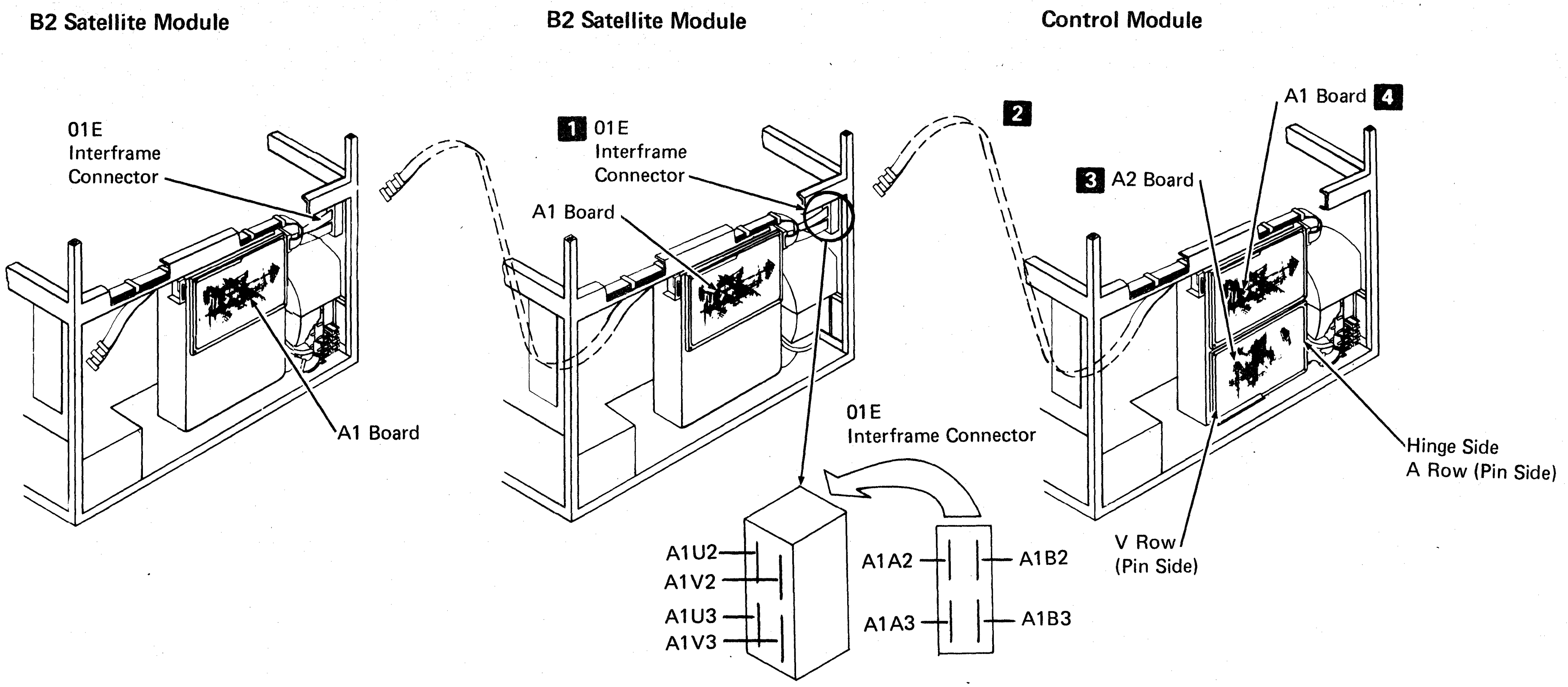
See DEV-I 102 for 3350 without C2 Module.

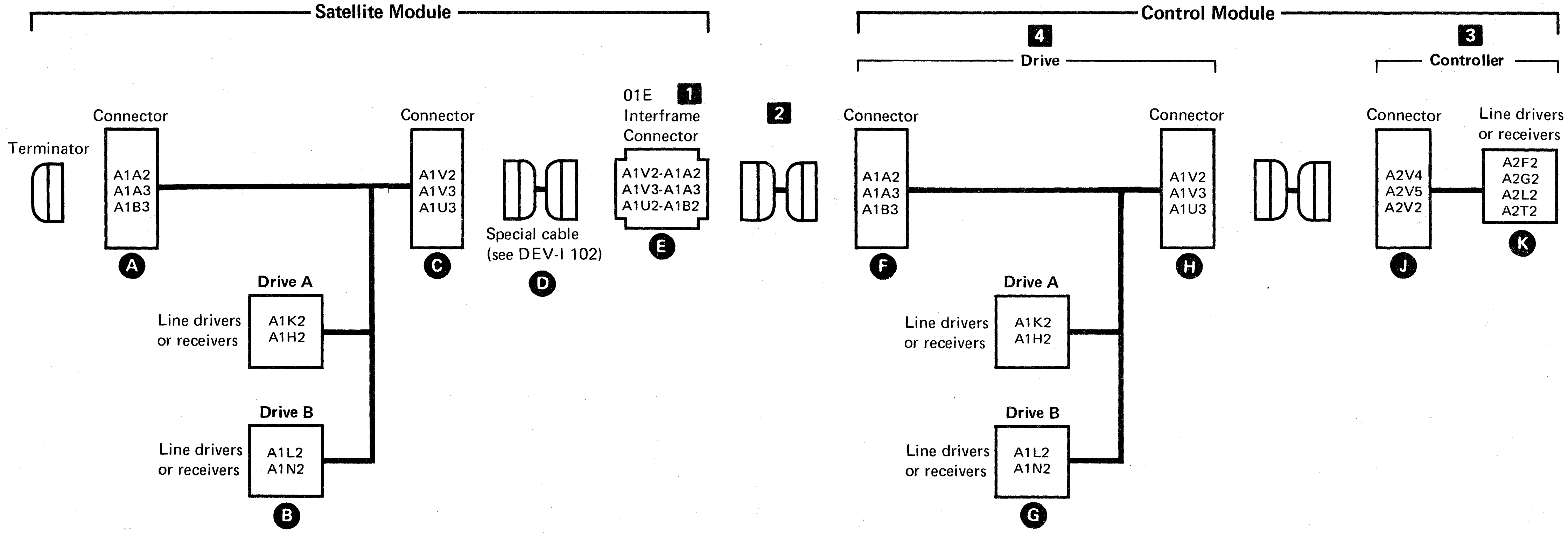
		Ⓐ	Ⓑ	Ⓒ	Ⓓ	Ⓔ	Ⓕ		Ⓖ		Ⓗ	Ⓙ	Ⓚ	Ⓛ		Ⓜ		Ⓝ	Ⓟ	Ⓠ	Ⓡ	Ⓢ
		A2F2	A2V4	A1V2	A1H2(A1N2)	A1A2	Special Cable		01E-A1V2	01E-A1A2	A1A2	A1H2(A1N2)	A1V2	Special Cable		01E-A1V2	01E-A1A2	A1A2	A1H2(A1N2)	A1V2	A2V4	A2F2
+Device Bus In Bit 0 NPL		B10	B02	B02	B05	B02	B02	D02	D02	B02	B02	B05	B02	B02	D02	D02	B02	B02	B05	B02	B02	B10
1		B07	B04	B04	D05	B04	B04	D04	D04	B04	B04	D05	B04	B04	D04	D04	B04	B04	D05	B04	B04	B07
2		G03	B05	B05	B09	B05	B05	D05	D05	B05	B05	B09	B05	B05	D05	D05	B05	B05	B09	B05	B05	G03
3	To Controller	B09	B06	B06	D10	B06	B06	D06	D06	B06	B06	D10	B06	B06	D06	D06	B06	B06	D10	B06	B06	B09
4		G12	B08	B08	D07	B08	B08	D08	D08	B08	B08	D07	B08	B08	D08	D08	B08	B08	D07	B08	B08	G12
5		J04	B09	B09	D02	B09	B09	D09	D09	B09	B09	D02	B09	B09	D09	D09	B09	B09	D02	B09	B09	J04
6		G05	B10	B10	B02	B10	B10	D10	D10	B10	B10	B02	B10	B10	D10	D10	B10	B10	B02	B10	B10	G05
7		G13	B12	B12	D06	B12	B12	D12	D12	B12	B12	D06	B12	B12	D12	D12	B12	B12	D06	B12	B12	G13
P		J13	B13	B13	B07	B13	B13	D13	D13	B13	B13	B07	B13	B13	D13	D13	B13	B13	B07	B13	B13	J13
		A2G2	A2V4	A2V2	A1K2(A1L2)	A1A2			01E-A1V2	01E-A1A2	A1A2	A1K2(A1L2)	A1V2			01E-A1V2	01E-A1A2	A1A2	A1K2(A1L2)	A1V2	A2V4	A2G2
+NPL Attn Select Bus Bit 0		U03	D02	D02	D10	D02	D02	B02	B02	D02	D02	D10	D02	D02	B02	B02	D02	D02	D10	D02	D02	U03
1		U04	D03	D03	D07	D03	D03	B03	B03	D03	D03	D07	D03	D03	B03	B03	D03	D03	D07	D03	D03	U04
2		U06	D05	D05	B13	D05	D05	B05	B05	D05	D05	B13	D05	D05	B05	B05	D05	D05	B13	D05	D05	U06
3	To Controller	U07	D06	D06	D12	D06	D06	B06	B06	D06	D06	D12	D06	D06	B06	B06	D06	D06	D12	D06	D06	U07
4		S08	D07	D07	D13	D07	D07	B07	B07	D07	D07	D13	D07	D07	B07	B07	D07	D07	D13	D07	D07	S08
5		U10	D09	D09	D11	D09	D09	B09	B09	D09	D09	D11	D09	D09	B09	B09	D09	D09	D11	D09	D09	U10
6		U11	D10	D10	D06	D10	D10	B10	B10	D10	D10	D06	D10	D10	B10	B10	D10	D10	D06	D10	D10	U11
7		S12	D11	D11	B12	D11	D11	B11	B11	D11	D11	B12	D11	D11	B11	B11	D11	D11	B12	D11	D11	S12
S		S04	D13	D13	B10	D13	D13	B13	B13	D13	D13	B10	D13	D13	B13	B13	D13	D13	B10	D13	D13	S04
		A2F2	A2V5	A1V3	A1K2(A1L2)	A1A3			01E-A1V3	01E-A1A3	A1A3	A1K2(A1L2)	A1V3			01E-A1V3	01E-A1A2	A1A3	A1K2(A1L2)	A1V3	A2V5	A2F2
+Device Out Bus Bit 0 NPL		P10	B02	B02	M07	B02	B02	D02	D02	B02	B02	M07	B02	B02	D02	D02	B02	B02	M07	B02	B02	P10
1		P12	B04	B04	U11	B04	B04	D04	D04	B04	B04	U11	B04	B04	D04	D04	B04	B04	U11	B04	B04	P12
2		U02	B05	B05	S12	B05	B05	D05	D05	B05	B05	U12	B05	B05	D05	D05	B05	B05	U12	B05	B05	U02
3		S03	B06	B06	S11	B06	B06	D06	D06	B06	B06	S11	B06	B06	D06	D06	B06	B06	S11	B06	B06	S03
4	From Controller	S12	B08	B08	U04	B08	B08	D08	D08	B08	B08	U04	B08	B08	D08	D08	B08	B08	U04	B08	B08	S12
5		U12	B09	B09	S04	B09	B09	D09	D09	B09	B09	S04	B09	B09	D09	D09	B09	B09	S04	B09	B09	U12
6		U05	B10	B10	S02	B10	B10	D10	D10	B10	B10	S02	B10	B10	D10	D10	B10	B10	S02	B10	B10	U05
7		U09	B12	B12	M09	B12	B12	D12	D12	B12	B12	M09	B12	B12	D12	D12	B12	B12	M09	B12	B12	U09
P		M07	B13	B13	U03	B13	B13	D13	D13	B13	B13	U03	B13	B13	D13	D13	B13	B13	U03	B13	B13	M07
		A2L2	A2V5	A1V3	A1K2(A1L2)	A1A3			01E-A1V3	01E-A1A3	A1A3	A1K2(A1L2)	A1V3			01E-A1V3	01E-A1A3	A1A3	A1K2(A1L2)	A1V3	A2V5	A2L2
+NPL Tag Bus Bit 0		J10	D02	D02	J05	D02	D02	B02	B02	D02	D02	J05	D02	D02	B02	B02	D02	D02	J05	D02	D02	J10
1		P03	D03	D03	G03	D03	D03	B03	B03	D03	D03	G03	D03	D03	B03	B03	D03	D03	G03	D03	D03	P03
2	From Controller	J12	D05	D05	G05	D05	D05	B05	B05	D05	D05	G05	D05	D05	B05	B05	D05	D05	G05	D05	D05	U12
P		J04	D06	D06	G04	D06	D06	B06	B06	D06	D06	G04	D06	D06	B06	B06	D06	D05	G04	D06	D06	U04
+Device Tag Gate NPL		J02	D07	D07	P09	D07	D07	B07	B07	D07	D07	P09	D07	D07	B07	B07	D07	D07	P09	D07	D07	U02
+Device Sel Hold NPL		M03	D09	D09	M08	D09	D09	B09	B09	D09	D09	M08	D09	D09	B09	B09	D09	D09	M08	D09	D09	M03
	To Controller	A2G2	A2V5	A1V3	A1K2(A1L2)	A1A3			01E-A1V3	01E-A1A3	A1A3	A1K2(A1L2)	A1V3			01E-A1V3	01E-A1A3	A1A3	A1K2(A1L2)	A1V3	A2V5	A2G2
+File Tag Valid NPL		S07	D13	D13	B07	D13	D13	B13	B13	D13	D13	B07	D13	D13	B13	B13	D13	D13	B07	D13	D13	S07
		A2T2	A2V2	A1U3	A1H2(A1N2)	A1B3			01E-A1U2	01E-A1B3	A1B3	A1H2(A1N2)	A1U3			01E-A1U2	01E-A1B2	A1B3	A1H2(A1N2)	A1U3	A2V2	A2T2
–PLO Pulse Driver	To Controller	D06	D03	D03	B04	D03	D03	B03	B03	D03	D03	B04	D03	D03	B03	B03	D03	D03	B04	D03	D03	D06
+PLO Pulse Driver		D05	D02	D02	B03	D02	D02	B02	B02	D02	D02	B03	D02	D02	B02	B02	D02	D02	B03	D02	D02	D05
	To/From Controller				A1J2(A1M2)							A1J2(A1M2)							A1J2(A1M2)			
+R/W Data		D07	B12	B12	D13	B12	B12	D12	D12	B12	B12	D13	B12	B12	D12	D12	B12	B12	D13	B12	B12	D07
–R/W Data		B05	B13	B13	D12	B13	B13	D13	D13	B13	B13	D12	B13	B13	D13	D13	B13	B13	D12	B13	B13	B05

CC0092 Seq. 1 of 2	2358713 Part No.	441301 1 June 76	441303 30 Jul 76			

DEVICE INTERFRAME CABLES

See DEV-I 90 for 3350 with C2 Module.





3350	CC0092 Side 2 of 2	2358713 Part No.	441301 1 Jun 76	441303 30 Jul 76			

DEVICE INTERFACE CABLES

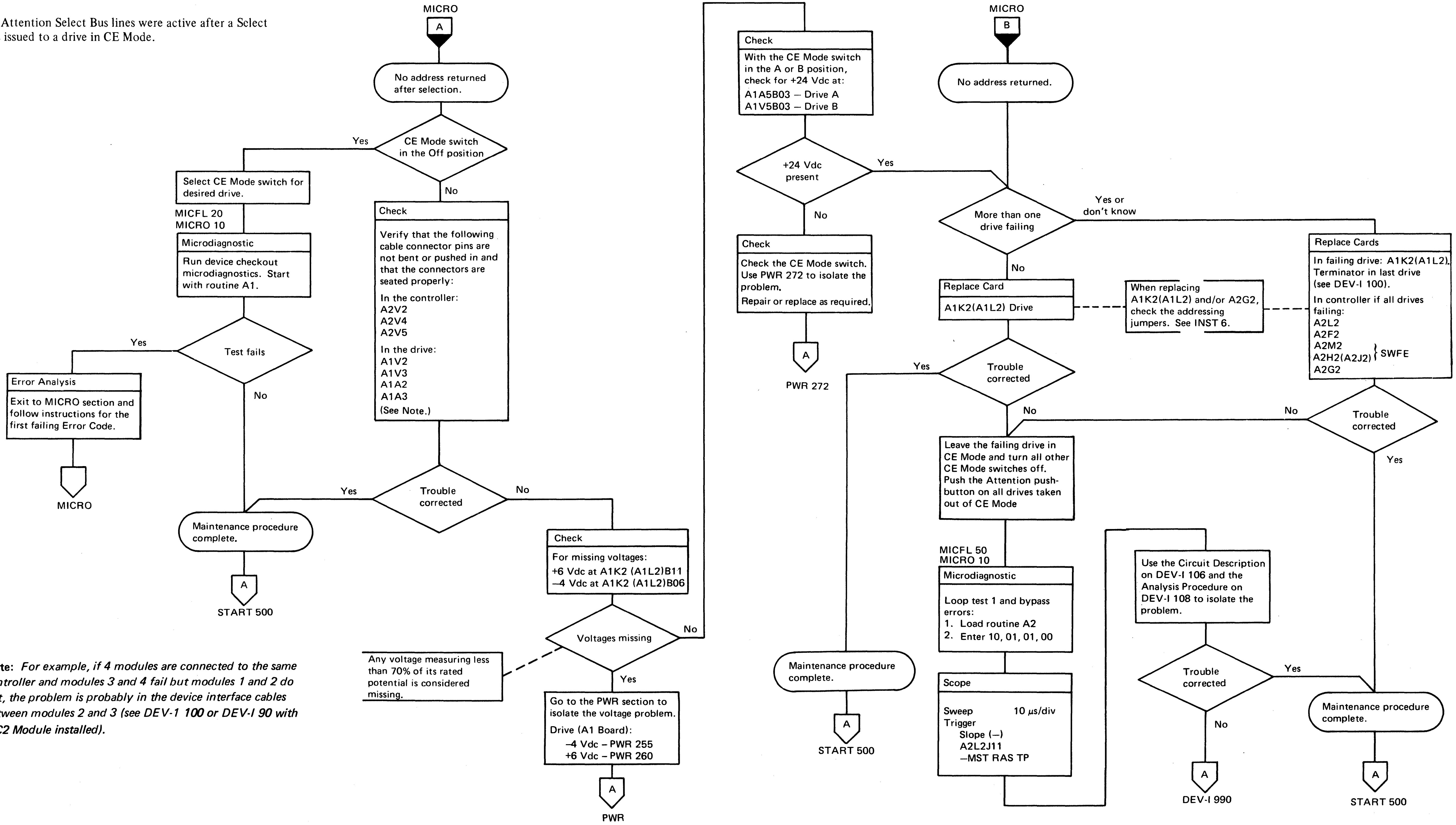
See DEV-I 92 for 3350 with C2 Module.

		Ⓐ	Ⓑ	Ⓒ	Ⓓ		Ⓔ		Ⓕ	Ⓖ	Ⓗ	Ⓙ	Ⓚ
		A1A2	**A1H2(A1N2)**	**A1V2**	**Special Cable**		**A1V2**	**A1A2**	**A1A2**	**A1H2(A1N2)**	**A1V2**	**A2V4**	**A2F2**
+Device Bus In Bit 0 NPL	To Controller	B02	B05	B02	B02	D02	D02	B02	B02	B05	B02	B02	B10
1		B04	D05	B04	B04	D04	D04	B04	B04	D05	B04	B04	B07
2		B05	B09	B05	B05	D05	D05	B05	B05	B09	B05	B05	G03
3		B06	D10	B06	B06	D06	D06	B06	B06	D10	B06	B06	B09
4		B08	D07	B08	B08	D08	D08	B08	B08	D07	B08	B08	G12
5		B09	D02	B09	B09	D09	D09	B09	B09	D02	B09	B09	J04
6		B10	B02	B10	B10	D10	D10	B10	B10	B02	B10	B10	G05
7		B12	D06	B12	B12	D12	D12	B12	B12	D06	B12	B12	G13
P		B13	B07	B13	B13	D13	D13	B13	B13	B07	B13	B13	J13
		A1A2	**A1K2(A1L2)**	**A1V2**			**A1V2**	**A1A2**	**A1A2**	**A1K2(A1L2)**	**A1V2**	**A2V4**	**A2G2**
+NPL Attn Select Bus Bit 0	To Controller	D02	D10	D02	D02	B02	B02	D02	D02	D10	D02	D02	U03
1		D03	D07	D03	D03	B03	B03	D03	D03	D07	D03	D03	U04
2		D05	B13	D05	D05	B05	B05	D05	D05	B13	D05	D05	U06
3		D06	D12	D06	D06	B06	B06	D06	D06	D12	D06	D06	U07
4		D07	D13	D07	D07	B07	B07	D07	D07	D13	D07	D07	S08
5		D09	D11	D09	D09	B09	B09	D09	D09	D11	D09	D09	U10
6		D10	D06	D10	D10	B10	B10	D10	D10	D06	D10	D10	U11
7		D11	B12	D11	D11	B11	B11	D11	D11	B12	D11	D11	S12
S		D13	B10	D13	D13	B13	B13	D13	D13	B10	D13	D13	S04
		A1A3	**A1K2(A1L2)**	**A1V3**			**A1V3**	**A1A3**	**A1A3**	**A1K2(A1L2)**	**A1V3**	**A2V5**	**A2F2**
+Device Out Bus Bit 0 NPL	From Controller	B02	M07	B02	B02	D02	D02	B02	B02	M07	B02	B02	P10
1		B04	U11	B04	B04	D04	D04	B04	B04	U11	B04	B04	P12
2		B05	U12	B05	B05	D05	D05	B05	B05	U12	B05	B05	U02
3		B06	S11	B06	B06	D06	D06	B06	B06	S11	B06	B06	S03
4		B08	U04	B08	B08	D08	D08	B08	B08	U04	B08	B08	S12
5		B09	S04	B09	B09	D09	D09	B09	B09	S04	B09	B09	U12
6		B10	S02	B10	B10	D10	D10	B10	B10	S02	B10	B10	U05
7		B12	M09	B12	B12	D12	D12	B12	B12	M09	B12	B12	U09
P		B13	U03	B13	B13	D13	D13	B13	B13	U03	B13	B13	M07
		A1A3	**A1K2(A1L2)**	**A1V3**			**A1V3**	**A1A3**	**A1A3**	**A1K2(A1L2)**	**A1V3**	**A2V5**	**A2L2**
+NPL Tag Bus Bit 0	From Controller	D02	J05	D02	D02	B02	B02	D02	D02	J05	D02	D02	J10
1		D03	G03	D03	D03	B03	B03	D03	D03	G03	D03	D03	P03
2		D05	G05	D05	D05	B05	B05	D05	D05	G05	D05	D05	J12
P		D06	G04	D06	D06	B06	B06	D06	D06	G04	D06	D06	J04
+Device Tag Gate NPL		D07	P09	D07	D07	B07	B07	D07	D07	P09	D07	D07	J02
+Device Sel Hold NPL		D09	M08	D09	D09	B09	B09	D09	D09	M08	D09	D09	M03
		A1A3	**A1K2(A1L2)**	**A1V3**			**A1V3**	**A1A3**	**A1A3**	**A1K2(A1L2)**	**A1V3**	**A2V5**	**A2G2**
+File Tag Valid NPL	To Controller	D13	B07	D13	D13	B13	B13	D13	D13	B07	D13	D13	S07
		A1B3	**A1H2(A1N2)**	**A1U3**			**A1U2**	**A1B2**	**A1B3**	**A1H2(A1N2)**	**A1U3**	**A2V2**	**A2T2**
–PLO Pulse Driver	To Controller	D03	B04	D03	D03	B03	B03	D03	D03	B04	D03	D03	D06
+PLO Pulse Driver		D02	B03	D02	D02	B02	B02	D02	D02	B03	D02	D02	D05
			A1J2(A1M2)							**A1J2(A1M2)**			
+R/W Data	To/From Controller	B12	D13	B12	B12	D12	D12	B12	B12	D13	B12	B12	D07
–R/W Data		B13	D12	B13	B13	D13	D13	B13	B13	D12	B13	B13	B05

3350	CC0102 Side 1 of 1	2358343 Part No.	441300 31 Mar 76	441301 1 June 76			

NO ADDRESS RETURNED AFTER SELECT

No Attention Select Bus lines were active after a Select was issued to a drive in CE Mode.



Note: *For example, if 4 modules are connected to the same controller and modules 3 and 4 fail but modules 1 and 2 do not, the problem is probably in the device interface cables between modules 2 and 3 (see DEV-1 100 or DEV-I 90 with a C2 Module installed).*

NO ADDRESS RETURNED AFTER SELECT

Circuit Description

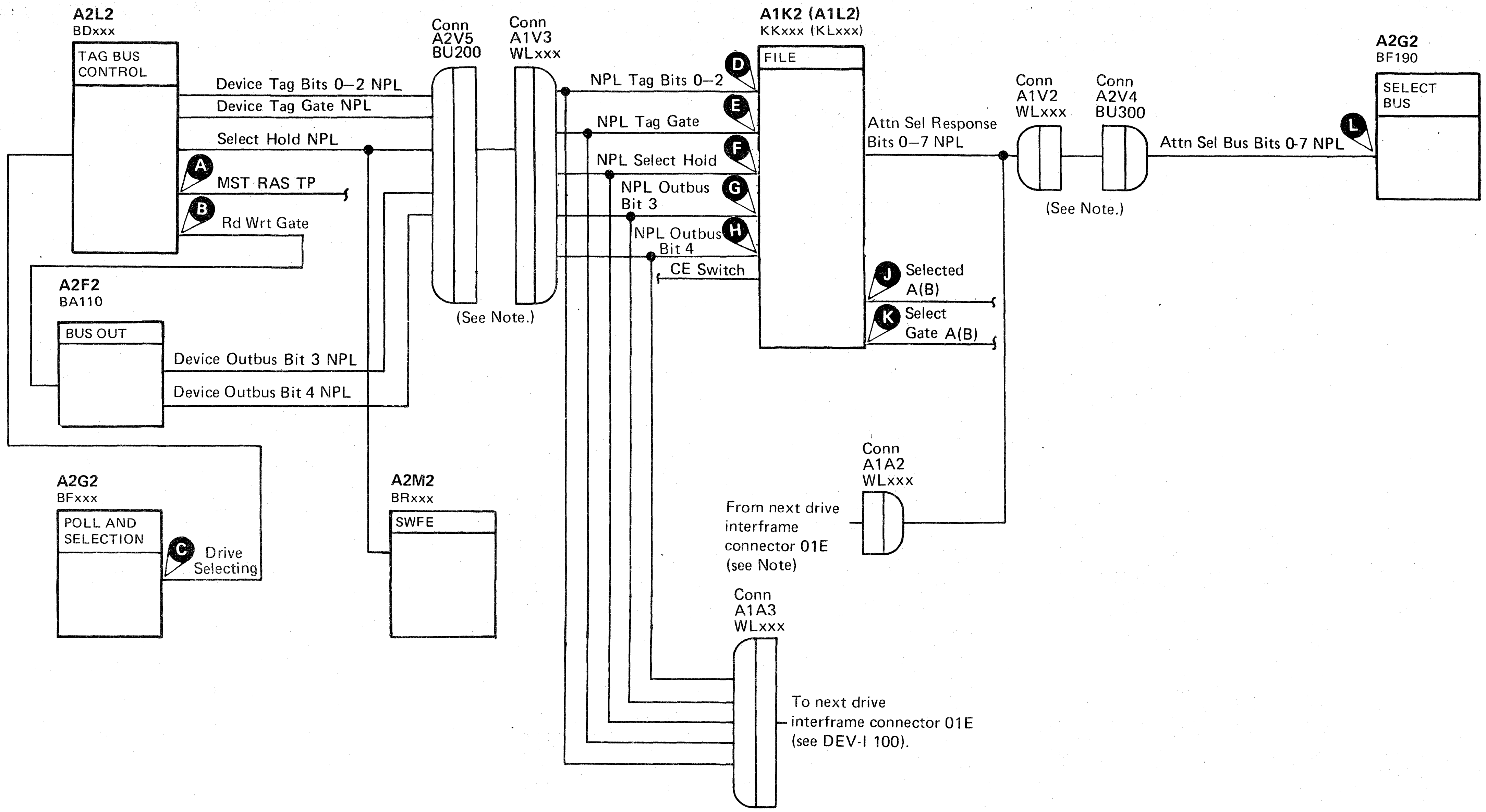
The A210 Error Code indicates that no drive physical address was returned on the Attention Select Bus Ⓛ after selection. A Select was sent (Tag '83') to a drive in CE Mode, the microprogram issued a Sense Physical Address (Tag '04' Bus '01'), and found all Attention Select Bus lines inactive. The address of the drive in CE Mode should activate the corresponding Attention Select Bus line (drive 0 = Attention Select Bus Bit 0 line is active, drive 1 = Attention Select Bus Bit 1 line is active, etc). See Figure 1.

To determine drive addresses, see INST 6. DEV-I 164 shows the Attn Sel Bus in detail.

Figure 1. Attn Sel Bus Bits Pin Locations Ⓛ

Bits	+Attn Sel Bus NPL A2G2	+NPL Attn Sel Response A1K2 (A1L2)
0	U03	D10
1	U04	D07
2	U06	B13
3	U07	D12
4	S08	D13
5	U10	D11
6	U11	D06
7	S12	B12

See OPER 92 for additional theory.



Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

NO ADDRESS RETURNED AFTER SELECT

Analysis Procedure

Scope the +Selected A(B) Ⓙ line for the drive in CE Mode. Selected A(B) becomes Normal Attn (KK150, KL150). Normal Attn and the addressing jumpers activate Attn Sel Response.

If +Selected A(B) Ⓙ is + level (MST-1), scope the Attn Sel Bus Bit Ⓛ line. If the Attn Sel Bus Bit line is –level (NPL) during Tag '83' time, check the following:

The address jumpers on A1K2 (A1L2) card (KK130, KL130) (see INST 6).
The Attn Sel cables and connectors (see DEV-I 164).

If +Selected A(B) Ⓙ is – level (MST-1), all of the following conditions must be satisfied at Tag '83' time for a drive to select:

+Select Gate A(B) Ⓚ is + level (MST-1).
+NPL Outbus Bit 4 Ⓗ is – level (NPL).
+NPL Select Hold Ⓕ is + level (NPL).
+NPL Outbus Bit 3 Ⓖ is + level (NPL).
–CE Switch is – level (MST-1) (KK140, KL140).

+Select Gate is activated by decoding the Tag Bus as 000.

+NPL Tag Bus Bits 0, 1, and 2 Ⓓ are – level (NPL).
+NPL Tag Gate Ⓔ is + level (NPL).

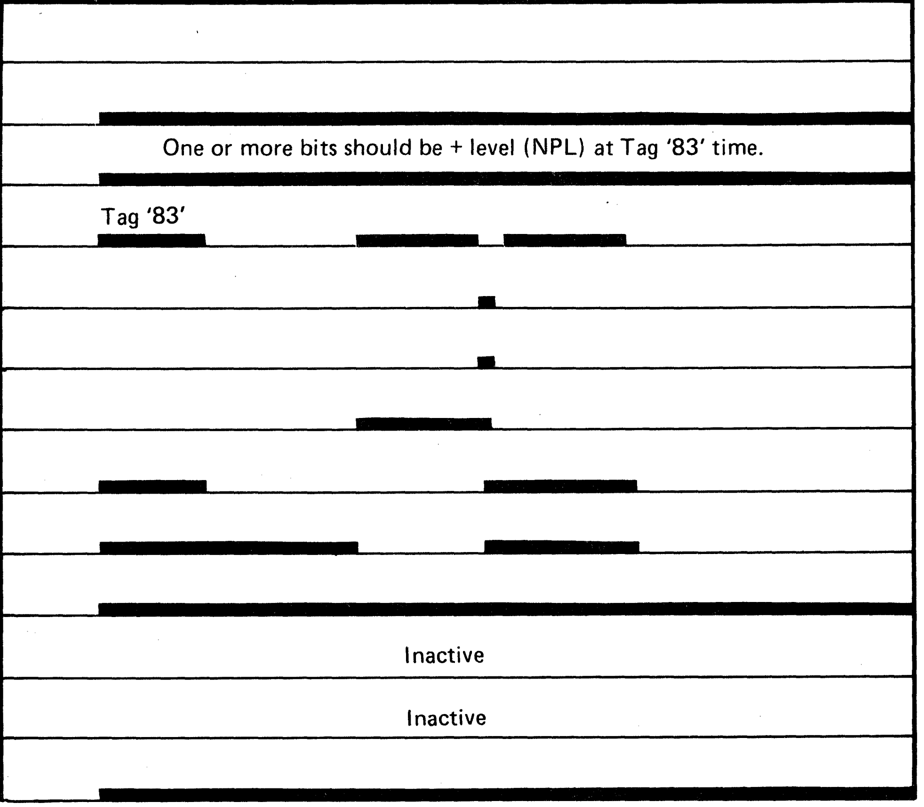
If NPL Outbus Bit 4 is + level (NPL), it prevents the drive from selecting.

If –Rd Wrt Gate Ⓑ is – level (MST-1), it causes bit 4 to be active.

+NPL Select Hold is activated by –Drive Selecting Ⓒ.

Legend: ▭ Inactive
▬ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		
1	–MST RAS TP	BD100	A2L2 J11	Ⓐ	
2	+NPL Select Hold	KK100 (KL100)	A1K2 (A1L2) M08	Ⓕ	
3	+Attn Sel Bus Bit 0–7 NPL	BF160	See Figure 1 on DEV-I 106 for pin locations.	Ⓛ	One or more bits should be + level (NPL) at Tag '83' time.
4	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓔ	Tag '83'
5	+NPL Tag Bus Bit 0	KK100 (KL100)	A1K2 (A1L2) J05	Ⓓ	
6	+NPL Tag Bus Bit 1	KK100 (KL100)	A1K2 (A1L2) G03	↓	
7	+NPL Tag Bus Bit 2	KK100 (KL100)	A1K2 (A1L2) G05		
8	+Select Gate A(B)	KK120 (KL120)	A1K2 (A1L2) P13	Ⓚ	
9	+NPL Outbus Bit 3	KK110 (KL110)	A1K2 (A1L2) S11	Ⓖ	
10	+Selected A(B)	KK140 (KL140)	A1K2 (A1L2) G12	Ⓙ	
11	+NPL Outbus Bit 4	KK110 (KL110)	A1K2 (A1L2) U04	Ⓗ	Inactive
12	–Rd Wrt Gate	BD150	A2L2 G10	Ⓑ	Inactive
13	–Drive Selecting	BF120	A2G2 S11	Ⓒ	



MULTIPLE SELECTION ERRORS

When a drive is selected, one and only one unique physical address bit is expected on the Attention Select Bus Ⓗ. If multiple Attention Select Bus bit lines are active at the same time, a Check 1 of 8 Ⓙ occurs. The Check 1 of 8 activates the Drive Selection error (Bus In bit 2).

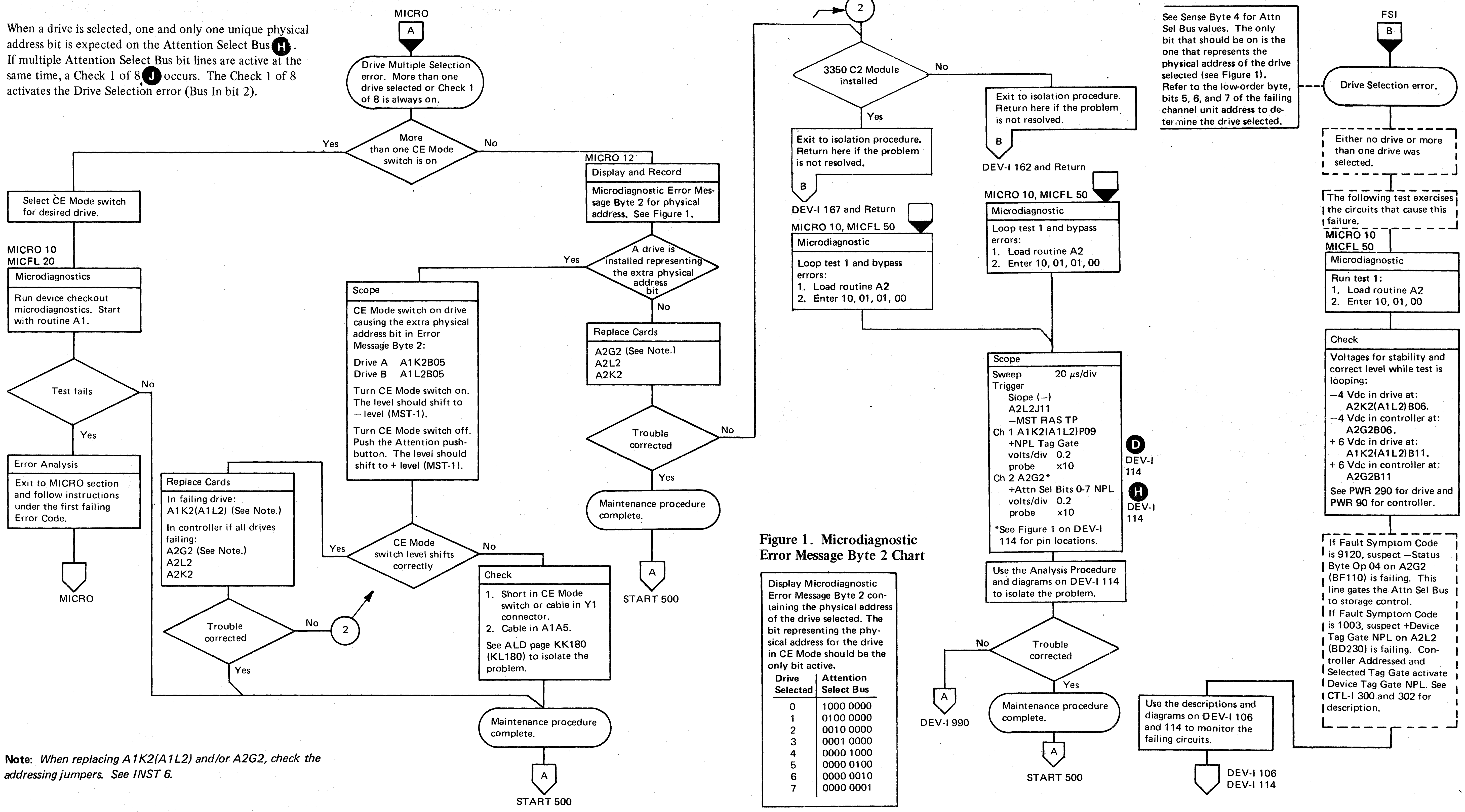


Figure 1. Microdiagnostic Error Message Byte 2 Chart

Display Microdiagnostic Error Message Byte 2 containing the physical address of the drive selected. The bit representing the physical address for the drive in CE Mode should be the only bit active.

Drive Selected	Attention Select Bus
0	1000 0000
1	0100 0000
2	0010 0000
3	0001 0000
4	0000 1000
5	0000 0100
6	0000 0010
7	0000 0001

Note: *When replacing A1K2(A1L2) and/or A2G2, check the addressing jumpers. See INST 6.*

MULTIPLE SELECTION ERRORS

Circuit Description

The A212 Error Code indicates that multiple Attention Select Bus Bit lines are active or the Check 1of 8 Ⓙ circuit is failing.

Analysis Procedure

Microdiagnostic Error Message Byte 2 indicates the drive(s) selected. Determine the Attention Select Bus Bit line that is active (drive in CE Mode) for this test and place the scope probe on one of the active error lines and continue scoping.

+Attn Sel Bus Bits 0-7 NPL Ⓗ line is active because of the error caused by:

- Miswired address jumpers on A1K2(A1L2) card KK130 (KL130). See INST 6.
- –Normal Attn is – level (MST-1) KK130(KL130), but should be + level (MST-1).

–Normal Attn KK130(KL130) is active when +Selected A(B) Ⓖ is active (MST-1).

+Selected A(B) is active (MST-1) when:

+Select Gate A(B) Ⓕ is + level (MST-1).
CE Switch Ⓔ is active KK140(KL140).

+Select Gate A(B) is active when the decode of the Tag Bus is zeros and the NPL Tag Gate Ⓓ is active. If the Tag Gate is active for too long a time, both drives of the module under test select.

See OPER 92 for additional theory.

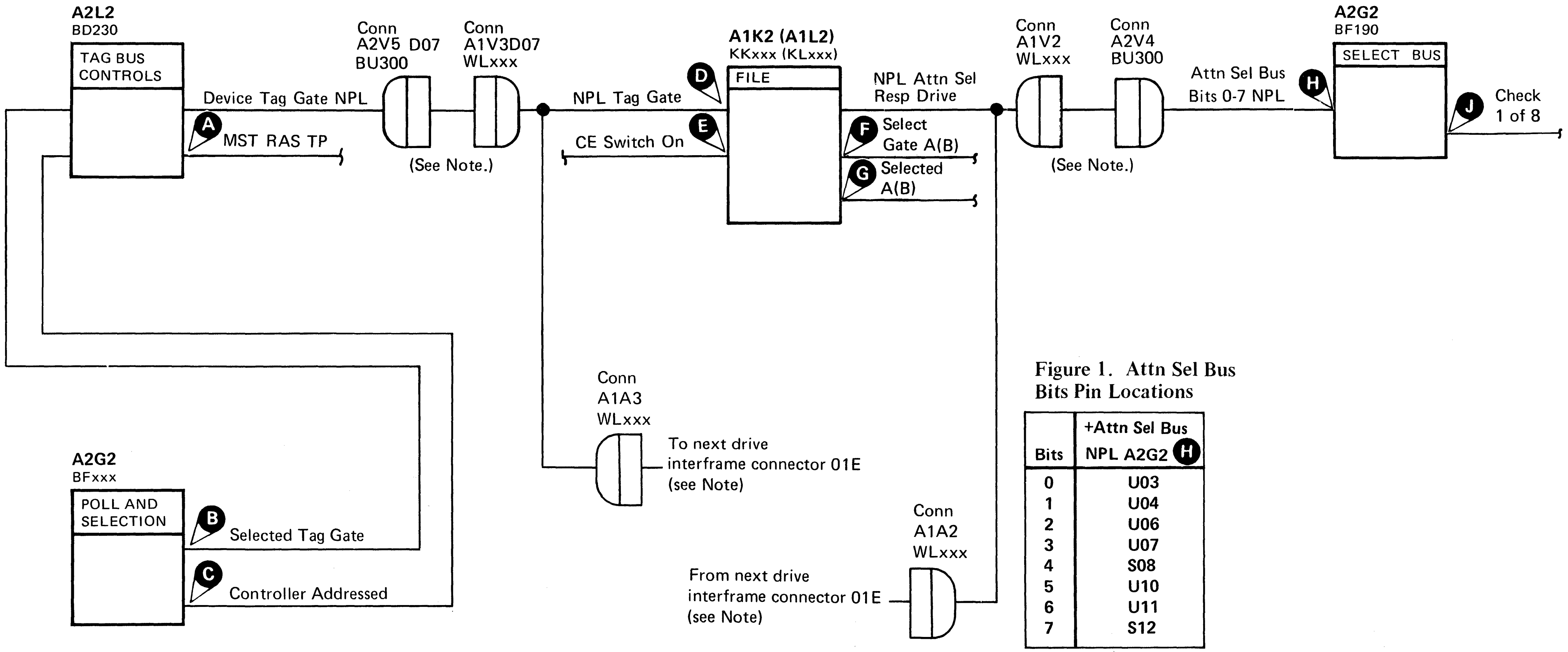
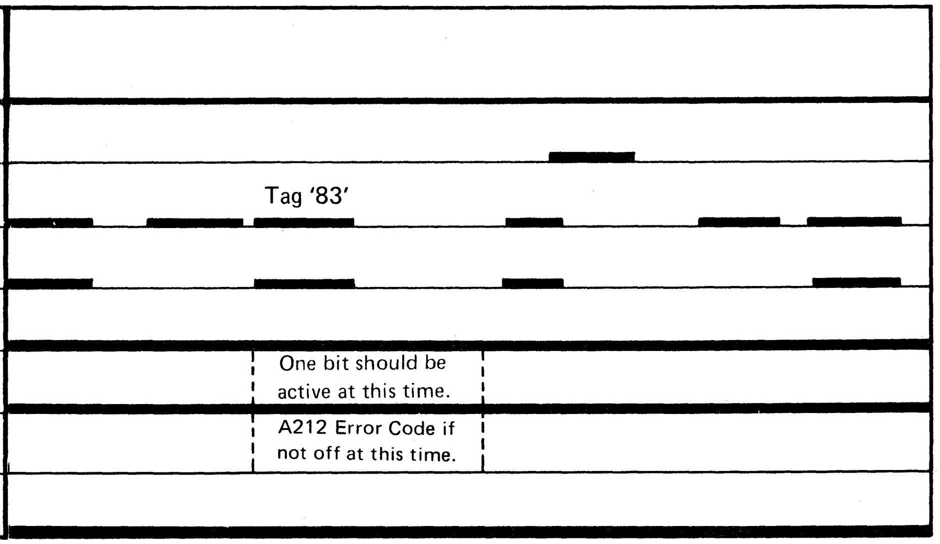


Figure 1. Attn Sel Bus Bits Pin Locations

Bits	+Attn Sel Bus NPL A2G2 Ⓗ
0	U03
1	U04
2	U06
3	U07
4	S08
5	U10
6	U11
7	S12

DEV-I 164 shows the Attention Select Bus in detail. To determine drive address see INST 6.

Legend:
▭ Inactive
▬ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		
1	–MST RAS TP	BD100	A2L2J11	Ⓐ	
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓓ	Tag '83'
3	+Select Gate A(B)	KK120 (KL120)	A1K2 (A1L2) P13	Ⓕ	
4	+Selected A(B)	KK160 (KL160)	A1K2 (A1L2) G12	Ⓖ	
5	+Attn Sel Bus Bits 0-7 NPL	BF160	See Figure 1.	Ⓗ	One bit should be active at this time.
6	+Check 1 of 8	BF200	A2G2 S13	Ⓙ	A212 Error Code if not off at this time.
7	+CE Switch	KK140 (KL140)		Ⓔ	

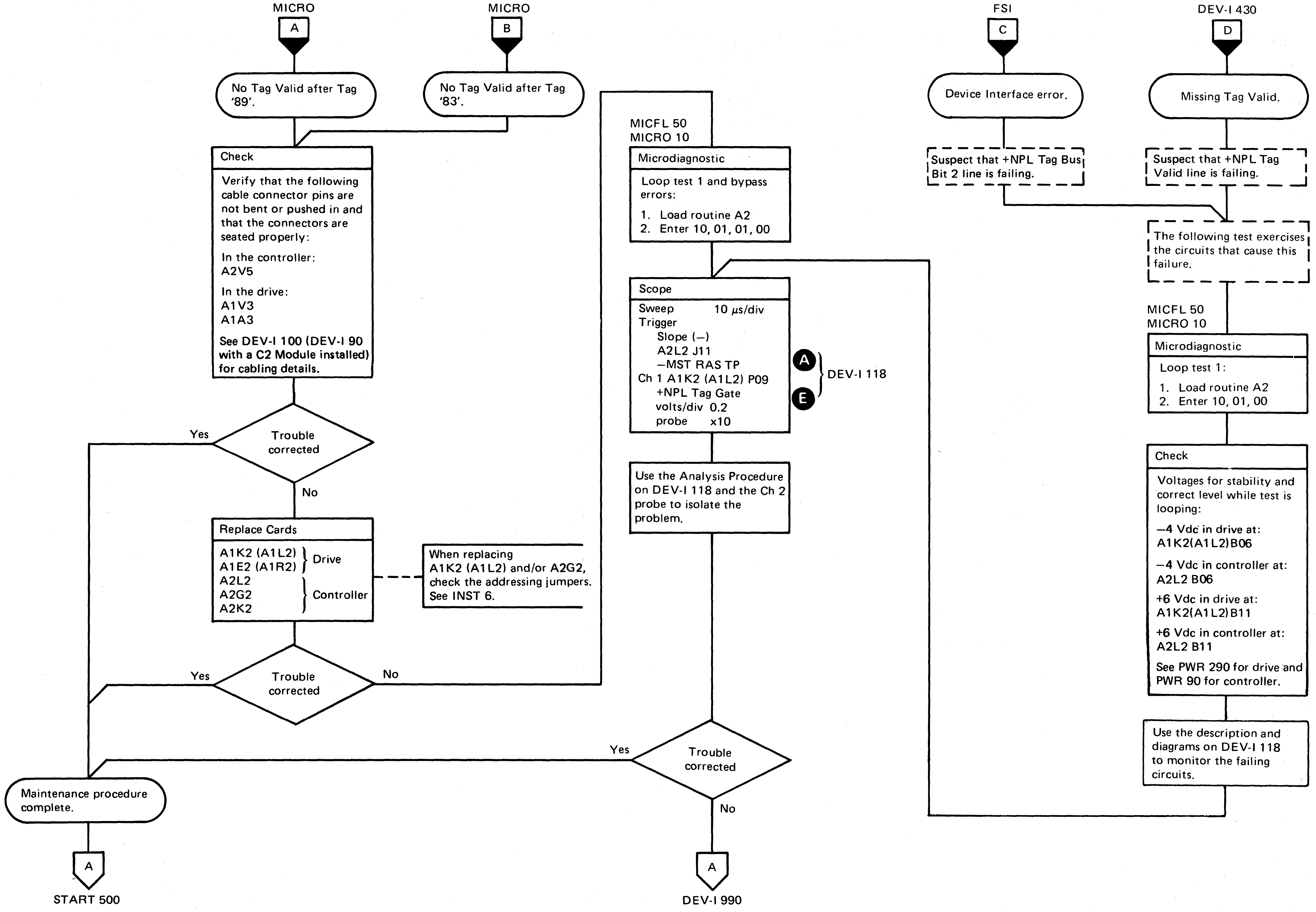
Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

3350

CC0114 Seq. 1 of 2	2358346 Part No.	441300 31 Mar 76	441303 30 Jul 76	441310 27 Jun 80		

NO TAG VALID

The drive forces NPL Tag Valid Ⓕ to the controller even if Device Interface checks exist.



3350	CC0114 Seq. 2 of 2	2358346 Part No.	441300 31 Mar 76	441303 30 Jul 76	441310 27 Jun 80		

NO TAG VALID

Circuit Description

Sense Interface (Tag '89') or a Select (Tag '83') did not return a +NPL Tag Valid Ⓕ to the controller. Tag Resp Ⓒ in the controller is developed from +NPL Tag Valid.

Analysis Procedure

+Tag Resp Ⓒ is active (MST-1) when +File Tag Valid NPL Ⓑ is active.

+File Tag Valid NPL is active when +NPL Tag Valid Ⓕ in the drive is active.

DURING TAG '89' TIME

+NPL Tag Valid is active when:
- +Sense Interface A(B) Ⓖ is + level (MST-1).
- +Selected A(B) Ⓗ is + level (MST-1).

+Sense Interface is active (MST-1) when:
- +NPL Tag Gate Ⓔ is + level (NPL).
- +NPL Tag Bus Bit 0 Ⓓ is – level (NPL).
- +NPL Tag Bus Bit 1 is – level (NPL).
- +NPL Tag Bus Bit 2 is + level (NPL).
- +NPL Tag Bus Bit P is – level (NPL).

DURING TAG '83' TIME

+NPL Tag Valid is active when:
- +Selected A(B) is + level (MST-1).
- +NPL Tag Bus Bit 0, 1, 2 is – level (NPL).
- +NPL Tag Bus Bit P is + level (NPL).
- +Selected A(B) Ⓗ is active when NPL Select Hold is active.

See OPER 92 for additional theory.

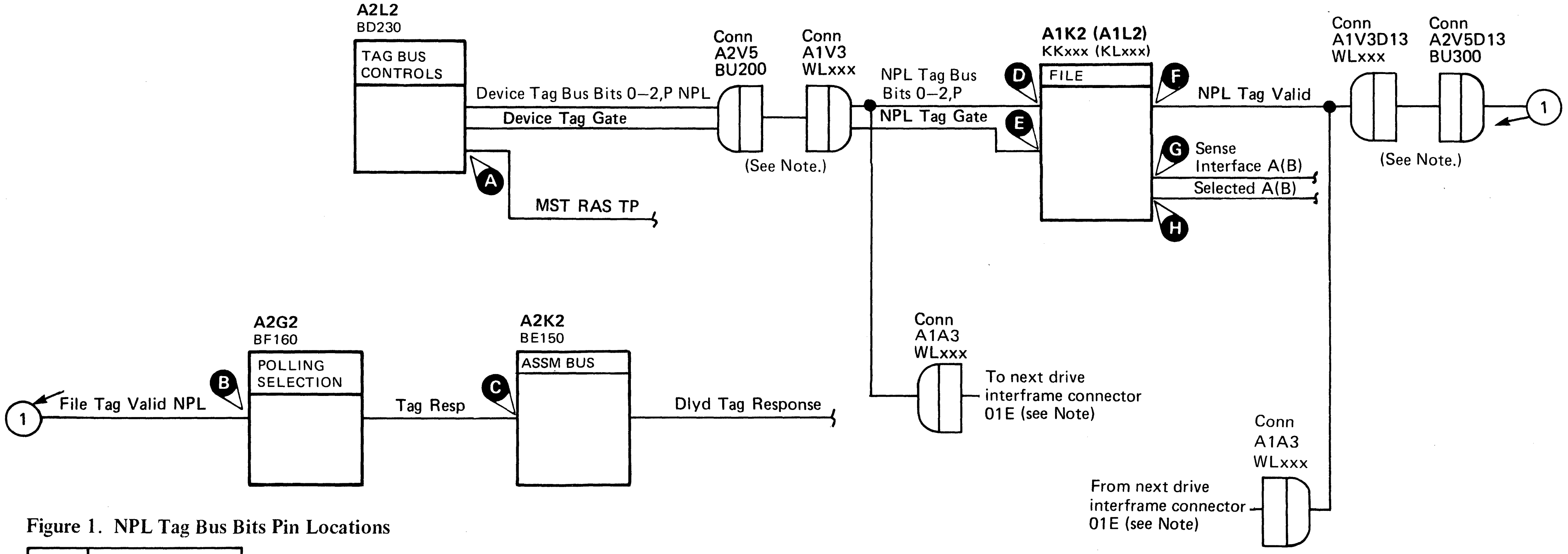
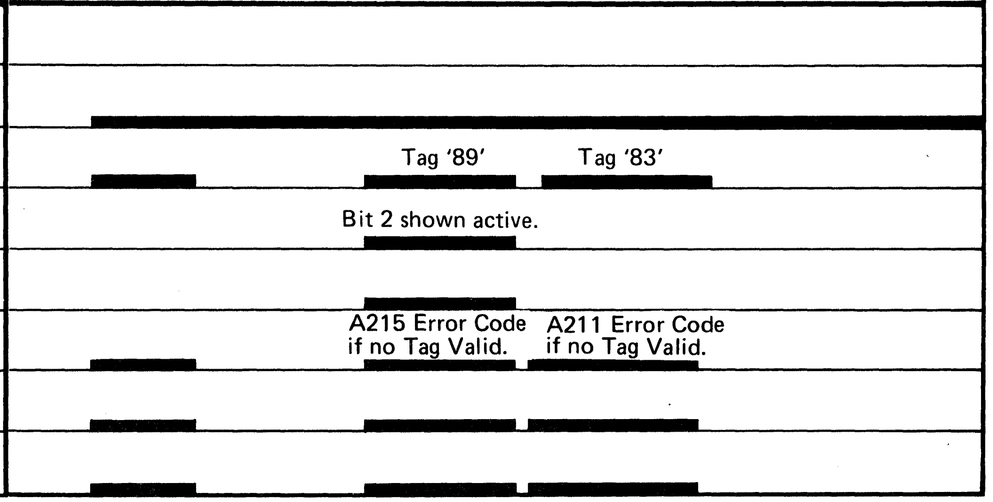


Figure 1. NPL Tag Bus Bits Pin Locations

Bits	+NPL Tag Bus A1K2 (A1L2) Ⓓ
0	J05
1	G03
2	G05
P	G04

Legend: ▭ Inactive ▬ Active level ▨ Tolerance

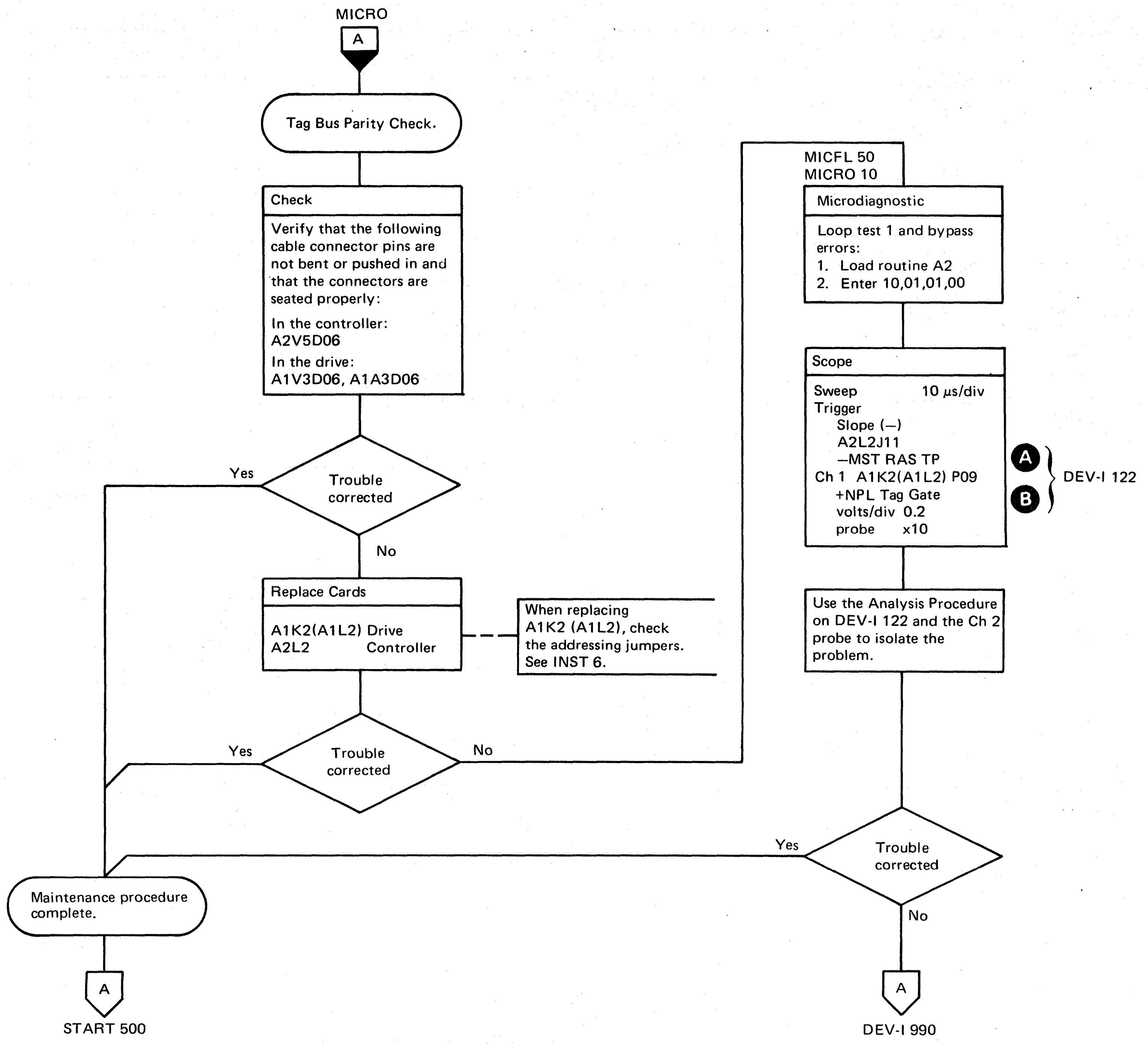
Chart Line No.	Line Name	ALD	Test Point		
1	–MST RAS TP	BD100	A2L2 J11	Ⓐ	
2	+Selected A(B)	KK140 (KL140)	A1K2 (A1L2) G12	Ⓗ	
3	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓔ	Tag '89' Tag '83'
4	+NPL Tag Bus Bits 0–2,P	KK100 (KL100)	See Figure 1.	Ⓓ	Bit 2 shown active.
5	+Sense Interface A(B)	KK140 (KL140)	A1K2 (A1L2) J09	Ⓖ	
6	+NPL Tag Valid	KK140 (KL140)	A1K2 (A1L2) B07	Ⓕ	A215 Error Code if no Tag Valid. A211 Error Code if no Tag Valid.
7	+File Tag Valid NPL	BF160	A2G2 S07	Ⓑ	
8	+Tag Resp	BE150	A2K2 B02	Ⓒ	



Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

TAG BUS PARITY CHECK

A drive is selected and no +NPL Tag Valid Ⓒ returned to the controller because of a Tag Bus Parity error.



Verify that the following cable connector pins are not bent or pushed in and that the connectors are seated properly:
In the controller:
A2V5D06
In the drive:
A1V3D06, A1A3D06

A1K2(A1L2) Drive
A2L2 Controller

When replacing A1K2 (A1L2), check the addressing jumpers. See INST 6.

Loop test 1 and bypass errors:
1. Load routine A2
2. Enter 10,01,01,00

Sweep 10 μs/div
Trigger
Slope (−)
A2L2J11
−MST RAS TP
Ch 1 A1K2(A1L2) P09
+NPL Tag Gate
volts/div 0.2
probe x10

Use the Analysis Procedure on DEV-I 122 and the Ch 2 probe to isolate the problem.

CC0118 Seq. 2 of 2	2358347 Part No.	441300 31 Mar 76	441303 30 Jul 76			

TAG BUS PARITY CHECK

Circuit Description

A Tag Bus Parity Error Ⓓ has occurred during a Tag '83' which prevents +NPL Tag Valid Ⓒ from becoming active.

Analysis Procedure

The –Tag Bus Parity Error line, KK120 (KL120), should be inactive during Tag '89' and Tag '83' time. If not, scope the Tag Bus bits beginning at bits 0 through 2, and P, as shown in Figure 1.

DURING TAG '89' TIME

Tag Bus Bits 0, 1, and P are – level (NPL).
Tag Bus Bit 2 is + level (NPL).

DURING TAG '83' TIME

Tag Bus Bits 0, 1, and 2 are – level (NPL).
Tag Bus Bit P is + level (NPL).

See OPER 90 for additional theory.

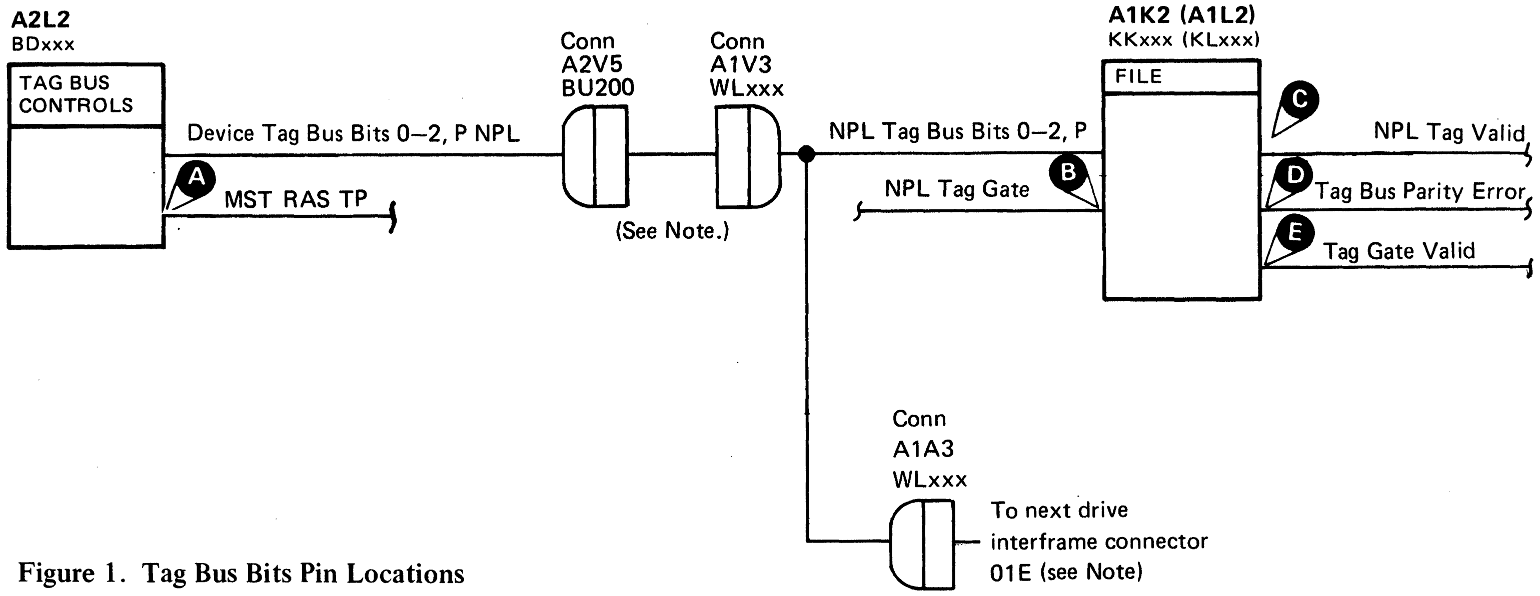
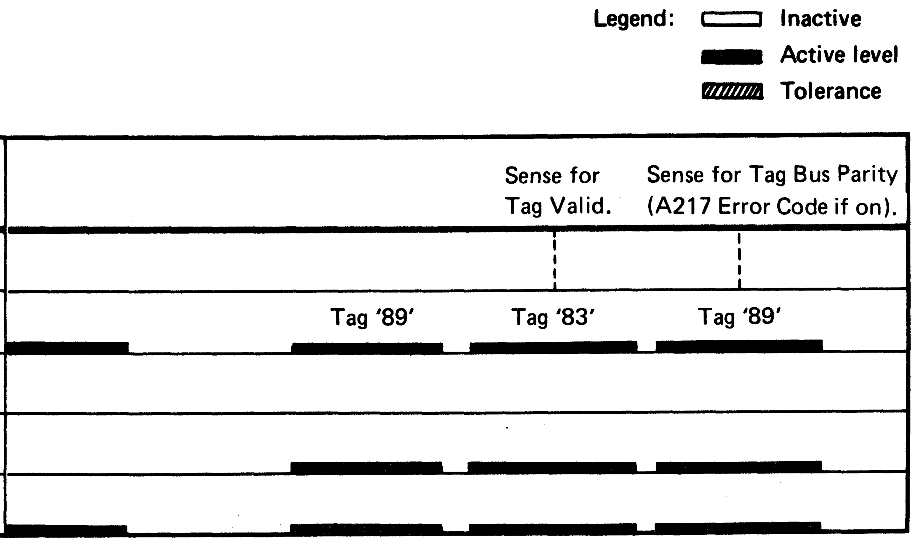


Figure 1. Tag Bus Bits Pin Locations

Bits	Device Tags Bus NPL A2L2 BD220	NPL Tag Bus A1K2 (A1L2) KK100 (KL100)
0	J10	J05
1	P03	G03
2	J12	G05
P	J04	G04

Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

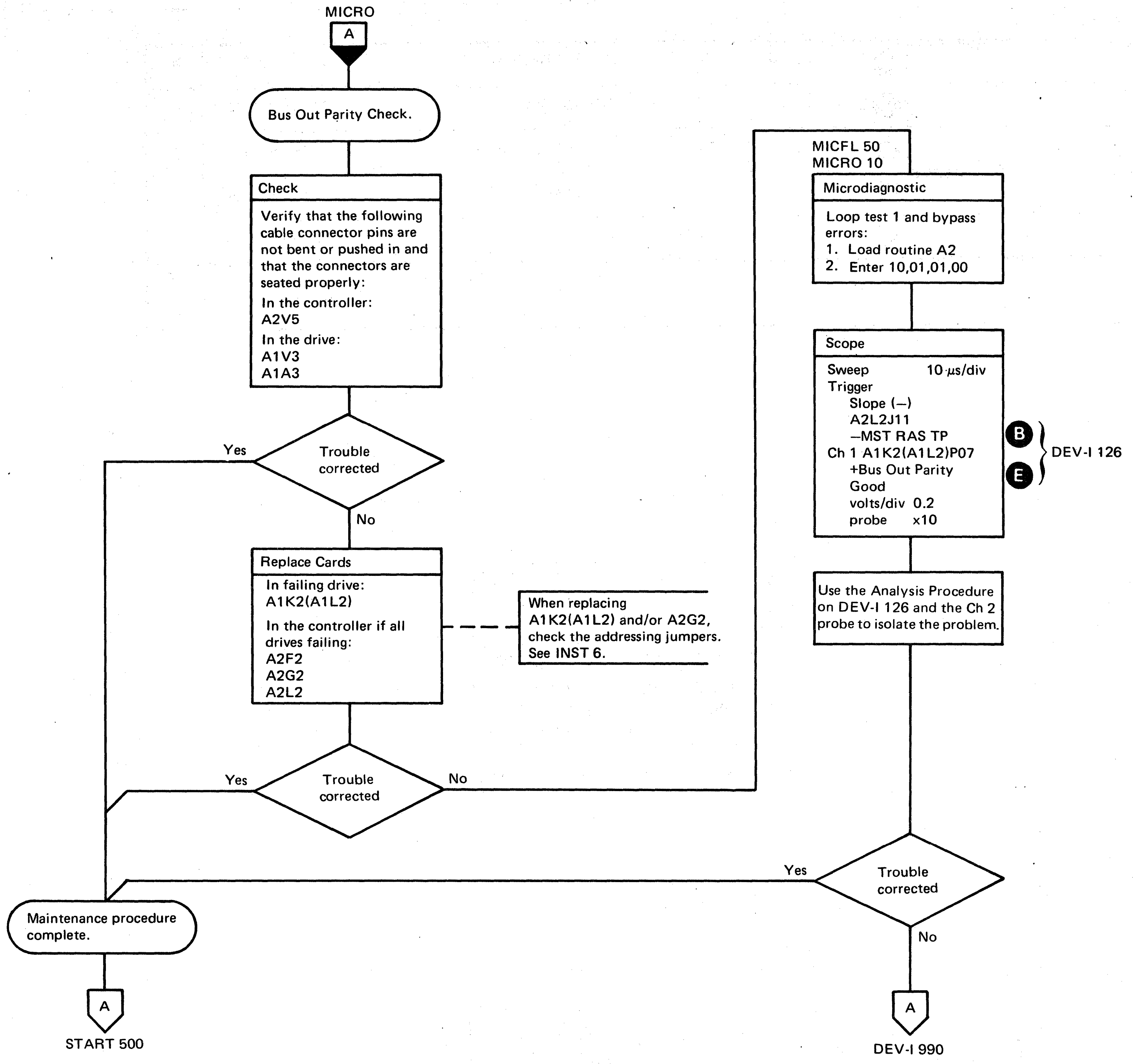
Chart Line No.	Line Name	ALD	Test Point	
1	–MST RAS TP	BD100	A2L2 J11	Ⓐ
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓑ
3	–Tag Bus Parity Error	KK120 (KL120)	A1K2 (A1L2) P05	Ⓓ
4	–Tag Gate Valid	KK190 (KL190)		Ⓔ
5	+NPL Tag Valid	KK140 (KL140)	A1K2 (A1L2) B07	Ⓒ



CC0122 Seq. 1 of 2	2358348 Part No.	441300 31 Mar 76	441303 30 Jul 76			

BUS OUT PARITY CHECK

A drive is selected and no +NPL Tag Valid Ⓕ was returned to the controller because of a Bus Out Parity error.



Bus Out Parity Check.

Check

Verify that the following cable connector pins are not bent or pushed in and that the connectors are seated properly:

In the controller:
A2V5

In the drive:
A1V3
A1A3

Replace Cards

In failing drive:
A1K2(A1L2)

In the controller if all drives failing:
A2F2
A2G2
A2L2

When replacing A1K2(A1L2) and/or A2G2, check the addressing jumpers. See INST 6.

Microdiagnostic

Loop test 1 and bypass errors:
1. Load routine A2
2. Enter 10,01,01,00

Scope

Sweep 10 µs/div
Trigger
Slope (–)
A2L2J11
–MST RAS TP
Ch 1 A1K2(A1L2)P07
+Bus Out Parity
Good
volts/div 0.2
probe x10

Use the Analysis Procedure on DEV-I 126 and the Ch 2 probe to isolate the problem.

Maintenance procedure complete.

3350	CC0122 Seq. 2 of 2	2358348 Part No.	441300 31 Mar 76	441303 30 Jul 76			

BUS OUT PARITY CHECK

Circuit Description

A Bus Out Parity error has occurred preventing +NPL Tag Valid **F**.

Analysis Procedure

The +Bus Out Parity Good **E** line of KK120 (KL120) should be + level (MST-1) during Tag '83' time. If not, scope the NPL Outbus bits in Figure 2 **C**.

At Tag '83' time, the Bus Out bit pattern is dependent on the controller address. See Figure 1 to determine the bit pattern.

Controller address may be determined by checking the address jumpers on A2G2 (see INST 6).

Invert Bus Out Par Bit **A** should be inactive.

Figure 1. Controller Address Bits

Controller Address	Bus Out Active Bits at Tag '83' time
0	3
1	2, 3, P
2	1, 3, P
3	1, 2, 3
4	0, 3, P
5	0, 2, 3
6	0, 1, 3
7	0, 1, 2, 3, P

See OPER 90 for additional theory.

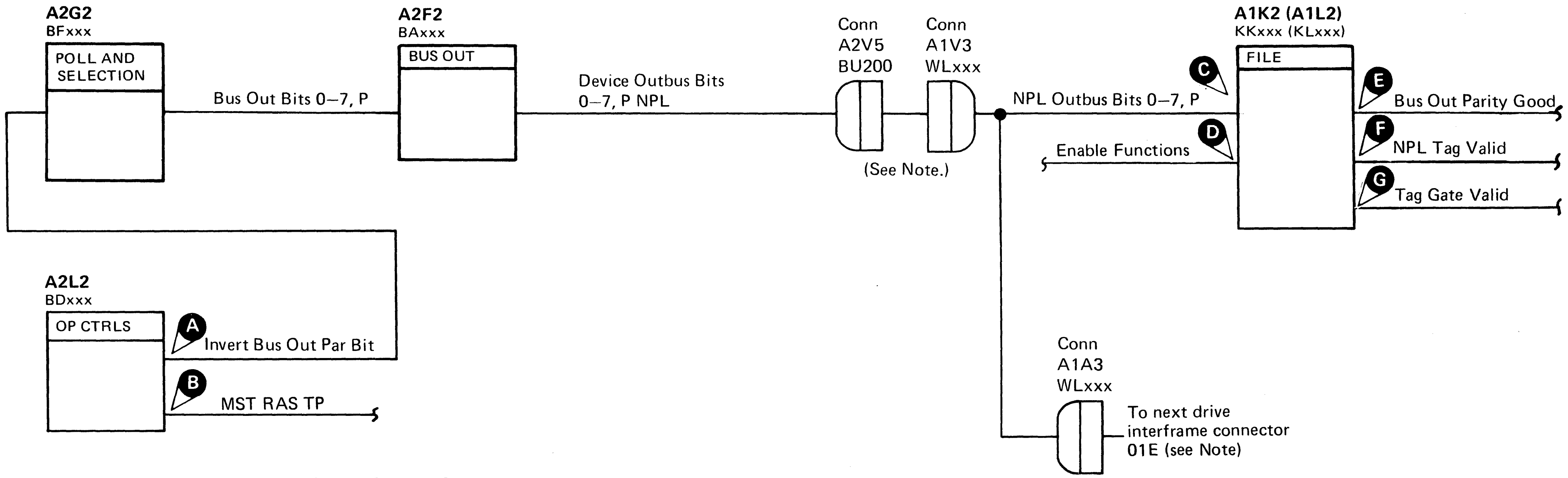
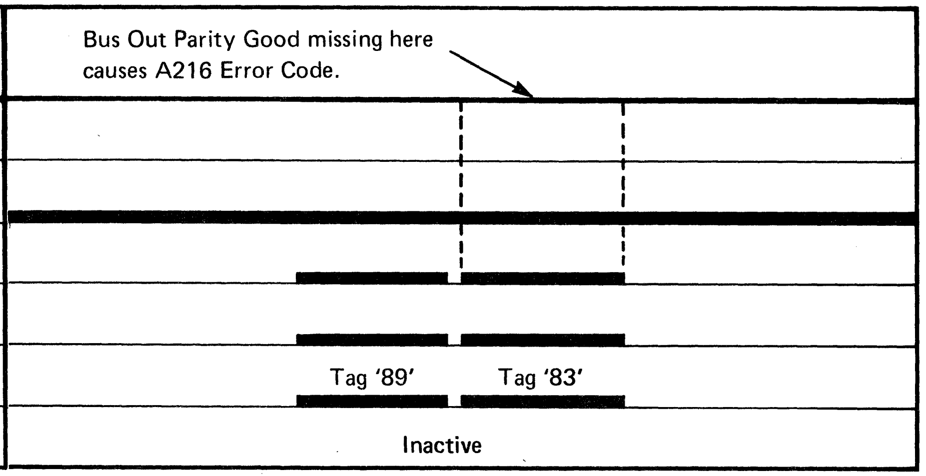


Figure 2. Bus Out Bits Pin Locations

Bits	–Bus Out A2G2 BF130	+NPL Outbus **C** A1K2 (A1L2) KK100 (KL100)	+Device Outbus A2F2 BA110
0	P02	M07	P10
1	J13	U11	P12
2	M02	U12	U02
3	P05	S11	S03
4	P04	U04	S12
5	P06	S04	U12
6	P11	S02	U05
7	M10	M09	U09
P	M11	U03	M07

Legend:
▭ Inactive
▬ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	–MST RAS TP	BD100	A2L2 J11	**B**
2	+Bus Out Parity Good	KK190 (KL190)	A1K2 (A1L2) P07	**E**
3	–Tag Gate Valid	KK190 (KL190)		**G**
4	+Enable Functions	KK150 (KL150)	A1K2 (A1L2) G10	**D**
5	+NPL Tag Valid	KK140 (KL140)	A1K2 B07	**F**
6	–Invert Bus Out Par Bit	BD170	A2L2 J06	**A**

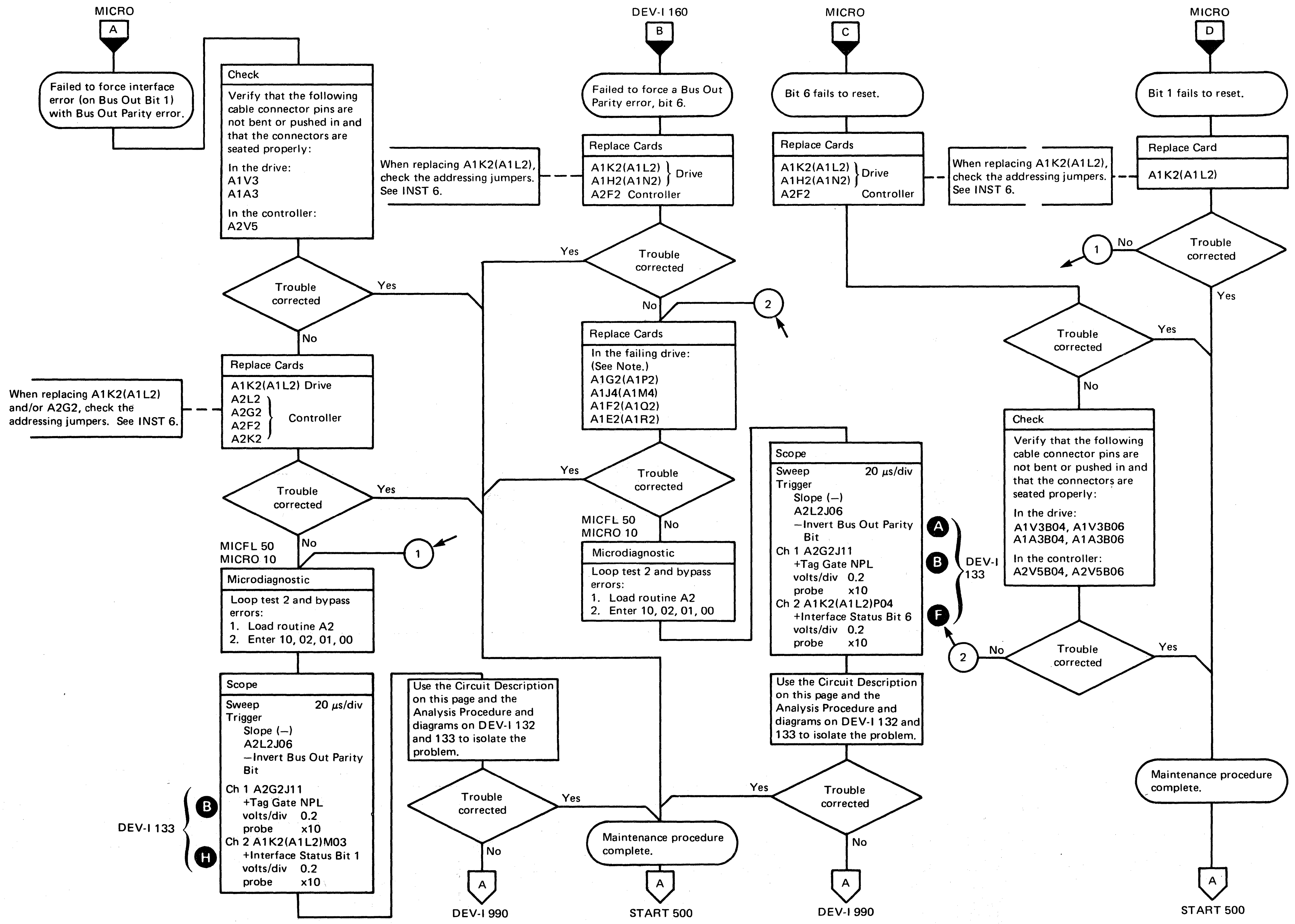


Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

BUS OUT PARITY ERROR

Circuit Description

The microdiagnostic issues Tag '09' Bus '22' to invert the Bus Out Parity Bit, which causes a Bus Out Parity Check (Bus Out Parity Good Ⓙ is inactive). Bus Out Parity Check is gated to the NPL Inbus Bit 1 Ⓜ as Interface Status Bit 1 Ⓗ at Tag '84' time and as Interface Status Bit 6 Ⓕ at Tag '89' time. Tag '89' also resets the Bus Out Parity Check. Tag '84' is issued again to check that Interface Status Bit 1 is off and Tag '89' is issued to check that Interface Status Bit 6 is off.



Note: *(See DEV-I 184.) Each bit on the Device Bus In is affected by six different cards in each drive.*

Drive A		Drive B	
A1E2 *A1F2* *A1G2* *A1J4* *A1K2*	*DOT OR at A1H2*	*A1R2* *A1Q2* *A1P2* *A1M4* *A1L2*	*DOT OR at A1N2*

Any one of these cards can cause a bit to remain active or inactive. If the error remains after replacing or swapping cards, perform the following:

1. *ALWAYS ACTIVE BIT — Scope the failing line.*
   - a. *If the bit line is at a + level (MST-1), remove the cards one at a time until the line drops to — level (MST-1). If all cards are removed and the bit line is still active, look for tight wire wraps, bent pins, etc.*
   - b. *If the bit line is still at a — level (MST-1), return to the flowchart.*
2. *ALWAYS INACTIVE BIT — Return to the flowchart.*

Analysis Procedure (A224 Error Code)

The microdiagnostic forces an Interface Check (NPL Inbus Bit 1) Ⓜ by inverting the Bus Out Parity Bit. NPL Inbus Bit 1 was not on when checked with a Read Status command (Tag '84').

+Interface Status Bit 1 Ⓗ is set when:

–Gate Machine Status is active (KK140, KL140).
+Bus Out Parity Good Ⓙ is inactive.
+Set Read*Write Ⓚ is inactive.

+Bus Out Parity Good is inactive because –Invert Bus Out Parity Bit Ⓐ is active.

NPL Tag Bus Bit 1 Ⓓ inactive (Figure 2) causes a decode error (Tag '88' decodes as Tag '89') allowing the Interface Check to reset before the Sense Interface command is issued.

Analysis Procedure (A225 Error Code)

The microdiagnostic forces a Bus Out Parity Check (NPL Inbus Bit 6 Ⓛ). NPL Inbus Bit 6 was not on when checked with a Sense Interface command (Tag '89').

+NPL Inbus 6 is activated when +Interface Status Bit 6 Ⓕ is active.

Analysis Procedure (A226 Error Code)

The microdiagnostic indicates a failure to reset the Interface Status Bit 1 latch (KK190, KL190) after a Sense Interface command (Tag '89').

Analysis Procedure (A227 Error Code)

The microdiagnostic indicates that the Bus Out Parity Check latch is still on after a Sense Interface command (Tag '89').

Tag '89' resets the Bus Out Parity Check latch after gating Interface Status Bit 6 Ⓕ to the NPL Inbus Bit 6 Ⓛ.

Suspect at the first Tag '89' time:

- Tag Bus Parity latch does not reset.
- Device Outbus Parity is bad, all NPL Outbus bits should be off ('00'), and the P bit on. See Figure 1 for scope points. Scope at Ⓒ.
- Sense Status 4 Ⓖ or Sense Status 0 Ⓔ is active causing NPL Inbus Bit 6 Ⓛ to be active.

See OPER 90 for additional theory.

Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

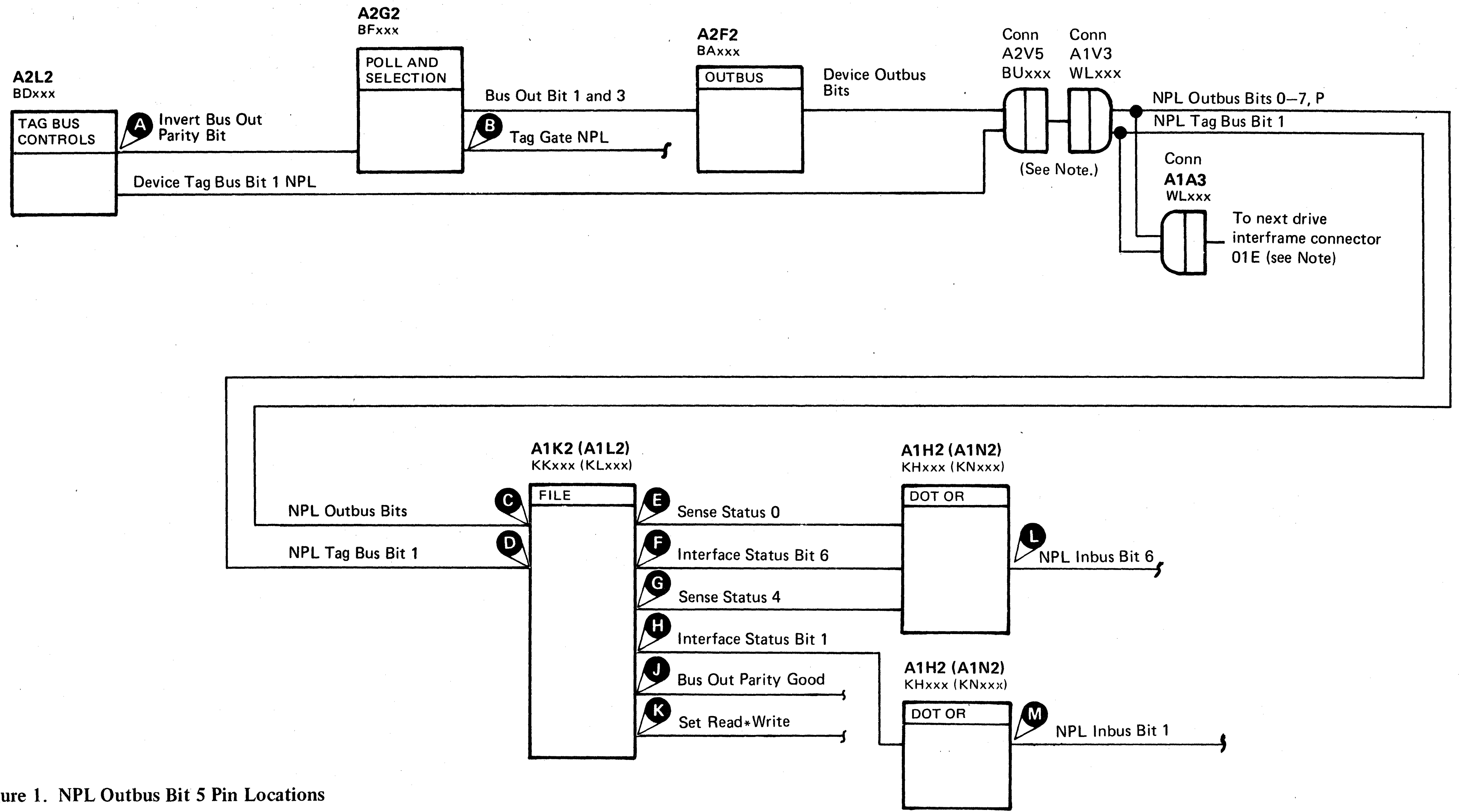


Figure 1. NPL Outbus Bit 5 Pin Locations

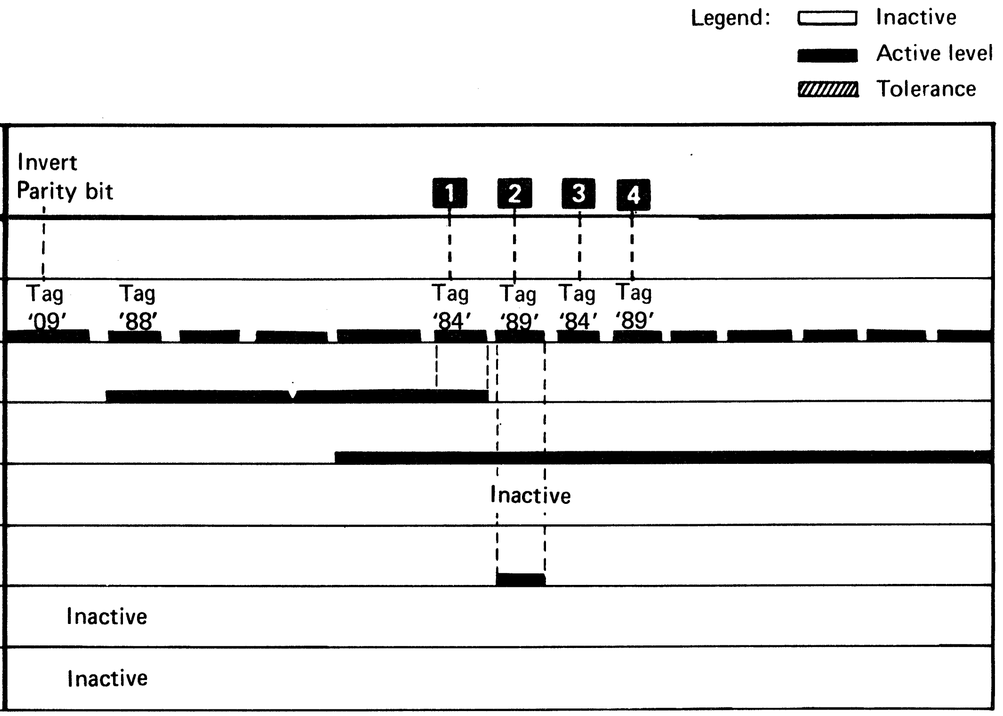
Bits	+Device Outbus A2F2 BA110	+NPL Outbus A1K2 (A1L2) KK100 (KL100) Ⓒ
0	P10	M07
1	P12	U11
2	U02	U12
3	S03	S11
4	S12	U04
5	U12	S04
6	U05	S02
7	U09	M09
P	M07	U03

Figure 2. NPL Tag Bus Bit 1 Pin Locations

Bit	–Device Tag Bus NPL NPL A2L2 BD220	Conn A2V5	Conn A1V3	+NPL Tag Bus A1K2 (A1L2) KK100 (KL100) Ⓓ
1	P03	D03	D03	G03

BUS OUT PARITY ERROR

Chart Line No.	Line Name	ALD	Test Point	
1	—Invert Bus Out Parity Bit	BD170	A2L2 J06	Ⓐ
2	+Tag Gate NPL	BF130	A2G2 J11	Ⓑ
3	+Interface Status Bit 1	KK190 (KL190)	A1K2 (A1L2) M03	Ⓗ
4	+Bus Out Parity Good	KK120 (KL120)	A1K2 (A1L2) P07	Ⓙ
5	+Set Read*Write	KK170 (KL170)	A1K2 (A1L2) U13	Ⓚ
6	+Interface Status Bit 6	KK190 (KL190)	A1K2 (A1L2) P04	Ⓕ
7	—Sense Status 4	KK170 (KL170)	A1K2 (A1L2) S08	Ⓖ
8	—Sense Status 0	KH110 (KN110)	A1H2 (A1N2) J03	Ⓔ



1 Interface Status Bit 1 must be on at Tag '84' time or an A224 Error Code occurs.

2 Resets Interface Status Bits 1 and 6 and sets Interface Status Bit 6 on.
Interface Status Bit 6 must be on at Tag '89' time or an A225 Error Code occurs.

3 Interface Status Bit 1 must be off at Tag '84' time or an A226 Error Code occurs.

4 Interface Status Bit 6 must be off at Tag '89' time or an A227 Error Code occurs.

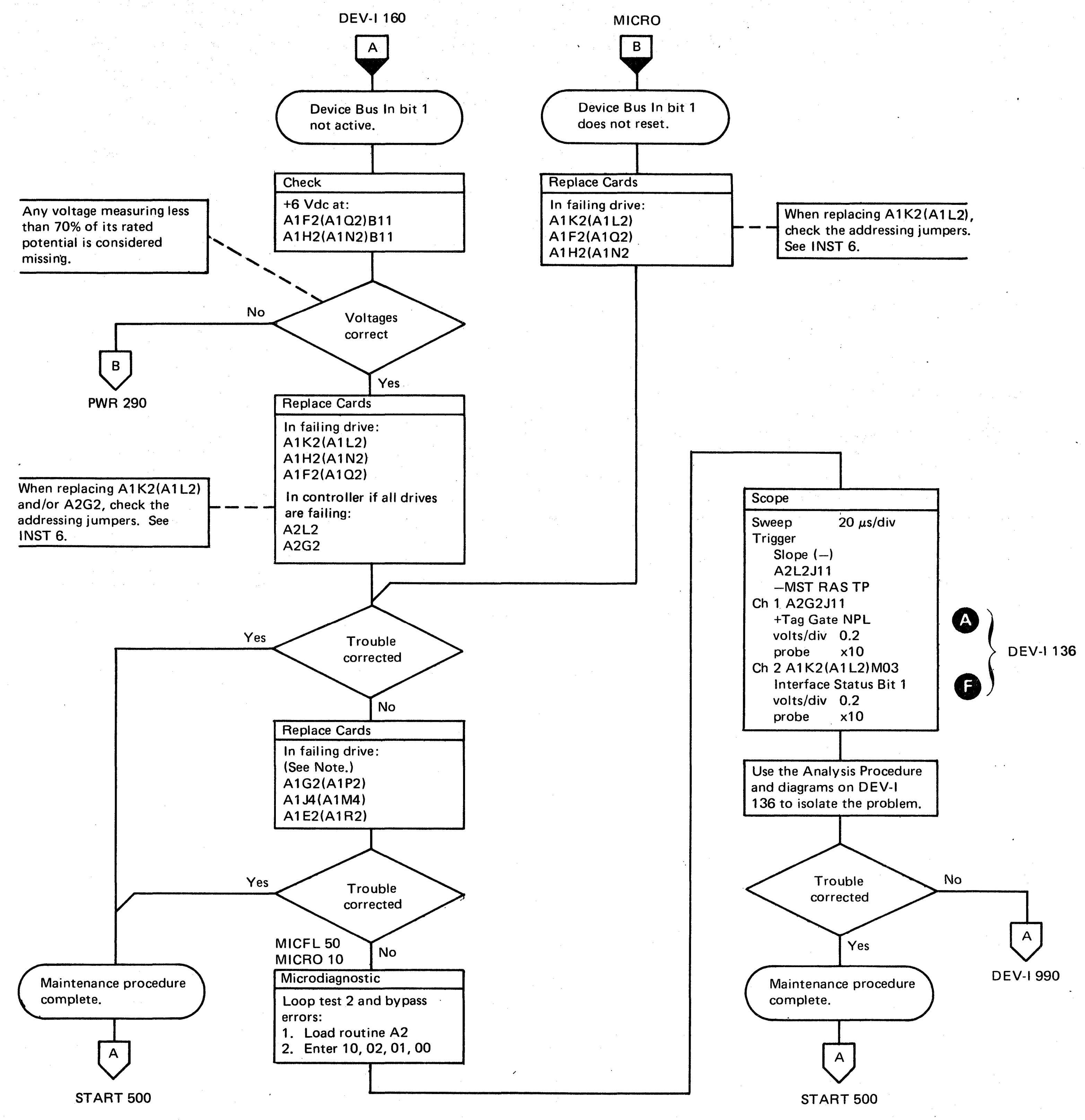
3350	CC0133 Side 1 of 2	2358351 Part No.	441300 31 March 76	441303 30 Jul 76			

Note: *(See DEV-I 184.) Each bit on the Device Bus In is affected by six different cards in each drive.*

Drive A		Drive B	
A1E2	*DOT OR at A1H2*	*A1R2*	*DOT OR at A1N2*
A1F2		*A1Q2*	
A1G2		*A1P2*	
A1J4		*A1M4*	
A1K2		*A1L2*	

Any one of these cards can cause a bit to remain active or inactive. If the error remains after replacing or swapping cards, perform the following:

1. *ALWAYS ACTIVE BIT – Scope the failing line.*
   a. *If the bit line is at a + level (MST-1), remove the cards one at a time until the line drops to – level (MST-1). If all cards are removed and the bit line is still active, look for tight wire wraps, bent pins, etc.*
   b. *If the bit line is still at a – level (MST-1), return to the flowchart.*
2. *ALWAYS INACTIVE BIT – Return to the flowchart.*



BUS IN PARITY

Analysis Procedure (A220 Error Code)

The microdiagnostic forces an Interface Check (NPL Inbus Bit 1) by inverting the Tag Bus Parity Bit. The NPL Inbus bit 1 was not on when checked with a Read Status command (Tag '84').

+NPL Inbus Bit 1 is activated when +Interface Status Bit 1 Ⓕ is active.

+Interface Status Bit 1 is active when:
- –Gate Machine Status is active (KK190, KL190).
- –Tag Bus Parity Error TP Ⓒ is active.
- +Selected Ⓓ is active.

–Tag Bus Parity Error is activated when the microprogram inverts the Tag Bus Bit P.

If Diag Set is active, –Gate Machine Status is held inactive, not allowing +MST Inbus Bit 1 to become active (KK190, KL190).

If Sense Interface is decoded before the Tag '89' is issued, the error latches are reset.

Analysis Procedure (A222 Error Code)

The microdiagnostic indicates a failure to reset Interface Status Bit 1 Ⓕ latch after a Sense Interface command, Tag '89' (KK190, KL190). The following conditions cause this error:

- –Sense Status 2 Ⓖ held active causes HDA Status Bit 1 to be active.
- –Sense Status 3 Ⓔ held active causes Access*Check Status Bit 1 to be active.

See OPER 90 for additional theory.

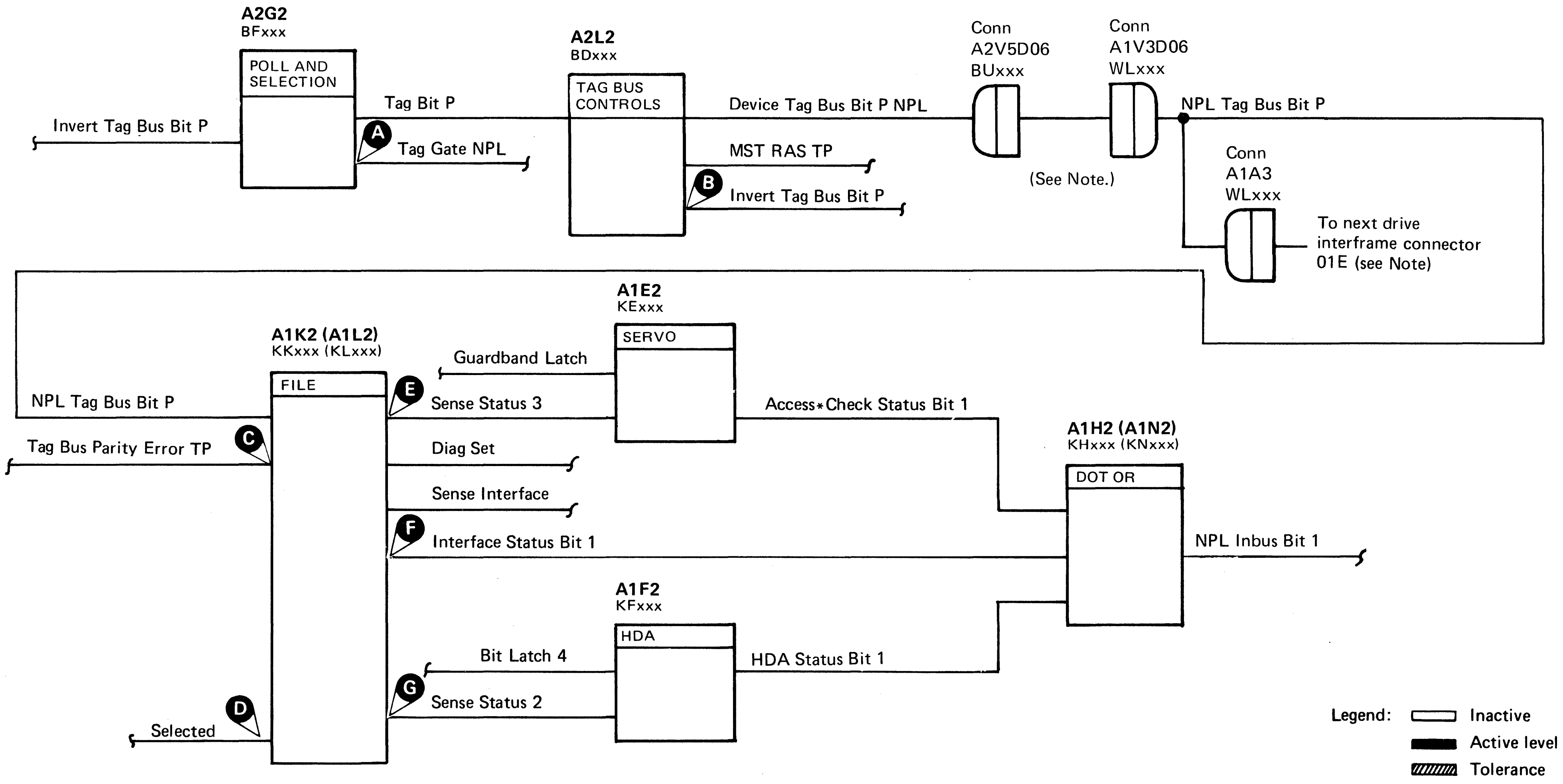
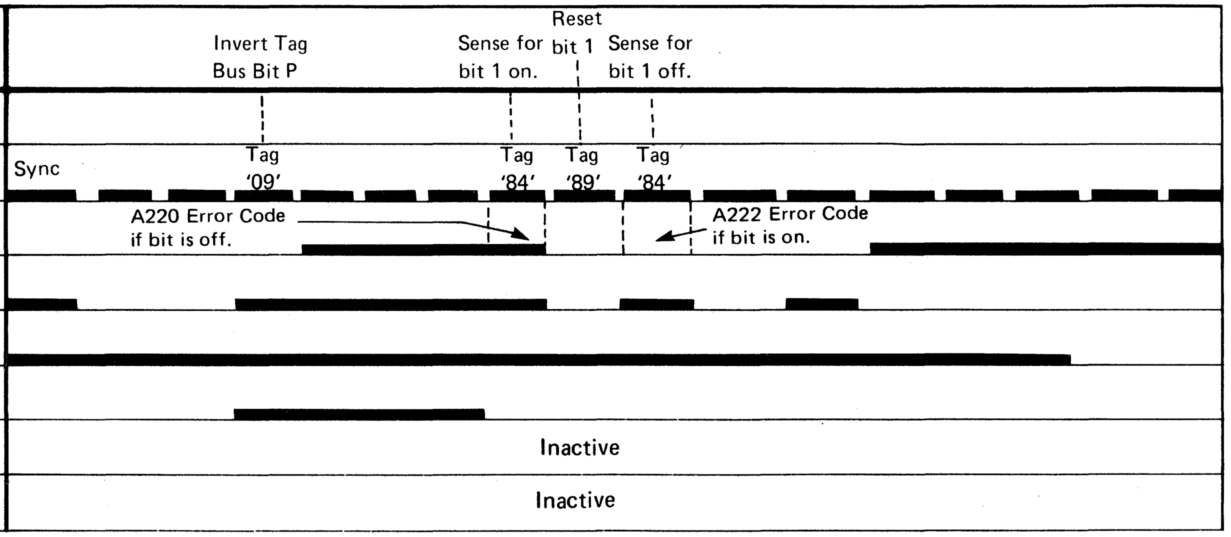
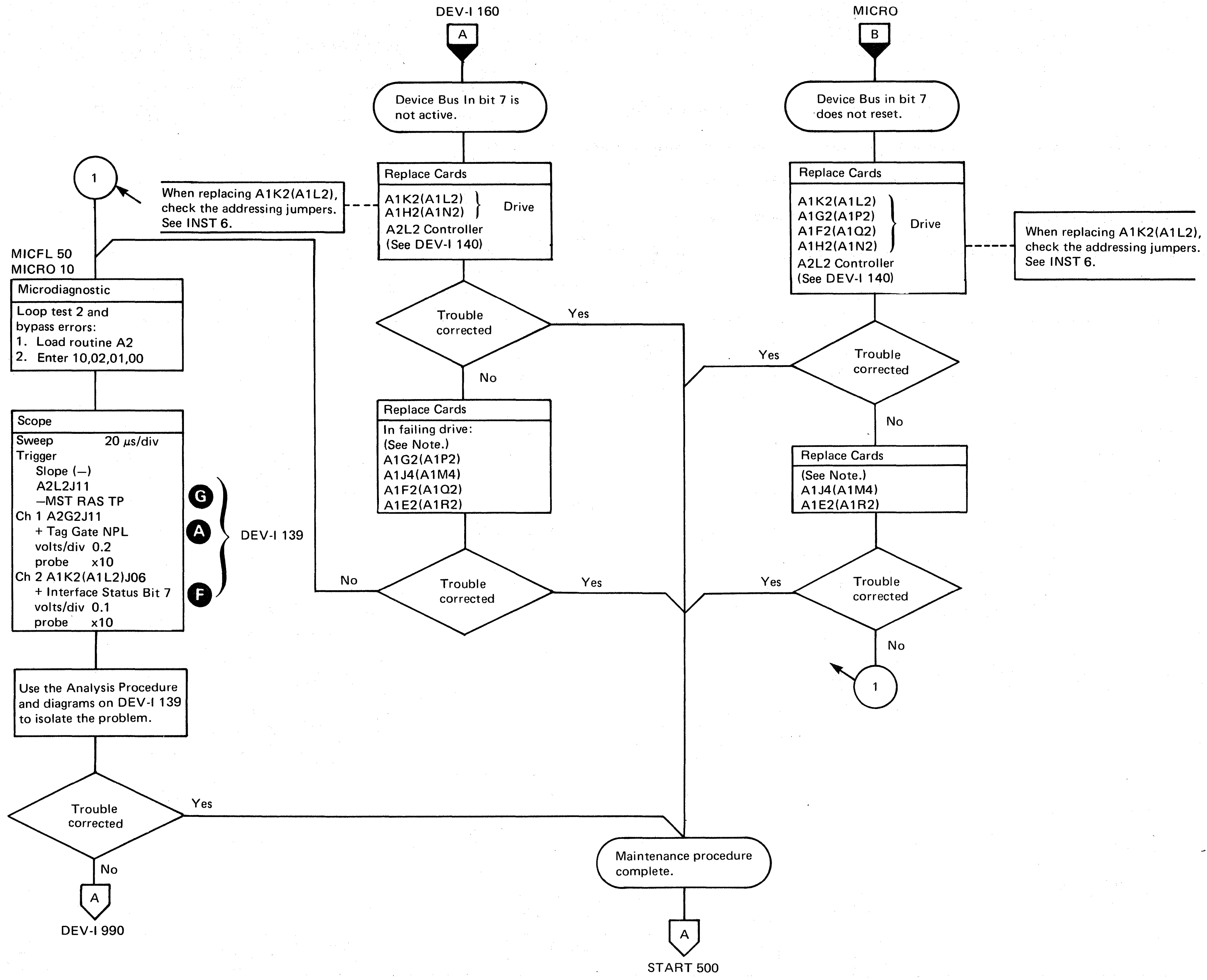


Chart Line No.	Line Name	ALD	Test Point	
1	–MST RAS TP	BD100	A2L2 J11	
2	+Tag Gate NPL	BF130	A2G2 J11	Ⓐ
3	+Interface Status Bit 1	KK190 (KL190)	A1K2 (A1L2) M03	Ⓕ
4	–Tag Bus Parity Error TP	KK120 (KL120)	A1K2 (A1L2) P05	Ⓒ
5	+Selected	KH100 (KN100)	A1K2 (A1L2) G12	Ⓓ
6	–Invert Tag Bus Bit P	BD170	A2L2 J07	Ⓑ
7	–Sense Status 2	KK170 (KL170)	A1K2 (A1L2) U06	Ⓖ
8	–Sense Status 3	KK170 (KL170)	A1K2 (A1L2) U09	Ⓔ



Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*



Note: (See DEV-I 184). Each bit on the Device Bus In is affected by six different cards in each drive.

Drive A		Drive B	
A1E2 *A1F2* *A1G2* *A1J4* *A1K2*	*DOT OR at A1H2*	*A1R2* *A1Q2* *A1P2* *A1M4* *A1L2*	*DOT OR at A1N2*

Any one of these cards can cause a bit to remain active or inactive. If the error remains after replacing or swapping cards, perform the following:

1. *ALWAYS ACTIVE BIT – Scope the failing line.*
   - *a. If the bit line is at a + level (MST-1), remove the cards one at a time until the line drops to – level (MST-1). If all cards are removed and the bit line is still active, look for tight wire wraps, bent pins, etc.*
   - *b. If the bit line is still at a – level (MST-1), return to the flowchart.*
2. *ALWAYS INACTIVE BIT – Return to the flowchart.*

BUS IN PARITY

Analysis Procedure (A221 Error Code)

The microdiagnostic forces a Tag Bus Parity Check (Interface Status Bit 7). The Interface Status Bit 7 was not on when checked with a Sense Interface command.

+NPL Inbus Bit 7 is activated when +Interface Status Bit 7 Ⓕ is active.

+Interface Status Bit 7 is activated when:
- –Tag Bus Parity Error Ⓒ is active.
- +Selected Ⓓ is active.
- +Sense Interface Ⓔ is active.

Analysis Procedure (A223 Error Code)

The microdiagnostic indicates a failure to reset Interface Status Bit 7 Ⓕ after a Sense Interface command (Tag '89'). If NPL Tag Bus Bit P Ⓑ is active, it causes a Tag Bus Parity Check, which sets Interface Status Bit 7 on.

The following conditions also cause this error:

- –Sense Status 0 is held active (KG190).
- –Sense Status 1 is held active (KF130).
- –Sense Target Reg is held active (KG190).
- –Sense Status A is held active (KG190).
- –Sense Status 3 is held active (KF130).
- –Selected Tag Gate is held active (BD100).
- –Bus Out Bit 3 is held inactive (BD100).

See OPER 92 for additional theory.

Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

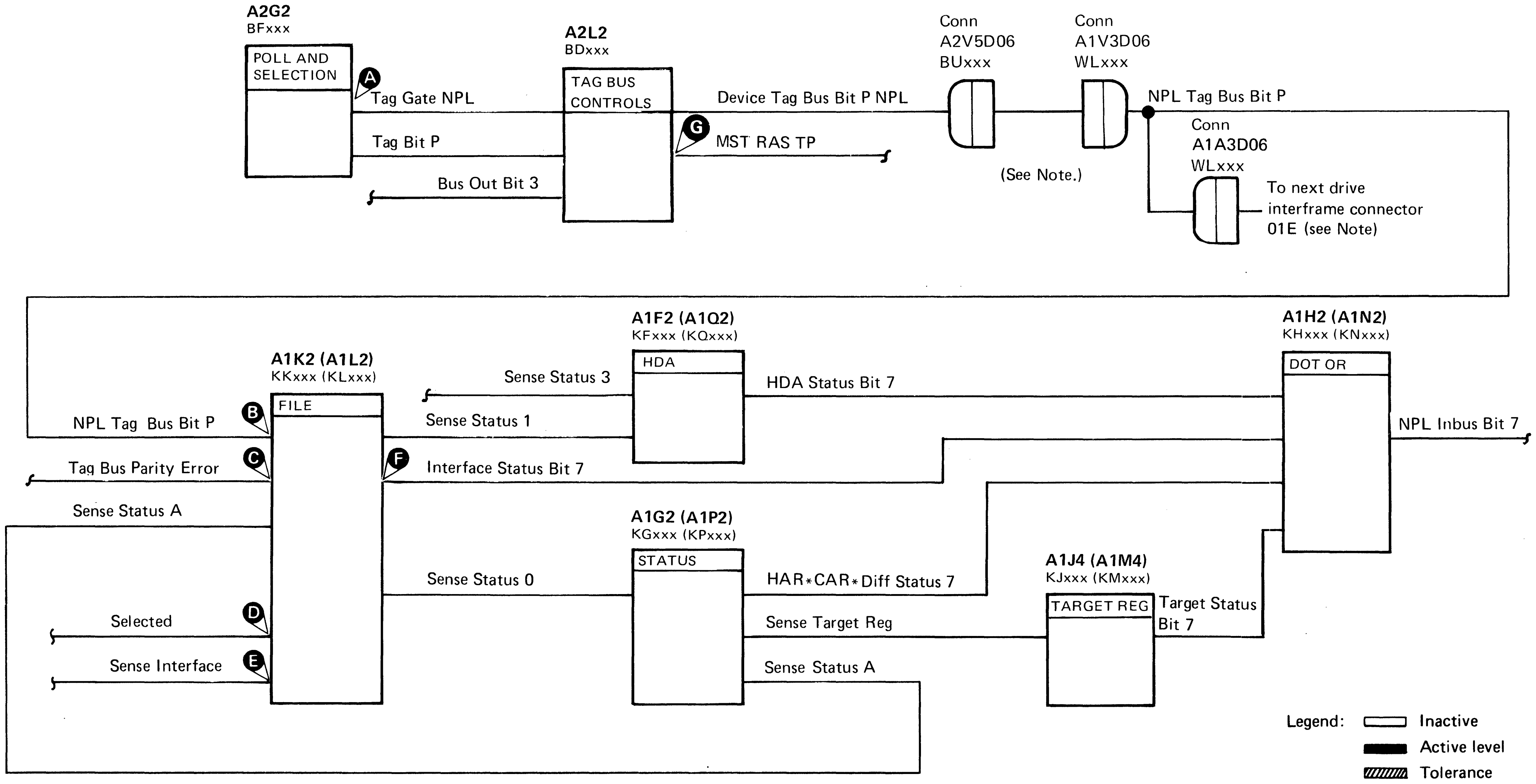
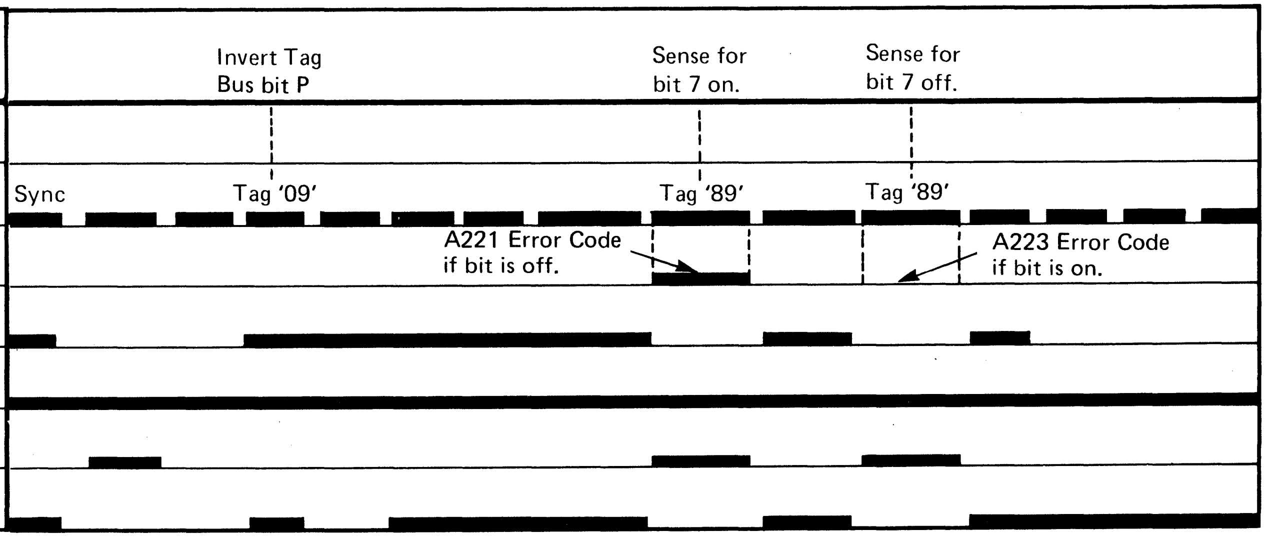


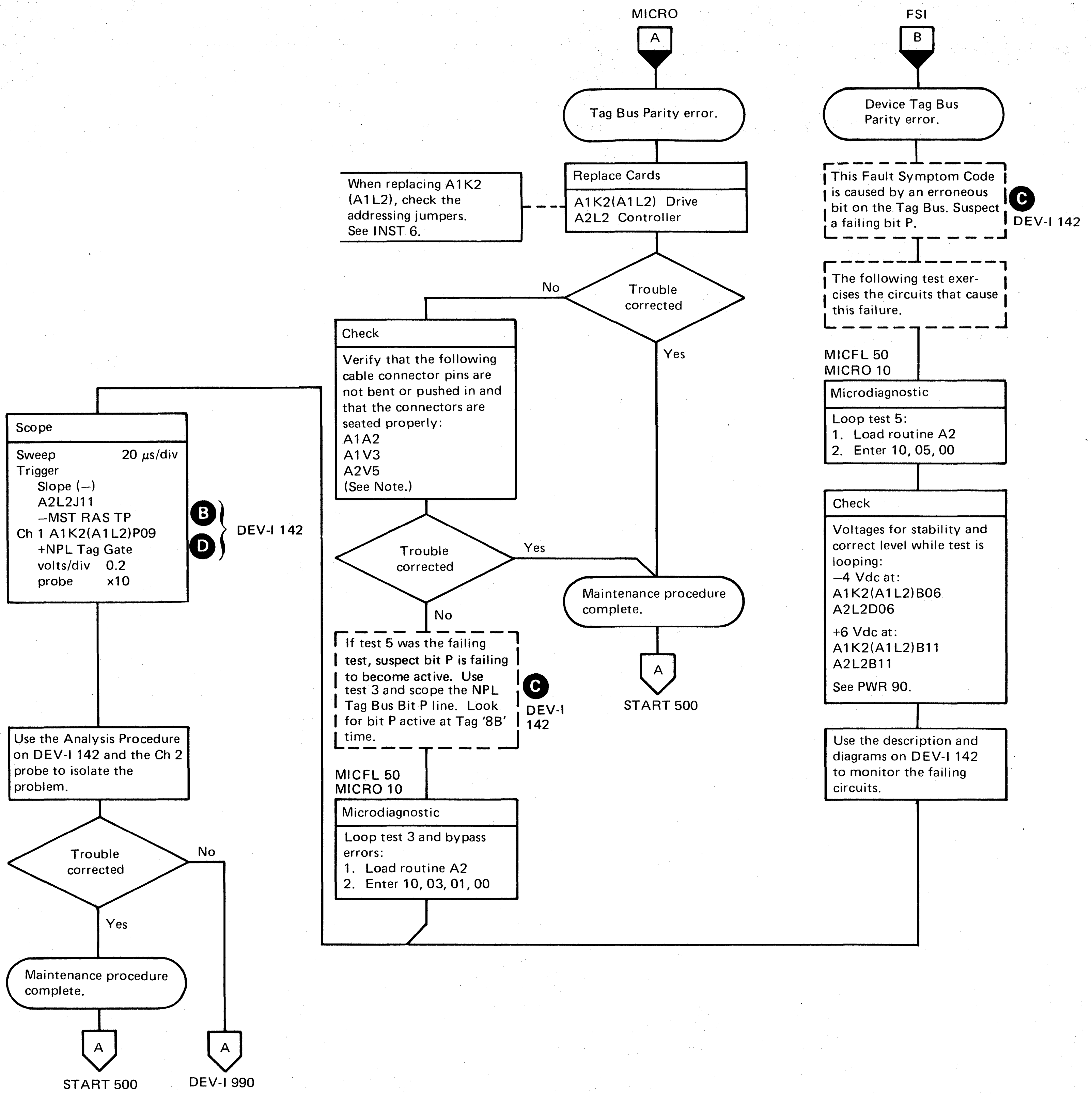
Chart Line No.	Line Name	ALD	Test Point	
1	–MST RAS TP	BD100	A2L2 J11	Ⓖ
2	+Tag Gate NPL	BF130	A2G2 J11	Ⓐ
3	+Interface Status Bit 7	KK190 (KL190)	A1K2 (A1L2) J06	Ⓕ
4	–Tag Bus Parity Error	KK190 (KL190)	A1K2 (A1L2) P05	Ⓒ
5	+Selected	KK190 (KL190)	A1K2 (A1L2) G12	Ⓓ
6	+Sense Interface	KK190 (KL190)	A1K2 (A1L2) J09	Ⓔ
7	+NPL Tag Bus Bit P	KK100 (KL100)	A1K2 (A1L2) G04	Ⓑ



TAG BUS PARITY

Note: *A terminator card is located in A1A3 in the last module of the string. The A1A3 and A1A4 connectors can be pulled in any module and the terminator moved to facilitate isolation to a drive module or cable. See DEV-I 162.*

If a C2 Module is installed, the terminators exist on the offline controller driver or receiver card.



3350

CC0139 Seq. 2 of 2	2358353 Part No.	441300 31 Mar 76	441301 1 June 76	441303 30 Jul 76		

TAG BUS PARITY

Circuit Description

The microdiagnostic issues a Tag '8F' Bus '00' (Tag Bits 0, 1, and 2 are on and bit P is off). There should be no Tag Bus Parity error sensed and Interface Status Bit 7 should be off at Tag '89' time.

Analysis Procedure

If a Tag Bus Parity error occurs at Tag '8F' time, scope the Device Tag Bus Bits 0-2, P NPL Ⓐ and determine why the Tag Bus Parity Error Ⓖ line is active (it should not be active for this test).

Tag Bits 0, 1, 2, and P are on or off depending on the Tag issued. Check for the on/off condition only at Tag '8F' time.

If the Tag Bus Parity Error Ⓖ line is not active at Tag '8F' time (this error indicates that Interface Status Bit 7 Ⓔ was on at Tag '89' time and should be off), scope the Interface Status Bit 7 line.

See OPER 92 for additional theory.

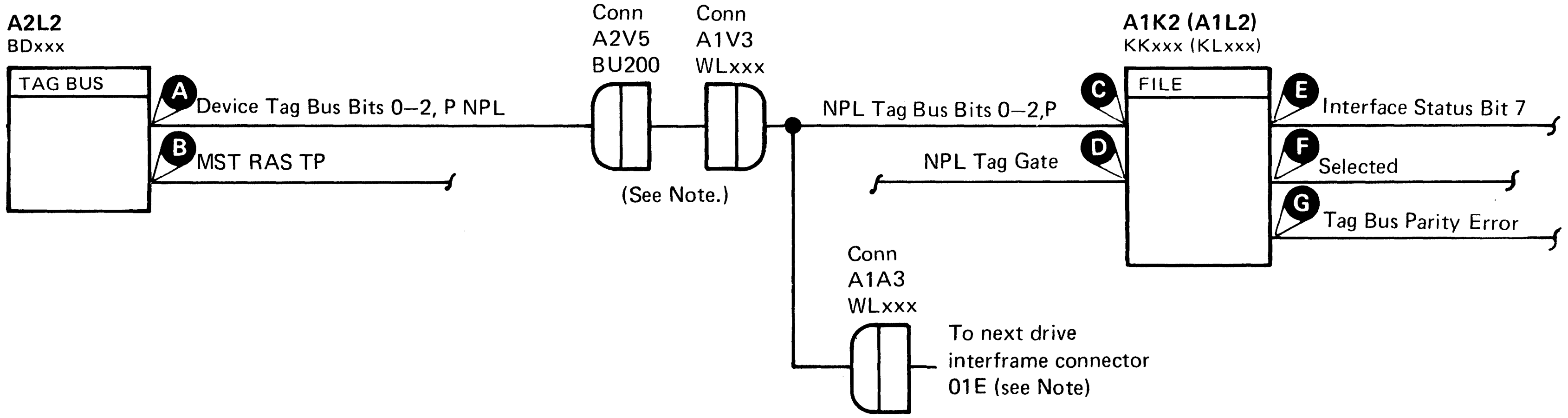
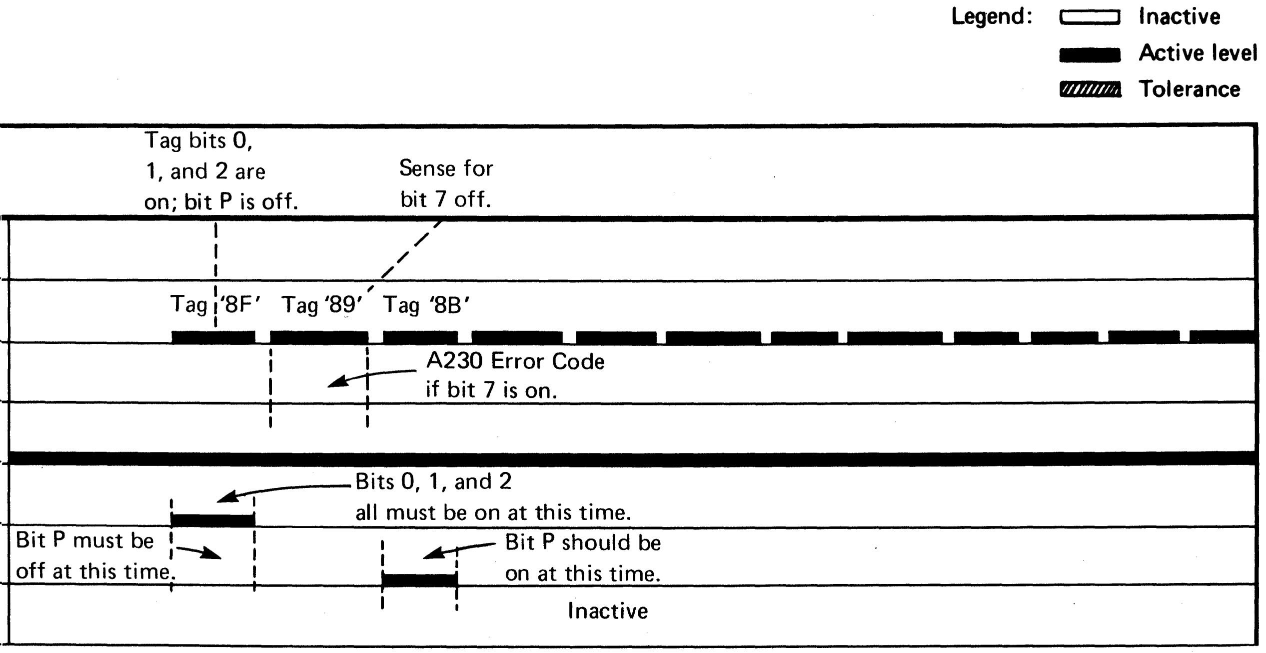


Figure 1. Tag Bus Bits 0-2, P Pin Locations

Bits	+Device Tag Bus NPL A2L2 Ⓐ	+NPL Tag Bus A1K2 (A1L2) Ⓒ
0	J10	J05
1	P03	G03
2	J12	G05
P	J04	G04

Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

Chart Line No.	Line Name	ALD	Test Point	
1	–MST RAS TP	BD100	A2L2 J11	Ⓑ
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓓ
3	+Interface Status Bit 7	KK190 (KL190)	A1K2 (A1L2) J06	Ⓔ
4	+Selected	KK190 (KL190)	A1K2 (A1L2) G12	Ⓕ
5	+NPL Tag Bus Bits 0–2	KK100 (KL 100)	See Figure 1.	Ⓒ
6	+NPL Tag Bus Bit P	KK100 (KL100)	A1K2 (A1L2) G04	Ⓒ
7	–Tag Bus Parity Error	KK190 (KL190)	A1K2 (A1L2) P05	Ⓖ



CC0142 Seq. 1 of 2	2358354 Part No.	441300 31 Mar 76	441301 1 June 76	441303 30 Jul 76		

DEVICE BUS OUT PARITY

ISOLATION PROCEDURE

See the diagram on DEV-I 152 for referenced test points.

1. Remove A1A3 connector at Ⓒ.
2. Move the terminator card from the last module Ⓔ to Ⓒ.
3. Turn on the CE Mode switch for Drive A in the Control Module and turn off the CE Mode switches for all other drives in the string.
4. Push the Attention pushbutton on all drives taken out of CE Mode.

Microdiagnostic Setup

Run microdiagnostic routine A2.

1. Load routine A2.
2. Enter 10,00.

Microdiagnostic fails?

YES

Troubleshoot the drive in CE Mode.

NO

Remove terminators and replace connector; remove connector from next module in string at Ⓓ and insert terminator; rerun microdiagnostics.

Note 1: *An A1K2(A1L2) Ⓑ card may cause all drives to fail. (If a C2 Module is installed, the A2F2 card in the off-line controller can also cause failure.) To determine if a card is causing the problem, perform the following actions:*

1. *Leave the A1K2 Ⓑ card in the A2 Module.*
2. *Remove the A1K2(A1L2) card from all other drives in the string.*
3. *Run the failing microdiagnostic on Drive A of the A2 Module. (See the diagram on DEV-I 152.)*

   To loop failing test:
   1. *Load routine A2*
   2. *Enter 10,XX,00*
      (XX = Failing test)

Microdiagnostic fails?

NO

Install A1K2(A1L2) cards one at a time and run the micro-diagnostic to isolate the failing card.

YES

1. *Swap the A1K2 card with an A1K2 card from another drive.*
2. *Rerun the failing microdiagnostic.*

Microdiagnostic fails?

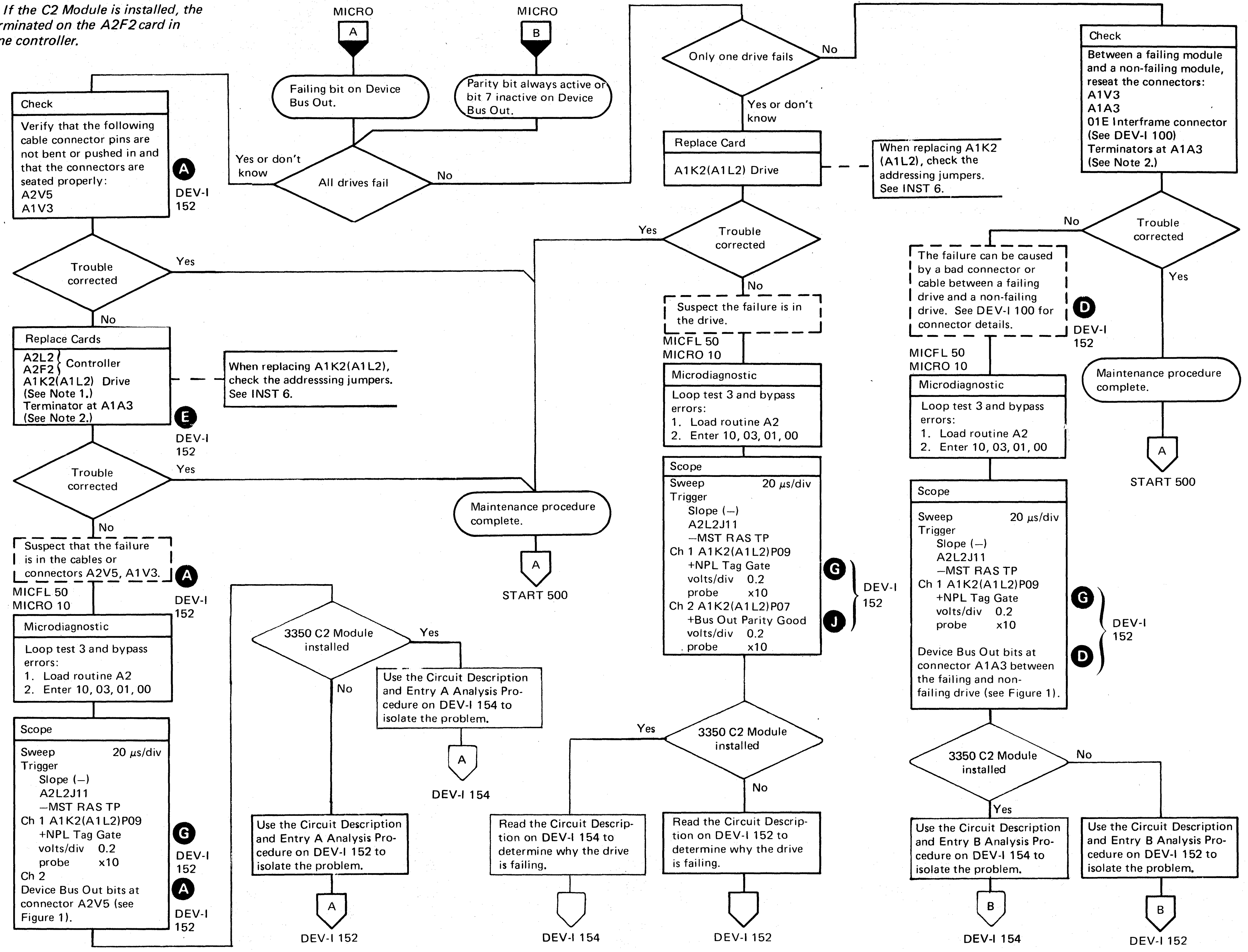
NO

Replace the bad card.

YES

Replace all cards and continue with the flowchart.

Note 2: *If the C2 Module is installed, the bus is terminated on the A2F2 card in the offline controller.*



3350	CC0142 Seq. 2 of 2	2358354 Part No.	441300 31 Mar 76	441301 1 June 76	441303 30 Jul 76		

DEVICE BUS OUT PARITY

Circuit Description

The microdiagnostic program sets HAR to '01' (Tag '8B') and senses the interface (Tag '89') for a Bus Out Parity Check. An A231 Error Code occurs if the Bus Out Parity Check is active; suspect that the failing line is an active P bit or an inactive 7 bit.

HAR is then set to 'FF' (Tag '8B') and sensed (Tag '89') for a Bus Out Parity Check. If any bits are missing, an A232 Error Code occurs.

A Sense Interface Ⓚ (Tag '89') gates Interface Status Bit 6 Ⓗ to the controller if Bus Out Parity Good Ⓙ is at a −level (MST-1).

Analysis Procedure

A

With the Ch 2 probe, scope all the Outbus Bits listed in Figure 1 (connector A2V5) and use the sequence chart to determine if the Outbus bits are correct at the Tag '8B' times.

If a bit is not correct, scope at the A2F2 card to locate the problem. If the bit is correct at the input to A2F2, suspect a shorted cable causing all drives to fail. Use the isolation procedure on DEV-I 150 to isolate the problem.

If the Outbus bits are correct, use the Ch 1 probe and scope the bits at connector A1V3 in the control module.

If the bit is not correct at connector A1V3, suspect a cable/connector problem at Ⓐ.

If the bit is correct, continue scoping in the control module to isolate the problem.

B

With the Ch 2 probe, scope all the Outbus Bits listed in Figure 1 (connector A1A3) and use the sequence chart to determine if the Outbus bits are correct at the Tag '8B' times.

If a bit is not correct, scope at the A2F2 card to locate the problem.

If the Outbus bits are correct, use the Ch 1 probe and scope the bits at connector A1V3 in the failing drive.

If the bit is not correct at connector A1V3, suspect a cable/connector problem at Ⓓ.

If the bit is correct, continue scoping in the failing drive to locate the problem.

See OPER 92 for additional theory.

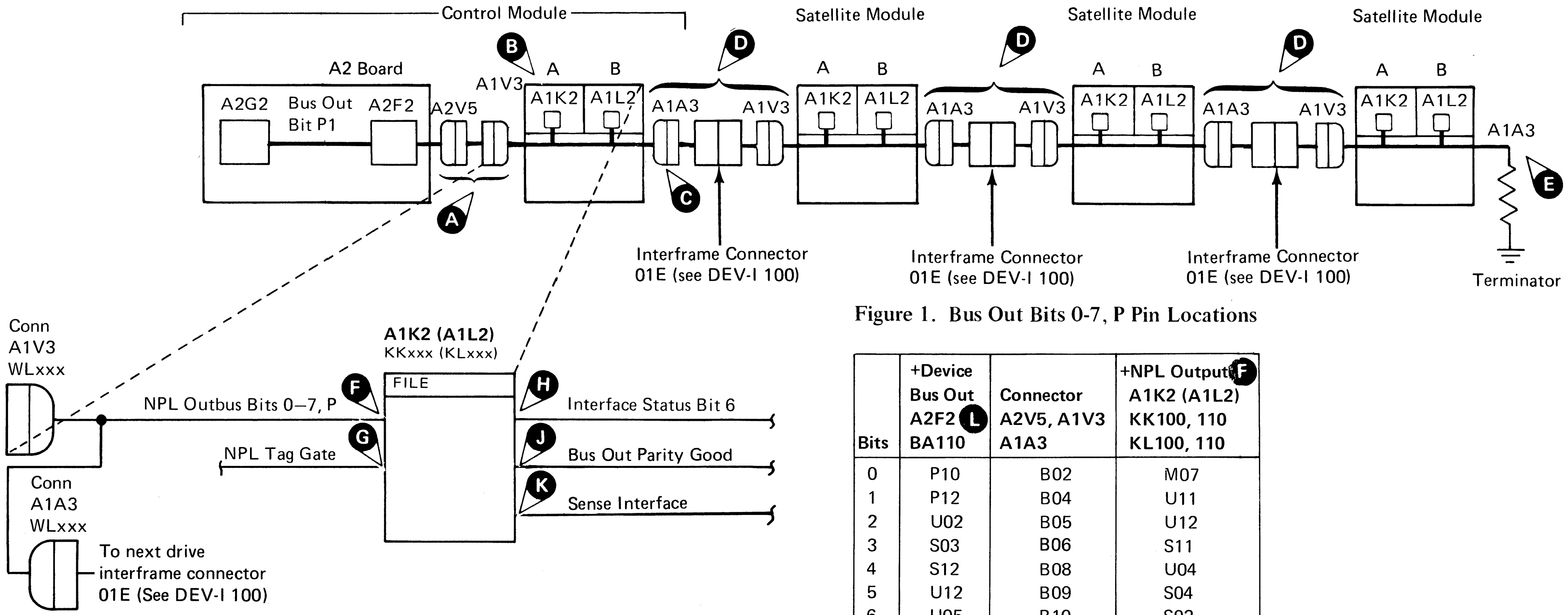
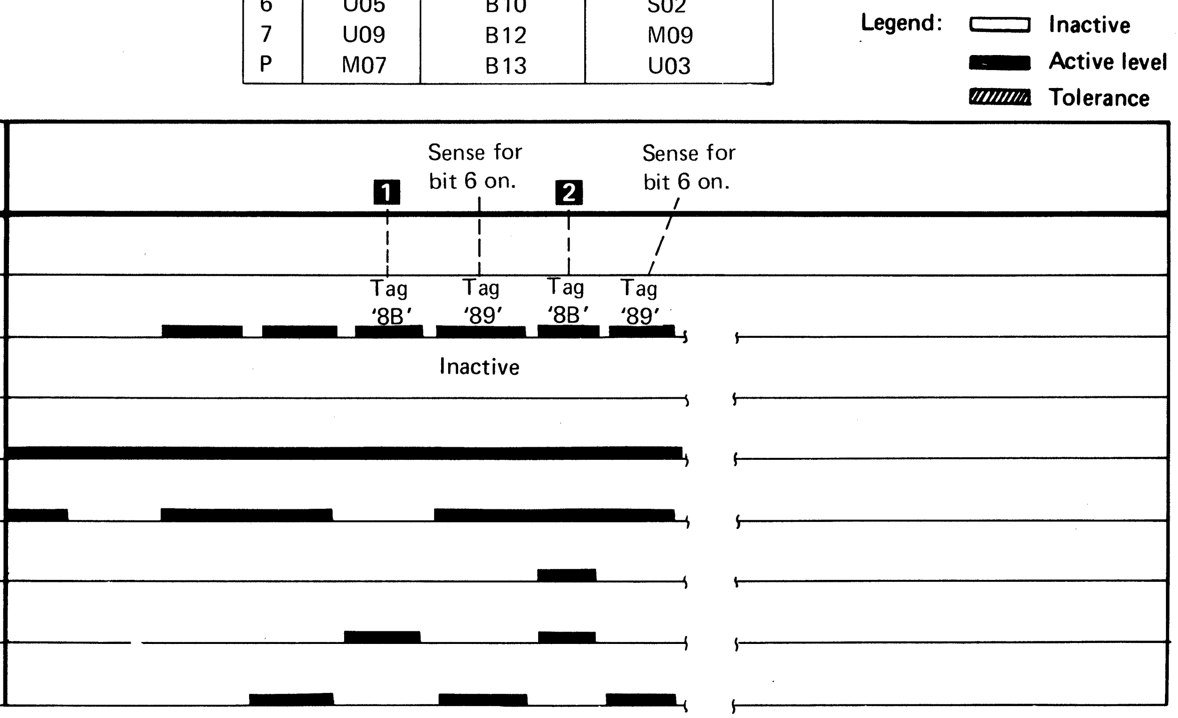


Figure 1. Bus Out Bits 0-7, P Pin Locations

Bits	+Device Bus Out A2F2 Ⓛ BA110	Connector A2V5, A1V3 A1A3	+NPL Output Ⓕ A1K2 (A1L2) KK100, 110 KL100, 110
0	P10	B02	M07
1	P12	B04	U11
2	U02	B05	U12
3	S03	B06	S11
4	S12	B08	U04
5	U12	B09	S04
6	U05	B10	S02
7	U09	B12	M09
P	M07	B13	U03

Chart Line No.	Line Name	ALD	Test Point	
1	−MST RAS TP	BD100	A2L2 J11	
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓖ
3	+Interface Status Bit 6	KK190 (KL190)	A1K2 (A1L2) P04	Ⓗ
4	+Bus Out Parity Good	KK120 (KL120)	A1K2 (A1L2) P07	Ⓙ
5	+NPL Outbus Bit P	BF130	See Figure 1.	Ⓕ
6	+Device Bus Out Bits 1–6	BA110	See Figure 1.	Ⓛ
7	+NPL Outbus Bit 7	BA110	See Figure 1.	Ⓕ
8	+Sense Interface	KK190 (KL190)	A1K2 (A1L2) J09	Ⓚ



1 Set HAR to '01'. Outbus bit 7 is on, all others are off.

2 Set HAR to 'FF'. All Outbus bits are on.

3350	CC0152 Seq. 1 of 2	2358355 Part No.	441300 31 Mar 76	441301 1 June 76	441303 30 Jul 76	

DEVICE BUS OUT PARITY

Circuit Description

See the diagram on DEV-I 155 for referenced test points.

The microdiagnostic program sets HAR to '01' (Tag '8B') and senses the interface (Tag '89') for a Bus Out Parity Check. An A231 Error Code occurs if the Bus Out Parity Check is active; suspect that the failing line is an active P bit or an inactive 7 bit.

HAR is then set to 'FF' (Tag '8B') and sensed (Tag '89') for a Bus Out Parity Check. If any bits are missing, an A232 Error Code occurs.

A Sense Interface Ⓚ (Tag '89') gates Interface Status Bit 6 Ⓗ to the controller if Bus Out Parity Good Ⓙ is at a –level (MST-1).

Analysis Procedure

A

See the diagram on DEV-I 155 for referenced test points.

With the Ch 2 probe, scope all the Outbus Bits listed in Figure 1 on DEV-I 155 (connector A2V5) and use the sequence chart to determine if the Outbus bits are correct at the Tag '8B' times.

If a bit is not correct, scope at the A2F2 card to locate the problem. If the bit is correct at the input to A2F2, suspect a shorted cable causing all drives to fail. Use the Isolation Procedure to isolate the problem.

If the Outbus bits are correct, use the Ch 1 probe and scope the bits at connector A1V3 in the control module.

If the bit is not correct at connector A1V3, suspect a cable/ connector problem at Ⓐ.

If the bit is correct, continue scoping in the control module to isolate the problem.

Isolation Procedure

1. Remove the A1A3 connector in the A2 control module at Ⓒ.
2. Install a 2-wide terminator card (P/N 4516953) A1A2 and A1A3 Ⓒ on the A2 control module on the pin side of the board.
3. Set the CE Mode switch for Drive A in the control module and turn off the CE Mode switches for all other drives in the string.
4. Push the Attention pushbutton on all drives taken out of CE Mode.

Microdiagnostic Setup

Run microdiagnostic routine A2 from the A2 control module.

1. Load routine A2
2. Enter 10, 00

Microdiagnostic fails?

YES

Troubleshoot the drive in CE Mode.

NO

Remove the terminators and replace the connectors. Rerun microdiagnostics.

Note: *When adding the C2 control module to the string, replace connectors at A1A2 and A1A3, remove terminator card, and run microdiagnostics on the complete string.*

If the microdiagnostics run error free, one of the following may be causing the problem:

1. *Failing A2F2 terminator card located in either controller.*
2. *Faulty cable or improper seating of cable connectors.*

Analysis Procedure

B

See the diagram on DEV-I 155 for referenced test points.

Run microdiagnostics on the A2 controller.

With the Ch 2 probe, scope all the Outbus bits listed in Figure 1 on DEV-I 155 (connector A1A3) and use the sequence chart to determine if the Outbus bits are correct at the Tag '8B' times.

If a bit is not correct, scope at the A2F2 card to locate the problem.

If the Outbus bits are correct, use the Ch 1 probe and scope the bits at connector A1V3 (connector A1A3 in C2 Module) in the failing drive.

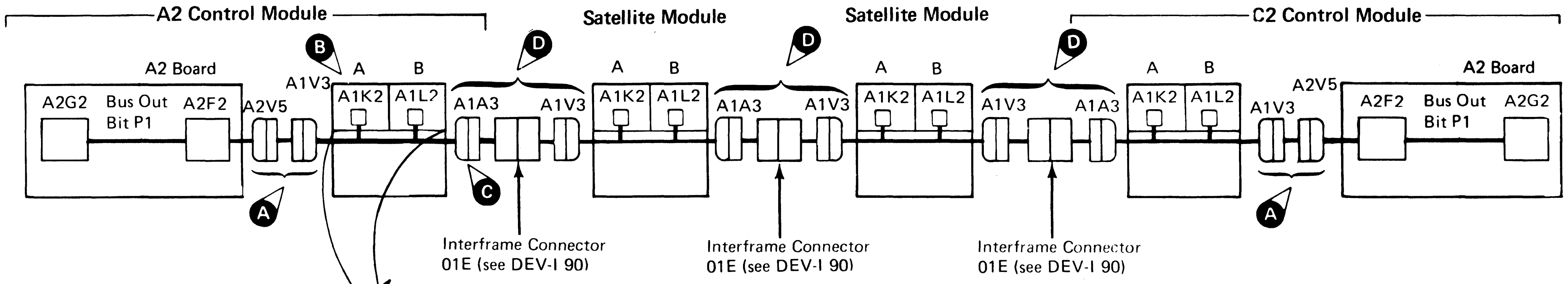
If the bit is not correct at connector A1V3, suspect a cable/ connector problem at Ⓓ.

If the bit is correct, continue scoping in the failing drive to locate the problem.

F
L

DEVICE BUS OUT PARITY

See OPER 92 for additional theory.



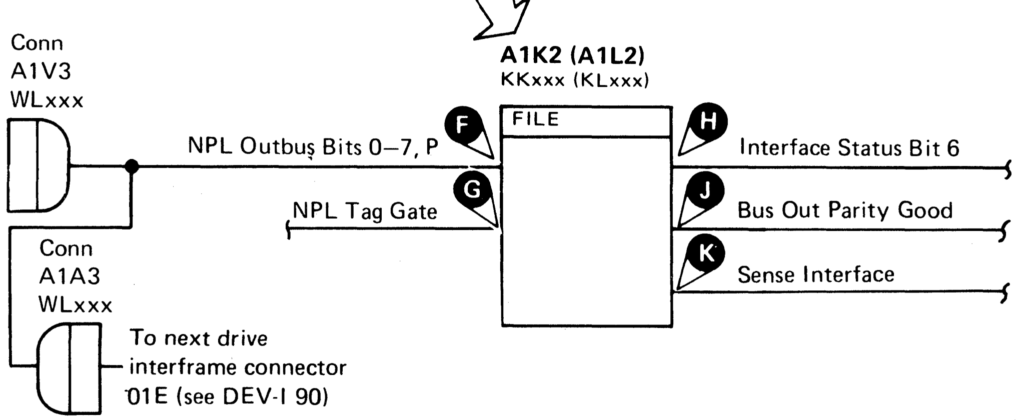
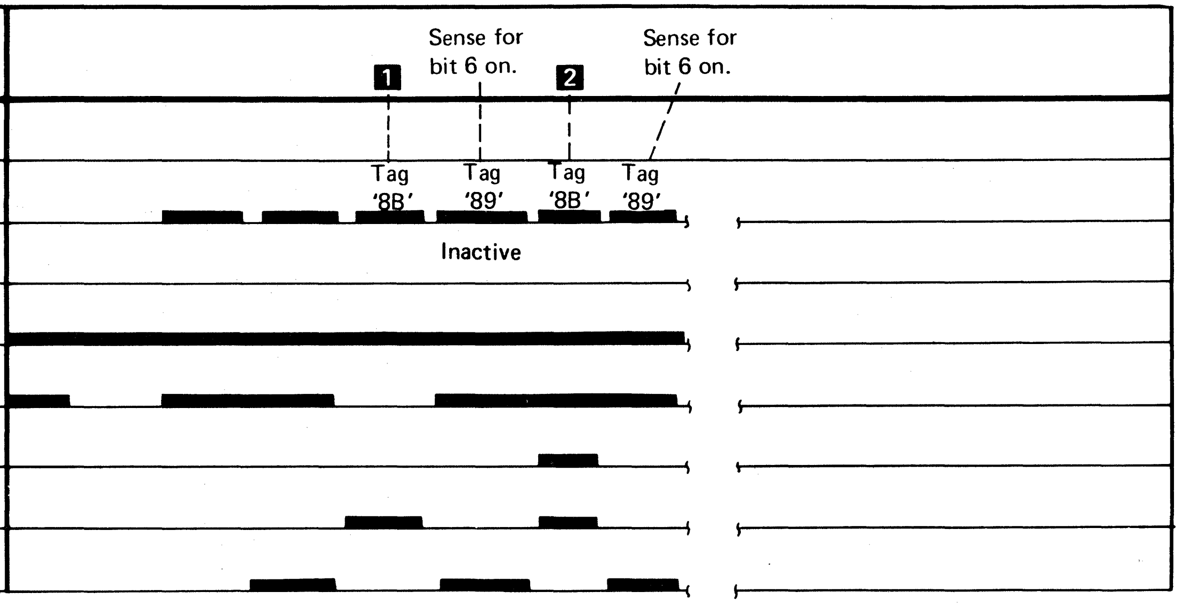


Figure 1. Bus Out Bits 0-7, P Pin Locations

Bits	+Device Bus Out A2F2 Ⓛ BA110	Connector A2V5, A1V3 A1A3	+NPL Output Ⓕ A1K2 (A1L2) KK100, 110 KL100, 110
0	P10	B02	M07
1	P12	B04	U11
2	U02	B05	U12
3	S03	B06	S11
4	S12	B08	U04
5	U12	B09	S04
6	U05	B10	S02
7	U09	B12	M09
P	M07	B13	U03

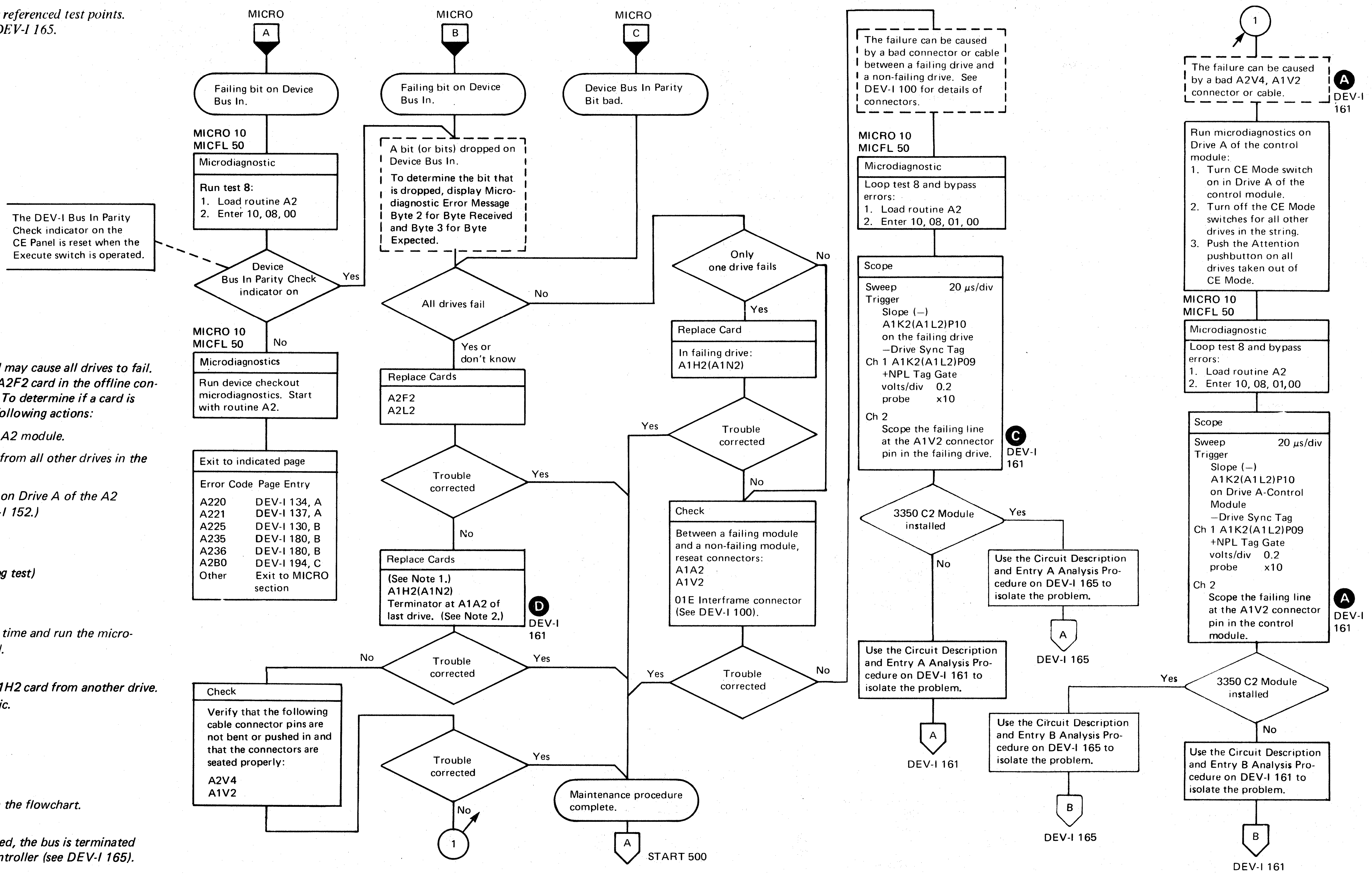
Legend: ▭ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	–MST RAS TP	BD100	A2L2 J11	
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓖ
3	+Interface Status Bit 6	KK190 (KL190)	A1K2 (A1L2) P04	Ⓗ
4	+Bus Out Parity Good	KK120 (KL120)	A1K2 (A1L2) P07	Ⓙ
5	+NPL Outbus Bit P	BF130	See Figure 1.	Ⓕ
6	+Device Bus Out Bits 1–6	BA110	See Figure 1.	Ⓛ
7	+NPL Outbus Bit 7	BA110	See Figure 1.	Ⓕ
8	+Sense Interface	KK190 (KL190)	A1K2 (A1L2) J09	Ⓚ



1 Set HAR to '01'. Outbus bit 7 is on, all others are off.
2 Set HAR to 'FF'. All Outbus bits are on.

See the diagram on DEV-I 161 for referenced test points.
If the C2 Module is installed, see DEV-I 165.



Note 1: *An A1H2(A1N2)* **B** *card may cause all drives to fail. (If the C2 Module is installed, the A2F2 card in the offline controller can cause all drives to fail.) To determine if a card is causing the problem, perform the following actions:*

1. *Leave the A1H2* **B** *card in the A2 module.*
2. *Remove the A1H2(A1N2) card from all other drives in the string.*
3. *Run the failing microdiagnostic on Drive A of the A2 module. (See the diagram DEV-I 152.)*

To loop failing test:

1. *Load routine A2*
2. *Enter 10,XX,00 (XX = Failing test)*

Microdiagnostic fails?

NO
Install A1H2(A1N2) cards one at a time and run the microdiagnostic to isolate the failing card.

YES
1. *Swap the A1H2 card with an A1H2 card from another drive.*
2. *Rerun the failing microdiagnostic.*

Microdiagnostic fails?

NO
Replace the bad card.

YES
Replace all cards and continue with the flowchart.

Note 2: *If the C2 Module is installed, the bus is terminated on the A2F2 card in the offline controller (see DEV-I 165).*

3350	CC0155 Seq. 2 of 2	2358719 Part No.	441301 1 Jun 76	441303 30 Jul 76	441305 29 Oct 76		

DEVICE BUS IN

Circuit Description

The microdiagnostic sets HAR to '00' (Tag '8B') and senses HAR for '00' (Tag '8F'). Only bit P should be active. If bit P is not active or any bit (0-7) is active, an A281 Error Code occurs.

HAR is then set to 'FF' (Tag '8B') and sensed (Tag '8F'). If a bit is dropped, an A280 Error Code occurs.

Analysis Procedure

DEV-I 160

A

If the bit is not active at the correct time, scope in the failing drive to isolate the problem.

If the bit is active at the correct time at the A1V2 connector Ⓒ, move the Ch 1 probe to the A1A2 connector pin in the next non-failing drive.

If the bit is lost between the connectors, the problem is in the cables or connectors (see DEV-I 100 to isolate the problem).

If the bit is not lost between the connectors, continue scoping in the non-failing drive to find where the bit is lost.

DEV-I 160

B

If the bit is not active at the correct time, scope the Inbus at the input to A1H2 in Drive A. If the bit is not active at the correct time, continue scoping in Drive A to isolate the problem. If the bit is active at the correct time, suspect a shorted cable causing all drives to fail. Use the isolation procedure on DEV-I 162, Entry C to determine the failure.

If the bit is active at the correct time, move the Ch 1 probe to the A2V4 connector pin Ⓐ.

If the bit is lost between the connectors, the problem is in the cable or connector.

If the bit is not lost between the connectors, continue scoping in the controller board to find where the bit is lost.

See OPER 92 for additional theory.

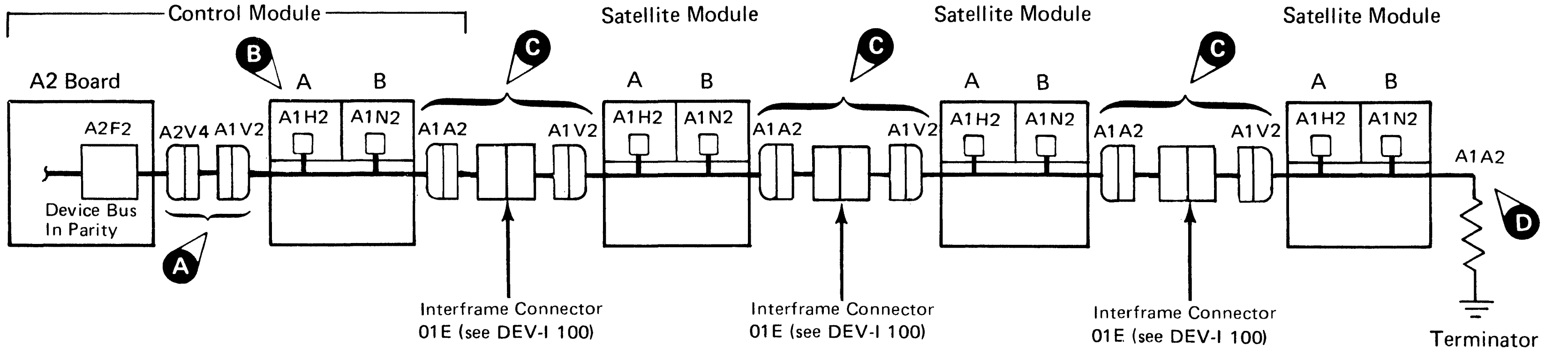


Figure 1. Inbus Bits 0–7, P Pin Locations

Bits	A2V4 Connector (BU300)	A1A2/A1V2 Connector WLxxx	A1H2(A1N2) Card KHxxx(KNxxx)
0	B02	B02	B05
1	B04	B04	D05
2	B05	B05	B09
3	B06	B06	D10
4	B08	B08	D07
5	B09	B09	D02
6	B10	B10	B02
7	B12	B12	D06
P	B13	B13	B07

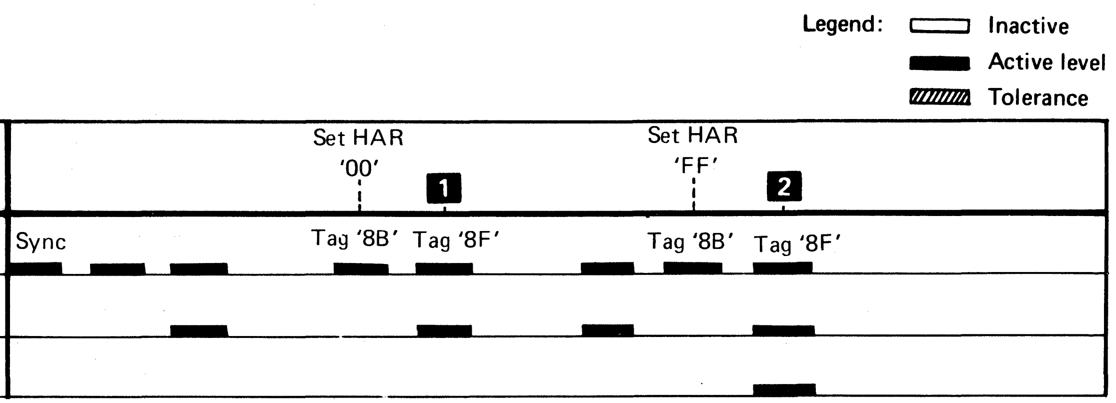
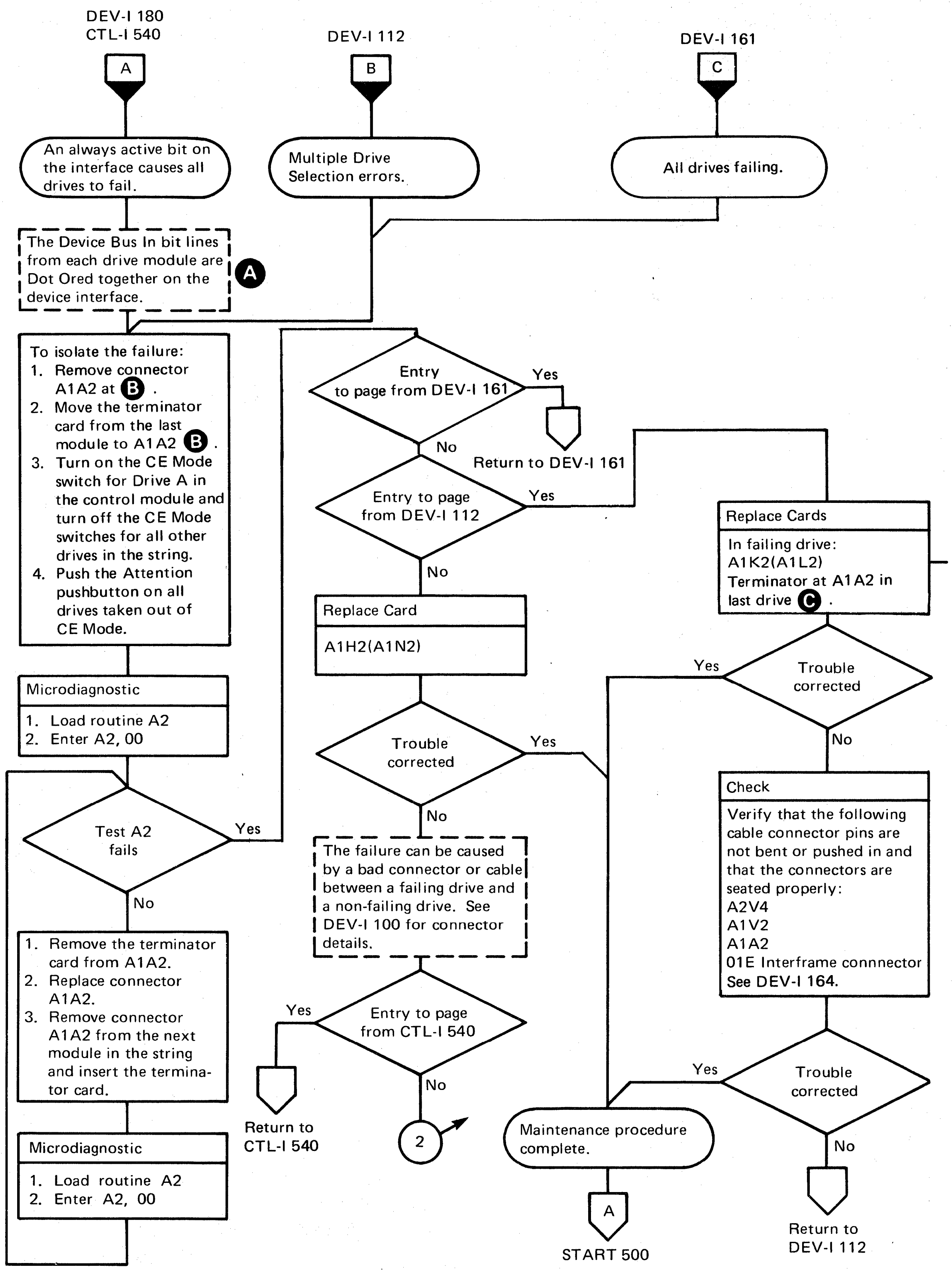
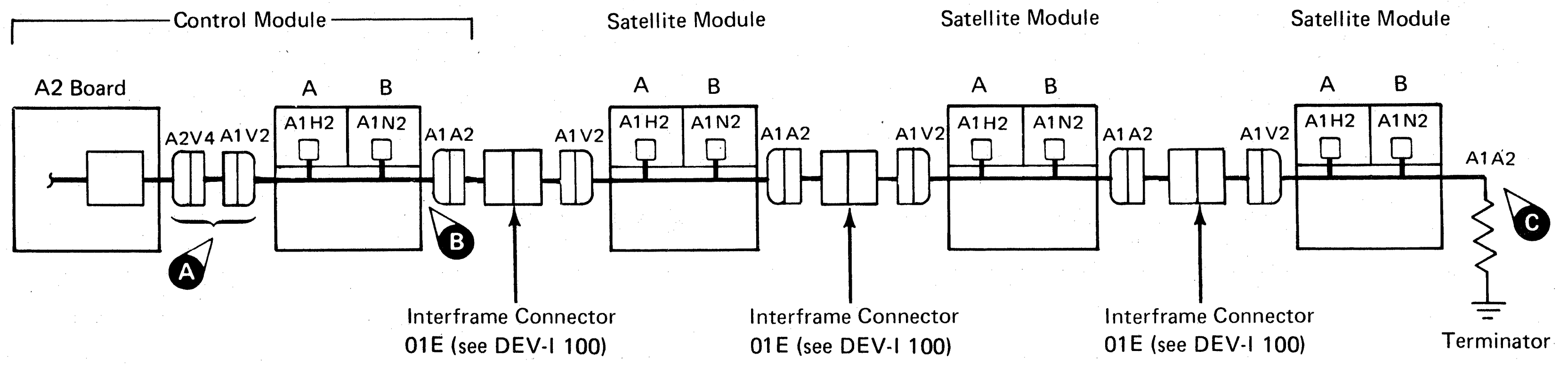


Chart Line No.	Line Name	ALD	Test Point	
1	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	
2	+NPL Inbus Bit P	KH200 (KN200)	A1H2 (A1N2) B07	
3	+NPL Inbus Bits	KH200 (KN200)	See Figure 1.	

1 Sense HAR, bit P, should be on.

2 Sense HAR, all bits, should be on.





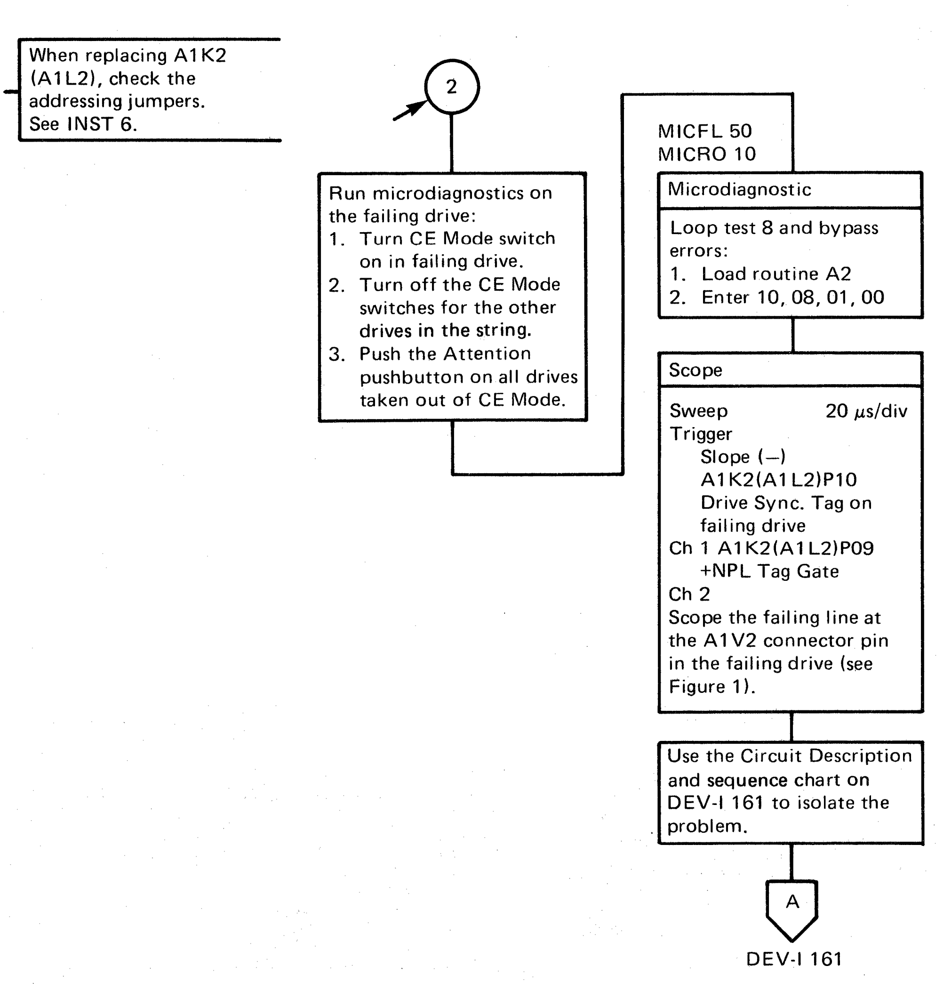


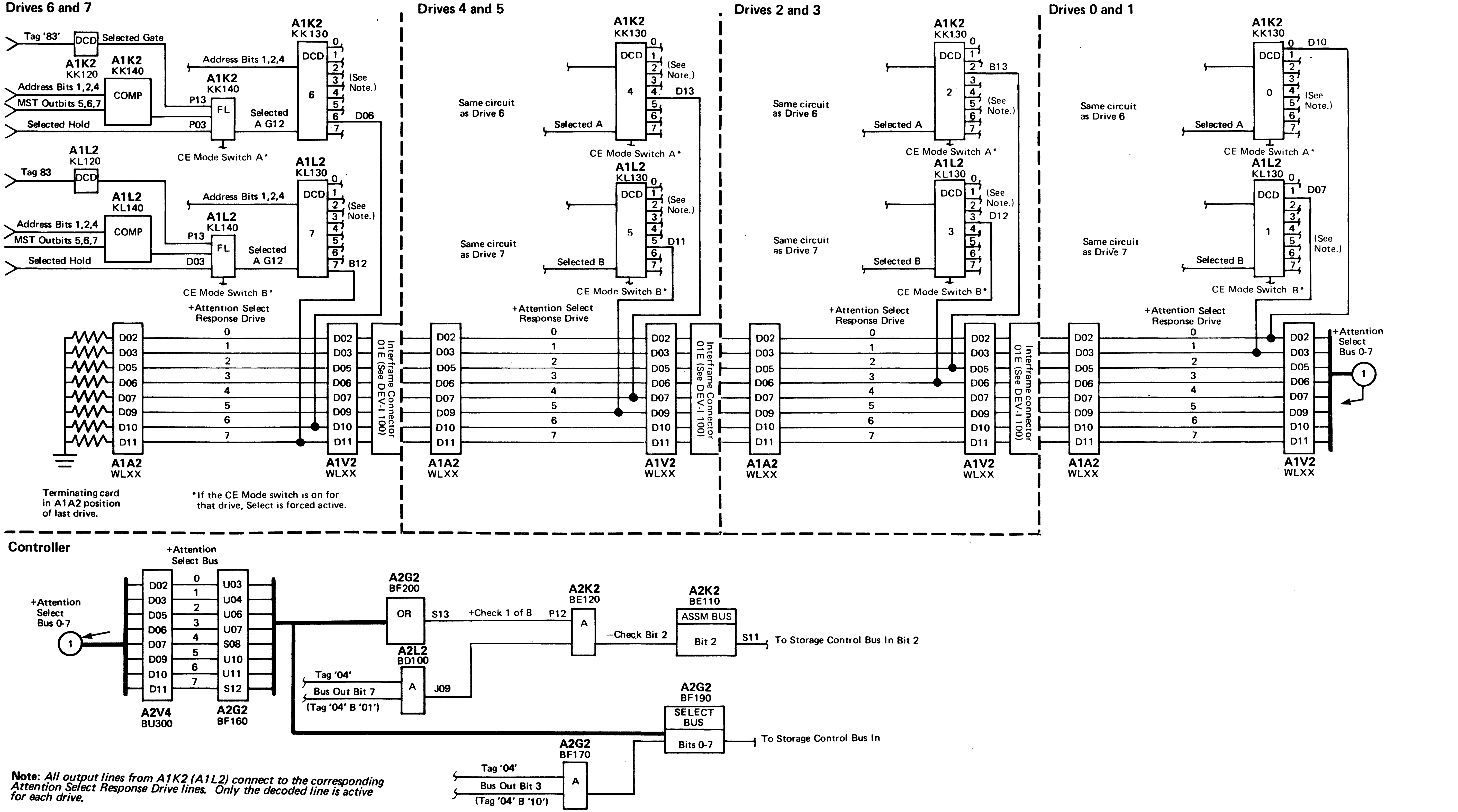
Figure 1. Inbus Bits 0-7, P Pin Locations

Bits	A2V4 Connector BU300	A1A2/A1V2 Connector WLxxx	A1H2(A1N2) Card KH200 (KN200)
0	B02	B02	B05
1	B04	B04	D05
2	B05	B05	B09
3	B06	B06	D10
4	B08	B08	D07
5	B09	B09	D02
6	B10	B10	B02
7	B12	B12	D06
P	B13	B13	B07

CC0161 Seq. 2 of 2	2358356 Part No.	441300 31 Mar 76	441303 30 Jul 76			

ATTENTION SELECT RESPONSE

See DEV-I 168 for 3350 with C2 Module.



Note: *All output lines from A1K2 (A1L2) connect to the corresponding Attention Select Response Drive lines. Only the decoded line is active for each drive.*

3350	CC0164 Seq. 1 of 1	2358357 Part No.	441300 31 Mar 76	441301 1 June 76			

F
L

DEVICE BUS IN

Circuit Description

The microdiagnostic sets HAR to '00' (Tag '8B') and senses HAR for '00' (Tag '8F'). Only bit P should be active. If bit P is not active or any bit (0-7) is active, an A281 Error Code occurs.

HAR is then set to 'FF' (Tag '8B') and sensed (Tag '8F'). If a bit is dropped, an A280 Error Code occurs.

Analysis Procedure

A

Run microdiagnostics on the A2 controller.

If the bit is not active at the correct time, scope in the failing drive to isolate the problem.

If the bit is active at the correct time at the A1V2 connector (A1A2 in C2 control module) **C**, move the Ch 1 probe to the A1A2 connector pin in the next non-failing drive.

If the bit is lost between the connectors, the problem is in the cables or connectors (see DEV-I 90 to isolate the problem).

If the bit is not lost between the connectors, continue scoping in the non-failing drive to find where the bit is lost.

B

If the bit is not active at the correct time, scope the Inbus at the input to A1H2 in Drive A. If the bit is not active at the correct time, continue scoping in Drive A to isolate the problem. If the bit is active at the correct time, suspect a shorted cable causing all drives to fail. Use the isolation procedure on DEV-I 167, Entry C to determine the failure.

If the bit is active at the correct time, move the Ch 1 probe to the A2V4 connector pin **A**.

If the bit is lost between the connectors, the problem is in the cable or connector.

If the bit is not lost between the connectors, continue scoping in the controller board to find where the bit is lost.

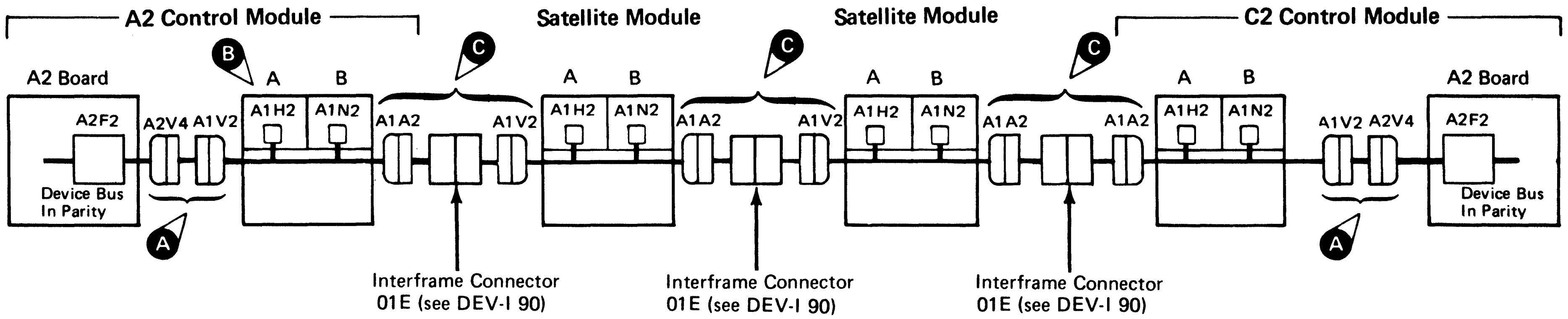
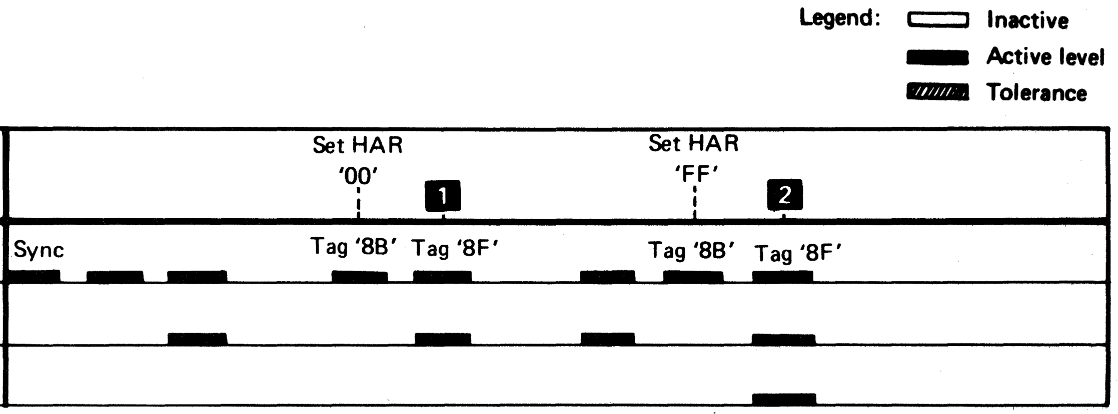


Figure 1. Inbus Bits 0-7, P Pin Locations

Bits	A2V4 Connector (BU300)	A1A2/A1V2 Connector WLxxx	A1H2(A1N2) Card KHxxx(KNxxx)
0	B02	B02	B05
1	B04	B04	D05
2	B05	B05	B09
3	B06	B06	D10
4	B08	B08	D07
5	B09	B09	D02
6	B10	B10	B02
7	B12	B12	D06
P	B13	B13	B07

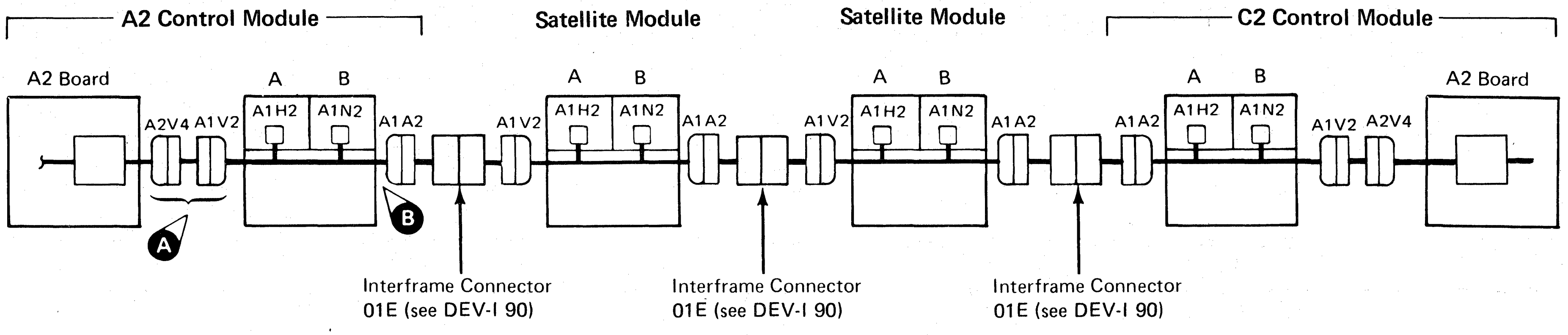
Chart Line No.	Line Name	ALD	Test Point	
1	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	
2	+NPL Inbus Bit P	KH200 (KN200)	A1H2 (A1N2) B07	
3	+NPL Inbus Bits	KH200 (KN200)	See Figure 1.	

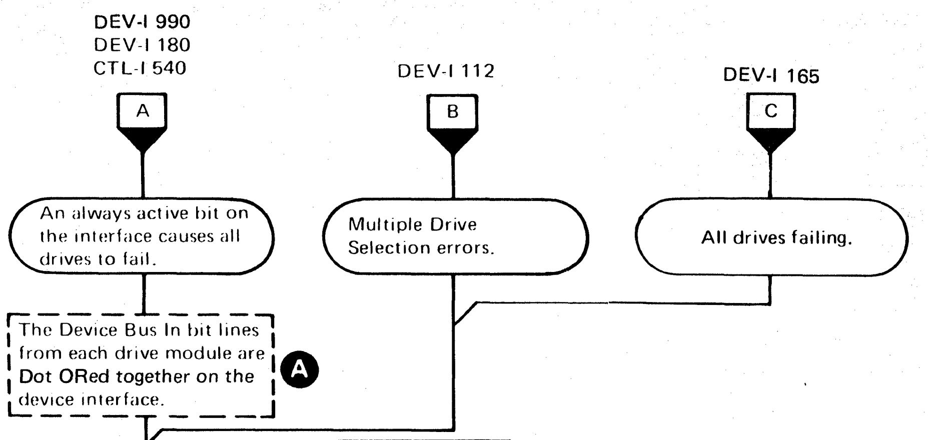


1 Sense HAR, bit P, should be on.

2 Sense HAR, all bits, should be on.

3350	CC0165 Seq. 1 of 2	2358720 Part No.	441301 1 June 76	441303 30 Jul 76			



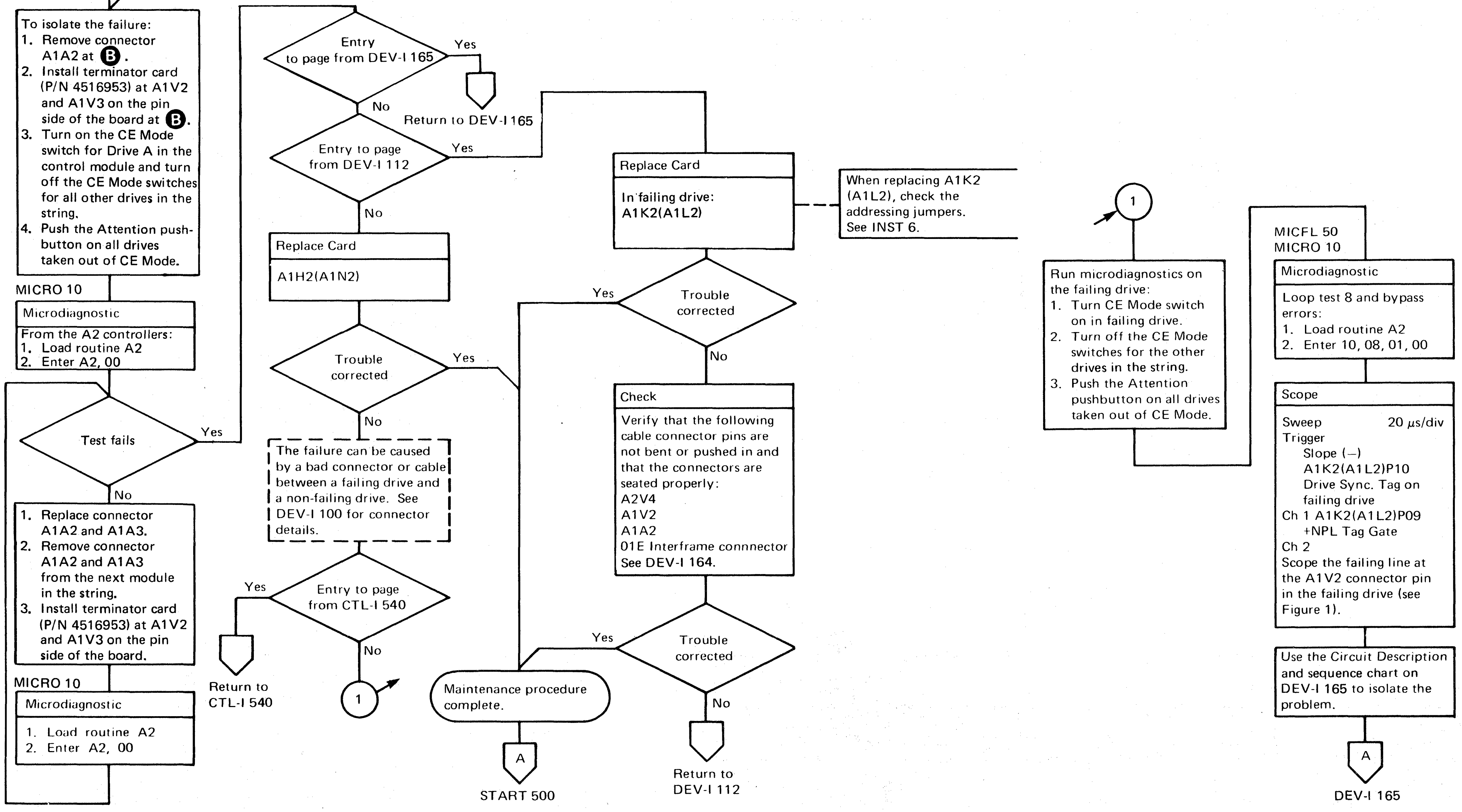


An always active bit on the interface causes all drives to fail.

Multiple Drive Selection errors.

All drives failing.

The Device Bus In bit lines from each drive module are Dot ORed together on the device interface. **A**



To isolate the failure:
1. Remove connector A1A2 at **B**.
2. Install terminator card (P/N 4516953) at A1V2 and A1V3 on the pin side of the board at **B**.
3. Turn on the CE Mode switch for Drive A in the control module and turn off the CE Mode switches for all other drives in the string.
4. Push the Attention pushbutton on all drives taken out of CE Mode.

Microdiagnostic

From the A2 controllers:
1. Load routine A2
2. Enter A2, 00

Test fails

1. Replace connector A1A2 and A1A3.
2. Remove connector A1A2 and A1A3 from the next module in the string.
3. Install terminator card (P/N 4516953) at A1V2 and A1V3 on the pin side of the board.

Microdiagnostic

1. Load routine A2
2. Enter A2, 00

Entry to page from DEV-I 165

Return to DEV-I 165

Entry to page from DEV-I 112

Replace Card

A1H2(A1N2)

Trouble corrected

The failure can be caused by a bad connector or cable between a failing drive and a non-failing drive. See DEV-I 100 for connector details.

Entry to page from CTL-I 540

Return to CTL-I 540

Replace Card

In failing drive:
A1K2(A1L2)

When replacing A1K2 (A1L2), check the addressing jumpers. See INST 6.

Trouble corrected

Check

Verify that the following cable connector pins are not bent or pushed in and that the connectors are seated properly:
A2V4
A1V2
A1A2
01E Interframe connnector
See DEV-I 164.

Trouble corrected

Maintenance procedure complete.

START 500

Return to DEV-I 112

Run microdiagnostics on the failing drive:
1. Turn CE Mode switch on in failing drive.
2. Turn off the CE Mode switches for the other drives in the string.
3. Push the Attention pushbutton on all drives taken out of CE Mode.

Microdiagnostic

Loop test 8 and bypass errors:
1. Load routine A2
2. Enter 10, 08, 01, 00

Scope

Sweep 20 μs/div
Trigger
Slope (−)
A1K2(A1L2)P10
Drive Sync. Tag on failing drive
Ch 1 A1K2(A1L2)P09
+NPL Tag Gate
Ch 2
Scope the failing line at the A1V2 connector pin in the failing drive (see Figure 1).

Use the Circuit Description and sequence chart on DEV-I 165 to isolate the problem.

DEV-I 165

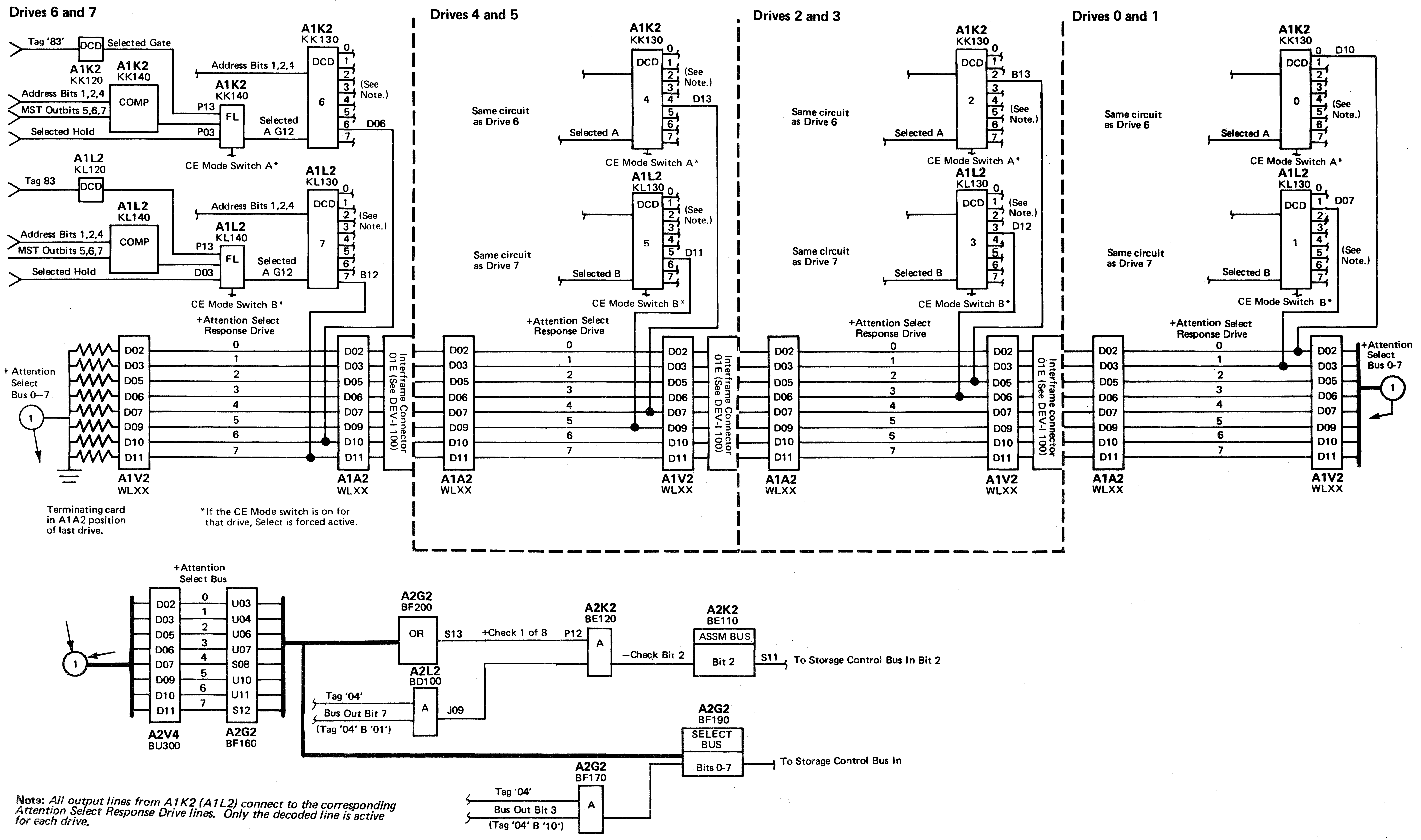
Figure 1. Inbus Bits 0-7, P Pin Locations

Bits	A2V4 Connector BU300	A1A2/A1V2 Connector WLxxx	A1H2(A1N2) Card KH200 (KN200)
0	B02	B02	B05
1	B04	B04	D05
2	B05	B05	B09
3	B06	B06	D10
4	B08	B08	D07
5	B09	B09	D02
6	B10	B10	B02
7	B12	B12	D06
P	B13	B13	B07

3350	CC0165 Seq. 2 of 2	2358720 Part No.	441301 1 June 76	441303 30 Jul 76			

ATTENTION SELECT RESPONSE

See DEV-I 164 for 3350 without C2 Module.

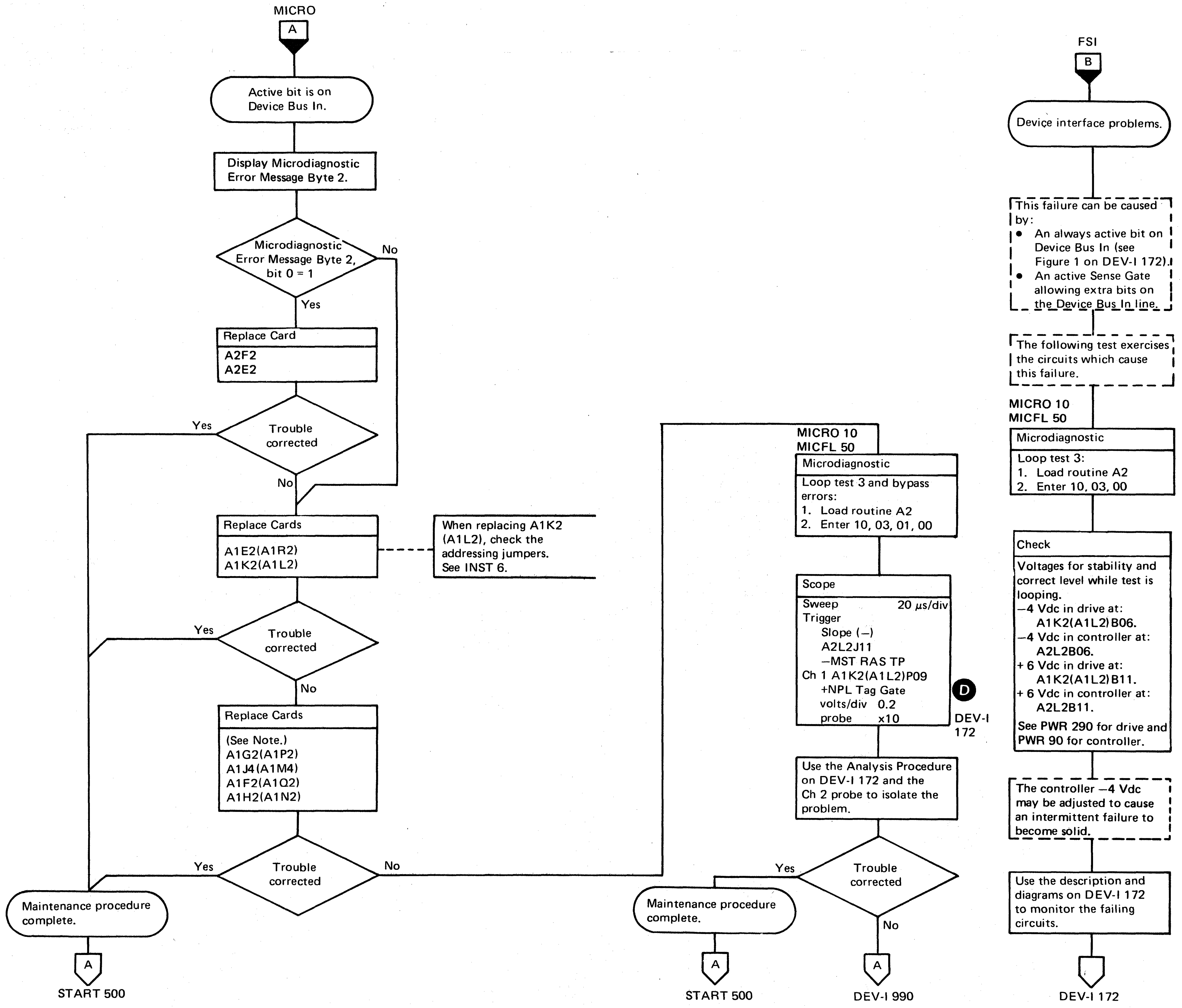


Note: *All output lines from A1K2 (A1L2) connect to the corresponding Attention Select Response Drive lines. Only the decoded line is active for each drive.*

3350

CC0168 Seq. 1 of 2	2358721 Part No.	441301 1 June 76	441303 30 Jul 76	441308 18 Aug 78		

DEVICE BUS IN BIT ACTIVE



Note: *(See DEV-I 184.) Each bit on the Device Bus In is affected by six different cards in each drive.*

Drive A		Drive B	
A1E2 *A1F2* *A1G2* *A1J4* *A1K2*	*Dot OR at A1H2*	*A1R2* *A1Q2* *A1P2* *A1M4* *A1L2*	*Dot OR at A1N2*

Any one of these cards can cause a bit to remain active or inactive. If the error remains after replacing or swapping cards, perform the following:

1. *ALWAYS ACTIVE BIT – Scope the failing bit line.*
   a. *If the bit line is at a + level (MST-1), remove the cards one at a time until the line drops to – level (MST-1). If all cards are removed and the bit line is still active, look for tight wire wraps, bent pins, etc.*
   b. *If the bit line is at a – level (MST-1), return to the flowchart.*
2. *ALWAYS INACTIVE BIT – Return to the flowchart.*

DEVICE BUS IN BIT ACTIVE

Circuit Description

The microdiagnostic resets HAR Ⓑ (Tag '8F', Bus '04') to '00' then issues a Sense Interface (Tag '89'). '00' should be returned on the NPL Inbus Bits 0-7.

Analysis Procedure

Scope the NPL Inbus Bit Ⓔ that is active (see Figure 1) as determined by Error Message Byte 2. If at Tag '89' time the bit is active, scope in the drive. If the bit is not active, scope in the controller to determine where it became active.

If NPL Inbus Bit 4 is active, suspect +Gate Mach or RW Status Ⓒ line is active erroneously at Tag '89' time. This causes Access∗Check Status Bit 4 Ⓐ to be active.

Gate Mach or RW Status can be active because:

+Gate Mach Status is active (KK140, KL140).
+Set Read*Write is active (KK140, KL140).

See OPER 92 for additional theory.

Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

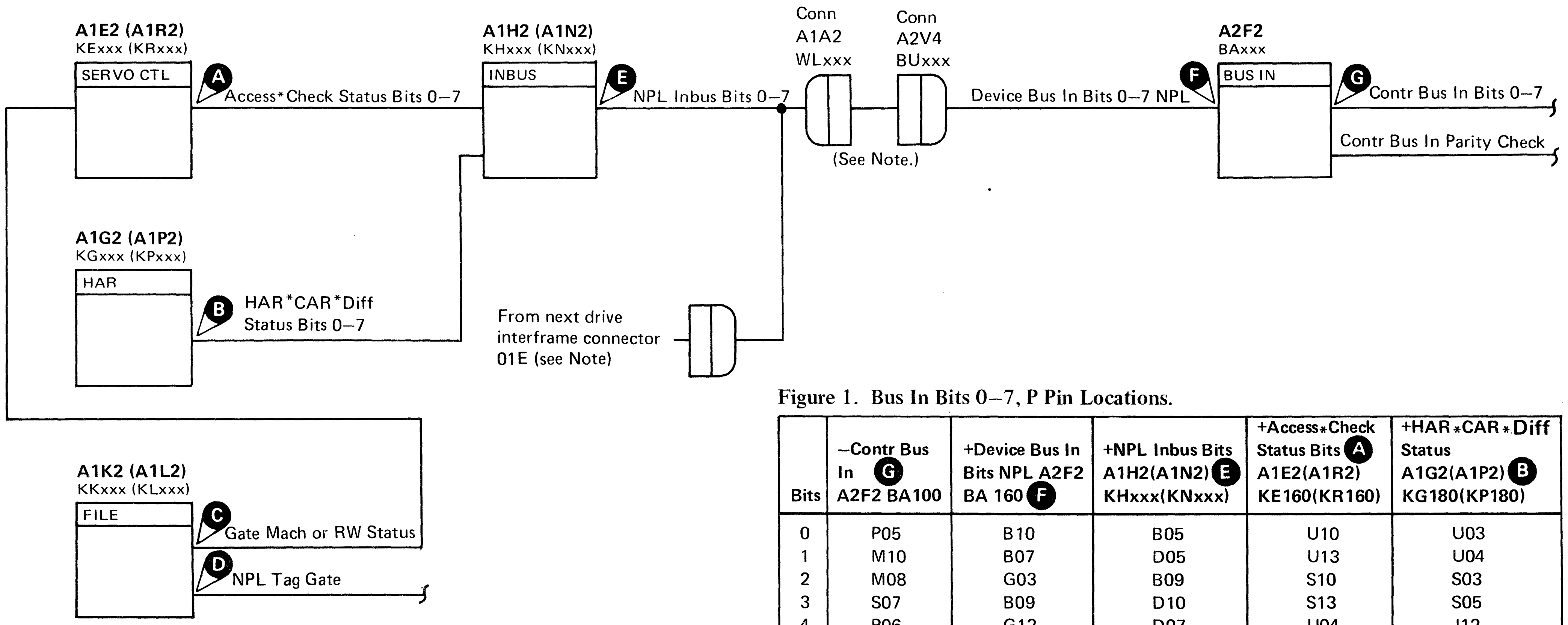
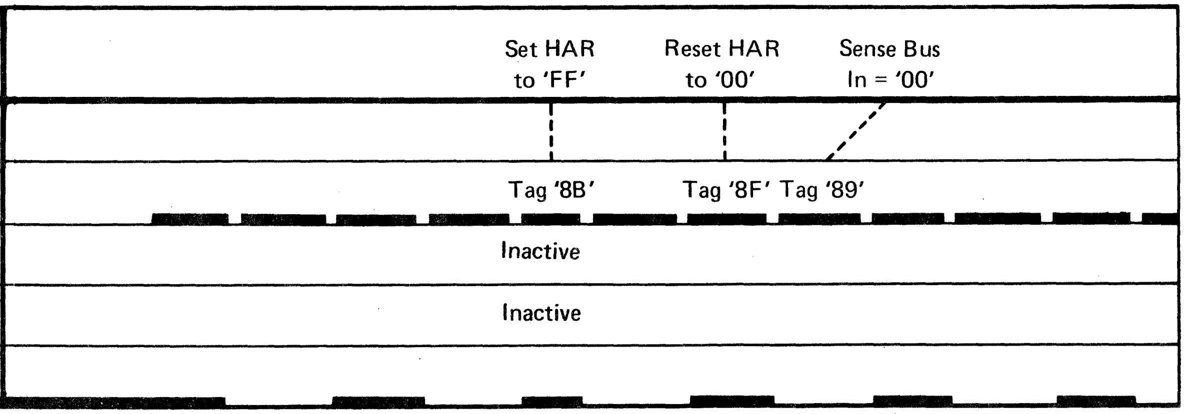


Figure 1. Bus In Bits 0–7, P Pin Locations.

Bits	−Contr Bus In Ⓖ A2F2 BA100	+Device Bus In Bits NPL A2F2 BA 160 Ⓕ	+NPL Inbus Bits A1H2(A1N2) Ⓔ KHxxx(KNxxx)	+Access∗Check Status Bits Ⓐ A1E2(A1R2) KE160(KR160)	+HAR∗CAR∗Diff Status A1G2(A1P2) Ⓑ KG180(KP180)
0	P05	B10	B05	U10	U03
1	M10	B07	D05	U13	U04
2	M08	G03	B09	S10	S03
3	S07	B09	D10	S13	S05
4	P06	G12	D07	U04	J12
5	U03	J04	D02	P13	G12
6	P09	G05	B02	S04	G10
7	U06	G13	D06	M13	J10

Legend: ▭ Inactive ▬ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Set HAR to 'FF' Reset HAR to '00' Sense Bus In = '00'
1	−MST RAS TP	BD100	A2L2 J11		
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓓ	Tag '8B' Tag '8F' Tag '89'
3	−Contr Bus In Bit 0	BA100	A2F2 P05	Ⓖ	Inactive
4	+Access∗Check Status Bits 0–7	KE160 (KR160)	See Figure 1.	Ⓐ	Inactive
5	+Gate Mach or RW Status	KK140 (KL140)	A1K2 (A1L2) S13	Ⓒ	



HEAD ADDRESS REGISTER (HAR) AND DIFFERENCE COUNTER (DIFF) FAILS

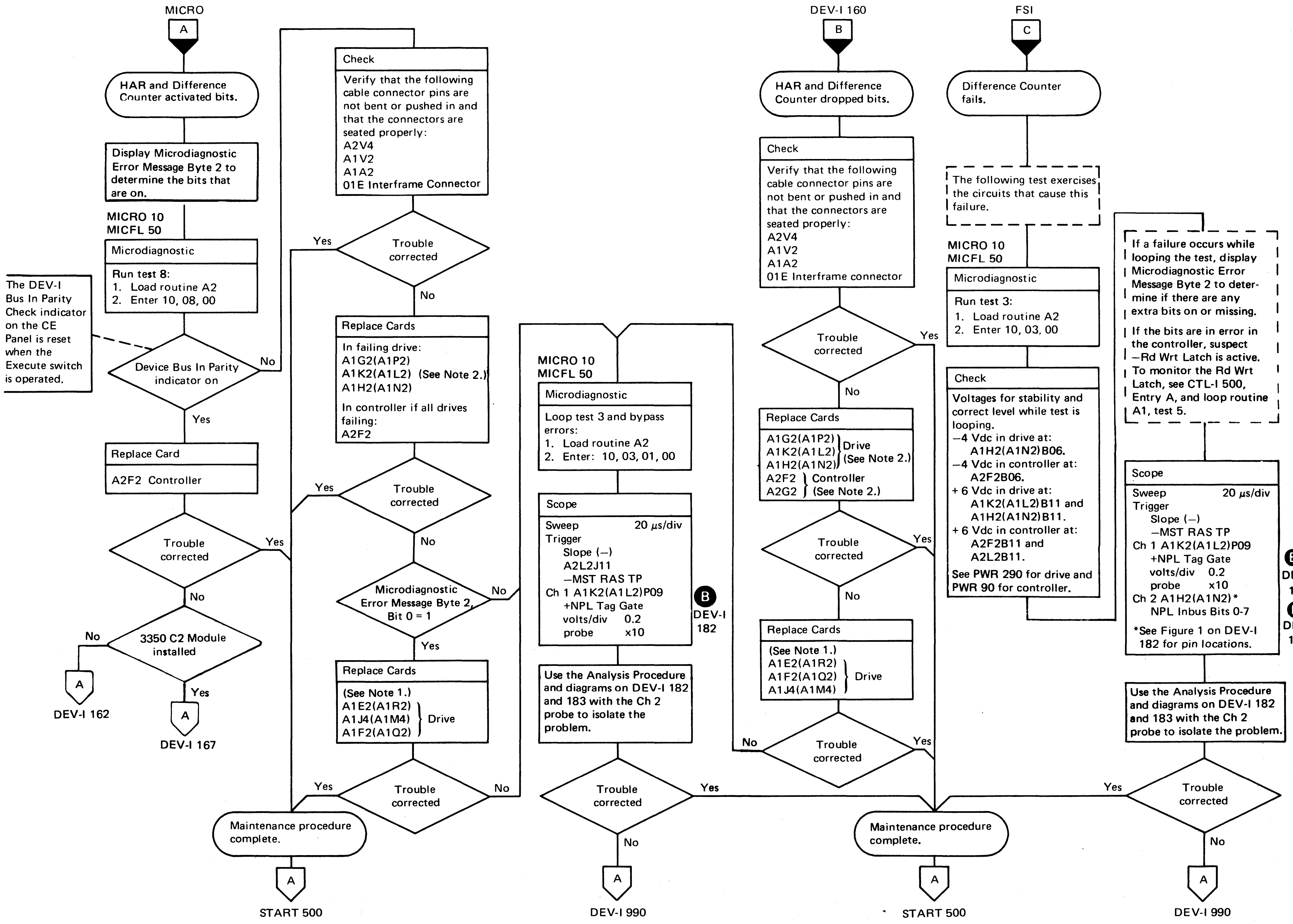
Note 1: *(See DEV-I 184.) Each bit on the Device Bus In is affected by six different cards in each drive.*

Drive A		Drive B	
A1E2 *A1F2* *A1G2* *A1J4* *A1K2*	*Dot OR at A1H2*	*A1R2* *A1Q2* *A1P2* *A1M4* *A1L2*	*Dot OR at A1N2*

Any one of these cards can cause a bit to remain active or inactive. If the error remains after replacing or swapping cards, perform the following:

1. *ALWAYS ACTIVE BIT — Scope the failing line.*
   a. *If the bit line is at a + level (MST-1), remove the cards one at a time until the line drops to — level (MST-1). If all cards are removed and the bit line is still active, look for tight wire wraps, bent pins, etc.*
   b. *If the bit line is still at a — level (MST-1), return to the flowchart.*
2. *ALWAYS INACTIVE BIT — Return to the flowchart.*

Note 2: *When replacing A1K2(A1L2) and/or A2G2, check the addressing jumpers. See INST 6.*



3350

CC0180 Seq. 1 of 2	2358359 Part No.	441300 31 Mar 76	441301 1 June 76	441303 30 Jul 76	441306 1 Apr 77	

HEAD ADDRESS REGISTER (HAR) AND DIFFERENCE COUNTER (DIFF) FAILS

Circuit Description

Use the sequence chart and follow the descriptions of the Tag sequence listed below as a scoping aid:

1. Tag '8C' Bus '00' Set Diff Counter to '00'.
2. Tag '8F' Bus '09' Sense Diff Counter for '00' (all NPL Inbus Bits 0-7 are off; bit P is on). If Diff Counter equals '00', go to Step 5. If Diff Counter is not equal to '00', go to Step 3.
3. Tag '8B' Bus '00' Set HAR to '00'.
4. Tag '8F' Bus '05' Sense HAR for '00' (all NPL Inbus Bits 0-7 are off, bit P is on). If HAR is not equal to '00', an A234 error occurs. If HAR equals '00', continue with Step 5.
5. Change scope sweep time to 50 μs.
6. Tag '8C' Bus 'FF' Set Diff Counter to 'FF'.
7. Tag '8F' Bus '09' Sense Diff Counter for 'FF' (all NPL Inbus Bits 0-7 are on). If Diff Counter equals 'FF', go to Step 10. If Diff Counter is not equal to 'FF', go to Step 8.
8. Tag '8B' Bus 'FF' Set HAR to 'FF'.
9. Tag '8F' Bus '05' Sense HAR for 'FF' (all NPL Inbus Bits 0-7 are on). If HAR is not equal to 'FF', an A235 error occurs. If HAR equals 'FF', go to Step 10.
10. Sliding ones pattern placed on Diff Counter and HAR Bus In must equal Bus Out or an A236 error occurs. See MICFL 50.

See OPER 92 for additional theory.

Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

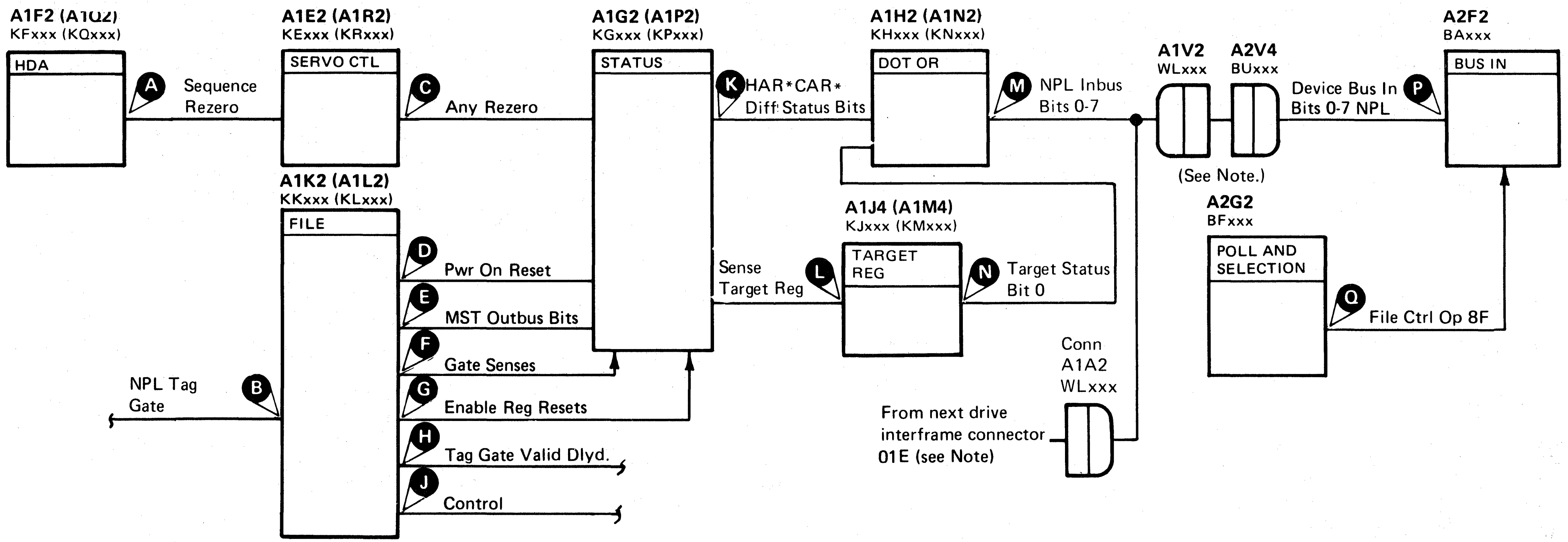


Figure 1. Outbus and Inbus Bits 0–7, P Pin Locations

Bits	–MST Outbus Ⓔ A1K2 (A1L2) KK100 (KL100)	+HAR*CAR* Diff Status Ⓚ A1G2 (A1P2) KG180 (KP180)	+NPL Inbus Ⓜ A1H2 (A1N2) KH200 (KN200)	+Device Bus In NPL A2F2 Ⓟ BA160
0	S05	U03	B05	B10
1	S07	U04	D05	B07
2	S09	S03	B09	G03
3	M04	S05	D10	B09
4	P11	J12	D07	G12
5	M02	G12	D02	J04
6	P02	G10	B02	G05
7	S03	J10	D06	G13

3350

CC0180 Seq. 2 of 2	2358359 Part No.	441300 31 Mar 76	441301 1 June 76	441303 30 Jul 76	441306 1 Apr 77	

HEAD ADDRESS REGISTER (HAR) AND DIFFERENCE COUNTER (DIFF) FAILS

Analysis Procedure

- Tags '8C' (Set Diff Counter) and '8B' (Set HAR) activate Tag Gate Valid Dlyd Ⓗ.
- Tag Gate Valid Dlyd activates Enable Reg Resets Ⓖ which resets the HAR and DIFF Counter to '00'.
- Tag '8C' and '8B' then set the Diff Counter and Har with the value on the MST Outbus Bits Ⓔ. Sense Diff Counter (Tag '8F' Bus '09') and Sense HAR (Tag '8F' Bus '05') activate Control.
- Control activates Gate Senses Ⓕ which gates HAR*CAR*Diff Status Bits Ⓚ to the NPL Inbus Bits 0-7 Ⓜ.

A234 ERROR CODE (Bit 0 = 1)

Target Status Bit 0 Ⓝ is active if Sense Target Reg Ⓛ is active.

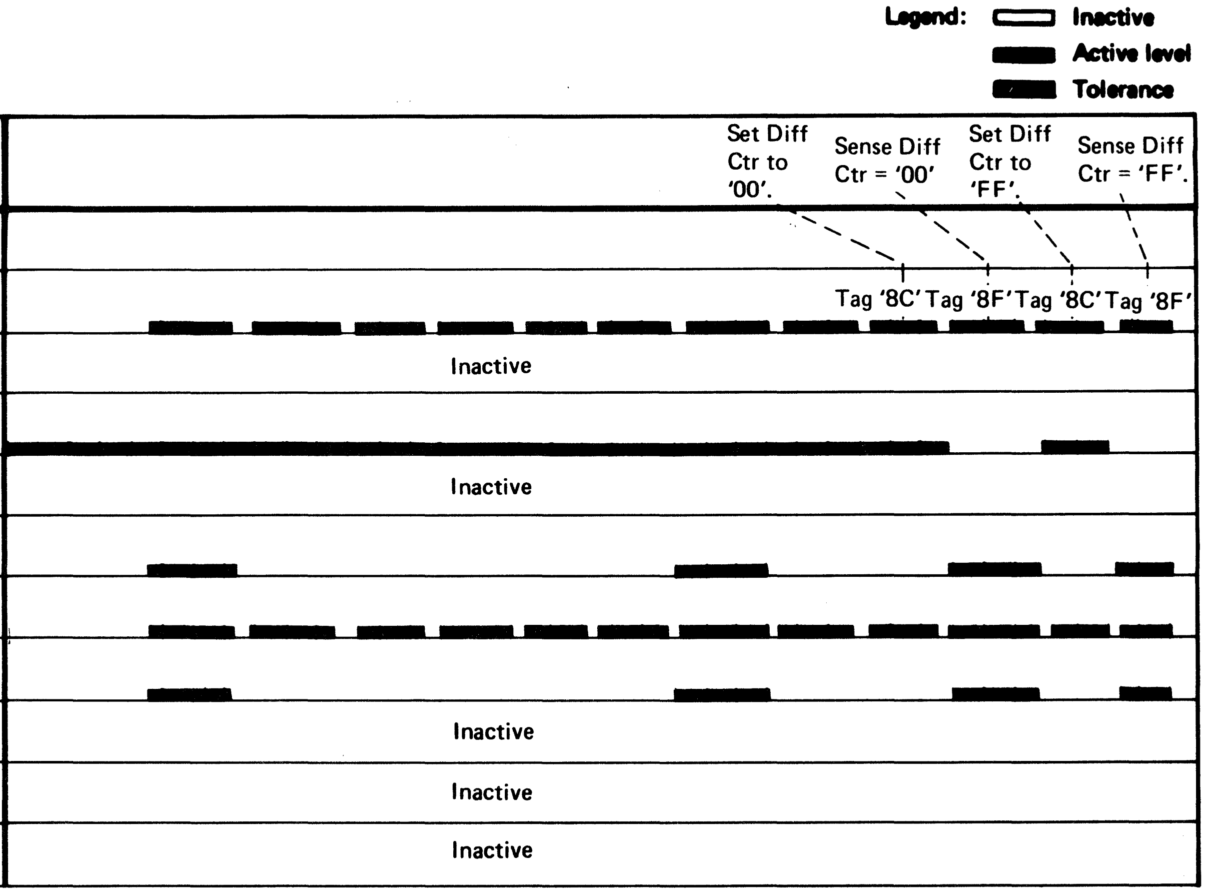
A235 ERROR CODE (Bit 0 = 0)

Suspect File Ctrl Op 8F Ⓠ line is not active at Tag '8F' time.

If Sense Byte 2 = '00', suspect Pwr On Reset Ⓓ or Any Rezero Ⓒ active holding the registers reset. Sequence Rezero Ⓐ causes Any Rezero to be active.

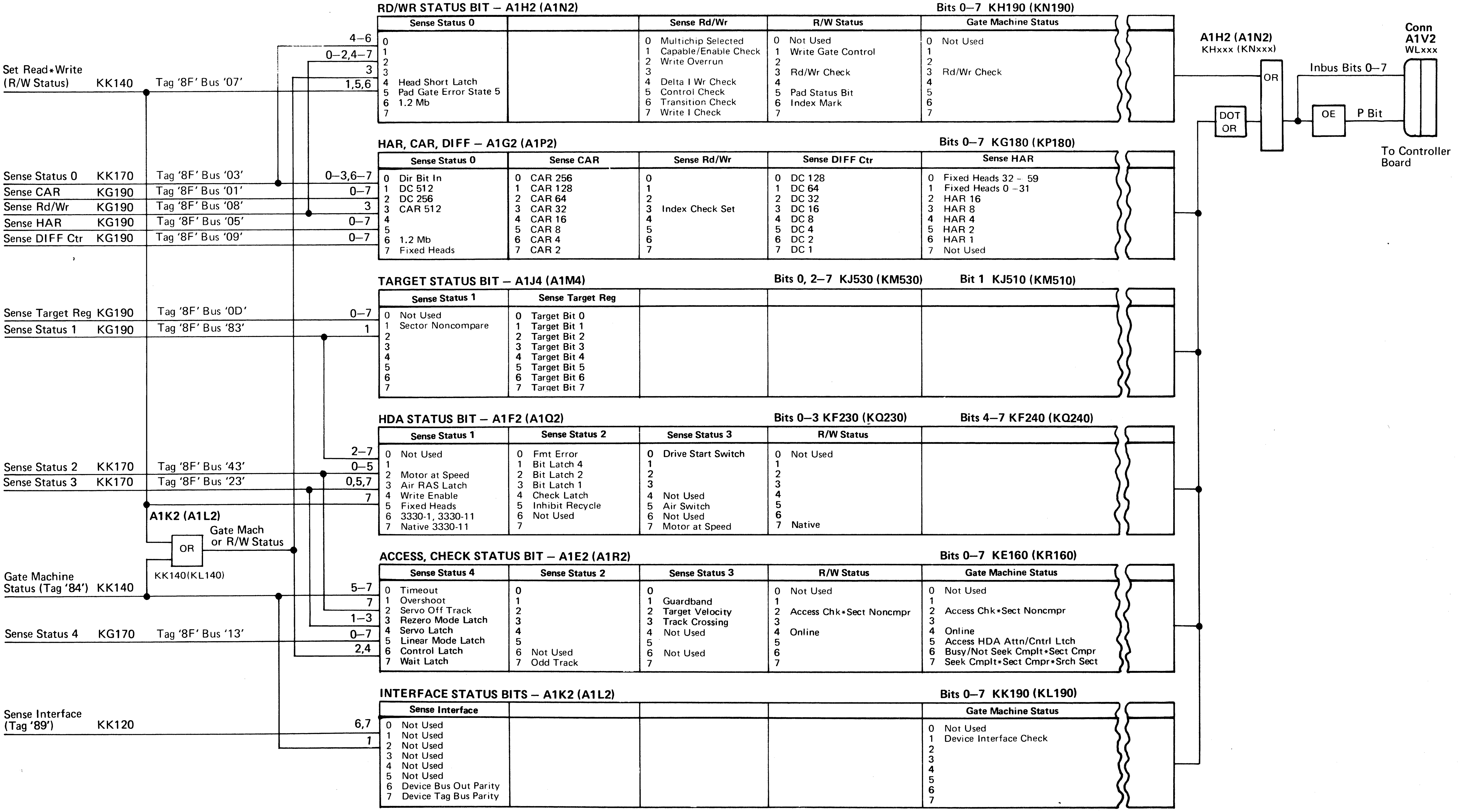
If a single bit is off, scope the inactive bit at the NPL Inbus Bit 0-7 Ⓜ line.

Chart Line No.	Line Name	ALD	Test Point	
1	–MST RAS TP	BD100	A2L2 J11	
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓑ
3	–Pwr On Reset	KK140 (KL140)	A1K2 (A1L2) B04	Ⓓ
4	+Gate Senses	KK170 (KL170)	A1K2 (A1L2) J10	Ⓕ
5	–Enable Reg Resets	KK150 (KL150)	A1K2 (A1L2) J12	Ⓖ
6	+Control	KK120 (KL120)	A1K2 (A1L2) M05	Ⓙ
7	+Tag Gate Valid Dlyd	KK160 (KL160)	A1K2 (A1L2) U02	Ⓗ
8	–File Ctrl Op 8F	BF110	A2G2 D02	Ⓠ
9	–Any Rezero	KG150 (KP150)	A1G2 (A1P2) D04	Ⓒ
10	–Sense Target Reg	KJ510 (KM520)	A1J4 (A1M4) B09	Ⓛ
11	+Sequence Rezero	KF150 (KQ150)	A1F2 (A1Q2) G12	Ⓐ



CC0183 Seq. 1 of 1	2358360 Part No.	441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77		

STATUS BUS BITS



RD/WR STATUS BIT – A1H2 (A1N2)

Bits 0–7 KH190 (KN190)

Sense Status 0		Sense Rd/Wr	R/W Status	Gate Machine Status
0		0 Multichip Selected	0 Not Used	0 Not Used
1		1 Capable/Enable Check	1 Write Gate Control	1
2		2 Write Overrun	2	2
3		3	3 Rd/Wr Check	3 Rd/Wr Check
4 Head Short Latch		4 Delta I Wr Check	4	4
5 Pad Gate Error State 5		5 Control Check	5 Pad Status Bit	5
6 1.2 Mb		6 Transition Check	6 Index Mark	6
7		7 Write I Check	7	7

HAR, CAR, DIFF – A1G2 (A1P2)

Bits 0–7 KG180 (KP180)

Sense Status 0	Sense CAR	Sense Rd/Wr	Sense DIFF Ctr	Sense HAR
0 Dir Bit In	0 CAR 256	0	0 DC 128	0 Fixed Heads 32 - 59
1 DC 512	1 CAR 128	1	1 DC 64	1 Fixed Heads 0 -31
2 DC 256	2 CAR 64	2	2 DC 32	2 HAR 16
3 CAR 512	3 CAR 32	3 Index Check Set	3 DC 16	3 HAR 8
4	4 CAR 16	4	4 DC 8	4 HAR 4
5	5 CAR 8	5	5 DC 4	5 HAR 2
6 1.2 Mb	6 CAR 4	6	6 DC 2	6 HAR 1
7 Fixed Heads	7 CAR 2	7	7 DC 1	7 Not Used

TARGET STATUS BIT – A1J4 (A1M4)

Bits 0, 2–7 KJ530 (KM530) Bit 1 KJ510 (KM510)

Sense Status 1	Sense Target Reg			
0 Not Used	0 Target Bit 0			
1 Sector Noncompare	1 Target Bit 1			
2	2 Target Bit 2			
3	3 Target Bit 3			
4	4 Target Bit 4			
5	5 Target Bit 5			
6	6 Target Bit 6			
7	7 Target Bit 7			

HDA STATUS BIT – A1F2 (A1Q2)

Bits 0–3 KF230 (KQ230) Bits 4–7 KF240 (KQ240)

Sense Status 1	Sense Status 2	Sense Status 3	R/W Status	
0 Not Used	0 Fmt Error	0 Drive Start Switch	0 Not Used	
1	1 Bit Latch 4	1	1	
2 Motor at Speed	2 Bit Latch 2	2	2	
3 Air RAS Latch	3 Bit Latch 1	3	3	
4 Write Enable	4 Check Latch	4 Not Used	4	
5 Fixed Heads	5 Inhibit Recycle	5 Air Switch	5	
6 3330-1, 3330-11	6 Not Used	6 Not Used	6	
7 Native 3330-11	7	7 Motor at Speed	7 Native	

ACCESS, CHECK STATUS BIT – A1E2 (A1R2)

Bits 0–7 KE160 (KR160)

Sense Status 4	Sense Status 2	Sense Status 3	R/W Status	Gate Machine Status
0 Timeout	0	0	0 Not Used	0 Not Used
1 Overshoot	1	1 Guardband	1	1
2 Servo Off Track	2	2 Target Velocity	2 Access Chk∗Sect Noncmpr	2 Access Chk∗Sect Noncmpr
3 Rezero Mode Latch	3	3 Track Crossing	3	3
4 Servo Latch	4	4 Not Used	4 Online	4 Online
5 Linear Mode Latch	5	5	5	5 Access HDA Attn/Cntrl Ltch
6 Control Latch	6 Not Used	6 Not Used	6	6 Busy/Not Seek Cmplt∗Sect Cmpr
7 Wait Latch	7 Odd Track	7	7	7 Seek Cmplt∗Sect Cmpr∗Srch Sect

INTERFACE STATUS BITS – A1K2 (A1L2)

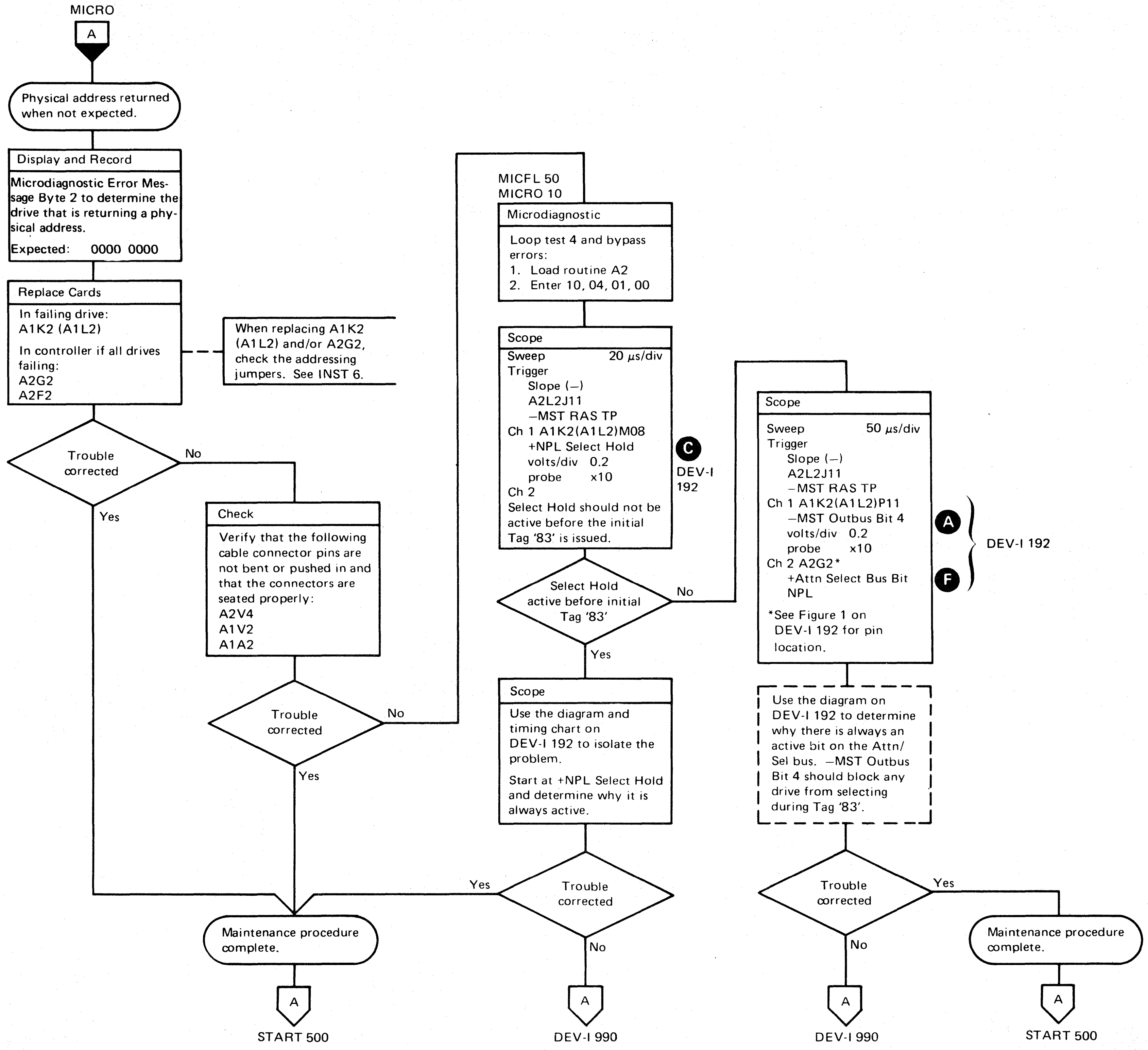
Bits 0–7 KK190 (KL190)

Sense Interface				Gate Machine Status
0 Not Used				0 Not Used
1 Not Used				1 Device Interface Check
2 Not Used				2
3 Not Used				3
4 Not Used				4
5 Not Used				5
6 Device Bus Out Parity				6
7 Device Tag Bus Parity				7

CC0184 Seq. 1 of 2	2358361 Part No.	441300 31 Mar 76				

ADDRESS RETURNED WHEN NOT EXPECTED

The A240 Error Code indicates that a drive physical address was returned when a Select was issued with Outbus Bit 4 on.



CC0184 Seq. 2 of 2	2358361 Part No.	441300 31 Mar 76				

ADDRESS RETURNED WHEN NOT EXPECTED

Circuit Description

The microdiagnostic issues a Select to a drive with MST Outbus Bit 4 Ⓐ on. MST Outbus Bit 4 blocks the Select and does not allow the drive address to be placed on the Attn Select Bus.

Analysis Procedure

The drive address appears on the Attn Select Bus in error because:

- +Selected Ⓔ is active. (+Selected is blocked by –MST Outbus Bit 4 active.)
- +NPL Select Hold Ⓒ is active before the initial Tag '83' is issued.

See OPER 92 for additional theory.

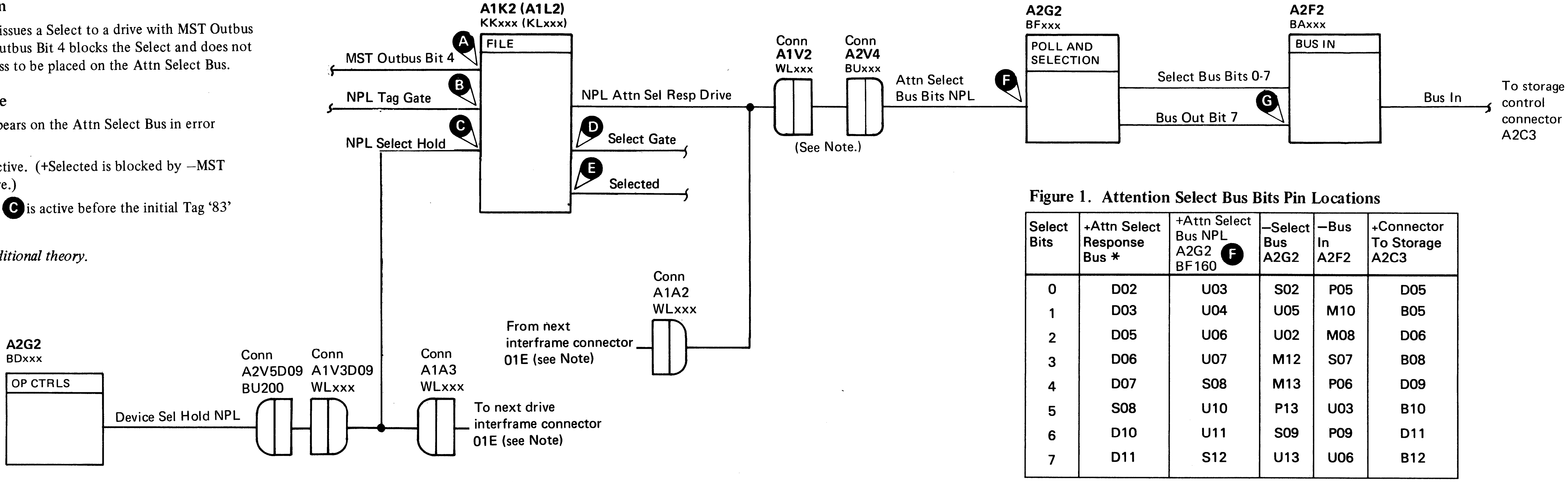


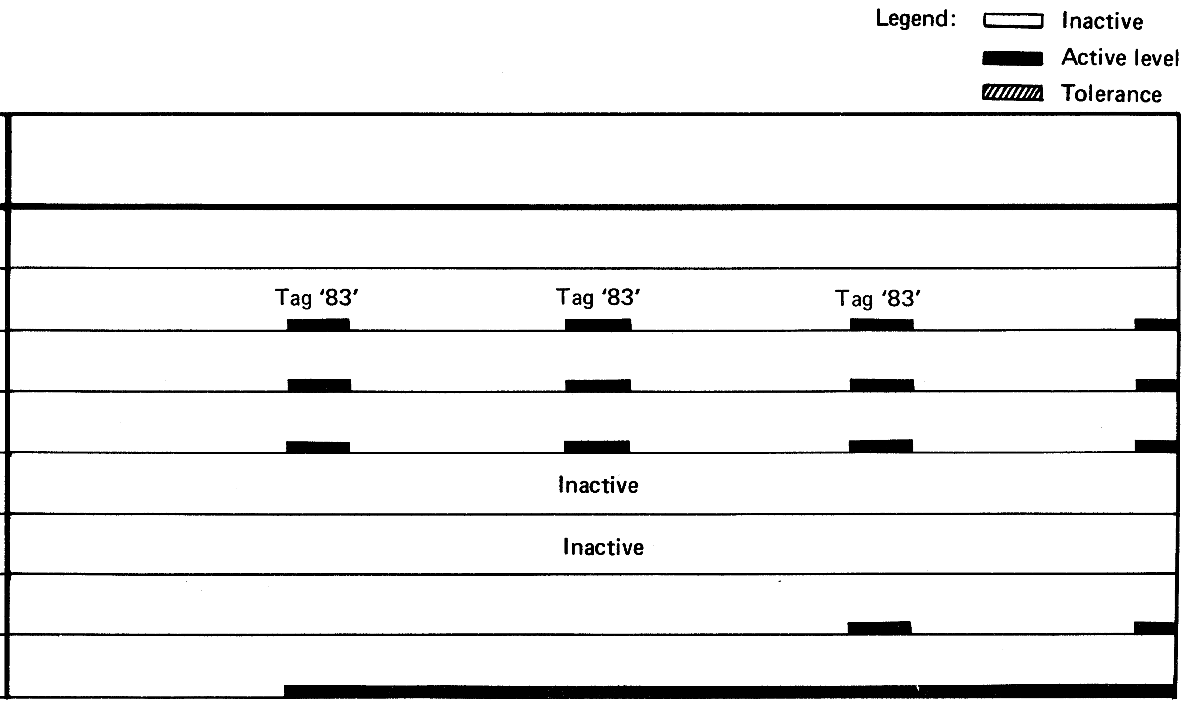
Figure 1. Attention Select Bus Bits Pin Locations

Select Bits	+Attn Select Response Bus *	+Attn Select Bus NPL A2G2 Ⓕ BF160	–Select Bus A2G2	–Bus In A2F2	+Connector To Storage A2C3
0	D02	U03	S02	P05	D05
1	D03	U04	U05	M10	B05
2	D05	U06	U02	M08	D06
3	D06	U07	M12	S07	B08
4	D07	S08	M13	P06	D09
5	S08	U10	P13	U03	B10
6	D10	U11	S09	P09	D11
7	D11	S12	U13	U06	B12

*Pins located on connectors A1V2, A1A2, and A2V4.

Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

Chart Line No.	Line Name	ALD	Test Point		
1	–MST RAS TP	BD100	A2L2 J11		
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓑ	Tag '83' Tag '83' Tag '83'
3	+Select Gate	KK140 (KL140)	A1K2 (A1L2) P13	Ⓓ	
4	–MST Outbus Bit 4	KK110 (KL110)	A1K2 (A1L2) P11	Ⓐ	
5	+Selected	KK190 (KL190)	A1K2 (A1L2) G12	Ⓔ	Inactive
6	+Attn Select Bus Bits NPL	BF160	See Figure 1.	Ⓕ	Inactive
7	–Bus Out Bit 7	BA130	A2F2 U13	Ⓖ	
8	+NPL Select Hold	KK100 (KL100)	A1K2 (A1L2) M08	Ⓒ	

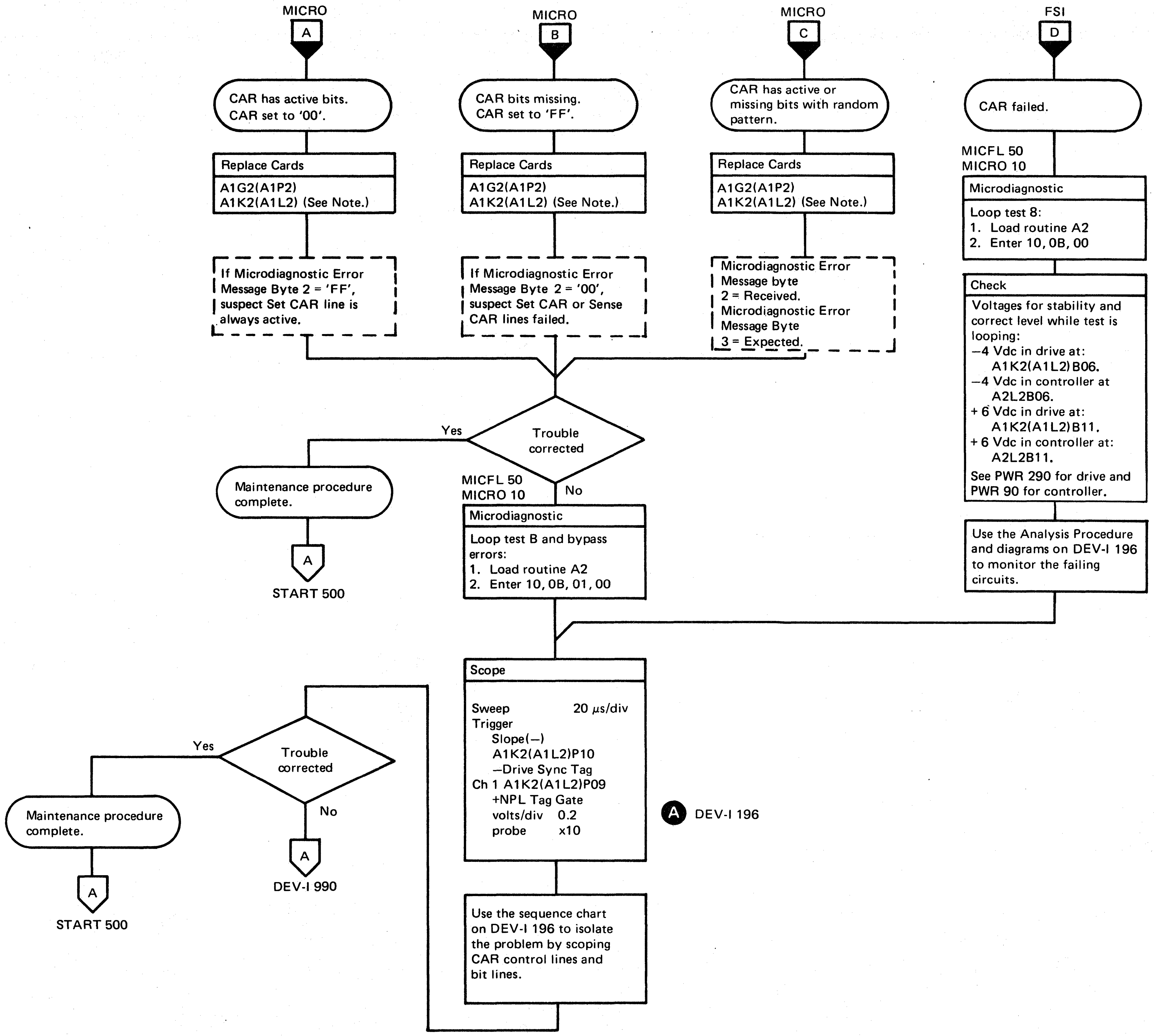


CC0192 Seq. 1 of 2	2358362 Part No.	441300 31 Mar 76	441303 30 Jul 76			

CYLINDER ADDRESS REGISTER (CAR)

The microdiagnostic sets and senses CAR to '00', 'FF', and a sliding ones pattern.

Note: *When replacing A1K2 (A1L2) and/or A2G2, check the addressing jumpers. See INST 6.*



3350	CC0192 Seq. 2 of 2	2358362 Part No.	441300 31 Mar 76	441303 30 Jul 76		

CYLINDER ADDRESS REGISTER (CAR)

Analysis Procedure

The microdiagnostic issues a Set CAR command (Tag '8E') and senses CAR (Tag '8F') for the correct value.

Since the HAR*CAR*Diff registers have been tested earlier in the microprogram, check the +Set CAR line for proper operation. If the Error Code is A2B4, change the time base on the scope to 50 μs. The Set and Sense CAR commands for the sliding ones pattern occur after the 'FF' pattern is set in the following sequence:

Tag '8F' Bus '01'	Sense CAR for 'FF'.
Tag '8F' Bus '01'	Sense CAR for Parity Check.
Tag '8F' Bus '01'	Sense CAR for Bus In = Bus Out. (An A2B4 Error Code occurs if Bus In is not equal to Bus Out.)

See OPER 92 for additional theory.

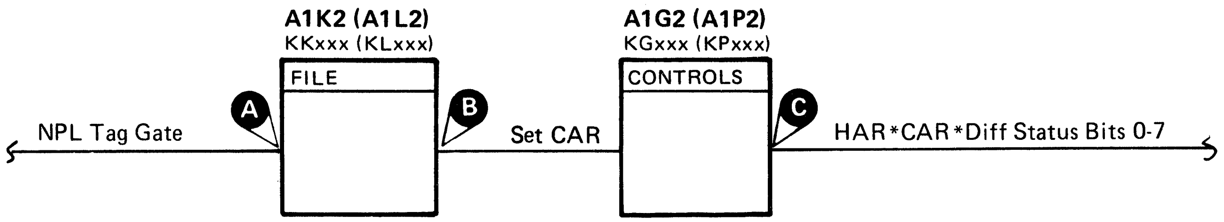
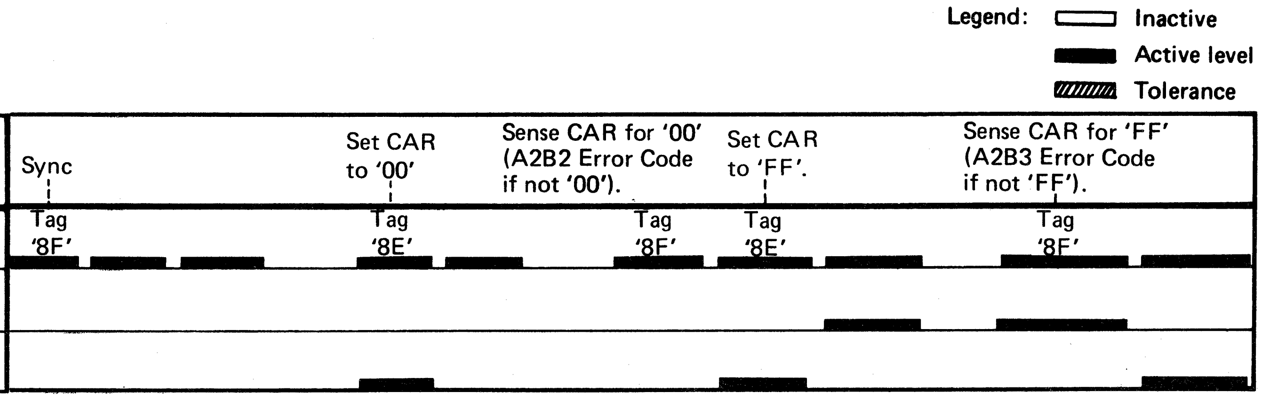


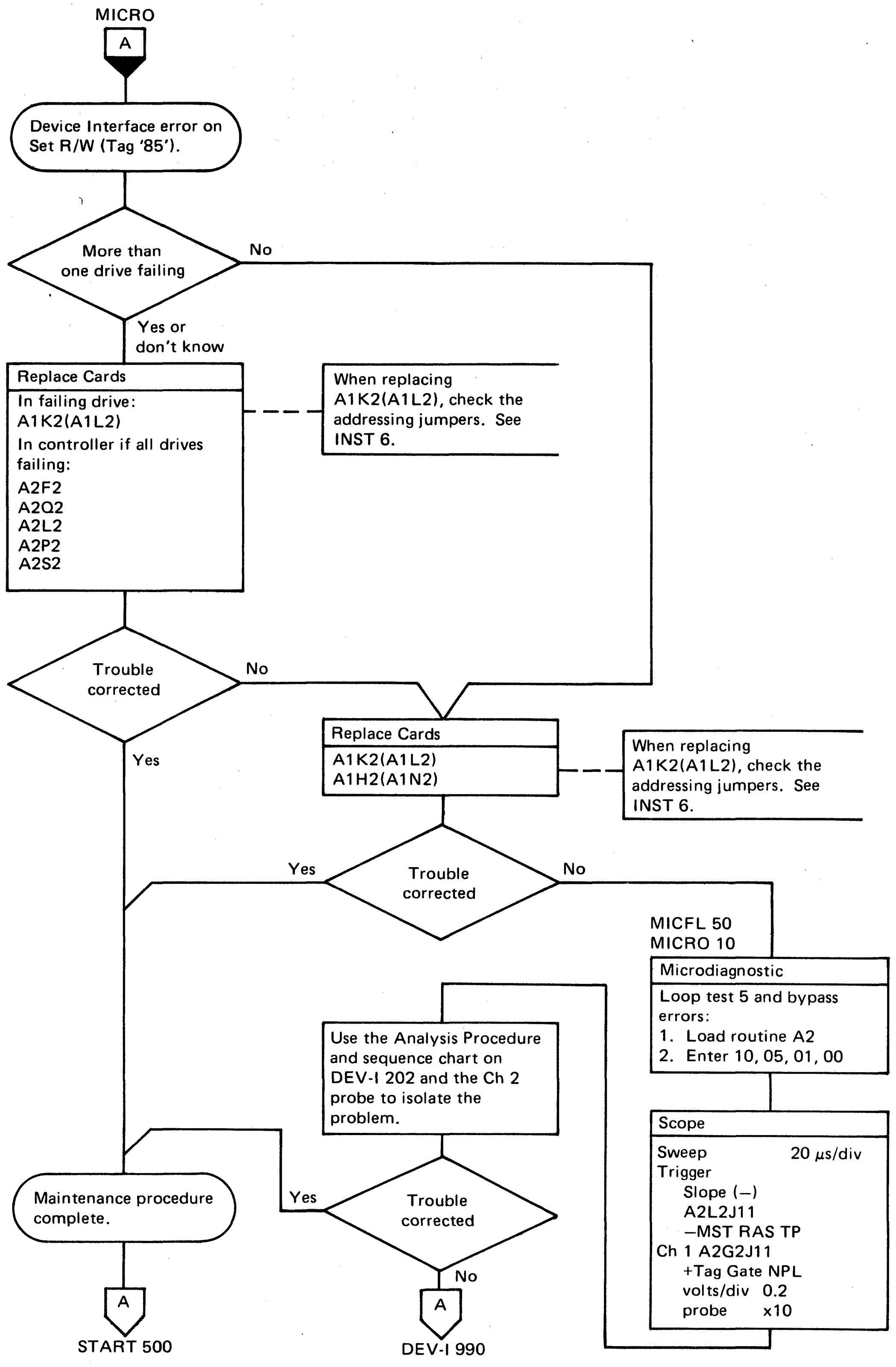
Figure 1. CAR Bit Pin Locations

Bits	+HAR*CAR*Diff Status A1G2 (A1P2) KG180 (KP180) Ⓒ
0	U03
1	U04
2	S03
3	S05
4	J12
5	G12
6	G10
7	J10

Chart Line No.	Line Name	ALD	Test Point	
1	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓐ
2	+HAR*CAR*Diff Status Bits 0-7	KG180 (KP180)	See Figure 1.	Ⓒ
3	+Set CAR	KG150 (KP150)	A1G2 (A1P2) D06	Ⓑ



DEVICE INTERFACE ERROR ON R/W



3350	CC0196 Seq. 2 of 2	2358363 Part No.	441300 31 Mar 76	441303 30 Jul 76			

DEVICE INTERFACE ERROR ON R/W

Analysis Procedure

This error occurs when:

Any line Ⓒ through Ⓖ is active.
Rd Wrt Gate is inactive (BA140).
AM Found is inactive (BC140).
Set Read/Write on KK170 (KL170) is inactive.

Set Read/Write (Tag '85') switches the Device Outbus bits Ⓚ to a Read/Write Control bus. Bits 5, 6, and 7 are forced to the active state, and bit P is forced to the inactive state. Device Outbus Parity is only checked for an instant and then it is blocked to allow varying values during Read/Write Control.

See OPER 92 for additional theory.

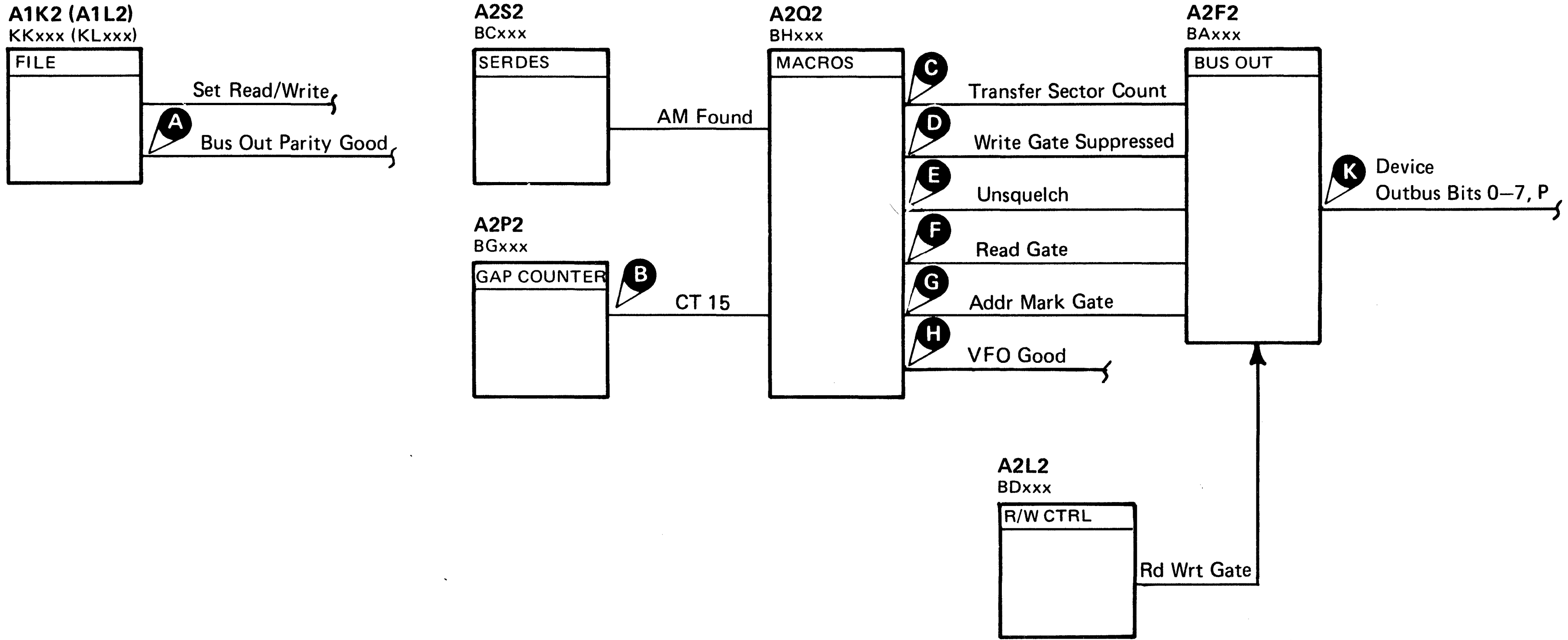
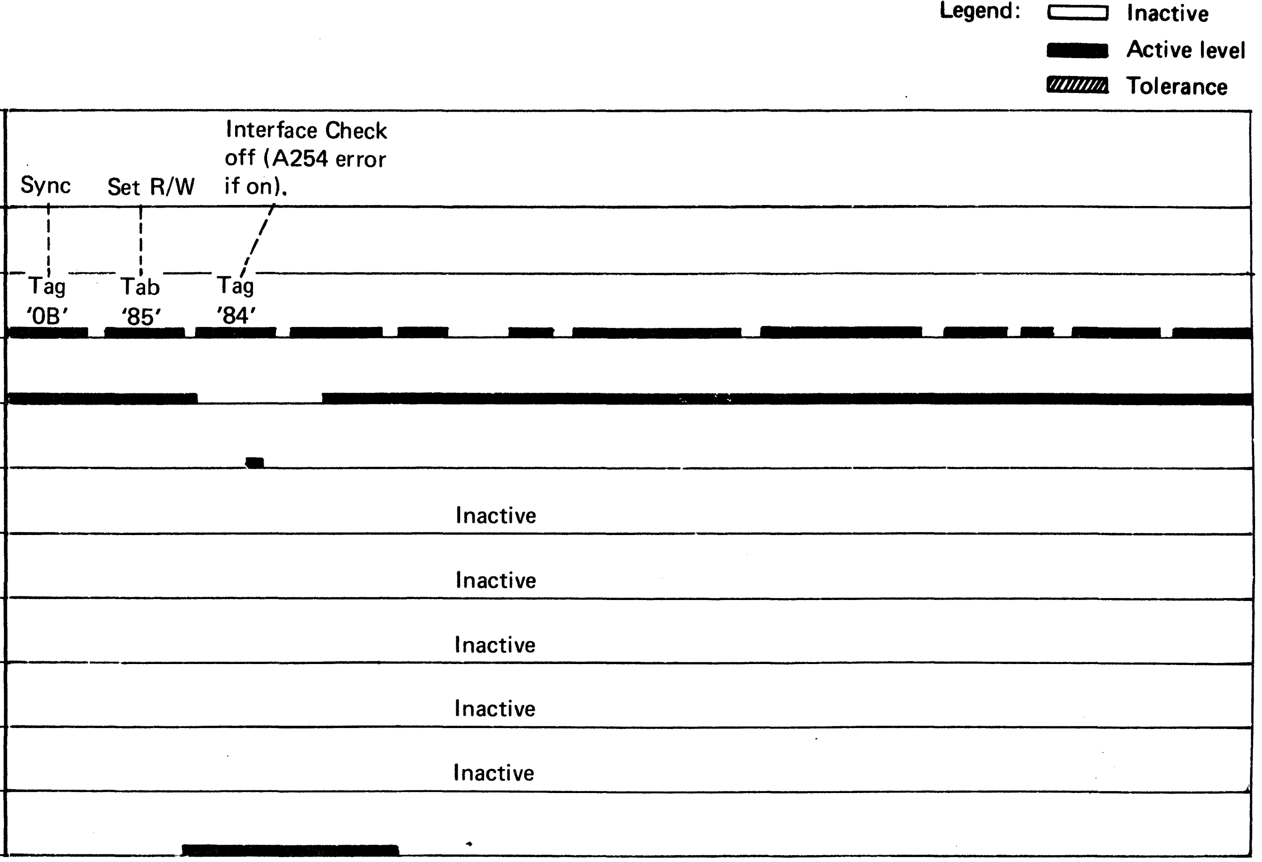


Figure 1. Outbus Bits 0-7, P Pin Locations

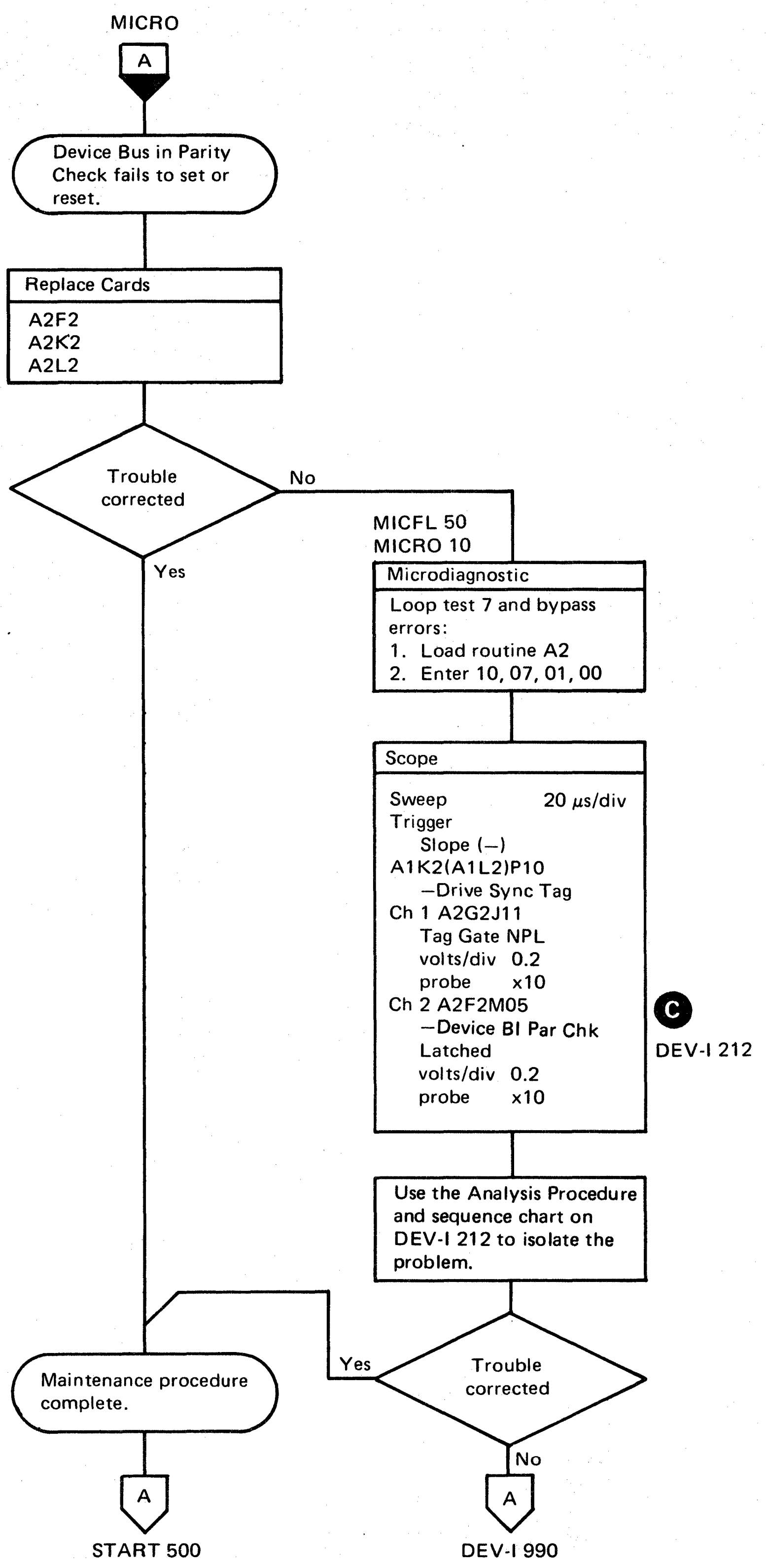
Bits	+Device Outbus A2F2 BA110 Ⓚ
0	P10
1	P12
2	U02
3	S03
4	S12
5	U12
6	U05
7	U09
P	M07

Chart Line No.	Line Name	ALD	Test Point	
1	−MST RAS TP	BD100	A2L2 J11	
2	+Tag Gate NPL	BD130	A2G2 J11	
3	+Bus Out Parity Good	KK190 (KL190)	A1K2 (A1L2) P07	Ⓐ
4	−CT 15	BG120	A2P2 B09	Ⓑ
5	−Transfer Sector Count	BA140	A2F2 P03	Ⓒ
6	−Write Gate Suppressed	BA140	A2F2 P04	Ⓓ
7	−Unsquelch	BA140	A2F2 U07	Ⓔ
8	−Read Gate	BA140	A2F2 S08	Ⓕ
9	−Addr Mark Gate	BA140	A2F2 S02	Ⓖ
10	−VFO Good	BH150	A2Q2 S13	Ⓗ



3350	CC0202 Seq. 1 of 2	2358364 Part No.	441300 31 Mar 76	441303 30 Jul 76		

DEVICE BUS IN PARITY CHECK



DEVICE BUS IN PARITY CHECK

Analysis Procedure

The microdiagnostic forces Device B1 Par Check Latched Ⓒ active by inverting the Bus In Parity bit (Tag '05' Bus '20') and verifies that the latch is on at Tag '04' time. A Controller Reset (Tag '09' Bus '10') is issued and the latch is checked for an off condition at the following Tag '04' time.

See OPER 92 for additional theory.

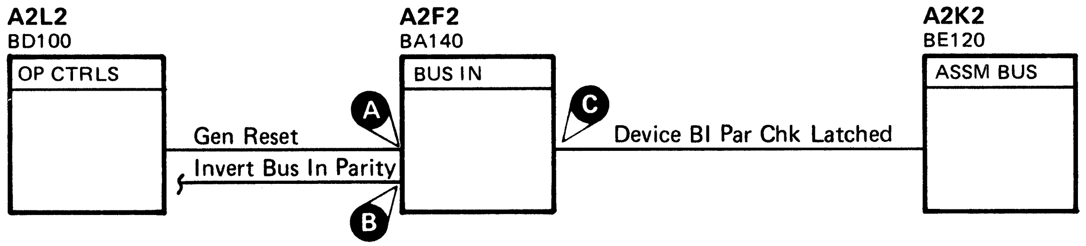
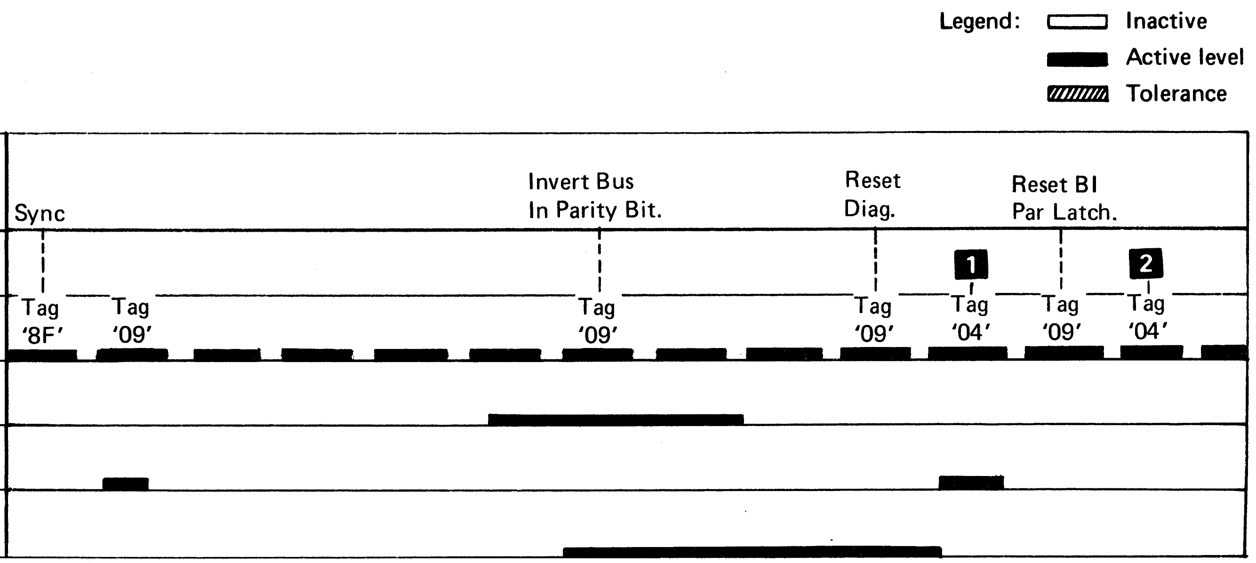


Chart Line No.	Line Name	ALD	Test Point	
1	−Drive Sync Tag	KK170 (KL170)	A1K2 (A1L2) P10	
2	+Tag Gate NPL	BF130	A2G2 J11	
3	−Invert Bus In Par	BA120	A2F2 P07	Ⓑ
4	+Gen Reset	BA140	A2F2 M11	Ⓐ
5	−Device BI Par Chk Latched	BA140	A2F2 M05	Ⓒ

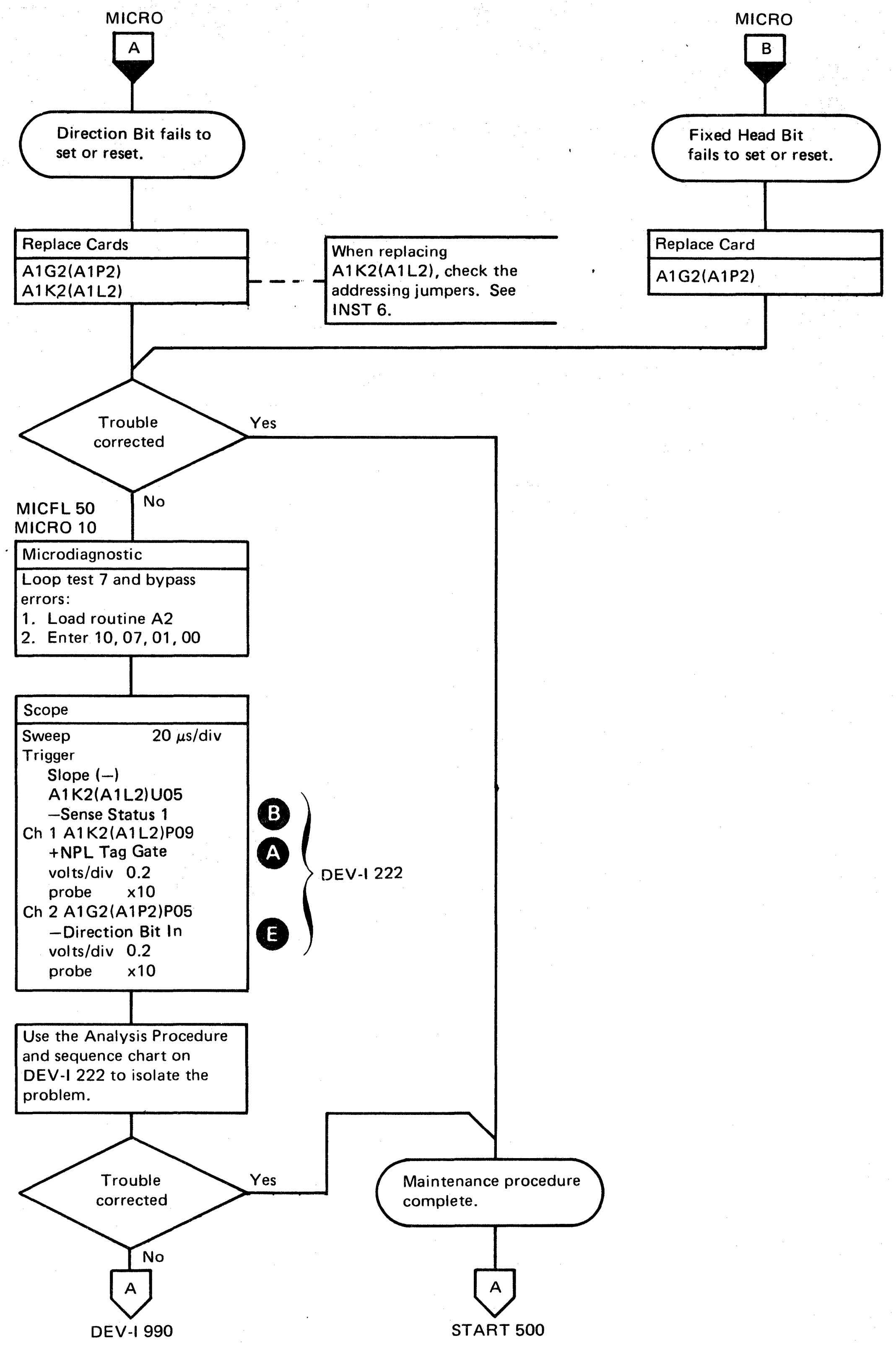


1 Check for Bus In Parity Check latch on (if not on, an A270 Error Code occurs).

2 Check for Bus In Parity Check latch off (if on, an A271 Error Code occurs).

CC0212 Seq. 1 of 2	2358365 Part No.	441300 31 Mar 76	441303 30 Jul 76

DIRECTION BIT OR FIXED HEAD BIT FAILS



DIRECTION BIT OR FIXED HEAD BIT FAILS

Analysis Procedure

A273 ERROR CODE

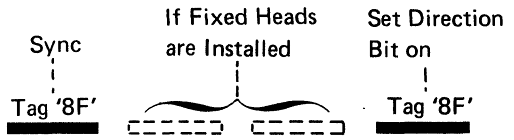
HAR Bit 1 is the Fixed Head Bit. The microdiagnostic sets HAR Bit 1 on (Tag '8B' Bus '40') and senses for the on condition (Tag '8F' Bus '05'). An A273 Error Code occurs if the HAR Bit 1 is not on in the following sequence:

Tag '8F' Bus '83'	(Sync) Sense Status 1. Check if fixed heads are installed.
Tag '8B' Bus '40'	Set Fixed Head Bit on.
Tag '8F' Bus '05'	Sense for Fixed Head Bit. An A273 Error Code occurs if not on.

A274 ERROR CODE

Difference Counter Bit 1 is the Direction Bit. The microdiagnostic sets the Direction Bit on (Tag '8F' Bus '8E') and senses for the on condition (Tag '8F' Bus '03'). The Direction Bit is then reset (Tag '8F' Bus '0E') and sensed for the off condition (Tag '8F' Bus '03').

The sequence chart indicates the tag sequence without fixed heads installed. If fixed heads are installed, two tags occur before the Direction Bit is set on:



The microdiagnostic sets the Direction Bit latch on and verifies that the latch is on. It then issues a reset and checks that the latch is off.

–Direction Bit In Ⓔ latch is set by:
  –MST Outbus Bit 0 (KG190) is active and
  Fixed heads installed.

+HAR*CAR*Diff Status 0 Ⓓ is active when:
  –Direction Bit In latch is set.
  –Sense Status 0 Ⓒ is active.

–Sense Status 0 is active when:
  –Sense Status is active
  +0B0 is inactive
  +0B1 is inactive
  +0B2 is inactive
  +0B3 is inactive

See OPER 92 for additional theory.

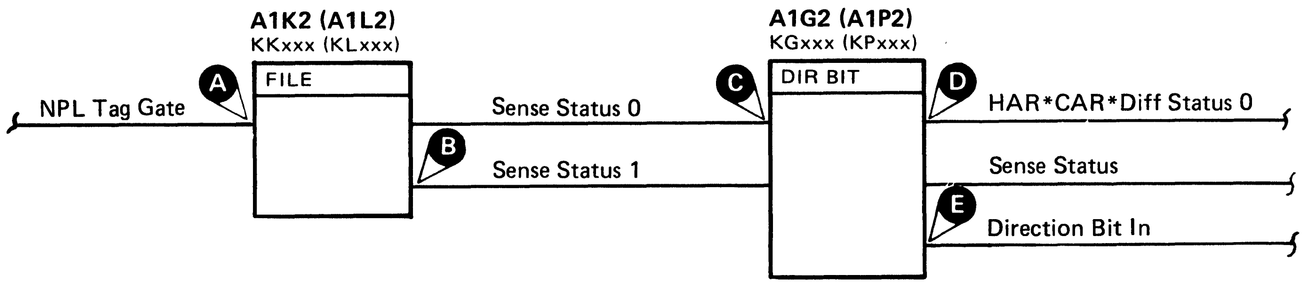
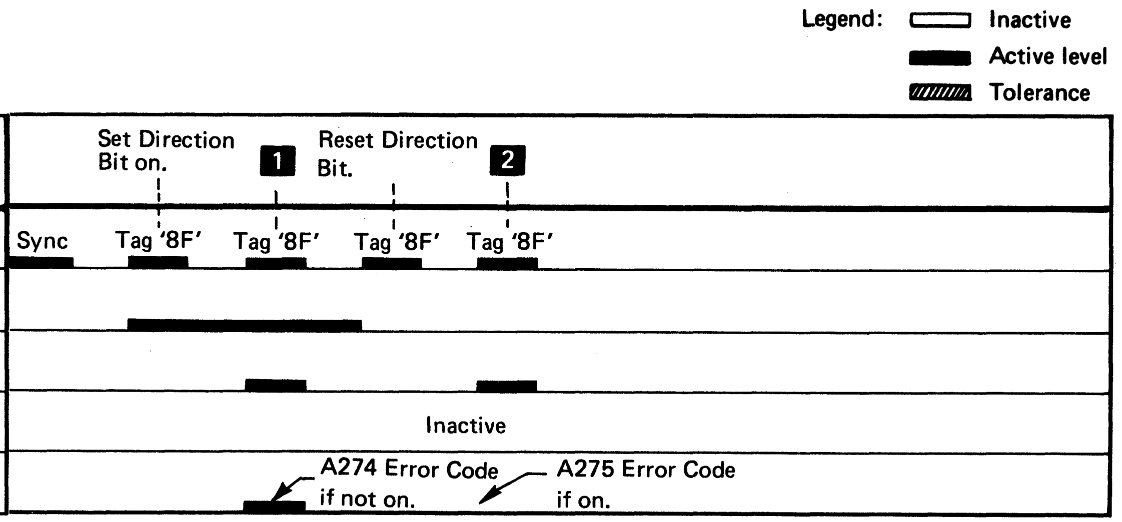


Chart Line No.	Line Name	ALD	Test Point	
1	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓐ
2	–Direction Bit In	KG190 (KP190)	A1G2 (A1P2) P05	Ⓔ
3	–Sense Status 0	KG190 (KP190)	A1G2 (A1P2) P09	Ⓒ
4	–Sense Status 1	KK170 (KL170)	A1K2 (A1L2) U05	Ⓑ
5	+HAR*CAR*Diff Status 0	KG180 (KP180)	A1G2 (A1P2) U03	Ⓓ

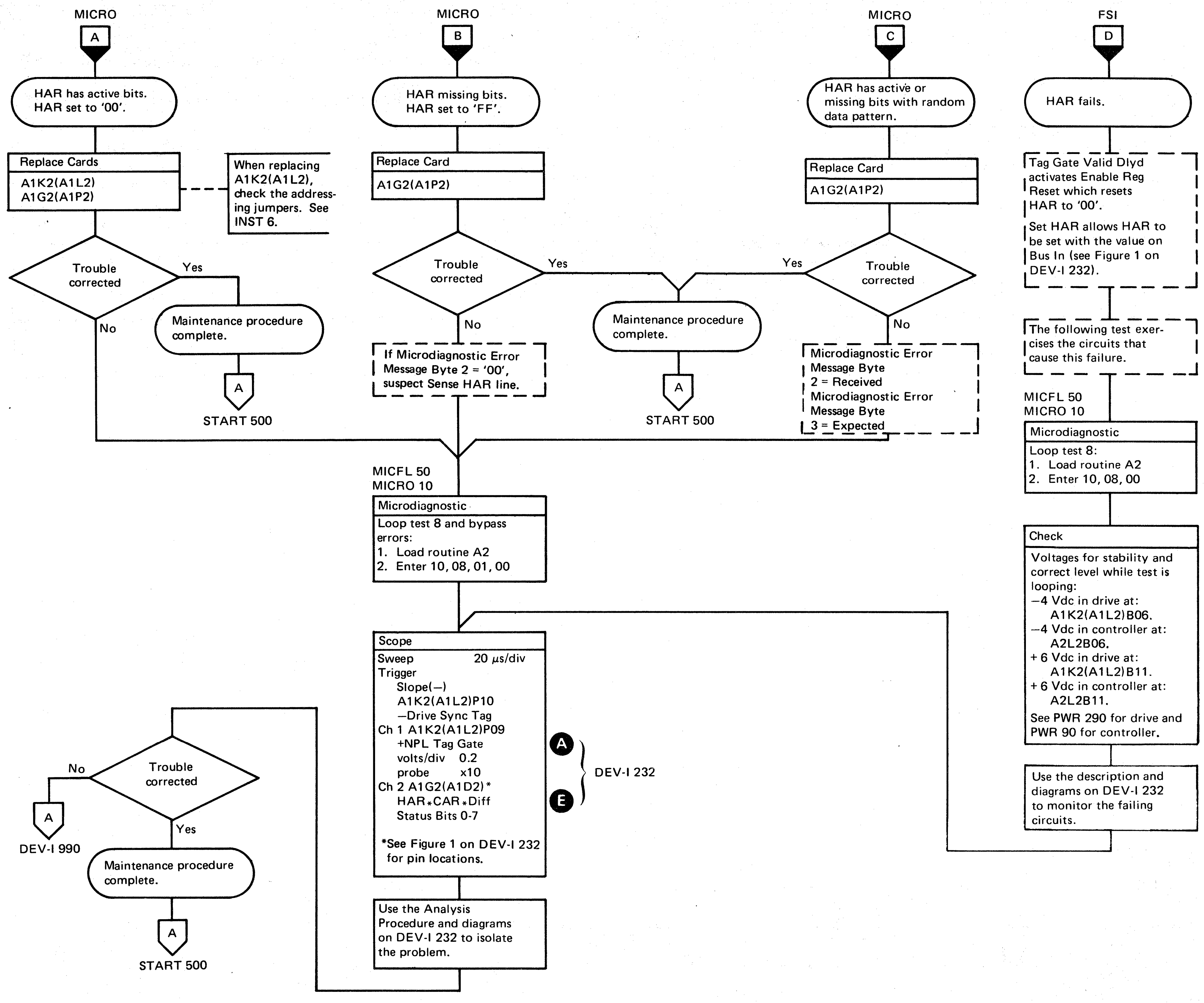


1 Sense for Direction Bit on. If not on, an A274 Error Code occurs.

2 Sense for Direction Bit off. If not off, an A275 Error Code occurs.

HEAD ADDRESS REGISTER (HAR)

The microdiagnostic sets and senses HAR to '00', 'FF', and a sliding ones pattern.



HEAD ADDRESS REGISTER (HAR)

Analysis Procedure

HAR*CAR*Diff bits have been tested earlier in the microprogram.

Suspect that Set HAR Ⓑ or Sense HAR (KG160, KP160) lines cause the error.

Set HAR (Tag '8B') resets HAR before setting it.

The Set HAR command and the Enable function load HAR with the value on MST Outbus, bits 0–7.

Tag Gate Valid Dlyd Ⓓ and Enable Reg Reset Ⓒ resets HAR to '00' in the following sequence:

Tag '8F' Bus '0A'	Drive Sync
Tag '8F' Bus '04'	Attention Reset
Tag '89'	Sense Interface
Tag '8B' Bus '00'	Set HAR to '00'
Tag '8F' Bus '05'	Sense HAR (Control Interface Checks off)
Tag '8F' Bus '05'	Sense HAR for '00'
Tag '8B' Bus 'FF'	Set HAR to off
Tag '8F' Bus '05'	Sense HAR (Control Interface Checks off)
Tag '8F' Bus '05'	Sense HAR for 'FF'

See OPER 92 for additional theory.

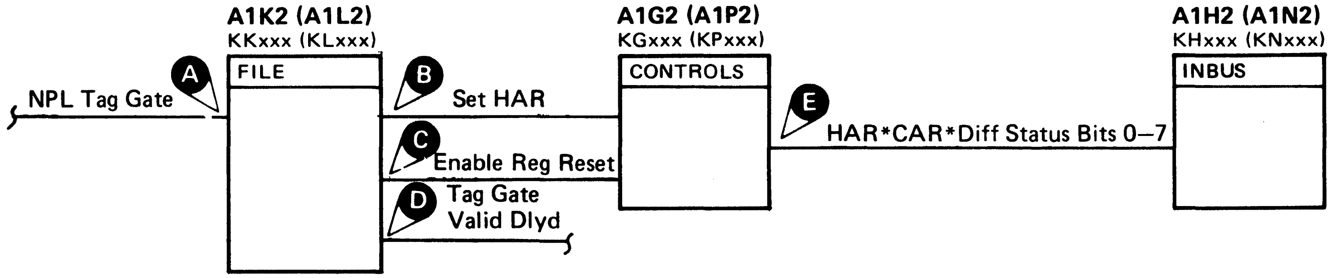
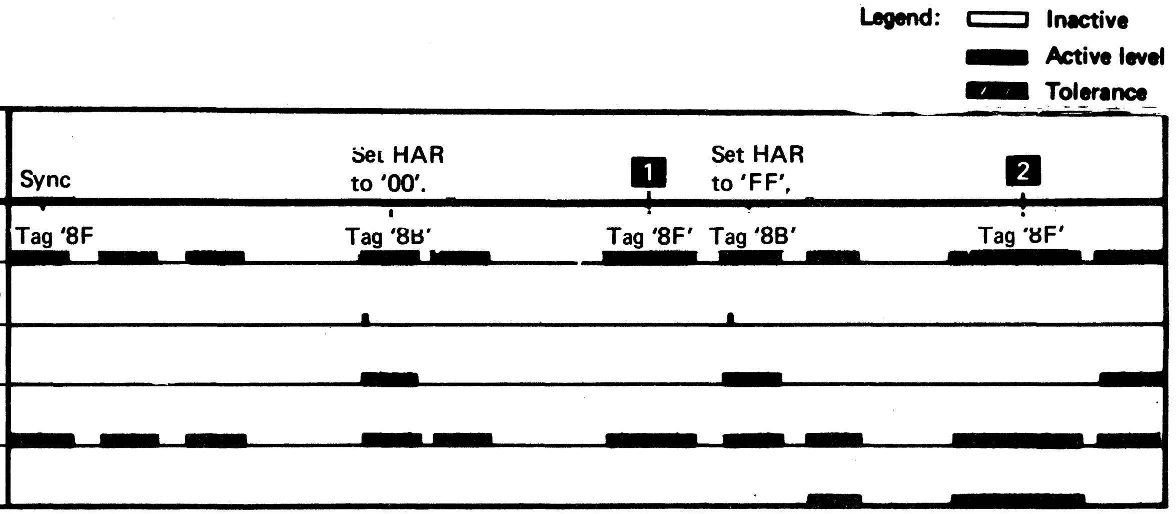


Figure 1. HAR Bits Pin Location

Bits	+HAR*CAR*Diff Status Ⓔ A1G2(A1P2) KG180(KP180)
0	U03
1	U04
2	S03
3	S05
4	J12
5	G12
6	G10
7	J10

Chart Line No.	Line Name	ALD	Test Point	
1	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓐ
2	–Enable Reg Reset	KK150 (KL150)	A1K2 (A1L2) J12	Ⓒ
3	+Set HAR	KG150 (KP150)	A1G2 (A1P2) B04	Ⓑ
4	+Tag Gate Valid Dlyd	KK150 (KL150)	A1K2 (A1L2) G09	Ⓓ
5	+HAR*CAR*Diff Status Bits 0-7	KG180 (KP180)	See Figure 1.	Ⓔ



1 Sense HAR for '00'. All HAR bits should be off or an A282 Error Code occurs.

2 Sense HAR for 'FF'. All HAR bits should be on or an A283 Error Code occurs.

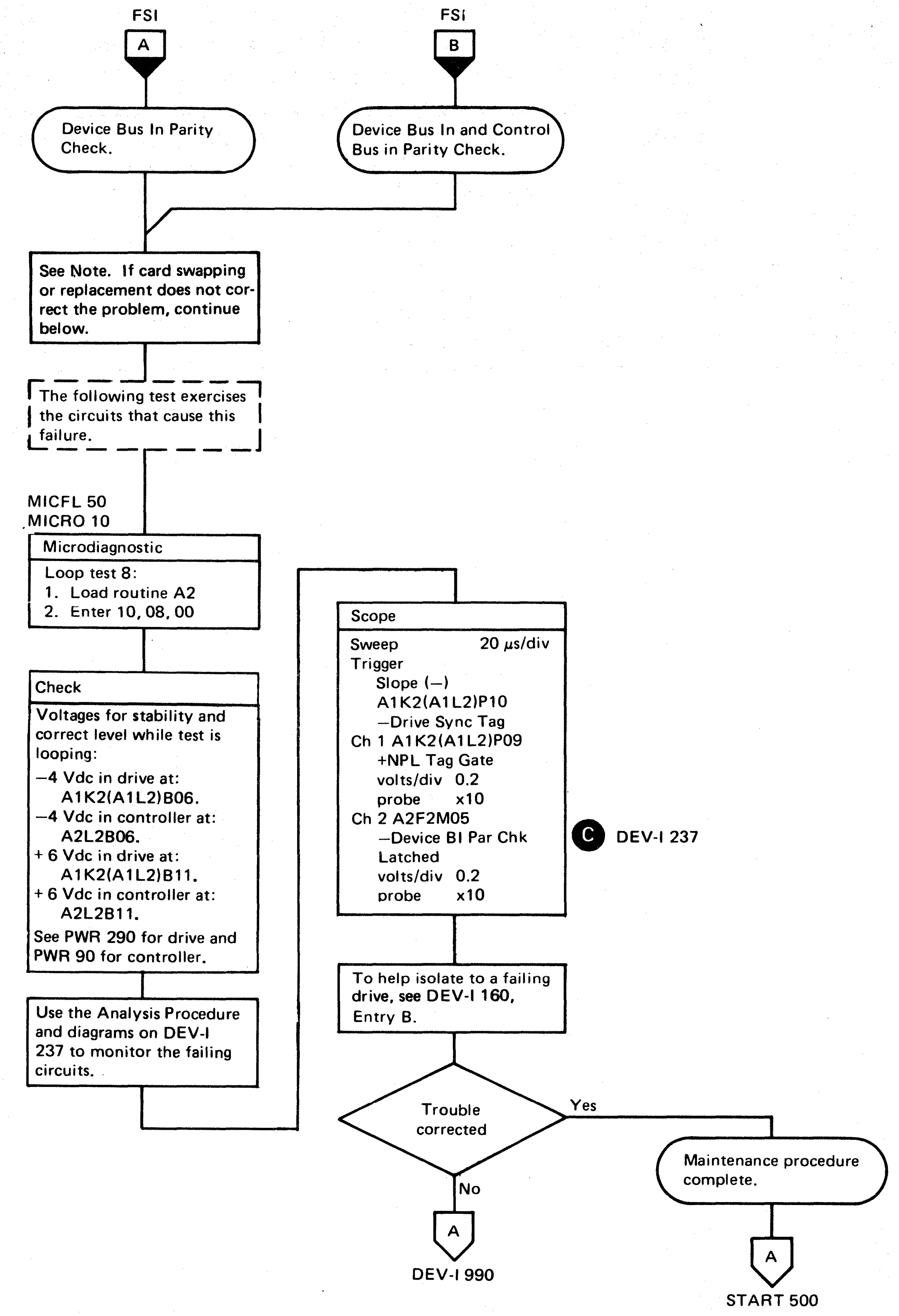
BUS IN PARITY

Note: *(See DEV-I 184.) Each bit on the Device Bus In is affected by six different cards in each drive.*

Drive A		Drive B	
A1E2	*Dot OR at A1H2*	*A1R2*	*Dot OR at A1N2*
A1F2		*A1Q2*	
A1G2		*A1P2*	
A1J4		*A1M4*	
A1K2		*A1L2*	

Any one of these cards can cause a bit to remain active or inactive. If the error remains after replacing or swapping cards, perform the following:

1. *ALWAYS ACTIVE BIT – Scope the failing line.*
   - a. *If the bit line is at a + level (MST-1), remove the cards one at a time until the line drops to – level (MST-1). If all cards are removed and the bit line is still active, look for tight wire wraps, bent pins, etc.*
   - b. *If the bit line is still at a – level (MST-1), return to the flowchart.*
2. *ALWAYS INACTIVE BIT – Return to the flowchart.*



3350	CC0232 Seq. 2 of 2	2358367 Part No.	441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77		

BUS IN PARITY

Analysis Procedure

The microdiagnostic sets a pattern of bits in the Head Address Register (HAR) and compares the Bus In and Bus Out values each time. When the Device BI Par Chk Latched Ⓒ is active and the Bus In equal the Bus Out, an A281 Error Code occurs.

A failure in the parity bit circuits exists at the Parity Bit Generator or between the generator and the controller.

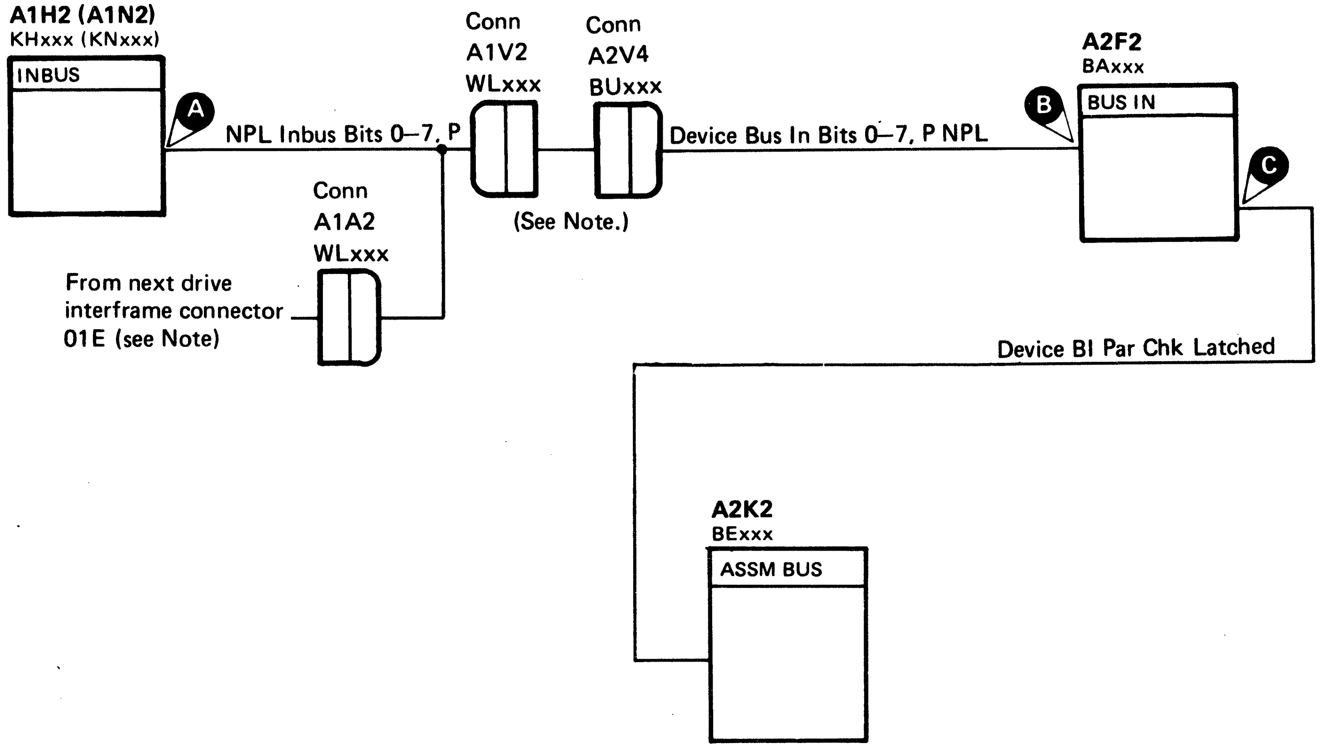
To help isolate a failing drive, see DEV-I 160, Entry B.

See OPER 92 for additional theory.

Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

Figure 1. Inbus Bits 0-7, P Pin Locations

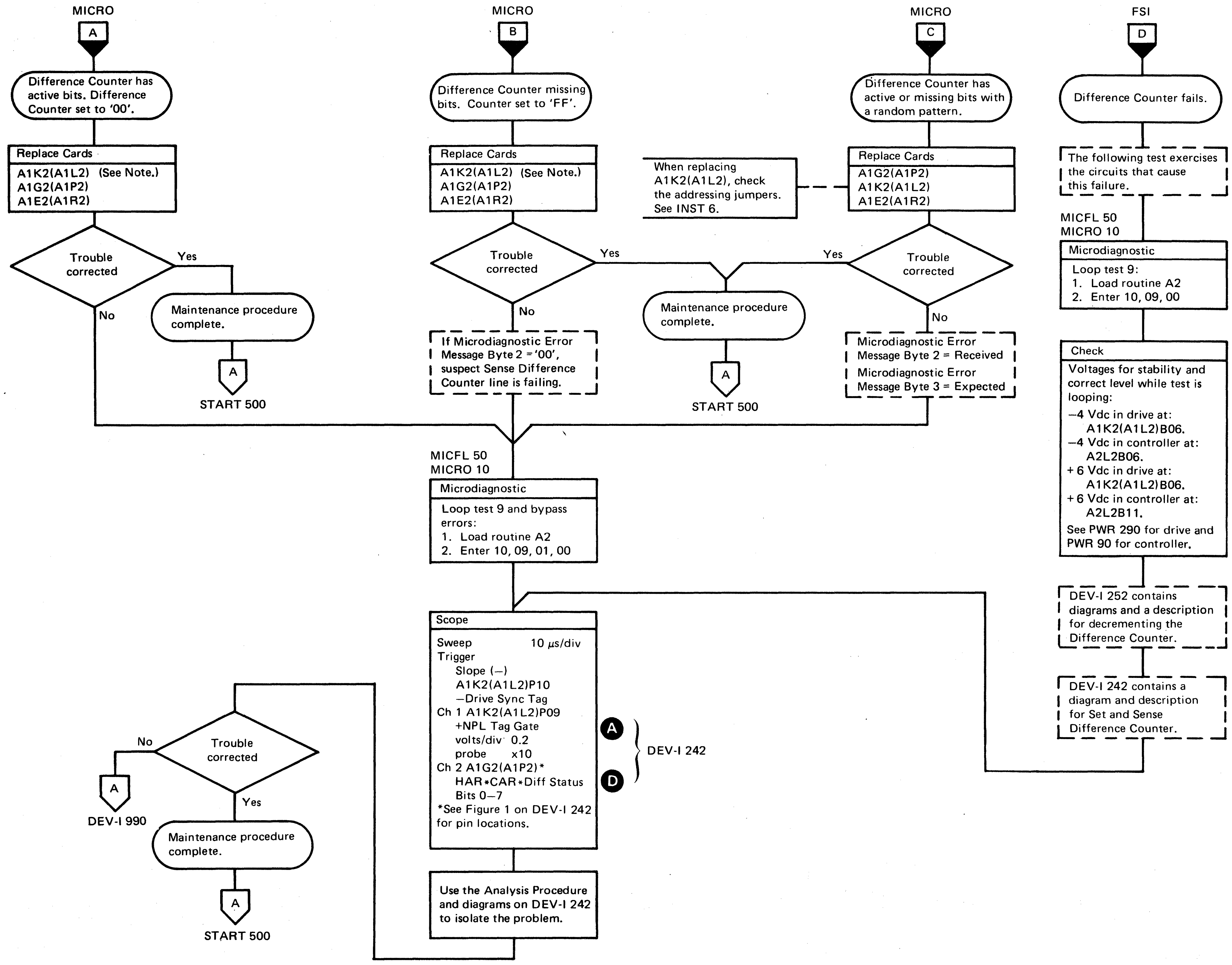
Bits	+NPL Inbus A1H2 (A1N2) Ⓐ	+Device Bus In NPL A2F2 Ⓑ
0	B05	B10
1	D05	B07
2	B09	G03
3	D10	B09
4	D07	G12
5	D02	J04
6	B02	G05
7	D06	G13
P	B07	J13



DIFFERENCE COUNTER (DIFF)

The microdiagnostic sets and senses the Difference Counter for '00', 'FF', and a sliding ones pattern.

Note: *When replacing A1K2(A1L2), check the addressing jumpers. See INST 6.*



3350	CC0237 Seq. 2 of 2	2358368 Part No.	441300 31 Mar 76	441303 30 Jul 76			

DIFFERENCE COUNTER (DIFF)

Analysis Procedure

SET DIFFERENCE COUNTER (TAG '8C')

The Set Difference Counter (Tag '8C') resets the Difference Counter before setting it. The Set Diff Count Ⓑ and Enable Function lines set the Difference Counter to the value on the MST Outbus.

Dec Diff Ⓔ and DC 7 Ⓒ should not be active during this test.

SENSE DIFFERENCE COUNTER (TAG '8F' BUS '09')

The Sense Difference Counter (Tag '8F' Bus '09') gates the Difference Counter value to the Device Inbus.

Since the HAR*CAR*Diff Status Bits are checked earlier in the microprogram, suspect the Set Diff Count Ⓑ, Dec Diff Ⓔ, DC7 Ⓒ, or the Difference Registers.

See OPER 92 for additional theory.

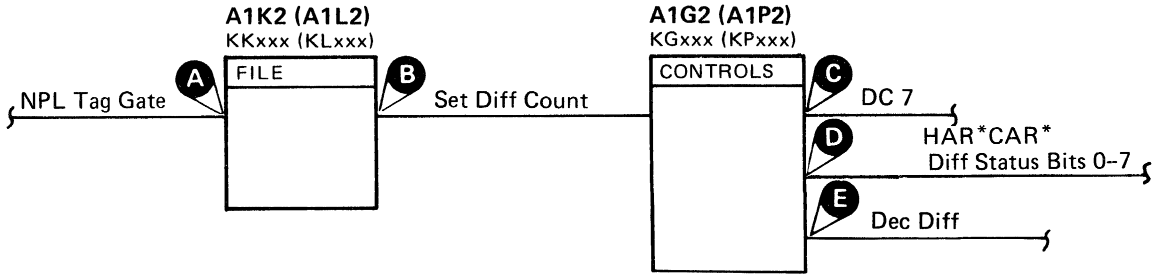
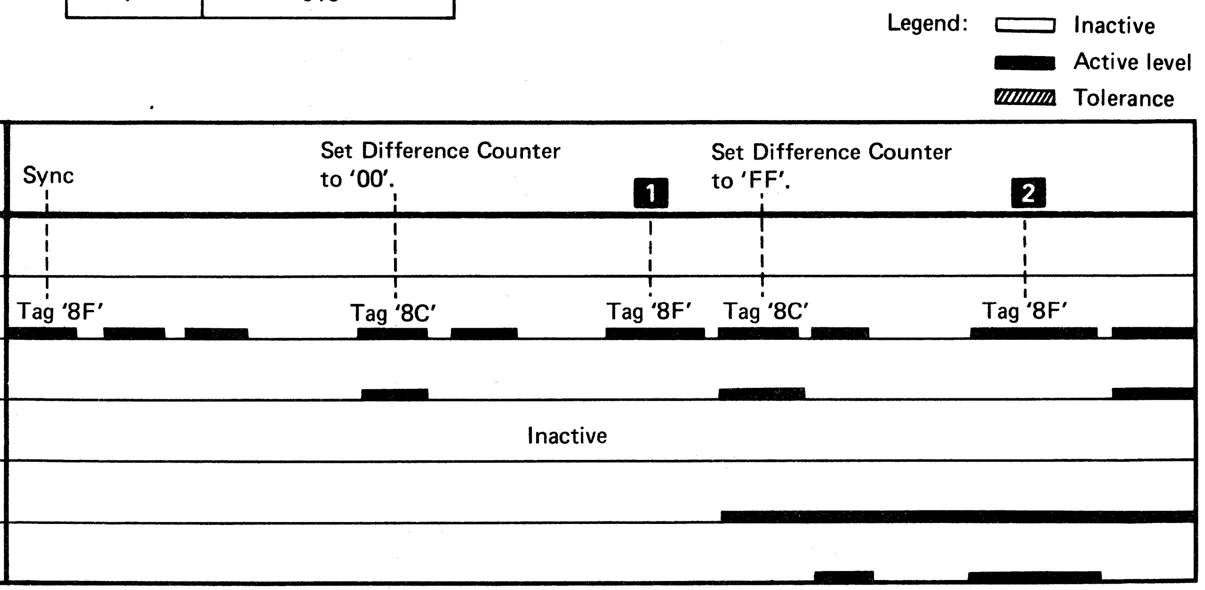


Figure 1. Diff Counter Bits Pin Locations

Bits	+HAR*CAR*Diff Status Ⓓ A1G2(A1P2) KG180(KP180)
0	U03
1	U04
2	S03
3	S05
4	J12
5	G12
6	G10
7	J10

Chart Line No.	Line Name	ALD	Test Point	
1	–Drive Sync Tag	KK170 (KL170)	A1K2 (A1L2) P10	
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓐ
3	+Set Diff Count	KG150 (KP150)	A1G2 (A1P2) B02	Ⓑ
4	–Dec Diff	KG100 (KP100)	A1G2 (A1P2) G02	Ⓔ
5	–DC 7	KG120 (KP120)	A1G2 (A1P2) G09	Ⓒ
6	+HAR*CAR*Diff Status Bits 0–7	KG180 (KP180)	See Figure 1.	Ⓓ



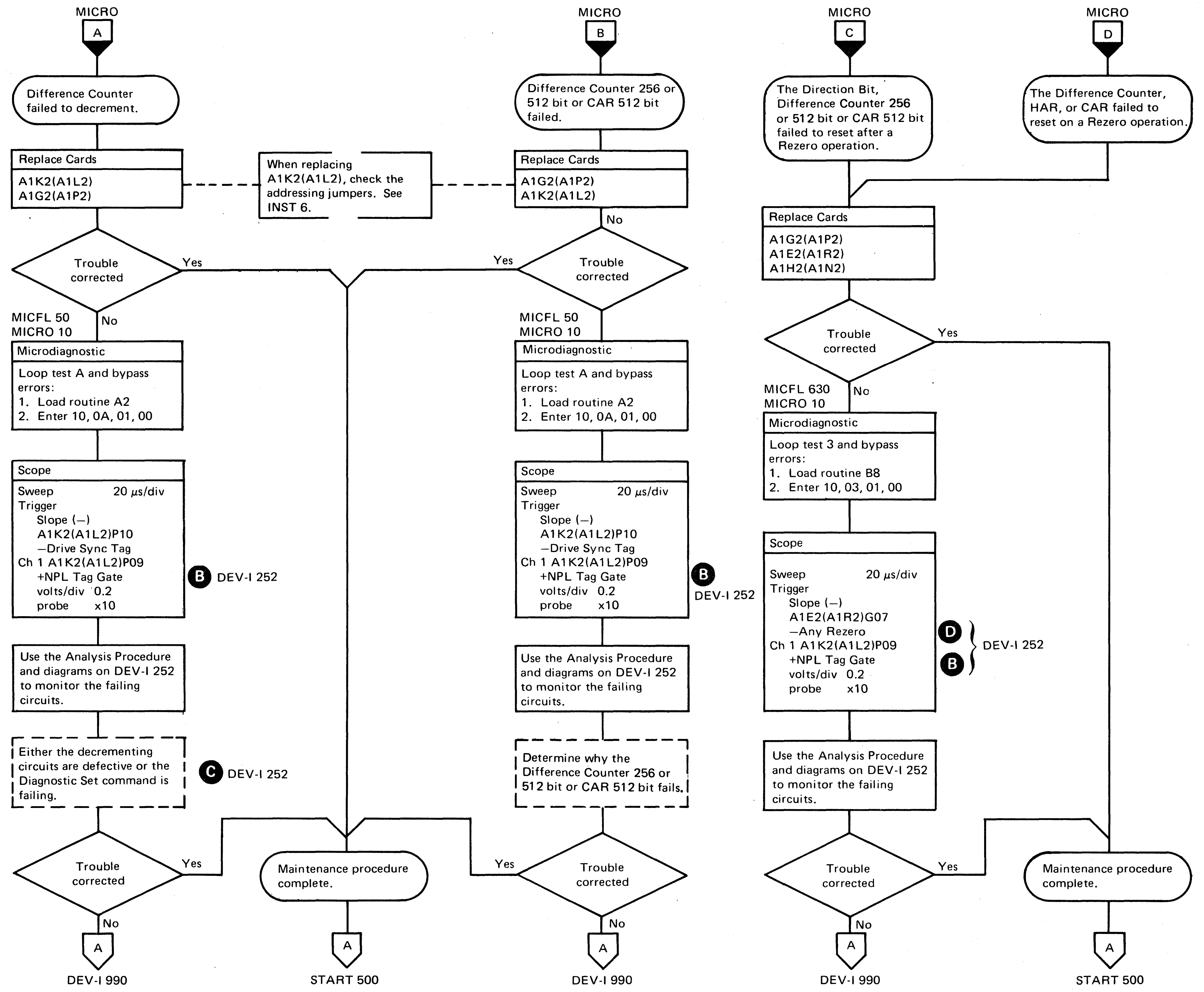
1 Sense Diff Counter for '00'. If any Diff Counter bits are on, an A292 Error Code occurs.

2 Sense Diff Counter for 'FF'. If any Diff Counter bits are off, an A293 Error Code occurs.

3350

CC0242 Seq. 1 of 2	2358369 Part No.	441300 31 Mar 76	441303 30 Jul 76			

DECREMENTING DIFFERENCE COUNTER



DECREMENTING DIFFERENCE COUNTER

Analysis Procedure

DECREMENT DIFFERENCE COUNTER (TAG '8A' BUS OUT '05')

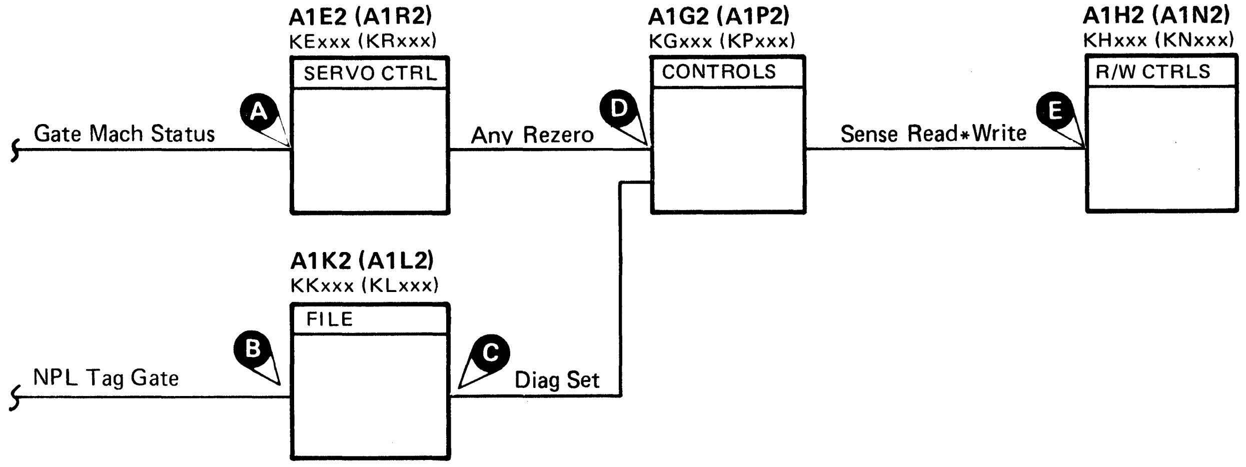
The Difference Counter decrements during a Seek operation with each track crossing pulse and Allow Diff active. A Diagnostic Set command and MST Bus Bit 7 on cause the Difference Counter to decrement by 1.

The Difference Counter resets when Any Rezero Ⓓ is active.

Gate Mach Status Ⓐ gates Access∗Check Status Bits to the Device Bus In.

Sense Read∗Write Ⓔ gates Rd∗Wr Status Bits to the Device Bus In.

See OPER 92 for additional theory.



1 Set Difference Counter 256 and 512 bits to ones.
2 Set Difference Counter 256 and 512 bits to zeros.
3 Set Difference Counter 256 and 512 bits to ones.
4 Diagnostic Set decrements Difference Counter.

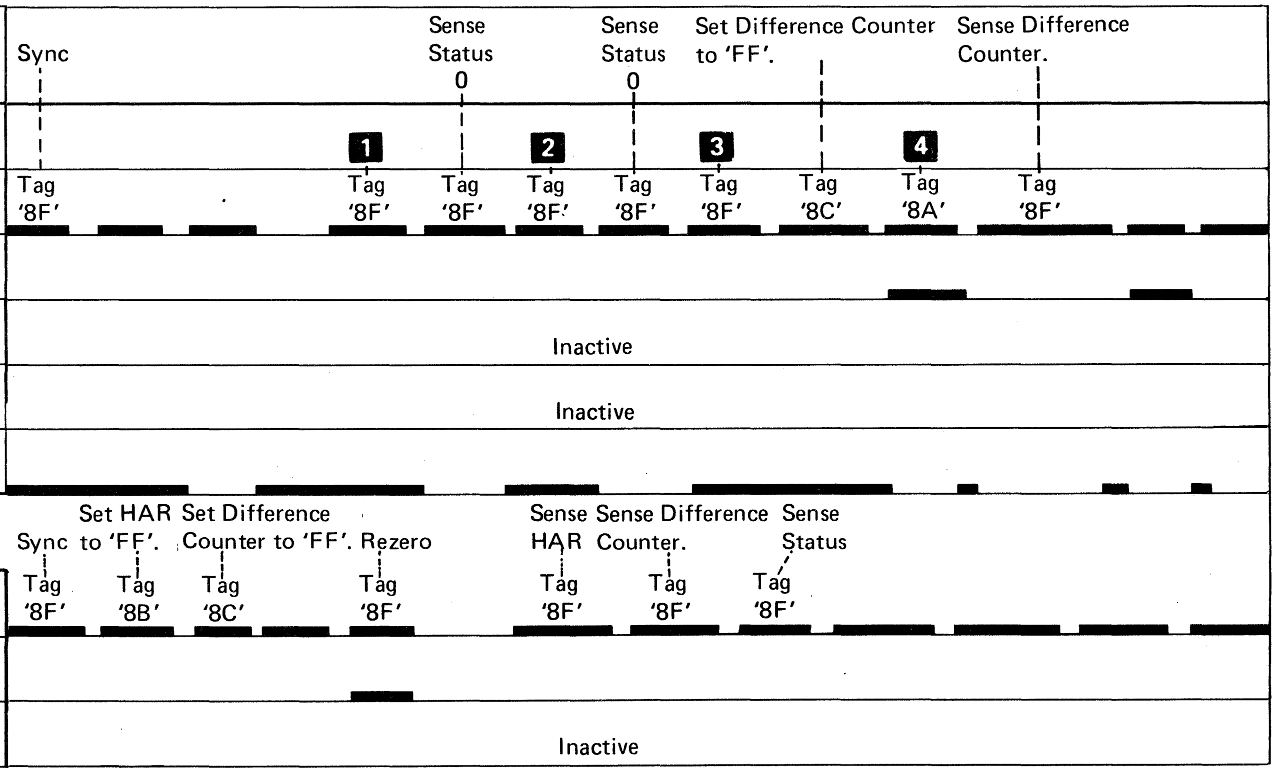
Legend: ▭ Inactive ▬ Active level ▨ Tolerance

A2AX Error Sequencing

Chart Line No.	Line Name	ALD	Test Point	
1	−Drive Sync Tag	KK170 (KL170)	A1K2 (A1L2) P10	
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓑ
3	+Diag Set	KG150 (KP150)	A1G2 (A1P2) B03	Ⓒ
4	−Any Rezero	KG150 (KP150)	A1G2 (A1P2) D04	Ⓓ
5	−Sense Read*Write	KH100 (KN100)	A1H2 (A1N2) M03	Ⓔ
6	+Gate Mach Status	KE160 (KR160)	A1E2 (A1R2) U05	Ⓐ

B83X Error Sequencing

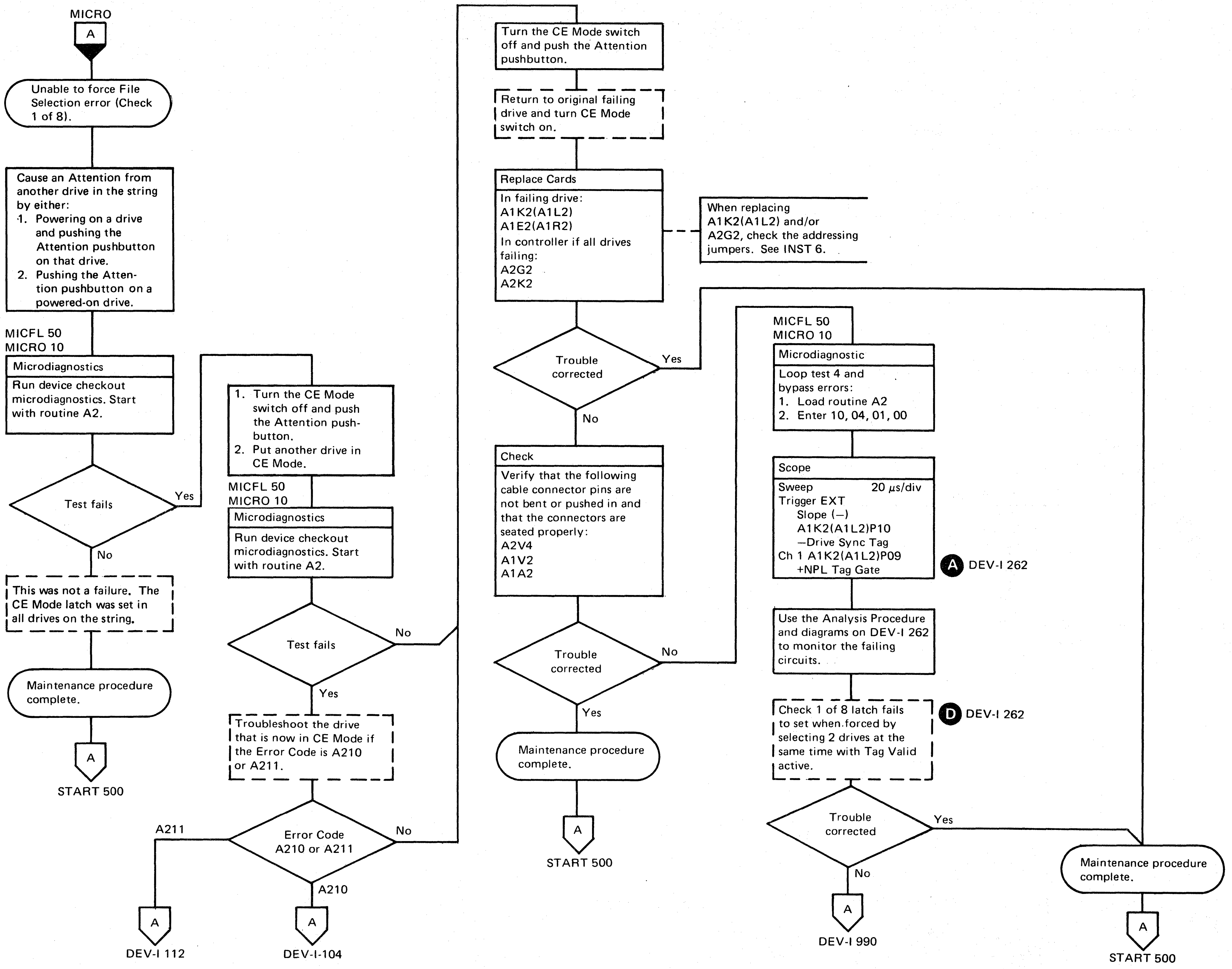
7	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓑ
8	−Any Rezero	KG150 (KP150)	A1G2 (A1P2) D04	Ⓓ
9	+Diag Set	KG150 (KP150)	A1G2 (A1P2) B03	Ⓒ



3350	CC0252 Seq. 1 of 2	2358370 Part No.	441300 31 Mar 76	441303 30 Jul 76			

NO FILE SELECTION ERROR

Routine A2, test 4 forces a File Selection error (Check 1 of 8) by selecting a CE drive and one of the eight customer drives at the same time.



Unable to force File Selection error (Check 1 of 8).

Cause an Attention from another drive in the string by either:
1. Powering on a drive and pushing the Attention pushbutton on that drive.
2. Pushing the Attention pushbutton on a powered-on drive.

MICFL 50
MICRO 10
Microdiagnostics
Run device checkout microdiagnostics. Start with routine A2.

Test fails

This was not a failure. The CE Mode latch was set in all drives on the string.

Maintenance procedure complete.

A START 500

1. Turn the CE Mode switch off and push the Attention pushbutton.
2. Put another drive in CE Mode.

MICFL 50
MICRO 10
Microdiagnostics
Run device checkout microdiagnostics. Start with routine A2.

Test fails

Troubleshoot the drive that is now in CE Mode if the Error Code is A210 or A211.

Error Code A210 or A211

A DEV-I 112

A DEV-I-104

Turn the CE Mode switch off and push the Attention pushbutton.

Return to original failing drive and turn CE Mode switch on.

Replace Cards
In failing drive:
A1K2(A1L2)
A1E2(A1R2)
In controller if all drives failing:
A2G2
A2K2

When replacing A1K2(A1L2) and/or A2G2, check the addressing jumpers. See INST 6.

Trouble corrected

Check
Verify that the following cable connector pins are not bent or pushed in and that the connectors are seated properly:
A2V4
A1V2
A1A2

Trouble corrected

Maintenance procedure complete.

A START 500

MICFL 50
MICRO 10
Microdiagnostic
Loop test 4 and bypass errors:
1. Load routine A2
2. Enter 10, 04, 01, 00

Scope
Sweep 20 μs/div
Trigger EXT
Slope (−)
A1K2(A1L2)P10
−Drive Sync Tag
Ch 1 A1K2(A1L2)P09
+NPL Tag Gate

Use the Analysis Procedure and diagrams on DEV-I 262 to monitor the failing circuits.

Check 1 of 8 latch fails to set when forced by selecting 2 drives at the same time with Tag Valid active.

Trouble corrected

A DEV-I 990

Maintenance procedure complete.

A START 500

NO FILE SELECTION ERROR

Analysis Procedure

This test causes two Attention Select Bus bits to be active resulting in a Check 1 of 8.

Check CE Mode Ⓑ line in the failing drive for proper operation.

See MICFL 50 for additional tag description.

See OPER 92 for additional theory.

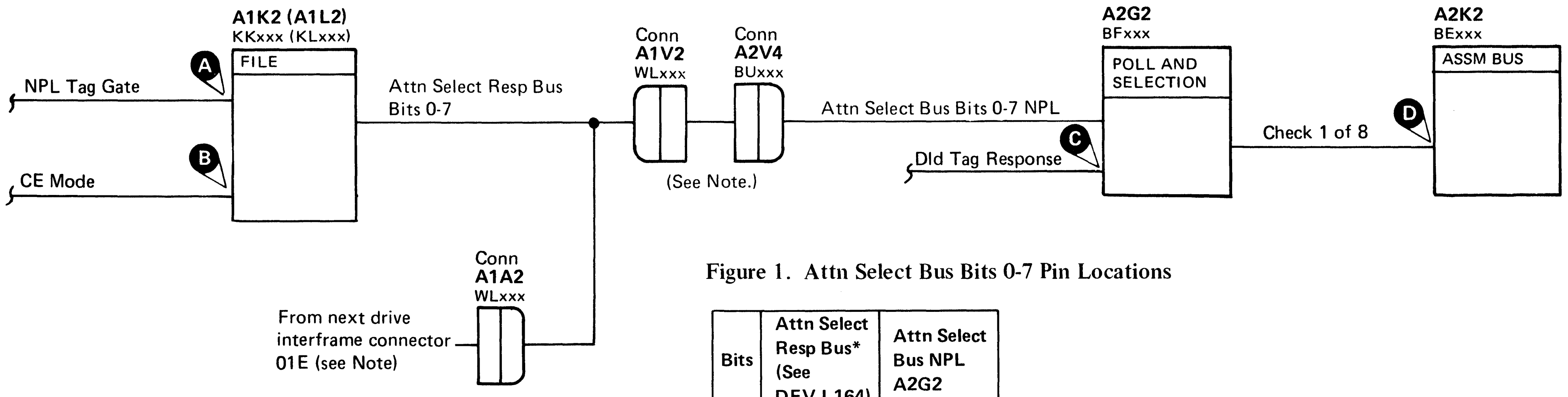


Figure 1. Attn Select Bus Bits 0-7 Pin Locations

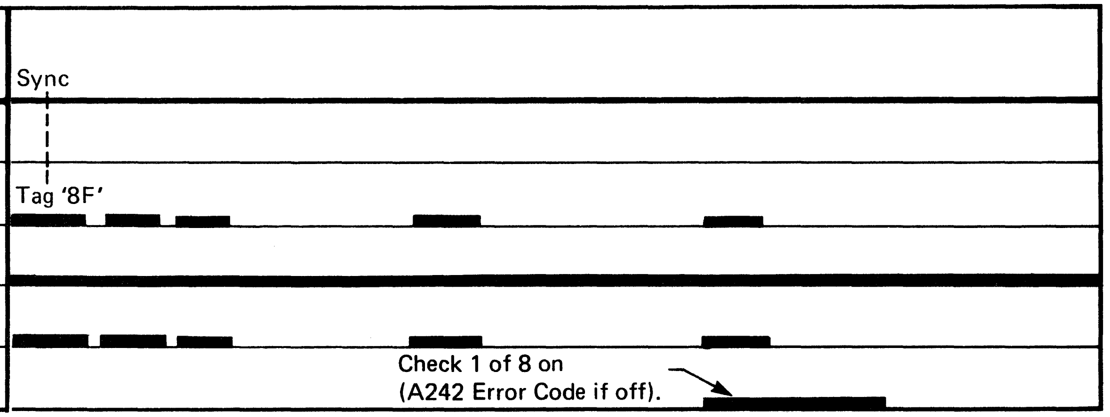
Bits	Attn Select Resp Bus* (See DEV-I 164)	Attn Select Bus NPL A2G2
0	D02	U03
1	D03	U04
2	D05	U06
3	D06	U07
4	D07	S08
5	S08	U10
6	D10	U11
7	D11	S12

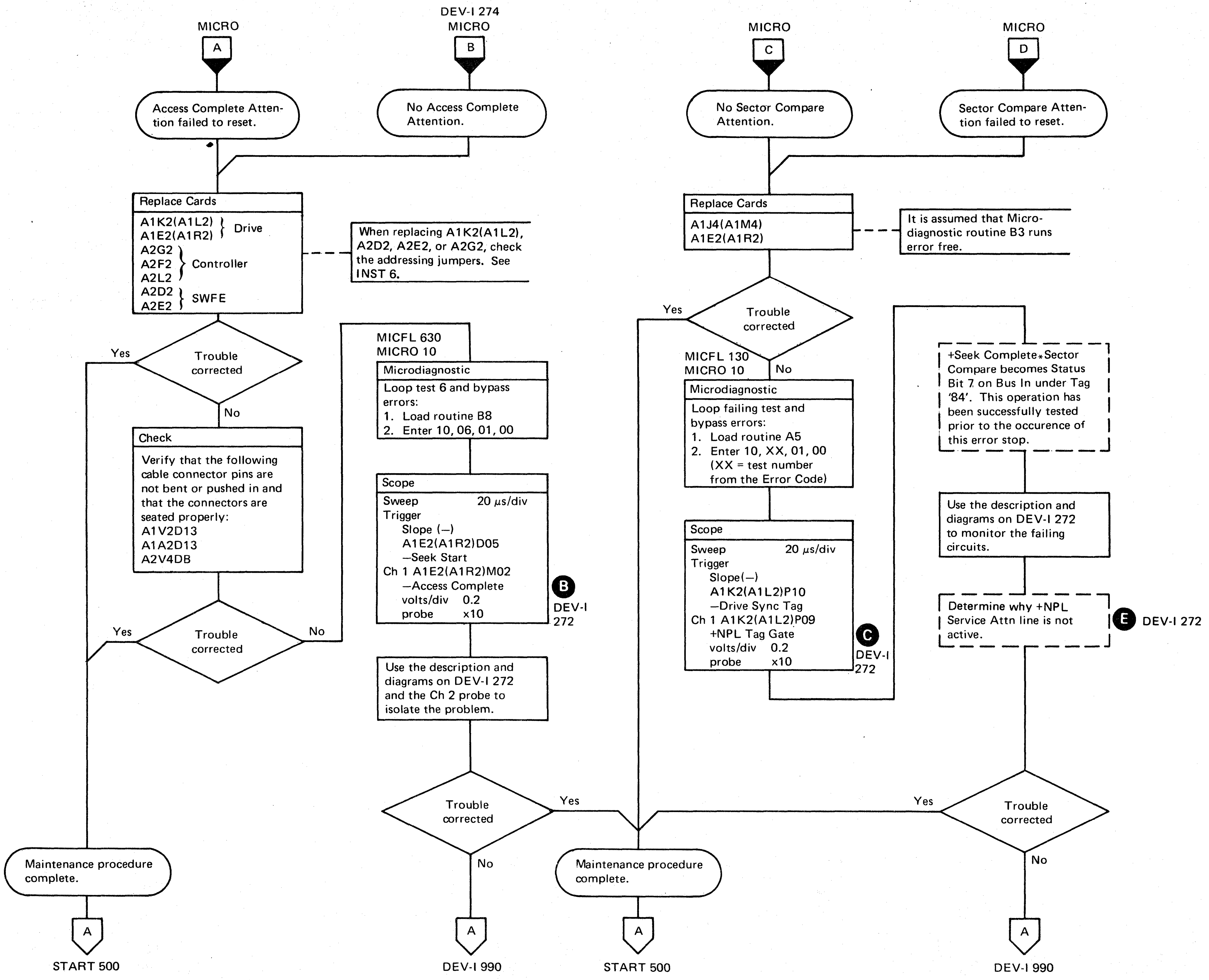
*Connector pins located at A1V2, A1A2, and A2V4.

Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

Legend: ▭ Inactive ▬ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	–Drive Sync Tag	KK170 (KL170)	A1K2 (A1L2) P10	
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓐ
3	–CE Mode	KK180 (KL180)	A1K2 (A1L2) B05	Ⓑ
4	–Dlyd Tag Response	BF200	A2G2 U09	Ⓒ
5	+Check 1 of 8	BF250	A2G2 S13	Ⓓ





CC0262 Seq. 2 of 2	2358371 Part No.	441300 31 Mar 76	441303 30 Jul 76			

ATTENTION ERROR

ATTENTION

A drive activates Attention Ⓐ by placing its unique physical address on the Attn Sel bus. The +NPL Attn Sel Response lines from each drive are wired to the Attention Select Bus (see DEV-I 164).

When storage control polls the controller (Tag '82' with Bus Out bits 0, 1, and 2 equal to the controller address), the Attn Sel Bus is gated to Bus In and good parity is generated.

SERVICE ATTENTION

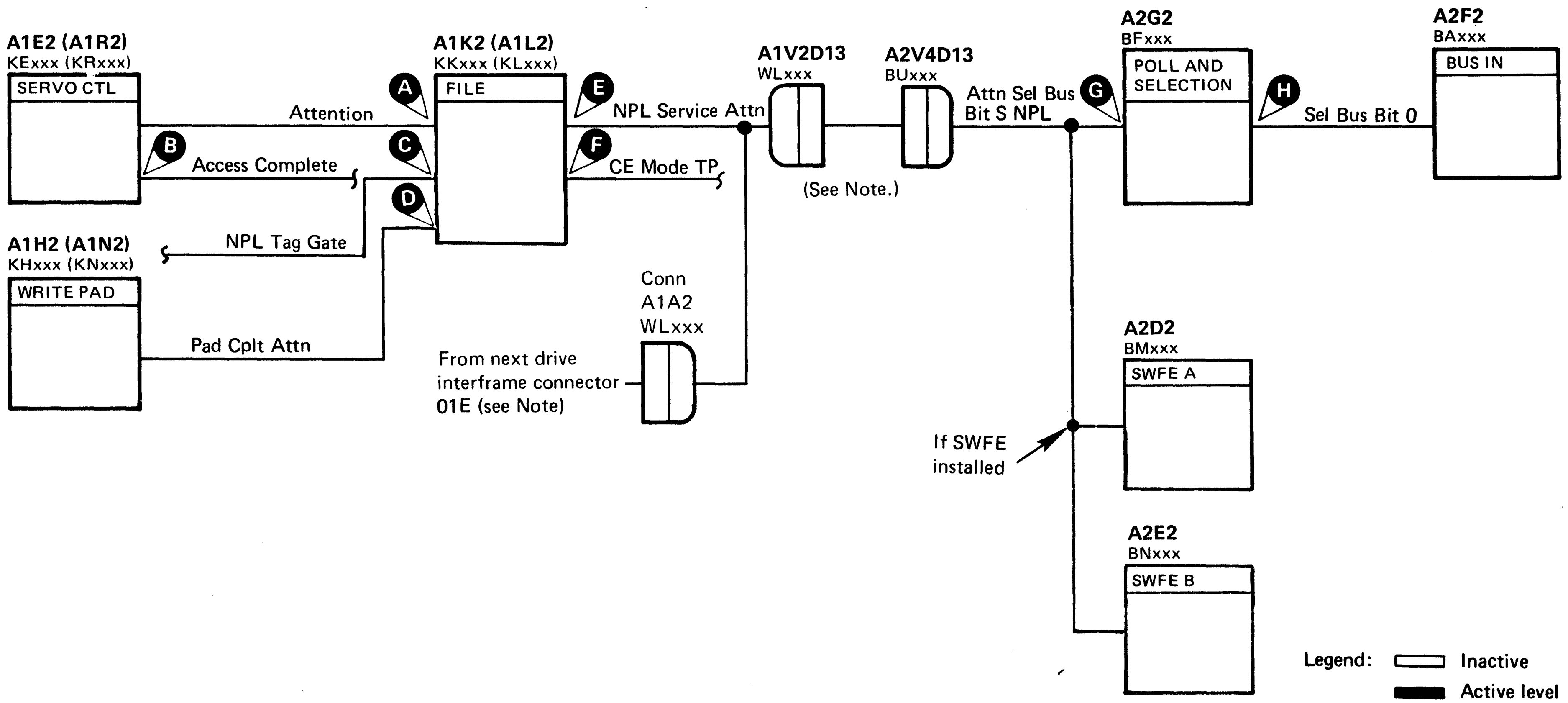
A Service Attention is activated instead of a normal Attention when the drive is in CE Mode. The Service Attention is placed on Attn Sel Bus Bit S NPL Ⓖ.

When storage control polls the controller for a Service Attention (Tag '82' with Bus Out bits 0, 1, and 2 equal to the controller address and bit 5 on), the Attn Sel Bus Bit S is gated to Bus In Bit 0.

Analysis Procedure

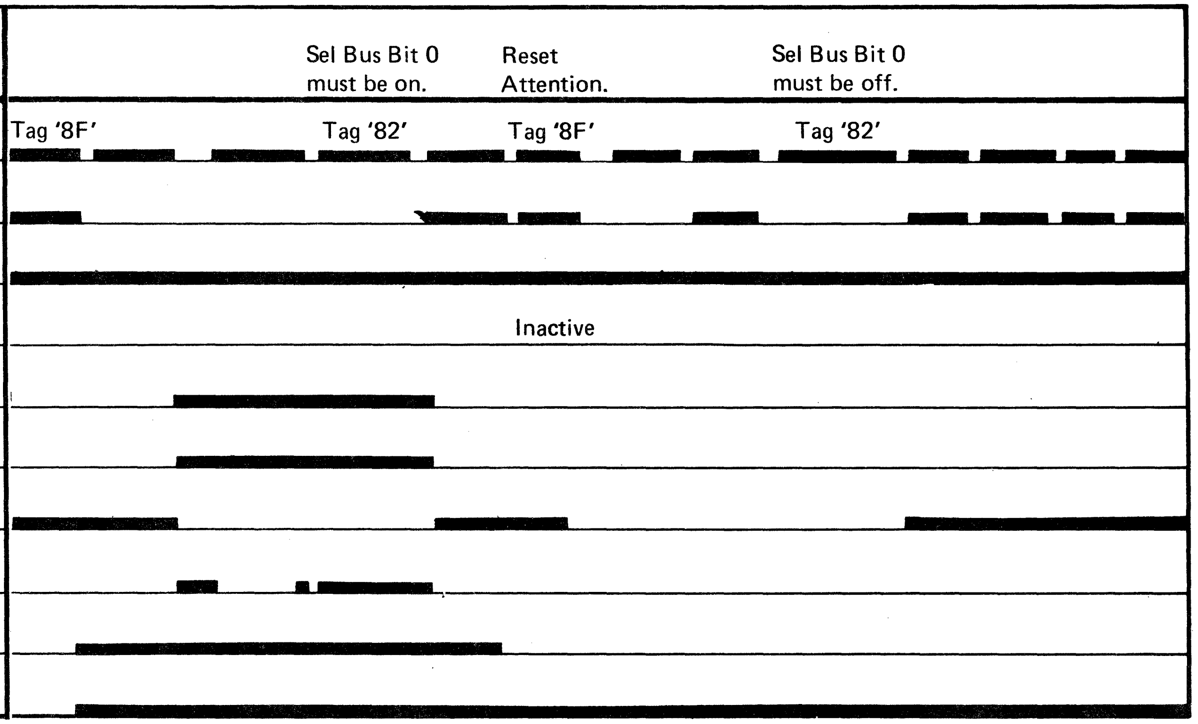
+Attention Ⓐ and –CE Mode TP Ⓕ cause +NPL Service Attn Ⓔ which is gated at Tag '82' time as –Sel Bus Bit 0. The microprogram resets +Attention with a Tag '8F' Bus '04' and issues a Tag '82' to check if –Sel Bus Bit 0 Ⓗ was reset.

See OPER 92 for additional theory.



Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

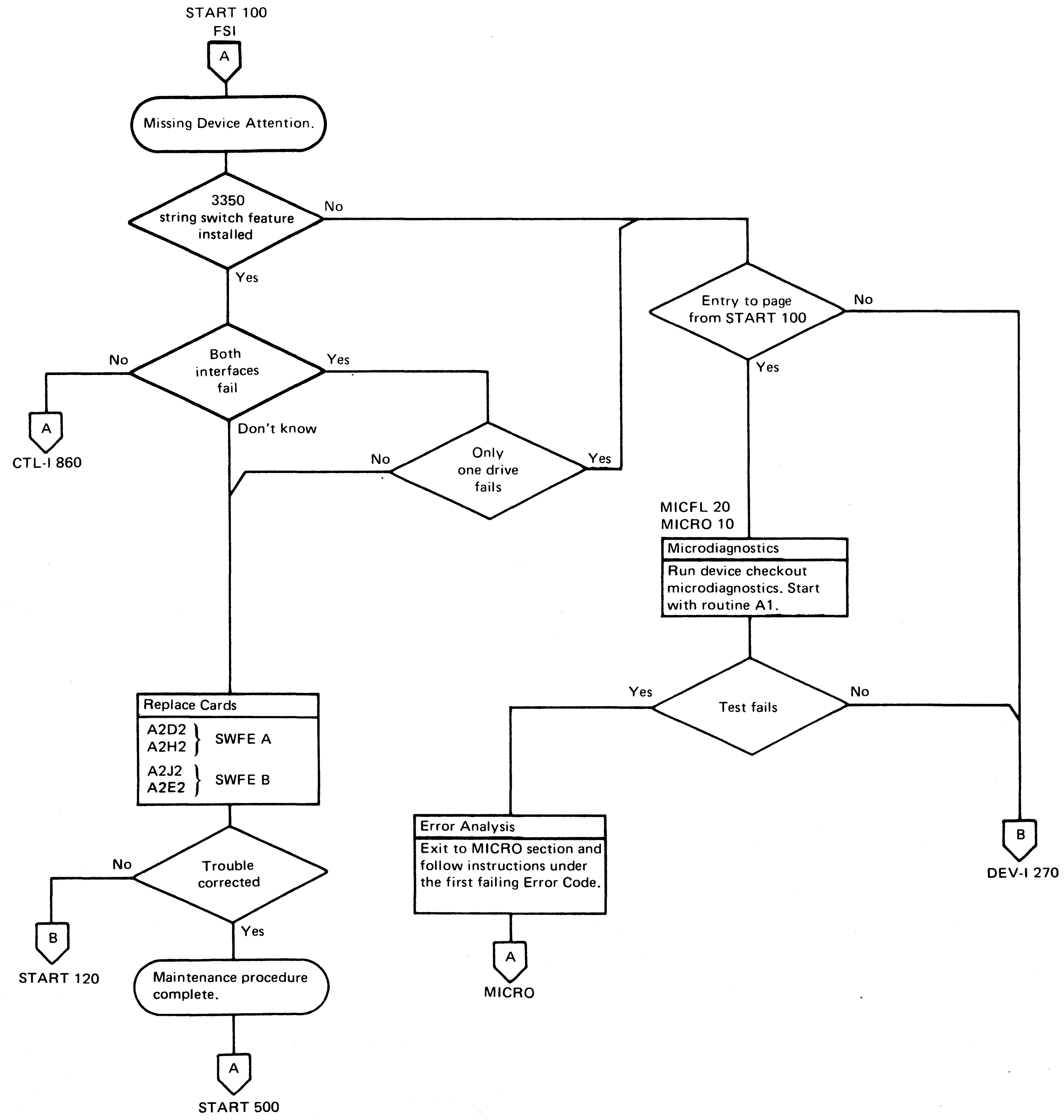
Chart Line No.	Line Name	ALD	Test Point	
1	+Tag Gate NPL	BF130	A2G2 J11	
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09	Ⓒ
3	–CE Mode TP	KK180 (KL180)	A1K2 (A1L2) B05	Ⓕ
4	+Pad Cplt Attn	KK150 (KL150)	A1K2 (A1L2) J07	Ⓓ
5	+NPL Service Attn	KK150 (KL150)	A1K2 (A1L2) B10	Ⓔ
6	+Attn Sel Bus Bit S NPL	BF160	A2G2 S04	Ⓖ
7	–Drive Selecting	BD150	A2L2 P07	
8	–Sel Bus Bit 0	BF190	A2G2 S02	Ⓗ
9	+Attention	KK150 (KL150)	A1K2 (A1L2) G08	Ⓐ
10	–Access Complete	KE140 (KR140)	A1E2 (A1R2) M02	Ⓑ



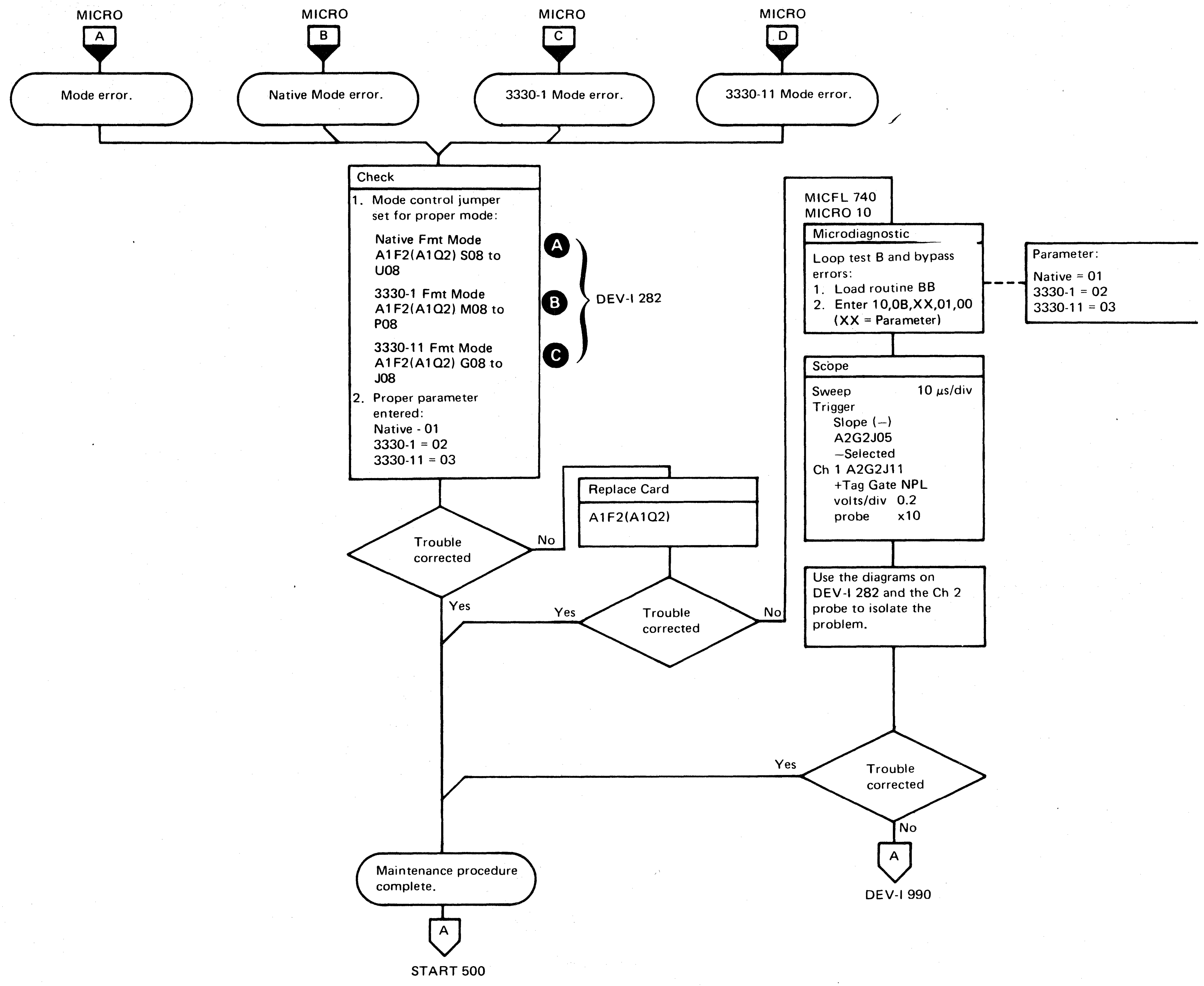
Legend: ▭ Inactive
▬ Active level
▨ Tolerance

3350	CC0272 Seq. 1 of 1	2358372 Part No.	441300 31 Mar 76	441303 30 Jul 76			

DEVICE ATTENTION MISSING



FORMAT (Fmt) MODE ERROR



3350	CC0274 Seq. 2 of 2	2358373 Part No.	441300 31 Mar 76	441306 1 Apr 77				

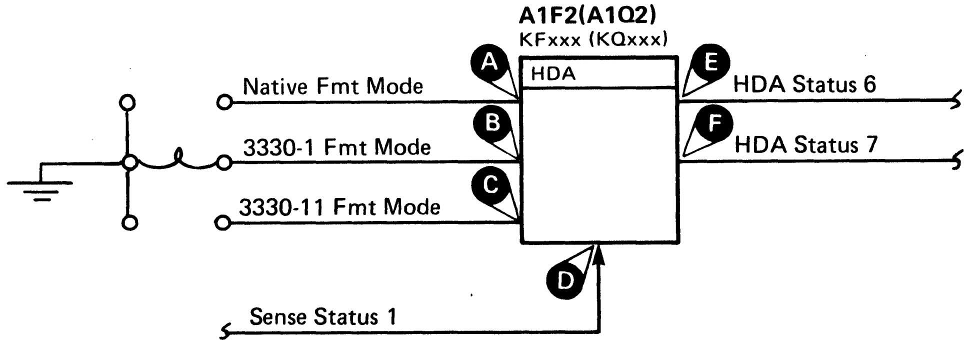
FORMAT (Fmt) MODE ERROR

Circuit Description

Sense Status 1 Ⓓ gates the Format (Fmt) Mode to Device Bus In Bit 6 and 7 if:

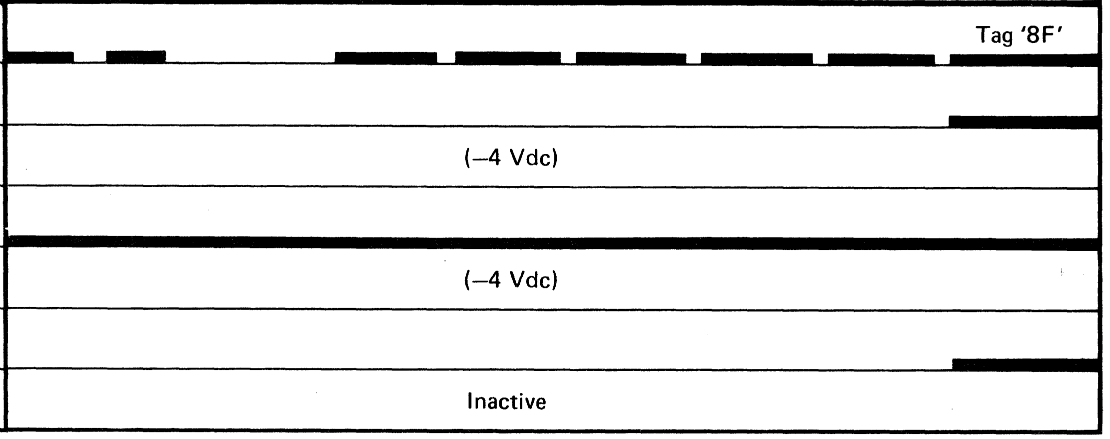
Native Fmt Mode Ⓐ = bit 6 off, bit 7 on.
3330-1 Fmt Mode Ⓑ = bit 6 on, bit 7 off.
3330-11 Fmt Mode Ⓒ = bit 6 on, bit 7 on.

See OPER 92 for additional theory.



Legend:
▭ Inactive
▬ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Sequence Chart Shown With The Drive Wired In 3330-1 Fmt Mode. 1
1	+Tag Gate NPL	BF130	A2G2 J11		Tag '8F'
2	–Sense Status 1	KF130 (KQ130)	A1F2 (A1Q2) D04	Ⓓ	
3	+Native Fmt Mode	KF110 (KQ110)	A1F2 (A1Q2) S08	Ⓐ	(–4 Vdc)
4	+3330-1 Fmt Mode	KF120 (KQ120)	A1F2 (A1Q2) M08	Ⓑ	
5	+3330-11 Fmt Mode	KF120 (KQ120)	A1F2 (A1Q2) G08	Ⓒ	(–4 Vdc)
6	+HDA Status 7	KF240 (KQ240)	A1F2 (A1Q2) J11	Ⓕ	
7	+HDA Status 6	KF240 (KQ240)	A1F2 (A1Q2) J03	Ⓔ	Inactive



1 Sense Status 1. Error occurs if HDA Status Bit 6 and 7 do not agree with Format Mode at this time.

CC0282 Seq. 1 of 1	2358374 Part No.	441300 31 Mar 76	441303 30 Jul 76			

BUS OUT PARITY ERROR

Analysis Procedure

FAULT SYMPTOM CODE 1002

Suspect that a bit is always active or missing on Device Outbus 0-7,P NPL Ⓔ . Different microdiagnostic tests check the Bus Out bits for correct operation. See Figure 1 for details.

1. Use Figure 1 to select the Error Code associated with the bit failure.
2. Loop the test associated with the failing bit using Figure 1:
   - Load routine A2
   - Enter 10, xx, 01, 00

   (xx = Test number to be loaded.)
3. Use Figure 2 for Outbus Bits pin locations and Figure 1 for Page Entry to section containing the scoping procedure and diagrams.

FAULT SYMPTOM CODE 9003

Suspect that one of the lines listed in Figure 3 causes erroneous bits to be on the Device Outbus Bits 0-7,P NPL Ⓔ.

1. Loop test 5 and bypass errors:
   - Load routine A2
   - Enter 10, 05, 01, 00
2. SCOPE SETUP
   Sweep 20 μs/div
   Trigger
   Slope(−)
   A2L2J11
   −MST RAS TP
   Ch 1 A1K2(A1L2)P09
   +NPL Tag Gate
   volts/div 0.2
   probe x10
3. Use Figure 3 and the Ch 2 probe to isolate the problem.

See OPER 92 for additional theory.

Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

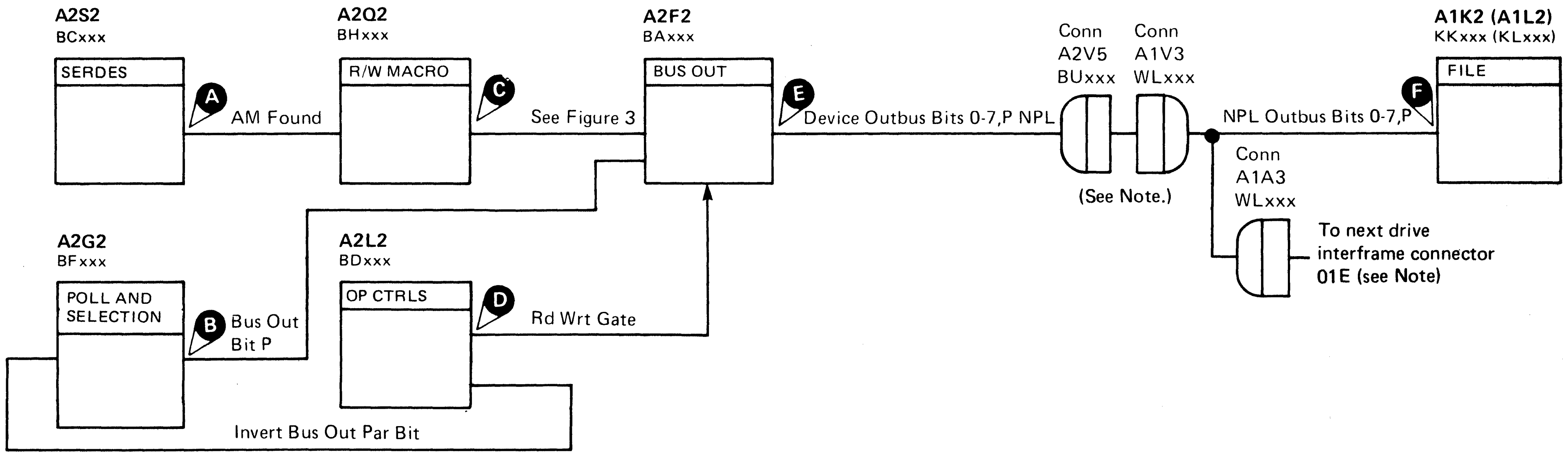


Figure 1. Outbus Bits

Error Code	Outbus Bits		Page Entry
	Always Active	Missing	
A210	4	3	DEV-I 104, A
A216	0, 2, 5, 6, 7	1, P	DEV-I 124, A
A227	1, 3		DEV-I 130, C
A231	P	7	DEV-I 150, B
A232		0, 2, 5, 6, 7	DEV-I 151, A

Figure 2. Outbus Bits Pin Locations

Bits	+Device Outbus NPL A2F2 BA110 Ⓔ	+NPL Outbus A1K2 (A1L2) KK100 (KL100) Ⓕ
0	P10	M07
1	P12	U11
2	U02	U12
3	S03	S11
4	S12	U04
5	U12	S04
6	U05	S02
7	U09	M09
P	M07	U03

Figure 3. Outbus Bits Line Failures

Line Name	Test Points	ALD	Outbus Bit Affected
−Transfer Sector Count	A2F2 P03	BA140	0
−Write Gate Suppressed	A2F2 P04	BA140	1
−Unsquelch	A2F2 U07	BA140	2
−Read Gate	A2F2 S08	BA140	3
−Addr Mark Gate	A2F2 S02	BA140	4
−AM Found*	A1Q2G13	BH130	4
Bits 5, 6, and 7 should be on with −Rd Wrt Gate.			

*If AM Found is always active, a Bus Out Bit 4 error occurs.

CC0400 Seq. 1 of 2	2358375 Part No.	441300 31 Mar 76	441301 1 Jun 76	441303 30 Jul 76	441306 1 Apr 77	

DRIVE SELECT ERROR

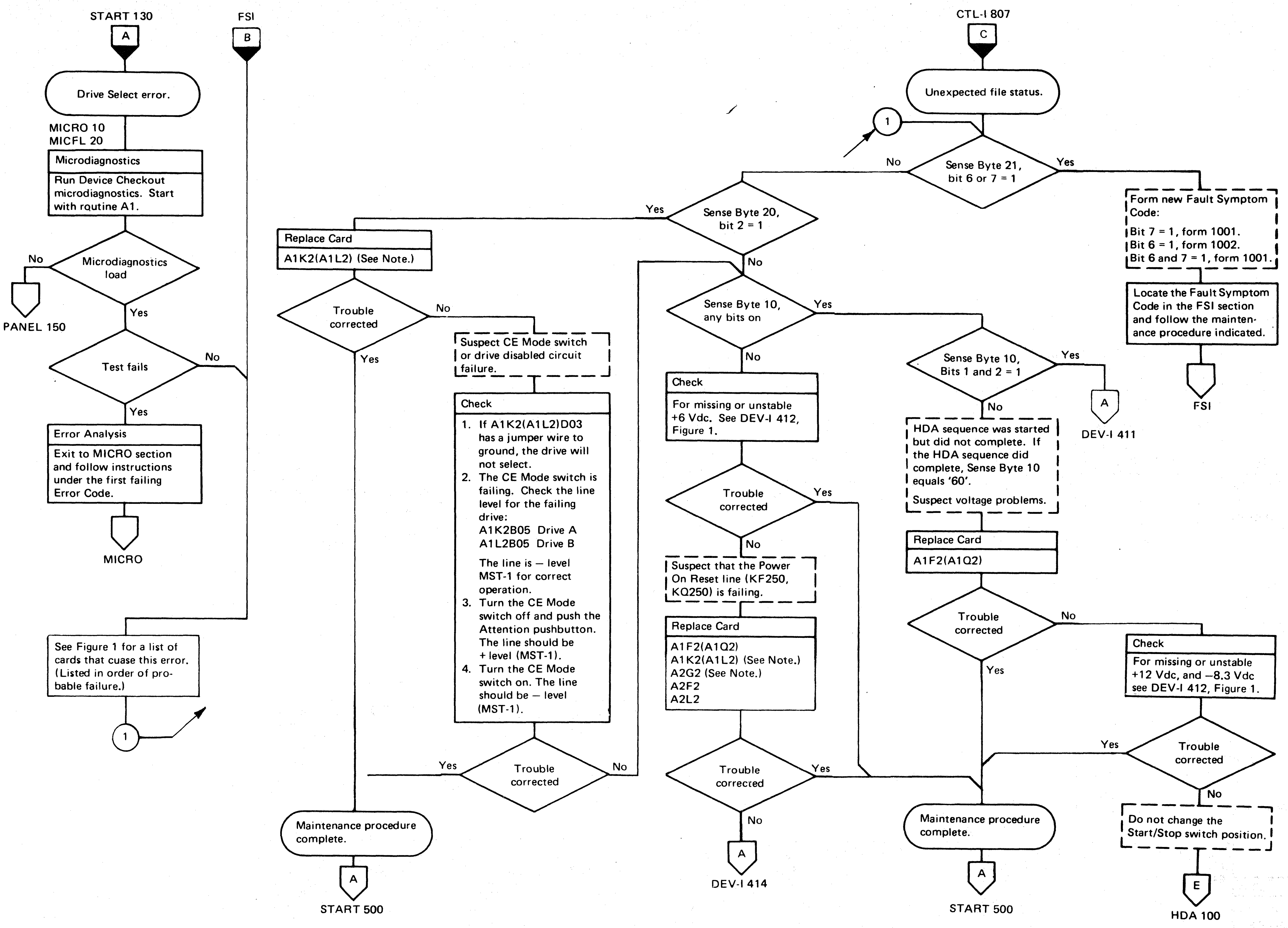
Figure 1. Failing Card List

POSSIBLE CAUSES (Listed in order of probability)	
A1 Board (Drive)	**A2 Board (Controller)**
A1K2 (A1L2)*	A2L2
A1E2 (A1R2)	A2F2
A1D4 (A1S4)**	A2G2*
A1H2 (A1N2)	
A1F2 (A1Q2)	A2K2
A1C2 (A1T2)**	A2D2*
	A2E2* SWFE
A1D2 (A1S2)**	A2H2
	A2J2
	A2M2

* *When replacing A1K2, A1L2, A2G2, A2D2, or A2E2, check the addressing jumpers. See INST 6.*

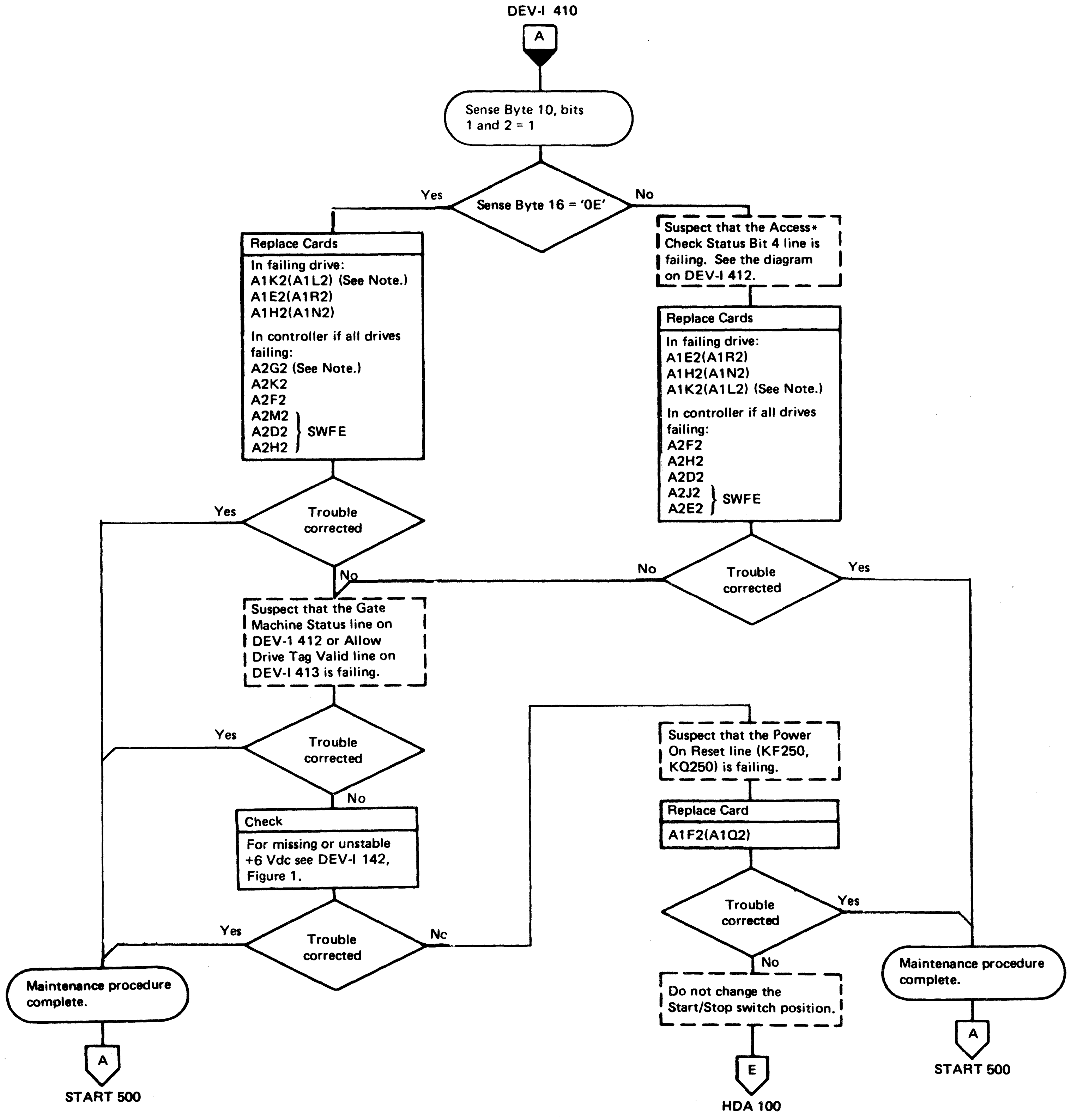
** *When replacing A1C2((A1T2), A1C4 (A1R4), A1D2 (A1S2), A1D4 (A1S4), or Pwr Amp P532 (P542), the servo velocity gain must be adjusted. See ACC 800, Entry B for the procedure.*

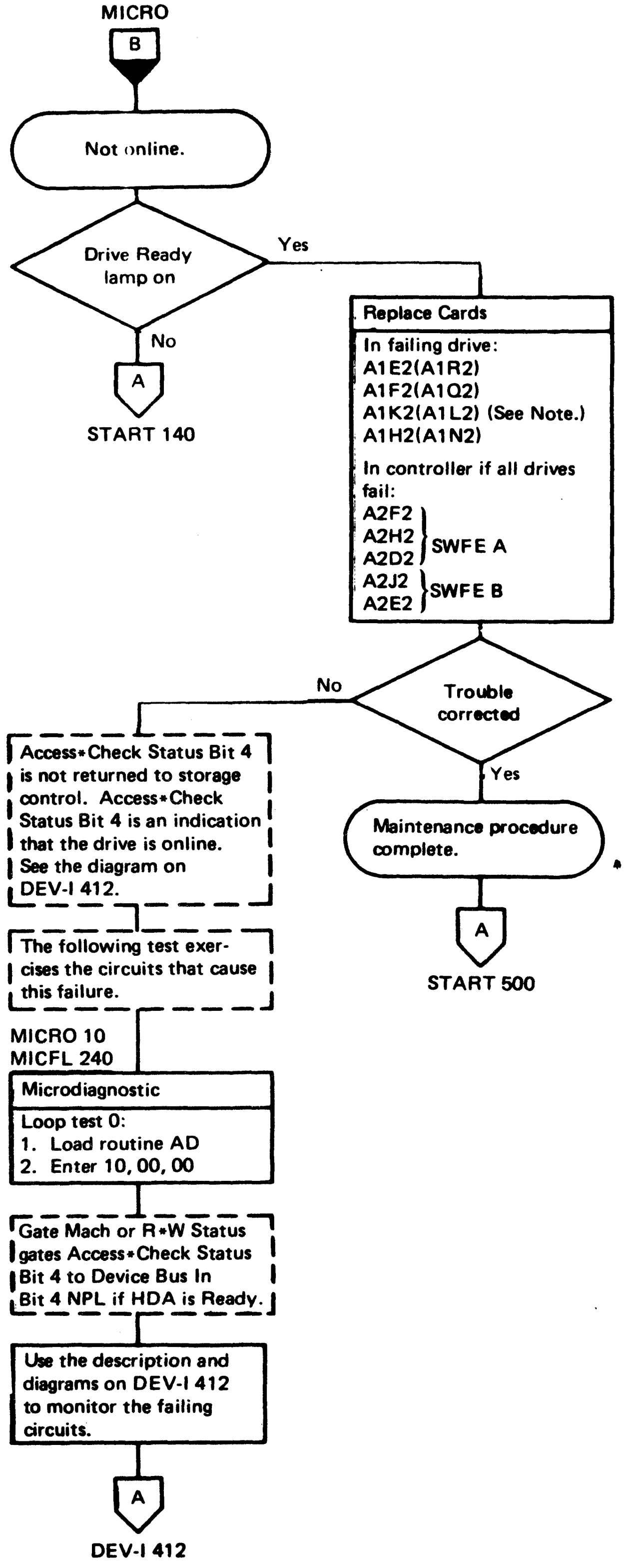
Note: *When replacing A1K2(A1L2) and/or A2G2, check the addressing jumpers. See INST 6.*



F
L

DRIVE SELECT ERROR





Note: *When replacing A1K2(A1L2) and/or A2G2, check the addressing jumpers. See INST 60.*

DRIVE SELECT ERROR

FSI
A

ACCESS*CHECK STATUS BIT 4

Circuit Description

If Sense Byte 10 = '60', the HDA sequence is complete and a drive is selected.

The drive should return Sense Byte 16 = '0E' indicating access is ready and Sense Byte 9 should have bit 4 on. If bit 4 is not on in Sense Byte 9 and 16, bit 4 may be failing.

STRING SWITCH FEATURE (SWFE)

If the string switch feature is installed, Contr Bus In Bit 4 A NPL Ⓙ is gated to storage control by Bus In Assm Bit 4 A Ⓕ and Contr Bus In Bit 4 B NPL Ⓚ by Bus In Assm Bit 4 B Ⓖ

Analysis Procedure

1. See Figure 2 for failing lines that cause this error.
2. Loop the routine and test as indicated by the Error Code to exercise the failing line.
3. Exit to the indicated Page Entry and use the description and diagrams on this page to isolate the problem.

Figure 1. Power Voltage Pin Locations

Voltage	Tolerance	Ripple	Pin Location
A1 Board			
+12 Vdc	+12.0 to 14.4 Vdc	0.1 V p-p	A1C2 (A1T2) D05
+6 Vdc	+5.76 to 6.24 Vdc	0.08 V p-p	A1F2 (A1Q2) B11
+6 Vdc	+5.76 to 6.24 Vdc	0.08 V p-p	A1H2 (A1N2) B11
–8.3 Vdc			A1C2 (A1T2) B02
A2 Board			
+6 Vdc	+5.76 to 6.24 Vdc	0.08 V p-p	A2F2 B11

See PWR 290 for voltage adjustments.

Figure 2. Line Failure Error Codes

Line Name	ALD	Pin	Error Code (line is faulty)	Test Point	Page Entry
Access*Check Status Bit 4	KE160 (KR160)	A1E2 (A1R2) U04	AD02	Ⓓ	
Device Bus In Bit 4 NPL	KH200 (KN200)	A1H2 (A1N2) D07	A235	Ⓔ	DEV-I 160, A
Contr Bus in Bit 4 NPL	BA150	A2F2 J02	A150	Ⓗ	CTL-I 500, C

See OPER 92 for additional theory.

FSI
B

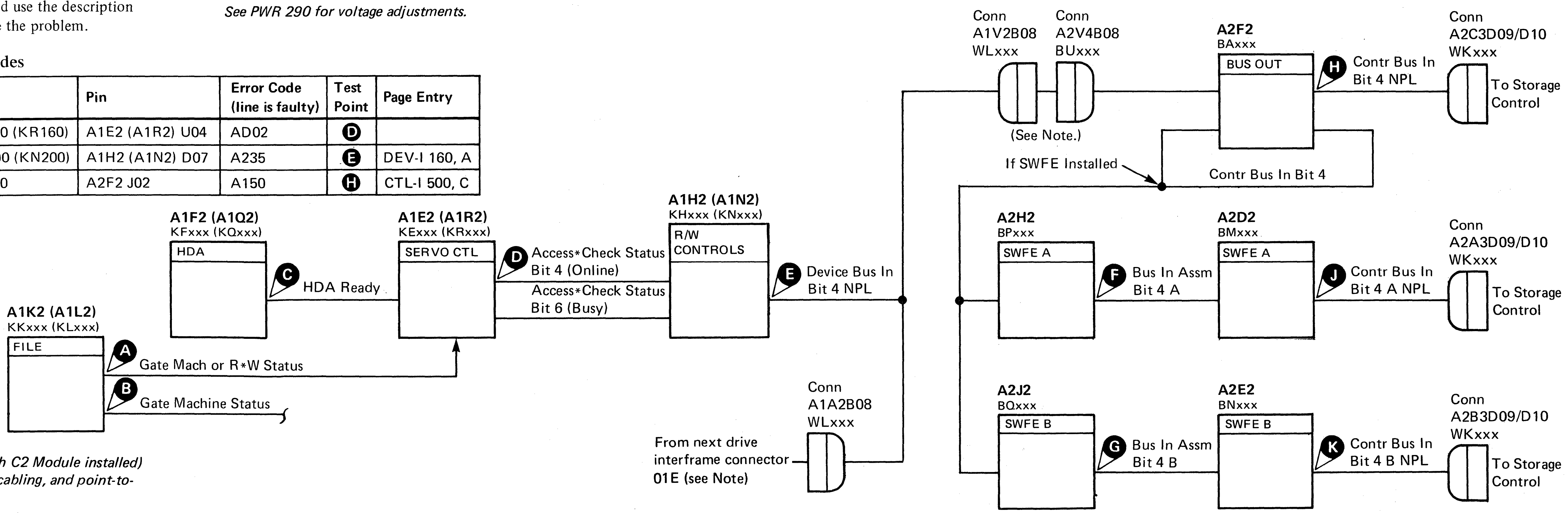
GATE MACHINE STATUS

Analysis Procedure

1. See Figure 3 for failing lines that cause this error.
2. Loop routine BB test 2 to exercise the failing line.
3. Exit to the indicated Page Entry and use the description and diagrams on this page to isolate the problem.

Figure 3. Line Failure Error Codes

Line Name	ALD	Pin	Error Code (line is faulty)	Test Point	Page Entry
+HDA Ready	KF220 (KQ220)	A1F2 (A1Q2) B10	B827	Ⓒ	ACC 210, C
+Gate Mach Status	KK140 (KL140)	A1K2 (A1L2) S12	B827	Ⓑ	ACC 210, C
+Gate Mach or R*W Status	KK140 (KL140)	A1K2 (A1L2) S13	B822	Ⓐ	ACC 101, A



Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

FSI
C

ALLOW DRIVE TAG VALID

Circuit Description

This Fault Symptom Code can be caused by a missing Tag Valid NPL Ⓑ.

Allow Drive Tag Valid Ⓐ activates Coerce Tag Valid Ⓒ. Coerce Tag Valid activates Tag Valid NPL.

STRING SWITCH FEATURE (SWFE)

If the string switch feature is installed, Tag Valid A NPL Ⓕ and Tag Valid B NPL Ⓖ are activated by Coerce Tag Valid if no Tag 06 Error A Ⓓ or B Ⓔ exist.

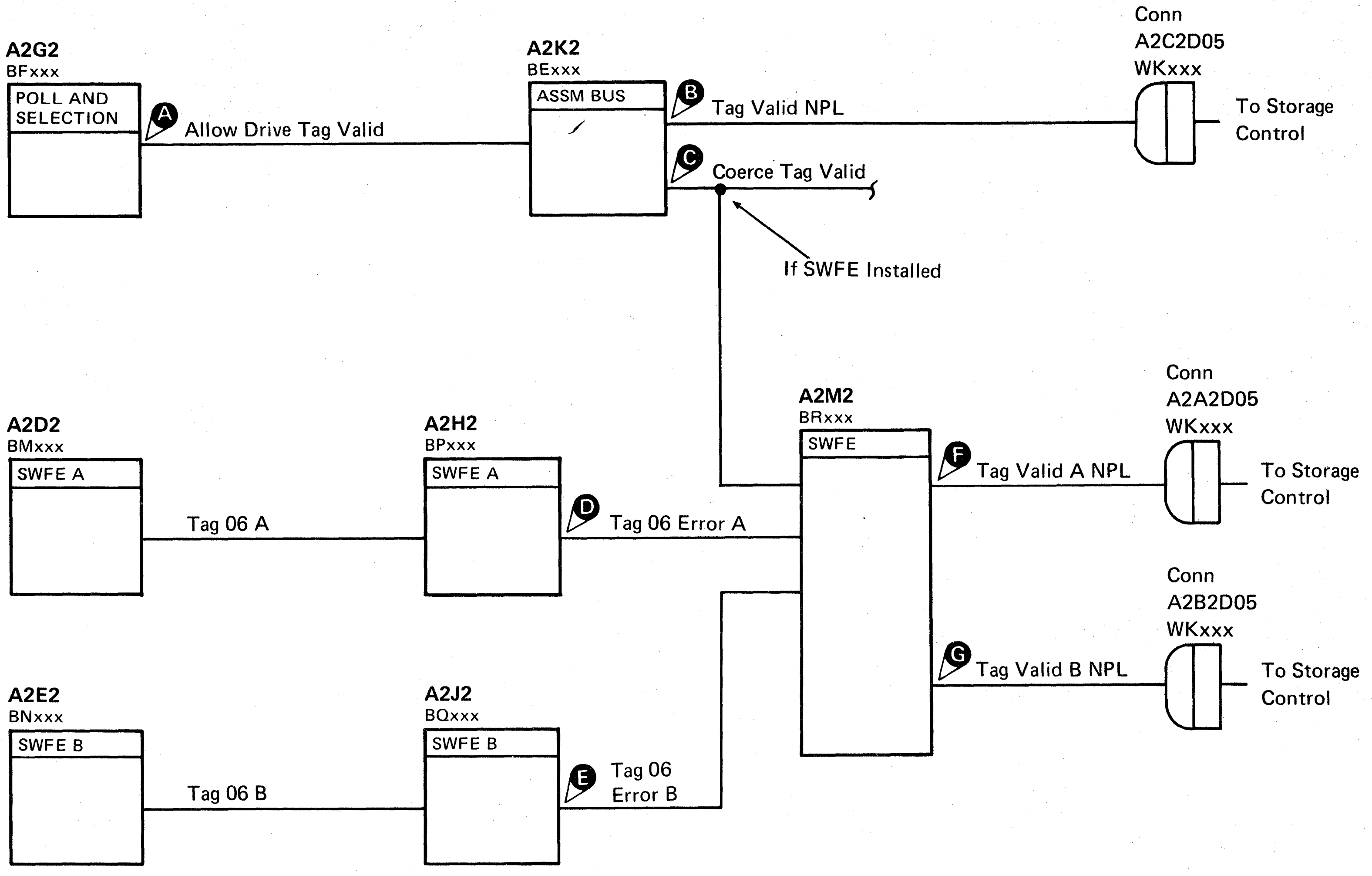
Analysis Procedure

1. See Figure 1 for failing lines that cause this error.
2. Loop routine A1, test 4 to exercise the failing line.
3. Exit to the indicated Page Entry and use the description and diagrams on this page to isolate the problem.

Figure 1. Line Failure Error Codes

Line Name	ALD	Pin	Error Code (line is faulty)	Test Point	Page Entry
–Allow Drive Tag Valid	BF110	A2G2 G11	A140	Ⓐ	CTL-I 430, A
+Tag 06 A(B)	BM150 (BN150)	A2D2 (A2E2) G13	A140		CTL-I 430, A
+Tag 06 Error A(B)	BP190 (BQ190)	A2H2 (A2J2) G07	A140		CTL-I 430, A

See OPER 92 for additional theory.



DRIVE SELECT ERROR

FSI

A

DRIVE FAILS TO SELECT

Circuit Description

A drive selects under the following conditions:

- +Select Gate Ⓚ + level (MST-1). The drive decodes Device Tag Bus Ⓖ as Select Gate if bits 0, 1, and 2 = 000 (Tag '83') and Device Tag Gate NPL Ⓕ is + level (NPL). Device Tag Gate NPL is active if Selected Tag Gate Ⓒ and Device Select Ⓑ are active – level (MST-1).
- –MST Outbus Bit 4 is + level (MST-1). If Outbus Bit 4 is active, it prevents a drive selection. If Rd Wrt Latch Ⓓ or Rd Wrt Gate Ⓗ are active – level (MST-1) during a Tag '83' (Select), Device Outbus Bit 4 Ⓙ is active which prevents a drive from selecting.
- +Device Sel Hold NPL Ⓔ is + level (NPL). Device Sel Hold NPL is activated if Drive Selecting Ⓐ is – level (MST-1).
- –MST Outbus Bit 3 is a + level (MST-1).
- –CE Switch is a + level (MST-1). For Normal Selection, the CE switch line must be inactive + level (MST-1).

  In CE Mode, the microprogram issues Outbus Bit 3 which allows the drive with the CE Switch active – level (MST-1) to select through the CE Selection latch.
- Address Jumper Compare line is active (see INST 6 for Address Jumper details).

STRING SWITCH FEATURE (SWFE)

If the string switch feature is installed, suspect that the Device Sel Hold NPL Ⓔ line is failing.

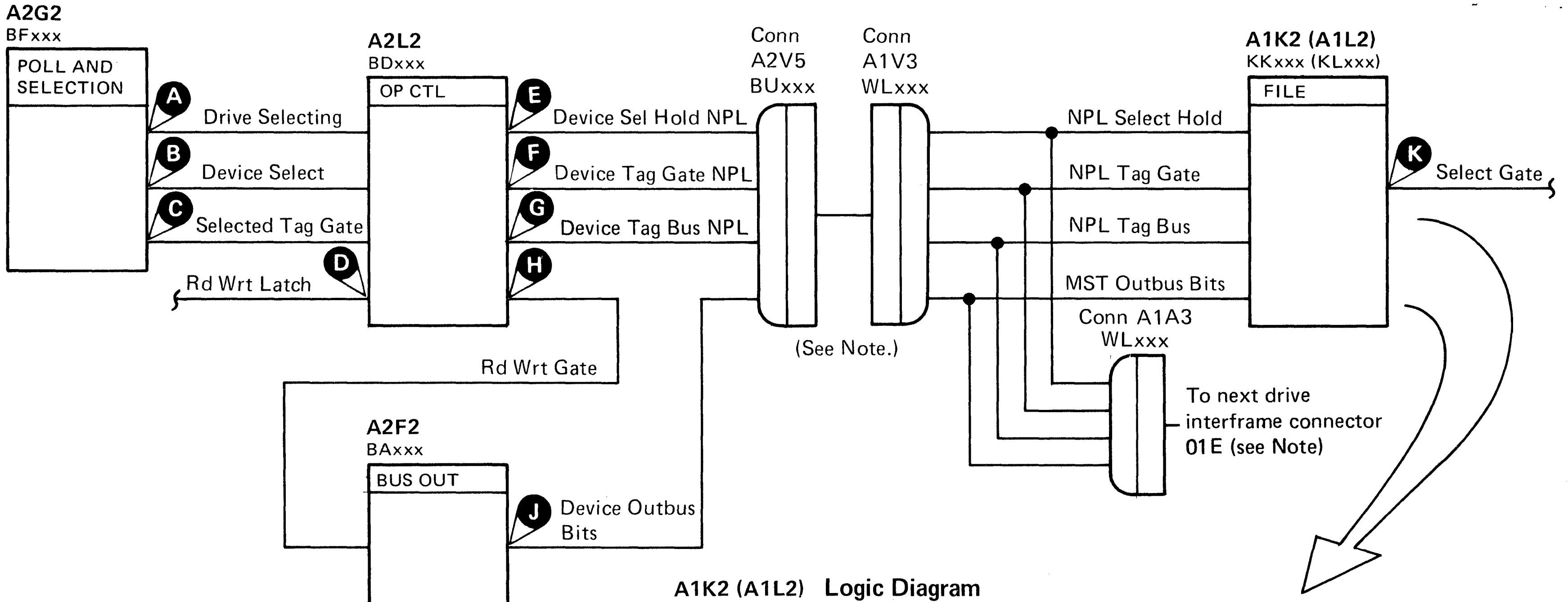
Analysis Procedure

1. See Figure 1 for failing lines that cause this error.
2. Loop routine A2, test 1 to exercise the failing line.
3. Exit to the indicated Page Entry and use the description and diagrams on this page to isolate the problem.

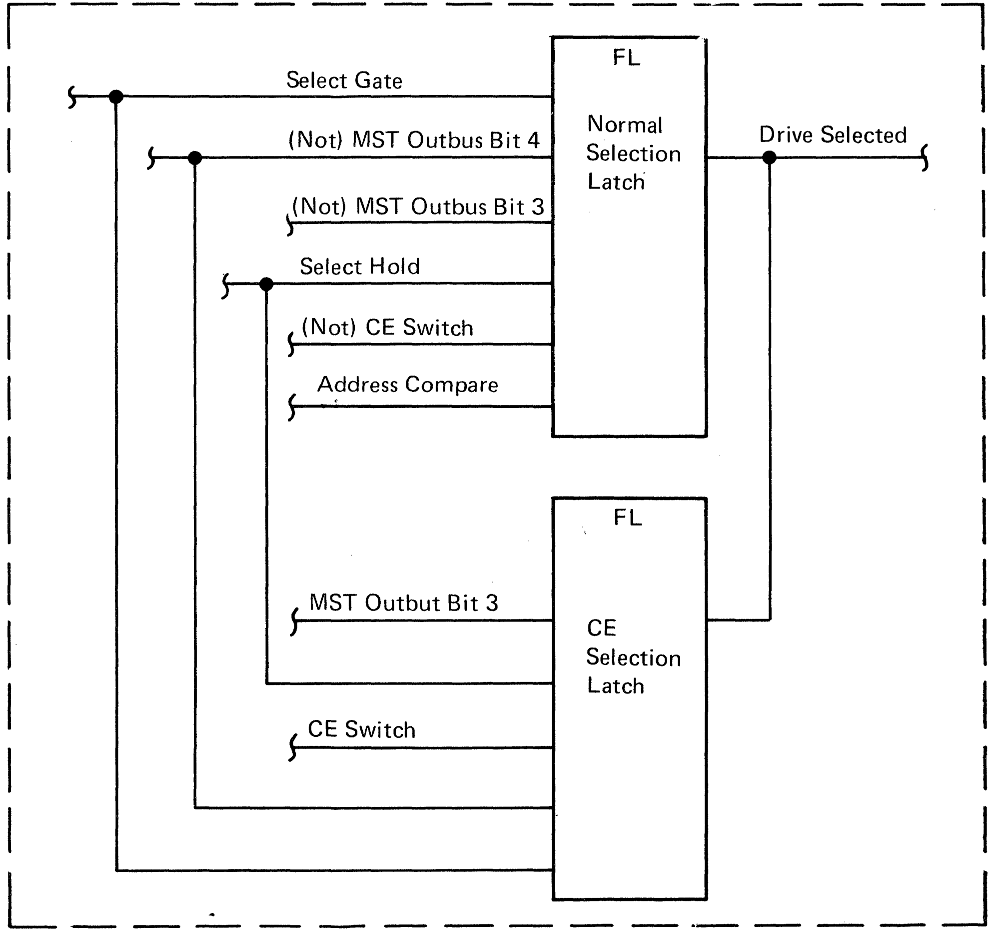
Figure 1. Line Failure Error Codes

Line Name	ALD	Pin	Error Code (line is faulty)	Test Point	Page Entry
–Device Sel Hold NPL	BD230	A2L2 M03	A210	Ⓔ	DEV-I 104, A

See OPER 92 for additional theory.

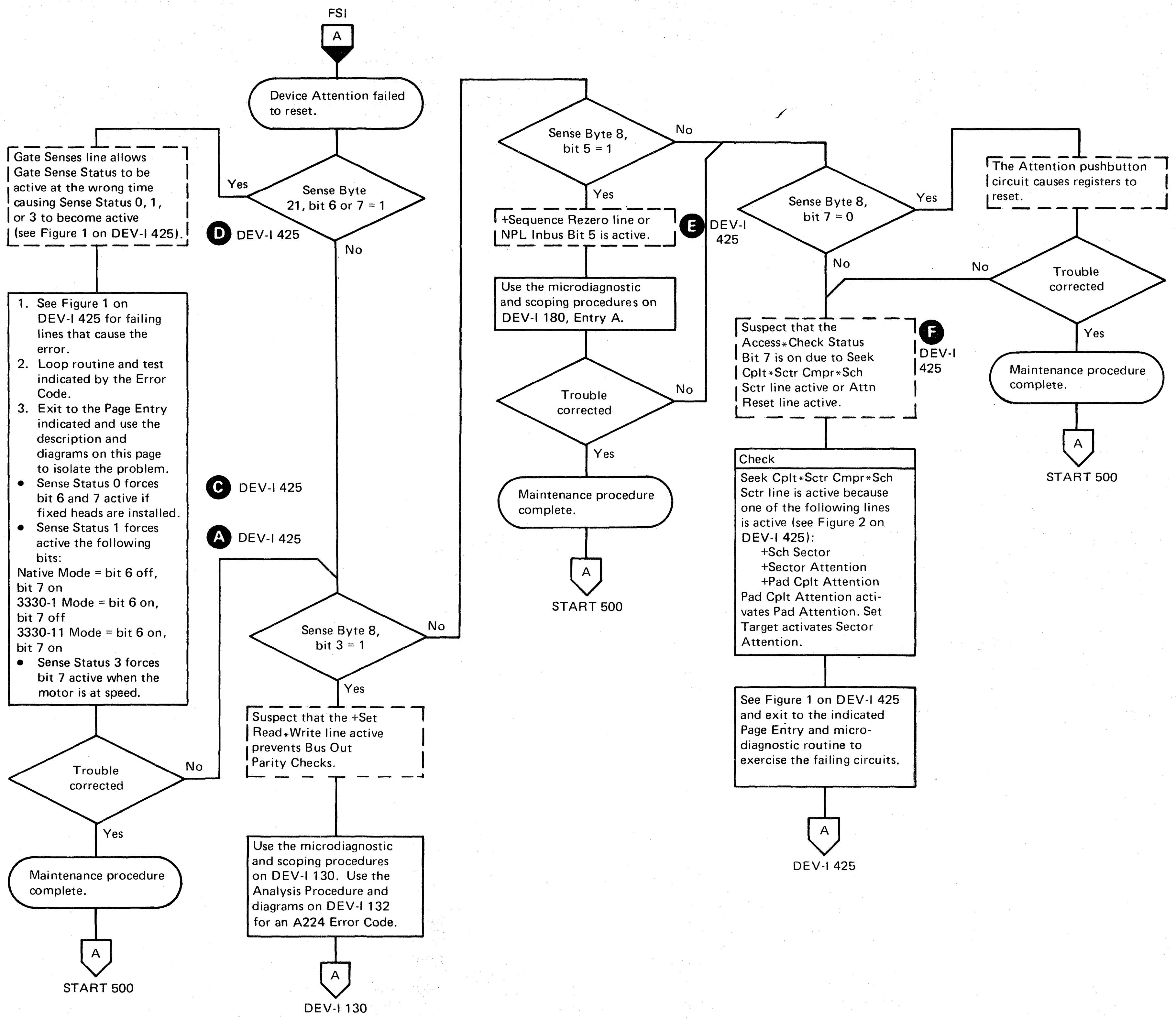


A1K2 (A1L2) Logic Diagram



Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

3350	CC0414 Seq. 1 of 2	2358377 Part No.	441300 31 Mar 76	441303 30 Jul 76



Device Attention failed to reset.

Sense Byte 21, bit 6 or 7 = 1

Gate Senses line allows Gate Sense Status to be active at the wrong time causing Sense Status 0, 1, or 3 to become active (see Figure 1 on DEV-I 425).

1. See Figure 1 on DEV-I 425 for failing lines that cause the error.
2. Loop routine and test indicated by the Error Code.
3. Exit to the Page Entry indicated and use the description and diagrams on this page to isolate the problem.

- Sense Status 0 forces bit 6 and 7 active if fixed heads are installed.
- Sense Status 1 forces active the following bits:

Native Mode = bit 6 off, bit 7 on
3330-1 Mode = bit 6 on, bit 7 off
3330-11 Mode = bit 6 on, bit 7 on

- Sense Status 3 forces bit 7 active when the motor is at speed.

Trouble corrected

Maintenance procedure complete.

Sense Byte 8, bit 3 = 1

Suspect that the +Set Read∗Write line active prevents Bus Out Parity Checks.

Use the microdiagnostic and scoping procedures on DEV-I 130. Use the Analysis Procedure and diagrams on DEV-I 132 for an A224 Error Code.

Sense Byte 8, bit 5 = 1

+Sequence Rezero line or NPL Inbus Bit 5 is active.

Use the microdiagnostic and scoping procedures on DEV-I 180, Entry A.

Trouble corrected

Maintenance procedure complete.

Sense Byte 8, bit 7 = 0

Suspect that the Access∗Check Status Bit 7 is on due to Seek Cplt∗Sctr Cmpr∗Sch Sctr line active or Attn Reset line active.

Check

Seek Cplt∗Sctr Cmpr∗Sch Sctr line is active because one of the following lines is active (see Figure 2 on DEV-I 425):
+Sch Sector
+Sector Attention
+Pad Cplt Attention
Pad Cplt Attention activates Pad Attention. Set Target activates Sector Attention.

See Figure 1 on DEV-I 425 and exit to the indicated Page Entry and micro-diagnostic routine to exercise the failing circuits.

The Attention pushbutton circuit causes registers to reset.

Trouble corrected

Maintenance procedure complete.

CC0414 Seq. 2 of 2	2358377 Part No.	441300 31 Mar 76	441303 30 Jul 76			

ATTENTION FAILED TO RESET

FAULT SYMPTOM CODE 900F

See OPER 92 for theory.

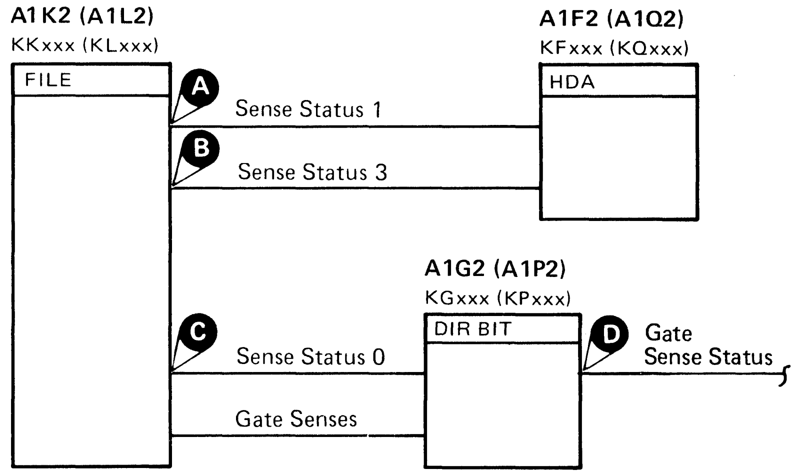


Figure 1. Line Failure Error Codes

Line Name	ALD	Pin	Error Code (Line is Faulty	Page Entry
–Gate Senses	KK170 (KL170)	A1K2 (A1L2) J10	B833	ACC 210, C
–Sense Status	KG190 (KP190)	A1G2 (A1P2) S13	A223	DEV-I 137, B
–Sense Status 0	KK170 (KL170)	A1K2 (A1L2) U10	A223	DEV-I 137, B
–Sense Status 1	KK170 (KL170)	A1K2 (A1L2) U05	A223	DEV-I 137, B
–Sense Status 3	KK170 (KL170)	A1K2 (A1L2) U09	A222	DEV-I 134, B

FAULT SYMPTOM CODE 9005

See OPER 92 for theory.

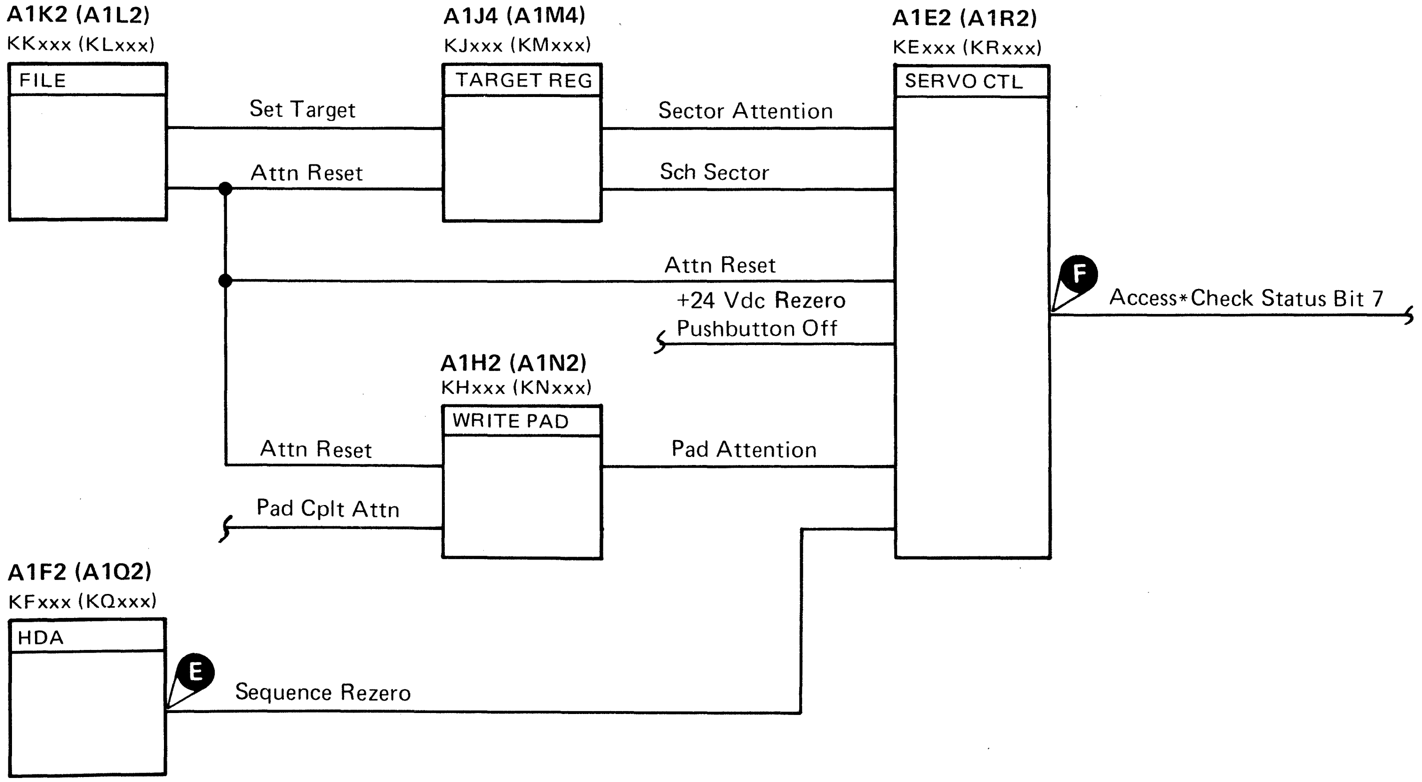


Figure 2. Line Failure Error Codes

Line Name	ALD	Pin	Error Code (Line is Faulty	Page Entry
–Attn Reset	KK170 (KL170)	A1K2 (A1L2) J02	B813	ACC 210, B
+Set Target	KK120 (KL120)	A1K2 (A1L2) J11	B813	ACC 210, B
–Pad Attention	KH210 (KN210)	A1H2 (A1N2) P04	B814	ACC 220, B
+Pad Cplt Attn	KH210 (KN210)	A1H2 (A1N2) P05	B814	ACC 220, B
+Sch Sector	KJ510 (KM510)	A1J4 (A1M4) B03	B813	ACC 210, B
+Sector Attention	KJ510 (KM510)	A1J4 (A1M4) D03	B814	ACC 220, B
+24 Vdc Rezero Pushbutton Off	KE150 (KR150)	A1E2 (A1R2) M03	B821	
+Sequence Rezero	KF150 (KQ150)	A1F2 (A1Q2) G12	A235	DEV-I 160, A

CC0425 Seq. 1 of 2	2358378 Part No.	441300 31 Mar 76	441303 30 Jul 76			

FORMAT MODE/TAG VALID

Fault Symptom Code 191E is caused when the drive Format Mode is not received by storage control or Device Tag Valid is not sent to storage control.

Analysis Procedure

FORMAT MODE

Determine the drive mode by checking the location of the jumper on the card as shown:

Format Mode	Jumper	Returned Bits (HDA Status Bits)
Native	A1F2 (A1Q2) S08 to U08	Bit 6 off, Bit 7 on
3330-1	A1F2 (A1Q2) M08 to P08	Bit 6 on, Bit 7 off
3330-11	A1F2 (A1Q2) G08 to J08	Bit 6 on, Bit 7 on

1. Loop test B and bypass errors:
   1. Load routine BB
   2. Enter 10, 0B, xx, 01, 00
   (xx = Parameter)

Parameter:
Native = '01'
3330-1 = '02'
3330-11 = '03'

2. SCOPE SETUP
   Sweep 10 μs/div
   Trigger
      Slope(−)
      A2G2J05
      −Selected
   Ch 1
      A2G2J11
      +Tag Gate NPL
   Ch 2
      Contr Bus In Bit 6 Ⓙ and 7 Ⓚ.
      Use the sequence chart on DEV-I 435.

TAG VALID

NPL Tag Valid is sent to the controller from the drive. The NPL Tag Valid line is activated by the following circuits:

HDA Status bits 6 and 7 Ⓔ and Ⓕ are gated by Sense Status 1 Ⓑ. Sense Status Ⓐ and Selected cause Sense Status 1 to be active.

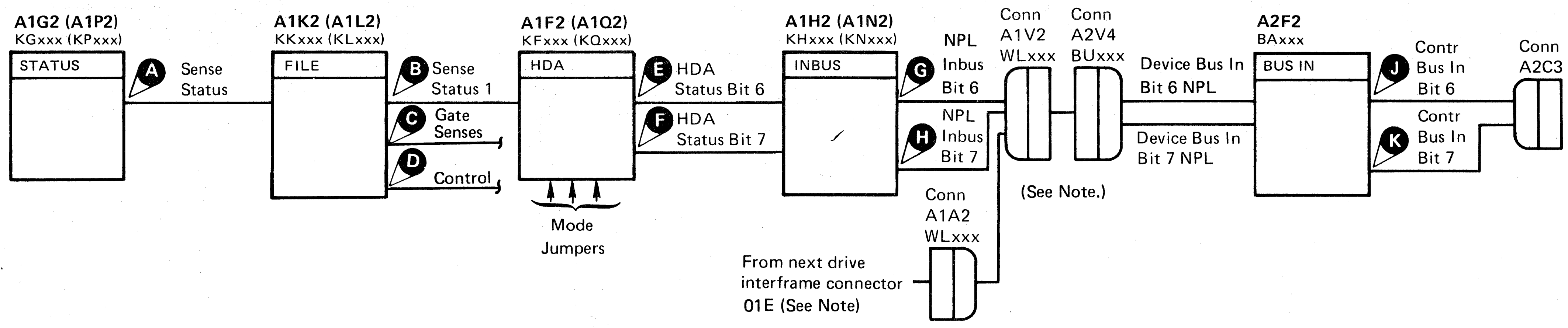
Control Ⓓ causes Gate Senses Ⓒ which activates Sense Status Ⓐ.

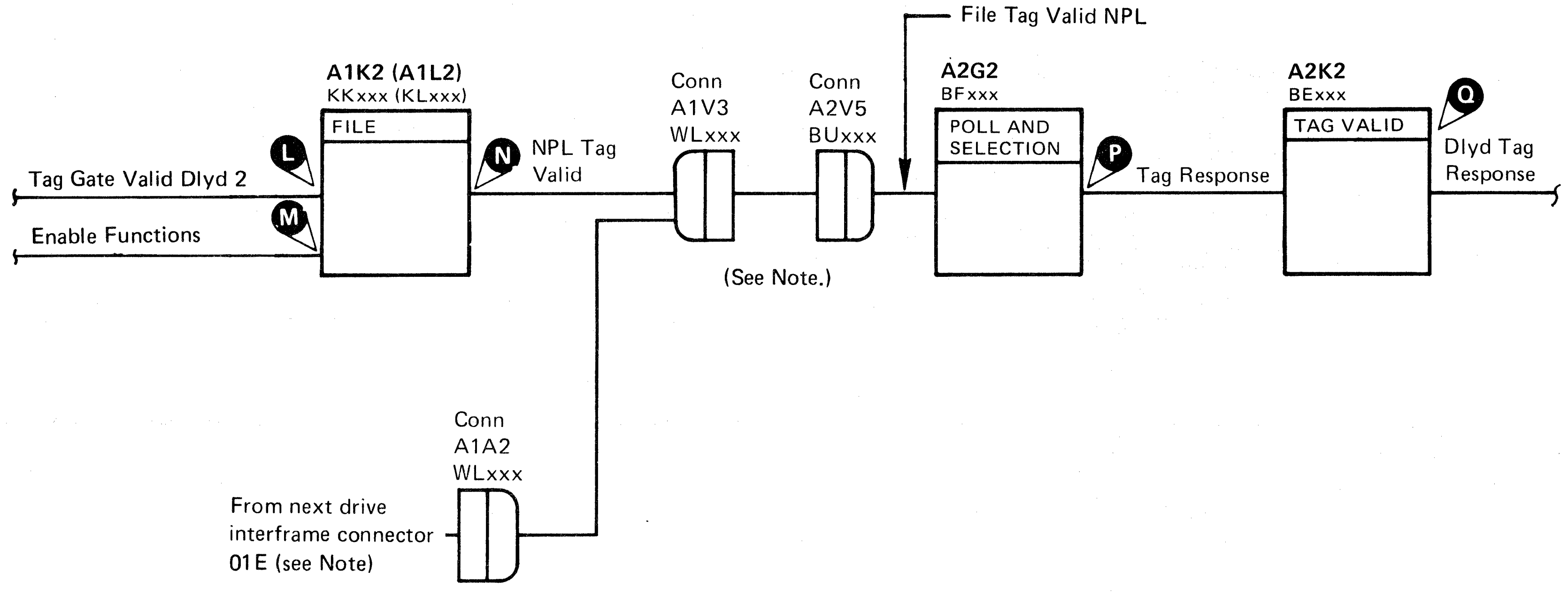
Tag Gate Valid Dlyd 2 Ⓛ, Tag Gate Valid, and Selected activate Enable Functions Ⓜ.

Enable Functions activates NPL Tag Valid Ⓝ.

See DEV-I 116, Entry D for microdiagnostic and scoping procedures.

See OPER 92 for additional theory.





Note: *See DEV-I 100 (DEV-I 90 with C2 Module installed) for details of connectors, interframe cabling, and point-to-point pin assignments.*

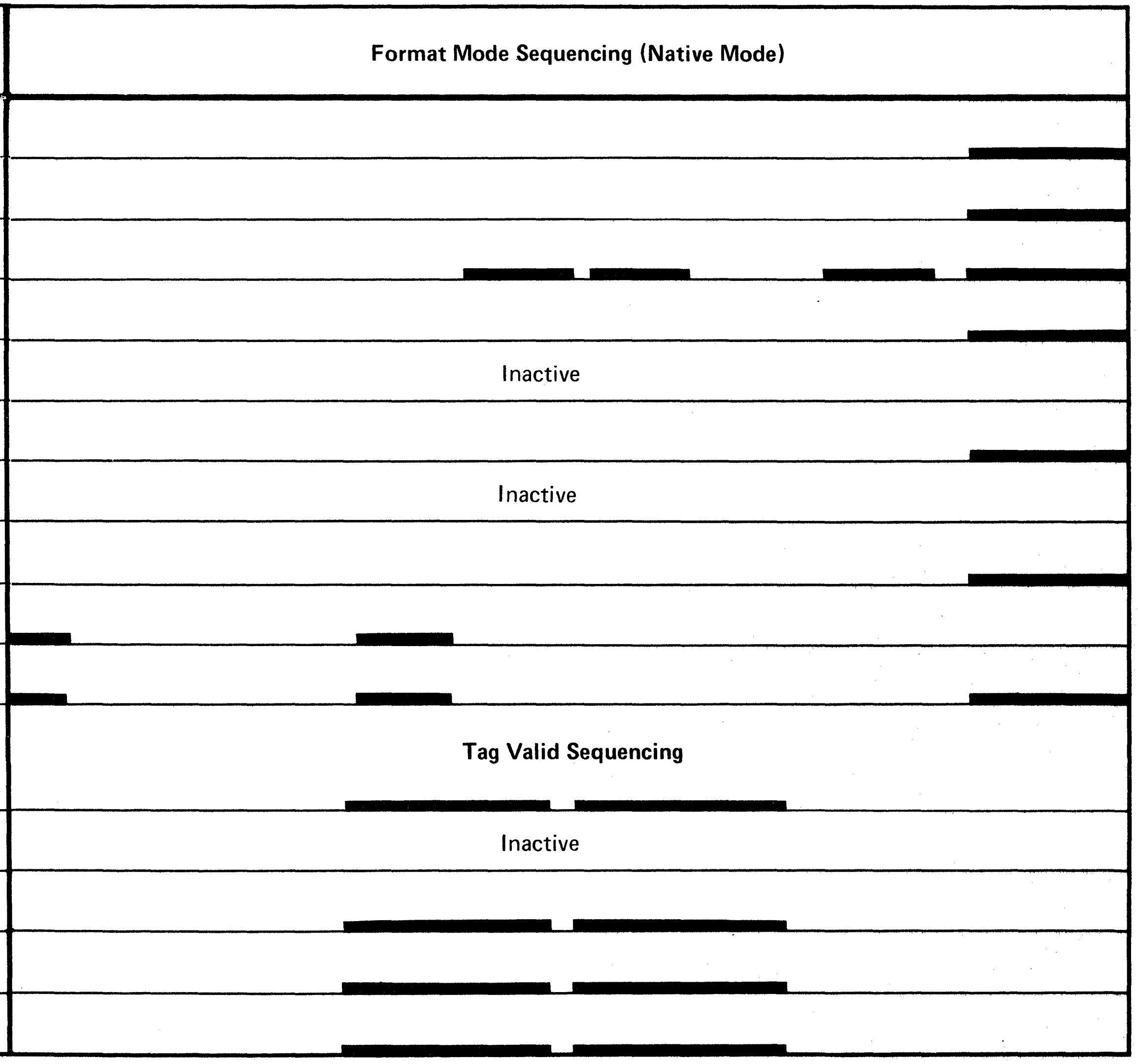
3350

CC0425 Seq. 2 of 2	2358378 Part No.	441300 31 Mar 76	441303 30 Jul 76			

FORMAT MODE/TAG VALID

Legend:
▭ Inactive
▬ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	–Gate Senses	KK170 (KL170)	A1K2 (A1L2) J10	Ⓒ
2	–Sense Status	KG190 (KP190)	A1G2 (A1P2) S13	Ⓐ
3	+Control	KK120 (KL120)	A1K2 (A1L2) M05	Ⓓ
4	–Sense Status 1	KK170 (KL170)	A1K2 (A1L2) U05	Ⓑ
5	+HDA Status Bit 6	KF240 (KQ240)	A1F2 (A1Q2) J03	Ⓔ
6	+HDA Status Bit 7	KF240 (KQ240)	A1F2 (A1Q2) J11	Ⓕ
7	+NPL Inbus Bit 6	KH200 (KN200)	A1H2 (A1N2) B02	Ⓖ
8	+NPL Inbus Bit 7	KH200 (KN200)	A1H2 (A1N2) D06	Ⓗ
9	+Contr Bus In Bit 6	BA150	A2F2 J11	Ⓙ
10	+Contr Bus In Bit 7	BA150	A2F2 J03	Ⓚ
11	–Tag Gate Valid Dlyd 2	KK160 (KL160)	A1K2 (A1L2) U02	Ⓛ
12	+Enable Functions	KK150 (KL150)	A1K2 (A1L2) G10	Ⓜ
13	+NPL Tag Valid	KK140 (KL140)	A1K2 (A1L2) B07	Ⓝ
14	+Tag Response	BF160	A2G2 S05	Ⓟ
15	–Dlyd Tag Response	BE150	A2K2 D10	Ⓠ



CC0435 Seq. 1 of 2	2358379 Part No.	441300 31 Mar 76	441303 30 Jul 76			

TROUBLE NOT FOUND

This page contains aids for problem resolution where insufficient error information is available to follow the maintenance analysis procedure. It may also be used as an aid in analyzing intermittent errors.

VOLTAGE CHECKS

Check for unstable voltage (–4 Vdc, +6 Vdc) on a drive or controller board. The voltages can be monitored while looping a failing microdiagnostic or while the machine is running online. See PWR 90 (controller) or PWR 290 (drive) for procedure and tolerances.

VISUAL CHECKS

Connectors

Check for bent or damaged pins, foreign objects between pins, and proper seating.

Back Panel Wiring

Check for a tight wire wrap cutting into a pin on the back panel.

Check for a cracked land pattern on a board or card.

EC INSTALLATION

If an engineering change has been recently installed, check the EC installation instructions and determine where the change was made.

ISOLATION PROCEDURE

If all drives fail, suspect a controller board or cabling problem. If one drive fails, cards can be interchanged to see if the trouble moves.

Drive A	Drive B
A1K2	A1L2
A1J2	A1M2
A1J4	A1M4
A1H2	A1N2
A1G2	A1P2
A1F2	A1Q2
A1E2	A1R2

If it is not known if all the drives or one drive is failing, use the isolation procedure on DEV-I 162, Entry A. Loop the failing test.

Isolation references:

DEV-I 100	Diagrams the Device cables.
DEV-I 162	Isolation procedure.
DEV-I 164	Attention/Select Response diagram

REFERENCES

Microdiagnostic Routine A2 Summary

Test 1

See OPER 110 (Select Operation).

- Selects a drive (Tag '83').
  See OPER 104.
- Resets Device Interface Checks (Tag '89').
  See OPER 104.
- Verifies that Tag Valid is returned for Tag '83' and Tag '89'.
  See OPER 105.

Test 2

- Verifies that Device Tag Bus Parity Check can be set and reset.
- Verifies that Device Bus Out Parity Check can be set and reset.

Test 3

- Verifies that a data path exists between Device Bus Out and Device Bus In.
  See OPER 105.
- Sets and senses Difference Counter and compares Device Bus Out and Device Bus In.
  If they are not equal, HAR is set and sensed and Device Bus Out is compared to Device Bus In.
  See OPER 105.

Test 4

- Test to be sure a drive cannot be selected with Bus Out Bit 4 on.
- Verifies Check 1 of 8 is operating properly.

Test 5

- Issues all drive tags and checks for Tag Valid.

Test 6

- Makes sure that Tag Valid is not received when Tag Bus Parity is inverted.

Test 7

- Verifies that Bus In Parity can be set and reset.
  See OPER 105.
- Tests the Fixed Head Bits and Direction Bit for proper operation.
  See OPER 105.

Test 8

- Sets and senses HAR for proper operation.
  See OPER 105.

Test 9

- Sets and senses the Difference Counter for proper operation.
  See OPER 105.

Test A

- Verifies that the Difference Counter decrements properly.
  See OPER 105.

Test B

- Sets and senses CAR for proper operation.
  See OPER 105.

DATA CONTENTS

The DATA section is organized by routine and test number. Each routine and test group contain:

1. One or more MAP pages (flowchart)
2. Overview diagram
3. Overview sequence chart
4. Supporting sequence charts (if required)

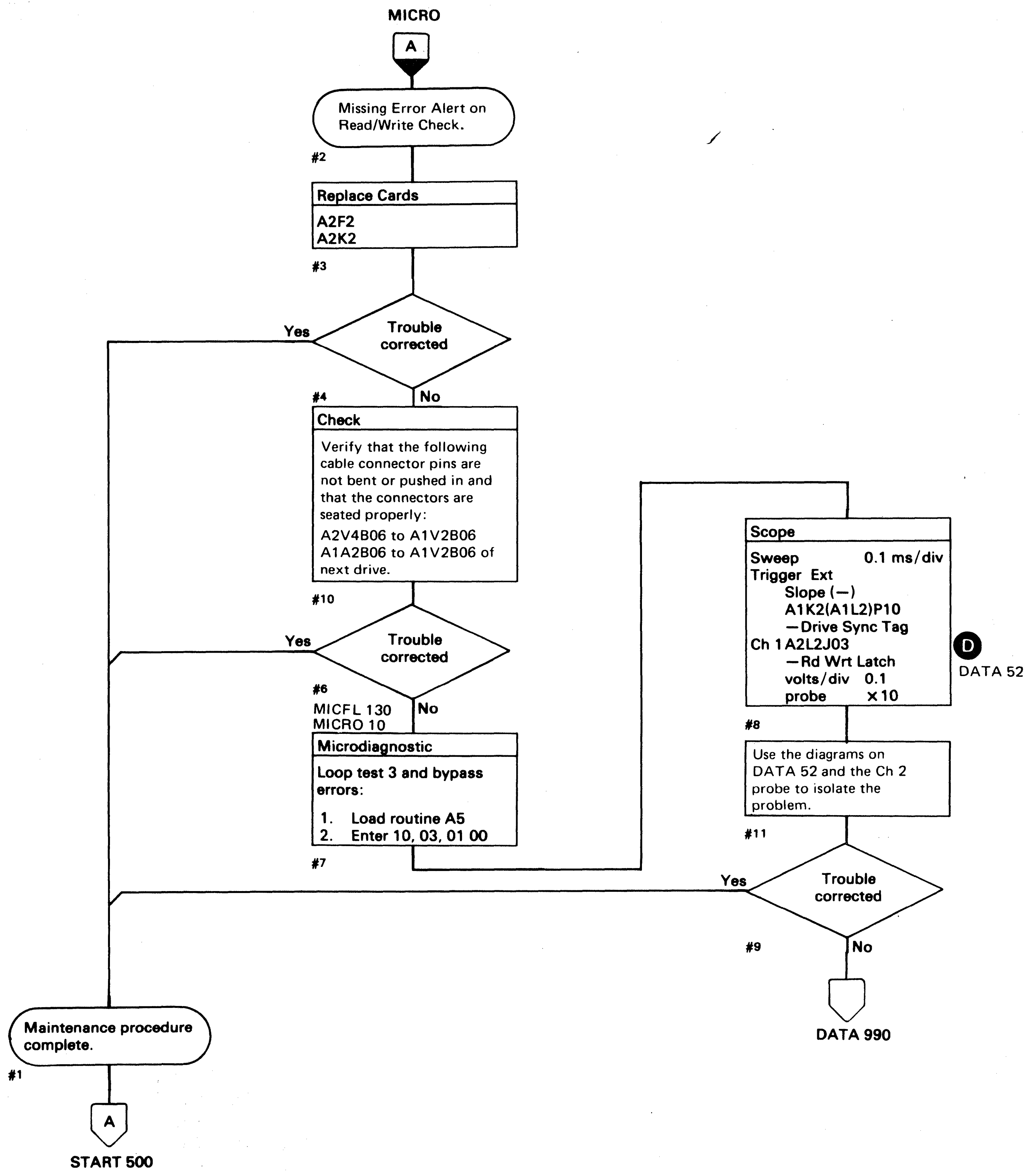
REFERENCE TO OTHER SECTIONS

ERROR DESCRIPTION

Device Bus In bit 3 indicates a Read/Write Check has occurred for an operation other than specified Sense operations. The Read/Write Check is the only drive-detected error condition causing an Error Alert.

Routine 5, test 3:

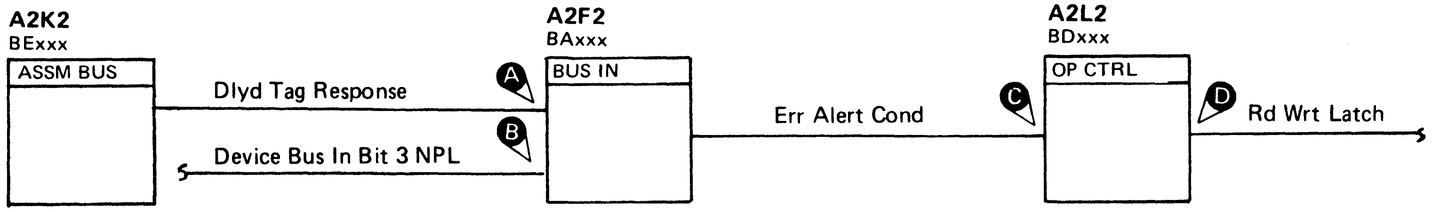
1. **Forces a Read/Write Check.**
2. **Verifies that the Read/Write Check latch is set.**
3. **Verifies that the Error Alert Condition line is active.**



CE0001 Seq 2 of 2	2358186 Part No.	441300 31 Mar 76	441303 30 Jul 76			

READ/WRITE CHECK

See OPER 241 for theory.



Legend:
- ▭ Inactive
- ■ Active level
- ▨ Tolerance

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 0.1 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A1K2(A1L2)
-Drive Sync Tag

Ch 1 A2L2 J03
-Rd Wrt Latch
Volts/div 0.1
Probe X10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 0.1 ms/div
Slope (-)
Delay Time-Delayed Sweep – 5 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Chart Line No.	Line Name	ALD	Test Point		32
1	-Rd Wrt Latch	BD150	A2L2 J03	D	
2	+Device Bus In Bit 3 NPL	BA160	A2F2 B09	B	
3	–Dld Tag Response	BA140	A2F2 D13	A	
4	-Err Alert Cond	BD170	A2L2 B07	C	

CE0085 Seq. 1 of 2	2358484 Part No.	441300 31 Mar 76	441303 30 Jul 76			

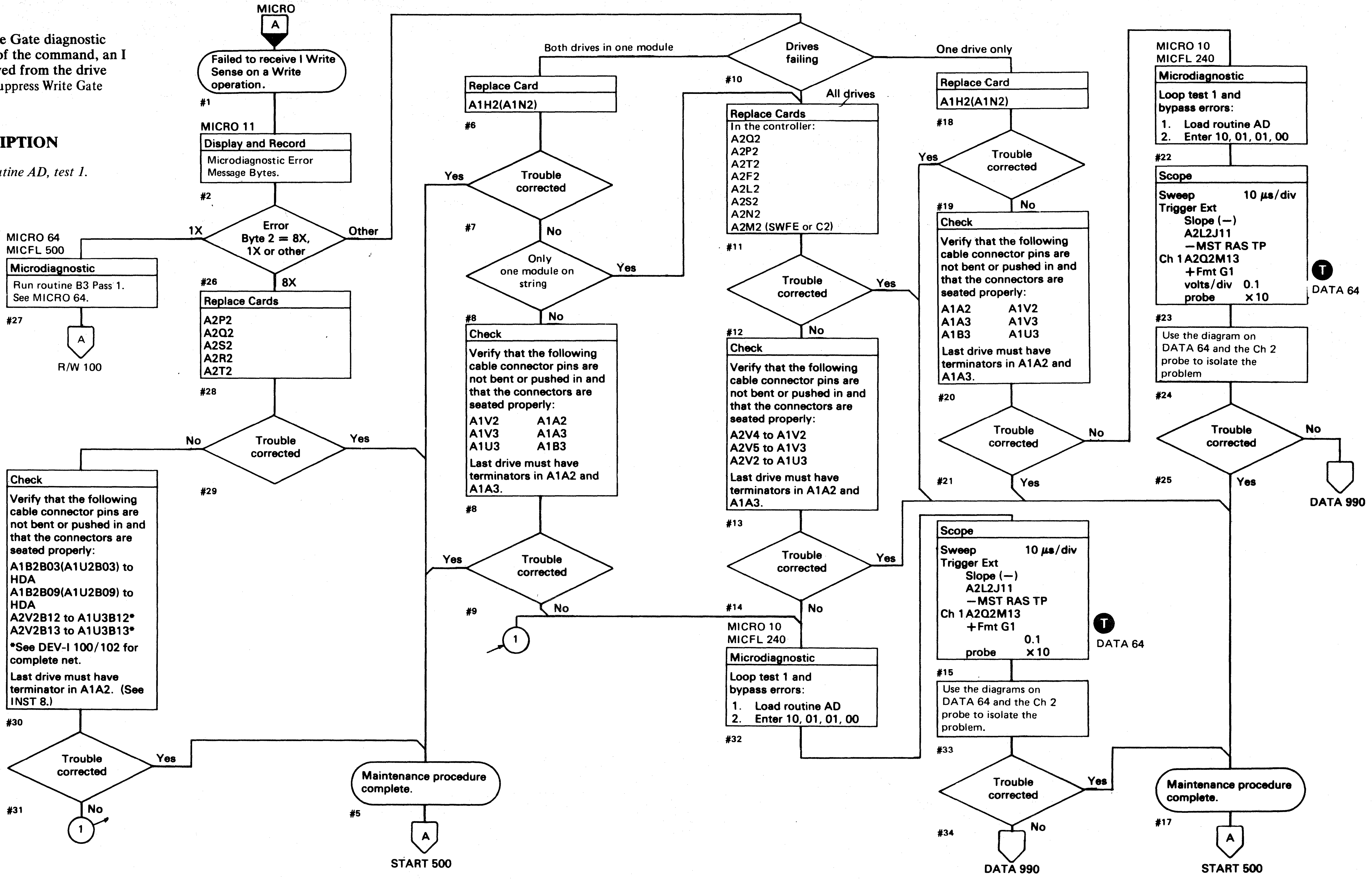
I WRITE SENSE FAILURE

ERROR DESCRIPTION

Routine AD uses the Suppress Write Gate diagnostic command. To verify the operation of the command, an I Write Sense response must be received from the drive when Write Gate is activated without Suppress Write Gate being set.

MICRODIAGNOSTIC DESCRIPTION

See DATA 140 for a description of routine AD, test 1.



3350	CE0085 Seq. 2 of 2	2358484 Part No.	441300 31 Mar 76	441303 30 Jul 76			

I WRITE SENSE AND SUPPRESS WRITE

ERROR DESCRIPTION

I Write Sense

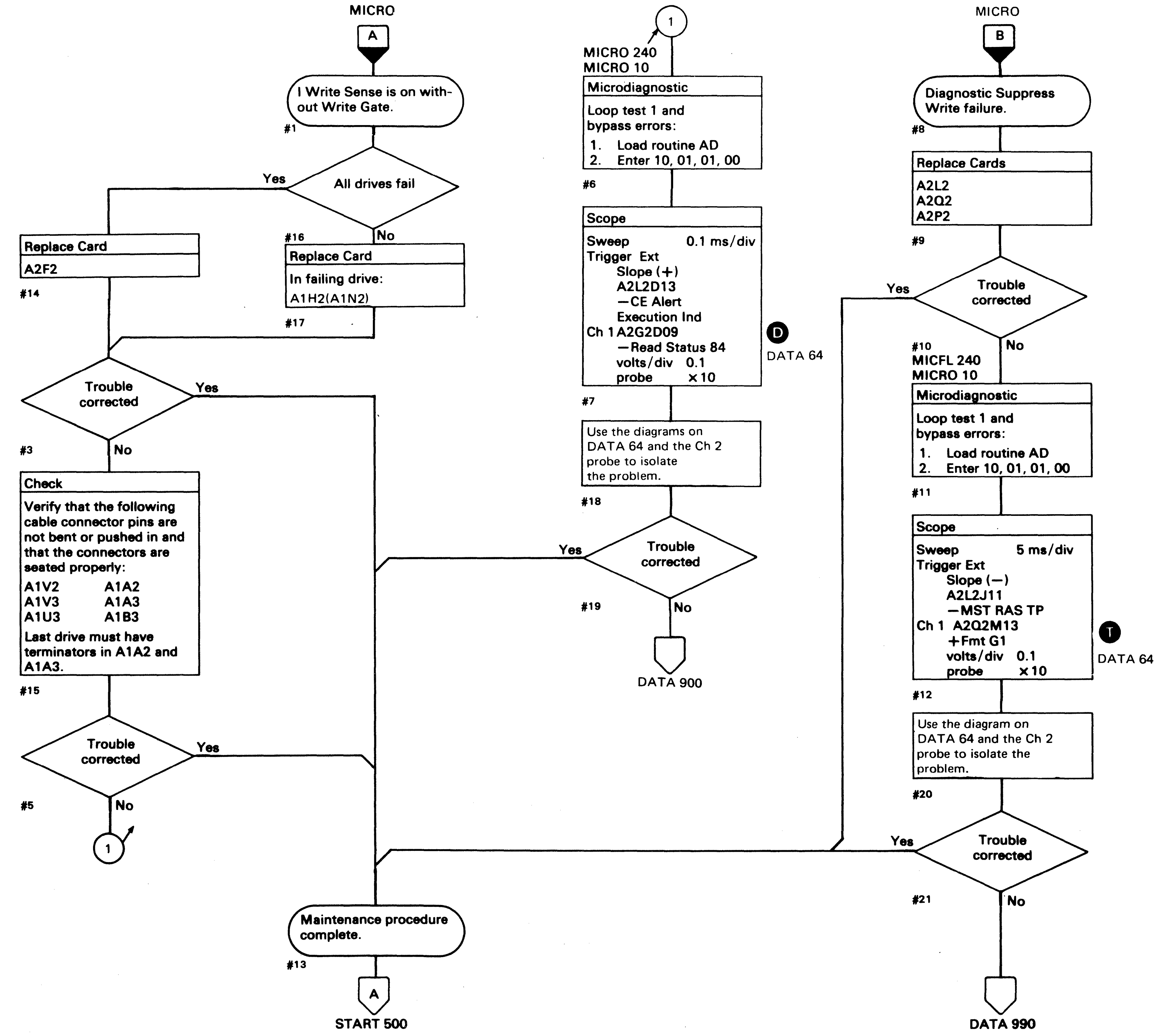
If I Write Sense is on after the Read/Write latch is set (but prior to raising Write Gate), an error stop occurs.

Diagnostic Suppress Write Failure

A failure occurs if Write Gate becomes active after setting Suppress Write. If I Write Sense is returned by the drive, Write Gate was not suppressed.

MICRODIAGNOSTIC DESCRIPTION

See DATA 140 for a description of routine AD, test 1.



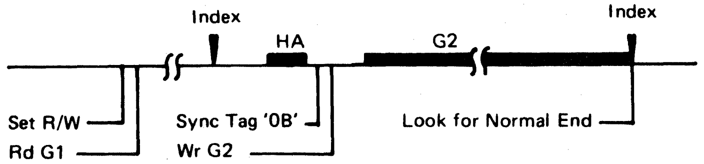
GAP COUNTER FAILURE

MICRODIAGNOSTIC DESCRIPTION

See DATA 74 for a description of routine AD, test 1.

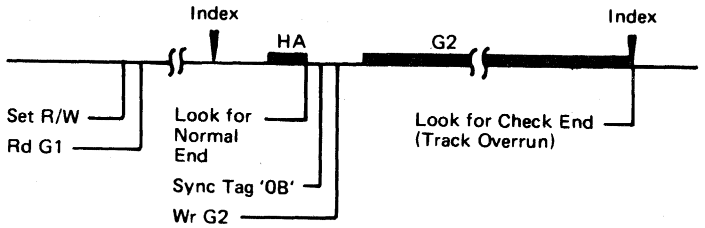
Routine AF, test 6 reads the Home Address and then writes a record that checks the track capacity, that is, the maximum number of bytes that fit the track. An Error Code of AF6B indicates a Track Overrun may result if the track is formatted with an Extend G1. Run routine AF, test E to restore the G1 field to its normal position.

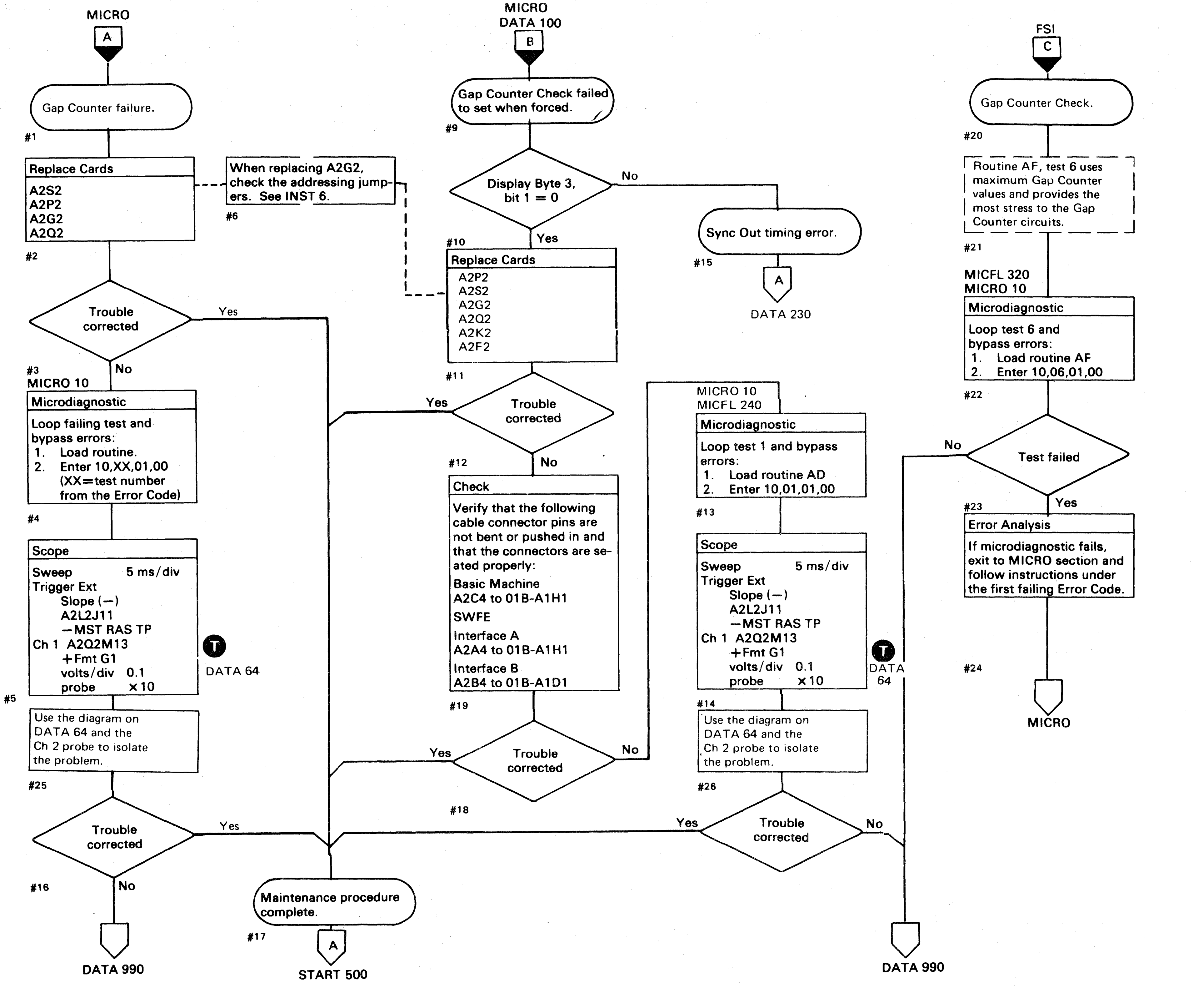
TEST 6



Routine AF, test 7 operates the same as test 6 except that a few bytes are added so that Track Overrun occurs.

TEST 7





PHASE ERROR

ERROR DESCRIPTION

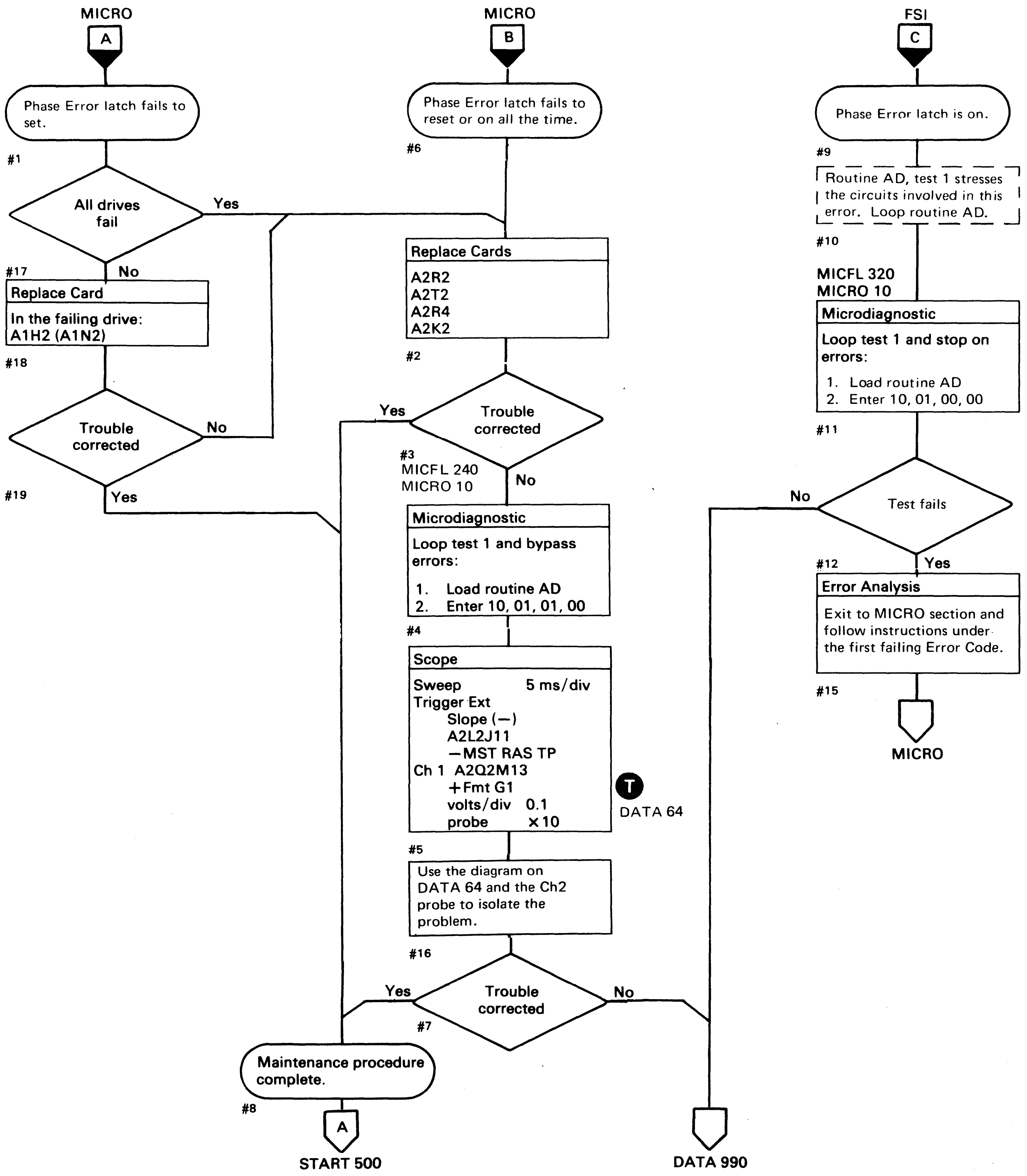
In Write mode, the VFO must be synchronized to the servo pulses from the drive to ensure proper data recording. If the synchronization does not occur, a phase error results.

The servo pulses are sent to the read circuits. If data bits (standardized data), as opposed to clock bits, are decoded, an error is posted.

This test forces standardized data during a Write operation and verifies that the Phase Error latch can be set and reset.

MICRODIAGNOSTIC DESCRIPTION

See DATA 74 for a description of routine AD, test 1.



AD TEST 1 DIAGRAM

See the sequence chart on DATA 66 for referenced test points.

MICRODIAGNOSTIC DESCRIPTION

Routine AD tests these operations:

- Diagnostic Suppress Write
- Gap Counter Check
- Write Data Check
- Phase Error

The most complex portion of the tests is the Diagnostic Suppress Write test because of the many interdependencies involved. After the drive is selected, a check is made to ensure that the I Write Sense latch is not on prior to activating Write Gate. (The I Write Sense latch activates Dev BI Bit 1 MST Ⓧ.)

The test establishes a timing relationship with the disk by searching for the Index. No Phy Index Ⓝ, within a prescribed period, results in Test Error Number 14. Approximately one half revolution of the disk later, a Write G1 command is issued, allowing the Fmt G1 Ⓣ gate to start at the following Index time. This sequence provides stability for scoping sequences.

Following the Index and the start of Fmt G1, Dev BI Bit 1 MST is sensed, and its status is saved for later examination; a Reset R/W operation is also performed. If Dev BI Bit 1 MST equals 0, I Write Sense is not active, and Test Error Number 15 is formed.

The signal lines that affect I Write Sense are:

Name		Condition
Suppress Write Gate	Ⓜ	Always active
Write Gate Suppressed	Ⓤ	Missing
Write Gate		Missing
Addr Mark Gate	Ⓦ	Missing
Rd Wrt Latch	Ⓗ	Missing
Fmt G1	Ⓣ	Missing
Reset RW Op 05	Ⓑ	Always active
Write Sense (in drive)		Missing

Successful execution proves that I Write Sense is operating correctly. The next step is to prove that Suppress Write Gate Ⓜ will block I Write Sense.

Suppress Write Gate is activated, and then the previously described procedure is executed, except that the I Write Sense latch is expected to be off, as indicated by the Device Bus In Bit 0 equal to 0. If the Device Bus In Bit 0 equals 1, I Write Sense is active, and Test Error Number 16 is formed.

The signal lines that affect I Write Sense are:

Name		Condition
Suppress Write Gate	Ⓜ	Missing
Write Gate Suppressed	Ⓤ	Not suppressed
Write Sense (in drive)		Active
Other unexpected error conditions		

Successful execution proves that I Write Sense is functioning correctly and can be used for the remainder of this test and for subsequent tests.

Invert Bus Out Par Bit Ⓙ activates Counter Check Ⓡ and Wr Data Check Ⓠ. This is accomplished in the following way:

- Counter Check is activated when Bus Out Bits 4 through 7 under Tag '0F' are transferred to the Gap Counter, along with the generated parity on 4 to 7 Odd Ⓔ. Invert Bus Out Par Bit also inverts 4 to 7 Odd to activate Counter Check.
- Wr Data Check is activated when a noncompare condition exists between the parity bit received and the parity generated for SERDES. The controller receives 8 bits plus parity for each data byte on a Write operation. Only the 8 bits are serialized into SERDES and written on the disk. After a byte has been serialized, parity is generated for SERDES and compared with the parity bit received.

Suppress Write Gate activates Phase Error Ⓛ when Invert Bus Out Par Bit and Suppress Write Gate are active, forcing Standard Data on a Write operation. Following the Write G1 operation, the following conditions are checked:

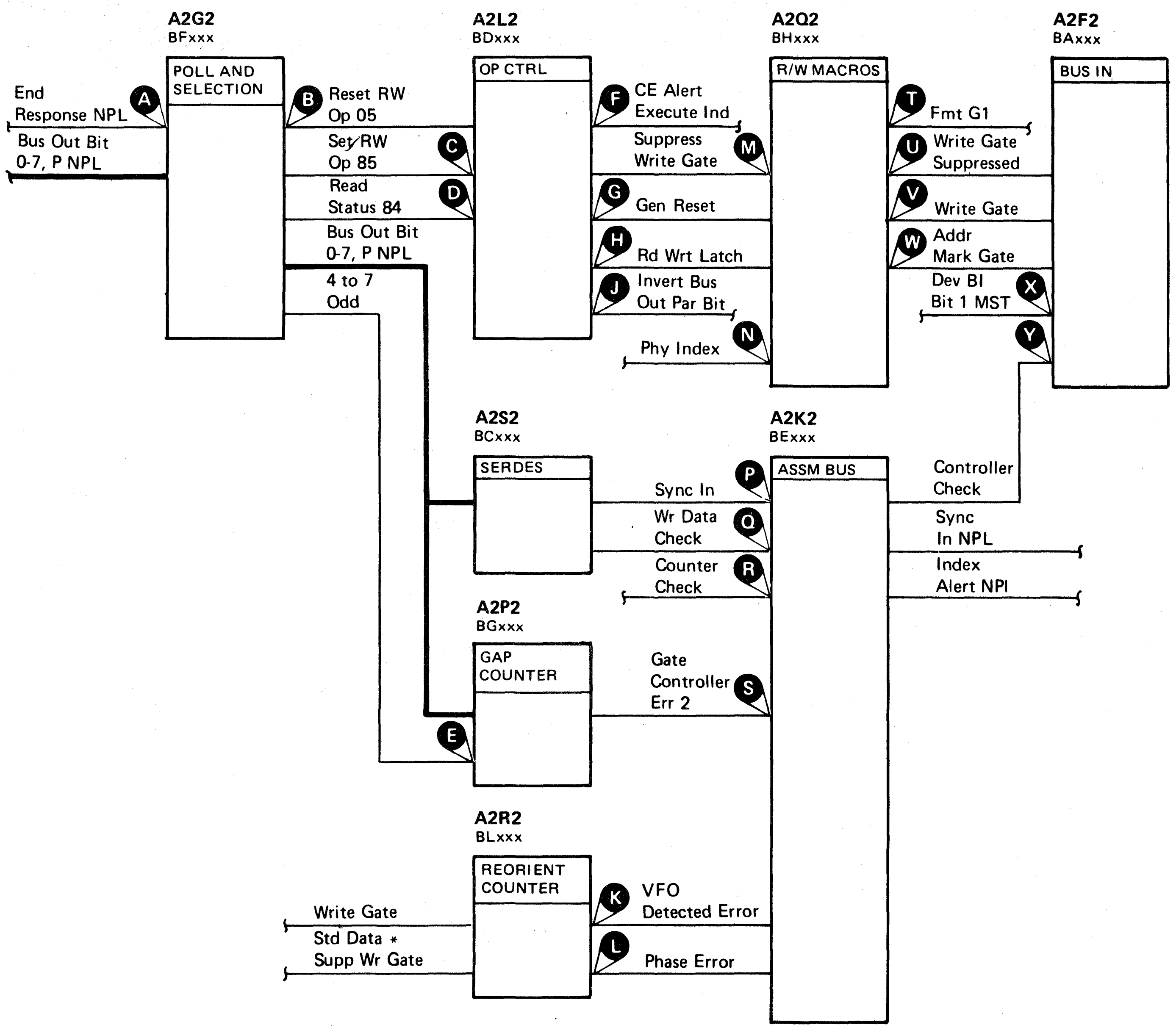
Name		Error Number (if not active)
Counter Check	Ⓡ	18
Wr Data Check	Ⓠ	1A
Phase Error	Ⓛ	1D
Controller Check	Ⓨ	1B

After a controller reset, the following latches are checked; they should be inactive:

Name		Error Number (if active)
Counter Check	Ⓡ	1C
Phase Error	Ⓛ	1E

These checks are made while data is being processed:

- If there are Sync In pulses but no End condition exists, Test Error Number 17 is formed.
- If there are no Sync In pulses prior to an End condition, Test Error Number 1F is formed.



AD TEST 1 SEQUENCE CHART

Microdiagnostic Setup

Routine AD, test 1

1. Load AD
2. Enter 10,01,01,00

Scope Setup

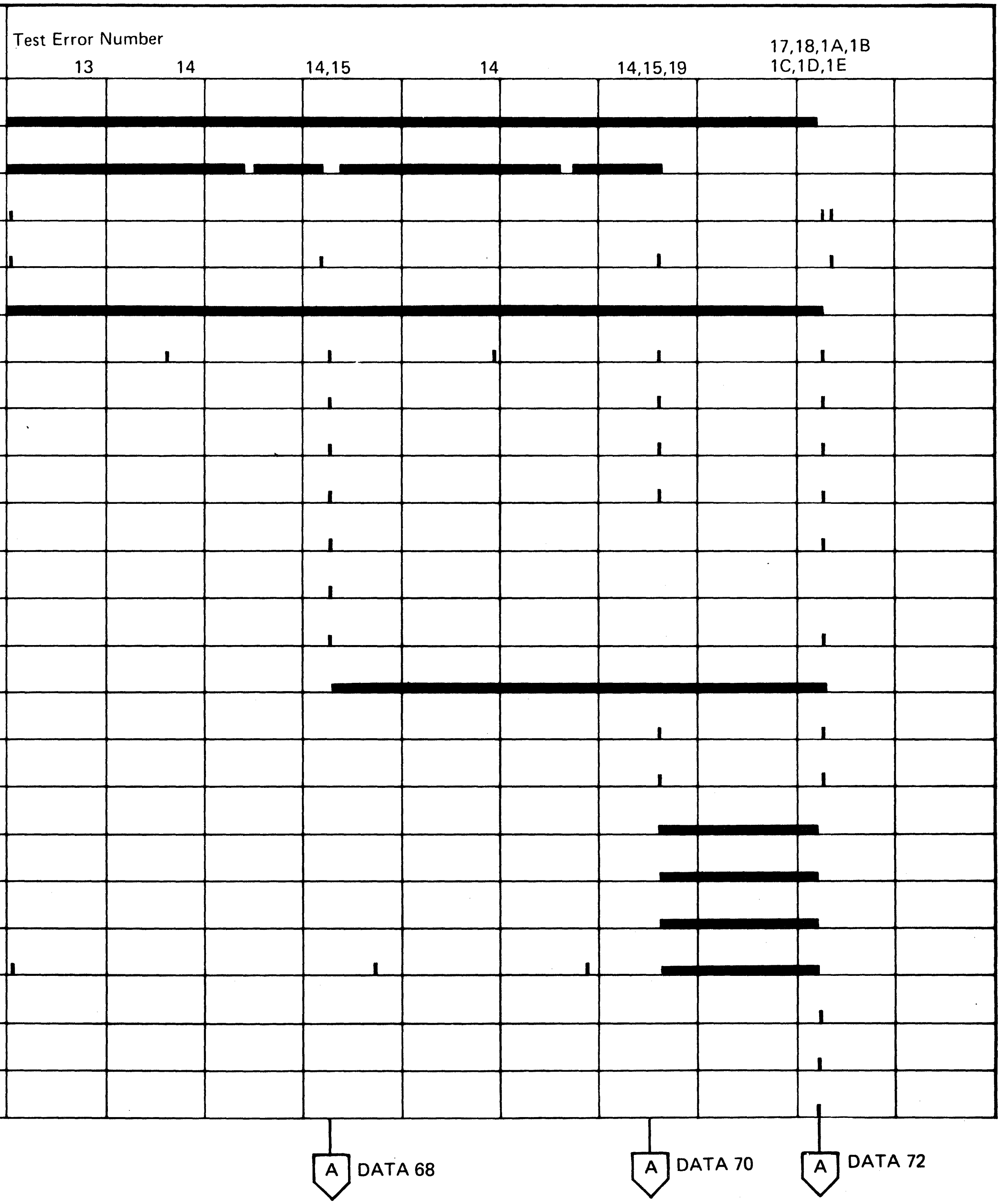
Sweep 5 ms/div
Mode Alt or Chop

Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	F
2	–Read Status 84	BD100	A2L2 P09	D
3	+ Gen Reset	BD100	A2L2 B10	G
4	–Set RW Op 85	BD150	A2L2 M08	C
5	–Rd Wrt Latch	BD150	A2L2 J03	H
6	–Phy Index	BH130	A2Q2 S07	N
7	+Fmt G1	BH140	A2Q2 M13	T
8	–Write Gate	BH140	A2Q2 G10	V
9	–Addr Mark Gate	BH140	A2Q2 U06	W
10	–Write Gate Suppressed	BH140	A2Q2 P07	U
11	+Dev BI Bit 1 MST	BA160	A2F2 S10	X
12	+Reset RW Op 05	BD100	A2G2 D05	B
13	+Suppress Write Gate	BH140	A2Q2 U03	M
14	–Gate Controller Err 2	BE120	A2K2 M03	S
15	+Phase Error	BL120	A2R2 D07	L
16	–VFO Detected Error	BL140	A2R2 G05	K
17	–Controller Check	BA130	A2F2 P02	X
18	–Invert Bus Out Par Bit	BD170	A2L2 J06	J
19	–4 to 7 Odd	BG100	A2P2 P05	E
20	–Counter Check	BE120	A2K2 S07	R
21	–Wr Data Check	BE120	A2K2 P05	Q
22	+End Response NPL	BF160	A2G2 S03	A



Line keys reference the diagram on DATA 64.

(For expanded sequence chart)

AD TEST 1 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 10 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2M13
+ Fmt G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 10 ms/div
Slope (+)
Delay Time-Delayed Sweep – 5 μs/div
Delay-Time Multiplier – 2.5
Source – Int Ch 1

DATA 66
A

Legend:
▭ Inactive
■ Active level
▨ Tolerance

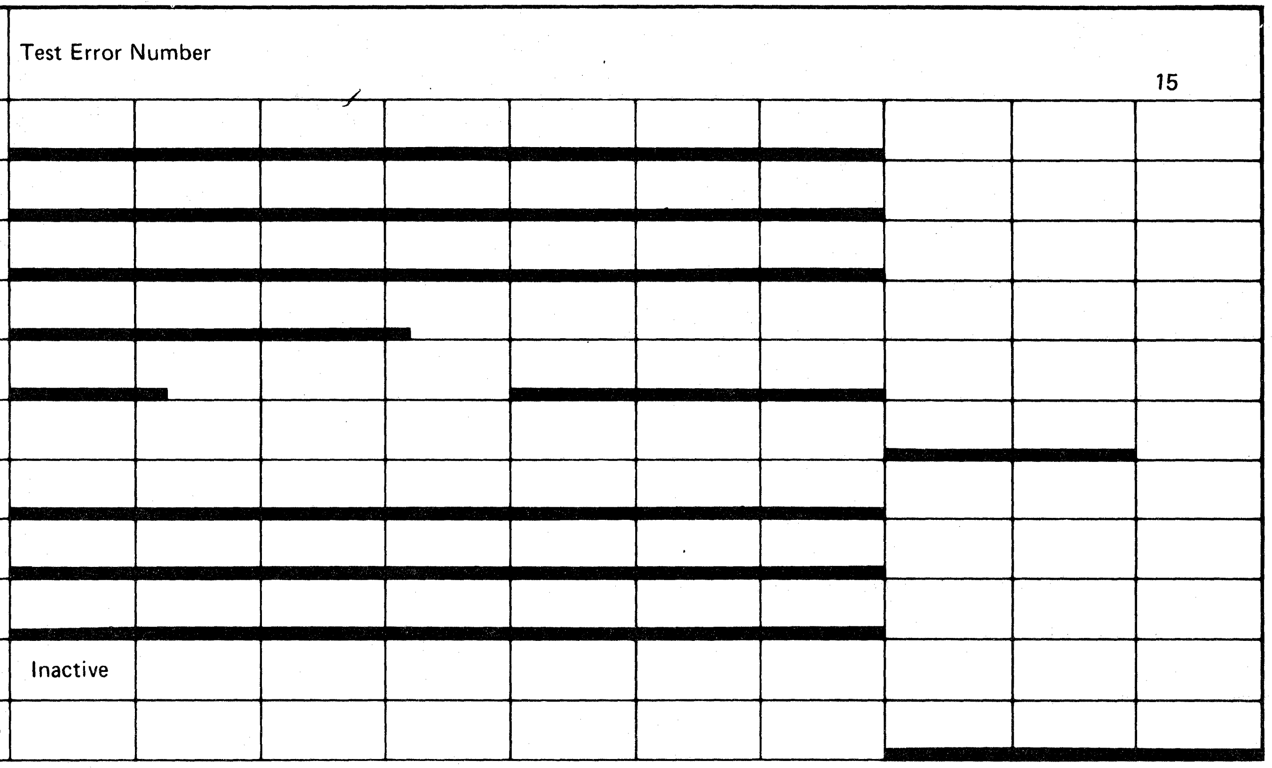


Chart Line No.	Line Name	ALD	Test Point		Test Error Number 15
1	+Fmt G1	BH140	A2Q2 M13	T	
2	+Dev BI Bit 1 MST	BA160	A2F2 S10	X	
3	–Rd Wrt Latch	BD150	A2L2 J03	H	
4	–Phy Index	BH130	A2Q2 S07	N	
5	–Read Status 84	BD100	A2L2 P09	D	
6	+Reset RW Op 05	BD100	A2G2 D05	B	
7	–Write Gate Suppressed	BH140	A2Q2 P07	U	
8	–Write Gate	BH140	A2Q2 G10	V	
9	–Addr Mark Gate	BH140	A2Q2 U06	W	
10	+Suppress Write Gate	BD170	A2Q2 U03	M	Inactive
11	–4 to 7 Odd	BG100	A2P2 P05	E	

Line keys reference the diagram on DATA 64.

AD TEST 1 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 10 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

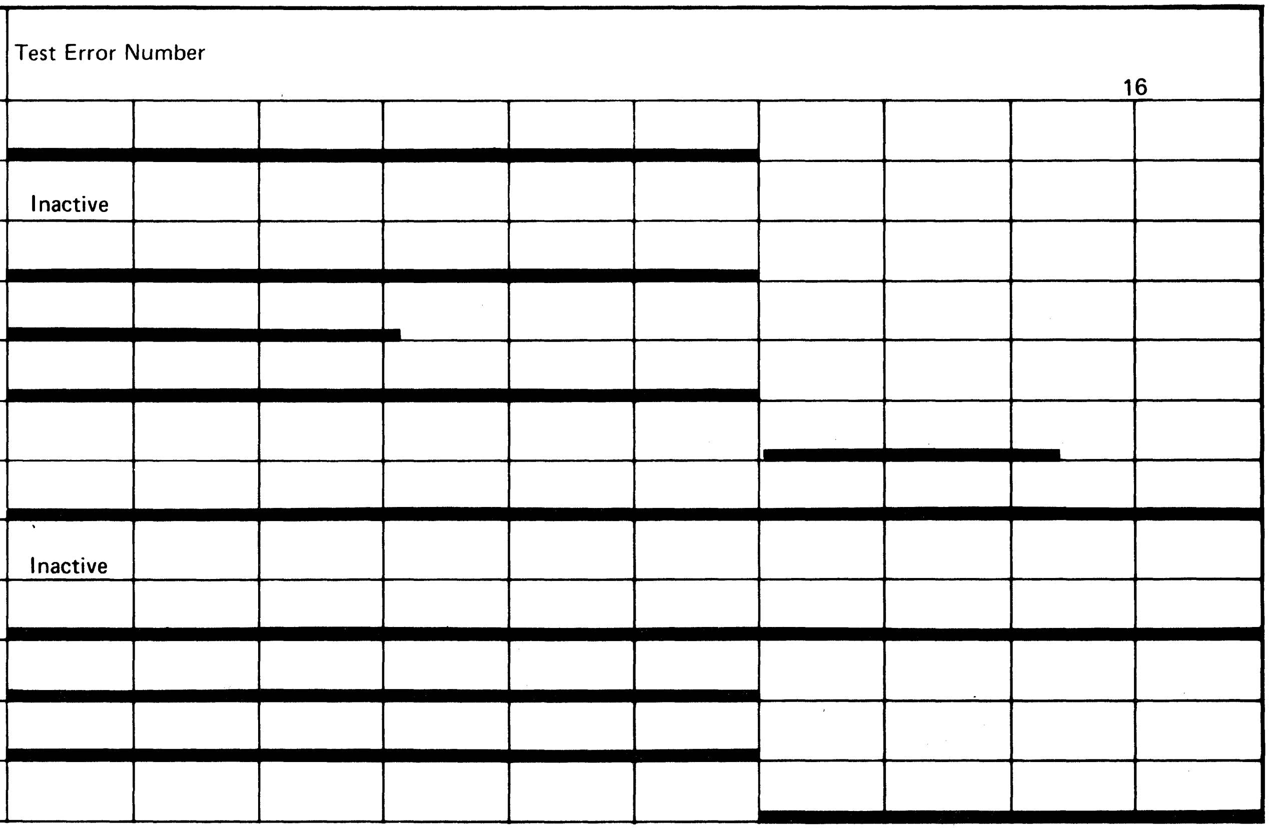
Ch 1 A2Q2M13
+Fmt G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 10 ms/div
Slope (+)
Delay Time-Delayed Sweep – 5 μs/div
Delay-Time Multiplier – 3.5
Source – Int Ch 1

DATA 66
A

Legend: ▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+Fmt G1	BH140	A2Q2 M13	T
2	+Dev BI Bit 1 MST	BA160	A2F2 S10	X
3	–Rd Wrt Latch	BD150	A2L2 J03	H
4	–Phy Index	BH130	A2Q2 S07	N
5	–Read Status 84	BD100	A2L2 P09	D
6	+Reset RW Op 05	BD100	A2G2 D05	B
7	+Suppress Write Gate	BH140	A2Q2 U03	M
8	–Write Gate Suppressed	BH140	A2Q2 P07	U
9	–VFO Detected Error	BL140	A2R2 G05	K
10	–Write Gate	BH140	A2Q2 G10	V
11	–Addr Mark Gate	BH140	A2Q2 U06	W
12	–4 to 7 Odd	BG100	A2P2 P05	E



Line keys reference the diagram on DATA 64.

AD TEST 1 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

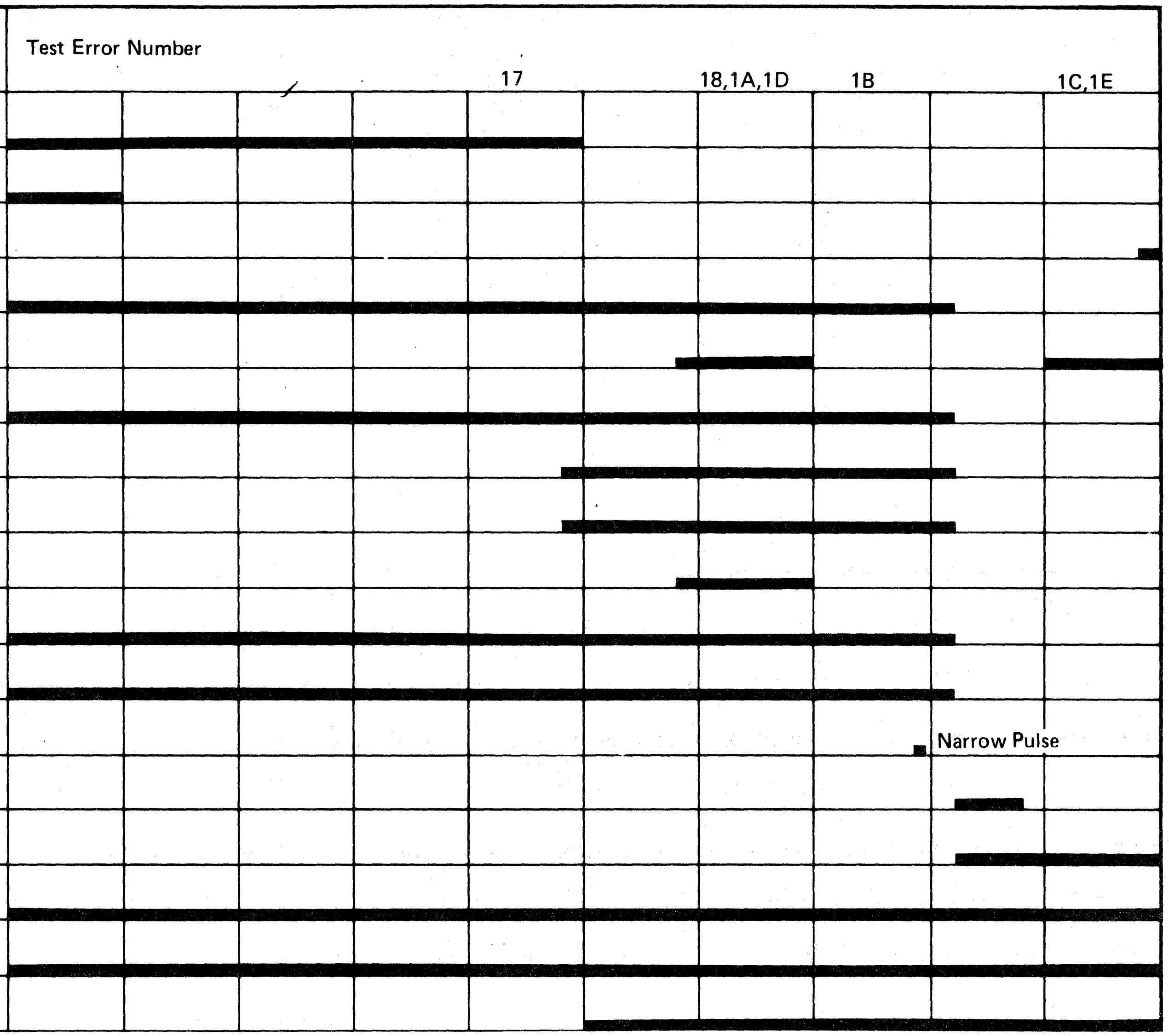
Sweep	10 ms/div	Ch 1 A2Q2M13	
Mode	Alt or Chop	+Fmt G1	
Trigger	Ext	Volts/div	0.1
	Slope (+)	Probe	x10
	A2L2D13	Ch 2 (See chart)	
	+CE Alert Execute Ind		

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 10 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 7.0
Source – Int Ch 1

DATA 66
A

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+Fmt G1	BH140	A2Q2 M13	Ⓣ
2	–Phy Index	BH130	A2Q2 S07	Ⓝ
3	+Reset RW Op 05	BD100	A2G2 D05	Ⓑ
4	+Suppress Write Gate	BH140	A2Q2 U03	Ⓜ
5	–Gate Controller Err 2	BE120	A2K2 M03	Ⓢ
6	–Invert Bus Out Par Bit	BD120	A2L2 J06	Ⓙ
7	–Counter Check	BE120	A2K2 S07	Ⓡ
8	–Wr Data Check	BE120	A2K2 P05	Ⓠ
9	+Phase Error	BL170	A2R2 D07	Ⓛ
10	–VFO Detected Err	BL140	A2R2 G05	Ⓚ
11	–Controller Check	BA130	A2F2 P02	Ⓨ
12	+End Response NPL	BF160	A2G2 S03	Ⓐ
13	+Gen Reset	BD100	A2L2 B10	Ⓖ
14	–Write Gate Suppressed	BH140	A2Q2 P07	Ⓤ
15	–Write Gate	BH140	A2Q2 G10	Ⓥ
16	–Addr Mark Gate	BH140	A2Q2 U06	Ⓦ
17	–4 to 7 Odd	BG100	A2P2 P05	Ⓔ



Line keys reference the diagram on DATA 64.

CONTROLLER CHECK

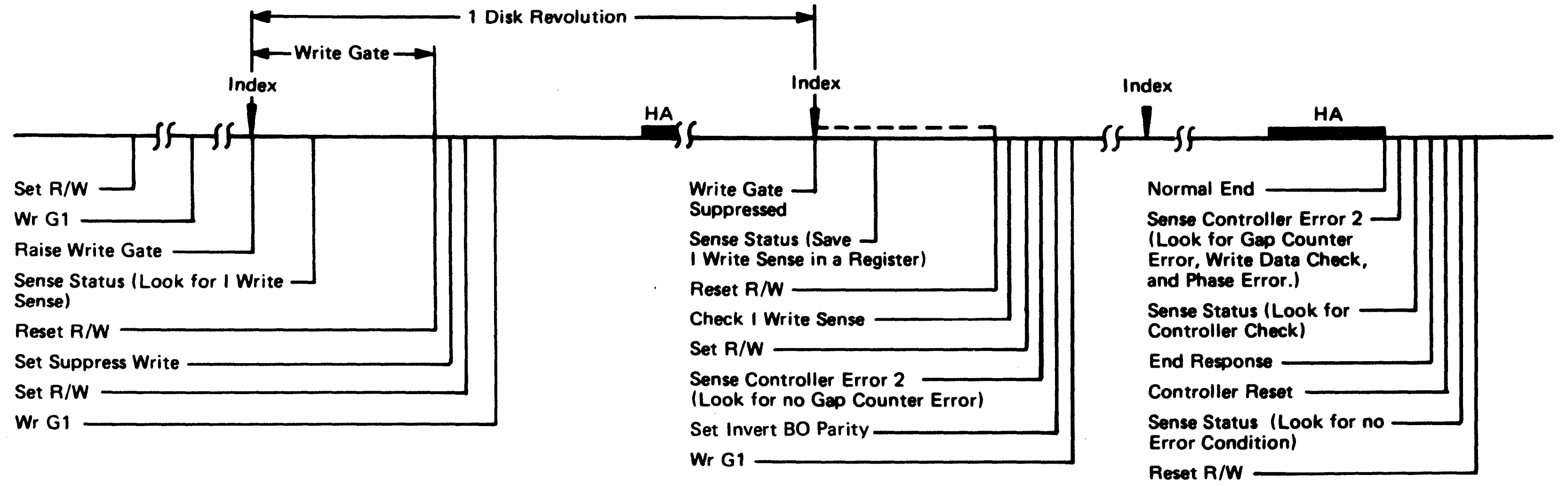
MICRODIAGNOSTIC DESCRIPTION

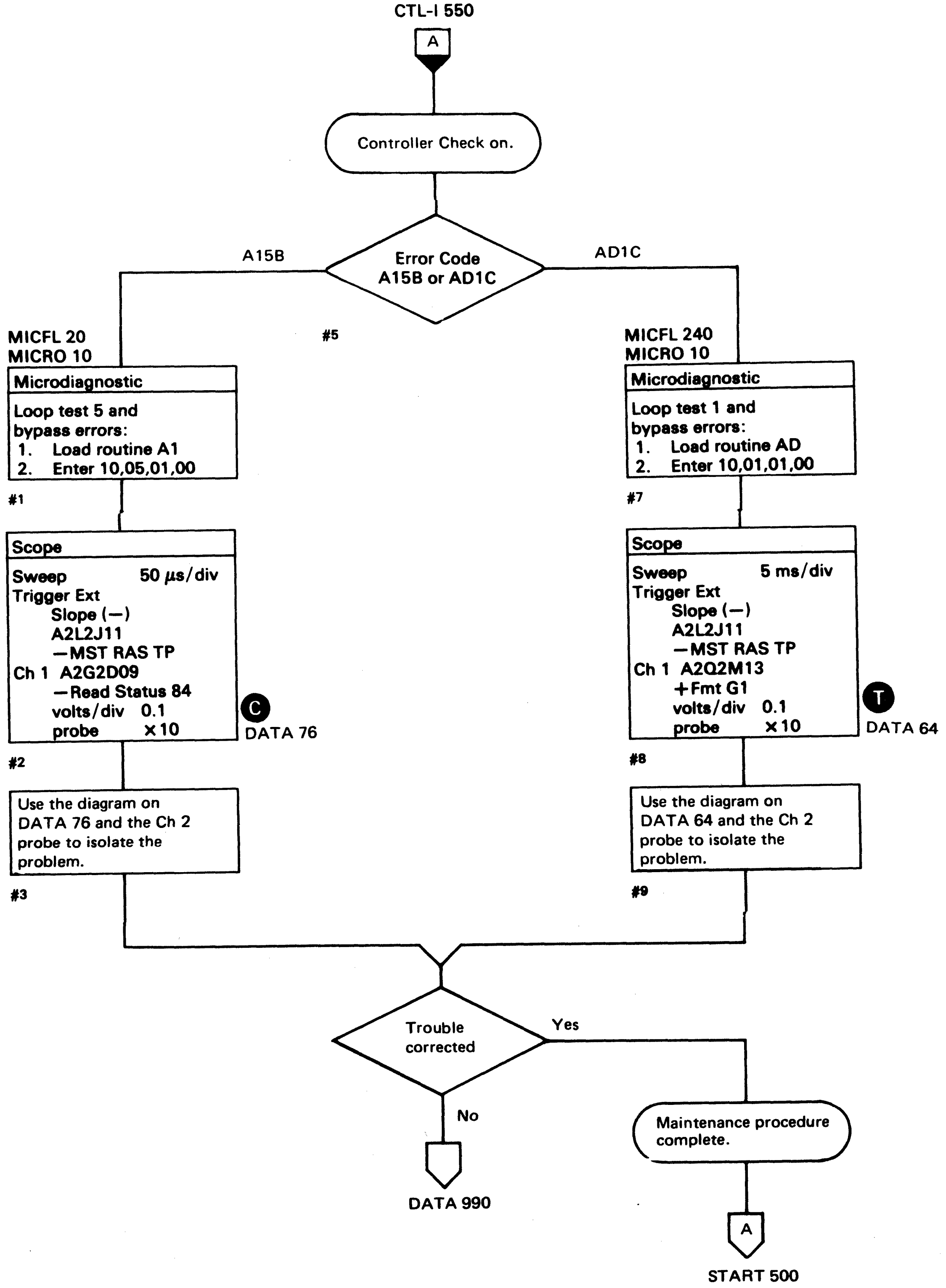
Routine AD, test 1 is the first of a series of tests that uses the controller in Write mode to test a variety of data handling functions. To prevent writing data on the disk, the Diagnostic Suppress Write command is used. The first function of routine AD, test 1 is to verify the operation of Diagnostic Suppress Write by activating the Write Gate at Index time for approximately 15 microseconds and to verify that an I Write Sense response is received. Suppress Write is then activated and Write Gate is activated again at the next Index time. No I Write Sense response indicates that Suppress Write functioned properly.

The test then uses Diagnostic Invert Bus Out Parity to force:

- Gap Counter Error
- Write Data Check
- Phase Error

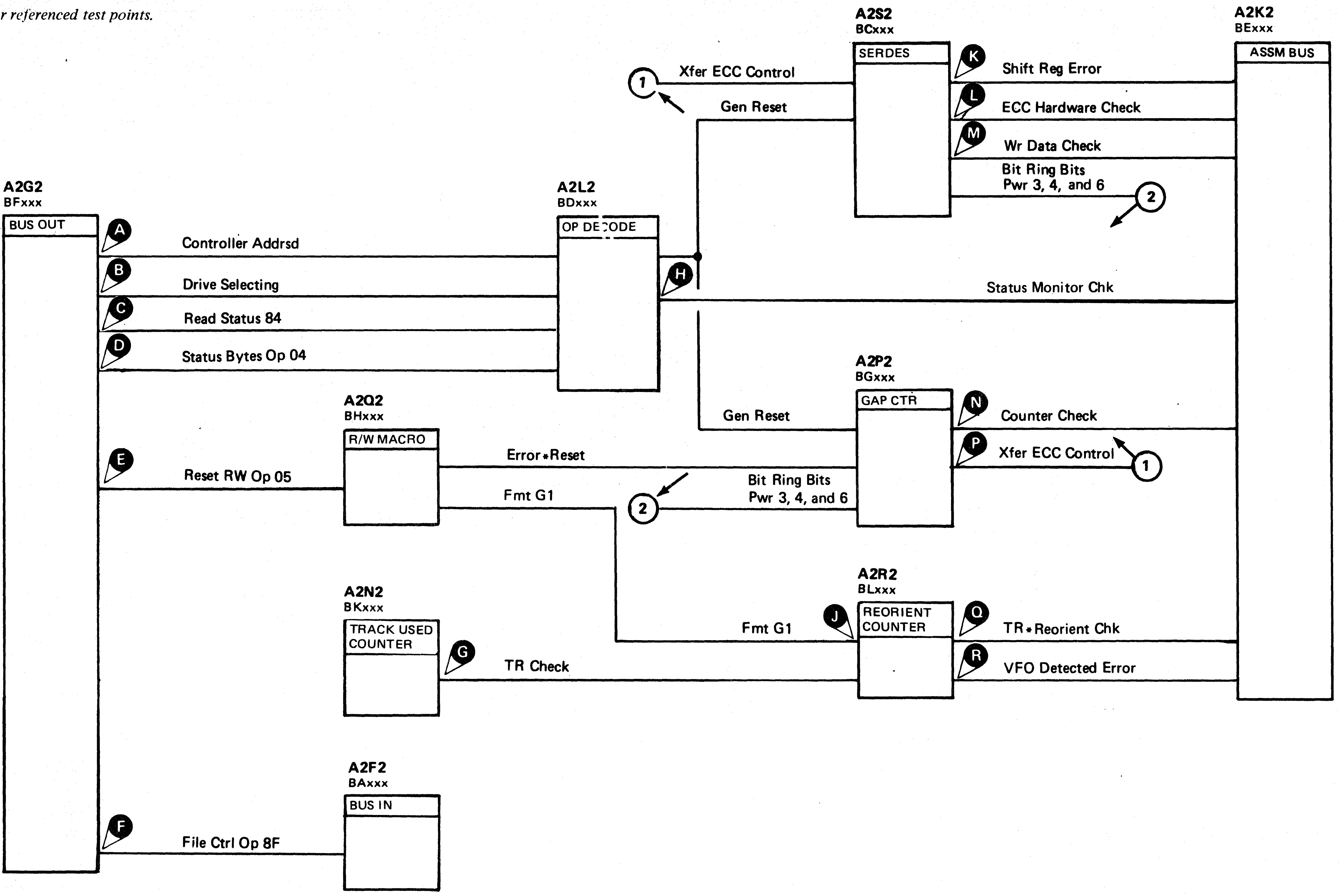
The test also verifies that a Controller Check follows the sensing of the error latches.





CONTROLLER CHECK

See the sequence charts on DATA 78 for referenced test points.
See OPER 241 for theory.



3350	CE0113 Seq. 2 of 2	2358489 Part No.	441300 31 Mar 76	441303 30 Jul 76			

CONTROLLER CHECK

TRIGGERING INSTRUCTIONS

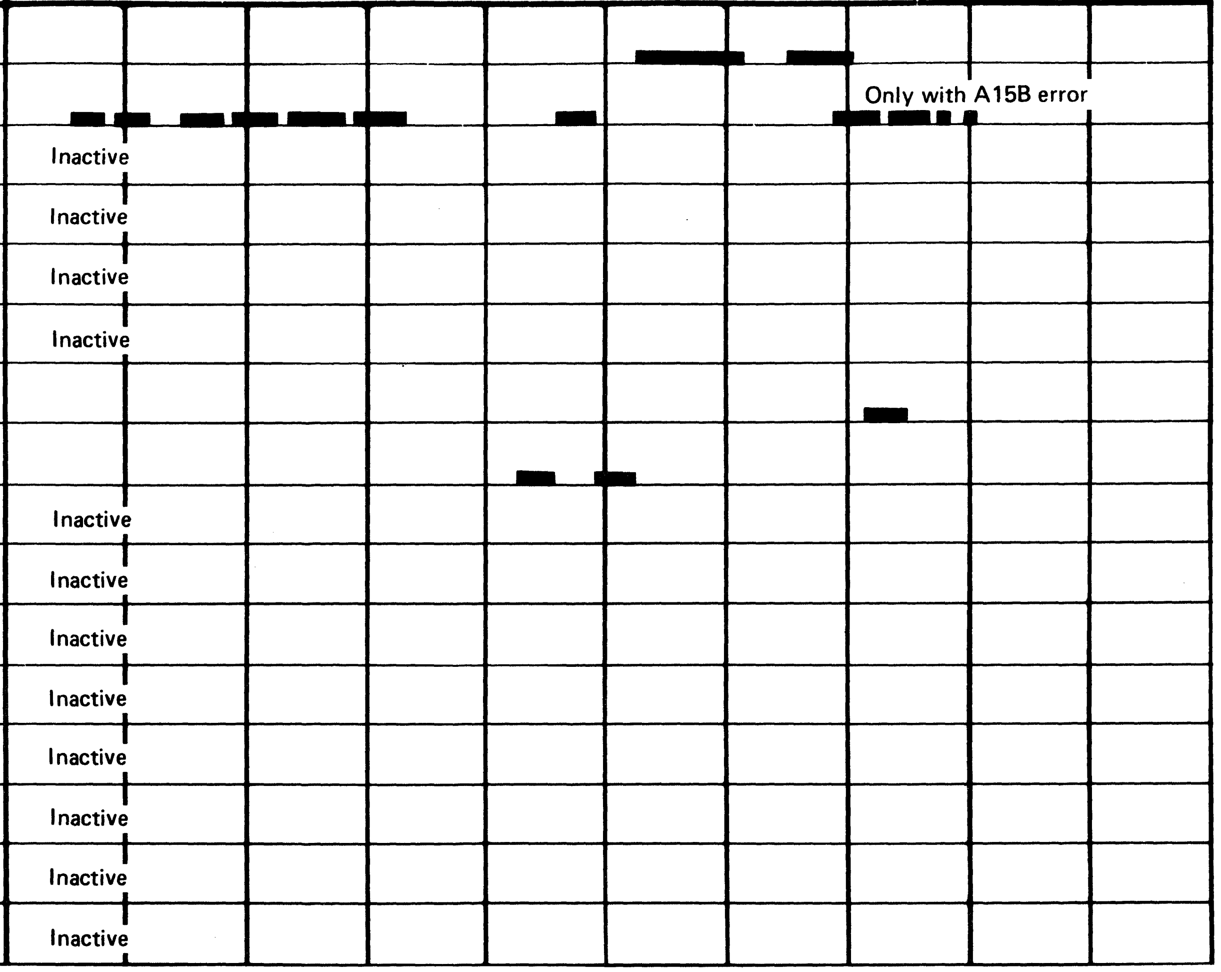
Scope Setup

Sweep 50 ns/div
Mode Alt or Chop
Trigger Ext
Slope (-)
A2L2J11
-MST RAS TP

Ch 1 A2G2D09
-Read Status 84
Volts/div 0.1
Probe X10
Ch 2 (See chart)

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	–Read Status 84	BF110	A2G2 D09	C
2	–Status Bytes Op 04	BF110	A2G2 G03	D
3	–VFO Detected Error	BL140	A2R2 G05	R
4	–TR * Reorient Chk	BL120	A2R2 J10	Q
5	+TR Check	BK140	A2N2 B10	G
6	+Fmt G1	BL130	A2R2 B12	J
7	–File Ctrl Op 8F	BF110	A2G2 D02	F
8	+Reset RW Op 05	BF110	A2G2 D05	E
9	–Controller Addrsd	BF120	A2G2 G04	A
10	–Drive Selecting	BF120	A2G2 S11	B
11	–Status Monitor Chk	BD160	A2L2 D09	H
12	–Shift Reg Error	BC110	A2S2 P02	K
13	–ECC Hardware Check	BC160	A2S2 S07	L
14	–Wr Data Check	BC130	A2S2 P06	M
15	–Xfer ECC Control	BG170	A2P2 J06	P
16	–Counter Check	BG160	A2P2 J09	R



Line keys reference the diagram on DATA 76.

TIMEOUT WAITING FOR RESPONSE FROM CONTROLLER

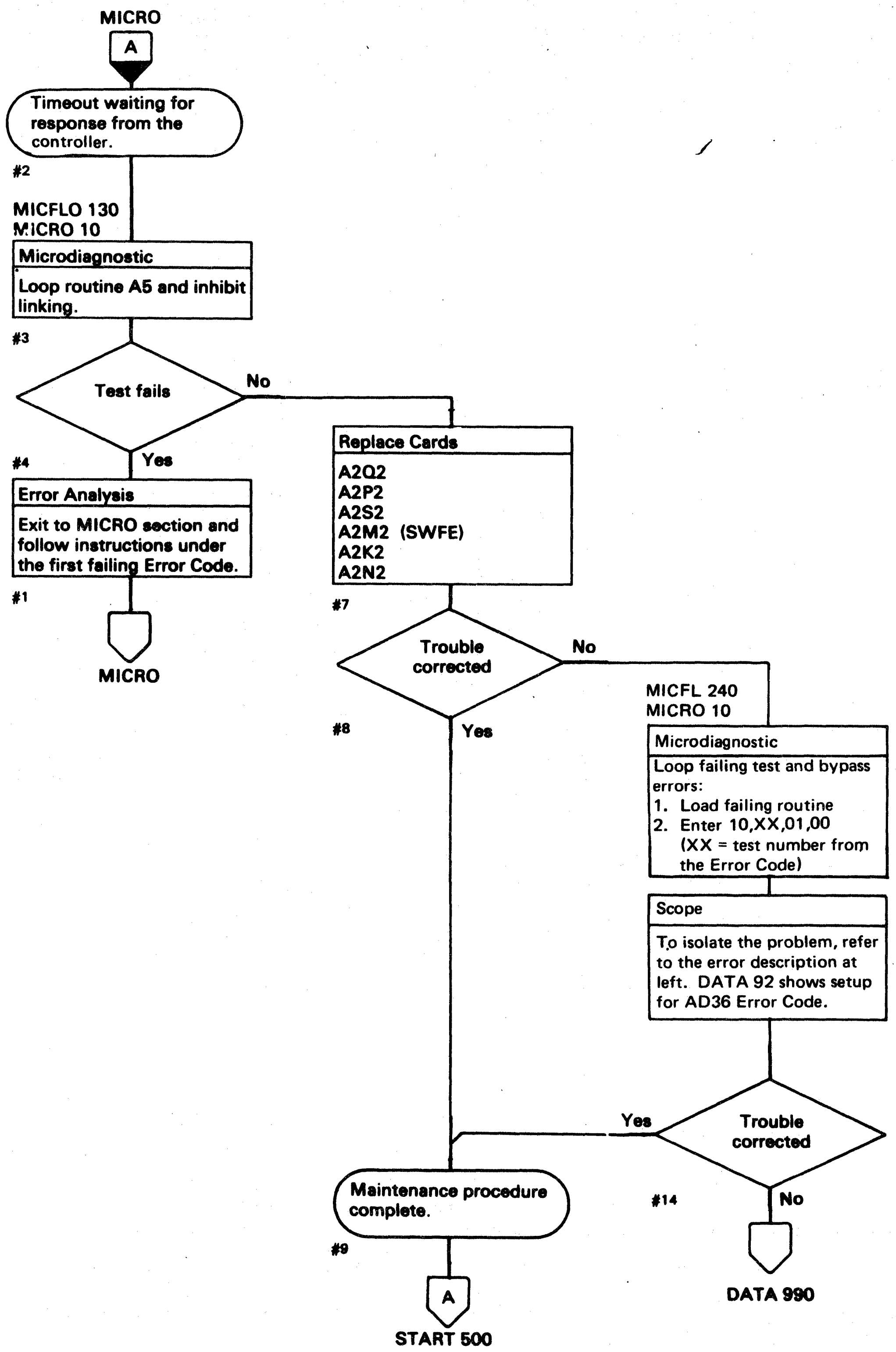
ERROR DESCRIPTION

Refer to the Sequence Chart below for the operation being performed when the timeout condition was encountered. The timeout condition usually results from a failure to decode the specific operation or from an early abnormal termination of the operation.

Sequence Chart

AD26	Fmt G1	
AD36	Wr Sp G1	
AD56	Wr G2	
AD66	Wr G3	
AD76	Fmt G1	
ADA5	Byte 4 = 1	Wr Sp G2 (1st record)
ADA5	Byte 4 = 2	Wr Sp G2 (2nd record)
ADA5	Byte 4 = 3	Wr G4
ADA5	Byte 4 = 4	Wr G2 (Extended Gap)
ADA5	Byte 4 = 5	Wr G2 (Normal Gap)
AEF3	Rd G1	

Loop the failing test and scope to isolate the problem. DATA 92 shows a scope setup for the AD36 Error Code.



GAP COUNTER OUT OF TOLERANCE

ERROR DESCRIPTION

The Gap Counter Tolerance test measures the duration of the various gaps. If the duration (time) is within 3 percent of normal, the Gap Counter is operating properly.

Out-of-tolerance indications point to troubles in:

- **Gap Counter or output decode.**
- **Bit Ring to the drive.**
- **A2P2 card that controls the Write operation.**

Sync In and other basic circuits must be operative to run this test.

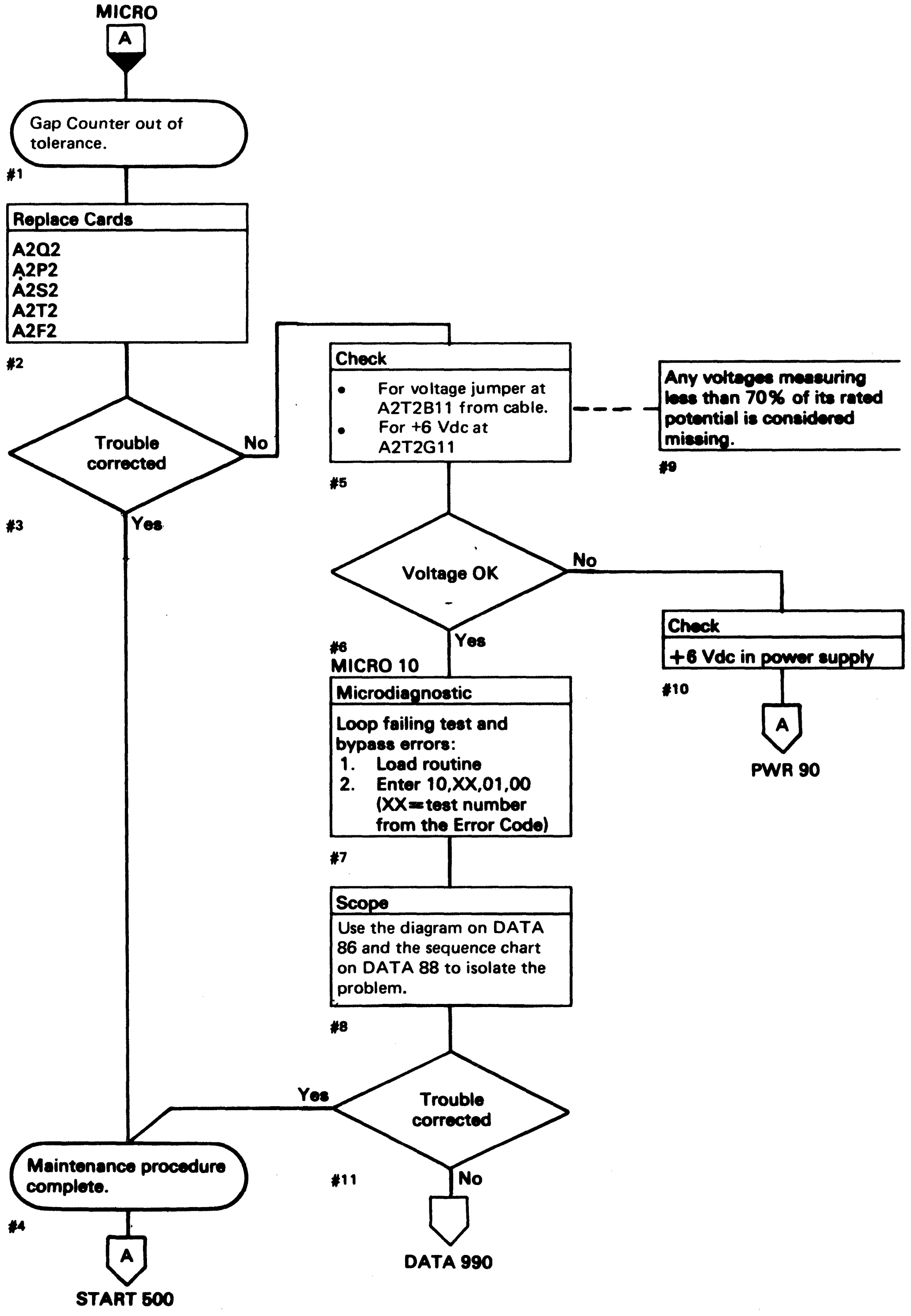
MICRODIAGNOSTIC DESCRIPTION

Routine AD, test 2 measures the duration of a G1 gap. When a Write G1 command is issued, the program measures the time from the Index (the start of a G1 gap) to the first Sync In pulse. The tolerance is 93 to 100 μsec. If the Sync In pulse is early or late, Test Error Number 28 is posted.

Routine AD, test 3 performs the same test on a Special Write G1 command which is used to skip a defect in the HA (Home Address) area. Test Error Number 38 indicates an out-of-tolerance condition (197 to 209 μsec).

Routine AD, test 5 measures the duration of a G2 gap by locating the end of an HA field and then issuing a Write G2 operation. The program measures the time from the end of the HA field to the first Sync In pulse for the G2 field. The tolerance is 60–64 μsec. If the Sync In pulse is early or late, Test Error Number 58 is posted.

Routine AD, test 6 measures the duration of a G3 gap by locating the end of an HA field and issuing a Write G3 operation. The program measures the time from the end of the HA field to the first Sync In pulse for the G3 field. The tolerance is 62 to 66 μsec. If the Sync In pulse is early or late, Test Error Number 68 is posted.

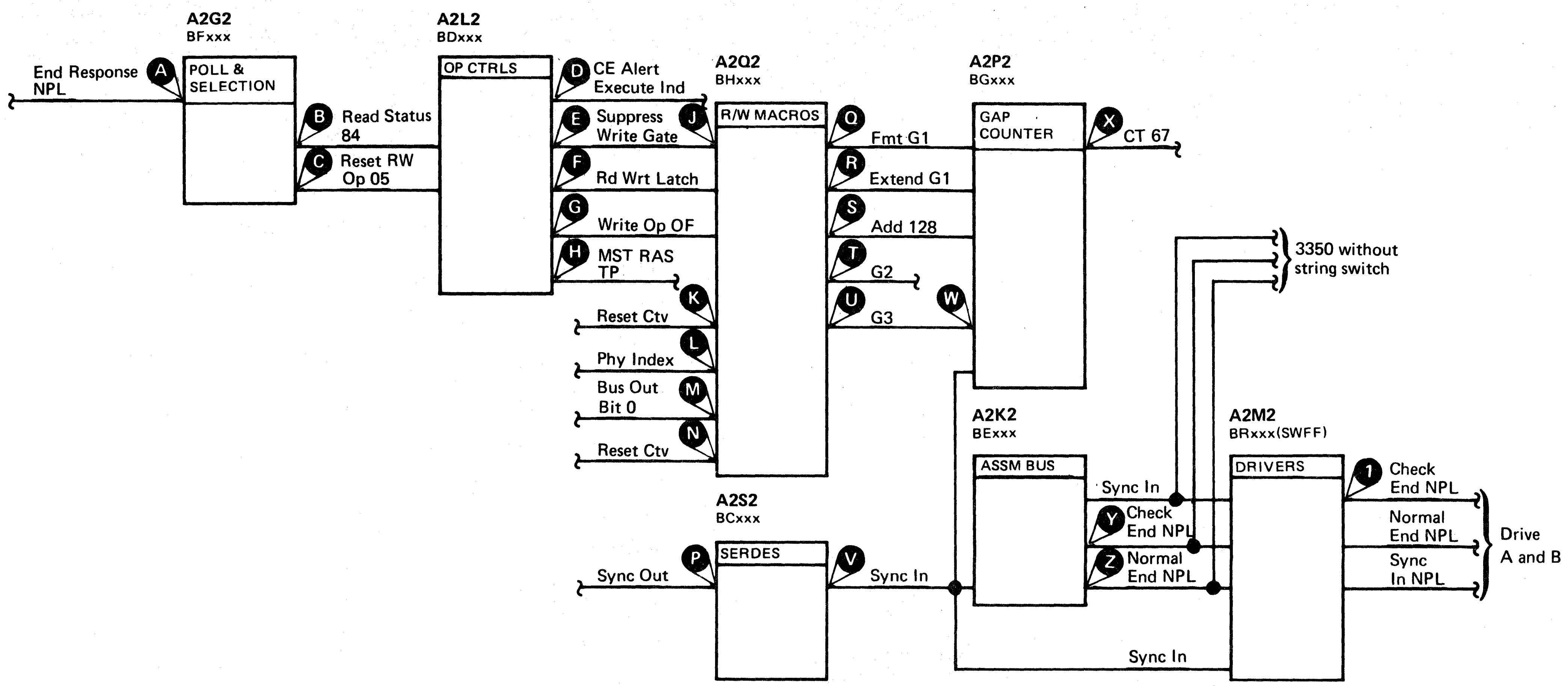


3350	CE0120 Seq. 1 of 2	2358491 Part No.	441300 31 Mar 76	441301 1 Jun 76	441303 30 Jul 76		

AD TEST 2 DIAGRAM

See the sequence chart on DATA 88 for referenced test points.

See OPER 6 for theory.



AD TEST 2 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

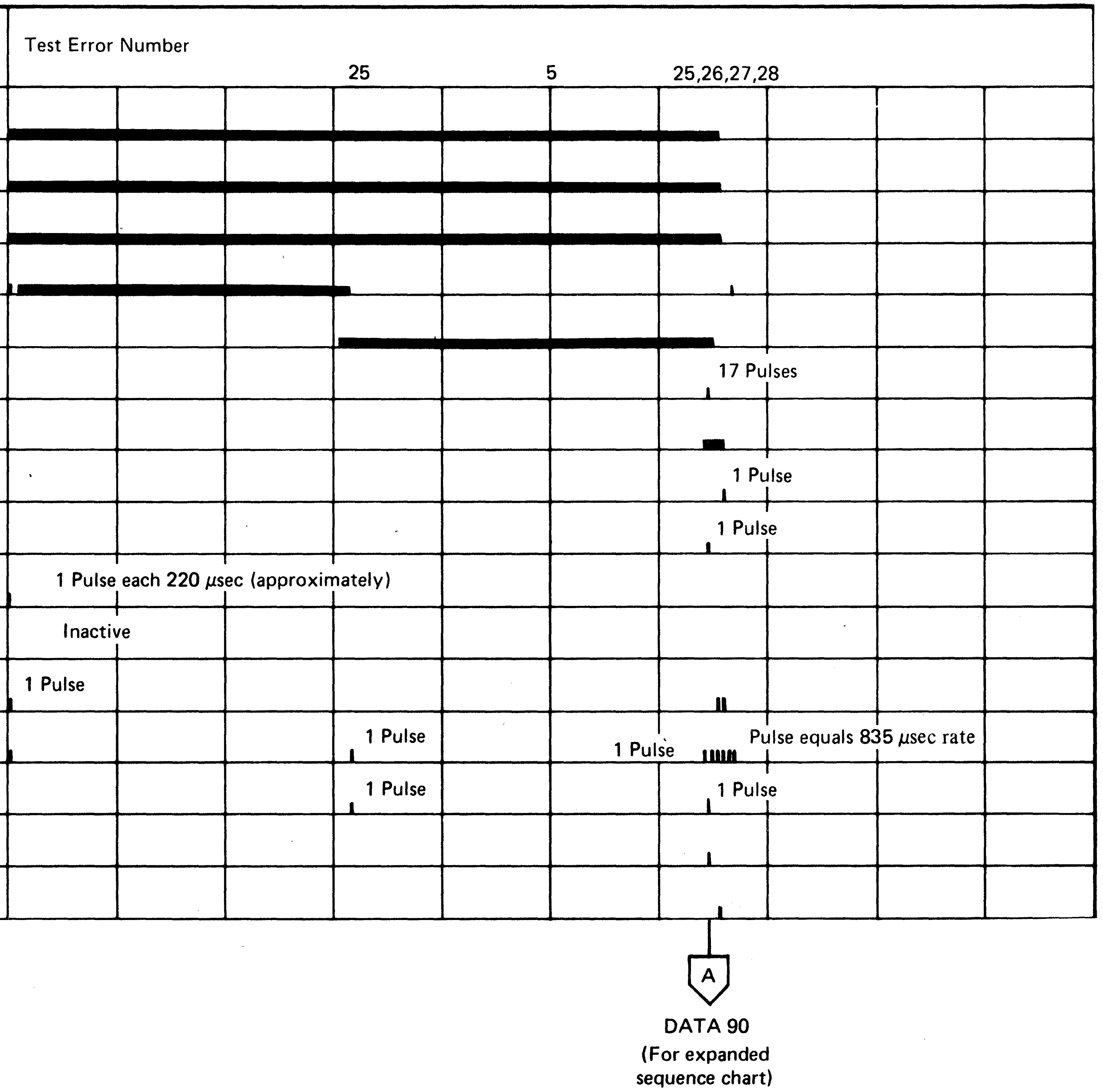
Routine AD, test 2
1. Load AD
2. Enter 10,02,00,00

Scope Setup

Sweep	5 ms/div	Ch 1	A2U4D13 +CE Alert Execute Ind
Mode	Alt or Chop		
Trigger	Ext	Volts/div	0.1
Slope (+)		Probe	x10
A2L2D13 +CE Alert Execute Ind		Ch 2 (See chart)	

Legend: ☐ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	D
2	+Suppress Write Gate	BD170	A2L2 G07	E
3	−Rd Wrt Latch	BD150	A2L2 J03	F
4	−Read Status 84	BF110	A2G2 D09	B
5	−Write Op 0F	BD100	A2L2 M04	G
6	−Sync In	BC170	A2S2 S10	V
7	−MST RAS TP	BD100	A2L2 J11	H
8	+Reset RW Op 05	BF110	A2G2 D05	C
9	+Fmt G1	BH140	A2Q2 M13	Q
10	−CT 67	BG130	A2P2 S05	X
11	−G3	BG140	A2P2 U04	W
12	−Bus Out Bit 0	BH100	A2Q2 B05	M
13	−Reset Ctr	BH150	A2Q2 U11	K
14	−Phy Index	BH170	A2Q2 S07	L
15	+Sync Out	BC170	A2S2 S12	P
16	+Check End NPL	BE160	A2K2 D05	I



Line keys reference the diagram on DATA 86.

AD TEST 2 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (–)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 4.0
Source – Int Ch 1

Ch 1 A2Q2S07
–Phy Index
Volts/div 0.1
Probe x10
Ch 2 (See chart)

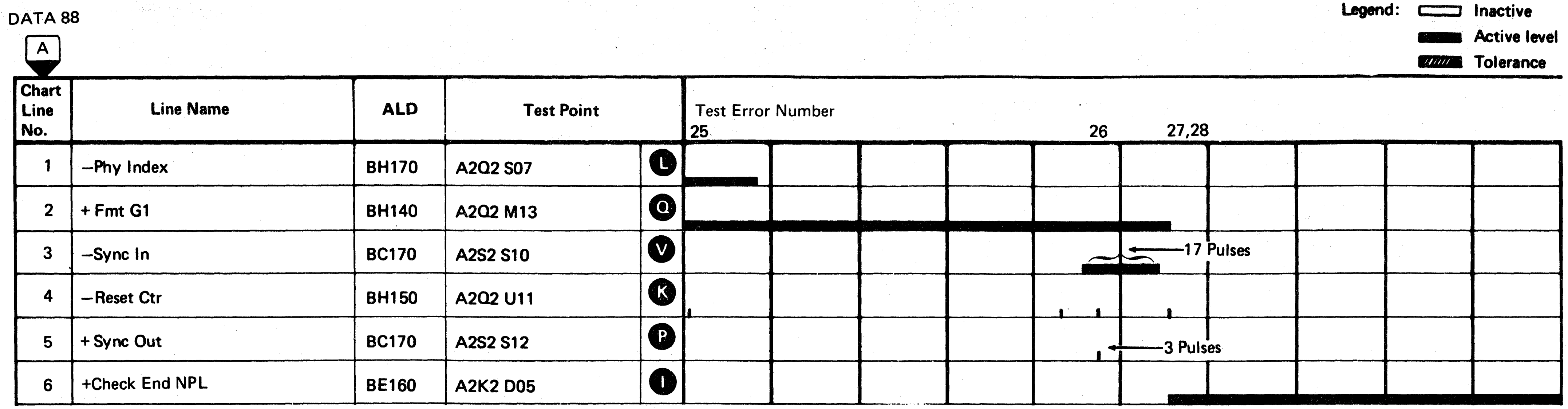


Chart Line No.	Line Name	ALD	Test Point	
1	–Phy Index	BH170	A2Q2 S07	L
2	+ Fmt G1	BH140	A2Q2 M13	Q
3	–Sync In	BC170	A2S2 S10	V
4	–Reset Ctr	BH150	A2Q2 U11	K
5	+ Sync Out	BC170	A2S2 S12	P
6	+Check End NPL	BE160	A2K2 D05	I

Line keys reference the diagram on DATA 86.

CE0123 Seq. 2 of 2	2358492 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AD TEST 3 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AD, test 3
1. Load AD
2. Enter 10,03,00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop

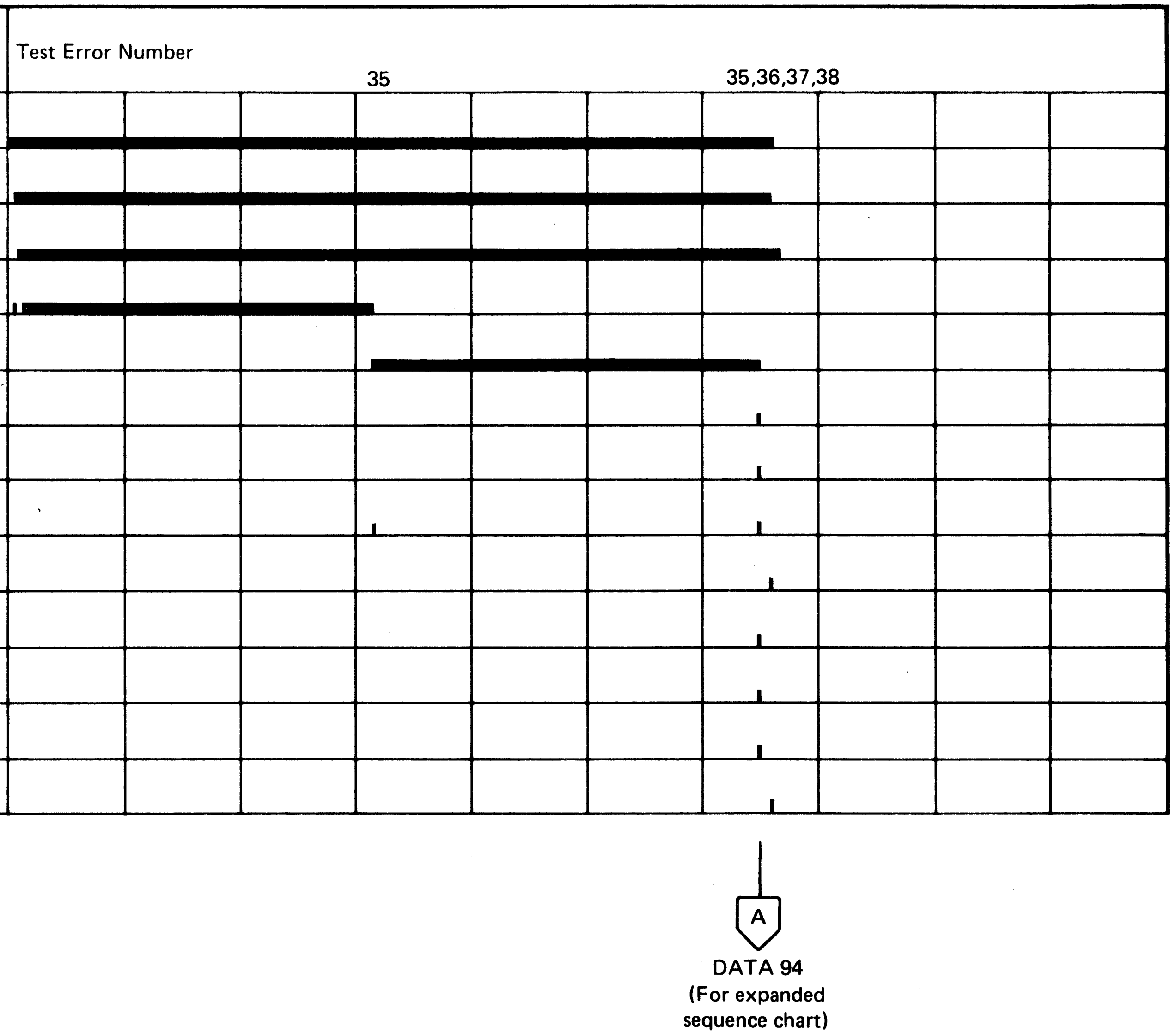
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	D
2	+Suppress Write Gate	BD170	A2L2 G07	E
3	−Rd Wrt Latch	BD150	A2L2 J03	F
4	−Read Status 84	BF110	A2G2 D09	B
5	−Wrt Op 0F	BD100	A2L2 M04	G
6	−Sync In	BC170	A2S2 S10	V
7	+Sync Out	BC170	A2S2 S12	P
8	−Phy Index	BH170	A2G2 D05	L
9	+Reset RW Op 05	BF110	A2G2 005	C
10	+Fmt G1	BH140	A2Q2 M13	Q
11	+Extend G1	BH160	A2Q2 J03	R
12	+Add 128	BH160	A2Q2 P13	S
13	+Check End NPL	BE160	A2K2 D05	I



Line keys reference the diagram on DATA 86.

AD TEST 3 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep	5 ms/div	Ch 1 A2Q2D07	
Mode	Alt or Chop	–Phy Index	
Trigger	Ext	Volts/div	0.1
	Slope (+)	Probe	x10
	A2L2D13	Ch 2 (See chart)	
	+CE Alert Execute Ind		

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (–)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 4.0
Source – Int Ch 1

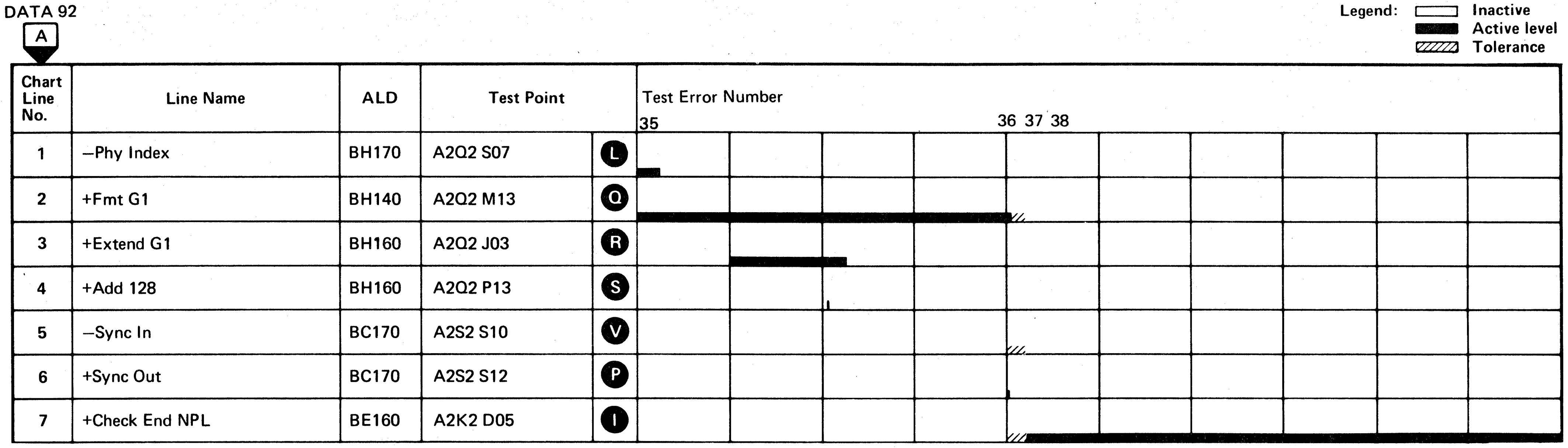


Chart Line No.	Line Name	ALD	Test Point	
1	–Phy Index	BH170	A2Q2 S07	L
2	+Fmt G1	BH140	A2Q2 M13	Q
3	+Extend G1	BH160	A2Q2 J03	R
4	+Add 128	BH160	A2Q2 P13	S
5	–Sync In	BC170	A2S2 S10	V
6	+Sync Out	BC170	A2S2 S12	P
7	+Check End NPL	BE160	A2K2 D05	I

Line keys reference the diagram on DATA 86.

3350	CE0125 Seq. 2 of 2	2358493 Part No.	441300 31 Mar 76	441303 31 Jul 76			

AD TEST 5 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AD, test 5
1. Load AD
2. Enter 10,05,00,00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop

Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend: ▭ Inactive ■ Active level ▨ Tolerance

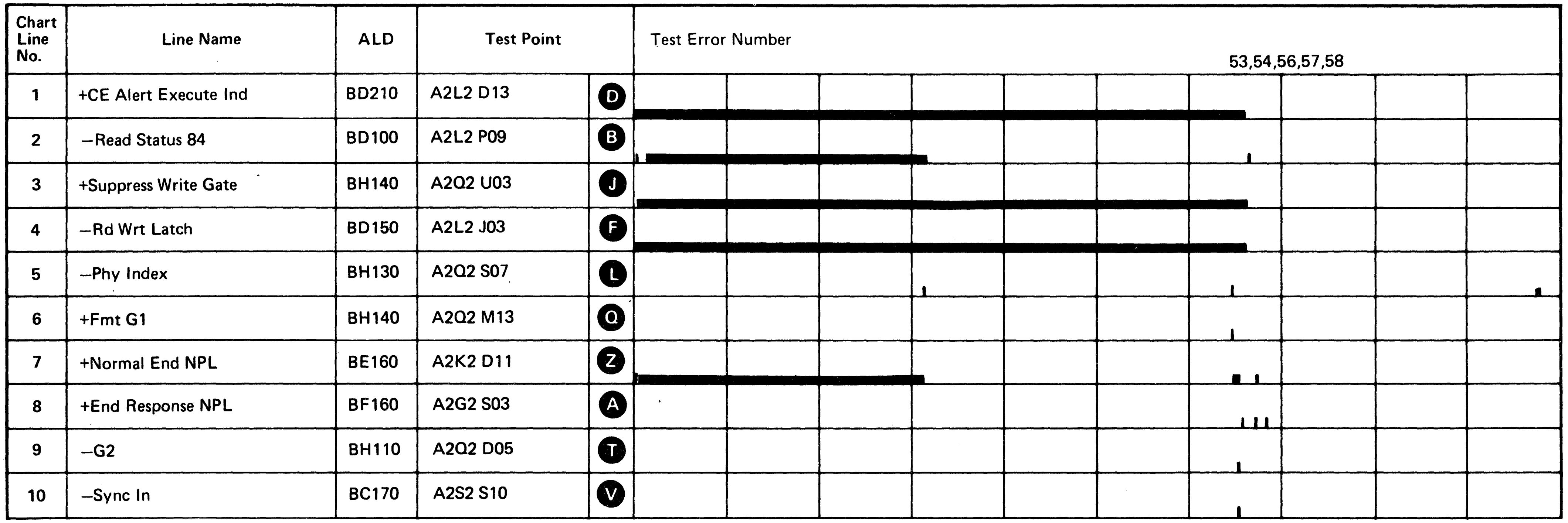


Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	D
2	−Read Status 84	BD100	A2L2 P09	B
3	+Suppress Write Gate	BH140	A2Q2 U03	J
4	−Rd Wrt Latch	BD150	A2L2 J03	F
5	−Phy Index	BH130	A2Q2 S07	L
6	+Fmt G1	BH140	A2Q2 M13	Q
7	+Normal End NPL	BE160	A2K2 D11	Z
8	+End Response NPL	BF160	A2G2 S03	A
9	−G2	BH110	A2Q2 D05	T
10	−Sync In	BC170	A2S2 S10	V

Line keys reference the diagram on DATA 86.

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2M13
+Fmt G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 4.0
Source – Int Ch 1

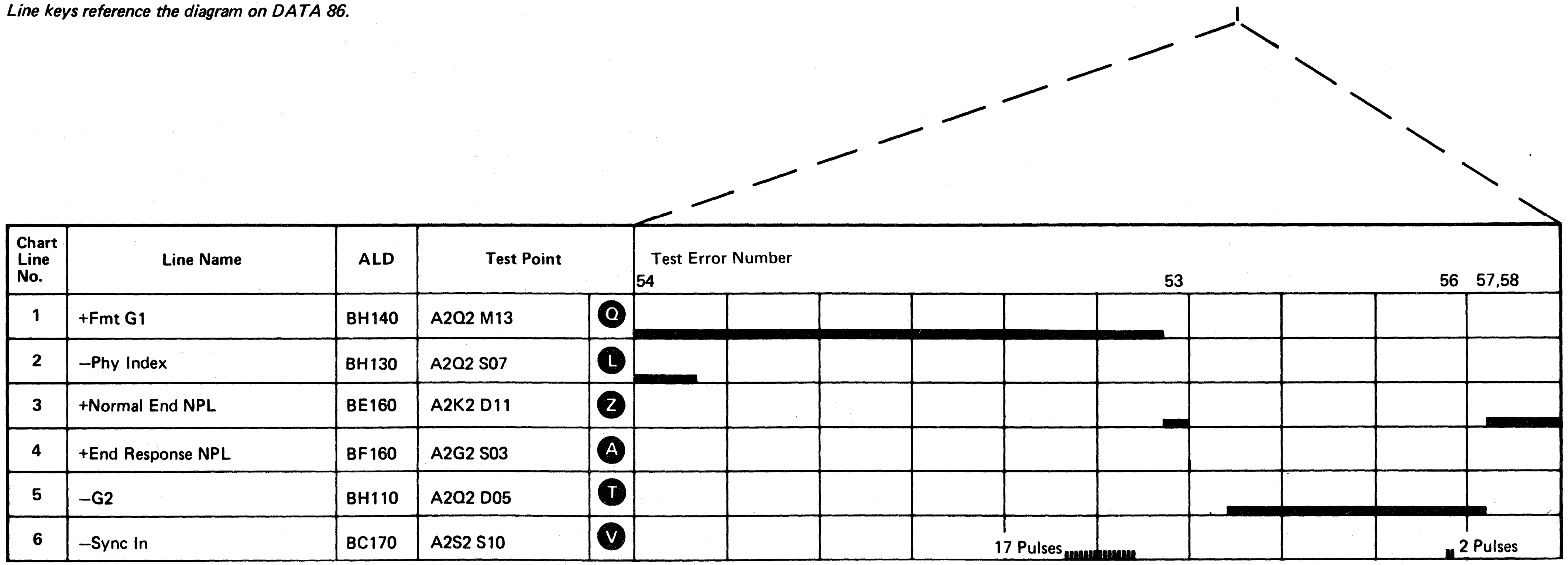


Chart Line No.	Line Name	ALD	Test Point	
1	+Fmt G1	BH140	A2Q2 M13	Q
2	−Phy Index	BH130	A2Q2 S07	L
3	+Normal End NPL	BE160	A2K2 D11	Z
4	+End Response NPL	BF160	A2G2 S03	A
5	−G2	BH110	A2Q2 D05	T
6	−Sync In	BC170	A2S2 S10	V

Line keys reference the diagram on DATA 86.

CE0127 Seq. 1 of 2	2358494 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AD TEST 6 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AD, test 6
1. Load AD
2. Enter 10,06,00,00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop

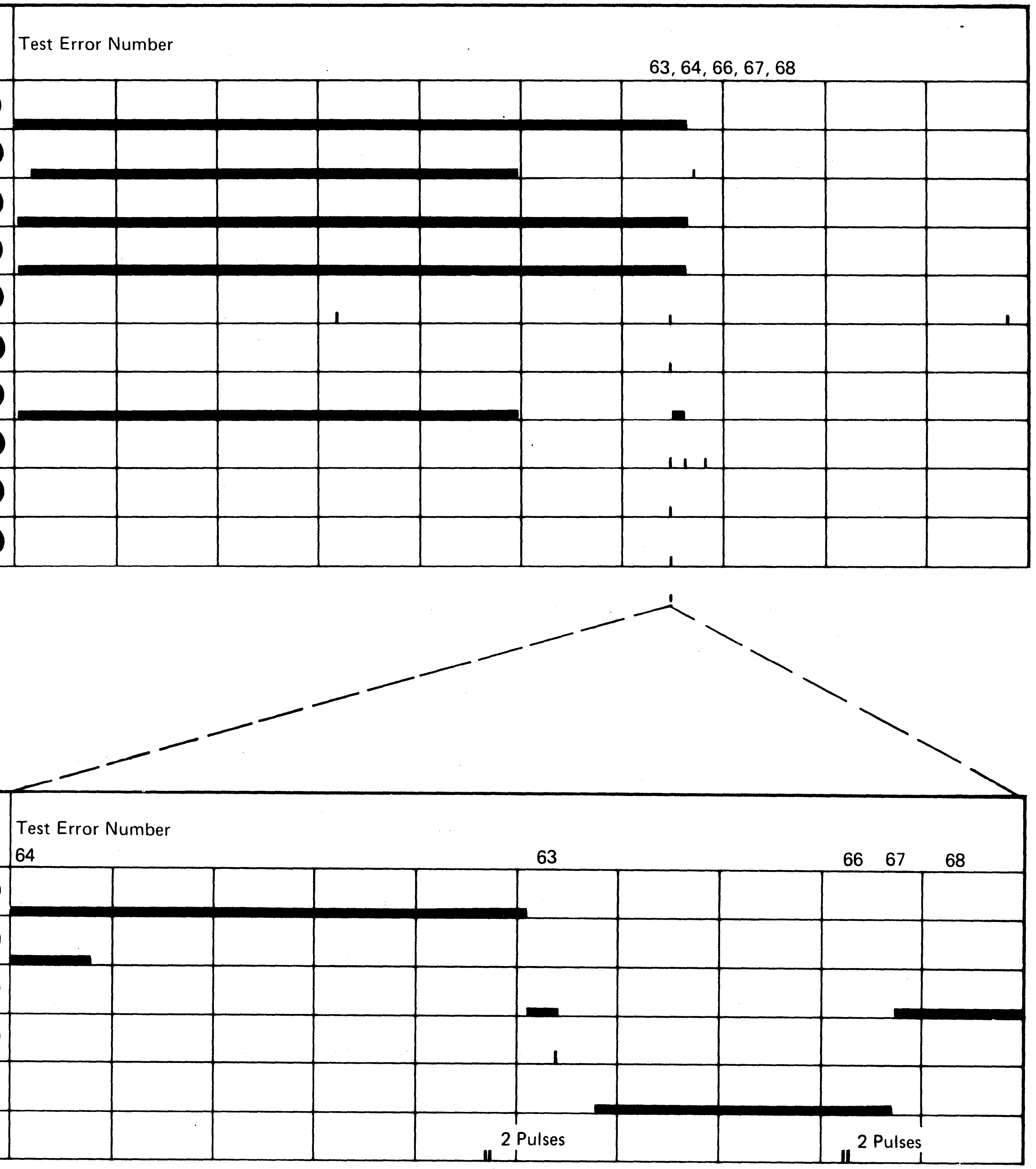
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	D
2	–Read Status 84	BD100	A2L2 P09	B
3	+Suppress Write Gate	BH140	A2Q2 U03	J
4	–Rd Wrt Latch	BD150	A2L2 J03	F
5	–Phy Index	BH130	A2Q2 S07	L
6	+Fmt G1	BH140	A2Q2 M13	Q
7	+Normal End NPL	BE160	A2K2 D11	Z
8	+End Response NPL	BF160	A2G2 S03	A
9	–G3	BH110	A2Q2 D02	U
10	–Sync In	BC170	A2S2 S10	V

Line keys reference the diagram on DATA 86.



TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 4.0
Source – Int Ch 1

Ch 1 A2Q2M13
+Fmt G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Chart Line No.	Line Name	ALD	Test Point	
1	+Fmt G1	BH140	A2Q2 M13	Q
2	–Phy Index	BH130	A2Q2 S07	L
3	+Normal End NPL	BE160	A2K2 D11	Z
4	+End Response NPL	BF160	A2G2 S03	A
5	–G3	BH110	A2Q2 D02	U
6	–Sync In	BC170	A2S2 S10	V

Line keys reference the diagram on DATA 86.

RECYCLE LINE FAILURE

ERROR DESCRIPTION

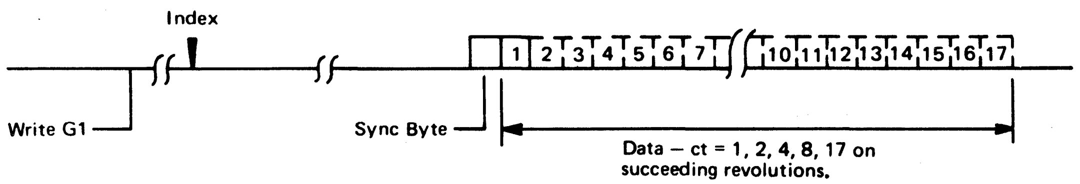
The Recycle line, in conjunction with the counter in Modulo-16 mode, determines when the interface operations are terminated. The Recycle line is activated by storage control to signal that more than 16 byte-times of interface operation are required. The Recycle line is de-activated when less than 8 byte-times remain. If less than 16 byte-times are required, Recycle is not activated.

The counter equal to 15 and the Recycle line inactive sets the End Data latch, which in turn starts an ending sequence in the controller. A premature or delayed ending may indicate a Recycle line failure.

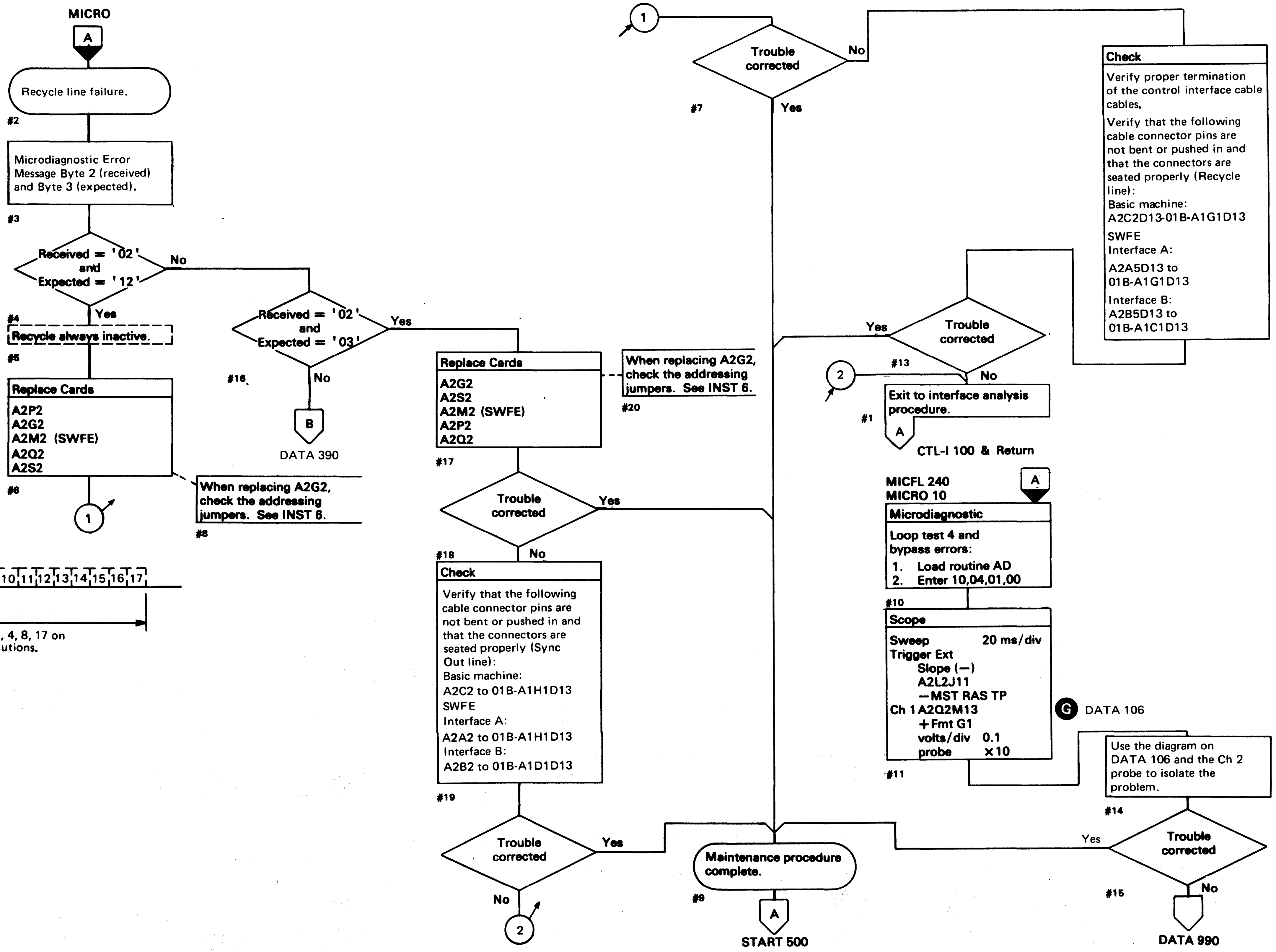
MICRODIAGNOSTIC DESCRIPTION

Routine AD, test 4 tests the Modulo-16 portion of the Gap Counter. During data handling operations, it is vital that the operation be precisely terminated. To accomplish this, the Modulo-16 counter is primed at the start of the operation with a number that is used to determine the end of the operation.

Test 4 verifies that each bit position of the Modulo-16 counter can be set to both states (on and off). Values of 1, 2, 4, 8, and 17 are used. The number of Sync In pulses are an indication of the Modulo-16 Counter operation. For example, when the counter is set to 1, two Sync In pulses are expected, for a count of 2, three pulses are expected, etc.



AD48 is the primary error stop for this test; it indicates an attempt to transfer an incorrect number of bytes.



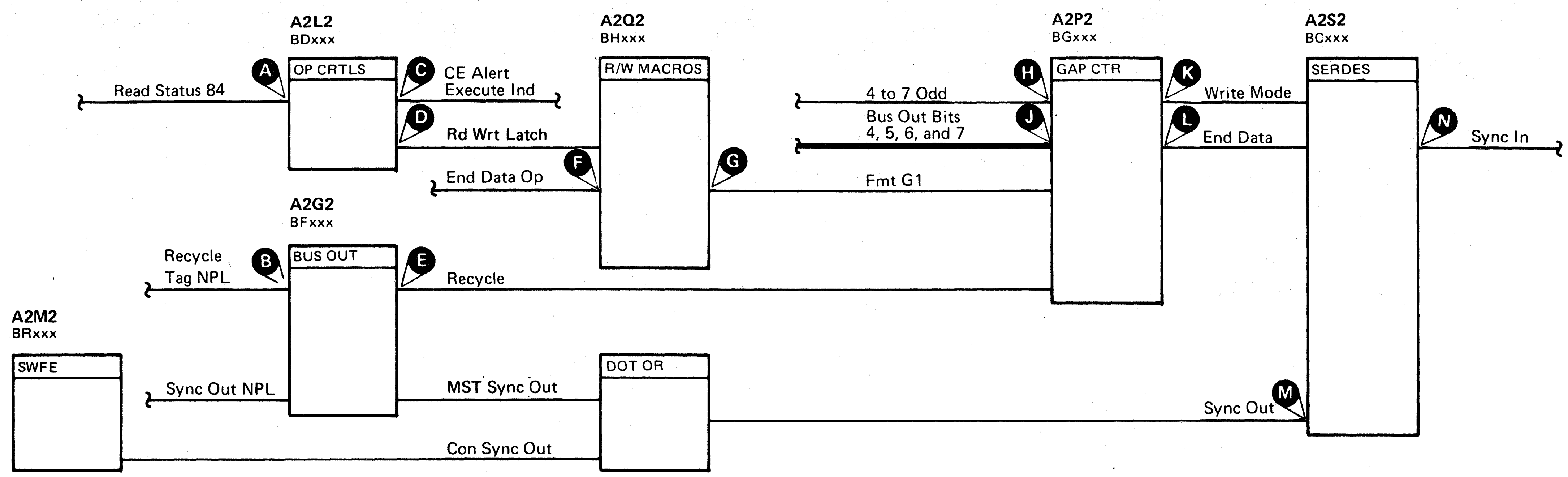
3350

CE0130 Seq. 1 of 2	2358495 Part No.

441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77		

AD TEST 4 DIAGRAM

See the sequence chart on DATA 108 for referenced test points.
See OPER 90 for theory.



3350

CE0130 Seq. 2 of 2	2358495 Part No.

441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77		

AD TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AD, test 4
1. Load AD
2. Enter 10,04,01,00

Scope Setup

Sweep 20 ms/div
Mode Alt or Chop

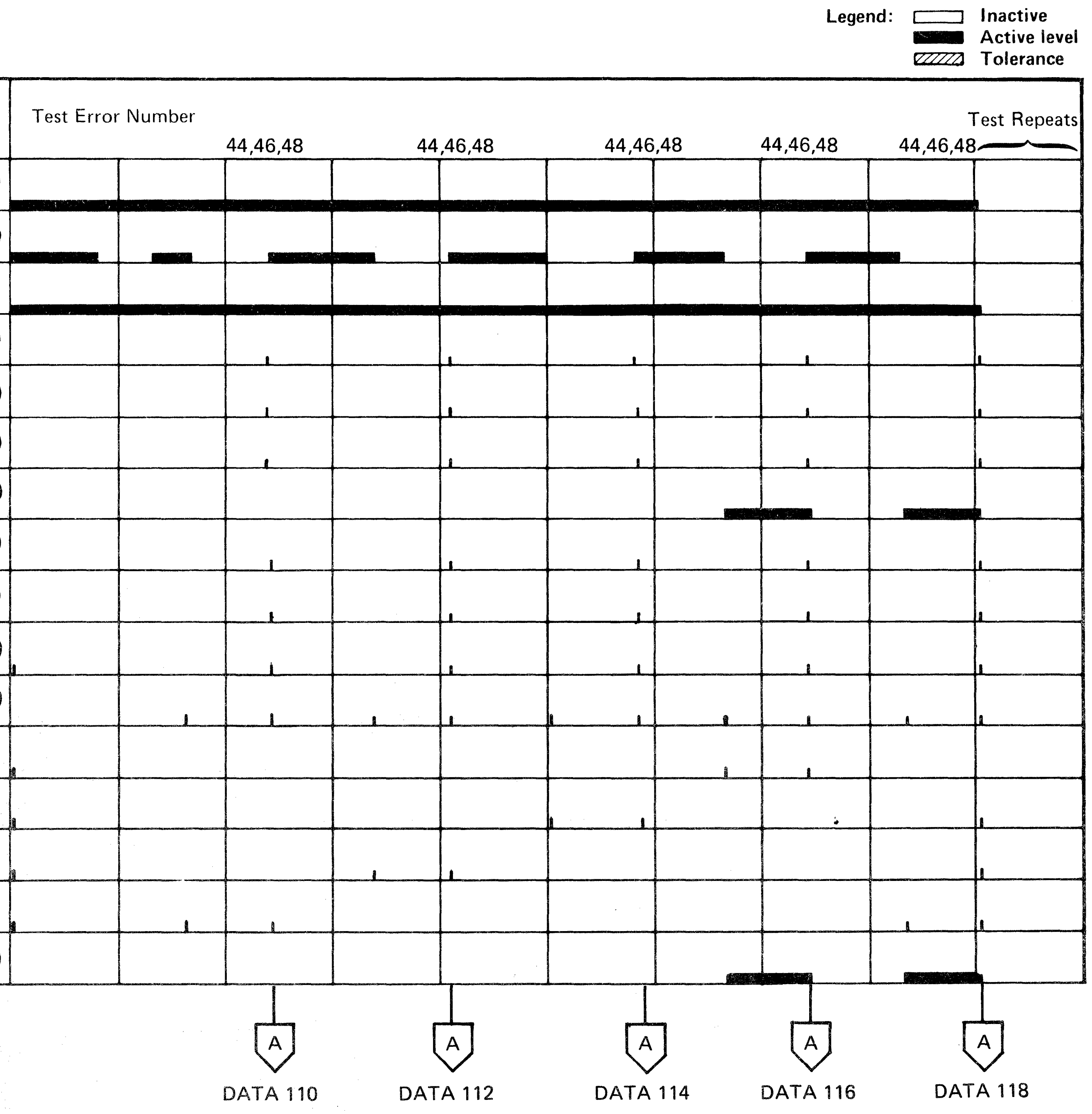
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	C
2	–Read Status 84	BD100	A2L2 P09	A
3	–Rd Wrt Latch	BD150	A2L2 J03	D
4	+Fmt G1	BH140	A2Q2 M13	G
5	–Sync In	BC170	A2S2 S10	N
6	–Write Mode	BG140	A2P2 M10	K
7	+Recycle	BF160	A2G2 S10	E
8	+Sync Out	BC170	A2S2 S12	M
9	+End Data	BG170	A2P2 G02	L
10	–End Data Op	BG170	A2Q2 G08	F
11	–4 to 7 Odd	BG100	A2P2 P05	H
12	–Bus Out Bit 4	BG100	A2P2 S10	J
13	–Bus Out Bit 5	BG100	A2P2 U11	
14	–Bus Out Bit 6	BG100	A2P2 S12	
15	–Bus Out Bit 7	BG100	A2P2 S13	
16	+Recycle Tag NPL	BF160	A2G2 U12	B

Line keys reference the diagram on DATA 106.



(For expanded sequence chart)

CE0137 Seq. 1 of 2	2358496 Part No.

441300 31 Mar 76	441303 30 Jul 76	441308 18 Aug 78		

AD TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 20 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

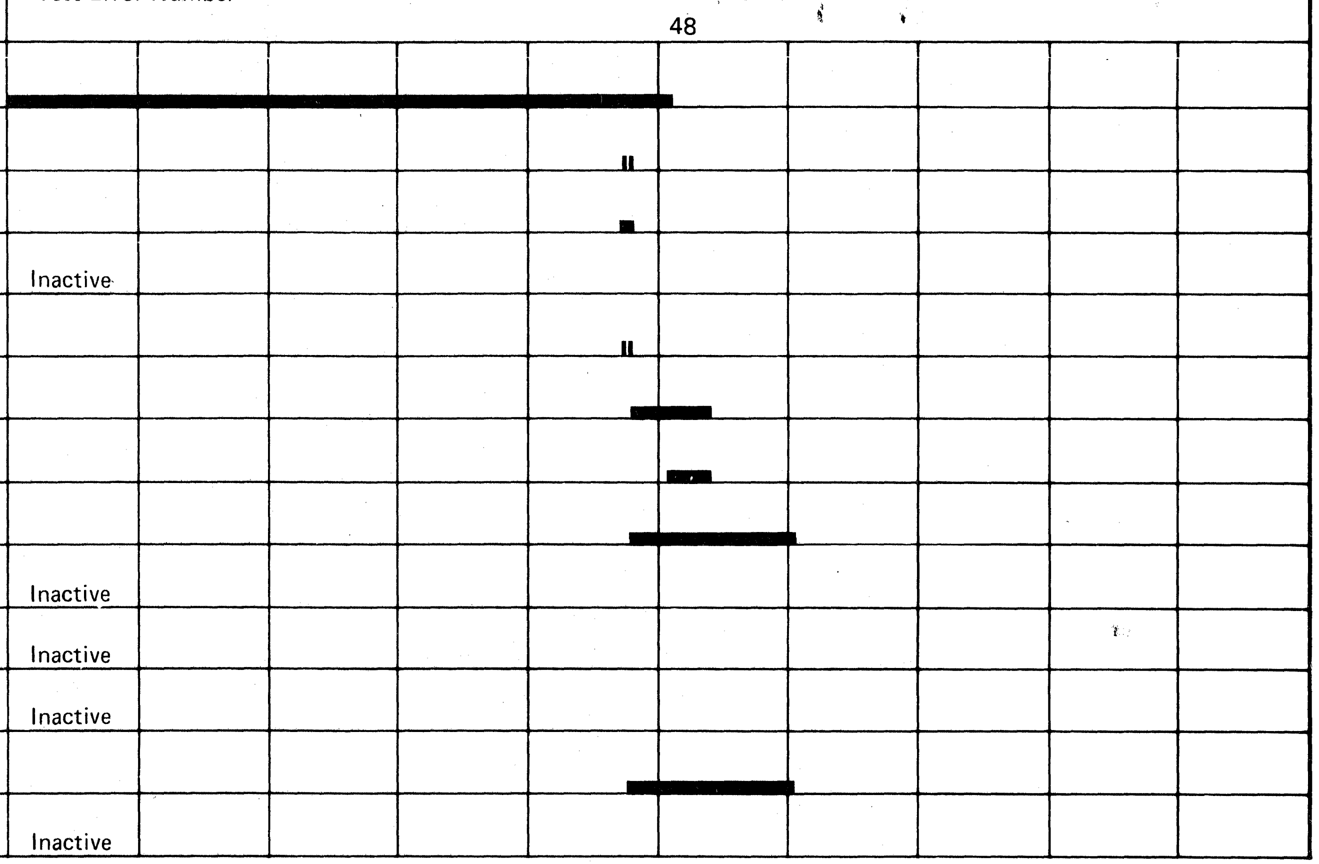
Ch 1 A2Q2M13
+Fmt G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 20 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

DATA 108
Ⓐ

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+Fmt G1	BH140	A2Q2 M13	G	
2	–Sync In	BC170	A2S2 S10	N	
3	–Write Mode	BG140	A2P2 M10	K	
4	+Recycle	BF160	A2G2 S10	E	Inactive
5	+Sync Out	BC170	A2S2 S12	M	
6	+End Data	BG170	A2P2 G02	L	
7	–End Data Op	BG170	A2Q2 G08	F	
8	–4 to 7 Odd	BG100	A2P2 P05	H	
9	–Bus Out Bit 4	BG100	A2P2 S10	J	Inactive
10	–Bus Out Bit 5	BG100	A2P2 U11		Inactive
11	–Bus Out Bit 6	BG100	A2P2 S12		Inactive
12	–Bus Out Bit 7	BG100	A2P2 S13		
13	+Recycle Tag NPL	BF160	A2G2 U12	B	Inactive



Line keys reference the diagram on DATA 106.

CE0137 Seq. 2 of 2	2358496 Part No.	441300 31 Mar 76	441303 30 Jul 76	441308 18 Aug 78		

AD TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 20 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

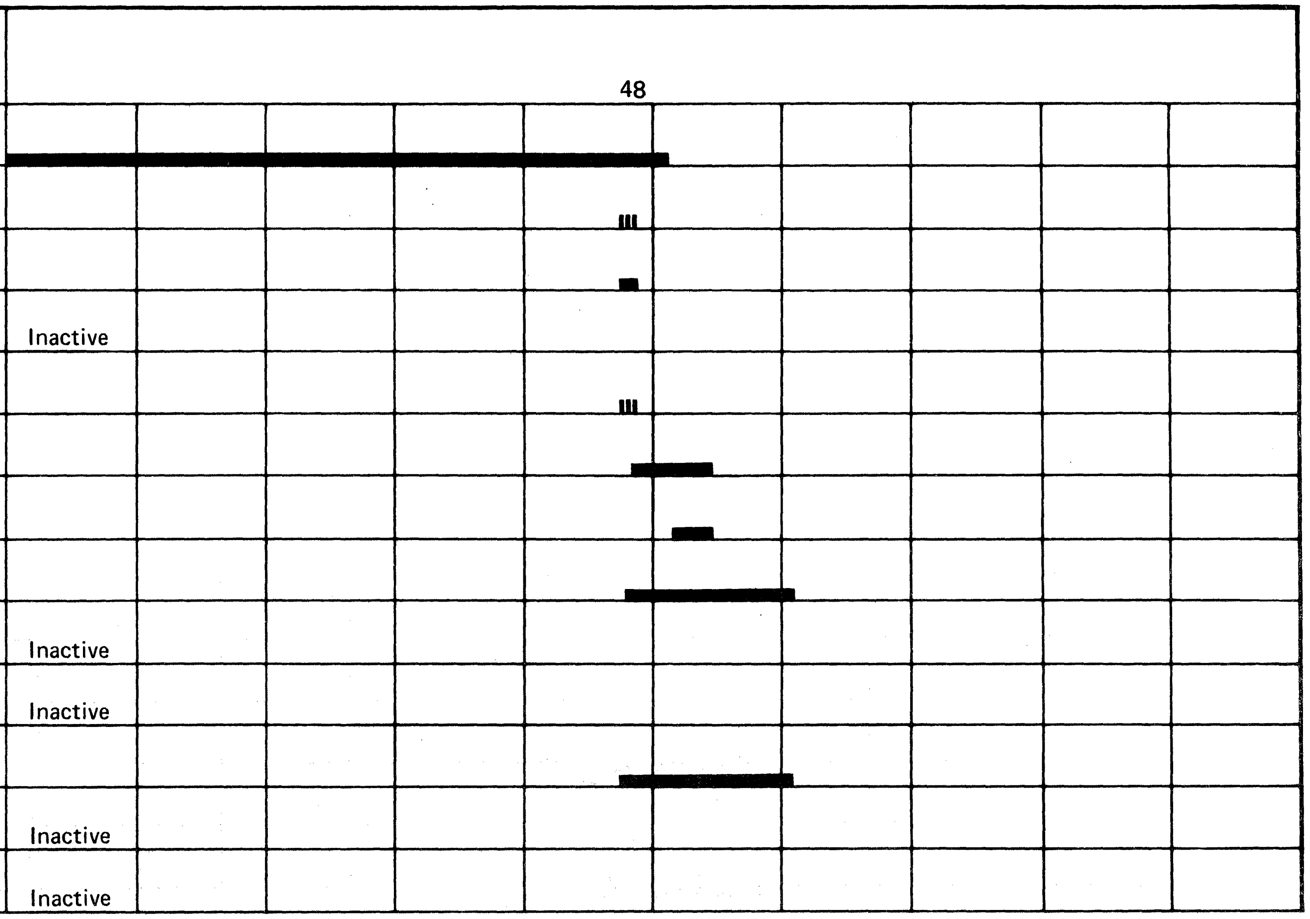
Ch 1 A2Q2M13
+Fmt G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 20 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 2.5
Source – Int Ch 1

DATA 108
A

Legend:
▭ Inactive
▬ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+Fmt G1	BH140	A2Q2 M13	G
2	–Sync In	BC170	A2S2 S10	N
3	–Write Mode	BG140	A2P2 M10	K
4	+Recycle	BF160	A2G2 S10	E
5	+Sync Out	BC170	A2S2 S12	M
6	+End Data	BG170	A2P2 G02	L
7	–End Data Op	BG170	A2Q2 G08	F
8	–4 to 7 Odd	BG100	A2P2 P05	H
9	–Bus Out Bit 4	BG100	A2P2 S10	J
10	–Bus Out Bit 5	BG100	A2P2 U11	↓
11	–Bus Out Bit 6	BG100	A2P2 S12	↓
12	–Bus Out Bit 7	BG100	A2P2 S13	↓
13	+Recycle Tag NPL	BG160	A2G2 U12	B



Line keys reference the diagram on DATA 106.

3350	CE0142 Seq. 1 of 2	2358497 Part No.	441300 31 Mar 76	441303 30 Jul 76	441308 18 Aug 78		

AD TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 20 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

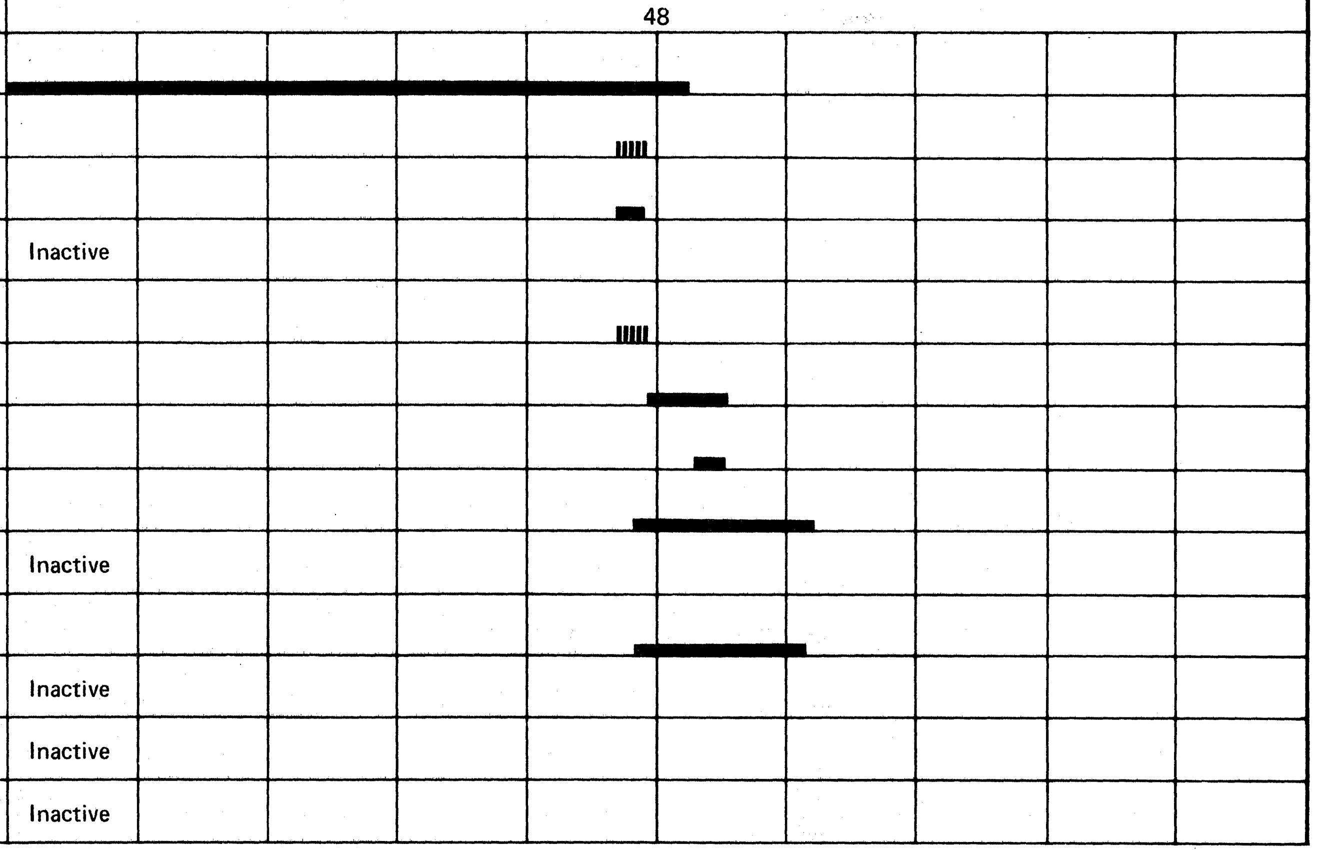
Ch 1 A2Q2M13
+Fmt G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 20 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 4.5
Source – Int Ch 1

DATA 108
A

Legend: ☐ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 48
1	+Fmt G1	BH140	A2Q2 M13	Ⓖ	
2	–Sync In	BC170	A2S2 S10	Ⓝ	
3	–Write Mode	BG140	A2P2 M10	Ⓚ	
4	+Recycle	BF160	A2G2 S10	Ⓔ	Inactive
5	+Sync Out	BC170	A2S2 S12	Ⓜ	
6	+End Data	BG170	A2P2 G02	Ⓛ	
7	–End Data Op	BG170	A2Q2 G08	Ⓕ	
8	–4 to 7 Odd	BG100	A2P2 P05	Ⓗ	
9	–Bus Out Bit 4	BG100	A2P2 S10	Ⓙ	Inactive
10	–Bus Out Bit 5	BG100	A2P2 U11		
11	–Bus Out Bit 6	BG100	A2P2 S12		Inactive
12	–Bus Out Bit 7	BG100	A2P2 S13		Inactive
13	+Recycle Tag NPL	BF160	A2G2 U12	Ⓑ	Inactive



Line keys reference the diagram on DATA 106.

3350	CE0142 Seq. 2 of 2	2358497 Part No.	441300 31 Mar 76	441303 30 Jul 76	441308 18 Aug 78	

AD TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 20 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2M13
+Fmt G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 20 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 6.0
Source – Int Ch 1

DATA 108
A

Legend:
☐ Inactive
■ Active level
▨ Tolerance

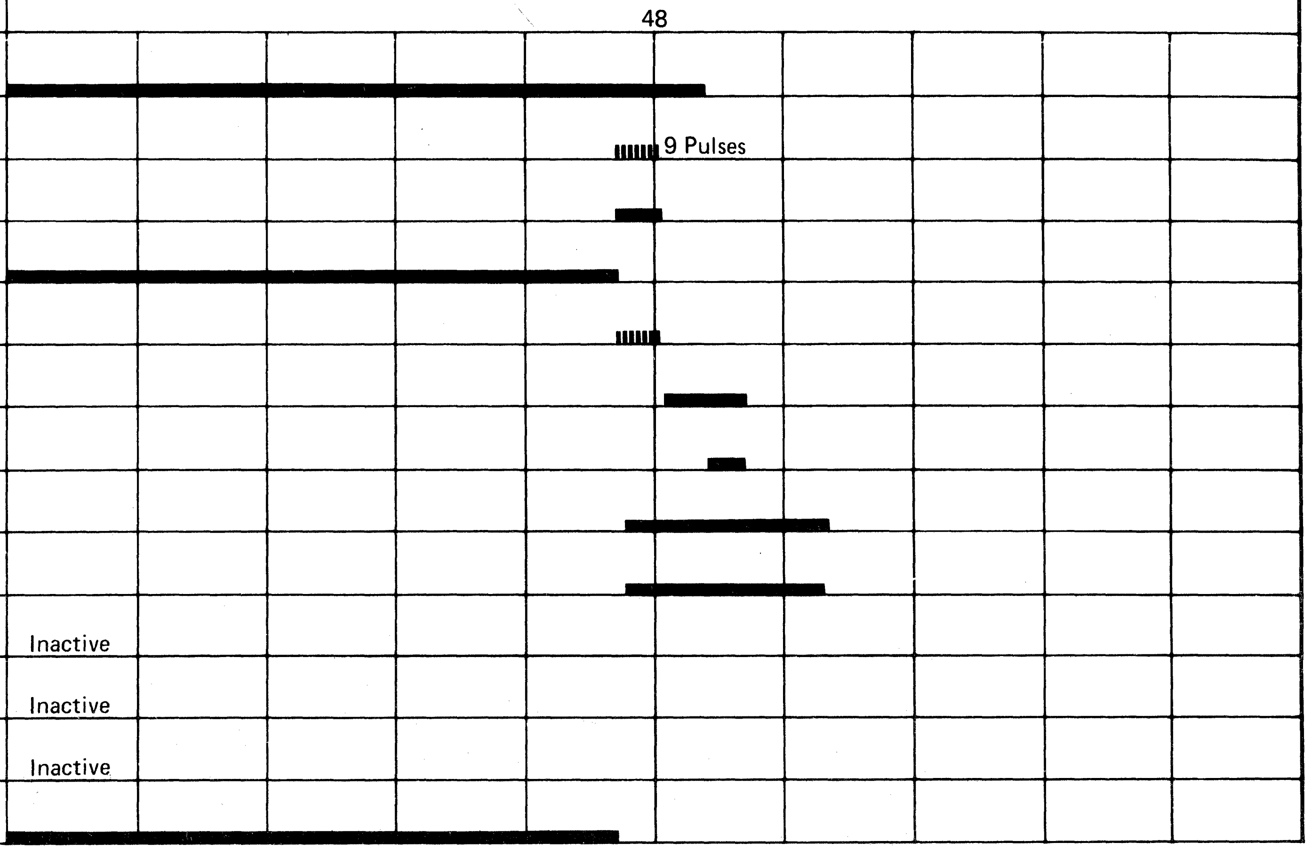


Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+Fmt G1	BH140	A2Q2 M13	G	
2	–Sync In	BC170	A2S2 S10	N	9 Pulses
3	–Write Mode	BG140	A2P2 M10	K	
4	+Recycle	BF160	A2G2 S10	E	
5	+Sync Out	BC170	A2S2 S12	M	
6	+ End Data	BG170	A2P2 G02	L	
7	–End Data Op	BG170	A2Q2 G08	F	
8	–4 to 7 Odd	BG100	A2P2 P05	H	
9	–Bus Out Bit 4	BG100	A2P2 S10	J	
10	–Bus Out Bit 5	BG100	A2P2 U11		Inactive
11	–Bus Out Bit 6	BG100	A2P2 S12		Inactive
12	–Bus Out Bit 7	BG100	A2P2 S13	↓	Inactive
13	+Recycle Tag NPL	BF160	A2G2 U12	B	

Line keys reference the diagram on DATA 106.

3350	CE0152 Seq. 1 of 2	2358498 Part No.	441300 31 Mar 76	441303 30 Jul 76	441308 18 Aug 78		

AD TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 20 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

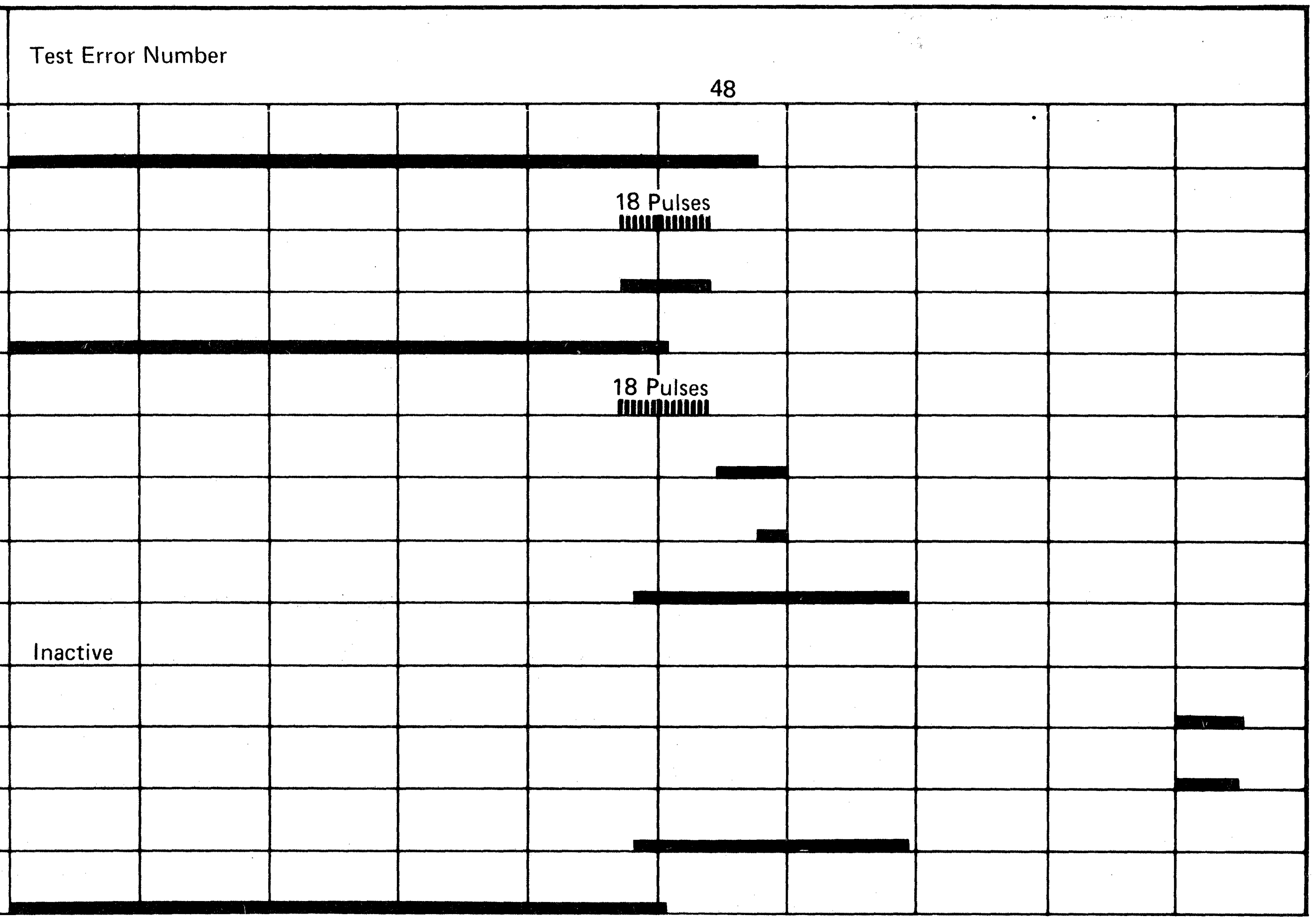
Ch 1 A2Q2M13
+Fmt G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 20 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 µs/div
Delay-Time Multiplier – 8.0
Source – Int Ch 1

DATA 108
A

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+Fmt G1	BH140	A2Q2 M13	G
2	–Sync In	BC170	A2S2 S10	N
3	–Write Mode	BG140	A2P2 M10	K
4	+Recycle	BF160	A2G2 S10	E
5	+Sync Out	BC170	A2S2 S12	M
6	+End Data	BG170	A2P2 G02	L
7	–End Data Op	BG170	A2Q2 G08	F
8	–4 to 7 Odd	BG100	A2P2 P05	H
9	–Bus Out Bit 4	BG100	A2P2 S10	J
10	–Bus Out Bit 5	BG100	A2P2 U11	
11	–Bus Out Bit 6	BG100	A2P2 S12	
12	–Bus Out Bit 7	BG100	A2P2 S13	
13	+Recycle Tag NPL	BF160	A2G2 U12	B



Line keys reference the diagram on DATA 106.

3350

CE0152 Seq. 2 of 2	2358498 Part No.	441300 31 Mar 76	441303 30 Jul 76	441308 18 Aug 78		

ECC HARDWARE CHECK

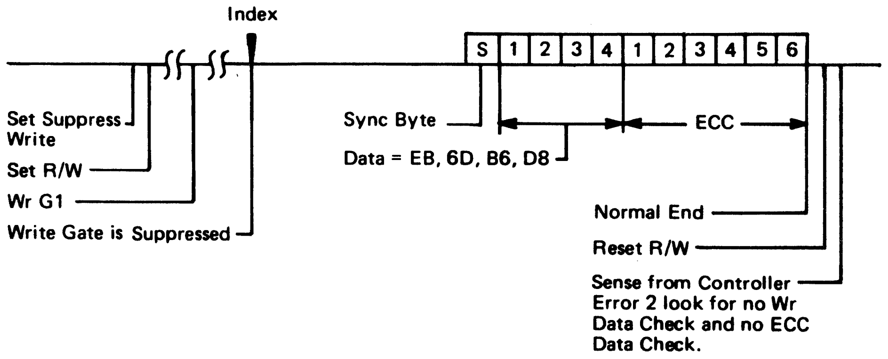
ERROR DESCRIPTION

The ECC Hardware Check is set by:

- Odd number of ECC SR bits at B time.
- Missing C pulse to the Shift Register as indicated by the lack of +Time B Response.
- Missing B pulse to the Shift Register as indicated by the lack of +Time B Response.
- +Time A Reset active all the time.
- Failure to activate Run ECC.
- Xfer ECC Control active without Run ECC active.

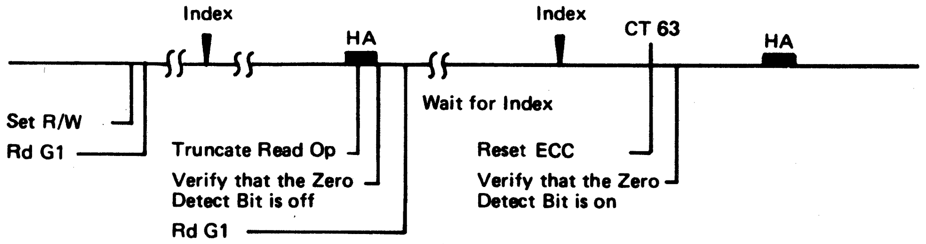
MICRODIAGNOSTIC DESCRIPTION

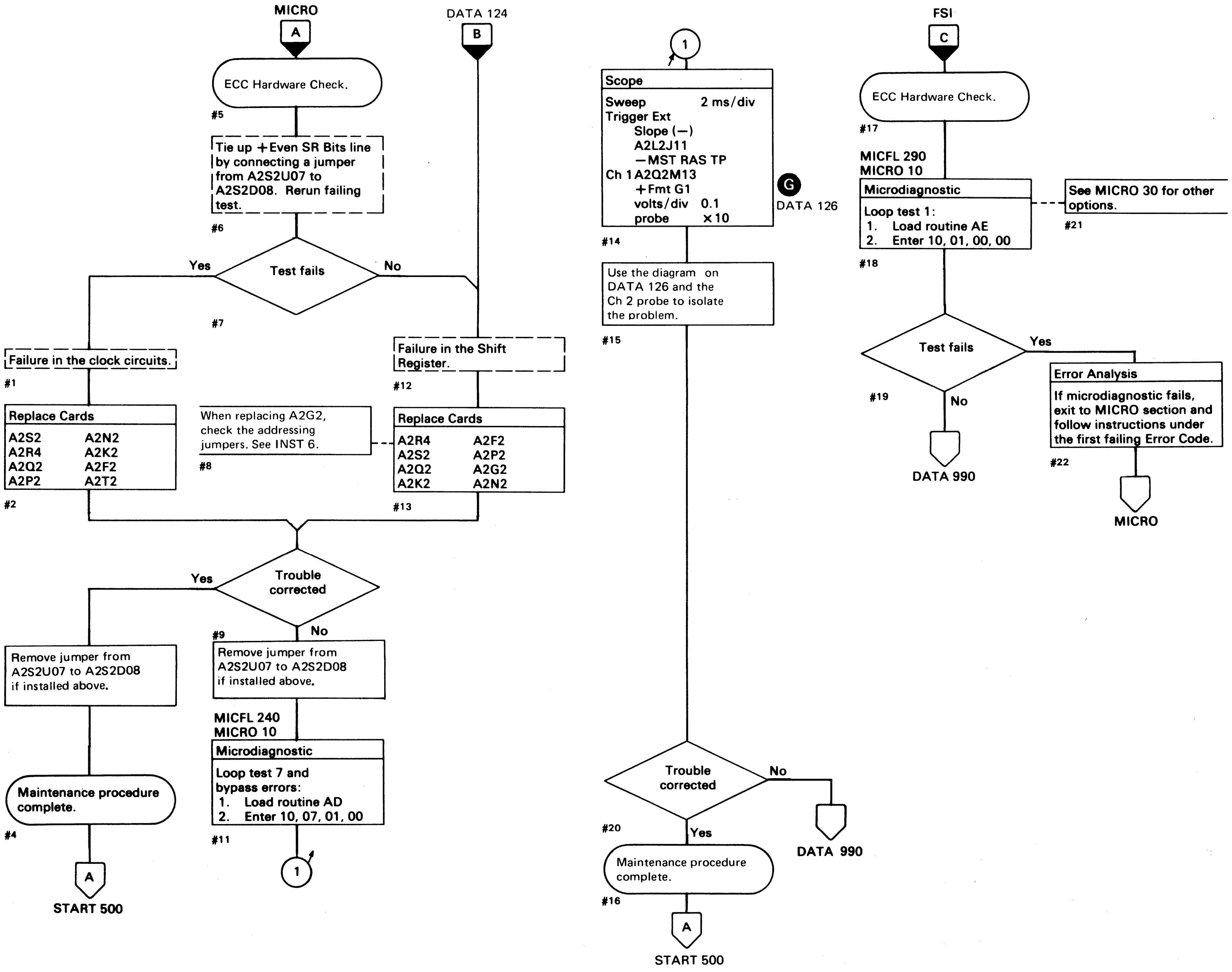
Routine AD, test 7 shifts a worst-case data pattern through SERDES and the ECC Shift Register. The test should not result in a Write Data Check or ECC Hardware Check.



Routine AE, test 1 checks the ability to set and reset the ECC Shift Register. After execution of a Rd G1 command with an erroneous byte count, the ECC Shift Register is expected to be nonzero. This condition is verified by checking that the Zero Detected Bit is zero. Another Rd G1 command is issued and the operation proceeds in the following manner:

1. Wait for an Index.
2. Delay until after ECC Shift Register reset time.
3. Verify that the ECC Shift Register is reset (the Zero Detected Bit is on).





CE0160 Seq. 1 of 1	2358499 Part No.	441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77		

WRITE DATA CHECK

ERROR DESCRIPTION

The 3350 does not record parity bits on the disk surface. The Error Correction Code ensures that recorded data is read properly. The Write Data Check ensures that the data was recorded properly.

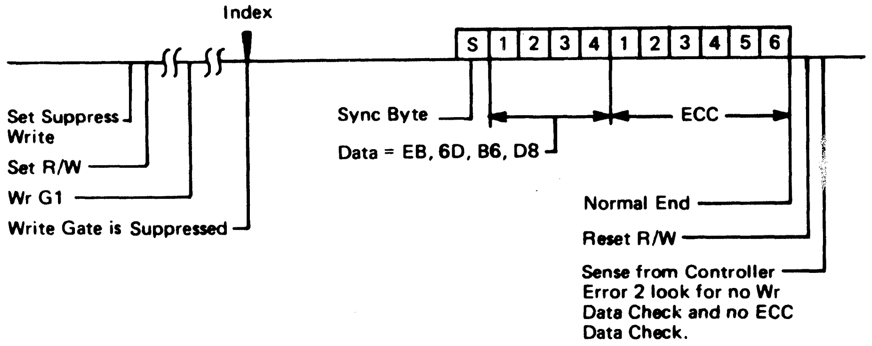
- The parity bit received at the controller from the storage control is saved, while the remainder of bits is sent serially to the SERDES Shift Register and to the disk.
- After the byte is serialized, the generated parity of the Shift Register is compared with the parity bit saved at the controller.

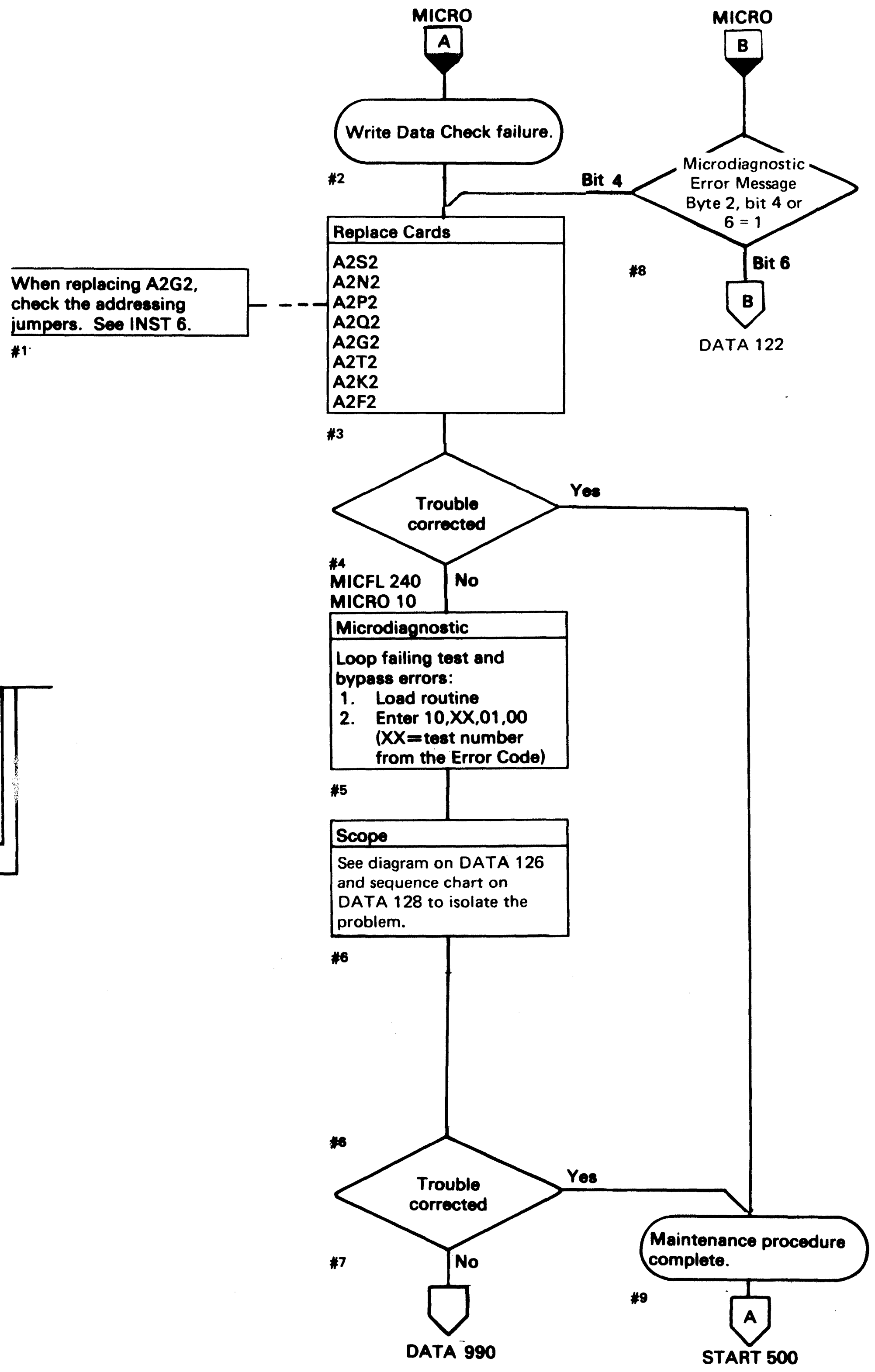
A comparison failure sets the Write Data Check latch.

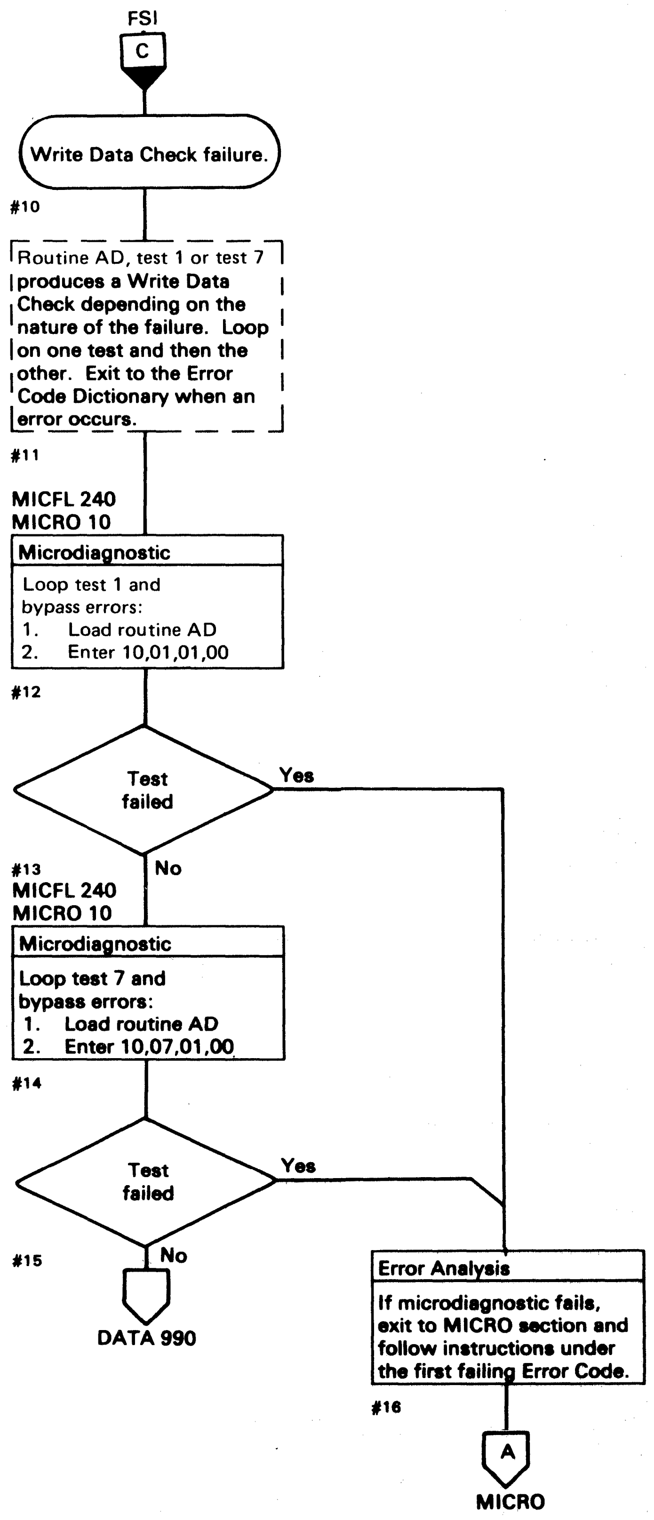
MICRODIAGNOSTIC DESCRIPTION

See DATA 74 for a description of routine AD, test 1.

Routine AD, test 7 shifts a worst-case data pattern through SERDES and the ECC Shift Register. The test should not result in a Write Data Check or ECC Hardware Check.

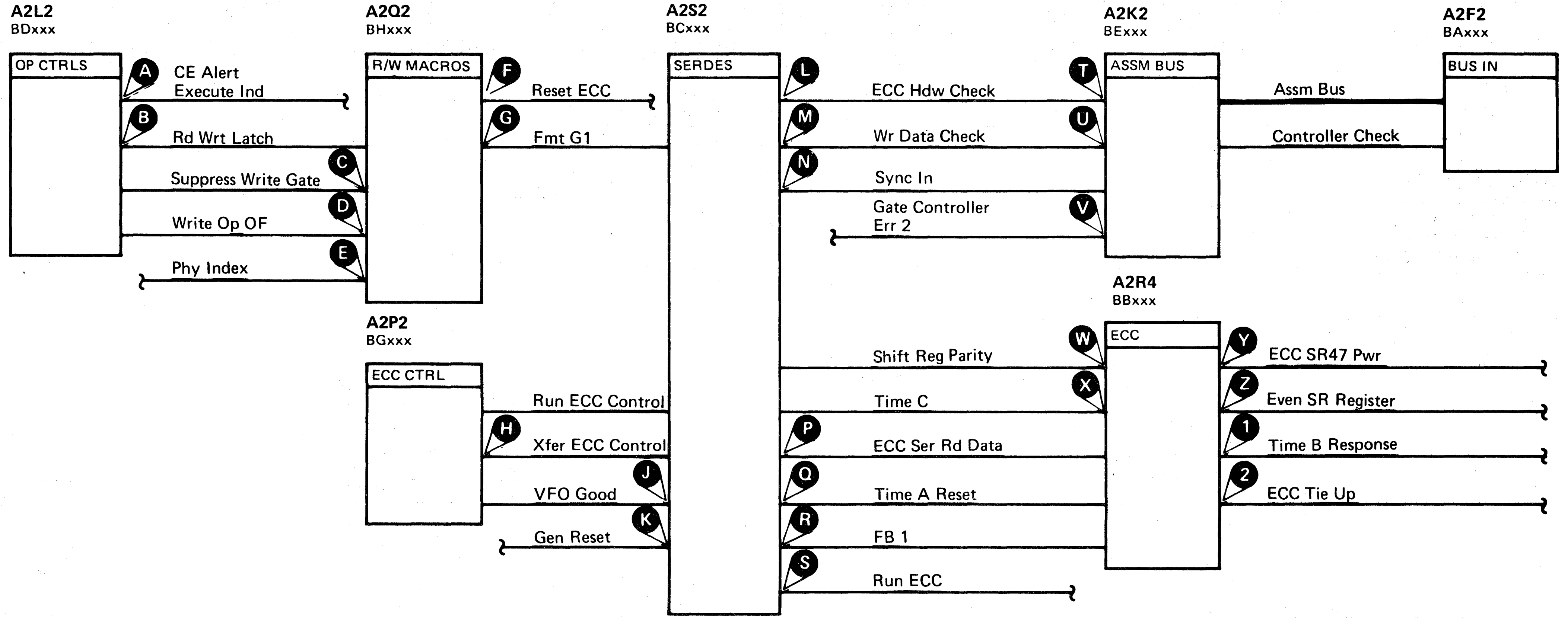






AD TEST 7 DIAGRAM

See the sequence chart on DATA 128 for referenced test points.
See OPER 241 for theory.



AD TEST 7 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AD, test 7
1. Load AD
2. Enter 10,07,00,00

Scope Setup

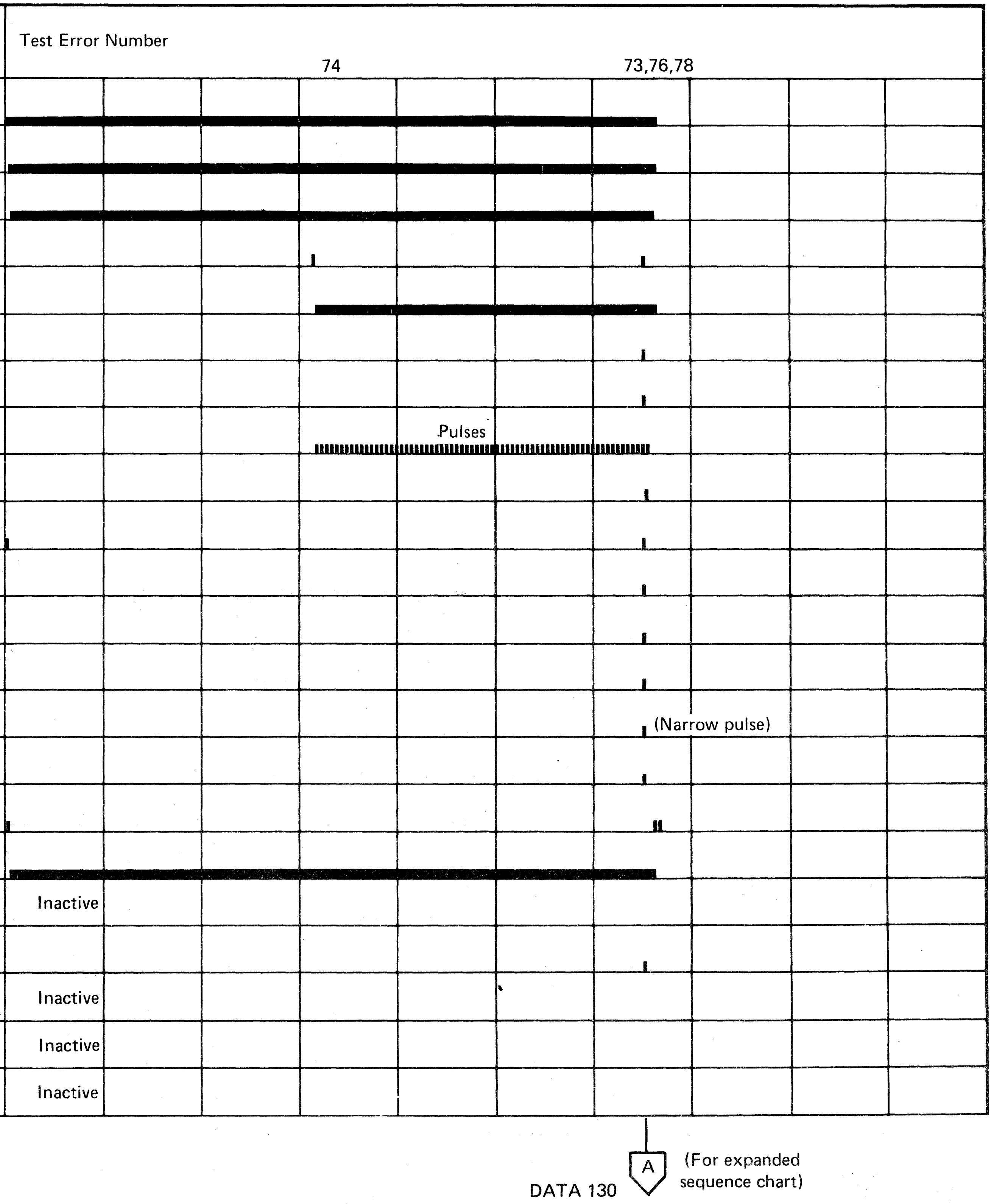
Sweep 5 ms/div
Mode Alt or Chop

Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend: ▭ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	A
2	+Suppress Write Gate	BH140	A2Q2 U03	C
3	−Rd Wrt Latch	BD150	A2L2 J03	B
4	−Phy Index	BH170	A2Q2 S07	E
5	−Write Op 0F	BH100	A2Q2 P03	D
6	+Fmt G1	BH140	A2Q2 M13	G
7	−Sync In	BC170	A2S2 S10	N
8	−Reset ECC	BH160	A2Q2 M04	F
9	−Xfer ECC Control	BG170	A2P2 J06	H
10	+Time A Reset	BC160	A2S2 U04	Q
11	+Time B Response	BB100	A2R4 B04	I
12	−Shift Reg Parity	BB150	A2R4 B05	W
13	+Time C	BB100	A2R4 B10	X
14	+Even SR Register	BB150	A2R4 D02	Z
15	−ECC SR 47 Pwr	BB140	A2R4 D04	Y
16	+Gen Reset	BC110	A2S2 G07	K
17	−VFO Good	BC140	A2S2 J11	J
18	−ECC Ser Rd Data	BC150	A2S2 J12	P
19	−FB1	BC150	A2S2 M04	R
20	−Run ECC	BC150	A2S2 M09	S
21	−Wr Data Check	BC130	A2S2 P06	M
22	−ECC Hdw Check	BC160	A2S2 S07	L



Line keys reference the diagram on DATA 126.

DATA 130 (For expanded sequence chart)

AD TEST 7 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2M13
+Fmt G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 µs/div
Delay-Time Multiplier – 4.0
Source – Int Ch 1

DATA 128
A

Legend:
☐ Inactive
■ Active level
▨ Tolerance

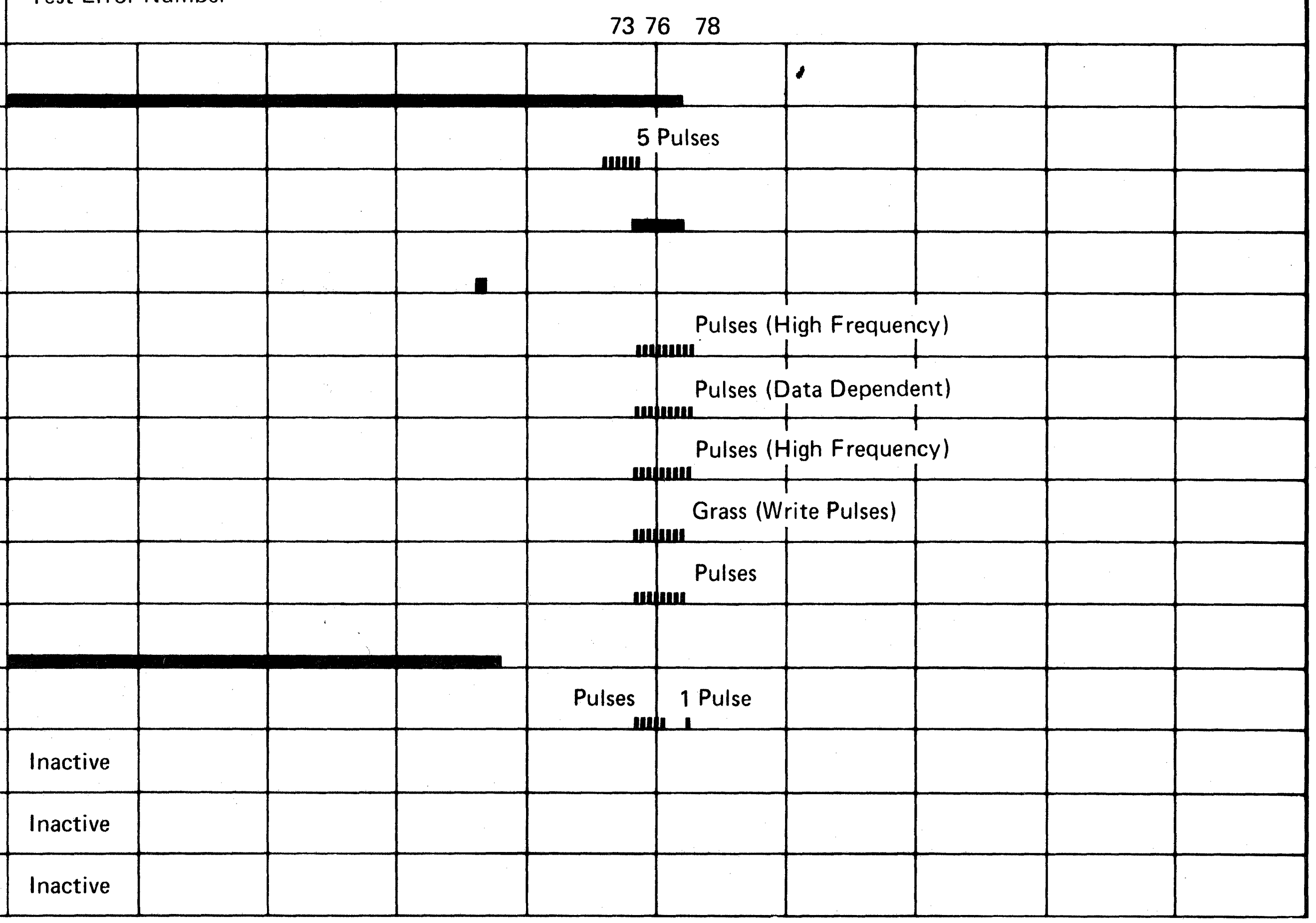


Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+Fmt G1	BH140	A2Q2 M13	Ⓖ	
2	–Sync In	BC170	A2S2 S10	Ⓝ	5 Pulses
3	–Xfer ECC Control	BG170	A2P2 J06	Ⓗ	
4	+Time A Reset	BC160	A2S2 U04	Ⓠ	
5	+Time B Response	BB100	A2R4 B04	Ⓘ	Pulses (High Frequency)
6	–Shift Reg Parity	BB150	A2R4 B05	Ⓦ	Pulses (Data Dependent)
7	+Time C	BB100	A2R4 B10	Ⓧ	Pulses (High Frequency)
8	+Even SR Register	BB150	A2R4 D02	Ⓩ	Grass (Write Pulses)
9	–ECC SR47 Pwr	BB140	A2R4 D04	Ⓨ	Pulses
10	–VFO Good	BC140	A2S2 J11	Ⓙ	
11	–FB1	BC150	A2S2 M04	Ⓡ	Pulses 1 Pulse
12	–Gate Controller Err 2	BE120	A2K2 M03	Ⓥ	Inactive
13	–ECC Hdw Check	BE120	A2K2 U06	Ⓣ	Inactive
14	–Wr Data Check	BE120	A2K2 P05	Ⓤ	Inactive

Line keys reference the diagram on DATA 126.

SKIP DEFECT GAP TOLERANCE

ERROR DESCRIPTION

Routine AD, test A writes a series of records on the disk testing the ability to create gaps of varying lengths, particularly the gaps associated with defect skipping. The gaps created and checked are (in order):

1. G1 gap (not checked in this test)
2. Special G2 (79 bytes)
3. Special G2 (128 bytes)
4. G4 gap (128 bytes)
5. G2 gap (128 bytes)
6. G2 gap (79 bytes)

If the Gap 128 latch fails to set, one or more of the 128-byte gaps will be 79 bytes. If the Gap 128 latch fails to reset, the last gap may be 128 bytes instead of 79 bytes.

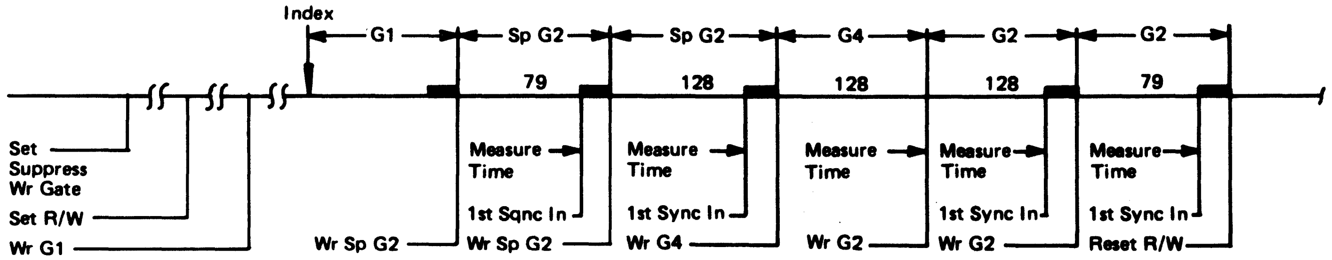
MICRODIAGNOSTIC DESCRIPTION

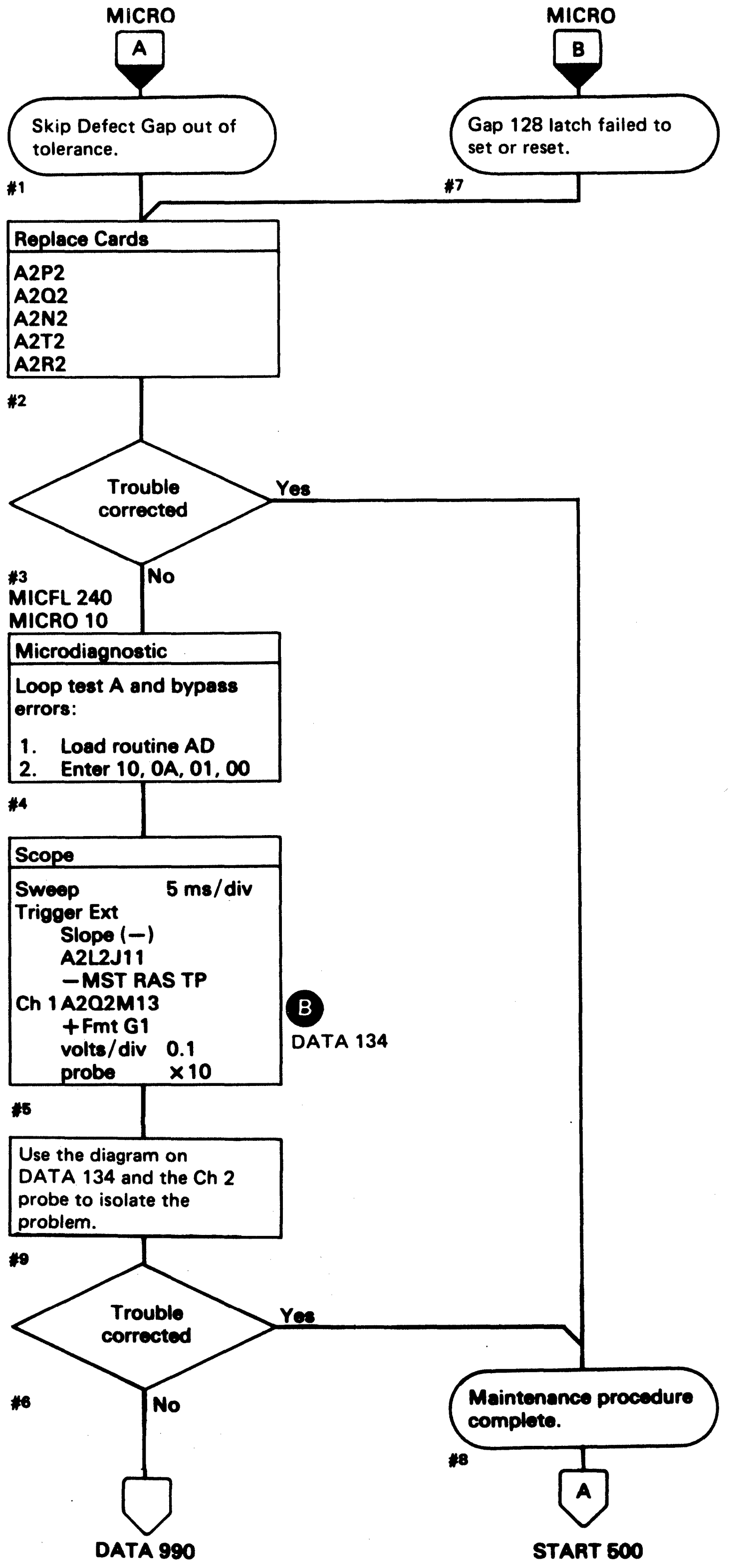
Routine AD, test A measures the generation of the gaps associated with Defect Skipping that are caused by the Special G2 and G4 operations.

Test A issues the following string of operations:

Write G1
Write G2 Special
Write G2 Special
Write G4
Write G2
Write G2

After initially orienting on Index, each gap is measured by timing from the end of one operation to the first Sync In of the subsequent operation. The times are compared with nominal values for each operation. Errors in this routine are ordinarily associated with the Gap 128 Latch.



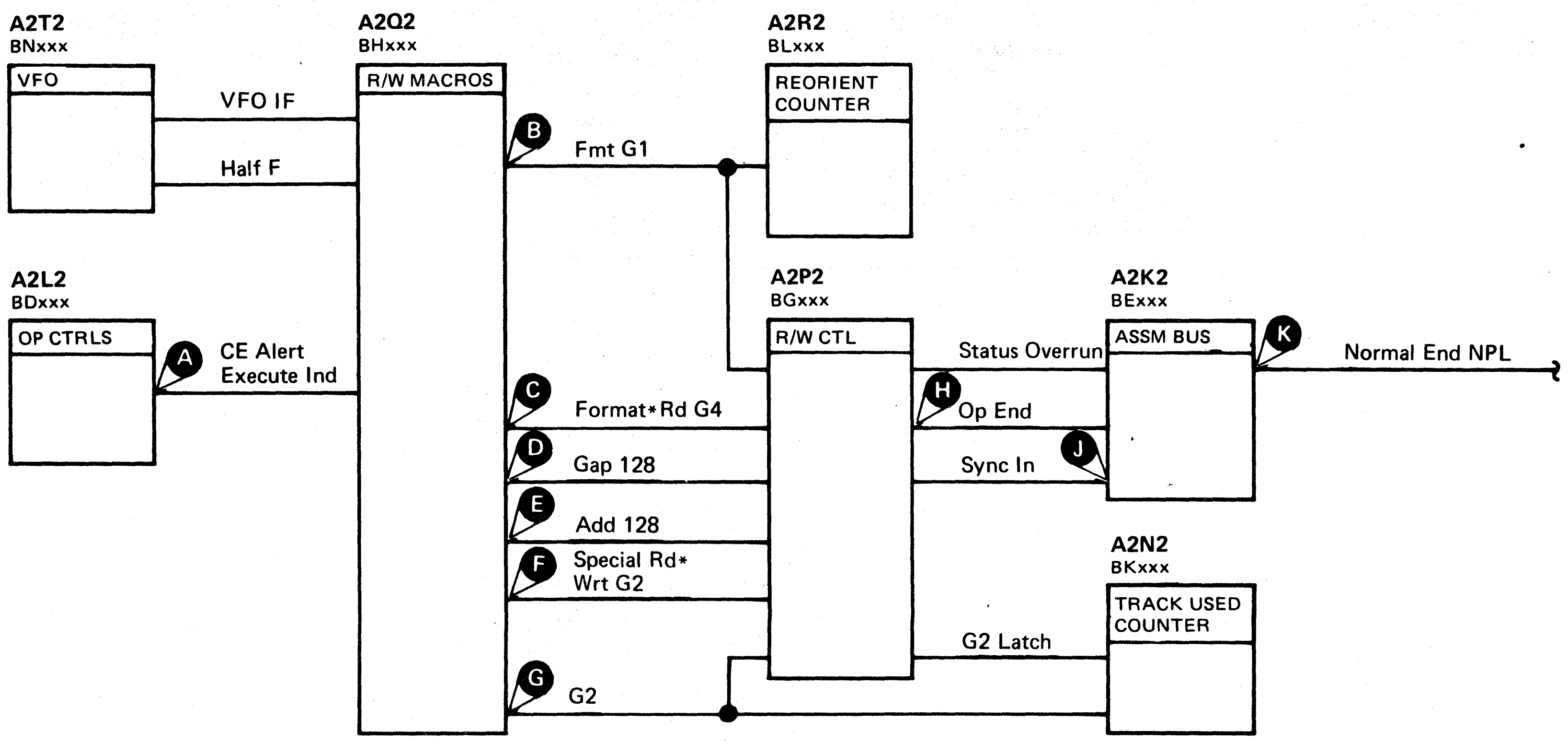


CE0172 Seq. 1 of 2	2358502 Part No.

441300 31 Mar 76	441303 30 Jul 76			

AD TEST A DIAGRAM

See the sequence charts on DATA 136 and 138 for referenced test points.
See OPER 36 for theory.



3350	CE0172 Seq. 2 of 2	2358502 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AD TEST A SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AD, test A
1. Load AD
2. Enter 10,0A,00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop

Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend: ▭ Inactive
■ Active level
▨ Tolerance

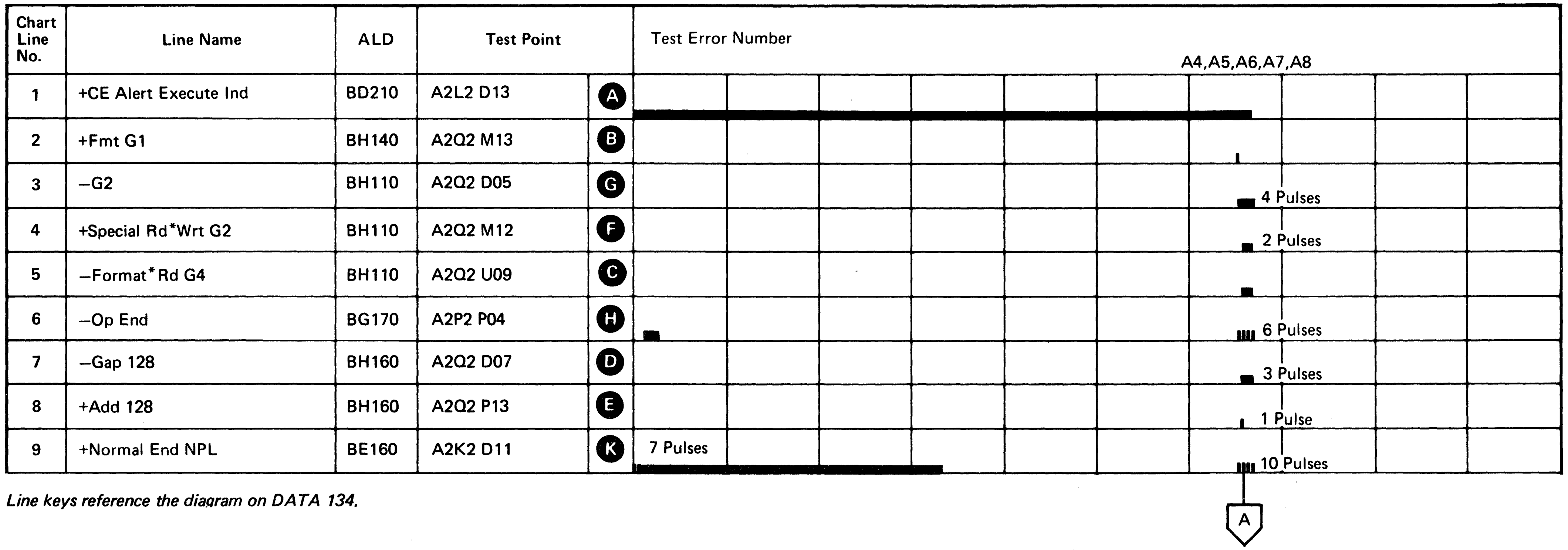


Chart Line No.	Line Name	ALD	Test Point		Test Error Number A4,A5,A6,A7,A8
1	+CE Alert Execute Ind	BD210	A2L2 D13	Ⓐ	
2	+Fmt G1	BH140	A2Q2 M13	Ⓑ	
3	−G2	BH110	A2Q2 D05	Ⓖ	4 Pulses
4	+Special Rd*Wrt G2	BH110	A2Q2 M12	Ⓕ	2 Pulses
5	−Format*Rd G4	BH110	A2Q2 U09	Ⓒ	
6	−Op End	BG170	A2P2 P04	Ⓗ	6 Pulses
7	−Gap 128	BH160	A2Q2 D07	Ⓓ	3 Pulses
8	+Add 128	BH160	A2Q2 P13	Ⓔ	1 Pulse
9	+Normal End NPL	BE160	A2K2 D11	Ⓚ	7 Pulses 10 Pulses

Line keys reference the diagram on DATA 134.

A
DATA 138
(For expanded sequence chart)

AD TEST A SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

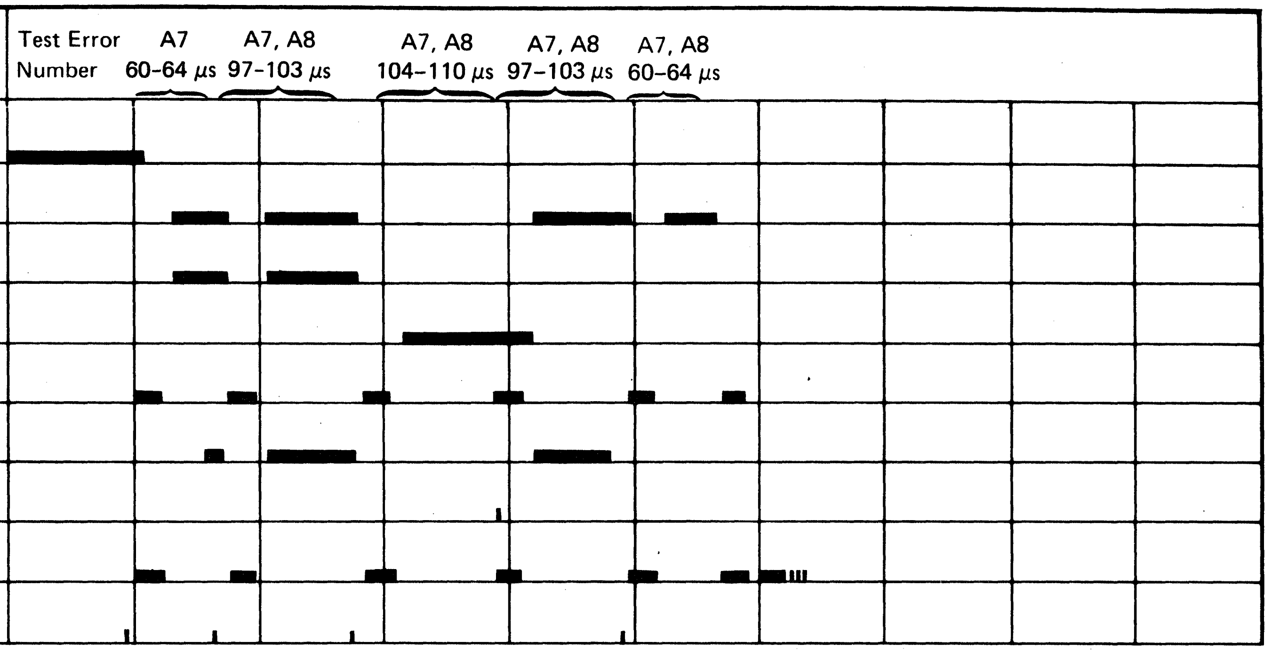
Ch 1 A2Q2M13
+Fmt G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 0.1 ms/div
Delay-Time Multiplier – 6.0
Source – Int Ch 1

DATA 136
A

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+Fmt G1	BH140	A2Q2 M13	Ⓑ
2	–G2	BH110	A2Q2 D05	Ⓖ
3	+Special Rd*Wrt G2	BH110	A2Q2 M12	Ⓕ
4	–Format*Rd G4	BH110	A2Q2 U09	Ⓒ
5	–Op End	BG170	A2P2 P04	Ⓗ
6	–Gap 128	BH160	A2Q2 D07	Ⓓ
7	+Add 128	BH160	A2Q2 P13	Ⓔ
8	+Normal End NPL	BE160	A2K2 D11	Ⓚ
9	–Sync In	BE160	A2K2 D07	Ⓙ



Line keys reference the diagram on DATA 134.

I WRITE FAIL ERROR

ERROR DESCRIPTION

When a Write operation is initiated, the controller provides the necessary control lines to the drive. When all the required controls are received by the drive, the I Write Sense line is returned to the controller on Bus In bit 1. The controller verifies that Bus In bit 1 is active at the proper time during the Write operation. If it is not, the I Write Fail error is indicated.

MICRODIAGNOSTIC DESCRIPTION

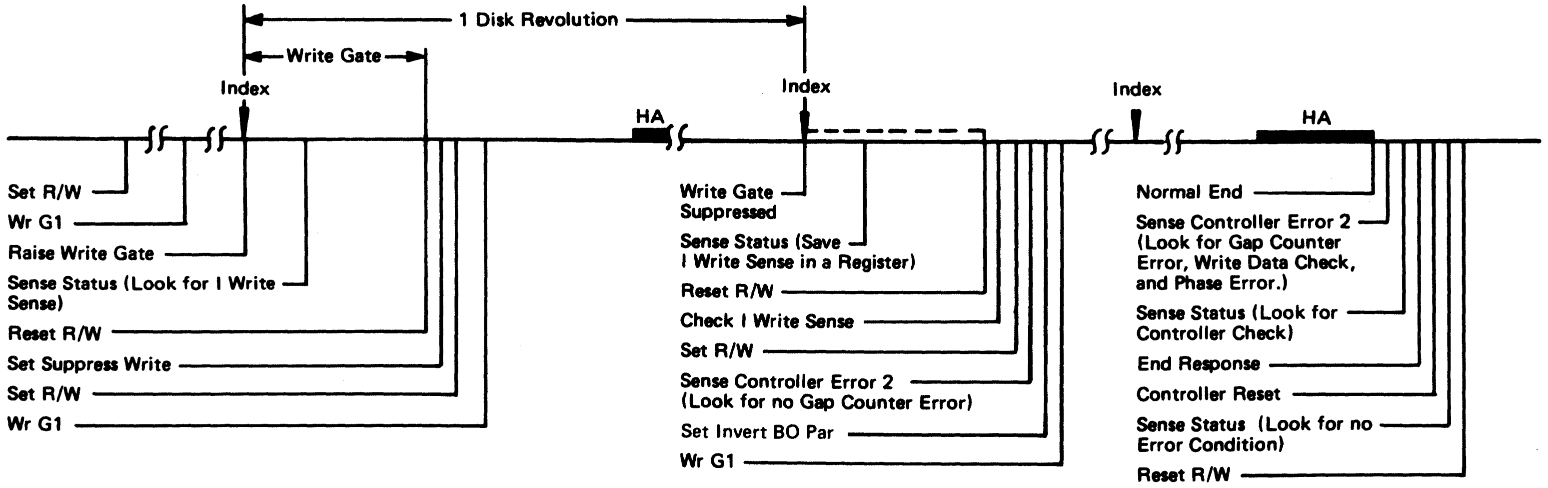
Routine AD, test 1 is the first of a series of tests that uses the controller in Write mode to test a variety of data handling functions. To prevent writing data on the disk, the Diagnostic Suppress Write command is used. The first function of Routine AD, test 1 is to verify the operation of Diagnostic Suppress Write by activating the Write Gate at Index time for approximately 15 microseconds and to verify that an I Write Sense response is received. Suppress Write is then activated and Write Gate is activated again at the next Index time. No I Write Sense response indicates that Suppress Write functioned properly.

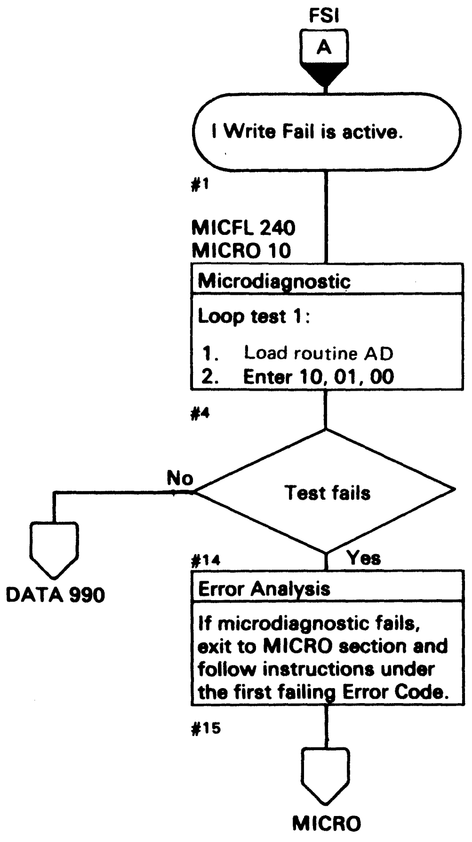
The test then uses Diagnostic Invert Bus Out Parity to force:

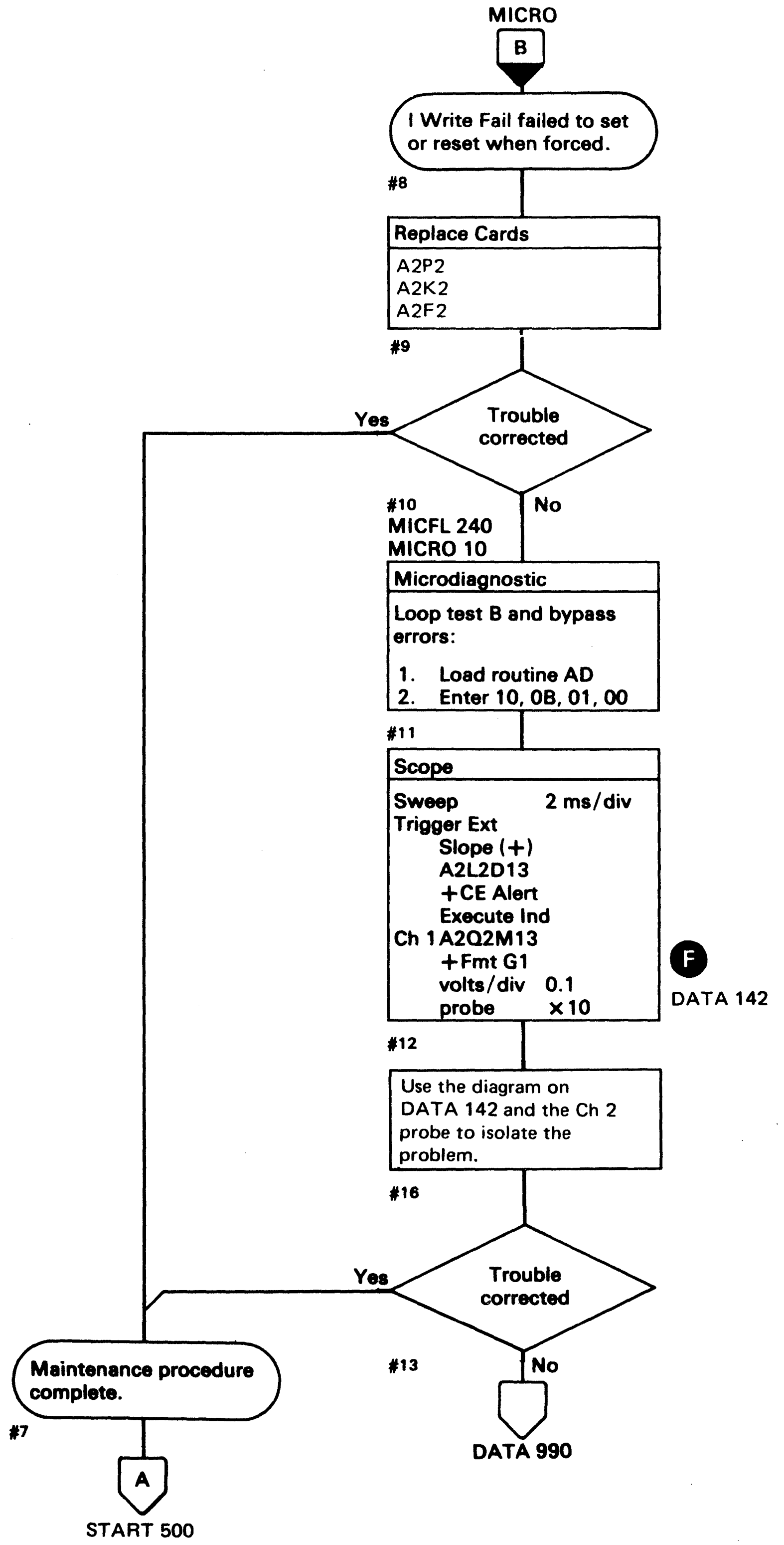
- Gap Counter Error
- Write Data Check
- Phase Error

The test also verifies that a Controller Check follows the sensing of the error latches.

Routine AD, test B tests the ability to force the I Write Fail latch on. A Monitor Check and a Read/Write Check are forced using circuits previously tested. A Write G1 command is issued. The Read/Write Check on in the drive blocks the generation of I Write Sense. In the controller, the combination of a Write operation and the lack of I Write Sense forces the I Write Fail latch on.

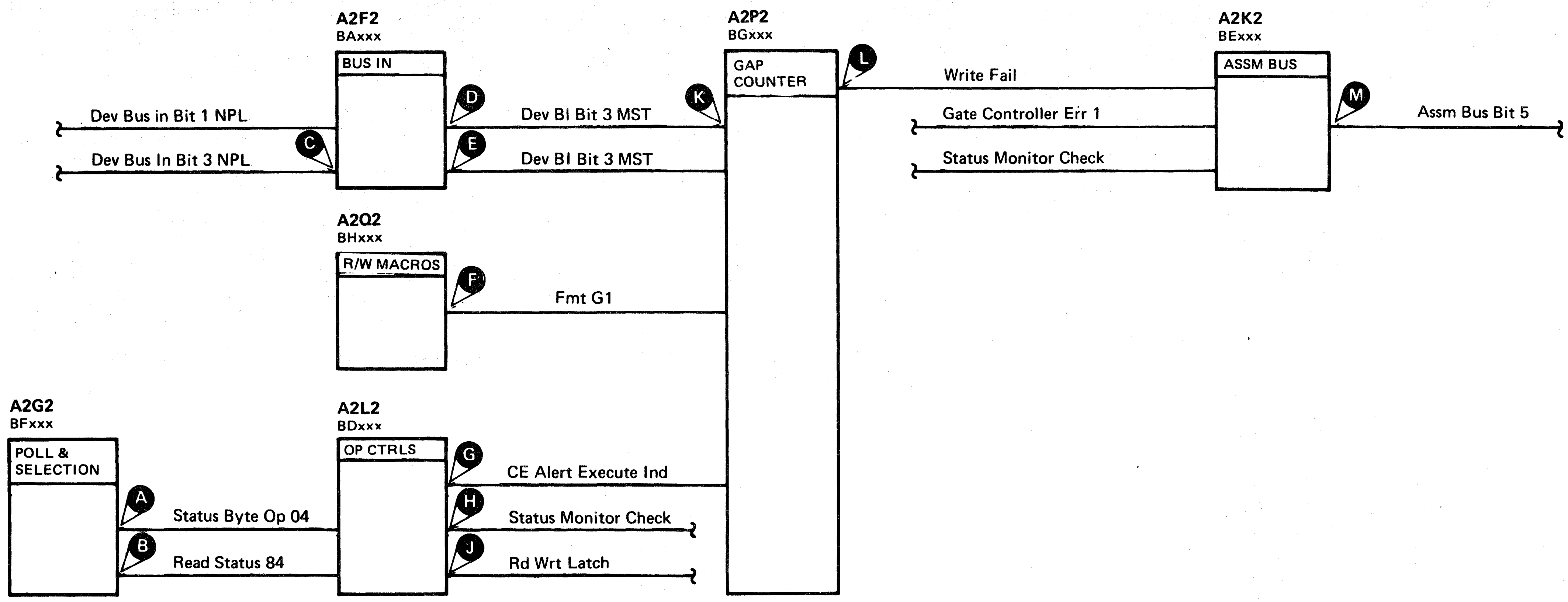






AD TEST B DIAGRAM

See the sequence chart on DATA 144 for referenced test points.
See OPER 241 for theory.



CE0182 Seq. 2 of 2	2358504 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AD TEST B SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AD, test B
1. Load AD
2. Enter 10,0B,00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop

Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend:
▭ Inactive
■ Active level
▨ Tolerance

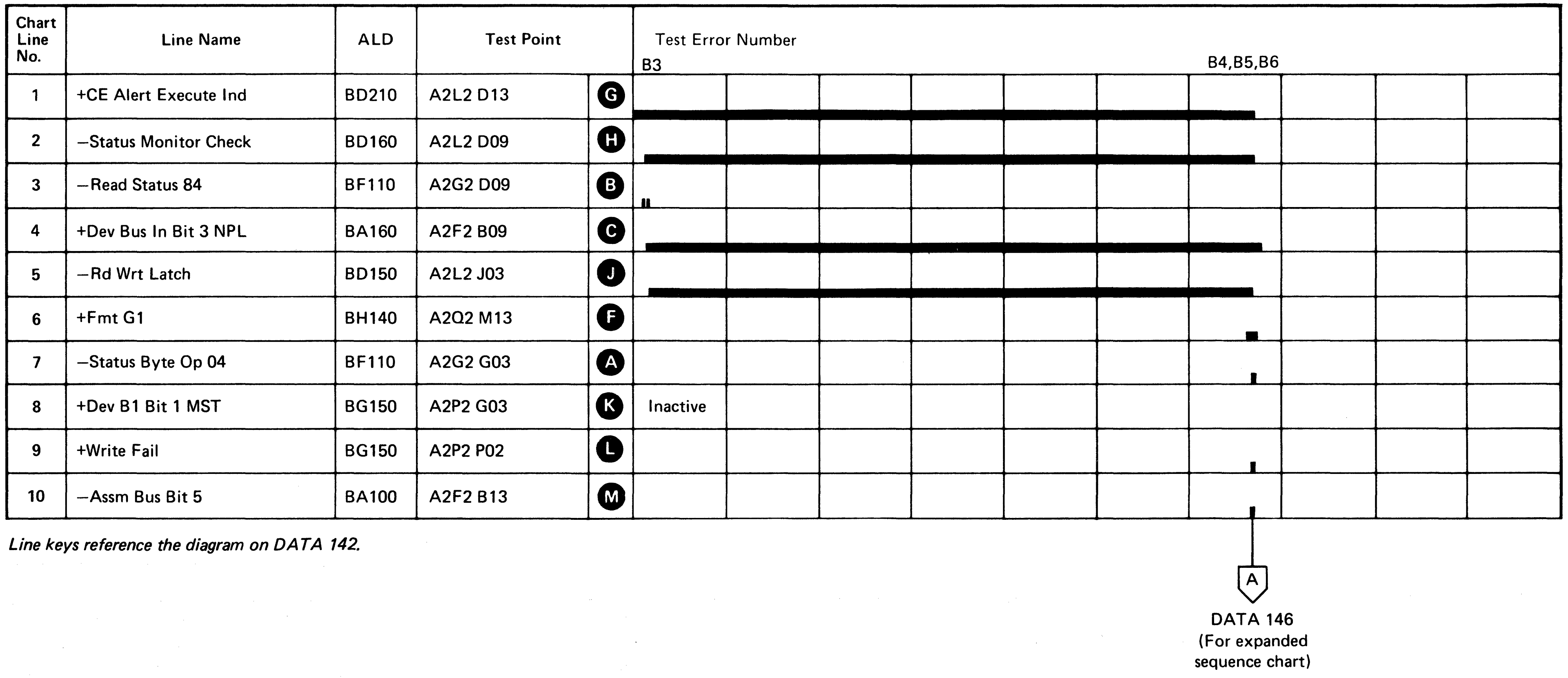


Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	G
2	−Status Monitor Check	BD160	A2L2 D09	H
3	−Read Status 84	BF110	A2G2 D09	B
4	+Dev Bus In Bit 3 NPL	BA160	A2F2 B09	C
5	−Rd Wrt Latch	BD150	A2L2 J03	J
6	+Fmt G1	BH140	A2Q2 M13	F
7	−Status Byte Op 04	BF110	A2G2 G03	A
8	+Dev B1 Bit 1 MST	BG150	A2P2 G03	K
9	+Write Fail	BG150	A2P2 P02	L
10	−Assm Bus Bit 5	BA100	A2F2 B13	M

Line keys reference the diagram on DATA 142.

AD TEST B SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

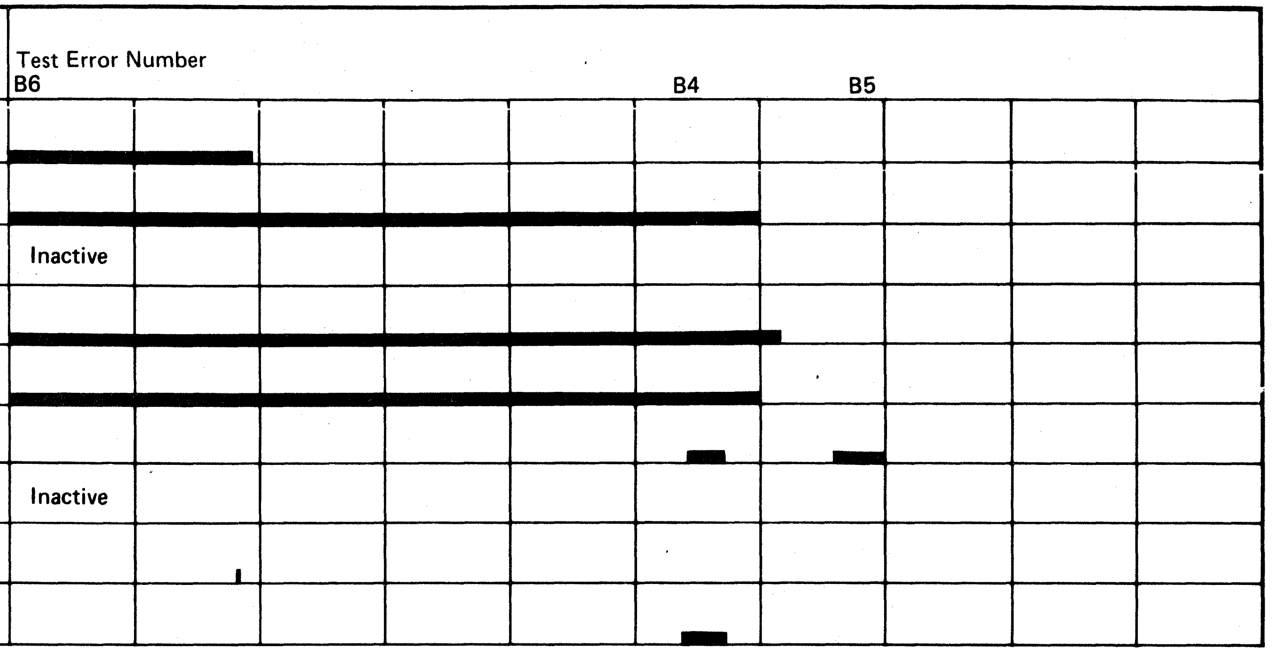
Sweep	5 ms/div	Ch 1	A2Q2M13 +Fmt G1
Mode	Alt or Chop	Volts/div	0.1
Trigger	Ext Slope (+) A2L2D13 +CE Alert Execute Ind	Probe	x10
		Ch 2	(See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 µs/div
Delay-Time Multiplier – 6.0
Source – Int Ch 1

DATA 144 Ⓐ

Legend: ▭ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+Fmt G1	BH140	A2Q2 M13	F
2	–Status Monitor Check	BD160	A2L2 D09	H
3	–Read Status 84	BF110	A2G2 D09	B
4	+Dev Bus In Bit 3 NPL	BA160	A2F2 B09	C
5	–Rd Wrt Latch	BD150	A2L2 J03	J
6	–Status Byte Op 04	BF110	A2G2 G03	A
7	+Dev B1 Bit 1 MST	BG150	A2P2 G03	K
8	+Write Fail	BG150	A2P2 P02	L
9	–Assm Bus Bit 5	BA100	A2F2 B13	M



Line keys reference the diagram on DATA 142.

MICROPROGRAM DETECTED ECC HARDWARE ERROR

ERROR DESCRIPTION

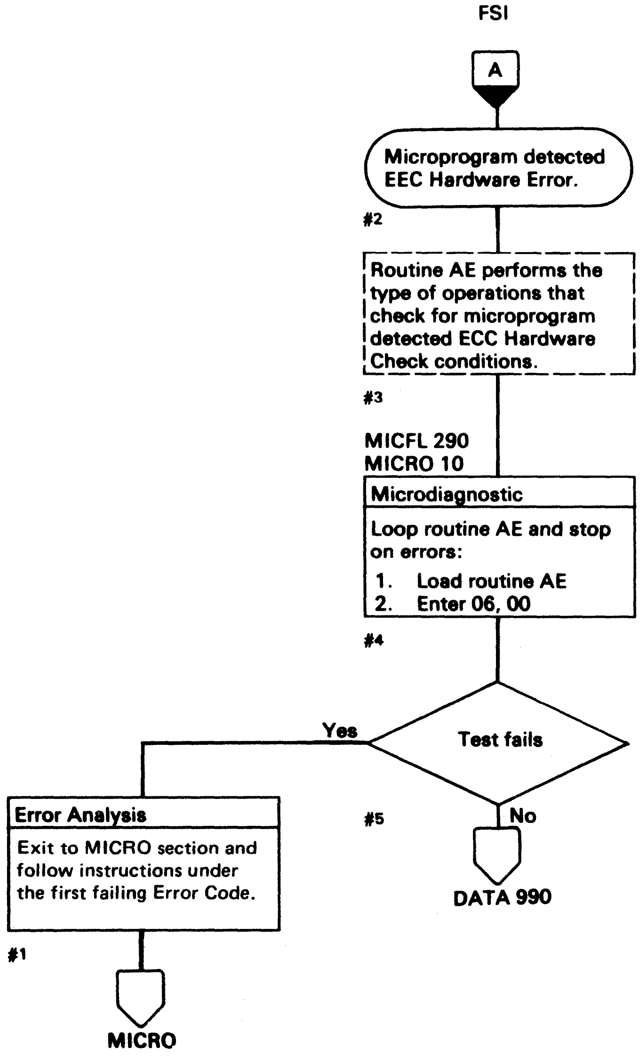
This error occurs when the controller is performing an ECC Correct operation (Tag '08'). An Index Alert signal indicates that a correctable pattern has been found. When Index Alert is received by the microprogram, a check is made to ensure Zero Detect is on. If Zero Detect is not on, an error is indicated.

If Zero Detect is present, the ECC pattern bytes are sensed (Tag '04'). If both bytes are zero, an error is indicated.

If No AM Found bit is on with a Check End following a data transfer, the ECC Data Check bit must be on also. No AM Found (bit 4) is used as a redundancy check.

If the controller fails to start the ECC Correct Op, as indicated by Sync In pulses on the interface, an error is indicated.

Microdiagnostic routine AE performs all of the operations necessary to create the conditions causing this error.



ECC ZEROS COMPARE

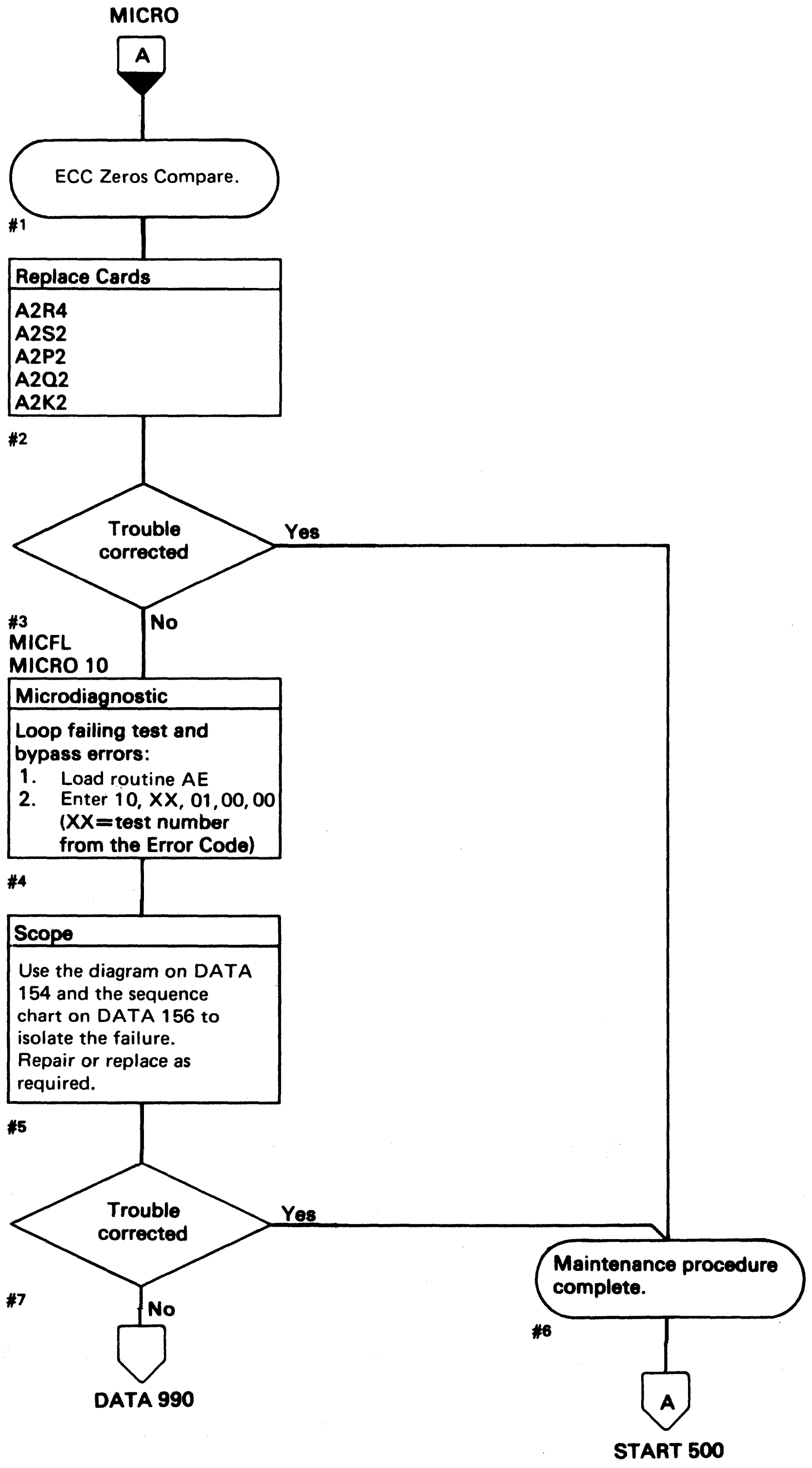
ERROR DESCRIPTION

ECC Zeros Compare is active when:

- All positions of the ECC Shift Register are off except during an ECC Correct operation.
- The first byte boundary is read during an ECC Correct operation after the ECC Shift Register positions 3 to 47 are off.

During an ECC Correct operation the correction pattern is in ECC Shift Register position 0 to 15. The pattern is gated to the storage control by Gate ECC Low Byte for bits 0 to 7 and Gate ECC Hi Byte for bits 8 to 15.

It is an error for both the high and low bytes to be zero at the end of an ECC Correct operation for a correctable Data Check, since zeros exclusive ORed with any value do not change that value.

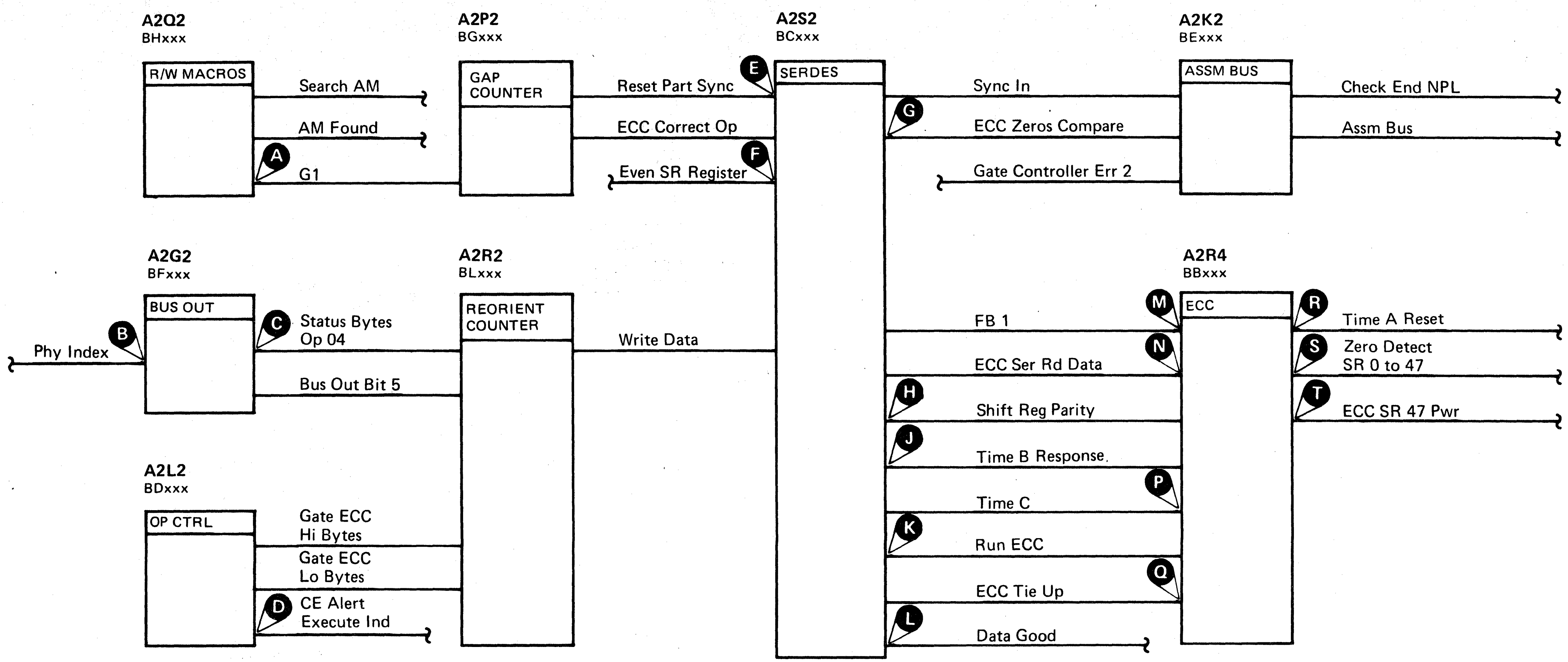


CE0203 Seq. 1 of 2	2358507 Part No.

441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77		

AE TEST 1 DIAGRAM

See the sequence chart on DATA 156 for referenced test points.
See OPER 235 for theory.



AE TEST 1 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AE, test 1
1. Load AE
2. Enter 10,01,00,00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop

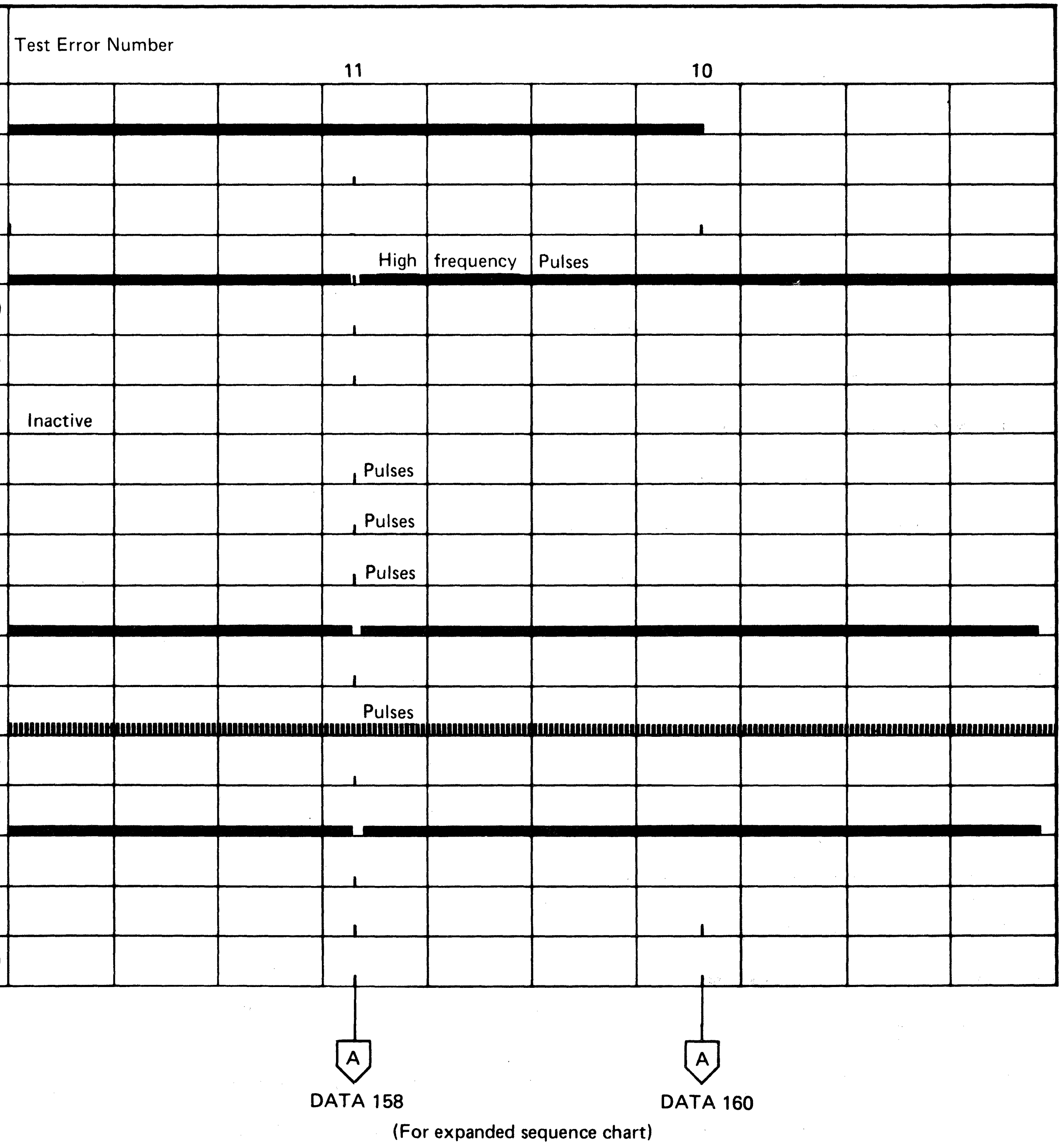
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	D
2	+G1	BH120	A2Q2 J09	A
3	+Time A Reset	BB150	A2R4 B02	R
4	+Even SR Register	BC160	A2S2 U07	F
5	−FB1	BB100	A2R4 B03	M
6	−ECC SR 47 Pwr	BB140	A2R4 D04	T
7	+ECC Tie Up	BB110	A2R4 D10/B09	Q
8	−Shift Reg Parity	BC100	A2S2 B12	H
9	+Time B Response	BC160	A2S2 S08	J
10	+Time C	BB100	A2R4 B10	P
11	−Zeros Detect SR 0 to 47	BC150	A2S2 S05	S
12	−Run ECC	BC150	A2S2 M09	K
13	+Reset Fast Sync	BC140	A2S2 M12	E
14	−Data Good	BC110	A2S2 U03	L
15	−ECC Zeros Compare	BC150	A2S2 U06	G
16	−ECC Ser Rd Data	BB100	A2R4 B07	N
17	−Status Bytes Op 04	BF110	A2G2 G03	C
18	−Phy Index	BH170	A2Q2 S07	B



Line keys reference the diagram on DATA 154.

CE0205 Seq. 1 of 2	2358508 Part No.	441300 31 Mar 76	441303 30 Jul 76				

AE TEST 1 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

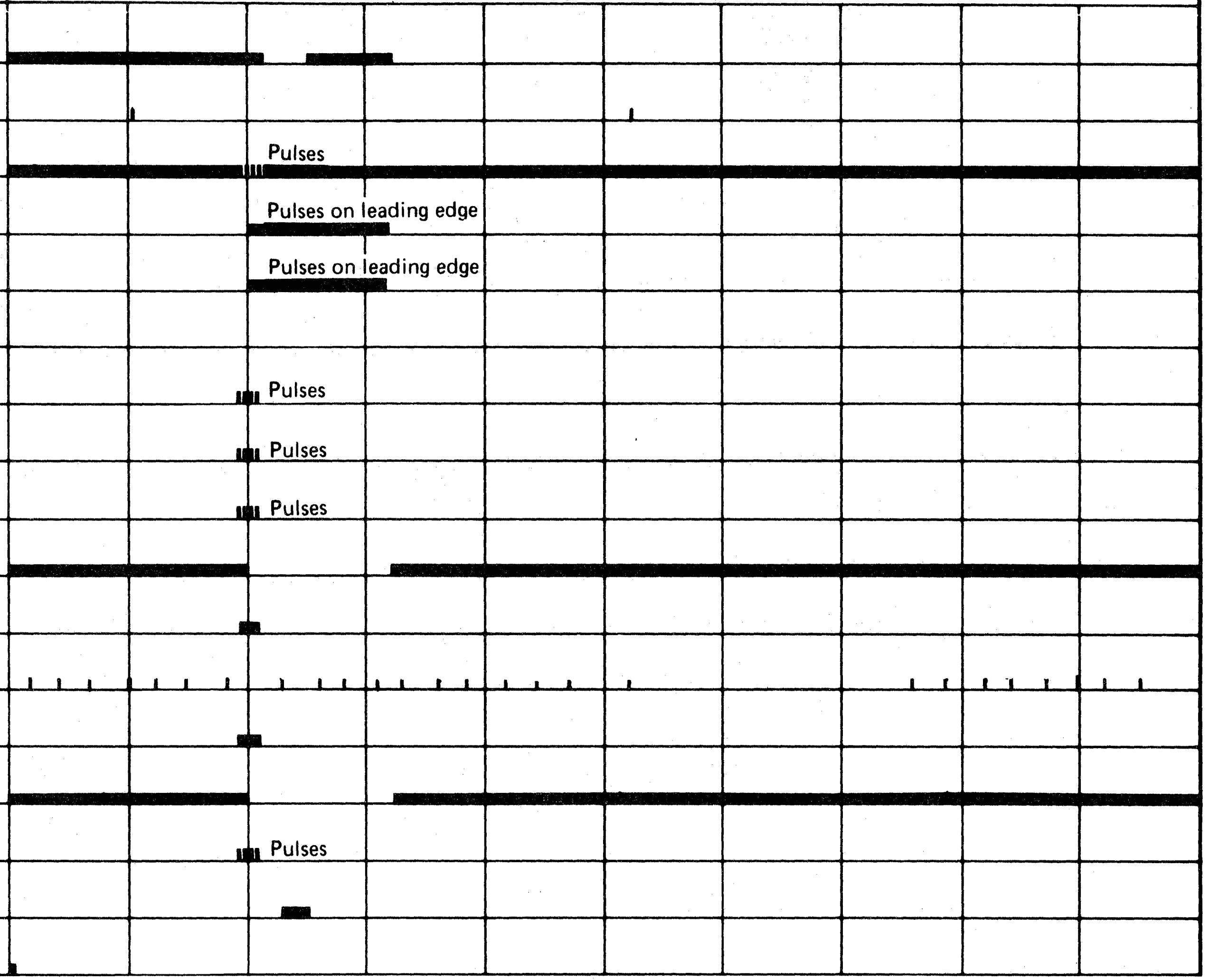
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 µs/div
Delay-Time Multiplier – 3.0
Source – Int Ch 1

DATA 156
Ⓐ

Legend: ☐ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+G1	BH120	A2Q2 J09	Ⓐ
2	+Time A Reset	BB150	A2R4 B02	Ⓡ
3	+Even SR Register	BC160	A2S2 U07	Ⓕ
4	–FB1	BB100	A2R4 B03	Ⓜ
5	–ECC SR 47 Pwr	BB140	A2R4 D04	Ⓣ
6	+ECC Tie Up	BB110	A2R4 D10/B09	Ⓠ
7	–Shift Reg Parity	BC100	A2S2 B12	Ⓗ
8	+Time B Response	BC160	A2S2 S08	Ⓙ
9	+Time C	BB100	A2R4 B10	Ⓟ
10	–Zeros Detect SR 0 to 47	BC150	A2S2 S05	Ⓢ
11	–Run ECC	BC150	A2S2 M09	Ⓚ
12	+Reset Fast Sync	BC140	A2S2 M12	Ⓔ
13	–Data Good	BC110	A2S2 U03	Ⓛ
14	–ECC Zeros Compare	BC150	A2S2 U06	Ⓖ
15	–ECC Ser Rd Data	BB100	A2R4 B07	Ⓝ
16	–Status Bytes Op 04	BF110	A2G2 G03	Ⓒ
17	–Phy Index	BH170	A2Q2 S07	Ⓑ

Test Error Number 11



Line keys reference the diagram on DATA 154.

CE0205 Seq. 2 of 2	2358508 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AE TEST 1 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

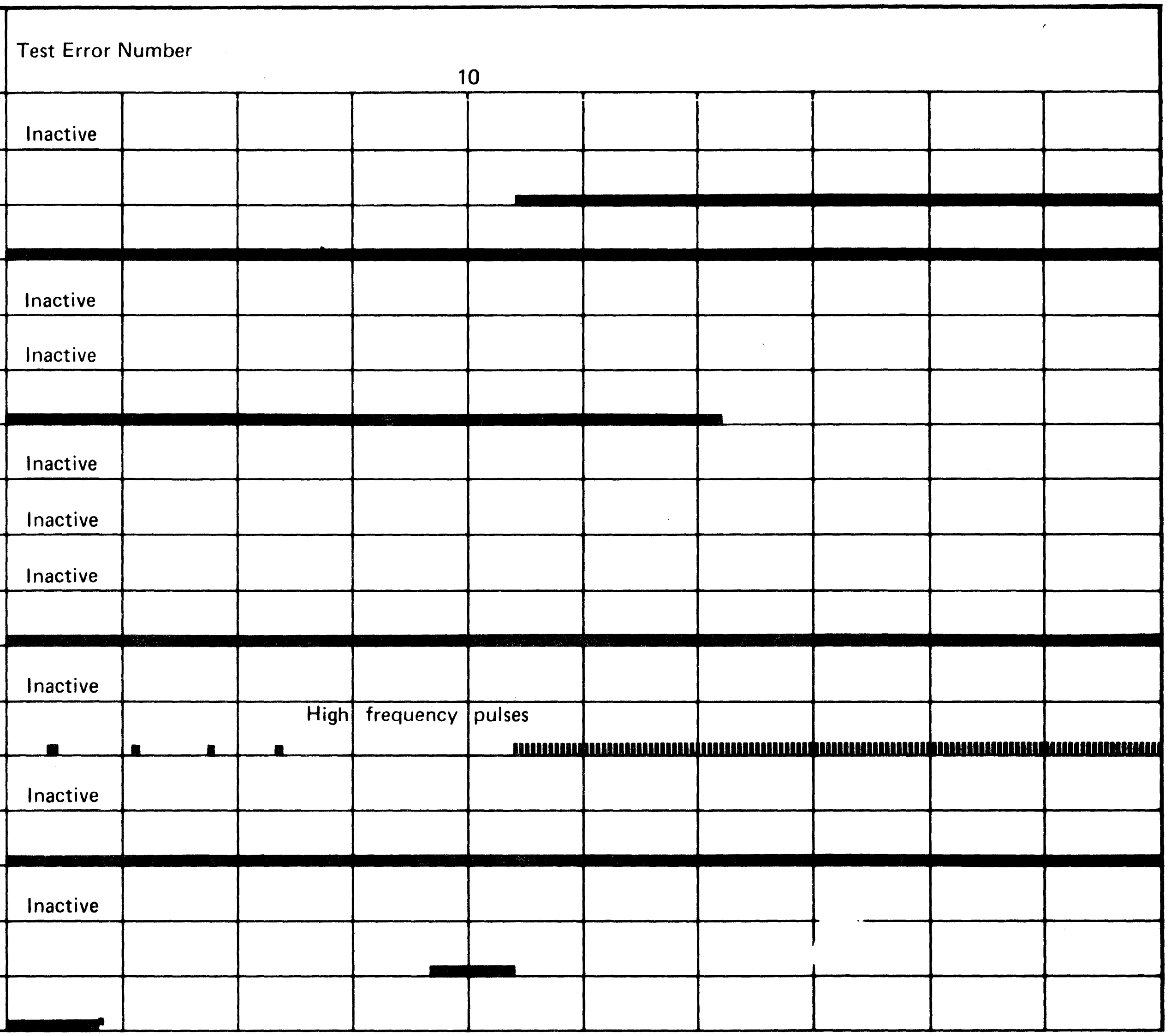
Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 6.0
Source – Int Ch 1

DATA 156 A

Legend: ☐ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+G1	BH120	A2Q2 J09	A
2	+Time A Reset	BB150	A2R4 B02	R
3	+Even SR Register	BC160	A2S2 U07	F
4	–FB1	BB100	A2R4 B03	M
5	–ECC SR 47 Pwr	BB140	A2R4 D04	T
6	+ECC Tie Up	BB110	A2R4 D10/B09	Q
7	–Shift Reg Parity	BC100	A2S2 B12	H
8	+Time B Response	BC160	A2S2 S08	J
9	+Time C	BB100	A2R4 B10	P
10	–Zeros Detect SR 0 to 47	BC150	A2S2 S05	S
11	–Run ECC	BC150	A2S2 M09	K
12	+Reset Fast Sync	BC140	A2S2 M12	E
13	–Data Good	BC110	A2S2 U03	L
14	–ECC Zeros Compare	BC150	A2S2 U06	G
15	–ECC Ser Rd Data	BB100	A2R4 B07	N
16	–Status Bytes Op 04	BF110	A2G2 G03	C
17	–Phy Index	BH170	A2Q2 S07	B



Line keys reference the diagram on DATA 154.

CE0207 Seq. 1 of 1	2358509 Part No.	441300 31 Mar 76	441303 30 Jul 76			

ECC PATTERN REGISTER

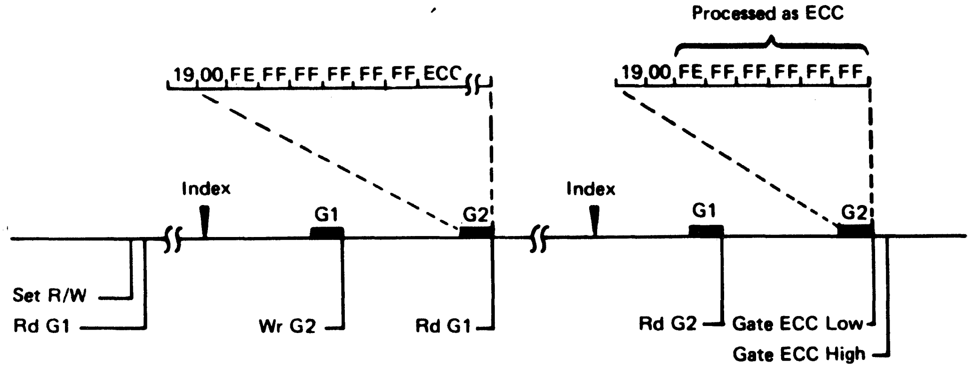
ERROR DESCRIPTION

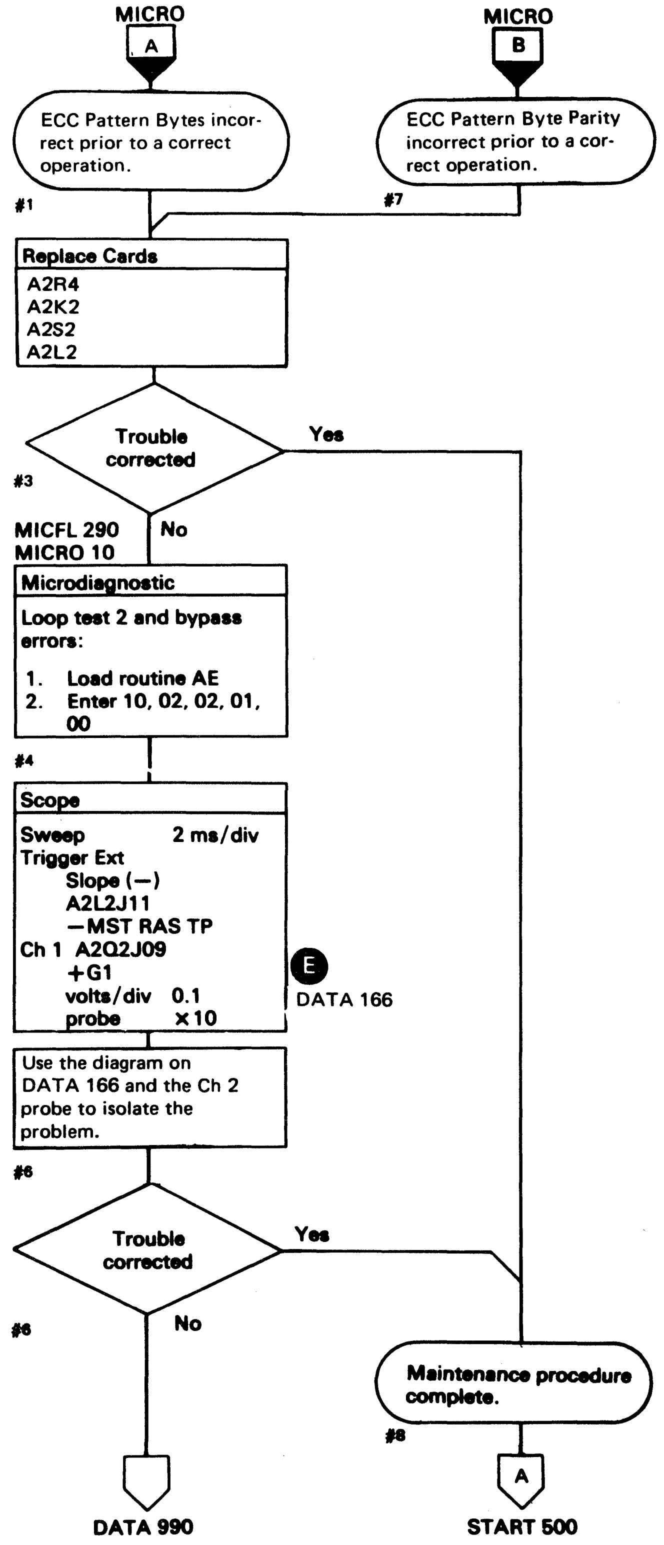
Routine AE, test 2 writes a record that when read, causes the ECC pattern bytes to be set to 'F5FD'. The commands Gate ECC Low and Gate ECC High are used to fetch the information for testing. This is a test for missing bits; extra bits would have been detected in test 1.

To analyze the problem, determine the missing bits by comparing the received value with the expected value and proceed.

MICRODIAGNOSTIC DESCRIPTION

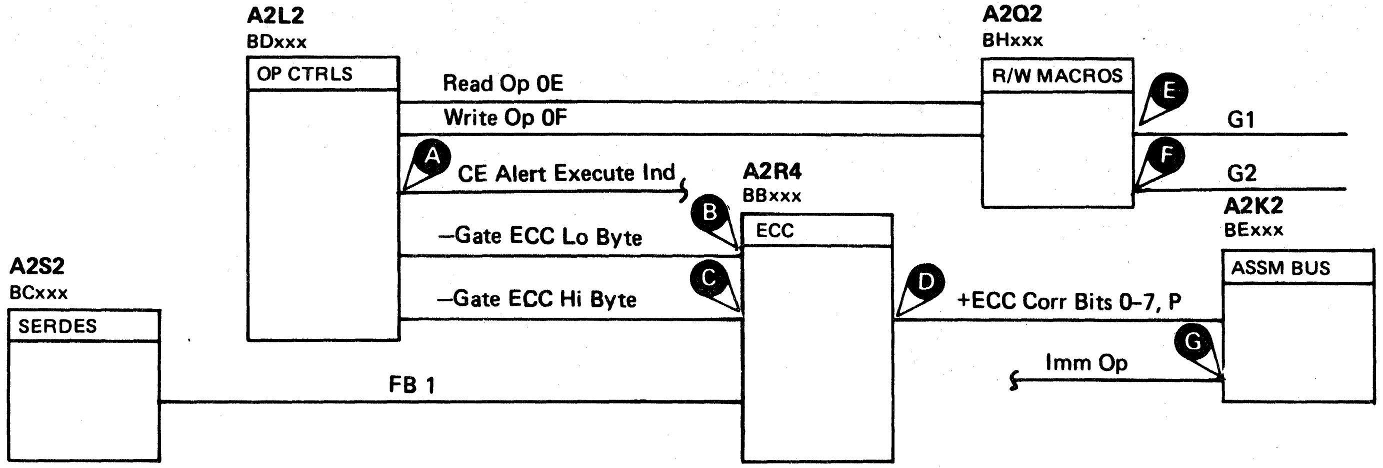
Route AE, test 2 writes an eight-byte record and reads it as a two-byte record. The remaining six bytes are processed as ECC bytes and produce a Data Check condition. The program verifies that the ECC low-pattern byte contains 'F5' and the ECC high-pattern byte contains 'FD'.





AE TEST 2 DIAGRAM

See the sequence chart on DATA 168 for referenced test points.
See OPER 235 for theory.



CE0208 Seq. 2 of 2	2358510 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AE TEST 2 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

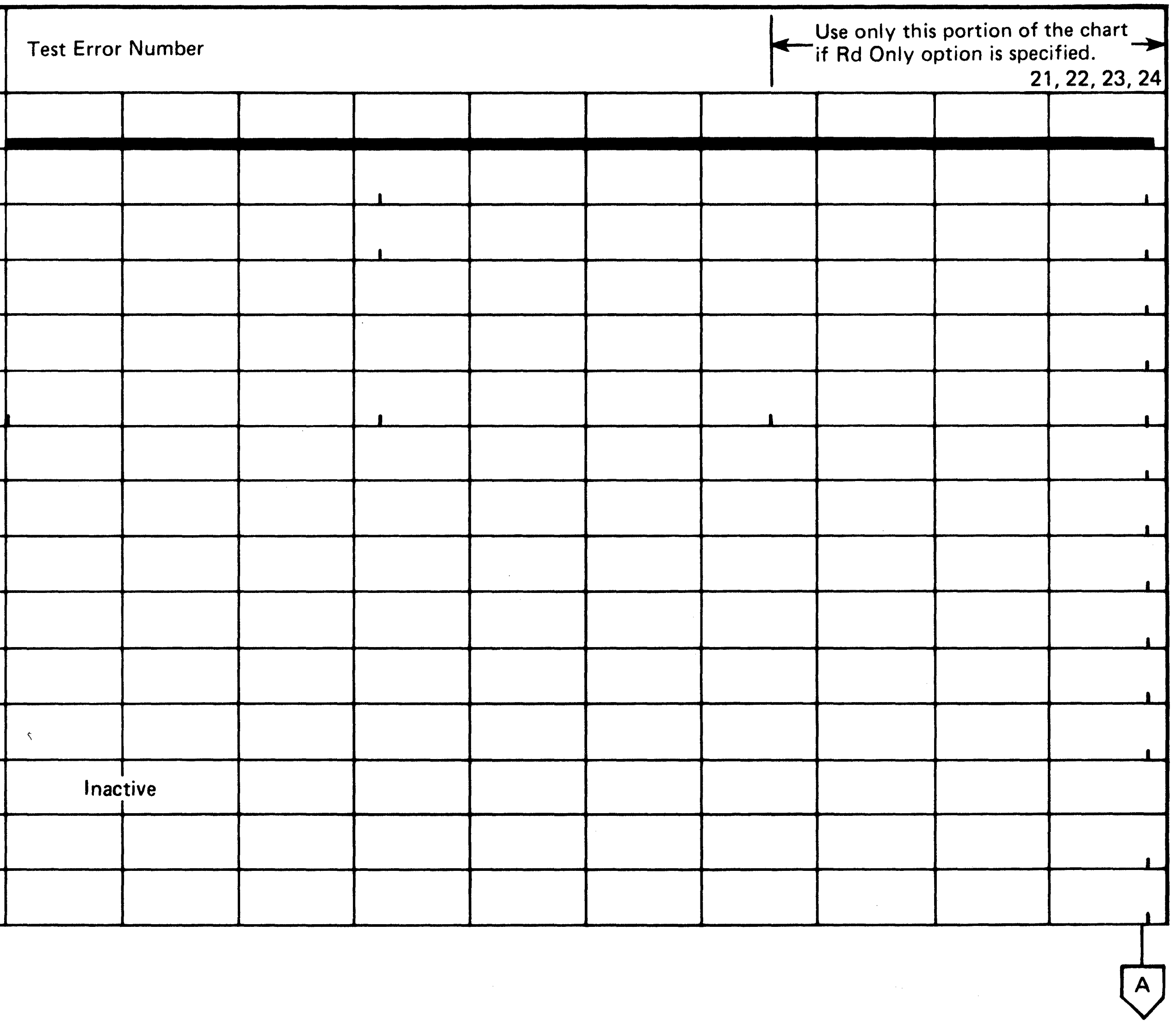
Routine AE, test 2
1. Load AE
2. Enter 10,02,00,00

Scope Setup

Sweep	5 ms/div	Ch 1 A2U4D13 +CE Alert Execute Ind	
Mode	Alt or Chop		
Trigger	Ext	Volts/div	0.1
	Slope (+)	Probe	x10
	A2L2D13 +CE Alert Execute Ind	Ch 2 (See chart)	

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	Ⓐ
2	+G1	BH120	A2Q2 J09	Ⓔ
3	−G2	BH110	A2Q2 D05	Ⓕ
4	−Gate ECC Lo Byte	BB160	A2R4 G10	Ⓑ
5	−Gate ECC Hi Byte	BB160	A2R4 G11	Ⓒ
6	−Imm Op	BE140	A2K2 B07	Ⓖ
7	+ECC Corr Bit 0	BB170	A2R4 J04	Ⓓ
8	+ECC Corr Bit 1	BB170	A2R4 J13	
9	+ECC Corr Bit 2	BB170	A2R4 G09	
10	+ECC Corr Bit 3	BB170	A2R4 J06	
11	+ECC Corr Bit 4	BB170	A2R4 J05	
12	+ECC Corr Bit 5	BB170	A2R4 J03	
13	+ECC Corr Bit 6	BB170	A2R4 G03	
14	+ECC Corr Bit 7	BB160	A2R4 G13	
15	+ECC Corr Bit P	BB170	A2R4 D09	↓



Line keys reference the diagram on DATA 166.

DATA 170
(For expanded
sequence chart)

AE TEST 2 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

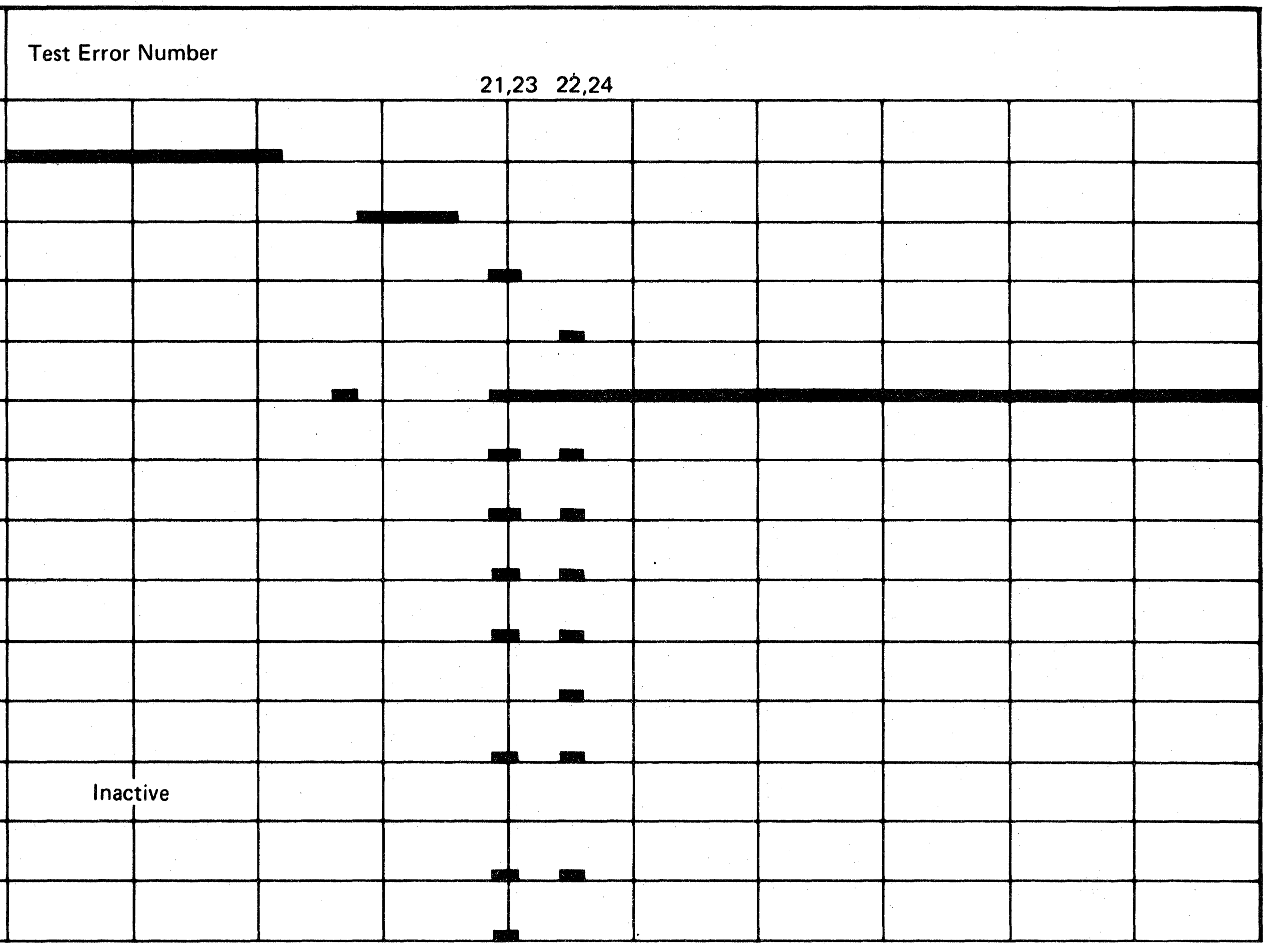
Sweep	5 ms/div	Ch 1 A2Q2J09		
Mode	Alt or Chop	+G1		
Trigger	Ext	Volts/div	0.1	
	Slope (+)	Probe	x10	
	A2L2D13	Ch 2 (See chart)		
	+CE Alert Execute Ind			

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 9.0
Source – Int Ch 1

DATA 168
A

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+G1	BH120	A2Q2 J09	Ⓔ
2	–G2	BH110	A2Q2 D05	Ⓕ
3	–Gate ECC Lo Byte	BB160	A2K4 G10	Ⓑ
4	–Gate ECC Hi Byte	BB160	A2R4 G11	Ⓒ
5	–Imm Op	BE140	A2K2 B07	Ⓖ
6	+ECC Corr Bit 0	BB170	A2R4 J04	Ⓓ
7	+ECC Corr Bit 1	BB170	A2R4 J13	
8	+ECC Corr Bit 2	BB170	A2R4 G09	
9	+ECC Corr Bit 3	BB170	A2R4 J06	
10	+ECC Corr Bit 4	BB170	A2R4 J05	
11	+ECC Corr Bit 5	BB170	A2R4 J03	
12	+ECC Corr Bit 6	BB170	A2R4 G03	
13	+ECC Corr Bit 7	BB160	A2R4 G13	
14	+ECC Corr Bit P	BB170	A2R4 D09	



Line keys reference the diagram on DATA 166.

3350	CE0212 Seq. 2 of 2	2358511 Part No.	441300 31 Mar 76	441303 30 Jul 76			

BUS IN NON ZERO ON NORMAL END

ERROR DESCRIPTION

Bus In should always be zero when Normal End is active. Routine AE, test 3 tests for zero.

Lost Orientation is an indication that the controller is no longer synchronized with the disk. It should only be presented at Tag Valid time.

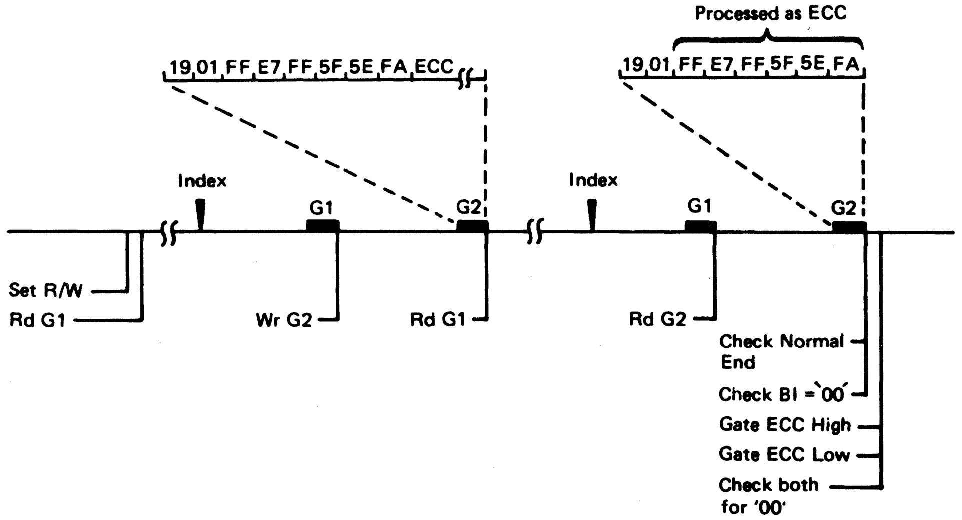
Status Overrun signals storage control that a Command Overrun should be presented to the channel. During a chained reselection sequence, when storage control receives Command Out, the command is decoded and an operation code is sent to the controller. Storage control responds to Command Out with Status In and expects to receive Service Out from the channel. While waiting for Service Out, storage control holds Tag Gate active. If Tag Gate is active too long, the channel is late with Service Out.

No Sync Found and Data Found are used by the microprogram to determine the reason for the No Sync Byte Found indication.

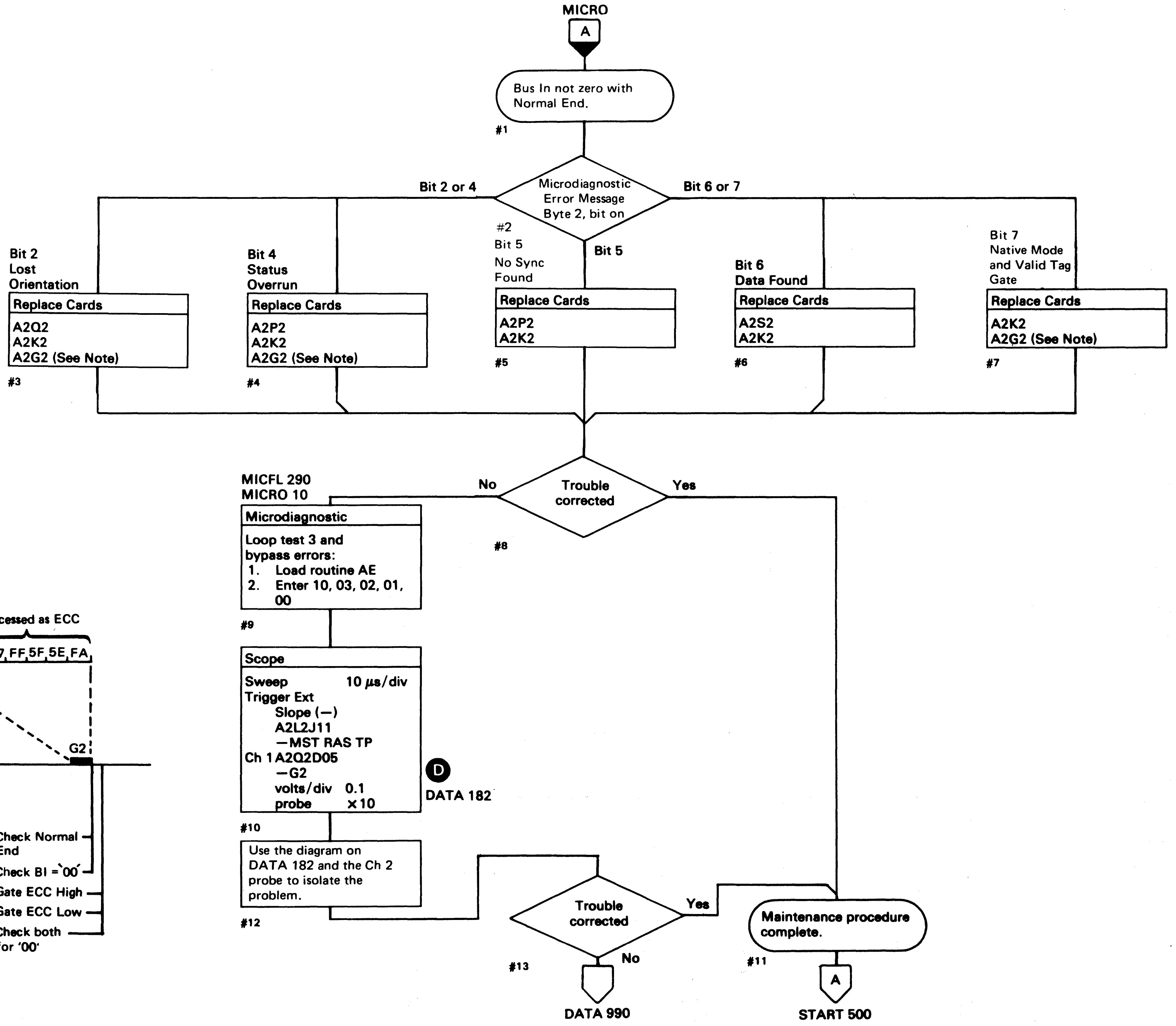
Native Mode and Valid Tag Gate indicate Native Mode at Tag Gate time.

MICRODIAGNOSTIC DESCRIPTION

Routine AE, test 3 writes an eight-byte record and reads it as a two-byte record. The remaining six bytes are processed as an ECC byte and it is expected to produce a Normal End, Pattern byte equal to zero, and Zero Detected latch on.



Note: *When replacing A2G2, check the address jumpers. See INST 6.*



ECC DATA CHECK

ERROR DESCRIPTION

The ECC control allows the serial data bits read from the disk to shift through the ECC Shift Register until the end of the data field.

After the end of data is reached, the six ECC bytes are shifted through the ECC Shift Register. If there are no data errors, the ECC Shift Register is zero and ECC Zeros Compare is active.

The absence of ECC Zeros Compare at the end of a Read operation sets the ECC Data Check latch causing Check End to be generated.

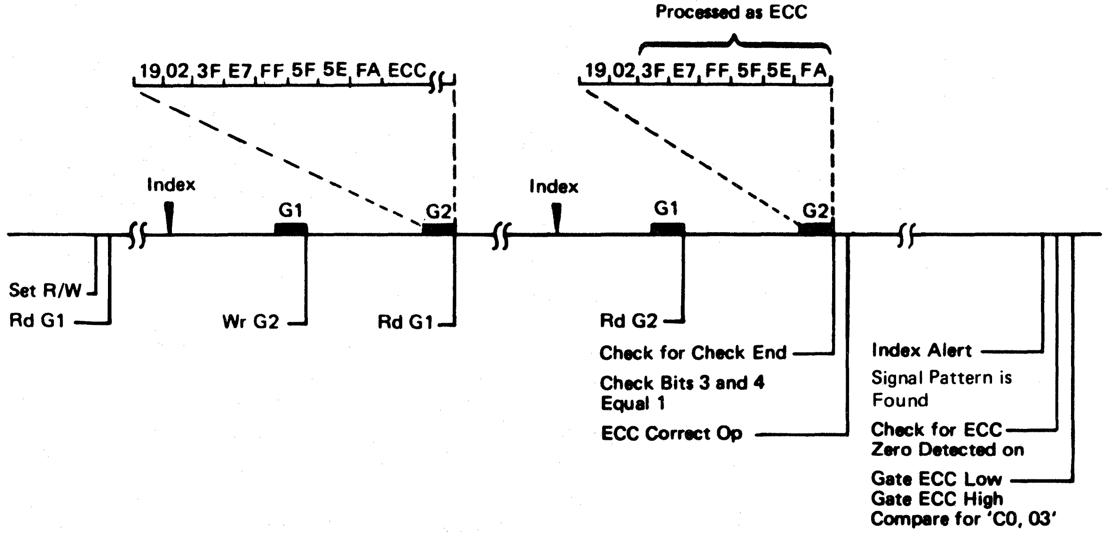
When Check End is active, Bus In bit 3 indicates ECC Data Check.

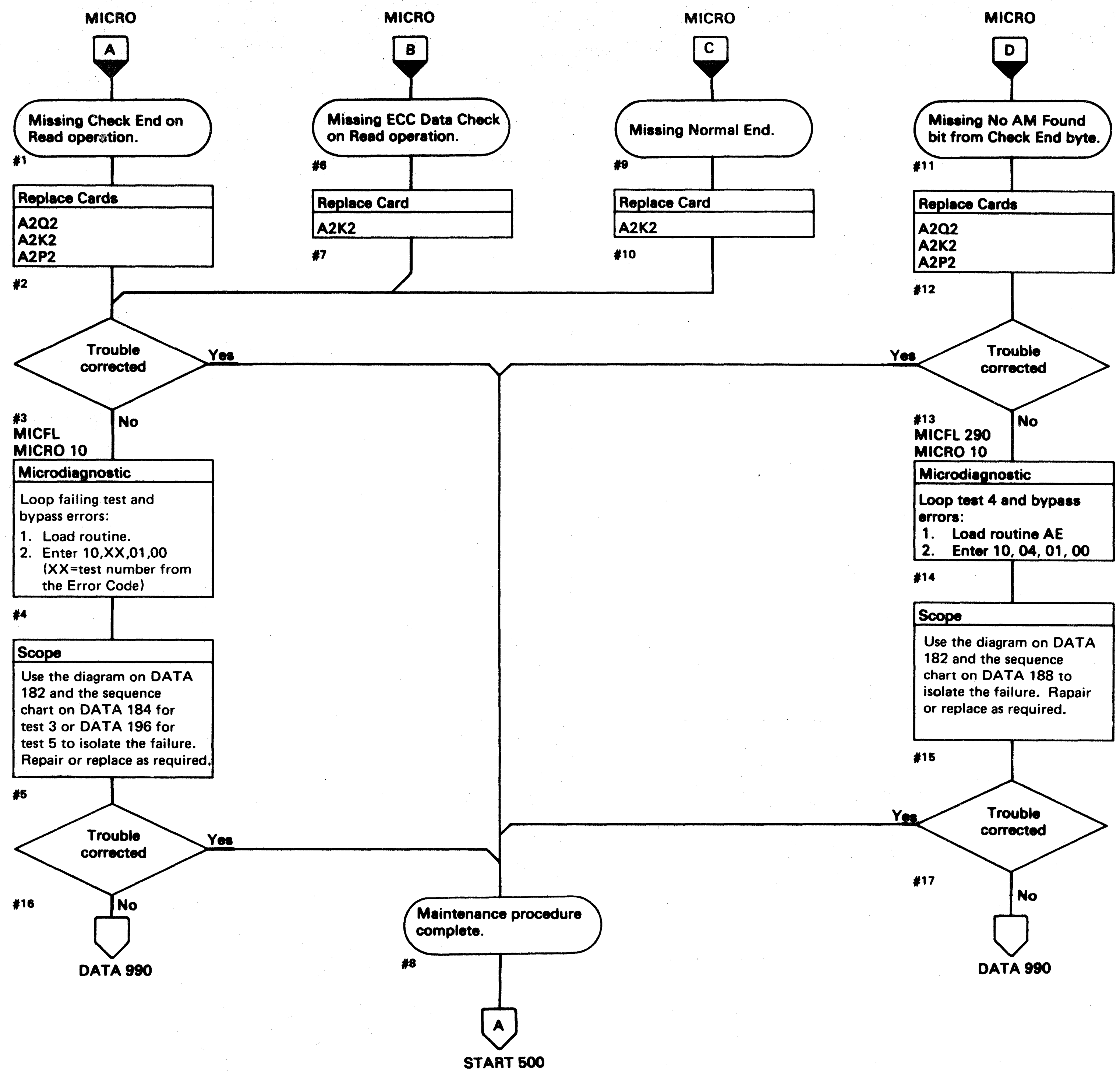
See OPER 235 for a description of Error Correction.

MICRODIAGNOSTIC DESCRIPTION

Routine AE, test 4 writes an eight-byte record which is read as a two-byte record. The remaining six bytes are processed as ECC bytes and are expected to produce Check End. The ECC Data Check (bit 3) and bit 4, which is used as a Redundant Data Check indication, should be on.

An ECC Correct Op is initiated. The result should be a Correctable Data Check, indicated by an Index Alert. The Pattern register is checked for proper values and the state of the Zeros Detected bit is verified.





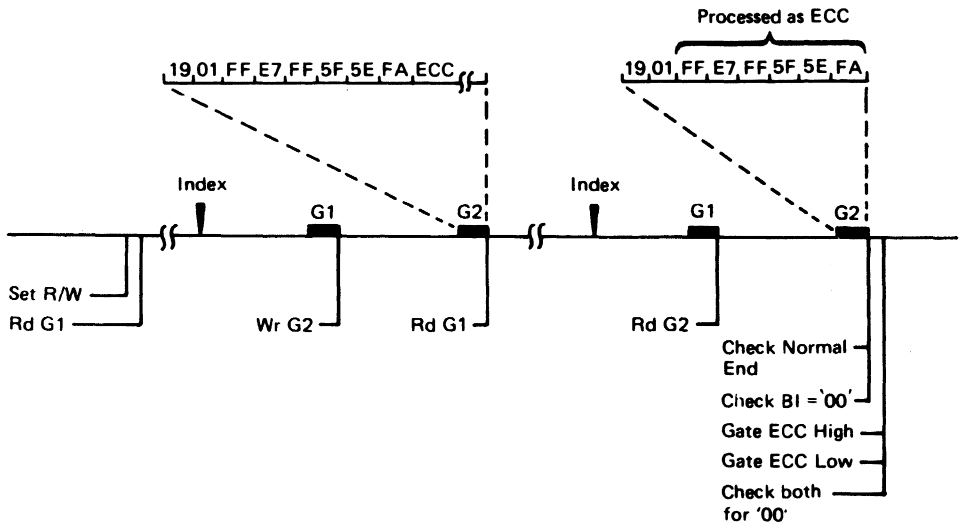
ECC PATTERN BYTE ERRORS

ERROR DESCRIPTION

During the ECC circuit test, the ECC pattern bytes are sensed and compared with known values. If they do not compare, an error is posted. In routine AE, test 3, they are expected to be '0000'. In routine AE, test 4, the high and low bytes are expected to be '03C0', respectively.

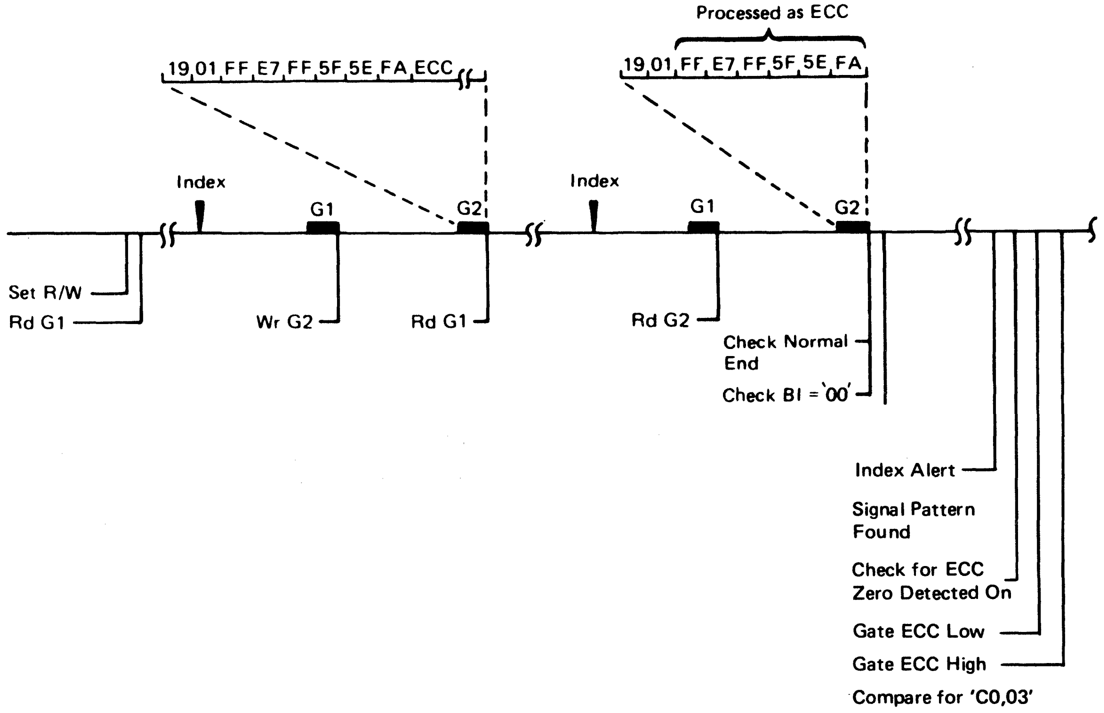
MICRODIAGNOSTIC DESCRIPTION

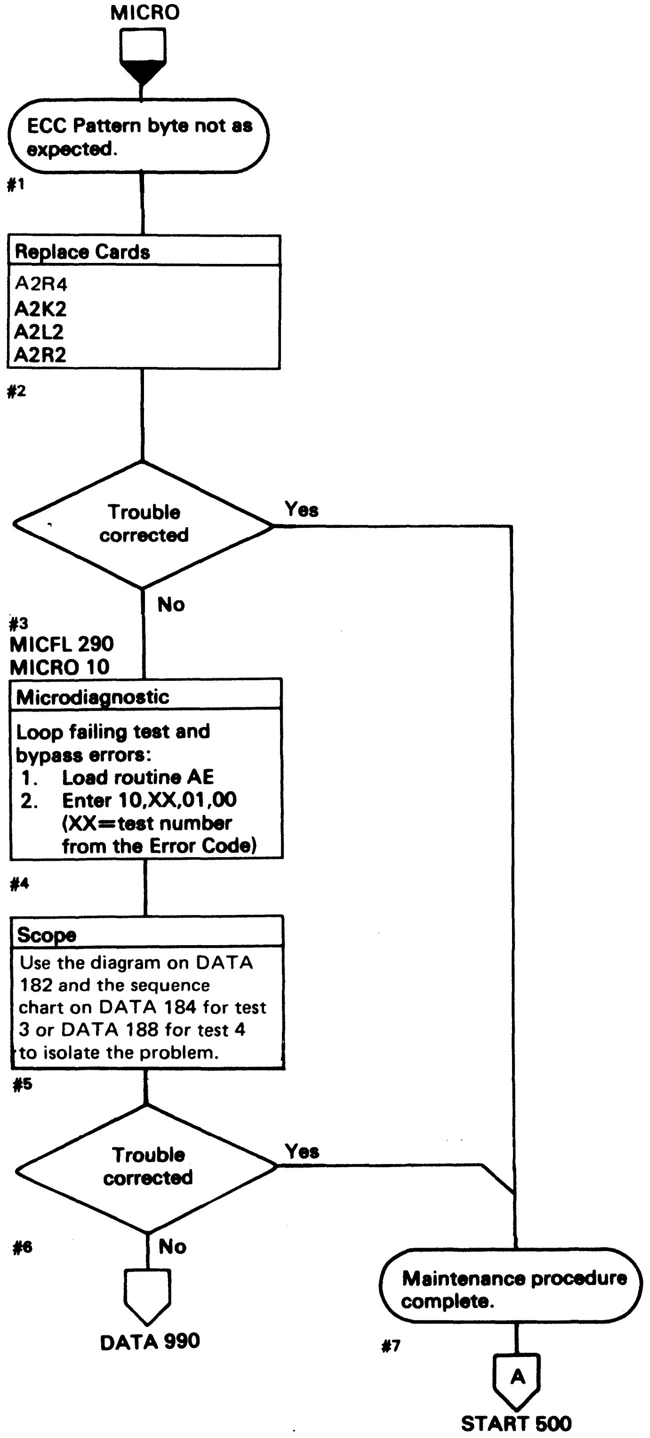
Routine AE, test 3 writes an eight-byte record and reads it as a two-byte record. The remaining six bytes are processed as ECC bytes and are expected to produce a Normal End, Pattern byte equal to zero, and Zero Detected latch on.



Routine AE, test 4 writes an eight-byte record which is read as a two-byte record. The remaining six bytes are processed as ECC bytes and are expected to produce Check End. The ECC Data Check (bit 3) and bit 4, which is used as a Redundant Data Check indication, should be on.

An ECC Correct Op is initialized. The result should be a Correctable Data Check indicated by an Index Alert. The Pattern register is checked for proper values and the state of the Zeros Detected bit is verified.

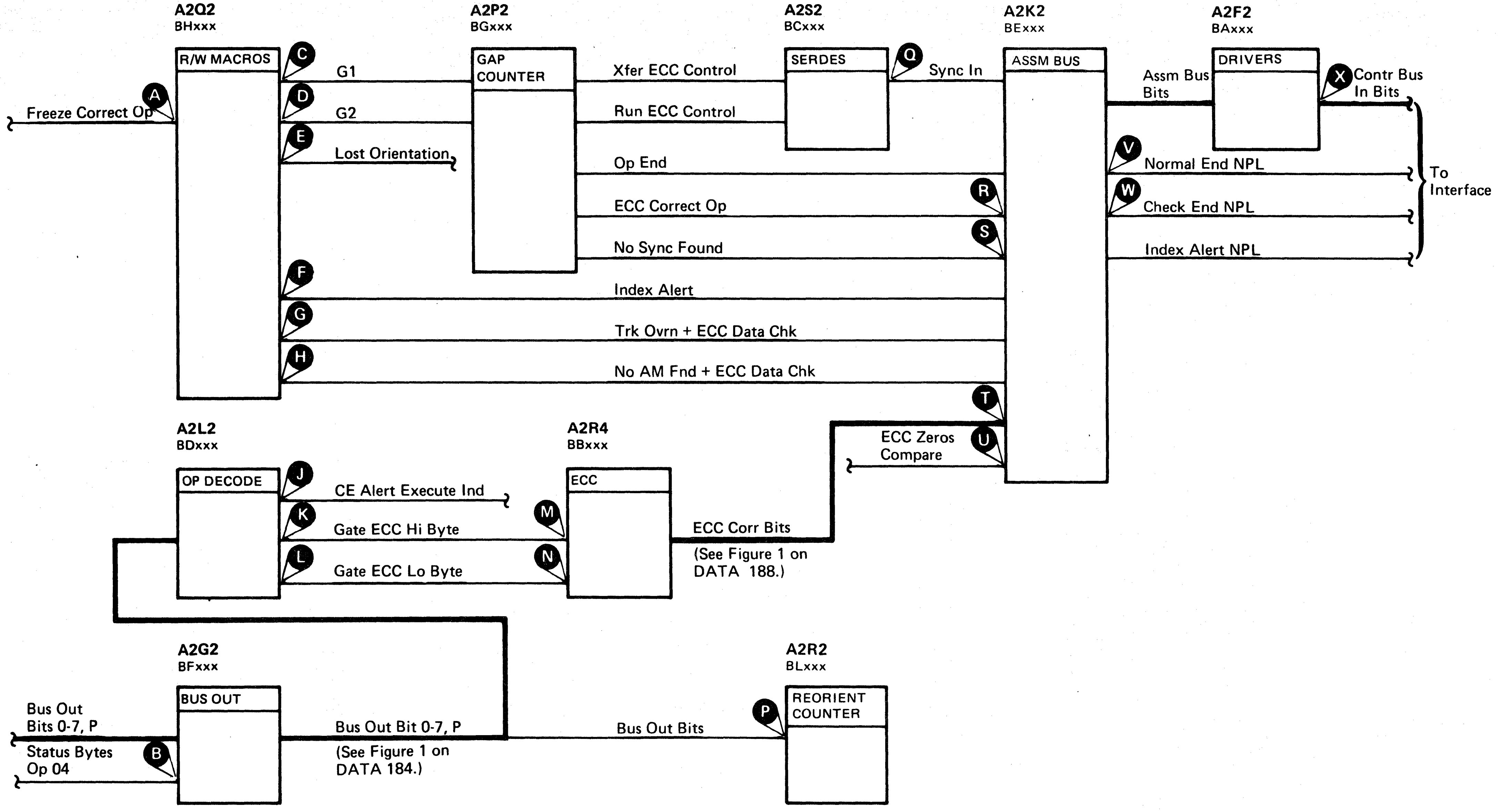




AE TEST 3, 4, and 5 DIAGRAM

See the sequence charts on DATA 184, 188, and 196 for referenced test points.

See OPER 235 for theory.



AE TEST 3 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AE, test 3
1. Load AE
2. Enter 10,03,00,00

Scope Setup

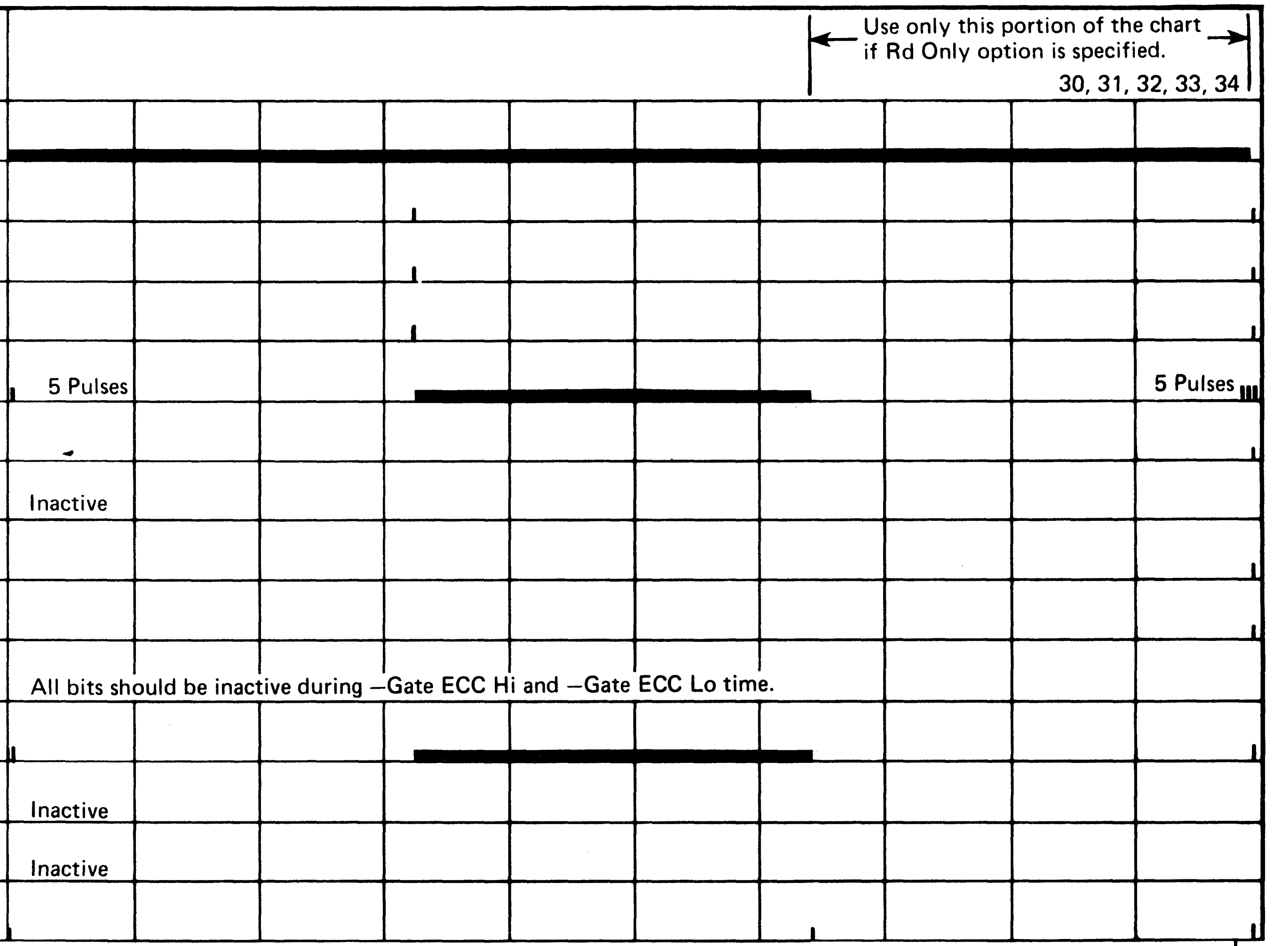
Sweep 5 ms/div
Mode Alt or Chop

Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend:
□ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	J
2	+G1	BH120	A2Q2 J09	C
3	–G2	BH110	A2Q2 D05	D
4	–Sync In	BC170	A2S2 S10	Q
5	+Normal End NPL	BE160	A2K2 D11	V
6	–Status Bytes Op 04	BF110	A2G2 G03	B
7	–ECC Zeros Compare	BE120	A2K2 S09	U
8	–Gate ECC Hi Byte	BB160	A2R4 G11	M
9	–Gate ECC Lo Byte	BB160	A2R4 G10	N
10	–Contr Bus In Bits (0-6)	BA100	See Figure 1	X
11	–Contr Bus In Bit 7	BA100	A2F2 U06	X
12	–No Sync Found	BE120	A2K2 P03	S
13	+Check End NPL	BE160	A2K2 D05	W
14	–Lost Orientation	BH130	A2Q2 U07	E



Line keys reference the diagram on DATA 192.

A
DATA 186
(For expanded sequence chart)

Figure 1. Controller Bus In Bits

Line Name	Test Point
–Contr Bus In Bit 0	A2F2 P05
1	M10
2	M08
3	S07
4	P06
5	U03
6	P09
7	U06
8	J08

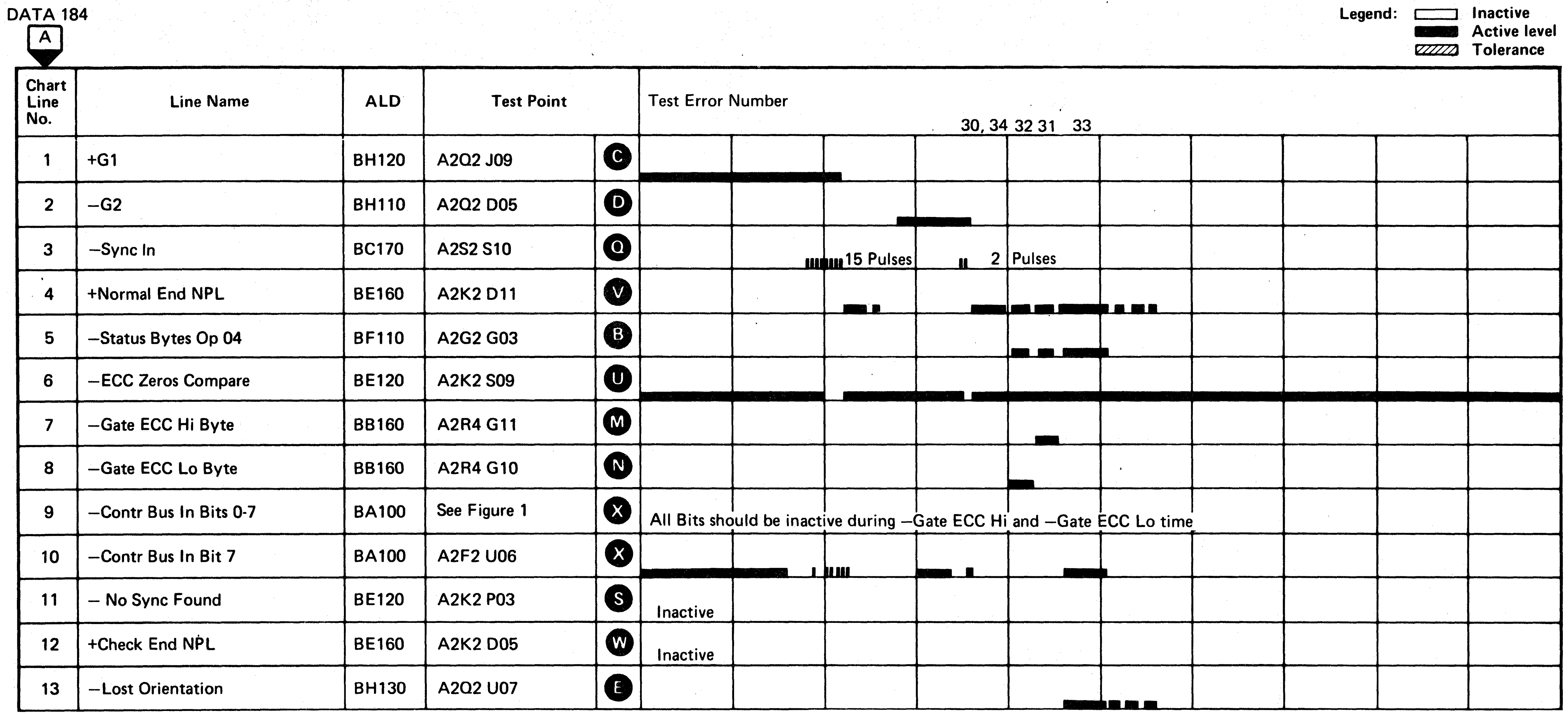
AE TEST 3 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 9.0
Source – Int Ch 1

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)



Legend: ▭ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+G1	BH120	A2Q2 J09	C	
2	–G2	BH110	A2Q2 D05	D	
3	–Sync In	BC170	A2S2 S10	Q	15 Pulses 2 Pulses
4	+Normal End NPL	BE160	A2K2 D11	V	
5	–Status Bytes Op 04	BF110	A2G2 G03	B	
6	–ECC Zeros Compare	BE120	A2K2 S09	U	
7	–Gate ECC Hi Byte	BB160	A2R4 G11	M	
8	–Gate ECC Lo Byte	BB160	A2R4 G10	N	
9	–Contr Bus In Bits 0-7	BA100	See Figure 1	X	All Bits should be inactive during –Gate ECC Hi and –Gate ECC Lo time
10	–Contr Bus In Bit 7	BA100	A2F2 U06	X	
11	– No Sync Found	BE120	A2K2 P03	S	Inactive
12	+Check End NPL	BE160	A2K2 D05	W	Inactive
13	–Lost Orientation	BH130	A2Q2 U07	E	

Line keys reference the diagram on DATA 182.

Figure 1. Controller Bus In Bits

Line Name	Test Point	
–Contr Bus In Bit 0	A2F2	P05
1		M10
2		M08
3		S07
4		P06
5		U03
6		P09
7		U06
8		J08

3350	CE0226 Seq. 2 of 2	2358574 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AE TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AE, test 4
1. Load AE
2. Enter 10,04,00,00

Scope Setup

Sweep 10 ms/div
Mode Alt or Chop

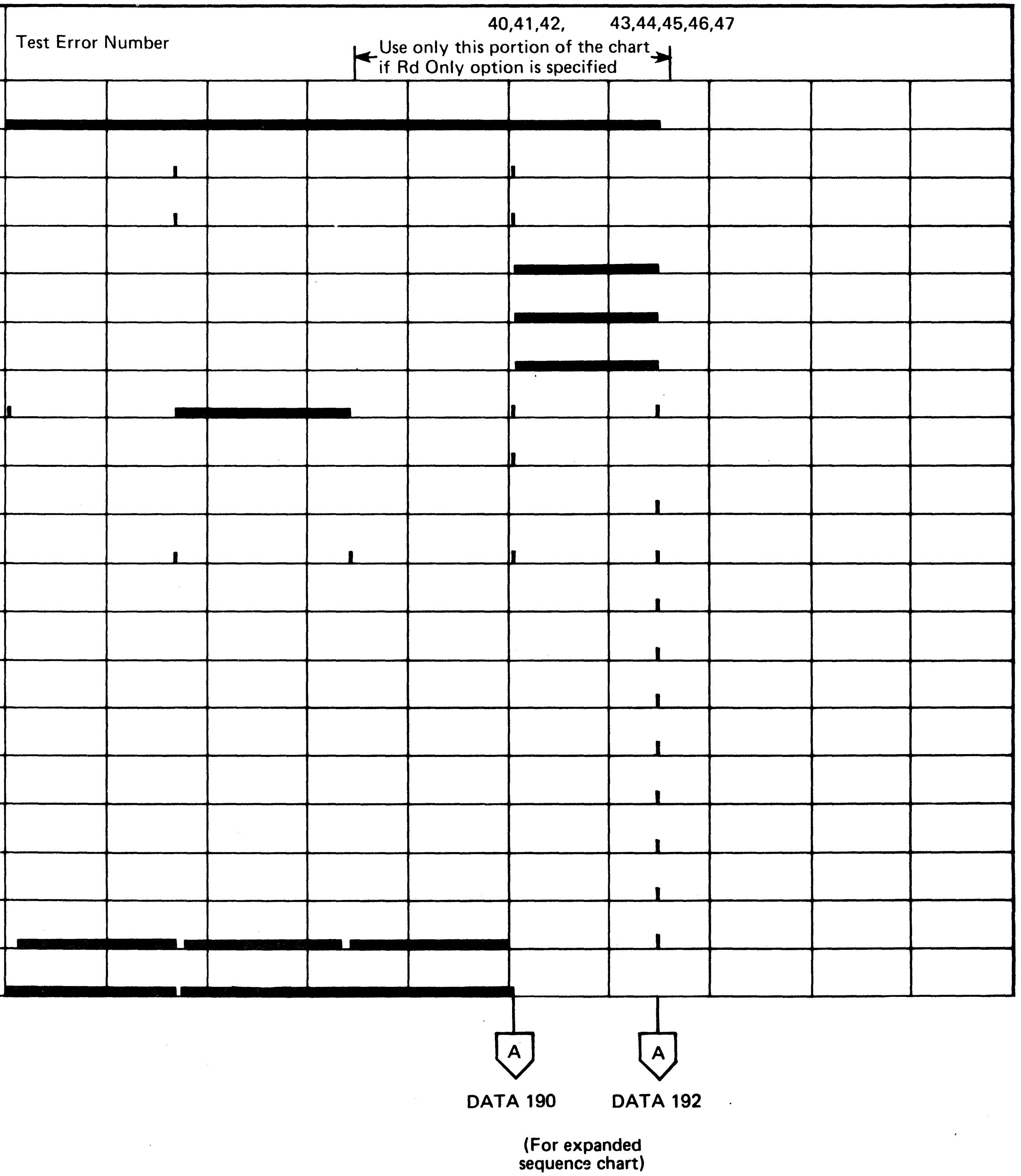
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend:
▭ Inactive
▬ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	J
2	+G1	BH120	A2Q2 J09	C
3	−G2	BH110	A2Q2 D05	D
4	−Trk Ovrn * ECC Data Chk	BH140	A2Q2 J05	G
5	−No AM End * ECC Data Chk	BH140	A2Q2 J13	H
6	−ECC Correct Op	BE120	A2K2 U07	R
7	+Normal End NPL	BE160	A2K2 D11	V
8	+Check End NPL	BE160	A2K2 D05	W
9	−Freeze Correct Op	BH150	A2Q2 U05	A
10	−Index Alert	BH170	A2Q2 J11	F
11	−Status Byte Op 04	BF110	A2G2 G03	B
12	−Gate ECC Lo Byte	BD100	A2L2 P10	L
13	−Gate ECC Hi Byte	BD100	A2L2 M13	K
14	+ECC Corr Bit 0	BE100	A2K2 D03	T
15	+ECC Corr Bit 1	BE110	A2K2 G09	
16	+ECC Corr Bit 6	BE110	A2K2 B04	
17	+ECC Corr Bit 7	BE110	A2K2 J04	
18	−Bus Out Bit 5	BL130	A2R2 J11	
19	−ECC Zeros Compare	BE120	A2K2 S09	V



Use only this portion of the chart if Rd Only option is specified

(For expanded sequence chart)

Line keys reference the diagram on DATA 182.

3350 | CE0228 Seq. 1 of 2 | 2358575 Part No. | 441300 31 Mar 76 | 441303 30 Jul 76

AE TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 10 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

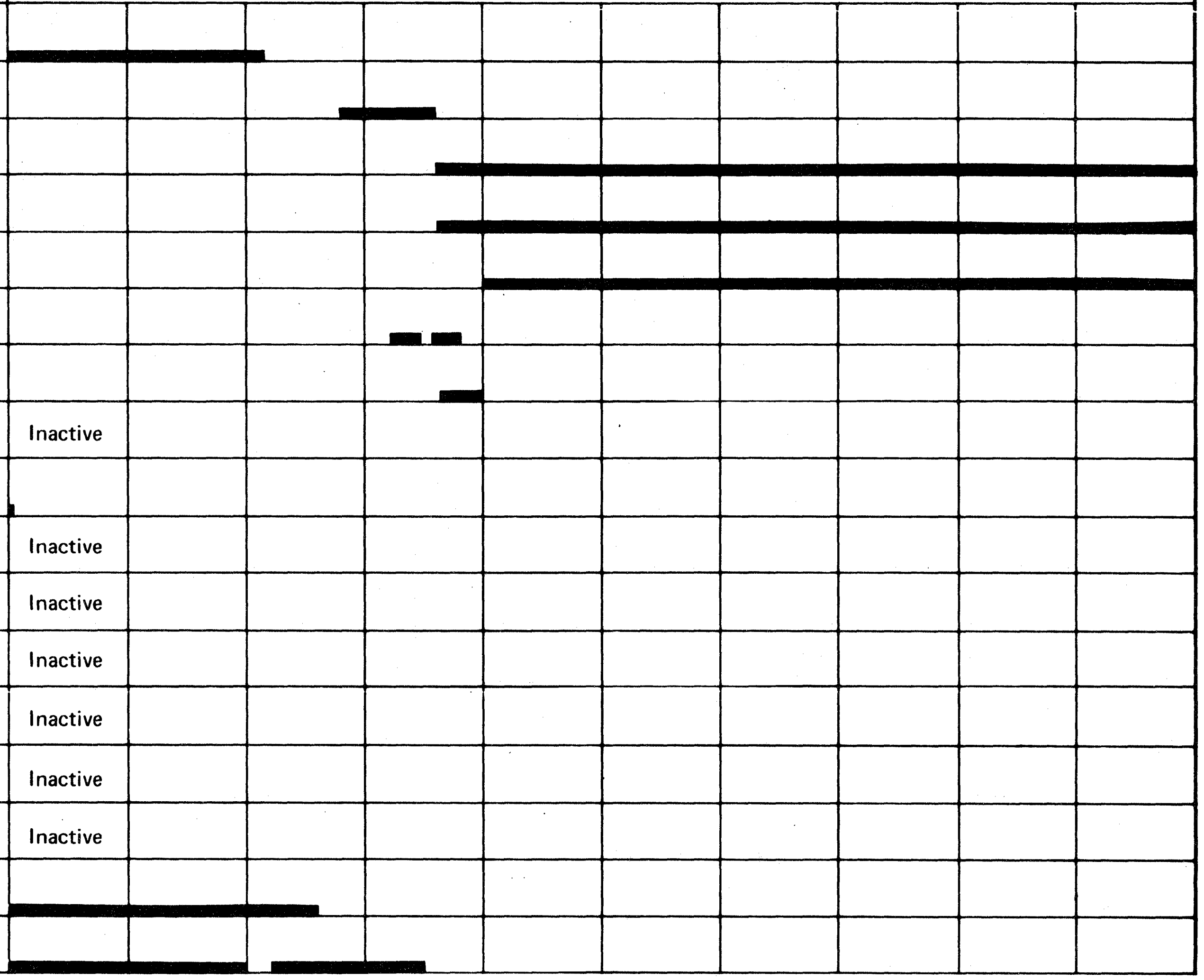
Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 10 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 4.5
Source – Int Ch 1

DATA 188
A

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 40,41,42
1	+G1	BH120	A2Q2 J09	C	
2	–G2	BH110	A2Q2 D05	D	
3	–Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	G	
4	–No AM Fnd *ECC Data Chk	BH140	A2Q2 J13	H	
5	–ECC Correct Op	BE120	A2K2 U07	R	
6	+Normal End NPL	BE160	A2K2 D11	V	
7	+Check End NPL	BE160	A2K2 D05	W	
8	–Freeze Correct Op	BH150	A2Q2 U05	A	Inactive
9	–Index Alert	BH170	A2Q2 J11	F	
10	–Status Byte Op O4	BF110	A2G2 G03	B	Inactive
11	–Gate ECC Lo Byte	BD100	A2L2 P10	L	Inactive
12	–Gate ECC Hi Byte	BD100	A2L2 M13	K	Inactive
13	+ECC Corr Bit 0	BE110	A2K2 G09	T	Inactive
14	+ECC Corr Bit 6	BE110	A2K2 B04		Inactive
15	+ECC Corr Bit 7	BE110	A2K2 J04		Inactive
16	–Bus Out Bit 5	BL130	A2R2 J11		
17	–ECC Zeros Compare	BE120	A2K2 S09	U	



Line keys reference the diagram on DATA 182.

AE TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

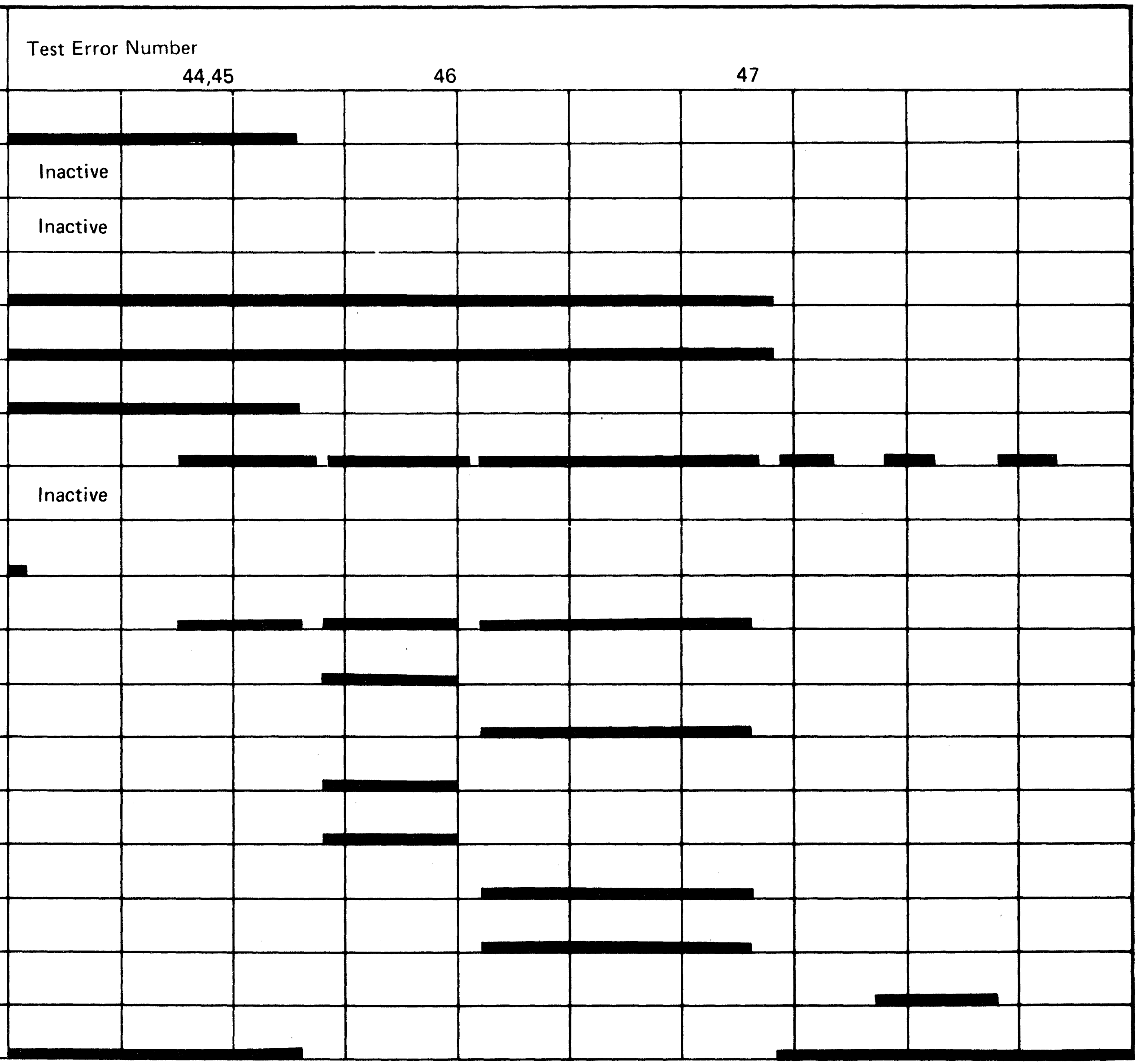
Sweep	10 ms/div	Ch 1 A2Q2U05	
		-Freeze Correct Op	
Mode	Alt or Chop	Volts/div	0.1
Trigger	Ext	Probe	x10
	Slope (+)	Ch 2 (See chart)	
	A2L2D13		
	+CE Alert Execute Ind		

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 10 ms/div
Slope (-)
Delay Time-Delayed Sweep – 10 μs/div
Delay-Time Multiplier – 6.0
Source – Int Ch 1

DATA 188
A

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	–Freeze Correct Op	BH150	A2Q2 U05	A
2	+ G1	BH120	A2Q2 J09	C
3	–G2	BH110	A2Q2 D05	D
4	–Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	G
5	–No AM Fnd*Data Chk	BH140	A2Q2 J13	H
6	–ECC Correct Op	BE120	A2K2 U07	R
7	+Normal End NPL	BE160	A2K2 D11	V
8	+Check End NPL	BE160	A2K2 D05	W
9	–Index Alert	BH170	A2Q2 J11	F
10	–Status Byte Op 04	BF110	A2G2 G03	B
11	–Gate ECC Lo Byte	BD100	A2L2 P10	L
12	–Gate ECC Hi Byte	BD100	A2L2 M13	K
13	+ECC Corr Bit 0	BE110	A2K2 D03	T
14	+ECC Corr Bit 1	BE110	A2K2 G09	
15	+ECC Corr Bit 6	BE110	A2K2 B04	
16	+ECC Corr Bit 7	BE110	A2K2 J04	
17	–Bus Out Bit 5	BL130	A2R2 J11	
18	–ECC Zeros Compare	BE120	A2K2 S09	U



Line keys reference the diagram on DATA 182.

AE TEST 5 SEQUENCE CHART

Routine AE, test 5 writes a record which, when read back, activates an ECC Data Check. An ECC Data Check activates Check End. Failure to receive ECC Data Check results in Test Error Number 51. Failure to receive Check End results in Test Error Number 50.

The program issues an ECC Correct Op. Normal End, following the ECC Correct Op, means that the Data Check is not correctable, ECC Zeros Detect should be inactive. Test Error Number 53 indicates a Normal End condition does not exist. Test Error Number 54 indicates that ECC Zeros Detect is active. Test Error Number 52 indicates that the record is correctable.

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AE, test 5
1. Load AE
2. Enter 10,05,00,00

Scope Setup

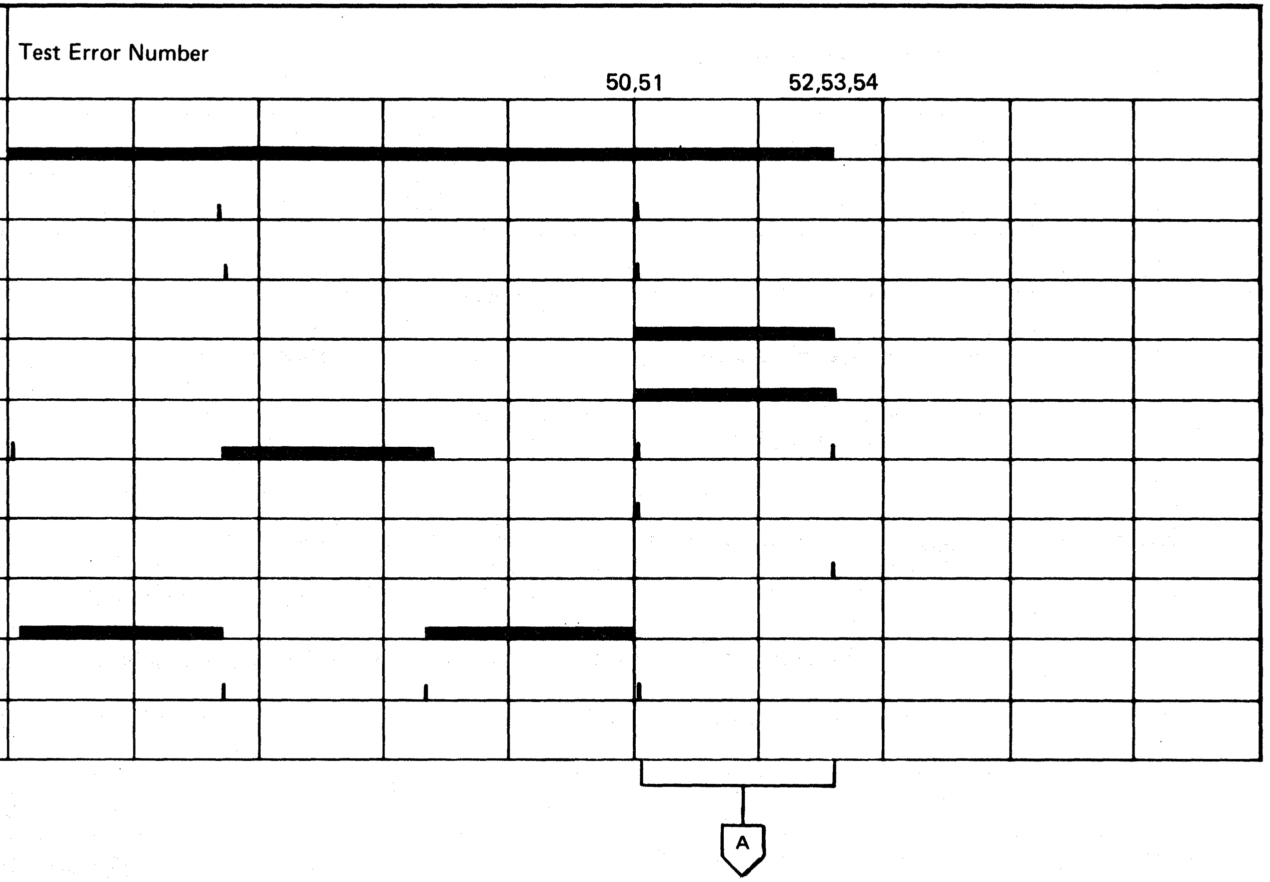
Sweep 10 ms/div
Mode Alt or Chop

Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2L2D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend:
- ▭ Inactive
- ▬ Active level
- ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	J
2	+G1	BH120	A2Q2 J09	C
3	−G2	BH110	A2Q2 D05	D
4	−Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	G
5	−ECC Correct Op	BG170	A2P2 B04	R
6	+Normal End NPL	BE160	A2K2 D11	V
7	+Check End NPL	BE160	A2K2 D05	W
8	−Status Bytes Op 04	BF110	A2G2 G03	B
9	−Contr Bus In Bit 7	BA100	A2F2 U06	X
10	−Index Alert	BH170	A2Q2 J11	F
11	−ECC Zeros Compare	BE120	A2K2 S09	U



Line keys reference the diagram on DATA 182.

DATA 198
(For expanded sequence chart)

3350	CE0230 Seq. 2 of 2	2358576 Part No.	441300 31 Mar 76	441303 30 Jul 76	

AE TEST 5 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

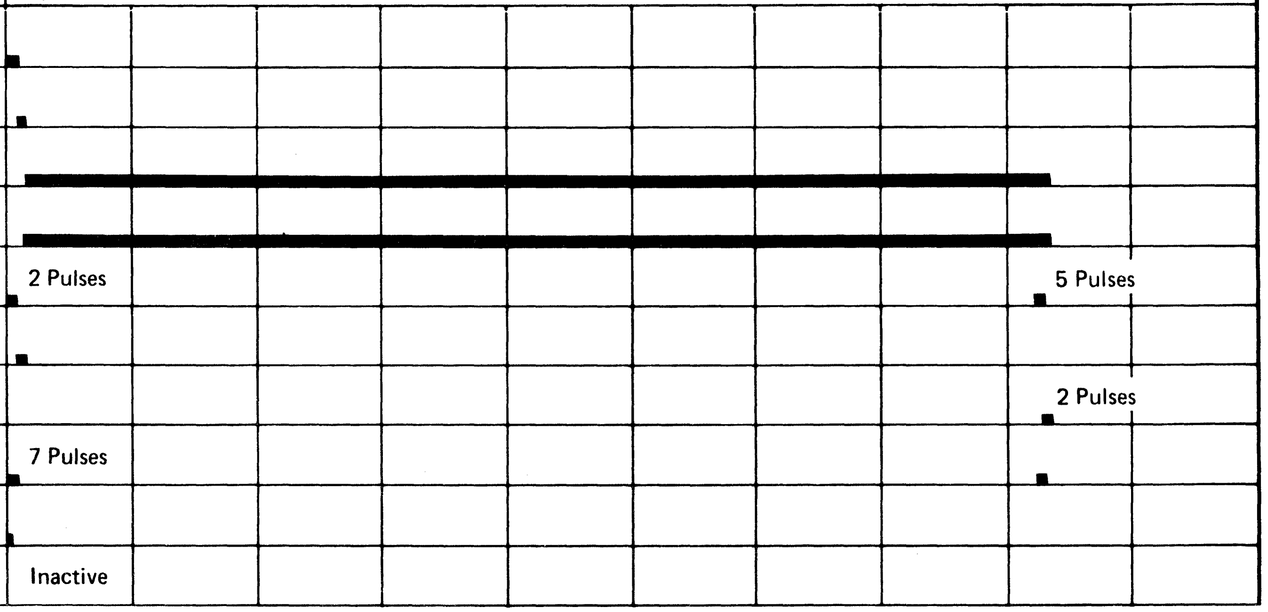
Sweep 10 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 10 ms/div
Slope (+)
Delay Time-Delayed Sweep – 2 ms/div
Delay-Time Multiplier – 4.5
Source – Int Ch 1

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

DATA 196
A

Legend:
□ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 50,51 … 52,53,54
1	+G1	BH120	A2Q2 J09	C	
2	–G2	BH110	A2Q2 D05	D	
3	–Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	G	
4	–ECC Correct Op	BG170	A2K2 U07	R	
5	+Normal End NPL	BE160	A2K2 D11	V	2 Pulses … 5 Pulses
6	+Check End NPL	BE160	A2K2 D05	W	
7	–Status Bytes Op 04	BF110	A2G2 G03	B	2 Pulses
8	–Contr Bus In Bit 7	BA100	A2F2 U06	X	7 Pulses
9	–Index Alert	BH170	A2Q2 J11	F	
10	–ECC Zeros Compare	BE120	A2K2 S09	U	Inactive



Line keys reference the diagram on DATA 182.

ECC SERIALIZATION ERROR

ERROR DESCRIPTION

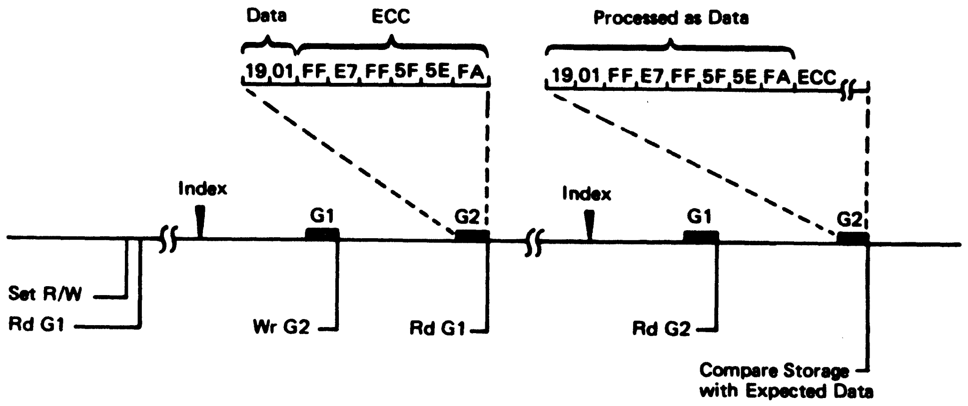
This test writes a two-byte record of '1901'. The ECC Bytes that are written are 'FFE7FF5F5EFA'. The record is then read as an eight-byte record and the Data Check is ignored. The data read is compared with the expected data.

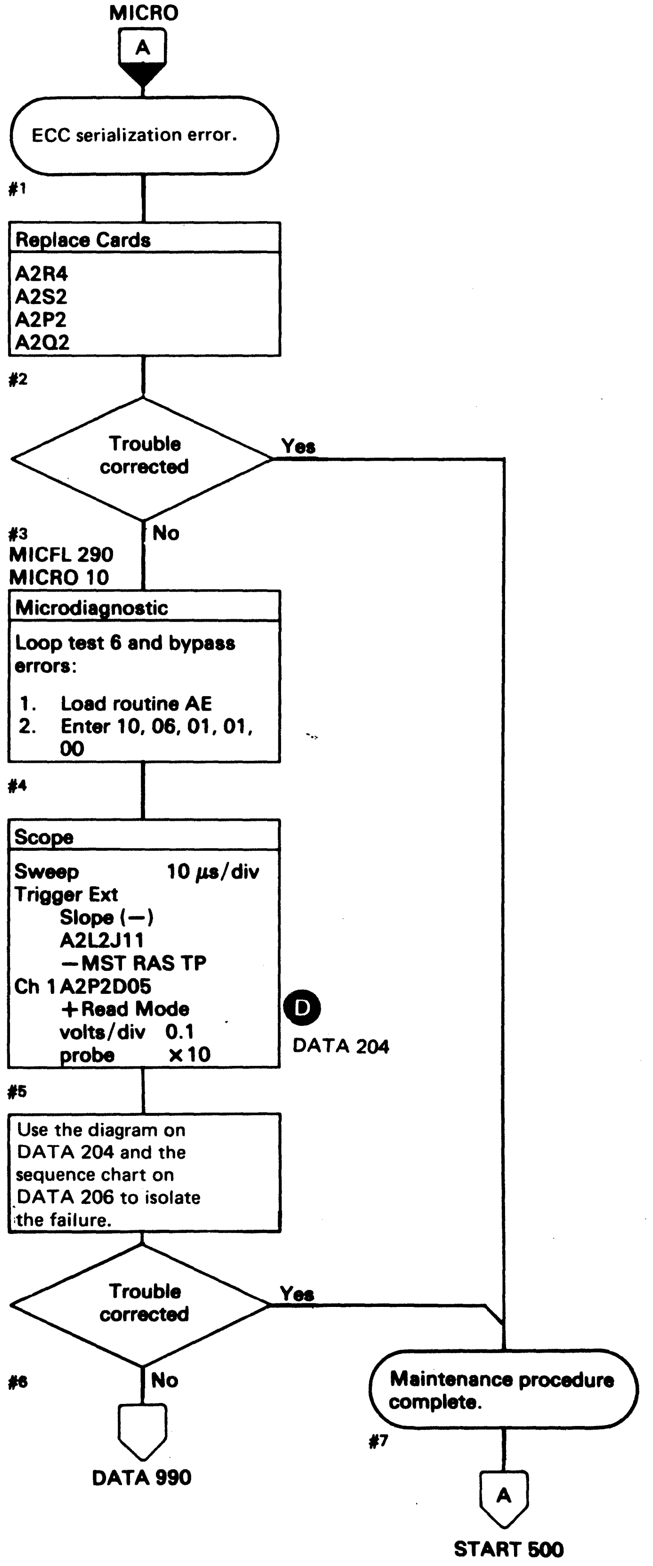
A non-compare indicates a failure to write the ECC bytes properly.

MICRODIAGNOSTIC DESCRIPTION

Routine AE, test 6 writes a two-byte record. The ECC hardware creates the ECC bytes for the record. The record is then read into storage as an eight-byte record and is compared with a known value.

This operation causes a Data Check which is ignored.





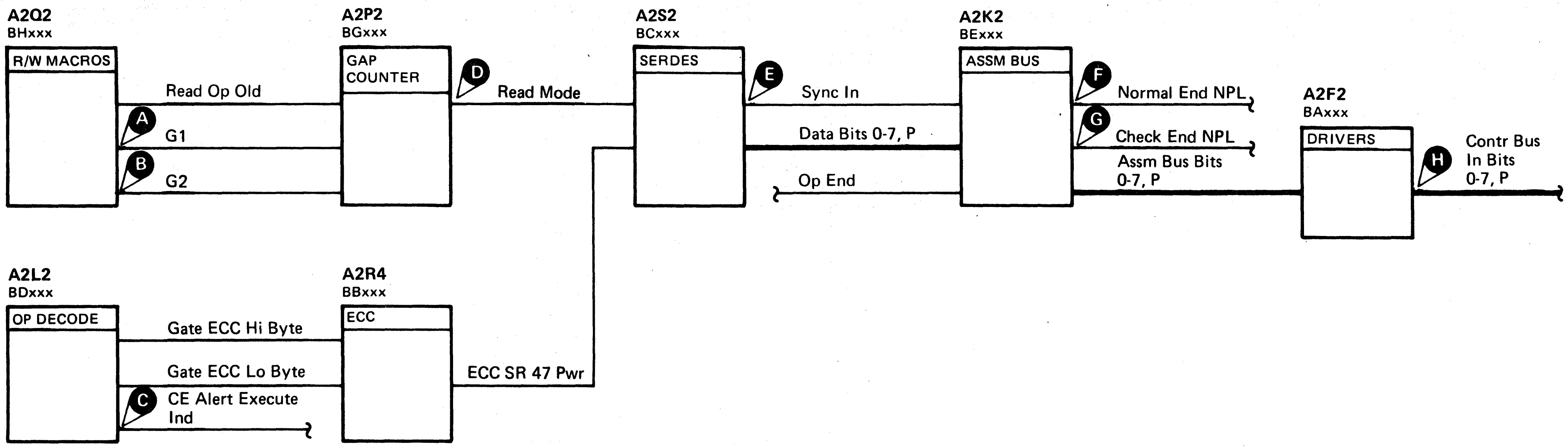
3350

CE0241 Seq. 1 of 2	2358578 Part No.

441300 31 Mar 76	441303 30 Jul 76			

AE TEST 6 DIAGRAM

See the sequence chart on DATA 206 for referenced test points.
See OPER 235 for theory.



CE0241 Seq. 2 of 2	2358578 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AE TEST 6 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AE, test 6
1. Load AE
2. Enter 10,06,00,00

Scope Setup

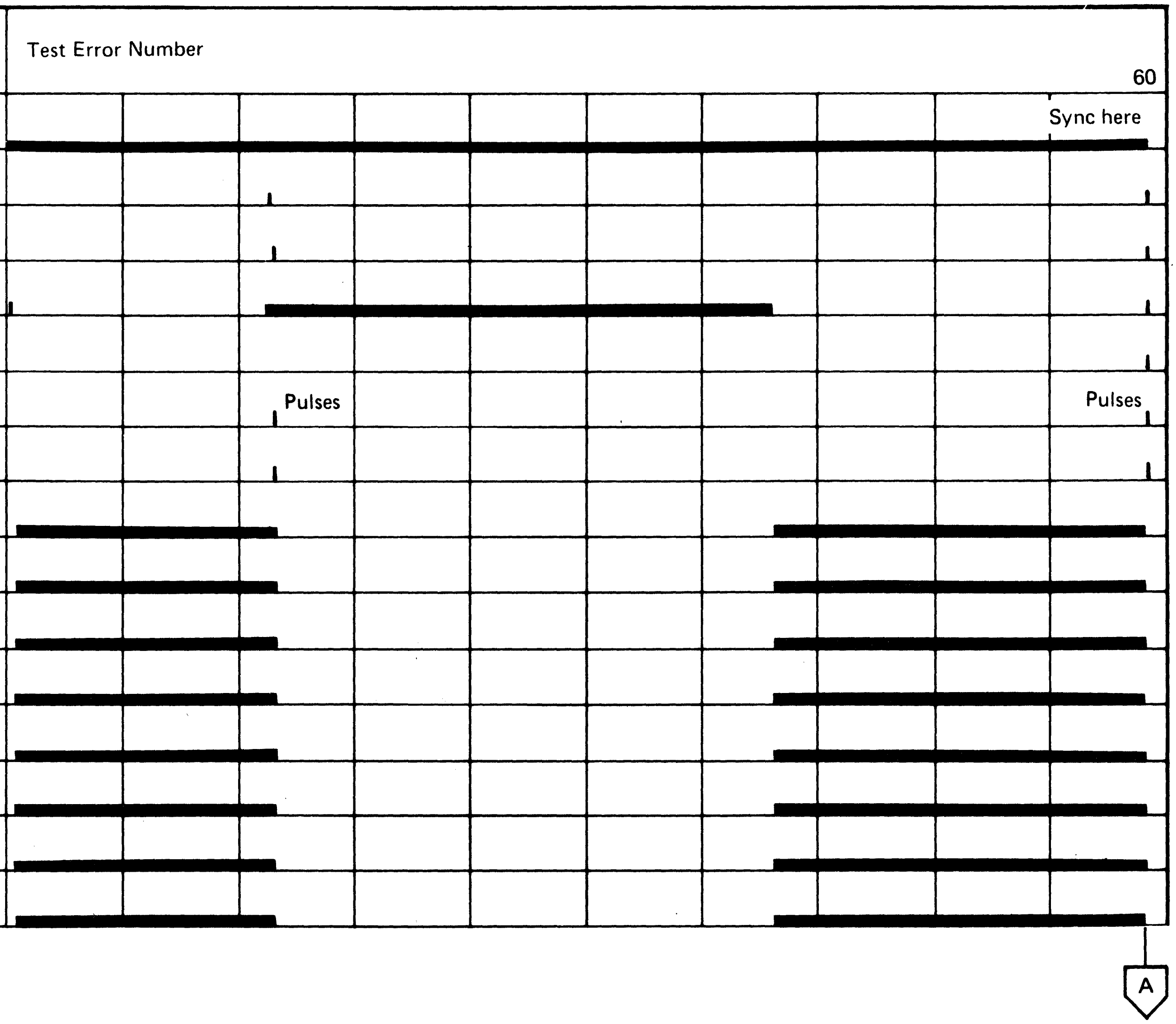
Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend:
▭ Inactive
▬ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	C
2	+G1	BH120	A2Q2 J09	A
3	−G2	BH110	A2Q2 D05	B
4	+Normal NPL	BE160	A2K2 D11	F
5	+Check End NPL	BE160	A2K2 D05	G
6	−Sync In	BC170	A2S2 S10	E
7	+Read Mode	BG170	A2P2 D05	D
8	+Cont Bus In Bit 0	BA100	A2F2 P05	H
9	+Cont Bus In Bit 1	BA100	A2F2 M10	
10	+Cont Bus In Bit 2	BA100	A2F2 M08	
11	+Cont Bus In Bit 3	BA100	A2F2 S07	
12	+Cont Bus In Bit 4	BA100	A2F2 P06	
13	+Cont Bus In Bit 5	BA100	A2F2 U03	
14	+Cont Bus In Bit 6	BA100	A2F2 P09	
15	+Cont Bus In Bit 7	BA100	A2F2 U06	



Line keys reference the diagram on DATA 204.

DATA 208
(For expanded
sequence chart)

AE TEST 6 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

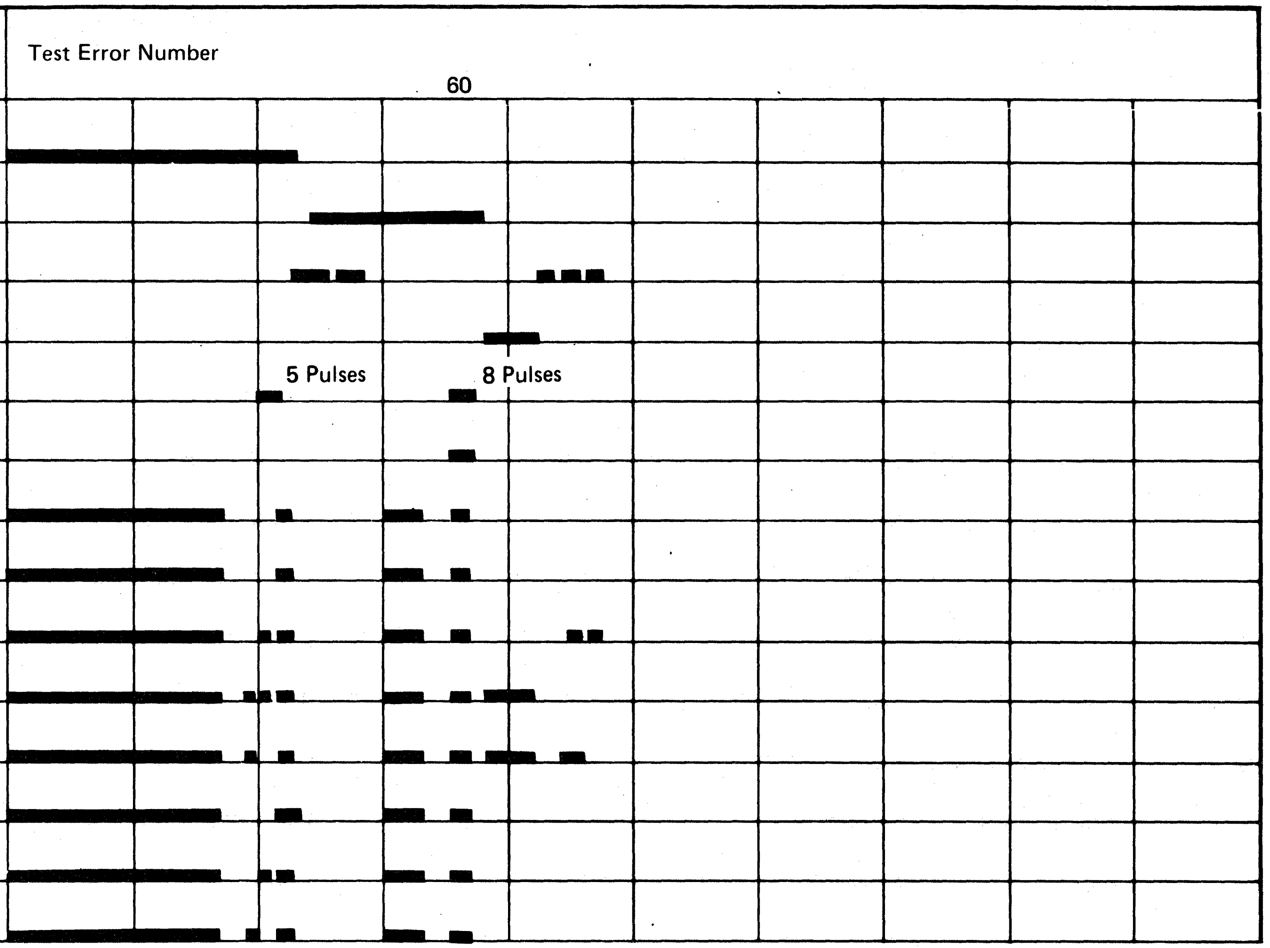
Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 9.0
Source – Int Ch 1

DATA 206 A

Legend: ☐ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+G1	BH120	A2Q2 J09	Ⓐ
2	−G2	BH110	A2Q2 D05	Ⓑ
3	−Normal End NPL	BE160	A2K2 D11	Ⓕ
4	+Check End NPL	BE160	A2K2 D05	Ⓖ
5	−Sync In	BC170	A2S2 S10	Ⓔ
6	+Read Mode	BG170	A2P2 D05	Ⓓ
7	+Cont Bus In Bit 0	BA100	A2F2 P05	Ⓗ
8	+Cont Bus In Bit 1	BA100	A2F2 M10	
9	+Cont Bus In Bit 2	BA100	A2F2 M08	
10	+Cont Bus In Bit 3	BA100	A2F2 S07	
11	+Cont Bus In Bit 4	BA100	A2F2 P06	
12	+Cont Bus In Bit 5	BA100	A2F2 U03	
13	+Cont Bus In Bit 6	BA100	A2F2 P09	
14	+Cont Bus In Bit 7	BA100	A2F2 U06	



Line keys reference the diagram on DATA 204.

3350	CE0243 Seq. 2 of 2	2358579 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AE TEST 6 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2S2S10
–Sync In
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B Triggerable after delay time
A and B Time/div – 5 ms/div
Slope (-) on set of 8 Sync In pulses
Delay Time-Delayed Sweep – 1 µs/div
Delay-Time Multiplier – 9.8
Source – Int Ch 1

Legend:
☐ Inactive
■ Active level
▨ Tolerance

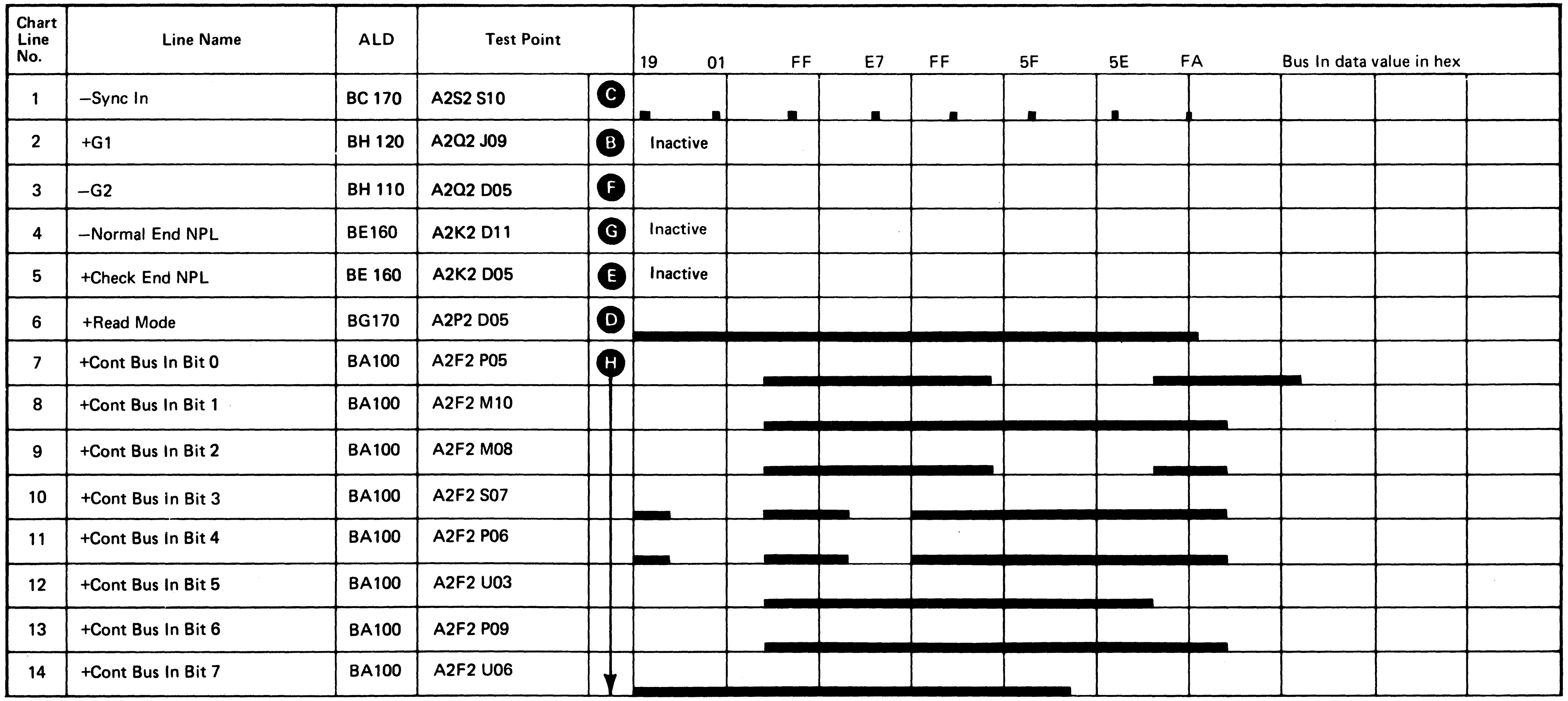


Chart Line No.	Line Name	ALD	Test Point		
1	–Sync In	BC 170	A2S2 S10	C	
2	+G1	BH 120	A2Q2 J09	B	Inactive
3	–G2	BH 110	A2Q2 D05	F	
4	–Normal End NPL	BE160	A2K2 D11	G	Inactive
5	+Check End NPL	BE 160	A2K2 D05	E	Inactive
6	+Read Mode	BG170	A2P2 D05	D	
7	+Cont Bus In Bit 0	BA100	A2F2 P05	H	
8	+Cont Bus In Bit 1	BA100	A2F2 M10		
9	+Cont Bus In Bit 2	BA100	A2F2 M08		
10	+Cont Bus In Bit 3	BA100	A2F2 S07		
11	+Cont Bus In Bit 4	BA100	A2F2 P06		
12	+Cont Bus In Bit 5	BA100	A2F2 U03		
13	+Cont Bus In Bit 6	BA100	A2F2 P09		
14	+Cont Bus In Bit 7	BA100	A2F2 U06		

Line keys reference the diagram on DATA 204.

3350	CE0244 Seq. 1 of 2	2358580 Part No.	441300 31 Mar 76	441303 30 Jul 76		

SHIFT REGISTER ERROR

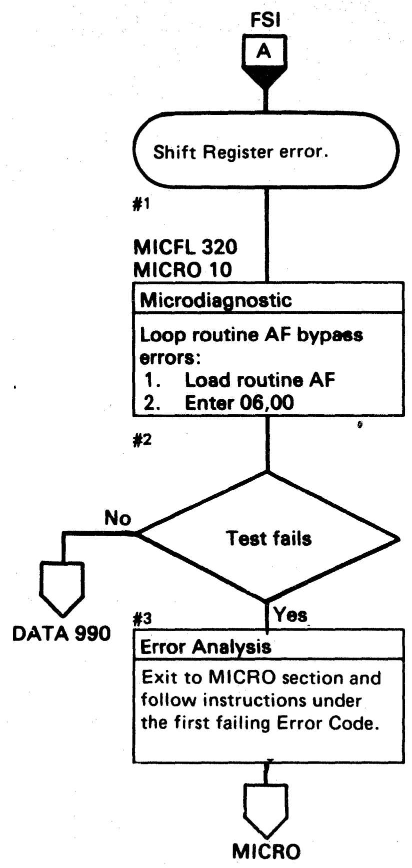
ERROR DESCRIPTION

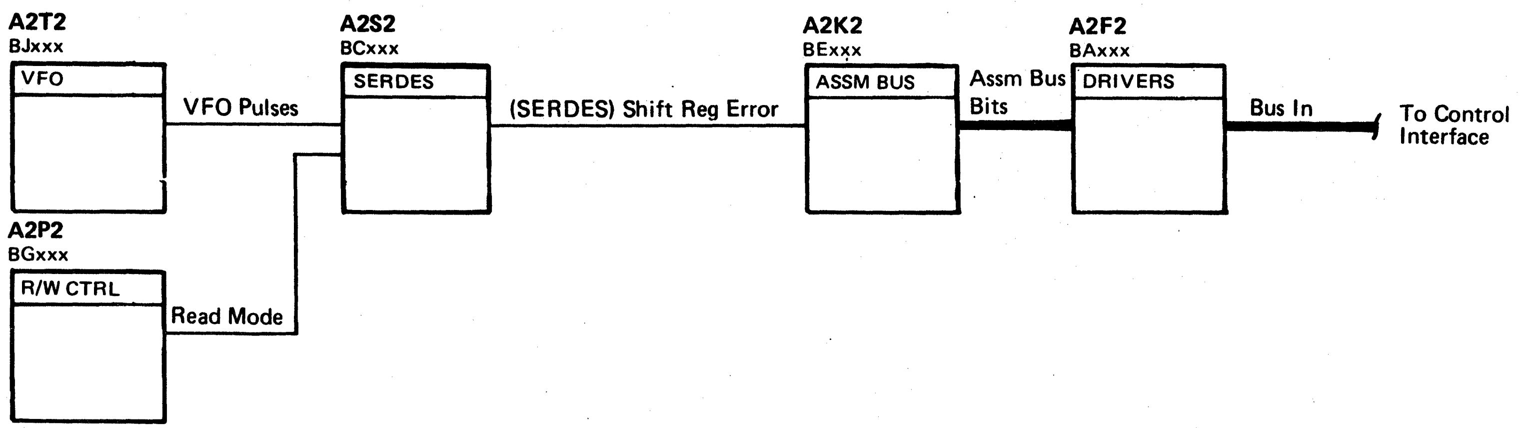
A Shift Register error is caused by a failure in any Shift Register position or in the SERDES Parity latch.

A Shift Register error activates Controller Check and Error Alert.

The data enters the Shift Register (SR) position 0 and shifts one position each bit time. The input is also exclusive ORed with the output of SERDES SR 7 to operate the SERDES Parity latch. The SERDES Parity latch changes state each time another bit enters the Shift Register unless one shifts out the end as indicated by the SERDES SR 7 line. The Shift Register outputs are fed to a parity generator to produce the SERDES SR P line. The SERDES SR P and the SERDES Parity latch are compared every bit time. The failure of any Shift Register position or the SERDES Parity latch activates the SERDES SR Check latch during the failing cycle.

See OPER 241 for additional theory.





3350

CE0244 Seq. 2 of 2	2358580 Part No.	441300 31 Mar 76	441303 30 Jul 76			

REPETITIVE COMMAND OVERRUN ON G1 OPERATIONS

ERROR DESCRIPTION

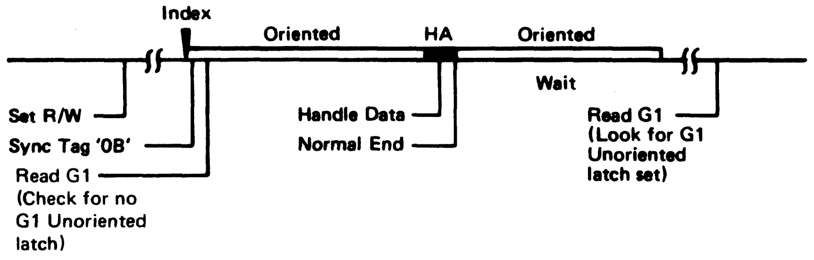
The Repetitive Command Overrun on G1 Operations error indicates a failure of the storage control to recognize that orientation has been achieved. This error is caused by the G1 Unoriented latch erroneously being on. If more than one controller with the same address is on the same interface, this may be the first error to appear, since all responses from the machines are nearly identical until they attempt to achieve orientation.

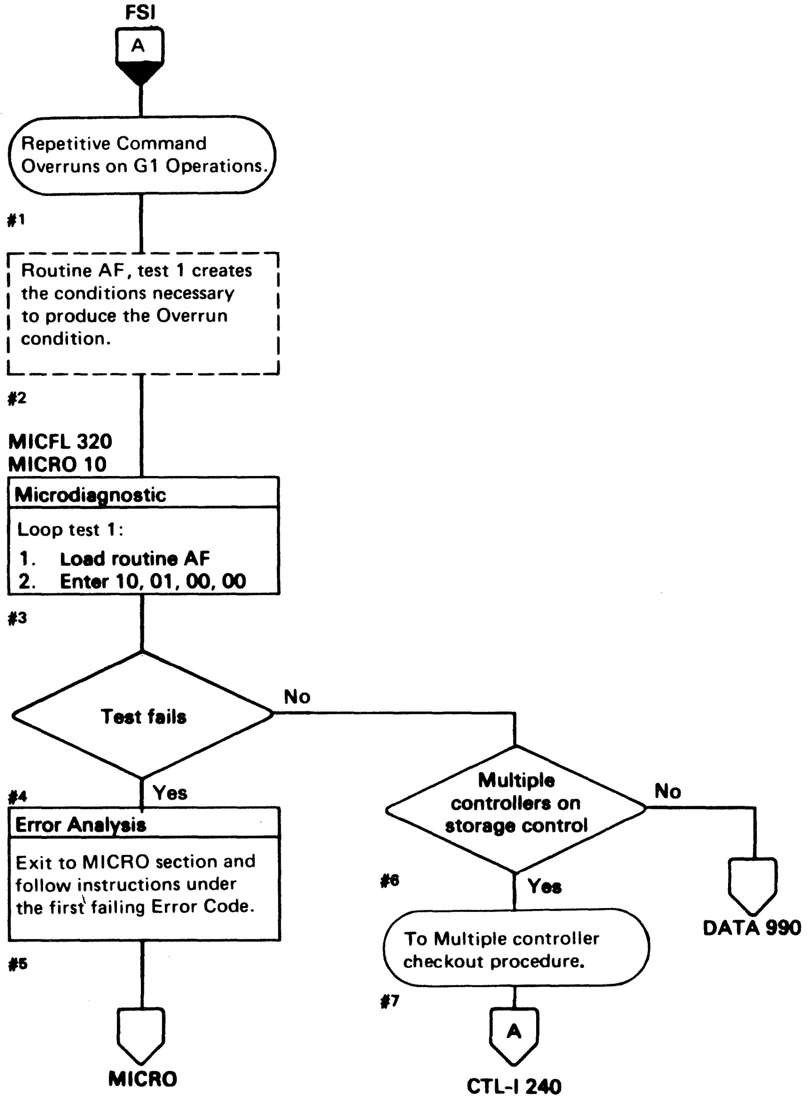
MICRODIAGNOSTIC DESCRIPTION

Routine AF, test 1 looks for an Index. The Index causes the Oriented latch to set. A Read G1 operation is initiated and the G1 Unoriented latch is not set (ALD BH130). The Read operation data handling is then completed.

The test delays approximately 500 microseconds during which time the Oriented latch is reset. Another Read G1 operation is initiated and the G1 Unoriented latch is set.

The program verifies the on-off state of the G1 Unoriented latch at the specified times.





G1 UNORIENTED

ERROR DESCRIPTION

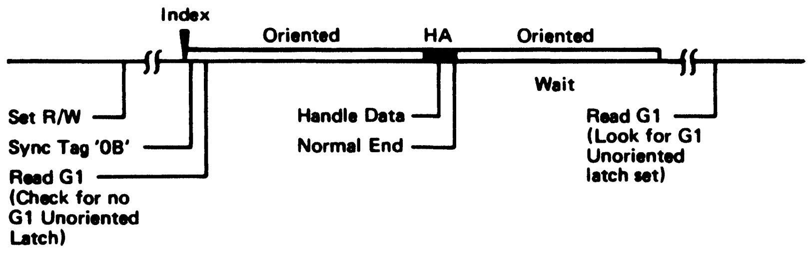
The G1 Unoriented line is used by the microprogram Read G1 operation to determine controller orientation. When it is active, G1 Unoriented indicates that a Read G1 command was issued outside a G1 gap area.

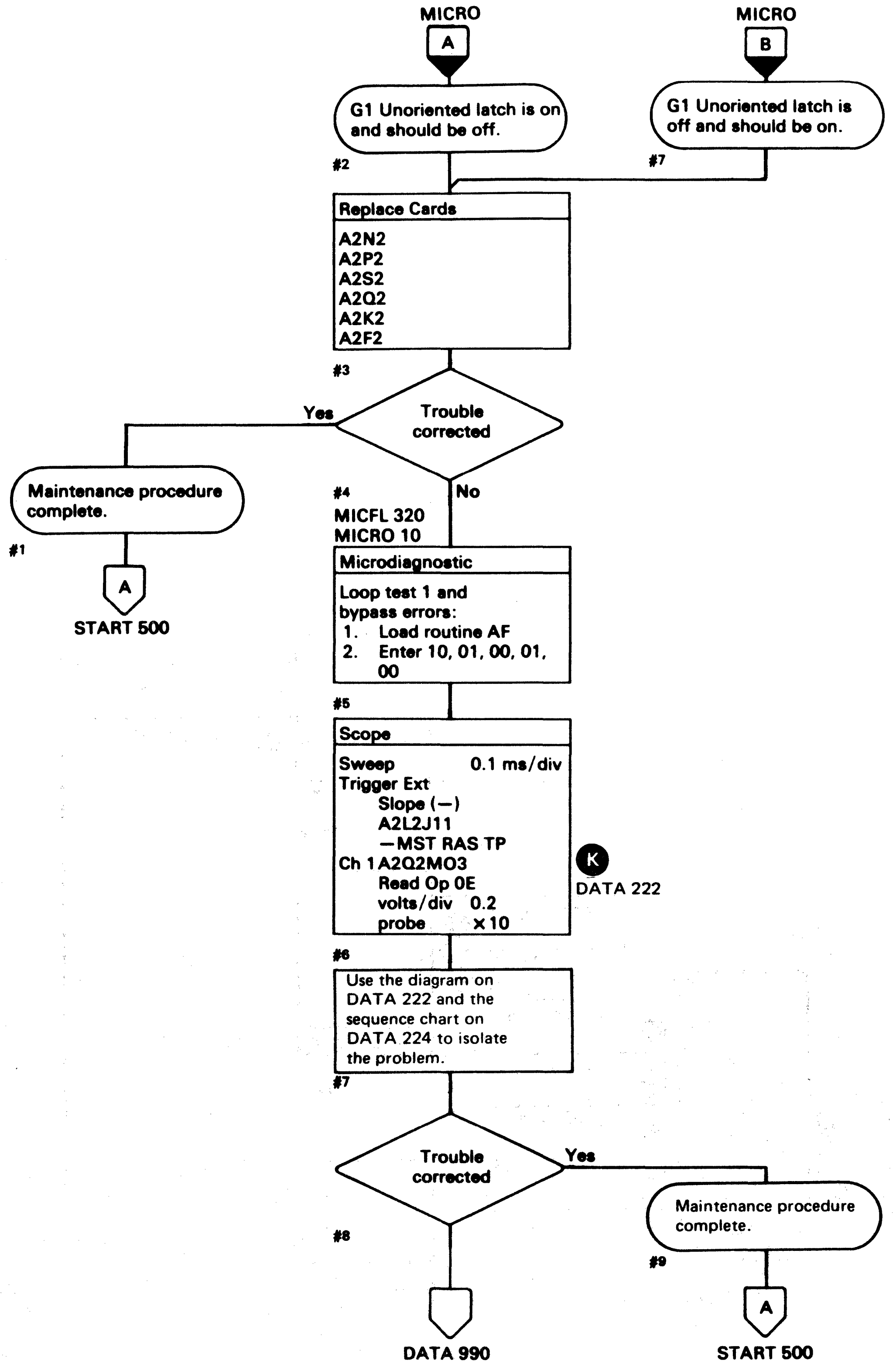
MICRODIAGNOSTIC DESCRIPTION

Routine AF, test 1 searches for an Index. The Index causes the Oriented latch to set. A Read G1 operation is initiated and the G1 Unoriented latch is not set (ALD BH130). The Read operation data handling is then completed.

The test delays approximately 500 microseconds during which time the Oriented latch is reset. Another Read G1 operation is initiated and the G1 Unoriented latch is set.

The program verifies the on-off state of the G1 Unoriented latch at the specified times.



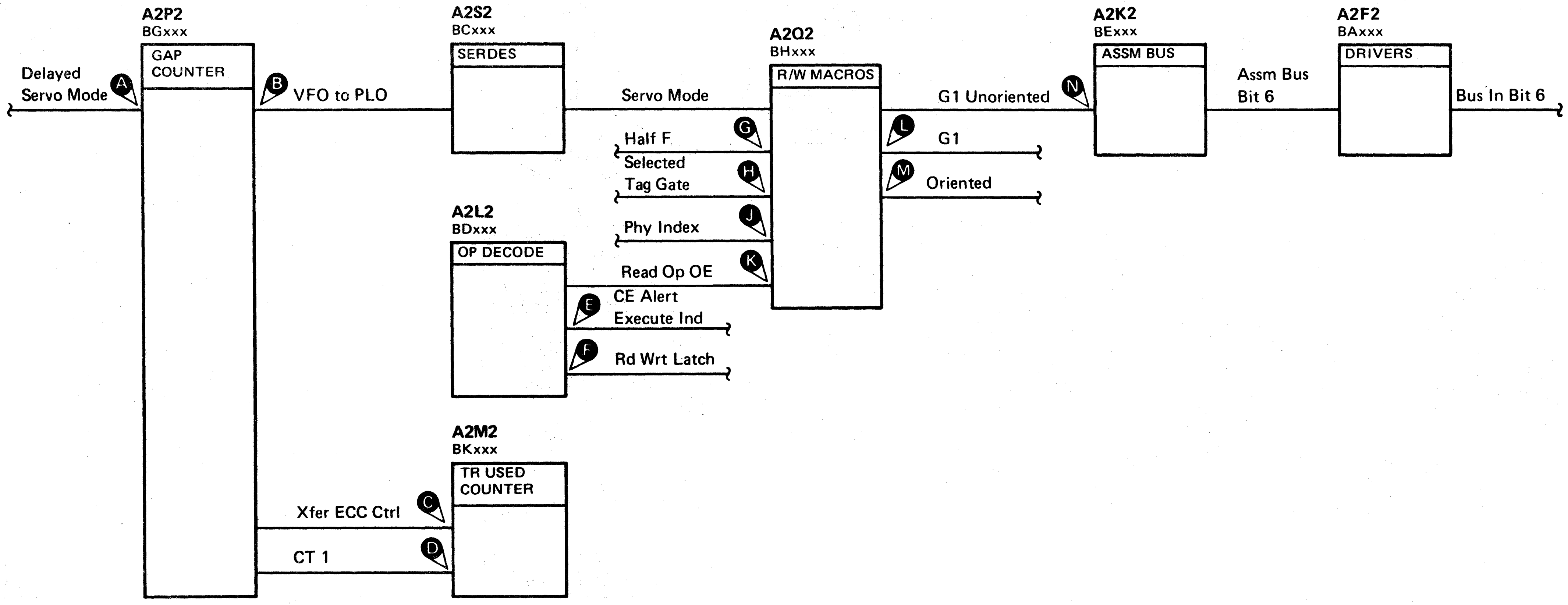


3350	CE0250 Seq. 1 of 2	2358582 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST 1 DIAGRAM

See the sequence chart on DATA 224 for referenced test points.

See OPER 103 for theory.



3350

CE0250 Seq. 2 of 2	2358582 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST 1 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

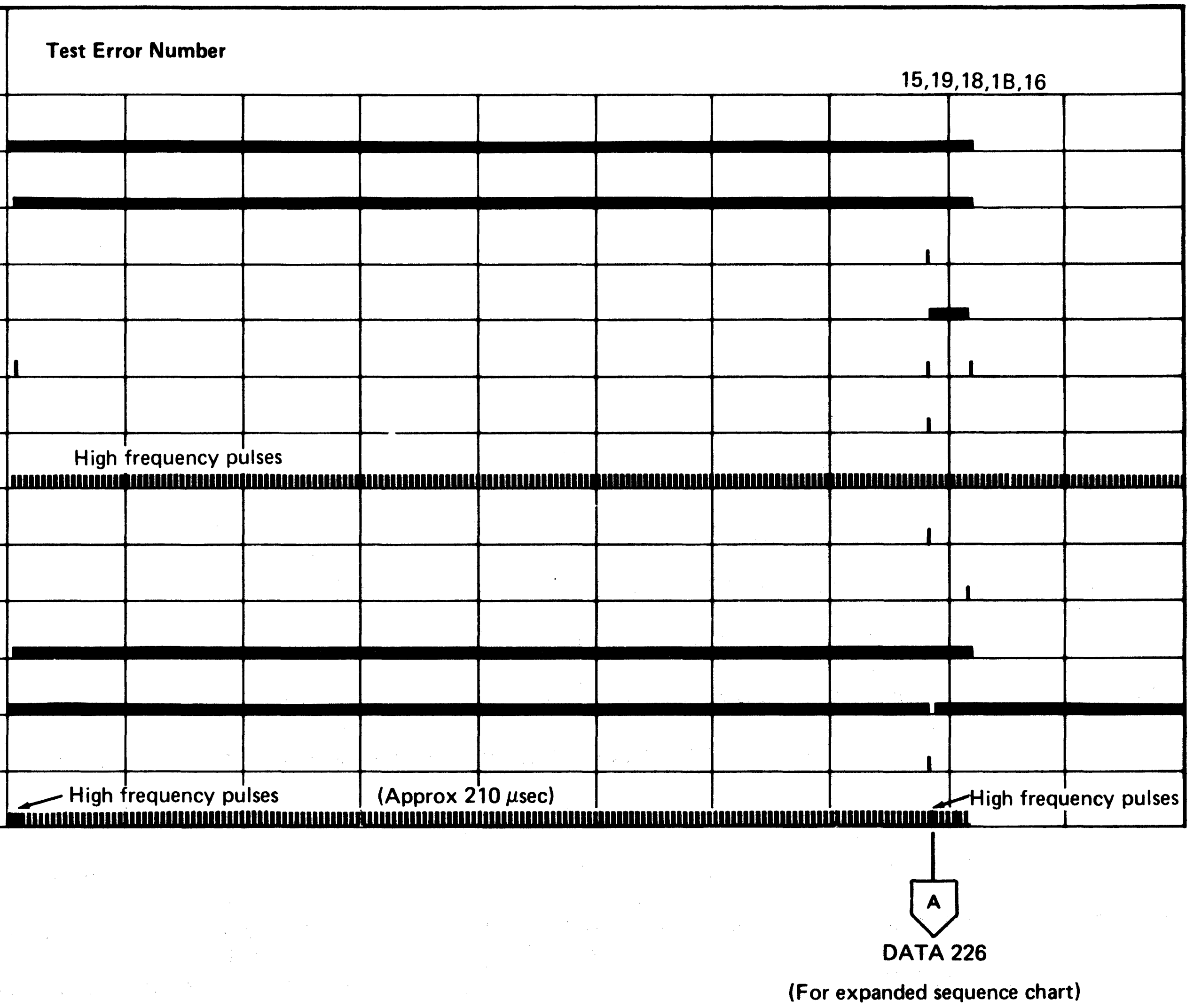
Routine AF, test 1
1. Load AF
2. Enter 10, 01, 00, 00

Scope Setup

Sweep	2 ms/div	Ch 1 A2U4D13 +CE Alert Execute Ind	
Mode	Alt or Chop		
Trigger	Ext		
Slope (+)		Volts/div	0.1
A2L2D13		Probe	x10
+CE Alert Execute Ind		Ch 2 (see chart)	

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	E
2	–Rd Wrt Latch	BD150	A2L2 J03	F
3	–Phy Index	BH140	A2Q2 S07	J
4	–Rd Op OE	BH100	A2Q2 M03	K
5	–Selected Tag Gate	BH100	A2Q2 G05	H
6	–Oriented	BH130	A2Q2 J06	M
7	+Half F	BH100	A2Q2 D09	G
8	+G1	BH120	A2Q2 J09	L
9	+G1 Unoriented	BE120	A2K2 B03	N
10	+Delayed Servo Mode	BG150	A2P2 B11	A
11	+VFO To PLO	BG150	A2P2 B13	B
12	–Xfer ECC Ctrl	BK100	A2N2 B05	C
13	–CT 1	BK100	A2N2 P03	D



Line keys reference the diagram on DATA 222.

AF TEST 1 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

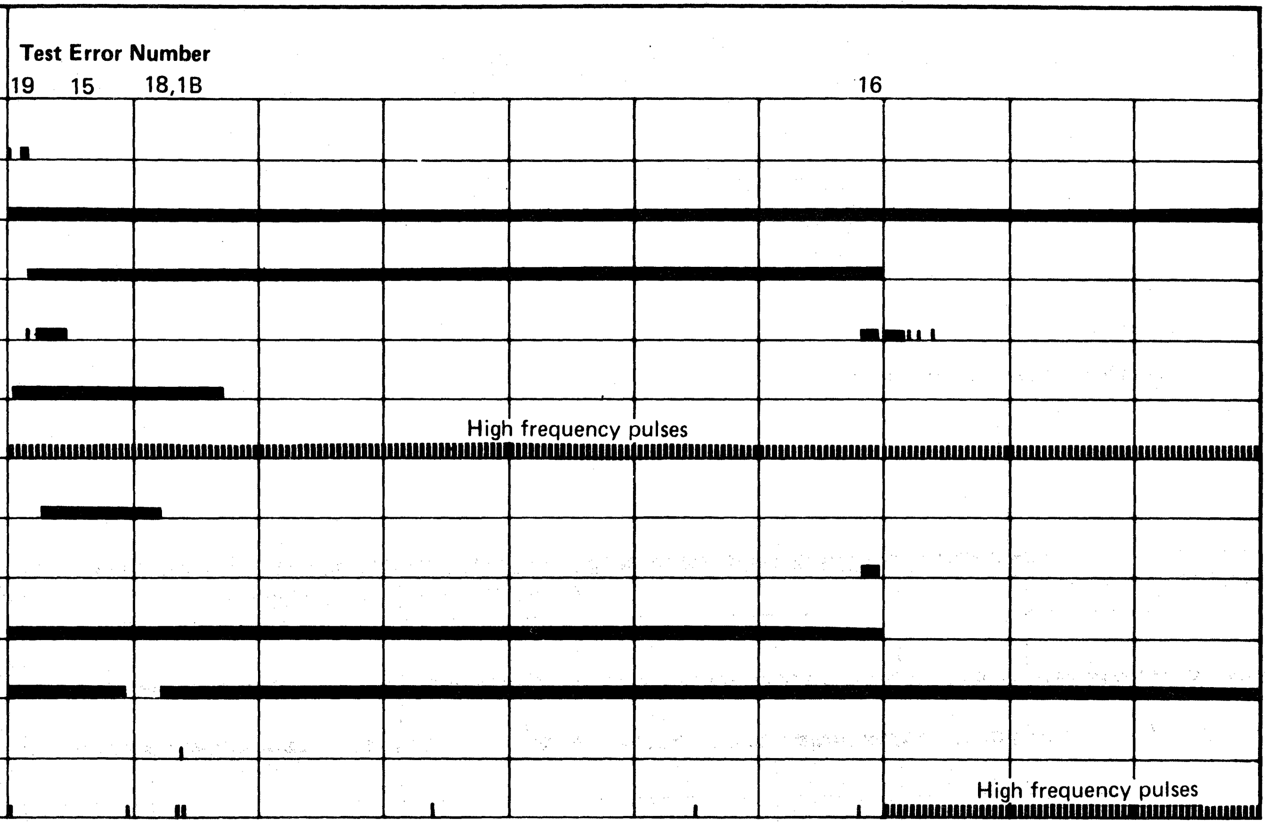
Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Ch 1 A2Q2S07
−Phy Index
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 2 ms/div
Slope (–)
Delay Time-Delayed Sweep – 0.1 ms/div
Delay-Time Multiplier – 0.4
Source – Int Ch 1

DATA 224 A

Legend: ☐ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	−Phy Index	BH140	A2Q2 S07	J
2	+Rd Wrt Latch	BD150	A2L2 J03	F
3	−Rd Op OE	BH100	A2Q2 M03	K
4	−Selected Tag Gate	BH100	A2Q2 G05	H
5	−Oriented	BH130	A2Q2 J06	M
6	+Half F	BH100	A2Q2 D09	G
7	+G1	BH120	A2Q2 J09	L
8	+G1 Unoriented	BE120	A2K2 B03	N
9	+Delayed Servo Mode	BG150	A2P2 B11	A
10	+VFO to PLO	BG150	A2P2 B13	B
11	−Xfer ECC CTRL	BK100	A2N2 B05	C
12	−CT 1	BK100	A2N2 P03	D



Line keys reference the diagram on DATA 222.

3350	CE0253 Seq. 2 of 2	2358583 Part No.	441300 31 Mar 76	441303 30 Jul 76

SYNC OUT TIMING ERROR

ERROR DESCRIPTION

The Sync Out Timing error verifies the Sync In/Sync Out timing relationship. The controller originates Sync In pulses and the storage control must respond, within time limits, with Sync Out.

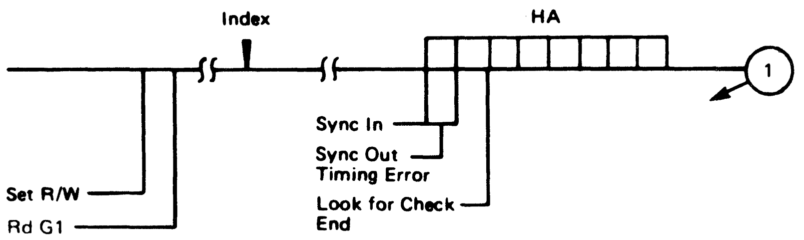
The following conditions can cause Sync Out Timing errors:

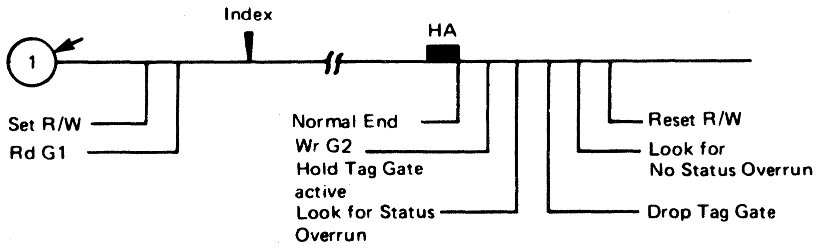
Sync Out late
Sync Out missing
Extra Sync Out pulses

MICRODIAGNOSTIC DESCRIPTION

See DATA 140 for a description of routine AD, test 1.

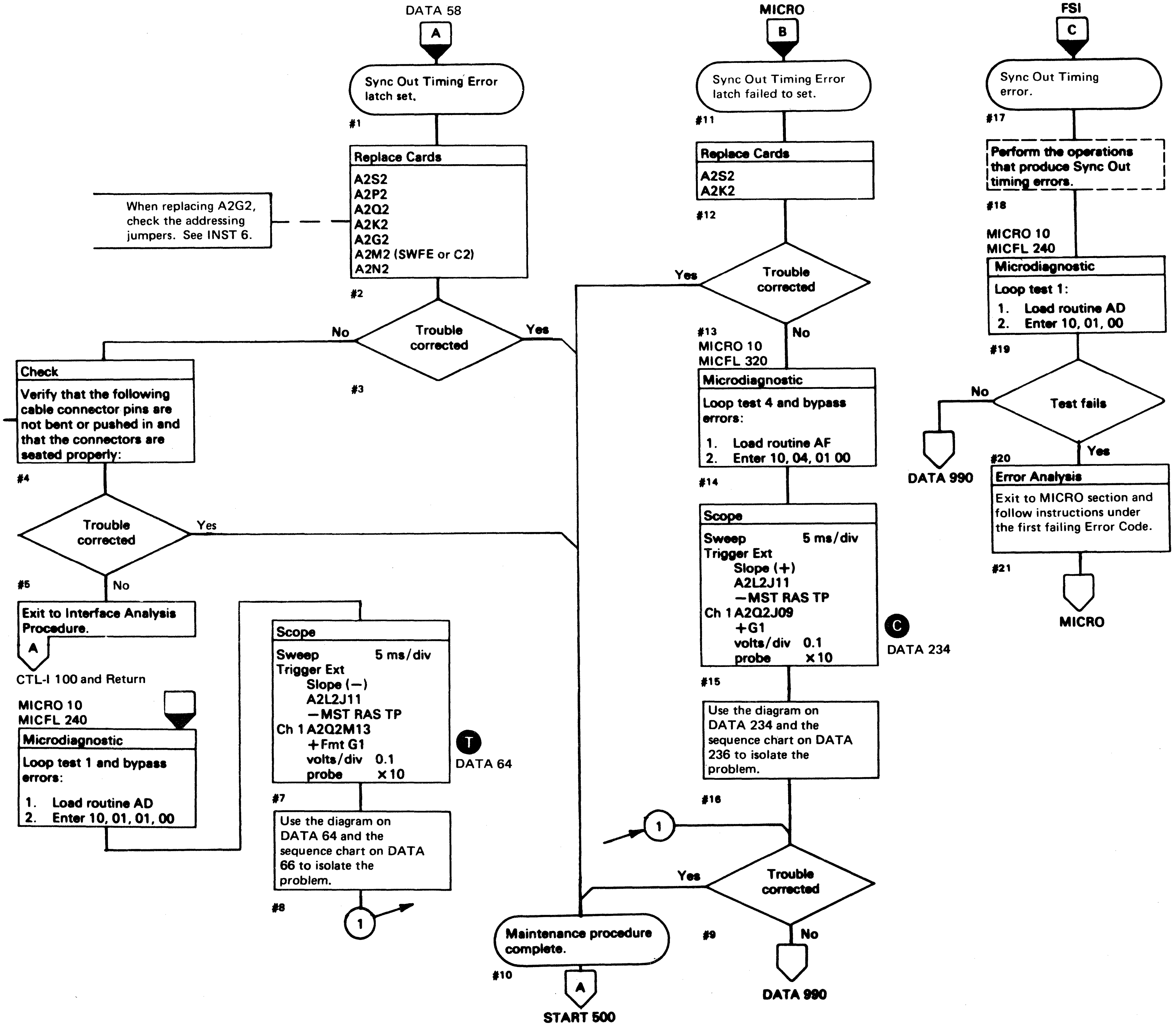
Routine AF, test 4 forces a Sync Out timing error by **initiating a data handling type of operation (Write G1) and by *not* responding to Sync-In pulses. The program expects Check End in addition to Sync Out Timing Error.**





		SWFE	
	Basic	Interface A	Interface B
Sync Out	A2C4D13 - 01B-A1H1D13*	A2A4D13 - 01B-A1H1D13*	A2B4D13 - 01B-A1D1D13*
Sync In	A2C3D13 - 01B-A1H1J13*	A2A3D13 - 01B-A1H1J13*	A2B3D13 - 01B-A1D1J13*

Indicates the tailgate connector 01B. **See LOC 2 for locations.*



CE0256 Seq. 1 of 1	2358584 Part No.	441300 31 Mar 76	441303 30 Jul 76			

STATUS OVERRUN

ERROR DESCRIPTION

During selection or chained reselection, the storage control interlocks the channel sequence with the control interface sequence. After receiving Command Out, the storage control decodes the command and:

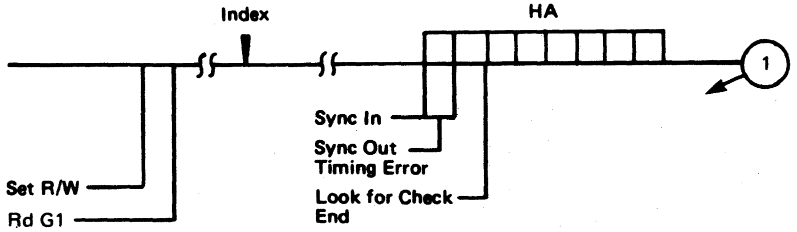
1. **Sends an operation code to the controller over the control interface.**
2. **Sends Status In to the channel.**
3. Holds Tag Gate active on the control interface until the channel responds with Service Out.

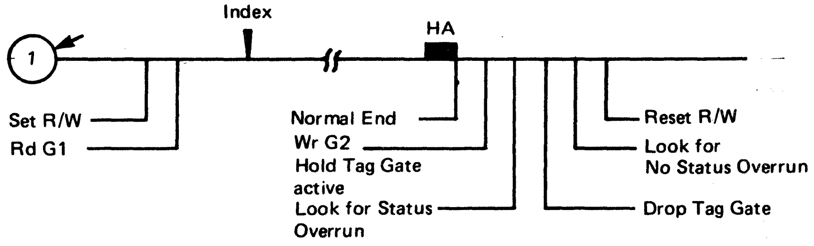
If a chained reselection is in process and the disk is oriented, Tag Gate must drop within a specified time to avoid an overrun condition. If not, the Status Overrun latch is set indicating that the channel did not respond in time to Status In.

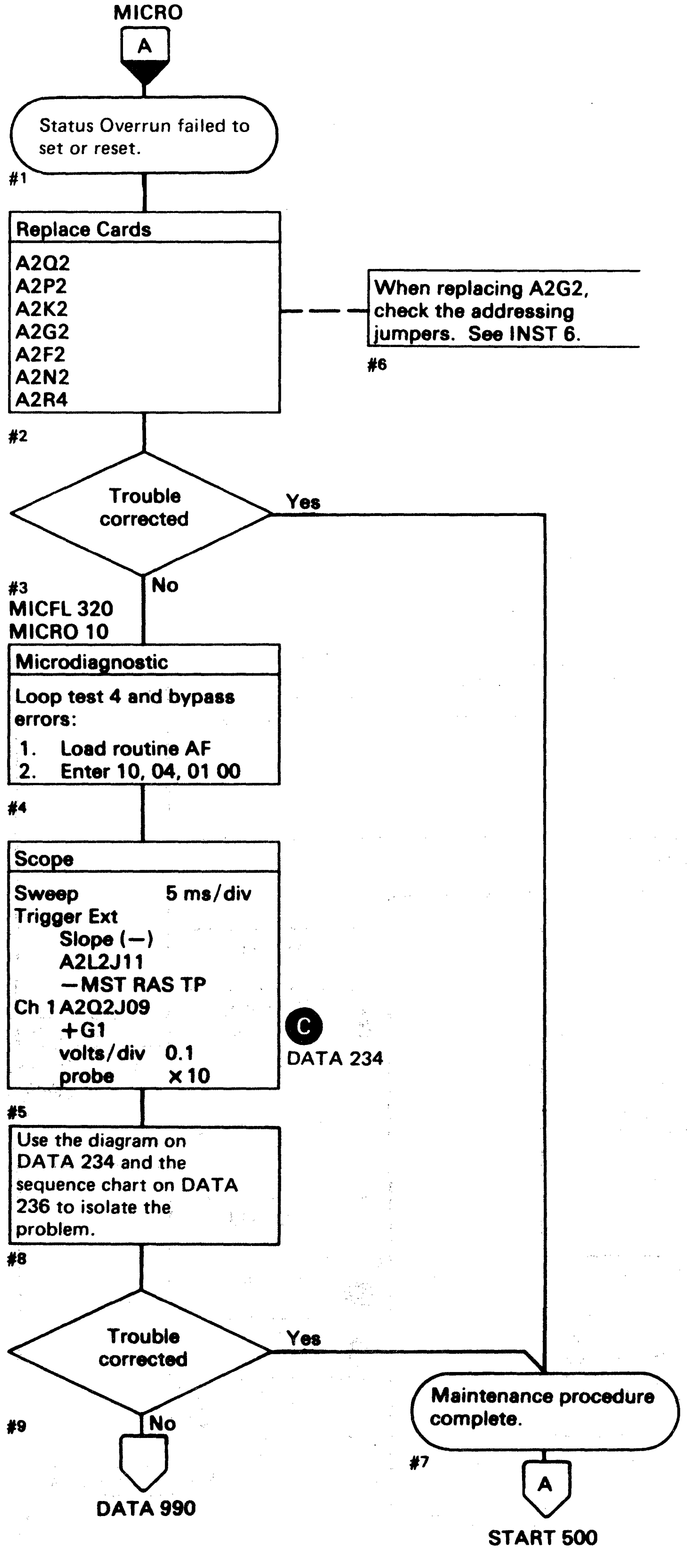
Command Overruns may occur occasionally in normal operation due to channel loading. Repetitive Command Overruns after a retry cause a Fault Symptom Code of 9009 to be posted.

MICRODIAGNOSTIC DESCRIPTION

Routine AF, test 4 forces a Sync Out Timing error by initiating a data handling type of operation (Read G1) and by *not* responding to Sync In pulses. The program expects Check End in addition to Sync Out Timing error. Then a Status Overrun Check is performed.







Status Overrun failed to set or reset.

Replace Cards
A2Q2
A2P2
A2K2
A2G2
A2F2
A2N2
A2R4

When replacing A2G2, check the addressing jumpers. See INST 6.

Trouble corrected

MICFL 320
MICRO 10

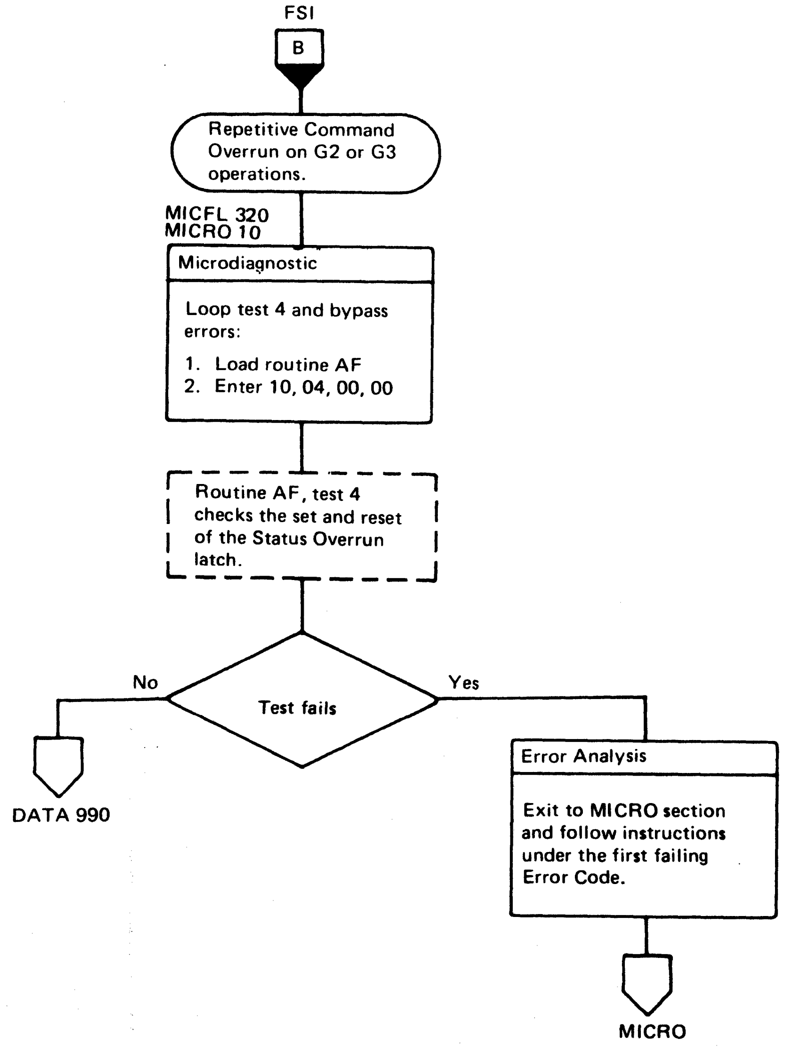
Microdiagnostic
Loop test 4 and bypass errors:
1. **Load routine AF**
2. **Enter 10, 04, 01 00**

Scope
Sweep 5 ms/div
Trigger Ext
Slope (—)
A2L2J11
—MST RAS TP
Ch 1 A2Q2J09
+G1
volts/div 0.1
probe ×10

Use the diagram on DATA 234 and the sequence chart on DATA 236 to isolate the problem.

Trouble corrected

Maintenance procedure complete.



Repetitive Command Overrun on G2 or G3 operations.

MICFL 320
MICRO 10

Microdiagnostic
Loop test 4 and bypass errors:
1. Load routine AF
2. Enter 10, 04, 00, 00

Routine AF, test 4 checks the set and reset of the Status Overrun latch.

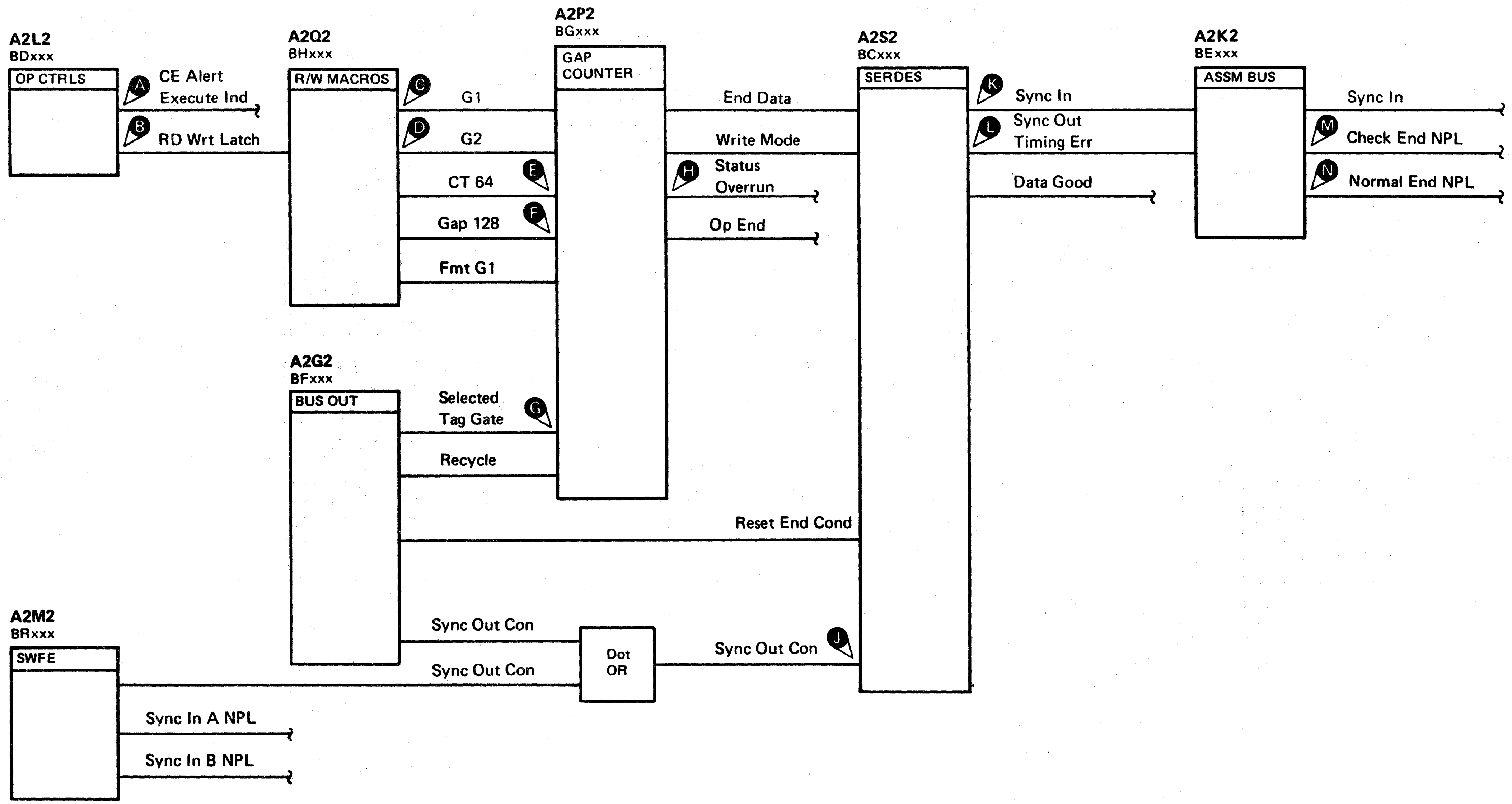
Test fails

Error Analysis
Exit to MICRO section and follow instructions under the first failing Error Code.

AF TEST 4 DIAGRAM

See the sequence chart on DATA 236 for referenced test points.

See OPER 103 for theory.



AF TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AF, test 4
1. Load AF
2. Enter 10, 04, 00, 00

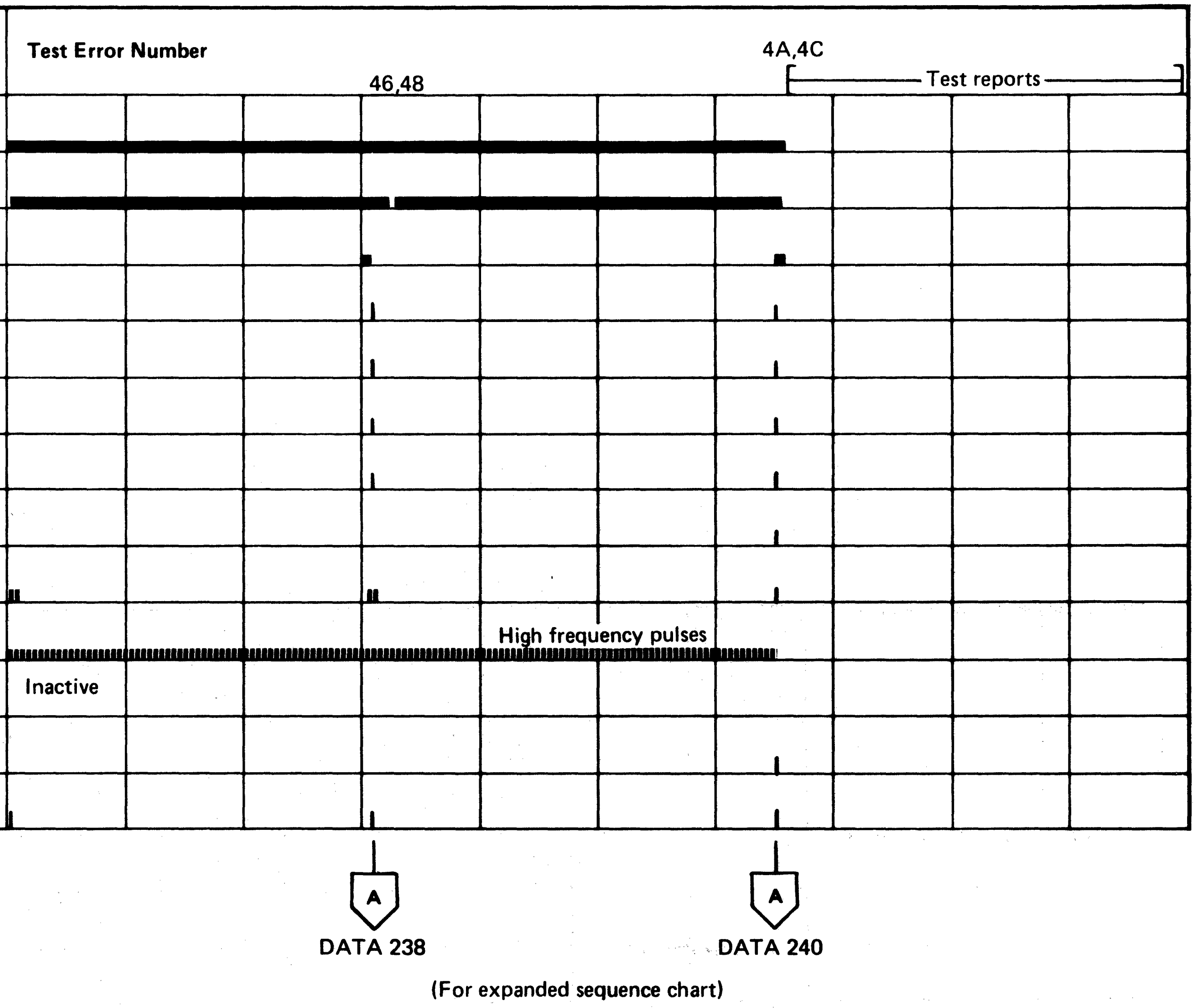
Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Legend: ☐ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	A
2	–Rd Wrt Latch	BD150	A2L2 J03	B
3	+G1	BH120	A2Q2 J09	C
4	–Sync In	BC170	A2S2 S10	K
5	+Sync Out Con	BC170	A2S2 S12	J
6	+Check End NPL	BE160	A2K2 D05	M
7	–Sync Out Timing Err	BC170	A2S2 U10	L
8	–G2	BH110	A2Q2 D05	D
9	–Selected Tag Gate	BG140	A2P2 J11	G
10	–CT 64	BG140	A2P2 U06	E
11	–Gap 128	BG140	A2P2 U09	F
12	–Status Overrun	BG140	A2P2 P03	H
13	+Normal End NPL	BE160	A2K2 D11	N



Line keys reference the diagram on DATA 234.

AF TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

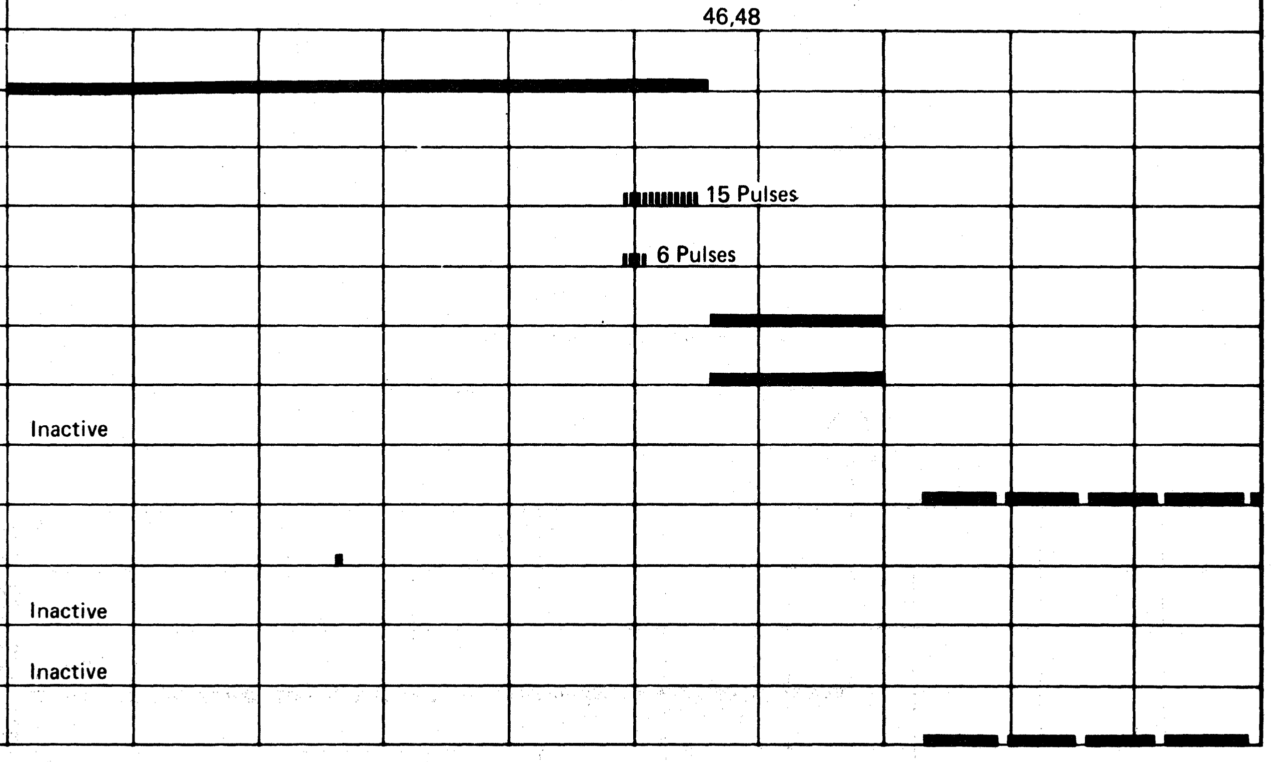
Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

DATA 236
Ⓐ

Legend:
▭ Inactive
▬ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+G1	BH120	A2Q2 J09	Ⓒ	
2	–Rd Wrt Latch	BD150	A2L2 J03	Ⓑ	
3	–Sync In	BC170	A2S2 S10	Ⓚ	
4	+Sync Out	BC170	A2S2 S12	Ⓙ	
5	+Check End NPL	BE160	A2K2 D05	Ⓜ	
6	–Sync Out Timing Err	BC170	A2S2 U10	Ⓛ	
7	–G2	BH110	A2Q2 D05	Ⓓ	Inactive
8	–Selected Tag Gate	BG140	A2P2 J11	Ⓖ	
9	–Ct 64	BG140	A2P2 U06	Ⓔ	
10	–Gap 128	BG140	A2P2 U09	Ⓕ	Inactive
11	–Status Overrun	BG140	A2P2 P03	Ⓗ	Inactive
12	+Normal End NPL	BE160	A2K2 D11	Ⓝ	



Line keys reference the diagram on DATA 234.

AF TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

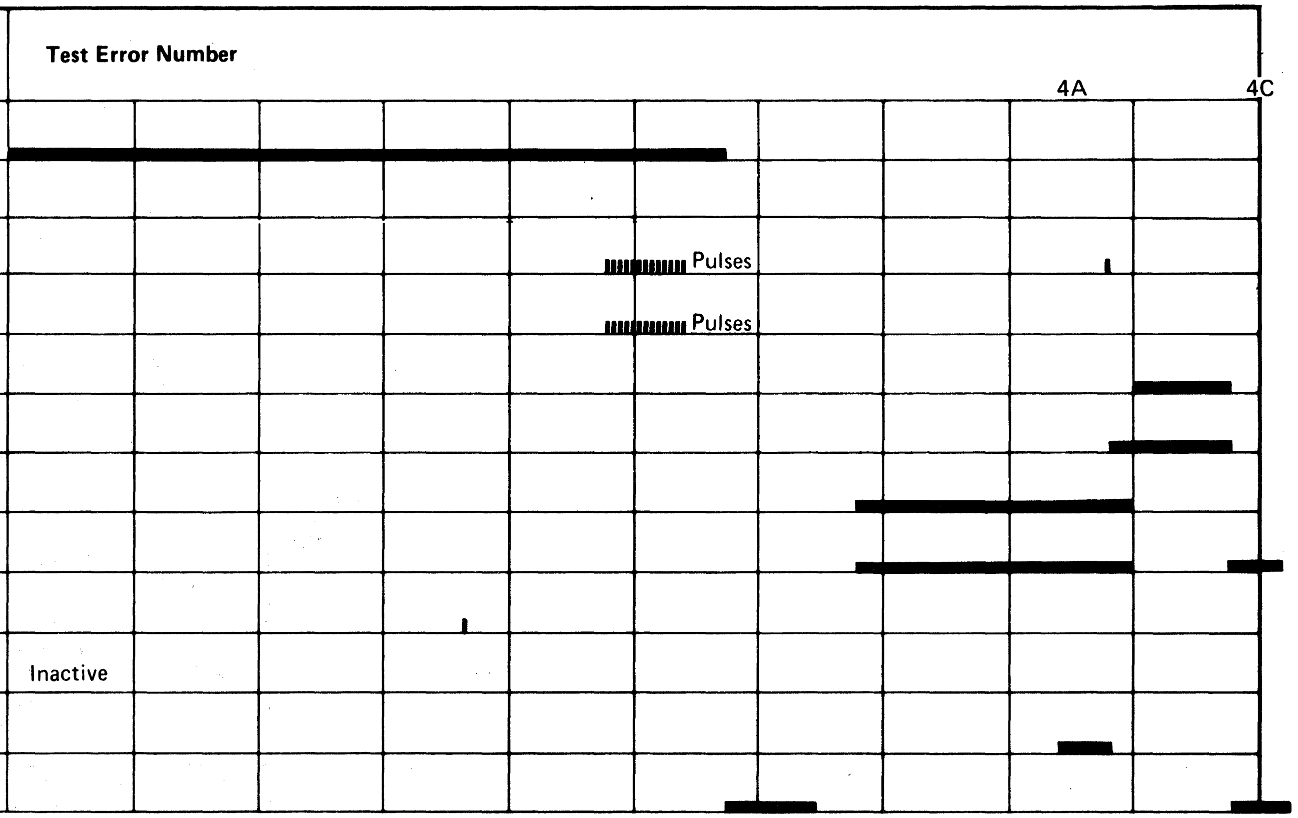
Scope Setup

Sweep 5 ms/div — Ch 1 A2Q2J09 +G1
Mode Alt or Chop — Volts/div 0.1
Trigger Ext — Probe x10
Slope (+) — Ch 2 (see chart)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 3.5
Source – Int Ch 1

DATA 238
A

Legend: ☐ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+G1	BH120	A2Q2 J09	C
2	−Rd Wrt Latch	BD150	A2L2 J03	B
3	−Sync In	BC170	A2S2 S10	K
4	+Sync Out Con	BC170	A2S2 S12	J
5	+Check End NPL	BE160	A2K2 D05	M
6	−Sync Out Timing Err	BC170	A2S2 U10	L
7	−G2	BH110	A2Q2 D05	D
8	−Selected Tag Gate	BG140	A2P2 J11	G
9	−CT 64	BG140	A2P2 U06	E
10	−Gap 128	BG140	A2P2 U09	F
11	−Status Overrun	BG140	A2P2 P03	H
12	+Normal End NPL	BE160	A2K2 D11	N



Line keys reference the diagram on DATA 234.

TRACK OVERRUN FAILURE

ERROR DESCRIPTION

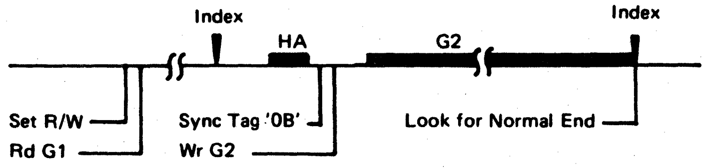
Track Overrun indicates an attempt to write data past the Index. This may be a programming choice and not an error. Track Overrun causes a Check End and sets Bus In bit 3 on.

MICRODIAGNOSTIC DESCRIPTION

Routine AF, test 6 reads the Home Address and then writes a record that checks the track capacity, that is, the maximum number of bytes that will fit the track.

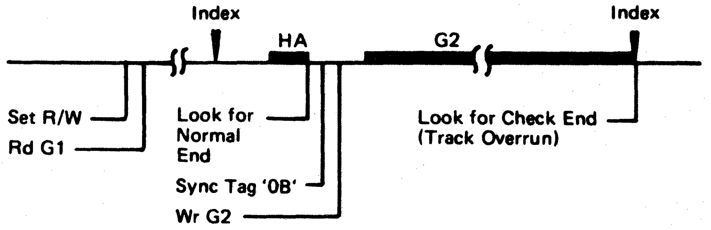
An Error Code of AF6B indicates a Track Overrun may result if the track is formatted with an Extended G1. Run routine AF, test E to restore the G2 field to its normal position.

TEST 6

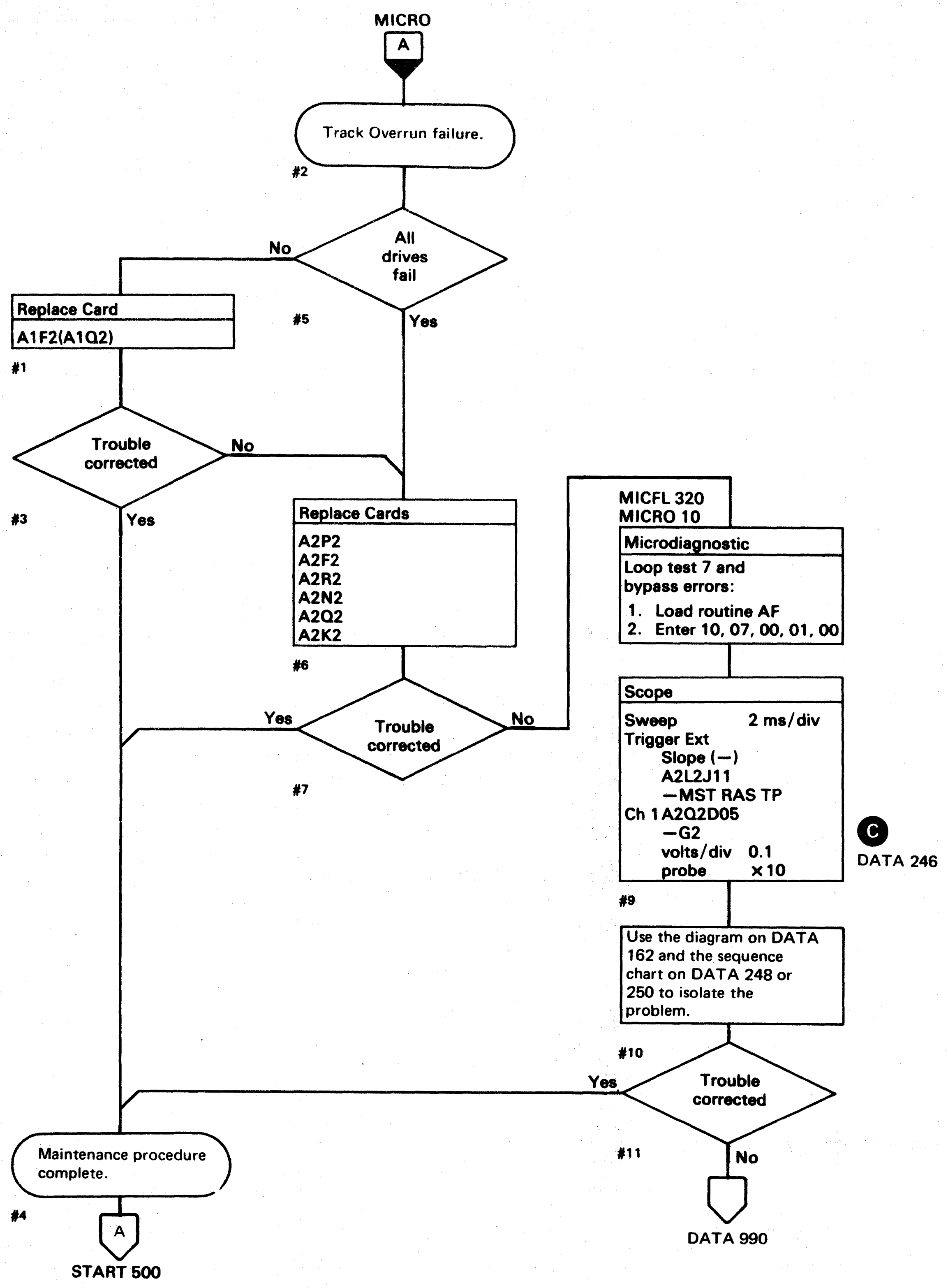


Routine AF, test 7 performs the test just as test 6 except that a few bytes are added so that Track Overrun occurs.

TEST 7



Tests can be run in 3330-1 Compatibility Mode (see the sequence chart on DATA 248) or Native Mode (see the sequence chart on DATA 250).

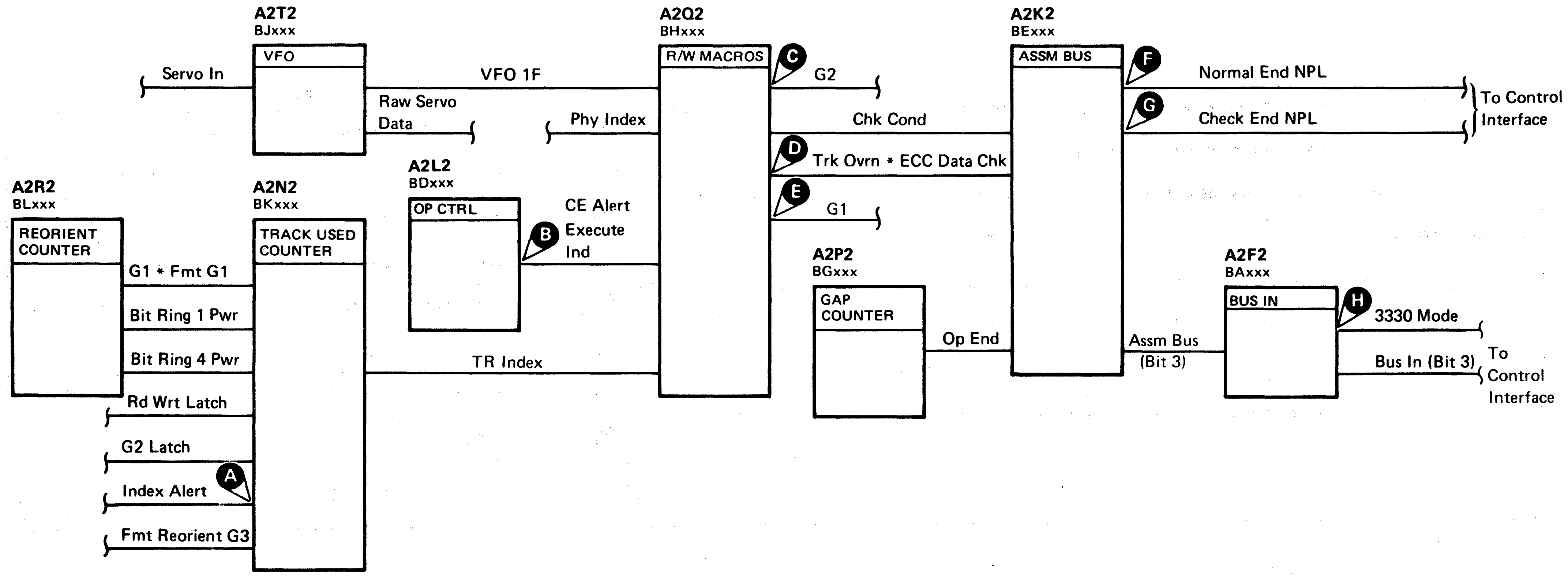


CE0275 Seq. 2 of 2	2358587 Part No.	**441300** **31 Mar 76**	441303 30 Jul 76			

AF TEST 6 AND 7 DIAGRAM

See the sequence chart of DATA 248 for referenced test points.

See OPER 240 for theory.



AF TEST 6 AND 7 SEQUENCE CHARTS

3330-1 COMPATABILITY MODE

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Microdiagnostic Setup

Routine AF, test x { x = 6 for 3330-1 Compatibility Mode
x = 7 for Native Mode

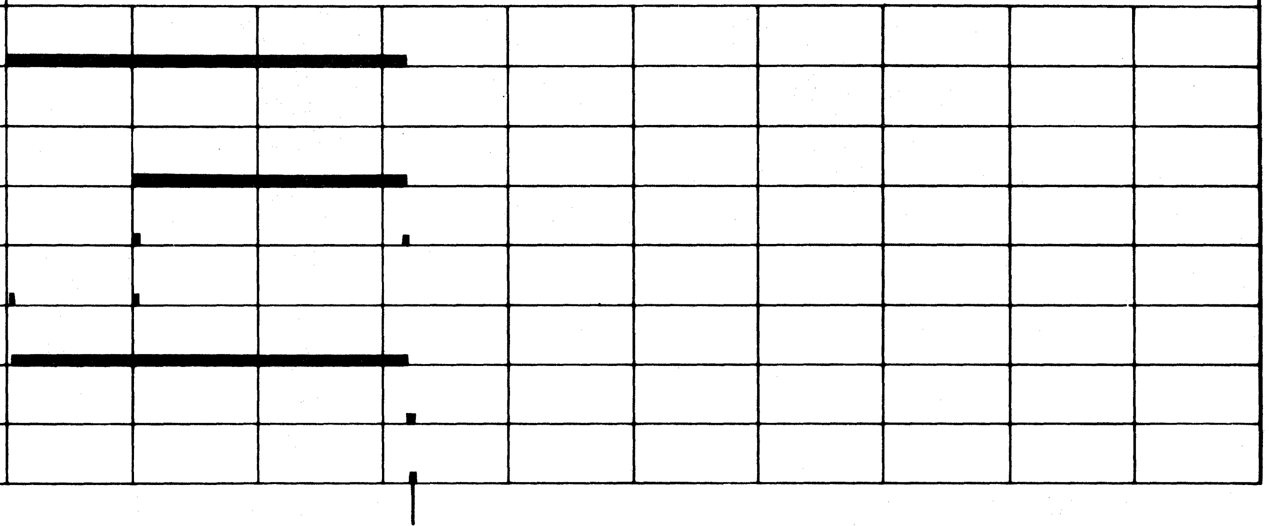
1. Load AF
2. Enter 10, 0x, 00, 00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 74,76
1	+CE Alert Execute Ind	BD210	A2L2 D13	B	
2	+G1	BH120	A2Q2 J09	E	
3	+G2	BH110	A2Q2 D05	C	
4	−Index Alert	BH170	A2Q2 J11	A	
5	+Normal End NPL	BE160	A2K2 D11	F	
6	−3330 Mode	BA140	A2F2 M04	H	
7	+Check End NPL	BE160	A2K2 D05	G	
8	−Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	D	



Line keys reference the diagram on DATA 246.

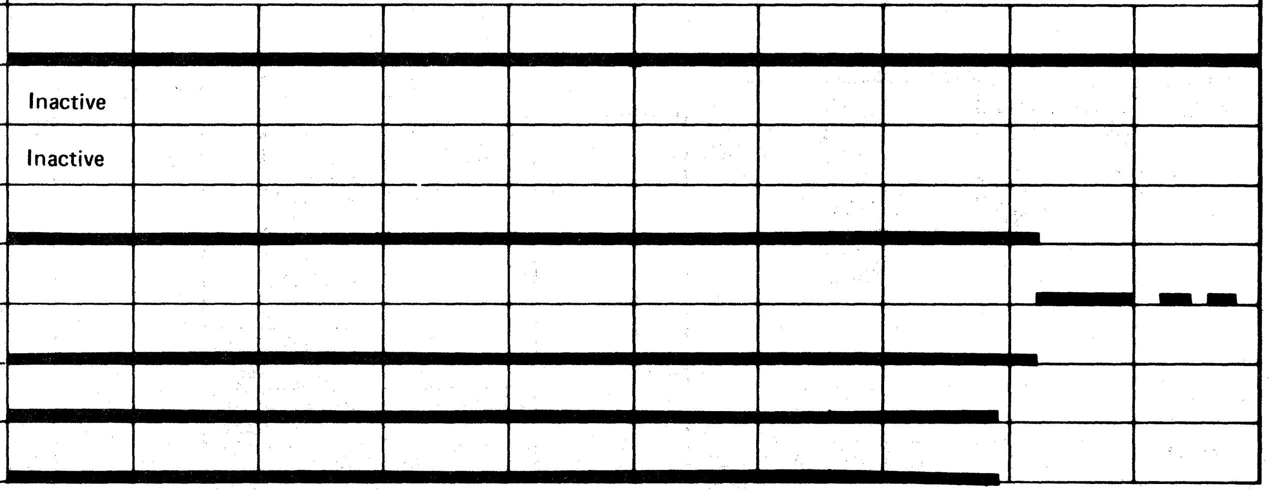
Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2D05
−G2
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 74,76
1	+CE Alert Execute Ind	BD210	A2L2 D13	B	
2	+G1	BH120	A2Q2 J09	E	Inactive
3	−G2	BH110	A2Q2 D05	C	Inactive
4	−Index Alert	BH170	A2Q2 J11	A	
5	+Normal End NPL	BE160	A2K2 D11	F	
6	−3330 Mode	BA140	A2F2 M04	H	
7	+Check End NPL	BE160	A2K2 D05	G	
8	−Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	D	



Line keys reference the diagram on DATA 246.

AF TEST 6 AND 7 SEQUENCE CHARTS

NATIVE MODE

Microdiagnostic Setup

Routine AF, test x { x = 6 for 3330-1 Compatibility Mode
x = 7 for Native Mode

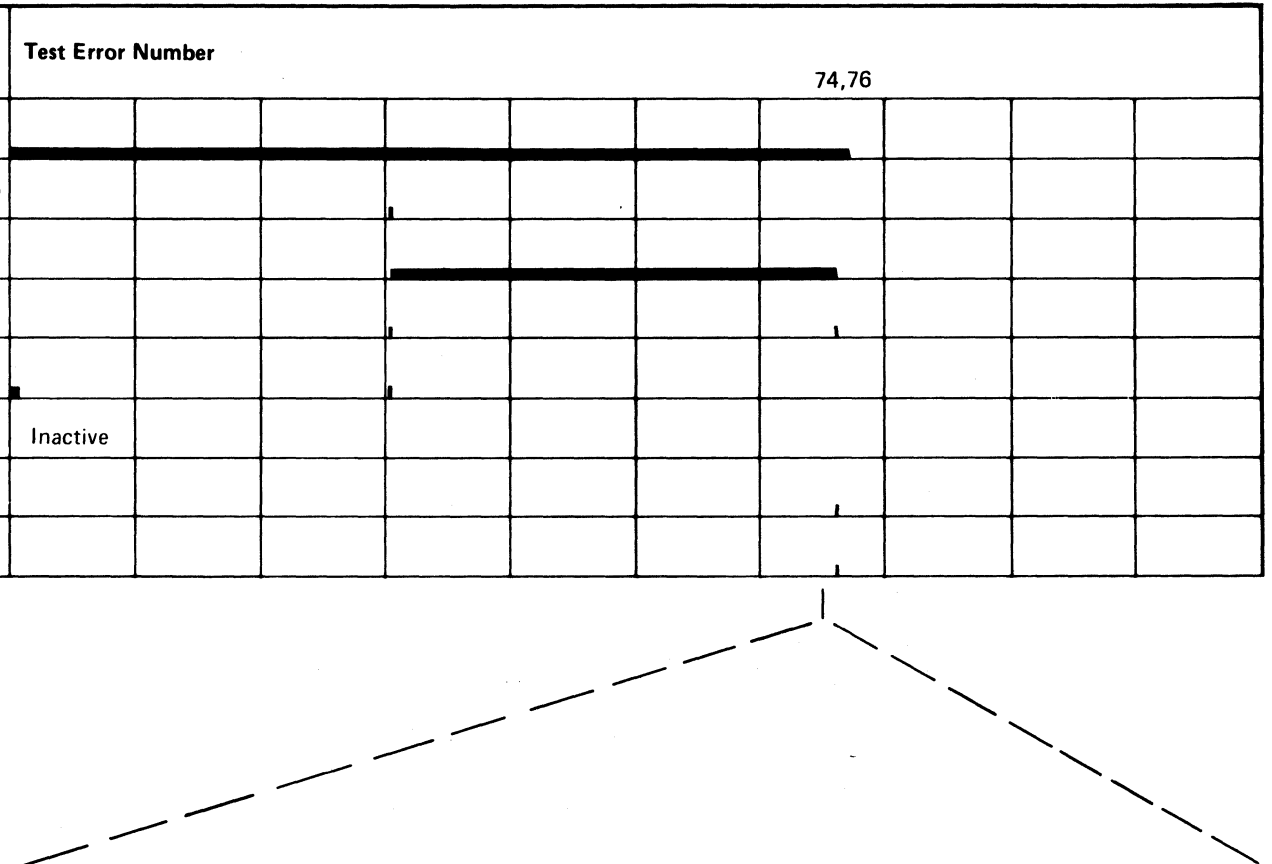
1. Load AF
2. Enter 10, 0x, 00, 00

Scope Setup

Sweep	5 ms/div	Ch 1	A2U4D13 +CE Alert Execute Ind
Mode	Alt or Chop	Volts/div	0.1
Trigger	Ext Slope (+) A2L2D13 +CE Alert Execute Ind	Probe	x10
		Ch 2	(see chart)

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 74,76
1	+CE Alert Execute Ind	BD210	A2L2 D13	B	
2	+G1	BH120	A2Q2 J09	E	
3	−G2	BH110	A2Q2 D05	C	
4	−Index Alert	BH170	A2Q2 J11	A	
5	+Normal End NPL	BE160	A2K2 D11	F	
6	−3330 Mode	BA140	A2F2 M04	H	Inactive
7	+Check End NPL	BE160	A2K2 D05	G	
8	−Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	D	



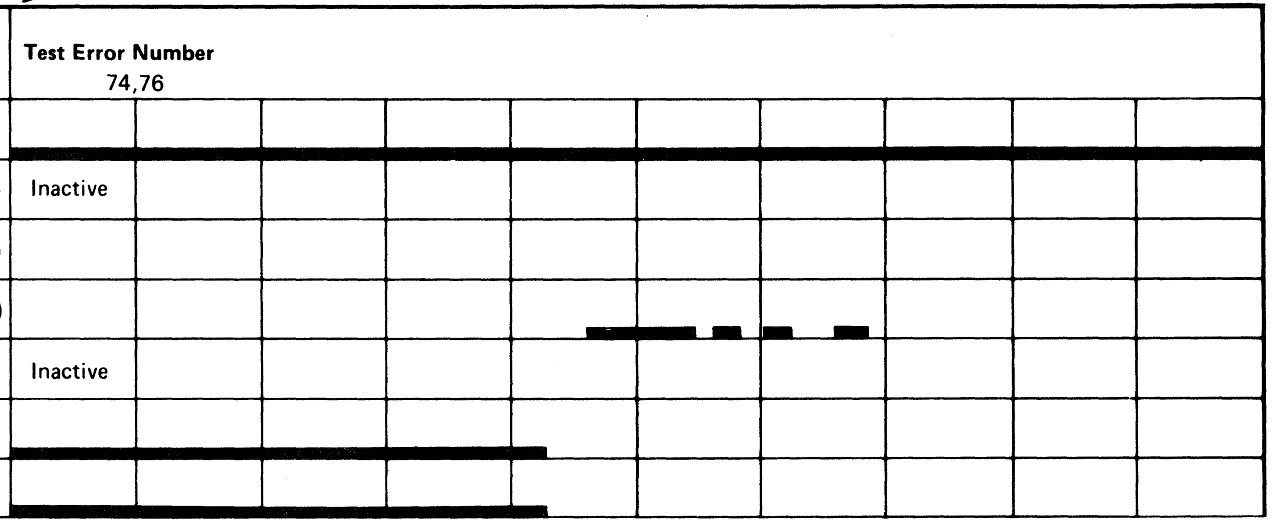
Line keys reference the diagram on DATA 246.

Scope Setup

Sweep	5 ms/div	Ch 1	A2Q2D05 −G2
Mode	Alt or Chop	Volts/div	0.1
Trigger	Ext Slope (+) A2L2D13 +CE Alert Execute Ind	Probe	x10
		Ch 2	(see chart)

Horz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 74,76
1	+CE Alert Execute Ind	BD210	A2L2 D13	B	
2	−G2	BH110	A2Q2 D05	C	Inactive
3	−Index Alert	BH170	A2Q2 J11	A	
4	+Normal End NPL	BE160	A2K2 D11	F	
5	−3330 Mode	BA140	A2F2 M04	H	Inactive
6	+Check End NPL	BE160	A2K2 D05	G	
7	−Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	D	



Line keys reference the diagram on DATA 246.

CE0315 Seq. 1 of 1	2358589 Part No.	441300 31 Mar 76	441303 30 Jul 76			

FORMAT FAILURE

ERROR DESCRIPTION

The following are conditions of the Format Latch operation:

- Padding takes place on format operations by checking that I Write Sense is still on after data and ECC Write operations are complete.
- Padding stops with Reset Read/Write command.

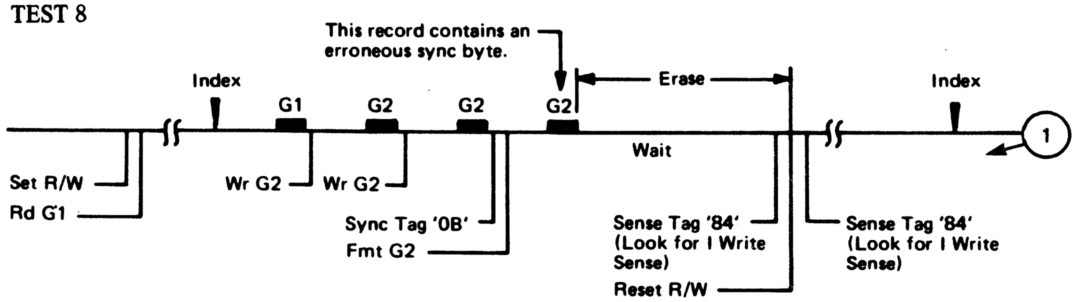
MICRODIAGNOSTIC DESCRIPTION

Routine AF, test 8 orients on Index and performs a Read G1 operation. The test then performs two Write G2 operations followed by a Format G2 operation. In addition to performing an I Write Sense test, these operations format the track for use in test 9.

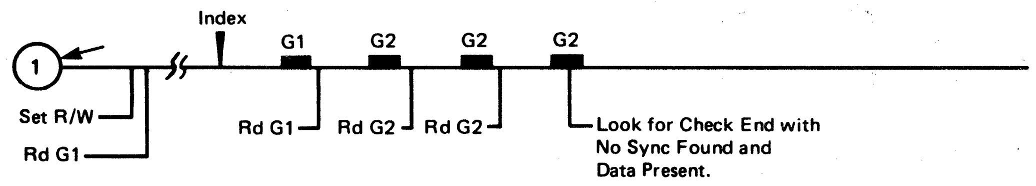
The Format G2 operation creates a record which, when read back, causes the No Sync Found and Data Present latches to be set.

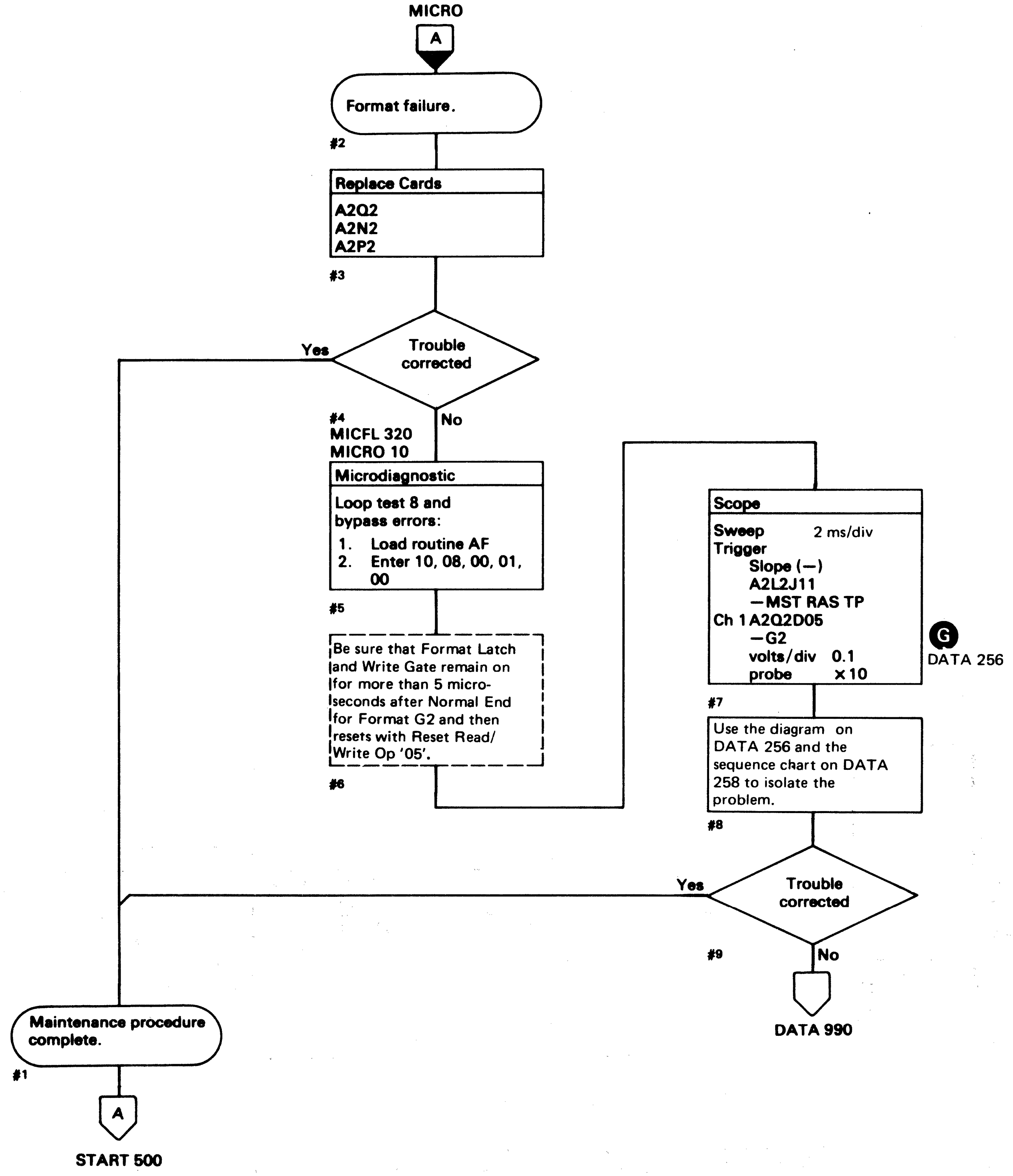
Routine AF, test 9 orients on the G1 Field, reads a G2, clocks a G2, and then reads the final G2 field. The last G2 field results in Check End with No Sync Found and Data Present.

TEST 8



TEST 9



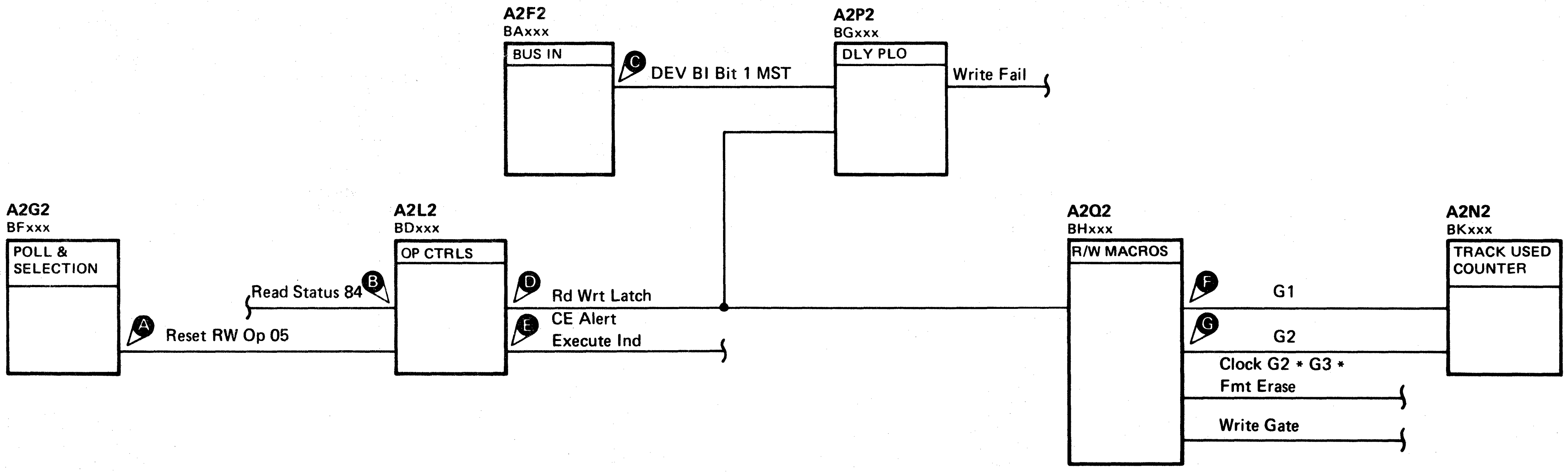


3350	CE0320 Seq. 1 of 2	2358590 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST 8 DIAGRAM

See the sequence chart on DATA 258 for referenced test points.

See OPER 240 for theory.



3350

CE0320 Seq. 2 of 2	2358590 Part No.

441300 31 Mar 76	441303 30 Jul 76			

AF TEST 8 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AF, test 8
1. Load AF
2. Enter 10, 08, 00, 00

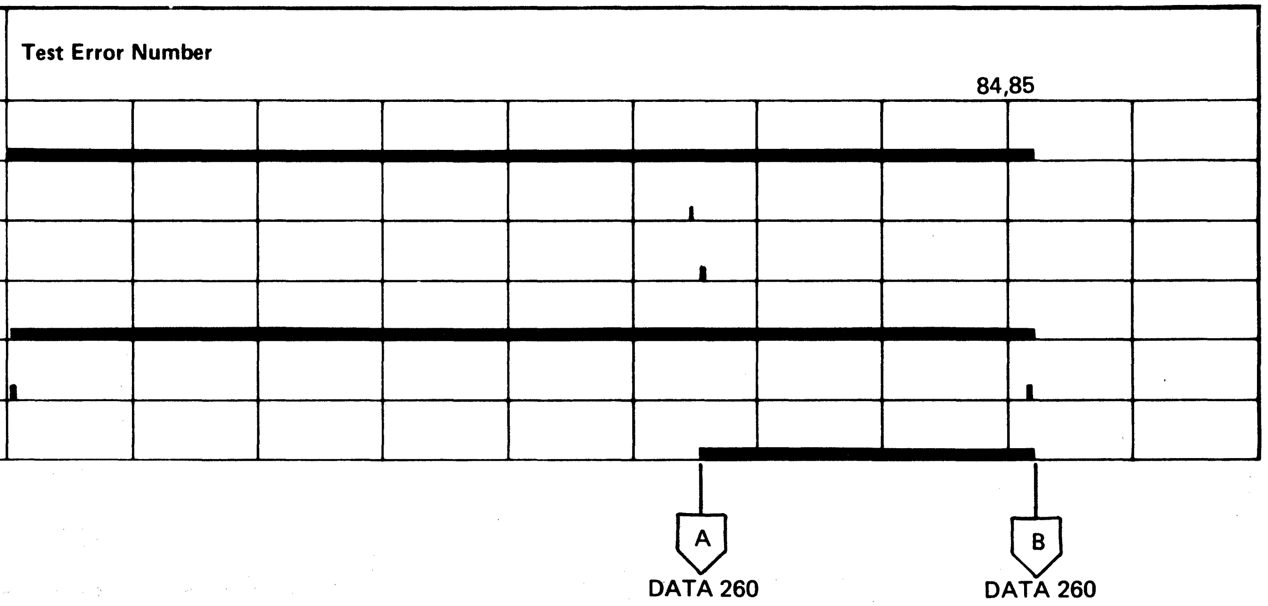
Scope Setup

Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	Ⓔ
2	+G1	BH120	A2Q2 J09	Ⓕ
3	−G2	BH120	A2Q2 D05	Ⓖ
4	−Rd Wrt Latch	BD150	A2L2 J03	Ⓓ
5	−Read Status 84	BF110	A2G2 D09	Ⓑ
6	+Dev BI Bit 1 MST	BA160	A2F2 S10	Ⓒ



Line keys reference the diagram on DATA 256.

(For expanded sequence chart)

CE0335 Seq. 1 of 2	2358591 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST 8 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

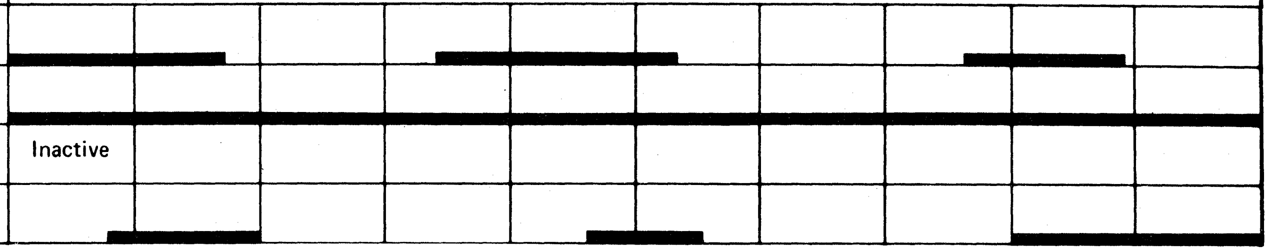
Ch 1 A2Q2D05
−G2
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 2 ms/div
Slope (–)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

DATA 258
A

Legend: ▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number None
1	−G2	BH120	A2Q2 D05	Ⓖ	
2	−Rd Wrt Latch	BD150	A2L2 J03	Ⓓ	
3	−Read Status 84	BF110	A2G2 D09	Ⓑ	
4	+Dev BI Bit 1 MST	BA160	A2FZ S10	Ⓒ	



Line keys reference the diagram on DATA 256.

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

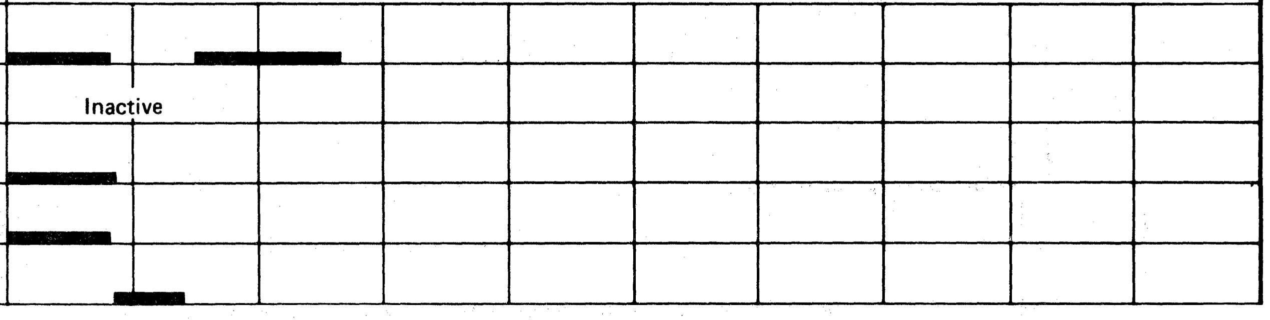
Ch 1 A2G2D09
−Read Status 84
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 2 ms/div
Slope (–)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

DATA 258
B

Legend: ▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 84 85
1	−Read Status 84	BF110	A2G2 D09	Ⓑ	
2	−G2	BH120	A2Q2 D05	Ⓖ	
3	−Rd Wrt Latch	BD150	A2L2 J03	Ⓓ	
4	+Dev BI Bit 1 MST	BA160	A2F2 S10	Ⓒ	
5	+Reset R/W Op 05	BF110	A2G2 D05	Ⓐ	



Line keys reference the diagram on DATA 256.

3350	CE0335 Seq. 2 of 2	2358591 Part No.	441300 31 Mar 76	441303 30 Jul 76

NO SYNC BYTE FOUND/DATA PRESENT

ERROR DESCRIPTION

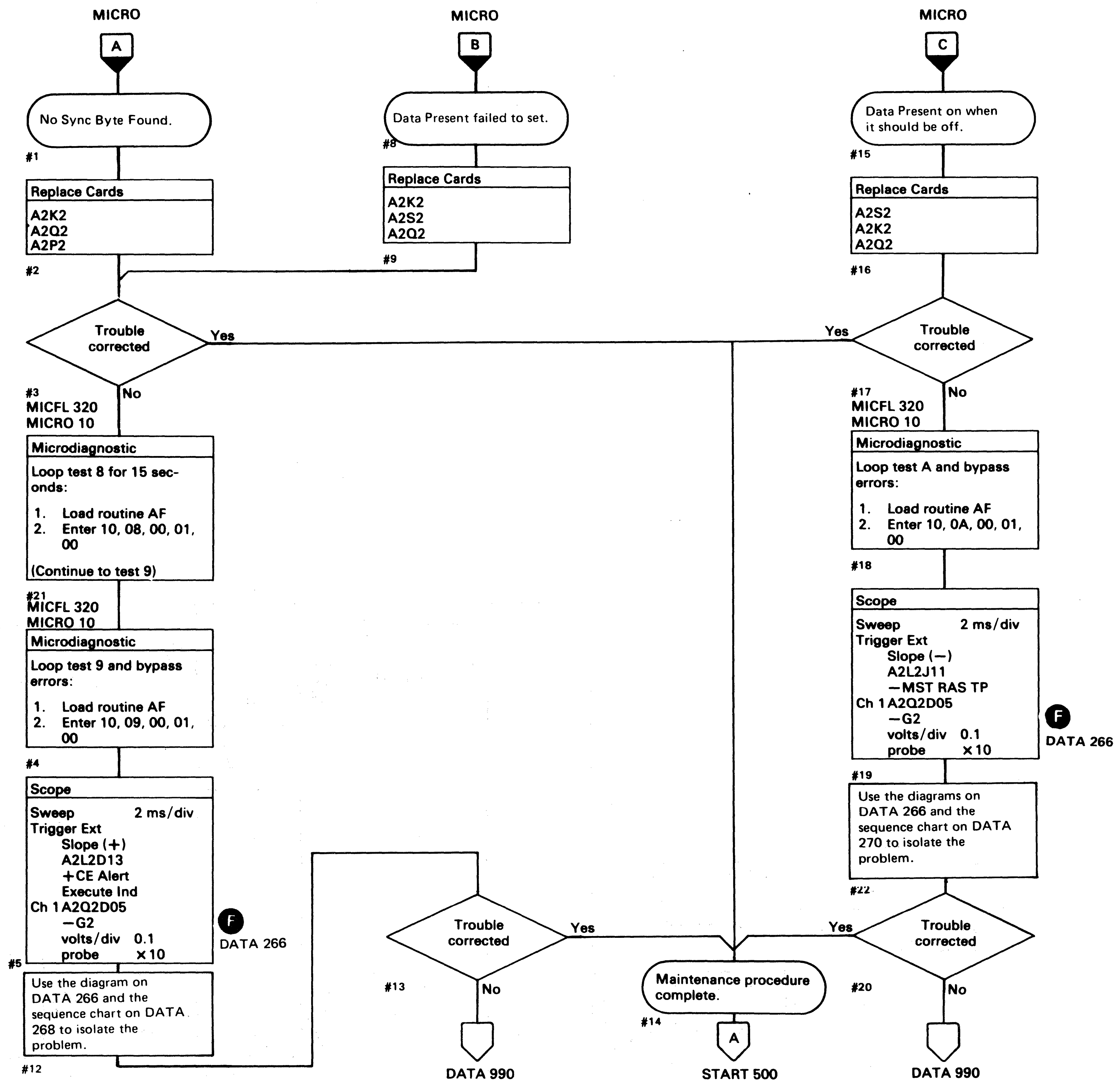
The Sync Byte ('19'), identifies the start of every field written on the disk. No Sync Byte Found is an indication that a Sync Byte was not found at the proper place on the disk. This would be a normal condition if the field did not exist. It is an error if the field exists but the Sync Byte cannot be determined.

The No Sync Byte Found latch causes a check condition which sets the End Data Op latch. End Data Op combined with the check condition causes a Check End to be sent to storage control.

If Bus In bit 5 is on during Check End, No Sync Byte is found. The No Sync Byte Found latch and the End Data Op latch are reset by the End Response signal from storage control. The Data Present latch monitors the Data area near the Sync Byte. If data is found but a Sync Byte cannot be decoded, the Data Present latch is set and indicated by Bus In bit 6 during Check End. Storage control analyzes No Sync Byte Found and Data Present to determine the status of the field involved. A No Sync Byte Found in a Data field causes a Data Check (Format 4, Message 7) regardless of the condition of the Data Present latch. A No Sync Byte Found in the Key field causes a Data Check (Format 4, Message 6) regardless of the condition of the Data Present latch.

Examples:

Record On Track	Operation	No Sync Byte Found	Data Present	Results
5	SCHIDEQ R5 TIC RD CKD	OFF ON	OFF OFF	Record does not exist. R0 is read.
6	SCHIDEQ R5 TIC RD CKD	OFF ON	OFF ON	Record 6 cannot be processed. Data Check with Count field. No Sync Byte Found (Format 4, Message 5 is indicated).
6	SCHIDEQ R6 TIC etc.	ON –	ON –	Search terminated. Data Check with Count field. No Sync Byte Found (Format 4, Message 5 is indicated).
5	SCHIDEQ R6 TIC etc.	ON	OFF	Search continues until two active Track Indexes and a No Record Found is posted.



AF TEST 9 AND A DIAGRAM

MICRODIAGNOSTIC DESCRIPTION

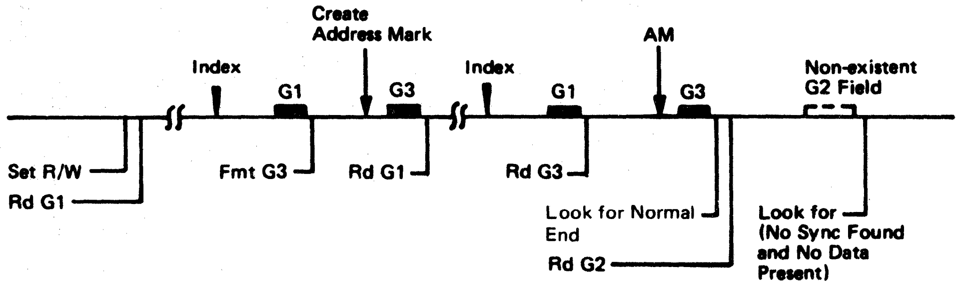
See DATA 254 for a description of routine AF, tests 8 and 9.

Routine AF, test A orients on Home Address (Read G1 operation) and performs a Format G3 operation which creates a G3 gap, generates an Address Mark, writes a record, and then erases the remainder of the track (Write Clock Bits to Index).

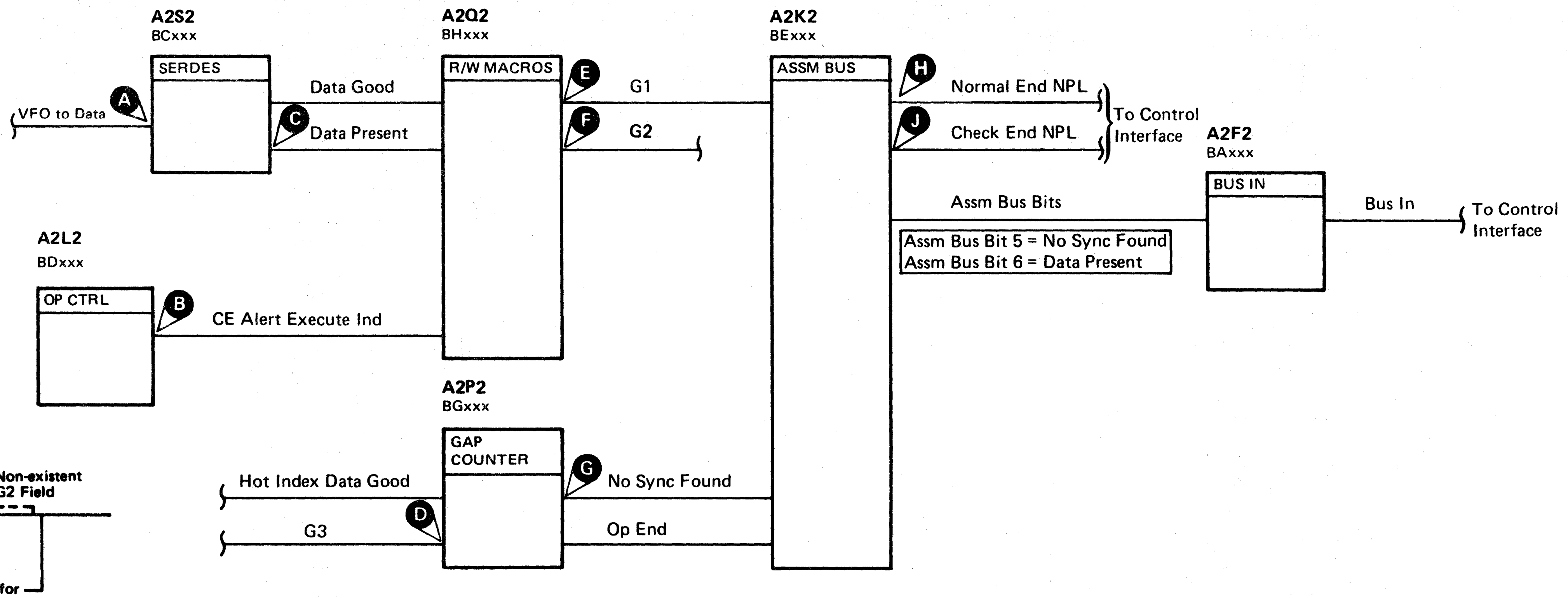
The Read portion of the test reads and verifies the Home Address and the record created.

The test then attempts to read another nonexistent field. The program checks for Check End with No Sync Found and No Data Present indicated.

See OPER 240 for additional theory.



See the sequence charts on DATA 268 and DATA 270 for referenced test points.



AF TEST 9 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Microdiagnostic Setup

Routine AF, Test 9
1. Load AF
2. Enter 10, 09, 00, 00

Scope Setup

Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A 2L2D13
+ CE Alert Execute Ind

Ch 1 A2U4D13
+ CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

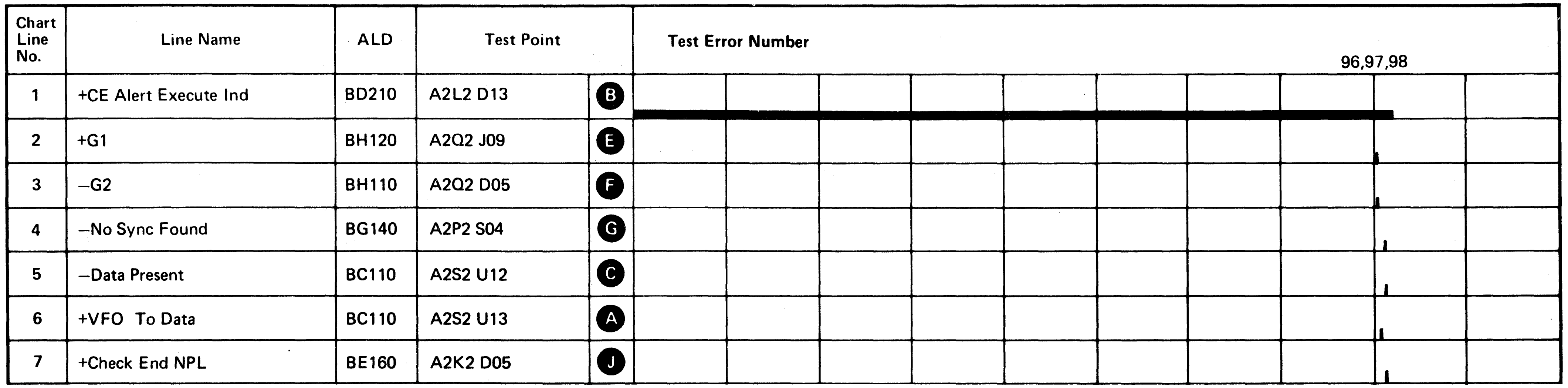


Chart Line No.	Line Name	ALD	Test Point		Test Error Number 96,97,98
1	+CE Alert Execute Ind	BD210	A2L2 D13	B	
2	+G1	BH120	A2Q2 J09	E	
3	–G2	BH110	A2Q2 D05	F	
4	–No Sync Found	BG140	A2P2 S04	G	
5	–Data Present	BC110	A2S2 U12	C	
6	+VFO To Data	BC110	A2S2 U13	A	
7	+Check End NPL	BE160	A2K2 D05	J	

Line keys reference the diagram on DATA 266.

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+ CE Alert Execute Ind

Ch1 A2Q2D05
–G2
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 2 msTdiv
Slope (–)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

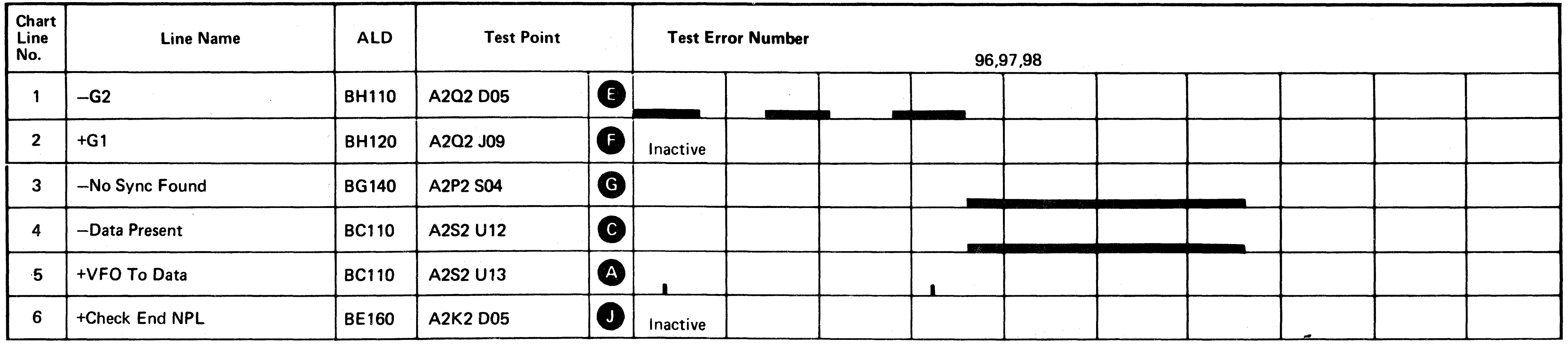


Chart Line No.	Line Name	ALD	Test Point		Test Error Number 96,97,98
1	–G2	BH110	A2Q2 D05	E	
2	+G1	BH120	A2Q2 J09	F	Inactive
3	–No Sync Found	BG140	A2P2 S04	G	
4	–Data Present	BC110	A2S2 U12	C	
5	+VFO To Data	BC110	A2S2 U13	A	
6	+Check End NPL	BE160	A2K2 D05	J	Inactive

Line keys reference the diagram on DATA 266.

AF TEST A SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AF, test A
1. Load AF
2. Enter 10, 0A, 00, 00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Legend: ▭ Inactive ■ Active level ▨ Tolerance

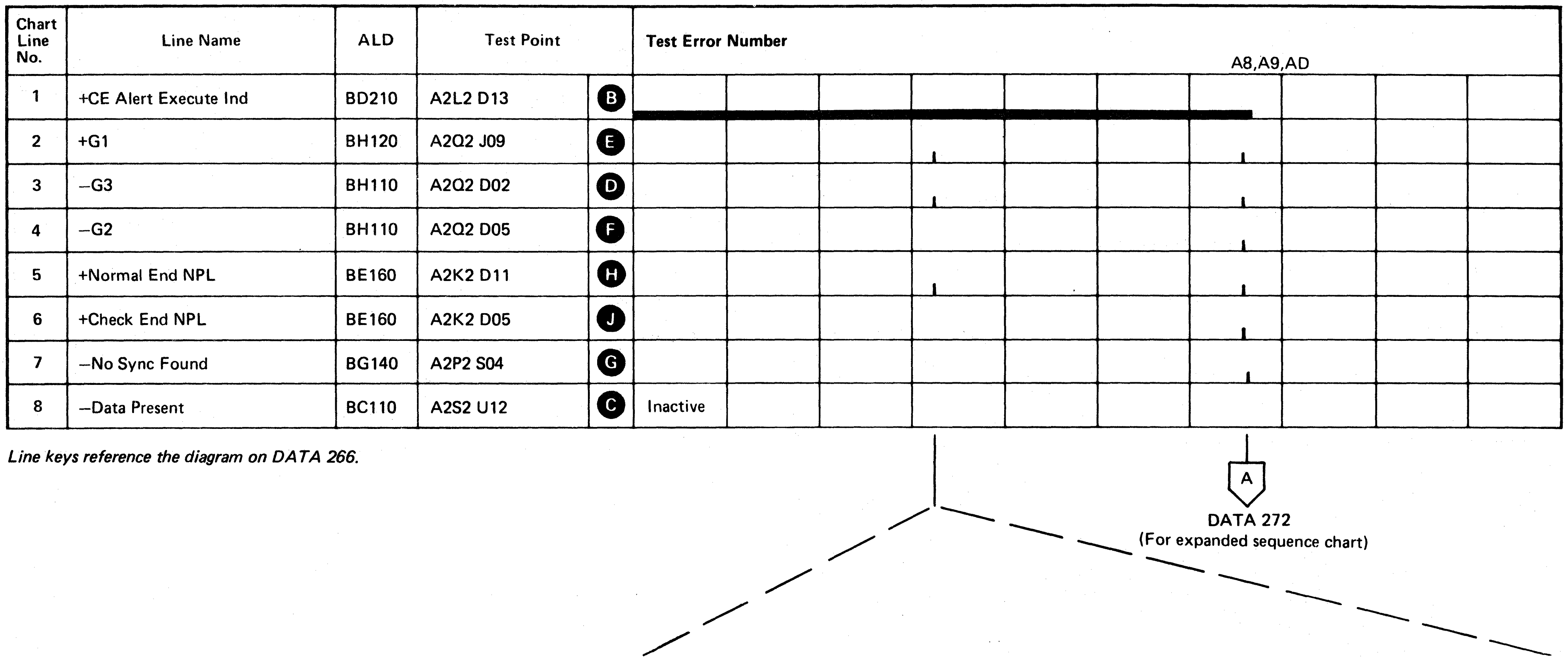


Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+CE Alert Execute Ind	BD210	A2L2 D13	B	
2	+G1	BH120	A2Q2 J09	E	
3	–G3	BH110	A2Q2 D02	D	
4	–G2	BH110	A2Q2 D05	F	
5	+Normal End NPL	BE160	A2K2 D11	H	
6	+Check End NPL	BE160	A2K2 D05	J	
7	–No Sync Found	BG140	A2P2 S04	G	
8	–Data Present	BC110	A2S2 U12	C	Inactive

Line keys reference the diagram on DATA 266.

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

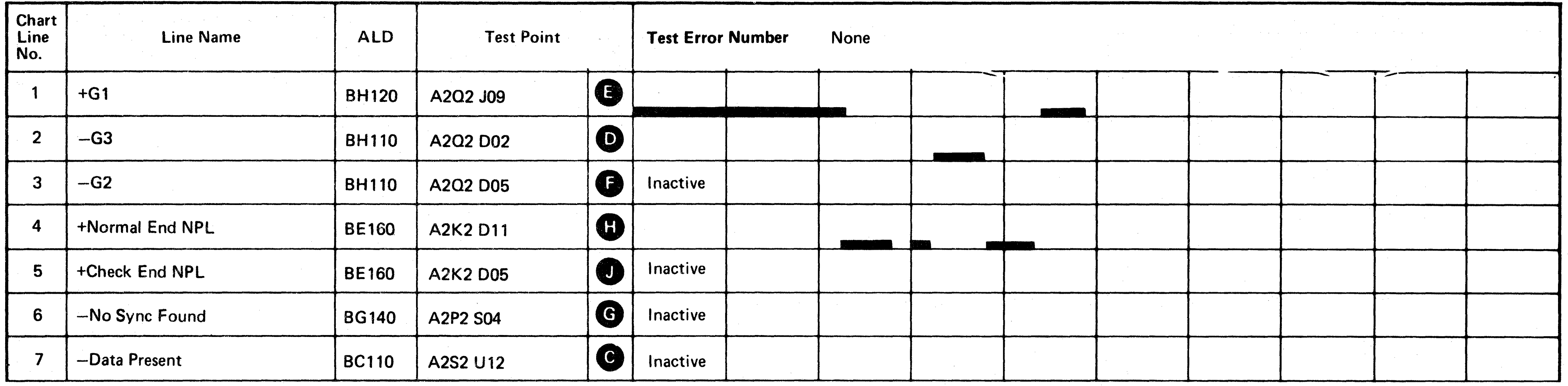


Chart Line No.	Line Name	ALD	Test Point		Test Error Number None
1	+G1	BH120	A2Q2 J09	E	
2	–G3	BH110	A2Q2 D02	D	
3	–G2	BH110	A2Q2 D05	F	Inactive
4	+Normal End NPL	BE160	A2K2 D11	H	
5	+Check End NPL	BE160	A2K2 D05	J	Inactive
6	–No Sync Found	BG140	A2P2 S04	G	Inactive
7	–Data Present	BC110	A2S2 U12	C	Inactive

Line keys reference the diagram on DATA 266.

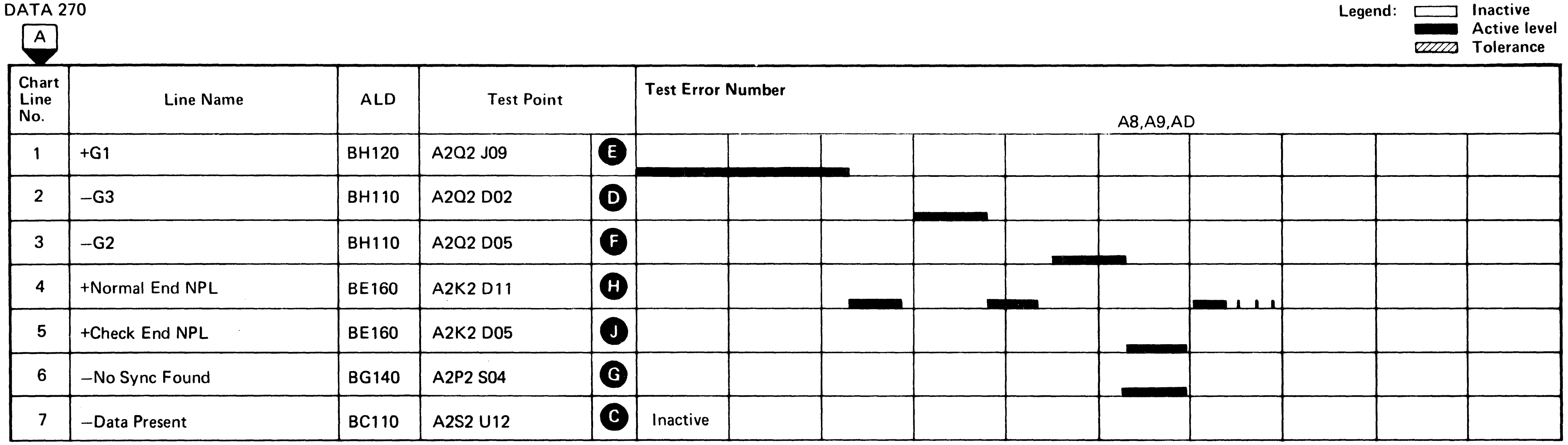
AF TEST A SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B time/Div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 3.5
Source – Int Ch 1

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (see chart)



Legend: ▭ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+G1	BH120	A2Q2 J09	E	
2	–G3	BH110	A2Q2 D02	D	
3	–G2	BH110	A2Q2 D05	F	
4	+Normal End NPL	BE160	A2K2 D11	H	
5	+Check End NPL	BE160	A2K2 D05	J	
6	–No Sync Found	BG140	A2P2 S04	G	
7	–Data Present	BC110	A2S2 U12	C	Inactive

Line keys reference the diagram on DATA 266.

CE0365 Seq. 1 of 1	2358594 Part No.	441300 31 Mar 76	441303 30 Jul 76			

NO ADDRESS MARK (AM) FOUND

ERROR DESCRIPTION

For normal operation, No AM Found indicates that an Index Mark was received before an Address Mark during an Address Mark Search operation. In most cases, AM Search is used to establish orientation; however, when an Index Mark is encountered, it establishes orientation. Degraded throughput suggests AM Search problems, since Index Mark is the only orientation point.

Routine AF tests Address Mark creation, AM Search, and No AM Found circuits.

No AM Found becomes active which sets Check End. When Check End is active, Bus In bit 4 indicates as follows for:

- Read Operations except Rd G3 AM Search

Bus In bits 3 and 4 identify an ECC Data Check. If Bus In bit 4 is on and bit 3 is off, an ECC Hardware Check is indicated and an Equipment Check is posted.

- Rd G3 AM Search Operation

If no data has been transferred, Bus In bit 4 indicates that no AM was found.

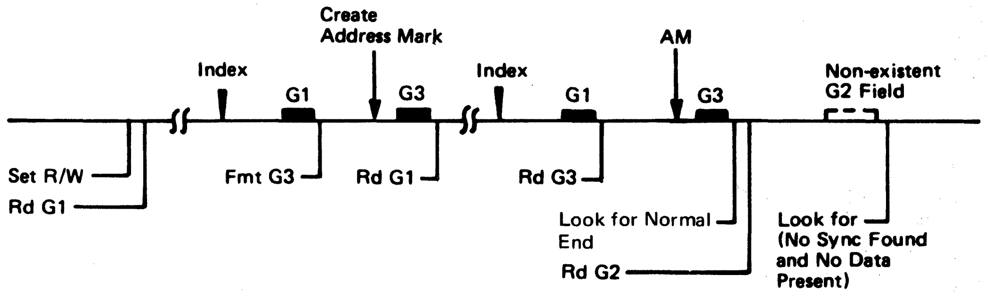
If data has been transferred, Bus In bit 4 is on and bit 3 is off, an ECC Hardware Check occurred, and an Equipment Check is posted.

MICRODIAGNOSTIC DESCRIPTION

Routine AF, test A orients on Home Address (Read G1 operation) and performs a Format G3 operation which creates a G3 gap, generates an Address Mark, writes a record, and then erases the remainder of the track (Write Clock Bits to Index).

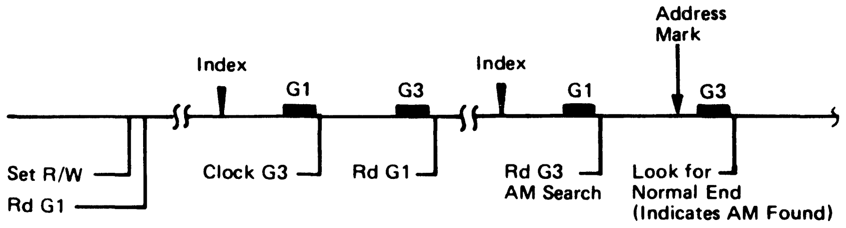
The Read portion of the test reads and verifies the Home Address and the record created.

The test then attempts to read another nonexistent field. The program checks for Check End with No Sync Found and No Data Present indicated.

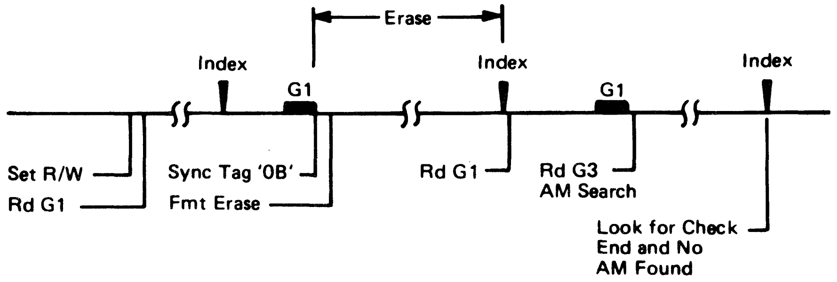


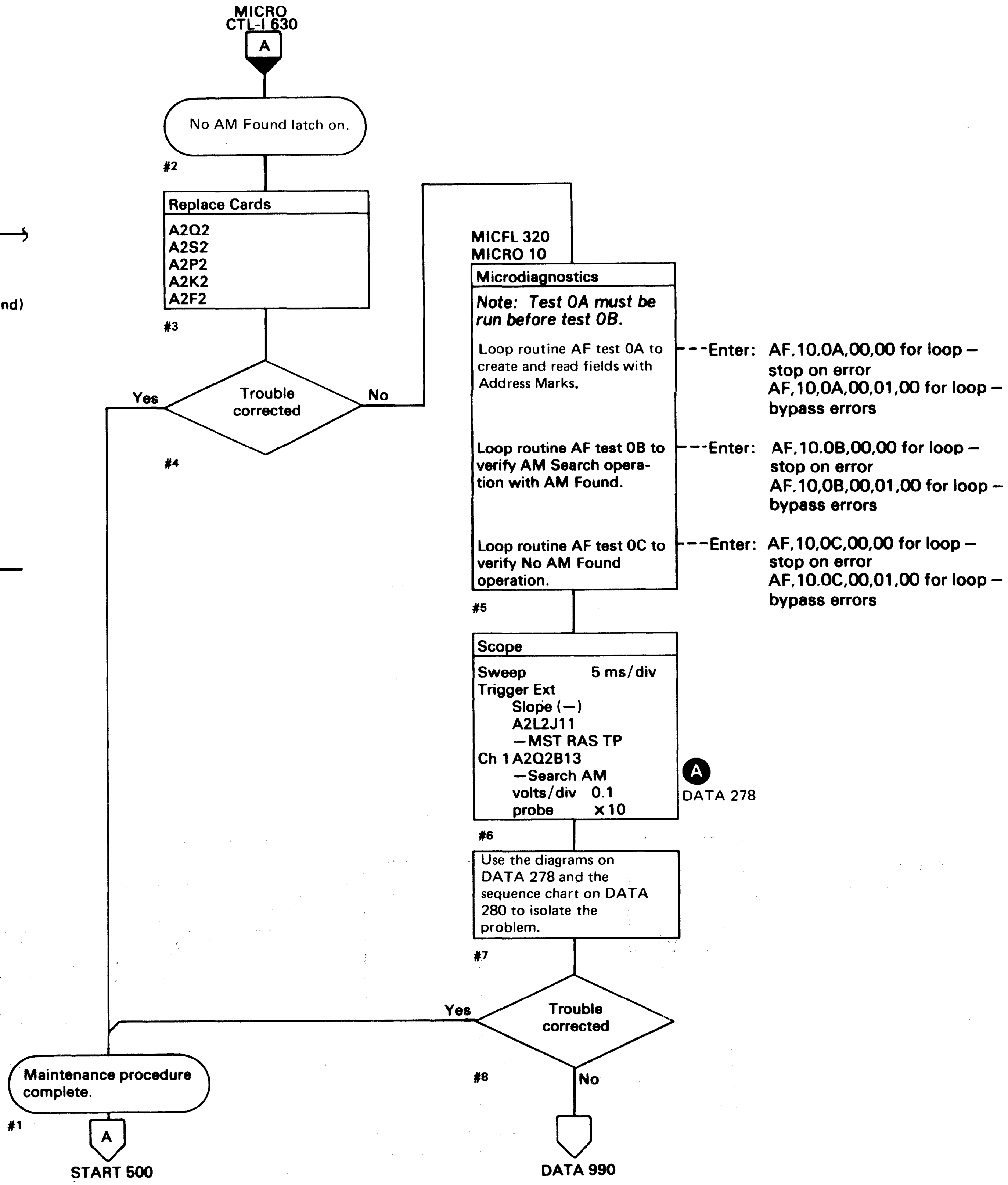
Routine AF, test B uses the data formatted in routine AF test A. The test orients on the Home Address and performs a Clock G3 operation.

If successful, the test again orients on Home Address and performs a Read G3 AM Search operation. Failure to read or decode an Address Mark results in an error.



Routine AF, test C formats a track with a Home Address only and erases the G3 field previously written. The test then orients on the Home Address and attempts to perform an Address Mark Search operation. No AM Found is the expected result.

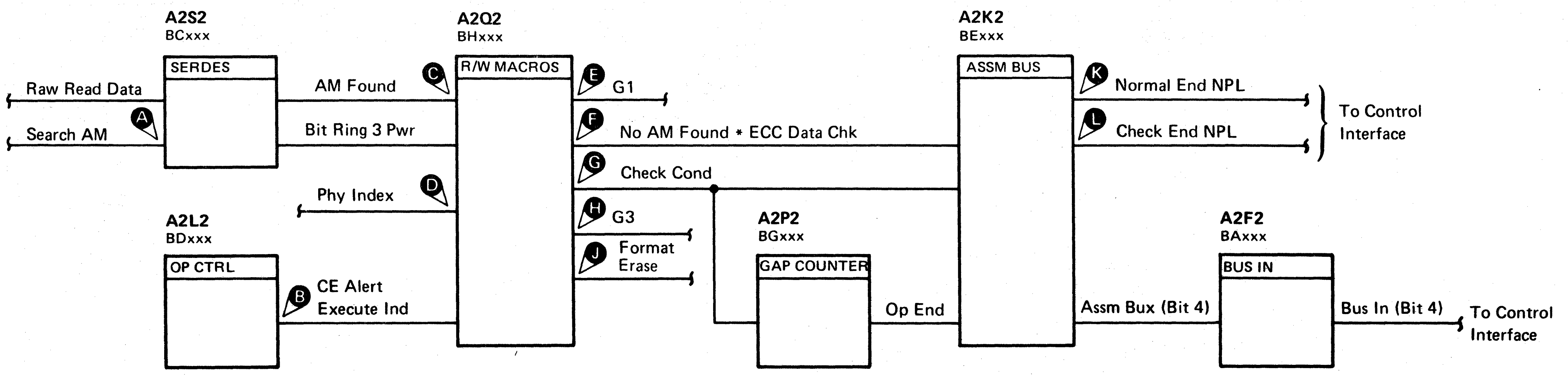




AF TEST C DIAGRAM

See the sequence chart on DATA 280 for referenced test points.

See OPER 240 for theory.



3350	CE0385 Seq. 2 of 2	2358595 Part No.	441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77		

AF TEST C SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

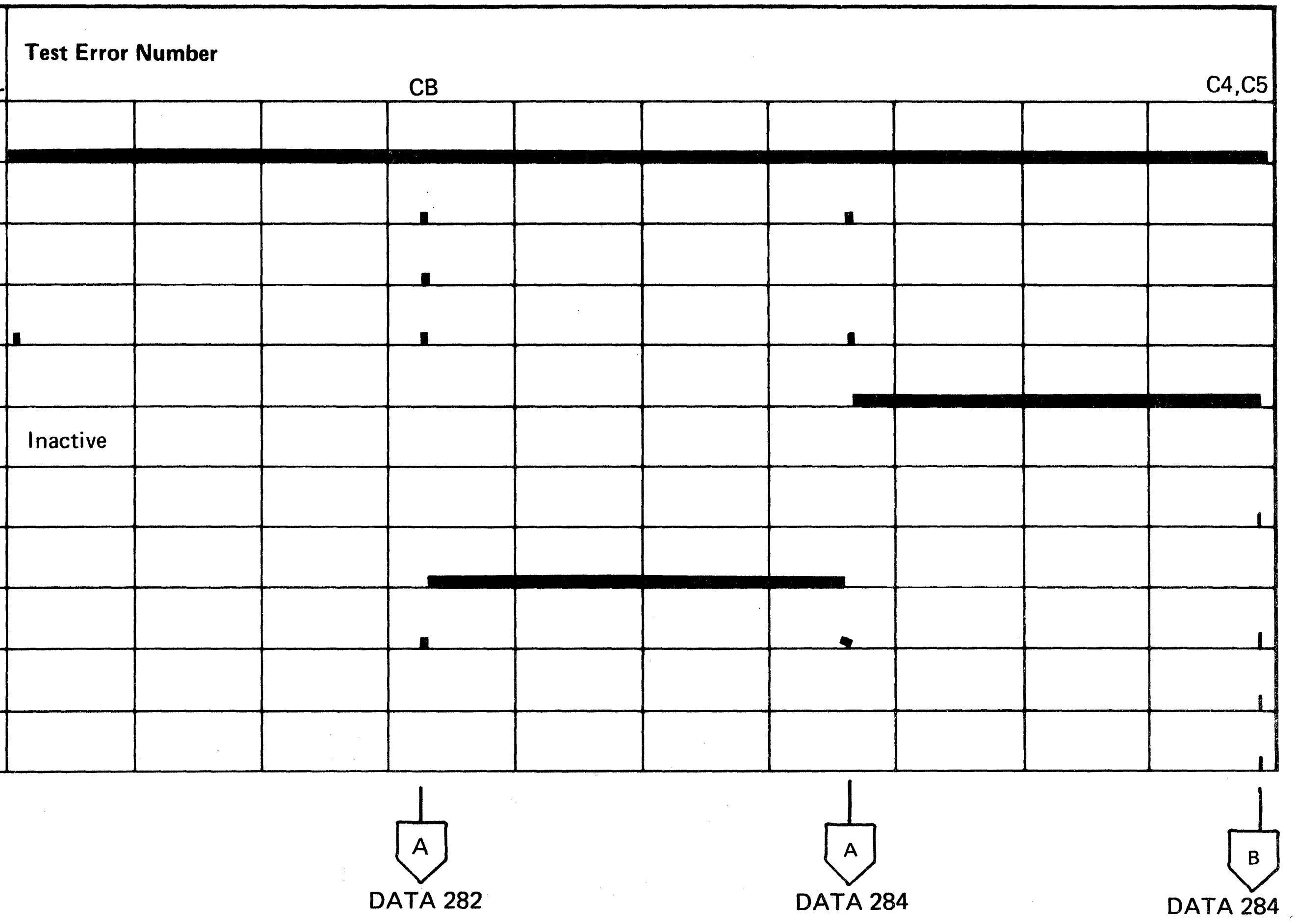
Routine AF, test C
1. Load AF
2. Enter 10, 0C, 00, 00

Scope Setup

Sweep	5 ms/div	Ch 1 A2U4D13	
Mode	Alt or Chop	+CE Alert Execute Ind	
Trigger	Ext		
Slope (+)		Volts/div	0.1
A2L2D13		Probe	x10
+CE Alert Execute Ind		Ch 2 (see chart)	

Legend: ▭ Inactive ▬ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	B
2	+G1	BH120	A2Q2 J09	E
3	−G3	BH110	A2Q2 D02	H
4	+Normal End NPL	BE160	A2K2 D11	K
5	−Search AM	BC140	A2S2 B03	A
6	−AM Found	BH130	A2Q2 G13	C
7	−No AM Found*ECC Data Chk	BH140	A2Q2 J13	F
8	+Format Erase	BH110	A2Q2 G02	J
9	−Phy Index	BH140	A2Q2 S07	D
10	+Check Cond	BH150	A2Q2 B12	G
11	+Check End NPL	BE160	A2K2 D05	L



Line keys reference the diagram on DATA 278.

(For expanded sequence chart)

3350	CE0390 Seq. 1 of 2	2358596 Part No.	441300 31 Mar 76	441303 30 Jul 76	441308 18 Aug 78		

AF TEST C SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Ch 1 A2L2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (see chart)

DATA 280
A

Legend: ▭ Inactive
■ Active level
▨ Tolerance

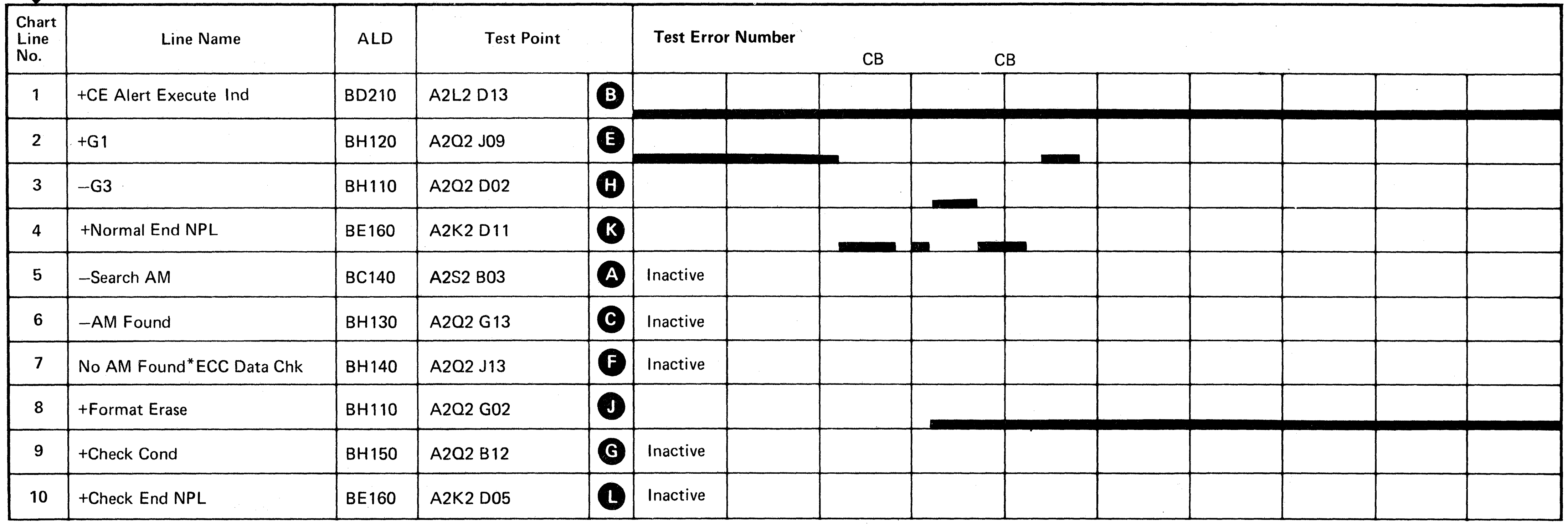


Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+CE Alert Execute Ind	BD210	A2L2 D13	B	
2	+G1	BH120	A2Q2 J09	E	
3	–G3	BH110	A2Q2 D02	H	
4	+Normal End NPL	BE160	A2K2 D11	K	
5	–Search AM	BC140	A2S2 B03	A	Inactive
6	–AM Found	BH130	A2Q2 G13	C	Inactive
7	No AM Found*ECC Data Chk	BH140	A2Q2 J13	F	Inactive
8	+Format Erase	BH110	A2Q2 G02	J	
9	+Check Cond	BH150	A2Q2 B12	G	Inactive
10	+Check End NPL	BE160	A2K2 D05	L	Inactive

Line keys reference the diagram on DATA 278.

CE0390 Seq. 2 of 2	2358596 Part No.	441300 31 Mar 76	441303 30 Jul 76	441308 18 Aug 78		

AF TEST C SEQUENCE CHART

TRIGGERING INSTRUCTIONS

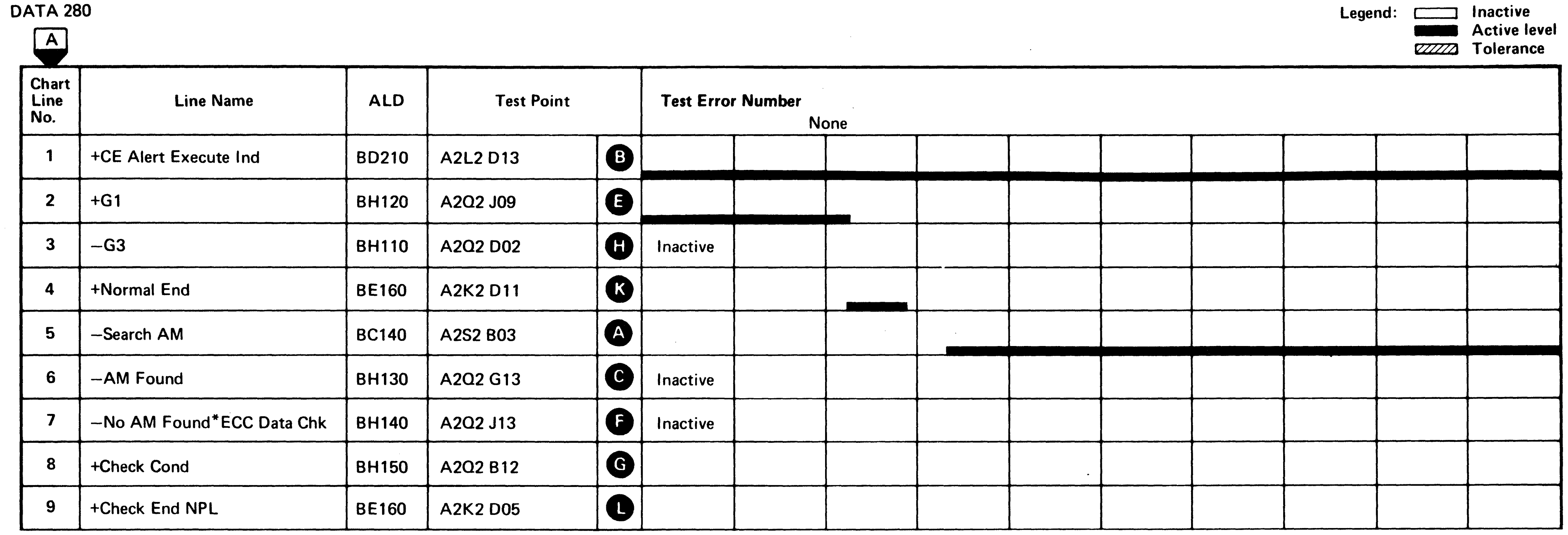
Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 µs/div
Delay-Time Multiplier – 3.5
Source – Int Ch 1

Ch 1 A2Q2J09
+G1
Volts/div
Probe
Ch 2 (see chart)

DATA 280

A



Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number None
1	+CE Alert Execute Ind	BD210	A2L2 D13	B	
2	+G1	BH120	A2Q2 J09	E	
3	–G3	BH110	A2Q2 D02	H	Inactive
4	+Normal End	BE160	A2K2 D11	K	
5	–Search AM	BC140	A2S2 B03	A	
6	–AM Found	BH130	A2Q2 G13	C	Inactive
7	–No AM Found*ECC Data Chk	BH140	A2Q2 J13	F	Inactive
8	+Check Cond	BH150	A2Q2 B12	G	
9	+Check End NPL	BE160	A2K2 D05	L	

Line keys reference the diagram on DATA 278.

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (–)
Delay Time-Delayed Sweep – 10 µs/div
Delay-Time Multiplier – 6.5
Source – Int Ch 1

Ch 1 A2Q2S07
–Phy Index
Volts/div 0.1
Probe x10
Ch 2 (see chart)

DATA 280

B

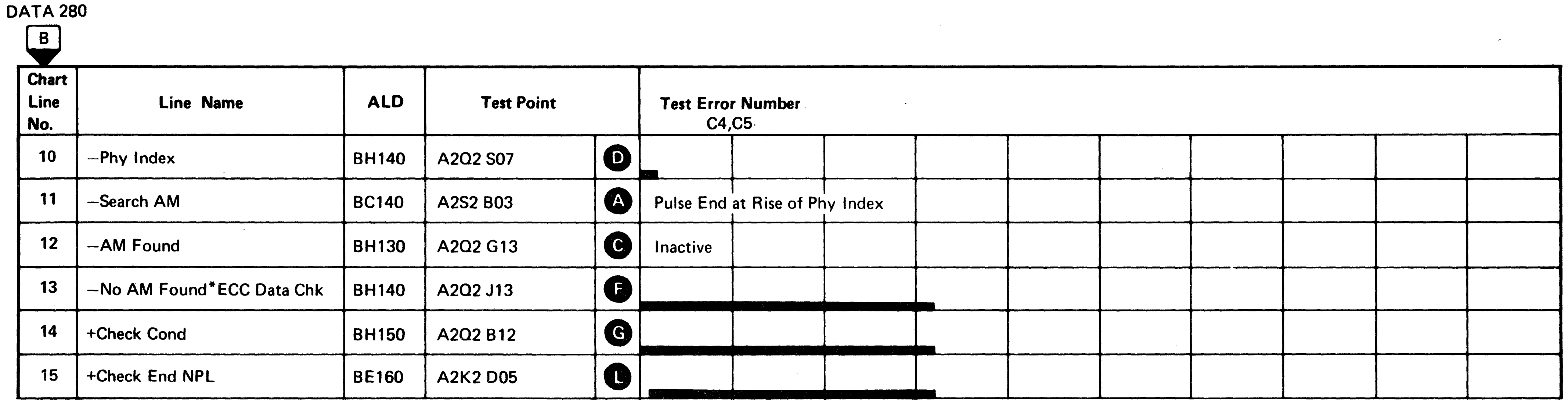


Chart Line No.	Line Name	ALD	Test Point		Test Error Number C4,C5
10	–Phy Index	BH140	A2Q2 S07	D	
11	–Search AM	BC140	A2S2 B03	A	Pulse End at Rise of Phy Index
12	–AM Found	BH130	A2Q2 G13	C	Inactive
13	–No AM Found*ECC Data Chk	BH140	A2Q2 J13	F	
14	+Check Cond	BH150	A2Q2 B12	G	
15	+Check End NPL	BE160	A2K2 D05	L	

Line keys reference the diagram on DATA 278.

3350	CE0505 Seq. 1 of 1	2358597 Part No.	441300 31 Mar 76	441303 30 Jul 76			

MISSING SERVO PULSES OR DATA BITS

ERROR DESCRIPTION

The Variable Frequency Oscillator (VFO) requires entry of pulses from the servo of data circuits to maintain the proper frequency.

Servo pulses from the HDA are used to control the VFO at all times in Read/Write mode except while in a Read operation. Missing servo pulses causes the VFO to operate at the wrong frequency. During this time, a continual check is made for missing pulses.

Raw Read Data is used to control the VFO during Read operations. In addition, the Raw Read Data bits are used to establish a clock/data bit relationship during the VFO Fast Sync time. A check for missing data bits is made during VFO Fast Sync time.

This test checks the ability of the machine to detect missing servo and data pulses. It also tests the ability to reset the error latch.

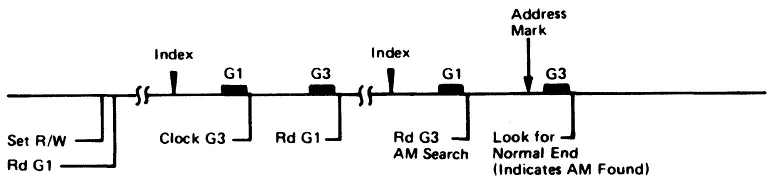
MICRODIAGNOSTIC DESCRIPTION

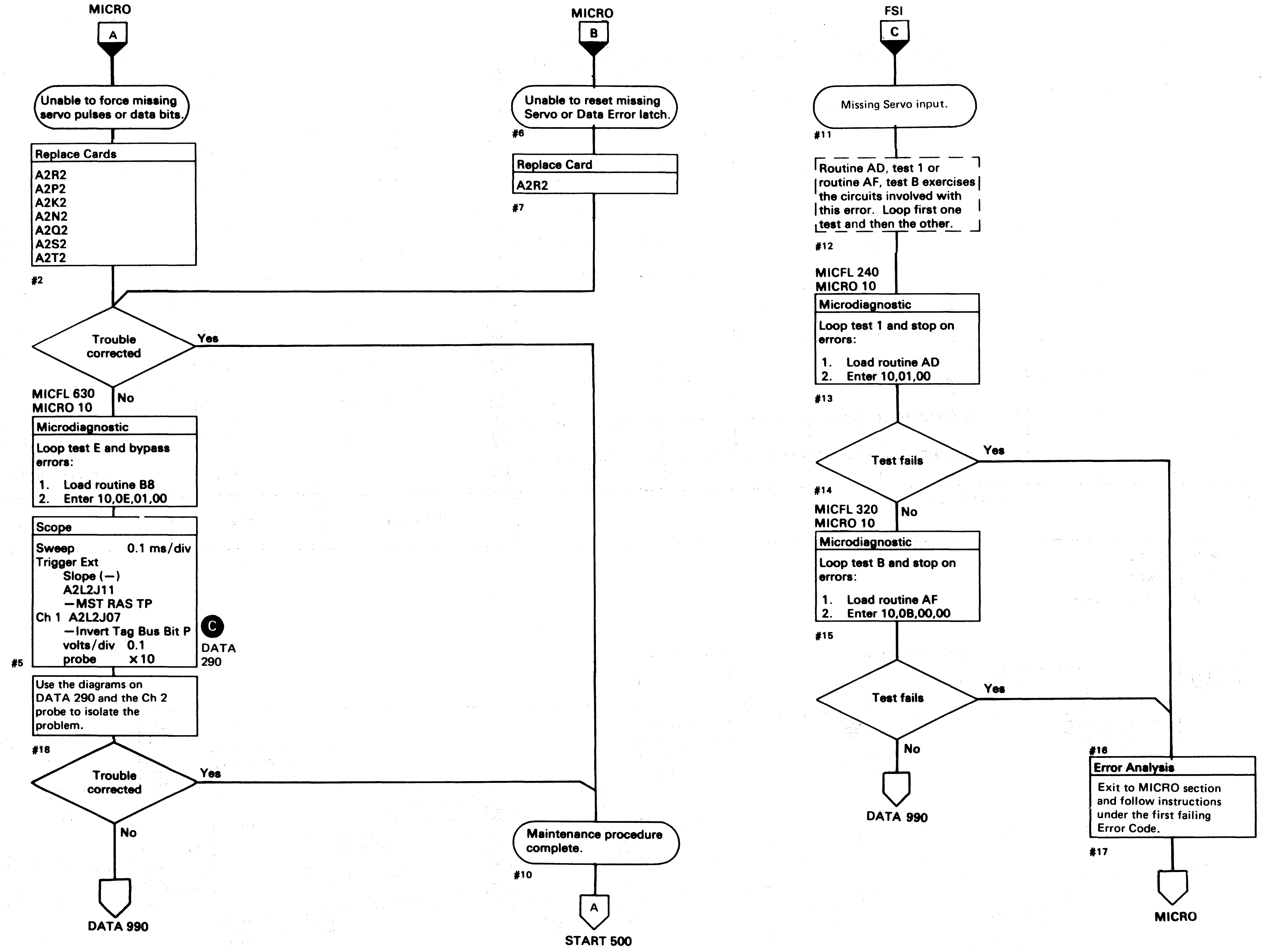
See DATA 74 for a description of routine AD, test 1.

See DATA 300 for a description of routine B8, test E.

Routine AF, test B uses the data formatted in routine AF, test A. The test orients on the Home Address and performs a Clock G3 operation.

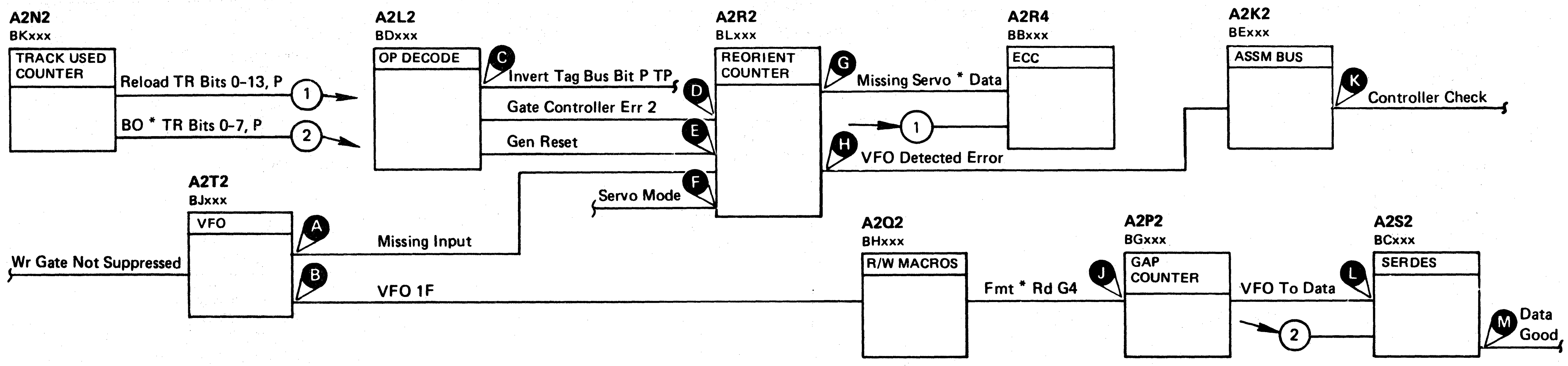
If successful, the test again orients on Home Address and performs a Read G3 AM Search operation. Failure to read or decode an Address Mark results in an error.





MISSING SERVO PULSES OR DATA BITS

See OPER 230 for theory.



Legend: ▭ Inactive ▬ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number E2,E3 E4,E5 E6,E7
1	–Invert Tag Bus Bit P TP	BD170	A2L2 J07	C	
2	–VFO Detected Error	BL140	A2R2 G05	H	
3	–Gate Controller Err 2	BL140	A2R2 G03	D	
4	+Gen Reset	BL140	A2R2 B13	E	
5	+Missing Servo * Data	BL140	A2R2 G07	G	
6	+Servo Mode	BL120	A2R2 D03	F	Inactive
7	–Controller Check	BE130	A2K2 M12	K	
8	–Data Good	BC110	A2S2 U03	M	Inactive
9	+VFO To Data	BC140	A2S2 U13	L	Inactive
10	–Fmt * Rd G4	BG170	A2P2 D06	J	Inactive
11	–VFO 1F	BJ130	A2T2 D10	B	High frequency pulses*
12	–Missing Input	BJ120	A2T2 B10	A	

*See DATA 996 for a description of pulse duration and repetition rate.

MONITOR CHECK CHECKER

ERROR DESCRIPTION

This test uses a diagnostic decode to block the Function pulses to the Monitor Check circuits. Missing Function pulses set the checker. The test verifies the setting and resetting of the checker.

A test is made to verify that the Controller Check is active while the Monitor Check is on.

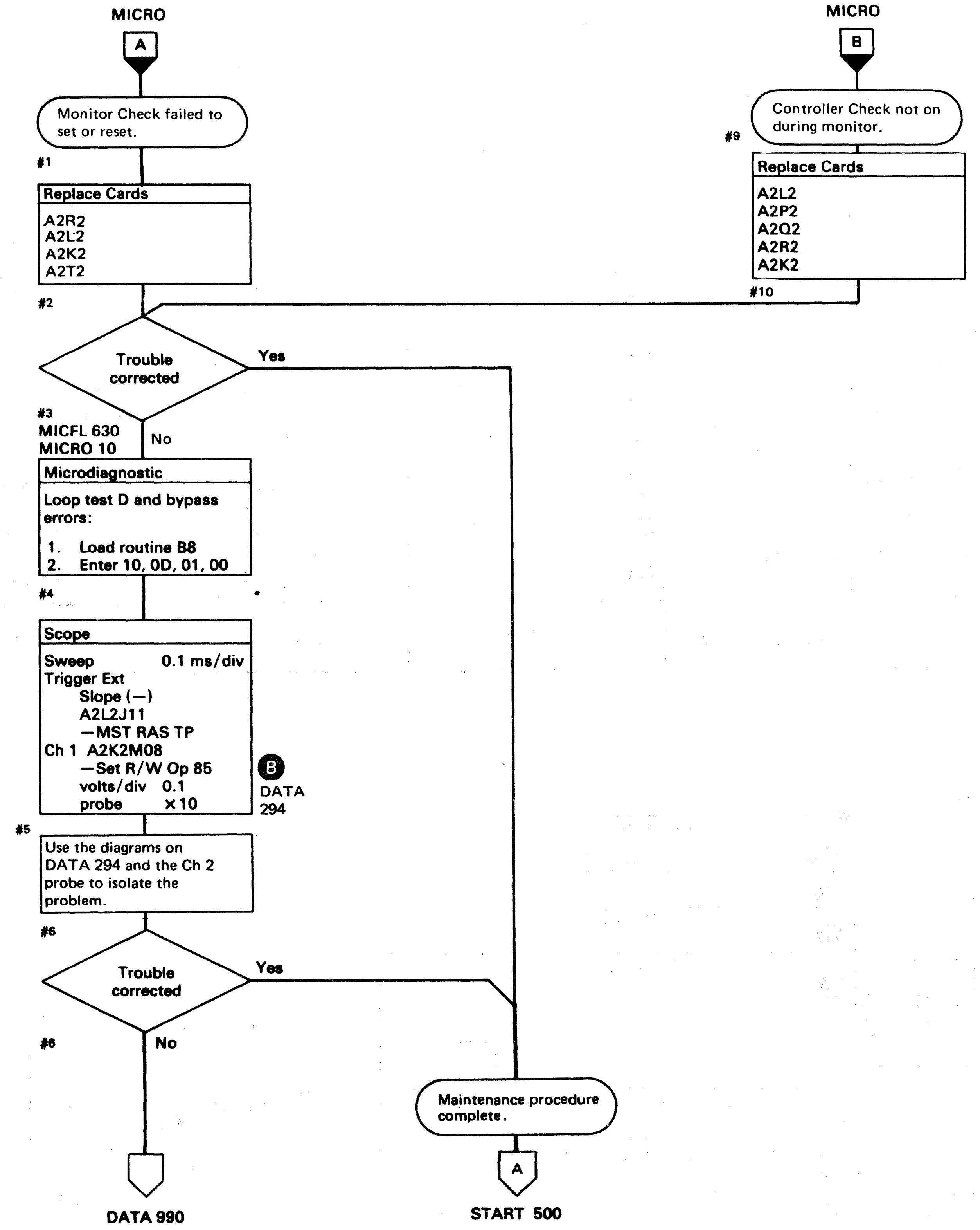
MICRODIAGNOSTIC DESCRIPTION

Routine B8, test D verifies that a Set Read/Write operates in the following way:

1. Functions as in Extended Operation; that is, does not return Normal End with Tag Valid.
2. Returns Normal End at the proper time to signify completion of the operation.

Test D also verifies that Normal End is reset by the End Response tag. Check conditions that occur during this operation are also indicated.

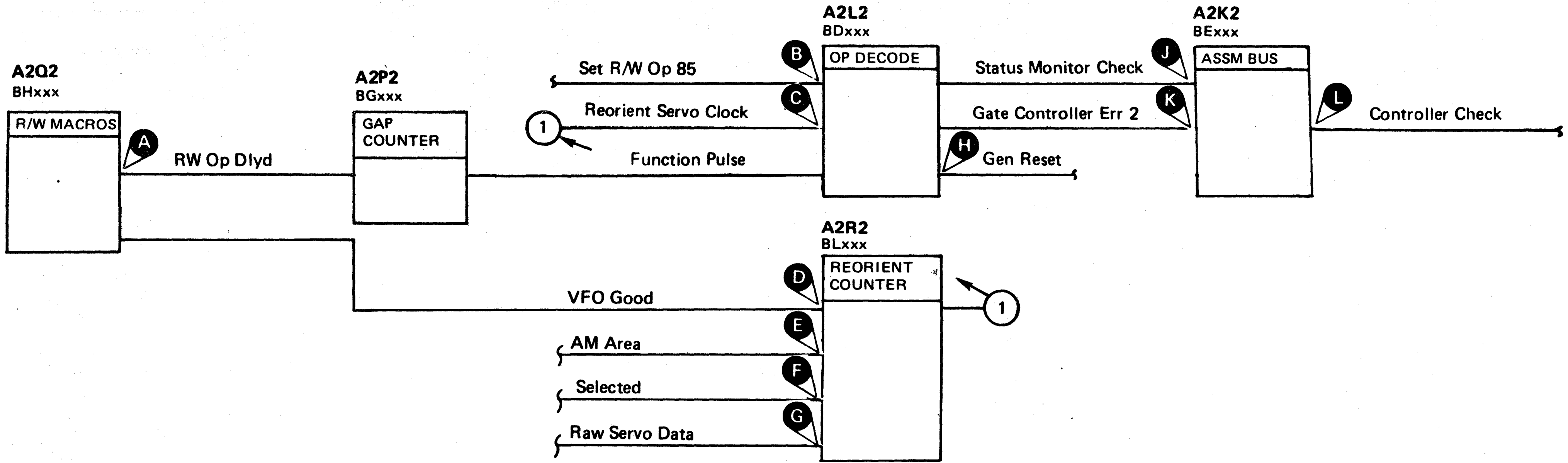
The test also forces Monitor Check.



3350	CE0510 Seq. 1 of 2	2358599 Part No.	441300 31 Mar 76	441303 30 Jul 76			

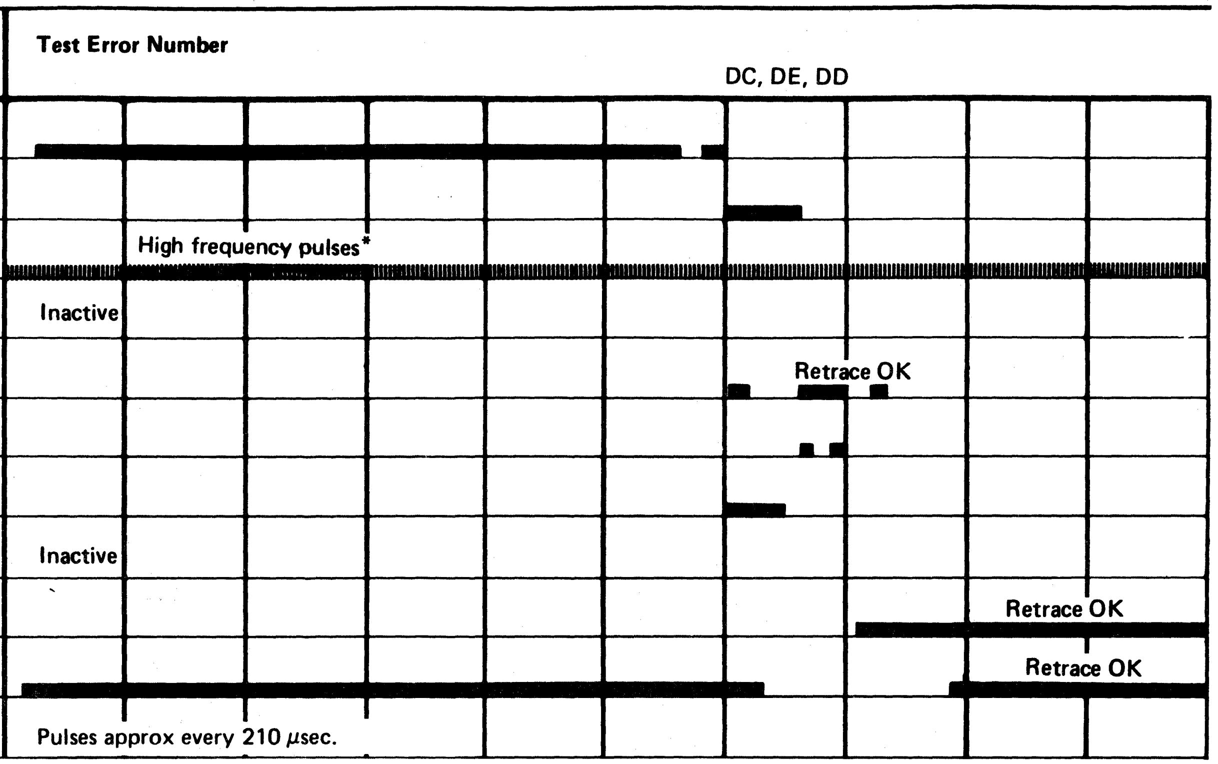
MONITOR CHECK CHECKER

See OPER 241 for theory.



Legend:
▭ Inactive
▬ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number DC, DE, DD
1	–Set R/W Op 85	BD150	A2L2 M08	B	
2	–Status Monitor Check	BE120	A2K2 P06	J	
3	+Reorient Servo Clock	BD160	A2L2 D05	C	High frequency pulses*
4	+RW Op Dld	BH100	A2Q2 B10	A	Inactive
5	–Gate Controller Error 2	BE120	A2K2 M03	K	Retrace OK
6	+Gen Reset	BD160	A2L2 B10	H	
7	–Controller Check	BE130	A2K2 M12	L	
8	–AM Area	BL120	A2R2 G08	E	Inactive
9	–Selected	BL140	A2R2 D06	F	Retrace OK
10	–VFO Good	BL120	A2R2 G13	D	Retrace OK
11	Raw Servo Data	BL140	A2R2 G10	G	Pulses approx every 210 µsec.



*See DATA 996 for a description of pulse duration and repetition rate.

CE0510 Seq. 2 of 2	2358599 Part No.	441300 31 Mar 76	441303 30 Jul 76			

MONITOR CHECK SYMPTOM CODE

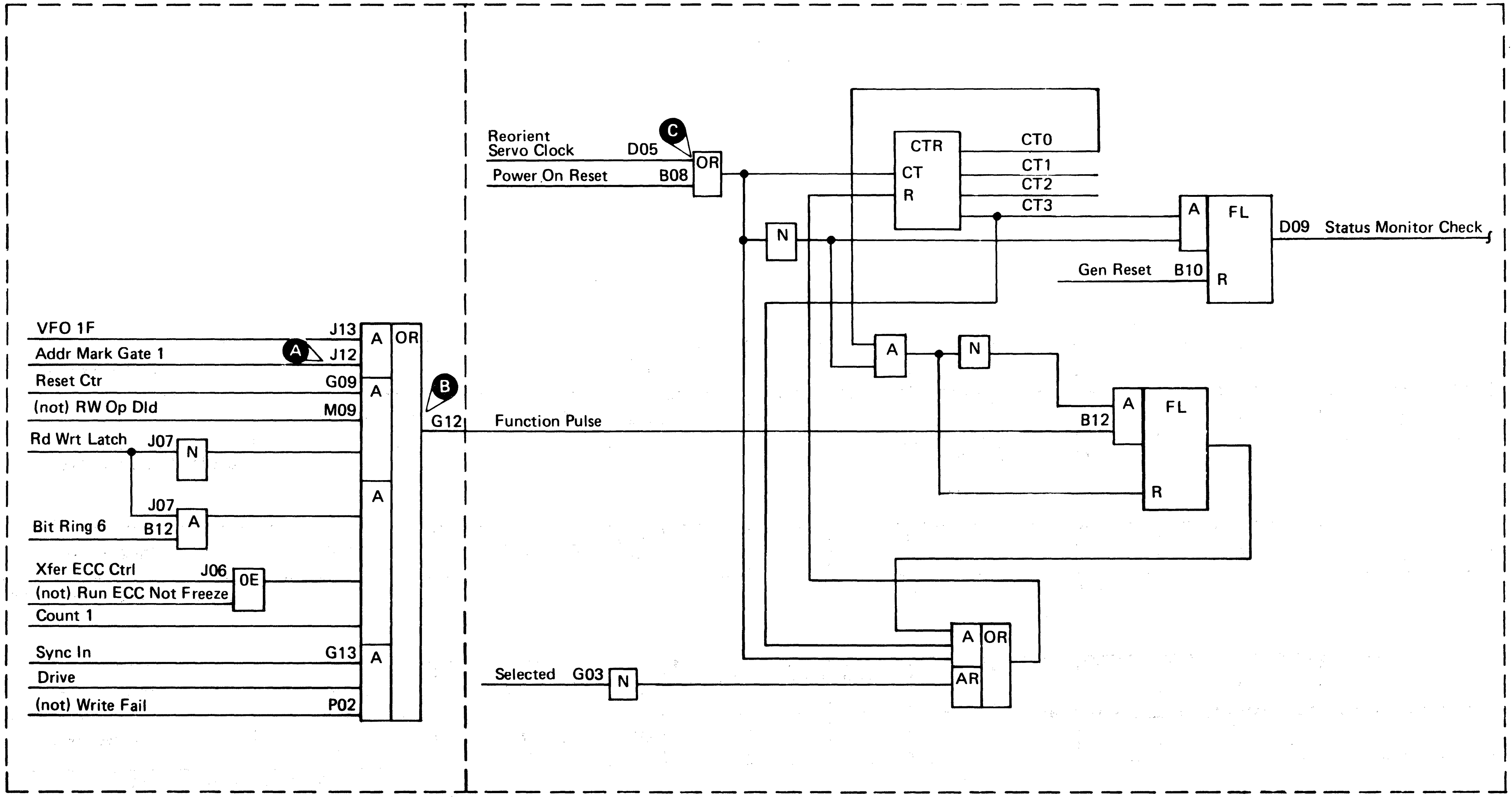
See the sequence charts on DATA 298 for referenced test points.

Status Monitor Check detects hang up conditions. The Monitor Check Counter is held reset when the controller is not selected. When the controller and a drive are selected and after a Set Read/Write operation has been issued, Reorient Servo Clock pulses are sent to the counter. The counter advances once on the leading edge of each pulse. If the counter counts to 3 without a Function Pulse having primed the counter reset, a Monitor Check is generated at the fall of the Reorient Servo Clock pulse. Function pulses that occur prior to count-3 time set a latch, which gates Reorient Servo Clock pulses to reset the counter as it steps to count 3 and before the Monitor Check latch can set. Since Reorient Servo Clock pulses occur at approximately 1.67 microsecond intervals and a count of 3 causes a Monitor Check, at least one Function Pulse is required every 6.5 microseconds (approximately).

Function Pulses indicate:

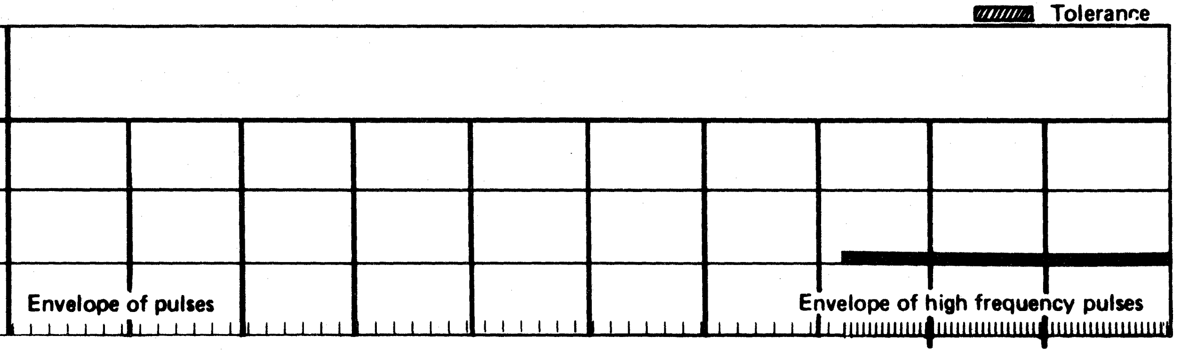
1. **That clock or data bits are being recognized during an Address Mark search.**
2. **That the Bit Ring is running after Read/Write was reset.**
3. **That the Bit Ring and Gap Counter are functioning during Read/Write operations when no Sync In pulses are being generated.**
4. **That Sync In pulses are being generated during data handling operations. (An I Write Sense failure blocks pulses and forces a Monitor Check.)**

A2P2 BGxxx Logic Diagram **A2L2 BDxxx Logic Diagram**



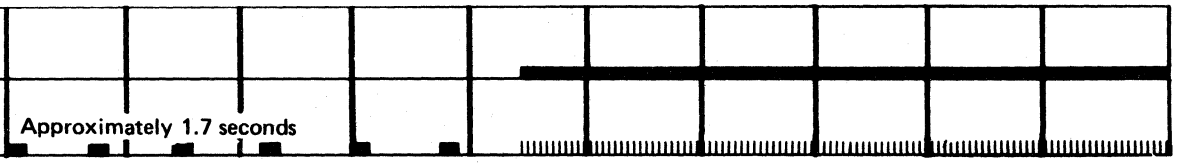
Legend:
- ▭ Inactive
- ▬ Active level
- ▨ Tolerance

Line Name	ALD	Test Point	
-MST RAS TP	BD100	A2L2 J11	
-Addr Mark Gate 1	BG160	A2P2 J12	Ⓐ
-Function Pulse	BG160	A2P2 G12	Ⓑ



Change horizontal display to: B Delayed by A.
Turn Delay-Time Multiplier to 8.3 on the dial.
Delayed Sweep to 2 μs/div.

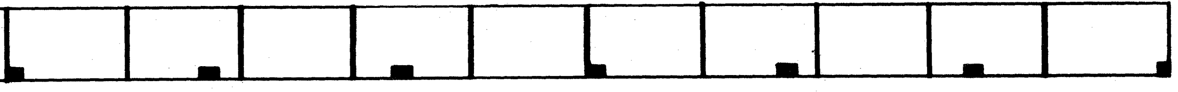
Line Name	ALD	Test Point	
-Addr Mark Gate 1	BG160	A2P2 J12	Ⓐ
-Function Pulse	BG160	A2P2 G12	Ⓑ



ALTERNATE PARAMETER 1

Alternate Bit Ring Time

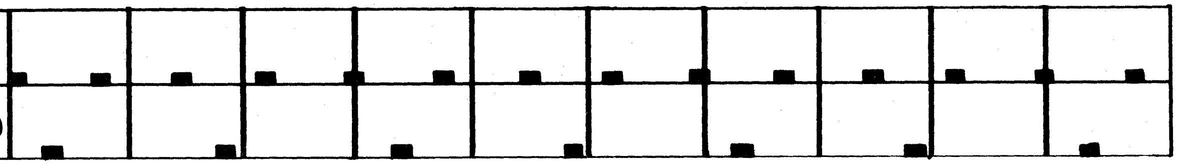
Line Name	ALD	Test Point	
-Function Pulse	BG160	A2P2 G12	Ⓑ



ALTERNATE PARAMETER 2

Reset Counter Time

Line Name	ALD	Test Point	
-Function Pulse	BG160	A2P2 G12	Ⓑ
+Reorient Servo Clock	BD160	A2L2 D05	Ⓒ



3350	CE0525 Seq. 2 of 2	2358600 Part No.	441300 31 Mar 76	441303 30 Jul 76			

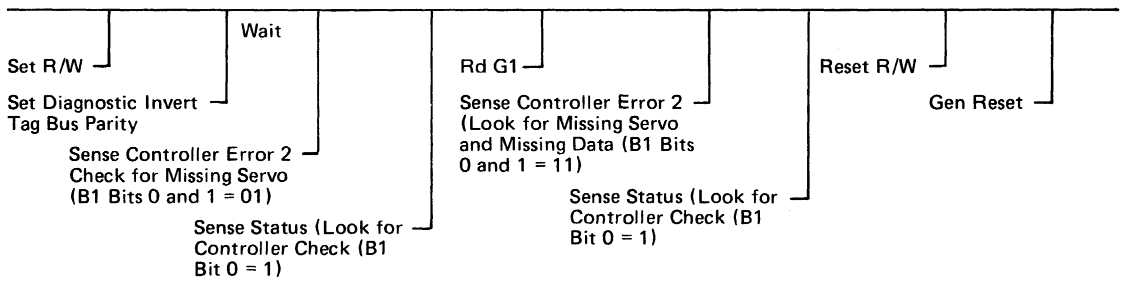
NO CONTROLLER CHECK FOR MISSING SERVO PULSES OR DATA BITS

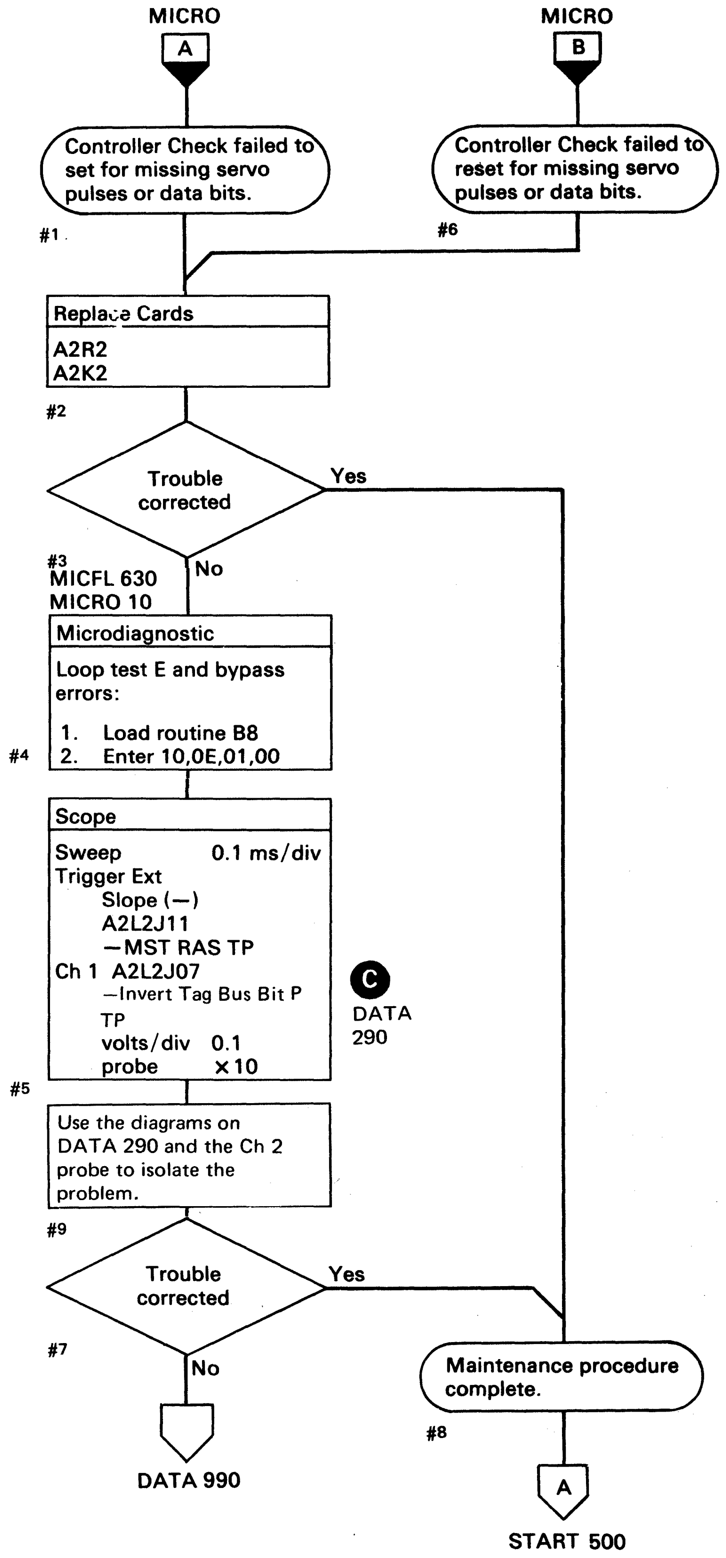
ERROR DESCRIPTION

Missing servo pulses and data bits cause a Controller Check. This test verifies that the Controller Check circuits operate correctly for these errors.

MICRODIAGNOSTIC DESCRIPTION

Routine B8, test E tests that the Missing Servo and Missing Data errors can be forced and reset and that a Controller Check can be generated. A Set Read/Write activates the Servo Mode circuitry, Diagnostic Invert Tag Bus Parity blocks VFO pulses, and a Missing Servo Error occurs. A Read operation is initiated and when the VFO switches from Servo (pulse) mode to Data (pulse) mode, Missing Data is detected.





CE0535 Seq. 1 of 2	2358601 Part No.	441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77	441310 27 Jun 80	

MONITOR CHECK SYMPTOM CODE

ERROR DESCRIPTION

Monitor Check tests the Bit Ring and Gap Counter operation and ensures that an Address Mark Search operation is progressing satisfactorily. Failures in these areas result in a machine hang condition.

Microdiagnostic routine AF, test 0C tests the operation of the Monitor Check circuits during Address Mark Search. Looping this test provides a method for scoping.

The two sets of parameters provided for routine B4 cause scoping loops for:

- Function Pulses during Set Read/Write.
- After Set Read/Write.

If scoping is required, use the diagram on DATA 296 and the sequence chart on DATA 230. If the sequence relationships are not as indicated, use the ALDs to resolve the problem.

MICRODIAGNOSTIC DESCRIPTION

Routine AF, test C formats a track with a Home Address only and erases the G3 field previously written. The test then orients on the Home Address and attempts to perform an Address Mark Search operation. No AM Found is the expected result.

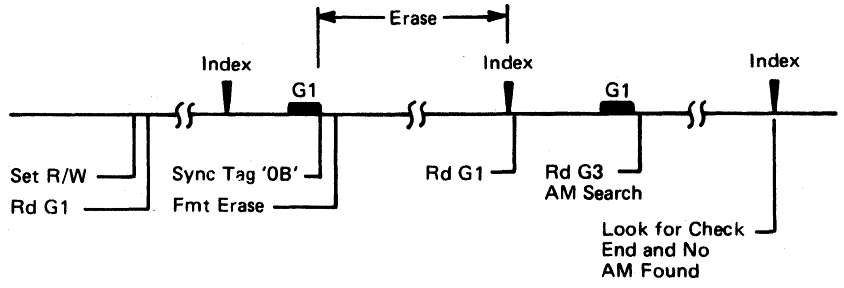
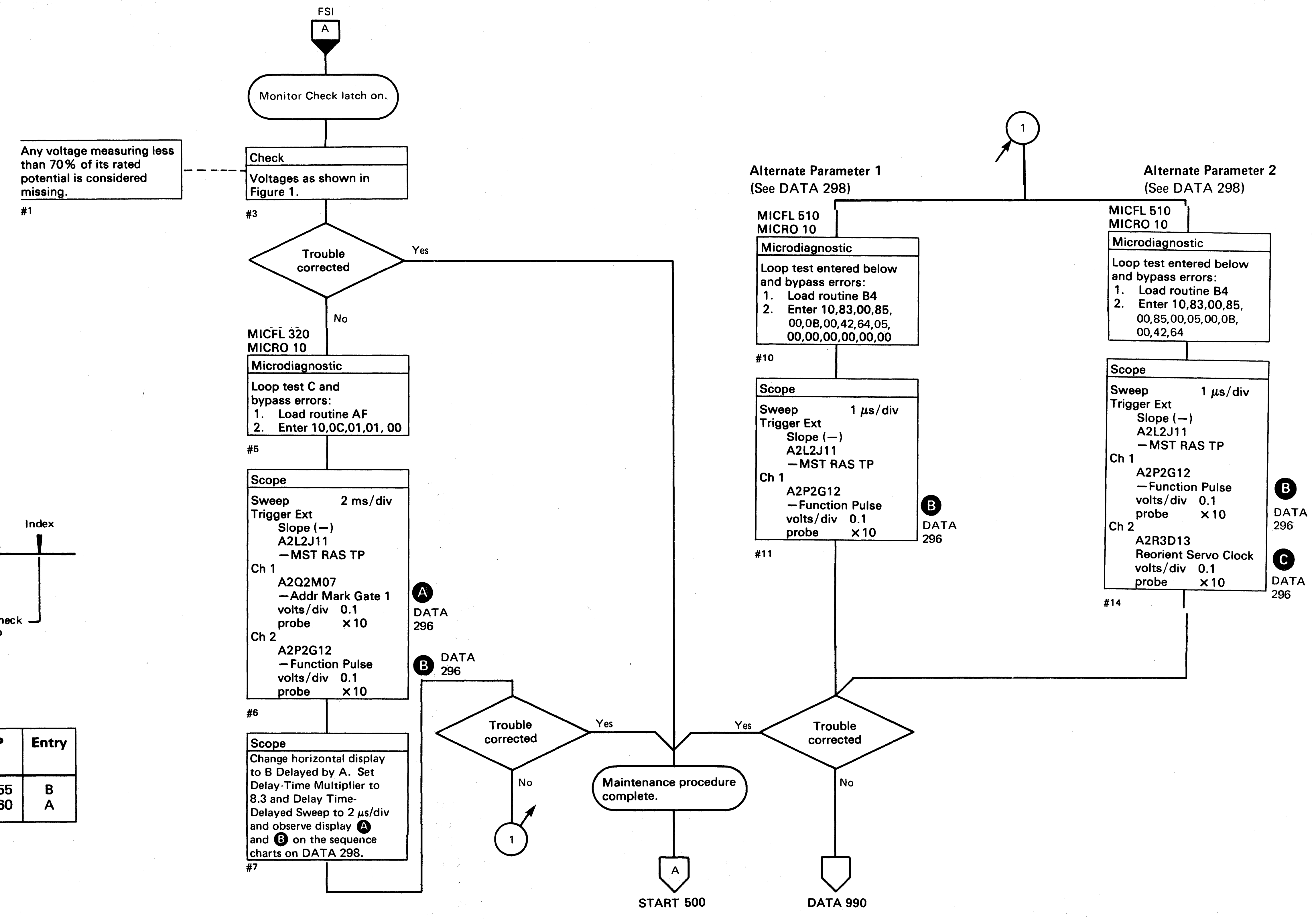


Figure 1. Controller Voltages

Voltage	Test Point	Tolerance	Maximum AC Ripple	MAP	Entry
−4 V	A2D2B06	−3.84 to −4.16 V	0.04 V p-p	PWR 55	B
+6 V	A2T2G11	+5.76 to +6.24 V	0.08 V p-p	PWR 60	A



CE0535 Seq. 2 of 2	2358601 Part No.	441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77	441310 27 Jun 80	

DEFECT SKIPPING REORIENTATION ERROR

ERROR DESCRIPTION

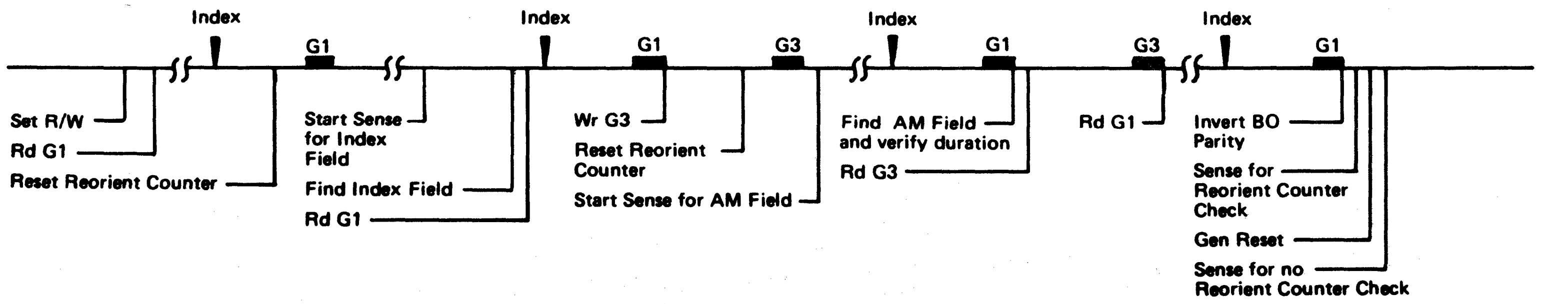
To format a record that contains a defect, the Count field is processed before it can be determined that the defect will fall within the current record. The Count field must be rewritten with the correct flag bytes and skip defect information. To accomplish this, the disk must be reoriented to the gap preceding the Count field. If an Error Alert occurs during the reorientation, a Defect Skipping Reorientation Check is indicated.

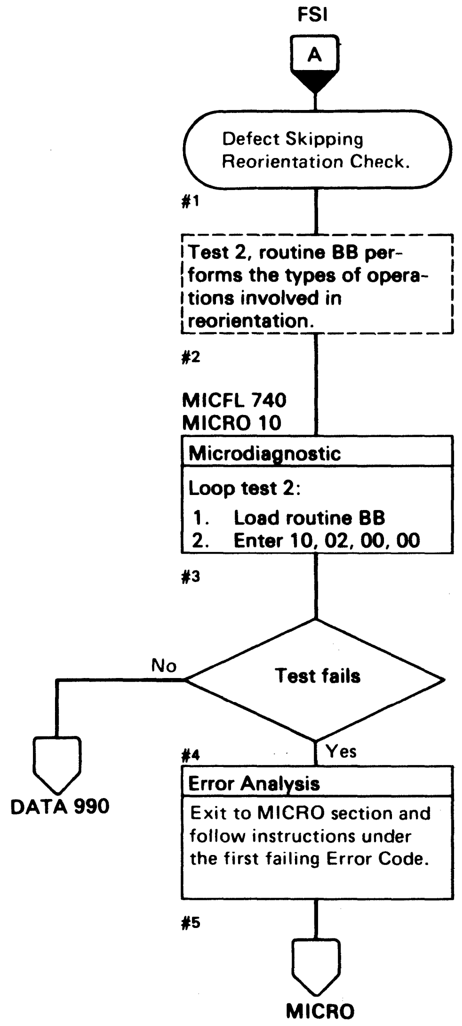
MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 2 checks the Reorient Counter operation. The test performs a Read G1 operation to start the Reorient Counter in Index Mode and then checks that the Index Field pulse is generated at the proper time. The G1 field is read again to ensure the proper relationship.

A Write G3 operation is then performed to start the counter in AM (Address Mark) mode and then checks that the AM field pulse occurs at the proper time with respect to Index and has the proper duration. The G3 field is read again to ensure the proper relationship.

Another Read G1 operation is initiated and Invert Bus Out Parity is used to force a Reorient Counter Check. Proper operation of the Reorient Counter Check and Controller Check is verified.





CE0545 Seq. 1 of 2	2358602 Part No.	441300 31 Mar 76	441303 30 Jul 76			

REORIENT COUNTER CHECK

ERROR DESCRIPTION

During the retry of data operations, a Set Sector command is used to establish an approximate orientation point and to allow time to reconnect to the channel. Orientation to a point where data transfer can be resumed must be more precise. The Reorient Counter is used to time the retry precisely to the gap preceding the record to be retried. This is done by counting byte times around the entire disk. When the proper number of byte times has passed, Index (IX) Field or Address Mark (AM) Field is indicated, depending on the type of operation.

The Reorient Counter generates parity for self-checking. This test forces parity errors and verifies that they are detected, and then tests that the error can be reset.

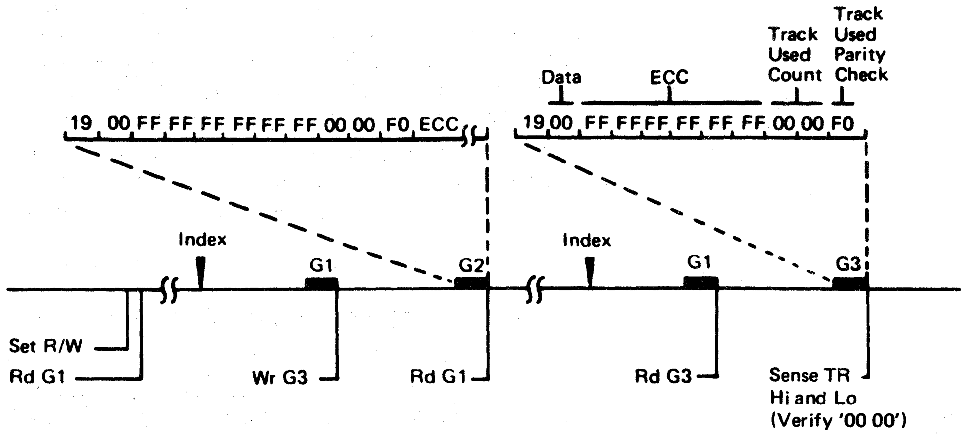
MICRODIAGNOSTIC DESCRIPTION

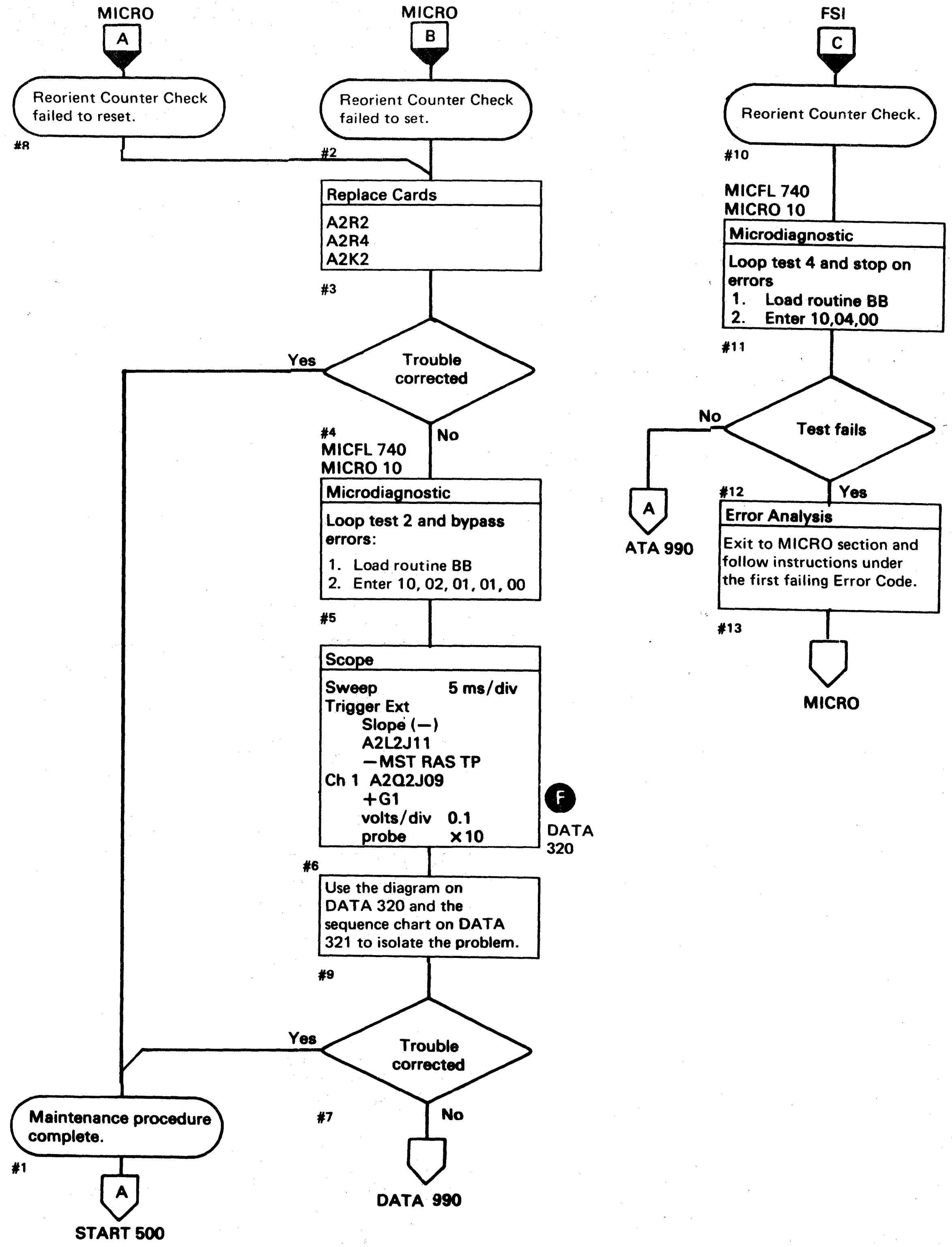
See DATA 310 for a description of routine BB, test 2.

Routine BB, test 4 reads a G2 field and then writes G3 field of 10 bytes. The G3 field is read using a byte count of one. The field produced has the following components:

- 1 Data byte
- 6 ECC bytes
- 3 Track Used Count Bytes (2 count + Parity Check)

The Track Used Counter bytes are loaded into the counter as they are read. Sense Track Used High and Sense Track Used Low operations are performed and values of '0000' are expected.





ADDRESS MARK (AM) FIELD LATE TIMING

ERROR DESCRIPTION

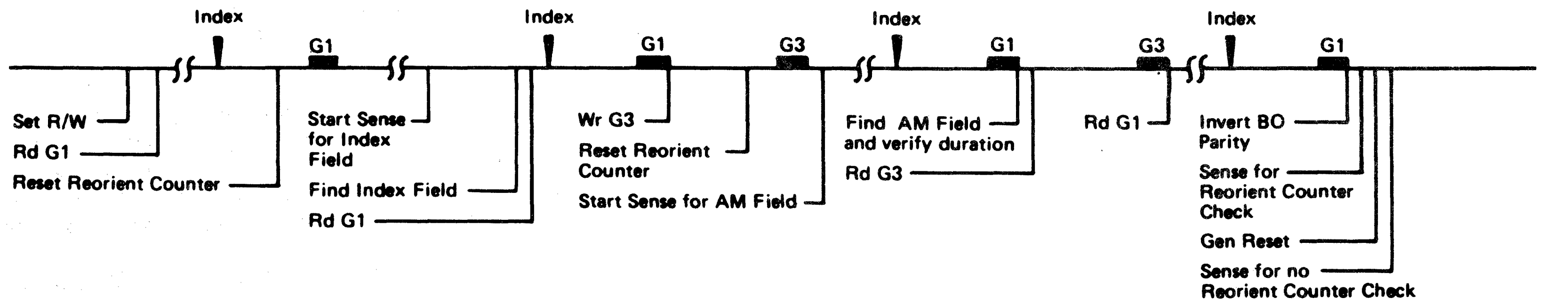
During the retry of data operations, a Set Sector command is used to establish an approximate orientation point and to allow time to reconnect to the channel. Orientation to a point where data transfer can be resumed must be more precise. The Reorient Counter is used to time the retry precisely to the gap preceding the record to be retried. This is done by counting byte times around the entire disk. When the proper number of byte times has passed, Index (IX) Field or Address Mark (AM) Field is indicated depending on the type of operation.

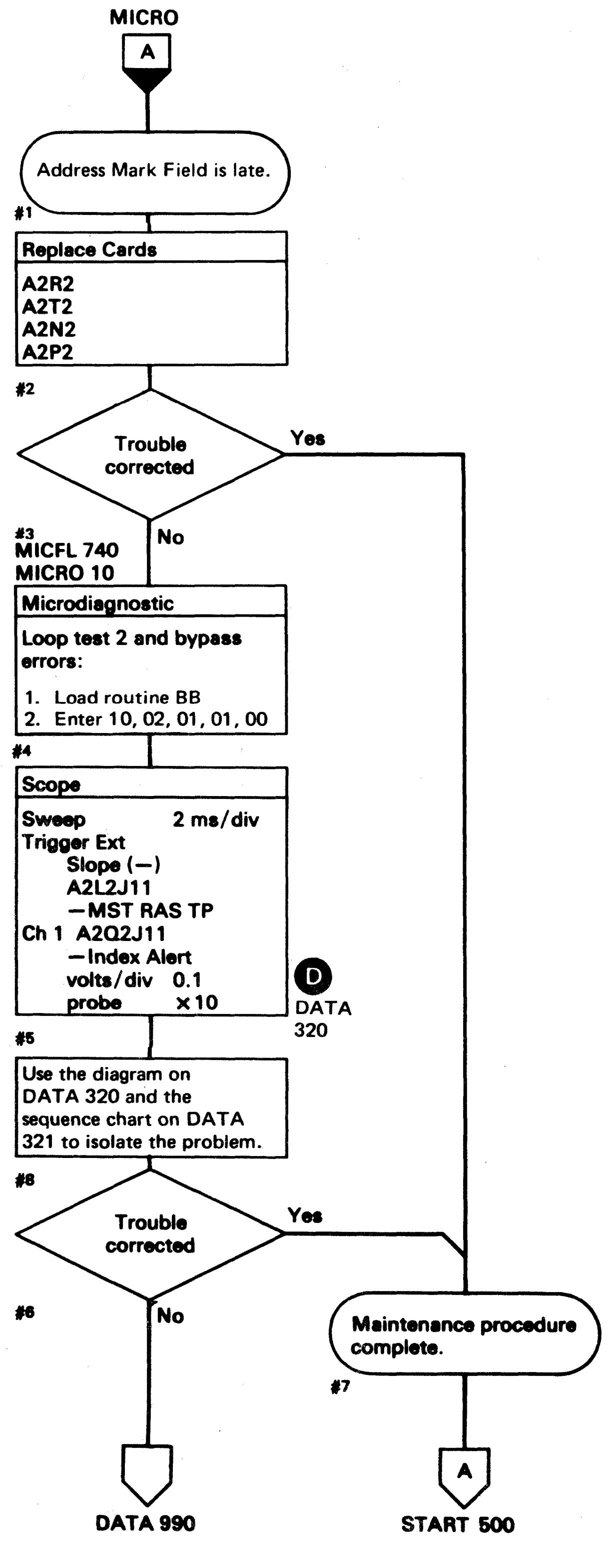
This test checks the timing of the Address Mark field.

MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 2 checks the Reorient Counter operation. The test performs a Read G1 operation to start the Reorient Counter in Index mode and then checks that the Index Field pulse is generated at the proper time. The G1 field is read again to ensure the proper relationship.

A Write G3 operation is performed to start the counter in AM (Address Mark) mode. A Write G3 checks that the AM Field pulse has the correct duration and occurs at the proper time with respect to Index. The G3 field is read again to ensure the proper relationship. Another Read G1 operation is initiated and Invert Bus Out Parity is used to force a Reorient Counter Check. Proper operation of the Reorient Counter Check and Controller Check is verified.





CE0555 Seq. 1 of 2	2358603 Part No.	441300 31 Mar 76	441303 30 Jul 76			

ADDRESS MARK (AM) FIELD DURATION

ERROR DESCRIPTION

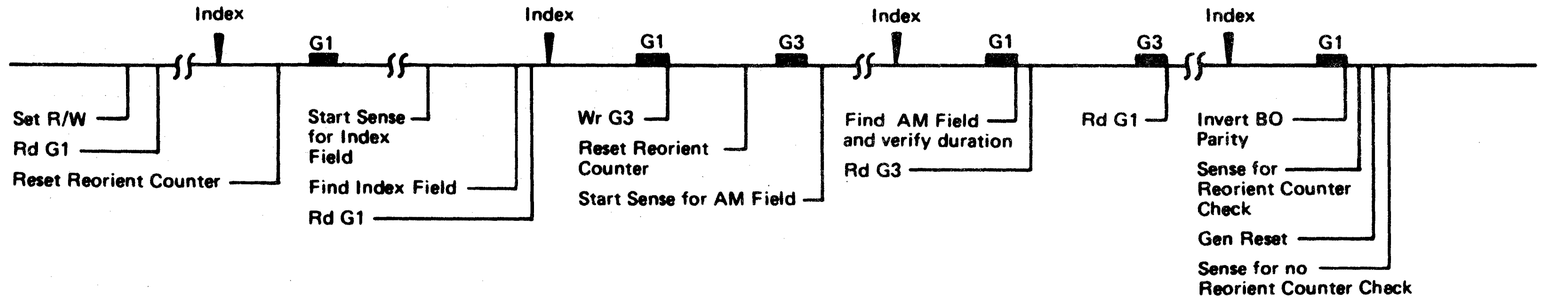
During the retry of data operations, a Set Sector command is used to establish an approximate orientation point and to allow time to reconnect to the channel. Orientation to a point where data transfer can be resumed must be more precise. The Reorient Counter is used to time the retry precisely to the gap preceding the record to be retried. This is done by counting byte times around the entire disk. When the proper number of byte times has passed, Index (IX) Field or Address Mark (AM) Field is indicated depending on the type of operation.

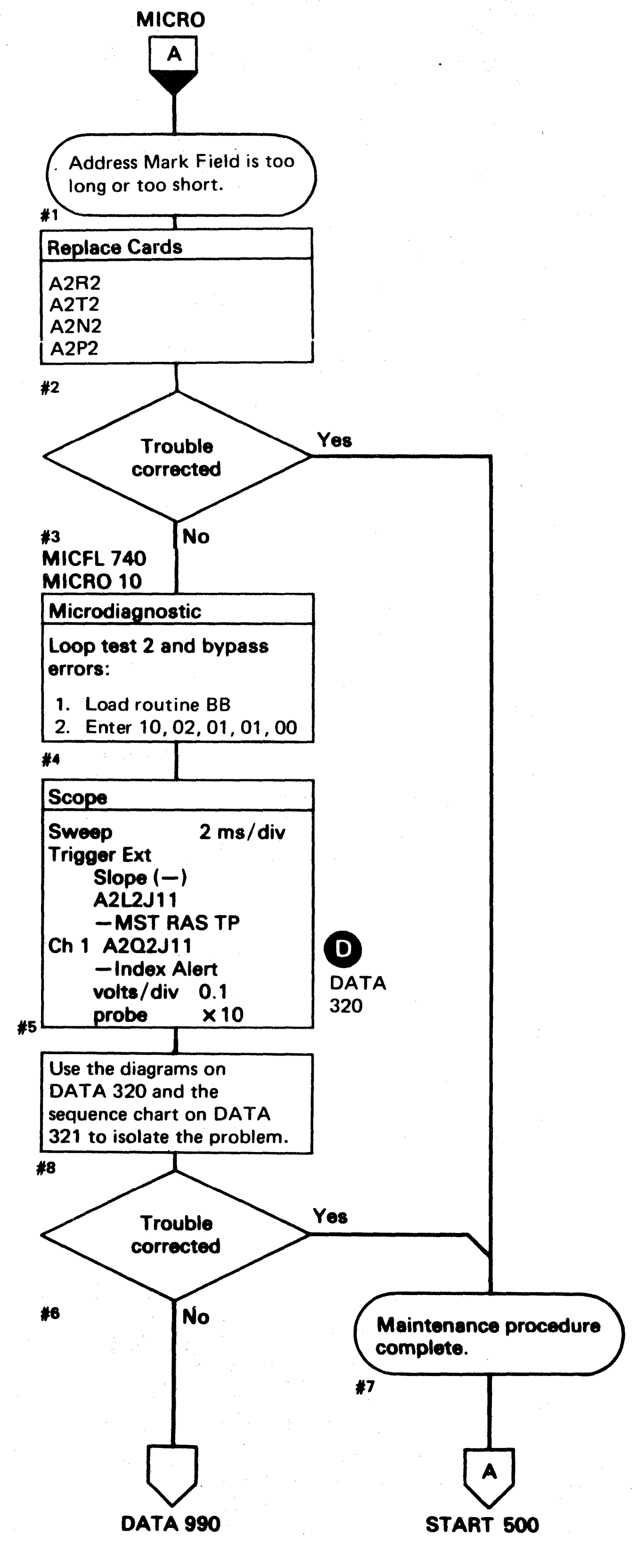
This test checks the duration of the Address Mark field.

MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 2 checks the Reorient Counter operation. The test performs a Read G1 operation to start the Reorient Counter in Index mode and then checks that the Index Field pulse is generated at the proper time. The G1 field is read again to ensure the proper relationship.

A Write G3 operation is performed to start the counter in AM (Address Mark) mode. A Write G3 checks that the AM Field pulse has the correct duration and occurs at the proper time with respect to Index. The G3 field is read again to ensure the proper relationship. Another Read G1 operation is initiated and Invert Bus Out Parity is used to force a Reorient Counter Check. Proper operation of the Reorient Counter Check and Controller Check is verified.





INDEX FIELD EARLY OR LATE

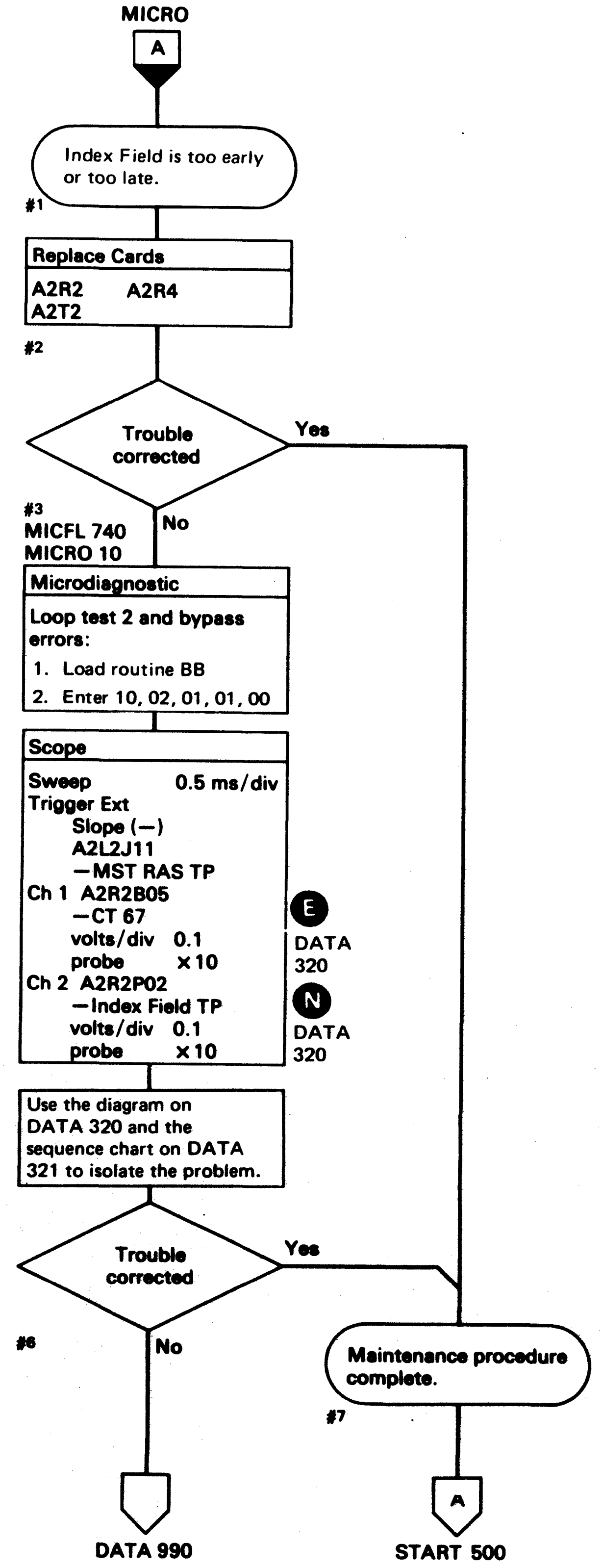
ERROR DESCRIPTION

During the retry of data operations, a Set Sector command is used to establish an approximate orientation point and to allow time to reconnect to the channel. Orientation to a point where data transfer can be resumed must be more precise. The Reorient Counter is used to time the retry precisely to the gap preceding the record to be retried. This is done by counting byte times around the entire disk. When the proper number of byte times has passed, Index (IX) Field or Address Mark (AM) Field is indicated depending on the type of operation.

This test checks the counting speed of the Reorient Counter.

MICRODIAGNOSTIC DESCRIPTION

See DATA 320 for a description of routine BB, test 2.



CE0565 Seq. 1 of 2	2358604 Part No.	441300 31 Mar 76	441303 30 Jul 76			

NO INDEX FIELD OR ADDRESS MARK (AM) FIELD

ERROR DESCRIPTION

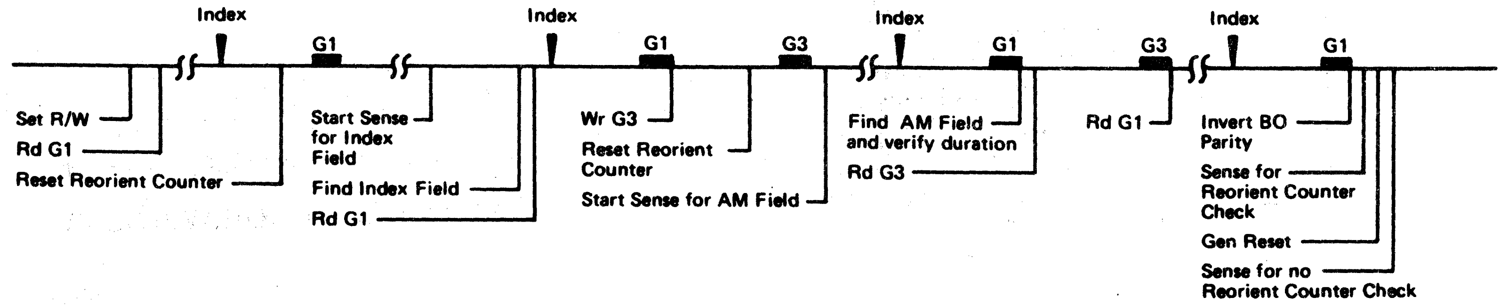
During the retry of data operations, a Set Sector command is used to establish an approximate orientation point and to allow time to reconnect to the channel. Orientation to a point where data transfer can be resumed must be more precise. The Reorient Counter is used to time the retry precisely to the gap preceding the record to be retried. This is done by counting byte times around the entire disk. When the proper number of byte times has passed, Index (IX) Field or Address Mark (AM) Field is indicated depending on the type of operation.

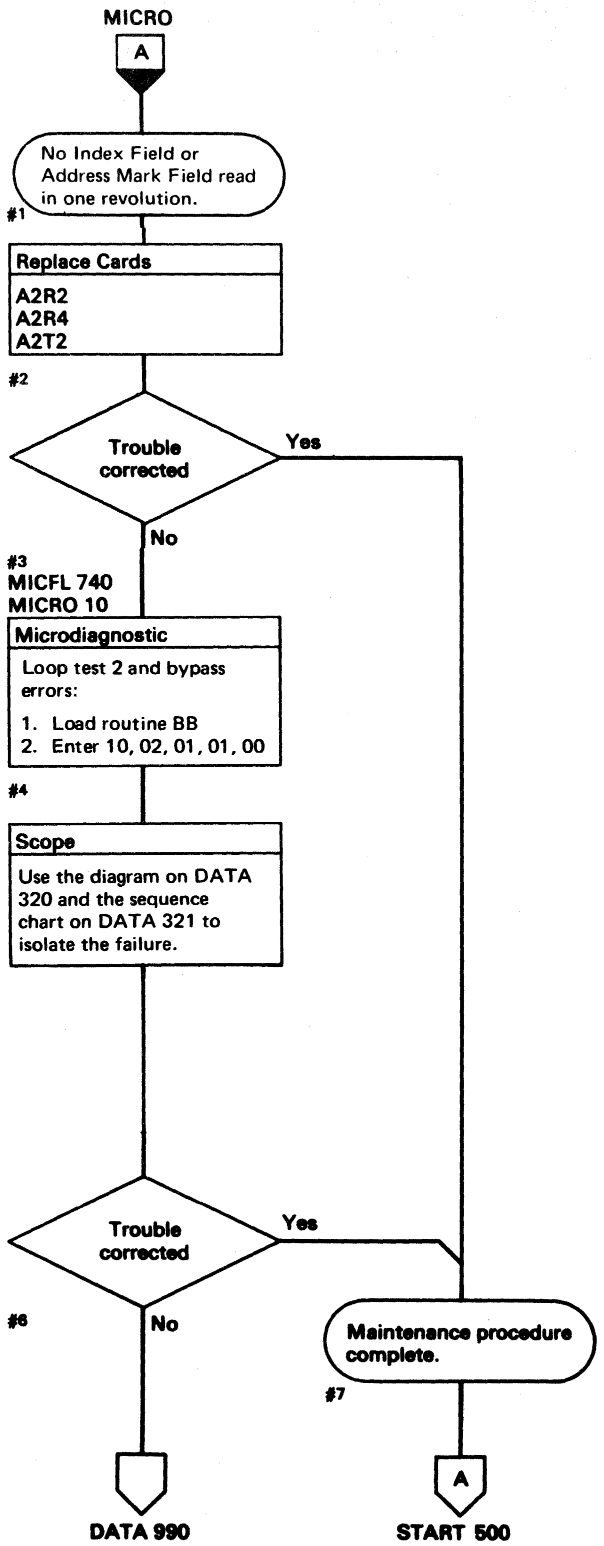
This test checks the ability of the Reorient Counter to count and generate Index Field and Address Mark Field lines.

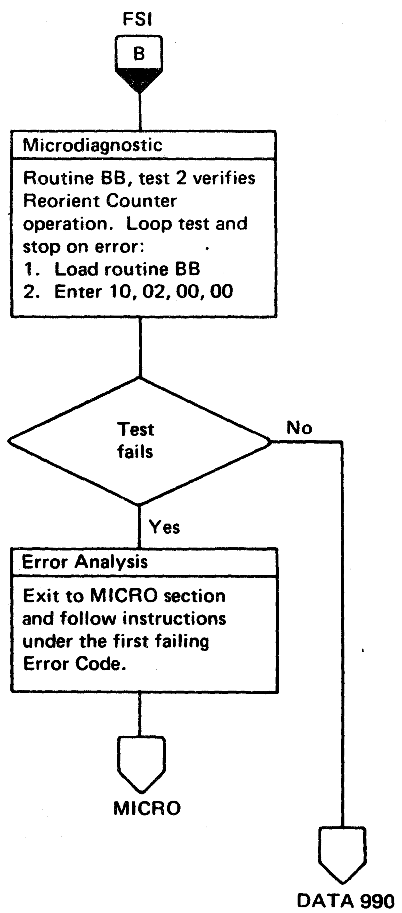
MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 2 checks the Reorient Counter operation. The test performs a Read G1 operation to start the Reorient Counter in Index mode and then checks that the Index Field pulse is generated at the proper time. The G1 field is read again to ensure the proper relationship.

A Write G3 operation is performed to start the counter in AM (Address Mark) mode. A Write G3 checks that the AM Field pulse has the correct duration and occurs at the proper time with respect to Index. The G3 field is read again to ensure the proper relationship. Another Read G1 operation is initiated and Invert Bus Out Parity is used to force a Reorient Counter Check. Proper operation of the Reorient Counter Check and Controller Check is verified.







TRACK USED COUNTER ERROR

ERROR DESCRIPTION

The Track Used Counter accumulates the number of 3330-1 Compatibility Mode bytes that has been used on the track. This byte count is written on the track following each count field.

During Search/Read operations, the Track Used count is read from the Count field and used to prime the Track Used Counter.

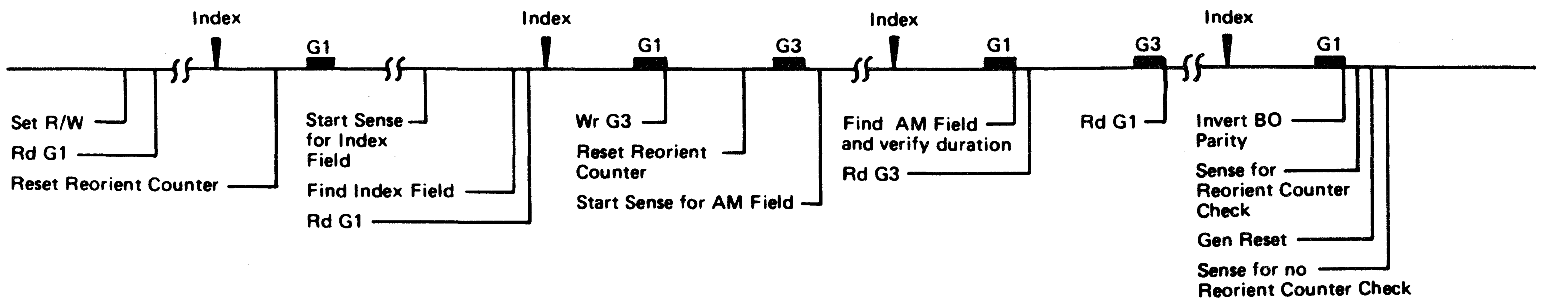
When the Track Used Counter reaches its limit, the TR Index line indicates that the 3330 track capacity has been exceeded. If the limit is reached while in Write mode, a Check End with Track Overrun is posted to the storage control.

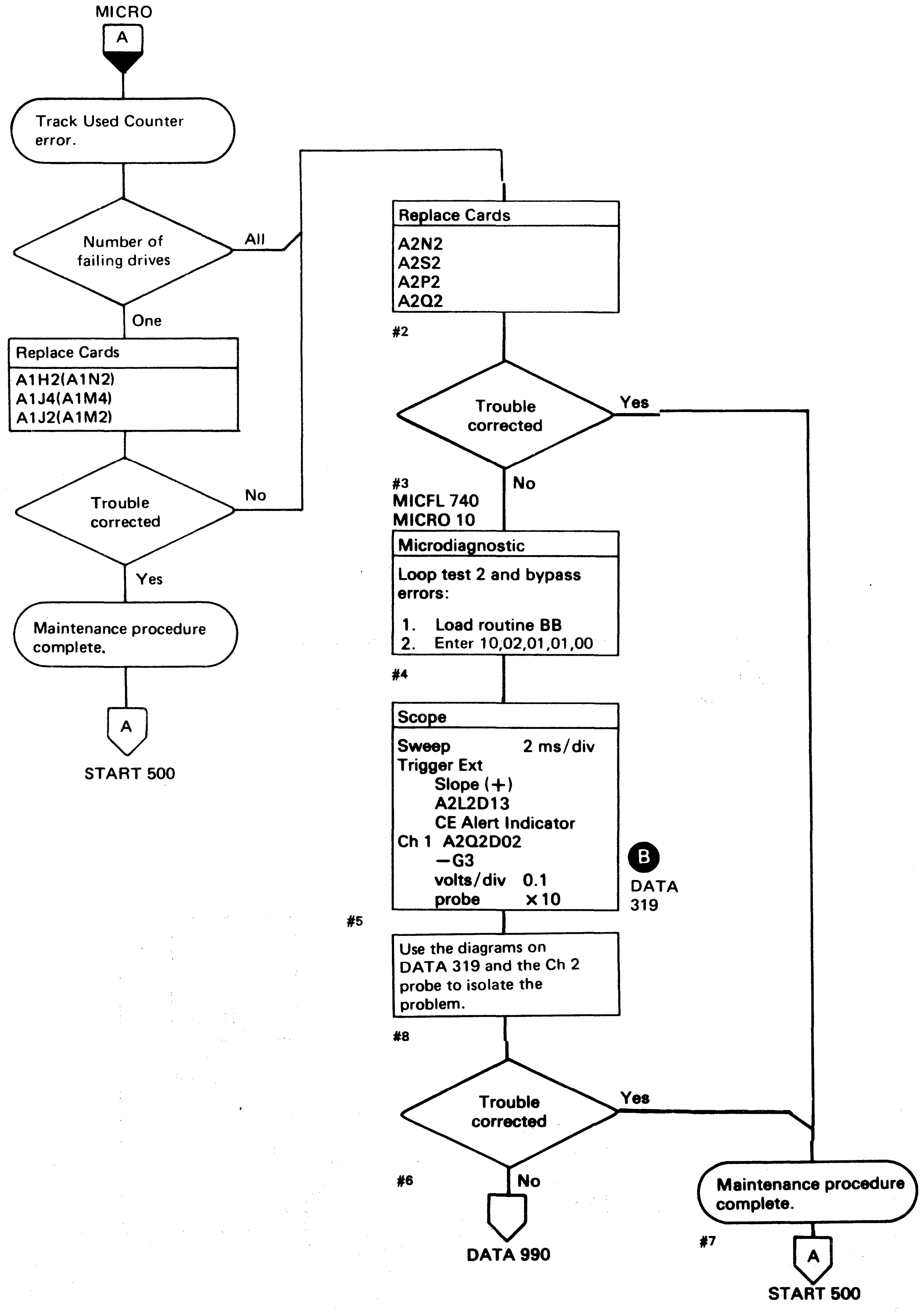
This test verifies that the correct value of the Track Used Counter was written on the disk.

MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 2 checks the Reorient Counter operation. The test performs a Read G1 operation to start the Reorient Counter in Index mode and then checks that the Index Field pulse is generated at the proper time. The G1 field is read again to ensure the proper relationship.

A Write G3 operation is then performed to start the counter in AM (Address Mark) mode and then checks that the AM Field pulse occurs at the proper time with respect to Index and has the proper duration. The G3 field is read again to ensure the proper relationship. Another Read G1 operation is initiated and Invert Bus Out Parity is used to force a Reorient Counter Check. Proper operation of the Reorient Counter Check and Controller Check is verified.

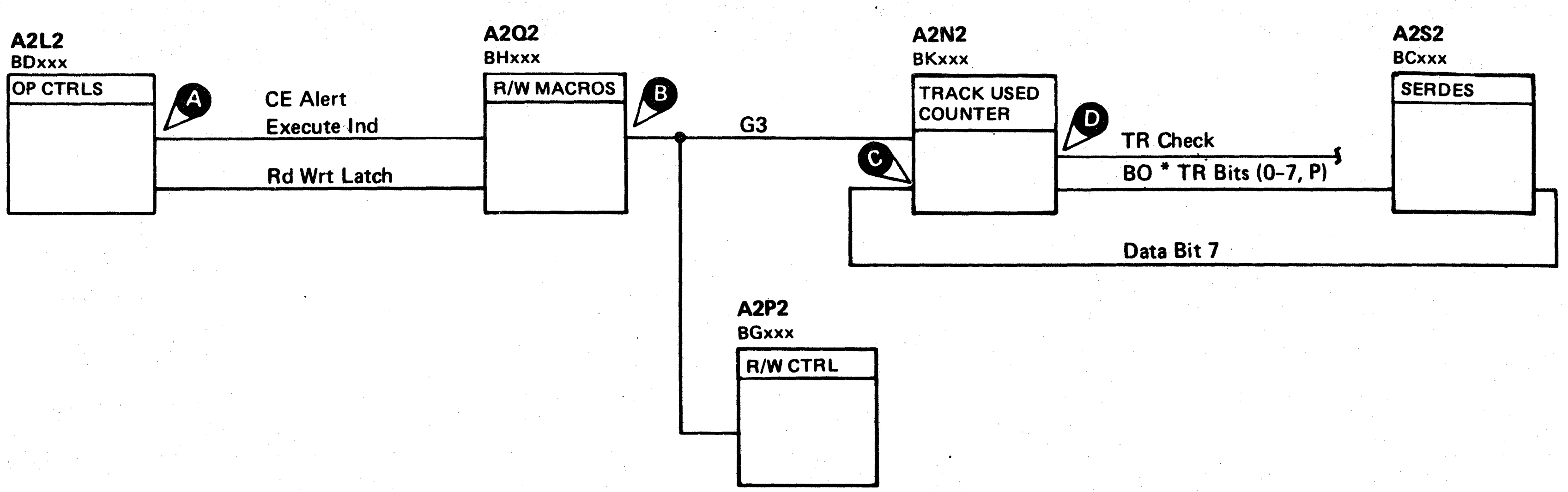




3350	CE0575 Seq. 1 of 2	2358605 Part No.	**441300** **31 Mar 76**	441303 30 Jul 76			

TRACK USED COUNTER ERROR

See OPER 42 and 52 for theory.



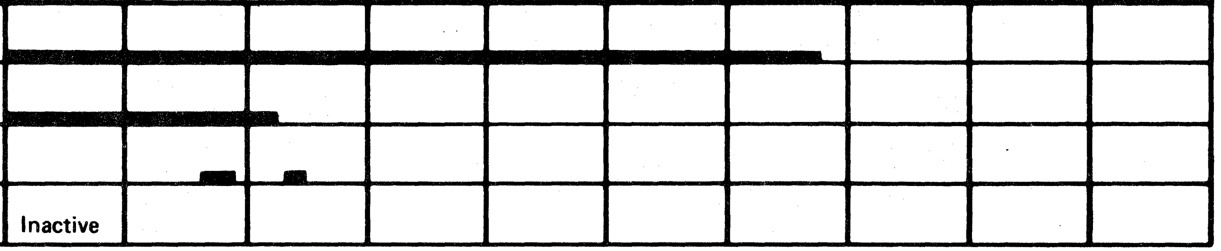
TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 2ms/div — Ch 1 A2Q2D02
Mode — -G3
Trigger — Volts/div 0.1
Slope (+) — Probe X10
A2L2D13 — Ch 2 (see chart)
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 2 ms/div
Slope (–)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		
1	+CE Alert Execute Ind	BD210	A2L2 D13	A	
2	-G3	BH110	A2Q2 D02	B	
3	-Data Bit 7	BK150	A2N2 B12	C	
4	+TR Check	BK140	A2N2 B10	D	Inactive

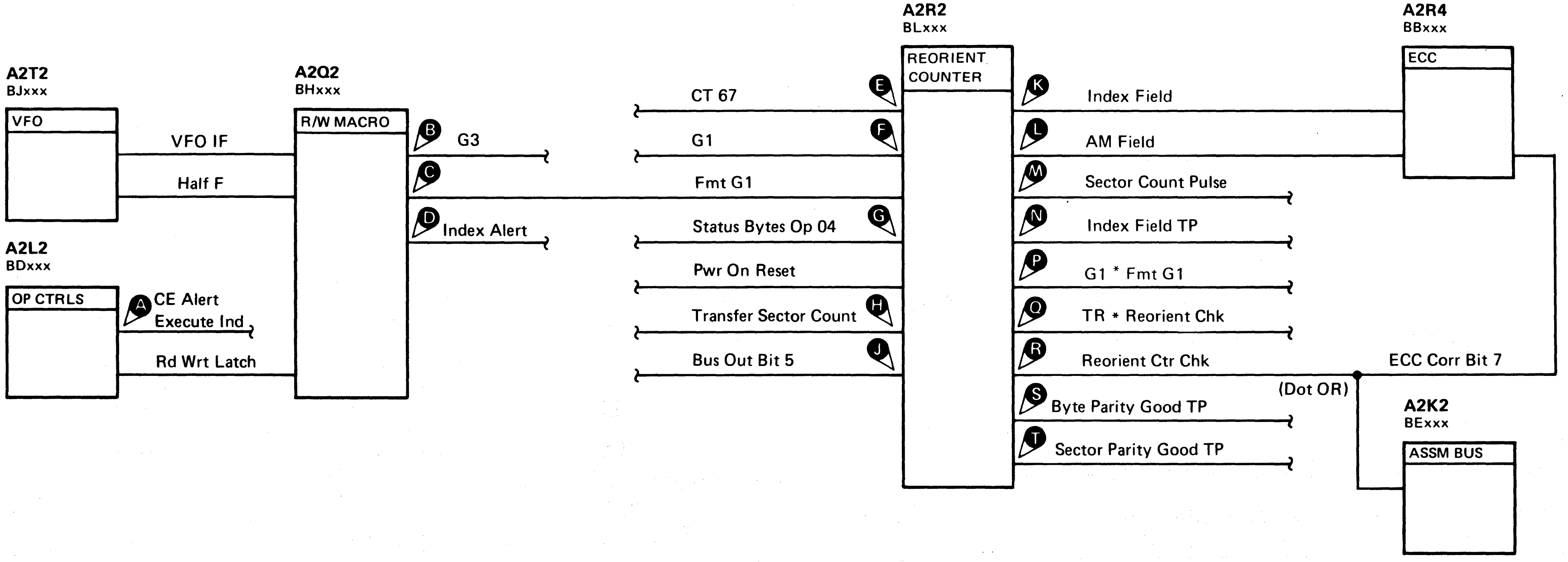


CE0575 Seq. 2 of 2	2358605 Part No.	441300 31 Mar 76	441303 30 Jul 76			

BB TEST 2 DIAGRAM

See the sequence chart on DATA 321 for referenced test points.

See OPER 240 for theory.



3350	CE0585 Seq. 1 of 2	2358606 Part No.	441300 31 Mar 76	441303 30 Jul 76			

BB TEST 2 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine BB, test 2
1. Load BB
2. Enter 10, 02, 00, 00

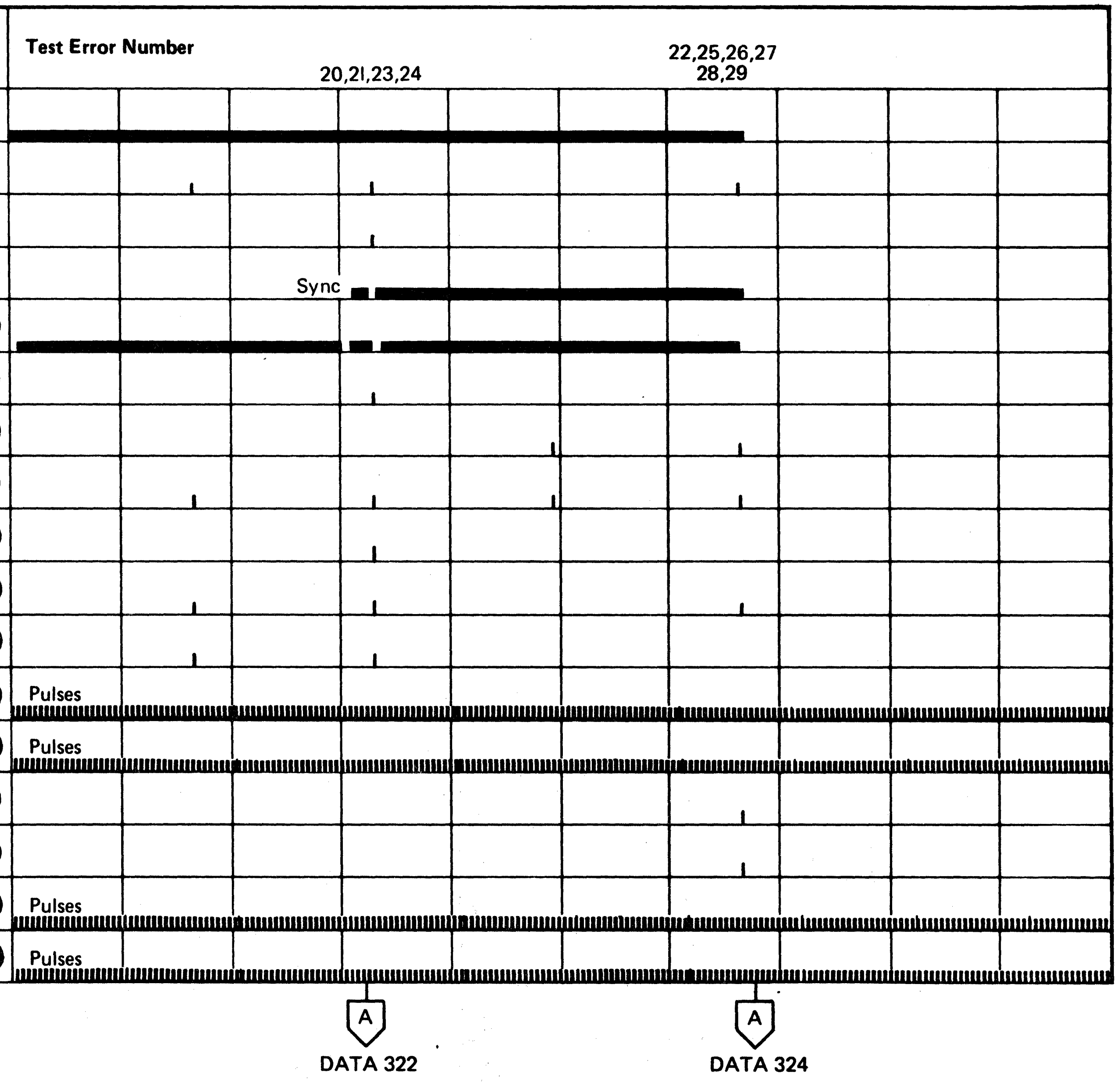
Scope Setup

Sweep 10 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	A
2	+G1	BH120	A2Q2 J09	F
3	−G3	BH110	A2Q2 D02	B
4	−Status Bytes Op 04	BL130	A2R2 J05	G
5	−Bus Out Bit 5	BL130	A2R2 J11	J
6	+Index Field	BL130	A2R2 J04	K
7	+AM Field	BL130	A2R2 G02	L
8	−Index Alert	BH170	A2Q2 J11	D
9	−Index Field TP	BL130	A2R2 D02	N
10	−G1*Fmt G1	BC130	A2R2 B04	P
11	−Transfer Sector Count	BL120	A2R2 J07	H
12	+Sector Count Pulse	BL120	A2R2 D09	M
13	−CT 67	BL120	A2R2 B05	E
14	+Reorient Ctr Chk	BL120	A2R2 G04	R
15	−TR*Reorient Chk	BL120	A2R2 J10	Q
16	+Byte Parity Good TP	BL120	A2R2 B11	S
17	+Sector Parity Good TP	BL120	A2R2 D11	T



Line keys reference the diagram on DATA 320.

(For expanded sequence chart)

BB TEST 2 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

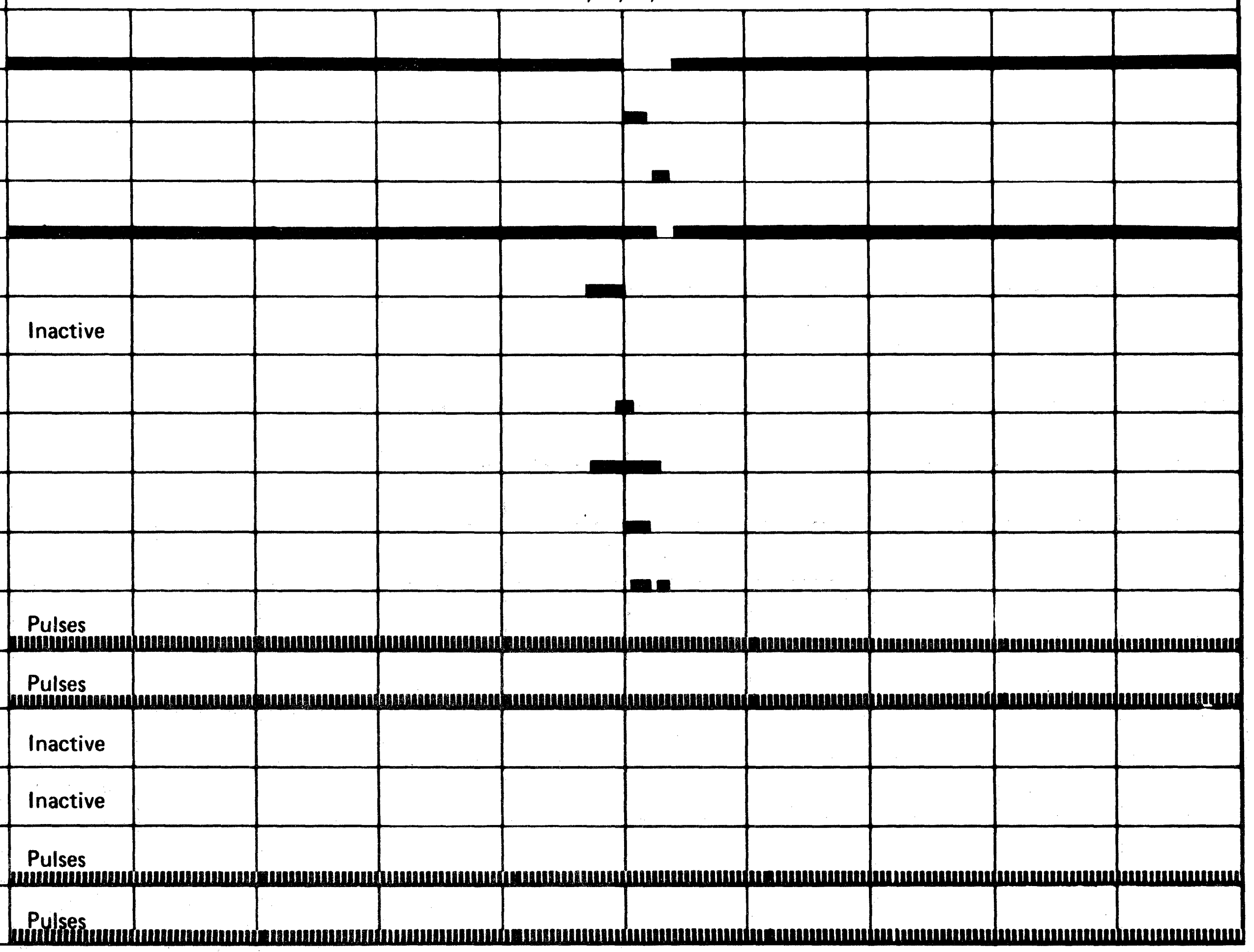
Sweep 10 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 10 ms/div
Slope (–)
Delay Time-Delayed Sweep – 0.5 ms/div
Delay-Time Multiplier – 2.8
Source – Int Ch 1

Ch 1 A2R2J05
–Status Bytes Op 04
Volts/div 0.1
Probe x10
Ch 2 (see chart)

DATA 321
Ⓐ

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 23,24,21,20
1	–Status Bytes Op 04	BL130	A2R2 J05	G	
2	+G1	BH120	A2Q2 J09	F	
3	–G3	BH110	A2Q2 D02	B	
4	–Bus Out Bit 5	BL130	A2R2 J11	J	
5	+Index Field	BL130	A2R2 J04	K	
6	+AM Field	BL130	A2R2 G02	L	Inactive
7	–Index Alert	BH170	A2Q2 J11	D	
8	–Index Field TP	BL130	A2R2 D02	N	
9	–G1*Fmt G1	BL130	A2R2 B04	P	
10	–Transfer Sector Count	BL120	A2R2 J07	H	
11	+Sector Count Pulse	BL120	A2R2 D09	M	Pulses
12	–CT 67	BL120	A2R2 B05	E	Pulses
13	+Reorient Ctr Chk	BL120	A2R2 G04	R	Inactive
14	–TR*Reorient Chk	BL120	A2R2 J10	Q	Inactive
15	+Byte Parity Good TP	BL120	A2R2 B11	S	Pulses
16	+Sector Parity Good TP	BL120	A2R2 D11	T	Pulses



Line keys reference the diagram on DATA 320.

BB TEST 2 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 10 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 10 ms/div
Slope (–)
Delay Time-Delayed Sweep – 50 µs/div
Delay-Time Multiplier – 6.0
Source – Int Ch 1

Ch 1 A2Q2J11
–Index Alert
Volts/div 0.1
Probe x10
Ch 2 (see chart)

DATA 321

A

Legend:
□ Inactive
■ Active level
▨ Tolerance

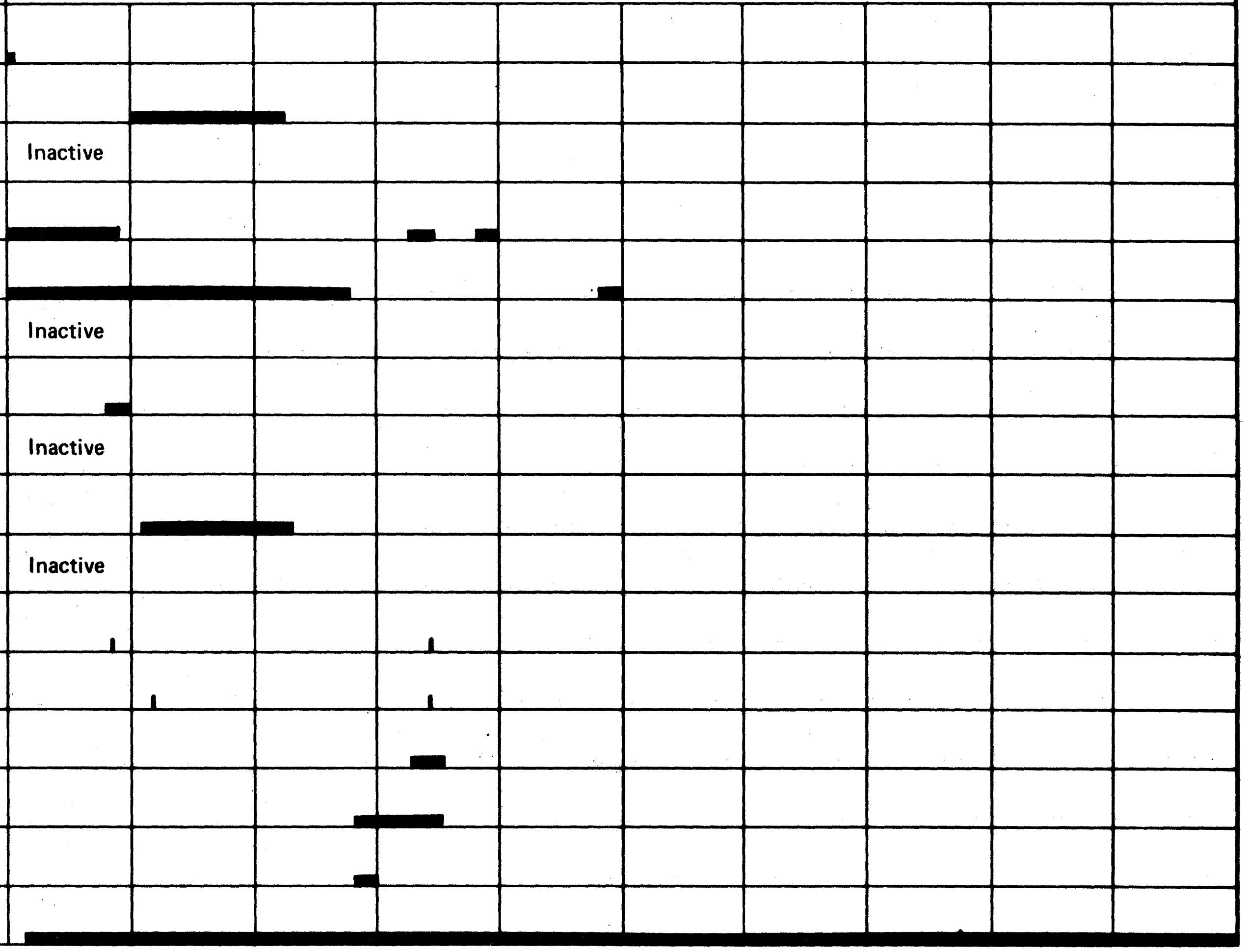


Chart Line No.	Line Name	ALD	Test Point		Test Error Number 26,25,27,22 28,29
1	–Index Alert	BH170	A2Q2 J11	D	
2	+G1	BH120	A2Q2 J09	F	
3	–G3	BH110	A2Q2 D02	B	Inactive
4	–Status Bytes Op 04	BL130	A2R2 J05	G	
5	–Bus Out Bit 5	BL130	A2R2 J11	J	
6	+Index Field	BL130	A2R2 J04	K	Inactive
7	+AM Field	BL130	A2R2 G02	L	
8	–Index Field TP	BL130	A2R2 D02	N	Inactive
9	–G1*Fmt G1	BL130	A2R2 B04	P	
10	–Transfer Sector Count	BL120	A2R2 J07	H	Inactive
11	+Sector Count Pulse	BL120	A2R2 D09	M	
12	–CT 67	BL120	A2R2 B05	E	
13	+Reorient Ctr Chk	BL120	A2R2 G04	R	
14	–TR*Reorient Chk	BL120	A2R2 J10	Q	
15	+Byte Parity Good TP	BL120	A2R2 B11	S	
16	+Sector Parity Good TP	BL120	A2R2 D11	T	

Line keys reference the diagram on DATA 320.

TRACK USED COUNTER CHECK SYMPTOM CODE

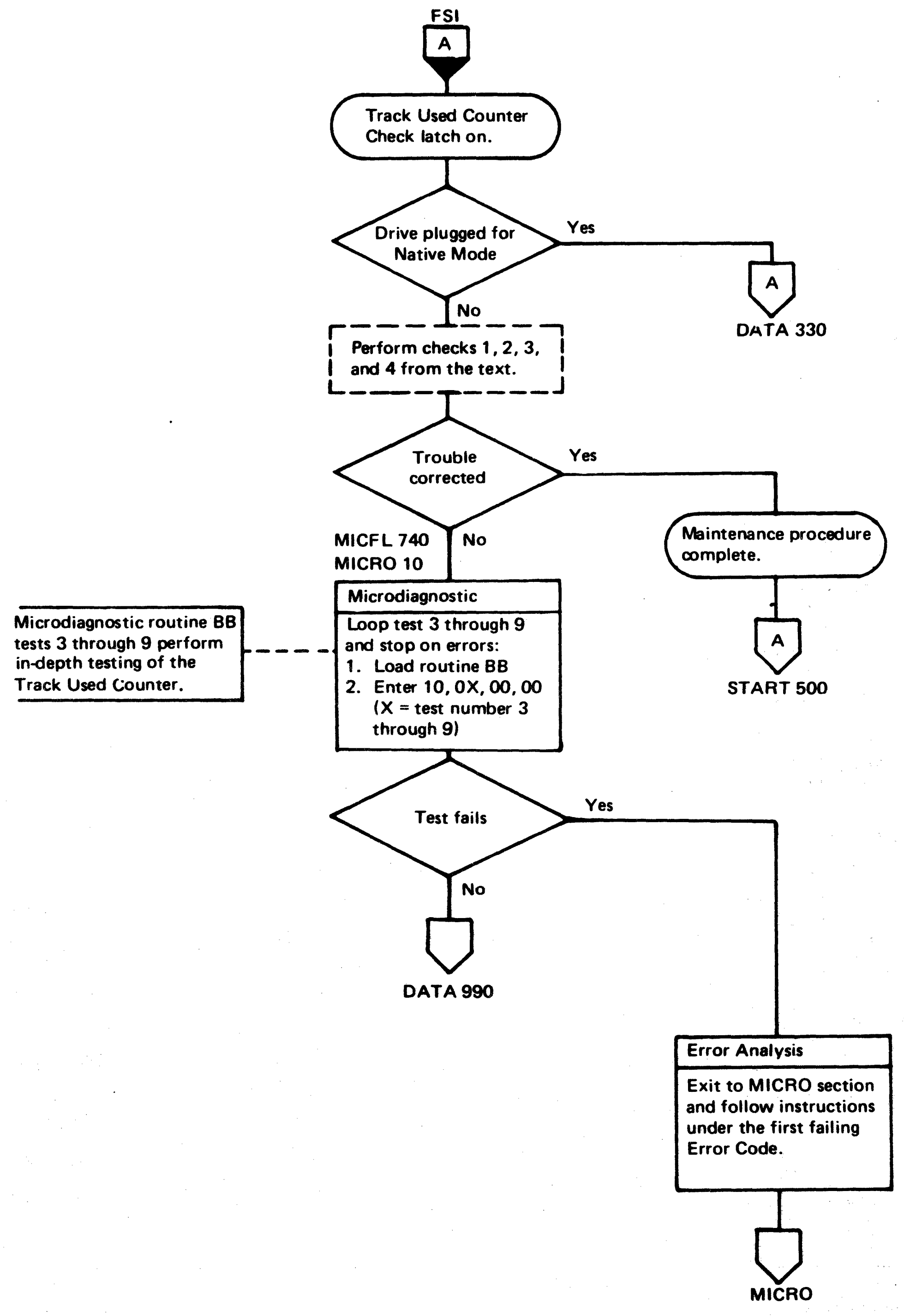
ERROR DESCRIPTION

Count fields (except Record 0) written in Native Mode produce Track Used (TR) Counter Checks if they are read in 3330-1 Compatibility Mode. Perform the following checks:

1. Verify the intended mode of the drive with the customer. If the mode has been changed, verify that DASDI has been run.
2. Visually check that the mode selection jumpers correspond with the desired mode (see chart below). Run microdiagnostic routine BB, test 0B to verify mode selection circuitry. Enter parameters per MICRO 41 (see chart below). Exit to the Error Code Dictionary if errors are encountered.
3. A machine malfunction relating to the improper mode of operation may leave residual data causing this error. Ask the operator to reformat the track(s) affected.
4. If the error occurred on the CE cylinder, that is, in routine B1 or FRIEND, run microdiagnostic routine B2 to initialize the track to the mode presently selected.

Mode	Jumper	Parameters
3350	A1F2 (A1Q2)S08 to U08	10, 0B, 01, 00
3330-1	A1F2 (A1Q2)M08 to P08	10, 0B, 20, 00
3330-11	A1F2 (A1Q2)G08 to J08	10, 0B, 03, 00

Note: *ALD pages KF110, KF120 (KQ110, KQ120) show circuits of mode selection.*



TRACK USED COUNTER RESET

ERROR DESCRIPTION

The Track Usec Counter accumulates the number of 3330-1 Compatibility Mode bytes that has been used on the track. This byte count is written on the track following each Count field.

During Search/Read operations, the Track Used count is read from the Count field and used to prime the Track Used Counter.

When the Track Used Counter reaches its limit, the TR Index line indicates that the 3330 track capacity has been exceeded. If the limit is reached while in Write mode, a Check End with Track Overrun is posted to the storage control.

This test verifies that the Track Used Counter is reset to zero following a Read G1 operation.

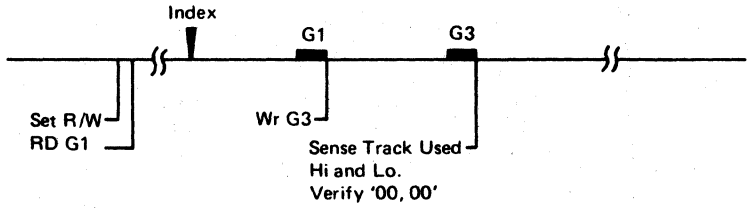
MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 3 checks the Track Used Counter reset in either 3330-1 Compatibility or Native Mode depending on the device configuration.

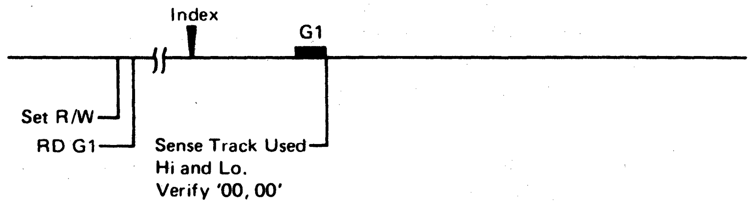
In Native Mode, the test reads a G1 record and writes a G3 record. The Track Used Counter is examined for zeros. The mode circuits should provide continuous reset to the counter.

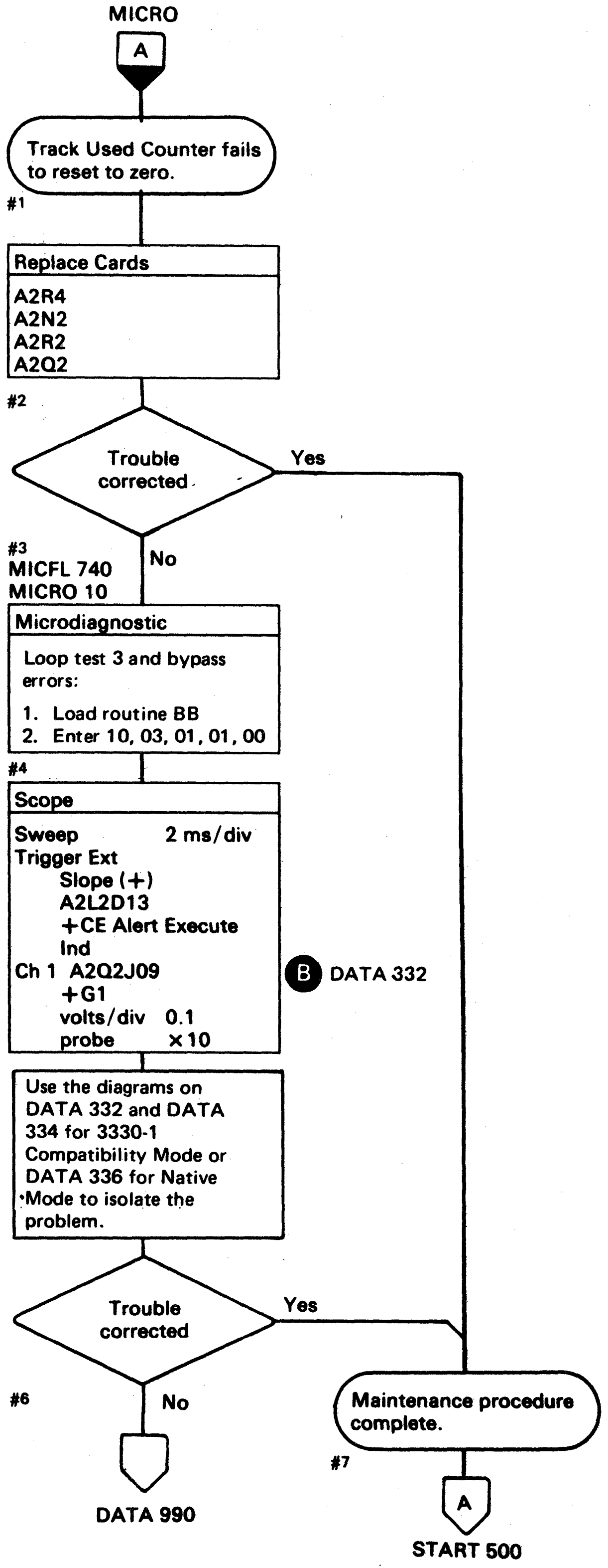
In 3330 Compatibility Mode, the test reads a G1 record and examines the Track Used Counter for zeros.

NATIVE MODE



3330-1 COMPATIBILITY MODE





#1 Track Used Counter fails to reset to zero.

#2 Replace Cards
A2R4
A2N2
A2R2
A2Q2

Trouble corrected

#3 MICFL 740
MICRO 10

Microdiagnostic

Loop test 3 and bypass errors:

1. Load routine BB
2. Enter 10, 03, 01, 01, 00

#4 Scope

Sweep 2 ms/div
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Ch 1 A2Q2J09
+G1
volts/div 0.1
probe ×10

Use the diagrams on DATA 332 and DATA 334 for 3330-1 Compatibility Mode or DATA 336 for Native Mode to isolate the problem.

#6 Trouble corrected

#7 Maintenance procedure complete.

CE0605 Seq. 2 of 2	2358816 Part No.	441303 30 Jul 76				

NATIVE MODE TRACK USED COUNTER

ERROR DESCRIPTION

The Track Used Counter accumulates the number of 3330-1 Compatibility Mode bytes that has been used on the track. This byte count is written on the track following each Count field.

During Search/Read operations, the Track Used count is read from the Count field and used to prime the Track Used Counter.

When the Track Used Counter reaches its limit, the TR Index line indicates that the 3330 track capacity has been exceeded. If the limit is reached while in Write mode, a Check End with Track Overrun is posted to the storage control.

When the drive is in Native Mode, the Track Used Counter is held at zero. This test causes the Track Used Counter to count if the reset circuits are failing. The counter is checked to be sure that it equals zero.

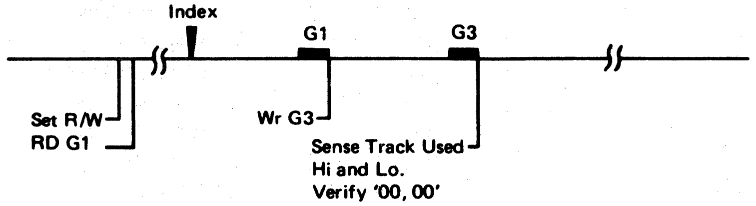
MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 3 checks the Track Used Counter reset in either 3330-1 Compatibility or Native Mode depending on the device configuration.

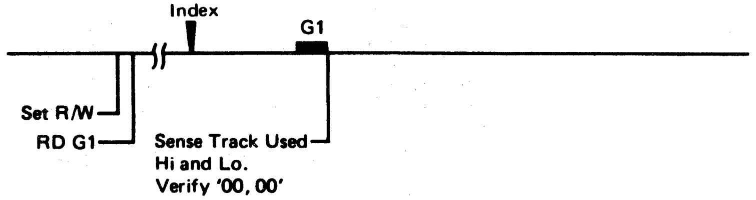
In Native Mode, the test reads a G1 record and writes a G3 record. The track Used Counter is examined for zeros. The mode circuits should provide continuous reset to the counter.

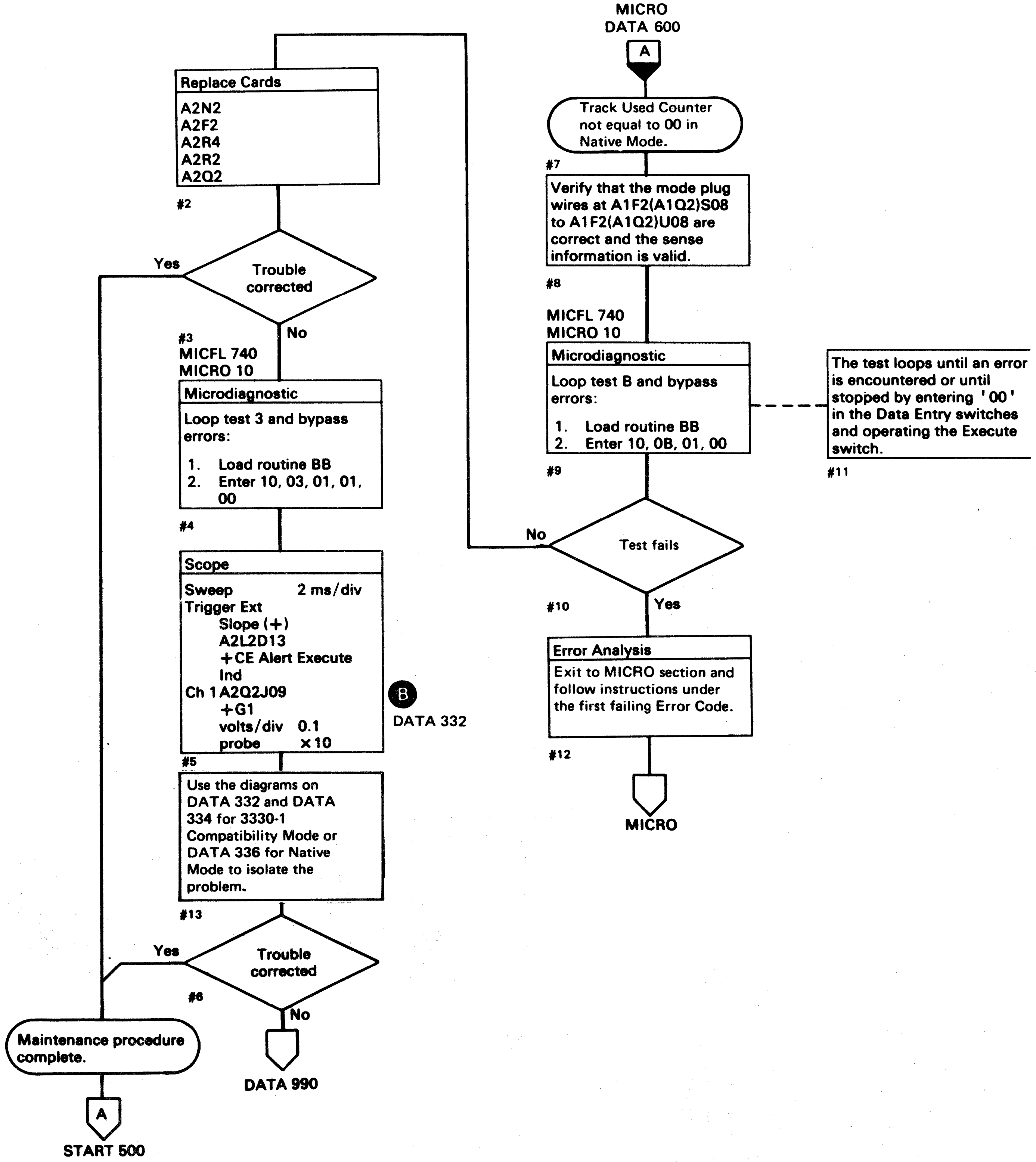
In 3330-1 Compatibility Mode, the test reads a G1 record and examines the Track Used Counter for zeros.

NATIVE MODE



3330-1 COMPATIBILITY MODE





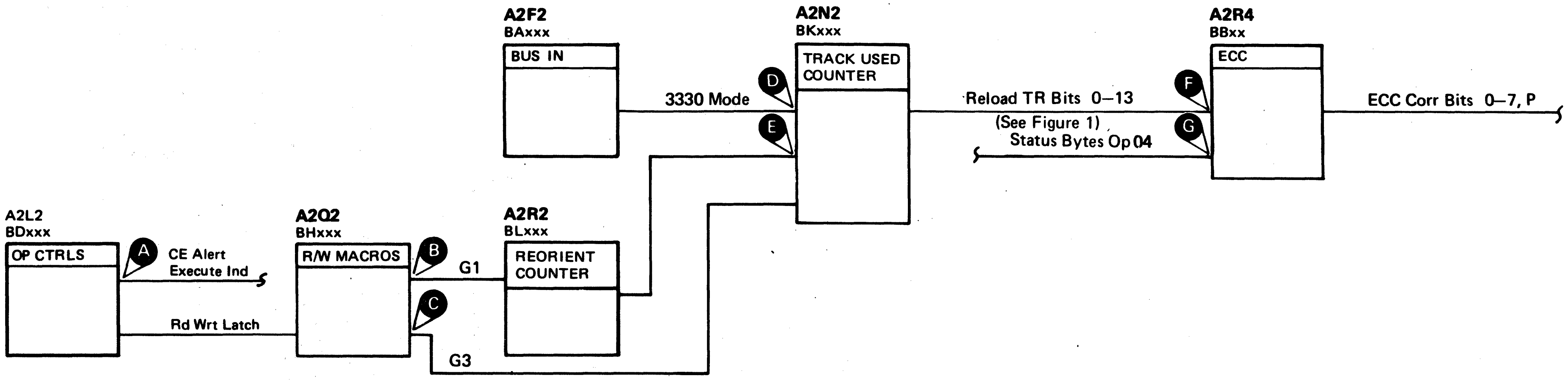
CE0610 Seq. 1 of 2	2358817 Part No.		441303 30 Jul 76				

BB TEST 3 DIAGRAM

See the sequence chart on DATA 334 for referenced test points.
See OPER 42 for theory.

Figure 1. Reload TR Bits 0–13

Line Name	A2N2 BK200	A2R4 Ⓔ BB170
–Reload TR Bit 0	U06	J10
–Reload TR Bit 1	M11	J12
–Reload TR Bit 2	S02	G08
–Reload TR Bit 3	U02	J07
–Reload TR Bit 4	S07	G04
–Reload TR Bit 5	P05	J02
–Reload TR Bit 6	U04	B11
–Reload TR Bit 7	M09	J11
–Reload TR Bit 8	G11	G12
–Reload TR Bit 9	G12	J09
–Reload TR Bit 10	J11	G07
–Reload TR Bit 11	M07	G05
–Reload TR Bit 12	M04	G02
–Reload TR Bit 13	P02	D11



BB TEST 3 SEQUENCE CHART

3330 COMPATIBILITY MODE

Microdiagnostic Setup

Routine BB, test 3
1. Load BB
2. Enter 10, 03, 00, 00

Scope Setup

Sweep	2 ms/div	Ch 1	A2U4D13 +CE Alert Execute Ind
Mode	Alt or Chop		
Trigger	Ext	Volts/div	0.1
Slope (+)		Probe	x10
A2L2D13 +CE Alert Execute Ind		Ch 2	A (see chart)

Legend: ▭ Inactive ■ Active level ▨ Tolerance

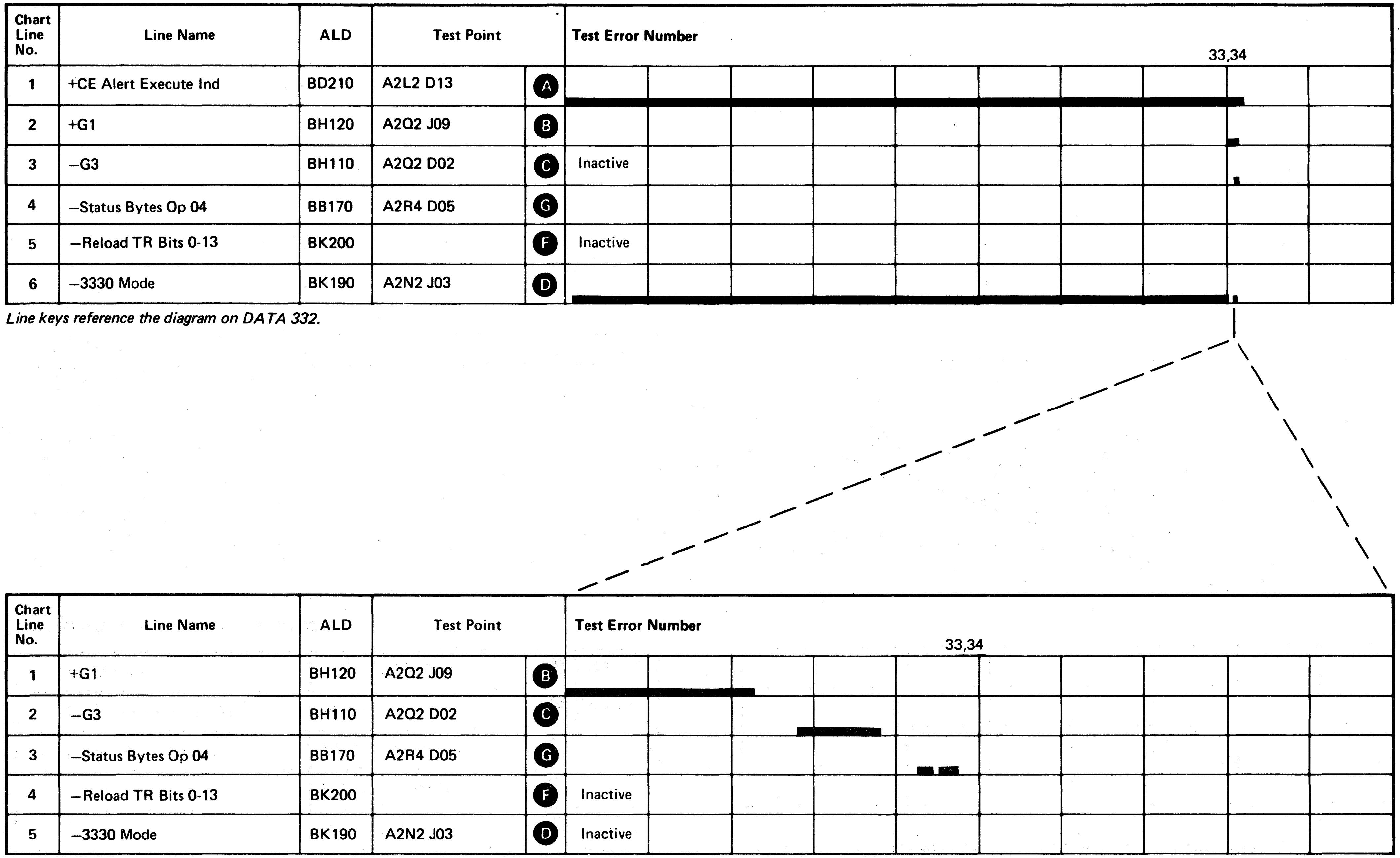


Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+CE Alert Execute Ind	BD210	A2L2 D13	Ⓐ	
2	+G1	BH120	A2Q2 J09	Ⓑ	
3	–G3	BH110	A2Q2 D02	Ⓒ	Inactive
4	–Status Bytes Op 04	BB170	A2R4 D05	Ⓖ	
5	–Reload TR Bits 0-13	BK200		Ⓕ	Inactive
6	–3330 Mode	BK190	A2N2 J03	Ⓓ	

Line keys reference the diagram on DATA 332.

Scope Setup

Sweep	2 ms/div	Ch 1	A2Q2J09 +G1
Mode	Alt or Chop		
Trigger	Ext	Volts/div	0.1
Slope (+)		Probe	x10
A2L2D13 +CE Alert Execute Ind		Ch 2	(see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 2 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 7.5
Source – Int Ch 1

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+G1	BH120	A2Q2 J09	Ⓑ	
2	–G3	BH110	A2Q2 D02	Ⓒ	
3	–Status Bytes Op 04	BB170	A2R4 D05	Ⓖ	
4	–Reload TR Bits 0-13	BK200		Ⓕ	Inactive
5	–3330 Mode	BK190	A2N2 J03	Ⓓ	Inactive

Line keys reference the diagram on DATA 332.

BB TEST 3 SEQUENCE CHART

NATIVE MODE

Legend: ☐ Inactive
■ Active level
▨ Tolerance

Microdiagnostic Setup

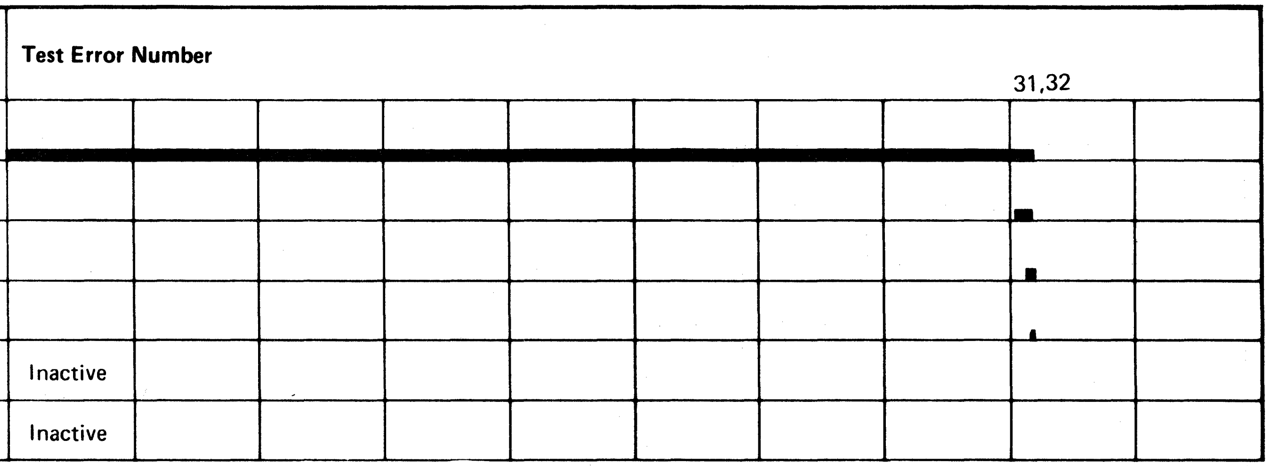
Routine BB, test 3
1. Load BB
2. Enter 10, 03, 00, 00

Scope Setup

Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+CE Alert Execute Ind	BD210	A2L2 D13	Ⓐ	
2	+G1	BH120	A2Q2 J09	Ⓑ	
3	−G3	BH110	A2Q2 D02	Ⓒ	
4	−Status Bytes Op 04	BB170	A2R4 D05	Ⓖ	
5	−Reload TR Bits 0-13	BK200		Ⓕ	Inactive
6	−3330 Mode	BK190	A2N2 J03	Ⓓ	Inactive



Line keys reference the diagram on DATA 332.

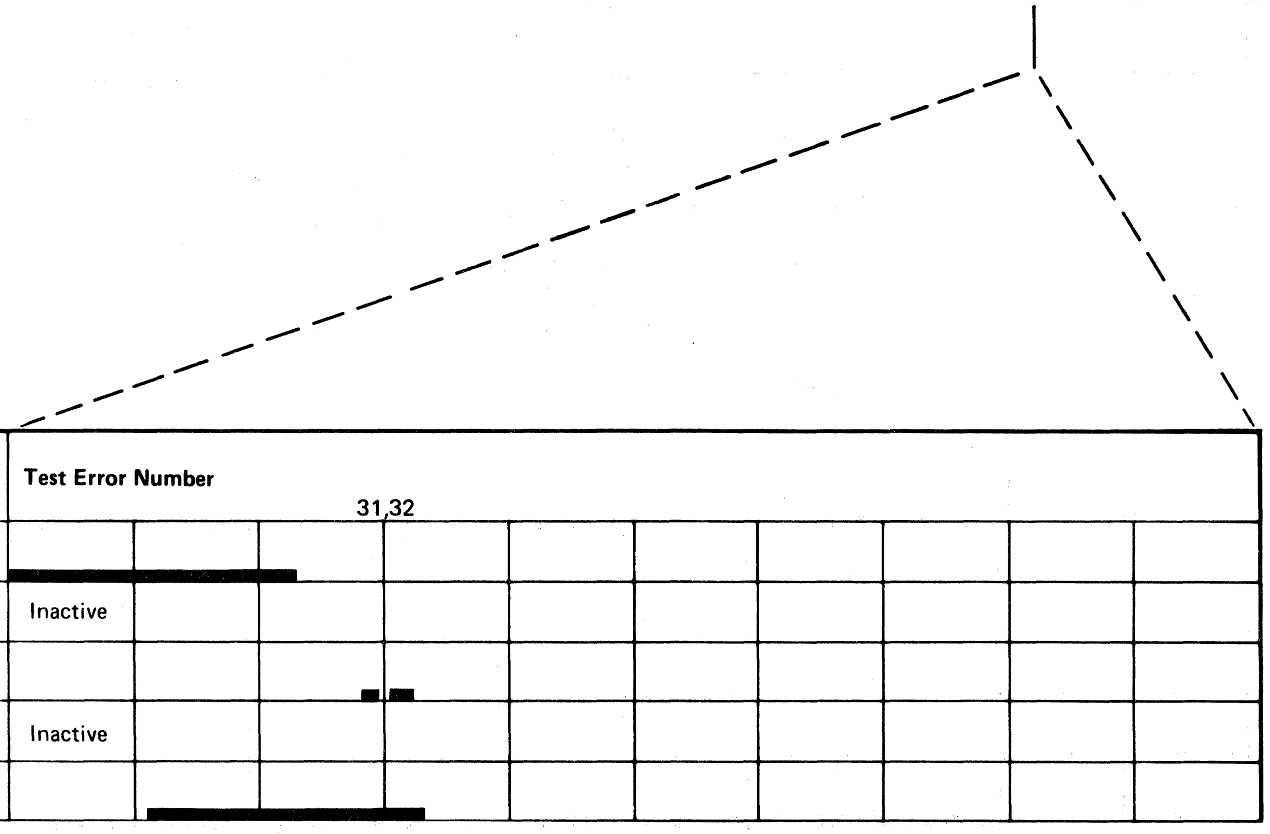
Scope Setup

Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 2 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 7.5
Source – Int Ch 1

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+G1	BH120	A2Q2 J09	Ⓑ	
2	−G3	BH110	A2Q2 D02	Ⓒ	Inactive
3	−Status Bytes Op 04	BB170	A2R4 D05	Ⓖ	
4	−Reload TR Bits 0-13	BK200		Ⓕ	Inactive
5	−3330 Mode	BK190	A2N2 J03	Ⓓ	



Line keys reference the diagram on DATA 332.

TRACK USED DESERIALIZER FAILURE

ERROR DESCRIPTION

The Track Used Counter accumulates the number of 3330-1 Compatibility Mode bytes that has been used on the track. This byte count is written on the track following each Count field.

During Search/Read operations, the Track Used count is read from the Count field and used to prime the Track Used Counter.

When the Track Used Counter reaches its limit, the TR Index line indicates that the 3330 track capacity has been exceeded. If the limit is reached while in Write mode, a Check End with Track Overrun is posted to the storage control.

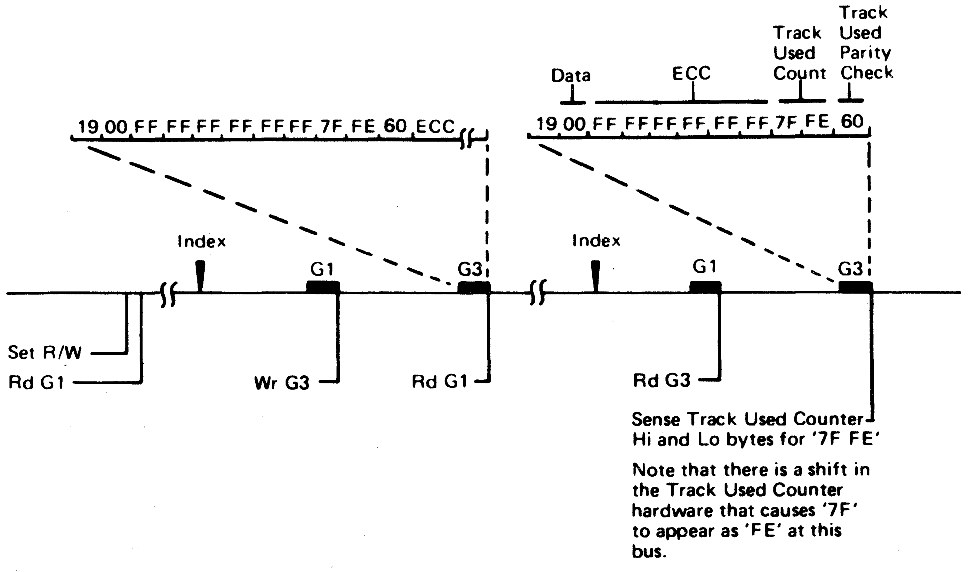
MICRODIAGNOSTIC DESCRIPTION

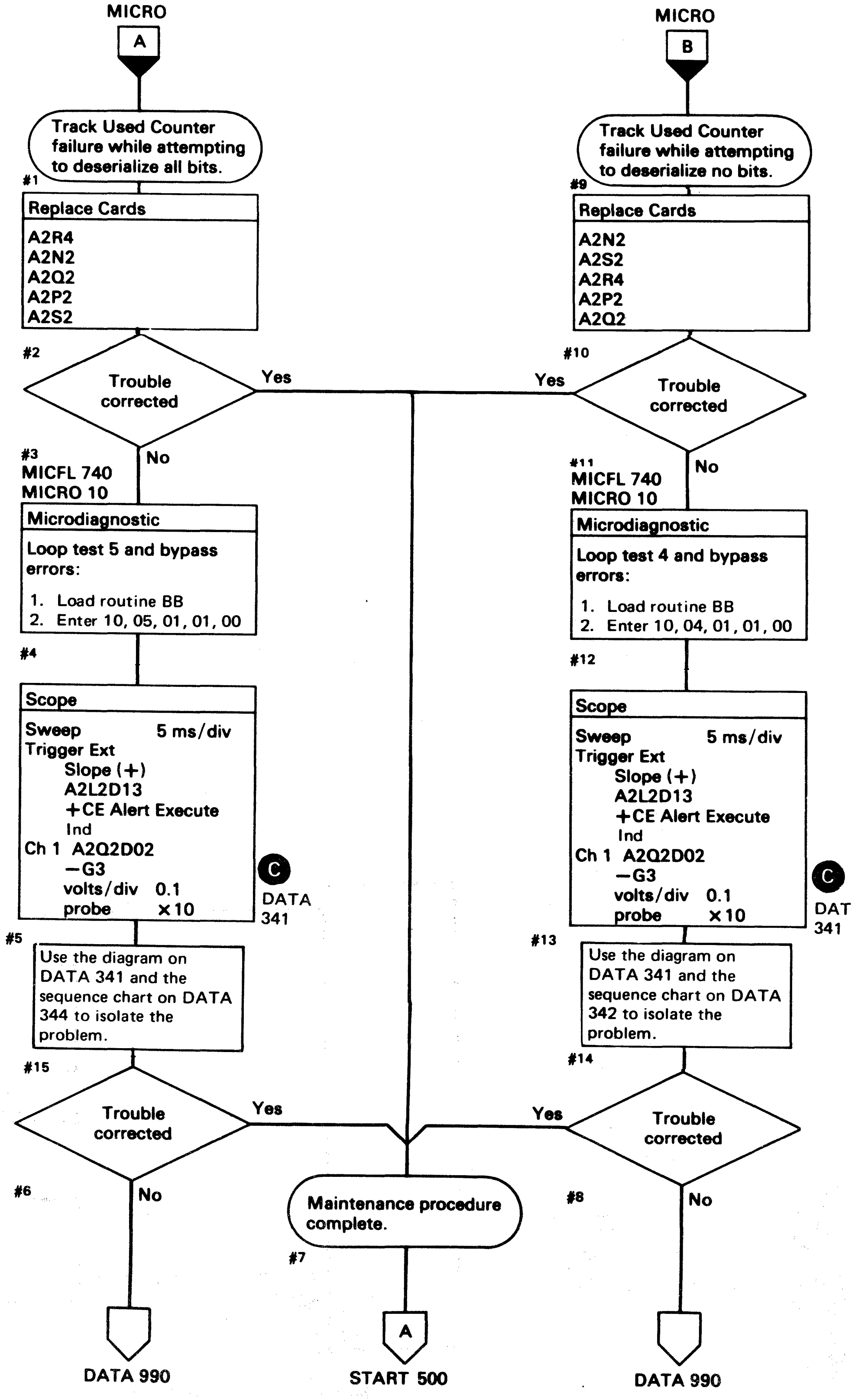
See DATA 308 for a description of routine BB, test 4.

Routine BB, test 5 reads a B1 field and then writes a G3 field of 10 bytes. The G3 field is read using a byte count of one. The field produced has the following components:

- 1 Data byte
- 6 ECC bytes
- 3 Track Used Count Bytes (2 count + Parity Check)

The Track Used Counter bytes are loaded into the counter as they are read. Sense Track Used Counter High and Sense Track Used Counter Low operations are performed and values of 'FEFE' are expected at Bus In.





CE0620 Seq. 1 of 2	2358819 Part No.	441303 30 Jul 76				

BB TEST 4 AND 5 DIAGRAM

See the sequence charts on DATA 342 and 344 for referenced test points.

See OPER 241 for theory.

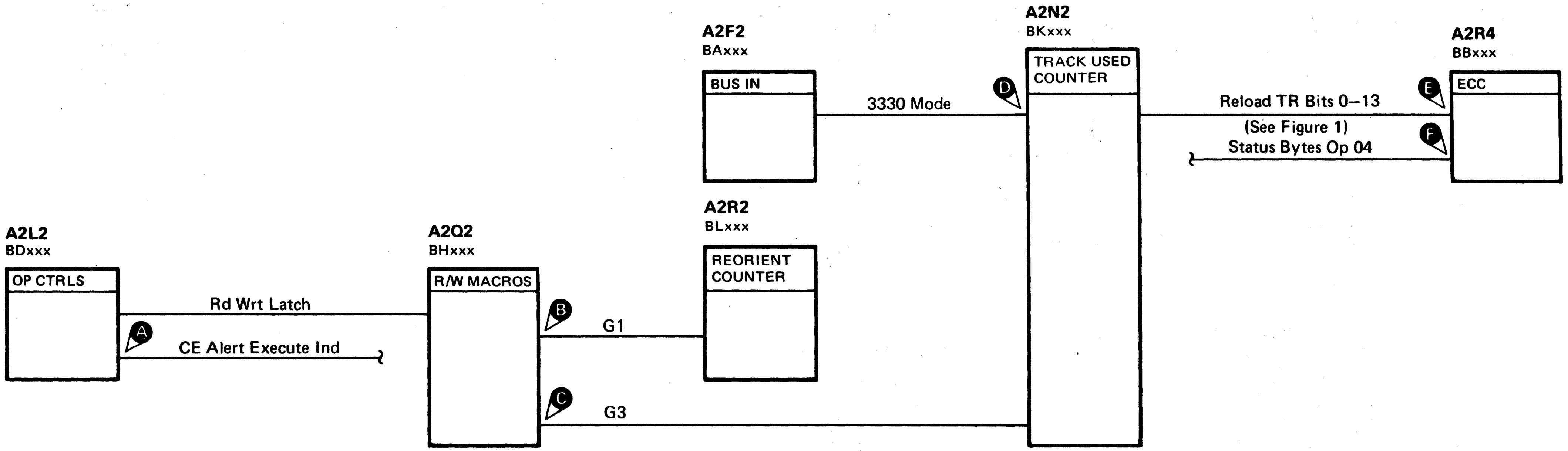


Figure 1. Reload TR Bits 0–13

Line Name	A2N2 BK200	A2R4 BB170 Ⓔ
–Reload TR Bit 0	U06	J10
–Reload TR Bit 1	M11	J12
–Reload TR Bit 2	S02	G08
–Reload TR Bit 3	U02	J07
–Reload TR Bit 4	S07	G04
–Reload TR Bit 5	P05	J02
–Reload TR Bit 6	U04	B11
–Reload TR Bit 7	M09	J11
–Reload TR Bit 8	G11	G12
–Reload TR Bit 9	G12	J09
–Reload TR Bit 10	J11	G07
–Reload TR Bit 11	M07	G05
–Reload TR Bit 12	M04	G02
–Reload TR Bit 13	P02	D11

BB TEST 4 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine BB, test 4
1. Load BB
2. Enter 10, 04, 00, 00

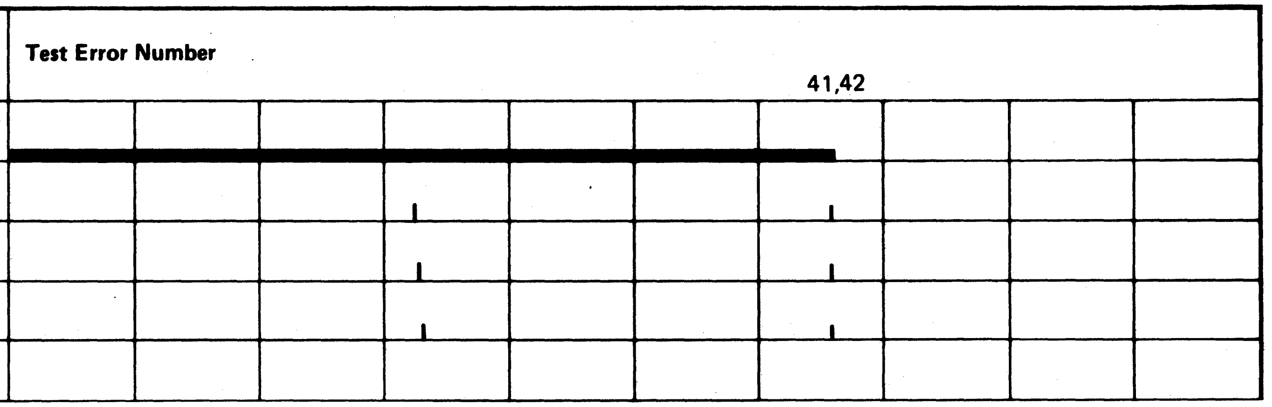
Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Legend:
- ▭ Inactive
- ■ Active level
- ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 41,42
1	+CE Alert Execute Ind	BD210	A2L2 D13	A	
2	+G1	BH120	A2Q2 J09	B	
3	−G3	BH110	A2Q2 D02	C	
4	−Status Bytes Op 04	BB170	A2R4 D05	F	
5	−Reload TR Bits	BK200	See Figure 1 on DATA 341	E	



Line keys reference the diagram on DATA 341.

TRIGGERING INSTRUCTIONS

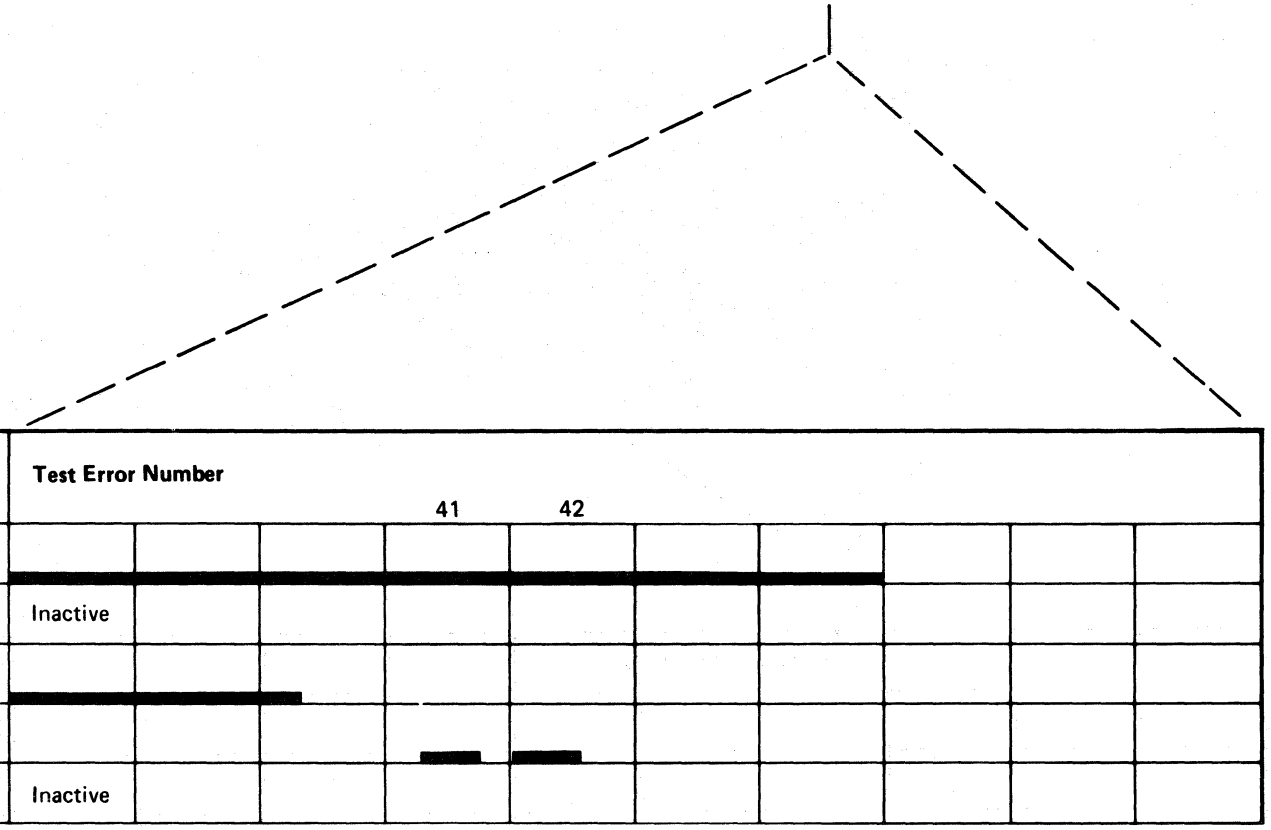
Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2D02
−G3
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (–)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 6.0
Source – Int Ch 1

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 41 42
1	+CE Alert Execute Ind	BD210	A2L2 D13	A	
2	+G1	BH120	A2Q2 J09	B	Inactive
3	−G3	BH110	A2Q2 D02	C	
4	−Status Bytes Op 04	BB170	A2R4 D05	F	
5	−Reload TR Bits 0-13	BK200	See Figure 1 on DATA 341	E	Inactive



Line keys reference the diagram on DATA 341.

BB TEST 5 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine BB, test 5
1. Load BB
2. Enter 10, 05, 00, 00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Legend:
▭ Inactive
■ Active level
▨ Tolerance

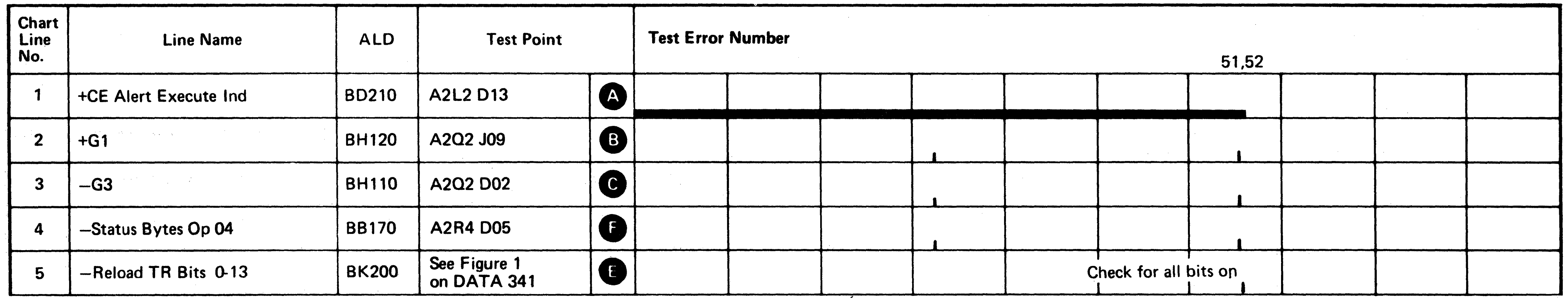


Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	Ⓐ
2	+G1	BH120	A2Q2 J09	Ⓑ
3	–G3	BH110	A2Q2 D02	Ⓒ
4	–Status Bytes Op 04	BB170	A2R4 D05	Ⓕ
5	–Reload TR Bits 0-13	BK200	See Figure 1 on DATA 341	Ⓔ

Line keys reference the diagram on DATA 341.

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 5 ms/div
Slope (–)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 6.0
Source – Int Ch 1

Ch 1 A2Q2D02
–G3
Volts/div 0.1
Probe x10
Ch 2 (see chart)

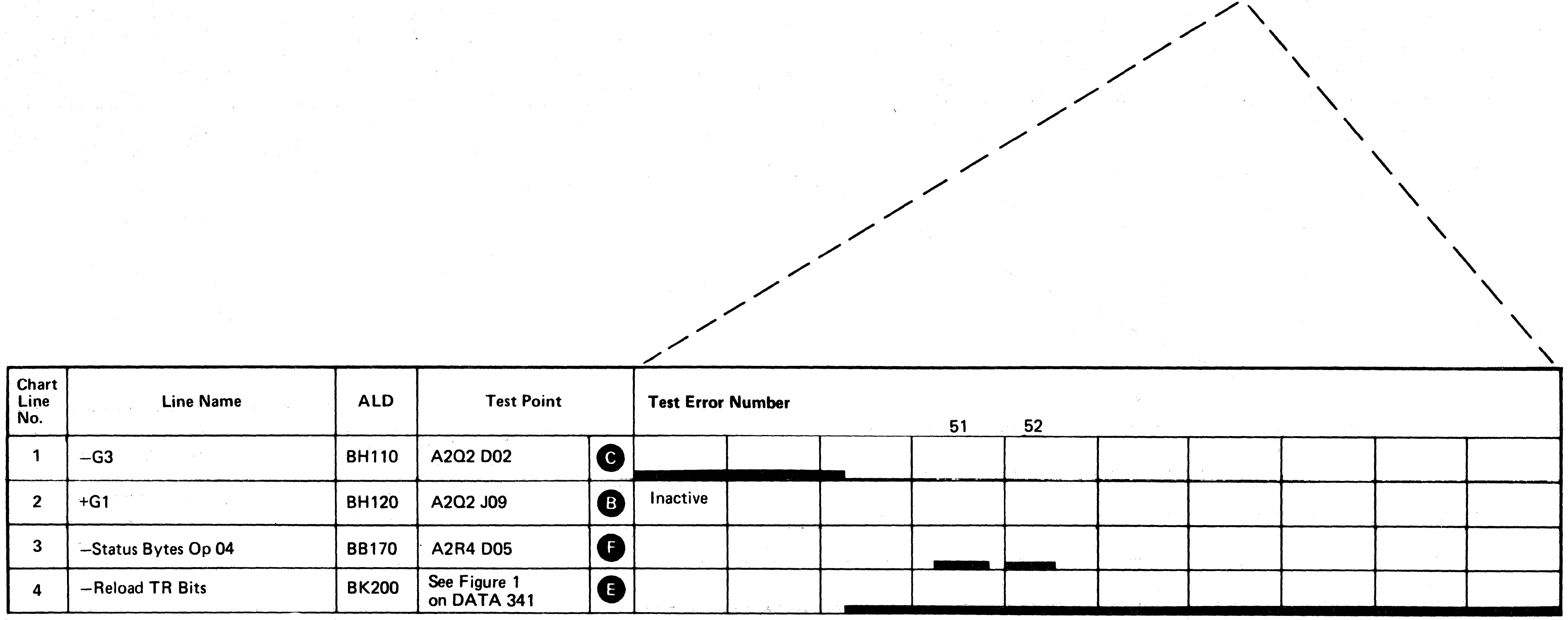


Chart Line No.	Line Name	ALD	Test Point	
1	–G3	BH110	A2Q2 D02	Ⓒ
2	+G1	BH120	A2Q2 J09	Ⓑ
3	–Status Bytes Op 04	BB170	A2R4 D05	Ⓕ
4	–Reload TR Bits	BK200	See Figure 1 on DATA 341	Ⓔ

Line keys reference the diagram on DATA 341.

NO CONTROLLER CHECK WITH TRACK USED COUNTER CHECK

ERROR DESCRIPTION

The Track Used Counter accumulates the number of 3330-1 Compatibility Mode bytes that has been used on the track. This byte count is written on the track following each Count field.

During Search/Read operations, the Track Used count is read from the Count field and used to prime the Track Used Counter.

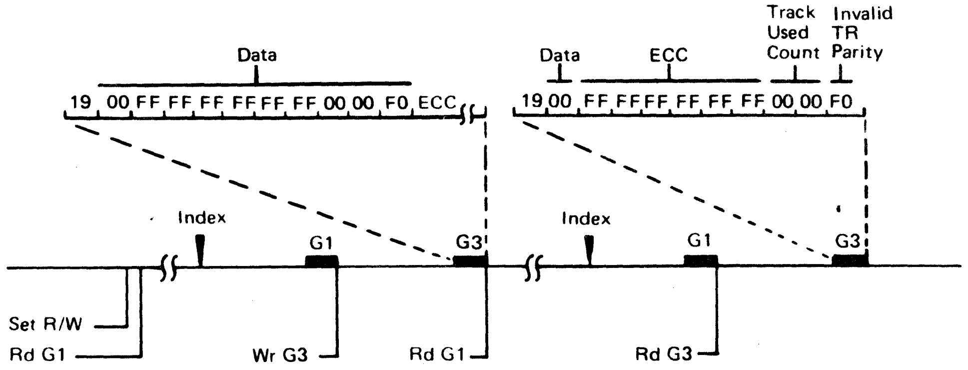
When the Track Used Counter reaches its limit, the TR Index line indicates that the 3330 track capacity has been exceeded. If the limit is reached while in Write mode, a Check End with Track Overrun is posted to the storage control.

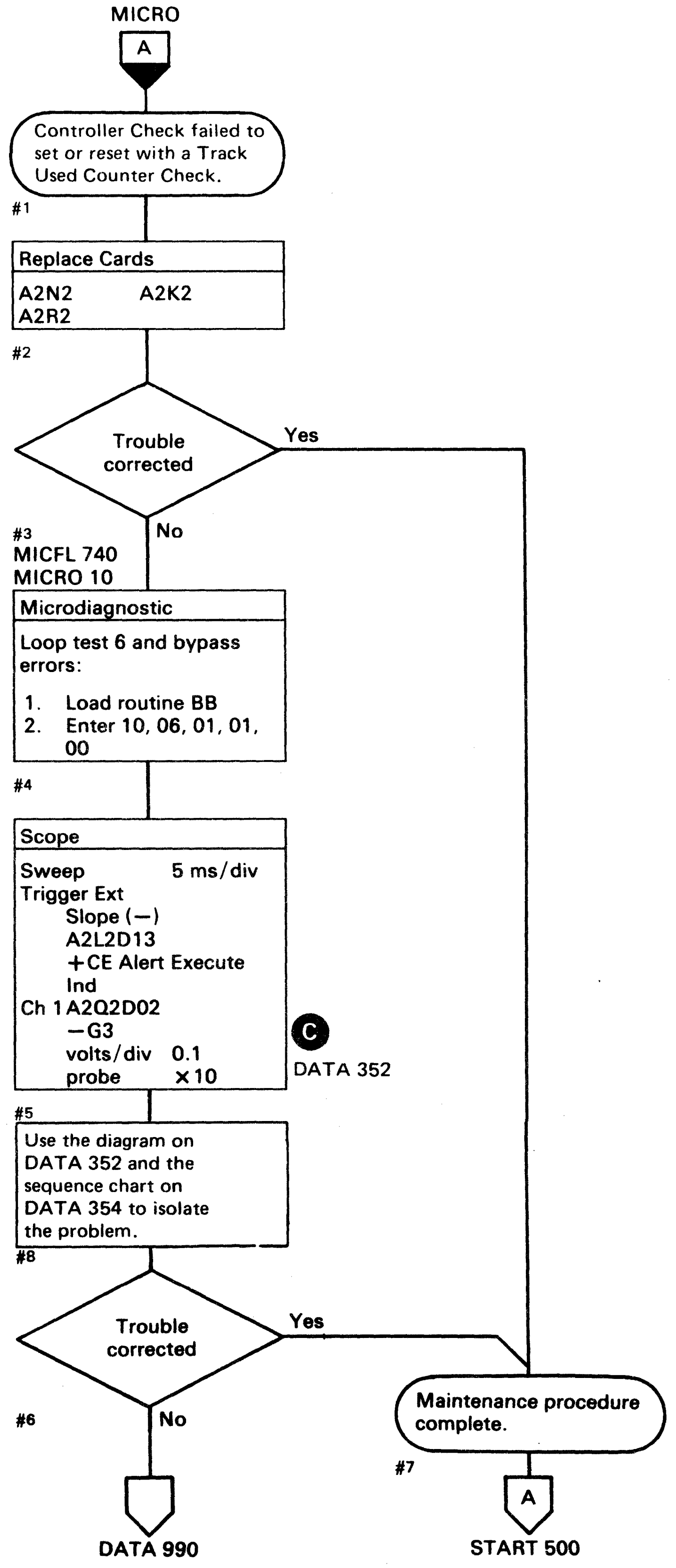
This test creates a Track Used field that has incorrect parity. When the field is read, a Parity Check is generated and verified.

The Parity Check circuit that causes a Controller Check is tested for proper operation.

MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 6 forces a Track Used Counter Check by formatting a G3 record, which, when read, appears to have an incorrect parity byte. The diagram below shows the record written and read.





3350	CE0630 Seq. 1 of 1	2358821 Part No.	441303 30 Jul 76				

TRACK USED COUNTER CHECK FAILED

ERROR DESCRIPTION

The Track Used Counter accumulates the number of 3330-1 Compatibility Mode bytes that has been used on the track. This byte count is written on the track following each Count field.

During Search/Read operations, the Track Used count is read from the Count field and used to prime the Track Used Counter.

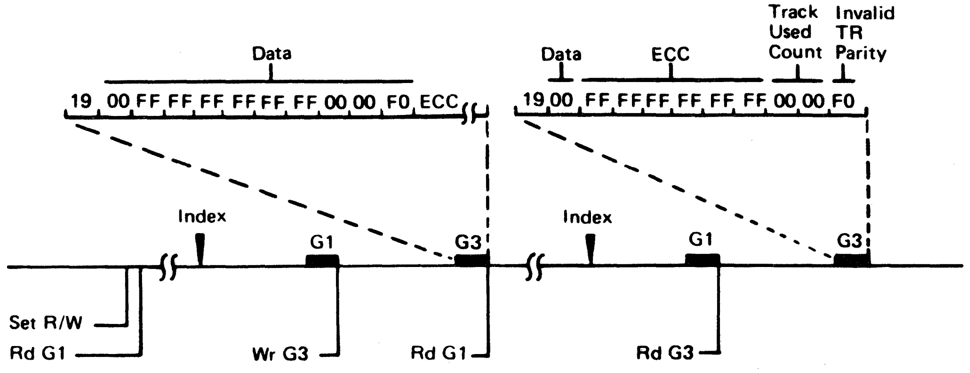
When the Track Used Counter reaches its limit, the TR Index line indicates that the 3330 track capacity has been exceeded. If the limit is reached while in Write mode, a Check End with Track Overrun is posted to the storage control.

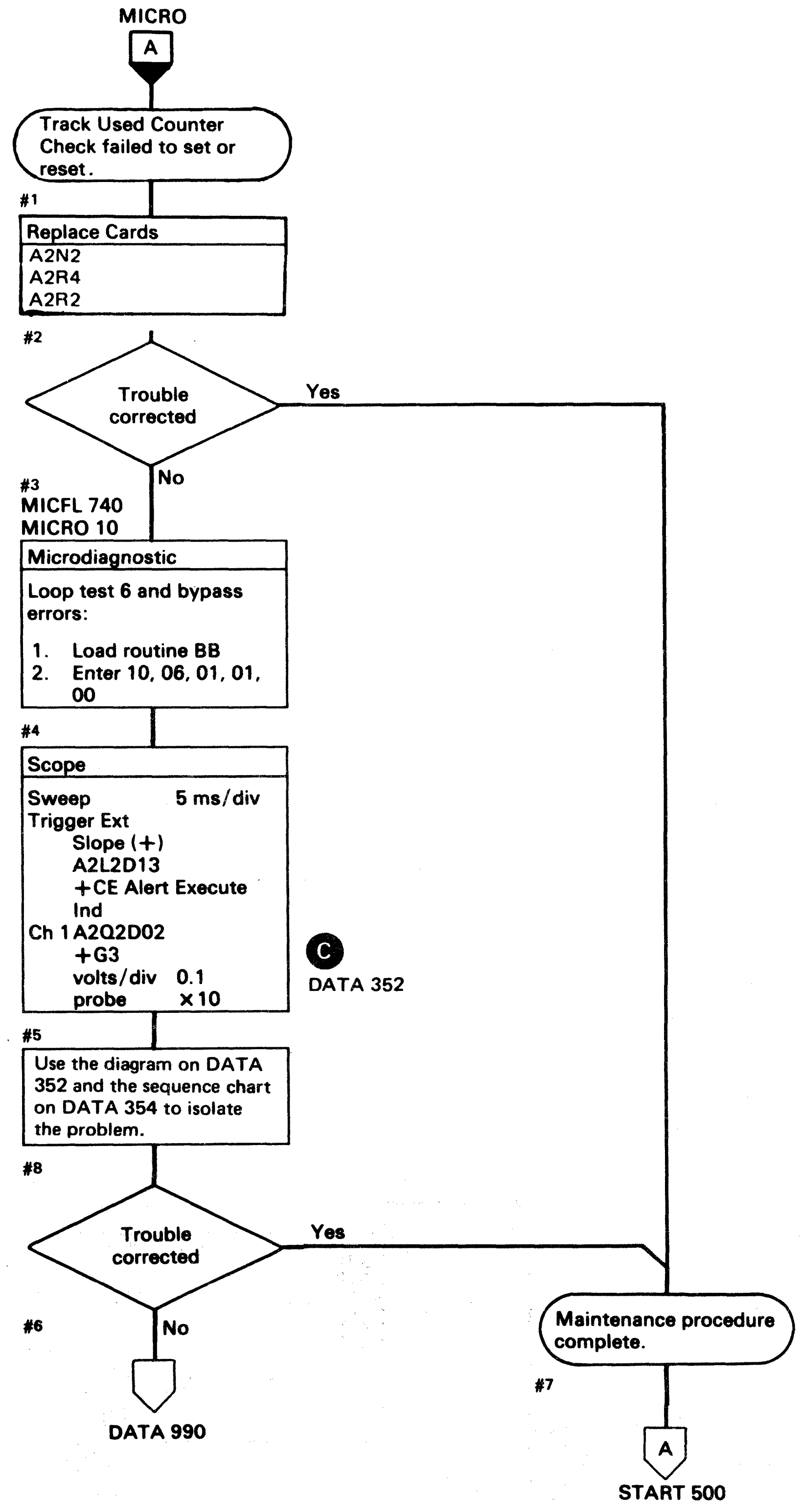
This test creates a Track Used field that has incorrect parity. When the field is read, a Parity Check is generated and verified.

The Parity Check circuit that causes a Controller Check is tested for proper operation.

MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 6 forces a Track Used Counter Check by formatting a G3 record which, when read, appears to have an incorrect parity byte. The diagram below shows the record written and read.



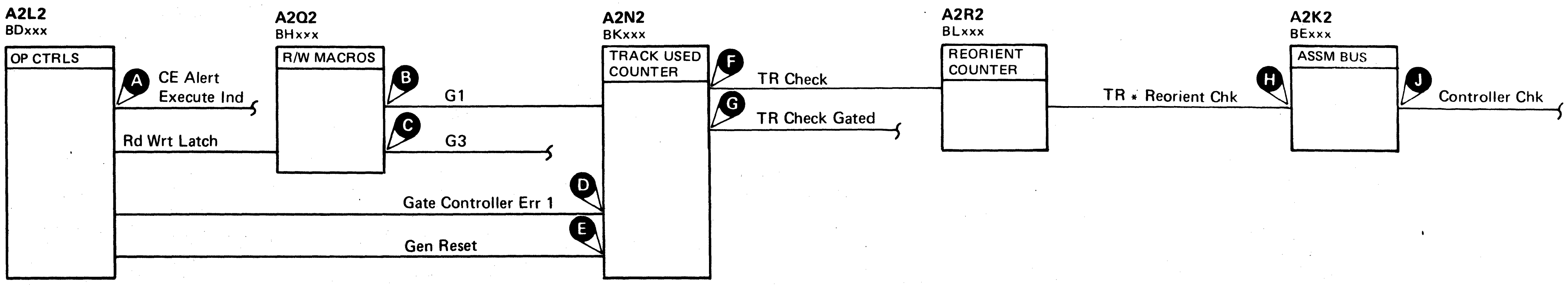


3350
CE0635 Seq. 1 of 2
2358822 Part No.
441303 30 Jul 76

BB TEST 6 DIAGRAM

See the sequence chart on DATA 354 for referenced test points.

See OPER 240 for theory.



CE0635 Seq. 2 of 2	2358822 Part No.	441303 30 Jul 76				

BB TEST 6 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine BB, test 6
1. Load BB
2. Enter 10, 06, 00, 00

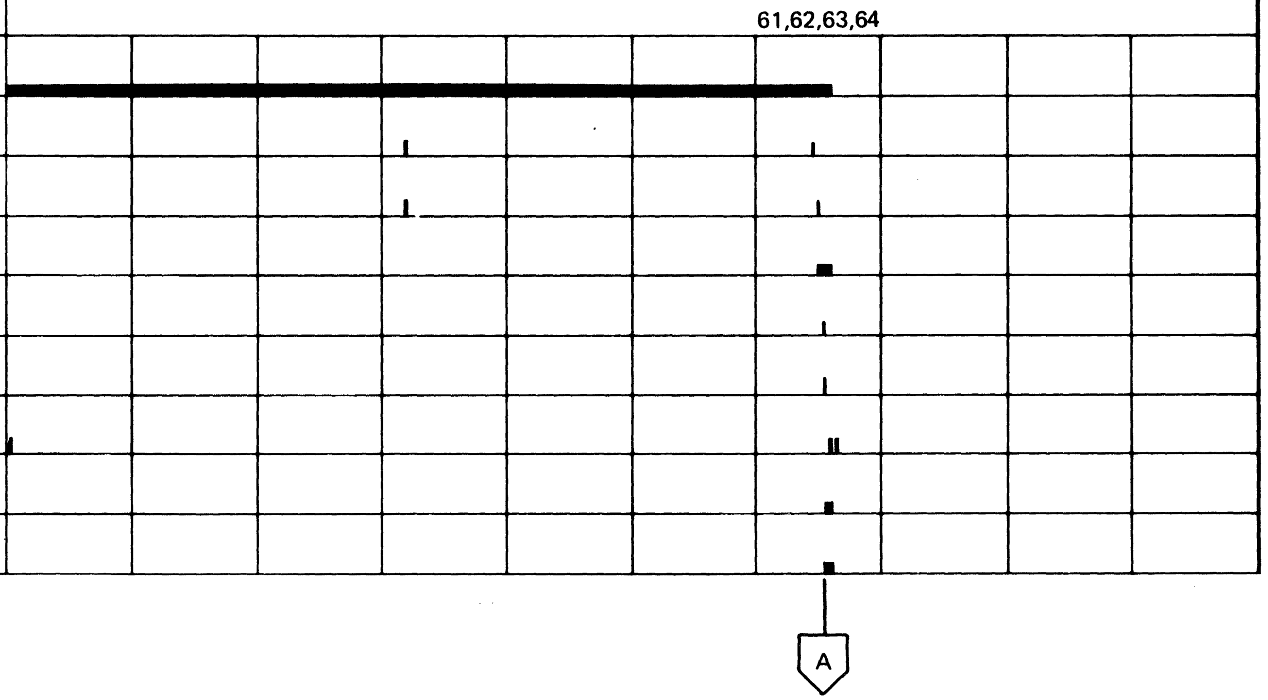
Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+CE Alert Execute Ind	BD210	A2L2 D13	Ⓐ	
2	+G1	BH120	A2Q2 J09	Ⓑ	
3	−G3	BH110	A2Q2 D02	Ⓒ	
4	+TR Check	BK140	A2N2 B10	Ⓕ	
5	−Gate Controller Err 1	BK140	A2N2 D05	Ⓓ	
6	+TR Check Gated	BK140	A2N2 B04	Ⓖ	
7	+Gen Reset	BK140	A2N2 D06	Ⓔ	
8	−Controller Check	BE130	A2K2 M12	Ⓙ	
9	−TR*Reorient Chk	BE130	A2K2 U03	Ⓗ	



Line keys reference the diagram on DATA 352.

DATA 356
(For expanded sequences chart)

BB TEST 6 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

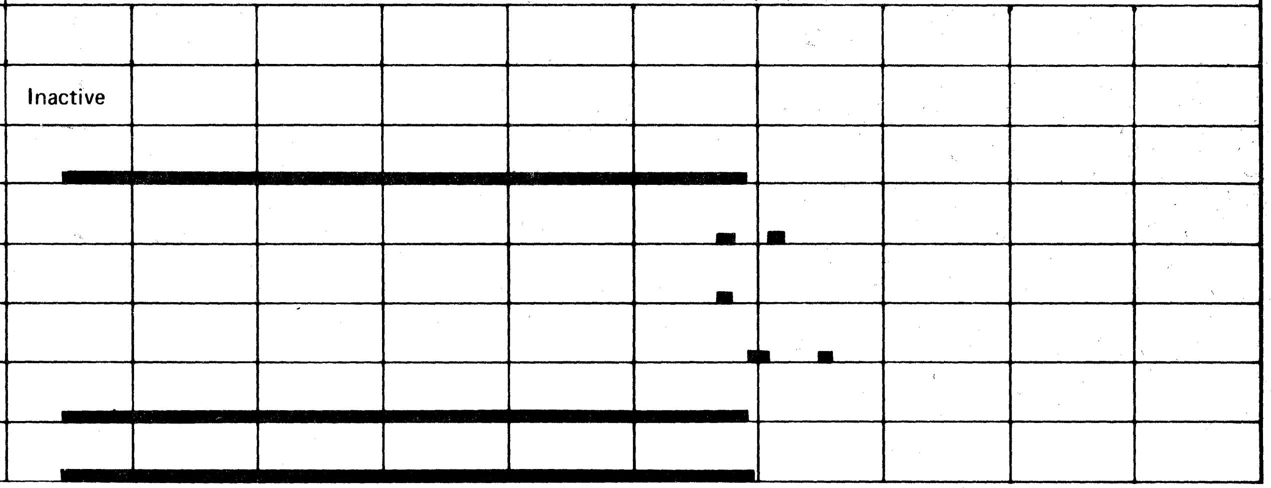
Scope Setup

Sweep 5 ms/div — Ch 1 A2Q2D02
Mode Alt or Chop — −G3
Trigger Ext — Volts/div 0.1
Slope (+) — Probe x10
A2L2D13 — Ch 2 (see chart)
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (−)
Delay Time-Delayed Sweep – 0.1 ms/div
Delay-Time Multiplier – 6.0
Source – Int Ch 1

DATA 354
A

Legend:
□ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 61,62,63,64
1	−G3	BH110	A2Q2 D02	C	
2	+G1	BH120	A2Q2 J09	B	Inactive
3	+TR Check	BK140	A2N2 B10	F	
4	−Gate Controller Err 1	BK140	A2N2 D05	D	
5	+TR Check Gate D	BK140	A2N2 B04	G	
6	+Gen Reset	BK140	A2N2 D06	E	
7	−Controller Check	BE130	A2K2 M12	J	
8	−TR*Reorient Chk	BE130	A2K2 U03	H	



Line keys reference the diagram on DATA 352.

TRACK USED COUNTER FAILS TO SERIALIZE

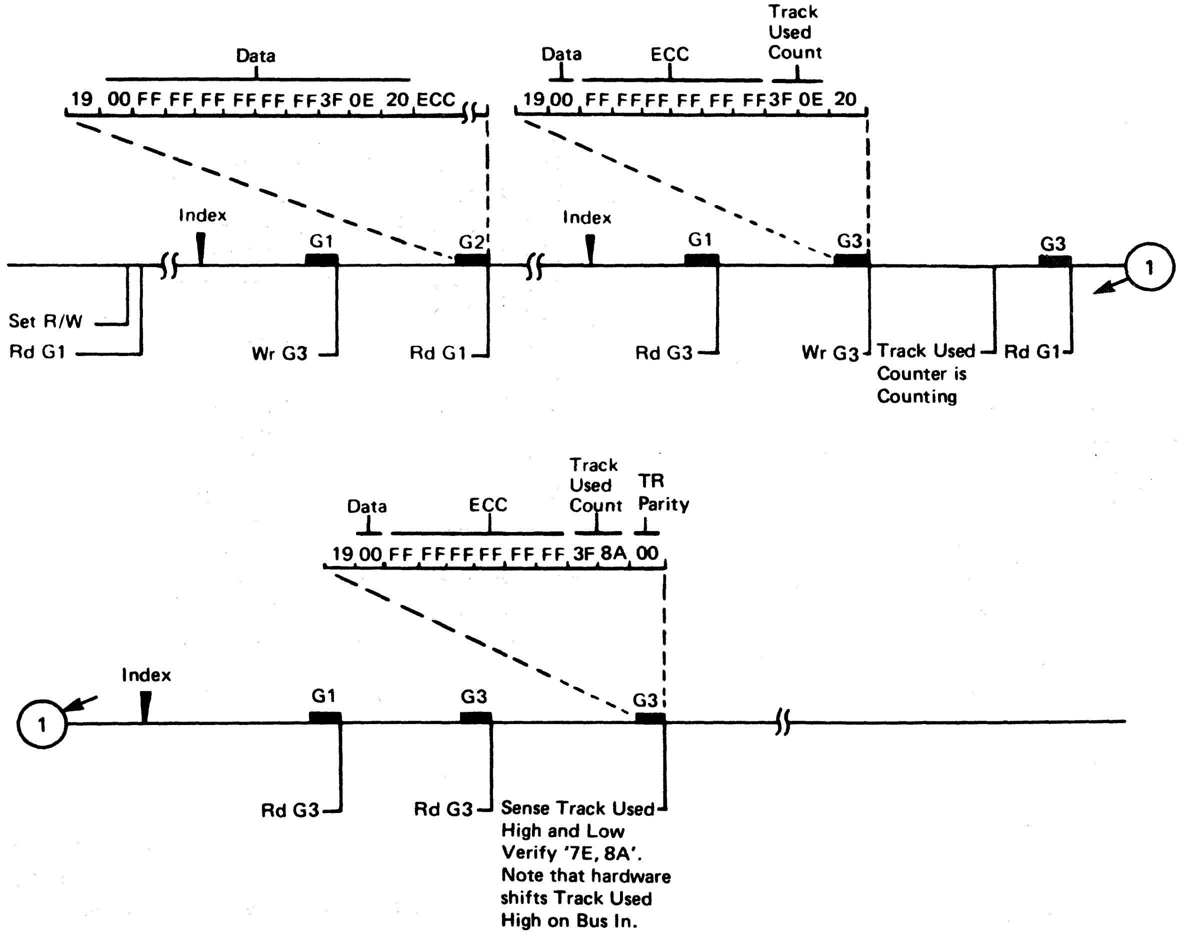
ERROR DESCRIPTION

The Track Used Counter accumulates the number of 3330-1 Compatibility Mode bytes that has been used on the track. This byte count is written on the track following each Count field.

During Search/Read operations, the Track Used count is read from the Count field and used to prime the Track Used Counter.

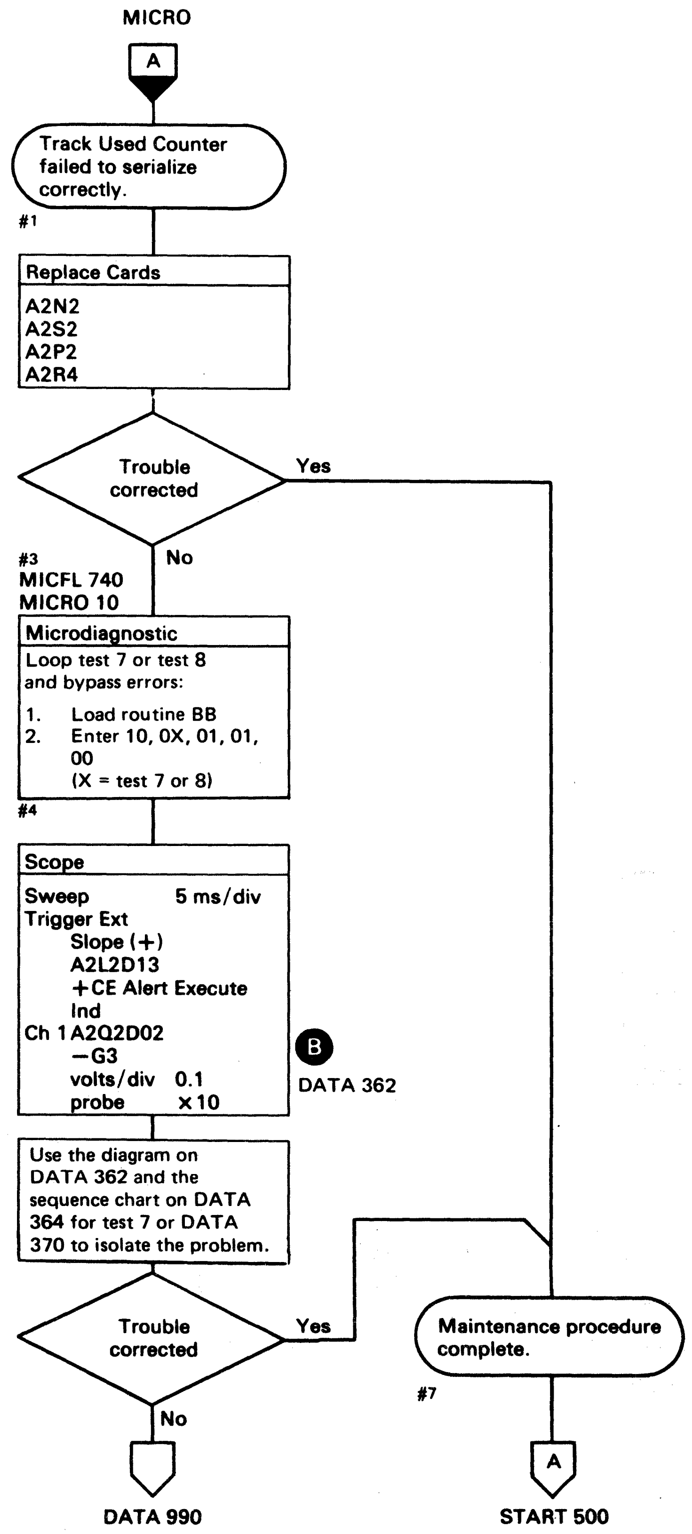
When the Track Used Counter reaches its limit, the TR Index line indicates that the 3330 track capacity has been exceeded. If the limit is reached while in Write mode, a Check End with Track Overrun is posted to the storage control.

This test causes predetermined information to be serialized from the Track Used Counter. The information is then read into the Track Used Counter storage and compared for accuracy.



MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 7 reads a G1 record and creates a G3 record, which when read, loads the Track Used Counter with a predetermined value. The Track Used Counter then starts to count, beginning with the value read. A subsequent Write G3 writes a value that reflects the results of that count. The value is read and verified using Sense Track Used High and Sense Track Used Low commands.



CE0645 Seq. 1 of 2	2358824 Part No.	441303 30 Jul 76				

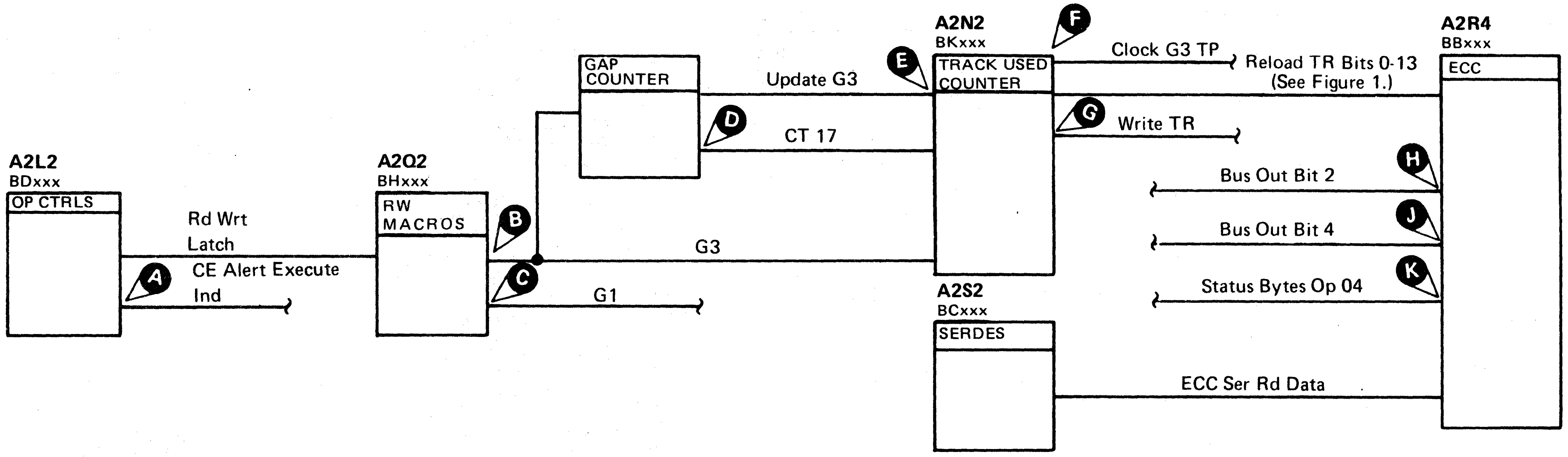
BB TEST 7 AND 8 DIAGRAM

See the sequence charts on DATA 364 and 370 for referenced test points.

See OPER 240 for theory.

Figure 1. Reload TR Bits 0–13

Line Name	A2N2 BK200	A2R4 BB170
–Reload TR Bit 0	U06	J10
–Reload TR Bit 1	M11	J12
–Reload TR Bit 2	S02	G08
–Reload TR Bit 3	U02	J07
–Reload TR Bit 4	S07	G04
–Reload TR Bit 5	P05	J02
–Reload TR Bit 6	U04	B11
–Reload TR Bit 7	M09	J11
–Reload TR Bit 8	G11	G12
–Reload TR Bit 9	G12	J09
–Reload TR Bit 10	J11	G07
–Reload TR Bit 11	M07	G05
–Reload TR Bit 12	M04	G02
–Reload TR Bit 13	P02	D11



BB TEST 7 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine BB, test 7
1. Load BB
2. Enter 10, 07, 00, 00

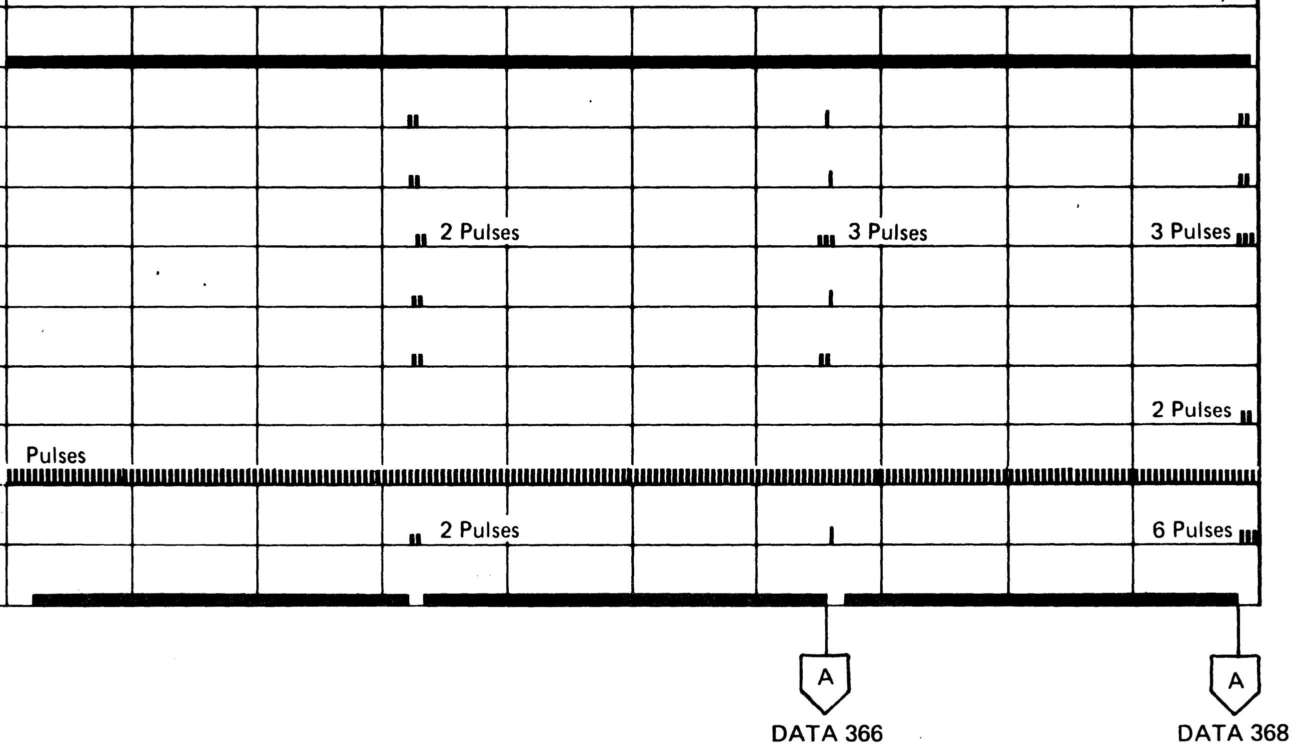
Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Legend: ▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 71,72
1	+CE Alert Execute Ind	BD210	A2L2 D13	A	
2	+G1	BH120	A2Q2 J09	C	
3	−G3	BH110	A2Q2 D02	B	
4	+Clock G3 TP	BK200	A2N2 D09	F	
5	−Write TR	BK100	A2N2 D12	G	
6	+Update G3	BK210	A2N2 G05	E	
7	−Status Bytes Op 04	BB150	A2R4 D05	K	
8	−CT 17	BG130	A2P2 P12	D	
9	−Bus Out Bit 2	BB170	A2R4 B12	H	
10	−Bus Out Bit 4	BB170	A2R4 D12	J	



(For expanded sequence chart)

Line keys reference the diagram on DATA 362.

BB TEST 7 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep	5 ms/div	Ch 1	A2Q2D02 −G3
Mode	Alt or Chop		
Trigger	Ext	Volts/div	0.1
	Slope (+)	Probe	x10
	A2L2D13 +CE Alert Execute Ind	Ch 2	(see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 5 ms/div
Slope (–)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 6.0
Source – Int Ch 1

DATA 364
A

Legend: ▭ Inactive ■ Active level ▨ Tolerance

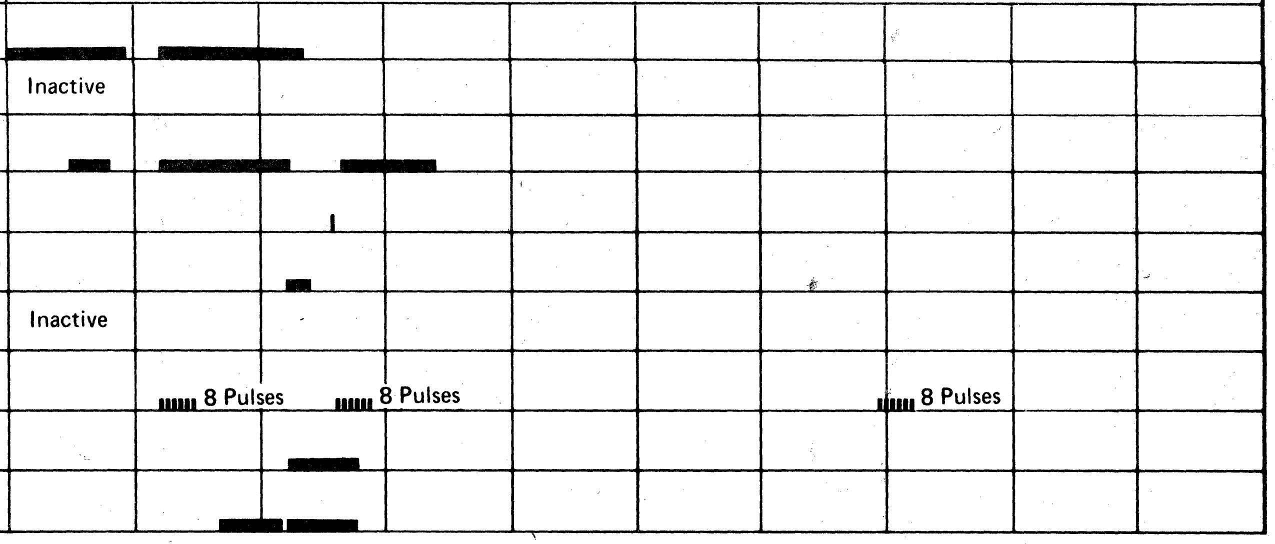


Chart Line No.	Line Name	ALD	Test Point		Test Error Number None
1	−G3	BH110	A2Q2 D02	B	
2	+G1	BH120	A2Q2 J09	C	Inactive
3	+Clock G3 TP	BK200	A2N2 D09	F	
4	−Write TR	BK100	A2N2 D12	G	
5	+Update G3	BK210	A2N2 G05	E	
6	−Status Bytes Op 04	BB150	A2R4 D05	K	Inactive
7	−CT 17	BG130	A2P2 P12	D	8 Pulses 8 Pulses 8 Pulses
8	−Bus Out Bit 2	BB170	A2R4 B12	H	
9	−Bus Out Bit 4	BB170	A2R4 D12	J	

Line keys reference the diagram on DATA 362.

3350	CE0650 Seq. 2 of 2	2358825 Part No.	441303 30 Jul 76				

BB TEST 7 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2D02
−G3
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (–)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 9.5
Source – Int Ch 1

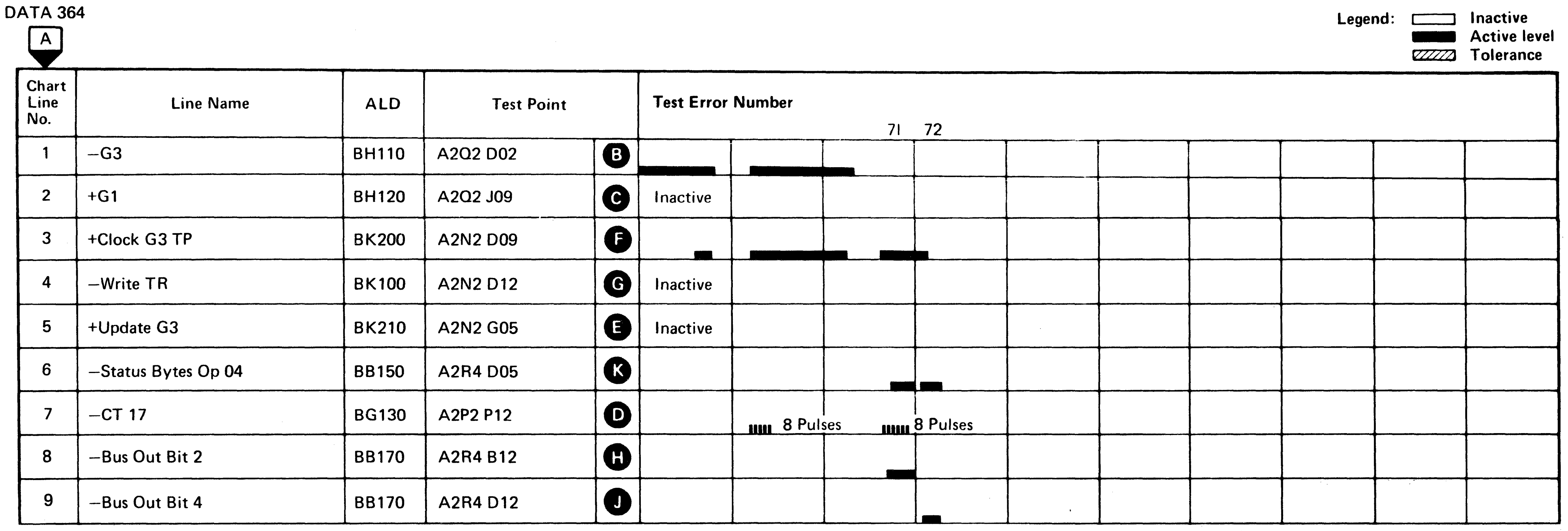


Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	−G3	BH110	A2Q2 D02	B	
2	+G1	BH120	A2Q2 J09	C	Inactive
3	+Clock G3 TP	BK200	A2N2 D09	F	
4	−Write TR	BK100	A2N2 D12	G	Inactive
5	+Update G3	BK210	A2N2 G05	E	Inactive
6	−Status Bytes Op 04	BB150	A2R4 D05	K	
7	−CT 17	BG130	A2P2 P12	D	8 Pulses 8 Pulses
8	−Bus Out Bit 2	BB170	A2R4 B12	H	
9	−Bus Out Bit 4	BB170	A2R4 D12	J	

Line keys reference the diagram on DATA 362.

CE0655 Seq. 1 of 2	2358826 Part No.	441303 30 Jul 76				

BB TEST 8 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Legend: ▭ Inactive ■ Active level ▨ Tolerance

Microdiagnostic Setup

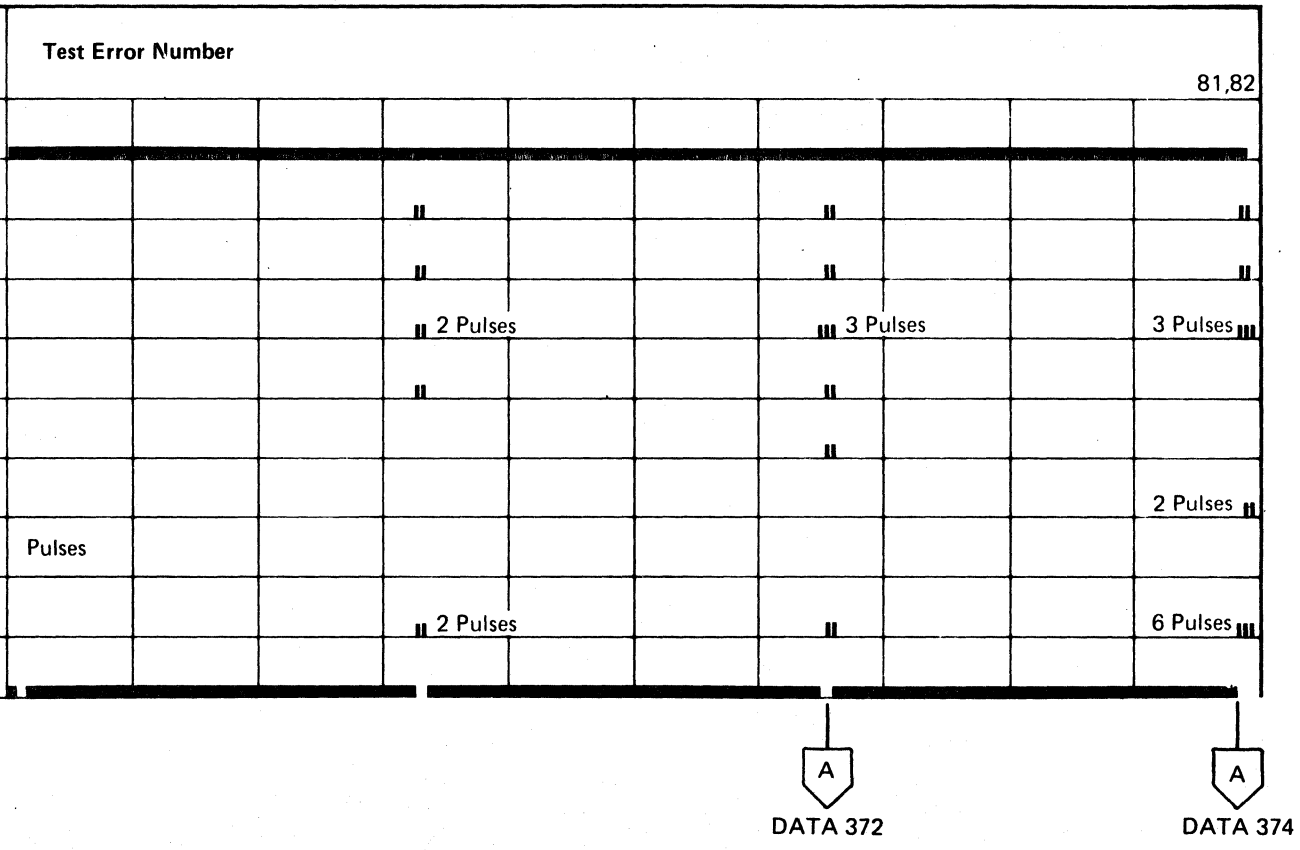
Routine BB, test 8
1. Load BB
2. Enter 10, 08, 00, 00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 81,82
1	+CE Alert Execute Ind	BD210	A2L2 D13	A	
2	+G1	BH120	A2Q2 J09	C	
3	−G3	BH110	A2Q2 D02	B	
4	+Clock G3 TP	BK200	A2N2 D09	F	2 Pulses 3 Pulses 3 Pulses
5	−Write TR	BK100	A2N2 D12	G	
6	+Update G3	BK210	A2N2 G05	E	
7	−Status Bytes Op 04	BB150	A2R4 D05	K	2 Pulses
8	−CT 17	BG130	A2P2 P12	D	Pulses
9	−Bus Out Bit 2	BB170	A2R4 B12	H	2 Pulses 6 Pulses
10	−Bus Out Bit 4	BB170	A2R4 D12	J	



Line keys reference the diagram on DATA 362.

(For expanded sequence chart)

BB TEST 8 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope(+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2D02
−G3
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/Div – 5 ms/div
Slope (–)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 6.0
Source – Int Ch 1

DATA 370

A

Legend: □ Inactive ■ Active level ▨ Tolerance

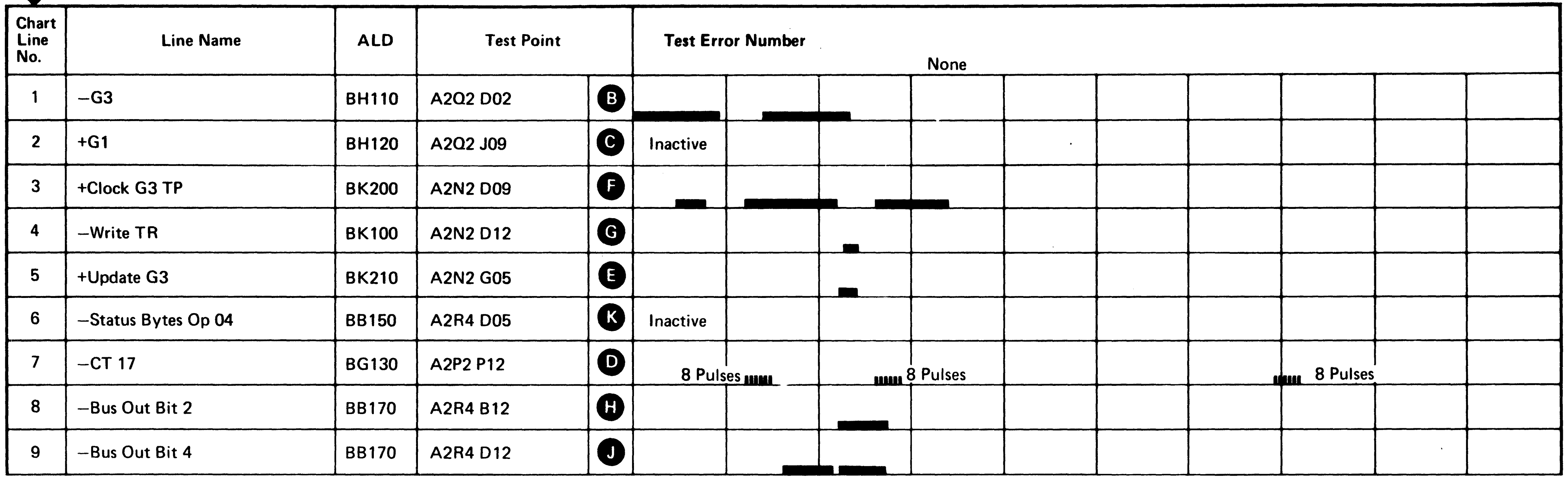


Chart Line No.	Line Name	ALD	Test Point		Test Error Number None
1	−G3	BH110	A2Q2 D02	B	
2	+G1	BH120	A2Q2 J09	C	Inactive
3	+Clock G3 TP	BK200	A2N2 D09	F	
4	−Write TR	BK100	A2N2 D12	G	
5	+Update G3	BK210	A2N2 G05	E	
6	−Status Bytes Op 04	BB150	A2R4 D05	K	Inactive
7	−CT 17	BG130	A2P2 P12	D	8 Pulses 8 Pulses 8 Pulses
8	−Bus Out Bit 2	BB170	A2R4 B12	H	
9	−Bus Out Bit 4	BB170	A2R4 D12	J	

Line keys reference the diagram on DATA 362.

3350	CE0660 Seq. 1 of 2	2358827 Part No.	441303 30 Jul 76				

BB TEST 8 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

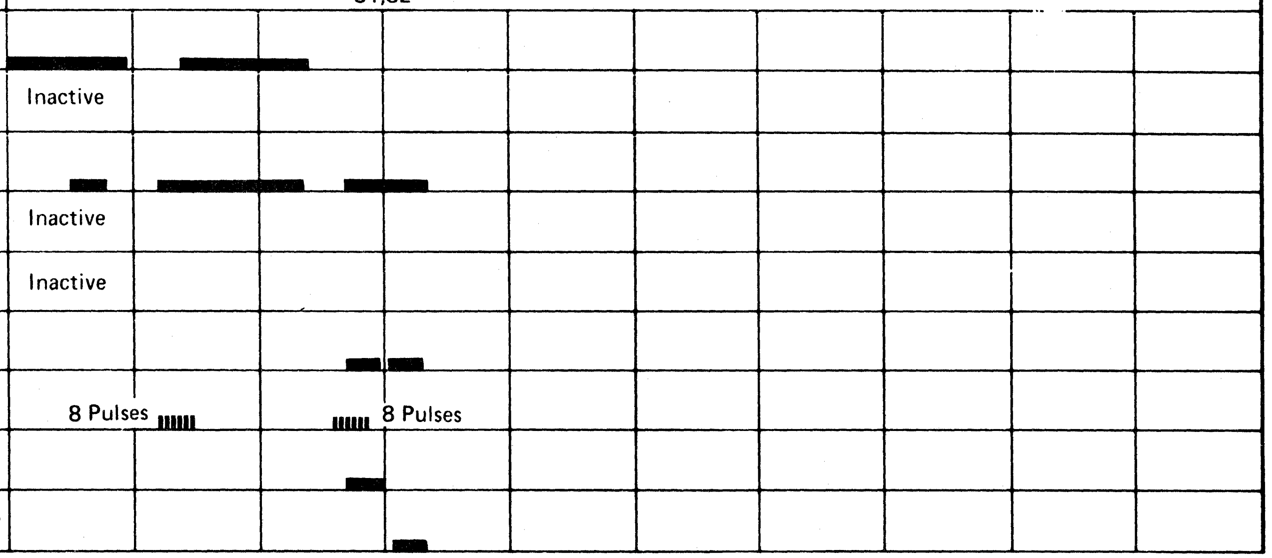
Ch 1 A2Q2D02
−G3
Volts/div 0.1
Probe x10
Ch 2 (see chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B time/div – 5 ms/div
Slope (–)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 9.5
Source – Int Ch 1

DATA 370 A

Legend: ☐ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 81,82
1	−G3	BH110	A2Q2 D02	B	
2	+G1	BH120	A2Q2 J09	C	Inactive
3	+Clock G3 TP	BK200	A2N2 D09	F	
4	−Write TR	BK100	A2N2 D12	G	Inactive
5	+Update G3	BK210	A2N2 G05	E	Inactive
6	−Status Bytes Op 04	BB150	A2R4 D05	K	
7	−CT 17	BG130	A2P2 P12	D	8 Pulses 8 Pulses
8	−Bus Out Bit 2	BB170	A2R4 B12	H	
9	−Bus Out Bit 4	BB170	A2R4 D12	J	



Line keys reference the diagram on DATA 362.

CE0660 Seq. 2 of 2	2358827 Part No.	441303 30 Jul 76	

TRACK OVERRUN

ERROR DESCRIPTION

The Track Used Counter accumulates the number of 3330-1 Compatibility Mode bytes that has been used on the track. This byte count is written on the track following each Count field.

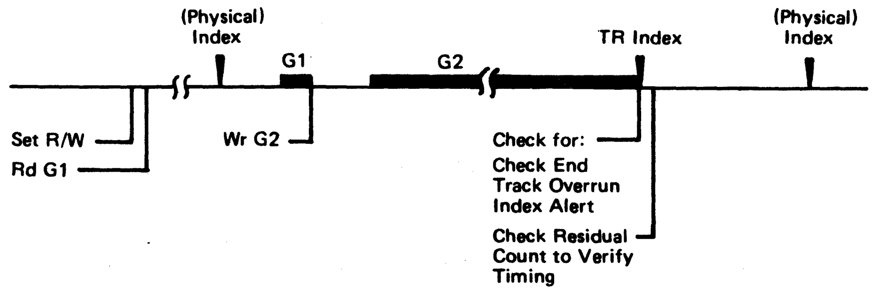
During Search/Read operations, the Track Used count is read from the Count field and used to prime the Track Used Counter.

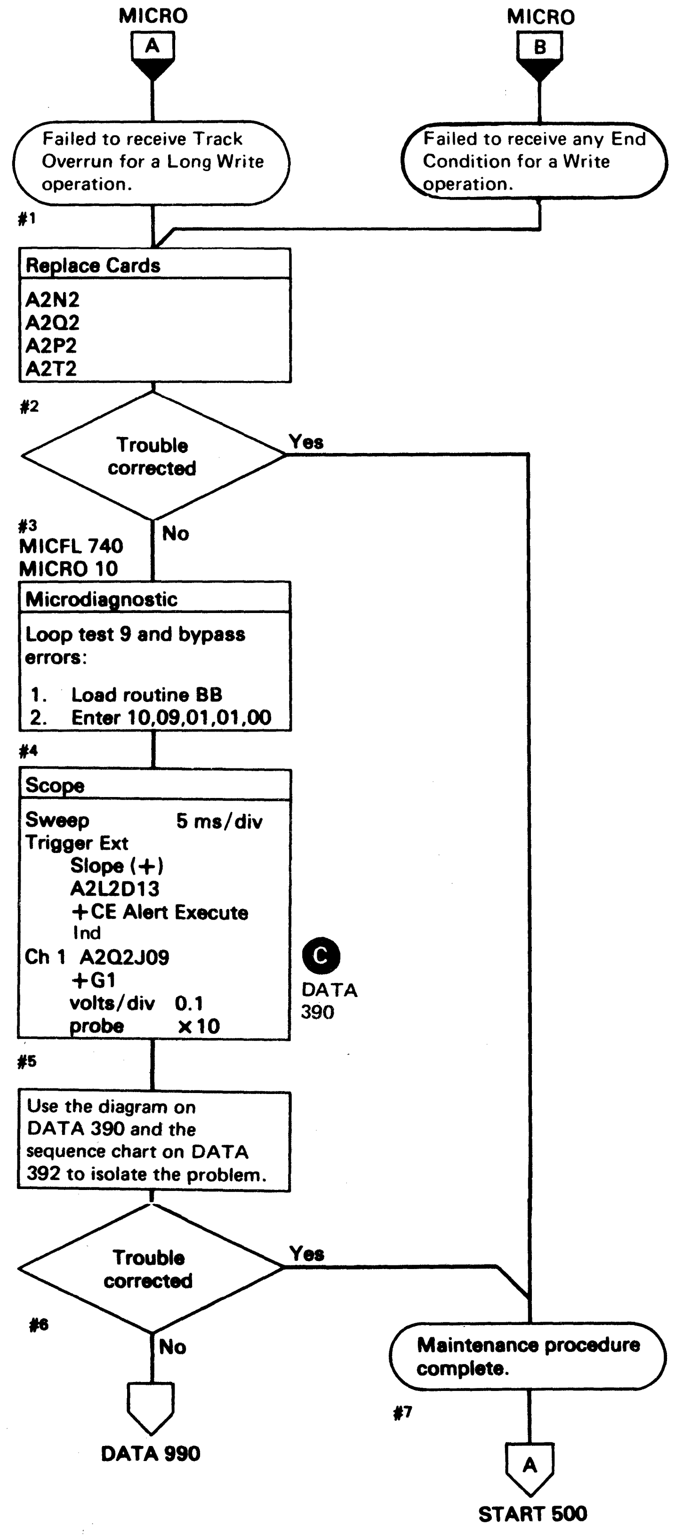
When the Track Used Counter reaches its limit, the TR Index line indicates that the 3330 track capacity has been exceeded. If the limit is reached while in Write mode, a Check End with Track Overrun is posted to the storage control.

This test writes a long record and determines if Track Overrun occurs at the correct time.

MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 9 forces the Track Used Counter to count a maximum number of bytes during a Write operation. The test orients on a Read G1 and then performs a Write G2 using a byte count that exceeds the track capacity 3330-1 Compatibility Mode. The test checks that Check End, Track Overrun, and Index Alert are produced at the proper time.





CE0665 Seq. 1 of 2	2358828 Part No.	441303 30 Jul 76				

NO CHECK END FOR A LONG WRITE OPERATION

ERROR DESCRIPTION

The Track Used Counter accumulates the number of 3330-1 Compatibility Mode bytes that has been used on the track. This byte count is written on the track following each Count field.

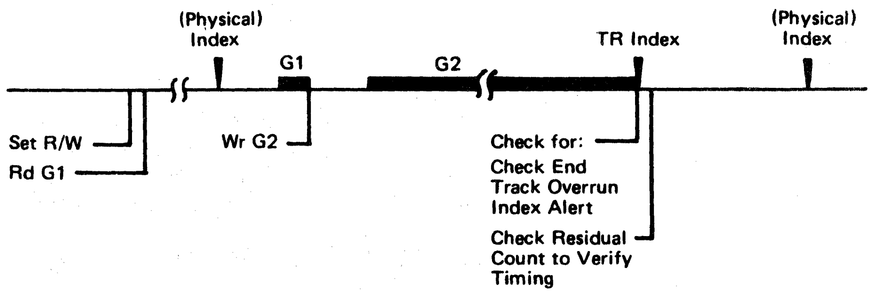
During Search/Read operations, the Track Used count is read from the Count field and used to prime the Track Used Counter.

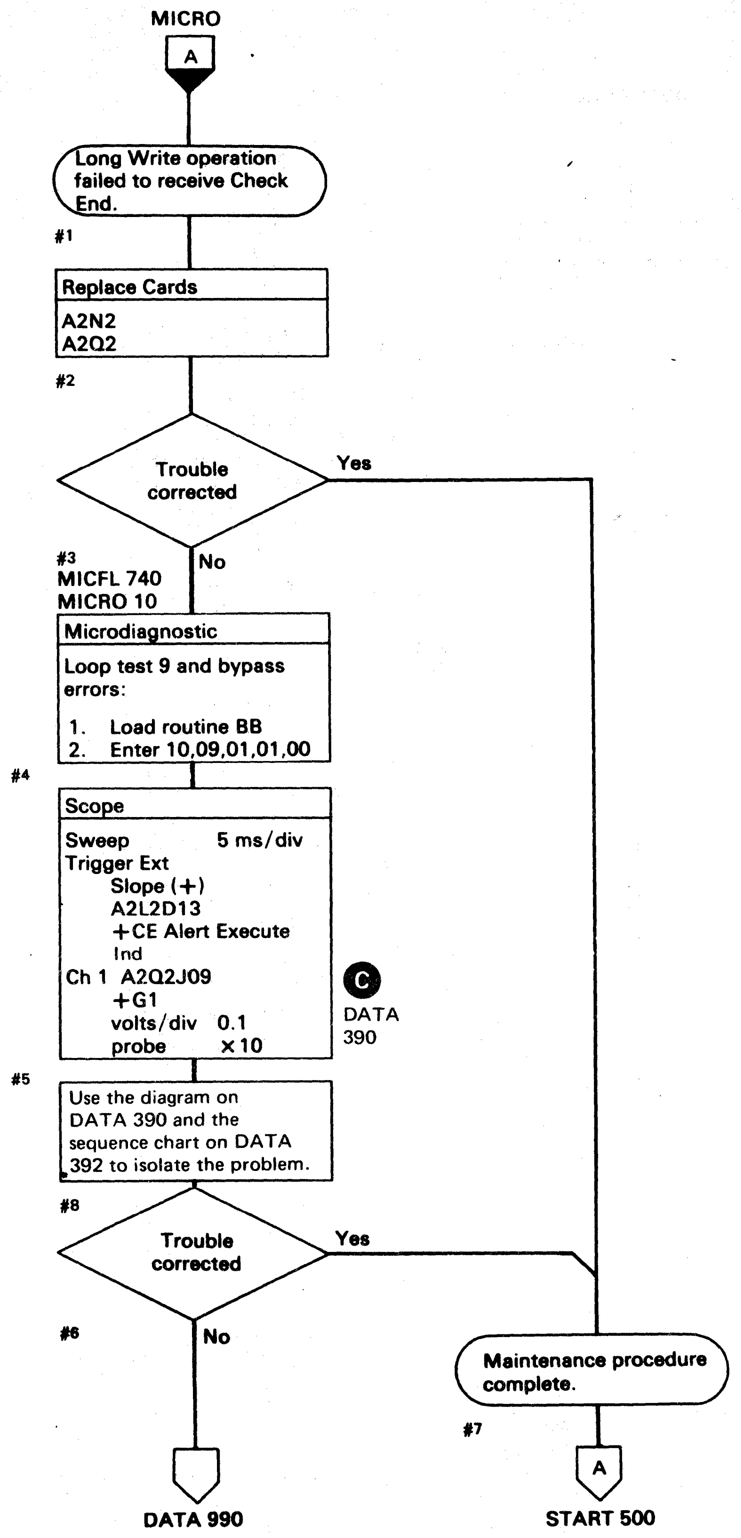
When the Track Used Counter reaches its limit, the TR Index line indicates that the 3330 track capacity has been exceeded. If the limit is reached while in Write mode, a Check End with Track Overrun is posted to the storage control.

This test writes a long record and determines if Check End occurs at the correct time.

MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 9 forces the Track Used Counter to count a maximum number of bytes during a Write operation. The test orients on a Read G1 and then performs a Write G2 using a byte count that exceeds the track capacity in 3330-1 Compatibility Mode. The test checks that Check End, Track Overrun, and Index Alert are produced at the proper time.





NO INDEX IN 3330 MODE

ERROR DESCRIPTION

The Track Used Counter accumulates the number of 3330-1 Compatibility Mode bytes that has been used on the track. This byte count is written on the track following each Count field.

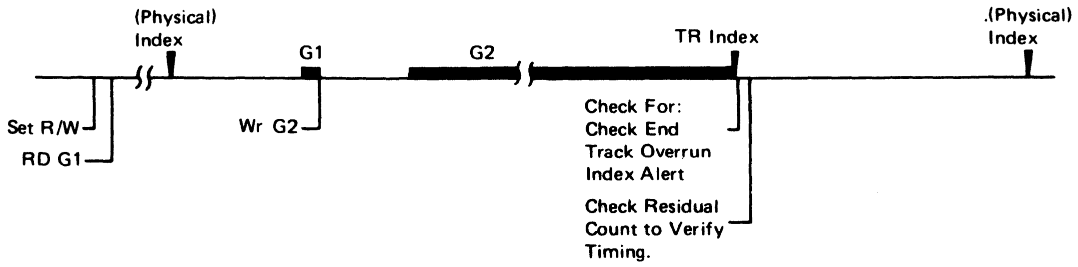
During Search/Read operations, the Track Used count is read from the Count field and used to prime the Track Used Counter.

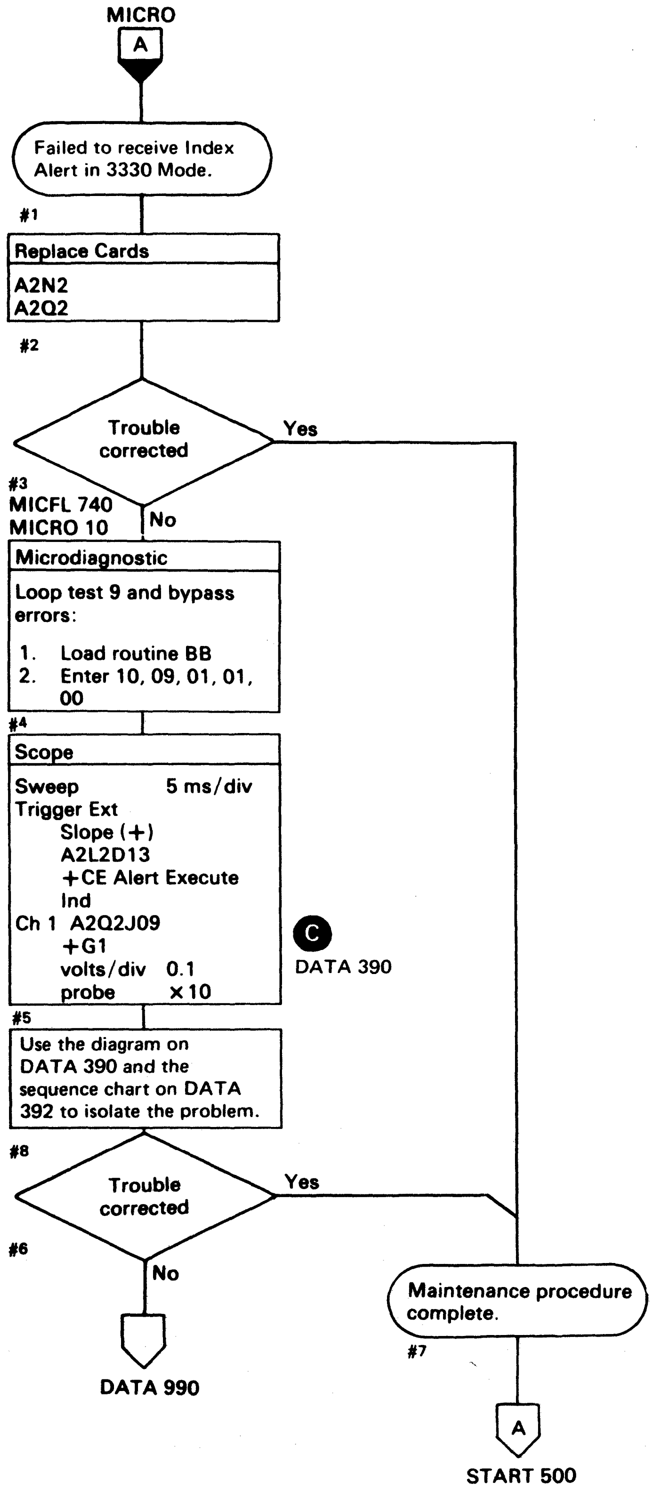
When the Track Used Counter reaches its limit, the TR Index line indicates that the 3330 track capacity has been exceeded. If the limit is reached while in Write mode, a Check End with Track Overrun is posted to the storage control.

This test writes a long record and determines if an Index Alert occurs at the correct time in 3330-1 Compatibility Mode.

MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 9 forces the Track Used Counter to count a maximum number of bytes during a Write operation. The test orients on a Read G1, then performs a Write G2 using a byte count that exceeds the track capacity in 3330-1 Compatibility Mode. The test verifies that Check End, Track Overrun, and Index Alert are produced at the proper time.





TRACK USED COUNTER OUT OF TOLERANCE

ERROR DESCRIPTION

The Track Used Counter accumulates the number of 3330-1 Compatibility Mode bytes that has been used on the track. This byte count is written on the track following each Count field.

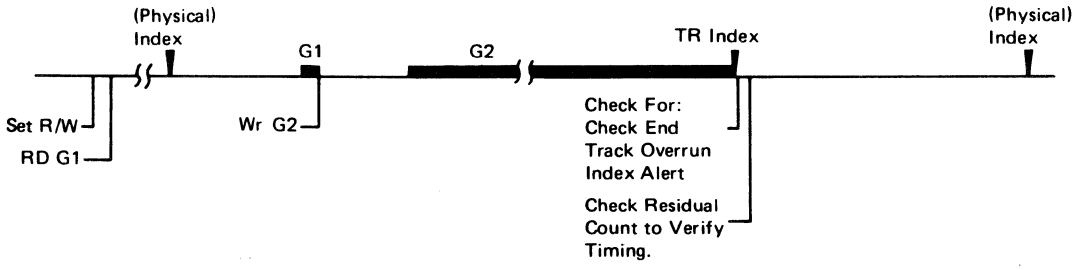
During Search/Read operations, the Track Used count is read from the Count field and used to prime the Track Used Counter.

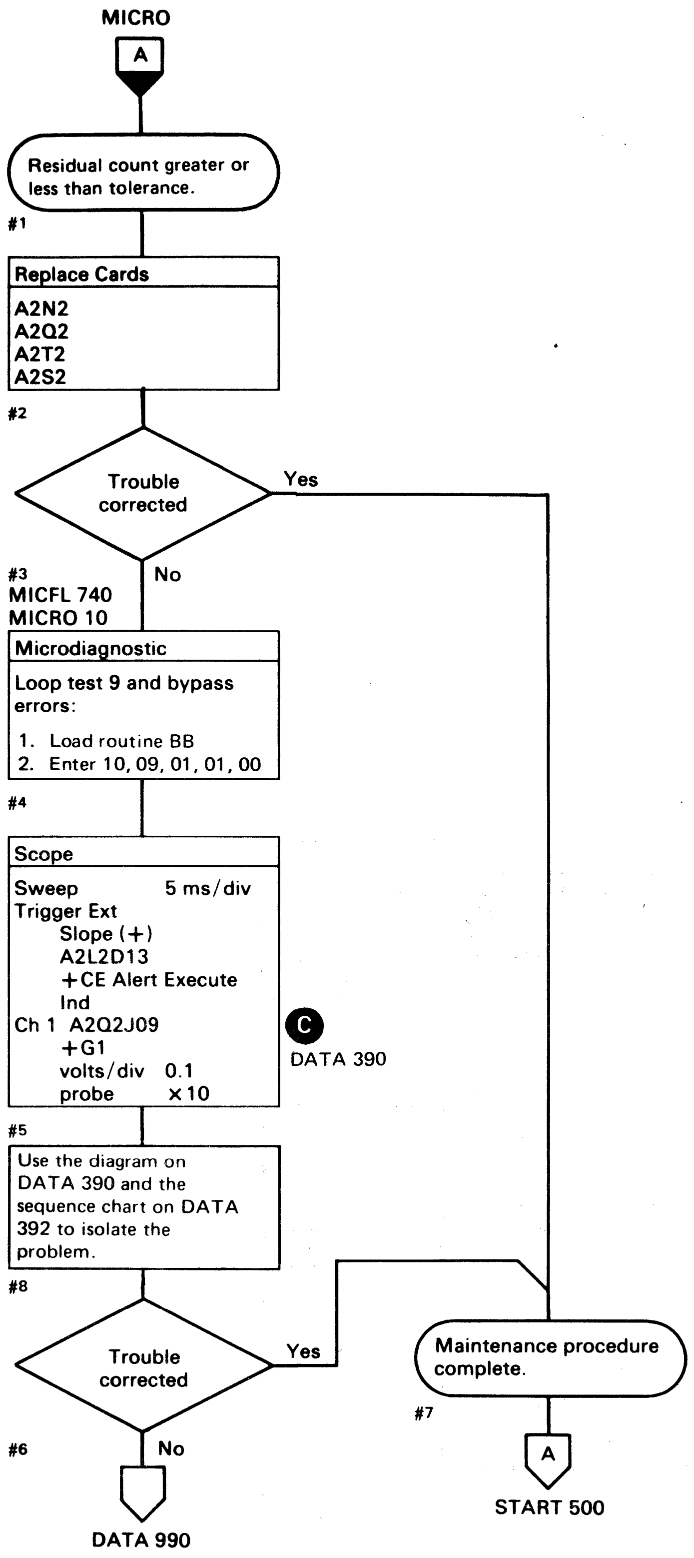
When the Track Used Counter reaches its limit, the TR Index line indicates that the 3330 track capacity has been exceeded. If the limit is reached while in Write mode, a Check End with Track Overrun is posted to the storage control.

This test attempts to write a record of 13,300 bytes and then examines the count after the Write operation has been terminated (end of the logical track). If the count is out of tolerance, an error is indicated.

MICRODIAGNOSTIC DESCRIPTION

Routine BB, test 9 forces the Track Used Counter to count a maximum number of bytes during a Write operation. The test orients on a Read G1, then performs a Write G2 using a byte count that exceeds the track capacity in 3330-1 Compatibility Mode. The test verifies that Check End, Track Overrun, and Index Alert are produced at the proper time.

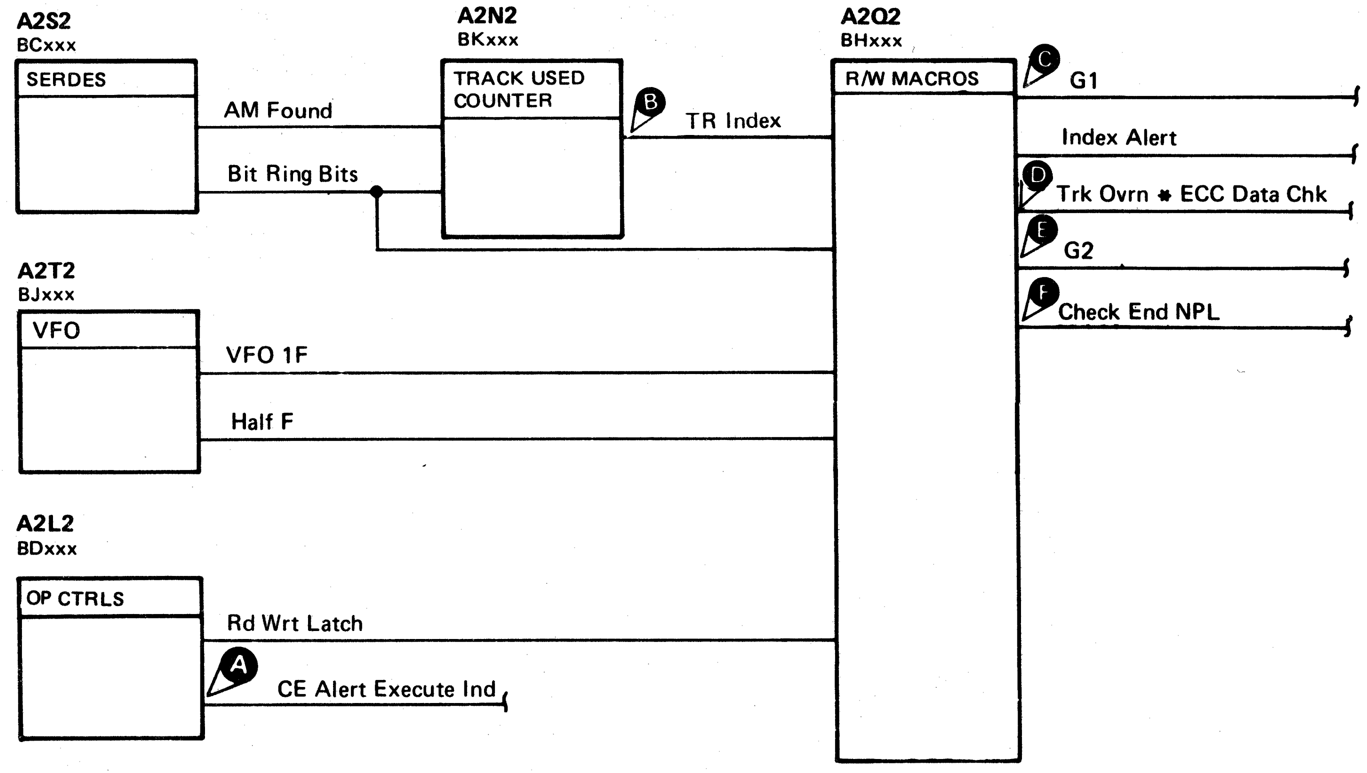




CE0675 Seq. 1 of 2	2358830 Part No.	441303 30 Jul 76				

BB TEST 9 DIAGRAM

See the sequence chart on DATA 392 for referenced test points.
See OPER 42 for theory.



3350	CE0675 Seq. 2 of 2	2358830 Part No.	441303 30 Jul 76				

BB TEST 9 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine BB, test 9
1. Load BB
2. Enter 10, 09, 00, 00

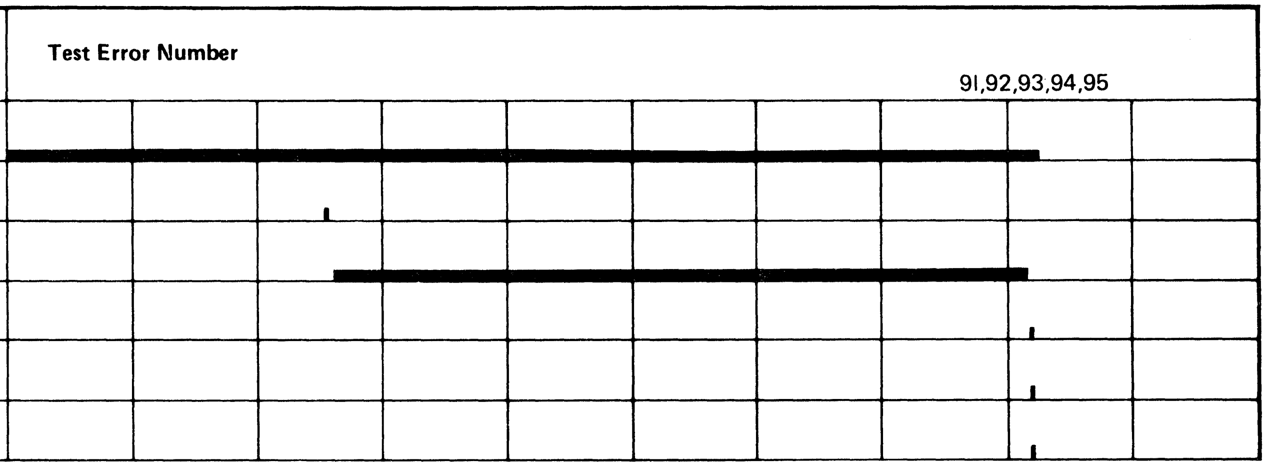
Scope Setup

Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

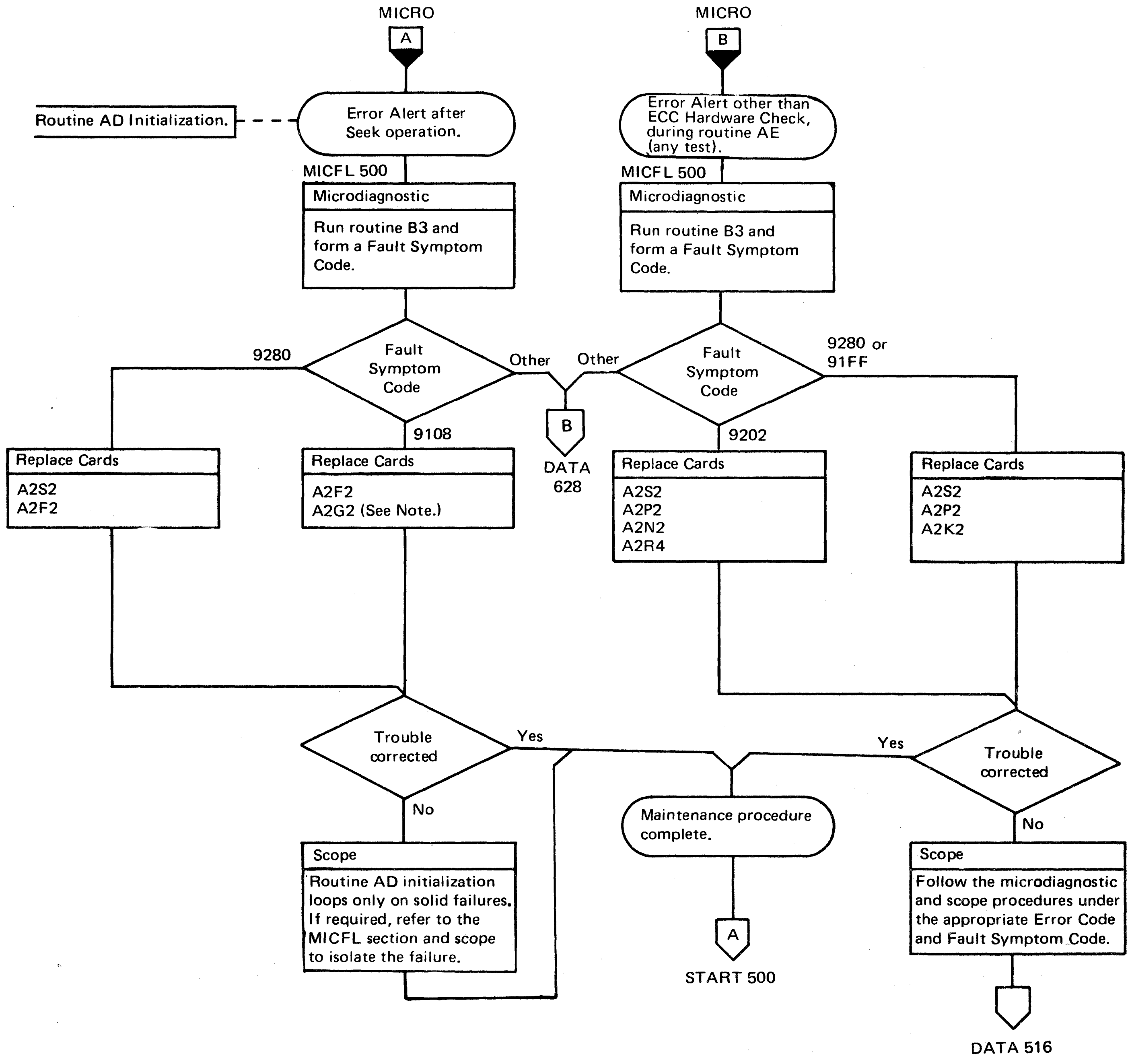
Ch 1 A2U4D13
+CE Alert Execute Ind
Volts/div 0.1
Probe x10
Ch 2 (see chart)

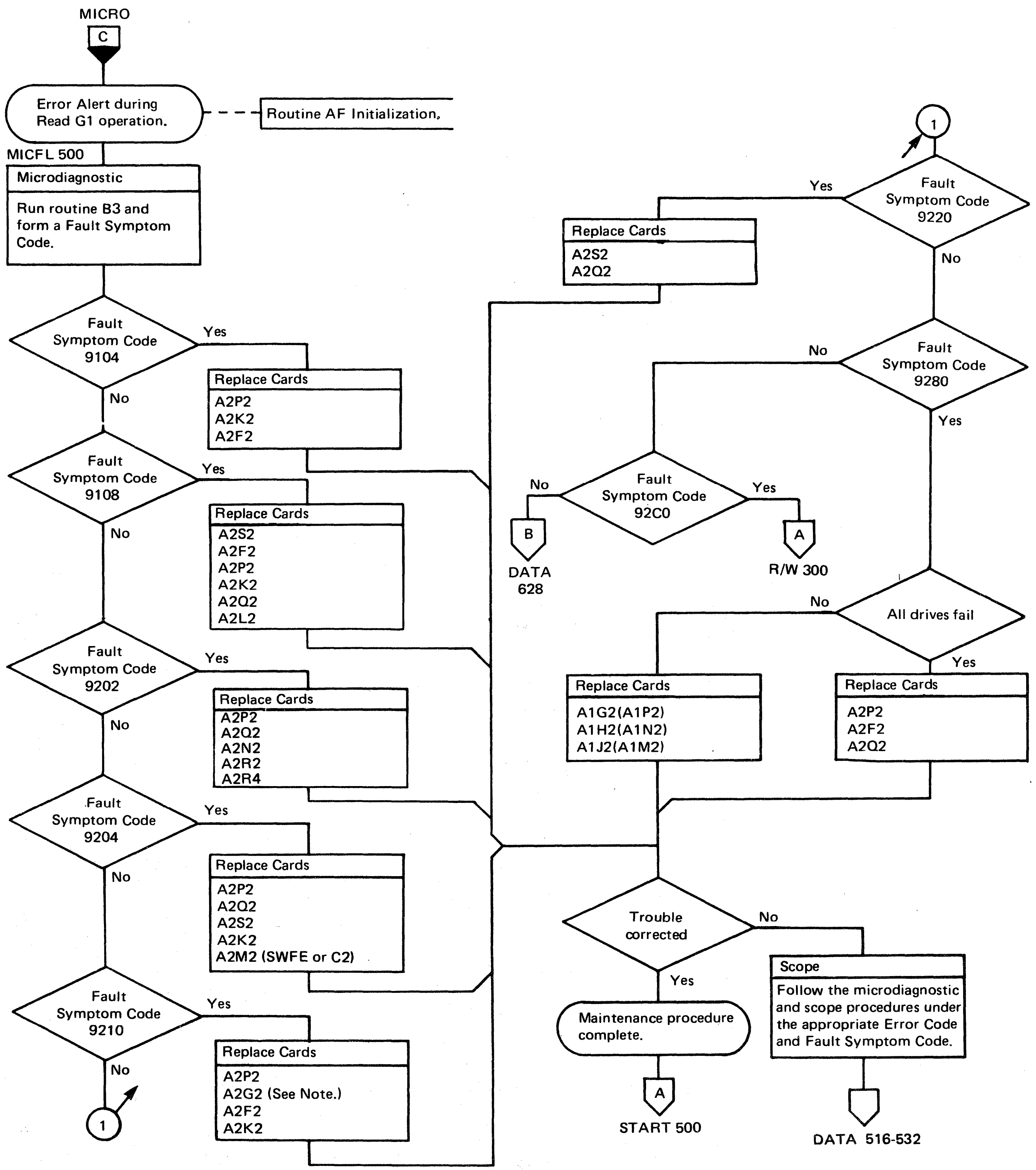
Legend: ☐ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	Ⓐ
2	+G1	BH120	A2Q2 J09	Ⓒ
3	−G2	BH110	A2Q2 D05	Ⓔ
4	+Check End NPL	BE160	A2K2 D05	Ⓕ
5	−TR Index	BK210	A2N2 J10	Ⓑ
6	−Track Ovrn*ECC Data Chk	BH140	A2Q2 J05	Ⓓ



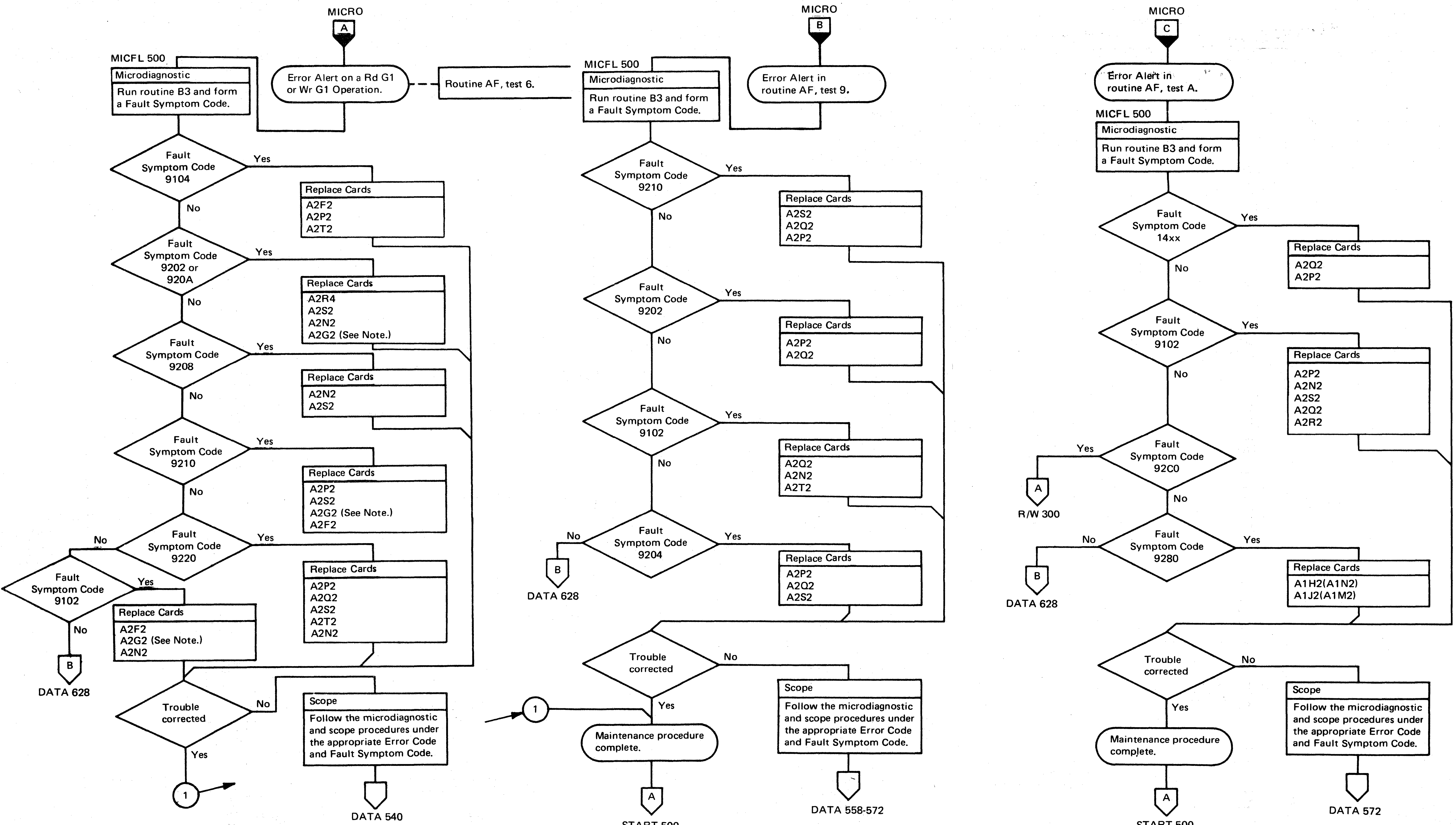
Line keys reference the diagram on DATA 390.





Note: *When replacing A2G2, check the addressing jumpers. See INST 6.*

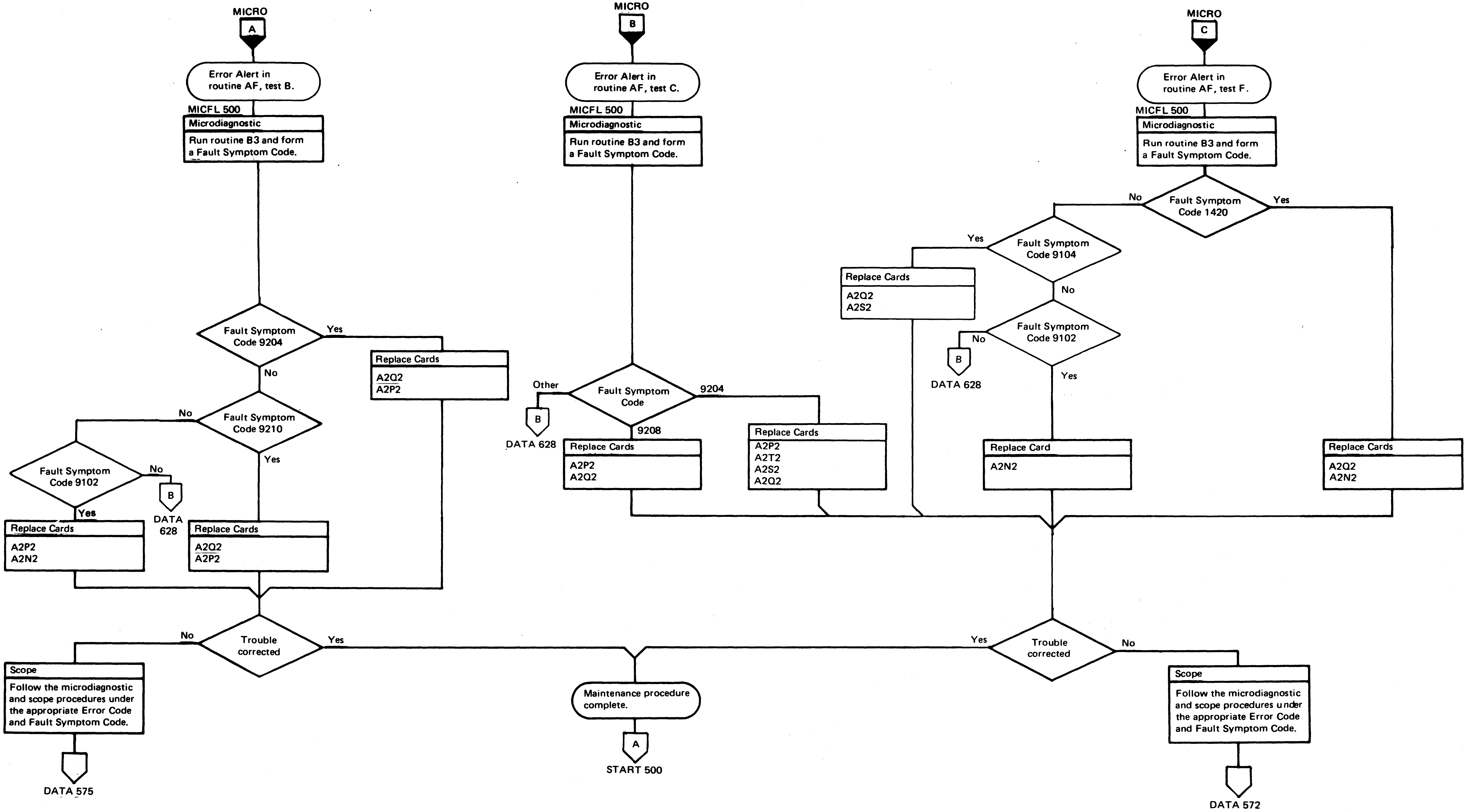
3350	CE0900 Side 1 of 2	2358608 Part No.	441300 31 Mar 76	441301 1 Jun 76	441303 30 Jul 76	441308 18 Aug 78



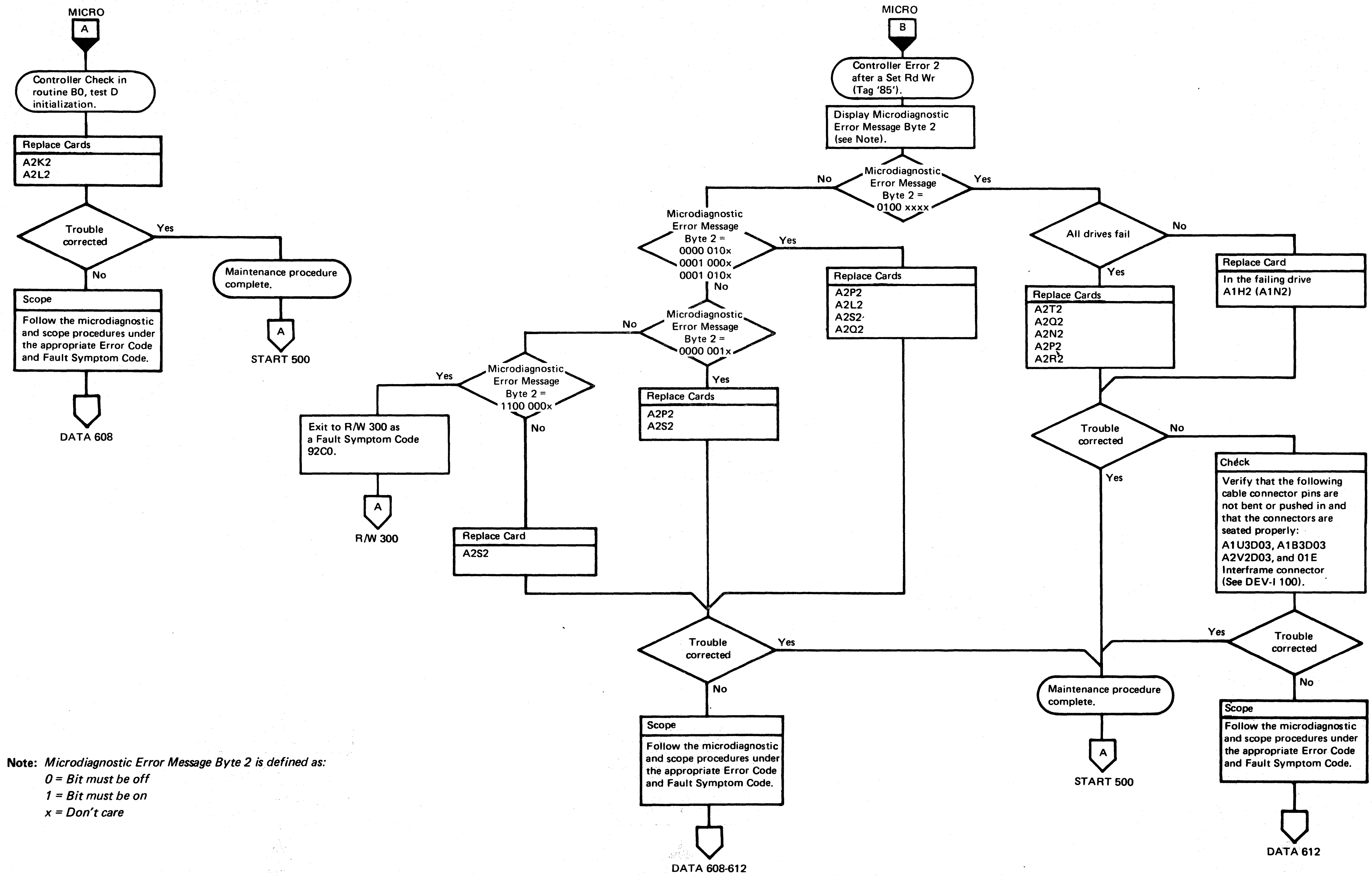
Note: *When replacing A2G2, check the addressing jumpers. See INST 6.*

CE0900 Seq. 2 of 2	2358608 Part No.	441300 31 Mar 76	441301 1 Jun 76	441303 30 Jul 76	441308 18 Aug 78	

ERROR ALERT 3 DATA



3350	CE0910 Side 1 of 2	2358609 Part No.	441300 31 Mar 76	441303 30 Jul 76			

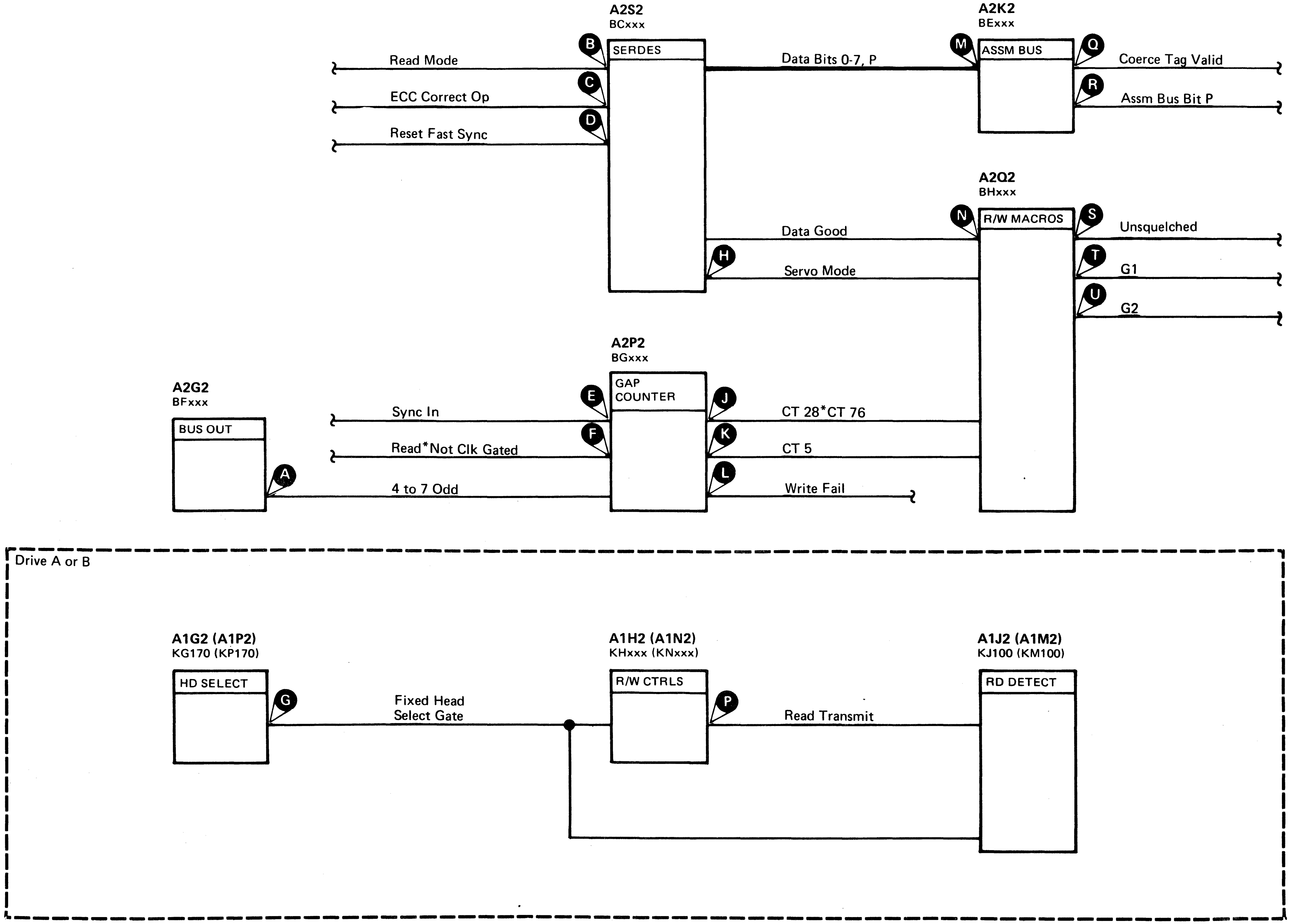


Note: *Microdiagnostic Error Message Byte 2 is defined as:*

0 = Bit must be off
1 = Bit must be on
x = Don't care

AE TEST 1 DIAGRAM

See the sequence charts on DATA 520 through 532 for referenced test points.



CE0925 Seq. 1 of 2	2358610 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AEF9 ERROR CODE WITH FAULT SYMPTOM CODE 9280

Microdiagnostic Setup

Loop routine AE, test 1.

1. Load routine AE.
2. Enter 10, 01, 02, 01, 00.

See DATA 122 for a description of routine AE, test 1.

Scope Setup *(See DATA 154 for additional information.)*

Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 A2S2M12
+Reset Fast Sync
Volts/div 0.1
Probe x10

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 2 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

AEF9 ERROR CODE WITH FAULT SYMPTOM CODE 91FF

Microdiagnostic Setup

Loop routine AE, test 4.

1. Load routine AE.
2. Enter 10, 04, 02, 01, 00.

See DATA 176 for a description of routine AE, test 4.

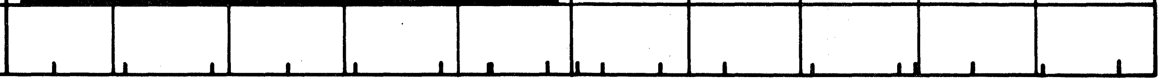
Scope Setup *(See DATA 182 for additional information.)*

Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (-)
A2L2J11
–MST RAS TP

Ch 1 A2S2S02
–ECC Correct Op
Volts/div 0.1
Probe x10
Ch 2 A2Q2D05
–G2
Volts/div 0.1
Probe x10

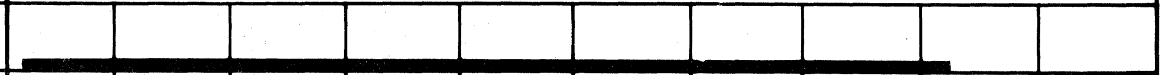
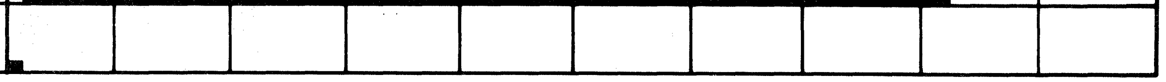
Legend:
▭ Inactive
■ Active level
▨ Tolerance

For Fault Symptom Code 9280

Chart Line No.	Line Name	ALD	Test Point		
1	+G1	BH120	A2Q2 J09	Ⓣ	
2	+Reset Fast Sync	BC140	A2S2 M12	Ⓓ	

Line keys reference the diagram on DATA 516.

For Fault Symptom Code 91FF

Chart Line No.	Line Name	ALD	Test Point		
1	–ECC Correct Op	BC100	A2S2 S02	Ⓒ	
2	–G2	BH110	A2Q2 D05	Ⓤ	

Line keys reference the diagram on DATA 516.

CE0925 Seq. 2 of 2	2358610 Part No.	441300 31 Mar 76	441303 30 Jul 76			

ERROR ALERT

AF1A ERROR CODE WITH FAULT SYMPTOM CODE 9104

Microdiagnostic Setup

Loop routine AF, test 1.

1. Load routine AF.
2. Enter 10, 01, 00, 01, 00.

See DATA 218 for a description of routine AF, test 1.

Scope Setup *(See DATA 222 for additional information.)*

Sweep	20 µs/div	Ch 1 A2Q2J09 +G1	
Mode	Alt or Chop	Volts/div	0.1
Trigger	Ext Slope (–) A2L2J11 –MST RAS TP	Probe	x10
		Ch 2 (see chart)	

AF1A ERROR CODE WITH FAULT SYMPTOM CODE 9108

Microdiagnostic Setup

Loop routine AF, test 1.

1. Load routine AF.
2. Enter 10, 01, 00, 01, 00.

See DATA 218 for a description of routine AF, test 1.

Scope Setup *(See DATA 222 for additional information.)*

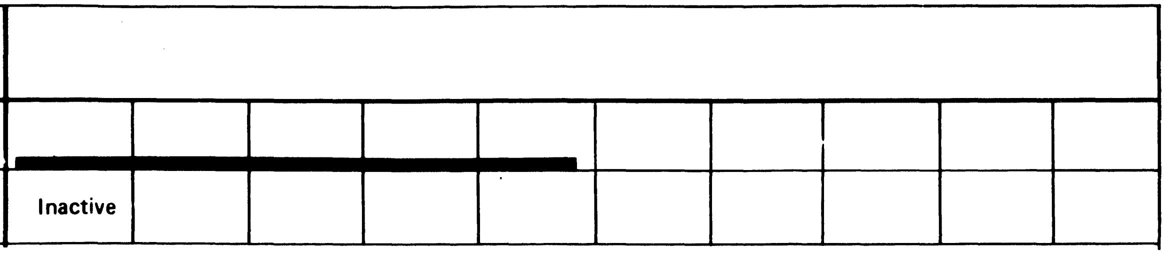
Sweep	20 µs/div	Ch 1 A2Q2J09 +G1	
Mode	Alt or Chop	Volts/div	0.1
Trigger	Ext Slope (–) A2L2J11 –MST RAS TP	Probe	x10
		Ch 2 (see chart)	

Legend:

☐	Inactive
■	Active level
▨	Tolerance

For Fault Symptom Code 9104

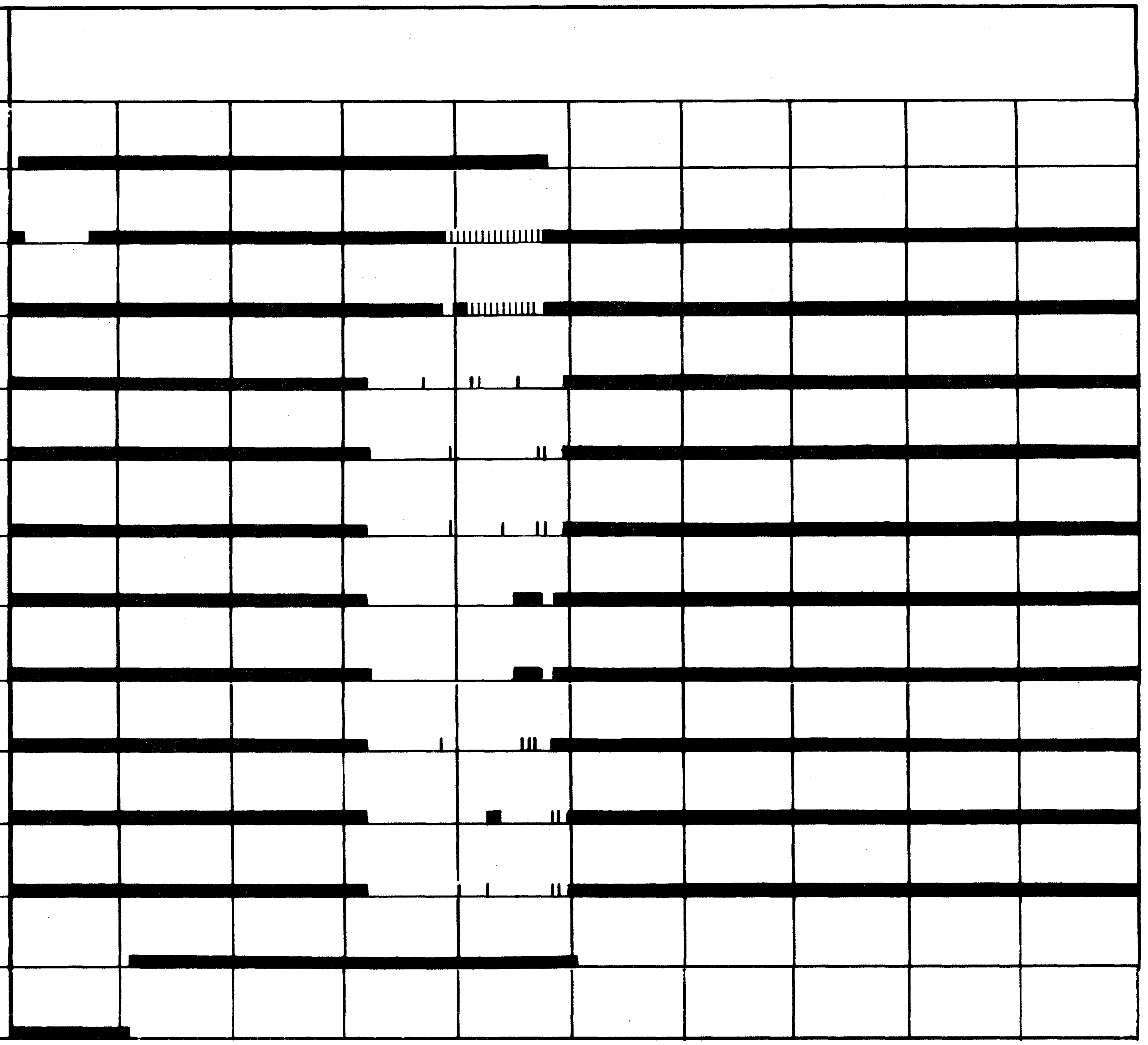
Chart Line No.	Line Name	ALD	Test Point	
1	+G1	BH120	A2Q2 J09	Ⓣ
2	+Write Fail	BG150	A2P2 P02	Ⓛ



Line keys reference the diagram on DATA 516.

For Fault Symptom Code 9108

Chart Line No.	Line Name	ALD	Test Point	
1	+G1	BH120	A2Q2 J09	Ⓣ
2	–Assm Bus Bit P	BE110	A2K2 G07	Ⓡ
3	–Data Bit P	BE110	A2K2 J07	Ⓜ
4	–Data Bit 6	BE110	A2K2 M10	
5	–Data Bit 4	BE110	A2K2 P02	
6	–Data Bit 5	BE110	A2K2 P04	
7	–Data Bit 0	BE110	A2K2 P07	
8	–Data Bit 1	BE110	A2K2 P09	
9	–Data Bit 7	BE110	A2K2 P13	
10	–Data Bit 2	BE110	A2K2 S10	
11	–Data Bit 3	BE110	A2K2 U12	
12	–Read•Not Clk Gated	BG140	A2P2 D02	Ⓕ
13	–Coerce Tag Valid	BE150	A2K2 B10	Ⓠ



Line keys reference the diagram on DATA 516.

AF1A ERROR CODE WITH FAULT SYMPTOM CODE 9202

Microdiagnostic Setup

Loop routine AF, test 1.

1. Load routine AF.
2. Enter 10, 01, 00, 01, 00.

See DATA 218 for a description of routine AF, test 1.

Scope Setup *(See DATA 222 for additional information.)*

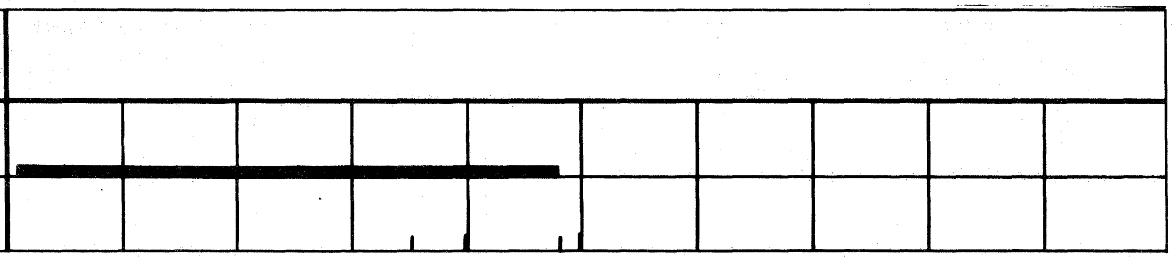
Sweep 20 µs/div
Mode Alt or Chop
Trigger Ext
Slope (-)
A2L2J11
–MST RAS TP

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 A2P2B07
–CT5
Volts/div 0.1
Probe x10

For Fault Symptom Code 9202

Legend: ▭ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+G1	BH120	A2Q2 J09	T
2	–CT 5	BG120	A2P2 B07	K



Line keys reference the diagram on DATA 516.

AF1A ERROR CODE WITH FAULT SYMPTOM CODE 9204

Microdiagnostic Setup

Loop routine AF, test 1.

1. Load routine AF.
2. Enter 10, 01, 00, 01, 00.

See DATA 218 for a description of routine AF, test 1.

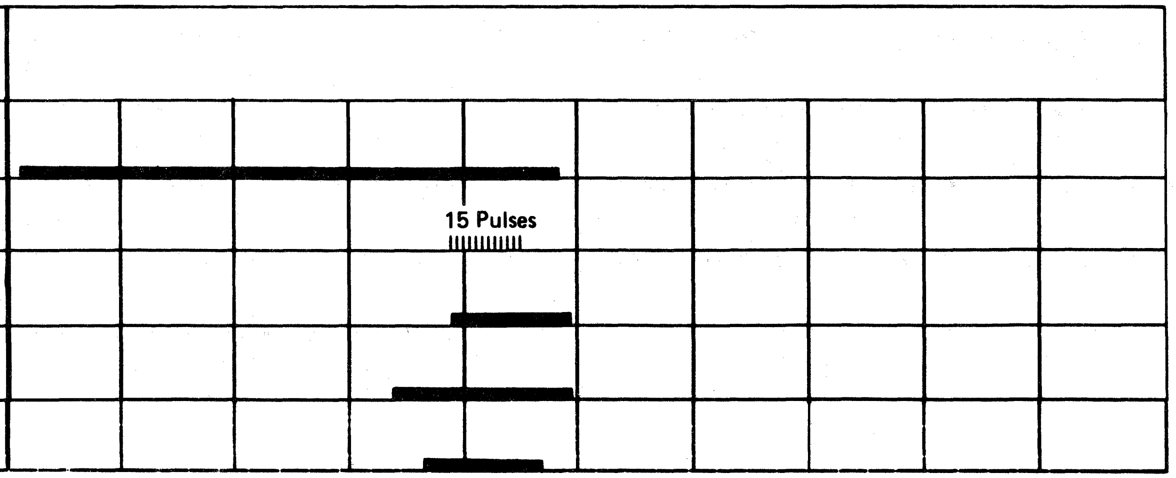
Scope Setup *(See DATA 222 for additional information.)*

Sweep 20 µs/div
Mode Alt or Chop
Trigger Ext
Slope (-)
A2L2J11
–MST RAS TP

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (see chart)

For Fault Symptom Code 9204

Chart Line No.	Line Name	ALD	Test Point	
1	+G1	BH120	A2Q2 J09	T
2	–Sync In	BG140	A2P2 G13	E
3	–Data Good	BH160	A2Q2 G11	N
4	+Servo Mode	BC140	A2S2 G10	H
5	+Read Mode	BC170	A2S2 G13	B



Line keys reference the diagram on DATA 516.

ERROR ALERT

AF1A ERROR CODE WITH FAULT SYMPTOM CODE 9210

Microdiagnostic Setup

Loop routine AF, test 1.
1. Load routine AF.
2. Enter 10, 01, 00, 01, 00.

See DATA 218 for a description of routine AF, test 1.

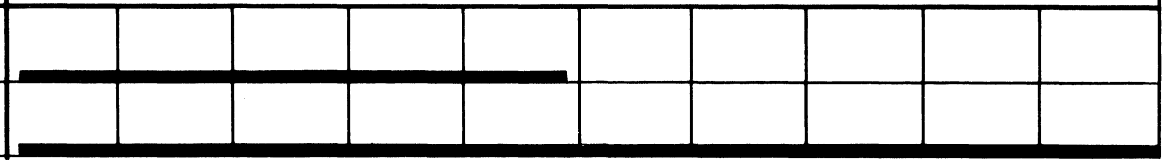
Scope Setup *(See DATA 222 for additional information.)*

Sweep	20 μs/div	Ch 1 A2Q2J09		
Mode	Alt or Chop		+G1	
Trigger	Ext	Volts/div		0.1
	Slope (-)	Probe		x10
	A2L2J11	Ch 2 A2G2P07		
	–MST RAS TP		–4 to 7 Odd	
		Volts/div		0.1
		Probe		x10

For Fault Symptom Code 9210

Legend: ▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+G1	BH120	A2Q2 J09	Ⓣ
2	–4 to 7 Odd	BF200	A2G2 P07	Ⓐ



Line keys reference the diagram on DATA 516.

AF1A ERROR CODE WITH FAULT SYMPTOM CODE 9280

Microdiagnostic Setup

Loop routine AF, test 1.
1. Load routine AF.
2. Enter 10, 01, 00, 01, 00.

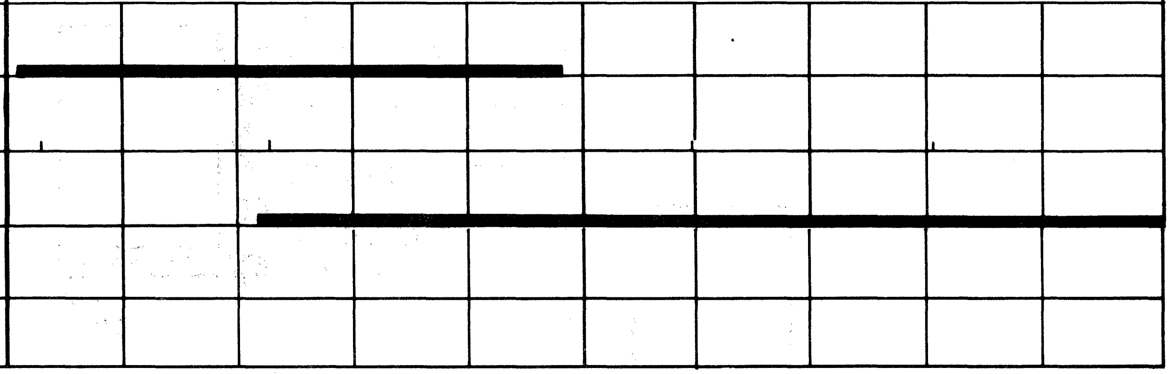
See DATA 218 for a description of routine AF, test 1.

Scope Setup *(See DATA 222 for additional information.)*

Sweep	20 μs/div	Ch 1 A2Q2J09		
Mode	Alt or Chop		+G1	
Trigger	Ext	Volts/div		0.1
	Slope (-)	Probe		x10
	A2L2J11	Ch 2 (see chart)		
	–MST RAS TP			

For Fault Symptom Code 9280

Chart Line No.	Line Name	ALD	Test Point	
1	+G1	BH120	A2Q2 J09	Ⓣ
2	–CT 28*CT 76	BG130	A2P2 S02	Ⓙ
3	–Unsquelched	BH140	A2Q2 M09	Ⓢ
4	+Fixed Hd Sel Gate	KG170 (KP170)	A1G2 (A2P2) P10	Ⓖ
5	–Read Transmit	KH170(KN170)	A1H2 (A1N2) V04	Ⓟ



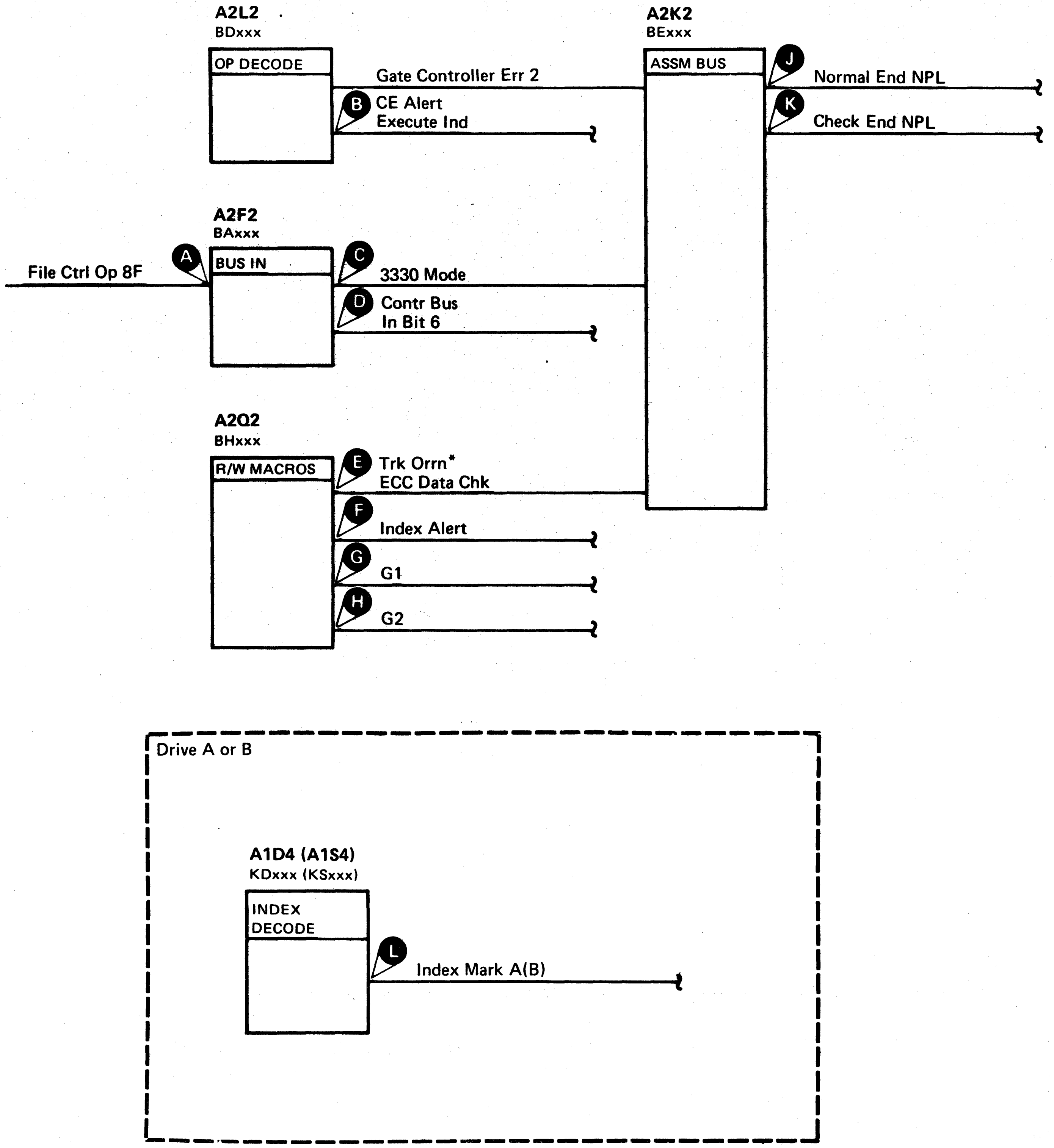
Line keys reference the diagram on DATA 516.

CE0939 Seq. 1 of 2	2358612 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST 6 DIAGRAM

See the sequence charts on DATA 546 and DATA 550 for referenced test points.

See OPER 240 for theory.



3350

CE0939 Seq. 2 of 2	2358612 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST 6 SEQUENCE CHART

NATIVE MODE

Microdiagnostic Setup

Routine AF, test 6
1. Load AF
2. Enter 10,06,00,00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop

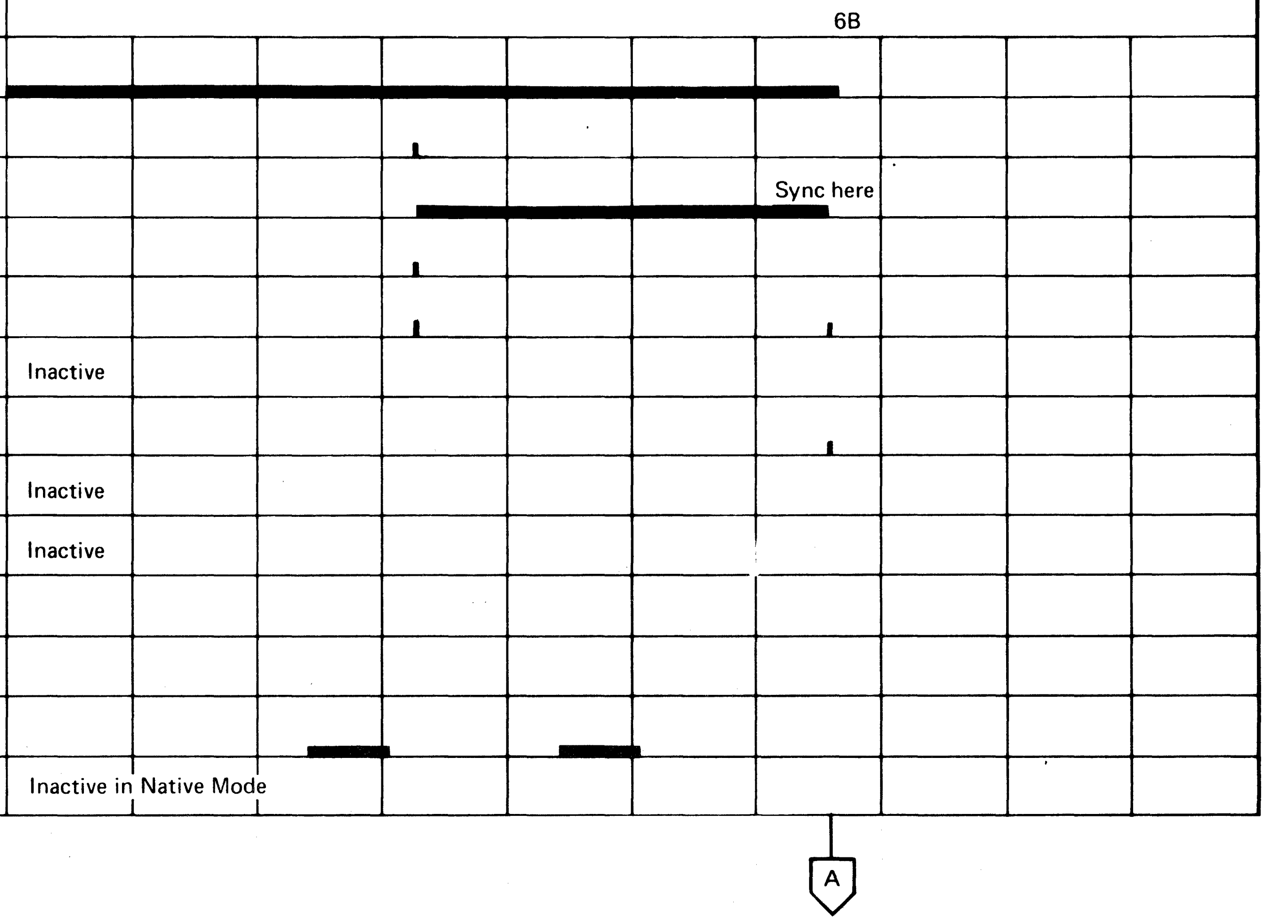
Trigger Ext.
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend: ☐ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+CE Alert Execute Ind	BD210	A2L2 D13	B	
2	+G1	BH120	A2Q2 J09	G	
3	−G2	BH110	A2Q2 D05	H	Sync here
4	−Index Alert	BH170	A2Q2 J11	F	
5	+Normal End NPL	BE160	A2K2 D11	J	
6	−3330 Mode	BA140	A2F2 M04	C	Inactive
7	−Index Mark A(B) TP	KD520 (KS520)	A1D4 G03 (A1S4 G03)	L	
8	+Check End NPL	BE160	A2K2 D05	K	Inactive
9	−Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	E	Inactive
Change A and B Time/Div switch to 20 μsec.					
10	−File Ctrl Op 8F	BA130	A2F2 P13	A	
11	−Contr Bus In Bit 6	BA100	A2F2 P09	D	Inactive in Native Mode



Line keys reference the diagram on DATA 540.

DATA 554
(For expanded sequence chart)

AF TEST 6 SEQUENCE CHART

3330-1 COMPATIBILITY MODE

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop

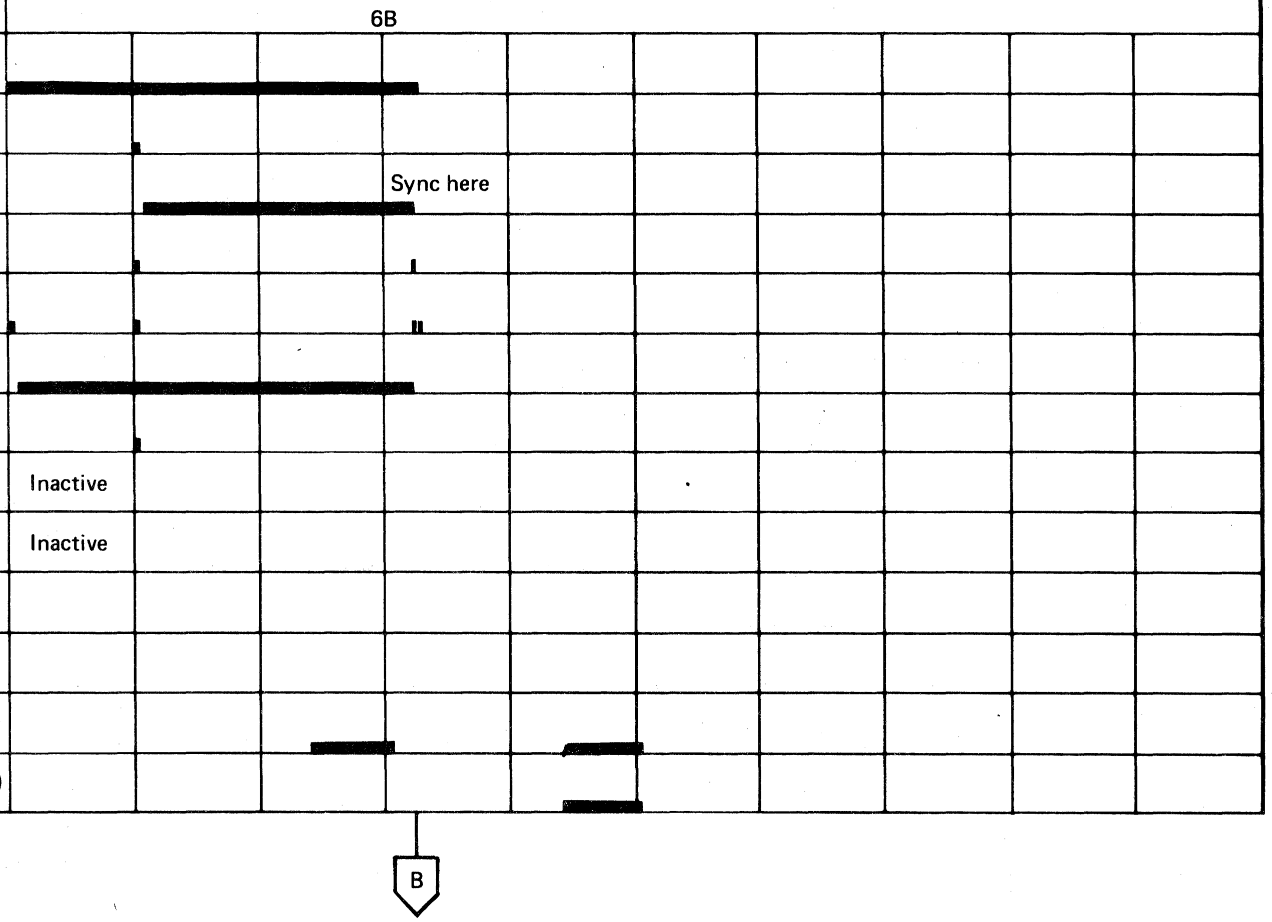
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend:
▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+CE Alert Execute Ind	BD210	A2L2 D13	B	
2	+G1	BH120	A2Q2 J09	G	
3	−G2	BH110	A2Q2 D05	H	Sync here
4	−Index Alert	BH170	A2Q2 J11	F	
5	+Normal End NPL	BE160	A2K2 D11	J	
6	−3330 Mode	BA140	A2F2 M04	C	
7	−Index Mark A(B)	KD520 (KS520)	A1D4 G03 (A1S4 G03)	L	
8	+Check End NPL	BE160	A2K2 D05	K	Inactive
9	−Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	E	Inactive
Change A and B Time/Div switch to 20 μsec.					
10	−File Ctrl Op 8F	BA130	A2F2 P13	A	
11	−Contr Bus In Bit 6	BA100	A2F2 P09	D	



Line keys reference the diagram on DATA 540.

DATA 554
(For expanded sequence chart)

CE0943 Seq. 2 of 2	2358711 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST 6 SEQUENCE CHART

NATIVE MODE

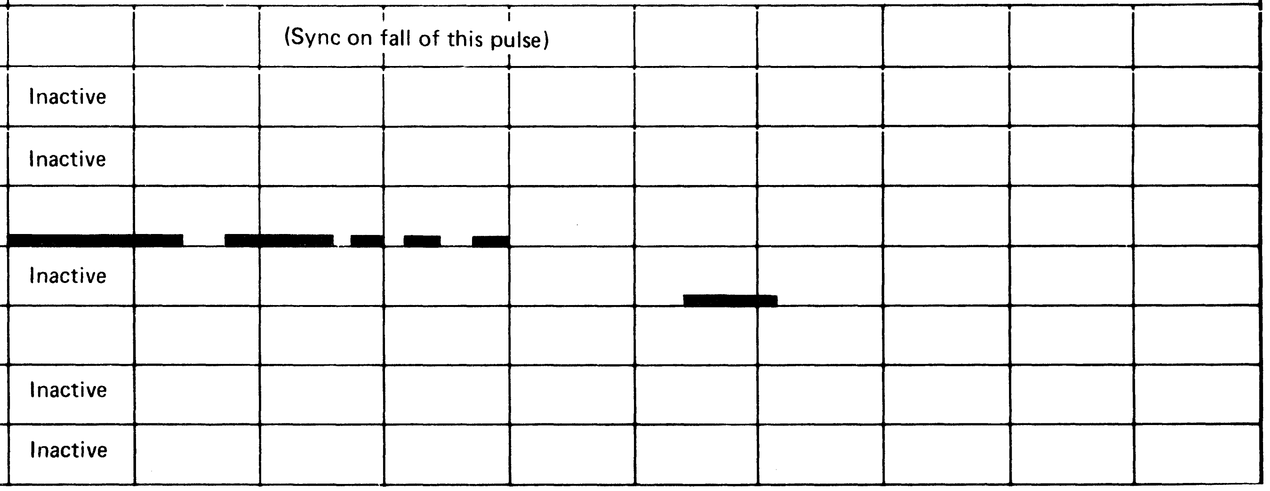
Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Ch 1 A2Q2D05
−G2
Volts/div 0.1
Probe x10
Ch 2 (See chart)
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Legend: ☐ Inactive ■ Active level ▨ Tolerance

DATA 546
A

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 6B
1	−G2	BH110	A2Q2 D05	Ⓗ	(Sync on fall of this pulse)
2	+G1	BH120	A2Q2 J09	Ⓖ	Inactive
3	−Index Alert	BH170	A2Q2 J11	Ⓕ	Inactive
4	+Normal End NPL	BE160	A2K2 D11	Ⓙ	
5	−3330 Mode	BA140	A2F2 M04	Ⓒ	Inactive
6	−Index Mark A(B)TP	KD520 (KS520)	A2D2 G03 (A1S4 G05)	Ⓛ	
7	+Check End NPL	BE160	A2K2 D05	Ⓚ	Inactive
8	−Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	Ⓔ	Inactive



Line keys reference the diagram on DATA 540.

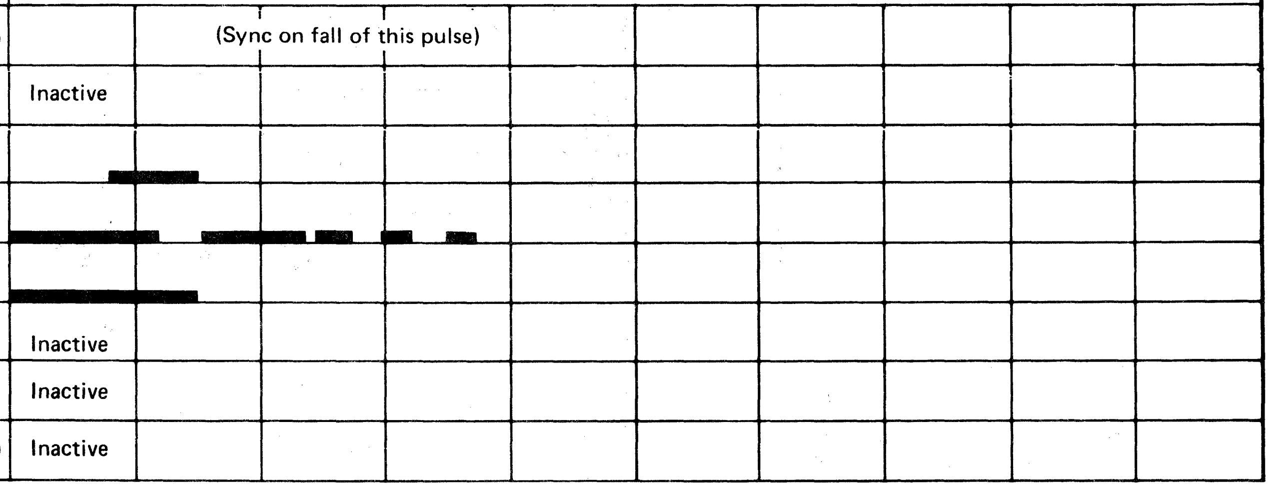
3330-1 COMPATIBILITY MODE

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Ch 1 A2Q2D05
−G2
Volts/div 0.1
Probe x10
Ch 2 (See chart)
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

DATA 550
B

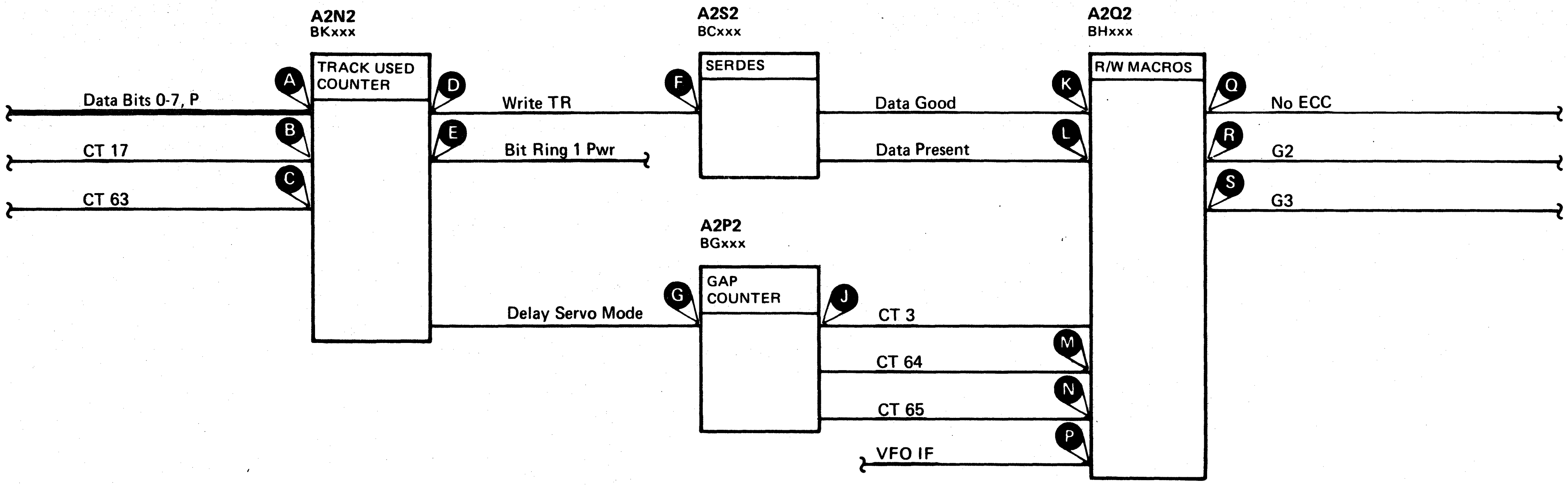
Chart Line No.	Line Name	ALD	Test Point		Test Error Number 6B
1	−G2	BH110	A2Q2 D05	Ⓗ	(Sync on fall of this pulse)
2	+G1	BH120	A2Q2 J09	Ⓖ	Inactive
3	−Index Alert	BH170	A2Q2 J11	Ⓕ	
4	+Normal End NPL	BE160	A2K2 D11	Ⓙ	
5	−3330 Mode	BA140	A2F2 M04	Ⓒ	
6	−Valid Index Mark A(B)TP	KD520 (KS520)	A1D4 G03 (A1S4 G03)	Ⓛ	Inactive
7	+Check End NPL	BE160	A2K2 D05	Ⓚ	Inactive
8	−Trk Ovrn*ECC Data Chk	BH140	A2Q2 J05	Ⓔ	Inactive



Line keys reference the diagram on DATA 540.

AF TEST 8 and A DIAGRAM

See the sequence charts on DATA 560 through 572 for referenced test points.
See OPER 241 for theory.



3350	CE0945 Seq. 2 of 2	2358613 Part No.	441300 31 Mar 76	441303 30 Jul 76			

ERROR ALERT

AF9A ERROR CODE WITH FAULT SYMPTOM CODE 9202

Microdiagnostic Setup

Loop routine AF, test 8 (for 15 seconds only).
1. Load routine AF.
2. Enter 10, 08, 00, 01, 00.

After 15 seconds – continue.

Loop routine AF, test 9.
1. Load routine AF.
2. Enter 10, 09, 00, 01, 00.

See DATA 254 for a description of routine AF, tests 8 and 9.

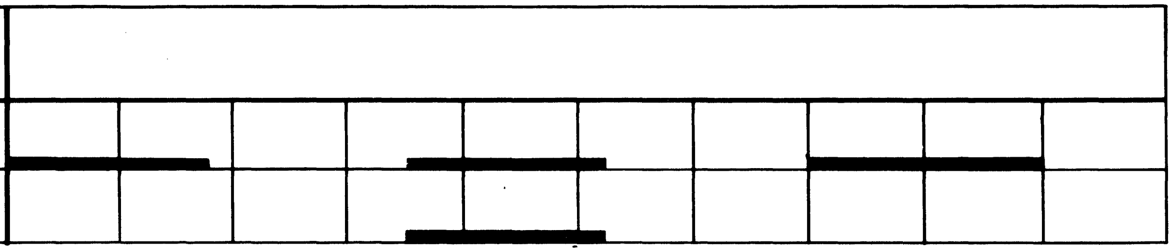
Scope Setup *(See DATA 256 for additional information.)*

Sweep	2 ms/div	Ch 1 A2Q2D05 –G2	
Mode	Alt or Chop	Volts/div	0.1
Trigger	Ext	Probe	x10
	Slope (+)	Ch 2 A2Q2B03 +No ECC	
	A2L2D13	Volts/div	0.1
	+CE Alert Execute Ind	Probe	x10

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 2 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Legend: ▭ **Inactive** ■ **Active level** ▨ **Tolerance**

Chart Line No.	Line Name	ALD	Test Point	
1	–G2	BH110	A2Q2 D05	Ⓡ
2	+No ECC	BH160	A2Q2 B03	Ⓠ



Line keys reference the diagram on DATA 558.

AF9A ERROR CODE WITH FAULT SYMPTOM CODE 9210

Microdiagnostic Setup

Loop routine AF, test 8 (for 15 seconds only).
1. Load routine AF.
2. Enter 10, 08, 00, 01, 00.

After 15 seconds – continue.

Loop routine AF, test 9.
1. Load routine AF.
2. Enter 10, 09, 00, 01, 00.

See DATA 254 for a description of routine AF, tests 8 and 9.

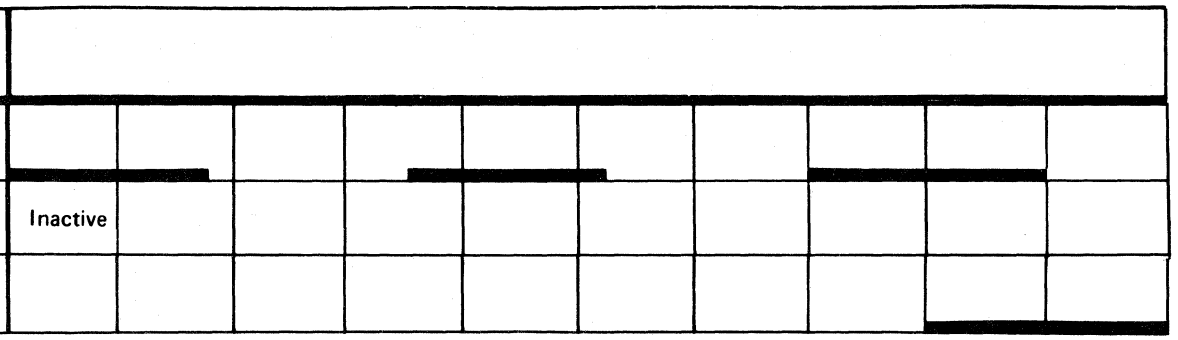
Scope Setup *(See DATA 256 for additional information.)*

Sweep	2 ms/div	Ch 1 A2Q2D05 –G2	
Mode	Alt or Chop		
Trigger	Ext	Volts/div	0.1
	Slope (+)	Probe	x10
	A2L2D13	Ch 2 (see chart)	
	+CE Alert Execute Ind		

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	–G2	BH110	A2Q2 D05	Ⓡ
2	–Write TR	BC180	A2S2 P13	Ⓕ
3	–Data Present	BH160	A2Q2 B08	Ⓛ



Line keys reference the diagram on DATA 558.

CE0949 Seq. 2 of 2	2358715 Part No.	441300 31 Mar 76	441303 30 Jul 76			

ERROR ALERT

AF9A ERROR CODE WITH FAULT SYMPTOM CODE 9102

Microdiagnostic Setup

Loop routine AF, test 8 for 15 seconds only).
1. Load routine AF.
2. Enter 10, 08, 00, 01, 00.

After 15 seconds – continue.

Loop routine AF, test 9.
1. Load routine AF.
2. Enter 10, 09, 00, 01, 00.

See DATA 254 for a description of routine AF, tests 8 and 9.

Scope Setup *(See DATA 256 for additional information.)*

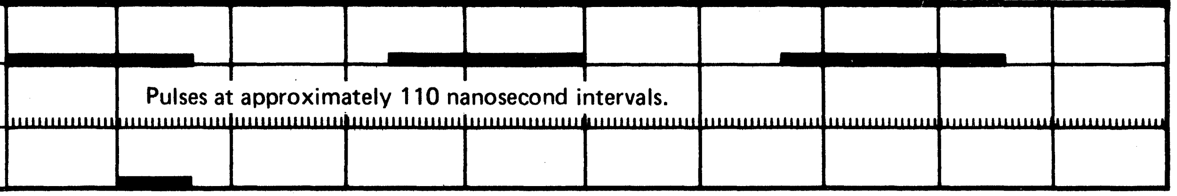
Sweep 2 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2D05
–G2
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 2 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	–G2	BH110	A2Q2 D05	R
2	–VFO 1F	BH100	A2Q2 B11	P
3	–Data Good	BH130	A2Q2 G11	K



Line keys reference the diagram on DATA 558.

AFAA ERROR CODE WITH FAULT SYMPTOM CODE 14xx

Microdiagnostic Setup

Loop routine AF, test A.
1. Load routine AF.
2. Enter 10, 0A, 00, 01, 00.

See DATA 276 for a description of routine AF, test A.

Scope Setup *(See DATA 266 for additional information.)*

Sweep	10 μs/div	Ch 1 A2Q2D02 –G3	
Mode	Alt or Chop	Volts/div	0.1
Trigger	Ext Slope (-) A2L2J11 –MST RAS TP	Probe	x10
		Ch 2 (see chart)	

AFAA ERROR CODE WITH FAULT SYMPTOM CODE 9102

Microdiagnostic Setup

Loop routine AF, test A.
1. Load routine AF.
2. Enter 10, 0A, 00, 01, 00.

See DATA 276 for a description of routine AF, test A.

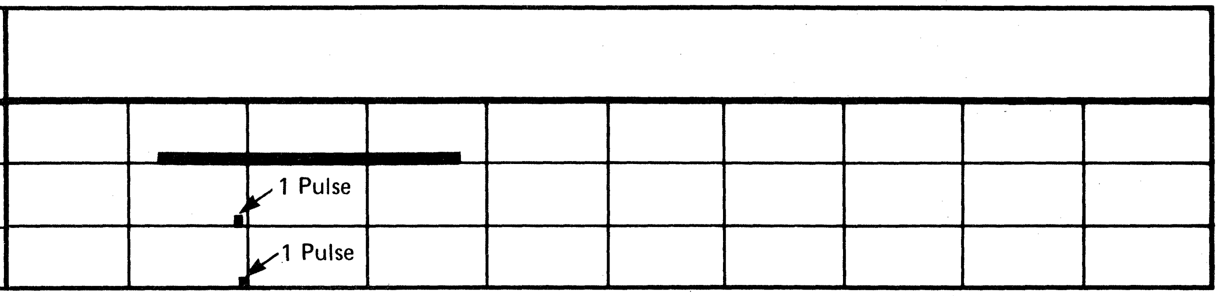
Scope Setup *(See DATA 266 for additional information.)*

Sweep	10 μs/dis	Ch 1 A2Q2D02 –G3	
Mode	Alt or Chop	Volts/div	0.1
Trigger	Ext Slope (-) A2L2J11 –MST RAS TP	Probe	x10
		Ch 2 (see chart)	

Legend:
- ☐ Inactive
- ■ Active level
- ▨ Tolerance

For Fault Symptom Code 14xx

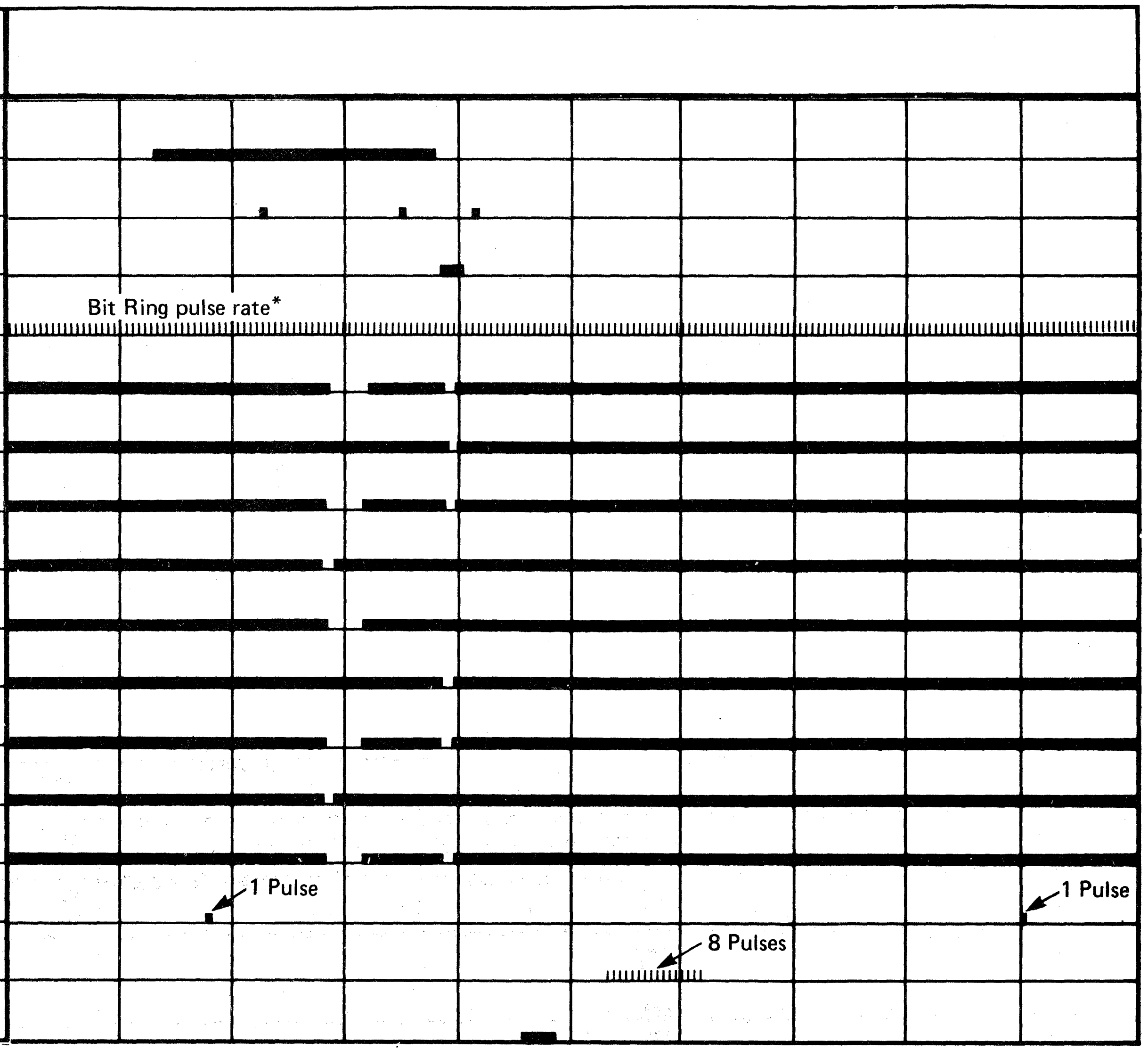
Chart Line No.	Line Name	ALD	Test Point	
1	–G3	BH110	A2Q2 D02	Ⓢ
2	–CT 64	BH140	A2Q2 G09	Ⓜ
3	–CT 65	BH130	A2Q2 G04	Ⓝ



Line keys reference the diagram on DATA 558.

For Fault Symptom Code 9102

Chart Line No.	Line Name	ALD	Test Point	
1	–G3	BH110	A2Q2 D02	Ⓢ
2	–CT 3	BG120	A2P2 M08	Ⓙ
3	–Write TR	BK100	A2N2 D12	Ⓓ
4	–Bit Ring 1 Pwr	BK100	A2N2 D03	Ⓔ
5	–Data Bit 0	BK140	A2N2 S05	Ⓐ
6	–Data Bit 1	BK140	A2N2 U12	
7	–Data Bit 2	BK140	A2N2 S12	
8	–Data Bit 3	BK140	A2N2 U05	
9	–Data Bit 4	BK150	A2N2 J04	
10	–Data Bit 5	BK150	A2N2 G04	
11	–Data Bit 6	BK150	A2N2 G02	
12	–Data Bit 7	BK150	A2N2 B12	
13	–Data Bit P	BK150	A2N2 J05	
14	–Ct 63	BK190	A2N2 D04	Ⓒ
15	–Ct 17	BK190	A2N2 M05	Ⓑ
16	+Delay Servo Mode	BG150	A2P2 B11	Ⓖ



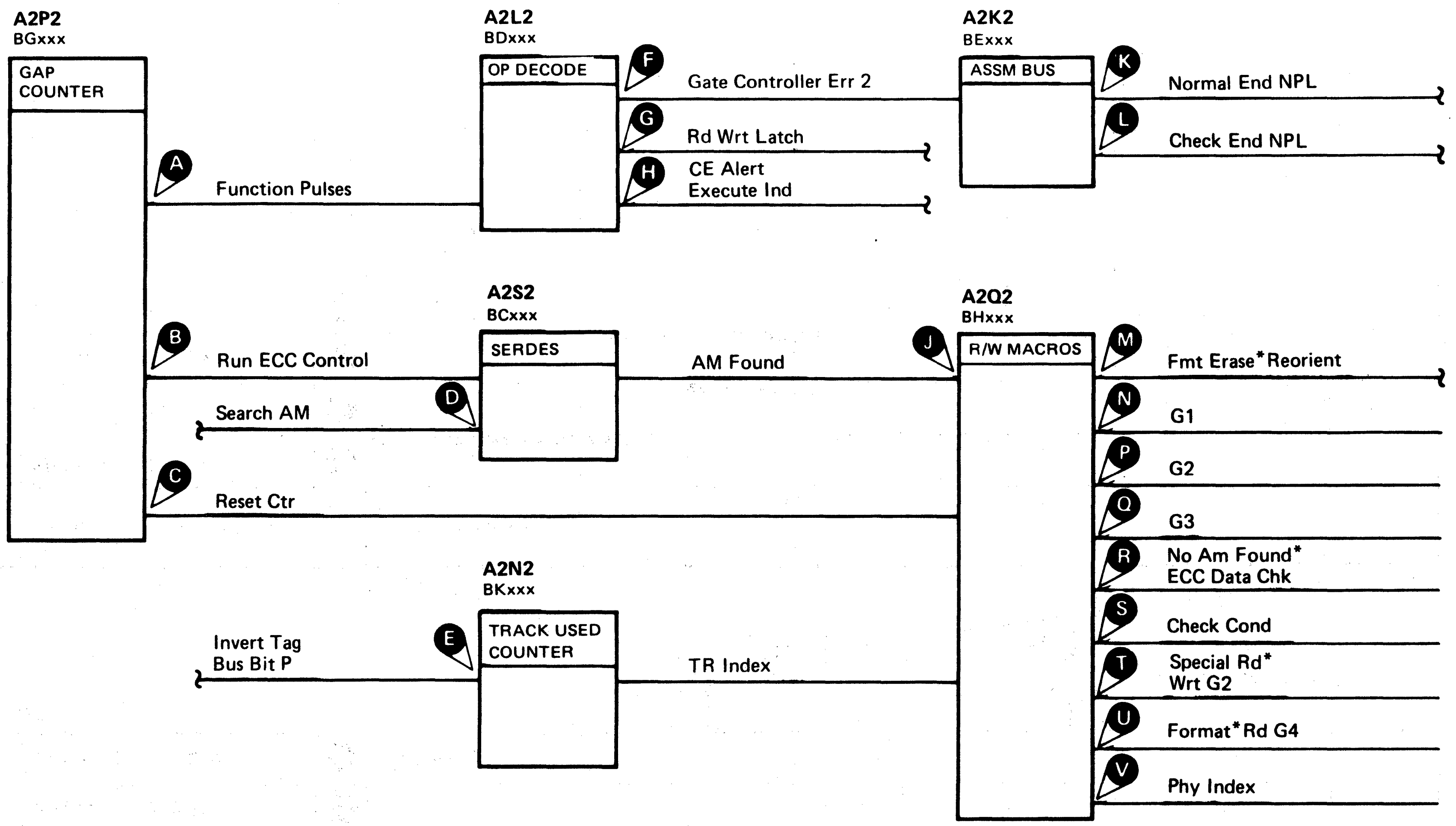
Line keys reference the diagram on DATA 558.

**See DATA 996 for description of pulse duration and repetition rate.*

AF TEST B AND F/ B8 TEST D DIAGRAM

See the sequence charts on DATA 580, DATA 590, DATA 608, and 612 for referenced test points.

See OPER 241 for theory.



3350	CE0957 Seq. 1 of 2	2358615 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST B SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AF, test B
1. Load AF
2. Enter 10,0B,00,00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop

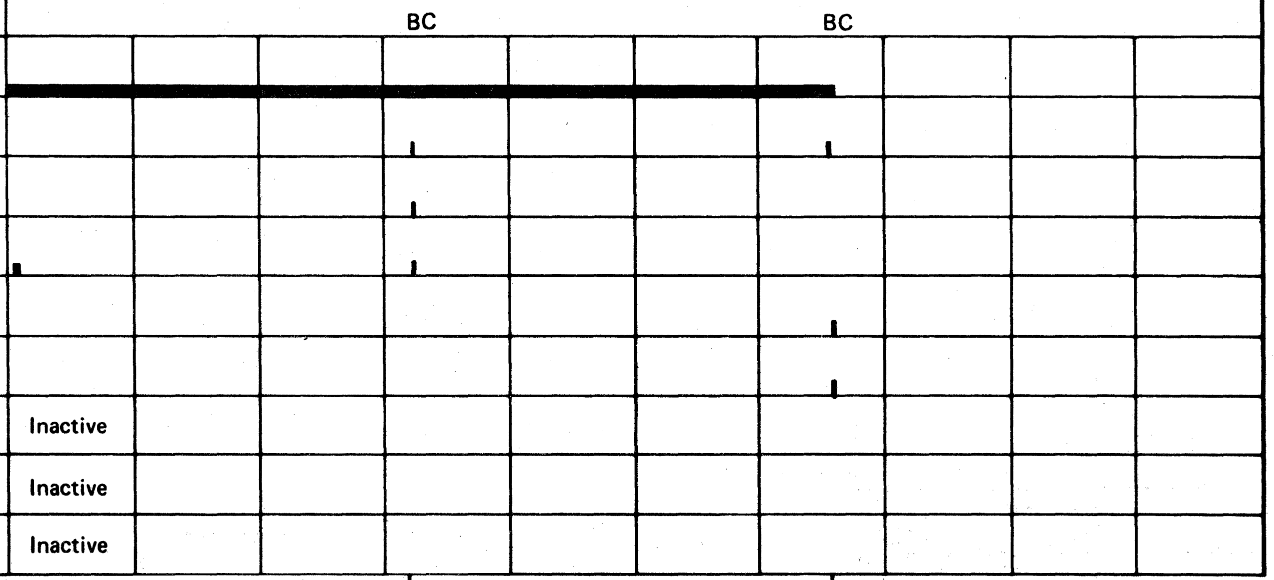
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend: ☐ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+CE Alert Execute Ind	BD210	A2L2 D13	H	
2	+G1	BH120	A2Q2 J09	N	
3	−G3	BH110	A2Q2 D02	Q	
4	+Normal End NPL	BE160	A2K2 D11	K	
5	−Search AM	BC140	A2S2 B03	D	
6	−AM Found	BH130	A2Q2 G13	J	
7	−No AM Found*ECC Data Chk	BH140	A2Q2 J13	R	Inactive
8	+Check Cond	BH150	A2Q2 B12	S	Inactive
9	+Check End NPL	BE160	A2K2 D05	L	Inactive



Line keys reference the diagram on DATA 575.

A (For expanded sequence chart)
DATA 584

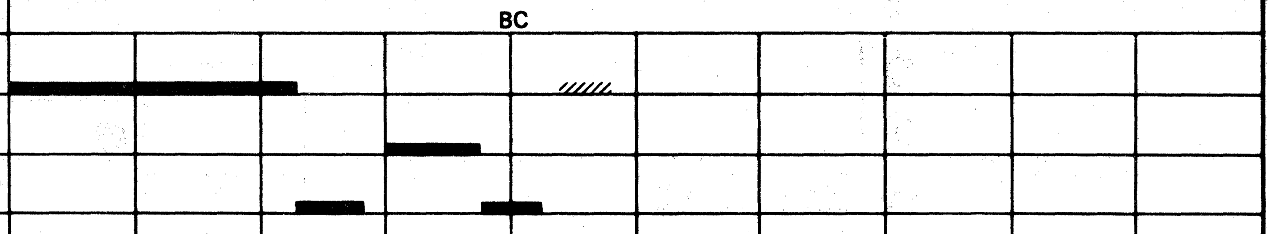
TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 µs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Ch 1 A2Q2J09
−G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Chart Line No.	Line Name	ALD	Test Point		Test Error Number
1	+G1	BH120	A2Q2 J09	N	
2	−G3	BH110	A2Q2 D02	Q	
3	+Normal End NPL	BE160	A2K2 D11	K	
4	−Search AM	BC140	A2S2 B03	D	Inactive
5	−AM Found	BH130	A2Q2 G13	J	Inactive
6	−No AM Found*ECC Data Chk	BH140	A2Q2 J13	R	Inactive
7	+Check Cond	BH150	A2Q2 B12	S	Inactive
8	+Check End NPL	BE160	A2K2 D05	L	Inactive



Line keys reference the diagram on DATA 575.

3350	CE0957 Seq. 2 of 2	2358615 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST B SEQUENCE CHART

TRIGGERING INSTRUCTIONS

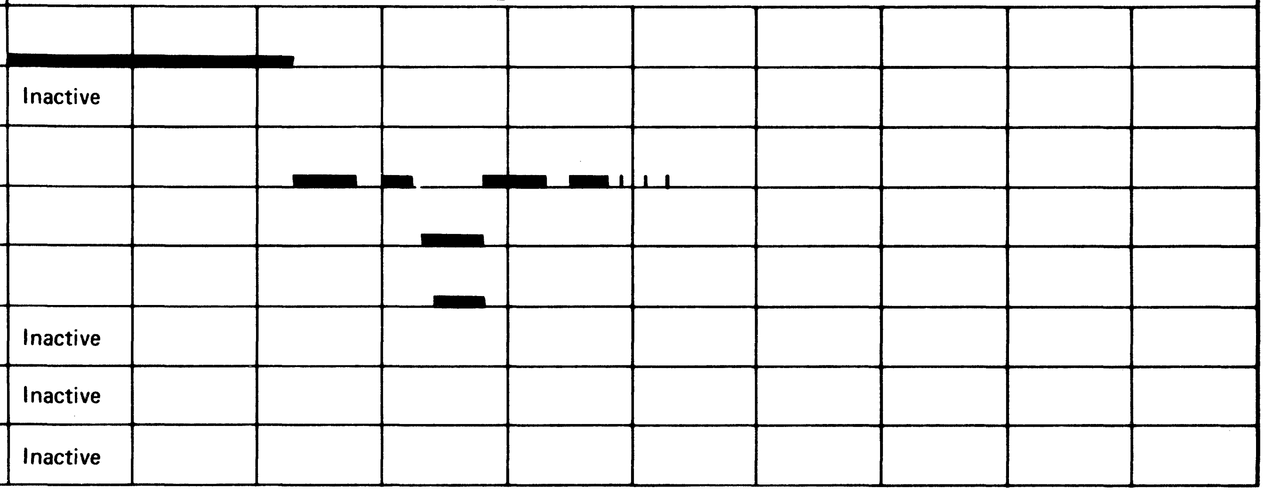
Scope Setup

Sweep	5 ms/div	Ch 1 A2Q2J09 +G1	
Mode	Alt or Chop	Volts/div	0.1
Trigger	Ext	Probe	x10
	Slope (+)	Ch 2 (see chart)	
	A2L2D13 +CE Alert Execute Ind		

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 50 μs/div
Delay-Time Multiplier – 3.5
Source – Int Ch 1

Legend: ▭ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number BC
1	+G1	BH120	A2Q2 J09	Ⓝ	
2	–G3	BH110	A2Q2 D02	Ⓠ	Inactive
3	+Normal End NPL	BE160	A2K2 D11	Ⓚ	
4	–Search AM	BC140	A2S2 B03	Ⓓ	
5	–AM Found	BH130	A2Q2 G13	Ⓙ	
6	–No AM Found*ECC Data Chk	BH140	A2Q2 J13	Ⓡ	Inactive
7	+Check Cond	BH150	A2Q2 B12	Ⓢ	Inactive
8	+Check End NPL	BE160	A2K2 D05	Ⓛ	Inactive



Line keys reference the diagram on DATA 575.

3350

CE0962 Seq. 1 of 2	2358714 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST F SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AF, test F
1. Load AF
2. Enter 10,0F,00,00

Scope Setup

Sweep 10 ms/div
Mode Alt or Chop

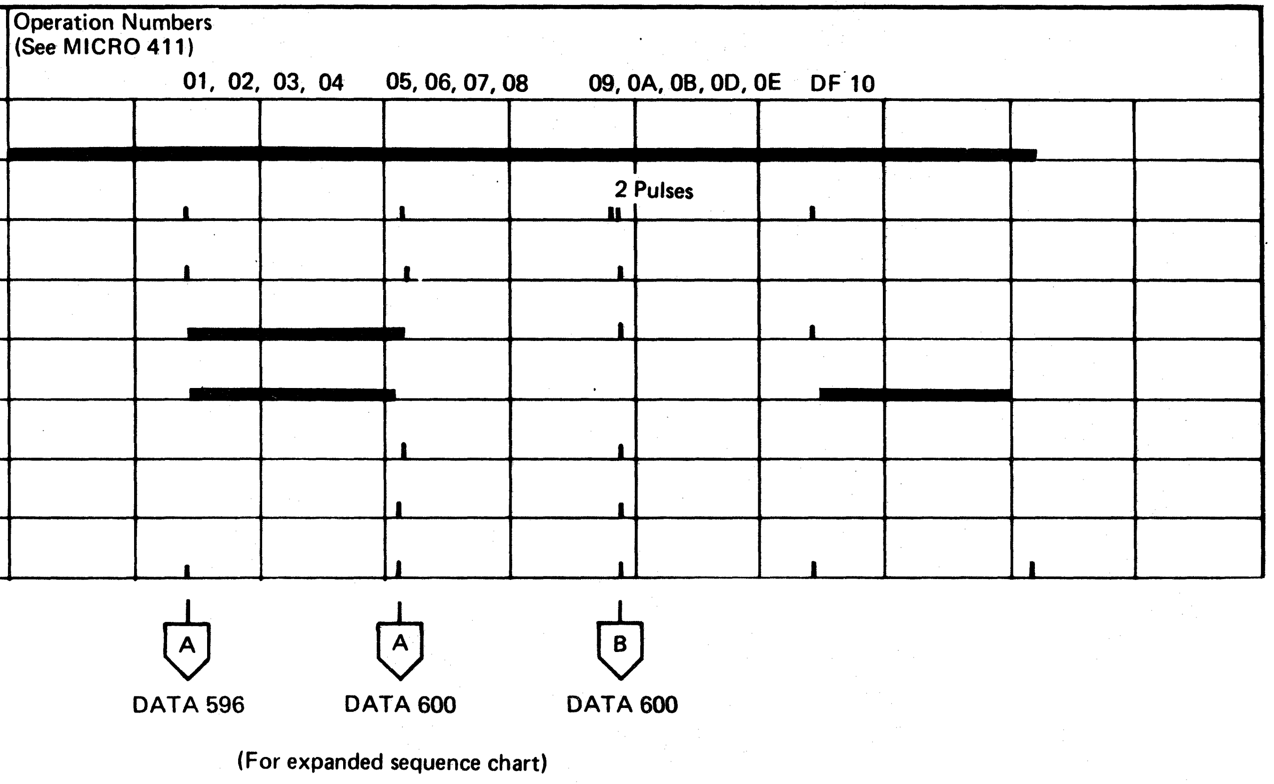
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	H
2	+G1	BH120	A2Q2 J09	N
3	−G2	BH110	A2Q2 D08	P
4	−G3	BH110	A2Q2 D02	Q
5	+Fmt Erase∗Reorient	BH110	A2Q2 G02	M
6	+Special Rd∗Wrt G2	BH110	A2Q2 M12	T
7	−Format∗Rd G4	BH110	A2Q2 U09	U
8	−Phy Index	BH130	A2Q2 S07	V



Line keys reference the diagram on DATA 575.

3350	CE0962 Seq. 2 of 2	2358714 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST F SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 10 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 10 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 ms/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Legend: ▭ Inactive
■ Active level
▨ Tolerance

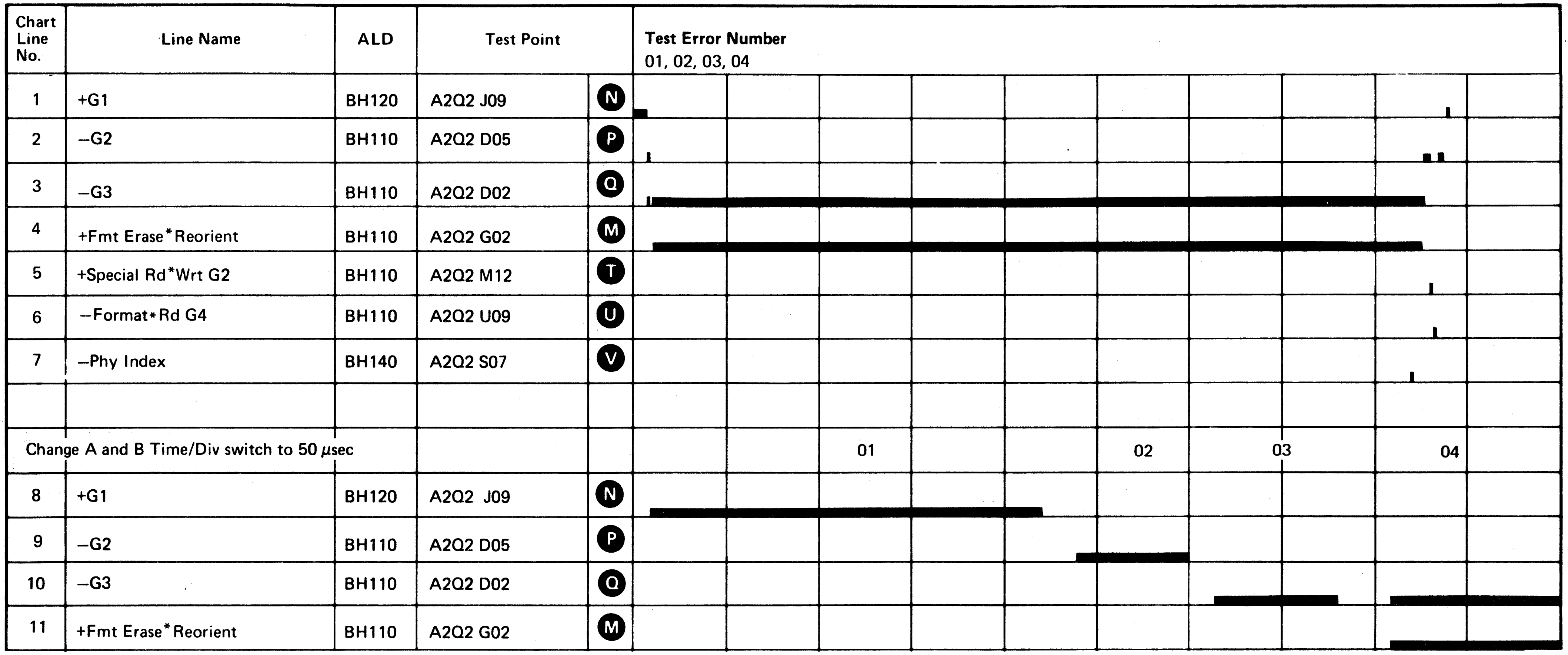


Chart Line No.	Line Name	ALD	Test Point		Test Error Number 01, 02, 03, 04
1	+G1	BH120	A2Q2 J09	N	
2	–G2	BH110	A2Q2 D05	P	
3	–G3	BH110	A2Q2 D02	Q	
4	+Fmt Erase*Reorient	BH110	A2Q2 G02	M	
5	+Special Rd*Wrt G2	BH110	A2Q2 M12	T	
6	–Format∗Rd G4	BH110	A2Q2 U09	U	
7	–Phy Index	BH140	A2Q2 S07	V	
Change A and B Time/Div switch to 50 µsec					01 02 03 04
8	+G1	BH120	A2Q2 J09	N	
9	–G2	BH110	A2Q2 D05	P	
10	–G3	BH110	A2Q2 D02	Q	
11	+Fmt Erase*Reorient	BH110	A2Q2 G02	M	

Line keys reference the diagram on DATA 575.

3350	CE0963 Seq. 1 of 2	2358616 Part No.	441300 31 Mar 76	441303 30 Jul 76			

AF TEST F SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 10 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2S07
–Phy Index
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 10 ms/div
Slope (–)
Delay Time-Delayed Sweep – 0.1 ms/div
Delay-Time Multiplier – 1.6
Source – Int Ch 1

Legend:
☐ Inactive
■ Active level
▨ Tolerance

DATA 590

A

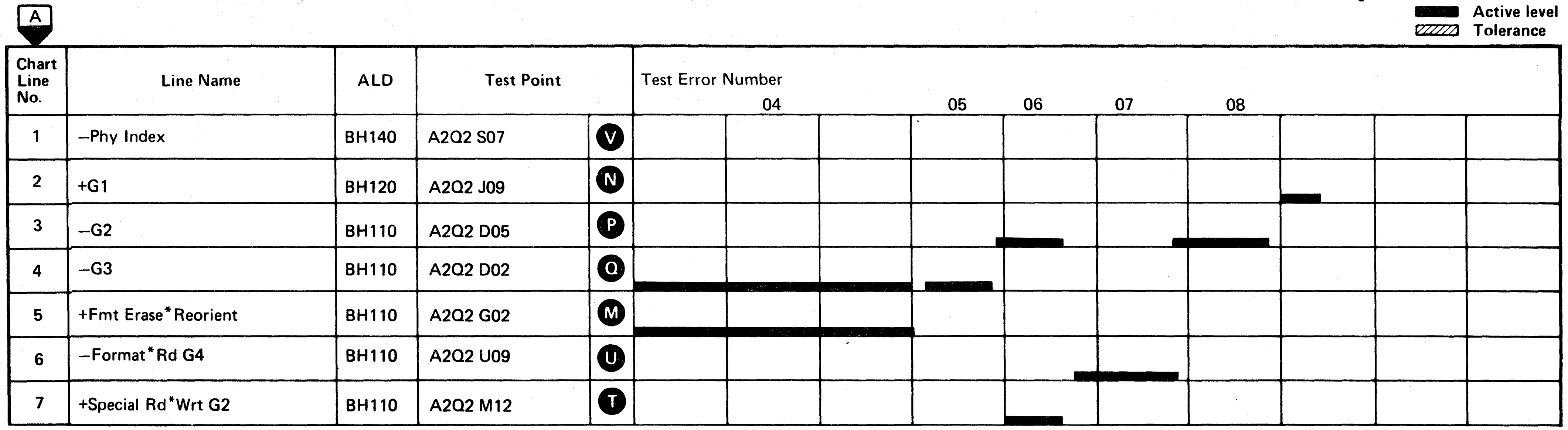


Chart Line No.	Line Name	ALD	Test Point		Test Error Number 04 05 06 07 08
1	–Phy Index	BH140	A2Q2 S07	Ⓥ	
2	+G1	BH120	A2Q2 J09	Ⓝ	
3	–G2	BH110	A2Q2 D05	Ⓟ	
4	–G3	BH110	A2Q2 D02	Ⓠ	
5	+Fmt Erase*Reorient	BH110	A2Q2 G02	Ⓜ	
6	–Format*Rd G4	BH110	A2Q2 U09	Ⓤ	
7	+Special Rd*Wrt G2	BH110	A2Q2 M12	Ⓣ	

Line keys reference the diagram on DATA 575.

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 10 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 10 ms/div
Slope (+)
Delay Time-Delayed Sweep – 0.1 ms/div
Delay-Time Multiplier – 3.5
Source – Int Ch 1

DATA 590

B

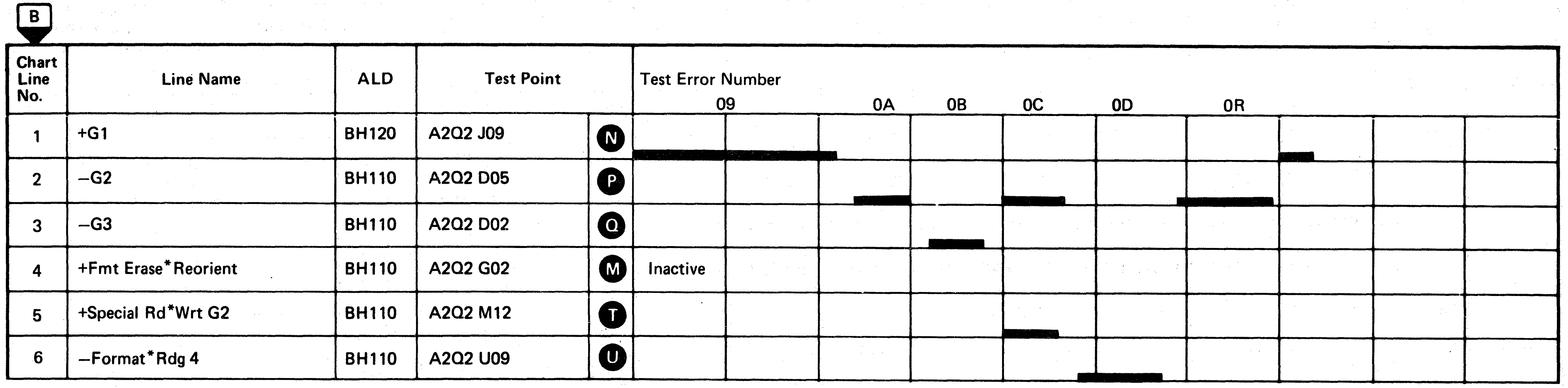


Chart Line No.	Line Name	ALD	Test Point		Test Error Number 09 0A 0B 0C 0D 0R
1	+G1	BH120	A2Q2 J09	Ⓝ	
2	–G2	BH110	A2Q2 D05	Ⓟ	
3	–G3	BH110	A2Q2 D02	Ⓠ	
4	+Fmt Erase*Reorient	BH110	A2Q2 G02	Ⓜ	Inactive
5	+Special Rd*Wrt G2	BH110	A2Q2 M12	Ⓣ	
6	–Format*Rdg 4	BH110	A2Q2 U09	Ⓤ	

Line keys reference the diagram on DATA 575.

3350	CE0963 Seq. 2 of 2	2358616 Part No.	441300 31 Mar 76	441303 30 Jul 76		

ERROR ALERT

B8D0 ERROR CODE

Microdiagnostic Setup

Loop routine B8, test D.

1. Load routine B8.
2. Enter 10, 0D, 00, 01, 00.

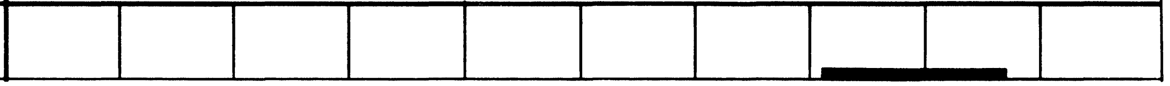
See DATA 292 for a description of routine B8, test D.

Scope Setup *(See DATA 294 for additional information.)*

Sweep 10 μs/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2L2P13
–Gate Controller Err 2
Volts/div 0.1
Probe x10

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		
1	–Gate Controller Err 2	BD100	A2L2 P13	F	

Line keys reference the diagram on DATA 575.

B8D6 ERROR CODE WITH FAULT SYMPTOM CODE 9202

Microdiagnostic Setup

Loop routine B8, test D.

1. Load routine B8.
2. Enter 10, 0D, 00, 01, 00.

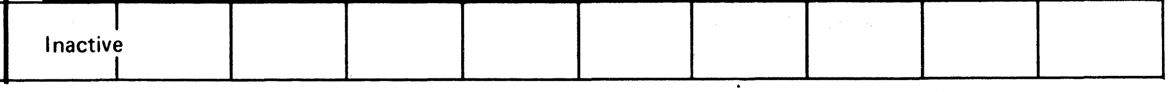
See DATA 292 for a description of routine B8, test D.

Scope Setup *(See DATA 294 for additional information.)*

Sweep 0.1 ms/div
Mode Alt or Chop
Trigger Ext
Slope (–)
A2L2J11
–MST RAS 7P

Ch 1 A2L2J03
–Rd Wrt Latch
Volts/div 0.1
Probe x10
Ch 2 A2P2J02
–Run ECC Control
Volts/div 0.1
Probe x10

For Fault Symptom Code 9202

Chart Line No.	Line Name	ALD	Test Point		
1	–Rd Wrt Latch	BD150	A2L2 J03	G	
2	–Run ECC Control	BG170	A2P2 J02	B	

Line keys reference the diagram on DATA 575.

CE0970 Seq. 1 of 2	2358617 Part No.

441300 31 Mar 76	441303 30 Jul 76			

B8D6 ERROR CODE WITH FAULT SYMPTOM CODE 924x

Microdiagnostic Setup

Loop routine B8, test D.
1. Load routine B8.
2. Enter 10, 0D, 00, 01, 00.

See DATA 292 for a description of routine B8, test D.

Scope Setup *(See DATA 294 for additional information.)*

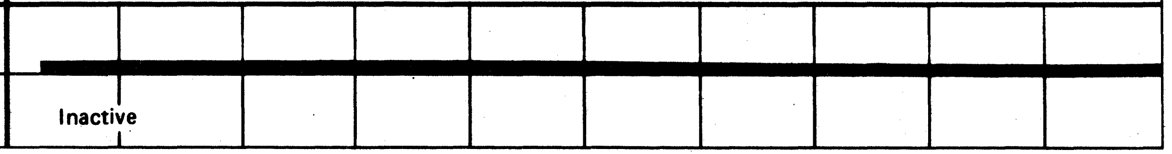
Sweep 0.1 ms/div
Mode Alt or Chop
Trigger Ext
Slope (-)
A2L2J11
−MST RAS TP

Ch 1 A2L2J03
−Rd Wrt Latch
Volts/div 0.1
Probe x10
Ch 2 A2N2J09
−Invert Tag Bus Bit P
Volts/div 0.1
Probe x10

Legend: ▭ Inactive
■ Active level
▨ Tolerance

For Fault Symptom Code 924x

Chart Line No.	Line Name	ALD	Test Point		
1	−Rd Wrt Latch	BD150	A2L2 J03	Ⓖ	
2	−Invert Tag Bus Bit P	BK110	A2N2 J09	Ⓔ	



Line keys reference the diagram on DATA 575.

B8D6 ERROR CODE WITH FAULT SYMPTOM CODE 92x4

Microdiagnostic Setup

Loop routine B8, test D.
1. Load routine B8.
2. Enter 10, 0D, 00, 01, 00.

See DATA 292 for a description of routine B8, test D.

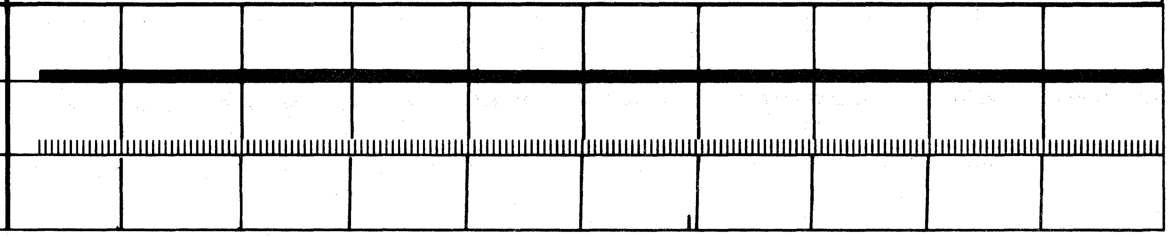
Scope Setup *(See DATA 294 for additional information.)*

Sweep 0.1 ms/div
Mode Alt or Chop
Trigger Ext
Slope (-)
A2L2J11
−MST RAS TP

Ch 1 A2L2J03
−Rd Wrt Latch
Volts/div 0.1
Probe x10
Ch 2 (see chart)

For Fault Symptom Code 92x4

Chart Line No.	Line Name	ALD	Test Point		
1	−Rd Wrt Latch	BD150	A2L2 J03	Ⓖ	
2	−Function Pulses	BG160	A2P2 G12	Ⓐ	
3	−Reset Ctr	BG100	A2P2 G09	Ⓒ	



Line keys reference the diagram on DATA 575.

CE0970 Seq. 2 of 2	2358617 Part No.	441300 31 Mar 76	441303 30 Jul 76			

ERROR ALERT 5 DATA

MICRODIAGNOSTIC DESCRIPTION

See DATA 292 for a description of routine B8, test D.

Routine B8, test D verifies that a Set Read/Write operates in the following way:

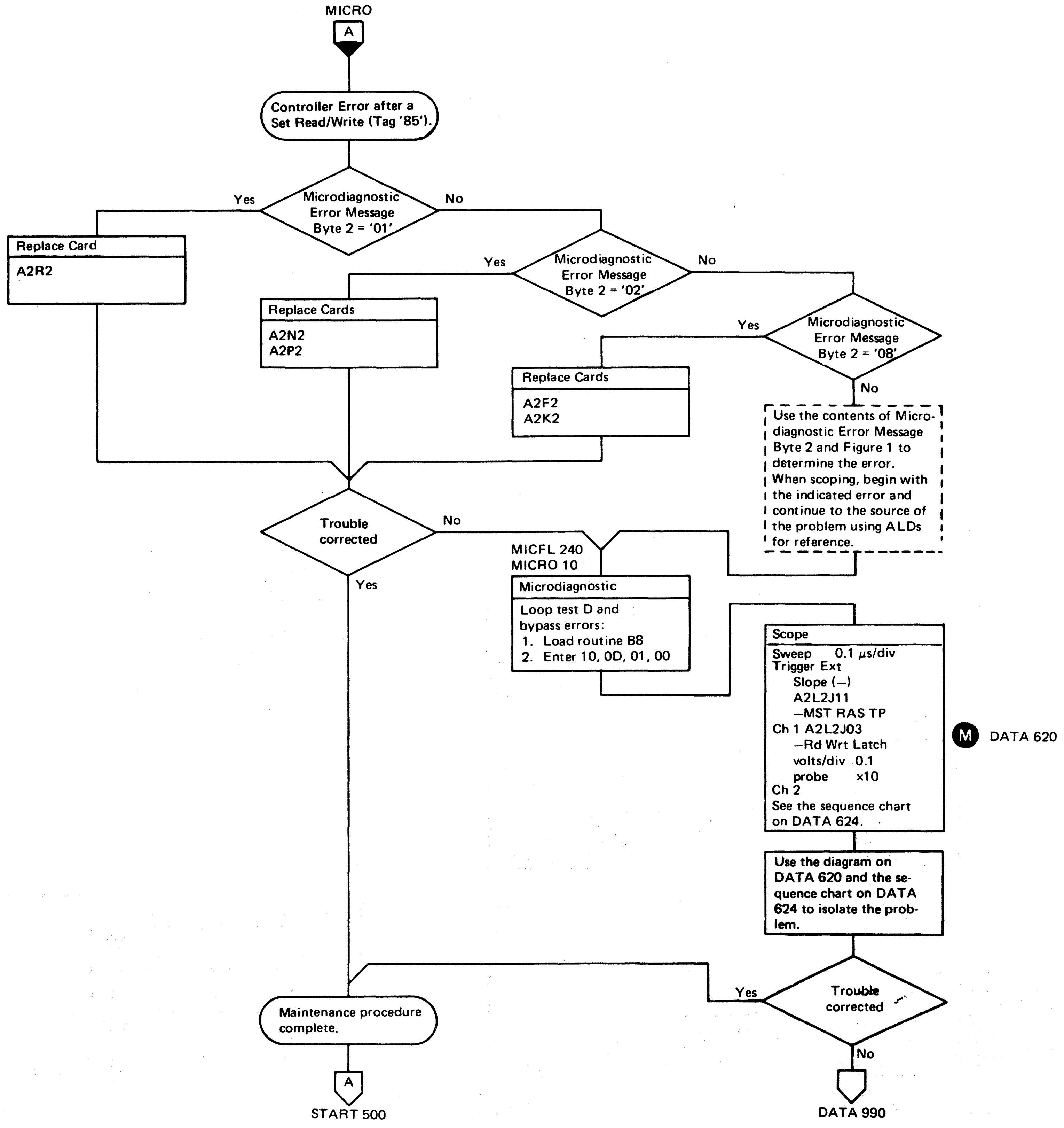
1. Functions as in Extended operation; that is, does not return Normal End with Tag Valid.
2. **Returns Normal End at the proper time to signify completion of the operation.**

Test D also verifies that Normal End is reset by the End Response tag. Check conditions that occur during this operation are also indicated.

The test also forces Monitor Check.

Figure 1. Microdiagnostic Error Message Byte 2 Display Definitions

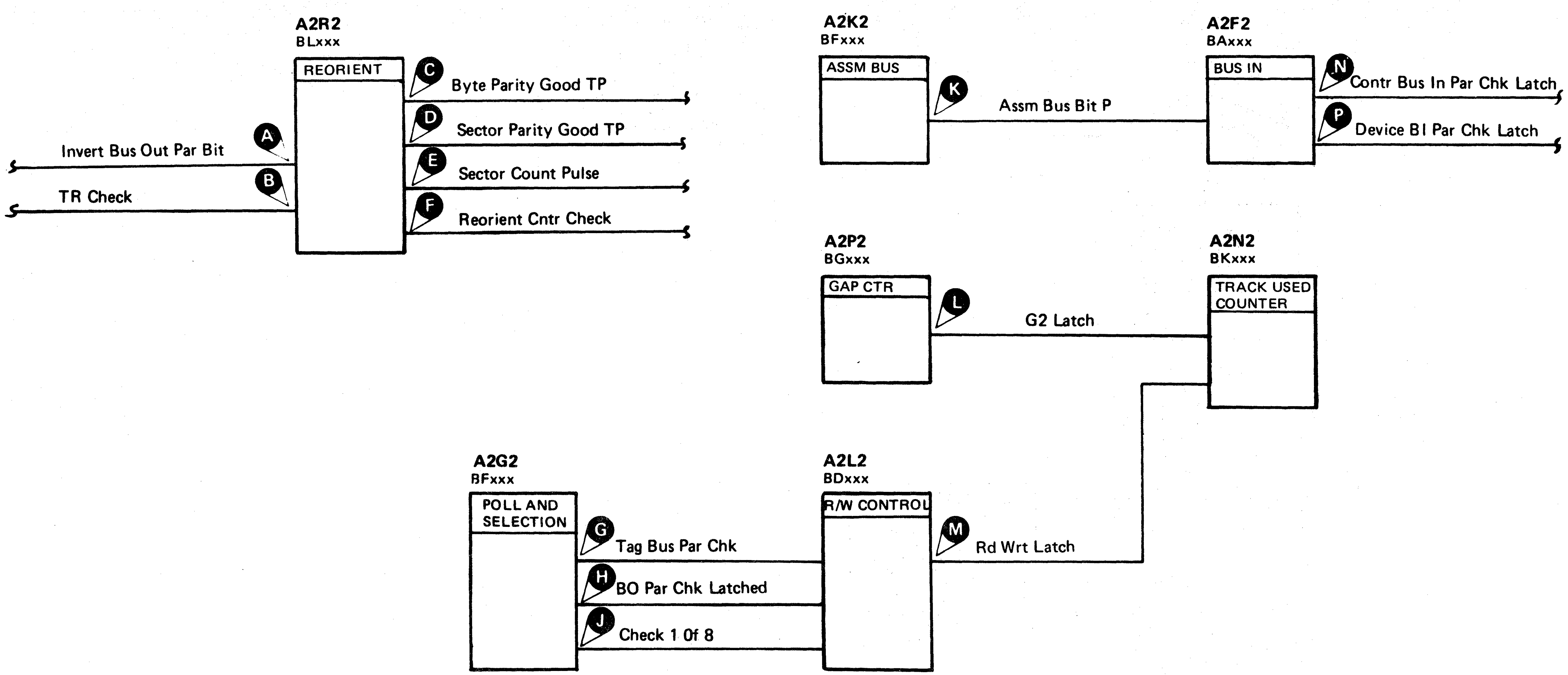
Byte 2	**Error Name**
'80'	Tag Bus Parity Check
'40'	Bus Out Parity Check latched
'20'	Check 1 of 8
'10'	Device Bus In Parity Check latched
'08'	Controller Bus In Parity Check latched
'04'	Invalid
'02'	TR Check
'01'	Reorient Counter Check



ERROR ALERT 5 DATA

See the sequence chart on DATA 624 for referenced test points.

See OPER 241 for theory.

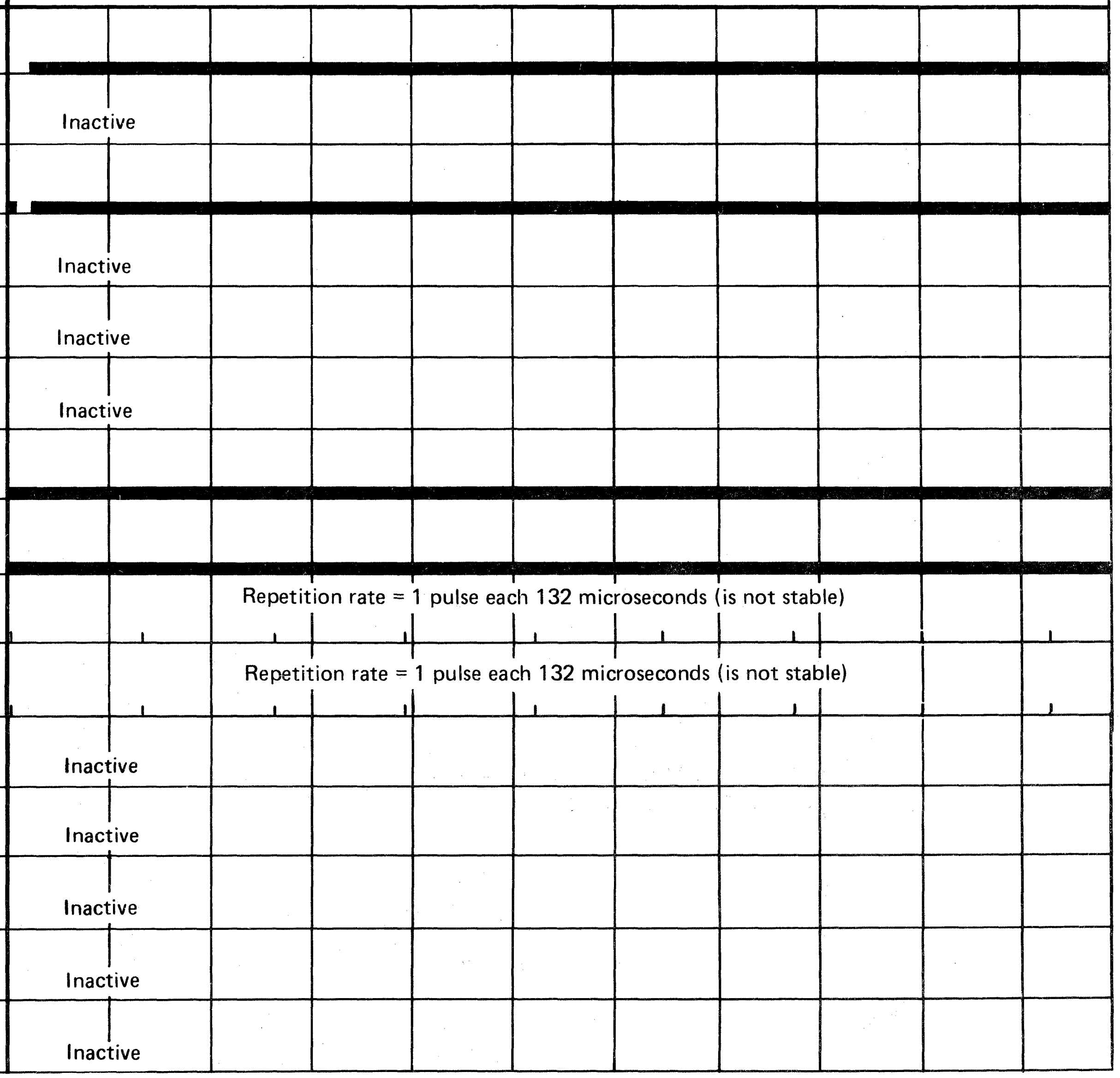


CE0974 Seq. 2 of 2	2358618 Part No.	441300 31 Mar 76	441303 30 Jul 76			

ERROR ALERT 5 DATA

Legend: ☐ Inactive ■ Active level ▨ Tolerance

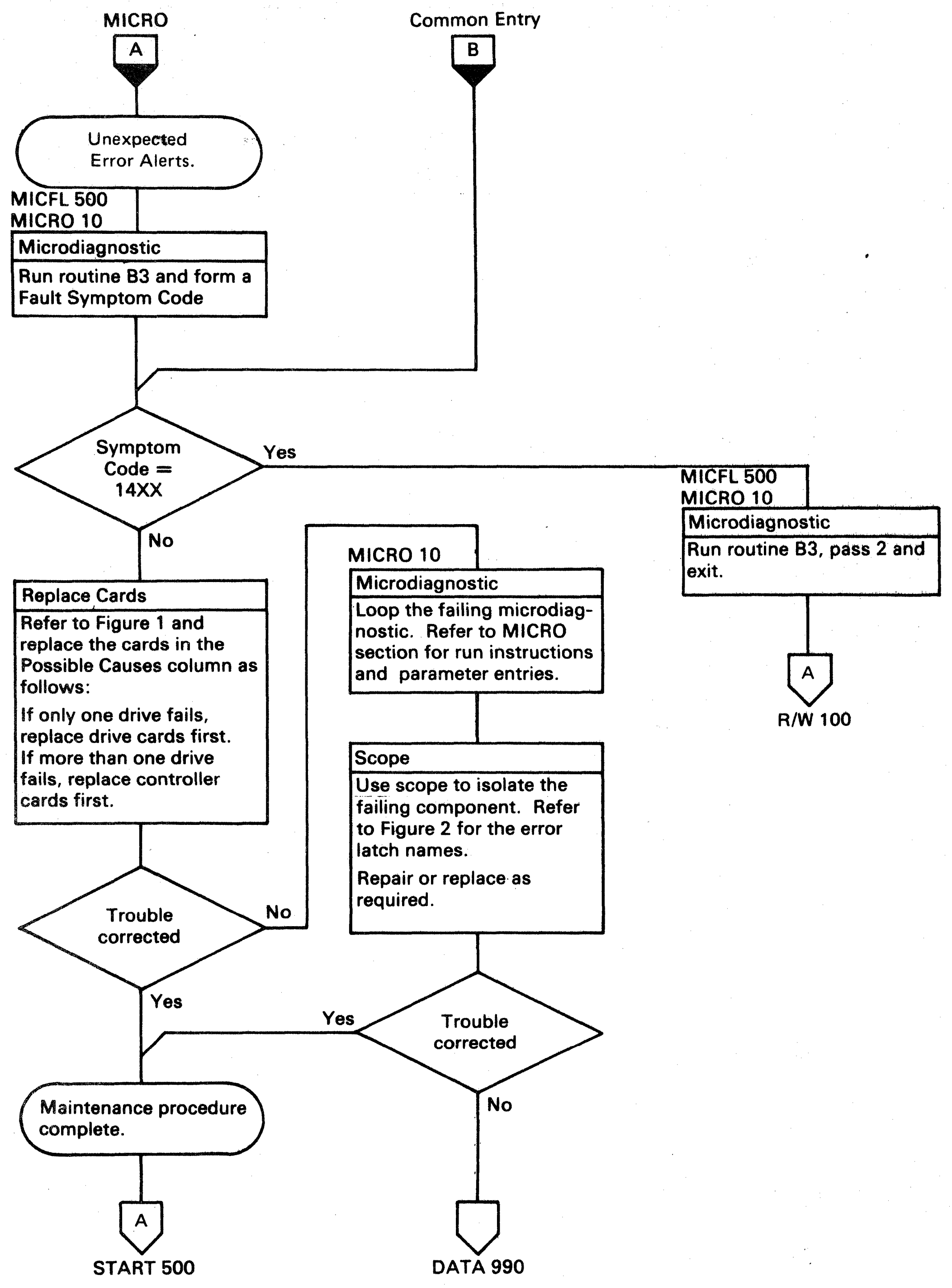
Chart Line No.	Line Name	ALD	Test Point		
1	–Rd Wrt Latch	BD150	A2L2 J03	Ⓜ	
2	–Contr Bus In Par Chk Latch	BA130	A2F2 P11	Ⓝ	Inactive
3	–Assm Bus Bit P	BE110	A2K2 G07	Ⓚ	
4	+TR Check	BK140	A2N2 B10	Ⓑ	Inactive
5	+G2 Latch	BG180	A2P2 U10	Ⓛ	Inactive
6	+Reorient Cntr Check	BL120	A2R2 G04	Ⓕ	Inactive
7	+Byte Parity Good TP	BL100	A2R2 B11	Ⓒ	
8	+Sector Parity Good TP	BL110	A2R2 D11	Ⓓ	
9	+Sector Count Pulse	BL120	A2R2 D09	Ⓔ	Repetition rate = 1 pulse each 132 microseconds (is not stable)
10	–Sector Count Pulse	BL120	A2R2 D12	Ⓔ	Repetition rate = 1 pulse each 132 microseconds (is not stable)
11	–Invert Bus Out Par Bit	BL100	A2R2 J02	Ⓐ	Inactive
12	–Tag Bus Par Chk	BF110	A2G2 G10	Ⓖ	Inactive
13	–BO Par Chk Latched	BF110	A2G2 J10	Ⓗ	Inactive
14	+Check 1 of 8	BF200	A2G2 S13	Ⓙ	Inactive
15	–Device BI Par Chk Latch	BA140	A2F2 M05	Ⓟ	Inactive



Line keys reference the diagram on DATA 620.

CE0976 Seq. 1 of 2	2358832 Part No.	441303 30 Jul 76	441308 18 Aug 78			

FAULT SYMPTOM CODE LIST



Use bit configuration in Fault Symptom Code Byte 2 column for symptom codes not shown in Figure 1.

Figure 1. Fault Symptom Code Card Replacement List

Fault Symptom Code	Fault Symptom Code Byte 2 91xx (xx)	Possible Causes
9180	Bit 0 = 1	A2G2, A2K2, A2L2, A2F2 – SWFE A2D2 (A2E2), A2H2 (A2J2)
9140	1 = 1	A2G2, A2K2, A2F2 – SWFE A2D2 (A2E2)
9120	2 = 1	A2G2, A2L2, A2K2, A2F2 – A1K2 (A1L2)
9110	3 = 1	A2F2, A2K2, A2G2 – A1H2 (A1N2), A1K2 (A1L2)
9108	4 = 1	A2F2, A2G2, A2P2, A2K2
9104	5 = 1	A2P2, A2F2, A2Q2, A2K2 – A1H2 (A1N2)
9102	6 = 1	A2N2, A2P2, A2Q2, A2S2, A2R2
9101	7 = 1	A2R2, A2P2, A2Q2, A2N2, A2F2, A2K2
	92xx (xx)	
92C0	Bits 0, 1 = 11	Exit to R/W 300, Entry B
9280	Bits 0, 1 = 10	A2S2, A2F2, A2P2, A2Q2 – A1G2 (A1P2), A1H2 (A1N2), A1J2 (A1M2)
9240	Bits 0, 1 = 01	A2T2, A2Q2, A2N2, A2P2, A2R2 – A1H2 (A1N2), Cable A2V2 (A1V3)
9220	Bit 2 = 1	A2S2, A2P2, A2K2, A2T2
9210	Bit 3 = 1	A2P2, A2G2, A2S2, A2Q2, A2L2
9208	Bit 4 = 1	A2N2, A2P2, A2Q2, A2S2
9204	Bit 5 = 1	A2P2, A2Q2, A2S2, A2L2
9202	Bit 6 = 1	A2S2, A2P2, A2R4, A2Q2, A2N2
9201	Bit 7 = 1	Invalid Symptom Code
9200	All Bits = 0	A2S2, A2K2, A2R2, A2F2

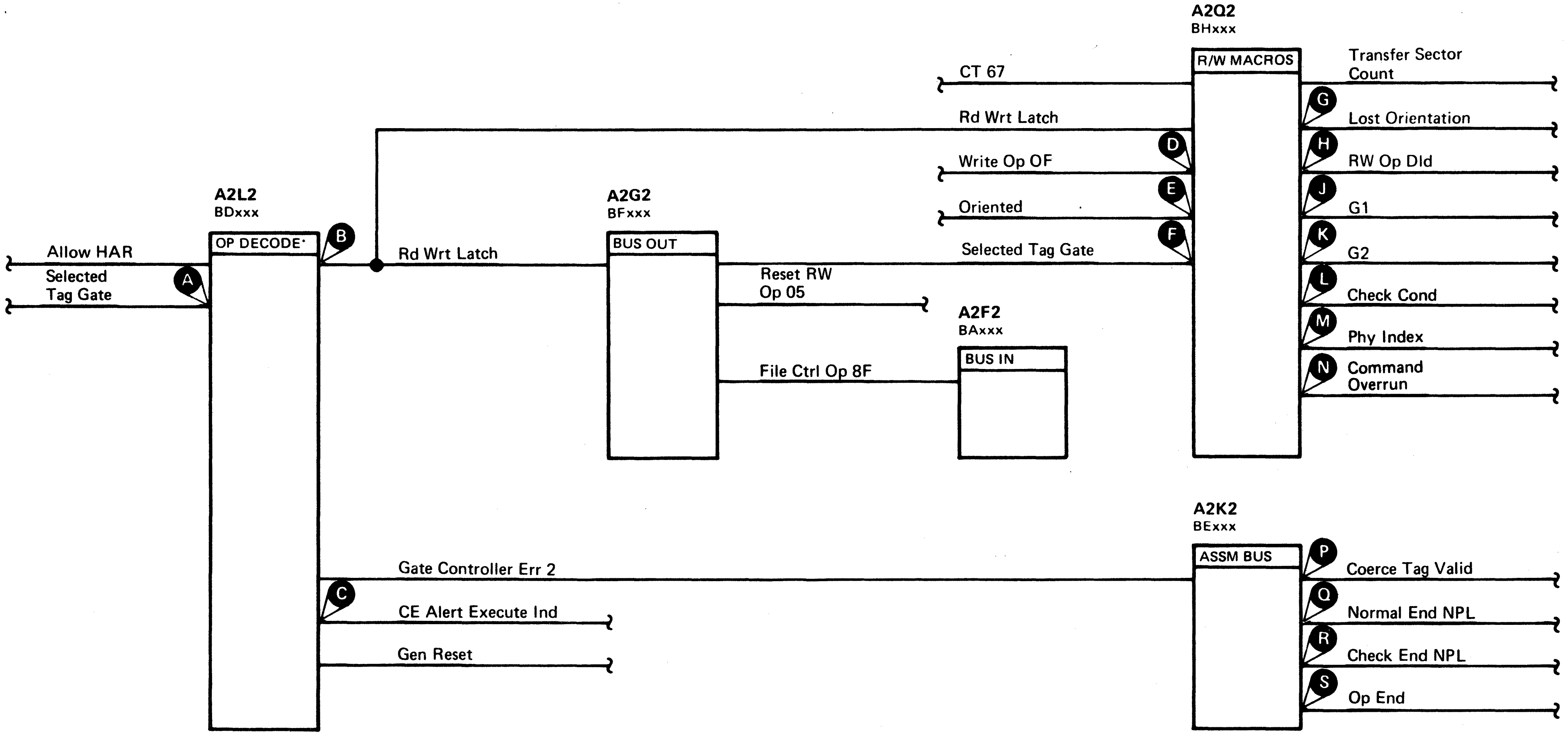
Figure 2. Fault Symptom Code Test Point List

Fault Symptom Code	Error Latch Name	ALD	Test Point
9180	Tag Bus Parity Check	BF110	A2G2 G10
9140	Bus Out Parity Check	BF110	A2G2 J10
9120	Check 1 of 8	BF200	A2G2 S13
9110	Device Bus In Parity Check	BA140	A2F2 M05
9108	Ctl Bus Parity Check	BF130	A2F2 P11
9104	I Write Fail	BG150	A2P2 P02
9102	TR Check	BK140	A2N2 B10
9101	Reorient Counter Check	BL120	A2R2 J10
9200	Missing Data	BL140	A2R2 D07
9280	Phase Error	BL140	A2R2 D07
9240	Missing Servo Pulses	BL140	A2R2 G07
9220	Shift Register Error	BC110	A2S2 P02
9210	Counter Check	BG160	A2P2 J09
9208	Write Data Check	BC130	A2S2 P06
9204	Monitor Check	BD160	A2L2 D09
9202	ECC Hardware Check	BE160	A2S2 S07

AF TEST 2, 3, and 5 DIAGRAM

See the sequence charts on DATA 632 and DATA 642 for referenced test points.

See OPER 241 for theory.



3350	CE0978 Seq. 1 of 2	2358833 Part No.	441303 30 Jul 76				

AF TEST 2 SEQUENCE CHART

MICRODIAGNOSTIC DESCRIPTION

Routine AF, test 2 tests the oriented circuitry and timing. The program orients on the Index and reads the Home Address field. The program then delays a maximum allowable amount of time before issuing a Write G2 operation. The Command Overrun or unoriented condition at this time produces error Number 24.

When the first part of test 2 is complete, the previous steps are repeated. The program delay is increased, resulting in an unoriented condition before the Write G2 operation is issued. The Command Overrun indication is the expected response. Error Number 28 indicates the 3350's failure to recognize the Command Overrun indication. The Command Overrun causes a Check End condition. Error Number 26 indicates the 3350's failure to receive the Check End indication.

Legend:
- ☐ Inactive
- ■ Active level
- ▨ Tolerance

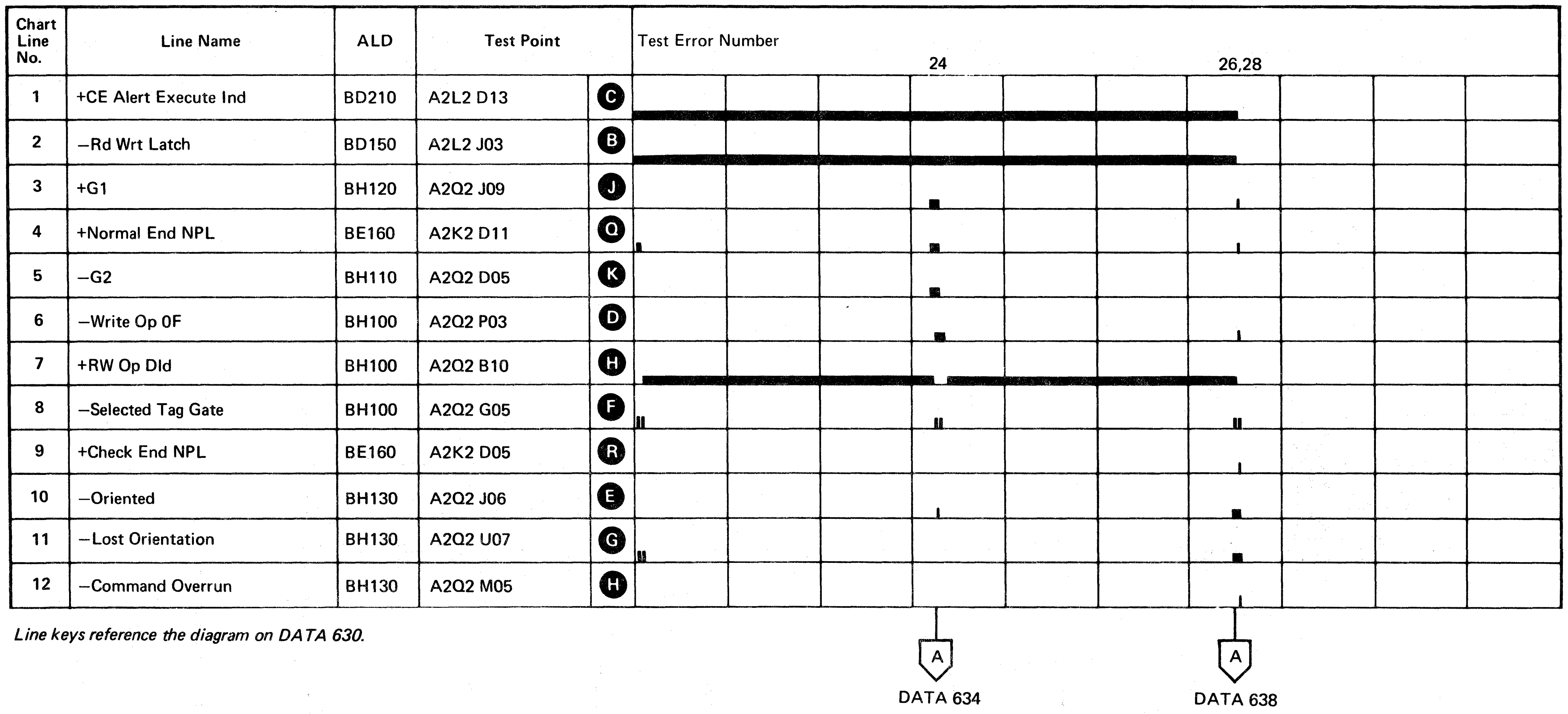


Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	C
2	−Rd Wrt Latch	BD150	A2L2 J03	B
3	+G1	BH120	A2Q2 J09	J
4	+Normal End NPL	BE160	A2K2 D11	Q
5	−G2	BH110	A2Q2 D05	K
6	−Write Op 0F	BH100	A2Q2 P03	D
7	+RW Op Dld	BH100	A2Q2 B10	H
8	−Selected Tag Gate	BH100	A2Q2 G05	F
9	+Check End NPL	BE160	A2K2 D05	R
10	−Oriented	BH130	A2Q2 J06	E
11	−Lost Orientation	BH130	A2Q2 U07	G
12	−Command Overrun	BH130	A2Q2 M05	H

Line keys reference the diagram on DATA 630.

(For expanded sequence chart)

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AF, test 2
1. Load AF
2. Enter 10,02,00,00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop

Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Ch 1 A2U4D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

AF TEST 2 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

DATA 632
A

Legend:
▭ Inactive
■ Active level
▨ Tolerance

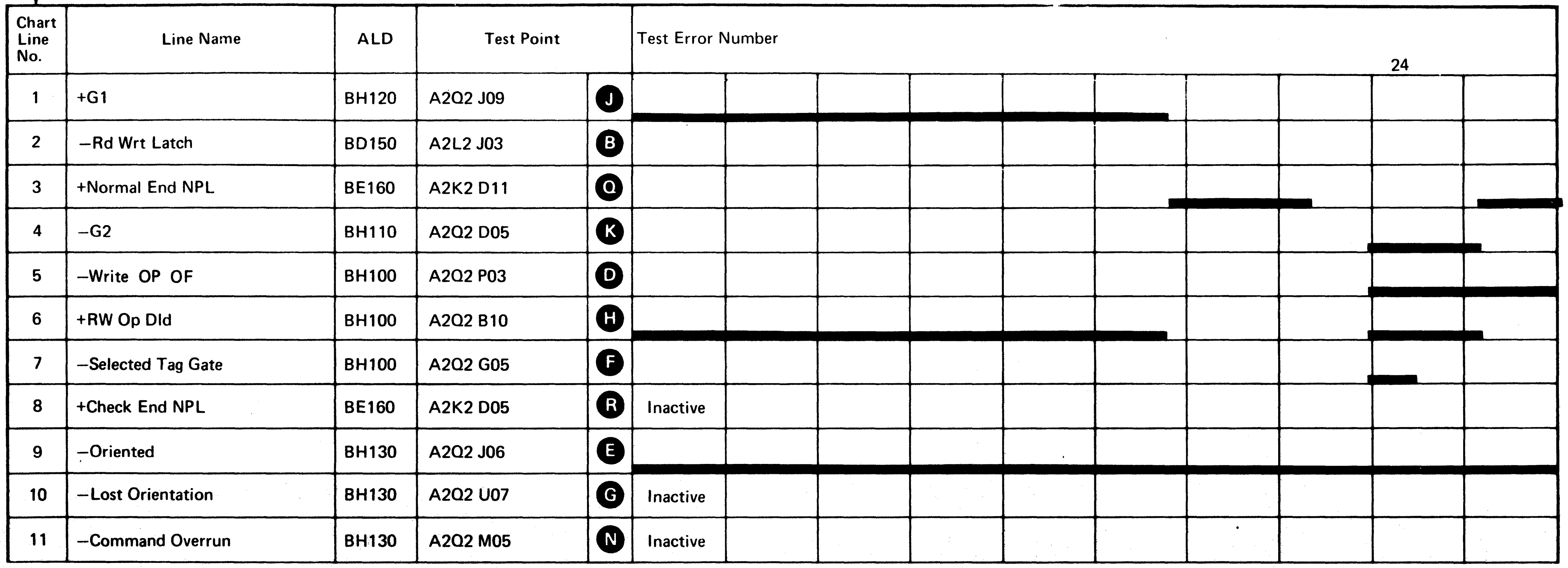


Chart Line No.	Line Name	ALD	Test Point		Test Error Number
					24
1	+G1	BH120	A2Q2 J09	Ⓙ	
2	–Rd Wrt Latch	BD150	A2L2 J03	Ⓑ	
3	+Normal End NPL	BE160	A2K2 D11	Ⓠ	
4	–G2	BH110	A2Q2 D05	Ⓚ	
5	–Write OP OF	BH100	A2Q2 P03	Ⓓ	
6	+RW Op Dld	BH100	A2Q2 B10	Ⓗ	
7	–Selected Tag Gate	BH100	A2Q2 G05	Ⓕ	
8	+Check End NPL	BE160	A2K2 D05	Ⓡ	Inactive
9	–Oriented	BH130	A2Q2 J06	Ⓔ	
10	–Lost Orientation	BH130	A2Q2 U07	Ⓖ	Inactive
11	–Command Overrun	BH130	A2Q2 M05	Ⓝ	Inactive

Line keys reference the diagram on DATA 630.

3350	CE0980 Seq. 1 of 2	2358834 Part No.	441303 30 Jul 76				

AF TEST 2 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (+)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 3.5
Source – Int Ch 1

Ch 1 A2Q2J09
+G1
Volts/div 0.1
Probe x10
Ch 2 (See chart)

DATA 632
A

Legend: ▭ Inactive
■ Active level
▨ Tolerance

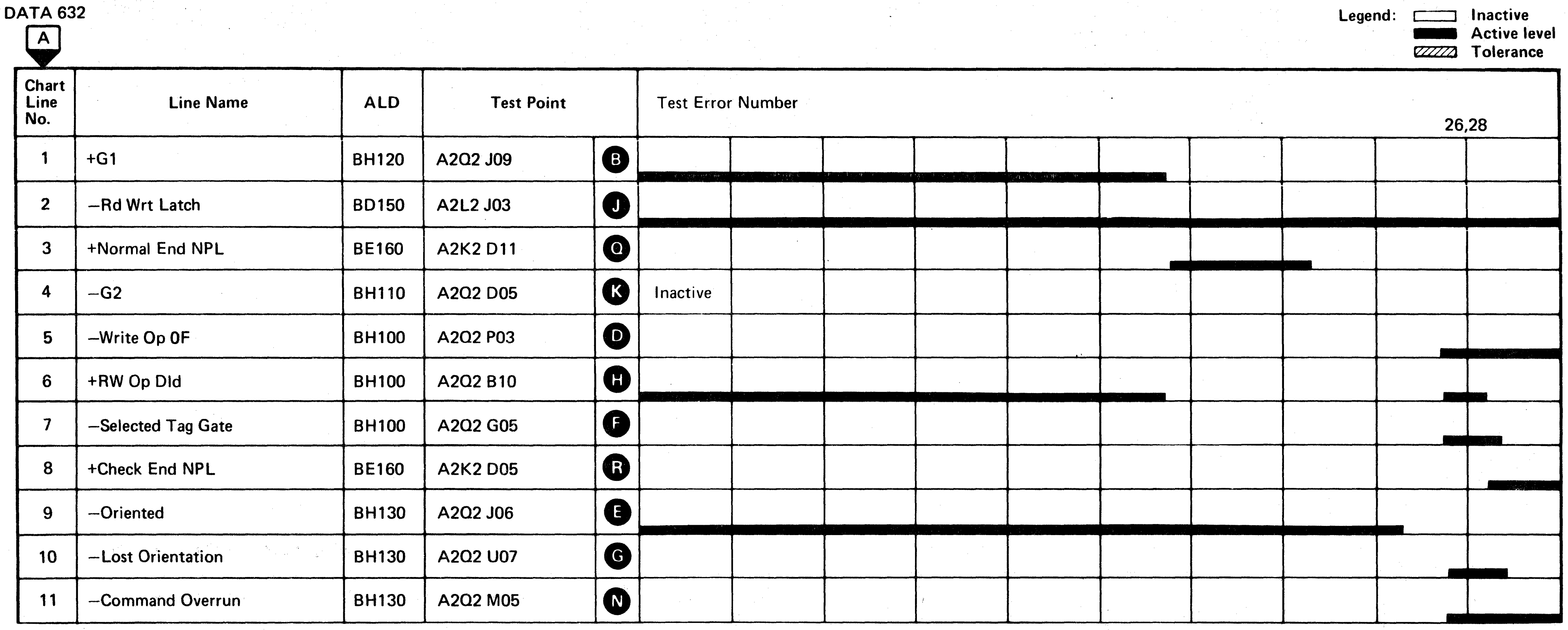


Chart Line No.	Line Name	ALD	Test Point		Test Error Number 26,28
1	+G1	BH120	A2Q2 J09	B	
2	–Rd Wrt Latch	BD150	A2L2 J03	J	
3	+Normal End NPL	BE160	A2K2 D11	Q	
4	–G2	BH110	A2Q2 D05	K	Inactive
5	–Write Op 0F	BH100	A2Q2 P03	D	
6	+RW Op Dld	BH100	A2Q2 B10	H	
7	–Selected Tag Gate	BH100	A2Q2 G05	F	
8	+Check End NPL	BE160	A2K2 D05	R	
9	–Oriented	BH130	A2Q2 J06	E	
10	–Lost Orientation	BH130	A2Q2 U07	G	
11	–Command Overrun	BH130	A2Q2 M05	N	

Line keys reference the diagram on DATA 630.

AF TEST 3 SEQUENCE CHART

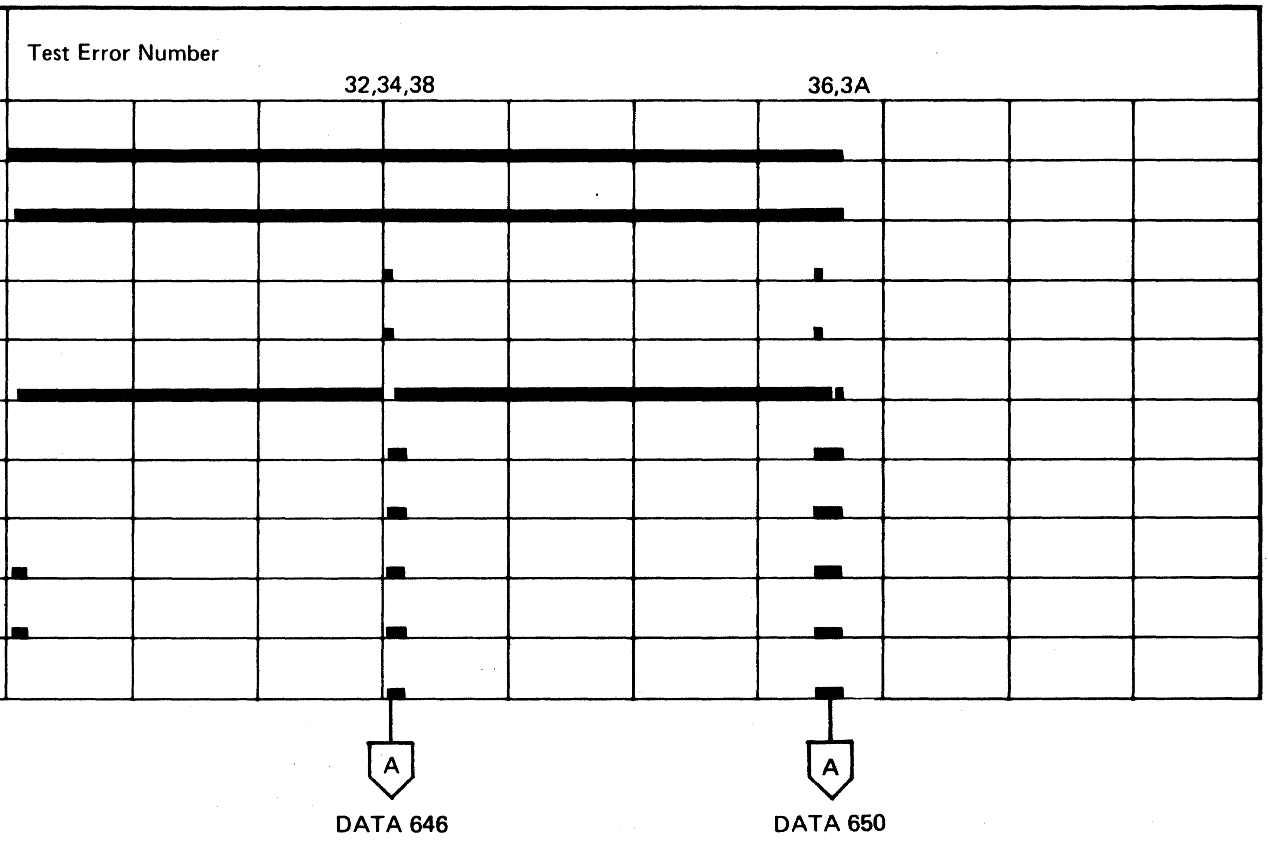
MICRODIAGNOSTIC DESCRIPTION

Routine AF, test 3 continues the Command Overrun tests that were started in test 2. Test 3 attempts a Write G2 and Clock G2 operation during a Home Address (HA) gap. Both operations should produce a Command Overrun indication. The Command Overrun indication then produces the Check End indication. The test Error Numbers are:

Error Number	Description
38	No Command Overrun or Write G2
3A	No Command Overrun or Clock G2
32	No Check End or Write G2
34	No Check End or Clock G2.

Legend: ▭ Inactive ■ Active level ▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	+CE Alert Execute Ind	BD210	A2L2 D13	C
2	−Rd Wrt Latch	BD150	A2L2 J03	B
3	−Phy Index	BH170	A2Q2 S07	M
4	−G2	BH110	A2Q2 D05	K
5	−Selected Tag Gate	BH130	A2Q2 G05	F
6	−Command Overrun	BH130	A2Q2 M05	N
7	+Check Cond	BE140	A2K2 D02	L
8	−Op End	BE140	A2K2 D09	S
9	−Coerce Tag Valid	BE140	A2K2 B10	P
10	+Check End NPL	BE160	A2K2 D05	R



Line keys reference the diagram on DATA 630.

(For expanded sequence chart)

TRIGGERING INSTRUCTIONS

Microdiagnostic Setup

Routine AF, test 3
1. Load AF
2. Enter 10,03,00,00

Scope Setup

Sweep 5 ms/div
Mode Alt or Chop

Ch 1 A2U4D13
+CE Alert Execute Ind

Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind

Volts/div 0.1
Probe x10
Ch 2 (See chart)

3350 | CE0982 Seq. 1 of 2 | 2358835 Part No. | 441303 30 Jul 76

AF TEST 3 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

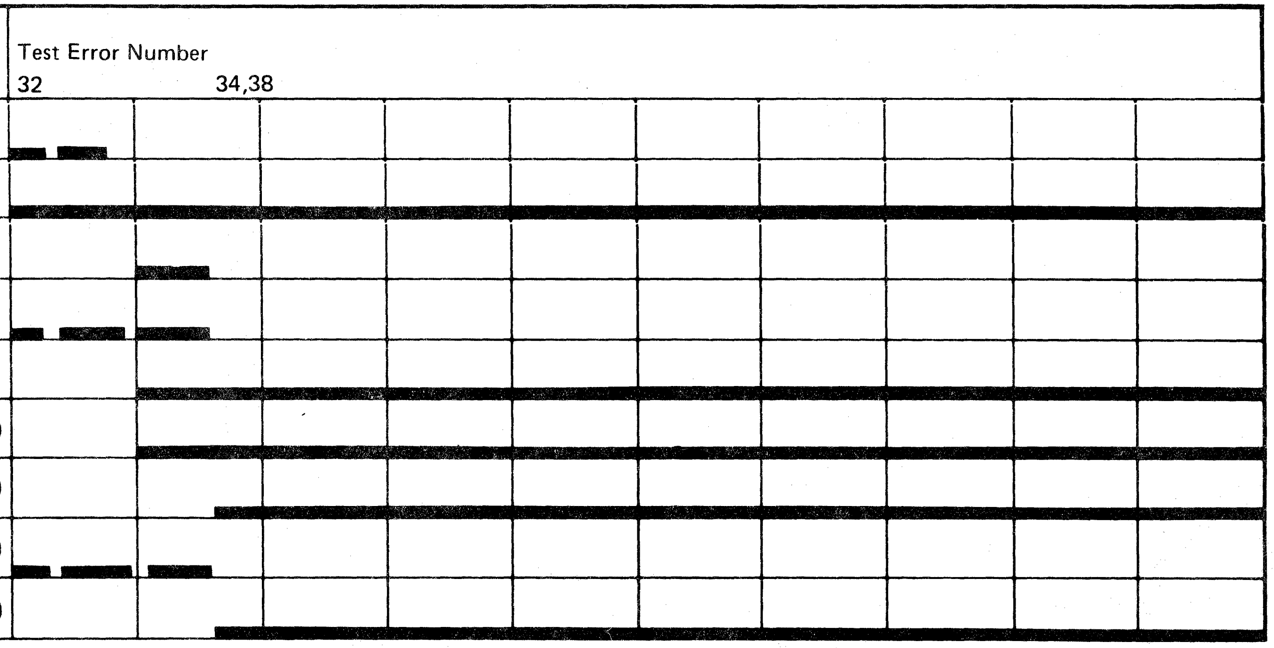
Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (–)
Delay Time - Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 0.3
Source – Int Ch 1

Ch 1 A2Q2S07
Phy Index
Volts/div 0.1
Probe x10
Ch 2 (See chart)

DATA 642
Ⓐ

Legend: □ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point	
1	–Phy Index	BH170	A2Q2 S07	Ⓜ
2	–Rd Wrt Latch	BD150	A2L2 J03	Ⓑ
3	–G2	BH110	A2Q2 D05	Ⓚ
4	–Selected Tag Gate	BH130	A2Q2 G05	Ⓕ
5	–Command Overrun	BH130	A2Q2 M05	Ⓝ
6	+Check Cond	BE140	A2K2 D02	Ⓛ
7	–Op End	BE140	A2K2 D09	Ⓢ
8	–Coerce Tag Valid	BE140	A2K2 B10	Ⓟ
9	+Check End NPL	BE160	A2K2 D05	Ⓡ



Line keys reference the diagram on DATA 630.

AF TEST 3 SEQUENCE CHART

TRIGGERING INSTRUCTIONS

Scope Setup

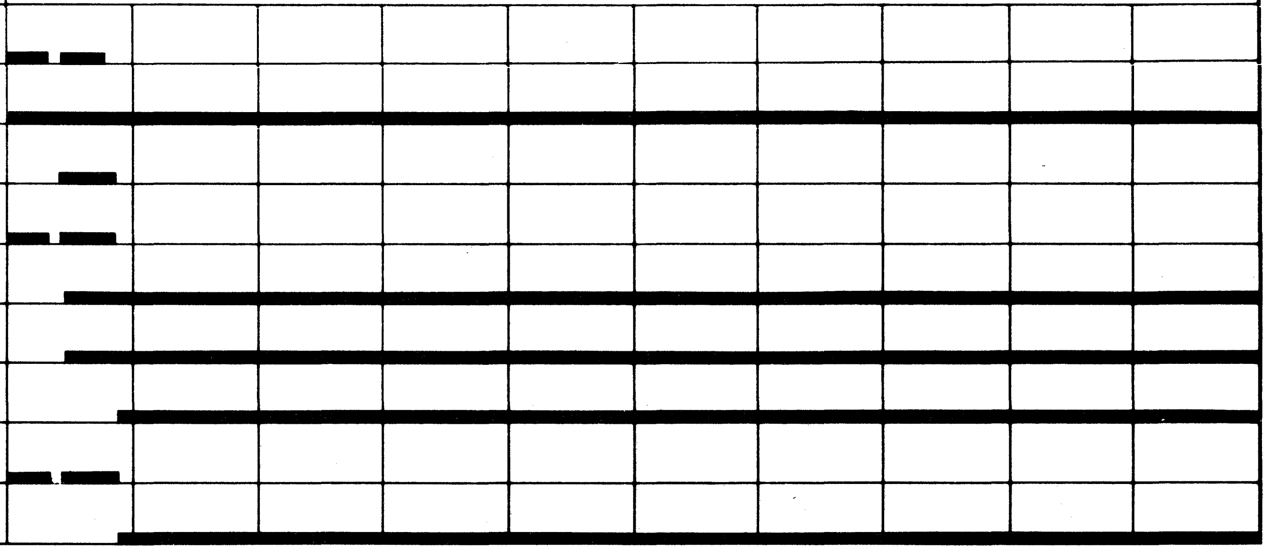
Sweep 5 ms/div
Mode Alt or Chop
Trigger Ext
Slope (+)
A2L2D13
+CE Alert Execute Ind
Horiz Display – Delayed Sweep (B)
B Sweep Mode – B triggerable after delay time
A and B Time/div – 5 ms/div
Slope (–)
Delay Time-Delayed Sweep – 20 μs/div
Delay-Time Multiplier – 3.5
Source – Int Ch 1

Ch 1 A2Q2S07
–Phy Index
Volts/div 0.1
Probe x10
Ch 2 (See chart)

DATA 642
Ⓐ

Legend: ▭ Inactive
■ Active level
▨ Tolerance

Chart Line No.	Line Name	ALD	Test Point		Test Error Number 36,3A
1	–Phy Index	BH170	A2Q2 S07	B	
2	–Rd Wrt Latch	BD150	A2L2 J03	M	
3	–G2	BH110	A2Q2 D05	K	
4	–Selected Tag Gate	BH130	A2Q2 G05	F	
5	–Command Overrun	BH130	A2Q2 M05	N	
6	+Check Cond	BE140	A2K2 D02	L	
7	–Op End	BE140	A2K2 D09	S	
8	–Coerce Tag Valid	BE140	A2K2 B10	P	
9	+Check End NPL	BE160	A2K2 D05	R	



Line keys reference the diagram on DATA 630.

3350	CE0985 Seq. 1 of 1	2358836 Part No.	441303 30 Jul 76				

TROUBLE NOT FOUND

DATA 990 – DATA 996 contains aids for problem resolution where insufficient error information is available to follow the maintenance analysis procedure. It may also be used as an aid in analyzing intermittent errors.

The DATA section describes the controller operations required for the transfer of Read/Write data between the storage control and the device.

READ OPERATION

The drive transfers clock, data, and Index information to the controller where it is analyzed to determine orientation. Once orientation is established, the controller deserializes the data and controls the transfer of the deserialized data over the control interface to the storage control. The controller processes error detection and correction data to determine the validity of the data read and to provide correction information when possible. The controller provides status information at the completion of the operation which indicates the success of the preceding operation (Normal End or Check End).

WRITE OPERATION

The Write operation is normally preceded by a Read operation to establish orientation. The controller requests information from the storage control and receives the information. The information is then serialized by the controller and sent to the drive. The controller creates the error detection and correction information and causes it to be written at the end of each record. The controller creates the gaps that separate and identify the various record components. During Format operations, the controller controls or initiates the erasure of unwanted data.

CIRCUIT DESCRIPTION

Circuit description by card location for the controller DATA section is listed for reference.

A2F2–(BAxxx), Bus In, Bus Out

This card has little effect on the DATA section and contains the following circuits:

- Final Control Interface Bus In Assembler and MST to NPL converter.
- Device Interface Bus In receiver and converter.
- Device Interface Bus Out driver and converter.
- Controller Bus In Parity Checker and generator.
- Device Bus In Parity Checker circuits.

A2G2–(BFxxx), Polling and Selection

This card has limited effect on the DATA section and contains the following circuits:

- Control Interface Bus Out receiver and converter.
- Receivers and converters for various other Control Interface control lines such as Recycle, Response, Sync Out, etc.
- Control Interface Tag Bus receivers and converters.
- Partial operation code decode circuits.
- Address compare and selection circuits.
- Polling and Attention handler circuits.
- Device type code generation.
- The Check latch 1 of 8.

A2K2–(BExxx), Assembler Bus and Response

- Contains a seven-way assembler:

  R/W Status
  Controller Error 1
  Controller Error 2
  ECC Zeros Detected
  ECC Correction bits (ORed with various other data)
  CE Data Bits
  Data Bits

- Generates Controller Check, Normal End, Check End, and Tag Valid.
- Contains the drivers for Control Interface control lines such as, Normal End, Check End, Select Active, etc.

A2L2–(BDxxx), Operation Controls and CE Controls

- Contains the Operation decode, Bus Controls, CE Display.
- Contains the R/W Latch and Device Tag Bus. Controls drivers and converters, Status Monitor Check Latch, and CE Diagnostic controls.

A2N2–(BKxxx), Track Used Counter

- Contains the Track Used Counter and the Track Used Counter Parity Check circuits.

A2P2–(BGxxx), Gap Counter

- Contains the Gap Counter and controls and Gap Counter Check circuits.
- Controls R/W Operation termination and ECC timings.

A2Q2–(BHxxx), R/W Macro Card

- Contains the Read and Write operation decode circuits.
- Checks command timing.
- Establishes orientation.
- Controls:

  Read Gate
  Write Gate
  Address Mark Gate
  Unsquelched

- Processes Index Alert information.
- Provides Status information relative to R/W operations.

A2R2–(BLxxx), Reorientation Counter

- Establishes precise reorientation controls necessary for certain Retry operations.
- Contains the Reorientation Counter Check and the Missing Data Pulse detector.
- Contains the Missing Servo Pulse detector and the Phase Error detector.

A2R4–(BBxxx), ECC Card

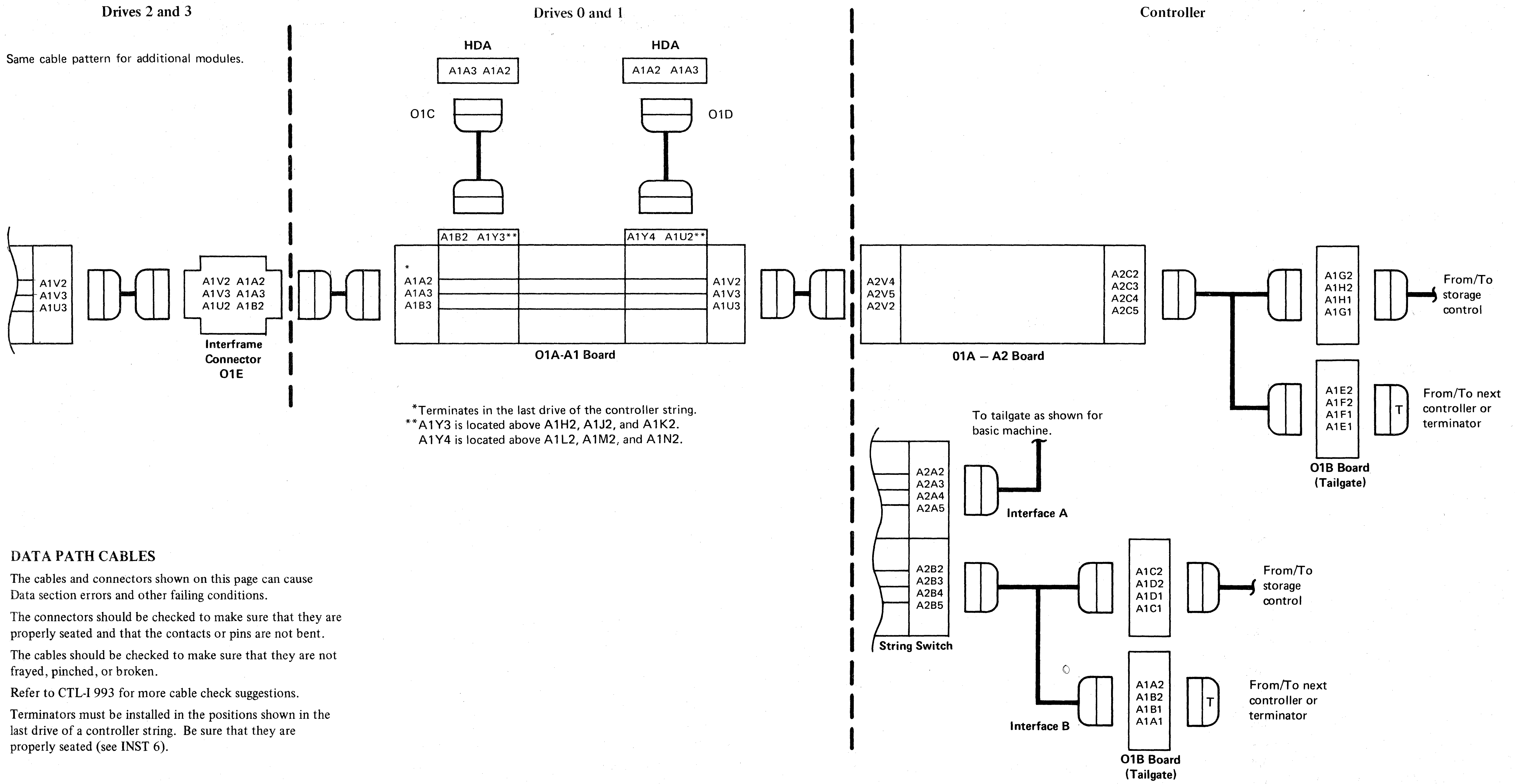
- Contains the ECC Shift register and ECC Zeros detector.
- Provides output for the ECC Hardware Check circuits.
- Contains the ECC Correction Pattern outputs.
- Provides Track Used Counter output gating.

A2S2–(BCxxx), SERDES

- Contains the serializing and deserializing circuits.
- Recognizes Sync Bytes and Address Marks.
- Provides controls and input to the ECC Shift register and accepts output from the ECC Shift register.
- Receives and buffers Write information for the serializer.
- Buffers and transmits data from the deserializer.
- Provides pulses for the synchronization of data between the storage control and the controller.
- Contains the (SERDES) Shift Register Parity Check; Write Data Check, and ECC Hardware Check.
- Contains the Sync Out timing error which is an indication of a Data Overrun.

A2T2–(BJxxx), VFO

- Encodes serial data for recording on the disk.
- Developes the major timing pulses for operating the string.
- Provides the interface for data and servo pulses between the drive and the controller.



*Terminates in the last drive of the controller string.

**A1Y3 is located above A1H2, A1J2, and A1K2.
A1Y4 is located above A1L2, A1M2, and A1N2.

DATA PATH CABLES

The cables and connectors shown on this page can cause Data section errors and other failing conditions.

The connectors should be checked to make sure that they are properly seated and that the contacts or pins are not bent.

The cables should be checked to make sure that they are not frayed, pinched, or broken.

Refer to CTL-I 993 for more cable check suggestions.

Terminators must be installed in the positions shown in the last drive of a controller string. Be sure that they are properly seated (see INST 6).

TROUBLE NOT FOUND

Check the voltage in the controller and the drive in CE Mode as shown in Figures 1 and 2. Exit to the indicated page entry if problems are suspected or further information is required. See PWR 90 for complete voltage check procedures.

Figure 1. Voltage Chart for the Controller

Voltage	Test Point	Tolerance	Maximum AC Ripple	Page Entry
-4V	A2T2 B06	-3.84 to -4.16V	0.04 V p-p	PWR 55, B
+6V	A2T2 G11	+5.76 to +6.24V	0.08 V p-p	PWR 60, A

Figure 2. Voltage Chart for the Drive

Voltage	Test Point	Tolerance	Maximum AC Ripple	Page Entry
-4V	A1C2 (A1T2) B06	-3.85 to -4.50V	0.23 V p-p	PWR 255, A
+6V	A1F2 (A1Q2) B11	+5.76 to +6.24V	0.08 V p-p	PWR 260, A

Voltages are distributed to the A2 Board by several plug-on connectors. Figure 3 contains the test points and connector locations for all of the plug-on connectors on the A2 Board.

Figure 3. Plug-on voltage connector list

Voltage	Test Point	Input Point	Reference
+6	A2F2 B11	A2E2 B11	PWR 60, Entry A
+6	A2D2 S11	A2E2 S11	
+6	A2K2 B11	A2L2 B11	
+6	A2M2 S11	A2L2 S11	
+6	A2T2 G11	A2T2 B11	
-4	A2T2 B06	A2S2 B06	PWR 55, Entry B
-4	A2T2 G06	A2S2 G06	
-4	A2D2 B06	Planar Conn.*	

*Located at the top of the A2 Board.

TROUBLE NOT FOUND

Scope the basic timing pulses to verify proper timing and operation. Load routine B4 and enter: 10, 83, 00, 85, 00, 42, 64, 05, 00, 00, 00, 00, 00, 00, 00, 00, 00. This loop selects the CE drive, sets Read/Write to cause Servo pulses to drive the VFO, delays 200 milliseconds, and then resets Read/Write.

It is critical that the pulses shown have the proper relationship in order to satisfy the timing tests that result in microdiagnostic routine stops that lead to the DATA section. The rise of pulses identified by B must follow the rise of pulses A by 0.835 ± .025 microseconds. The rise of pulse D must follow the rise of pulse C by 1.669 ± 0.05 microseconds.

Index Alert pulses should occur at the rate of one each 16.667 milliseconds or once each disk revolution.

Pulses are measured with times 10 probes that are grounded. All except −Servo In are MST-1 voltages. −Servo In should be 0 Vdc to −0.6 Vdc.

Legend:
☐ Inactive
■ Active level
▨ Tolerance

Scope Setup

Sweep 0.1 μs/div
Trigger A Int
Slope (as shown in chart)
Ch 1 (see chart)

Chart Line No.	Line Name	ALD	Test Point	Sync Slope
1	Raw Servo Data	BJ100	A2T2 G07	+
	Plus Phase shown measured at 30% above minus level.			
2	−Servo In	BJ100	A2T2 D06	−
	Approximately 0V to −0.6V measured at −0.4V level.			
3	−VFO 1F	BJ130	A2T2 D10	−
	Measured at 30% above minus level.			
4	−VFO 2F TP	BJ120	A2T2 B09	−
5	−Half F	BJ130	A2T2 B12	−
6	+Reorient Servo Clock	BL140	A2R2 D13	+

To see the timing relationship: Sync on Int Ch 1 and leave the Ch 1 probe on −Bit Ring 0 Pwr. Use the Ch 2 probe to scope the other Bit Ring lines.

Scope Setup

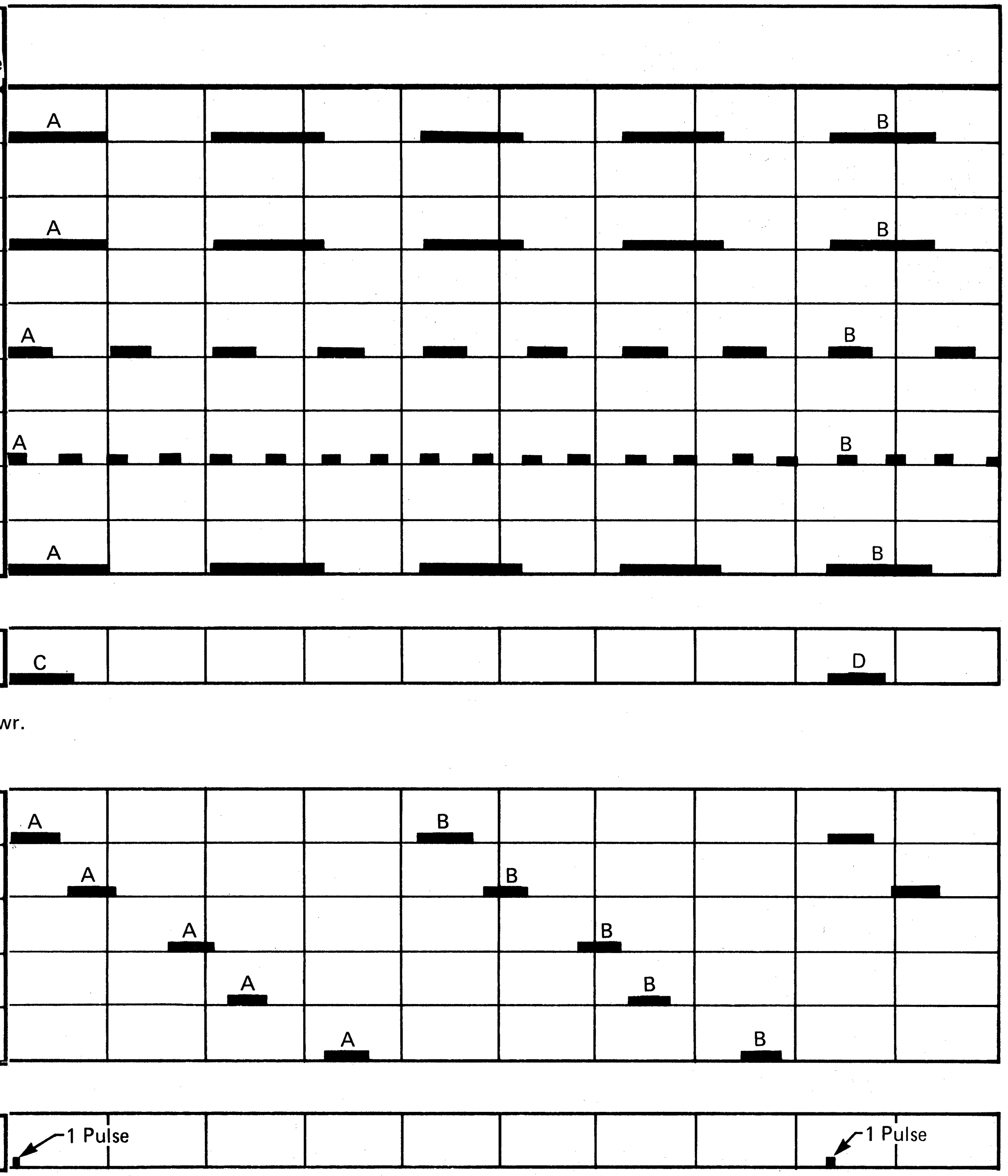
Sweep 0.2 μs/div
Trigger A Int
Slope (as shown in chart)
Ch 1 (see chart)

Chart Line No.	Line Name	ALD	Test Point	Sync Slope
7	−Bit Ring 0 Pwr	BC130	A2S2 D07	−
8	−Bit Ring 1 Pwr	BC130	A2S2 D11	−
9	−Bit Ring 3 Pwr	BC130	A2S2 D13	−
10	−Bit Ring 4 Pwr	BC130	A2S2 D12	−
11	−Bit Ring 6 Pwr	BC130	A2S2 P05	−

Scope Setup

Sweep 2 ms/div
Trigger A Int
Slope (−)
Ch 1 A2Q2J11
Index Alert
volts/div 0.1
probe x10

Chart Line No.	Line Name	ALD	Test Point	Sync Slope
12	−Index Alert	BH170	A2Q2 J11	−



3350	CE0994 Seq. 2 of 2	2358620 Part No.	441300 31 Mar 76	441303 30 Jul 76	441310 27 Jun 80	