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IBM 9020 A SYSTEM PROCESSING AND CONTROL

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Archival notes

Chapter 5 *I/O Operations* was missing from the source document.

This training manual was produced in July 1968 several years before the first operational installation was deployed. The text does not reflect the final 9020 version in several respects. It was still being used as training course material in the late 1970s, long after all the 9020 systems (with a slightly different configuration) were operational.

The handwritten notes are from 1975, and several of them reflect the differences between the 1968 configuration described in the text and what was finally delivered.

Amongst the differences are the following:

At the time the text was written there was only a single 9020 version, hence the reference to just "*9020*" in the title. A second, more powerful, version was added later, namely the "*9020D*". The version described in this text became the "*9020A*".

The text does not mention disks (DASD). These were added later to 9020As and 9020Ds and referred to as Storage Control Units (SCUs). See the handwritten amendment on page 6-64.

The 9020 was originally conceived as a maximum three-CE configuration. The final 9020A version included up to four CEs. The text and diagrams reflect either the three or four CEs maximum configuration in different sections, presumably depending on when that section was written.

The text refers to Large Capacity Storage (LCS) elements. These were deleted from the final delivered configurations.

The Storage Elements (SEs) referred to in the text are the 128 KB Model-03 and 256 KB Model-04. The final 9020A version used 256 KB Model-08 and 512 KB Model-08A SEs.

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CHAPTER 1

GENERAL INTRODUCTION TO IBM-9020 HARDWARE

1-1. GENERAL CONCEPTS OF SYSTEM OPERATION

The IBM-9020 Central Computer Complex is a multi-element data processing system utilized as En Route subsystem of the National Airspace System. Individual elements within the system are interconnected by means of interface cables. The ATC Operational Program is provided with instructions to enable major elements to be combined into a multiprocessing environment without manual intervention. In the normal Air Traffic Control System there will be more elements than are necessary to perform the ATC function. These redundant elements when not active in the ATC program may be used for auxiliary functions such as diagnostic maintenance or data reduction runs. However, these elements are recallable to the ATC problem in the event of the failure of one of the active elements. The recalling of a redundant element to the ATC problem is accomplished under program control; however, it is subject to certain manual conditions that will be more fully covered later in this text.

The elements in the IBM-9020 Central Computer Complex consist of:

1. Up to 4 Compute Elements (CE)
2. A maximum of 3 Input/Output Control Elements (IOCE)
3. Up to 12 Storage Elements (SE)
4. Up to 3 Peripheral Adapters/Modules (PAM)
5. A maximum of 3 Tape Control Units (TCU) with up to 24 Tape Drives
6. 1 or more Card Reader/Punches and High Speed Printers with associated Control Units
7. A System Console with its associated entry typewriters

The number of the various types of elements is determined by the workload and air traffic density of the site at which the installation is to be made; however, any of the smaller sites may be enlarged by the addition of equipment.

The fact that the 9020 computer is composed of elements and the ATC Operational Program is capable of reconfiguring these elements into sub-systems gives rise to the possibility that two or more programs may be simultaneously processed.

To ensure proper operation of the ATC program as well as the subordinate program(s) certain restrictions must be placed on the elements within the system:

1. No element outside the ATC program should be able to communicate with active elements.
2. No active element may drop power except for catastrophic conditions while in the ATC state. Conversely, the dropping of power on an inactive element should not adversely affect the active elements.
3. While active in the ATC program, the manual controls of the elements will be disabled. This would prevent operating personnel from inadvertently interfering with this operation.
4. No single system element failure should impair the system operation. Element failures should be recognized and alternate elements added to replace the failing element.

Figure 1-66 (a foldout at the end of this chapter) is a block diagram of a triplex system. Notice that each of the major elements is cabled and thus is available to each of the other major elements. In the operation of the IBM-9020 Computer there is no inherent master/slave relationship between Compute Elements. Each Compute Element is capable of supervisory (configuration) control over other elements; however, the receiving elements must be conditioned to receive this control. Configuration control has a twofold function in the 9020 System. The first function is that of control within the system. In other words, which Compute Element (CE) has the capability

of conditioning the other elements within the system to accept future control instructions related to configuration. The elements are conditioned by setting what is referred to as a SCON field by a Set Configuration Instruction or by manual operation from the element console. The manual operations permissable from the element console may be limited by associated STATE BITS for the particular element. The second function is to set the Communication Field of each element which controls the communication between elements within a system. It necessarily follows that the Set Configuration Instruction is composed of SCON, STATE, and COMMUNICATION fields. For detailed information on this instruction refer to Principles of Operation (CBB890).

In the established multi-system environment it would not be desirable to limit the flexibility of the various sub-systems by placing restrictions on storage addressing. The 9020 computer has an address translation feature employed. Simply stated, the Address Translation Feature permits any logical storage address to be placed into any physical storage element. This translation takes place automatically once the Address Translation Registers (ATR) are set up. The ATR may be set up either manually or under program control by the Set ATR Instruction.

The storage area used to contain the old and new Program Status Word as well as the Channel Address Word and the logout area may also be relocated by Preferential Storage Base Address (PSBA) circuitry contained within the Compute Element. The Preferential Storage Base Address Register and associated circuitry is activated any time the logical storage address contains high order zeros in address bits 8 thru 19. When activated, PSBAR may relocate the preferential storage area into any one of the 32 available 1024 word blocks within an SE, or upon detection of certain errors, may relocate from one SE to the next configured SE in the system. The Preferential Storage Base Address Register (PSBAR) may be set up manually or by program using the Set PSBA Instruction.

In view of the concepts presented it may be stated that the Compute Element is the focal point of the 9020 System. As such, the CEs are equipped with circuits to permit them to issue control type instructions to the other elements. The CEs also contain circuits to handle the processing of all data and the issuance of all I/O instructions. The control of the I/O devices once started from a Compute Element (CE) is delegated to the Input/Output Control Element (IOCE). Data presented to the system from the I/O devices as well as data presented from the system to the I/O devices is routed to or from storage via the IOCE. Once an I/O operation is completed, the IOCE advises the CE of this by a request for an I/O interrupt. If the CE is so conditioned by the current PSW, the interrupt will take place and the current PSW will be stored as the I/O old PSW. The I/O new PSW will become the current PSW and the system will continue the execution of the program at the new location. Using this scheme, the system will be permitted to operate at an overall higher speed since it is not tied to the slower I/O devices.

The I/O interrupt and subsequent PSW swap are but one way the 9020 System has of changing the operation of the program in response to the external environment. The other interrupts to which the system is capable of responding are: Machine check interrupts which occur when a functional unit detects a malfunction. Program interrupts which occur when the programmer specifies invalid operations, invalid data, or incorrect boundaries. The Supervisory Call interrupt which provides the programmer a method of status switching under program control, and the external interrupt which in general occurs as a result of conditions external to the element. These external conditions may be a manual depression of the interrupt button, certain bits set in the Diagnose Accessible Register (DAR), the timer, or as a result of the read or write direct instruction, etc.

1-2. FUNCTIONAL USE OF COMPONENT ELEMENTS

A. Compute Element

The Compute Element contains the circuits to process the instructions, initiate the I/O operations, and process the interrupts. As a result of its capabilities to perform these functions, the CE is capable of exercising control on the remaining elements in the system.

B. I/O Control Element

The I/O Control Element through its channel circuits is capable of controlling the data flow from the I/O devices to storage and from storage to the I/O devices. The IOCE is also capable of accepting I/O instructions from a CE and in response to these initiating the request operation. It is also capable of accepting system control (reconfiguration) type instructions from appropriate CEs. Since all system operations require some form of input and some form of output, the IOCE for purposes of testing may be operated as a stand alone computer (Diagnostic Mode). To this end the IOCE has its own internal storage area (MACH) which may be utilized. In system operations MACH store is used only for certain Channel Operations; while in the diagnostic mode, MACH store may be used as data storage also. MACH store is 8K words in size; however, the top 1024 words are reserved for Channel. Since in system operations the IOCE controls the I/O devices, it must also be capable of advising the CE of their status. To accomplish this the IOCE has circuits to request the I/O interrupt.

C. Storage Element

The Storage Elements act as the medium for storing data and instructions necessary for the operation of the program. This storage functions to make the data readily available from any address in the same time required to access any other address (Random Access). To accomplish this task, the SE contains circuits to store and/or fetch information in response to requests

from either a CE or an IOCE on a priority basis. The SE also contains circuits to accept configuration information from appropriate CEs. The Storage Element contains core arrays capable of storing 32,768 words (32K) each containing 32 data bits plus 4 parity bits. It might be advantageous at this point to answer the following questions: When and for what purpose does the Compute Element (CE) access storage? For what purpose does the IOCE access storage? In the first instance the CE must access storage in order to get the next or future instructions it is to execute and in processing that instruction, the CE may need to access storage for the data that is to be processed. In the latter case the IOCE must access storage when handling the I/O operations, either to store incoming data or to fetch out going data.

D. Peripheral Adapter Module

The Peripheral Adapter Module was designed to permit the interfacing of non computer oriented devices to the 9020 System. The PAM is composed of the common circuitry to connect itself to the IOCE channel as well as adapter circuitry to connect itself to the devices. The PAM also has circuits to permit its control from one or more of the System's CEs.

E. The System Console (SC)

The System Console (SC) is the central monitoring and control position in the 9020 System. This console is divided into four functional parts:

1. Operator's Control
2. Maintenance Controls
3. Monitor-Displays
4. Emergency Power-Off

All critical console functions are duplicated elsewhere in the System in the event the System Console is inoperable. The System Console is addressable in the same manner as other input/output devices. This allows the ATC operational program to communicate with the System Console to read or supply

various indications of operations. These features provide part of the monitoring functions. Several important functional operations associated with the active system may be controlled from the System Console. By means of select switches and pushbuttons the operator may cause initial program loading, manually enter or display information in the active system, or assist the ATC operational program in accomplishing the overall system tasks. The System Console also contains the circuitry for control of the 1052 Console Typewriter.

F. Other Input/Output Control Units

In addition to the remote I/O devices which are serviced through the Peripheral Adapter Module, there are two remaining control elements which are found on the computer floor. These include the 2821 (Integrated Control Unit) which is used to control the High Speed Printer (1403) and Card Reader/Punch (2540), and the Tape Control Unit (2803) which is used to control the tape drives.

1. Integrated Control Unit (2821)

This Control Unit contains the control and buffer circuitry to transmit information between the associated system channel and the Card Read/Punch device and the High Speed Printer. Within the Control Unit are areas of storage (buffer) that permit high-speed transfer of information between the IOCE and the input/output devices. This arrangement provides for more efficient time-sharing of the I/O interface since the channel is not restricted to the slower-speed operations of input/output devices. For example, in a cardread operation the information from the card is loaded into a buffer in the 2821 Control Unit. This loading proceeds at card-reader speed. When the channel is ready to accept the data, it is transferred from the buffer via channel to the storage unit at a rate that is not dependent upon reading time in the card reader.

2. Tape Control Unit

The basic purpose of a Tape Control Unit is to adapt high-speed, electronic data channel circuits to control a mechanical tape unit. To accomplish this, Tape Control Units are logically divided into high-speed channel interface circuits and low-speed tape unit controlling circuits. Interface circuits include all of the functions needed to communicate with the channel while the control section provides timed control signals to operate the Tape Unit. Data transmitted from the channel to the Tape Control Unit is handled at electronic speed on the channel interface lines. The control unit holds each byte of data until the Tape Unit is ready for it. When data is transmitted to the channel, each byte from the Tape Unit is held in the control unit until the channel interface accepts it. As data is transmitted through the Tape Control Unit, it is checked for errors. If an error occurs, the interface adapter circuits inform the data channel at the end of the operation.

1-3. PREINSTALLATION PLANNING

The following is a general discussion of requisite planning for the IBM-9020 Central Computer Complex.

A. Building Requirements

When locating the IBM-9020 System, consideration should be given to the following items:

1. Availability and location of proper and adequate power.
2. Space to house air conditioning equipment.
3. Ceiling height, outside wall area, and glass area.
4. Work flow to other areas.
5. Operational considerations in connection with other ATC functions.
6. Floor loading capacity.

The floor area required for this system will be determined by the flight configuration and allowances for future expansion. Space should be provided in the area of the IOCEs for storage of FLT documentation which will be constantly referenced during maintenance. Space may also be needed for FSPC Modules, CUE Adapters, teletype equipment, storage cabinets, card files, work tables and desks, and printer form stands as well as other punched card equipment.

Such items as permanent master document files, card files, and magnetic tape files require different types of storage areas and should be carefully planned to minimize both the amount of space necessary and the travel time between areas.

A substantial amount of test equipment will be assigned to the installation to maintain the system. Equipment such as tape drives and 1052's may be moved into the Maintenance Room, depending upon the type of work to be done. These areas should be on the same floor level. The Maintenance Room should contain a minimum of 400 square feet of space, be at least 12 feet wide, and be air conditioned to the same specifications as the machine room. Air conditioning should be sized to include the heat load of at least one oscilloscope and magnetic tape unit.

1. Equipment Layout

Included in this manual are plan drawings which show the clearances required to allow working room for the field engineer and his equipment. They also show the swinging radii of the component gates and machine covers, caster and cable hole locations. All dimensions are with covers installed. In some cases, clearances may be overlapped as long as the larger clearance is maintained. The gate swing of an auxiliary unit must not interfere with the gate swing of its corresponding control unit.

The units must be located so that the length of connecting cables will not exceed maximum limits. In the interest of best electrical design, all cable

lengths should be kept as short as possible. In the "Cabling" section, the cabling connections between units are illustrated, and the length limitations for the system are given. The limits given are center-to-center lengths between cabling access holes at the floor line; allowances will be necessary for false floor height and cases of indirect cable routing.

The final layout must be reviewed to ensure that cable limitations have not been violated and that proper clearances have been maintained. After the cables have been ordered, any layout changes that affect cable length will require an engineering change and may result in delays. Procurement and installation arrangements for external cables should be made with sufficient lead time to permit the cables to be installed prior to delivery of the computer system.

In laying out a system, the following points should be taken into consideration:

1. There should be visual access between a control unit and at least one of its associated I/O devices.
2. The 7265-02 System Control Console is the central unit of operation; it should be so considered when planning the layout.
3. The 2540 Card Reader Punch and 1403-2 Printer should be convenient to the console operator.
4. The fronts of the magnetic tape units should be visible from the 7265-02.
5. The control panels of the 7201-01 Computing Elements should be visible from the 7265-02.
6. Adequate working area is required around the console and magnetic tape units.

IBM will provide a scaled layout of equipment which will be installed in the Maintenance Room to be used as a guide in locating such items as receptacles and lights. The room should contain both 115-volt and 208-volt outlets adequate to repair any unit that can be serviced in the Maintenance Room. Following is a list of typical furniture and fixtures to be located in the Maintenance Room and their dimensions in inches.

Item	Length	Width	Height
Desk	45	34	29
Work Bench	72	30	35
Shelf Cabinet	36	18	72
Parts Cabinet	42	24	87
File Cabinet	18	28	60
Bookcase	33	15	42
Study Table	60	30	29
Book Cart	40	13	31
Card File	17	24	9

A typical Maintenance Room Layout is shown in Figure 1-1.

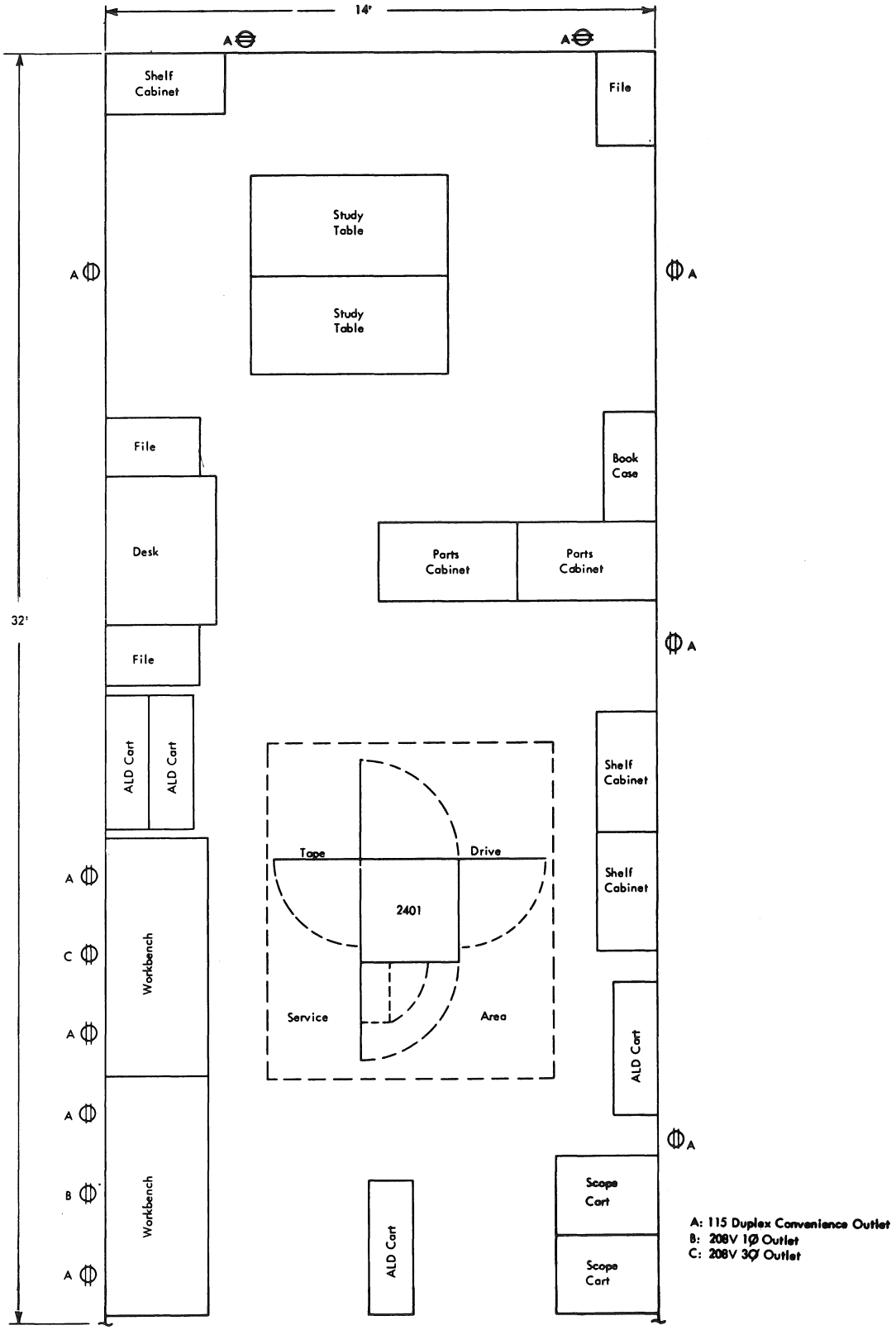


Figure 1-1. Typical Maintenance Room.

2. Floor Construction

The weight of each unit is listed in the "Unit Specifications" section. The unit and floor loading weights in the following listing are given on an element basis and for the expected grouping of units.

Unit	Quantity	Weight (lb)	Average Floor Loading (lb/sq. ft.)
2803-1	1	1,400	31
2821-1	1	1,000	29
2540	1	1,050	23
1403-2	1	750	22
2401-2/3	1	800	29(1)
2401-2/3	4	3,200	47(2)
7265-02	1	1,850	13
7289-02	1	3,850*	32(3)
7289-02	1	4,200*	35(4)
7231-02	3	15,600	43(5)
7201-01	1	4,000	40
7251-03	1	1,500	16
7251-04	1	2,650	24(6)
7251-04	3	7,950	26(7)

*Weight will be determined by Adapter Configuration for each site

NOTES:
1. Tape drives when located singly.
2. Tape drives in groups of 4.
3. NAFEC PAM.
4. JACKSONVILLE PAM.
5. I/O CE's butted in a group of 3.
6. Storage Element when located singly.
7. Storage Elements when butted in a group of 3.

Floor loading is distributed by the use of 3.25-inch-diameter leveling pads. Four of these pads are included with each shipping section (see plan views) to distribute the floor loading across 33.2 square inches. The center of gravity is located as close to the geometric center of each frame as possible for even distribution of floor loading. Leveling pad locations are included in the plan views. Factors considered in determining average floor loading are as follows.

1. If more than three units are placed side by side, no allowance can be taken for side clearances at the ends of the machine.
2. Regardless of the actual service clearances required, clearances used in floor loading computations cannot be more than 30 inches in any one direction from the machine.
3. Twenty pounds for each square foot of service area used in calculation must be applied as live-load in floor loading computations.
4. Ten pounds for each square foot of total area used in calculation must be applied as false-floor weight.
5. The weight of cable must be considered. Cabling within the 9020 System is accomplished almost exclusively through the use of 20 conductor coax cables. This cable averages approximately 7 ounces per foot, including connectors.

   NOTE: The listing above does not include cable weight, which cannot be calculated until the equipment configuration is selected and cable lengths determined.

The system concept is such that false floors are an absolute requirement. The false floor will also accomplish the following major objectives:

1. Allow future layout change with minimum reconstruction costs.
2. Provide better working area (covers interconnecting cables and power receptacles).
3. Contribute to personnel safety.

A false floor can be constructed of steel, aluminum or fire-resistant wood. The 24-inch-grid, free-access, pedestal-supported type floor, as illustrated in Fig. 1-2, offers advantages over the stringer-supported type floor illustrated in Fig. 1-3; cable installation and relocation is much less time-consuming without subframing.

IBM recommends that there be no metal exposed to the walking surface where a metal raised floor is used. Such exposure is considered a safety hazard.

When selecting a raised floor covering, consider such factors as the frequency of moving machine units and the resistance to cracking and flaking, appearance, and cost of the tile. Experience has shown that a material such as vinyl tile is most applicable because of its resilience and its resistance to cracking and flaking. Materials used in the underfloor area should be treated to prevent the generation of dust.

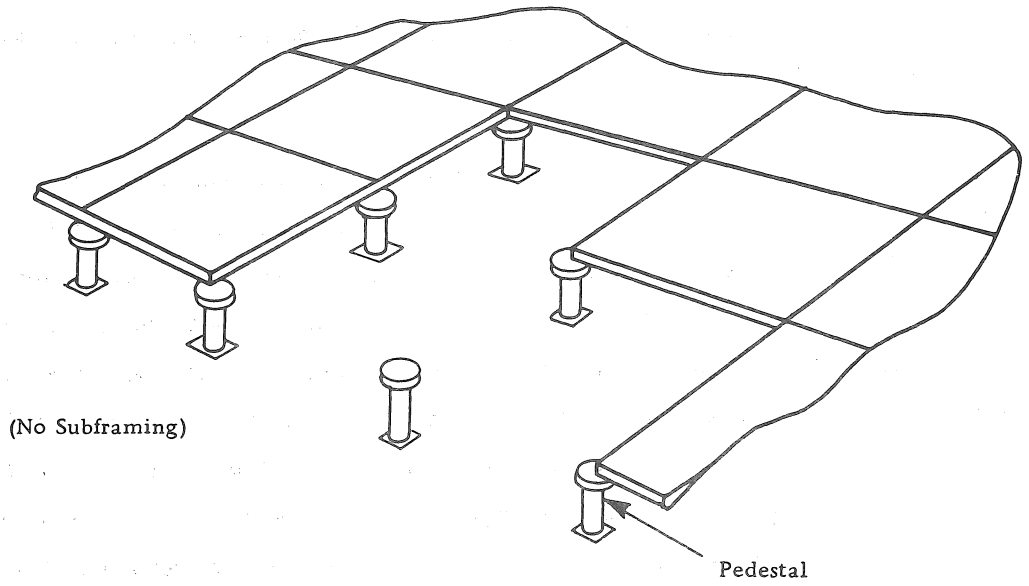


Figure 1-2. Pedestal-Supported Type Floor.

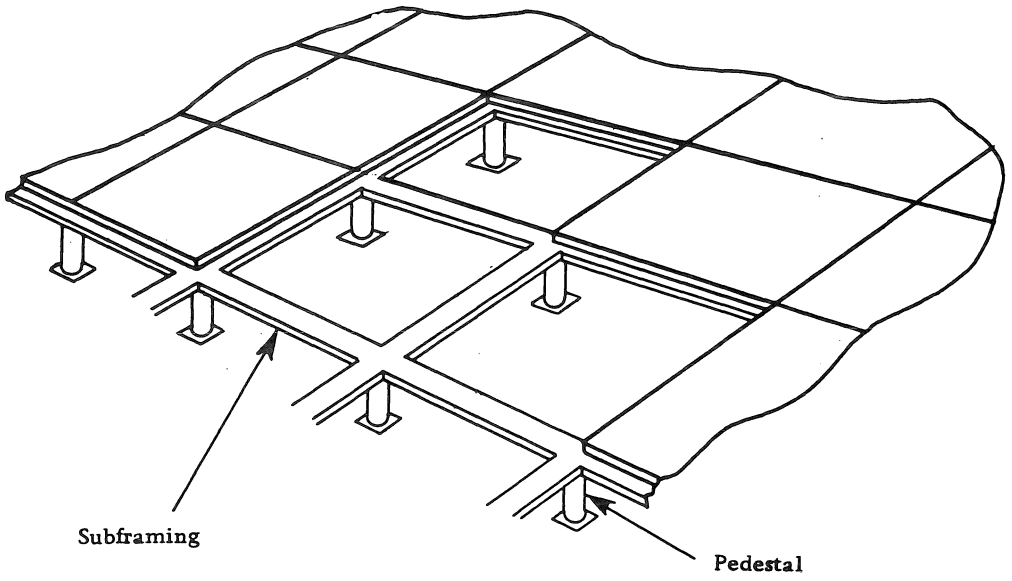


Figure 1-3. Stringer-Supported Type Floor.

3. Acoustical Treatment

The principal noise sources in this system are the mechanical units, such as card machines, printers, and blowers.

The floor construction should be such that vibration to other areas is minimized. The walls should be constructed so as to prevent the transmission of noise to the adjacent area. It is important that these walls be constructed from the floor to the base ceiling and properly sealed. The doors must also have a good seal. Wall surfaces should be made soft to prevent reverberations. (The importance of this feature diminishes as the room size increases.) The greatest sound reduction will be obtained by properly treating the ceiling. Best results can be expected from a dropped porous ceiling. If overheat duct work exists, noise generated in the machine room may be transmitted to other rooms unless proper precautions are taken.

4. Lighting

A minimum average illumination of 40 foot-candles measured from 30 inches above the floor should be maintained in the general machine room area. Direct sunlight should be avoided because a level of illumination lower than that of direct sunlight is necessary for observing various console and signal lamps. The lights for general illumination should be sectionally controlled by switches so that portions of the lighting can be turned off as desired.

5. Vibration

It may be necessary to install the 9020 System in an area that is subject to minor vibrations. The intensity of vibrations in an office environment will not effect the reliable operation of the 9020 System.

6. Tape Storage

The relative humidity and temperature of the storage facilities for magnetic tape should be maintained as follows:

- Heavy Duty Tape: relative humidity, 20 to 80 percent; temperature, 50 to 90° F.

  Mylar* Tape (long-term storage): relative humidity, 20 to 80 percent; temperature, 50 to 90° F.

Tape exposed to atmospheric conditions outside these limits will require reconditioning before it is used. This is accomplished by placing the tape in the correct operating environment for a length of time equal to the storage time (up to maximum reconditioning period of 24 hours).

The tape should be stored in a dust-proof container in a vertical position and should never be allowed to come into contact with magnetic material at

*Trademark of E. I. duPont deNemours Company, Incorporated

any time. Magnetic fields of greater than 50-oersted intensity can cause loss of information or introduction of noise on tape.

When magnetic tape is shipped, each reel should be sealed in a plastic bag and packed individually in stiff cardboard shipping boxes. These may be obtained from IBM.

B. Air Conditioning

The components of the machines are internally cooled by air circulated by blowers in most units. The air intake varies slightly from one unit to another, but in general, is through the bottom and also through louvers along the bottom edge. One inch dust filters are included at each air input. Warm air exhausts from the top of each unit.

To determine the air conditioning capacity necessary for an installation, the following factors must be taken into consideration:

> Machine heat dissipation, personnel, latent load, fresh air introduction, infiltration of heat through outer walls, ceiling, floors, door openings, partitions, glass wall area, and possible reheat.

1. Temperature and Humidity Requirements

Individual units may require special consideration and/or have more restrictive requirements. See unit specification pages for individual requirements.

A. Machine power ON:	Operational Period
Temperature	60-90°F
Relative Humidity	20-80%
Max Wet Bulb	78°F

B.	Machine power OFF:	Non-operational Period
	Temperature	50-110°F
	Relative Humidity	8-80%
	Max Wet Bulb	80°F

THE RECOMMENDED DESIGN CONDITION FOR THE INSTALLATION OF THESE COMPUTER SYSTEMS IS 75°F AND 50% R.H. In areas where it is not feasible to maintain 50% R.H., a design condition of 40-45% should be used.

THE AREA MUST BE AT THE CONDITIONS FOR THE OPERATIONAL PERIOD BEFORE MACHINE POWER IS TURNED ON.

Under all conditions of operation, the machine input air and room air should not exceed 90°F. This is a maximum operating temperature and should not be considered a design condition. System ambient barometric pressure limits are sea level to 7,000 feet operating and no altitude limit when not operating.

When conditioned air is supplied to the base of any unit by means of an under floor duct or plenum chamber, the relative humidity in the duct should not be greater than 80%. This specification is an absolute maximum. Air temperature in this duct should be kept above room dew point temperature to prevent condensation within or on the machines. When it is necessary to add moisture to the system for control of low relative humidity, one of the following methods should be used:

1. Steam grid or jets.
2. Steam cup.
3. Water atomizers.

NOTE: In localities where the outside temperature drops below freezing, condensation will form on single glazed window panes. Also, if outside temperatures are considerably below freezing, the outside walls of the building should be waterproofed or vapor sealed on the inside, or in time, structural damage will occur in outside walls.

2. Air Filtration

A high efficiency filter rated according to the following specifications should be installed to filter all air supplied to the computer room.

Mechanical and electrostatic air cleaners operate on two entirely different principles. Therefore, it is necessary to specify a different efficiency rating for each type.

Mechanical Air Filter: This type must be rated at a minimum of 20% efficient by the Bureau of Standards discoloration test using atmospheric dust. This rating applies to a clean filter and must be maintained throughout the life of the filter.

Electrostatic Plate Type Filter: This type must be rated at a minimum of 85-90% efficient by the Bureau of Standard discoloration test using atmospheric dust. Electrostatic air cleaners are designed to operate at 85-90% efficiency at a given face velocity. As you increase the face velocity through an electrostatic filter, its efficiency decreases. Therefore, an electrostatic filter operated an increased face velocities or below 85% efficiency would allow a greater number of particles charged by the ionizing wires to pass through the plate section and enter the room. This would increase what is known as space charge. As the space charge increases, a greater voltage differential occurs between the positive charged particles and the negative surfaces in the room. This causes dust to accumulate rapidly on all surfaces, defeating the purpose of a high efficiency filter.

Special air filtration is necessary only where installations are exposed to corrosive gases, salt air or unusual dirt or dust conditions.

3. Air Distribution and Types of Systems

Even though the heat loads of the computer system are considerably reduced from previous systems, the heat load is concentrated in a relatively small area. For this reason careful attention should be given to the method of air distribution to eliminate areas of excessive air motion.

Several different types of air conditioning systems can be designed to satisfy the temperature and humidity requirements. The following are the most common types of systems in use with a brief description of each. In no case should these descriptions be considered complete, and the use of an experienced air conditioning design engineer is strongly recommended. All local building codes should be checked including the electrical code, as some localities will not permit the use of the raised floor as an air conditioning plenum as described in the following.

a. Single Duct - Overhead System

In this system the entire heat load of the room including the heat generated by the computer system, is absorbed by the air supplied to the machine room. The air is generally supplied from either an overhead duct and diffuser system or by means of a ceiling plenum.

The return air to the air conditioning unit is taken from either ceiling return registers located above the heat producing units, or a fixed pattern of returns both in the ceiling or on the walls around the periphery of the room.

The temperature control system would consist of temperature and humidity controls placed in a representative location within the machine room. A temperature and humidity recorder (discussed in detail later) would be mounted adjacent to the controls to monitor the room conditions.

b. Two Duct - Two Air-Conditioning-Unit System

One air handling unit with separate controls supplies conditioned and filtered air to the air inlets on the machines. This air may be supplied to the machines through ducts laid beneath the raised floor or fed to a floor plenum chamber with holes through the floor located under the machines. Each machine is supplied with a quantity of air equal to its internal fan capacity. This air absorbs the heat generated by the machine and is discharged from the top of the units into the room. Relative humidity of the air supplied to the units should be maintained below 80% and temperatures should be controlled to prevent condensation on or within the units.

To insure a controlled relative humidity, it will be necessary to provide for a reheat system to operate in conjunction with the cooling unit. This unit is basically a sensible cooling operation.

The second air handling unit supplies air directly to the room through a separate duct system and should be large enough to absorb the remaining heat load in the computer area. It should be capable of maintaining room temperature and relative humidity as specified in this manual and give complete year-round air condition, ventilation and heating.

This system should use predominantly recirculated air with a set minimum for introduction of fresh air for personnel. This minimum fresh air introduction will enable the machine area to be pressurized so that air leakage is always outward. This will help prevent dust entry from adjacent areas.

c. Two Duct - Single Air-Conditioning-Unit System

This system is similar to the preceding system except in one respect: this system uses only one air handling unit to supply both air circuits. The air is filtered and the temperature and humidity regulated before it is delivered to the room and the individual units through separate ducts.

A split coil with reheat and/or face and bypass dampers can be used to regulate the air to be supplied directly to the individual unit. Relative humidity of this air should be maintained below 80% and temperature should be controlled to prevent condensation on or with the units.

The temperature control system for the air being supplied to the overhead system would be the same as for the single duct system. In addition, a control system would have to be installed in the discharge duct to regulate the air supply to the underfloor system. The controls would operate either the separate cooling and reheat coils or the face and bypass dampers to maintain the require conditions. A remote reading temperature and humidity recorder should be installed with the sensing elements in the discharge air to the underfloor system to monitor the air entering the machine units.

d. Underfloor System

In this system the space between the regular building floor and the raised floor is used as a supply plenum. All air is discharged into the room through floor registers around the perimeter of the area. The air is returned to the air conditioning unit by means of ceiling registers located directly above the machine units.

A higher return temperature can be used in this system without affecting the design conditions of the over-all room. The design of this system takes into consideration a heat transfer factor through the metal floor. This affords a certain amount of reheat to control R.H. of air before it enters the room.

The temperature control system would consist of the same controls as described for the single duct system. In addition, the system must have controls of air temperature in the underfloor supply system to prevent an uncomfortably cold floor. Air entering the machine through the cable holes must be within stated machine specifications.

The air conditioning load should not be supplied from the same transformer that supplies the computer system.

e. Temperature and Humidity Recording Instruments

It is recommended that all customers install temperature and humidity recording instruments. Recording instruments are necessary to provide a continuous record of temperature and humidity conditions in the machine area. Also, if the air conditioning requirements are not met, a record is available to indicate the extent and duration of the undesirable condition and indicate whether a drying-out period is required. This may, in some cases, save machine shut-down time.

The record of temperature and humidity can be used:

1. To assure the customer that his air conditioning installation is continuously performing its job properly. Installation errors and loss of efficiency due to malfunction of some part of the air conditioning system can be quickly detected.
2. To determine if a mandatory drying-out period is necessary when humidity limitations are exceeded. The drying-out may be necessary if the excess humidity occurs either during periods of actual machine operation or during periods when the machine is shut down and unattended. The extent and duration of the excess humidity is used to determine the duration of the drying-out period.
3. To determine if the environment in the area meets the requirements of the drying-out period.

A visual or audible signal device should be incorporated into the instrument. Its purpose is to provide a visual or audible indication that the temperature or humidity conditions in the computer area are nearing the maximum limitations stated in this manual. Action can then be taken by the customer's personnel to correct this situation.

Direct-reading instruments with a 7-day electric-drive chart should be used for all installations to monitor the ambient room conditions. The recorder should be located at a representative location within the room and adjacent to the control devices.

For use in monitoring the underfloor air conditions, a remote indicating instrument is recommended. This should also have a 7-day electric-drive chart and can be the wet and dry bulb or electronic type if direct reading is not available. The recording instrument can be located on the wall in the room or in the mechanical equipment room or any other location convenient to the building engineer.

C. Safety and Fire Precautions

Safety is a vital factor in planning for a large computer installation. This consideration is reflected in the choice of a computer location, building materials used, fire prevention equipment, air conditioning and electrical systems, and personnel training.

1. Locating a Computer Area

The computer area should be in a noncombustible or fire resistive building or room.

The computer room should not be located above, below, or adjacent to areas where inflamable or explosive materials or gases are stored, manufactured, or processed. If the customer must locate near such an area, he should take precautions to safeguard the area.

2. Structural Safety

Walls enclosing a computer area should be of noncombustible materials wherever possible. These walls should extend from floor to ceiling. If walls are made or combustible material they should be protected as prescribed by code.

If a computer area has one or more outside walls adjacent to a building that is susceptible to fire:

Installation of shaterproof windows in the computer room would improve the safety of personnel and equipment from flying debris and water damage.

Sprinklers could be installed externally over the windows to protect them with a blanket of water in case of fire in the adjacent area.

Where a false (or hung) ceiling is to be added it should be of noncombustible or fire-resistant material. All ducts and insulating materials should be noncombustible and nondusting. If combustible materials are used in the space between the regular ceiling and the false ceiling, proper protection should be provided.

A raised floor, installed over the regular floor, should be constructed of noncombustible or fire-retardant materials. If the regular floor is of combustible material, it should be properly protected from the ceiling below, preferably by water sprinklers. (Note: Before the computer is installed, the space between the raised and regular floors should be cleared of debris. Also, this space should be periodically checked after installation, to keep it free of accumulated dust and possible debris.)

The roof or floor above the computer and tape storage areas should be a watertight slab. If practical, the walls of the room should be sealed to the slab in such a manner as to prevent water entering from above.

3. Type of Fire Prevention Equipment in a Computer Area

Portable carbon dioxide fire extinguishers of suitable size (15 pounds) and number should be provided in the machine room. This is the recommended nonwetting agent for electrical equipment (Class C Hazard). Extinguishers should be overhead, marked, and readily accessible to individuals in the immediate

area. Local codes govern the frequency of inspecting the cylinders, which is done by weighing for dissipation of contents.

Where portable carbon dioxide cylinders are used as the primary extinguishing agent, it is advisable to locate a standpipe or hose unit within effective range of the computer area as a secondary extinguishing agent for a Class A Hazard.

In some cases, local building codes and ordinances, or insurance regulations, require automatic water sprinklers. One of the following should be used, if it conforms to such codes and ordinances:

> Pre-action sprinkler system. High temperatures actuate heat-sensitive devices, which open a control valve. This valve, located outside the room, admits water into the sprinkler piping before the sprinkler heads operate. This type of system minimizes the possibility of accidental discharge of water due to failure or mechanical breakage of the automatic sprinkler heads.
>
> Higher temperature sprinkler heads. Replace the sprinkler heads with high-rated ones (preferably in the intermediate range of 175°F rating).

A fire detection system should be installed to protect the computer and tape storage areas. This detection system should actuate an alarm and shut down the air conditioning system.

4. Data Storage

Any data stored in the computer room -- whether in the form of magnetic tape, paper tape, cards, or paper forms -- should be in enclosed metal cabinets or fire-resistant containers.

For security purposes or for maintaining duplicates of master records, a separate storage room should be used. This room should be of fire-resistant

material and contain the same type of fire prevention equipment as described in "Type of Fire Prevention Equipment in a Computer Area".

5. Supporting Facilities

a. Air Conditioning Systems

In most installations, the computer area is controlled by a completely separate air conditioning system. In these cases, an emergency power-off switch should be placed in a convenient location, preferably near the operating console or next to the main exit door. Fusible-link dampers should be located at fire walls and at places as prescribed by local code.

Where the regular building air conditioning system is used, with supplemental units in the computer area, the supplemental units would then be handled as stated above. The regular building air conditioning system should have an alarm in the regular building maintenance area to alert the maintenance personnel of an emergency. Air ducts serving other areas but passing through the computer room should contain fusible-link dampers at each wall of the computer room.

The air filters used as part of the air conditioning system should contain noncombustible material.

b. Electric Systems

The main line breaker for the computer equipment should be pushbutton operated. This pushbutton control should be in a convenient location, preferably near the operating console and next to the main exit door. A light should be installed to indicate when power is on.

Some local codes require a special battery operating lighting unit that will automatically illuminate an area in case of power or lighting circuit failure.

These units are wired to and controlled by the lighting circuit. Even when not required by code it is recommended that such lights be installed.

Protection against lightning surges can be obtained by installing lightning arresters on the secondary power source, especially when:

The utility company installs lightning protectors on the primary power source.

Primary power is supplied by an overhead power service.

If power receptacles are located under the false floor which could be susceptible to excessive water, waterproof connectors should be used. Proper drainage will guard against flooding or trapping water under the false floor in the computer room. This is important in certain new buildings where the regular floor is depressed and the raised surface is on the level of the adjacent areas.

6. Preplanning to Continue Operation in an Emergency

The continuous operation of a customer's computer is dependent on information stored on cards, tape, etc. Duplicate or master records should be maintained from which the necessary information can be taken to resume operation.

A reliable stand-by power source should be installed to allow continued Air Traffic Control in cases of commercial power failure.

7. General Precautions and Personnel Training

The computer room, air conditioning equipment room, and data storage room should be monitored.

Steampipes and waterpipes running above the false ceiling should be inspected to guard against possible damage due to accidental breakage, leakage, or condensation.

Emergency exit doors should be located in the computer area. The number of doors depends on the size and location of the area.

Personnel should be trained in emergency measures such as:

Proper method and sequence of shutting off all electrical power.

Shutting off air conditioning system

Handling fire extinguishers in the approved manner.

Properly operating a small-diameter fire hose.

Evacuating records.

Evacuating personnel.

Calling fire company.

First aid.

Location of shut-off valves for steam lines, water pipes, sprinkler systems, etc.

D. Power Requirements

The 9020 System is designed to operate from a 208-volt, three-phase, four-wire, 60-cycle supply. The four wires consist of three-phase wires and one equipment bond. The line-to-line voltage tolerances must be maintained within plus or minus 10 percent, measured at the receptacles when the system is operating. The line frequency must be maintained at 60 cycles plus or minus 2 percent.

A separate feeder connected to the main building distribution panel should provide a suitable supply. However, in cases where the building power fluctuates in excess of plus or minus 10 percent, a separate transformer or motor alternator may be necessary. If a transformer is used, it should be fed from the highest primary source readily available. The feeder for the computer system should feed no other loads and should be protected by a main line circuit breaker. (The "Safety and Fire Precautions" section carries additional pertinent details.)

NOTE: Considering the desired reliability of the 9020 System, it might be advisable to group branch circuits in separate load centers, each fed from the main line circuit breaker. Thus, total outage of the system could be avoided in the case of individual branch circuit CB failure.

The individual branch circuits on the distribution panel should be protected by suitable circuit breakers properly derated according to manufacturer specifications. Three-phase thermomagnetic circuit breakers are used in all of the main 9020 units. Ratings are as follows:

7265-02 Systems Control Console: 20 amperes
7201-01 Computing Element: 50 amperes
7251-03/04 Storage Element: 50 amperes
7231-02 I/O Control Element: 50 amperes
7289-02 Peripheral Adapter Module: 50 amperes
2803-1 Tape Control Unit: 50 amperes
2821-1 Control Unit: 30 amperes

The power distribution panel should be located in an unobstructed, well-lighted area in the computer room. Branch circuits should terminate under the raised floor as close as possible to the machine they supply. However, they should not be located directly beneath the cabling access holes because of interference with the installation of the signal cabline. The receptacle or connector should in all cases be within 10 feet of the cable access hole and be under a freely removable cover.

1. Phase Rotation

The three-phase power receptacles used with this system must be wired for correct phase rotation. Looking at the face of the receptacle and running counterclockwise from the ground pin, the sequencing will be phase 1, phase 2, and phase 3. Refer to Fig. 1-4.

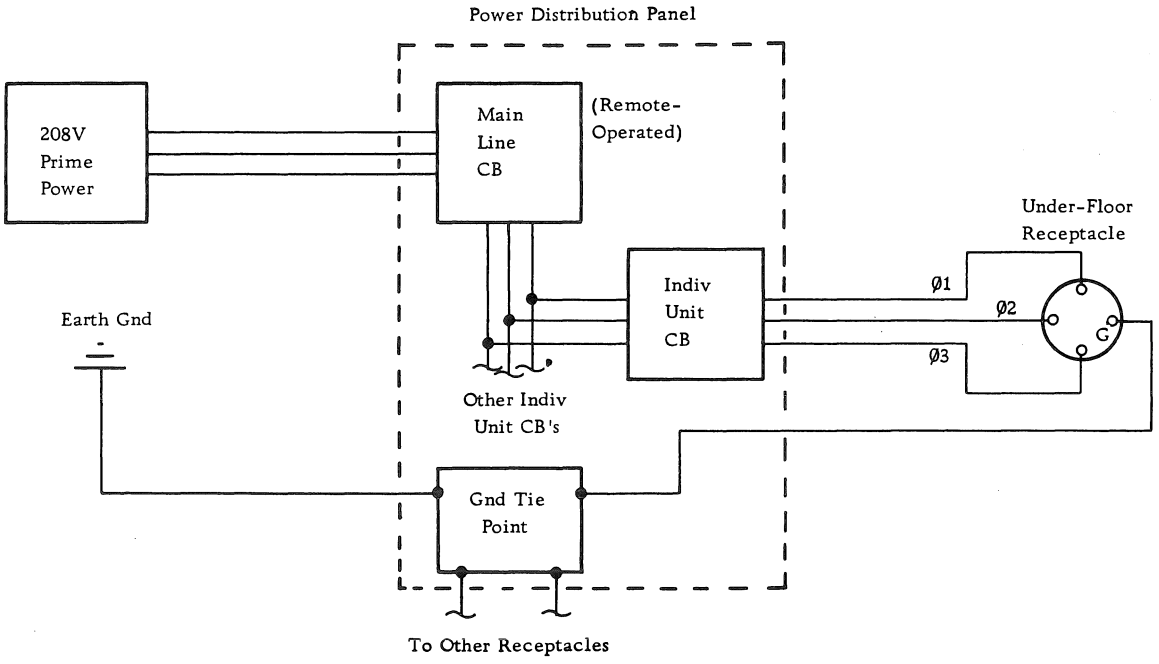


Figure 1-4. Prime Power Distribution.

2. Convenience Outlets

A suitable number of convenience outlets should be installed in the Computer Room and Maintenance Room for use by building maintenance personnel, porter service, field engineers, etc. Recommendations for the Maintenance Room are shown in Fig. 1-1. Convenience outlets are also located on each of the main 9020 System units. These outlets are protected by separate fuses or circuit breakers.

3. Lightning Protection

It is recommended that the customer install lightning protection on his secondary power source when:

1. The utility company installs lightning protectors on the primary.
2. Primary power is supplied by an overhead power service.

3. The area is subject to electrical storms or equivalent type power surges.

A recommended type of service protector to be installed is the GE Pellet-Type, Model 9LA15A1, Model 9 LA15A4, or its equivalent. One of either model is required for single-phase or two or either model are required for three-phase. The determination as to whether lightning protection is desirable, the selection of the service protector needed, and its proper installation are to be made by the Agency.

4. System Grounding

An earth ground is required at the computer distribution panel. This wire shall be carried directly back to the service ground or suitable building ground. Conduit must not be used as the only grounding means. From the central tie point at the computer distribution panel, individual ground wires accompany the three-phase wires through the under-floor receptacle to each element of the 9020 System. This ground is actually a safety ground wire and is tied directly to the frame of the element. The dc returns (signal ground) will be referenced to the frame ground in one box of the system. There will not be an additional equipment bond between frames. Signal ground reference between boxes is accomplished through the coax shielding. When peripheral I/O devices are connected to the 9020 System, signal ground reference will be accomplished through the interconnecting signal cable shielding. As in the case of the 9020 System, it should be possible to separate or join the power and signal grounds inside the peripheral I/O devices.

5. Surge Currents

To minimize the effects of system surge currents, each of the following elements contains a time-delay relay:

7289-02 Peripheral Adapter Module
7201-01 Computing Element

7231-02 I/O Control Element
7251-03/04 Storage Element
7265-02 Systems Control Console

The purpose of the time-delay relay is to provide a sequencing of main line power to the elements. The time-delay relays, adjustable from 5 to 30 seconds, will be set to a value to obtain a staggered power-on sequence of the various system elements.

The following is a listing of approximate element power factors:

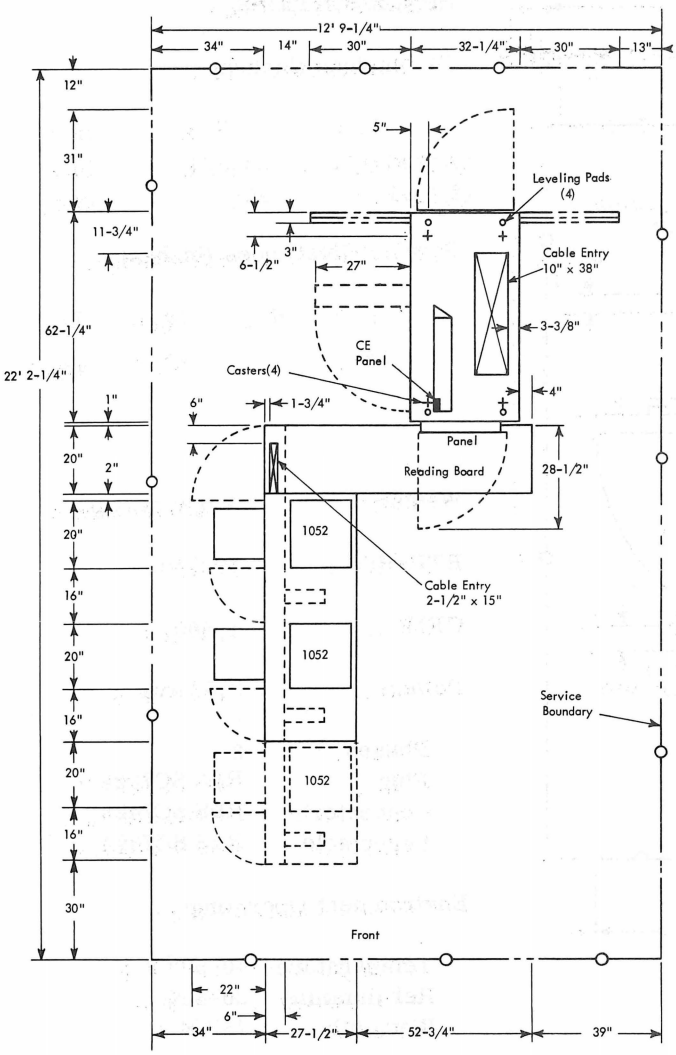
7201-01 Computing Element	0.785
7251-03/04 Storage Element	0.765
7231-02 I/O Control Element	0.82
7265-02 Systems Control Console	0.70
7289-02 Peripheral Adapter Module	0.70
2803-1 Tape Control Unit	0.74
2821-1 Control Unit	0.85

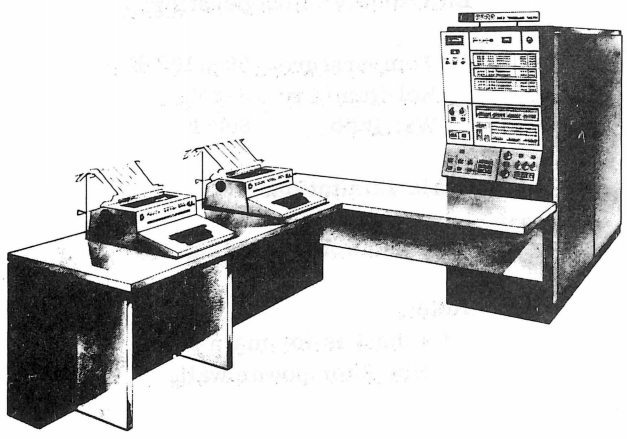
The maximum harmonic content of the phase voltage waveforms is not to be in excess of 5 percent with the equipment not operating.

E. Physical Planning

Detailed specifications for each of the elements are included in the following Figures 1-5 through 1-16.

PLAN VIEW





SPECIFICATIONS

Dimensions (Inches)

F	S	H
See Plan View.		70-3/4

Service Clearances (Inches)

F	R	Rt	L
30	43	39	34

Weight:	1,850 pounds
BTU/Hr:	3,450
CFM:	350
Power:	1.4 kva
Phases	3
Plug	R&S FS3760
Connector	R&S FS3934
Receptacle	R&S FS3754

Environment Operating:

Temperature	60-90° F
Rel Humidity	20-80%
Wet Bulb	78° F

Environment Nonoperating:

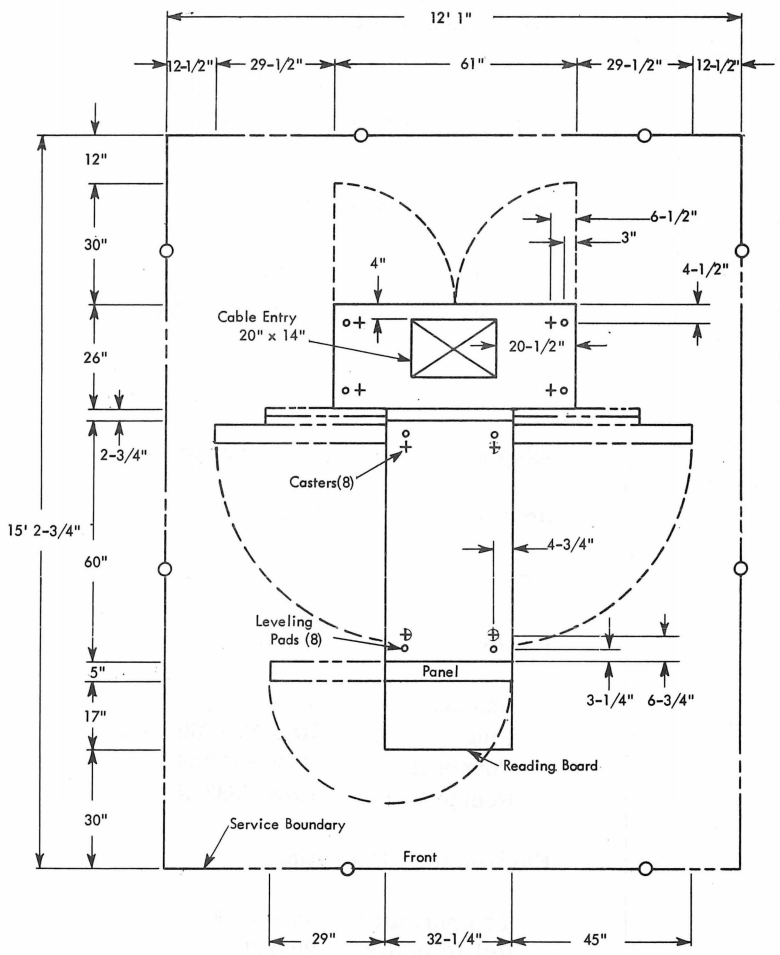
Temperature	50-110° F
Rel Humidity	8-80%
Wet Bulb	80° F

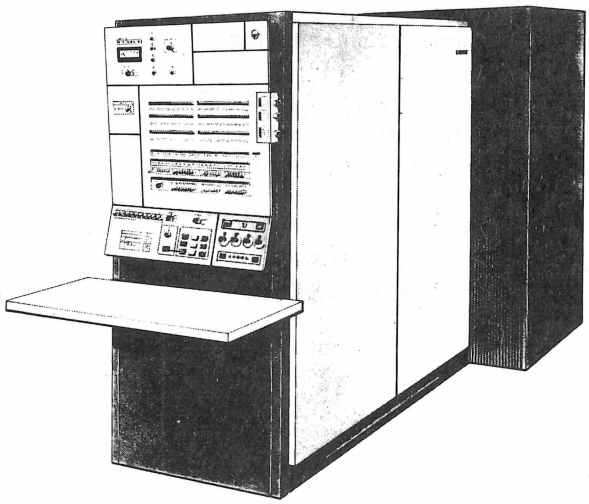
Cable Limitations:

See section on cabling.

Figure 1-5. SC Specifications (7265-02).

PLAN VIEW





SPECIFICATIONS

Dimensions (Inches)

	F	S	H
(1)*	32-1/4	84-3/4	70
(2)*	61	26	72

Service Clearances (Inches)

F	R	Rt	L
30	42	42	42

Weight:	4,000 pounds
BTU/Hr:	10,240
CFM:	1,800
Power:	3.82 kva
Phases	3
Plug	R&S SC7328
Connector	R&S SC7428
Receptacle	R&S SC7324

Environment Operating:

Temperature	60-90° F
Rel Humidity	20-80%
Wet Bulb	78° F

Environment Nonoperating:

Temperature	50-110° F
Rel Humidity	8-80%
Wet Bulb	80° F

Cable Limitations:

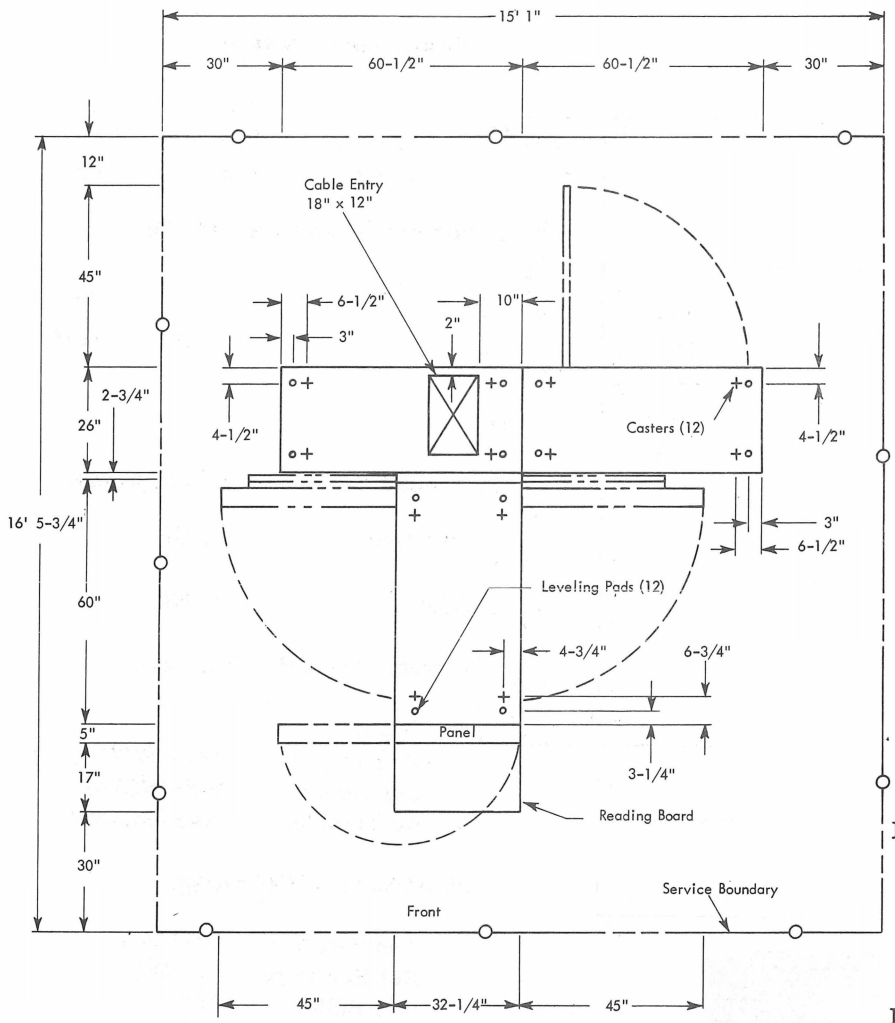
See section on cabling.

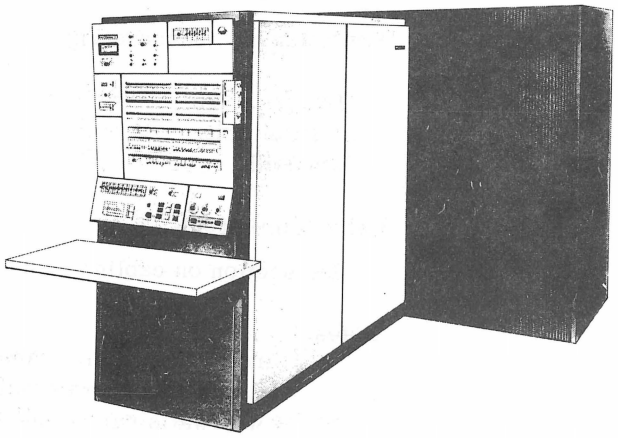
Note:

* Line 1 is for main frame and line 2 for power wall.

Figure 1-6. CE Specifications (7201-01).

PLAN VIEW





SPECIFICATIONS

Dimensions (Inches)

	F	S	H
*	32-1/4	84-3/4	70
*	121	26	72

Service Clearances (Inches)

F	R	Rt	L
30	57	30**	30**

Weight:	5,200 pounds
BTU/Hr:	13,200
CFM:	2,550
Power:	4.75 kva
Phases	3
Plug	R&S SC7328
Connector	R&S SC7428
Receptacle	R&S SC7324

Environment Operating:

Temperature	60-90° F
Rel Humidity	20-80%
Wet Bulb	78° F

Environment Nonoperating:

Temperature	50-110° F
Rel Humidity	8-80%
Wet Bulb	80° F

Cable Limitations:

See section on cabling.

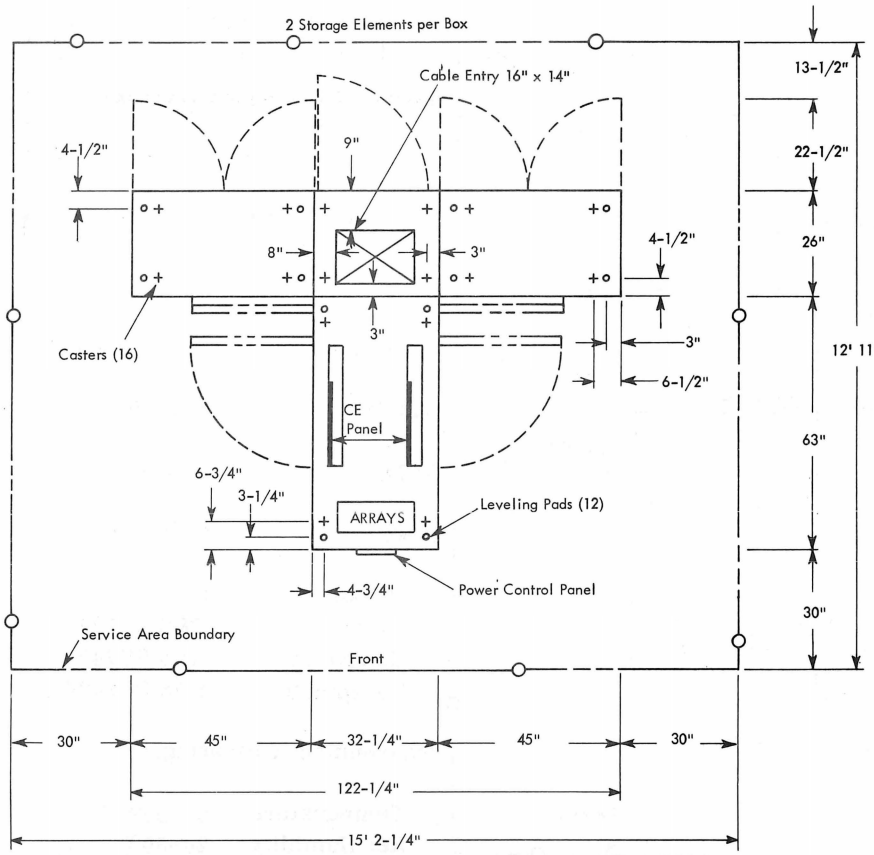
Notes:

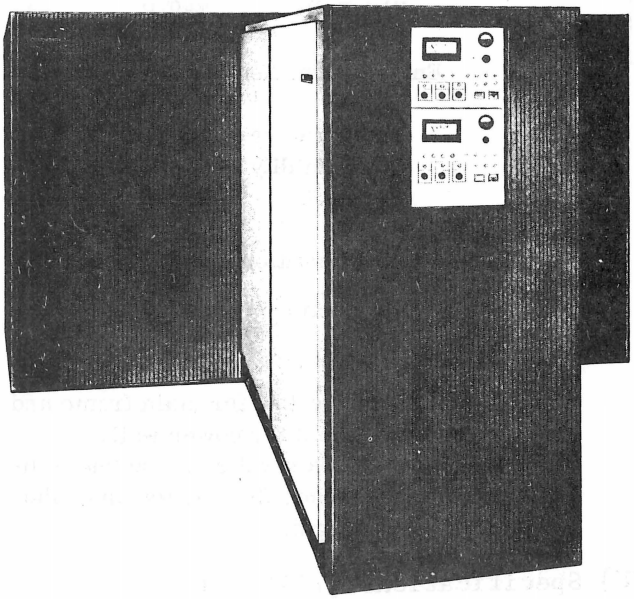
* Line 1 is for main frame and line 2 for power wall.

** Power walls can be butted to reduce floor space and cable length.

Figure 1-7. I/O Control Element (IOCE) Specifications (7231-02).

PLAN VIEW





SPECIFICATIONS

Dimensions (Inches)

	F	S	H
*	32-1/4	63	70
*	122-1/4	26	72

Service Clearances (Inches)

F	R	Rt	L
30	36	30**	30**

Weight:	2,650 pounds
BTU/Hr:	11,200
CFM:	1,500
Power (Total):	4.3 kva
Phases	3
Plugs (2)	R&S SC7328
Connectors	R&S SC7428
Receptacles	R&S SC7324

Environment Operating:

Temperature	60-90° F
Rel Humidity	20-80%
Wet Bulb	78° F

Environment Nonoperating:

Temperature	50-110° F
Rel Humidity	8-80%
Wet Bulb	80° F

Cable Limitations:

See section on cabling.

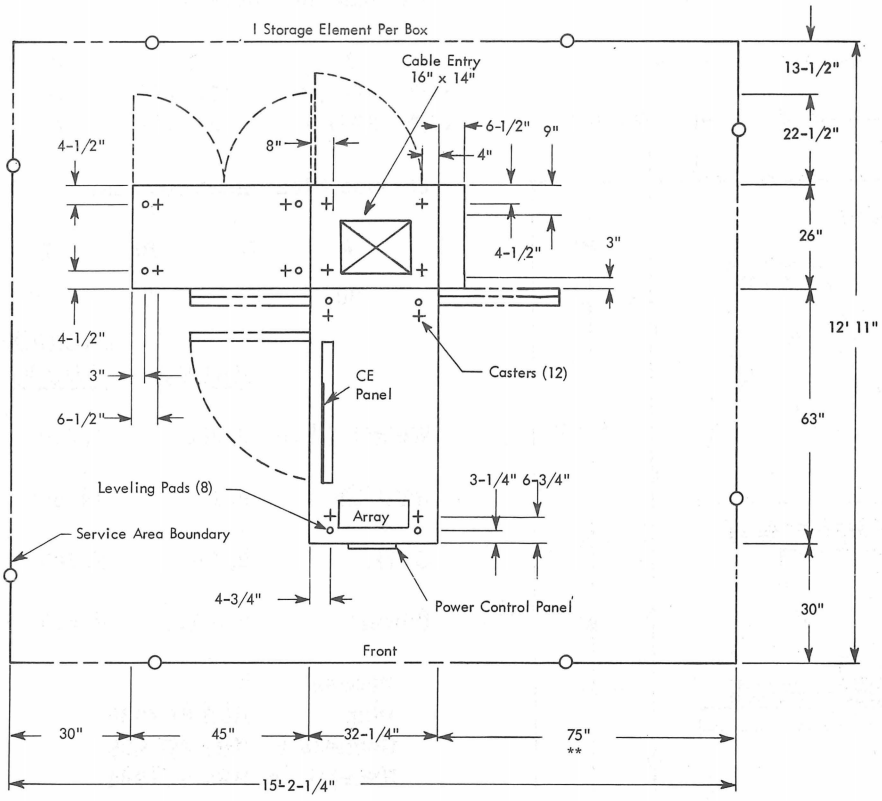
Notes:

* Line 1 is for main frame and line 2 for power wall.

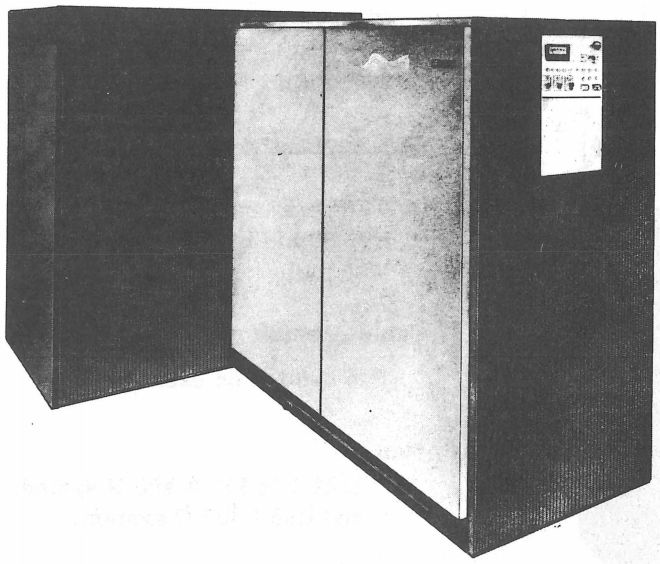
** Power walls can be butted to reduce floor space and cable length.

Figure 1-8. SE Specifications (7251-04).

PLAN VIEW



** Includes 30" service clearance and 45" for expansion.



SPECIFICATIONS

Dimensions (Inches)

	F	S	H
*	32-1/4	63	70
*	77-1/4	26	72

Service Clearances (Inches)

F	R	Rt	L
30	36	30	30

Weight:	1,500 pounds
BTU/Hr:	5,600
CFM:	1,000
Power:	2.15 kva
Phases	3
Plug	R&S SC7328
Connector	R&S SC7428
Receptacle	R&S SC7324

Environment Operating:

Temperature	60-90° F
Rel Humidity	20-80%
Wet Bulb	78° F

Environment Nonoperating:

Temperature	50-110° F
Rel Humidity	8-80%
Wet Bulb	80° F

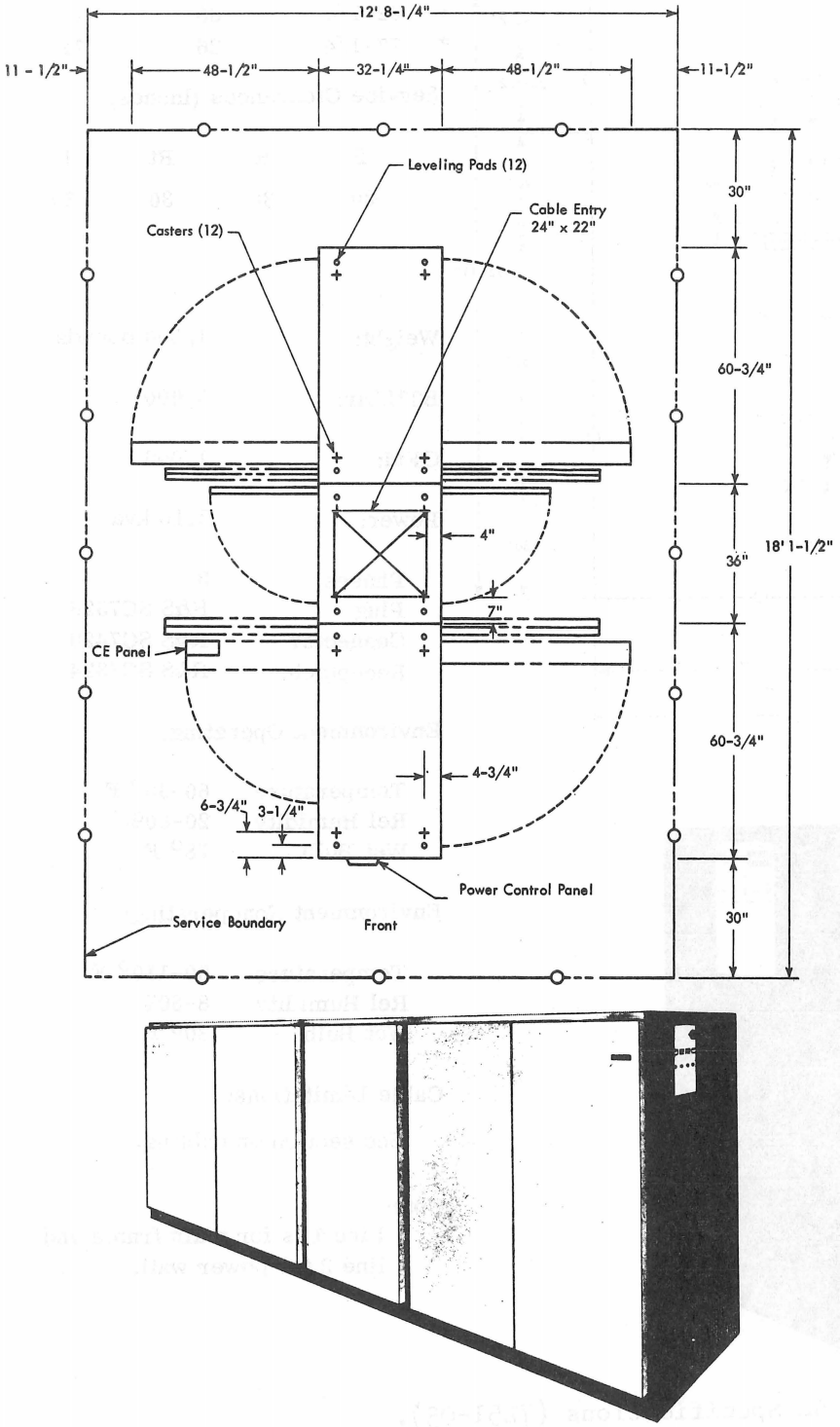
Cable Limitations:

See section on cabling.

Note:
* Line 1 is for main frame and line 2 for power wall.

Figure 1-9. SE Specifications (7251-03).

PLAN VIEW



SPECIFICATIONS

Dimensions (Inches)

	F	S	H
(1)*	32-1/4	157-1/2	70
(2)*	32-1/4	96-3/4	70

Service Clearances (Inches)

F	R	Rt	L
30	30	60	60

	NAFEC	JACKSON-VILLE
Weight (lb.):	3,850	4,200
BTU/Hr:	9,100	14,300
CFM:	2,760	2,760
Power:	3.8 kva	6 kva
Phases	3	
Plug	R&S SC7328	
Connector	R&S SC7428	
Receptacle	R&S SC7324	

Environment Operating:

Temperature	60-90° F
Rel Humidity	20-80%
Wet Bulb	78° F

Environment Nonoperating:

Temperature	50-110° F
Rel Humidity	8-80%
Wet Bulb	80° F

Cable Limitations:

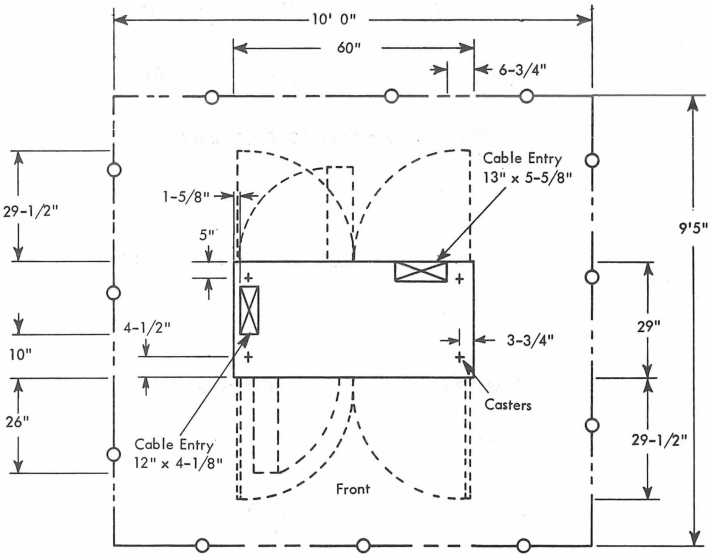
See section on cabling.

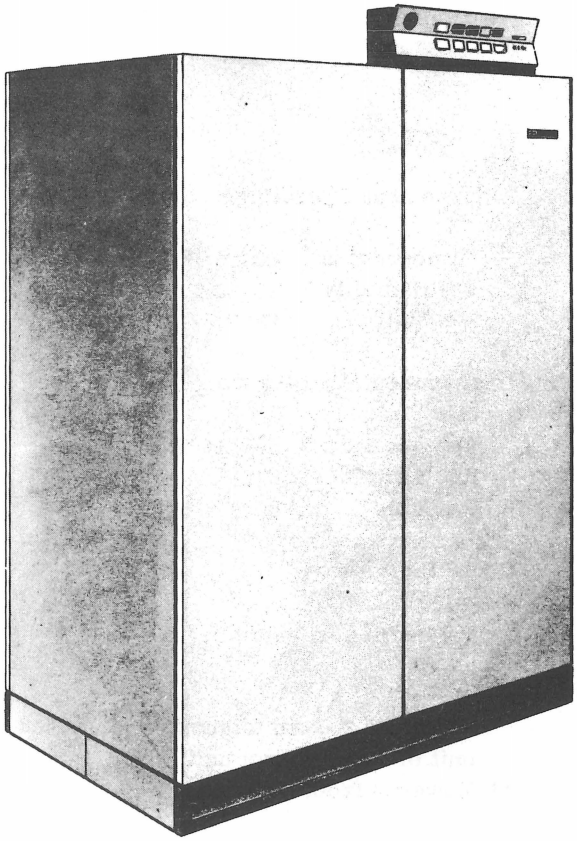
Note:

* Line 1 is for A and B system and line 2 for C system.

Figure 1-10. PAM Specifications (7289-02).

PLAN VIEW





SPECIFICATIONS

Dimensions (Inches)

F	S	H
60	29	60

Service Clearances (Inches)

F	R	Rt	L
42	42	30*	30

Weight:	1,400 pounds
BTU/Hr:	2,500
CFM:	500
Power:	1.0 kva
Phases	3
Plug	R&S SC7328
Connector	R&S SC7428
Receptacle	R&S SC7324

Environment Operating:

Temperature	60-90°F
Rel Humidity	20-80%
Wet Bulb	78°F

Environment Nonoperating:

Temperature	50-110°F
Rel Humidity	8-80%
Wet Bulb	80°F

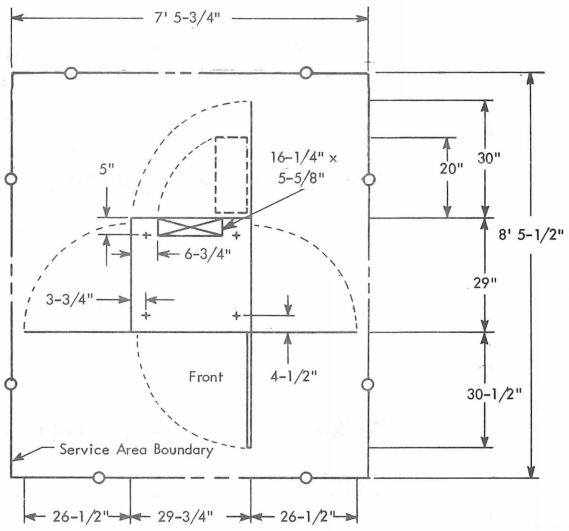
Cable Limitations:

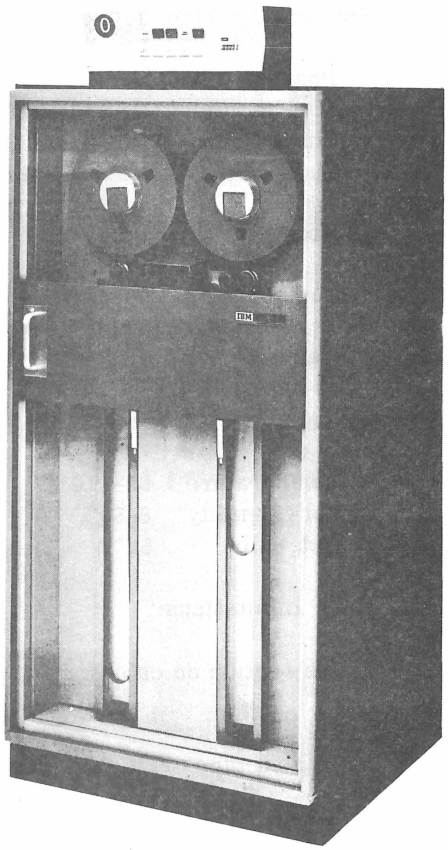
See section on cabling.

Notes:
* Can abut tape drive this side only.

Figure 1-11. TCU Specifications (2803-1).

PLAN VIEW





SPECIFICATIONS

Dimensions (Inches)

F	S	H
30	29	60

Service Clearances (Inches)

F	R	Rt	L
36	36	30*	30*

Weight: 800 pounds

BTU/Hr: 3,500

CFM: 500

Power: 1.6 kva**

Environment Operating:

Temperature	60-90°F
Rel Humidity	20-80%
Wet Bulb	78°F

Environment Nonoperating:

Temperature	50-110°F
Rel Humidity	8-80%
Wet Bulb	80°F

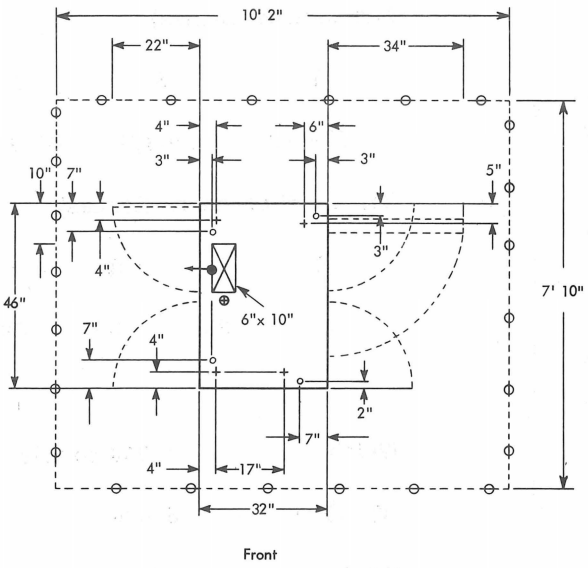
Cable Limitations:

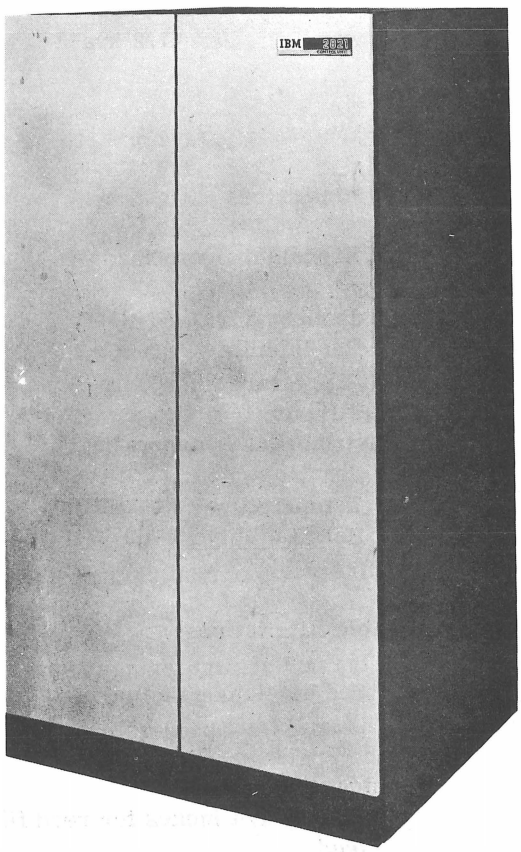
See section on cabling.

Notes:
* When not abutted to another tape unit or tape control unit
** Powered from control unit

Figure 1-12. Tape Drive Specifications (2401).

PLAN VIEW





SPECIFICATIONS

Dimensions (Inches)

F	S	H
32	46	60

Service Clearances (Inches)

F	R	Rt	L
30	18	48	42

Weight:	1,000 pounds
BTU/Hr:	7,000
CFM:	300
Power:	2.4 kva
Phases	3
Plug	R&S FS3760
Connector	R&S FS3934
Receptacle	R&S FS3754

Environment Operating:

Temperature	60-90°F
Rel Humidity	8-80%
Wet Bulb	78°F

Environment Nonoperating:

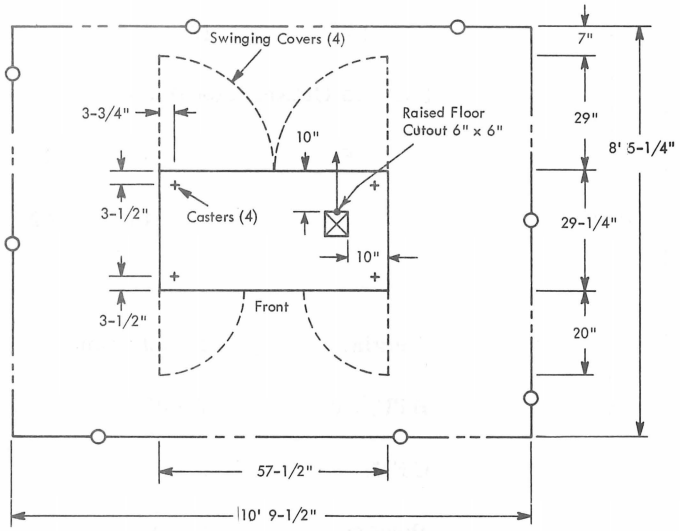
Temperature	50-110°F
Rel Humidity	8-80%
Wet Bulb	80°F

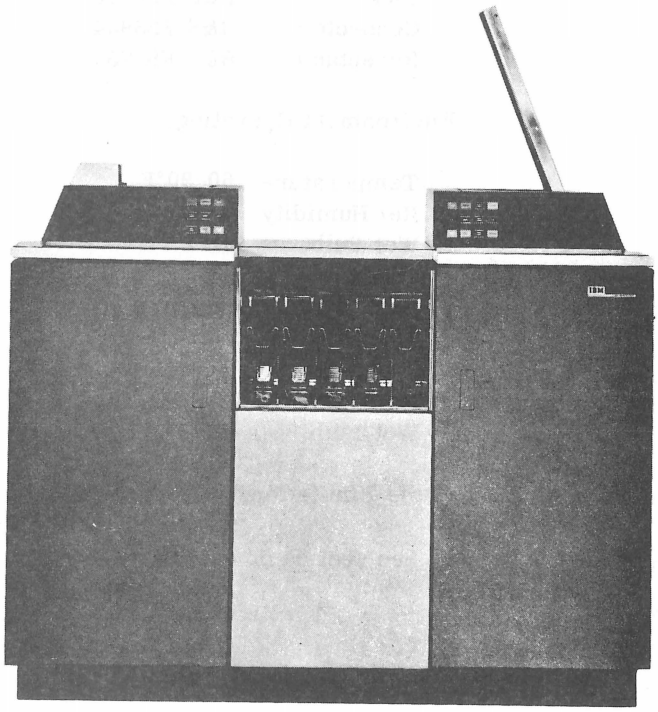
Cable Limitations:

See section on cabling.

Figure 1-13. ICU Specifications (2821-1).

PLAN VIEW





SPECIFICATIONS

Dimensions (Inches)

F	S	H
57-1/2	29-1/4	45-1/4*

Service Clearances (Inches)

F	R	Rt	L
36	36	36	36

Weight: 1,050 pounds

BTU/Hr: 3,000

CFM: 50

Power: 1.2 kva**

Environment Operating:

Temperature 60-90°F
Rel Humidity 20-80%

Environment Nonoperating:

Temperature 50-110°F
Rel Humidity 8-80%

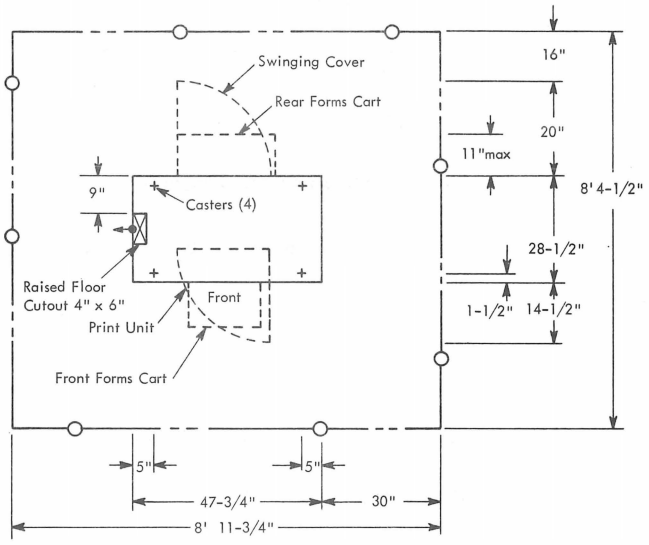
Cable Limitations:

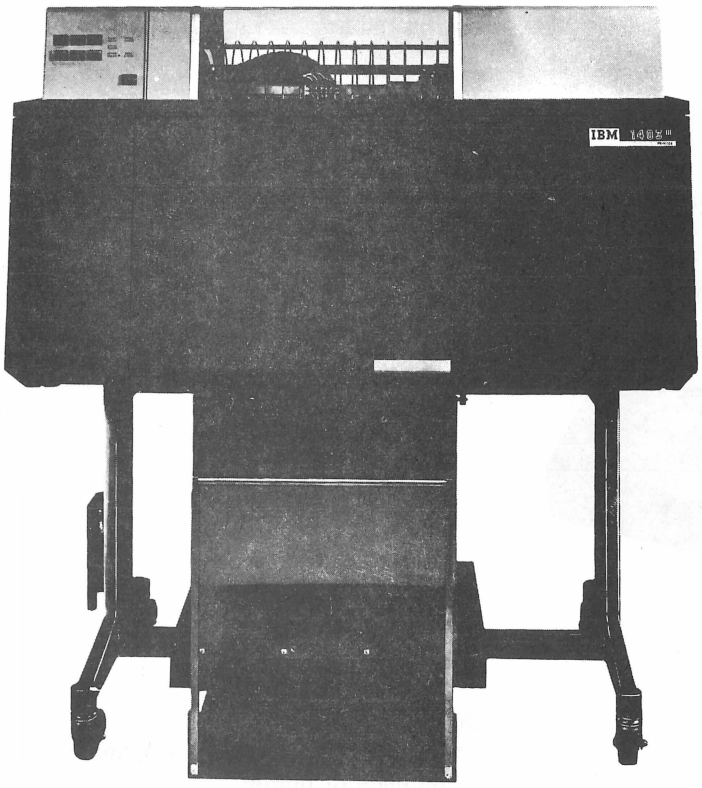
See section on cabling.

Notes:
* Add 20-1/4 inches for read file feed.
** Powered from 2821

Figure 1-14. Card Reader/Punch Specifications (2540).

PLAN VIEW





SPECIFICATIONS

Dimensions (Inches)

F	S	H
47-3/4	28-1/2	53-1/4

Service Clearances (Inches)

F	R	Rt	L
36	36	30	30

Weight: 750 pounds

BTU/Hr: 3,000

CFM: 310

Power: 1.0 kva*

Environment Operating:

Temperature	60-90°F
Rel Humidity	20-80%

Environment Nonoperating:

Temperature	50-110°F
Rel Humidity	8-80%

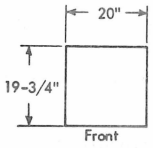
Cable Limitations:

See section on cabling.

Note:
* Powered from 2821

Figure 1-15. High-Speed Printer Specifications (1403).

PLAN VIEW



SPECIFICATIONS

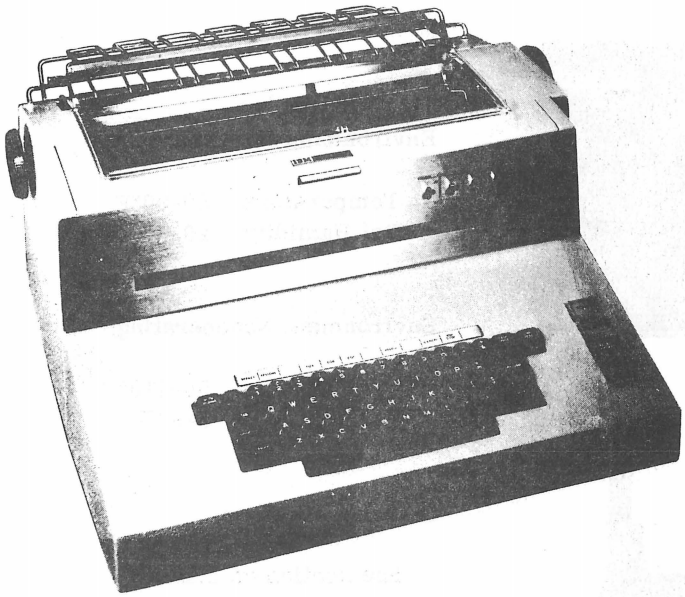
Dimensions (Inches)

F	S	H
23*	19-3/4	9

Service Clearances (Inches)

F	R	Rt	L
0	0	0	0

Weight:	65 pounds
BTU/Hr:	335
CFM:	0
Power:	0.1 kva**



Environment Operating:

Temperature	50-110°F
Rel Humidity	10-80%
Wet Bulb	80°F

Environment Nonoperating:

Temperature	50-110°F
Rel Humidity	10-80%
Wet Bulb	80°F

Notes:
* Includes 1-1/2 inches for knobs on ends of platen
** Powered from system console

Figure 1-16. Printer Keyboard Specifications (1052).

F. Cabling

In this section cabling schematic diagrams are presented for each element and for groups of elements (see Figs. 1-22 through 1-30). Each cable group is broken down into individual paths and applicable flight configurations. For each group, the number of cables used, routing, maximum lengths, and other descriptive information is given.

Cabling within the 9020 System is accomplished, amost exclusively, by the use of 20 conductor coax cables (0.95 $\pm$ 0.040 inch O.D). The cables are terminated with interface connectors (Fig. 1-17). Figures 1-18 through 1-21 are representative of other cable connectors used in the system. The dimensions given are maximum over-all measurements.

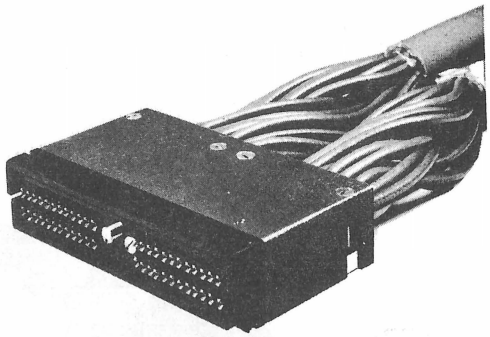


Figure 1-17. System/360 Interface Connector.

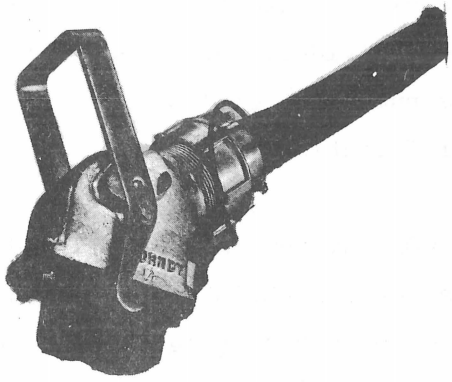


Figure 1-18. Tape Power Cable Connector (3-5/8 inches high, 4-1/2 inches deep, 2-1/16 inches wide).

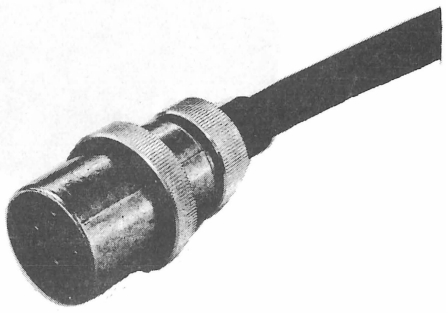


Figure 1-19. Power Cord Plug (3-phase, 30-ampere, 4-wire; O.D. 2-1/4 inches, 4-1/2 inches long). Used on 7265 SCC and 2821 ICU.

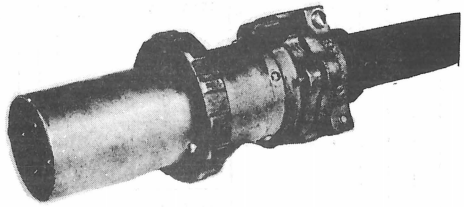


Figure 1-20. Power Cord Plug (3-phase, 60-ampere, 4-wire; O.D. 3-3/4 inches, 9 inches long). Used on PAM, TCU, CE, IOCE, and SE.

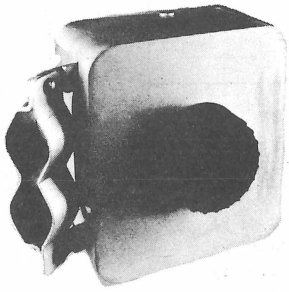
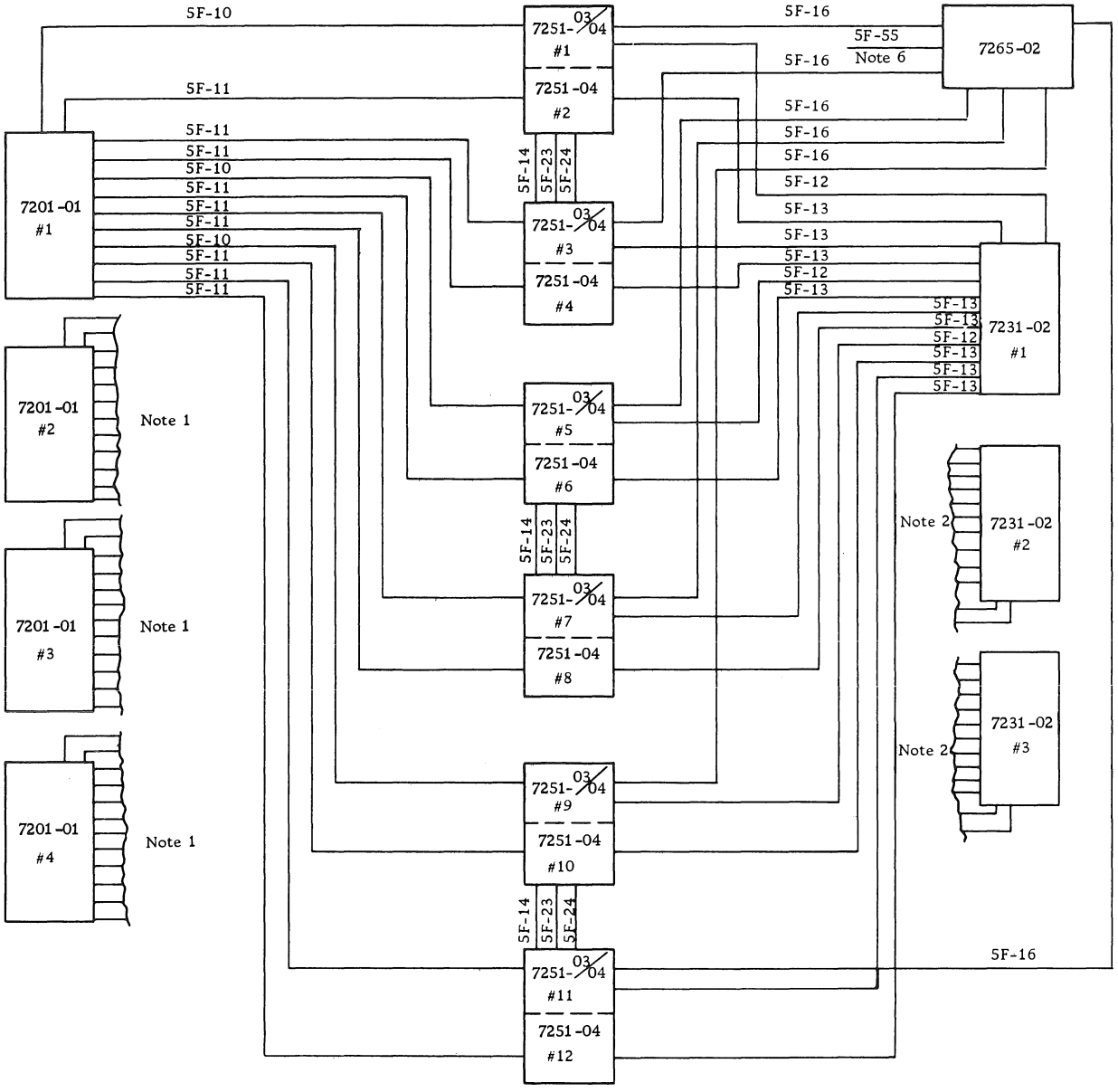


Figure 1-21. 200-Pin Signal Connector (7-11/16 inches high, 4-1/8 inches deep, 5-15/16 inches wide). Used on card machines and tapes.



Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 4)	Notes
5F-10	4	7251-03/04 #1	7201-01 #1		100-325X	5
	4	7251-03/04 #1	7201-01 #2		100-325X	5
	4	7251-03/04 #1	7201-01 #3		200-325X	5
	4	7251-03/04 #1	7201-01 #4		325X	5
	4	7251-03/04 #5	7201-01 #1		200-325X	5
	4	7251-03/04 #5	7201-01 #2		200-325X	5
	4	7251-03/04 #5	7201-01 #3		200-325X	5
	4	7251-03/04 #5	7201-01 #4		325X	5
	4	7251-03/04 #9	7201-01 #1		325X	5
	4	7251-03/04 #9	7201-01 #2		325X	5
	4	7251-03/04 #9	7201-01 #3		325X	5
	4	7251-03/04 #9	7201-01 #4		325X	5

Figure 1-22. 7251-03/04 Storage Element Cabling Schematic.

Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 4)	Notes
5F-11	2	7251-04 #2	7201-01 #1		100-325X	5
	2	7251-04 #2	7201-01 #2		100-325X	5
	2	7251-04 #2	7201-01 #3		200-325X	5
	2	7251-04 #2	7201-01 #4		325X	5
	2	7251-03/04 #3	7201-01 #1		100-325X	5
	2	7251-03/04 #3	7201-01 #2		100-325X	5
	2	7251-03/04 #3	7201-01 #3		200-325X	5
	2	7251-03/04 #3	7201-01 #4		325X	5
	2	7251-04 #4	7201-01 #1		200-325X	5
	2	7251-04 #4	7201-01 #2		200-325X	5
	2	7251-04 #4	7201-01 #3		200-325X	5
	2	7251-04 #4	7201-01 #4		325X	5
	2	7251-04 #6	7201-01 #1		325-325X	5
	2	7251-04 #6	7201-01 #2		325-325X	5
	2	7251-04 #6	7201-01 #3		325-325X	5
	2	7251-04 #6	7201-01 #4		325X	5
	2	7251-03/04 #7	7201-01 #1		325-325X	5
	2	7251-03/04 #7	7201-01 #2		325-325X	5
	2	7251-03/04 #7	7201-01 #3		325-325X	5
	2	7251-03/04 #7	7201-01 #4		325X	5
	2	7251-04 #8	7201-01 #1		325-325X	5
	2	7251-04 #8	7201-01 #2		325-325X	5
	2	7251-04 #8	7201-01 #3		325-325X	5
	2	7251-04 #8	7201-01 #4		325X	5
	2	7251-04 #10	7201-01 #1		325X	5
	2	7251-04 #10	7201-01 #2		325X	5
	2	7251-04 #10	7201-01 #3		325X	5
	2	7251-04 #10	7201-01 #4		325X	5
	2	7251-03/04 #11	7201-01 #1		325X	5
	2	7251-03/04 #11	7201-01 #2		325X	5
	2	7251-03/04 #11	7201-01 #3		325X	5
	2	7251-03/04 #11	7201-01 #4		325X	5
	2	7251-04 #12	7201-01 #1		325X	5
	2	7251-04 #12	7201-01 #2		325X	5
	2	7251-04 #12	7201-01 #3		325X	5
	2	7251-04 #12	7201-01 #4		325X	5
5F-12	4	7251-03/04 #1	7231-02 #1		100-325X	5
	4	7251-03/04 #1	7231-02 #2		100-325X	5
	4	7251-03/04 #1	7231-02 #3		200-325X	5
	4	7251-03/04 #5	7231-02 #1		200-325X	5
	4	7251-03/04 #5	7231-02 #2		200-325X	5
	4	7251-03/04 #5	7231-02 #3		200-325X	5
	4	7251-03/04 #9	7231-02 #1		325X	5
	4	7251-03/04 #9	7231-02 #2		325X	5
	4	7251-03/04 #9	7231-02 #3		325X	5
5F-13	2	7251-04 #2	7231-02 #1		100-325X	5
	2	7251-04 #2	7231-02 #2		100-325X	5
	2	7251-04 #2	7231-02 #3		200-325X	5
	2	7251-03/04 #3	7231-02 #1		100-325X	5
	2	7251-03/04 #3	7231-02 #2		100-325X	5
	2	7251-03/04 #3	7231-02 #3		200-325X	5
	2	7251-04 #4	7231-02 #1		200-325X	5
	2	7251-04 #4	7231-02 #2		200-325X	5
	2	7251-04 #4	7231-02 #3		200-325X	5
	2	7251-04 #6	7231-02 #1		325-325X	5
	2	7251-04 #6	7231-02 #2		325-325X	5
	2	7251-04 #6	7231-02 #3		325-325X	5
	2	7251-03/04 #7	7231-02 #1		325-325X	5
	2	7251-03/04 #7	7231-02 #2		325-325X	5

Figure 1-22. 7251-03/04 Storage Element Cabling Schematic (Cont'd).

Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 4)	Notes
5F-13 (cont'd)	2	7251-03/04 #7	7231-02 #3		325-325X	5
	2	7251-04 #8	7231-02 #1		325-325X	5
	2	7251-04 #8	7231-02 #2		325-325X	5
	2	7251-04 #8	7231-02 #3		325-325X	5
	2	7251-04 #10	7231-02 #1		325X	5
	2	7251-04 #10	7231-02 #2		325X	5
	2	7251-04 #10	7231-02 #3		325X	5
	2	7251-03/04 #11	7231-02 #1		325X	5
	2	7251-03/04 #11	7231-02 #2		325X	5
	2	7251-03/04 #11	7231-02 #3		325X	5
	2	7251-04 #12	7231-02 #1		325X	5
	2	7251-04 #12	7231-02 #2		325X	5
	2	7251-04 #12	7231-02 #3		325X	5
5F-14	8	7251-04 #2	7251-03/04 #3		100-325X	5
	8	7251-04 #6	7251-03/04 #7		325-325X	5
	8	7251-04 #10	7251-03/04 #11		325X	5
5F-16	1	7265-02	7251-03/04 #1	100	100-325X	
	1	7265-02	7251-03/04 #3	100	100-325X	
	1	7265-02	7251-03/04 #5	100	200-325X	
	1	7265-02	7251-03/04 #7	100	325-325X	
	1	7265-02	7251-03/04 #9	100	325X	
	1	7265-02	7251-03/04 #11	100	325X	
5F-23	4	7251-04 #2	7251-03/04 #3		200-325X	5
	4	7251-04 #6	7251-03/04 #7		325-325X	5
	4	7251-04 #10	7251-03/04 #11		325X	5
5F-24	2	7251-04 #2	7251-03/04 #3		325X	5
	2	7251-04 #6	7251-03/04 #7		325X	5
	2	7251-04 #10	7251-03/04 #11		325X	5
5F-55	1	7251-03/04 #1	7265-02	100	100-325X	3
	1	7251-04 #2	7265-02	100	100-325X	3
	1	7251-03/04 #3	7265-02	100	100-325X	3
	1	7251-04 #4	7265-02	100	200-325X	3
	1	7251-03/04 #5	7265-02	100	200-325X	3
	1	7251-04 #6	7265-02	100	325-325X	3
	1	7251-03/04 #7	7265-02	100	325-325X	3
	1	7251-04 #8	7265-02	100	325-325X	3
	1	7251-03/04 #9	7265-02	100	325X	3
	1	7251-04 #10	7265-02	100	325X	3
	1	7251-03/04 #11	7265-02	100	325X	3
	1	7251-04 #12	7265-02	100	325X	3

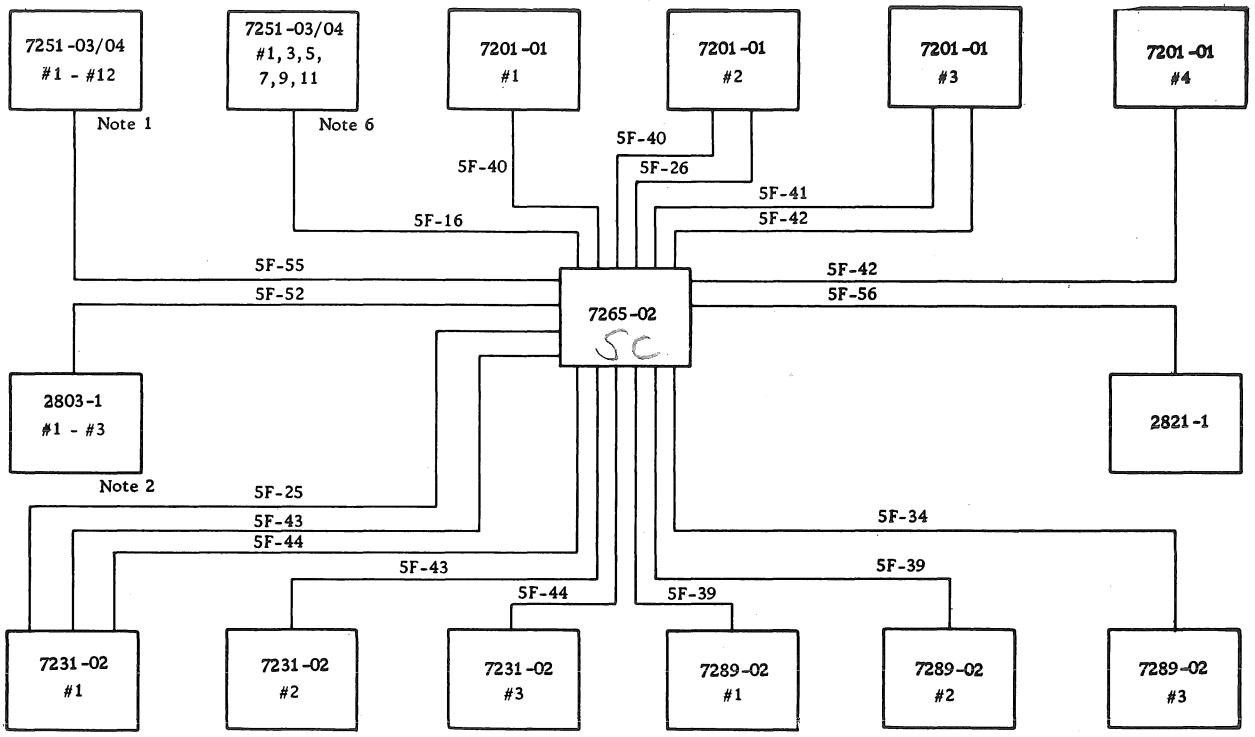
NOTES:

1. The cabling will be the same as for the 7201-01 #1 with the same group numbers.
2. The cabling will be the same as for the 7231-02 #1 with the same group numbers.
3. EPO cable is included in the group.
4. To determine what cables are in a flight configuration, use those which indicate the configuration desired.

   Example: 100-325X indicates the 100, 200, 325 and 325X (expanded) configuration.

5. Refer to illustrations of maximum serial or loop cabling length for maximum cable length.
6. EPO cabling between 7265-02 and each 7251-03/04 (1-12).

Figure 1-22. 7251-03/04 Storage Element Cabling Schematic (Cont'd).



Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 4)	Notes
5F-16	1	7265-02	7251-03/04 #1	100	100-325X	
	1	7265-02	7251-03/04 #3	100	100-325X	
	1	7265-02	7251-03/04 #5	100	200-325X	
	1	7265-02	7251-03/04 #7	100	325-325X	
	1	7265-02	7251-03/04 #9	100	325X	
	1	7265-02	7251-03/04 #11	100	325X	
5F-25	2	7231-02 #1	7265-02	100	100	
5F-26	4	7265-02	7201-01 #2	75	100	
5F-34	4	7289-02 #3	7265-02	100	200-325X	3
5F-39	4	7289-02 #1	7265-02	100	100-325X	3
	4	7289-02 #2	7265-02	100	100-325X	3
5F-40	6	7265-02	7201-01 #1		100-325X	3,5
	2	7265-02	7201-01 #2	75	100-325X	3
5F-41	6	7265-02	7201-01 #3	75	200-325X	3
5F-42	1	7265-02	7201-01 #3	75	325X	
	6	7265-02	7201-01 #4		325X	3,5
5F-43	2	7231-02 #1	7265-02	100	100-325X	3
	4	7231-02 #2	7265-02	100	100-325X	3

Figure 1-23. 7265-02 System Control Console Cabling Schematic.

Group No.	No. of Cables	From	To	Maximum Length(ft)	Flight Configuration (Note 4)	Notes
SF-44	2	7231-02 #1	7265-02	100	200-325X	
	4	7231-02 #3	7265-02	100	200-325X	3
SF-52	2	2803-1 #1	7265-02	100	100-325X	3
	2	2803-1 #2	7265-02	100	100-325X	3
	2	2803-1 #3	7265-02	100	100-325X	3
SF-55	1	7251-03/04 #1	7265-02	100	100-325X	3
	1	7251-04 #2	7265-02	100	100-325X	3
	1	7251-03/04 #3	7265-02	100	100-325X	3
	1	7251-04 #4	7265-02	100	200-325X	3
	1	7251-03/04 #5	7265-02	100	200-325X	3
	1	7251-04 #6	7265-02	100	325-325X	3
	1	7251-03/04 #7	7265-02	100	325-325X	3
	1	7251-04 #8	7265-02	100	325-325X	3
	1	7251-03/04 #9	7265-02	100	325X	3
	1	7251-04 #10	7265-02	100	325X	3
	1	7251-03/04 #11	7265-02	100	325X	3
	1	7251-04 #12	7265-02	100	325X	3
SF-56	3	2821-1	7265-02	50	100-325X	3

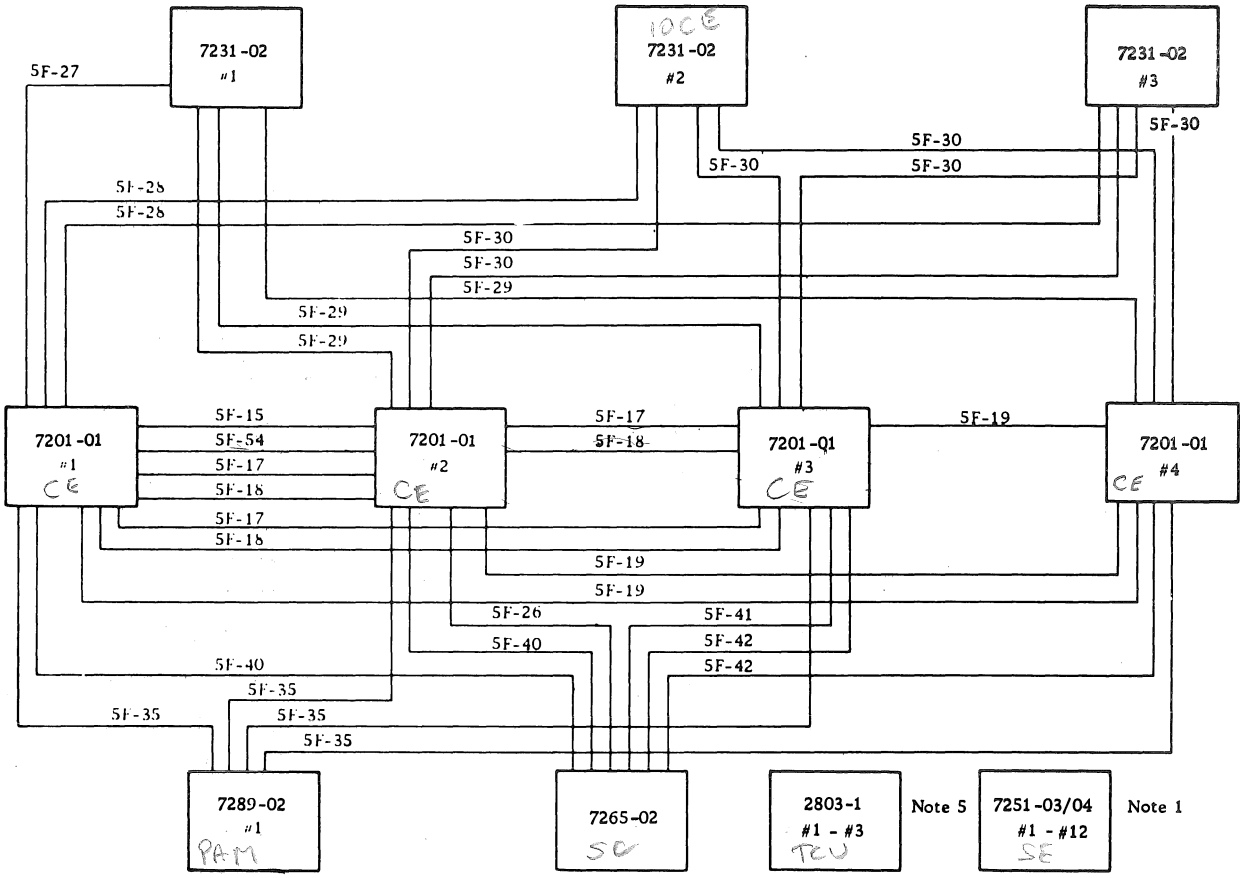
NOTES:

1. This group number applies to all 7251-03/04's (#1 through #12).
2. This group number applies to 2803-1 #1, 2, and 3.
3. EPO cable is included in this group.
4. To determine what cables are in a flight configuration, use those which indicate the configuration desired.

   Example: 100-325X includes the 100, 200, 325 and 325X (expanded) configuration.

5. Refer to illustrations of maximum serial or loop cabling length for maximum cable length.
6. The group number applies to 7251-03/04 # 1, 3, 5, 7, 9, and 11.

Figure 1-23. 7265-02 System Control Console Cabling Schematic (Cont'd).



Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 3)	Notes
5F-15	10	7201-01 #1	7201-01 #2		100-325X	4
5F-17	4	7201-01 #1	7201-01 #2		200-325	4
	7	7201-01 #1	7201-01 #3	100	200-325	
	14	7201-01 #2	7201-01 #3		200-325	4
5F-18	7	7201-01 #1	7201-01 #2		325X	4
	1	7201-01 #1	7201-01 #3	100	325X	
	17	7201-01 #2	7201-01 #3		325X	4
5F-19	1	7201-01 #2	7201-01 #4	100	325X	
	8	7201-01 #1	7201-01 #4	100	325X	
	17	7201-01 #3	7201-01 #4		325X	4
5F-26	4	7265-02	7201-01 #2		100	4
5F-27	5	7201-01 #1	7231-02-#1	100	100-325X	4
5F-28	2	7201-01 #1	7231-02 #2	100	100-325X	4
	2	7201-01 #1	7231-02 #3	100	200-325X	4

Figure 1-24. 7201-01 Computing Element Cabling Schematic.

Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 3)	Notes
5F-29	4	7201-01 #3	7231-02 #1	100	200-325X	4
	4	7201-01 #2	7231-02 #1	100	100-325X	4
	4	7201-01 #4	7231-02 #1	100	325X	4
5F-30	1	7201-01 #2	7231-02 #2	100	100-325X	4
	1	7201-01 #2	7231-02 #3	100	200-325X	4
	1	7201-01 #3	7231-02 #2	100	200-325X	4
	1	7201-01 #3	7231-02 #3	100	200-325X	4
	1	7201-01 #4	7231-02 #2	100	325X	4
	1	7201-01 #4	7231-02 #3	100	325X	4
5F-35	1	7201-01 #1	7289-02 #1		100-325X	4
	1	7201-01 #2	7289-02 #1		100-325X	4
	1	7201-01 #3	7289-02 #1		200-325X	4
	1	7201-01 #4	7289-02 #1		325X	4
5F-40	6	7265-02	7201-01 #1		100-325X[4]	2, 4
	2	7265-02	7201-01 #2	75	100-325X	2
5F-41	6	7265-02	7201-01 #3	75	200-325X	2
5F-42	1	7265-02	7201-01 #3	75	325X	
	6	7265-02	7201-01 #4		325X	2, 4
5F-54	3	7201-01 #1	7201-01 #2		100	4

NOTES:

1. Refer to 7251-03/04 Storage Element cabling schematic.
2. EPO cable is included in this group.
3. To determine what cables are in a flight configuration, use those which indicate the configuration desired.

   Example: 100-325X includes the 100, 200, 325 and 325X (expanded) configuration.

4. Refer to illustrations of maximum serial or loop cabling length for maximum cable lengths.
5. Refer to 2803-1 Tape Control Unit Cabling schematic.

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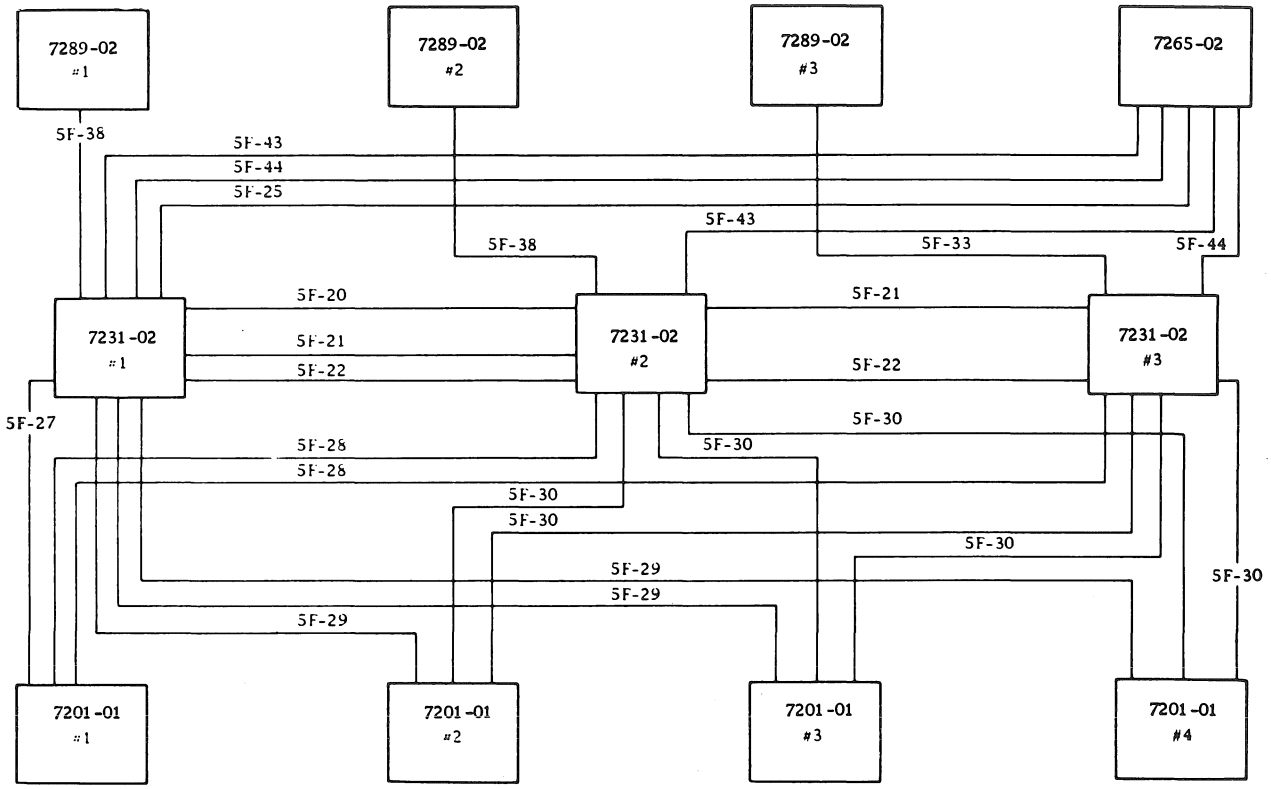
Figure 1-24. 7201-01 Computing Element Cabling Schematic (Cont'd).



7251-03/04 #1 - #12 Note 1

2803-1 #1 - #3 Note 5

Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 3)	Notes
5F-20	6	7231-02 #1	7231-02 #2		100-325X	4
5F-21	9	7231-02 #2	7231-02 #3		200-325X	4
	3	7231-02 #1	7231-02 #2		200-325X	4
5F-22	3	7231-02 #1	7231-02 #2		325X	4
	3	7231-02 #2	7231-02 #3		325X	4
5F-25	2	7231-02 #1	7265-02	100	100	
5F-27	5	7201-01 #1	7231-02 #1	100	100-325X	4
5F-28	2	7201-01 #1	7231-02 #2	100	100-325X	4
	2	7201-01 #1	7231-02 #3	100	200-325X	4
5F-29	4	7201-01 #2	7231-02 #1	100	100-325X	4
	4	7201-01 #3	7231-02 #1	100	200-325X	4
	4	7201-01 #4	7231-02 #1	100	325X	4

Figure 1-25. 7231-02 I/O Control Element Cabling Schematic.

Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 3)	Notes
5F-30	1	7201-01 #2	7231-02 #2	100	100-325X	4
	1	7201-01 #2	7231-02 #3	100	200-325X	4
	1	7201-01 #3	7231-02 #2	100	200-325X	4
	1	7201-01 #3	7231-02 #3	100	200-325X	4
	1	7201-01 #4	7231-02 #2	100	325X	4
	1	7201-01 #4	7231-02 #3	100	325X	4
5F-33	2	7289-02 #3	7231-02 #3		200-325X	4
5F-38	2	7289-02 #1	7231-02 #1		100-325X	4
	2	7289-02 #2	7231-02 #2		100-325X	4
5F-43	2	7231-02 #1	7265-02	100	100-325X	2, 4
	4	7231-02 #2	7265-02	100	100-325X	2, 4
5F-44	2	7231-02 #1	7265-02	100	200-325X	
	4	7231-02 #3	7265-02	100	200-325X	2

NOTES:

1. Refer to 7251-03/04 Storage Element cabling schematics.
2. EPO cable is included in the group.
3. To determine what cables are in a flight configuration, use those which indicate the configuration desired.

   Example: 100-325X indicates the 100, 200, 325 and 325X (expanded) configuration.

4. Refer to illustrations of maximum serial or loop cabling length for maximum cable length.
5. Refer to 2803-1 Tape Control Unit abling schematic.

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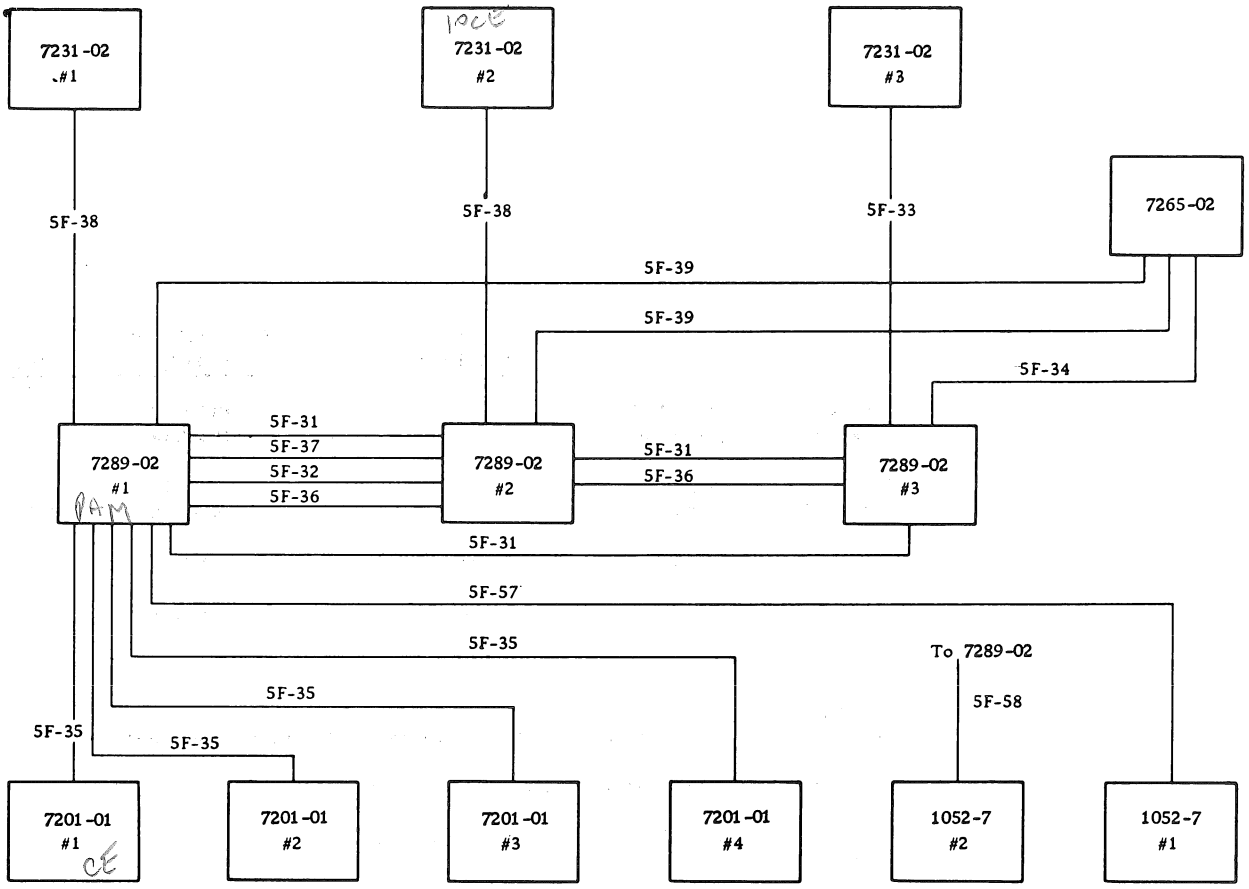
Figure 1-25. 7231-02 I/O Control Element Cabling Schematic (Cont'd).



Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 2)	Notes
5F-31	5	7289-02 #2	7289-02 #3		200-325X	3
	2	7289-02 #1	7289-02 #3		200-325X	3
	1	7289-02 #1	7289-02 #2		200-325X	3
5F-32	2	7289-02 #1	7289-02 #2		100	3
5F-33	2	7289-02 #3	7231-02 #3		200-325X	3
5F-34	4	7289-02 #3	7265-02	100	200-325X	1,3
5F-35	1	7201-01 #1	7289-02 #1		100-325X	3
	1	7201-01 #2	7289-02 #1		100-325X	3
	1	7201-01 #3	7289-02 #1		200-325X	3
	1	7201-01 #4	7289-02 #1		325X	3
5F-36	1	7289-02 #1	7289-02 #2		325X	3
	1	7289-02 #2	7289-02 #3		325X	3
5F-37	7	7289-02 #1	7289-02 #2		100-325X	3,4

Figure 1-26. 7289-02 Peripheral Adapter Module Cabling Schematic.

Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 2)	Notes
5F-38	2	7289-02#1	7231-02 #1		100-325X	3
	2	7289-02#2	7231-02 #2		100-325X	3
5F-39	4	7289-02#1	7265-02	100	100-325X	1, 3
	4	7289-02#2	7265-02	100	100-325X	1, 3
5F-57	4	1052-7 #1	7289-02 #1	300	100-325X	4
5F-58	4	1052-7 #2	7289-02	300	100-325X	4

NOTES:

1. EPO cable is included in the group.
2. To determine what cables are required in a flight configuration, use those which indicate the configuration desired.

   Example: 100-325X indicates the 100, 200, 325 and 325X (expanded) configuration.

3. Refer to illustrations of maximum serial or loop cabling length for maximum cable length.
4. Power cable is included in this group.

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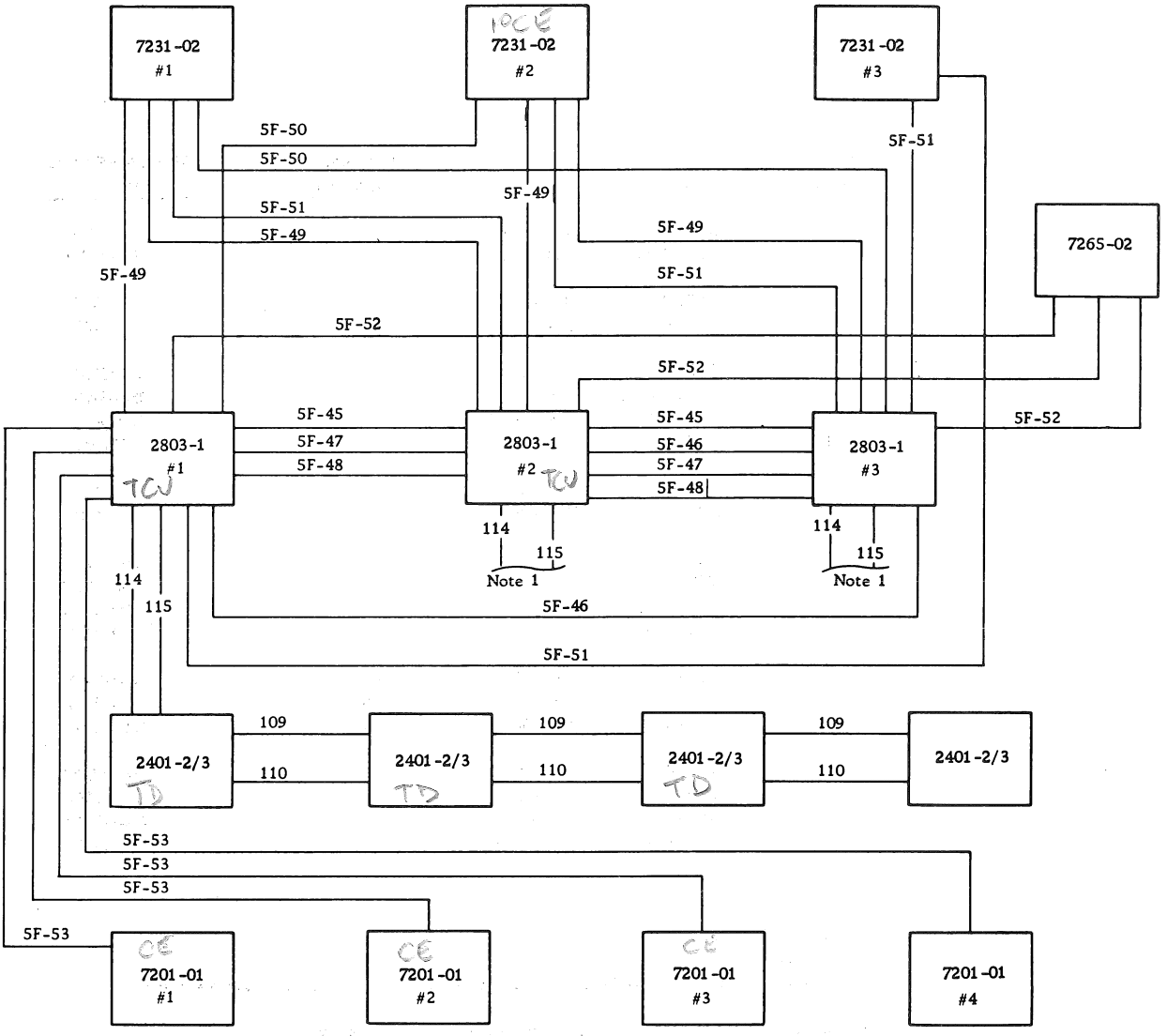
Figure 1-26. 7289-02 Peripheral Adapter Module Cabling Schematic (Cont'd).



Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 3)	Notes
109	1	2401-2/3	2401-2/3		100-325X	4
110	1	2401-2/3	2401-2/3		100-325X	4
114	1	2401-2/3	2803-1		100-325X	4
115	1	2401-2/3	2803-1		100-325X	4
5F-45	2	2803-1 #1	2803-1 #2		100-325X	5
	2	2803-1 #2	2803-1 #3		100-325X	5
5F-46	2	2803-1 #3	2803-1 #2		100	5
	2	2803-1 #3	2803-1 #1		100	5

Figure 1-27. 2803-1 Tape Control Unit Cabling Schematic.

Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 3)	Notes
5F-47	1	2803-1 #1	2803-1 #2		200-325X	5
	1	2803-1 #2	2803-1 #3		200-325X	5
5F-48	1	2803-1 #1	2803-1 #2		325X	5
	1	2803-1 #2	2803-1 #3		325X	5
5F-49	4	2803-1 #1	7231-02 #1		100-325X	5
	2	2803-1 #2	7231-02 #1		100-325X	5
	4	2803-1 #2	7231-02 #2		100-325X	5
	2	2803-1 #3	7231-02 #2		100-325X	5
5F-50	2	2803-1 #3	7231-02 #1		100	5
	2	2803-1 #1	7231-02 #2		100	5
5F-51	4	2803-1 #3	7231-02 #3		200-325X	5
	4	2803-1 #1	7231-02 #3		200-325X	5
	2	2803-1 #3	7231-02 #2		200-325X	5
	2	2803-1 #2	7231-02 #1		200-325X	5
5F-52	2	2803-1 #1	7265-02	100	100-325X	2
	2	2803-1 #2	7265-02	100	100-325X	2
	2	2803-1 #3	7265-02	100	100-325X	2
5F-53	1	2803-1 #1	7201-01 #1		100-325X	5
	1	2803-1 #1	7201-01 #2		100-325X	5
	1	2803-1 #1	7201-01 #3		200-325X	5
	1	2803-1 #1	7201-01 #4		325X	5

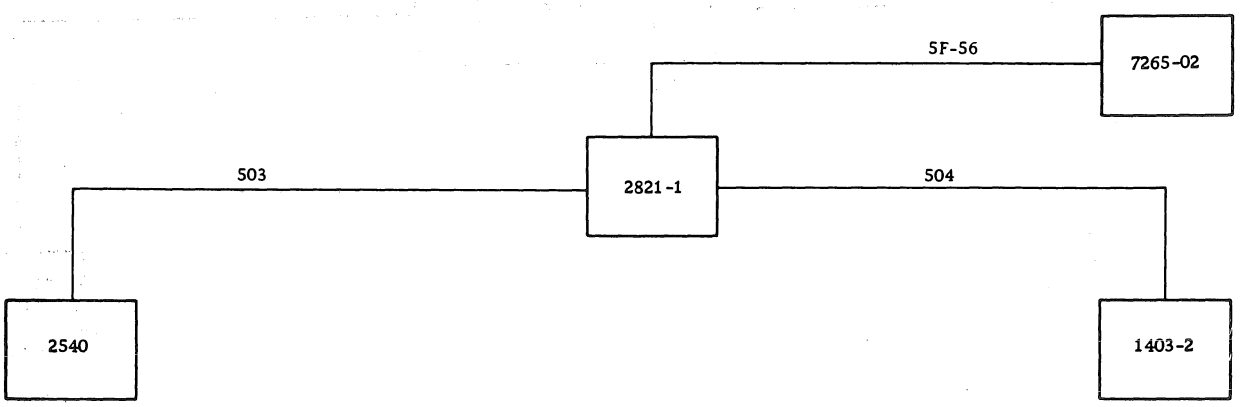
NOTES:

1. Same cabling as for 2803-1 #1.
2. EPO cable is included in this group.
3. To determine what cables are in a flight configuration, use those which indicate the configuration desired.

   Example: 100-325X includes the 100, 200, 325 and 325X (expanded) configuration.

4. Maximum total serial length should not exceed 100 feet. For example, 115 + 109, or 114 + 110 should not exceed 100 feet.
5. Refer to illustrations of maximum serial or loop cabling length for maximum cable length.

Figure 1-27. 2803-1 Tape Control Unit Cabling Schematic (Cont'd).



Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 1)	Notes
503	2	2540	2821-1	25	100-325X	
504	3	1403-2	2821-1	25	100-325X	
5F-56	3	2821-1	7265-02	50	100-325X	2

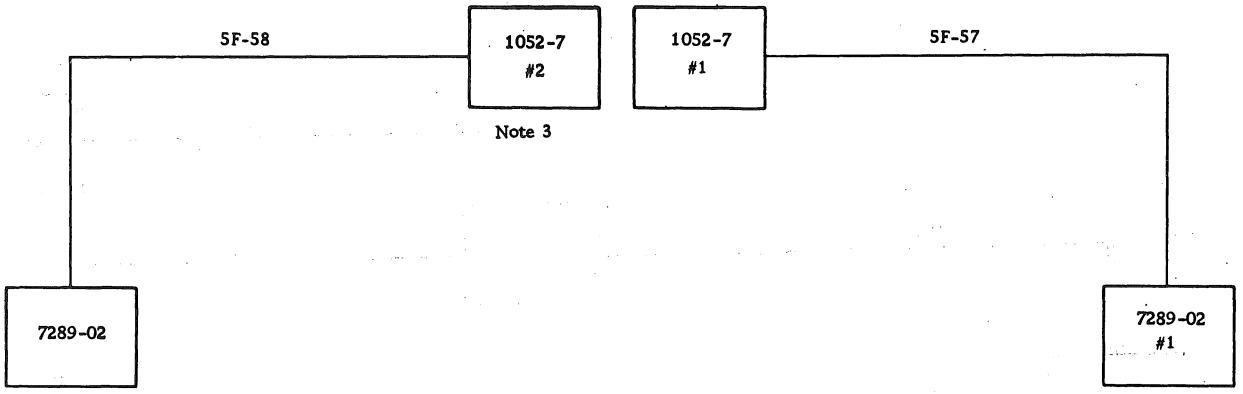
NOTES:

1. To determine what cables are in a flight configuration, use those which indicate the configuration desired.

   Example:. 100-325X includes the 100,. 200, 325 and 325X (expanded) configuration.

2. Power control cable is included in this group.

Figure 1-28. 2821-1 Control Unit Cabling Schematic.



Group No.	No. of Cables	From	To	Maximum Length (ft)	Flight Configuration (Note 2)	Notes
5F-57	3	1052-7 #1	7289-02 #1	300	100-325X	1
5F-58	3	1052-7 #2	7289-02	300	100-325X	1

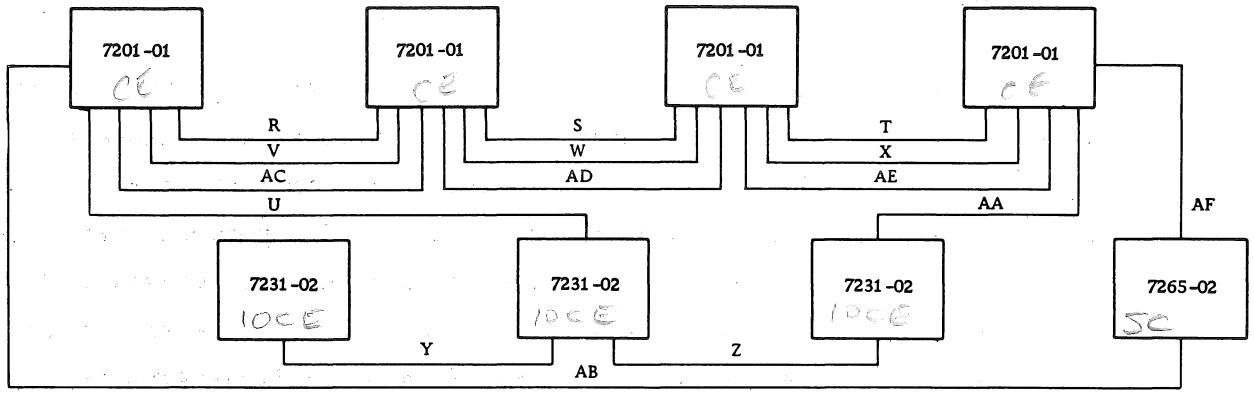
NOTES:

1. Power cable is included in this group.
2. To determine what cables are required in a flight configuration, use those which indicate the configuration desired.

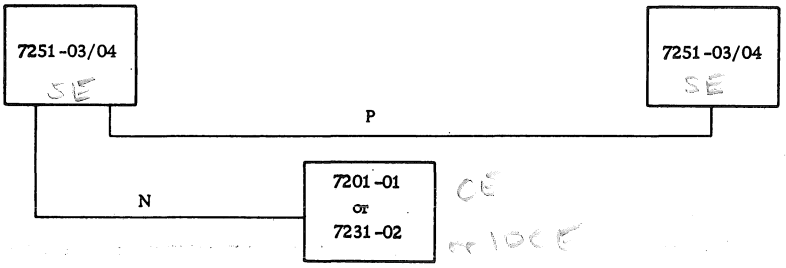
   Example: 100-325X indicates the 100-200-325-325X (expanded) configurations.

3. 1052-7 on reading board nearest the 7265-02 control panel is considered part of the console and is cabled internally. 1052-7 #2 (shown above) is optional, would be mounted on an extension to the 7265-02 Reading Board and would be cabled externally.

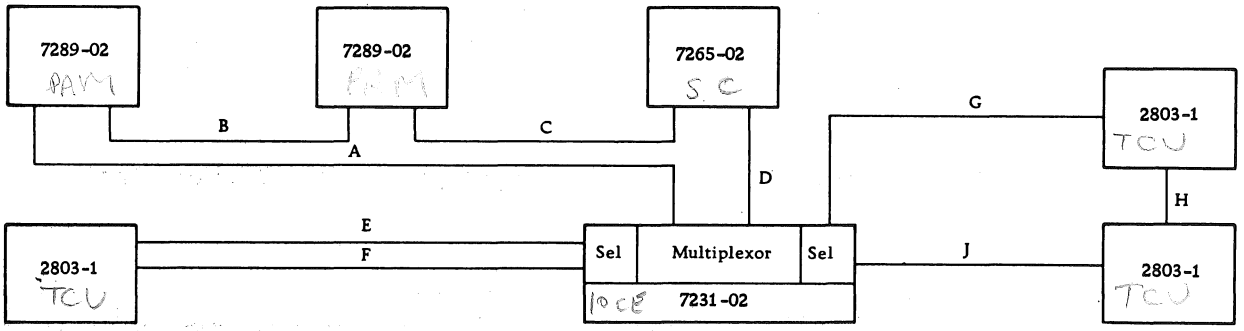
Figure 1-29. 1052-7 Printer-Keyboard Cabling Schematic.



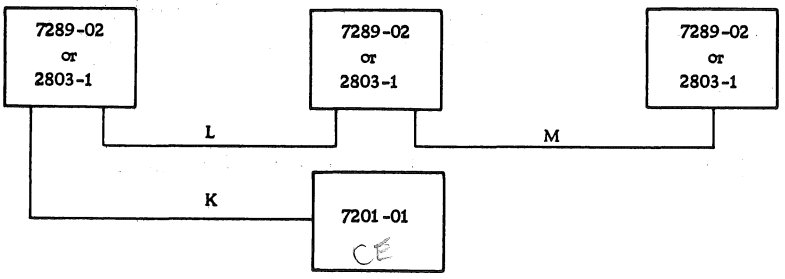
Maximum Cable Length Floor to Floor: R+S+T = 100'; U+V+W+X = 150'; Y+Z+AA = 150'; AB+AC+AD+AE+AF = 150'



Maximum Cable Length Floor to Floor: N+P = 60'



Maximum Cable Length Floor to Floor: A + B + C + D = 200'; G + H + J = 200'*; E + F = 200'*



Maximum Cable Length Floor to Floor: K + L + M = 150'

* The 200-foot maximum is for the units shown and should also be used as a planning guide when attaching other external devices to the 9020 System selector channels. However, there may be specific instances where greater distances are required. In these instances, consult the planning coordinator at the IBM-FAA Project Office.

Figure 1-30. Maximum Serial or Loop Cabling Length.

1-4. INTERFACE CABLING

In a data processing system composed of more than one element, it is essential that there be some form of interconnection between the various elements in the system. Since the IBM-9020 falls into this category, it might be well at this time to examine the interface cables present within this system. This interfacing provides a means of communication and control between the various elements. The cabling between elements in the 9020 System is generally carried on 20 conductor coax cables connected in one of four possible arrangements. The arrangements and a block diagram of each type are shown in Fig. 1-31.

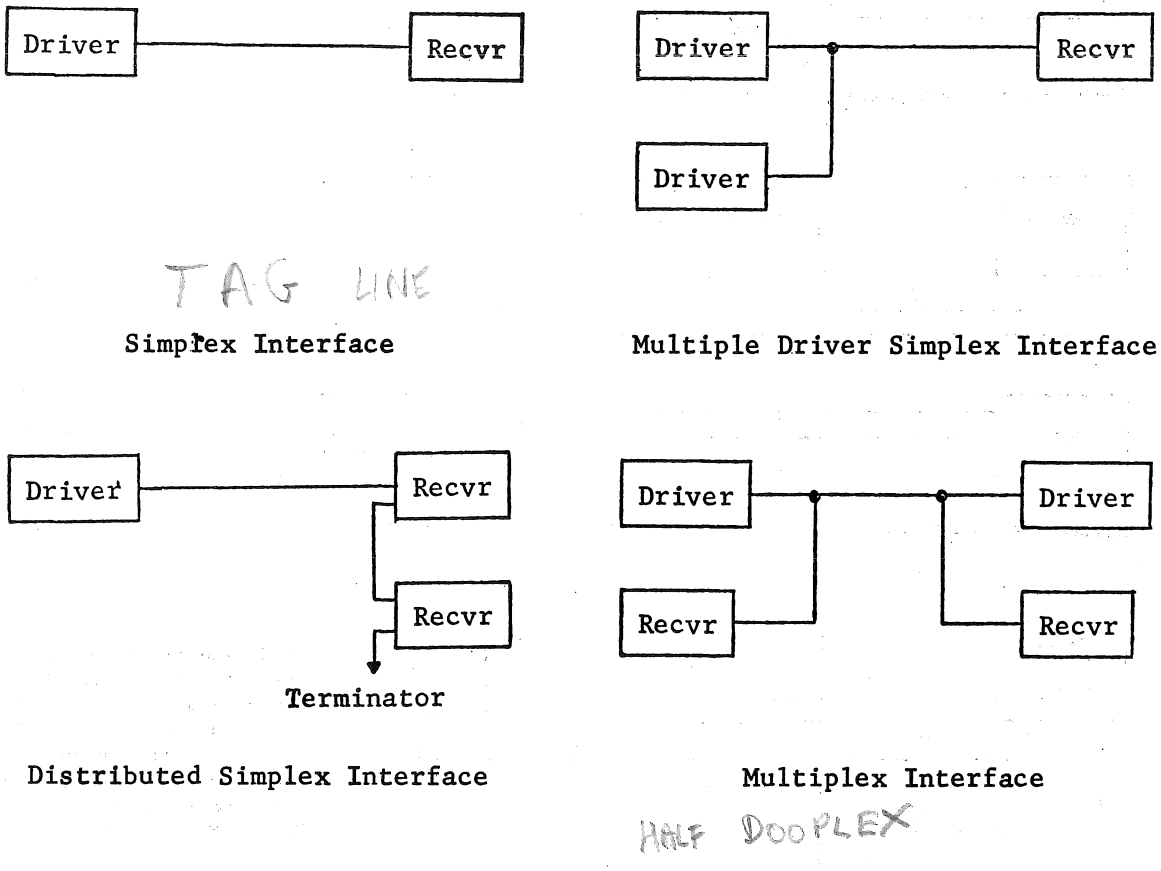


Figure 1-31. Interface Cabling.

In the simplex interface the communication takes place from the driver to the receiver. It is normally a unidirectional path.

The distributed simplex interface utilizes a data path from one driver to a series string of receivers. The data presented on the interface is thus available to all receivers simultaneously; normally only one of the receivers is conditioned to receive the data. The maximum number of receivers allowable on the distributed simplex interface is four.

The multiple driver simplex interface is a type where several drivers are capable of sending data to a single receiver. Normally only one driver will be active at a time. An example of this type of interface would be the connection between the CE and the System Console.

The multiplex interface is an example of a bidirectional connection where data or signals may be passed in either direction between the two boxes.

For purposes of explanation the interfacing paths between the elements of the 9020 System are divided into two categories. The DATA paths and the CONTROL paths. Figures 1-32 and 1-33 exemplify the data paths and control paths respectively while Fig. 1-34 represents overall combination for a simplified system.

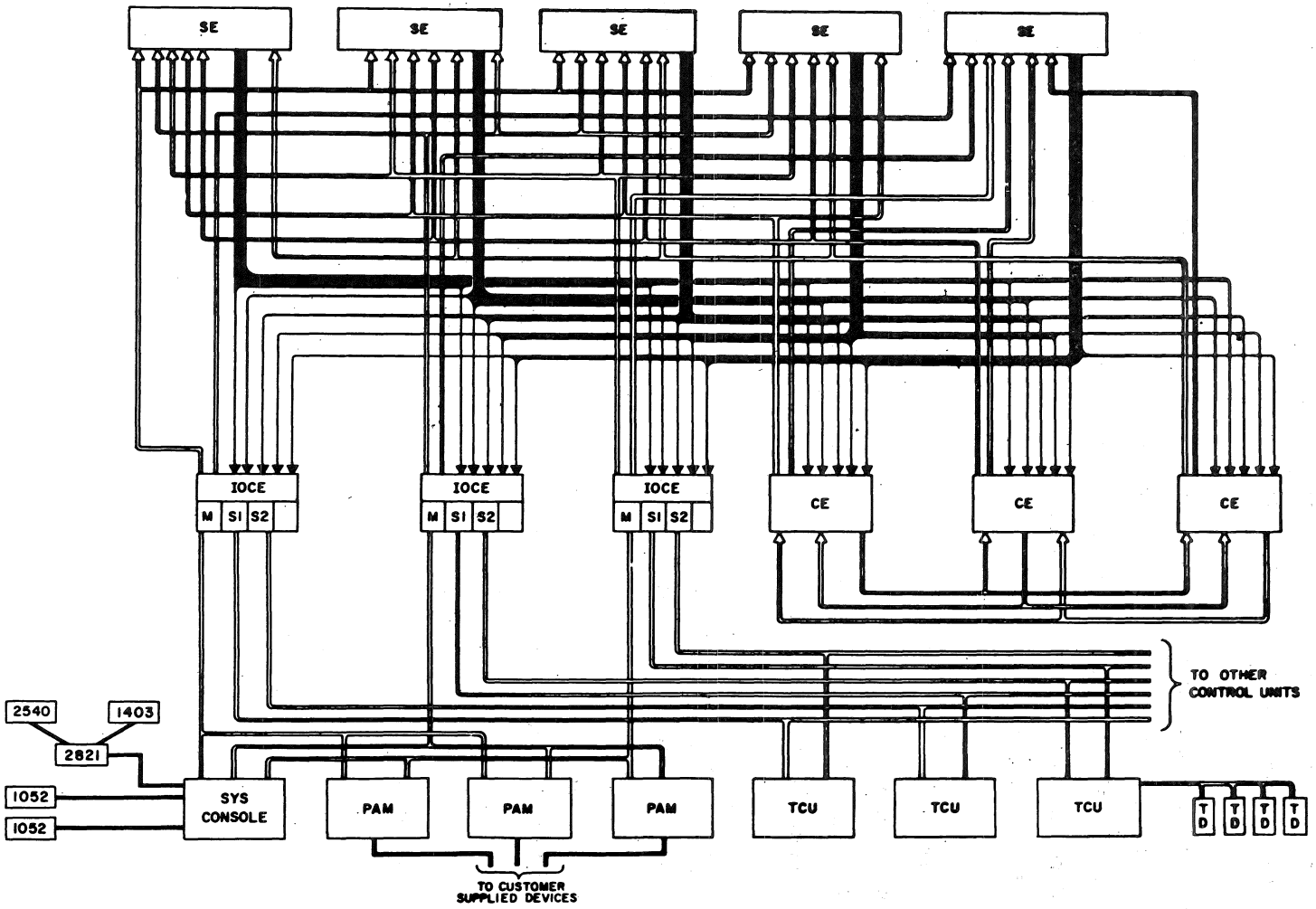


Figure 1-32. 9020 System Data Paths.

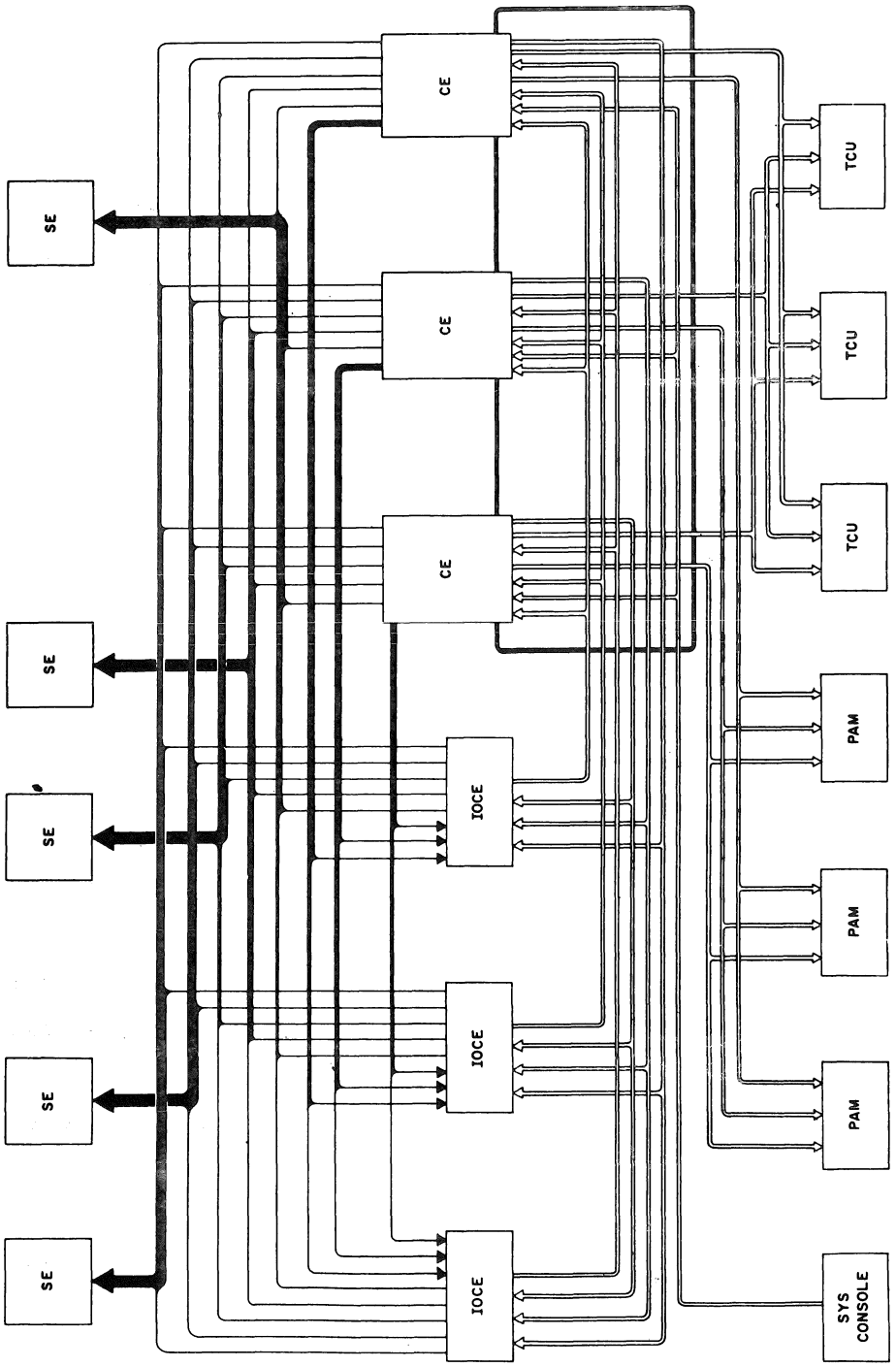
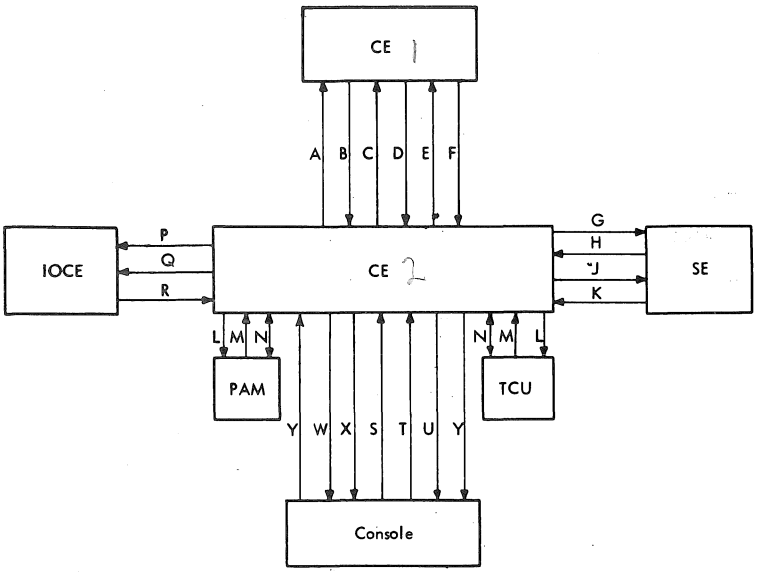


Figure 1-33. 9020 System Control Paths.



NOTE: The connecting lines are not cables; instead, they represent logical sets of interface lines keyed to subsequent figures.

Figure 1-34. CE Interfacing.

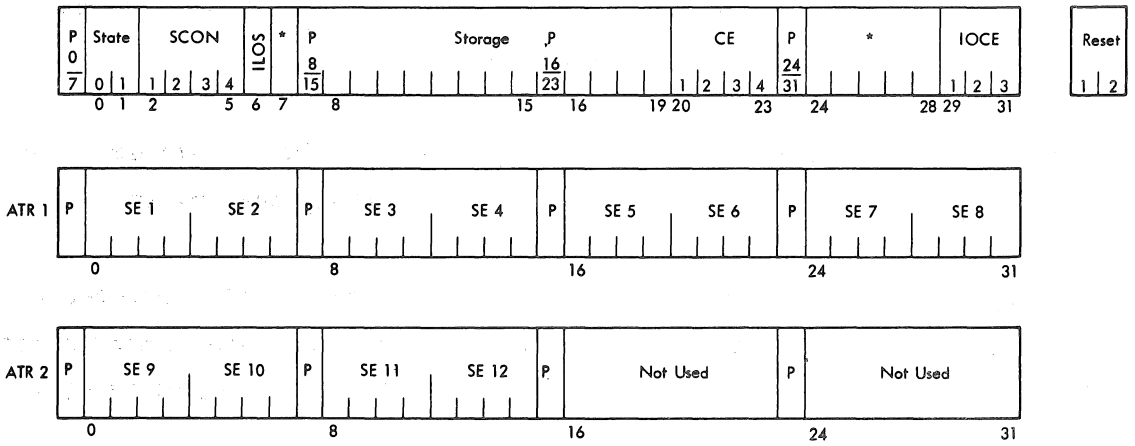
1-5. INTER ELEMENT CABLING

A. CE - CE Interfacing

The CE is the only element that directly communicates with other elements of its kind. Figure 1-35 shows the CE to CE interface lines. The intercommunication is concerned primarily with direct control operations which include data communication (one byte), and external CE starts and logouts. In addition to the direct control function there are controls for reconfiguration and element check monitoring.

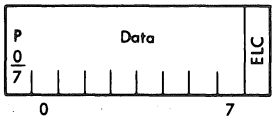
Control Bus: This bus is used for both configuration control and ATR assignment.

Configuration control (established by the configuration mask) is used to define which elements comprise a subsystem, and to avoid interference between



NOTE: The configuration and ATR mask originate from the external register.
The two system resets originate from control circuitry.
* Not Used

(a) Keys A and B



NOTE: This data byte is concerned with direct control.
The configuration mask, system resets, direct data byte, and ELC are distributed simplex originating in a CE and received by one or more CE's.

(b) Keys C and D

KEY E FIGURE 85 is a set of simplex lines as follows:

1. CE External Start Command Out
2. CE Logout Command Out
3. CE Write Direct Command Out
4. CE Read Direct Command Out
5. Reconfigure Select Out
6. Reconfigure Response Out
7. Address Translation Select Out

KEY F FIGURE 85 is a set of simplex lines as follows:

1. CE External Start Command In
2. CE Logout Command In
3. CE Write Direct Command In
4. CE Read Direct Command In
5. Reconfigure Select In
6. Reconfigure Response In
7. Address Translation Select In

NOTE: These simplex signals originate from direct control and configuration control circuitry.

(c) Keys E and F

Figure 1-35. CE to CE Interface Lines.

subsystems. The configuration control registers in the various elements will contain positions to define the other elements with which any given element may communicate at any given time. The CCR positions, or bits, enable or inhibit data and control paths between elements.

ATR assignment establishes a correlation between logical addresses referred to by the program, and actual storage elements within the system.

System Reset: 2.5 millisecond "double-railed" signals which precede a system IPL and perform both hardware and microprogram resets. The reset is not gated by the CCR. All bits in the CCR are reset to 0's except the SCON bits which are set to 1's.

Element Check (ELC): The element check signal is sent to all CEs within the system with the exception of itself. This signal may result from a CCR or ATR parity error, certain PSBAR stepping situations, and certain hard stops or CE error conditions.

Direct Control Bus: During execution of a write direct CE-to-CE data communication, this bus represents eight data bits and one parity bit fetched from a storage element. This byte of data remains as static signals until the next write direct instruction is executed.

CE External Start Command: This command is issued by a write direct instruction and causes the receiving CE to start execution after it obtains a new PSW from location 00000 of its PSA. The receiving CE must be properly SCON'ed to the sending CE to perform the external start operation.

CE Logout Command: This command is issued by a write direct instruction and causes the receiving CE to initiate logout procedures. The receiving CE must be properly SCON'ed to the sending CE to perform the logout operation.

CE Write Direct Command: This command is issued by a write direct instruction and indicates a data communication type operation between the sending and

receiving CEs. This command causes an external interrupt at the receiving CE by setting a unique bit in its external interrupt register, provided that the receiving CE is properly configured (CCR 20-23) to listen to the originating CE.

CE Read Direct Command: This command is issued by the read direct instruction and indicates that a byte of data has been taken from the direct data bus. The command causes an external interrupt at the receiving CE by setting a unique bit in its external interrupt register. The receiving CE must be properly configured (CCR 20-23) to the originating CE.

Reconfigure Select: A line carrying a 2.5 microsecond pulse from the CE to another CE, causing the CE to set into its configuration register the mask on the output bus. The CE will honor the select if the selector's SCON bit is on in the receiving CE's CCR.

Address Translation Select: This select line signals and conditions the selected CE for receiving the new address translation assignment mask on the 36-bit control bus. Three select pulses are required: one for initial selection, and two for transmission of ATR 1 and ATR 2.

Reconfiguration Response: A line sent to the CEs in response to configuration select, provided that the select was honored and the CCR parity is correct.

This response signal is also used as a set address translation response to acknowledge that: first, the receiving CE was properly SCON'ed and, second, the ATR 1 and ATR 2 assignment masks were properly received.

B. CE - SE Interfacing

Interfacing from the CE to an SE involves a data-out bus and associated control signals. The data-out bus is concerned with a variety of functions including: the transfer of data addresses, actual data itself, storage protect keys, and configuration masks. The various control signals define

the current usage of the data-out bus and synchronize the overall operations. Figure 1-36 indicates the distributed simplex and simplex lines concerned with the CE to SE Interfacing.

Interfacing from the SE to a CE involves an input bus and associated control lines. The input bus is concerned with the transmission of both normal data and logout data. The signals are used to synchronize the various operations and indicate check conditions within the SE. Note that the input bus and control signals are transmitted on simplex line, and not distributed simplex as was the case with the CE to SE interfacing. Figure 1-36 indicates the various simplex lines associated with the SE to CE interface.

Output Bus: A group of 36 lines carrying data and control information from one CE to one of four SEs. The accessed SE gates its receivers to accept the signals from the bus. During the first part of a cycle, 27 lines carry the address bits and parity, and 5 lines carry the storage protect key and parity. During the remainder of the cycle, if a store is called for, 36 lines carry data. During execution of a SCON instruction 15 lines carry the configuration mask.

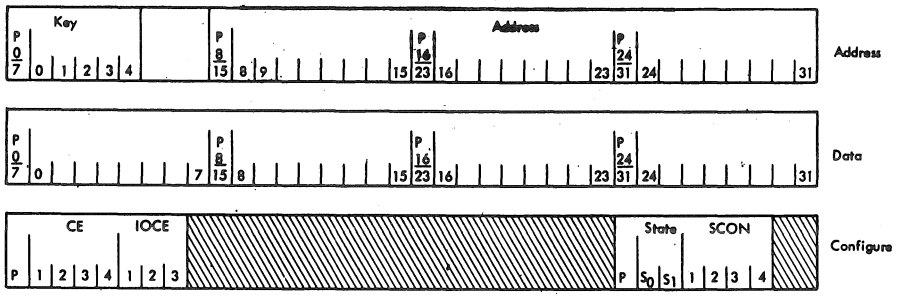
Access Request: A line by which the CE requests a storage cycle. The line rises at the beginning of the first machine cycle associated with a storage cycle, and stays static until the request has been accepted by the SE. The CE taken one or more dummy cycles, as required, while waiting for the acceptance; the number depends on the priority of the request.

Byte Stat Lines: Five lines, including parity, which indicate the bytes to be stored. There is no signal on these lines except when data is to be gated onto the output bus during a store operation.

used when only one byte is to be stored with the other 3 unchanged

Set Key: A line signaling the SE to store the key found on the output bus in the storage protect location specified by bits 15-20 of the SAR. The cycle accompanying this operation is a No-Operation; a word is fetched from

G

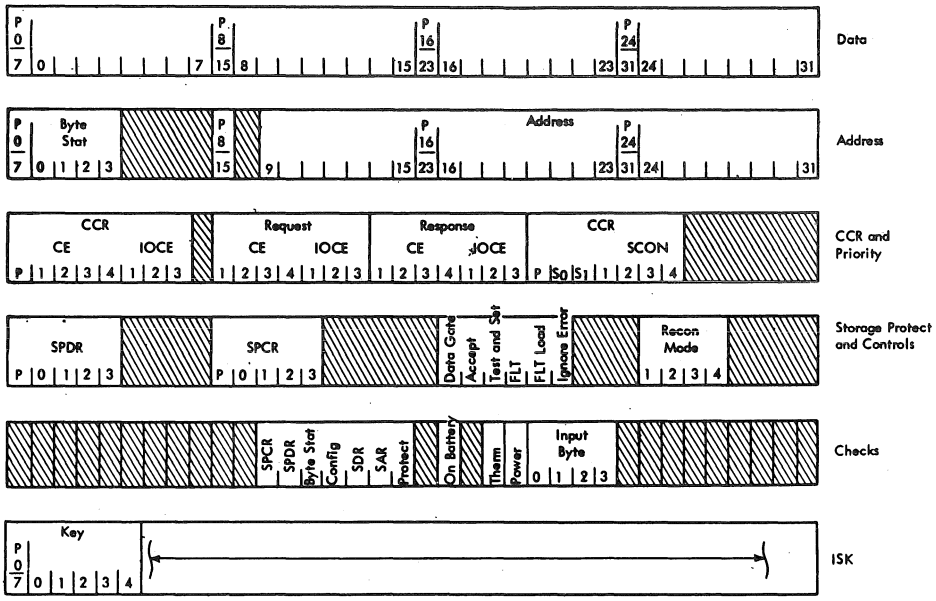


G

NOTE: These distributed simplex lines originate in one CE and are received by one to four SE's. The 36-bit bus is time-shared by the above formats.

(a) Key G CE to SE

H



H

NOTE: These simplex lines originate in one SE and are received by only one CE. The 36-bit bus is time-shared by the above formats. The formats shown are for normal storage operation (top) and SE logout.

(b) Key H SE to CE

J

1. Access Request
2. Byte Stat 0
3. Byte Stat 1
4. Byte Stat 2
5. Byte Stat 3

(See page 1-74)

6. Byte Stat Parity
7. Set Key
8. Insert Key
9. Reconfigure Select
10. Test and Set (PTO)
11. FLT Op
12. Split Cycle
13. Logout Proceed 1
14. Logout Proceed 2
15. Logout Proceed 3
16. Logout Proceed 4
17. Logout Proceed 5
18. Logout Complete
19. Logout Stop
20. Ignore Errors
21. System Reset A
22. System Reset B

J

Both must be up to do a system reset

NOTE: These are simplex lines originating from one CE to one SE.

(c) Key J CE to SE

K

1. Accept
2. Request Acknowledged
3. Gate Data
4. Storage Check
5. SE Stopped
6. Element Check
7. Protect Check
8. Reconfigure Accept

NOTE: These are simplex lines originating from one SE to one CE.

(d) Key K SE to CE

Figure 1-36. CE to SE Interface Lines.

the addressed location (any location within the block of 512 words associated with the key) and regenerated, but no data bytes are transmitted.

Insert Key: A line signaling the SE to fetch the key from the storage protect location specified by bits 15-20 of the SAR and place it on the input bus. The cycle accompanying this operation is a No-Operation; a word is fetched from the addressed location (any location within the block of 512 words associated with the key) and regenerated, but no data bytes are transmitted.

Reconfigure Select: A line carrying a 2.5-μsec pulse from the CE to the SE, causing the SE to set into its configuration register the mask on the output bus. The SE will honor the select if the selector's SCON bit is on in the SE's CCR.

Logout Stop: A line brought up by the CE when a parity error is detected on a fetch or when the SE issues a storage check on a store cycle, or when SE logout diagnose instruction is used. This signal stops the SE at the end of the cycle in process to allow the CE to proceed with a logout. The stop line prevents higher-priority elements from accessing the SE.

FLT Op: A line causing suppression of data checking during execution of a fault locating test. It permits bad data to be transmitted to the CE in order to check out the CE error detection circuits.

Test and Set: This signal line causes the contents of the location specified by the current address to be fetched and sent to the accessing element. The contents of the byte specified by bits 30 and 31 of the address are replaced with all 1's. All other information is unchanged.

Split Cycle: A line causing the SE to insert a delay of approximately 75 nanoseconds between the read and write portions of its cycle. It is brought up whenever the specific operation (store or fetch) is not specified by the

end of the first machine cycle following an access and is required to guarantee that data to be stored is available at the SE in time for the write portion of its cycle.

Logout Proceed: Five lines brought up in sequence as the CE executes a logout of the SE, following a logout stop signal. Each line requests a particular word of logout data from the SE. USUALLY with DIAGNOSE INSTR.

Logout Complete: A line brought up by the computing element to indicate completion of a logout or by subsystem reset during subsystem IPL to reset the logout stop condition.

System Reset: A double-railed signal (two lines) which precedes an IPL to reset the SE. The SESDR, SESAR, SPDR, and SPCR are set to 0's including parity. Check triggers are also reset. The system reset is not gated by the CCR. Instead, the CCR is reset to 0's with the exception of the four SCON bits which are set to 1's.

Ignore Error: A signal generated by PSW bit 13 to force the SE to accept and store data with wrong parity.

Input Bus: A group of 36 lines carrying data from one SE to one CE. During a normal cycle, if a fetch is called, 36 lines carry data and parity. During execution of an ISK instruction, six lines carry the storage protect key and parity. During logout, all lines carry logout data.

Request Acknowledged: A line carrying a dc signal, indicating that the SE receiving an access request has recognized the request and is configured to the CE.

Accept: A line acknowledging the receipt of an Access Request signal with a valid address and the availability of storage (i.e., no higher priority element also requesting access). The rise of accept indicates that the SE has stored the key and address, and that the CE may place data on the bus at

any time (store operation). The fall of accept on store indicates that the CE may restart.

Gate Data: A line indicating that data is about to be placed on the input bus during a fetch or Insert Storage Key (ISK) and the CE may restart.

Storage Check: A line brought up during any storage cycle, indicating one or more of the following:

1. A parity error in data received from the CE.
2. A parity error in data read from storage.
3. A parity error in address received from the CE.
4. An address not included in the SE which was accessed.
5. A parity error on the key received or read out.
6. Parity error on the byte stats received. Whenever bad data, address, or key is sent to the SE, a no-op cycle is taken to preserve the old and reject the new. The SE stops for 2.5 microseconds following the storage check signal to allow the receiving element to issue a logout stop.

Protect Check: A line brought up during a store or fetch operation in which the storage protect tag sent from the CE does not match the tag fetched from storage protect buffer, and neither tag is zero. This is a program check, not a hardware check. It does not cause a logout.

Element Check: An element check is sent to all computing elements without regard to the storage element configuration register or to accessing controls.

An element check pulse is issued when one of the following conditions is detected. (Other functions within the SE are not inhibited, except under storage check, and the SE will continue to function as normally as possible.)

1. CCR Parity
2. Thermal Check
3. On Battery
4. Storage Check

A static element check signal will be issued upon detection of one of the following conditions and will remain until the condition has been cleared:

5. Power Check
6. Power Off
7. Logout Stop Latch On

Reconfigure Response: A line carrying a pulse from the SE to the CE indicating that a reconfiguration operation has been completed and correct parity exists in the CCR.

SE Stopped: A line to any accessing CE indicating that the SE is in the process of being logged out.

C. CE - IOCE Interfacing

Interfacing for the CE to IOCE includes a control bus and associated signal lines. This control bus transfers a variety of information such as configuration masks, ATR assignment masks, I/O instructions, IPL and FLT operations, and PSBAR indications. The control bus is never used for the transfer of data. Control signals are used to define the information on the control bus and to synchronize the various operations.

Interfacing from the IOCE to the CE is concerned primarily with control type signals. The control bus which is used to transfer information from the CE to the IOCE is strictly a one-way bus, and performs no functions in this section. Programming restrictions allow an IOCE to be configured to only one CE at a time. Figure 1-37 shows the IOCE to CE interfacing lines.

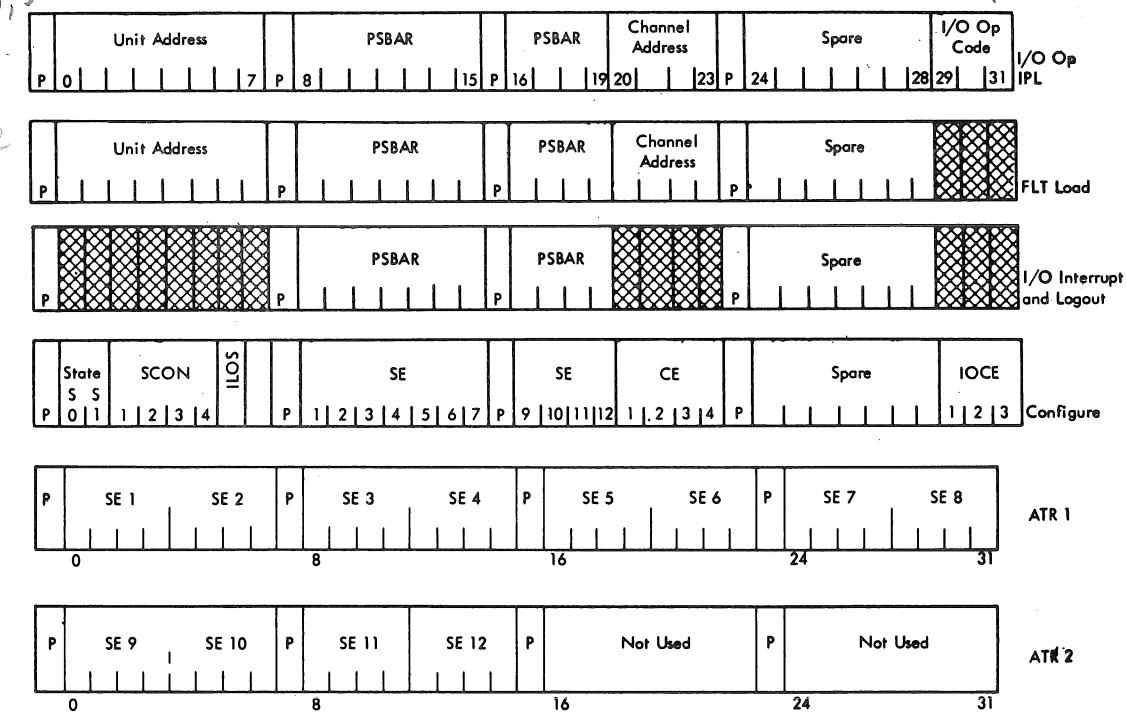
Control Bus: The control bus has 36 distributed simplex lines: 32 bit positions, plus 4 parity bits. The bus is time-shared between set configuration, ATR select, I/O instructions (with PSBAR), and channel unit addresses. The bus contains 22 bits for set configuration, 32 bits for ATR 1, 16 bits for ATR 2, 12 bits for the PSBA, 8 bits for the unit address, 4 bits for the channel address, and 3 bits for I/O instruction. The five I/O instruction lines (start I/O, test channel, test I/O, halt I/O, and set PCI), and the control line IPL, all use the PSBA and channel unit address. The two control lines, logout and permit interrupt, need only the PSBA.

360 Mode Operation: This signal causes the IOCE to operate in the 360 mode.

I/O Instruction: This line is sent to a selected IOCE. The preferential storage base address, unit address, channel address, and the decoded I/O instruction are placed on the control bus. The I/O instruction line is then brought up to tell the IOCE to take the information from the control bus. The line remains static until a response is received from the IOCE.

Configuration Select: Configuration select is three lines, one to each IOCE. Each line is generated from the select mask (SSR) and gates the configuration bits from the control bus into the IOCE. The IOCE must be configured to the CE.

Initial Program Load: This line, generated in the same manner as I/O instruction, indicates to the selected IOCE that it is to perform an IPL. The control bus contains the preferential storage base address and the unit and channel address when this line is brought up.



Note: These lines are distributed simplex originating in one CE and received by one or more IOCE's. The bus is 36 bits time-shared by the above formats.
Also included in these distributed simplex lines are:

1. System Reset (2 lines)
2. Subsystem Reset (1 line)
3. System Mask Bits 16-19
4. 360 Mode Operation

(a) Key P

CE to IOCE

1. I/O Instruction
2. FLT Load
3. Initial Program Load
4. Permit I/O Interrupt
5. IOCE Logout
6. Configuration Select
7. Simplex System Mask Bits
8. Permit Machine Check Interrupt
9. FLT Backspace
10. SATR Select
11. OBS From IOCE to CE
12. OTC From IOCE to CE

13. write direct start
14. write direct stop
15. write direct interrupt

} from IOCE to CE !

Note: These are all Simplex lines. TAG LINES

(b) Key Q

CE to IOCE except 11, 12

1. Condition Code (2 lines)
2. I/O Interrupt Request (simplex)
3. Machine Check Interrupt Request (simplex)
4. Configuration Response
5. Response
6. Check Response
7. Reset ROS Timeout
8. PSBAR Lockout
9. FLT Complete
10. Element Check (ELC)

Note: These are distributed simplex lines from one IOCE to one or more CE's

(c) Key R

IOCE to CE

Figure 1-37. CE to IOCE Interface Lines.

System Mask: The system mask lines are static lines from the CE's PSW register bits 0-6 and 16-19. These lines mask the channels in the IOCEs and are distributed as follows:

PSW bits 0-3 to IOCE 1

PSW bits 4-6, 16 to IOCE 2

PSW bits 17-19 to IOCE 3

PSW bits 16-19 to all IOCEs

Bits 16-19 are sent to all IOCEs and are used in forming the first portion of the PSW byte on channel interrupts.

Subsystem Reset: This is a reset line generated in the CE and sent to the IOCE. The IOCE must be configured to the sending CE. The IOCE's CCR is not affected by a subsystem reset.

System Reset: A double-railed signal (two lines) issued from the CE after that CE receives a system IPL from the system console or its own console. This signal performs both hardware and microprogram resets within the IOCE, provided the IOCE is not in state zero with the test switch ON. The CCR is reset to 0's with exception of the SCON bits which are set to 1's.

FLT Load: This line requests the IOCE to perform an FLT load from a selected tape unit into a specified SE.

FLT Backspace: This signal causes the IOCE to branch from its wait loop and backspace the FLT tape over one record. When the operation is completed, an FLT complete signal is returned to the CE.

Logout: This line is issued from a write direct instruction and causes the IOCE to begin a logout operation. The IOCE must be SCON'ed to the sending CE.

Permit I/O Interrupt: A line sent to the IOCE in response to an IOCE I/O interrupt request. This signal allows the IOCE to store its CSW and interrupt code field of the PSW.

Permit Machine-Check Interrupt Request: A line sent to a configured IOCE in response to a machine-check interrupt request. This signal allows the IOCE to continue with the logout.

Condition Codes: Two lines sent to the CEs as the result of an I/O operation indicating a value to be set into the PSW.

Response: A line sent to the CE to indicate that: the condition code for an I/O operation is present; IPL is complete; I/O interruption is complete (CSW and the interrupt code field of the old PSW are stored); machine check interrupt is complete (CLU logout).

I/O Interrupt Request: A signal from the IOCE informing the CE of status changes in the channels or I/O devices.

When a status change is detected by the IOCE and the channel is masked on, an I/O interrupt request is sent to the CE. The channel which requested the interrupt waits for a "permit I/O interrupt" from the CE before storing a channel status word which indicates the reason for the interrupt request.

Also stored are the channel and unit address, IOCE address, and mask bits 16-19 in the interrupt code field for the old PSW. If the channel control check or the interface control check bit is on in the CSW, a selector channel logout has been performed.

Machine Check Interrupt Request: The detection of a CLU error by an IOCE causes the IOCE to stop and request a PSBA for logout via the machine check interrupt request.

A CE in an I/O instruction or interrupt process with the IOCE issuing the machine check interrupt request terminates the process and proceeds to the next I-Fetch. That I-Fetch, or any I-Fetch, has an exception branch to a special microprogram routine. This routine issues a "permit machine check interrupt" and enters a timing loop while the IOCE performs a logout. The IOCE holds up "reset time out" while logging out. The CE waits for a response line or, in the event of further IOCE error, a time out. In either case, the CE completes a machine check interrupt by storing and fetching the correct PSWs. No logout occurs in the CE. The old PSW contains the IOCE identity in the interrupt code as follows:

	Bit	
IOCE	30	31
1	0	1
2	1	0
3	1	1

A time out condition should always be accompanied by an IOCE element check. Simultaneous I/O interrupt requests or MC interrupt requests from multiple IOCEs are serviced in priority of IOCE 3, 2, and 1.

Element Check: This signal is issued by an IOCE as a pulse whenever:

1. A parity error is detected in the ATR.
2. An error condition is detected requiring a CLU or selector channel logout.

The element check signal is issued as a static condition if, during a CLU logout, the IOCE detects a condition which will not permit logout to be performed. An element check signal causes an external interrupt in the CE.

On Battery Supply: This signal, when issued as a static condition to the CE, indicates that the IOCE is operating on its battery supplies.

The OBS signal is issued as a pulse whenever a CCR parity is detected during execution of the SCON operation in the IOCE.

The OBS signal causes an external interrupt in the CE.

Out of Tolerance: A signal to the CE indicating that the IOCE temperature sensing thermals have detected an out-of-bounds temperature. This signal causes an external interrupt in the CE.

FLT Complete: A response to the CE indicating that the operation initiated by the FLT load or the FLT backspace request has been completed.

PSA Lockout: A line indicating that the IOCE tried to access the PSA but did not receive a reply from the storage element accessed or that the PSA access was issued to a logout-stopped SE. This signal causes a program interruption in the CE.

Reset ROS Time Out: A signal sent to the CE indicating that the IOCE will process the I/O instruction but is presently processing data. The signal resets the CE's countdown loop to its maximum value, preventing it from timing out.

Configuration Response: A response sent to the CE after the SCON instruction has been accepted and the IOCE has set its CCR without detecting a parity error in the CCR.

This response signal is also used as a set address translation response to acknowledge that: first, the receiving CE was properly SCON'ed and, second, the ATR 1 and ATR 2 assignment masks were properly received.

Check Response: A signal line to the CE indicating that a parity check has been detected in the IOCE on data from the CE via the control bus.

When in FLT mode, this signal indicates that a tape error was detected during an FLT load operation.

D. CE - PAM and TCU Interfacing

Interfacing between the CE and PAM is similar to that between the CE and TCU. These lines, for the most part, represent reconfiguration, system reset and element checks. Other than these lines, there is no control or data flow directly to or from the CE. Figure 1-34 shows overall CE interfacing. Figure 1-38 shows interface formats between the CE and the PAM/TCU.

Configuration Mask: Only the required 11 positions of the overall configuration mask are sent to the PAMs and TCUs. The items sent include the two state bits, the 4-bit SCON field for reconfiguration, and the 3-bit field to define the controlling IOCEs. Two parity bits are used in the transfer.

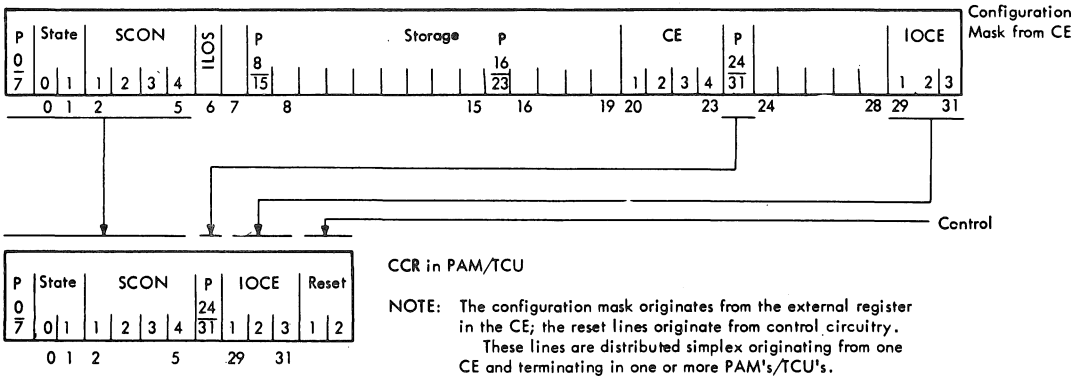
System Reset: 2.5 millisecond "double-railed" signals which precede a system IPL and perform hardware resets. The reset is not gated by the CCR. All bits in the CCR are reset to 0's except for the SCON bits which are set to all 1's.

Configuration Select: A line carrying a 2.5 microsecond pulse causing the PAM/TCU to set the configuration mask into its CCR. The PAM/TCU will honor the select if the selector's SCON bit is on in the receiving PAM/TCU's CCR.

Element Check: A static simplex signal is sent from each PAM and TCU to each CE.

An element check from the PAM indicates:

1. Parity Check in the CCR.
2. Check-stop error in priority controls.
3. Power failure.



NOTE: The configuration mask originates from the external register in the CE; the reset lines originate from control circuitry. These lines are distributed simplex originating from one CE and terminating in one or more PAM's/TCU's.

(a) Key L

1. Element check (ELC) from PAM's 1, 2, and 3
2. Element check (ELC) from TCU's 1, 2, and 3

NOTE: These six simplex lines originate one from each PAM and TCU. These lines are in the same cable as key L.

(b) Key M

1. Configuration Select/Configuration Response signal between the CE and each PAM and TCU.

NOTE: These six multiplexed lines have both a driver and a receiver on the same line.

DUPLEX or ½ DUPLEX

(c) Key N

Figure 1-38. CE to PAM/TCU Interface Lines.

An element check from the TCU indicates:

1. Parity check in the CCR.
2. Power failure.

Configuration Response: A line sent to the CE in response to configuration select if the select was honored and the CCR parity was correct.

E. CE - System Console Interfacing

The CE - system console interfacing is concerned primarily with sending indication (status) signals from the CE to the System Console, and control signals from the System Console to the CE.

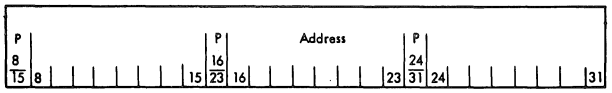
The CE cannot initiate any data flow directly to the System Console. Subsystem configuration indications, for example, which are under program control at the System Console, are initiated by the CE and handled as a normal I/O operation via the IOCE.

All System Console controls to the CEs (except for emergency power off) are gated by the system interlock switch which requires a key operation to activate logic. In addition, all functions going to the CE (except for "all stop") are further gated in the appropriate CE by a "select CE" signal originating from the select CE rotary switch on the System Console. Figures 1-32, 1-33, and 1-39 show system console to CE interface lines as referred to Fig. 1-34.

Many of the indications from the CE to the System Console represent the current status of the CE. The most important dynamic indications include the state of the CE, logic checks, and manual and wait status.

Storage Data Register: These multiple-driver simplex lines originate in one or more CEs and terminate in one set of indicators at the System Console. During manual display operations, these indicators display either the contents of main storage (SDR) or local storage (L register) at the selected CE.

Instruction Address Register: These simplex lines originate in each CE and terminate in separate rows of indicators at the System Console to continuously indicate the contents of each CE's IAR.



NOTE: These are simplex lines originating in one CE and terminating at the system console.

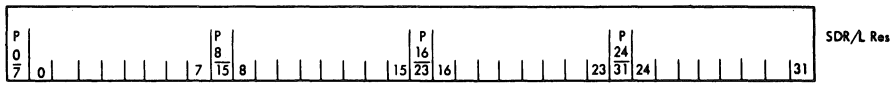
(a) Key U

The following are miscellaneous simplex indicator lines originating at a CE and terminating at the system console.

1. Manual Indicator
2. Wait Indicator
3. State Three Indicator
4. State Two Indicator
5. State One Indicator
6. State Zero Indicator
7. Logic Check Indicator

Several simplex lines.

(b) Key X



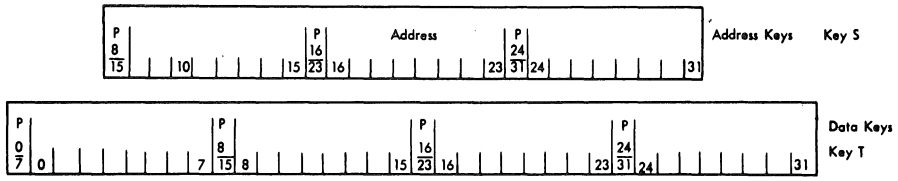
These are multiple driver simplex lines originating in one or more CE's and terminating at the system console. These lines are time-shared between the displaying of SDR or L register for local store display.

(c) Key V

The following multiple driver simplex lines are driven by one or more CE's and terminate at the system console:

1. Load Indicator
2. Invalid Selection

(d) Key W



NOTE: These are distributed simplex lines originating in the system console and terminated at one or more CE's.

(e) Keys S and T

The following are distributed simplex lines originating in the system console and terminated in one or more CE's.

1. Select CE (4 lines)
2. Interrupt
3. All Stopped
4. Stop
5. Start
6. Store
7. Display
8. Store Select Main
9. Address Keys (27 lines)
10. Data Keys (36 lines)
11. Control CE (4 lines)
12. Activate
13. Load Unit Address Bits (9 lines)
14. Load Channel Address Bits (5 lines)
15. Load Storage Select Bits (5 lines)
16. Address Compare Stop
17. Address Compare Loop
18. Set IAR
19. Rate Instruction Step
20. Load

(Set 10)

(f) Key Y

Figure 1-39. CE to System Console Interface Lines.

Manual Indicator: These simplex lines originate in each CE and terminate in a unique indicator at the System Console to indicate when the associated CE is in the stopped state.

Wait Indicator: These simplex lines originate in each CE and terminate in a unique indicator at the System Console when the wait bit in the associated CE's PSW is set to 1.

State Indicators: These four simplex lines originate in each CE and terminate in unique indicators at the System Console. One and only one of these four signals will always be active to reflect the present status of the originating CE.

Logic Check Indicator: These simplex lines originate in each CE and terminate in a unique indicator at the System Console to indicate that the CE has detected one of its own logic check conditions.

Power Check: A signal line indicating that the temperature in the CE has drifted to within approximately 10% of the shut-down tolerance. The signal also indicates the loss of voltage, normal power off, or an element master power off condition.

Battery: A signal indicating that the CE has switched to battery power.

Load Indicator: This multiple driver simplex line originates in one or more CEs and turns on a common indicator. The indicator is lit by the respective CE from the time an IPL operation starts until the operation is complete.

Invalid Selection: This multiple driver simplex line originates in one or more CEs and turns on a common indicator. The selected CE lights the indicator whenever an invalid or illegal storage address is specified by the operator during a manual operation.

Select CE 1-4: These four select lines result from the four-position rotary switch at the System Console. Proper CE selection is under switch card control in the receiving CEs. This signal provides the necessary gating in the CEs for all manual operations (except "all stop") issued from the System Console. The system interlock (key) switch must be turned on for this select switch to be enabled.

Interrupt: This signal results from depression of the interrupt key and causes a console interrupt signal which sets bit 25 in the PSW of the selected CE.

All Stopped: This signal causes all CEs to enter the stopped state. The system interlock switch must be turned on to activate the all stop key, but the setting of the select CE switch does not affect this operation.

Stop: This signal places the selected CE in the stopped state without destroying its environmental status. The selected CE proceeds to the end of the instruction being executed at the time the stop is initated. If the current instruction causes a program interrupt, the change of program status words (PSW) will be accomplished before stopping. An I/O device will be allowed to complete its operation although I/O or external interrupts will not be recognized.

Start: This signal starts the selected CE. If start is issued after a manual stop, the CE continues as if no stop occurred.

Store: This signal causes the selected CE to store the contents of the System Console storage data keys in the storage location specified by the 24 address keys and the storage select switch.

Display: This signal causes the selected CE to place the contents of a storage location specified by the address keys and storage select switch into the System Console display register.

Store Select Main: This signal results from the storage select switch being in the main storage position and causes main storage addressing at the selected CE during either fetch or store manual operations. This signal line is not active with the storage select switch in the local store position and causes local storage addressing at the selected CE.

Address Keys: These 24 signal lines (+3 parity) result from the 24 instruction address keys on the System Console and provide addressing of any addressable local store or main storage location.

Data Keys: These 32 signal lines (+4 parity) result from the 32 storage data keys on the System Console and provide manual data for storing into any addressable local store or main storage location.

Control CE: These four signal lines (+ parity) result from individual switches on the System Console and allow manual setting of the SCON bits in the configuration register. Actual setting of the SCON field occurs with depression of the activate key on the System Console.

Activate: This signal causes the SCON bits at the selected CE to be set according to the setting of the control CE switches on the System Console.

Load Unit Address Bits: These eight signal lines (+ parity) result from two of the three rotary-type load unit switches on the System Console. These two hexadecimal characters provide an I/O unit address for use during IPL operations.

Load Channel Address Bits: These four signal lines (+ parity) result from one of the three rotary-type load unit switches on the System Console. This hexadecimal character selects one of the eleven possible channels on the 9020 System.

Load Storage Select Bit: These four signal lines (+ parity) result from a rotary main storage select switch on the System Console. This hexadecimal

character represents a main storage element to be selected during IPL, or manual operations.

Address Compare Stop: This line conditions the selected CE so that any storage access to the address specified in the System Console Address Keys causes the CE to enter the stopped state at the end of the instruction that made the memory reference.

Address Compare Loop: This line causes the selected CE to loop between the address set in the System Console Address Keys and the address set in the System Console Storage Data Keys. When the selected CE makes a memory access to the address specified in the address keys, an unconditional branch is made to the address specified in the storage data keys. Programming can establish a loop condition between the two sets of keys.

Set IAR: This signal transfers the contents of the system console address keys into the IAR of the selected CE.

Rate Instruction Step: This signal operates with the selected CE and the start and stop keys on the System Console. With this signal, each depression of the start key results in one complete instruction being executed. Any machine instruction can be executed in this mode.

Load: This signal line initiates an IPL in the selected CE.

F. IOCE Interfacing

The IOCE is primarily concerned with the movement of data both to and from the I/O equipment. The IOCE therefore is connected to the PAMs, TCUs, and SEs to act as a control and synchronizing element in the transfer of data both into and out of the main system.

As described in a previous section, communication between IOCE and CE is necessary for the initiation, control, and monitoring of the various I/O

operations. This communication is strictly concerned with control as there is no data transfer between the CE and the IOCE. Therefore, the interfacing between IOCE and other elements are the subject of the discussion to follow.

The basic interfacing with the IOCE is shown in Fig. 1-40.

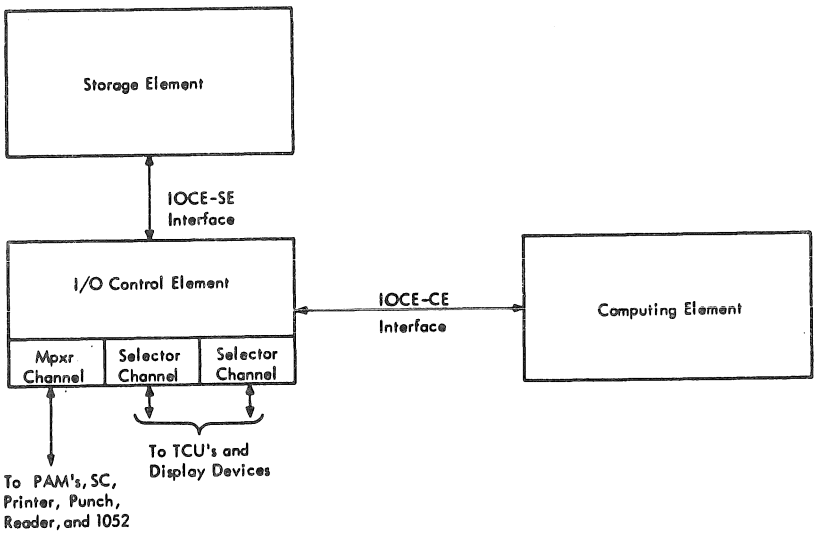


Figure 1-40. Basic IOCE Interfacing.

G. IOCE - SE Interfacing

Interfacing between the IOCE and SE is similar in many respects to the one described previously between the CE and SE. The following section will, therefore, show the differences between the CE/IOCE-SE interfaces.

FLT Load: This signal is used when loading FLTs into the system, and causes the OR'ing of data on the SE bus with the data in the storage location addressed by the IOCE. The OR'ing is under byte stat control, and the OR'ed data is returned to the addressed location in storage.

Suppress Log Check: This signal causes suppression of checking at the Storage Element Storage Data Register (SESDR) and input switch, and allows data with incorrect parity to be stored into the indication location.

H. IOCE - SC Interfacing

The System Console is also addressable by means of the standard System/360 I/O interface. A series of channel commands can, for example, be used to sound a bell or buzzer, set the mode indicator, set the programmable configuration lights, and read the sense key settings.

In addition to the programmable indications sent to the System Console, several static signals are sent directly to the System Console Panel. These indications include:

Element States: Four indicators representing states three, two, one, and zero.

Logic Check: An indication that a logic check has occurred in the IOCE.

Power Check: An indication that the temperature in the IOCE has drifted to within 10% of the shutdown tolerance. This indication includes loss of voltage, a normal power off, or a master power off condition.

Battery: An indication that the IOCE has switched to battery power.

These are dynamic indications and are not under direct program control.

I. SE Interfacing

The Storage Element, as has been stated in previous sections, is directly interfaced with both the CE and IOCE. This interfacing is concerned primarily with the transfer of information in the form of both data and instructions to

and from these two major elements. In addition, control signals provide the proper timing and synchronization for the intercommunications.

Inferfacing between the SE and System Console is on a one-way basis, to the System Console. The System Console exerts no direct control over the SE except, of course, for an emergency power-off condition.

Indications from the SE to the System Console include:

Element States: Four indicators representing states three, two, one, and zero.

Logic Check: An indication that a data check, address check, key check, or protect check has occurred in the SE.

Power Check: An indication that the temperature in the SE has drifted to approximately 10% of the shutdown tolerance. This also indicates a loss of a voltage, a normal power off, or an element master power off condition.

Battery: An indication that the SE has switched to battery supply.

These signals from the SE dynamically indicate their respective conditions at the lights on the System Console Operator's Panel.

J. PAM Interfacing

PAM interfacing between the CEs is concerned primarily with reconfiguration, resets, and element checks. Data bytes are not transmitted directly between the PAM and CE.

Interfacing between the PAM and the IOCE is based on the standard System/360 I/O interface. Information passed between the PAM and IOCE is on a byte basis and can represent data, commands, and sense and status bits.

Interfacing from the PAM to the System Console consists of the following indications:

Element States: Four indicators representing states three, two, one, and zero.

Logic Check: An indication that a logic check has occurred in the PAM.

Power Check: An indication that the temperature in the PAM has drifted to approximately 10% of the shutdown tolerance. This also indicates the loss of a voltage, a normal power off, or an element master power off condition.

These signals from the PAM dynamically indicate their respective conditions at the lights on the System Console Operator's Panel. Note that there is no battery indication. The PAM has no battery backup supply.

Communication between the PAM and the I/O devices is based on unique interfacing for each of the various classes of devices. These interfaces differ because of the data rates and formats. Each interface has the necessary data lines and controls to perform the required functions.

K. TCU Interfacing

TCU interfacing between the CEs is similar to that of the PAM; i.e., concerned primarily with reconfiguration, resets, and element checks. Data bytes are not transmitted directly between the TCU and CE.

Interfacing between the TCU and IOCE is based on the standard System/360 I/O interface. Interfacing between the TCU and the System Console is, again, on a one-way basis consisting of the following indications:

Element States: Four indicators representing states three, two, one, and zero.

Logic Check: An indication that a logic check has occurred in the TCU.

Power Check: An indication that the temperature in the TCU has drifted to approximately 10% of the shutdown tolerance. This also indicates a loss of a voltage, a normal power off, or an element master power off condition.

These signals from the TCU dynamically indicate their respective conditions on the System Console Operator's Panel. Note that there is no battery indication. The TCU has no battery backup supply.

L. System Console Interfacing

Interfacing between the System Console and the major elements within the system has been covered and explained in the preceding sections. The majority of interface signals take the form of element state and check conditions. Therefore, many of the interfaces are of a one-way nature.

Because the System Console is the main control console within the system, many interface lines extend to the CE to enable manual operator intervention for starting, stopping, altering, and monitoring the overall operation. These various functions have been explained already in the Computing Element Interfacing section. The System Console is the only major element in the system which is not duplicated. Therefore, all of the essential System Console functions have been duplicated at the CE Operator's Panel.

The System Console is also under limited program control by the EXC control program. Therefore, the standard System/360 I/O interface which connects with the IOCE multiplexor channel provides a path for both sense and control I/O functions. In these cases, the System Console is treated as just another I/O device.

1-6. SYSTEM COMMUNICATIONS

To demonstrate the use of the heretofore discussed tag lines between individual elements within a system the following examples are presented:

A. CE to CE and IOCE Communications

In the proposed ATC program, at the time of this writing, it is anticipated that only one CE will have control of all IOCEs at any particular time. Therefore, only one CE will be able to issue a Start I/O to an IOCE. If a CE, not configured to communicate with an IOCE, is executing a program requiring an I/O operation, it must be able to initiate this I/O operation through the CE that is configured to communicate with the IOCEs. A method of accomplishing this is provided by allowing CEs to communicate via the Read and Write direct instruction with each other.

Assume that you have a system executing an ATC type of program, and within that system the following elements are configured:

1. Two CEs, consisting of CE1 and CE2.
    a. CE2 is configured to communicate with all IOCEs.
    b. CE2 is configured to communicate with CE1 and vice versa.
2. One IOCE.
3. An input/output device.

Assume that CE1 is executing a program that requires an I/O operation. Since CE1 is not configured to communication with the IOCE, it must initiate the I/O operation via CE2 which is configured to communicate with the IOCE. This is accomplished by CE1 issuing a write direct instruction to CE2 (refer to the flow diagram shown in Fig. 1-41).

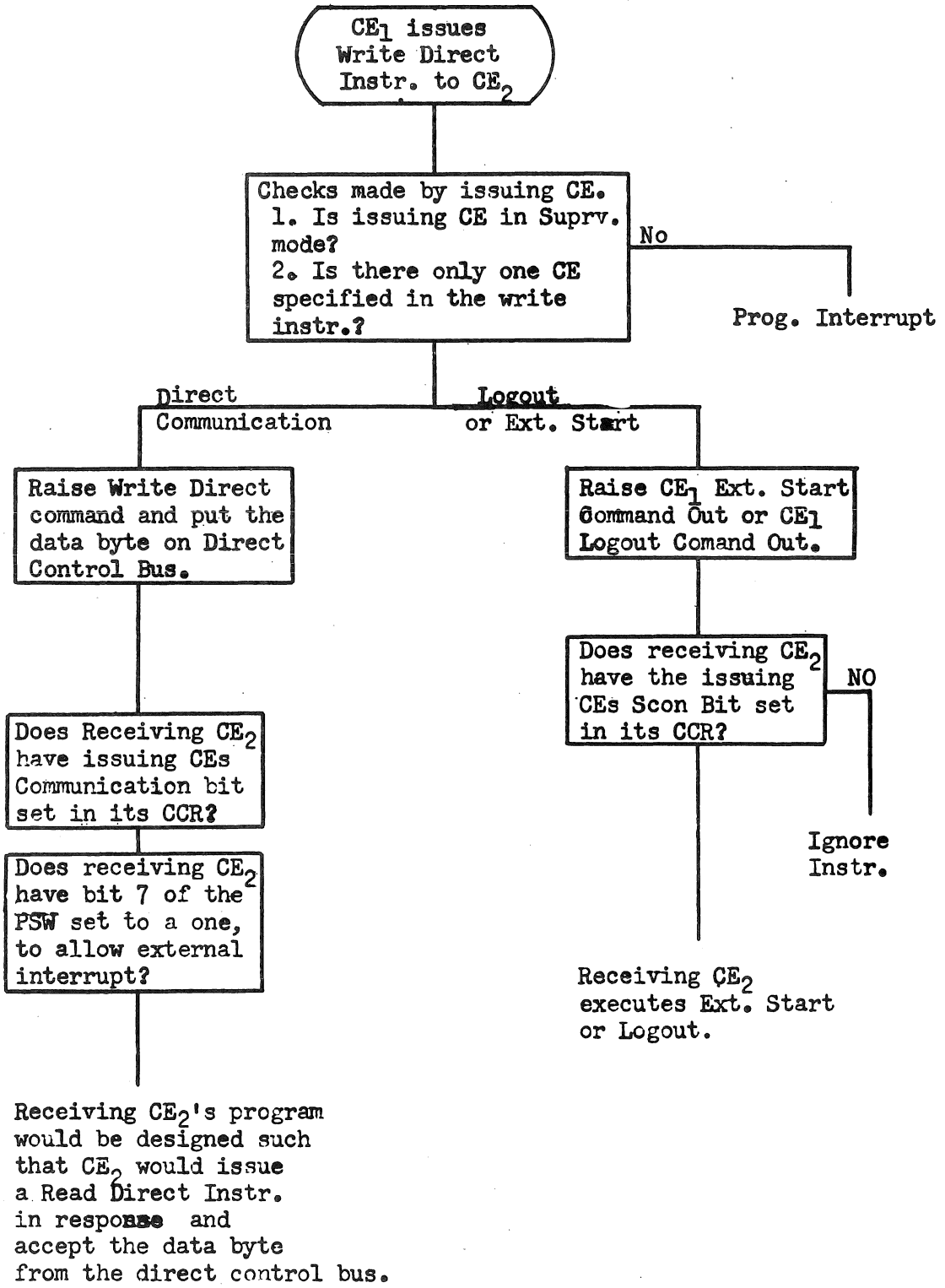


Figure 1-41. CE Issues Write Direct.

CE1, if it is in the supervisory mode and there is only one CE specified in the write direct instruction, will execute the instruction placing a byte of data on the Direct Control Bus and subsequently raise the Write Direct Control line to CE2. This notifies CE2 that a byte of data is available on the Direct Control Bus.

If the receiving CE (CE2) has CE1 communication bit set in its configuration register and its PSW bit 7 set to a one, CE2 will take an external interrupt when it completes its current instruction. As a result, if the programmer has provided it, the program branch is in CE2 due to the PSW swap will execute a Read Direct instruction which accepts the data byte transferred as a result of the Write Direct. The data byte could be the coded information that causes CE2 to initiate a SIO. Upon the execution of the Read Direct instruction a read direct control line is raised back to CE1. As a result CE1, if properly masked will take an external interrupt. If the programmer has provided the program which will issue a second Write Direct, CE1 will be able to transfer a second byte of data to CE2. This operation would be repeated between CEs until all the necessary information needed for CE2 to handle the I/O operation has been transferred. The data transferred might be the CCW address to be placed in CAW for the handling of the I/O operation by CE2.

Another example of communications between elements of a system, such as between CE and CE and IOCE is shown in flow diagram of Fig. 1-42. Note on this diagram a SCON instruction is issued to reconfigure the system being used. CE1 issues the instruction and the selected elements that receive the SCON are CE2 and IOCE1. After making initial checks CE1 places the configuration mask on the Control Bus and raises the Reconfiguration Select Lines to the elements selected (CE2 and IOCE). This control line informs the selected elements that the reconfiguration is on the Control Bus. The receiving elements check to see if the CE1 bit is set to a one in their respective CCR (Configuration Control Register). If it is set, they accept the data from the Control Bus and raise a Response Line back to the issuing CE1. If both accepted the configuration, the condition code in the issuing CE1 is set to a zero; if not, it is set to a two or one.

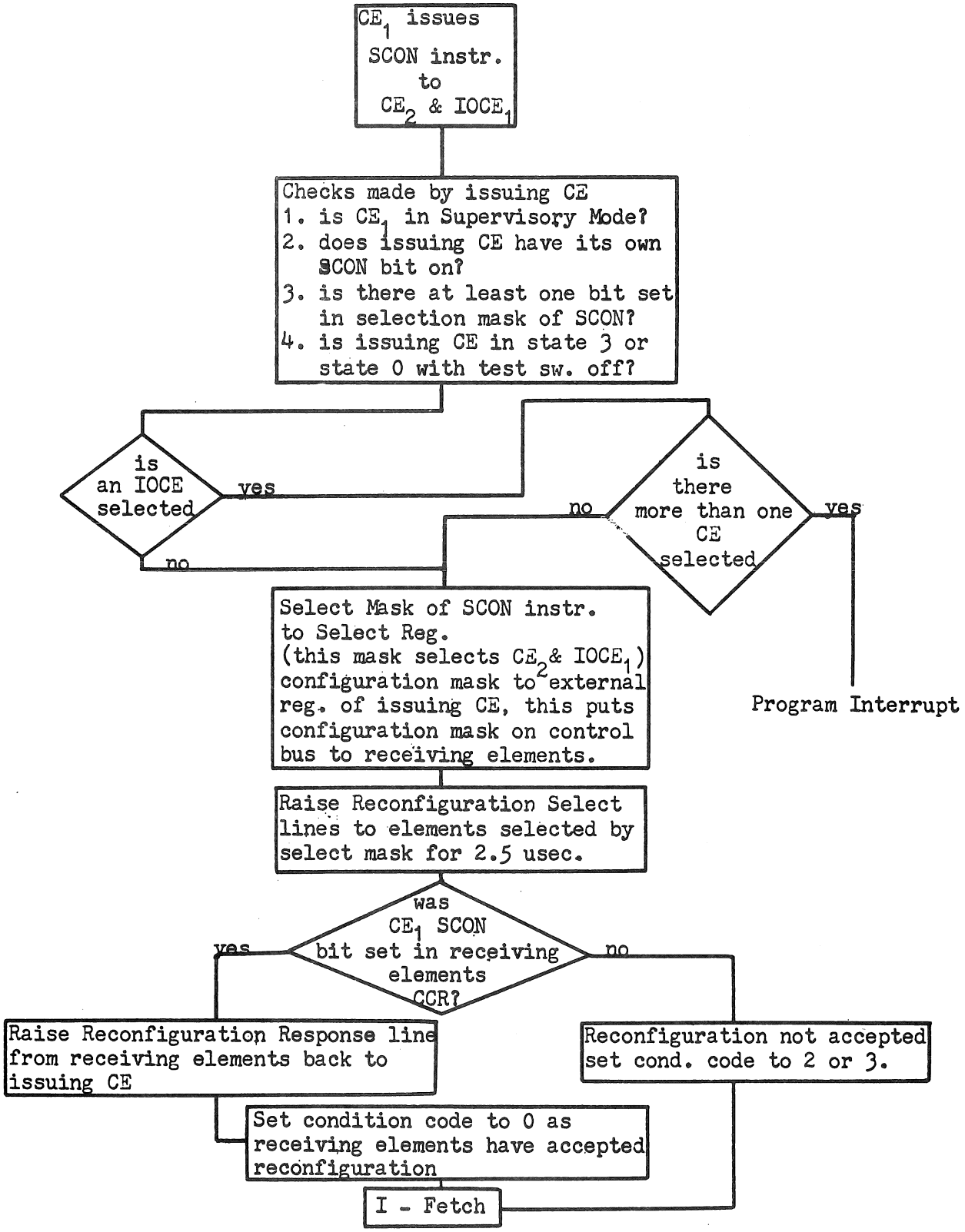


Figure 1-42. CE Issues SCON Instruction.

B. CE to SE Communication

In the normal execution of instructions of a program it is necessary for the CE to access storage for instructions and data. In making this access the following control lines between elements are used (refer to the flow diagram shown in Fig. 1-43). In this diagram the CE is accessing storage for data addressed in the instruction. The CE puts the address on the output bus to the SE and if the CE is configured to communicate with the SE, it raises Access Request control line to the SE. The SE checks to see if its configuration communication bit is set for the accessing CE and if it is, the SE raises a line called acknowledged back to the CE. The acknowledged line back to the CE causes it to wait for 25 msec. During this time the SE is resolving priority and raises Accept to the CE when it has resolved and accepted this CE. Upon reception of the Accept line the CE drops Access Request. The SE places the data on the bus obtained from storage and raises a Gate Data line back to the CE informing the CE its data is on Bus-In.

The examples given in the preceding discussion are not meant to be a complete discussion of all communications between elements, but are presented to give the reader insight as to how control lines are used to accomplish specific tasks necessary for the operation of the 9020 System.

1-7. IBM-9020 SYSTEM DOCUMENTATION

The documentation available for reference in the 9020 System can be separated into two general classifications:

1. Hardware Documentation
2. Operation and Software Documentation

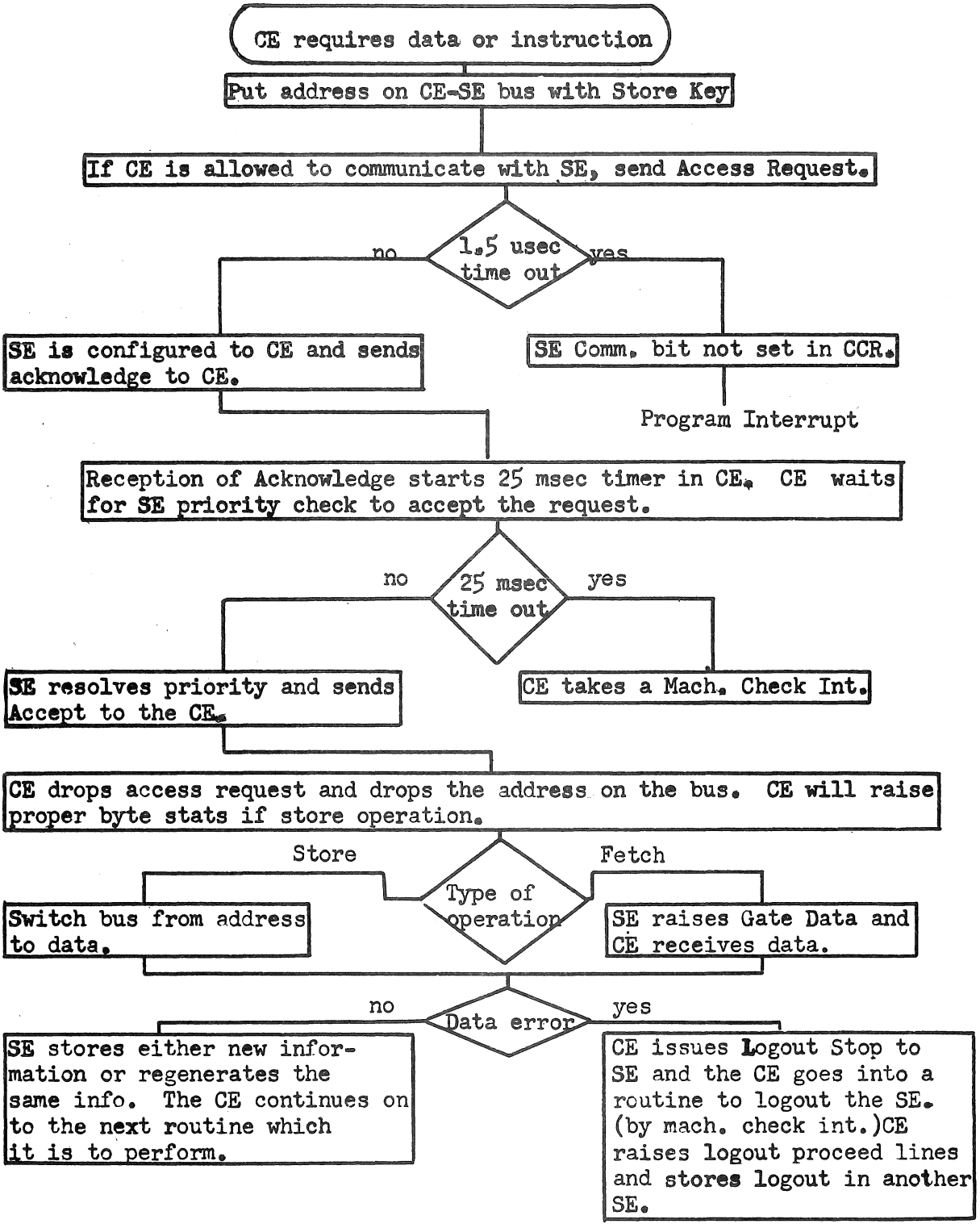


Figure 1-43. CE Accesses Main Storage.

A. Hardware Documentation

The types available for hardware information can be reviewed by referring to Fig. 1-44.

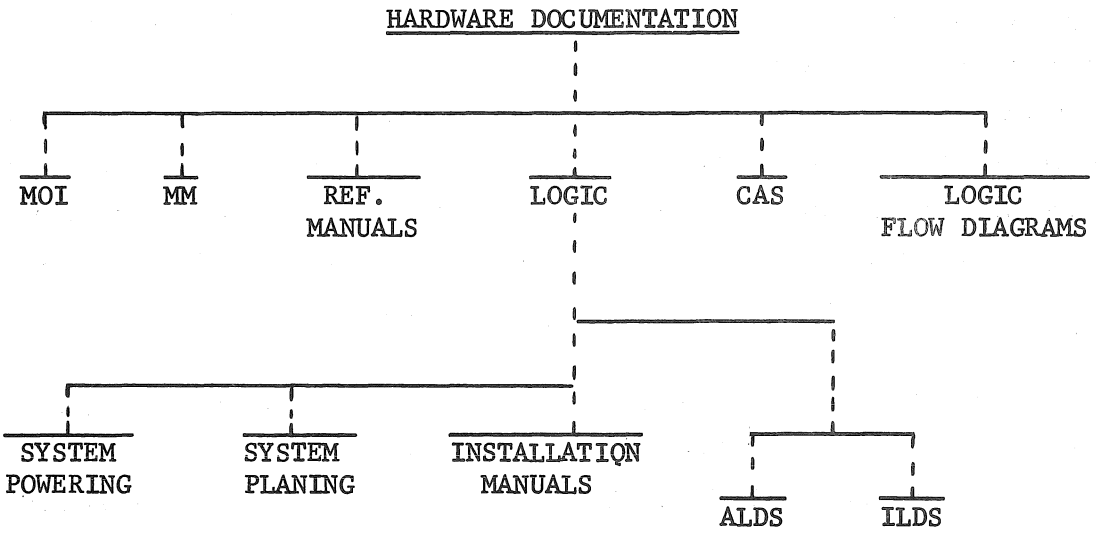


Figure 1-44. Hardware Documentation.

The Manual of Instructions (MOI) is published for every major element contained in the Computer Complex. These manuals consist of a narrative discussion of the general operation of the particular element. An example of this manual is the "IBM-9020 7201-01 Compute Element Instruction Manual".

The Maintenance Manuals (MM) generally contain the maintenance philosophy for the particular element. Included in this philosophy are error detection, malfunction recovery, reconfiguration, fault locating test, maintenance manual controls, preventive maintenance, service checks, etc. An example of this type of manual is the "IBM-9020 7201-01 Compute Element, 7231-02 I/O Control Element, Maintenance Manual".

The Reference Manuals (REF.) contain such information as System Powering, System Planning and Installation Data. An example of such a manual is the "IBM-9020 System Powering Manual".

The ALDS are automatic computer generated logic diagrams which describe the complete logical functions performed by the hardware of the particular element. There are approximately 20 volumes of the ALD type which describe the logical functions of the hardware for the Compute Element (7201). These volumes are stored on roll-around carts contained or the Computer Complex floor. Stored in the same manner are some 21 volumes of ALDS for the IOCE, 5 volumes for the SE, 5 volumes for the ICU, 5 volumes for the PAM, 1 volume for the Reader-Punch (RP), 2 volumes for the TCU, and 3 volumes for the SC.

The ILDS are intermediate logical diagrams which attempt to describe the logical operations in a simplified form. Thus, enabling one to obtain a general idea of the logical functions performed by a particular element.

The CAS (Control Automation System) are diagrams that document the micro-program routines. Each block on the CAS diagrams represents one microprogram word. The micro-orders that are specified by the word are shown in the CAS block. Each block represents one machine cycle. There exists on the Computer Complex floor CAS volumes which describe the internal microprogram of both the Compute Element and the I/O Compute Element.

Logic Flow diagrams are made available for practically all the major elements of the Computer Complex. These diagrams attempt to describe the overall operation of the particular element taking into account both the logical hard-ware functions and the microprogram control.

B. Operation and Software Documentation

The manuals available for operation and software description can be reviewed by referring to Fig. 1-45.

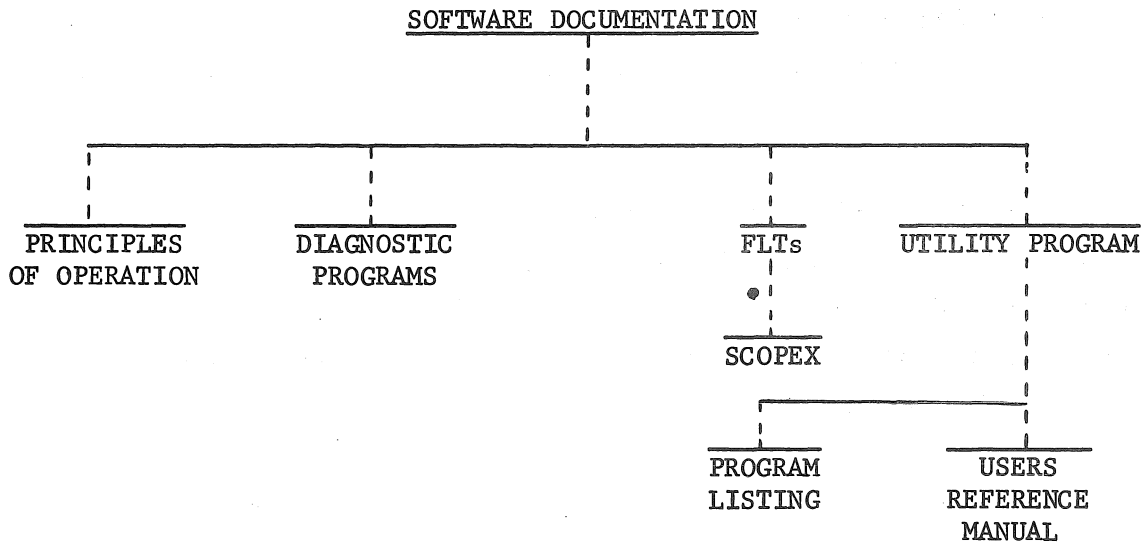


Figure 1-45. Software Documentation.

The Principles of Operation Manual contains essentially all the operational information that is needed from a programming standpoint. This manual contains definitions of the instruction set, masking for the interrupt scheme, masking for I/O operations, and a variety of operational subjects which are important for system operation.

Diagnostic Program Manual contains the diagnostic program writeups which are run to determine if the system will perform the instruction set. These programs are presented in "listing format". The programs include GO NO/GO, Small Storage Test, Subsystem Diagnostic Monitor (IDM), and Multi-Processing Diagnostic Monitor (MDM).

The Fault Locating Techniques Manual provides a description and operating procedure for each type of Fault Locating, or Fault Detecting category of tests used in the maintenance of the CE and IOCE of the 9020 System. Specifically, the manual includes a description of the utility program to maintain and update the test tapes, the purpose of the tests, the equipment required, the procedure for operating the tests, reference information, and preferred troubleshooting techniques. A companion to this manual are several SCOPEX volumes which are keyed to the addressed error stops that occur from running the FLTs.

The Utility Program Manual is a program which provides many functions related to the software operation of the IBM-9020 System. Examples of these functions are programs which enable one to edit tape, make program listings, etc. One volume contains the Utility Program Listing. There are several other manuals that describe the procedures used with the Utility Monitor.

C. Description of the Logic Contained in Documentation

The Solid-Logic Technology (SLT) and Standard Modular System (SMS) are the type of electronic circuitry used within the IBM-9020 System. The bulk of this circuitry is made up the SLT type. The following is a description of the logic documentation contained in the ALD volumes discussed previously.

1. SLT Logic Description

The Solid-Logic Technology (SLT) used in the CE consists of a coordinated family of miniaturized basic circuits and complete packaging techniques optimized for use in electronic computing equipment. The three basic SLT building blocks are modules, cards, and boards. A module, which is generally a complete logic circuit, is an integrated component-package device with advanced performance, reliability, and environmental operating characteristics. Modules are mounted on printed circuit cards in groups of 6, 12, or 24. These cards, in turn, are plugged onto a printed circuit board.

Basically, SLT utilizes screened-film linear components and silicon semiconductors integrated on a ceramic substrate. These assemblies are the functional building blocks.

The basic circuits used are diode-transistor (NAND) logic with an average operating time of 30 ns per decision. The choice of the NAND circuit configuration provides circuit simplicity, transistor drive currents which are independent of the input signals, and large, well-controlled noise thresholds. The basic circuits require only three basic components: diodes, transistors, and resistors (capacitors and inductors are used to meet special requirements). They are designed to operate properly with all components at their end-of-life value in the direction most detrimental to operation. Three supply voltages (+6v, +3v, and -3v) are used to reduce the dependence of circuit speed on semiconductor characteristics and provide a very narrow range of delay variation from circuit to circuit.

Modules are normally mounted on glass epoxy printed circuit cards with conductors on both sides. Three types of SLT cards are used: the 6-module card, the 12-module card, and the 24-module card.

The card is provided with a connector having beryllium copper contacts and welded gold contact points. There are 24 contacts on the 6- or 12-module cards and 48 contacts on the 24-module cards. The connector is keyed to prevent insertion in the wrong orientation.

Printed circuit cards are, in turn, plugged onto a multilayer glass epoxy printed circuit board. This board has four conductor layers: the two outside layers are used for signals; the two inside, for power distribution and signal returns. Pins are soldered into plated-through holes on the board to provide contacts to mate to the card connector. Eighty-two 24-contact card positions are provided on the board which can be used to mount cards or interboard conductors. Additional plated through holes are provided for interconnection between conductor layers.

Figure 1-46 is an example of the SLT Module construction.

Figure 1-47 is an example of the module assembly to form the 3 types of cards used in the 9020 System.

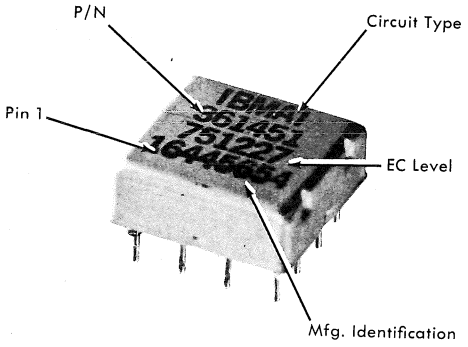


Figure 1-46. Typical SLT Module Before and After Encapsulation.

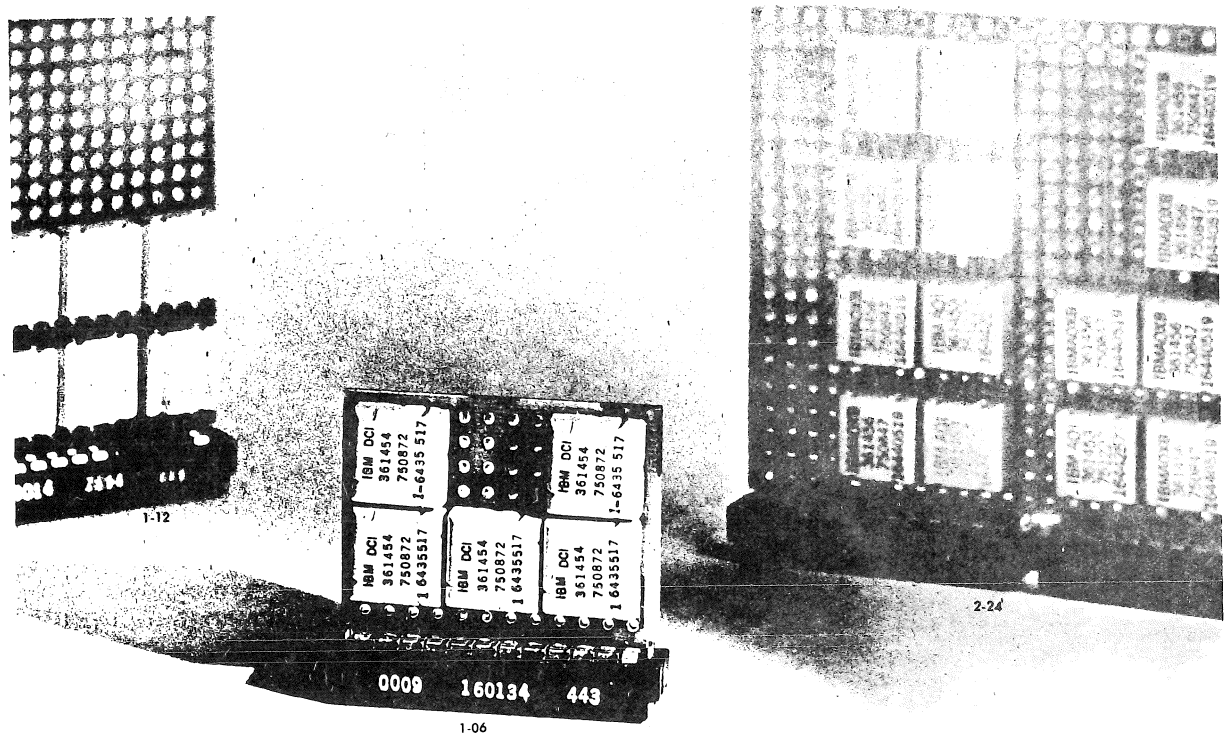


Figure 1-47. IBM-9020 SLT Card Types.

It is visualized that in the maintenance of the 9020 System, repairs should not be attempted on the cards at the field locations due to the specialized procedures and test equipment required.

The boards are arranged on the gates according to the functions which are to be performed or according to the applicable functional unit. The frame-gate locations and gate-board locations as well as the board function usage are shown on Figs. 1-48 through 1-50.

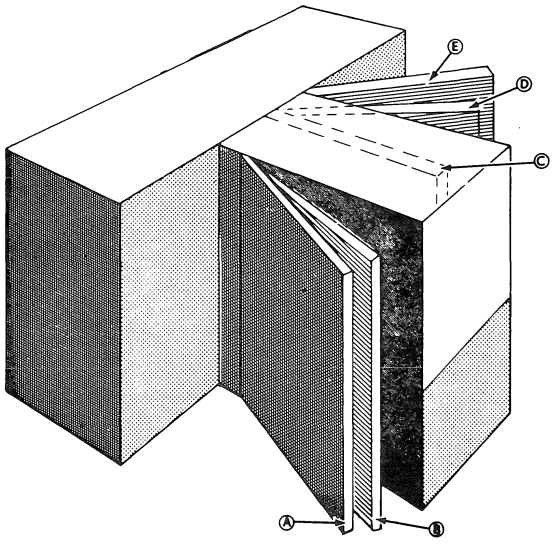


Figure 1-48. Frame - Gate Location.

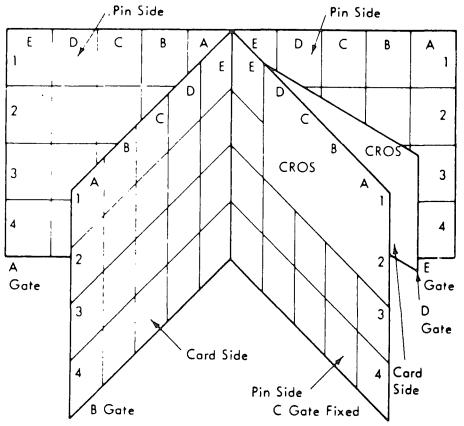
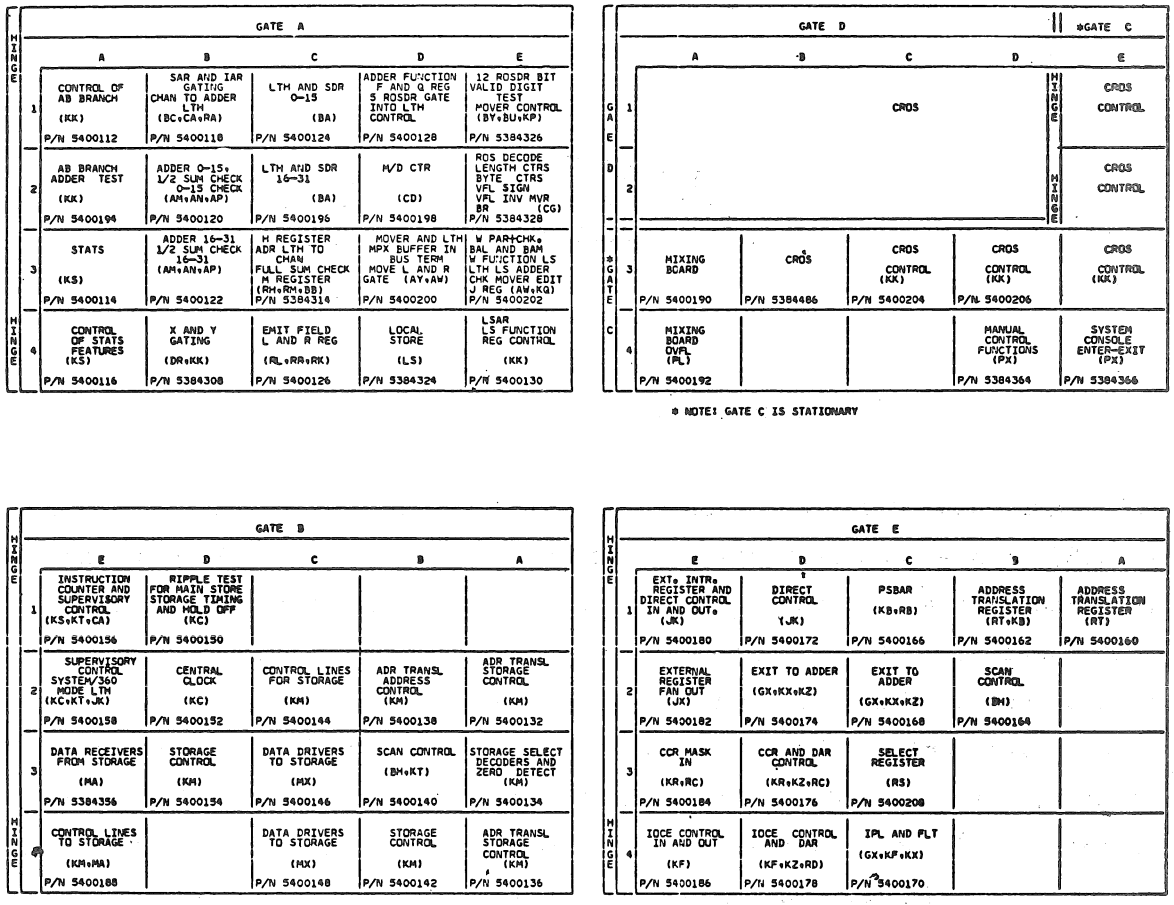


Figure 1-49. Gate - Board Location.

SYSTEM 9020 COMPUTING ELEMENT GATES A, B, C, D, E—BOARD LAYOUT



GATE A

HINGE	A	B	C	D	E
1	CONTROL OF AB BRANCH (KK) P/N 5400112	SAR AND IAR GATING CHAN TO ADDER LTH (BC,CA,RA) P/N 5400110	LTH AND SDR 0-15 (BA) P/N 5400124	ADDER FUNCTION F AND Q REG S ROSDR GATE INTO LTH CONTROL P/N 5400128	12 ROSDR BIT VALID DIGIT TEST MOVER CONTROL (BY,BU,KP) P/N 5384326
2	AB BRANCH ADDER TEST (KK) P/N 5400194	ADDER 0-15, 1/2 SUM CHECK 0-15 CHECK (AM,AN,AP) P/N 5400120	LTH AND SDR 16-31 (BA) P/N 5400196	M/D CTR (CD) P/N 5400198	ROS DECODE LENGTH CTRS BYTE CTRS VFL SIGN VFL INV MVR BR (CG) P/N 5384328
3	STATS (KS) P/N 5400114	ADDER 16-31 1/2 SUM CHECK 16-31 (AM,AN,AP) P/N 5400122	M REGISTER ADR LTH TO CHAN FULL SUM CHECK M REGISTER (RM,RM,BB) P/N 5384314	MOVER AND LTH MPX BUFFER IN BUS TERM MOVE L AND R GATE (AY,AW) P/N 5400200	W PAR+CHK, BAL AND BAM W FUCTION LS LTH LS ADDER CHK MOVER EDIT J REG (AW,KQ) P/N 5400202
4	CONTROL OF STATS FEATURES (KS) P/N 5400116	X AND Y GATING (DR,KK) P/N 5384308	EMIT FIELD L AND R REG (RL,RR,RK) P/N 5400126	LOCAL STORE (LS) P/N 5384324	LSAR LS FUNCTION REG CONTROL (KK) P/N 5400130

GATE D | *GATE C

GATE	HINGE	A	B	C	D	E
D	1	CROS				CROS CONTROL
D	2					CROS CONTROL
*C	3	MIXING BOARD P/N 5400190	CROS P/N 5384486	CROS CONTROL (KK) P/N 5400204	CROS CONTROL (KK) P/N 5400206	CROS CONTROL (KK)
*C	4	MIXING BOARD OVFL (PL) P/N 5400192			MANUAL CONTROL FUNCTIONS (PX) P/N 5384364	SYSTEM CONSOLE ENTER-EXIT (PX) P/N 5384366

* NOTE: GATE C IS STATIONARY

GATE B

HINGE	E	D	C	B	A
1	INSTRUCTION COUNTER AND SUPERVISORY CONTROL (KS,KT,CA) P/N 5400156	RIPPLE TEST FOR MAIN STORE STORAGE TIMING AND HOLD OFF (KC) P/N 5400150			
2	SUPERVISORY CONTROL SYSTEM/360 MODE LTH (KC,KT,JK) P/N 5400158	CENTRAL CLOCK (KC) P/N 5400152	CONTROL LINES FOR STORAGE (KM) P/N 5400144	ADR TRANSL ADDRESS CONTROL (KM) P/N 5400138	ADR TRANSL STORAGE CONTROL (KM) P/N 5400132
3	DATA RECEIVERS FROM STORAGE (MA) P/N 5384356	STORAGE CONTROL (KM) P/N 5400154	DATA DRIVERS TO STORAGE (MX) P/N 5400146	SCAN CONTROL (BM,KT) P/N 5400140	STORAGE SELECT DECODERS AND ZERO DETECT (KM) P/N 5400134
4	CONTROL LINES TO STORAGE (KM,MA) P/N 5400188		DATA DRIVERS TO STORAGE (MX) P/N 5400148	STORAGE CONTROL (KM) P/N 5400142	ADR TRANSL STORAGE CONTROL (KM) P/N 5400136

GATE E

HINGE	E	D	C	B	A
1	EXT. INTR. REGISTER AND DIRECT CONTROL IN AND OUT (JK) P/N 5400180	DIRECT CONTROL (JK) P/N 5400172	PSBAR (KB,RB) P/N 5400166	ADDRESS TRANSLATION REGISTER (RT,KB) P/N 5400162	ADDRESS TRANSLATION REGISTER (RT) P/N 5400160
2	EXTERNAL REGISTER FAN OUT (JX) P/N 5400182	EXIT TO ADDER (GX,KX,KZ) P/N 5400174	EXIT TO ADDER (GX,KX,KZ) P/N 5400168	SCAN CONTROL (BM) P/N 5400164	
3	CCR MASK IN (KR,RC) P/N 5400184	CCR AND DAR CONTROL (KR,KZ,RC) P/N 5400176	SELECT REGISTER (RS) P/N 5400208		
4	IOCE CONTROL IN AND OUT (KF) P/N 5400186	IOCE CONTROL AND DAR (KF,KZ,RD) P/N 5400178	IPL AND PLT (GX,KP,KX) P/N 5400170		

Figure 1-50. Board Location.

As previously mentioned, the SLT cards plug directly into a board. These boards are made of epoxy glass laminated to provide four conducting planes. These conducting planes are used to carry signals, voltages, and ground to the logic cards, crossover connectors, and cable connectors. Figure 1-51 is a cross section view of an SLT board.

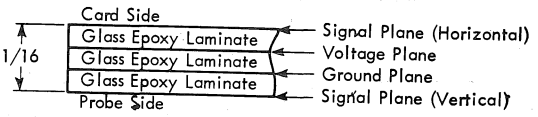


Figure 1-51. Board Cross Section.

Holes are located at the intersection of vertical and horizontal lines making a 0.125 inch ± .002 inch grid on the board. There are 6,370 holes arranged in 65 columns and 98 rows, each of the holes is copper plated to permit circuit connections from plane to plane. The plane conductor patterns are brought to the edge of the hole when a hole is used to complete an interplane connection. Pins, which make the connection to a card, cable, or crossover connector contact, are inserted into some of the holes. On the probe side (side opposite to the cards) the pins are used as terminals for discrete wires when wire routings are difficult or impossible to route by the Design Automation Program. Also, pins are used for wiring of field repairs and engineering changes.

Board logic wiring is programmed by computer. A maximum of three printed conductors 0.010 inches wide on 0.020 inch centers may be located between any two columns or rows. All conductors on one plane run in the same direction. The conductors run horizontally on the card side outer plane and vertically on the probe side plane. Noise coupling on the signal lines is reduced by running these conductors parallel to the voltage lines; noise coupling on the probe side is reduced by the close proximity to the ground plane.

Only standard SLT supply voltages are carried by the inner planes. These are +3, +6, and -3. If special voltages are required, they are distributed by one of the following methods:

1. Printed pattern on signal plane.
2. Discrete wires on the probe side of the board.
3. Minature laminar bus connection to pins on the probe side of the board.
4. Special internal pattern.

Each gate on the IBM-9020 System is a double frame; one of these is used to hold the boards and the other to provide channels for the flat interconnecting cables. On the card side, the gate is made of pressed or molded channels. These channels are notched opposite the card rows so a cable can leave the channel and connect to a board. This notching also allows the installation of cable retainers. Cooling air enters the gate at the bottom. An air seal around the card side of a board is made by foam lined covers which force the air up past the cards and out the top of the gate.

Board locations within a gate are identified by an alphabetic character that specifies a column and a number that specifies a row. The numbering sequence is left to right and top to bottom when looking at the card side of the gate. The numbering sequence is the same regardless of how the gate is oriented with respect to the machine unit. A swinging gate may be hinged from either end with the card side facing either way, but the numbering sequence is still left to right, top to bottom as viewed from the card side.

The logic gates are hinged to frame 01 on the 7201 Compute Element. Frame 02 contains the inverter/converter, low voltage power supplies and other powering circuits. The layout of this frame is shown on the line drawings Figs. 1-52 and 1-53. Functionally, the converter takes the incoming 60 cycle power and rectifies it using a full wave bridge. The rectified output of the converter is filtered to within 3% ripple (the nominal dc output is 276 v.) and fed to

the inverter. The inverter with its silicon controlled rectifiers and 2.5 kc oscillator invert the filtered 60 cycle power to a 2.5 kc square wave with a peak to peak amplitude of 276 volts. This square wave is passed through a sine wave filter and results in a 2.5 kc sine wave output with an amplitude of 100 volts RMS. This voltage is fed to the low voltage power supplies where it is converted to the logic voltages used throughout the element.

While it is not visualized that the Systems Engineer will be required to perform actual repairs on the 9020 Computer, it may be necessary from time to time for him to verify certain facts in the systems wiring diagrams. For this reason a brief discussion on the various logic blocks found in the Automated Logic Diagrams (ALD) and a sample ALD with appropriate notations are included in this area. Since ALD type documentation is oriented to a specific machine, the examples presented in this area will not have any meaning as far as the machine is concerned. Rather, the examples will include most every circumstance encountered in ALD type analysis.

On an ALD, circuits are represented by rectangular blocks which symbolize logical functions. The blocks are connected by printed lines which symbolize electrical connections. Inputs enter the circuits on the left; outputs leave at the right. Most of the page is used for the representation of logic; page identification and supplemental information appear at the bottom of the sheet.

The page number is located in three places on the sheet. The page number in Fig. 1-67 is KH142. In this illustration the page number is in the upper right-hand corner, as well as in both the lower right and the lower left corners.

Logic pages are numbered according to a coded prefix consisting of two alphabetic letters, representing the major and the minor characters. The general scheme of the coding is shown in Fig. 1-55.

CE POWER FRAME

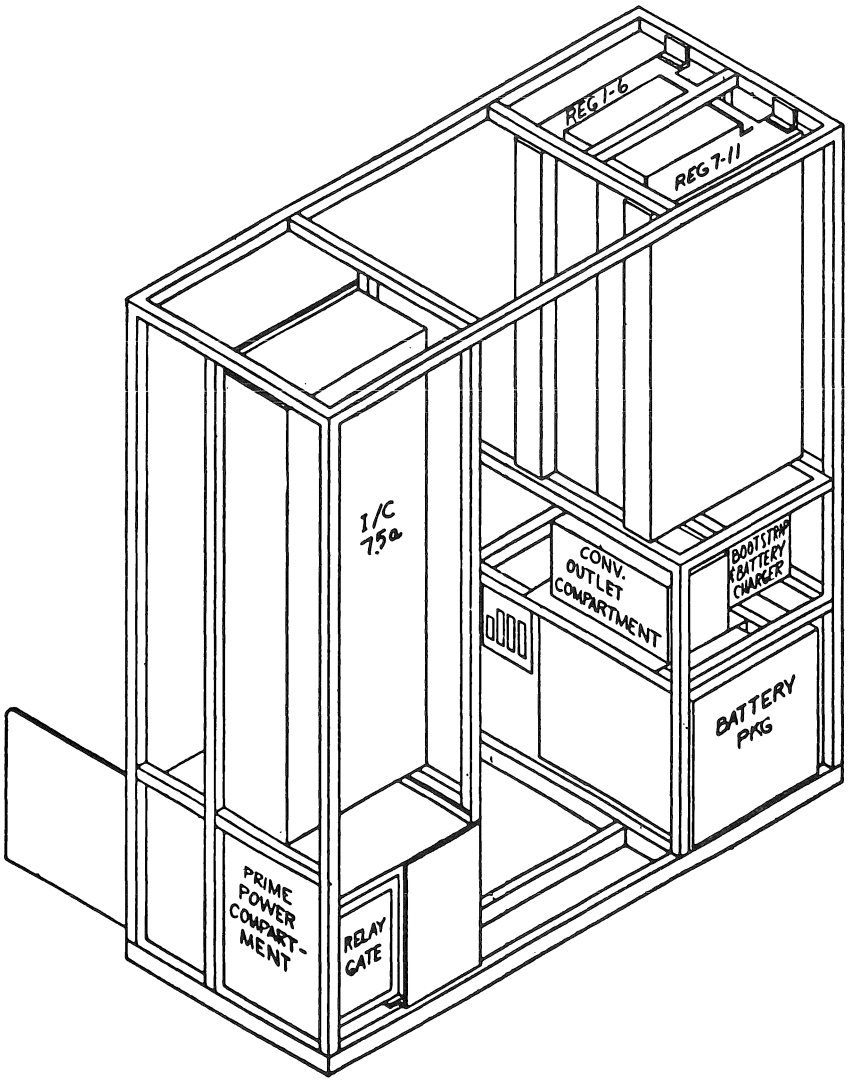


Figure 1-52. CE Power Frame.

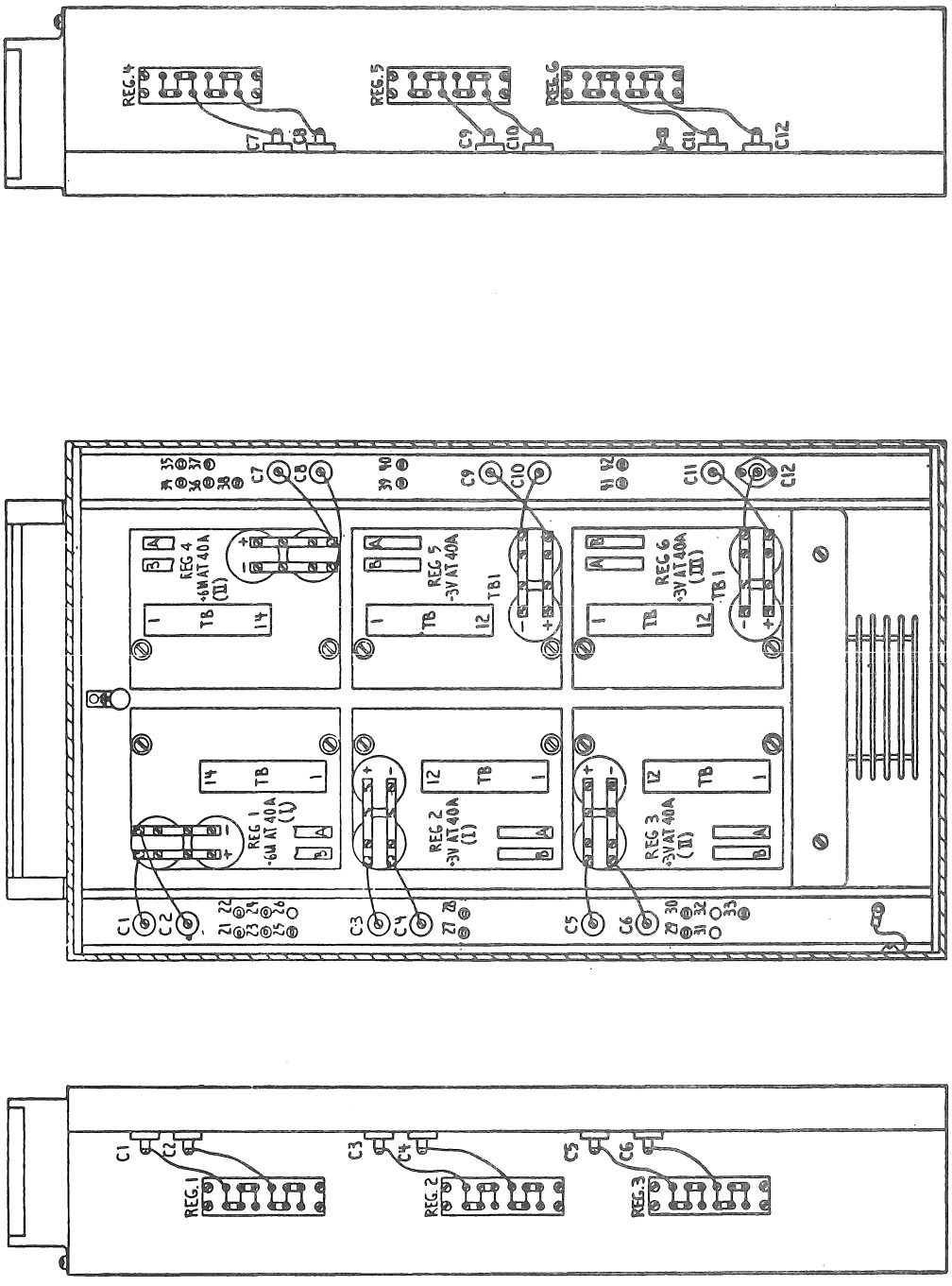


Figure 1-53. Power Supply and Regulator 1-6 Layout.

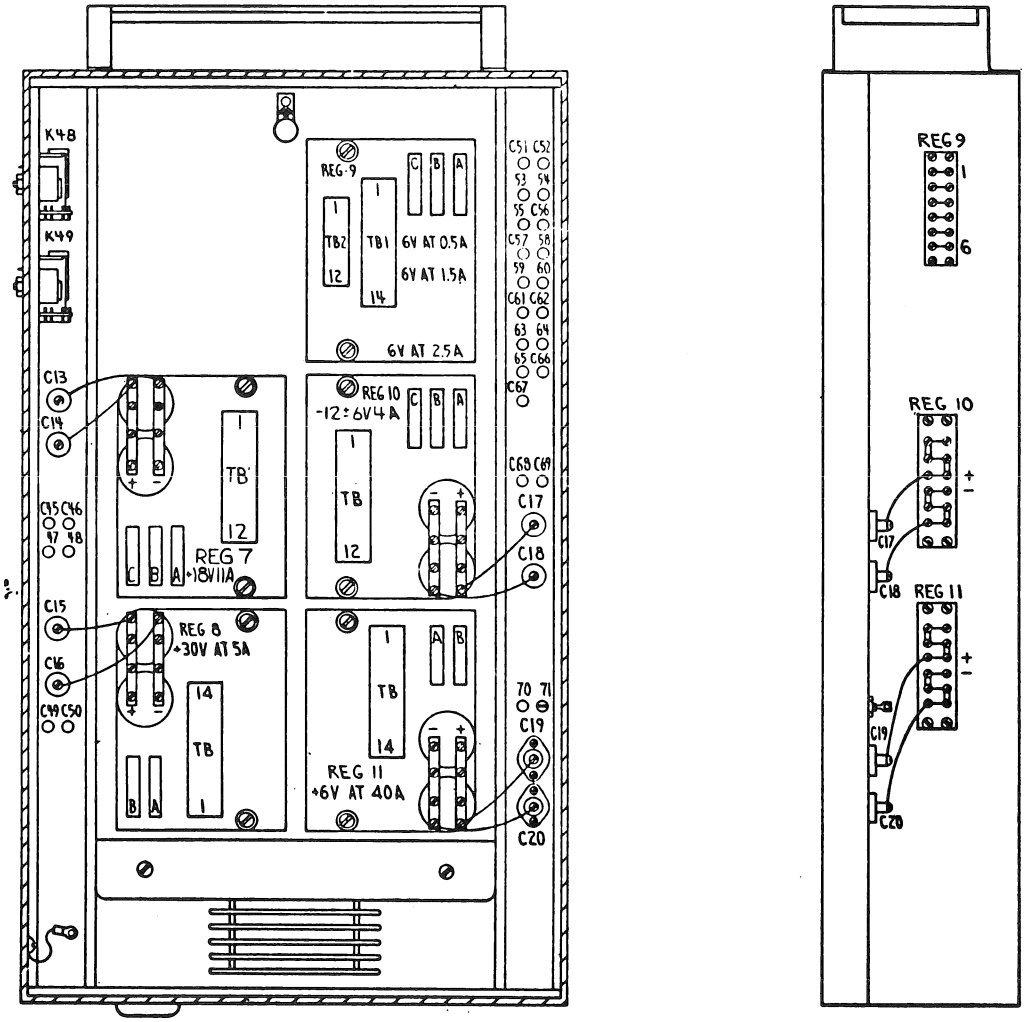


Figure 1-54. Power Supply and Regulator 7-11 Layout.

For example, the coding for the A Register is RA. "R" is the major character; it means register "A" is the minor character, designating the particular register. Another example is KR101, which means control (K), check triggers (R), Page 101.

The general scheme as shown in Fig. 1-55 is utilized to some extent in the IBM-9020 processor; however, some variations are evident in the practical case.

A version page shows wiring and cards that are not on the basic machine. This wiring must be added to that used by the basic machine. This is in direct contrast to the additive card code, in which the wiring is part of the basic machine, and only cards are added to make the feature operative. An example of a version page is those pages that added the cards and wiring for floating point.

A version page is made up of all basic page blocks which are unchanged in the version design plus additional blocks (version blocks) needed to change the basic page into a version page. A version number is printed at the top of each version block to differentiate it from a basic block.

The machine version number appears below the page number; for a basic (standard) machine this number is 000. A version page assigned by Design Automation has a number other than 000.

I.	Adders	
	1. Addressing Adder	AA-AB
	2. IC Incrementer	AC-AD
	3. Exponent Adder	AE-AF
	4. Main Adder	AM-AQ
	5. Serial Adder	AS
	6. VFL and DEC Adder	AV-AW
II.	Decoders	
	1. Op Decoders	DN
	2. FLP and Gen. Decoder	DP
	3. Addressing and Pre FTH	DA
	4. Trap Decode	DB
	5. Reg Decode	DG
	6. ROM Decode	DR-DS
III.	Counters	
	1. Instruction Ctrs	CA-CB
	2. Local Store Address Ctr	CC-CD
	3. Misc. Ctr	CE-CZ
IV.	Busing (Excluding Memory Bus)	BA-BZ
V.	Registers	
	1. A Reg	RA
	2. B Reg (BOP REG, Mod 70)	RB
	3. D Reg	RD
	4. E Reg (PSW for Mod 70)	RE
	5. F Reg (I/O Reg, Mod 70)	RF
	6. G Reg (Gen Purpose, Mod 70)	RG
	7. H Reg	RH
	8. J Reg	RJ
	9. K Reg	RK
	10. L Reg	RL
	11. M Reg	RM
	12. N Reg (Op Code Reg, Mod 70)	RN
	13. P Reg (FLT Pt Reg, Mod 70)	RP
	14. Q Reg (FLT Pt Reg, Mod 70)	RQ
	15. R Reg (Reg Bus Latch, Mod 70)	RR
	16. S Reg (Shift Ctr & Exp in, Mod 70)	RS
	17. T Reg	RT
	18. U Reg	RU
	19. V Reg	RV
	20. W Reg	RW
	21. X Reg	RX
	22. VFL and Decoder Reg, Mod 70	RY
	23. Direct Data Reg	RZ
VI.	Main Storage Registers and Controls in CPU (Includes SDR Registers, Storage Buses, SAR, SBI "OR", M and N Regs in Mod 30)	MA-MC
VII.	Controls	
	1. Advance or Seq Cntls	KA
	2. Branch and IC Cntls	KB
	3. Clock Cntls	KC
	4. I Exec (Mod 70) I Fetch & Exec (Mod 60)	KD
	5. Chan Cntrls	KE
	6. Fix Seq Cntls	KF
	7. Gen Reg Cntls	KG
	8. FLT Cntls	KH
	9. ROS Cntls	KK
	10. Local Store Cntls	KL
	11. Priority and Interrupt Cntls	KM
	12. I/O Instr Cntls	KN
	13. VFL Cntls	KP
	14. VFL Cntls	KQ
	15. Check Triggers	KR
	16. Status Triggers	KS
	17. VFL Cntls & Decimal Cntls	KY
	18. Any Misc. Cntls such as FP	KT-KU
	19. Fixed Pt, Storage Protect, Real Time clk, Status Cntls	KW-KZ
VIII.	Consoles	PA-PE,PJ-PZ
	1052 Console Adapter	PF,PG,PH
IX.	Local Store	LS-LT
X.	TROS	EA-EC
XI.	CROS	ED-EF
XII.	Spec. Features	XA-XZ
XIII.	Hardware Oriented Pages	ZA-ZZ
XIV.	I/O Channels	
	Multiplex Channel	FA-FZ
	Selector Channel #1	GA-GZ
	Selector Channel #2	HA-HZ
	Direct Data	JA-JZ
XV.	ROS Flow charts	QA-QZ
XVI.	Power Supplies	YA-YZ

Figure 1-55. Definitions of Page Number Prefixes.

The title block is printed in the lower right corner of the page. As Fig. 1-56 shows, information can be found at three places in the block:

1. At the Top
   a. The Page Title ("LS Address Register J Bits 0 through 3" in Fig. 1-56)
2. On the Left Side
   a. Date of Processing by Design Automation (05-12-64)
   b. Log Number (or Computer Run), "074A", assigned by design automation
   c. The Corporate Division, WTC (World Trade Corporation)
3. On the Right Side
   a. Machine Type, "2040". This may be a pseudo number or it may be the machine number followed by a suffix. The suffix differentiates between models or features of the machine number.
   b. Frame "01"; within the machine, may be 01 to 63.
   c. Part number of the page "5348221"
   d. Block DF is, in terms of design automation, the next available block serial number available for use on that page.

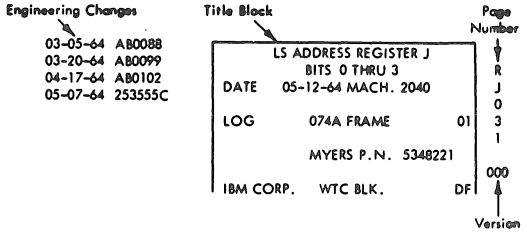


Figure 1-56. Example of Title Block, Page Number and Version, and Engineering Changes.

Logic blocks shown in Fig. 1-67 are positioned on the page in a matrix seven columns wide and 13 rows high. The columns are numbered 1-7. Rows are lettered A-N, excluding I.

A logic block is six increments wide by seven increments high; it may be lengthened downward to a maximum of 24 increments. The block may have one to seven input and/or output lines on the basic block; one to 24 input and/or one to 10 output lines on the extended block.

a. Information Inside the Logic Block

LINE 1

The logical function being performed by the circuit represented appears on Line 1; for example, A, OR, N, FF, etc. An asterisk (*) preceding the logical function symbol means to design automation that the input line positions are placed in a certain arrangement.

The suffix, preceded by a space and following the function, is additional information describing the function. The suffix is used to indicate DOT functions such as A OR, OR A, N OR, OR WL; to indicate the blocks in a multi-block configuration of bi-stable circuits such as A FF, OR FF, A PH, OR PH, N PH; and to indicate additional information in special component blocks such as RY CT, RY P, A LT.

An asterisk (*) following the suffix and/or in position six indicates a special block that does not follow the rules of design automation. Some of the special blocks are exit and entry, service-voltage logic, switch, and jack blocks, as well as discrete components such as capacitors, resistors, etc.

LINE 2

The additive card code (special machine feature) appears here in the first four characters, for example, 7TR (seven-track tape feature). Additive card codes identify those logic blocks which pertain to a special class of machine features in which the feature can be installed by plugging in the feature cards.

The last two characters of Line 2 contain the symbolic package designation. The use of these two characters allows design automation to generate the ALDs, to position the card on the board, and to generate the wiring (printed or discrete) on the board. Blocks with the same characters in the symbolic package field will be placed on the same board by the card partitioning program used by design automation.

NOTE: Blocks with different symbolic packages may be packaged on the same board.

LINE 3

The circuit number (Fig. 1-57) appears on Line 3 except when design automation generates a pseudo block for a DOT function. In this case DOT appears on line three. A DOT block is a tie point for the output of two or more circuits feeding one circuit.

The circuit number is the coded name given to a particular circuit. (See Fig. 1-58)

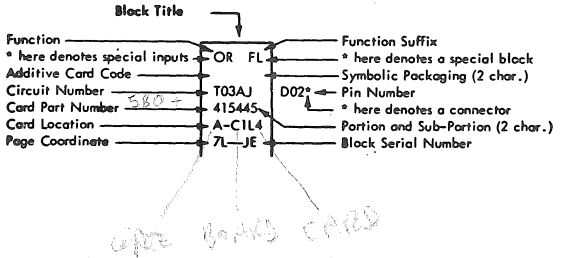


Figure 1-57. The ALD Logic Block.

Block Titles in DFD-53 P page 5-12

SRETL - Screened Resistor Etched Transistor Logic

Logic General Form - XYYZZ

X Defined

S - SRETL General
T - 30 ns
U - 5-10 ns
V - 700 ns
O - Analog

YY Defined

03 - Logic Blocks
05 - Voltage Translate Circuits
06 - Transmission Line Drivers and Receivers
07 - Sense Amplifiers
10 - Inverting Drivers less than 50 ma
11 - Non-Invert Driver less than 50 ma
15 - Power Driver more than 50 ma
16 - Magnetic Head and Core Driver
20 - Triggers
21 - Singleshots
22 - Oscillators
25 - Regulators, Clamps, Clippers, and Limiters
32 - Gates
40 - Specials
45 - Delay Circuits
55 - Indicator Circuits
60 - Integrators and Filters
61 - Components
63 - Reed Relays
65 - Functional Card
66 - Field Replacement Card

ZZ Defined - The Unique Card

Figure 1-58. Circuit Number Code.

LINE 4

The last four digits of the card part number appear here. The first three numbers, 580, are the same for all cards and are not recorded.

The last two characters on Line 4 represent the portion and sub-portion. A portion represents an independent section of a card. A section may be represented by one or more logic blocks, each of which has a sub-portion number. The portion character is of the form A, B, ... Z, excluding I, O, and R. ALD blocks which are interconnected on a card are in the same portion. Every block in a portion has a unique sub-portion number. These sub-portion numbers are assigned in the sequence 1, 2, ... 9, A, B, ... Z (excluding I, O, and R).

EXCEPTION: When a circuit with an unloaded collector and an associated load resistor packaged on the same card are used together, the block designating the load resistor has the same portion as the unloaded circuit, and the sub-portion character is R.

LINE 5

The card location is placed at Line 5 as follows:

1. Character one is the gate (A-Z) followed by a dash.
2. Characters three and four are the board location, one alphabetic and one numeric.
3. Characters five and six are the card location, one alphabetic and one numeric.

LINE 6

The print location in positions 1 and 2 of Line 6 are the grid co-ordinates of the block on the ALD page, for example, 1B, 3F. The serial number of the logic block appears in positions 5 and 6, and is expressed in alphabetic characters. Serial numbers begin with AA and proceed in a sequential order (AA, AB, AC, ... ZZ). Serial numbers AA through RZ refer to the basic system group, and numbers SA through ZZ, to the special engineering group.

An Engineering Change (EC) may add logic blocks in which case the sequence of double alphabetic characters would be continued. An EC may move a block to another print location, but the serial number for that block will stay the same. If an EC eliminates a block, that serial number will not appear again on that page. The block serial number is an integral part of the net number. (See the "Glossary".)

b. Information Outside the Block

Title and Version Number

When logic blocks have been assigned a title, the title appears over the block. The version number appears in the title area for all version blocks.

Pin Numbers

Pin numbers are in line with the input or output line. They are the actual numbers of the base pins of the card.

Asterisk (*) On an Input or Output Line

An asterisk (*) on an input or output line denotes a connection that leaves the board. The routing is found at the bottom of the ALD page, keyed with the serial number of the block and the output line number, e.g., AQ4.

c. Information on the Side of the Block

Wedges

The wedge (◺) is a small triangle at the point where a signal line joins a logic block. The wedge indicates that the active state of this line (the state which satisfies the function of the block to produce an output line of the state indicated) is at the least positive potential with respect to the most positive potential shown by the signal line without a wedge.

A wedge is placed in the edge of the block on an input or output line. When the block or circuit is performing its function, the wedge indicates the most negative (least positive) DC voltage that will be found on the line.

NOTE: Signal lines are operated at one of two voltages, an up level and a down level. Because SLT circuits operate at different speeds and at different pulse levels (0.0v to +12.0v; +0.9v to 3.0v, etc.), the line level designated by the wedge must be described as the most negative

(least positive); the absence of the wedge is the most positive (least negative) level of the line.

E in the Side (Figure 1-59)

An E is placed in the side of the block whose inputs are being extended. An example is a circuit that is used to add inputs to another AND or OR circuit; the connection from this second circuit to the first is made at other than a normal input or output of the first circuit. A connection of this kind is shown without polarity and is labeled E (for extender).

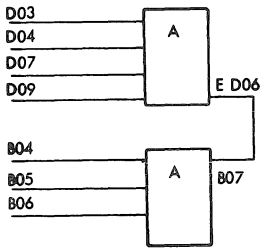


Figure 1-59. Extended Logic Block.

K in the Side (Figure 1-60)

Non-logical outputs of different blocks are not tied together by DOT blocks. Instead, a K is put in the edge of the block in line with each (except one) of the outputs connected together. The one exception is the output used to determine the net number.

Output (or input) lines on the same block may be tied together. In this case the net number will be the position without the K in the edge of the block.

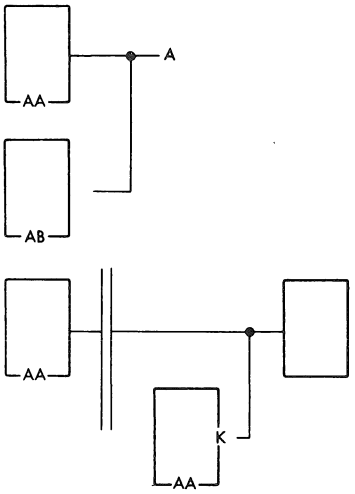


Figure 1-60. Non-Logic Designation (Output).

Nonlogical outputs on different blocks may be tied together when:

1. All the outputs tied together appear on the same page. The net number then includes the line origin of one of the outputs from one block. The commoned outputs are differentiated from the source by a K in the edge of the box position.

2. All of the outputs tied together are not on the same page. In a situation of this kind the outputs tied together on one page show an output to the right side of that page. The outputs in the same net on other pages return to the left of their respective pages and are referenced to the first page in the normal manner. The net number includes the line origin of one of the commoned outputs of the first page. In the edge of all the other blocks having outputs in the same net, a K appears in line with each commoned output.

P or N in the Side (Figure 1-61)

When a capacitive input to a block is designated, a P or N in the side of the block indicates the polarity of the shift necessary to satisfy the function of the block.

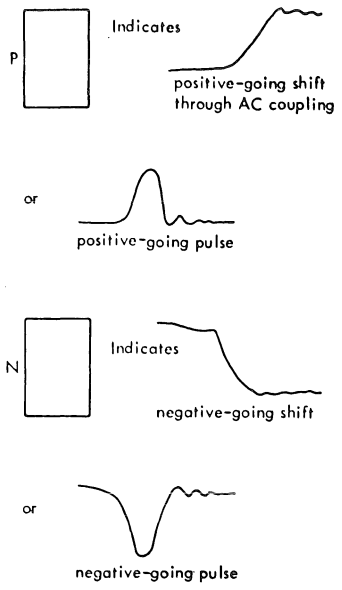


Figure 1-61. Capacitive Input Logic Block.

X in the Side (Figure 1-62)

Non-logic connections to a logic block have an X in the side at the place where the polarity indicator (wedge) is normally placed. This non-logic input or output can be a bias line. In the accompanying illustration D06x is a non-logic connection to the two-way OR block.

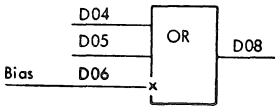


Figure 1-62. Non-Logic Designation (Input).

The following example shows the use of the X in the edge of the block. There is an X on the lines labeled D05 and J13, showing that that these lines are the same. (It is really one ground line that is common to several blocks and completes the ground circuit in these blocks.) At location 1L, lines D13 and G13 are similar to lines D05 and J13 except that there is a K at G13 because a net may have only one source. (Other input lines to a net are designed with the K.)

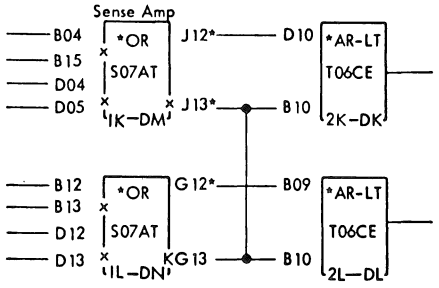


Figure 1-63. Multiple Block Logic.

d. Line Names

Input Line

Each input line (Fig. 1-67) entering an ALD page has a net number and a line name.

The net number is composed of the source page, the serial number of the source block, and the line origin of the source block. For example, KH141BD4 means that this line came from page KH141, from the block whose serial number at BD on that page, and from the fourth line position on the block. When an input line comes from more than one particular unit, such as one of many types of I/O units, or from more than one memory, a pseudo-net number will be put on the ALD net number position. These pseudo-net numbers will generally be in sequence on a page starting at 000.

A net is a set of signal points (a source and sinks) which are electrically interconnected. Generally the source point refers to the output pin of the driving block, and the sink points refer to the input pins at the driven blocks. The net identification is used to indicate which points (pins) belong to a given network.

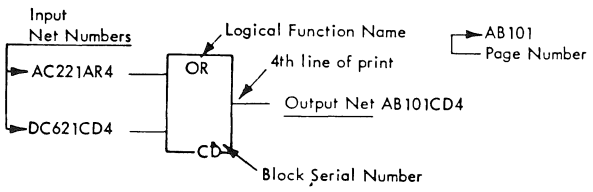


Figure 1-64. Circuit Description.

The line name is generally a description of the line function and is signed plus (+) or minus (-), depending upon the active condition of the line at that point. If most of the lines in the box are plus (+), the sign may not appear unless it is minus (-).

Output Line

On each output line (Fig. 1-67) leaving the ALD page, the sink page number (where the line is going), the line name (with the sign of the active state of the line), and the line origin are printed.

The line origin is composed of the serial number of the last logic block before the line name and the number of the printing line of that block.

Whenever the output line branches to several pages, the other "to" pages are listed below the sink page number.

In Fig. 1-67 the output line is "KH141 System Reset and MSS1". The sink page number is KH141 (the page where the line is going); the active state of the line is minus (-) and a description of the line would be "System Reset and MSS1"; the source point is the logic block whose serial number is AW, and the line leaves the block at position 4.

2. SMS Description

Basically the SMS logic blocks are presented in similar fashion as the SLT logic. However, there are some important differences which are pointed out by the following: (Refer to Fig. 1-65)

The logical blocks are identified with the same type symbols, but in addition, the symbol is preceded by a polarity of negative when that is the relative polarity necessary in order to satisfy that logical function. For example, a negative AND gate requires all the inputs to be negative in order to be satisfied. The flags used in SLT logic are not used on the SMS logic.

The position of the output line with respect to the logic block indicates whether the output is of the same relative polarity or the opposite relative polarity with respect to the input polarity when the logic block is satisfied. If the output line is connected to the upper half of the logic block, the output is of the opposite polarity. If the output line is connected to the lower half of the logic block, it is of the same relative polarity of the input when the logic function is satisfied.

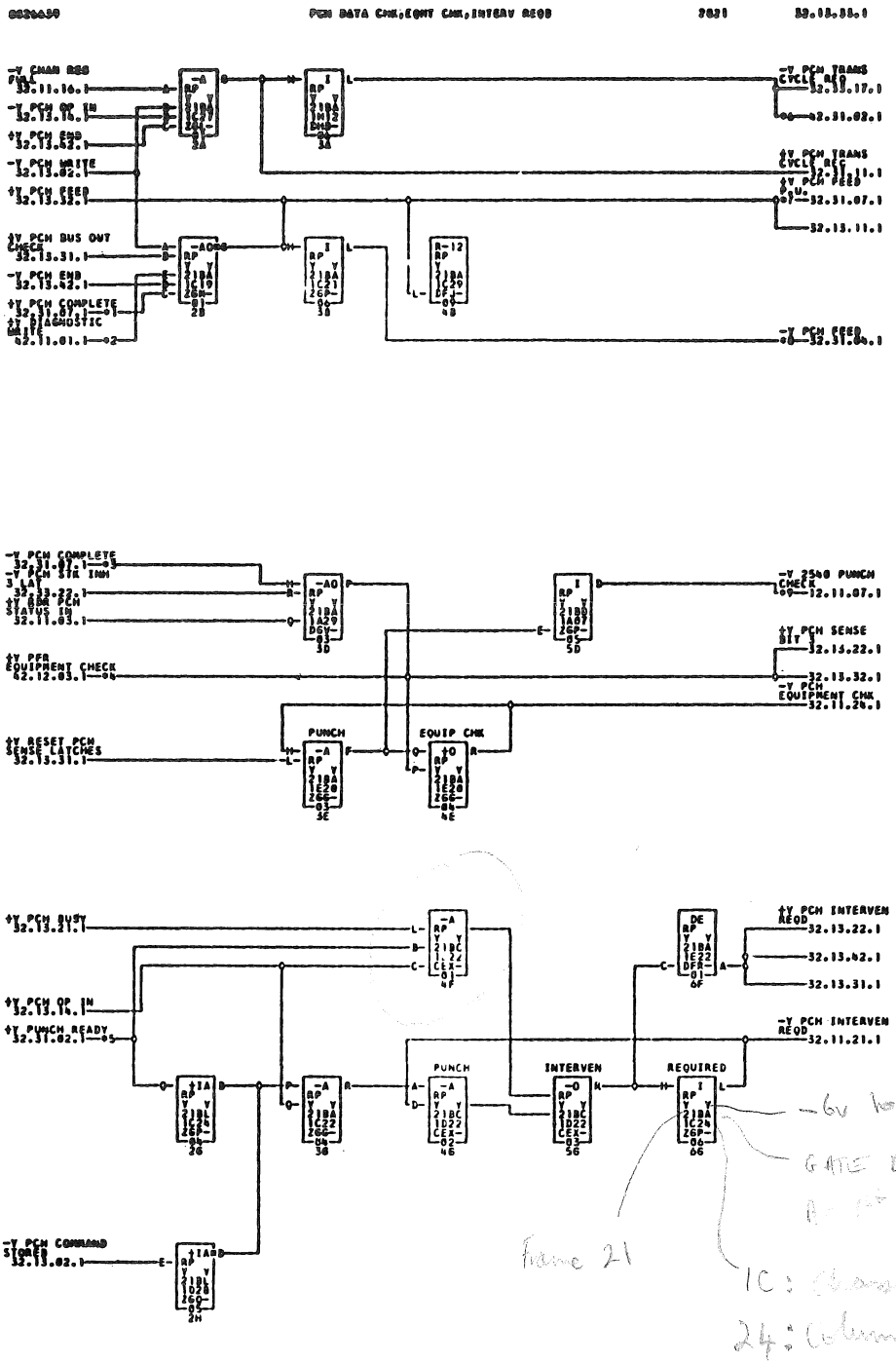


Figure 1-65. SMS, ICU ALD Example.

CHAPTER 2

COMPUTING ELEMENT

2-1. COMPUTING ELEMENT

The IBM-7201-01 Computing Element (CE) in the IBM-9020 System contains the logic to perform arithmetic, logical, and I/O instructions. In addition, the CE contains other facilities, such as maintenance aids and unique circuitry for the control and monitoring of a multi-element system.

The IBM-7201 Computing Element has a wide range of computing and processing capabilities. It can operate using fixed or variable-field length data. Arithmetic operations may be performed with decimal numbers, floating-point numbers, or binary numbers.

The CE has sixteen fullword general registers and four doubleword floating-point registers that are available to the programmer. These registers are located within a sixty-four word, Local Storage. The other locations within Local Storage contain working registers used for CE internal operations, and are not available to the programmer.

Data flow and instruction execution are controlled by a Read Only Storage unit. This is a capacitor storage unit operating on a 0.5-μsec cycle. The storage unit holds 2816, ninety-bit words used for CE internal control. Each ninety-bit word termed a microinstruction, controls the actions of the CE for that 0.5-μsec cycle. Groups of microinstructions are linked to form a microprogram. The microprogram controls an entire sequence of machine operating cycles to perform a complete operation. Read Only Storage is not normally addressable by the main program, and modification of the data contained in this unit can be made only by physically changing the components.

A control panel contains the switches and indicators necessary to monitor, operate, and control the computing element. The main functions of the control panel are to provide various operator controls and facilities for

displaying the contents of various functional units within the CE. The controls are divided according to their functions into the monitor section and the maintenance/operation section.

The 7201-01 Computing Element is constructed using the SLT structural form. There are 2 frames, a logic frame (01) and a power frame (02). The logic frame has five gates (A-E) and each gate contains up to 20 boards (A1-E4).

2-2. COMPUTING ELEMENT FUNCTIONAL UNITS

Within the Computing Element are blocks of electronic circuitry used to perform various computational functions. These blocks are referred to as the "functional units" of the element. The functional units and their related data paths are shown in Fig. 2-64. Those functional units shown within the heavy lines (Mover Out Bus and Adder Out Bus) are concerned primarily with internal data manipulation, while those around the periphery of the diagram are used primarily for system monitoring and system control features.

In examining the data flow chart in Fig. 2-64 the following 3 rules should be observed:

1. Data gates into the top of a functional unit and out the bottom.
2. The numerical bit positions shown above each functional unit, designate the bit position of the bus that can be gated into the functional unit. The line position, on which the numerical designations occur with respect to the functional unit, designate the bit positions assumed within the functional unit. Example: Bits 0 - 15 of the Adder Out Bus can be gated into bit positions 16 - 31 of the M register.
3. The bit positions at the output of the functional unit are represented numerically. The bit positions gated out of a functional unit are shown by the line position under the functional unit. The numerical designations under a functional unit refer to the

input positions of another functional unit or bus. Example: Bits 24 - 31 of the M Register are gated to bit position 0 - 7 at the right side of the mover.)

A. Registers

Registers in the 7201 processor are temporary storage devices usually composed of a number of polarity hold logic blocks. (A polarity hold is a block similar to a latch or trigger except that there are no resets.) A register may hold either control information or data as determined by the microprogram. Information is set into a register by a clock pulse which is also gated by the microprogram. A brief discussion of each of the registers follows. For convenience, these registers are arranged in alphabetic order.

1. Address Translation Register

The Address Translation Register (ATR) contains 48 bits although it is physically divided into ATR 1 and ATR 2 containing 32 bits and 16 bits respectively. This register is divided into twelve 4 bit groups. Each group is assigned a range of logical storage addresses. The content of each ATR position determines the physical Storage Element to be accessed for an assigned range of logical addresses.

The Address Translation Registers may be altered by the SATR instruction or changed manually from the CE Console during maintenance or testing. The contents of the ATR may be stored by the IATR instruction. Figures 2-1 and 2-2 are positive logic diagrams of the ATR.

This register is one of those used primarily for system control features and will be functionally incorporated into the system operation in subsequent material.

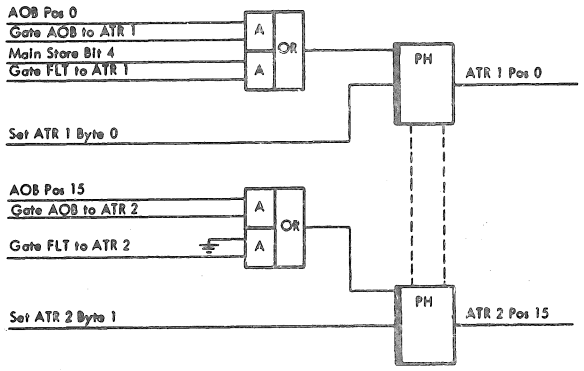


Figure 2-1. Typical ATR Positions.

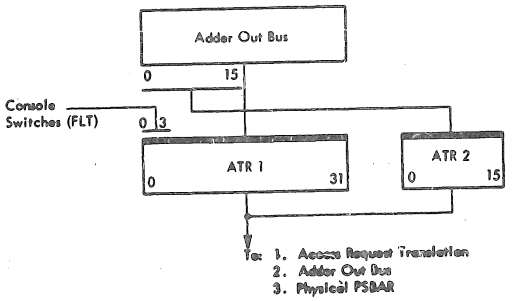


Figure 2-2. Address Translator Data Flow.

2. Check Registers

The check registers are used to indicate data flow erros within the processing unit. The Check Register Table shows the bit assignment for each position of these registers. They are displayed on the CE Operator's Console and included in the logout of the system.

CHECK REGISTER #1

Bit	Error Indicated
0	Half-Sum 0-7
1	Half-Sum 8-15
2	Half-Sum 16-23
3	Half-Sum 24-31
4	Full-Sum 0-7
5	Full-Sum 8-15
6	Full-Sum 16-23
7	Full-Sum 24-31
8	Group Carry
9	LB Counter
10	MB Counter
11	MD Counter
12	Length Counter (G1)
13	Length Counter (G2)
14	Mover Left Input
15	Mover Right Input
16	Mover Output
18	Storage Address Register 8-15
19	Storage Address Register 16-23
20	Storage Address Register 24-31
21	ROS 1-30
22	ROS 32-55
23	ROS 57-89
26	Log Request

CHECK REGISTER #2

Bit	Error Indicated
0	CCR Parity
1	Storage Check
2	Storage Timeout
3	SE LOS
4	Fetch Data Check
5	Invalid ROS Address
6	Log ROS
7	Log Adr
8	CE Logout Request
9	Control Bus Check
10	PSBAR ELC
11	PSBAR Parity
12	Split Logout

STORAGE CHECK REGISTER

Bit	
0	Binary decode to determine SE
1	
2	
3	

Check Register Table

3. Configuration Control Register (CCR)

The Computing Element's Configuration Control Register contains 36 bit positions (32 control bits and 4 parity bits). This register is set internally or from another CE's External Register by means of a SCON instruction. It may also be set from the CE Control Panel for maintenance or tests. The CCR defines which elements are able to communicate with one another, and from what element certain control instructions may be accepted. (See Fig. 2-3).

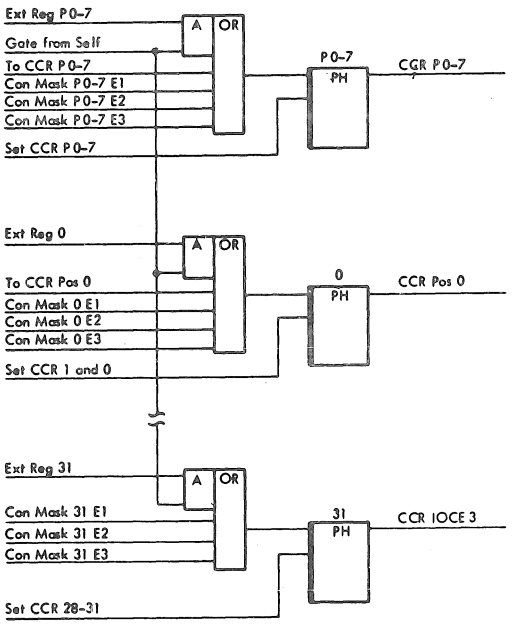


Figure 2-3. Typical Configuration Control Register Positions.

4. Diagnose Accessible Register

The Diagnose Accessible Register (DAR) is a 32 position register normally accessible by the diagnose instruction. The register contains the external interrupt requests shown in Fig. 2-4. Any DAR bits not masked by the DAR mask in the Select Register will cause an external interrupt if PSW bit 7 is on. This interrupt will cause bit 31 of the old PSW to be set. Figure 2-5 is a typical DAR position.

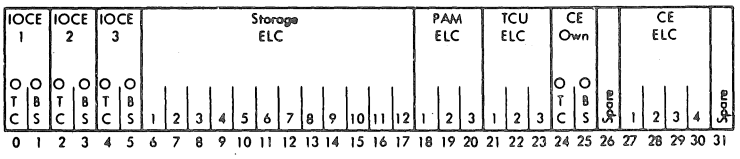


Figure 2-4. Diagnose Accessible Register.

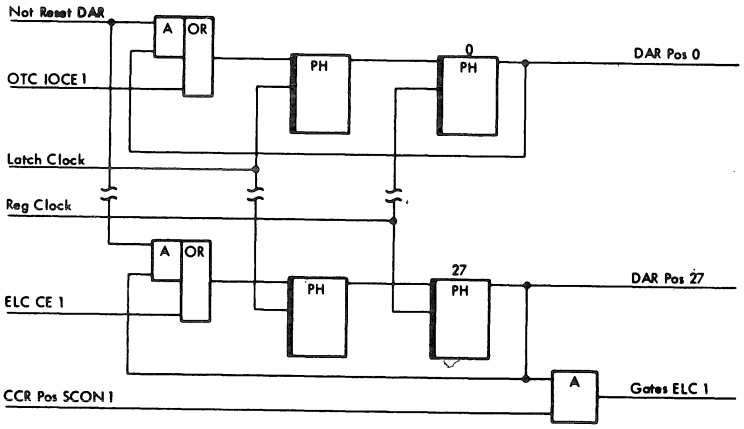


Figure 2-5. Typical Positions of DAR.

5. External Register

The External Register in the Computing Element is a 36 bit (32 data bits plus 4 parity) register used to supply I/O operation codes, unit and channel address, and PSW information for FLT, IPL and I/O instructions. This register also provides the configuration mask for selected elements in the Set Configuration (SCON) instruction. Figures 2-6 and 2-7 are typical positions of the External Register and Data Flow and gating for the External Register.

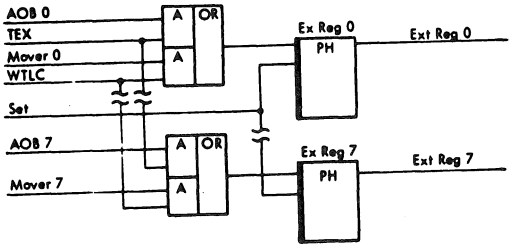


Figure 2-6. Typical Positions of External Register.

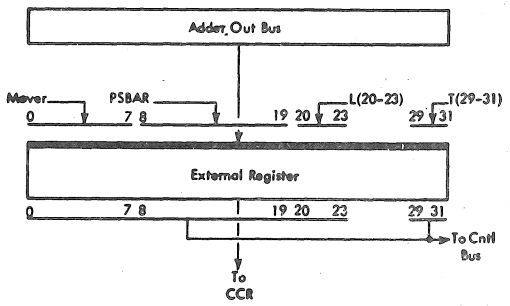


Figure 2-7. External Register Data Flow and Gating.

6. External Interrupt Register

The External Interrupt Register (INTR) provides buffering for 12 interrupts. Referring to Fig. 2-8 positions 20-23 and 26-29 indicate CE read direct and write direct interrupts. Positions 24 and 25 indicate timer and console key interrupts respectively. Position 30 is a spare and position 31 indicates that one or more interrupt requests are pending in the DAR. These interrupt conditions are maskable by PSW bit 7. Position 31 is also maskable by the Select Register. (Position 0-26 of DAR will set bit 31 of INTR if the corresponding bit of the DAR mask in the Select Register is on.)

7. F Register

The F Register is a 4 bit register used in the shifter data path. When added outputs are shifted, the bits entering the overflow latches may be spilled into the F Register for temporary storage. Also, bits from the F Register may be entered into the adder out bus latch positions.

Figure 2-9 shows both the overflow latches and how they are set. Because the F Register is involved with shifting the adder outputs, additional information will be found in the section on the Shifter Data Path.

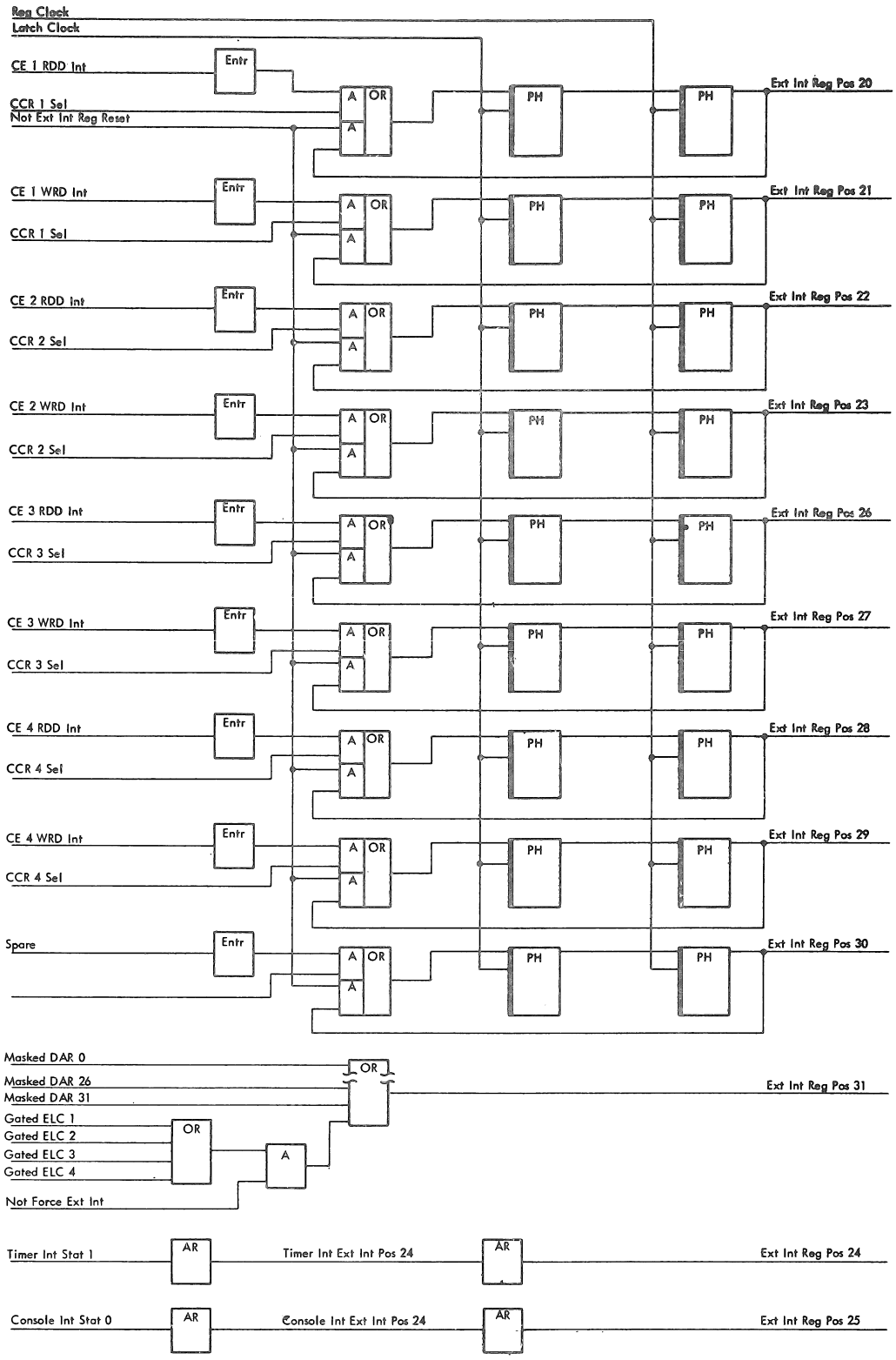


Figure 2-8. External Interrupt Register.

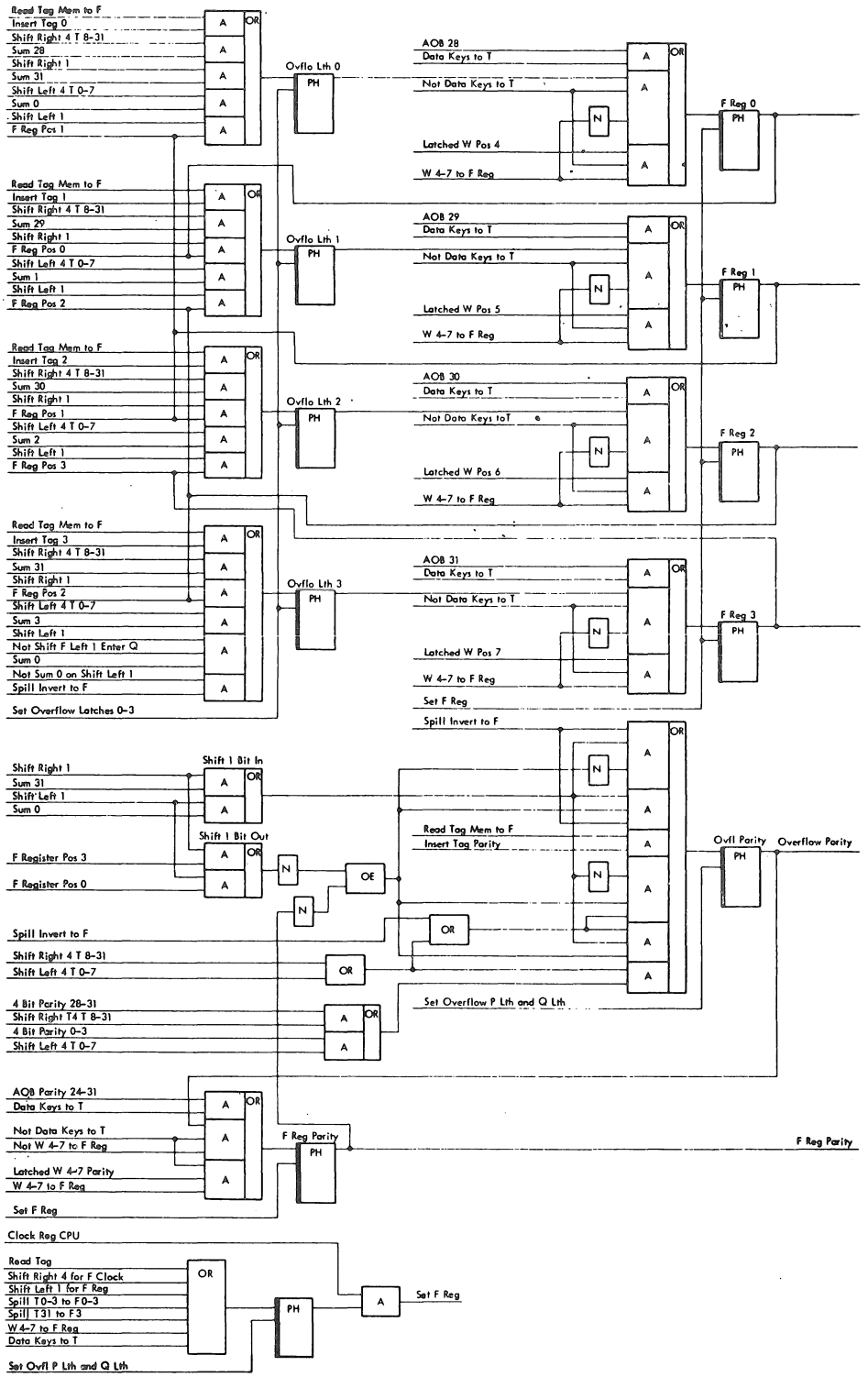


Figure 2-9. F Register and Overflow Latches.

8. H Register

The H Register is an alternate source of data for the adder Y input. Information may be gated into the H Register from the instruction address bus (bits 8-31), the adder out bus (bits 0-31), or the adder overflow latches (bits 0-3). Figure 2-10 is the graphic representation of the H Register while Fig. 2-11 shows how this register is set.

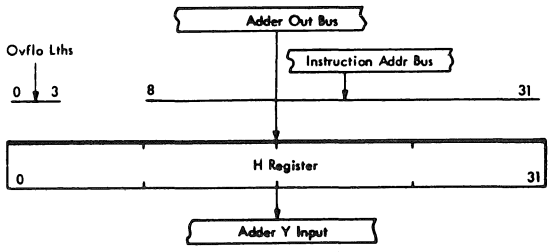


Figure 2-10. H Register Data Flow and Gating.

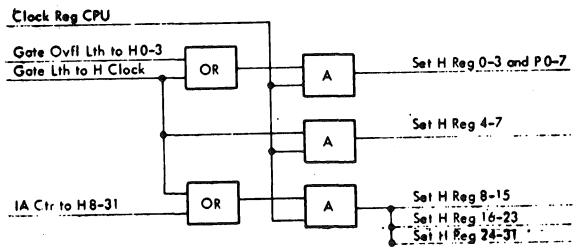


Figure 2-11. H Register Set.

9. Instruction Address Register

The Instruction Address Register (IAR) together with the instruction address counter and its associated output latches, is used to keep track of the address in main storage of the NEXT instruction.

Because all instructions are either 2, 4, or 6 bytes long and main storage delivers data in one word (4 byte) increments, we update the instruction address by either 2 or 4 (bytes) each time it is used.

Figure 2-12 shows the low order positions of the Instruction Address Register and the circuitry used to update the instruction address after each use. High order positions are similar except instead of "count by 2 and count by 4" lines, carry lookahead lines from the lower positions are used.

10. J Register

The J Register is a four bit storage area used to supply bits 2-5 of the local storage address under control of the microprogram. The J Register is supplied inputs from either the adder out bus or from the mover out bus and parity is supplied from the adder latch 8-11 or the mover latch 0-3 parity positions respectively. Figure 2-13 is the logic flow and gating 2nd level for the J Register.

11. L Register

The L Register is the primary source of data for the adder left (XG) input; it also serves as a data buffer register for local storage. The entire contents of the L Register may be gated to the adder input, or bit positions 16-31 may be gated to positions 0-15 of this input. In addition, any byte of data from the L Register may be gated to the U input of the Mover, and a path is available to gate the entire contents of this register to Local Store. Figure 2-14 is the data flow and gating diagram for the L Register and Fig. 2-15 is the register set logic for this register. The inputs to the L

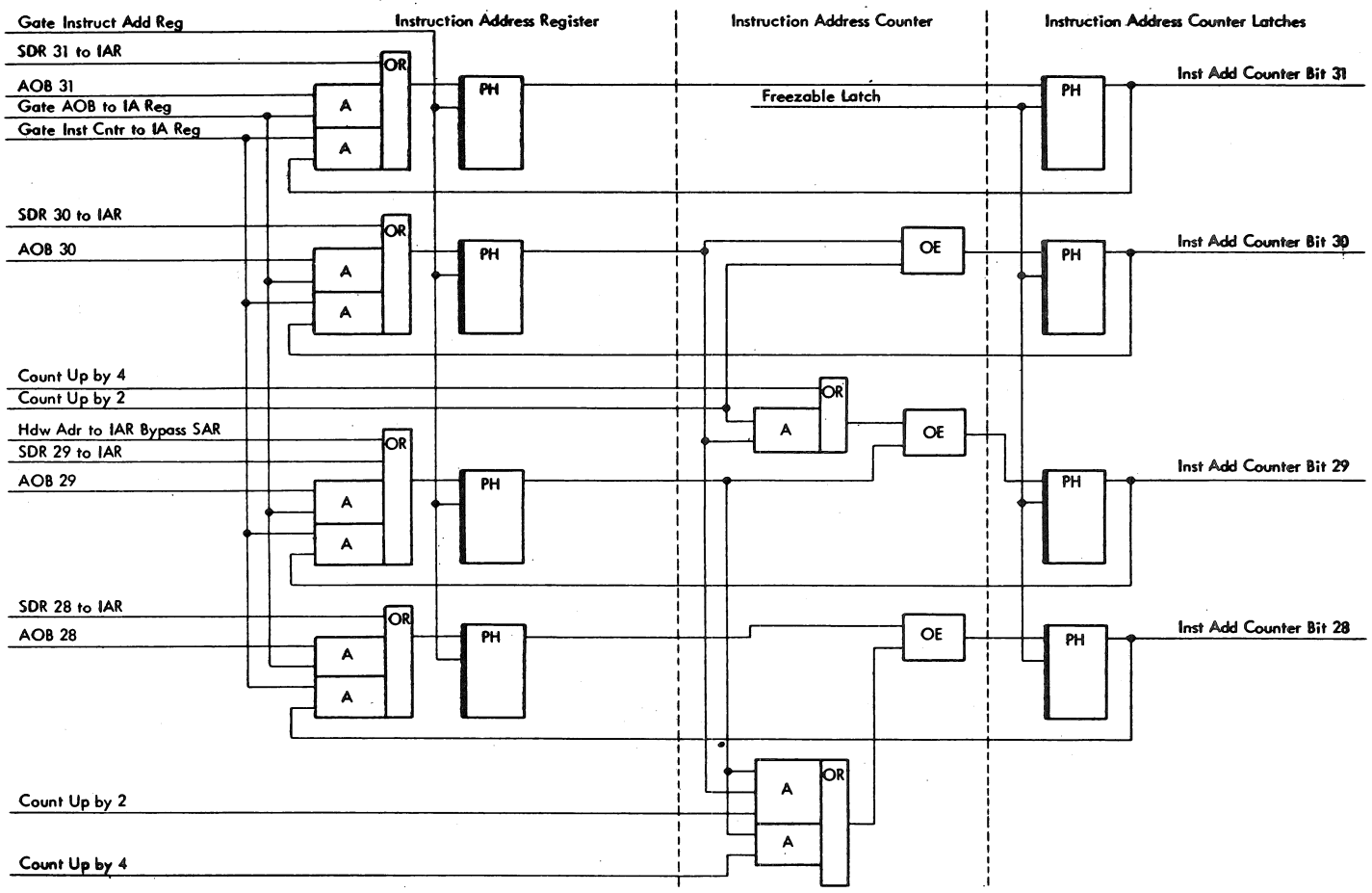


Figure 2-12. Instruction Address Register and Counter.

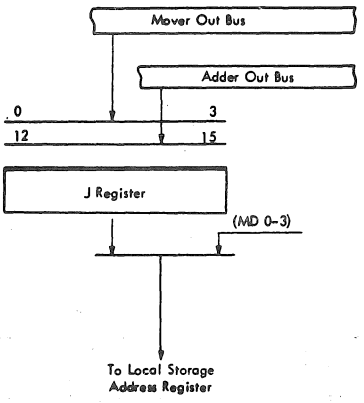


Figure 2-13. J Register Data Flow and Gating.

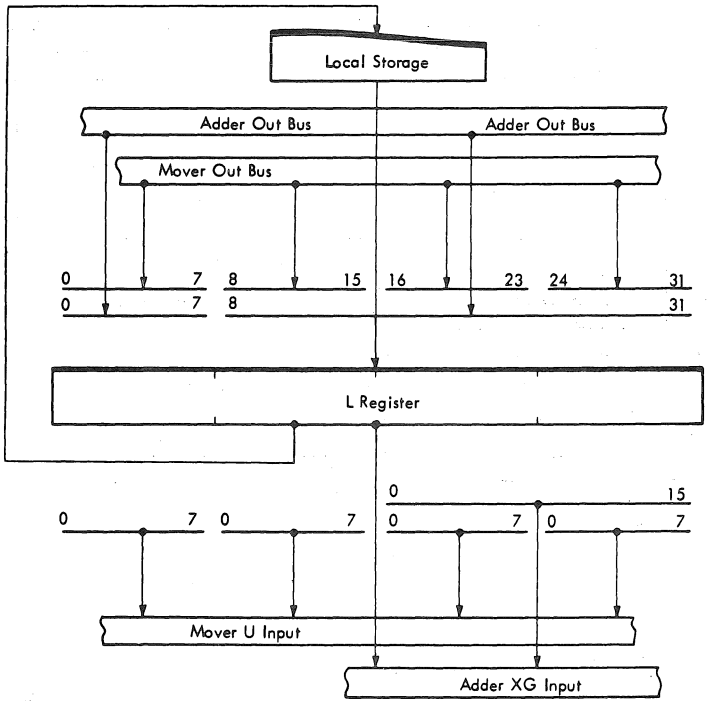


Figure 2-14. L Register Data Flow and Gating.

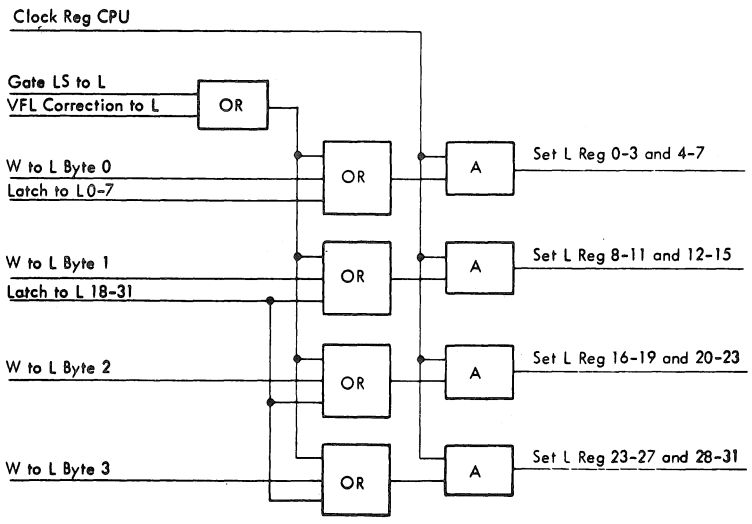


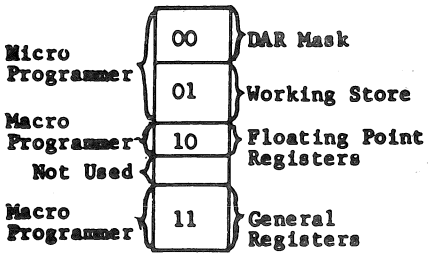
Figure 2-15. L Register Set.

Register are supplied from either the adder out bus, the mover out bus, or local store, all of which are under control of the microprogram.

12. Local Store Address Register

Local Storage in the 7201 Computing Element consists of a two dimensional ferrite core storage unit providing storage for 64 words of 36 bits each. Not all of the available storage space is utilized in the Computing Element. Local Storage operates on a 500 nanosecond read/write cycle time thus providing high speed random access storage for use within the processor.

The table in Fig. 2-16 indicates the permanent uses to which the various local store areas are put to in the 9020 System. Notice that the local store array is divided into quadrants, with each quadrant having a specific function or type of data. This data will be supplied from either the L Register or the R Register under the control of the microprogram. Once the data is stored in the array it will remain until it is changed (or read out and not restored) even though power may have dropped. The preservation of the data in local store in power off conditions will be true provided that the control



Sector	Word	
00	0000 to 1111	DAR Mask-all words
01		WORKING STORE Entire Sector is Micro-Programmer scratch pad
	0111	PSW left half backup
	1110	Instruction backup
10		FLOATING POINT REGISTERS
	0000 thru 0111	FP Registers 1 thru 4 (Double Word Registers)
11		GENERAL REGISTERS
	0000 thru 1111	Fixed Point Registers (16)

Figure 2-16. Local Storage Location Chart.

lines to memory were off prior to the power loss and that the local store is not selected until the logic voltages have all sequenced up.

Figure 2-17 shows the data and addressing paths for Local Store. It should be noted that either the L or the R Registers may be used for the input and/or output. It is also possible to read data into one of these registers and write data back to Local Store from the other. The sense register latches retain the data readout during a Local Store cycle until the next start memory cycle occurs. It is in this manner that a parity error associated with Local Storage operation may cause the data readout to be gated back into the same address from which it was read out.

The Local Storage matrix is addressed by a six bit address register. This register feeds the gate drivers, read drivers, and the write drivers to determine the specific word for read or write operations. Decoding of the LSAR bits to determine gate, read, and write drive lines may be examined on Fig. 2-17. The data contained in this register is retained from one cycle to the next. Local storage addressing is under the control of the micro-program and data may be supplied to the LSAR either directly from the ROSDR, or under micro-order control from the Local Store Function Register, the J Register, or the MD counter.

13. Local Store Function Register

The Local Store Function Register is a two bit register used to store the high order bits of the address. This register will gate these two bits to the Local Store Address Register (under the control of the microprogram) to select the quadrant of local store to be used for this access. The data is gated into the LSFN directly from the microprogram control word (Emit Field).

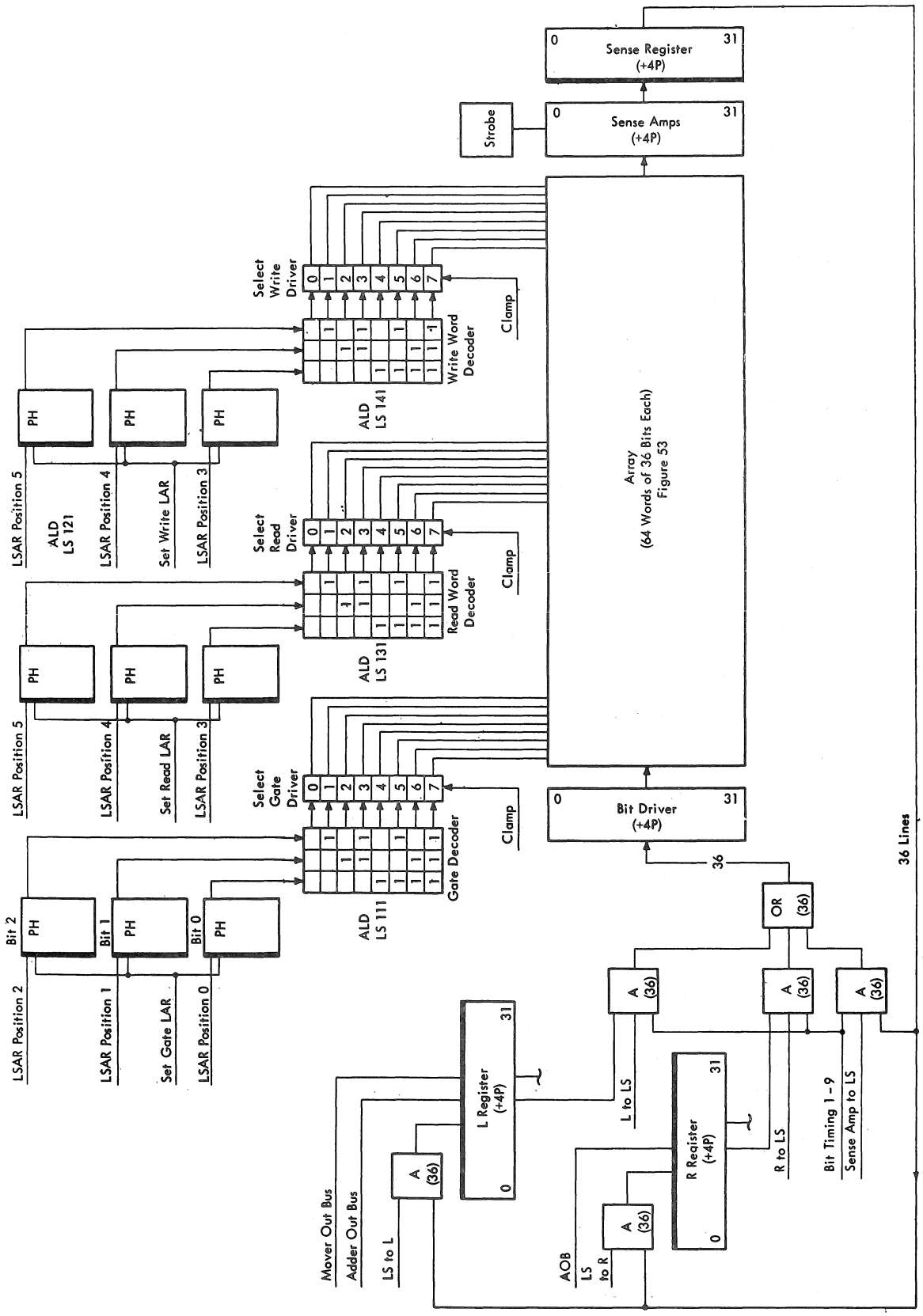


Figure 2-17. Local Storage Address and Data Paths.

14. M Register

The M Register is a source of data for both the adder Y input and the mover V input.

Figure 2-18 shows that information on the mover out bus can gate into any byte of the M Register. Also, either the entire 32 bits of the adder out bus can gate into the M Register or bits 0-15 can gate into positions 16-31.

Notice that any M Register byte can gate out to the mover V input. Notice also that by gating positions 0-15 of the AOB into positions 16-31 of the M Register it is possible to effectively shift right by 16 positions (or two bytes).

Figure 2-19 shows how the M Register is set.

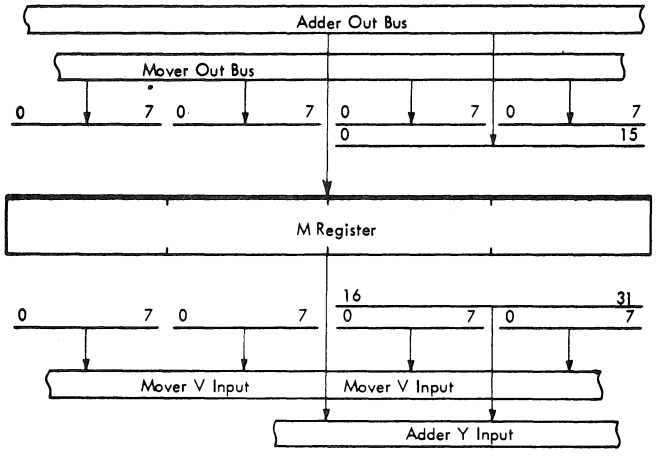


Figure 2-18. M Register Data Flow and Gating.

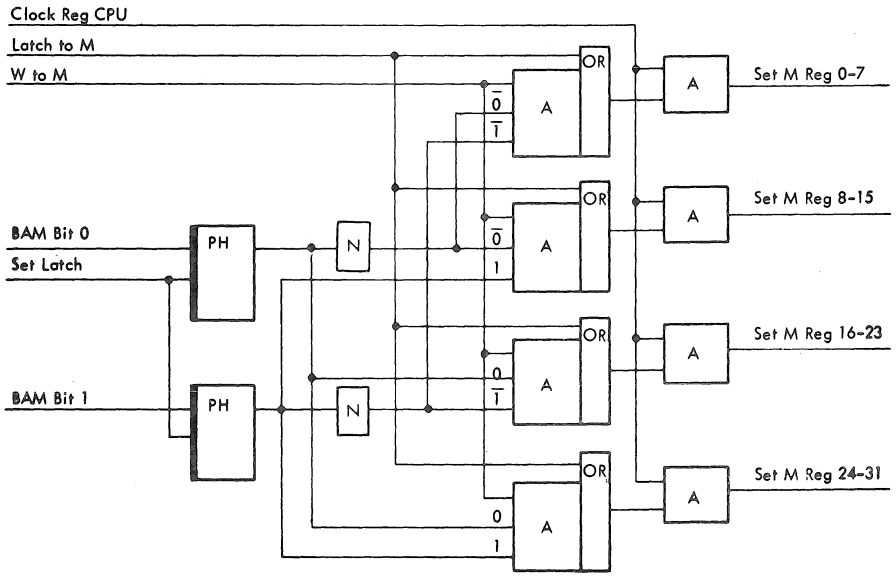


Figure 2-19. M Register Set.

15. Mover Function Register

Because many of the commands given to the mover are repetitive for a given situation, a mover function register can temporarily store a micro-order. The content of the mover function register, then controls the particular function to be performed by the mover.

Figure 2-20 is an active level diagram of the mover function register and Fig. 2-21 shows what each possible bit combination causes the mover to do. The active level diagram shown is for the IOCE; however, by the deletion of the circuits used in the I/O mode, the circuits in the CE are identical.

16. Preferential Storage Base Address Register

The purpose of the PSBAR is to reference the proper PSA currently assigned and associated with the CE or IOCE program. PSA references to old and new PSWs, channel CAWs, and CSWs, and logout areas always refer to low-order

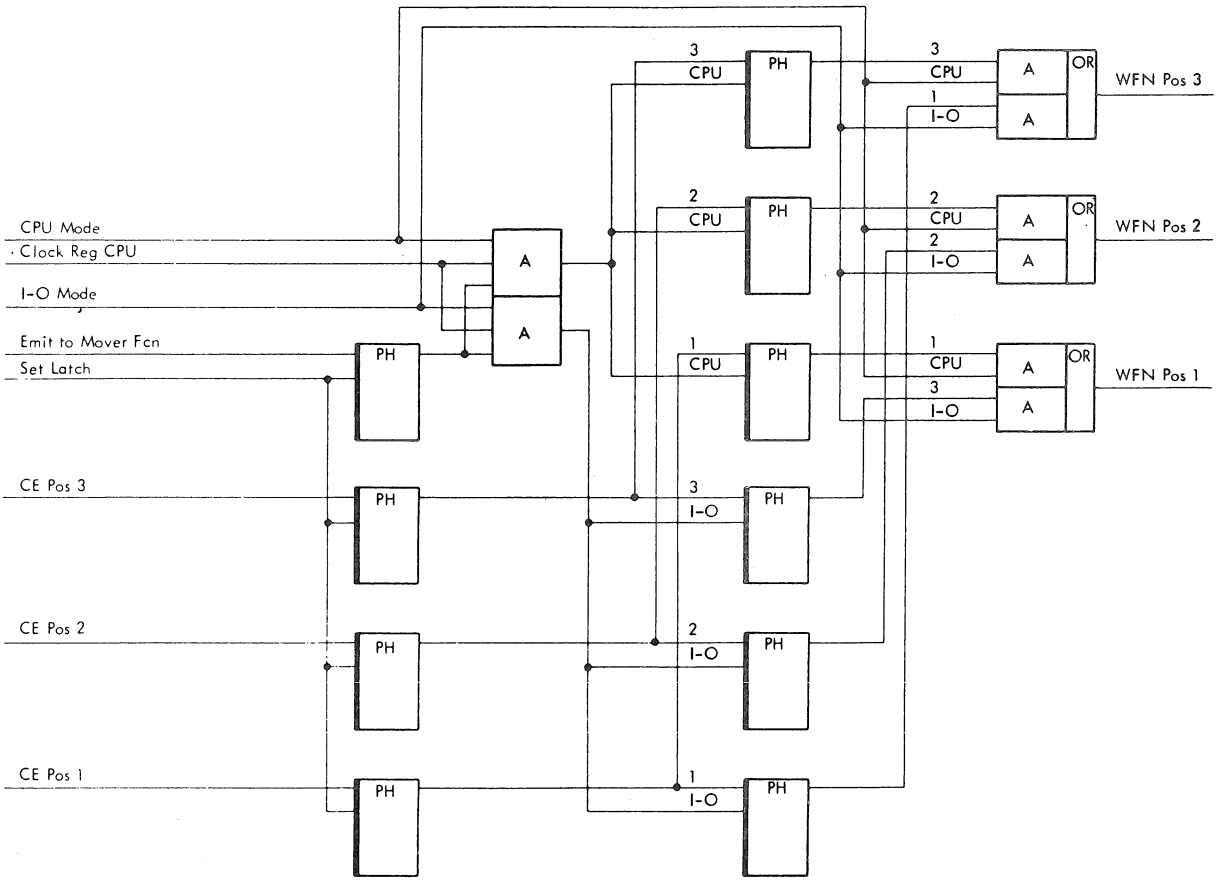


Figure 2-20. Mover Function Register (WFN).

	U0-3 to W4-7 U4-7 to W0-3	OR	AND	Exclusive OR	U0-3 to W0-3 U4-7 to W4-7	U0-3 to W0-3 V4-7 to W4-7	V0-3 to W0-3 U4-7 to W4-7
CPU Mode	000	001	010	011	100	101	110
I/O Mode	000	100	010	110	001	101	011

Figure 2-21. Mover Function Register Values.

fixed addresses starting at location zero. The low-order addressing is automatically recognized by hardware circuits whenever the 12 high-order bits are all 0's. When high-order 0's are detected, the 12 bit PSBAR value is OR'ed with these zeros to produce a reference to the proper PSA area.

The OR'ing of PSBAR is completely automatic and is performed at the out bus to the SE. Note that the original address contained in the instruction is not changed. PSBAR is composed of both a logical and physical PSBAR related to each other through the Address Translation Register as shown in Fig. 2-23.

17. Logical PSBAR

This 12 position register is loaded by the load PSBA instruction, and once loaded will retain its initial setting until reloaded or changed by an external start. Figure 2-22 is the positive logic diagram for the logical PSBAR.

Positions of the register are labeled to match their corresponding address positions. The twelve positions may be divided into three logical sections: positions 15-19, which can select a particular PSA within a storage element; positions 9-14 which select a particular SE (or LCS); and position 8 which is not used.

As will be explained later, positions 9-14 of logical PSBAR are gated into a 6 position binary counter that is used to automatically select a new SE under certain malfunction conditions. The logical register bits (15-19) and the present position of the 6 position counter (9-14) can be obtained by the program by means of the Store PSBA instruction.

18. Physical PSBAR

The physical PSBAR specifies the physical (actual) SE/LCS to be used in the storage reference. This physical PSBAR can be thought of as a seven position register accounting for positions 8-14 of the address. Actually, physical PSBAR is a four position register set to the identification character found

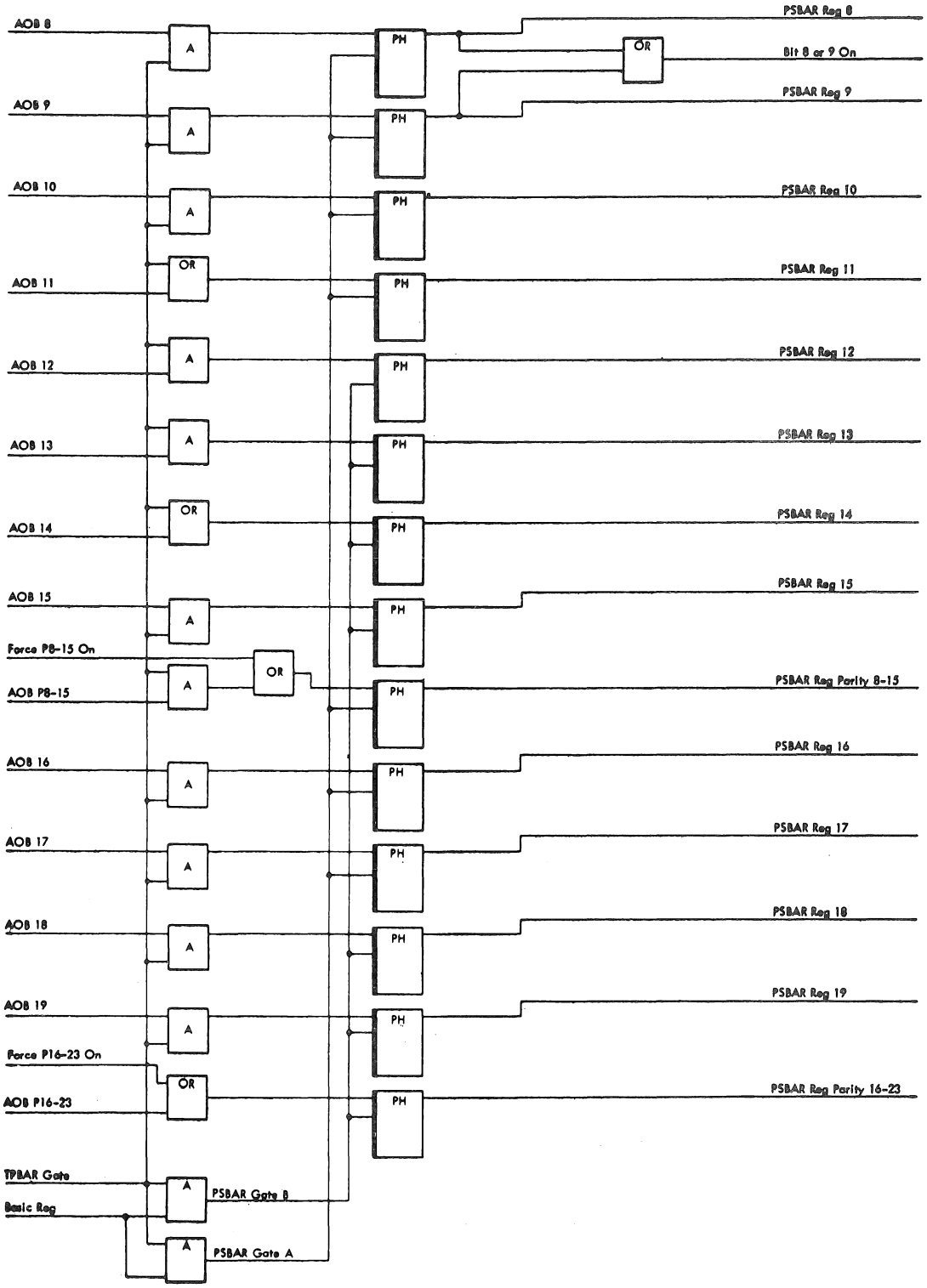


Figure 2-22. Logical PSBAR.

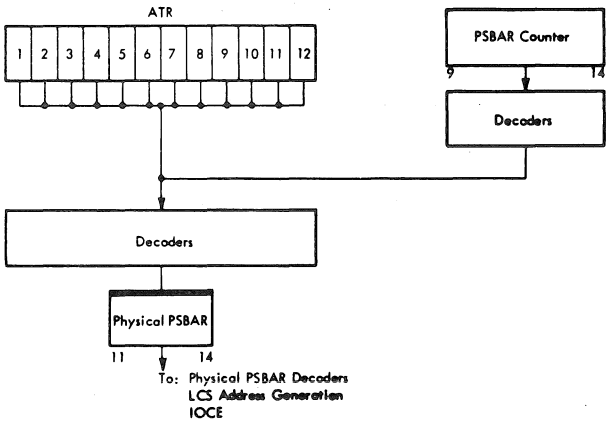


Figure 2-23. Physical PSBAR Data Flow.

in the corresponding position of the ATR. Because the contents of Physical PSBAR are always available in translated form, references to the preferential storage are relocated independent of the ATR. (Refer to Figs. 2-23 and 2-24).

19. PSBAR Counter

Positions 9-14 of the logical PSBAR are set into a six position binary counter which is considered to be an integral part of the logical PSBAR. By means of this counter, each CE can automatically reference an alternate PSA whenever inhibit logout stop (ILOS) bit is off in the CCR, and a failure occurs on an access to the SE containing the primary PSA. The alternate PSBA is obtained by incrementing the counter (adding successive 131,072-byte increments) until the next configured SE is reached.

As the counter is stepped, each higher logical position of ATR is tested for an identifier character of a configured SE. When the first configured SE is FOUND IN THE ATR, physical PSBAR is updated with the new identifier character. PSA references are now made to this new storage element where the operational program has previously set up proper PSWs, CAWs, CSWs, etc., for use in this situation.

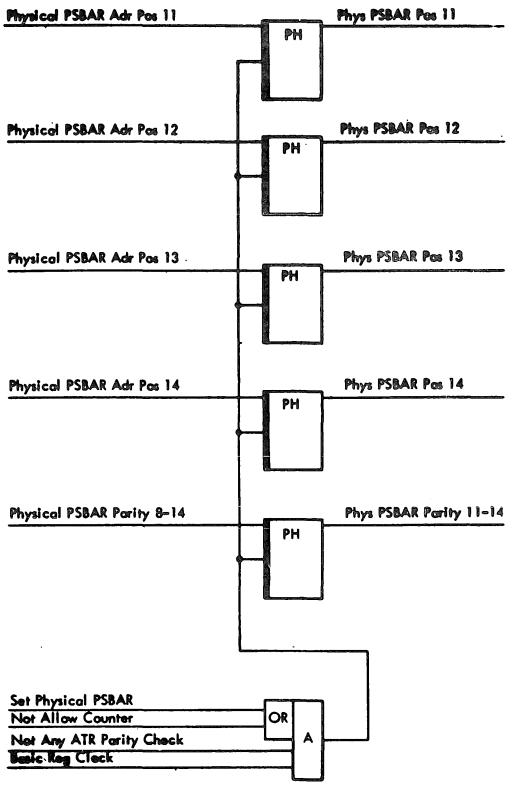


Figure 2-24. Physical PSBAR

If the counter reaches the highest SE in the system, incrementing continues past the non-existing SEs until an end-around effect is achieved, stepping from the highest to the lowest SE. The ATR is again tested from left to right until an alternate SE is found. After stepping to an alternate storage element, the PSBAR counter is inhibited from further stepping until a load PSBA instruction is executed by the CE. This instruction (or an external start) resets the counters stepping abilities and allows normal incrementing to take place. (Refer to Fig. 2-25).

20. Program Status Word Register

The Program Status Word (PSW) contains detailed information on the status of the CE. The current PSW is divided between transistor register positions and a local storage location. PSW bits 0-19 are maintained in transistor registers, which perform the required functions by direct logic controls or by being accessible for microprogram branching. These positions are also buffered in local storage location 01, 0111 since they do not have a read-out path (except for scan-out). Positions 32-39 of the PSW are also held in transistor register positions, which may be set by logic or through the mover. These bits may be read out through the mover. Positions 40-63 of the PSW are held in the instruction address register. See 7201-01 Data Flow Diagram, Fig. 2-64.

The type of interrupt determines the interruption code to be stored in positions 20-31 of the old PSW address. In the basic interruption sequence the old PSW is assembled from the local storage buffer location, the interruption code, the transistor registers containing positions 32-39, and the instruction address register. Each of the two words of the PSW is stored as it is assembled. The storage protection key is set to zero in order to ensure successful storing.

By storing the PSW, the program can preserve the detailed status of the CE for later use. By loading a new PSW or part of a PSW, the state of the CE may be changed.

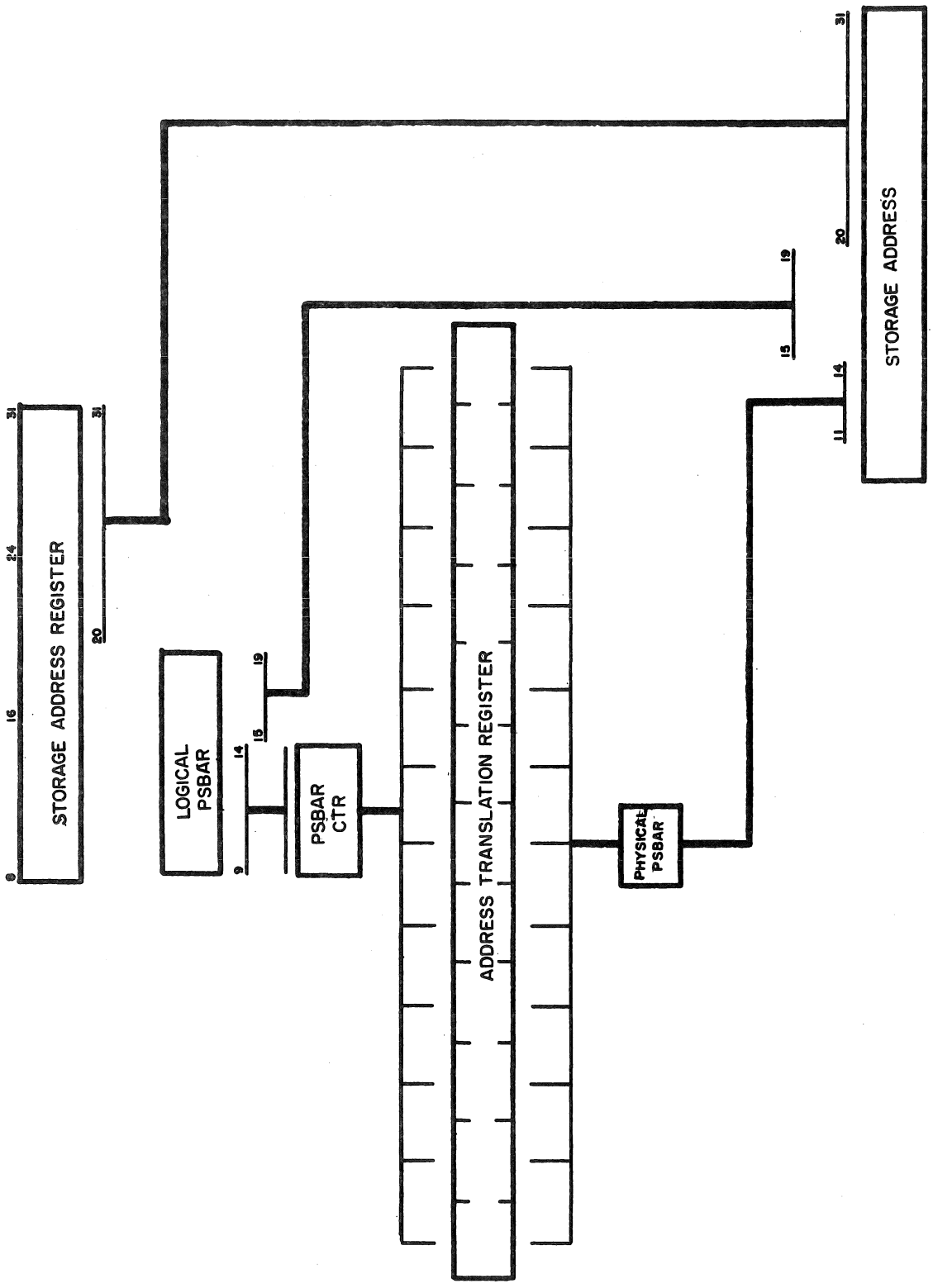


Figure 2-25. Preferential Storage Data Flow.

All or part of a PSW may be stored or loaded. The entire PSW is stored and a new PSW is introduced when the CE is interrupted. The rightmost 32 bits are stored in Branch and Link. The Load PSW instruction introduces a new PSW. Set Program Mask introduces a new condition code and program mask in the PSW. Set System Mask introduces a new system mask. See Fig. 2-26.

System Mask: Bits 0-7 and 16-19 of the PSW are associated with I/O Channels and external signals as specified in the following table. When a mask bit is 1, the source can interrupt the CE. When the bit is 0, the corresponding source cannot interrupt the CE and the interruption remains pending.

System Mask Bit	Interruption Source
0	Multiplexor Channel A
1	Selector Channel 1A
2	Selector Channel 2A
3	Selector Channel 3A
4	Multiplexor Channel B
5	Selector Channel 1B
6	Selector Channel 2B
7	Timer, Interrupt Switch; External Switch
16	Selector Channel 3B
17	Multiplexor Channel C
18	Selector Channel 1C
19	Selector Channel 2C

Protection Key: Bits 8-11 of the PSW form the CE protection key. The key is matched with the four high-order bits of a storage key whenever data are to be stored, or whenever data are to be fetched and the fetch-protection bit in the storage key is 1.

AMWP: These letters represent bits 12-15 of the PSW.

A (bit 12) represents ASCII. When bit 12 of the PSW is 1, the codes for the extended ASCII format are generated for decimal results. When PSW bit 12 is 0, the codes for the extended binary-coded-decimal format are generated.

M (bit 13) represents machine-check mask. When PSW bit 13 is 1, the machine-check interruption, element check (ELC) out signal and diagnostic logout

occur upon malfunction detection. When PSW bit 13 is 0, the CE is masked for machine-check interruptions. The interruption and logout do not occur. An ELC out signal is issued as before and the interruption remains pending.

W (bit 14) represents the wait state. When bit 14 of the PSW is 1, the CE is in the wait state. When PSW bit 14 is 0, the CE is in the running state.

P (bit 15) represents the problem state. When PSW bit 15 is 1, the CE is in the problem state. When PSW bit 15 is 0, the CE is in the supervisor state.

Interruption Code: Bits 20-31 of the PSW identify the cause of an I/O, program, supervisor call, external or machine-check interrupt. Use of the code for all five interruption types may be found in 9020 Principles of Operation.

Instruction Length Code (ILC): The code in PSW bits 32 and 33 indicates the length in halfwords of the last interpreted instruction when a program or supervisor-call interruption occurs. The code is unpredictable for I/O, External, or machine-check interruptions.

Condition Code (CC): PSW bits 34 and 35 represent the condition code. The condition codes for all instructions may be found in 9020 Principals of Operation.

Program Mask: PSW bits 36-39 represent the program mask bits. Each bit is associated with a program exception. When the mask bit is 1, the exception results in an interruption. When the mask bit is 0, no interruption occurs. The significance mask bit also determines the manner in which floating-point addition and subtraction are completed.

Instruction Address: Bits 40-63 of the PSW are the instruction address. This address specifies the left-most 8-bit byte position of the next instruction and is in the instruction address register.

Figure 2-27 is a partial data flow diagram for the PSW Register, while Fig. 2-28 represents the active logic diagram for this functional unit.

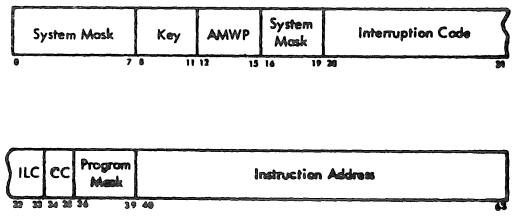


Figure 2-26. Program Status Word Format.

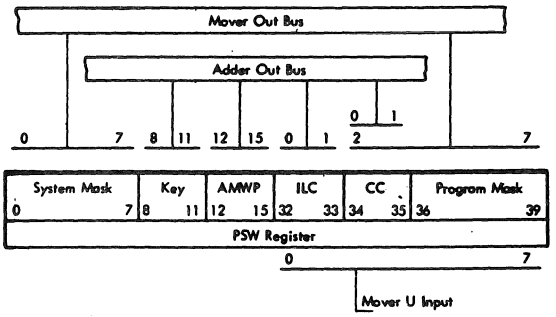


Figure 2-27. Functional Flow Diagram for PSW Register.

21. Q Register

The Q Register is a one-bit register used in the shifted data path. When adder outputs are shifted, bits entering the overflow latches may be spilled into the Q Register for temporary storage. Also depending on the micro-order, a bit in the Q Register may be entered into the AOB latch positions that may be left vacant by a shift.

Figure 2-29 is a positive logic diagram showing the gating into and out of the Q Register.

Because the Q Register is involved with shifting the adder outputs, additional information on this register may be found in the section entitled Shifter Data Path.

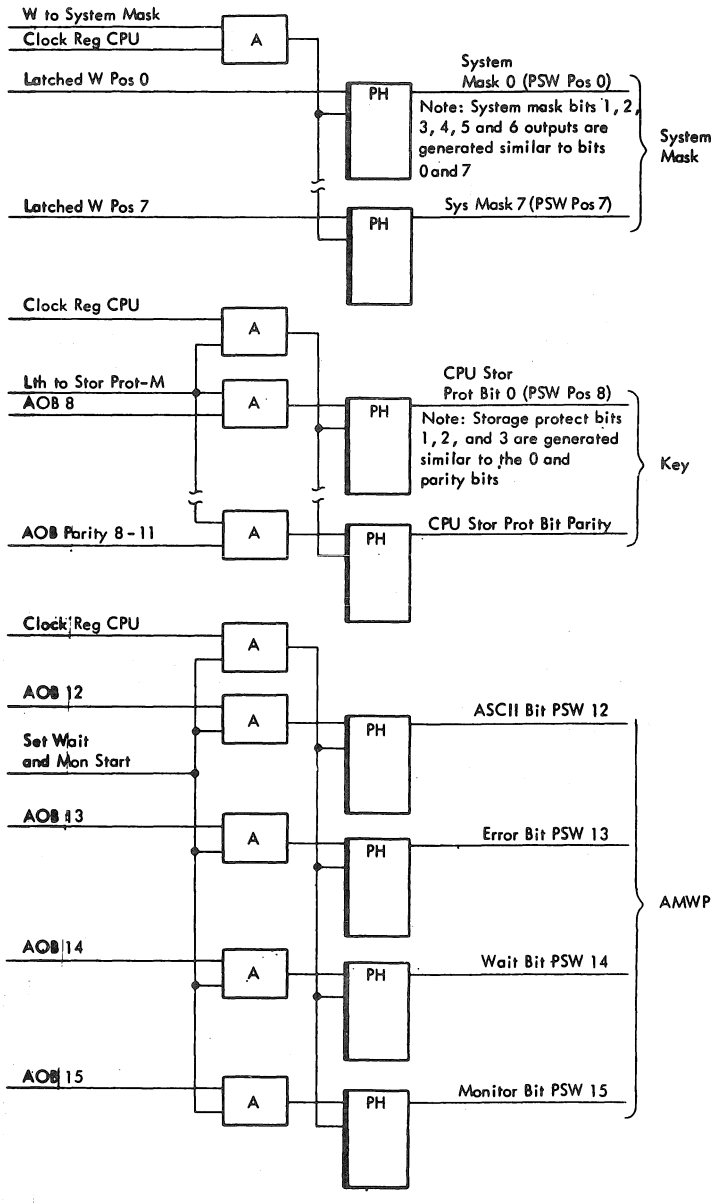


Figure 2-28. PSW Register (Page 1 of 2).

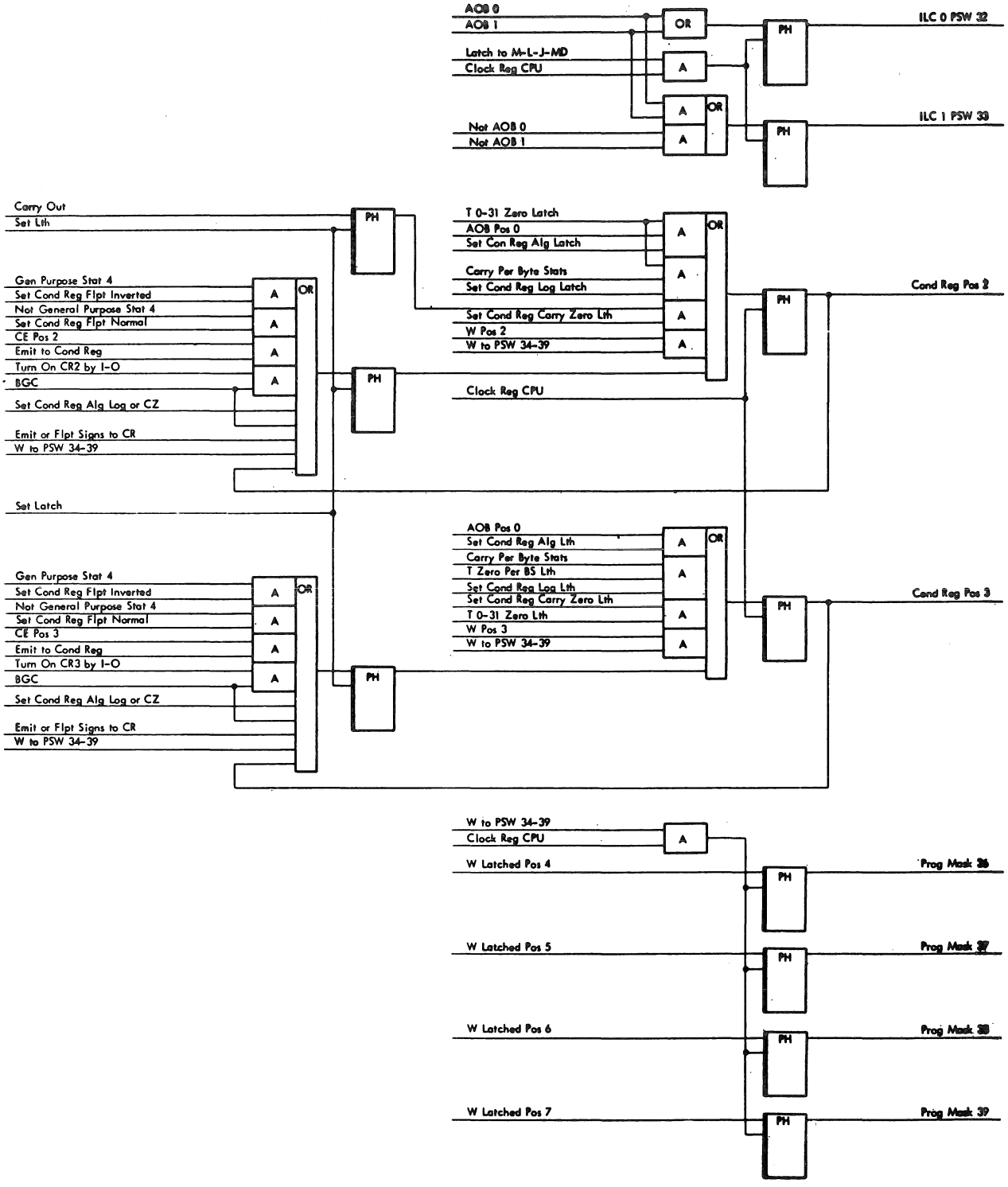


Figure 2-28. PSW Register (Page 2 of 2).

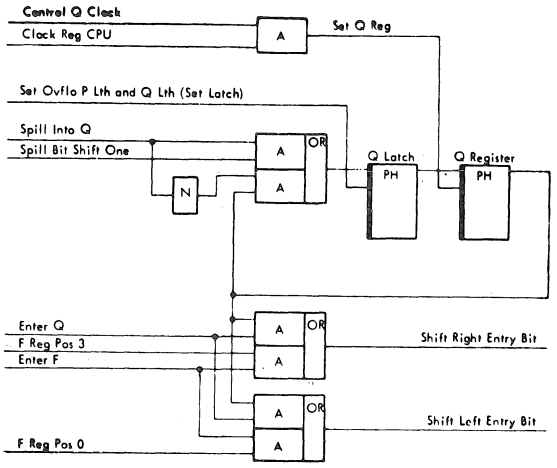


Figure 2-29. Q Register and Latch.

22. R Register

The R Register is the primary source of data for the adder Y input and serves as a buffer register for local storage. The entire R Register word can be gated to both the adder Y input and local storage. In addition, the low-order byte (bits 24-31) can be gated to the mover U input. Figure 2-30 is the data flow diagram for the R Register and Fig. 2-31 is the R Reg set circuitry.

23. Read Only Address Register

The Read Only Storage Address Register (ROAR) supplies the address that selects the next CROS word. The present CROS word controls the address sent through the address register. ROAR is composed of a 12-position address register and three 12-position buffer registers.

The address register is not a storage register; instead, the address register is an OR circuit that gates the output of other system-registers to the address-decode circuits.

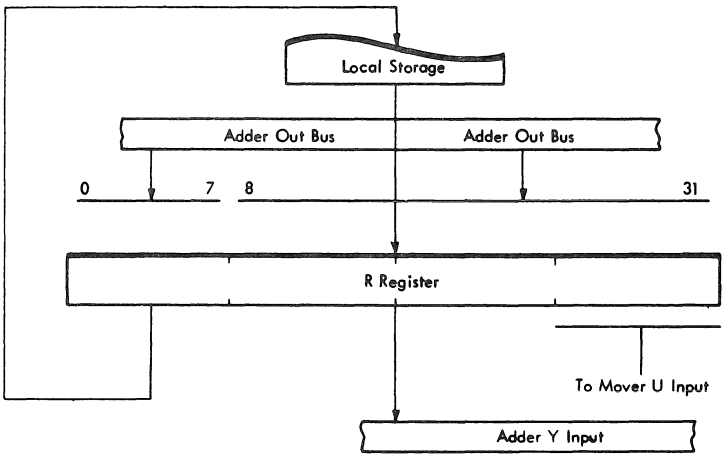


Figure 2-30. R Reg Data Flow.

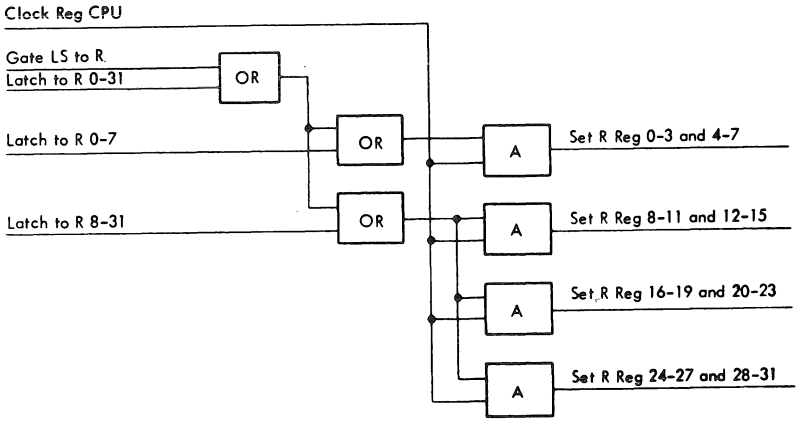


Figure 2-31. R Register Set.

The ROAR bit positions are divided, by the source of their input data, into four groups. These groups are the base-address bits (positions 0-5), the function-branch bits (positions 6-9), the A-branch bit, and the B-branch bit. Figure 2-32 shows the control circuits for all ROAR positions.

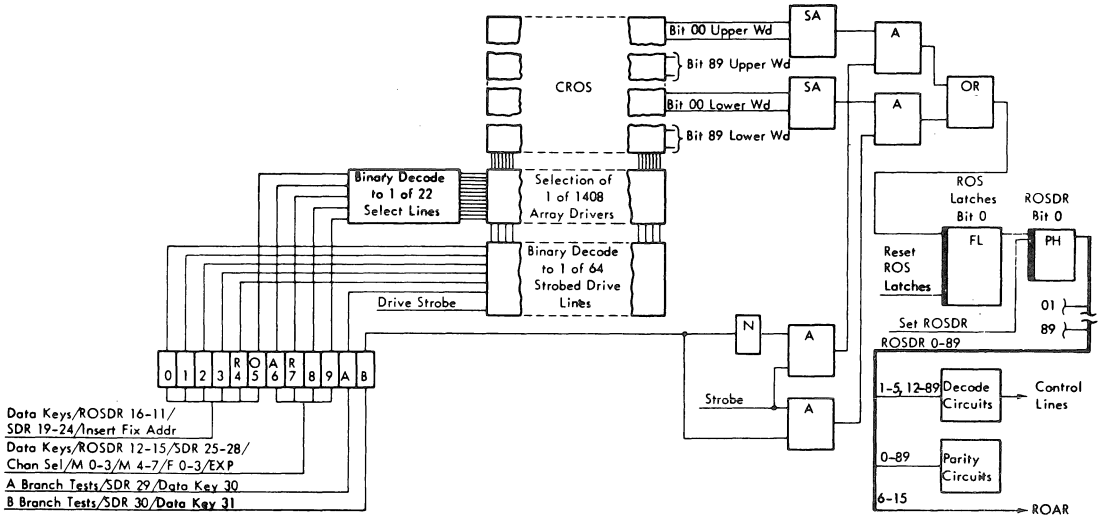


Figure 2-32. CROS Data Flow.

24. Read Only Storage Data Register

The ROS Data Registers store the CROS word for use during the machine cycle. The output of the data registers controls the decode circuits, parity check circuits, and the ROAR addressing circuits.

ROSDR is divided into two sets of registers, the ROSDR outgate registers which control the machine from 0 time of 1 cycle to 0 time of the next, and the ROSDR ingate circuits which control the machine from 130 time of one cycle to 130 time of the next. Figure 2-32 is a composite Data Flow Diagram of the CROS. For further information on this subject see the section on Capacitor Read Only Storage in this manual.

25. Read Direct Register

The Read Direct Register is set from another CE's Write Direct Register as a result of a RDD instruction. This register contains 8 bits plus a parity bit and its output is gated to the U input of the Mover. See Fig. 2-33.

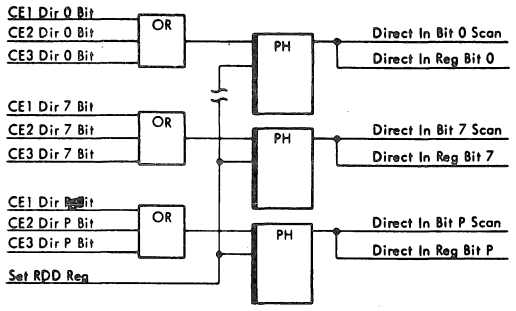


Figure 2-33. Typical Read Direct Register Positions.

26. Select Register

This register consists of 32 bits plus parity. Normally it contains the DAR mask used to mask off the element check, out of tolerance, and on battery interrupts stored in the diagnose accessible register.

During the SCON instruction, the DAR mask in the select register is replaced by the select mask. When SCON is completed, the DAR mask is again placed into the select register from local store location 00,0000.

The Select Register contents (DAR Mask) is made available to the programmer by use of Diagnose Kernal F17 and may be set by the use of Diagnose Kernal F16. For further explanation of these Kernals, see 9020 Principals of Operation Manual, CBB890.

Figures 2-34 and 2-35 are the Select Register Data Flow and a typical bit position logic diagram.

27. Write Direct Register

The Write Direct Register is set by the Write Direct Instruction; once set, this register's contents will remain the same until the next Write Direct Instruction is executed. The data input to this register is from bit

positions 24-31 of the H Register and the output of this register is to the drivers and thence to the bus to the other elements. Figure 2-36 is a typical bit position in the Write Direct Register.

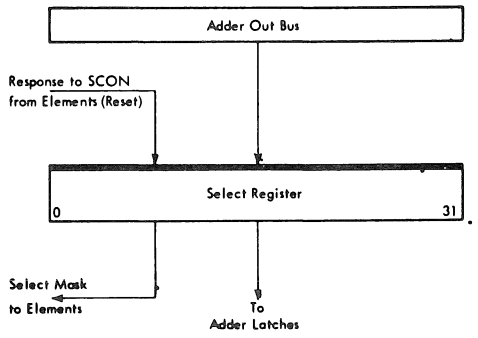


Figure 2-34. Select Register Data Flow and Gating.

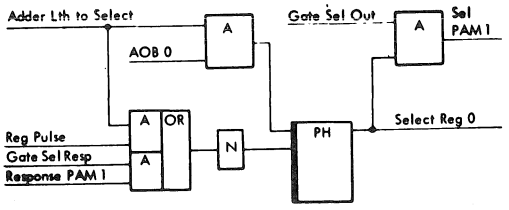


Figure 2-35. Typical Select Register Position.

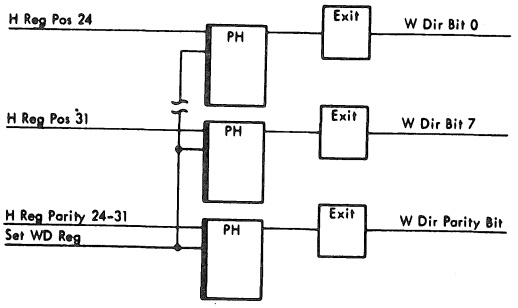


Figure 2-36. Typical Write Direct Positions.

28. Storage Address Register

The Storage Address Register as its name implies is an intermediate storage register for the address (logical) being sent to the SE. The address contained in this register is a result of the output of either the adder, or the IAR and will represent the logical address before either ATR or PSBA circuitry has translated it to a physical SE access. Figure 2-37 is the data flow diagram for the inputs to the SAR; however, Fig. 2-64. is a more complete data flow diagram of the actual storage address generation.

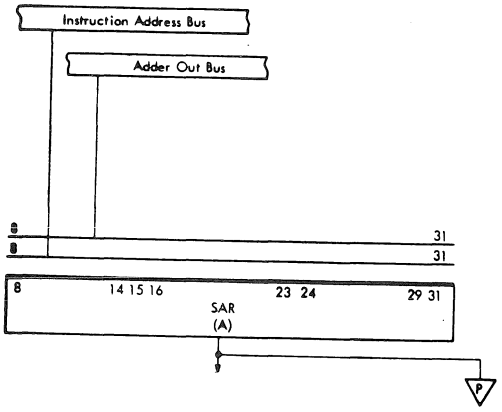


Figure 2-37. SAR Data Flow and Gating.

29. Storage Data Register

The Storage Data Register is a 32 bit interface buffer between the Compute Element and the Storage Elements. This buffer is active both on accesses to fetch data and on the store operations. Figure 2-38 shows the data flow for the SDR.

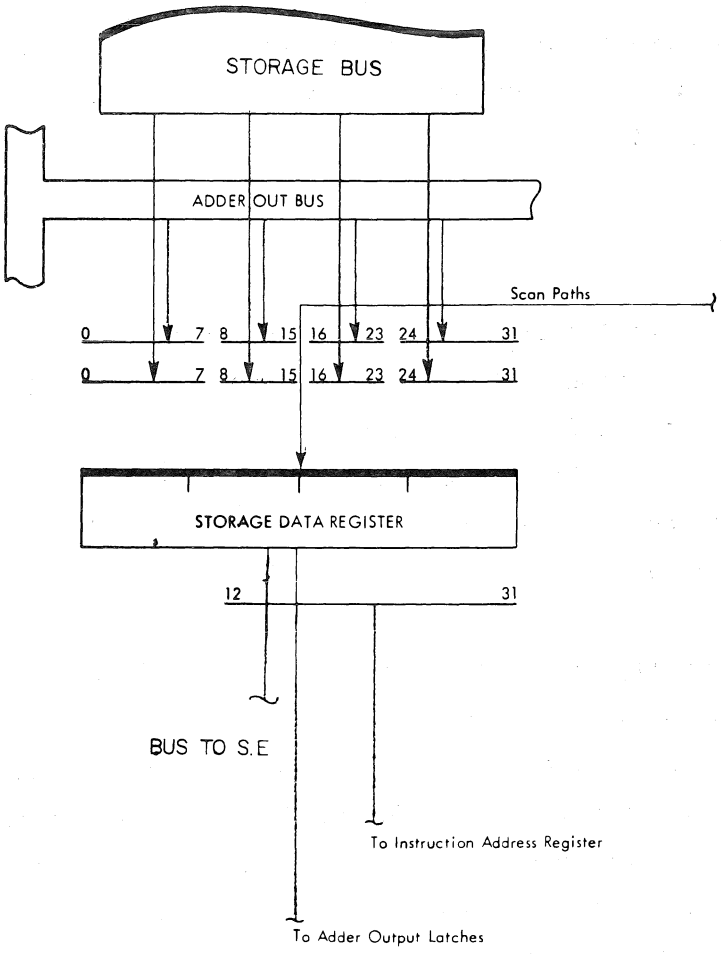


Figure 2-38. SDR Data Flow and Gating.

2-3. COMPUTING ELEMENT INTERNAL DATA PATHS

Within the Computing Element are six basic data paths capable of moving the instructions and/or data from one functional unit to another. These data paths include: the adder, shifter, mover, instruction address, local storage, main store in-out.

A. Adder

Figure 2-39 shows the basic path that data takes when it is processed through the adder. In a single 500-nanosecond cycle, two 32-bit numbers are gated into the XG and Y adder inputs and through the adder to set the output latches. With the sum available in the adder output latches, it can be gated into any of the operating registers at the very beginning of the following 500-nanosecond processing unit cycle.

More specifically, after taking a 500-nanosecond cycle to place one 32-bit number in an operating register, the add cycle begins at set register pulse time (000) by setting a second 32-bit number into another operating register and simultaneously opening the XG and Y gates into the adder. The numbers are combined and at about 375 time the sum is available at the adder output. Adder output latches are opened to pass information by the latch pulse at 375 time and "freeze" at 475 time to hold the adder sum through the end of the processing unit cycle so the next register set pulse can gate the sum back into an operating register.

Notice in Fig. 2-39 that the two inputs to the adder are labeled XG and Y. These symbols were chosen both for convenience in microprogramming symbology and to permit short line labels in the ALDs.

Notice also the ingates for the L and R Registers. Separate controls are assigned to the high-order bytes of these registers to permit floating-point numbers to be handled. In floating-point notation, the high-order byte

contains a binary exponent and the remaining 24 bits contain a fraction expressed in hexadecimal form.

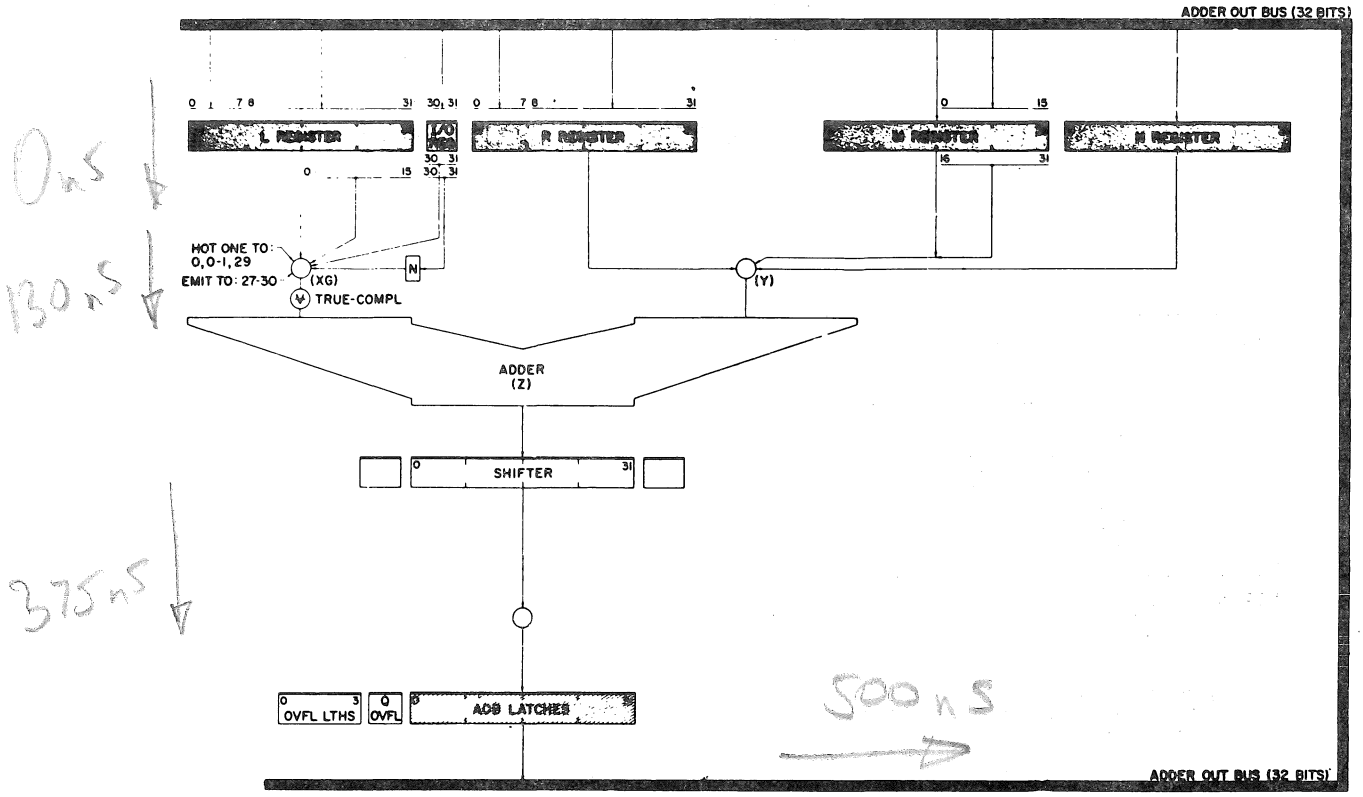


Figure 2-39. Adder Data Path.

B. Shifter

The shifter enables the adder outputs to be shifted left or right by either one bit or four bits before being gated into the adder output latches (Fig. 2-40). A group of four overflow latches accommodates the bit or bits shifted out of either the high- or low-order ends of the shifter. Bits entering the overflow latches may be spilled into the F Register while a bit entering the Q latch may be spilled into the Q Register, depending on the specific micro-order. Bits from the F or Q Register may be entered into AOB latch positions that may be left vacant by a shift.

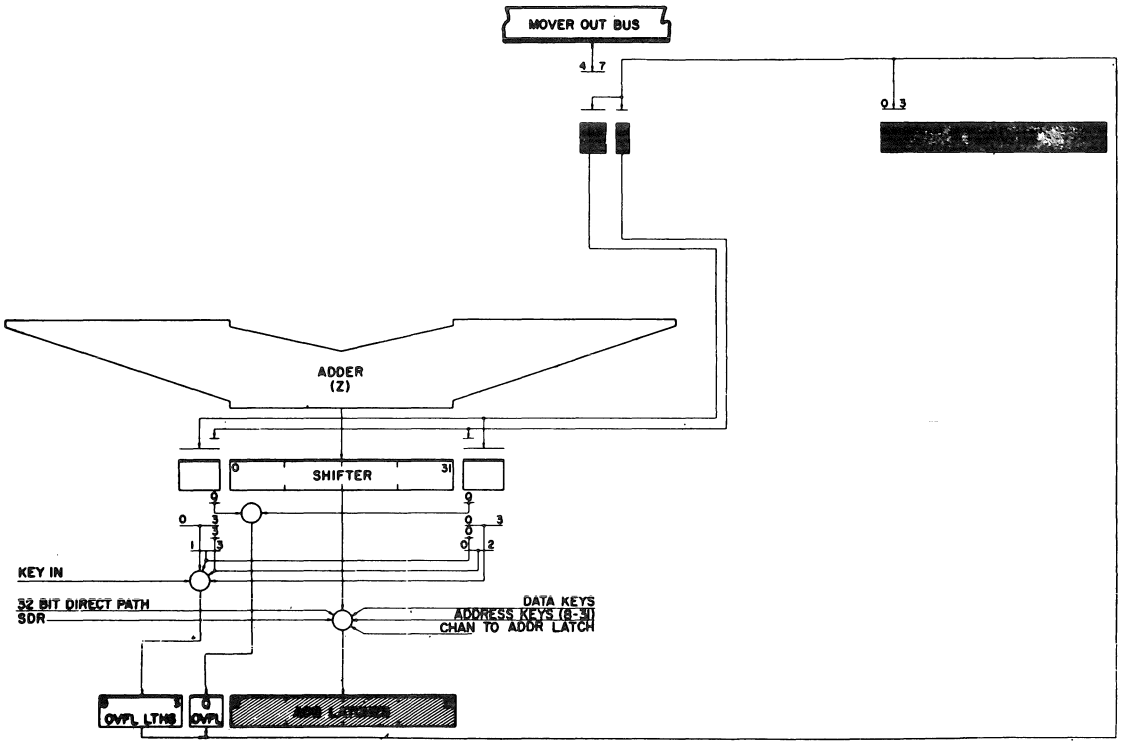


Figure 2-40. Shifter Data Path.

For a shift left of one, the adder outputs enter the shifter logic and are skewed left one place. The high-order adder output bit (position 0) is shifter left in either true or complement form into the low-order overflow latch position (position 3). The remaining overflow latch positions have bits from the F Register skewed into them with the high-order F Register bit lost. Either the Q Register bit or the bit in position zero of the F Register may be entered into position 31 of the AOB latches.

For a shift left of one, then, the only bit that may be lost is the bit in the high-order position of the F Register.

Information in the overflow latches may be immediately spilled to the F Register or into the Q Register, again depending on the micro-order. Bits

may spill to and enter from either the F or the Q Registers during the same cycle. The low-order position of the shifter may be zero inserted.

The shift right of one is similar to the shift left of one. Adder outputs enter the shifter logic and are skewed right one place. The low-order adder output bit (position 31) shifts into the high-order overflow latch position (position 0). The remaining overflow latch positions have bits from the F Register skewed into them. For a shift right of one, then, the only bit lost is the bit in the low-order position of the F Register. Either the Q Register bit or the bit in position three of the F Register may be entered into position zero of the AOB latches.

Information in the overflow latches may be immediately spilled to the F or Q Register, depending on the micro-order. Bits may spill to and enter from either the F or the Q Registers during the same cycle. The high-order position of the shifter may be zero inserted.

For a shift left of four, the adder outputs enter the shifter logic and are skewed to the left four places. The four high-order adder output positions are gated into the overflow latches. Data in the overflow latches may be immediately spilled to the F Register. In the same cycle, depending on the specific micro-order, the four low-order bits of the shifter may have:

1. The contents of the F Register entered.
2. The contents of the emit field entered.
3. Zeros inserted.

A shift left four for floating-point op codes does not shift position 0-7. Only bits 8-31 are shifted and bits 8-11 are lost.

The shift right of four is similar to the shift left of four. The adder outputs enter the shifter logic and are skewed right four places. The four low-order adder output positions are gated into the overflow latches. Information in the overflow latches may be immediately spilled to either the

F Register or positions 0-3 of the H Register. In the same cycle, depending on the specific micro-order, the four high-order shifted bits of the shifter may have:

1. The contents of the F Register entered.
2. The number 0001 entered.
3. Zeros inserted.

A shift right four for floating-point op codes does not shift positions 0-7. Only bits 8-31 are shifted and bits 28-31 are lost.

C. Mover

The mover is a functional unit that manipulates one byte block of data in half-byte increments. Provided with two inputs (U and V), each one byte wide, the mover is able to:

1. Logically AND inputs U and V together to form a new byte.
2. Logically OR inputs U and V together to form a new byte.
3. Exclusive OR the inputs together to form a new byte.
4. Select any two half-bytes available at inputs U and V to form a new byte.
5. Select any half-byte from eitherinput and select the half-byte available from the emit field to form a new byte.

Figure 2-41 shows the basic path data takes when it is processed through the mover. In a single 500-nanosecond processing unit cycle, two 8-bit bytes of data are gated into the U and V mover inputs, the mover function is accomplished, and the new data is gated back into a register at the very beginning of the next cycle.

More specifically, U and V in-gates are opened at set register pulse time (000) of the processing unit cycle and the bytes enter the mover to be acted

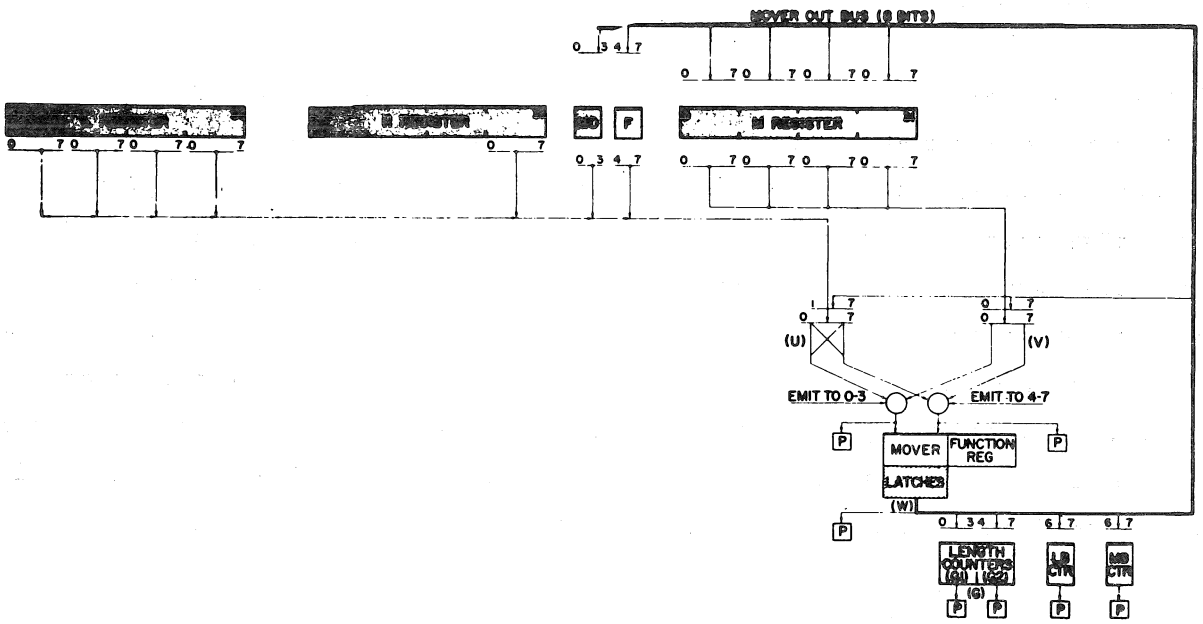


Figure 2-41. Mover Data Path.

upon. At latch pulse time (375), the new byte is set into the mover latches where it is held until latch pulse time of the following cycle.

Mover U input bytes can come from the L, R, MD, or F Registers while mover V inputs can come only from the M Register. Mover outputs can go to either the L, M, MD, or F Register and the L byte, M byte, and Length (G1 and G2) counters.

To control the data flow and keep track of the bytes being moved from registers that are more than one byte wide, two 2-bit counters, the L and M byte counters, are used. For fields more than one word wide, such as the fields in variable field length instructions, the length counters (G1 and G2) keep track of the bytes being processed.

D. Instruction Address Data Path

Figure 2-42 shows the basic data paths open to the instruction address. Note that in addition to the primary path to the storage address register, a path exists for the instruction address to be updated. Normally, the instruction address is gated out of the instruction address register (IAR) and into the instruction address counter (IA counter) where it is updated by either two or four. At the beginning of the next processing unit instruction cycle, the updated address is gated from the IAR counter latches to both the storage address register and back to the IAR. Not only can the next instruction then be fetched from storage, but the IAR will hold the instruction address until it is updated just prior to the next instruction cycle.

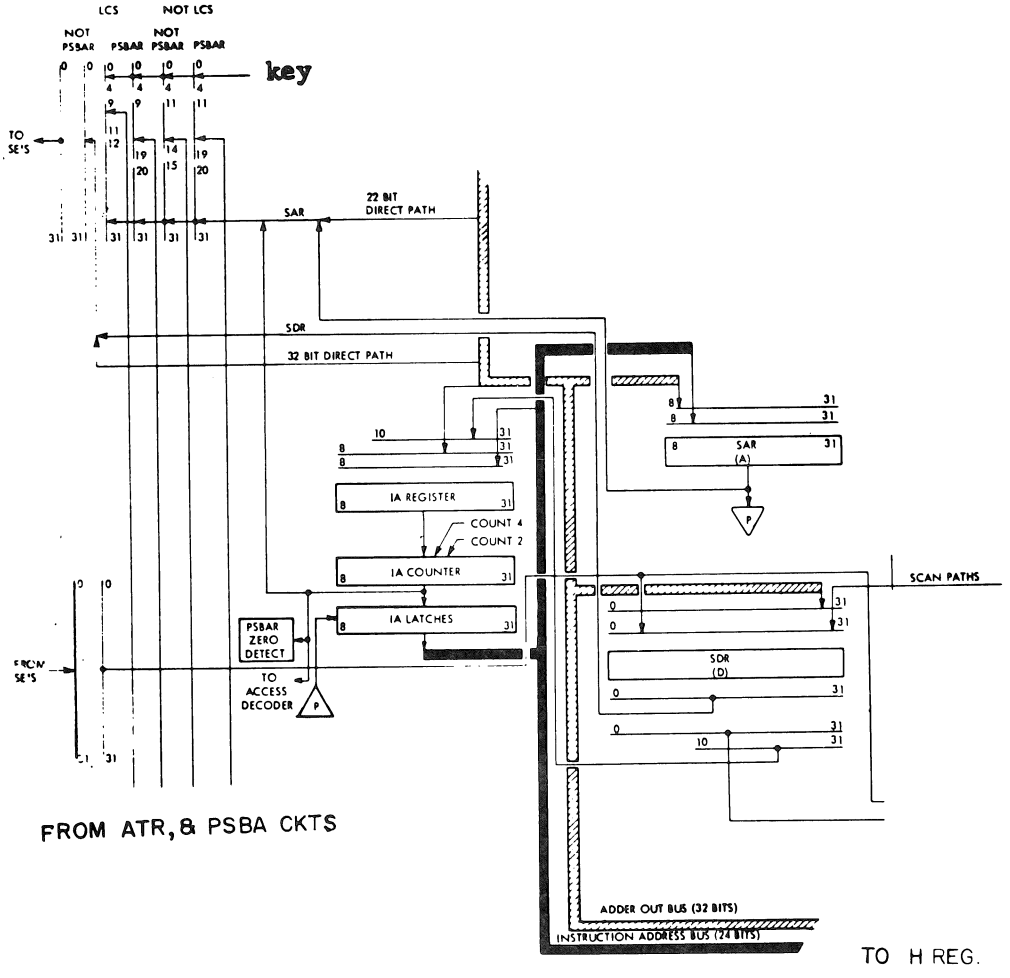


Figure 2-42. Instruction Address Data Path.

When the processing unit executes an instruction out-of-sequence, such as when a branch or an interruption occurs, the IAR is set from the adder out bus. Also, when an interrupt occurs, a path from the IA counter to the H Register allows the existing instruction address to be stored for later use.

To assist in checking system operation with fault locating tests, a data path from bits 8-31 of the storage data register to the IAR is available.

For FLTs, storage words 32 and 33 (addresses 128 and 132) are reserved to serve as working registers. The system can insert these two addresses into the IAR (Hdw Adr into bits 24 and 29).

E. Local Store Data Path

Figure 2-43 shows the basic path data takes when local storage supplies a word to the processing unit. Because the L and R Registers are used as local storage data registers (buffers), the local storage cycle must start early enough to have its word available to the L and R Registers at register set pulse time (the beginning of a processing unit cycle). Halfway through a processing unit cycle, then, local storage starts its cycle so that the read portion is completed by register set pulse time. The data word gates into either the L or the R Register where it is now available to the processing unit.

Note the regen path from either the L or the R Register back to the local storage. Because local storage effectively has two data registers, it is possible for data to be gated out to one register and for the contents of the other register to be gated back into local storage in the same cycle.

Another regen path is available directly from the local storage sense latches to preserve valid data in the event of an error. If an error occurs, the data in the L or R Register may not be valid. In this case, the data in the local storage sense latches is gated directly back into local storage at set register pulse time.

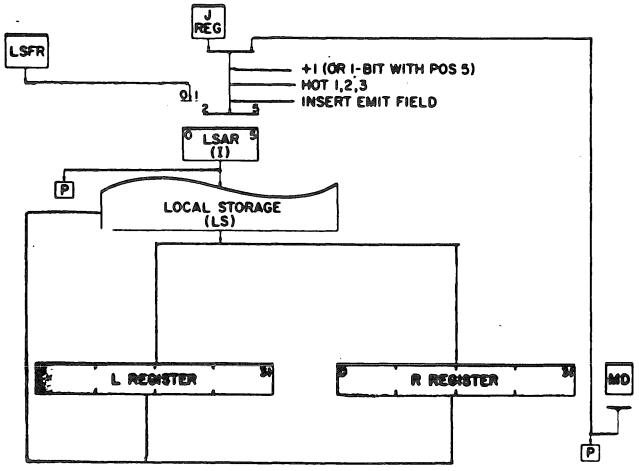


Figure 2-43. Local Store Data Path.

Addresses for the Local Storage Address Register (LSAR) are six bits wide. The two high-order bits determine which sector of local storage is to be used, and the four remaining bits specify which of the sixteen words within the sector is desired.

The two high-order bits are set into the Local Storage Function Register (LSFR) from the microprogram word before they gate into LSAR. The four remaining bits come from either the emit field, the mover out bus (0-3), the adder out bus (12-15) via the J Register, or the MD Register. Notice the provision for ORing a one-bit into the units position of the LSAR. This OR'ing one-bit provides an easy way to automatically address the second word of a floating-point double precision operation.

F. Main Storage In-Out Data Path

Figure 2-44 shows the basic path data takes in order to enter or to leave main storage. Before starting to move data in or out of storage, however, remember that the CPU clock cycle is 500-nanoseconds and the main storage clock cycle is 2.5 microseconds. Remember also that each time storage is cycled it both reads out to the Storage Data Register (SDR) and writes back into the same address from SDR. The only difference, then, between a storage read or a storage write cycle is deciding whether to change the data in SDR between the read half and the write half of the storage cycle.

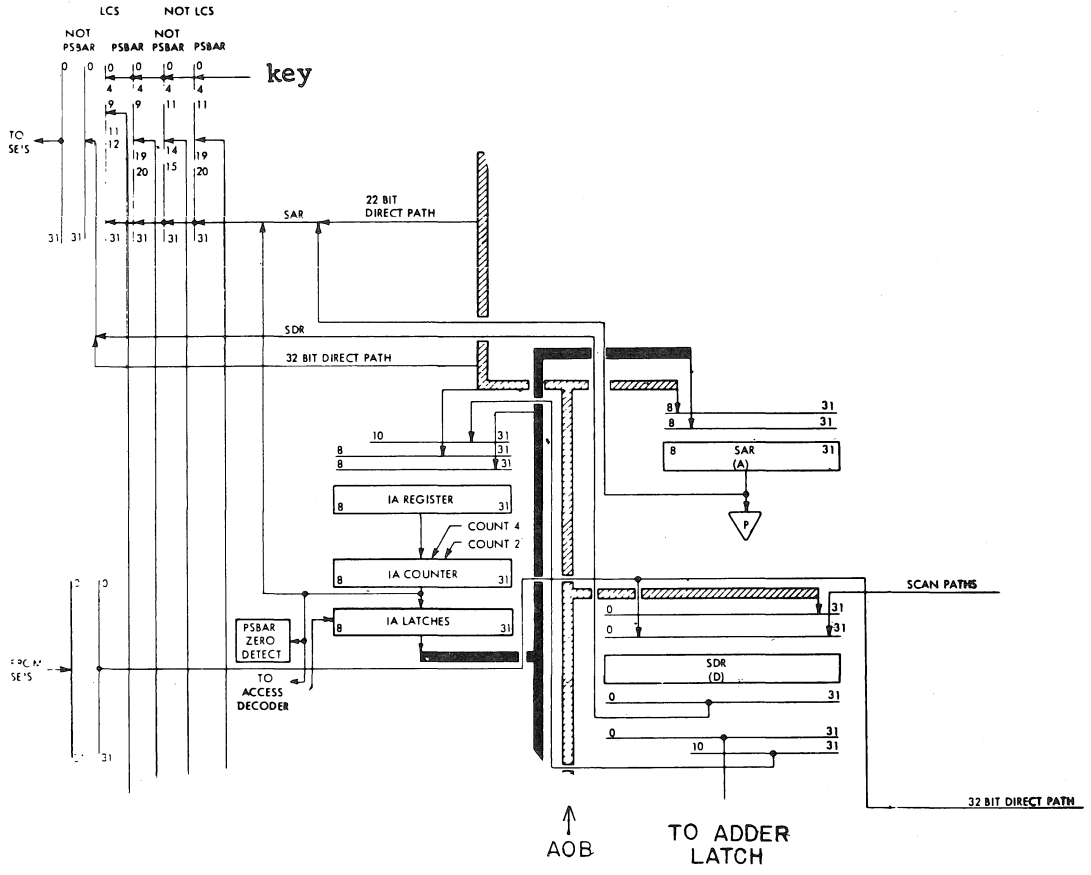


Figure 2-44. Main Store Data Path.

To move data from storage to CPU, an address is set into the Storage Address Register (SAR) at set register pulse time (the beginning of a CPU cycle) and the storage delay line clock starts. Nearly a microsecond later, the data addressed from storage is set into SDR where it can be gated into the AOB latches before the third CPU cycle for use by the CPU. An additional path for bits 8-31 of the SDR goes to the Instruction Address Register for fault locating test branching purposes.

Data is moved into storage by gating the CPU data in the AOB latches into SDR at set register pulse time of the third CPU cycle, or before. Note that data from the AOB latches is gated into SDR by four separate ingates. This effectively allows data to be stored on a byte basis (per byte stats) even though main storage handles data by the word.

Addresses for main storage are normally set into SAR from either the instruction address bus or the adder out bus, depending on whether the information desired is a new instruction or data for an instruction being executed.

2-4. COMPUTING ELEMENT INTERNAL CONTROL

Capacitor Read Only Storage (CROS) is the storage device that contains the IBM System/360 Model 9020 microprogram. The microprogram is stored in 2816 words of 90 bits. Each 90-bit word enables the gates and control lines of the system or functional unit for one 500 ns machine cycle; gating for each functional unit is controlled by the decode of the bit combination within a field read out of CROS. For example, 001 in bit positions 65-67 of the CROS word gates the R Register to the right side of the adder input. (Refer to Data Flow Diagram.)

The storage media for CROS plane is composed of two printed circuit sheets; one etched with pairs of straight sense lines, and the other etched with drive and balance line pairs, having tabs in areas where a capacitor is required. These sheets are separated by a thin dielectric sheet. The sense

line plate is a permanent part of the array. The bit plate is removable and may be changed to modify the information contained in the CROS unit.

The bit pattern of a CROS word is determined by the presence or absence of capacitors within the hardware. A microprogram word from CROS cannot be altered by the external program. However, the Engineer or Technician may change the information in the CROS words by ordering specifically designed bit planes custom tailored to suit his needs. These will modify the operation of the functional units of the Computing Element. By implementation of CROS in the computer design, the computer flexibility is increased by a factor not previously available in control hardware. This flexibility allows making control circuit changes for a special features relatively easy (replacing printed bit plates in CROS).

As stated previously CROS is a read only storage, i.e., the read-out is non-destructive. Therefore, the designed microprogram remains until it is changed by replacement of bit sheet or is physically damaged.

Figure 2-45 shows the relationship of CROS to system clock and control lines. Only the clock can operate independently of the microprogram words from CROS. Note, that the element control lines are controlled by a decode of the CROS word. The Read Only Storage Data Register (ROSDR) stores the sense amplifier outputs from CROS when the word is read out. ROSDR holds this CROS word available to the decode circuits for one machine cycle. The address selection of the CROS word is under control of the Read Only Address Register (ROAR) which in turn is fed by fields of the ROSDR.

A. Physical Construction

Capacitor Read Only Storage uses a capacitor between drive and sense lines to represent a bit of information. Figure 2-46 shows a simplified drawing representing storage matrix. Only one driver at a time may be active. If driver 1 is made active, the voltage shift of the drive line is capacity coupled to the A-sense line. The sense amplifier amplifies the voltage shift and produces

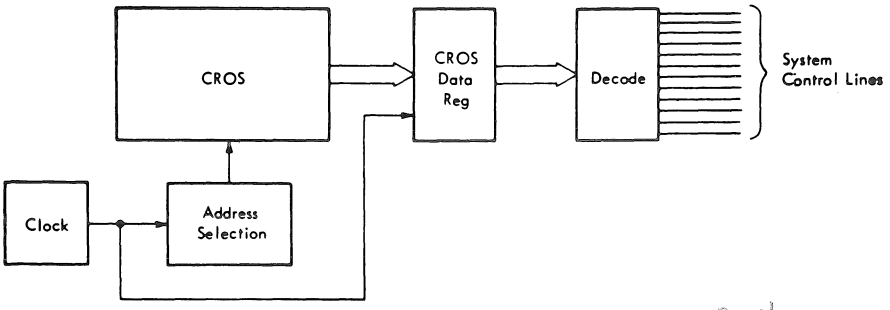


Figure 2-45. CROS Data Flow.

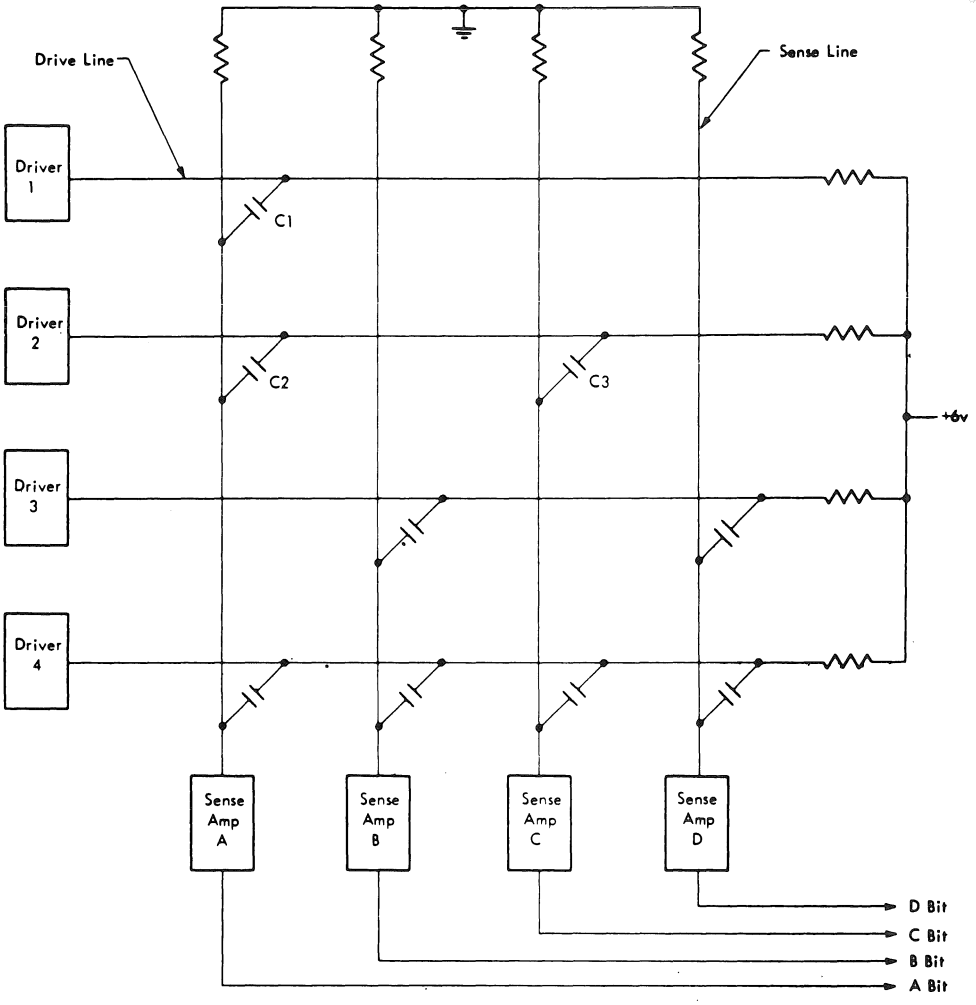


Figure 2-46. Basic Capacitor Matrix.

an A-bit output. If driver 3 is made active, the drive line voltage shift is capacity-coupled to the B and D sense lines, producing a B-bit and a D-bit output. From this example one can see that any specific bit combination could be designed into the matrix with the appropriate placement of coupling capacitors.

An extra line, called a balance line, is added for each drive line. The balance line is not connected to a driver, instead it is connected to the drive line voltage source at one end and allowed to float at the other end. Thus, each sense line has the same capacitive load regardless of the bit configuration (determined by the placement of coupling capacitors). (See Fig. 2-47).

The CROS matrix is placed on what is referred to as CROS plane. There are 16 CROS planes with 88 doublewords per plane for a total of 2,816 (90-bit) words. The 16 planes are held on Gates C and D. Planes 0-7 are on Gate C and 8-15 are on Gate D. (Refer to Fig. 2-48.)

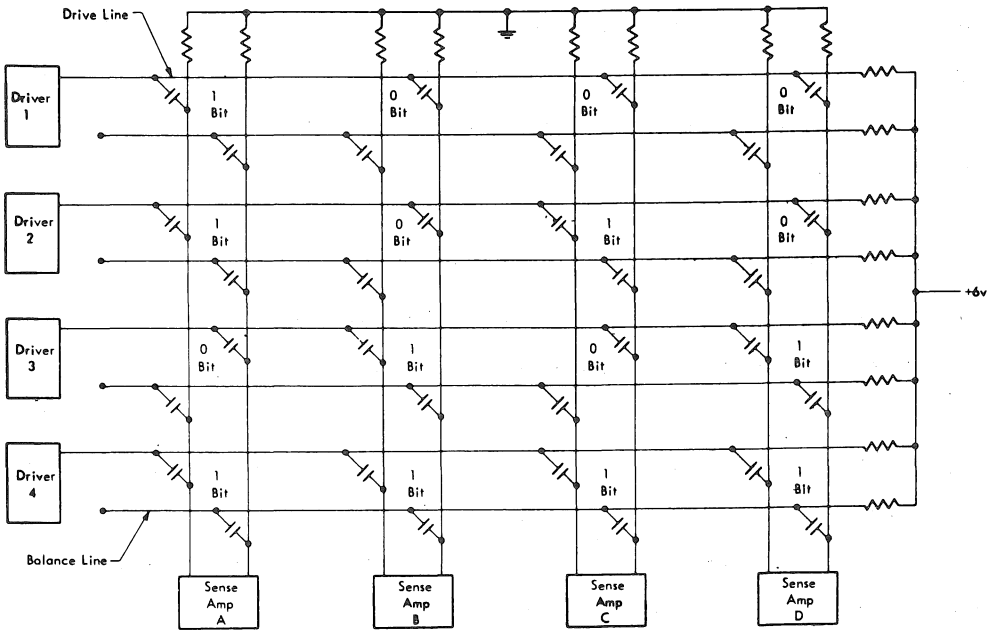


Figure 2-47. Basic 4 x 4 CROS Matrix.

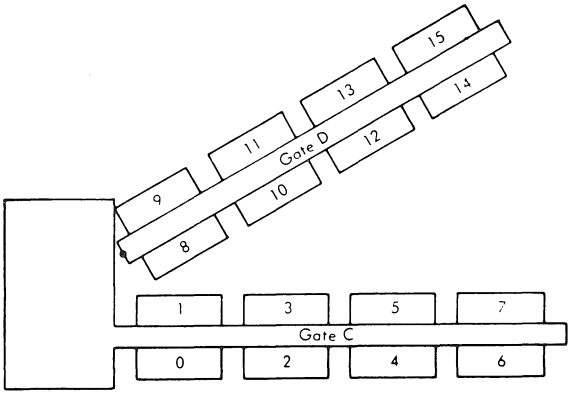


Figure 2-48. CROS Plane Locations - Top View.

The drive and balance lines are photo-etched from a sheet of copper that is bonded to epoxy glass (Fig. 2-49). The resulting epoxy sheet with copper drive and balance lines is called a bit plate. A separate bit plate controls the bit configuration for each CROS plane.

Tabs at the top and bottom of the bit plate are used for electrical connections to the drive and balance lines. The top tabs connect the drive and balance lines to terminating resistors. The bottom tabs connect the drive lines to the driver circuits.

The four holes in the bit plate are used to align the bit plate within the plane. Two holes snap over locating studs in the plane, while the other two holes provide clearance for the center mounting studs.

The bit capacitors are formed by sandwiching a sheet of Mylar between the bit plate and sense lines (Fig. 2-50). Pressure plates hold these pieces firmly together. The Mylar is the dielectric, while the drive, balance, and sense lines become the plates of the capacitors.

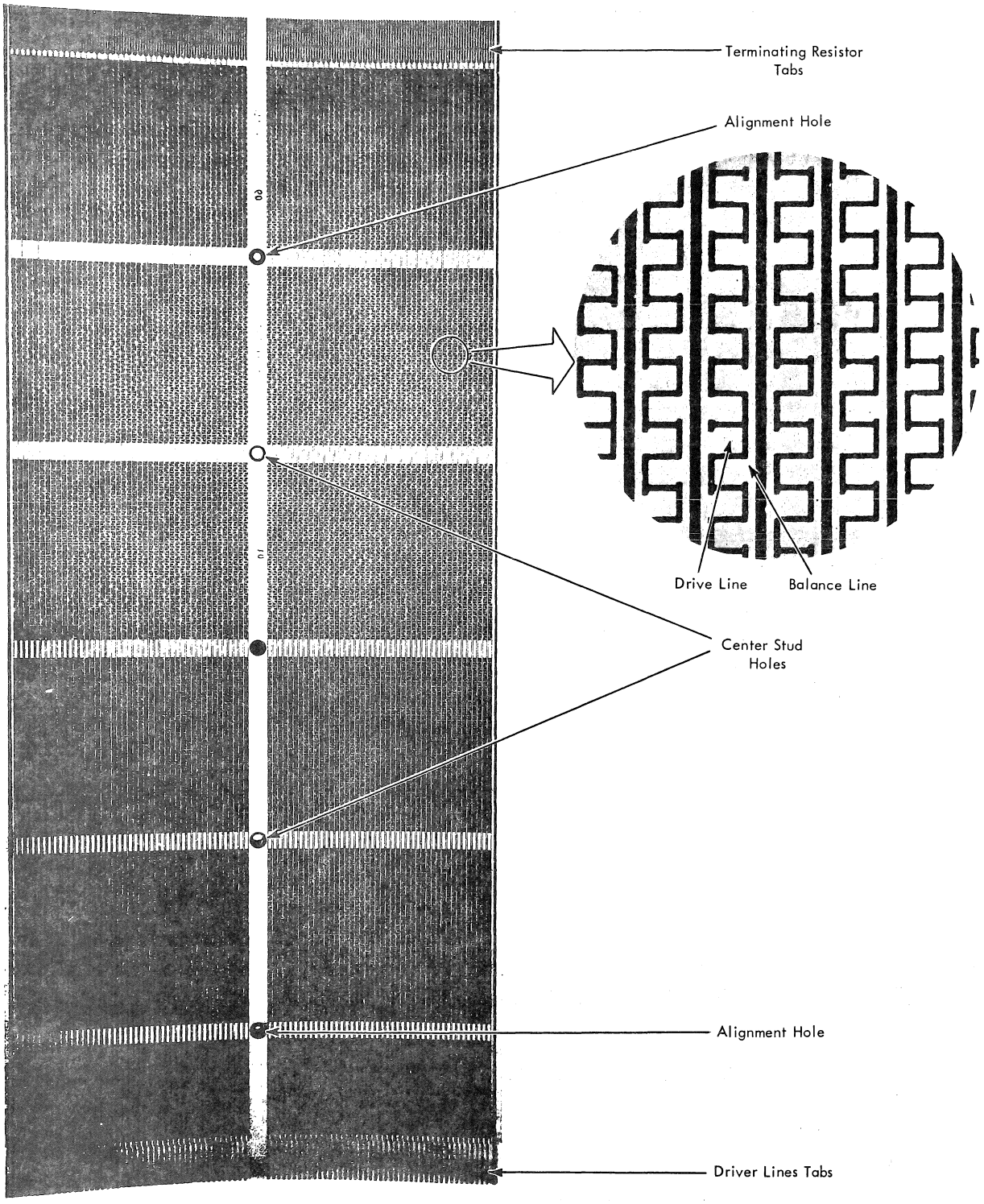
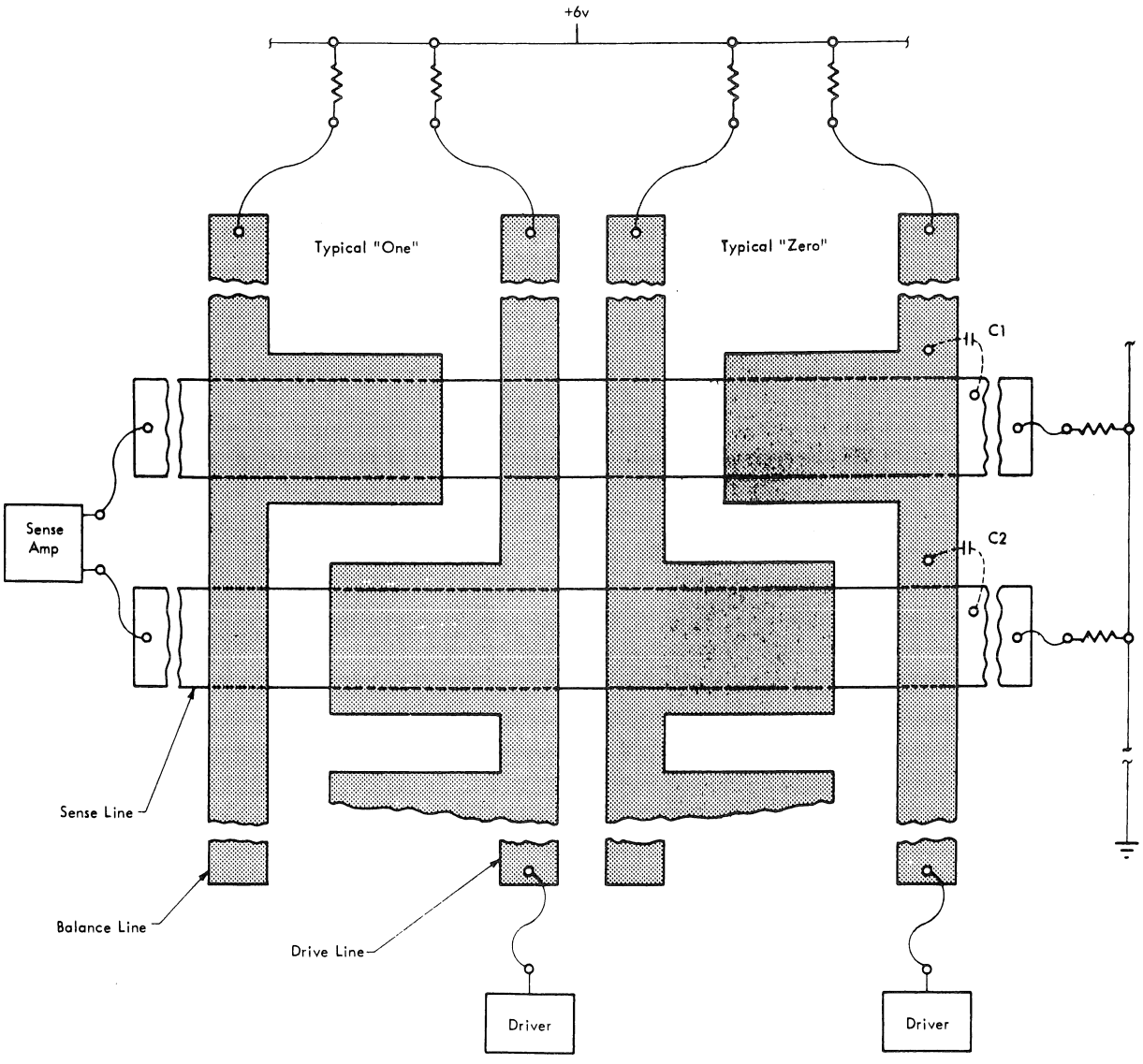


Figure 2-49. Bit Plate.



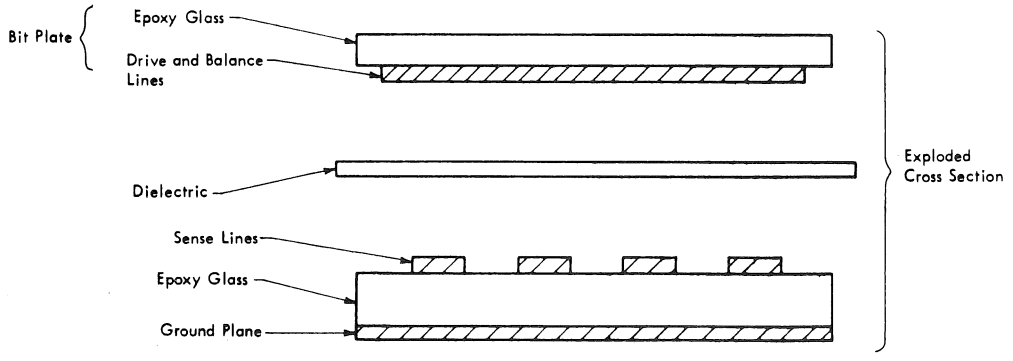


Figure 2-50. Bit Capacitors.

B. Theory of Operation

A CROS word is read out and stored in ROSDR every machine cycle. This CROS word, the microprogram word, controls the processing unit's gates and control lines during the machine cycle that the word is stored in ROSDR. The address of the next microprogram word is gated into ROAR from ROSDR, or data flow paths under ROSDR control, or from fixed address insertion circuits.

A series of microprogram words cause the system to perform a specific routine. When the machine is manufactured, a microprogrammer specifies which bits each microprogram word must contain to make the routines work. The microprogrammer's routines are used to make the CROS bit plates and the CAS logic diagrams.

A microprogram word is one CROS word. To control the system, the microprogram word must be read into ROSDR.

The microprogram word is divided into control fields. The control fields are used to address the next CROS word and to control the system's gates and control lines.

1. Control Fields

The control fields and their functions are shown in Fig. 2-51. The bit combination within a control field is decoded into a micro-order. Only one micro-order is possible from a control field for any one microprogram word. However, one micro-order can control a number of control lines and gates.

2. Micro-Orders

A micro-order represents a specific bit combination within a control field. The microprogrammer writes the microprogram routines by specifying the micro-orders for each microprogram word. The CAS logic diagram is a listing of the micro-orders specified by the microprogrammer for each microprogram word.

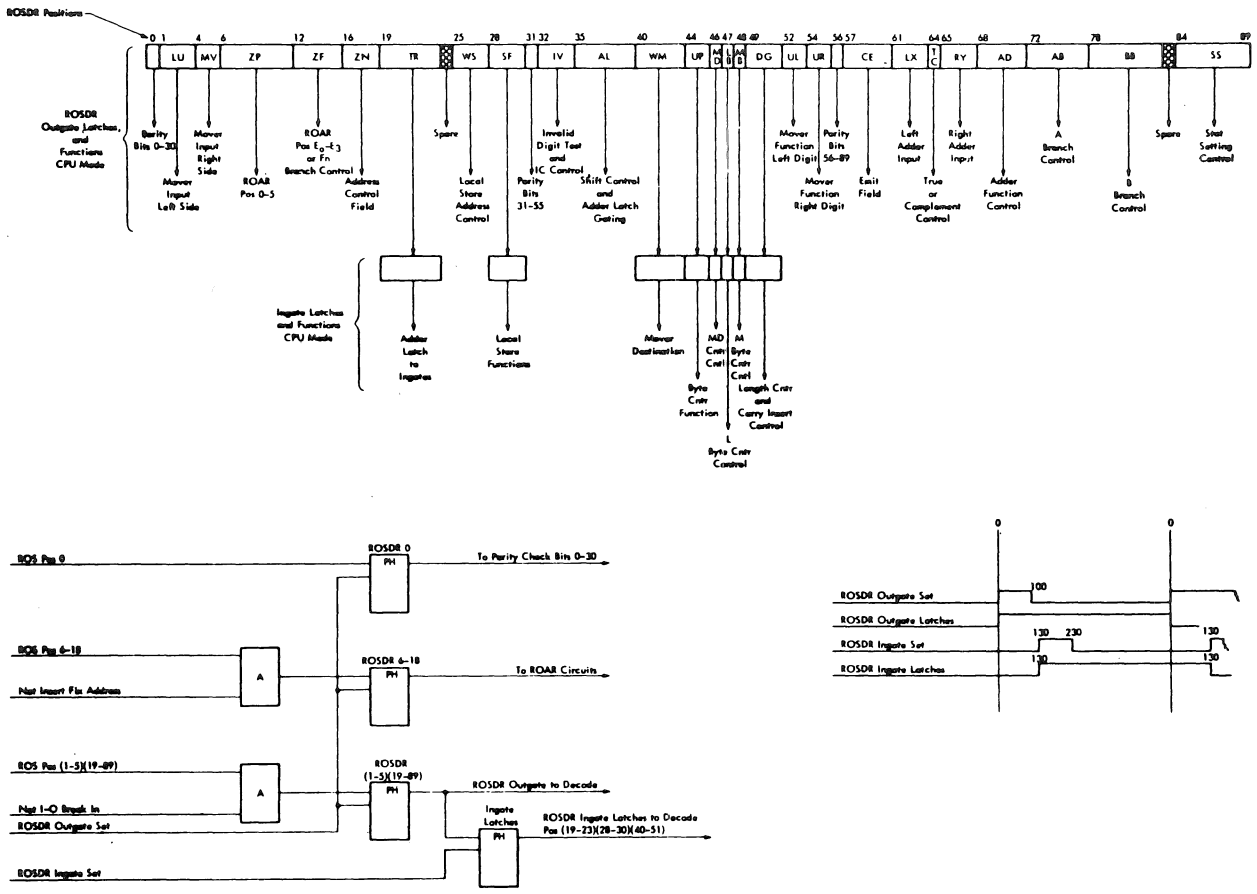


Figure 2-51. Decoding of Microprogram Word into Control Fields.

3. CAS Logic Diagrams (CLDs)

The CAS diagrams are control automation system diagrams that document the microprogram routines. Each block on the CAS diagrams represents one microprogram word. The micro-orders that were specified by the microprogrammer are shown in the CAS block. Control fields that have no micro-order specified by the microprogrammer are automatically set to a predetermined bit configuration when the bit plate is manufactured. These automatically inserted bits usually represent a no-operation condition for the control field. However, some control fields are set to a pertinent micro-order when no other micro-order has been specified. These control fields are shown in Fig. 2-51.

The CAS used in the 9020 System group pertinent micro-orders (fields) to form symbolic control words. These words in conjunction with the edge character define the operations to be performed as explained in the example given. Figure 2-52 defines the edge characters and appropriate functional units, and also set forth the special characters which are used.

Figure 2-53 is a CAS word in the 9020 format with the explanations keyed to the edge characters.

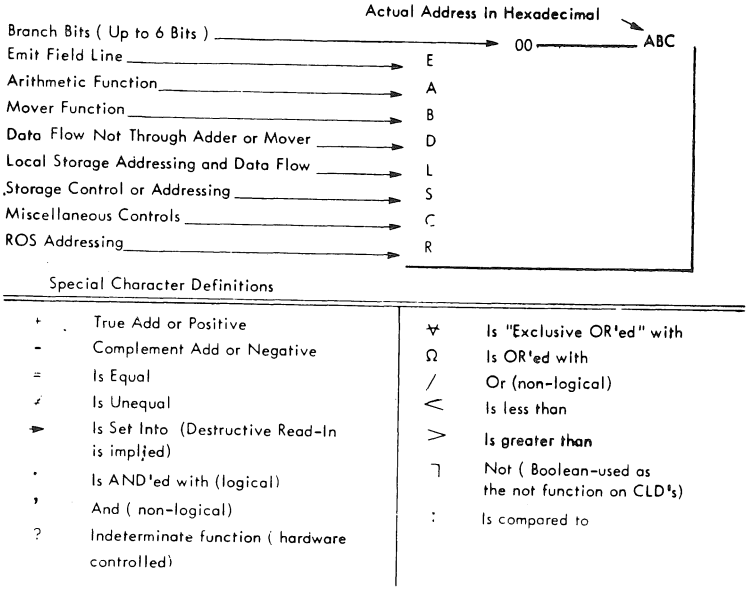


Figure 2-52. CAS Diagram Block.

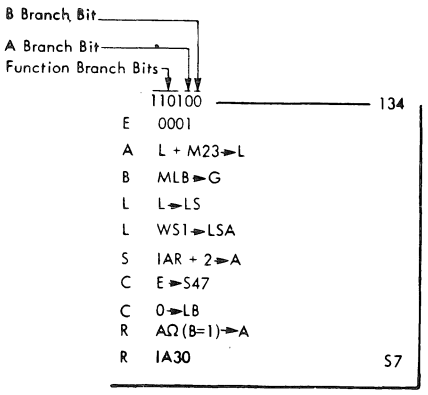


Figure 2-53. CAS Word in 9020 Format.

The top line of the CAS block on the left side is the ROS branch bit setting; this may be up to 6 bits in length and may include the function branch bits as well as the A branch bit and the B branch bit. (Normally only the A and B bits are used.) The right side of this top line is the actual ROS address of this block expressed as three hex digits.

The E line is the emit field of the micro-instruction and is taken from the CE field of the 90-bit word.

The A line implies that an arithmetic function is to take place (in this case the adder is to be used) to take the contents of the L Register and add it to bits 16-31 (bytes 2 and 3) of the M Register and place the result back into the L Register.

The B line indicates that a mover function is used. In the case presented the byte of the M Register specified by the LB counter is placed via the mover into the G counters.

The L edge character specifies the Local Storage addressing and data flow. In the example we combine the two L lines and determine that the new contents of the L Register are to be placed into an area of local store called working store 1. The S edge character is used for storage (main) addressing. In the

example the micro-instruction is to update the IAR by two and take the updated result to the SAR and initiate a storage request. (Any time an address is placed in the SAR a storage access is initiated.

The C edge character is the miscellaneous controls (usually direct control). In the example there are two independent actions to take place; first, the emit field is to be set into the general purpose stats 4-7; second, the LB counter is to be set to zero (after it is used in the M Register selection).

The R edge character defines the ROS address for the NEXT ROS address. The two R lines taken together indicate that if the IAR bit 30 is a 1 OR the general purpose stat #7 is a 1 the A branch bit in the next ROS address will be a one. If the general purpose stat #7 is a 1 (before the emit field is set in), then the B branch bit will also be a one. The result of these micro-orders is that instead of four possible branches from this block (00, 01, 10, 11) only three are valid since any time the B bit is set, the A bit will also be set.

The CAS micro-instructions are grouped into microroutines which are designed to perform specific functions. These microroutines are further grouped into the microprogram.

4. Example Routines Showing Part of the CROS Microprogram

A couple of example routines which are included in the microprogram of CROS are what is referred to as the First Level I-Fetch and the Second Level I-Fetch. These routines are called up to execute the instruction set in a particular external program to be executed.

In fetching and executing a particular instruction, the ROS routine is in control. For example, in the First Level I-Fetch routine, the first word of the instruction is fetched and examined to determine format. Upon detection of the format, the routine either updates the IAR for either the next instruction or for the remaining portions of the present instruction under execution

if it is of the SS format (1 1/2 words), or for the other half of an instruction if it is of the RX, RS, or SI format and the starting address in IAR was on odd half word bounds. The routine determines this format from the first op code digit (bits 0-3) of the instruction.

In the Second Level I-Fetch the particular format instruction is decoded to determine what operation is called for by this instruction. This routine determines the operation by examining and branching on the second digit of the op code of the particular instruction.

The discussion above gives a general description of two routines. These particular routines will be discussed later in detail after the study of the CE is complete.

2-5. COMPUTING ELEMENT INTERRUPT SCHEME

The interruption system permits the Computing Element (CE) to change the program flow state as a result of conditions arising outside the system in input/output (I/O) operations or in the CE itself. The five classes of these conditions are:

1. Input/Output Interruptions
2. Program Interruptions
3. Supervisory Call Interruptions
4. External Interruptions
5. Machine-Check Interruptions

A. The Input/Output Interrupt

The I/O interruption provides a means by which the CE responds to signals from I/O devices. A request for an I/O interruption may occur at any time, and more than one request may occur at the same time. The requests are preserved in the IOCE until accepted by the CE. Priority is established among requests so that only one interruption request is processed at a time.

To demonstrate the use of the I/O interrupt, assume that a subsystem is in operation with CE, IOCE, SE, and an input/output device. The program being executed by the CE requires an I/O operation. Therefore, the CE issues a Start I/O command to the IOCE which in turn initiates the I/O operation. Once the IOCE indicates it has accepted the I/O command the CE is released to continue with the program it was in the process of executing. In order for the CE to determine whether the I/O device has completed the job properly it must in some way be notified that the operation was completed properly or was terminated for some reason such as a malfunction. This is accomplished by the I/O interrupt scheme. When the I/O operation is completed or terminated, the status of the I/O device is stored in the CSW location of the PSA area and the IOCE notifies the CE by requesting an I/O interrupt. This I/O interrupt if masked properly causes a PSW swap in the CE executing the program. The PSW swap allows the programmer to have a compiled program routine which is addressed by the new PSW. This routine will be designed by the programmer to examine the status of the device which was used in the I/O operation by evaluation of the status stored in the CSW. By examining this status the compiled program routine can determine whether the I/O operation it originally stated has been completed properly or if it was terminated due to a malfunction. If upon examining the status it is determined by this program routine, that the job was in fact completed properly it could then branch back to the original program it was executing and possibly issue another Start I/O to the device via the IOCE. If the job had been terminated due to a malfunction, the compiled routine might examine the I/O malfunction in more detail by issuing a sense command. This command subsequently returns more data which can be examined and the malfunction analyzed in greater detail.

B. The Program Interrupt

The program interrupt is provided and is responsive to programming errors made on the part of the programmer, which could be in the form of improper boundaries assigned to instructions or the compilation of improper instructions for the particular operation. This interrupt could be used purposely by the programmer in particular situations to branch to specific routines by

the subsequent PSW swap. Therefore, the program interruption scheme is used as a safety factor concerning the program compiled by the programmer. In this system design the burden for successful, efficient operation is placed on the software; thereby, allowing versatility in the use of the computer for many different tasks. The interrupts occur as a result of improper specification or use of instructions and data by the programmer contingent on the proper masking of the program interrupt mask in the PSW.

The program interrupt is divided into specific classifications depending on the error committed by the programmer. These classifications are:

1. Operation Exception - This occurs when the Op Code is not a proper or assigned Op Code in the instruction set.
2. Privileged-Operation Exception - This occurs when what is referred to as a privileged instruction, is executed with the computing element in the problem state. An example would be an attempt to execute a Set ATR instruction with the CE in the problem state. This type of instruction can only be executed when the CE is in the supervisory mode or in other words is providing system or subsystem control.
3. Execute Exception - This occurs when the subject instruction of execute is another execute instruction.
4. Protection Exception - This occurs when the storage key of an accessed location does not match the protection key in the PSW.
5. Addressing Exception - This occurs when an address specifies any part of data, instruction, or control word outside the available storage assigned by the storage address translator for a particular CE or IOCE.
6. Specification Exception - This occurs when the programmer violates specific rules which must be complied with in order to have proper execution of the program, e.g., such things as violation of boundary conditions for particular instructions, call out of an invalid register for a specific operations.

7. Data Exception - This occurs when the sign or digit codes of operands in decimal arithmetic or editing operations, or in convert to binary are incorrect.

8. Arithmetic Exceptions - This occurs when the arithmetic operations exceed the expected limits of the programmer or the computing element. This includes Decimal-Divide Exception, Decimal-Overflow, Exponent-Overflow, Exponent Underflow, Significance Exception, Floating-Point Divide Exception, Fixed-Point Overflow, and Fixed-Point Divide Exception. It should be pointed out that the above expression Arithmetic Exception is not an exception itself, but is used to group a number of related exceptions. There are several in this group that can be masked such that they do not cause an interrupt by a particular setting of the mask bits in the PSWs.

9. Preferential-Storage PSA Area Lockout Exception - This occurs when an IOCE fails to gain access to the preferential storage area on a CAW fetch, on an I/O interruption, on a CSW store pertaining to an I/O instruction, or on a store during a logout operation.

10. SE Stopped Exception - This occurs when a CE attempts to gain access to a storage element which is in logout-stop status.

C. The Supervisor-Call Interruption

The supervisor-call interrupt is a result of executing a specific instruction (Supervisor-Call) available to the programmer to induce an interrupt in the normal sequence of executing instructions. The interrupt is generally used by the programmer to change the status of the computing element from supervisory mode to the problem mode or vice versa. However, it could be and is used for any branch routine that the programmer desires.

D. The External Interruption

The external interruption provides a means by which the CE responds to signals from the timer, the external interrupt switch located on the control panel,

external element checks from an element within the configured system and in certain circumstances from itself.

1. External Interrupt Caused by a Time Out or the Interrupt Key

If the interval timer times out, the CE will take an external interrupt if the PSW is properly masked (refer to Fig. 2-54). This same interrupt is taken, if properly masked, upon depressing the interrupt switch. The programmer would have the obligation of having a program routine which will place the CE in the status he desires upon branching to this routine as a result of the PSW swap on the external interrupt. For example, the programmer may desire to branch to the wait state or a program loop waiting for intervention by the operator.

2. External Interrupt Caused by a Read Direct or Write Direct Instruction Execution

If a read direct or a write direct instruction is issued for the purpose of transferring a byte of control data between CE and CE, the receiving CE, if properly masked, will take an external interrupt (refer to Fig. 2-54).

An example of the use of the external interrupt by execution of the Write and Read Direct Instruction is demonstrated by the following:

a. Assume that the system configured consists of two CEs, two IOCEs, several SEs, and several I/O devices.

b. Assume that only one CE can communicate with the IOCEs for the purpose of handling all I/O operations. This CE will be referred to as CE2.

c. Assume the CE1 is set up to communicate via the write instruction with CE2 and vice versa.

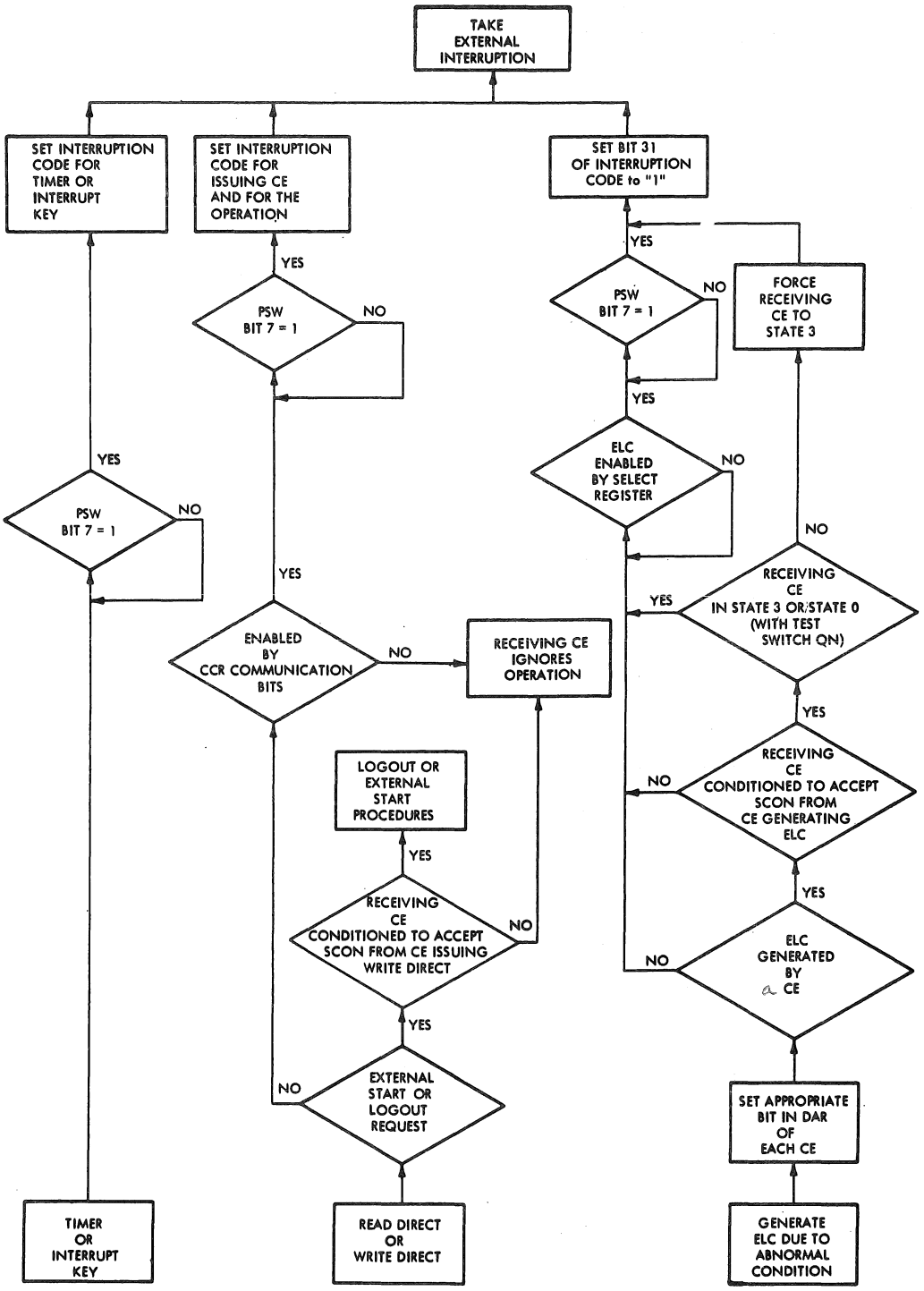


Figure 2-54. External Interrupt Scheme.

With these assumptions in mind, suppose that CE1 is executing a program that calls for an I/O operation. Since CE1 cannot communicate with the IOCEs, the I/O operation would be accomplished by CE1 issuing a Write Instruction to CE2 for the purpose of causing CE2 to execute a program which will perform or initiate the I/O operation. The write instruction executed would raise a direct-control line to CE2 indicating that CE1 was making a byte of control data available in its write register for CE2. As a result of the indication received via the direct-control line, CE2 will taken an external interrupt and the resulting PSW swap would branch CE 2 to a program which would issue a Read Direct Instruction back to CE1 indicating to CE1 that CE2 has accepted the data made available (provided proper masking exists). This first data byte may have contained the information which informed CE2 that it was to do a Start I/O instruction. The Read Direct Instruction issued by CE2 to CE1 subsequently causes, if CE1 is properly masked, to do an external interrupt. This external interruption in CE1 would cause CE1 to branch to a program which issues another Write Direct Instruction to CE2 making another byte of data available to CE2. This byte of data would be additional information such as part of the CCW address to be placed in CAW of the PSA area for CE2. In turn CE2 would issue a Read Direct Instruction to CE1 to notify CE1 that it has accepted the 2nd data byte. This operation would continue until the CE2 program had sufficient data information to perform the I/O operation by initiating a Start I/O to the IOCE controlling the I/O device.

The other operations initiated by the Write Direct Instruction are the external start and logout. Neither of these two operations cause an external interrupt.

3. The External Interrupt Caused by an Element Check Due to Abnormal Conditions

The abnormal condition which results in an external interrupt provides a means by which the CE responds to certain hardware generated signal from a CE, IOCE, SE, TCU, or PAM. In certain circumstances, a CE also responds to signals from itself. Three categories of abnormal condition signals are recognized, element check (ELC), out-of-tolerance check (OTC), and on-battery-signal (OBS).

A request for an abnormal condition interruption may occur at any time, and up to 30 requests may occur at the same time. The requests are preserved in the Diagnose Accessible Register (DAR) until accepted by the CE.

An abnormal condition interruption can occur only while the CE is interruptable for the element presenting the request. The manner which an interruption is handled depends upon the masking conditions prevailing in the CE, the type of element requesting the interruption, and upon the content of the configuration control registers in both the CE and the requesting element.

An abnormal condition interruption requested by an IOCE, SE, TCU, PAM, or by a CE (own) OTC, or CE (own) OBS signal sets an identifying bit in the DAR register (OTC being an out-of-tolerace check and OBS being an on-battery-supply).

An example of the use of the External Interrupt caused by an abnormal condition is demonstrated by the following discussion:

a. Assume that the system consists of two CEs, and IOCE and several SEs.

b. Assume that one of the CEs is executing a program.

c. Assume the system is properly masked to allow external interrupts.

During execution of this program while CE1 is accessing an SE, the SE goes on battery supply. The SE raises an ELC pulse which sets a bit in CE1 DAR register resulting in an external interrupt to occur in CE1. The CE1 could then branch on the interrupt to a program that would either ignore the condition or reconfigure another SE to take its place in the system. The example given is not an attempt to forecast how the interrupts will be used in any given case, but are presented only to give the reader a possible situation for a better understanding of the interrupt and its use. The masking necessary is shown in the flow diagram, Fig. 2-54.

E. The Machine Check Interrupt

The machine check interrupt provides a means of recovery from a logic malfunction in the CE or from IOCE itself and in certain cases recovery from logic checks in the SE configured in the system. In doing the machine check interrupt, the CE is automatically logged out prior to allowing the interrupt. By forcing this logout the data is stored in the PSA area where the subsequent machine check interrupt could possibly branch to a program which would analyze the logout data to determine the location of the fault. The indication of the check condition which caused the machine check interruption is preserved in the Check Register until reset by a diagnose instruction.

One example where an external element can cause a machine check is where an SE being accessed by a CE and the SE issues a Storage Check, this causes a bit in the check register to be set resulting, if properly masked, in a machine check interrupt after the automatic logout of the CE.

F. Summary of the Interrupt Scheme

The responsibility of providing the proper masking for the successful operation of the particular interrupt scheme is a burden that the programmer must bear. As in the prior examples given, there must be proper masking in general to handle the interrupt operation.

In addition to problems of masking, the programmer has the burden of placing the correct information in the corresponding PSW locations related to the particular interrupt anticipated by the programmer. The new PSWs must contain the information necessary for the branch operation desired on the PSW swap as a result of a particular interrupt. The new PSW information and the old PSW information is stored on a discrete doubleword boundaries in the PSA area corresponding to a particular interrupt. A summary of these locations are shown in Fig. 2-55.

	ADDRESS	LENGTH	PURPOSE
0	0000 0000	Double Word	Initial Program Loading PSW
8	0000 1000	Double Word	Initial Program Loading CCW1
16	0001 0000	Double Word	Initial Program Loading CCW2
24	0001 1000	Double Word	External Old PSW
32	0010 0000	Double Word	Supervisor Call Old PSW
40	0010 1000	Double Word	Program Old PSW
48	0011 0000	Double Word	Machine Old PSW
56	0011 1000	Double Word	Input/Output Old PSW
64	0100 0000	Double Word	Channel Status Word
72	0100 1000	Word	Channel Address Word
76	0100 1100	Word	Unused
80	0101 0000	Word	Timer
84	0101 0100	Word	Unused
88	0101 1000	Double Word	External New PSW
96	0110 0000	Double Word	Supervisor Call New PSW
104	0110 1000	Double Word	Program New PSW
112	0111 0000	Double Word	Machine New PSW
120	0111 1000	Double Word	Input/Output New PSW
128	1000 0000		Diagnostic Logout Area

Figure 2-55. PSA Area.

To review the basic masking requirements for a particular interrupt note the following:

1. An I/O interruption can occur only after execution of the current instruction is completed, and while the CE is interruptible for the channel presenting the request. Channels are masked by system mask bits 0-6 and 16-19 of the PSW. The interruptions are masked off by placing zero in the corresponding bit position. Interruptions masked off remain pending. The I/O interruption causes the old PSW to be stored at location 56 in the PSA and causes the channel status word associated with the interruption to be stored at location 64. Subsequently a new PSW is loaded from location 120. The interruption code in the old PSW identifies the channel and device causing the interruption in bits 20-23 and 24-31 respectively. The instruction-length code is unpredictable.

Whenever the status bits of the Channel Status Word (CSW) associated with the interruption indicate that the storing of the CSW was due to a channel control check, or an interface control check, additional information is provided by a diagnostic logout into the preferential storage area (PSA). To prevent the contents of the logout area from being destroyed by an immediately following logout, all channels of the selected IOCE must be masked until the logout information has been acted upon or stored elsewhere for later use.

2. A program interruption can occur only when the corresponding mask bit, if any, is one. When the mask bit is zero the interruption is ignored. Program interruptions do not remain pending. Program mask bits 36-39 permit masking of four of the interruption causes. The program interruption causes the old PSW to be stored at location 40 in the preferential-storage area and a new PSW to be fetched from location 104.

3. A supervisor-call interruption does not require any masking. It is a result of the execution of the supervisor-call instruction. The interruption causes the old PSW to be stored at location 32 in the PSA and a new PSW to be fetched from location 96.

4. The external interrupt caused by the interrupt switch or a timeout of the interval timer requires only that PSW bit 7 be set to a one.

The external interrupt caused by the execution of the write direct or read direct instruction causing a byte of data to be transferred requires PSW bit 7 and the communication bits of the sending CE to be set in the CCR register of the receiving CE.

The external interrupt caused by an ELC requires the corresponding mask bit to be set in the select register and PSW bit 7 in order for the interrupt to be taken. There is an exception when the ELC is issued by a CE and the receiving CE is sconed to the CE generating the ELC. If the receiving CE is not in state 3 or in state 0 with the test switch on, the receiving CE will

be forced into state 3 and will take an external interrupt. This occurs even though the PSW bit 7 is not set to a one or the corresponding mask bit is not on in the select register.

5. The machine check interrupt requires that the mask bit 13 to be set. When the machine check mask bit is one, occurance of a machine check due to a CE malfunction terminates the current instruction, issues a signal on the element check (ELC) out line, initiates a CE diagnostic procedure, and subsequently causes the machine-check interruption. The status of the CE is logged out into the PSA area, starting with location 132 and extending through as many words as the CE requires. The old PSW is stored at location 48 in the PSA area with an interruption code of zero. The new PSW is fetched from location 112. Proper execution of these steps depends upon the nature of the machine check. The indication of the check condition which caused the machine check interruption is preserved in the CE check registers until reset by a diagnose operation.

2-6. COMPUTING ELEMENT INTERNAL ERROR CHECKING

Hardware Failure conditions within the 7201 Computing Element are normally detected by internally contained redundancy check circuits. These circuits examine the bit contents of each byte during data transfers between registers and between the registers and any storage element. Each byte of data has 1 additional bit referred to as a parity bit; this bit serves to make the total bit count within the byte an odd number (even number under special conditions). This odd bit count is then tested during the aforementioned data transfers. Thus any dropped or picked bit will become immediately apparent. The loss or gain of a bit will be indicated by an error indication on the functional unit affecting the transfer and may cause a machine check interrupt (if proper masking exists) and subsequent logout. To provide a high degree of error resolution each error check is indicated individually on the CE operator's console.

A. Parity Tests

Each of the data paths within the 7201 (CE) have parity check circuits, and as necessary, parity generator circuits. Each of the counters for example is required to alter its parity bit each time it is decremented, the adder is required to generate correct parity for the two operands at the input. Parity, however, is still tested in the case of the adder or mover, based on the predicted parity as a result of the operands. During certain manual operations from the CE operator's panel, even parity may be inserted. There is a switch available for this purpose and is active only in the test state.

B. Error Check Analysis Diagrams

To simplify the analysis of the error indications, each position of the check register is indicated on an Error Check Analysis Diagram. These diagrams appear in the Logic Automated Diagrams (LADS) for the 7201. Figure 2-56 is an example of the Error Check Analysis Diagram (ECAD) cross reference while Fig. 2-57 is an example of the actual error check diagram.

The page listing in the left hand column refers to the ALD page where the unique parity check circuit is located. The ECA page listing on the interconnecting line refers to the ECAD applicable to the unique check under consideration, and the log bus information is the ALD page where the path for powering the indicator lamp is present.

An example of the use of the ECADs for analysis of a machine check would be as follows:

Assume that an Invalid ROS Address Check has occurred and the machine has "Hard Stopped". Examining Fig. 2-56 indicates that the circuits affecting this particular check are to be found on Page KT039 of the ALDs. The applicable ECA is number 122. Figure 2-57 is the ECA and Fig. 2-58 is the ALD Page KT039. Examining the ECA indicates that any time the three micro-orders, TCO, AL23, and DG2, occur within the same micro-instruction, an invalid ROS address

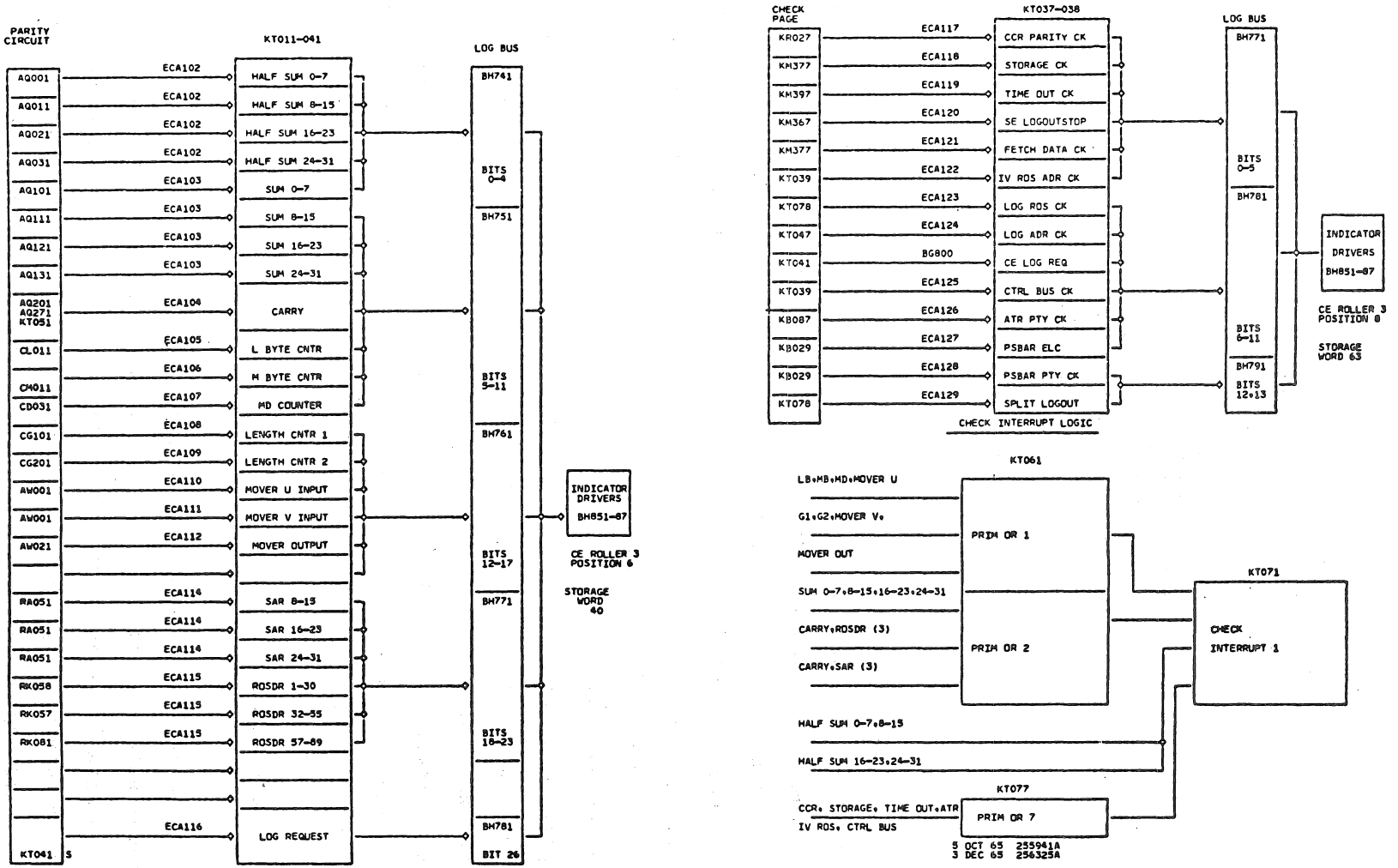


Figure 2-56. Check Registers.

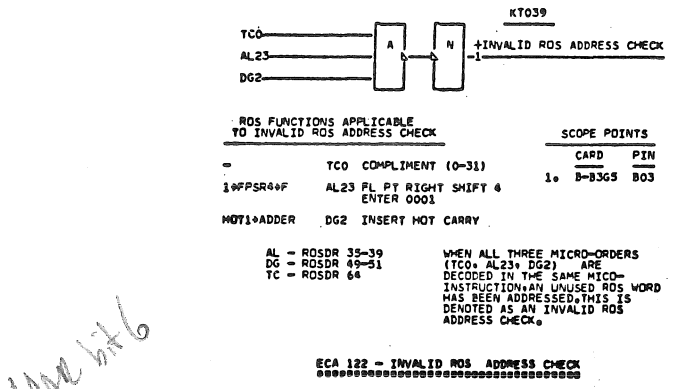


Figure 2-57. ECAD Example.

check will be indicated. Examining Fig. 2-58 which is the ALD representation of this check, it should be noted that the check is actually a result of the output of the OR gate at 6F which can be enabled by a ROS base address bit 5 and ROS function bit 0 or the aforementioned three micro-orders. The ECAD, while it is correct, is not complete since it does not indicate the second path. The ECAD and the ALD representation both indicate that on any unused micro-instruction, the micro-programmer will insert the three micro-orders to signify the invalidity of the instruction. Any time a ROS address has both the base address bit 5 and the function bit 8 on, a ROS select line greater than the possible 21 has been selected and thus a malfunction has occured. Since neither the unused words, nor the invalid selection of ROS select lines may occur in normal ROS operation, both of these situations are flagged as a machine check.

C. Logout Analysis

The 7201 Computing Element as mentioned previously is capable of recognizing internal data flow errors and in response to these errors will generate a machine check interrupt. Prior to the processor taking the interrupt, a logout of internal registers will occur. (It is at the programmer's option whether this logout takes place or not.) If the error is not ignored,

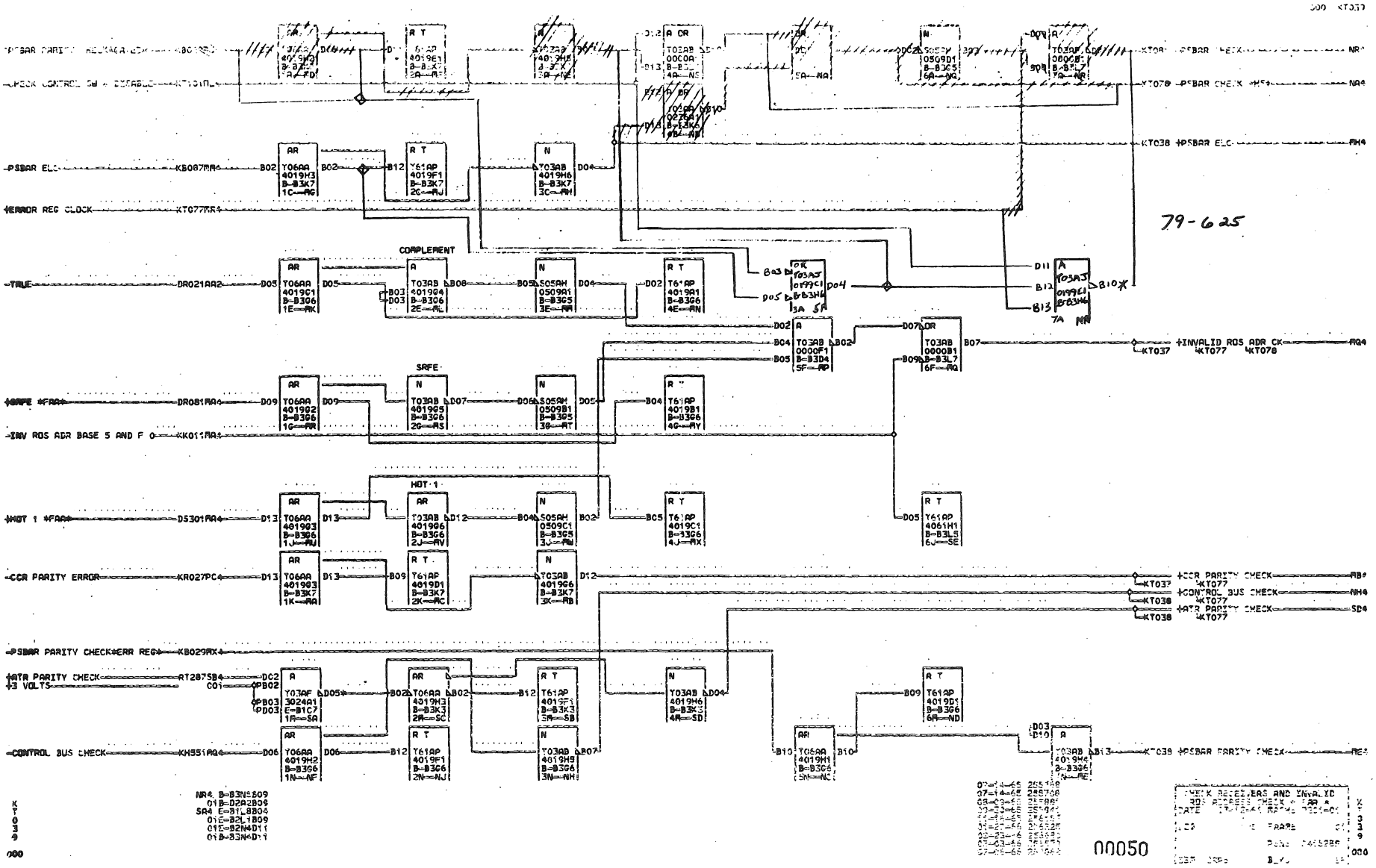


Figure 2-58. ALD Example.

immediately upon detecting an error, the machine status is frozen and a log-out is begun.

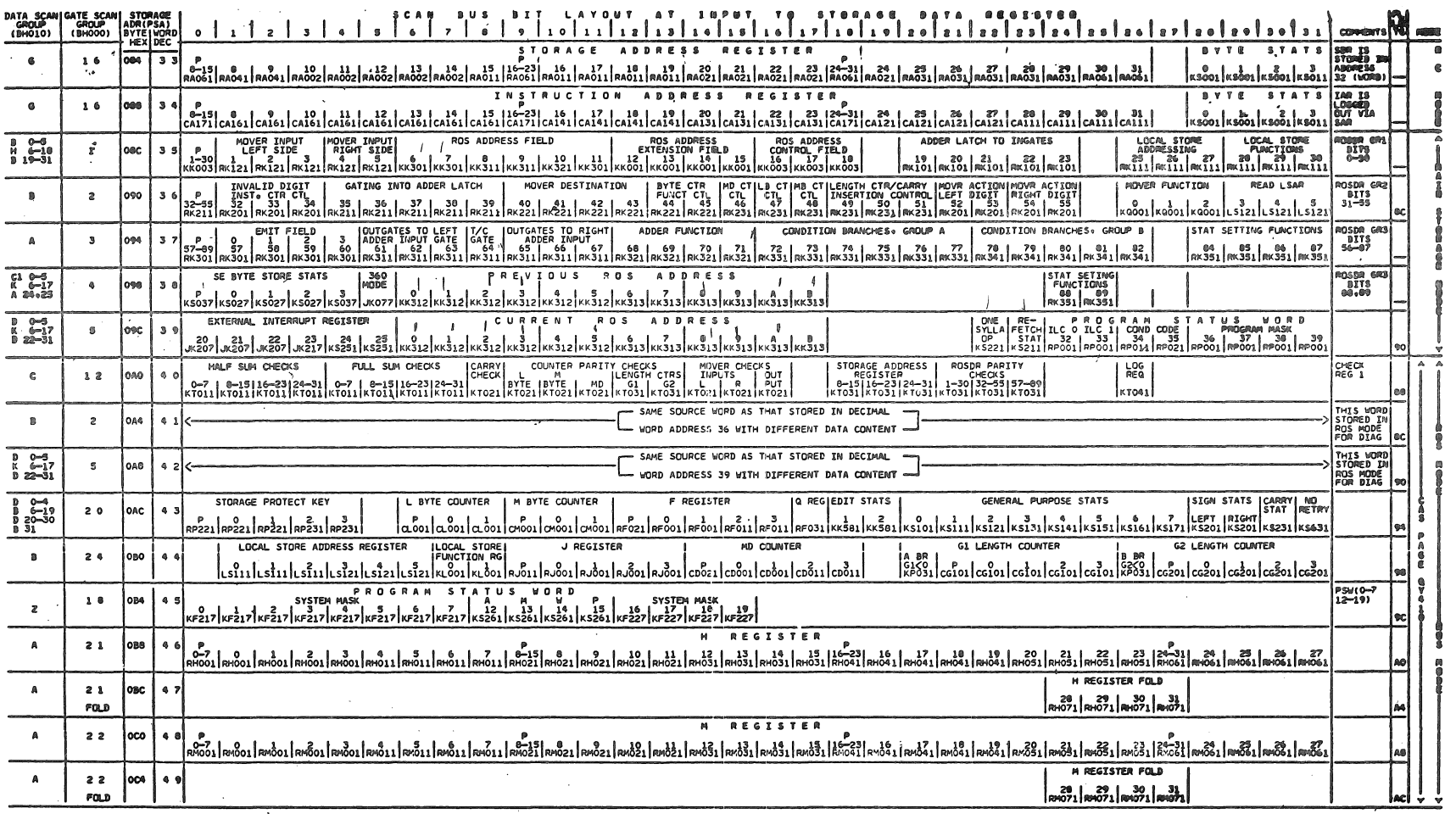
The first three words of a logout are stored under the control of the log counter in ring-counter mode. These words contain the SDR, SAR, and IAR at the time of the error. The next five words of the logout are stored under control of the log counter in Main Store Mode. These words contain the ROSDR information and ROS address information as well as certain PSW information. The remaining 26 words are stored under the control of ROS and contain information pertinent to the registers, counters, latches, etc., of the machine.

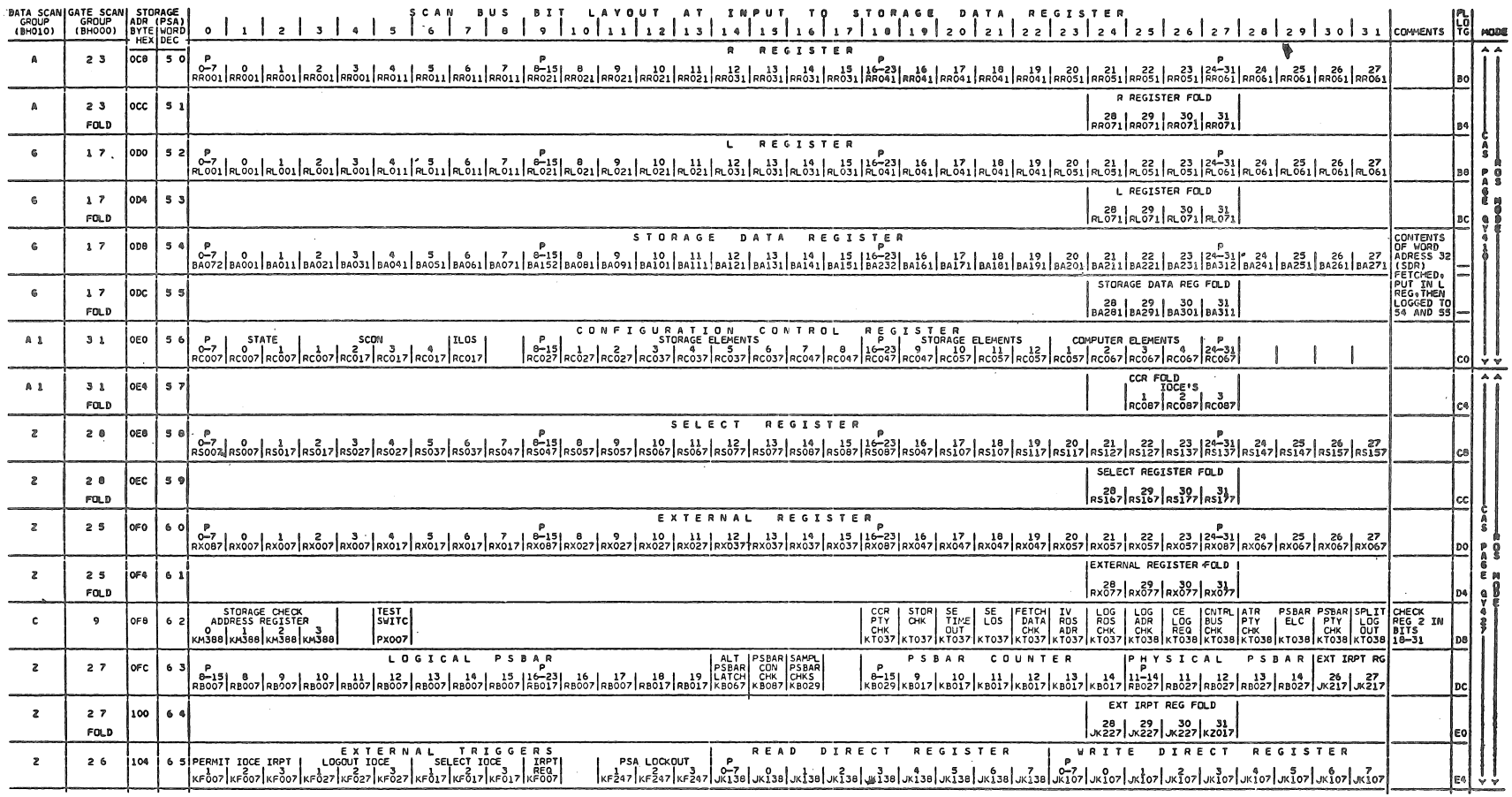
Figure 2-59 is a representation of the logout format.

Using the data contained in the logout of the element the technician or engineer should be able to reconstruct the environment of the system at the time of the malfunction. For example, assume a logout of the system exists where a sum-check is indicated in the check register number one. The engineer or technician may then consult the current ROS address to determine exactly what the machine was in the process of doing when the malfunction occured. Using the CAS logic diagrams in conjunction with the program listing and the IAR information, the technician or engineer may reconstruct the exact conditions and thus determine if the malfunction was merely a transient situation, or a solid failure condition. Should a solid failure exist, the technician may determine from the logout analysis of the registers being used and the appropriate data path in use approximately where the malfunction or failing unit is. In the event of a transient failure the engineer may elect to defer the maintenance until a scheduled period or he may elect to use Fault Locating Tests (FLTs) to assist him in isolating the failure and affixing the repair.

2-7. COMPUTING ELEMENT POWERING

A high-frequency power system is employed. The power system includes the following units:


SCAN BUS BIT LAYOUT AT INPUT TO STORAGE DATA REGISTER
DATA SCAN GROUP (BM010)
GATE SCAN GROUP (BM000)
STORAGE ADR(PSA) BYTE HEX
WORD DEC
COMMENTS
STORAGE ADDRESS REGISTER
INSTRUCTION ADDRESS REGISTER
BYTE STATS
IAR IS STORED IN ADDRESS 32 (WORD)
IAR IS LOADED OUT VIA SAR
MOVER INPUT LEFT SIDE
MOVER INPUT RIGHT SIDE
ROS ADDRESS FIELD
ROS ADDRESS EXTENSION FIELD
ROS ADDRESS CONTROL FIELD
ADDER LATCH TO INGATES
LOCAL STORE ADDRESSING
LOCAL STORE FUNCTIONS
ROSDR GR1 BITS 0-30
INVALID DIGIT INST. CTR CTL
GATING INTO ADDER LATCH
MOVER DESTINATION
BYTE CTR FUNCT CTL
MD CT CTL
LB CT CTL
MB CT CTL
LENGTH CTR/CARRY INSERTION CONTROL
MOVR ACTION LEFT DIGIT
MOVR ACTION RIGHT DIGIT
MOVER FUNCTION
READ LSAR
ROSDR GR2 BITS 31-55
EMIT FIELD
OUTGATES TO LEFT ADDER INPUT
T/C GATE
OUTGATES TO RIGHT ADDER INPUT
ADDER FUNCTION
CONDITION BRANCHES. GROUP A
CONDITION BRANCHES. GROUP B
STAT SETTING FUNCTIONS
ROSDR GR3 BITS 56-87
SE BYTE STORE STATS
360 MODE
PREVIOUS ROS ADDRESS
STAT SETING FUNCTIONS
ROSDR GR4 BITS 88,89
EXTERNAL INTERRUPT REGISTER
CURRENT ROS ADDRESS
ONE SYLLA OP
RE-FETCH STAT
ILC 0
ILC 1
COND CODE
PROGRAM MASK
PROGRAM STATUS WORD
HALF SUM CHECKS
FULL SUM CHECKS
CARRY CHECK
COUNTER PARITY CHECKS
MOVER CHECKS INPUTS
STORAGE ADDRESS REGISTER
ROSDR PARITY CHECKS
LOG REG
CHECK REG 1
SAME SOURCE WORD AS THAT STORED IN DECIMAL WORD ADDRESS 36 WITH DIFFERENT DATA CONTENT
THIS WORD STORED IN ROS MODE FOR DIAG
SAME SOURCE WORD AS THAT STORED IN DECIMAL WORD ADDRESS 39 WITH DIFFERENT DATA CONTENT
THIS WORD STORED IN ROS MODE FOR DIAG
STORAGE PROTECT KEY
L BYTE COUNTER
M BYTE COUNTER
F REGISTER
Q REG
EDIT STATS
GENERAL PURPOSE STATS
SIGN STATS
CARRY STAT
NO RETRY
LOCAL STORE ADDRESS REGISTER
LOCAL STORE FUNCTION RG
J REGISTER
MD COUNTER
G1 LENGTH COUNTER
G2 LENGTH COUNTER
PSW(0-7 12-19)
SYSTEM MASK
PROGRAM STATUS WORD
M REGISTER
M REGISTER FOLD
SCAN BUS PAGE 07610
2-76A


DATA SCAN GROUP (BH010)
GATE SCAN GROUP (BH000)
STORAGE ADR (PSA) BYTE HEX
STORAGE ADR (PSA) WORD DEC
SCAN BUS BIT LAYOUT AT INPUT TO STORAGE DATA REGISTER
COMMENTS
PL LOG TG
MODE
A 2 3 OC0 5 0 R REGISTER
A 2 3 FOLD OCC 5 1 R REGISTER FOLD
G 1 7 OD0 5 2 L REGISTER
G 1 7 FOLD OD4 5 3 L REGISTER FOLD
G 1 7 OD8 5 4 STORAGE DATA REGISTER CONTENTS OF WORD ADRESS 32 (SDR) FETCHED, PUT IN L REG, THEN LOGGED TO S4 AND S5
G 1 7 FOLD ODC 5 5 STORAGE DATA REG FOLD
A 1 3 1 OE0 5 6 CONFIGURATION CONTROL REGISTER
A 1 3 1 FOLD OE4 5 7 CCR FOLD
Z 2 0 OE8 5 8 SELECT REGISTER
Z 2 0 FOLD OEC 5 9 SELECT REGISTER FOLD
Z 2 5 OF0 6 0 EXTERNAL REGISTER
Z 2 5 FOLD OF4 6 1 EXTERNAL REGISTER FOLD
C 9 OF8 6 2 CHECK REG 2 IN BITS 18-31
Z 2 7 OFC 6 3 LOGICAL PSBAR PSBAR COUNTER PHYSICAL PSBAR EXT IRPT RG
Z 2 7 FOLD 100 6 4 EXT IRPT REG FOLD
Z 2 6 104 6 5 EXTERNAL TRIGGERS READ DIRECT REGISTER WRITE DIRECT REGISTER
CAS PAGE 0 Y 4 2 7
MOS MODE
CAS PAGE 0 Y 4 1 0
MOS MODE

1. Converter - This unit takes the 60-cycle power directly from the line, rectifies it, using a full wave bridge, and filters the output. The output of the converter is a nominal 276 vdc with a 3 percent ripple.

2. Inverter - This unit utilizes a silicon-controlled rectifier which, in conjunction with a 2.5 kc oscillator, changes the dc output of the converter to a 2.5 kc square wave with a nominal peak-to-peak amplitude of 276v.

3. Sine Wave Filter - The filter accepts the 2.5 kc inverter square wave output and changes it to a 2.5 kc sine wave of 100v (RMS).

4. Power Module - The high-frequency ac to dc converter is called the Mag-Amp-Ferro as its design combines the desirable features of a ferroresonant circuit with the simplicity of a magnetic amplifier. The ferroresonant circuit provides a relatively constant output voltage for wide variations of the input voltage. Another important advantage of ferroresonance is its inherent overvoltage and overcurrent capability. If a short circuit or near short circuit condition occurs, the ferroresonance collapses and the current is limited by the linear input inductance. Output voltage regulation is accomplished by the use of the mag-amp.

The basic operation of Power Control is explained by the following discussion in conjunction with Fig. 2-60.

A. AC Distribution

Three-phase, 208 volts ac, 60-cycle power input to the PCU (Fig. 2-60) is routed directly from the customer's ac service to a filter network. Each ac feed capacitor in the filter network has a 1 megohm resistor connected to ground. These resistors bleed off any charge remaining on the capacitors when the ac service is disconnected.

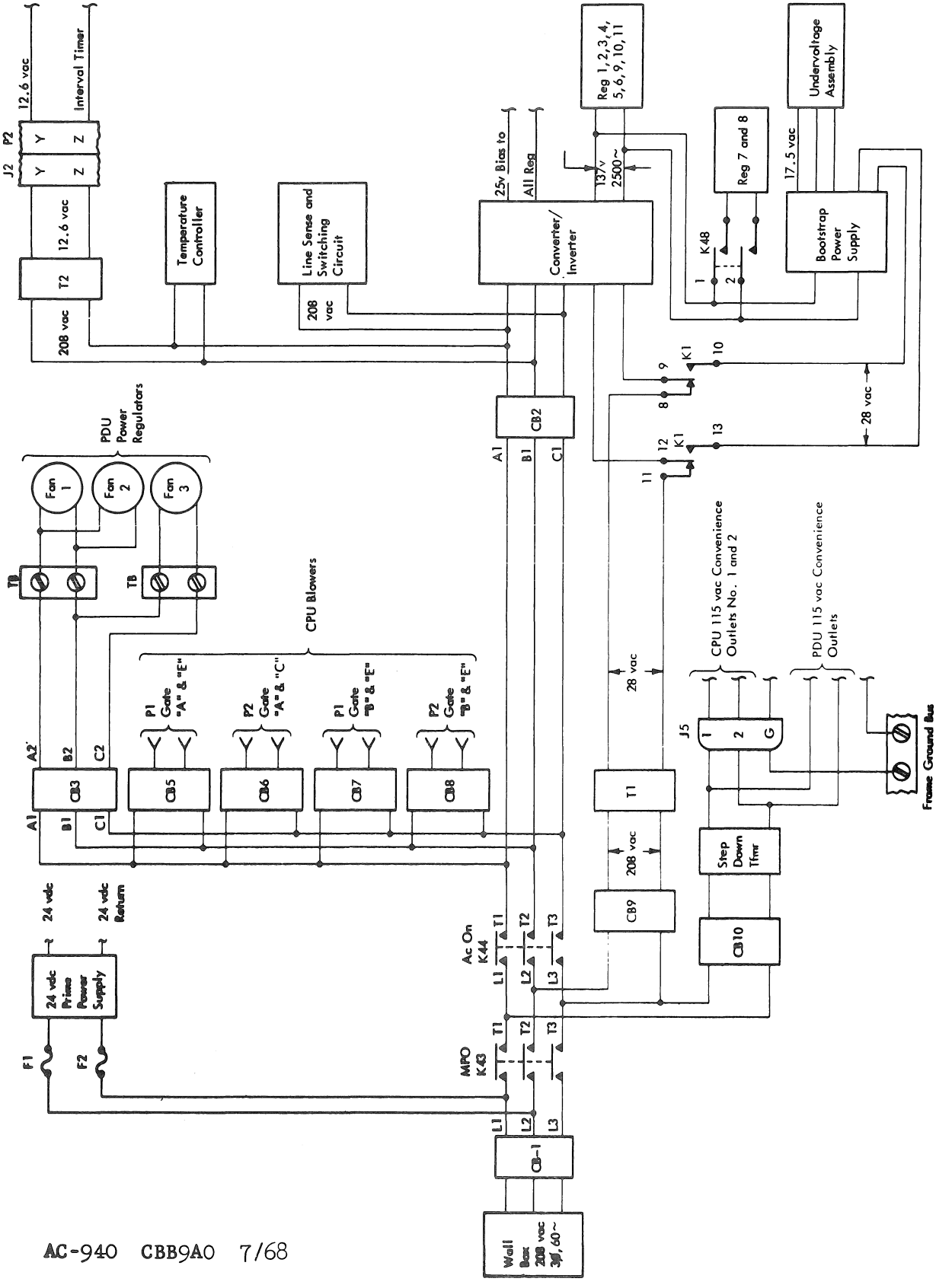


Figure 2-60. CE AC Distribution.

Initial turn-on of the main line circuit breaker CB1 applied 208 volts ac, single-phase via fuses F1 and F2 to the 24-volt dc prime power supply which provides power, via N/C contacts of K1 to the 24 volt dc bus. The 24 volts is first routed to the system Emergency Power Off (EPO) circuit in the System Console. If the EPO switch is closed, K37 (in the console) will pick, providing a return for element's Master Power Off (MPO) contact K43. If the element's MPO switch is closed, 24 volts dc is applied to the other leg of MPO relay K43, causing it to pick. From the contacts of K43, 208 volts ac, single-phase is routed via circuit breaker CB10 to the step-down transformer which provides 115 volts ac to the convenience outlets in the PDU and CPU. Single-phase 208 volts ac is also applied via circuit breaker CB9 to transformer T1. The secondary of T1 initially supplies 28 volts ac via relay K1 N/C contacts to the converter/inverter. With the contact of K43 closed, 24 volts dc is now applied to the sequence and control relays.

Before any further distribution of 208 volts ac can occur, ac on relay K44 must be picked. The picking of the relay takes place only after the operator's and PDU panels Power On/Off keys are on and time delay relay K45 has been picked. From the contacts of K44, 208 volts ac is applied to circuit breaker CB2, CB3, and CB5 through CB8. Circuit breaker CB2 control the three-phase 208 volts ac input to the converter/inverter and the single-phase 208 volts ac input to the temperature controller, line sense and switching circuit, and to the primary of transformer T2. The secondary of T2 (12.6 volts ac) is routed to the interval timer. Circuit breakers CB3, and CB5 through CB8 control the single-phase 208 volts ac to the PDU power regulator fans and CPU blowers.

Once the converter/inverter is on, its 2500 cycle output is routed to the standard voltage DC regulators and to the bootstrap power supply. This power supply provides the following voltages:

1. 17.5 volts ac to the undervoltage assembly.
2. 24 volts dc to the line sense and switching circuit.

3. 24 volts dc via N/O contacts of K15 or K48 to bootstrap power relay K1 shown on Fig. 2-60.

Once K1 is picked, the bootstrap power supply provides the 28 volts ac input to the converter/inverter, and 24 volts dc to the 24 volt dc bus (Fig. 2-60) through N/O contacts of K1.

B. Converter/Inverter Interlock Circuit

The converter/inverter interlock circuit insures that all necessary conditions are met before certain power and signal circuits are energized. Figure 2-61 is a simplified diagram of the interlock circuit. Prior to energizing the interlock circuit, 24 volts must be available, and the system EPO circuit in the System Console and the element MPO circuit must be closed.

When MPO contactor K43 picks, 24 volts dc is routed via K43 auxiliary contacts to one leg of the converter/inverter circuit breaker CB2-1 and thermal switch S2, to the dc return bus. Circuit breaker CB2-1 controls the operation of the converter/inverter, which supplies excitation to all regulators. Thermal switch S2 is closed if the correct temperature is maintained in the converter/inverter.

C. DC Distribution

Outputs of the dc regulators are distributed to the CE logic gates by standard dc bus distribution. All regulator outputs are shielded.

D. Power On Sequencing

Refer to the power-on sequence chart (Figs. 2-60 and 2-62) during the following discussion.

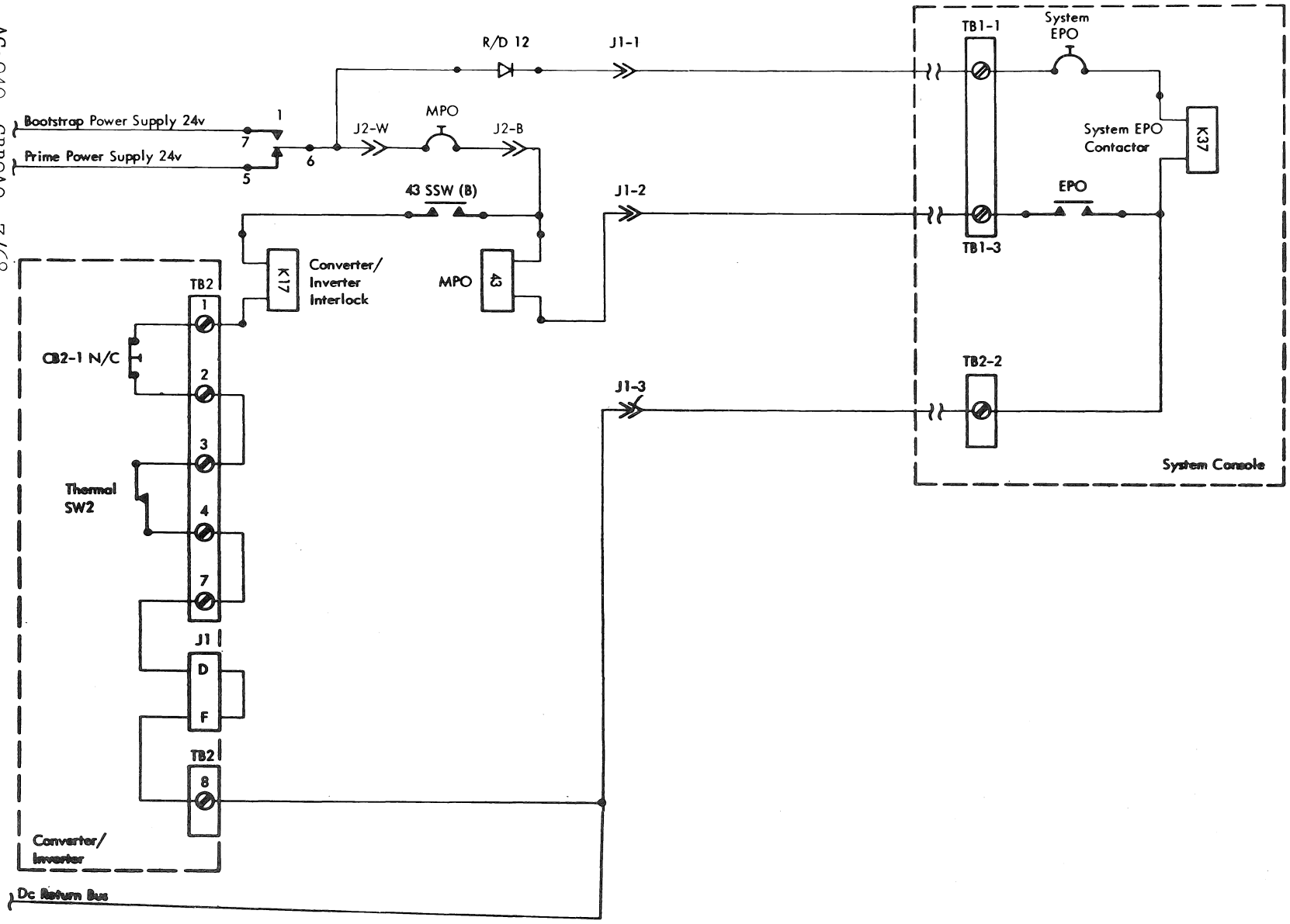


Figure 2-61. CE Converter-Inverter Interlock Circuit.

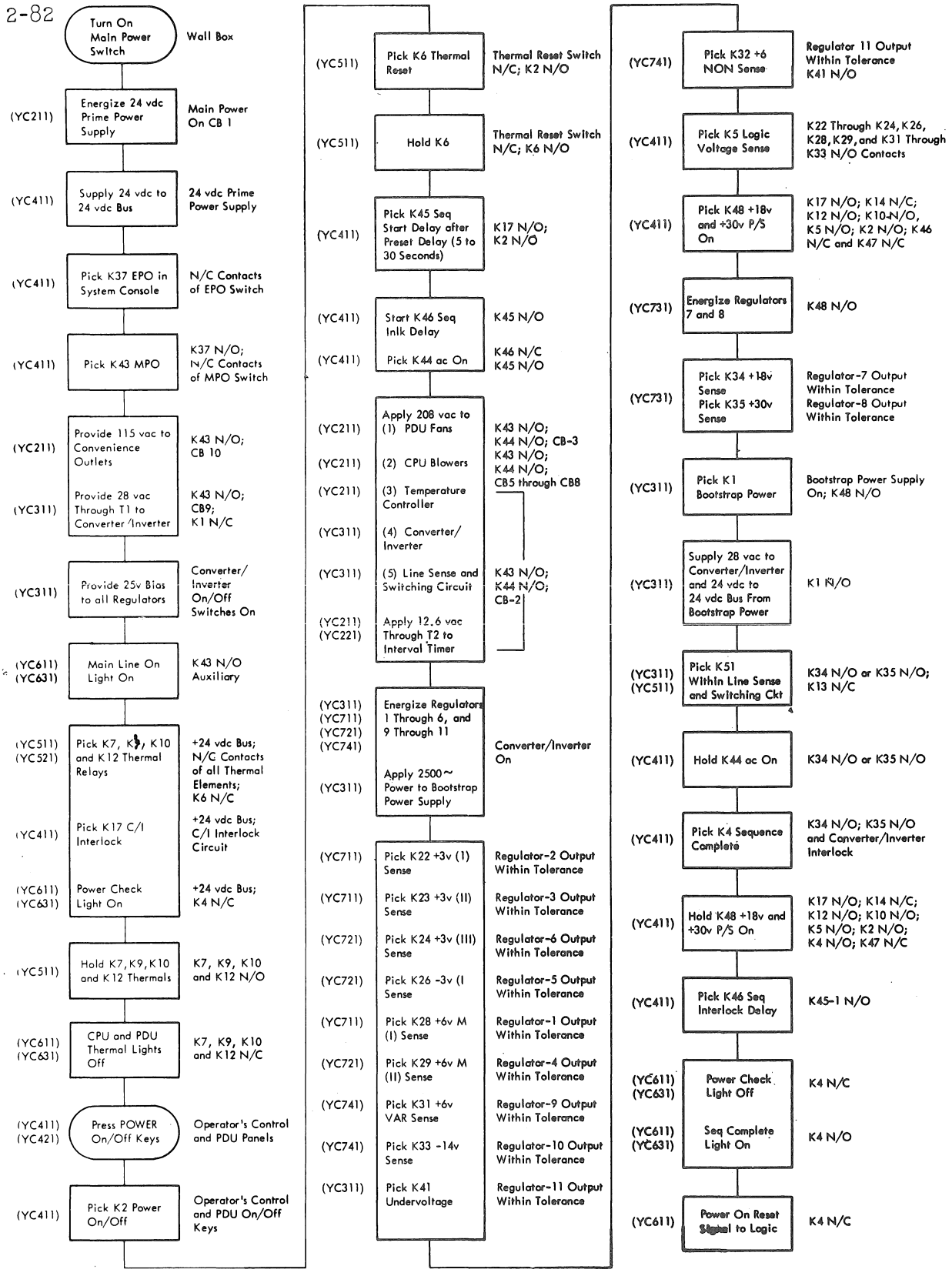


Figure 2-62. CE Power On Sequence Chart.

Before the power-on sequence in the CE can commence, circuit breaker CB1 must be closed, and system EPO contactor K37 and element MPO contactor K43 must be energized. The following action now occurs:

1. Main Line On light is lit.
2. Power Check light is lit through N/C contacts of K4 to indicate that a normal power off situation prevails.
3. If all thermal elements are in the normally closed position, thermal relays K7, K9, K10 and K12 are picked via K6 N/C contacts. After the thermal relay contacts transfer, each relay is held in a pick state through its own N/O contacts. The N/C contacts of K7, K9, K10 and K12 are used to turn off the thermal lights.
4. If circuit breakers CB3, and CB5 through CB9 are closed, relay K16 is maintained in a de-energized state. If the converter/inverter interlock circuit shown on Fig. 2-61 is closed, relay K17 is picked.

With the foregoing requirements satisfied, the power-on sequence commences by pressing the Power On/Off switches, completing the circuit which picks relay K2 (power on/off). The N/O contacts of K2 provide a return for thermal reset relay K6 and relay K45 (sequence start delay), causing both relays to pick. Relay K6 holds through its N O contacts until a manual thermal reset is initiated, or either an EPO or element MPO occurs. Relay K45 is adjustable from 5 to 30 seconds, and is set to a value to allow staggering of the 9020 System power-on sequence. When relay K45 times out, its N/O contacts allow relay K45 (sequence interlock) to start and relay K44 (ac on) to be picked. The delay time for relay K45 is adjusted to a value greater than the total time necessary to sequence up this element.

Once relay K44 is picked, three-phase 208 volts ac is applied to the converter/inverter, and single phase 208 volts ac is routed to the temperature controller, line sense and switching circuit, blowers and fans in the CPU and PDU, and to transformer T2.

The converter/inverter 2500 cycle output is first routed directly to the bootstrap power supply and to DC regulators 1 through 6 and 9 through 11. When the regulator outputs (except for regulator (11) are sensed, relays K22 through K24, K26, K28, K29, K31, and K33 are picked. As regulator 11 output is sensed, relay K41 (undervoltage) picks. The N/O contacts of K41 allow regulator 11 sense relay K32 to be picked. Relay K5 (logic voltage sense) is picked via the transferred contacts of K22 through K24, K26, K28, K29, and K31 through 33. The N/O contacts of K5 complete the return for relay K48 (+18V and +30V) P/S on, causing this relay to pick. Relay K48 controls the 2500 cycle input to regulator 7 (+18V) and regulator 8 (+30V). Relay K48 N/O contacts also provide a return for relay K1 (bootstrap power), causing this relay to pick. With K1 picked, the 24 volts to the 24 volt dc bus and the 28 volt ac input to the converter/inverter is applied from the bootstrap power supply. Regulators 7 and 8 control sense relays K34 and K35, respectively. N/O contacts of K34 and K35 complete the return for relay K51 (line sense and switching) allowing this relay to pick and provide a hold path for relay K44. Relays K34 and K35 N/O contacts also control the picking of relay K4 (sequence complete). When relay K4 is picked, a hold path is provided for relay K48, the Sequence Complete light is turned on, the Power Check light is turned off, and a logic power on reset signal becomes available. Relay K46 (sequence interlock delay) should now pick. Power is now applied to the CE logic circuits.

E. Normal Power Off

Refer to Fig. 2-60 and the power off sequence chart (Fig. 2-63) during the following discussion.

To initiate a normal power-off sequence, the CE must be in state zero (State Zero lamp on), and State Test switch on the Operator's Control Panel must be positioned to on. With these two conditions prevailing, relay K42 (power bit interlock) is in a de-energized state. Relay K42 N/O contacts interrupt the hold path for relay K2 (power on/off), which bypasses the Power On/Off switches.

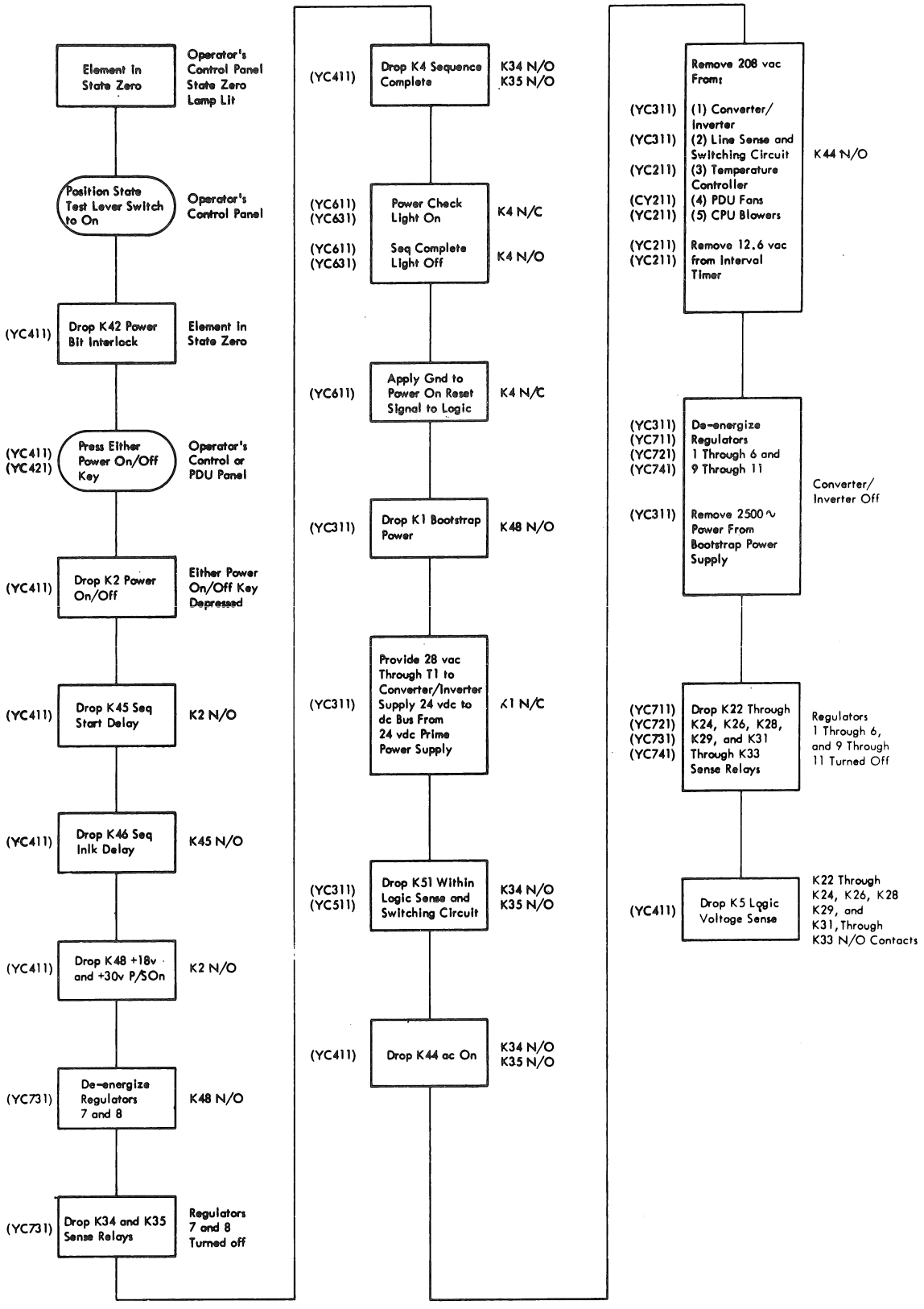


Figure 2-63. CE Power Off Sequence Chart.

When either the operator's control or the PDU panel Power On/Off key is depressed to Off, relay K2 is dropped. The transfer of K2 contacts to their N/O position interrupts the return for relay K45 (sequence start delay) and relay K48 (+18V and +30V P/S on), causing both relays to drop. Relay K45 N/O contacts cause relay K46 (sequence interlock delay) to drop. The N/O contacts of K48 cause relay K1 (bootstrap power) to drop. With K1 dropped, the 24 volts dc to the dc bus is supplied from the 24 volt prime power supply and the 28 volts ac to the converter/inverter (Fig. 2-60) is applied from transformer T1. Dropping relay K48 also removes excitation from regulator 7 (+18 volt), and regulator 8 (+30 volt). Removing these regulator outputs drops relay K34 (18 volt sense) and relay K35 (+30 volt sense). N/O contacts of K34 and K35 cause relay K4 (sequence complete) to drop. The Power Check light goes on (K4 N/C), the Sequence Complete light goes off (K4 N/O), and the power on signal is removed from the CE logic (K4 N/O). Also N/O contacts of relay K34 and K35 cause relay K51 (line sense and switching) and relay K44 (ac on) to be dropped. Once relay K44 is dropped, three-phase 208 volts ac is removed from the converter/inverter and single-phase 208 volts is removed from the temperature controller, line sense and switching circuit, all blowers and fans within the element, and transformer T2. De-energizing the converter/inverter turns off the remaining standard voltage regulators and the bootstrap power supply. Removing the outputs from regulators 1 through 6 and 9 through 11 causes the associated sense relays K22 through K24, K26, K28, K29, and K31 through K33) to be dropped.

When the contacts of these sense relays transfer, relay K5 (logic voltage sense) will be dropped. All CE power has now been removed, except for the ac input power, the 24 volts dc to the dc bus and the 28 volts ac to the converter/inverter.

F. Battery Back-Up Power Control

The CE contains a battery back-up power source that permits uninterrupted power for 5.5 seconds following the loss of the 208 volts ac primary input power.

Loss of primary input power is sensed as a decay of the converter/inverter output. When this output drops below a preset limit, reed relay RR1 within the sense and switching circuit is picked, and the battery package is switched into the converter/inverter. Reed relay points RR1-1 provide a return for relay K15 (on battery), causing the relay to pick. Relay K15 N/C contacts provide an on-battery signal to the logic circuits. The N/O contacts of K15 turn on the On Battery light on the Operator's Control Panel and SC Control Panel, provide a hold path for K1, and allow relay K47 (on battery limit) to be picked. Relay K47 is a delay pick (5.5 seconds) relay that controls the amount of time that the battery package output is applied to the converter/inverter. If the primary input power is re-applied to the CE within 5.5 seconds, relay K13 will be picked and relay K15 is dropped. Relay K13 N/C contacts interrupt the return for relay K51, causing the relay to drop. Relay K51 contacts remove the battery package input to the converter/inverter. After 5.5 seconds relay K47 is picked, and its N/O contacts cause relay K48 to drop. From this point, a normal power-off sequence takes place.

NOTE: The battery package output will not be applied to the converter/inverter during an emergency power-off situation.

If either the system EPO or the element MPO pull switch is activated, all power after the entry terminal, except for the 24 volt prime power supply, is turned off. The EPO and MPO switches are mechanical latch type switches that must be manually reset after being pulled.

The contacts of system EPO relay K37 provide a return for the element MPO relay K43, which must be picked before the element circuits can be energized. Whenever either an EPO or MPO occurs, relay K43 is dropped, and element power is sequenced off within 2 seconds.

H. Special Power-Off Sequences

Power Fault

Each CE regulator contains an overvoltage/overcurrent sense relay and a regular output sense relay. If an overvoltage/overcurrent condition exists in a given regulator, its respective sense relay (contained on the overvoltage/overcurrent SMS card) is picked. The N/O contacts of the picked sense relay causes relay K14 (overvoltage/overcurrent) to be picked. Each regulator output sense relay insures that the associated regulator output is at the proper amplitude required for normal element operation. The outputs from regulators 1 through 6 and 9 through 11 are sensed by relays K22 through K24 through K26, K28, K29, and K31 through K33. Should any one of these relays drop, relay K5 will be dropped. The outputs from regulators 7 and 8 are sensed by relays K34 and K35, respectively. Should any of these relays drop, relay K4 will be dropped.

The N/C contacts of relay K14 and N/O contacts of relays K5 and K4 are used in the return line for relay K48 (+18V and +30V P/S on). Thus, if an overvoltage/overcurrent condition occurs or should one of the regulator outputs be out of tolerance relay K48 is dropped. From this point on, a normal power-off sequence takes place.

Thermal Check

Two types of thermal checks (thermal warning and thermal catastrophic) can occur in the CE. The first check (thermal warning) occurs when the CE operating temperature in the CPU is 120° F but less than 130° F, or when the operating temperature in the PDU is 140° F but less than 165° F. The CPU and PDU thermal warning sensing devices control relays K7 and K9 respectively. When a thermal warning condition exists in either the CPU or PDU the associated thermal warning relay is dropped. The related Thermal light and the Power Check light on the Operator's Control Panel is turned on, 24 volt dc signal is routed to the Power Check light located on the SC, and an out-of-tolerance signal is applied to the CE logic circuits.

The second check (thermal catastrophic) occurs when the operating temperature in the CPU is more than 130° F or when the operating temperature in the PDU is more than 165° F. The CPU and PDU thermal catastrophic devices control relays K10 and K12, respectively. When a thermal catastropic condition exists in either the CPU or PDU, the associated thermal catastrophic relay is dropped. The N/C contacts of the dropped relay will cause the associated Thermal light and the Power Check light to turn on, providing a 24 volt dc signal to the Power Check light on the SC. The N/O contacts of either relay K10 or K12 interrupt the return for relay K48, causing this relay to drop. Relay K48 N/O contacts now initiate a normal power-off sequence.

A Thermal Reset switch is provided to reset the thermal relays. By activating this switch after the temperature in the overheated unit(s) has fallen below the warning level, the associate thermal relay will pick, causing the related thermal light to go out.

I. PDU Circuit Breaker Trip

The CE is provided with an Open CB lamp which indicates a tripped circuit breaker in the PDU. If any one of circuit breakers CB3 or CB5 through CB9 trips, relay K16 will pick. Relay K16 N/O contacts cause the Open CB light, on the Operator's Control Panel to be turned on and provide 24 volts dc to the SC Power Check light.

J. Controls and Indicators

1. Introduction

Following is a list of the controls and indicators associated with CE power. Some controls and indicators are located on the Operator's Control Panel, others are located on the PDU. The Operator's Control Panel and the PDU will be discussed separately.

2. Operator's Control Panel

The controls and indicators associated with CE power are located in the upper left-hand and lower right-hand sections of the panel. The Element MPO Pull switch is located in the upper right-hand corner of the panel.

Marginal Voltage Lights

These lights indicate when a marginal voltage is varied from its nominal value. One set of lights is used for each marginal voltage control.

3. PDU

The PDU controls and indicators are located on the front of the lower frame door panels. Controls and indicators on the regulators and converter/inverter are discussed in the Instruction Manual for SLT Power Supplies Z22-2799.

Mainline CB1 Circuit Breaker

CB1 controls the three-phase, 208 volt ac, 60-cycle input to the CE applied from the customer's ac service.

CB2 Circuit Breaker

CB2 controls inputs to converter/inverter, line sense and switching circuit, temperature controller, and transformer T2, which supplies excitation to the interval timer.

CB3 Circuit Breaker

CB3 controls input to PDU power Regulator fans.

CB5 through CB8 Circuit Breakers

CB5 through CB8 control inputs to the b[illegible] located in gates A, B, C, and E within the CPU.

CB9 Circuit Breaker

CB9 controls input to transformer T1, which supplies 28 volt ac excitation to the converter/inverter.

CB10 Circuit Breaker

CB10 controls input to the convenience outlets in the PDU and CPU.

Power On/Off Switch

This switch can initiate the power on/power off sequence for the CE. After the completion of a power on sequence, this switch is active only when the CE is in state zero, and the State Test switch is in the On position. The PDU Power On/Off switch is connected in series with the Power On/Off key located on the Operator's Control Panel.

Thermal Reset Key

Pressing this key resets tht thermal relays controlled by the thermal sensing elements within the CPU and PDU frames. Activation of this key will also turn off the Thermal Check light(s) if the related frame temperature has fallen below the warning level.

Fuses F1 and F2

These fuses protect the 24-volt prime power supply and its associated circuits from overload.

2-10. COMPUTING ELEMENT TESTING

Within the 7201 Computing Element there exists special hardware and ROS routines to assist the maintenance technician or engineer in isolating malfunctions and affixing repairs. Due to the complexity of this system, the testing of it must be performed in stages. Therefore, it stands to reason that a hierarchy of procedures should exist. Since the Read Only Storage of the Computing Element must be functional before even the most basic of programs

may be executed, there are a series of tests which may be executed from the Operator's Panel which enable the technician or engineer to verify that each bit of the ROSDR may be set and reset under the influence of data read from the CROS Planes. (Refer to CLD Page QW111-222.) There are also operator panel initiated ROS routines to ripple selected quadrants of local storage, to ripple sequential locations of main storage, and to transfer data from the data keys to the registers. These tests require only that the clocks be operational, and that the addressing circuits of ROS be capable of selecting the proper words. As the tests are completed, the element under test is readied for the next higher form of testing.

Since the Built-In ROS routines provide a visual indication of the ability of the microprogram to set and reset the bits in the various registers and storages from the data keys, the next higher echelon of tests should provide some method of verifying the elements ability to set and reset these registers using normal data paths, and finally the ability to use the functional units in conjunction with each other to process data. This job of testing is related to the Fault Locating Tests (FLTs). The FLTs utilize the data paths into the machine from storage and the logout paths within the machine to place the data back into storage. FLTs may be executed and their results interpreted, or in the case of an exclusive intermittent, the FLTs may be executed while the logic voltages are raised or lowered in order to induce a solid failure. Since the FLTs are considered a higher form of testing, the requirements placed on the equipment for their execution are greater. To execute the most basic FLT for example 8K words of operating storage are required as well as an operating selector channel and an operating Tape Control Unit and Tape Drive. The FLT load circuitry between the IOCE and CE must also be operational and the interface between the CE and SE must be functional. The result of the performance of the FLTs and the data presented to the technician or engineer is in the form of visual indications in the SDR and IAR of the element under test. This information, when properly interpreted will lead the technician or engineer to the failing functional unit in a minimum of time.

Fault Locating Tests as mentioned previously may be run with the logic voltages either raised or lowered to induce failures in the functional units. By gradually lowering the voltages, an intermittent failure may be induced to become a solid failure and thus permit successful repair in an otherwise difficult situation. In general, the repair of a malfunction should be attempted at the lowest echelon of testing where its indications are well defined. Thus, if a functional unit failure is manifest both in ROS tests from the panel (Bring-Up Aids) and in the FLT tests, it is probably easier to affect the repair using the Bring-Up routine for the scoping sync, etc.

Since both the Bring-Up Aids and the FLTs have verified the ability of the functional units to operate under varying conditions, the machine is now ready to be tested under simulated operating conditions. The Maintenance Diagnostic Monitor Program provides a method of testing using actual machine instructions. The MDM program starts using only one instruction, after verifying the operation of the instruction, the program uses it to "bootstrap" its way to more instructions. Since this is a progressive form of testing, any time an instruction is incapable of being executed, an interrupt to the monitor may occur. This permits the program to branch to a routine to either print out on the console printer or, if incapable of the interrupt, the program will stop and IAR and SDR indications in conjunction with the program listings may be used to isolate the malfunction. The operation of the MDM presupposes that the element under test has successfully passed the FLT tests. In general the malfunctions detected by these tests will be due to the inability to perform certain micro-orders unique to the particular instruction under test.

MDM tests are designed with many options. They may be executed in a multiprocessing environment, they may be used to test the various I/O devices in the system, and may utilize various available I/O devices for loading and communication between the operator and the monitor. This great flexibility is due to the elaborate monitor used to direct the testing of the instructions. This monitor also provides optional features such as the editing of the printout of the machine check logouts, and the ability to reconfigure the system under test.

Successful completion of the MDM tests by the system indicate that the system is capable of performing the jobs assigned under this form of testing and may be further and more completely tested by a group of tests contained on the same record. The final and highest form of testing available in the 9020 System is referred to as the SEVA tests. These tests, while the most comprehensive, give the poorest resolution for maintenance purposes. The machine check logout provides a document for maintenance resolution which may be analyzed as described in a previous section.

CHAPTER 3

STORAGE ELEMENT

3-1. 7351-04 STORAGE ELEMENT

Storage elements are basic units of an IBM-9020 System. Each storage element contains its own core arrays, registers, power supplies, backup power (batteries), and maintenance panel. A sub-assembly within each storage element called Basic Operational Storage (BOS) contains the core arrays, address decoding circuits, and drive circuits for the arrays.

Storage elements hold stored programs and the data to be used in the execution of the programs. Some of the reasons for selecting a core storage unit to hold these items are: reliability of operation, random access to data, speed of operation, and convenience of size.

The storage element performs the five functions shown in Fig. 3-1:

1. Receives input from input/output machines such as a tape unit, card reader, or drum storage.
2. Sends output information to input/output machines such as a tape unit, printer, or drum storage.
3. Sends instructions and control information to the control section of the processing unit.
4. Sends data to the processing unit.
5. Receives data from the processing unit.

The storage element handles all stored information as data, making no distinction between program instructions, control words, or numbers.

If we compare the information in a core storage unit to a file of punched cards, one item of information in the storage unit is similar to one card of the deck. All cards of one deck are equal in length and each card can hold a certain quantity of information. Likewise, all items in a storage unit

are equal in length and each item can hold a given quantity of information, called a word.

In some customer applications, the whole card is one field of information. In other applications, cards are subdivided into smaller fields (Fig. 3-2). Words in a storage unit may be subdivided into smaller units called bytes. Storage units of the IBM-9020 System have basic field lengths of one word.

3-2. THEORY OF MAGNETIC CORE STORAGE

A. Ferrite Core

A ferrite core is a small, doughnut-shaped ring of ferromagnetic material prepared from iron oxide, sinc, manganese, and nickel. These materials are ground to a fine powder, mixed with a binder, and pressed into shape by automatic presses. After firing in a kiln, the ferrite core is hard and brittle. The resistivity of the ferrite material makes eddy current losses and shielding requirements negligible, and results in efficient magnetic cores.

B. Magnetic Properties

The ferromagnetic character of the ferrite core permits it to be magnetized by any convenient magnetomotive force (mmf). After being magnetized, the core retains its magnetic polarity even though the mmf is removed. This makes the core useful as a storage device. Electric (drive) current carried by a wire through the hole in the core can generate the mmf. Thus, the polarity and strength of the mmf (and the polarity of the core) can be controlled by varying the direction and strength of the drive current.

Under static conditions (no current), the ferrite core is magnetized in one of two stable states. Items 1 and 0 (Fig. 3-3) shows a schematic representation of these two states. In either state, the magnetic flux is contained entirely within the ferrite material. The actions of a core changing state occur in sequence. Drive current through the horizontal wire builds up a

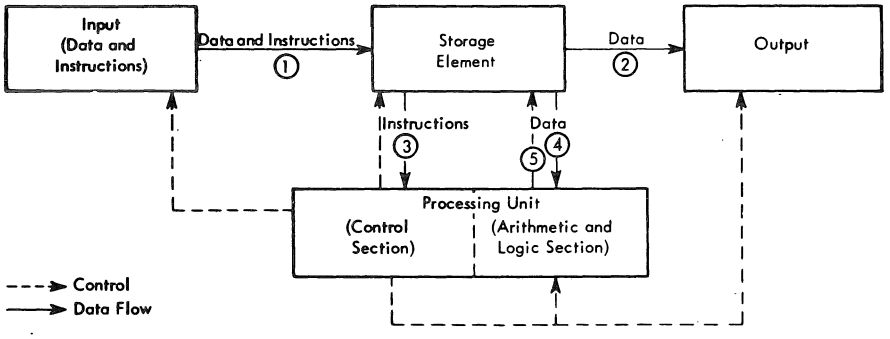


Figure 3-1. Computer Functions.

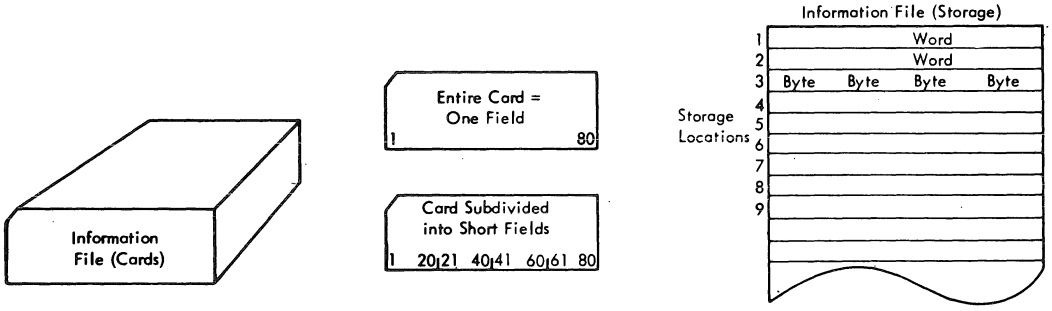


Figure 3-2. Comparing Core Storage to Punched Cards.

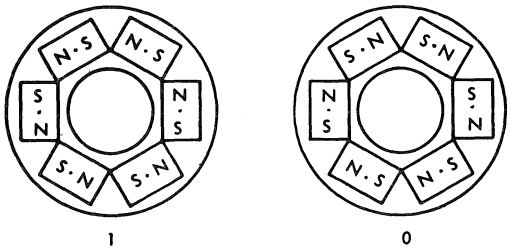


Figure 3-3. Two Stable States of Magnetic Core.

magnetic field in the direction of the outer curved arrows (Fig. 3-4). When the current generates an opposing field of sufficient strength, the magnets break from each other and spin about (small curved arrows) to align themselves in the opposite direction. Once "flipped", the magnets maintain their new position. During the realignment of the magnetism in the core, magnetic lines of force extend beyond the ferrite material (Fig. 3-5). The external lines occur only while the magnets are changing direction and recede into the ferrite when the change is complete. The lines of force that cut the sense output line generate a pulse that is amplified and sensed by a sense amplifier. A pulse indicates that the magnetic state of a core changed.

A certain field strength must be exceeded to cause the core to change state; neither a lower level nor a greater level has much effect. This field strength or mmf is developed by an electric current. An amount of current, I, is more than adequate to flip the core, whereas I/2 is not sufficient to flip the core. Current can be sent through the drive line in one direction (+I) to place the core in the 1 status, and in the other direction (-I) for 0 status.

All the drive current through the core does not have to be carried by one wire. If two wires go through the core in the same direction, I/2 in each has the same effect as I in one wire. The drive wires are called X and Y. Half current (called inhibit or Z) in a direction to oppose one of the drive currents (in a third wire) is used to control changing the status of the core to a 1. The fields developed by the current add together algebraically.

Figure 3-6 shows an arrangement affording complete selectivity and control of the core according to the following table:

Drive Line

Case	X	Y	Z	Effect
1	+I/2			None
2		+I/2		None
3	-I/2			None
4		-I/2		None
5	-I/2	-I/2		Write Zero
6	+I/2	+I/2		Write One
7	+I/2	+I/2	-I/2	None
8	+I/2		-I/2	None
9		+I/2	-I/2	None

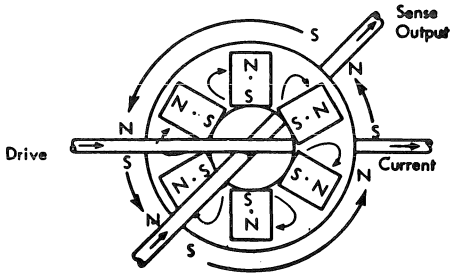


Figure 3-4. 1 Changing to 0.

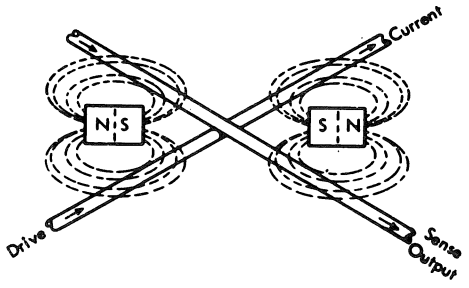


Figure 3-5. Core Field While Changing States.

C. Hysteresis Loop

The switching of a ferrite core may be plotted on a graph called a hysteresis loop. The graph in Fig. 3-7A shows the relationship of magnetic flux density (B) on the vertical axis and drive currents (mmf) on the horizontal axis.

A ferrite core at A is unmagnetized. If +I/2 is applied to both the X and Y drive lines in the same direction through the core, the resulting mmf causes the core to magnetize along path AC. The core is saturated at point C, and any further increase in current has no significant effect on the core. When the current is cut off, the flux state of the core slips to point D, which is arbitrarily designated as a 1.

While the core is at point D, a +I/2 current applied to either or both the X and Y drive lines cause the core to magnetize toward point C. A -I/2 on either the X or Y drive line causes the state of the core to move toward point E. In either of these cases, when current is removed, the status of the core reverts to point D.

When -I/2 is applied to both the X and Y drive lines, the core follows path DF and switches at a point between -I/2 and -I. When drive current is removed from both drive lines, it causes the flux to settle at point G, which arbitrarily represents a 0. A +I/2 on either the X or Y drive line advances the status of the core toward point H, but does not flip the core; and when current is removed, the core reverts to or near point G. A +I/2 applied to both the X and Y drive switches the core along the path GC. When current is removed, the core reverts to point D.

Once a core has flipped, drive currents are removed and the status of the core settles, along the curve, to the vertical axis, where it remains until drive currents are applied again. Plus or minus I/2 moves the status of the core along the hysteresis loop, but does not flip the core; and the core settles back near the starting point on the vertical axis.

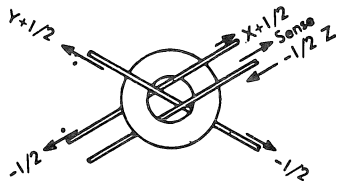


Figure 3-6. Core Wires (Three Wire System).

Note that:

1. Current in a direction that would magnetize the core to a specific state has little effect on a core already magnetized to that state.
2. One-half current in a direction to reverse the magnetic state of a core has little effect on core magnetism and does not flip the core.
3. Full current in a direction to reverse the magnetic state of a core does reverse the state.
4. Ferrite cores used for storage require a nearly square hysteresis loop for reliable operation.

The preceding description applies to a ferrite core having characteristics desirable for information storage and operating under normal conditions. Abnormal conditions, such as high temperature, can distort the hysteresis loop (Fig. 3-7B) so that the core is no longer a reliable storage device. With a distorted hysteresis loop, a magnetized core is unable to resist half-select current and does not retain full magnetization when drive current ceases to flow.

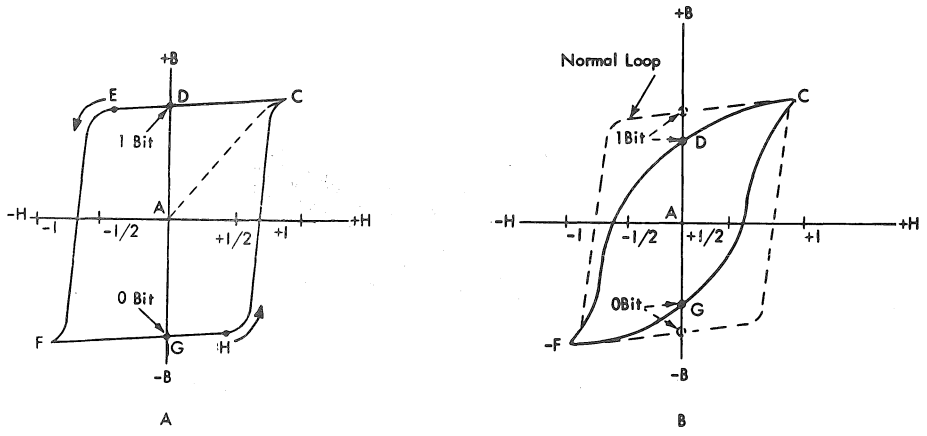


Figure 3-7. Normal and Heat-Distorted Hysteresis Loops.

A core may become hot and lose its storage ability because temperature control of the core environment has been lost, or because one core location has been repeatedly driven from 1 to 0 and back to 1 again many times in rapid succession. The latter condition is known as "beating" a core location. Defects such as cracks, breaks, and voids make the cores sensitive to high temperature.

3-3. CORE PLANES

Because each core can hold only one bit of information (1 or 0) many cores are required. To use them as a main storage unit, the cores are arranged in planes as shown in Fig. 3-8. Adjacent cores are aligned at 90 degrees to each other to reduce interference. Cores are held in place by the wires that pass through them.

The X drive lines are all parallel to each other and pass through all cores in a line across the plane. Y drive lines are parallel to each other but are perpendicular to X drive lines. Each Y drive line passes through all cores in a line.

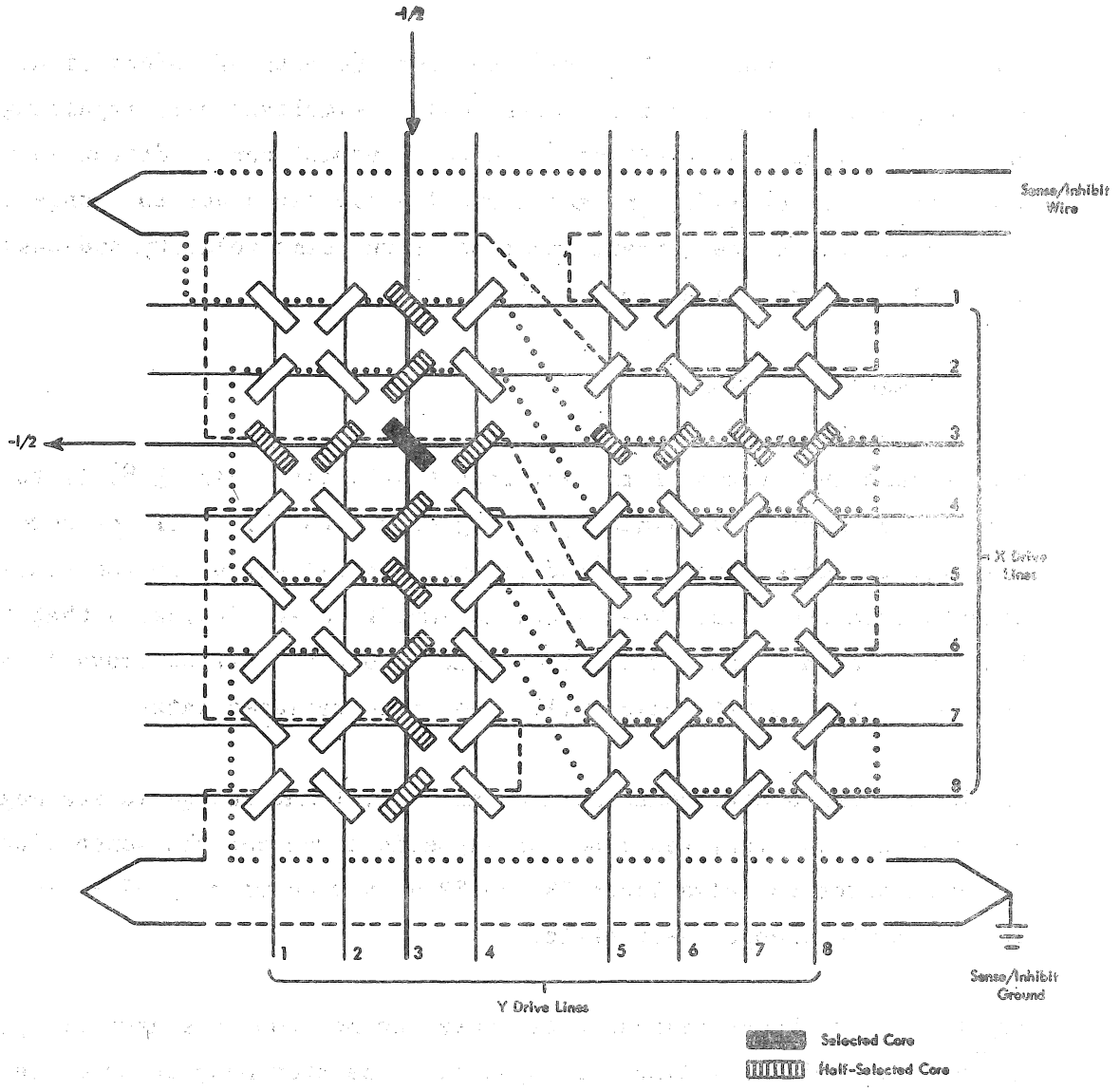


Figure 3-8. Arrangement of Cores.

The sense/inhibit wire is parallel to X drive lines and passes through all cores in the plane. The sense wire serves a double purpose in that it is used to prevent the writing of one bits. See the "Inhibit" section.

3-4. COINCIDENT CURRENT ADDRESSING

The 8 x 8 plane shown in Fig. 3-8 can store 64 bits of information. Any core in the plane can be selected (addressed) by simultaneously impulsing the X and Y drive lines intersecting the core. Current can be driven in either direction (+I/2 or -I/2) in each X and Y drive line; but to change the status of a core, both drive currents must be of the same polarity and pass through a core in the same direction.

3-5. READ-OUT, SENSE

Assume that the status of the selected (dark) core (Fig. 3-8) is to be read out by impulsing drive lines X3 and Y3 each with -I/2. If the core contains a 1 bit, the core flips to 0 and induces a small signal on the sense/inhibit wire through the core. The signal is amplified and indicates that the core had contained a 1 bit. The act of reading out a 1 bit destroys it and leaves the core with a 0 bit, which will have to be replaced later.

If the addressed core contains a 0, no significant change in its magnetic state occurs and very few lines of magnetic force cut the sense winding. The other 14 cores on drive lines X3 and Y3 each receive only -I/2, which is not sufficient to change their state.

Strobe: Even though half-selected cores do not change status (flip), the accumulation of a few lines of magnetic force from many cores causes a disturbance (Noise) on the sense wire. The amplitude of the noise may, under certain conditions, exceed the amplitude of a signal from a core that changes status. Therefore, a special timing pulse, called strobe, is generated to gate the signal from a core changing status to the sense amplifier.

3-6. WRITE, STORE

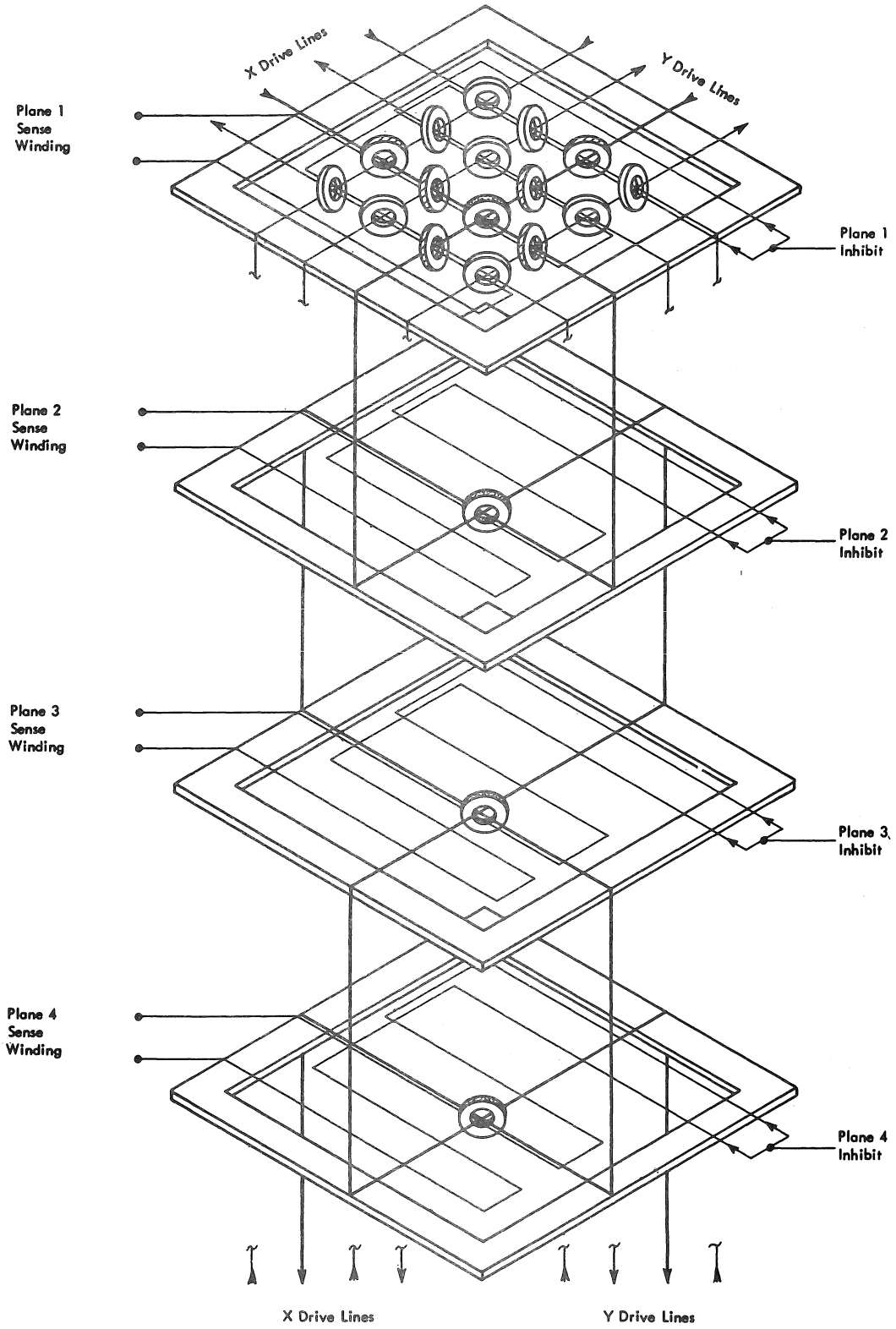
Putting information into the core plane is called a write, or store, operation. The write operation changes the status of selected cores from 0 to 1. Status of the selected core (Fig. 3-8) can be changed from 0 to 1 by impulsing drive lines X3 and Y3 with +I/2 (opposite to the direction of the read current).

Inhibit: Each time +I/2 is sent through drive lines X3 and Y3 (Fig. 3-8), the two drive currents attempt to change the status of the core to a 1. However, to store useful information, some cores must remain in the 0 status. Therefore, another current, called inhibit or Z, retains a status in a core by opposing and cancelling X drive write-current. The Y drive current alone is not sufficient to change the status of a core to a 1.

Note: In some core storage units, a fourth wire is added to carry inhibit current. (Sense and inhibit are separate wires.) However, because an output from a core is not wanted during writing, the sense wire can carry inhibit current and thus simplify core wiring.

3-7. CORE ARRAY

We have discussed only one plane in which only one core at a time can be addressed. To represent characters other than 0 and 1, several bits must be read out or stored at one time. To handle more than one bit of information at a time, planes are stacked vertically (Fig. 3-9) to form an array. The number of places in an array is determined by the number of bits that must be handled on one read or write operation. Each X and Y drive line is connected from plane to plane through the whole array (Fig. 3-9), while each sense and inhibit winding is for only one plane or a section of a plane. In actual practice, four sense inhibit wires are in each plane to reduce the length of each wire and thereby increase the speed of operation by getting the sensed output to an amplifier sooner than would be possible with only one sense wire per plane.



NOTE: Arrows indicate current direction.

Figure 3-9. Core Array, 4 x 4 x 4.

The X and Y drive lines pass through many planes in an array and thus some delay occurs between the arrival of the drive current at the first and last planes. Therefore, the strobe pulse also is delayed for the last planes to ensure that only sensed outputs and not noise are gated to the sense amplifiers.

3-8. CAPACITY

A core storage unit can be large or small. The smallest ones have only a few hundred cores in them and the largest contains millions of cores. Usually, the larger sizes are slower in operation. Optimum sizes, determined by programs to be run and speed required, are selected for each computer. The optimum size, called capacity, is the maximum number of locations or items of information that can be held in the storage unit.

The IBM-9020 System transmits information between main storage and the processing unit in words (four bytes). One word fills one location in the 9020 main storage.

A core storage unit is like a cube with pigeonholes where information can be stored and later retrieved. Figure 3-10 shows a small core storage unit utilizing a two-digit system of addressing. The units digit defines the X coordinate and the tens digit defines the Y coordinate. Together, the X and Y coordinates make up the address of a location of storage. Any location can be addressed by its coordinates, thus random access. The capacity of the cube shown is 8 x 8, or 64 words (256 bytes).

Capacity of each 7251-03 Storage Element is 32,768 words (131,072 bytes). To hold this amount of data, requires two 18-plane arrays.

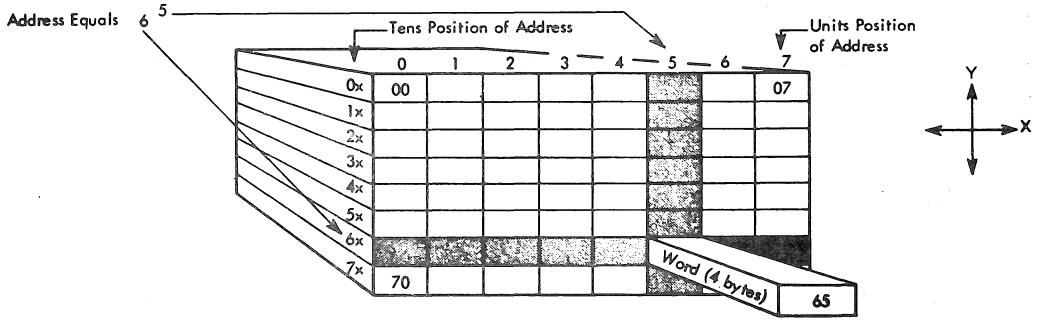


Figure 3-10. Pigeonhole Storage.

3-9. STORAGE CYCLE

Random access storage units have a set routine (called a storage cycle) to read out or store data. The processing unit provides storage with an operation (fetch or store), an address, and a start signal. The address from the processing unit is decoded within the storage unit to select an X and a Y drive line for the addressed location. The start signal from the processing unit initiates a storage cycle to read out or store the data. Once started, the storage cycle proceeds under the control of a storage unit clock, independently of processing unit timing (asynchronous operation).

Figure 3-11 shows a basic core storage operation and data flow. The sequence of events in a core storage cycle is shown by the circled numbers and the timing chart in Fig. 3-12. A storage cycle is divided into two equal parts: read-out (fetch) and write (store). The first three steps are the same for both the read operation and write operation. An address is sent from the processing unti to storage and is decoded in the storage unit to form the X and Y coordinates of the selected location in storage.

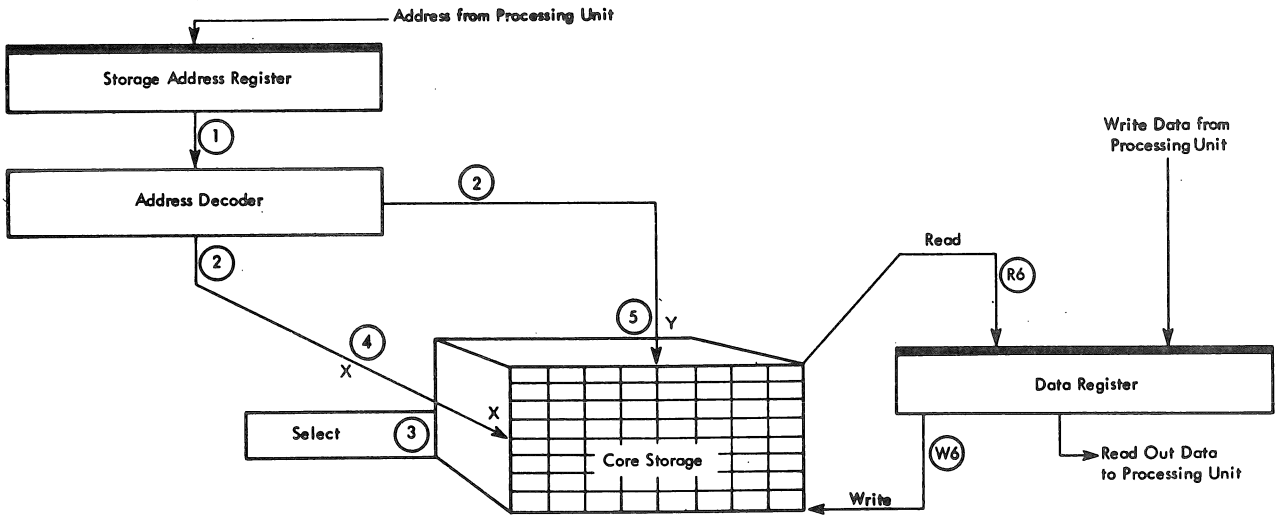


Figure 3-11. Core Storage Operation -- Data Flow and Addressing.

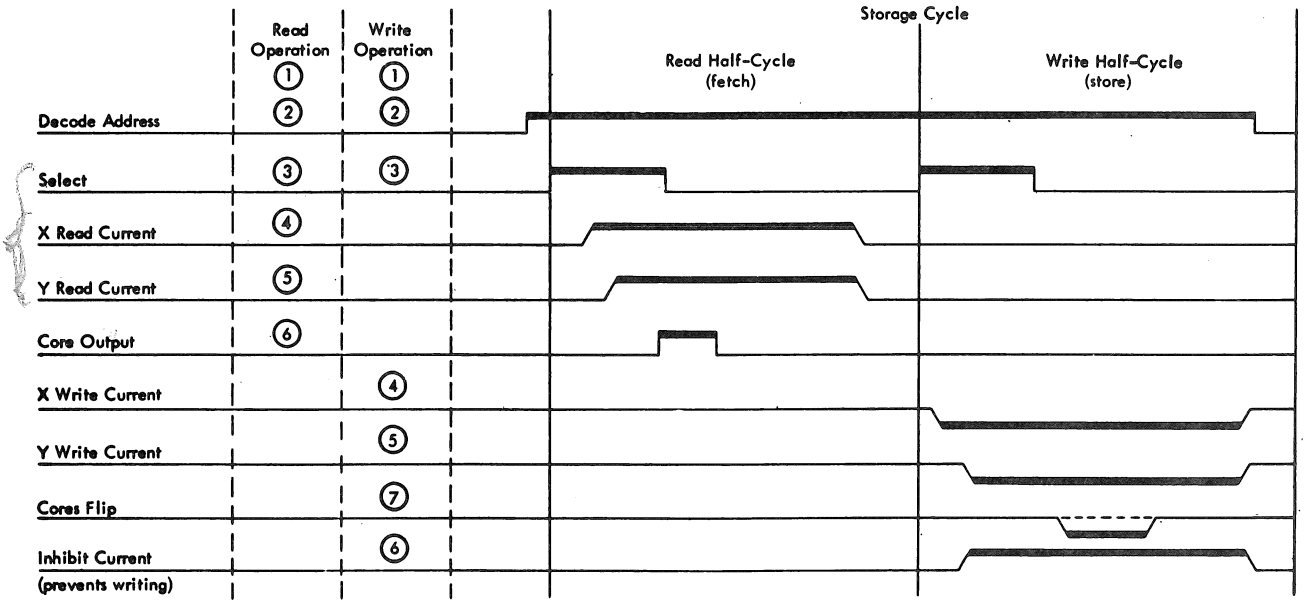


Figure 3-12. Typical Core Storage Cycle.

3-10. READ OPERATION

In a read (fetch) operation, the contents of the selected location are placed in the storage data register for use by a Computing Element or Input/Output Control Element. Because all cores are set to 0 during read, the read operation destroys the information at the selected address (destructive read-out), if the original information is to remain at the same core storage address, the information must be replaced.

Therefore, the write half-cycle necessarily follows the read half-cycle. In a read operation, the write half-cycle places the original information in the storage data register back into the arrays.

3-11. WRITE OPERATION

To write (store) new information into the storage unit, the processing unit places a word in the storage data register. The storage unit goes through a read operation to reset the cores at the selected location to 0's, but the word that is read out is not allowed to go to the storage data register. Instead, the new word from the processing unit is transferred from the storage data register into the selected location. Words pass through the storage data register both on the way into and out of the storage unit.

3-12. 7251 DATA FLOW

Data flow in the 7251-03 (Fig. 3-13) consists of moving words into the arrays and taking them out again when a computing or input/output control element needs them. Words from up to three Input/Output Control Elements (IOCE) or from up to four Computing Elements (CE) can be gated to the input switch in the Storage Element. Priority controls determine which of the inputs to the input switch are to be gated into the Storage Element. See "Priority Controls" section.

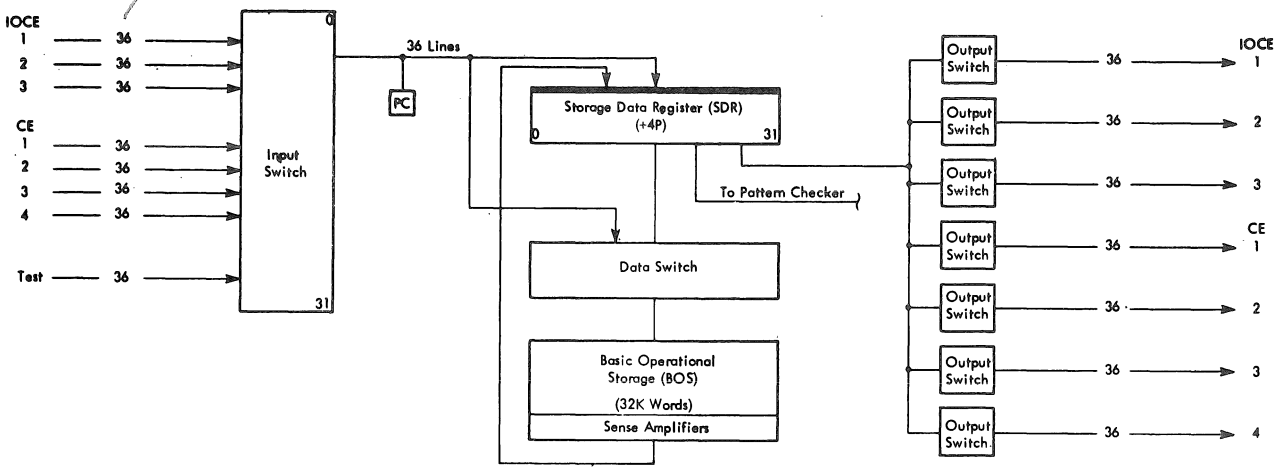


Figure 3-13. Main Storage Element Basic Data Flow.

During normal fetch cycles, data is read from the BOS into the storage data register where it is available to external elements through the output switch. The word in the storage data register is regenerated back into the addressed location in the arrays.

NOTE: Because CEs, IOCEs, and SEs each contain a Storage Data Register (SDR), the one in the SE may be referred to as the Storage Element Storage Data Register (SESDR) to avoid confusion. However, throughout this manual, Storage Data Register (SDR) refers to SESDR.

Storing of information is controlled on a byte basis by byte stats, which are set by the accessing element. The word from the addressed location is read out to the storage data register (Fig. 3-14). The four bytes from the accessing element are parity checked upon arrival, and if parity is good, those bytes whose stats are on are gated from the input bus to the data switch. Input data must remain on the bus until 2,000 nanoseconds of all normal store cycles. Those bytes whose stats are not on are regenerated from the storage data register. No parity check is allowed from the storage data register in a store operation.

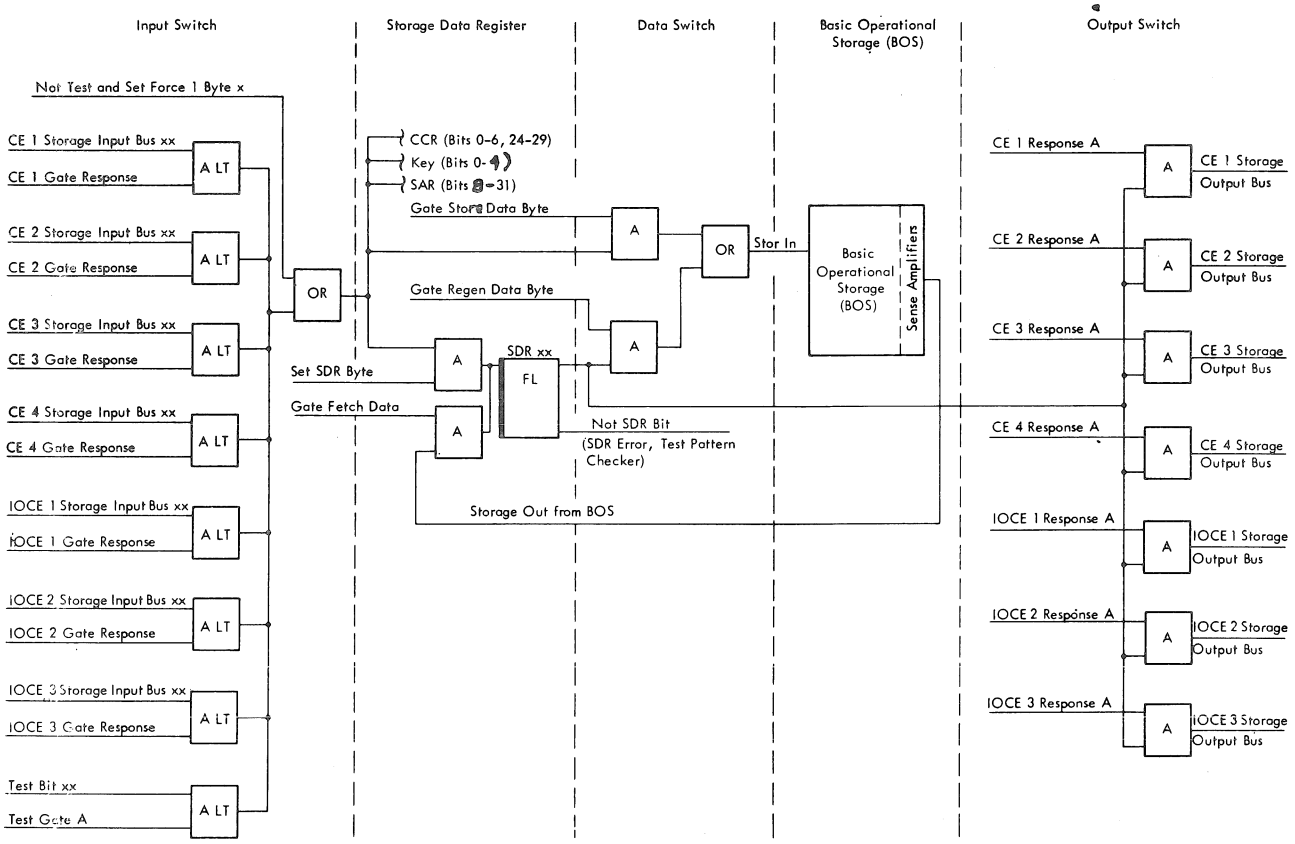


Figure 3-14. Data Flow for One Bit.

In any byte at the input bus is incorrect, all bytes are regenerated from the storage data register, and at the conclusion of the write portion of the cycle, data from the input bus are dumped into the storage data register for logout.

Outputs from the storage data register are also available to the pattern checker for testing the Storage Element off-line.

3-13. CONTROLS

Controls for moving data into and out of the Storage Element consist of configuration and priority controls, input and output switches, byte stats, an

addressing scheme, read and write latches, and a delay line clock. Configuration controls indicate the operational status of the Storage Element and with which other elements of the 9020 System the Storage Element may communicate. Priority controls set an order in which Input/Output Control Elements and Computing Elements may communicate with a Storage Element in case more than one element attempts to communicate with the Storage Element. Input switches gate data into the Storage Element from the Input/Output or Computing Element that is sending data; output switches gate data from the Storage Element to the element that is to receive data. The addressing scheme is a method for locating data in the Storage Element. Read and write latches set up circuits to take data out of the Storage Element (read) and to put data into it (write). The delay line clock times operations within the Storage Element.

The Storage Element operates asynchronously from other elements, and if not in use does not cycle, but awaits an access request from a Computing Element or Input/Output Control Element to activate the internal timing circuits. To start the Storage Element, a Computing Element or Input/Output Control Element sends an address and an access request to the Storage Element.

A. Configuration

Because there is no preferred system structure in the 9020 -- no inherent master-slave relationship -- which requires that a specific Computing Element exercise primary control over other elements, a scheme known as configuration is employed to specify:

1. Which elements of the 9020 System may exercise control over other elements.
2. Which elements may communicate with which other elements.
3. The operational capability of each element.
4. Which Computing Elements that a Storage Element may accept configurations from.

This information is retained in each element in a Configuration Control Register (CCR). Positions of a Storage Element (Configuration Control Register) are shown in Fig. 3-15. Four parts of the register are: CE, IOCE, State, and SCON. When a position of either the CE or IOCE section is on, the Storage Element may receive data from or send data to (communicate with) the corresponding element. The positions of set configuration (SCON) section of the configuration control register determine which of the Computing Elements that a Storage Element may accept configurations from.

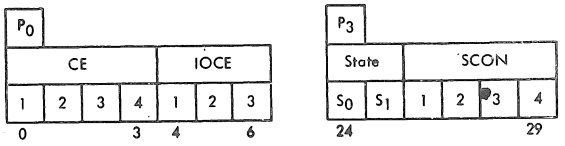


Figure 3-15. Configuration Control Register.

State is the operational capability of the element and is 3, 2, 1, or 0. Three is the highest operational state and indicates that the element is performing Air Traffic Control programs. Zero is the lowest state and is provided to accommodate maintenance.

The set configuration (SCON) instruction is the program means by which a Computing Element sets the positions of a Configuration Control Register. Positions of the register are set from positions 0-6 and 24-29 of the input bus. Two parity bits are associated with the Configuration Control Register.

B. Priority Controls

Priority controls are a group of circuits (Fig. 3-16) that set the order of accepting requests for access to storage from Input/Output Control Elements (IOCE) and Computing Elements (CE) in case more than one CE or IOCE requests access simultaneously. Except for reconfiguration requests by CEs, on

simultaneous access requests, IOCEs have priority over CEs. Within each group of elements, priority is assigned in order. For example, IOCE 1 has priority over IOCE 2. Except in the case of simultaneous requests, service is given on a first-in first-out basis. When simultaneous requests for access occur, service is given on succeeding cycles as defined by priority. Each accessing element within each group (CE or IOCE) has the same weight. Therefore, if three elements of equal priority request service simultaneously, they are serviced on succeeding storage cycles. The element serviced first is not honored for access again until the other two elements have been serviced.

A CE or IOCE (with its Configuration Control Register bit turned on in a Storage Element) that sends an access request to a Storage Element, receives a request acknowledged signal from the Storage Element to signify: (1) that the Storage Element has received the access request, and (2) that the Storage Element is configured to the accessing element.

C. Addressing

The address assigned to a word instructs the Storage Element where to put the word. In the Storage Element, addressing is a method of selecting each of the locations in the core arrays where a word can be stored and later located. Locations of bytes are consecutively numbered from zero to the capacity of storage; each numbered location is considered the address of the corresponding byte. Because Storage Elements operate with words (four bytes), storage addresses are multiples of 4.

An address where a word is to be located in the Storage Element is specified by a Computing or Input/Output Control Element. The address (24 bits) arrives at positions 8-31 of the Storage Element input switch (Fig. 3-17). From the input switch, bits 8-31 of the address go to the Storage Address Register (SAR) and bits 15-29 go also the address switch. The Storage Address Register acts as a buffer to hold the address while the parallel path from the input switch to the address switch serves to reduce circuit delay.

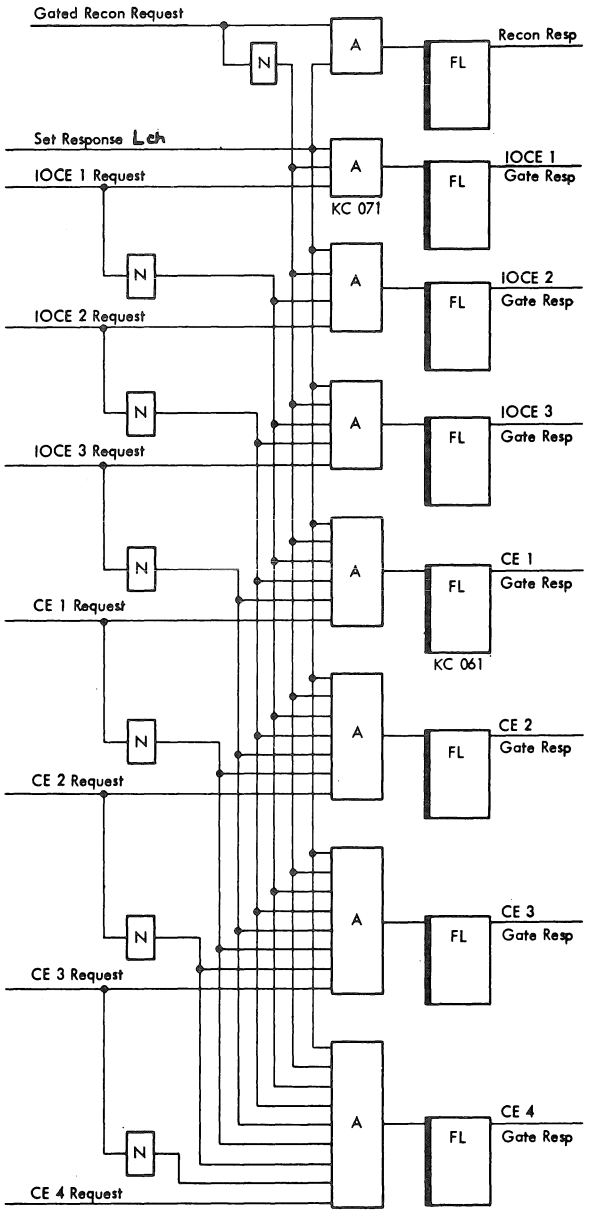


Figure 3-16. Priority Circuits.

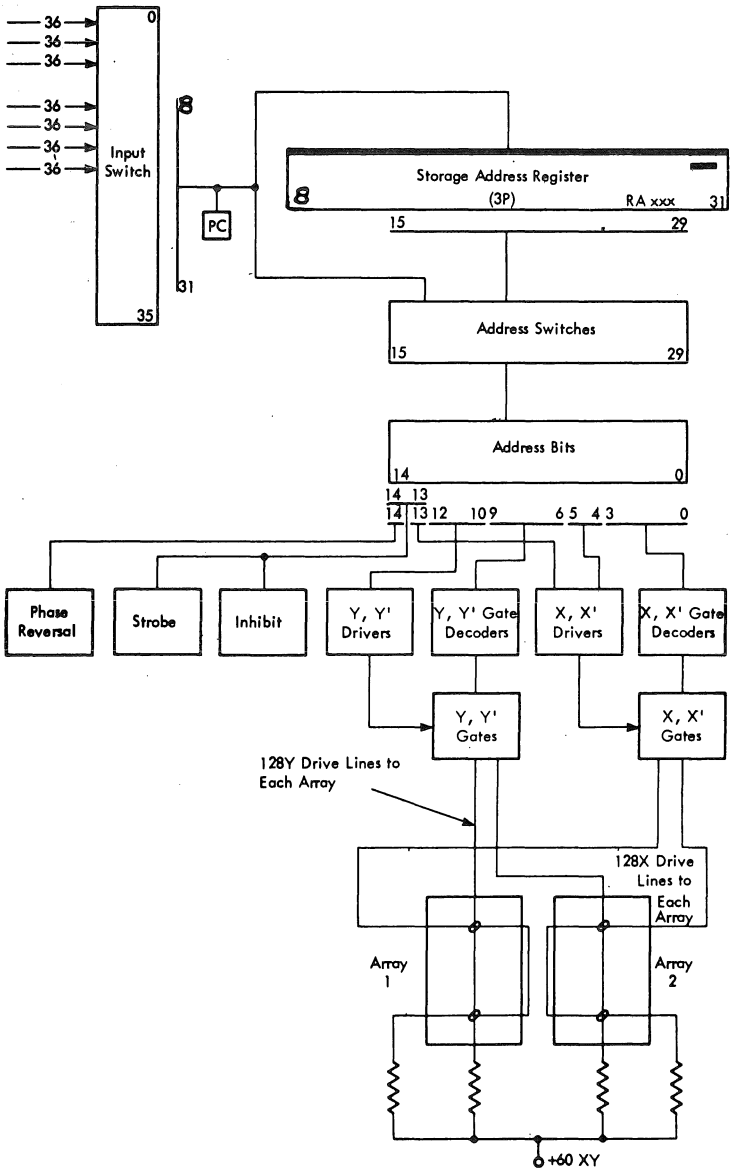


Figure 3-17. Addressing.

Bits 15-29 from the address switches become address bits 14-0 in the basic operational storage. These storage address bits are divided into two groups: one group to select the X drive lines and the other group to select the Y drive lines. Address bits 0-5 and 13 are powered and decoded to select one of 128 X drive lines in each array; address bits 6-12 are powered and decoded to select one of 128 Y drive lines in each array.

Bits 13 and 14 select segments in the arrays for strobe and inhibit, and bit 14 controls phase reversal.

Because a Storage Element operates with words, all storage addresses are multiples of 4. This is why address register bits 30 and 31 (Fig. 3-17) do not become storage address bit lines in the Storage Element.

An IBM-9020 System may have several Storage Elements, each of which contains 131K bytes. A block of 131K addresses is assigned to each storage element; this block is preset by mechanical connections and it is the responsibility of the accessing element to decode the high-order bits of an instruction or data address and to select the proper Storage Element. The Storage Element checks the high-order bits of an address received to ensure that the address lies within the selected Storage Element. A discrepancy indicates a high-order address error.

D. Integral Boundaries

Fixed-length fields, such as words, halfwords, and doublewords, must be located in a Storage Element on an integral boundary (Fig. 3-18) for a unit of information. A boundary is called integral for a unit of information when its storage address is a multiple of the length of the unit in bytes. For example, words (four bytes) must be located so that their address is a multiple of 4. Halfwords (two bytes) must have an address that is a multiple of 2, and doublewords (eight bytes) must have an address that is a multiple of 8.

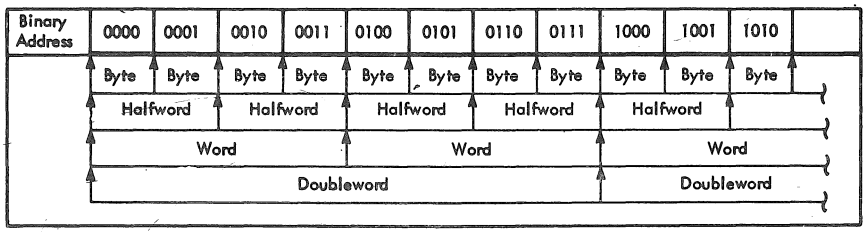


Figure 3-18. Integral Boundaries for Halfwords, Words, and Doublewords.

E. Byte Stats

To give the 9020 System the flexibility of storing individual bytes, while operating the Storage Element with four-byte words, latches in the Storage Element called byte stats 0-3 (Fig. 3-19) are set to gate byte from the input switch into the BOS. When only one byte is to be stored, the Storage Element reads four bytes out of the arrays during the read portion of a storage cycle; during the write portion of the cycle, the one byte whose stat is on is stored from the input switch while the other three bytes are regenerated to the arrays from the data register. Thus, four bytes from the SDR and input switch are combined at the data switch for storing in the arrays.

3-13. STORAGE ELEMENT TIMING

Storage Element timing is asynchronous from Computing Element and Input/Output Control Element timing; the Storage Element contains a clock to time internal operations. The clock consists of two parts; several adjstable time delay circuits and six 250-nanosecond delay lines (Fig. 3-20). The adjustable delays generate pulses to:

1. Set and reset the Storage Address Register (SAR).
2. Set and reset the response latch.
3. Degate the request latch.

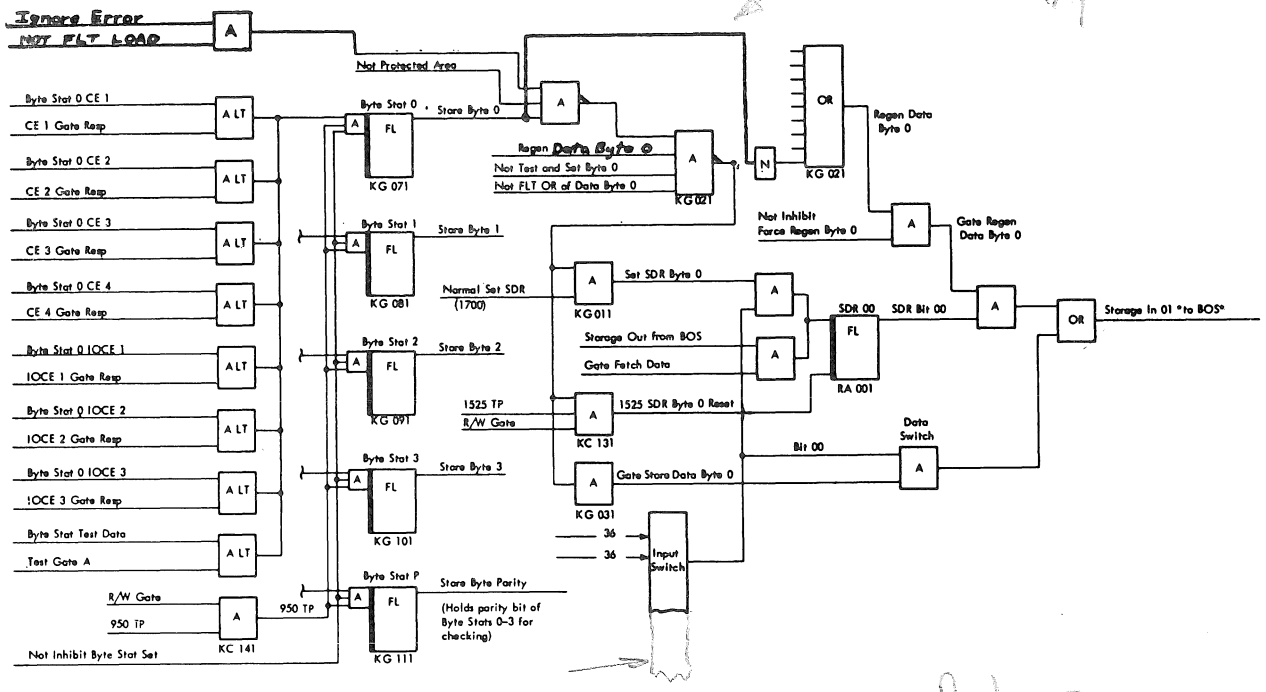


Figure 3-19. Byte Stat Latches.

The delay lines are in series and provide 125-nanosecond timing pulses with delays up to 1,500 nanoseconds in 25-nanosecond increments. By running the delay line a second time, timing pulses are generated for the second half of the 2.5-microsecond cycle.

An access request pulse from an external element starts a Storage Element cycle and the Storage Element clock. A Storage Element cycle consists of two parts: read-out (fetch) and write (store). The access request becomes a start clock pulse to start the clock for the first half of a cycle. At 140 nanoseconds, the first output from the delay line sets the read latch which serves as a gate to timing pulses for a read-out or fetch half-cycle. With the read latch on, the write latch is set at 1, 175 nanoseconds. When the write latch comes on, the delay line is started for the second half (write or store portion) of a cycle. Thus, for the delay line clock, the write portion of a cycle starts before the read portion ends. By running the delay line a second time, pulses delayed up to 2,650 nanoseconds are generated from a delay

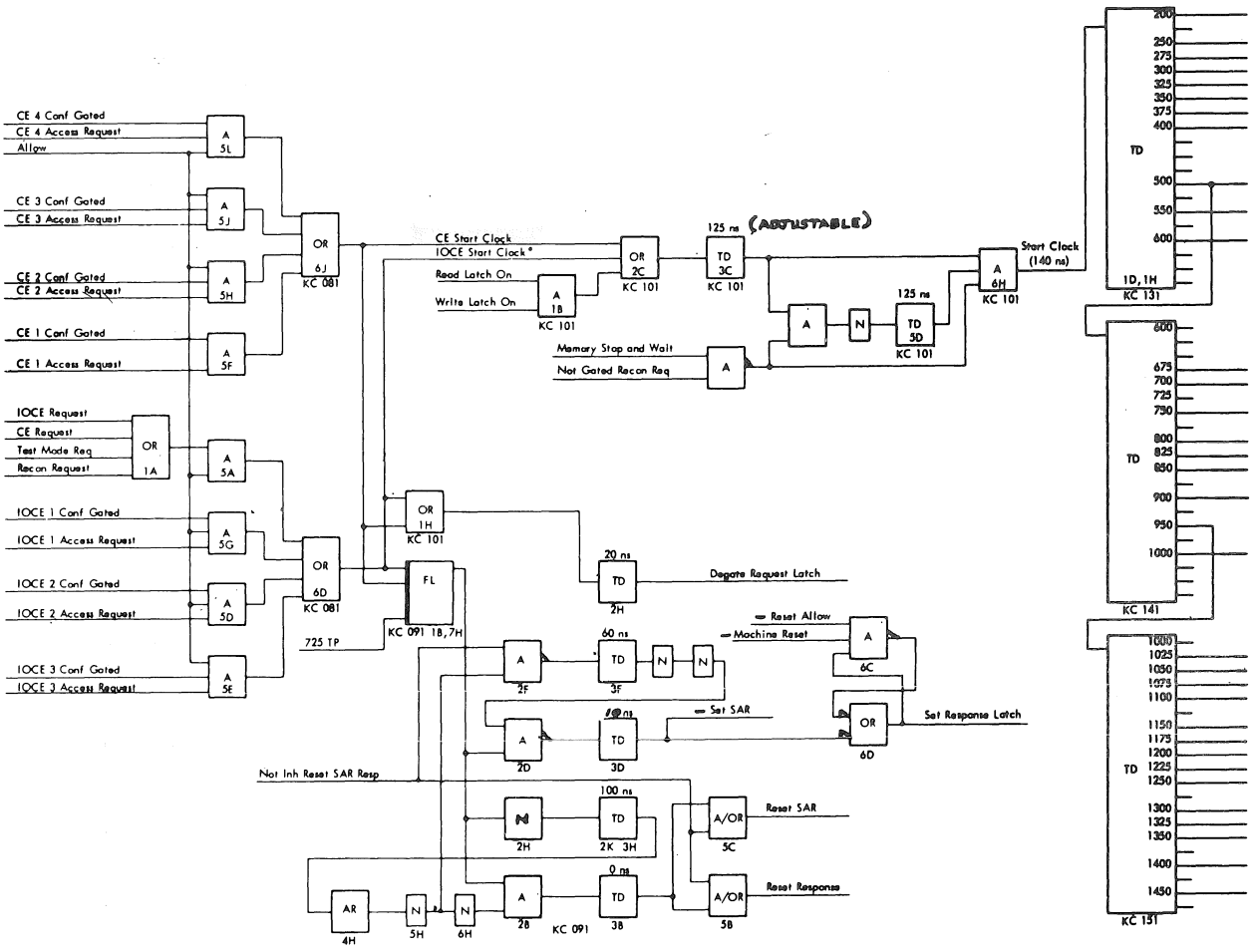


Figure 3-20. Storage Element Clock.

line of 1,500-nanosecond duration. Pulses to set and reset latches and registers are tapped off the delay line at various times and are gated by read or write for the read and write portions of a cycle.

Figure 3-21 lists the timing pulses in the Storage Element and the type of operation in which they are used.

During store cycles, the Storage Element may operate with the read and write portions of the cycle separated by a 75-nanosecond delay. This is called a split cycle and occurs only when called for by the accessing element. Because

Clock Pulses Read	(Actual Timing)	Read	Write	Split Cycle	Recon-figure	Checking and Storage Protect	Manual Test
00	Access Request	*					
00	Reconfigure Request				*		
55	Degate Request Latch	*					
80	Set SAR	*					
90	Reset SAR	*					
140	Set Read Latch	*					
280	Set Accept Latch	*					
280	Gated Recon Request				*		
290	Set Select	*					
360	Reconfigure Response Latch				*		
400	Reset Allow	*			*		
500	Gated High-Order Address Check					*	
560	Reset Test Timer Latch						*
560	Reset Test Position Check Latch						*
560	Set Storage Check Gate					*	
640	Reset Select Latch	*					
700	Block Parity					*	
725	725-950 Set Config Register				*		
760	Set R/W Gate	*					
775	Reset Config Register				*		
825	Set Split Cycle Latch			*			
950	Set Byte Stat Latches	*					
800	Set Gate Data Latch	*					
1000	Set Protected Area Latch					*	
1050	Set FLT Load Latch					*	
1100	Set Input Data Check					*	
1100	Reset Block Parity Latch					*	
1125	Reset Input Data Check Split Cycle			*			
1160	Sample Byte Stat Check	*				*	
1200	Sample Input Data Check	*				*	
1125	Reset Accept	*					
Write							
1275	Set Write Latch		*				
1275	Sample Input Data Check (Split Cycle)			*		*	
1200	Reset Accept (Split Cycle)			*			
1250	Set Write Latch (Split Cycle)			*			
1300	Sample Fetch Data	*					
1325	Reset Recon Mode				*		
1350	Set Write Condition		*				
1400	Set Select		*				
1450	Set Allow				*		
1525	Reset SDR Bytes 0 and 1		*				
1550	Reset SDR Bytes 2 and 3		*				
1560	Reset Read Latch	*					
1600	Reset Gate Data Latch	*					
1600	Set Error Stop Latch					*	*
1700	Reset Request Latches	*					
1750	Set SDR (Normal)		*				
1750	Reset Select Latch		*				
1825	Reset Ripple Counter						*
1900	Set Stop Latch					*	*
1930	Reset R/W Gate	*					
2100	Reset Run Mode Latch						*
2100	Gate Ripple Counter Latches On						*
2350	Set Allow		*				
2400	Reset Write Latch		*				
2500	Reset SDR Error					*	
2650	Set SDR Error					*	
2650	Reset Storage Clock Error					*	

Figure 3-21. Storage Element Timing Pulses.

the pulse cannot be stopped when traveling through a delay line, the delay is created by the split-cycle latch. This latch prevents setting the write latch until 1,250 nanoseconds and also degates normal clock pulses to: reset the input data check latch, sample byte stat check, and reset the accept latch. Clock pulses that are 75 nanoseconds later in time than the normal pulses are gated out by the split-cycle latch to perform these functions.

A. Basic Operational Storage (BOS) Timing

BOS timing is asynchronous from the Storage Element timing because the BOS contains a delay line clock (Fig. 3-22) for control of drive line, inhibit, and strobe timing circuits for the arrays. The BOS delay line clock is started by a select pulse, from the Storage Element clock, which fires a 135-nanosecond singleshot. The 135-nanosecond pulse travels through the delay line and can be tapped off at any of 60 taps at 25-nanosecond increments. A delay line with 5-nanosecond increments is provided for a finer adjustment in timing the strobe pulse. The master reset latch regenerates the 135-nanosecond pulse in case it degenerates in traveling through the delay line.

For one storage cycle (read followed by write), the BOS delay line clock runs twice: once for the read portion of the cycle and once for the write portion of the cycle. Therefore, it is sometimes referred to as the common delay line clock. Outputs of the read/write latch are used to gate the timing pulses for operations that are not performed at the same time in both the read and write portions of a cycle.

Timing latches that control other circuits in the storage unit are:

X Read/Write Terminator Gate Timing
Y Read/Write Terminator Gate Timing
X Read/Write Driver Timing
Y Read/Write Driver Timing
Inhibit (Z) Timing
Strobe Timing
Bump Driver Timing

Connection of the timing latches to clock outputs is shown in Fig. 3-22.

B. Read/Write Controls

Storage operations consist of two operations: read (fetch) and write (store). Once an access request for a fetch or store operation has been accepted by a Storage Element, the Storage Element performs a complete cycle in which either the fetch or store operation is accomplished. Read takes data out of the array for use by a Computing or Input/Output Control Element, and write puts data into the arrays. In an IBM-9020 System, the external element controls whether the operation is read or write by the setting of a byte stat latch for each of the four bytes contained in the word at the addressed location. For a fetch operation byte stats are not set, and the word from the addressed location is delivered to the data register where it is available, through the output switch, to the element that request access.

In a store operation, the word from the addressed location of the arrays is delivered to the Storage Data Register. Each of the four bytes that has its byte stat turned on is gated from the input bus through the data switch into the arrays. The bytes with byte stat latches off are gated from the Storage Data Register through the data switch into the arrays. Input data must remain on the bus until the Storage Element has completed the store operation.

Each of the four bytes from the accessing element is parity checked. If any byte has incorrect parity, all bytes are regenerated from the Storage Data Register; and at the conclusion of the write portion of the cycle, the bytes on the input bus are dumped into the Storage Data Register in preparation for logout.

The read latch is set at 140 nanoseconds of the cycle and the write latch is set at 1,175 nanoseconds of the cycle (Fig. 3-23). These latches control outputs of the Storage Element delay line clock. The read/write gate latch gates a timing pulse at 1,350 nanoseconds to turn on the write condition latch in the Storage Element. The write condition goes to the BOS and to storage protection to control the direction of drive currents through the arrays.

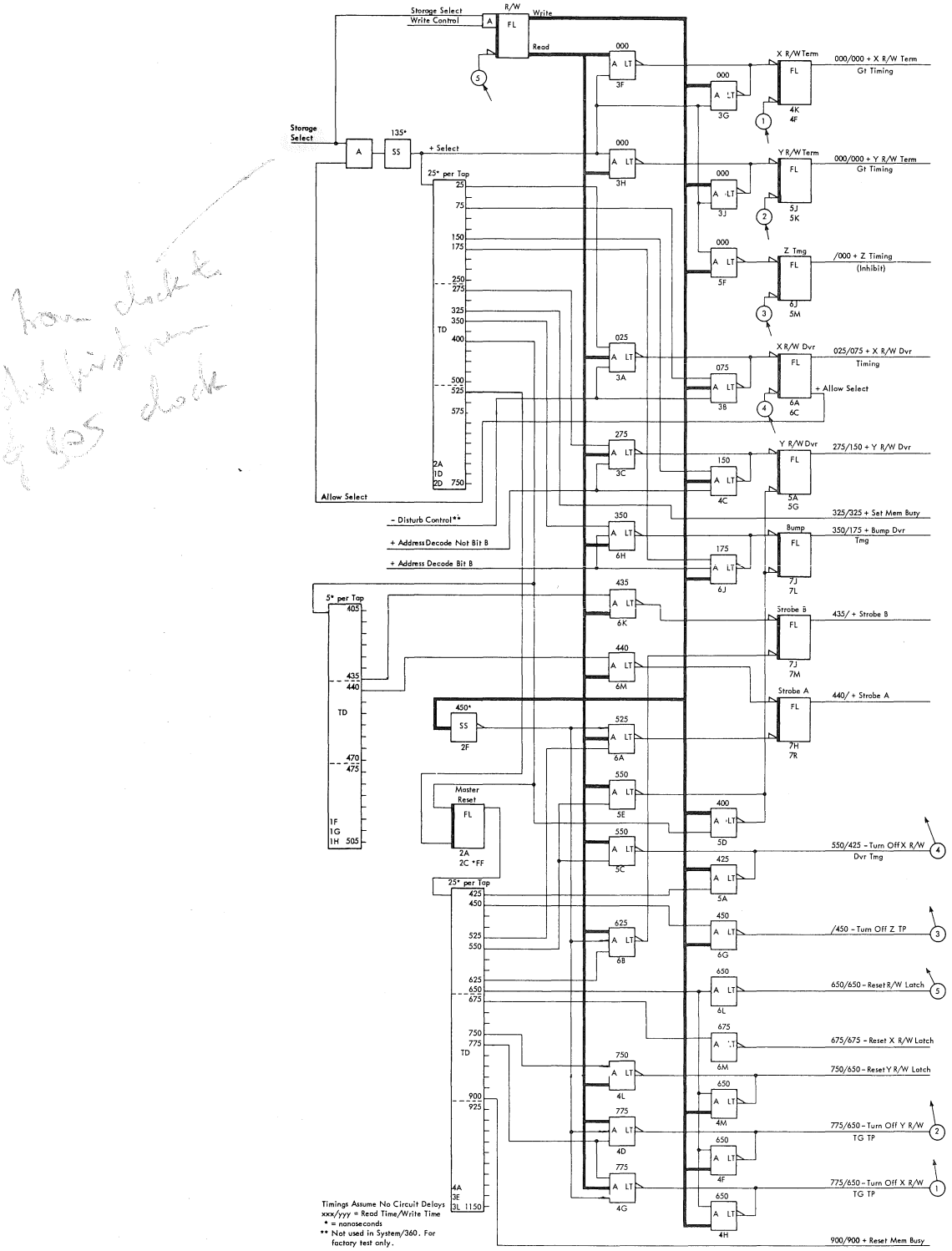


Figure 3-22. BOS Timing Logic (MA011 - MA041).

3-14. STORAGE PROTECTION

Storage protection is provided to protect the contents of certain areas of storage from destruction due to storing of erroneous information during the execution of a program. Similarly, fetch protection is provided to protect a program from making erroneous use of the contents of certain areas of storage as data or instruction. This protection is achieved by identifying blocks of storage with a storage key and comparing this key with a protection key supplied with the data to be stored (Fig. 3-24). The detection of a mismatch results in a protection interrupt.

For protection purposes, main storage is divided into blocks of 2,048 bytes. A five-bit storage key is associated with each block. When data are stored in a storage block, the four high-order bits of the storage key are compared with the protection key. When data are fetched, the fetch-protection (fifth or low-order) bit is inspected. When the fetch-protection bit from the SP array is 1, the four high-order bits of the storage key are compared with the protection key. The protection key of the current PSW is used as the comparand when a storage access is specified by an instruction. When a storage access is specified by a channel operation, a protection key supplied by the channel is used as the comparand. The keys match when they are equal or when either one is 0.

The storage key is not part of addressable storage. The key is changed by the set storage key instruction and is inspected by the insert storage key instruction. The protection key in the PSW occupies bits 8-11 of that control word. The protection key of a channel is recorded in bits 0-3 of the channel address word, which is stored as a result of the channel operation. When a protection mismatch due to an instruction is detected, the execution of the instruction is suppressed or terminated and the program execution is altered by an interruption. The contents of the protected storage location always remain unchanged on a storage-protection violation and are never loaded into an addressable register or moved to another storage location on a fetch-protection violation.

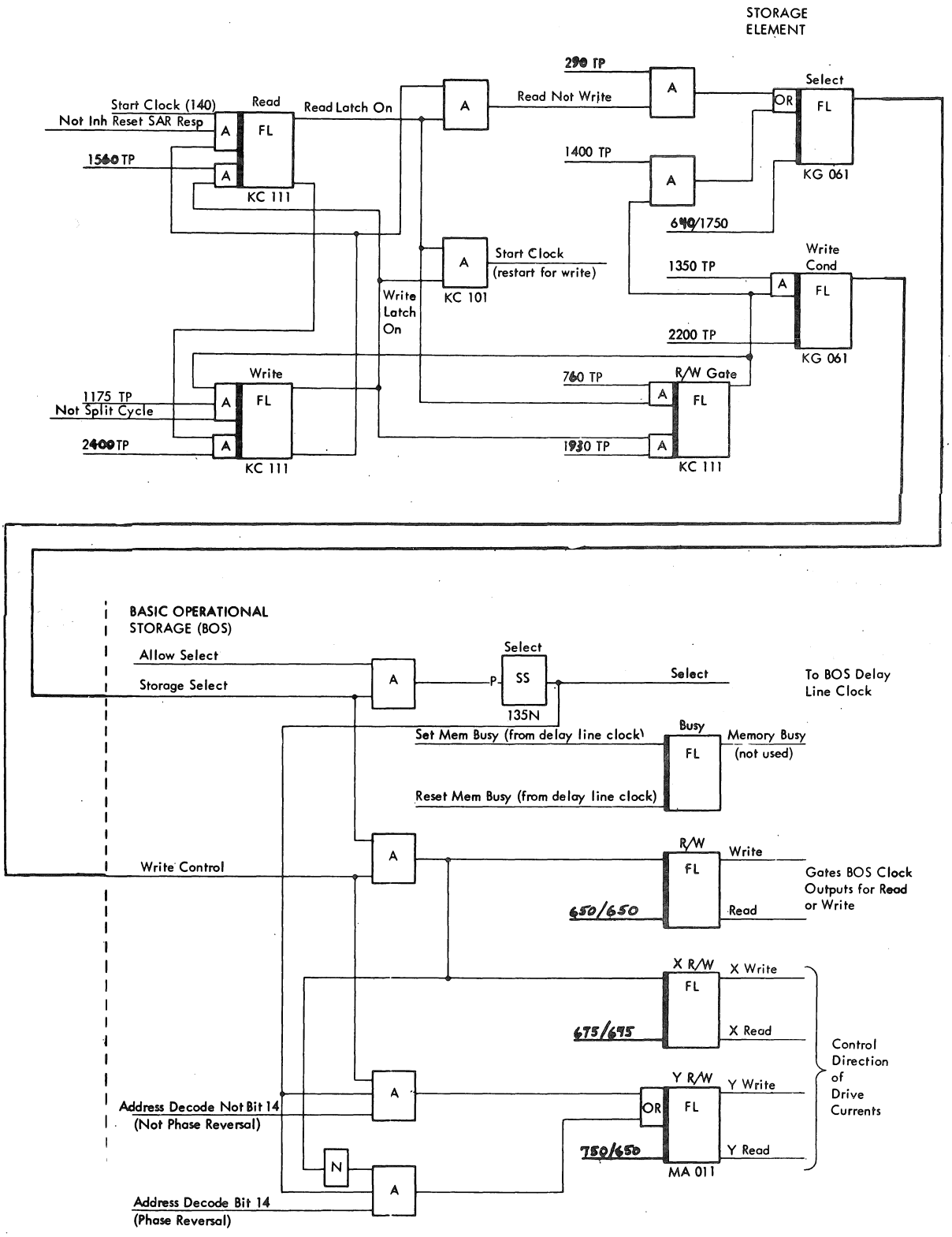


Figure 3-23. Read/Write Controls.

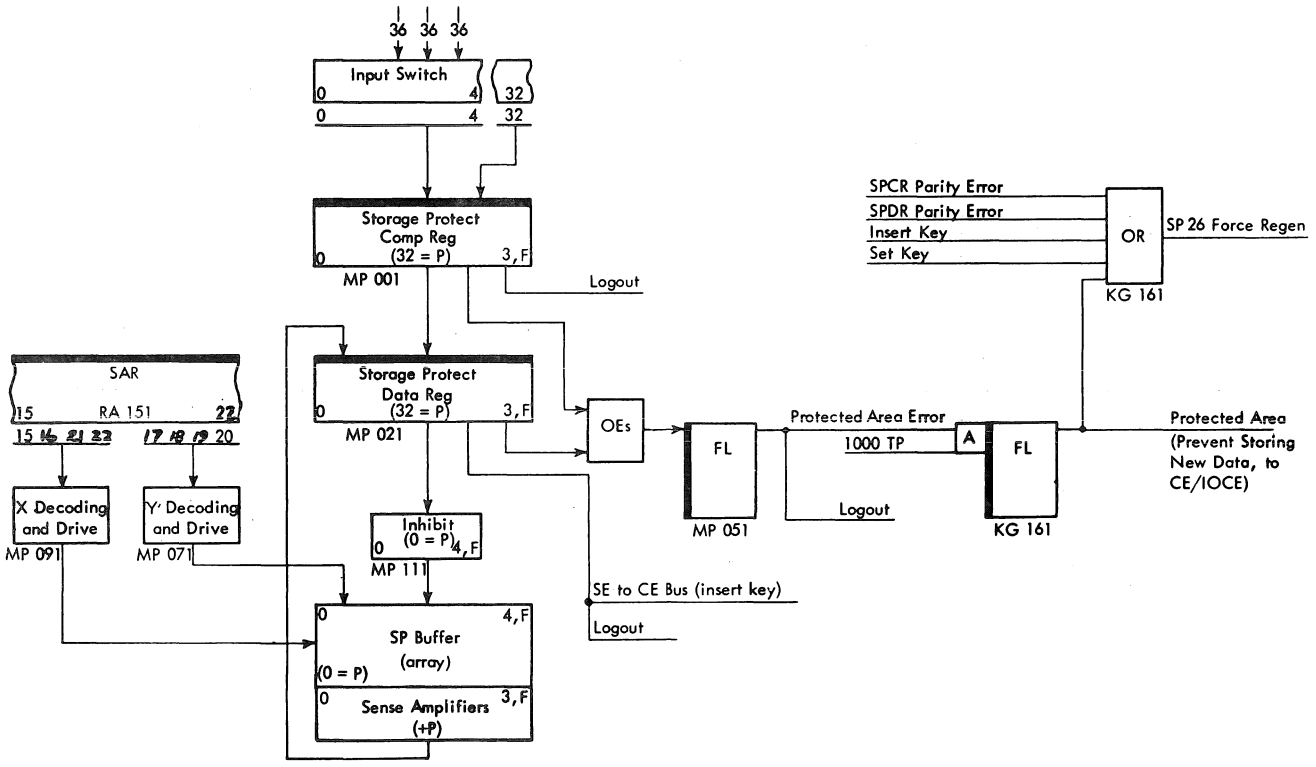


Figure 3-24. Storage Protect.

3-15. LOGOUT

Logout is the capability of an element to transmit information that is held in latches and registers to a CE for monitoring and error detection. When an error is detected by the SE, a storage check signal is sent to the accessing CE to request a logout. The Storage Element then pauses for 2.5 microseconds, awaiting a logout stop command from an IOCE or CE. The SE sends an element check and a logout stopped signal to all CEs and inhibits the memory from starting another cycle.

Five or more microseconds after the receipt of the logout stopped signal from the SE, and CE may send a logout proceed signal to interrogate the latched information. The SE remains logout stopped until a CE sends a logout complete signal to the SE. Logout complete resets all request latches in the SE. Data logged out is sent to all CEs.

Logout of an SE requires five words (Fig. 3-25). Execution of a reconfigure cycle prior to logout may alter the configuration control register and the indication of the unit last accessing the Storage Element.

The logout stop and logout complete signals are degated by CE gate and hi test (isolated test conditions).

3-16. TEST AND SET

Test and set is an instruction performed only by CEs. The instruction fetches one byte of data from storage and tests the leftmost bit of the byte for a 0/1 condition. As a result of the test, the condition code is set to a 0 or 1, respectively.

To obtain the byte, the Storage Element fetches a word from the BOS. Positions 30 and 31 of the storage address determine which byte of the word to send to the CE. As this byte is returned to the BOS, all nine bits are forced to 1's.

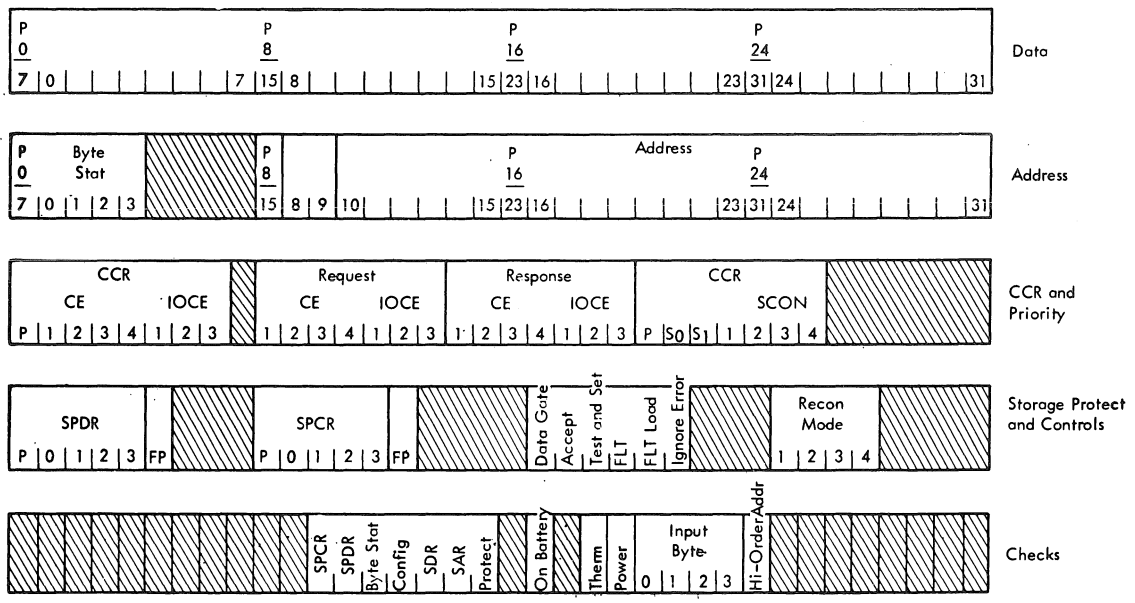


Figure 3-25. Storage Element Logout Formats.

The other three bytes of the word are returned to the BOS from the Storage Data Register.

Test and set controls the use of common data or tables by more than one CE. For an example of test and set, refer to the Field Engineering Manual of Instruction, IBM-9020 System Introduction, Form Z22-2860.

3-17. ERROR CHECKS

Seven types of check signals may be generated by error conditions:

Element Check
Storage Check
Protected Area
Logic Check
Power Check
On Battery
Emergency Power Off

A. Element Check

An element check is sent to all attached Computing Elements. Other functions within the SE are unaffected by the signal, but normal operation cannot be guaranteed. A constant element check is generated by the following:

Logout Stopped Signal
Overcurrent on any supply
Overvoltage or Undervoltage on any supply
Normal Power Off, Master Power Off, or Loss of any Voltage

A pulsed element check (10 microsecond pulse) is sent to all attached CEs for the following conditions:

Incorrect Configuration Register Parity
Marginal Temperature
Catastrophic Temperature
On Battery
Storage Check (parity)

CE looks at ILOS bit in CCR

Other functions within the SE continue to operate normally.

B. Storage Check

see also page 1-75

The SE can request logout by sending a storage check signal to the accessing CE at the time an error is detected. Storage check is generated by parity check errors with the exception of Configuration Control Register parity checks. The SE pauses for 2.5 microseconds following completion of the cycle in which the error was detected. If logout stop has not been signaled by an attached CE, the SE proceeds following the pause and error information may be destroyed.

If Logout stop is received the SE stops and logs out

The SDR, SAR, SPDR, SPCR, and input bus are parity checked on a byte basis. The output from checking the input bus is available to logout on a byte basis and the output from check the registers is available to logout on a word basis.

Any detected parity or address error is sent to the accessing element and the SE is forced to perform a regen cycle. If any byte at the input bus has bad parity, all bytes are regenerated.

The SDR is parity checked on all fetch cycles. The SDR parity check output is disabled on all normal store cycles, ISK, SSK, FLT op, and suppress log check cycles. If the SDR has incorrect parity, it is not corrected, but is placed back in the arrays with incorrect parity.

The SPDR is parity checked under the following conditions:

1. ISK and SSK cycles
2. When the SPCR is not all zeros and
   a. the SE is executing a store cycle or
   b. any cycle when the fetch protect bit is on in the SP array.

Byte stat parity is checked on all cycles except ISK and SSK cycles. The SPCR is parity checked on all cycles. Input data parity is checked on all cycles except FLT op, suppress log check, and fetch cycles. SAR is parity checked on all cycles. Address checking also occurs on all cycles.

C. Protected Area

In general, a protected area violation is generated when the four data bits of the key sent by the accessing element do not match the four data bits of the key from the SP array. This violation is suppressed on ISK and SSK cycles. The conditions for issuing a protect check vary when the cycle is taken under ignore error.

On a non-ignore error cycle, a protect check is issued for the following conditions:

1. Non ISK and SSK cycles when the keys match (are identical or either one is all zeros) with correct parity in both keys and
   a. the SE is executing a store cycle or
   b. any cycle when the fetch protect bit is a 1 in the storage protect array.

In ignore error cycles, a protected area signal is generated the same as in non-ignore error cycles and also under the following conditions:

1. The keys do not match and incorrect parity is in either or both the SPCR and SPDR, and the key at the input bus is not all zeros. This signal is suppressed during SSK and ISK cycles.

D. Logic Check

A logic check signal is sent to the System Console whenever the storage check line is active.

E. Power Check

Power check is sent to the System Console whenever the following conditions are present:

Marginal or Catastrophic Temperature
Overvoltage
Overcurrent
Normal Power Off or Loss of Power
Voltage or Master Power Off (MPO)
Undervoltage

F. On Battery

An on battery signal is generated whenever the SE transfers from main line to battery power.

G. Master Power Off

A master power off signal is generated whenever the MPO switch is activated.

3-18. STORAGE ELEMENT TESTING

The testing of the SE could be broken down into two classifications, i.e., OFF-LINE testing and ON-LINE testing. Since the SE is isolated from external control via the engineering control panel when it is not in state zero with the test switch on, the SE can only be controlled by system programming and is said to be ON-LINE When the SE is in state zero with the test switch on, it is isolated from the system and can only be controlled from the engineering

panel. This is referred to as being OFF-LINE. The following discussion will attempt to point out the various facilities available from both types of testing when troubleshooting checks on the SE. The discussion will not attempt to detail all procedures, but it will present a general discussion sufficient to enable the technician or engineer to have a general understanding of the testing available.

A. OFF-LINE Testing

Refer to Fig. 3-26, note the switches in the lower right hand corner of the engineering control panel. There is one switch which is labeled Normal and Test. This is the ON or OFF-LINE switch when the SE is in state zero. If this switch is in the TEST position and the SE is in state zero, the SE is isolated from the system and is in the OFF-LINE condition. In this condition all the remaining switches are enabled and the SE can be controlled from the engineering panel.

When the SE has had a check or malfunction, probably the first thing that should be checked are the various monitor indicators at the top of the engineering control panel, refer to Fig. 3-26. Such things as parity error, protection check, high order address check, configuration, state, etc., can be analyzed. Once this information is noted the SE, if in zero state, can be tested from the engineering panel.

An example of store operation is demonstrated by the following:

1. Place the Store-Fetch switch in the Store position, the Normal-Single Cycle switch in the Single Cycle position, place the address of the desired location in the IAR keys, place the desired data to be stored in the SDR keys, place the Storage Select Rotary switch to the Data Switch position, depress Reset and depress depress Start.

2. One can determine if the store was completed by placing the Store-Fetch switch to the Fetch position, depress Reset and depress Start.

Many other tests, controls, and monitor facilities are available on the engineering control panel located on the inside gate and on the maintenance panel located on the front of the SE frame. A summary of these are listed below under the sub-topics: "Indicators", "Switches", and "Rotary Switches". (Refer to Figs. 3-26 and 3-27.)

a. Indicators

Title	Number of Indicators
Storage Data Register	36
Storage Address Register	27
Storage Protect Data Register	6
Storage Protect Compare Register	6
Configuration Control Register	15
Priority Status Request	7
Priority Status Response	7
Error Detection (2 spares)	12
Byte Stats	5
Controls	6
Run (active only in test state)	1
*Element Status	4
*Marginal Off Normal -- Indicates that the corresponding margin check potentiometer has been set off normal.	3
*Main Line On -- Indicates that primary power is present at the input of the SE power wall.	1
*Thermal Check -- Indicates that the temperature is marginal or a high temperature condition exists. Remains on with a high thermal condition.	1
*Power Check -- Indicates that an overvoltage, voltage marginal, overcurrent, or high thermal condition exists within the SE.	1

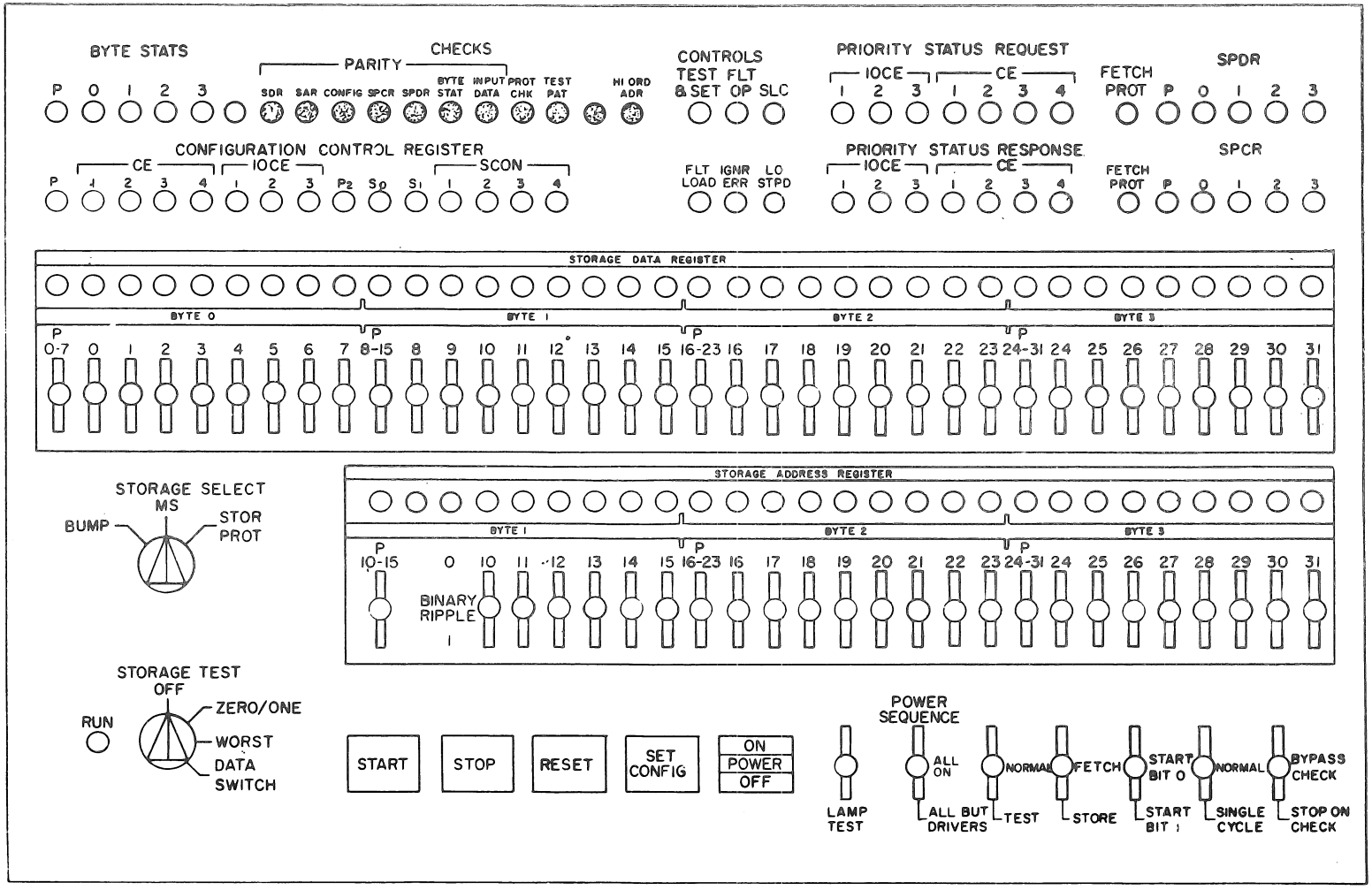


Figure 3-26. 7251-03/04 Maintenance Panel.

Title	Number of Indicators
*Battery - Indicates that the Storage Element is on battery power.	1
*Power Sequence Complete -- Indicates that both logic and special voltages are present in the SE. If the option to sequence power only through logic voltages is exercised, this indicator will not be lighted.	1
*CB Tripped -- Indicates that a circuit protector has been tripped. In the SE, this indicator signifies only that the blowers are not operating.	1
*DC On -- This indicator is active whenever the SE logic voltages are on, exclusive of the memory special voltages.	1

*All the above Indicators indicated by an asterisk are located on the power control panel on the front of the SE Frame. (See Figure 3-27.)

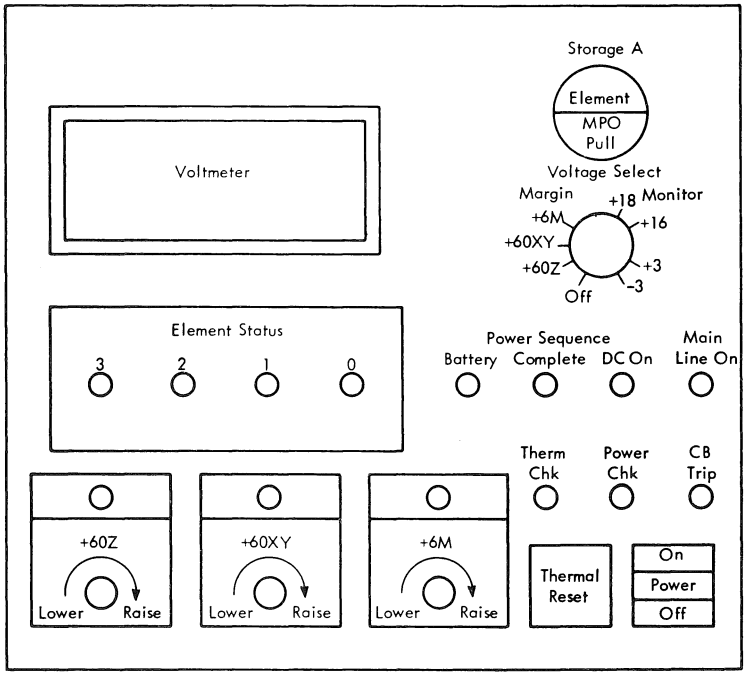


Figure 3-27. Power Control Panel.

b. Switches

All manual switches and pushbuttons on the SE Maintenance Panel are under control of the S_0 and S_1 bits and the test switch with the exception of the lamp test switch. The test switch is active only when S_0 and S_1 are off.

On the power control panel the monitor and element select switches are always active so voltages may be monitored in any state. The marginal test potentiometers and thermal reset switches and element master power off are always enabled.

The power on/off is enabled only in state 0 with the test switch on.

c. Pushbuttons

Title	Description	Number of Buttons
Set Config	Gates contents of appropriate data switches to configuration register.	1
Start	Initiates a storage cycle. Further operation is controlled by the status of other switches.	1
Stop	Stops storage cycles at end of current cycle.	1
Reset	Resets all error indications and storage registers to 0's; stops any operation at end of write portion of cycle. Resets CCR.	1
*Therm Reset	Resets relay picked when a thermal fault is detected in an SE.	1

d. Rotary Switches

Title	Description	Number of Switches
*Monitor (7 position)	Selects voltage for display on the maintenance panel voltmeter.	1
*Marginal Test	Allows a marginal voltage to be varied around its nominal value (potentiometer).	3
Storage Select (3 psn)	Selects one of three SE areas to be exercised. These areas are: bump area of main storage, main storage locations themselves, and storage protect.	1
Storage Test	Gates a pattern generator to allow various combinations of data to be entered into core to facilitate testing. The following patterns are used: Zero/One--Test pattern all 0's or all 1's are used as controlled by the start bit 1/ start bit 0 switch. Worst--Worst case pattern is used. Data Switch--The data switches may be used to enter random bits into a word. Byte parity must be correct or data checks will occur. Off--Switch in this position enables the operator to regenerate existing information.	1

e. Level Switches

Title	Description	Number of Switches
*Power On/Off	Utilized by maintenance and power control panel. Sequences all voltages up and down in SE.	2

Title	Description	Number of Switches
Power Sequence all on/ all but drivers	When set to off position, stops power up sequence prior to turn on X-Y and Z voltages.	1
Lamp Test	Tests all SE logic indicators.	1
Data Switches	Used in combination with storage test switch to enter data into SDR. Also used to set configuration register for off-line testing. Allows storage of invalid bytes in test status.	1
Address Control Switches	Used to gate bits into SAR for repeated accessing of one or more addresses.	25
Error Check Switch Bypass/Stop on Error	Setting switch to stop position enables normal error checking. Setting switch to bypass forces output of error logic to maintain a constant no error status.	1
Cycle Rate Switch Normal/Single Cycle	In normal status, storage will run continuously, once started, until stopped by error or the stop or reset pushbutton. In single cycle, storage will take one read/write cycle and stop.	1
STT Bit Zero/One	Defines information to be stored in core in combination with storage test switch. (See above.)	1
Normal/Test Mode	Activates manual switches in 0 state and provides isolation from all other system elements.	1
Cycle Control Switch Store/Fetch	Fetch position allows contents of storage to be regenerated only. Store position allows contents of storage to be changed under control of storage test switch.	1

f. Miscellaneous Maintenance Panel Items

Title	Description	Number of Items
*Voltage Meter	DC voltmeter used to monitor all voltages used in SE.	1
*Master Power Off	Red handle pull type switch that drops all power in the SE. When this switch is operated, maintenance personnel action is required to restore power to the SE.	1

*All switches and controls designated by the asterisk are located on the front power control panel. (See Fig. 3-27.)

B. ON-LINE Testing

ON-LINE testing must be performed with the SE configured into a system or sub-system with an IOCE, CE, SE, and I/O device when the testing program is on MDM (Maintenance Diagnostic Monitor). When the test is on SDM (System Diagnostic Monitor), an IOCE, SE, and I/O device is required. There are also tests concerning the SE checkout on the SEVA (System Evaluation) program. To run SEVA requires a system such as a simplex, duplex, or triplex.

All of these programs or routines check out the operational characteristics of the SE and give directional error checks for use in troubleshooting the problem, if any. It might be pointed out here that while the off-line facilities available from the engineering maintenance panels provide a means for checking out the SE as an individual element. The ON-LINE tests provide better resolution of the check in the majority of cases.

For instance from the engineering panel one can determine that a bit is not being set, while possibly the ON-LINE test would locate the error and type out drive line, etc., that was not functioning properly.

Another aspect of the ON-LINE testing is that it checks the SE from the standpoint of operating within a system. For instance SEVA checks out the SE for acceptance of reconfiguration and its ability to communicate with the various IOCEs and CEs.

3-19. CE/IOCE TO STORAGE ELEMENT INTERFACE LINES

Formats of communications with the Storage Element are shown in Fig. 3-28.

A plus level (+3) on the CE/IOCE to SE bus is interpreted as a 1. A minus level (ground) is a 0. On all other SE inputs, a minus level (ground) is active.

A. CE/IOCE to SE Bus

A group of 36 lines that feed the SE input switch. The accessed SE gates the signals from the bus. The contents of the bus during the first part of the cycle are gated into the SAR (27 lines) and into SPCR (5 lines).

During the last portion of a storage cycle in which the Storage Element is executing a store operation, the contents of the CE/IOCE to SE bus are gated into the BOS and Storage Data Register (format 2). Bytes read out and not replaced by stored data are regenerated from the Storage Data Register.

Under control of the SCON instruction, the contents of the bus are gated into the Configuration Control Register. (See format 3.)

B. Access Request

Access request is a line requesting a main storage cycle. This signal must remain until the Storage Element has indicated it is honoring the request. This signal is gated by the CCR data bits.

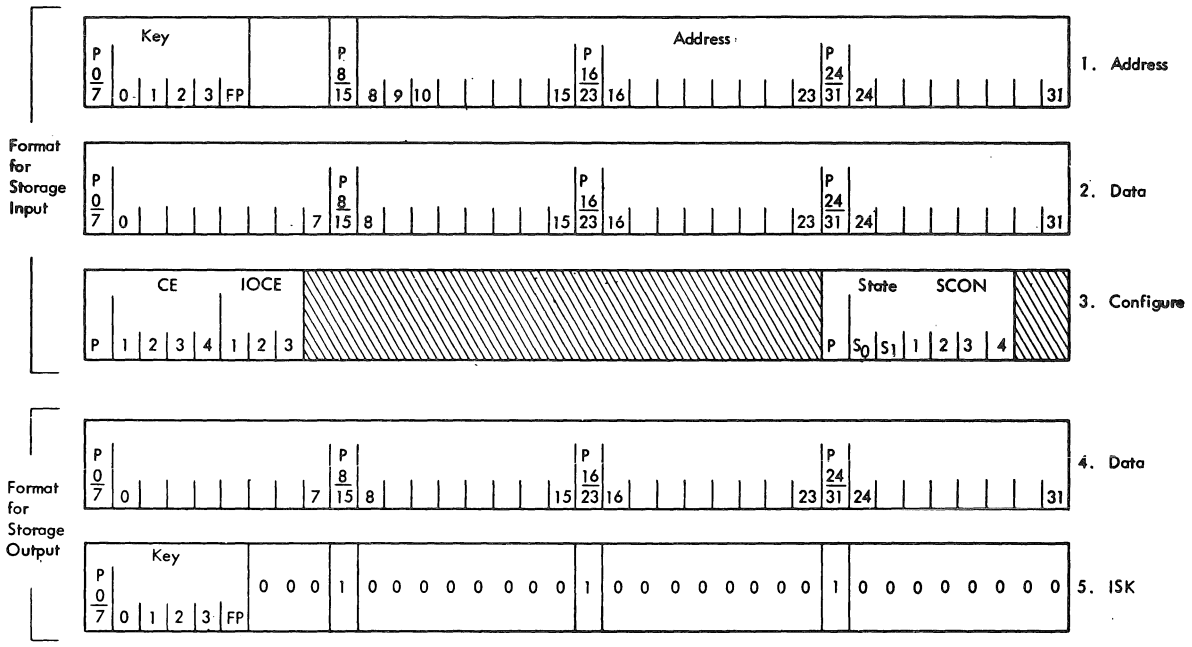


Figure 3-28. Storage Communication Formats.

C. Byte Stats

Four lines indicate whether a particular byte in main storage is to be regenerated or replaced with the data from the CE/IOCE to SE bus. A fifth line, contains parity for the byte stats. These signals are gated with the response latches.

D. Set Storage Key

The set storage key line signals the SE to store the key found on the CE/IOCE to SE bus in the storage protect buffer location specified by bits 15-20 on the SAR (format 1). The storage cycle accompanying this operation is a No-Op; that is a word is fetched from the addressed BOS location (any location within the block of 512 words associated with the key) and regenerated but no checking is done. This line is found only in the CE to SE interface. This signal is gated with the response latches.

E. Insert Storage Key

The insert storage key fetches the key from the storage protect buffer location specified by bits 15-20 of the SAR and places it on the SE to CE/IOCE bus. Accompanying this operation is a No-Op; a word is fetched from the addressed BOS location (a location within the block of 512 words associated with the key) and regenerated but no checking is done. This line is found only in the CE to SE interface. This signal is gated with the response latches.

F. FLT Op

The FLT Op line causes the suspension of checking on the SDR and input switch. This signal is gated with the response latch. This line is found only in the CE to SE interface.

G. FLT Load

The FLT load line causes the SE to OR the contents of the BOS with the data on the CE/IOCE to SE bus. OR'ing is under byte stat control. The OR'ed information is returned to BOS. This line is found only in the IOCE to SE interface. The signal is gated with the response latch.

H. Test and Set

The test and set line causes the contents of core specified by the current address to be fetched and placed on the SE to CE/IOCE bus. Contents of the byte specified by bits 30 and 31 of the address are replaced with all 1's. All other information is unchanged. Normal fetch parity checking occurs. This signal is gated with the response latches. This line is found only in the CE to SE interface.

I. Split Cycle

The split cycle line causes the Storage Element to delay 75 nanoseconds between the read and write portions of the BOS cycle. This signal is gated by the response latches.

J. Logout Stop

The logout stop line causes the Storage Element stop latch to be set. Element check is generated. No further accesses are honored. The SE stops at the end of a cycle. With the stop latch on, only logouts and configuration may take place. This signal is gated with the CCR data bit.

K. Logout Proceed 1-5

These lines cause the Storage Element to place on the SE to CE bus the contents of registers and latches. These lines are gated with the stop latch

on. All sequencing is under control of the external unit. This line is found only in the CE to SE interface.

L. Logout Complete

The logout complete line turns the stop latch off. If any unit is requesting access, the memory honors it. If an element check was generated by the stop latch turning on, the element check is reset. This signal is gated by the CCR data bit. This line occurs only in the CE to SE interface.

M. Reconfigure Select

The reconfigure select line carrys a 2.5-microsecond pulse from the CE to the SE, causing the SE to set into its configuration register the data on the CE to SE bus. This signal is gated with the contents of the respective SCON bit. This line is found only in the CE to SE interface.

N. System Reset A-B and CE Gate

Simultaneous occurance of system reset signals (-) on A and (+) on B input lines cause the SE to reset. SAR, SDR, SPCR, and SPDR all reset to zeros including parity. Error check triggers are reset. The system reset signals are not gated by the Configuration Control Register. No parity error is indicated as a result of a system reset.

All CCR SCON bits are turned on and all other CCR bits except parity are turned off.

The CE gate consists of simultaneous signals (+ on A and - on B). All other dc level conditions on A and B input lines inhibit the line from a CE. The CE gate from a CE causes the SE to allow the following input lines from that CE:

1. Access Request
2. Reconfigure

3. Logout Stop
4. Logout Complete

O. Ignore Error

The ignore error line causes the SE to ignore all action that would occur as a result of a parity or address check. However, a storage check signals the accessing unit upon detection of an error. No regeneration is forced as a result of detected error and no 2.5-microsecond wait is encountered. ELC signals are unaffected by this line.

Protected area violated signals are issued as under normal storage cycles. This signal is gated with the response latch.

P. Suppress Log Check

The suppress log check line causes suspension of checking on SDR and the input switch. The signal is gated with the response latch. This line occurs only in the IOCE/SE interface.

3-20. STORAGE ELEMENT TO CE/IOCE INTERFACE LINES

A plus level (+3) on the bus is a 1. A plus level is considered significant for all control lines.

A. SE to CE/IOCE Bus

Thirty-six lines that carry fetch data, logout data, and ISK data. Data are gated only to the accessing element during fetching.

B. Accept

Accept is a line to acknowledge the receipt of an access-request signal and to indicate that the Storage Element is executing the request. The rise of

accept indicates that the SE has stored the key and address. If this cycle is a store, data may now be placed on the CE/IOCE to SE bus. The signal is sent only to the unit whose request is being processed currently. It is gated with the response latches.

C. Request Acknowledged

A request acknowledged signal signifies that the SE has received an access request and is configured to the accessing element.

D. Gate Data

Gate data is a line to signal that data are about to be placed on the SE to CE/IOCE bus during a fetch or ISK. This line does not rise during reconfigure or logout cycle. The signal is sent only to the unit whose request is being processed currently.

E. Protected Area Violated

Protected area violated is a line brought up during a fetch or store operation in which the storage protect key sent from the CE/IOCE does not match the tag fetched from storage protect buffer, and neither tag is 0. The signal is gated with the response latches.

F. Storage Check

Storage check is a line brought up by the occurrence of a parity check, address check, or logic function check. Following any cycle (except ignore error) in which this signal is sent out, the Storage Element stops for 2.5 microseconds. The signal is gated with the response latches. A pulses ELC is sent to all CEs on any cycle during which the storage check occurs.

G. Element Check

Element check is a line to signal that one or more of the following conditions has been detected within the SE:

1. CCR Parity Check
2. Thermal Check
3. On Battery
4. Storage Check
5. Power Off
6. Logout Stop Latch On

Items 1-4, upon detection, cause a pulse to occur on the ELC line. Items 5-6 cause the SE to signal ELC until the condition has cleared. ELC is sent to all CEs and is not gated.

H. Reconfigure Response

Reconfigure response is a line to carry a pulse indicating that a reconfigure operation has been executed, and correct parity of the CCR now exists. This signal is sent to all CEs without regard to the configuration register.

I. Logout Stopped

Logout stopped is a line to signal that the logout stop latch has been set. The SE honors only requests to logout or reconfigure. This signal is issued to all elements.

3-21. SYSTEM CONSOLE TO SE INTERFACE

State 3

State 3 is a line to indicate that S_0 and S_1 of the SE configuration register are on.

State 2

State 2 is a line to indicate that S_0 is on and that S_1 is off in the SE configuration register.

State 1

State 1 is a line to indicate that S_0 is off and S_1 is on in the SE configuration register.

State 0

State 0 is a line to indicate that both S_0 and S_1 are off in the SE configuration register.

Logic Fault

Logic fault is a line to indicate that a data check, address check, key check, or protect check has occurred in the SE.

3-22. POWER INTERFACE LINES

Emergency Power Off (EPO)

1. +24 volt dc line (from the SE power supply to the console)
2. 24 volt return from console
3. The EPO control line from the console to the SE EPO contactor

Power Check

Power check is a line to the console to indicate that the temperature in the SE has drifted within 5 percent of the shutdown tolerance. The signal also indicates the loss of a voltage, a normal power off, or an element master off condition. This signal is a +24 volt dc level.

Battery

Battery is a line to indicate that the SE has switched to battery power.

3-23. LATCHES AND REGISTERS -- ALD PAGE

Latches and Registers	ALD Page
Accept	KG041
Address Error	KR081
Allow	KC111
Byte Stat Parity	KG111
Byte Stat Parity Error	KG121
Byte Stats	KG071-101
Cable Connector Area	ZS001
CCR Parity Check	KM051
Configuration Control Register	RAxxx
Configuration Gated, CE/IOCE	KC021
Error Stop	KT191
Fetch Data Error	KR041
FLT Load	KG171
FLT Op	KG171
Force Memory Stop and Wait	KT172
Gate Data	KG041
Gate Fetch Data	KG061
Gated Recon Req	KC121
High-Order Address Error	KR111
Ignore Error	KG191
Input Data Check Byte 0, 1, 2, 3	KR001, 011, 021, 031
Input Lines CE to SE	ZS091
Input Lines IOCE to SE	ZS101
Input Switch	RAxxx
Insert Key	KG141

Latches and Registers	ALD Page
Logout Stop	KM121
Logword Format	ZS131
Output Lines SE to CE	ZS081
Output Lines SE to IOCE	ZS111
Output Powering	RBxxx
Output Switch	RBxxx
Pattern Generator	KT321
Priority CE 1, 2, 3, 4	KC061
Priority IOCE 1, 2, 3	KC071
Protected Area	KG161
Protected Area Error	MP031
Read	KC111
Read/Write Gate	KC111
Recon Mode CE 1, 2, 3, 4	KM011
Reconfigure Response	KC071
Request Acknowledged	KC041
Request CE 1, 2, 3, 4	KC001
Request Control	KC021
Request IOCE 1, 2, 3	KC011
Request Reset	KC031
Reset Stops	KT191
Ripple Counter	KT231-311
Run Mode	KT191
S_0, S_1	KM021
SAR/SDR to BOS Data	ZS131
SCON	KM001
SE Entry	ZZ107-257, 427-457
SE Exit	ZZ267-417, 467-527
Select	KG061

Latches and Registers	ALD Page
Set Key	KG151
Set Response Latch	KC091
SP 26 Clock	MP061
SP Compare Reg	MP001
SP Data Reg	MP021
SPCR Parity Error	MP051
SPDR Fetch	MP031
SPDR Parity Error	MP051
Split Cycle	KG131
Start Clock Latch	KC081, KC091
Stop and Wait	KC121
Stop Latch	KT191
Storage Address Register and Address Switch	RAxxx
Storage Check	KG041
Storage Data Register and Data Switch	RAxxx
Store Byte 0, 1, 2, 3	KG071, 081, 091, 101
Suppress Log Check	KG171
Test and Set	KG181
Test Pattern Check Latch	KT401
Test Timer Latch	KT181
Write	KC111
Write Condition	KG061

3-24. POWER

Each Storage Element contains the necessary power to drive the basic operational storage and associated logic for data transfer, timing, and priority. The high frequency inverter/converter package is used in the Storage Element. The following regulators are used for each Storage Element: +3, -3, 6 volt nonmarginal, 6 volt marginal, 18, 60XY, and 60Z.

Voltage sequencing is such that the contents of the BOS and SP 26 are retained on any power on/off sequence except catastrophic failure of units within the Storage Element.

The Storage Element automatically sequences up when primary power is sensed at the input to the Storage Element. Provision for delaying the start of the power on sequence from 0 to 1 minute with each element allows staggering of the power on surge current. Any Storage Element with a power switch in the off position cannot sequence up.

Sensing of power input failure causes automatic switching over to a battery supply. At the end of 5.5 seconds, the Storage Element sequences down. Battery power is then cleared. If input power is restored prior to the 5.5 seconds, battery power is automatically cleared.

After a power down sequence, a five-second time out is encountered before power can be sequenced up again.

3-25. POWER SWITCHES AND INDICATORS

A Master Power Off switch (MPO, Fig. 3-27) for each element is on an exposed power panel. This switch is not interlocked, and when pulled, shuts down the Storage Element. Contents of the BOS and storage protect may or may not be destroyed.

Power on/off switches that are operative only when the Storage Element is in state 0 with the test switch on are located on the power and engineer panels.

A. Marginal Conditions

1. Thermal Check

Indicates that the temperature is one or more of the following:

1. 122 ± 3 degrees Fahrenheit in the logic gate.
2. 112 ± 3 degrees Fahrenheit in the BOS.
3. 140 ± 3 degrees Fahrenheit in the BOS inhibit resistor stack.

NOTE: These are exhaust temperatures and are balanced for maximum input temperature of 90 degrees Fahrenheit.

2. Power Check

Indicates that an overvoltage, voltage marginal, overcurrent, or high thermal condition exists within the SE. Also indicates that X - Y and Z voltages are not on.

B. Catastrophic Conditions

Catastrophic conditions are signals to indicate that the element will lose or has lost power because of:

1. Overvoltage or undervoltage:

Voltage	Overvoltage	Undervoltage
+3	+4.5	+2.5
-3	-4.5	-2.5
+6	+8.0	+5.0
+6M	+9.0	+4.5
+18	+22.0	+16.2
+60 XY	+68.5	-----
+60Z	+68.5	-----

2. Overcurrent - The output current of a power supply exceeds 110 to 140 percent of nominal.

3. High Temperature - The gate temperature exceeds 134 ± 3 degrees Fahrenheit and/or the BOS inhibit resistor stack temperature exceeds 155 ± 3 degrees Fahrenheit.

NOTE: These are exhaust temperatures and are balanced for a maximum input temperature of 90 degrees Fahrenheit.

1. Battery Power

Battery power indicates that the element has gone on battery power. Battery power is indicated on the power panel.

2. Emergency Power Off

An emergency power off signal from the System Console drops Storage Element power and contents of the arrays may or may not be destroyed.

3. Element Power Isolation

Because failure of one Storage Element must not affect another element, complete duplexing of power is necessary. Isolation between the two Storage Elements physically housed together is sufficient to allow normal maintenance (including power sequencing) to be performed on one Storage Element without affecting another Storage Element. A master circuit breaker is provided to remove ac from each Storage Element for servicing.

NOTE: During unit testing of the Storage Element, the master power off switches (2 per frame) are tied in series for safety of operating personnel. Only at the time of actual shipment to a customer are the two master power off switches made independent (as per customer instructions).

For more information on power supplies, refer to IBM-9020 System Power Distribution and Control, Form Z22-2861.

This section shows locations of components and subassemblies of the 7251-03/04. Figure 3-29 shows the right side of a 7251-04. A 7251-03 does not contain the upper BOS nor all of the panels of gate B. Power supplies of the 7251-03/04 and basic packaging concepts of System/360 are covered in separate manuals.

Gates A and B are alike except for the address switch card (P/N 5800529 at A4E3). The power control panels, maintenance panels, and basic operational storage units are also alike. The left power wall, gate A, BOS A (bottom), and power panel A (top) are for one Storage Element, and the other comparable components are for the second Storage Element.

3-26. DOCUMENTATION ON THE SE

The SE documentation available consists of the following text:

1. IBM-9020 7251-04 Storage Element Instruction-Maintenance Manual, CAB011

This text contains a general discussion of the operational characteristics of the SE.

2. IBM-9020 SE ALD Texts:

   CAB111-1
   CAB111-2
   CAB111-3
   CAB111-4
   CAB111-5

These books contain the Automatic Logic Diagrams (ALD) of the SE circuitry. Included in these books are the socket listings and the logic diagrams.

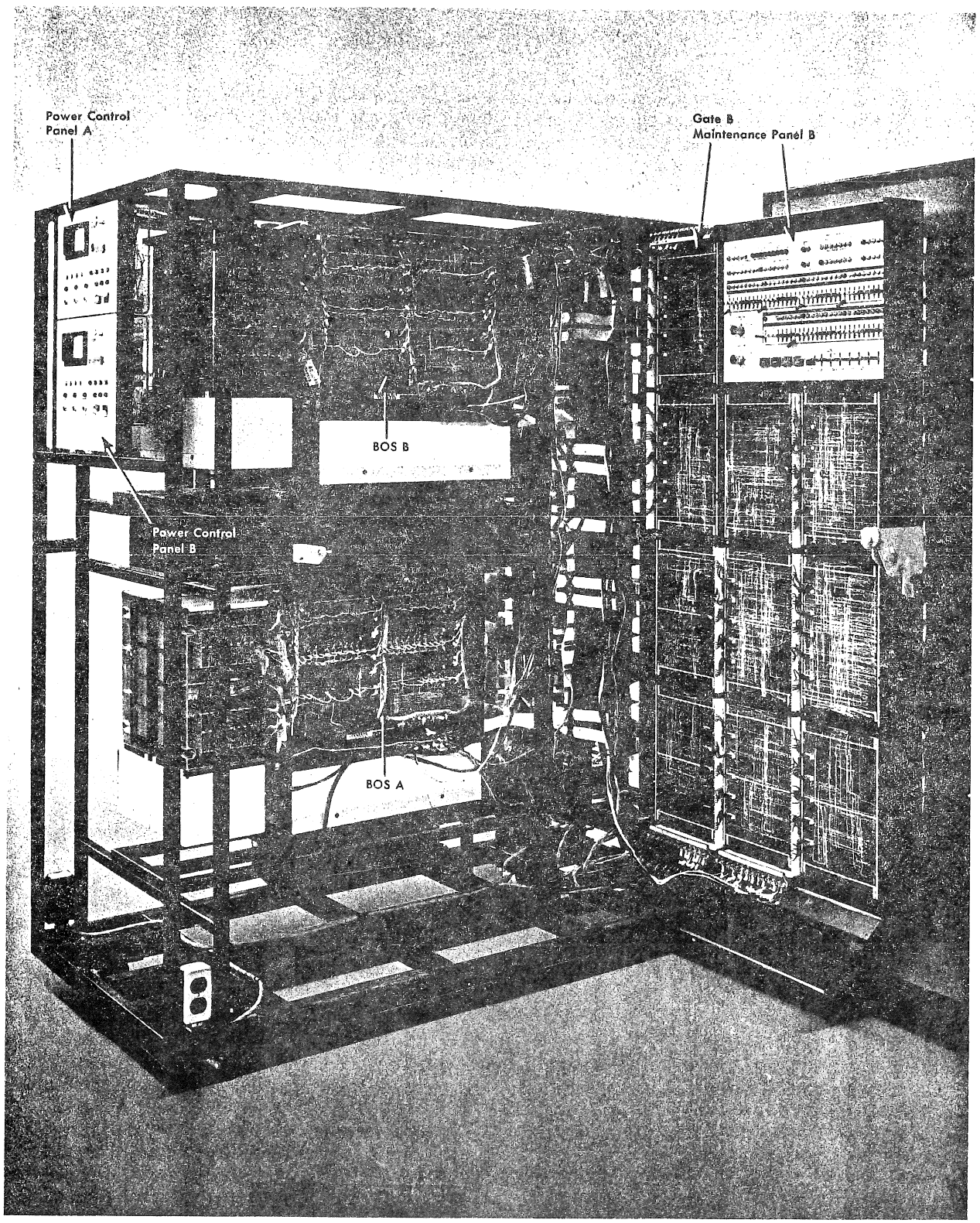


Figure 3-29. 7251-04 Right Side.

A. Socket Listings

The socket listings can be used to obtain the ALD page when the physical location of a card is known. (Refer to Fig. 3-30.) If one were to examine the card G5 on the socket listing, it could be determined that the logic on this card is used on ALD pages RA141, RA151, RA331, and KG071. It is noted that this is a single card which has a portion of its logic not in use at this location (this unused portion being segment "F"). This logic portion on an identical card at another location which is used can be switched because at G5 the failing "F" portion is unused.

B. Logic Diagrams

The ALDs provide detail logic diagrams of the circuitry used to perform the operations of the SE. (Refer to Fig. 3-31.)

If one looks at the lower right hard corner of this page, he will find a title block. Included in this title block are the subject description of the logic located on this page, the physical frame in which the logic resides, the date this ALD page was published, etc. On the example page shown in Fig. 3-31 the subject description is labeled "Byte Stat 0 Input". To the right hand side of the title block on the 3rd line is the frame location of this logic. The logic contained on this page is located within frame "02". Just to the right of the frame designation and outside of the block is the ALD page designation KG071.

Other information in this title block includes the date published, order number for this ALD page if one were interested in obtaining a new page, etc.

The physical location designating the gate, board, and card of a particular logic block on this ALD page occurs within the particular logic block. For instance on Fig. 3-31 look at the logic block labeled 7L representing an AND gate. The gate location of this logic block is gate "X", the board is located at C3 on said gate, and the card is located at position G5 on the board. It

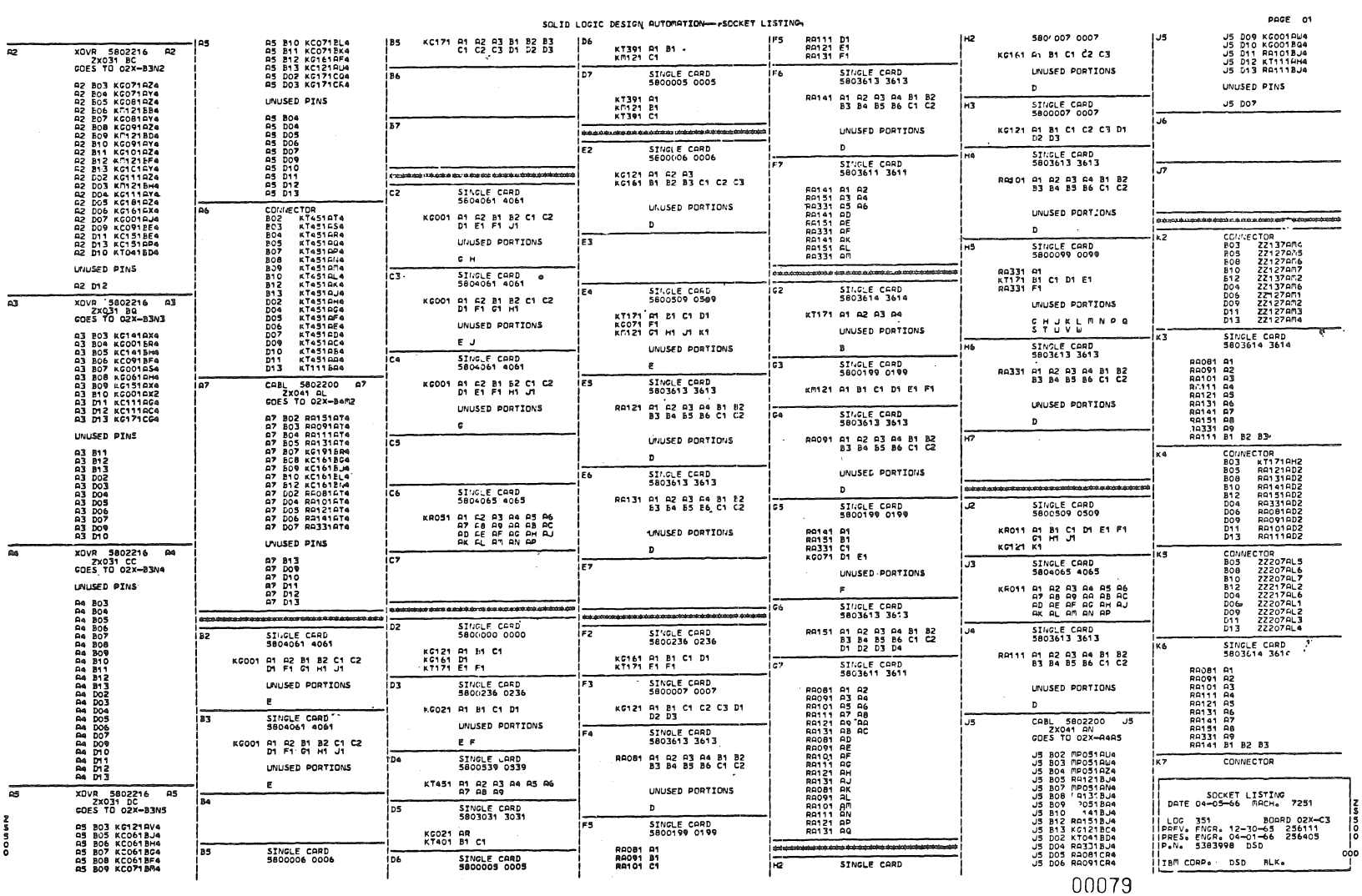


Figure 3-30. Socket Listings.

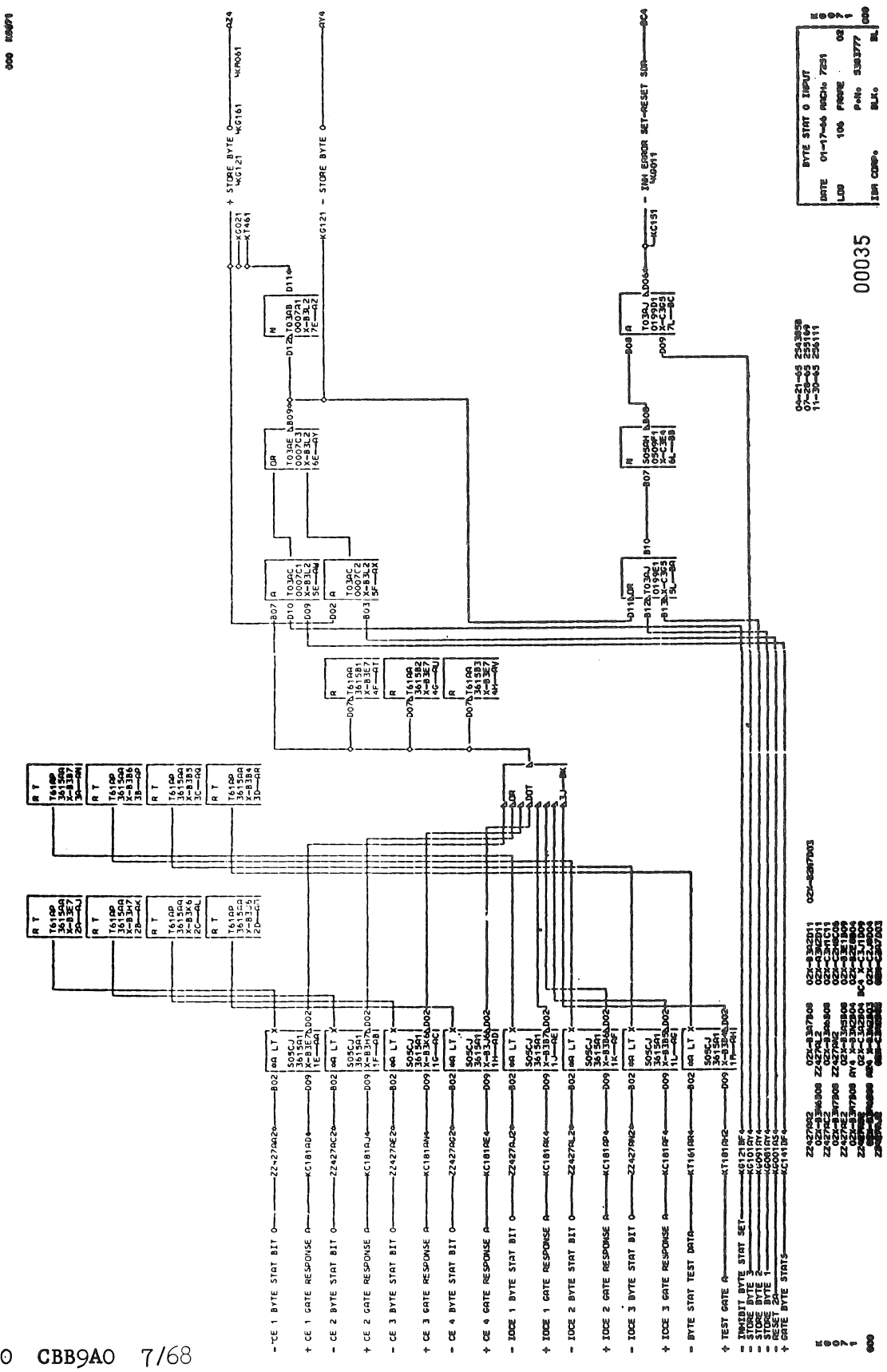


Figure 3-31. ALD Example.

might be noted that there is no gate "X" on the SE frame. The reason such a designation is used, is that there are two SEs contained within the frame and the logic diagrams are identical. Therefore, only one set of ALDs are published for both gates. One looks first to determine which SE he is working on and then goes to the corresponding gate for that SE.

CHAPTER FOUR

INPUT/OUTPUT CONTROL ELEMENT

4-1. INTRODUCTION

The IBM 7231-02 Input/Output Control Element provides the linkage between the Input/Output devices and the 9020 System. The IOCE provides communication between the I/O devices and the SE as specified by instructions from the CE. A simplified IOCE data flow is shown on Fig. 4-1. Note that the IOCE primarily interfaces with other elements in the system. The channels noted on the diagram include 2, (or possible 3), Selector Channels and 1 Multiplexor Channel. These channels act as the interface between the various I/O devices and the IOCE. The IOCE has many functional units in common with the CE; however, due to different operational requirements it also contains some unique functional units. The IOCE has 8,192 (32K (20K hex)) words of storage referred to as MACH Store. Of these 1,024 (1 bump store) are used for channel control words associated with the Multiplexor Channel. ROS within the IOCE makes use of two modes of operation. One mode, CPU mode, operates identically with the Compute Element in processing instructions. The second mode is unique to the IOCE and is referred to as I/O mode. In I/O mode the various channel functions are performed on a priority basis. I/O mode overrides CPU mode and permits channel operations to take precedence over CPU functions. The IOCE utilizes Local Store to a greater degree than does the CE since all channel operations are dependent upon local store control words for their operation.

Before going into any detailed discussion on the functional units of the IOCE, we should become acquainted with the differences between the Selector and Multiplexor Channels. Also we must define some of the more commonly used terms. As both the IOCE and the CE have the same functional units in the area referred to as the Common Logic Unit (CLU), discussion will be limited to those function units which are unique to the IOCE. Reference should be made to the CE sections whenever a question arises about the units which are common to both.

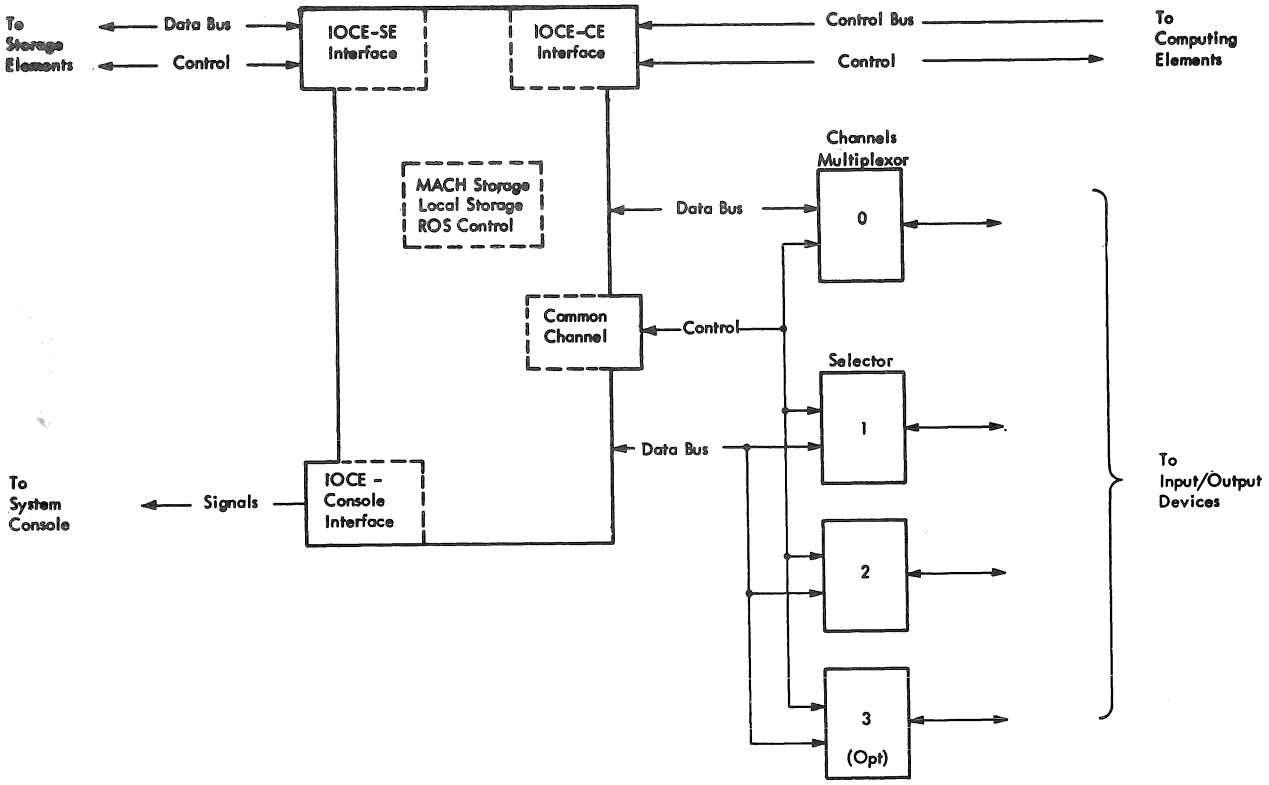


Figure 4-1. Simplified IOCE Data Flow.

The Multiplexor Channel is capable of servicing several I/O devices on a byte interleave basis simultaneously in multiplex mode or a single device at a time when operating in burst mode. The Multiplexor Channel uses the CLU only for the length of time required to service the I/O device request and requires fetching control words for each device from MACH Store when the channel is operating in multiplex mode. When in "burst" mode, the Multiplexor Channel can only service one device at a time and the channel retains control of the CLU for the entire duration of the operation. The Multiplexor utilizes special I/O mode ROS routines in its operation and utilizes the CLU extensively for its data transfers.

The Selector Channel on the other hand may operate only in burst mode, and as such may control only one device at a time. The control words being used by the Selector Channel during an I/O operation are stored in Local Store and

are more rapidly available to the IOCE for use. (MACH Store cycle time = 2 μsec, Local Store cycle time = 0.5 μsec.) Then too, since only one device is being serviced at any given time, the control words need not be fetched and re-fetched. The Selector Channels use conventional sequential logic circuits to control operations and require the use of the microprogram and CLU only when data transfers are to be accomplished between the IOCE and the Storage Element. (Using the data supplied by the Program I/O Instruction, the channel assigns priority to these ROS routines and requests them as needed.)

Another factor which tends to speed up operations on the Selector Channels is the fact that data is handled on a full word basis whereas on the Multiplexor Channel the data is handled on a byte basis.

4-2. PHYSICAL MAKE-UP

The IOCE like the CE utilizes the same "building block" construction techniques. It is made up of the same card, board, gate and frame arrangement as the previously discussed Compute Element; however, in the case of the IOCE there are some additions. Frame 01 contains the logics for the CLU and the channels. Frame 02 contains the logics and the core array for the MACH storage. Frame 03 contains the power supplies, the configuration control circuitry, and the optional 3rd channel.

4-3. UNIQUE IOCE FUNCTIONAL UNITS FOR SELECTOR CHANNEL

Figure 4-15 is the overall data flow diagram for the IOCE. From this it may be seen that with the exception of the I/O oriented registers, the basic CLU is identical with that of the CE. The I/O oriented functional units for Selector Channel will be briefly discussed in the following sections.

A. B Register

The B Register acts as a buffer to data being transferred to or from the C Register. All data enroute to or from channel passes through this register. While the logic diagrams (ALDs) and the data flow chart indicate only one B Register, there is actually one of these register per Selector Channel. ALD representation for these registers is ALWAYS WITH REFERENCE TO SELECTOR CHANNEL NUMBER ONE....To determine the card location for Selector Channel 2, take the board card location from the ALDs and subtract 2 from the board location, e.g. a bit position for the B Register is given as E gate, board D4 card F6. The equivalent bit position for Selector Channel 2 B Register is E gate, board D2 card F6. To determine the card location for the optional 3rd channel, the J gate is substituted for the specified E gate location on the ALDs.

B. C Register

The C Register is used for distributing the word from storage to the channel on a byte basis. This register is also used to assemble the incoming bytes from channel into a word prior to sending it to storage. Like the B Register, there is one C Register per Selector Channel. The C Register is fed directly from the channel interface on input operations and placed its output into the B Register. On output operations the C Register is fed from the B Register and places its output directly on the channel interface bus. The rules for finding card locations for channel 2 and 3 are the same as for the B Register. Figure 4-2 should be examined for relative board locations.

Since both the B and C Registers are concerned with the operations in the Selector Channel, it may be wise at this time to cover the remainder of the registers whose application is primarily in this area. This is the area enclosed by the dashed line in Fig. 4-15. The logical units are also shown in greater detail in Fig. 4-16. In this figure they are related to the CLU functional units with which they operate. For convenience and ease in correlating these diagrams to the ALDs, the corresponding ALD pages are

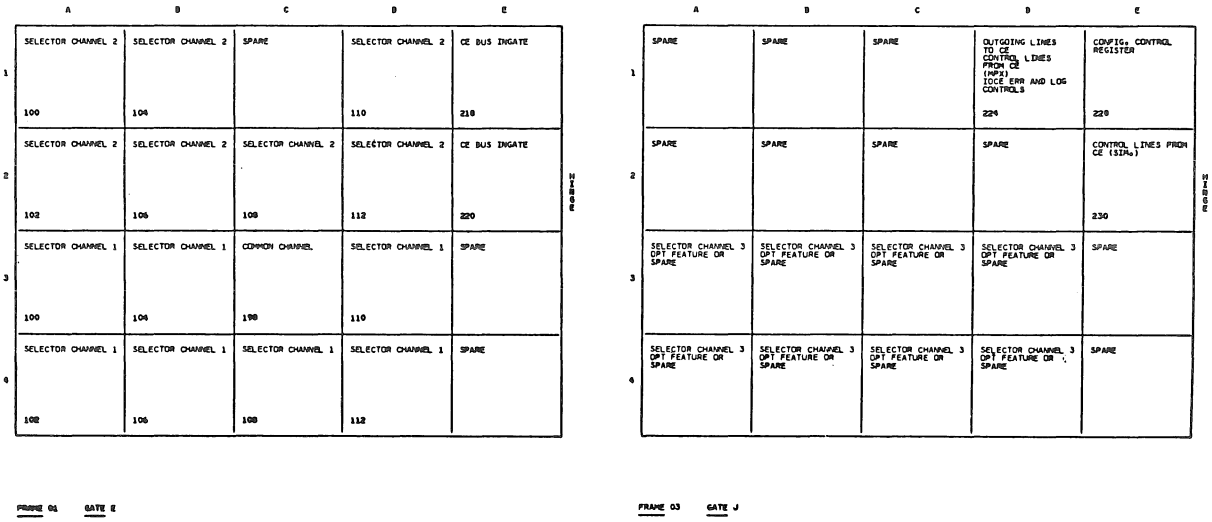


Figure 4-2. Selector Channel Board Locations.

included. In Selector Channel operation the hardware circuits make use of the programmer supplied control words such as the Command Address Word (CAW) and the Channel Command Word (CCW). Since only one control unit may be operating on a channel at a time in the Selector Channel, the information is stored in the General Purpose Register. It is from this register then that the Selector Channel derives operational control. Because the General Purpose Register can store only eleven bits, the outputs of several register positions have more than one destination. These positions are modified with appropriate data more than once while the channel is processing the CCWs.

C. General Purpose Register

Figure 4-4 shows the contents of the General Purpose Register for various channel states. The logic flow of Fig. 4-3 indicates that the General Purpose Register feeds the Byte Counter, the End Register, the Operation Register, and the Flag Register.

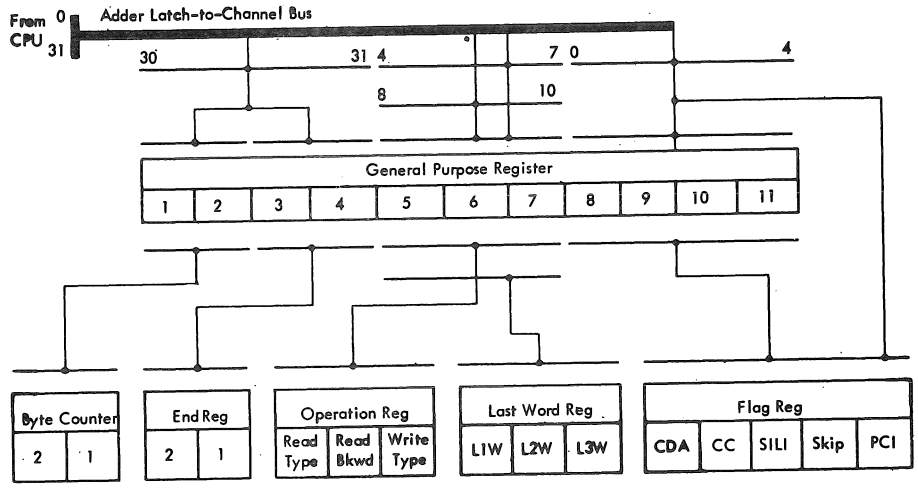


Figure 4-3. General Purpose Register Logic Flow.

General Purpose Latches							
1	2	3	4	5	6	7	Channel State
0	0	0	0	0	0	0	Idle → CCW-1, Step 1
← BC Information →		0	0	Rd Op	Bkwds	Wr Op	CCW-1, Step 1 → CCW-2, Step 1
← BC Information →		0	0	0	0	0	CCW-2, Step 1 → CCW-2, Step 2
← BC Information →		← ER Information →		L1W	L2W	L3W	CCW-2, Step 2 → CCW-2, Step 3 A1
← BC Information →		0	0	L1W	L2W	L3W	CCW-2, Step 3 A1 → Rd Store or Wr Fetch
← MBCR Information →				L1W	L2W	L3W	Rd Store
← BC Information (Original) →		0	0	L1W	L2W	L3W	Wr Fetch
—	—	← BC Information (Final) →		L1W or Compare Equal	L2W	L3W	End Up (Rd) → Interrupt → Reset
← BC Information (Original) →		0	0	L1W or Compare Equal	L2W	L3W	End Up (Wr) → Interrupt → Reset

Figure 4-4. General Purpose Register Utilization.

D. Byte Counter

Figure 4-3 indicates that the General Purpose Register positions 1 and 2 feed the Byte Counter. This Byte Counter is used to control byte selection within the C Register. The Byte Counter set to 00 selects byte 0 of the C Register, Byte Counter set to 01 selects byte 1 of the C Register and so forth through byte 3. The Byte Counter is made up of two stages of logic. The A side is used to select C Register byte positions and is stepped upon the completion of a data transfer across the interface. The B side of the Byte Counter is used to determine, early in the operation, if the the present data sequence with the interface will transfer the last byte to be stored (or fetched) from the designated storage block. It is also used to store or unload the byte in C Register byte 3. The B side of the counter is advanced when the interface data sequence begins. Figure 4-5 is a second level logic diagram of the Byte Counter and its gating circuitry.

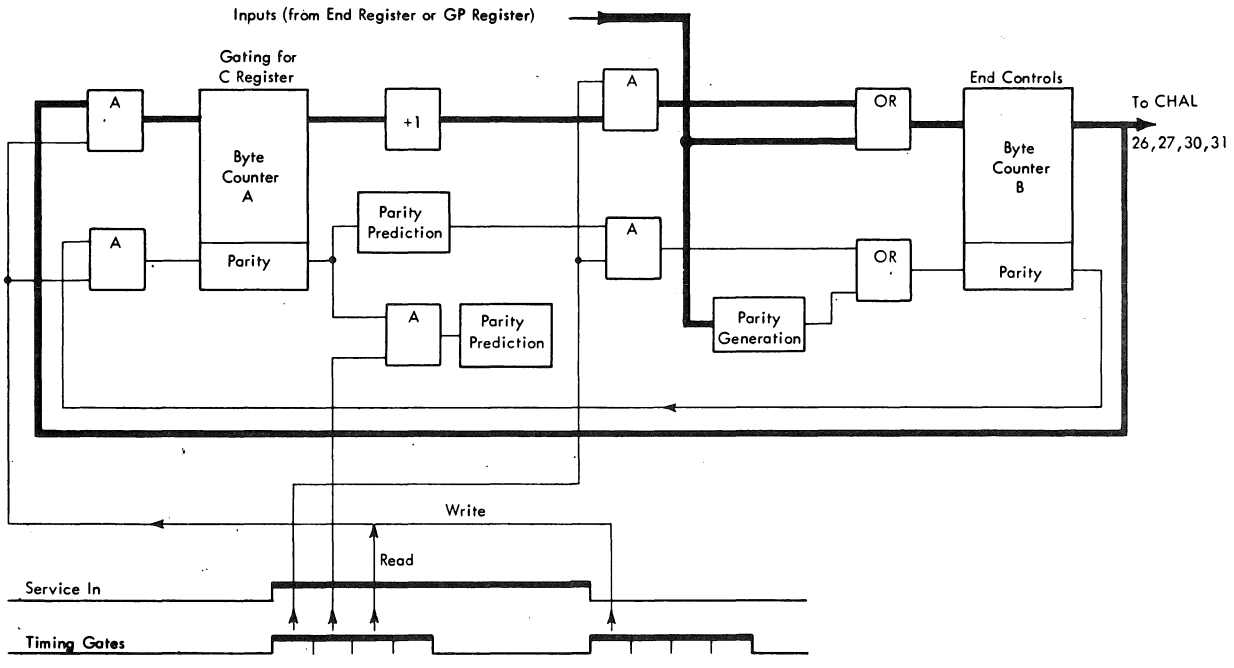


Figure 4-5. Channel Byte Counter.

E. End Register

Bits 3 and 4 of the General Purpose Register are used to contain the results of adding the last two bits of the data address with the last two bits of the count. The resultant is placed in the End Register for use when an off-bounds data transfer between the channel and storage exists.

F. Last Word Register and Operation Register

Bits 5, 6, and 7 of the General Purpose Register may contain either the last word information or the Operation Register information. In operation the CCW can specify one of five commands that may require communication between the channel and an I/O unit. The channel cannot distinguish between write and control or between sense and read command; therefore, the commands are divided into three categories: Read, Read Backward, and Write. The CLU transfers bits to the channel to identify a command. The channel decodes the bits and sets one of three positions of the Operation Register. The last word information takes on different significance in the Read and Write operations. In Read operations a Last Word Register position is normally set when three or less words are left to be stored in the designated block in main storage; whereas in the write operation a Last Word Register position is set after the last word is taken from the designated storage position.

G. Flag Register

The Flag Register is set from positions 8-11 of the General Purpose Register. The set state of any Flag Register position causes channel to deviate from normal procedures in executing the operation. This register is normally set while processing the second half of the CCW except in the write chain data operation.

H. Channel Status Register

The Channel Status Register is supplied with data from the common channel circuits. This data is used to indicate the following:

1. Program Controlled Interrupt
2. Incorrect Length Indication
3. Program Check
4. Protection Check
5. Channel Data Check
6. Channel Control Check
7. Interface Control Check
8. Chain Check

Any bit set in this register will appear as information in the Channel Status Word when a channel interrupt occurs, and may be utilized by the programmer to ascertain the ending status of the operation.

Referring once again to Fig. 4-15 the remaining functional units of the Selector Channel may be divided into two categories. The first of these is the priority and routine request circuitry, and the second is the external channel and interface controls.

I. Routine Request Circuitry, I/O External Channel, and Interface Controls

In the operation of the IOCE an area of circuitry called common channel deals with all circuitry common to the Multiplexor Channel and the Selector Channels. This circuitry processes requests for service from the channels, and assigns priorities to the service requirements. All requests are held active until they are serviced and the routine requested is in progress. The priorities assigned indicate that requests for Local Storage Read, and Local Store Write routines, carry the highest priority (referred to as higher than 1). The Write Fetch or Read Store routines are assigned as priority 1 since these routines imply that an I/O device is awaiting immediate data service and the

possibility of a channel over-run is impending. On the other hand Interrupt Preparation or instruction (SIO) processing are assigned the lowest priority (priority 3) since these in general are not time dependent (within limitations). Figure 4-6 is a second level logic diagram depicting the interrelationship between the Priority Circuits, the Request Register, and the Position Register in the Selector Channel operation.

4-4. CHANNEL ROS RELATIONS

Although channel can perform a limited number of actions without direction from the Read Only Storage, neither the multiplexor nor the selector can operate completely independent of this control. Since it is possible for the CLU to be performing operations other than the servicing of the channel requests when a request is received that requires the use of the functional units of the CLU, ROS is required to switch from the CPU mode of operation to I/O mode of operation. This is defined as Break-in and may be accomplished any time that the CLU is operating in the CPU mode and is not in the R-1 or R-2 cycle of the storage timing ring. Break-in always occurs at zero time of the machine cycle and results in the degating to the ROSDR (that is, all of the μ-orders are decoded as no-ops) and the R Register is automatically backed up into local store quadrant two, word twelve. The ROS address of the CPU mode instruction which was to have been processed at the time of the break-in is stored in the I/O Back-up Register for the subsequent breakout. (After the break-in cycle is completed and the ROS is operating in the I/O mode, the I/O Backup Register is not altered.) When operating in the I/O mode, the sequence of ROSDR bits, which go to make up a field, are altered and the method of decoding these fields is changed to permit additional μ-orders applicable only to this mode of operation.

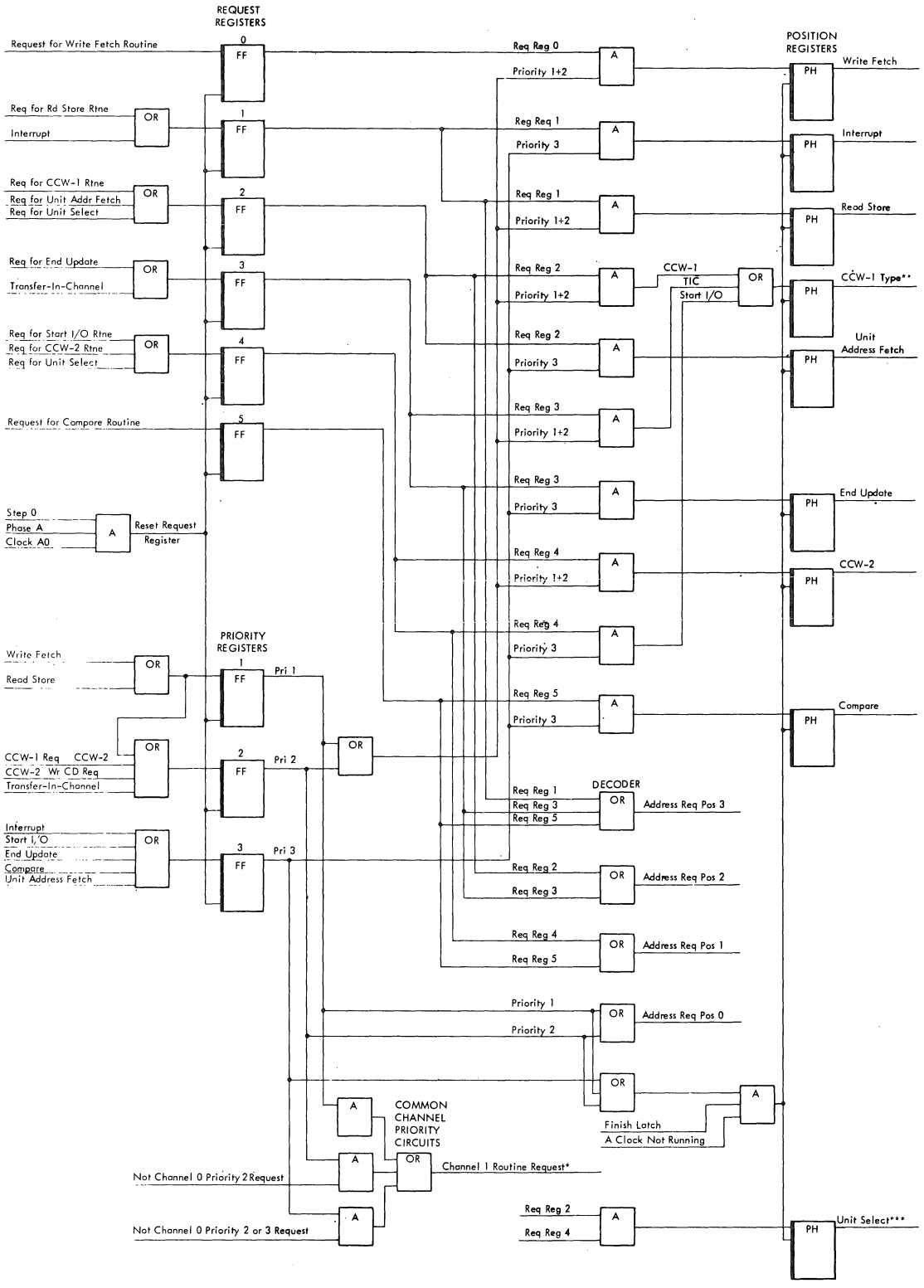


Figure 4-6. Routine Request and Priority Circuits.

There are twelve ROS routines used in the IOCE to service Selector Channel requirements. These are:

	Routine Name	ROS Address
1.	Start I/O	0010
2.	Transfer-in-Channel	002C
3.	CCW-1	0028
4.	CCW-2	0030
5.	Write Fetch	0020
6.	Read Store	0024
7.	Compare	0014
8.	Unit Address Fetch	0008
9.	End Update	000C
10.	Interrupt	0004
11.	Local Store Read	0040
12.	Local Store Write	0044
13	Set ATR	
14	Read Store routine	

Each of the aforementioned ROS routines performs a different service to the channel. For more complete details of these services, the student is advised to consult the CAS logic diagrams for the specific IOCE. The first ROS address of each of the routines is generated by the routine request circuitry. This circuitry consists of two registers. A six position register referred to as the Request Register, and a three position register called the Priority Register. These two sets of registers drive or set the position register as well as signal common channel to force the first ROS address of the requested routine. Since there are two Selector Channels in the IOCE, there are control registers for both, and while the ALD listings refer only to Selector Channel number one, the appropriate Selector Channel two circuits may be determined as previously mentioned. The optional channel three circuitry may also be found on gate J.

4-5. CE - IOCE SELECTOR CHANNEL OPERATION

Examination of a Start I/O instruction to a specific device on the Selector Channel shows that the instruction is fetched from storage by the CE and the initial data movements are accomplished to gate proper data to the CE's External Register. The flowcharts (Figs. 4-17 and 4-18) in conjunction with the Data Flow Diagrams (Figs. 2-64 and 4-15) for the CE and IOCE may be examined to clarify the locations and paths within the CE and IOCE. Notice from the flowcharts that once the CE has sent the I/O Op Signal to the IOCE that it (the CE) goes into a countdown loop to await a response from the IOCE. The data to be used in this instruction would be stored at the following storage locations prior to execution of the SIO.

Storage Location	Date	Comments
0A00	9C000101	Start I/O to Tape Drive
0048	0000A000	Channel Address Word (CAW) specifying a key of zero' and a command address of A000
A000	0200C000	Channel Command Word-1 (CCW-1) with a read command and a data address of C000
A004	20000020	Channel Command Word-2 specifying a SILI flag set on and a byte count of X'20' bytes

For proper operation of the instruction it must be assumed that the current PSW is properly masked to allow the execution of this privileged instruction and that the Selector Channel is properly masked to allow the subsequent I/O interrupt. Bear in mind that the PSW under consideration is contained in the CE only. Any channel masking will be taken care of via intercommunication linkage. We are also concerned with two ROS control units. The ROS of the CE will be concerned with the instruction fetching and initial processing. The IOCE ROS on the other hand will operate as follows:

The IOCE ROS unit is normally operating in CPU mode. When this element is not processing I/O instructions, processing interrupts, performing logouts, or performing other maintenance functions, ROS is cycling in the halt or wait loop. (The IOCE must be in the wait loop before any processing of this instruction can take place.) Under the conditions mentioned, a General Purpose Stat (stat 1) is set and branching from the halt loop will take place under its influence. The IOCE will permit its circuits to gate the data from the CE external register into its own functional units. Under the control of the I/O op code sent from the CE, the IOCE will branch to the appropriate μ-routine to handle the requested operation. In the case of the SIO, this would require the fetching of the CAW from the SE and using the address contained in this word to fetch CCW-1. When if the CCW is tested and found to be valid, the IOCE will take the data it has available from the CE external register, the CAW, and CCW-1, and gate it to the correct functional registers. When this is completed, the IOCE raises a tag line to the Common Channel, then establishes and enters its own count'down loop. The tag line to the Common Channel in our case causes Common Channel to force the first address of the Selector Channel SIO ROS routine. As a result of forcing the ROS address and the ensuing break-in, the IOCE goes to I/O mode. (Until this time the IOCE has been operating in CPU mode.)

As was mentioned previously, in the I/O Mode, the IOCE ROS routines are used to perform the functions or services as requested by the Selector Channel's logic circuits. In a read operation for instance, channel data is accepted by the IOCE circuits and routed to the appropriate storage facilities under ROS routine and channel logic circuit control. The ROS routine synchronizes the Channel Clock to start taking data off the bus with a DTC pulse on the cycle prior to its putting data on the bus. The data may be Unit Address, Data Address, or Chaining Flags (I/O data during Write operations also).

The SIO ROS routine places the Unit Address in C Register byte 0 and the Operation Code in the B Register byte 0. It also sets the Byte Counter and places the Command Address, Data Address, and Unit Address in Local Store. A test is made for a Transfer-In-Channel (TIC) command, and a request is made

of Common Channel for CCW-2 routine. Assuming the request for CCW-2 will be honored immediately, there will be no break out cycle at this time.

The CCW-2 routine fetches the CCW-2 word from storage and stores the bits for the Flag, End, and Last Word Registers in the General Purpose Register. It also sets the first word and first byte latches and sets the GP reg bits to the Last Word, Flag, and End Regs as well as modifying the initial count and initiating the hardware controlled Selector Channel - I/O control unit sequences.

The channels logic circuits perform the Selector Channel - I/O control unit portions of the I/O operation on the interface independent of ROS control. The Unit Select routine called for by the Start I/O CCW-2 ROS routine sets up the interface linkages with the control unit of the selected I/O device. The diagram of Fig. 4-10 depicts the hardware controlled operations of the Unit Select Routine.

Once the CCW-2 routine requests the hardware to take over, ROS is no longer required to sustain the operation ROS takes a break-out cycle and returns to the CPU mode. It should be remembered that the CPU ROS was in a count-down loop and consequently will return to this loop. When the hardware routine has completed its work and ascertained the status of the I/O device, it will set the required stat 3 to cause the IOCE to break out of the count-down loop and continue processing this instruction. As indicated, this results in a stat 3 response and condition code being sent to the CE. The IOCE completes its operation then returns to the wait loop to await another instruction or an I/O break-in when the channel requires a data service.

The CE, upon receiving the condition code and stat 3 from the IOCE is now freed from its count-down loop and will return to I-Fetch for the next program instruction.

As indicated on the hardware Unit Select Routine flowchart, the selected I/O device will raise "Service In" to the channel hardware circuits to begin the

interface data sequence. This sequence will start the Tag Generator and store the byte on the bus in the C Register at the byte position designated by the Byte Counter (A section). This action will continue until the byte counter indicates that the C Register is full. When this register is full, the word is transferred to the B Register and Common Channel is requested to supply a Read-Store ROS routine. (This is the first I/O mode break-in since the IOCE ROS returned to the halt or wait loop.) This Read Store Routine updates the storage data address and stores the word from the B Register. It also updates the count field from the CCW and tests the End-Of-Record latches. If these latches are not set (which they would not be on the specified instruction) the ROS returns to the halt loop via a break-out routine and the reloading of the C Register is once again under hardware control. This sequence of loading the C Register under hardware control and requesting ROS routines to store the data in storage will continue until the last byte of data as specified by the count field of the CCW is transferred. At this time, the Read Store Routine will test the Chain Data Flag and if not set, will request the End Update Routine of ROS. The End Update results in the correction of the command address and the count in Local Store and the interrupt request being made. This interrupt request is gated through channel logic circuitry and, if the CE PSW bit is masked to allow, results in the CE taking an I/O interrupt.

As a result of the interrupt request from the IOCE, the CE will begin processing the interrupt at the end of the instruction it is executing. In processing this interrupt the CE will load the Preferential Storage Base Address on the External Bus to the IOCE and raise a tag line to permit the interrupt. The CE will then go into a count-down loop to await the IOCE response.

While the CE is in this count-down loop, the IOCE will, using its internal ROS routine, break from the halt loop and request the Interrupt Routine from Common Channel. While the IOCE is waiting on Common Channel to honor its request, it also goes into a count-down loop. The I/O mode operation of the Interrupt Routine in the Selector Channel causes the Channel Status Word

information to be loaded into the L, M, and R Registers. This data is then stored by CPU Mode Operation in the SE at the address specified by the PSBA + 64 (dec). The Unit Address is loaded into storage as the interrupt code. The IOCE then sends a response (stat 3) to the CE and returns to the halt loop. Upon receiving the (stat 3) reply from the IOCE the CE will branch out of the count-down loop and proceed to store the remainder of the PSW in the old PSW area. The new PSW is then loaded into the PSW Registers and becomes the current PSW, processing continues at the address specified by the IA portion of this control word.

While it is recognized that the foregoing discussion on the Selector Channel was greatly simplified, the scope of this course prevents discussion to greater depth. Additional information regarding this subject may be found in the following manuals:

1.	Input/Output Control Element Instruction Manual	CAB020
2.	Input/Output Control Element Panel Manual	CAB021
3.	System 360 Model 50 Selector Channel Theory of Operation Manual	CAA021-1
4.	7231-02 IOCE Diagram Manual	CAB520
5.	7231-02 IOCE ALD Manuals Vol. 1 - Vol. 21	CAB121-1 - CAB121-21

4-6. IOCE MULTIPLEXOR CHANNEL

The Multiplexor Channel is capable of servicing several I/O devices simultaneously when operating in the byte or multiplex mode. Actually, the channel is capable of servicing several devices sequentially (on a priority basis) and sustaining their operations simultaneously. The channel however is capable of sustaining only one operation at a time when operating in burst mode. The IOCE data flowchart of Fig. 4-15 indicates that the only additional functional units over and above those previously discussed are the Buffer 1, Buffer 2, and Buffer Latches.

The multiplexor handles data on a byte basis and as such requires the buffering provided by the 2 buffers and the associated latches. Both of the buffers are capable of accepting data from either the Mover or the Bus In from the interface. Both of the buffers are likewise capable of supplying data to the input to the Mover; however, only buffer 2 is capable of setting the Bus Out Latches to the interface. Figure 4-7 is the ILD for the buffer registers and the buffer latches while Fig. 4-8 is the logic flow for the Multiplexor Channel.

Operation on the Multiplexor Channel may be carried on in either byte mode or burst mode and may change modes in the same operation. When in burst mode, the I/O unit performing the operation remains logically connected to the interface. This differs from the byte (multiplex) mode in that in the byte mode the I/O unit is logically connected only during the time required to complete a data byte transfer. The channel facilities are time shared between the I/O devices.

The Multiplexor Channel is primarily ROS controlled in its operation. While the selector was controlled by sequential logic circuits (hardware), it had 12 ROS routines to accomplish the requested tasks. The Multiplexor on the other hand, has 34 ROS routines which are used to control its entire operation. The selection of these routines is a function of the Common Channel Circuitry and the Routine Request Generator. The channel receives its requests from the I/O devices (which are operating asynchronously). Channel in turn requests the appropriate ROS routine to service the request it received from the device. The channel request for ROS routine is serviced by the Common Channel which assigns a priority to it and in turn causes the Routine Request Generator to generate the starting address of the requested routine (when its turn comes up in the sequence). It is in this manner that the Multiplex Channel is capable of sustaining multiple operations.

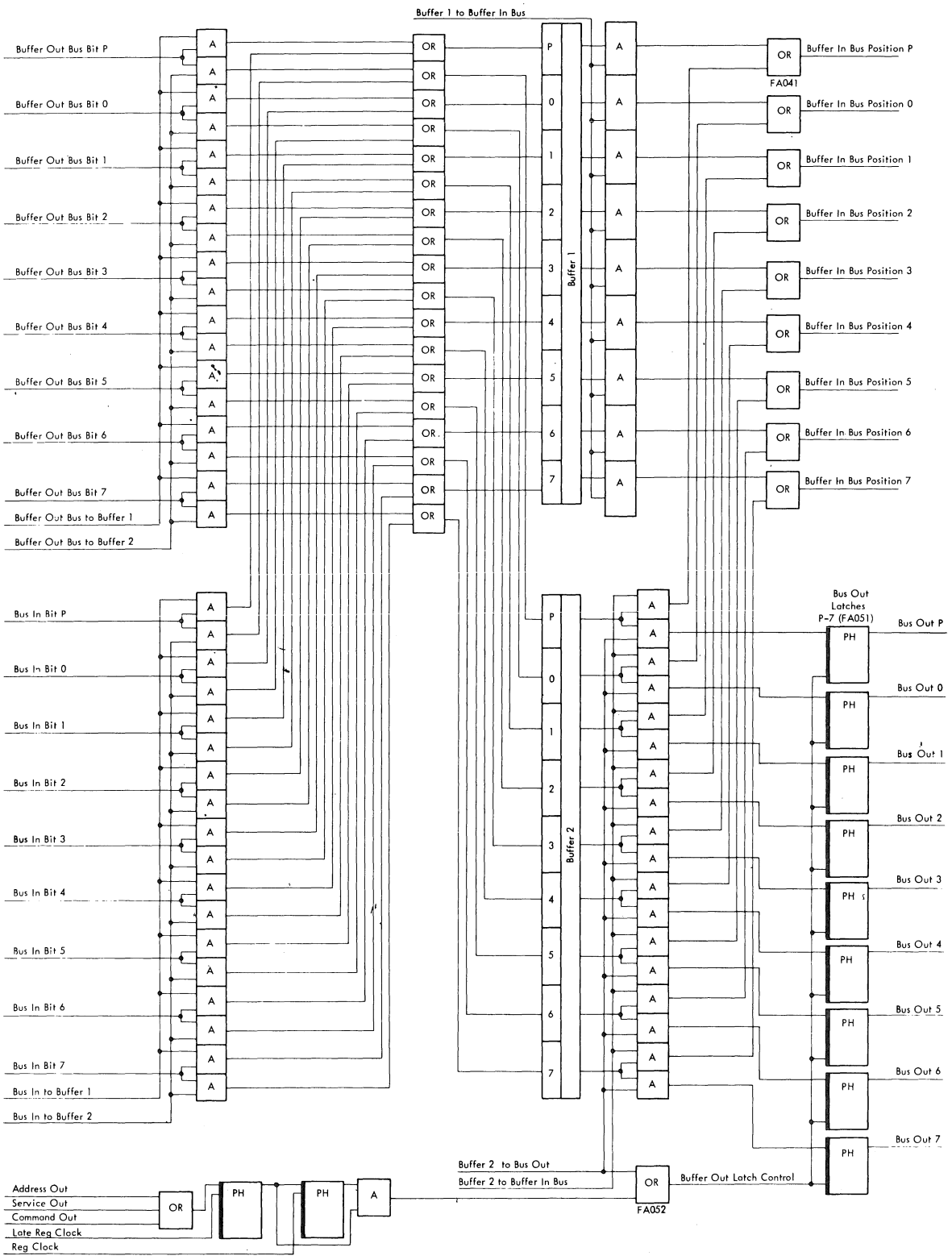


Figure 4-7. Buffer 1 and Buffer 2 Sets and Resets.

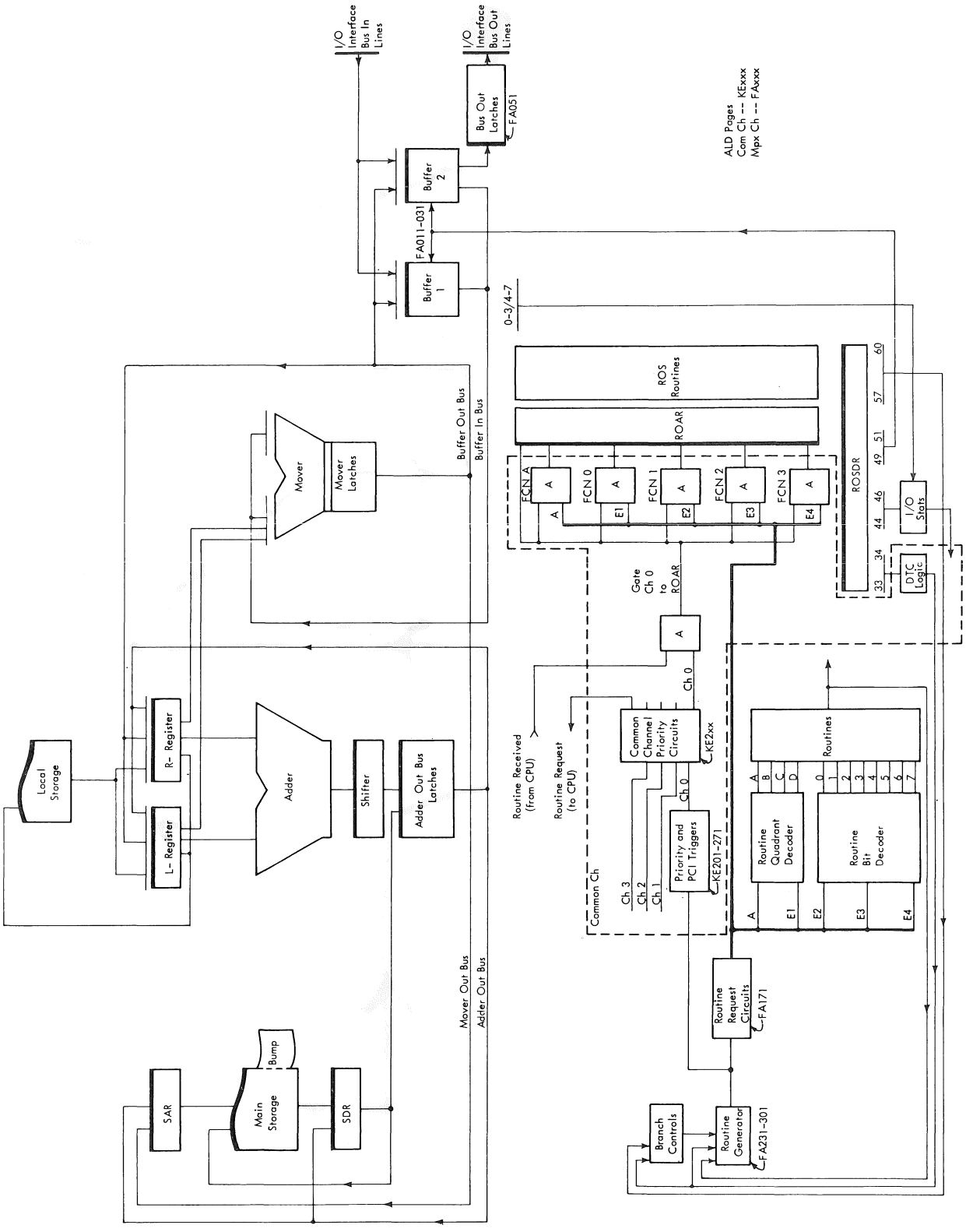


Figure 4-8. Data Flow in Multiplexor Channel Operations.

The 34 ROS routines which the Multiplex Channel has available for its operational control are all executed in the I/O mode, and as such, require that a break-in take place. At the end of each of the routines, Common Channel tests its priority control circuits to ascertain if a routine with a higher priority has been requested. Assuming that none has been, the Routine Request Generator will start into the next lowest priority routine or permit the continuation of the sequence. If there are no routine requests pending (higher or lower priority) the IOCE ROS will perform a break-out cycle and return to CPU mode. The 34 routines are functionally divided into 5 general categories.

"A" type routines which in general deal with the CCW and data handling include:

- AØ - Count Fetch and Update
- A1 - Data Address Fetch and Update
- A2 - Data Address and Count Correction
- A3 - Data Handling
- A4 - End Status Analysis
- A5 - Comm Chain End Status Analysis
- A6 - Interrupt Preparation
- A7 - Count = Ø Analysis

The "B" type routines deal primarily with the SIO instruction and the interface operation during this instruction. Routines B5 and B6 are multipurpose routines and may be used with other categories.

- BØ - Sequence Control Fetch
- B1 - Start I/O Unit Select
- B2 - Start I/O Unit Address Compare
- B3 - Status Analysis
- B4 - Unused
- B5 - Count Store
- B6 - Data Address Store
- B7 - Channel Check Handling

The "C" type routines in general deal with the interface operation for the other program instructions which the channel is capable of performing.

- CØ - PCI
- C1 - Test I/O Unit Select - 1
- C2 - Test I/O Unit Address Compare
- C3 - Test I/O Accept Status
- C4 - Control Check
- C5 - Control Unit Busy
- C6 - HIO Unit Select
- C7 - Test I/O Unit Select - 2

The "D" routines in general deal with the chaining operations specified in the CCW for the operation being performed. Since in the original I/O instruction processing CCW word 1 was fetch and processed in CPU mode, provisions had to be made to permit fetching the additional CCW-1 words in chaining operations.

- DØ - Command Address Fetch/Store
- D1 - CCW-1
- D2 - Command Chain - UA Compare
- D3 - Command Chain - Initial Status Analysis
- D4 - CCW-2 Fetch
- D5 - Load 64 Prep-Test I/O No End Qued
- D6 - Not Used
- D7 - Data Chain

The interrupts are handled under the control of the "H" routines.

- HØ - SPCI Interrupt
- H1 - Interrupt Handling
- H2 - Interrupt Handling - 2
- H3 - Interrupt Handling - 3

The flowchart of Fig. 4-19 is the general routine selection sequence for typical I/O operations on the Multiplex Channel. Figure 4-9 is the flowchart for a typical routine.

The general routine selection sequence chart is not in the true sense of the words a flowchart since there is no differentiation made between the hardware operations and those of the ROS routines. This chart is presented merely to acquaint the student with the normal sequencing of the routines. For a more complete analysis of the Multiplexor Channel ROS routine selection the student is advised to consult the flow diagrams in FAA manual CAD-520.

Figure 4-9 is the logic flowchart of the B1 Unit Select ROS routine. The decisions made in this routine are made as a result of the A and B branch bits of ROAR. These bits would be set as a result of channel action on the I/O stats, or as a result of the data supplied to the beginning u-instruction. This figure also indicates that there are exits from this routine to hardware sequential logic circuits.

These circuits would set the stat 3 reply, and set the condition code to 2. Setting the stat 3 reply would allow the IOCE to exit from its count-down loop, this in turn would cause the response to be sent to the CE. The condition code being set to 2 would present a Unit Busy Status to the CE as a result of the I/O instruction.

Note that the operation of the Multiplex SIO is identical to the SIO on the Selector Channel (as shown on Fig. 4-17) until the IOCE goes to the count-down loop. The operation is identical when the stat 3 reply is received. The only difference between the two types of channels is in the I/O mode operations while in the initial selection, and the manner in which data is transferred to storage and to the device.

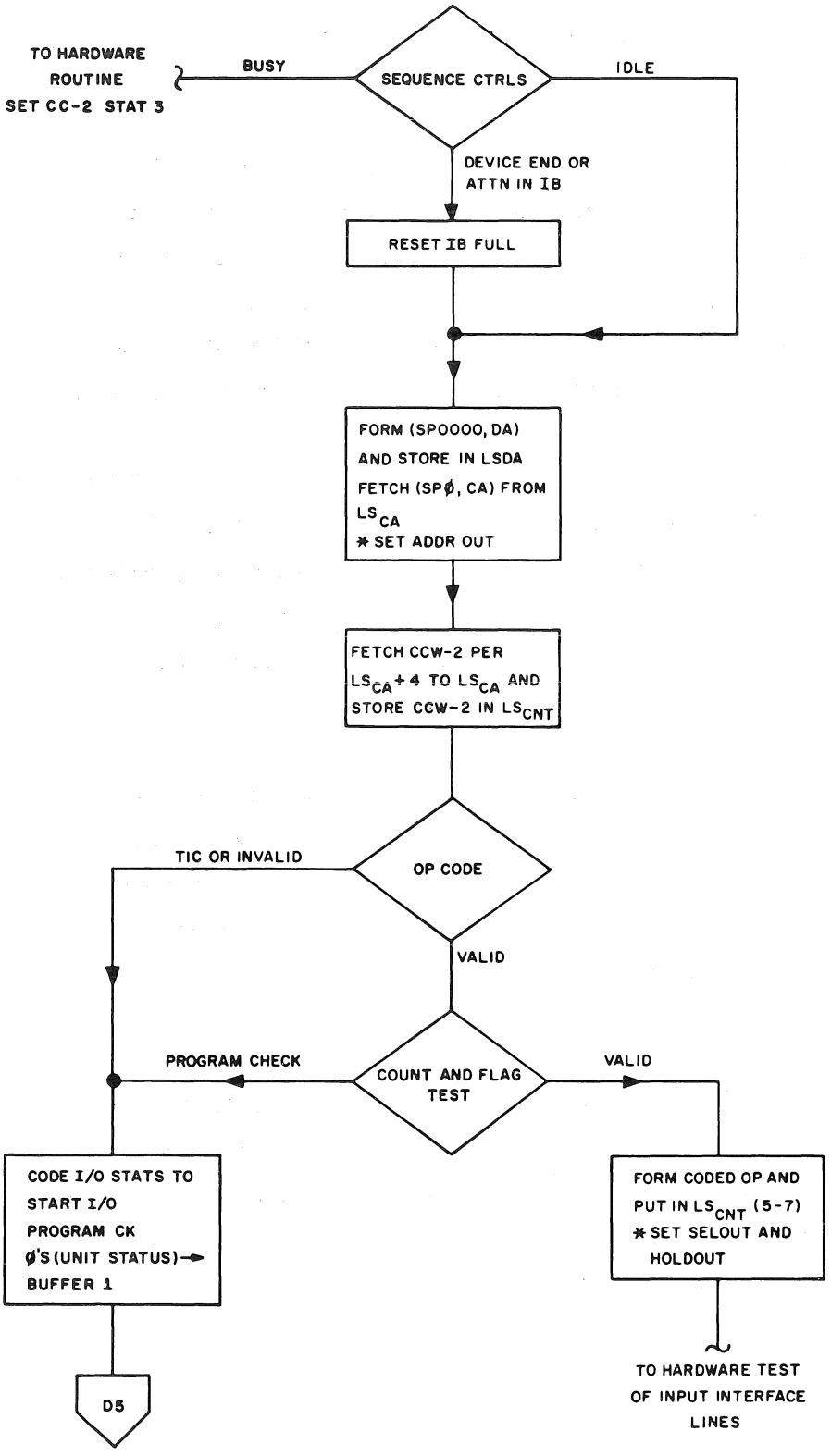


FIGURE 4-9 MULTIPLEXOR BI ROUTINE

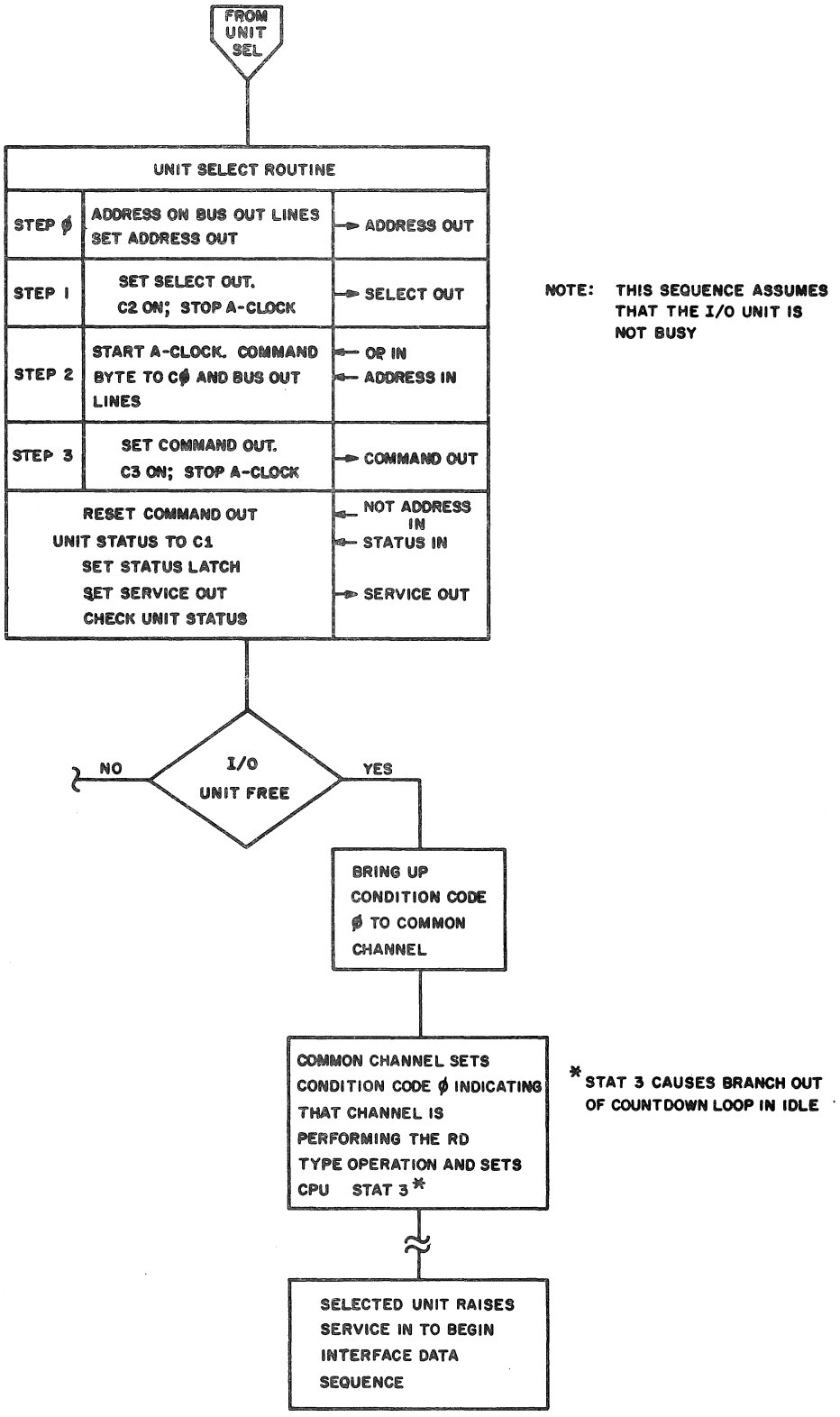


FIGURE 4-10 SELECTOR CHANNEL HARDWARE UNIT SELECT ROUTINE

4-7. UNIT CONTROL WORDS

Up to this time the Selector Channel and the Multiplexor Channel have been treated as separate and independent functional units. In truth, these functional units are so interrelated that the IOCE has special provisions to literally keep track of what it is doing and with whom. Since there are two Selector Channels (possibly three) each capable of sustaining an I/O operation and one Multiplex Channel capable of sustaining up to 256 simultaneous I/O operations, the problem becomes acute. In practice, each Selector Channel is allocated 4 control words to sustain its operation. These words are contained in Local Storage and remain there as long as the channel is operating with the selected device. Each of the possible devices on the Multiplex Channel are assigned 4 control words also. These words, however, are stored in MACH storage and are brought out as required.

There is a great deal of similarity between the control words used for the Selector Channel and those used on the Multiplex. Both for instance contain the Command Address, the updated Data Address, the updated Count, and other information essential to sustaining the device operation. The Selector Channel control words omit information which is stored in hardware registers such as Sequence Controls, Op Codes, Status, and Unit Address. The Multiplex Channel, on the other hand, will use this information for control.

In operation the Multiplex Channel will transfer the control words (UCW) from the location assigned to it in MACH to Local Store when a device requires a data service. The information is used during the routine. When the routine is complete and the device no longer is using the interface, the updated data is transferred back to its assigned locations in MACH. On the Selector Channel the device is always on the interface, the words are retained in Local Store throughout the operation. As part of the ending routine, pertinent data regarding the channel status etc., is placed in the CSW and PSW area of the SE. Some of this data is taken from the Local Store locations and some of it is taken from the hardware latches.

Figure 4-11 is the Local Store map for the IOCE. Notice that provisions have been made for the optional third channel even though this channel may not be installed. Notice also that there is only one group of registers set aside for the Multiplex Channel. This, as was explained previously, is due to the fact that only one device at a time may utilize the channels facilities.

Figure 4-12 is the format of the control words in the MACH Store locations. These words occupy an area of MACH referred to as "BUMP" store, and are unique to the Multiplex Channel. Actually, "BUMP" store is the high order 1024 words of MACH. (4 words x 256 devices) These control words referred to as the UCW will contain the data indicated and present a method whereby the channel can ascertain the previous ending conditions of a device. As a matter of convenience to the microprogrammer the indicated data may be modified by certain routines, however, in the ending analysis the data will be presented as indicated.

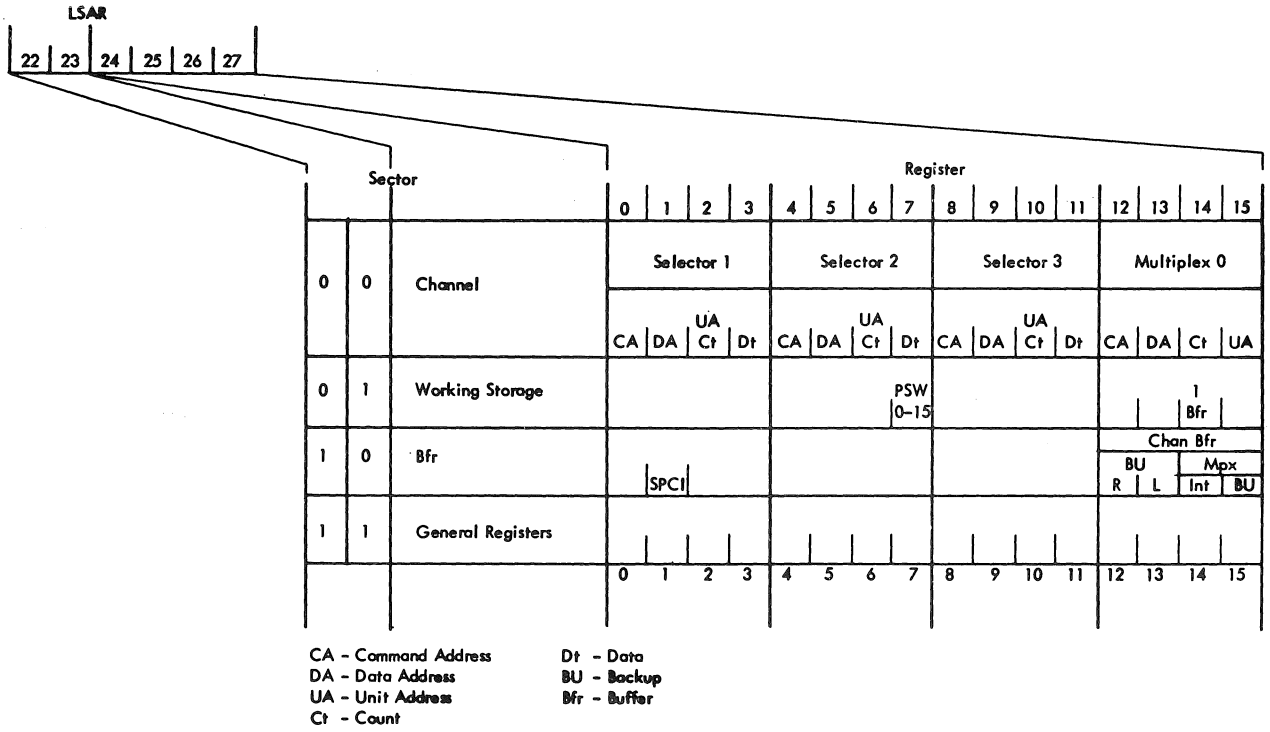


Figure 4-11. Local Store Map for IOCE.

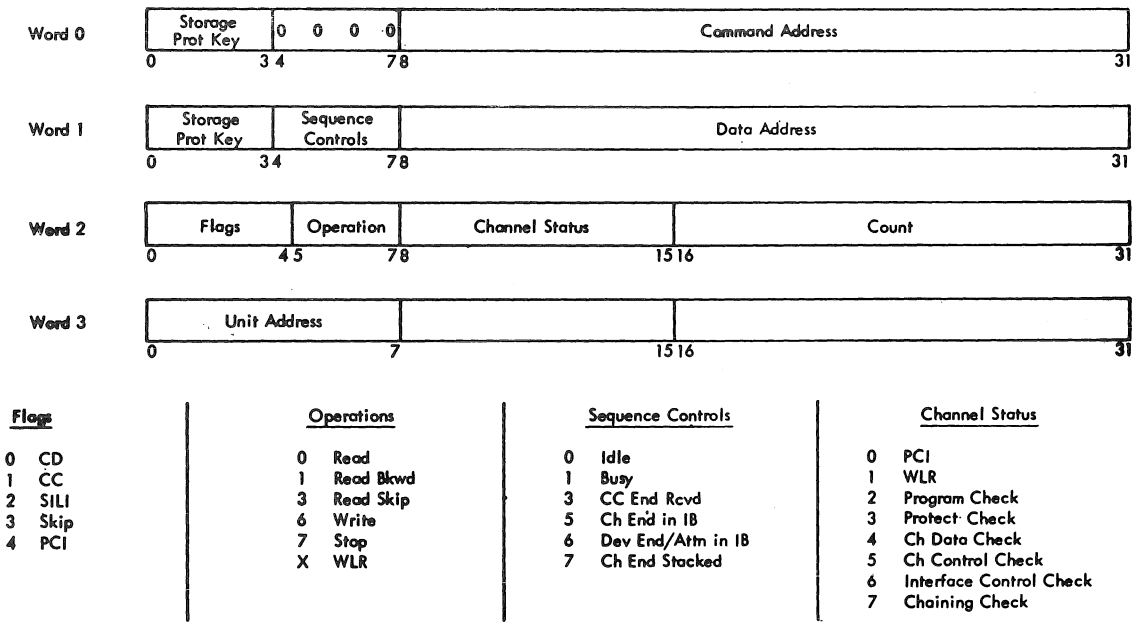


Figure 4-12. UCW Format in MACH Store.

MULTIPLEX

The Selector Channel control words in Local Store are shown for two stages of the operation in Fig. 4-13. Notice that only three words of the allocated Local Store are used, the fourth word serves as the data register for the channel.

This register then may be used should two Selector Channels require the service of an SE simultaneously.

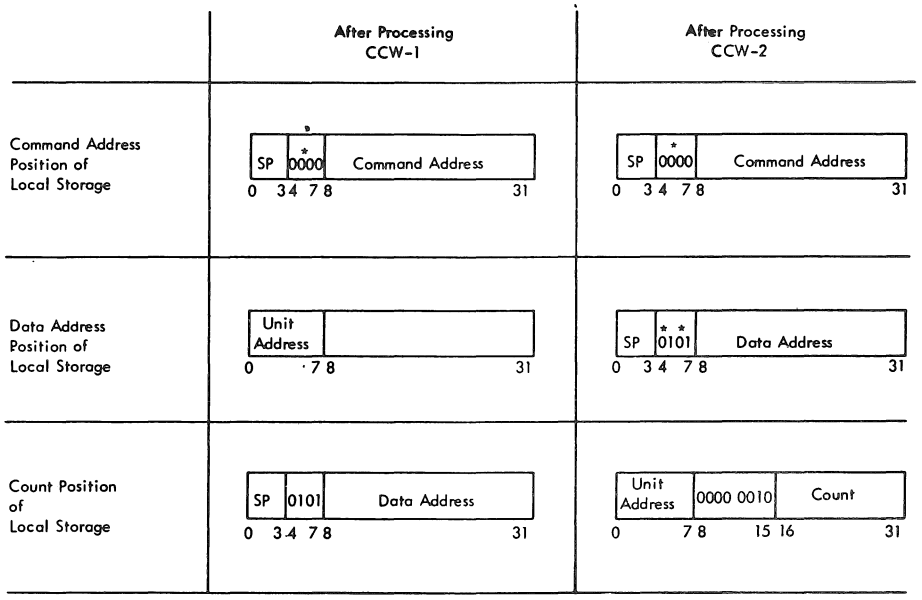


Figure 4-13. Selector Channel Local Store Positions.

4-8. IOCE STANDARD INTERFACE

Data transfers and controls between the IOCE and the external devices are accomplished on a Standard Interface Cable. The block diagram of the standard interface is shown in Fig. 4-14. This connection between the IOCE channels and the I/O control unit provides an information format and a signal sequence common to all control units. The interface consists of a set of 34 lines that connect a number of control units to a channel. Except for signals used to establish selection control, all communications to and from the channel occur over a common bus, i.e., any signal provided by the channel is available to all control units. At any one instant, however, only one control can logically be connected to the channel. Selection of a control unit for communication with the channel is controlled by a signal passing serially through all control units that permits, sequentially, each control unit to respond to the signals provided by the channel. A control unit remains

logically connected on the interface until it transfers the information it needs or has, or until the channel signals it to disconnect.

For purposes of simplicity the I/O interface is divided into five functional categories:

(1) BUS OUT - Used to transmit information (data, I/O device address, commands, control orders) from the channel to the control unit.

(2) BUS IN - Used to transmit information (data, I/O device identification, status information, sense data) from the control unit to the channel.

(3) TAGS - Used for interlocking and controlling information on the buses and for special sequences.

(4) SEL CTRLS - Used for the scanning of, or the selection of attached I/O devices.

(5) METERING - Used for conditioning of elapsed time meters in the various attached units.

A. BUS Information

Each of the buses (in and out) consists of eight information lines and one parity line. Information on the buses is always arranged so that bit position 7 always carries the low order information bits and the bits proceed from right to left, thus any unused information lines will appear in the high order positions (0, 1, 2.....etc.). The information transmitted over the bus is indicated by the appropriate tag line, i.e. when "Address Out" tag is active, the bus out will contain valid address information; when the tag "Status In" is active, the bus in will contain a byte of information describing the status of the I/O device.

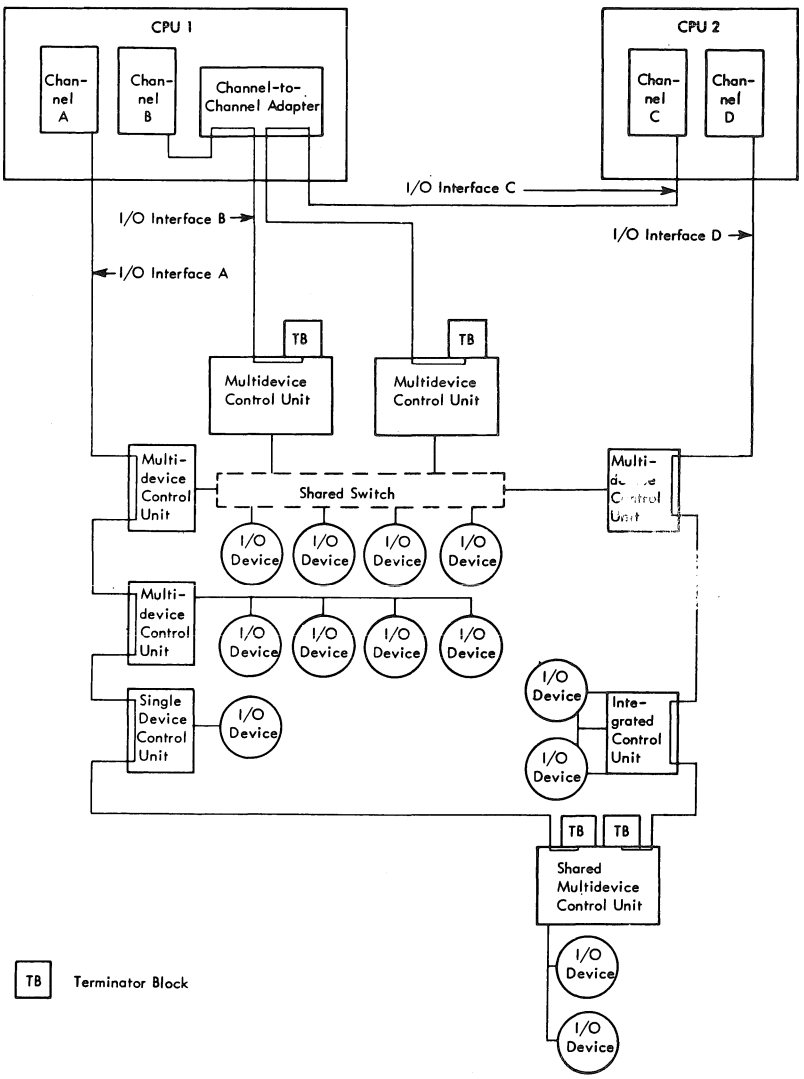


Figure 4-14. Input/Output Interface—Multiple Configurations.

B. Interface Tag Lines

Address-Out: Active during the channel initial selection sequence, bus-out specifies the address of an I/O device.

Command-Out: Active during channel initial selection sequence when the bus-out specifies a command.

Service-Out: Is active in response to a service-in tag during the execution of a Write or Control Command. The data on the bus-out is dependent upon the operation being performed, for instance on a Write the bus will contain the data to be recorded by the I/O device.

Address-In: Is active as a result of channel tag "Address Out" the bus-in at this time will contain the address of the selected I/O device. When this tag line is active, the bus-in contains the address of the currently selected I/O device.

Service-In: Is active during the execution of a read or sense command. The data on the bus-in will depend upon the instruction, for instance on a read command the bus will contain a byte of data from the I/O device.

C. Selection Control Lines

Operational-Out: Used as an interlock to all control units. With the exception of the suppress-out line, all lines from the channel are significant only when the operational-out line is active.

Operational-In: Is a line from all attached control units used to signal channel that an I/O device has been selected, and is communicating with the channel.

Select-Out: Is a line propogated from the channel to the highest priority I/O control unit, and thence from this control unit to the next lower priority unit. This line provides a loop for scanning the attached control units. The Select-Out line returns to the channel as a Select-In line.

Select-In: This line emanates from the lowest priority control unit and provides the return path for the Select-Out line to the channel.

Suppress-Out: Is a line from the channel to the control units and is used both alone and in conjunction with the out-tag to provide the following special functions: Suppress Data, Suppress Status, Command Chaining and Selective Reset.

Request-In: Is a line from all attached control units to the channel. This line is used to signal channel when any control unit has a data service or status service requirement.

D. Metering Control Lines

Metering-Out: Is a line from the channel to the I/O control unit used to condition all attached control unit and device elapsed time meters to run.

Metering-In: Is a line from all attached control units to the channel which permits the system elapsed time indicator to run even though the system may be in the stopped or wait state.

Clock-Out: Is a line from the channel used to indicate that the processor is not stopped or waiting.

Since the 9020 System does not have an elapsed time meter, the metering control lines and clock-out lines are not utilized. Elapsed time meters on the Tape Control Unit, and the 2821 Integrated Control Unit must however be enabled for these units to function.

4-9. IOCE STAND ALONE OPERATION

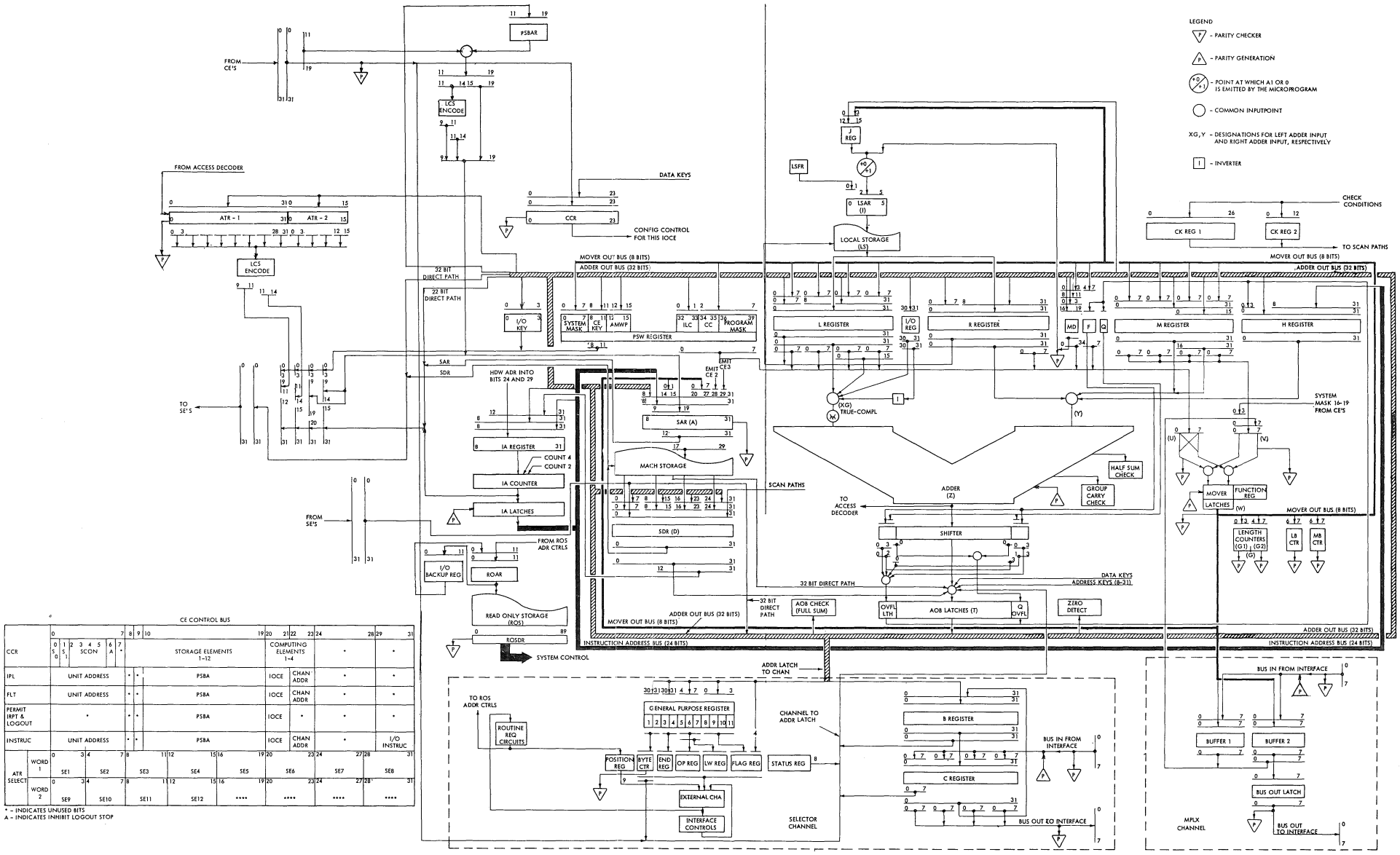
To facilitate the maintenance of the 9020 System each of the elements associated with the system are capable of certain manual operations. These operations are normally limited in their scope since no single element up to this time contains all of the essential logic circuitry. The IOCE however contains all of the facilities to perform as a standalone computer. The IOCE contains its own internal control (ROS), it contains its own common logic unit for processing data (CLU), it contains its own storage capability (8K MACH), and it contains logic to permit communication with the external environment (Channel - I/O, and I/O - Channel).

To make use of this unique feature of the IOCE it is necessary that the IOCE be placed in the "Diagnostic" mode. (Any time there is no CE bit on in the IOCE Configuration Control Register the IOCE is in the Diagnostic Mode.) If it is desired to further isolate the IOCE from the operating system, the test switch may be turned on (down).

When operating in the diagnostic mode the IOCE closely resembles the operation of the IBM System 360/Model 50. That is, it is capable of performing Initial Program Loads, (IPL) executing the standard Model 50 instruction set (no Floating Point or Decimal features), and processing the normal interrupts. It should be borne in mind however that the size of the programs is limited by the 8K of available storage. This storage is not all available to the program since the upper 1024 words are utilized as channel UCW area, and the lower 256 bytes are designated for PSW's, CAW, CSW, and the Diagnostic Scan-out area.

The diagnostic standalone capabilities of the IOCE are primarily intended for use in element maintenance programs such as the Fault Locating Tests and the Sub-System Diagnostic Monitor. This does not preclude the possibility of utilizing this feature for running the Diagnostic Sections used for testing the Various I/O devices, nor for the execution of small scale programs. As previously mentioned the size of these programs is limited by the storage available.

The ability to use the IOCE as a standalone processor permits the technician or engineer to use this element to "bootstrap" the system up to operating capability. Since all of the maintenance programs require some form of input device, the technician or engineer may, with built-in tests and FLT's, verify the operation of the IOCE. Then using the pre-tested IOCE, and the SDM tests, he may verify the operation of the Storage Element. He may then, with a manually configured system use the IOCE and SE to load the FLT's for testing the CE. He may then use the FLT's to locate and correct any CE malfunctions. Having accomplished this the engineer or technician may run the MDM's and SEVA tests to assure the systems operation.



CE CONTROL BUS

		0	1	2	3	4	5	6	7	8	9	10	19	20	21	22	23	24	28	29	31
CCR		0	S	S	SCON				7	*		STORAGE ELEMENTS 1-12		COMPUTING ELEMENTS 1-4				*		*	
		0	0	1					A												
IPL		UNIT ADDRESS								*	*	PSBA		IOCE		CHAN ADDR		*		*	
FLT		UNIT ADDRESS								*	*	PSBA		IOCE		CHAN ADDR		*		*	
PERMIT INPT & LOGOUT		*								*	*	PSBA		IOCE		*		*		*	
INSTRUC		UNIT ADDRESS								*	*	PSBA		IOCE		CHAN ADDR		*		I/O INSTRUC	
ATR SELECT	WORD 1	0		3	4		7	8		11	12		15	16		19	20		23	24		27	28		31
		SE1			SE2			SE3			SE4			SE5			SE6			SE7			SE8	
	WORD 2	0		3	4		7	8		11	12		15	16		19	20		23	24		27	28		31
		SE9			SE10			SE11			SE12			****			****			****			****	

* - INDICATES UNUSED BITS
A - INDICATES INHIBIT LOGOUT STOP

Figure 4 - 15 IOCE Data Flow Registers

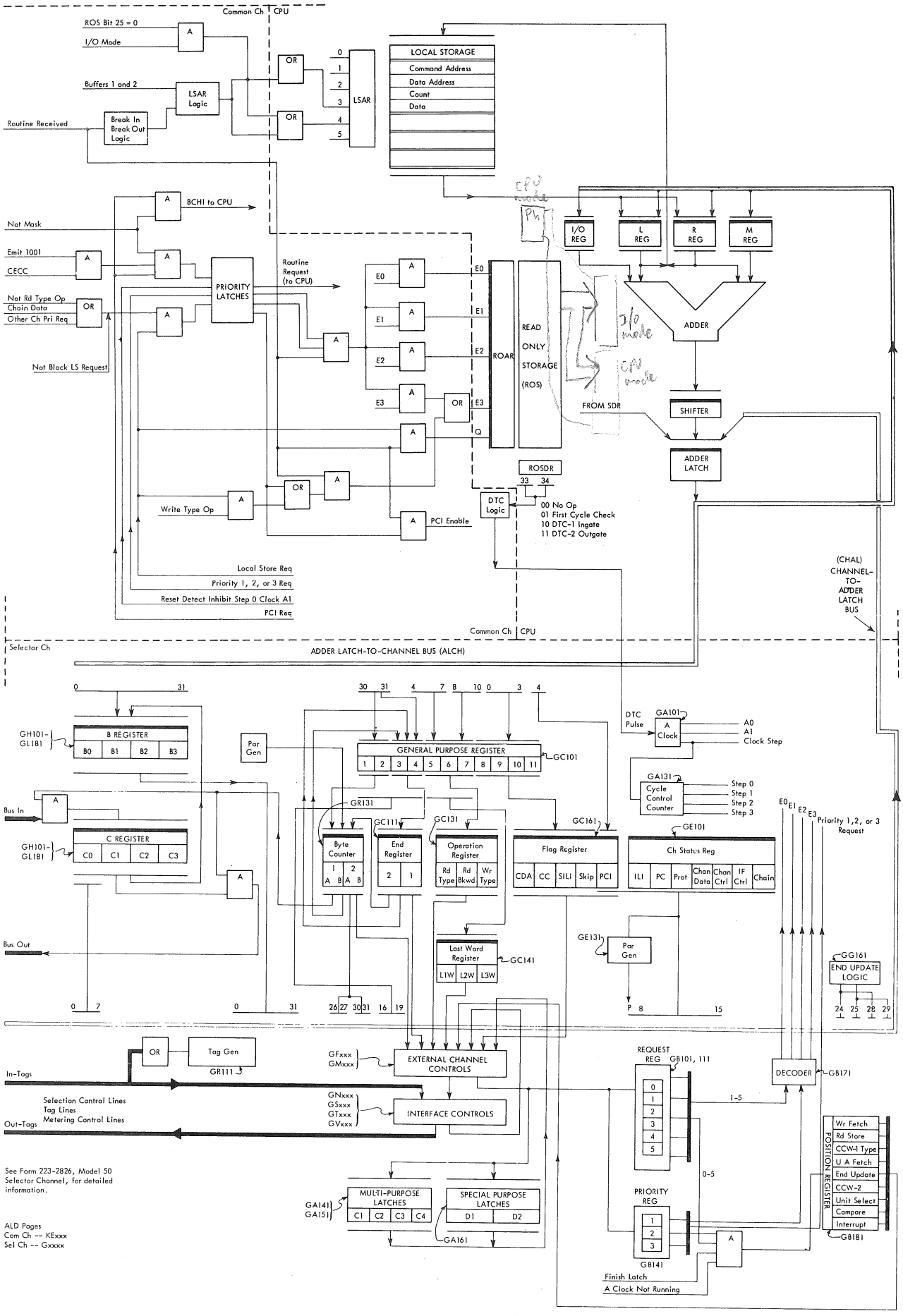
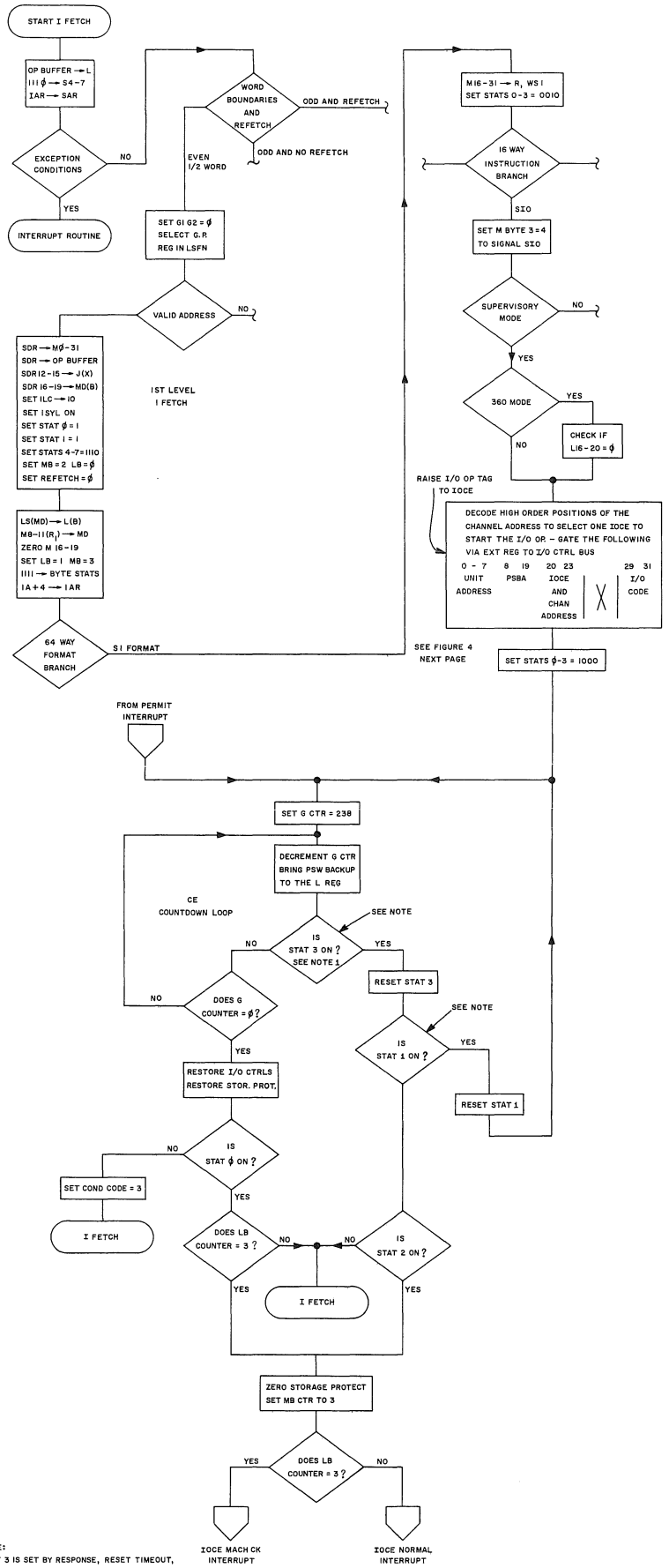


Figure 4 - 16 Functional Units of Selector Channel



NOTE:
STAT 3 IS SET BY RESPONSE, RESET TIMEOUT, PSBAR LOCKOUT, ELEMENT CHECK, OR MACH CK, IN THE LATTER 3 CASES CONDITION CODE 3 WILL ALSO BE SET BY HARDWARE.
STAT 1 WILL BE SET BY RESET TIMEOUT FROM THE SELECTED IOCE UNDER NORMAL CONDITIONS.
ELEMENT CK, PSBAR LOCKOUT, OR IOCE MACHINE CK, WILL BLOCK RESET TIMEOUT AND RESET STAT 2. (FOR IOCE NORMAL PERMIT INTERRUPT ONLY)

FIGURE 4-17 COMPUTE ELEMENT START I/O, INTERRUPT

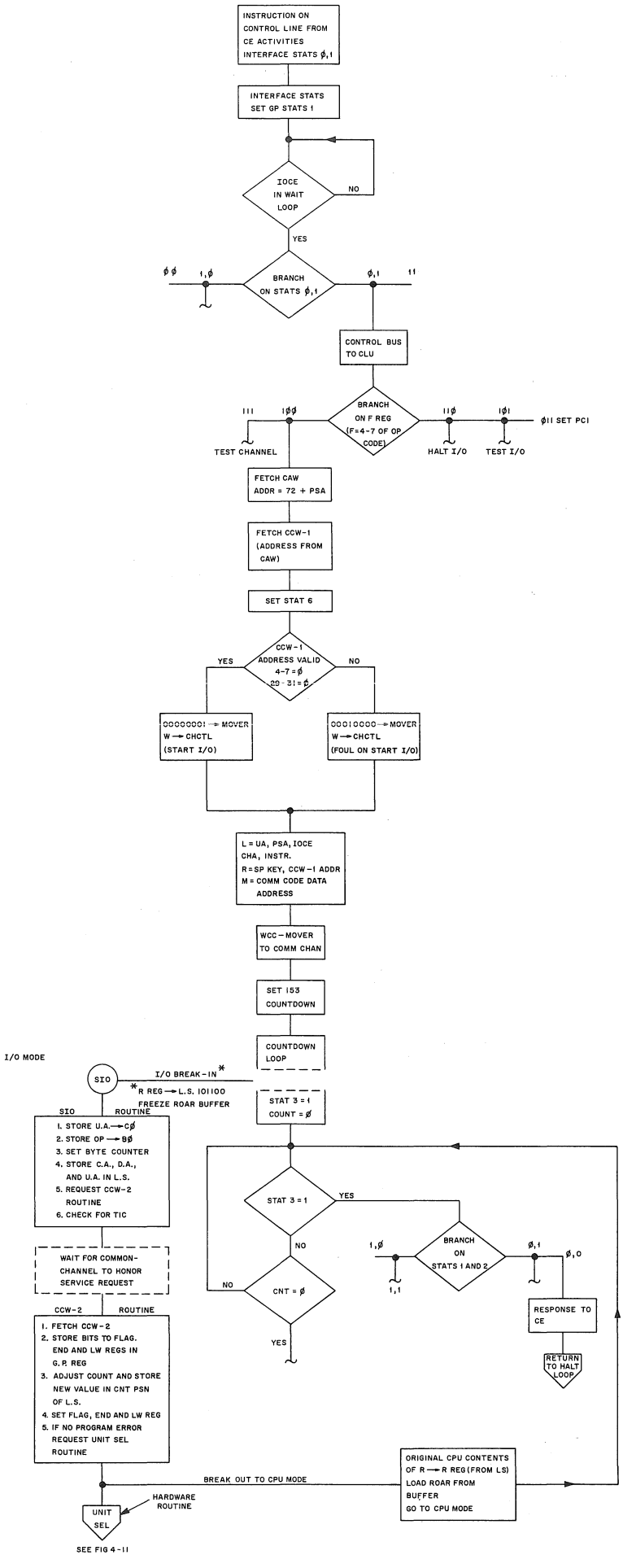


FIGURE 4-18 IOCE START I/O

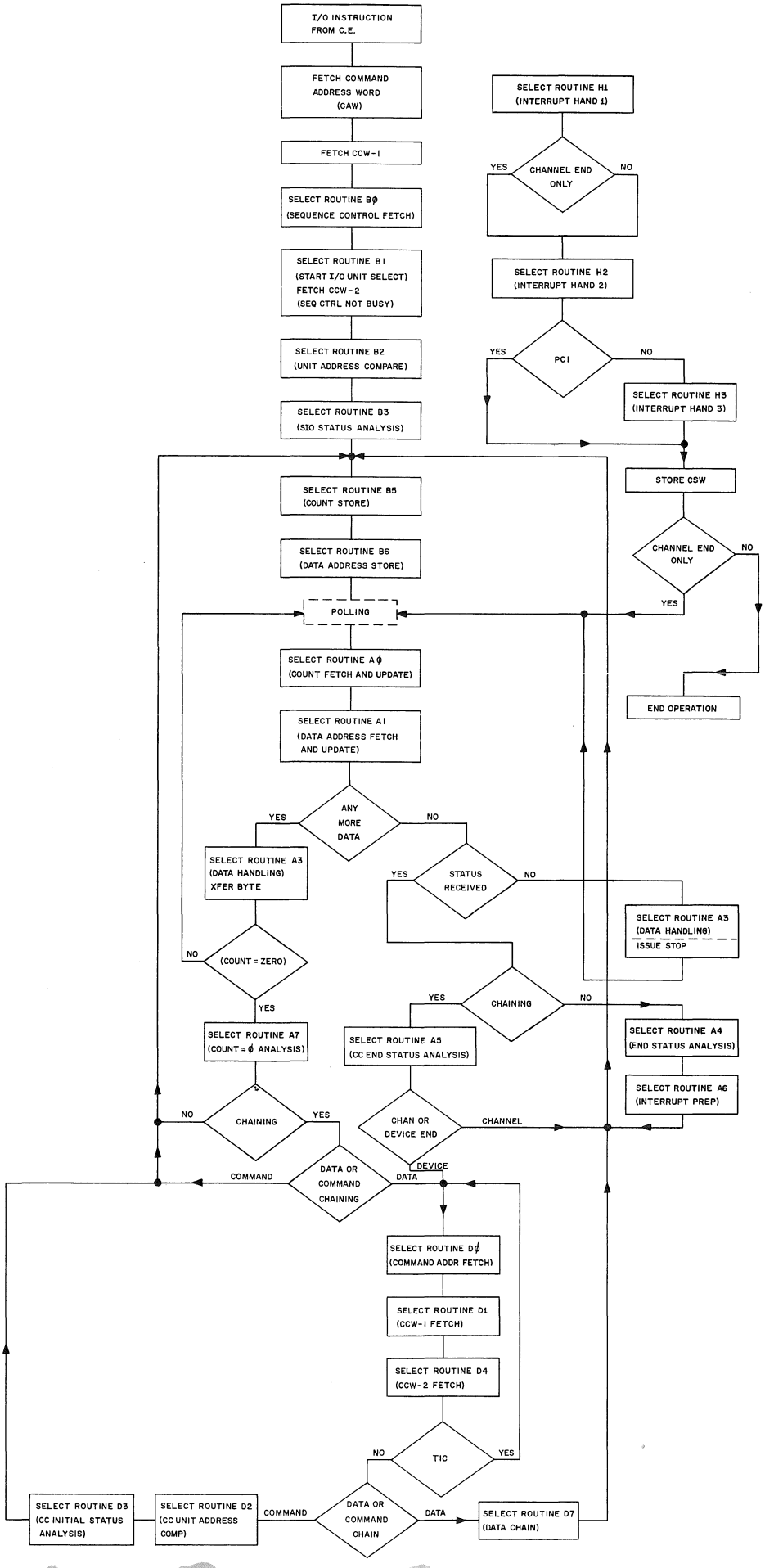


FIGURE 4-19 IOCE MULTIPLEX CHANNEL ROUTINE SELECTION SEQUENCE

CHAPTER 6

IBM-9020 SYSTEM OPERATION

6-1. INTRODUCTION

The previous chapters have presented the characteristics of the individual elements that make up the IBM-9020 System. This chapter will consider the operation of the elements within a system environment.

The IBM-9020 System is designed to provide maximum hardware control through program initiated and monitored actions. Included are such features as system organization, system control, and system monitoring. Therefore, these features and the programming procedures for their operations will be examined in detail.

A. Addressing

Within the multielement system there are generally several different circuit paths through which I/O devices can be addressed. The IBM scheme of addressing, for input/output control units and devices, is a function of the control unit, the number of devices connected to the control unit, and the accessing path. The scheme can be divided basically into two parts:

Addressing for control units with only one attached input/output device.

Addressing for control units with more than one attached input/output device.

The device and control unit address is formed by the two low order Hex digits of the address whereas the high order digit of the three digit address defines the accessing path.

1. Addressing to Control Units with Only One Attached I/O Device

The address of an input/output device is made up of the low order 8 bits (2 hex digits). The decode of this address is shown in the following example:

3 Hex Digit Address

X	X	X
0 0 0 0	0 0 0 0	0 0 0 0
IOCE	Channel	I/O Device Address
Four bits used to identify the accessing path.		Eight bits used to address the device.

In applying this addressing scheme the 2821 Integrated Control Unit is considered to be three control units with one I/O device per control unit. The first fifteen addresses will be reserved for the I/O devices located on the computer complex floor. At the time of this writing the addresses are assigned as follows: 01 will be the address of the System Console, the 1052 Typewriter with its adapter on the SC will be assigned an address of 02, the Card Reader an address of 03, the Card Punch an address of 04, the High Speed Printer an address of 05, etc. Therefore, if one were addressing the High Speed Printer via IOCE1 and its associated multiplexor channel, the three hex digit address is shown in the following example:

3 Hex Digit Address

X	X	X
0	0	5
0 0 0 0	0 0 0 0	0 1 0 1
IOCE	Channel	Device Address

In a triplex system one might desire to access the High Speed Printer (address 05 via IOCE2) provided the system console interface switch is set for IOCE2. The address used would be as follows:

X	X	X
4	0	5
0 1 0 0	0 0 0 0	0 1 0 1

IOCE2 Channel 4 Device Address

Or if the same high speed printer were to be accessed via IOCE3 (provided the system console interface switch is set for IOCE3), the address used would be as follows:

X	X	X
8	0	5
1 0 0 0	0 0 0 0	0 1 0 1

IOCE 3 Channel 8 Device Address

The above examples hold true for the addressing scheme assigned to the Peripheral Adapter Module (PAM) which basically can be looked at as one control unit with one I/O device for each control adapter. The first 16 address is reserved for the devices on the computer complex. The PAM adapters are assigned a two hex digit address dependent upon the adapter priority for a particular center.

For example, assume that one was addressing 03C (the 1052) via PAM1, IOCE1, and multiplexor channel zero, the address would be as follows:

X	X	X
0	3	C
0 0 0 0	0 0 1 1	1 1 0 0

IOCE1 Channel 0 Device Address

If for some reason one could not access the device through this adapter, there is a secondary 3C adapter located in PAM3 which can be accessed through the same path. However, the program must issue a command which will set the secondary latch for access. Therefore, one reaches the same device via the same accessing path (IOCE 1 and CH 0) but through a different or secondary adapter located in PAM3. The command used to access the secondary address is called Pass Address.

2. Addressing Scheme to Control Units with More Than One I/O Device

The addressing scheme used in this case differs from the preceding example in that the eight bit address is divided such that the low order hex digit is reserved to address the I/O devices to be attached. The next lower order hex digit is reserved for the tape control unit. An example of this addressing scheme is shown in the following example:

X	X	X	
1	1	0	- - - Hex Digit
0 0 0 1	0 0 0 1	0 0 0 0	
IOCE1 Channel 1	Control Unit #1	Device Address - Tape Drive #0	

Possibility of 16 I/O devices could be attached with this boundary.

This address is an access to Tape Control Unit #1 and Tape Drive #0 via IOCE1 and Selector Channel #1. As pointed out on the subject of interfacing, the Tape Control Unit may be accessed via two distinct selector channel paths through an interface switch. This transfer of interfaces may be accomplished by program by an assigned command to the Tape Control Unit. The interface switch also has a neutral position and if it is in this position, the switch will be transferred to the selector channel on which an access is attempted. However, if the interface switch is set on one or the other selector channels

it must be transferred by program to the neutral position before access can be made on the alternate channel. Therefore, in the example used on the Tape Control Unit above only the high order digit of the address would be changed to correspond to the accessing IOCE and selector channel.

3. Address Modification

The address of particular control units may be changed by manual alteration of the address cards or by a switch which will enable access through another channel as described earlier. To perform the manual modification refer to the example given in Fig. 6-1, which is an address card used in the card reader.

B. Storage Address Translation

The following discussion does not include the (08) Storage Element which is proposed at the time of this writing to be included in the IBM-9020 System. Material which will show the modifications necessary to include the Model 08 SE into the 9020 System will be issued as supplementary handout or eventually incorporated in an appendix.

This feature significantly increases the flexibility of the 9020 System and its ability cope with malfunctions. The IBM-9020 System used Storage Elements (SE) with a capacity of 131,072 bytes (32,768 words), and large capacity storage (LCS) elements with a capacity of 1,048,576 bytes (262,144 words). A maximum of 12 Storage Elements per system may be installed. Three of the 12 may be LCS elements.

The ability to place a particular main storage (logical) address in any physical Storage Element requires the use of a programmable address translator and additional decoding. The address translator (ATR)--see Functional Units section of this manual--contains 12 four-bit positions. Each of these positions is assigned to a block of logical addresses. The bit configuration within a selected position determines the physical storage element to be used.

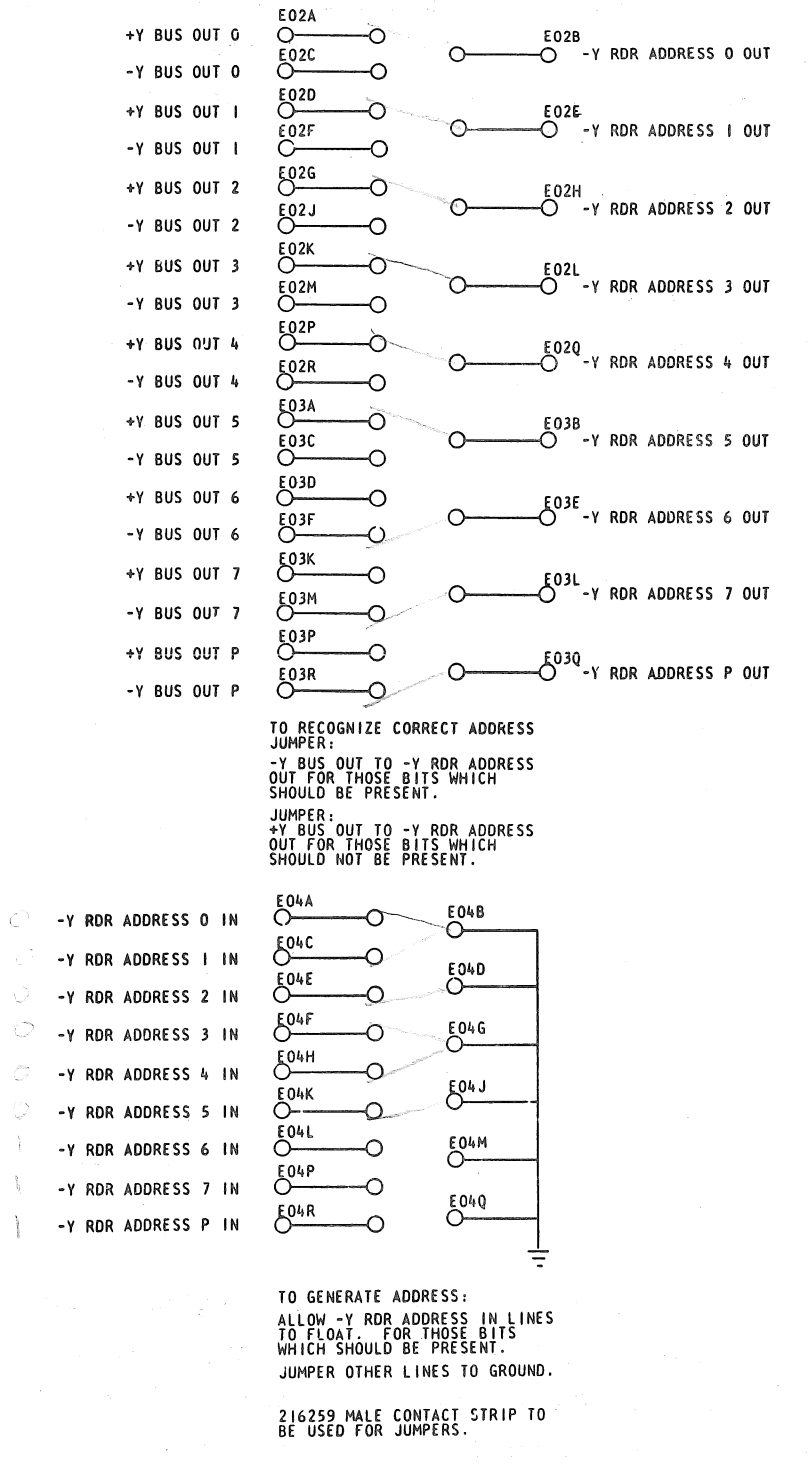


Figure 6-1. Example of an Address Card.

Basically, address translation is accomplished as follows:

Bits 9-14 of a main storage address (logical) are decoded. This decoding will select one four-bit position of the 12-position address translator (ATR) for additional decoding. The bit configuration found in this position of the ATR is now decoded to determine which physical storage element is to be accessed. This physical storage element will then be sent an access request if the SE's bit is on in the CE's configuration control register. See Figs. 6-2 and 6-3.

With no LCS elements present, each position of the ATR represents a block of 131,072 bytes. For example, position one of the ATR would be decoded if the logical address was between byte 0 and 131,071. If the logical address was between byte 131,072 and 262,143, position two of the ATR would determine the physical SE to be used. For the range of logical addresses assigned to each position of the ATR with and without LCS elements present, see Fig. 6-4.

As mentioned previously, a maximum of three LCS elements may be installed; ATR positions 10, 11, and 12 are assigned to LCS elements when required. The starting address for LCS is constant and is byte 2,097,152. When one LCS element is present, position 12 of the ATR is used and refers to a 1,048,576 byte block of storage starting at byte 2,097,152 and extending through byte 3,145,727. When two LCS elements are present, positions 11, and 12 of the ATR are used and refer to two 1,048,576 byte blocks starting at byte 2,097,152 and extending through byte 4,194,303. Similarly, when three LCS elements are present, positions 10, 11, and 12 of the ATR are used and refer to three 1,048,576 byte blocks starting at byte 2,097,152 and extending through byte 5,242,879.

1. Logical Address

For simplicity, a logical address may be considered as shown in Fig. 6-5. For an SE, bits 20-31 pick out a byte within a 4096 byte sector of storage.

Bits 15-19 specify a 4096 byte sector. Bits 9-14 specify an ATR position. Decoding of logical address bits 9-14 follows:

Bit						ATR Position
9	10	11	12	13	14	
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
0	0	0	1	0	0	5
0	0	0	1	0	1	6
0	0	0	1	1	0	7
0	0	0	1	1	1	8
0	0	1	0	0	0	9
0	0	1	0	0	1	10
0	0	1	0	1	0	11
0	0	1	0	1	1	12

When large capacity storage elements are addressed, in addition to the decoding mentioned previously for an SE, bits 12-14 specify a 131,072 byte section of an LCS. Bits 9-11 specify an ATR position. Decoding of bits 9-11 when LCS elements are present follows:

Bit			ATR Position
9	10	11	
0	1	0	LCS 1
0	1	1	LCS 2
1	0	0	LCS 3

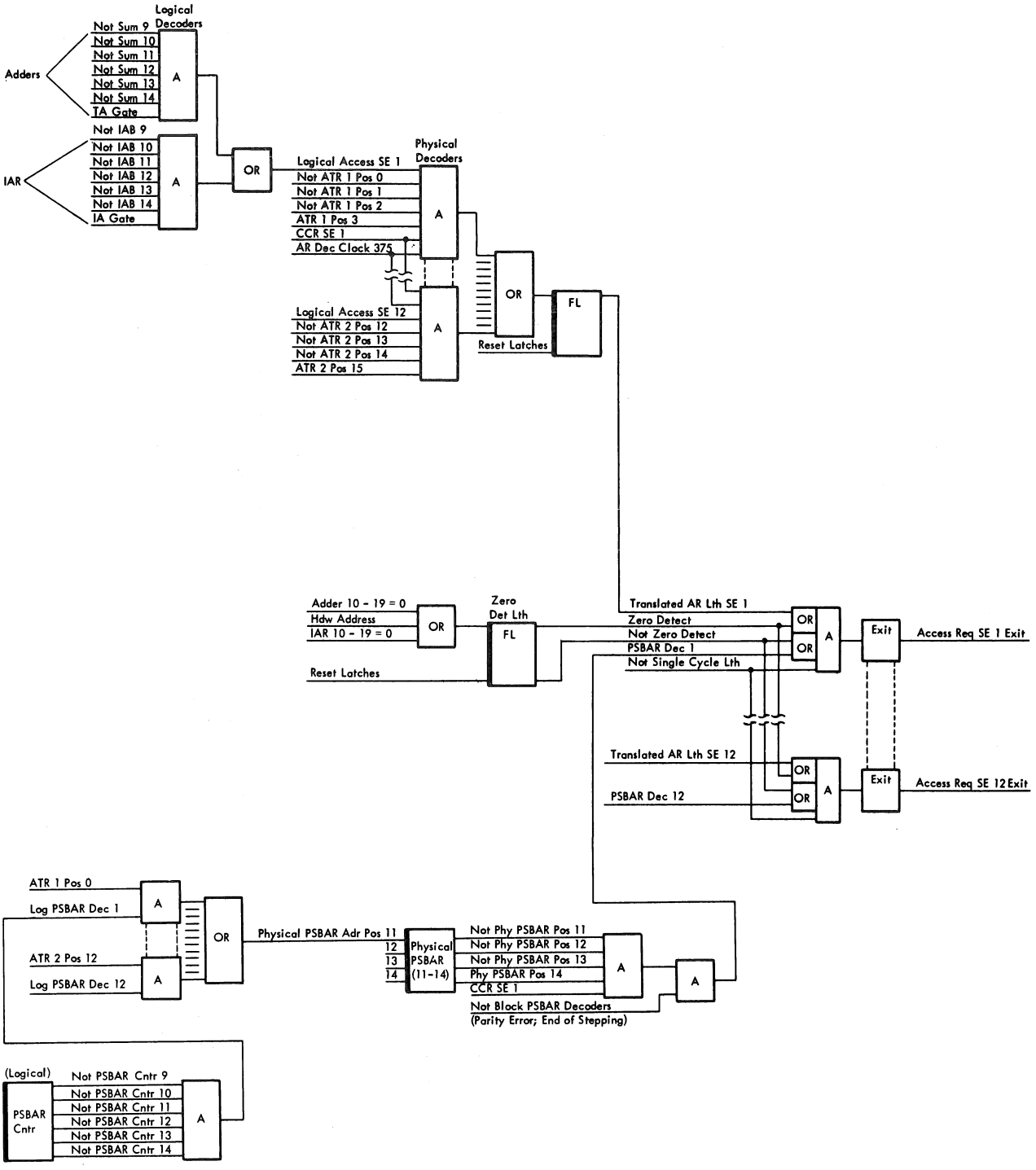
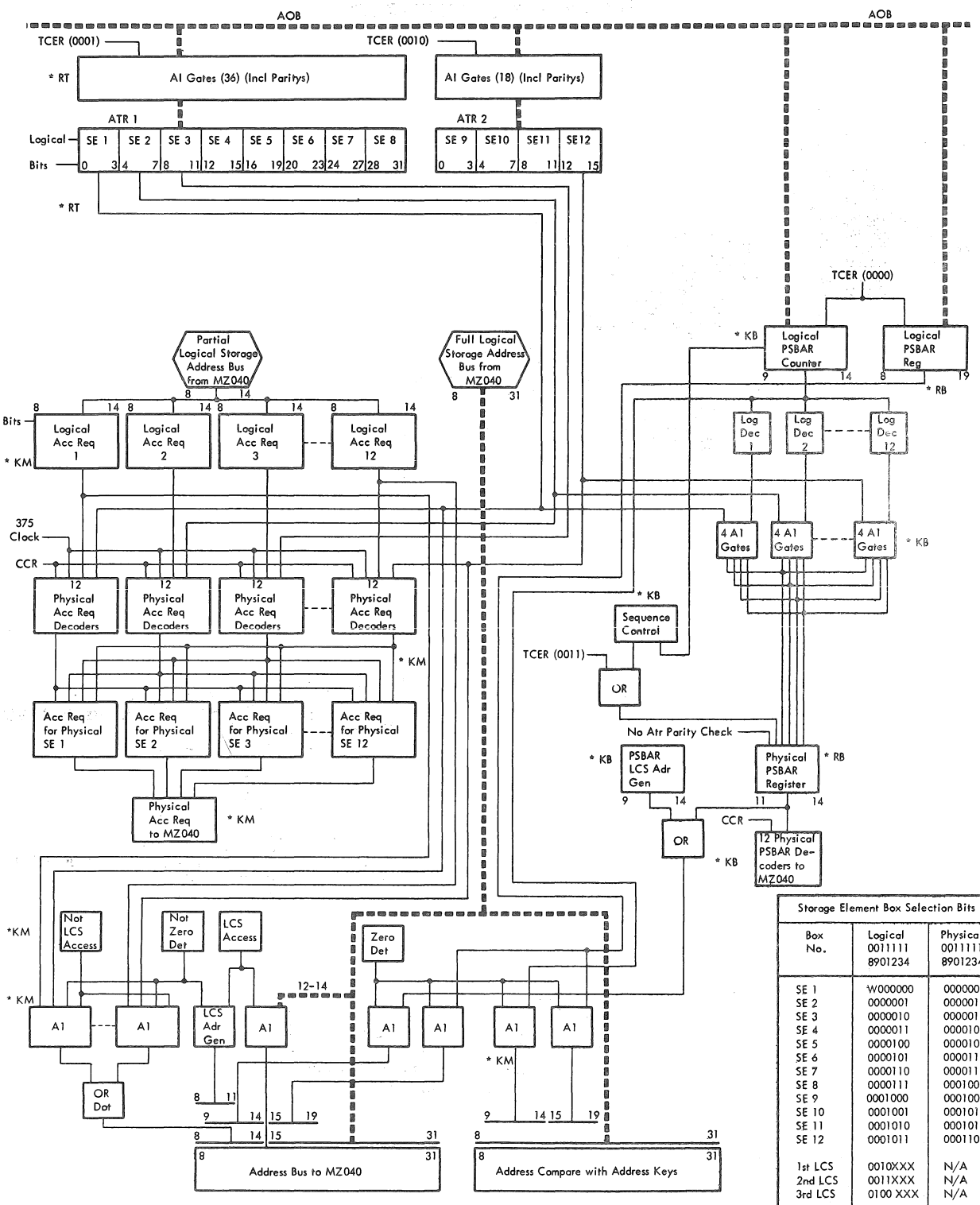


Figure 6-2. Storage Access Decoding.



Storage Element Box Selection Bits		
Box No.	Logical 0011111 8901234	Physical 0011111 8901234
SE 1	W000000	0000001
SE 2	0000001	0000010
SE 3	0000010	0000011
SE 4	0000011	0000100
SE 5	0000100	0000101
SE 6	0000101	0000110
SE 7	0000110	0000111
SE 8	0000111	0001000
SE 9	0001000	0001001
SE 10	0001001	0001010
SE 11	0001010	0001011
SE 12	0001011	0001100
1st LCS	0010XXX	N/A
2nd LCS	0011XXX	N/A
3rd LCS	0100 XXX	N/A
LCS 10	N/A	0010XXX
LCS 11	N/A	0100XXX
LCS 12	N/A	0111XXX

W=0, May be 1 for Diagnose
X= Don't Care
Phy=Logical Octant Select Bits.

Note:
1. If 1 LCS is present it is No. 12.
2. If 2 LCS's are present they are 11 and 12.
3. If 3 LCS's are present they are 10, 11 and 12.
4. * = ALD page group.

Figure 6-3. ATR and PSBAR Data Flow.

Range of Addresses When the Number of LCS Modules in the Installation Is:

Address Translator Position	None		One		Two		Three	
	From	To	From	To	From	To	From	To
1	000,000	131,071	000,000	131,071	000,000	131,071	000,000	131,071
2	131,072	262,143	131,072	262,143	131,072	262,143	131,072	262,143
3	262,144	393,215	262,144	393,215	262,144	393,215	262,144	393,215
4	393,216	524,287	393,216	524,287	393,216	524,287	393,216	524,287
5	524,288	655,359	524,288	655,359	524,288	655,359	524,288	655,359
6	655,360	786,431	655,360	786,431	655,360	786,431	655,360	786,431
7	786,432	917,503	786,432	917,503	786,432	917,503	786,432	917,503
8	917,504	1,048,575	917,504	1,048,575	917,504	1,048,575	917,504	1,048,575
9	1,048,576	1,179,647	1,048,576	1,179,647	1,048,576	1,179,647	1,048,576	1,179,647
10	1,179,648	1,310,719	1,179,648	1,310,719	1,179,648	1,310,719	2,097,152	3,145,727
11	1,310,720	1,441,791	1,310,720	1,441,791	2,097,152	3,145,727	3,145,728	4,194,303
12	1,441,792	1,572,863	2,097,152	3,145,727	3,145,728	4,194,303	4,194,304	5,242,879

Figure 6-4. Translator Logical Address Assignments.

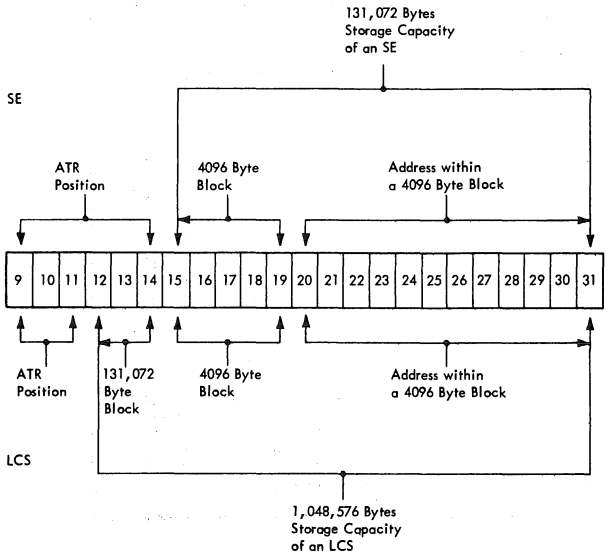


Figure 6-5. Logical Address Decoding.

2. Physical Address

The physical address refers to the physical SE or LCS element specified by the selected position of the ATR. There is no difference between a physical and logical address for those positions of the address that are used internally by the particular storage device for addressing (bits 15-29 for an SE and bits 12-29 for an LCS). See Fig. 6-6 for physical storage module identifiers.

The contents of the ATR may be altered or examined. See the instructions Set Address Translator (SATR) and Insert Address Translator (IATR) in the instruction section of this manual. The ATR may be entered or displayed manually from the CE's control panel during maintenance (state zero, test switch on).

Storage Module Referenced When the Number of LCS Elements in the Installation Is:

Storage Module Identifier (Hexadecimal)	None	One	Two	Three
0		Unassigned Position		
1	SE 1	SE 1	SE 1	SE 1
2	SE 2	SE 2	SE 2	SE 2
3	SE 3	SE 3	SE 3	SE 3
4	SE 4	SE 4	SE 4	SE 4
5	SE 5	SE 5	SE 5	SE 5
6	SE 6	SE 6	SE 6	SE 6
7	SE 7	SE 7	SE 7	SE 7
8	SE 8	SE 8	SE 8	SE 8
9	SE 9	SE 9	SE 9	SE 9
A	SE 10	SE 10	SE 10	LCS 1
B	SE 11	SE 11	LCS 1	LCS 2
C	SE 12	LCS 1	LCS 2	LCS 3
D, E, F	Invalid Identifiers			

Figure 6-6. Storage Module Identifiers.

1. PSBAR Handling

Computer control and status information is located in a section of storage known as the preferential storage area (PSA). Single computer configurations generally set aside a low-order portion of main storage for this purpose.

Multi-computer configurations require the ability to use any portion of storage as a PSA. In addition, for greater reliability, a computing element (CE) must be able to transfer its PSA to an alternate storage element (SE) if trouble arises in the primary SE.

The logical preferential storage base address register, PSBAR counter, and physical PSBAR provide the 9020 System with the capability of locating the PSA of a CE in any 1024-word section of any 32K SE. A large capacity storage element may have a PSA located in any 1024-word section of the low-order 32K words. For maximum safety and reliability, no more than one primary and/or alternate PSA should be located in an SE.

In normal address translation, bit positions 9-14 of a logical main storage address are decoded to select a position of the ATR. The identifier in this position of the ATR then determines the physical module to be accessed. When the PSA is required, the value of physical PSBAR determines the physical module to be used.

The value of physical PSBAR is determined by the content of the ATR position specified by the PSBAR counter. The instruction LPSB loads the logical PSBA register and counter. The counter positions (9-14) specify an address translator position. The value found in this ATR position is placed in physical PSBAR. The content of physical PSBAR is retained until replaced by another LPSB, an IPL, PSW restart, external start, a condition that causes PSBAR stepping, or by a change in the identifier appearing in the position of the ATR specified by the PSBAR counter. See Fig. 6-7.

When the 12 high-order bits of an address are zeros, the effective address is developed by OR'ing bits 15-19 of the logical PSBAR and bits 11-14 with 9 and 10 = 0 of the physical PSBAR (bits 9, 10, and 11 are independently generated with 12, 13, and 14 = 0 when accessing an LCS) into the 12 high-order positions of the address. Since the content of physical PSBAR is always available in translated form, references to the preferential storage area are completed without repeated reference to the address translator.

The move to an alternate PSA, when necessary, is accomplished automatically by the system. No manual intervention is required. PSAs may also be altered under program control.

All interrupts and logouts require PSBAR. IOCE references to channel address and channel status words also require the use of PSBAR.

The PSBAR counter will step to an alternate PSA if:

A storage check or fetch cycle error occurs in an SE and the PSA is located in that SE.

A 25-ms check occurs and the program is addressing the PSA.

An invalid address check occurs and the program is addressing the PSA.

The CE receives an external start.

The CE receives a reconfiguration select with PSBAR Element Check on. See Figs. 6-8, 6-9, and 6-10.

The PSBAR counter will step until an ATR position is reached whose identifier references a configured storage module. This is equivalent to inspecting the ATR from left to right, starting at the position that references the primary PSA and proceeding until the first identifier for a configured storage module is found. When the alternate PSA is reached, physical PSBAR is updated by the contents of this configured ATR position.

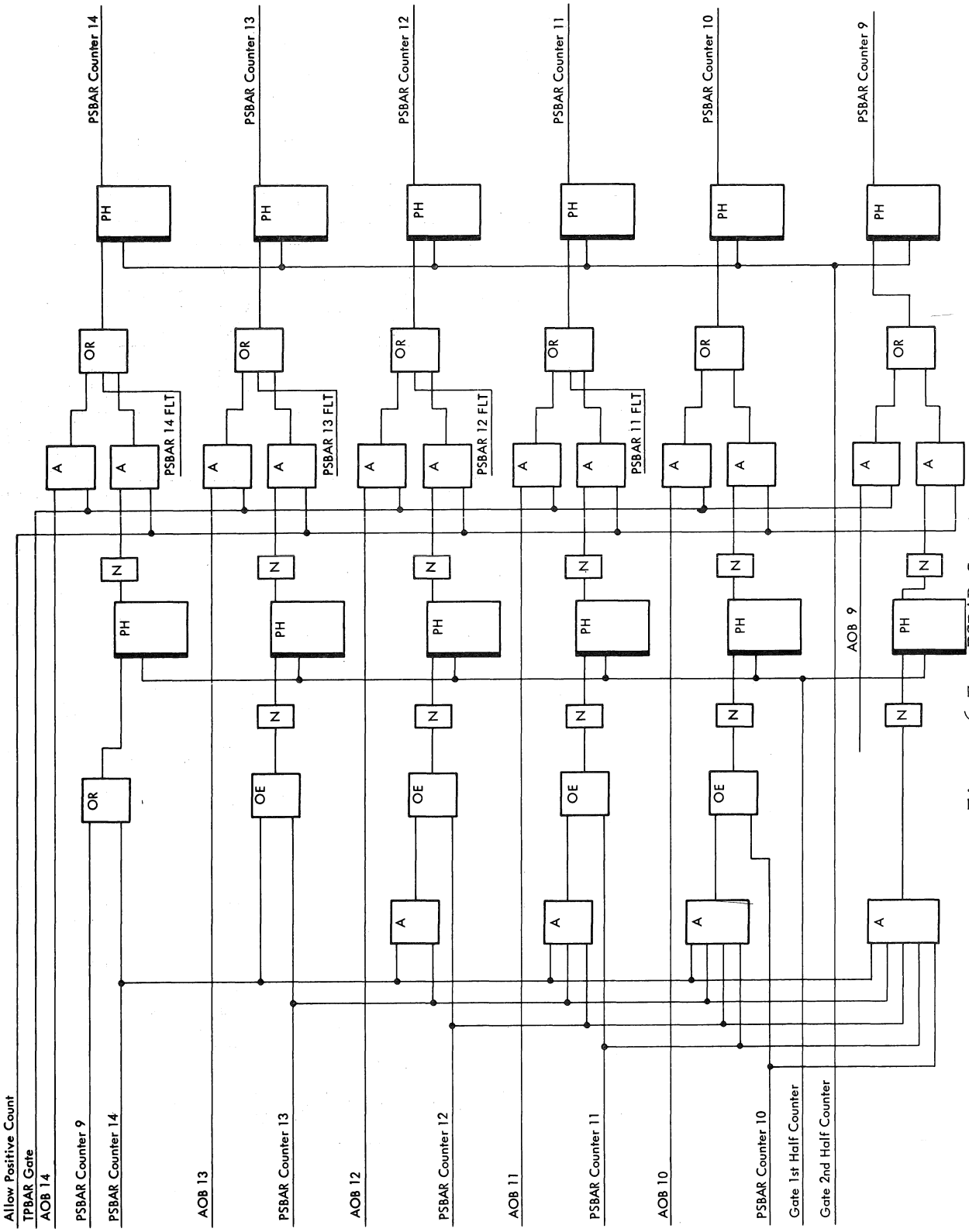


Figure 6-7. PSBAR Counter.

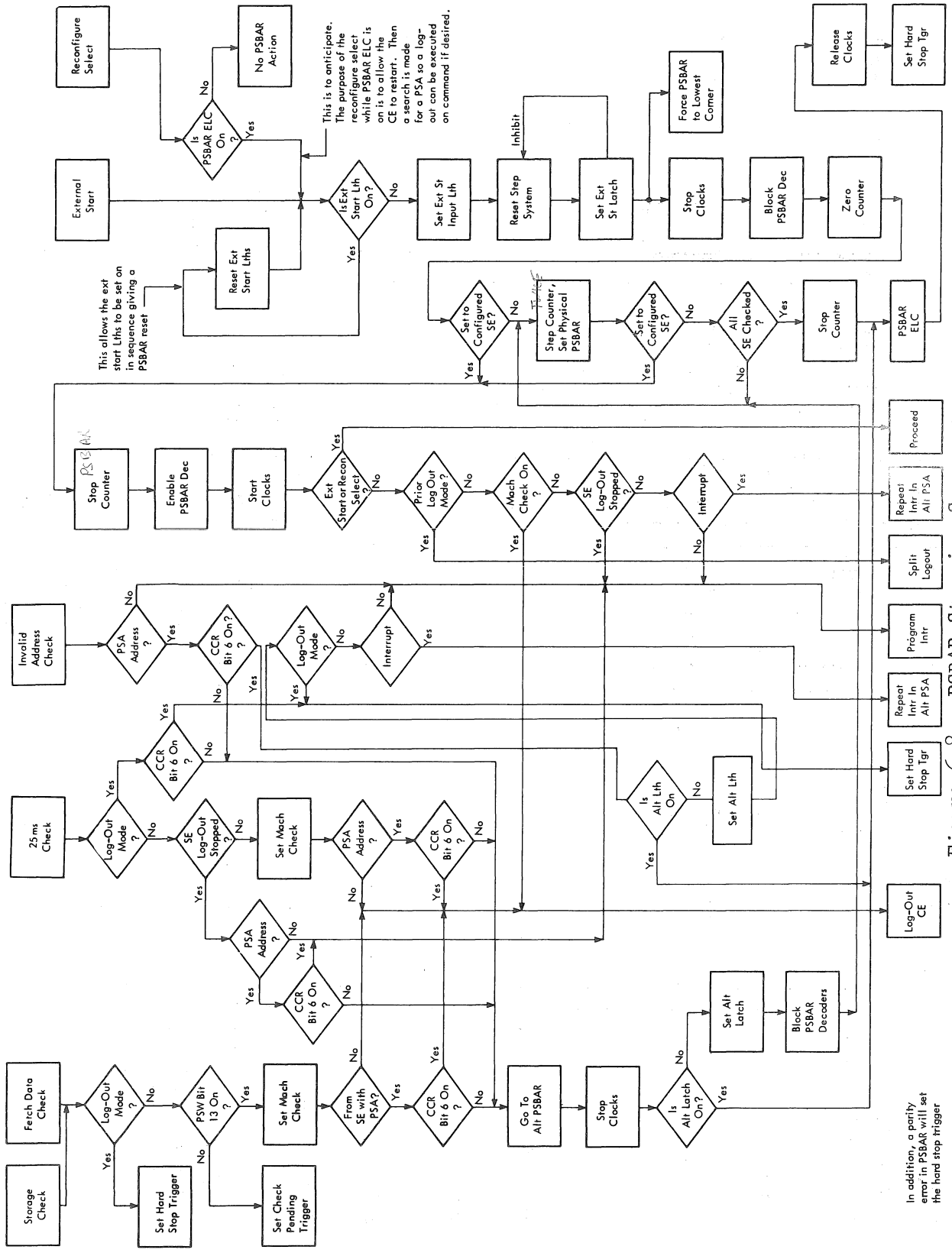


Figure 6-8. PSBAR Stepping Sequence.

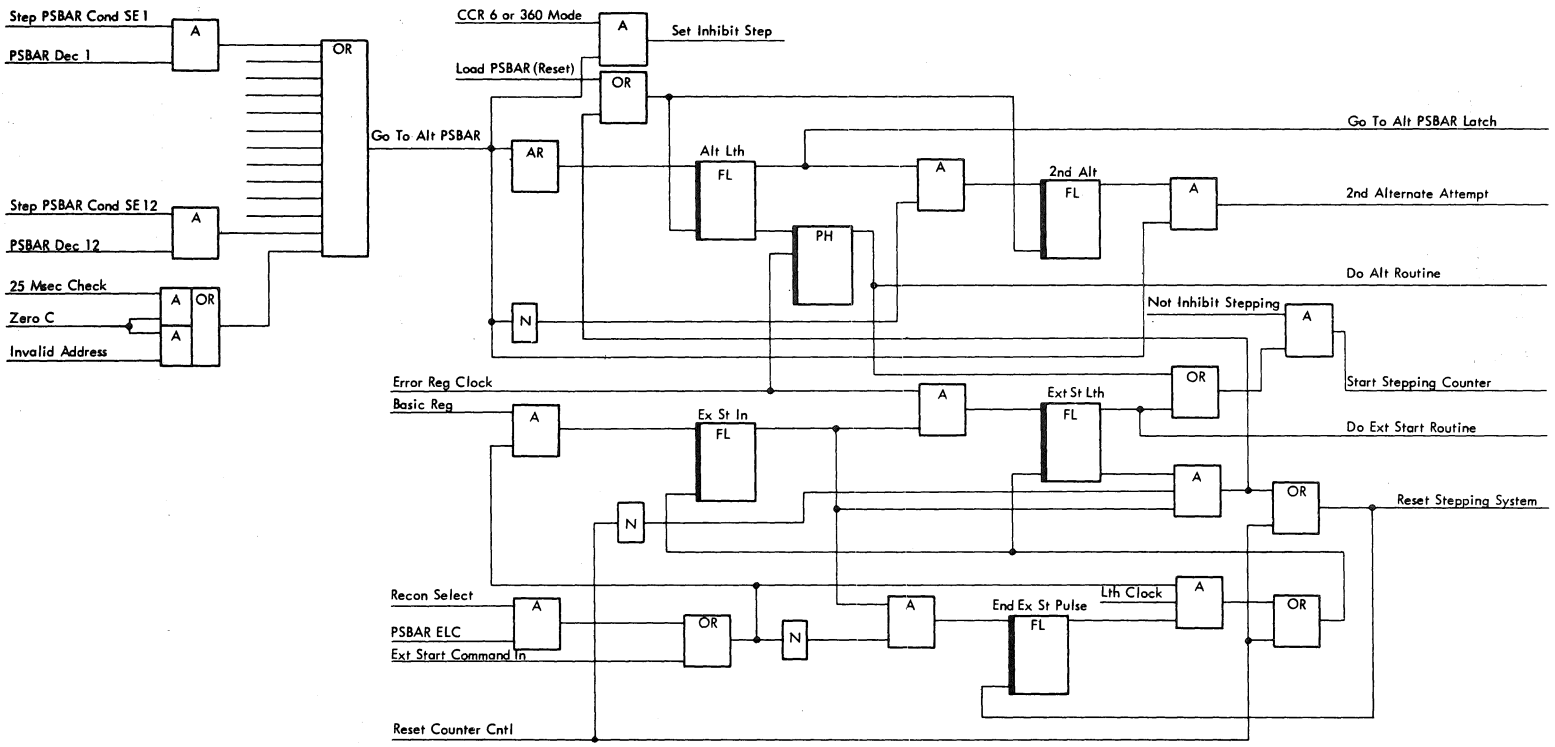


Figure 6-9. PSBAR Counter Controls.

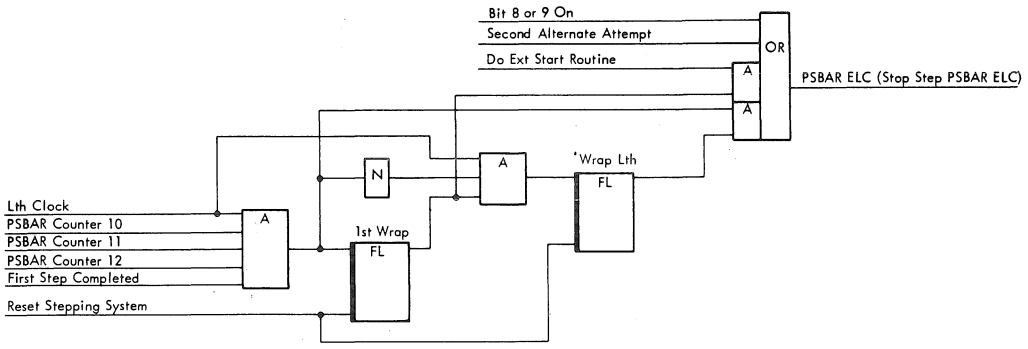


Figure 6-10. PSBAR Counter Controls.

The counter will be inhibited from further stepping once an alternate SE has been located unless the instruction load PSBAR is issued or an Ext Start is received.

C. Configuration Control

The 9020, with its various system elements, may be structured at will into many different configurations, with varying degrees of autonomy or interdependency. The equipment and techniques used to achieve the various configurations have been classified under the aggregate heading of configuration control.

The controlling mechanism for the 9020 will be the ATC Operational program. There is no preferred system structure in the 9020, i.e., the 9020 contains no inherent master - slave relationships which require that a specific computing element exercise primary control. Configuration Control does contain certain features which could, however, restrict the critical control functions to designated computing elements in order to obtain an orderly processing of the ATC task.

The use of the 9020 in the National Airspace System imposes certain fundamental requirements upon the system with regard to its ability to assume

various sub-system configurations. These requirements stem from the total nature of the ATC task, including both the critical operational work and the important, but necessarily subservient, support functions. These requirements may be briefly summarized as follows:

When units of the 9020 System are actively engaged in performing the ATC operational task, other units not so engaged, or malfunctioning units, must not be permitted to destructively interfere.

If units of 9020 are not required for the operational task, they should be available for subsidiary tasks or maintenance.

Those units of 9020 which are not actually malfunctioning or undergoing maintenance should be immediately available to EXC to perform the operational task, regardless of their current subsidiary tasks.

Units requiring maintenance must be provided with adequate maintenance facilities and effective isolation from the remainder of the operating system.

D. General Characteristics of Configuration Control

Configuration control establishes the instantaneous structure of the 9020 System by specifying to each major system element which other major system elements it may "listen" to at any given time. This "listening" on the part of a major system element is actually the reception of data and/or control information from other major system elements. To achieve the requisite flexibility, separate controllable paths for both types of information flow between elements are provided.

1. General Description of Element States

Each major system element of the 9020 can be in one of four states. These states are established by the ATC Operational program via configuration control. Element states are closely related to the immediate role of the element

in the overall ATC task. The following four sub-sections give a general description of each state. A more detailed analysis of each state is available from Fig. 6-11.

a. State Three

If a major system element is designated as being in State Three by the ATC Operational program, the element is presumed to be at its highest operational capability level. Normally, it is presumed that the ATC operational task would be run in this state. A CE in State Three has the ability to initiate reconfiguration of the existing system structure, subject to the information and control paths established by the ATC Operational program.

b. State Two

A major system element designated by the ATC Operational program as being in State Two is considered free of malfunctions and completely capable of performing the ATC operational task, except that a CE in this state cannot effect a system reconfiguration. While in State Two, a major system element might be employed in performing subsidiary processing tasks, but it is capable of being immediately recalled by ATC Operational program to assist other units in an operational task or to replace a malfunctioning unit. It is assumed that any subsidiary programs run while in State Two will be debugged and under tight monitor control. Preventive Maintenance programs of the "confidence routine" variety may also be effectively run in this state. If a computing element has been designated by ATC Operational program to be recallable, it will automatically interrupt its current tasks and go to State Three when certain check signals from other computing elements are received.

c. State One

State One may be considered to be a quasi-redundant state. When in State One, an element may be designated as recallable by ATC Operational program. However, certain operator manual controls will be enabled. These controls will

provide the necessary manual intervention to debug programs and run diagnostic programs. Thus, this state permits a non-malfunctioning unit to be used for various tasks which are not sufficiently predictable to be run in State Two with its tight monitor control, yet remain available to ATC Operational program for operational use. As in State Two, a CE in State One, when designated as recallable, will automatically terminate its current task and go to State Three upon receipt of certain check signals from other CEs.

d. State Zero

To accommodate the maintenance needs of the 9020, State Zero has been provided. The zero state is actually composed of two sub-states. The desired substate is selected by a switch which is enabled only in zero state, i.e., state field = 00.

With the Test switch off, the zero state is considered primarily useful for subsystem testing. All manual controls, except those governing the manual setting of CCRs, and those which turn off element power are enabled. An element may, however, be recalled by ATC Operational program if it has been designated as recallable. If so designated, a CE will go to State Three upon receipt of certain check signals from other computing elements. Effective subsystem isolation can be retained in this mode if desired. Care must be exercised when in the zero state with the Test switch off, due to the availability of all manual intervention capabilities of the system. It is assumed that a system performing the ATC task will protect itself, via configuration control, from spurious signals generated by a subsystem under test.

When an element's Test switch is "on" it is isolated from the remainder of the system to the extent required for its standalone or unit test operations to be used. In the case of PAM, TCU, and SE, this a blanket isolation, i.e., all system interfaces are closed. For the CE and IOCE, this isolation is primarily achieved by refusing to accept the SCON instruction. Complete isolation is not desirable for these elements. In this sub-state, all manual controls including power and manual CCR controls are active. To preclude

	State Bits		Issue SCON[1]	Accept SCON	CE ELC Maskable[5]	Element Controls[6]	Maint. Controls	Sys. Cons. Controls	Power & CCR Controls
	S_0	S_1							
Three	1	1	Yes	Yes[3]	Yes	No	No	Yes	No
Two	1	0	No[2]	Yes[3]	No	No	No	Yes	No
One	0	1	No[2]	Yes[3]	No	Yes	No	Yes	No
Zero Test Switch "OFF"	0	0	Yes	Yes[3]	No	Yes	No[8]	Yes	No
Zero Test Switch "ON"	0	0	Yes[7]	No[4]	Yes	Yes	Yes	No	Yes

Notes:

1. Where "Yes" is entered, it implies a legal or permissive ability to issue SCON. The issuing CE must have its own SCON bit set and meet all other SCON restrictions.
2. If a CE attempts SCON, a specification check interruption will result. No signals will issue to other elements.
3. Receiving element must have proper SCON bit set.
4. SCON's will be rejected regardless of CCR, except that a CE may accept SCON from itself if it has its own SCON bit set.
5. This column applies to receiving CE's. All incoming CE ELC's are masked by SCON bits in receiving CE's. Where "Yes" is entered, the ELC may also be masked by normal interruption mask controls. Where "No" is entered, no further masking is possible.
6. These include: IPL, Interrupt, Store, Display, Rate Switch, Address Compare.
7. When switch is "ON", SCON will not affect any external element. The issuing CE may accept SCON from itself. When the test switch is "ON", it will be possible for a CE to have its state bits changed manually. If the state bits are changed from 00 to 11, SCON may be exercised by the CE, but no element except the issuing CE will respond. If the state bits are changed to 10 or 01, Note 2 applies.
8. Maintenance controls are generally disabled except where other truth tables indicate exceptions.

Figure 6-11. Summary of State Definitions.

loss of switch control, the state bits of each element will be reset to 00 whenever the Test switch is turned off after having been in the "On" state. There is a technique that can be employed by an authorized maintenance man for putting into State Zero an element or unit that is hung-up in a higher state.

2. SCON Instruction

The Set Configuration (SCON) instruction is the program means by which the 9020 may be configured into the desired system configuration. SCON establishes the system configuration by specifying to the system elements: a) the state they are to assume, b) the CEs which can issue future SCON instructions to them, and c) the system elements they are to receive data from.

Since SCON is a vital part of configuration control, many tests, both hardware and program, are made to ascertain that it can legally be issued by a given CE and accepted by other system elements. Fig. 6-11 summarizes the conditions necessary for issuance and acceptance of SCON.

Two conditions imposed on the use of SCON are not given by Fig. 6-11. They are:

The SCON instruction can be issued by a CE only when it is in the supervisor state. If SCON is attempted in the problem state, a program interruption (privileged operation exception) will result.

It is prohibited to configure a system element so that it will not accept a SCON instruction from at least one CE. An automatic check will be made to prevent this and if detected will result in a program interruption (specification exception).

a. Configuration Control Register

Configuration control, in conjunction with the interface circuitry design, provides a protection facility for active system components from a malfunctioning system component. When one system component is not configured to communicate with another, circuit failures and/or spurious signal emissions from one component will not disrupt the operation of the other.

The configuration control register (CCR) is a physical register in each major system element. The CCR is set by SCON, and contains the information necessary to establish the state of the element to which it is attached, the CEs from whom it will accept future SCONs, and the other system elements to which it may "listen", or receive data from. The CCR will also indicate if a "Log-out Stop" of SE should take place for SE logout. Because of the various functions of the system elements, there are differences in the format of their respective CCRs. The CCR format for each system element is shown on Fig. 6-12. A position is assumed to be set when it contains a "1".

A CCR bit, when set, enables the interface from the associated unit. In some cases this may involve only the control lines, and in other cases may also involve data lines. In the use of all interfaces, some control action is required before any data bus is examined. If this control function is inhibited, it is unnecessary to further degate the data bus since it will not be examined. No signals to the DAR are gated by configuration control because it may be desirable to monitor the status of an element without being required to accept the communication from it. Also response signals to reconfiguration are not gated by the issuing CE's CCR since it is desirable to reconfigure elements without being required to accept other communications from them. The error detection circuitry of the system provides the protection from propagation of logic errors. The program may then use configuration control to isolate the malfunctioning unit for maintenance purposes. Each power supply contains an over-voltage, over-current sensor, which when activated will turn the power off in that unit before damage occurs. Configuration control provides degating from units with normal power status.

The circuitry which directly connects to a multiplexor interface has been designed so that the interface will not be disabled by commonly encountered component failures, unless, of course, the failure occurs in the primary element. The latter case is exemplified by a component failure in the drivers on the CE to (4) SE interface, while the former is exemplified by a component failure in an SE receiver in the same interface.

The circuitry which is directly connected to the I/O Interface, Channel to Device Control Unit, in the PAM, TCU and System Console has been designed so that power may be turned on and off in these units without disrupting any activity not concerning that unit in the interface. Also, in the interfaces in the 9020 System of the type exemplified by the one from a CE to four SEs, turning power on and off in an SE connected to that interface will not disrupt the functioning of that interface. However, in order to prevent turning power on and off in the CE from disrupting the activities of the SEs connected to that interface, the SEs must be configured not to accept communications from that CE.

b. Configuration Mask

The Configuration Mask (CM) is made available to SCON from a general purpose register. Its contents are loaded by SCON into the CCR of major system elements. The CM contains the necessary configuration control information appropriate to each element. The CM format is shown in Fig. 6-13. The CM format is sufficient to contain necessary configuration data for any type of element. For those elements which do not need all its contents, the necessary data is selectively sent.

c. Selection Mask

The Selection Mask (SM) shown in Fig. 6-13 is also made available to SCON from a general purpose register. The SM designates the elements to receive the data contained in the CM when SCON is issued. In effect, the SM is an address word for the CM. Multiple CCRs may be set with one SCON instruction, provided that identical masks are to be used in each receiving element.

A selected element will allow its CCR to be set by the incoming configuration mask if the sending CE's SCON bit is on in the selected element's CCR. A selected element will not be reconfigured by another CE if the selected element is in state zero with the test switch on.

Elements that accept the configuration mask respond by resetting their respective bit in the select register of the issuing CE. If the bit was on, resetting turns it off. The select register is then tested for zero and the condition code set as follows:

Condition Code 00 (Select Register zero) - All selected elements have accepted the configuration mask.

Condition Code 10 (Select Register not zero) - One or more of the selected elements failed to accept the configuration mask.

Condition Code 01 and 11 - Invalid

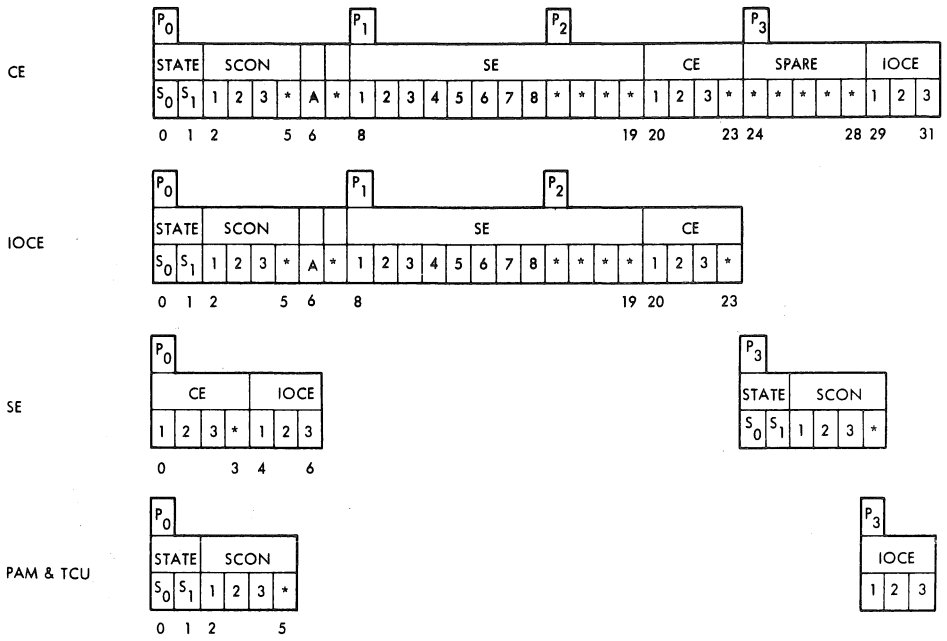
If the state bits of a CE in state zero with the test switch on are altered, the state will automatically be set to zero when the test switch is turned off.

A SCON field of all zeros is permissible in state zero to allow subsystem testing in complete isolation. The all zero SCON field must be set manually.

A select-for-reconfiguration received in a CE or IOCE processing an I/O instruction or interruption will stop processing of the instruction or interruption.

CEs and IOCEs will not reconfigure during a cycle involved with a main memory access. If such an access results in a hold signal from a memory, the access request condition will be reset if reconfiguration occurs.

As stated previously, a SCON field of zero is permissible in state zero. If, because of some error, a zero SCON field should occur in any other state, a "cheater" circuit will bypass normal SCON gating and make the SCON field



NOTES

1. * DENOTES SPARE BITS
2. 325 FLIGHT SYSTEM IS ASSUMED. FOR LESSER SYSTEMS, UNUSED BITS BECOME SPARES
3. BIT 7 AND 24-28 IN CE CONFIGURATION MASK ARE FORCED TO ZERO PRIOR TO MOVING CONFIGURATION MASK OUT OF THE CE
4. SE MASK IS POSITIONED AS SHOWN AND TRANSMITTED VIA THE STORAGE DATA BUS TO ACCOMMODATE THE SE'S CCR
5. PAM'S AND TCU'S RECEIVE ONLY THE INDICATED BITS
6. A IN BIT 6 DENOTES INHIBIT LOGOUT STOP

Figure 6-12. Configuration Control Register Format.

CONFIGURATION MASK

STATE		SCON						SE												CE								IOCE		
S_0	S_1	1	2	3	*	A	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	*	*	*	*	1	2	3
0	1	2			5	6		8											19	20			23	24			28	29		31

SELECTION MASK

PAM			TCU					SE												CE								IOCE		
1	2	3	1	2	3	*	*	1	2	3	4	5	6	7	8	*	*	*	*	1	2	3	*	*	*	*	*	1	2	3
0		2	3		5			8											19	20			23	24			28	29		31

NOTES:
1. * DENOTES SPARE BIT.
2. 325 FLIGHT SYSTEM IS ASSUMED. FOR LESSER SYSTEMS, UNUSED BITS BECOME SPARE BITS.
3. THE A IN BIT POSITION 6 DENOTES INHIBIT LOGOUT STOP.
4. BIT 7 AND 24-28 IN CONFIGURATION MASK ARE FORCED TO ZERO PRIOR TO MOVING CONFIGURATION MASK OUT OF CE.

Figure 6-13. Configuration Mask and Selection Mask Formats.

appear to be all ones. If the occurrence of all zeros in the SCON field results in a CCR parity error, an Element Check (ELC) will be issued.

An external, power on, or system reset will set all SCON field bits to one. A system initial program load (IPL) will set the selected CE's CCR according to the SE and IOCE select switches on the console. A simulated SCON instruction sets the CCR's in the selected elements according to the configuration selected. An element or subsystem reset will not alter the CCR of any element.

A CE's SCON field bits can be altered from the system console. The CE must be stopped. Microprogramming is used to load the CCR manually. The operation is similar to a normal SCON instruction, except that machine stat 0 is set prior to the SCON latch. This blocks the gating of selects for reconfigure to other elements. Stat 0 will also force a CE self-selected condition.

If CCR bit 6 is on, it will inhibit the issuance of a Logout Stop signal to an SE issuing a storage check. CCR bit 6 is set or reset according to the configuration mask used on a particular SCON instruction.

E. Program Status Word

The Program Status Word (PSW) contains detailed information on the status of the CE. The current PSW is divided between transistor register positions and a local storage location. PSW bits 0-19 are maintained in transistor registers, which perform the required functions by direct logic controls or by being accessible for microprogram branching. These positions are also buffered in local storage location 01 0111 since they do not have a read-out path except for scan-out). Positions 32-39 of the PSW are also held in transistor register positions, which may be set by logic or through the mover. These bits may be read out through the mover. Positions 40-63 of the PSW are held in the instruction address register. See 7201-01 Data Flow Diagram.

The type of interrupt determines the interruption code to be stored in positions 20-31 of the old PSW address. In the basic interruption sequence the

old PSW is assembled from the local storage buffer location, the interruption code, the transistor registers containing positions 32-39, and the instruction address register. Each of the two words of the PSW is stored as it is assembled. The storage protection key is set to zero in order to ensure successful storing.

By storing the PSW, the program can preserve the detailed status of the CE for later use. By loading a new PSW or part of a PSW, the state of the CE may be changed.

All or part of a PSW may be stored or loaded. The entire PSW is stored and a new PSW is introduced when the CE is interrupted. The rightmost 32 bits are stored in Branch and Link. The Load PSW instruction introduces a new PSW. Set Program Mask introduces a new condition code and program mask in the PSW. Set System Mask introduces a new system mask. See Fig. 6-14 for the PSW format.

The following is a summary of the purposes of the PSW fields:

System Mask: Bits 0-7 and 16-19 of the PSW are associated with I/O Channels and external signals as specified in the following table. When a mask bit is 1, the source can interrupt the CE. When the bit is 0, the corresponding source cannot interrupt the CE and the interruption remains pending.

System Mask Bit	Interruption Source
0	Multiplexor Channel A
1	Selector Channel 1A
2	Selector Channel 2A
3	Selector Channel 3A
4	Multiplexor Channel B
5	Selector Channel 1B
6	Selector Channel 2B
7	Timer; Interrupt Switch; External Signal
16	Selector Channel 3B
17	Multiplexor Channel C
18	Selector Channel 1C
19	Selector Channel 2C

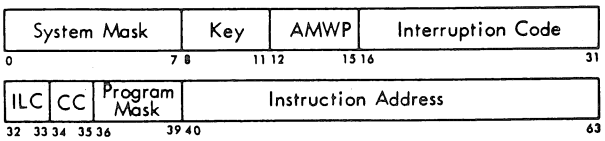


Figure 6-14. Program Status Word Format.

Protection Key: Bits 8-11 of the PSW form the CE protection key. The key is matched with the four high-order bits of a storage key whenever data are to be stored, or whenever data are to be fetched and the fetch-protection bit in the storage key is 1.

AMWP: These letters represent bits 12-15 of the PSW.

A (bit 12) represents ASCII. When a bit 12 of the PSW is 1, the codes for the extended ASCII format are generated for decimal results. When PSW bit 12 is 0, the codes for the extended binary-coded-decimal format are generated.

M (bit 13) represents machine-check mask. When PSW bit 13 is 1, the machine-check interruption, element check (ELC) out signal and diagnostic logout occur upon malfunction detection. When PSW bit 13 is 0, the CE is masked for machine-check interruptions. The interruption and logout do not occur. An ELC out signal is issued as before and the interruption remains pending.

W (bit 14) represents the wait state. When bit 14 of the PSW is 1, the CE is in the wait state. When PSW bit 14 is 0, the CE is in the running state.

P (bit 15) represents the problem state. When PSW bit 15 is 1, the CE is in the problem state. When PSW bit 15 is 0, the CE is in the supervisor state.

Interruption Code: Bits 20-31 of the PSW identify the cause of an I/O, program, supervisor call, external or machine-check interrupt. Use of the code for all five interruption types may be found in Table 6-1.

Instruction Length Code (ILC): The code in PSW bits 32 and 33 indicates the length in halfwords of the last interpreted instruction when a program or supervisor-call interruption occurs. The code is unpredictable for I/O, external or machine-check interruptions. See Fig. 6-15.

Instruction Length Code	PSW Bits 32-33	Instruction Bits 0-1	Instruction Length	Instruction Format
0	0 0		Not Available	
1	0 1	0 0	One Halfword	RR
2	1 0	0 1	Two Halfwords	RX
2	1 0	1 0	Two Halfwords	RS or SI
3	1 1	1 1	Three Halfwords	SS

Figure 6-15. Instruction Length Recording.

Condition Code (CC): PSW bits 34 and 35 represent the condition code. The condition codes for all instructions may be found in Fig. 6-15.

Program Mask: PSW bits 36-39 represent the program mask bits. Each bit is associated with a program exception. When the mask bit is 1, the exception is allowed. (See Fig. 6-16.)

Program Mask Bit	Program Exception
36	Fixed-Point Overflow
37	Decimal Overflow
38	Equipment Underflow
39	Significance

Figure 6-16. Program Mask Assignment.

Instruction Address: Bits 40-63 of the PSW are the instruction address. This address specifies the leftmost 8-bit byte position of the next instruction and is in the instruction address register.

A set of operations is provided to switch the status of the computing element (CE), of storage, and of communication between elements of the system.

The over-all CE status is determined by several program-state alternatives, each of which can be changed independently to its opposite and most of which are indicated by a bit in the program status word (PSW). The CE status is further defined by the instruction address, the condition code, the instruction-length code, the storage-protection key, and the interruption code. These all occupy fields in the PSW.

Storage is protected by means of storage keys, which are matched with a protection key in the PSW or in a channel. The protection status of storage may be changed by introducing new storage keys, using SET STORAGE KEY. The storage keys may be inspected by using INSERT STORAGE KEY.

F. PSW Control and Program States

The four types of program-state alternatives, which determine the over-all computing element status, are named Problem/Supervisor, Wait/Running, Masked/Interruptable, and Stopped/Operating. These states differ in the way they affect the CE functions, and in the way their status is indicated and switched. Each state has one alternative, except Masked, which has many.

All program states are independent of each other in their function, indication, and status-switching. Status-switching does not affect the contents of the arithmetic registers or the execution of I/O operations, but may affect the timer operation.

1. Problem State

The choice between supervisor and problem state determines whether or not the full set of instructions is valid. The names of these states reflect their normal use.

In the problem state all I/O, protection, and direct-control instructions are invalid, as well as LOAD PS BASE, STORE PS BASE, SET ADDRESS TRANSLATOR, SET CONFIGURATION, LOAD PSW, SET SYSTEM MASK, and DIAGNOSE. These are called privileged instructions. A privileged instruction encountered in the problem state, constitutes a privileged-operation exception and causes a program interruption. In the supervisor state all instructions are valid.

When bit 15 of the PSW is zero, the CE is in the supervisor state. When bit 15 is one, the CE is in the problem state. The supervisor state is not indicated on the operator sections of the CE control panel.

The CE is switched between problem and supervisor state by changing bit 15 of the PSW. This bit can be changed only by introducing a new PSW. Thus status-switching may be performed by LOAD PSW, using a new PSW with the desired value for bit 15. Since LOAD PSW is a privileged instruction, the CE must be in the supervisor state prior to the switch. A new PSW is also introduced when the CE is interrupted. The SUPERVISOR CALL causes an interruption and thus may change the CE state. Similarly, initial program loading introduces a new PSW and with it a new CE state. The new PSW may introduce the problem or supervisor state regardless of the preceding state. No explicit operator control is provided for changing the supervisor state.

Timer updating is not affected by the choice between supervisor and problem state.

To allow return from an interruption-handling routine to a preceding program by a LOAD PSW, the PSW for the interruption routine should specify the supervisor state.

After the review of the actual PSW it will be advantageous to summarize its control characteristics of the CE in any operation. For instance, look at the PSW bit 12-15 which control the status of the computing element. Suppose that bit 15 is set to a one, the computing element as a result of this setting is in the problem state. In this state the computing element cannot execute

the privileged instructions such as SCON, I/O Op, etc. Therefore, if one were executing a program in this state, he would have to perform a PSW swap in order to change the status of the computing element to the supervisory state by installing a new PSW with bit 15 set to a zero and thereby allow the execution of a privileged instruction. In such a case the PSW swap could be forced by the programmer via his program.

One might ask the question why not leave the computing element in the supervisory state where the total instruction set can be executed? There are probably as many answers to this question as there are programmers, but basically the answer can be formed by observing a few facts related to system operation. When executing a program in the problem state, that particular program cannot interfere with the system concurrent operations or configuration. Because of this the programmer is free from the responsibility of providing interrupt handling for the interrupt scheme. Thus one supervisory program can be written to handle all configuration, monitoring, interrupt handling, and I/O operations. This one supervisory program can be used in conjunction with all the programs one compiled in the problem state. Several of these supervisory programs are already in existence such as the NOSS monitor. If such a scheme were not used each individual program would have to handle all such monitoring, interrupt handling, and configuration. This would result in compiling many error and interrupt handling routines along with the problem program. If such routines are not provided the computer operator has no indication as to whether the program is still being executed or hung up on a particular instruction, thereby causing ineffecient use of computer time waiting for some type of response.

2. Wait State

In the wait state no instructions are processed and storage is not addressed repeatedly for this purpose, whereas in the running state, instruction fetching and execution proceed in the normal manner.

When bit 14 of the PSW is one, the CE is waiting. When bit 14 is zero, the CE is in the running state. The wait state is indicated on the operator control section of the CE control panel by the wait light.

The CE is switched between wait and running state by changing bit 14 of the PSW. This bit can be changed only by introducing an entire new PSW, as is the case with the problem-state bit. Thus, switching from the running state may be achieved by the privileged instruction LOAD PSW, or by an interruption such as for SUPERVISOR CALL, or by initial program loading. Switching from the wait state may be achieved by an I/O or external interruption or, again, by initial program loading. The new PSW may introduce the wait or running state regardless of the preceding state. No explicit operator control is provided for changing the wait state.

Timer updating is not affected by the choice between running and wait state.

One might ask, for what purpose does the wait bit exist? This might be answered in general by showing an application. Suppose that one is executing a program in the supervisory state but does not have any error or interrupt routines incorporated, one could set the wait bit on for all the error or interrupt PSWs. When an interrupt occurred in which no routine was provided such a PSW swap would force the computing element to the wait state, thereby notifying the operator by a control panel indicator that something occurred during the execution of the program which was not expected. If it were otherwise, the operator would have no indication that the program was not being executed. Another example of the use of the wait state, is where the programmer desires to go to the wait state after the issuance of a start I/O and wait until said I/O operation is completed. This is possible because if one will recall, the computing element is capable of handling the interrupts in the wait state.

To leave the wait state without manual intervention, the CE should remain interruptable for some active I/O or external interruption source.

3. Stopped State MANUAL LIGHT ON

When the CE is in the stopped state, instructions and interruptions are not executed. In the operating state the CE executes instructions (if not waiting) and interruptions (if not masked off).

The stopped state is indicated on the operator control section of the CE control panel by the manual light. The stopped state is not identified by a bit in the PSW. A change in the stopped or operating state can be effected only by manual intervention or by machine malfunction. No instructions or interruptions can stop or start the CE. (Except WRITE DIRECT - STOP CE & START CE) The CE is commanded to stop when the stop switch on the operator section of the CE control panel (System Console) is pressed, when an address comparison indicates equality and the address-compare switches are set to STOP, and when the rate switch is set to INSTRUCTION STEP. In addition the CE is placed in the stopped state after power is turned on. The CE is placed in the operating state when the start switch on the operator panel is pressed. The CE is also placed in the operating state when initial program loading is commenced. (or WRITE DIRECT INTERRUPTION)

The transition from operating to stopped state occurs at the end of instruction execution, prior to starting the next instruction execution. When the CE is in the wait state the transition takes place immediately. All interruptions pending and not masked off, are taken while the CE is still in the operating state. They cause an old PSW to be stored and a new PSW to be fetched before entering the stopped state. Once the CE is in the stopped state, interruptions are no longer taken, but remain pending.

The timer is not updated in the stopped state.

Except for timing considerations, execution of a program is not affected by stopping the CE.

When the CE is unable to end an instruction because of machine malfunction, the stop switch is not effective. An initial program loading reset or CE-reset should be used to terminate the operation.

Input/output operations continue to completion while the CE is in the problem wait, masked, or stopped state. However, no new I/O operations can be initiated while the CE is stopped, waiting, or in the problem state. Also, the interruption caused by I/O completion remains pending when masked off, or when the CE is in the stopped state.

4. Masked States

The CE may be masked or interruptable for all system and machine-check interruptions, and for some program interruptions. When the CE is interruptable for a class of interruptions, these interruptions are accepted. When the CE is masked, the program interruptions are ignored, and system and machine-check interruptions remaind pending.

The system mask bits (PSW bits 0-7 and 16-19), the program mask bits (PSW bits 36-39), and the machine-check mask bit (PSW bit 13), indicate as a group the masked state of the CE. When a mask bit is one, the CE is interruptable for the corresponding interruptions. With the exception of certain CE element check conditions, when the mask bit is zero, these interruptions are always masked off. The system mask bits indicate the masked state of the CE for the multiplexor channels, the selector channels, and the external signals. The program mask bits indicate the masked state for four of the program exceptions. The machine-check mask bit pertains to all machine checks. Those program interruptions not maskable, as well as the supervisor-call interruption, are always taken.

The masked states are not indicated on the operator sections of the CE control panel.

Most mask bits do not affect the execution of CE operations. The only exception is the significance mask bit, which determines the manner in which a floating-point operation is completed when a significance exception occurs.

The interruptable state of the CE is switched by changing the mask bits in the PSW. The program mask may be changed separately by SET PROGRAM MASK, and the system mask may be changed separately by the privileged instruction SET SYSTEM MASK. The machine-check mask bit can be changed only by introducing an entire new PSW, as is the case with the problem-state and wait-state bits. Thus a change in the entire masked status may be achieved by the privileged instruction LOAD PSW, or by an interruption such as for SUPERVISOR CALL, or by initial program loading. The new PSW may introduce a new masked state regardless of the preceding state. No explicit operator control is provided for changing the masked state.

Timer updating is not affected by the choice between masked or interruptable states.

To prevent an interruption-handling routine from being interrupted before necessary housekeeping steps are performed, the new PSW for that interruption should mask the CE for further interruptions of the kind that caused the interruption.

The interruption system permits the computing element (CE) to change its state as a result of conditions arising outside the system, in input/output (I/O), or in the CE itself. The five classes of these conditions are input/output, program, supervisor-call, external, and machine-check interruptions.

a. Interruption Action

An interruption consists of storing the current PSW as an <u>old</u> PSW and fetching a <u>new</u> PSW.

Processing resumes in the state indicated by the new PSW. The old PSW contains the address of the instruction which would have been executed next if an interruption had not occurred and the instruction-length code of the last-interpreted instruction.

Interruptions are taken only when the CE is interruptable for the interruption source. Input/output and external interruptions may be masked by the system mask, four of the program interruptions may be masked by the program mask, and the machine-check interruptions may be masked by the machine-check mask.

With the exception of DELAY, an interruption always takes place after one instruction interpretation is finished and before a new instruction interpretation is started. However, the occurrence of an interruption may affect the execution of the current instruction. To permit proper programmed action following an interruption, the cause of the interruption is identified and provision is made to locate the last-interpreted instruction.

When the CE is commanded to stop, the current instruction is finished and all interruptions which are pending or become pending before the end of the instruction, and which are not masked, are taken.

The details of instruction execution, source identification, and location determination are explained in the following sections, and are summarized in Table 6-1.

A pending interruption will be taken even if the CE becomes interruptable during only one instruction.

b. Instruction Execution

With the exception of DELAY, an interruption occurs when the preceding instruction is finished and the next instruction is not yet started. The manner in which the preceding instruction is finished may be influenced by the cause of the interruption. The instruction is said to have been completed, terminated or suppressed.

In the case of instruction completion, results are stored and the condition code is set as for normal instruction operation, although the result may be influenced by the exception which has occurred.

In the case of instruction termination, all, part, or none of the result may be stored. Therefore, the result data are unpredictable. The setting of the condition code, if called for, may also be unpredictable. In general, the results should not be used for further computation.

In the case of instruction suppression the execution proceeds as if no operation were specified. Results are not stored and the condition code is not changed.

c. Source Identification

The five classes of interruptions are distinguished by the storage locations in which the old PSW is stored and from which the new PSW is fetched. These storage locations are in the preferential-storage area. The detailed causes are further distinguished by the interruption code of the old PSW. The bits of the interruption code are numbered 20-31, corresponding to their position in the PSW.

For I/O interruptions additional information is provided by the contents of the channel status word, stored as part of the I/O interruption.

For machine-check interruptions, additional information is provided by the diagnostic procedure which is part of the interruption.

Interruption PSWs are assigned to an area of storage called the preferential-storage area. The location of the preferential-storage area is determined by a base address in each CE, thus, allowing different areas to be assigned for each CE. All addresses generated automatically by the CE are constructed using the current value of the preferential-storage base address.

The following table lists the main-storage locations in the preferential-storage area. The addresses shown are relative to the preferential-storage base address.

ADDRESS		LENGTH	PURPOSE
0	0000 0000	Double Word	Initial Program Loading PSW
8	0000 1000	Double Word	Initial Program Loading CCW1
16	0001 0000	Double Word	Initial Program Loading CCW2
24	0001 1000	Double Word	External Old PSW
32	0010 0000	Double Word	Supervisor Call Old PSW
40	0010 1000	Double Word	Program Old PSW
48	0011 0000	Double Word	Machine Old PSW
56	0011 1000	Double Word	Input/Output Old PSW
64	0100 0000	Double Word	Channel Status Word
72	0100 1000	Word	Channel Address Word
76	0100 1100	Word	Unused
80	0101 0000	Word	Timer
84	0101 0100	Word	Unused
88	0101 1000	Double Word	External New PSW
96	0110 0000	Double Word	Supervisor Call New PSW
104	0110 1000	Double Word	Program New PSW
112	0111 0000	Double Word	Machine New PSW
120	0111 1000	Double Word	Input/Output New PSW
128	1000 0000		Diagnostic Logout Area*

*The diagnostic logout area extends through byte location 511.

Whenever a CE fails to gain access to the storage element (SE) containing its preferential-storage area (PSA), and provided the inhibit logout-stop bit is set off in its CCR, hardware automatically develops a new preferential-storage base address which references its alternate PSA.

If the access is attempted because of an instruction fetch (including SUPERVISOR CALL), an operand fetch, or an interval timer update, an addressing exception is recognized and a program interruption is taken using the alternate PSA. If the access if attempted in order to take a program interruption, input/output interruption, external interruption, or a supervisor-call interruption, the original interruption request is preserved and is taken using the alternate PSA.

Whenever a CE fails to gain access to the SE containing its alternate PSA, an element check (CE-ELC) is issued and the CE performs a check stop.

No indication of the change in the preferential-storage base address from the primary PSA to the alternate PSA is made by the hardware. The programmer may take cognizance of such a change in the interruption routines entered via the alternate PSA.

d. Location Determination

For some interruptions it is desirable to locate the instruction being interpreted when the interruption occurred. Since the instruction address in the old PSW designates the instruction to be executed next, it is necessary to know the length of the preceding instruction. This length is recorded in bit positions 32 and 33 of the PSW as the instruction-length code.

The instruction-length code is predictable only for program and supervisor-call interruptions. For I/O and external interruptions the interruption is not caused by the last-interpreted instruction, and the code is not predictable for these instructions. For machine-check interruptions the setting of the code may be affected by the malfunction and therefore is unpredictable.

For the supervisor-call interruption the instruction-length code is 1, indicating the halfword length of SUPERVISOR CALL. For program interruptions the codes 1, 2, and 3 indicate the instruction length in halfwords. The code 0 is reserved for those program interruptions where the length of the instruction is not available because of certain overlapping conditions in instruction fetching. In code 0 cases the instruction address in the old PSW does not represent the next instruction address. Instruction-length code 0 can occur for a program interruption only when caused by a protected or an unavailable data address. The states of the instruction-length code are shown in the following table.

Instruction Length Code	PSW Bits 32-33	Instruction Bits 0-1	Instruction Length	Instruction Format
0	00		Not Available	
1	01	00	One Halfword	RR
2	10	01	Two Halfwords	RX
2	10	10	Two Halfwords	RS or SI
3	11	11	Three Halfwords	SS

When a program interruption is due to an incorrect branch address, the location determined from the instruction address and instruction-length code is the branch address and not the location of the branch instruction.

When an interruption occurs while the CE is in the wait state, the instruction-length code is always unpredictable.

The instruction EXECUTE represents upon interruption an instruction-length code which does not reflect the length of the instruction executed, but is 2, the length of EXECUTE.

e. Input/Output Interruption

The I/O interruption provides a means by which the CE responds to signals from I/O devices.

A request for an I/O interruption may occur at any time, and more than one request may occur at the same time. The requests are preserved in the IOCE until accepted by the CE. Priority is established among requests so that only one interruption request is processed at a time.

An I/O interruption can occur only after execution of the current instruction is completed, and while the CE is interruptable for the channel presenting the request. Channels are masked by system mask bits 0-6, and 16-19. Interruptions masked off remain pending.

The I/O interruption causes the old PSW to be stored at location 56 in the preferential-storage area and causes the channel status word associated with the interruption to be stored at location 64. Subsequently a new PSW is loaded from location 120.

The interruption code in the old PSW identifies the channel and device causing the interruption in bits 20-23 and 24-31 respectively. The instruction-length code is unpredictable.

Whenever the status bits of the channel status word (CSW) associated with the interruption indicate that the storing of the CSW was due to a channel control check, or an interface control check, additional information is provided by a diagnostic logout into the preferential-storage area. To prevent the contents of the logout area from being destroyed by an immediately following logout, all channels of the selected IOCE must be masked until the logout information has been acted upon or stored elsewhere for later use.

f. Program Interruption

Exceptions resulting from improper specification or use of instructions and data, or from conditions preventing an IOCE from accessing the preferential storage area, cause a program interruption.

The current instruction is completed, terminated, or suppressed. Only one program interruption occurs for a given instruction and is identified in the old PSW. The occurrence of a program interruption does not preclude the simultaneous occurrence of other program-interruption causes. Which of several causes is identified may vary from one occasion to the next.

A program interruption can occur only when the corresponding mask bit, if any, is one. When the mask bit is zero the interruption is ignored. Program interruptions do not remain pending. Program mask bits 36-39 permit masking of four of the interruption causes.

The program interruption causes the old PSW to be stored at location 40 in the preferential-storage area and a new PSW to be fetched from location 104.

The cause of the interruption is identified by interruption-code bits 24-31. The remainder of the interruption code, bits 20-23 of the PSW, is made zero. The instruction-length code indicates the length of the preceding instruction in halfwords. For a few cases the instruction length is not available. These cases are indicated by code 0.

A description of the individual program exceptions follows. The application of these rules to each class of instructions is further described in the applicable sections. Some of the exceptions listed may also occur in operations executed by I/O channels. In that event, the exception is indicated in the channel status word stored with the I/O interruption.

(1) Operation Exception

When an operation code is not assigned, an operation exception is recognized. The operation is suppressed.

The instruction-length code is 1, 2, or 3.

(2) Privileged-Operation Exception

When a privileged instruction is encountered in the problem state, a privileged-operation exceptionis recognized. The operation is suppressed.

The instruction-length is 1 or 2.

(3) Execute Exception

When the subject instruction of EXECUTE is another EXECUTE, an execute exception is recognized. The operation is suppressed.

The instruction-length code is 2.

(4) Protection Exception

When the storage key of an accessed location does not match the protection key in the PSW, a protection exception is recognized.

The operation is suppressed on a store-protection violation, except in the case of STORE MULTIPLE, READ DIRECT, and variable-length operations, which are terminated. The operation is always terminated on a fetch-protection violation.

The instruction-length code is 0, 2, or 3.

(5) Addressing Exception

When an address specifies any part of data, instruction, or control word outside the available storage for the particular installation, or outside the configured storage, or storage assigned by the storage address translator for a particular CE or IOCE, an addressing exception is recognized.

The operation is terminated for an invalid data address. Data in storage remain unchanged, except when designated by valid addresses. The operation is suppressed for an invalid instruction address. The instruction-length code normally is 1, 2, or 3; but may be 0 in the case of a data address.

(6) Specification Exception

A specification exception is recognized when:

A data, instruction, or control-word address does not specify an integral boundary for the unit of information.

The R_1 field of an instruction specifies an odd register address for a pair of general registers which contain a 64-bit operand.

A floating-point register address other than 0, 2, 4, or 6 is specified.

The multiplier or divisor in decimal arithmetic exceeds 15 digits and sign.

The first operand field is shorter than or equal to the second operand field in decimal multiplication or division.

The block address specified in SET STORAGE KEY or INSERT STORAGE KEY has the four low-order bits not all zero.

SET CONFIGURATION is attempted by a CE whose own scon bit is off in its configuration control register; or whose state bits are either set to One or Two. A configuration mask has its scon-field bits all zeros, or all referencing CEs not available to the particular installation. A selection mask has an IOCE selection bit set when two or more CE communication bits are set in the configuration mask.

The operand address of LOAD PREFERENTIAL-STORAGE BASE ADDRESS, or STORE PREFERENTIAL-STORAGE BASE ADDRESS does not have the two low-order bits both zero. Bit positions 8-19 of the operand addressed by LOAD PREFERENTIAL-STORAGE BASE ADDRESS, interpreted as the 12 high-order bits of a storage address, do not specify a location within a storage element configured to communicate with the CE executing this instruction, or do not specify a location within the first block of 131,072 bytes in an LCS element.

WRITE DIRECT does not select an element; or selects more than one element. READ DIRECT does not select a computing element; or selects more than one computing element.

DIAGNOSE is not located in main storage on an integral boundary for a fullword; it specifies an operation whose execution is not permitted for a CE in state Three, Two, or One.

Execution of SET ADDRESS TRANSLATOR is attempted by a CE whose own scon bit is off in its configuration control register; or assignment mask references a particular storage module more than once, or references a storage module not available to a particular installation, or assigns a LCS module to other than positions 10, 11, or 12.

The operation is suppressed. The instruction-length code is 1, 2, or 3.

(7) Data Exception

A data exception is recognized when:

The sign or digit codes of operands in decimal arithmetic or editing operations, or in CONVERT TO BINARY are incorrect.

Fields in decimal arithmetic overlap incorrectly.

The decimal multiplicand has too many high-order significant digits.

The operation is terminated. The instruction-length code is 2 or 3.

(8) Fixed-Point-Overflow Exception

When a high-order carry occurs or high-order significant bits are lost in fixed-point add, subtract, shift, or sign-control operations, a fixed-point-overflow exception is recognized.

The operation is completed by ignoring the information placed outside the register. The interruption may be masked by PSW bit 36.

The instruction-length code is 1 or 2.

(9) Fixed-Point-Divide Exception

A fixed-point-divide exception is recognized when a quotient exceeds the register size in fixed-point division, including division by zero.

The result of CONVERT TO BINARY exceeds 31 bits.

Division is suppressed. Conversion is completed by ignoring the information placed outside the register.

The instruction-length code is 1 or 2.

(10) Decimal-Overflow Exception

When the destination field is too small to contain the result field in a decimal operation, a decimal-overflow exception is recognized.

The operation is completed by ignoring the overflow information. The interruption may be masked by PSW bit 37.

The instruction-length code is 3.

(11) Decimal-Divide Exception

When a quotient exceeds the specified data field size, a decimal-divide exception is recognized. The operation is suppressed.

The instruction-length code is 3.

(12) Exponent-Overflow Exception

When the result characteristic exceeds 127 in floating-point addition, subtraction, multiplication, or division, an exponent-overflow exception is recognized. The operation is terminated.

The instruction-length code is 1 or 2.

(13) Exponent-Underflow Exception

When the result characteristic is less than zero in floating-point addition, subtraction, multiplication, or division, an exponent-underflow exception is recognized.

The operation is completed by making the result a true zero. The interruption may be masked by PSW bit 38.

The instruction-length code is 1 or 2.

(14) Significance Exception

When the result of a floating-point addition or subtraction has an all-zero fraction, a significance exception is recognized.

The operation is completed. The interruption may be masked by PSW bit 39. The manner in which the operation is completed is determined by the mask bit.

The instruction-length code is 1 or 2.

(15) Floating-Point-Divide Exception

When division by a floating-point number with zero fraction is attempted, a floating-point divide exception is recognized. The operation is suppressed.

The instruction-length code is 1 or 2.

(16) Preferential-Storage Area Lockout Exception

When an IOCE fails to gain access to the preferential storage area on a CAW fetch, on an I/O interruption, on a CSW store pertaining to an I/O instruction, or on a store during a logout operation, a preferential storage area lockout exception is recognized.

If the CE is executing an I/O instruction, or if a request for an I/O interruption has been accepted, the current operation is terminated.

The instruction-length code is unpredictable.

For other than the preceding, the instruction operation is completed.

The instruction-length code is 1, 2, or 3.

(17) SE Stopped Exception

When a CE attempts to gain access to a storage element which is in logout-stop status, a SE stopped exception is recognized.

The operation is suppressed on an instruction fetch, and terminated on a data access.

The instruction-length code is 1, 2, or 3.

g. Supervisor-Call Interruption

The supervisor-call interruption occurs as a result of the execution of SUPERVISOR-CALL.

The supervisor-call interruption causes the old PSW to be stored at location 32 in the preferential-storage area and a new PSW to be fetched from location 96.

The contents of bit positions 8-15 of the SUPERVISOR CALL become bits 24-31 in the interruption code of the old PSW. Bits 20-23 of the interruption code are made zero. The instruction-length code is 1, indicating the halfword length of SUPERVISOR CALL.

The name "supervisor call" indicates that one of the major purposes of the interruption is the switching from problem to supervisor state. This major purpose does not preclude the use of this interruption for other types of status-switching.

The interruption code may be used to convey a message from the calling program to the supervisor.

When SUPERVISOR CALL is performed as the subject instruction of EXECUTE, the instruction-length code is 2.

h. External Interruption

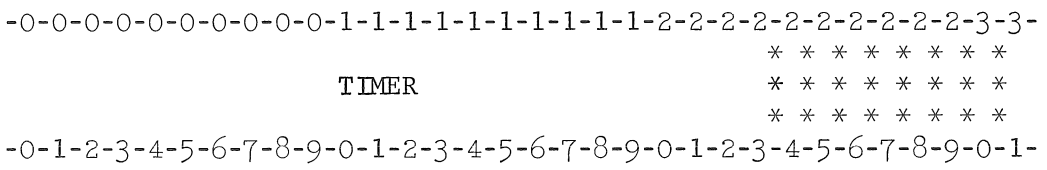
The external interruption provides a means by which the CE responds to signals from the timer, from the interrupt switch, from external units, and in certain circumstances from itself.

A request for an external interruption may occur at any time, and requests from different sources may occur at the same time. Requests are preserved until honored by the CE. All pending requests are presented simultaneously when an external interruption occurs. With the exception of abnormal condition requests which are preserved in the Diagnose Accessible Register (DAR) until removed by a diagnostic operation, each request is presented only once. When several requests from one source are made before the interruption is taken, only one interruption occurs.

With the exception of a request for a CE element check (ELC) presented to a CE in state Zero (with test switch off), One, or Two, an external interruption can occur only when system mask bit 7 is one and after the execution of the current instruction is completed (with the exception of DELAY which is terminated). The interruption causes the old PSW to be stored at location 24 in the preferential-storage area and a new PSW to be fetched from location 88. The source of the interruption is identified by interruption-code bits 20-31. The source of interruption-code bit 31 is further identified by the contents of the Diagnose Accessible Register. The instruction-length code is unpredictable for external interruptions.

(1) Timer

A timer value changing from positive to negative causes an external interruption with bit 24 of the interruption code turned on.



The timer occupies a 32-bit word at storage location 80 in the preferential-storage area. The contents of the timer are reduced by a one in bit position 21 and in bit position 23 every 1/60th of a second, as determined by the line frequency. The gross result is equivalent to reducing the timer by one in bit position 23 every 1/300th of a second. The full cycle time is 15.5 hours.

The count is treated as a signed integer by following the rules for fixed-point arithmetic. The negative overflow, occurring as the timer is counted from a large negative number to a large positive number, is ignored. The interruption is initiated as the count proceeds from a positive number, including zero, to a negative number.

The timer is updated whenever access to storage permits. An updated timer value is normally available at the end of each instruction execution; thus a real-time count can be maintained. Timer updating may be omitted when I/O data transmission approaches the limit of storage capability.

The timer may have been updated several times after an interruption is initiated, before the CE is actually interrupted, depending upon instruction execution time. The timer remains unchanged when the CE is in the stopped state, or when the rate switch on the operator intervention panel is set to INSTRUCTION STEP. The timer value may be changed at any time by storing a new value in storage location 80 in the preferential-storage area.

The timer in association with a program can serve both as a real-time clock and as an interval timer.

The timer is not updated whenever the CE is in state Zero, with the Disable Interval Timer switch on.

(2) Interrupt Switch

Pressing the interrupt switch on the operator control section of the CE control panel causes an external interruption with bit 25 of the interruption code turned on, provided the CE is in state Zero, or state One; or provided the CE is in state Two or Three with the CE control panel interlock switch on.

Pressing the interrupt switch on the System Console also causes an external interruption with bit 25 of the interruption code turned on, provided that the CE is selected by the CE Select switch and the CE is not in state Zero with the test switch on, and the System Console Interlock switch is on.

(3) External Signal

An external signal causes an external interruption, with the corresponding bit in the interruption code turned on.

The pattern presented in interruption-code bits 20-31 depends upon the pattern received before the interruption is taken. Two categories of external signals are recognized: those due to execution of the Direct Control instructions, and those due to detection of Abnormal Conditions.

(4) Direct Control Signals

Pairs of direct-control signal-out lines, originating in each CE, are connected into corresponding pairs of signal-in lines in each of up to three other CEs. The signal-in lines are designed CE(x) Write Direct and CE(x) Read Direct, where "x" identifies the source of the signal. An interconnection of this kind allows one CE to interrupt another by executing the direct control instructions READ DIRECT and WRITE DIRECT. A similar interconnection of the direct-out lines of one CE to the direct-in lines of other CEs, and vice versa, provides an eight-bit data path (plus parity) for moving information between CEs.

A direct control interruption can occur only while the CE is interruptable for the CE presenting the request. Interruptions will be taken, provided PSW mask bit 7 is one, and the communications bit for the requesting CE is set on in the configuration control register of the receiving CE.

(5) Abnormal Condition Signals

The abnormal condition interruption provides a means by which the CE responds to certain hardware generated signals from a CE, IOCE, SE, TCU, or PAM. In certain circumstances, a CE also responds to signals from itself. Three categories of abnormal condition signals are recognized: element check (ELC), out-of-tolerance check (OTC), and on-battery-signal (OBS).

A request for an abnormal condition interruption may occur at any time, and up to 30 requests may occur at the same time. The requests are preserved in the diagnose accessible register (DAR) until accepted by the CE.

An abnormal condition interruption can occur only while the CE is interruptable for the element presenting the request. The manner in which an interruption is handled depends upon the masking conditions prevailing in the CE, the type of element requesting the interruption, and upon the content of the configuration control registers in both the CE and the requesting element.

An abnormal condition interruption requested by an IOCE, SE, TCU, PAM, or by a CE(own) OTC, or CE(own) OBS signal sets an identifying bit in DAR. These bits are maskable by the DAR mask bits 0, 2, 4, or 6-25. (See Table 6-2). An unmasked bit set in DAR causes an interruption to be taken with bit 31 set in the old PSW, provided PSW mask bit 7 is one.

An abnormal condition interruption request from a CE (i.e., a CE-ELC also sets an identifying bit in DAR which is maskable by the DAR mask (bits 27-30).

Any CE-ELC bit set in DAR causes an interruption to be taken with bit 31 set in the old PSW, provided the scon bit for the requesting CE is already set in the CCR of the receiving CE, and either (a) or (b) is also satisfied.

(a) The receiving CE is in state Three, or in state Zero with the test switch on, and both the corresponding DAR mask bit and PSW mask bit 7 are ones.

(b) The receiving CE is in state One, Two, or Zero with the test switch off. Both the corresponding DAR mask bit and PSW bit 7 are ignored. The state field in the configuration control register of the receiving CE is set to Three.

When the scon bit for the requesting CE is not set in the CCR of the receiving CE, any CE-ELC bit set in DAR causes an interruption to be taken regardless of the state of the receiving CE, provided the corresponding DAR mask bit and the PSW mask bit 7 are ones.

Abnormal condition signals are out-of-tolerance check (OTC), on-battery-signal (OBS), and element check (ELC).

The OTC signal indicates that a rise in temperature above the normal operating range has been detected.

The OBS check indicates that the element is switched from its normal power supply to its battery supply.

The ELC signal indicates that an element failure is detected. Although precise interpretation of an ELC may require diagnostic analysis, generally a CCR parity check, machine check, or a power supply check is indicated.

Definitions for the abnormal condition signals peculiar to a TCU or PAM are described in System Reference Library (SRL) publications provided for each unit.

A bit in the diagnose accessible register (DAR) is unconditionally set on the receipt of an abnormal condition interruption request. Once set, a bit remains in DAR until reset by the execution of the store DAR kernel initiated

by the DIAGNOSE instruction. The entire content of DAR is then obtained without regard to the DAR masking.

If the condition which requested the interruption prevails after DAR reset, the bit is again set on.

The DAR mask is set by the execution of the set DAR mask kernal initiated by the Diagnose instruction. Once set, a DAR mask bit remains on until altered by another set operation.

i. Machine-Check Interruption

The machine-check interruption provides a means for recovery from, and fault location of CE and IOCE machine malfunctions.

(1) CE Machine Check

When the machine-check mask bit is one, occurrence of a machine check due to a CE malfunction terminates the current instruction, issues a signal on the element check (ELC) out-line, initiates a CE diagnostic procedure, and subsequencly causes the machine-check interruption.

The state of the CE is logged out into the preferential-storage area, starting with location 132 and extending through as many words as the CE requires. The old PSW is stored at location 48 in the preferential-storage area with an interruption code of zero. (An interruption code of four is stored to identify a Read Direct timeout.) The new PSW is fetched from location 112. Proper execution of these steps depends upon the nature of the machine check.

When the machine-check mask bit is zero, an attempt is made to complete the current instruction upon the occurrence of a machine check, and to proceed with the next sequential instruction. The element check (ELC) out-line is signaled upon occurrence of the machine-check condition. The diagnostic procedure and interruption occur upon the machine-check mask bit being changed to one.

A change in the machine-check mask bit due to the loading of a new PSW results in a change in the treatment of machine checks. Depending upon the nature of a machine check, the old treatment may still be in force for several cycles.

Following emergency power turn-off and turn-on, or system reset, incorrect parity may exist in storage or registers. Unless new information is loaded a machine check may occur erroneously. Once storage and registers are cleared a machine check can be caused only by machine malfunction and never by data or instructions.

The indication of the check condition which caused the machine-check interruption is preserved in the CE check registers until reset by a Diagnose operation.

(2) IOCE Machine Check

When the machine-check mask bit is one, occurrence of a machine check due to an IOCE malfunction issues a signal on the IOCE element check (ELC) out-line, initiates an IOCE diagnostic procedure, and subsequently causes the machine-check interruption. The current instruction is terminated in the controlling CE if it is an I/O instruction, otherwise the diagnostic procedure and the interruption take place after the current instruction interpretation is finished.

The state of the IOCE is logged out into the controlling CE's preferential-storage area, starting with location 324 and extending through as many words as the IOCE requires. The old PSW is stored at location 48 in the preferential-storage area with an interruption code of 1, 2, or 3 to identify the particular IOCE. The new PSW is fetched from location 112. Proper execution of these steps depends upon the nature of the machine check.

When the machine-check mask bit is zero, the IOCE waits in check-top status. The IOCE element check (ELC) out-line is signaled upon occurrence of the machine-check condition. The IOCE diagnostic procedure and interruption occur upon the machine-check mask bit being changed to one.

The indication of the check condition which caused the machine-check interruption is preserved in the IOCE check registers until reset during any IOCE logout.

G. Priority of Interruptions

During execution of an instruction, several interruption-causing events may occur simultaneously. The instruction may give rise to a program interruption, an external interruption may occur, a machine check may occur, and an I/O interruption request may be made. Instead of the program interruption, a supervisor-call interruptions might occur, however both can not occur, since these two interrupts are mutually exclusive. Simultaneous interruption requests are honored in a predetermined order.

The machine-check interruption has highest priority. When it occurs the current operation is terminated. Program and supervisor-call interruptions which would have occurred as a result of the current instruction are eliminated. Every reasonable attempt is made to limit the side-effects of a machine check. Normally, I/O and external interruptions, as well as the progress of the I/O data transfer and the updating of the timer, remain unaffected.

When no machine check occurs, the program interruption or supervisor-call interruption is taken first, the external interruption is taken next, and the I/O interruption is taken last. The action consists of storing the old PSW and fetching the new PSW belonging to the interruption first taken. This new PSW is subsequently stored without any instruction execution and the next interruption PSW is fetched. This storing and fetching continues until no more interruptions are to be serviced. The external and I/O interruptions are taken only if the immediately preceding PSW indicates that the CE is interruptable for these causes.

Instruction execution is resumed using the last-fetched PSW. The order of executing interruption subroutines is therefore the reverse of the order in which the PSWs are fetched.

The interruption code of a new PSW is not loaded, since a new interruption code is always stored. The instruction-length code in a new PSW is similarly ignored, since it is unpredictable for all interruptions other than program or supervisor call. The protection key of a new PSW is stored unchanged.

When interruption sources are not masked off, the order of priority in handling the interruption subroutines is machine chec, I/O, external, and program or supervisor call. This order can be changed to some extent by masking. The priority rule applies to interruption requests made simultaneously. An interruption request made after some interruptions have already been taken is honored according to the priority prevailing at the moment of request.

H. Interruption Exceptions

The instruction address in a new PSW is not tested for availability or resolution as the PSW is fetched during an interruption. However, an unavailable or odd instruction address is detected as soon as the instruction address is used to fetch an instruction. These exceptions are described in the section on normal sequential operation.

If the new PSW for the program interruption has an unacceptable instruction address, another program interruption occurs. Since this second program interruption introduces the same unacceptable instruction address, a string of program interruptions is established. This string may be broken by an external or I/O interruption. If these interruptions also have an unacceptable new PSW, new supervisor information must be introduced by initial program loading or by external or manual intervention.

Input/Output (old PSW 56, new PSW 120, priority 4)

INTERRUPTION SOURCE IDENTIFICATION	INTERRUPTION CODE PSW BITS 20-31	MASK BITS	ILC SET	INSTRUCTION EXECUTION
Multiplexor Channel A	0000 aaaaaaaa	0	x	Completed
Selector Channel 1A	0001 aaaaaaaa	1	x	Completed
Selector Channel 2A	0010 aaaaaaaa	2	x	Completed
Selector Channel 3A	0011 aaaaaaaa	3	x	Completed
Multiplexor Channel B	0100 aaaaaaaa	4	x	Completed
Selector Channel 1B	0101 aaaaaaaa	5	x	Completed
Selector Channel 2B	0110 aaaaaaaa	6	x	Completed
Selector Channel 3B	0111 aaaaaaaa	16	x	Completed
Multiplexor Channel C	1000 aaaaaaaa	17	x	Completed
Selector Channel 1C	1001 aaaaaaaa	18	x	Completed
Selector Channel 2C	1010 aaaaaaaa	19	x	Completed

Program (old PSW 40, new PSW 104, pariority 2)

INTERRUPTION SOURCE IDENTIFICATION	INTERRUPTION CODE PSW BITS 20-31	MASK BITS	ILC SET	INSTRUCTION EXECUTION
Operation	0000 00000001		1,2,3	Suppressed
Privileged Operation	0000 00000010		1,2	Suppressed
Execute	0000 00000011		2	Suppressed
Protection	0000 00000100		0,2,3	Suppressed/ Terminated
Addressing	0000 00000101		0,1,2,3	Suppressed/ Terminated
Specification	0000 00000110		1,2,3	Suppressed
Data	0000 00000111		2,3	Terminated
Fixed-Point Overflow	0000 00001000	36	1,2	Completed
Fixed-Point Divide	0000 00001001		1,2	Suppressed/ Completed
Decimal Overflow	0000 00001010	37	3	Completed
Decimal Divide	0000 00001011		3	Suppressed
Exponent Overflow	0000 00001100		1,2	Terminated
Exponent Underflow	0000 00001101	38	1,2	Completed
Significance	0000 00001110	39	1,2	Completed
Floating-Point Divide	0000 00001111		1,2	Suppressed
IOCE-3 PSA Lockout	0000 00010000		1,2,3	Terminated/ Completed
IOCE-2 PSA Lockout	0000 00100000		1,2,3	Terminated/ Completed
IOCE-1 PSA Lockout	0000 01000000		1,2,3	Terminated/ Completed
SE Stopped	0000 10000000		1,2,3	Suppressed/ Terminated

Supervisor Call (old PSW 32, new PSW 96, priority 2)

INTERRUPTION SOURCE IDENTIFICATION	INTERRUPTION CODE PSW BITS 20-31	MASK BITS	ILC SET	INSTRUCTION EXECUTION
Instruction Bits	0000 rrrrrrrr		1	Completed

External (old PSW 24, new PSW 88, priority 3)

INTERRUPTION SOURCE IDENTIFICATION	INTERRUPTION CODE PSW BITS 20-31	MASK BITS	ILC SET	INSTRUCTION EXECUTION
DAR	xxxx xxxxxxx1	7	x	Completed
Spare PIR (IOCE)	xxxx xxxxxx1x	7	x	Completed
CE4 Write Direct	xxxx xxxxx1xx	7	x	Completed
CE4 Read Direct	xxxx xxxx1xxx	7	x	Completed
CE3 Write Direct	xxxx xxx1xxxx	7	x	Completed
CE3 Read Direct	xxxx xx1xxxxx	7	x	Completed
Interrupt Switch	xxxx x1xxxxxx	7	x	Completed
Timer	xxxx 1xxxxxxx	7	x	Completed
CE2 Write Direct	xxx1 xxxxxxxx	7	x	Completed
CE2 Read Direct	xx1x xxxxxxxx	7	x	Completed
CE1 Write Direct	x1xx xxxxxxxx	7	x	Completed
CE1 Read Direct	1xxx xxxxxxxx	7	x	Completed

Machine Check (old PSW 48, new PSW 112, priority 1)

INTERRUPTION SOURCE IDENTIFICATION	INTERRUPTION CODE PSW BITS 20-31	MASK BITS	ILC SET	INSTRUCTION EXECUTION
CE Malfunction	0000 00000000	13	x	Terminated
IOCE-1 Malfunction	0000 00000001	13	x	Completed
IOCE-2 Malfunction	0000 00000010	13	x	Completed
IOCE-3 Malfunction	0000 00000011	13	x	Completed
Read Direct Timeout	0000 00000100	13	x	Completed

Legend

a	Device Address Bits
r	Bits of R_1 and R_2 Field of SUPERVISOR CALL
x	Unpredictable
DAR	Diagnose Accessible Register
PSA	Preferential Storage Area

Table 6-1. Interruption Action.

INTERRUPTION SOURCE IDENTIFICATION	DIAGNOSE ACCESSIBLE REGISTER CODE BIT	DIAGNOSE ACCESSIBLE REGISTER MASK BIT
IOCE-1a (See Note	0	0
IOCE-1b	1	
IOCE-2a	2	2
IOCE-2b	3	
IOCE-3a	4	4
IOCE-3b	5	
SE-1 ELC	6	6
SE-2 ELC	7	7
SE-3 ELC	8	8
SE-4 ELC	9	9
SE-5 ELC	10	10
SE-6 ELC	11	11
SE-7 ELC	12	12
SE-8 ELC	13	13
SE-9 ELC	14	14
SE-10 ELC	15	15
SE-11 ELC	16	16
SE-12 ELC	17	17
PAM-1 ELC	18	18
PAM-2 ELC	19	19
PAM-3 ELC	20	20
TCU-1 ELC	21	21
TCU-2 ELC	22	22
TCU-3 ELC	23	23
~~CE (own) OTC~~ SCU 1	24	24
~~CE (own) OBS~~ 2	25	25
~~Spare~~ 3	26	26
CE-1 ELC	27	27
CE-2 ELC	28	28
CE-3 ELC	29	29
CE-4 ELC	30	30
~~Spare~~ CE (own) OBS	31	31

Legend

ELC - Element Check OTC - Out of Tolerance OBS - On Battery Supply

NOTE:

External Signals from IOCEs are encoded as a two-bit field, designated a and b.

Interruption Source Identification	Bit Setting a	b
Normal Operation	0	0
OBS	0	1
OTC	1	0
ELC	1	1

Table 6-2. Abnormal Condition Interruption Action.

6-2. GENERAL CHARACTERISTICS OF 9020 OPERATION

A. Overall Operation

Figure 6-17 shows the general method of monitoring one element malfunctions by another. The case presented is the interruption of a CE to control the analysis procedure and determine a course of action after a malfunction is detected in another CE. Simplifying assumptions have been made (e.g., intermittent parity check) to present the philosophy. The two CEs are labeled malfunctioning and "attentive" since the attentive element need only be configured to listen to the malfunctioning CE and is not necessarily performing the ATC task (as may have been inferred previously). No indication is given of the masking which could be performed.

The general course of action taken in this situation may be divided into four phases, labeled A, B, C, and D on Fig. 6-17.

A. The malfunctioning CE detects an error. It stops its current processing and generates an element check to all CEs. It then proceeds to perform its own logout in three parts, as shown.

B. An "attentive" CE responds to the element check by performing an external interruption. It will indicate to the malfunctioning CE (by alteration of a program in storage) that there is a listening element. The attentive CE will then perform the necessary "first-line" analysis of the situation, in order to determine the immediate course of action necessary. This could also be extended to include a reasonably detailed analysis of logout data from the malfunctioning CE.

C. The malfunctioning CE now waits until action is taken by the attentive CE. In the event that the malfunctioning CE had not been informed that someone had been listening to its element check, it could elect to start an analysis of its own logout data. The success of this would depend upon the nature of the condition.

D. The malfunctioning CE will now respond to the course of action taken by the attentive CE.

B. System Facilities

Certain system facilities are provided to enable system monitoring. Among the more important of these facilities are:

Inter Element Signal Lines

Logout

External Interrupt

Diagnose Accessible Register (DAR)

Select Register (SR)

1. Inter Element Signal Lines

These are lines that exist between system elements and the CEs used to indicate that an exception condition (i.e. temperature tolerance check, power shutdown, CCR parity check, logic check, etc.) has occurred in that element. These external signals will cause a single external interruption in each of the receiving CEs that are not masked against the condition. If the originating element is a CE, the signal will bring all receiving CEs not in the zero state with Test switch "ON" into State Three, provided these CEs are configured to accept a SCON instruction from the originating CE.

Upon receipt of such a signal, the receiving CE will take appropriate actions to determine the operational status of the originating element and (1) attempt to alleviate the condition which generated the external signal, or (2) remove the element from the operation system.

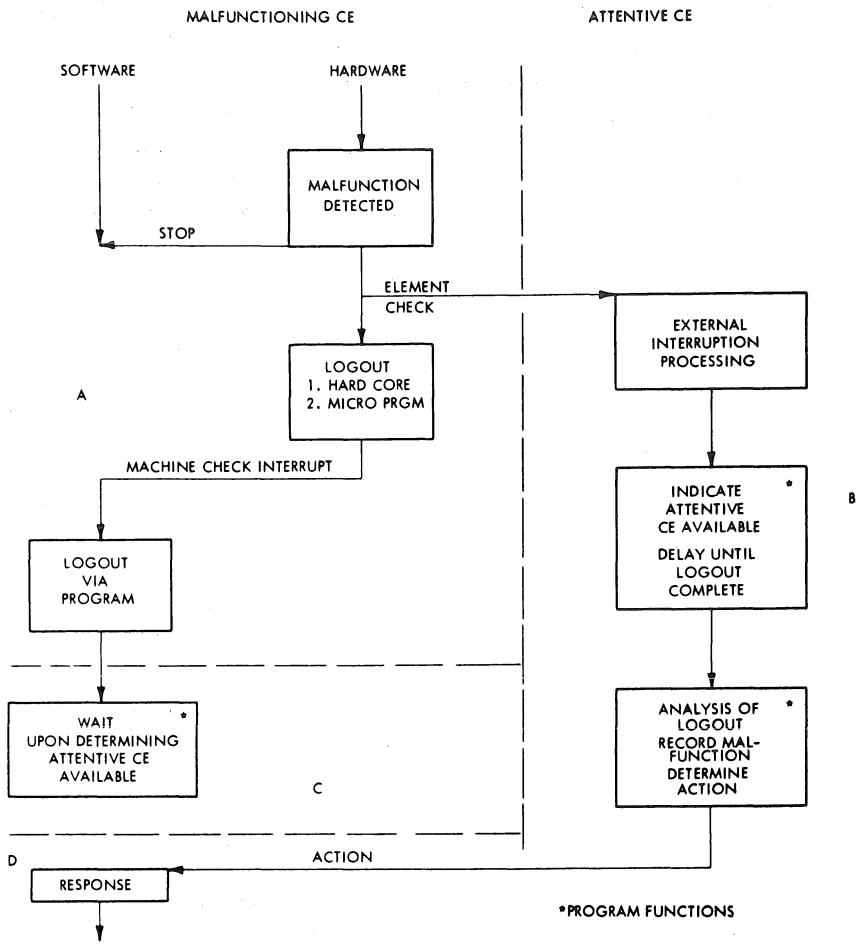


Figure 6-17. Monitoring of Element Malfunction.

The External Signals that can be expected are divided into three general categories:

Element Check (ELC); caused by an element failure (power or logic).

Out of Tolerance Check (OTC); caused by element temperature approaching marginal condition.

On Battery Signal (OBS); caused by an element switching from Main Line Power to batteries.

Figure 6-18 summarizes the conditions which result in an external interruption.

Element	Generating Condition	External Signal	Originating Element Status After Signal
CE	CCR Parity	ELC	Operational
	Logic Check & Storage	ELC	Check Stop*
	OTC	OTC	Operational
	OBS	OBS	Operational (5.5 sec)
	Power Check	ELC	Down
SE	Logout Stop	ELC	Stopped
	CCR Parity	ELC	Operational
	OTC	ELC	Operational
	OBS	ELC	Operational (5.0 sec.)
	Power Check	ELC	Down
	Storage Check	ELC	Operational
IOCE	CCR Parity	OBS/ Pulse	Operational
	Common Logic Check	ELC	Check Stop**
	Storage Check	ELC	Check Stop**
	OTC	OTC	Operational
	OBS	OBS/ level	Operational
	Power Check	ELC	Down
PAM-TCU	CCR Parity	ELC	Operational
	Power Check	ELC	Down
	Check Stop (PAM)	ELC	Down

OTC - out of tolerance (temperature)
OBS - on battery signal
* - This is the status of the element if the generating condition occurred during logout. If it occurred during processing, the CE initiates its own logout.
** - This is the status of the element if the generating condition occurred during logout. If it occurred during processing, the IOCE issues a machine check interruption request to its associated CE and waits for a response.

Figure 6-18. External Interruption (Non-Programmed) Status Table.

2. Logout

A logout signal to a CE or an IOCE will cause an orderly storing of control conditions and critical registers into a Preferential Storage Area (PSA) of a Storage Element (SE). The address of the specific PSA is pointed to by the PSBAR (Preferential Storage Base Address Register). Successful completion of the hardware logout will automatically activate a "machine check" interruption in the CE, or an I/O interruption by the IOCE. The processing of the interruption may include the "stored program" saving of additional registers (for the CE) to be placed in the PSA for later analysis, or it may result in a wait.

Logout of storage is under program control of a CE and the data is automatically placed in the local storage of the CE performing the logout. It is then placed in the PSA by the CE. The logout data is not available for analysis in Local Storage.

Detailed malfunction information is available for TCUs and PAMs via the normal I/O SENSE commands.

3. External Interruption

This facility allows the CEs to continually monitor System conditions of selected elements while simultaneously performing the normal processing functions.

The external interruption scheme (Fig. 6-19) of the 9020 System is provided to allow programmed signalling between various CEs and hardware signalling between the system elements and the CEs. Whenever an external interruption is accepted by a CE, a unique bit is set in that CE. The external interruptions are completely maskable by bit 7 of the current PSW, except as described in Fig. 6-21. The interruptions are divided into two classes: normal, and abnormal.

4. Normal Interruptions

Interruptions that fall into this category are those illustrated by item three on Fig. 6-19. These are program controlled and not related to System Check conditions. The CE Read and Write (Direct) indications are under control of the CCR described previously. The Interrupt and Timer bit positions in the PSW will be set regardless of the CCR. A more detailed description of this type of interruption is given in the 9020 System Principles of Operation Manual. Normal interruptions do not require use of the DAR and, therefore, bit 31 of the PSW will not be set for normal interruptions.

5. Abnormal Interruptions

Interruptions that fall within this category are illustrated by item 4 of Fig. 6-19. These are the hardware generated signals of current or impending failures. Each signal of this class, if not masked, will cause the DAR bit to be set in the PSW. This, in turn, will cause an external interruption if bit 7 of the PSW is not set to mask external interruptions. The components of the external interruption system of each CE, with usage and control, are defined below.

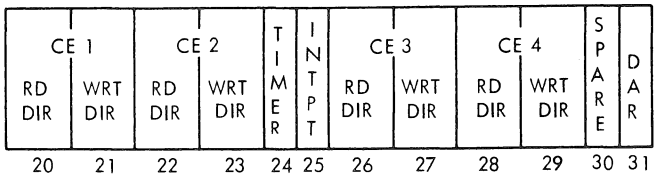
6. Masking

Bit 7 of the System Mask section of the current PSW is used to mask external interruptions with the exception of CEs in State Two, One, or Zero (with Test Switch Off) which are configuration accept a SCON instruction from the originating CE, when CE ELCs ignore Mask Bit 7. If this bit is a "one", interruptions can proceed as usual. If zero, all interruptions are held pending until the bit is one or the CE is reset. There are multiple unique reasons for external interruptions. If, while masked, more than one request for a single reason is received, all but the last request will be lost (i.e., although multiple external interruption requests may be stacked, only one of a particular type will be saved).

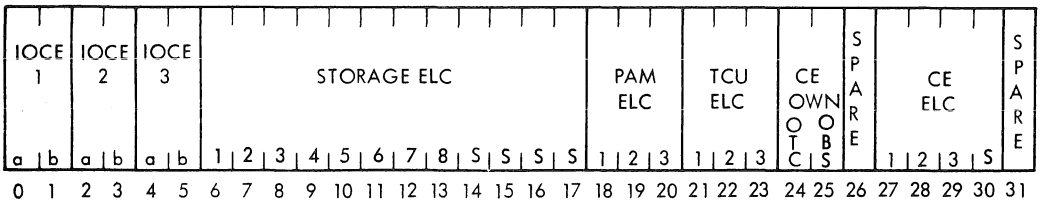
1. All External Interruptions except those from CE's are maskable with bit 7 of the PSW.

2. The old PSW contains the interruption source in bits 20 thru 31.

3. These indications are as shown:



4. Bit 31 above, the DAR bit, indicates that at least one of the bits in the Diagnose Accessible Register (DAR) has been set. The format of DAR is:



Note that ELC's from IOCE's are encoded as follows:

a	b	
0	0	No Checks Signals
0	1	OBS (Note: pulse = CCR parity; level = OBS)
1	0	OTC
1	1	ELC

5. The DAR provides detailed interruption source information. A bit in the DAR is unconditionally set on the receipt of an abnormal condition signal. These bits are set without regard to existing CCR settings, except for CE ELC's which are masked by SCON bits. Each bit in the DAR is individually maskable by a corresponding bit in the Select Register (SR), except for the bits indicating IOCE information. Since IOCE data is encoded, one bit in SR will mask both IOCE bits. Specifically, SR bit 0 will mask DAR bits 0 and 1. SR bit 2 will mask DAR bits 2 and 3. SR bit 4 will mask DAR bits 4 and 5. SR bits 1, 3, and 5 will be considered spare. If the corresponding bit is "on" in SR, a bit in DAR will cause the DAR bit (bit 31) to be set in the PSW at the time the interruption is taken.

Figure 6-19. External Interruption Controls and Indications.

7. PSW Interruption Code

Bits 20 through 31 of the PSW contain the identification of the external interruption source. Item three of Fig. 6-19 illustrates the source identification.

The eight bits associated with CE Read and Write Directs are gated through the CCR. That is, if the CE is not configured to listen to the requesting CE, the request will be ignored, and the bit in the Interruption Code will not be set. If the CE is configured, the appropriate bit will be set in the PSW and an external interruption will be attempted if not masked by PSW bit 7.

The Interrupt and Timer bits are set any time the source signals, and will cause an interruption if bit 7 is not masked.

The DAR bit refers to a special register that contains a group of interruption identification conditions, too numerous to be included in the PSW. The DAR bit is set at the time the external interruption is taken.

8. Diagnose Accessible Register (DAR)

The DAR is so named because it is not normally an addressable register; a Diagnose instruction is required for access. This register is used to store and identify hardware generated external interruption requests. At the time of an external interruption this register will be read to supplement the PSW. The conditions that set this register are illustrated by Fig. 6-18. The register layout is shown by item 4 of Fig. 6-19.

When any element generates one of the specified interruption requests, its identification bit is set in DAR. This bit will cause an external interruption if the mask conditions are met. These conditions are:

Each position of the DAR has a corresponding mask position in the Select Register (SR - to be described later). If the SR bit is 1, and bit 7 in the current PSW is set to 1, an external interruption

will occur at the completion of the current instruction with the DAR bit in the old PSW set to 1. (The following section will describe the special masking technique for IOCE bits in the DAR.)

When a CE is in State Two, One, or Zero (with the Test Switch Off), CE ELCs cannot be masked off -- that is, mask bits are ignored, if the CE is configured to receive a SCON instruction from the originating CE. — Receiving CE goes to State 3.
If Receiving CE is in State 3 or Ø and Test switch ON then you look at DAR Mask and PSW bit 7.

The bits in the DAR will remain set until a read instruction (Diagnose) is issued to the register; then the entire register will be reset.

The character of each signal (pulse or level) which sets DAR is specified in this chapter under the subsequent topic labeled "9020 Malfunction Handling". If the signal which sets DAR is specified as a pulse, then reading of DAR will clear the affected bit and it will not be set again, unless, of course, the condition occurs again. If the signal which sets DAR is a level, then reading of DAR will clear the bit momentarily, but it will be immediately set again. This forced setting of DAR will continue until the condition causing the signal is cleared. An examination of these level signals, however, will show that there should be no ambiguity in interpretation, since a level will indicate either a non-determinable time for the condition; e.g., OTC, power off, etc., or will indicate the condition causing the signal has also forced the affected unit to cease operation and require assistance. This method of signaling, in fact, will provide valuable in determining whether or not an element can perform some degree of self-diagnosis or must be assisted. As an example, assume that a CE has detected some error and generates a check signal. This is sent to all other CEs as an ELC and will set the appropriate DAR bit. This signal is a pulse; when read by the receiving CE, the receiving DAR bit will be cleared. The CE which generated the ELC will proceed to log-out to its PSA. Suppose, however, that the CE is unable to perform this log-out. This could occur for several reasons, but usually because of double errors. The CE would generate a second ELC and stop. This signal, however, is a level. A receiving CE, if it read its DAR twice in succession, would

find the DAR bit still set. This static ELC would remain until the CE which generated it was restarted by some external means.

When DAR is read via Diagnose, the entire register is obtained without regard for any mask which may be used to control interruptions. No interruptions will set DAR during the read operation.

9. Select Register (SR)

The SR is program addressable (write) by a special Diagnose instruction. It serves the purpose of allowing program control over the elements and conditions from the elements that will be allowed to cause an external interruption in this particular CE. The CCR limits normal data flow between the various system elements while the SR independently limits exception data flow between the system elements.

SR contains a position for each position of DAR, except as noted in the next paragraph. If the SR position is set to one, a corresponding interruption request through DAR will set the DAR bit in the PSW and request an external interruption. If the SR is zero, corresponding positions of DAR will not be allowed to propagate to the DAR bit in the PSW; note previous exceptions on CE ELCs.

There are only two bits allotted for each IOCE, and they are not sufficient to indicate the necessary conditions. Consequently, these bits are encoded (see Fig. 6-19), and can not be considered to be distinct indications. SR will mask both bits for each IOCE with a single mask bit. Specifically, the masking arrangement is as follows:

DAR Bits	SR Mask Bit
0, 1	0
2, 3	2
4, 5	4

SR bits 1, 3, and 5 will be considered spare bits.

10. Special Element and System Condition Signals

The conditions which generated external interruptions were itemized in the previous section. This section discusses all the signals of this nature from the elements and the method of handling them independent of whether an external interruption is generated. Figure 6-20 summarizes the handling procedure.

Condition / Element	OTC (Out of Tolerance)	Power Off	CCR Parity	Logic Check	OBS (On Batteries)
CE	EXT - to itself only	EXT	EXT	EXT	EXT - to itself only
IOCE	EXT	EXT	EXT Pulse on OBS line	EXT - Common Equip PRGRM - Sel. Chn	EXT
SE	EXT	EXT	EXT	EXT (Sto check also to using element)	EXT
TCU	PRGRM	EXT	EXT	PRGRM	NONE
PAM	PRGRM	EXT	EXT	PRGRM EXT (Check Stop)	NONE

Note: EXT = External interruption to all listening CE's

PRGRM = PROGRAM interruption handled by the subsystem monitor in normal programming fashion

Figure 6-20. Summary of Procedure for Handling External Interruption Signals.

a. Power Supply

The power supply output malfunction of any major element will cause an ELC condition to be generated for that element at the Computing Elements.

b. Out of Tolerance (OTC)

Sensing is provided by all major system elements for control temperature conditions. The following indications have been defined for each element of the system for OTC checks.

CE: An OTC condition in a CE will cause that CE to take an external interruption. This condition will cause a unique identification bit to be set in the DAR of the CE to allow identification of the cause.

It is expected that each CE can handle its own OTC checks since they do not indicate an error environment but instead provide a warning of an environment that could soon become erroneous. If the CE cannot finish its expected actions before a power shutdown, the latter condition (Power Supply above) will cause an ELC signal to the remaining CEs indicating trouble.

SE: An OTC condition in an SE will cause that element to generate an ELC. This ELC will be sent to all CEs. Those that are not masked for the condition will taken an external interruption. This condition will set a unique identification bit in DAR. The functional capability of the SE shall not be impaired by the generation of this ELC. An SE logout will be necessary to further isolate the ELC originating conditions.

IOCE: An OTC condition in an IOCE will cause that element to generate an OTC. This OTC will be sent to all CEs. Those that are not masked for that condition will taken an external interruption. This condition will set a unique identification code in DAR. The functional capability of the IOCE shall not be impaired by the generation of this OTC.

TCU: An OTC condition in a TCU will cause that element to generate an "Attention" on its IOCE - TCU interface as part of the status byte either at the end of an operation or when an attempt is made to select the TCU. The Attention signal is only used for OTC indications by this unit. This interruption condition is handled in the same manner as any other interruption condition.

The generation of the OTC condition will not affect the operational capabilities of the TCU.

PAM: At OTC condition in a PAM will cause that element to generate "Attention" status from the Test and Monitor Adapter. This interruption condition is handled in the same manner as any other interruption condition.

The generation of the OTC condition will not affect any of the operational capabilities of the PAM. A sense command through the IOCE will be necessary to detect that an OTC condition does exist. The sense data will include among other things an OTC bit and CCR parity indication.

c. CCR Parity

Every major element has a CCR register. Parity is continually monitored on this register by the element and whenever incorrect parity is detected, an ELC is generated. However, if the CCR is actually being loaded, generation of ELC is suppressed since other means are used to inform EXC (Executive Control Program) of the condition. This ELC will be transmitted to all CEs. Those that are not masked for that condition will taken an external interruption. The ELC condition will cause an ELC identification bit or code to be set in DAR.

Should an element's CCR become set to allow no CE to issue a SCON to the element, this element would be lost to automatic system control. This condition can occur only through a malfunction or through manual action. Equipment is provided to detect this condition.

When this condition is detected, the CCR SCON field gating is bypassed, and the element will accept a SCON from any CE, provided that the element is not in State Zero. If an element is in State Zero, and its SCON field is set to all zeros, it is presumed to be a desired condition, and all SCONs are rejected.

A special indicator is used for CCR parity from the IOCE. This is a pulse on the OBS indication to provide ease of identification. The normal OBS indication is a level.

The generation of the ELC will not affect the operational capability of the element. For further analysis of the condition it is necessary to logout or sense the element.

d. Logic Check

Every system element has built-in internal checking procedures which are delineated in the following section. This section does not include the CCR which has been described previously.

CE: An internal logic check will cause the CE to signal an ELC to all other CEs. The CE which has the logic check may proceed with a logout, depending upon whether its machine check interruption is masked or not.

IOCE: An internal common logic check (or multiplex channel check) will cause the IOCE to CHECK STOP and signal an ELC to all CEs, the reception of which was described previously. The IOCE will request a special machine check interruption which will allow it to logout from the configured controlling CE.

A malfunction in a selector channel hardware will cause that channel to STOP. The IOCE will request an I/O interruption of its configured CE. When the interruption is permitted, the selector channel will be logged out and the interruption performed.

SE: An internal logic check of an SE will only be signalled when another element is using it. The signal will appear as a pulse ELC to all CEs, and as a Storage Check to the using element.

TCU: The TCU will attempt to signal the IOCE of any logic failures and expect remedial action through the IOCE using normal I/O checking hardware (and software). Malfunctions affecting only an individual Tape Drive or associated path will not affect the operation of the remainder of the TCU. Malfunctions originating from the common logic of the TCU will affect the entire TCU system.

PAM: PAM malfunctions are attempted to be signalled to the IOCE and remedial action is expected through the IOCE interface in much the same fashion as the TCU. Some malfunctions in PAM common will stop all PAM data service cycles, while malfunctions originating in the PAM adapters will only affect the malfunctioning adapter.

e. On Battery Signal (OBS)

Three of the major elements of the system (CE, IOCE, and SE) have battery backup in case of power failure. A means is provided to signal when the batteries are being utilized. Switching from normal operation to batteries will cause an On Battery Signal (OBS) to be generated.

This OBS will be treated in the following manner for the affected elements.

CE: Only the generating CE will receive its own OBS signal. This signal will cause an external interruption. This condition will set a unique identification bit in DAR. The operational status of the CE will not be affected by the generation of the signal.

IOCE: The IOCE will transmit its OBS to the CEs as a level. The CEs, if not masked for the condition, will taken an external interruption. A unique OBS identification code will be set in DAR in the CE. The operational status of the IOCE will not be affected by the generation of this signal. To enable

rapid identification, the CCR parity indication is signalled as a pulse in the OBS line.

SE: The SE will transmit its OBS signal under the common heading of ELC to all CEs. These CEs, if not masked for the condition, will taken an external interruption. This condition will set that SEs unique ELC bit in DAR in the CE. An SE logout is necessary to determine the cause of the ELC. The generation of the signal will not affect the operational capability of the SE. A chart summarizing the method of handling external interruptions is shown in Fig. 6-21.

6-3. SYSTEM MAINTENANCE CONCEPTS

Maintenance of the 9020 System, as is true with all types of maintenance, is generally accepted to take place in two broad categories, routine preventive maintenance and corrective maintenance. Routine preventive maintenance, as visualized, would include the lubrication, adjustment, and cleaning of the various component equipments which go to make up the system. The operation of the system using diagnostic tests as well as the operation of elements using Fault Location Tests either under normal conditions or under biased voltage conditions are also included in this broad category. Since these activities are covered in detail in the various maintenance manuals, they will not be covered at this time.

Corrective maintenance of the system presents several other problems. The first problem faced by the Systems Engineer will be to resolve whether the failure was due to program malfunction, or due to an actual hardware failure. While it would seem unlikely that a program which had operated satisfactorily for some period of time would suddenly develop trouble, this should not be overlooked. Programs have been known to operate satisfactorily for months or even years and suddenly refuse to operate due to an unforseen branch or interrupt. The next problem faced in the correction of the malfunction would be to determine which element of the system is failing. Due to the interrelationships of the elements this may not be as readily apparent as it might

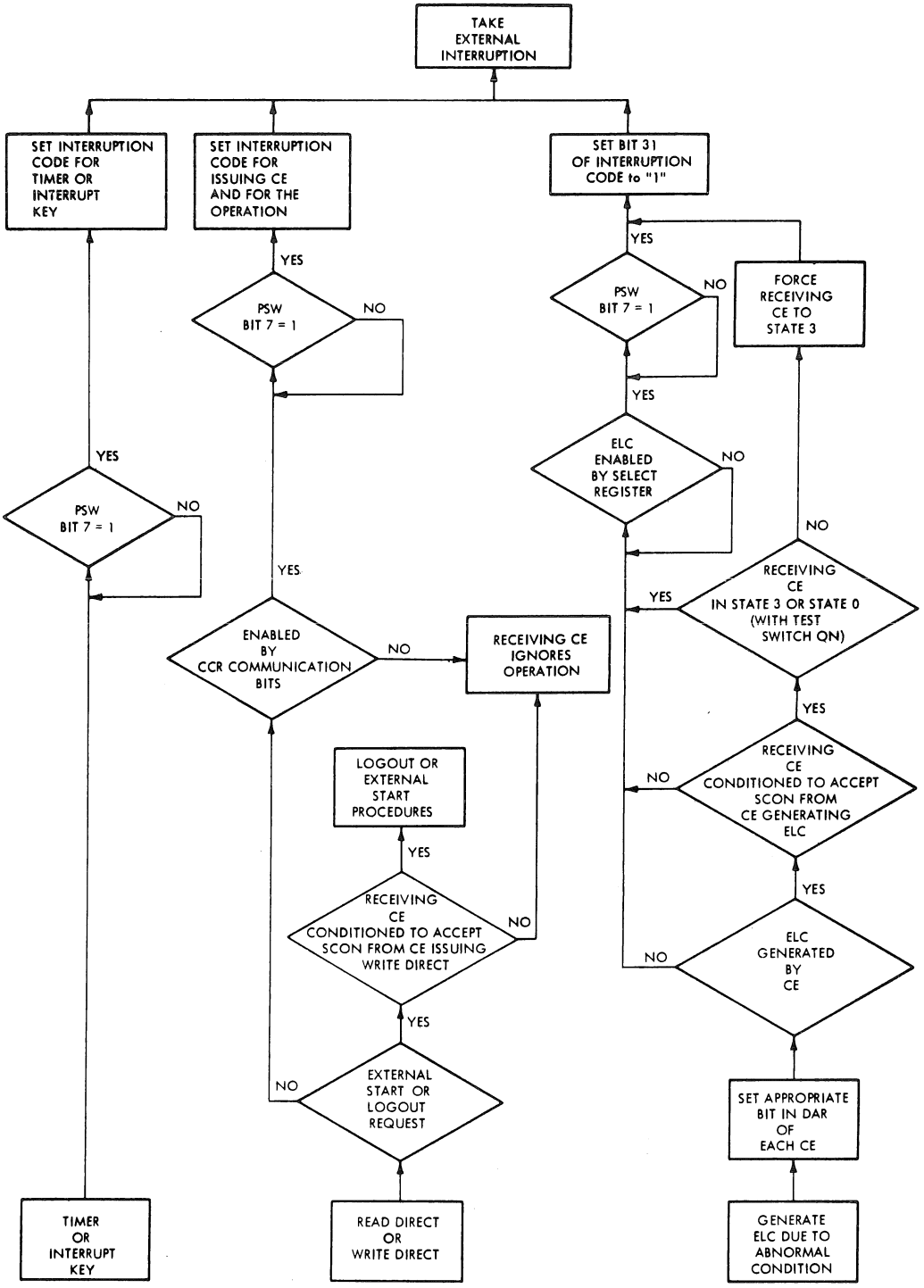


Figure 6-21. External Interruption Handling.

seem; however, with the aid of logout information or diagnostic programs isolation of the failing element should be possible. Once this is accomplished, the maintenance technician should be capable of correcting the malfunction and returning the element to service.

To assist in the repair of the failing element the technician or engineer has various tools and methods at his disposal. Depending upon the circumstances, the technician or engineer may elect to begin trouble analysis at the engineering panel of the element, or, he may elect to begin diagnostic program tests. This is dictated by such factors as the availability of a subsystem, whether a logout is already available, whether the element has already been isolated from the system, whether the failure is intermittent in nature or a solid fail, etc. The important thing is that within the system there is a definite hierarchy of tests.

Each of the elements has provision for testing its own internal circuitry. This may be in the form of an engineering or maintenance panel, or in the form of an externally connected tester. The major elements such as the CE and IOCE have special purpose test circuitry built into them to enable a certain degree of circuit evaluation without any additional equipment. These elements also have special purpose ROS routines to further enhance the ability to test.

The ROS routines and special purpose test circuitry generally require very little operational hardware to present indications pointing to malfunctioning units.

The next step in the hierarchy of testing procedure would be the running of the Fault Locating Tests (FLT) for the element. These tests utilize the special purpose hardware to verify the operation of other special purpose test circuitry and then uses this circuitry to assure the operation of the ROS. Once the test circuitry and the ROS operation is assured, the FLTs test the functional units and finally the data paths between the functional units. This is a boot-strapping procedure whereby a failure in an early portion may

create multiple failures in later steps. For this reason it is generally wise to troubleshoot the earliest possible stop in the tests. Since FLTs perform their tests on the functional units and data paths 16 times, these tests have been found very useful in isolating intermittent failures.

Having used the element test panels and successfully run the FLTs, the elements are now ready to be tied together to form a subsystem. The next form of tests provides the ability to test intercommunication between elements of the system and isolate malfunctions in the processing of actual machine instructions. The MDM and SDM tests (Maintenance Diagnostic Monitor and Subsystem Diagnostic Monitor) use certain basic instructions with predetermined data to assure the capability to perform these instructions, then using these instructions prove or test the ability to perform others in the set. MDM and SDM assume that the functional units are operating and in general do not provide resolution other than the inability to perform a given machine instruction. These tests are tailored to the system on which they are to be operated and must be modified any time there is equipment added or deleted. The highest form of testing for the 9020 System is the System Evaluation tests (SEVA). These tests provide virtually no resolution to hardware malfunctions; however, the ability to perform this series is a good indication of the systems ability to perform peroperly. These tests are contained with the SDM and MDM and may be called by the diagnostic test operator. MDM, SDM, and SEVA also contain sections to verify the operation of the various I/O devices.

A. 9020 Malfunction Handling

This section describes the actions of the 9020 System when errors are detected in a 9020 element or unit. The discussion is limited primarily to a description and explanation of the way in which the built-in equipment for error-processing functions. It must be understood, however, that the complete system response to an error is of necessity a combination of reactions by both program and equipment. Where it is important to the discussion, certain programming functions will be discussed. Considerable flexibility of program

action is permissible, making possible a total system error response as sophisticated as desired.

Errors occurring in the PAM and TCU are also treated in this section, although most errors which occur in those elements are communicated to the system via the usual input/output control programs. Errors which result in an ELC from those units will be handled as an external interruption by the receiving CE(s). There is no special hardware which causes unusual action in these two elements, such as exists in the CE, IOCE, and SE. The equivalent of logout information in PAM and TCUs is obtained as sense data through regular program operation.

1. General Considerations

A useful preliminary to a detailed discussion of error processing will be a summary of the types of errors which affect each of the three elements, and a brief examination of the kind of action which can result.

a. Computing Element (CE)

Four broad categories of errors are of concern to a CE:

1. The inability of a CE to obtain, upon request, a cycle from a storage element.
2. Errors which the CE detects in its own error detection logic.
3. Errors which are signalled to the CE by an SE with which it is currently communicating or by an IOCE which the CE is controlling.
4. Errors which are manifested as External, Program, or I/O interruptions from other elements.

If a CE is unable to obtain a cycle from a storage element, it will conclude, in general, that either a program error or an equipment malfunction has occurred. If the circumstances indicate a program error, a program interruption will occur; otherwise a machine check interruption will be taken with appropriate

inter-element error signals generated. Where the inability to obtain a storage cycle occurs on a reference to the PSA, the CE will attempt to obtain a corresponding location in an alternate PSA.

Errors detected by the CE in its own error detection equipment will cause a machine check interruption, logout, and appropriate inter-element error signals to be generated. If the error detected by the CE is at the point of data entry from an SE, and if the CE is using that SE for a data fetch type operation, then the CE will cause the SE to be stopped in order that the SE may be logged out also. This action is taken to assist in the isolation of interface errors, since without knowing whether or not the data was correct as it left the SE, it cannot be determined if the CE or SE caused the malfunction.

If an SE detects an error in its own equipment when working with a CE, this error signal is communicated to the using CE. The CE will cause the SE to stop, and a CE machine check interruption will occur, followed (normally) by a programmed logout of the SE. It is necessary to proceed in this fashion in order to permit the system to obtain sufficient data for malfunction isolation and subsequent recovery. An error in the IOCE will be signalled to the CE as a special Machine Check interruption. This mechanism is used to allow the CE to respond quickly and orderly to IOCE malfunctions. The CE will not logout, but can immediately enter a program for diagnosis of the IOCE problem.

The last category of errors with which the CE is concerned directly are those which are signalled via the various interruption facilities. These are external, program, and I/O interruption; their handling is a programming function and will not be of immediate concern here since no unusual equipment functions are involved. It should be pointed out again, however, that the processing of these interruptions must be considered in the overall sense as a significant part of the system malfunction handling technique. The type of error communicated via an interruption will usually originate in an element external to the CE. Hence, the programming response must integrate these into a complete, cohesive malfunction handling scheme.

b. Input/Output Control Element (IOCE)

There are three categories of errors in the IOCE which are of concern here, viz:

1. The inability of an IOCE to obtain, on request, a cycle from a storage element.
2. Errors which the IOCE detects in its own error detection logic.
3. Errors which are signalled to the IOCE by an SE with which it is currently communicating.

If an IOCE is unable to obtain a cycle from a storage element, it will in general conclude that either the address it is using is invalid, indicating a programming error, or that an equipment malfunction has occurred. If the circumstances indicate that the cause is an invalid address, then the IOCE will notify the using CE via an I/O interruption with a program check in the channel status word that this has occurred.

If the invalid address indication occurs during IOCE logout, the IOCE will request a new PSA from the CE. If the circumstances indicate an equipment malfunction, then the IOCE will generate the necessary inter-element signals and will perform a logout to the PSA.

Errors detected by the IOCE in its error detection logic include those which occur in the common logic area and those which occur in the channels. An error occurring in the IOCE common logic or multiplexor channel will cause the IOCE to request a logout via a special machine check interruption request to the controlling CE. An error occurring in the IOCE's selector channels will cause a logout of that channel via an I/O interruption, unless the selector channel is performing a Test Channel operation; in this case the logout will be done via the special machine check interruption. In both cases, appropriate inter-element error signals are generated.

If an SE working with an IOCE detects an error, it is communicated to the IOCE, which will cause the SE to stop. The IOCE will request, via the special machine check interruption, that the IOCE be allowed to logout. This would then (normally) be followed by a programmed logout of the SE by the controlling CE.

In each case of IOCE malfunction, every possible effort is made to reduce its effect on the IOCE's handling of data from channels not affected. It is assumed that most errors are of a transient, self-clearing nature, and that continuation is usually possible.

c. Storage Element (SE)

Malfunctions in the SE are classified in two groups:

1. Storage Checks - These are malfunctions resulting from internal storage equipment parity check, address check, or logic function check. Detection of this type error will cause an ELC to all CEs, plus a storage check signal to the using element (CE or IOCE).
2. Others - These include CCR parity check, OBS, OTC, and power failure. CCR parity, OBS, and OTC, cause a pulse ELC to all CEs. Power failure causes a static (level) ELC to all CEs.

The significance of this grouping is that the SE operations are not directly affected as a result of a malfunction in (2) above. These malfunctions are considered to be in equipment external to the SE; thus, the SE does not take any action insofar as error processing or special procedures on these malfunctions.

Those malfunctions in (1), i.e., storage checks, could immediately affect the validity of the storage data; thus, a signal is sent to the using element. When a storage check occurs, the SE will complete its current cycle and wait 2.5 μs before beginning a new cycle. During this 2.5 μs, the using element

may issue a logout stop signal to the SE (Figs. 6-24 and 6-25). This signal will cause the storage to refuse any further requests for service until it has been logged out or told to resume action by a CE.

2. Storage Access Malfunctions

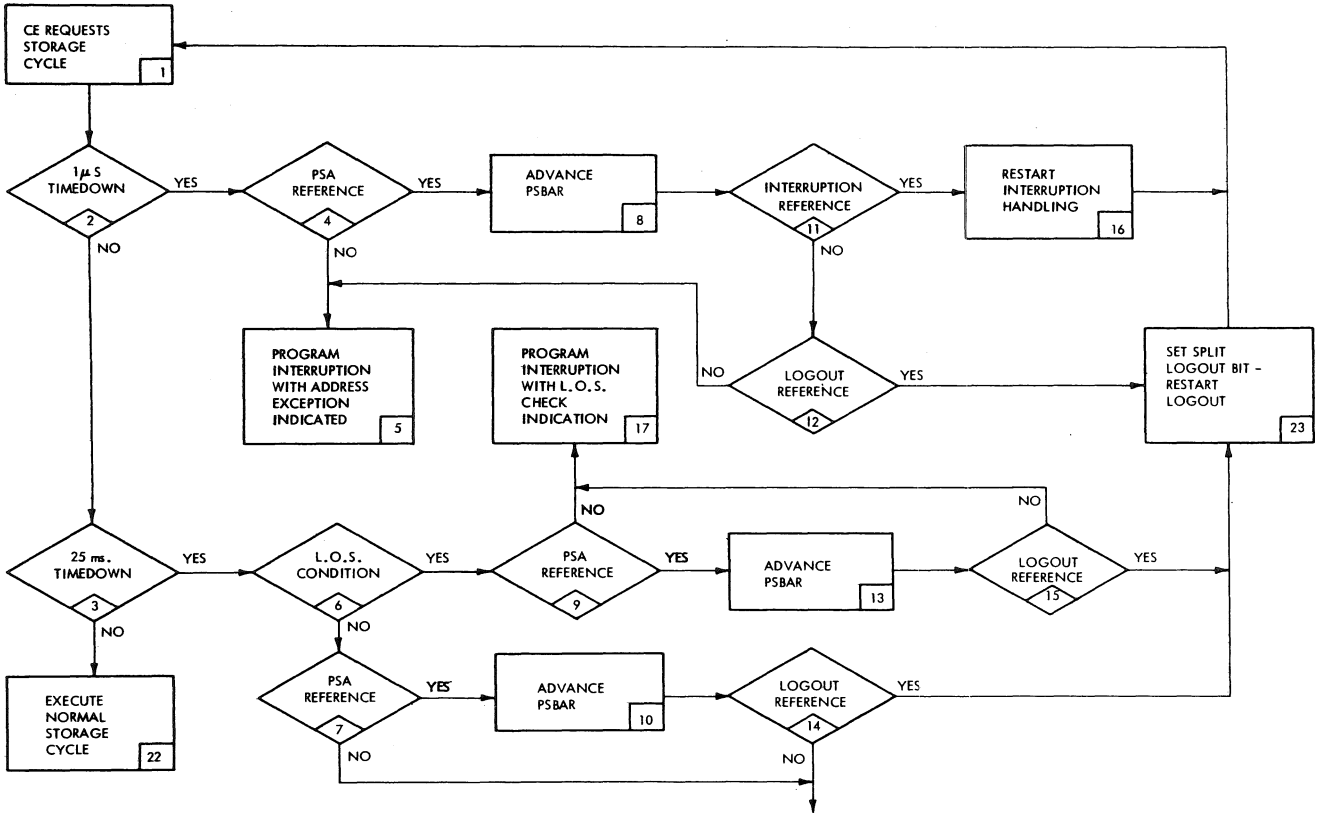
This section describes the actions which occur in the CE and the IOCE when either of these elements is unable to obtain a requested storage cycle from an SE.

The diagrams which accompany the explanations in this and all following sections are intended as functional representations of the sequence of events. All actions shown are accomplished by 9020 hardware; however, the diagrams do not necessarily reflect the manner in which the functions are implemented.

For ease of reference, each separate function on a diagram is enclosed. These enclosures are numbered sequentially on the diagram. They will all be referred to as "boxes", e.g., box 12, in the text. The rectangular "boxes" indicate an action or procedure. The diamond-shaped "boxes" indicate decision points in the flow, with exits reflecting the outcome of the decision.

a. CE Actions

Figure 6-22 portrays the sequence of events which will occur when a CE requests access to an SE for a cycle, either to read or store a word. It is assumed that the address of the desired storage location has been determined in the CE, and the CE then sends a request for a storage cycle to the selected SE at box 1. If the CE is configured to listen to the selected SE, and the selected SE is configured to listen to the requesting CE, then a response to this request will be returned to the CE (assuming power is up on the SE). A period of 1 μs nominal (referred to as a 1 μs timedown) is allowed for this request-response completion. Box 2 indicates this.



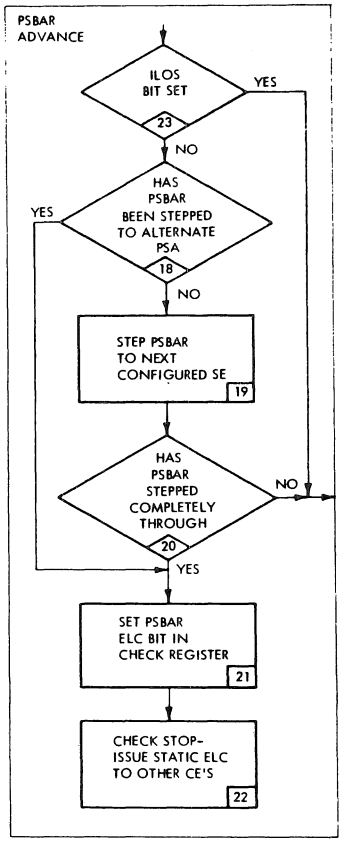


FIGURE 6-24

Figure 6-22. Response Type Error Handling for CE-SE Accesses.

Assuming the response is received within 1 μs (No exit for box 2), then the CE will wait for the honoring of its cycle request an average period of 25 milliseconds (ms). This delay is present to account for situations where the CE is low on the priority chain, with the possibility that an extended I/O operation is occurring in the SE. The 25 ms (avg.) period can vary from approximately 16 to 32 ms, depending upon the position of the interval timer when the request is initiated. If the cycle is made available to the CE within this period (No exit from box 3), the storage cycle is used by the CE.

Return to box 2. If the initial access request is not acknowledged to the SE within a nominal 1 μs (Yes exit from box 2), then an exception condition has been encountered. Box 4 indicates that a determination is next made as to the reason for the storage request, i.e., was it a PSA reference or was the request a normal one. If the reference was not to the PSA (No exit from box 4), then a program interruption with address exception is taken at box 5. If the request was to the PSA (Yes exit from box 4), then the PSBAR will be advanced to locate an alternate PSA. (An expansion of the PSBAR advance function is given in Fig. 6-22). At box 11, a decision is made as to whether an interruption was in progress. If so (Yes exit from box 11) then the interruption handling is restarted at box 16, resulting in a new request for a storage cycle. The interruption will then be to the alternate PSA. If no interruption was in progress, (No exit from box 11) a check is made at box 12 to see if logout was being performed. If not (No exit from box 12) then a program interruption is taken at box 5.

If the reference to PSA was made during logout (Yes exit from box 12), then the CE will set a "split logout" bit in the check register and prepare to restart logout from the beginning at box 23. It then will proceed to request a storage cycle to perform the logout. This will result in a so-called "split logout", i.e., the part of the logout which had occurred prior to the access malfunction will be in the primary PSA, and the logout representing the machine environment at the time of the access malfunction will be in the alternate PSA. It will be possible to reconstruct the original environment from the combined contents of the primary and alternate PSAs.

Return to box 3. If the storage cycle is not made available to the CE within the 25 ms (avg.) period, then it is assumed that either an equipment malfunction has occurred, or that the CE tried to access an SE which was stopped for logout. At box 6, it is determined whether or not a logout stop condition exists in the SE which was referenced. If not (No exit from box 7), then the CE can take no further action and proceeds to the CE error sequence, shown on Fig. 6-24. If the reference was to PSA (Yes exit from box 7), then the CE first advances PSBAR and checks to see if logout was in progress at box 14. If not (No exit from box 14), then the CE error sequence is entered. If logout is in progress (Yes exit from box 14), then the CE proceeds to box 23 to begin the logout restart sequence.

If it is determined that the SE which is being referenced is stopped for logout (Yes exit from box 6), then there is no reason to logout the CE or execute the CE error routine. At box 9, it is again determined whether the reference was to the PSA. If not (No exit from box 9), a program interruption with the chaining check in the PSW is taken at box 17. If the reference was to the PSA (Yes exit from box 9), then PSBAR is advanced and it is determined at box 15 if logout was in progress. If not (No exit from box 15), then the LOS program interruption is taken at box 17. If logout is in progress (Yes exit from box 15), then the logic proceeds to box 23 to restart logout.

The right portion of Fig. 6-22 is an expansion of the PSBAR Advance function. At box 23 it is determined whether the Inhibit Logout Stop (ILOS) bit is set on. If it is, (Yes exit from box 23), PSBAR is not advanced and the logic flow proceeds. If ILOS is not on (No exit from box 23), then it is ascertained whether or not PSBAR has been stepped to an alternate PSA as a result of a previous malfunction (Box 18). If it has (Yes exit from box 18), then the CE will set the PSBAR ELC bit in the check register (box 21) and it will check-stop and issue a static ELC to all other CEs, since there is no further action it can take on its own. If PSBAR has not been stepped (No exit from box 18), then it is stepped to the next configured SE (box 19).

In its search for the next configured SE as an alternate PSA, the PSBAR is stepped by 32K words each time. To preclude an endless loop if the CE had no storage configured to it, a check is made at box 20 to see whether or not PSBAR has been stepped completely through its range during this search. When PSBAR steps through the entire range and then begins the search a second time, without finding any configured SE, a Yes exit from box 20 will occur, resulting in the CE setting the PSBAR ELC bit in its check register and in a CE stop and a static ELC. If PSBAR has not stepped through the entire range (No exit from box 20), then the logic flow proceeds.

b. IOCE Action

Figure 6-23 depicts the IOCE actions which occur when an IOCE makes a request for a storage cycle. It is presumed that the IOCE has developed the necessary address and makes the storage request at box 1.

If the IOCE is configured to listen to the selected SE, and the selected SE is configured to listen to the requesting CE, then a response to this request will be returned to the IOCE, (assuming power is up on the SE). A period of one μs nominal, referred to as 1 μs timedown, is allowed for this request-response completion. Box 2 indicates this.

Assuming this response is returned to the IOCE within one μs, (No exit from box 2), then the IOCE will wait for a maximum of 16 μs for the SE to honor its request for a storage cycle. This is referred to as a 16 μs timedown. This period is a convenient interval which is greater than the time that any IOCE should have to wait for a storage cycle due to its high place on the priority chain. If the request is honored within the 16 μs interval (No exit from box 3), then a normal storage access is obtained at box 19.

If no response to the access request is received (Yes exit from box 2), then the IOCE checks to see if a PSBAR reference was being made at box 4. If the PSA is not being referenced (No exit from box 4), then the IOCE will ascertain whether or not the SE reference was made as part of an I/O instruction at box

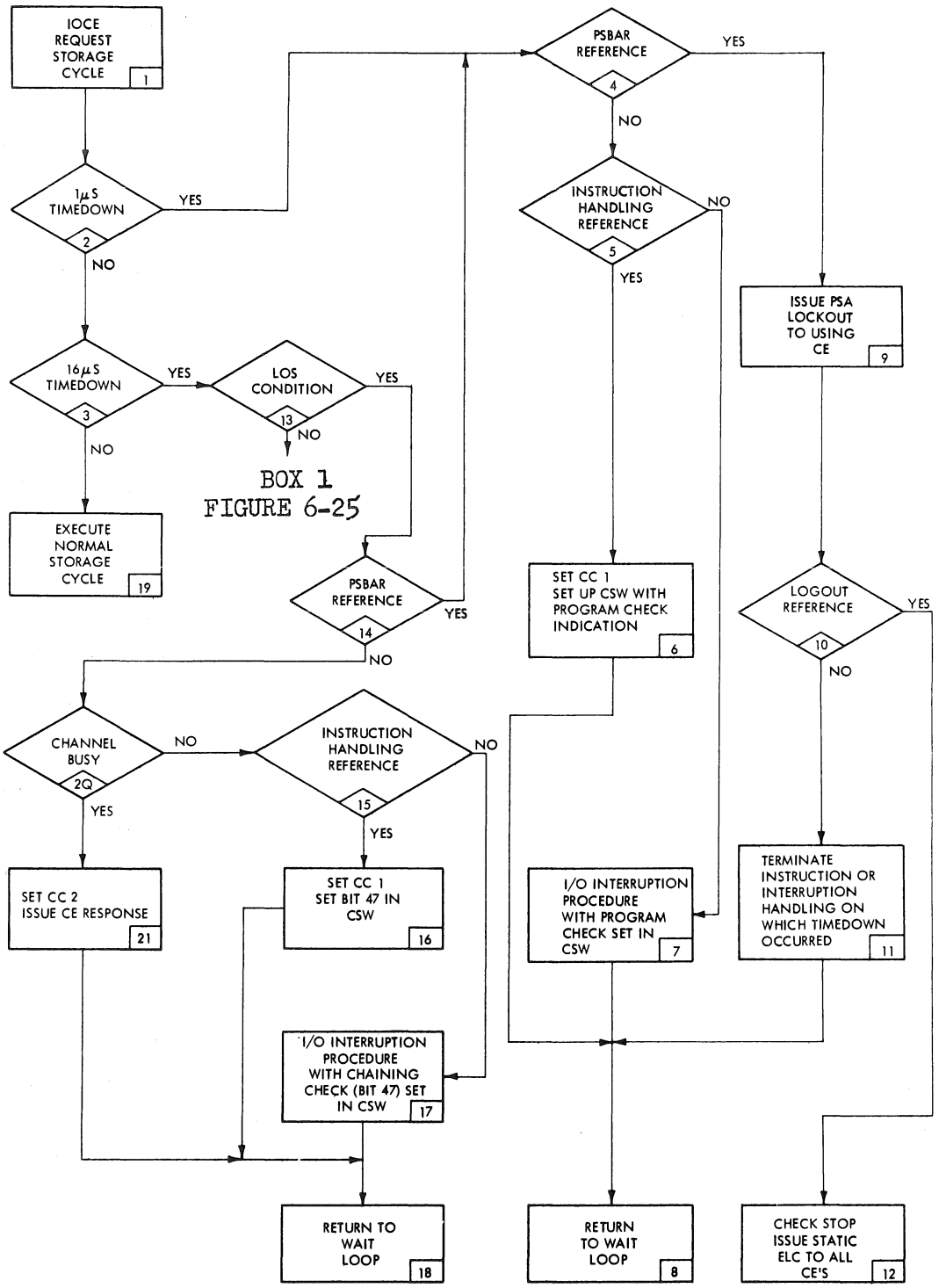


Figure 6-23. Response Type Error Handling for IOCE-SE Accesses.

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5. If an instruction is in progress (Yes exit from box 5), then the IOCE will set condition code 1 and set up a CSW with a program check indication at box 6. It will then return to the wait loop, i.e., revert to waiting for further instructions or data handling requests at box 8. If an instruction is not in process (No exit from box 5), then the reference was for a normal data transfer cycle. The IOCE will cause the usual invalid address indication to be returned to the channel. At such time, then, as the channel signals an I/O interruption because of this (box 7), a program check will be set in the CSW. The IOCE will go to the wait loop until the occurrence of the interruption. This is the usual method of operation when a device presents an invalid address to the IOCE for storage access.

If the addressed location was a PSBAR reference (Yes exit from box 4), then the IOCE will present a PSA lockout signal (box 9) to the using CE. This will cause a program interruption in the using CE, which can respond with a new PSBAR setting, if it desires. If the IOCE is doing a logout (Yes exit from box 10), then it will come to a stop and issue a static ELC to all CEs (box 12). If the CE which is controlling the IOCE wishes to have it resume logout, it must issue a logout to the IOCE presumably after changing PSBAR. In this event, logout will be restarted from the beginning in the alternate PSA. There will be, in general, no problem reconstructing the logout formats since the CE has been notified by the PSA lockout signal that a "split logout" is going to take place, and the logout contents will be available to deduce what has happened in detail.

If no logout is in progress (No exit from box 10), the IOCE will terminate the instruction or interruption handling on which the time down occurred (box 11). It returns to the wait loop at box 8. The I/O interruption will be lost and is not recoverable. If an I/O instruction is in progress, the CE will set condition code 3.

If the IOCE is not able to obtain a storage access within 16 μs (Yes exit from box 3), it assumes that there has been either an equipment malfunction or that it has attempted to reference an SE which was stopped for logout. It determines

at box 13 whether or not the SE was stopped. If not, (No exit from box 13), then it assumes an error. The logic then goes to the IOCE error handling procedures on Fig. 6-24.

If the SE was stopped (Yes exit from box 13), then the IOCE determines whether or not a PSBAR reference was in progress at box 14. If so (Yes exit from box 14), then the IOCE proceeds to the logic previously described at box 4. (There will, in this case, be a Yes exit from box 4). If no PSBAR reference (No exit from box 14), then it is ascertained whether or not the channel is busy (box 20). If it was (Yes exit from box 20), then at box 21 condition code 2 is set and a response is issued to the CE. The IOCE then returns to the wait loop. If the channel is not busy (No exit from box 20), then it is ascertained whether or not an instruction was being executed at box 15. If it was, (Yes exit from box 15), then at box 16 condition code 1 is set, and a CSW is stored with a chaining check indication. It will then go to the wait loop at box 18. If no instruction is in progress (No exit from box 15), then the same I/O interruption actions will be taken as discussed under box 7, except that the CSW will be set with the chaining check bit. The IOCE will then return to the wait loop.

3. Computing Element Malfunctions

The CE's actions in the event it detects an error in its internal hardware or is notified that the SE with which it is working has a malfunction are depicted on Fig. 6-24.

The action on Fig. 6-24 can be initiated by either the detection of a CE error (box 1), the occurrence of a storage check from an SE (box 19), a logout request from another CE via a Write Direct (box 21), or a signal from the CE Logout pushbutton (box 20). These signals are recovered in the CE's check registers (box 2). A decision as to whether or not machine check interruptions are masked is made at box 3. If machine check is masked (No exit from box 3), then a pulse ELC is issued (box 4) and normal processing is continued. The masked interruption will remain pending. If machine check is not masked (Yes

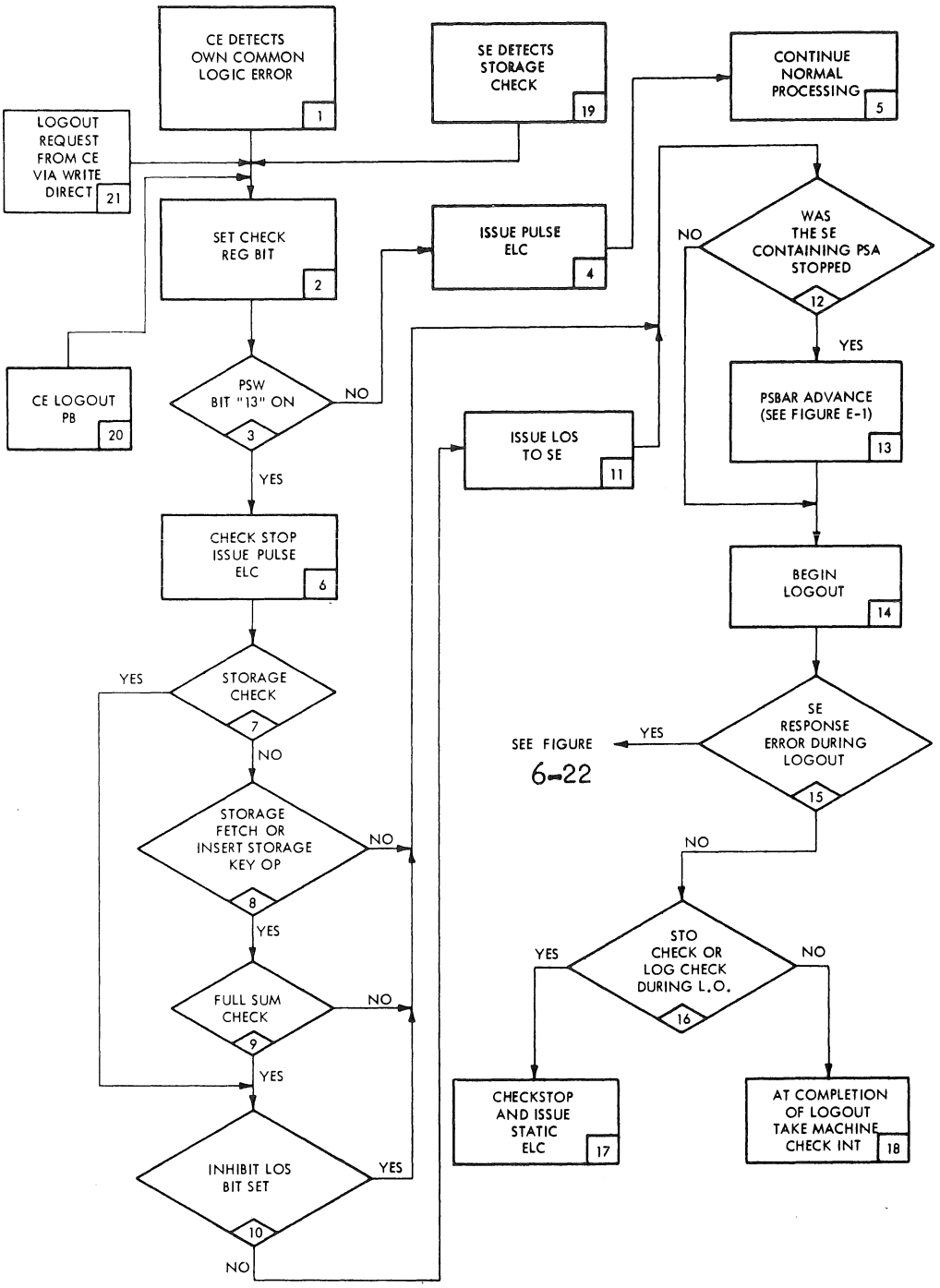


Figure 6-24. CE Error Handling.

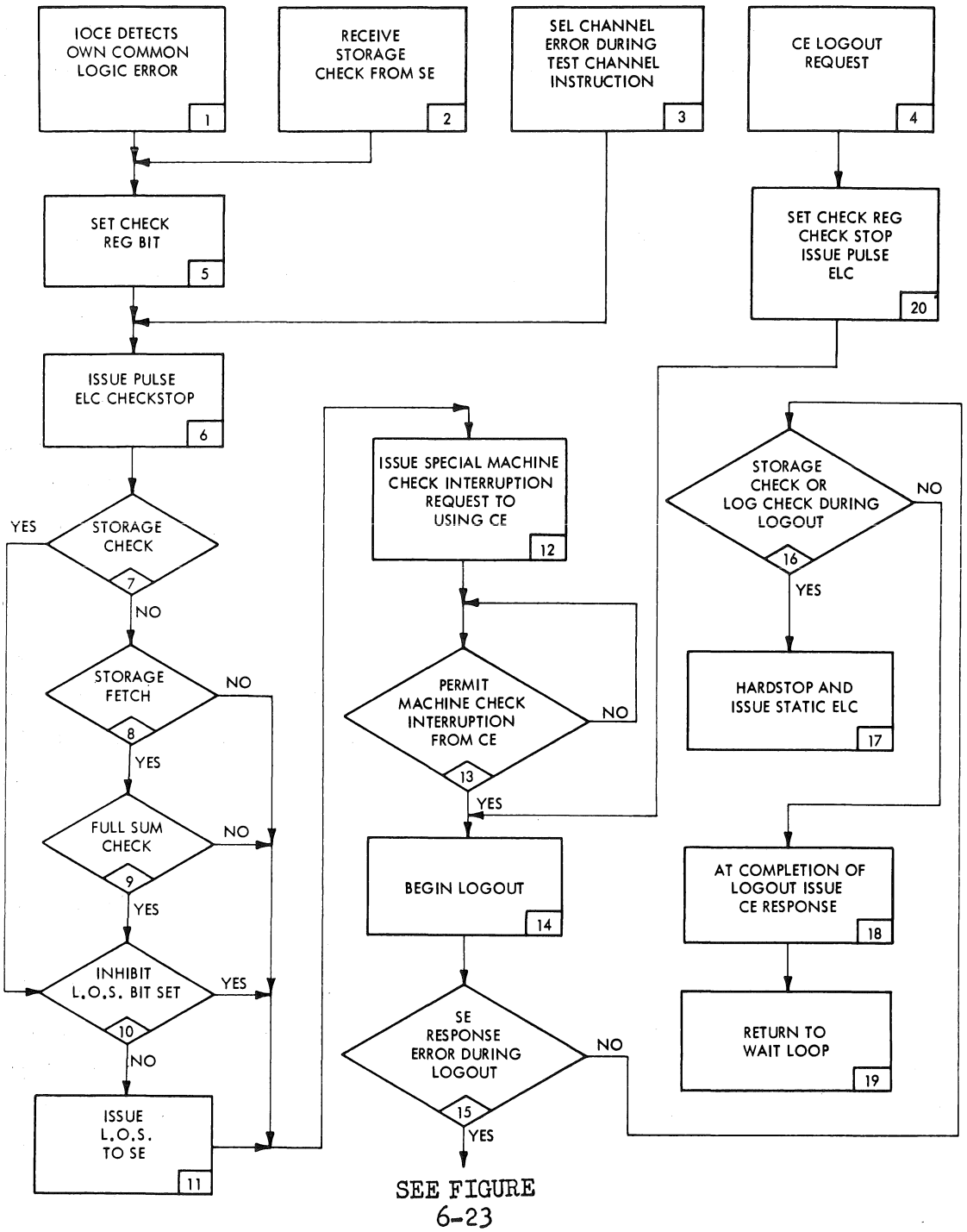


Figure 6-25. IOCE Error Handling for Common Logic Errors.

exit from box 3) then a check stop will occur and a pulse ELC is issued (box 6). This check stop is not actually a true stop in the sense that the CE does not continue to operate. Rather, check stop indicates that execution of the current stored program is discontinued, and the CEs internal controls begin the necessary actions required to perform logout and begin the machine check interruption program.

Boxes 7, 8, 9, 10, and 11 indicate the logic flow necessary to determine whether or not the SE with which the CE is currently working should be stopped for logout, i.e., whether the logout stop (LOS) signal should be issued.

If a storage check is present in the check register (Yes exit from box 7) then the LOS inhibit bit in the CCR is interrogated at box 10. If it is not set (No exit from box 10), then LOS is issued to the SE at box 11 and the CE proceeds to determine at box 12 whether or not the initial logout should be to the primary or alternate PSA.

If there is no storage check register (No exit from box 7), a check is made at box 8 to determine if the CE was executing a fetch or insert storage key operation. Either of these would cause data to be read into the CE from the SE, with the attendant possibility of an interface error which could not be detected by the SE. If neither of these was being done (No exit from box 8), then the SE will not be stopped and the logic proceeds to box 12. If one of these operations was being performed (Yes exit from box 8), then the check register is interrogated at box 9 to determine if the error was a full sum check from the adder. This is the earliest check on input data from the SE and it is here than an interface error would be signaled. If the error was not a full sum check (No exit from box 9), then it is assumed that the input data from the SE is valid and the SE will not be stopped. Logic proceeds to box 12. If a full sum check is present (Yes exit from box 9), then the SE will be stopped for logout unless inhibited. This is again decided via boxes 10 and 11.

At box 12, the CE determine whether the PSA is contained in the SE which was (perhaps) stopped. This is done to preclude the CEs having to wait up to 32 ms before a timedown signal occurs and causes a step to an alternate PSA (see Fig. 6-22 for details). If the SE which was stopped by this CE contains the PSA (Yes exit from box 12) then the PSBAR is stepped to the alternate PSA (see Fig. 6-22 for details) and logout is started at box 14. If the PSA is not contained in the SE which was stopped by this CE or if the Inhibit LOS bit was on, (No exit from box 12), then logout begins immediately at box 14.

Should the CE be unable to get a storage cycle during logout (Yes exit from box 15), the resultant actions are as shown on Fig. 6-22. At box 16 is the schematic indication that a storage check or log check (error in Read Only Storage) during logout (Yes exit from box 16) will cause the CE to stop and issue a static ELC (box 17). When this stop occurs, the CE will respond only to an external start from another CE, a logout signal from another CE, a SCON instruction, or IPL. If neither of the two types of errors occur (No exit from box 16), then the CE will proceed to take a machine check interruption at box 18.

4. IOCE Malfunctions

a. Common Logic Unit

Figure 6-25 depicts the action taken by an IOCE upon the detection of an error in its own equipment, a storage check from the SE with which it is working, a selector channel error during the Test channel instruction, or when it is instructed to logout by a CE.

Assume the IOCE detects an error in its common logic (box 1) or receives a storage check from the SE with which it is working (box 2). The necessary bit is set in the check-register (box 5) and a pulse ELC is issued to all CEs at box 6. If a selector channel error during the test channel instruction occurs (box 3), it enters the logic at box 6 by issuing a pulse ELC and executing a checkstop. No check bit is set since logout data will indicate that the selector channel error occurred.

At box 7, a determination of whether or not to stop the SE with which the IOCE is working is begun. If a storage check had occurred (Yes exit from box 7), then a check is made at box 10 to determine if the inhibit logout stop bit is set. If not (No exit from box 10), then a logout stop (LOS) signal is sent to the SE at box 11.

If there was no storage check (No exit from box 7), then a check is made to see whether the IOCE was fetching data from the storage element. This is done to enable the IOCE to stop the SE if the error occurred at the data input point, since an interface error could have occurred. If not (No exit from box 8), the IOCE will proceed to initiate the necessary action for logout at box 12. If a fetch was in progress (Yes exit from box 8), then at box 9 a check is made to see whether or not the error was a full sum check, which is the malfunction to be expected if an interface error had occurred. If there was a full sum check (Yes exit from box 9), then the IOCE checks the LOS inhibit bit at box 10 to determine whether or not it is permitted to issue a LOS to the SE. If no full sum check had occurred (No exit from box 9), then the logic proceeds to box 12.

At box 12, the IOCE begins the sequence of actions which will result in a logout. The IOCE issues a request for a machine check interruption to the controlling CE. This machine check interruption differs from the normal one in the CE in that the CE will not perform a logout, will honor it only at the completion of the current instruction, and will result in an interruption code in the old PSW as follows:

0000	0000	0001	IOCE 1
0000	0000	0010	IOCE 2
0000	0000	0011	IOCE 3

This machine check interruption is masked by PSW bit 13 in the CE.

Box 13 indicates that the IOCE will wait until the CE honors its request before beginning its logout at box 15.

Should an SE response error occur during logout; i.e., the IOCE cannot obtain a storage cycle (Yes exit from box 15), it will proceed as shown on Fig. 6-23.

Box 16 indicates that account is taken of errors which could occur during the logout. These errors are storage check or a log check (read only storage error). If one of these occurs (Yes exit from box 16), the IOCE will come to a check stop and issue a static ELC to all CEs. It will not resume operation until an external signal is received. This could be a signal from a CE requesting the IOCE to attempt logout again, or a reset as a result of IPL. The IOCE will respond to SCON instructions while in the check stop.

If no error occurred during the logout, the IOCE will respond to the CE to clear the interruption hold and return its normal operation (wait loop).

Box 4 at the top of Fig. 6-24 shows that if an IOCE receives a logout signal from a CE, it will enter the checkstop mode at box 20. It will set the proper bit in the check register to indicate what has occurred and will issue a pulse ELC. It then proceeds to box 14 to initiate the logout sequence.

b. Selector Channel

Figure 6-26 shows the IOCE actions when an error is detected in a selector channel. This sequence of actions differs from the usual IOCE logout primarily in that logout is handled via an I/O interruption and is interleaved with the IOCE's normal operation, causing no interruption in IOCE service on the non-failing channels.

At box 1, the IOCE detects a selector channel error. At box 1a, a check is made to determine if the error was a channel data check. If it was (Yes exit for box 1a), then the parity is corrected (for inputs bytes only), the check condition is recorded and command chaining is suppressed (Box 15). The IOCE then resumes the I/O Operation (box 16). If the error was not a data check (No exit from box 1a), then the IOCE issues a pulse ELC to all CEs and terminates the channel operation at box 2. At box 3, a check is made to see if

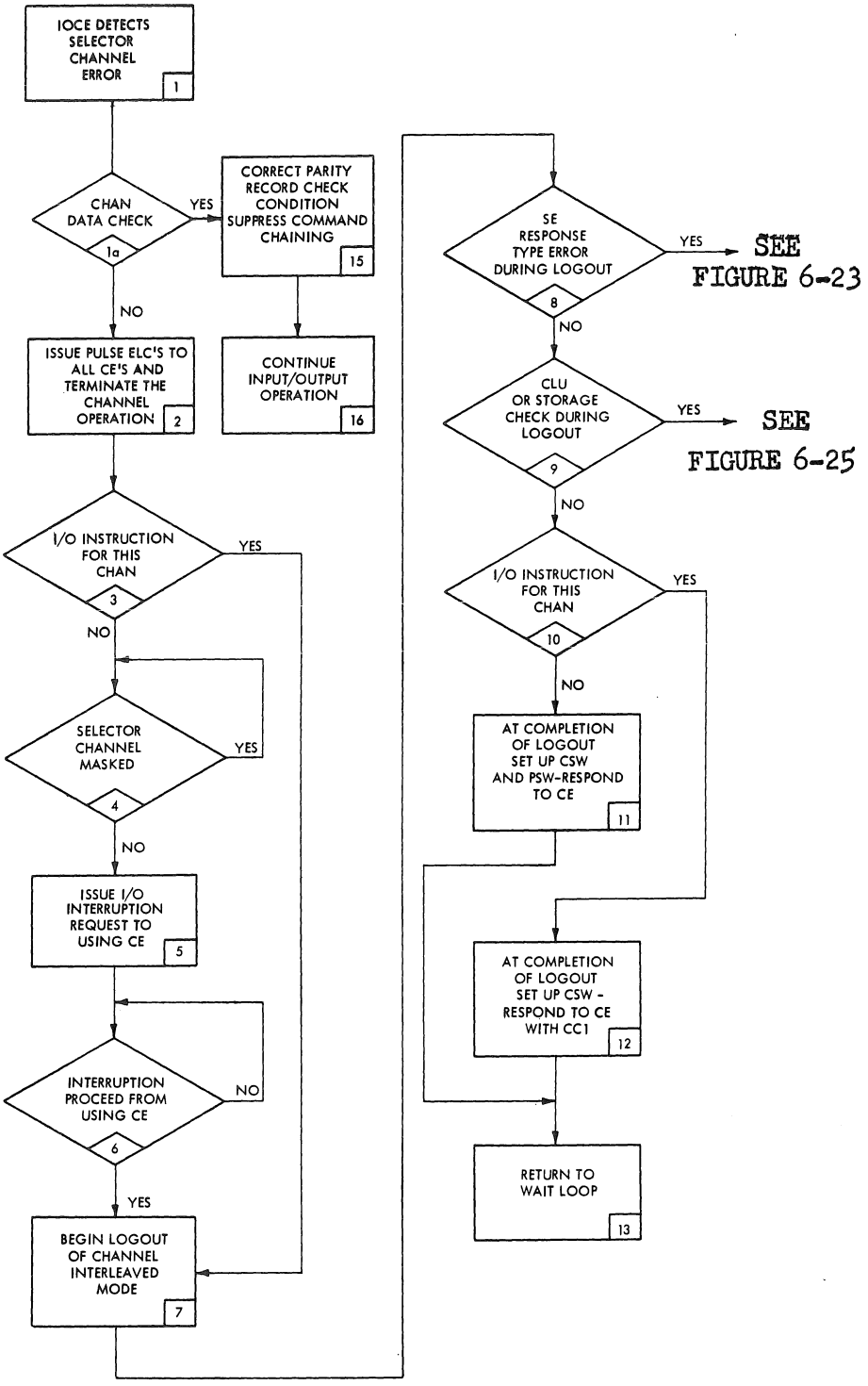


Figure 6-26. IOCE Error Handling for Selection Channel Errors.

there is currently an I/O instruction in process for that channel (except Test channel). If there is (Yes exit from box 3), then the CE is waiting for its completion and a PSBAR setting is already available to the IOCE. The logic then proceeds directly to the beginning of logout at box 7. If there is no I/O instruction in progress for that channel (No exit from box 3), the mask is checked at box 4. If the channel is masked, the interruption request will wait (Yes exit from box 4). If the channel is not masked (No exit from box 4), then an I/O interruption request is made to the CE at box 5. Box 6 indicates that the channel will wait until the CE responds with a proceed signal, at which time it will begin the channel logout at box 7. The interleaved mode indicates that the IOCE will service the selector channel for logout along with the other channels' normal requests.

Boxes 8 and 9 indicate that account is taken of the IOCE's failure to get a storage cycle or an error during logout. If a common logic unit error or a storage check occur during the logout, the IOCE will check stop and issue a static ELC to all CEs.

When the logout is complete, the IOCE will take alternate actions depending on whether or not an I/O instruction was in progress when the malfunction occurred. If an I/O instruction was in progress (Yes exit from box 10), a CSW will be stored indicating logout has occurred, and condition code 1 will be set in the CE and a response sent to the CE to clear the instruction hold. If no I/O instruction was in progress (No exit from box 10), the IOCE will set up a CSW and set the I/O interruption code in the PSW. The response will be sent to the CE to clear the interruption hold.

At the conclusion of either of these terminal operations, the IOCE will return to the wait loop.

5. Storage Element Malfunctions

Figure 6-27 depicts the SE actions when it detects an error in its internal logic or parity or address error. This type of error is detected at box 1.

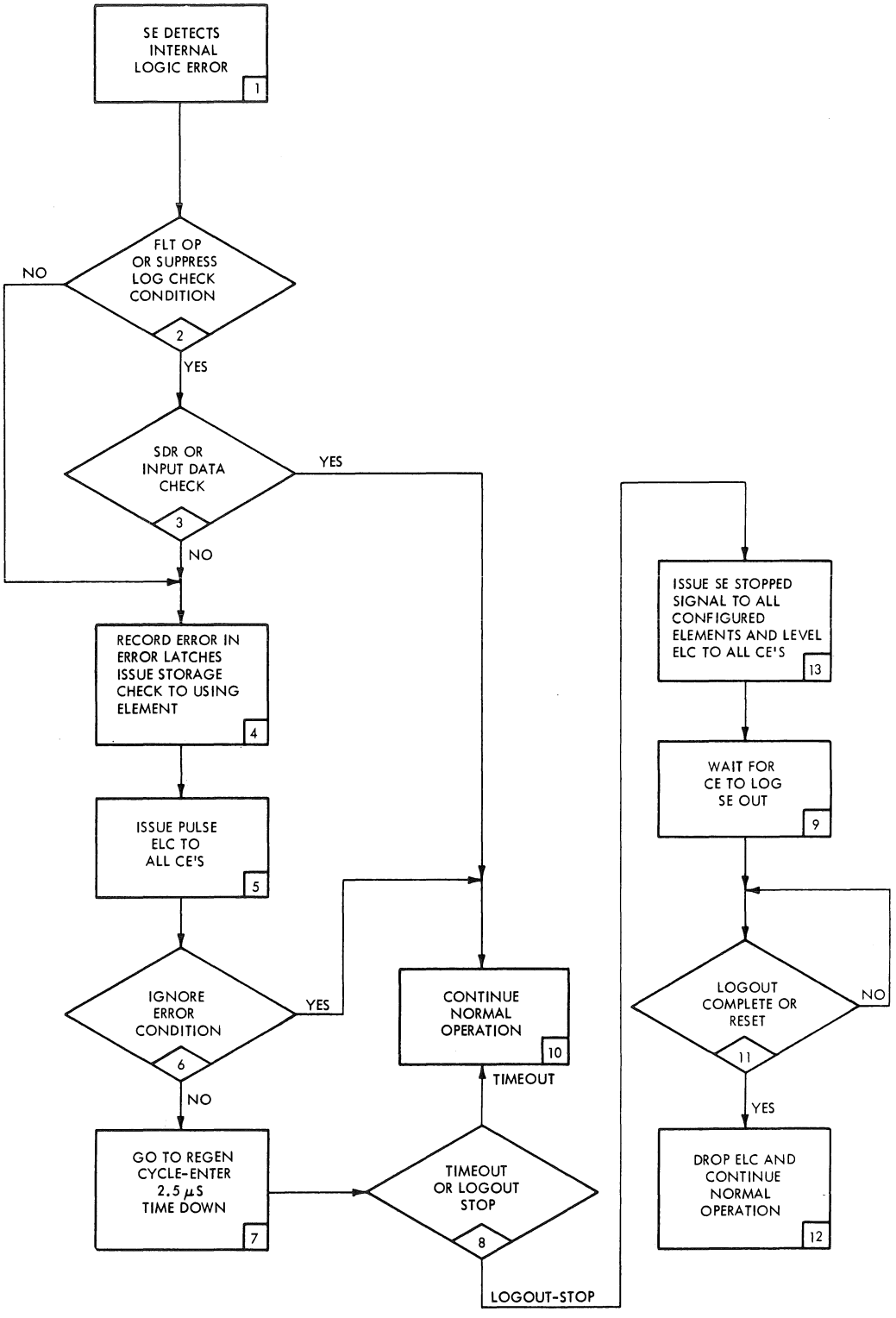


Figure 6-27. SE Error Handling.

Boxes 2 and 3 denote the control conditions which can cause the suppression or recording of errors under various conditions. If the FLT OP or SUPPRESS LOG CHECK lines are not up (No exit from box 3), then the error is recorded at box 4 and a storage check is issued at box 4. If FLT OP or SUPPRESS LOG CHECK is up, (Yes exit from box 2), then SDR or input data checks will be ignored. If one of these occurs (Yes exit from box 3), then the SE continues normal operation at box 10. If neither of these has occurred (i.e., some other error was originally detected), then the error is recorded at box 4 (No exit from box 3), and a storage check is issued. The SE then issues a pulse ELC to all CEs (box 5).

At box 6, the SE determines if the IGNORE ERROR line is up. If so (Yes exit from box 6), the SE will proceed to box 10 as though no error had occurred at box 10. If this line is not up (No exit from box 6), the SE will regenerate the word which was read out of storage (box 7), i.e., if a store operation was in progress, it will not be executed. The SE will then wait for 2.5 μs before honoring any further requests for service to permit the using element to stop it for logout if desired.

At box 8, the SE determines if it should stop or proceed. If the 2.5 μs period elapses without receipt of a logout stop (Timeout exit from box 6), the SE will proceed with its normal operation. If a logout stop signal is received from a using element (Logout Stop exit from box 8), then the SE will stop and honor no further requests for storage cycles. When the SE stops for logout, it issues an "SE Stopped" signal to all configured elements and a level ELC to all CEs (box 13). At box 9, it is indicated that the SE will wait for logout. It cannot proceed with regular operations unless it is given a Logout Complete signal from a CE or is reset. This is shown at box 11. The SE will respond to the SCON instruction while stopped. Upon receipt of Logout Complete or a reset (Yes exit from box 11), the SE will drop the ELC line and resume normal operation.

6. TCU Malfunctions

Figure 6-28 depicts the malfunction reporting actions taken by the TCU when it detects a check condition (Start 0), a CCR Bad Parity Condition (Start 10), or a temperature Out of Tolerance Condition (Start 20). In all cases, there are three primary actions that must take place to complete the reporting of a detected malfunction:

I. Identify the malfunction and set appropriate indicator.

II. Inform the program through the channel equipment or the system monitoring equipment that a malfunction has occurred.

III. Supply malfunction identification to the channel equipment.

Check Condition Reporting -- (Start 0) At block 1, the TCU equipment detects a check condition during the execution of a command, identifies the condition, stores this information in the appropriate Sense Register Indicator at block 4 (Action I), and sets the Unit Check Indicator in the Status Register at block 5. The operation in progress is not stopped at this point but is allowed to continue to its normal conclusion at block 31. At block 32, the TCU now attempts to inform the channel that a malfunction has been detected by presenting the Status information having the Unit Check Indicator set. At blocks 34, 35, and 36, the IOCE, when able, elects to receive the Status information, either through the I/O interruption facilities (Yes exit, block 34) or by use of the Test I/O command (Yes exit, block 36). At block 37, the TCU transfers the Status Register contents indicating Unit Check which was set at block 5, to the IOCE channel (Action II). Having transferred the Status information, the TCU at block 38 resets the Status Register. As a consequence of receiving the Unit Check bit, it is expected that the program will request details of the malfunction by issuing a Sense Command as indicated at blocks 41, 42, 43, and the Yes exit of block 44. As a result, at block 45 the TCU will transfer the Sense data to the IOCE channel (Action III) for analysis and subsequent appropriate action. Back at block 44, following the No exit, the decision at block 46 is significant. If the Command to be executed is Test I/O or I/O No-Op, the accumulated Sense information is

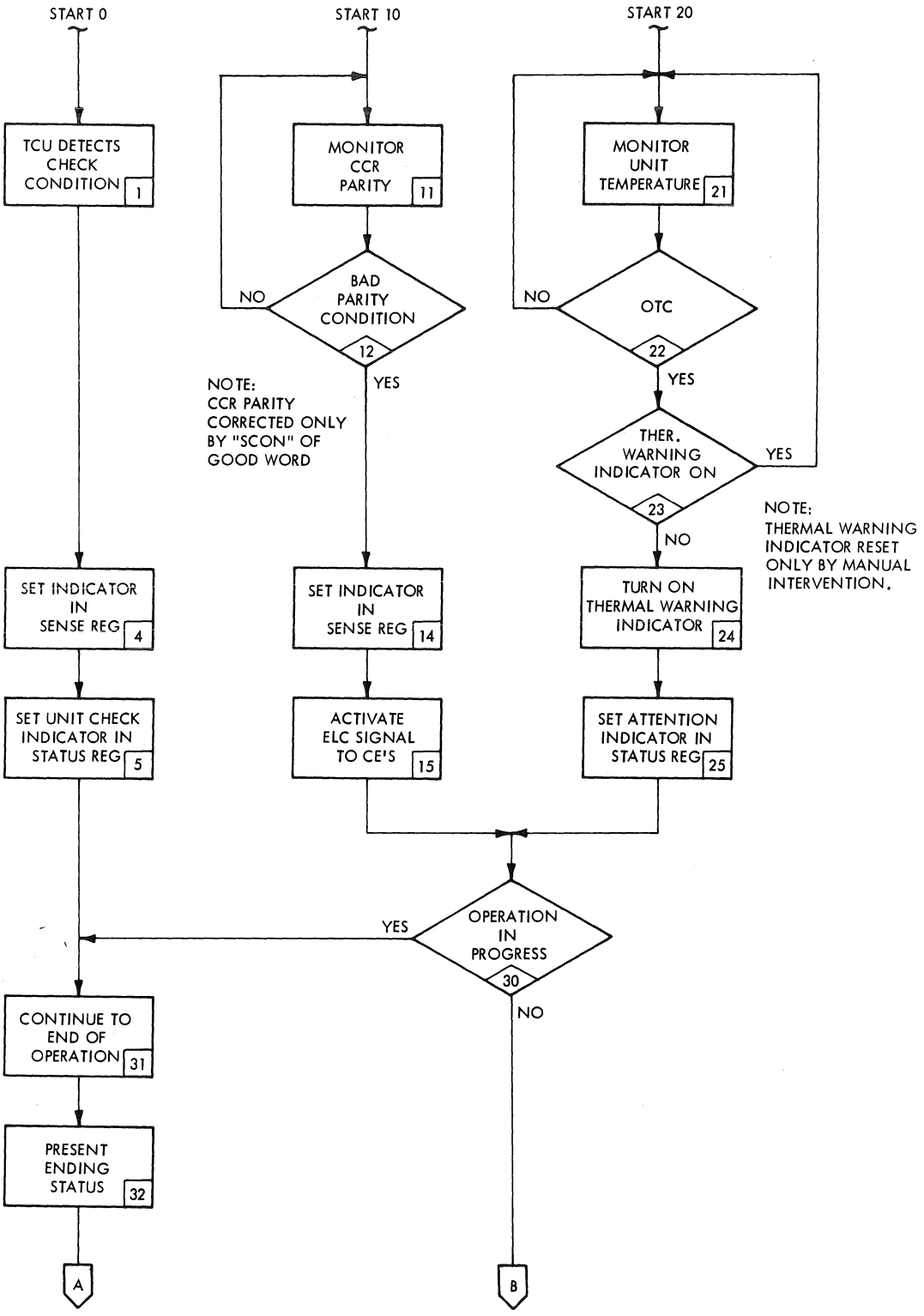


Figure 6-28. TCU Error Handling (Sheet 1 of 2).

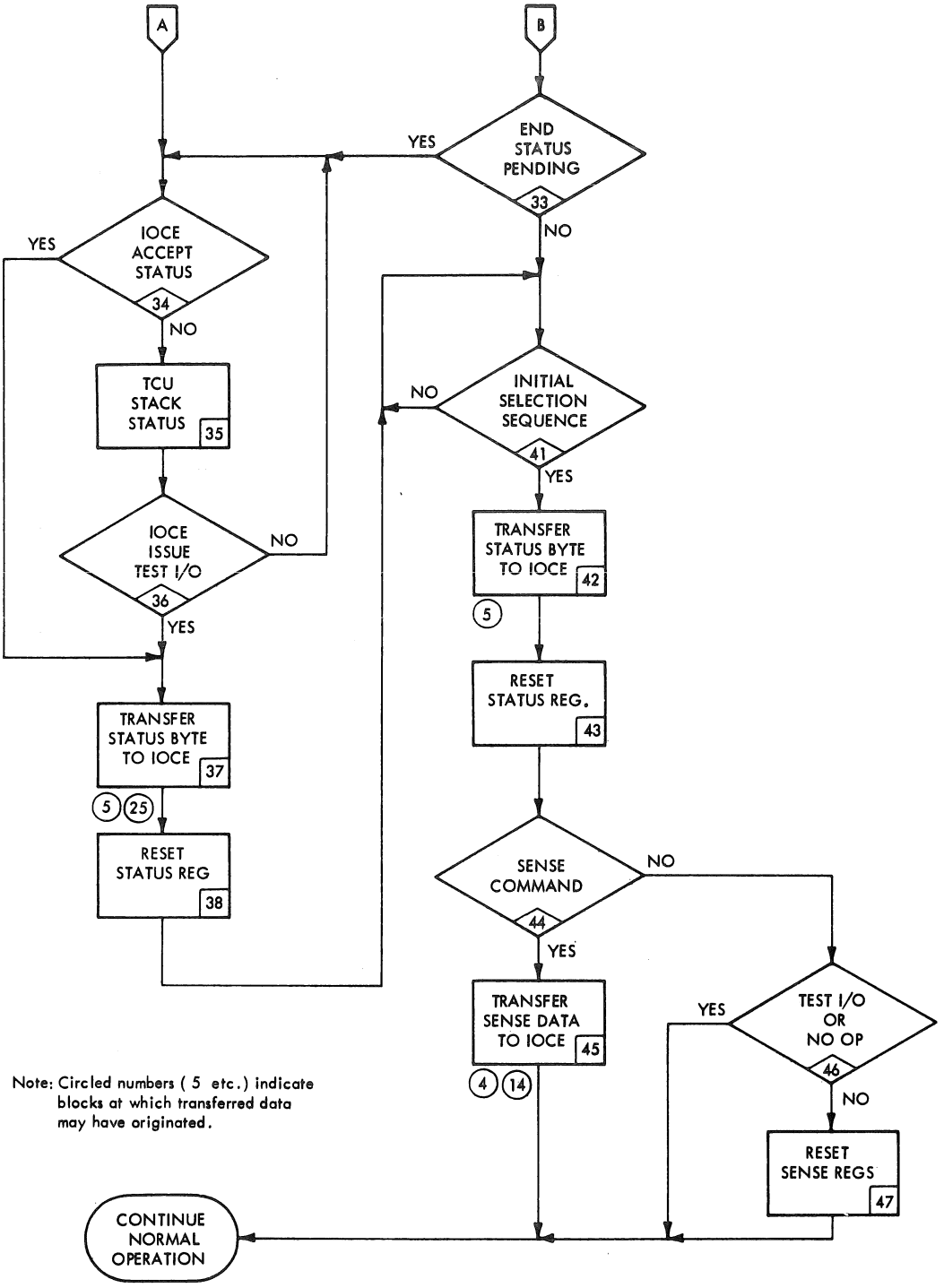


Figure 6-28. TCU Error Handling (Sheet 2 of 2).

retained and still available to the program through a subsequent Sense operation. However, if the exit from block 46 is No, indicating that a new tape operation is to be performed, the Sense Registers are reset at block 47 and the detail malfunction information contained therein is lost.

CCR Bad Parity Condition Reporting -- (Start 10) At blocks 11 and 12, the TCU continuously monitors the CCR for a Bad Parity condition. When it detects this condition, it stores this fact in the appropriate Sense Register Indicator at block 14 (Action I) and activates the ELC Signal to system monitoring equipment in all CEs (Action II). This signal will be held on as long as the Bad Parity condition exists. The condition may be corrected only by performing a SCON operation to replace the contents of the CCR with data having proper parity. The exit options from blocks 30 and 33 have little significance, except to indicate the alternate paths which are followed under varying conditions of operation activity to culminate in the availability of the Sense Indicator information (Action III) through blocks 41, 42, 43, 44, and 45.

Out of Tolerance Condition Reporting -- (Start 20) At blocks 21 and 22, the TCU continuously monitors the thermal sensing equipment for an out of tolerance condition. When it detects this condition it determines, at block 23, whether the Thermal Warning Indicator is presently on. If the indicator is not on, the TCU will turn on the visual Thermal Warning Indicator at block 24 (Action I) and will set the Attention Indicator in the Status Register at block 25. If at block 30 it is determined that there is an operation in progress, the path to block 31 will be taken and the operation will continue to its normal end. At blocks 32, 34, 35, 36, and ultimately block 37, the TCU transfers the Status Register contents indicating Attention which was set at block 25, to the IOCE channel (Action II) and then resets the Status Register at block 38. Because the Attention Indicator is unique to OTC in the TCU, the malfunction requires no further identification and Action III has been effected without the need for a Sense Operation. Back at block 30, if no operation is in progress, the No exit to block 33 is followed where it is determined whether the Ending Status from the previous operation has been accepted. If End Status is pending, the "Accept status loop" is entered at block 34 and the

Attention Status indicator is transferred to the IOCE channel at block 38 as before. The No exit from block 33 enters a new operation at block 41. At the conclusion of the Initial Selection Sequence for the new operation, the Attention Status indicator will be included in the Status Byte transferred to the IOCE at block 42 and is reset at block 43. Since in every case the Status Register is reset after its contents are transferred to the channel (blocks 38 and 43), the Attention Status Indicator is presented once only for any one occurrence of OTC. An attempt to manually reset the Thermal Warning Indicator before the OTC is corrected will cause the Attention Status Indicator to be set again.

7. PAM Malfunctions

a. PAM Common

Figure 6-29 depicts the action taken by PAM Common when it detects an error in its internal logic, or an out-of-tolerance condition (OTC). The sequence of actions does not apply to the case where PAM Common detects a parity error on an address from the multiplexor channel. In this case, PAM sets a sense bit in the Test and Monitor (TAM) adapter and does not respond to the address. It does not set the Attention bit. Errors occurring when the TAM adapter is the addressed unit (Bus Out Check or Command Reject) are covered under adapter malfunction handling.

At box 1, PAM Common detects the logic error or OTC. At box 2, the appropriate bit or bits are set in the TAM adapter's sense register, bytes 2 or 3. Box 3 denotes two check conditions which cause Element Check (ELC). If the check condition was caused by a CCR parity (Configuration Check) or Check Stop (check condition in the priority circuitry), the Yes exit is made to block 4. The ELC line is then raised to all CEs. ELC remains static until the condition causing it is cleared. After setting ELC or if neither above condition was detected (No exit from block 3), the Attention status bit is set at block 5 and presented to the channel. No further action takes place until the IOCE accepts the Attention status (Yes exit from block 6) or issues TEST I/O to the TAM adapter (No exit from block 6 and Yes exit from block 7).

After accepting Attention, the program can issue the Sense command to the TAM adapter (Yes exit from block 8) to obtain information regarding the cause of the Attention status. If the Check Stop bit is not set (No exit from block 9) the program may try to continue I/O operations. A solid check condition will result in starting at block 1 again. If the Check Stop bit was set (Yes exit from block 9), the cause of Check Stop is indicated in four other sense bits and may be examined. The program may then issue the Bypass Check Stop command (Yes exit from block 10) which will clear the Check Stop latch allowing the next priority scan to begin. Clearing the Check Stop latch also clears the ELC line at block 11. If the cause of Check Stop was intermittent, the program will be able to continue with I/O operations in PAM (Block 12). If the cause of Check Stop is solid, the cycle begins again at block 1.

If the Sense command is not issued (No exit from block 8), or if issued and Check Stop is present and not cleared by the Bypass Check Stop command (No exit from block 10), the I/O operations in PAM will stop at the respective blocks.

b. PAM Adapters

Figure 6-30 depicts the actions taken by PAM adapters when a check condition is detected by the adapter. Check conditions can result from other than logic errors in the adapter; i.e., they may also be caused by errors in data transmission from the channel or device, by conditions reported by the device through its control lines, or by failure of the channel to service an adapter in a particular period of time.

In block 1 the adapter detects a check condition and sets the associated bit in its sense register (block 2). If initial selection is in progress (Yes exit from block 3), the I/O operation is not performed and the adapter presents status to the channel with Unit Check in response to the command (Block 6).

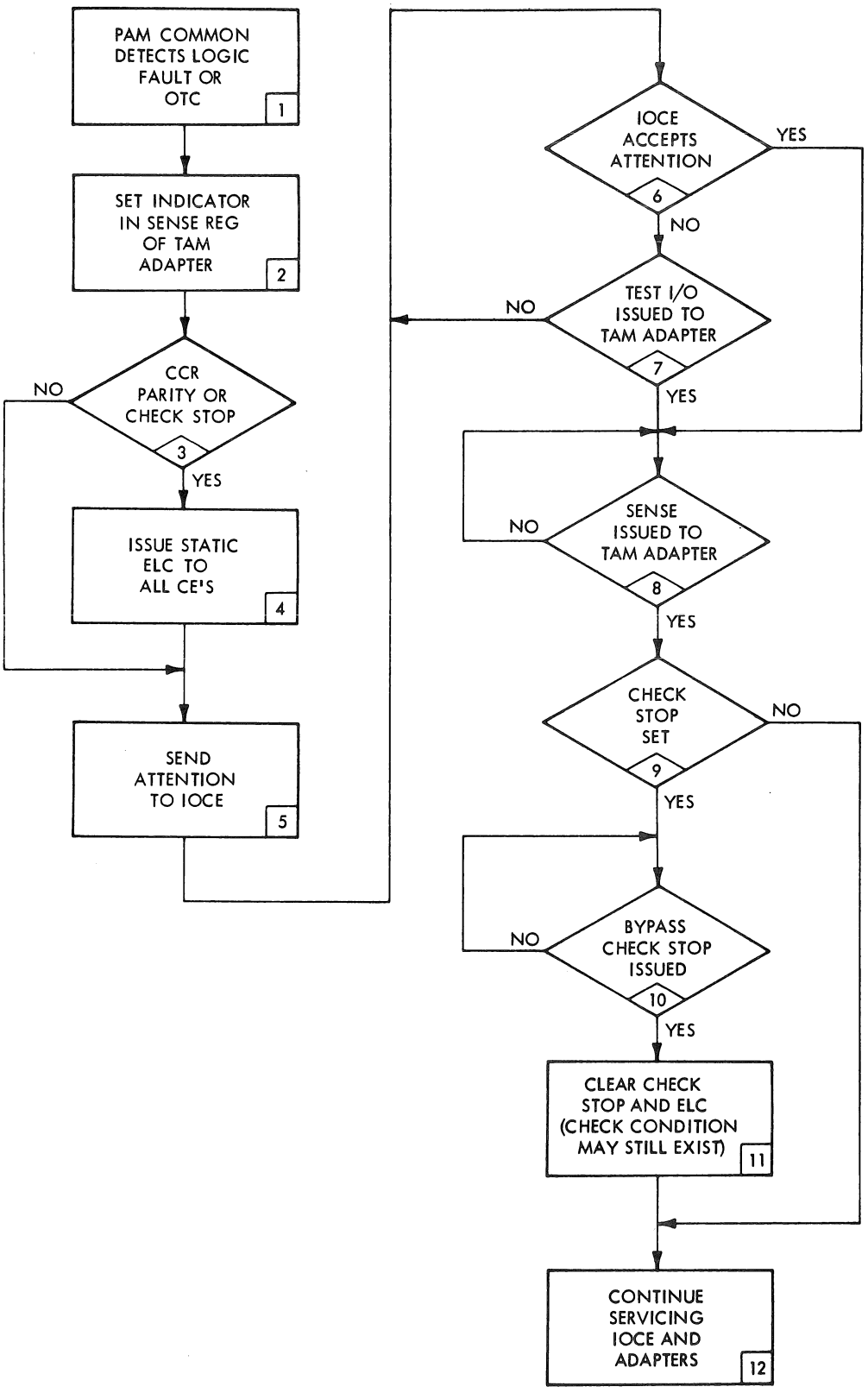
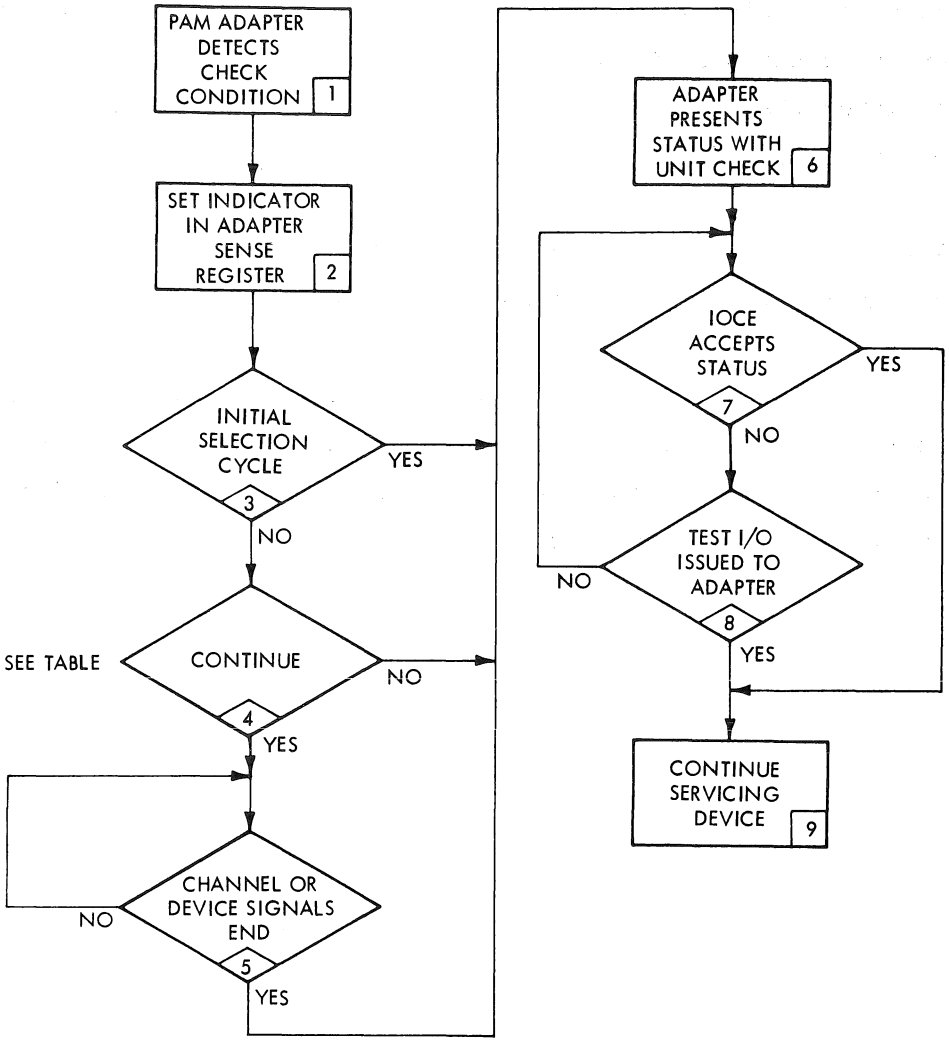


Figure 6-29. PAM Common Error Handling.



	GPI	GPO	INTI	INTO	TTYLL	RVDP	1052	CD	FDEP
BUS OUT CHECK		T		C	C		C		C**
DATA CHECK	C	T	C	C	C				C
EQUIPMENT CHECK			T				C		
OVERRUN			T	T	T			T	T
ECHO CHECK					T				T
LRC			C		C				C
DEVICE INOPERATIVE		T							
DEVICE STATUS 3, 5, 6		T							
DEVICE STATUS 7		*							
INTERVENTION REQ'D							C		T
TIMEOUT									T

T = TERMINATE C = CONTINUE

BLANK - NOT APPLICABLE DURING DATA TRANSFER OPERATIONS
* MAY BE WIRED TO TERMINATE OR CONTINUE
**IN CONTROL MODE, ADAPTER TERMINATES

Figure 6-30. PAM Adapter Error Handling.

If a data transfer operation is in progress (No exit from block 3), the adapter will either terminate the operation immediately (No exit from block 4) or will continue until either the channel or the device signals the end of transmission (Yes exit from block 4 and Yes exit from block 5).

The Table in Fig. 6-30 indicates which adapters will continue and which will terminate data transfer for each applicable check condition.

When the data transfer is terminated, the adapter presents ending status with Unit Check (Block 6). If the IOCE accepts status (Yes exit from block 7) or clears status with a TEST I/O command (Yes exit from block 8), the adapter is free to continue with the next command.