# 2100 SERIES COMPUTER
# FLOATING POINT DIAGNOSTIC

## EXTERNAL REFERENCE SPECIFICATION

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## SCOPE

The purpose of this diagnostic is to test the floating point instruction set for any 2100 series computer.

This diagnostic is of the GO-NOGO type in that it exercises the Floating Point instructions to check that they are working properly. No attempt is made at fault isolation.

The actual Floating Point result is compared with the expected result obtained by a software routine.

This diagnostic assumes the following diagnostics have been successfully executed:

Alter-skip instruction test
Memory reference instruction test
Shift-rotate instruction test
Teleprinter diagnostic
Memory Protect diagnostic
EAU diagnostic

## Required Hardware

The hardware required is a 4K or greater 2100 series computer and a teleprinter. Also required is an EAU.

## Required Software

The required software is the binary object tape and the Diagnostic Configurator (DC).

Location $126_8$ contains the Diagnostic Serial Number (DSN) of the diagnostic being run. The DSN for this diagnostic is $1Ø1ØØ7_8$.

## PROGRAM ORGANIZATION

The diagnostic consists of 7 tests - one for each floating point instruction and one test to test both the memory protect fence and multiple indirect execution of the floating point add.

| TEST | FUNCTION TESTED |
|---|---|
| 1. | Fence and indirect test (if memory protect available) |
| 2. | FAD - Floating add |
| 3. | FSB - Floating subtract |
| 4. | FMP - Floating multiply |
| 5. | FDV - Floating divide |
| 6. | FIX - Fix a floating point number |
| 7. | FLT - Float a fixed point number |

Test 1 will not be performed if memory protect is not available. Normally, each test is exercised in sequence using arguments from a number generator to get the actual results. The same arguments are also used in a software routine to get the expected results. An error is any difference between the actual and the expected results.

## NUMBER GENERATION

At the start of each test, new arguments are generated by an internal random number generator unless switch 6 is on.

## INDIRECT ADDRESSING

A multi-level indirect add test is executed on the first test. One execution of this test is enough to insure that indirects are being handled properly. This test is executed at the beginning of each 1ØØ cycles.

## OV REGISTER CHECKING

At the beginning of each test the overflow register is cleared and the expected OV result is compared to the actual OV result during the test. Any difference will cause an error.

Error Handling

All message data is in octal except for the cycle and error counts. There are two types of messages: error and information.

The information messages include the

1. introductory message
2. end of test message
3. cycles and errors message

The information messages with the exception of the cycle and error message are switch independent. For the cycle and error message switch 11 must be off.

The introduction message is printed only at the start of the diagnostic. The message is:

H1 2100 SERIES FLOATING POINT DIAGNOSTIC

The end message is printed on sensing switch 10 on. The message is:

H4 XXXXX CYCLES WITH YYYYY ERRORS
H5 TEST COMPLETE
H6 FOR RESTART, PUSH RUN

where XXXXX is the number of cycles to 32,767 cycles and YYYYY is the number of errors to 32,767. If 32,767 cycles of errors are exceeded the valus is reset to zero.

The cycles and errors message is printed if switch 9 is on and switch 11 is off. The message is:

H4 XXXXX CYCLES WITH YYYYY ERRORS

Where XXXXX and YYYYY are the same as in the end message. This message can occur after each test if desired.

The error description messages are self describing. They are:

E1 MEMORY PROTECT BOUNDARY TOO HIGH

The above message is printed if switch 11 is off and the floating point hardware modified the memory protect fence value to a higher value. This test is made in the first test:

E2 MEMORY PROTECT BOUNDARY TOO LOW

The above message is printed if switch 11 is off and the floating point hardware modified the memory protect fence value to a lower value. This test is made during the first test.

E3 STORE ON BOUNDARY DID NOT WORK PROPERLY

The above message is printed if switch 11 is off and an attempted store on the memory protect fence did not work but also did not cause a memory protect violation. This test is made during the first test.

E1-E3 will not be printed with no memory protect installed

| | | | | |
|---|---|---|---|---|
| E4 | INDIRECT ADDITION | | | |
| E5 | ADDEND1 | | 123456 | 1Ø21Ø2 |
| E6 | ADDEND2 | | 177777 | Ø2134Ø |
| E7 | EXPECTED | 1 | 177777 | 111111 |
| E8 | ACTUAL | Ø | 177777 | 111111 |

The above message is printed if switch 11 is off and an error occurs in the indirect address type of floating add. The indirect addressing of the second addent need only be tested once to conform that this aspect of the floating point routines are working properly. An error is caused by a difference between the hardware and software results or a difference between the OV registers.

The numbers are in octal and represent a floating point number. The high word represents the left word of the two word floating point number; the low word represents the right word. The overflow bit = Ø means that it was not set on while 1 indicates on.

| | | | | |
|---|---|---|---|---|
| E9 | ADDITION | | | |
| E5 | ADDEND1 | | 123456 | 1Ø21Ø2 |
| E6 | ADDEND2 | | 177777 | Ø2134Ø |
| E7 | EXPECTED | Ø | 177731 | 123456 |
| E8 | ACTUAL | 1 | 143210 | 123456 |

The above message is printed if switch 11 is off and an error has occurred in a floating add test. The meanings of the numbers is the same as for an indirect floating add error. This message is the result of the second or add test.

| | | | |
|---|---|---|---|
| E1Ø | SUBTRACTION | | |
| E11 | MINUEND | 123456 | 154321 |
| E12 | SUBTRAHEND | ØØØ123 | Ø54321 |
| E7 | EXPECTED | Ø 111111 | 111111 |
| E8 | ACTUAL | 1 ØØØØØØ | ØØØØØØ |

The above message is printed during the third or subtraction test when an error occurs and bit 11 of the switch register is off. The numeric meanings of the message are the same as for indirect floating addition errors.

| | | | |
|---|---|---|---|
| E13 | MULTIPLICATION | | |
| E14 | MULTIPLICAND | 123456 | 152433 |
| E15 | MULTIPLIER | Ø12345 | ØØ1ØØØ |
| E7 | EXPECTED | Ø 1Ø123Ø | 123322 |
| E8 | ACTUAL | 1 Ø1Ø32Ø | 112233 |

The above message is printed when switch 11 is off and a multiplication error occurs. This occurs during the fourth test and the meanings of the results are the same as for an indirect floating addition error.

| | | | |
|---|---|---|---|
| E16 | DIVISION | | |
| E17 | DIVIDEND | 144322 | 123331 |
| E18 | DIVISOR | ØØ1111 | ØØ2136 |
| E7 | EXPECTED | Ø 111111 | 111111 |
| E8 | ACTUAL | Ø 111111 | 111112 |

The above message is printed when switch 11 is off and a division error occurs. This occurs during the fifth test and the meanings of the message are the same as those of an indirect floating addition error.

| | | | |
|---|---|---|---|
| E19 | FIX | | |
| E20 | OPERAND | 155555 | 333333 |
| E21 | EXPECTED | 1 123456 | |
| E22 | ACTUAL | Ø 123456 | |

The above message is printed if switch 11 is off and an error occurs in the FIX routine. The number in the results is an octal number representing the value returned in the A register. The other numbers are the same format as for indirect add. This is the sixth test.

| | | | | |
|---|---|---|---|---|
| E23 | FLOAT | | | |
| E24 | OPERAND | | 123321 | |
| E7 | EXPECTED | Ø | 112211 | 125521 |
| E8 | ACTUAL | 1 | 143512 | 161631 |

The above message is printed if switch 11 is off and a FLOAT error is detected. The number to be floated is an octal number representing the number to be floated in core. All other numbers are the same as described for indirect floating addition error. This is the seventh and last test of a cycle.

OPERATING INSTRUCTIONS

1. Use the Binary Loader to load the Diagnostic Configurator (DC) and configure. Then use the Binary Loader to load the diagnostic.

2. Set a starting address of $100_8$.

3. Set the switch register for the desired program options according to Table 1. If all bits of register are off, the program uses a fixed internal switch register which executes all tests. If any bits are set in switch register, that register is used.

4. Press PRESET or INTERNAL, EXTERNAL PRESETS and RUN.
   If bit 12 is set, the program requires ~~1 → 2~~ 2-4 seconds to run.

Table 1

Switch Register Settings

| Switch | Meaning If Set (or on) |
|---|---|
| 0 | Add test will be executed. |
| 1 | Subtract test will be executed. |
| 2 | Multiply test will be executed. |
| 3 | Divide test will be executed. |
| 4 | Fix test will be executed. |
| 5 | Float test will be executed. |
| 6 | New random number will not be generated. |
| 7 | Not used. |
| 8 | Not used. |
| 9 | Display number of cycles and errors. |
| 10 | Terminate program. |
| 11 | Suppress error messages. |
| 12 | Halt at end of 100 cycles. |
| 13 | Loop back to last executed test. |
| 14 | Halt on each error. |
| 15 | Halt after each test. |

NOTE: If switches 0 through 15 are not set, ~~all tests are executed in the normal sequence~~.

the program uses dfault switch register settings. IE Bits 0-5, 12, 14 and 15 will be used.

Table 2

Halt Codes

| HALT | MEANING |
|---|---|
| 102002 | Memory protect did not interrupt on an illegal store operation |
| 102003 | Memory protect interrupted on a store in the fence boundary |
| 102004 | Memory protect did not interrupt on an illegal store operation |
| 102010 | End of first test |
| 102011 | End of floating addition test |
| 102012 | End of floating subtraction test |
| 102013 | End of floating multiplication test |
| 102014 | End of floating division test |
| 102015 | End of FIX test |
| 102016 | End of Float test |
| 102020 | Indirect floating addition error |
| 102021 | Floating add error |
| 102022 | Floating subtract error |
| 102023 | Floating multiply error |
| 102024 | Floating divide error |
| 102025 | Fix error |
| 102026 | Float error |
| 102076 | End of 100 cycles |
| 102077 | End of test |
| 106077 | Unexpected trap cell halt |

HEWLETT hp PACKARD

# SOFTWARE CERTIFICATION TEST REPORT

1. SOFTWARE NAME: FLP

2. VERSION:

3. DATE: 5-17-73

4. SOFTWARE CERTIFICATION CYCLE NUMBER: 1

5. SOFTWARE CERTIFICATION TEST REPORT NUMBER: 1

6. EVALUATOR: LON JOHNSON

7. DESCRIPTION OF TEST RESULTS:

PAR. NO. 3, Page 4 of ERS IS NOT WORKING CORRECTLY. WITH Ø REQ'S SET, PROGRAM ACT. AS IF BIT 15 IS SET AND STOPS AT END OF EACH TEST

8. ACCOMPANYING DOCUMENTATION:

- [ ] OBJECT TAPE/DECK
- [ ] SOURCE TAPE/DECK
- [ ] PROGRAM LISTING
- [ ] CORE DUMP
- [ ] TELETYPE LOG
- [ ] PROGRAM OUTPUT
- [ ] OTHER (Describe below)

(FOLLOWING SECTION TO BE COMPLETED BY PROJECT MANAGER)

9. DESCRIPTION OF ACTION TO BE TAKEN:

Correct if SWR is set to 0's the program will default to an internal bit setting ie 15077

10.

A J Stolz
PROJECT MANAGER SIGNATURE

5-24-73
DATE

HEWLETT hp PACKARD

# SOFTWARE CERTIFICATION TEST REPORT

1. SOFTWARE NAME: F. P.

2. VERSION: ———

3. DATE: 5-28-73

4. SOFTWARE CERTIFICATION CYCLE NUMBER: 1

5. SOFTWARE CERTIFICATION TEST REPORT NUMBER: 2

6. EVALUATOR: D. Delano

7. DESCRIPTION OF TEST RESULTS: SW11 ON and SW 9 on get no message H4 until SW 11 OFF

8. ACCOMPANYING DOCUMENTATION:

- [ ] OBJECT TAPE/DECK
- [ ] SOURCE TAPE/DECK
- [ ] PROGRAM LISTING
- [ ] CORE DUMP
- [ ] TELETYPE LOG
- [ ] PROGRAM OUTPUT
- [ ] OTHER (Describe below)

(FOLLOWING SECTION TO BE COMPLETED BY PROJECT MANAGER)

9. DESCRIPTION OF ACTION TO BE TAKEN:

Correct; will change pgm to put H4 with 11 on

10.

A. J. Stolz
PROJECT MANAGER SIGNATURE

6-4-73
DATE

HEWLETT hp PACKARD

# SOFTWARE CERTIFICATION TEST REPORT

1. SOFTWARE NAME: FP

2. VERSION: _____

3. DATE: 5-28-73

4. SOFTWARE CERTIFICATION CYCLE NUMBER: 1

5. SOFTWARE CERTIFICATION TEST REPORT NUMBER: 3

6. EVALUATOR: D. Delano

7. DESCRIPTION OF TEST RESULTS: E2 printed with SW 11 ON

8. ACCOMPANYING DOCUMENTATION: 210X

- [ ] OBJECT TAPE/DECK
- [ ] SOURCE TAPE/DECK
- [ ] PROGRAM LISTING
- [ ] CORE DUMP
- [ ] TELETYPE LOG
- [ ] PROGRAM OUTPUT
- [ ] OTHER (Describe below)

(FOLLOWING SECTION TO BE COMPLETED BY PROJECT MANAGER)

9. DESCRIPTION OF ACTION TO BE TAKEN:

Will add correction to pgm to fix.

10.

G. J. Stolz
PROJECT MANAGER SIGNATURE

6-4-73
DATE

HEWLETT hp PACKARD

# SOFTWARE CERTIFICATION TEST REPORT

1. SOFTWARE NAME: XFCP1

2. VERSION: ———

3. DATE: 6-16-73

4. SOFTWARE CERTIFICATION CYCLE NUMBER: 1

5. SOFTWARE CERTIFICATION TEST REPORT NUMBER:

6. EVALUATOR: D. DeLano

7. DESCRIPTION OF TEST RESULTS: Message E2 not suppressed by switch 11

```
E2  MEMORY PROTECT BOUNDARY TOO LOW
E2  MEMORY PROTECT BOUNDARY TOO LOW
E2  MEMORY PROTECT BOUNDARY TOO LOW
E2  MEMORY PROTECT BOUNDARY TOO LOW
E2  MEMORY PROTECT BOUNDARY TOO LOW
E2  MEMORY PROTECT BOUNDARY TOO LOW
E2  MEMORY PROTECT BOUNDARY TOO LOW
```

8. ACCOMPANYING DOCUMENTATION:

- [ ] OBJECT TAPE/DECK
- [ ] SOURCE TAPE/DECK
- [ ] PROGRAM LISTING
- [ ] CORE DUMP
- [X] TELETYPE LOG
- [ ] PROGRAM OUTPUT
- [ ] OTHER (Describe below)

(FOLLOWING SECTION TO BE COMPLETED BY PROJECT MANAGER)

9. DESCRIPTION OF ACTION TO BE TAKEN:

Have checked both code and operation and cannot duplicate. The check for this bit being set requires that the EAU instruction RRL [redacted] works correctly. There maybe a problem with this instruction

10.

AJ Ftak
PROJECT MANAGER SIGNATURE

6-18-73
DATE