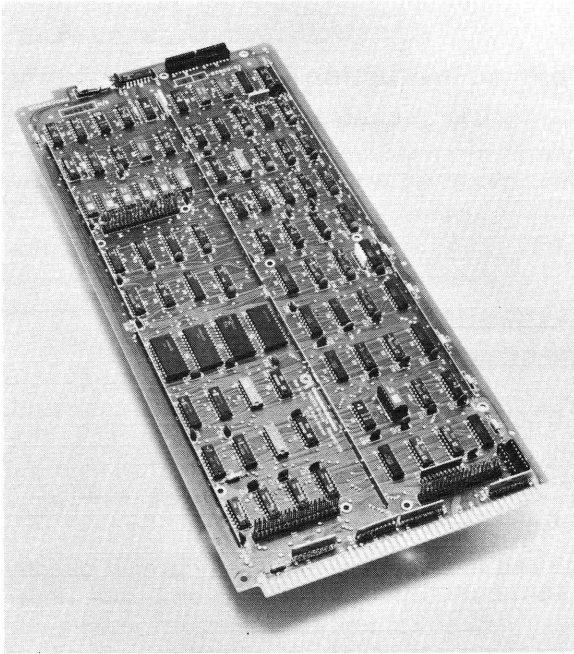# NAKED MILLI

NAKED MILLI BRIDGES MINI-MICRO GAP — Offering upward-compatible flexibility and the most important features of minicomputers, yet priced competitively with micro-computers is Computer Automation's new NAKED MILLI.

MEET THE MILLI

Nature abhors a vacuum. So naturally something eventually comes along to fill it.

In the case of computers, the gap between microcomputers has been so abysmally broad that it fairly begged to be bridged.

So here it is. The millicomputer. A big little processor for a microcomputer price, but a lot more machine for the money.

A more powerful instruction set than you can get with any micro.

Plus a lot more I/O - three standard I/O systems and the new exclusive Distributed I/O System allowing up to 8 interfaces on a single half-size card.

The world's first millicomputer: a new breed of computers designed to be cost effective in many application areas where a microcomputer might otherwise have been used, while providing the power of a mini.

KEEPING PEACE IN THE FAMILY

Naturally, the NAKED MILLI is program compatible with our large family of NAKED MINI® machines. Which instantly gives you a broad choice of memories, interfaces and software. Which also gives you compatible expandability upward through the full range of minicomputer performance.

The NAKED MILLI LSI-3/05 is a single half-card bipolar MSI computer approximately 7" x 15". It is electrically and mechanically interchangeable with the other processors in the LSI family. The LSI-3/05 instruction set is a subset of the instruction sets of the larger machines. All programs written for the LSI-3/05 will run on the largers members of the family. Programs written in the larger instruction sets will run on the LSI-3/05 using software Macros which perform the operations that are not directly implemented in 3/05 hardware.

POWERFUL INSTRUCTIONS FOR SHORTER, FASTER PROGRAMS

There's a big and very important difference between raw cycle time and "getting the job done" time. We believe computers should work smart, as well as hard. They should offer built-in features that assure faster execution.

With the NAKED MILLI you get a powerful instruction set with 95 instructions including 8 addressing modes; the NAKED MILLI offers better memory efficiency than micros — 8 or 16 bits.

This efficiency lets you write shorter programs with faster run times — and keeps memory costs to a minimum, since tasks run in less memory. And programs are easier to write, too.

In short, you get speed where it counts: on the job.

Memory Reference Instructions

In typical minicomputer applications, the computer usually spends a large percentage of its execution time successively doing a few operations on each of many pieces of data stored in memory — rather than performing repeated operations on just a few pieces of data which could be stored in registers. This usually means that memory is referenced frequently.

NAKED MILLI optimizes its instruction set for these typical minicomputer applications, to get greater efficiency and ease of programming. It provides a varied and powerful set of memory reference instructions ideal for OEM's.

Indirect Addressing

True multi-level indirect addressing lets the user construct and use powerful addressing methods for effective table addressing.

Word and Byte Addressing

We provide both word and byte addressing for most memory reference instructions. This means that you can deal directly with either bytes or full words, as the application requires, without the complications required in computers without byte addressing.

Full Shift Capability

We provide a full complement of shift instructions which can be: single or multiple place; left or right; logical or circular. Compare this with the basic single place shift found in most microcomputers.

Fast, Efficient Conditional Jumps

The conditional jump instructions test conditions within the processor (overflow, sense indicator, A and X registers) and perform conditional jumps, depending upon the results. Since each of these single word instructions performs both the test and the jump, memory is more efficiently utilized than with other computers which need two words for this function.

Immediate Instructions

We provide a full complement of immediate instructions. The address portion of the instruction actually contains the 8-bit operand itself, rather than an address. Only half as much memory is needed, since both instruction and operand are contained in a single word. Immediates include Add, Subtract, Load, and Compare.

Single Word Instruction Format

With only a few exceptions, our instructions require only one memory location. Compare this with many other minicomputers which require two or more memory locations for most instructions.

I/O MAXI-BUS™ FOR EASE OF INTERFACING

Maxi-Bus provides 58 parallel lines for data, command, device address, status, and control information. This eliminates the timing problems created when data and address lines are time-shared. It makes interfacing easier, faster and less expensive.

Memory and input/output interfaces connect directly to the Maxi-Bus. Each operates at its own pace. Under DMA this means that transfers can be made directly between external devices and memory without affecting the central processor, if desired.
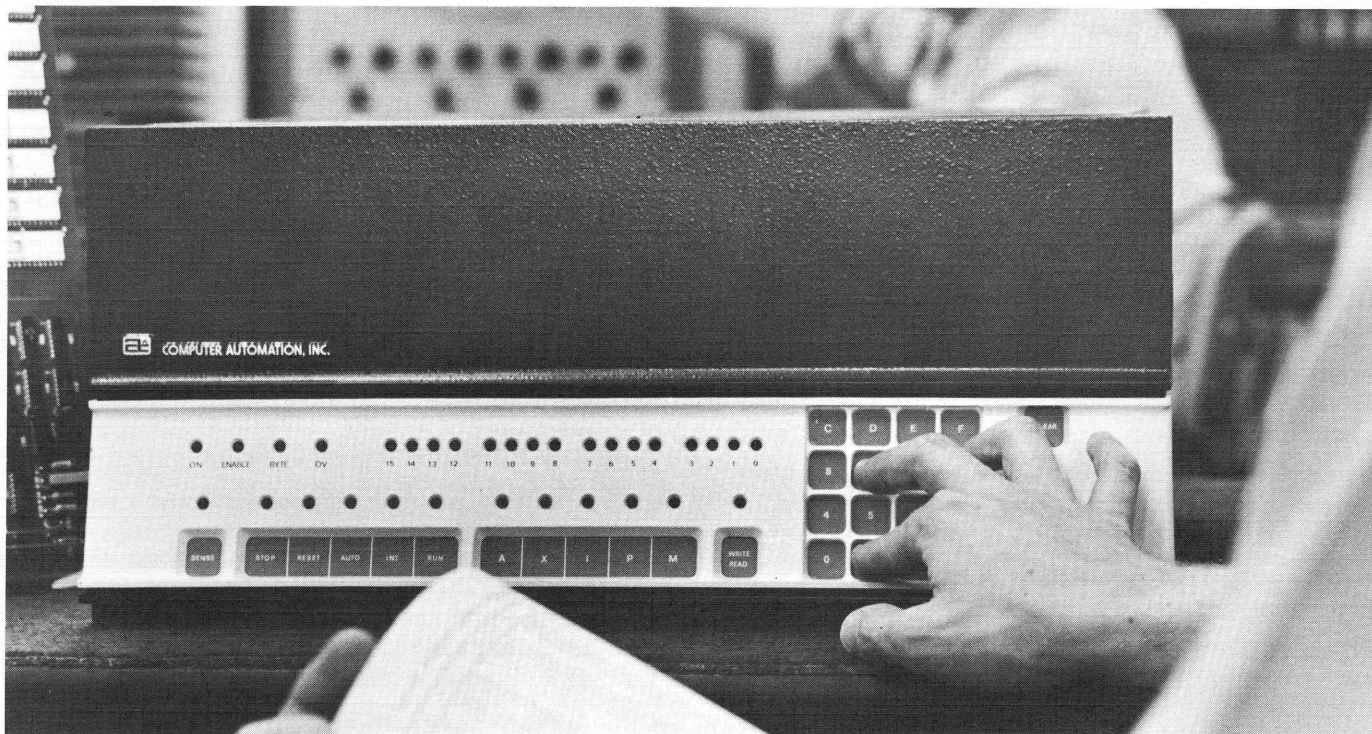
NAKED MILLI can be used with Computer Automation's unique hexadecimal keyboard which makes data entry fast and convenient.

It also means that as faster or lower cost memories and processors become available, they can be plugged into the system directly, without the need for modification.

This open ended design assures you of growth capabilities for the future, whenever your needs change.

Three Input/Output Modes for Maximum Power

You get three standard input/output systems for flexibility. Combined with a powerful set of I/O instructions, this results in an I/O structure which is exceptionally efficient and easy to use.

Both word and byte data can be handled directly, with byte data being packed or unpacked automatically as desired.

Direct Memory Access (DMA)

For highest speed transfer rates, DMA transfers data on a cycle-stealing basis directly between the memory and the external device, bypassing the central processor.

Programmed Input/Output

For greater flexibility, Programmed I/O provides transfers between the external interface and the A or X registers. Especially effective in applications where data must be examined immediately upon input (such as message handling, keyboard response, etc.) or where data is the result of a computation which must be output immediately.

Automatic Input/Output Channels

Auto I/O channels transfer data between memory and external interfaces in blocks of any size without disturbing the processor's working registers. Word or Byte Count and Current Address for each channel are held in memory; each transfer automatically updates them until the count is complete. This use of memory for control registers lowers the cost of interfacing. Multiple channels can operate concurrently, with hardware priority control of each channel. Transfers can be full 16-bit words or 8-bit bytes with automatic packing/unpacking.

HARDWARE PRIORITY INTERRUPTS

Our hardware priority interrupts provide automatic handling of:

- recognition of an external event which requires immediate attention.
- identification of which event, among many, actually occurred.

- resolution of priority when several events occur simultaneously.
- automatic vectoring of each interrupt to unique memory locations.

It also means really fast response to the event which caused the interrupt.

The necessary interrupt routines are simple, easy to write, take less memory space, and execute more quickly. Wasteful polling is completely eliminated.

POWER FAIL RESTART

Allows the LSI-3/05 computer to operate from unreliable power sources without human monitoring. Continually monitors power supply voltage to provide an orderly shutdown upon power failure and automatic restart when power is restored.

REAL TIME CLOCK

Provides increments at twice the AC line frequency. Allows maintenance of an accurate time of day clock and measurement of elapsed time.

AUTOLOAD OPTION

Allows program loading to be initiated automatically, remotely or from a front panel switch.

BIT SERIAL TELETYPE CONTROLLER OPTION

A low cost I/O interface for program loading or debugging which mounts piggyback on the processor card.

ADD-ON MEMORIES

Any combination of memories in any mix of types and speeds can be used with any LSI processor. This means the user can configure exactly the combination which best suits his needs now, and later change the combination to meet new needs merely by exchanging or adding the appropriate processor or memory boards. Now, indeed, any LSI system can "grow up" and change easily and quickly, even the the field.

Compatible add-on memories available with the NAKED MILLI are:

- Core memory in modules of 4K (half-card), 8K, and 16K words, offering memory cycle times as fast as 980 nanoseconds.
- Low-cost random access semiconductor (RAM) memory in modules of 256, 1K, 2K, 4K, and 8K words with optional Battery Pack.

- Nondestructive programmable read-only (PROM) and read-only (ROM) semiconductor memories in various sizes and combinations with RAM memory; optional On-card Battery Backup.
- Erasable programmable ROM (EPROM) in various sizes and combinations with RAM memory; optional On-card Battery Backup.

PACKAGED CONFIGURATIONS

Combinations of NAKED MILLI processor and memory cards are offered for economy in handling, and provide a substantial price discount compared to separately ordered units. For applications requiring packaged systems, the NAKED MILLI processor is also available in low-cost ALPHA Series configurations which include a 19-inch (rack-mountable) chassis, power supply, and console. Both CPU/Memory Combinations and the ALPHA Series are offered with four initial memory configurations:

- RAM/ROM/PROM
- RAM/EPROM
- RAM-only
- Core

In addition to available Add-on Memories, a 1K word half-card Core module is offered with packaged configurations.

SUPPORT

Because the LSI-3/05 is a member of a large family of compatible computers, the millicomputer user has available to him a wealth of memory and input/output options that simply are not available with any microcomputer. For example, he can use with the LSI-3/05 our new Distributed I/O System, the minicomputer industry's first unified approach to low cost, high performance I/O interfacing. One half-card I/O Distributor can support up to eight Intelligent Cables interfaced to any combination of input or output, serial or parallel peripherals - - all transferring data directly to or from memory concurrently.

From paper tape readers and punches through floppy disks and large moving head disks, a complete line of peripheral systems, peripherals, controllers, diagnostics and software is available to assist in developing millicomputer based products and also for use within these products. With the NAKED MILLI the user can concentrate on designing his product, not spending time designing special interfaces. A complete line of general purpose interfaces is also available.

NAKED MILLI (right) and I/O Distributor pictured with variety of standard peripherals and user-designed I/O devices, including special consoles, instruments. etc.

The NAKED MILLI LSI-3/05 is supported by four chassis types, four power supplies and two types of consoles.

Software for the LSI-3/05 includes loaders, utilities, a conversational debug package, Computer Automation's unique 4K and 8K-word OMEGA conversational assemblers/ editors and a Real Time Executive (RTX) system which includes an I/O Executive (IOX). Programming support for the LSI-3/05 is also provided by LSI-2 based Disk Operating Systems. FORTRAN IV programs may be executed under the LSI-3/05 RTX system. An extensive set of arithmetic and conversion routines is also available to LSI-3/05 users.

FEATURES

Obsolescence-proof Family

Open-ended design: change capacity or speed, quickly and easily, in the field.
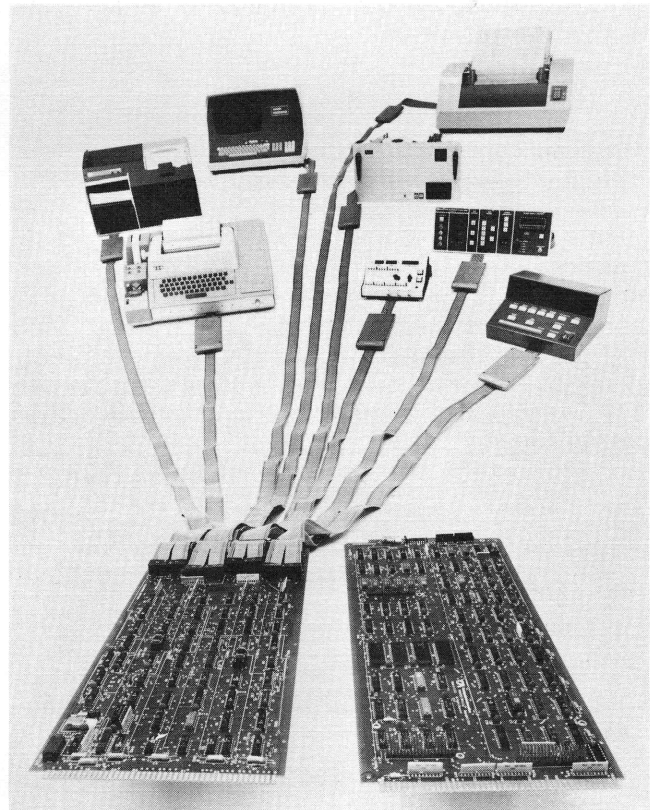
Four processors; core and semiconductor memories in twelve sizes; variety of options and interfaces.

Efficient Hardware Means Easy Integration

Memory from 256 to 256K (16-bit) words

Relative addressing eliminates fixed page problems

Indexed addressing for efficient loop control and table processing

High temperature testing in an oven to verify long-term reliability. Test includes seventy-two hours at 50°C.

Multi-level indirect addressing

Vectored priority interrupts

Full range of options includes Power Fail Restart, Real Time Clock, and Autoload

Complete set of peripheral and general purpose interface modules

Quality Construction

100% burn-in of IC's to MIL-STD-883

Powerful Instruction Set For More Efficient Use of Memory

Single word instruction format saves memory

Extensive byte capability means easier programming

Immediate instructions save storage space for constants

Complete set of logical instructions: OR, XOR, AND

Multi-place register rotate and logical shift instructions

Maxi-Bus Provides Three Standard Input/Output Systems

Direct Memory Access (DMA) standard for very high speed transfers

Automatic Input/Output channels for concurrent I/O directly to/from memory

Programmed I/O through A or X registers

INSTRUCTION TIMES

Instruction times given here apply to core memories. See Computer Handbook for timings for other memories.

Memory Reference instruction times apply for scratchpad addressing mode. For other modes add the times listed below.

Addressing Mode	Additional Time
Scratchpad	-----
Relative	+ .25 μ sec
Indexed	+ .25 μ sec
Indirect Scratchpad	+ 1.75 μ sec
Indirect Relative	+ 2.0 μ sec
Indirect Scratchpad Post-Indexed	+ 2.25 μ sec

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Memory Reference

WORD MODE

Instruction	Description	Time (μsec)
ADD	Add to A	6.25
AND	AND to A	6.5
CMS	Compare A with Memory, Skip (Low, High, Equal)	6.75 (no skip) 8.0 (skip)
EMA	Exchange Memory with A	8.75
IMS	Increment Memory, Skip on Zero	9.75 (no skip) 10.0 (skip)
IOR	Inclusive OR to A	6.5
JMP	Jump Unconditional	6.25
JST	Jump and Store P	9.75
LDA	Load A	5.5
LDX	Load X	5.5
STA	Store A	7.75
STX	Store X	7.75
SUB	Subtract from A	6.5
XOR	Exclusive OR to A	6.5

BYTE MODE

Instruction	Description	Time (μsec)
ADDB	Add to A	6.75
ANDB	AND to A	7.0
CMSB	Compare A with Memory, Skip (Low, High, Equal)	7.25 (no skip) 8.5 (skip)
EMAB	Exchange Memory with A	9.25
IORB	Inclusive OR to A	7.0
LDAB	Load A	6.0
LDXB	Load X	6.0
STAB	Store A	8.25
STXB	Store X	8.25
SUBB	Subtract from A	7.0
XORB	Exclusive OR to A	7.0

Byte Immediate

Instruction	Description	Time (μsec)
AAI	Add to A Immediate	5.25
AXI	Add to X Immediate	5.25
CAI	Compare to A Immediate, Skip on Not Equal	5.0 (no skip) 5.25 (skip)
CXI	Compare to X Immediate, Skip on Not Equal	5.0 (no skip) 5.25 (skip)
LAM	Load A Minus Immediate	3.75
LAP	Load A Positive Immediate	3.75
LXM	Load X Minus Immediate	3.75
LXP	Load X Positive Immediate	3.75
SAI	Subtract from A Immediate	5.25
SXI	Subtract from X Immediate	5.25

Conditional Jump

Instruction	Description	No Jump	Jump
JAG	A Greater than Zero	4.25	5.5
JAL	A Less than, or Equal to Zero	4.4	5.75
JAM	A Minus	4.0	5.25
JAN	A Not Zero	4.5	5.75
JAP	A Positive	4.25	5.0
JAZ	A Zero	4.25	5.5
JOR	OV Reset	4.5	6.25
JOS	OV Set (and Force OV Reset)	5.25	6.75
JSR	SENSE Reset	4.5	5.5
JSS	SENSE Set	4.5	5.5
JXN	X Not Zero	4.5	5.75
JXZ	X Zero	4.25	5.5

Single Register Bit Change

LLA	Logical Left A	5.75*
LLX	Logical Left X	5.75*
LRA	Logical Right A	5.75*
LRX	Logical Right X	5.75*
RLA	Rotate Left A with OV	5.75*
RLX	Rotate Left X with OV	5.75*
RRA	Rotate Right A with OV	5.75*
RRX	Rotate Right X with OV	5.75*

*Add .25 microseconds per positions shifted

Register Change and Control

Instruction	Description	Time (μsec)
ICA	Input Console Data Reg. to A	5.5
ICX	Input Console Data Reg. to X	5.5
ISA	Input Console Sense Reg. to A	5.5
ISX	Input Console Sense Reg. to X	5.5
NAR	Negate A	7.0
NAX	Negate A and Put in X	7.0
NXA	Negate X and Put in A	7.0
NXR	'Negate X	7.0
OCA	Output A to Console Data Reg.	4.75
OCX	Output X to Console Data Reg.	4.75
ROV	Reset OV	5.5
SOV	Set OV	5.5
TAX	Transfer A to X	4.75
TPX	Transfer P to X	4.75
TXA	Transfer X to A	4.75
CID	Console Interrupt Disable	6.25
CIE	Console Interrupt Enable	6.25
DIN	Disable Interrupts	7.25
EIN	Enable Interrupts	7.25

Instruction	Description	Time (μsec)
HLT	Halt	
NOP	No Operation	4.75
RTCD	Real Time Clock Disable	6.5
RTCE	Real Time Clock Enable	6.5
SBM	Set Byte Mode	5.75
SIA	Status Input to A	4.75
SIN	Status Inhibit	6.25
SIX	Status Input to X	4.75
SOA	Status Output from A	4.75
SOX	Status Output from X	4.75
SWM	Set Word Mode	5.75

Input/Output

Instruction	Description	Time (μsec)
AIB	Auto. Input to Memory, Byte	20.0*
AIN	Auto. Input to Memory, Word	19.75*
AOB	Auto. Output from Memory, Byte	18.5*
AOT	Auto. Output from Memory, Word	18.5*
INA	Input Word to A	5.5
INX	Input Word to X	5.5
OTA	Output A	4.75
OTX	Output X	4.75
SEA	Select and Present A	4.75
SEN	Sense and Skip on Response	4.75
SEX	Select and Present X	4.75

*Add .25 μ sec if last word of block.
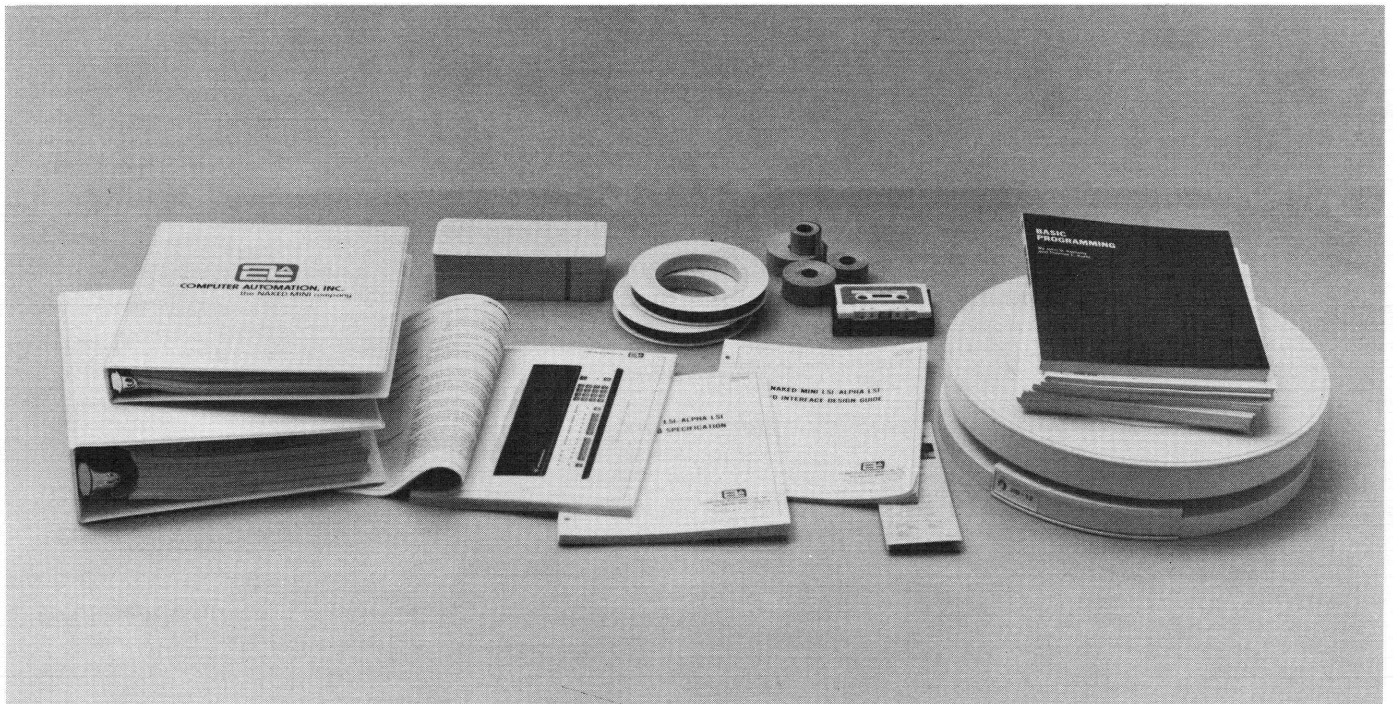
NAKED MILLI support includes extensive software and full documentation.

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