INTEGRATED CIRCUITS SERIES

MOS DIGITAL INTEGRATED CIRCUITS

Delco Electronics

GENERAL MOTORS CORPORATION MILWAUKEE, WISCONSIN 53201

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MOS DIGITAL INTEGRATED CIRCUITS

a programed instructional text

programed by:

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Delco Electronics

GENERAL MOTORS CORPORATION MILWAUKEE, WISCONSIN 53201

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HOW TO USE THIS TEXT

This is a programed text. Unlike a conventional text, it is divided into numbered sections called frames. In most cases, each frame represents a single concept or unit of information. As in all programed texts, the student must actively participate in the program to obtain full benefit.

To enable the student to participate, the majority of frames contain one or more questions. The answer to each question is shaded and always appears in the beginning of the following frame.

There are two basic types of questions used in this text. The first is used with "lecture" frames; i.e., frames which present complete units of information or concepts. This type of question simply tests your comprehension of the material presented in that frame.

The other type of question is used with frames in which the information or concept is intentionally left incomplete. In these frames, which are in the majority in this text, the student is required to use whatever information he is given (either in the text of the frame or in the accompanying illustration) to answer the question. The answer to the question, then, completes the concept or unit of information presented in the frame.

When you have completed the text, do the sample test at the end of the text. Correct the sample test using the answer sheet provided at the end of the test. If your score is 80 or higher and you are satisfied with your comprehension of the material presented in the text, complete the examination (bound into the text following the sample test) and submit it for correction.

INTRODUCTION

Metal-Oxide-Semiconductor (MOS) technology is one of the fastest changing fields in electronics. New techniques are being experimented with or put into production almost daily. It would be impossible to publish a book covering all the latest techniques and devices; it would be out of date by the time it was in print. The purpose of this text, therefore, is to explain the basics of MOS and to provide the background knowledge necessary for an understanding of state-of-the-art discussions and articles. In this way it is similar to the Bipolar Digital Integrated Circuits text. When you finish this text, you will not be an MOS expert, but you will at least have a good idea of what MOS is all about, and articles describing the latest MOS devices and techniques should make sense to you.

STUDENT PREREQUISITES

Before starting this text, you should be able to:

1. Identify the components in a cross-sectional drawing of a bipolar integrated circuit.

2. Define diffusion, epitaxial growth, and deposition as they apply to integrated circuits.

3. Identify schematic drawings and state characteristics of the different types of bipolar digital integrated circuits such as DTL and TTL.

4. Given the polarity of the applied voltage and the type of current carriers (holes or electrons), determine the direction the current carriers will flow.

5. Identify the logic function or functions represented by a given switching diagram or truth table.

6. Describe the results of forward or reverse biasing a P-N junction.

STUDENT LEARNING OBJECTIVES

Upon completion of this text, you will be able to:

1. Identify schematics, state characteristics, and explain operation of inverters, NAND gates, and NOR gates of each of the following types:

   A. PMOS with enhancement MOSFET's used as loads
   B. PMOS with depletion MOSFET's used as loads
   C. CMOS

2. Given either a schematic symbol or a cross-sectional drawing of the physical construction, identify each of the four basic types of MOSFET and, given the polarity of the applied voltage, identify the source and drain.

3. State characteristics, identify cross-sectional drawings, and identify steps in the construction of each of the following:

   A. MNOS
   B. MOSFET's using self-aligning metal gates
   C. MOSFET's using self-aligning silicon gates
   D. SIS
   E. Coplamos

4. Define and/or identify the effects of the following:

   A. Threshold voltage
   B. Pinch-off voltage
   C. Field threshold
   D. Threshold adjustment
   E. Ion implantation
   F. Self-alignment
   G. Gate capacitance
   H. Parasitic capacitance
   I. Parasitic current
   J. Polysilicon
   K. IGFET
   L. Work function
   M. Passivation

(1) In any discussion of MOS devices or technology, the first thing to do is establish a few definitions and then clarify the definitions. As you probably know, MOS is the acronym for M _____ O _____ S _____ .

---

(2) *Metal Oxide Semiconductor*

This sounds as if it refers to the materials from which MOS devices are made, and, in a way, this is true — but not completely. Notice, for instance, that a bipolar transistor is actually constructed of metal, oxide, and semiconductor materials. In a bipolar transistor, however, the "active" parts are all made of doped sections of the semiconductor. The oxide is simply an insulator, and the metal is used only for connections to other components. In MOS, as we will see shortly, metal and oxide are integral parts of the transistor. A device made of metal, oxide, and semiconductor materials, then, would be considered _____ (only MOS/only bipolar/either bipolar or MOS).

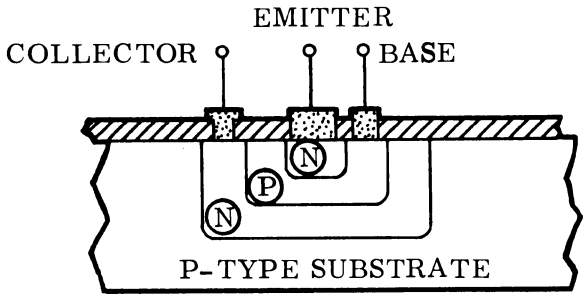
---

(3) *either bipolar or MOS*

For example, the transistor in the previous frame was bipolar. The capacitor shown here would be considered MOS because one plate is metal, the other is semiconductor, and the dielectric is oxide.

Even this definition, however, can be misleading. The first MOS devices were strictly metal-oxide-semiconductor devices; but, since that time, other materials have been used in addition to or in place of the original three. For example, nitride is sometimes used in place of oxide. Even so, the general term MOS is still applied to these devices. Some of the other materials and their functions will be discussed later.

(1)
(2)



BIPOLAR TRANSISTOR

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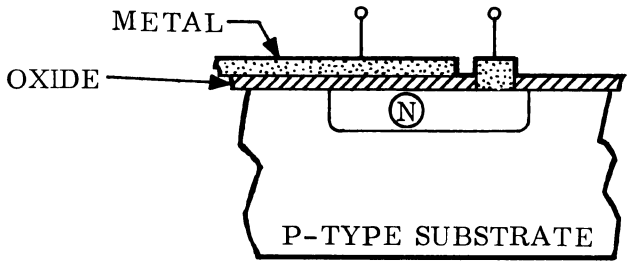
(3)



MOS CAPACITOR

(4) The other important acronym in this text is FET, which stands for Field Effect Transistor. A FET is simply a transistor which is controlled not by biasing a P-N junction but by the electric field generated by an applied voltage. How this field effect works will be explained shortly, but first there are a couple of general statements that should be made about MOS and FET's.

1. Most — but not all — MOS devices are FET's. (There are, for instance, the MOS capacitors mentioned above.)

2. Most — but not all — FET's are MOS. (There are also junction FET's — JFET's — which, while utilizing a voltage field effect for control, do not utilize metal, oxide, or any direct substitute as integral parts of their construction.)

It would seem logical, then, to refer to an MOS device which is also an FET as a/an _____ .

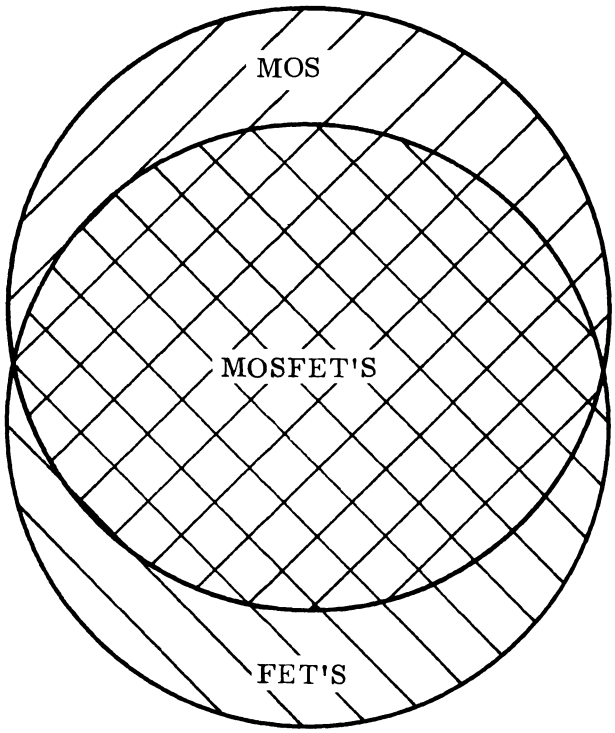
---

(5) *MOSFET*

MOSFET's — MOS Field Effect Transistors — are what we will be covering in this text. There is one more acronym to be introduced first, however : IGFET. The FET part still stands for Field Effect Transistor; the IG stands for Insulated Gate. All you need to remember at this point is that IGFET and MOSFET can, for our purposes, be used interchangeably. The reason for this will become clear as we get into the construction and operation of MOSFET's.

Which of the following terms are synonymous? MOS, FET, MOSFET, JFET, IGFET_____ .

(4)
(5)



(6) MOSFET and IGFET

There are four basic types of MOSFET. We will start with the type that first came into general use and still accounts for a large percentage of all MOSFET's being manufactured. All four types are similar in principle so that, once this first type is understood, the other three can be explained by comparing them with this first type.

Notice first that the MOSFET, like the bipolar transistor, has three elements. In the bipolar transistor, these elements were the emitter, base, and collector. In the MOSFET, the three elements are the _____ , _____ , and _____ .

---

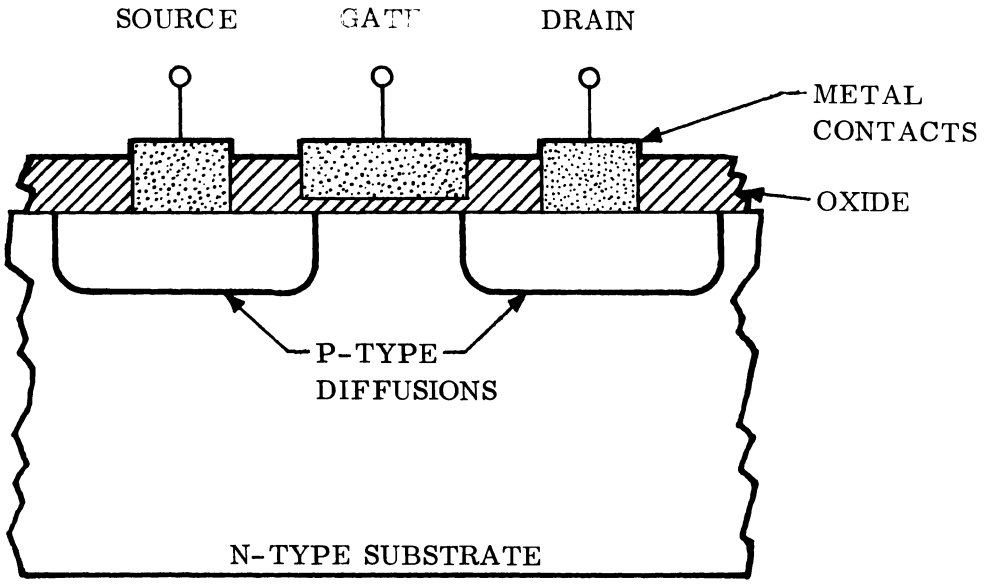
(7) *source, gate, and drain*

In a general sense, the source is comparable to the emitter of a bipolar transistor, the gate to the base, and the drain to the collector. Similarly, the MOSFET can be compared to a vacuum tube, with the source corresponding to the cathode, the gate to the grid, and the drain to the plate. In fact, as we will see shortly, the similarity between MOSFET's and tubes is greater in some ways than the similarity between MOSFET's and bipolar transistors.

---

(8) The two diffused areas themselves are the source and drain. The metal contacts are simply that — contacts used to connect the drain and source to other circuits. Internally, the only path between the source and drain is through the substrate material. As indicated, the substrate in this type of MOSFET is N-type and the source and drain are both P-type. Regardless of the polarity of voltage applied between the source and drain, then, the resistance of the source-to-drain path would always be _____ (high/low) because one of the P-N junctions would always be _____ (forward/reverse) biased.

(6)
(7)
(8)


SOURCE
GATE
DRAIN
METAL CONTACTS
OXIDE
P-TYPE DIFFUSIONS
N-TYPE SUBSTRATE

(9) high

reverse

The same could be said of the emitter-to-collector path of a bipolar transistor. If this were a bipolar transistor, it could be turned on by applying a negative voltage to the substrate (or "base"). This would forward bias the transistor and allow a heavy current flow as long as the drain was positive with respect to the source. In the MOSFET, this_____ (can also/can not) be done because the gate is _____ (connected to/insulated from) the substrate.

---

(10) can not

insulated from

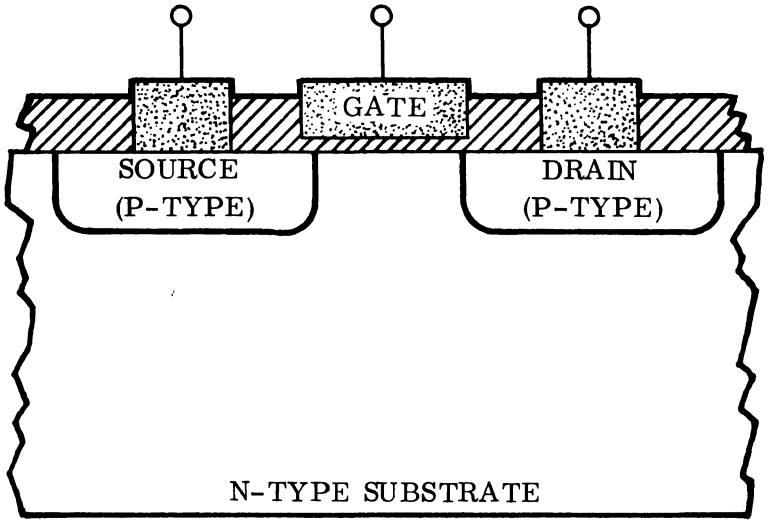
Notice that we said "gate" rather than "gate contact". This is because the metal itself is the gate. It is not simply a contact as is the case for the source and drain contacts. Thus, as was stated earlier, the FET is constructed of metal, oxide, and semiconductor and is therefore an MOS device. The fact that the gate is insulated from the substrate, as well as from the source and drain, is the reason the MOSFET is also known as a/an _____ FET.

---

(11) Insulated Gate (IG)

Notice, however, that the oxide separating the gate from the substrate is _____ (thinner/thicker) than the rest of the oxide.

(9)
(10)
(11)



(12) thinner

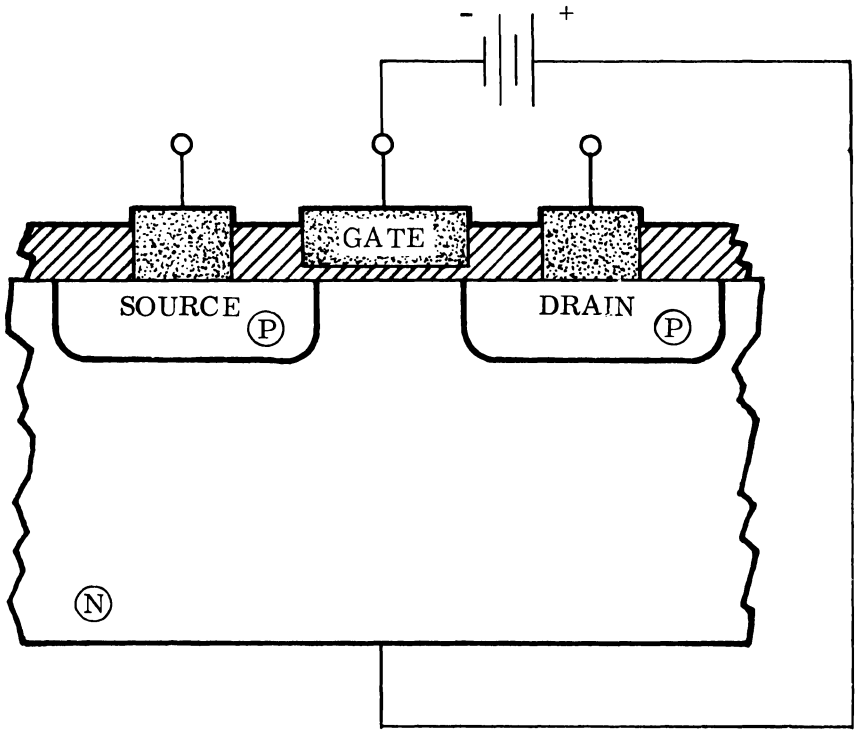
The oxide beneath the gate is made as thin as possible so that the field generated by the voltage applied to the gate will have as great an effect as possible on the substrate directly beneath the oxide. To see what this effect will be, we will apply a negative voltage to the gate as shown. Notice that the voltage is applied between the gate and the substrate. As a result of this gate voltage, the gate _____ (will/will not) draw current.

---

(13) will not

Because of the insulating oxide, there is no current flow, not even as much as there would be through a reverse-biased P-N junction. Even so, the substrate is affected. The negative voltage on the gate will repel the _____ (electrons/holes) in the substrate and attract the _____.

(12)
(13)



(14) electrons

holes

Since the substrate is N-type material, there are more free electrons than holes. How many more depends on how heavily it is doped. Even so, a sufficiently negative voltage applied to the gate will attract enough holes to make the MOSFET look like this. As indicated in the illustration, a "channel" is formed. The negative gate voltage, in effect, transforms a small part of the substrate into _____ _____ (N-type/P-type) material.

---

(15) P-type

As a result, the P-type material in the source is connected to the P-type material in the drain by the induced channel of P-type material in the substrate. With a negative voltage applied to the gate, then, the source-to-drain path has _____ (0/1/2) P-N junction(s) and will present a _____ (higher/lower/unchanged) resistance than it would with no voltage on the gate.

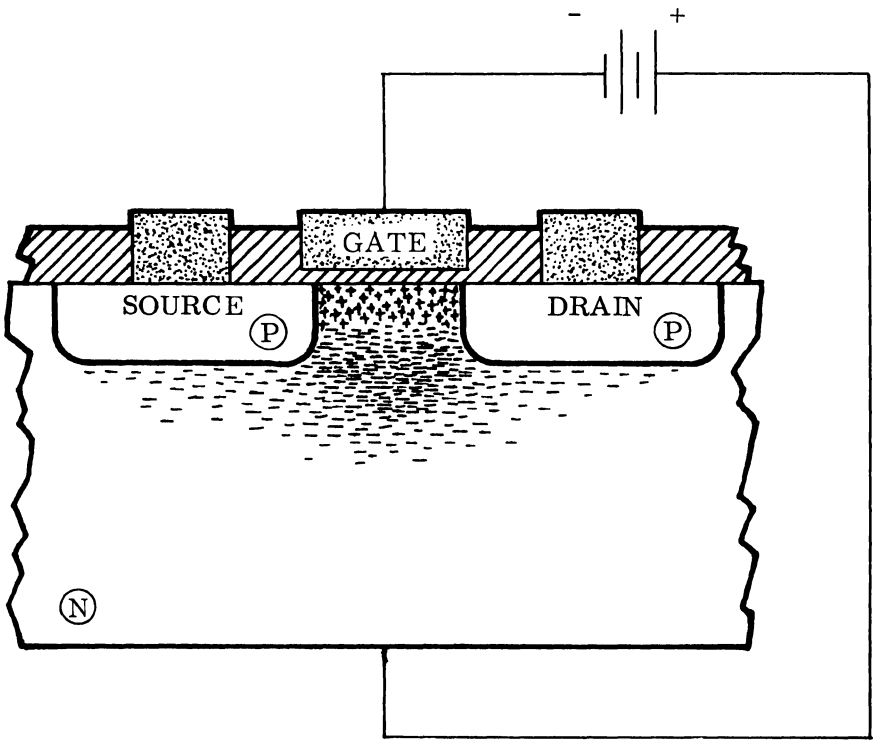
---

(16) 0

lower

Loosely speaking, we can say that the gate voltage at which this channel of P-type material — or simply the "P-channel" — appears is called the threshold voltage. (This definition will be modified and tightened later.) At first, when the gate voltage is equal to the threshold voltage, the channel is very thin. As the gate voltage is made more negative, the channel becomes thicker and the source-to-drain resistance_____ (increases/decreases).

(14)
(15)
(16)



(17) decreases

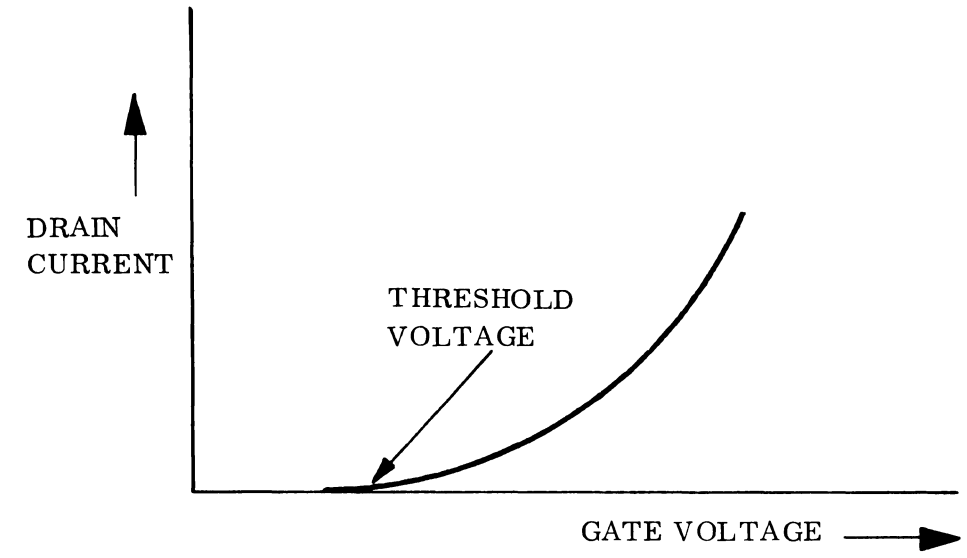
One way of looking at this effect is shown in the illustration. As you can see, there is no point at which the drain current can be said to start abruptly. It is a gradual process. For convenience, the threshold voltage is often defined as the gate voltage at which 10 microamperes of drain current flows. Based on this definition, you would expect the threshold voltage to be _____ (somewhat dependent on/totally independent of) the drain voltage.

---

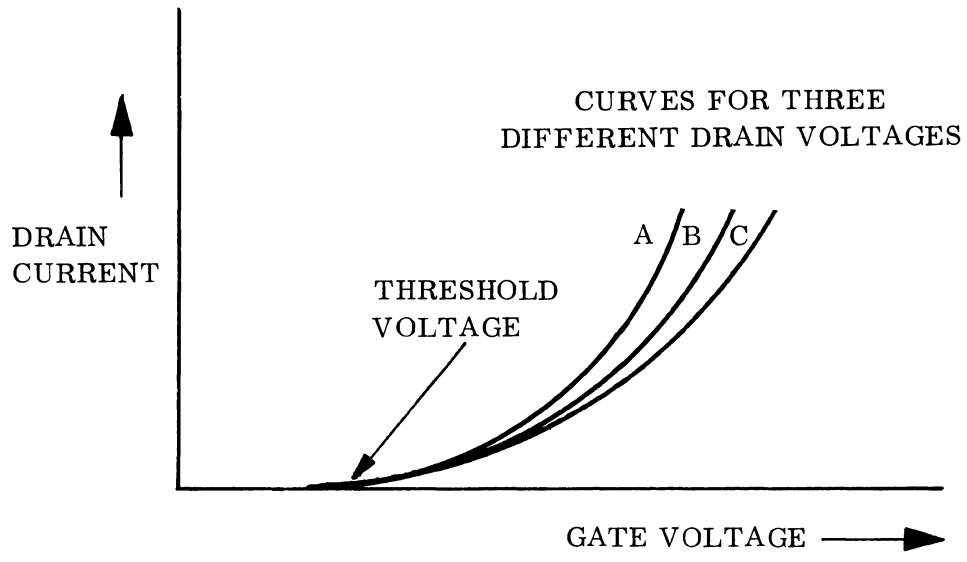
(18) *somewhat dependent on*

The dependence, however, is quite slight. For our purposes we can say that the threshold voltage is essentially constant. As indicated in the illustration, the drain voltage has a greater effect on the slope of the curve than on the threshold voltage itself. Which of the three curves shown would represent the highest drain voltage? _____ The lowest? _____

(17)


DRAIN
CURRENT
THRESHOLD
VOLTAGE
GATE VOLTAGE

(18)


CURVES FOR THREE
DIFFERENT DRAIN VOLTAGES
A
B
C
DRAIN
CURRENT
THRESHOLD
VOLTAGE
GATE VOLTAGE

(19) A (highest)

C (lowest)

In some ways, then, our MOSFET is similar to a bipolar transistor. There are some important differences, however. One of the more obvious differences, which has been touched on already, is that, because of the oxide gate insulation, the current drawn by the gate will be essentially zero _____
(at all times/only when the MOSFET is turned on/only when the MOSFET is turned off).

---

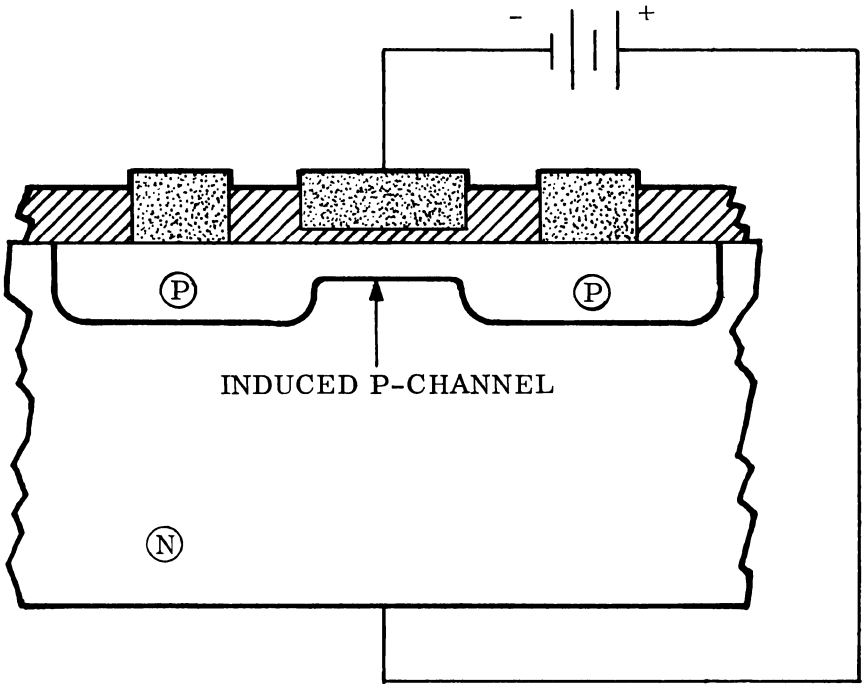
(20) at all times

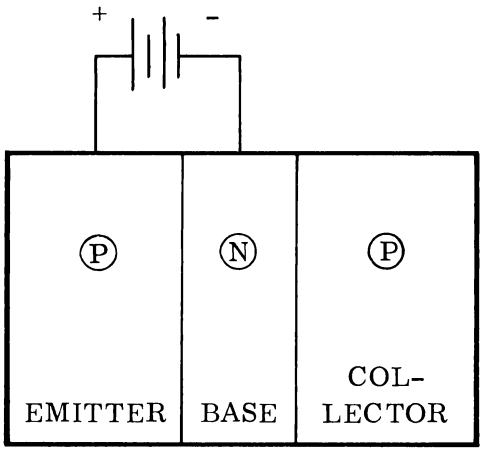
The gate acts like a small capacitor and, except for leakage, draws current only while being charged. In a bipolar transistor, on the other hand, the base draws a fairly high current whenever the transistor is turned on.

Another difference can be seen if we take a closer look at the source-to-drain path and compare it to the emitter-to-collector path of a bipolar transistor. When a bipolar transistor is turned on, the two junctions are, in effect, forward biased as far as the collector current is concerned. Even so, the P-N junctions still exist, and there is a certain voltage drop developed across these junctions no matter how forward biased they are (short of total breakdown, of course). Since there are no P-N junctions in the turned-on MOSFET, there are no corresponding voltage drops developed. The only voltage drop is a result of the resistance of the semiconductor material itself.

Assuming adequate gate and base voltages are available, which device could be made to exhibit the lower apparent resistance in a given circuit? _____

(19)
(20)





(21) A MOSFET

This does not mean that MOSFET's always have lower voltage drops than do bipolar transistors. It only means that, given sufficient gate voltage and the proper circuit, MOSFET's are capable of lower voltage drops than bipolar transistors, simply because MOSFET's, when turned on, do not have P-N junction voltage drops to contend with.

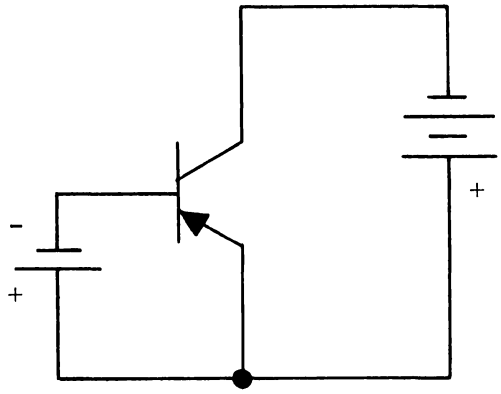
Still another difference between MOSFET's and bipolar transistors has to do with the direction of current flow. Current through a turned-on bipolar transistor would flow in only one direction. In the PNP transistor shown here, for instance, a heavy collector current would be flowing. But if the collector voltage were reversed, there would be no collector current. From what you have seen of the MOSFET so far, you would expect current to flow through the induced channel _____ _____ (only in one direction/equally well in either direction).

---

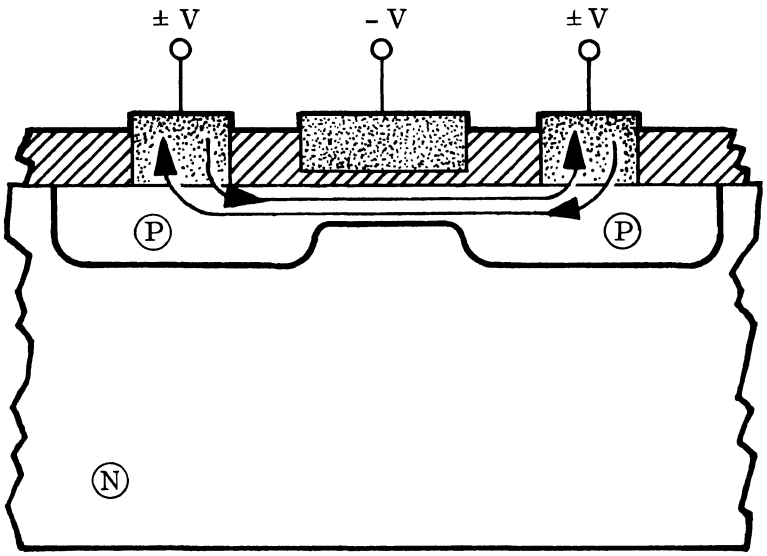
(22) *equally well in either direction*

Since there are no P-N junctions to be forward or reverse biased, current can flow in either direction as long as the gate is sufficiently negative to induce the P-channel between the source and drain. The polarity of the source and drain voltage would make no difference. Thus, you could say that MOSFET's are theoretically symmetrical, meaning that the drain and source are functionally interchangeable. (An explanation of how to tell which is the source and which is the drain is coming up shortly in the section on MOSFET symbology.)

(21)



(22)



(23) As we said at the start, the MOSFET we have been discussing is only one of four basic types. A second type is shown here. This MOSFET is identical to the previous type except that there is a channel of P-type material built into the substrate between the source and drain. With no voltage applied to the gate, the source-to-drain path would present a _____ (high/low) resistance.

---

(24) low

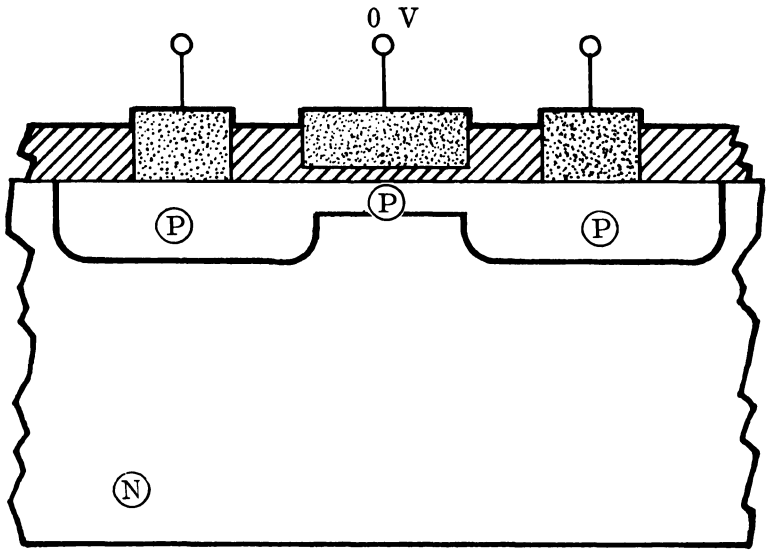
In other words, this type of MOSFET would be turned on when no gate voltage is applied. Now, what happens if we apply a negative voltage to the gate, as we did to the first type of MOSFET? The negative gate voltage will, as before, repel the electrons and attract the holes in the substrate. As a result, the concentration of holes in the P-channel, as well as the depth of the P-channel, will increase, and the resistance of the channel will _____ (increase/decrease).

---

(25) decrease

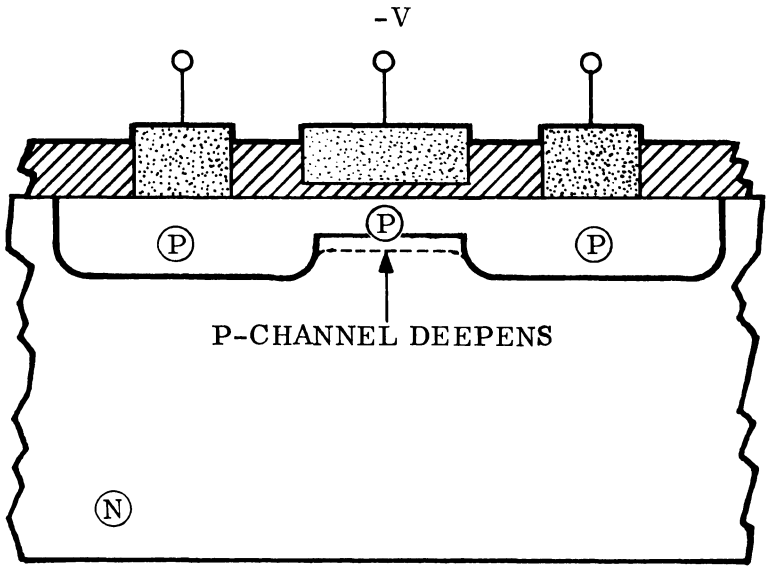
Suppose, however, that a positive voltage is applied to the gate. A positive voltage would repel the holes and attract the electrons. It would cause a channel of _____ material to form within the built-in channel of P-type material.

(23)



(24)

(25)



(26) N-type

The current, of course, cannot pass through the N-type material since, in order to do so, it would have to pass through two P-N junctions, one of which would always be reverse biased, regardless of the way current was flowing. The induced channel of N-type material within the P-channel is called a "depletion zone." This is because the majority carriers, the holes, have been depleted. The current through the P-channel would be cut off when the depletion zone _____ _____ (first formed/filled the built-in P-channel/reached the bottom of the substrate).

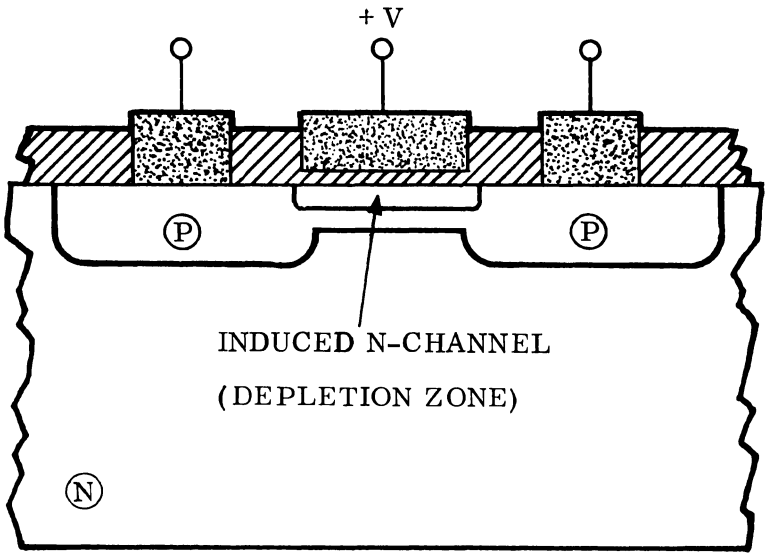
---

(27) filled the built-in P-channel

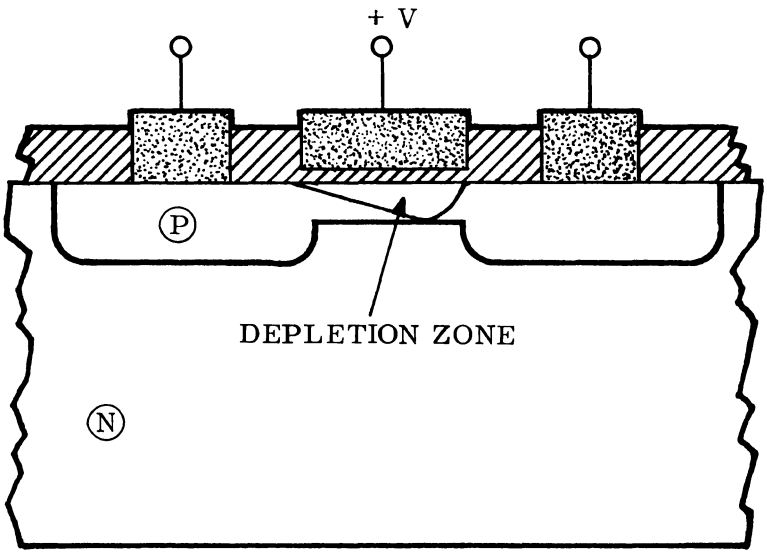
The term actually used is "pinched off," rather than "cut off." The reason for this can be seen in the illustration. As you can see, the depletion zone does not expand evenly and literally pinches off the P-channel at some point. (This is at least partly the result of the source and drain voltages.)

You would expect the gate voltage at which this condition is reached to be called the _____ voltage.

(26)



(27)



(28) pinch-off

Current flow in both of the MOSFET's we have discussed so far has been through a channel of P-type material. Logically enough, they are called P-channel MOSFET's. They can be further identified as either enhancement type or depletion type, depending on whether the channel is induced or built in. The MOSFET with the built-in channel would be a/an _____ type, while the MOSFET in which a channel must be induced would be a/an _____ type.

---

(29) *depletion (built-in channel)*

enhancement (induced channel)

The other two major types of MOSFET's are shown here. In these, the substrate is made of P-type material, and the source and drain are made of N-type. You would expect these MOSFET's to both be called_____-channel.

---

(30) *N*

As the P-channel MOSFET's were further identified as enhancement and depletion types, so are the N-channel MOSFET's. The upper MOSFET in the illustration is a/an _____ type, while the lower is a/an _____ type.

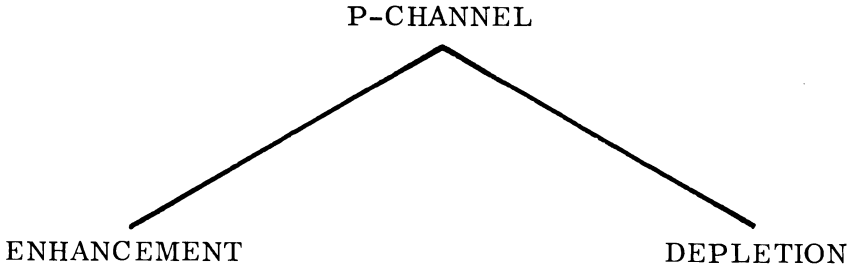
---

(31) *enhancement (upper)*

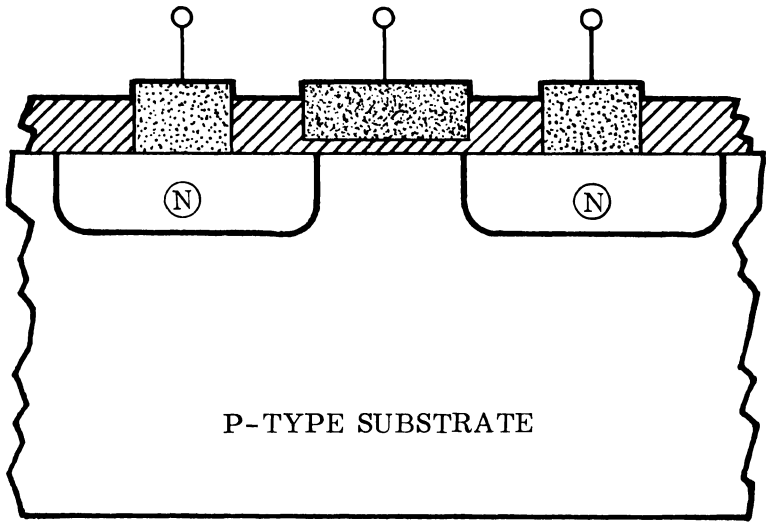
depletion (lower)

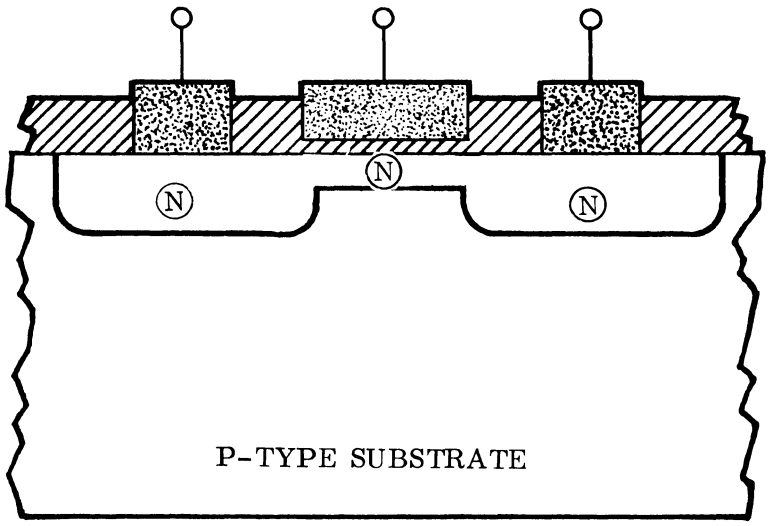
We'll start with the enhancement type. To produce the N-channel necessary to turn the N-channel enhancement MOSFET on, you would have to apply a _____ (positive/negative) gate voltage.

(28)


P-CHANNEL
ENHANCEMENT
DEPLETION

(29)
(30)
(31)


N
N
P-TYPE SUBSTRATE


N
N
N
P-TYPE SUBSTRATE

(32) positive

A positive gate voltage would attract the necessary electrons to the gate area of the substrate. Similarly, an N-channel depletion MOSFET would require a _____ _____ (positive/negative) voltage to produce a depletion zone and pinch off the built-in N-channel.

---

(33) negative

As far as basic operation goes, then, the N-channel and P-channel MOSFET's are quite similar, differing primarily in the polarity of the required gate voltages. One other difference worth noting at this time has to do with the type of current carriers utilized. As has been indicated, the P-channel current carriers are holes, and the N-channel current carriers are electrons. Electrons are inherently better current carriers than holes, simply because electrons are able to move around more easily. Electrons are said to have a higher mobility, roughly twice that of holes. For the same size channel and the same drain-to-source voltage, an N-channel MOSFET would have _____ (twice/half/the same) source-to-drain current as would a P-channel MOSFET.

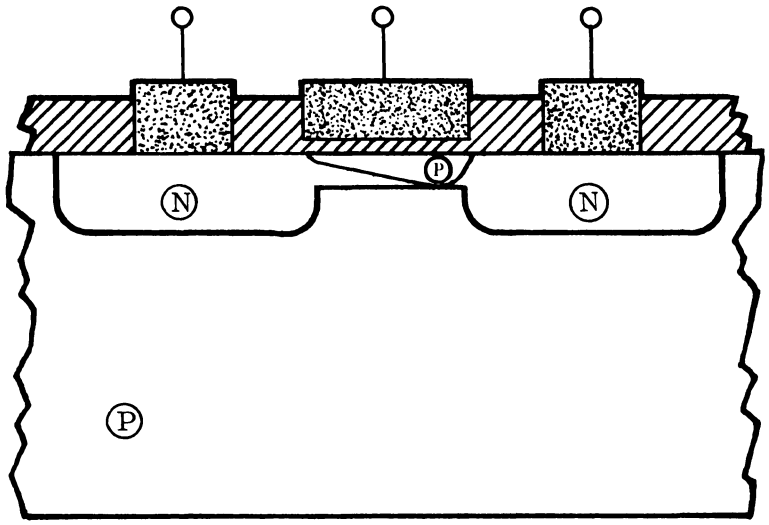
---

(34) twice

The easier the current carriers are to move, the greater the current for a given voltage. This, of course, would be an advantage for N-channel MOSFET's. It is, however, only one difference among many. Each of the four types has certain advantages and disadvantages, either in terms of performance and size or in terms of cost and manufacturing difficulty, and no single type presently has a clearcut advantage over all other types. A number of the advantages and disadvantages of each type will be discussed later.

V = ?

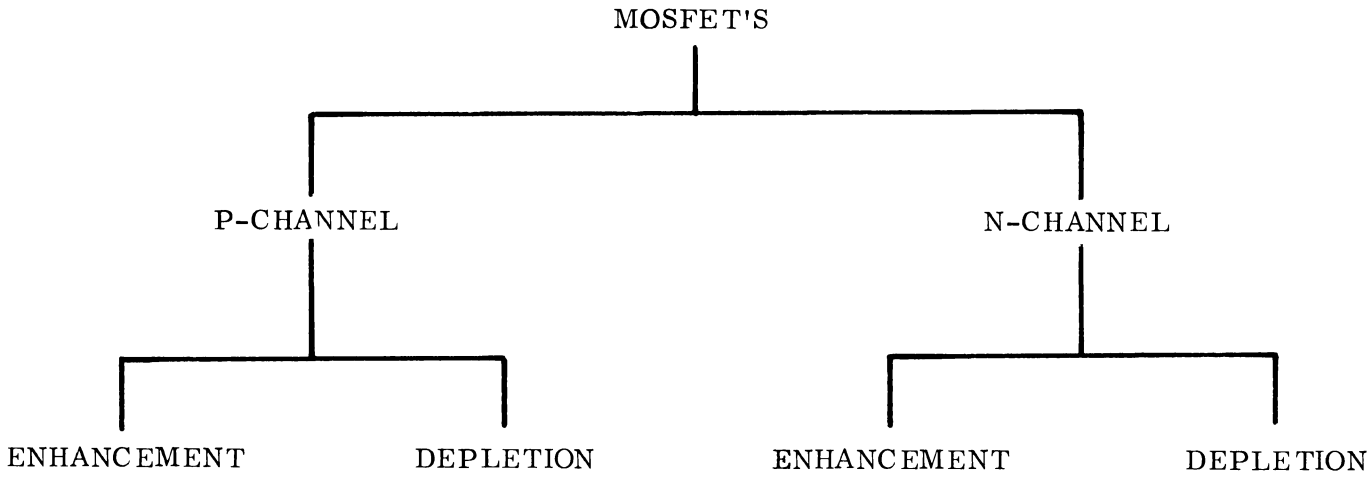
(32)


P
N
N
P

---

(33)

(34)


MOSFET'S
P-CHANNEL
N-CHANNEL
ENHANCEMENT
DEPLETION
ENHANCEMENT
DEPLETION

(35) REVIEW

1. Identify each MOSFET in the illustration (P-channel, N-channel, enhancement, depletion). In each case, indicate whether the MOSFET will be turned on or off when no gate voltage is applied. Also indicate what polarity of gate voltage would then be required to turn it off or on.

   A. _____

   Normally_____(on/off)

   Turned_____(on/off) by a _____(positive/negative) gate voltage

   B. _____

   Normally_____(on/off)

   Turned_____(on/off) by a _____(positive/negative) gate voltage

   C. _____

   Normally_____(on/off)

   Turned _____(on/off) by a _____(positive/negative) gate voltage

   D. _____

   Normally_____(on/off)

   Turned _____(on/off) by a _____(positive/negative) gate voltage

2. The gate current in these MOSFET's will be essentially zero_____.

   A. only when they are turned off

   B. only when they are turned on

   C. at all times

   D. only when the gate is negative

   E. only when the gate is positive

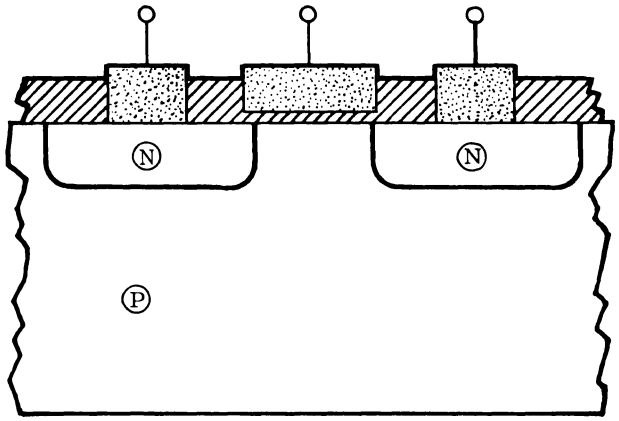
3. When any of these MOSFET's is turned on, current can flow_____.

   A. only when the source is positive with respect to the drain

   B. only when the drain is positive with respect to the source

   C. regardless of the source and drain polarities

(35)



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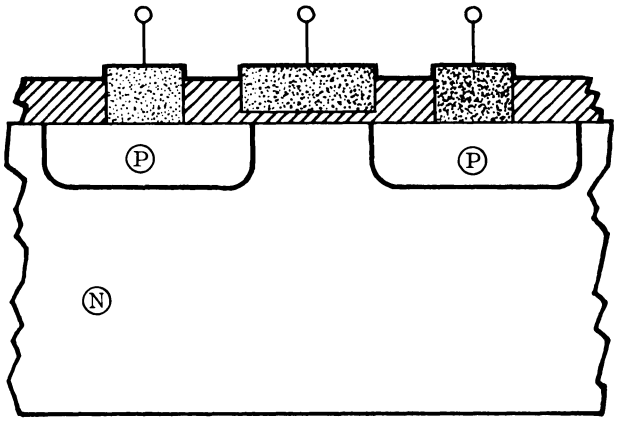

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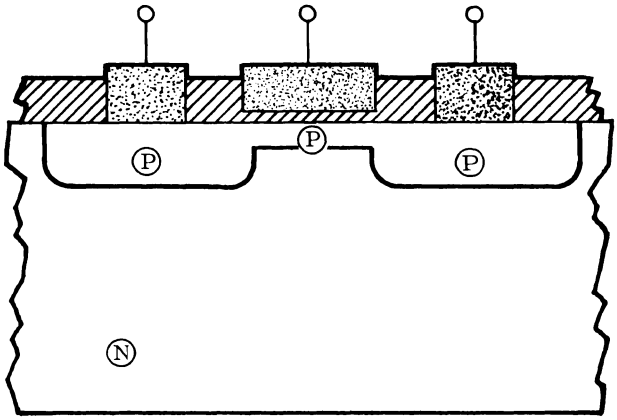

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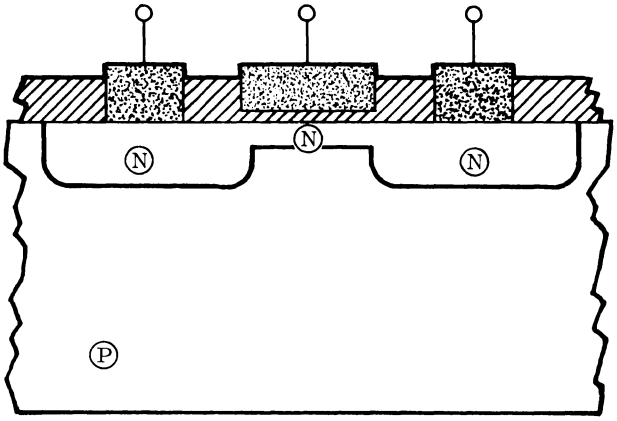


Ⓓ

(35) (continued)

4. Another acronym which can be used interchangeably with MOSFET is _____.

   It stands for _____.

5. For two channels of the same size, a/an _____(N-channel/P-channel) would present a lower resistance.

6. Current through a turned-on MOSFET would have to pass through _____ (0/1/2) P-N junctions.

---

(36) REVIEW ANSWERS

1. A. N-channel enhancement
   off
   on, positive

   B. P-channel enhancement
   off
   on, negative

   C. P-channel depletion
   on
   off, positive

   D. N-channel depletion
   on
   off, negative

2. C. at all times

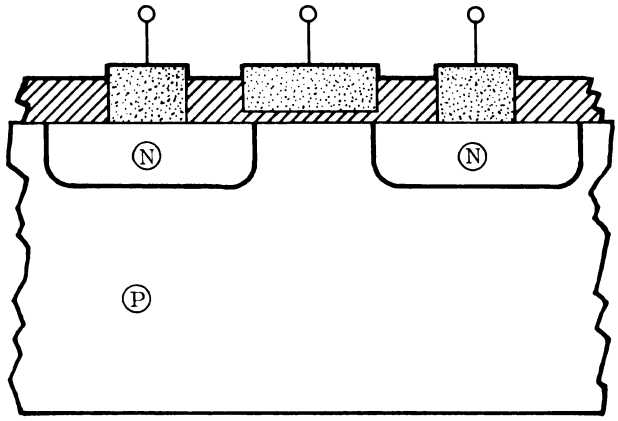
3. C. regardless of the source and drain polarities

4. IGFET
   Insulated Gate FET

5. N-channel

6. 0

(35)
(36)



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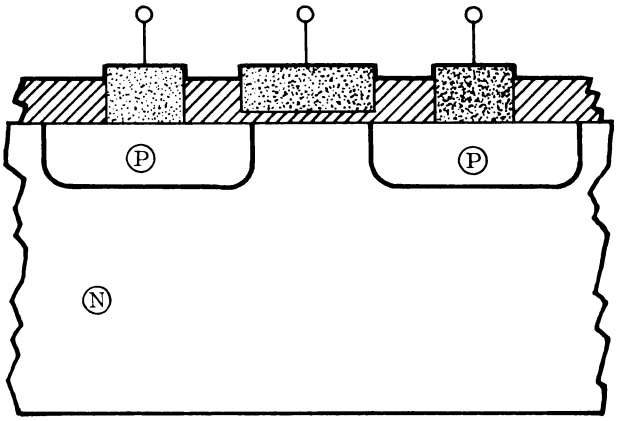

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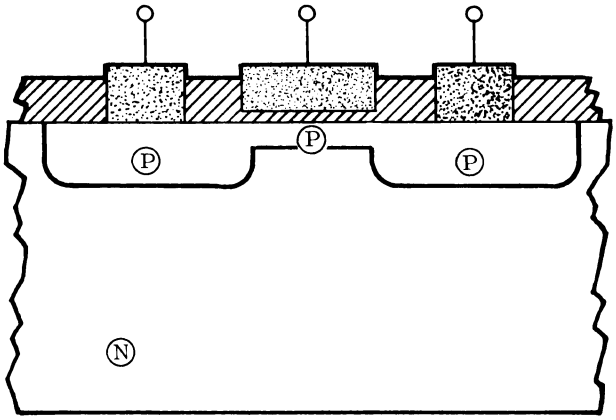

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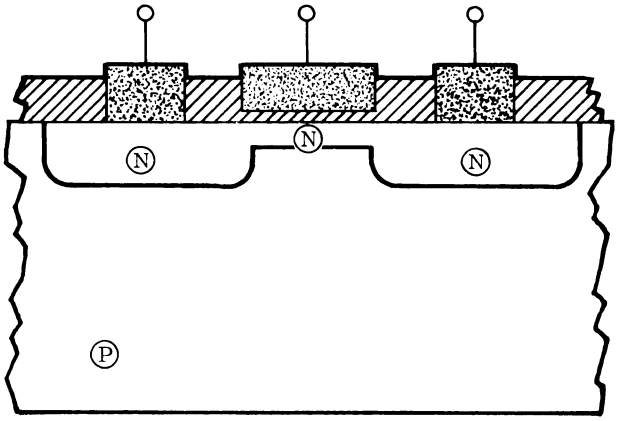


Ⓓ

MOSFET SYMBOLS

(37) There has as yet been no industry-wide standardization of MOSFET symbols. A "general" symbol, often used to represent any of the four types we have discussed, is shown here. Notice that, unlike any of the symbols for bipolar transistors, one of the three elements is not physically connected to the others. This "unconnected" element would be the _____ (source/gate/drain).

---

(38) *gate*

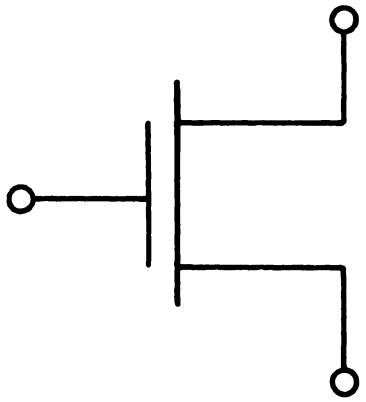
Remember that this separation, or insulation, between the gate and the rest of the MOSFET is one of the major differences between bipolar transistors and MOSFET's. The other two connections, of course, are the source and drain, and the line connecting them (parallel to the gate) represents the channel. When the symbol stands alone as it does here, there is no way of telling which is the drain and which is the source. The only way to distinguish the source from the drain is by looking at the circuit the MOSFET is in. First, though, we need a definition of the terms source and drain. From the names themselves, you would expect current to flow from the _____ to the _____.

---

(39) *source to the drain*

Next, we have to define current flow as it applies to MOSFET's. If only electrons were involved, it would be simple. Current would flow from negative to positive. In MOSFET's, however, holes are current carriers as often as electrons, and they flow from positive to negative. Thus, both the polarity of the applied voltage and the type of current carriers must be taken into account. In a P-channel MOSFET, current flow would be from _____ (positive/negative to _____. In an N-channel MOSFET, current flow would be from _____ to _____.

(37)
(38)
(39)



(40) positive to negative (P-channel)

negative to positive (N-channel)

In a MOSFET, then, the source is defined as the terminal at which the current carriers, whether they are holes or electrons, originate. If the MOSFET shown here was N-channel, terminal _____(2/3) would be the source. If it was a P-channel, terminal_____would be the source.

---

(41) 3 (N-channel)

2 (P-channel)

Thus, you can't tell the source from the drain unless you know what type of MOSFET it is. In addition, unless you know whether it is a depletion or enhancement type, you won't be able to tell what any given gate voltage will do to it. It would therefore seem to be a good idea to use a symbol which allows you to distinguish among the four types of MOSFET's.

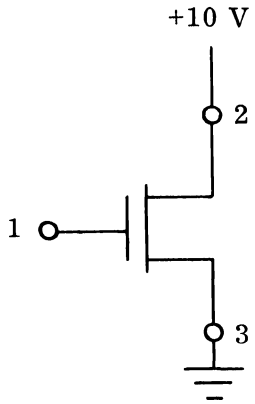
First, let's borrow something from bipolar symbology: an arrowhead. It is used here as a symbol for the substrate. In bipolar symbology, the arrowhead always pointed toward the N-type material. Thus the bipolar transistor shown here would be a PNP. Applying the same logic to the MOSFET symbol, the arrowhead pointing toward the channel means that this is a/an _____ (P-channel/N-channel) MOSFET.

---

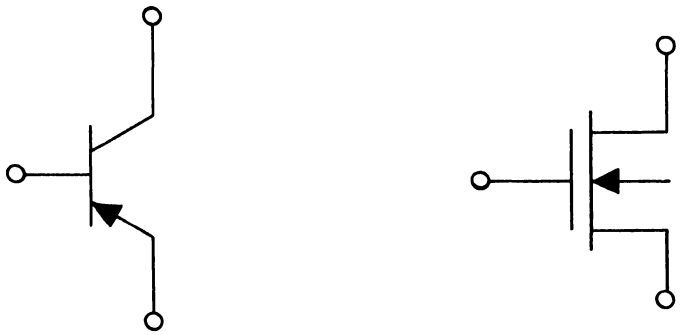
(42) N-channel

Similarly, the symbol shown here, with the arrowhead pointing away from the channel and into the substrate would represent a/an _____ MOSFET.

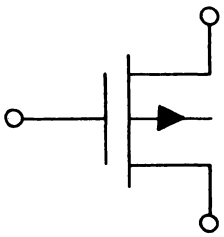
(40)



(41)



(42)



(43) P-channel

The direction of the arrowhead, then, distinguishes between N-channel and P-channel, but what about enhancement and depletion types? The answer is shown here. The symbol on the right is the same P-channel MOSFET we saw in the last frame. The symbol on the left is another P-channel symbol, but notice that the channel in this one is represented by a broken line, indicating the channel is _____ (conducting/not conducting).

---

(44) *not conducting*

If we assume that the symbols represent a "neutral state," i.e., no gate voltage applied, then the symbol with the broken line for the channel would represent a/an_____ (depletion/enhancement) MOSFET.

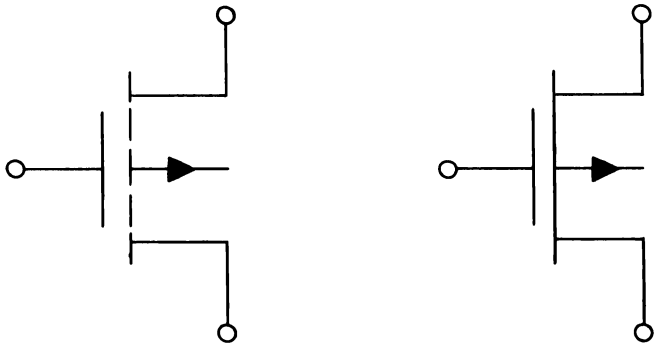
---

(45) *enhancement*

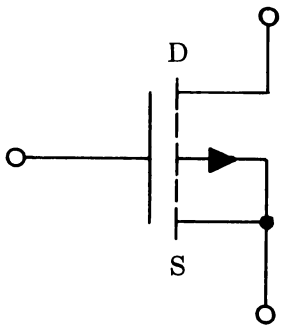
With no gate voltage, an enhancement MOSFET is shut off; the channel is open. Therefore it is represented by a broken line. On the other hand, a depletion type MOSFET with no gate voltage is turned on. The built-in channel provides a current path, and it is therefore represented by a solid line.

Going back to an earlier discussion for a moment, recall that the voltage which turns on a MOSFET is the voltage between the gate and the substrate. This means that we must have a way of indicating what the substrate is connected to. The simplest way of doing this is to use the arrowhead, as shown here. This drawing indicates that the substrate is tied to the _____ .

(43)
(44)



(45)



(46) source

For the present we will show all substrates connected in this way. In reality, the substrates are, more often than not, grounded, but the explanations of MOSFET operation that we will be going through shortly are more easily understood if we assume the substrate is connected to the source. The reason for this will, hopefully, become clear by the time the explanations are completed.

REVIEW

1. Identify each of the four MOSFET's in the illustration (P-channel, N-channel, enhancement, depletion). In each case, indicate which terminal is the source when the MOSFET is connected as shown.

   A. _____

   Source terminal _____

   B. _____

   Source terminal _____

   C. _____

   Source terminal _____

   D. _____

   Source terminal _____

2. The substrate in MOSFET A is _____ (P-type/N-type) material.

3. With no gate voltage, MOSFET A would be turned _____ (on/off). It would be turned _____ (on/off) by a _____ (positive/negative) gate voltage.

---

(47) REVIEW ANSWERS

1. A. *P-channel depletion*
   3

   B. *N-channel enhancement*
   3

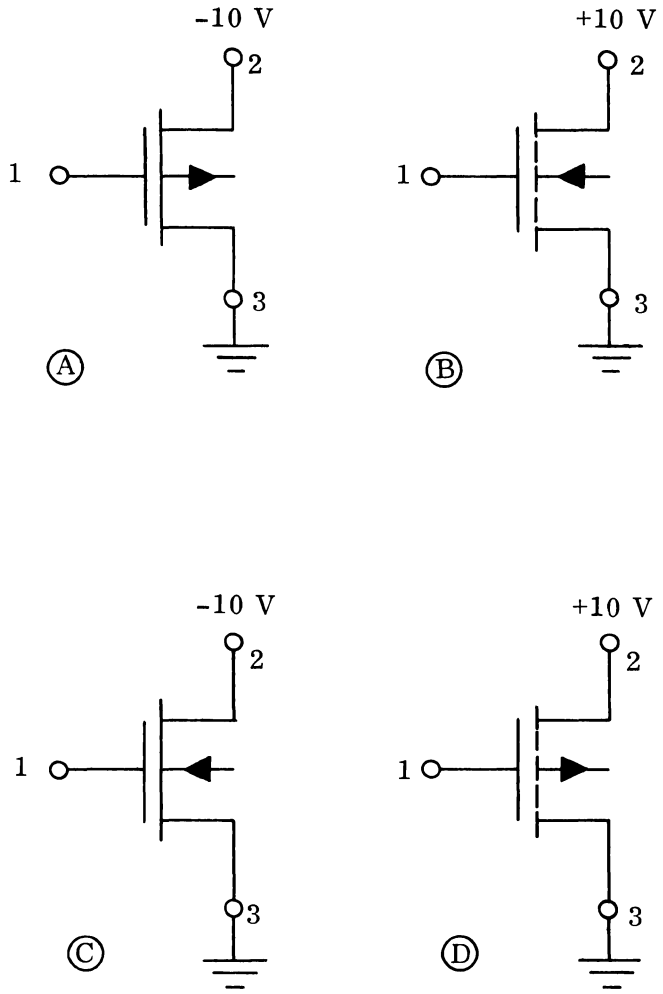
   C. *N-channel depletion*
   3

   D. *P-channel enhancement*
   3

2. *N-type*

3. *on (no gate voltage), off by positive gate voltage*

(46)
(47)



(48) In bipolar logic circuits, the main emphasis was on the different types of logic that were used, such as DTL, CML, TTL, etc. The circuits, such as the one for a TTL NAND gate shown here, were often fairly complex, even though each performed only a single logic function. This TTL gate, for instance, contains five resistors and five transistors to perform a simple NAND function. In MOSFET logic circuits, as we will see shortly, things can be much simpler.

---

(49) Since the P-channel enhancement MOSFET was the first type to be widely used, that is what we will start with. Other types will be introduced as the discussion progresses.

The three basic MOSFET logic circuits are shown here. Assuming negative logic is used, -10 volts represents a logic 1, and 0 volts, or ground, represents a logic 0. This means that if a logic 1 is applied to the input of circuit A, the output would be a logic _____ .

---

(50) 0

The negative voltage on the gate would turn the MOSFET on, shorting the output to ground. This circuit, then, is simply an inverter. Circuit B is a/an _____ _____ (OR/NOR/AND/NAND) gate, and circuit C is a/an_____ gate.

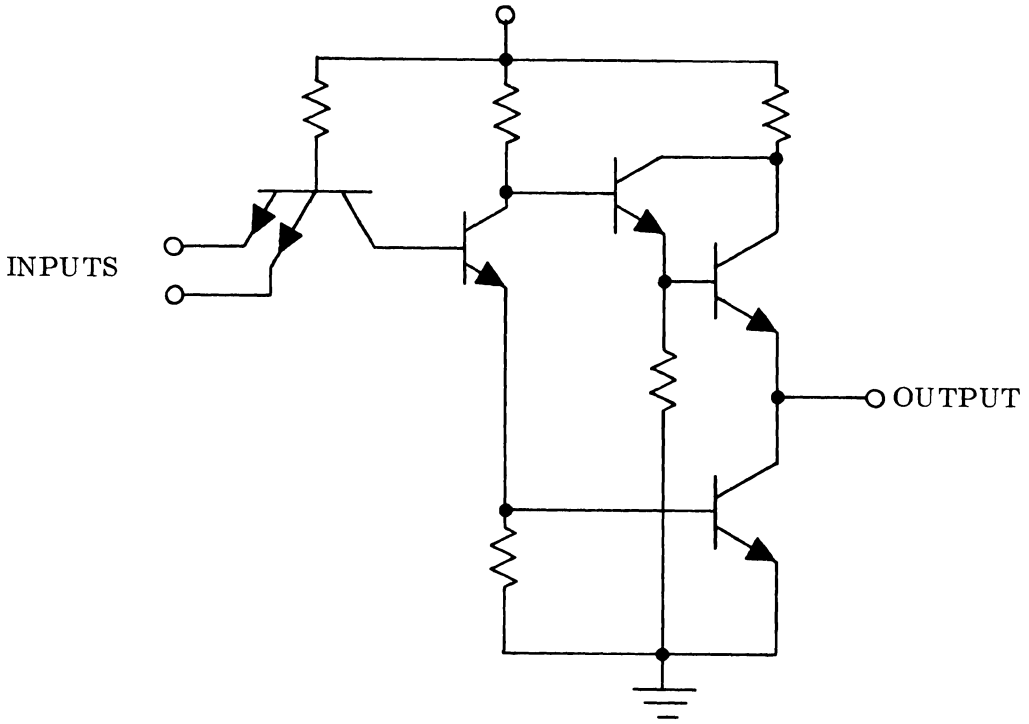
---

(51) NOR

NAND

There are variations on these, some of which we will discuss later, but basically these three circuits are the only ones used extensively. They are often used in complex and extensive combinations, but the overall circuits can usually be broken down into a number of these basic circuits.

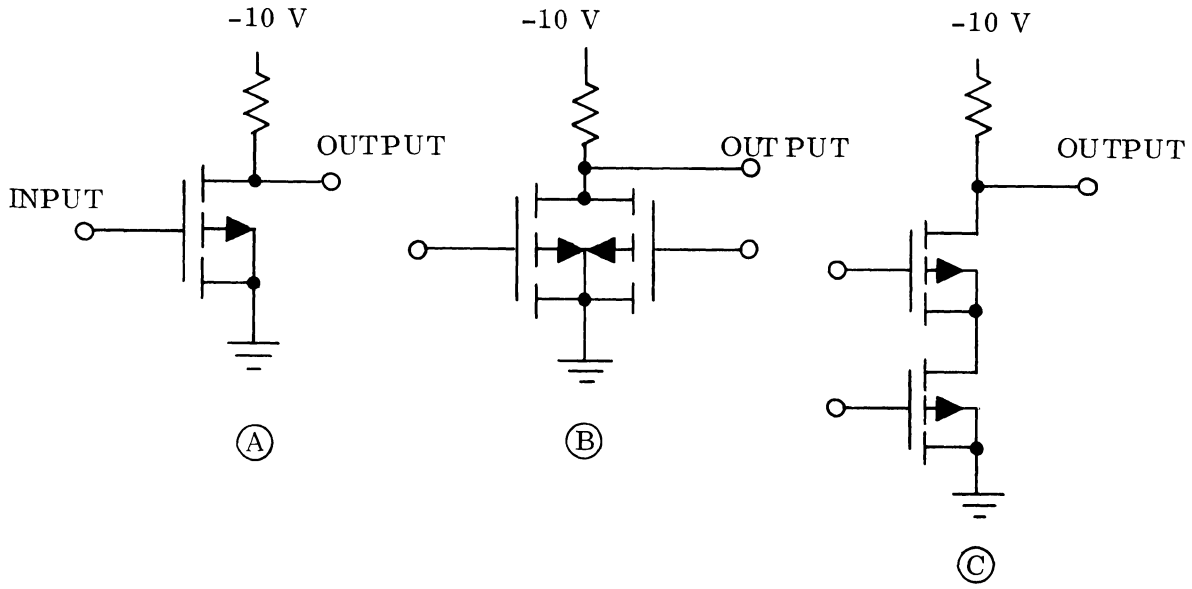
(48)



(49)

(50)

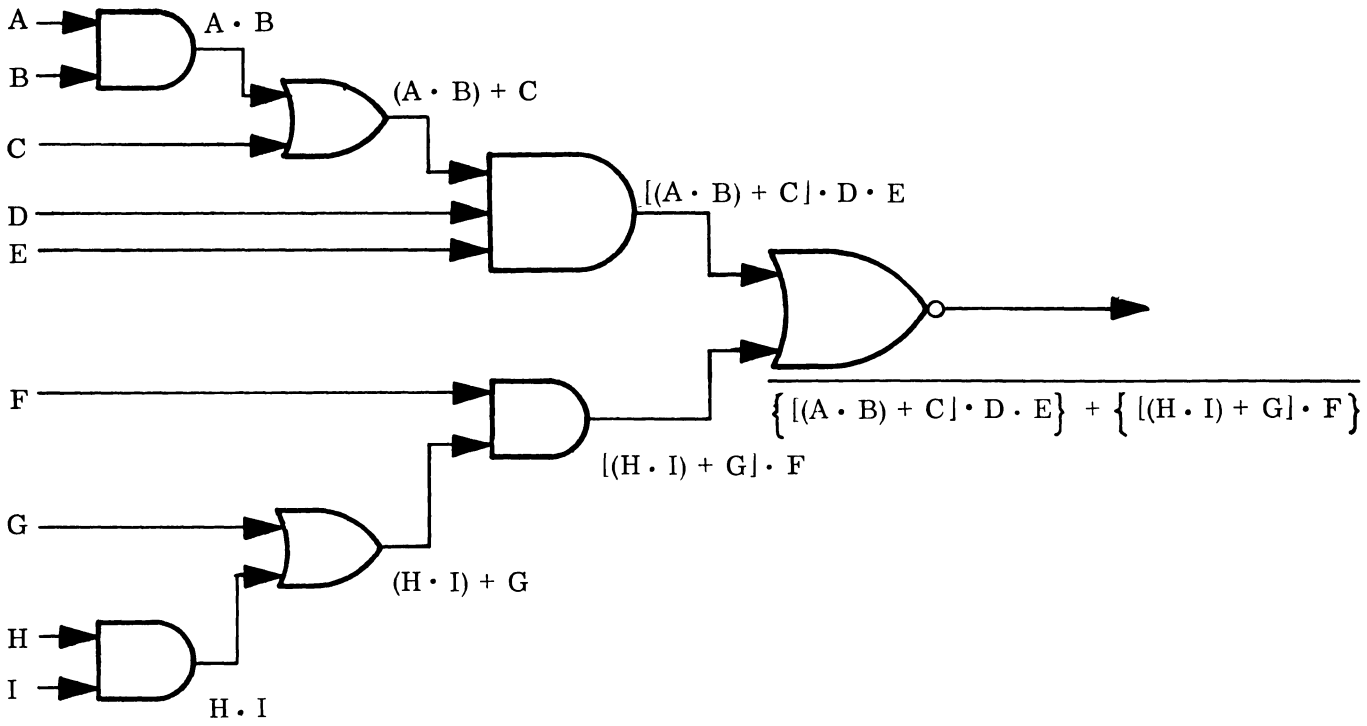
(51)

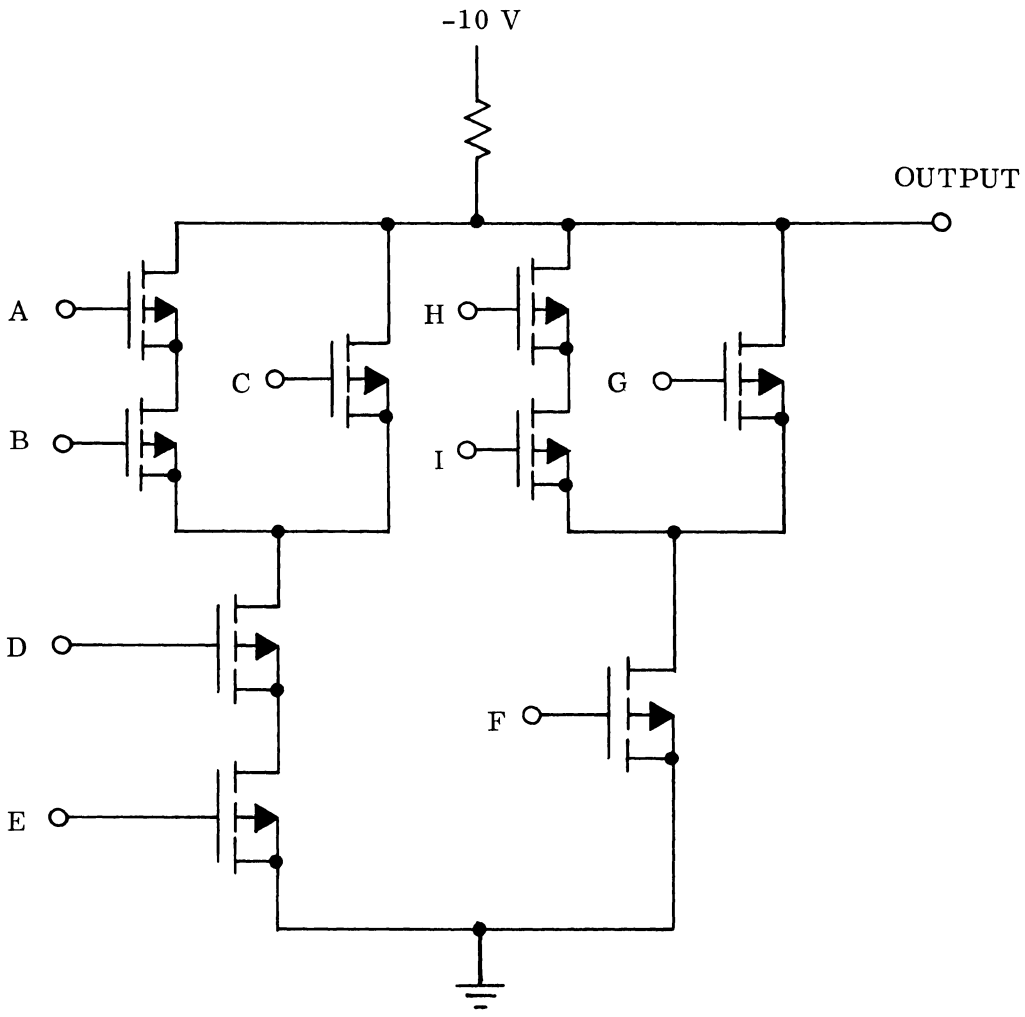


(52) Another important difference between bipolar and MOSFET logic stems from a MOSFET characteristic that was discussed briefly several frames ago. At that time it was pointed out that, given the proper gate voltage, a MOSFET could be made into a short circuit. Its source-to-drain circuit would not have the built-in P-N junction voltage drop that all bipolar emitter-to-collector circuits have. It is this characteristic, plus the fact that the gate is insulated from the source and drain, that allows the NAND gate to operate well. It would be difficult to get two bipolar transistors to operate efficiently as switches when connected in series that way. Several MOSFET's, however, can be connected in series without any great problems. As a result, fairly complex logic functions can be performed by what is essentially a single gate. For instance, the logic diagram shown here can be implemented using the single gate illustrated below it. Each individual input controls a single MOSFET, and each MOSFET can be turned on or off independently.

This type of circuit is possible because a MOSFET gate _____ (does/does not) have to draw current in order to turn the source-to-drain path on, and because there _____ (is/is not) a fixed minimum voltage drop across a turned-on MOSFET.

(52)


A
B
A · B
C
(A · B) + C
D
E
[(A · B) + C] · D · E
F
G
(H · I) + G
H
I
H · I
[(H · I) + G] · F
{[(A · B) + C] · D · E} + {[(H · I) + G] · F}


-10 V
OUTPUT
A
B
C
H
I
G
D
E
F

(53) does not

is not

Now let's go back to the simplest of our basic circuits, the inverter, and look at it in a little more detail. First, notice that there is one MOSFET and one resistor in the circuit. The circuit could probably be made physically smaller if the _____ was replaced by another _____ .

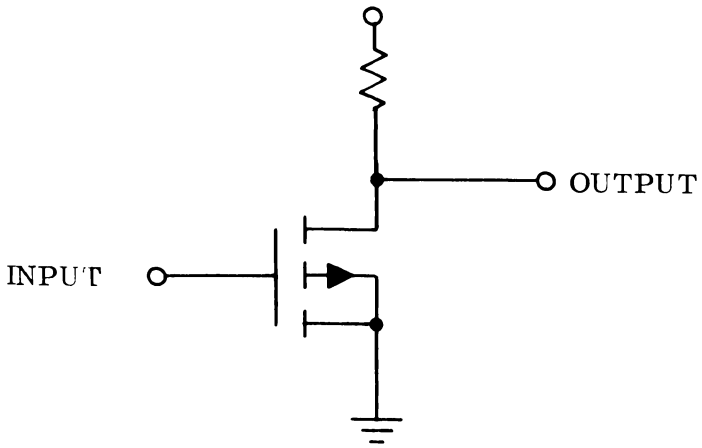
---

(54) *resistor*

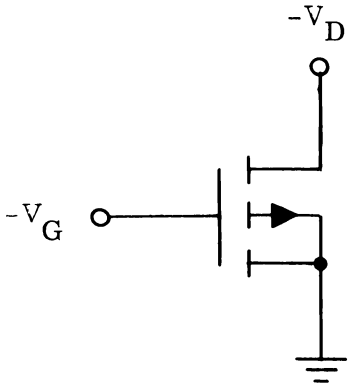
MOSFET or transistor

As was pointed out in the text on bipolar integrated circuits, resistors are rarely used when one or more transistors can be used to perform the same function. The same principle holds true for MOSFET's, only more so. For one thing, the size advantage of MOSFET's over resistors is even greater than that of bipolar transistors over resistors. For another, a resistor can usually be replaced by a single MOSFET rather than by a complete circuit. To see why, let's look at the operating characteristics of a MOSFET. We will use a P-channel enhancement MOSFET such as the one shown here. Notice that a negative drain voltage (V_D) and a negative gate voltage (V_G) have been applied. The resistance offered by this MOSFET would depend primarily on the (drain/gate) voltage.

(53)



(54)



(55) gate

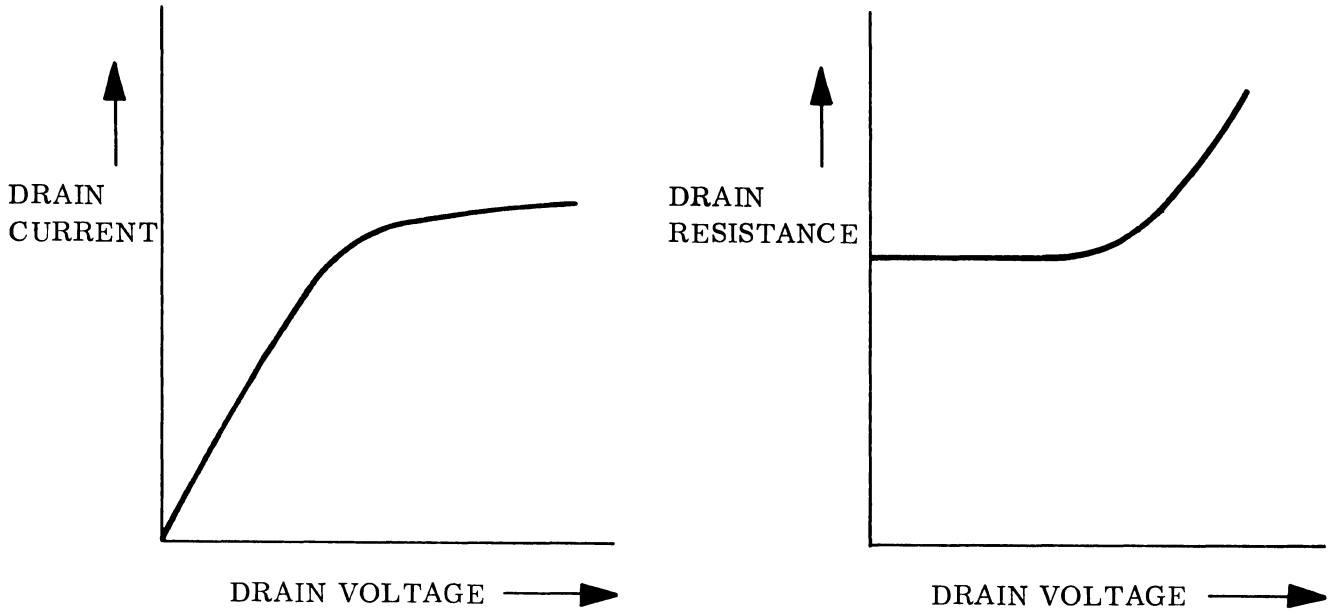
This is much like the grid voltage in a triode vacuum tube. With the gate-to-substrate voltage held constant at $-V_G$, the source-to-drain path acts like a fixed resistor — up to a point. Assuming the gate voltage is greater than the MOSFET's threshold voltage, the curves shown here indicate roughly what will happen. As long as the drain-to-source voltage is relatively low, the current increases more or less linearly as the drain-to-source voltage increases. Throughout this range, then, the resistance of the source-to-drain path remains fairly constant. Once this range is exceeded, however, the channel induced by gate voltage becomes saturated and the current levels off. In effect, the resistance begins to rise. If the gate voltage were higher, you would expect the induced channel to saturate at _____ (a higher/a lower/the same) level.

---

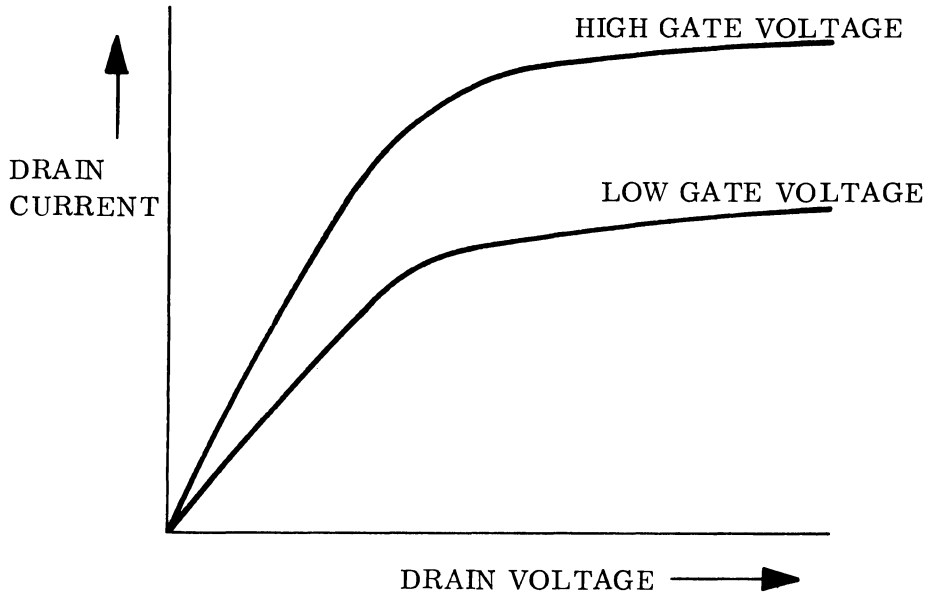
(56) a higher level

The higher gate voltage would cause a deeper conduction channel to be formed, allowing more current to flow. Not only would the saturation current be greater, but the current for any given drain voltage would also be greater, as shown in these curves. The effective resistance of the MOSFET with the higher gate voltage would be _____ (higher/lower/unchanged).

(55)


DRAIN
CURRENT
DRAIN VOLTAGE
DRAIN
RESISTANCE
DRAIN VOLTAGE

(56)


HIGH GATE VOLTAGE
LOW GATE VOLTAGE
DRAIN
CURRENT
DRAIN VOLTAGE

(57) lower

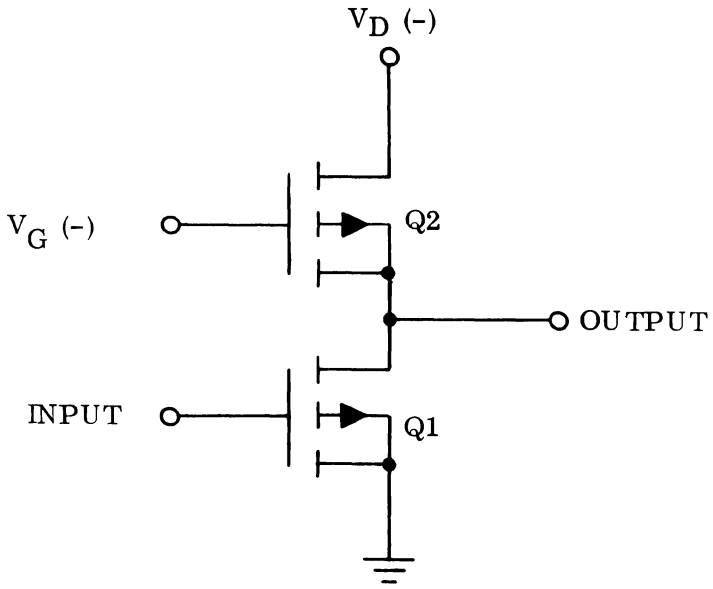
Now let's see what some of the differences are between a resistor and a MOSFET being used as a resistor. To start with, we will look at one of the basic MOSFET logic circuits, the inverter. In the inverter shown here, _____ (Q1/Q2) is being used as a resistor.

---

(58) Q2

Precisely what happens in this circuit depends on a number of things, including the various voltage levels. To simplify the situation, we will assume that the drain supply voltage (V_D), the gate supply voltage (V_G), and the logic 1 voltage are all equal. If a logic 1 is applied to the Q1 gate, Q1 will be turned on heavily, and its drain voltage will begin to drop. Since the source and substrate of Q2 are both tied to the drain of Q1, the voltage there will also begin to drop. This means that the gate-to-substrate voltage of Q2 will _____ (increase/decrease).

(57)
(58)



(59) increase

Thus, turning Q1 on tends to turn Q2 on as well. As long as there is a voltage drop across Q1, however, the Q2 gate-to-substrate voltage will always be somewhat _____ (less/greater) than the Q1 gate-to-substrate voltage.

---

(60) less

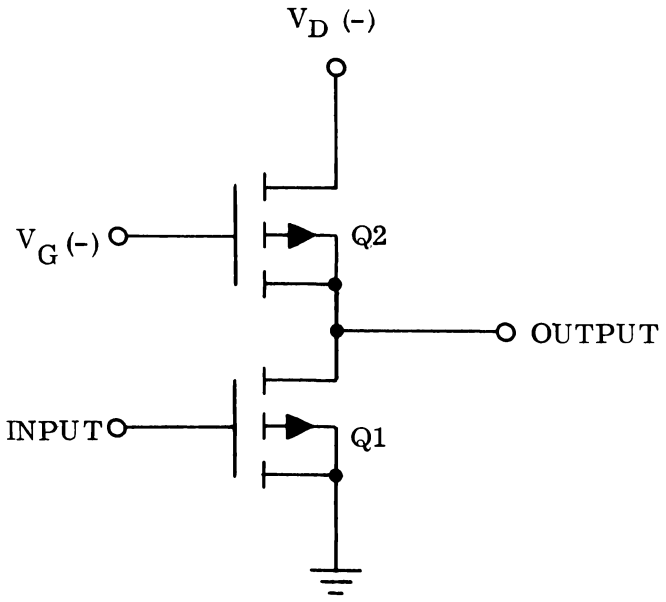
Thus, the resistance offered by Q2 would be somewhat greater than that offered by Q1. At some point, a balance would be reached and the output voltage would level off. At that balance point, the output would be closer to _____ (V_D/ground) than to _____.

---

(61) closer to ground than to V_D

Ideally, though, the output should be very close to ground. If Q1 and Q2 are physically identical, this will never happen. The balance will be reached at some point well above ground. To avoid this problem, Q1 and Q2 should be constructed so that Q1 has a much _____ (higher/lower) saturation current and therefore a much _____ (higher/lower) resistance.

(59)
(60)
(61)



(62) higher (saturation current)

lower (resistance)

In practice, with the same gate voltage, Q2 would have roughly 20 times the resistance of Q1. This means that Q1 can be considered to act like a switch, being opened and closed by the voltage applied to its gate. As we have just seen, a logic 1 will produce an output voltage that is very nearly zero. But now let's see what happens when a logic 0 is applied to the Q1 gate. Q1 would be turned off, and the circuit could be represented as shown here. The capacitor connected to the output represents the gate capacitance of the MOSFET circuit being driven by the inverter. As this capacitor charges up, the gate-to-substrate voltage of Q2 will _____ (increase/decrease).

---

(63) decrease

This is just the reverse of what happened when Q1 was turned on. The voltage on the substrate and source of Q2 is increasing while the gate voltage remains constant. If the Q2 gate-to-substrate voltage drops below the threshold voltage, Q2 will be _____ (turned on more heavily/turned off).

---

(64) turned off

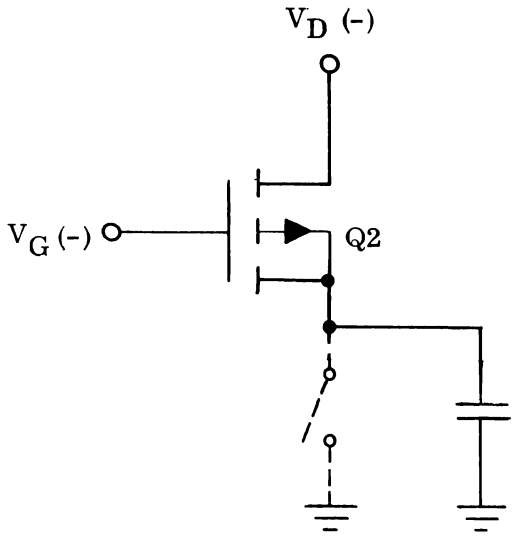
With Q2 turned off, the capacitor will stop charging and the voltage will level off. If the Q2 threshold voltage (V_{TH}) is -4 volts and V_G and V_D are both -10 volts, the voltage across the capacitor will level off at _____volts.

---

(65) -6

At that level, the gate, at -10 volts, is one threshold voltage away from the substrate, at -6 volts. If the capacitor were replaced by a resistor, the output voltage _____ (would/would not) level off at approximately the same value.

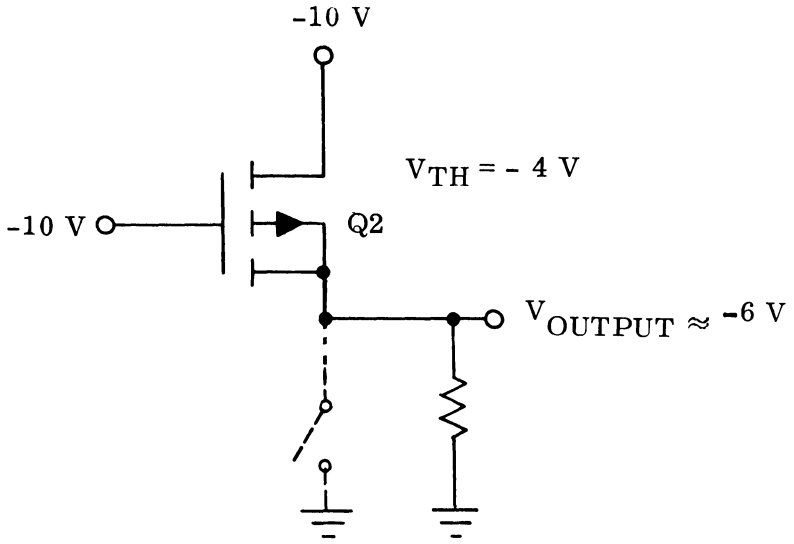
(62)
(63)
(64)
(65)



(66) would

The voltage across the resistor would probably be slightly lower than that across the capacitor, but not much. The voltage across the capacitor would build up until Q2 was completely cut off, and the capacitor would retain its charge and keep Q2 cut off. The voltage across the resistor, on the other hand, would stop building up before Q2 was cut off. If the resistor were 100 kilohms, for example, the balance would be reached at a current level of about 0.06 milliampere, which would provide the necessary -6 volts on the Q2 source and substrate. In most cases, the difference between the voltage across the capacitor and the voltage across the resistor would be small. In either situation, the source voltage is going to build up to a level that is approximately one threshold voltage away from the _____ (source/gate/drain) voltage.

(66)



(67) gate

V_D and V_G have, until now, been kept at the same value. Aside from simplicity, one reason for doing this is that the same power supply can then be used for both, and it is more economical to use one power supply than it is to use two. With V_D and V_G equal, however, the highest voltage you can get at the output is $V_D - V_{TH}$. But what if you want to get the complete V_D at the output? There is one fairly simple (but costly) solution: Use separate power supplies for V_D and V_G. Assuming Q2 still has a threshold voltage of -4 volts, in order to get -10 volts at the output, you would have to raise _____ (V_D/V_G) to _____ volts.

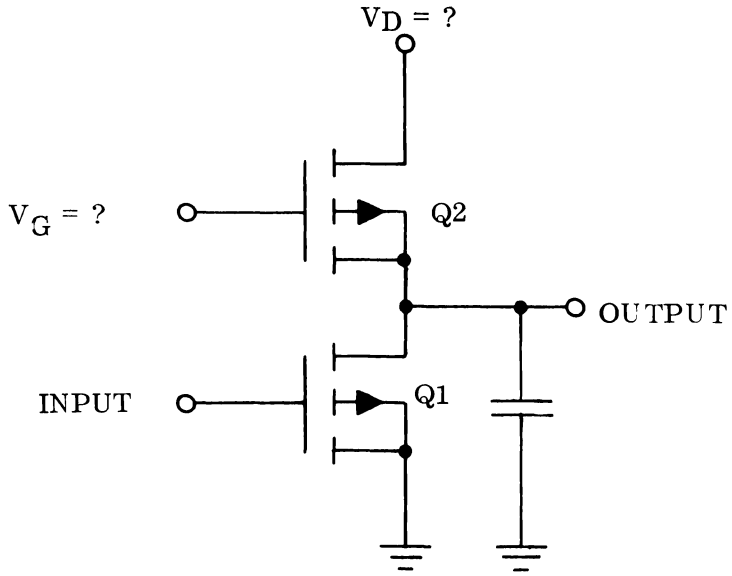
---

(68) V_G

-14

With V_G at -14 volts, the output voltage could rise to -10 volts before the Q2 threshold voltage was approached. If V_D were increased to -12 volts and V_G to -20 volts, the maximum output voltage would be _____ volts.

(67)
(68)



(69) -12

REVIEW

1. Name the three basic MOSFET logic circuits.

   _____

   _____

   _____

2. In the illustrated circuit, _____(Q1/Q2) is being used as a resistor.

3. Given equal gate-to-substrate voltages, which of the MOSFET's in the illustration would offer the lower resistance? _____

4. Assume a Q2 threshold voltage of -3 volts, a V_G of -10, and a V_D of -15. What would the maximum possible output voltage be?_____

5. What would the maximum possible output voltage be if the V_G and V_D values in question 4 were interchanged? _____

---

(70) REVIEW ANSWERS

1. Inverter, NOR gate, NAND gate

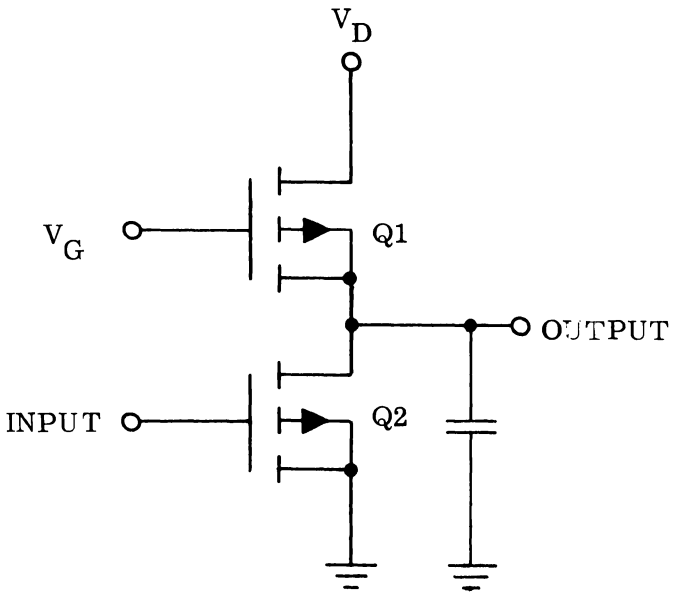
2. Q1

3. Q2

4. -7 volts

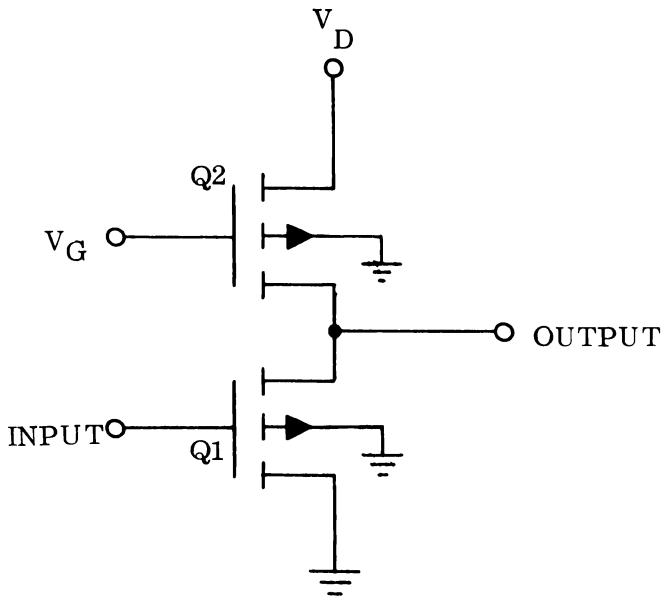
5. -10 volts

(69)
(70)



(71) As we pointed out several frames ago, we have been taking a couple of liberties with the facts for the sake of simplicity. Now it's time to set them straight. First, we have said that it is the gate-to-substrate voltage which determines when a MOSFET turns on or off. Second, we have shown all MOSFET's with their substrates tied to their sources. The fact is, the substrates in most integrated circuits are grounded, so the inverter we have been discussing would actually look like this. Now, if our other statement, about the gate-to-substrate voltage, were completely true instead of "sort of true," it would seem that grounding the substrate in this way would eliminate the threshold voltage problem we have been discussing. That is, when Q1 is turned off and the Q2 source voltage is rising, the substrate would remain at ground level. It would seem only logical, then, for the gate-to-substrate voltage to remain constant, and for the output voltage not to level off as the output voltage approaches V_G. The output voltage does level off, however, and it levels off at roughly the same point it did in the circuits in which the substrates were tied to the sources.

(71)



(72) To see why this leveling off still occurs, we have to look at the physical structure of the MOSFET again. Notice the induced channel between the drain and source. Since this channel forms a current-carrying path between the source and drain, it would have to be at _____ (ground level/roughly the same level as the source and drain).

---

(73) *roughly the same level as the source and drain*

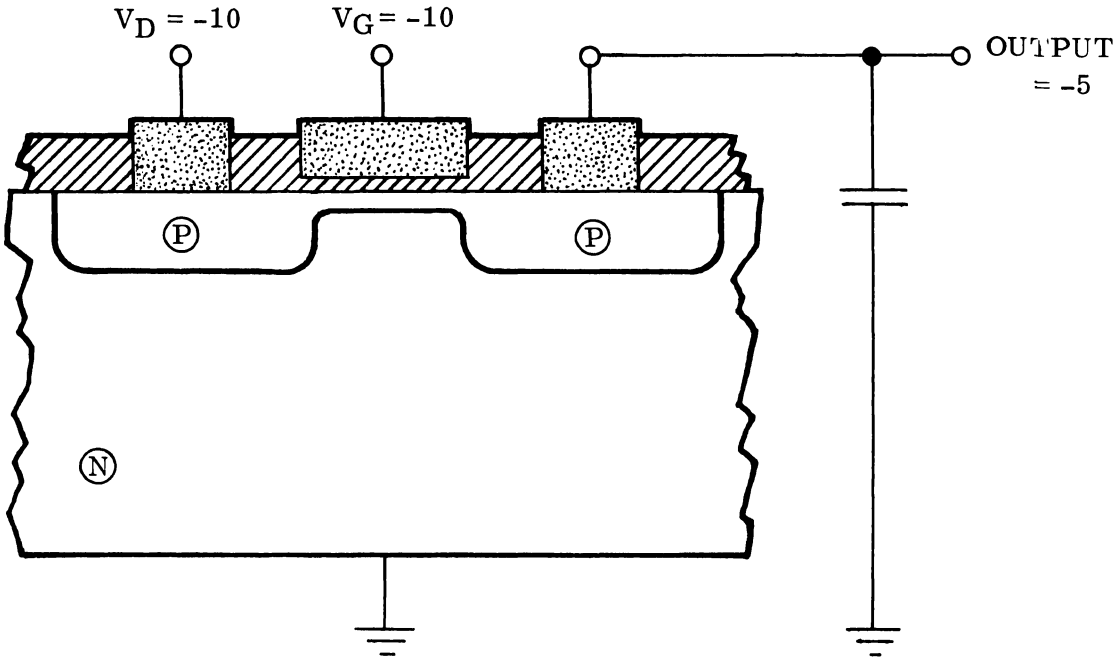
The channel is, in effect, a resistor connected between the source and drain, isolated from the rest of the substrate by a P-N junction. The source end of the channel would, in this case, be at -5 volts and the drain end at -10. Thus, whether the bulk of the substrate is grounded or tied to the source, that part of the substrate on which the gate voltage acts (the induced channel) will be at roughly the same voltage level as the source and drain. Raising the drain voltage would have little effect, largely because this would make the drain end of the channel negative with respect to the gate, which would simply raise the already high resistance of the channel even higher. Thus it would seem that, in reality, a MOSFET is turned on or off by the voltage between the gate and the _____(drain/source/substrate).

---

(74) *source*

That is, the threshold voltage we have been discussing is, technically, the gate-to-source voltage rather than the gate-to-substrate voltage. This is, of course, a simplified way of looking at it, but, for purposes of circuit analysis, it will work fairly well. In reality, the threshold (i.e., gate-to-source threshold) voltage will itself vary, depending on what the source-to-substrate voltage is. For instance, the threshold voltage of the MOSFET we have been discussing would be raised if the substrate, instead of being grounded, were connected to +5 volts. Similarly, it would be lowered if the substrate were connected to -5 volts. The formulas used to compute these variations, however, as well as the detailed reasons for the variations, are beyond the scope of this text. And, as we said, this relatively simple definition will be adequate for our purposes.

(72)
(73)
(74)



(75) Now that the definition of threshold voltage is somewhat straightened out, let's go back to the inverter circuit and look at it a little more closely. Recall that the last thing we did to it was to provide separate V_G and V_D power supplies. To simplify matters, we will say that the V_G supply is nominally -15 volts, the V_D supply -10 volts, and V_{TH} -5 volts.

One item to consider in any integrated circuit, but particularly in MOSFET circuits, is power consumption — the lower the better. As long as Q1 is turned off, there is no problem. The only current drawn by the inverter is the leakage current through Q1 and the current necessary to charge the gate capacitance of the next stage. But what about the opposite state, when Q1 is turned on? Both Q1 and Q2 are turned on, but, because of the differences in construction between the two MOSFET's, one of them will saturate at a much lower current level than the other. The MOSFET which will saturate at the lower current level is_____(Q1/Q2).

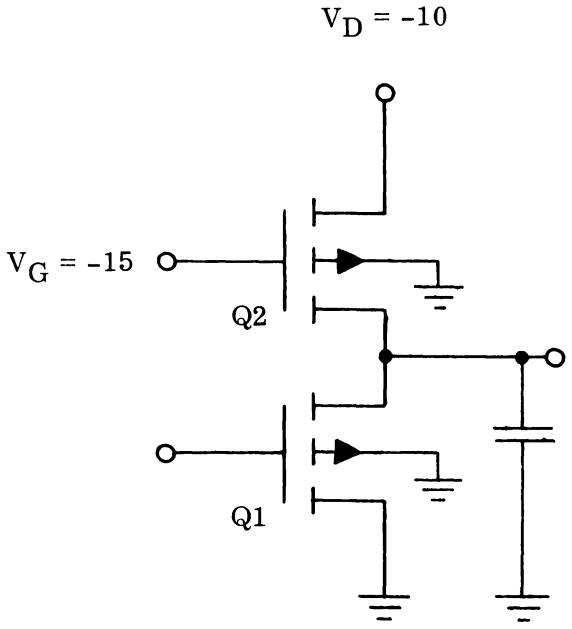
---

(76) Q2

The driver MOSFET, Q1, is constructed so that, for any given gate voltage, it would be essentially a short circuit when compared to Q2. With the two in series, then, Q2 will saturate at relatively low current, thereby limiting the current through both itself and Q1.

The question now is, at what level does Q2 saturate? Keep in mind that the Q2 gate voltage has been raised to -15 volts in order to allow the full V_D (-15 volts) to be coupled to the output when Q1 is off. In the first configuration of our inverter, the Q2 gate voltage was only -10 volts. Of the two configurations, which would draw the most current during the time Q1 is turned on, the one in which -15 volts is on the Q2 gate or the one in which -10 volts is on the Q2 gate? _____

(75)
(76)



(77) The one in which -15 volts is on the Q2 gate.

The higher the gate voltage, the higher the saturation current. With a higher saturation current, of course, this configuration would have a higher power consumption. Thus, changing V_G from -10 volts to -15 volts has resulted in one advantage and two disadvantages. List them.

Advantage _____

Disadvantages _____

_____

---

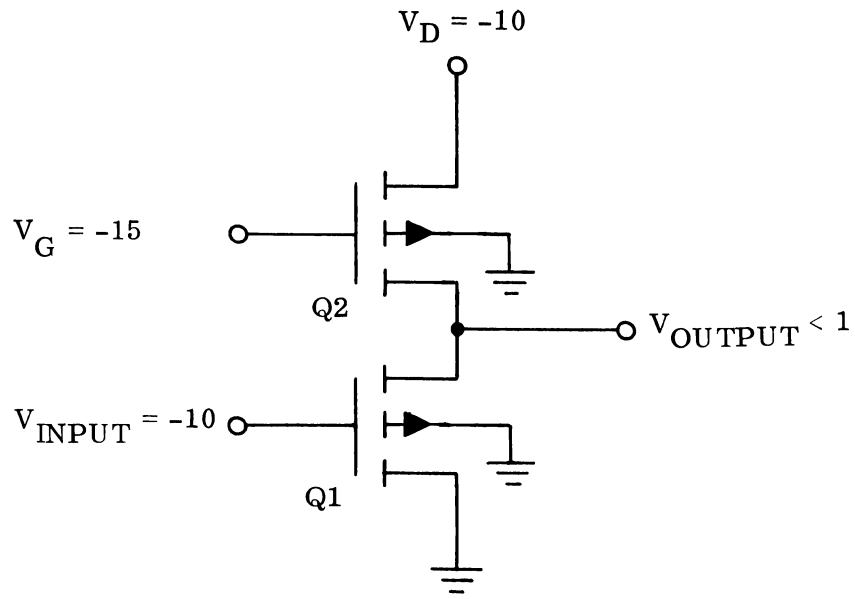
(78) *Advantage: Full V_D available at output.*

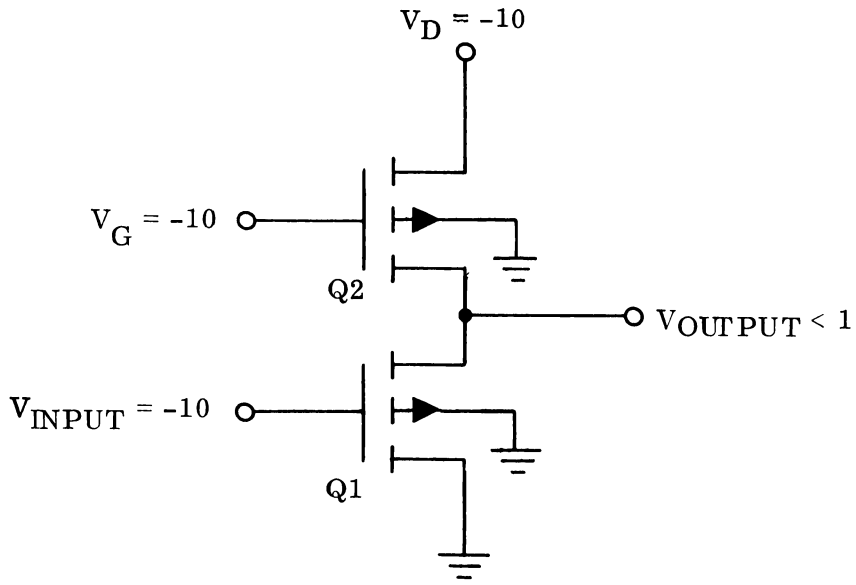
Disadvantages: Two power supplies needed.

Higher power consumption.

In addition, both configurations share a disadvantage in the way they respond to supply voltage variations. To see what this shared disadvantage is, you first have to realize that, no matter how heavily Q1 is turned on, a certain amount of resistance remains, and that there is a certain voltage drop across this resistance. Remember, this is strictly a resistive voltage drop, not a P-N junction drop such as that which occurs in bipolar transistors. Because it is resistive, it can become quite low for a fully turned-on MOSFET, but it cannot be eliminated entirely. As long as this resistance exists, the output cannot go completely to zero. This means that, if the current through the MOSFET increases, the output voltage of the circuit will _____ (go up/go down/remain unchanged).

(77)
(78)


$V_D = -10$
$V_G = -15$
Q2
$V_{OUTPUT} < 1$
$V_{INPUT} = -10$
Q1


$V_D = -10$
$V_G = -10$
Q2
$V_{OUTPUT} < 1$
$V_{INPUT} = -10$
Q1

(79) go up

Assume that, for the next circuit to recognize this circuit's output as a logic 0, the output must be less than 1 volt. Also assume that the output of both configurations in the illustration is slightly less than 1 volt. If the gate voltage on Q2 in either configuration increased, the current through Q1 would _____ (increase/decrease/remain unchanged).

---

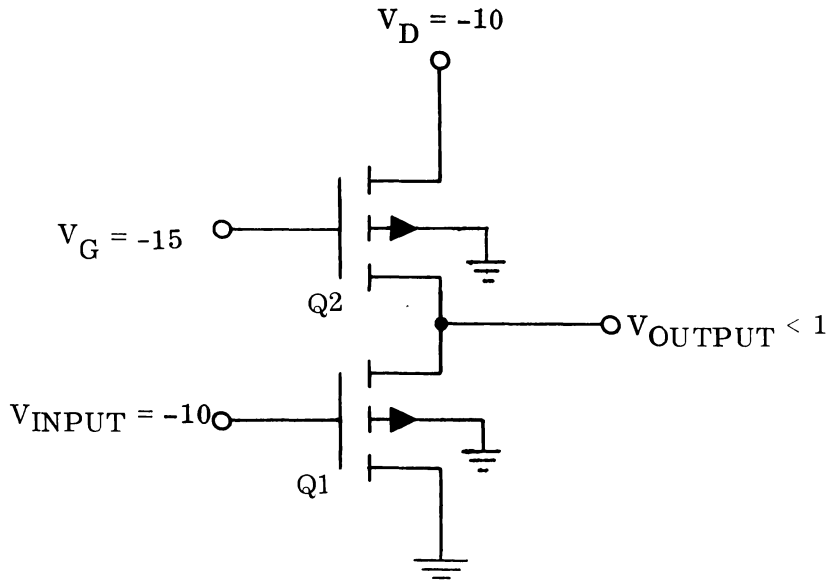
(80) increase

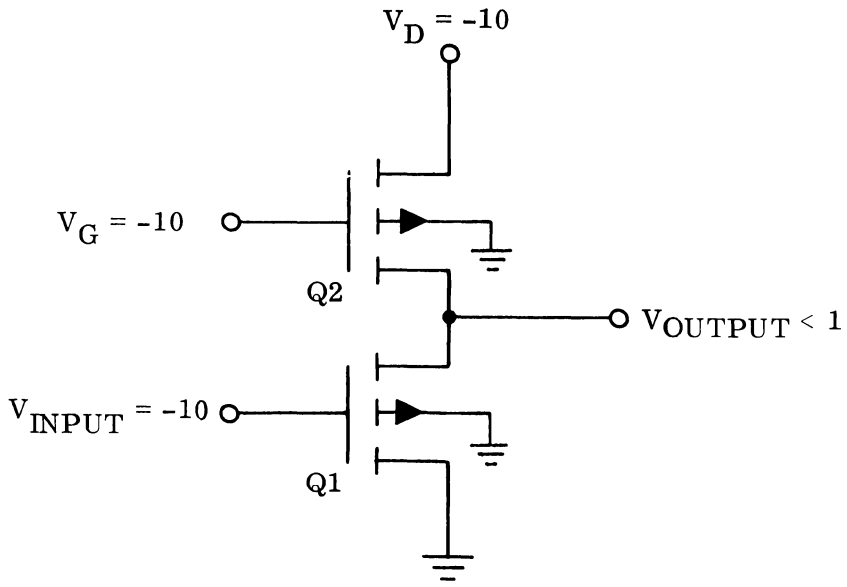
The increased current would raise the voltage drop across Q1, possibly enough to drive the output voltage above the required logic 0 level. Thus, either of the configurations we have been discussing would be particularly susceptible to variations in supply voltage or transient voltages (noise). Any variation, whether momentary or long term, could cause the output to switch from a logic 0 to a logic 1.

Similarly, supply voltage variations or noise which occur while Q1 is turned off could cause the level of the logic 1 output to vary. However, unless the variations are extreme enough to knock the output down to less than 1 or 2 volts, which is the normal switchover point between logic 1 and logic 0, this can be ignored.

The inverter we have been discussing is susceptible to noise problems only for logic _____(1/0) outputs.

(79)
(80)


$V_D = -10$
$V_G = -15$
Q2
$V_{OUTPUT} < 1$
$V_{INPUT} = -10$
Q1


$V_D = -10$
$V_G = -10$
Q2
$V_{OUTPUT} < 1$
$V_{INPUT} = -10$
Q1

(81) 0

One way of getting around the disadvantages we have been discussing is to substitute a depletion MOSFET for the enhancement MOSFET we have been using as a resistor. Before we try it, however, let's take a look at the operation of a depletion MOSFET in light of what we have been finding out about enhancement MOSFET's. Recall first that a P-channel depletion MOSFET is turned on while its gate voltage is zero and is pinched off when the gate voltage goes _____ (positive/negative).

---

(82) *positive*

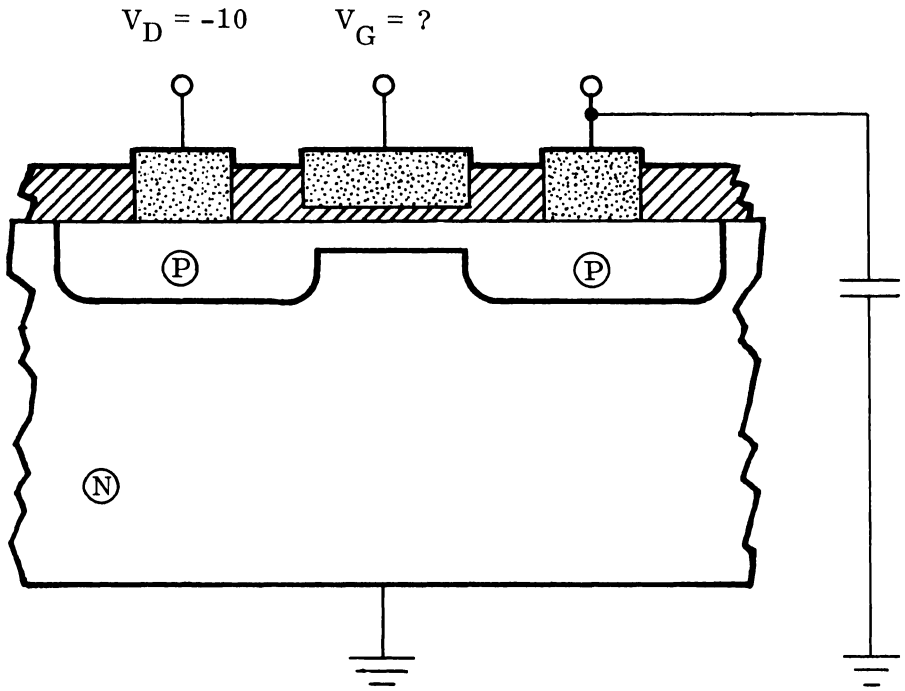
A positive gate voltage repels the holes and attracts the electrons, creating an N-type area within the built-in P-channel. When the voltage is positive enough, the N-type area (or depletion zone) fills the P-channel and pinches off the current. The built-in P-channel in a depletion MOSFET would be at roughly the same voltage level as the _____ (source and drain/substrate).

---

(83) *source and drain*

The same situation exists in an enhancement MOSFET. The P-channel is connected between the source and drain and isolated from the substrate by a P-N junction. Thus, as in the enhancement MOSFET, all gate voltages, including the pinch-off voltage, would be measured with respect to the _____ (substrate/source/drain).

(81)
(82)
(83)



(84) source

Now let's put a depletion MOSFET into the inverter circuit and see what happens. Notice first that the gate of the depletion MOSFET is tied to the _____ .

---

(85) source

This means we have already eliminated one of the disadvantages discussed earlier, the need for two power supplies. Only one power supply, V_D, is needed here.

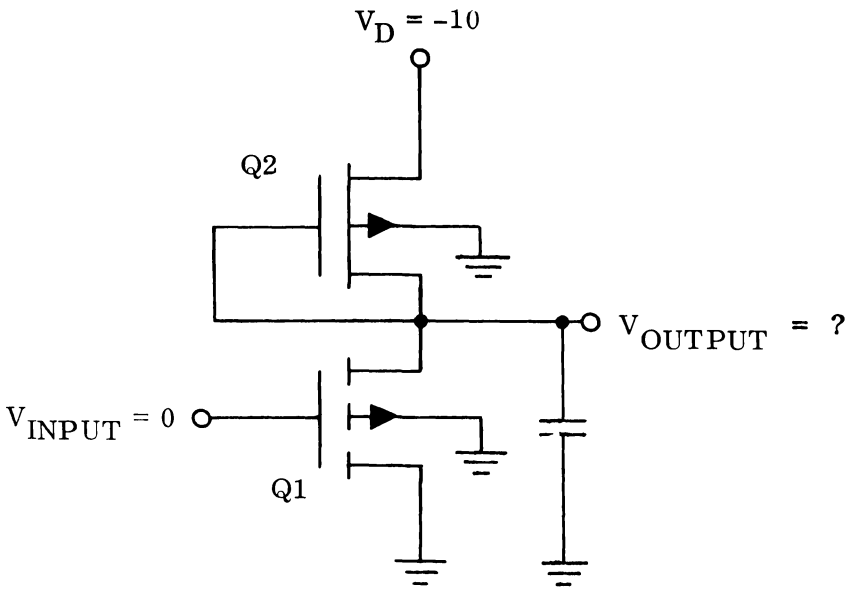
Let's start with the situation in which Q1 is turned off and the output is driving another gate. As the gate capacitance of the next stage is charged and the output of the inverter goes up, the gate-to-source voltage of Q2 will, of course, remain at zero since the gate and source are tied together. Thus, as the output approaches the level of V_D, Q2 _____ (will/will not) be approaching pinch-off.

---

(86) will not

Q2 will remain turned on regardless of the output level, which means that the inverter output _____ (can/cannot) reach the level of V_D.

(84)
(85)
(86)



(87) can

So, even with only one power supply, the full V_D can be coupled through to the output when a logic 1 output is called for.

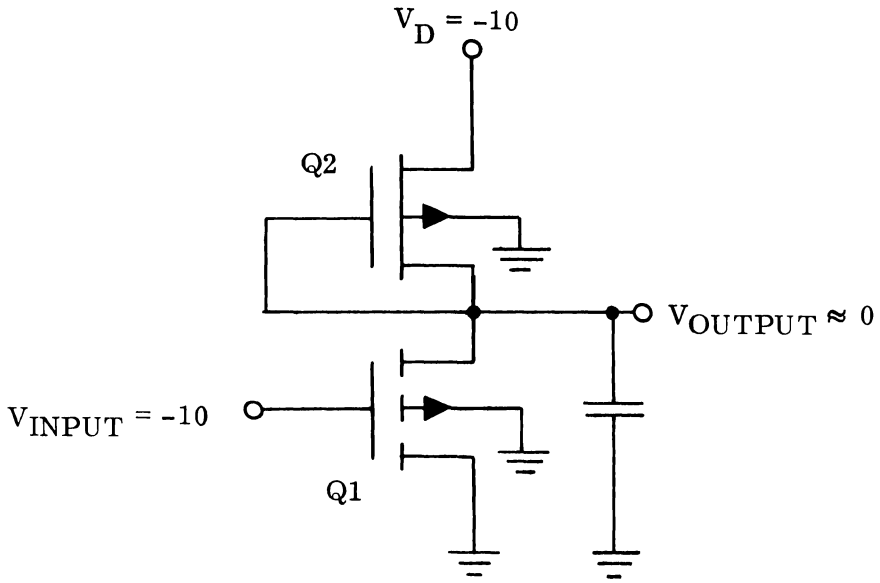
Now, what about the power consumption? Recall that power consumption was highest for logic 0 outputs. In either of the enhancement configurations, Q2 was turned on more heavily for a logic 0 output than for a logic 1 output. This was simply because the gate voltage was constant and the gate-to-source voltage therefore varied greatly, reaching its maximum value when the output was a logic _____(1/0).

---

(88) 0

With a depletion MOSFET, however, the gate voltage varies along with the source voltage, and the gate-to-source voltage itself remains a constant 0 volts regardless of the output voltage. This means, of course, that the depletion MOSFET is turned on no more heavily for a logic 0 output than for a logic 1 output. Thus, it would seem only logical that, for logic 0 outputs, an inverter using a depletion MOSFET as a resistor would draw _____ (more/less) current than an inverter using an enhancement MOSFET.

(87)
(88)



(89) less

Less current, of course, means less power consumption.

Finally, let's see what happens when the V_D supply fluctuates. As before, we will be concerned only with what happens when the output is a logic 0. To see what happens, we will have to look at a curve of the drain current versus drain voltage, shown here. Notice first that, for 0 gate voltage, the MOSFET saturates at a drain voltage which is fairly low when compared to the value of V_D. This means that, if the V_D supply voltage dropped to -5 volts, say, the current through Q1 in the inverter would be _____ (doubled/halved/virtually unchanged).

---

(90) *virtually uncharged*

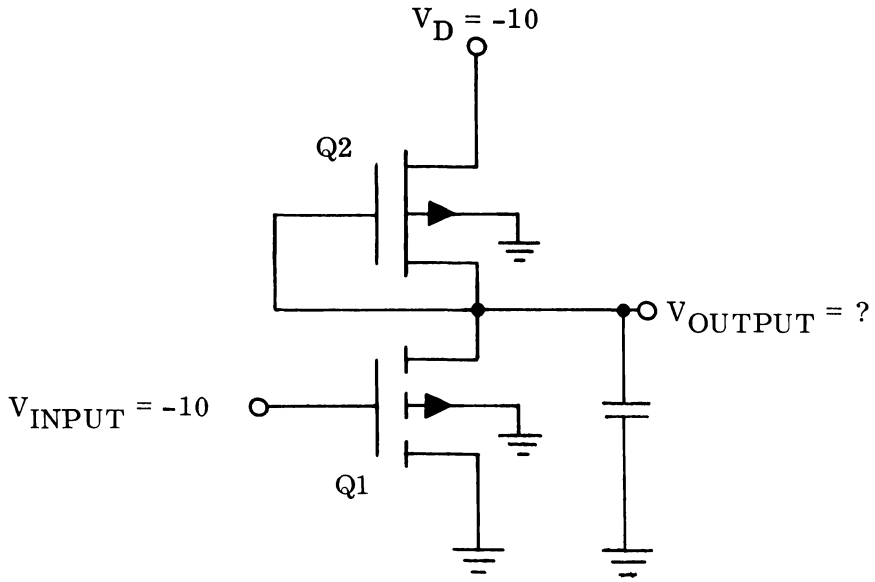
There would be no significant change in current level until the drain-to-source voltage dropped below the level which causes the MOSFET to saturate — roughly -3 volts in this example. Similarly, raising the level of the V_D supply voltage would have very little effect on the current. Because of this relatively constant current, the voltage across Q1 would _____ (vary linearly/ remain constant).

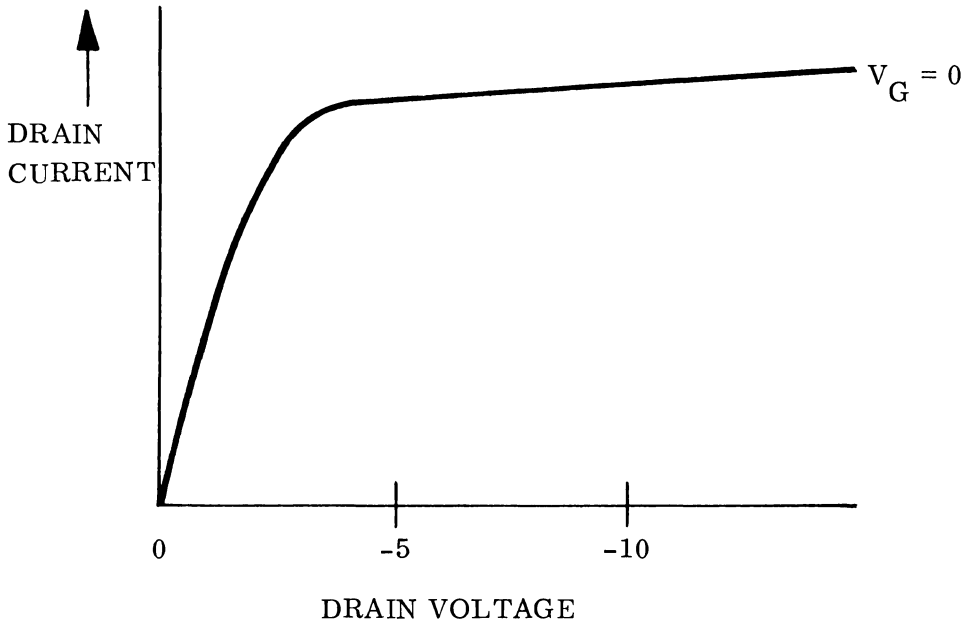
---

(91) *remain constant*

As a result, an inverter using a depletion MOSFET would be essentially immune to supply voltage fluctuations and transient voltages.

(89)
(90)
(91)


$V_D = -10$
Q2
$V_{OUTPUT} = ?$
$V_{INPUT} = -10$
Q1


DRAIN
CURRENT
$V_G = 0$
0
-5
-10
DRAIN VOLTAGE

(92) REVIEW

1. The threshold voltage in a/an _____ (enhancement/ depletion) MOSFET and the pinch-off voltage in a/an _____ MOSFET are measured between the gate and the _____ (source/ drain/substrate/ground).

2. Sketch an inverter in which a depletion MOSFET is used.

3. List four advantages an inverter using a depletion MOSFET would have over a similar inverter using only enhancement MOSFET's.

_____

_____

_____

_____

(92)

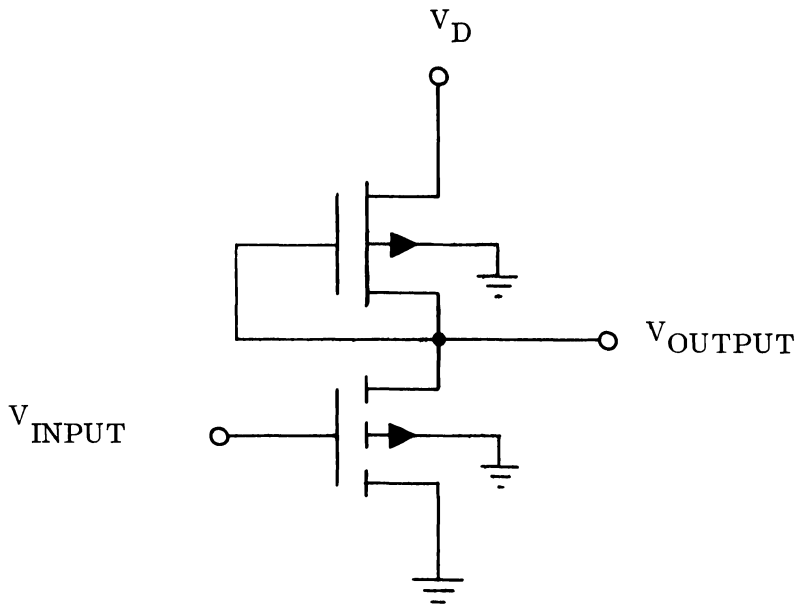
(93) REVIEW ANSWERS

1. enhancement
   depletion
   source

2. See opposite page.

3. Only one power supply required.
   Full V_D available at output.
   Less power consumption.
   Relatively immune to noise or power supply variations.

(93)



COMPLEMENTARY MOS

(94) Another configuration which should be discussed is called complementary MOS, or CMOS. A CMOS inverter is shown here. (Don't worry about the fact that the substrates aren't tied to anything; we'll get around to that shortly.) Instead of one P-channel enhancement MOSFET and one P-channel depletion MOSFET, the CMOS inverter contains one _____ MOSFET and one _____ MOSFET.

---

(95) *P-channel enhancement*

N-channel enhancement

Since the input is applied directly to both gates, neither MOSFET can be considered strictly a driver or strictly a load. If either is thought of as a load, it would probably be Q2, the P-channel MOSFET, because it is between the output and the supply voltage.

Before we look into the operation of the circuit, we have to find out something about the MOSFET's themselves. For one thing, which pin on each is the source and which is the drain? Remember from earlier discussions that the source and drain are determined by the direction of current flow. In the P-channel MOSFET, current flow is in the form of _____ (holes/electrons), while in the N-channel MOSFET, it is in the form of _____.

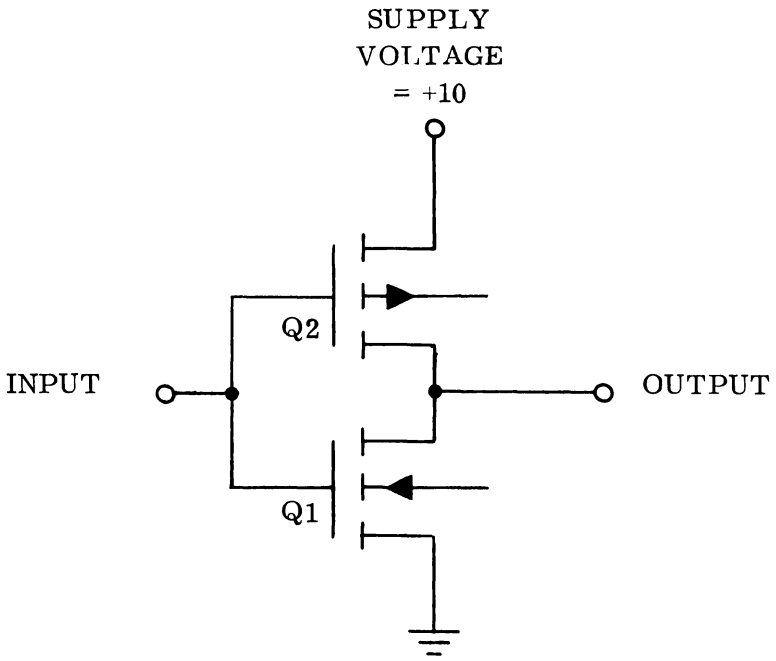
---

(96) *holes (P-channel)*

electrons (N-channel)

Keeping this and the polarity of the supply voltage in mind, indicate on the illustration which pins represent the source and which represent the drain for each MOSFET.

(94)
(95)
(96)



(97) The source and drain of each MOSFET are marked in the illustration. Now let's see what can be done with the substrates. The first thing to realize is that the substrate of a P-channel MOSFET is _____ (N/P) material and the substrate of an N-channel MOSFET is _____ material.

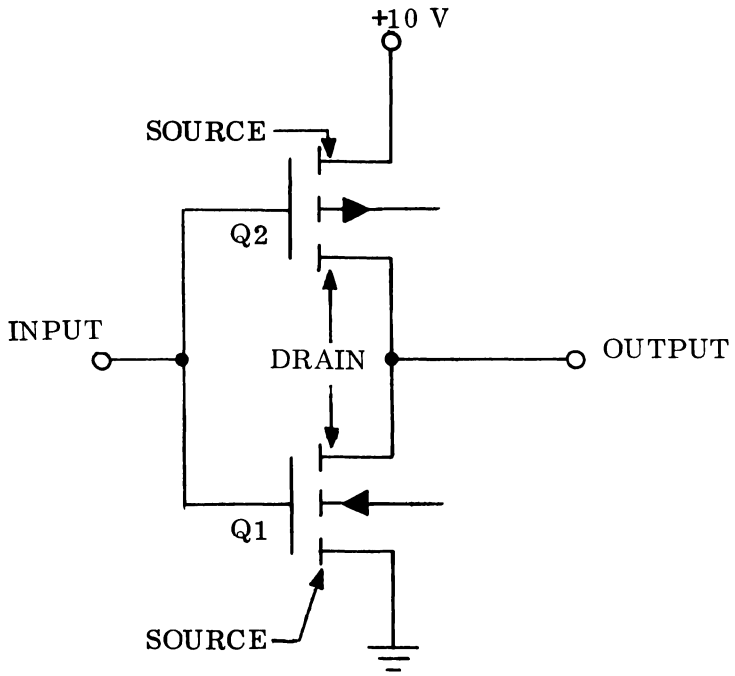
---

(98) N (P-channel)

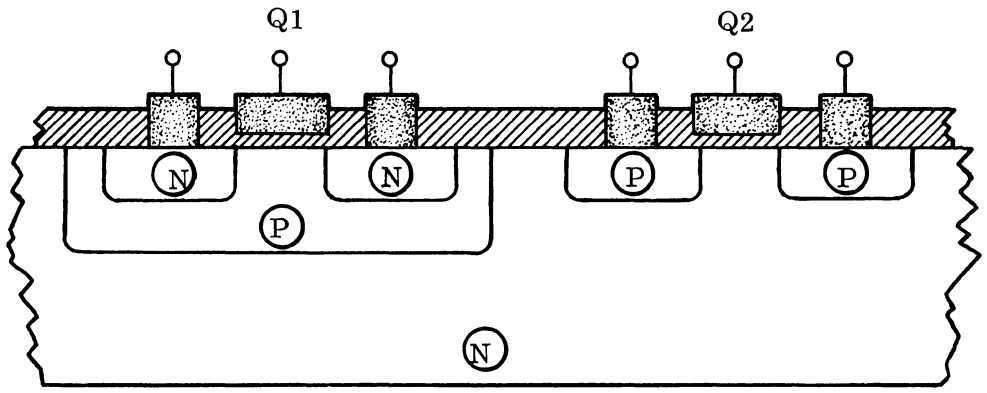
P (N-channel)

Physically it looks something like this. A well of P-type material is diffused into the N-type bulk substrate. The P-well acts as a substrate for the N-channel MOSFET. The two substrates, then, are isolated from each other by a P-N junction as long as a reverse bias is present. To maintain this reverse bias, the Q1 substrate should be _____ (grounded/connected to the +10 volts) and the Q2 substrate should be _____ (grounded/connected to the +10 volts).

(97)



(98)



(99) grounded

connected to the +10 volts

In CMOS, then, all N-channel substrates are grounded and all P-channel substrates are connected to the most positive point in the circuit, i.e., the positive power supply. In the simple inverter we have been discussing, the result is to have the substrate effectively tied to the source in each case. We will look at some slightly more complicated CMOS circuits later, but first we have to see how the inverter itself works. Assume the input is grounded and that the threshold voltages of Q1 and Q2 are +2 volts and -2 volts, respectively. Q1 would be turned _____ (on/off), and Q2 would be turned _____ .

---

(100) *off (Q1)*

on (Q2)

The Q1 gate and source would both be at zero volts, so Q1 would be turned off. The Q2 gate, on the other hand, would be at -10 volts with respect to the source, so Q2 would be turned on.

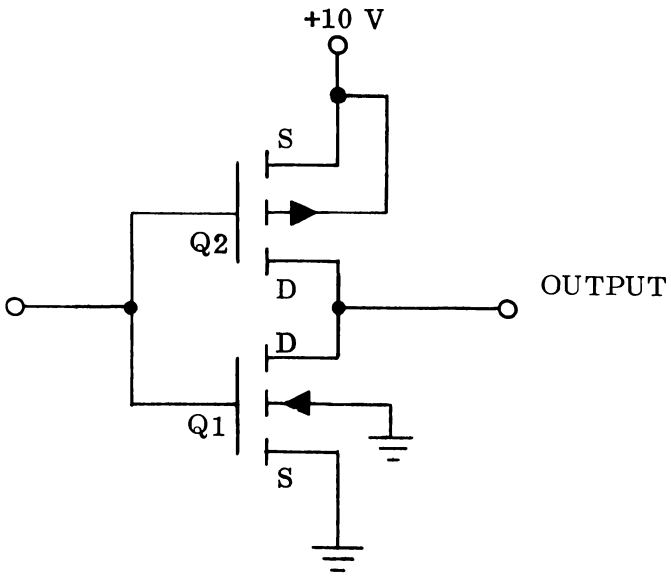
Now, how closely can the output approach the supply voltage? Notice that, as the output voltage increases, the gate-to-source voltage of Q2 will _____ (decrease/increase/remain constant).

---

(101) *remain constant*

If the Q2 gate-to-source voltage remains constant at -10 volts, Q2 will remain turned on. Its resistance will not, as it did in earlier inverter configurations, increase. If anything, the resistance of the induced channel will decrease as the output voltage rises, simply because the drain end of the channel will become more positive with respect to the gate. With a logic 0 input, then, Q1 is turned off, Q2 is turned on, and the inverter output voltage will rise to _____ (+10/+8/+2) volts.

(99)
(100)
(101)



(102) +10

So, we can already see one advantage to the CMOS inverter: There is no threshold voltage drop even with only a single power supply.

Now let's apply a logic 1 to the input. Assuming the logic 1 is being supplied by another CMOS logic circuit, it will be approximately +10 volts. This means that Q1 will be turned _____ (on/off), and Q2 will be turned_____ .

---

(103) on (Q1)

off (Q2)

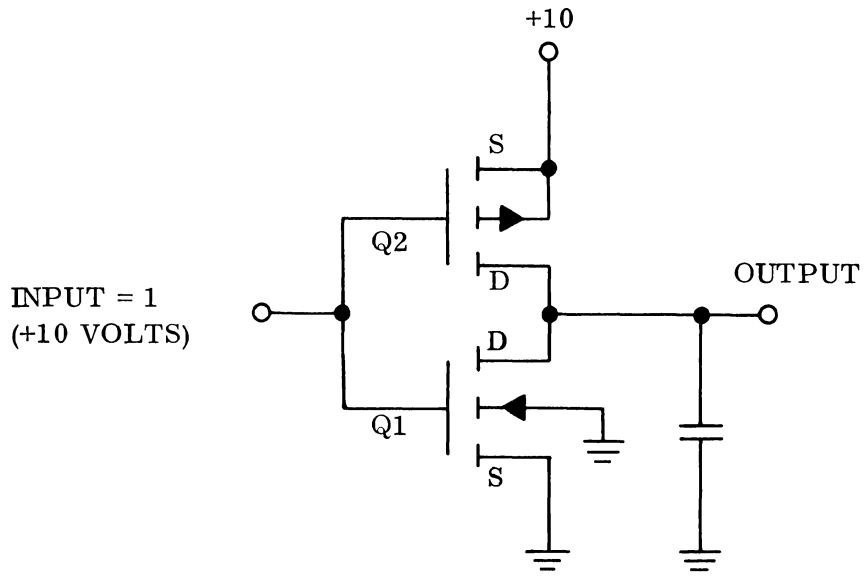
The output, of course, would be near 0. By way of comparing this with logic 0 outputs of the previous, all-P-channel MOS (PMOS) configurations, recall that, in the PMOS configurations, both Q1 and Q2 were turned on when the inverter output was a logic 0. The output voltage was low only because the turned-on Q2 had a much higher resistance than the turned-on Q1. In the CMOS inverter, on the other hand, Q2 is completely turned off and is essentially an open circuit. This means that the logic 0 output level in a CMOS inverter would probably be _____ (higher/lower) than the logic 0 output level in a PMOS inverter.

---

(104) lower

The fact that, regardless of the output, one or the other of the MOSFET's is always turned off, gives the CMOS inverter another important advantage over the PMOS inverter. Because at least one of the MOSFET's is always turned off, the CMOS inverter will always draw _____ (less current/the same current as/more current than) any of the PMOS inverters.

(102)
(103)
(104)



(105) less current than

Except for the current drawn by the following stage, the only current that will ever flow through the CMOS inverter will be the result of leakage through whichever MOSFET is turned off. A major advantage of the CMOS inverter, then, is its extremely_____ (low/high) power consumption.

---

(106) *low*

Consider also the effect of variations in the supply voltage. The logic 1 output level will simply be equal to the supply voltage, and any variations in the supply voltage will be duplicated by the output. As in the PMOS configurations, this presents no problem unless the supply voltage variations become extreme.

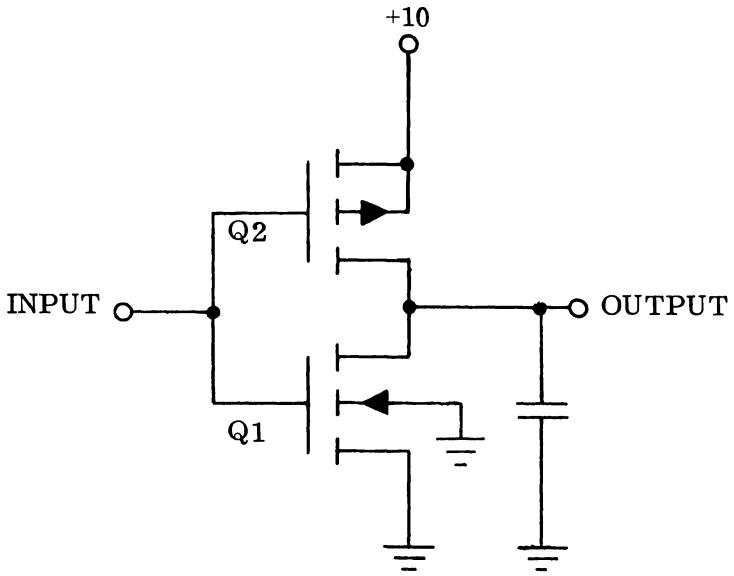
But what about the logic 0 output level? It might seem at first that increasing the supply voltage would make the source positive with respect to the gate, thereby turning Q2 on. But don't forget that the input to the inverter is coming from the output of another MOSFET logic circuit which is being driven by the same power supply. Thus, if the supply voltage increases, so will the input voltage, and the Q2 gate-to-source voltage will_____.

---

(107) *remain constant, or remain essentially at zero*

As a result, increases in supply voltage will not produce any significant increase in current through Q2, and the output level will remain very near 0. This means, of course, that a CMOS inverter can tolerate _____ (very high/only very low) noise levels.

(105)
(106)
(107)



(108) very high

Another difference between the CMOS and the PMOS inverters can be seen if we compare the paths through which current must flow in order to charge and discharge the gate capacitances of the following stages. The CMOS inverter and the PMOS inverter with a depletion MOSFET used as a load are shown here.

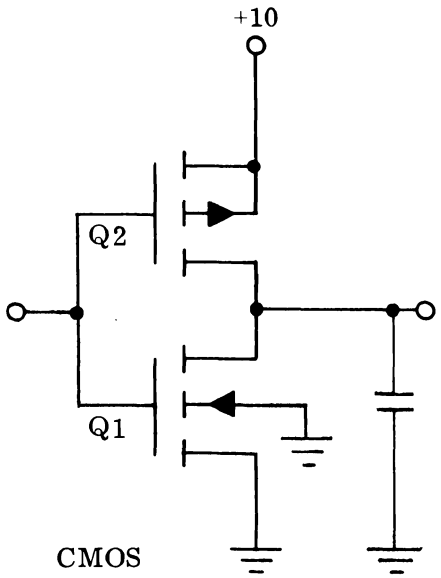
Notice first that the charge path for the gate capacitance in both cases is through Q2. Both capacitances would charge to nearly the full supply voltage, but the charge path in the CMOS inverter would offer a lower resistance to the charging current than would the charge path in the PMOS inverter. This is simply because Q2 in the CMOS inverter has 10 volts between the gate and source and is therefore more heavily turned on than Q2 in the PMOS inverter, in which the gate and source are tied together. As a result, the CMOS gate capacitance would charge more _____ (slowly/rapidly) than the PMOS gate capacitance.

---

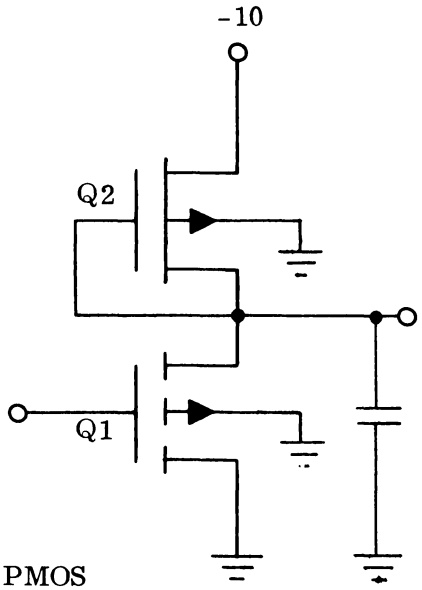
(109) rapidly

Now notice the discharge path in both inverters. In the PMOS the discharge path is through a P-channel MOSFET, while in the CMOS it is through an N-channel. This means that the current carriers for the discharge of the PMOS capacitance would be holes, while the current carriers for the discharge of the CMOS capacitance would be electrons. Electrons, as we have said before, have greater mobility than holes, which means that the _____ (CMOS/PMOS) capacitance would discharge more quickly.

(108)
(109)



CMOS



PMOS

(110) CMOS

Because of these shorter charge and discharge times, of course, a CMOS inverter would operate more rapidly than a PMOS inverter.

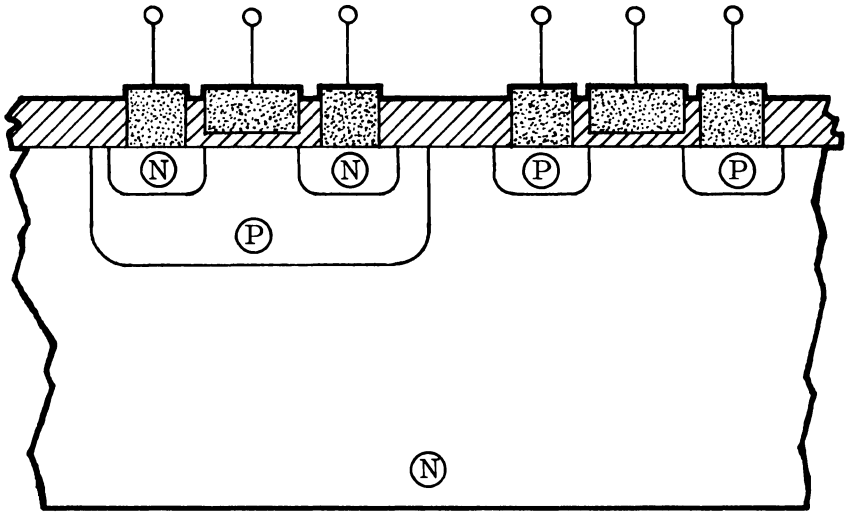
Another difference between CMOS and PMOS can be seen in the illustration. Because of the well of P-type material into which the source and drain of the N-channel MOSFET must be diffused, a CMOS inverter would always be _____ (larger/smaller) than a PMOS inverter.

---

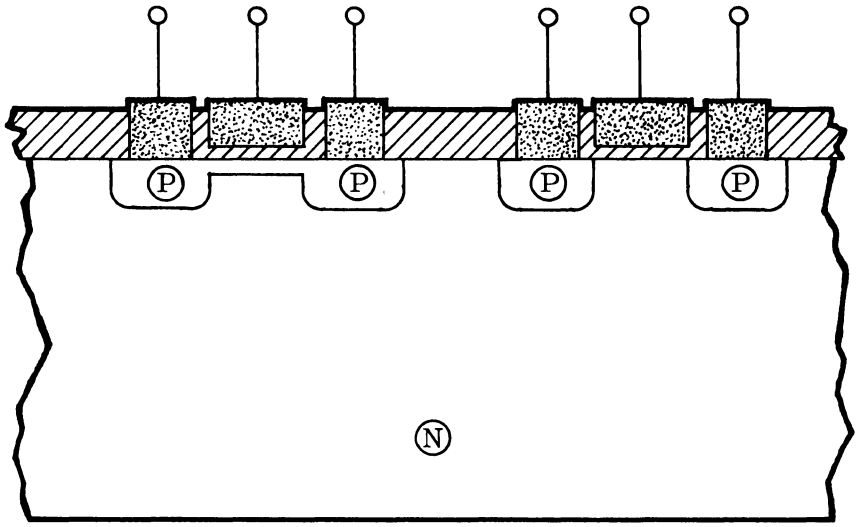
(111) larger

CMOS, then, would be at a disadvantage as far as size is concerned. A related disadvantage can be seen if you consider the number of steps needed to produce each circuit. The CMOS inverter would require _____ (more/less) diffusions than the PMOS inverter.

(110)
(111)



CMOS



PMOS

(112) more

A further size disadvantage can be seen if we look at some circuits other than the simple inverter we have been discussing. One of these circuits is shown here. Assuming that a logic 1 equals approximately +10 volts and that a logic 0 is ground, the circuit shown here is a _____ (NOR/NAND) gate.

---

(113) NOR

To get a logic 1 out, of course, Q1 and Q2 must be turned on and Q3 and Q4 must be turned off. The only way to accomplish this is to ground both inputs.

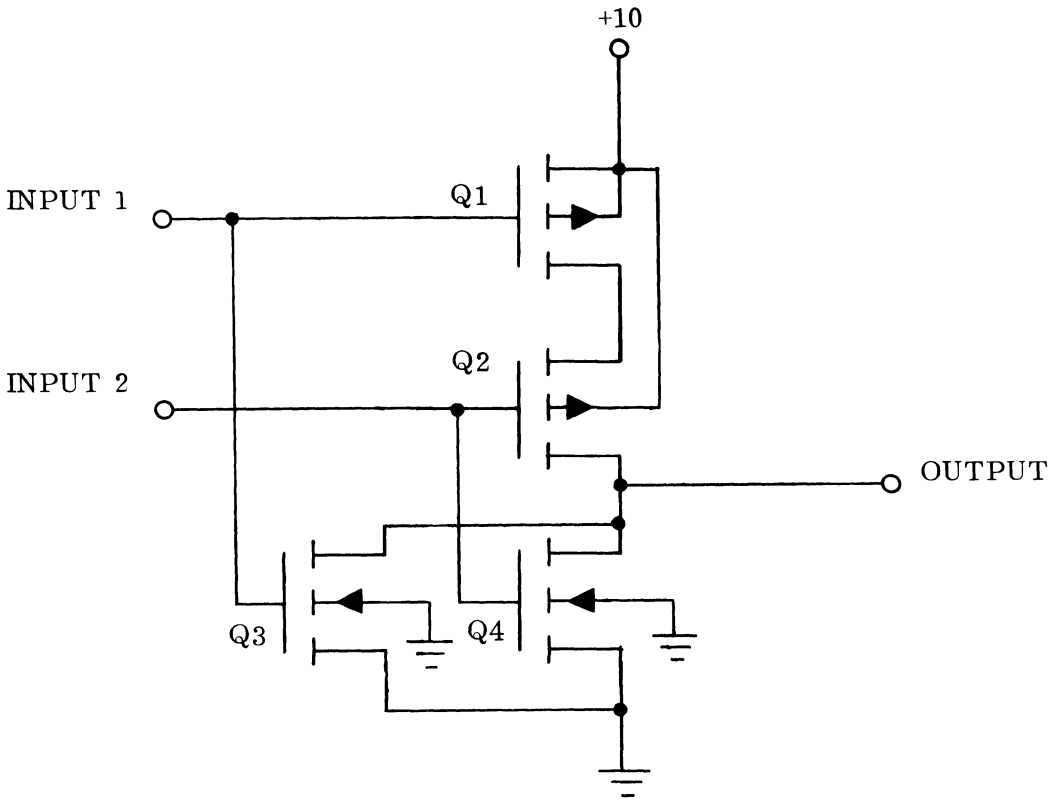
As you can see, this 2-input CMOS NOR gate requires 4 MOSFET's. A 2-input PMOS NOR gate would require _____ MOSFET's.

---

(114) 3

Similarly, a 4-input CMOS NOR gate would require 8 MOSFET's, one pair for each input. CMOS NAND gates are similar in that they require a pair of MOSFET's for each input. On the opposite page, sketch a 2-input CMOS NAND gate. As in the NOR gate, the drivers (discharge paths) are N-channel and the loads (charge paths) are P-channel.

(112)
(113)



(114)

(115) A 2-input CMOS NAND gate is shown on the opposite page.

REVIEW

1. Indicate the source and drain of Q1 and Q3 in the illustration.

2. List two disadvantages and four advantages of CMOS inverters. Indicate which two of the advantages are shared to some extent by PMOS inverters which use depletion MOSFET's as loads.

   Disadvantages:

   _____

   _____

   Advantages:

   _____

   _____

   _____

   _____

(116) REVIEW ANSWERS

1. Q1: Source at top, drain at bottom.

   Q3: Source at bottom, drain at top.

2. Disadvantages:

   CMOS is larger, or takes more space.

   CMOS is more difficult to make, or requires more steps to produce.

   Advantages:

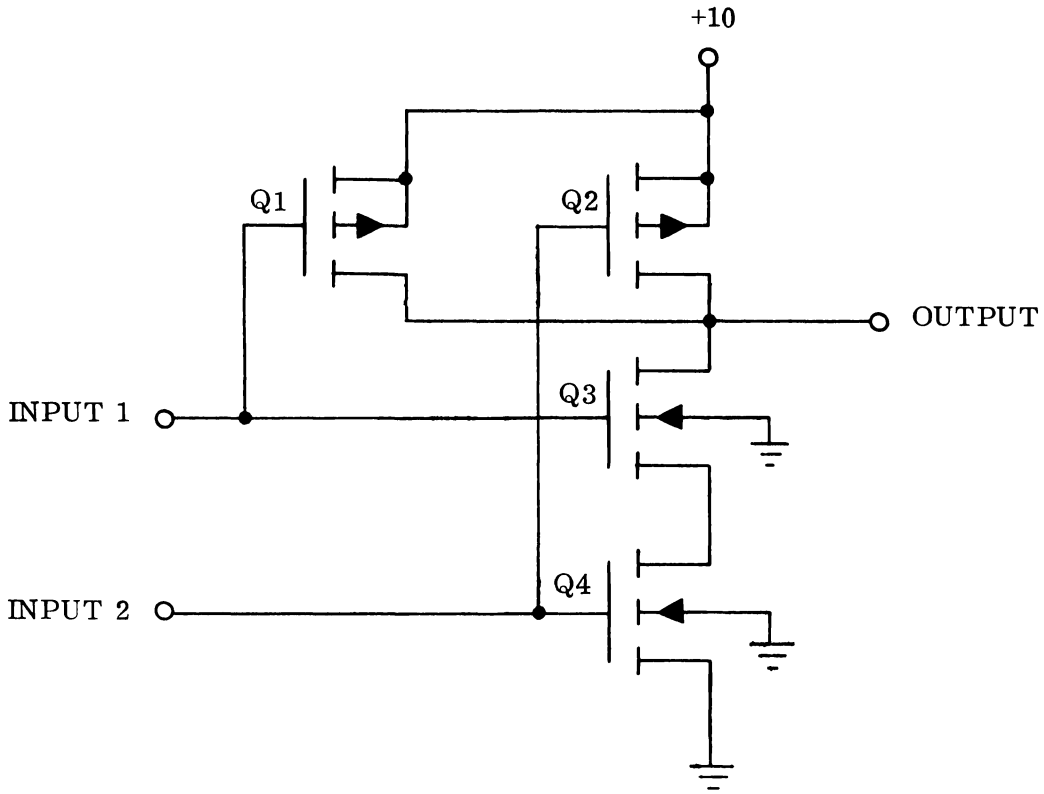
   CMOS is very fast.

   CMOS has very low power consumption.

   CMOS has high noise immunity. (Shared)

   CMOS requires only one power supply in order to get the full supply voltage at the output. (Shared)

(115)
(116)



(117) Until this point, we have spoken primarily of how to use the different types of MOSFET's in simple logic circuits. Except for a brief comment about the extra diffusions necessary in a CMOS inverter, we have not concerned ourselves with the methods of construction. There are, however, several different methods and several different structures, all with their own advantages and disadvantages. In the following frames, we will look at some of the more common methods and structures.

Before getting into the construction of the MOSFET's themselves, however, we should look briefly at how interconnections between MOSFET's are made. The interconnections discussed in earlier texts in this series were made by depositing a layer or layers of _____ .

(117)

P-CHANNEL ENHANCEMENT

P-CHANNEL DEPLETION

N-CHANNEL ENHANCEMENT

N-CHANNEL DEPLETION

(118) aluminum, or metal

As far as resistivity is concerned, metal contacts and interconnections are the best. When a certain amount of resistance is permissible, however, interconnections can be made using silicon. As indicated in the illustration, there are two ways of producing silicon conductors. Silicon conductors can be either _____ _____ or _____ .

---

(119) *deposited on the oxide or diffused into the substrate*

The deposited conductor is isolated from the substrate and from other conductors by the oxide. In order for the diffused conductor to be isolated from the substrate, the doping of the diffused conductor would always have to be _____ _____ (the same as/the opposite of) the doping of the substrate.

---

(120) *the opposite of*

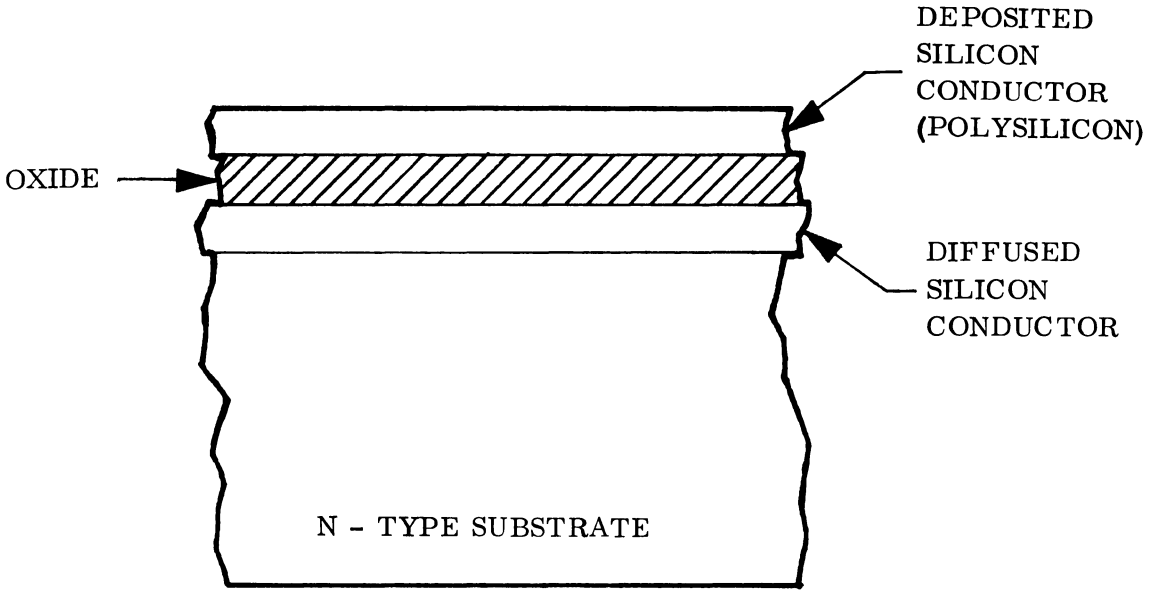
In this illustration, then, the diffused conductor would be heavily doped P-type material, or P+. If the substrate were P-type silicon, the diffused conductor would be heavily doped N-type material, or_____ .

---

(121) *N-*

As for the deposited conductors, there is no need to dope them at all. This is because deposited silicon is, in its undoped form, at least as good a conductor as is the heavily doped substrate silicon. The reasons for this lie in the fact that the substrate silicon was grown rather than deposited, and it therefore has a much more orderly and regular crystalline structure than does the deposited silicon. The well-ordered crystalline structure of the grown silicon does not lend itself to conductivity, whereas the more haphazard structure of the deposited silicon results in a fairly high conductivity. Deposited silicon is also known as _____ . The conductivity of undoped deposited silicon is similar to that of _____ _____ (aluminum/undoped grown silicon/heavily doped grown silicon).

(118)
(119)
(120)
(121)



(122) polysilicon

heavily doped grown silicon

Using all three types of interconnect on a single chip, as shown here, is known as triple layer interconnect. (This should not be confused with triple layer metallization, which is a less popular method using three layers of deposited aluminum separated by layers of oxide.) The diffused conductor, of course, is always on the bottom. The metal conductor is usually on top because metallization is normally one of the last steps to be performed. For circuits in which a relatively high current was expected to flow, _____ interconnects would be used as much as possible.

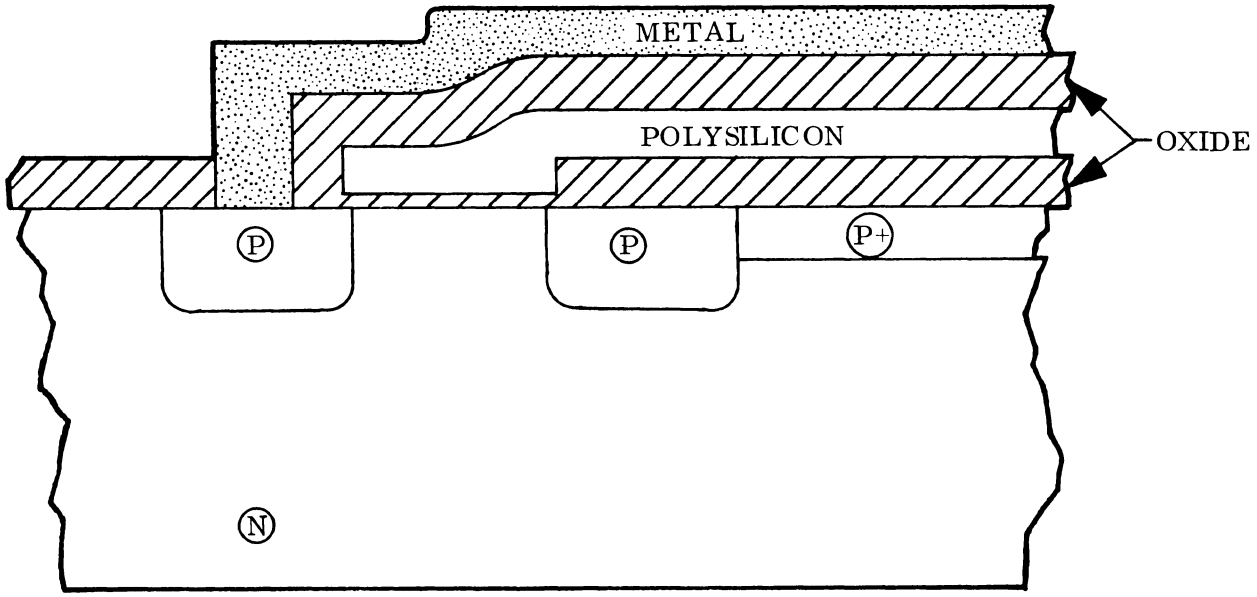
---

(123) metal

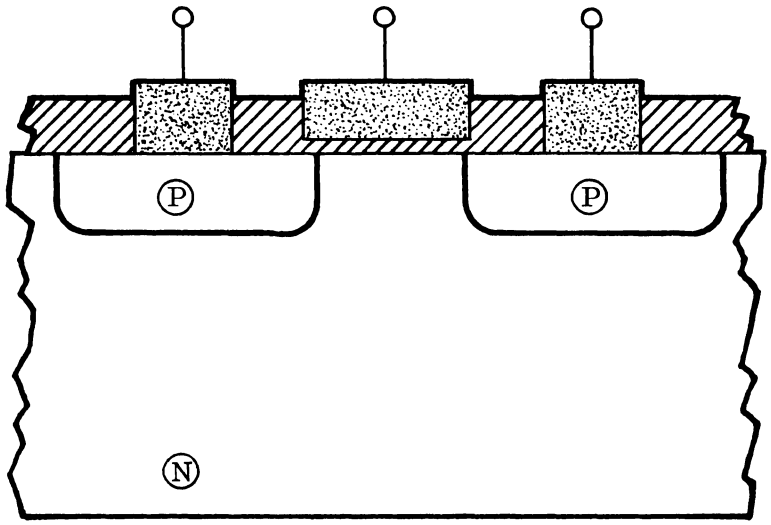
Now, for the construction of the MOSFET's themselves, let's start with the P-channel enhancement MOSFET, shown here. One of the early problems in MOS was that of high threshold voltages. To operate a gate, the logic 1's would have to be higher than the threshold voltage. Often these MOS gates required such high 1's that the logic 1 output of a bipolar circuit, such as TTL, was not high enough to drive the MOS gate.

The threshold voltage of a given MOSFET is dependent on a number of things, including the thickness and dielectric constant of the gate oxide, the crystalline structure of the substrate, the type of material used to construct the gate, and the doping level of the substrate. To lower the threshold voltage of a MOSFET, you have to increase the effect the field developed by the gate voltage has on the channel in the substrate. To lower the threshold voltage of the MOSFET shown here, you could _____ (increase/decrease) the oxide thickness or _____ (increase/decrease) the dielectric constant.

(122)



(123)



(124) decrease (thickness)

increase (dielectric constant)

Since the gate oxide thickness is only on the order of 1,000 Angstroms, decreasing its thickness is not too practical. The thinner the oxide is made, the more susceptible it is to breakdowns and to the tiny pin holes which are produced during the manufacturing process. Increasing the dielectric constant is somewhat more practical. One of the methods is shown here in an expanded view of a MOSFET gate. In this method, most of the oxide beneath the gate has been replaced by a layer of_____ .

---

(125) silicon nitride, or Si_3N_4

The overall thickness of the gate insulation is about the same as before, but the nitride has a dielectric constant roughly twice that of the oxide. MOSFET's made in this way are often referred to as MNOS, or M _____ - N _____ -O _____ -S _____ .

---

(126) Metal-Nitride-Oxide-Semiconductor

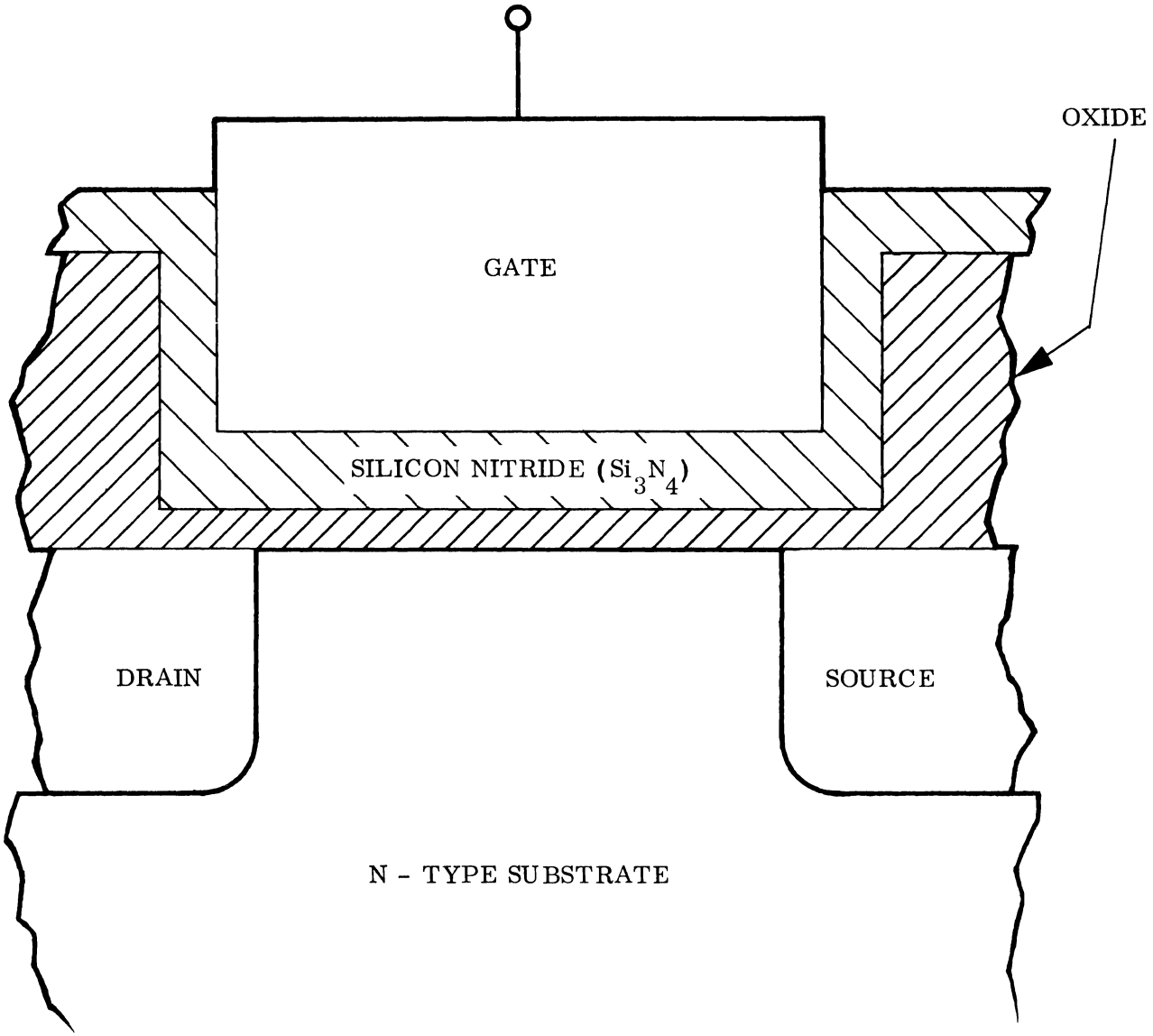
In addition to the lower threshold voltage resulting from the increased dielectric constant, MNOS has another advantage, this one resulting from the fact that the oxide and the nitride are produced in separate steps. Pin holes are produced in each step, but only in the specific material being processed. This means that the pin holes in the nitride probably_____ (would/would not) line up with the pin holes in the oxide.

---

(127) would not

The likelihood of any two pin holes lining up and producing one continuous pin hole completely through both the nitride and the oxide is very small. In MNOS, then, the pin holes would have very little effect on the MOSFET's operation.

(124)
(125)
(126)
(127)



(128) Another method of changing the threshold voltage, ion implantation, is shown here. In ion implantation, the chip is bombarded with P-type dopant ions after the source and drain have been diffused but before the gate metal has been deposited. The thick oxide coating over most of the chip stops the ions, but the thin gate oxide allows some to penetrate, thereby changing the doping level of the substrate immediately beneath the gate oxide. If the ion bombardment is continued long enough, a channel of _____ material will be formed beneath the gate oxide.

---

(129) P-type

The result, of course, would be a depletion MOSFET. The substrate directly under the gate oxide would have gradually shifted from N to N+ to neutral to P- and finally to P. To see what this means in terms of threshold voltage, we can look at the curves shown here. The curve on the right would represent the _____ (enhancement/depletion) MOSFET, while the curve on the left would represent the _____ MOSFET.

---

(130) enhancement (right)

depletion (left)

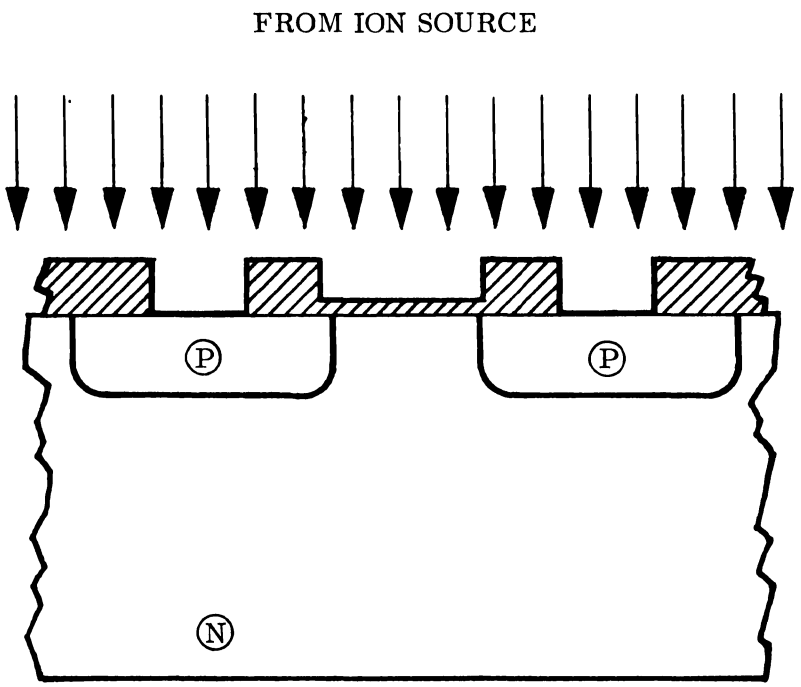
As you can see, the depletion MOSFET curve is identical to the enhancement MOSFET curve. It has simply been shifted to the left by the ion implantation. The threshold voltage has gone from some negative value to 0 and then beyond. Once it is to the left of 0, it is no longer called a threshold voltage. Instead, it would be called the _____ voltage.

---

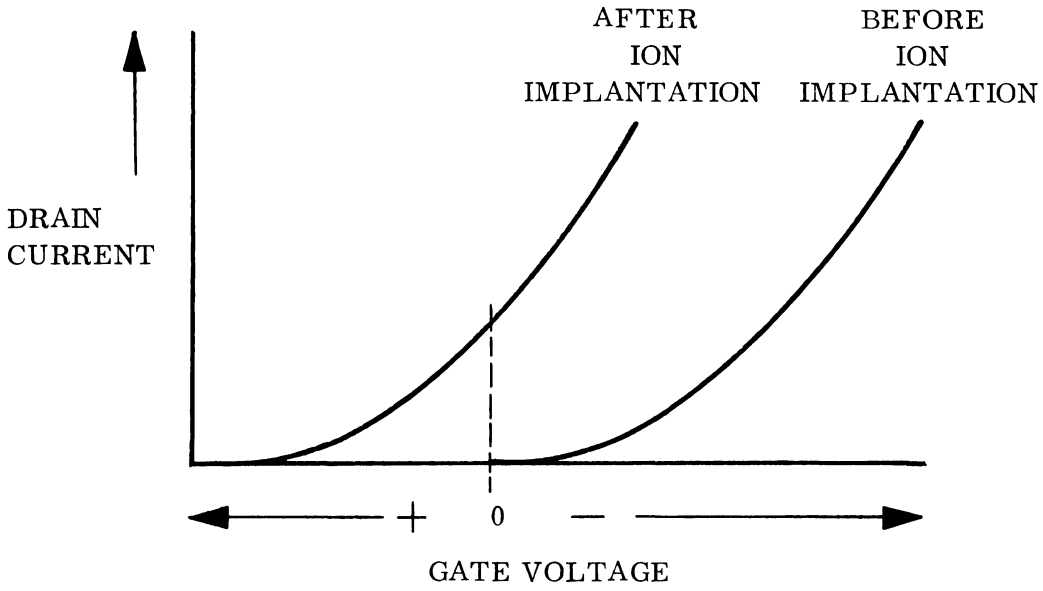
(131) pinch-off

Once ion implantation can be completely and precisely controlled, MOSFET's having any desired threshold or pinch-off voltages can be produced.

(128)



(129)
(130)
(131)



(132) Another method of changing the threshold voltage is based on the fact that the threshold voltage is dependent on the work functions of the substrate and gate materials. The work function is essentially a measure of the energy level of the current-carrying electrons it contains. In general, then, the work function of a material is closely related to its conductivity. The work function of the gate metal in a MOSFET would be _____ (nearly the same as/ much different from) the work function of the semiconductor substrate.

---

(133) *much different from*

As a result of these different work functions, or energy levels, an electrostatic field is generated. This field, in effect, opposes the field generated by the gate voltage. To achieve a lower threshold voltage, then, the work functions of the gate and substrate materials should be _____ (nearly the same/much different).

---

(134) *nearly the same*

One way of accomplishing this is shown here. In this MOSFET, the gate material is not aluminum but _____ .

---

(135) *polysilicon*

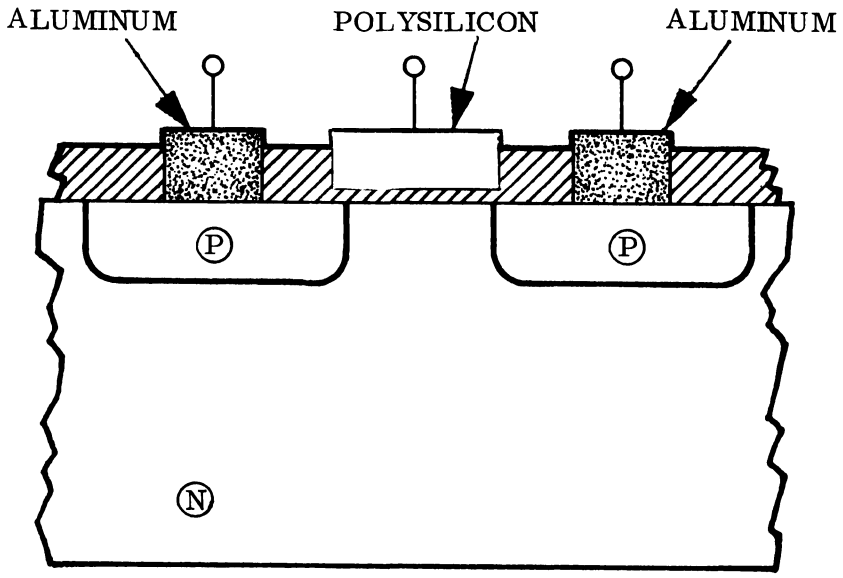
The polysilicon, even though it is a fairly good conductor, has a work function which is much closer to that of the substrate silicon than is that of aluminum. As a result, the threshold voltage is considerably lowered. MOSFET's produced in this way are called silicon gate MOSFET's. They have threshold voltages comparable to those of MNOS MOSFET's.

(132)
(133)

WORK FUNCTION $\propto$ CONDUCTIVITY

---

(134)
(135)



(136) REVIEW

1. List three methods of lowering the threshold voltage of enhancement MOSFET's.

_____

_____

_____

2. Which of the methods would, if carried far enough, result in a depletion MOSFET? _____

3. What is one major reason low threshold voltages are desirable in MOSFET's?

_____

---

(137) REVIEW ANSWERS

1. Partially replacing the gate oxide with silicon nitride.

   Ion implantation.

   Making the gate of polysilicon instead of aluminum.

2. Ion implantation

3. Compatibility with bipolar circuits.

(136)
(137)

THRESHOLD VOLTAGE REVIEW

(138) Compared to bipolar logic circuits, the early MOS logic circuits were very slow. One of the basic reasons for this slowness was, as it was in the early bipolar circuits, capacitance. The two major types of capacitance which affect MOSFET switching speed are gate capacitance and parasitic capacitance. Both are shown in the illustration. The gate capacitance is between the gate and the _____ _____ , while the parasitic capacitance is between the metal interconnections and the_____ .

---

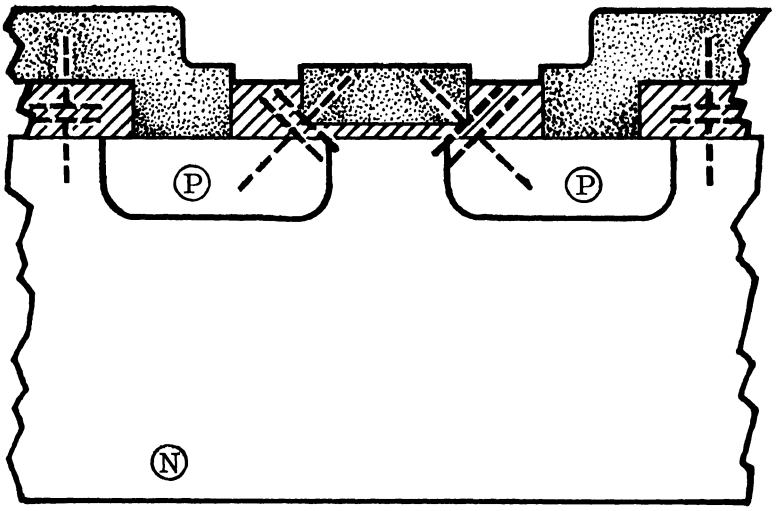
(139) source and drain

substrate

This part of the substrate, which lies between the areas into which the MOSFET's and other components are diffused, is often called the bulk substrate.

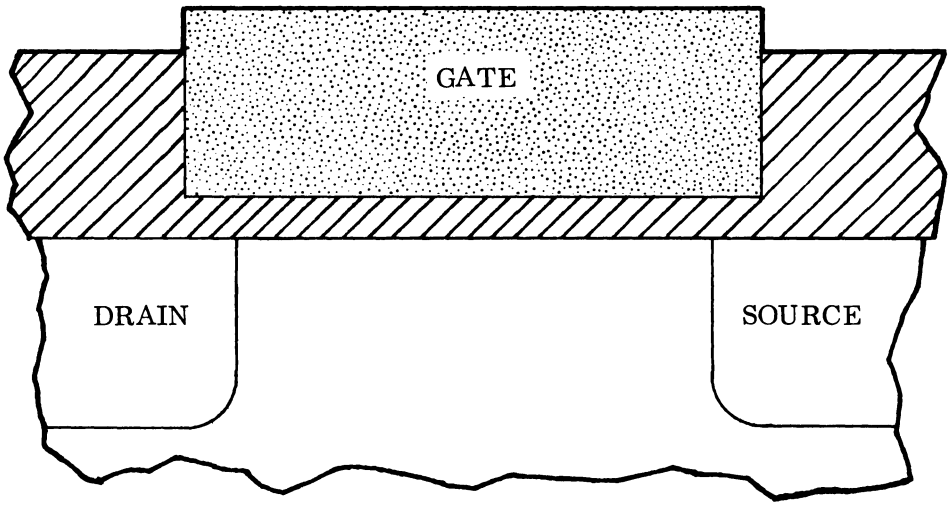
To see how these capacitances can be reduced, we first have to see what causes them. First we will look at the gate capacitance. Of the two MOSFET's shown here, which would have the greater gate capacitance? _____

(138)



(139)

Ⓐ



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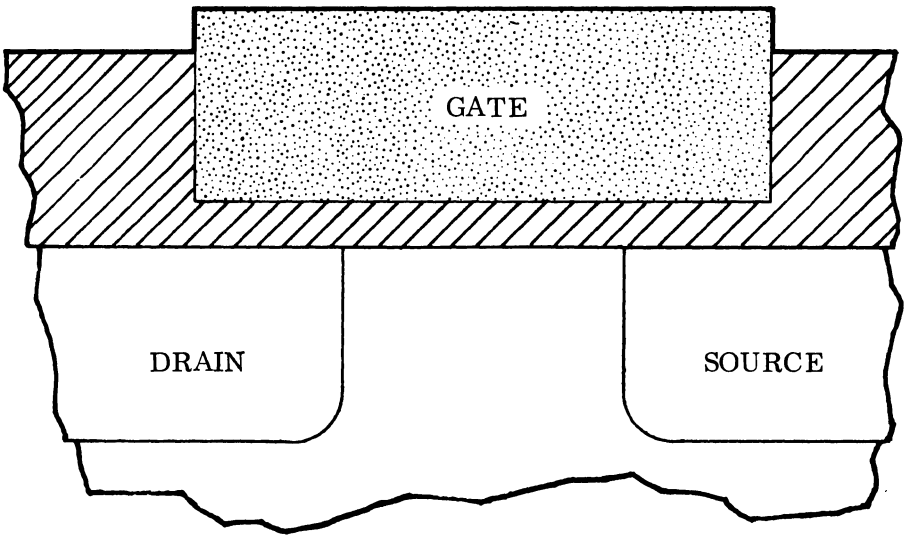


(140) B

The greater capacitance is due to the fact that the gate metal extends further over the source and drain diffusions, thereby increasing the plate area of the capacitors. One way to reduce this capacitance, then, would be to reduce this area of overlap. To see how this can be done, we must first look into the construction process and see why the overlap exists.

Recall, from an earlier text, that the substrate was first covered with a layer of oxide, and then the oxide was removed from the areas into which diffusions were to be made. The removal was a fairly complicated process involving photomasks, photoresist, and several types of solvent. The overall process can be simplified for our purposes, however, if most of the intermediate steps are left out. It can all be reduced to the fact that, when a given sequence of steps is completed, the oxide under the opaque areas of the mask is gone, exposing the substrate. Assume a single P-channel enhancement MOSFET is to be constructed in the area shown in the illustration. The mask shown above the oxide would be the mask which defines the _____ areas.

---

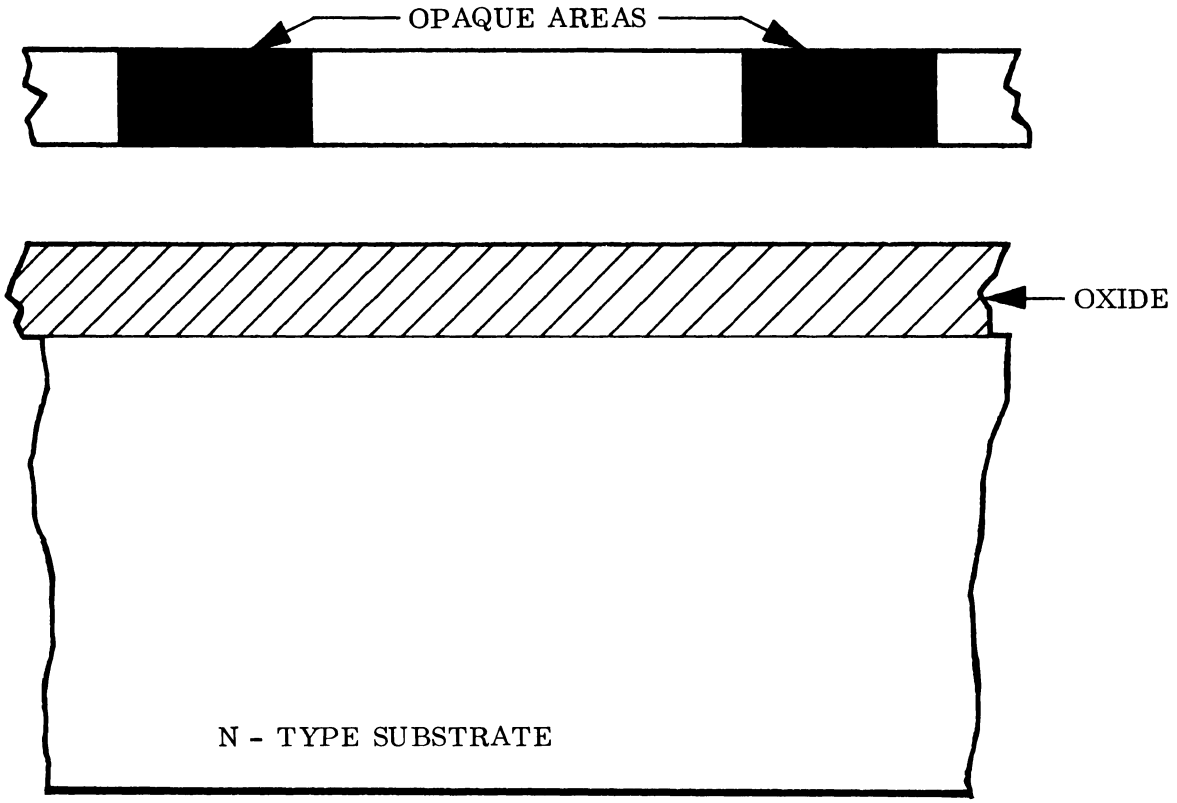
(141) source and drain

After the sequence involving this mask, the oxide will be gone from the areas which were under the opaque areas of the mask. These areas, shown here, correspond to the source and drain. The next step is to diffuse P-type impurities into the substrate through the exposed surface. In diffusion, the impurities will penetrate

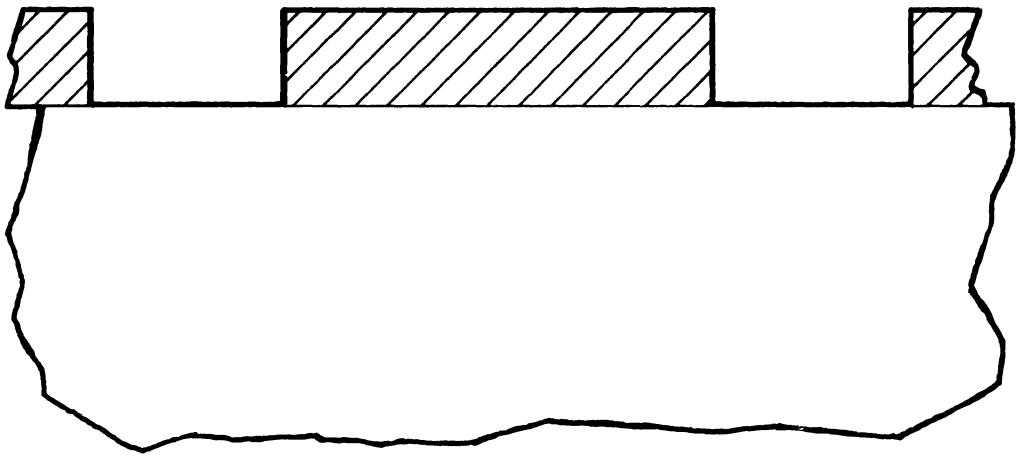
---

(only vertically down into the substrate/radially outward from the exposed surface areas as well as vertically downward).

(140)



(141)



(142) radially outward from the exposed surface areas as well as vertically downward

The result is shown here. The diffused area extends under the oxide roughly as far as it extends down into the substrate. This illustration is somewhat more accurate in this respect than the previous ones we have used, most of which were exaggerated in one way or another, either for convenience or to illustrate a point.

---

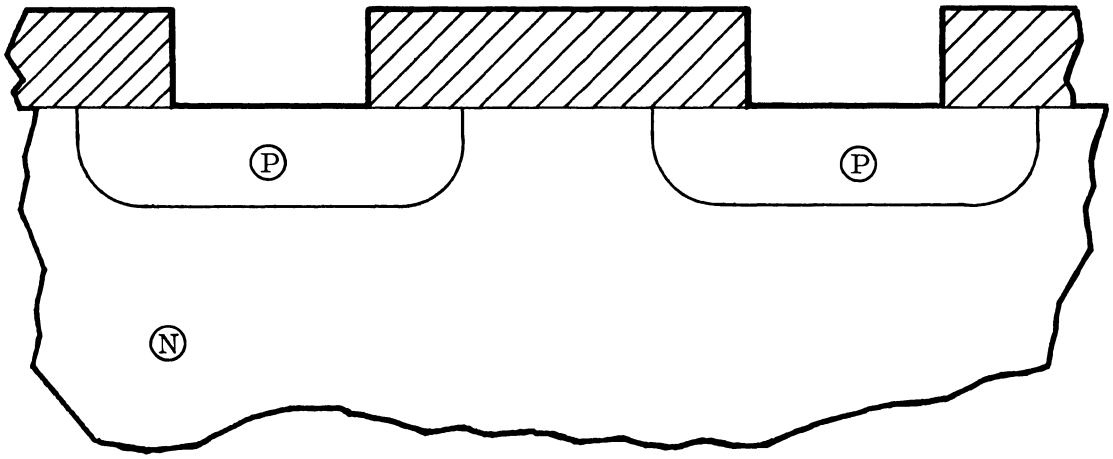
(143) The next step is to remove the oxide from the gate area and then regrow a thinner layer of oxide in its place. The mask which defines the gate area is shown here. The gate, when deposited, will have excessive overlap if this mask is too_____. (small/large).

---

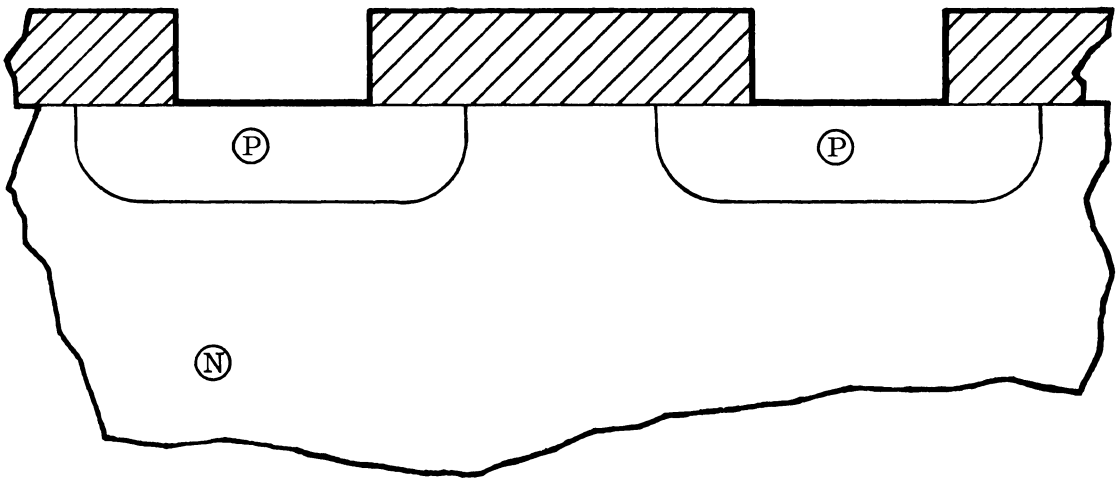
(144) large

On the other hand, if the mask is too small, the gate will not cover the entire area between the source and drain. Inducing a complete channel between the source and drain using too small a gate would require a much _____ (higher/lower) gate voltage than it would using a gate that was too large.

(142)



(143)
(144)



(145) higher

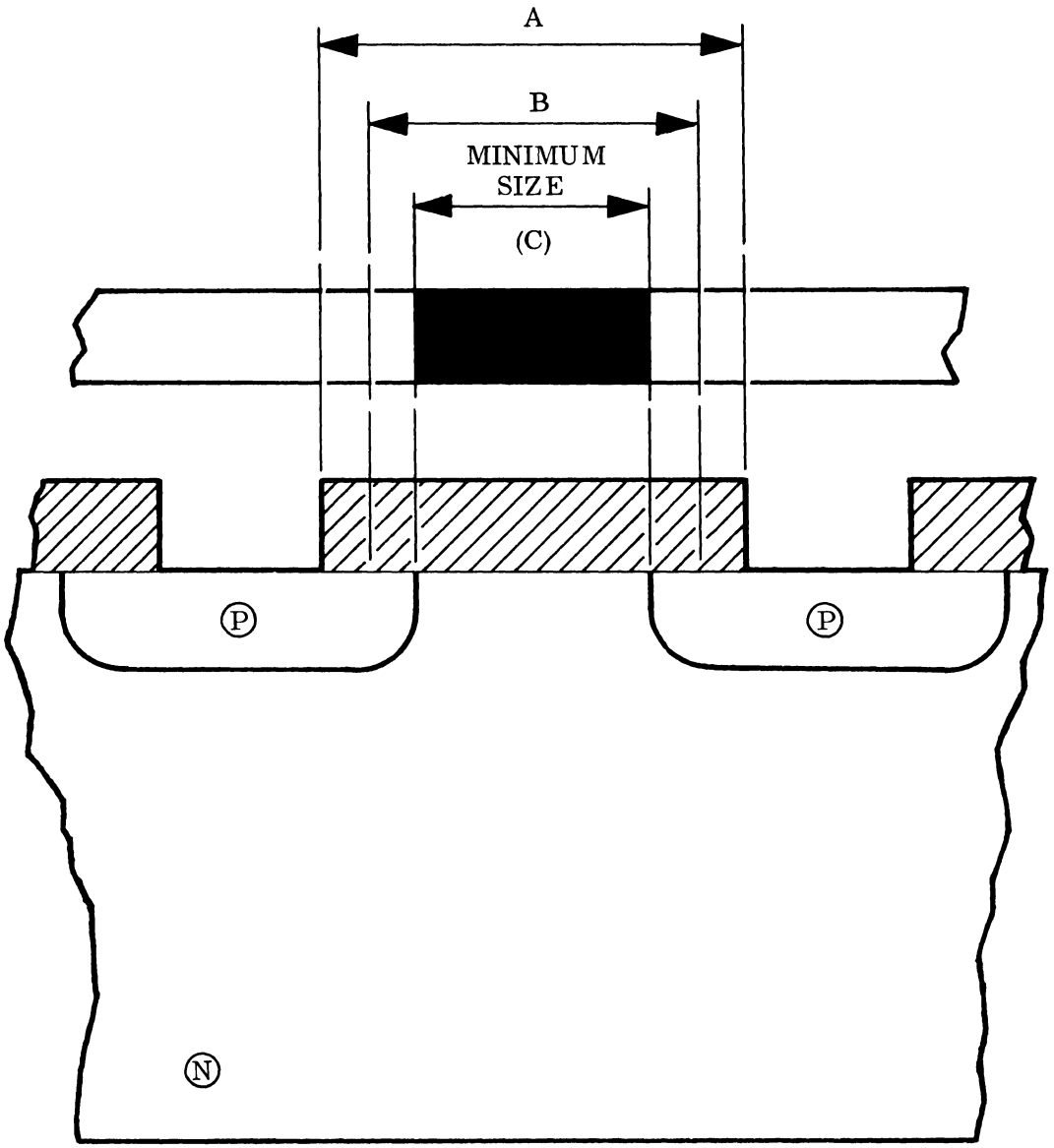
In other words, for the threshold voltage to remain at an acceptable value, the gate must extend over the entire channel area. This requirement sets a minimum size limit on the gate mask, shown here. An ideal gate would result from a gate mask which had a width equal to _____ (A/B/C).

---

(146) C

The ideal mask, then, would be the minimum size mask. Because of the tolerances in the making and positioning of the masks, however, the manufacturer would have to aim for a size that is closer to the B dimension than the minimum. That is, to insure that the gate is no smaller than the minimum, the manufacturer would have to make the gate somewhat larger than necessary. The "ideal" size, rather than being in the center of the allowable tolerance range, is at one extreme. Add to this the fact that there are similar tolerances in the size and positioning of the source and drain masks, and you can see that a comparatively large overlap is almost inevitable.

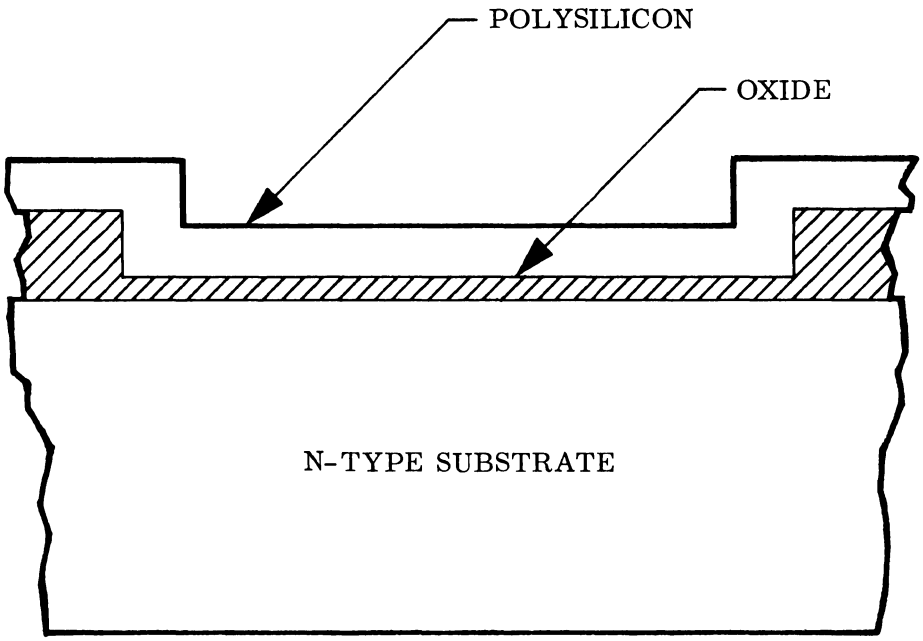
(145)
(146)



(147) The commonest way of reducing gate overlap is to use the gate itself as a mask. Gates used in this way are called self-aligning gates, and there are two basic processes involving self-aligning gates. One process uses a silicon gate and the other uses a metal gate. We will discuss the silicon gate process first.

In the silicon gate process, as in the processes we have already discussed, the first step is to deposit a layer of thick oxide over the substrate. Then, instead of two separate windows, a single window is etched out. Following that, a thin layer of oxide is regrown over the window, and a layer of polysilicon is deposited over the entire surface. The results are shown here. The next step is to remove all the polysilicon except that which covers the area(s) which will be used as the _____ (source and drain/source/gate/drain).

(147)



(148) gate

Next, with the polysilicon gate acting as a mask, all the thin oxide except that directly beneath the gate is removed. The next step, diffusion, is shown here. At the conclusion of this step, the source and drain diffusions will be complete. Because the gate itself acted as a mask during the diffusion, the only gate overlap will be the result of _____.

---

(149) sideways or radial diffusion

This overlap would be considerably less than in the non-self-aligning processes discussed earlier. As a result, the gate capacitance would be lower and the switching speed of the resultant MOSFET would be _____ (slower/faster).

---

(150) faster

Another feature of the self-aligning silicon gate is one that is sometimes called "immediate passivation". This simply means that the thin gate oxide is covered ("passivated") by the polysilicon immediately after it is formed. The gate oxide is therefore not exposed during later steps in the construction. This fact would make oxide damage due to contamination _____ (more/less) likely.

---

(151) less

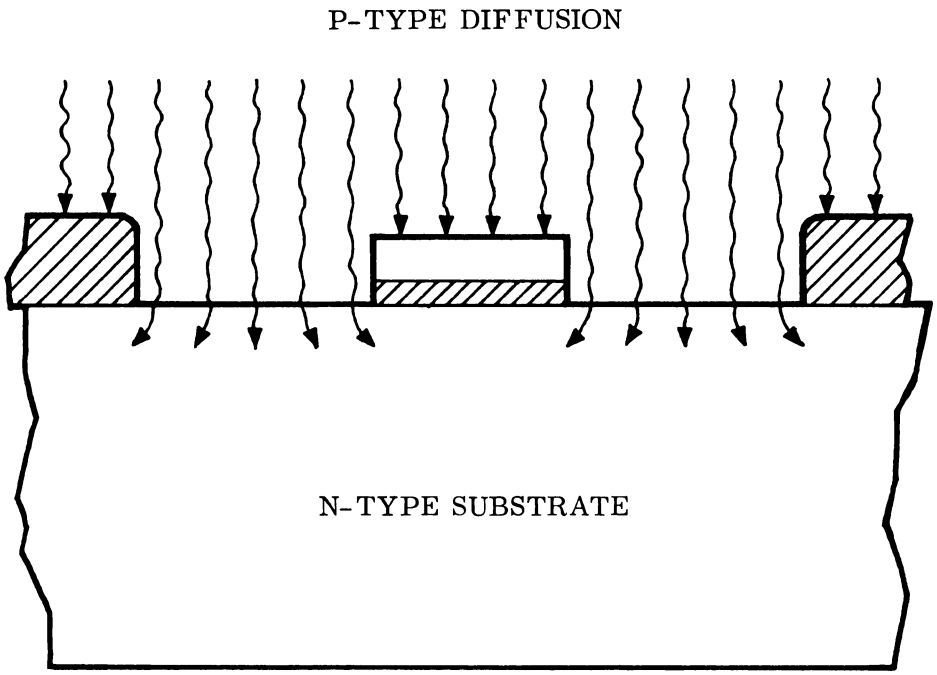
Compared to non-self-aligning metal gates, then, the self-aligning silicon gate produces three advantages. These advantages are:

_____

_____

_____

(148)
(149)
(150)
(151)



(152) Low threshold voltage

Smaller gate capacitance, or higher switching speed

Less chance of oxide contamination, or immediate passivation

The other type of self-alignment involves a metal gate. In this process, the construction of the MOSFET continues normally until the stage shown here is reached. Notice that the source and drain diffusions are both too _____ (large/small).

---

(153) small

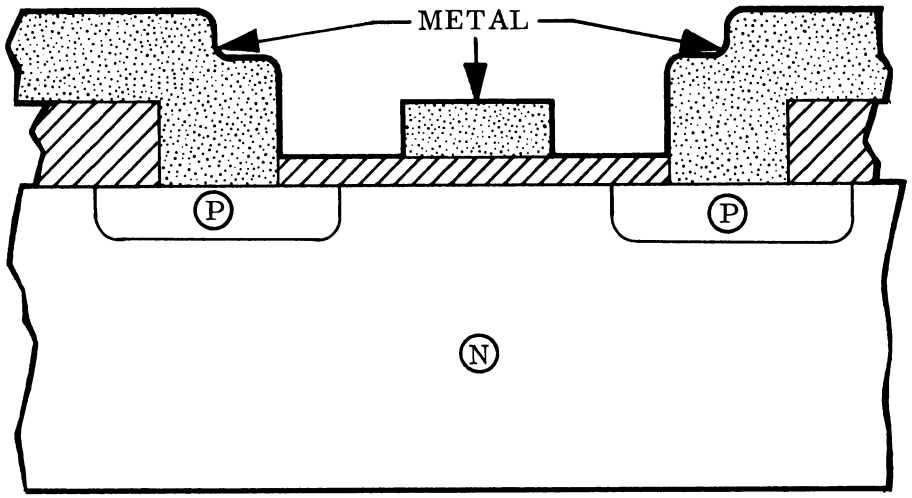
This was done purposely. The source and drain will both be extended by ion implantation as shown in the illustration. The metal gate acts as a mask and blocks the ions. In a MOSFET constructed using this process, the gate overlap would be _____ (roughly the same as that for a self-aligning silicon gate/roughly the same as that for a non-self-aligning metal gate/essentially zero).

---

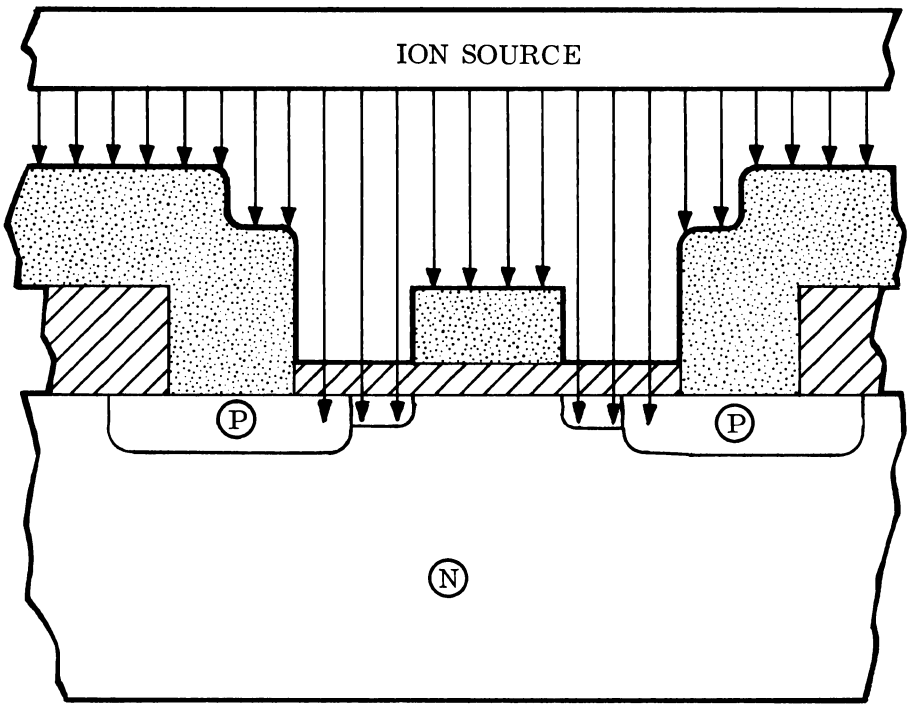
(154) essentially zero

Ion implantation is pretty much a "line of sight" process. Unlike diffusion, it produces no sideways migration of the ions. The substrate shielded by the gate metal will remain unchanged. Compared to the self-aligning silicon gate MOSFET, then, the self-aligning metal gate MOSFET would be _____ (faster/slower) and would have a _____(higher/lower)threshold voltage.

(152)



(153)
(154)



(155) faster (because of the lower gate capacitance)

higher (because of the metal gate work function)

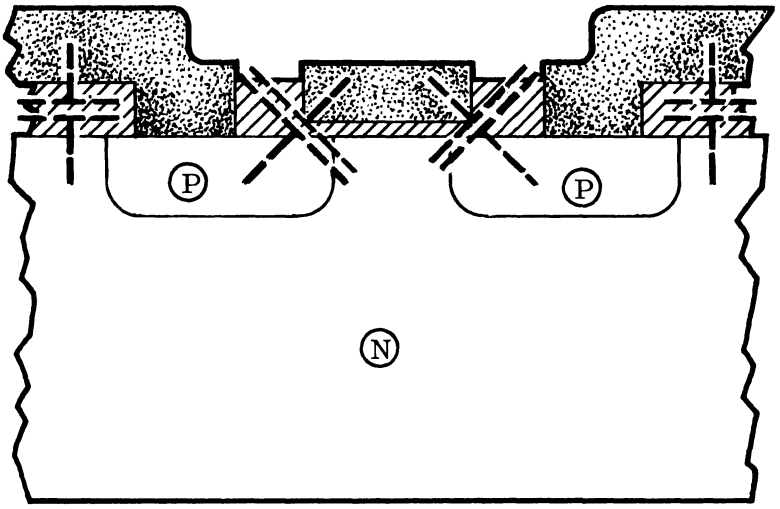
Even with gate overlaps virtually eliminated, however, the parasitic capacitances still exist, and these hamper switching speed equally as much as the gate capacitances. Recall that parasitic capacitances were primarily between the metal interconnections and the _____.

---

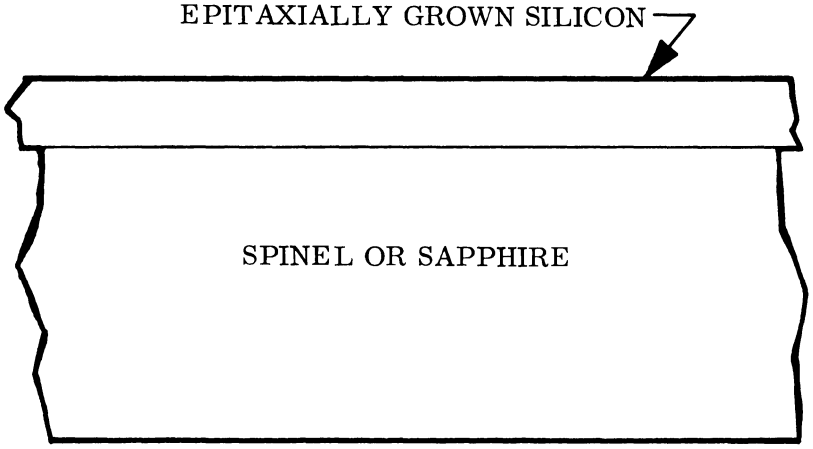
(156) substrate, or bulk substrate

A simple way of eliminating parasitic capacitances, then, would be to eliminate the bulk substrate. In one construction process, called SIS (silicon on insulated substrate), this is exactly what is done. Instead of starting with a wafer of doped silicon, this process starts with a wafer of insulating material, usually either sapphire or an artificial metal oxide crystal called spinel. A thin layer of silicon is then grown epitaxially on the surface of the wafer of insulating material. Notice that the silicon is grown epitaxially, not deposited. This means that the silicon is a _____ (conductor/semiconductor).

(155)



(156)



(157) semiconductor

Portions of this layer of silicon are then removed, leaving completely isolated silicon "islands" such as the ones shown here. Each individual island can then be doped so as to form the source, channel, and drain of a MOSFET. In the center island of the illustration, indicate the type of doping necessary to form the source, channel, and drain of a P-channel enhancement MOSFET.

---

(158) The necessary doping is shown in the illustration.

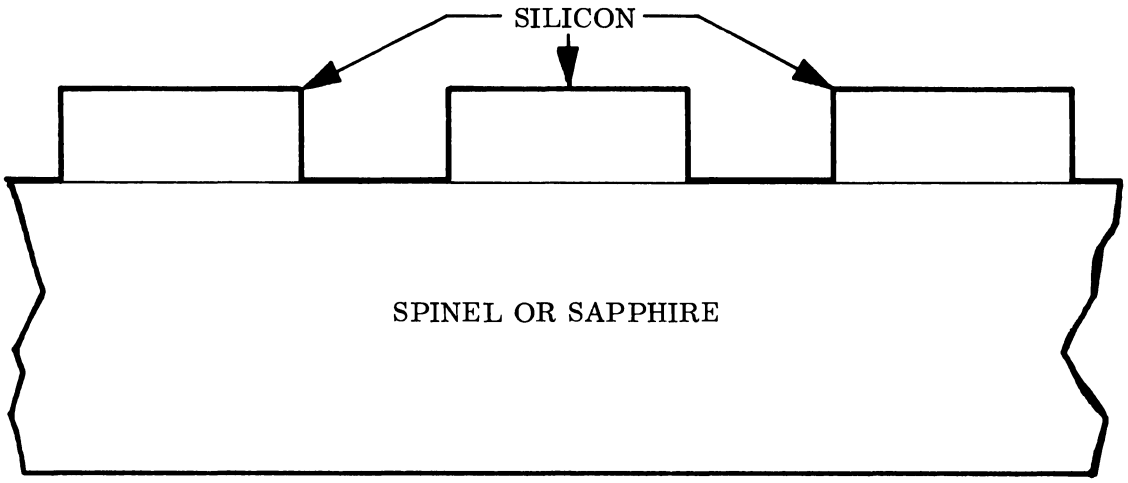
Following the doping, a thin layer of oxide is grown over the channel area, and the metal connections, including the gate and the drain and source contacts, are deposited. The interconnections from one MOSFET to another _____ (would/would not) have to be insulated from the substrate.

---

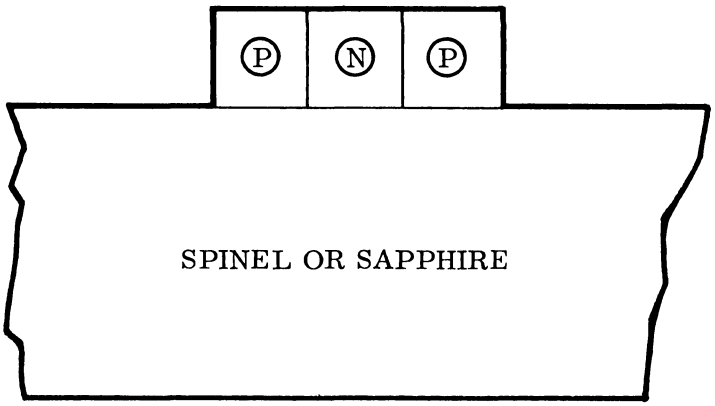
(159) would not

Because the substrate is itself an insulator, the interconnections can be deposited directly on the substrate, as shown here. Since one of the "plates" of the parasitic capacitor is now an insulator, the parasitic capacitance would be _____ _____(fairly high/unchanged/virtually nonexistent).

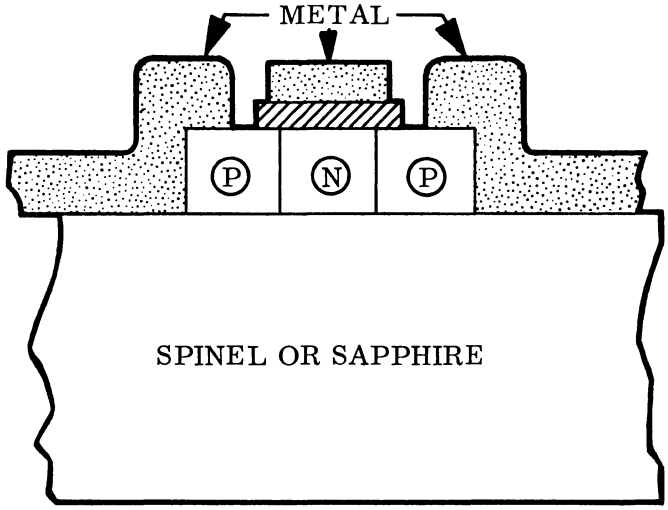
(157)


SILICON
SPINEL OR SAPPHIRE

(158)


P
N
P
SPINEL OR SAPPHIRE

(159)


METAL
P
N
P
SPINEL OR SAPPHIRE

(160) virtually nonexistent

REVIEW

1. What is meant by the term "self-aligning gate"? _____

_____

_____

2. Which type of self-aligning gate produces less gate capacitance? _____

3. In the construction of a MOSFET with a self-aligning metal gate, the source and drain are formed by _____ (diffusion/ion implantation/diffusion and ion implantation).

4. On the facing page, sketch both types of self-aligning MOSFET as they would appear during the self-alignment step.

5. On the facing page, sketch a cross section of an SIS (silicon on insulated substrate) N-channel enhancement MOSFET. Include gate metal and source and drain contacts.

(160)

(161) REVIEW ANSWERS

1. The gate itself, either metal or silicon, is used as a mask in defining the source and drain areas.

2. Metal gate, or ion implantation.

3. diffusion and ion implantation

4. See figure 1.

5. See figure 2.

(161)

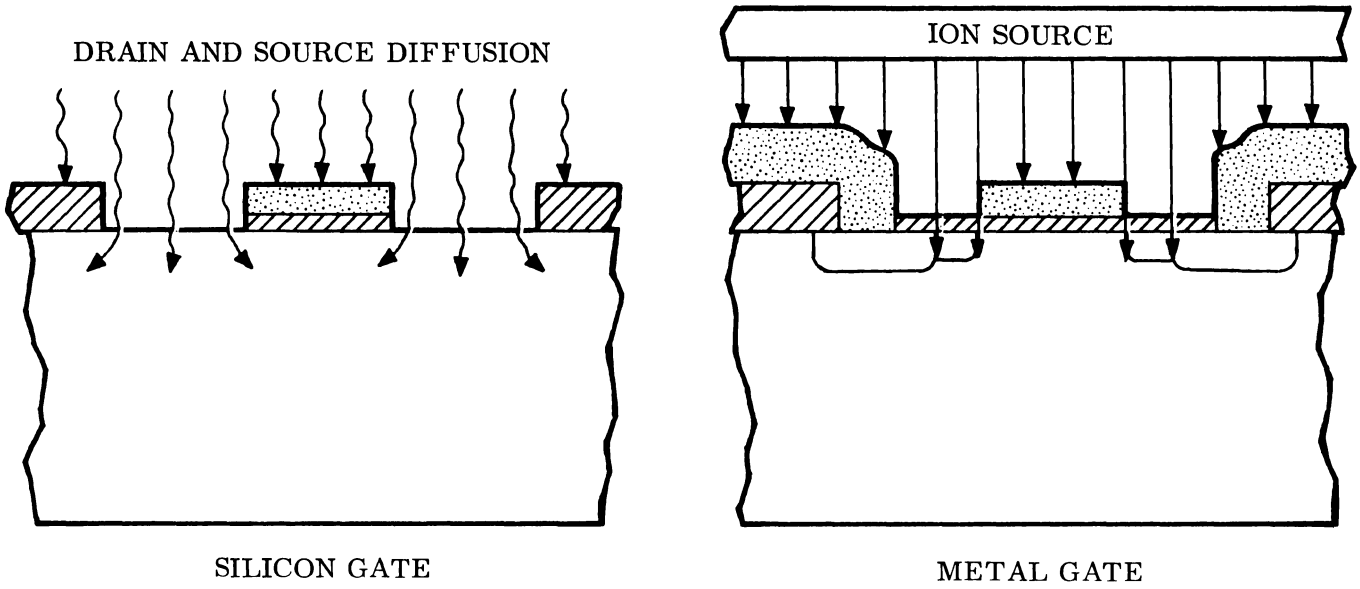


FIGURE 1

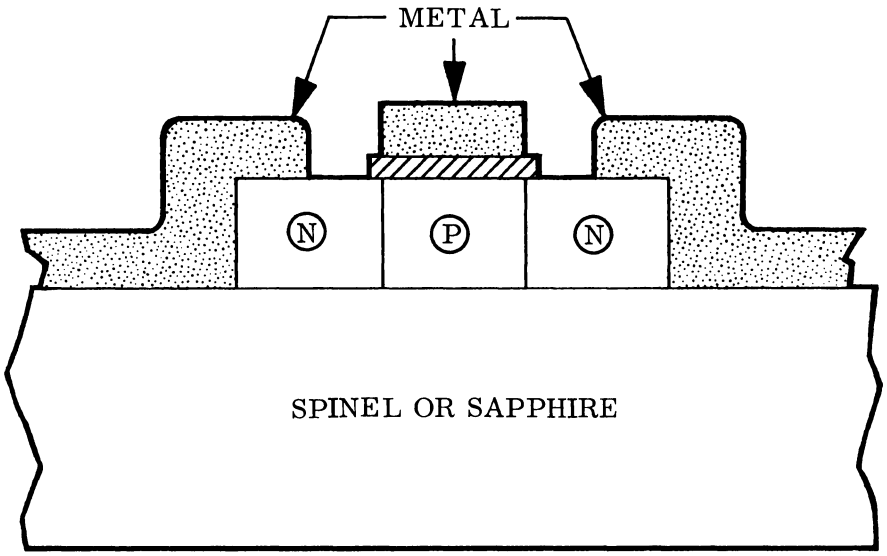


FIGURE 2

(162) As was mentioned earlier, N-channel MOSFET's, because of the higher mobility of electrons as current carriers, would be inherently more desirable than P-channel MOSFET's, but difficulties in the construction processes, particularly in the diffusion of N-type material in a P-type substrate, have slowed the development of N-channel devices. Recently, however, the construction problems have begun to be overcome, and N-channel MOSFET's are becoming more widely used.

Even with the construction problems largely overcome, however, there are still some difficulties that are unique to N-channel devices. The primary difficulty is parasitic current, and it is a result of the very thing which makes N-channel devices otherwise more desirable: higher carrier mobility. Because of the higher carrier mobility, it would be _____ (easier/harder) to induce an N-channel in a P-type substrate than it would be to induce a P-channel in an N-type substrate.

---

(163) easier

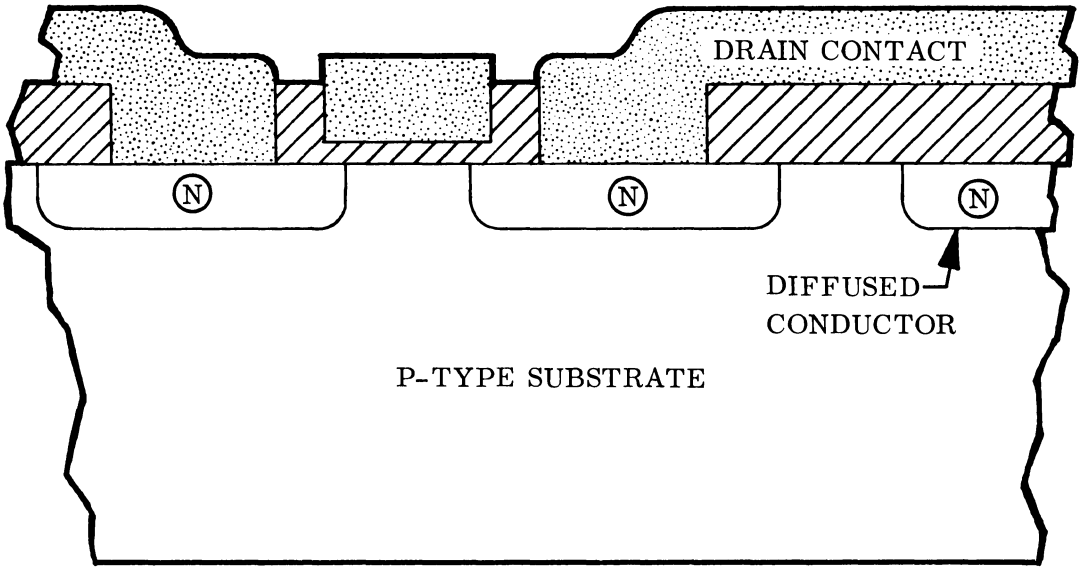
For the substrate under the gate, the easier a channel can be induced, the lower is the threshold voltage. This is, of course, a desirable situation, but what about the substrate which separates the MOSFET's from each other? If the drain voltage in the illustration was sufficiently high, the metal interconnection would act like a gate and induce a conduction channel between the _____ and the _____.

---

(164) drain and diffused conductor

The voltage necessary to induce a channel in this way is called the field threshold. There are two ways of raising this field threshold voltage so that such unwanted channels are not induced. One way is to make the oxide layer _____ (thicker/thinner). Another way is to _____ (increase/decrease) the P-type doping concentration in the substrate.

(162)
(163)
(164)



(165) thicker

increase

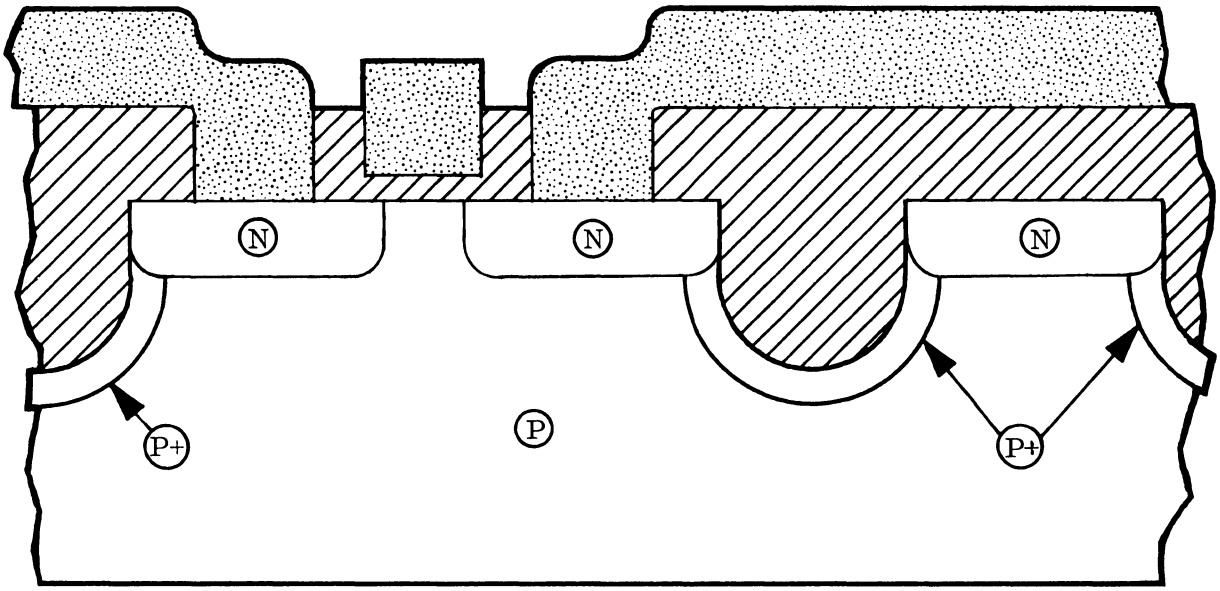
Thickening the oxide layer is simply the reverse of what is done to make the gate threshold voltage low. Increasing the doping concentration is similar to the ion implantation method of adjusting the threshold level. The only differences are that a different and more complicated procedure is used to change the doping concentration and the threshold is raised rather than lowered. One method which accomplishes both of these objectives, as well as some others which we haven't discussed, is called Coplamos. A cross section of the same circuit we have been discussing is shown here as it would appear if it had been built using the Coplamos method. In the Coplamos method, all diffused areas, including conductors, are on built-up areas, or mesas, separated by deep wells of oxide. In addition, each oxide well is lined with a more heavily doped layer of silicon. As a result, parasitic current is virtually eliminated. Parasitic capacitance would _____ _____(be raised/also be lowered).

---

(166) also be lowered

Because of the much thicker layer of oxide, the separation between the plates would be greater and the capacitance, of course, would be smaller. Of the MOSFET structures we have discussed, the only one with lower parasitic capacitance and greater component-to-component isolation would be the _____ _____structure.

(165)
(166)



(167) SIS, or silicon on insulated substrate

Another advantage of Coplamos is shown here. In the circuit in this illustration, the indicated contact misalignment could cause unwanted drain-to-substrate current flow in the _____(standard/Coplamos) structure but not in the _____ structure.

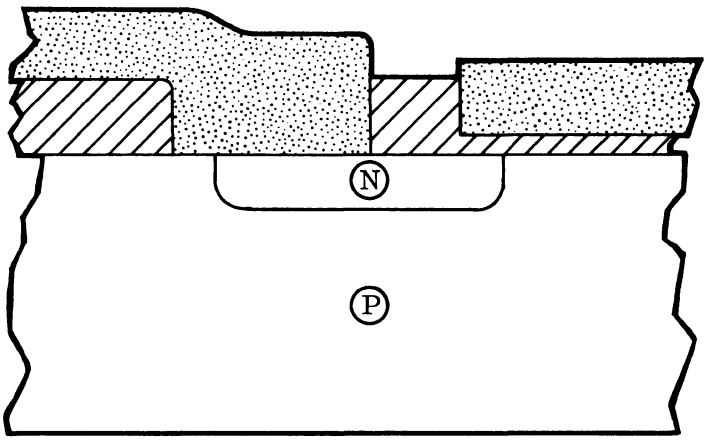
---

(168) standard

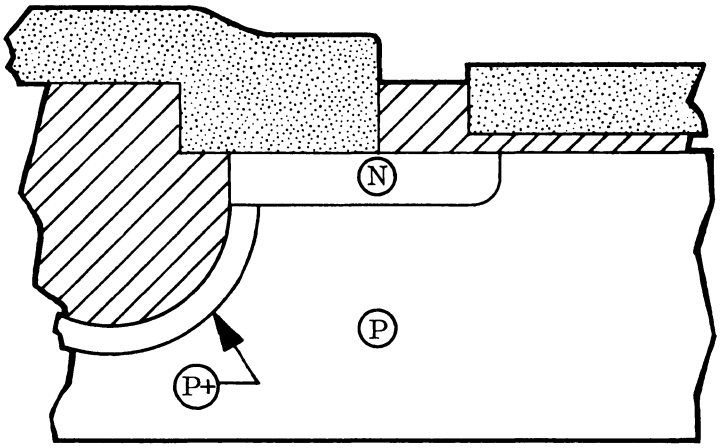
Coplamos

In the Coplamos structure the misaligned contact would touch only the oxide well, while in the standard structure it would be in direct contact with the substrate.

(167)
(168)



STANDARD



COPLAMOS

(169) REVIEW

1. One major problem which is much more pronounced in N-channel MOSFET's than it is in P-channel MOSFET's is that of _____.

2. List two ways of overcoming the problem in question 1.

_____

_____

3. Sketch a cross section of a pair of diffused conductors in a Coplamos structure.

4. In a Coplamos structure, small misalignments of source and drain contacts would have _____ (more/less) effect on MOSFET operation than they would have in non-Coplamos structures.

(169)

(170) REVIEW ANSWERS

1. parasitic current

2. Thickening the oxide.

   Increasing the substrate doping concentration.

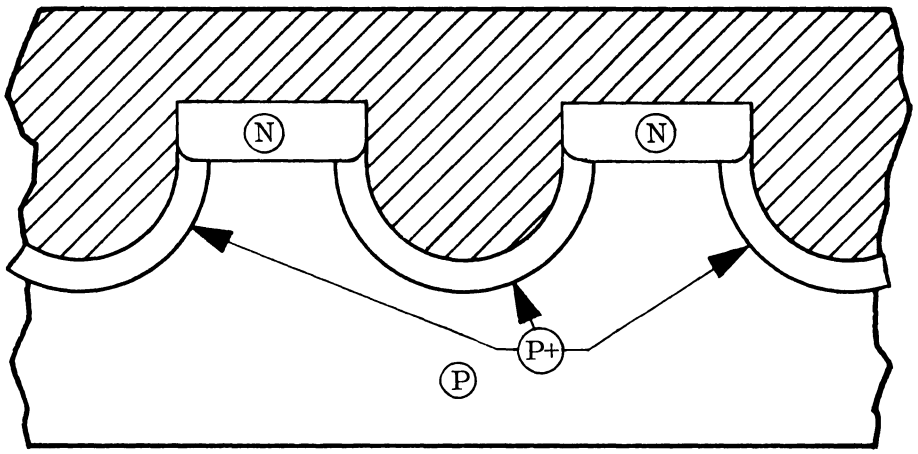
3. See illustration.

4. less

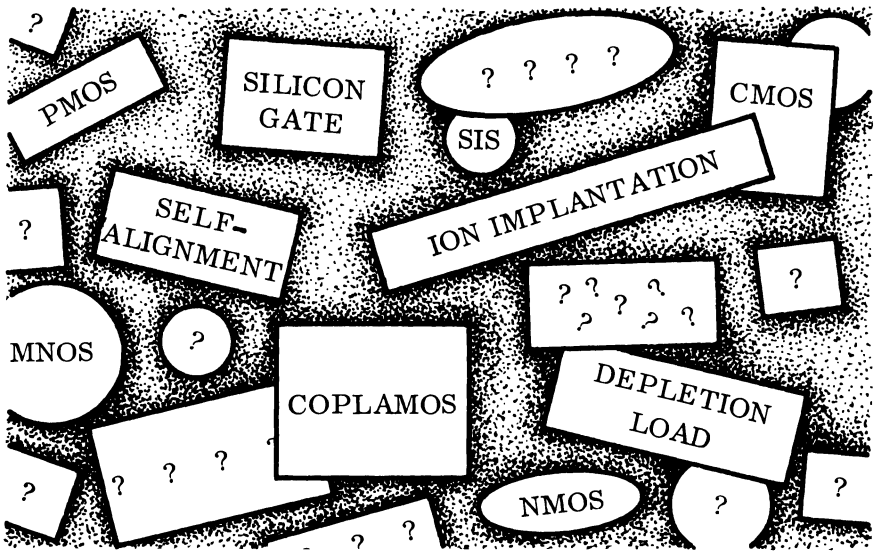
---

(171) This text has by no means covered all existing MOS technologies. It has discussed only the basic ones, and it has treated each technology (e.g., silicon gate, CMOS, MNOS, ion implantation, etc.) separately. The separate treatments have been primarily for convenience; that is, the subjects were easier to explain separately than together. This does not mean that, in reality, the different technologies are never combined in a single MOSFET. On the contrary, it would be unusual to find a modern MOSFET construction process that did not combine two or more technologies. And, with new technologies coming into being almost daily, the combinations can only become more numerous and more complicated in the future. Still, the basic principles and technologies presented in this text should remain applicable and provide a valuable background of understanding, regardless of the technological advances that will undoubtedly continue to be made.

(170)


N
N
P+
P

(171)


PMOS
SILICON GATE
SIS
CMOS
ION IMPLANTATION
SELF-ALIGNMENT
MNOS
COPLAMOS
DEPLETION LOAD
NMOS

SAMPLE TEST

FOR

MOS DIGITAL INTEGRATED CIRCUITS

PART I. PROBLEMS (3 points per blank)

1. Which of the four basic types of MOSFET is shown in figure 1?

_____

With the voltage applied as shown, the source is pin _____.

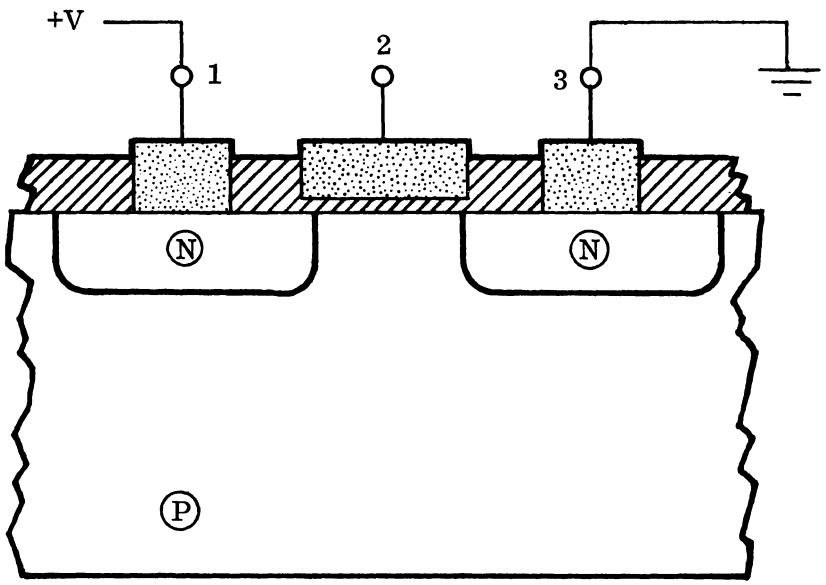


FIGURE 1

2. Which of the four basic types of MOSFET is shown in figure 2?

_____

With the voltage applied as shown, the source is pin _____.

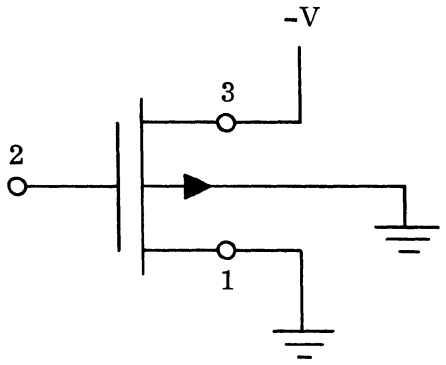


FIGURE 2

3. What is the maximum output voltage that can be obtained from each of the circuits in figure 3? Assume the threshold voltage to be -2 volts in all cases.

A. _____

B. _____

C. _____

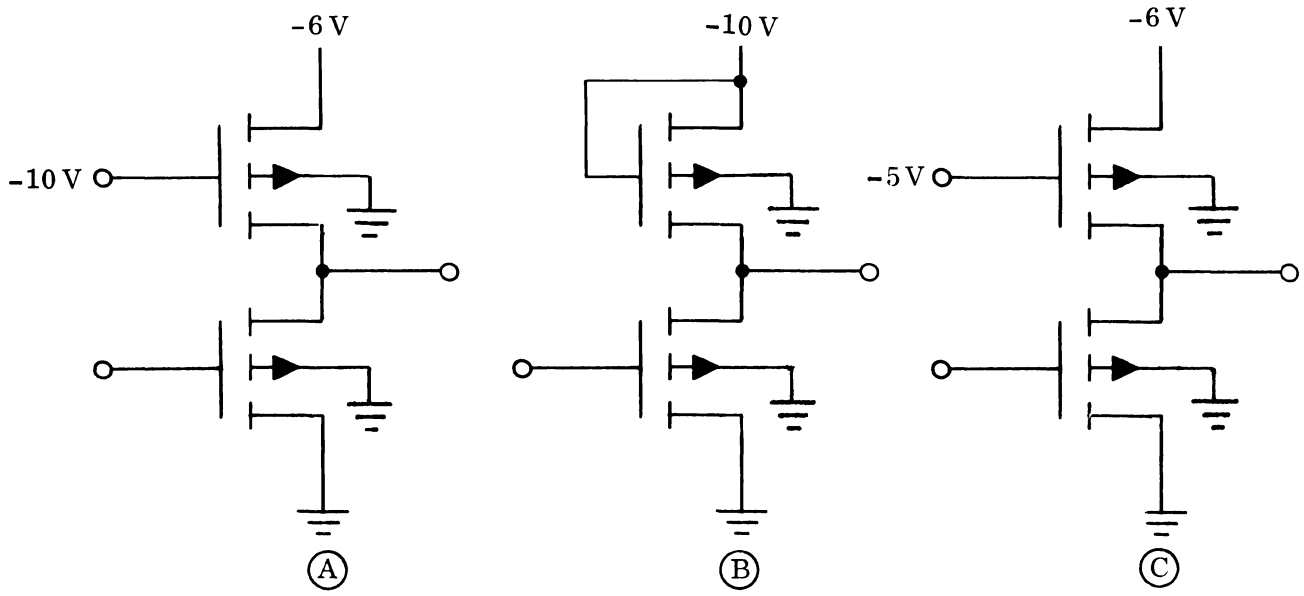


FIGURE 3

4. A 3-input CMOS NOR gate would contain how many MOSFET's? _____

5. A 4-input PMOS NAND gate would contain how many MOSFET's? _____

6. Identify the lettered items in figure 4 (i.e., metal, N-type material, oxide, etc.). Assume the illustrated cross-section shows part of an MNOS P-channel enhancement MOSFET.

A. _____

B. _____

C. _____

D. _____

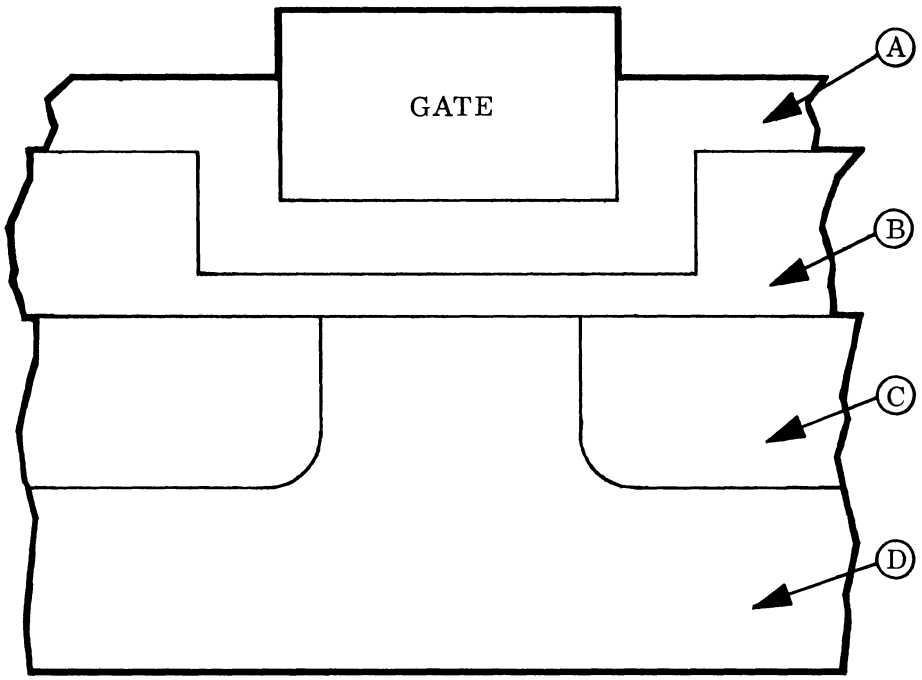


FIGURE 4

7. In Coplamos construction, parasitic current is reduced by what two methods?

_____

_____

8. In SIS construction, the first step is to grow a layer of _____ on the surface of a wafer of _____.

PART II. MULTIPLE CHOICE (3 points per answer)

NOTE: More than one choice may be correct in each question. Indicate all correct choices.

9. Compared to a PMOS inverter, a CMOS inverter would be _____.

A. faster but more susceptible to noise

B. faster and less susceptible to noise

C. slower but would use less power

D. faster but would use more power

E. faster and would use less power

10. MOSFET is synonymous with _____.

A. MOS device

B. IGFET

C. FET

D. field effect device

11. Silicon conductors can be _____.

A. either deposited or diffused

B. only diffused

C. used more advantageously in circuits in which current flow is low

D. used more advantageously in circuits in which current flow is high

E. only deposited

12. The circuit shown in figure 5 is _____ .

A. a PMOS NAND gate

B. a PMOS NOR gate

C. A CMOS NAND gate

D. A CMOS NOR gate

E. an NMOS NOR gate

F. none of the above

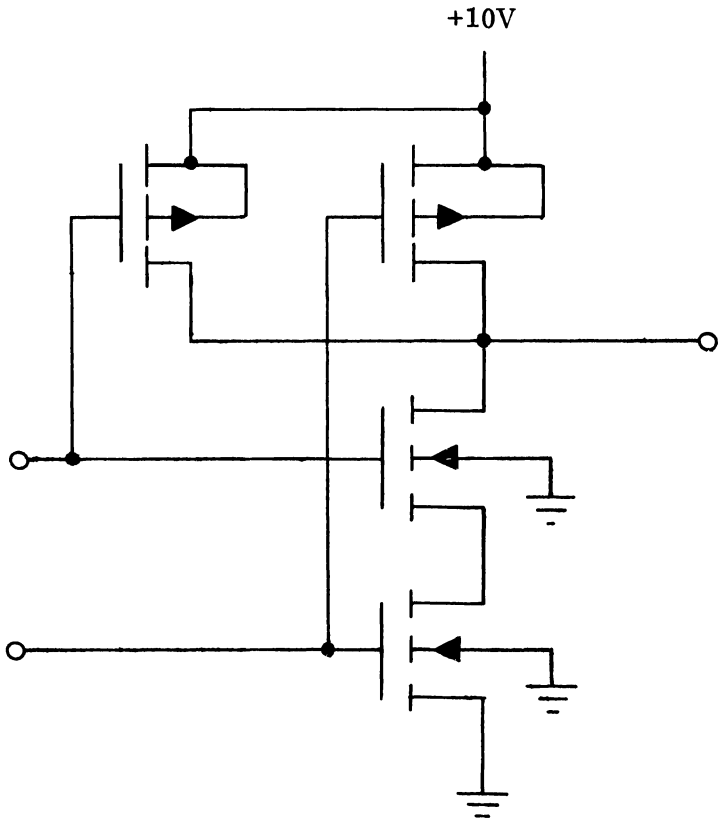


FIGURE 5

13. A self-aligning silicon gate _____ .

A. results in less gate capacitance than a self-aligning metal gate

B. results in more gate capacitance than a self-aligning metal gate

C. results in less parasitic capacitance than a self-aligning metal gate

D. is used as a mask during the diffusion of the source and drain

E. is used as a mask during an ion implantation step

F. results in a lower gate threshold voltage than a self-aligning metal gate

G. cannot be made

14. In a PMOS inverter using a depletion MOSFET as a load, the gate of the depletion MOSFET is tied to _____ .

A. a separate power supply

B. its source

C. its drain

D. its substrate

E. ground

15. In constructing a MOSFET with a self-aligning metal gate, _____.

A. ion implementation is not used

B. the source and drain are completely formed by ion implantation

C. the source and drain are completely formed by diffusion

D. the source and drain are formed partly by ion implantation and partly by diffusion

E. the source and drain diffusions are done after the gate is formed

PART III. TRUE OR FALSE (2 points each)

T — F 16. In a CMOS inverter, the gates of the two MOSFET's are tied together.

T — F 17. In a CMOS inverter, one MOSFET is an N-channel enhancement type and the other is a P-channel depletion type.

T — F 18. All other things being equal, the field threshold of an N-channel device would be higher than the field threshold of a P-channel device.

T — F 19. The greater the difference between the gate and substrate work functions, the lower the threshold voltage will be.

T — F 20. Polysilicon is heavily doped silicon that has been grown epitaxially.

T — F 21. If the ion implantation method of threshold adjustment is continued long enough, an enhancement MOSFET can be changed to a depletion MOSFET.

T — F 22. Gate capacitance and parasitic capacitance are both factors in slowing down the switching speed of a MOSFET.

T — F 23. If a MOSFET has a pinch-off voltage of -3 volts, it has to be an N-channel depletion MOSFET.

SAMPLE TEST ANSWERS

PART I. PROBLEMS

1. N-channel enhancement
   3
2. P-channel depletion
   1
3. A. -6 volts
   B. -8 volts
   C. -3 volts
4. 6
5. 5
6. A. silicon nitride, or Si_3N_4
   B. oxide, or silicon dioxide, or SiO_2
   C. P-type material
   D. N-type material
7. Wells of oxide between components
   Layer of extra heavily doped material immediately under the oxide layer
8. silicon
   sapphire, or spinel, or insulating material

PART II. MULTIPLE CHOICE

9. B. faster and less susceptible to noise
   E. faster and would use less power
10. B. IGFET
11. A. either deposited or diffused
    C. used more advantageously in circuits in which current flow is low
12. C. a CMOS NAND gate
13. B. results in more gate capacitance than a self-aligning metal gate
    D. is used as a mask during the diffusion of the source and drain
    F. results in a lower gate threshold voltage than a self-aligning metal gate
14. B. its source
15. D. the source and drain are formed partly by ion implantation and partly by diffusion

PART III. TRUE OR FALSE

16. TRUE
17. FALSE
18. FALSE
19. FALSE
20. FALSE
21. TRUE
22. TRUE
23. TRUE

FROM

_____

_____

_____

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EXAMINATION-A
INTRODUCTION TO MOS DIGITAL INTEGRATED CIRCUITS

Approximate time required to complete the text -_____ Hours

Approximate time required to complete this examination -_____ Minutes

NAME: _____

DEPARTMENT: _____

PLANT, BLDG. NO., OR FIELD
MAILING ADDRESS: _____

_____

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ZIP CODE: _____

DATE: _____

SS NO. _____

This exam is to be completed without the use of notes or other reference material.

PART I. PROBLEMS (2-1/2 points per blank)

1. Name the four basic types of MOSFET.

_____

_____

_____

_____

2. Which type of MOSFET is shown in figure 1? _____
With the voltage applied as shown, the source is pin_____.

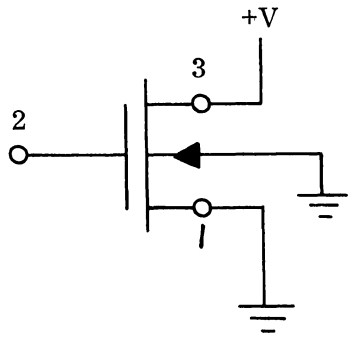

FIGURE 1

3. Which type of MOSFET is shown in Figure 2? _____
With the voltage applied as shown, the source is pin ____.

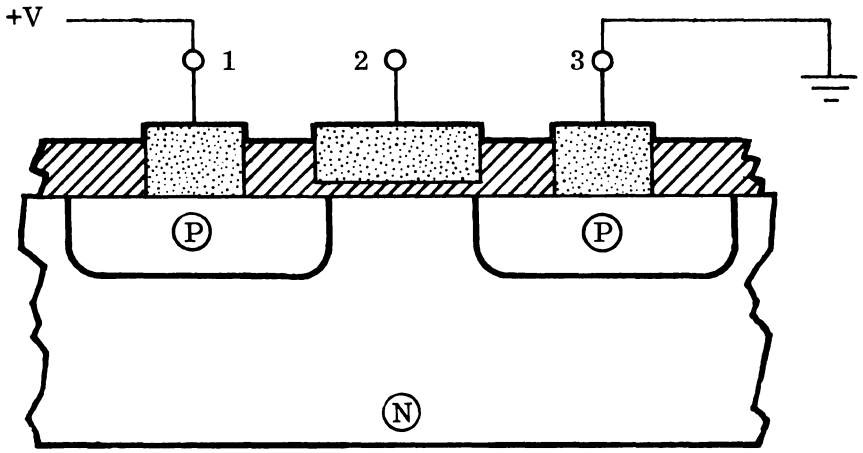

FIGURE 2

4. IGFET is an acronym for _____.

5. What is the maximum the output of each of the circuits in figure 3 can reach? Assume the threshold voltage to be -3 volts in all cases.

A. _____

B. _____

C. _____

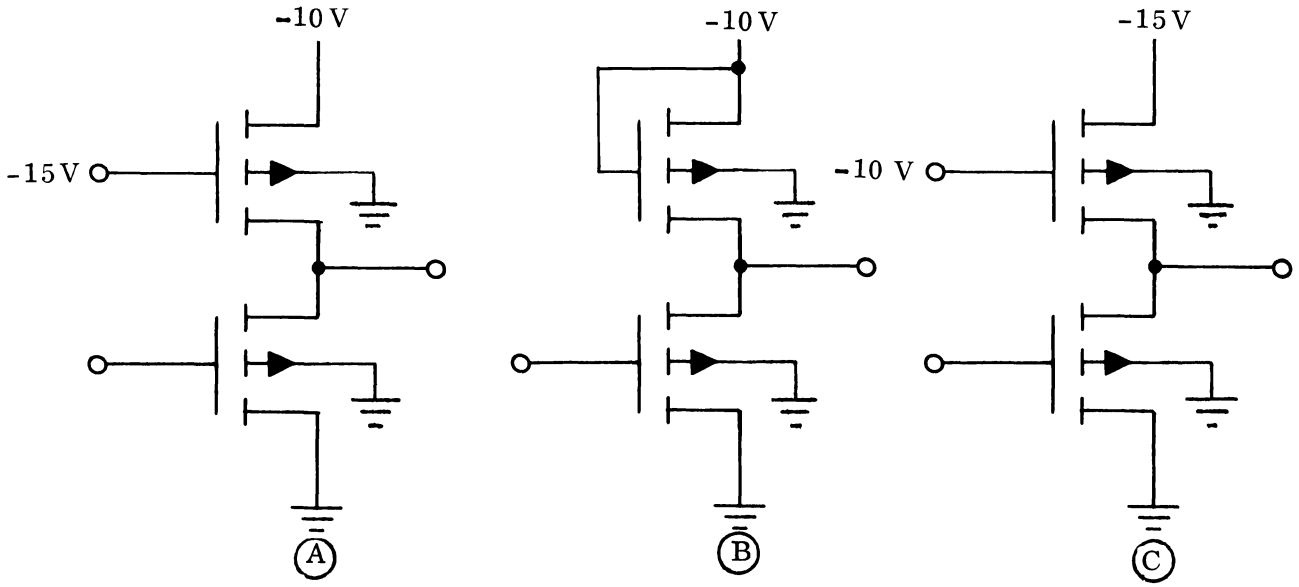

FIGURE 3

6. Which type of inverter listed below would use the most power? _____

The least power? _____

Which would need the most area for construction? _____

Which would be the most susceptible to noise? _____

A. CMOS

B. PMOS with a depletion MOSFET used as a load

C. PMOS with an enhancement MOSFET used as a load

7. SIS is an acronym for _____ .

8. Identify the lettered items in figure 4 (i.e., metal, N-type material, etc.). Assume the MOSFET shown is a P-channel enhancement type.

A. _____

B. _____

C. _____

D. _____

E. _____

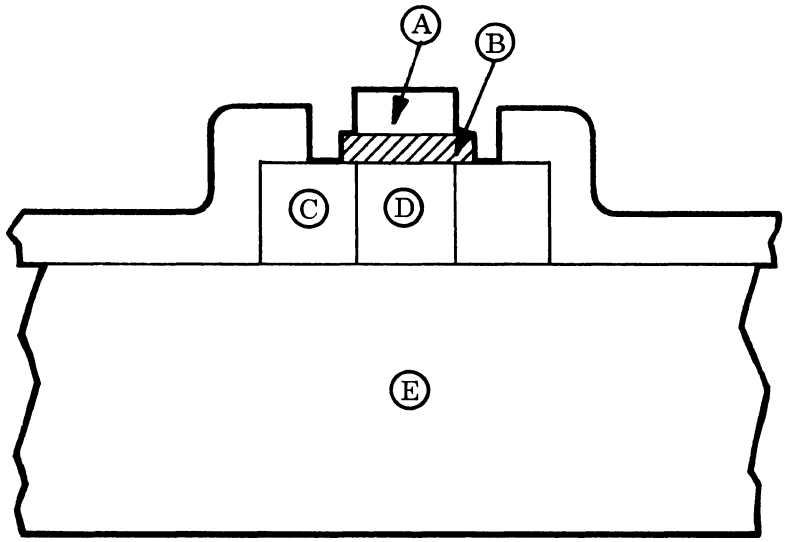

FIGURE 4

9. A 4-input CMOS NAND gate would contain how many MOSFET's? _____

10. A 4-input PMOS NOR gate would contain how many MOSFET's? _____

PART II. MULTIPLE CHOICE (2 points per answer)

NOTE: More than one choice may be correct in each question.
Indicate all correct choices.

11. A self-aligning metal gate _____.

A. cannot be made

B. results in less gate capacitance than a self-aligning silicon gate

C. results in more gate capacitance than a self-aligning silicon gate

D. results in less parasitic capacitance than a self-aligning silicon gate

E. is used as a mask during the diffusion of the source and drain

F. is used as a mask during an ion implantation step

G. results in a lower gate threshold voltage than a non-self-aligning silicon gate

12. Which of the following features are considered desirable? _____

A. High field threshold voltage

B. High gate threshold voltage

C. Low field threshold voltage

D. Low gate threshold voltage

13. The indicated areas in figure 5 are _____.

A. P-

B. P+

C. N

D. N-

E. N+

F. oxide

G. polysilicon

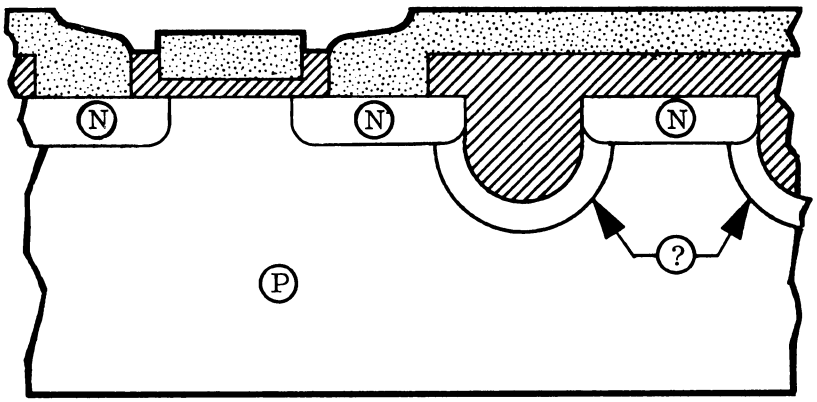

FIGURE 5

14. The purpose of the areas indicated in figure 5 is to_____.

A. lower parasitic capacitance

B. lower parasitic current

C. lower the field threshold

D. raise the field threshold

E. lower the gate capacitance

15. Parasitic current is_____.

A. more of a problem in N-channel than in P-channel devices

B. more of a problem in P-channel than in N-channel devices

C. particularly troublesome in Coplamos

D. virtually eliminated in Coplamos

E. the result of a low field threshold voltage

F. the result of a low gate threshold voltage

16. Ion implantation can be used_____.

A. to adjust gate threshold voltage

B. to make a depletion MOSFET

C. in constructing a MOSFET with a self-aligning gate

D. to reduce parasitic capacitance

17. Silicon gates are_____.

A. either deposited or grown

B. deposited rather than grown

C. often referred to as polysilicon gates

D. less conductive than the undoped silicon substrate

E. heavily doped in order to be highly conductive

18. An MNOS device _____.

A. is always N-channel

B. uses nitride in place of the thin gate oxide and the thick field oxide

C. has a lower threshold voltage than a standard PMOS device

D. uses nitride in place of part of the thin gate oxide

19. Which of the illustrations in figure 6 correctly represent a PMOS inverter using a depletion MOSFET as a load? _____

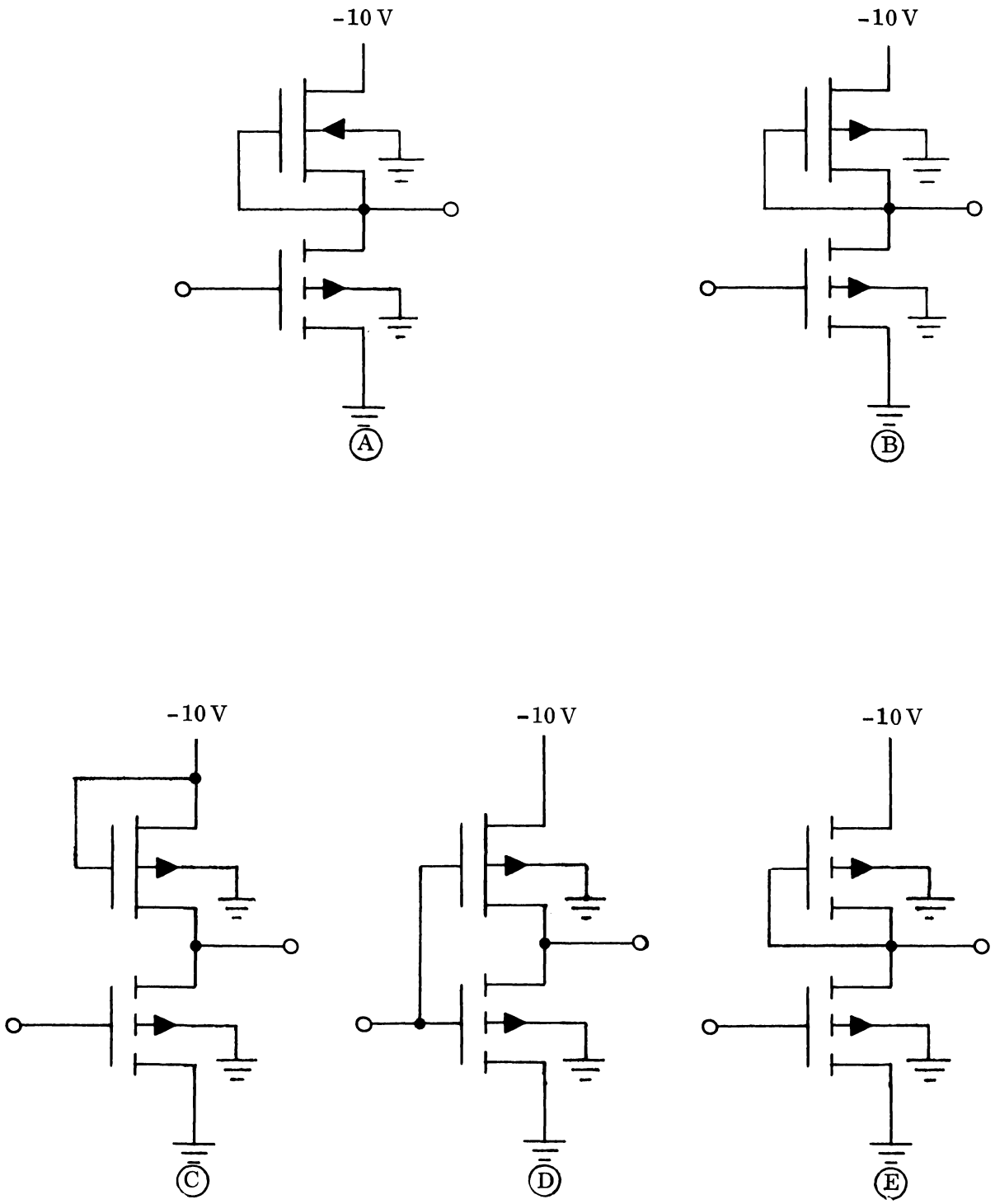

FIGURE 6

20. Which of the illustrations in figure 7 correctly represents a CMOS inverter?_____

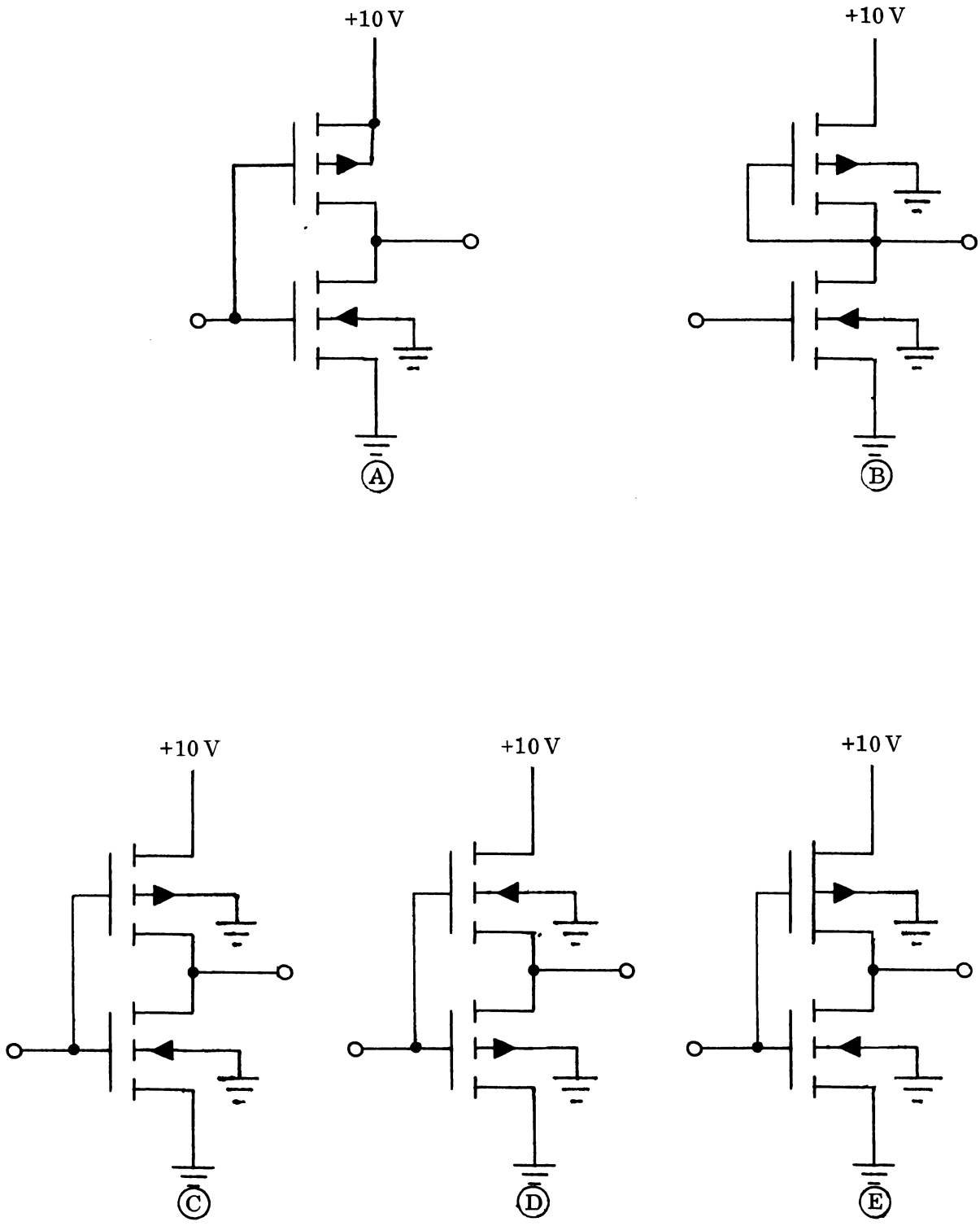

FIGURE 7

21. The circuit shown in figure 8 is _____.

A. a CMOS NOR gate

B. a PMOS NOR gate

C. an NMOS NOR gate

D. a CMOS NAND gate

E. a PMOS NAND gate

F. an NMOS NAND gate

G. none of the above

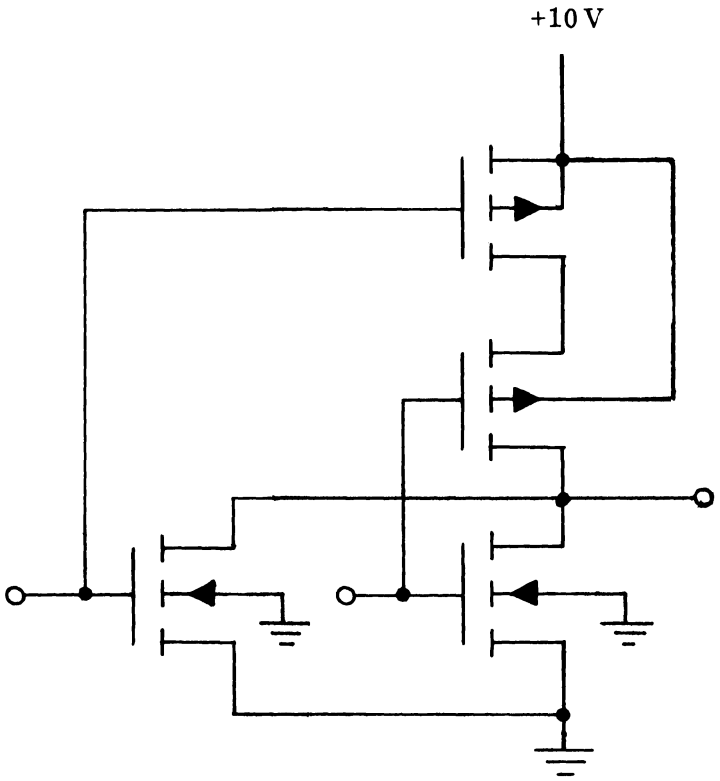

FIGURE 8

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