

USER'S GUIDE

A.C.T.

CACHE/434

&

CACHE/440

*See p 8-4 for
use as bus terminator
* register DIP's ..*

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by

ABLE COMPUTER TECHNOLOGY, INC.

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SECTION 1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This User's Guide contains the necessary information to install and benchmark the product in the appropriate computer.

SECTION 2 Provides general mechanical information pertaining to the PDP11/34 and illustrates the proper location of the CACHE/434.

SECTION 3 Provides general mechanical information pertaining to the PDP 11/40 and illustrates the proper location of the CACHE/440.

SECTION 4 Describes the Cache controls and indicators.

SECTION 5 Installation procedure for the CACHE/434.

SECTION 6 Installation procedure for the CACHE/440.

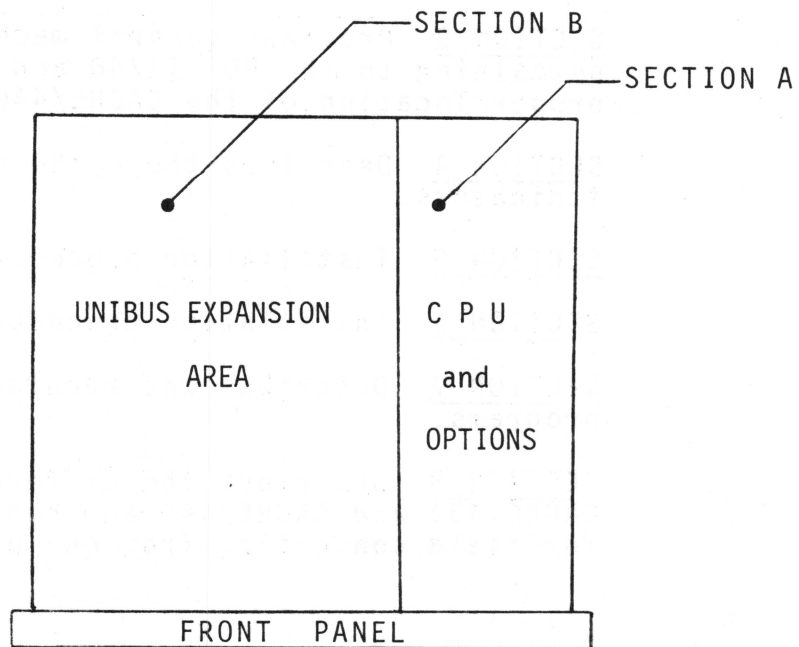
SECTION 7 Describes the running of benchmark programs.

SECTION 8 Describes the differences between the CACHE/434 and CACHE/440 and contains a procedure for **field converting** from one product to the other.

SECTION 2
CACHE/434 MECHANICAL INFORMATION

2.1 PDP 11/34 PHYSICAL LAYOUT

The PDP 11/34 main chassis can be discussed as 2 sections. The first 9 slot backpanel is specially prewired to accept the Central Processor and processor options. The remaining chassis space is provided for Unibus options.



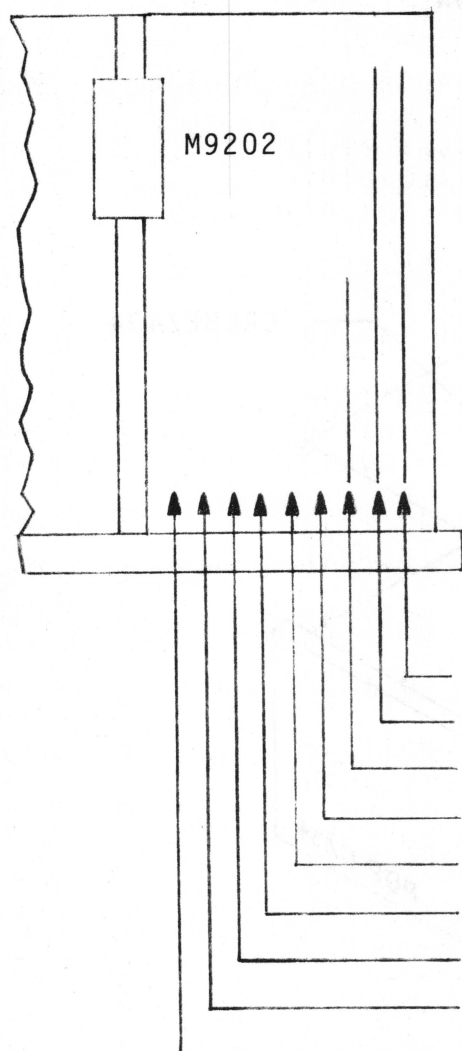
SECTION A is prewired to accept the processor.

The PDP 11/34 processor (KD11-E) consists of 3 printed circuit boards.

The PDP 11/34 A processor (KD11-EA) consists of 2 printed circuit boards.

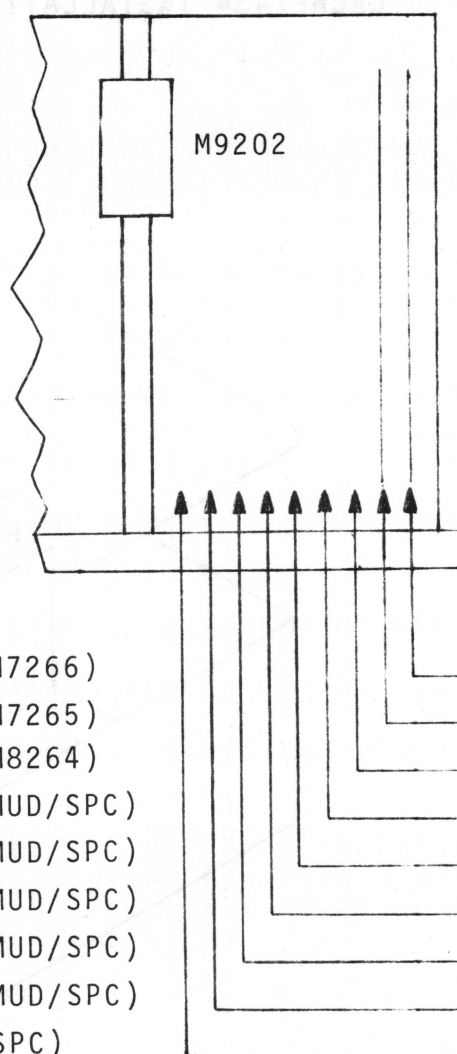
SECTION B is for Unibus expansion. Unibus compatible devices, such as memories and I/O controllers, will be installed and jumpered to the existing Unibus.

PDP 11/34



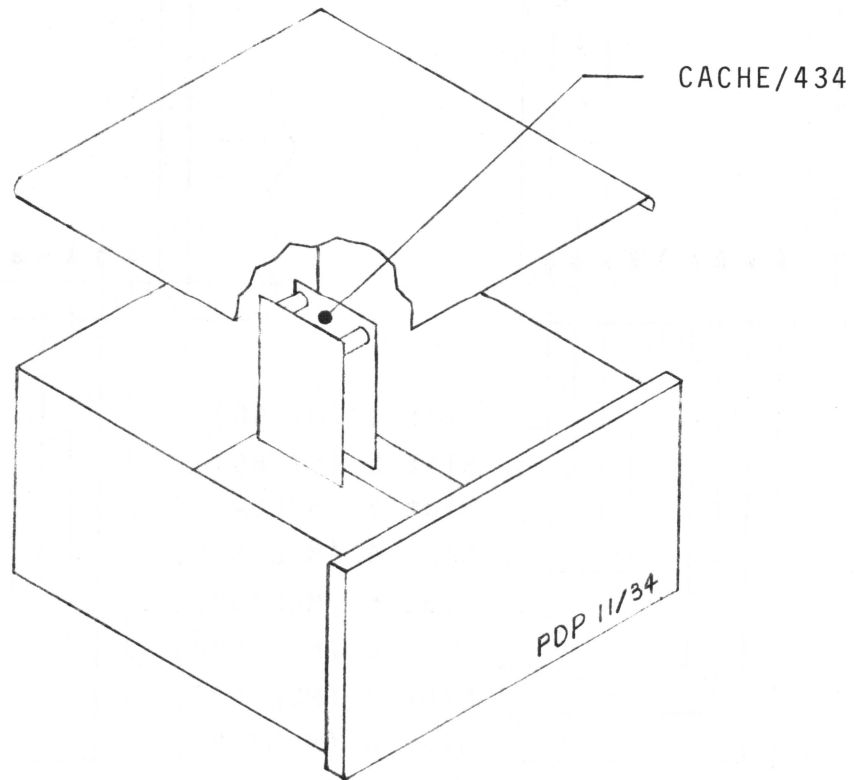
Slot 1 (M7266)
 Slot 2 (M7265)
 Slot 3 (M8264)
 Slot 4 (MUD/SPC)
 Slot 5 (MUD/SPC)
 Slot 6 (MUD/SPC)
 Slot 7 (MUD/SPC)
 Slot 8 (MUD/SPC)
 Slot 9 (SPC)

PDP 11/34A



Slot 1 (M8266)
 Slot 2 (M8265)
 Slot 3 (MUD/SPC)
 Slot 4 (MUD/SPC)
 Slot 5 (MUD/SPC)
 Slot 6 (MUD/SPC)
 Slot 7 (MUD/SPC)
 Slot 8 (MUD/SPC)
 Slot 9 (SPC)

2.2 CACHE/434 INSTALLATION LOCATION

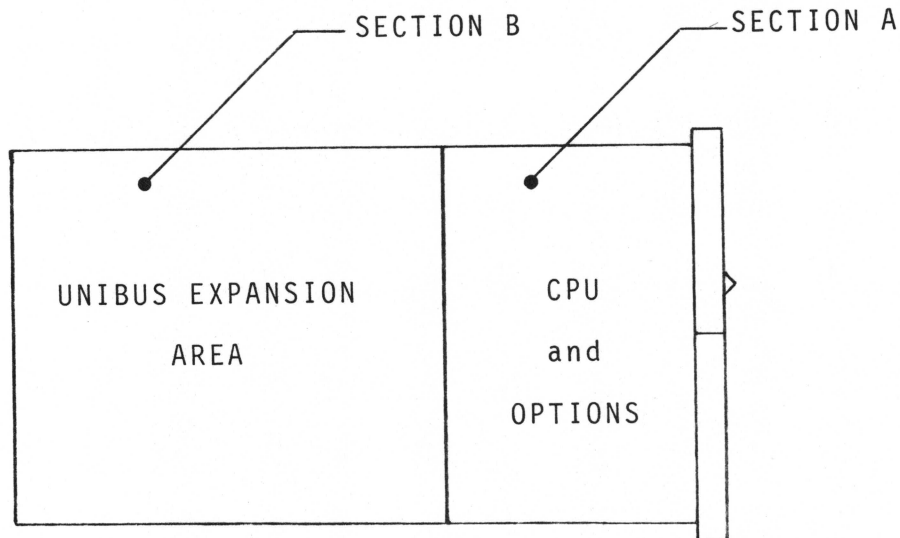


The CACHE/434 replaces the M9202 Interconnection Module.

SECTION 3
CACHE/440 MECHANICAL INFORMATION

3.1 PDP 11/40 PHYSICAL LAYOUT

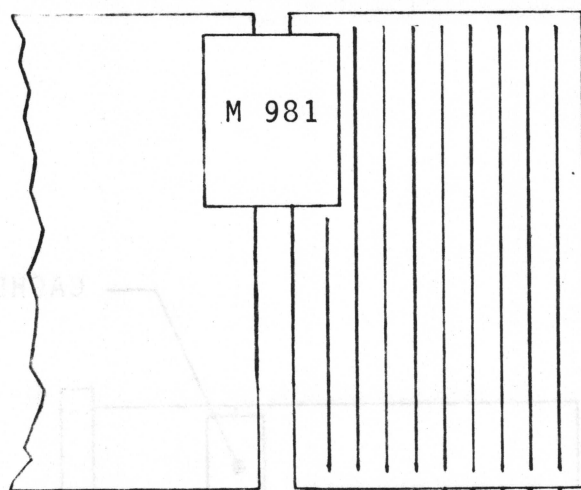
The PDP 11/40 main chassis can be discussed as 2 sections. The first 9 slot backpanel is specially prewired to accept the Central Processor and processor options. The remaining chassis space is provided for Unibus options.



SECTION A is prewired to accept the following:

Central Processor	(KD11-A)
Extended Instruction Set	(KE11-E)
Floating Point	(KE11-F)
Memory Management	(KT11-D)
Programmable Stack Limit	(KJ11-A)
Real Time Clock	(KW11-L)
SPC location	(slot 9)

SECTION B is for Unibus expansion. Unibus compatible devices, such as memories and I/O controllers, will be installed and jumpered to the existing Unibus.



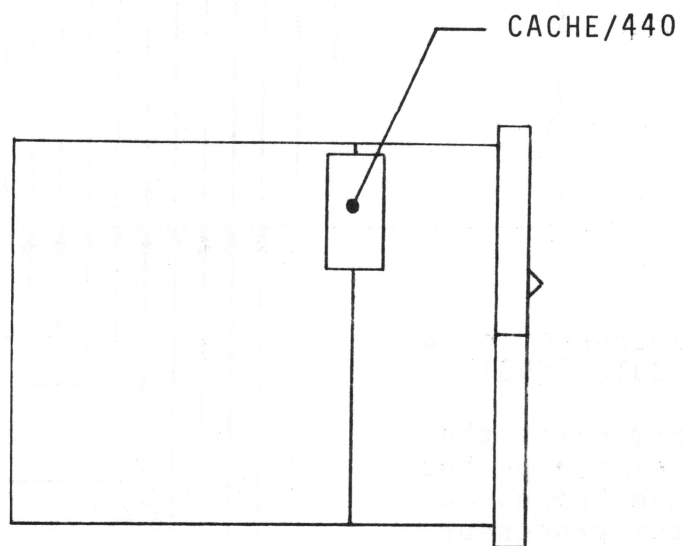
Backpanel Interconnection & Termination Module (M981)

This module terminates the processor end of the Unibus and provides the Unibus connection from the processor backpanel to the next backpanel.

- Slot 1 (M7239)
- Slot 2 (M7238)
- Slot 3 (M7232, M7237, M787)
- Slot 4 (M7231)
- Slot 5 (M7233)
- Slot 6 (M7235)
- Slot 7 (M7234)
- Slot 8 (M7236)
- Slot 9 (SPC location)

The CACHE/440 replaces the M981 Interconnection Module.

3.2 CACHE/440 INSTALLATION LOCATION



The CACHE/440 replaces the M981 Interconnection Module.

SECTION 4

CACHE CONTROL AND INDICATOR DESCRIPTIONS

4.1 ON LINE SWITCH

Controls the response of the Cache.

ON LINE POSITION - The Cache will respond with data when it contains a copy of the data being requested.

OFF LINE POSITION - The Cache will NOT respond with data even when it contains a copy of the data being requested.

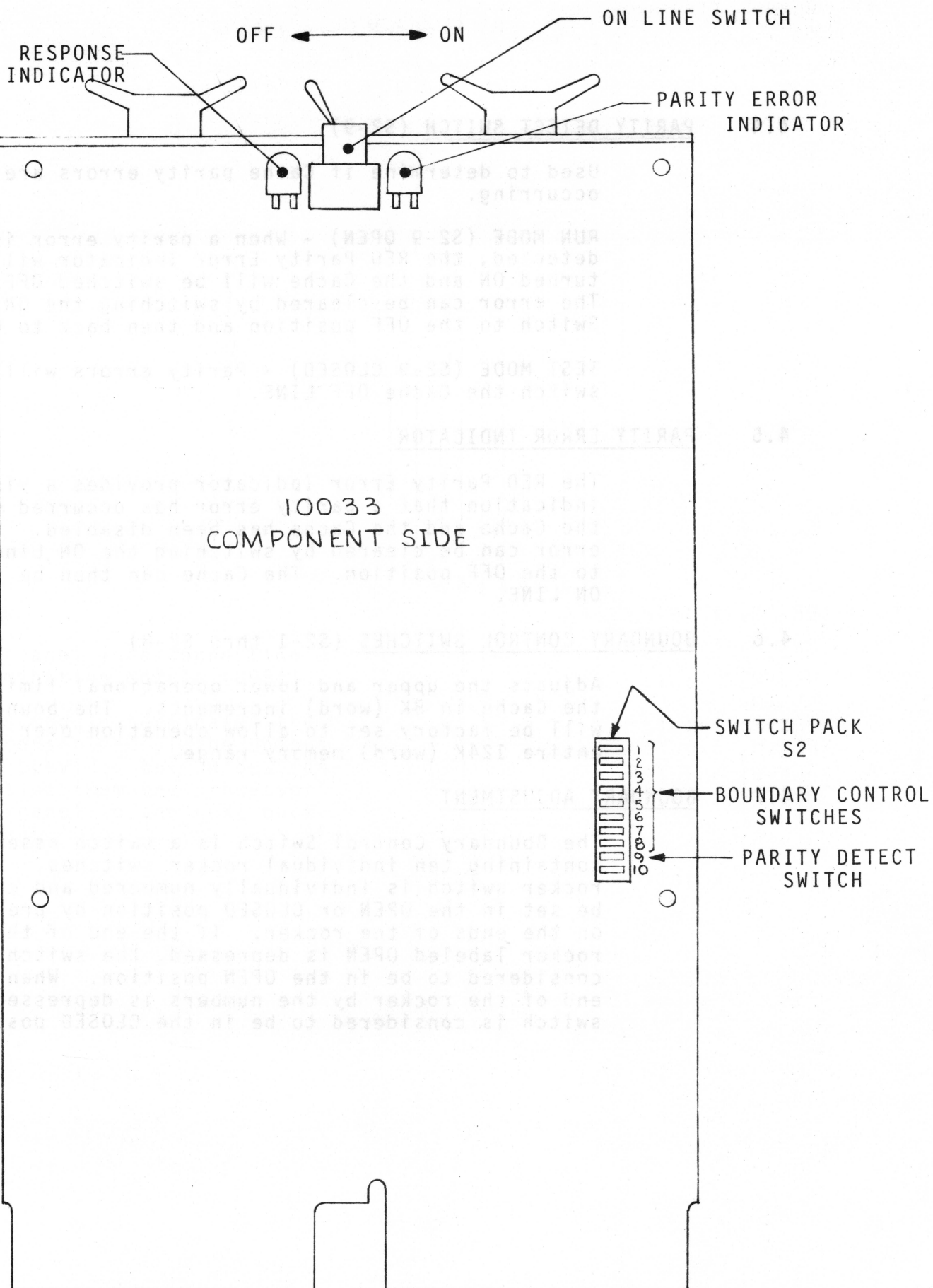
4.2 RESPONSE INDICATOR

The GREEN Response Indicator provides a visual indication when the Cache is responding with data. The light will become brighter as the percent of Cache responses increases.

4.3 CACHE PARITY DESCRIPTION

ADDRESS PARITY checks the mapping integrity of the Cache. When a mapping error is detected, the Cache will not respond with data for the current read operation, but instead, will pass the request on to the Unibus memory. Thus, preventing the Cache from providing incorrect data.

DATA PARITY checks each byte of the word for data integrity. When a data error is detected, the Cache will not respond with data for the current read operation, but instead, will pass the request on to the Unibus memory. Thus, preventing the Cache from providing incorrect data.



CACHE CONTROL LOCATION DRAWING

4.4 PARITY DETECT SWITCH (S2-9)

Used to determine if Cache parity errors are occurring.

RUN MODE (S2-9 OPEN) - When a parity error is detected, the RED Parity Error Indicator will be turned ON and the Cache will be switched OFF LINE. The error can be cleared by switching the ON Line Switch to the OFF position and then back to ON.

TEST MODE (S2-9 CLOSED) - Parity errors will not switch the Cache OFF LINE.

4.5 PARITY ERROR INDICATOR

The RED Parity Error Indicator provides a visual indication that a parity error has occurred within the Cache and the Cache has been disabled. The error can be cleared by switching the ON Line Switch to the OFF position. The Cache can then be switched ON LINE.

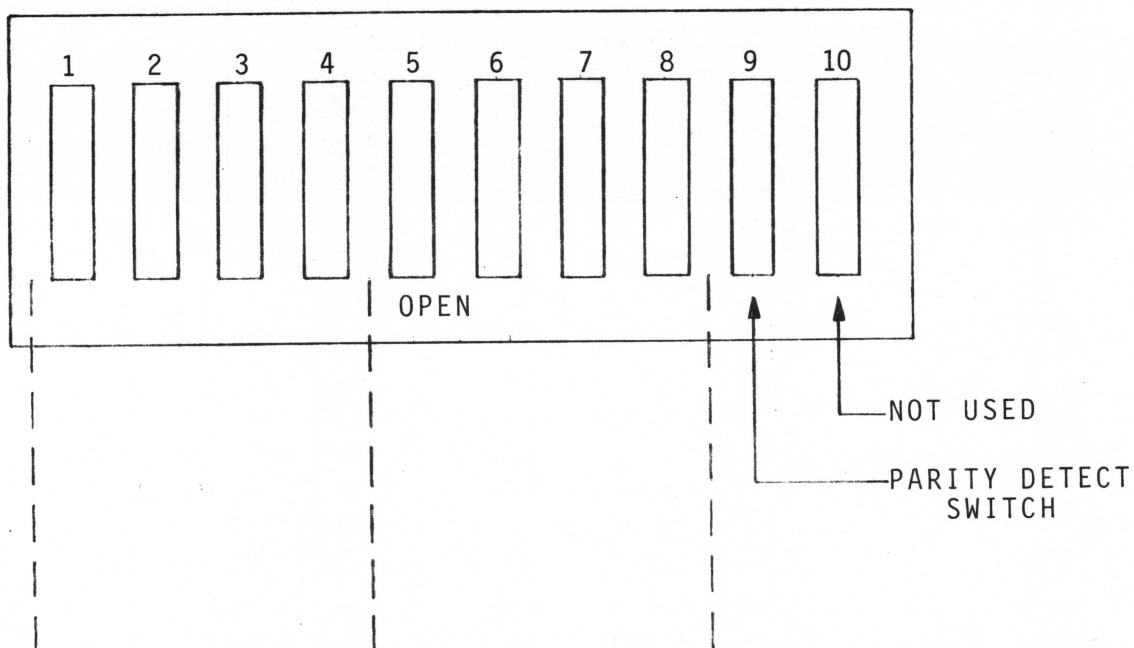
4.6 BOUNDARY CONTROL SWITCHES (S2-1 thru S2-8)

Adjusts the upper and lower operational limits of the Cache in 8K (word) increments. The boundaries will be factory set to allow operation over the entire 124K (word) memory range.

4.7 BOUNDARY ADJUSTMENT

The Boundary Control Switch is a switch assembly containing ten individual rocker switches. Each rocker switch is individually numbered and can be set in the OPEN or CLOSED position by pressing on the ends of the rocker. If the end of the rocker labeled OPEN is depressed, the switch is considered to be in the OPEN position. When the end of the rocker by the numbers is depressed, the switch is considered to be in the CLOSED position.

DETAIL OF SWITCH S2

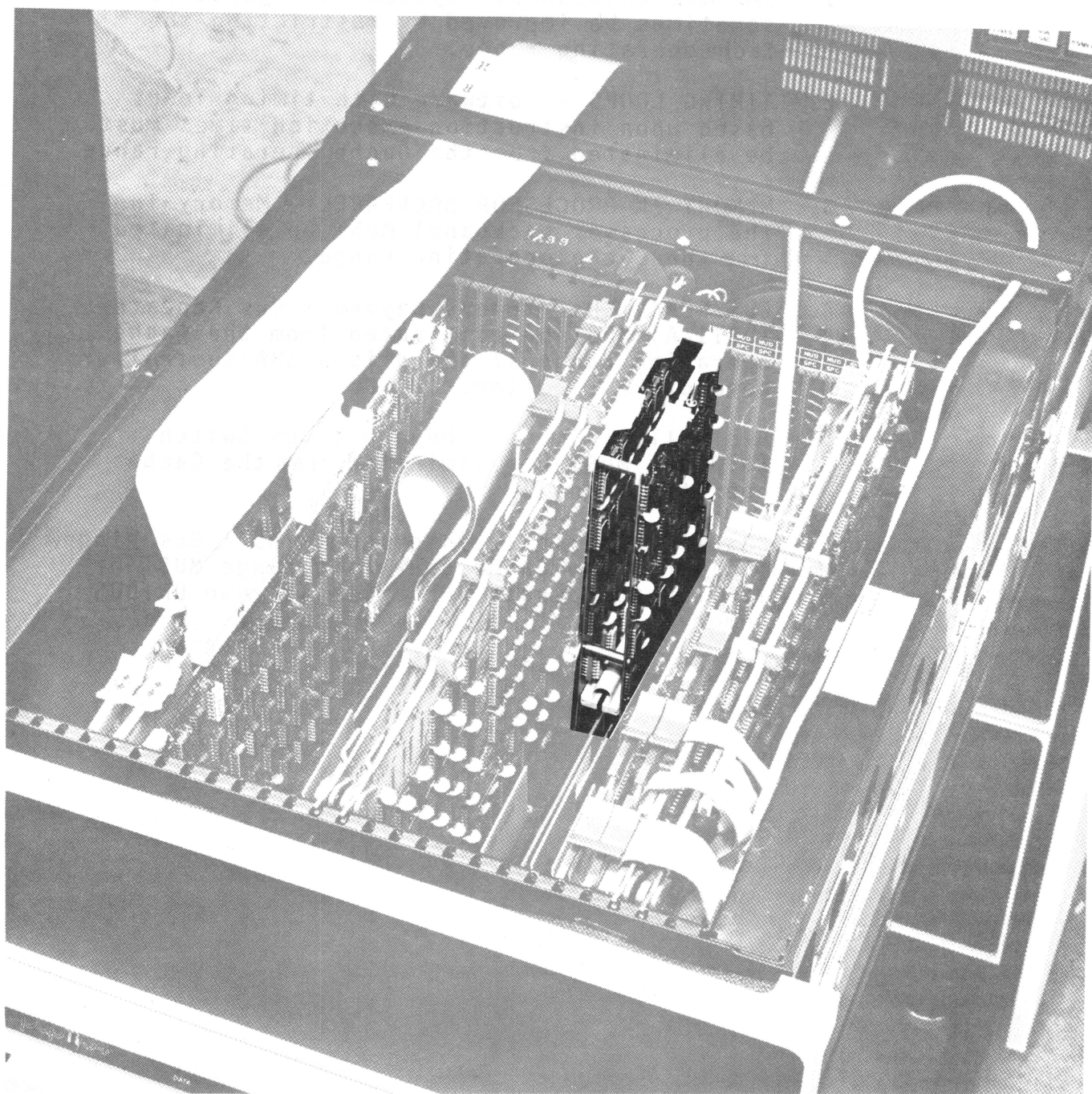


LOWER BOUNDARY	1	2	3	4	5	6	7	8	UPPER BOUNDARY
0K	C	C	C	C	C	C	C	C	8K
8K	0	C	C	C	0	C	C	C	16K
16K	C	0	C	C	C	0	C	C	24K
24K	0	0	C	C	0	0	C	C	32K
32K	C	C	0	C	C	C	0	C	40K
40K	0	C	0	C	0	C	0	C	48K
48K	C	0	0	C	C	0	0	C	56K
56K	0	0	0	C	0	0	0	C	64K
64K	C	C	C	0	C	C	C	0	72K
72K	0	C	C	0	0	C	C	0	80K
80K	C	0	C	0	C	0	C	0	88K
88K	0	0	C	0	0	0	C	0	96K
96K	C	C	0	0	C	C	0	0	104K
104K	0	C	0	0	0	C	0	0	112K
112K	C	0	0	0	C	0	0	0	120K
120K	0	0	0	0	0	0	0	0	124K

TABLE 4.1

4.8 REASONS FOR BOUNDARY ADJUSTMENTS

1. IMPROVE THROUGHPUT- System throughput can sometimes be improved by restricting the Cache operating range.
2. TIMING LOOPS - Software with timing loops based upon instruction execution times must be eliminated from the Cache operating range.
3. MEMORY IN PROCESSOR BACKPANEL - Memory in the processor backpanel MUST be eliminated from the Cache operating range.
4. BUS REPEATER - Memory beyond a Bus Repeater (DB11-A) MUST be eliminated from the Cache operating range if there is a DMA controller beyond the repeater.
5. BUS SWITCH - Memory beyond a Bus Switch (DT03-F) MUST be eliminated from the Cache operating range.
6. BUS WINDOW - If a system contains a Bus Window (DA11-F), the Cache operating range MUST be limited to operate ONLY with its own UNIBUS memory.



INSTALLED I

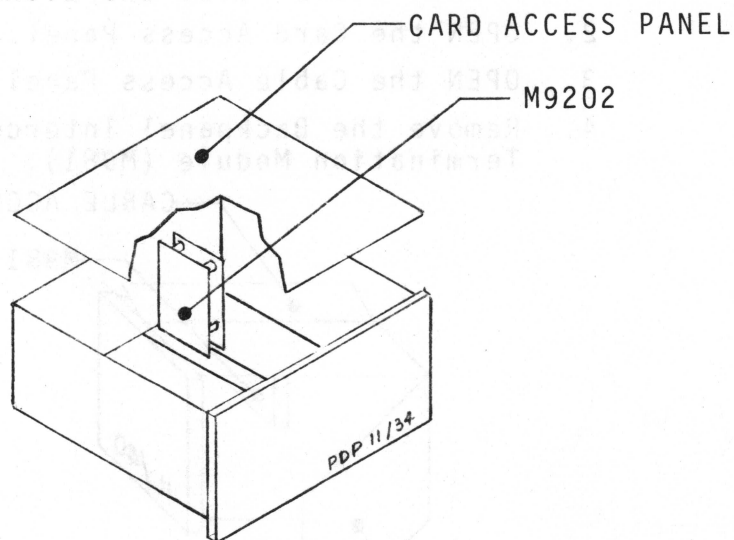
SECTION 5
CACHE/434 INSTALLATION PROCEDURE

5.1 PREPARE THE CACHE/434

1. Set the Boundary Switches
(Refer to Table 4.1)
2. Set the Parity Detect Switch to the RUN mode.(S2-9 OPEN)
3. Set the On Line Switch to the ON line position.

5.2 PREPARE THE SYSTEM

1. With power OFF, pull the Processor Cabinet OUT to its fully extended position.
2. REMOVE the Card Access Panel.



3. Remove the Backpanel Interconnection Module (M9202).

5.3 INSTALL THE CACHE/434

With the components toward the processor backpanel, plug the Cache into the M9202 location.

THE INSTALLATION IS NOW COMPLETE.

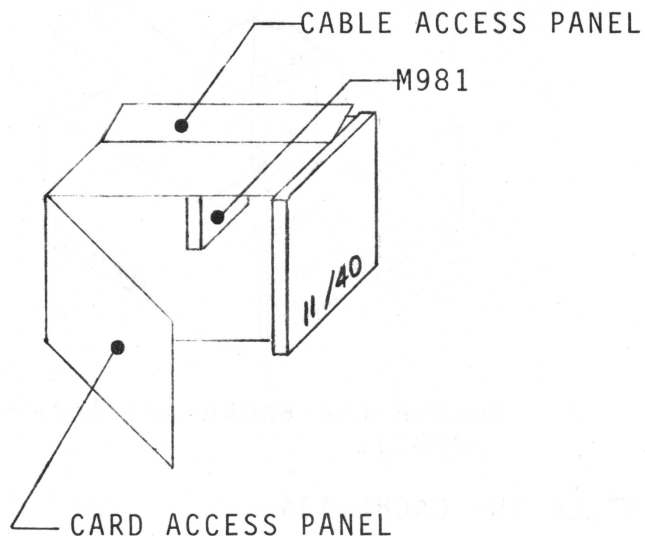
SECTION 6
CACHE/440 INSTALLATION PROCEDURE

6.1 PREPARE THE CACHE/440

1. Set the Boundary Switches.
(Refer to Table 4.1)
2. Set The Parity Detect Switch to the RUN mode.
(S2-9 OPEN)
3. Set the On Line Switch to the On Line position.

6.2 PREPARE THE SYSTEM

1. With power OFF, pull the Processor Cabinet OUT to its fully extended position.
2. OPEN the Card Access Panel.
3. OPEN the Cable Access Panel.
4. Remove the Backpanel Interconnection and Termination Module (M981).



6.3 INSTALL THE CACHE/440

With the components toward the front of the computer, plug the Cache into the M981 location.

THE INSTALLATION IS NOW COMPLETE.

SECTION 7

BENCHMARKS

7.1 BENCHMARKING MADE EASY

The Cache is equipped with an ON Line Switch to make benchmarking easy. Simply time any benchmark program in both positions. While ON LINE, the GREEN Response Indicator will provide a visual indication of the Cache activity. No need to worry about changing the switch while the computer is running, the Cache has been designed to handle that.

7.2 CALCULATING THE INCREASE

$$\text{INCREASE IN THROUGHPUT} = \frac{\text{Benchmark time with Cache OFF Line}}{\text{Benchmark time with Cache ON Line}}$$

EXAMPLE:

$$\text{Increase in throughput} = \frac{30 \text{ seconds}}{20 \text{ seconds}}$$

$$\text{Increase in throughput} = 1.66$$

or a

66% increase in throughput

DIFFERENCE BETWEEN CACHES

8.1 THE DIFFERENCE BETWEEN A CACHE/434 AND A CACHE/440

The difference is small.

The CACHE/434 does not contain Unibus termination resistors because it normally replaces a M9202 Unibus Jumper Module.

The CACHE/440 contains the Unibus termination resistors because it normally replaces a M981 Unibus Jumper and Termination Module.

If you purchased a CACHE/434 you will find a package containing 6 resistor termination modules within the shipping container. These have been provided to allow you to convert the CACHE/434 into a CACHE/440 if you should desire.

If you purchased a CACHE/440 the 6 resistor termination modules will already be installed in the sockets provided on the Cache Data Board.

8.2 CONVERTING A CACHE/434 TO A CACHE/440

1. Remove 4 screws. (See figure 1)
2. Separate the 2 boards by disconnecting the jumper cable between them.
3. In the same manner as shown in figure 2, install the 6 resistor modules in the sockets.
4. Connect the jumper cables between the 2 boards and replace the 4 screws.

The cache is now ready to be used in a PDP 11/40 computer.

8.3 CONVERTING A CACHE/440 TO A CACHE/434

1. Remove 4 screws. (See figure 1)
2. Separate the 2 boards by disconnecting the jumper cable between them.
3. Remove the 6 resistor modules shown in figure 2.

4. Connect the jumper cables between the 2 boards and replace the 4 screws.

The cache is now ready to be used in a PDP 11/34 computer.

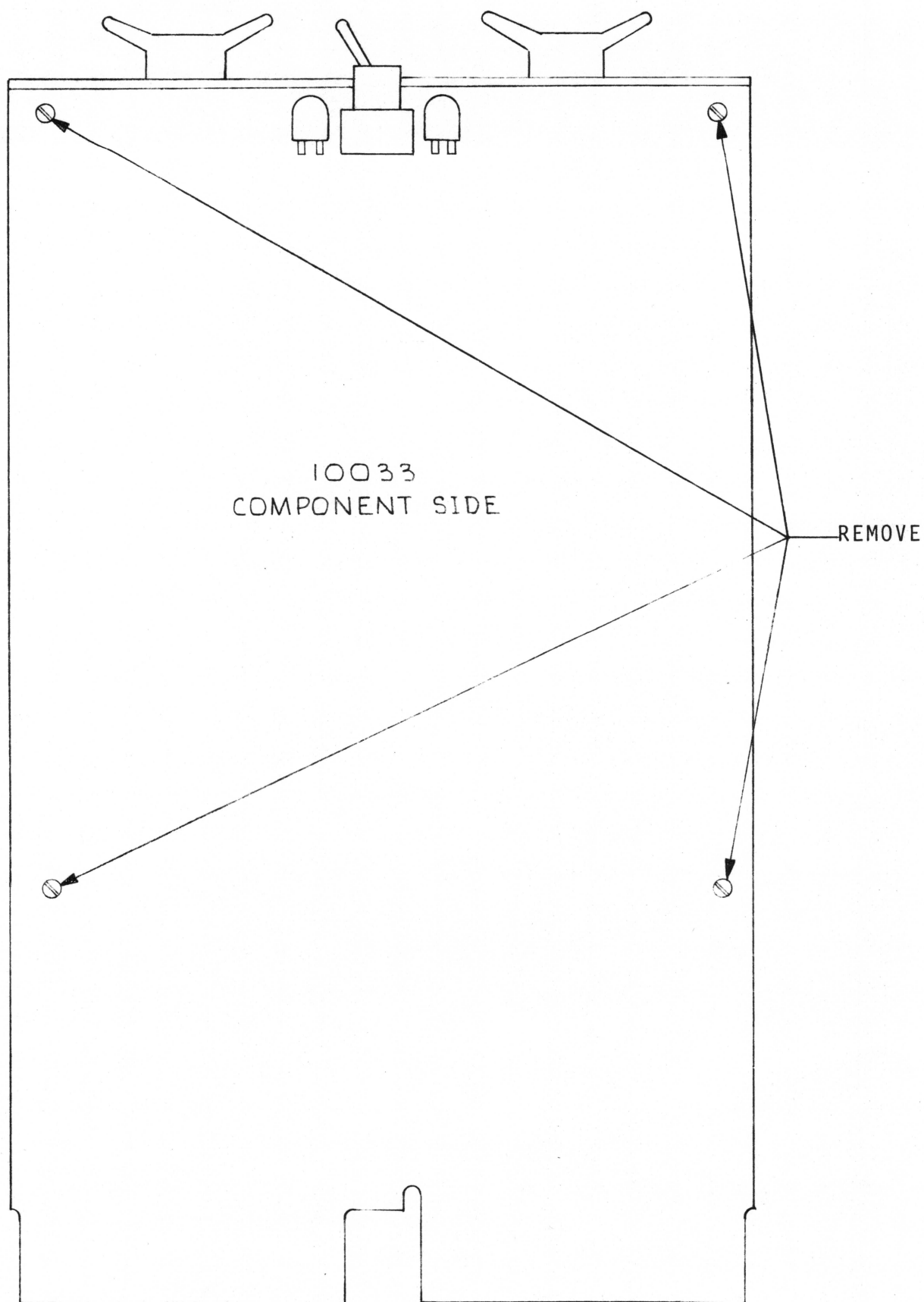


FIGURE 1
8-3

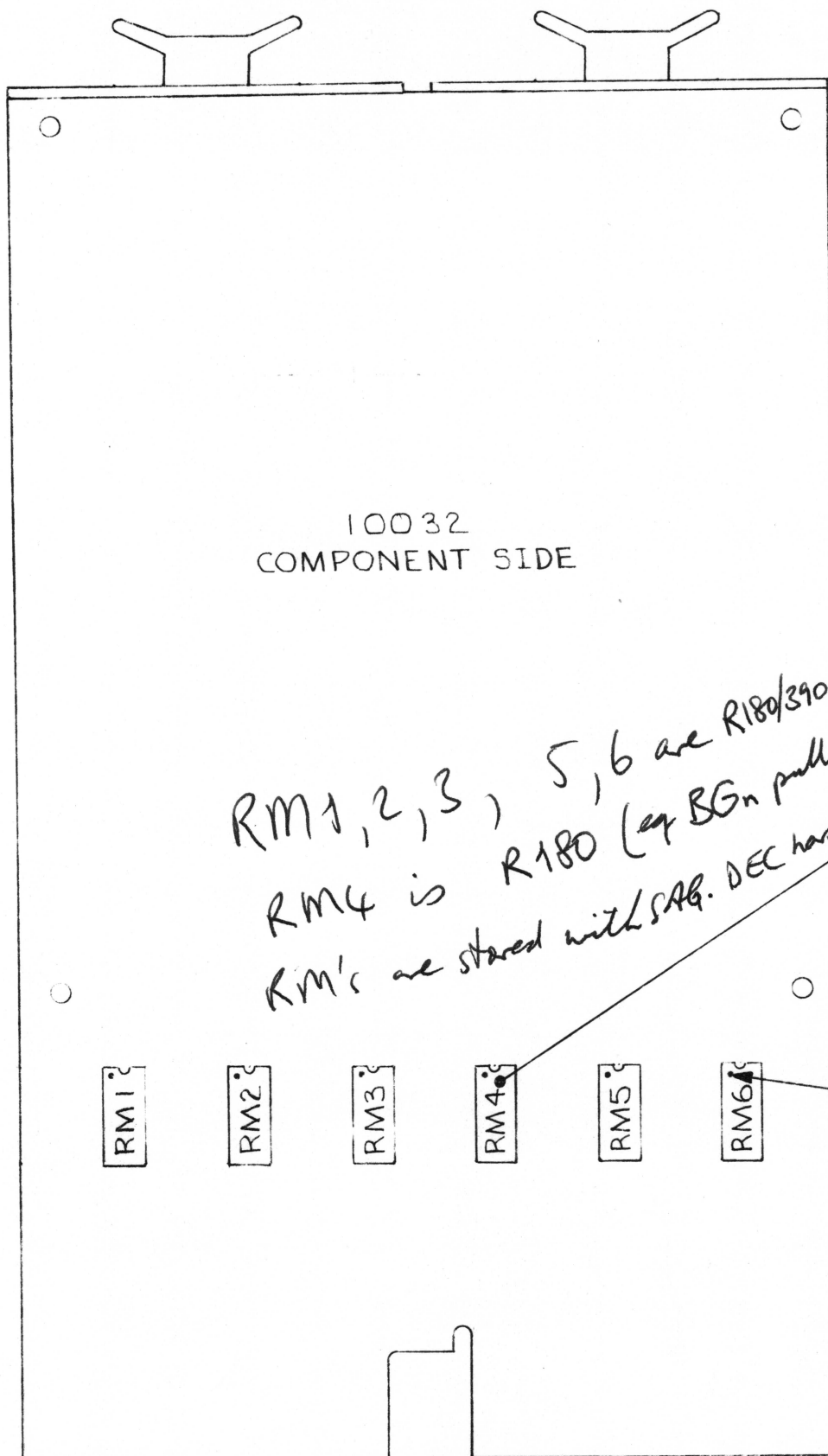


FIGURE 2



MAY, 1979

PRODUCT WARRANTY

WARRANTY & CLAIMS:

ABLE warrants its devices against faulty workmanship or the use of defective materials (except in those cases where materials are supplied by the BUYER) for a period of one (1) year from the date of shipment.

The liability of ABLE under this Warranty is limited to replacing, repairing, or issuing credit for any devices which are returned by BUYER during such period provided that:

- A) ABLE Contract Administration Department, Irvine, California is promptly notified in writing upon discovery of such defects by BUYER.
- B) PRIOR to return of any defective unit, BUYER obtains from ABLE, a "Return Authorization Number" and references said number on all documents relating to the return.
- C) Should the defective unit be returned to ABLE, transportation charges are prepaid by BUYER.
- D) ABLE's examination of such unit shall establish warrantability in that such defects have not been caused by misuse, neglect, improper installation, repair, alteration or accident. In no event shall ABLE be liable to BUYER for consequential, special, incidental or direct damages of any kind.

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