FOR ENGINEERS AND ENGINEERING MANAGERS - WORLDWIDE

MAY 1, 1986

# ELECTRON A HAYDEN PUBLICATION Silicon compilers

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Application-specific IC performs like PC board

What's hot at Electro/86

Programmable transistors bring a new touch to analog arrays

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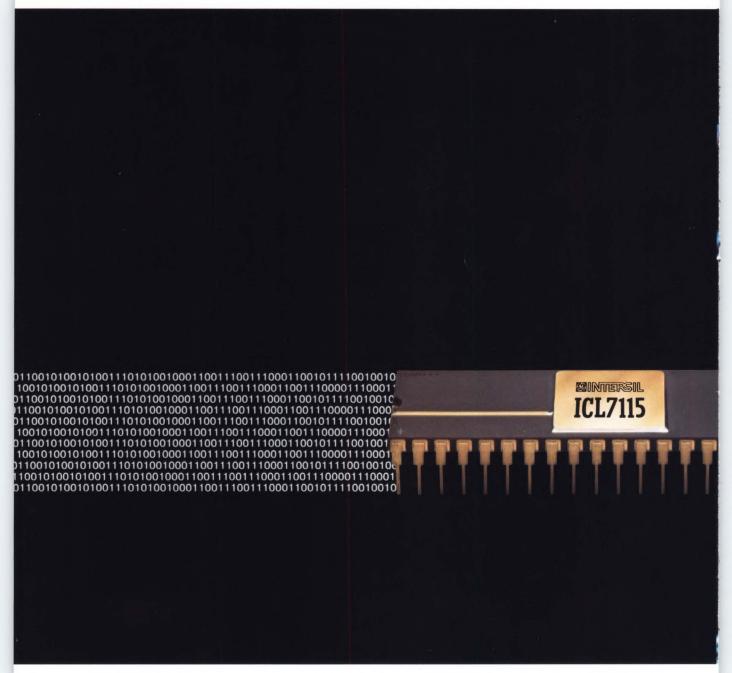
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CIRCLE 131

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#### BEHIND THE COVER



G. GIANNELLA

A few years back, Giovanni Giannella, manager of engineering services at Exar, made an astounding proposal. He told Surgit Nijjer, the company's marketing manager for linear products, that he could design a bipolar analog array so that any transistor could become an npn or a pnp device simply by changing the metallization. Nijjer reacted with disbelief, a feeling that intensified

when Giannella added that transistor density would double.

Eventually Giannella brought Nijjer and the rest of the Exar staff members over to his side. But while he set about his work, Nijjer spent several sleepless nights—happily tossing about thoughts of chips that could reach 130% silicon utilization. Clearly, transistor structures that could assume dual roles (npn or pnp) had tremendous appeal.

Giannella, for his part, seemed an unlikely candidate for designing the Beta analog array that scores as this issue's cover story (p. 171). "About 14 years ago," he recalls, "I got tired of IC design and switched over to manufacturing and marketing"; his primary responsibility now at Exar is test system development. However, he did begin to dabble again in IC design several years ago. In fact, in his spare time he conceived the Alpha array, predecessor of the Beta array.

One day, as work on the Alpha array was nearing completion, Giannella was sitting in bumper-to-bumper Silicon Valley traffic when an idea struck him. Though it was too late to implement in the Alpha array, the idea still seemed attractive. Why not combine the Alpha's npn transistor structure (similar to a structure used on many standard products but never on arrays) with a pnp structure that he had designed 12 years earlier and that he knew worked.

With a great deal of confidence—and moxie—he devised not one but three unique transistor structures: the Twinstor, the Twinbooster, and the Padstor.

Giannella had one more trick up his sleeve. Though the Beta array was to be Exar's largest ever, he convinced the company to lay it out and fabricate it without first building and characterizing the three internal structures. So much faith did Exar place in the Beta array that it has decided to patent the three transistor structures in virtually every Western country, investing about as much money in that campaign as it did in designing the array itself.

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81 Preamplifier IC advances fiber-optic receivers Priced under \$2, a low-noise 300-Mbaud device heralds low-cost fiber-optic systems and other interesting applications.

Wide output swings mark CMOS op amp For the first time, a quad CMOS op amp gives designers a mix of dc and dynamic specifications from chips running off a 5-V rail.

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Last year's 'wunderkind' struggles with reality. But once in its niche, silicon compilation will lead to much higher productivity.

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171 Cover: Array presents new ways to customize analog circuits without wasting silicon

Exploiting the unusual cell-like architecture of an analog array, designers can freely turn any transistor into an npn or pnp device.



1986 winner, Jesse H. Neal Editorial Achievement Award. Best in-depth analysis article series: 1985 Technology Forecast







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Working with three rather than two buses, a fast digital signal processor makes short work of real and complex data.

#### 201 EEPROM-based ASIC propels programmable logic to new levels of complexity

With a NOR structure and multiple logic levels, a reprogrammable ASIC replaces about 20 low-power TTL devices.

#### 213 Interface chip links floating-point coprocessors to host to form supermini look-alike

A memory-mapped interface and its companion coprocessors bring 5 MFLOPS to a host CPU.

#### 229 **68000-type** microprocessor packing peripheral subsystems smooths workstation design

Designers can build low-cost, high-performance CAE workstations with a chip that sports dual DMA channels and MMU counters.

#### 239 1-Mbit DRAM controller shuns complex timing and protocol to streamline high-speed systems

Engineers looking for new and better ways to drive and control dynamic memory arrays can turn to a fast controller.

#### Cover photograph by Herbert/Wagner Computer Images

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- 250 Op amp driven by  $\pm 0.8$ -V supplies
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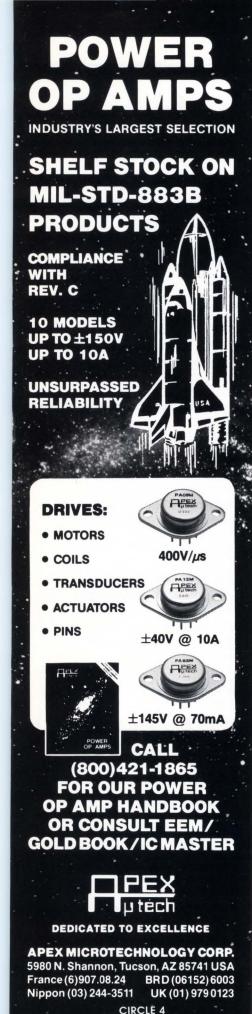
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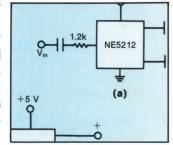
42 For about \$1300, the Commodore Amiga can make a cost-effective color workstation. Add-in boards further enhance the box. In one case a 68020 processor shares a board with a floating-point processor.

68000		6
512-kbyte RAM (expandable to 8 Mbytes)	RS-422 (800 kHz)	512- kbyte RAM

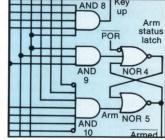
**51** On the agenda at the upupcoming Custom IC Conference: In a 20,000-gate chip, using a few thousand gates for self-testing more than pays for itself. Eliminating wiring channels leads to a chip with almost 100,000 gates. A layout program, Sparcs, produces digital and analog ICs independent of device technology.



**81** What's holding back fiber optics? The cost of receivers, for one. Now there's a preamplifier IC with wide dynamic range, broad bandwidth, low noise, and a superlow price of just \$2. A transimpedance-type amplifier, it also makes a good voltage-controlled amplifier or crystal oscillator.



**201** Here's a CMOS programmable logic device that contains 800 electrically reprogrammable gates. On a board it packs 1000 logic gates/in.<sup>2</sup>. And running with a 10-MHz clock, it draws less than 20 mA—about 50% to 90% less than other bipolar and CMOS PLDs.



249 A voltage-to-pulse-width converter can lend a hand in measuring voltages that may vary by as much as a million to one. Its dynamic range falls between 120 and 126 dB, and in a typical input voltage range, it generates pulses of about  $400 \mu s$ .





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Am29325

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CIRCLE 5

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CIRCLE 6

# WEEK WEEK WEEK

Announcing the Am29C827/28 high-performance CMOS Bus Buffers, the first members of AMD's hot new Am29C800 series-9 and 10-bit buffers, latches, registers and transceivers in CMOS. They're bipolar fast, CMOS cool.

Am29C827/28

#### Hot is cool.

Requiring only 80 microAmps of stand-by current, both parts have 8ns propagation delays for truly high-performance systems. With 24mA of drive, they can be used in place of or along with their Am29800 bipolar counterparts to match your drive and power requirements.

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If you're looking for bus interface chips that keep their cool under the pressure of high performance, look no further.

CIRCLE 7

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# WEEK

Introducing the Am29C01 4-Bit CMOS Microprocessor Slice. The latest CMOS part of AMD's 2900 family. Advanced Micro Devices created the 2900 phenomenon in the first place. So you can count on the Am29C01 being a product

of elegant engineering.
Because the Am29C01 is in CMOS, it uses a mere 25% of the power used by the bipolar version. But it doesn't ask you to give up anything in performance. Anything.

#### Am29C01

#### The arrival of the fittest.

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The Am29C01, Am29C10 and the Am29C101 are here now. Soon you'll be able to get the Am29C116/117 and the Am29C516/517. All so you can create the next generation of high performance, cooler boards.

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CIRCLE 8

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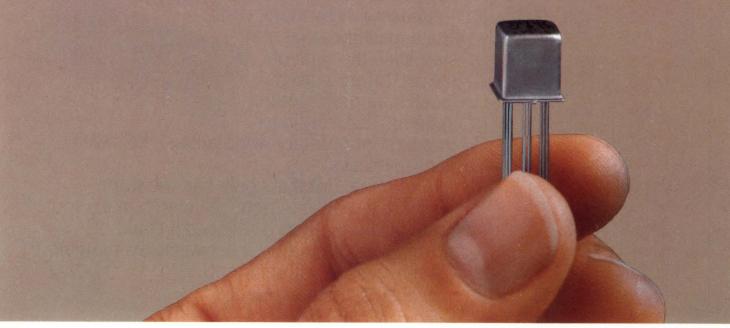
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#### **NEWSPULSE**

#### Japanese break into bit-slice macrocells

Close to a dozen Japanese semiconductor manufacturers plan to offer CMOS standard-cell libraries with macros that mimic the popular microprogrammable 2901 bit-slice family. Six of the companies—Toshiba, Sharp, Sanyo, Ricoh, NEC, and Mitsubishi—have already committed design resources to develop the macros by 1987, and several others are considering doing the same. Although the 2901 architecture is close to 10 years old, its flexibility and performance upgrades still find new design applications. A number of U.S. companies are also offering CMOS versions of the 2901 family, including its creator, Advanced Micro Devices Inc. (Sunnyvale, Calif.).

#### **MOSFET** packs 2 million cells/in.<sup>2</sup>

The demise of bipolar power transistors may be at hand. RCA Corp.'s Solid State Division (Somerville, N.J.) is about to introduce a MOSFET carrying 2 million cells/in.<sup>2</sup>—twice the maximum density of typical MOS transistors. What's more, the company plans to price the 50-V transistor at 3¢ per ampere, about the same tag as the popular 2N3055 bipolar transistor. The new MOSFET is 100 times faster than the bipolar device and claims lower resistive losses: The on-resistance is about  $1.5 \,\mathrm{m}\Omega/\mathrm{cm}^2$ . In addition, it has reached fall times of 30 ns, one-third that of bipolar chips with the same on-resistance. Thus the MOSFET should excel in power-switching applications in the megahertz range.

#### IC will tie Multibus II to popular µPs

System designers around the world are anxiously awaiting the release soon of a Multibus II interface chip that will link boards to a wide variety of microprocessors. The message-passing coprocessor (MPC), developed by Intel Corp.'s Systems Group (Hillsboro, Ore.), will interface not only with the company's 80186, 80286, and 80386 chips, but also with the 68000 family from Motorola and the 32000 line from National Semiconductor. To avoid contention, interrupts and data are transmitted across the 32-bit bus in packets. VLSI Technology Inc.'s Application-Specific Logic Products Division (Phoenix) has already agreed to manufacture and offer the interface chip.

Bull Systems (Les Claye, France) is just one of the system suppliers now turning to Multibus II. It is counting on the coprocessor to give its 68010- and 68020-based workstations an upward expansion path. High-performance-system designers will be particularly interested in the extra board space available with Multibus II—the card is 60 mm deeper than the 160-mm-deep VME card. Designers can fill the extra space with memory extensions and controllers.

#### **Icons** shape new software era

Microcomputer software pioneer Bill Gates forecasts a new era of man-machine interfacing, sparked by the icons that Apple Computer Inc. (Cupertino, Calif.) created for the Macintosh. Indeed, specifications for the symbols will soon emerge, he predicts. In a recent seminar for top business users, the chairman of Microsoft Inc. (Bellevue, Wash.) and the creator of IBM PC and compatible operating systems, noted that graphics is becoming standard equipment in microcomputer systems. From a processing angle, Gates says that software now

#### NEWSPULSE

at hand takes advantage of the faster throughput and larger main memories of desktop machines based on the 80286, but the further development of software for 8088 machines is unlikely, he adds.

#### 32 ports on 80286 PC

Looking for a personal computer-network host that sports more ports than the IBM PC AT or its clones? ITT's Information Systems Division (San Jose, Calif.) equips its new 80286-based personal computer with up to 32 intelligent I/O ports for a maximum of 16 concurrent users. The XTRA XL is more than just a soupedup PC AT look-alike. ITT redesigned the motherboard using programmable logic arrays and a faster, 8-MHz CPU without memory wait states. As a result it can cram up to four 80186-based, eight channel I/O boards and an optional 80287 math coprocessor into the computer's console. With a unit base price of \$5300, it establishes a new price-performance benchmark for PC network hosts at around \$12,300 for 8-port host.

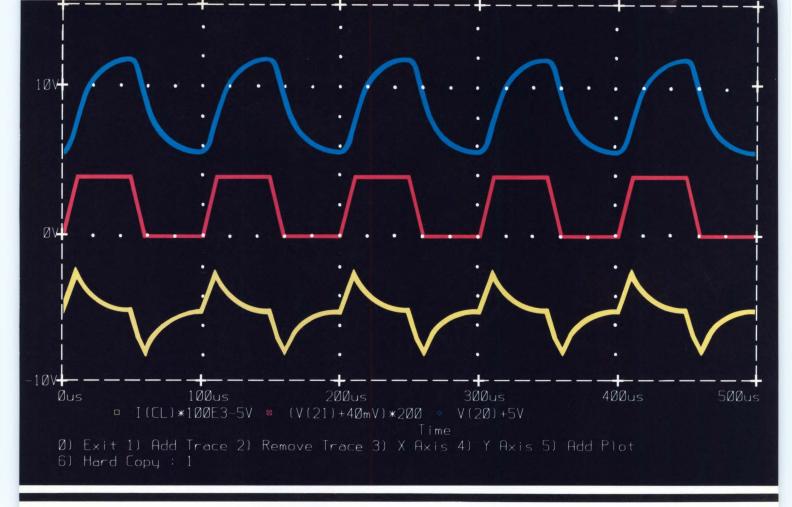
As a file server, the XL offers up to two 72-Mbyte hard-disc drives with an access time of just 28 ms. An ITT version of MS-DOS 3.1 handles file-server tasks, and a proprietary version of the Xenix operating system takes over in the networking mode.

#### ECL chip combines logic, memory circuits

Using tight-feature geometries and a self-aligned structure, an ECL chip integrates more memory and circuits than previously possible on a commercial IC. Fujitsu Ltd. (Kawasaki, Japan) squeezed 4608 bits (512 by 9) of static RAM onto the device along with circuits like a parity generator-checker and a 9-bit highspeed comparator. The MB70802 performs address or parity matching in a maximum of 20 ns, and either data matching in 15 ns or chip-select access in 10 ns. The high speed offers engineers the option of designing fast cache subsystems and rapid translation look-aside buffers. The ECL chip consumes about 1.35 W and interfaces with 10K family logic levels. Fujitsu plans to sample the chip this summer.

#### Router handles odd blocks and analog

A block placement and routing program will handle not just regular digital cells but odd-sized and analog blocks too. The package, now under development at SGS Microelettronic: SpA (Agrate Brianza, Italy), will work with the outlines and pinouts provided for such predefined blocks as standard cells or special macrocells. Since the router is insensitive to the elements inside the blocks, it can place and route both analog and digital cell blocks, even mixed analog-digital cells like data converters. The software is expected to perform 100% placement and routing and to generate data on interconnection path lengths and capacitive loading for subsequent use by a simulator. The program will run on a VAX and be used with the company's Zodiac family of predefined cells.



#### Accuracy. Speed. Reliability. Support. PSpice.

Since its introduction over two years ago, MicroSim's PSpice has become the most popular commercial SPICE program in the world.

With over 20 years of combined real world experience in CAD, MicroSim offers an analog circuit simulator based on Berkeley version 2G.6 that has set the standard for IBM PC based machines.

PSpice allows you to simulate up to 140 transistor circuits (and over 10,000 nodes). With PSpice you will be able to design in minutes complicated circuits that used to take hours, without doing costly breadboarding, all with the convenience of using your own PC.

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(The picture above was generated using Probe.)

If you are interested in doing your circuit simulations in a timely manner and at a fraction of a mainframe's cost, please give us a call today!

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There's really nothing else to compare it to. Unless you count the 10ns series we'll be introducing soon.

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Or write Monolithic Memories, 2151 Mission College Blvd., Santa Clara, CA 95054.

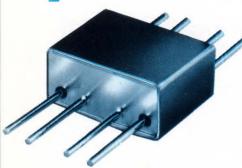
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CIRCLE 11



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CIRCLE 12

C96-3 REV. ORIG.

#### **Engineers vs programmers:** Will myth become truth?



There is a common myth in the design community that engineers are conservative and rigid while programmers are more flexible and open-minded. But generally, it is the other way around. Engineers are the ones who must be flexible, as they are continually forced to keep pace with hardware technology. Take logic designers. Every few

years they must adapt to new logic families, new bus and microprocessor systems, and new packaging constraints coming down the pike. Programmers, on the other hand, usually stick with one or two programming languages and operating systems, and many assemblylanguage programmers become bound to one microprocessor family. In fact, it is not uncommon for programmers to swear by a single language—say, Fortran -throughout their entire career. They become tied to it, even acolytes of it.

I've spent time in both camps: seven years as a system software developer following six years as a logic designer. I never heard the same kind of heated, almost religious arguments among engineers that I did among programmers over languages. Small wonder, since engineers must always be ready for the next circuit family.

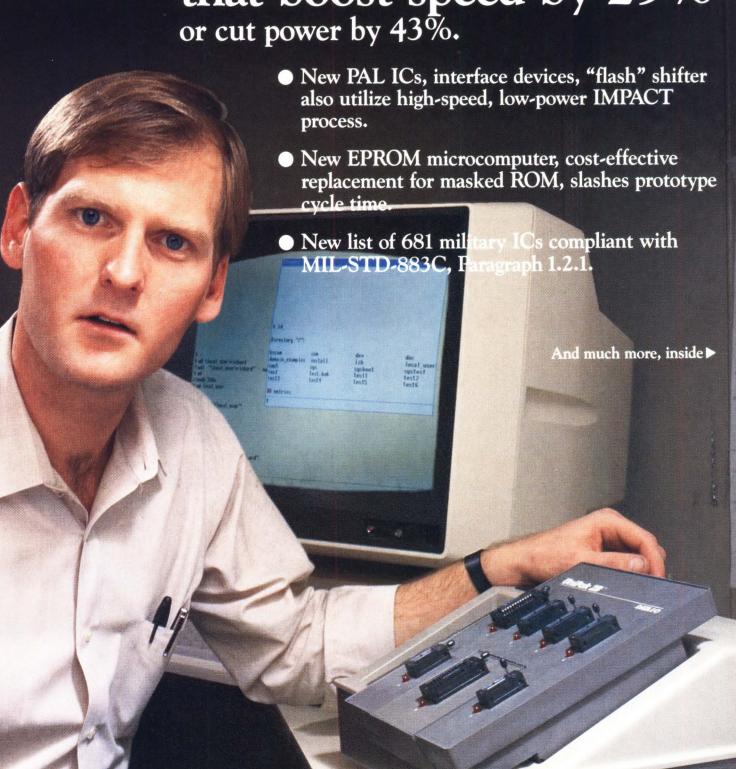
Today the balance is shifting. Programmers are beginning to loosen up; they are starting to experiment with several languages and use different ones where needed. Concurrently, engineers are becoming more adept at programming

The bottom line is this: Engineers who cling too closely to one design tool or language risk becoming like the rigid programmers of yesterday. If we're not careful, the myth may become truth.

Ray Weiss

#### "WHAT'S NEW FROM TEXAS INSTRUMENTS?"

# IMPACT PROMs that boost speed by 29% or cut power by 43%.



# IMPACT PROMs deliver 25-ns speed at industry-standard power.

New Series 3 IMPACT™ PROMs from Texas Instruments make 16K-memory performance upgrades quick and easy. If speed is your most critical parameter in a high-complexity PROM, you can achieve it now without paying a power penalty. Just design in TI's new 25-ns, 175-mA IMPACT PROMs: The TBP38S165-25 (2K×8) or the TBP34S162-25 (4K×4).

Or use the world's fastest 16K registered PROMs. TI's TBP34R165-18 ( $2K \times 8$ ), with a minimum address-to-clock setup time ( $t_{su}$ ) of only 18 ns, is nearly 2½ times faster than the closest competitor. And the TBP34R162-30 ( $t_{su} = 30$  ns) is the only  $4K \times 4$  registered PROM on the market.

#### Standard speed at 43% less power

You can also cut power without sacrificing speed, using Tl's new TBP38L165-35 IMPACT PROM. It is pin-for-pin compatible with existing 2K × 8 PROMs and operates at the same 35-ns speed, but instead of 175 mA, it draws *only 100 mA*. Tl's broad family of Series 3 IMPACT PROMs also includes 256-bit, 1K and 2K devices.

#### Reliability built in

IMPACT PROMs are designed by TI for exceptional reliability. Current densities, metal spacing, and contact sizes are all conservatively designed. Electrostatic-discharge tolerance up to 4,000 V

is designed in. During programming, TI-developed titanium-tungsten fuse links insulate themselves with titanium-oxide caps. Electromigration is eliminated by copper-doped aluminum in the first-level interconnection. And you can program any of TI's new Series 3 PROMs on widely available commercial equipment, using TI's standard Series 3 programming algorithm.

#### Shift 32 positions in less than 29 nanoseconds.

Now Tl's 2-µm IMPACT technology also brings you high-speed "flash-shift" operations — with the new 74AS838 32-bit barrel shifter. Shifting as many as 32 positions in a single 29-ns instruction cycle, it can dramatically increase throughput in such applications as graphics systems, wide-word CPUs, and array processors. At an energy cost of less than 1.5 W, you get higher speed with lower power, in a single 84-pin ceramic pin-grid-array package.

You can program the 74AS8838 for logical, circular, or arithmetic shifts. Its two 3-state, 16-bit outputs give it the versatility to be configured as a 32-bit-in, 32-bit-out barrel shifter, as a 16-bit funnel shifter, or as a 16-bit shifting transceiver. And it can drive buses directly with 24-mA low-level output — with no additional circuitry.

The 74AS8838 barrel shifter, first

device in TI's 74AS88XX 32-bit processor chip set, is available today through your local authorized Texas Instruments distributor.

### MPACT technology doubles speed of new PAL ICs.

Four new exclusive-OR programmablearray logic (PAL®) ICs from TI feature the highest speed available today. Their 20-ns propagation delay at 180 mA makes them twice as fast as any comparable devices.

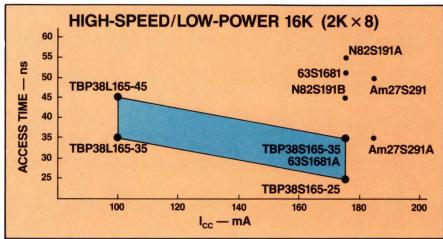
These devices — TIBPAL20L10-20, TIBPAL20X4-20, TIBPAL20X4-20, TIBPAL20X8-20, and TIBPAL20X10-20 — are designed primarily for counter-intensive applications. The exclusive-OR feature suits them ideally to digital voice applications and video-screen information correction. They can also be useful in memory addressing and mapping.

# Programmable logic sequencer is 250% faster because of IMPACT processing.

Still another new product in TI's growing line of high-speed programmable logic devices is the TIB82S105B. At 50 MHz, it is 2½ times as fast as functionally equivalent 16 × 48 × 4 field-programmable logic sequencers — at the same 180-mA power. Unlike them, however, it maintains that speed even when using many product terms.

Because of its improved clocking scheme, the IMPACT TIB82S105B is not a direct replacement for the TI or Signetics N82S105A. But it is ideal for those new high-speed state machines designed to control peripheral I/O, dynamic memory systems, and video blanking systems.

For more detailed information about any of TI's growing line of highspeed, low-power IMPACT products, just check the appropriate box on the attached reply card and return it to TI.



**Bracketing the speed/power spectrum,** TI's IMPACT PROMs cut power requirements from 180 to 100 mA for "standard" 35- to 45-ns access time. Or at 180 mA, they can give you 25-ns speed.

# High-density IMPACT circuits speed logic, memory access.

TI's unique Implanted Advanced Composed Technology (IMPACT) capitalizes on the advantages of ion implantation, oxide isolation, and composed-masking techniques to increase the speed and density of bipolar ICs.

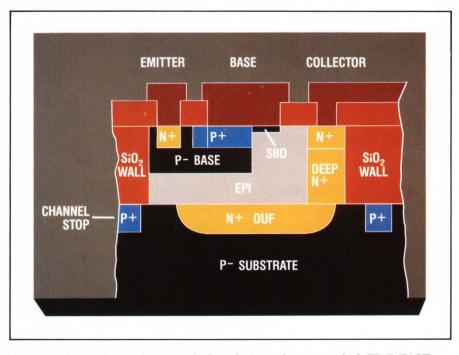
This innovative technology dramatically reduces the size and the sidewall capacitance of circuit elements (*see diagram*). As a result, speed/power ratios are significantly improved: In PROMs that cut power consumption by 43%, or more than double the speed (*see story opposite*). In PAL ICs that reduce propagation delay by as much as 40% — to only 15 ns at 180 mA.

With the high speed and low power that TI's IMPACT process makes feasible, its potential for large-scale integration will reduce package counts in many high-complexity circuits.

Composed masking yields high density

In composed masking, critical components are defined on the chip with a minimum number of masks. Thus they can be more tightly defined and more densely spaced than by conventional

masking.



A major reduction in capacitance results from the 2-µm feature size which TI's IMPACT processing makes possible. Silicon dioxide is the isolation material. Switching speed is further enhanced by utilizing this silicon dioxide for emitter and base sidewalls.

The IMPACT process also makes it possible to insulate critical base and emitter components

with oxide walls. This insulation reduces sidewall capacitance, which, at the 2-µm dimensions of IMPACT features, can represent as much as half the overall capacitance. Small size and oxide walling together contribute significantly to

the increase in switching speed.

DRAM technology spurs IMPACT growth

The IMPACT process is not a direct descendant of DRAM technology. Nevertheless, TI's commitment to DRAM production has provided IMPACT technology with vital processes.

It was the DRAM effort, for example, that drove photolithography to its present advanced state and contributed key dry-etching processes. Ion implanters designed to produce CMOS DRAM ICs enhance the quality — and the economy — of TI's bipolar IMPACT ICs. And this vital "crossfertilization" from VLSI memory is one

reason Texas Instruments — almost alone among U.S. semiconductor manufacturers — is committed to the development and manufacture of DRAM devices.

■ More chips per slice help cut costs. The 150-mm wafers now used on TI's advanced MOS 256K DRAM wafer-fabrication line have 125% more area than the 100-mm slices formerly used.

### your competitive edge.

6

# Keeping you competitive: ASICs and TI.

If you're looking for increased systemlevel integration and performance, shorter design-cycle time, and reduced VLSI development costs, take a hard look at application-specific integrated circuits (ASICs). And a long look at TI.

#### Broad choice lets you pick the right implementation

Texas Instruments supports an extensive library of  $3\mu$ m CMOS standard cells — more than 200 of the standard SN54/74 TTL functions you have designed with for years — including MSI, analog, and procedural LSI functions like RAM, ROM, PLA, and ALU. In addition, high-drive cells (up to 48 mA) are true TTL replacements.

From TI's new family of advanced standard cells you'll be able to choose among more than 280 functions and achieve increased system integration and performance.

Or for the performance you need, and quick turnaround to get your product to market fast, there's TI's DLM TAC-H and TAC-VH silicon-gate CMOS gate-array family. These devices, fully alternate-sourced, offer complexities from 440 to 8,000 gates.

Extensive design support

Whatever level of help you need, you get it from TI. In your design cycle as well as in meeting your prototype and production requirements *on time*. TI's proven expertise and worldwide manufacturing facilities are your assurance of dedicated support and products in the volume you require. And you have a wide range of package options: DIPs, SOs, PLCCs, pin-grid arrays — from 8 to 179 pins.

Design your own way

You can reduce your costs and speed your ASIC design with TI because you don't need special proprietary software or design tools. And you can do it at a TI regional design center or at your own work station. Because TI's cell libraries are supported by most work stations, including Daisy LOGICIAN®, MEGALOGICIAN®, and

GATEMASTER®; Mentor IDEA 1000®; Valid SCALDsystem®; and P-CAD® and FutureNet® in IBM PC® environments.

TI's worldwide network of 13 training and design centers, staffed with experienced ASIC design engineers, can provide access to work stations, as well as mainframe capability. And you can learn ASIC design in one of TI's unique hands-on workshops. Using TI's semicustom libraries with a real-world standard-cell example, you'll learn every phase of design from schematic capture through test-pattern generation and simulation.

Select TI distributors can also give you local access to Tl's leading-edge ASIC options, with dedicated facilities, tools, and trained engineers.

To find out more about what TI ASICs can mean to you, check the appropriate box on the return card.

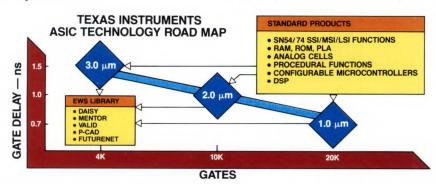
8

## And now, a new, easy-to-use EPROM microcomputer.

TI's new TMS7742 EPROM microcomputer can cut to zero your lead time for development, prototyping, field tests, and product qualification. And it bridges the gap to ROM-based volume production. For low-volume applications, it can be a cost-effective alternative to mask-programmed ROM. Its 4K bytes of on-chip EPROM are identical to TI's TMS2732A - transferred into the chip area vacated by masked ROM. So if you can program the TMS2732A you can program the TMS7742. This new microcomputer provides EPROM capability for the TMS7020, the TMS7040, and the new TMS7042 ROM microcomputer.

Also new to TI's TMS7000 family is the ROM-less TMS7002 microprocessor. Both the TMS7002 and the TMS7042 feature 256 bytes of RAM, a serial port for USART and serial I/O functions, 32 I/O lines, and three timers. And with their 60% performance increase over earlier TMS7000 ICs, they can improve system performance in such applications as disk and tape drives, printers, and industrial and

motor controls.



Advancing technology in ASICs need not demand new rules and tools. Your investment in hardware and training is protected when you move up with Texas Instruments to faster, more complex ASIC functions.

7

ew series of inputlatched and registered PAL ICs lowers parts counts.

Eight new 30 MHz PAL devices from TI are the first input-latched (TIBPALT19XX) and input-registered (TIBPALR19XX) PAL ICs in the marketplace. Functionally similar to TI's TIBPAL20XX series, they include either 11 D-type transparent latches or 11 D-type input registers on chip. This added circuitry allows you to synchronize inputs without external registers or latches. These devices can reduce your parts counts and simplify your design task in a wide range of applications such as random logic, businterface logic, and input synchronization to custom controllers.

### 8 new ways TI can help sharpen

1

# A new alternative for memory-systems design: TI SIP DRAM modules.

Memory-intensive packaging for the future is available today — in Tl's highly reliable modules in single-in-line packages (SIPs). With them you can have the many advantages of surface-mount technology (SMT) — while using

through-hole-mounted or socketable packages. Thus without changing your manufacturing technology, you can increase memory density by a factor of up to 3.5 over

dual-in-line packages (DIPs). And you can simplify board layout while facilitating replacement and future upgrades.

Each SIP module uses DRAM chips in plastic leaded chip carriers (PLCCs),

surface-mounted along with decoupling capacitors on an epoxy substrate. Since all connection points are on one edge of the substrate, the module "stands on end" to make the most of your board area.

TI's full line of SIP memory modules — from 64K × 4 to 256K × 9 and 1M × 1 — includes standard DRAMs and Multiport Video RAMs in various organizations. And all are available through your authorized TI distributor.

For more information, just check the appropriate box on the reply card.



Memory can be 3.5 times denser using fully-qualified, production-proven RAMs configured in SIP modules. TI SIPs combine the density of surface-mount technology with economies of through-hole insertion.

2

#### Interface performance enhanced by TI.

Also new from Texas Instruments is an improved direct replacement for the UCN5812 vacuum fluorescent display driver. TI's TL5812 is 11% faster and

draws 60% less current. With an output voltage swing of 70 V and an output source-current capability of 40 mA.

Only TI's patented BIDFET technology — combining bipolar, double-diffused MOS (DMOS) and N-channel and P-channel CMOS transistors on the same chip — makes these improvements possible. And at a competitive price.

3

#### F ast line drivers and bus transceivers from TI.

In the new SN75ALS192/194 quadruple EIA Standard RS-422-A differential line drivers, TI's exclusive ALS 1.5 process technology (oxide-isolated Advanced Low-power Schottky) yields the best speed/power ratio in the industry: At approximately half the power consumption, these devices are 30% faster than the competition.

A new family of differential bus transceivers, SN75176B, 177B, 178B, and 179B, are faster than earlier versions. Designed for bidirectional communication on multipoint transmission lines in noisy environments, they meet

EIA Standards RS-422-A and RS-485. Typical propagation time is only 22 ns.

Want to know more about these new interface products from TI? Just check the appropriate box on the reply card.

INDUSTRY'S FIRST ADVANCED LINE DRIVERS
USE ALS TECHNOLOGY

MC3487 \*\*

AM26LS31 \*\*

SPEED — ns (t<sub>PHL</sub>, t<sub>PLH</sub>)

Advanced TI line drivers are 30% faster, typically draw only half the power of the devices they are designed to replace.

4

#### F ast, economical new 8-bit SAR A/D converters.

Now Texas Instruments offers 8-bit SAR (serial-approximation resolution) A/D converters that are as economical as any you can use. And because they use LinCMOS™ polysilicon-gate-process technology, they are unsurpassed in speed. TI's TLC549 analog-to-digital converter performs 40,000 conversion cycles per second (cps), while the new TLC548 pushes speed to an unprecedented 45,500 cps. At any supply voltage between 3 and 6 V. And typical power consumption is only 6 mW.

Performance of the serial-approximation algorithm is not only fast. It's accurate: Conversions are performed with the guaranteed low error rate of  $\pm 0.5$  LSB (least significant bit) across the temperature range from  $-55^{\circ}$  to  $125^{\circ}$ C.

5

### 681 military TI devices comply with 1.2.1.

Now designers of military electronics have the broadest choice ever of devices that comply with the requirements of MIL-STD-883C, Paragraph 1.2.1. The vast majority of TI's military ICs — 681 different devices — now qualify:

Product T	ype	Number
ALS/AS		83
TTL		131
LS/S		238
<b>HCMOS</b>		80
PAL ICs		16
Linear		113
Memory/LSI		19
MOS DSP		1
	TOTAL:	681

For more detailed information on specific TI military devices, just check the appropriate box on the reply card.

# Texas Instruments quality recognized in Tokyo and Detroit.

Outstanding Texas Instruments quality-assurance programs were lauded during 1985 both at home and abroad. In June, Ford Motor Company granted TI linear products the coveted Q1 Award. And in November, TI's wholly owned Japanese semiconductor operation received the prestigious Deming Prize. Both awards recognize exceptional levels of quality and reliability, achieved through aggressive defect-prevention programs.



First Ford Q1 Award to a semiconductor supplier

Ford Motor Company's Q1 Award to Texas Instruments Linear is the first ever to a major U.S. semiconductor manufacturer.

Qualification is based on a demonstrated defect-prevention program,

along with Ford's review of warranty returns, specifically keying part numbers to failures. Thus it recognizes both initial product quality and continuing reliability.

Both quality and reliability are attributes that TI Linear has pursued aggressively through its "monitor program," begun in 1979. The goal of the program has been to achieve levels of quality and reliability equal to or better than the best worldwide competition. And the Ford Q1 Award is one visible token of its success.

First U.S. winner of Japan's Deming Prize

At ceremonies on November 11 in Tokyo, the Japanese Union of Scientists and Engineers awarded the prestigious Deming Prize for total quality control to TI's bipolar semiconductor operation in Japan.

The prize, never before won by a wholly U.S.-owned company, recognizes outstanding quality-control achievement in all aspects of business including marketing, engineering, manufacturing, and support. It is named for W. Edwards Deming, the American statistician whose work in defining and measuring quality control in Japan after World War II became the basis for the legendary Japanese commitment to quality. In 35 years, the Deming Prize has been awarded to only 48 individuals and 111 institutions. Texas Instruments Japan, Ltd. was one of only eight companies so honored



As is the case with the Ford Q1 Award, sensitivity to customers' requirements is a key factor in selecting winners of the Deming Prize. TI's successful commitment to quality and reliability in support of all our customers' needs has been demonstrated twice again. And TI is justifiably proud of this achievement.

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#### More news upcoming from TI in the next issue:

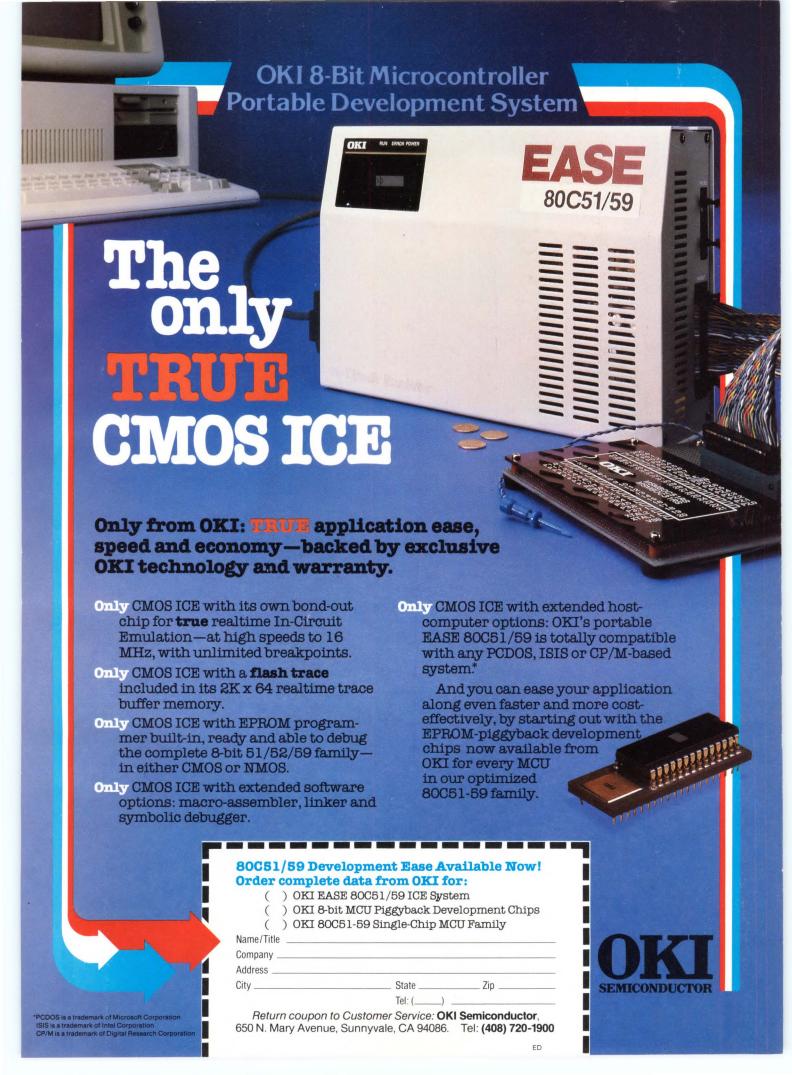
- A new CMOS version of TI's trendsetting TMS320 Digital Signal Processor.
- More new additions to TI's growing family of IMPACT PAL ICs.
- New CMOS standard cells and gate arrays that augment TI's leadership in Application-specific Integrated Circuits (ASICs).
- And more ...

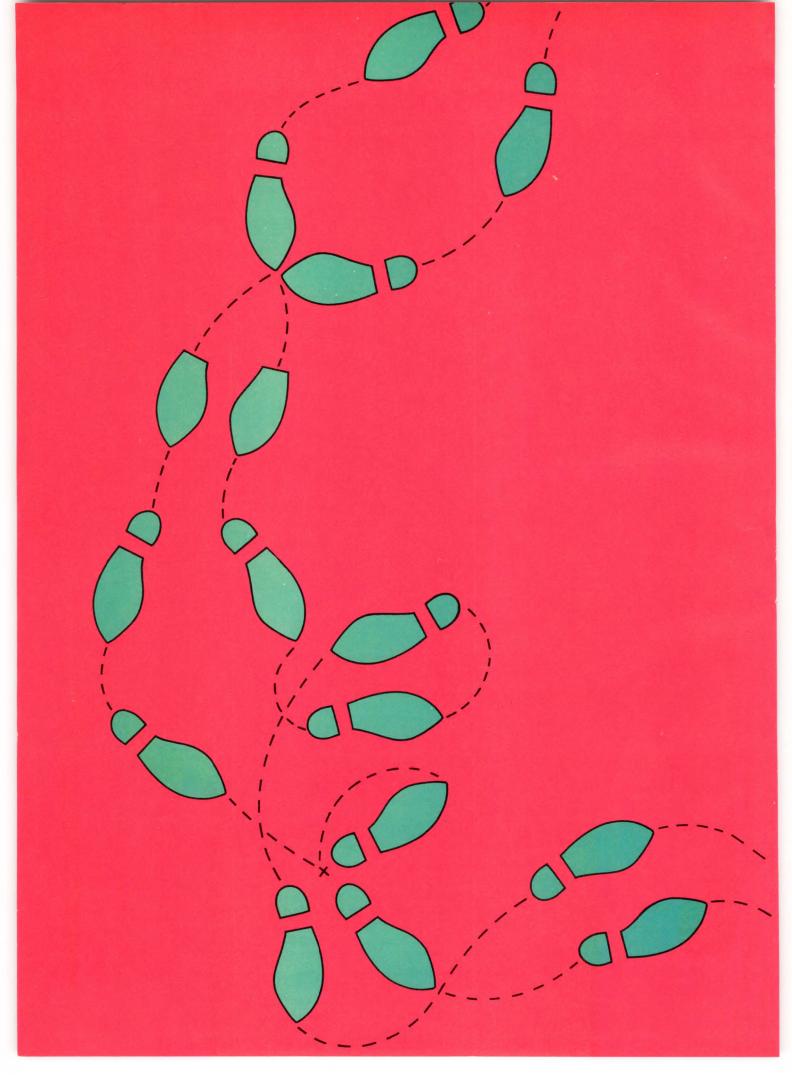
#### For more information...

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Creating useful products and services for you.





#### For four hours, you can quit living one step at a time.

Every great idea was new once, even the waltz. But one step at a time is one step behind the latest technology. At INMOS, we've made the move to parallelism and we're bringing our act to you.

INMOS invites design engineers and engineering managers to come to the free, half-day seminars we're conducting throughout the USA and Canada. We will present a proven, practical and economic approach to the design and implementation of high performance concurrent systems using our Transputer family. Not only will we talk, we'll actually demonstrate scalable, parallel designs using our readily-available Transputer evaluation boards. And we'll be on our toes for any questions you may have.

Transputers are high performance microprocessors optimized for high level language use, and incorporate special features for multitasking and multiprocessor support. The IMS T414—the first in the family—is a 32-bit machine, integrating a high performance processor, 2 kilobytes of fast RAM, four fullduplex interprocessor communications links (with an eight channel DMA engine to service them), and a 32-bit memory interface which includes a DRAM controller: all on a single CMOS chip, dissipating under a watt. And the best part—it's available now.

With its special design, the processor offers execution rates up to 10 MIPs. It combines direct support for multitasking, floating point and block transfer with submicrosecond procedure call and task switching.

The links are used to connect any number of Transputers to form systems for a wide range of applications, including numerical computation, AI, robotics, distributed systems, real-time control and digital signal processing.

Development tools for the T414 are available now to support programming both single and multiprocessor systems. Versions of the development system exist for use with IBM PC XT and AT machines, VAX/VMS and Stride 440.

The Transputer family includes 32 and 16-bit Transputers, peripheral controllers, link adaptors, evaluation boards and development tools to support OCCAM, C, Fortran and Pascal.

Now that you know a little more about Transputers, point your feet in our direction. Mark the date on your calendar, put us on your dance card and phone us now to RSVP.

INMOS Corporation, Colorado Springs, Colorado, Telephone (303) 630-4000; Bristol, England, Telephone 0272-290-861; Paris, France, Telephone (1) 687-2201; Munich, Germany, Telephone (089) 319-1028.

#### Transputer Seminar Schedule

DATE	LOCATION	PHONE NUMBER
May 5	*Vancouver	(206) 453-8881
May 5	Chicago	(312) 382-3001
May 6	*Seattle	(206) 453-8881
May 7	Minneapolis	(612) 941-9790
May 7	Portland	(503) 620-1931
May 9	Salt Lake City	(801) 268-8440
May 9	St. Louis	(314) 521-6683
May 12	Dallas	(214) 234-8438
May 12	San Jose	(408) 988-6300
May 13	*San Jose	(408) 988-6300
May 14	Austin	(512) 346-9186
May 14	+Los Angeles	(818) 704-1655
May 15	*Los Angeles	(818) 704-1655
May 16	Houston	(713) 531-4144
May 16	Orange County	(714) 261-2123
May 19	Tulsa	(918) 744-9964
May 19	San Diego	(619) 565-9444
May 21	Oklahoma City	(918) 744-9964
May 21	Albuquerque	(505) 888-0800
May 23	Kansas City	(913) 342-1211
May 23	Phoenix	(602) 996-0635
May 27	Cherry Hill, New Jersey	(215) 322-7100
May 28	Orlando	(305) 660-9600
May 28	+ Baltimore	(301) 544-4100
May 29	*Baltimore	(301) 544-4100
May 30	Fort Lauderdale	(305) 660-9600
May 30	Washington, D.C.	(301) 544-4100
June 2	Indianapolis	(317) 844-5222
June 2	Huntsville	(205) 883-9630
June 4	Cleveland	(216) 831-9555
June 4	Atlanta	(205) 883-9630
June 6	Detroit	(313) 478-8106
June 6	Raleigh	(919) 878-8600
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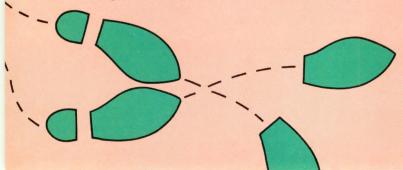
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CIRCLE 14



#### SIXTEEN TOUGH ASSIGNMENTS.



A period measurement is made on a 100 MHz clock using the extended accuracy and resolution of the Counter/Timer/ Trigger in the 2465 DVS.



A frequency measurement is made with the same high precision. Simply press two buttons, and the period measurement on the left is converted to frequency.



Short time intervals can be measured most accurately with the easy-to-use time cursors. They also make quick work of longer intervals, with 1% accuracy.



Calculated frequency takes only seconds. The time cursor measurement on the left can be converted to frequency with push-button ease and 1% accuracy.



This fast-pulse rise time is nearly that of the scope. The 2465 achieves maximum bandwidth with minimum waveform aberrations. This level of pulse



response ensures that **pulse** width and amplitude measurements on fast waveforms (above) truly reflect conditions in a circuit under test.



Propagation delay measurement accuracy is assured by built-in propagation delay matching. Delay between Channels 1 and 2 can be corrected to the probe tip.



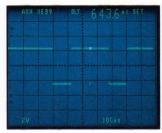
Overshoot and ringing measurement accuracy requires flat response in a probe/oscilloscope system. Tek probes and scopes are designed to work together.



**Logic-level violations** can be spotted quickly on a TTL waveform (above) with measurement cursors set to define logic-level boundaries.



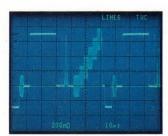
The Word Recognizer (with a binary word) is used to pick out a pulse train in a data stream. The time cursors measure pulse train duration.



**Identify a word position.** The Word Recognizer (in HEX) is intensifying a word position and measuring delay relative to a waveform on another line.



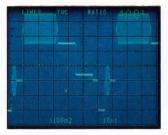
**Delayed sweep** is used to expand the last pulse in a pulse train. The intensified zone identifies the expanded pulse position.



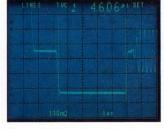
TV line trigger in the 2465 DVS displays a full-field composite test signal. The built-in TV clamp circuit removes hum and tilt on the ac-coupled video.



Calibrate cursors in IRE units with variable attenuation. Blanking level to reference white level is defined as 100 IRE units in NTSC video.



Burst amplitude should be 40 IRE units in NTSC video. The cursors quickly measure other waveform amplitudes. Field triggering checks any line.



**Sync width** and blanking are common, easy-to-make timing measurements. Accurate time measurements can be made anywhere in a video system.

# FIVE EASY ANSWERS. THE TEK 2400 SERIES.



You can simplify even the most complex measurements with the performance and convenience of Tek's 2400 Series family. No other portable scopes meet such diverse requirements in research and design, manufacturing

Features

and service.
The 300 MHz 2465 and
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foundation of the family.

They include all the features that set a new high performance precedent. For example, standard delayed sweep Δ-Time to 0.5% accuracy. Coupled sweep speeds to 1 ns/div in the 2445 and 500 ps/div in the 2465 for tough timing measurements. And four-channel capability for observing and trouble-shooting logic circuits.

Best of all, these standalone scopes are proof that powerful capability doesn't have to be complicated. Time and voltage cursors for fast and easy measurements, CRT readouts showing waveform parameters and front

reatures	2445	2465	2465 CTS	2465 DMS	2465 DVS	
Bandwidth	150 MHz	300 MHz	300 MHz	300 MHz	300 MHz	
Max. Sweep Speed	1 ns/div	500ps/div	500ps/div	500ps/div	500ps/div	
Accuracy; Vert/Hor	2%/1%	2%/1%	2%/1%	2%/1%	2%/1%	
Vertical Sensitivity	2 mV/div	2 mV/div	2 mV/div	2 mV/div	2 mV/div	
Trigger Freq. Range	250 MHz	500 MHz	500 MHz	500 MHz	500 MHz	
Trigger Modes	Auto Leve	l, Auto, Norn	n, Single Sec	luence		
Counter/Timer/ Trigger/Word Recognizer	*	*	STD	STD	STD	
DMM	*	*	N/A	STD	STD	
Video/TV	*	*	N/A	N/A	STD	
Four P6131 Probes	*	*	STD	STD	STD	
GPIB	*	*	STD	STD	STD	
Rackmount	*	*	*	* .	*	
Warranty	3-year on	parts and lal	oor, including	CRT		
	\$3590	\$5350	\$7150	\$8400	\$9200	

2465 CTS 2465 DMS 2465 DVS

\$595

\$400

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panel settings, and simplified trigger operation make these scopes a pleasure to use.

Three specially configured, specially priced Special Editions offer enhanced measurement capabilities for both systems and stand-alone use. At the top is the 2465 DVS with integral GPIB interface, DMM, Counter/Timer/Trigger/Word Recognizer, and Video measurement capabilities. Easily the most powerful portable ever developed.

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CIRCLE 16

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CIRCLE 17

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#### NEWSFRONT

#### 'Hard' cells lift ASICs to board-level performance

#### BY MARTIN GOLD

Somerville, N.J.—A new approach to placing and routing standard cells and macrocells gives applicationspecific ICs the performance normally expected from discrete logic elements connected on a pc board. The so-called "silicon circuit board," conceived by RCA Corp.'s Solid State Division, draws on an extensive library of CMOS logic cells and on new software that automatically lays out and interconnects rectangular cells of any size.

"It's a comprehensive package including simulation—that takes the ASIC designer from a functional block diagram to a patterngeneration tape or a mask, all in as little as two weeks," says Hesh Khajezadeh, division vice president for ICs. Already the software is up and running for a few RCA customers, and by mid-year it will be available at RCA design centers and then at distributors.

#### MODEL SHORTCOMINGS

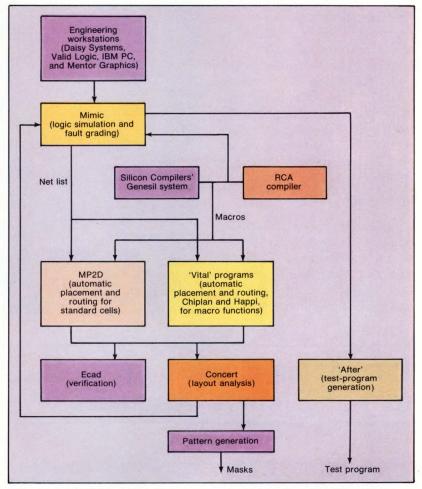
Until now cell-based ASICs used software models for the logic functions. The models are assembled by interconnecting the elements of a net list to emulate a desired function. However, when migrating from discrete components on a pc board to an ASIC, performance can be lost, basically because of wiring

RCA's technique turns that upside-down. Designers now have more than a fighting chance of getting pc board performance from their ASIC chips. Instead of connecting only net-list elements, the actual discrete components are replicated on the ASIC chip as hardware-based macrofunctions. Masks

from existing discrete logic elements are used, with their bonding pads and any unnecessary output structures removed.

Before placement and routing begin, the chip is fully simulated by a program RCA dubs Mimic, for module imitating modern ICs (see the figure). Then the design is verified and a waveform analysis run. At this point the placement and routing software, based on proprietary algorithms, takes over. It automatically determines the number of "domains" on the chip. Domains represent the blocks of standard cells and macrofunctions drawn from a customer's net list.

The system actually uses two placement and routing programs



RCA's development system for application-specific ICs uses hardware-based macrocircuits to deliver boardlike performance. Key elements include Chiplan and Happi, two Vital programs that handle placement and routing, and RCA's Mimic logic simulator. Other macrofunctions can be designed with silicon compilers.

#### NEWSFRONT

that fall under the name Vital, for VLSI interactive and automatic layout. The first program, called Chiplan, routes the chip automatically but lets the designer interactively move the cells around the chip. Basically a floor planner, it allows the designer to view the overall layout and make changes as necessary. The second program, referred to as Happi, makes both placement and routing automatic, using data culled either from a net list or a schematic diagram.

The software programs will define the standard cells and macrofunctions in the RCA library, as well as the size of those cells.

At the start, the "hard" cells will encompass HC and HCT circuits in 3-µm CMOS, followed by the company's 2-µm ACL circuits. Eventually the lineup will include more complex 2-µm macrofunctions, for example, core processors and analog circuits.

#### IN THE WORKS

In addition, nonvolatile memory cells and bit-slice devices will work their way in, thanks to RCA's alliance with WaferScale Integration Inc. (Fremont, Calif.). What's more, silicon compilation tools developed by RCA and Silicon Compilers Inc. (San Jose, Calif.) will generate new cells as well.

The placement and routing programs now run on VAX superminis and will be ported to Mentor Graphics workstations. The Chiplan interactive software also works with certain Tektronix terminals.

Following the package's release to RCA design centers, the software will be available through RCA's distributors, Schweber Electronics and Hamilton/Avnet. Later this year, customers will be able to license the software for their own use.□

#### National readies 250-cell library

Santa Clara, Calif.—National Semiconductor Corp. is quick on RCA's heels. Later this month, at the Custom IC Conference in Rochester, N.Y., the company will unveil an extensive library of standard cells and macrocell functions—nearly 250 in all. Among the initial pickings will be CMOS 74HC logic devices, dual-port RAM building blocks, 2900 series bit-slice processors, microcontrollers (for instance, the new 16-bit HPC), and advanced products like RAM and PLA generators. Moreover, the analog portion of the library will be filled by comparators, simple op amps, voltage regulators, and digital-to-analog converters.

Next year the cell library will expand considerably, taking in the 32-bit 32000 microprocessor, as well as telecommunication devices like codecs, filters, and building blocks for the Integrated Services Digital Network.

National targets cells with 2-µm geometries now and 1.5-µm geometries later this year. "Many of our functions will be available as either cells or gate arrays, so that system designers can migrate to either technology," says Fred Horne, National's vice president for customer-specific products.

Like RCA, National will offer a variety of design automation software for its cell library, but mostly it will rely on popular packages from outside software vendors. It also has its own automated CAE system that performs timing analysis as an integral part of logic simulation. The program, called Newton, will be described in detail at the conference.

Already National has lined up workstation support for the library. IBM PC-based FutureNet and Daisy systems will take care of schematic capture and prerouting simulation; support for workstations from Mentor Graphics and Valid Logic is due later this year. Placement and routing tasks run on National's IBM-compatible mainframes, using the Merlyn-S software from Tektronix's CAE Systems Division. Engineers will also be able to work through National's design centers and its distributor, Hamilton/Avnet.

#### Packaging catches up to VLSI power demands

BY VINCENT BIANCOMANO

Seattle-The thermal and electrical problems spawned by dense chips and packed circuit boards force packaging technology to depart radically from its traditional evolutionary path. Consequently, a package's primary job-to house the chip—now takes a back seat to the more technically challenging task of making a chip carrier thermally and electrically inert.

Fortunately, tape-automated bonding and surface mounting already minimize a package's parasitic capacitance and inductance, the biggest obstacles so far to achieving high-frequency response in a chip. At next week's Electronic Components Conference, attention will be focused on the packages working with speedy chips, that can handle power much higher than the 3 to 5 W typical of today's applica-

Dissipating or otherwise withstanding large amounts of power remains the most elusive goal for VLSI packages. To increase reliability, manufacturers are turning to such esoteric techniques as cooling chips with liquid reservoirs and laser-bonding packages for highfrequency, high-power work. In addition, the relatively new art of photolithography is bolstering pin-grid array packages.

In an innovative scheme, water

carries off heat from an array of 25 square packages mounted on an alumina substrate. Nippon Telegraph and Telephone Corp.'s Electrical Communications Laboratory (Tokyo) fabricates 29 coolant channels 1 mm deep on a six-layer substrate containing 900 I/O pins. The channels are staggered to avoid disturbing the arrangement of the via holes, which are formed before the coolant channels.

NTT's experimental watercooled substrate, with dimensions of 85 by 105 mm, dissipates up to 600 W (7.5 W/cm<sup>2</sup>) for a flow rate through the channels of 0.8 liter/ min. Power-handling capacity of the module (per volume) is 5 kW per liter of water, which the company claims is a tenfold improvement over conventional methods for indirect cooling. If practical in production volumes, it is a breakthrough.

The minimal thickness of the cooling channels enables designers to reach a long-sought goal of stacking VLSI packages. From the manufacturing standpoint, the same punching process that makes via holes can form the cooling and conductor sections on the substrate.

#### STRONG SEALS

Heat from a package is only half the cause of poor reliability. Equally responsible is the heat produced by high-temperature processing. For example, arc welding used during hermetic sealing of ceramic packages calls for a package that can endure a short, intense beam of energy. As a result, new materials and laser welding are prominent.

Nickel plating of aluminum-alloy housings, suitable for high thermal conductivity, simplifies hermetic sealing by laser. Fujitsu Laboratories Ltd. (Atsugi, Japan) applies the experimental technique to a chip for microwave applications. The nickelplating scheme overcomes cracks in the weld zone caused by hightemperature arcs. Indeed, just the opposite occurs: The electroless nickel plating strengthens the weld

and protects the package from outside elements.

Today's chip carriers owe their high density to photolithography. This technology, combined with some new materials, could make the pin-grid array the leading package for both speed and power.

#### **POWERFUL PIN GRIDS**

A 208-pin grid array with a ceramic base and cap comes from Mitsubishi Electric Corp. (Hyogo, Japan). Courtesy of photolithography, the device has etched copperfoil patterns on a film of polyimide. This technique is an extension of one used by Amp Inc. (Harrisburg, Pa.) earlier in the year for in its densely packed leadless ceramic chip carrier.

Mitsubishi puts to work an inexpensive method for creating lowresistance, low-loss signal paths as well as for the array's power and ground planes. Line width is reduced to 0.1 mm and spacing to 0.05 mm.

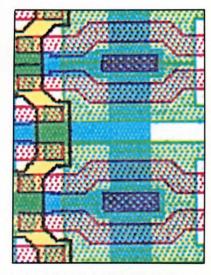
The polyimide film draws its advantage from a low dielectric constant, about 40% that of the alumina ceramic typically found in pin-grid arrays. Thus, pin-to-pin capacitances are reduced by a factor of four, and capacitance between signal leads and ground by a factor of five. Furthermore, thermal conductivity can be improved several times over that of alumina if the housing's base plate contains silicon carbide. □

### 400-dot/in. plotter attacks thermal and ink-jet arenas

#### BY STEPHAN OHR

Santa Clara, Calif.—The electrostatic color plotter stands poised to defend its position in the low-cost CAE plotter market from a challenge by ink-jet and thermal machines. At the forefront of the de-

fense is a new version of Versatec Co.'s Spectrum series. With a price tag below \$15,000, it may be the first color plotter to lay down 400 dots/in. for 81/2-by-11-in. and 11-by-17-in. narrow-paper formats



Versatec's 400-dot/in. electrostatic printing process allows higher drawing resolution and densities (left) than that of the previous generation of 200-dot/in. printers (right) at lower cost. The layouts are magnified 400%.

#### NEWSFRONT

known as the A- and B-sizes.

Versatec, a subsidiary of Xerox Corp., plans to introduce the plotter at the National Computer Graphics Association convention in Anaheim in two weeks. Versatec's move is in response to the recent explosion of low-cost CAE workstations.

Used with these machines, inkjet, thermal, and electrostatic plotters take on engineering applications such as IC design and pc board layout, as well as business graphics. They can deliver thousands of colors and print at speeds of under 2 minutes per page at a cost of less than 20¢ each.

Typical of what Versatec is up against is the CH-5300 series of thermal printers from Seiko Instruments Inc. (Milpitas, Calif.). The units deliver as many as 4912 colors with resolutions of up to 203 dots/in. for less than \$10,000. The Seiko plotters use a thermal transfer process in which heated probes transfer ink to paper.

Improvements in ink-jet technology now yield resolution that approaches the density needed for CAE drawings, at the \$15,000 price point. The information display group of Tektronix Inc. (Beaverton, Ore.) just introduced a unit that produces paper copies in 2 minutes at a resolution of 154 dots/in.

#### **CLEARER AND SMOOTHER**

Versatec raises the stakes with its higher-resolution machine, which produces printouts with smoother lines and curves. It is particularly suited to complex circuit layouts because it generates denser plots than 200-dot/in. machines (see the figure).

Versatec extensively modified the Spectrum's print head to yield the improved resolution, according to company product manager Dale Richmond. Not only did the dots have to be smaller, but the headand paper-positioning system also had to be refined.

The company added a second row of 200-dot/in. electrodes to the head, with the second row offset from the first. The ink deposition from the two rows is timed so that negative charges on the moving paper attract a single line of overlapping 4-mil dots, each on 2.5-mil

#### **GOOD MEMORY**

High resolution depends not only on the size of the deposited dot, but also on the plotter's mechanical ability to bring the paper back to the same spot exactly to deposit a second or third color. The registration for each dot-what Richmond calls the dot-to-dot accuracy—is within 0.5 dot, or 1.25 mils over a 17-in. range. In comparison, 8-mil dots are held to a 3- or 4-mil registration accuracy on 200-dot/in. plotters.

A resolution of 400 dots/in. re-

quires enormous memory, since each dot must be addressed individually. For instance, standard bitmapped technology would require a 13-Mbyte file to store an 11-by-17-in. drawing.

Versatec, though, incorporates a vector-polygon drawing technique into its controllers that demands less memory. Drawing elements, such as an npn transistor layout, are stored as a combination of polygons on a hard disk. With about 1.2 million elements involved, approximately 12 Mbytes of memory are needed to store the entire library of symbols as polygons. But since a typical drawing requires only 30 elements, the data file would be significantly less than the 13 Mbytes required for standard bit-mapped technology.

Richmond foresees the 51/4-in. optical disk, with 140-Mbyte capacity, as the eventual storage device for the plotter.□

# Fabrication line for 6 in. wafers foils spies

#### BY TERRY COSTLOW

Bloomington, Minn.—Worried about Soviet spies stealing your chip fabrication techniques? Concerned that the microwave dish on the building next door may be picking up confidential product specs? VTC Inc. can set your mind at ease. On the ground floor of its recently opened headquarters, in a Minneapolis suburb known as "silicon tundra," is a high-security vault that meets Department of Defense requirements for the entire IC production process, from design to fabrication.

Elsewhere, devices destined for military equipment are designed in one facility, their masks created in a second, and the chips fabricated in a third. Now the cautious designer, or someone with a paranoid client, can

go the whole nine yards in one place. The walls of the VTC vault, 14 in. thick and lined with copper, shield CAE devices from external spooks. Fiber-optic telephone and data cables prevent rf leakage, and bandpass filters on power lines ward off tapping. Access controls limit entry to the entire vault, including the 30,000-ft<sup>2</sup> clean room.

The VTC facility contains CAE workstations from Mentor Graphics working with a VAX superminicomputer host. CMOS chips with 1.25-µm geometries are fabricated there from 6-in. wafers.

Under a recent agreement, the Genesil compiler system from Silicon Compilers Inc. (San Jose, Calif.) will be available for VTC's cell library.□

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### NEWSFRONT

# High-power switchers survive 100,000 hours

#### BY VINCENT BIANCOMANO

Melville, N.Y.—A hot innovation in power-supply technology enables high-power switchers to run cooler and longer. The latest example of increased reliability at lower cost will arrive in July when Lambda Electronics Corp. introduces the LFS family of power-supply switchers for 50 W to 2 kW. Compared with current supplies, specifications for mean time between failure will double to 100,000 hours while the price will drop about 25%. Pivotal to the price-performance of the fowardconverter supplies is a bipolar controller chip.

The chip includes a 150-kHz time base and voltage reference as well as circuitry for current limitation, brownout protection, and soft start. The combination of chip and module handles over-voltage protection

To handle a power range 50 W to 2 kW, a switcher would normally need several hundred discrete components. The bipolar chip and the module it mounts on (see the figure) cut the parts count to 70. Furthermore, the IC and the module are compatible with other Lambda supplies, owing to a proprietary circuit for voltage-offset compensation.

The chip includes a 150-kHz time

Module V<sub>CC</sub> (chip) Output Source-sink functions output Line-Turn-off Circuit Enable Time Currentcircuit Oscillato amplifier Opto solator forward Closed for Current-limiter IC functions shaping

The bipolar controller chip from Lambda contains virtually all the logic for switching high-power supplies. Compatible with the company's entire line of supplies, the combination of chip and module delivers current limitation, voltage regulation, brownout protection, and a stage for driving the supply's output transistor.

and line and load regulation of  $\pm 0.1\%$ . A 500-W unit will carry a price tag of about \$330, while a 200-W supply will go for about \$150.

Credit for the switcher's flexibility goes to Lambda's undisclosed improvements in forward-converter technology, in which both the primary and secondary circuits operate simultaneously. The new generation of forward converters improves costperformance threefold over the previous models. (The ratio of power per dollar is multiplied by the supply's power-vs-size ratio.)

"Compared with push-pull, fly-back, and half-bridge topologies common in a conventional switcher, forward converters yield the most efficient and low-cost design," explains Dan Enzone, vice president of engineering. "They inherently require fewer parts, and they apply less electrical stress to those components."

The forward converter permits the bipolar chip to easily extend the supply's duty cycle by controlling both the switcher's on-time and the switching period. Thus, the on-off timing ratio can be adjusted automatically depending on the line voltage.

The current limiter works in three modes—standard, foldback limiting, and foldback with frequency shifting. The choice of modes improves the regulation's efficiency and the supply's response time. The overload circuitry also reduces the supply's susceptibility to switching noise.

Despite the high power levels handled by the relatively small supply, the unit meets the European VDE standard of 5-mm spacing between primary and secondary circuits

Finally, with a special demagnetizing circuit, Lambda can employ a single-ended FET rated at 500 V at 100 kHz in the power output stage, instead of the usual tandem FETs or bipolar stages.□

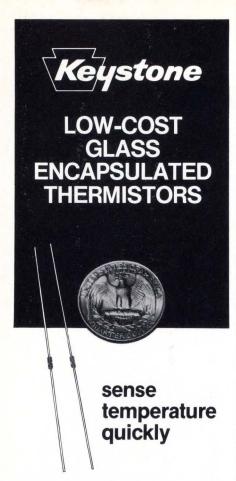
(Newsfront section continues on p. 42)



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CIRCLE 21

**INDUSTRY WATCH** 

# Chip users, prepare. Spring cleanup could affect your supply



After the dust settles from the industry recession, your favorite semiconductor devices may suddenly become hard to find. Many IC vendors are busily cleaning house, dropping products they no longer deem worthwhile producing in volume.

For example, Motorola recently said it will discontinue more than a half-dozen microprocessor components, including some from the

once-popular 6800 series. In addition, over the past year Fairchild Semiconductor has phased out some 8-bit microcontrollers and cut back production of its low-power Schottky logic circuits. These moves are just the tip of the iceberg. No doubt chip vendors will increasingly examine their old product lines, training an eye on turning them off quickly if necessary.

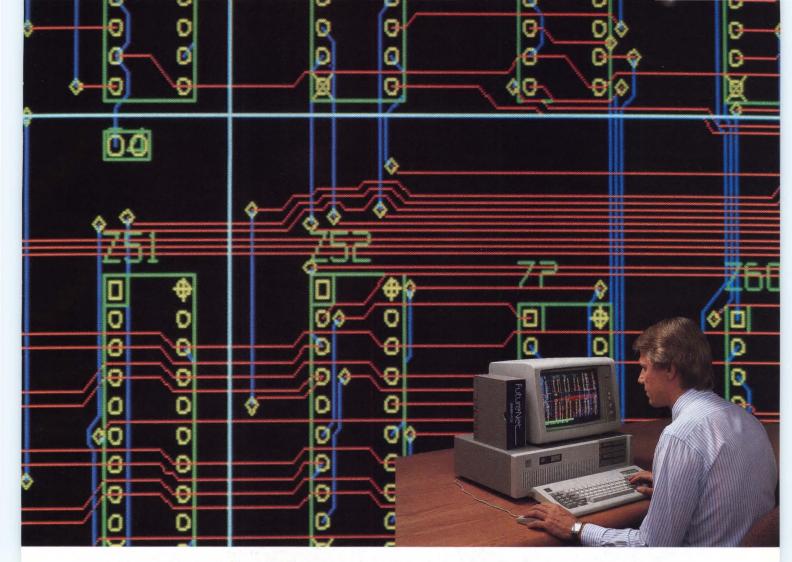
The reasons are clear-cut. Technology is changing rapidly. CMOS now wins out over NMOS as the process of choice; in fact, few new NMOS devices are being designed. Gate arrays and standard cells are displacing "glue logic" in new system designs, and many, if not most, companies are refurbishing their older 3and 4-µm production lines with equipment that can produce chips with 2- and 1.5- $\mu$ m geometries.

Another factor comes into play, too. As the semiconductor industry recovers from the worst setback in history, resources are severely limited. Layoffs over the past year have sharply reduced the head count at many companies. Naturally, deploying the smaller staffs to the areas of greatest potential profit means that older product lines will no longer get support. Moreover, available capital is going into upgrading equipment.

Chip users, you should devise your strategy with care. To ensure the future of your products, you may have to change your design methods and throw your lot in with the latest chip design techniques and software. It's also important to improve your relationship with chip vendors: Make them aware of your long-term needs for specific components.

True, many discontinued circuits will become available from alternative suppliers, but second and third sources are rarely as good as the first. With fewer companies supplying a specific product, prices could rise. And don't forget, there's no guarantee that the alternative source won't do the same as the original manufacturer and discontinue products as the market declines.

Martin Gold



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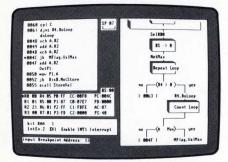
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CIRCLE 23

#### NEWSFRONT

### Amiga taking bows as bench workstation

#### BY RAY WEISS

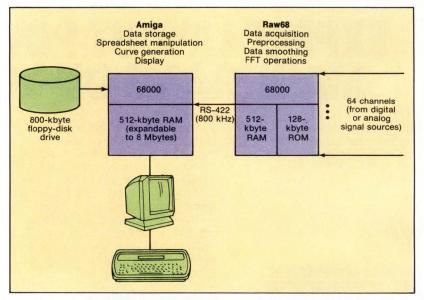
Gardena, Calif.—Introduced last year as the latest and brightest personal computer for the low-end home market, the Commodore Amiga is finding a niche as a tool for engineers working in the laboratory. What attracts the technical community to the machine is its ability to deliver the performance of a 68000-based, multitasking color graphics workstation for \$1300far below the cost of any competing model.

At the winter Comdex, Datacraft Inc. took the wraps off an engineering data acquisition system that uses the Amiga for data analysis. The computer serves as a back-end system for Datacraft's specialized

front-end processor, the RAW 68. Data is piped into the Amiga from a data acquisition subsystem at rates of up to 800 kbits/s. The data is then processed and held for later use.

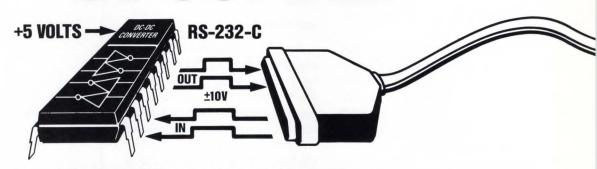
The front-end subsystem fields up to 64 channels of data from applications as diverse as process control, medical monitors, and laboratory analytics. Moreover, the front end can support 12-bit resolution of analog-to-digital conversion at up to 100-kHz.

The front end is based on another 68000 mounted with 512 kbytes of RAM and 128 kbytes of ROM. Inside the ROM are various routines for smoothing and correlating raw data, including fast Fourier trans-



Datacraft uses an Amiga personal computer to provide back-end processing for a 68000-based data-acquisition front end, the RAW 68. Front-end routines smooth and preprocess the data. The Amiga stores, manipulates, and displays the data.

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While you're thanking people, don't forget Maxim's Dave Bingham, the guy who's invented more industry standard parts than most companies. It was his design genius that turned Charlie's idea into silicon.

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#### NEWSFRONT

forms and spectral analysis. Additionally, users can specify line filtering and optoisolation.

Data fed to the Amiga is entered into a spreadsheet with 256 columns by 8000 rows for further manipulation and processing. Using Amiga's graphics package, designers can map the data into curves for display.

The only modification to the Amiga involved converting the system's 20-kbyte/s RS-232-C serial interface into a 2-Mbyte/s RS-422 port. The conversion increased throughput to more than 800 kHz from less than 100 kHz.

#### **NEW GAME PLAN**

Commodore International Ltd. (Westchester, Pa.), developer of the Amiga, targeted the machine at the home and commercial end user, not the technical professional. But its sophisticated multitasking hardware and operating system and graphics capabilities designed for advanced video games are more than adequate for many engineering tasks. A variety of software packages are now available for Amiga's distinctive operating system, developed by Metacomco Inc. (Monterey, Calif.).

Under its plastic case are some savvy design techniques that account for its high performance and low cost. For instance, special VLSI processors offload operations from the microprocessor for graphics, animation, and I/O processing.

Amiga designers take advantage of the 68000's relatively slow, 10-MHz clock rate. The custom coprocessors steal memory cycles while the CPU is processing an instruction. For most instructions, every other memory cycle can be used by the coprocessors without interfering with the CPU. Thus, multiple operations, such as graphics and I/O processing, are generally concurrent with the Amiga's CPU pro-

cessing cycles.

Amiga's 25 DMA channels bypass the CPU, further aiding multitasking and intensive I/O processing. Each device or port is assigned its own channel, reducing contention. Also, the limited memory of some low-end personal computers is not a problem, since up to 8 Mbytes can be directly addressed with expansion boxes.

#### WHAT'S NEXT?

Amiga's growing reputation as a capable engineering tool is prompting a host of other improvements. Rumors that a full 32-bit version is under development are flying. Some industry observers say Commodore will release a new model based on the full 32-bit 68020 by the end of this year.

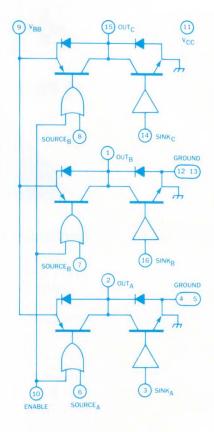
Already, there is at least one supplier of a plug-in 68020 board. Introduced last year by Computer Systems Associates Inc. (San Diego, Calif.), the board connects directly into the Amiga's 68000 socket. Computer Systems' latest board, the 68020-PGYC/MEM, also carries a 68881 floating-point unit and 512 kbytes of 120-ns static RAM for high-speed, number crunching.

Datacraft plans to use the Amiga as a terminal for other engineering systems. Moreover, the company is working on an interface for direct data acquisition and a number of additions to speed the Amiga's integration into the engineering world. Also being readied is a peripherals box that will link add-on boards for the IBM PC to the Amiga, offsetting the incompatibility of its operating system.

Be sure to see Electronic Design's Professional Opportunities Section.

It starts on page 334.

# SPRAGUE PIC



#### UDN-2933B 3-CHANNEL HALF-BRIDGE MOTOR DRIVER

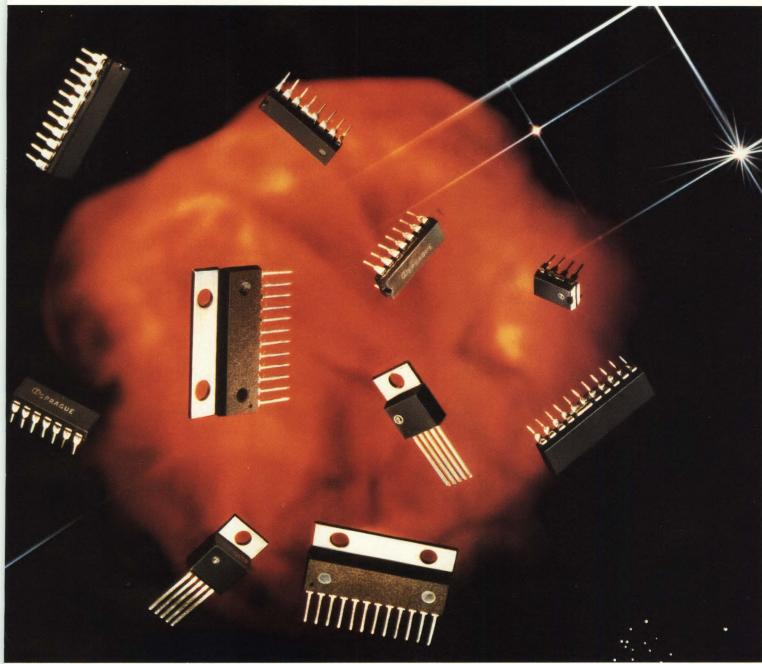
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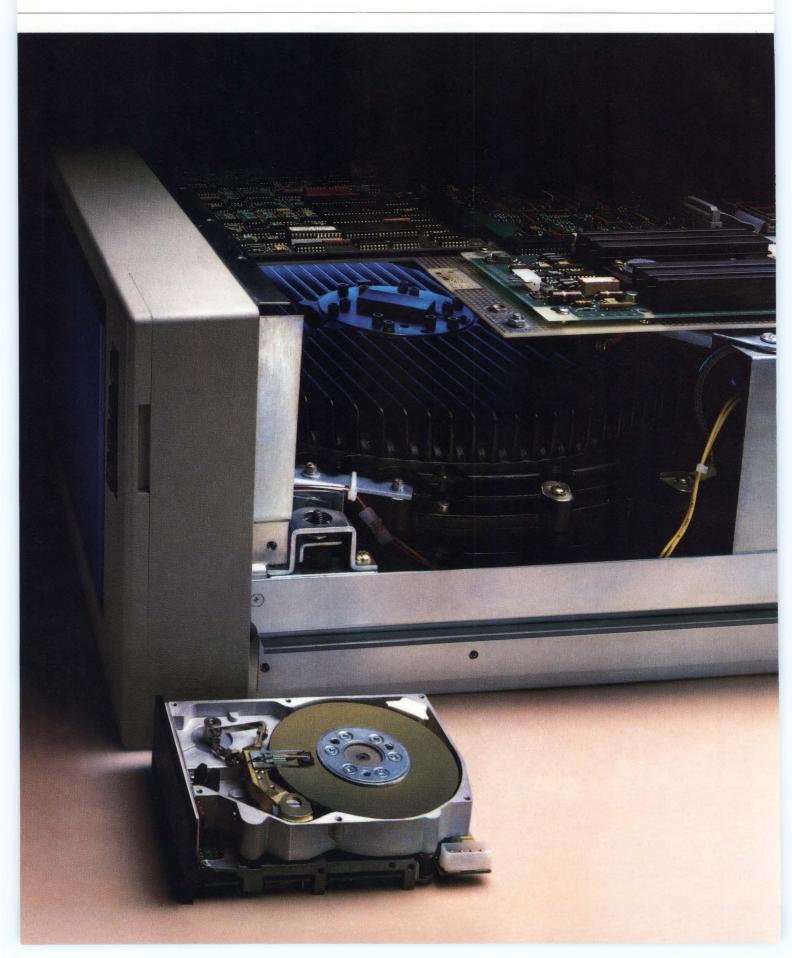
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Sprague has led the way in power interface since 1970. After originating its line of Power ICs (PICs), Sprague has increased emphasis on circuits for stepper, servo, and brushless d-c motors. Output drive capabilities have been extended to ±4 A per channel and to sustaining voltages exceeding 60 V. Motor driver types include half-bridge, full-bridge, dual full-bridge, three-phase, translator/driver, and power driver sink or source arrays. All devices include diode transient protection. Many feature current limiting (PWM), thermal shutdown, over-voltage and/or short-circuit protection. Sprague

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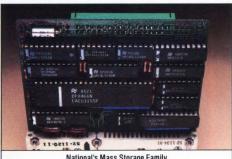
The disk industry today has a lot of heads spinning. With drives of all sizes, shapes, types and interface requirements. With more advanced technologies pushing transfer rates and densities ever higher. And with users demanding higher capacities — but in smaller, lower-power packages.

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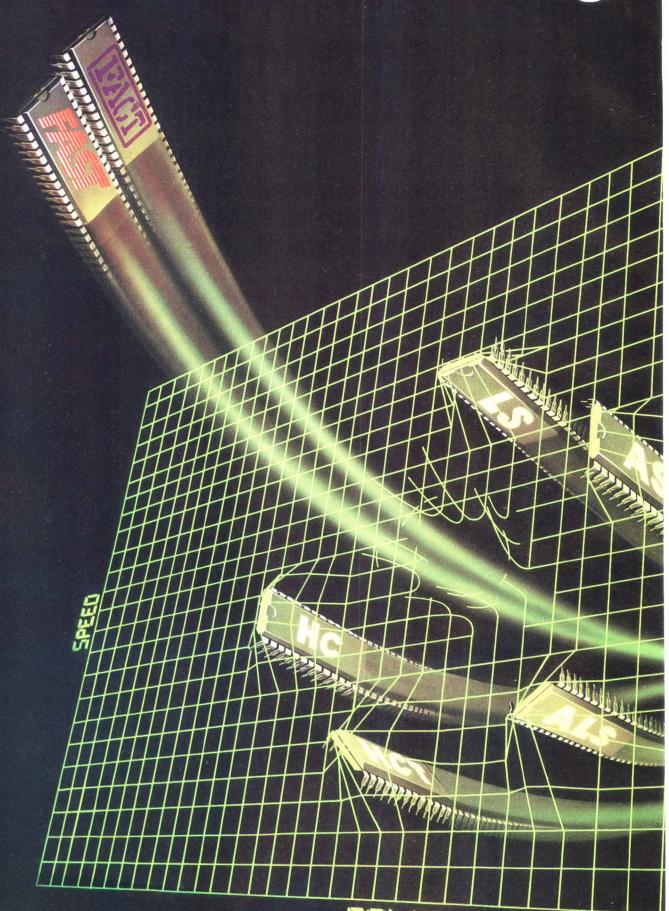
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CIRCLE 27

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along with the highest noise immunity available.

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FACT: Semicustom IC vendors report a 97–99% success rate for gate arrays, yet only 33% actually work when first tested in the system. Daisy's complete simulation environment improves design control and success rates two ways: First, array resimulation incorporating circuit timing modifications due to physical layout. Second, system level simulation where the array is simulated in the context of the target system. RESULTS: Substantially increased gate array and system design success rates.

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California Devices, Inc.® NEC Electronics Inc.® and RCA® have each introduced automatic gate array layout design kits for the MegaGATEMASTER. Now eight ASIC vendors support physical layout on the MegaGATEMASTER, in addition to the over 55 vendors who support electrical design and simulation on Daisy workstations—and the list is growing. Designers can select from a wide "portfolio" of ASIC vendor capabilities, gate counts and technologies.

MegaFAULT,™ Daisy's new high speed fault simulator provides the engineer with the highest confidence level in working, manufacturable silicon through reliable fault grading of test patterns required to detect potential manufacturing defects. MegaFAULT is fully integrated with Daisy design and verification tools and provides full support of ECL, CMOS, and other circuit technologies, and can also be used for fault simulations of board-level designs.

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### **CONFERENCE PREVIEW**

### Testing complex chips and software issues top agenda at Custom IC Conference

BY DAVE BURSKY and MAX SCHINDLER

With the use of gate arrays and cellbased chips expected to grow dramatically over the next few years, designers are beginning to attack the problem of testing chips with many tens of thousands of gates. At the same time, work is under way to enhance present design methods and to extend speed and density benchmarks. These developments, and others related to the fastest growing segment of semiconductor design, form the backbone of the annual Custom Integrated Circuits Conference.

Testing emerges as a critical issue as designers cram more and more high-speed circuitry onto a semicustom chip. As a result, designers are focusing on incorporating selftesting and fault-isolation schemes in their new chip designs.

In parallel with the efforts to crack the testing issues, designers are increasing density and speed. If you go . . .

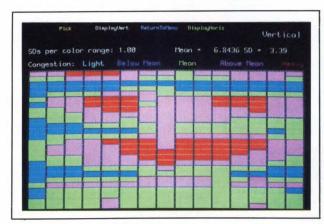
**CUSTOM INTEGRATED** CIRCUITS CONFERENCE MAY 12-14 ROCHESTER, N.Y. **ROCHESTER RIVERSIDE CONVENTION CENTER** (716) 865-7174

The channelless, sea-of-gates approach is expanding the density of gate arrays, while parameterized cells are adding to the complexity of cell-based chips. Many companies with standard-cell libraries are busy adding large cells that can be custom-configured simply by setting a few basic format values. Included among the cells are RAMs, ROMs, PLAs, shift registers, and other standard and simple structures.

Meanwhile, silicon compilation schemes are emerging that can produce complex devices like multiplier-accumulators. Furthermore, silicon compilation routines for analog-to-digital and digitalto-analog converters as well as switched-capacitor filters are becoming more practical.

That is not all that designers will hear at the conference. While CMOS comes on as the dominant process technology for semicustom and custom ICs, other approaches such as bipolar, gallium arsenide, and a mixture of CMOS and bipolar offer higher speeds than CMOS can achieve, but at a higher power consumption. For example, designers are now starting to use bipolar processing, which made its mark in high speed gate arrays, for cellbased circuits.

The volume of technical papers, however, shows that testing the upcoming generation of semicustom chips continues to be of paramount importance for designers. As circuit complexities reach 20,000 gates, setting-aside a few thousand gates for self testing and fault isolation more than pays for itself, according to designers at ETA Systems Inc. (St. Paul, Minn.). They believe that many VLSI circuits can no longer be tested at a reasonable cost unless





1. Congestion on a gate array as originally laid out shows up in red (left). But General Electric's ICmove can step in to produce a more easily routed layout (right).

### CONFERENCE PREVIEW

testability is built in.

ETA designers have developed a CMOS array that combines 12,000 logic cells (1.5 equivalent gates per cell), 2000 gates that form self-testing circuitry, and 238 signal I/O cells. The array, fabricated by Honeywell Inc. (Colorado Springs, Colo.), contains test circuitry that consists of an internal pattern generator which drives the logic array while a check-sum register accumulates the results. The final check sum can be compared with the desired value by an external maintenance controller. A test system with fewer than 40 pins can analyze the chip. Moreover, the test logic reduces the complexity of the test programs.

#### **SELF-TESTING 30,000 GATES**

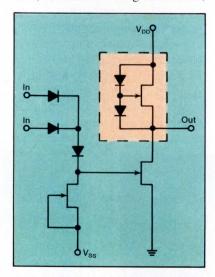
Fujitsu Laboratories Ltd. (Atsugi, Japan) developed a prototype for self-testing circuitry: a 30,000gate array patterned with RAM, ROM, and multiplier blocks. The concept uses a pseudorandom number generator and a pattern compressor that operate as 32-bit pattern manipulators, 16-bit pattern manipulators, or 32-bit shift registers. A simple counter generates memory addresses. The test circuitry, consisting of about 1160 gates, takes up about 4% of the chip; another 4% goes to a signal multiplexer and related wiring channels.

Stanford University (Stanford, Calif.) proposes a technique using scan paths to test for stuck-at-open faults in CMOS circuits. The twopattern test employs specially designed shift register latches and cannot be invalidated by arbitrary delays.

At Caedent Corp. (Colorado Springs), engineers devised a method to apply deterministic fault grading at the transistor level. On

the other hand, Microelectronics Center of North Carolina (Research Triangle Park) came up with a way to apply accelerated methods of testing combinatorial logic to synchronous, sequential logic. The technique relies on an extension to the center's Fault Blaster program, since its CPU and memory demands grow linearly with circuit size rather than exponentially.

As the test issues are being resolved, other companies are using new schemes and software tools to reap higher-density gate arrays. Two separate developments squeeze close to 100,000 gates on a chip by eliminating wiring channels. For one, LSI Logic Corp. (Milpitas, Calif.) teamed up with Toshiba Corp. (Kawasaki, Japan) to develop a channelless array with 318 programmable I/O pads. Any one of the pads can be an input, an output, or a bidirectional signal line. However, because of wiring limitations,



2. A bootstrapped arrangement (highlighted area) for the output buffer of a Schottky-diode FET logic gate yields circuit operation at close to twice the speed of a standard SDFL gate. Honeywell and the Mayo Foundation developed the array.

the company estimates that only about 40% of the gates are actually usable for now.

The second development, from Mitsubishi Electric Corp. (Itami, Japan), does away not only with wiring channels, but also with the dedicated I/O buffers. Since the company puts extra transistor pairs into the regions that would have been occupied by the I/O buffers, designers can create the buffers as needed for the system (ELECTRONIC DESIGN, Feb. 20, p. 38).

Software is often the major factor when it comes to designing gate arrays and standard-cell-based circuits. Designers from General Electric Co. (Research Triangle Park, N.C.) are readying two software tools for gate-array design. The first, Hicap, accepts a hierarchical logic description in the Tegas design language (TDL) and simplifies placement of modules and submodules. The second, ICmove, then displays a figure of merit for the flattened design and predicts the degree of congestion after routing (Fig. 1). In the displayed 13,000-gate array, the number of failed router connections could be reduced from 15 to 1 by relieving expected congestion.

As multilevel logic arrays gain popularity, conventional techniques often create designs with a large fan-in. But low fan-in is preserved by a design technique conceived at the University of California at Berkeley. Using this method, the gates in a Weinberger array can be stacked, producing a multilevel matrix (MLM) that, in turn, controls the fan-in. The MLMs are connected to their neighbors simply by abutment, because the routing is contained within the MLM tiles. The resulting layout consumes more silicon, but can be two to three times faster than an equivalent PLA im-

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### CONFERENCE PREVIEW

plementation.

Another Berkeley program, Sparcs, addresses constraints in hierarchical circuit descriptions. The program is a graph-based symbolic layout system for manual and automated design. Both digital and analog circuits can benefit from the program, whose algorithm detects overconstraints and produces layouts that are independent of technology.

For designing complex ICs from scratch, the future belongs to silicon compilation. Although graphics will be the preferred designer interface with the compiler, description languages will play an essential part. One such language, Skill from SDA Systems (Santa Clara, Calif.), is well-suited for the purpose. An expression entered in this incremental language can be immediately observed in the graphic representation. Combined with a general-purpose structured compiler, the language easily supplies the user with generators for specific function modules.

#### IT'S AN ANALOG WORLD

Much of today's digital circuitry owes its existence to the difficulties of producing analog ICs. As these problems get under control, designers want to mix the two technologies. They especially want translations into digital and back into analog, since the physical world runs under an analog regime.

A joint project by Seattle Silicon Technology Inc. (Bellevue, Wash.) and the University of Washington (Seattle) produced a compiler that synthesizes and lays out switchedcapacitor filters. The compiler generates either LC ladder simulation (leapfrog) or building block (biquad) realizations of Butterworth,

Chebyshev, Cauer, or Thompson low-pass, high-pass, bandpass, or band-elimination filters. Also working in the analog world, a software package compiles CMOS d-a and successive approximation a-d converters. Developed by the Georgia Institute of Technology (Atlanta), the software requires the designer simply to specify the number of bits and the linearity requirement.

In the digital world, the first compiler for multipliers, multiplier-accumulators, and arithmetic units puts LSI Logic in the spotlight (ELECTRONIC DESIGN, April 3, 1986, p. 51). Designers using the software can specify CMOS blocks that perform the operation  $A \times B + \Sigma C_i$ . Elsewhere, Silicon Design Labs Inc. (Liberty Corner, N.J.) has set about to develop an 8051 CPU core. To keep the core small, designers eliminated all I/O overhead. The supporting functions are highly modularized so that they can be integrated with the core on an as-needed basis.

#### **QUICK RELIEF**

To take many of the design headaches away from the engineer, research teams from the University of Illinois (Urbana), Gould Inc.'s Research Center (Rolling Meadows, Ill.), and the Electronics Technology and Device Laboratory of Fort Monmouth (Fort Monmouth, N.J.) have combined expert-system techniques with silicon compilation. The experimental Descart system translates behavioral descriptions and user constraints into a standard-cell representation. It applies user constraints to design strategies, evaluates the design, and makes trade-offs to satisfy the design goals. The translation process takes place in two steps: First the microarchitecture is generated, and then the functional units are created. During the first step, the software makes area and time estimates to aid in optimizing routines.

#### **BIPOLAR LEADS THE WAY**

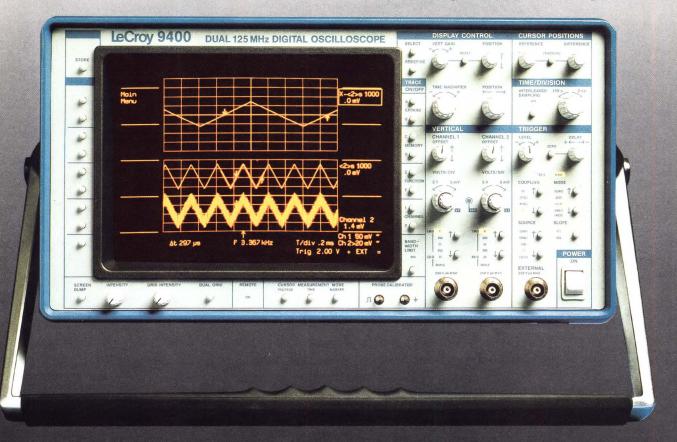
As a process technology, bipolar is leading to faster and denser circuits. And thanks to unusual circuit techniques such as nonthreshold logic, it can achieve extremely short gate delays. Such short delays can be compared with speeds that have been recorded for gallium arsenide.

The Electrical Communications Laboratory of Nippon Telegraph and Telephone Public Corp. (Atsugi, Japan) exploits nonthreshold logic and a super self-aligned transistor structure to develop a 7000gate array that cuts the propagation delays to a blazing 50 ps. Each cell in the array consists of a nonthreshold logic gate and a currentmode logic macrocell (with two levels of series gating), which together consume 16 transistors and 16 resistors. To keep the chip area as small as possible—just 8 mm on a side—no wiring channels are

Researchers at Honeywell Inc.'s Physical Sciences Center (Bloomington, Minn.) and the Mayo Foundation (Rochester, Minn.) capitalized on Schottky-diode FET logic to develop an array with 630-ps unloaded delays and power per gate of a tenth that of Ford's chip—just 150 μW. The array employs a bootstrapped buffer circuit to improve the gate's ability to handle higher-capacitance loads (Fig. 2). Although the circuit consumes about 50% more power than a standard SDFL gate, it is twice as fast for the same loading condition.□

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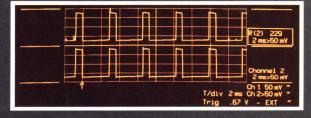
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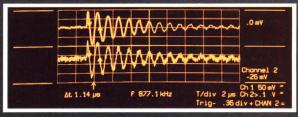
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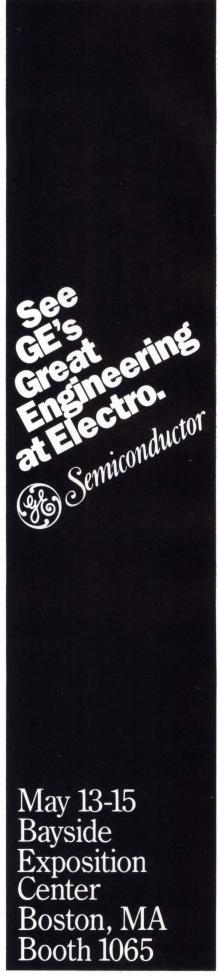
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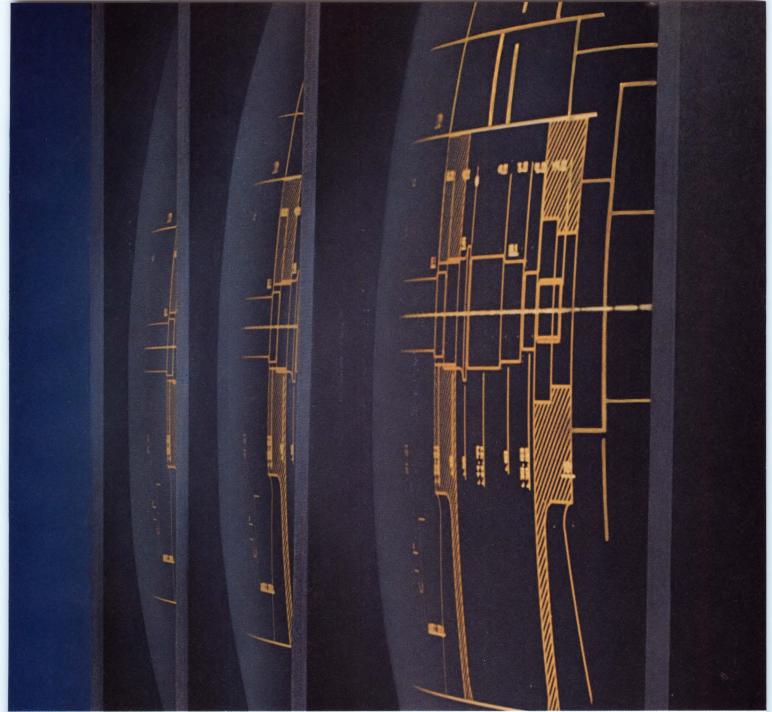
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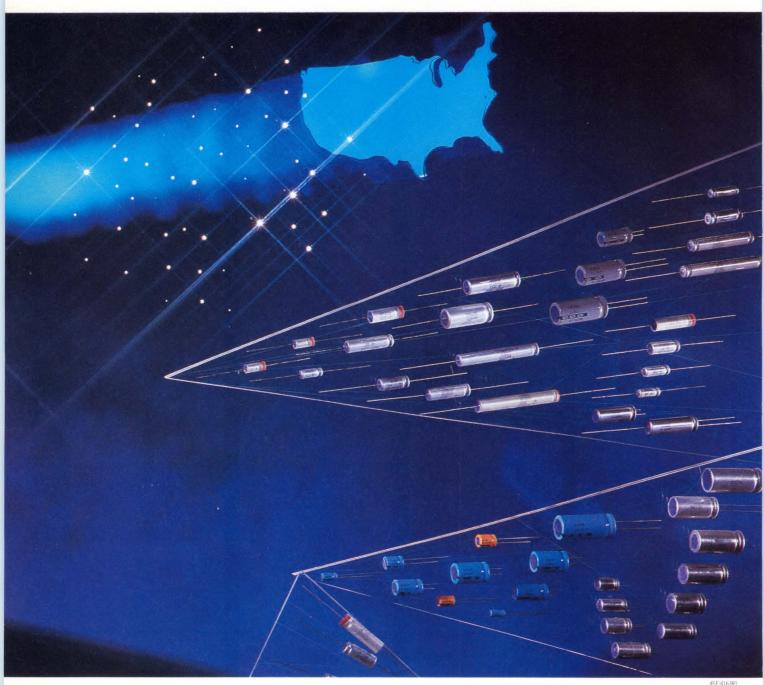


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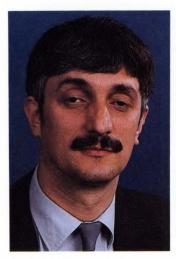
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CIRCLE 34

### VIEWPOINT

**EXCLUSIVE INTERVIEW** 

## How to avoid the pitfalls of surface mounting



David Topham

David Topham cofounded Cambridge Interconnection Technology Ltd. in England two years ago. The company is a surface-mounting technology consultant and subcontractor. Previously, he worked at **Newmarket Microsystems** Ltd. for eight years as a hybrid-circuit engineer. Topham received a degree from Cambridge University in natural and electrical sciences.

Excitement over surface-mounting technology (SMT) seems to know no bounds. Companies are rushing to follow the Japanese example in their conversion of assembly lines in the hope of saving money and improving system design. They consider the technique to be the ideal weapon to fight price competition, yet they ignore the drawbacks.

On the other hand, David Topham urges caution. After being involved with hybrid and surface mounting techniques for the past 10 years, Topham has observed the many mistakes of overzealous designers chasing the brass ring. "Many people see Japanese companies churning out high volume with surface mounting, and they think they should be doing the same," notes Topham. "They are tempted to invest in high-volume placement machines, but that could be a disaster."

Consider the different design and production requirements of a product as it matures. Surface mounting suits the limited volume of a new product expected to create a fresh demand. However, the equipment that handles relatively small runs today may be inappropriate for tomorrow's large volume.

Once the product is established in the market, it can be made more efficiently by integrating discrete functions into silicon. Thus, the final version of the product is more likely to have several high-pin-

Mitch Beedie

count chip carriers than many small DIP ICs, notes Topham. "Someone who invested too soon in expensive high-volume placement equipment may find himself with inflexible machines that are totally unsuited to his needs," he warns. "He would have been better off with smaller machines and robotic handling."

After deciding to convert to surface mounting, it is commonplace for manufacturers to try to recreate a product in the new environment. "People still try to fit existing products into a surface-mounted straightjacket," Topham says, incredulously. "For a start, not all components will come in surface mounted form." Indeed, components such as large transformers and pot cores do not lend themselves to the technology.

Topham urges that designers rethink the type of parts to be duplicated in surface mounting in the context of VLSI. He advises designers to "avoid transformers by turning to switching-mode power supplies and reject pot cores by using active filters instead of passive ones." The SMT conversion enables designers to take advantage of advances not only in VLSI techniques but also in packaging and production, he adds (see "Surface Mounting as a Halfway House," p. 68).

Furthermore, redesigning a product does not end with a net list of revised components on a CAD/CAM system. Topham warns that production practices

#### VIEWPOINT

and other subjects once dismissed as mundane or ignored entirely are vital to a successful conversion of surface mounting. For example, quality control must get renewed attention to to avoid a disaster when converting to SMT.

"Surface mounting forces us to do all those things we were always supposed to do but could usually ignore and get away with," Topham states. "It leaves much less room for error and doesn't allow us to be sloppy."

Incoming inspections must ensure that a vendor's components meet the specifications. Tape reels of components are of particular concern, Topham states, since it is not uncommon for a batch of incorrect devices to be added to the component feeder during tape loading. "Just testing the first few components on each tape will miss this mistake. You could end

up with boards using 100-nF capacitors where you had intended 10 nF."

The assembly process must also be thoroughly scrutinized. "Zero defects, with their attendant testing and inspection, are particularly important to

planning process for conversion to surface mounting. Even the choice of chip carrier technology is an important factor, though Topham believes it may have been overemphasized.

The debate over thermal mismatching, for example, was

#### 'Automated equipment can make products quickly, but it can also be a fast system for producing rejects.'

surface mounting. You are not only checking the finished product, you are monitoring the process itself," he notes. "Fast, automated equipment can make products very quickly, but unless you monitor the process, it can also be a fast system for producing rejects."

Consideration of VLSI design techniques and production procedures are only part of the

blown out of proportion, he explains. "The problem was caused by leadless ceramic chip carriers (LCCCs), which were mainly pushed by component manufacturers." LCCCs appeal to a manufacturer because the solder pads eliminate the materials and manufacturing costs and the handling problems associated with leads.

Unfortunately, users may not find LCCCs so attractive. "The lack of leads robs components of compliance and brings into play the different coefficients of expansion between ceramic material and standard epoxy resin pc boards," notes Topham. "That ruins reliability. An estimated 2 million man-hours were poured into trying to mount LCCCs reliably onto pc boards.

"The whole problem was unnecessary, in fact, since plastic leaded chip carriers do not give the same trouble," he states. As for hermetic sealing of components, ceramic leaded chip carriers fill the bill. Says Topham, a bit defiantly, "that is just what we should have had in the first place."□

#### Surface mounting as a halfway house

Hidden opportunities abound for designers considering surface mounting, asserts David Topham. Reducing manufacturing costs is just the first step. "Surface mounting should really be a halfway house to integrating a product in silicon," he says. That is, a host of advances in semiconductor technology is replacing discrete parts and improving reliability; increased integration, therefore, joins board fabrication economies in reducing the parts count as well

as manufacturing costs.

Furthermore, with surface mounting the equipment casing can support the electronics in some instances, saving the cost of a separate board, Topham explains. For example, assemblers can mount a touch-sensitive membrane keyboard onto a standard pc board with surface-mounted components on the back, he notes. Another trick is "to reduce equipment weight by making the substrate a structural member.'

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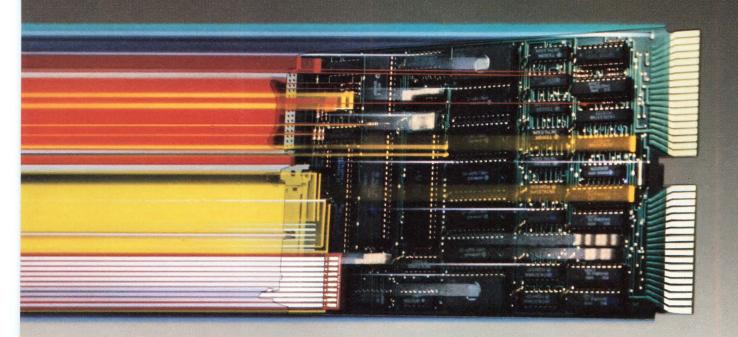
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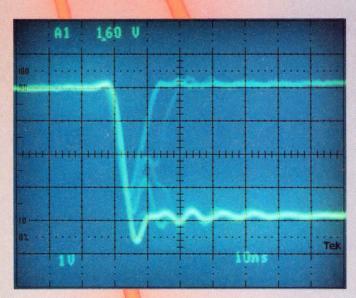
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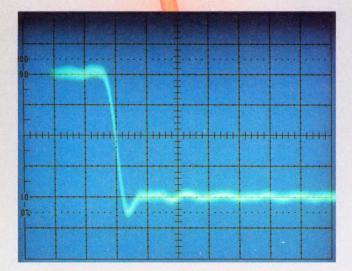
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# INDUSTRY NEWSMAKER

**ELECTRONIC DESIGN EXCLUSIVE** 

# PLD software takes on big-board projects

CAE software tracks, compiles, and simulates designs full of programmable logic. Any logic compiler or device technology can take part.

#### BY STEPHAN OHR

In the world of semicustom design, few applications use only one or two programmable logic devices. More likely, a Daisy Systems study reveals, design jobs call for hundreds of devices. That was the conclusion that prompted the company to add PLD design to its CAE system.

The PLDMaster brings design files to the workstation for an almost limitless list of PLDs, including the latest from Altera, Advanced Micro Devices, Cypress, Lattice Semiconductor, and Texas Instruments. With the software, you can enter logic in any form you want, compile the logic patterns or fuse maps in a convenient language, and then simulate the behavior of the device in situ. Once comfortable with the predicted performance, you can download the logic program into the device of your choice.

The system manages each PLD by its IC number rather than by its Unix path name, a convenient feature for hierarchical design. In fact, it is probably the most sophisticated setup of its kind, since it alone combines the top-down hierarchical philosophy with file-management tools and with interactive simulation. However, it still leaves the user free to choose devices, compilers, and programming inputs.

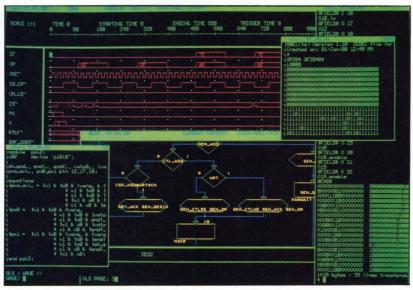
In its "mixed mode" environment, PLDMaster simulates an entire system by using a variety of component models—behavioral, hardware, gate-level, or even transistor-level—and making them all work together. Large-system design teams, in particular will appreciate the capabilities, since separate sections of their systems may be at different stages of the design process.

While the simulator runs in the background, the user manipulates the circuit inputs—say, for a state machine (Fig. 1)—in one window and displays the response waveforms in another window. At the same time, the multiwindow DNIX environment presents the compiler

source file (Abel is shown) and the programming logic (a JEDEC file) in two more windows. With this visual tracking, the user gets almost continuous feedback on the incircuit performance of his PLD.

In practice, a system containing a large number of PLDs would be designed in a hierarchical manner with several modules or boards. The engineer typically starts the design at the block level and works his way down to the component level at which PLD functions are defined. In Daisy's simulation environment, in contrast, many PLD functions can be tried out on the block level. As a result, you have the opportunity to modify, combine, or eliminate logic before blowing a single fuse.

Versatility also comes in the form of inputs the PLDMaster accepts. Daisy says it studied the general uses of PLDs and concluded that state machines constitute 30% of the applications, encoding-decoding functions slightly less than 30%, and glue logic under 10%. Whereas glue



1. The PLDMaster takes good advantage of Daisy's multiwindow DNIX environment. In the design of a state machine, for example, a state-machine flow chart appears in the center window while simulation results show up in the top window. The source file for high-level language compilers (Abel, here) is displayed at the left, with the compiled JEDEC file appearing in the upper right.



#### **INDUSTRY NEWSMAKER**

#### PLD programming software

logic can be described in schematic form, more demanding applications require a more direct means of logic entry: state-machine and high-level language descriptions.

With those findings taken into account, the PLDMaster is among the first to let programmers not only work from state-machine inputs—flow charts or tables—but also to enter a logic pattern as a schematic diagram (with patterns of gates) or a textual description written in a high-level language.

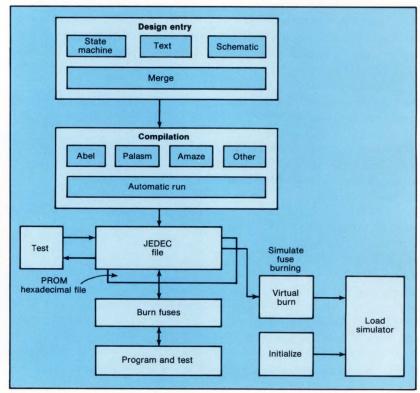
In addition, the PLDMaster supports a number of universal compilers—including Data I/O's Abel—as well as compilers dedicated to particular PLD types. Specific semiconductor compilers include Monolithic Memories' Palasm and Signetics' Amaze.

#### Price and availability

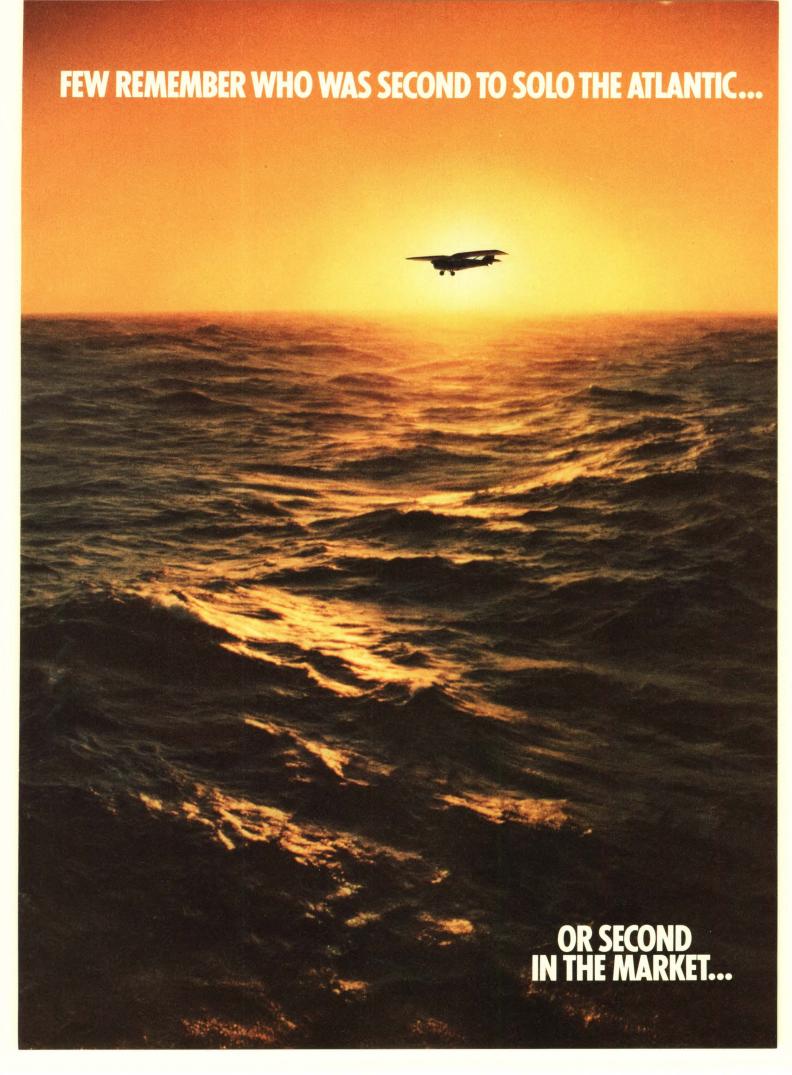
The PLDMaster, which goes for \$6500, is available as a software package for any Daisy hardware. Deliveries will begin in August.

Daisy Systems Corp., 700 Middlefield Rd., Mountain View, CA 94039; Pamela Lawrence, (415) 960-6593. CIRCLE 511

In the actual design flow, the compilers convert the state machine, schematic, or high-level language inputs into a JEDEC file that describes a target logic component and is used to program it (Fig. 2). The file feeds both a simulator and a PLD programmer machine. A byproduct, a test pattern, can be fed to an automatic tester. □



2. As a typical design progresses, the user can select his logic in any form and compile a JEDEC file with any compiler. The file flows into a simulator, as well as into a PLD programmer. The diagram is a facsimile of the PLDMaster's on-screen menu.



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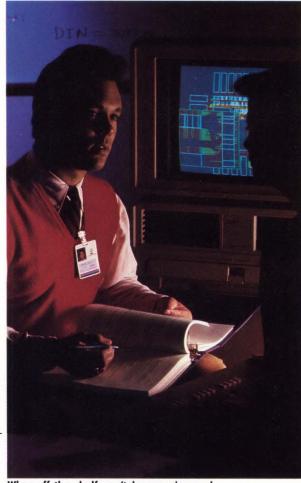
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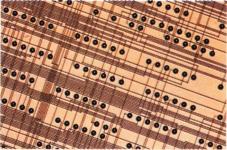
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**CIRCLE 40** 

#### INDUSTRY NEWSMAKER

**ELECTRONIC DESIGN EXCLUSIVE** 

### Preamplifier advances fiber-optic receivers

Priced under \$2, a low-noise 300-Mbaud IC heralds low-cost fiber-optic systems and other interesting applications, too.

#### BY ROGER ALLAN

Optical fiber has been widely promoted as a panacea for an assortment of communication problems. Yet despite its advantages, optical fiber has not proliferated in systems requiring wide bandwidths of 100 MHz and above. Why? Receiver components have simply cost too much.

The receiver cost problem is underscored by price reductions in transmitter components. Prices of popular light-emitting diode sources have dropped to about one-fourth of last year's levels. Yet on the receiver side, designers have been forced to limit the data rates to about 20 Mbaud to keep prices under, say, \$50.

The 5212 transimpedance amplifier IC changes that. The 5-V device, made from an oxide-isolated bipolar process, is optimized for fiber-optic receiver tasks; the part offers broad dynamic range, wide bandwidth, and low noise when operating at high data rates.

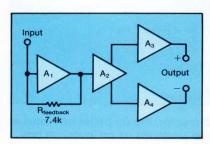
The alternative, a high-inputimpedance FET preamplifier, is more limited in bandwidth. Furthermore, FETs exhibit integrating characteristics that must be equalized by a differentiating second stage followed by an integrating stage, to achieve a broad frequency response. Moreover, the integrating stage is more overloaded by lowfrequency signals, compromising the amplifier's dynamic range.

The transimpedance amplifier's 60-dB dynamic range improves on that of available parts by about 20 dB. The 5212 handles input currents ranging from just above the noise level at 33 nA to a maximum of  $50 \mu A$ .

#### **WIDE 3-DB BANDWIDTH**

Another facet of the device's superior performance is its wide 3-dB bandwidth of 100 to 150 MHz for the 8-pin commercial version and 90 to 160 MHz for the 8-pin military version. For the 14-pin commercial ICs, the 3-dB bandwidth is 140 to 220 MHz; for the military version, 120 to 220 MHz.

Receiver noise performance is



1. With buffered differential outputs, the 5212 low-noise preamplifier, a four-stage transimpedance amplifier, achieves a high power-supply rejection ratio of 70 dB. The unit, designed for optical-fiber systems, interfaces easily with ECL circuitry.

particularly important, since most fiber-optic systems use noncoherent transmission. The receiver thus detects the total incident power, including noise.

The preamplifier's input stage achieves a respectable noise-current density of 3 pA/Hz<sup>1/2</sup> over the entire operating bandwidth of 10 kHz to 200 MHz. This represents an improvement of about an order of magnitude compared with the performance of existing parts.

The IC employs a single-ended signal input and differential outputs (Fig. 1). The differential output achieves a high power-supply rejection ratio of 70 dB and simplifies interfacing with ECL circuitry that follows the amplifier.

#### **CURRENT INPUT**

The 5212's high performance stems from the fact that it is a transimpedance amplifier; that is, it converts a current input into a voltage output. Thus, the IC's transfer function equals voltage divided by current with dimensions in ohms.

Since the input is current-driven, input resistance must be low  $(110\,\Omega)$  and input capacitance must be kept to a minimum  $(10\,pF)$ , thereby ensuring low input-voltage swings and consequently low output-voltage swings of just 3.2 V. The low input capacitance also reduces capacitive charge and discharge currents, contributing to the amplifier's wide frequency response.

The device consists of four amplifier stages. In the first, the single-ended input has an open-loop gain of about 70 and a feedback resistance of 7.4 k $\Omega$ . This leads to a second-stage differential amplifier and then to a pair of output emitter-followers. The last two stages have a voltage gain of about 2. The 5212 amplifier has an input-to-output transresistance, which equals its gain, of

#### Preamplifier IC

14.5 k $\Omega$ , about twice the value of the feedback resistance of the first stage.

Configuring the input stage with a cascode circuit would have achieved an even wider bandwidth, say the chip's designers. But a single-ended input enables the device to fend off external photodiode and stray capacitances. For example, a relatively high source capacitance of 4 pF reduces the amplifier's bandwidth only 30%.

#### **LESS NOISE**

Moreover, the transresistance of the amplifier ensures that the external high-value bias resistors often required for biasing avalanche and p-i-n photodiodes do not contribute to total system noise. Equivalent input rms noise current does not depend on the Miller effect of the input transistor. Therefore, input rms noise current is about 30 nA.

Package parasitics, particularly ground-lead inductances and capacitances, can significantly degrade a preamplifier's frequency response. To minimize parasitics, designers developed the 14-pin small-outline version in addition to the basic 8-pin small-outline package. The 14-pin unit's multiple grounds reduce equivalent lead inductance and thus give it a wider frequency response.

In either version, bandwidth can be modified by inserting a small capacitance between input and output or between input and ground of the preamplifier. In addition, the amplifier's differential output stage suits it for applications requiring both a peaking and notch-frequency response.

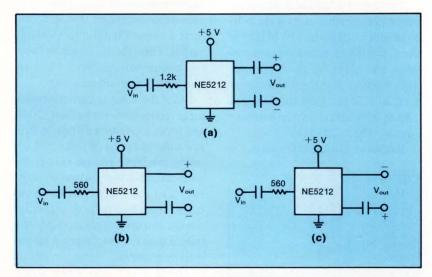
Besides operating in optical-fiber

receivers with high data rates, the IC applies to many other tasks too. For example, the part can be configured as a 20-dB gain amplifier by inserting a resistor in series with its input (Fig. 2). The amplifier performs in a differential manner; as a singleended output amplifier, the unit operates in an inverting and noninverting mode.

#### RESISTOR SETS GAIN

With no output load, the voltage gain of the differential amplifier can be set by the value of the input series resistor. The gain is the ratio of the amplifier's transresistance  $(14.5 \text{ k}\Omega)$  to the sum of the input resistance (110  $\Omega$ ) and the external gain-setting resistor. With a singleended configuration, about half the gain-setting resistor value achieves the same voltage gain.

As in all other rf applications, designers must pay attention to power supply bypassing, clean grounds, and minimum input stray capaci-



2. With the addition of a single input resistor, the amplifier operates in a differential manner (a). The unit also performs as an inverting amplifier (b) and in a noninverting mode (c).

#### Price and availability

The 5212 fiber-optic preamplifier is available in several packages for commercial, military, and automotive use. Commercial (0° to 70°C) and automotive 40° to +80°C) versions come in small-outline packages of 8 and 14 pins, as well as in 8-lead plastic DIPs. Military-grade parts (-55° to +125°C) are available in 20-pin leadless chip carriers and in 8-lead ceramic DIPs. Commercial-grade ICs in SO packages are available in sample quantities for about \$3 apiece. In lots of 1000, the parts sell for \$2 apiece. Samples of the military and automotive versions will be available by summer.

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CIRCLE 512

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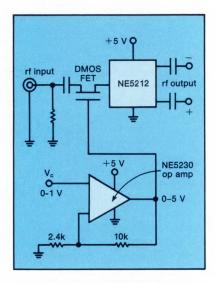
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#### INDUSTRY NEWSMAKER

#### Preamplifier IC



3. A voltage-controlled amplifier can be constructed around the IC by adding a few external components, including a DMOS FET and an op amp.

tance to obtain optimum perfor-

In yet another application, the 5212 performs as a voltage-controlled amplifier (Fig. 3), with the help of a DMOS FET biased in the linear region as the gain-setting resistor. An operational amplifier with a supply-to-ground output swing and a supply-to-ground input common-mode range (such as Signetics' NE5230 amplifier) can supply adequate gain-control voltage even with a single 5-V supply.

The circuit has a 25-dB control range at 50 MHz and a 45-dB control range at 10 MHz, with a harmonic content of less than 1%. The FET's on-resistance and the feedthrough capacitance of the drain to source terminals determine control

range. Placing the FET in a shunt configuration rather than in series minimizes rf feedthroughs.

#### AN OSCILLATOR, TOO

In addition, the 5212 amplifier's utility shines in a simple crystal oscillator with a buffered output. The 5212 amplifier, a crystal, and one 2-pF capacitor make up the oscillator. The positive output of the preamplifier's differential stage connects to one end of the crystal. With the capacitor in series, the crystal shunts the amplifier back to its input. The resulting 16-MHz oscillator has minimal components. Furthermore, the unit gives an independent output that can drive 50  $\Omega$ when the crystal operates in the series resonance mode.□

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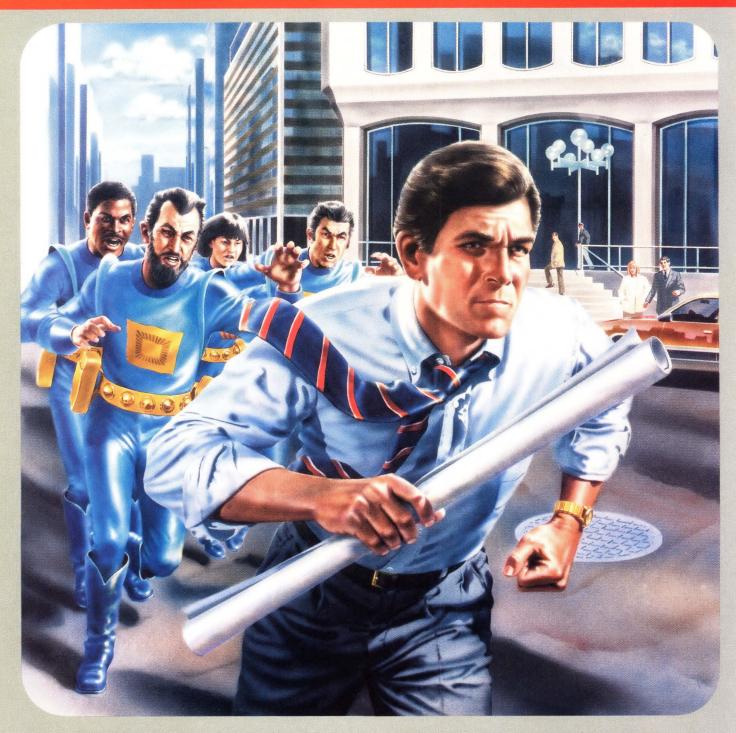
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#### INDUSTRY NEWSMAKER

ELECTRONIC DESIGN EXCLUSIVE

#### Wide output swings mark CMOS op amp

For the first time, a quad CMOS op amp gives designers superior dc and dynamic specifications with chips running off a 5-V rail.

#### BY FRANK GOODENOUGH

Beauty is in the eye of the beholder, they say. National Semiconductor's LMC660 quad op amp not only is the best-looking chip in some time, partly because of its symmetry, but it also sets a new level of performance at low cost. Unlike many quad op amps, the chip was obviously designed from scratch to hold four amplifiers (Fig. 1), and it offers many benefits beyond its low price -\$1.45 in quantities of 100.

The op amp serves up strong specifications with its jellybean cost:

- Its output swings rail to rail when driving a  $600-\Omega$  load.
- It operates from 3- to 16-V supplies.
- It exhibits an open-loop gain of 120 dB, a bias current of 40 fA, and a slewing rate of 1.7 V/ $\mu$ s.
- The chip's offset voltage falls under 2 mV.

The op amp, designed by Dennis Monticelli, National's group leader for industrial linear IC design, is available in commercial, automotive-industrial, and military versions. In addition, National guarantees vital specifications over each grade's operating temperature range (see the table, p. 92).

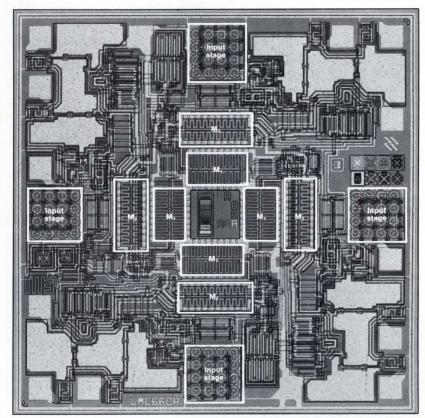
Monticelli's first goal was to achieve a rail-to-rail output swing. The op amp can run from any supply from 3 to 16 V. But if you put it to work in a digital system with only a 5-V bus, you probably would expect the chip to deliver a maximum output swing into a low impedance load.

Consider its operation under worst-case conditions-from 5 V with a maximum load,  $R_L$ , of 600  $\Omega$ and at  $-55^{\circ}$  or  $+125^{\circ}$ C. The chip swings its output at least 3.61 V, that is, from 0.63 to 4.24 V. Under a typical load of 2 k $\Omega$  and at a similar

voltage supply and temperature, the minimum swing exceeds 4.5 V.

The op amp's ability to operate on a low supply voltage puts it in the forefront of an industry trend. In fact, a panel session at this year's International Solid State Circuits Conference considered the ramifications of lowering the supply voltage for VLSI circuits from 5 to 3.3 V (ELECTRONIC DESIGN, March 20, p. 31). However, the panel and the audience predicted that when and if the reduction takes place, high-performance analog circuits, especially CMOS ICs, will be last in line. Ironically, one of the conference papers described the workings of this very CMOS quad

Though at present the chip's minimum operating voltage is specified

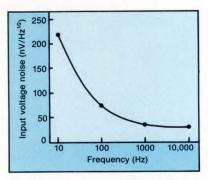


1. The symmetrical layout of National's LMC660 quad CMOS op amp ensures that the eight heat-producing, output transistors  $(M_1, M_2)$ create minimal offset-producing, thermal gradients across the four input stages.

#### Quad CMOS op amp

at 4.5 V, its designer says all chips he has seen will run off 3 V. Monticelli makes this statement based on his observation of chips from at least five wafer runs. Of course, the op amp slows down a bit when the power supply is changed from 5 to 3.3 V (as do digital VLSI circuits), but it meets most vital specifications at 3.3 V.

The chip's characteristics remain constant over this wide range of supply voltage range because its quiescent current remains virtually unchanged between 3 and 15 V. On the other hand, the quiescent current of some earlier single-supply op amps appears resistive, changing by up to a factor of two as the supply voltage varies. Such devices are often specified (and production-



2. Though the 1/f noise of the CMOS op amp is high, spot noise at 10 kHz is less than that of some bipolar parts such as the 324.

tested) at 10 V, although they are used in most tasks at 5 or 15 V, levels at which many important specifications may be quite different.

High performance at low voltage also lends the 660 to precision battery- or solar-cell-powered circuits. Though the chips are not power hogs, they do not aim at very low power jobs either; maximum quiescent current over the full temperature range is 2.9 mA.

#### WHAT ABOUT NOISE?

So far, the CMOS op amp looks appealing from all angles. But on the flip side, how is its input voltage noise? The answer is, not bad at all.

First, at 1 kHz, spot noise is typically 36 nV/Hz 1/2—which equals or surpasses that of other CMOS op amps. Moreover, at the chip's rather high 1/f corner frequency of 10 kHz, the voltage noise is about 20% less than at 1 kHz (Fig. 2). However, 1/f noise is severe, reaching  $250 \,\text{nV/Hz}^{1/2}$  at  $10 \,\text{Hz}$ .

On the other hand—and often more important—the chip's ultralow bias current (typically 40 fA) ensures virtually zero current noise, typically 2 fA/Hz<sup>1/2</sup>. Thus, in circuits with a source impedance of just a few thousand ohms, the op amp's combined current and voltage noise is less than that of other singlesupply op amps-notably the ubiq-

#### Price and availability

The LM660 op amp is available in 14-pin ceramic and plastic DIPs. In the future, it will appear in a narrowbody, small-outline package. In quantities of 100, the commercial-grade LM660C in a plastic package sells for \$1.45 apiece. Small quantities are available from stock.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051; Hugh Wright, (408) 721-5856. CIRCLE 513

uitous bipolar 324, which has a bias current of 45 nA. The 660's voltage noise at 1000 Hz resembles that of

The op amp's typical bias current is 40 fA, but the guaranteed maximum current is 2 pA—50 times that value. Why? With high-speed automatic handling and testing systems, it is impossible to measure 40 fA within 4 fA. Guaranteeing 40-fA maximum bias current requires more testing and could easily increase the cost of the chip tenfold.

#### YOUR CHIP OR MINE

If you are building mixed analogdigital chips in CMOS with standard cells or fully custom methods. the 660's capability is enticing. Today's typical semicustom CMOS op amp has a gain of 60 dB and an offset of 10 to 50 mV and some cannot even drive a resistive load (ELEC-TRONIC DESIGN, Jan. 9, p. 137).

However, the future holds some hope. The quad op amp, rather than being built with an exotic CMOS process for linear circuits, is fabricated with a 4-µm, silicon-gate pwell process designed for digital circuits. Thus, the 660 or similar parts could appear for custom or even semicustom designs.□

The LMC660 op amp's guaranteed specifications					
Specification	Military (-55° to +125°C)	Industrial (-40° to +85°C)	Commercial (0° to +70°C)		
Offset voltage (mV)	2.5	2.3	6.3		
Bias current (pA)	30	4	2		
Common-mode rejection ratio (dB)	70	70	62		
Large-signal voltage gain (dB) Sourcing/sinking at $R_L=2~k\Omega$ Sourcing/sinking at $R_L=600~\Omega$	109/97 103/96	113/101 107/96	109/98 103/92		
Total supply current (mA)	2.9	2.6	2.6		
Output current (mA) Sourcing, V <sub>OUT</sub> = 0 V at V = 5 V	12	14	11		



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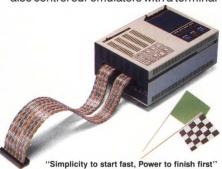
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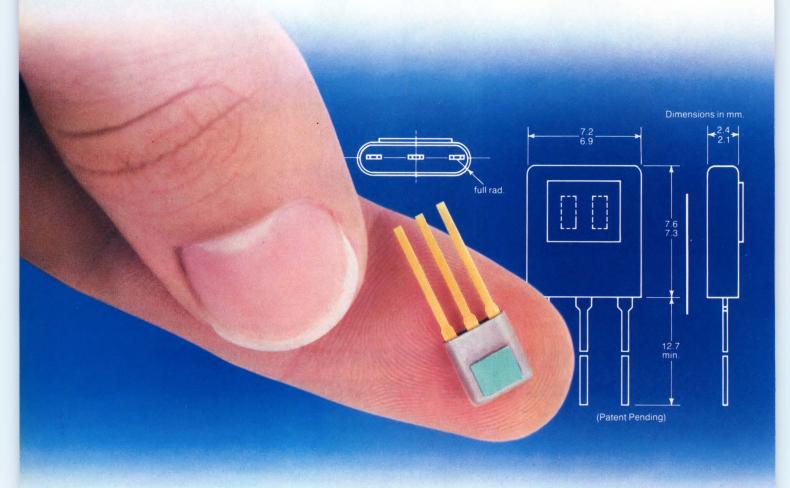
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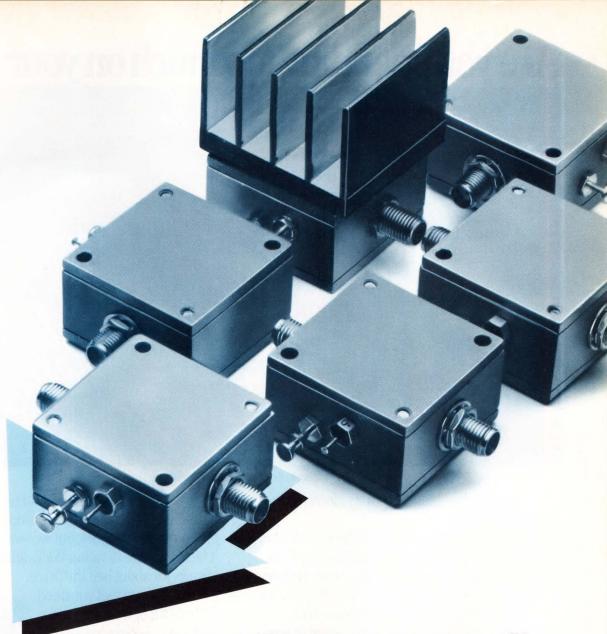
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CIRCLE 45





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Gain Flatness (dB) Max.	±1.0	±1.5	±1.5	±1.0
Max. Power (dBm)				
(1dB compression)	+10	+3	+17*	+20
NF (dB) typ.	5.3	12.0	7.0	5.0
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Intercept pt (dBm)	+18	+13	+25	+33
Current at 15V dc	80mA	90mA	100mA	150mA
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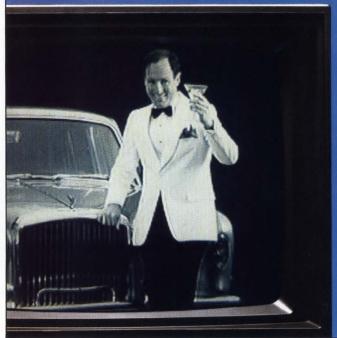
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**CIRCLE 46** 

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#### **NEWSTRENDS**

#### Isolation amplifiers get better as their sizes and costs shrink

With advances in packaging and transformer technologies, isolation amplifiers can tackle the most demanding applications.

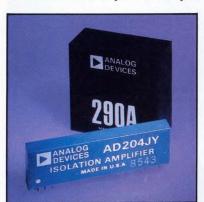
#### BY GENE HEFTMAN

Keeping the harsh electrical environment of the industrial and medical worlds from affecting the pristine sanctuaries of their sensitive computers and measuring instruments is the task of a hardy breed of devices known as isolation amplifiers. Designers have long used isolation amplifiers where low-level analog signals must be separated from high common-mode voltages and electrical noise or where ground-loop currents introduce unwanted errors in the signals being measured. Isolators have also served well as the first line of defense in protecting patients from dangerous voltages and currents generated by medical equipment.

These missions remain unchanged, but a new generation of isolators is arriving, bearing little resemblance to its forebears and offering designers high performance at relatively low cost. Amplifier manufacturers are improving packaging and magnetic components. And they are building-in greater resolution and linearity to make performance compatible with the analogto-digital converters and computer systems to which isolators are increasingly feeding data.

Meanwhile, some isolation amplifiers are headed toward gaining the status of building-block or commodity components rather than highly specialized, design-intensive

parts. In the past, many users built their own isolators to obtain a mix of cost, size, and performance that was unavailable from manufacturers. But with new construction techniques, manufacturers can now turn out drastically slimmed-down versions of the well-known bricklike modules that were mainstays for many years. The new devices, including a rapidly emerging class of hybrids, deliver reasonably high accuracy and isolation voltage and are much less expensive than modules. Modules, however, are far from dead and remain important compo-



1. The shrinking size of the isolation amplifier is apparent in a comparison of Analog Devices' new single in-line package AD204 and its 5-year-old modular 290A. The use of surfacemounted chips and smaller transformers are two factors behind the growing popularity of these low-cost isolators.

nents in uses demanding premium specifications.

The AD202 and AD204 single inline packages (SIPs) from Analog Devices (Fig. 1) exemplify the direction in which isolation amplifiers are moving. Because the parts are just 0.25 in. wide, a designer can cram four channels of isolation into 1 in. of board space. Each small, narrow package is made possible by a new circuit design, a novel but proprietary transformer construction, and the use of surface-mounted components on the device's internal printed circuit board. A dual in-line package (DIP) version boasting twice the isolation voltage of the SIPs-1500 V vs 750 V—is due out this spring.

Although transformer coupling is by far the most common isolation technique used in amplifiers, the marriage of magnetic components to the hybrid circuits used in many isolators is not exactly a match made in heaven. In fact, hybrid circuits incorporating transformers and chokes are usually very difficult and costly to manufacture because of problems with magnetic-component size, uneven mounting surfaces, and substrate-to-magnetwire interconnections.

When Burr-Brown decided to enter the hybrid isolation-amplifier market, it knew that it had to develop a better way to mount a toroidal transformer on a hybrid substrate. The result is a hybridcompatible transformer design that the company employs in its Model 3656 isolation amplifier (Fig. 2). Rather than winding the transformer with conventional magnet

#### **Isolation** amplifiers

wire, the hybrid-compatible design breaks the windings into two parts. Half of each turn is printed onto the ceramic substrate as a pattern of gold conductors. The radial pattern of printed wiring is covered with a layer of glass, except for its outermost edges, and the toroidal core is mounted onto it. Conventional gold bonding wire completes the transformer turns. This transformer construction produces a hybrid isolation amplifier, measuring only 1.1 by 1.1 by 0.26 in., that offers both signal and power-supply isolation.

#### THE CASE FOR HYBRIDS

Now, such hybrids represent the wave of the future in isolator technology, since they are generally less expensive and smaller than modules, but offer comparable performance.

Burr-Brown's 3656 and Analog Devices' AD295 use similar pulsewidth-modulation techniques to transfer signals and power across the isolation barrier (Fig. 3). The

3656 is designed around the single multiple-winding, hybrid-compatible transformer, which also furnishes three-port isolation. Both devices can be had in different grades depending on the linearity accuracy required. The AD295 contains two internal transformers to provide its three-port (input, output, and power-supply) isolation.

The 3656's nonlinearity specifications range from  $\pm 0.15\%$  down to  $\pm 0.05\%$  while gain drift with temperature can be as low as 60 ppm/°C. All versions offer a dc isolation voltage of 3.5 kV and an ac isolation voltage of 2 kV. Because the 3656's internal switching rate is 750 kHz, it can operate over a 3-dB small-signal bandwidth of 30 kHz -unusually high for a transformercoupled isolator.

With the AD295, designers can choose from among nonlinearity grades A, B, and C. The leastaccurate A grade is a respectable  $\pm 0.05\%$  while the C grade is specified for ±0.012% maximum nonlinearity. Isolation voltage is rated at ± 2.5 kV peak, ac or dc. The AD295's internal oscillator runs at 80 kHz, giving it a typical bandwidth of 4.5 kHz.

#### THE ISOLATOR SPECTRUM

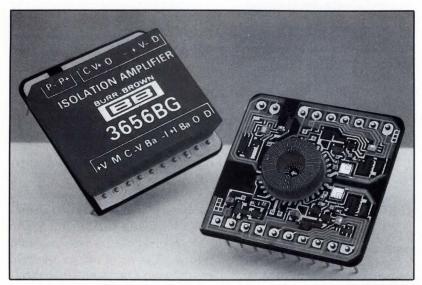
All isolation-amplifier manufacturers agree on three application areas for the devices: industrial, instrumentation, and medical. The industrial world requires isolators that yield accurate signal amplification, reject common-mode voltages and noise, and eliminate ground loops.

Since industrial and instrumentation systems involve numerous transducers and multichannel data acquisition, designers need isolators that are inexpensive, can be packed tightly on pc boards, and provide good signal-processing accuracy.

As indicated earlier, Analog Devices' AD202 and AD204 SIPs represent the leading edge of packaging technology for multichannel industrial applications. But the parts also offer good specifications for a range of industrial uses: ± 1000 V continuous common-mode isolation, ± 0.05% maximum nonlinearity, 130-dB common-mode rejection (CMR), and a full-power bandwidth of 5 kHz. The prices—\$28 for the AD202 and \$25 for the AD204 in 100-piece quantities-make the devices attractive for multichannel systems.

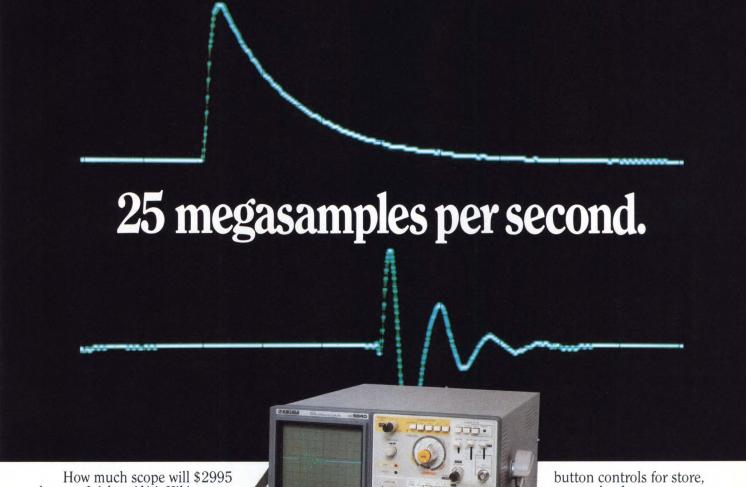
Amplifying microvolt-level signals in data acquisition is the forte of Datel's AM-227 isolation amplifier. Analogic makes an almost identical isolator called the MP227A, thereby giving designers the assurance of multiple sources. At gains between 50 and 500, the AM-227's nonlinearity is specified at  $\pm 0.005\%$ while the MP227A's is rated at  $\pm 0.0075\%$ .

Both devices typically offer a common-mode isolation voltage of



2. A miniature multiturn toroidal transformer, with turns made of gold rather than conventional magnet wire, holds center court in Burr-Brown's 3656 hybrid isolation amplifier. Gold wires from the transformer are bonded to a screened gold interconnection pattern on the ceramic substrate.

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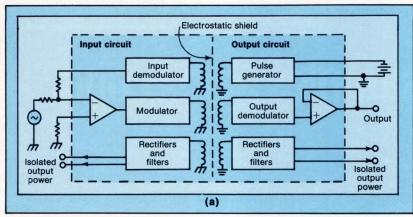
#### Isolation amplifiers

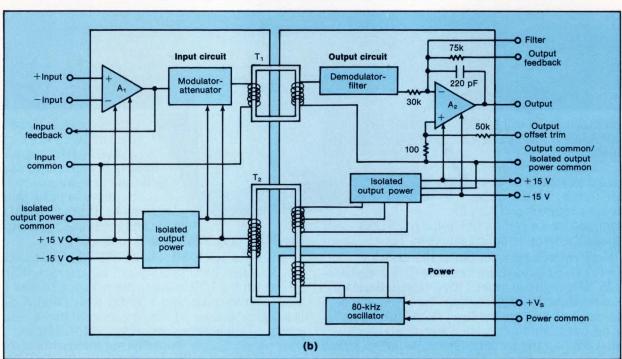
1000 V dc (750 V rms) and a CMR of 176 dB. The parts are designed with the same chopper-stabilized techniques used in the highest precision operational amplifier designs. Both contain an internal power oscillator and isolated power supply, so no external drivers are needed.

While instrumentation or dataacquisition applications may not involve the high-voltage hazards of the industrial world, they generally need a higher order of accuracy. A 12-bit system, for example, must be accurate to about 0.01%. Not only must an isolator afford considerable front-end linearity, it also must be able to reject common-mode interference and to break ground loops. Interference and ground loops can

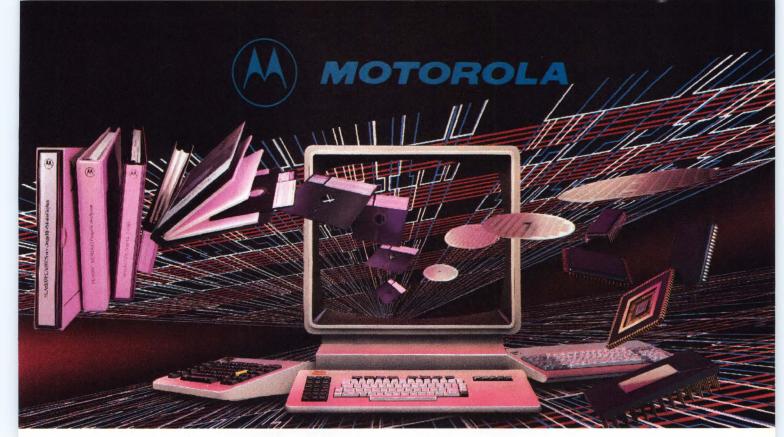
lead to unacceptable errors in 12-bit measurements. Because of its CMR and galvanic isolation features, an isolator is better equipped for data acquisition than an instrumentation amplifier.

Although SIPs, DIPs, and hybrids are becoming more common forms of the isolation amplifier, the tightest linearity specifications and highest isolation voltages usually go to modules. Because of their larger size, they can withstand higher breakdown voltages than can other types of isolators. Intronics, for example, designed its IA175 transformer-coupled amplifier to operate at continuous de common-mode input voltages as high as  $\pm 5$  kV, and ac common-mode voltages up to 3 kV. At the same time, the device is highly linear, offering maximum nonlinearity specifications of  $\pm 0.01\%$  and  $\pm 0.02\%$  for  $\pm 5-V$ 





3. Two transformer-coupled hybrid isolators—the 3656 from Burr-Brown (a) and the AD295 from Analog Devices (b)—share similar designs. Both are three-port isolators using a type of pulse modulation to get signals and power across the isolation barrier. And both employ novel but different transformer designs to obtain high isolation voltages in a smaller-than-usual package.



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#### **Isolation** amplifiers

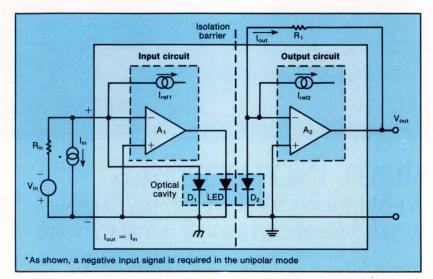
and ±10-V output swings, respectively. These ratings make the IA175 suitable for 12-bit data acquisitions.

Medical isolation amplifiers exist mainly to protect patients from leakage currents and to protect other medical equipment from the extremely high defibrillation pulses —up to 5 kV—generated by resuscitation equipment. At 120 V ac, a ground-fault current as low as 10 μA can be lethal to a patient. On the other hand, if an electrocardiograph is damaged or destroyed by a high-voltage pulse, it could lose

its effectiveness in monitoring the patient's vital signs. Medical isolators must provide good noise rejection, since signal levels as low as 0.5 V are sometimes measured in the presence of high noise levels.

Medical equipment designers needing an isolator that can withstand the high-voltage pulses of defibrillators will find it in the Intronics IA294. The 2-by-3-in. module provides  $\pm 6.5$ -kV isolation from input to output, as well as  $\pm 6.5$ -kV differential-input protection. Input-tooutput leakage current is typically less than 10  $\mu$ A, and the input circuit incorporates a fail-safe design. For signal handling, the IA294 incorporates a true instrumentation front-end featuring a CMR of up to 126 dB and so-called active right-leg drive. The latter is important in multilead electrocardiography for improving the CMR between the amplifier's input and isolated common terminals. With an active drive, any common-mode voltage appearing between the two terminals is driven to zero.

A comparable amplifier for the



4. An LED and photodiode D<sub>2</sub> form the isolation barrier of an optically coupled isolation amplifier from Burr-Brown. Feedback through photodiode D<sub>1</sub> improves the amplifier's linearity. Essentially, the optical isolator is a 1:1 current translator, since current on the input side of the isolation barrier is the same as that on the output side.

Company		Transformer-coupled			Optically coupled		
	Industrial	Instrumentation	Medical	Industrial	Instrumentation	Medical	Circle
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Note: This is a representative sampling of manufacturers and parts; it is not meant to be a definitive list.



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#### **NEWSTRENDS**

#### Isolation amplifiers

same medical applications is Analog Devices' AD286J. Also capable of withstanding 6.5 kV, the module supplies an input-to-output CMR of 114 dB. For patient protection, maximum leakage current is held to 2.5  $\mu$ A rms. The AD286J's gain stage has a maximum nonlinearity of  $\pm 0.2\%$  and a maximum temperature drift—gain drift with temperature—of just 100 ppm/°C.

#### THE OPTO NICHE

Isolation amplifiers generally use transformer coupling to form an isolation barrier. Burr-Brown, however, relies on an optical isolator to isolate its input and output stages. The optical isolator contains a cavity in which an LED and a pair of matched photodiodes are mounted. One photodiode is connected to the

input stage to improve linearity; the other is in the output stage, where its only connection to the input is through the light generated by the LED. An optocoupled device is essentially a 1:1 current transformer on the input side and a current-to-voltage converter on the output side (Fig. 4). Current produced on the input side is duplicated on the other side of the isolation barrier.

Because optical coupling provides wider bandwidth than with transformer coupling, optical isolators are better suited to high-speed switching inputs. The isolators shine especially bright in systems in which bandwidth and response speed are more important than gain accuracy and linearity. For the latter parameters, the transformer-coupled type is preferred.

Designers who want optically coupled isolators can narrow their choices to Burr-Brown's ISO100 or 3650 and 3652. The ISO100 is a miniaturized device rated for 750-V continuous isolation voltage and a very wide 60-kHz bandwidth. Nonlinearity is typically 0.07% for the highest of the three grades offered. The 3650 and 3652 optical isolators yield lower bandwidth but greater isolation voltage. The devices are rated for a 3-dB small-signal bandwidth of 15 kHz, while the continuous isolation voltage is 2000 V peak or dc. Their higher isolation voltages require a larger package size—a hybrid—than for the ISO100. Nonlinearity specifications are also better than the ISO100, a maximum of 0.05% for the best of the five different grades.



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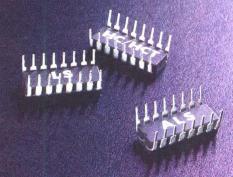


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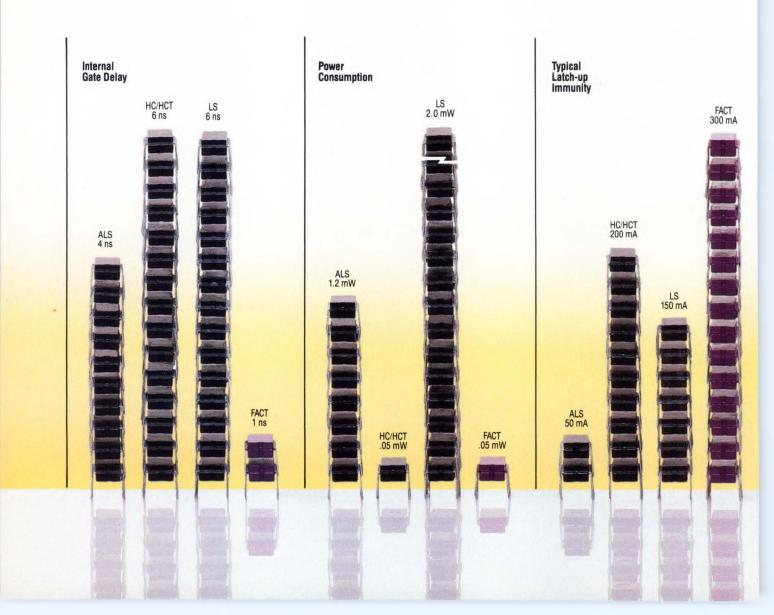
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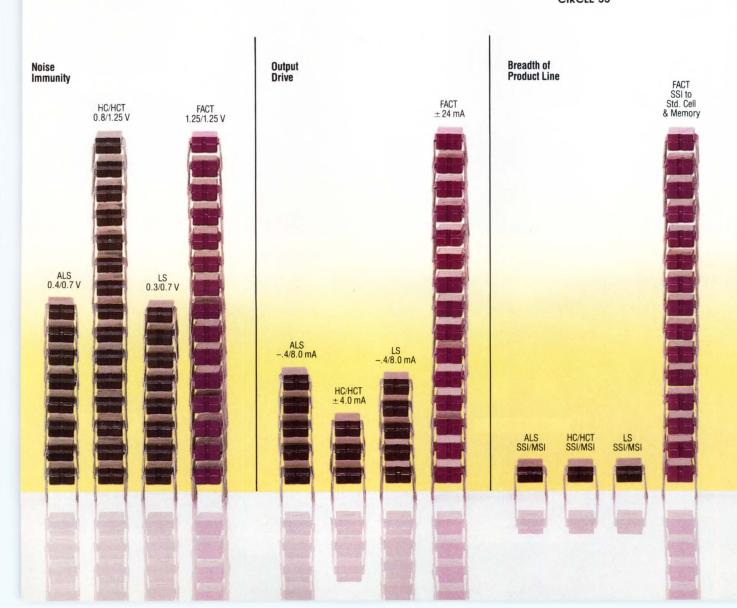
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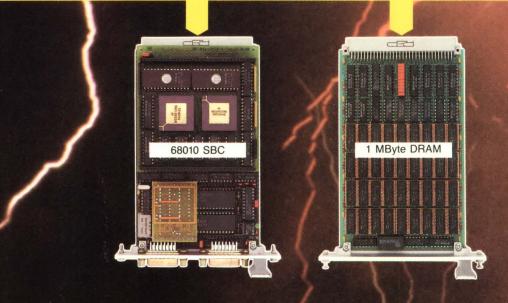
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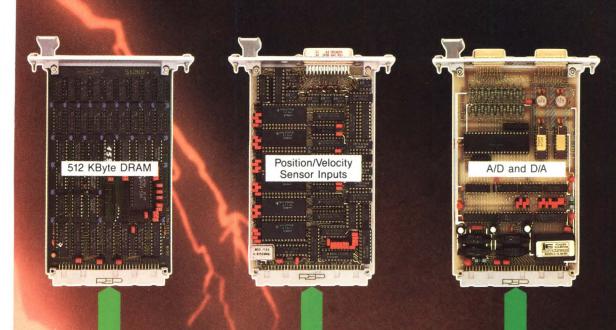




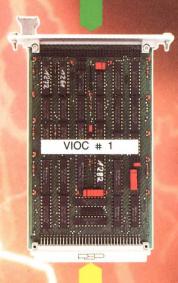
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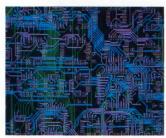
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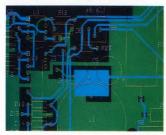
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**CIRCLE 55** 

# Electro/8

About 50,000 engineers and professionals will descend on Boston later this month, when Electro/86 unfolds May 13-15 at the Bayside Exposition Center and the new World Trade Center. Besides more than 1300 exhibits, the technical program should catch, and keep, the interest of engineers and industry managers.

Of the 27 technical sessions planned, 8 will devote themselves to semicustom and custom design techniques. Scheduled papers will cover trends in application-specific ICs, choosing design centers, and the latest advances in standard cells, silicon compilers, and programmable logic. Talks are also slated for packaging technologies, power ICs, fault simulation, and testability analysis. A session on the Strategic Defense Initiative will more than likely interest everyone, as will discussions on engineering education and the whys and wherefores of technology transfers.

Once again, Mini/Micro Northeast will pair up with Electro. It encompasses 173 exhibitors and has its own technical program of 27 sessions. Both gatherings will afford the first look at a host of new products, ranging from analog-to-digital converters to integrated calibration systems and highly efficient switching power supplies. A preview of some high points in Electro's technical sessions follows, and our customary look at some of the conference's most exciting products begins on p. 129.

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## Electro/8

#### ASIC issues—design centers and semicustom techniquesheat up Electro/86 program

The immense interest in application-specific ICs is prompting a flurry of questions, particularly from engineers at system houses. On one hand, they must evaluate and ultimately choose a design center; on the other, they must balance the advantages and drawbacks of the various semicustom design techniques, including silicon compilation. A good choice can help guarantee success; a poor one may doom a project to failure.

So critical are the decisions that ASIC houses and design techniques appear high on the technical agenda at Electro/86. Like Southcon/86 earlier this year, the technical sessions will explain the many mysteries underlying this new generation of semicustom technology. Engineers will examine the tradeoffs in design centers run by chip makers, industrial distributors, independent third parties, or even their own companies.

Apart from design centers, different ASIC methods are vying for the designer's attention. The familiar gate arrays and standard cells now face stiff competition from macrocells, silicon compilers, and programmable logic devices. Designers need to develop a feel for each one's turnaround, modification costs, and performance.

Those issues dominate the technical sessions, but they are by no means all that Electro holds in store. Filling the agenda will be surface mounting (see "Solderability Issues Surface," p. 118), high-performance interconnection technologies (like tape-automated bonding), and progress in ECL and power ICs.

#### **CAREFUL SELECTION**

Choosing an ASIC design center should not be an afterthought. "The selection should not be based simply on economics; it should be based on a number of factors critical to the customer's needs," says Mel Kutzin, director of semicustom services at industrial distributor Arrow Electronics (Melville, N.Y.). Whether a designer goes with custom or semicustom systems, Kutzin identifies several constants, namely, the technologies a design house offers, the amount of technical assistance given, the equipment available, turnaround, and alternative sources.

Though the considerations may

#### Martin Gold



seem obvious on paper, rarely are they given the proper study. Kutzin warns engineers to make sure that the design center can indeed handle the chosen technology. For instance, does the prospective design house specialize in gate arrays, standard cells, or both; in digital, analog, or mixed digital-analog circuitry; and in bipolar or MOS. If it works with MOS, is the process n channel, p channel, or CMOS; one metal layer or more; channeled or channelless; 5 or 15 V?

Even technical assistance is not clear-cut: Does the design center really assist and support the engineer, or does it simply supply a workstation operator for the customer? Nor should designers underestimate the importance of the computers and workstations being used. And what level of confidence does the design center inspire in delivering an ASIC that meets expectations? Moreover, how long does it need to convert a customer's design into working silicon—that is, the ASIC hardware—and after that, how many can it turn out?

Methods and assistance aside, modification costs are extremely important. Kutzin explains: "Sometimes a design does not meet the company's actual needs and has to be modified. Should that happen, many customers don't want to incur the costs of a completely new design, especially when the modification may simply entail a few more gates or another I/O connection." If the design center or its approved supplier has caused an error, Kutzin maintains that customers should not be charged for the modifications that would bring the device up to the agreed-on specifications.

The CAE industry is also getting

into the act, not just through design centers but more recently through tools that let engineers design circuits in-house.

These workstation-based design kits are assembled jointly by a CAE company and an ASIC vendor, so that their mutual customers can glean the best design possible. Essentially the CAE company lends its expertise in implementing a design technique and the integrated circuit vendor in guaranteeing the design data.

#### COMPLETE CONTROL

CAE leader Mentor Graphics Corp. (San Jose, Calif.) is one participant in the kit business. Says its semicustom product manager, Lisa Hampton, "The design kit offers a dependable way (for engineers) to learn a new design method. With it, the task is left completely to the de-

#### Solderability issues surface

surface-mounted devices onto a board? Looking at this year's Electro program, a lot of work is going into finding the answer. Two companies, National Semiconductor Corp. (Santa Clara, Calif.) and Hewlett-Packard Co., share their experiences.

To National Semiconductor's Robert J. Walker, marketing manager for surface-mounted devices, part of the solution may lie in an innovative lead-frame package with perforated leads. In developing it, the company also proved that vaporphase reflow soldering does not degrade semiconductor reliability as much as wave soldering does.

Dipping a semiconductor component into a hot solder bath, as done with wave soldering, can substantially damage a part, says Walker. In fact, the effects are reminiscent of the "purple plague," a result of chip contamination that caused major device failure in the 1960s. When a standard small-outline package is

materials expand at different rates, stressing and cracking the interface and giving moisture a clear path to the chip. With the lead-frame package, National seems to have solved the problem, explains Walker. Holes in each lead act as a barrier that retards moisture ingress.

A series of tests helped National compare the reliability of its package with that of the standard smalloutline package. Among 30 standard packages, 7 failed after vapor-phase soldering and 11 after wave soldering. In sharp contrast, Walker reports, the perforated lead frame incurred no failures after either soldering method.

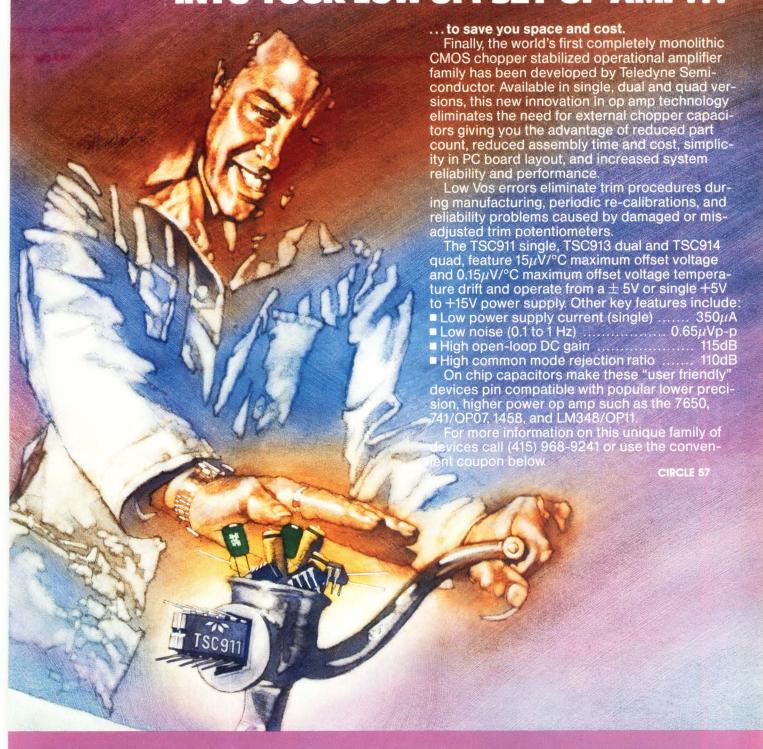
Two Hewlett-Packard engineers-Bert Anderson from the plant in Andover, Mass., and Stephen Hinch from the facility in Rohnert, Calif.—focus on a dilemma facing users of surface-mounted components. Although the job would be easier if soldering requirements

What's the best way to solder immersed in the solder, its composite could be specified as a total interconnection system-board, component, solder—no overall solderability test exists. Thus the HP specification they describe covers only the solderability of the component leads. Anderson and Hinch cite HP's salient specifications:

- Component terminations must be solder-coated with a tin-lead alloy containing 60% to 63% tin.
- The tin-lead finish must be at least 300 µin. thick.
- · Solder finishes applied over precious metal electrodes, such as the palladium-silver found on ceramic capacitors, must have a nickel diffusion barrier at least 50 µin. thick.

Both men note that during vaporphase reflow soldering, a component can experience a severe temperature gradient. After considerable discussion with component suppliers, they conclude that preheating the part at 80°C to 100°C for at least 30 seconds can prevent component damage due to thermal shock.

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signer, who now has control over the entire process, over his schedules, and over the data that allows him to experiment and produce a better design."

According to Hampton, a design kit usually takes anywhere from six to nine months to complete, with the time divided among entering and verifying data, customizing programs, trying out program options, setting up documentation, and fully testing the system. Once the kit is complete, the semicustom IC vendor maintains and distributes it.

Some design kits reach beyond data and programs to documentation and tutorial information. Mentor, for one, gives the IC vendor a generic design manual that details how to execute the design steps on a specific workstation. Then the two companies cooperate on modifying the manual for the kit's technology.

Consider the worldwide design

centers of chip maker Texas Instruments Inc. (Dallas). Its seven design centers in the U.S.—as well as others in Japan, Europe, and Canada currently implement circuits based on gate arrays and standard cells.

#### **ETHERNET CONNECTIONS**

Right now TI is upgrading its U.S. design centers, expanding the CAE hardware and connecting all equipment through the Ethernet local network (see the figure). Daisy Megalogician workstations will be installed for system simulation and Daisy Gatemaster computers for functional design, logic capture, logic simulation, and delay calculation.

In addition, designers will have access to Apollo computers fitted with Mentor software, which will take care of automatic layout and test-vector grading. Rounding out the hardware are Texas Instruments

personal computers, which simulate and capture logic and grade test

The centers use model libraries developed, distributed, and supported by TI for several commercial workstations—for logic capture and simulation of gate-array and standard-cell circuits. According to Herman W. van Beek, department manager for ASIC design support, this year TI plans to significantly increase the number of model libraries. "To make that happen," he stresses, "the model libraries must be converted to the Electronic Design Interchange Format (EDIF)."

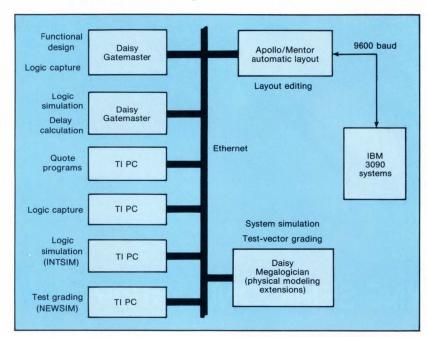
In the hands of a silicon vendor, an EDIF library can make the support of model libraries far more effective. "In the present environment, upgrades in engineering workstation software often render a part-model library obsolete overnight. Having an EDIF data base makes it much more practical to stay abreast of system upgrades," van Beek notes.

Quarterly updates add new features to the libraries and correct any errors that may have escaped quality control. Yet if a workstation vendor changes the operating system or application software in a way that necessitates an overhaul of the library, TI will issue a new library.

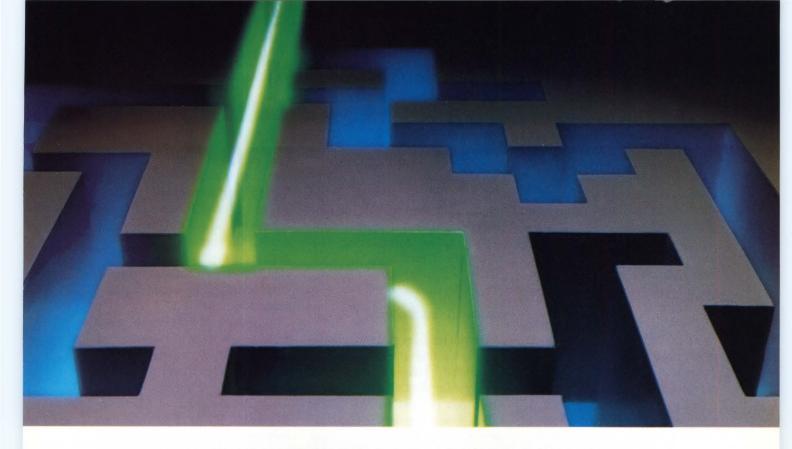
#### STRIKING A DESIGN BALANCE

Clearly trade-offs abound in selecting a design center. But Martin H. Malecki, strategic marketing manager for Gould AMI Semiconductors (Santa Clara, Calif.), warns that the task is further complicated by trade-offs in semicustom design techniques: gate arrays, standard cells, macrocells, or even silicon compilers.

Quick development is the biggest advantage that gate arrays enjoy over the other semicustom techniques, says Malecki. But their fixed



Texas Instruments is upgrading its regional design centers this year. For the first time, all CAE hardware will be linked through the Ethernet network. To improve design support, TI is adding the Daisy Megalogician and physical modeling extensions for system simulation and test-vector grading.



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architecture limits designers' flexibility and puts production prices slightly higher than for an equivalent circuit based on standard cells or macrocells.

Standard cells fare slightly better than gate arrays. On the plus side, they offer more design flexibility, greater performance, and more analog and digital capabilities—all for a good unit price. On the minus side, each standard cell requires a unique set of masks, a fact that lengthens development time and raises development costs.

The trade-offs continue. Though standard cells take longer to create than gate arrays, they nevertheless can be developed more quickly and at less expense than optimized macrocell-based circuits. Moreover, they boast a greater chance of firsttime success. In exchange, however, standard-cell-based circuits carry a higher production price tag than do comparable optimized cell-based circuits.

Undeniably, silicon compilation has become an important part of the design picture too. Malecki says that silicon compilation gives the designer leeway in adjusting an IC's performance without imposing the time, expense, or risk penalties normally associated with fully custom designs. Electro will have several talks on silicon compilation. The presentations, most being tutorial in nature, will largely cover the types of compilers now available.

#### STANDARD-CELL SPECIFICS

Overall progress in standard cells gets the nod from Intel Corp.'s Matt Townsend, technical marketing manager for the Cellular Products Operation (Chandler, Ariz.). His talk is billed as a way to clean up microcontroller-based designs using standard cells. More important, it gives some insight into Intel's standard-cell strategy and comments on a very important ASIC trend: using a microcontroller core as a building block for complex cell-based chips.

As a case in point, Townsend relates the conversion of the 80C51, a popular 8-bit controller, into the UC51 core cell, which is about to be released. The standard-cell approach eliminates much of the support logic associated with the standard microcontroller. For example, assume that an 80C51 needs an extra 16 inputs and outputs—the equivalent of about 300 gates of glue logic. Ordinarily, designers might commit the glue logic to a separate gate array or standard cell, a plan that increases pin count, complicates board wiring, and ultimately raises design costs.

Cells like the UC51 can be modeled in several ways, explains Townsend. The most straightforward method involves modeling them as transistors or simple gates, but a software subroutine that behaves like the UC51 is more powerful. The subroutine becomes a behavioral description of the cell and works much like gate primitives do within Intel's iCEL design system simulator.

In fact, Intel plans to introduce a behavioral model for the UC51 that would contain as many as 6000 gates. Especially noteworthy, the model renders UC51 simulation several orders of magnitude faster than a gate-level run. As a result, the simulator can spend most of its time on user-defined logic.

An Intel-generated test program derived directly from the standard microcontroller can test the UC51 completely. As for the application logic, it can be evaluated by using the model and an extended version of the ASM51 assembler. The special assembly language enables designers to associate 80C51 and UC51 instructions with external stimuli in a source-level test program.

#### PLDs: NOT TO BE FORGOTTEN

No discussion of ASIC technology would be complete without programmable logic devices: fusebased PLDs, such as the wellestablished PLAs and Monolithic Memories' PAL devices: electrically erasable PLDs; and programmable

Comparing ASIC techniques						
Feature	Fuse PLDs (PALs/PLAs)	Erasable PLDs	In-circuit reprogrammable logic devices	Gate array		
Maximum logic capacity (equivalent usable gates)	100-300	100-400	1000-1500	1000-10,000		
Nonrecurring engineering costs	None	None	None	Very high		
Device costs (1200-gate application)	High	Moderate	Low	Very low		
Design cycle time	Days	Days	Days	Months		
Redesign cycle time	Minutes	Minutes	Minutes	Months		
Field-programmable Reprogrammable Programming losses	Yes No Moderate	Yes Yes Low	Yes Yes None	No No Not applicable		
Architecture	Fixed	Fixed	Flexible	Very flexible		
100% tested	No	No	Yes	Seldom		
Simulation	Optional	Optional	Optional	Required		
Design risk	Low	Low	Low	High		
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CUPL is the most powerful high-level design language for PLD's. It incorporates features like macro substitution, free-form comments, indexed variables and parenthetical capability, to speed

program development.

CUPL provides superior state machine capability, and supports all popular models of logic description, including truth tables and

high-level equations. CUPL's logic minimizers (3

are supplied), and deMorgan expansion capability are unequalled.

And CUPL's documentation out-

CIRCLE 60

put file gives you invaluable feedback on your design's progress. These features, plus continual enhancements, make CUPL the benchmark in PLD design languages—flexible and powerful enough for the most sophisticated logic designer's needs.

Call P-CAD's Assisted Technology Division now for additional information, at (800) 523-5207. (In CA: (800) 628-8748.) Or write: Personal CAD Systems, Inc., 1290 Parkmoor Ave., San Jose, CA 95126. TELEX: 278866.

Because getting held up in customs can be an unsettling experience.

### CUPL. THAT'S THE BENCHMARK.

From the Assisted Technology Division



THE BENCHMARK



gate arrays (see the table, p. 122). Add to those a new type, the incircuit reprogrammable logic device developed by Xilinx Inc. (San Jose).

Combining the convenience of PLDs with the flexibility and capacity of small gate arrays, the incircuit device substitutes CMOS static RAM cells for the traditional fuses or dedicated IC mask techniques (ELECTRONIC DESIGN, Oct. 31, 1985, p. 123). As a result, devices can be programmed in the field or configured in the application circuit.

Steve Landry, technical marketing engineer at Xilinx, says that the reprogrammable chips are off-the-shelf standard projects; thus they can eliminate the high engineering costs and long lead times associated with other ASIC prototypes. Semi-

custom logic devices traditionally take several months to create, eating up tens of thousands of dollars in nonrecurring engineering charges. Xilinx's PLDs, on the other hand, can be designed into an application in a few days using a CAD workstation.

#### PROTOTYPE PRESSURE

In Landry's view, design engineers often hesitate to experiment once their breadboarded logic is operating properly. The reluctance usually stems from short project schedules, not to mention the mechanics of reworking what might possibly be the only working prototype. Experimenting with multiple breadboards is a luxury few engineers can afford. If an experiment proves unsuccessful, restoring the

previous circuit configuration without introducing new errors becomes another potential pitfall. Many limitations are eliminated with in-circuit programmable devices.

Trimming the time needed to generate prototype circuits emerges as the objective of Laserpath Corp. (Sunnyvale, Calif.). As IC design manager Conrad J. Boisvert tells Electro attendees, a universal network physically connects all elements of a gate array. A laser beam severs the network at prescribed points, creating a personalized logic circuit (ELECTRONIC DESIGN, April 3, 1986, p. 31). Thanks to the technique, Laserpath can turn out prototype devices in one day at a fraction of the cost for a conventional gate array.□

#### Wells-Gardner takes the "cuss" out of customized



MOD 35 (15") High-density display features up to 35 kHz scanning frequency. CIRCLE 61



Optimiser " (12", 15", 17", 19") Optimum performance in a space-saving package. CIRCLE 64



Spectrum 14<sup>™</sup> (14") High resolution color display. CIRCLE 62



Customiser II<sup>™</sup> (7", 9", 12", 14") Wide variety of application choices. CIRCLE 65



MOD 64 (15", 17", 19") High-density display features up to 70 kHz scanning frequency.



Minimiser" (5" x 9", 7" x 12") Low profile design for microcomputers, point-of-sale terminals, instrumentation. CIRCLE 66 Customizing means frustrating in some engineering circles—synonymous with costly time and development delays.

At Wells-Gardner, as much as 80% of the custom design work is already done for you and skilled systems engineers are available to work with you in tailoring the remaining 20% to your application. Choose from any of the base models shown.

For details, call Larry Brady, Vice President, Data Display.

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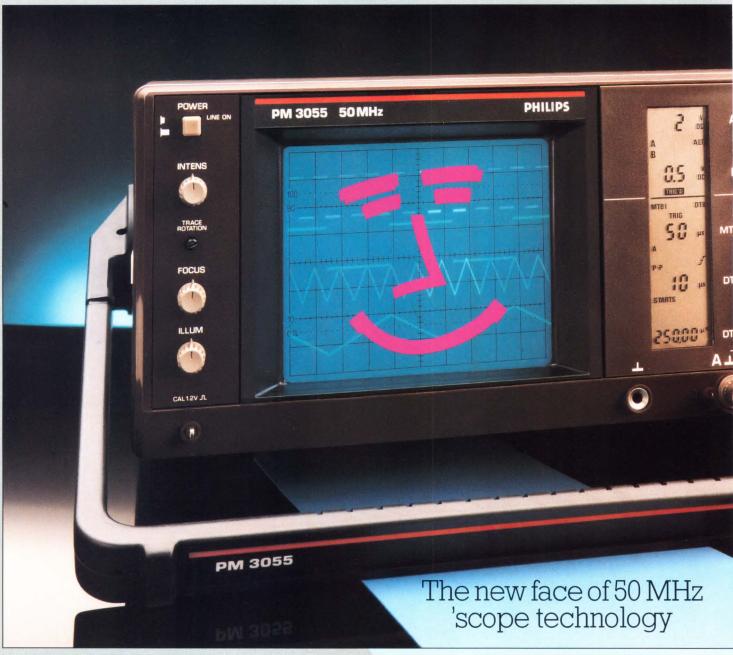


### **PHILIPS**



The new face of 50 MHz 'scope technology

## PHILIPS THE SMART







Advanced-design CRT. Philips' world-leading know-how in display and monitor tubes ensures optimum brilliance and spot quality. A 16 kV acceleration voltage and advanced electron optics give you display performance you've never seen before in this price class.



Versatile triggering functions up to 100 MHz. The PM 3050 family 'scopes have all the regular functions of auto, manual and single-shot triggering, plus smart, secure microcomputer control that 'thinks for you' in auto-triggering mode. Trigger bandwidth is an unmatched 100 MHz.

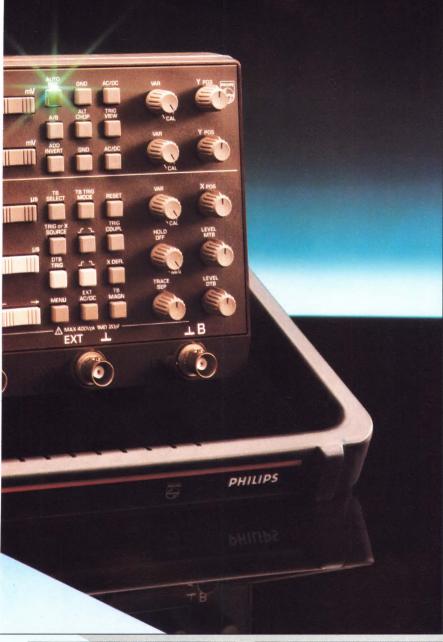


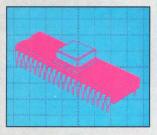
Fast computer hook-up. An add-on IEEE-bus option provides fast hook-up to a computer or controller, for use in ATE environments, quality control systems, training and many more applications. The ingenious separate IEEE option is readily interchangeable for automated scope calibration.

## SCOPE

Now, Philips' new technology in 50 MHz 'scopes puts the exciting PM 3050 family way out in front of the world's toughest competition.

For the first time ever in this price range, Philips PM 3050 uses the electronics and manufacturing technologies of the 1990s to take a giant step forward in ease of use and cost-effectiveness.

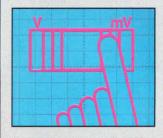




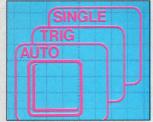
Autoset. PM 3050's green button gives you instant, fully automatic setting of all scope parameters – amplitude, timebase and triggering – for any input signal.



LCD panel. Gives clear indications of instrument settings, parameter values and selected control key functions at a glance, right next to the CRT screen.

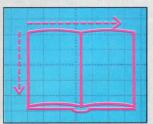


Up/down controls. Today's technology for fast, convenient input of amplitude (V/div.) and time (s/div.) settings.
Fingertip operation – just press one way for up, and the other for down.



Softkey function selection. Multifunction softkeys simplify the front panel layout, and make operation clearer and more logical. An instantly accessible

menu shows all available functions.



All-new front-panel design.

The all-new front-panel design makes operation clearer and simpler.

Control sequence is left to right, and top to bottom – just like reading a book!

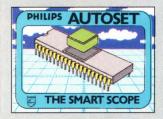


Designed for easy service. PM 3050 was designed to make any required service fast and simple. Swing-up PCBs make access easy, and flat ribbon cables allow instant disconnection. Each oscilloscope has a complete, built-in testing routine, to provide a quick assurance of correct operation.

"Special introductory price Dual Timebase.

PM 3055 at a Single Timebase Price \$ 1250\*"

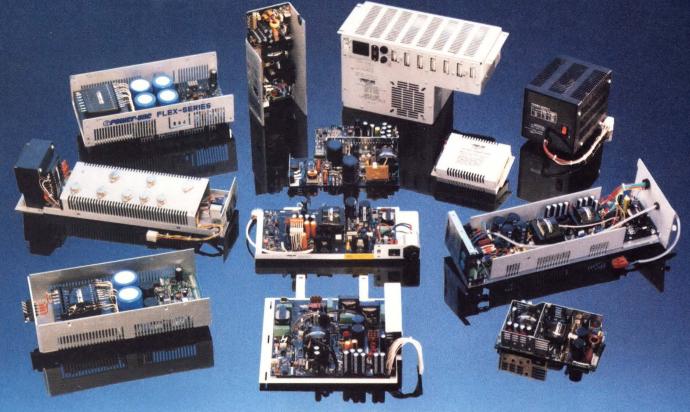
\*valid on orders received by July 31, 1986; not valid in combination with other Philips pricing programs.



For full information about the PM 3050 scopes family, contact PHILIPS TEST & MEASURING INSTRUMENTS, INC. 85 McKee Drive, Mahwah, New Jersey 07430 (201) 529-3800 TWX: 710 988-5348. For the Philips Sales Office or Representative nearest you call Toll Free 800-631-7172

Philips PM 3050 family: setting the new standard

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**ELECTRONIC DESIGN EXCLUSIVE** 

#### 800-W synchronous switcher guarantees 86% efficiency on all auxiliaries

Hard-disk-based computer systems require precise power regulation, as well as extra power for start-up surges. The Elpac EPC-800 is the first switching power supply to deliver 800 W of regulated power with up to five fully regulated outputs. Moreover, because of its unique synchronous switching design, the four secondary, or auxiliary, regulators have minimal power losses, coming in at 86% efficiency.

The unit is designed to handle start-up surges of up to 930 W. The secondary switchers feed off of the primary switching transformer and are thus synchronized to the main switching frequency. Such synchronization eliminates the need for auxiliary input filtering, thus cutting down on the unit's overall size.

Because the secondaries do not move large amounts of current, they can use MOSFET switches. Thanks to the voltage characteristics of these switches, outputs from the secondaries can be combined to share loads. Thus users can upgrade their systems to work with higher amperage disk drives by pairing secondaries. One way to plan for disk upgrades would be to use supplies larger than called for, with unused secondaries. Those secondaries can then be added as needed.

Both the main and the auxiliary outputs are tightly regulated to 0.2% for 5-V outputs, to 0.5% for 12-V,

and to 8% for 24-V. Also, ripple and noise are held to a  $\pm 1\%$  maximum pk-pk. The line is regulated to  $\pm 0.2\%$ .

A 50 ft<sup>3</sup>/min. fan cools the supply. If the air flow is restricted or the 50°C operating temperature is exceeded, the supply will shut down. Further, the inrush current is limited by a thermistor. At cold start, peak current is held to 57 A at a line voltage of 230 V ac.

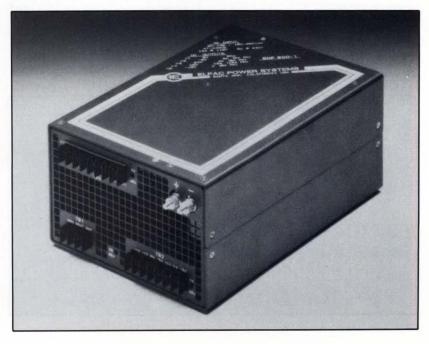
The switcher meets the following safety requirements: UL 1012/478,

CSA 22.2, VDE 0730/0804, and IEC 380/435. Additionally, both the VDE 0871/6.78 and the FCC 20870 Part 15 EMI standards are

The Model EHP800, with 4 switching auxiliaries, costs \$600 each in lots of 100. Switching auxiliaries can be purchased at \$72 each.

Elpac Power Systems Inc., 3131 S. Standard St., Santa Ana, CA 92705; (714) 979-4440.

CIRCLE 304 **BOOTH 1036, 1038** 





**ELECTRONIC DESIGN EXCLUSIVE** 

#### 500-ns conversion time keeps hybrid a-d converters at the head of the pack

A record-setting 500- to 600-ns conversion time puts Datel's hybrid analog-to-digital converters in a class by themselves. What's more, at 1.5 W, the ADC 500 series of 12-bit converters consumes half the power of earlier devices. Further, the commercial and military versions of the chip miss no codes over 12 bits and have more specifications guaranteed over temperature than do other parts.

The hybrid converters not only sport three-state outputs (allowing them to access 8-, 12-, and 16-bit buses) but also furnish a trio of novel pins. First, an Overflow pin indicates when the input signal exceeds the full-scale range of the device. Second, when used with the almost mandatory sample-and-hold amplifier, the signal on the Sample/Hold pin returns the amplifier to the sampling mode 50 ns before the conversion is complete, thereby reducing total conversion time by 10%. Finally, the Comp Bin pin makes it possible to select the output code format.

The conversion time for the commercial-grade model, the 500BMC, is a maximum of 500 ns at 25°C and no more than 550 ns between 0° and 70°C. If a 600-ns conversion time can be tolerated at 70°C, the Model 505BMC does the job at a 12%

lower cost. When the military temperature range is required, the user can turn to the 505BMM, which has a maximum conversion time of 650 ns between -55° and 125°C (550 ns at 25°V).

Between 0° and 70°C, the specifications for all three models are similar. Both integral and differential nonlinearity are a maximum of  $\pm 1/2$  LSB. For the military unit, they rise to  $\pm 3$  and  $\pm 1$  LSB respectively over the temperature

Full-scale absolute accuracy (often unspecified) is within  $\pm 10$  LSB from  $0^{\circ}$  to  $70^{\circ}$ C. It rises to  $\pm 20$ LSB for the military devices. Both unipolar and bipolar offset voltage errors are under  $\pm 25$  ppm/°C. The offset as well as gain errors can be trimmed to zero by the user.

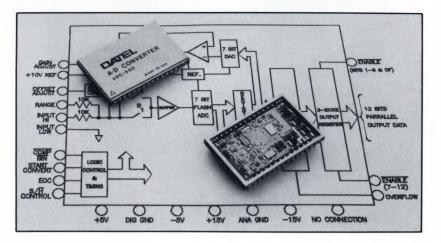
The converters can be configured to work with full-scale input signal ranges of 0 to 10, 0 to 20 and  $\pm$  10 V. Power requirements are 18 and 12 mA respectively from the +15and -15 V rails and 48 and 161 mA from 5 and -5 V rails. The devices are housed in 32-pin hermetically sealed triple-width ceramic DIPs.

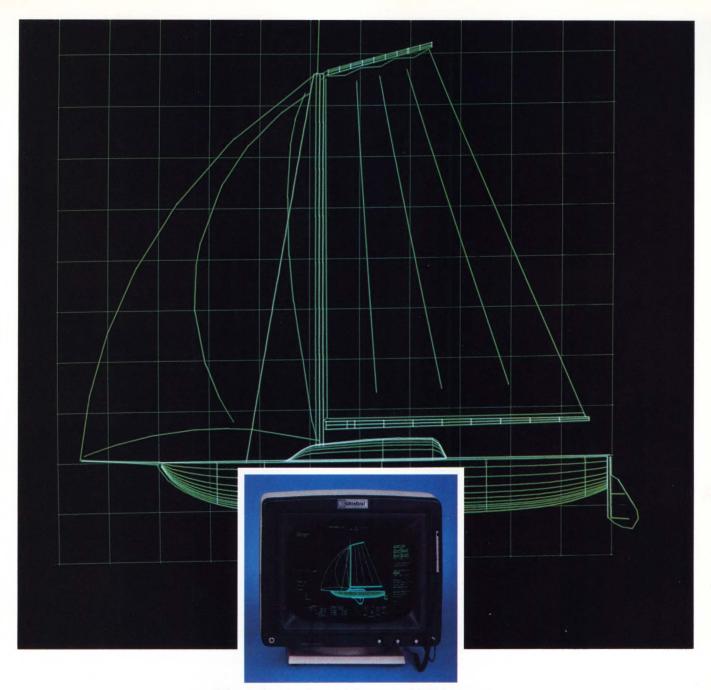
In quantities of 100, the 500 BMC, 505BMC and 505BMM cost \$397, \$346 and \$450. Small quantities are available from stock.

Datel, 11 Cabot Blvd., Mansfield, MA 02048; Bob Leonard, (617) 339-9341.

CIRCLE 305 **BOOTH 1170** 

#### Frank Goodenough





### Designing Is a Breeze with Lundy's New UltraGraf® II

No matter what business you're in, sluggish productivity could blow you—and your profits—away. But now, thanks to Lundy's new UltraGraf® II, there's an economical way to fight back. UltraGraf® II is an intelligent 3-D graphics workstation with features and functions that help you breeze through intricate designs.

#### **Exceptional Quality and Performance**

What sets UltraGraf® II apart from other workstations in its price range is its exceptional quality and performance. That's because Lundy engineers have developed extremely efficient vector and hardware processors that permit fast, high resolution design. And unlike many

other workstations, UltraGraf® II is highly intelligent. So functions such as 3-D translation, rotation, and scaling are performed locally, increasing design speed even further while freeing your host. The result is fast, high quality design that helps keep rigid development schedules firmly on course.

A wide variety of options and accessories are available to help make graphics design as convenient as possible. And as with all Lundy products, UltraGraf® II is backed by our customer service and support network, one of the largest in the industry.

This combination of speed, intelligence, responsiveness, economy, options, accessories, service and support

make UltraGraf® II the ideal choice for mechanical design and drafting, architectural engineering, finite element analysis, robotics, and other applications that require high resolution display.

So don't let sluggish design productivity take the wind out of your sails. Fight back with UltraGraf® II.

Contact: Graphics Marketing, Lundy Electronics & Systems, Inc. 1 Robert Lane, Glen Head, N.Y. 11545 (516) 671-9000.





**ELECTRONIC DESIGN EXCLUSIVE** 

## 300-kHz dc-dc converters reach 82% efficiency, deliver 1.5 W per in.<sup>3</sup>

Over the past ten years, ac-powered switching power supplies have made great, albeit gradual, progress. Dc-dc converters, by contrast, have more or less stagnated, sticking to the 25-kHz switching frequency and bipolar power devices of a decade ago. Now, in one dramatic leap, dc-dc converters have attained parity with line-powered supplies in Kepco/TDK's ERD series of 300-kHz converters. Built with power FETs and the company's latest cool-running ferrite—type H7C4—the ERD series comes in with efficiencies as high as 82%, which permits a volumetric power density of 1.5 W/in.3—a 2.5 times improvement over its predecessors. Units in the series also cost about half as much per watt as their forebears and deliver three times the power per unit weight.

#### Michael Riezenman

The converters employ two hybrid ICs, which provide overvoltage and overcurrent protection while also performing the pulse-width modulation function. The ICs make possible a 50% reduction in parts count over previous converters, resulting in a boost in MTBF from roughly 50,000 hours to about 250,000 hours (6 years to 29 years).

The single-output series comprises a total of 30 models. They come with power ratings of 30, 60, and 150 W; input-voltage ratings of 24 and 48 V; and output voltages of 5, 12, 15, 24, and 48 V.

All units in the ERD series contain an EMI filter so they can meet the conducted-noise specification of MIL-STD-461B. They also meet the UL 478 and CSA C22.2-154 safety standards. Additional features include remote sensing (to maintain tight regulation at the load even in the presence of substantial

voltage drops in the main output lines) and isolated remote on/off control, which can be actuated by a TTL level.

For all models, the output can be adjusted around its nominal value. The adjustment range is -20% to +10% for the 5-V and 15-V models and -30% to +10% for all of the others.

Maximum peak-to-peak ripple is no more than 50 mV (30 mV, typical) for the 5-V supplies, increasing to 150 mV (60 mV, typical) for the 48-V units. Maximum peak-to-peak spike noise ranges from 100 mV (5 V) to 530 mV (48 V). Line regulation is 0.8% (0.2%, typical). Load regulation for a load change from 10% to 100% is no more than 1% (0.3%, typical). The maximum combined effect of line, load, and temperature changes, over the range of 0° to 71°C, is 2% (0.6%, typical). When presented with a 50% load change, supplies in the ERD series will suffer output excursions of no more than 4% and will recover to within 1% in less than a millisecond.

For single units, the 30-W converters are priced at \$135; the 60-W devices go for \$160, and the 150-W supplies sell for \$225. Quantity discounts are available. Deliveries begin this month.

Kepco/TDK Inc., 131-38 Sanford Ave., Flushing, NY 11352; Paul Birman, (718) 461-7000.

CIRCLE 325 BOOTH 1111, 1112 IF YOU THINK MEMORIES IS A CLOSED MARKET, THINK AGAIN.



#### Single box calibrates 61/2-digit DMMs

Except for cheap, hand-held instruments, the biggest selling digital multimeters today are 61/2-digit units. These extremely precise instruments are typically calibrated with difficulty and at great expense. Now, with Datron's Model 4700 calibrator, there exists a single box that can calibrate all of the functions of a modern 51/2- or 61/2-digit multimeter-ac and dc voltage, ac and dc current, and resistance. What's more, for suitable meters, it is equipped to calibrate automatically over the IEEE-488 interface bus.

Before the 4700, calibrating a 61/2-digit DMM required from two to five instruments with a total cost of \$40,000 or more. Moreover, the



job was difficult to automate because the use of multiple instruments almost always meant that a technician had to be standing by to swap test leads from calibrator to calibrator.

The 4700, when fitted with its resistance, current, and highvoltage options, costs only \$17,985, and can do a complete calibration through a single set of terminals.

The instrument supplies dc volt-

ages from 10 nV to 1100 V with 90-day absolute accuracies to  $\pm 10$ ppm. The ac voltage outputs are accurate to better than  $\pm 300$  ppm, and range from 90  $\mu$ V to 1100 V. Frequency is continuously variable from 10 Hz to 1 MHz, although the frequency and voltage cannot be maximized at the same time.

The instrument itself can be calibrated automatically. In its basic form, in which it puts out ac and dc voltages up to 200 V, it sells for \$9995. Delivery takes 60 days.

Datron Instruments Inc., 4125 S.W. Martin Hwy., Stuart, FL 33497; (305) 283-0935 or (800) 327-0938.

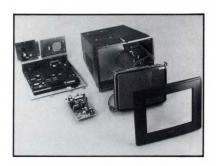
**CIRCLE 308** BOOTH 0576, 0578

#### Touch screen cuts design time 80%

Traditionally, integrating touch control into a system meant gathering the necessary parts and spending time piecing them together. Now, Fluke unveils the 1020 touchcontrol screen, which has all the hardware and software working in concert, reducing design time 80%.

The hardware includes a 12-in.diagonal green phosphor monitor (amber is optional) with a factoryaligned touch screen mounted on it. Touch-screen parameters, such as baud rate (up to 19.2 kbaud) and parity are entered through the screen itself and are stored in a 256 bit EEPROM. The system can display the entire ASCII character set, and it recognizes X3.64 commands, as well as command strings.

Software, running on a 68008 processor with 10 kbytes of RAM is



stored in 64 kbytes of ROM. It simplifies the host programmer's job by passing back the number of the depressed touch screen cell—freeing him from having to calculate it. It also allows touch targets to be displayed on the screen by sending high-level commands over an RS-232 link. These commands can specify target shape, size, and location.

The screen has an antiglare and

antiscratch coating, and each cell can be touched over 1 million times. If the screen is damaged or soiled it can be snapped off without trouble for replacement.

The system was designed to meet the safety specifications of the VDE, CSA, UL, and IEC and comply with the radio-emission standards established by FCC class B.

Depending on configuration, the unit draws between 30 and 50 W. In single quantities the part costs between \$1400 and \$1600. Delivery takes six to eight weeks.

John Fluke Mfg. Co. Inc., P.O. Box C9090, Everett, WA 98206; (800) 426-0361. (206) 356-5400 (Washington and Alaska).

**CIRCLE 307** 

BOOTH 2303, 2305, 2307, 2309, 2402, 2404, 2406, 2408

## THERE'S A NEW CONTENDER IN THE MEMORY GAME.

When it comes to memory products, Samsung is coming on strong.

We're offering an ever-broadening line of products. We're building top-quality, industry-standard products of our own design, like our 64K and 256K DRAMs. And we're keeping costs down and volume up with production facilities internationally recognized as being among the most advanced in the industry. For example, Samsung is one of the few semiconductor companies fabricating 6-inch wafers in production quantities.

In fact, in the last four years, Samsung has made a \$500 million commitment to developing and producing memory products, primarily for the U.S. market.

That means we're here to stay.

So if your current memory suppliers are less committed than you'd like, find out about Samsung. Just call your local Samsung sales representative or distributor to get our databook, samples and reliability report.

Samsung. We're on your side in the memory game.

#### Samsung Memory Products

Density	Org.	Access Time (ns)	Mode	Packaging
64K 256K 256K		120/150 120/150 120/150	PAGE NIBBLE NIBBLE	DIP DIP, PLCC, ZIP DIP, PLCC, ZIP
16K 16K 64K	2Kx8 2Kx8 8Kx8	300/350 300/350 250/300	R/B	DIP DIP DIP, PLCC
64K	8K x 8	100/120/150		DIP/SOP
	64K 256K 256K 16K 16K 64K	64K 256K 256K 16K 16K 16K 2Kx8 64K 8Kx8	64K 120/150 256K 120/150 256K 120/150 16K 2Kx8 300/350 16K 2Kx8 300/350 64K 8Kx8 250/300	64K 120/150 PAGE 256K 120/150 NIBBLE 16K 2Kx8 300/350 R/B 64K 8Kx8 250/300



#### SAMSUNG

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CIRCLE 69



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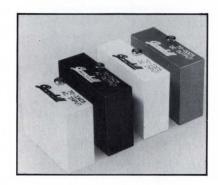


#### Surface mounting cools I/O modules

A family of solid-state I/O modules employs surface-mounted parts to lower its internal operating temperature, thereby improving reliability. In fact, burn-in tests reveal that Grayhill's Series 70 modules typically exhibit more than a 100,000 hour mean time before failure.

The modules are built to standard external dimensions, so using smaller chip components frees up more space within the casing, making for a cooler device. For example, a 3.5-A module's internal temperature is roughly 100°C, about 15° cooler than equivalent parts.

The family can be closely matched to the output current of a controller, improving efficiency. Such matching minimizes current loss, letting each controller handle



more modules than can systems that use external resistors to equalize currents. The modules deliver up to 4000 V of isolation protection for the controller's logic circuitry.

The ac modules operate with either 120- or 240-V ac power supplies. Ac input modules monitor these loads and furnish 5-, 15-, or 24-V dc signals to the controller. Ac

output modules switch the ac power loads based on 5-, 15-, or 24-V dc

The dc output modules switch 3to 60-V dc loads using 5-, 15-, or 24-V inputs. Dc input packages monitor 3- to 32-V dc loads and put out standard voltage signals to logic circuitry. Finally, both ac and dc modules meet ANSI and IEEE specifications for false triggering.

In 100-lot quantities, prices range from \$6.20 to \$8.17, depending on the module and voltage. Evaluation units are available from stock; production shipments take five weeks.

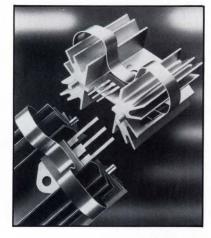
Grayhill Inc., 561 Hillgrove Ave., La Grange, IL 60525; (312) 354-1040.

CIRCLE 302 BOOTH 1517, 1519, 1521, 1523, 1525

#### Heat sink clips to 20-W parts

For the first time, power transistors packaged in plastic and dissipating 20 W can be mounted to heat sinks as easily as their lower-power brethren. Aavid Engineering's Series 5334-36 employs a simple spring clip to hold the heat sink to device, greatly reducing board assembly time and cost. The clips eliminate the nut, lock washer, and bolt conventionally required to mount sinks to power semiconductors housed in TO-218 and TO-220 packages.

The clip also eliminates the gap that occurs between a power device and the heat sink when the nut is overtightened. Instead, the spring clip applies even pressure across the package, resulting in maximum metal-to-metal thermal contact between the sink and the device. The result is a surface-to-ambient ther-



mal resistance of 3°C/W in air moving at 200 ft/min.

The sink mounts vertically on a board and is supplied in four heights:  $1, 1^{1/2}$ , 2, and  $2^{1/2}$  in. It is furnished with two mounting pins that solder to the card or with two predrilled holes for self-threading

A notch in the bottom of the sink permits wiring on the board to pass under the sink. Thus the pins of the power device can be reached without danger of a short circuit.

The Series 5334-36 are fabricated from extruded aluminum. For maximum heat dissipation they have a black anodized finish, but other colors are also available.

In quantities of 1000 the 2-in. heat sink costs 83¢ each. Free samples are available, and all deliveries are from stock.

Aavid Engineering Inc., One Kool Path, P.O. Box 400, Laconia, NH 03247; Allen Hillman, (603) 524-4443.

**CIRCLE 306 BOOTH 1349** 

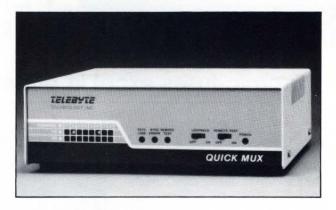
## **QUICK MUX**

Reduces costly equipment requirements.
Allows simultaneous 8 channel operation.

QUICK MUX drastically reduces the amount of equipment and cost required to link 8 remotely located RS-232 devices to a host computer.

The wiring requirements are reduced by a factor of eight by providing up to eight terminal operation over the same twisted pairs that usually support single channel operation.

Each input port of the QUICK MUX can accept full duplex data at any rate up to 19,200 bps. and can operate at its own baud rate with any bit protocol. Different speeds in each direction are easily accomodated. The composite port which is used to link multiplexers together features a built-in line driver with the ability to communicate over 5000' feet of two twisted pair. A long range option is available for greater distances.



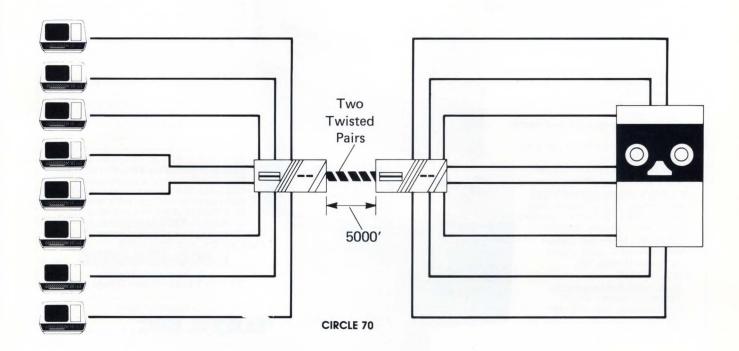
Diagnostic features of the QUICK MUX include visual displays of Receive Data and Transmit Data for each port and Data Error and Data Loss Indicators for the composite link. In addition, switches are provided to force either a local loopback or remote multiplexer test.

The Model 570 QUICK MUX with 8-25' cables and 8 Plugaverters sells for \$548 in single quantity. Substantial discounts are available for OEM's. Model 571 incorporates 8 built-in tail circuit modems to support distances up to 1 mile.

Input ports have built-in surge protection while the composite link has built-in lighting protection.

Contact us today at Telebyte Technology Inc., 270 E. Pualsky Road, Greenlawn, New York 11740, 800-835-3298 or (516) 423-3232.





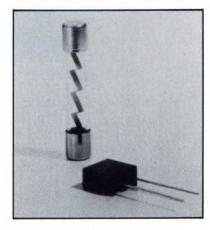


#### Ceramic fuses excel in protection

A family of ceramic fuses breaks new ground in a number of areas. Bussmann's PC-Tron series passes far less current during short circuits than do any other fuses, thus protecting sensitive ICs to an unrivaled degree. It also contains the first surface-mounted fuse.

The fuse comprises a thin-film element sandwiched between layers of ceramic (ELECTRONIC DESIGN, April 17, p. 12). The film elements break far more quickly than do wire elements suspended in air.

The family also sharply trims board space requirements: up to eight PC-Trons can fit in the space taken up by a single glass fuse. In fact, the components are only



slightly larger than their subminiature counterparts. Their dimension are 0.184 by 0.350 in. They stand 0.350 in. above a board, enabling them to be used with standard automatic insertion equipment. The pins are spaced 0.200 in. apart, fitting standard grid spacings.

The family includes the first surface-mounted fuse. Its gull-wing leads also fit standard pad layouts. Both standard and surface-mounted fuses withstand normal solder and washing operations.

The members of the family cost about 45¢ each in 100-lot quantities. Prices will vary with different current and voltage values. Delivery is from stock.

Bussmann Division, Cooper Industries Inc., P.O. Box 14460, St. Louis, MO 63178; (314) 527-3877.
CIRCLE 301

BOOTH 2253, 2255

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## If your system is only using this many colors, isn't it time to grow up?

The INMOS IMSG170 Color Look-up Table offers a grown-up solution to video display color enhancements. It lets you and your RGB analog display advance to a palette of more than a quarter million colors.

This programmable DAC conforms to RS170A standards with pixel rates up to 50 MHz, in a 28 pin package.

And to simplify things, the table integrates the functions of a 256 word x 18 bit color mapping table, three 6bit DACs, 75 ohm drivers and microprocessor interface into a monolithic CMOS device. The result? Reduced

board space and power consumption at a lower cost.

The Color Look-up Table from INMOS. Designing with thousands of colors just became child's play.

INMOS Corporation, Colorado Springs, Colorado, Tel. (303) 630-4000 Bristol, England, Tel. 0272-290-861 Paris, France, Tel. (1) 687-2201 Munich, Germany, Tel. (089) 319-1028



Compare your computer design colors to these crayons. If the crayons win, call INMOS.



## DISCRETE LOGIC ISN'T AS SAFE AS IT USED TO BE.

Discrete takes just too much time, space, effort and materials to keep you competitive. That's not good at a time when the marketplace is getting downright treacherous. You have to put more and more functions in less and less space—at lower costs. And if you're not out there sooner than your competitors, they'll eat you alive.

Fortunately there's a way to minimize that risk. One that's safe, reliable, simple and fast.

Programmable Logic Devices from Signetics. In fact, Signetics has the most complete, most flexible, best-supported PLD series in the industry.

Want to reduce your part count? Often, as few as five Signetics PLDs can replace as many as 60 SSI/MSI devices. They not only simplify state machine design and reduce the package count of random logic functions, but also cut your time to market.

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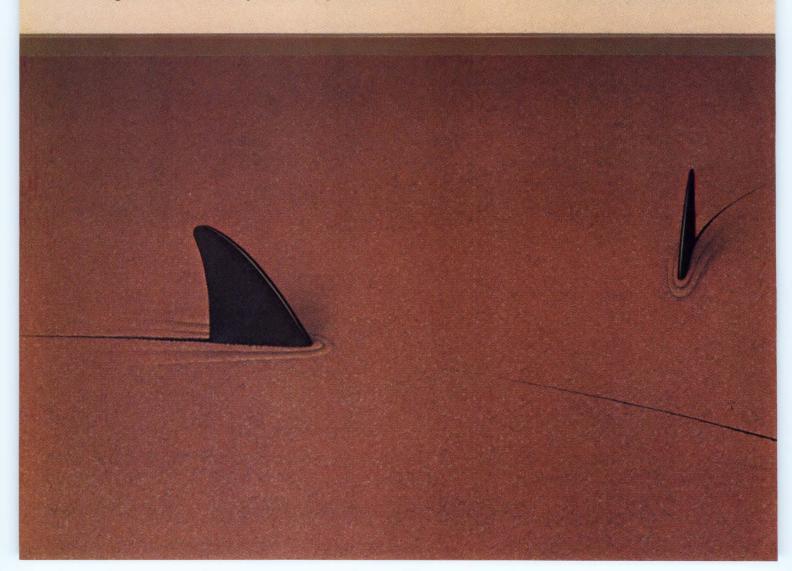
your function in terms of a Boolean equation, program the fuses and your circuit is ready to go. We provide software—free of charge to qualified users—that turns an IBM\* PC into a PLD work station. Complete documentation and design simulation let you perfect your ideas to the nth degree. And if you have any questions, a phone call to one of our field applications engineers will get you the answers fast.

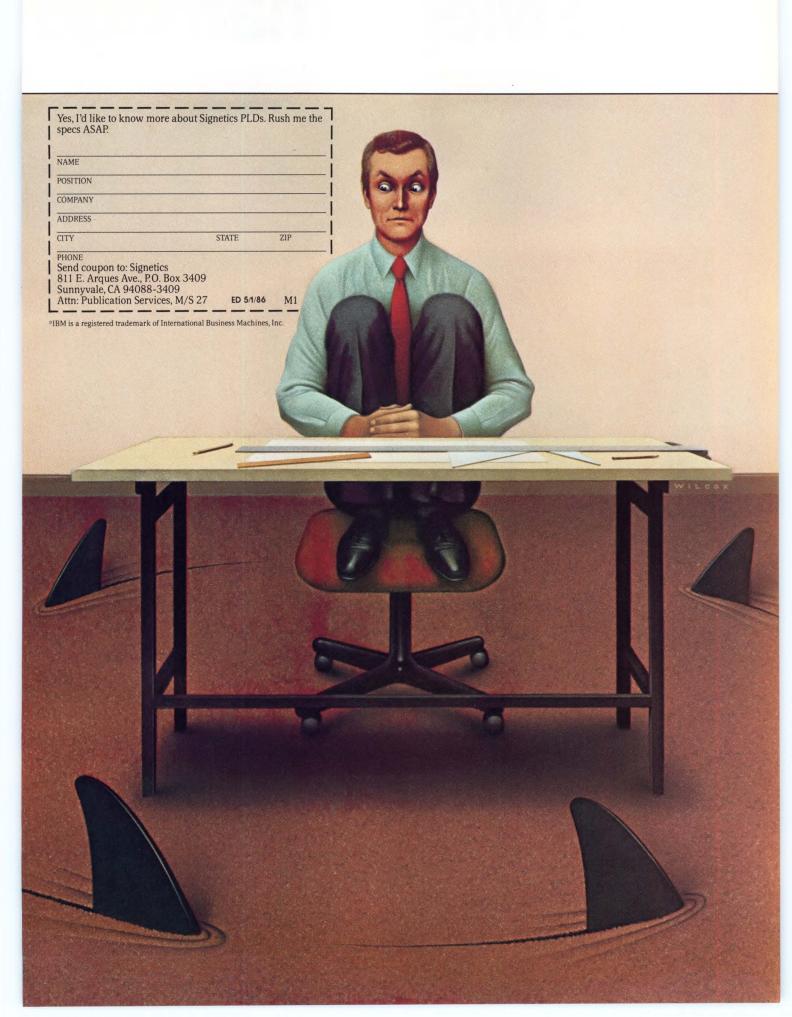
There's more you should know about Signetics PLDs. For details and specs, just send in the coupon.

Signetics Programmable Logic Devices. Because these days, you either perform swimmingly, or you're sunk.

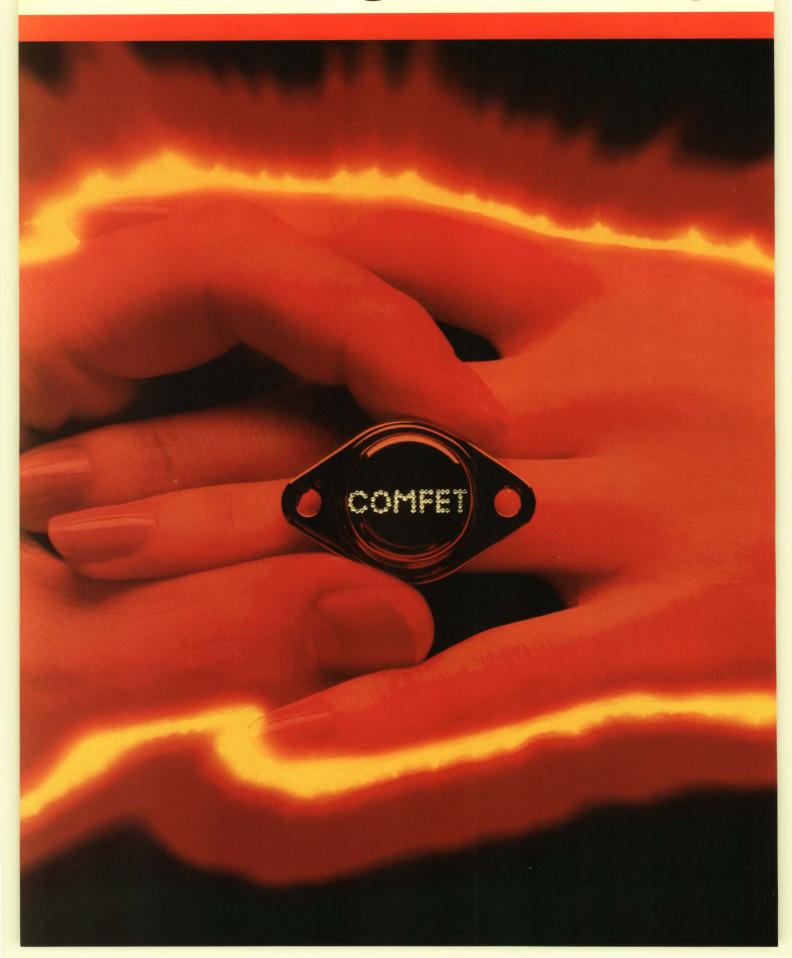
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## The Mega-marriage



## of MOS and Bipolar.

## New COMFETs combine the best features of MOSFETs and Bipolars.

The best features of MOSFETs are high input impedance, fast switching and reduced driver circuitry. The best features of Bipolars are cost effectiveness and low conduction losses.

Now, you get the best of both with new RCA COMFETs.

In MOSFETs, on-resistance increases with increasing drain-source breakdown voltage (BV<sub>DSS</sub>) capability. In COMFETs, the conductivity is dramatically increased (modulated) by injected carriers. That's why we use the acronym COMFET (COnductivity Modulated FET). That's why conduction losses of COMFETs are an order of magnitude lower than MOSFET conduction losses. And that's why COMFETs are ideal for high voltage, high current applications.

#### Less than half the price of MOSFETs.

As the chart shows, COMFETs use considerably less silicon than Bipolars or MOSFETs in high voltage applications. Reduced size makes COMFETs less than half the cost of MOSFETs and very price competitive with Bipolars.

Since COMFETs are gated on/off like MOSFETs and provide traditional MOSFET advantages, they can reduce overall system cost significantly in high voltage applications such as switch mode power supplies and motor controls.

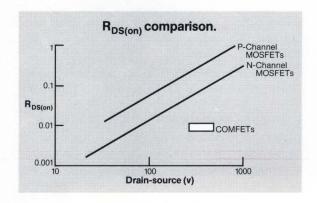
#### Five times faster than Motorola or G.E. devices.

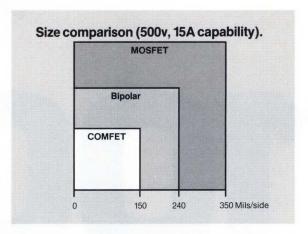
RCA invented the first conductivity modulated FETs, and our design is by far the fastest, with typical fall times of only 400 ns at room temperature.

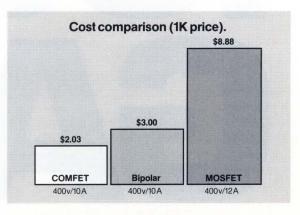
And our line is expanding rapidly. We'll soon have COMFETs that are twice as fast as present COMFETs, plus 500V, 20A devices.

#### Order samples today.

Call your RCA stocking distributor or RCA sales office for samples. Or write: RCA Solid State, Box 2900, Somerville, NJ 08876.





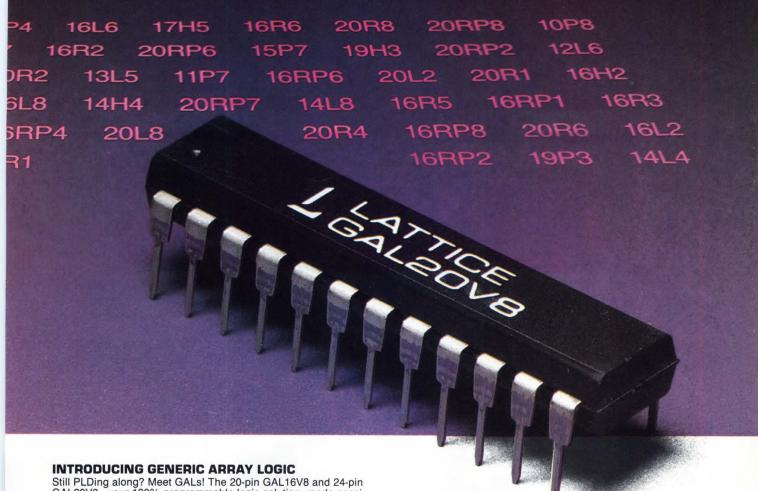


Call: Hamburg, 49-4106-6130; London, 44-93-2785511; Paris, 33-3-946-5656; Hong Kong, 8-52-3-723-6339; Sao Paulo, 55-11-210-4033.





# 100% GAL



Still PLDing along? Meet GALs! The 20-pin GAL16V8 and 24-pin GAL20V8...your 100% programmable logic solution, made possible by Lattice's ultrafast E²CMOS™ technology. 100% bipolar-compatible (truly, with 24mA output drive) — both offer a t<sub>pd</sub> of 17ns typical, 25ns worst-case over temperature. With 100% programming and 100% programming the conditions of the conditions gramming yields...and 100% + architectures. Generic means they take any architecture - odd, even, or even unknown. 100% programmable and reprogrammable — anytime, everytime — instantly. With outputs that you define to be active-high, active-low, synchronous, asynchronous - on any pin, at any time.

#### A PROTOTYPER'S DREAM

Prototyping new systems? Save yourself the nightmare of trashing 50 or 100 PAL® devices per board design (or running back and forth from your UV lamp). GAL devices are 100% instantly reprogrammable to any pattern, any device architecture, any output polarity — registered or nonregistered — anytime, everytime, instantly. GAL — a prototyping dream — in low-power E<sup>2</sup>CMOS, from Lattice.

#### YOUR NAME IN SILICON

Tired of taping PLDs to your wall? Production control out of control? Now you can store your name, or your division's name, in every part. Only Lattice GAL devices give you 64 bits — 8 alphanumeric characters — of electronic signature to help you keep track of your designs, socket locations, pattern IDs, rev. numbers, girlfriends' phone numbers, and more

#### **QUARTER YOUR POWER WITH E2CMOS**

GALs, the fastest CMOS PLDs, won't burn up your boards, power supplies (or fingers). Plug in our GAL devices and you've instantly cut power consumption — without sacrificing performance. Quarter-power GALs run cool at typically 30 mA. And lower power translates to cooler-running, more reliable systems

#### STANDARD PROGRAMMING TOOLS

No need to waste money on new boxes. If you're already using programmable logic, you can upgrade to GAL devices immediately. Data I/O, Stag, and other hardware will program them, and standard software like CUPL®, ABEL™, and PALASM® will compile your source code. In most cases, your existing master devices and JEDEC files can be used without modification. and JEDEC files can be used without modification.

#### ZERO DEFECTS — 100% YIELD — GUARANTEED

98% programming yield? Forget it. E²CMOS technology guarantees a quality level in parts per million, not parts per hundred. Move up to a standard that only 100% tested E²CMOS GAL devices — cycled through every worst-case pattern at our factory — can provide. Not 98%. Not 99.9%. Stop wondering what your programming yield will be. Lattice guarantees you 100%. Period.

#### DOCK-TO-STOCK, JUST-IN-TIME

Believe your eyes. Only multiple-tested E<sup>2</sup>CMOS GAL devices give you 100% guaranteed programming yield without incoming QA. Tired of writing cumbersome test vectors — for every device type, for every different pattern? Buy one device type, not a whole



catalog of parts. Then take your GAL devices straight to the manufacturing floor. Incoming QA? Just count the pins! GAL devices are the first programmable logic devices to take the hassle out of production control and inventory management.

#### CH-LOCKED™ CMOS — A NEW STANDARD

Hot-socket your GAL devices, again and again. You've moved up to a new standard in CMOS reliability with Latch-Lock — a proprietary new technology (patent pending) that makes GALs impossible to latch up under any conditions! Only Lattice guarantees 100% latch-up proof E<sup>2</sup>CMOS — the high-speed CMOS technology of the future.

#### IN VOLUME PRODUCTION NOW

Some day, all systems will be built with the technology you can program to be anything, everytime, instantly: E<sup>2</sup>CMOS. Make your move with Lattice GALs today.



When specifying circuit breakers, protection is not the only consideration. Because different applications require different features, we introduce four exciting new products to the most comprehensive line of magnetic circuit breakers in the world. International spacing and appealing design are combined in our new G and L Series circuit breakers with X-style handle. The L version is the first 50 amp breaker ever to sport an attractive rocker handle. Both versions combine on/off switching with circuit protection in one device. Attractive enough to mount up front, X-style breakers save real estate and eliminate the need to stock and install multiple components. They comply with VDE spacing requirements and are available in one- to four-pole models, 0.050 to 50 amps, with white, grey, black, orange or red handles. The beauty of N-style breakers (also available in G and L Series) lies in their ability to withstand harsh environments by providing waterproof panel integrity. The L Series is the first 50 amp frame size breaker with this benefit. Models are available in one- to three-poles, 0.050 to 50 amps. Call us today with your specifications. Airpax Corporation, Cambridge Division, Woods Road, Box 520, Cambridge, MD 21613. (301) 228-4600. A North American Philips Company.





















#### READER FEEDBACK

#### Compelled to speak out

There were two contrasting doublepage advertisements in the Jan. 9 issue that are worthy of comment. RCA's "Pursuing Halley's Comet" [pp. 134-135] shows all five satellites involved, including the Soviet one. This has a very positive message of international cooperation.

The Valid Logic ad (pp. 236-237) shows quite clearly a picture of a laser weapon destroying something. Even though the copy identifies the something as space junk, the suggestion of Star Wars is very strong, if not unavoidable.

The time is long overdue for me and other engineers to say that making vast quantities of useless weapons, \$1000 toilet seats, or whatever, is not only a pointless waste of effort and time in itself, but also requires governments and business to justify it.

You probably realize that the great surge in the peace movement in Europe was triggered by the need to justify new weapons of which, in Britain, Cruise missiles are a prime example.

The Cruise missile is a nuclear system that is very slow, low flying, and extremely accurate. Hence its purpose is to destroy military targets, particularly missile silos, and because it has a flight time of up to about 4 hours, it is suitable only for a first-strike surprise attack. (See "The Ground-Launched Cruise Missile: A Technical Assessment" by Tim Williams, published by Electronics for Peace, Townsend House, Green Lane, Marshfield, Chippenham, Wilts. SN14 8JW, U.K.). Fortunately, although deployed, it does not work yet.

One could well argue that you don't get something for nothing, and the U.S. present of the Cruise missile gives Britain nothing. Certainly Star Wars would not give the world anything.

**Andrew Lohmann Tunbridge Wells** Kent, England

#### Trademarks: Making a case for caps

Thank you for including Multiflow Computer in "Minisupercomputers Mix Vector Speed, Scalar Flexibility," in the March 6 ELECTRONIC DESIGN.

I would also like to make you aware that Multiflow has adopted and used TRACE SCHEDUL-INGTM and VLIWTM, respectively, as trademarks for its compacting compiler and wide-instructionword computer. Your article used TRACE SCHEDULING<sup>TM</sup> in a generic fashion; We request that your future use include appropriate acknowledgment of these terms as our trademarks.

Leigh Cagan **Director of Administration** Multiflow Computer Inc. Branford, Conn.

Our style in handling trademarks—like that of every other technical publication we know of—is to use simply an initial capital letter for each word without the "TM" superscript. Thus, in this case, we should have cited the feature as Trace Scheduling.

Be sure to see **Electronic Design's Professional Opportunities** Section. It starts on page 334.





We're sure that Ma Bell had another idea in mind when she designed the original phone booth, but good olde Yankee ingenuity took over and was not about to let all that space go to waste – giving new meaning to the words "High Density". No easy in, easy out here. Jonathan saw this same situation arising in standard 19" cabinetry, as it lent itself more and more to high density chassis packaging but still contended with less than acceptable stickslip access with friction chassis slides.

**The answer** to this predicament is Jonathan's new Series 375QD TRU-GLIDE® ballbearing steel chassis slide. The replacement for the friction Accuride 830, Chassis Trak C-300, Grant SS-168 and Zero C-300 models, this new 75-lb. capacity slide is thin (3/8") enough to fit easily in a standard 19" cabinet, while providing smooth ball-bearing action and all the precise mounting, locking and chassis disconnect features you could want.

**Don't fight** with binding friction slides... when, for a few dollars more, you can put Jonathan's 30 years of packaging experience to work to smooth out all your access problems.



**Jonathan** Manufacturing Corp., 1101 So. Acacia Ave., Fullerton, CA 92634 • (714) 526-4651

#### UPCOMING MEETINGS

Fiber Optics '86 Conference & Exhibition, April 29-May 1. Earl's Court, London, England. Sira Ltd., South Hill, Chislehurst, Kent BR7 5EH, England; (+44) 1 467 2636.

36th Electronic Components Conference (ECC '86), May 5-7. Westin Hotel, Seattle, WA. ECC '86, Tom Pilcher, Publicity Chairman, Mallory Capacitor Co., P.O. Box 372, Indianapolis, IN 46206; (317) 261-1306.

Society for Information Display Conference & Exhibition (SID '86), May 6–8. Town and Country Hotel, San Diego, CA. Hildegarde Hammond, Palisades Institute for Research Services Inc., 201 Varick St., New York, NY 10014; (212) 620-3388.

Videotex '86, International Electronic Information Services Conference & Exhibition, May 6-8. Infomart, Dallas, TX. Cynthia Parsons, OnLine International Inc., 989 Avenue of the Americas, New York, NY 10018; (212) 279-8890.

5th Annual Small Computer Systems Conference, May 12–13. Opryland Hotel, Nashville, TN. Gartner Group Inc., 72 Cummings Point Rd., P.O. Box 10212, Stamford, CT 06904; (203) 964-0096, or Ashley Pearce, (203) 967-6757.

Custom Integrated Circuits Conference (CICC '86), May 12-14. Rochester Riverside Convention Center, Rochester, NY. Laura A.H. Silzars, Convention Coordinator, 6900 S.W. Canyon Dr., Portland, OR 97225; (503) 292-6347.

1986 Microwave Power Tube Conference, May 12-14. Naval Postgraduate School, Monterey, CA. David Zavadil, General Chairman, 1986 Microwave Power Tube Conference, Northrop Corp., 600 Hicks Rd., Rolling Meadows, IL 60008; (312) 259-9600, ext. 5934.

Computer Graphics '86 Exposition, May 12-15. Anaheim Convention Center, Anaheim, CA. National Computer Graphics Association, 2722 Merrilee Dr., Ste. 200, Fairfax, VA 22031; Christine Radiske, (703) 698-9600.

4th European Automated Manufacturing Systems Conference & Exhibition (AUTOMAN), May 12-15. National Exhibition Center, Birmingham, England. Cahners Exhibitions Ltd., Chatsworth House, 59 London Rd., Twickenham TW1 3SZ, England; (+44) 1 891 5051.

Electro '86 Conference & Exhibition, May 13–15. Bayside Exposition Center, World Trade Center, Boston, MA. Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (213) 772-2965.

Mini/Micro Northeast '86 Computer Conference & Exhibition, May 13-15. World Trade Center, Boston, MA. Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (213) 772-2965.

1986 Computer Standards Conference, May 13–15. Sheraton Palace Hotel, San Francisco, CA. R. Poston, PEI, Technical Program Committee Chairman, 68 Monmouth Rd., Oakhurst, NJ 07755; (201) 571-1071.

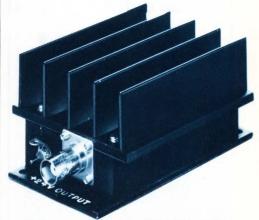
6th European Optoelectronics Conference (Opto '86), May 13–15. Palais des Congres, Paris, France. ESI Publications, 12 rue de Seine, 75006 Paris, France; (+33) 1 325 5874.

Expotronica '86, Professional Electronics, Equipment and Components Show, May 13-17. Barcelona Fair, Av. Reina M. Cristina, s/n. 08004 Barcelona-Espana; (93) 223 31 60-223 99 00.

1st Lasers in Manufacturing: Selection/Planning of Lasers Systems, Opportunity for Applications Growth and Latest Technology (S.P.O.T '86) Conference & Exposition, May 19-22. Philadelphia Dunfey-City Line Hotel, Philadelphia, PA. S.P.O.T. '86 Conference, Kathleen Warren, Society of Manufacturing Engineers, 1 SME Dr., P.O. Box 930, Dearborn, MI 48121; (313) 271-1500, ext. 317.

(continued on p. 150)

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## 50 KHz to 130 MHz only \$199 (1-9)

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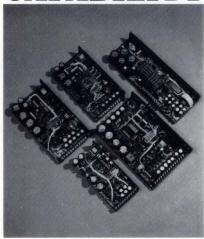
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115/230V user selectable input

20 msec hold-up time standard for 50 Hz applications

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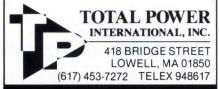
Less than 10 µA leakage for medical use

UL, CSA, VDE design offers onboard EMI/RFI filtering

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custom designs welcome

For information on these please call or write



#### UPCOMING MEETINGS

(continued from p. 149)

5th Beama International Electrical Insulation Conference, May 19-22. Metropole Hotel, Brighton, England. Mike Cavanagh, Beama Ltd., 8 Leicester St., London WC2H 7BN England; (01) 437-0678.

SEMICON/West '86, May 19-22. San Mateo Fairgrounds and Bay Meadows Race Course, San Mateo, CA. SEMICON/West '86, Mathews & Clark Communications, 410 Cambridge Ave., Palo Alto, CA 94306; (415) 327-3721.

6th International Conference on Distributed Computing Systems, May 19–23. Hyatt Regency Cambridge, Cambridge, MA. DCS-6, IEEE Computer Society, 1730 Massachusetts Ave. N.W., Washington, D.C. 20036; (202) 371-0101.

38th Annual National Aerospace and Electronics (NAECON '86) Conference & Exhibition, May 19–23. Dayton Convention Center, Dayton, OH. NAECON '86, William R. Baker, IEEE, 655 Ridgedale Rd., Dayton, OH 45406; (513) 255-6548.

2nd International Computer Applications in Production and Engineering (CAPE '86) Conference & Exhibition, May 20-23. Bella Center, Copenhagen, Denmark. Peter Falster, Conference Chairman, CAPE '86, DIS Congress Service, 48 Linde Alle, DK-2720 Vanlose, Denmark; 45-1-71 22 44.

Techex '86 Americas, Technical Developments Exposition, May 20–23. Expo Center, Orlando, FL. Anne E. Klenner, Dr. Dvorkovitz & Associates, P.O. Box 1748, Ormond Beach, FL 32075; (904) 677-7033.

1986 International Symposium on Multiple-Valued Logic, May 26–28. Virginia Polytechnic Institute and State University, Blacksburg, VA. Dr. Joseph G. Tront, Symposium Chairman, ISMVL-86, Dept. of Electrical Engineering, Virginia Polytechnic Institute, Blacksburg, VA 24061; (703) 961-5067.

AUTOMACH Australia '86, Automated Integrated Factory Focus Conference & Exhibition, May 26–29. Hilton International Sydney and the Royal Hall of Industries on the RAS Showgrounds, Sydney, Australia. AUTOMACH Australia '86, Adolph Greco, A. Greco & Associates Ltd., Integrated Project Management Services, P.O. Box 68, Pennant Hills, 2120 N.S.W., Australia; (02) 875-2377.

1st Annual High Frequency Power Conversion Conference & Exhibition, May 28–30. The Cavalier Resort, Virginia Beach, VA. Sam Davis, Conference Director, c/o Intertec Communications, 2472 Eastman Ave., Bldg. 34, Ventura, CA 93003; (805) 658-0933.

40th Annual Frequency Control Symposium, May 28–30. Marriott Hotel, Philadelphia, PA. Dr. J. Vig, U.S. Army Electronics Technology & Devices Lab, ATTN: SLCET-EQ, Fort Monmouth, NJ 07703; (201) 544-1510.

1986 VLSI Technology Symposium, May 28–30. Hotel Intercontinental, San Diego, CA. Moiz M. Beguwala, Program Chairman, Rockwell International, MS 501-369, Semiconductor Products Division, 4311 Jamboree Rd., P.O. Box C, Newport Beach, CA 92660; (714) 833-4712.

3rd International VLSI Multilevel Interconnection (V-MIC) Conference, June 9-11. Santa Clara Marriott Hotel, Santa Clara, CA. Dr. Thomas E. Wade, General Chairman, IEEE VLSI Multilevel Interconnection Conference, College of Engineering, University of South Florida, Tampa, FL 33620; (813) 974-3786.

1986 National Computer Conference & Exhibition (NCC '86), June 16-19. Las Vegas Convention Center, Las Vegas, NV. NCC '86, American Federation of Information Processing Societies (AFIPS), 1899 Preston White Dr., Reston, VA 22091; (800) NCC-1986.

23rd Design Automation Conference & Exhibition (DAC '86), June 29-July 2. Las Vegas Hilton, Las Vegas, NV. DAC '86. Donald E. Thomas, Program Chairman, IBM Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY 10598.



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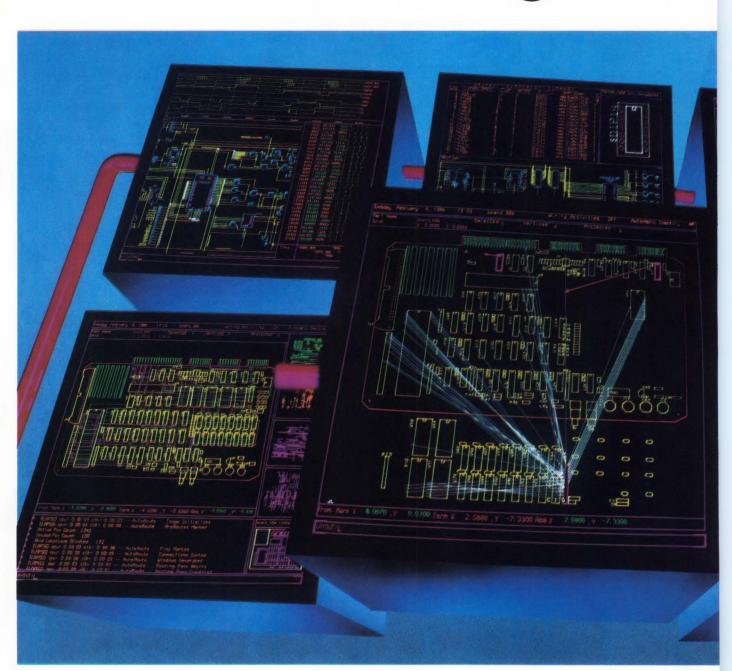
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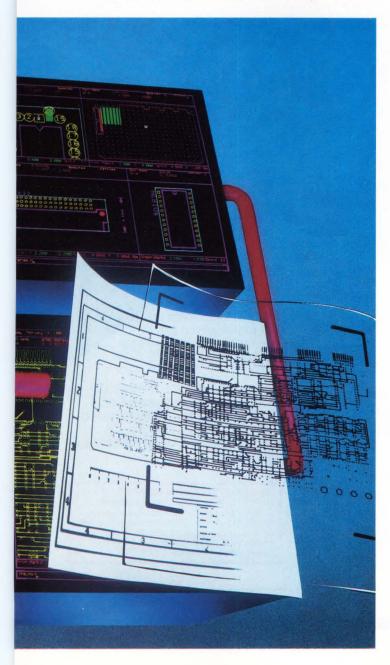
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egarded as the Holy Grail by some and as a fraud by others, silicon compilation is in the midst of an identity crisis. Just as software compilation freed the programmer from worries about the zeroes and ones of machine code, silicon compilation set out to bypass an IC designer's concern with mask geometry. But whereas Fortran permit any engineer to write programs, silicon compilation has not lived up to an equivalent goal — to let any system engineer design his own ICs.

In fact, silicon compilers have been oversold. Enthusiasm for the new technology has given way to the sobering realization that during the learning phase, this marvelous productivity-enhancement tool can indeed curtail productivity. Furthermore, users have discovered the hidden expenses of silicon compilation, namely, costlier chips and slower deliveries than with, say, gate arrays. But then, early language compilers also produced inefficient — in other words, costlier — code.

Nevertheless, silicon compilation will eventually prevail for several reasons:

• Whether the compiler is used by IC or system

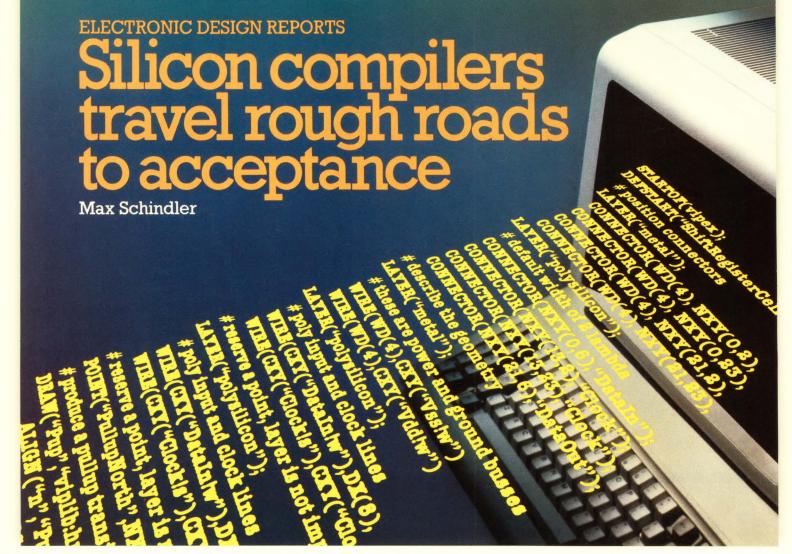
designers, it can raise productivity.

- Even when compiled ICs are not of production quality, they often suffice for rapid prototyping.
- The most glaring shortcomings of today's compilers are under vigorous attack, and some solutions already approach the test phase.
- As IC complexity grows, compilers will turn from simply a desirable extension of standard CAE tools into an absolute necessity.

To sift through the confusion that surrounds silicon compilation, a clarification of the term is in order. Following that, comes a review of the compiler types in production, with an eye to their shortcomings. Some specific problems — and their solutions — stand out: the impact of IC processing on design, the issue of testability, the rising demands on simulation, and the search for adequate hardware description languages.

As the spectrum of compilation techniques unfolds, it will become clear that one company's compiler is another firm's assembler. Vendors and users debate not only what constitutes a desirable degree of design automation, but also how the user should interface with the compiler.

Dave Johanssen set the direction for the new in-



dustry. With his doctoral work at Caltech and his subsequent founding of Silicon Compilers Inc., his definition of silicon compilation warrants special attention. In his view, a silicon compiler must accept an architectural specification for an IC and successively refine it at the block, logic, circuit and layout stages of design. He demands that a compiler support not only the functional and geometric views of a design, but also its performance and test aspects. The design's integrity must be verified at all levels—from logic and timing behavior to topological and electrical characteristics.

Johanssen regards compilation more as a methodology than simply another CAE tool. But the actual compiler functions can be understood more easily by plotting them on the Y chart, introduced by Daniel Gajski at the University of Illinois. The chart connects three representations of an IC (Fig. 1a): functional (expressed by a hardware description language), structural (the circuit and block diagram), and geometrical (the layout). The most detailed levels of description appear near the junction of the axes—for example, transistors and polygons.

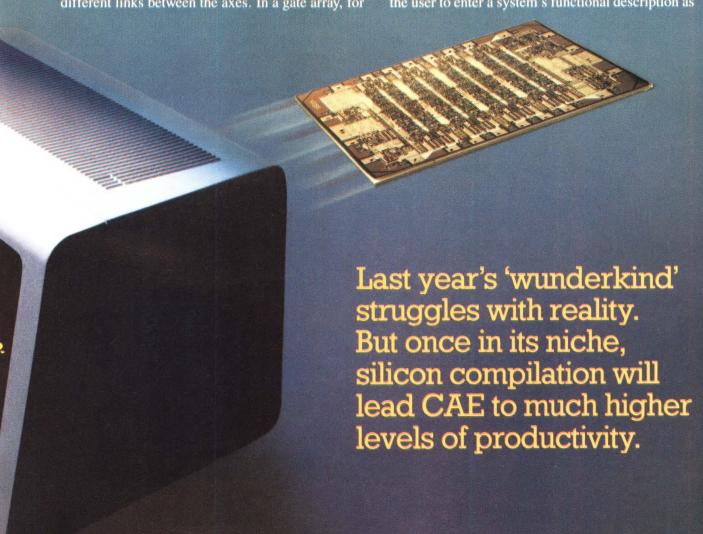
Different design methods appear on the Y chart as different links between the axes. In a gate array, for

example, the designer builds up increasingly higherlevel functions starting with gates (Fig. 1b). Translation to the geometric level is already built into the array. Simulation usually proceeds at the gate level, although functional simulation is possible.

For the silicon compiler methodology, the graph looks quite different. A compiler's designer usually provides generators, which can translate functional descriptions at different levels of detail into geometric descriptions (Fig. 1c).

Perhaps the purest compiler is MacPitts, designed at the Massachusetts Institute of Technology. It accepts a programlike system description — say, for an 8086 — from which it automatically synthesizes the logic structure and, without further intervention, produces mask tapes. Though a commercial version of MacPitts was available, it proved too far removed from the real world. The logic synthesis step was especially restrictive, because it permitted only one silicon implementation for any given function. Today's compilers can transform one model into many silicon implementations. (For a list of participants in the silicon compiler contest, see the table.)

Silicon Compilers' Genesil, for example, permits the user to enter a system's functional description as



### **Electronic Design Reports** SILICON COMPILATION



a structural representation of, say, CPU, RAM, ROM, and I/O port. The user frequently remains involved in floor planning, the highest level of the geometric representation. Based on Genesil's knowledge of the desired technology and on user-defined inputs and outputs, the compiler begins to construct a gate-level circuit and its silicon implementation. The latter is needed even in the early design stages to calculate delays and power consumption. Unlike MacPitts, Genesil is interactive, enabling the user to examine and change the circuit at any level of abstraction.

Nevertheless, among commercial compilers Genesil comes closest to Johanssen's definitions. Take a datapath module whose steering input STDIN\_1 is first defined as a constant. In the corresponding schematic, the constant input is identified as a small rectangle labeled INTER0\_ST1 (Fig. 2). When the user changes the input to EXTERNAL and gives it the name INTERO\_EXT1, the schematic automatically reflects the change (highlighted inset, Fig. 2).

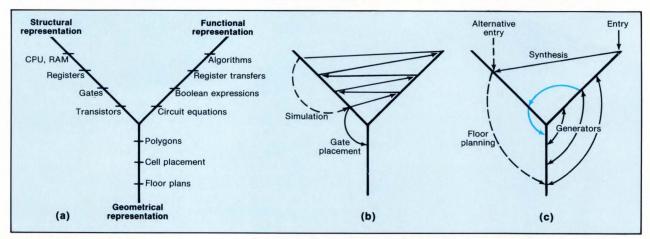
To produce new feedback for the user, Genesil recompiles the circuit and simulates the new version. Because compilation takes less than a minute for 1000 transistors on a MicroVAX II, simulation—consuming 80% of the CPU's time—determines the system's reaction speed. Unfortunately, accelerators have been of little help to ease the burden because setup time becomes the dominant factor. A nominal acceleration factor of 1000 can thus drop to as little as 10.

The second popular compiler, Seattle Silicon's Concorde, proceeds in a more pragmatic fashion. Its component classes are more rigidly defined, so that the user need only fill in a "data sheet" on the screen. This practice is familiar to users of parameterized standard cells or even of standard MSI-components. In fact, a new feature dubbed cell immigration permits the mixing of compiled and standard cells, many equivalent to TTL components. The Concorde runs on Mentor, Tektronix, and Valid workstations and is usually tightly integrated. To hide the interface with the host, for example, Valid Logic implements its own migration facility for foreign cells (Fig. 3). However, use of Seattle Silicon's editor permits Valid to benefit from the compiler's new autorouter, which can zip through 25,000 transistors in 4 minutes.

### CHIP OFF A NEW BLOCK

Last year a radically different approach to silicon compilation made inroads in the ASIC industry. Instead of offering users a set of module generators, the new school gives them the tools to build their own generators. Silicon Design Labs exemplifies this approach with its Generator Development Tools system (ELECTRONIC DESIGN, Nov. 28, 1985, p. 97). With it, users can build, or compile, a library of modules of increasing complexity to suit their specific needs.

The "compiler-compiler" school primarily addresses the interests of IC designers, not system designers. The former number somewhere between 2000 and 4000, while the latter have been estimated anywhere from 300,000 to 500,000. Such a large market attracts venture capital, but gaining converts among these engi-



1. The Y chart represents three views of integrated circuits (a). A gate-array design alternates between the structural and functional view in a bottom-up fashion (b). Silicon compilers, on the other hand permit two top-down entry points (c), leading to successive refinement steps (colored arrows). Functional and geometric representations are interconnected by ready-made generators.

neers is more difficult. Silicon Compilers, for example, has so far shipped fewer than 100 of its compilers to system designers, even though Genesil is most attuned to their needs.

The fact that all compiler vendors now offer generator development tools lends some credence to the approach. Silicon Compilers' Genesis, Seattle Silicon's compiler development system, and SDA's structure compiler all toe the compiler-compiler line. The development is reminiscent of the fledgling AI industry's discovery that expert system shells are more salable products than full-fledged expert systems.

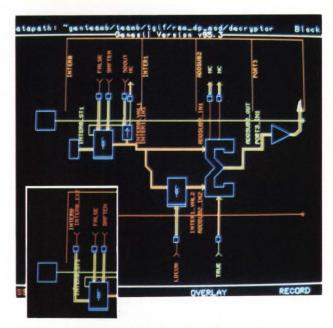
However, silicon compilation faces harsher judgment than did expert sytems, because well-proven alternative technologies exist and are hard to topple. System designers are comfortable with existing merchant chips and MSI (or SSI) component libraries. Frequently, a microprocessor or microcontroller is connected to peripheral chips through MSI glue logic. A system can be upgraded rather painlessly by replacing the glue logic with programmable logic arrays.

### WHO NEEDS IT?

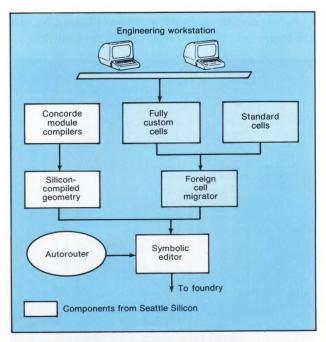
The customization of CPUs and peripheral chips has often been brandished as the only way for system houses to stay competitive. Though a board packed with 100 chips—CPU, glue logic, and more—could conceivably be replaced with a single custom chip, most designers prefer to retain standard CPUs and convert the remaining circuitry into a handful of gate arrays. Even when customized processor chips are really needed, silicon compilation faces growing competition. Users seem to prefer core processors or similar megacells, which afford comparable rewards without the risk of venturing into the uncharted waters of CPU compilation.

If a system designer could buy a compiler that automatically converts a board full of TTL ICs into a single CMOS chip, he might give it a try. But even compilers that claim technology independence cannot use an existing net list or parts catalog to transform TTL logic into MOS logic. Worse yet, for the top-down redesign of glue logic alone, compilers offer little incentive, because few handle random logic well. Die size savings may be irrelevant, too, when the often high number of connections determines the glue chip's size. Furthermore, logic arrays save time—important for small system vendors who often rely on random logic to implement proprietary concepts.

A large vendor, on the other hand, has its own IC designers, and more likely than not, will choose a PLA for fast response, followed by a custom chip to optimize



2. Silicon Compilers' Genesil automatically converts architectural user definitions into registerlevel schematics. A change in the definitions leads to an equivalent change in the schematic (highlighted inset).



3. In Valid Logic's Scaldstar workstation, Seattle Silicon's Concorde is closely integrated with resident libraries. Consequently, standard and compiled cells can be combined in the same chip.

### **Electronic Design Reports** SILICON COMPILATION



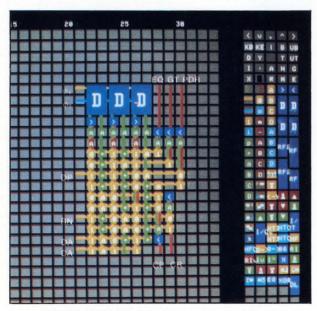
price and performance. Another alternative lies in standard cells that correspond closely to the TTL components.

Furthermore, large system houses consult their IC designers before they buy compilers. The judgment is often less than flattering: "They predict at most a 10% size penalty," says one compiler vendor, "but when you're done, the chip is 40% larger and 50% slower." Getting a design to market six months late may eradicate 33% of the potential profit, but IC designers know that 12% higher production costs will do the same. And chip costs rise exponentially with die size, practically ruling out most compiled ICs.

### IT'S MAGIC

The IC gurus may be small in number, but they wield a great deal of influence. "A system designer with a good compiler may be able to solve 90%, even 95% of the problems," confides one, "but the last 5% are pure magic." Some of the magic is knowing your foundry. In fact, process variations often prove the downfall of compiler projects, so compiler vendors tend to work closely with specific foundries. Often they are one and the same, as in the case of Cirrus Logic, Cademic, VLSI Technology, and LSI Logic.

Purists may frown on the inclusion of Cirrus, because the company implements logic in "storage logic arrays,"



4. The Cirrus methodology lets the user compose circuits with a displayed "alphabet" of icons (top, right screen edge). The displayed circuit module corresponds to the logic diagram of a vending machine, as described in the test.

or SLAs. The array looks similar to a sea of gates—a gate array without routing channels (Fig. 4). Because the user assembles logic from an "alphabet" of about 30 primitives (at the screen's right edge), it may be correct to call the process silicon assembly. But, on the other hand, the term gate-array compiler has become quite acceptable. Cirrus believes that its approach is more cost-effective than standard cells or megacells for a chip that carries 5000 to 10,000 gates and is used in quantities of at least a few thousand a month.

The example shows part of the logic for a soda-pop vending machine. The inputs, CP, CR, PDR, GT, and EQ report the machine state (coin present, changer ready, and so on). After inverters produce the complement for three of these inputs, all signals are fed to nine AND gates. Some of their outputs activate the machine (RN returns a nickel and DP drops the soda can). Others feed into three OR gates, which in turn set the flip-flops that are labeled D and driven by a two-phase clock. A user would normally work from a state chart or a state map to design the SLA.

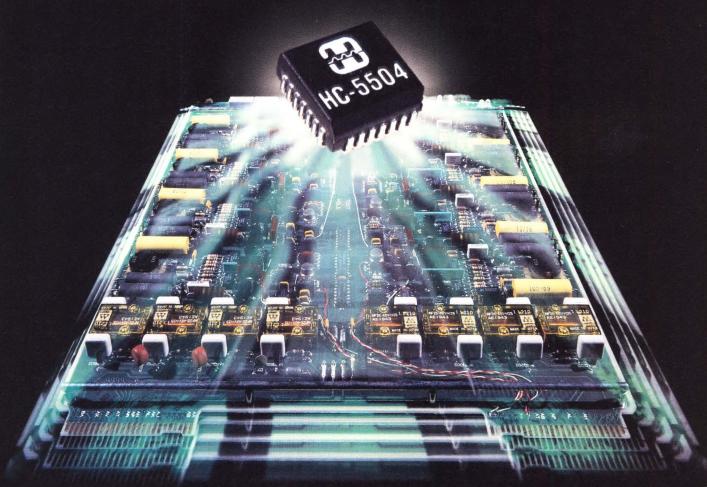
Whatever the implementation technique, the distinction between foundries and compiler service firms (which rarely sell the compilers by themselves) is largely outdated. Rather, a term like ASIC house should be used to describe vendors that serve both purposes. In fact, these companies have more or less replaced foundries because, as one engineer puts it, "a CIF tape is not an adequate umbilical cord between designer and implementor."

### DOING IT RIGHT

Today, "first silicon" success is almost taken for granted. LSI Logic, for example, states that 97% of its 2500-plus designs work the first time. To keep the promise of first silicon, the ASIC designer and foundry must cooperate. For one thing, test procedures cannot be established from mask generation tapes—a functional description is needed. For another, designing testability into a chip via compilation is a tough proposition. Silicon Compilers has added a testability compiler to Genesil that supports such methodologies as signature analysis or levelsensitive scan detection (LSSD), but most IC designers decry the penalty in die size imposed by the necessary testability structures.

European firms like Philips or Plessey appear to hold the lead because they are more geared to consumer products. Plessey operates a foundry in California and offers self-testing capabilities for both megacells and "paracells" (parameterized microcells). The approach reduces testing for a 50,000-gate chip to a few seconds on the average. However, self-testing is inherently limited to

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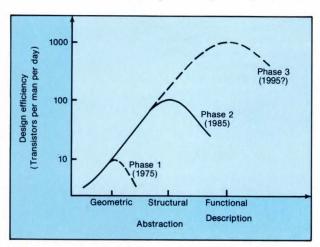
synchronous circuits.

Testing naturally gets even more difficult as circuit size increases. For data-path chips, functional testing may become the only viable alternative. A test language that is consistent with the hardware description language then becomes important. For example, VLSI Technology's language, VTI-test, meshes well with the Mainsail-based description language. It incorporates two important operators, one for setup (<-) and the other for test (->). For a simple NAND gate, part of the test program reads as follows:

```
CYCLE set_inputs (InBus, OutVal);
ln < -lnBus @beg_cyc;
Out -> OutVal @ end_cyc;
END:
FUNCTIONTEST quickTest;
BEGIN
Set_inputs(15,0);
Set_inputs (3,1);
END
```

Here, quickTest checks the basic NAND function; the first line applies all 1s to the 4-bit bus to obtain a 0 at the output, while the second applies 0011 (binary) to obtain an output of 1.

Another ASIC house, SDA Systems, plans to control both simulation and test with one language, STL. It will match the C-inspired description language Skill, which is quite comprehensive because SDA, like Silicon Design Labs, subscribes to the compiler-compiler dogma. How-



5. IC design efficiency increases as the designer applies high-level abstractions. At present, the structural approach is giving way to a functional description.

ever, SDA also offers a module library, a task that the other company has just started.

Recently, SDA introduced two other important software tools, Extract and LVS (layout vs schematic). The former extracts a schematic from the layout and feeds it to the simulator. The latter, a circuit reconstruction program, compares the layout with the schematic and highlights any differences. The circuit parameters and the parasitics both can be compared. Such programs are fairly common for ASIC design; as a generic term for circuit reconstruction, network vs layout, or NVL, is often used.

Only a few years back, network-vs-layout software was declared superfluous by design automation gurus. After all, a circuit designed by a computer simply had to be correct. Since then, IC designers have found that bits can get lost on phone lines and even in data bases. Do-ityourself silicon compilers add another hazard, and even professional compiler writers welcome an NVL check after changes have been made. Because changes never cease, the routine usually runs indefinitely.

Circuit reconstruction works well for small schematics because they can easily be flattened; but upper hierarchical levels have yet to be addressed. Still, network-vslayout routines provide a safety net for those who must tinker with a silicon compiler to optimize it for their needs. Most IC designers fall into that group, since they are anxious to boost their productivity, provided the size and speed penalties associated with a compiler are tolerable.

Tinkering also pays off because compiled circuits are usually overdesigned with extra buffers and control lines to interface smoothly with other automatically generated components. An IC-literate designer can excise the unneeded baggage and stay ahead of someone going the fully custom route. The first MicroVAX CPU, for example, was designed quickly with a compiler. The second generation, hand-tuned for performance, turned out to be nearly three times faster. The difference will be much smaller once less rigid compilers can be used.

### **UNEXPECTED ALLIANCES**

With the exception of Silicon Compilers, which sold 95% of its products to system designers, all interviewed companies report that IC engineers make up one-third to three-quarters of their clientele. The waxing cooperation between the two parties is bound to yield more sophisticated compilers. In fact, many of the users come from the leading edge of IC design, namely, VHSIC projects. On one hand, they are more willing to trade off speed for cost (few VHSIC chips ever reach even moderate volume); on



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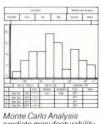
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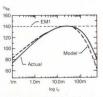
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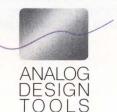
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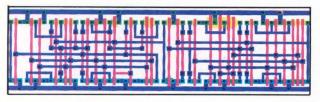
the other hand they work closely with system designers, the real targets for silicon compilation.

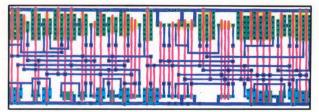
Many engineers expect a quantum leap in design automation from this cooperation, especially in the upper hierarchical levels. There functional modeling poses a major roadblock, which may fall if the Pentagon has its way. Not only is the DOD pressing hard for its Ada-like VHDL description language, within a few years it plans to require that all chips it buys come fully characterized in VHDL. Thus, functional models will eventually be available for all ICs used by the military.

When the modeling roadblock falls, we may cross the threshold to the third phase of IC design, which will emphasize functional rather than geometric or behavioral circuit descriptions (Fig. 5).

Whether VHDL can adequately address CPU parallelism, a vital concern of companies like Silicon Solutions, remains to be seen. In designing the accelerators it sells, the company uses its own compilers, essentially starting with the Mead-Conway implementation called Bristle Blocks, followed by compaction. But designers trying to express parallelism in a functional IC description encounter the same difficulties as the designers of computer languages did.

That problem has been solved by the Occam language, which was developed specifically for the Inmos Transputer, a CPU meant to operate in parallel. With hundreds of CPUs ganged together, the Transputer indeed works as planned. Now a superset of Occam is being used as a





AT&T's Tilos and SC-2 programs here select different transistor sizes for a 2-bit adder, depending on the maximum tolerable delay. At the top, the user has requested 10 ns, at the bottom 4 ns.

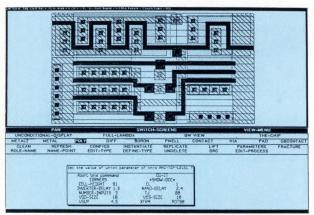
hardware description language at Inmos' UK laboratories, primarily for the design of Transputer variants. For example, the following code defines parallelism in a pipelined processor:

### WHILE TRUE

PAR — execute these tasks in parallel: bitOfPipe (in, interPipe(0)) PARi = 0 FOR (number Of Stages - 2)bitOfPipe(interPipe(i), interPipe(i+1)) bitOfPipe (interPipe (numberOfStages - 1), out) : -- end of complete pipeline model

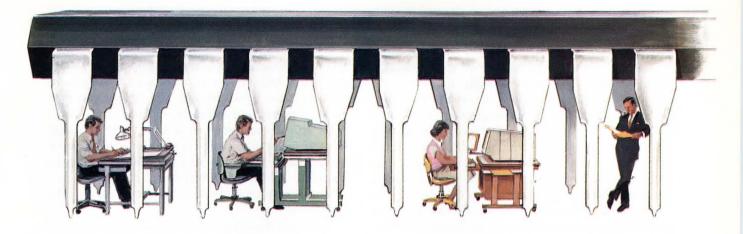
That compiled circuits can surpass manual designs in specific applications has been clearly demonstrated. LSI Logic recently announced its Macgen package, which lays out multiplier-accumulator chips (ELECTRONIC DESIGN, April 3, 1986, p. 51). By concentrating on the Wallace-tree algorithm and by cleverly folding the compiled layout, the resulting chip is both dense and fast—2.5 times faster than other multipliers. Most remarkable, the designer knows neither the schematic nor the layout of the resulting circuit—a hallmark of true compilation. "It could take a year to derive the full schematic," comments the compiler's architect.

Another widely "unknown" ASIC house also reports noteworthy results—AT&T's facility in Allentown, Pa. Compared with standard cells, the SC-2 "silicon converter" not only saves 10% to 20% in die size, but produces either twice the throughput or three to four times the out-



7. A gate sizer developed at Gould-AMI can produce bent-gate transistors to save silicon space. Of the four dark horizontal lines that represent transistors, three use bent gates.

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CIRCLE 81

### **Electronic Design Reports** SILICON COMPILATION



put power for digital signal processors. If speed is essential at a given location, the Tilos (timing logic simulator) package changes transistors accordingly (Fig. 6).

Gould-AMI adds a wrinkle of its own to gate sizing: space-saving folded transistors that can save over 20% of a chip's real estate (Fig. 7). In the procedural languages used for most CAE software, the folding algorithm would be difficult to implement. But AMI has switched to Lisp for its software development and now reports about a threefold speedup in the construction of CAE tools.

To deliver the flexibility it promises, silicon compilation will likely have to call on expert system technology. Lisp and other AI languages will, of course, figure dominantly in expert systems for IC design now under development at university and industry laboratories. AT&T's Bell Laboratories, for example, has two such efforts under way. One is the Design Automation Assistant (DAA), born at Carnegie-Mellon University. Though still experimental, the tool blends OPS-5 rules (currently about 700) with algorithmic modules written in C (encompassing 20,000 lines). DAA's designers hope to broaden the narrow confines of present silicon compilers, thereby eliminating many of the shortcomings.

Another Bell Labs effort, dubbed Cadre, has barely outgrown its baby boots. It concentrates on the lower abstraction levels of IC design (from register transfer on down) and could therefore eventually use DAA outputs as its inputs. Unlike a single expert system, Cadre will comprise a collection of small expert "agents," all coordinated by a manager agent, which implements the system's metarules.

One area of silicon compilation not addressed by expert system could use the help of one—analog circuitry. ASIC houses are, however, aware of the need to address the problem. Some report that over 50% of their customers are anxious to put analog functions in their chips.

Describing such functions in a high-level language, however, seems to be a long way off. Although Seattle Silicon and SDA offer analog cells, true compilation remains a problem. Unlike digital components, analog circuitry is hard to classify, except for some specialties like switchedcapacitor filters.

You might think that operational amplifiers also can be characterized easily, but Martin Walker from Analog Design Tools disagrees: "I can think of at least six distinct classes of op amps, and some demand rather esoteric design knowledge—for example, which transistors must be placed in isotherms." In fact, finding those lines of equal temperature on an IC is quite a feat in itself.

Even in the digital field, the first step of transformation—synthesis— remains largely unsolved. Gateway Design plans to tackle the problem because it considers compilation impossible without synthesis. As company president Prabhu Goel explains: "Without logic synthesis, you don't have a compiler, you have an assembler. All the transformations are essentially 1:1 translations of the 'machine code' of a manual layout."

A compiled computer language like Fortran, on the other hand, is completely independent of the underlying hardware. But since IC design deals strictly with hardware, we can only wonder whether a CAE "Fortran" will even become a reality.

### Players in the silicon compiler game

#### Analog Design Tools Inc. 66 Willow Pl. Menlo Park, CA 94025 (415) 328-0780 CIRCLE 451

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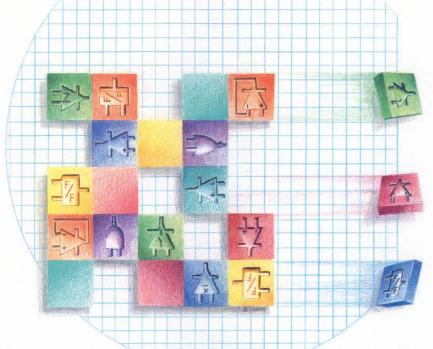
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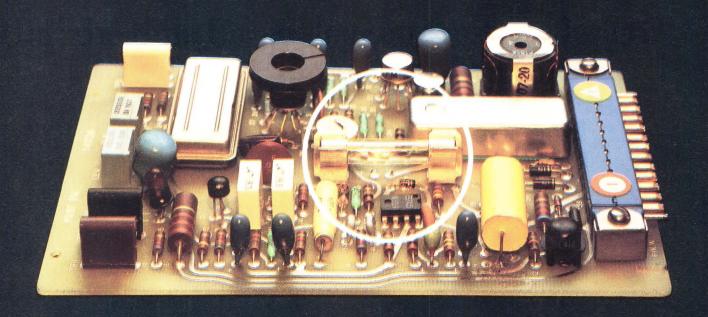
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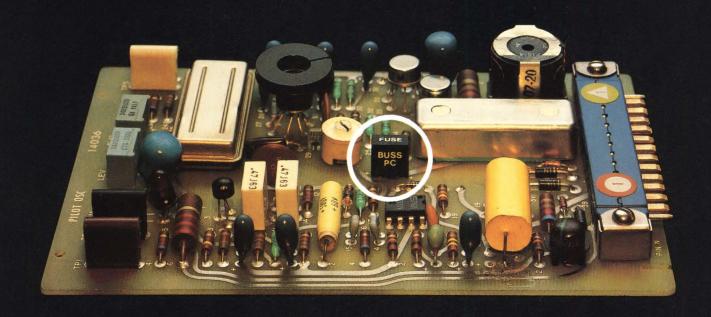




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### **DESIGN ENTRY**

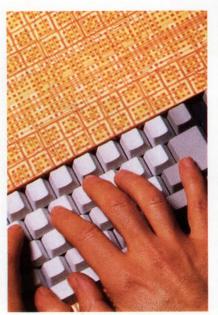
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In the digital world, gate-array designers frequently brag about using 90% of a chip's active silicon. Analog array designers have not been so lucky: Rarely can they employ even half the active silicon. The reasons for such inefficient use of silicon are complex and interrelated, but they boil down to this: Analog array designers do not have the freedom to have npn and pnp transistors exactly where they need them. As a result, they

often must opt for slow, expensive fully custom chips or hybrids to

satisfy the application at hand.

The development of the Flexible Array architecture—as well as the Beta array family that implements it—puts to rest the worries of analog array designers. Besides evolutionary changes, the architecture stands out for one revolutionary concept: Each active device prediffused on the chip can be wired during metallization as either an npn or a pnp transistor. Moreover, some devices can be connected as resistors, others as capacitors. The Flexible Array goes a long way toward conserving the chip space wasted by unused components, a common complaint in analog array design. In fact, silicon use can jump to 100%.

At first glance, the chip's regular structure resembles that of the latest analog arrays. Both are laid out in well-defined grids, both work on the basis of cells, and both invite the use of complex macrocircuits (ELECTRONIC DESIGN, June 13, 1985, p. 86). Now the differences start: Whereas the older chips comprise about a dozen large, identical cell "tiles," each capable of holding a complex circuit like an op amp, the largest Flexible Array chip carries 80 small cells, each of which can be independently configured. Moreover, macrocircuits in tile-type analog arrays may eat up one cell plus a portion of a second cell, leaving the remainder of the latter vacant. With the new array, macrocircuits can be positioned anywhere on the chip, consuming only the number of cells needed and sacrificing at most one or two active devices.

To define the purpose of each chip, designers have three multifunction structures, or "mutants," at their disposal (Fig. 1). At the

### **DESIGN ENTRY**

### Cover: Space-efficient analog array

center of each small cell are three devices, each called a Twinstor. (The Beta-240, the largest chip in the series, carries 80 cells and hence 250 Twinstors.) Each Twinstor can be connected during metallization as a pair of npn transistors, a pair of pnp transistors, an npn transistor and a crossunder, or a three-terminal pnpn switch. In addition, each cell contains 23 resistors, about equally divided into groups at each end of the cell. Another multifunction structure, a Twinbooster, resides at one end of the chip. A power device, it handles up to 500 mA when connected as an npn transistor or up to 50 mA as a pnp device.

The most interesting mutant structure, the Padstor, combats the high percentage of unused silicon on the periphery of a chip. It incorporates the material surrounding and beneath the bonding pads; with functional devices now moving onto the chip's periphery, Flexible Array chips can reach a remarkable usage factor of 100% or more. Besides its basic use as a pad, the Padstor can double as a vertical pnp or npn transistor, as a junction or oxide capacitor (or both in parallel), or finally as a crossunder.

#### STRUCTURAL EFFICIENCY

Because of its sheer number on chip, the Twinstor acts as the basic building block, whether designers work at the device level or at the macrocircuit level on a workstation. At the system level, they need not be aware of its existence.

By far, versatility is the most salient characteristic of

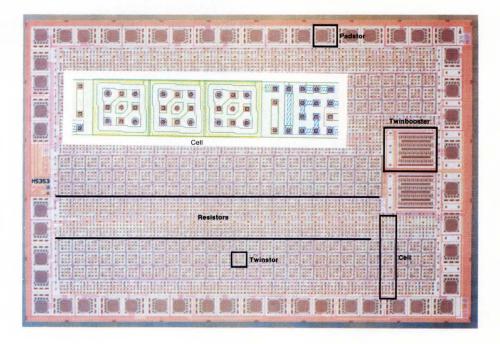
the structure, since it can be connected as two transistor types. Contacts C<sub>1</sub> and C<sub>2</sub>, which are built with the same n-type diffusion, are connected internally as common collectors in an npn configuration, but become the common bases in a pnp configuration.

As a dual, vertical npn transistor (Fig. 2a), the device may be used in any common circuit as a single transistor with its bases and emitters tied together. In two alternative setups, it serves as two transistors, effectively increasing the number of active devices—and hence the functional scope—of the chip. The Twinstor can be wired as a pair of emitter-followers, with separate base inputs and emitter outputs, or show up in a Darlington circuit, with the emitter of one transistor driving the base of the other ( $E_1$  tied to  $B_2$ ). In the latter two cases, 200 Twinstors can replace as many as 250 transistors on a standard array. Furthermore, one complete device occupies only 75% the area of one typical npn transistor.

#### **LEADING TWO LIVES**

When a pnp transistor is needed, a Twinstor can form a single-base, dual-collector lateral pnp device. Doing so involves converting the p material forming the bases of the npn transistors into collectors (Fig. 2b) and the n-type material used for the collectors into the base. At the center of the device, a separate p-type diffusion makes up the emitter. When connected by metal as a pnp transistor, either the device can be used singly (with its collectors tied together), or each collector can independently drive a different load.

1. Three "mutant" structures, as well as two banks of resistors. characterize the Beta-240, just one of the chips implementing the Flexible Array architecture. As is the case with other chips in the series, each cell (see inset) incorporates three Twinstors. During metallization, a Twinstor can be connected as an npn or a pnp transistor.



The p material for the npn bases is L-shaped for the most compact geometry. If the Twinstor is not needed as an active device, the dual contacts permit it to act as matched low-value resistors or as crossunders.

When connected as an npn transistor, the Twinstor has the same operating characteristics as those in present arrays, but it handles triple the current for the same emitter area. (The credit goes to the dual-base contacts and the larger emitter perimeter facing the contacts.) When both halves are tied in parallel, current handling doubles. That is, a Twinstor can handle about six times the current of a typical analog-array npn transistor.

In addition, an independent metal line can be routed between each base and emitter contact, simplifying interconnections both inside Twinstors and between them. Further, the device is fabricated with deep sinker diffusion, just as in most bipolar processes; as a result, its saturation resistance drops by a factor of 10, reaching about  $20 \Omega$ .

Price and availability

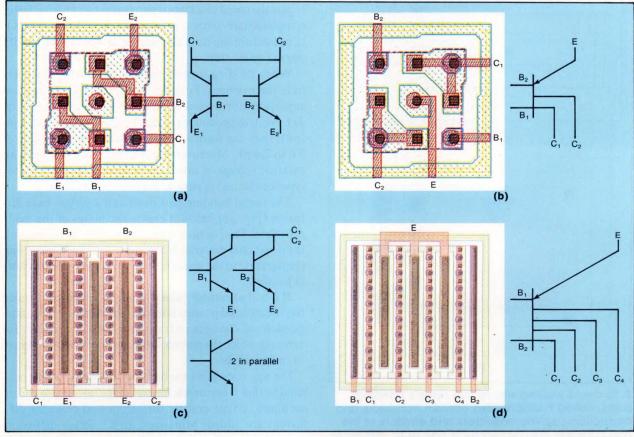
The Beta family of analog array chips has a turnaround of three weeks. Nonrecurring engineering costs range from \$4000 to \$9000, depending on the complexity of the device.

CIRCLE 504

Similar advantages accrue when the Twinstor is connected as a pnp structure. The second collector contact lowers saturation resistance, while the emitter shape doubles the emitter perimeter, in turn doubling current handling. Finally, metal runs from the emitter can exit in all directions, simplifying routing.

For extra power, designers can turn to the Twinbooster. Each device is an assemblage of silicon structures that may be connected in parallel to form either a 500-mA npn transistor (Fig. 2c) or a 50-mA pnp transistor (Fig. 2d). In the former configuration, saturation resistance is just 3  $\Omega$ ; in the latter, about 20  $\Omega$ .

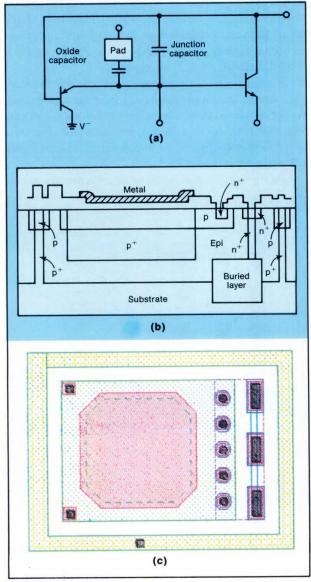
As an npn device, the Twinbooster implements a pair of



2. The Twinstor represents the basic building block of the programmable arrays. At the designer's discretion, it can be connected as either one or two npn transistors (a) or as a dual-collector pnp transistor (b). Power on the array is handled by a mutant structure called a Twinbooster, which handles 500 mA as an npn transistor (c) and 50 mA as a pnp transistor (d).

### Cover: Space-efficient analog array

Table 1. Inside the Flexible Array family				
Device type	Beta-240	Beta-180	Beta-100	
Cells	80	60	33	
Twinstors	240	180	99	
Padstors	40	38	28	
Twinboosters	2	1	1	
Die size	110 × 160 mils	110 × 122 mils	110 × 79 mils	



3. To avoid wasting silicon, the array's bonding pads, called Padstors, also contain transistors and capacitors (a). The collectors and emitters of the npn transistor are formed by a pair of n<sup>+</sup> diffusions (b) and correspond to the circles and bars shown in the chip plan (c). The capacitors can serve to stabilize op amps or as hold capacitors in sample-and-hold circuits.

250-mA emitter-followers with separate inputs,  $B_1$  and  $B_2$ , and separate outputs,  $E_1$  and  $E_2$ . When set up as a pnp transistor, it can work as a quad collector driving up to four different loads—for example, providing four equal current sources from a single reference input.

### WHAT A PAD

For chameleonlike performance, the Padstor cannot be surpassed. Few designs require more than a handful of bonding pads—several inputs, several outputs, power rails—and even fewer would need the Beta-240's full complement of 48 bonding pads (Table 1). Thus, if not for the Padstor, many applications might waste as much as 10% of the chip.

Moreover, the Padstor adds capabilities not found on earlier arrays—voltage-insensitive oxide capacitors and vertical pnp transistors. The first not only stabilize op amps but also can be used as hold capacitors for sample-and-hold circuits. The vertical pnp transistor, a rarity with all but the highest performance bipolar processes, triples the speed of a lateral pnp transistor, making faster complementary circuits a possibility. In addition, the Padstor structure can form a resistor or an npn transistor with one to five emitters.

When building capacitors with the Padstor, designers have three options. First, they can set it up as a junction capacitor with a fixed value of 4.5 pF at zero bias (Fig. 3a). Next, depending on oxide thickness (under user control), they can form an oxide capacitor with a value of 0.6 to 2.4 pF. Moreover, these capacitors can handle an external voltage of over 100 V. Finally, both capacitor types can be tied in parallel for maximum values.

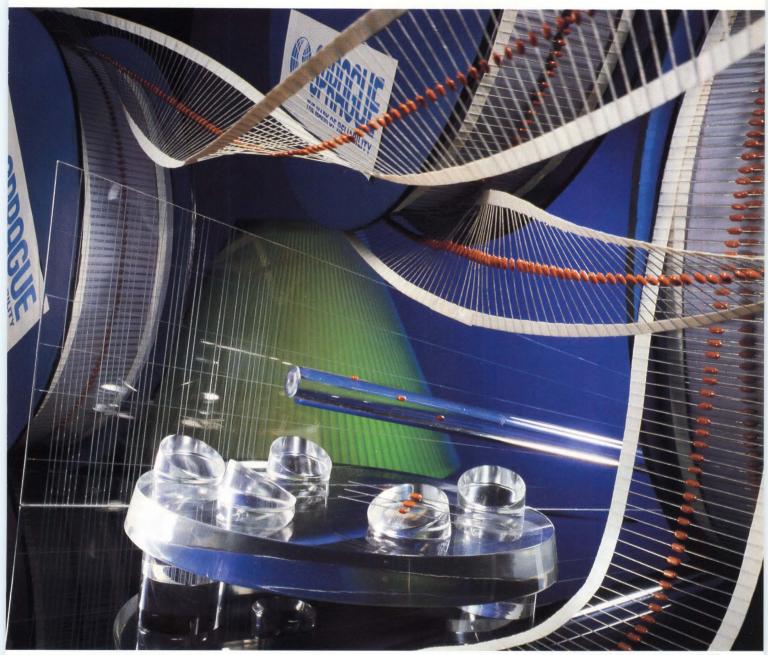
The metal bonding pad itself and a p-type base diffusion (Fig. 3b) below it create the plates of the oxide capacitor. This, in turn, forms a junction capacitor with the n epitaxial material below the diffusions. Connecting the top plate to the epitaxial layer puts the two capacitors in parallel.

If a ballast resistor valued at only a few ohms is called for, the diffused p<sup>+</sup> area does the job. Moreover, it is independent of changes in transistor beta, a problem for arrays in which the emitter diffusion provides the resistors in epitaxial tubs.

The npn transistors are built by diffusing a p base material so that it surrounds the pad (Fig. 3c). At one end of each pad, n-type emitter diffusions and collector diffusions are added. Moreover, an n<sup>+</sup> sinker diffusion connects the collector to the buried layer, minimizing saturation resistance.

The p material under the pad does not go to waste either. It forms the emitter of the vertical pnp transistor,

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### Cover: Space-efficient analog array

while the deep n<sup>+</sup> diffusion for the collector of the npn transistor acts as its base. The pnp device's collector is formed by the p-type isolation material. Since this is a vertical pnp transistor, with a heavily doped emitter and a thin base, it has a typical beta of 50 and an f<sub>T</sub> of 15 MHz—far superior to lateral devices on this or other arrays (Table 2).

With the medium-current npn and pnp transistors in proximity to any point on the array, designers can build complementary class AB amplifiers for output stages. The devices also can act as high-impedance input buffers or be connected in parallel to form a power stage in which heat dissipation is distributed evenly over the chip. In addition, this pn junction can be used as a high-voltage greater than 120 V—transient protection diode for input or output protection. And the Padstor can serve as a zener zap device for precision trimming of passive or active components at the wafer or package stage.

Finally, the bonding pad itself can be used in all of these circuits, as long as its 0.6-µF capacitance, coupled to the p-type material beneath it, does not limit circuit bandwidth.

Although resistors are built into each mutant structure, most of the chip's resistors lie in groups at each end of a cell (Fig. 1 again). All 80 cells in the Beta-240 contain ten

Device	Range or minimum
Twinstor as npn	
Beta when $I_C = 1 \text{ mA}$	100-400
Beta when $I_C = 15 \text{ mA}$	30
Saturation resistance	30 Ω
$f_T$ when $I_C = 3$ mA	600 MHz
Twinstor as pnp	
Beta when $I_C = 10 \mu A$	50-250
Beta when $I_C = 1 \text{ mA}$	10
Saturation resistance	300 Ω
$f_T$ when $I_C = 10 \mu A$	6 MHz
winbooster as npn	
Beta when $I_C = 50 \text{ mA}$	100
Beta when $I_C = 500 \text{ mA}$	30
Saturation resistance	3 Ω
$f_T$ when $I_C = 15 \text{ mA}$	300 MHz
winbooster as pnp	
Beta when $I_C = 1 \text{ mA}$	25
Beta when $I_C = 30 \text{ mA}$	10
Saturation resistance	20 Ω
$f_T$ when $I_C = 3$ mA	2 MHz
adstor as npn	
Beta when $I_C = 5 \text{ mA}$	100
Beta when $I_C = 50 \text{ mA}$	30
Saturation resistance	15 Ω
$f_T$ when $I_C = 15$ mA	400 MHz
adstor as vertical pnp	
Beta when $I_C = 1 \text{ mA}$	25
Saturation resistance	50 Ω
$f_T$ when $I_C = 3$ mA	15 MHz

Note: All specifications given for  $V_{CE} = 5 \text{ V}$ .

### A glimpse at the processing

The Flexible Array chips are fabricated with a standard single-metal bipolar process following 6-µm design rules. A maximum of 26 V can be placed across the supply rails. In addition, a four-step passivation process increases reliability and protection. First, a thermal oxide layer is grown to protect the junctions and to attract residual ionic impurities to the top of the oxide. The impurities are trapped there by a layer of nitride, preventing further contamination. After the metal interconnection layer is deposited, separate oxide and nitride layers are again laid down, leaving only the bonding pads exposed.

500- $\Omega$ , two 1.5-k $\Omega$ , and four 25-k $\Omega$  resistors laid out in matching pairs, with another 500- $\Omega$  and a 25-k $\Omega$  device rounding out the selection. To simplify routing, some of the resistors are positioned at 90° angles, some are parallel.

In addition, each cell contains three low-value resistors (two 20  $\Omega$  and one 25  $\Omega$ ) which can serve as crossunder devices if needed. Unlike most arrays, the deep diffusion forming these resistors is relatively insensitive to electrostatic discharge.

Besides the routing advantages offered by the mutants, the designer's efficient use of the epitaxial and substrate ground lines simplifies the routing process. The epitaxial line is formed by a deep diffusion that reaches the buried layer; a contact to this material can replace a metal interconnection to the plus supply rail. The substrate ground, called the semiground, is reached at the isolation walls that contact the substrate.

Prior to routing, the circuit designer should divide power-supply and ground lines into two categories: those that can use low-grade lines (epitaxial and substrate) and those that demand metal runs. When routing gets difficult, either the layout designer or an automatic router can determine which interconnections need not use metal. Moreover, in these arrays, substrate contacts in the central area are essential, otherwise parasitic coupling increases between components.

Naturally, proof of the pudding lies in a working chip. Consider, for example, a signal processor that takes on all read, write, and erase functions for double-sided floppy disk drives. The original handcrafted chip, built with a two-metal process, eats up 22,000 mils<sup>2</sup>; in contrast, if implemented with the Beta-240, the processor occupies only 17,600 mils<sup>2</sup>. Not only that, layout takes only one week as opposed to four.

The chip exemplifies a complex circuit designed at the



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### Cover: Space-efficient analog array

transistor level using standard analog building blocks: current sources, level shifters, differential amplifiers, and timing circuits (Fig. 4). Although dominated by smallsignal analog circuits, including op amps, comparators, and filters (as well as a peak detector and an automatic gain-control loop), the chip also contains one-shots, logic gates, and flip-flops.

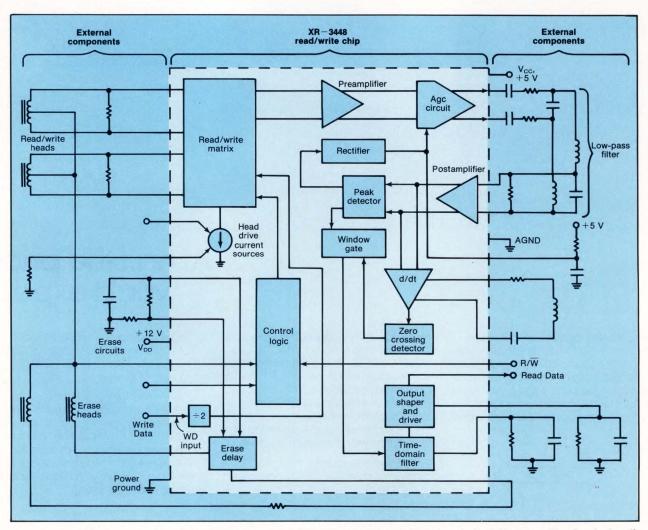
The small-signal circuits use the Twinstors very effectively, with 211 of them forming npn transistors and 52 forming pnp transistors. Another 53 npn devices are connected as diodes, most in the read/write matrix. The total count of 316 transistors hints at the ease with which many of the 250 Twinstors can be used separately as a pair of emitter-followers or in Darlington connections.

Twinboosters drive the write and erase heads, as well as

the outputs. A total of 204 resistors of various types are used, as are 28 bonding pads. □

Giovanni Giannella, Exar's group manager of engineering services, supervises product development and test systems design. He has held engineering, marketing, and manufacturing positions in the U.S. and Europe. He received a doctorate in electrical engineering from the University of Rome.

How valuable?	Circle
Highly	541
Moderately	542
Slightly	543



4. A floppy-disk read/write signal processor, the XR-3448, has been built on a Beta-240 array. The final circuit, which contains more than 300 transistors and over 200 resistors, creates the signals that drive the heads and then processes the signals emanating from them.

# How to bring system design out of the twentieth century.

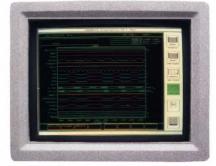


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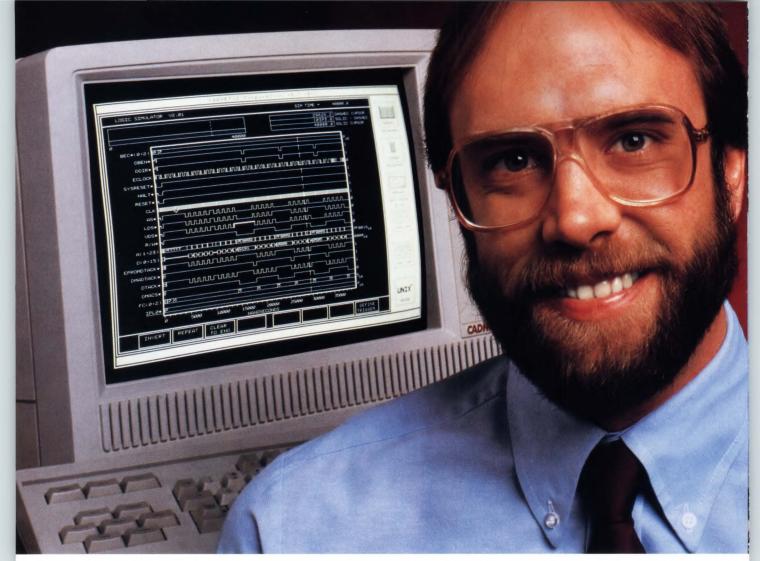
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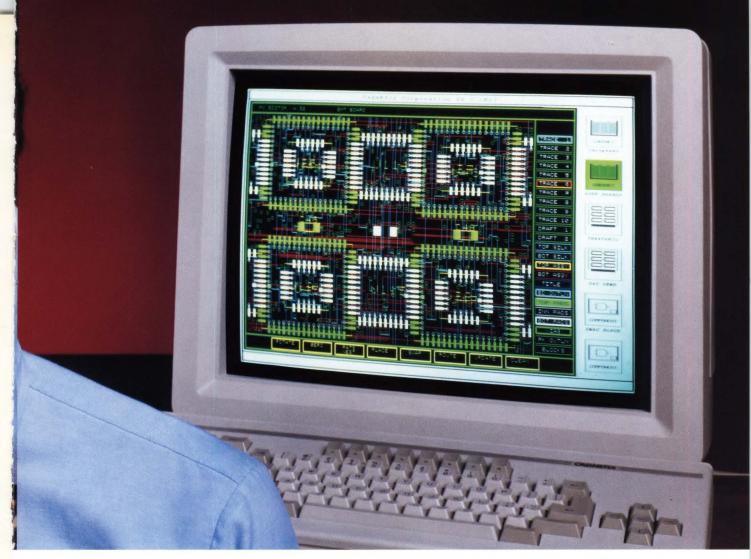
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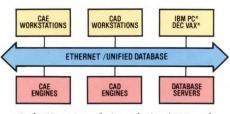
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Cadnetix systems design solution (CAE and CAD tied together by network and DB).

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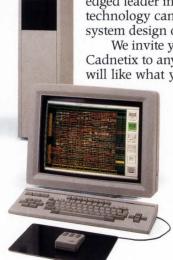
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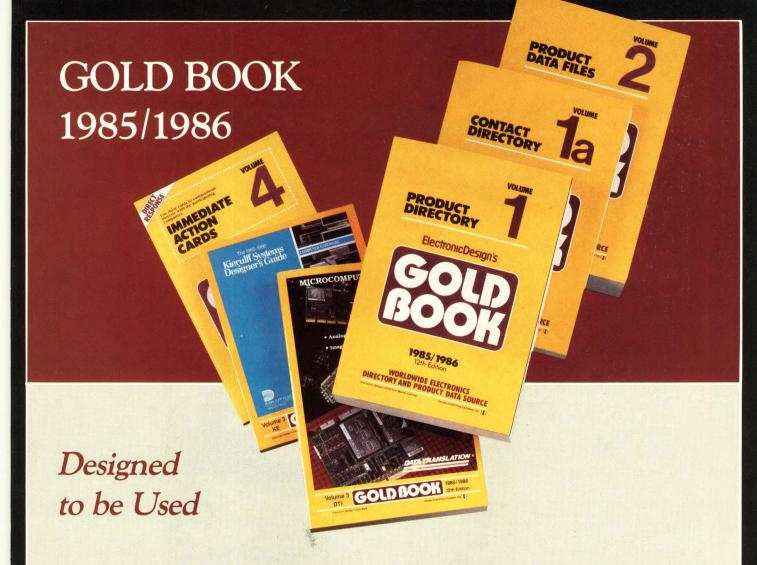
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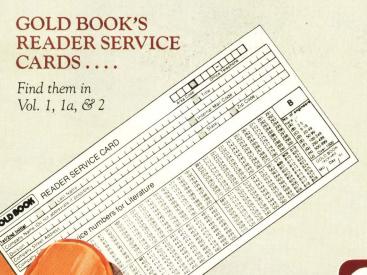
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## Targeted for speed, triple-bus DSP IC dispatches real numbers at 6.25 MIPS

Working with three rather than two buses, a fast signal processor chip makes short work of real and complex data. It serves as a platform for three operand algorithms.

Daniel F. Martin, Luc Mary and Baradir Barazesh **Thomson Semiconducteurs** Centre d'Etudes et de Fabrication Circuits Intégrés MOS Avenue des Martyrs BP217 38019 Grenoble Cedex, France (33) 76.49.36.00 ext. 38.23

Though Harvard architectures and short cycle times are common in digital signal processors, they are not particularly rare in general-purpose processors either. True improvements in DSP performance must be made in more specialized areas. A digital signal processor, for example, spends a lot of time moving data in and out of internal memories through its single data bus, creating a bottleneck in the flow of operations. In

contrast, an unconventional three-bus structure could execute equations with three operands—the daily fare of digital signal processing and arithmetic algorithms—at the rate of one cycle per equation.

The first VLSI processor to embody a practical three-bus structure, the TS68930 programmable signal-processing integrated circuit (PSI), performs repetitive data-intensive tasks at 6.25 MIPS (160-ns cycle time) on real-number data and at half that rate on complex data. For window operations (multiplying a block of variables by a block of constants) the chip works faster than its competitors, in some cases by a factor of 275%.

While a processor rarely includes complex number operations in its repertoire, such computations are the lifeblood of digital signal processing. DSP algorithms often use complex numbers in operations such as FFTs, convolutions, demodulation, and echo cancellation, among others. Thus, the DSP chip directly reads, multiplies, adds, and performs other operations on complex numbers to implement the required algorithms.

A single-chip microcomputer in its own right, the chip includes a multiplier, an ALU, ROM, RAM, and other circuitry. All together 120,000 transistors fit on a 57-mm<sup>2</sup> die in a 48-pin low-cost package. An open version (TS68931) in which the ROM is external is available in an 84-pin package.

The chip, fabricated with a 2-\mu NMOS process, typically dissipates 1.5 W. Two-phase logic is used throughout, with both 160-ns clocks obtained from an external 25-MHz crystal. The entire system is synchronized to the two clocks and in some cases to locally generated quarter-phase clocks (80 ns) used in the multiplier or for pre-

## Triple-bus DSP chip

charging the RAMs.

The small size and low cost of systems based on the chip especially shine in stand-alone equipment, small add-on boards, and embedded applications. For more complicated jobs, the DSP chip can serve as a building block in a multiprocessor tree.

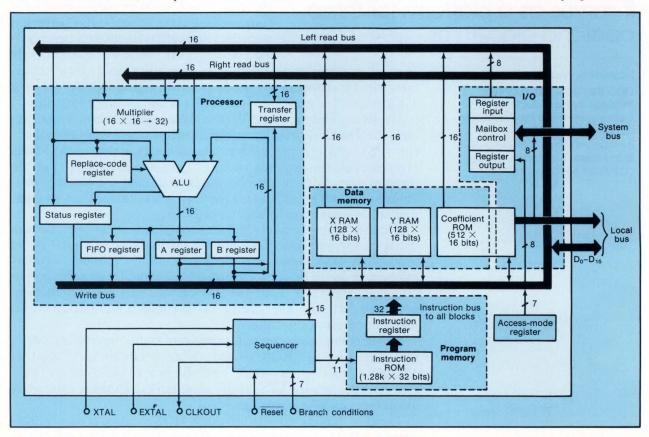
Because its instructions run independently of the data flow, a Harvard architecture requires separation of program and data memories and their buses. Though the obvious advantage is speed, the scheme also permits each bus to accommodate different word widths. Thus, the chip uses 32 bits for instructions and 16 bits for data.

While the Harvard architecture is parallel only in the sense that the fetching and execution of instructions occur simultaneously, to be truly parallel an architecture must work on at least two pieces of data simultaneously. Two 16-bit read buses continously feed the operating units with new data while the 16-bit write bus transfers the results to the RAMs (Fig. 1). Because the DSP chip has a 32-bit instruction word, two operands can be read from internal or external memories, a multiplication can be executed, and an ALU operation can take place—all in a single cycle. The multiplier result, which is stored in one of the working registers, serves as one operand for the ALU operation. In addition, the result of an ALU operation can be written into internal or external memory. Addresses can be generated for up to three operands, and those three addresses can be modified later.

### CANCELLING DELAYS

A delay occurs between reading and processing data and writing the results into RAM (multiplication alone takes two cycles). However, by pipelining the operations (Fig. 2), the delay has no effect on the processor's throughput. As an example, for a multiplication started at time N, the result will be available at time N+2. That, of course, does not prevent a multiplication from starting at N+1, which in turn gives a product at N+3, and so on.

Another special feature of the chip is the way in which it handles external resources. From the programmer's



1. In the TS68930 DSP chip, new data is continuously applied to the operating units over the two 16-bit left and right read buses. Results flow to the RAMs over the 16-bit write bus. Thus, the truly parallel architecture can work on two pieces of data simultaneously.

viewpoint, all those resources work the same way as the internal registers do. The processor, for example, will perform at full speed with an external RAM (55-ns access time). That is, a read-modify-write operation takes only 320 ns on 16-bit external data, delivering a data-modification rate of 50 Mbits/s.

Designers assess a processor's architecture by the improvements it supports in processing power, memory space, and precision. For the DSP chip, connecting processors in a tree hierarchy increases processing power. Each unit effectively becomes an independent module nested in an expanded machine in the same way that subroutines are nested in a program tree.

Memory area is expanded with external program memory of up to 64 kbytes and data of up to 4 kbytes. For more precision, a double-precision mode extends the width of all data paths to 32 bits but doubles cycle time.

The double-precision mode (32 bits), the real mode (16 bits), and the complex mode (16 bits real and 16 bits imaginary) correspond to the three processor data types. The programmer need only declare the mode in an initialization instruction and leave the remaining operations to the chip.

## DIVIDING TO REIGN

The chip is divided into four major sections: the processing block, data memory, program memory, and the I/O section (Fig. 1, again). All units and registers operating on data reside in the processing block. Included are a 16-by-16-bit complex multiplier with a parallel pipeline, a 16-bit ALU, 32-bit registers (A and B), a 4-by-16-bit FIFO, the replace-code register, and the transfer register.

The multiplier, which is separate from the ALU, is programmed independently as well. Full parallel multiplication takes two cycles, but thanks to the pipeline, a multiplication can execute every cycle. Operating on two 16-bit two's-complement numbers in two input registers, the multiplier yields a 32-bit result in its output register. In the real-number mode, the 16 MSBs are rounded and stored; the double-precision mode gives the full product.

## **COMPLEX MADE SIMPLE**

The complex number multiplication:

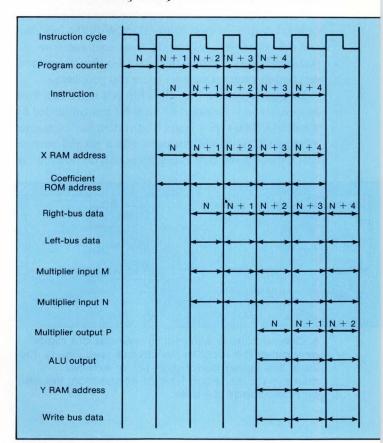
$$(A + jB) \times (C + jD) = (AC - BD) + j(AD + BC)$$

requires four multiplications, one addition, and one subtraction. All those operations are done internally in the multiplier, which includes four levels of pipeline, one adder-subtracter, a small sequencer, four input buffers, and an 80-ns clock. The throughput is 3.125 million complex multiplications a second. Since the hardware takes

care of the operations, the user does not have to keep track of the real and imaginary parts; he simply programs a complex operation exactly the same way as for real numbers.

On the next rung of the computational ladder sits the ALU and its associated registers. Having one of 27 different ALU codes in the instruction word establishes direct control over the ALU. Indirect control of the ALU stems from loading a variable into the replace-code register, which then replaces the ALU code. Thus, instructions can be data-controlled, and the ALU operations can be masked, making it impossible for a competitor to understand an algorithm. The ALU contains the third computational unit, a barrel shifter, which in one cycle can shift right or left and rotate any logical and arithmetic numbers from 1 to 15 positions.

Three sections make up the data memory space: a 512-by-16-bit coefficient ROM, two 128-by-16-bit data RAMs, and an external 4k-by-16-bit space. The coefficient ROM works separately from the instruction ROM



2. Pipeline operations eliminate the inherent delay between reading and processing data. Consequently, a multiplication started at time N, for example, completes at time N+1.

## Triple-bus DSP chip

and feeds the multiplier and ALU. It supplies coefficients and tables of constants for arithmetic calculations (sine waves and linear-to-μ-law conversion).

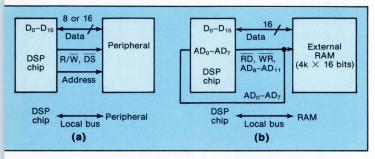
Variable data storage falls to the X and Y data RAMs, which store input and output samples, intermediate samples, long tables, and other data. The data RAMs (including the external memory) access all three buses, and the coefficient ROM accesses the left read bus.

### ADDRESSING A' LA MODE

The memories have four addressing modes: direct, indirect, immediate, and circular. Indirect addressing, the most common mode in vector or signal processing, enables the chip to offer many pointers. Two pointers, which address each memory, can be held, decreased, and increased independently or simultaneously. They also can be loaded with constants or computed values (for indexed addressing) and saved for context switching. The circular mode, particularly useful in filtering and convolution, simulates a shift register without moving the stored data.

Two external subsystems, external memory and a peripheral device, connect to the chip. With the local bus and the system bus, several different configurations are possible (Fig. 3). Through the local 16-bit bus, the processor controls external memory space and peripherals.

Using the system bus, the chip is a slave to a host processor and is accessed by an 8-bit bus controlled by standard 68000-type signals. The system bus exchanges information, data, and messages with a general-purpose host through a mailbox; a semaphore tells the host if it can



3. Connections to external subsystems are made over either the local or system bus (see Fig. 1). The local bus serves peripherals (a) or external memory (b). For each type of connection, the appropriate leads are used.

## Price and availability

Engineering samples of the TS68931 digital signal processor, housed in an 84-pin grid array, are available now. Commercial temperature parts go for \$150 apiece. Details on the price and availability of the TS68930 processor can be obtained by contacting the manufacturer. **CIRCLE 505** 

access the mailbox. The semaphore also can handle internal testing and control.

DSP programs must synchronize to external events (such as sampling clocks and buffer empty). For example, the seven branch-condition pins on the processor can serve as ready signals. The sequencer can directly test the ready signals and seven arithmetic flags (zero, overflow, sign, and so on).

The chip is also well suited to DSP tasks containing computation-intensive loops. To that end, a loop counter repeats up to 16 instructions as many as 255 times, with the possibility of a variable initialization delay. The loop counter avoids the use of a test and branch instruction in the loop. Also available are standard sequences such as jump to subroutine, return from subroutine, computed branches, and computed calls.

The instruction ROM can contain 1.28 kwords (each 32 bits long) in the 48-pin version and 64 kwords (external) in the 84-pin version. The user can access 256 locations that are reserved for self-testing of the circuit.

### **COMPOUND INSTRUCTIONS**

Processor resources are only as good as the instruction set that controls them. With 32-bit-wide instruction fields, programming could be a tiresome task (2<sup>32</sup> instructions to learn), but happily the chip's assembly language greatly eases the task. The 14 instructions fall into two main classes: normal and compound.

Like a microprocessor instruction set, normal instructions include sequencing instructions, register initialization, saving, and shift operations. Compound instructions are arithmetic instructions that perform up to four operations in parallel. Each operation corresponds to one or more instruction fields; namely, source and destination of operand 1; source and destination of operand 2; source, destination, and code of the ALU; and source and destination of the result. The three compound instructions each have a different addressing mode.

The amount of signal processing that the DSP chip can perform depends on the cycle time, that is, the time for basic operations such as multiplying, reading, writing, or initializing a register. Specifically, if the sampling fre-



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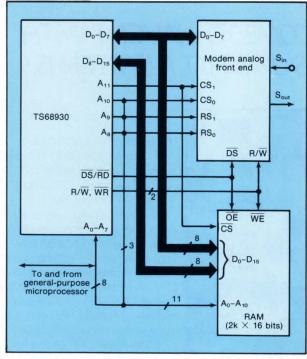
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## Triple-bus DSP chip

quency is F<sub>S</sub> (in kilohertz) and the cycle time is t<sub>C</sub> (in nanoseconds), the number of machine cycles available per sample is  $F_S^{-1}/t_C$ . For the DSP chip, the cycle time is 160 ns at an 8-kHz sampling rate that provides 781 cycles per sample period.

However, with the parallel pipeline architecture, 781 cycles does not dictate 781 operations. If the algorithm lends itself to repetition and parallelism, many more operations are possible. For example, a four-coefficient biquadratic filter requires six cycles or 0.960 µs, which is fast enough for many applications. For a cascade of biquadratic filter sections, the number of cycles can be reduced to four per section by shrewd programming, by using parallelism, and by taking advantage of the pipeline. Hence, the algorithm requiring 18 operations for



4. The TS68930 chip forms the basis of a modem that meets the V.29 9600-bit/s European standard. Besides the DSP chip, a modem analog front end consisting of three chips is also required.

each biquad section is accomplished at a throughput of one section for every four cycles, giving an average of 4.5 operations per cycle.

Until recently, digital signal processors were too slow and required too much interfacing to do many jobs inexpensively. Now, however, a dedicated analog front end has been introduced (Fig. 4). Illustrating this approach, the modem analog front end consists of a three-chip set: a transmitter, a receiver, and a time base circuit.

To meet the V.27 4800-bit/s European standard, the DSP chip connects to a modem front end, a microcomputer, and a line interface. The chip implements the transmission end in about 400 cycles and 250 instructions and the reception side in 2500 cycles and 700 instructions. In each baud period (625  $\mu$ s), the chip takes only 465  $\mu$ s to execute a complete modulation-demodulation cycle. Supplementary tasks, including multistandard data encryption and image compression in facsimile, occupy the remaining 160  $\mu$ s, or 1000 instructions. On the hardware side, only four chips handle the modem signal processing.

Furthermore, the multichip or kit approach applies equally well to other types of modems. For a modem that meets the V.29 9600-bit/s European standard, the chip has enough power and program memory to implement all signal-processing tasks (about 1100 instructions and 85% of the baud period). Except for a supplementary RAM, the hardware is the same as for the V.27 standard.  $\square$ 

Daniel F. Martin is application manager for the TS68930 at Thomson. Prior to joining the company, he held various positions in the British telecommunications industry. He has a BSc in electronics and communications from the Polytechnic of North London.

Luc Mary is project leader for the TS68930 at TRT, a telecommunication company affiliated with Thomson. Mary was previously TRT's group manager for data modems and signal processing and received the Diplome d'Ingénieur from Ecole Nationale Supérieure d'Electronique et de ses Applications (ENSEA) in Paris.

Now Thomson's modem strategic manager, Baradir Barazesh was formerly engineer and codesigner of the TS68930 at TRT. He has a Diplome d'Ingénieur and a PhD in systems and communications from the Ecole Nationale de Service de Trésor (ENST) in Paris.

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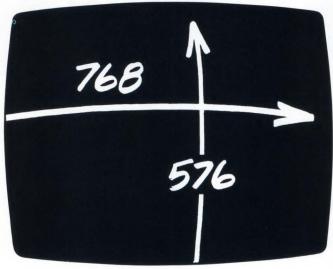
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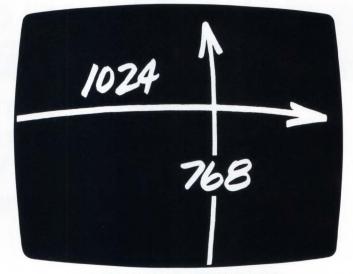
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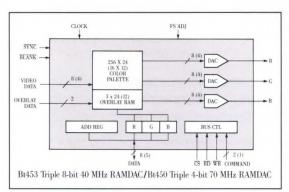
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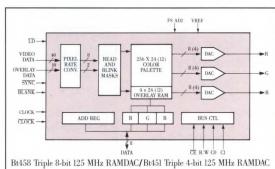
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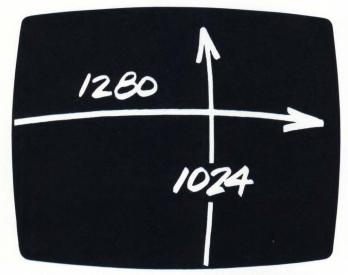
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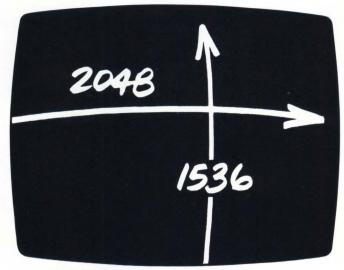


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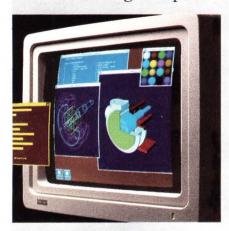




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## EEPROM-based ASIC propels programmable logic to new levels of complexity

By switching to a NOR structure and a novel mechanism for building up multiple logic levels, an electrically reprogrammable ASIC replaces about 20 low-power TTL devices.

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Choosing the best logic family for leadingedge designs can be difficult. TTL components encompass a wide range of logic elements, but they incur a high parts count, consuming much board space and power. Gate arrays solve those problems by offering high degrees of integration, yet they create their own equally serious headaches —namely, long development time, high cost, and the risk of failure. Programmable

logic devices (PLDs) offer designers instant configurability with reasonable levels of integration. But their AND-OR architecture proves restrictive, and bipolar versions are power-hungry and difficult to test.

Now a new breed of PLD branded the electrically reprogrammable application-specific IC, or Erasic, gives designers another alternative. The Erasic combines the multilevel logic functions of TTL with the integration and low power of CMOS gate arrays. An off-the-shelf device, it can be designed and programmed by standard personal computer—based CAE tools.

The first Erasic is the XL78C800. A 24-pin device, it carries up to 800 gates and replaces over 20 small-scale TTL components, yielding a density of about 1000 gates/in.<sup>2</sup> of board space. A power miser, the chip consumes typically less than 20 mA running with a 10-MHz clock, or 50% to 90% less than other bipolar and CMOS PLDs.

The chip's ability to incorporate multiple levels of logic functions is a virtue of its multilevel single-plane architecture. That structure assumes functions of one, two, or more levels by forging multiple passes through a single NOR plane. In contrast, conventional PLDs generate two-level functions, at most, by driving cascaded AND and OR planes with complementary inputs (Fig. 1).

In the new chip, complementary inputs and programmable polarity outputs shape the internal NOR plane into virtually any logic function. For example, single-level functions take one pass through the array. Selecting the input and output polarity transforms the NOR plane into equivalent AND, NAND, and OR functions. Two-level logic takes an additional pass, which generates sum-of-product

## Reprogrammable ASIC

and product-of-sum terms. And three or more passes produce the logic structures for word comparators, parity generators, and adders.

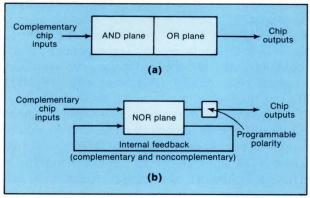
The NOR function is a natural CMOS building block. In fact, the AND planes of CMOS AND-OR PLDs are built from NOR functions by inverting their input polarities. The result improves performance because large fan-in CMOS NOR gates are faster than their AND counterparts.

The chip's single NOR array generates 66 programmable one-level logic functions, each of which acts on one or more of 96 array inputs. Although each logic function within the chip operates as a NOR, inverting various output and input lines creates AND, NAND, and OR functions. Besides the inputs and the outputs, which also serve as feedback paths, other signals constitute the chip's in-

## Inside the XL78C800

The XL78C800 ASIC is the first to combine the double-poly CMOS found in EEPROM memories and the double-metal techniques of 32-bit microprocessors. The former crams low power, high performance, reprogrammability, and complete testability into a plastic package. The latter affords high-speed interconnections in two overlapping and orthogonal directions.

Without incurring the RC delays found in long runs of polysilicon, the chip outperforms small-scale bipolar families such as low-power Schottky TTL. The two metalization layers also pay circuit-density dividends, squeezing twice the density of a 16-bit microprocessor into a 24-pin, 300-mil package.



1. By cascading separate AND and OR planes (a), most programmable logic devices create, at best, two-level logic functions. In contrast, the 78C800 electrically reprogrammable ASIC generates a multitude of levels by feeding back the original and complemented versions of signals through a single NOR plane (b).

terface. Those are J and K inputs, which control the flipflops in each I/O macrocell; Clear, which clears the flipflops asynchronously; and Latch Enable, which controls the input latch sections.

The chip's asynchronous feedback terms are a flexible means for adding logic levels. Those terms supply the first N-1 levels of an N-level logic structure. For example, sum-of-product functions are constructed by using the asynchronous feedback lines as product terms and making the J, K, and O lines the sum terms.

Ten macrocells form an important part of the chip's logic capability. They provide programmable flip-flops and I/O pins (Fig. 2). Each macrocell contains a flip-flop that can be configured for D, T, or JK operation. Moreover, a flip-flop can be freed from an I/O pin and "buried" into the internal logic because the chip's array has separate logic paths for synchronous and asynchronous inputs. Similarly, I/O pins can serve asynchronously without wasting a flip-flop. They can be programmed as fixed inputs or outputs, three-state outputs, or bidirectional paths.

Six bits configure each macrocell. Three of the bits select one of eight basic architectures. The bits are decoded into four lines that control the input and output multiplexers, as well as the output control logic. Moreover, the input multiplexer selects either a pin or an O term as the asynchronous input; the output multiplexer picks a flipflop or an O term as a pad output; and the control logic configures the I/O pin to be an input, an output, or a bidirectional line. The remaining three bits set the polarity of the J, K, and output terms.

With eight transparent input latches, the chip can synchronize to external signals or catch values from a bus. Moreover, the latches resolve external signals to their nearest valid logic level without oscillating. They are grouped into two sections of four bits each, and a separate Latch Enable signal controls each group. That signal, like others that form the chip's terms, can initiate a complex multilevel logic function. Alternatively, setting Latch Enable to logic 0 renders the latches transparent when they are not called for.

Possessing logic functions that are multiple levels deep, the new chip surpasses other PLDs and achieves parity with gate-array and standard-cell ASICs. Having multiple levels not only means higher integration over other PLDs, but also better performance because it minimizes the need to route signals off chip—a move that wastes I/O pins and adds signal delays.

One example is the chip's ability to function as a bytewide comparator. The chip integrates the function by using three levels and only 25 terms. The first two levels generate eight separate bit-wise comparisons, which are then NORed by a third level (Fig. 3a). The output of the NOR function becomes high when the inputs compare favorably. In contrast, it would take the summing of 256 product terms to create the comparator function from a two-level PLD.

At the same time, the chip is an efficient source of functions that require only one or two levels of logic. A single-level logic function, for example, requires only one pass through the chip's array. The programmable input and output polarities take advantage of DeMorgan's equivalence theorem and condition the chip's intrinsic NOR function to serve as OR, NAND, and AND gates (Fig. 3b).

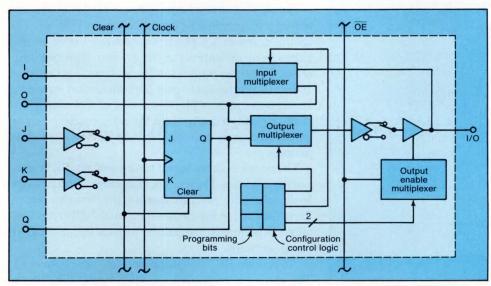
Furthermore, a single-level function takes only one term. That is an increasingly important advantage as the complexity of PLDs approaches that of gate arrays, since single-level gates tend to form a large percentage of the logic functions. On the other hand, AND-OR PLDs that have fixed OR planes must dedicate an entire set of product terms for every single-level function, thereby limiting integration. Even PLDs that have programmable OR planes must pass a signal through two arrays, adding delays.

The chip generates two-level, sum-of-products functions by making two passes through its array. The first pass creates the product terms; the second pass sums the results of the first. Inverting the inputs and outputs creates the sum-of-products function. On the other hand, omitting the inversion generates a product-of-sums structure, which is useful for active-low logic circuits (Fig. 3c).

Both sum-of-products and product-of-sums can be constructed from between 2 and 42 first-level terms. Thus, a designer can allocate the chip's logic resources precisely as needed. In addition, once a term is generated, it can be a part of other second-level functions throughout the chip and can even be brought out directly, if needed. Therefore, the new chip can combine one- and two-level functions to create powerful logic structures. Such flexibility remedies a paradox frequently encountered with typical AND-OR PLDs in which some logic structures run out of terms, while others leave terms unused.

Set-reset (SR) latches are another element that the new chip can create efficiently, and which other PLDs cannot. In fact, although common in TTL and gate arrays, SR latches are rarely found in PLDs because they are inefficient to implement. Even though the latch needs only two NOR gates, it can consume up to 25% of a typical PLD's logic and I/O pins. The new chip, on the other hand, takes merely two terms and no I/O pins (Fig. 3d). As a result, SR latches can appear freely in a logic design. They can be buried in the logic and combined with other functions, creating powerful and efficient internal logic structures.

Designing with the chip requires no more than industry-standard CAE and programming tools, such as Data

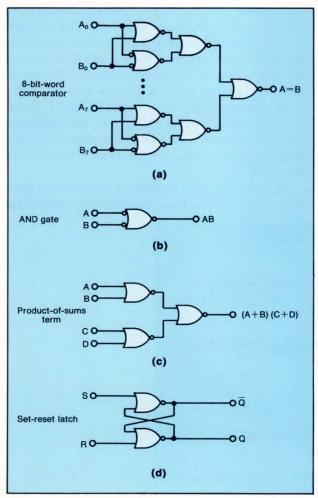


2. Each of the chip's ten macrocells contains several I/O paths and a programmable flip-flop. I/O pins can be programmed to be inputs, outputs, three-state outputs, or bidirectional signal paths. The flip-flops can be set for D, T, or JK operation. Moreover, each can be separated from its corresponding I/O pin and buried in the chip's internal logic.

## Reprogrammable ASIC

I/O's Abel system. Version 2.0 of that system has been enhanced to handle PLDs like the 78C800, which do not have AND-OR arrays. The system is available alone or as part of a personal computer-based personal silicon foundry. The personal foundry lets a designer enter a schematic, convert a net list, and derive and reduce Boolean equations. It also includes fuse map generation and programming facilities.

Because the new chip is electrically programmable, it eliminates discarding costly fuse-link PLDs. Existing logic programmers can erase a chip in a few milliseconds and reprogram it to reflect any upgrades. The total reprogramming turnaround time is just a few seconds (see "Inside the 78C800," p. 202).



3. Typical of the multilevel and single level functions that can be built within the new PLD are an 8-bit comparator (a), AND gate (b), product-of-sums term (c), and a set-reset latch (d). In other PLDs, these functions tend to be inefficient, difficult, or impossible to implement.

## Price and availability

The Erasic costs \$28.50 each in quantities of 100. That price applies to part number XLS78C800C, which has a 35-ns propagation delay, commercial temperature range, and is packaged in a ceramic DIP. Sample quantities will be available in July; production quantities will follow in October.

The chip also discourages reverse engineering. Activating a mechanism called SecurityPlus prevents the logic configuration from being read out and, at the same time, disables all internal addressing circuitry. Only erasing the chip can deactivate the security measure. In addition, optical inspection of this chip, unlike fuse-linked PLDs, offers no design clues, since EEPROM technology does not destroy any interconnections.

At the same time, the security mechanism does not impede testing of the chip. It is not activated until the first time the chip is powered up after programming the security bit. Thus, even if the security bit is set, the entire logic configuration, including the architecture and security bits, can be read out and verified as long as the chip remains powered. However, once the power is removed, the security feature is activated for the life of the logic configuration.

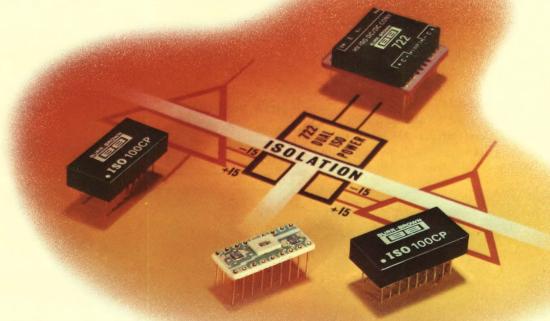
## ACCESS CONTROLLER, FOR EXAMPLE

The chip's multilevel logic is exemplified in its application as a programmable access controller (Fig. 4). The controller prevents a person's access to a device or area unless he or she enters the correct four-digit code. Attempting access without doing so sounds a two-tone alarm. In all, the single-chip implementation replaces a circuit board of 20 TTL components of SSI complexity. It also tightens security, since the entry code can be programmed directly into the chip without a DIP switch or jumpers.

The design includes buried state machines, SR latches, and input latches. The levels of logic range from one to six. In the schematic, gates are shown in the form that best reflects their use in the circuit; the actual NOR representation can be derived manually or with the help of the CAE design software.

An on-chip RC oscillator generates the system clock. The chip's high-impedance CMOS inputs simplify the oscillator and time delay circuits. A 2-kHz (nominal) clock feeds the keypad scanning circuit, the disarming sequencer, and the two-tone alarm circuit. The keypad scanner uses a pair of buried JK flip-flops configured as a two-bit counter whose output is decoded into three active-

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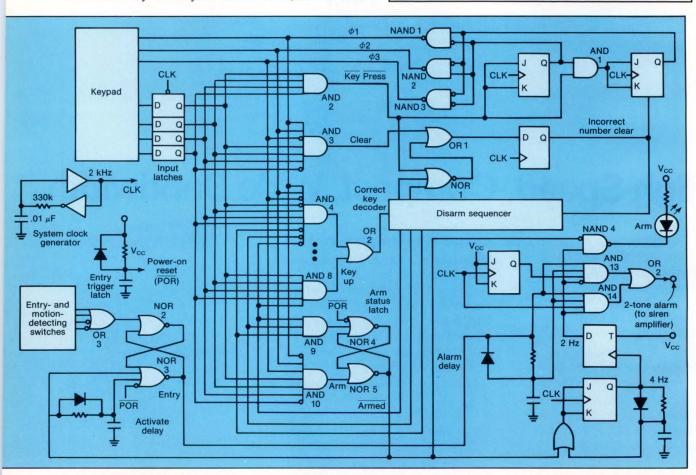
low phases that drive the keypad.

When a key is pressed, one of the keypad row lines goes low, activating the signal Key Press and stopping the counter. An input latch stores the selected row and feeds that data to the decoding state machine. From there the outputs of AND gates AND4 through AND7 of the state machine go high, but only if the correct key is pressed during the proper state. Pressing a correct digit advances the sequencer count by two. When the proper four digits are entered, as encoded by gates AND<sub>4</sub> through AND<sub>7</sub>, the disarm sequencer reaches an all 1s logic state. That state causes gate AND<sub>9</sub> to reset an Arm Status latch, putting it in the disarmed state. If an incorrect key is pressed, a clear signal resets the disarm sequencer.

In addition, if one of the monitor switches detects that someone has gained access, OR gate OR<sub>3</sub> goes high. That, in turn, sets the entry trigger latch and initializes the alarm delay circuitry. After about 30 s, the alarm delay RC circuit goes to a logic 1, gating the two-tone alarm signal to an external alarm amplifier. An authorized entry, signified by the entering of the correct 4-digit sequence within 30 s, resets the entry trigger latch and inhibits the alarm.□

Erich Goetting is the principal architect and designer of the 78C800 electrically reprogrammable ASIC, a project he spearheaded. He holds a BS in electrical engineering and another in finance, both from the University of Pennsylvania, as well as an MS in computer science from the University of Southern California.

How valuable?	Circle
Highly	547
Moderately	548
Slightly	549



4. A programmable access controller circuit fits into the EEPROM-based reprogrammable ASIC. The circuit includes logic functions ranging from one to six levels deep, and devices such as a state machine, SR latches, and input latches. The circuit prevents access to equipment and areas, except for those who know a 4-digit code.



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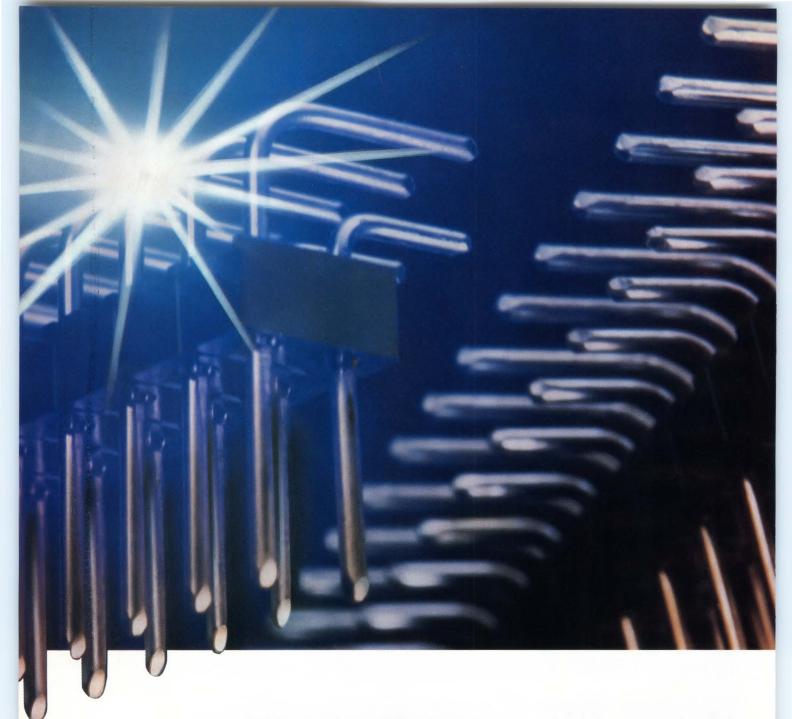
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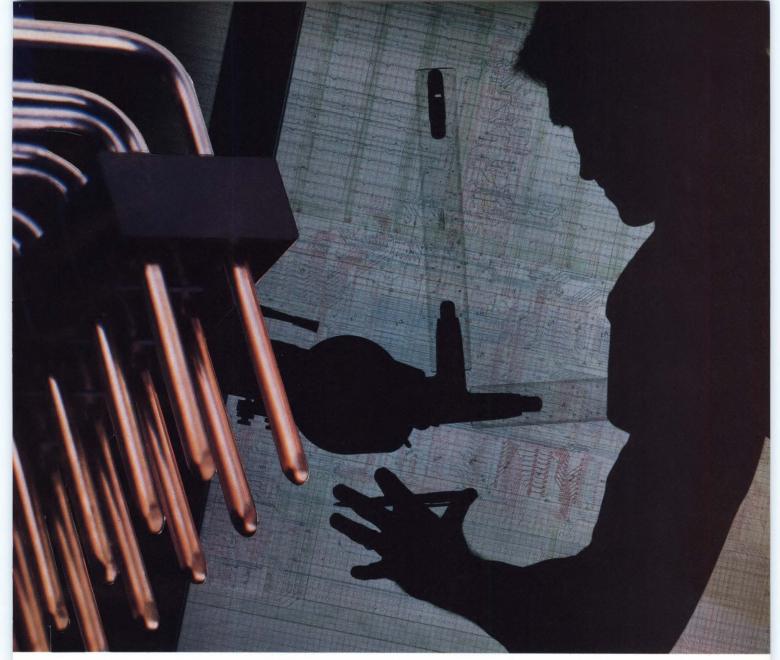
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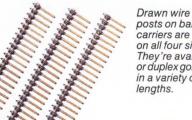
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**ELECTRONIC DESIGN EXCLUSIVE** 

## Interface chip links floating-point coprocessors to host to form supermini look-alike

A memory-mapped interface and its companion coprocessors bring 5 MFLOPS to a host CPU. Racing through 3.5 million Whetstones/s, the chips near full-scale computer speed.

Eric Hildebrandt, Tony Funari, and John Oxaal Weitek Corp. 1060 E. Arques Ave. Sunnyvale, CA 94086 (408) 738-8400 This article is the second in a series on a new family of floating-point devices. The first installment presented a 32-bit processor and sequencer, and the third entry will describe a floating-point multiplier, an ALU, and a 32-word register file.

Coprocessors that work with microprocessors offer a convenient way to add floating-point math operations to a system. The convenience in the past, however, has

come at the cost of computational speed. Assuming a coprocessor could perform floating-point operations in zero time, protocol handling still limits the improvement in overall speed to a factor of about two. Even the new, high-performance floating-point arithmetic units, which are multiported and highly pipelined, are difficult to integrate into a microprocessor. It is also very difficult, if not impossible, to develop compilers for them.

Though a coprocessor's performance may suffice for most general-purpose requirements, many applications need all the floating-point performance they can get. For example, 32-bit systems such as engineering workstations, industrial robots, and graphics controllers require extensive computations.

Such demanding jobs call for more than specialized floating-point multipliers and ALUs. To reach higher processing speeds, the system must employ a memory-mapped interface from the floating point chips to the CPU rather than a standard coprocessor protocol. As a memory-mapped alternative for 80386-based systems, the WTL 1163 performs all the necessary interfacing tasks. That is achieved on one chip, compared to the previously required board full of bit-slice components. Operating with the WTL 1164 floating-point multiplier and the WTL 1165 ALU, the system executes computations at about 3.5 million Whetstones/s, which compares favorably with 5.5 million Whetstones/s of a VAX 8600 supermini that costs about \$500,000. That speed offers a fivefold to tenfold improvement in register-to-register operations compared with the fastest floating-point coprocessors.

Though the actual speed depends on the operation involved, the

## Memory-mapped interface

interface chip clearly hastens processing. For example, in an application requiring the host CPU to dedicate 50% of its time to floating-point calculations, with the remaining 50% devoted to other work. Even an improvement by a factor of five in floating-point performance means that the main CPU is only 60% occupied instead of pushing its limits at 100% of its capacity.

### **MEMORY MAPPING**

The interface chip maps the floating-point chips into the CPU's memory space, enabling more efficient use to be made of the system's data bus than do coprocessor protocols. The trade-offs inherent in memory-mapping can be reconciled in performance-oriented applications.

Primarily, the memory-mapped interface must compromise exception tracking for speed, since it uses a pipelined procedure to execute one instruction while fetching the next. If an exception occurs, associating it with the correct instruction proves difficult. However, exception tracking in numerical processing applications is more important during software debugging than in actual problem solving, and the floating-point subsystem can run in a nonpipelined mode during software development. Once the major bugs have been eliminated from the design, the interface can shift to the faster pipelined operation.

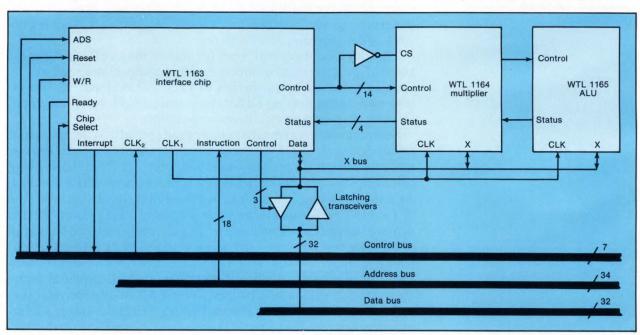
Another potential concession, software compatibil-

ity, can be resolved by the Fortran, C, and Pascal compilers that work with the chip. The compilers, transparent to a user, translate high-level commands into appropriate instructions for the floating-point chips. Besides handling intrinsic functions such as add, subtract, multiply, and divide, the compilers include a library of extrinsic functions such as the sine and cosine for the Unix V/386 operating system.

To link to an 80386, the interface chip works with the WTL 1164 multiplier and WTL 1165 ALU (Fig. 1). A few external chips such as a decoder and latching transceivers complete the interface between the CPU and the floating-point chips. Though the interface functions can be realized using discrete logic chips, the single interface chip combines all the required functions (Fig. 2) and frees engineers from designing and programming high-performance logic.

## **UP-SCALE ADDRESS**

The floating-point subsystem is mapped into memory and occupies a part of system memory that is addressed by the upper 15 bits of the system address bus. When an external decoder detects activity on those address lines, and the Address Strobe signal (ADS) indicates that the address is valid, the decoder generates the Chip Select signal for the interface chip. With decoding off the chip, designers directly control the subsystem's location in the CPU's memory map, thereby minimizing the num-



1. Working with the WTL 1164 multiplier and the WTL 1165 ALU mapped into memory, the WTL 1163 interface chip adds high-speed coprocessing to an 80386. Instructions and data are transmitted simultaneously.

ber of lines to the chip.

An understanding of the 1163's address decoding begins with the CPU's byte-addressing system. The CPU's 34-bit address bus consists of 30 word-address lines and 4 byte enable bits. By using the 4 byte-enable bits instead of the 2 least significant address bits, the CPU supplies dedicated lines to specify each of the 4 bytes in a 32-bit memory location. The 1163's 17-bit instruction consists of the lower 15 word-address bits and 2 bits that are encoded from the CPU's 4 byte-enable bits. Actually, the interface chip uses only 3 of the byte-enable bits to derive the 2 least significant address bits.

When Chip Select is generated, the contents of the address' lower 15 bits and 3 of the CPU's byte-enable bits designate which of the interface chip's registers contain the data and the instruction for the desired operation. By specifying both the operands and the instructions in the address field, 32 data bits can be transferred at the same time as the instruction. That reduces bus transfer requirements for operations involving transfers between memory and the chip's data registers. In contrast, some memory-mapped schemes rely on the address bus to specify the math subsystem's address and then employ the data bus to specify the desired math

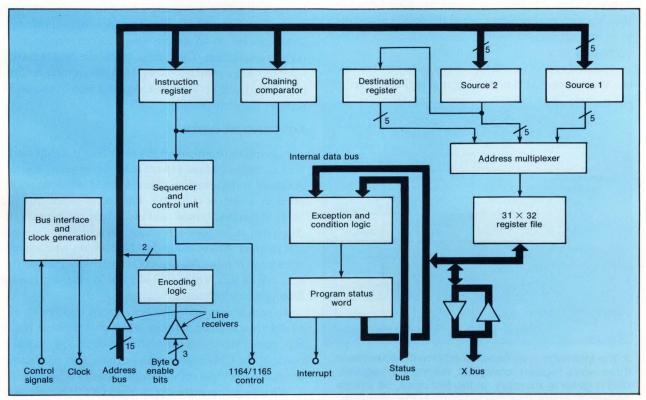
instruction—two bus transfers compared with the interface chip's single operation.

ADS latches instructions into an internal register of the interface chip. A Ready signal from the chip indicates when it can accept another instruction from the CPU. If a transfer to the floating-point chip starts while the chip is busy, Ready holds the bus until the current operation is completed. After a new instruction begins and the chip's internal instruction latch empties, the chip acknowledges the transfer with Ready.

Additional off-chip logic required by the subsystem consists of latching transceivers that act as buffers between the floating-point chip's data bus and the CPU's data bus. The transceivers hold the data going to the interface chip until the floating-point processor is ready for it.

### 17-BIT COMMANDS

Interface-chip instructions are 17 bits long and consist of the lower 15 address bits plus the 2 bits internally encoded from 3 of the CPU's 4 byte-enable bits. The floating-point subsystem thus occupies 131 kbytes (2<sup>17</sup>) of the system's 4-Gbyte (2<sup>32</sup>) total address space. The 17-bit format contains a 7-bit op-code field and two operand fields: SRC<sub>1</sub>, the source of one operand, and



2. For instructions the interface chip makes use of the lower 15 bits of the address bus, plus 3 of the 4 byte-enable bits from the CPU. The 3 bits are encoded into 2 additional bits to make up a 17-bit address bus.

## **Memory-mapped interface**

SRC<sub>2</sub>/DEST, for the source of a second operand in twooperand calculations and the destination for a computation's result (Fig. 3).

Users can access 31 registers in the chip, each of which is 32 bits long and contains data for calculations. Doubleprecision values occupy two contiguous registers, with the most significant word in the even-numbered register.

Although the chip does not contain an R<sub>0</sub> register, specifying R<sub>0</sub> for the SRC<sub>1</sub> operand indicates an operation that involves data residing in both system memory and the chip's register file. If single-precision operation is intended, the data from memory is transferred on the data bus along with the instruction on the address bus. If the operation calls for double precision, the most significant 32 data bits are transferred with the instruction; however, the least significant 32 bits have to have been written previously into register R<sub>1</sub> with a Load instruction.

## SOFTWARE ACTS AS KEY

Because the interface chip handles nearly all the hardware and software details for integrating the floatingpoint chips, the primary implementation task rests with the application programmer. For example, the chip handles arithmetic operations with a register-to-register instruction (Fig. 3 again). All source operands come from the chip's internal registers, while the results are written to an internal register to make them available for further

A second type of instruction, memory to register, takes one source operand from the internal registers. Further-

	16	10 9	5	4
Register-to-register instruction	7-bit op code		SRC <sub>2</sub> /Destination register	SRC <sub>1</sub> register
1	16	10 9	5	4
Register-to-memory instruction	7-bit op code	8	RC <sub>2</sub> /Destination register	00000
1	16	10 9	5	4
Register-to-register move	Load		Destination register	SRC <sub>1</sub> register
	16	10 9	5	4
Memory-to-register move	Load		Destination register	00000
1	16	10 9	5	4
Register-to-memory move	Store		Source register	00000

3. The interface chip handles arithmetic operations three ways: register to register, memory to register, and register to memory. In the first case, all source operands come from the registers in the interface chip. In the other two instances, transfers take place between the chip and the external system memory.

## Price and availability

The WTL 1163 will be available in production quantities in the third quarter, with samples available now. The WTL 1164 and WTL 1165 are currently in production. In quantities of 100, the 3-chip set sells for less than \$600.

more, results are written to an internal register. In register-to-memory instructions, data simply moves from the interface to the CPU system bus.

Register-to-register operations begin when an instruction is transferred to the interface chip over the system address bus. Only information that is transferred with the instruction is used; any other transfer of data is ignored. With an 80386, the Move Byte instruction [MOV-b (address) Reg. 1 is the minimum possible encoding. Other CPU instructions might also work, but they must not generate multiple transfers.

If a Move Word command were given, for example, and the word's address were not aligned on a word boundary in memory, the CPU automatically would make two transfers to move both parts of the word. Since the interface chip does not support misaligned data transfers, however, it will interpret the second transfer as another instruction. To avoid this situation the 4 byte-enable bits should always be set to zero when sending a register-toregister instruction. Those zeros signal the chip to start a word move at a word boundary. However, it remains simpler to use the Byte Move instruction, which can result in no more than one transfer.

### **EXERCISING THE SYSTEM**

A graphics transformation shows how the chip works with an 80386 and the 1164/1165 floating-point chip set. A typical transformation requires that a vector be multiplied by a matrix (Fig. 4a). The vector represents the point to be transformed, and the matrix contains coefficients that accomplish actions such as translating, scaling, and rotating. All the values for the example, which is representative of other floating-point algorithms that the system can handle, are assumed to be in single-precision floating-point format.

To perform the multiplication, matrix coefficients a21 to a44 are contained in the interface-chip registers R<sub>16</sub> to R<sub>31</sub>, respectively, and the vector elements x, y, z, and w reside in the CPU registers. Once the matrix coefficients are stored, they can transform any number of vectors.

With the values in their proper places, a 256-cycle algorithm (Fig. 4b) implements the vector matrix multiplication. As with any such multiplication, the trans-

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## Memory-mapped interface

formed vector is calculated by multiplying each element of the original vector by the corresponding coefficients in each column of the matrix and then accumulating each set of column values. The first vector-column multiplication produces x', the second y', and so on.

A Load instruction clears the interface's R2 register so that it can accumulate the results of the column multiplications. They are performed by the series of multiply and accumulate instructions (Mac.S), which also add the multiplication results into the interface's R2 register. After the four column multiplications are done and R<sub>2</sub> contains the final value for x' (the first element of the transformed vector), the Store instruction (Stor) moves the x' value into a register in the CPU. The entire process repeats three times to produce the other three transformed vector elements.

Execution of the transformation algorithm takes 250 cycles, excluding the initial register loading, which is done only once for a series of transformations. The graphics system must also perform other floating-point operations such as clipping and perspective division, which reduces the speed by a factor of about three. Since each cycle takes 60 ns, the system can transform 66,667 vectors per second to obtain overall operation of about 20,000 vectors per second. Thus, the general-purpose floating-point accelerator dramatically increases performance in a dedicated function like graphics. □

Eric Hildebrandt, a senior applications engineer, assists customers in using Weitek's products. He helped design the WTL 1163 and was employed at Harris Computer Systems and Hewlett-Packard. Hildebrandt holds a BSEE from Purdue University.

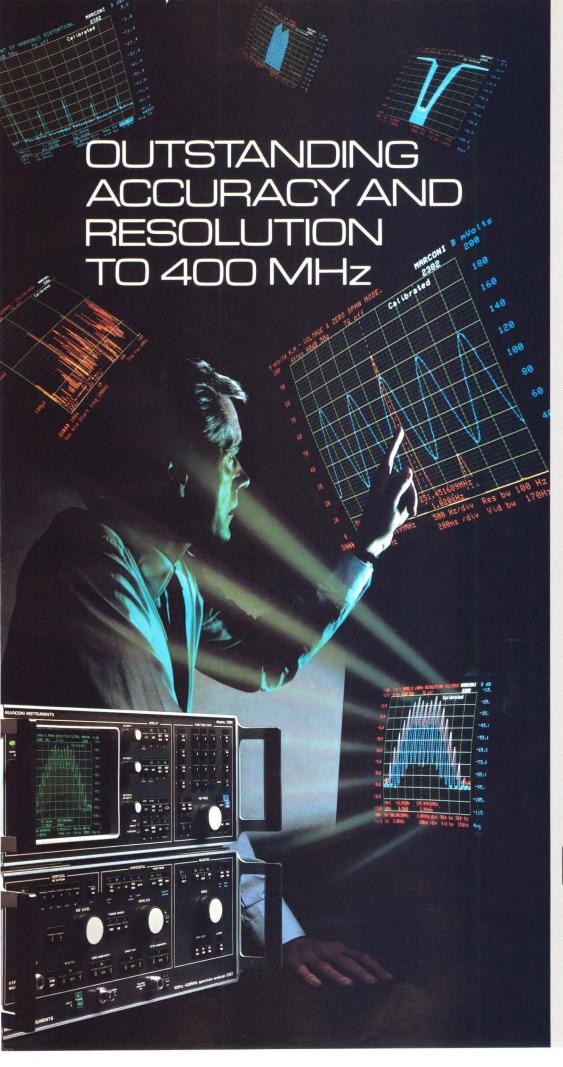
As a field applications engineer at Weitek, Tony Funari gives technical assistance to the sales department. Previously, he designed array and image processors at Computer Design and Application in Waltham, Mass. Tony earned a BSEE at Tufts University and an MSEE at Northeastern University.

John Oxaal joined Weitek in 1985 and manages product marketing for floating-point products. He also helps choose new products for development. Oxaal has a BS in engineering from Duke University and an MBA from the University of Chicago.

How valuable?	Circle
Highly	550
Moderately	551
Slightly	552

4. A transformation requiring that a vector be multiplied by a matrix (a) is accomplished in the program, which consists of 256 cycles (b). The matrix contains the coefficients to perform the transformation. All values are in single-precision floating-point format.

	(a)	
Mnemonic	Comments	Number of cycles
Load R2,0	: Clear accumulator	
Mac.S R16.X	: R2=R2+a11.X	6 cycles
Mac.S R17.Y	; R2=R2+Q11.X : R2=R2+q21.Y	13 cycles 13 cycles
Mac.S R18.Z	R2=R2+G21.7 R2=R2+G31.7	13 cycles
Mac.S R19,W	; R2=R2+Q41.W	13 cycles
Stor X',R2	$X' \le R2 = a11.X + a21.Y + a31.Z + a41.W$	6 cycles
Load R2.0	; Clear accumulator	6 cycles
Mac.S R20,X	: R2=R2+a12.X	13 cycles
Mac.S R21.Y	: R2=R2+q22.Y	13 cycles
Mac.S R22,Z	R2=R2+a32.Z	13 cycles
Mac.s R23,W	R2=R2+a42.W	13 cycles
Stor Y',R2	$Y' \le R2 = a12.X + a22.Y + a32.Z + a42.W$	6 cycles
Load R2.0	; Clear accumulator	6 cycles
Mac.S R24,X	: R2=R2+a13.X	13 cycles
Mac.S R25,Y	; R2=R2+q23.Y	13 cycles
Mac.S R26,Z	; R2=R2+a33.Z	13 cycles
Mac.S R27,W	R2 = R2 + a43.W	13 cycles
Stor Z'.R2	$Z' \le R2 = a_{13}X + a_{23}Y + a_{33}Z + a_{43}W$	6 cycles
Load R2.0	: Clear accumulator	6 cycles
Mac.S R28.X	; R2=R2+a14.X	13 cycles
Mac.S R29,Y	R2 = R2 + a24.Y	13 cycles
Mac.S R30.Z	R2=R2+G24.7	13 cycles
Mac.s R31,W	R2=R2+G04.2	13 cycles
Stor W',R2	W' < = R2 = a14.X + a24.Y + a34.Z + a44.W	6 cycles
		TOTAL 256 cycles
	(b)	200 37 0,00



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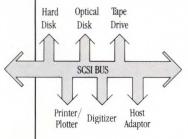
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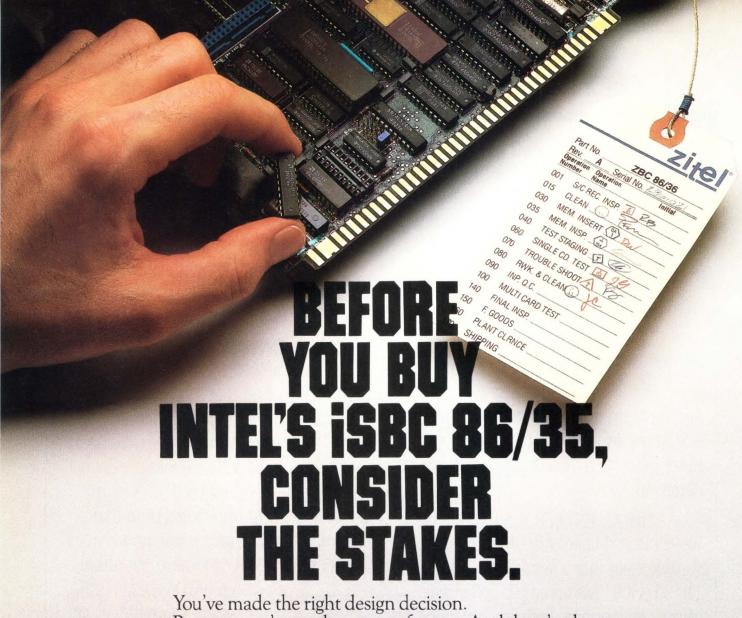


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**ELECTRONIC DESIGN EXCLUSIVE** 

# 68000-type microprocessor packing peripheral subsystems smooths workstation design

Designers can build low-cost, powerful workstations compatible with existing software by picking a processor that sports dual DMA channels, MMU counters, and serial I/O.

Dirk Braune and Jean-Claude Six

Philips International BV Microelectronics Support Center 4·16 Avenue du General Leclerc 92260 Fontenay aux Roses Paris, France 31·1·4702·7545

**Bob Rowe** 

Signetics Corp. 811 E. Arques Ave. P.O. Box 3409 Sunnyvale, CA 94088 (408) 991-2000. With rare exception, the workstation world revolves around designs centered on the 68000 microprocessor. Moreover, later generations of the processor, the 68010 and 68020, offer a path to compatible, higher performance products. Missing, though, has been a means to combine high performance with the ability to build low-cost systems in large volume. To achieve such flexibility, a processor chip would have to

absorb the multitude of peripheral circuits that surround it.

A new microprocessor, the 68070, is such a chip. Besides employing a CPU that is compatible with 68000 software, the chip boasts a dual-channel DMA controller; a sophisticated memory-management unit; three independent counter-timers; a full-duplex RS-232-C asynchronous serial communication channel; and a serial inter-IC (I<sup>2</sup>C) bus. In short, the 68070 encompasses functions that are essential for communicating effectively and efficiently, for managing multiple tasks, and for working in a distributed-processing environment.

With more functions crammed alongside its CPU than other 68000 family members, the 68070 promises to shave development and production costs. The chip holds down part counts, keeping circuit boards smaller, simpler, and less-expensive. Furthermore, power and cooling requirements are trimmed, since the chip demands fewer parts and consumes only about 1 W running at 10 MHz. High-speed 2-µm CMOS technology accounts for the chip's fast, low-power performance.

To ensure machine-code compatibility, the 68070 carries registers identical to the 68000's. Thus, any program compiled at the 68000's machine-code level runs on the 68070 without modification. The chip also incorporates the 68000's asynchronous bus and arbitration controller, as well as the same nonmultiplexed 24-bit address and 16-bit data buses. The 16-Mbyte addressing range accommodates large, complex applications.

The chip recovers fully from bus errors in the same way that the 68010 does: When a bus error occurs, the CPU saves its context on a

## Highly integrated 68000

stack and starts an exception routine. At the end of the routine, it restores its context before continuing with the current instruction.

Furthermore, a vector-interrupt scheme with seven priority levels equips the chip for real-time and highly interactive systems. The on-chip peripherals can trigger any of the interrupt levels; external subsystems can activate four levels through the chip's decoded interrupt and interrupt acknowledgment pins.

### **DUAL DMA CHANNELS**

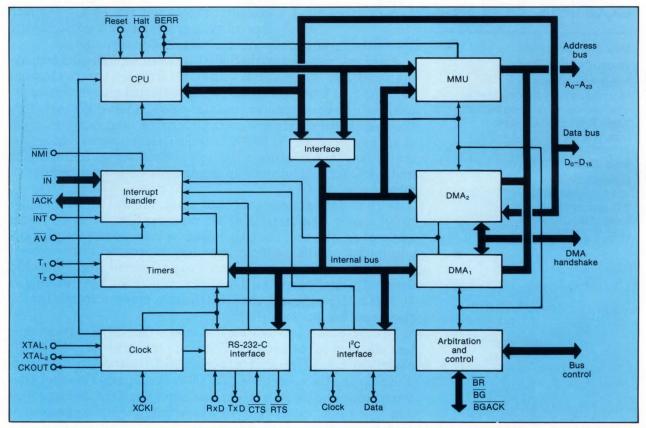
The processor features two independent DMA channels that move data between memory and I/O devices or other locations in memory (Fig. 1). Byte-wide transfers clip along at 3.2 million bytes/s, while 16-bit wordwide transfers are done at half that rate. Data can be transferred in single cycles and bursts, and the average bus latency never exceeds  $2.5 \mu s$ .

Each channel can be programmed for a different priority level, although during bus arbitration a DMA operation gets the highest priority, followed by external devices, and then the CPU. Of the two channels, channel 1 claims the highest priority and only transfers data between an I/O device and memory. Such transfers, relying on a set of handshake signals, can take place over 8- and 16-bit ports in a single bus cycle.

Channel 2 also transfers data between memory and I/O, as well as between different memory locations. Memory-to-memory transfers take two or more bus cycles, and data is stored temporarily in the CPU. Memory locations are addressed explicitly by the chip's address and control lines, instead of by the handshake signals used in I/O transfers.

Both channels have the same programming models as the 68430, 68440, and 68450 DMA controllers. Thus, they are functionally compatible with those devices. Equipped with two 16-bit counters and a 24-bit address counter, the channel can move blocks of up to 128 kbytes anywhere within the full addressing range. In other words, each channel can transfer 65,536 contiguous words or bytes without pause.

The on-board memory-management unit (MMU) is



 The 68070 microprocessor features a CPU that is machine-code compatible with the 68000. The 68070 also has dual DMA channels, a sophisticated MMU, and three independent counter-timers. For added I/O capacity, the chip sports a full duplex RS-232-C port and an inter-IC bus.

modeled after the 68910 and 68920 memory access controllers (ELECTRONIC DESIGN, Aug. 23, 1984, p. 153). The unit translates logical addresses into physical ones (Fig. 2). It also protects memory segments from illegal accesses, like attempts to change a write-protected area of memory. (For applications that do not require the MMU, it can be inhibited by resetting a control register bit.)

#### A BUILT-IN MEMORY MANAGER

The MMU can set the memory segment size in 1-kbyte increments. It manages anywhere from 8 segments of 2 Mbytes each to 128 segments of 128 kbytes each. As result, programmers can encapsulate entire modules in one protected space or maintain smaller and more numerous (even variable length) segments. The latter case allows shorter disk transfers and simpler swapping operations.

Each of eight descriptors stored in an on-chip table holds information like the base address and length of memory segments, as well as attributes. Typical attributes grant or deny permission to access supervisory memory, or read from, write to, and execute particular memory locations. Furthermore, attributes indicate when a stack segment is being accessed.

For every access, a memory segment number is compared to a segment number in the on-chip table. The comparison checks the memory displacement against the actual segment size, and access-protection and segment-enable bits are examined to ensure that the access is legal. If the access is legal, the MMU issues the necessary data strobe signal. If an illegal access is at-

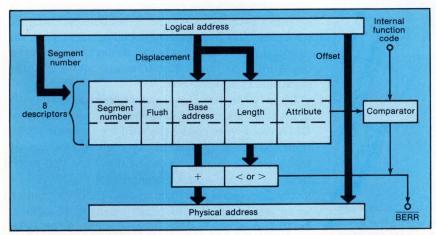
tempted, the MMU disables the data strobe pulse and the CPU executes a bus-error exception routine. After the error is resolved, the CPU resumes normal operation and completes the bus cycle like a 68010 would.

The processor's three independent 16-bit counter-timers serve a variety of general-purpose functions. One timer with a 10-µs resolution runs continuously, making it a useful reference clock. The other two circuits are programmable timers with independent 16-bit register-counters (Fig. 3). They can change output state whenever their contents match. Thus the registers can generate a timing pulse when a match occurs between the preset contents of one register and the reference-timer count accumulated in the second. Similarly, external events can be counted and timed. Timing is done by noting an event's occurrence in a count register and capturing the reference-timer contents at the same moment.

#### TO COMMUNICATE SERIALLY

Besides the counter-timers, two types of serial buses fortify the processor's ability to communicate with the world outside. The first, a dual RS-232-C serial bus interface, carries asynchronous data and connects printers, terminals, and other peripheral devices. The interface features full- and half-duplex communication, as well as an autoecho mode for diagnostics. Two baudrate generators paired with the buses can be independently programmed for one of eight transmitting and receiving rates between 75 and 19,200 baud.

The second serial interface, the I<sup>2</sup>C bus, consists of two lines: a clock signal and data. Handy for linking the



2. The on-board MMU translates the chip's 16-Mbyte logical address range into physical space in main memory. Besides storing translation data in its descriptors, the MMU also holds attributes that protect selected areas of memory from being read from, written to, or executed illegally.

#### **DESIGN ENTRY**

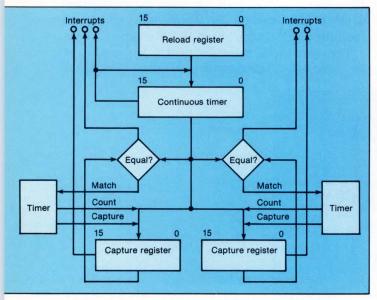
#### Highly integrated 68000

CPU to relatively slow devices, the bus also serves as the interface to an 8-bit single-chip microcontroller. The controller or a similar device can manage an LCD, clock-calendar, nonvolatile RAM, or other peripheral by taking control of the bus. The processor itself can serve as a master or a slave. In addition, it can operate over the bus as a receiver or a transmitter.

The chip also features a high-speed parallel data bus that is compatible with the other members of the 68000 family. The bus can transfer data at rates up to 40 Mbits/s, or 5 Mbytes/s. Moreover, it can accommodate several master devices by harnessing the chip's multilevel interrupt scheme. Importantly, no TTL glue logic is needed to connect multiple masters to the bus, either for the four fully decoded interrupt inputs or the bus arbitration logic.

#### **WORK AMONG FRIENDS**

Like other 68000 microprocessor family members, the chip can operate alongside intelligent controllers like the 68454 for disk operations and the 68562 for serial communications. The disk controller executes high-level commands that manage data transfers between a disk and the CPU, interrupting the CPU when it is finished. Even the serial communication controller takes advantage of the processor's DMA channels to transfer incoming data di-



3. Three independent counter-timers within the 68070 make it easy to keep track of events happening outside the chip. A continuous timer makes a useful reference clock, resolving time to increments of 10  $\mu$ s. The two remaining timers include registers that interrupt the CPU when their contents match.

#### Price and availability

The 68070 microprocessor, packaged in an 84pin plastic leaded chip carrier, can now be had in sample quantities. Production quantities are scheduled for early next year. The introductory low-volume price will be \$50. In high volumes, the chip is targeted for \$20. **CIRCLE 503** 

rectly to memory.

With the new chip's built-in functions and the ease with which it interconnects to other intelligent ICs, designers gain flexibility in tailoring a system to specific needs, price, and performance. For example, a very capable but economical workstation could be developed that handles some features locally and passes others to a compatible but more powerful processor. Given the vast majority of workstations that run on the 68000 family, the processor is a natural foundation for such a low-cost system.

Typical CAD and CAE workstations require text and graphics, multitasking ability, megabytes of main memory, hard and flexible disks, and communication ports. To serve as the core of such a system, the new chip connects to a number of subsystems transferring data at high speed (Fig. 4). Such subsystems which include the main memory, disk storage, and display electronics, exploit the chip's high-speed parallel bus and DMA channels. The MMU imparts the crucial ability to handle multiple tasks at once, like editing while printing.

#### **SAVING SLOTS**

In a workstation application, the chip's I<sup>2</sup>C interface serves wherever a slow response will do (for example, to support a keyboard or graphics input device). Using the slower interface frees the high-speed parallel bus for the subsystems that need it. Overall throughput also gets a boost, since the slower data transfers can occur at the same time as the faster ones.

Up to 16 Mbytes of main memory can connect directly to the chip's address and data buses because the internal DMA channels eliminate the need for an external controller. Moreover, because the chip easily accepts memory wait states, designers can choose the RAM that meets their cost and performance requirements.

The disk control subsystem employs the 68454 controller and a pair of 68459 disk phase-locked loop ICs. One of the PLL chips synchronizes the read and write timing for a flexible disk; the other handles the timing for a Winchester. In addition, low-power Schottky TTL circuits complete the drive- and head-selection interface.

A single intelligent graphics controller (like the 63484)

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MS710E	100kHz~23GHz	30kHz	_
MS710F	100kHz~23GHz	1MHz	_



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#### **DESIGN ENTRY**

#### Highly integrated 68000

handles the system's text and color display. It works with one of the microprocessor's DMA channels and can access a frame buffer of up to 2 Mbytes. Moreover, it draws 1 million pixels/s when clocked at 8 MHz. Where cost considerations are crucial and fewer features are needed, a less expensive CRT control subsystem can be built from Signetics' 267x family of display chips.

The keyboard and graphic input-control subsystems are built around two separate 80C51 microcontrollers. The microcontrollers consume little power, store their programs and data on chip, and carry their own serial I/O interface. One chip decodes key closures and sends data to the 68070 over the I<sup>2</sup>C bus' clock and data lines. The second microcontroller decodes and transmits X and Y position data from the graphics input device.

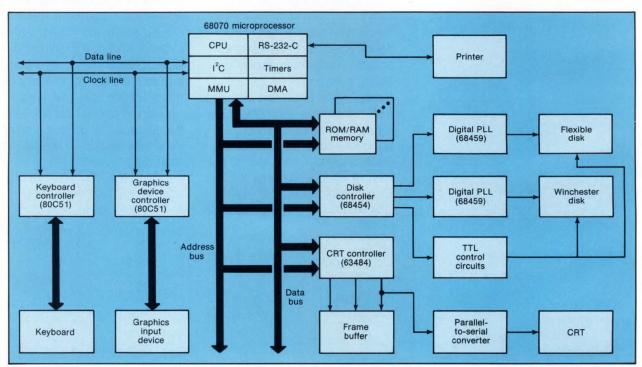
The basic workstation can be expanded through additional parallel and I<sup>2</sup>C buses. For instance, as design libraries grow, other kinds of mass storage, such as compact-disk ROMs, might be needed. A CD ROM interface, which is currently in development and compatible with the 68000 family, could be added onto the parallel bus. Similarly, additional hard copy peripherals like printers or X-Y plotters can be added to the RS-232-C interface, without the need for extra chips to convert data between serial and parallel formats.

Dirk Braune, a VLSI design manager, heads the 68070 project team. He earned a Dipl.-Ing. engineering degree in electrical control for Technische Universitaet Braunschweig in West Germany.

Jean-Claude Six is a 68000 sales support and product innovation manager. He has an engineering degree from the Institut Superieur d'Electronique du Nord in

Bob Rowe is a VLSI marketing manager at Signetics' MOS microprocessor division. He earned a BS degree with honors from the University of Notre Dame.

How valuable?	Circle
Highly	553
Moderately	554
Slightly	555



4. The 68070 forms the heart of a high-performance workstation that is also economical and expandable. Individual subsystems, many using the dual DMA channels, hang on the chip's various I/O buses. The subsystems manage disk, display, and keyboard operations. Upgrades and additions can be made later, as they are needed.

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#### Feature Size: 2 µ CMOS

	N-Channel	P-Channel
VTEO	0.5-1.0 <sub>V</sub>	0.5-1.0 <sub>V</sub>
BVDSS	>10 <sub>v</sub>	>10 <sub>v</sub>
$K^1 = \frac{\mu c}{2}$ linear region	21–25	6.5—8.5
B <sub>E</sub> (Long Channel)	$0.8 - 1.2 \text{V}^{1/2}$	$0.4 - 0.6 \text{V}^{1/2}$
Cap. Gate 10 <sup>4</sup> PF/cm <sup>2</sup>	8-10	8–10
Cap. Poly to Sub 10 <sup>4</sup> PF/cm <sup>2</sup>	0.55-0.65	0.55-0.65
Cap. Metal to Sub 10 <sup>4</sup> PF/cm <sup>2</sup>	0.27-0.32	0.27-0.32
Junction Depth	$0.4\mu - 0.6\mu$	$0.2\mu - 0.4\mu$
P-Well Junction	$2.5\mu - 3.5\mu$	
Poly Ps	15–30Ω/□	15–30Ω/□
Diffusion Ps	20-40Ω/□	60–100Ω/□
VTF Poly	>10 <sub>v</sub>	>10 <sub>v</sub>
ΔW	$-1.0\mu$	$-1.2\mu$
LEFF	$1.0\mu - 1.4\mu$	$1.3\mu - 1.7\mu$
Substrate Resistivity	2.5KΩ/□	$1.2\Omega/cm$

#### Feature Size: 3µ CMOS

	N-Channel	P-Channel
VTEO	0.5-1.0 <sub>V</sub>	0.5-1.0 <sub>V</sub>
BVDSS	>10 <sub>v</sub>	>10 <sub>v</sub>
$K^1 = \frac{\mu_c}{2}$ linear region	18-21	6–8
B <sub>E</sub> (Long Channel)	0.8-1.4 <sub>V</sub> <sup>1/2</sup>	0.4—0.6 <sub>V</sub> <sup>1/2</sup>
Cap. Gate 10 <sup>4</sup> PF/cm <sup>2</sup>	5.9-7.0	5.9- 7.0
Cap. Poly to Sub 10 <sup>4</sup> PF/cm <sup>2</sup>	0.45-0.55	0.45-0.55
Cap. Metal to Sub 10 <sup>4</sup> PF/cm <sup>2</sup>	0.2-0.25	0.2-0.25
Junction Depth	$0.6\mu - 1.0\mu$	$0.4\mu - 0.8\mu$
P-Well Junction	$3.5\mu - 4.5\mu$	
Poly Ps	15–30Ω/□	15–30Ω/□
Diffusion P <sub>s</sub>	10-30Ω/□	30–70Ω/□
VTF Poly	>10 <sub>v</sub>	>10 <sub>v</sub>
ΔW	$-1.0\mu$	$-1.0\mu$
LEFF	$1.4\mu - 2.0\mu$	$1.8\mu - 2.4\mu$
Substrate Resistivity	2.5K Ω/□	$1.0-1.5\Omega/cm$

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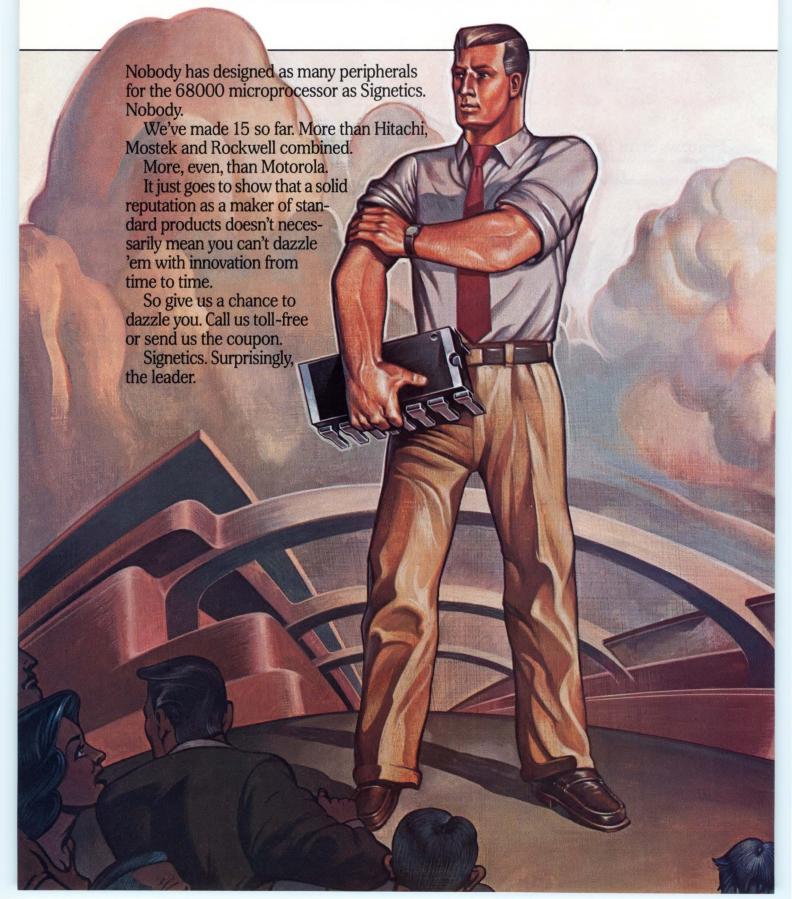


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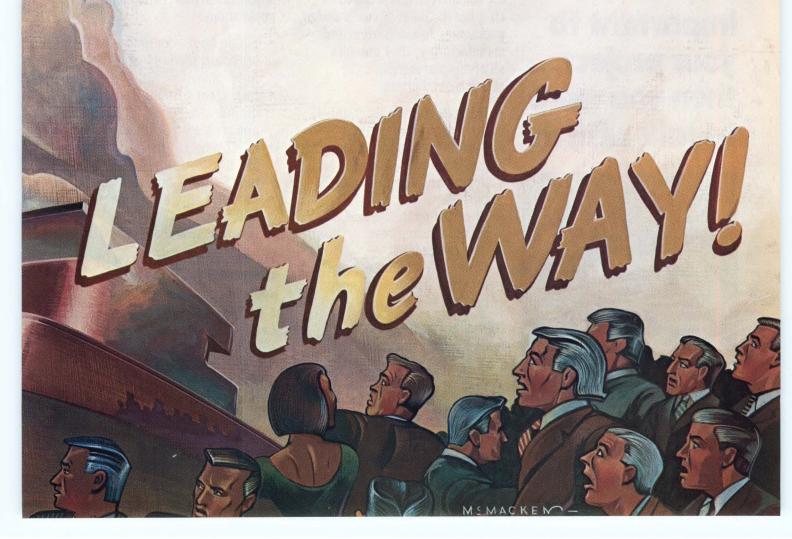
#### 68000 Peripherals Conceived and Designed by Signetics

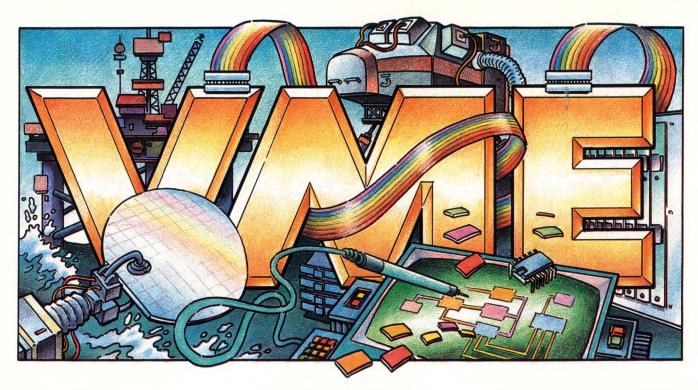
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68155	IVHAN	Interrupt Vectorizor and Handler	NOW
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68175	BUSMAS	VMEbus Master	NOW
68430	DMAI	Direct Memory Access Interface	NOW
68454	IMDC	Intelligent Multiple Disk Controller	NOW
68459	DPLL	Disk Phase Locked Loop	NOW
68562	DUSCC	<b>Dual Universal Serial Communications Controller</b>	NOW
68652	MPCC	Multi-Protocol Communications Controller	NOW
68653	PGC	Polynomial Generator Checker	NOW
68661	EPCI	Enhanced Programmable Communications Interface	NOW
68681	DUART	Dual Universal Asynchronous Receiver/ Transmitter	NOW
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68906	BMAC	Basic Memory Access Controller/32 bits	NOW
68920	MAC	32 bit Memory Access Controller.	Late 198

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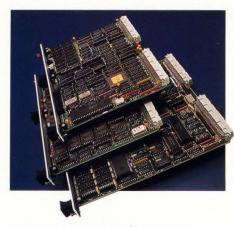
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### DESIGN ENTRY

**ELECTRONIC DESIGN EXCLUSIVE** 

# 1-Mbit DRAM controller shuns complex timing and protocol to streamline high-speed systems

System designers are looking for new and better ways to drive and control dynamic memory arrays. A fast controller provides an economical system solution with no drop in performance.

Zwie Amitai

Monolithic Memories Inc. 2175 Mission College Blvd. Santa Clara, CA 95054 (408) 970-9700 ext. 6196 In any system that uses dynamic RAMs, special circuitry in the address and control path must be introduced to drive the memory chips and link them to the CPU. The circuitry performs several functions: It generates refresh addresses; it multiplexes row, column, and refresh addresses; and it delivers control signals to dynamic RAMs. Moreover, it initiates the refresh cycles at the required rate to maintain data in the

memories and arbitrates between the refresh and access cycles. The sequence of the address and control signals must satisfy the protocol and timing requirements (row address hold, column address setup, and so on) of the dynamic RAMs themselves.

Most LSI dynamic RAM controllers aim at being a complete, single-chip solution by incorporating interface and access-refresh arbitration circuitry. However, because timing and memory-access protocol can vary greatly from one CPU to another, the effort of accommodating different systems is likely to compromise performance.

The touted flexibility of such controllers turns them into complex, multimode, power-hungry devices. Further, significant glue logic is still needed to interface the controllers with the memories, as well as with the system at large. The complexity and slow operation of these controllers have pushed many system designers to fashion their own controllers out of discrete SSI/MSI devices. Consequently, determination of an optimum level of integration has been a crucial factor in the development of a new family of controllers.

Designed for high-performance systems, the 673102, 673103, and 673104 controllers have simpler logic than has been available till now. A new oxide-isolated bipolar process shortens their propagation delays, minimizes delay variation, and paves the way for future models to operate in the industrial and military temperature ranges.

Each model has multiple Column Address Strobe input/output (CASIN/CAS) channels that increase addressing space and simplify individual byte access. Since the chips contain up to four independent CAS outputs, they are the first LSI controllers aimed at

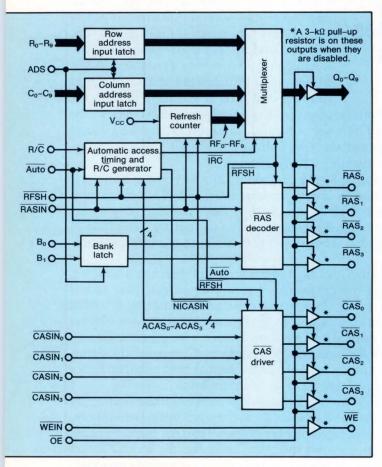
#### **DESIGN ENTRY**

#### Megabit DRAM controller

systems with 32-bit wide data.

The controllers provide all standard dynamic RAM control functions. They generate refresh addresses; multiplex row, column, and refresh addresses; generate the CAS, Row Address Strobe (RAS), and Write Enable (WE) control signals; and drive the memory array. Of their two access modes, one allows a designer to determine the control-signal timing sequence externally, the other automatically accommodates dynamic RAMs with access times of 150 ns or faster.

The externally controlled access mode gives the system direct and flexible control over the RAS, CAS, and address outputs. The controller serves as a straightforward multiplexer and driver for address and control signals to the dynamic RAMs. The Row Address Strobe input (RASIN) drives the particular RAS output selected by the bank-selection signals. The CAS outputs are indepen-



1. Multiple column address strobe input/output (CASIN/CAS) lines on the new 67310x controllers save the glue logic found on devices that carry only single channels. Other internal functions also cut parts count.

dently driven by their respective CASIN inputs, while the Row/Column input (R/C) controls the address multiplexer. In this mode, built-in propagation delays and skewing are minimized to achieve good resolution with any control-timing sequence. The externally controlled access mode supports page, static-column, and nibblemode accesses.

In the automatic access mode, once RASIN has been asserted, the chip automatically asserts RAS. It then switches the address multiplexer from row to column address and asserts CAS. The CASIN signals enable their respective CAS outputs and are active low. They can also be used to extend the time during which the CAS output and the column address are low. Specifically RASIN and RAS go high, satisfying precharge requirements for the next access cycle, while CAS stays low.

The new controllers contain a refresh counter, a threeway multiplexer, address and bank-selection latches, and output drivers for address and control signals (Fig. 1). A row decoder uses two bank-selection inputs to determine which of the four RAS outputs will be asserted, selecting one bank during a memory access and leaving the other three on standby.

All three models have four RAS outputs and one WE output. The 673102 and 673103, designed for 16-bit systems, have two CAS outputs, whereas the 673104, aiming at 32-bit applications, has four. Series resistors incorporated in the output stage of each line driver limit undershooting caused by inductive loads.

#### **REFRESHING THE BANKS**

When the refresh mode is selected, the refresh address is multiplexed onto the address outputs, and all four RAS outputs follow the RASIN input, refreshing all four banks.

The timing parameters for each model are specified for a load corresponding to 88 dynamic RAMs. The 673104 can address 16 Mbytes of dynamic memory arranged in four 4-byte banks; the 673103 can address 8 Mbytes in four 2-byte banks; the 673102, with nine address outputs, can address 2 Mbytes.

To allow the designer greater flexibility, the controllers do not incorporate system-independent handshaking and arbitration circuitry; instead, those circuits can be implemented through discrete or programmable logic devices. The multiple CASIN and CAS channels can connect to the system's byte-data strobes for individual byte access. Eliminating the logic required to split a single CAS output for that function helps control skewing and reduces the chip count.

The 67310x controllers enjoy several advantages over

those using discrete SSI/MSI devices. For instance, they need fewer chips, which occupy a smaller board area and cost less. In addition using fewer chips improves overall system reliability. While the placing of address and control signal drivers on the same chip affords tighter skewing.

A discrete design may use dynamic RAM drivers on the address and control lines of the dynamic memory array. To satisfy the memory's address hold time from the time  $\overline{RAS}$  goes low, the address propagation delay is based on the driver's best-case delay (4 ns) while the  $\overline{RAS}$  propagation delay is based on the worst-case delay (30 ns). When computing the required delay ( $t_1$ ) between  $\overline{RASIN}$  and  $\overline{R/C}$ , the 26-ns difference between the best-and worst-case delays must be added to the required address hold time. (The possibility of different devices being used on address and control lines makes it essential that these propagation delays be considered in circuit design; furthermore, the difference between the multiplexer's

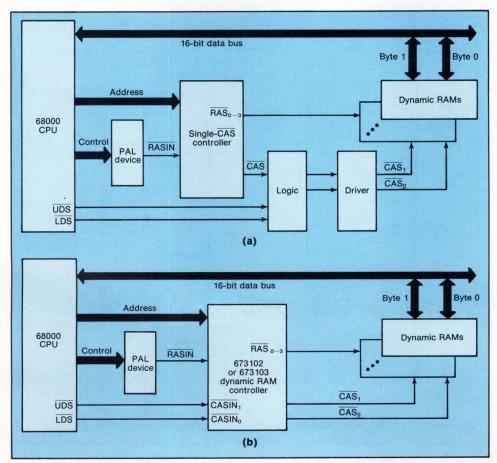
#### Price and availability

The price of each of the 673102 dynamic RAM controller is \$21.75; the 673103, \$39; and the 673104, \$46—all in 1000-piece quantities. The chips are available immediately. CIRCLE 506

best- and worst-case performance must be taken into account.)

Integrating drivers for address and control on the same controller chip more closely controls the differences between RAS, CAS, and the address outputs. A difference parameter is specified for the device's externally controlled access mode and is defined as  $t_{\rm DI} = t_{\rm RPDL} - t_{\rm RAH} = 0$  to 15 ns. Here  $t_{\rm RAH}$  equals the period from R/C low to row address not valid, and  $t_{\rm RPDL}$  equals the period from RASIN low to RAS low.

To guarantee a 15-ns row-address hold time,  $R/\overline{C}$  may be pulled low as early as 30 ns after  $\overline{RASIN}$  has gone low



2. Previous methods of addressing single bytes in large data words required extra logic and line drivers (a), which added both propagation delay and expense. By integrating these functions, the new controllers streamline the design (b).

#### Megabit DRAM controller

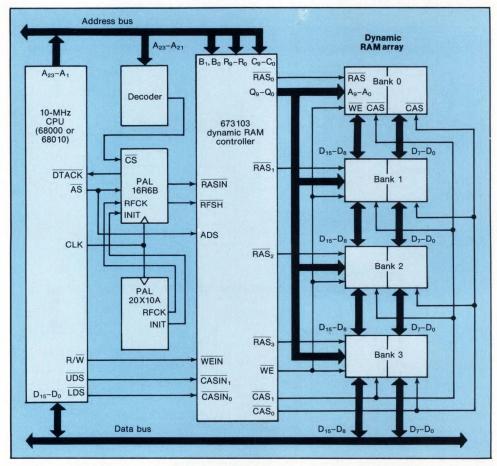
 $[t_1 = t_{D1} \text{ (min)} + t_{RAH} = 15 + 15 = 30 \text{ ns}].$  Another difference specification,  $t_{D2} = t_{CPDL} - t_{RCC}$  (where t<sub>CPDL</sub> equals CASIN low to CAS low and t<sub>RCC</sub> equals R/C low to column address valid), provides tight control for the column-address setup time (t<sub>ASC</sub>).

Unlike other currently available controllers, which have only one CAS output, the chips can be used in any system with 16- or 32-bit data to access any combination of bytes simultaneously. When a single-CAS dynamic RAM controller tries to access word-wide memory, external logic is needed to split the CAS output from the controller and create separate CAS signals for the individual bytes of the data word. Along with the required external drivers, this external logic adds to the system's chip count and extends the delay in propagating the CAS signal (Fig. 2). For example, in designs using devices having only one CAS output, the added CAS delay is 40 ns, which dramatically increases t<sub>RICL</sub> (the RASIN-to-CAS

delay) and so degrades system performance.

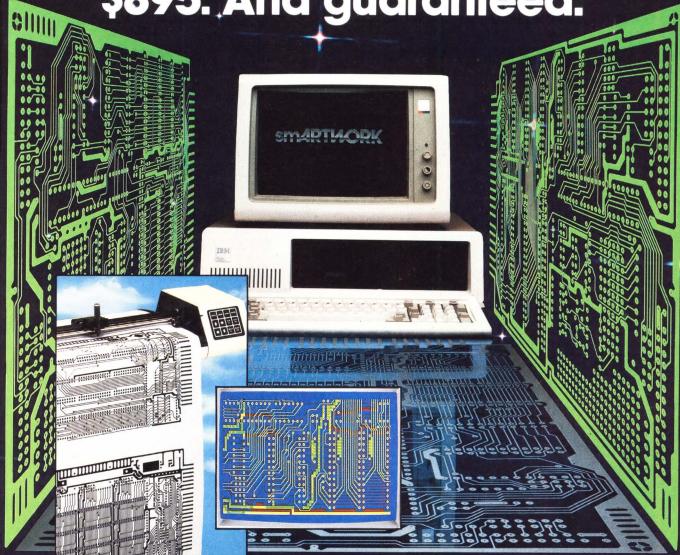
In systems with error detection and correction, separate controls are usually needed for data memory and check bits, a situation that calls for more than one CAS or WE signal. Since each of the new controllers carries at least two CAS outputs, one of those lines can be used to control the data while another controls the check bits. In systems that require separate WE signals for the data and the check bits, a designer may choose to control the memory array with one CAS signal and two WE signals. In such a case, the new controllers' CASIN and CAS channels operate independently in the externally controlled access mode; thus one CAS output may be connected to the WE inputs of the RAMs to produce the full complement of signals.

In a typical 16-bit system, a dynamic RAM array might be controlled by a 673103 that interfaces with a 68000 or a 68010 CPU through two programmable array



3. A system built around a 68000 or 68010 CPU and a 673103 dynamic RAM controller can run at 10 MHz and address 8 Mbytes of memory. Two programmable logic devices provide the refresh clock signal and handle all arbitration and handshaking functions.

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#### Megabit DRAM controller

logic devices (Fig. 3). One of these devices operates as a system clock divider and provides a refresh clock; the other performs arbitration and handshaking. The basic CPU circuitry includes an address decoder to select addressing spaces. The controller operates in the automatic access mode, with a hidden refresh scheme in the interface minimizing CPU wait states.

The hidden refresh scheme calls for a Refresh Clock signal (RFCK) to cycle in 15.6  $\mu$ s. Since one row of each dynamic RAM is refreshed during each cycle, all rows will be refreshed once every 2 ms, as specified by the memory manufacturers. The hidden refresh scheme operates when the refresh clock is high and the CPU is accessing memory elsewhere in the system.

The controller chip detects that condition when the Address Strobe signal (AS) is low but the Chip Select signal coming out of the address decoder is high. If the CPU continuously accesses the memory space addressed by the controller, hidden refreshing cannot occur. In that case, once RFCK goes low, the interface circuit allows the current access cycle to end and then initiates a refresh cycle.

During refreshing, the interface delays any request from the CPU for memory access until refreshing is complete and the RAS precharge requirements are met. A memory access cycle starts when AS is pulled low by the CPU and terminates once the interface circuitry responds by asserting the Data Acknowledge signal (DTACK).

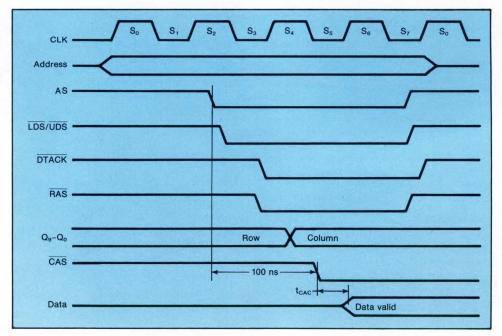
During a read cycle, data must be available to the CPU

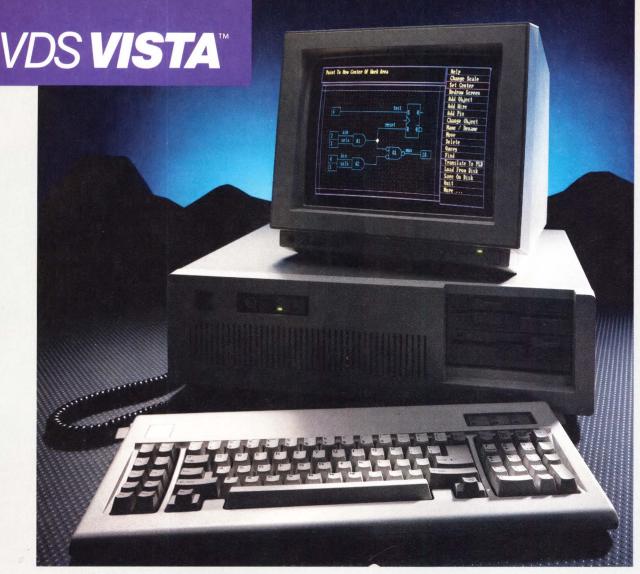
no less than 185 ns (for a 10-MHz design) after AS goes low, if no-wait-state operation is attempted. Since the data in this example is available 100 ns +  $t_{CAC}$  after AS goes to a logic low, no-wait-state operation can be achieved using 120-ns dynamic RAMs with a t<sub>CAC</sub> of 60 ns or less, leaving enough margin for buffer delays (Fig. 4). An early write cycle is used, so that data becomes available to the memory at least 20 ns before CAS goes low and is maintained at least 20 ns after CAS goes high. The design is 80 ns faster than a similar one using a controller with a single CAS output. Furthermore, it requires at least one chip fewer than designs using other kinds of controller. The design was built and tested at 10 MHz with no wait states and using 120-ns dynamic RAMs.□

Zwie Amitai is a product planning supervisor. As a planner, he did market research, system and logic design, and simulation for the 67301x family. When the chips were fabricated, he also helped write the test program and plan marketing strategy. Amitai has a BSEE from Ben-Gurion University in Israel and an MSEE from Brown University in Rhode Island.

How valuable?	Circle
Highly	556
Moderately	557
Slightly	558

4. Thanks to reduced propagation delays, the margins within the system allow 120-ns dynamic RAMs to run at 10 MHz without wait states.





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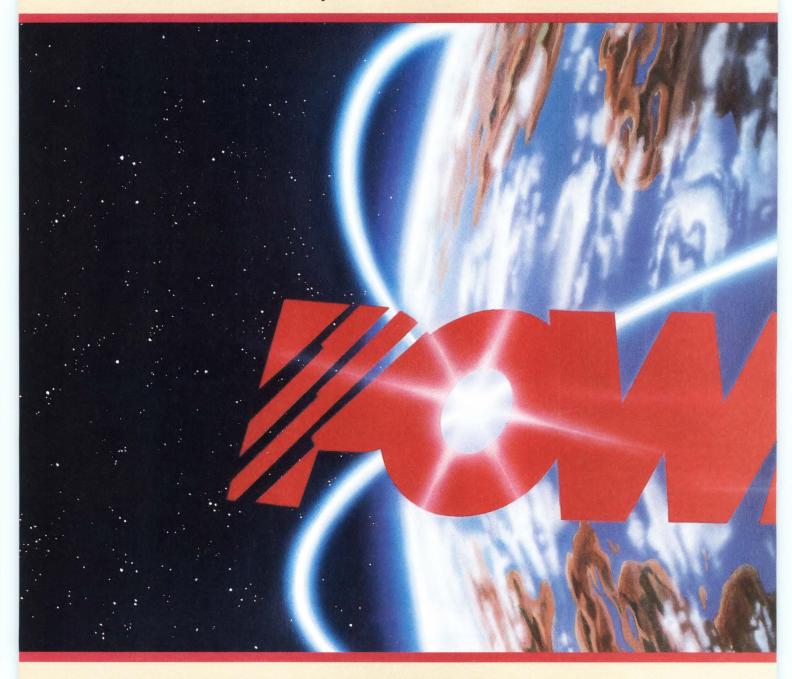
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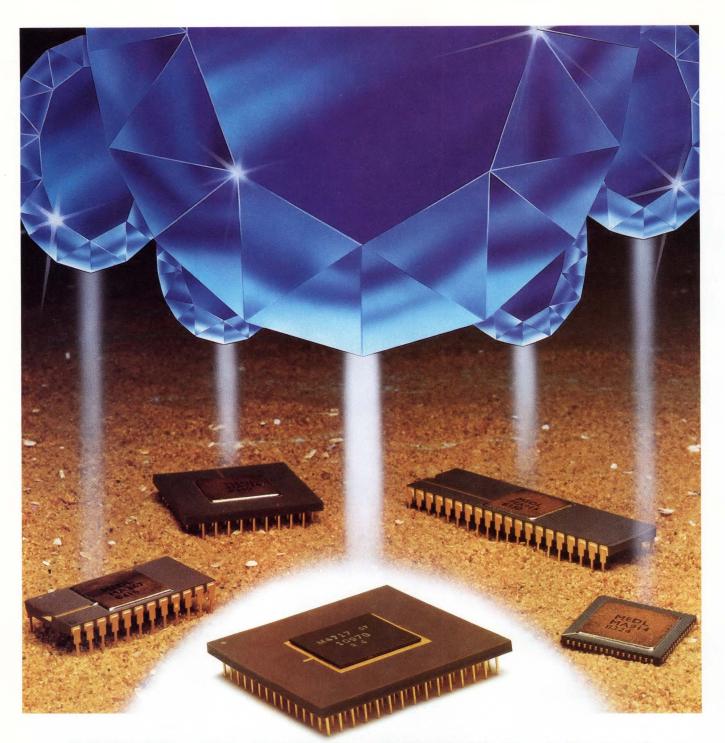
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CIRCLE 108

CIRCLE 109



ANALOG

**ELECTRONIC DESIGN EXCLUSIVE** 

# Converter handles 126-dB dynamic range signals with 15-bit accuracy

Until now, engineers designing scientific instruments capable of handling wide dynamic range analog inputs have been severely handicapped. Help is here: Analog Devices' AD367 combines a softwareprogrammable gain amplifier with the analog section of a dual-slope analog-to-digital converter, creating a voltage-to-pulse-width converter for slowly changing dc voltages. The converter has a dynamic range of 120 to 126 dB (20-21 bits) and an accuracy of 14 to 15 bits. Before, designers had to resort to various problematic approaches, such as filling a board with expensive components or resorting to in-house designs.

The 367's output is a pulse, the width of which is a direct linear function of the voltage out of the programmable gain amplifier at a scale factor between 360 and 410 µs/V. An external microprocessor or synchronous counter converts the width of the pulse into a digital word representing the converter's 15 LSBs.

The six MSBs are supplied by the six-bit input word that sets the gain of the programmable amplifier in 64 binary increments between 0.288 and 24. Operating with the virtually mandatory microprocessor, the voltage-to-pulse-width converter can be likened to a smart successiveapproximation converter in which the processor determines the MSBs by setting the gain of the amplifier just low enough so that its output does not exceed the full-scale input voltage of the integrating circuit.

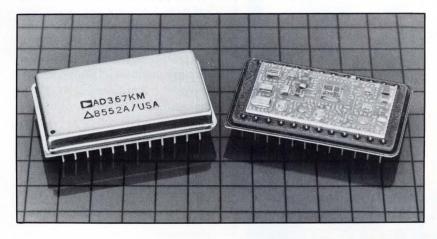
By choosing the value of the external integrating capacitor and the clock frequency, conversion time is user-selectable between 2 and 20 ms. The programmable-gain amplifier enables the device to handle full-scale input signals between 0.417 and 10 V, resulting in an LSB of just 305  $\mu$ V at maximum gain.

The linearity error of both the gain amplifier and the integrator are a maximum of 0.003% of full scale. The amplifier's gain error is no more than  $\pm 2\%$ , at any gain. The converter contains its own precision 10-V reference, which has a temperature coefficient of 15 ppm/°C

maximum. Alternatively, an external system reference may be used or the 367's reference can furnish up to  $500 \,\mu\text{A}$  to the system.

The impedance of the circuit's differential input is a minimum of 80 k $\Omega$ , and common-mode rejection is at least 70 dB. The converter typically draws 25 mA from  $\pm 15$ -V supplies and 30 mA from the 5-V rail. It is contained in a 24 pin hermetically sealed DIP and can operate from  $-25^{\circ}$  to  $+85^{\circ}$ C. The unit price, in quantities of 100, is \$130. Small quantities are available from stock.

Analog Devices Semiconductor, 804 Woburn St., Wilmington, MA 01887; Application Engineering Department, (517) 395-5565.





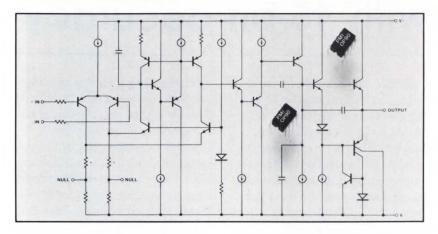
#### CIRCLE 111

## **NEW PRODUCTS**

**ANALOG** 

**ELECTRONIC DESIGN EXCLUSIVE** 

# Op amp is driven by $\pm$ 0.8-V supplies



Breaking records seems to be what the OP-90 is all about. Precision Monolithics' op amp needs an operating voltage of  $\pm 0.8$  V for a dual supply and 1.6 V for a single supply. Further, the device draws an unprecedented 20 µA operating current. The low supply voltage means that a smaller battery can be used to drive the op amp, thereby shrinking portable instruments in which they are used. Similarly, the small operating current also allows battery size to be reduced further. Nevertheless, despite its low power drain, the part displays an unusually high current drive of  $\pm 5$  mA, and it can drive loads up to 500 pf and still remain stable.

Most op amps require extra circuitry to remove an inherent residual 0.6 V that appears at the output when zero voltage is applied to the input. The OP-90, in comparison, requires no extra circuitry since it automatically produces a zero output for a zero input. What's more, at 700,000, the component exhibits the

**Curtis Panasuk** 

highest gain of any op amp operating under 100  $\mu$ A. The amplifier's input is  $3\mu$ V. Measured at 1 kHz, the noise density is  $60 \text{ nV/Hz}^{1/2}$ .

The low power of the device was achieved by adjusting the internal bias currents, which results in a reduced bandwidth of 25 kHz. The slew rate also was traded off to achieve low power: It is 8 V/ms. The offset voltage drift is  $1 \mu V/^{\circ}C$  and the power supply rejection ratio is  $10 \mu V/V$ . The input bias current hovers at 10 nA maximum and 5 nA typical. Finally, the commonmode rejection ratio comes in at over 110 dB.

The OP-90 is available now in sample quantities, with full production beginning in July. In quantities of 100, plastic 8-pin DIPs cost \$2.75 apiece. Ceramic DIPs cost \$3.75, in the same quantities. MIL-STD-883 parts can be had for \$14.90.

Precision Monolithics Inc., 1500 Space Park Dr., P.O. Box 58020, Santa Clara, CA 95052; Art Kapoor, (408) 727-9222, ext. 384.

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**ANALOG** 

**ELECTRONIC DESIGN EXCLUSIVE** 

# Intelligent modules link sensor to computer



Designers who must link one or more remotely sensed analog signals with a computer now have a family of small, low-cost, smart modules on hand to simplify the job. Capable of accommodating up to 32 channels over a multidrop RS-232 or RS-485 link, DGH's series D1000 works with input signals from virtually all common sensors. These include devices producing millivolt-level outputs as well as those producing currents, or pulse trains, in which the analog information is indicated by pulse width or frequency.

Squeezed into each module are an 8-bit microcomputer and circuitry for signal conditioning, analog-todigital conversions, communications, and on-off control. The signal conditioning circuitry excites the sensor and completes the bridges. The processor linearizes, compensates cold junctions, calibrates, and converts ASCII code into English. The communications circuits handle the RS-232/RS-485 signals, and

Frank Goodenough

the on-off circuits supply a minimum of one digital I/O.

Six basic modules have been designed to process particular signals or work with specific devices: voltages, currents, pulses, thermocouples, RTDs, and bridges. A seventh unit supplies seven digital inputs and eight digital outputs.

Each basic group of modules is rounded out by a number of versions. For example, the D1100 series comprises four models with fullscale ranges between 100 mV and 10 V. Similarly, the D1300 series contains eight variants for the eight most common thermocouples.

The units operate from 0° to 70°C and draw just 75 mA from 10to 20-V power supplies. Their dimensions are 3.6 by 2.45 by 0.85 in., and they are housed in lexan cases. Prices for single units run from \$250 to \$325. Small quantities are available from stock to 8 weeks.

DGH Corp., P.O. Box 5638, Manchester, NH 03108; Robert Glines, (603) 622-0452.

CIRCLE 312

#### R-d converter is programmable

A resolution of 10, 12, 14, or 16 bits is available with a single device from the RDC-19200 series of resolverto-digital converters. In addition to programmable resolution, a bandwidth of either 190 or 760 Hz may be selected. Accuracies of  $\pm 8$ ,  $\pm 4$ ,  $\pm 3$ ,  $\pm 2$ , and  $\pm 1$  min are available, as are two operating temperature ranges:  $-30^{\circ}$  to  $+105^{\circ}$ C and  $0^{\circ}$  to 70°C. A high-velocity output (VEL) in the RDC-19200 series is a ground-based voltage of 0 to  $\pm$  10 V dc for the maximum tracking rate of each programmed resolution. VEL can be scaled down with the addition of an external resistor. The converter comes in a 40-pin hybrid package.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, NY 11716; (516) 567-5600. From \$113.

CIRCLE 448

#### Chopper op amp minimizes error

Fabricated with Siliconix' Poly-MOS process, the Si7652 differential chopper-stabilized op amp offers low bias and offset current errors and reduces noise problems due to chopper charge injection at the amplifier inputs. Offset voltage, which is regulated without the use of potentiometers, is 5 µV maximum, and offset voltage drift is  $0.05 \mu V/^{\circ}C$ . Other specifications include bias current error of 30 pA maximum and noise of 0.2 µV pk-pk (dc to 1 Hz). Packages include 8and 14-pin plastic DIPs, 14-pin ceramic DIPs, and TO-99 cans.

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## NEW PRODUCTS

**ANALOG** 

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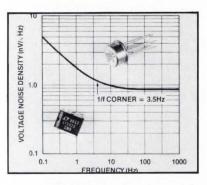
## Lowest noise op amp checks in at 1.1 nV/Hz 1/2

Input voltage noise for op amps has reached a new low. At 1000 Hz, the guaranteed maximum input noise of Linear Technology's LT1028 is onethird that of available op amps, just 1.1 nV/Hz ½ . What's more, its speed, offset voltage, 1/f noise, and high open-loop gain ensure that it remains precise from dc to beyond 100 kHz in high closed-loop gain circuits. The device is intended for designers who must handle fullscale ac and dc signals of a few millivolts or less, particularly from low source impedances.

Though basically aimed at dc applications, the design tricks needed to guarantee low noise also gave the op amp a minimum slew rate of 11 V/ $\mu$ s, lending it to precision audio applications (ELECTRONIC DESIGN, Feb. 20, p. 111). Its noise at 1000 Hz is less than the theoretical noise from a 50- $\Omega$  resistor, which means that it will not contribute errors when used with low-level sensors such as 100- to 350-Ω resistance-temperature detectors and strain gauges. The device's broadband noise between 0.1 and 10 Hz is a maximum of 90 nV pkpk, and its 1/f noise at 10 Hz is a maximum of 1.9 nV/Hz ½. The 1/f noise corner is just 3.5 Hz.

The input current noise (12 and  $1.8 \text{ pA/Hz} \frac{1}{2}$  at 10 and 100 Hz, respectively) is lower than that of super beta op amps. Of course, it cannot compete with that of biFET

Frank Goodenough



devices. Nevertheless, when used in the low-impedance circuits for which it is designed neither current noise nor its 260-nA bias current (over temperature) will cause even second-order errors.

The chip's offset voltage, a maximum of 180 µV over temperature, puts it in the OP-07 class, and its open-loop gain of at least 126 dB is far superior to that of the OP-07. The chip's gain-bandwidth product at 20,000 Hz is over 50 MHz, and it is stable down to a noise gain of two. About the only penalty paid for the 1028's performance is its almost 12 mA supply current—2 to 10 times that of typical op amps.

A total of 10 models are available, covering both commercial and military temperature ranges. They are housed in 8-pin cans and plastic and ceramic DIPs. In quantities of 100, the LT1028N8, a commercial unit in a plastic mini-DIP, costs \$4.95

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; Ed Ritter, (408) 942-0810. CIRCLE 310

# TURBOCHARGE YOUR PC'S GRAPHICS



...WITH A MATROX GRAPHICS BOARD

• 640 x 480 x 8 display (PG-640)

• 1280 x 1024 x 8 display (PG-1280)

• 40,000 vectors/sec. drawing speed

• 100% IBM PGC compatible

Full IBM CGA emulation

• 1 million pixels/second image load

Matrox now offers two new color graphics boards that dramatically boost PC performance. The PG-640 and PG-1280 provide the speed and resolution necessary to upgrade the IBM PC XT and AT into Professional Graphics workstations.

The PG-640 has a drawing speed of over 40,000 vectors/second and an image load speed of 1 million pixels/second. This means complex 640 x 480 pictures are drawn in under a second. The PG-1280 provides even faster picture updates, and displays four times the detail, 1280 x 1024 pixels.

Both the PG-640 and PG-1280 are 100% compatible with IBM's Professional Graphics card, and offer full Color Graphics Adapter emulation. All existing software runs without change.

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ANALOG

# Analog IC supports data separation

Designed to work in conjunction with the HDC9226 data separator and the HDC9224 hard-disk con-

troller, the HDC9223 eliminates all the discrete analog components that previously had to support the 9226. Additionally, the chip does away with all costly and time-consuming manual adjustments. Only a delay

line and a few resistors and capacitors are needed to supplement the device, thus forming a very compact subsystem that performs phase and frequency locking onto either MFM or FM data streams (double or single density). On-chip are a voltagecontrolled oscillator, analog filter, and pulse amplifier. A voltage regulator and bandgap voltage reference are also included to ensure stable operation and good power supply rejection. The HDC9223 operates from a +12-V supply, consumes 50 mA maximum, and is housed in a 14-pin Cerdip or plastic package.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, NY 11788; (516) 273-3100. \$10 in plastic (100 units); 10 to 12 weeks. CIRCLE 327

# Buffer improves input specs

A JFET-input voltage follower/ buffer guarantees 50 pA input bias current over the entire input voltage range of  $\pm 10 \text{ V}$  when the device is powered from  $\pm 15$ -V supplies (vs 2 nA for the industrystandard LH0033). The MAX460's cascoded input stage also increases the effective impedance to ground (3 pF in parallel with  $1000 \,\mathrm{G}\Omega$ ), allowing the device to be driven from very high impedances with no degradation in ac performance. Input characteristics are complemented by a bandwidth of 140 MHz, 1500-V/ $\mu$ s slew rate, and phase nonlinearity of 2 degrees. The maximum output current is specified at  $\pm 100$  mA.

Maxim Integrated Products, 510 N. Pastoria Ave., Sunnyvale, CA 94086; (408) 737-7600. From \$19.80 (100 units); stock.

CIRCLE 328



Delivering 1.5 or 3kW at 12 to 480 Vdc, these units are especially designed for high-power applications where tight regulation, low-ripple and high efficiency are critical. Features include: light weight, low panel height and high MTBF. Unique modular design and circuitry permit custom modification. Available rack-mountable or as OEM modules. Single or 3-phase. Call for complete details and custom design capabilities: 516-671-4400.

#### TYPICAL PERFORMANCE CHARACTERISTICS

. 117 Vrms, 220 Vrms 1-phase; 208 Vrms 3-phase . 47 Hz to 63 Hz, 400 Hz Input voltage Input frequency ..... 12 Vdc to 480 Vdc Output voltage Voltage adjustment range +20%, -10% of nominal value, wider adjustment range available Voltage regulation . < 1% line and load combined Adjustable from 40% to 100% of nominal rating Output current limit < 1% or 500 mV p-p, whichever is greater (lower ripple options Output voltage ripple available) Transient response Recovery time to normal range < 0.6 ms for 30% step load change Temperature coefficient < 0.02% per degree Centigrade 0 to 40 degrees Centigrade Ambient temp. (operating) EMI/RFI (conducted and radiated) . . Per FCC Class A and VDE 0875 limits

DISPLEX, LDC. Subsidiary of North Hills Electronics

1 Alexander Place, Glen Cove, New York 11542 (516) 671-4400. TELEX: 46-6886

# Simon says: "At LH Research, when Dr. Lee and I argue, our customers always win."



Introducing the LH Research MM Series: 26 models, 1 to 4 outputs, up to 28 V, up to 175 amps. LH is its own distributor—2 day shipment. 2 year guarantee.

"If you are not completely satisfied after trying them, call me at LH Research 714-669-2500."



14402 Franklin Avenue, Tustin, CA 92680

For price, delivery, and order placement call toll free: 1-800-LH SALES

# UL Recognized/CSA certified for easier system certification.

Also available upon request, similar units meeting VDE/IEC safety and VDE/FCC EMI specifications — contact factory.

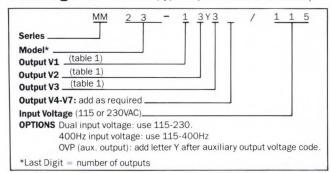
## Mighty-MITE® Switching Regulated Power Supplies

			OUTP	PUTS*			(	QUANTITY	PRICING	3
MODEL NUMBER	WATTS	MAIN	2	3	4	CASE	1-9	10-49	50-99	100
		VDC/AMPS	VDC/AMPS	VDC/AMPS	VDC/AMPS		1-9	10-49	50-99	100
MM11-0	375	2 @ 75				1	\$ 575	\$ 550	\$ 530	\$ 505
MM11-1	375	5 @ 75				1	575	550	530	50
MM11-2	375	12 @ 31				1	575	550	530	50
MM11-3	375	15 @ 25				1	575	550	530	50
MM11-5	375	24 @ 15				1	575	550	530	50
MM11-6	375	28 @ 13				1	575	550	530	50
MMX22-12	375	5 @ 75	12 @ 16			2	660	635	610	58
MM23-122	375	5 @ 75	12 @ 8	12 @ 8		2	690	665	640	60
MM23-133	375	5 @ 75	15 @ 8	15 @ 8		2	690	665	640	60
MM24-1221	375	5 @ 75	12 @ 8	12 @ 3	5 @ 5	2	750	720	695	65
MM24-1225	375	5 @ 75	12 @ 8	12 @ 3	24 @ 2	2	750	720	695	65
MM31-0	750	2 @ 175				3	690	665	640	60
MM31-1	750	5 @ 150				3	690	665	640	60
MM31-2	750	12 @ 62				3	690	665	640	60
MM31-3	750	15 @ 50				3	690	665	640	60
MM31-5	750	24 @ 31				3	690	665	640	60
MM31-6	750	28 @ 26				3	690	665	640	60
MM43-121	750	5 @ 150	12 @ 10	5 @ 12		4	925	890	855	81
MM43-122	750	5 @ 150	12 @ 10	12 @ 10		4	925	890	855	81
MM43-133	750	5 @ 150	15 @ 10	15 @ 10		4	925	890	855	81
MM44-1221	750	5 @ 150	12 @ 10	12 @ 5	5 @ 5	4	995	960	920	87
MM44-1122	750	5 @ 150	5 @ 12	12 @ 5	12 @ 5	4	995	960	920	87
MM44-1331	750	5 @ 150	15 @ 10	15 @ 5	5 @ 5	4	995	960	920	87
MM52-1/2	750	5 @ 75	12 @ 31	10 @ 0	3 (6) 3	5	1000	960	925	87
MM64-1/022	750	5 @ 75	2 @ 75	12 @ 10	12 @ 10	6	1150	1100	1065	100
MM64-1/122		5 @ 75	5 @ 75	12 @ 10	12 @ 10	6	1150	1100	1065	100

CAUTION: Total loading of all outputs not to exceed rated output power.

Prices subject to change without notice.

#### Ordering Information (Typical part number encoded)



Tat	ole 1
0 = 2VDC	4 = 18VDC
1 = 5VDC	5 = 24VDC
2 =12VDC	6 = 28VDC
3 =15VDC	8 = 48VDC

#### **Options for MM Series**

#### DELIVEDY.

Most MM Series Switching Power Supplies with selected options are shipped within 48 hours after placement of your order. Units with optional dual 115/230VAC input, or with optional 115VAC/400Hz input require 3-4 weeks.

OPTIONS	QUANTITY 1*
Dual 115/230V input	\$ 28.00
115V, 400Hz Input	160.00
OVP on auxiliary outputs	
1 auxiliary output	22.00
2 auxiliary outputs	44.00
3 auxiliary outputs	66.00
4 auxiliary outputs	88.00
5 auxiliary outputs	110.00
6 auxiliary outputs	132.00

\*For multiple unit pricing, contact factory.

<sup>\*</sup>Many additional standard voltage/current output combinations are available; refer to 1985 General Catalog or contact factory.

## **Product Specifications**

#### **OUTPUT POWER**

375 to 750 Watts maximum.

#### **OUTPUT VOLTAGES**

 $2,\,5,\,12,\,15,\,18,\,24,\,28\text{VDC}$  . 48VDC available on some models; contact factory.

#### **OUTPUT CURRENT**

See specific model

#### **NUMBER OF OUTPUTS**

1 to 7

#### COOLING

Fan. 100CFM airflow-fan intake, chassis vent exhaust.

#### **INPUT VOLTAGE**

115VAC  $\pm$  10%, or 230VAC  $\pm$  10%, 47-63Hz.

#### HOLD-UP TIME

20msec in regulation minimum, after removal of nominal AC input.

#### LINE REGULATION

0.4% over entire input range for all outputs.

#### LOAD REGULATION

0.4% from no load to full load for all outputs.

#### INTERACTION (CROSS REGULATION)

0.1% maximum.

#### PARD (RIPPLE & NOISE)

1%p-p or 50mV, whichever is higher.

#### **EFFICIENCY**

Up to 80%; 65% typical.

#### **POWER FAIL DETECTION**

Upon removal of AC, the power fail signal drops to logic zero at least 2msec before loss of DC output. Upon AC turn-on, signal remains low until outputs are in regulation.

#### **OVERVOLTAGE PROTECTION**

Standard on V1. Factory set for 125%  $\pm$  5%. Optional on auxiliary outputs.

#### **CURRENT LIMIT**

All outputs have fold-back current limiting to less than 50% of full load rating under short-circuit.

#### REVERSE VOLTAGE PROTECTION

To 100% of rated current for main output(s).

#### **OVERTEMPERATURE PROTECTION**

Internal thermal switch turns off power supply if overheating occurs.

#### **OVERSHOOT & UNDERSHOOT**

2% maximum deviation with a load change of 25% at  $5\text{A}/\mu\text{sec}$  . No overshoot or undershoot during AC turn-on or turn-off.

#### RESPONSE TIME

 $200\mu sec$  to within 1% after a 25% load change at  $5A/\mu sec$  .

#### **TEMPERATURE COEFFICIENT**

 $\pm 0.02\%$ °C from 0°C to 50°C after half hour warm-up

#### **OPERATING TEMPERATURE**

0°C to 70°C, full power to 40°C. Derates linearly to 60% power at 70°C.

#### STORAGE TEMPERATURE

-55°C to 85°C

#### **VOLTAGE ADJUST RANGE**

±5% minimum, all outputs.

#### MINIMUM LOAD

Zero for single output models. 10% required on V1 of multiple output models to insure regulation of auxiliary outputs. Contact factory for minimum load if main output is other than 5V. Lack of minimum load will not damage supply.

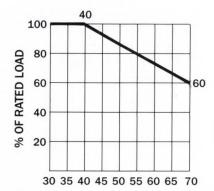
#### **OUTPUT POLARITY**

All outputs are floating and may be referenced to each other or chassis ground as required. Outputs may be isolated up to 100 volts from chassis ground.

#### LIMITED INRUSH CURRENT

The AC input inrush current is limited to 42A rms when averaged over one cycle.

#### POWER DERATING CURVE



T\_-AMBIENT TEMPERATURE-°C

#### REMOTE SENSE

Standard on main outputs and auxiliary outputs having 5V current rating of 10A or greater. Compensates for up to 250mV of total lead cable loss. All outputs are internally sensed if the sense leads are opened.

#### **REMOTE ON/OFF**

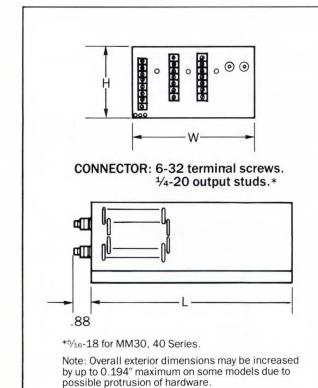
The power supply is turned on with open circuit or TTL logic '1', and turned off by switch closure or TTL logic '0'.

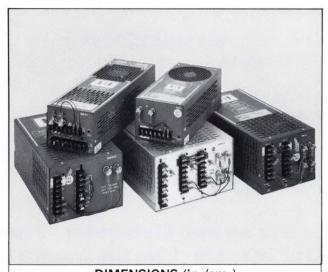
#### SAFETY

UL recognized. CSA certified.

#### **OPTIONS**

OVP on auxiliary outputs. Dual 115-230VAC inputs. 400Hz input.





	DIMENSION	S (in./cm.)	
Case Size	L	W	Н
1	11.12/28.24	5.00/12.70	3.90/9.91
2	14.25/36.20	5.00/12.70	3.90/9.91
3	11.75/29.85	5.00/12.70	5.00/12.70
4	11.75/29.85	7.00/17.78	5.00/12.70
5	12.50/31.75	6.50/16.51	5.00/12.70
6	12.50/31.75	8.50/21.59	5.00/12.70

# Simon says: "LH Research is number 2, my guardian angels are working to make us number 1 with you."



Nine major product lines.

Standard models 10 to 1500 watts, 1 to 9 outputs.

Seven factories in three countries on two continents.

250,000 sq. ft. dedicated to manufacturing switching regulated power supplies.

100 professional people dedicated to engineering and engineering support.

2 year guarantee on the MM Series.

Nationwide sales force.

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LH Research, Inc., the world's largest dedicated manufacturer
of switching regulated power supplies.

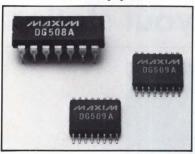


14402 Franklin Avenue, Tustin, CA 92680

For price, delivery, and order placement call toll free: 1-800-LH SALES

**ANALOG** 

# Multiplexers have ± 0.2 mA supplies



Two analog multiplexers are intended for high-speed general-purpose applications. The DG508A is an eight-channel multiplexer, while the DG509A is a differential four-channel device. Both parts are guaranteed not to latch up and operate from  $\pm 4.5$  to  $\pm 18$  V. Key specifications, which

reflect improvements over industry-standard devices, include positive and negative supply currents of 0.2 mA (reduced from  $\pm$  2.4 mA), drain-off and drain-on leakage currents of 5 nA maximum (vs 20 nA maximum), and a lower source-off leakage current of only 1 nA maximum. They also feature a lower drain-to-source on-resistance of 130  $\Omega$  typical, vs 230  $\Omega$  for many comparable devices. The parts are available in 16-pin plastic DIPs, Cerdips, and small-outline packages.

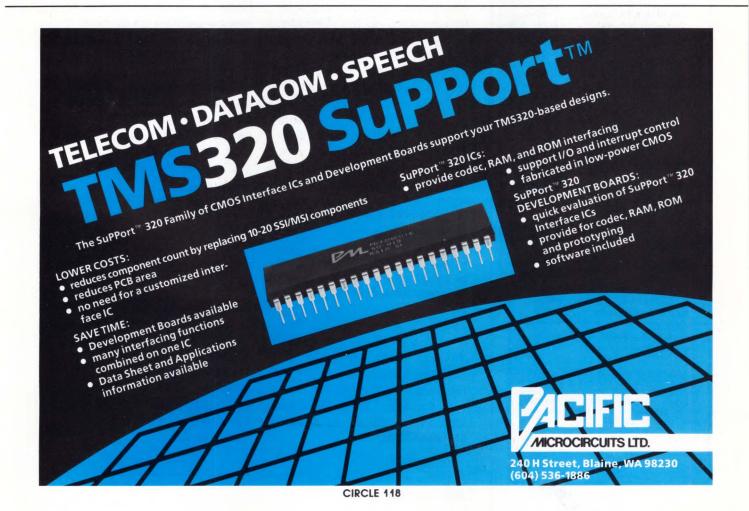
Maxim Integrated Products, 510 N. Pastoria Ave., Sunnyvale, CA 94086; (408) 737-7600. Prices range from \$4.30 to \$9.60 (100 units); stock.

CIRCLE 329

#### Op amp improves key parameters

An improved version of the industry-standard LM148 quad op amp, Precision Monolithics' PM-148 boasts an input offset voltage of 2.5 mV maximum, input offset current of 10 nA maximum, and input bias current of 75 nA maximum. Packaged in a 14-pin ceramic DIP, the amplifier is offered in grades specified over the full military and industrial temperature ranges.

Precision Monolithics Inc., 1500 Space Park Dr., Santa Clara, CA 95052; (408) 727-9222. \$2.50 (industrial grade); \$3.65 (military grade); \$5.75 (883C processing); stock.



### **Design electronic** circuits that perform as you want them to when translated into hardware

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Packed with the latest procedures in electronic design . . . and essential reference data . . . this practical guide will help you....

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go from ideas to prototypes to production in much less time with these and many other circuits: audio preamplifiers / driver and power amplifiers tuned amplifiers / AGC and related circuits wide-band amplifiers / oscillators / plus contextual circuit analysis, filter design, transient circuit design, and linear RC-voltage bootstrap circuitry.

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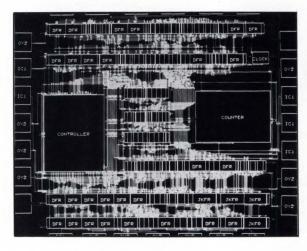
CIRCLE 119

## **NEW PRODUCTS**

COMPUTER-AIDED ENGINEERING

**ELECTRONIC DESIGN EXCLUSIVE** 

# Compact chip design ensured by layout station



Fully automatic cell placement and routing and a highly interactive interface distinguish the CellMaster IC layout station for cell-based designs. Daisy's system handles both uniform and odd-sized standard cells, as well as user-designed circuit elements. A compact chip layout is guaranteed by a simulated annealing algorithm that reduces chip area 10% to 20% when compared with traditional cell placement tools. What's more, the designer can squeeze out even tighter layouts using the layout station's interactive polygon editor.

The system employs a freeformat topology that allows cells to be placed anywhere on a chip. Not only does the station easily accommodate odd-sized cell blocks, it allows blocks to be "imported" from other systems. It also ensures that standard blocks are mixed efficiently with unusual-sized cells (see the figure).

In operation, design rules and

Stephan Ohr

special contingencies (like isolation layers or minimum spacings between transistors) are specified by the user on input forms displayed on the workstation screen.

For all operations that are not handled automatically, the station furnishes an on-line design rule check and an on-line electrical connectivity check. That eliminates the need for much of the expensive physical and electrical design rule checking.

The automatic cell placement and routing software runs under the user's supervision and control. The designer is able to interrupt, modify, or restart the process at any time. In addition, any editing changes are shown automatically in the layout.

The CellMaster is a turnkey system that sells for \$125,000. Shipments will begin in July.

Daisy Systems Corp., 700 Middlefield Rd., Mountain View, CA 94039; Pam Lawrence, (415) 960-6400.



### YOUR ELECTRONIC LINK TO THE FUTURE

Goldstar Electric has been continuing Lucky-Goldstar's pattern for high sophistication in advanced technology with the production of components and telecommunication equipment since 1970. Since then, company sales increased 200-fold, indicating world-wide trust in Goldstar Electric quality and reliability.

Goldstar Electric, long known as a specialist in carrier communication equipment, has applied the same recognized excellence in the production of printed wiring boards used in industrial and consumer electronic products.

Goldstar PWBs were given UL approval in 1979 and are made according to AT&T specifications. Goldstar Electric uses the latest CAD/CAM equipment to produce all types of PWBs; single-sided, doubled-sided through-hole, flexible, and even the latest multi-layer types.

For PWBs that incorporate zero defect, value and reliability, choose Goldstar PWBs. The price is more than right.

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COMPUTER-AIDED ENGINEERING

## Software tracks engineering tasks

A project management software package will help keep track of everexpanding CAE component and drawing libraries, as well as record those engineering tasks conducted by dozens of CAE system users over long periods. The Sherpa Data Management System (DMS), from Sherpa, automatically tracks and controls data, drawings, documents, and revisions related to a complex engineering project. Designed to run on a VAX under VMS, DMS oversees complicated projects such as designing ICs and creating multimodule software.

The DMS actually performs two services. First, it supplies integrated

data-base management. Second, it manages projects.

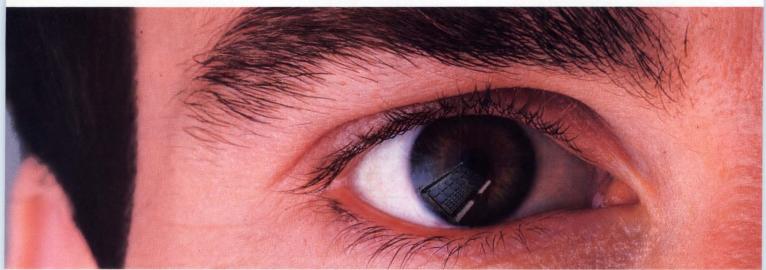
Integrated data-base management is performed by object-oriented software that assigns encrypted names to schematic diagrams, component files and libraries, simulation data, and so forth. While the content of these files remains untouched, the encrypted names become part of DSM-controlled directory.

Project management is performed by assigning a history and access structure to a record in the directory. Thus a hierarchy of users, passwords, and time stamping can be applied to all records. A separate project management record identifies who uses what file and when. The record is kept automatically by the system.

In addition to controlling access, the Sherpa system helps authorized users find a particular CAE file. It will also alert users to important changes in the structure, such as a new sign-off procedure.

The software costs from \$50,000 to \$80,000, depending on the size of its VAX host. Delivery is from stock.

Sherpa Corp., 2355 Old Oakland Rd., San Jose, CA 95131; Stuart Harrison; (408) 942-1535. CIRCLE 313



# ITI PROCESSES IMAGES FAS

In machine vision image processing systems, 'fast' used to mean 1/30 of a second – one video frame time. But there's a new name for fast image processing: Series 150.

Faster than Real Time.

Designed for VMEbus computers, the unique areaof-interest capabilities of the Series 150 modules let you process image subregions at 10 MHz. That means you can define an area of interest within the image, and process it many times in one RS-170 video frame. The Series 150 also gives you 512x512 spatial resolution, plus three separate areas of frame memory on a single board: one 16 bits deep, and two 8 bits deep. You can perform full-frame 4x4 convolutions in real time – the equivalent of 340 MOPS. And its open architecture lets you cascade memory and processing modules into a pipeline of any length, so you can build the ideal image processing engine for your needs.

-RTC-150 -ALU-150 -ADI-150 -FB-150

COMPUTER-AIDED ENGINEERING

### CAE package bows in for Apollo 3000

Schematic entry and simulation tools that will run on the new Apollo 3000 are soon to be introduced by GE Calma. Called the Logic Series, the CAE system ranges from schematic capture all the way to computer-aided test development.

The Logic Series comprises three elements: The Logic Scribe, a schematic entry and project management system; the Logic Explorer, an interactive simulation system based on the Tegas simulator; and the Logic Examiner, an interactive test development system. The software is available as a turnkey system or as individual packages.

The menu-driven Logic Scribe



draws and edits schematics, handles hierarchical designs, automatically generates net lists, and checks rules. A built-in project manager takes care of back annotation. Together with the Apollo 3000, it costs \$19,400 for monochrome and \$27,300 for color versions.

The Logic Explorer is a full-range

mixed-mode logic simulator. The Explorer carries out simulations with behavioral, gate, or MOS transistor circuit descriptions. Including an Apollo 3000, it costs \$50,000 for monochrome, \$58,000 for color.

The Logic Examiner is an interactive test development station that helps users convert simulator data patterns into test vectors. It costs \$50,000—including a monochrome Apollo 3000; \$58,000, for color.

Delivery will begin in June.

GE Calma Co., 12096 Park Thirty-Five Circle, Austin, TX 78753; Carolyn Mullery, (512) 339-0779.

CIRCLE 320



# TER THAN YOU CAN BLINK.

IBM™ PC AT Development System.

Our packaged Series 151 subsystem uses the 150 modules and a proprietary IBM PC AT-to-VMEbus interface. OEM's get a powerful development environment; VAR's, system integrators, and end users, a high performance workstation to support all kinds of image processing applications.

Both the Series 150 and 151 come with

Both the Series 150 and 151 come with complete software subroutine libraries.

Both employ advanced gate array technology that we developed. And both deliver the performance that's made ITI the world leader in image processing modules and subsystems.

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CIRCLE 230 FOR SERIES 150 CIRCLE 231 FOR SERIES 151

#### **COMPUTER-AIDED ENGINEERING**

# PC package designs wire-wrap boards

Consisting of a graphics card, light pen, and software, an interactive graphic CAD/CAM package for the IBM family of personal computers can be used to develop wire-wrap or discrete-wired prototypes. The Pen-Entry PC allows the user to develop the wire-wrap board directly from schematics or through optional

links for downloading and exchanging data bases between schematic net files created by other packages, such as FutureNet or P-CAD, and other workstations, such as Daisy, Valid, or Mentor.

Wire Graphics Inc., 95 Sherwood Ave., Farmingdale, NY 11735; (516) 293-1525. \$5999.

# Accelerator speeds simulation tasks

The Mach 100 simulation engine is a hardware accelerator that simulates integrated circuits and printed circuit boards 500 times faster than software running on a VAX-11/780. The system operates at speeds of 250,000 events/s and has a capacity for 32,000 fourinput modeling elements. Like its big brother the Mach 1000, the Mach 100 is designed to accelerate industry-standard simulators, including third-party software packages and major in-house simulators. At \$25,000 for logic simulation and \$30,000 for logic and fault simulation, the Mach 100 costs less than most simulation software packages alone.

Silicon Solutions, 1380 Willow Rd., Menlo Park, CA 94025; (415) 321-8574.

**CIRCLE 332** 

# For 16-bit emulation, Microcosm beats Intel three to one.



It's a fact. For about the price of one Intel 16-bit in-circuit emulator, you could buy three from Microcosm. And get exceptional performance at a third the cost.

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Our 80286 probe provides real time transparent emulation operating in the Real Address Mode. And combined with a native software debugger, the same probe creates an ideal environment for your Protected Virtual Address

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Intel's development software tools are available on your PC. So with Microcosm, you get
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**MBII** 



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Zendex Corporation manufactures a broad range of standard and custom designed ZBX Expansion Mod-

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### **ZBX 488**

IEEE-488 Interface Module

- Complete intelligent interface to IEEE-488 1978 standard
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- RMX-86 drivers available.

### **ZBX 349**

Centronics Printer Interface Module

- Provides direct interface to Centronics compatible parallel printers through the SBX bus.
- Includes an eight foot interface cable which plugs into a 50 pin edge connector on the
- Generates data strobe and latches data for use by printer.

### **ZBX 361**

Dual Serial I/O **Expansion Module** 

- Provides two RS 232C serial communications channels using
- two 8251A programmable USARTs. Two 26 pin edge connectors for mating with
- standard 3M type connectors. Switch selectable dual baud rate clock with 16
- variable rates from 50-19.2K baud.



- **ZBX 280** SCSI Interface Module
- Supports floppy disk drives, Winchester drives and streaming tape drives.
- Supports I/O and DMA modes with DMA transfers up to 1.5M bytes/sec.
  Utilizes NCR 5380 chip which provides
- complete control of the SCSI bus and full handshake signals.
- RMX-86 drivers available.

### **ZBX 350**

Parallel I/O Expansion Module

- Provides 24 programmable I/O lines configured as three 8-bit
  - ports through one 8255 programmable peripheral interface.
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- Four 14 pin sockets.



HHH





**ZBX 288** SCSI with Clock/

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- Provides seconds, minutes, hours, day, date, month and year to any hos
- single board computer. Lithium battery provides power for five years.
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- RMX-86 utilities available



Provides one RS232C or RS 449/442 programmable

**USART** with software selectable baud rates through one 8251A programmable communications interface.

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### COMPUTER-AIDED ENGINEERING

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To give users an affordable entry into computer-aided design, T&W Systems has introduced EasyCAD to the IBM personal computer market for under \$500. All programs are accessed through pull-down menus, including a variety of drawing objects such as lines, points, polygons, and arcs. The package also provides automatic dimensioning, rubber-banding, and infinite zoom capabilities. In addition, EasyCAD files can be interchanged with VersaCAD and AutoCAD.

T&W Systems Inc., 7372 Prince Dr., Suite 106, Huntington Beach, CA 92647; (714) 847-9960.

CIRCLE 333

# Models simulate Am29300 chip set

Logic simulation models are available for Advanced Micro Devices' Am29300 series of 32-bit microprocessor building blocks. Smart-Models make it possible for system designers to simulate a complete board or even a system-level design on their CAE workstations. To aid hardware debugging, a series of checks for timing and other error conditions are built into each model with corresponding messages that appear during a simulation run.

Logic Automation Inc., 19545 N.W. Von Neumann Dr., Beaverton, OR 97006; (503) 690-6900. From \$900 to \$1500 per device.

**CIRCLE 334** 

# Affordable tools run on IBM PC

Design Computation offers three affordable CAD packages for use on PC-based engineering workstations, including the IBM PC and AT&T 6300. Draftsman-EE is a schematic graphics editor that carries a price tag of \$749. It supports such features as unlimited zoom, nested macros, and orthogonal rubberbanding. Input is accepted via a mouse or keyboard. For use with Draftsman-EE, an autorouter and net-list generator sell for \$2498 and \$295, respectively.

Design Computation Inc., 10 Frederick Ave., Neptune, NJ 07753; (201) 922-4111.

**CIRCLE 335** 

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CIRCLE 124

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For example, an engineer working for a major aerospace company was stopped by an integral dealing with turbulence and boundary layers. Pencil and paper in hand, he had been looking at:

$$\int (k \log(x) - 2x^3 + 3x^2 + b)^4 dx$$

for more than three weeks. He always arrived at a different solution, never knowing which was the right one.

Less than 10 seconds after entering the problem into the computer, MACSYMA gave him the correct answer. Not just numerically, but in symbolic terms that gave him real insight into the physical nature of the problem.

How long would it take you or your staff to factor this expression?

$$3w^2z^6 + 2w^3z^4 - 10w^2y^2z^3 + 141xyz^3 + 45w^2x^3z^3 - 3w^2z^3 + 94wxyz - 2w^3z - 470xy^3 + 10w^2y^2 + 2115x^4y - 45w^2x^3$$

MACSYMA gives you the answer. In seconds.

 $(3z^3 + 2wz - 10y^2 + 45x^3)(w^2z^3 + 47xy - w^2)$ 

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- Generate FORTRAN output from MACSYMA expressions
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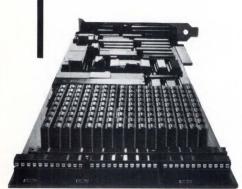
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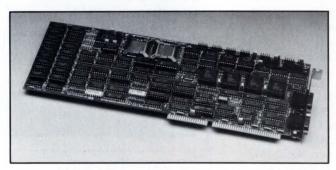
CIRCLE 126

# NEW PRODUCTS

COMPUTER BOARDS

**ELECTRONIC DESIGN EXCLUSIVE** 

# Drop-in board turns PCs into multiuser systems



Up until now, the promise of the IBM PC AT and its compatibles to serve as multiuser systems has remained unfulfilled. Although the PC AT's 80286, running under Xenix, executes multiple-programs, its performance degrades as the number of terminals increases. One way to ensure up to nine fully active users is to free the host CPU from communication-processing tasks. The DCP-2/86 MUX does exactly that. Developed by Persyst, the multiplexer board carries its own 80286, drops into any 16-bit expansion slot, and controls up to eight serial communication lines.

Designed for Xenix processing, the board directly controls the serial lines. It also preprocesses received data, translating characters and preparing data, thereby further offloading the personal computer. Additionally, its 128- or 512-kbyte memory is dual-ported and accessible to the host, eliminating buffering. A two-way interrupt scheme allows either processor to interrupt the other for critical transfers, and a software driver running under Xenix integrates the host and the coprocessor card.

**Ray Weiss** 

The board's eight serial lines work with asynchronous modems, and each is a full-duplex RS-232 port. Optionally, two of the lines can interface to synchronous modems, handling IBM's Bisync, SDLC, or HDLC line protocols. Also, each line can be configured as dataterminal or data-communication equipment (DTE or DCE). The card can be connected to an IBM mainframe with either Bisync or SNA protocols.

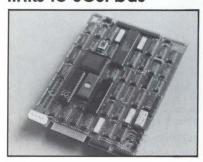
The DCP-2/86 MUX is a sixlayer board that is rfi-shielded and meets FCC Class B requirements. A special board assembly is supplied to support up to eight shielded line connections. The 2/86 MUX includes three programmable timers for timeouts and sequencing.

A single board, with 512 kbytes of memory, is priced at \$1795. If desired, an 8-MHz processor can replace the standard 6-MHz device, and the board can be configured to handle two synchronous modems. Those two options cost \$150 and \$100, respectively. A four-line board sells for \$1250.

Persyst Division, Emulex Corp., 3545 Harbor Blvd., Costa Mesa, CA 92626; (714) 662-5600. CIRCLE 319

COMPUTER BOARDS

# ESDI controller links to SCSI bus



The MD21 disk controller interfaces any two serial-mode ESDI 5<sup>1</sup>/<sub>4</sub>-in. Winchester disk drives with the Small Computer Systems Interface (SCSI) bus. The board comes with a 32-kbyte buffer and can interface through the SCSI bus with virtually any CPU. Emulex offers SCSI host adapters for Digital Equipment's Q-bus and Unibus systems, as well as the IBM family of personal computers (and compatibles).

Emulex Corp., 3545 Harbor Blvd., P.O. Box 6725, Costa Mesa, CA 92626; (800) EMULEX3 or (714) 662-5600. \$395.

**CIRCLE 336** 

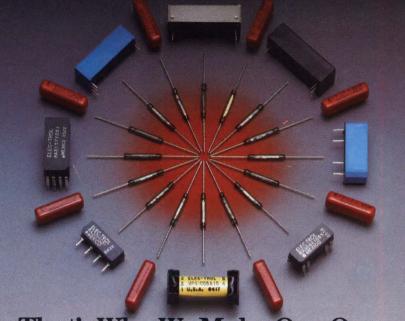
# Winchester card stores 30 Mbytes

A board-level hard-disk drive gives personal computer users 30 Mbytes of mass storage. Called the Drive-Card 30, the complete subsystem integrates two 3½-in. disk drives with controller electronics on a single plug-in card. It is compatible with the IBM family of personal computers and lookalikes, including most Compaq models and the AT&T PC 6300 and 6300 Plus.

Mountain Computer Inc., 360 El Pueblo Rd., Scotts Valley, CA 95066; (408) 438-6650. \$1449.

CIRCLE 337

# The Heart of a Hi-Rel Reed Relay is a Quality Reed Switch.



# That's Why We Make Our Own.

The heart of a reed relay is the reed switch.

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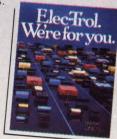
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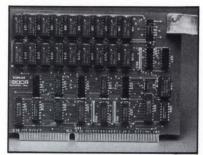
ELEC-TROL, INC., 26477 N. GOLDEN VALLEY RD., SAUGUS, CA 91350 TELEPHONE: (805) 252-8330 • TELEX: 310-372-0331

COMPUTER BOARDS

# Card fills out PC AT memory

Designed for the IBM PC AT, the TophAT memory board allows users to access the full 640-kbyte memory

capability of their computer. For the standard AT with 256 kbytes of RAM, a 384-kbyte version of TophAT is available. Likewise, for the enhanced AT with 512 kbytes of memory, a 128-kbyte card is avail-

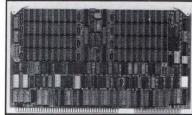


able. Used for conventional memory purposes only, the board does not require special software.

Boca Research Inc., 6401 Congress Ave., Boca Raton, FL 33431; (305) 997-6227. \$145 (128 kbytes) and \$195 (384 kbytes).

**CIRCLE 338** 

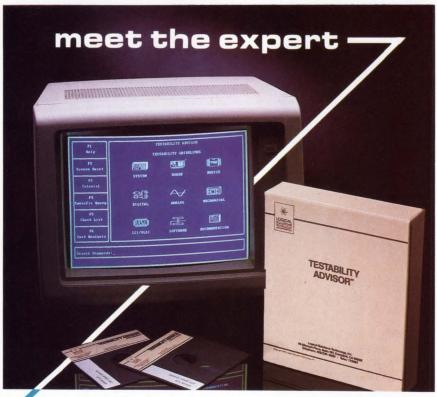




Offered in two versions, the LBX 512K-2M memory board adds up to 2 Mbytes of dual-port dynamic RAM to any Multibus system. The enhanced version delivers a typical read data access time of 145 ns (195 ns in the standard version) on the iLBX memory expansion interface. It operates without wait states in the asynchronous mode in systems based on Intel's 6-MHz 286/10 and synchronous with Intel's 8-MHz 286/10A or 286/12 CPU boards. Parity checking is standard, and both Multibus and iLBX cycles can optionally generate interrupts.

Central Data Corp., 1602 Newton Dr., Champaign, IL 61821; (800) 482-0315 or (217) 359-8010. \$1150 with 2 Mbytes (100 units).

CIRCLE 339



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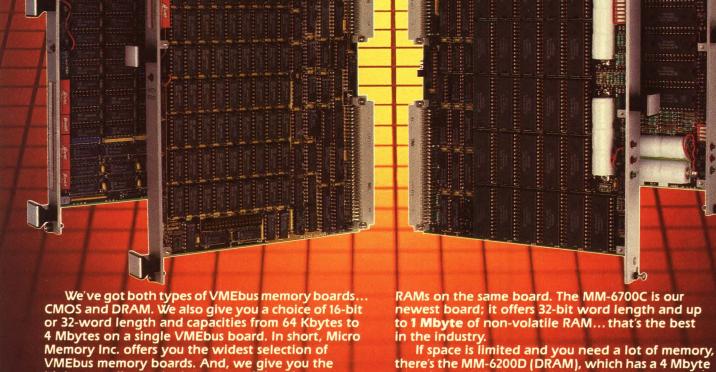
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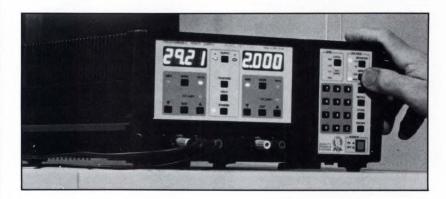


# NEW PRODUCTS

**POWER** 

**ELECTRONIC DESIGN EXCLUSIVE** 

# Variable supplies pump out programmable power



Precision and ease of programming mark the PD 7000 line of dual 60-W power supplies. From Quality Power Systems, the family comprises five members with outputs that range from 0 to 15 V at 4 A, to 30 V at 2 A, to 40 and 60 V at 1 A, and to 150 V at 0.25 A.

Each unit maintains its output to within  $\pm 0.005\% \pm 1$  mV and  $\pm 0.005\% \pm 1$  mA over line and load fluctuations. Combined output ripple and noise is  $300~\mu\text{V}$  and  $100~\mu\text{A}$  rms, and remote-sensing feedback corrects for voltage drops of up to 0.5~V in each lead. Moreover, voltage and current settings are guaranteed to stay within 0.02% over an eight-hour period. Outputs are floating and isolated, and all units are protected against overloads.

The voltage and current settings can be adjusted directly from a front panel keypad, or they can be set remotely. The supplies accept serial (RS-232-C) binary data and IEEE-488 commands. In addition, a battery-backed CMOS RAM holds 16 settings, and a ROM will perma-

Gil Bassak

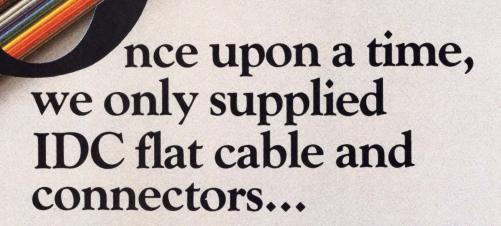
nently store the 5 most necessary output voltages.

The supplies' controls include Standby, which forces both outputs to zero, and Hold, which maintains the present output as new settings are entered. A third command, Tracking, makes certain that one output follows the other.

Programmable supplies often find their way into automatic test equipment. To facilitate test procedures, the new supplies can overlay their high and low voltage outputs with a 50-Hz ripple, as well as deviate ±10% from their settings. A single push button initiates each of the two changes. The supplies also run a series of self-tests when powered up. Error messages appear on the same twin LED displays that indicate the output voltage and current settings.

Each supply weighs 17.5 lbs, stands about 5.6 by 11.8 by 9.4 in., and occupies only 0.36 ft.<sup>3</sup>. Prices for single units start at \$1950.

Quality Power Systems, 2400 S. Texas Ave., Pearland, TX 77581; (713) 997-1700 (in Texas). Outside of Texas; (800) 922-1701. CIRCLE 322



# Take a look at us now!





**POWER** 

### Dc-dc converters pack 10.2 W/in.<sup>3</sup>



The LPS series of dc-dc converters consists of five models providing 5, 12, 15,  $\pm$  12, and  $\pm$  15 V at 15 W in a 1.6-by-2.0-by-0.46-in. package. All models maintain near constant efficiencies to 85% over the 3:1 input range of 20 to 60 V dc (48 V dc nominal). By using smaller magnets, made possible by a 200-kHz switching frequency, these units achieve a power density of 10.2 W per cubic in. without external heatsinking or forced-air cooling. Line regulation is  $\pm 0.5\%$  maximum; load regulation is  $\pm 0.5\%$  for single-output models and  $\pm 1.0\%$  for dual-output models (from full load to 1/4 full load).

Computer Products Inc., Power Conversion Group, 2900 Gateway Dr., Pompano Beach, FL 33069; (305) 974-5500. \$66.50 and \$69.30 for single and dual outputs (100 units); small quantities take four to six weeks.

CIRCLE 340

# Power transistors mount on surface

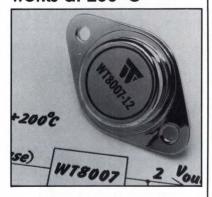
A wide range of power transistors, including bipolar and power MOS devices, are housed in a specially configured SOT-82 package for surface mounting. At a case tempera-

ture of 25 °C, the package can dissipate up to 65 W of power. Bipolar packages are available in  $V_{\rm CE}$  ranges of 60 to 450 V and current ratings of 0.5 to 10 A. Power MOS devices are offered in  $V_{\rm DS}$  ranges from 50 to 550 V. On-resistance ranges begin at 0.13  $\Omega$ .

SGS Semiconductor Corp., 1000 E. Bell Rd., Phoenix, AZ 85022; (602) 867-6100.

CIRCLE 341

# Voltage regulator works at 200°C



Designed for operation in severe environments, a hybrid linear voltage regulator withstands temperatures ranging from  $-55^{\circ}$  to  $+200^{\circ}$ C. The laser-trimmed output voltages of the WT8007-12, WT8008-12, and WT8009-5 are  $+12 (\pm 1\%)$ ,  $-12 (\pm 1\%)$ , and  $+5 (\pm 1.5\%)$  V, respectively. Both the line and load regulation for all three devices are  $\pm$  1% over the entire temperature range. At 25°C, foldback current for the 8007 and 8008 is 1.2 A, while the 8009 offers 2.2 A. The regulators come in hermetically sealed TO-3 headers.

White Technology Inc., 4246 E. Wood St., Phoenix, AZ 85040; (602) 437-1520. \$159 (8007 and 8008) and \$153 (8009) in lots of 100; stock to six weeks.

CIRCLE 342

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**POWER** 

# Dc-dc converters need 12-V source



A family of 3- and 6-W dc-dc converters is designed to operate from 12-V battery power sources. Ideal for use in portable instruments, the units convert standard 12-V dc battery power into single and dual sources of isolated  $\pm 5$ ,  $\pm 12$ , or  $\pm 15$  V dc. Isolation between the input and the outputs is 500 V dc. All outputs are protected against short circuits. The converters' compact 2-by-2-in. case is only 0.375 in. high to allow for minimum between-board spacing.

Calex Manufacturing Co. Inc., 3355 Vincent Rd., Pleasant Hill, CA 94523; (415) 932-3911. From \$93; stock to four weeks.

CIRCLE 343

# Power hybrids offer SPDT operation



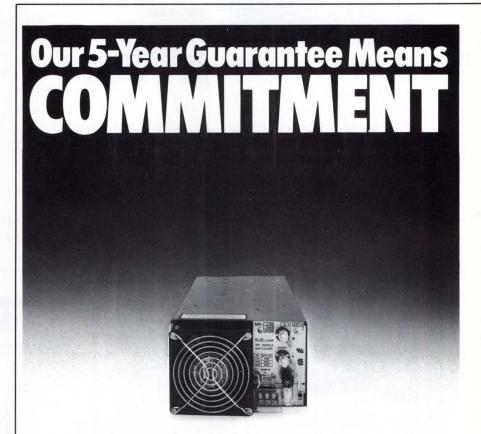
Intended to replace electromechanical relays in low-to-medium-power applications requiring a double-throw (form C) contact configuration, the M30 and M31 SPDT ac/dc power control hybrids provide a break-before-make switching function in a totally solid-state form. Models of the M30 series are rated up to 4.1 A and up to 380 V ac. Models of the

M31 series are rated up to 8.2 A and up to 380 V dc with an on-state resistance as low as  $0.15 \Omega$ . The devices are housed in a 22-pin low-profile hermetically sealed case.

Teledyne Solid State, 12525

Daphne Ave., Hawthorne, CA 90250; (213) 777-0077. \$106 and \$99 for the M30 and M31, respectively (250 units); 12 to 14 weeks.

CIRCLE 344



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COMMUNICATIONS

## Cable extender expands Apple LAN



A cable extender system is designed especially for Apple Computer's local area network, Appletalk. The color-coordinated system, which consists of a subminiature DIN plug (APP 9999) and cable extender (APE 9999), expands the network to as far as 300 meters (1000 ft). The extender connects to terminated Apple plug assemblies, while the DIN plug provides quick connection between the extender and

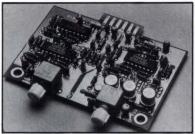
the dual connector tap. It terminates on standard Belden cables 9999 and 89999.

Belden Electronic Wire and Cable, P.O. Box 1980, Richmond, IN 47375; (317) 983-5200.

CIRCLE 345

### Optic transceiver hits 50 Mbaud

A fiber-optic transceiver is designed for applications requiring a 50-Mbaud data rate over a temperature range of 0° to 70°C. With a minimum optical power budget of 12 dB, the HFBR-0422 can function in fiber-optic links using HFBR-3000 series cable at distances of up to 2 km. The pc board



assembly, which contains a transmitter and receiver, supports circuitry that can interface with both TTL and ECL logic families. The device requires a single +5-V power supply, although the design and ECL components on the board also allow it to function at -5.2 V.

Hewlett-Packard Co., 1820 Embarcadero Rd., Palo Alto, CA 94303; call local sales office. \$185.

CIRCLE 346

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COMMUNICATIONS

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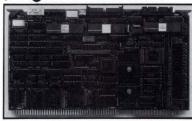
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# Ethernet board plugs into Multibus



A front-end processor provides a plug-in solution for standard Ethernet LAN interfaces. It can be used as a typical Ethernet node processor, functioning as a slave Ethernet Multibus controller, or it can be packaged with a power supply to function as a stand-alone serial/parallel/ SCSI gate to the Ethernet highway. Based on a 10-MHz 68000 microprocessor, the SBE/MLAN-11 comes with 128 or 512 kbytes of dynamic RAM. An on-board controller provides full-duplex DMA operation through the serial/parallel and iSBX channels.

SBE Inc., 2400 Bisso Ln., Concord, CA 94520; (800) 221-6458 or (415) 680-7722. \$1495 (100 units).

# Local network gets designers talking



As engineers increasingly rely on personal computers, there is a need to share information and resources. Although most networks are geared to business, FFT's MicroLAN 1553-NET was designed primarily to serve engineers.

Based on MIL-STD-1553B, the

network runs on IBM machines and lookalikes and joins as many as 254 nodes. All nodes interface directly with test and monitoring equipment and with the military's 1553 avionics bus. All resources on the network-disks, directories, files, tapes, displays, and other peripherals—can be shared. The CSMA/CD/CA network moves data at up to 3 Mbits/s and is able to pass data blocks as large as 64 kbytes. Either coaxial or twisted pairs can link nodes, and up to 1500 feet of the former can be driven without a repeater. Network software, PC/NOS, runs with MS- or PC-DOS. It defines a distributed network that does not require a master console or node.

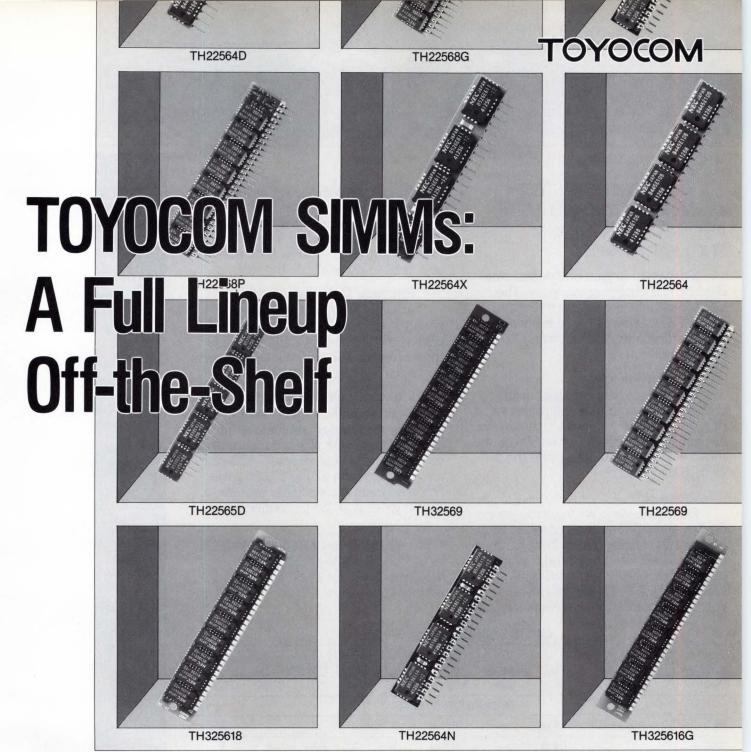
Fast Feedback Technologies Inc., 1505 Aviation Blvd., Redondo Beach, CA 90278; (213) 379-6100. \$350 (standard card); \$450 (with special on-board cache); stock.

CIRCLE 348

# LAN expander gives 4-way split

A network expander allows the installation of additional terminals in a local area network without cutting in new taps or reconfiguring the system in any way. Designed for midsplit systems with an outbound frequency range of 150 to 450 MHz and an inbound frequency of 5 to 112 MHz, the NE-4 takes one of the network drops and expands it to four. It provides the same output levels as the inbound and outbound frequency channels, even with a four-to-one split.

Augat Broadband Communications Group, 710 Narragansett Park Dr., Pawtucket, RI 02861; (401) 724-4400.



The Single In-line Memory Module is in vogue as never before among today's designers. By condensing a huge amount of memory into a small area, the SIMM is helping to slash the size of computers and electronic instruments and conserve valuable board space.

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centers in Mountain View, CA; Natick, MA; Dallas, TX; or Portland, OR.

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Start out with our gate arrays, optimize your design, then move into standard cells with NEC's computerized conversion. Our 1.5 micron CMOS gate arrays range from 320 to 20,000 gates. Standard cells are available with up to 17,000 gates and 256 I/O buffers.

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### CMOS ASIC Selection Guide

Gate		Prop.	Memory	Max. Toggle	Packages						
Count	I/O	Delay*	Bits	Frequency	DIP	Flat	PLCC	CPGA	PPGA		
			STANDAR	RD CMOS ARE	RAYS						
300 — 1500	54 — 100	1.4 ns	_	70 MHz	X	X	X		Х		
2000 — 20,000	84 — 266	1.4 ns	_	70 MHz	X	X	X	X	X		
		STA	NDARD CM	OS ARRAYS V	VITH RA	M					
2240	120	1.4 ns	2K	70 MHz	X	X	X	X	X		
4440	180	1.4 ns	4K	70 MHz	X	X	X	X	X		
			STAN	DARD CELLS							
800 — 17,000	up to 256	1.4 ns	_	70 MHz	X	X	X	X	Х		

<sup>\*</sup> (f/o = 3, L = 3 mm)

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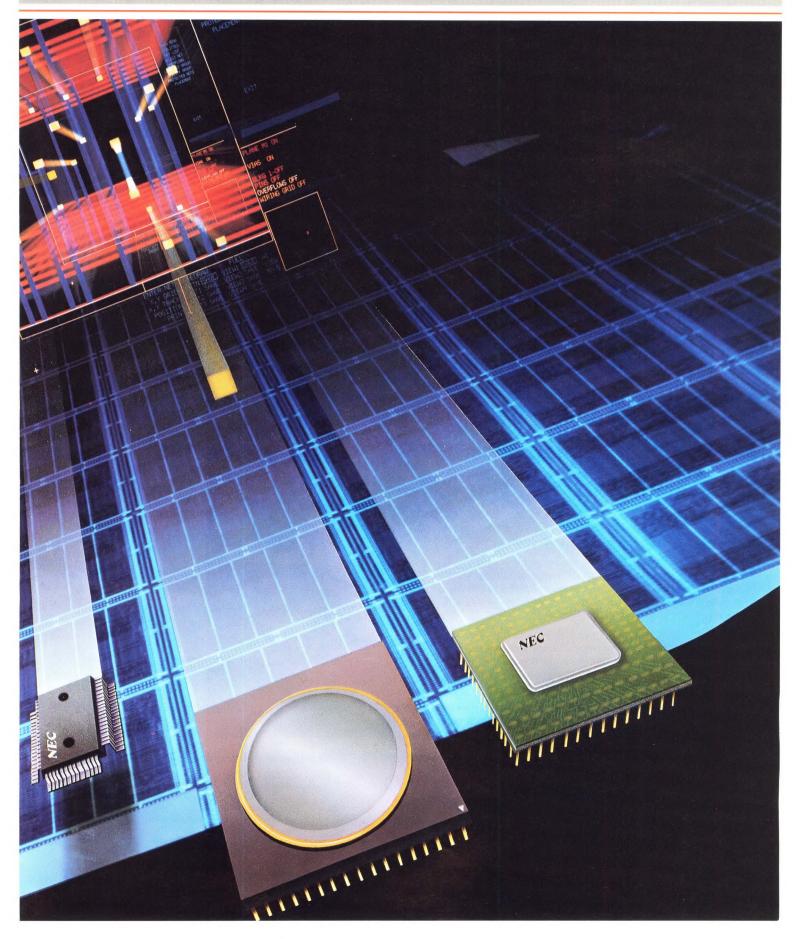
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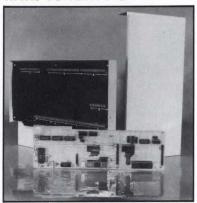


# THE COMPLETE CMOS APPROACH



### **FACTORY AUTOMATION**

# Industrial interface links to IBM PC



PCmate is an interface system for industrial data acquisition and control using an IBM PC or compatible computer. It provides 35 digital I/O lines, 4 analog input lines, 6 event counter-timers, and 2 serial I/O

ports (RS-232-C or RS-422). The system consists of a single board that is mounted on the computer's motherboard and a terminal strip chassis external to the PC.

Microcomputer Systems Inc., 1814 Ryder Dr., Baton Rouge, LA 70808; (504) 769-2154. \$995.

### **CIRCLE 350**

# Scanning system uses ultrasound

Used to nondestructively verify the integrity of bonds between semiconductor chips and packages, a scanning system produces ultrasonic images of exceptional resolution and quality. With the Hyscan system, defects as small as 1 to 2 mils can be



imaged. The system is made up of six basic components: an ultrasonic signal generator, digital gated peak detector, mechanical scanning system and immersion tank, programmable scan controller, image recorder, and oscilloscope monitor. Image printouts incorporate 16 quantized shades of gray.

Panametrics Inc., 221 Crescent St., Waltham, MA 02254; (617) 899-2719.

### CIRCLE 351



# Frequency standard upgrades your counter

Get the precision you paid for from your frequency counter. Connect the Counter-Mate to the "EXT STD" input or periodically check the internal oscillator to get traceable accuracy instead of just resolution.

The Counter-Mate frequency standard employs a precision third-overtone 10 MHz crystal in a proportionally controlled copper oven maintained at a computer optimized temperature. The excellent long-term and short-term stability is in a class with units costing much more.

Check the specifications—the Counter-Mate out-performs and is less expensive than most counters' oven oscillator options, it needs no installation, and it has sufficient drive to serve several instruments.

The Counter-Mate comes calibrated against national standards and you do not lose your counter when it is time to recalibrate! The unique 50-turn adjustor makes calibration easy and mechanically stable. Periodic calibration at Wenzel Associates is just \$15 plus shipping.

### Wenzel Associates, Inc.

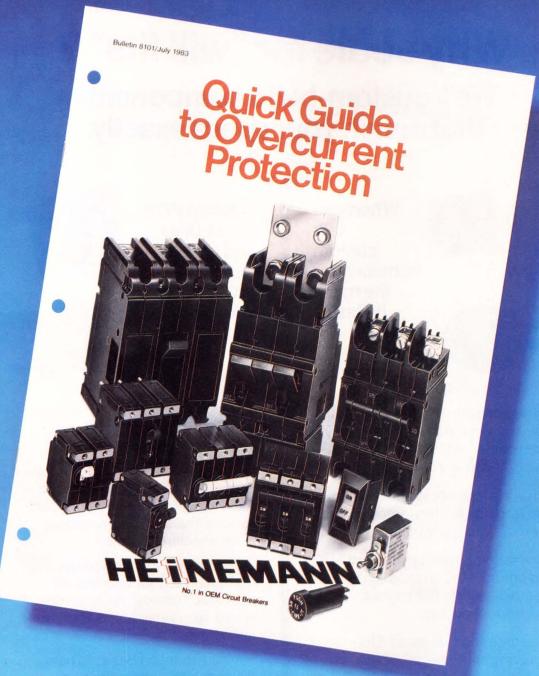
11124 Jollyville Road Austin, TX 78759 (512) 345-2703 TWX 910-997-4554





### COUNTER-MATE SPECIFICATIONS

Model										CM-
Frequency						•				1 MHz and 10 MHz
Output Drive										. TTL and 50 Ohm
Rise & Fall T	im	е								5 nsec
Aging Rate										. < 3x10 -8/Month
Temperature								<	+-	5x10 -8, 10° to 40° C
Setability .										. 2x10 -9, 50 turns
Oven Warm-	Up	)								10 minutes at 25° C
Power Requi	rm	ne	nt	S						9V Adapter included
Size										4.6" x 4.8" x 1.6"



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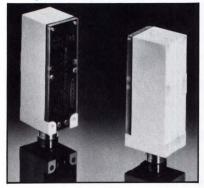
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BMP4132

**FACTORY AUTOMATION** 

# Infrared sensor responds in 1 ms



Consisting of only two self-contained units that can respond in 1 ms, the Light Screen System offers an alternative to cumbersome multiple-sensor photoelectric systems. The LS10E emitter contains a vertical row of infrared LEDs that cycle in sequence to create a modulated"curtain" of light approximately 3.5 in. high. The LS10R receiver unit contains a corresponding row of infrared light receivers. When an object passes between the two units, the receiver initiates both sinking and sourcing outputs. Since they respond only to infrared light, sensor interference from ambient light is minimized. The units detect objects as small as 1/10 of an inch in diameter and operate directly from 12 to 24 V dc.

Banner Engineering Corp., P.O. Box 9414, Minneapolis, MN 55440; (612) 544-3164. CIRCLE 352

# Robotic controller links to Apple

The VIP card is a low-cost Applecompatible robotic controller which may be used as either a stand-alone controller or in an expansion slot as an intelligent peripheral card. It employs a 65C02 CPU and provides up to 48 I/O lines, 6 counter-timers, and 24 kbytes of EPROM or static RAM. A control program may be loaded into the VIP card directly from the computer's disk drive. The card is then placed into the robot or

machine to be controlled.

Bukowski Robotics, 1555 W. University, Suite 105, Tempe, AZ 85281; (602) 966-6230. From \$129.



**FACTORY AUTOMATION** 

### Noncontact gauge measures distance



An affordable alternative to fullblown vision systems, a noncontacting gauge relies on a reflected, modulated infrared light source to measure distance to an object or surface. Typically used in automated manufacturing and quality control, the HVS 100 can operate alone or in conjunction with a host computer. The device computes the distance to an object every 21.1 ms, with a repeatability of 0.005 in. It operates over a wide range of reflective surfaces from diffuse to specular, including mirror or glossy paint surfaces.

Honeywell Visitronic, P.O. Box 5077, Englewood, CO80155; (303) 850-5050. From \$3995.

CIRCLE 359

# Optical gauges inspect objects



A series of intelligent optical inspection gauges for manufacturing applications offers a low-cost alternative to more comprehensive and expensive vision systems. The HVS 200 series is based on a linear detector array that measures the edge, position, and width of objects within the sensor's optical field of view. Presently available in six versions, the gauges are stand-alone devices that do not require additional information processing. However, they can be controlled by a computer or programmable controller.

Honeywell Visitronic, P.O. Box 5077, Englewood, CO 80155; (303) 850-5050. Prices start at less than \$2000.

CIRCLE 360

## System inspects solder joints

A machine vision system automatically inspects and monitors solder joints on pc boards with plated through-holes. The Solder Process Inspector SPI-2000 makes postwave checks of joints for insufficient solder, bridges, and holes. In less than four minutes, it inspects and marks typical soldered boards for correction, stores the information, and prints out the locations of defective joints. The collection data can then be used to adjust the solder process, resulting in fewer defective joints and less rework.

Consolidated Controls Corp., 15 Durant Ave., Bethel, CT 06801; (203) 798-3000.

CIRCLE 361

### System evaluates machine vision

The Genesis 4500 system provides an interactive environment for evaluating the feasibility of machine vision as a solution to inspection and robotic tasks. A second system, the Genesis 4600, is a more sophisticated application development environment. It provides the tools for

generating specific factory-floor applications for execution on MVI's image flow computer. Respective prices are \$42,200 (or \$47,200 with an IBM PC AT host computer) and \$65,000, including hardware, software, and support services.

Machine Vision International, 325 E. Eisenhower, Ann Arbor, MI 48104; (313) 996-8033.

CIRCLE 369

# Industrial terminal responds to voice



A voice recognition system for entering and verifying data does away with the need for keyboards and computer terminals in industrial, manufacturing, and warehouse environments. When used with a cordless microphone, the Voice Terminal 6050 Series II gives users complete mobility as well. Verification of data input is accomplished by digitally compressing voice data and replaying that data back to the user. The system has been field-proven in environments with noise levels of up to 100 dB. It has an RS-232-C serial port, and its 640-kbyte RAM holds 2000 to 3000 words at one time. A floppy-disk drive provides an additional 720 kbytes of storage.

Votan, 4487 Technology Dr., Fremont, CA 94538; (415) 490-7600. \$4950.

# "In ASIC, the customer has to be more than a job number."

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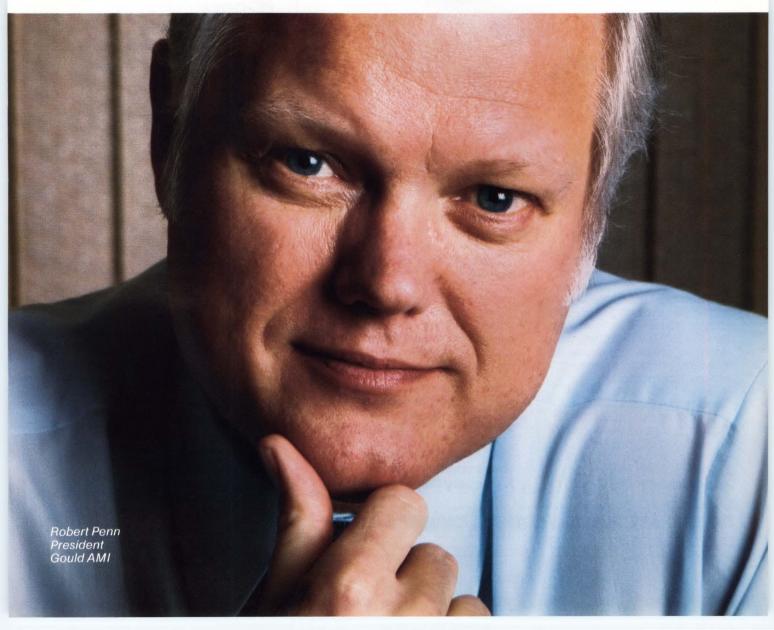
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**INSTRUMENTS** 

# Unit generates signals to 120 MHz

Offering high performance at an economical price, the VG-811 generates video clock frequencies from

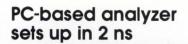
5 to 120 MHz and horizontal scan rates up to 200 kHz. The signal generator is suitable for testing, alignment, inspection, and evaluation of most current high-resolution color and monochrome video monitors.



All functions of the instrument are programmable via the IEEE-488 bus or through an RS-232-C port.

Test & Measurement Systems Inc., 349 Cobalt Way, Suite 301, Sunnyvale, CA 94086; (408) 720-8877. \$10.750.

CIRCLE 362





A 20-MHz logic analyzer has a 2-ns setup time, 10 to 15 times faster than most comparable units. Further, through an optional Doubler pod, the Logic-20 is capable of 40-MHz sampling over eight channels at double the standard 16-by-256-bit memory depth. The entire 16-channel system is incorporated into a single IBM PC expansion card and uses the computer as its controller.

Bitwise Designs Inc., 1223 Peoples Ave., Troy, NY 12180; (518) 274-0755. \$1495; Doubler pod will be available in the third quarter.
CIRCLE 363

# ROEDERSTEIN The Design



# **Power Supplies**

Roederstein Electronics recognizes that the two most critical components in any successful business are time and money. Both must be managed effectively and efficiently. That is why Roederstein is valuable to you – a single supply source with the right products at the right price – a powerful combination.

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If that were true, you'd only need one choice of application specific ICs. But an ASIC solution is more than a gate array. Or a standard cell. Or a cell-based custom circuit. These are simply different approaches to your system solution.

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**INSTRUMENTS** 

### 32-bit emulator works with $68020 \mu P$



An in-circuit emulator for Motorola's 32-bit 68020 microprocessor allows emulation at up to 12.5 MHz. The stand-alone unit provides a real-time look at all bus and control signals, as well as full width address and data, using trace modes. A wide and deep trace memory allows the capture of 2046 words of 72-bit processor cycles to reveal the actual sequence of its execution. The instrument also allows users to construct sophisticated breakpoints. Options include a RAM overlay of up to 512 kbytes and a 16-channel logic probe. Prices start at \$11,295. The cost for upgrading Applied Microsystems' ES 1800 in-circuit emulator with 68020 capabilities is \$6745.

Applied Microsystems Corp., 5020 148th Ave. N.E., Redmond, WA 98052; (206) 882-2000.

CIRCLE 354

### Signal generator covers vlf bands

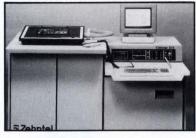


Enhancements to the 6060A programmable signal generator extend its frequency coverage to 10 kHz to cover the low frequency and very low frequency bands. The output of the 6060B extends to 1.05 GHz and has a guaranteed amplitude accuracy to within ± 1 dB from +13 to -127 dBm. Nonvolatile memory stores 50 settings for instant recall. The generator is protected against up to 50 W of reverse power. For additional stability, a reference oscillator is available with an aging rate of  $\pm 1 \times$ 10<sup>-7</sup>/month and an accuracy to within 0.1 ppm from 0° to 50°C. All functions are accessible via an IEEE-488 interface.

John Fluke Manufacturing Co, Inc., P.O. Box C9090, Everett, WA 98206; (800) 426-0361 or (206) 347-6100. \$4995; four weeks.

CIRCLE 355

# In-circuit tester checks 640 points



The latest addition to the 800 series of in-circuit testers, the Zehntel 875 can be configured with up to 640 hybrid, nonmultiplexed test points. The system provides a wide range of analog and digital test coverage, including a programmable pattern sequence generator for digital test. Up to 32 of these driver-receiver boards can be accommodated for a total of 512 LSI/VLSI test points. The 875 also features the Analog Test Board, a 16-bit instrument that allows six-wire measurement testing, transistor beta testing, parallel resistance-capacitance measurement, and mixed signal testing capability for testing hybrid devices.

Zehntel Inc., 2625 Shadelands Dr., P.O. Box 8016, Walnut Creek, CA 94596; (415) 932-6900. Less than \$85,000 (208 test points).

CIRCLE 356

### Low-cost DAS has powerful functions

Compatible with the IBM PC, a data acquisition system combines the low-cost advantage of boardlevel products with the performance capabilities of larger external systems. The System 570 provides seven preconfigured functions: 32 single-ended or 16 differential analog inputs, a programmable gain amplifier, a 12-bit a-d converter, two channels of 12-bit analog output, 16 digital inputs, 16 digital outputs, and 16 digital outputs for control of ac/dc power modules. An expansion slot is also available.

Keithley Instruments Inc., 28775 Aurora Rd., Cleveland, OH 44139; (216) 248-0400. \$1295; four weeks.

CIRCLE 357

## Waveform recorder plugs into IBM PC

A transient waveform recorder, the SDA2000, allows users to immediately begin testing by simply plugging into an IBM PC. The system offers a 200-ns sampling rate with 12-bit (0.025%) resolution and a simultaneous 300-kbyte per second DMA transfer to the IBM computer. Eight analog (dc to 3 MHz) channels are provided, as well as a 2-Mbyte sample buffer.

Soltec Corp., 11684 Pendleton St., Sun Valley, CA 91352; (800) 423-2344 or (818) 767-0044.

# "My philosophy on ASIC design? Whatever works for you."

"Some application specific IC (ASIC) houses are very rigid. You follow their rules—no questions asked. At Gould AMI, you make the rules.

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EVER WISH YOUR PC COULD OUT-PERFORM A VAX? A SUN?

Hardware Breakthrough - Ever wish your PC ran faster? Had 10 to 20 times more throughput? - Ever wish your PC had the same kind of high quality, professional software development tools (compilers, assemblers, simulators) you'd normally find in VAX, super-mini or super-micro Unix workstations?

- Ever wish you could port a scientific or commercial application to a PC without having to recode or restructure your software just to accommodate Intel's architecture?

- Ever wish you had a choice of MS-DOS or Unix V on the same system without having to commit your entire system to one or the other? Ever wish MS-DOS was a virtual demand paged operating system?...

# OASYS MS-DOS Co-Processor

... your wish has come true!

The DS-32 PC Co-Processor Board is a self-contained 32-bit computer system — it operates at super-micro speeds (10MHz and no wait states), comes with its own large memory space, full floating point support and highly optimized software tools (both native and cross). It's fully compatible with your standard PC MS-DOS system — no file conversions or retraining is needed. Installation takes just a few minutes — plug it in and go to work.

### **DS-32 Features:**

- Uses National's 32032 processor running at 10MHz. (a 32-bit processor running at super-micro speed; out-performs a mid-size VAX and most 68000 workstations. Your PC will run 10 to 20 times faster)
- Uses its own on-board memory: 1 or 2MB versions. 4 to 6MB expansion boards coming.

— Choice of Operating Systems:

- . MS-DOS Standard: You don't have to learn another OS or do any conversion.

  • VIRTUAL MS-DOS Option: the first demand paging
- version that supports files as big as your disk.

Unix System V Option.

- Fits any IBM PC, XT, AT or look-alike. (Compag, Wyse, etc.). Uses only one slot.
- Provides its own on-board floating point support.
- Based on Definicon Systems technology.
- Supports dozens of NATIVE high level, optimizing languages; C, Pascal, Fortran. Comes with Assembler, Linker, Loader and Debugger. Exciting new additions: Ada, APL, Basic, and Al tools (LISP, Prolog).
- Supports full complement of CROSS development tools to most 32-, 16-, and 8-bit target systems. Example: 68000/10/20 C, Pascal and Fortran Cross Compilers, Assemblers, Simulators, Debuggers, Profilers. 8086/186/286 C, Pascal and Fortran Compilers.

# Possible Applications:

- Run large, time consuming CPU-bound applications
  - · scientific, commercial, avionic, biomedical
  - · petrochemical, seismic
  - microprocessor simulations
  - CAD/CAM and graphic designs
  - numerical applications
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  - recursive type programs (e.g., Al tools)
  - · ...the possibilities are limitless
- Provide a low cost means of turning your PC into a high-powered software development workstation.
- Minimize porting time, effort, and support problems: eliminates having to contend with Intel 8086/88/186/286 architectural differences (e.g., 64KB addressing limits).

OASYS offers a "One-Stop Shopping" service for software developers. We support, maintain, develop, enhance, and port over 100 high quality, professional software and hardware tools running on numerous hosts (VAX, PC's, Apollo, Sun, Pyramid, etc.) and/or targeting popular 32-, 16-, and 8-bit micros and operating systems.



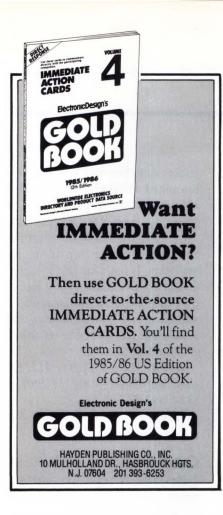
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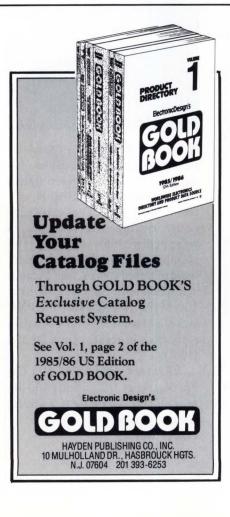
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# EAO SERIES 19 MINIATURES

# LOW LEVEL SWITCHES THAT FIT (NEARLY) ANYWHERE

At EAO, small applications are just as important as big ones. That's why we've designed and engineered the Series 19 pushbuttons and indicators: so even the smallest hole in your application can be filled with 100% EAO quality.

Series 19s are low voltage components packing all the features proven in our other dependable switching products: snap acting switch mechanisms with momentary or maintained action and gold plated contacts for over 2 million successful operations, switch ratings of 100mA/50VAC or 72VDC; contact resistance <50m $\Omega$ . bounce < 1.5ms and silver plated terminals for lamp. quick-connect terminals or wire soldering of two #20 AWG wires.

But the best part of these switches is their size: only 9mm (.354 in.) at the bezel and a maximum depth of only 33.5mm (1.320 in.). They mount in a hole only 8mm (.315 in.) round as close as 9mm on centers, and are available with round or square bezels, eight lens colors, lamp or LED illumination and optional quick-connect termination.

EAO Series 19 miniatures. You can feel (and see) the difference.





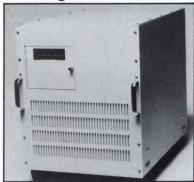


# EAO SWITCH CORP.

P.O. BOX 552, MILFORD, CT 06460 (203) 877-4577 • TELEX: EAO MFRD 964347 ELECTRO BOOTH NO. 1216-18

PACKAGING & PRODUCTION

# Rugged enclosure is refrigerated



Cooled by a closed refrigeration system, the SA-H152 industrial chassis allows the operation of computers (including fixed- and removablemedia disk drives) in harsh environments. Integrated into the enclosure is a thermostatically controlled freon-based air conditioning unit that cools and protects the internal modules against airborne contaminants. The unit comes with an eight-row quad Q-bus backplane compatible with Digital Equipment's processors and modules. A 300-W power supply and mounting for three disk drives are included.

Sigma Information Systems, 3401 E. La Palma Ave., Anaheim, CA 92806; (714) 630-6553. \$4500. CIRCLE 364

# Die attach paste imparts no stress



A conductive die attach adhesive for attaching semiconductor chips to lead frames imparts no measurable

stress to the chip. The paste can be used with standard epoxy dispensing equipment and baked at 135°C for 30 minutes. Alternatively, chips can be bonded on a standard eutectic die bonder in two seconds at 200°C without scrubbing. Bond strengths of Conductimer P-86 exceed military standards for die attach applications (MIL-STD-883C).

M&T Chemicals Inc., P.O. Box 1104, Rahway, NJ 07065; (201) 499-2152.

CIRCLE 365

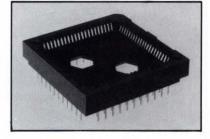
### Silver epoxy boosts conductivity tenfold

Prima-Solder ME 8410, a singlecomponent silver epoxy for hybrid applications, offers a resistivity of  $0.05 \text{ m}\Omega\text{-cm}$ , a tenfold increase in conductivity over that of conventional silver epoxies. The product is available in three viscosities for various methods of application. Curing times are 60 minutes at 150°C or 30 minutes at 175°C.

AI Technology Inc., P.O. Box 3081, Princeton, NJ 08540; (609) 799-5550.

**CIRCLE 370** 

# Socket holds leaded chip carrier



The PCC01 series of plastic leaded chip-carrier sockets is available in 68- and 84-contact versions with square or staggered grids. The

socket complies with the industrystandard JEDEC type A leaded chip carrier, and its construction allows easy access of test probes. Insulator polarization ensures proper registration of the chip during installation. It has a current rating of 1 A/pin with a contact resistance of 30 mΩ maximum. Withstanding voltage is 650 V ac (1 minute), and insulation resistance is 1000 M $\Omega$ minimum at 500 V dc.

Kel-Am Inc., P.O. Box 313, Eldon, MO 65026; (800) 233-2001 or (314) 392-7174.

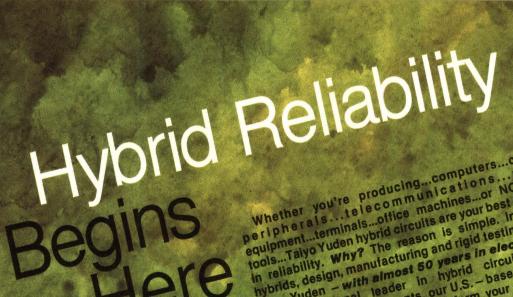
CIRCLE 372

# Cables have flat connecting sections



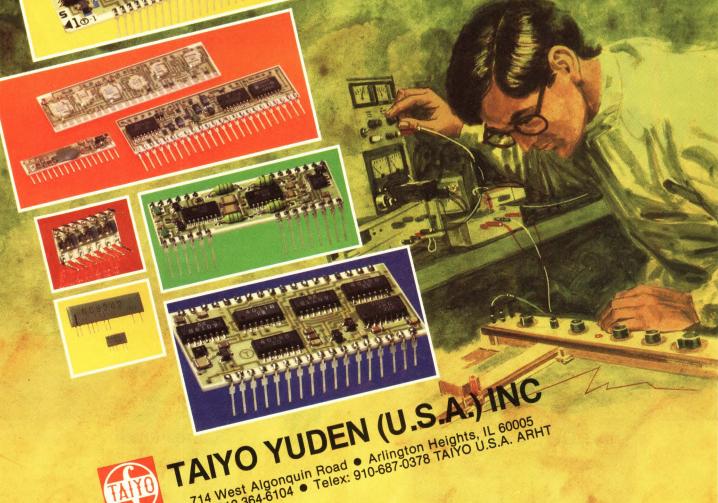
A line of FRF (flat-to-round-toflat) mass termination cables consists of 28 AWG stranded tinned copper conductors on 0.050-in. centers of 300-V PVC. The core of each cable, designated T-11302, is wrapped with an inner layer of aluminum/polyester and an outer braid of tinned copper, which results in a shield effectiveness of 70 dB at 100 MHz. A black flexible PVC jacket is extruded overall. Insulation resistance is greater than 10 M $\Omega$ (10 ft).

BRIntec Corp., Brand-Rex Cable Systems Division, 1600 W. Main St., Willimantic, CT 06226; (203) 456-8000.



Whether you're producing...computers...computer peripherals...telecommunications...medical equipment...terminals...office machines...or NC machine equipment...terminals...office machines...or NC machines equipment...terminals...office machines...or NC machines. equipment...terminals...office machines...or NC machine tools...Taiyo Yuden hybrid circuits are your best investment in reliability. Why? The reason is simple. In thick tical, in reliability, manufacturing and rigid testing is critical, hybrids, design, manufacturing and rigid testing in electronics. Taiyo Yuden — with almost 50 years in electronics— Talyo Yuden — with almost 50 years in electronics — Is the international leader in hybrid circuit assembly. — based engineering whatever your requirements, our U.S.—based engineering whatever your requirements, our U.S.—based engineering whatever your requirements, our U.S.—your hybrid design whatever your requirements, our U.S.—based engineering the latest in leading staff will work with you to transform the latest in leading into a working product incorporating the latest in leading into a working product incorporating the latest in leading into a working product incorporating the latest in leading into a working product incorporating the latest in leading into a working product incorporating the latest in leading Statt will work with you to transform your trystin leading.
Into a working product incorporating the latest in leading. into a working product incorporating the latest in leading leading to the leading world over. And like the rest of our electronic components, they're available at very competitive prices. To find out more about Taiyo Yuden hybrids, write or call today:

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Incorporating a touch activated display into your system shouldn't be an after-thought. Adding touch is the best way to make your product truly interactive, easier to use, and better suited for the real world.

It's no wonder that touch is growing in popularity. And used in a wide range of applications—from interactive video displays in stores, banks, airports, and hotels to specialized systems in hospitals, training facilities, and factories.

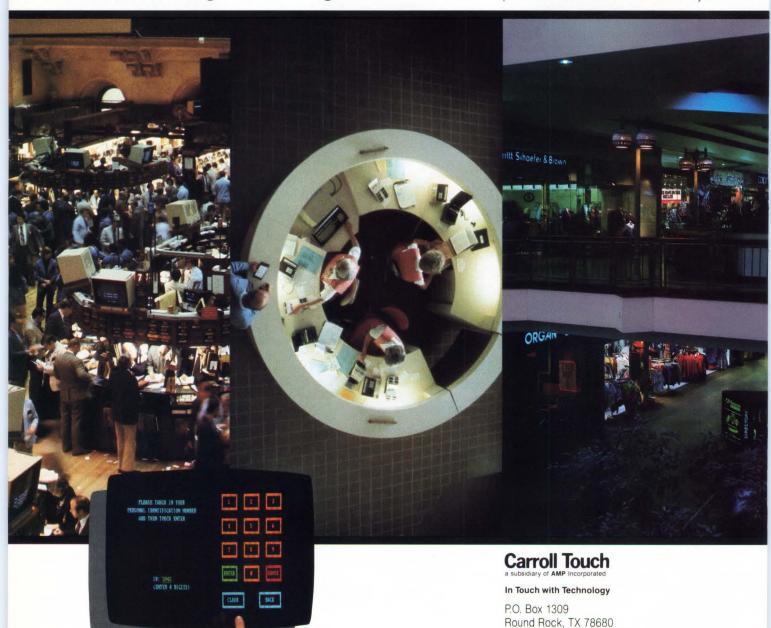
But it's important to add the right touch. That's why Carroll Touch developed the Smart-Frame™ line of low-cost scanning infrared touch systems. Featuring a powerful, built-in microcomputer, these add-in units provide exceptional functionality and reliability at the right price. Just the right touch for a great design.

Discover more about Smart-Frame products. Contact Carroll Touch today.

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# Start with the right touch. Finish with a great design.



# INTRODUCING

The ZN558 is our new 8-bit latched monolithic digital to analog converter that duplicates the performance of other 558 devices at low cost. Featuring industry standard pinout format, the applications-flexible ZN558 means a minimum of board alterations at maximum savings.

☐ Contains DAC with data latch and on-chip reference

☐ Guaranteed monotonic over the full operating temperature range

Single +5V supply

Microprocessor compatible TTL and 5V CMOS compatible

800ns settling time

Complementary to ZN447 A to D Series

ZN558E commercial temperature range 0 to +70°C

ZN558J-8 military temperature range -55 to +125°C

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CIRCLE 148

**NOW 558 8-BIT** ERFORMANCE R 30% LESS.



PACKAGING & PRODUCTION

# Motion controller sits on benchtop



A three-axis motion control system is suitable for small automatic assembly at manufacturing workstations. The benchtop Automove X-Y & Z system, which can be used with any RS-232-C computer, provides circular and linear interpolation, resolution of up to 0.00025 in., repeatability of  $\pm 0.001$  in., and position accuracy to within  $\pm 0.001$  in. Unlike conventional lead-screw positioning tables, the block-and-tackle cable design of the Automove allows it to make a 0.25-in. move from start to stop in 50 ms. Menu-driven software is available for programming the system with an IBM PC.

Asymtek, 2142-C Industrial Ct., Vista, CA 92083; (619) 727-7422. From \$3995 to \$9850.

CIRCLE 371

## Keyboard cable extends 6 ft

A retractile cable for use with computer keyboards features small coils and increased flexibility. The Belden 9693 has a 141/2-in. length of 0.710-in. diameter coils and tail lengths of 8 in. and 2 ft. Its practical



extended length is 6 ft. The cable consists of seven 26 AWG tinned copper, polypropylene-insulated conductors. These are covered with a Beldfoil aluminum/polyester shield and tinned copper spiral shield and a polyurethane jacket.

Belden Electronic Wire and Cable, P.O. Box 1980, Richmond, IN 47375: (317) 983-5200.



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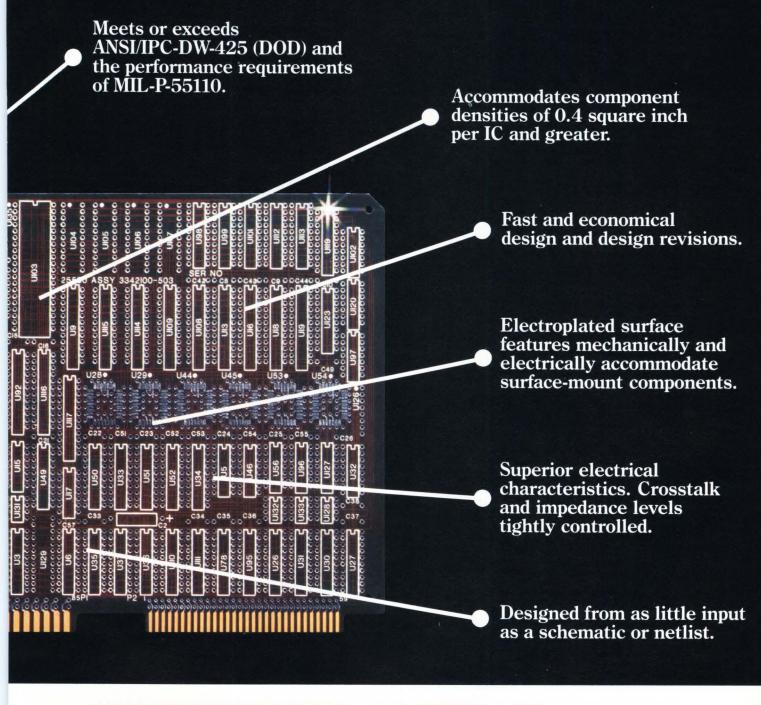
Wires cross over each other without shorting. X and Y axis routed on the same plane.

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Over the last 16 years, Multiwire Division has designed and manufactured thousands of Multiwire boards. We have produced boards for through-hole and surface-mount components, military and VHSIC/VLSI applications and used our expertise and experience to solve system and circuit design problems for high-speed logic and thermal management applications. Our sales, design and manufacturing centers located across the country are ready to prove to you the advantages of Multiwire boards from Multiwire Division. For a free copy of our brochure, just fill out and return the coupon.



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# Price: \$1599.00 Available from Stock

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- Ocomes complete with two 10:1 oscilloscope probes, two DMM probes, two "AA" batteries, rechargeable Ni-Cad battery pack and an AC adaptor plus deluxe carrying case.

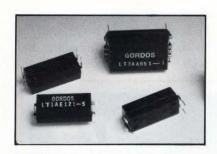
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#### **COMPONENTS**

#### Molded relays exhibit low thermal emf

Low leakage current, hence low thermal emf, over a broad range of temperature and humidity is guaranteed by the first molded relays. Gordos' LTM series is typically used to transfer the output of a thermocouple to some measuring device, without adding appreciable error due to the emf that nominally exists between the relay contacts.

Designers can specify a thermal offset of 1, 5, or  $10 \,\mu\text{V}$  (nominal at  $20^{\circ}$  C). The relays come with dry reed or mercury-wetted contacts, and are available in one- to three-pole configurations. (Only dry reed, low-voltage contacts, however, are available for the three-pole version.) The relay contacts handle up to



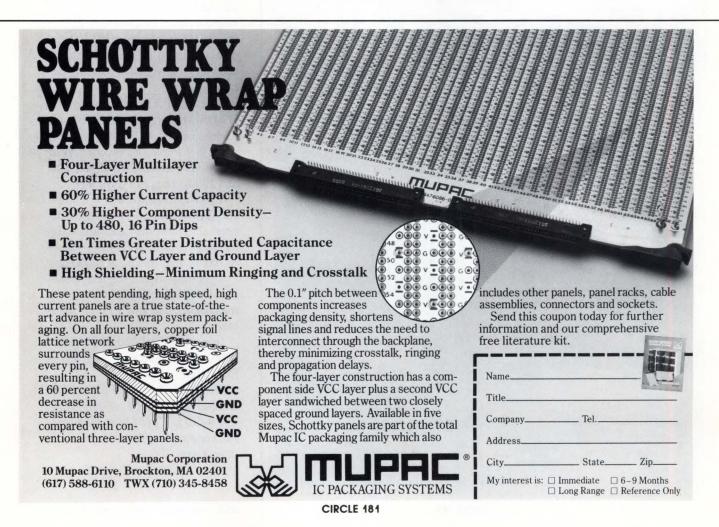
1000 V. All are switched on with a voltage of 5 or 12 V, either ac or dc. The typical lifetime of these relays is 100 million operations.

The LTM's molded body, made from a proprietary thermoset material, maintains a low leakage current, affording insulation resistance of  $10^{15} \Omega$ . The relays retain an insulation resistance of  $10^{12} \Omega$  after six

days at 40°C and a 95% relative humidity.

The relays fit into the standard 1-by-0.1-in. grid associated with printed circuit boards. Thus they directly replace potted-style relays. Further, unlike their potted counterparts, the molded relays can be wave or reflow soldered without incurring any damage. In lots of 100, the LTM-1 Form A 05 relay (single-pole, 5- $\mu$ V offset) costs \$6.90. The LTM-3 Form A 05-1 (three pole, 1- $\mu$ V offset) is priced at \$7.20. Delivery is from stock.

Gordos Corp., 250 Glenwood Ave., Bloomfield, NJ 07003; (201) 743-6800.

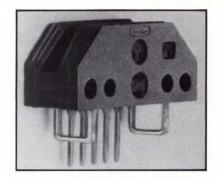


#### **COMPONENTS**

#### Tolerance sets apart shaft encoder

A highly collimated light source and a special photodetector array allows Hewlett-Packard's digital shaftencoder module to tolerate large mechanical variations in assembly and operation. Thus the need for special adjustment procedures and tools is avoided. The HEDS-9000





also gives users a high degree of freedom when selecting the shaft diameter (3/16 through 5/8 in. and 4 through 8 mm) and shaft material (metal or plastic).

The optical incremental encoder comes in a C-shaped plastic case. It translates the rotary motion of a motor shaft into a two-channel quadrature output. In operation, light is collimated by a single-lens LED and directed to an IC array of photodetectors and signal-processing circuitry.

The device works with the HEDS-5100 and 6100 series code wheels, as well as those from other manufacturers. The encoder delivers standard resolutions of 360, 500, and 1000 counts to a revolution.

The encoder's quadrature states vary by no more than 5 electrical degrees. Further, the quadrature signal is guaranteed from  $-40^{\circ}$  to  $+100^{\circ}$ C and from dc to 100 kHz.

Operating from a single 5-V supply, the device dissipates 40 mA maximum. Also, it is TTL compatible.

In quantities of 250, the HEDS-9000 costs \$20.50 each. Delivery is from stock.

Hewlett-Packard Co., 1820 Embarcadero Rd., Palo Alto, CA 94303. Call local Hewlett-Packard sales office.

# Two of our best Performers

14 day full money back guarantee



#### **HM205**

## an outstanding Oscilloscope with digital storage

This new oscilloscope offers all the features of a state-of-the-art **20 MHz** realtime instrument. In addition it provides digital storage capability for signals between **50s** and **0,3 ms** duration, with a max. sampling rate of **100 kHz**. Especially when working with comparatively slow phenomenae, the **HM205** can easily replace considerably more expensive digital storage scopes.

2 Probes x1/x10 incl. \$ 82000

#### **HM208**

### the high tech Storage Scope with 20 MHz sampling rate

The **HM208**'s high sampling rate of max. 20 MHz facilitates storing of relatively fast single shot events. Max. memory is **4096 x 8** bit, conveniently divided into two independent blocks. **XY-storage** capability enables easy viewing and recording of characteristic curves and Lissajous figures. An XY-recorder output and the optional **GPIB-Interface** allow full integration in automatic measurement systems. With more than **5000** units sold, this is one of Europe's bestselling digital storage scopes.

2 Probes x1/x10 incl. \$ 238000

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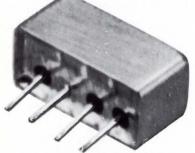
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# **frequency doublers**

+1 to  $+15\,dBm$  input



1 to 1000 MHz only \$21<sup>95</sup> (5-24)

AVAILABLE IN STOCK FOR IMMEDIATE DELIVERY

- micro-miniature, 0.5 x 0.23 in. pc board area
- flat pack or plug-in mounting
- high rejection of odd order harmonics, 40 dB
- low conversion loss, 13 dB
- · hermetically sealed
- ruggedly constructed MIL-M-28837 performance\*

\*Units are not QPL listed

#### SK-2 SPECIFICATIONS

FREQUENCY RANGE, (MHz) INPUT 1-500 OUTPUT 2-1000		
CONVERSION LOSS, dB	TYP.	MAX.
1-100 MHZ	13	15
100-300 MHz	13.5	15.5
300-500 MHz	14.0	16.5
Spurious Harmonic Output, dB 2-200 MHz F1 F3	TYP. -40 -50	MIN. -30 -40
200-600 MHz F1 F3	-25 -40	-20 -30
600-1000 MHz F1 F3	-20 -30	-15 -25

For complete specifications and performance curves refer to the 1980-1981 Microwaves Product Data Directory, the Goldbook or EEM.

finding new ways . . . setting higher standards

#### Mini-Circuits

A Division of Scientific Components Corporation World's largest manufacturer of Double Balanced Mixers 2625 E. 14th St. B'klyn, N.Y. 11235 (718) 769-0200

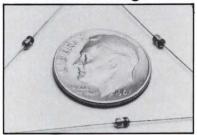
C78-3 REV. A

CIRCLE 184

#### NEW PRODUCTS

**COMPONENTS** 

#### Lamp eases troubleshooting

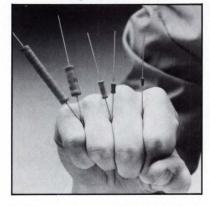


An axial-leaded specialty lamp, the MT1110-R, can be strategically placed in different areas of a circuit to simplify troubleshooting. Under normal operation, a faint light is visible from each lamp. If one of the lamps is not lit, the problem is localized to the defective area of the circuit. Luminous intensity is 0.1 mcd at 10 mA.

Marktech International Corp., 5 Northway Ln. N., Latham, NY 12110; (518) 783-1431. \$0.10 (1000 units); stock to four weeks.

**CIRCLE 373** 

#### High-power resistor is flameproof



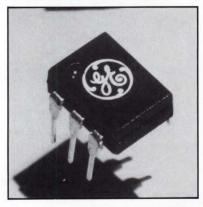
A family of metal-film resistors is intended for applications requiring high power-vs-size and/or operation at high environmental temperatures. The type CPF resistors, which are protected by a flameproof coating, are available with ratings (at

25°C) of 1, 2, 4, 7, and 10 W. They can operate, with appropriate derating, at temperatures up to 230°C. Standard resistance range, depending on size, is 5  $\Omega$  to 150 k $\Omega$ . When compared to oxide styles, the CPF devices offer a lower resistance tolerance ( $\pm 0.5\%$ ,  $\pm 1\%$ , and  $\pm 5\%$ ) and a lower temperature coefficient ( $\pm 100 \text{ ppm}/^{\circ}\text{C}$ ).

Dale Electronics Inc., 2300 Riverside Blvd., Norfolk, NE 68701; (402) 371-0080. \$0.16 (1-W, 1% version) in lots of 10,000.

**CIRCLE 374** 

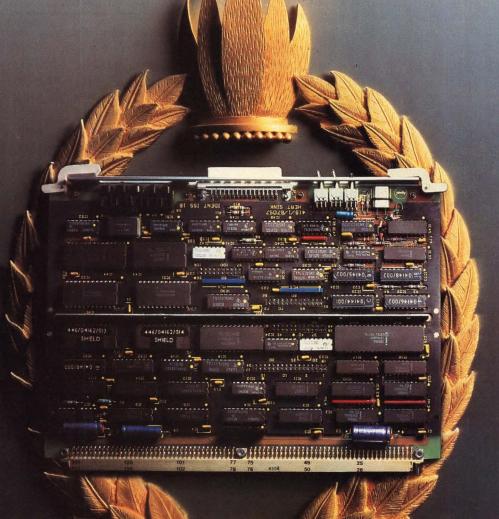
#### SCR optoisolator controls 480 V ac



An 800-V SCR optoisolator allows logic circuits to directly control up to 480-V industrial power circuits. Designated the H11M, the 6-pin DIP optoisolator can be controlled with a logic signal as low as 5 mA at 1.5 V. A 300-mA rms output rating allows two of the devices, with the output SCRs connected in antiparallel, to control more than 250 W on a 440-V ac line. It provides 4000 V rms of isolation and is capable of withstanding more than 600 V/ $\mu$ s.

General Electric Co., Semiconductor Division, 318 First St., Liverpool, NY 13088; call local sales office. \$1.89 (1000 units); stock.

# Why should military designers miss out on the best designs?



You shouldn't.
Because now, with the
Plessey PMM 86M range you
can have a range of Multibus\*
boards providing multi-processor
capability, working on a dual bus structure,
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Eurocard profiles. The range is fully compatible with Intel SBC 86/12A which provides a

natural path for system development.

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· Intel trademark

United Kingdom: Water Lane, Towcester, Northants. NN12 7JN. Telephone: (0327) 50312. Telex: 31628.
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 Germany: D-6090 Rüsselsheim, Bahnhofstraße 38. Telefon: (061 42) 680 04. Telex: 1761 4293.
 USA: One Blue Hill Plaza, Pearl River, New York 10965. Telephone: (914) 735 4661. TWX: 710 541 1512.

**MICROSYSTEMS** 

# Extra Features Earn Deltrol Its Reputation For Quality Relays. See For Yourself!



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Deltrol's patented plastic molded coils offer the best protection for tough environments — humidity, dirt, fungus. And better heat dissipation for lower heat rise, longer life.

#### DELTROL ENDS TERMINAL BREAKAGE

Why throw away a relay because of broken terminals? Deltrol eliminates this problem by molding in the terminals. Great protection at no extra cost.



#### ARMATURE STOPS MAINTAIN PERFORMANCE

Deltrol relays with armature stops stay together, even during shipping, and maintain adjusted characteristics throughout life.



#### TYPES & RATINGS FOR YOUR DESIGN

Deltrol has an excellent selection of general purpose, magnetic latching and time delay relays for light, medium and heavy duty power loads, including Appliance and Industrial rated units. Choose from many variations: open, enclosed, solder, quick-connect, printed circuit or octal plug-in termination.



#### **NEW 20-AMP POWER RELAY**

UL recognized, CSA certified, new 20-amp power relay available in base or side-mount types. Coil voltages range from 6 to 277 VAC, 6 to 125 VDC.

#### **QUALITY MEANS TRUST**

Deltrol builds relays that meet every serious designer's expectation for quality, performance and dependability. OUR REPUTATION DEPENDS ON IT.







See your local distributor or send for free engineering catalog.

# DELTROL CONTROLS



2745 So. 19th St., Milwaukee, WI 53215, Phone 414/671-6800, Telex 2-6871

CIRCLE 186

#### NEW PRODUCTS

#### **COMPONENTS**

#### 2.4-mm connectors span dc to 50 GHz

Three families of coaxial connectors incorporate a common 2.4-mm interface jointly developed by Hewlett-Packard, Amphenol, and M/A-Com Omni Spectra. By forgoing compatibility with existing connector types, a design was achieved that optimizes performance over the entire dc to 50-GHz range.

Production-grade connectors intended for use in systems, components, cabling, microstrip, and related transmission media are being manufactured by M/A-Com. Instrument-grade connectors for test and measurement equipment are the responsibility of Amphenol, while Hewlett-Packard is concentrating on the metrology grade for application on measurement standards.

Hewlett-Packard Co., 1820 Embarcadero Rd., Palo Alto, CA 94303; (707) 577-2663.

#### CIRCLE 446

Amphenol Products, 4300 Commerce Ct., Lisle, IL 60532; (312) 983-3581.

#### **CIRCLE 447**

M/A-Com Omni Spectra Inc., 21 Continental Blvd., Merrimack, NH 03054; (603) 424-4111.

CIRCLE 376

#### LED cluster emits 16,000 mcd

One of the industry's brightest LEDs, the Model B304 red LED cluster has a luminous intensity of 16,000 mcd at only 40 mA. It is directly interchangeable with T3 1/4 incandescents and has an average life of up to 20 years.

Ledtronics Inc., 4009 Pacific Coast Hwy., Torrance, CA 90505; (213) 676-7996.

CIRCLE 377

#### Strain gauges are ultrasmall

The ES series of semiconductor strain gauges is distinguished by its ultrasmall size coupled with gauge factors as high as 155. The devices are supplied in resistance ranges from 120 to 1500  $\Omega$  and in U- or bar-shaped configurations with lengths as small as 0.040 in.

Entran Devices Inc., 10 Washington Ave., Fairfield, NJ 07006; (201) 227-1002.

# Super Powers

Remote power supplies for microprocessors

Wall Units + 5VDC @ 750 ma ± 12VDC @ 80 ma (W512750/1)



MPI's remote new plug-in units let you take the power supply out of your product and put it practically anywhere. Insert it directly into a wall plug, or rest it on a table top, desk top, bench, or any flat surface.

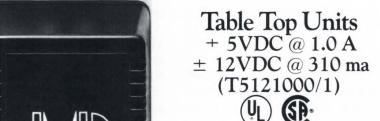
Designed for use with modems, calculators, appliances, games and a variety of other electronic products, MPI wall and table top power supplies are super-performers; providing outstanding dependability, flexibility and economy. They free up valuable board space, reduce weight and eliminate hazardous voltages, power supply heat and the need for costly cooling devices.

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- Multiple & single output
- Regulated low ripple
- UL and CSA listed
- Fully isolated outputs
- Comply with FCC EMI regs.
- · High efficiency

**CIRCLE 31** 





Input:  $120V \pm 10\% 50/60 \text{ Hz}$ 

Regulation: +5V 5% overall

Regulation: +15V or +12V 5% overall Regulation: -15V or -12V 5% overall

Ripple: 50 MV P-P

Operating Temp:  $0^{\circ}\text{C}$  to  $+40^{\circ}\text{C}$ , Storage Temp:  $-55^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ 

Operating

Altitude: 15,000'



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#### INTERNATIONAL

#### CMOS FIFOs cruise along at 25 MHz

The fastest FIFOs to date is a title that can be claimed by a series of five CMOS 64-word memories with a minimum data rate of at least 25 MHz and a maximum speed of 35 MHz. At the same time Plessey's MV66xxx family consumes roughly 200 mW at top speed, at least one half that of anything else yet available.

The MV66401, 402, 403, and 404 are 4 and 5 bits wide. The MV66030 is a 9-bit device. All of the buffers consist of sixty-four 4-, 5-, or 9-bit data registers.

Data is loaded from the data inputs by a pulse on the Shift In line. This information ripples through to the outputs, where it is sent on its way by a Shift Out pulse.

The devices can be cascaded easily-at the 25-MHz data rateto accommodate more than 64 en-



tries. To handle more than 9 bits of data, OR and AND gates must be added. Reads and writes are independent, which allows the chips to serve as asynchronous buffers. Further, all of the devices feature memory-full and memory-empty flags, which makes monitoring a system particularly simple.

The MV66401 and 403 are 4 bits wide and come in 16-pin plastic or ceramic DIPs. The MV66402 and 404 are 5 bits wide and are mounted in 18-pin packages (the latter memories have three-state outputs).

The three buffers are compatible with Monolithic Memories, Cypress, and National Semiconductor 400 devices. The MV66030 comes in a 28-pin plastic or ceramic DIP or a 28-pin leaded ceramic chip carrier. It is pin-compatible with TRW's TDC1030.

The 4- and 5-bit devices, in hundreds, cost roughly \$27. The 9-bit MV66030 is priced at just over \$38.

The ICs connect to a 5-V supply and work at  $-40^{\circ}$  to  $+85^{\circ}$ C.

Plessey Semiconductors, 3 Whatney, Irvine, CA 92718; (714) 951-5212: TWX: 701464.

#### CIRCLE 317

Plessey Semiconductors Ltd., Cheney Manor, Swindon, Wilts. SN2 2QW, England; (+44) 793 36251; Telex: 449637.

CIRCLE 318

#### $\mu$ C controls 50-MHz analog scope

The only 50-MHz analog scopes to run under microcomputer control make up Philips' 3050 family. And at \$1300, the scopes deliver features normally found in digital instruments costing at least twice as

An 8052 microcomputer brings multifunction soft keys to the scope, as well as an autoset key that calculates the amplitude, time base, and trigger setting needed to bring a signal onto the scope's 8-by-10-cm screen. In addition to the display, the instrument packs a separate 180-segment LCD. The liquidcrystal display is for menus, instrument status, and settings.

The 3050 has a sensitivity between 2 mV and 10 V/division. Its dynamic range is  $\pm 24$  divisions, and at a sensitivity of 2 mV/division, it shows a rise time better than 10 ns. The time base scale is between 1 ms and 50 ns/division. Further, the scope sports a 16-kV deflection voltage. That deflection voltage ensures good trace visibility at high writing speeds.

The PM 3050 and the rackmountable PM 3052 offer a single time base; the 3055 and the rackmountable 3057 deliver two. Circuits in the instrument communicate over Philips' I<sup>2</sup>C bus, which is brought out at the instrument's back on a 9-pin DIN plug for ease of testing. A built-in automatic checking routine exercises all of the scope's major functions.

The oscilloscope is 350 by 455 by 146 mm and weighs about 7.5 kg.

Philips Test and Measurement Department Inc., 85 McKee Dr., Mahwah, NJ 07430; (201) 529-3800.

#### CIRCLE 323

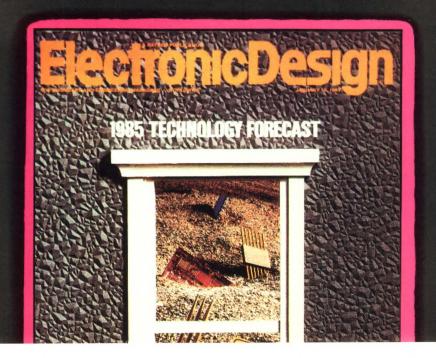
Philips I&E, PO Box 523, 5600 AM Eindhoven, The Netherlands; (+31) 40 757005; Telex: 51573.



### **BEST IN-DEPTH ANALYSIS**

The Jesse Neal Award is the "Pulitzer Prize" for journalism. This year, only 15 publications were recognized out of 730 entries. Among the world's largest magazines, Electronic Design was singled out for its 1985 Technology Forecast Report which predicted major change in the role of the design engineer.

This year's Neal Award acknowledges what loyal Electronic Design readers have known for years. Information of vital interest to electronics engineers is covered *first and best* in Electronic Design.



# The story behind IBM's new 32-bit RISC PCs.

These aren't your ordinary workstations.

For IBM RT Personal Computers—6150 and 6151—are built around a revolutionary 32-bit, virtual memory, RISC-based microprocessor. Developed and manufactured by IBM.

The significance? Far faster throughput. Because RISC (for Reduced Instruction Set Computer) architecture eliminates many of the unnecessary bells and whistles found in conventional chip design.

What's more, an IBM RT PC can directly address up to four megabytes (Mb) of real memory, over a trillion bytes of virtual memory and up to 210

Mb of DASD, or disk storage.

All of which makes IBM RT PC microprocessors particularly well suited for the total application requirements of technical professionals working in engineering, scientific, industrial and academic environments.

#### CADAM® and CIEDS¹ Software

One of the key programs available for the IBM RT PC—attached to the IBM 5080 Graphics System—is Professional CADAM. And it's compatible with established host-based CADAM.

There's also Computer-Integrated Electrical Design Series (CIEDS), which allows for the schematic

capture of integrated circuit designs.

And there is a growing list of applications available from software companies in the following fields: mechanical and electrical CAD/CAM, petroleum production, artificial intelligence, software engineering, project management and graphics.

#### UNIX<sup>2</sup> System V

The primary operating system is derived from the UNIX System V—with some very important enhancements added by IBM. These enhancements make this operating system—Advanced Interactive Executive or AIX<sup>3</sup>—much easier to use, give it improved performance and reliability, and also add a virtual storage capability.

This operating system gives you multi-user and multi-tasking operations for up to eight concurrent local or remote users working on low-cost ASCII terminals such as the IBM 3161.

There is also a full-function IBM SQL/RT relational data base management facility available.

#### **Understands Many Languages**

The IBM RT PCs are highly literate. You'll be able to write and run applications in C, Fortran 77, BASIC, PASCAL and Assembler.

And as for general-purpose applications, you'll be able to run UNIRAS<sup>4</sup> (for engineering and business graphics), RS/1<sup>5</sup> (for data analysis and graphing functions), IMSL<sup>6</sup> (a library of Fortran sub-

routines), Interleaf's Workstation Publishing Software, Solomon III<sup>8</sup> (for accounting), SAMNA+ (for spreadsheet and word processing) and Applix IA (for integrated office functions).



The IBM RT PC 6150 Model 20 Floor-standing unit

#### PC Compatible

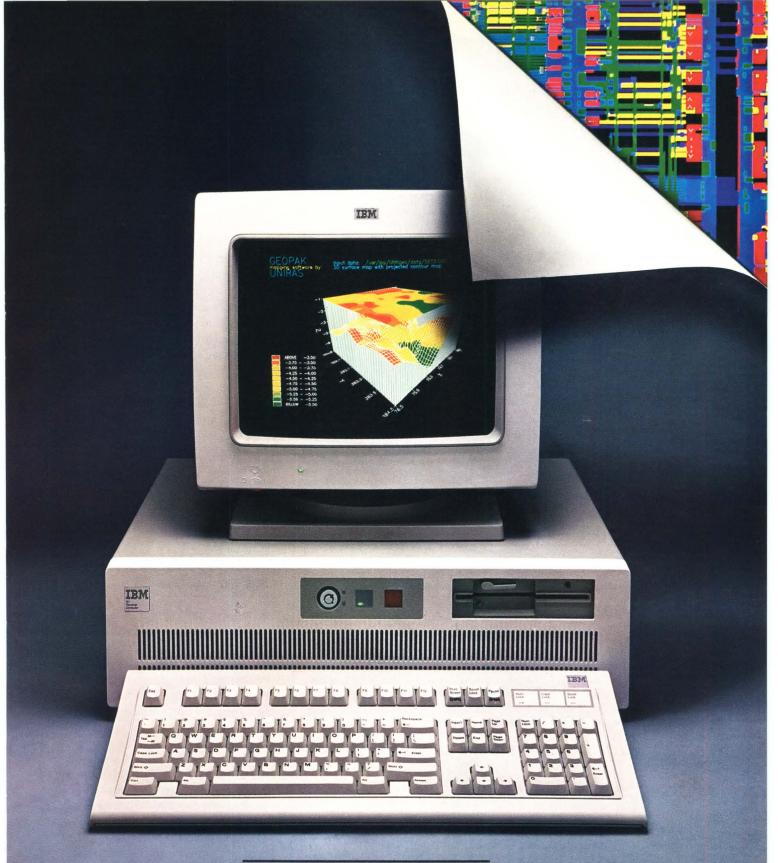
The IBM RT PCs can incorporate as an optional feature an Intel 80286 coprocessor (in effect a PC AT on-a-board) that runs concurrently with the 32-bit RISC processor. That means the RT PCs can support many existing IBM PC applications and the interchange of

their related data. It also means the RT PC I/O bus

can accept standard PC cards.

Contact your IBM marketing representative. Or call 1 800 IBM-2468, Ext. CZ/814, for participating Authorized Dealers, or for free literature. Software companies interested in writing programs for the IBM RT PC should call 1 203 783-7141.

IBM	"5-1"
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The IBM RT PC 6151 Model 10 Desk-top unit

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CIRCLE 190

#### **PRODUCT NEWS**

#### **RUN INTEL SOFTWARE ON IBM PC'S**

Transform an IBM PC, or compatible into a totally integrated Intel Micro Development Station capable of running all 8 bit ISIS-II, and 16 bit ISIS-III software. the MICRUN80, and MICRUN86 Universal Development Interfaces (UDI), will allow you to increase your development capabilities with faster, more reliable, and more affordable PC based development stations. Both (UDI)'s come complete with a communications program for transferring Intel software to your PC. Micro Interfaces Corporation, 6824 N.W. 169th St., Miami, FI 33015 (800) 637-7226 or (305) 823-8088 \$450 CIRCLE 236 each.

#### RUN CP/M-80 SOFTWARE ON IBM PC'S

New CP/M to MS-DOS interface combines hardware and software to provide PC's with the ability to execute CP/M80 software. RUN/CPM comes with an NEC V-20 microprocessor which replaces the PC's 8088 chip and provides dual 8 bit/16 bit processing ability. Software features include, terminal emulation, ability to run CP/M programs from hard disks or RAM disks, logical drive assignments, ability to run 8 bit or 16 bit programs from the same prompt, and a disk emulation feature which allows your PC's floppy disk drives to directly read, write, and format approx. 100 CP/M disks. Micro Interfaces Corporation, 6824 N.W. 169th St., Miami, FI 33015 (800) 637-7226 or (305) 823-8088 \$99.95 CIRCLE 237 ADVERTISEMENT

NEW PRODUCTS

INTERNATIONAL

#### Frequency counter resolves to 10 digits

A frequency counter offers 10-digit resolution for frequencies up to 1.3 GHz. The 1998 counter measures signals lasting ony 2 ms, with a resolution of six digits. Signals 1 second long can be measured to nine digits. The instrument has an IEEE-488 interface and can be supplied with one of a number of internal frequency standards (using ovened or other frequency references). Periods and ratios can be selected using a single key stroke.

Racal Dana Instruments Ltd., 21 Market Pl. Wokingham, Berks., RG11 1AJ, England; (+44) (734) 782158; Telex: 847936.

CIRCLE 385

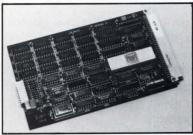
#### Prototyping system takes 21 cards

A Eurocard prototyping backplane accommodates up to 21 cards on 0.8-in. centers and enables busless backplanes to be assembled rapidly and easily. The board uses the company's Quick Connect IDC terminals for point-to-point signal wiring; each connector position on the EQC-3UBP board is tracked to a 64/96-pin pattern incorporating the Quick Connect terminals. The board can be reused without degrading the contacts. Options include 64- or 96-way three-level wire-wrapped DIN connectors, gold-plated terminals, and the number of populated connector positions.

Dage Eurosem Ltd., Rabans La., Aylesbury, Bucks. HP19 3RG, England; (+44) 296 33200/32881: Telex: 83518.

#### INTERNATIONAL

#### Card illuminates 1024 by 1024 pixels



A single-height G-64-bus Eurocard graphics controller has 1 Mbit of RAM and offers a resolution up to 1024 by 1024 pixels. Several Gesvig-2 monochrome boards may be synchronized to form a color display (three boards generate an eight-color display). The board uses an NEC-7220 graphic controller chip and can draw vectors, polygons, and circles. The board pulls 1.1 A maximum from the 5-V supply. It costs \$695.

Gespac Inc., 100 W. Hoover Ave. 11, Mesa, AZ 85202; (602) 962 5559.

#### **CIRCLE 387**

Gespac SA 3 Chemin des Aulx, CH-1228 Geneva/Plan-les-Ouates, Switzerland; (+41) 22 713400; Telex: 429989.

CIRCLE 388

E.0501 Holdover.1

#### Demo system stores speech

A demonstration and evaluation system for SGS-ATES' M8950 voice synthesizer has seven EPROM sockets for storing up to 180 seconds of speech. Standard firmware allows one of 16 words or phrases to be selected using manual switches or a parallel interface, and there is a breadboarding area for application-specific circuits or an external interface. The voice synthesizer itself has a sampling

frequency that can be programmed between 8 and 10 kHz. It uses LPC (Linear Predictive Coding), together with pitch-synchronous synthesis. A change in the synthesis filter parameter synchronizes with the pitch period to minimize distortion. The 28-pin synthesizer connects directly to a Z80 microprocessor and needs only a simple interface to work with most 8- and 16-bit devices.

SGS-ATES Componenti Eletronici SpA, Via C. Olivetti 2, 20041 Agrate Brianza, Italy, (039) 65551.

CIRCLE 389

#### System develops controller code

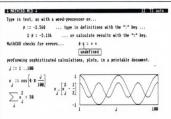
Two microcomputer development systems run on the IBM PC, XT, and AT or compatible personal computers. The A51 systems work with Intel 8031, 8032, and 8044 ROM-less controllers, as well as the 8051, 8052, 8044, and 8751 series when used in external memory mode. A similar system, the CT6301, works with Hitachi's 6301x and 6303x families (including ZTAT field-programmable types). The software development system for both series of controllers incorporates a full-screen windowing text editor, as well as an assembler and linker. The typical assembly time is 2000 lines a minute on an AT fitted with a hard disk. Files can be exchanged between the controllers and a PC using the Atrans file transfer software.

Ashling Microsystems Ltd., Enterprise House, Plassey Technological Park, Limerick, Ireland; (+353) 61 338177; Telex: 70182 INOV EI.

CIRCLE 390

### MathCAD





### A powerful computation and documentation tool for your IBM-PC.

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One Kendall Square Cambridge, Massachusetts 02139

**DIGITAL ICs** 

#### 32-bit MACs arrive in CMOS

The first 32-bit CMOS multiplier-accumulators to appear on the scene step through their paces in as little as 80 ns. LSI Logic's L64032 typically consumes just 900 mW when operating at 5 V. The only chip that will give them a run for the money is a power-hungry bipolar ECL device that Advanced Micro Device's is sampling. The CMOS multiplier-accumulators use three major buses to furnish separate 32-bit-wide X and Y inputs and a 32-bit product output. (Furthermore, a 4-bit extended product is also available.)

Versions of the L64032 are designated at six speeds. For the commercial temperature range, designers

can obtain cycle times of 125, 100, or 80 ns for single-precision operations. Over the military temperature range, the speeds drop to more conservative values: 160, 125 or 100 ns.

The device accommodates integer, two's complement integer, unsigned fractional, as well as two's complement fractional inputs and outputs. Double-precision (64-by-64-bit) fixed-point multiplication can be handled in just four pipelined or six nonpipelined cycles using the Add and Shift control inputs. Additionally, either positive or negative accumulation can be done by selecting the Add or Subtract control in-

put lines.

All input, output, and internal registers include scan testing logic to ease both chip and board-level system testing. What's more, the chips carry temporary registers that make it possible to preload the product registers.

The L64032 multiplier-accumulators are housed in 132-lead pin-grid arrays. Samples are available from stock. The 100-ns commercial version costs \$350 apiece in 100-unit quantities.

LSI Logic Corp., 1551 McCarthy Blvd., Milpitas, CA 95035; Rick Rasmussen, (408) 433-8000. CIRCLE 315

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Give us a day, and we'll save you weeks.



Everybody claims to have a CAD system that'll make your life as a printed circuit board designer easier. But talk is cheap. With Bishop's low-cost QUIK CIRCUIT PCB CAD/CAM system you can sample its time and work saving benefits before you buy. Bishop invites you to take the QUIK CIRCUIT Guided Tour. The Tour (a demonstration diskette and synchronized audio tape) takes just 35 minutes. And you can make stops along the way to put QUIK CIRCUIT through its paces, and try its easy-to-use features yourself.

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You'll be impressed with how easy it is to use QUIK CIRCUIT – no typing expertise required... no dozens of commands to memorize. You'll also be impressed with how powerful it is – multi-layer capabilities; surface mount technology (SMT); board sizes up to 32" X 32"; finished artwork, fabrication and assembly documentation at 1X, 2X and 4X.

And QUIK CIRCUIT is flexible. Create whatever pads, patterns and traces you need to complete your layout...your library of elements is unlimited! And design changes, which can be made at any time, are a snap.

# TAKE THE TOUR

You hear so much about

#### **PCB CAD SYSTEMS**

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Like the QUIK CIRCUIT software, the demonstration diskette runs on an Apple Macintosh 128K, 512K or XL personal computer, an Apple Lisa system with MacWorks, and the powerful new Macintosh Plus.

The QUIK CIRCUIT Guided Tour (Order No. 30008) is available now from your local authorized Bishop Graphics CAD Systems dealer for only \$15.00. Call Bishop Graphics CAD System Corporation TOLL-FREE at 800-222-5808 (in Alaska, Hawaii and California, call 818-991-2600) for the name of your nearest dealer.

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**DIGITAL ICs** 

#### EPROM pinouts meet system needs

Four variations of the pinout for a 1-Mbit CMOS UV EPROM give designers the flexibility to handle almost any system requirement. There will be two versions that offer a 64k-by-16-bit organization, the MBM27C1028 and the C1024, and two that offer 128k-by-8-bit formats, the MBM27C1001 and C1000. The  $\times$ 16 versions include a multiplexed address/data unit that comes in a 28-pin 600-mil DIP (the C1028) and a nonmultiplexed 40-pin option (the C1024). A 32-bit DIP houses one of the  $\times 8$  versions (the C1001), while a 28-pin package, compatible with the pinout of several 1-Mbit ROMs, will be used

for the other  $\times 8$  EPROM (the C1000).

Prices in 100-unit quantities start at \$225 apiece for the C1000 and C1001 and increase to \$255 for the C1024 and to \$265 for the C1028. Samples are available from stock.

Fujitsu Microelectronics Inc., 3320 Scott Blvd., Santa Clara, CA 95054; (408) 727-1700.

CIRCLE 391

#### DRAM driver handles 11 bits

An 11-bit—wide dynamic memory driver increases the efficiency of memory systems by accommodating wider address paths. In addition, the Am2976 allows all memory



array RAS and CAS lines to be driven by one chip, minimizing skew times between devices and optimizing system performance. With a capacity for driving up to 88 dynamic RAMs, the 11 inputs and 11 outputs of the Am2976 are ideal for driving memory devices with densities of up to 1 Mbit.

Advanced Micro Devices Inc., 901 Thompson Pl., Sunnyvale, CA 94088; (408) 982-7445. From \$4 (100 units).

CIRCLE 392



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The best CNC production drilling and routing equipment in the business coupled with top quality personnel mean PDI can build incredibly precise

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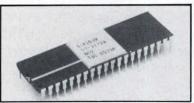


Precision Diversified Industries, Inc.

15285 Minnetonka Boulevard Minnetonka, Minnesota 55345 (612) 935-8825

**DIGITAL ICs** 

#### **NCO** provides 32-bit resolution

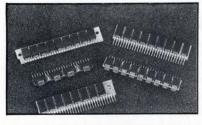


A number-controlled oscillator (NCO) generates digital sine and cosine outputs with a frequency resolution of 32 bits. The CMOS device, designated the ST-1172A, can operate with clock frequencies of up to 25 MHz. Power dissipation at 25 MHz is 330 mW. Sine and cosine outputs each have 8 bits of amplitude resolution. Packaged in a 40pin DIP, the device can be used in digital processing applications or with a d-a converter for analog frequency generation.

Stanford Telecommunications Inc., 2421 Mission College Blvd., Santa Clara, CA 95054; (408) 980-5684. \$300 (small quantities); stock.

CIRCLE 393

#### **RAM** modules meet diverse needs



A complete line of memory modules is available from Interplex Technologies, including dynamic RAM configurations of 4k, 8k, and 9k by 256 bits in both single-in-line packages and socket-insertable modules. Row access times of 100, 120, 150, and 200 ns are available, as well as page and nibble operating modes.

The devices have a 4-ms (256-cycle) refresh period and operate over a temperature range of 0° to 70°C.

Interplex Technologies Corp., 381 Park St., Hackensack, NJ 07602: (201) 343-3156.

CIRCLE 394

#### **CMOS logic ICs** replace bipolars

A family of CMOS replacements for Advanced Micro Devices' popular 29800 bipolar interface chips matches the speeds of the bipolar parts vet supplies the same output drive current with only 5% the active power. The CMOS chips derive their high speed from a 1.2-µm double-level metal process developed by Integrated Device Tech-

is 80%. Full power is provided at max operating temp., to 95°C, no derating.

nology. The CEMOS II process reduces parasitic losses so that standby (static) power consumption drops to just 5 µW or about 1/70 of the level consumed by bipolar versions of the 8-, 9-, and 10-bit-wide bus interface circuits.

First to be released are 9-bit noninverting circuits that include a bus interface register (IDT39C823), a bus interface latch (IDT-39C843), and a bus transceiver (IDT39C863). The 9-bit chips provide pin-to-pin delays ranging from 5.5 to 7.5 ns, eliminating the need for extra buffers and thus conserving board space.

Integrated Device Technology Inc., 3236 Scott Blvd., Santa Clara, CA 95054; (408) 727-6116. From \$5.90 (100 units).

A Penril COMPANY

P.O. Box 222, Commerce Park, Danbury, Conn. 06810 Phones: (203) 748-7001; In Calif. (805) 493-2244

CIRCLE 395



SEE US AT BOOTH #118 ELECTRO '86, BAYSIDE CTR. BOSTON

#### **COMPUTERS & PERIPHERALS**

#### PC hosts $\mu$ P development system

Using an IBM PC as a command control terminal, a "development laboratory" can help write and debug microcode for more than 50 mi-

croprocessors. Called the UniLab II by its developers at Orion Instruments, the hardware actually comprises four development system functions: a 48-channel logic analyzer, an in-circuit emulator, a stimulus generator, and an EPROM programmer. The UniLab II develops microcode for 8- and 16-bit processors, including those from RCA, Motorola, Intel, and Zilog.

The system's logic analyzer accepts user-specified trigger points or single-step triggers. Data is captured by UniLab's buffer memory without affecting the operation of the target system, a feature dubbed nonintrusive analysis.

For maximum accuracy, the incircuit emulator uses the actual target microprocessor. A separate UniLab Personality Pak is available for each microprocessor target, along with cabling and connectors.

The system's user interface includes an on-screen menu, with PC function-key listings. The symbolic debugger and microcode disassembler can be displayed simultaneously in different windows. A user either can enter commands directly from the PC keyboard or can develop his own macrocommands for single keystroke execution. To simplify matters, the system includes an on-line command glossary.

The price of the UniLab II depends on the size of its emulator's memory (which defines the depth of the code accepted by the in-circuit emulator). A UniLab II with 128 kbytes of emulation RAM is \$4485. A unit with 32 kbytes costs \$2995. The system requires a PC host with at least 256 kbytes of main memory. Delivery takes two weeks.

Orion Instruments Inc., 702 Marshall St., Redwood City, CA 94063; Terry Zimmerman, (415) 361-8883.



#### **COMPUTERS & PERIPHERALS**

#### Interface doubles as breakout box



The SmartCableMaker connects a host computer to a terminal, printer, modem, bar-code reader, digitizer, or any device that utilizes an RS-232-C asynchronous port. Essentially a smart breakout box, the device routes the signals on each line to the proper connection. Only three switches need be set by the user: one controls data lines two and three, one configures control lines, and a third sets the correct handshaking protocol. Fourteen LEDs indicate operating status for a graphic display of the interface. The unit comes with male and female connectors at each end.

IAM, P.O. Box 2545, Fair Oaks, CA 95628; (916) 961-8082.

CIRCLE 396

#### Unit buffers plotter data



To free the host computer during the plotting cycle, a buffer unit stores 512 kbytes (expandable to 8 Mbytes) of data and then sends it to the plotter. The Caddy buffer has two RS-232-C serial ports, each with user-selectable baud rates and

data formats. It automatically senses the end of a drawing and halts the output to the plotter, allowing multiple drawings to be buffered at a single time. The unit operates with plotters made by Calcomp, Ioline, and Houston Instruments, and it is currently being updated to support Hewlett-Packard plotters.

Dickerson Enterprises Inc., 8101 N. Milwaukee Ave., Niles, IL 60648; (312) 966-0290. \$1295 (512 kbytes of memory).

**CIRCLE 397** 

#### Subsystem emulates Tektronix 4107/4109

Metheus Corp. and Grafpoint have teamed to create Tektronix 4107 and 4109 emulation subsystems for the IBM PC and compatibles. The Omega/PC GRAF-07 and GRAF-09 subsystems combine Metheus Corp.'s Omega/PC display processor and 15- or 19-in. color monitors with a specially designed TGRAF emulation software package from Grafpoint. They provide complete Tektronix functionality at less cost, and their 1024-by-768-pixel resolution exceeds the 640-by-480-pixel resolution of the 4107 and 4109.

Metheus Corp., 5510 N.E. Elam Young Pkwy., Hillsboro, OR 97123; (503) 640-8000. \$4950 (15-in. monitor) and \$6950 (19-in. monitor).

CIRCLE 398

#### Microcomputer is PC AF-compatible

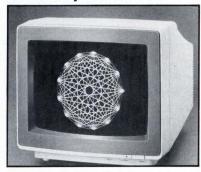
Designated the TCS-7000, an IBM PC AT-compatible computer employs an 80286 CPU and operates under MS-DOS 3.0 or higher. It has a 24-bit address bus and 16-bit data

bus. Memory comes in the form of 64 kbytes of ROM (expandable to 128 kbytes) and 512 or 640 kbytes of RAM. Battery backup and a real-time clock are also provided. Available add-on boards include a 2-Mbyte RAM card, color graphics cards (with resolutions of 640 by 200 or 640 by 480 pixels) and a serial/parallel card.

Tatung Co. of America Inc., Information and Communication Division, 2850 El Presidio St., Long Beach, CA 90810; (213) 637-2105.

CIRCLE 399

#### RGB monitor works with any controller



Because it automatically adjusts the horizontal scan rate to any frequency between 15 to 34 kHz, the ECM 1311 color monitor can be used with virtually any personal computer graphics controller. Moving easily from one application to another, the RGB monitor accepts both RS-170 and TTL inputs via BNC cable connections and a 9-pin D connector, respectively. It offers a resolution of 720 by 540 pixels on its 13-in. screen and uses a long-persistence phosphor.

Electrohome Ltd., 809 Wellington St. N., Kitchener, Ont. N2G 4J6, Canada; (519) 744-7111. \$1195.

SOFTWARE

#### Lisp meets CAD on PCs

Designers running Autodesk's AutoCad software on their IBM PCs and compatibles can now increase their efficiency by calling on the Lisp programming language. A Lisp interpreter, called AutoLisp, is embedded in the latest versions of AutoCad's Advanced Drawing Extensions, level 3 (ADE-3, an optional set of software modules for the program).

AutoLisp, a subset of Lisp, allows the user to design custom commands that can perform complex engineering functions with a minimum number of keystrokes. These commands are called in the same way as those stored on the original AutoCad disks-through keyboard entries, on-screen menu picks, or script file inputs. (A script file is a batch file that AutoCad recognizes and executes.)

Previously, creating custom menu commands was only possible by writing script files for each command on the menu. But this approach limited the versatility of the commands to tied-together strings of functions allowed by AutoCad.

Many of the functions that are important to engineers, such as the ability to perform calculations and make mathematical decisions, were very difficult to obtain by writing script files. With AutoLisp, they can be had very easily, making for powerful, engineering-specific operations.

Among their abilities, the Auto-Lisp commands can pause in the middle of an operation to prompt the user for an input from a keyboard, mouse, or tablet. Another indication of the package's power is its ability to allow commands to be constructed that read information from or write data to a disk or tape file, as well as from another system over a communications port.

AutoCad with ADE-1, -2, and -3, sells for \$2500. It is available from stock.

Autodesk Inc., 2320 Marinship Way, Sausolito, CA 94965; (415) 331-0356.

CIRCLE 309

#### C function library speeds programming

A comprehensive library of objectoriented functions and subsystems for the C programming language can cut programming time in half. Called PforCe, it offers programmers both high- and low-level functions that are fully integrated, optimized, debugged and ready to use. Subsystems for handling complex tasks include a data-base system with demand paging and B-trees to store access and index data, a windowing system, interrupt-driven communications, and background tasks. PforCe is written in C and assembly languages. Source code is included for all functions and supplied utilities.

Phoenix Computer Products Corp., 320 Norwood Pk. S., Norwood, MA 02062; (617) 762-5030. \$395.

CIRCLE 401

#### **Graphics library** runs on HP 9000

A two-dimensional graphics library provides powerful graphics functions when used with HP 9000 technical workstations and graphics hardware under the HP-UX operating system. The library is an implementation of Level 2b of the industry-standard Graphics Kernel System (GKS) and can be used in such applications as drafting, process control, mapping, simulation analysis, and presentation graphics. Applications that have already been written to the GKS standard are easily ported to the HP 9000. HP-GKS for the Series 200/300 is \$1000; for the Series 500, it costs \$3000.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Rd., Palo Alto, CA 94303; call local sales office.

CIRCLE 402

#### DOS debugger eases development

A symbolic debugger that runs on the IBM PC XT and AT, as well as selected compatibles running DOS 3.0 or higher, allows users to observe program execution at the source-code level by using highlevel procedure and variable names and labels. DOS PSCOPE provides software engineers with a symbolic test environment for program execution and includes source code display, high-level code patching, and a procedural command language. A syntaxdriven prompt line provides fully interactive operation.

Intel Corp., Literature Department W280, 3065 Bowers Ave., Santa Clara, CA 95051; (503) 681-2279. \$995; two or more debuggers can be purchased for \$795 each.

#### **OMIBYTE**

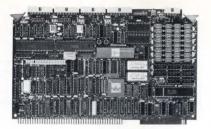
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A Look at Today . . . A Vision of Tomorrow

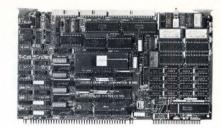


#### OB68K/MSBC1™ MULTIBUS\* SINGLE BOARD COMPUTER

- 12.5MHz 68000 16/32 bit CPU (other speeds and 68010 optional)

  • 256K/512K/1M/2M bytes dual-
- ported; zero-wait-state RAM with parity (4) RS-232C serial Synchronous/
- Asynchronous multiprotocol I/O ports
- (1) iSBX\* expansion connector (4) 28 pin ROM sockets (up to 256KB)
- Optional memory management
- Omnibyte two year limited warranty
  - \*Multibus and iSBX are trademarks of Intel Corp.

CIRCLE 213



#### OB68K1A™ MULTIBUS SINGLE BOARD COMPUTER

- 10MHz 68000 16/32 CPU32K/128K/512K bytes zero-wait-state dual-ported RAM
- Up to 192K bytes of EPROM(2) RS-232C serial ports

- (2) 16-bit parallel ports
  A triple 16-bit timer/counter
- (7) prioritized-vectored interrupts
- Omnibyte two year limited warranty

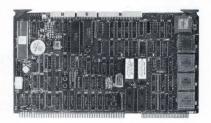
CIRCLE 214



#### OB68K/VME1™ SINGLE BOARD COMPUTER ON THE VME BUS

- 12.5MHz 68000 16/32 bit CPU
- (8) pairs of 28-pin sockets for RAM and ROM (up to 448K RAM or 896K ROM)
   (2) RS-232C serial ports using (1)
- 68681 DUART
- (2) 8-bit parallel I/O ports using (1) 68230 PI/T
- System controller functions are supported
- (7) Prioritized bus or auto vectored prioritized interrupts
- Omnibyte two year limited warranty

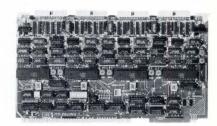
CIRCLE 215



#### OB68K/MMU™ MULTIBUS CPU BOARD WITH OPTIONAL MEMORY MANAGEMENT

- 10MHz 68010 16/32 bit CPUUp to (4) 68451 Memory Management Units (optional)
- High speed iLBX\* memory port
  8 channel DMA port
- (2) RS-232C serial ports
  4K/16K bytes of RAM
- (2) 28-pin ROM sockets
- Omnibyte two year limited warranty \*iLBX is a trademark of Intel Corp.

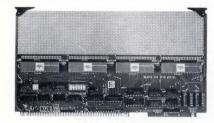
CIRCLE 216



#### OB68K/OCTAL™ MULTIBUS SERIAL I/O BOARD

- (8) RS-232C or RS-422 serial I/O ports
- Individually programmable baud rates between 50 and 38.4K baud
   (4) 68681 DUART chips
- (4) Multi-function programmable 16-bit counter/timers
- Omnibyte two year limited warranty

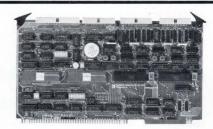
CIRCLE 217



#### OB68K23O™ MULTIBUS 96-BIT PARALLEL I/O TIMER BOARD

- 96 bits of software definable parallel I/O
- (4) 68230 PI/T chips
- (4) 24 bit timers
- 35 sq. in. of prototyping area
- Omnibyte two year limited warranty

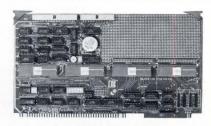
CIRCLE 218



#### OB68K/INT(S)™ MULTIBUS HOST ADAPTER/ SERIAL I/O BOARD

- 68230 PI/T chips
- (2) 68681 DUART chips
  (4) RS-232C or RS-422 serial I/O ports
- SASI interface to disk controller
- Parallel printer port
- · Real time calendar clock with battery
- Omnibyte two year limited warranty

CIRCLE 219



#### OB68K/INT(P)™ MULTIBUS HOST ADAPTER/ PARALLEL I/O BOARD

- 48 bits of software definable parallel I/O
- Real time calendar clock w/battery back-up
- (4) 68230 PI/T chips 15 sq. in. of prototyping area
- Parallel printer port
- SASI\* interface to disk controller
- Omnibyte two year limited warranty

\*SASI is a trademark of Shugart Associates.

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#### PRODUCT NEWS

#### **Emulation software mimics IBM 3270**

IBM 3270 terminal emulation is now an option for the DesignSet (DS) 1080 graphics workstation—one of the few workstations compatible with IBM's 5080 high-end graphics station. The DS1080 and its 3270 emulation software are products of **Spectragraphics Corp.** (San Diego, CA). The 3270 emulation appears as either a user-placed window on the DS 1080 or as a full screen. In the latter case, a single keystroke will toggle the display from 3270 alphanumerics to high-resolution graphics and back again. The \$900 option allows the DS 1080 to act like any member of the 3270 family, including the 3277, 3278, 3279, and 3290. Further, the software makes possible multiple screen partitions and extended highlighting. CIRCLE 409

#### Digital signal processor bows in CMOS

A CMOS version of the DSP32010 digital signal processor is now available from **General Instrument Corp.'s Microelectronics Division (Chandler, AZ)**. The new DSP320C10 is pin-compatible with and functionally equivalent to its predecessor, as well as the TMS32010 from Texas Instruments. It will initially support applications requiring a 20.5-MHz clock frequency. Users may expect a 60% or greater reduction in power dissipation over the current NMOS device. In lots of 100 units, the processor costs \$64. **CIRCLE 410** 

#### ASIC design tools run on VAXstation

In its continuing support of Unix-based engineering workstations, Via Systems Inc. (North Billerica, MA) has ported its BuildingBlocks ASIC design tools to the VAXstation II/GPX workstation. Recently introduced on Sun Microsystems' hardware, BuildingBlocks provides application-specific integrated circuit placement and routing software, integrated with Via's schematic entry, interactive physical layout, and other software modules. CIRCLE 411

#### Kit evaluates logic cell array

An evaluation kit from Xilinx Inc. (San Jose, CA) allows digital systems designers to evaluate a design application incorporating the company's logic cell array (LCA). The EK-01 kit comes with a macro library for entering designs using familiar building blocks, such as common TTL functions. It also provides a timing calculator that enables the designer to quickly look at worst-case timing for a given design. The software, which runs on the IBM family of personal computers and lookalikes, sells for \$250.

#### PRODUCT NEWS

#### 8-bit serial mode speeds RAM access

Although many 256-kbit dynamic RAMs include a 4-bit serial access mode, designers at Sharp Corp. (Tenri City, Japan) decided to distinguish one version of their RAM by letting it deliver twice the number of bits in its serial access mode. Thus, after the first access, which will initially require 150 or 120 ns, the successive bits can be transferred at just 35 or 30 ns, respectively. Therefore, the total transfer time for 8 bits can be shortened by about 100 ns vs the dynamic RAMs with 4-bit transfers. Engineering samples of the NMOS chip are now available in Japan and will soon be on hand in the company's Paramus, NJ, office.

**CIRCLE 413** 

#### PC AT chip set operates at 10 MHz

The PC AT ChipSet, introduced by Chips and Technologies Inc. (Milpitas, CA) last October, now provides full 10-MHz system operation. The fivecomponent set consists of two CMOS and three bipolar VLSI circuits, which replace 63 of the 94 components on the IBM PC AT motherboard and thus reduce AT-compatible system designs to a 36-component implementation, plus memory. Using the same design and pin-out as its 8-MHz predecessor, the 10-MHz set is priced at \$75.50 (100 units). **CIRCLE 414** 

#### Design software runs on Apollo hardware

Mentor Graphics Corp. (Beaverton, OR) is making available its entire line of design automation software on the Domain Series 3000 platform, a true 32-bit CPU and bus system. When configured with Mentor's Idea series software, the two combine to form a full-function CAE workstation with prices ranging from \$19,900 to \$31,900—slightly above the price of current 16-bit PC-based systems. Users will also have the option of installing a PC-DOS card, which will tie the IBM PC operating system to the CAE industry-standard Aegis and Unix operating systems. CIRCLE 415

#### Logic supply voltage guaranteed to 10%

Fairchild Semiconductor Corp. (South Portland, ME) is now offering its FAST (Fairchild Advanced Schottky TTL) line of standard logic circuits with the supply voltage guaranteed at 5 V  $\pm$  10%. The industry standard for other TTL technologies is just  $\pm$  5%. In addition to enhanced flexibility, the 10% tolerance also allows designs to tolerate a larger voltage droop caused by multiple device switching. There is no change to existing ac specifications as listed in the Fairchild FAST data book, and there is no increase in price for the improvement in performance.

CIRCLE 416

# ELECTRON

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#### APPLICATION NOTES

#### Signal processing newsletter



The latest issue of Analog Dialogue, a technical journal on circuits, systems, and software for realworld signal processing, describes the AD538—the industry's first monolithic analog computational unit with a transfer function of V<sub>o</sub> =  $Y(Z/X)^{M}$ . Applications illustrate how the chip performs division and multiplication and how powers, roots, logs, and antilogs are computed.

Analog Devices Inc., Literature Ctr., 70 Shawmut Rd., Canton, MA 02021; (617) 329-4700.

CIRCLE 417

#### Optical-fiber newsletter

The latest issue of Guidelines, Corning Glass Works' quarterly opticalfiber news magazine, focuses on the growth and movement of opticalfiber markets. Issues discuss industry trends, recent fiber installations and case histories, application engineering, Corning business activities, and Corguide optical-fiber products. Sections include fiber test and measurement, new products from fiber-optic component manufacturers, and literature available upon request.

Corning Glass Works, Telecommunications Products Division, MP-BH-5-1, Corning, NY 14831; (607) 974-9000.

CIRCLE 418

#### Half-bridge motor driver

A 12-page note describes the use of a GESmart power module as a versatile system building block to simplify motor drive design. By replacing the numerous discrete components previously required to interface digital control logic with output power switches, the GESmart half-bridge driver provides dramatic size reduction and enhanced reliability.

General Electric Co., Semiconductor Division, Electronics Pk., Bldg. 7, MD49, Syracuse, NY 13221; (315) 456-3269.

CIRCLE 419

#### **Photosensor** application



A photosensor application manual contains more than 65 examples of manufacturing, assembly, material handling, and quality control processes that are enhanced by the addition of photosensors. To assist in system design and factory integration, details include photosensor setup, model numbers, and recommended amplifier/power units.

Pulnix America Inc., 770-A Lucerne Dr., Sunnyvale, CA 94086; (408) 733-1560.

CIRCLE 420

#### Interfacing the AD7549 DAC

A three-page bulletin describes how to interface the AD7549—the industry's first dual 12-bit digital-toanalog converter-with the MCS-48 and MCS-51 microcomputer families. The note uses timing diagrams, program listings, and diagrams of interface circuits for each microcomputer to examine the use of the AD7549 in applications such as audio systems and control sys-

Analog Devices Inc., Literature Ctr., 70 Shawmut Rd., Canton, MA 02021; (617) 329-4700.

CIRCLE 421

#### **Temperature** transducer

A four-page note is dedicated to minimizing the influence of noise in remote temperature measurement circuits. It outlines how to build a remote temperature-to-current transducer with a range of -55° to +100°C and an output voltage of 100 mV/°C using Analog Devices' AD590 linear current-output temperature transducer. In-depth discussions include types of noise, initial noise effects, elements of noise, shielding to eliminate electrostatic noise, and rf noise.

Analog Devices Inc., Literature Ctr., 70 Shawmut Rd., Canton, MA 02021; (617) 329-4700.

#### APPLICATION NOTES

#### Microwave circuit design



Microwave Spice, a CAE tool for nonlinear circuit analysis, is featured in the latest issue of *EEsof's Fables*, a six-page newsletter from EEsof Inc. The publication details the program's special extensions for microwave applications and how it may be integrated with other EEsof tools. Also featured in the issue are interviews with the designers of the company's new line of microwave filter programs. Other topics include EEsof's customer support program and various stories on personnel and upcoming events.

EEsof Inc., 31194 La Baya Dr., Westlake Village, CA 91362; (818) 991-7530.

CIRCLE 423

#### Lock-in amplifier noise measurement

Preferred methods for lock-in amplifier noise measurement using digital integration are discussed in an eight-page bulletin (IAN 38). Described within are methods for measuring signals, noise, and signal-tonoise density ratios from 90 dB to below -20 dB. By using these

methods, the user can determine the level of confidence in the reproducibility of a signal measurement. Detailed techniques also permit the noise value to be used to determine the operating limits of a detector or system.

Ithaco Inc., 735 W. Clinton St., P.O. Box 6437, Ithaca, NY 14851; (607) 272-7640.

CIRCLE 424

#### Industrial local network

Described in a four-page pamphlet are those features of the MIL-STD-1553 data bus that can be readily applied to an industrial local network. The document gives details on how the readily available data bus interface components have achieved the desired result of flexible system integration with easier modification, growth, and testability. It is these features that make it attractive to adapt the components developed for the MIL-STD-1553 data bus to commercial-type local area networks.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, NY 11716; (516) 567-5600.

CIRCLE 425

#### High-precision calibrator

Typical applications for Honey-well's HCAL24010 high-precision calibrator are described in an eight-page note. These include a voltage source for calibrating channel gain, a programmable voltage generator, an offset voltage control to the output of an instrumentation amplifier, and a precision feedback source for a programmable gain amplifier.

Formulas and circuit diagrams illustrate these and other applications.

Honeywell Inc., Signal Processing Technologies, Marketing Communications Department, 1150 E. Cheyenne Mountain Blvd., Colorado Springs, CO 80906; (303) 577-1000.

CIRCLE 426

#### HRAM circuit design

Designing a memory subsystem that achieves a 100-MHz read data rate is the focus of a four-page illustrated report. It describes the hierarchical RAM (HRAM) that allows this continuous data rate to be achieved and presents a circuit design for easy implementation of the high-performance memory.

Visic Inc., 1120 Ringwood Ct., San Jose, CA 95131; (408) 945-9991.

CIRCLE 427

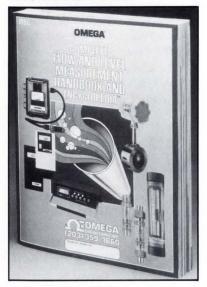
#### A-d converter testing

The cross-plot generator is a simple approach to analog-to-digital converter evaluation. The system uses basic test equipment, simple logic and timing, and is compatible with converters of any resolution. The test method described in PMI's application note (AN-101) yields four types of data: missing code identification, dynamic response, converter code width, and system noise. Included are a cross-plot matrix, diagrams, and schematic.

Precision Monolithics Inc., Literature Department, 1500 Space Park Dr., P.O. Box 58020, Santa Clara, CA 95052; (408) 727-9222. CIRCLE 428

#### APPLICATION NOTES

#### Flow and level measurement



The 1986 Flow and Level Measurement Handbook and Encyclopedia provides more than 250 pages offering a wide variety of products to meet all flow application requirements. An overview on flow measurement is provided with aids on selecting a complete flow measurement system, as well as unit conversion tables and a glossary of terms.

Omega Engineering Inc., 1 Omega Dr., P.O. Box 4047, Stamford, CT 06907; (203) 359-1660. CIRCLE 429

#### **IGT** power transistors

Motor control applications for General Electric's second-generation insulated gate transistors (IGTs) are discussed in an 11-page note. The operation and characteristics of the IGT power transistor are reviewed, and their advantages over conventional bipolar Darlingtons for PWM motor drive applications are discussed.

General Electric Co., Semiconductor Division, Electronics Pk., Bldg. 7, MD49, Syracuse, NY 13221; (315) 456-3269.

CIRCLE 430

#### Shaft-angle measurement



The two principal types of shaftangle digitizers—the resolver and the optical encoder—are evaluated and contrasted in an informative sixpage paper. The publication discusses the need for more accurate gimbal-angle measurement to achieve the desired overall system performance.

Itek Measurement Systems, 27 Christina St., Newton, MA 02161; (617) 969-7300.

CIRCLE 431

#### **Programmable** logic devices

Monolithic Memories' four-page brochure describes programmable logic devices now available for volume production designs. The document includes specification guidelines, sample flowchart, checklist, and nationwide locations of the manufacturer's representatives.

Monolithic Memories Inc.. 2175 Mission College Blvd., Santa Clara, CA 95054; (408) 970-9700. CIRCLE 432

#### **Toroidal power** transformers

A four-page guide describes the advantages of the toroidal design approach over the conventional laminated design of power transformers. The brochure discusses the size and weight advantages of toroids, as well as their higher efficiency.

Bicron Electronics Co., 100 Barlow St., Canaan, CT 06018; (203) 824-5125.

**CIRCLE 433** 

#### Microcomputer data acquisition

Interactive Microware's latest newsletter features application notes concerning Apple II and IBM PC data acquisition and data analysis.

Interactive Microware Inc., P.O. Box 139, State College, PA 16804; (814) 238-8294.

CIRCLE 434

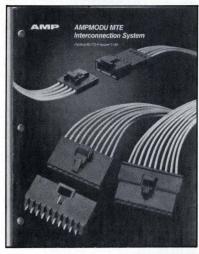
#### Fiber-optic instrumentation

A catalog features 112 pages of fiber-optic test equipment, as well as an overview of testing techniques. Detailed descriptions are provided for power meters, attenuators, OTDRs, and laser/LED sources.

Photodyne Inc., 1175 Tourmaline Dr., Newbury Park, CA 91320; (818) 889-8770 or (805) 499-3636.

#### NEW LITERATURE

#### Mass-terminated connectors



The latest additions to Amp's massterminated connector families are featured in a 32-page catalog. Included are alternatives in wire-toboard and wire-to-wire connections in 0.025-in. square post technology on 0.100-in. centers. Catalog 85-773 also highlights the AMPMODU MTE interconnection system. Electrical and mechanical specifications are provided for approximately 300 different connector types. Also included are descriptions of a complete range of application equipment and hand tools.

Amp Inc., P.O. Box 3608, Harrisburg, PA 17105; (717) 564-0100.

**CIRCLE 436** 

#### LED indicators

Modular, slide-in array LED indicators, as well as low-current miniature LEDs, are among the eleven new product groups in the latest LED optoelectronic product catalog from Leecraft. The 24-page publication details key specifications and characteristics for a wide range of pc

board and panel-mounted indicators used in a variety of industrial and commercial applications. Product categories representing hundreds of individual items include elevated printed circuit board indicators, red/green bicolor indicators, and rectangular LEDs.

Leecraft Manufacturing Co. Inc., 21-02 44th Rd., Long Island City, NY 11101; (718) 392-8800. CIRCLE 437

#### Data communication devices, equipment



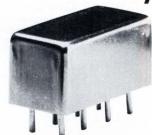
The latest edition of the *Black Box Catalog* is an excellent source book for anyone seeking solutions to data communications problems. This updated edition features 176 pages detailing over 600 unique and hard-to-find data communications and computer devices. Products range from interface connector kits and parallel printer switches to the latest in networking and hardware test sets. A technical reference section and a glossary of terms are also included. A technical support staff is on hand to answer questions.

Black Box Corp., P.O. Box 12800, Pittsburgh, PA 15241; (412)746-5500.

**CIRCLE 438** 

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ISOLATION, dB AMPLITUDE UNBAL. PHASE UNBAL.	25dB 0.2dB 2°	TYP. TYP. TYP.
IMPEDANCE	50 ohr	ns.

For complete specifications and performance curves refer to the Microwaves Product Data Director, the Goldbook, EEM, or Mini-Circuits catalog

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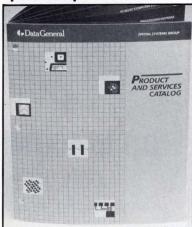
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C 73-3 REV. B

#### NEW LITERATURE

#### **Data General** special products



A 26-page catalog features 43 Special Systems' products designed to help users of Data General computers complete their system configurations. Descriptions and illustrations of processors, peripheral devices, switches, terminals and displays, and communication products are provided.

Data General Corp., Special Systems Group, MS 6-1, Rt. 9, Southboro, MA 01772; (617) 480-7150.

CIRCLE 439

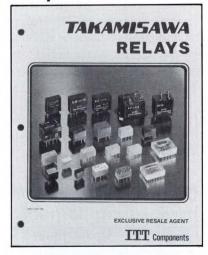
#### CAD/CAM software directory

The International CAD/CAM Software Directory provides detailed technical descriptions of manufacturing and engineering graphic software packages, indexed both by application and by company/product name. Each listing includes hardware and software requirements, list price, and availability of updates and source code.

Technical Database Corp., P.O. Box 720, Conroe, TX 77305; (713) 439-1687, \$35.

**CIRCLE 440** 

#### Electromechanical relays



A 52-page catalog details ITT Components' electromechanical relays, including subminiature and miniature pc board, general-purpose, and power types. Contact, coil, and general data specifications are given for relays used in appliance, computer, industrial control, security, and telecommunication applications.

ITT Components, 1201 E. McFadden Ave., Santa Ana, CA 92705: (714) 836-0351.

CIRCLE 441

#### Advanced CMOS integrated circuits

A 20-page directory describes a family of advanced CMOS integrated circuits. It provides detailed descriptions and technical data for GTE's full line of ADV-CMOS products, including microprocessors, microcomputers, communication ICs, gate arrays, logic devices, peripheral control circuits, and memory products.

GTE Microcircuits, Marketing Services, 2000 W. 14th St., Tempe, AZ 85281; (602) 921-6505.

CIRCLE 442

#### Pocket guide to connectors

A pocket reference enables connector specifiers to quickly determine which Lemo connector meets their needs. The guide's tables are organized around the main elements needed to specify connectors: number of contacts, working voltage, amps, and collet range.

Lemo USA Inc., P.O. Box 11488, Santa Rosa, CA 95406; (707) 578-8811.

CIRCLE 443

#### Injection-molded components

Design guidelines, engineering resin comparisons, and custom injectionmolding capabilities are discussed in a 14-page brochure to help the OEM engineer design quality, costefficient plastic components.

Security Plastics Inc., 14427 N.W. 60th Ave., P.O. Box 4723, Miami Lakes, FL 33014; (305) 823-5440.

**CIRCLE 444** 

#### Tools and test equipment

Over 1000 manufacturers are represented in a 96-page catalog of tools and test equipment for the electronics, computer, telecommunications, and field service industries. The publication illustrates tools used for electronic rework and repair, soldering and desoldering, equipment testing, and telecommunication

W.S. Jenks & Son, 2024 W. Virginia Ave. N.E., Washington, DC 20002; (202) 529-6020.

#### PROFESSIONAL NOTEBOOK

**CAROLE PATTON** 



# Free-market practices hit the skids in military bids

Despite "competition advocates" urging small companies to bid on military contracts, the free market—at least in the procurement world—is crumbling. The reason is simple: Prime contractors are levying heavy-duty complaints that the little guys threaten their profits.

In 1983 Congress became disenchanted with the Pentagon's use of sole sources—single suppliers for each piece of equipment—after \$640 toilet seats, \$400 lug wrenches, and other purchases hit the headlines. A Government Accounting Office study followed, indicating that competitive bidding could save 52% compared with single-source procurement.

The study sealed the fate of sole sources. Legislation was passed mandating open bidding, and thousands of competition advocates were hired to pull small companies into the fray.

But preaching a free market is easier than practicing it. Consider a recent report in the Wall Street Journal (March 6, 1986, p. 1). When one competition advocate recommended awarding a contract for F-100 jet-engine parts to a small company, procurement people at Kelly Air Force Base in San Antonio, Tex., put the company's parts samples through what a Department of Defense inspector calls "unnecessary" tests. Later, when the advocate recommended awarding the contract to the small company, he was overruled; instead it went to the F-100's prime contractor, Pratt & Whitney.

A similar scenario arose when Goodyear, Goodrich, and Bendix all complained that small companies were eating into their spare parts profits. The Air Force ignored a study of its own, which warned against buying the parts from the prime contractors, and essentially renounced the competition policy. Now, the three prime contractors have exclusive rights to manufacture all parts for five years.

#### Sole sources, beware: You're not the only game in town

According to my mechanic Dennis, competitive bidding is a great idea. In fact, Dennis said he could use the same approach to save me some money. When my car's oil pressure gauge needed a new bulb, Dennis got six bids on it—with some help from his brother-in-law, Archie.

Archie is a procurement officer for the government, and occasionally he lends his expertise to acquiring spare parts for Dennis. Last week, Archie flew up from Washington to hand-deliver the low bid on my bulb—\$11. Unfortunately, the manufacturer—Midnight Auto Parts—says its production line will only be up and running within two years.

Could I get a bulb sooner elsewhere? I asked Archie. "Well, I could get one today, but the contractor is a sole source. Sole sourcing," he emphasized, "is dead."

Since Archie was in town, he suggested stopping by my house for lunch so he could explain how government procurement works these days. Right now, he was looking around for bidders on a \$2 billion computer contract. "In the old days, this contract would have gone to Bigfoot Computers. Now I can guarantee we'll get at least 10 other bids, and every bid will be less than what Bigfoot would have charged."

Archie rang my doorbell around noon, armed with a stack of official-looking documents, and toured the place taking extensive notes. "Nice spot for IC fabrication," he said in the laundry room. "Plumbing's already in."

He pulled out a tape and began measuring the room. "It's six by six," I volunteered, "but if you make ICs here, I'll have to move the washer and dryer. Where will I wash the kids' dirty sneakers? And what's more, I don't want to make computers," I told Archie.

"You don't have to," he said.
"Just lighten up and play the game.
Do commodity brokers wind up with soybeans in their front yard?"

His strategy was simple. "if you win, just refuse to test your computers on the grounds that government specifications are too strict. That way, procurement will cancel the contract and award it to the prime contractor, Bigfoot Computers, and the Government Accounting Office will still be happy. It's the American thing to do."

Later that day, I stopped by the service station to see if Dennis had found a second source for the bulb. "Sure have," he said. "Not only that, but I've got 10 bids from bulb installers. Let's see, the lowest is from a small Maryland firm called Aunt Martha's Electronics Wonderland. They'll screw it in for \$10.95."

#### **PROFESSIONAL**

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NCC 86 Preview Automatic Test Equipment Connectors Interface ICs

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#### THE TELECOM LEADERS



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**Digital VLSI Engineers**—BSEE/MSEE with a minimum of 4-6 years experience in semicustom VLSI design, fast CMOS and ECL technology. Expertise with Daisy CAD sytems, custom VLSI and 50 MHz CMOS desired.

**Digital Signal Processing Engineer**—BSEE/MSEE with 4-8 years experience in DSP, time domain equalizers, 256 QAM modulation, multi-level modulation, passive filters and FIR digital filters required.

**High Speed Digital Engineers**—BSEE with 2-4 years experience in high speed digital design using ECL logic design, multiplex circuits, demultiplex circuits required. Knowledge of impediance matching and load termination desirable. Prior analog circuit experience very helpful. Expertise in LSI, SPICE, CAD, helpful. Position involves design of digital multiplex/demultiplex modules for high capacity lightwave transmission equipment.

#### **DIGITAL CROSS-CONNECT DESIGNERS**

**Software Project Leaders**—BSEE/CS or MSEE/CS with a minimum of 5 years experience in communications protocol interfaces, 68000/68HC11 microprocessor memory. VME Bus and Processor system peripherals. Experience in microprocessor assembly language and "C" level language required.

**Digital Cross-Connect Systems Engineers**—BSEE/CS or MSEE/CS with minimum of 3 years experience in the software design of real time systems for control, monitoring and provisioning of Digital Cross-Connect Subsystem modules. Experience in VAX based UNIX\* development system required. Knowledge of "C" language and 6800/68000 assembly, real time operating systems, data base management, test and maintenance software, matrix control and remote communication interfaces.

**Gate Array Designers**—BSEE/MSEE with minimum of 3 years experience in design of high density CMOS VLSI gate arrays for use in DS3 Cross-Connect Systems. DAISY, CADNETIX and CAD equipment knowledge required.

**Control Subsystem Project Leaders**—BSEE or MSEE with minimum of 6 years in communications protocol, interfaces, 68000/68HC11 microprocessors, VME Bus and Processor system peripherals. "C" language desirable.

**Switching Matrix Project Leaders**—BSEE/MSEE with minimum of 6 years experience in DS1, DS2, DS3 hierarchial rate MUX/DEMUX, input/output conditioners, space matrix modules and interconnect subsystems and knowledge of microprocessors.

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- **Navigation Systems**
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We are particularly interested in seasoned professionals with experience in real-time energy applications to largescale program development including PPS, design, coding, checkout, and documentation; SEL 32/27 and its software operating systems; Sperry-1100 equipment; and high order language programming, preferably Pascal, including design reviews, test, and evaluation of digital computer program performance.

In addition, Sperry's Corporate Technology Center in Reston is the site of advanced research in Al and signal processing. This is a creative research environment devoted to the exploration of many intriguing areas such as knowledge representation and acquisition, reasoning, natural language, distributed problem solving, and parallel algorithms and architectures, with applications in expert and knowledge-based systems, intelligent interfaces, data and information management, and Al development tools

Sperry in Reston offers all the advantages of a fast-paced, high-tech environment. Only 18 miles from Washington, D.C., Reston offers easy access to the sophistication and excitement of our nation's capital . . . as well as the beauty of nearby Shenandoah Valley and Blue Ridge Mountains.

The Sperry Corporation provides the compensation and benefits package you would expect of a Fortune 100 Company: medical coverage including a dental plan, life insurance, a retirement plan, tuition assistance, in-house education, and more. Please send your resume in complete confidence to: SPERRY COR-PORATION, SYSTEMS MANAGEMENT GROUP, 12010 Sunrise Valley Drive, Dept. EDCE, Reston, VA 22091. (703) 620-7000.

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High technology growth in the Pacific Northwest has resulted in significant expansion of the intellectual community. Major research and development facilities have been established.

One of the most exciting of these is the Artificial Intelligence Center of the Boeing Computer Services Company, a division of

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The center is situated on 28 campus-like acres just freeway minutes from downtown Seattle and the University of Washington. It's unique setting, complete with jogging trails, is only one reason to consider joining us. The area is also known for its intellectual stimulation, various cultural opportunities, quality of worklife and strong underlying pioneer spirit.

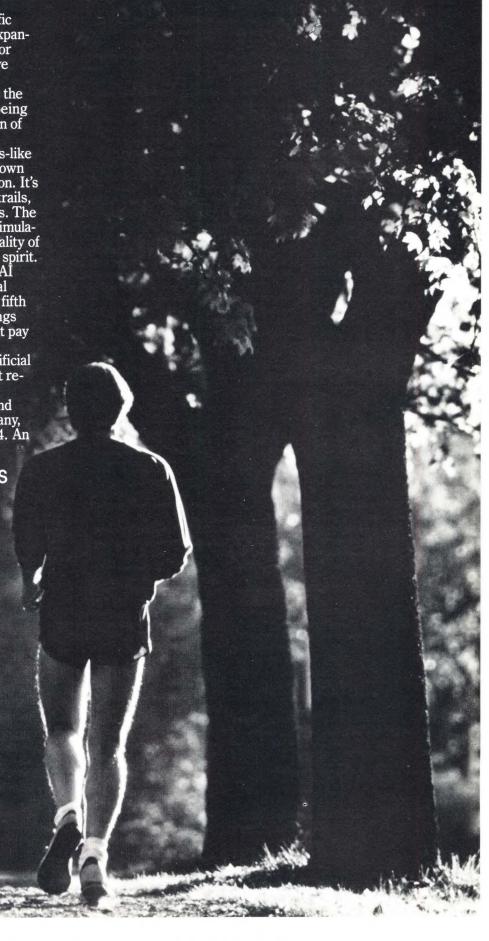
Even more important, work at our AI Center is on the leading edge of natural language and robotics as well as other fifth generation breakthroughs. Our openings offer plenty of challenge. Plus the right pay and comprehensive benefits.

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Digital has invested nearly a decade in building the LSI Division, and over that time many people have made significant contributions that have guided and shaped LSI to the highly respected organization it is today.

Our key goal is to create an environment that is technically challenging, is entrepreneurial in nature, stimulates learning and values people as our most important resource. We think the LSI organization's accomplishments reflect that environment and the excellent people who have chosen to work in LSI. We hope you will choose LSI for your future.

Our Semiconductor Engineering Group (SEG) is a winning, world-class VLSI component and system development group. We provide innovative VLSI components, systems and design services that give our customers a competitive advantage. We designed Digital's Micro T-11, Micro J-11 and MicroVAX chips. We have immediate need for engineering, physical science, and 1611111BH1417

computer science professionals with significant experience in:

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In addition to our custom VLSI technology, SEG develops high performance SEMICUSTOM technology as well. This area is growing very rapidly and as a result we have openings at all levels for individuals experienced in:

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- •VLSI SYSTEM DESIGN System Architecture Behavorial Modeling Logic Design Using Cell Libraries MOS Architecture and Simulation
- •SEMICUSTOM CAD Schematic Capture Auto Placement and Routing Mixed Mode Simulation Training and Documentation

• DESIGN ANALYSIS Semicustom Technology System Architecture System Partitioning Performance and Cost Modeling User Applications

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Responsible for the design and development of analog, digital and RF circuits and functions. In-depth managerial capabilities are required with minimum of 5 years' experience in TPS development.

#### ATPG ENGINEERS (All levels)

Automatic test program generation (ATPG) for test program sets, which require familiarity with computer-aided logic simulation tools such as LASAR, HITS, LOGO, and SPICE.

#### ORLANDO/ST. LOUIS OPPORTUNITIES

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#### TPS ENGINEERS (All levels)

Analysis of digital and analog circuitry as well as ATLAS program generation, integration and acceptance test procedures.

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Identify and develop new business opportunities for TPS avionic systems. Minimum 5 years' TPS experience in marketing and engineering with exposure to DOD agencies, specifically Air Force and Army.

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Manage programs from bid and proposal through completion. Requires minimum 5 years' experience in engineering, including 3 years in program management with profit and loss responsibilities.

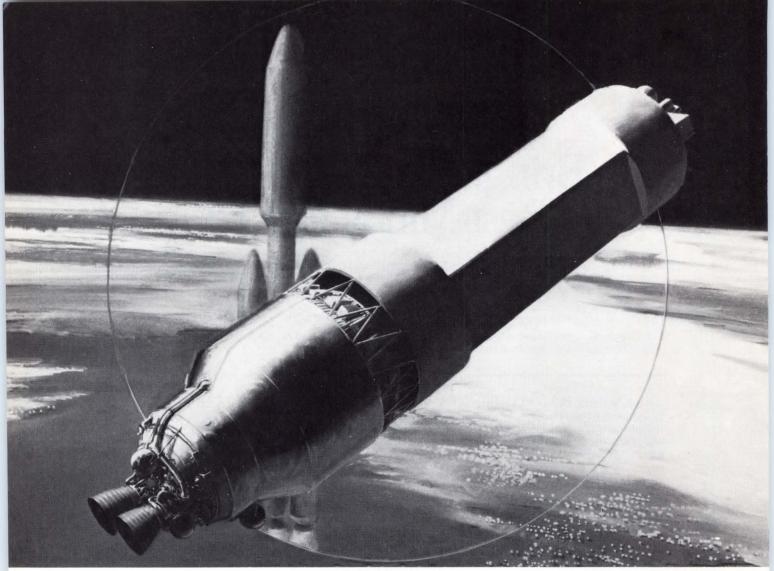
As part of the Fortune 200 Harris Corporation, Florida's largest industrial employer, GSSD offers excellent compensation and a comprehensive benefits package including relocation assistance. If interested and qualified, please forward your resume to Kathy Van Deusen at Harris GSSD, Dept. ED, 1401 S. Semoran Blvd., Bldg. 6, Winter Park, FL 32792.

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- Cryogenic/Propulsion Systems
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- Mission Analysis

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- Performance Analysis
- Trajectory Analysis
- Thermodynamics
- Structural Analysis

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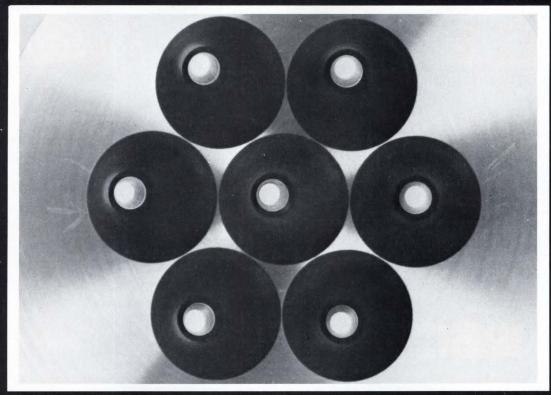
- Power Systems
- Digital/Analog Design
- Guidance, Navigation & Control
- Launch Control
- ATE
- Harness Design
- Instrumentation
- Radar Analysis/RF
- · Packaging

These positions require a technical degree or the equivalent combination of formal education and related experience. Government or aerospace industry background is preferred.

If you are interested in one or more of these areas, please send your resume to: Division Vice President — Research & Engineering, GENERAL DYNAMICS SPACE SYSTEMS DIVISION, MZ C1-7143-I020, P.O. Box 85990, San Diego, CA 92138.

#### **GENERAL DYNAMICS**

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Lincoln Laboratory is a federally funded research center operated by the Massachusetts Institute of Technology and offers competitive salaries and comprehensive benefits. Interested candidates are invited to send resumes, specifying area of interest, to: Susan B. Colcock, Box ED, MIT Lincoln Laboratory, Lexington, MA 02173.

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If you are such an individual and have a background in one of the following areas, we'd like to talk to you.

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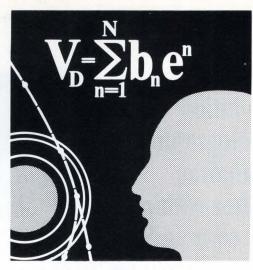
Engineers — Requires hardware oriented background, but principally involved in theoretical analysis of new satellite communication methods. Must possess good writing skills and strong customer interface ability. Responsible for development of new business in advanced wideband communication, including modems, bandwidth efficient modulation, link analysis, equalization and AM/FM. Prefer MSEE/PhD with 10 years related experience. Contact Paulette Dorris.

#### **Electronic Systems Engineers**

Develop electronic equipment specifications from requirements documents. Participate in the analysis/allocation of performance parameters between equipment comprising electronic systems/subsystems. Review performance achieved and recommend appropriate action. Should be familiar with design and analysis requirements of high performance receiving systems. Prefer BSEE with 5 years related experience. Contact Paulette Dorris.

#### Reliability Assurance Engineers

Responsible for product reliability in a production/field environment. Requires experience in circuit design, system analysis, environmental testing, failure analysis, and statistical analysis of complex electronics hardware/software. Conducts statistical analysis utilizing computer techniques. Prefer BSEE with 3 years experience in military products. Contact Bob Eddy.



#### Reliability & Components

Engineers — Current experience in maintainability design, analysis modeling and prediction, bit and self test effectivity/efficiency analysis, system safety/hazard analysis, safety fault tree analysis and FMEA. Sneak circuit analysis, plus automated production experience highly desirable. Prefer BSEE with 7 years experience in maintainability and safety engineering. Contact Bob Eddy.

#### Radiation Design Engineers

Provide circuit design guidelines, and perform circuit analysis and equipment survivability/ vulnerability (S/V) testing on digital and analog equipment to ensure S/V requirements. Prepare radiation hardness plans and reports. Prefer BSEE with 5 years related experience. Contact John Nolitt.

Join the people of Motorola's **Government Electronics Group**, where we are creating advanced electronics for a more productive world. The benefits are many, including sunny Arizona — a land as beautiful as it is abundant with recreation and culture.

For prompt consideration, forward your resume in confidence to the appropriate technical recruiter at Motorola Government Electronics Group, 8201 E. McDowell Rd., Dept. B606, Scottsdale, AZ 85252; (602) 949-3759.



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- Parts and Reliability
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- Communications

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#### Circulation by Industry

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Computers	12,295
Computer peripheral equipment	9,548
Systems integration	6,427
Office and business machines	3,007
Communications Systems and equipment	22,480
Total:	53,757

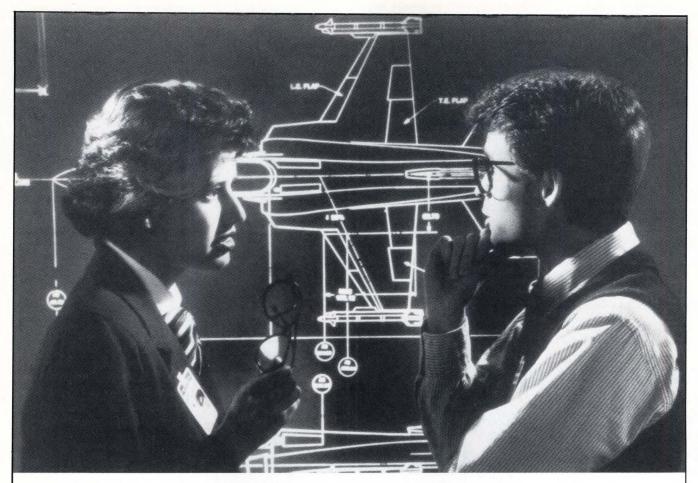
Military and Test	FET TO
Navigation and guidance	
systems and equipment	6,249
Aircraft, missiles, space,	
and ground support	15,037
Oceanography and support equipment	708
Test, measurement,	
and instrumentation	11,846
Government and military	10 104

Total:

43,944

Industrial Controls, Research, and Industrial control systems,	Medical
Industrial control systems,	
equipment, and robotics	15,354
Independent research and testing	2,616
Medical electronics	4,404
Total:	23,374

Components, Consumer, and Other	
Components and subassemblies	5,542
Consumer electronics	3,713
Other OEMs	4,597
Users of electronic equipment	1,255
Total:	15,107
Total qualified circulation:	136,182



## Technology knows one direction . . . Forward.

"Technology is obviously and undoubtedly cumulative and progressive." George Sarton, Science Historian

Each new scientific discovery builds upon the last, and provides a foundation for the next, forming a limitless ladder of technological achievement. If you are a professional who thrives on this kind of relentless exploration, you should explore Northrop DSD. You'll enter an atmosphere charged with innovative thinkers working together in close-knit project teams exploring new frontiers in ECM applications. We have positions available in the following areas:

Positions below require BSEE, or equivalent; MSEE preferred plus related experience.

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Duties will include analysis, design, development and testing of airborne ECM/EW antennas. Will also assist in preparation and debugging of new, state-of-the-art antenna range facility. Requires knowledge of phased arrays, monopulse D.F. systems and millimeter wave techniques.

#### **Power Supply Design Engineers**

Participate in the analysis, design and construction of power conversion, conditioning and control subsystems and modulators. Perform IR & D activities involving new techniques development in high voltage microwave/ millimeter wave transmission, nanosecond control of high DC voltages and modulation of microwave tube devices. Experience in switchmode/linear power system design at either high or low voltages required.

#### **Advanced Technology Engineers**

MICROWAVE: Active and/or passive microwave and millimeter wave integrated circuit design to include components such as oscillators, amplifiers, mixers, detectors and filters as well as integrated subsystems. Prior computer-aided design experience required.

RECEIVERS: Conceptual design, fabrication, and test of state-of-the-art receiver systems for ECM/Elint applications. Familiarity with systems architecture, signal processing, and channelized, set-on, and micro-scan techniques is desirable.

#### **Transmitter Engineers**

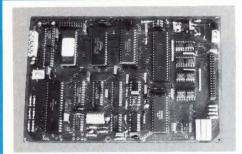
Responsibilities will include the specification, design and integration of high power microwave transmitter subsystems from first development models through production start-up. Applicants should have three or more years experience in high power transmitters and/or microwave frequencies. Background in analog and digital is desirable.

Qualified candidates are invited to submit resume with salary requirements to: Supervisor Staffing, NORTHROP CORPORATION, DEFENSE SYSTEMS DIVISION, 600 Hicks Road, Rolling Meadows, IL 60008. We are an equal opportunity employer M/F/V/H. All positions require U.S. Citizenship.

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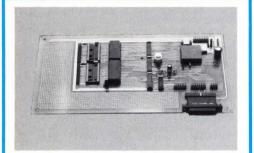
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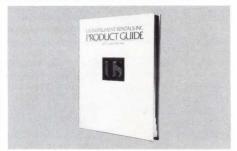
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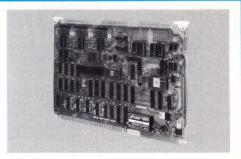
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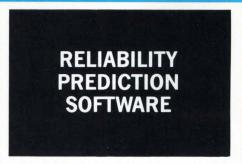
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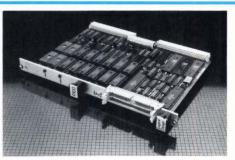
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EE/EPROM PROGRAMMER 264



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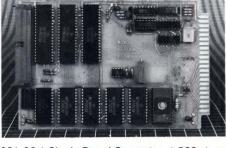


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\$91.00 \* Single Board Computer. \* 500 piece price, model MOL45 shown, 6800 MPU, serial I/O, parallel I/O, RAM, EPROM, 44-pin 4.5" × 6.5" PCB EXPANSION MODULES, RAM, EPROM, CMOS RAM battery, analog I/O, serial I/O, parallel I/O, counter/timer, IEEE-488, EPROM programmer, floppy disks, cassette, breadboard, keyboard display. Wintek Corporation, 1801 South Street, Lafayette, IN 47904 2993 (317) 742-8428, (800) 742-6809

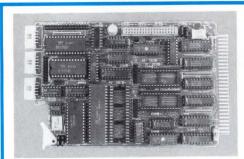
SINGLE BOARD COMPUTER



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15-20 MBYTE CARTRIDGE

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CMOS 80C88 SINGLE BOARD STD BUS COMPUTER features the 16-bit 8088 with 8087 coprocessor socket and 1 Mbyte addressing, On-board functions include 2 JEDEC 28-pin memory sockets for up to 128K bytes of RAM, EPROM, or EEPROM. Includes one RS-232/RS-422 serial port, 8259A interrupt controller, 3 16-bit counter/timers, SBX connector, and Watchdog timer. Available in NMOS/TTL or CMOS from WinSystems, Inc., PO Box 121361, Arlington, TX 76012; 817/274-7553.

8088 Single Board Computer

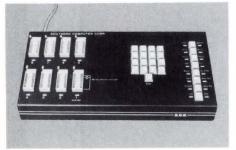
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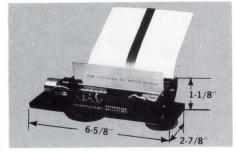
ANALOG WORKSTATION

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The SCC Cost Efficient Programmer for EPROMS/EEPROMS. Basic System \$1,195 includes: Keypad, serial port, display, 8 gang programming, set programming, and device menu—no personality modules. 256K byte memory option—program 512 devices. UV Eraser \$395. Southern Computer Corporation 3684 Clearview Avenue Atlanta, Georgia 30340 404/455-8018

PROGRAMMER

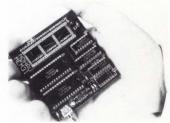


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SCI-NOVATIONS

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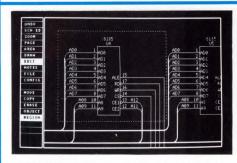
PC BASED INSTRUMENTS

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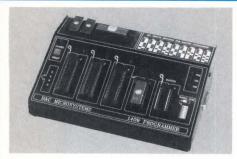


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**TRANSDUCERS** 

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SINGLE BOARD COMPUTER

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PCB LAYOUT PACKAGE

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8051/8048 DEVELOPMENT TOOLS

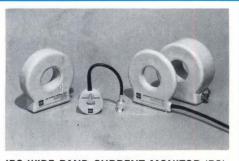
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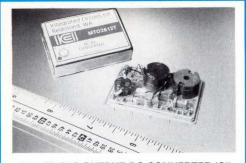
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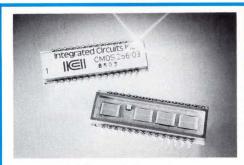
WIDE BAND CURRENT MONITOR



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INTEGRATED CIRCUITS

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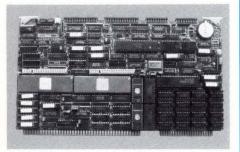
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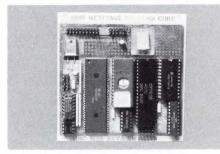
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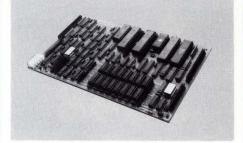
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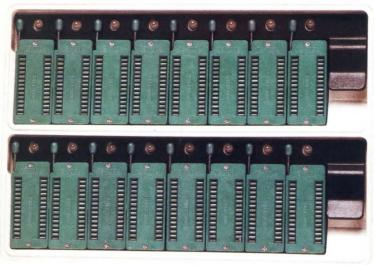
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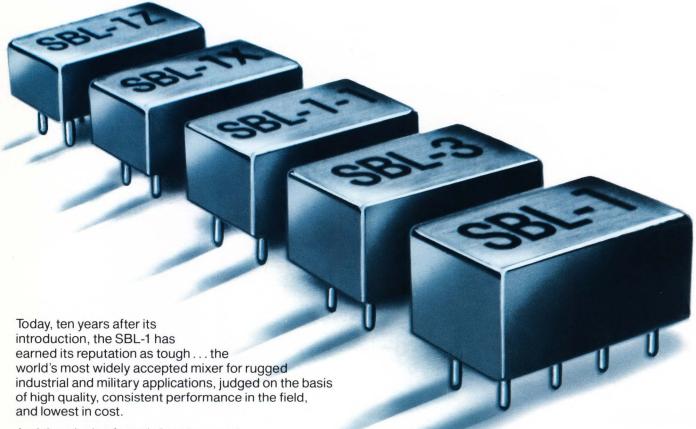
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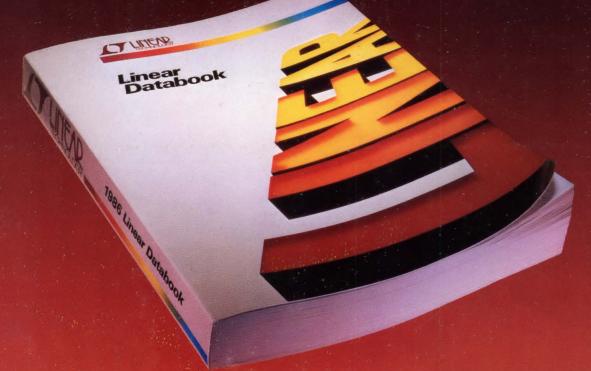
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