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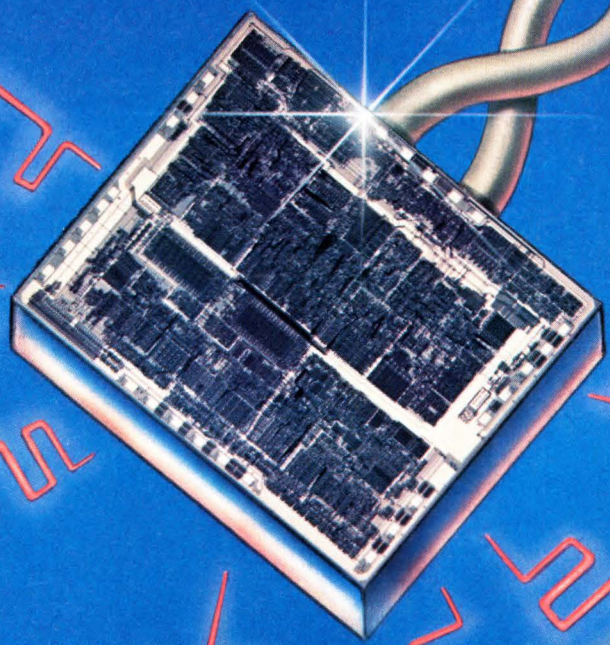
FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

DECEMBER 13, 1984

UNITING CONTROL AND ENCODING, A SINGLE CHIP SPAWNS PRACTICAL PC NETWORKS



Technology Report:
CAE software helps chisel verified designs into silicon

Product Report:
Modems trim size but not speed

Controller chip envelops full Basic interpreter

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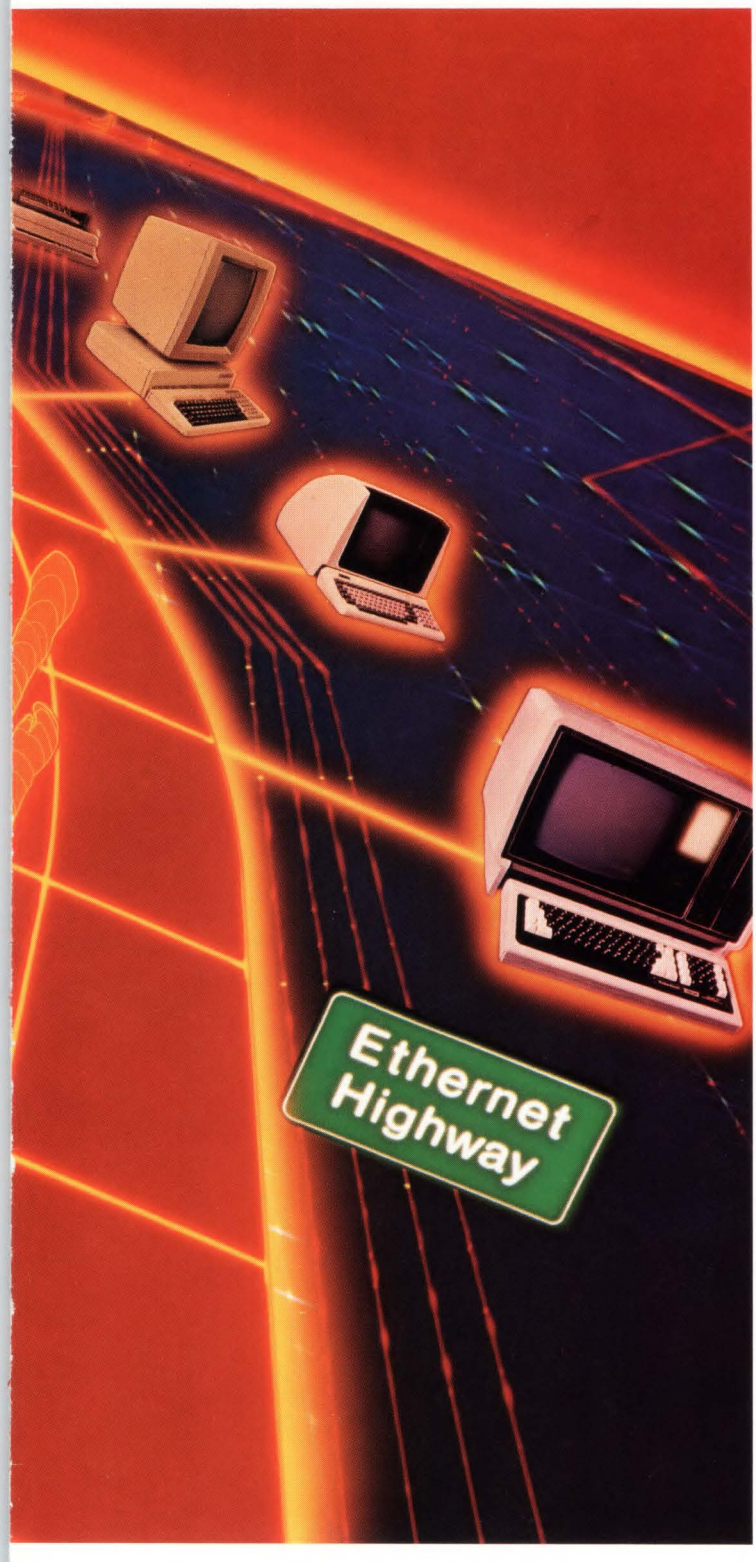

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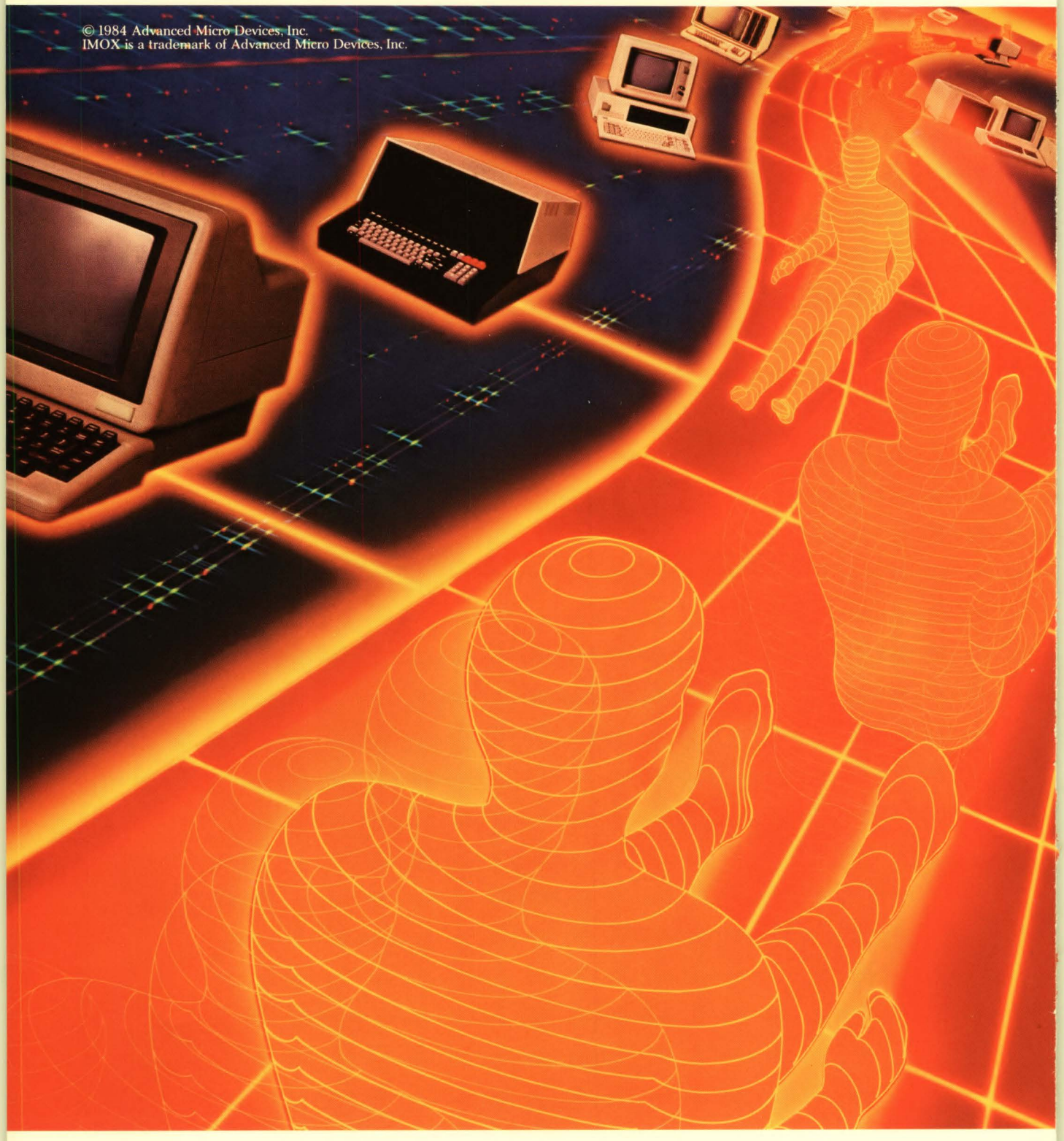

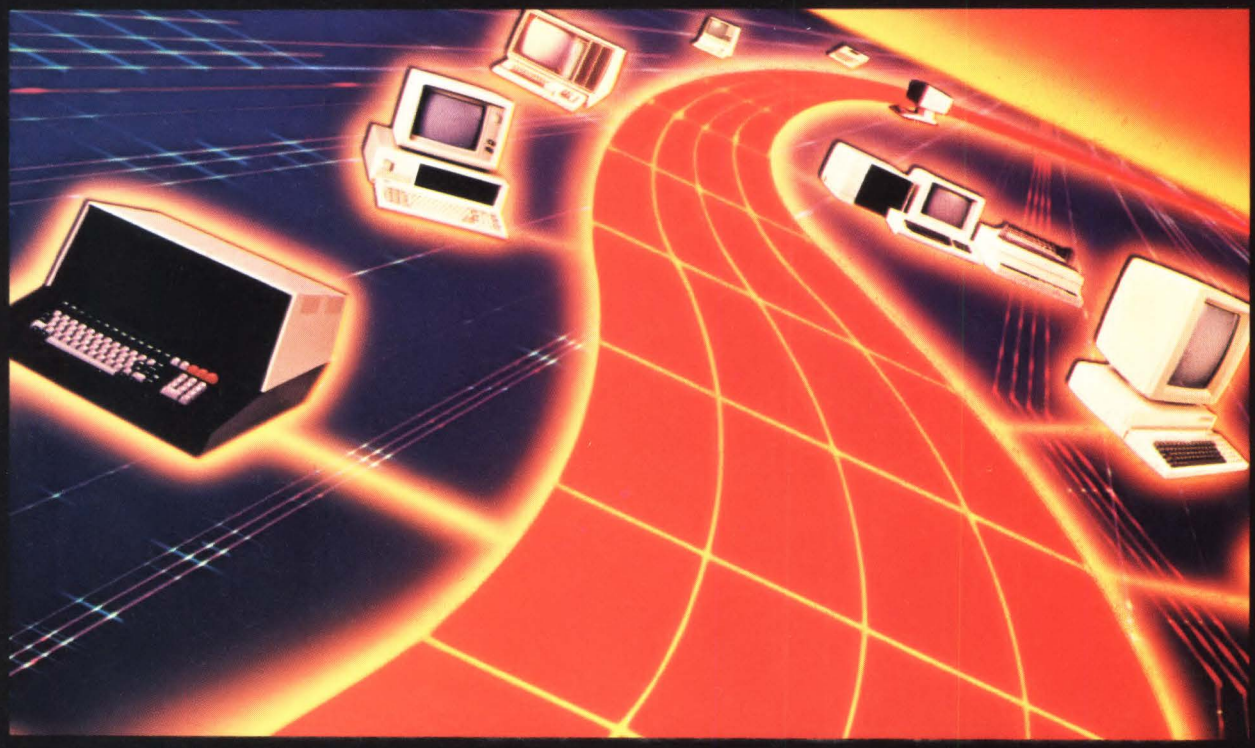

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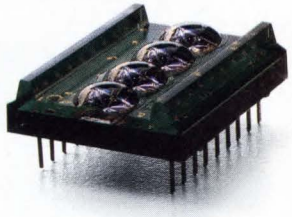

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BEHIND THE COVER

In an industry dominated by the notion that faster is better, Robert Galin talks proudly about a slower local-area network controller. "This is one case when the reverse is true," he says, "since lower speed means lower cost." Galin, who works in strategic planning at Intel, is not making an empty assertion: He helped devise the specifications for the 82588 LAN controller featured in our cover story (p. 141).

The idea behind the chip was born in 1981, out of the conviction that the telecommunications world would need more economical networks than Ethernet. Back then, Galin felt that Ethernet's CSMA/CD would be vital to such systems, but at more modest bit rates. He also predicted that both baseband and broadband transmissions would be successful.

Out of these beliefs, Galin helped design a highly versatile, low-cost single-chip controller—one that could be tailored to the networks he envisioned. The 1- and 2-Mbit/s 82588 does follow in the footsteps of an earlier Ethernet coprocessor, but its lower bit rate allows Manchester encoding to be done on chip. It also makes for an economical logic-based method for detecting collisions on the network, rather than the more costly analog-based scheme used in Ethernet.

Despite these differences, it proved possible to lift about 60% of the 82588 out of the coprocessor. Specifically, both chips' serial sections (which include parallel-to-serial conversion, framing, error checking, and the CSMA/CD mechanism) use identical masks. Modular design, Galin emphasizes, cut development time by at least a year.

Galin is rightfully proud of his role in helping his predictions come true. Two new systems—IBM's 2-Mbit/s broadband PC Network and AT&T's 1-Mbit/s baseband Starlan—aim squarely at low-cost personal computers. The 82588 suits both to a T.

ElectronicDesign
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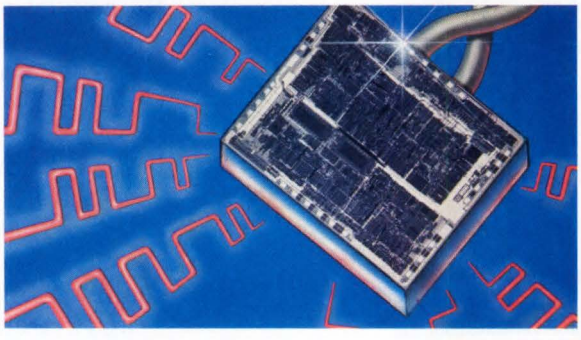
141 Cover: Monolithic controller builds PC network without toil or trouble
A controller chip puts CSMA/CD within the reach of personal computer networks, keeping a lid on parts count and simplifying software development.



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Cover illustration by Maura C. Flynn

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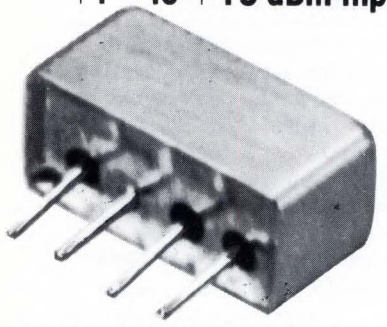

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F3	−40	−30
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CIRCLE 4

CONTENTS SPOTLIGHT

Technology Report: CAE tools 118

Circuit designers generally expend the most energy before and during IC simulation, but they rarely spend the same time on the steps that follow simulation. In fact, the decisions of how to translate the simulated circuit into silicon are perhaps the most critical, since they must balance cost, silicon use, and turnaround. As part two of our Technology Report details, a wealth of CAE software tools is emerging—many integrated into workstations—to steer designers to the optimum methods for layout and routing, verification, and circuit extraction.

Cover: PC network controller 141

Though system designers frequently tie personal computers into local networks, the systems themselves are usually geared more for minicomputers than for micros. Now a controller solves that problem in one chip: Designed specifically for personal computer-based networks, it slashes board count, board space, and development time. Moreover, its transfer rate—1 or 2 Mbits/s—is well suited to inexpensive twisted-pair cable.

Focus on board-level modems 251

Mix small computers with the ubiquitous phone lines, and the need for trimmer yet more powerful modem boards becomes inevitable. While shrinking the board circuitry, manufacturers are raising the transmission rate to a new high of 14.4 kbits/s and packing more features into their cards.

Conference Preview: ISSCC 61

Today's interest in application-specific ICs will be reflected when the International Solid-State Circuits Conference opens its doors next February. Naturally, memories and processors will grab the most attention, but traditional chips and analog circuits—including a 500-MHz digital-to-analog converter—will hold a place as well.

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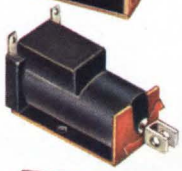

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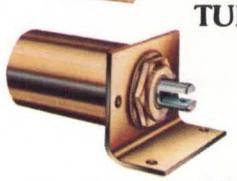

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CIRCLE 5

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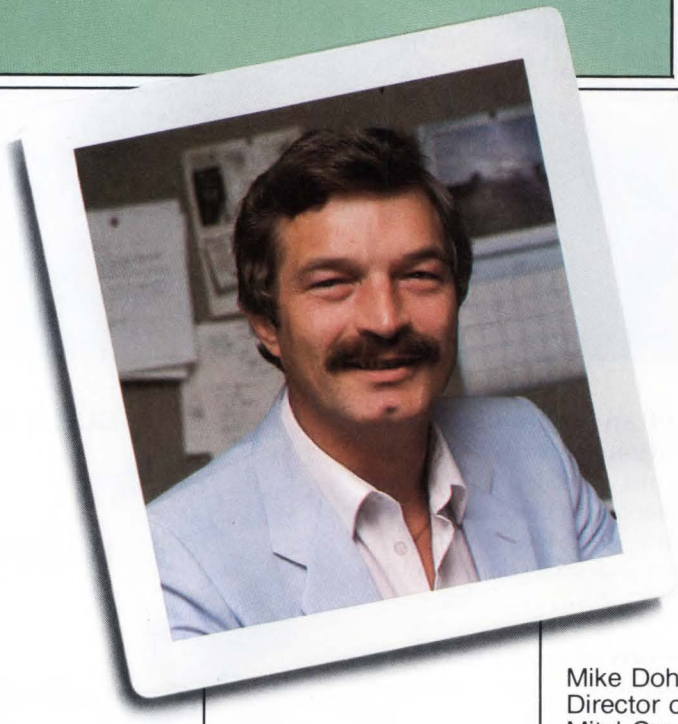

Mike Dohler,
Director of CAD/CAM
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Mitel's IC design group was assigned the task of integrating new technology into the manufacture of the DDX chips. Objective: maintain quality and function while making significant cost reductions.

"COMPLEXITY CREATES THE NEED FOR INCREASED CAPACITY."

–Duncan Klett, Manager, Work Stations & CAE

"We wanted to integrate dynamic RAM and the new silicon technology into the DDX design," said Duncan Klett. "The problem was the complexity of the circuit design. As you get more complex, your simulation needs increase geometrically. Our existing capabilities let us test pages and blocks of the design, but we couldn't simulate the chip as a whole. We tried to verify the total design using software simulation. After 30 CPU hours there were still no results, and we couldn't justify tying up the computer any longer."

THE ZYCAD LOGIC EVALUATOR.

Mitel's Logic Evaluator (Model LE 1001) has a capacity of 50,000 gates and a speed of 500,000 events per second. It is a dedicated hardware processor designed for complex logic simulation.

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Duncan Klett: "The Logic Evaluator was the perfect tool for this project. We found we could simulate the whole design quickly. As a matter of fact, we ran the DDX simulation over 100 times in a four month period and identified problems relating to interfaces and timing that wouldn't have shown up with partial simulation."

FIRST SILICON– RIGHT THE FIRST TIME.

In a project this complex, it is usual to go to a silicon prototype two, three or even more times. If the circuit design can be simulated and debugged perfectly before the first prototype, there are considerable savings in cost and the time it takes to get a new design to production.

Mike Dohler: "We found we could run a simulation of the complete DDX design in one hour and seventeen minutes on the LE. With that kind of capability, you can get all the information you need as fast as you can use it. That's a revolutionary shift for electronics designers."

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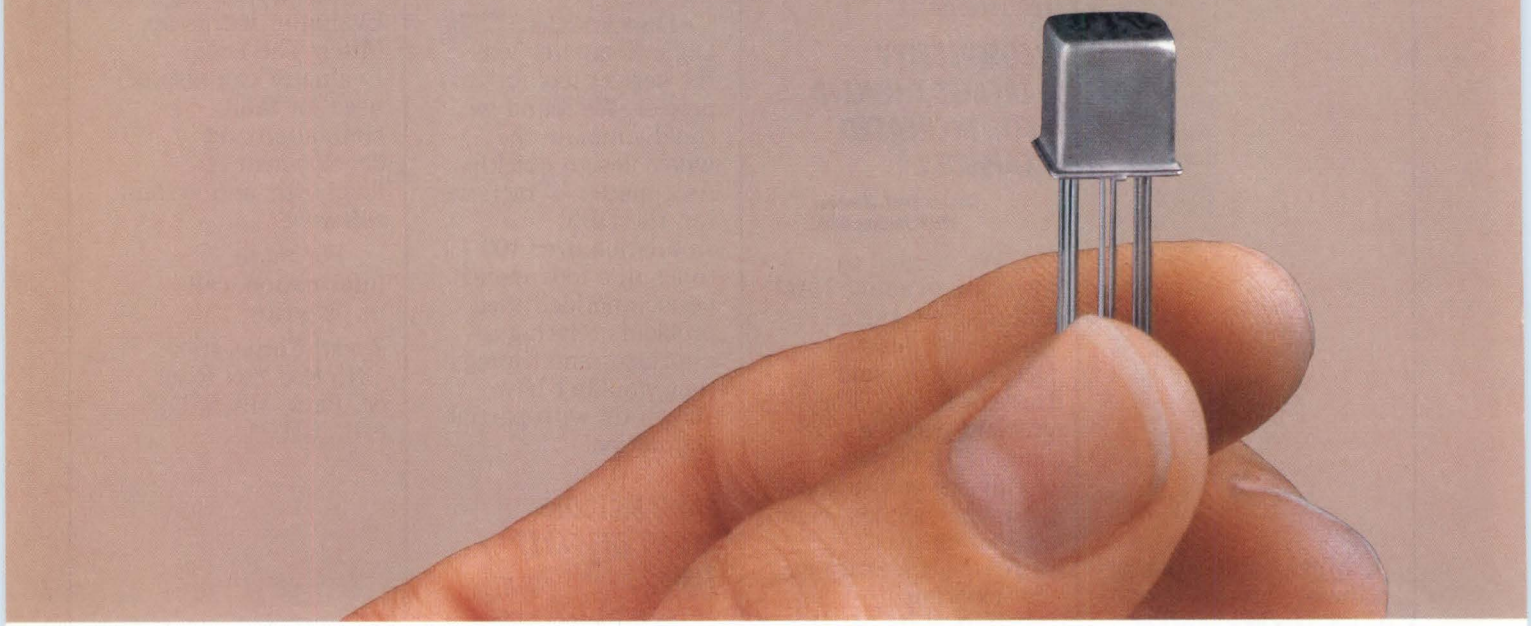

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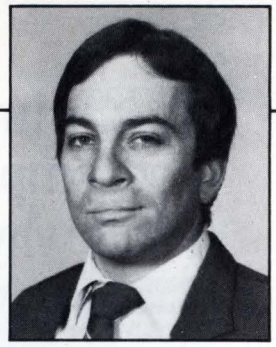
CIRCLE 7

ON REFLECTION



Be it design or test, cooperation is everyone's business

Perhaps the biggest obstacle standing in the way of higher productivity and shorter turnaround is the traditional separation between design and test engineers. As a former board test engineer, I have experienced the frustration of having boards handed to me, fait accompli, with no thought of their testability or ease of manufacture. Unfortunately, the design engineer is rarely graded on his performance in those two areas. For that reason, he generally hands the test enginer a prototype board (replete with many jumpers) and a schematic that may or may not be current and simply says, "Here."

My former colleagues in chip testing encounter similar situations. Here too, design and testing are separate and often hostile groups. In most cases, the test engineer has no input into the early stages of the design process. If he did, his trained eye would no doubt detect problems in testability. Minor changes made at that point could save millions of dollars during test generation and manufacture.

Make no mistake about the amount of money—not to mention time—involved here. High-level engineering talent may spend several man-years generating test programs for modern VLSI chips. Worse still, chips designed with little thought of testability demand test programs of inordinate complexity. Extremely costly to produce, those chips may also cause more than their share of difficulties on the manufacturing floor.

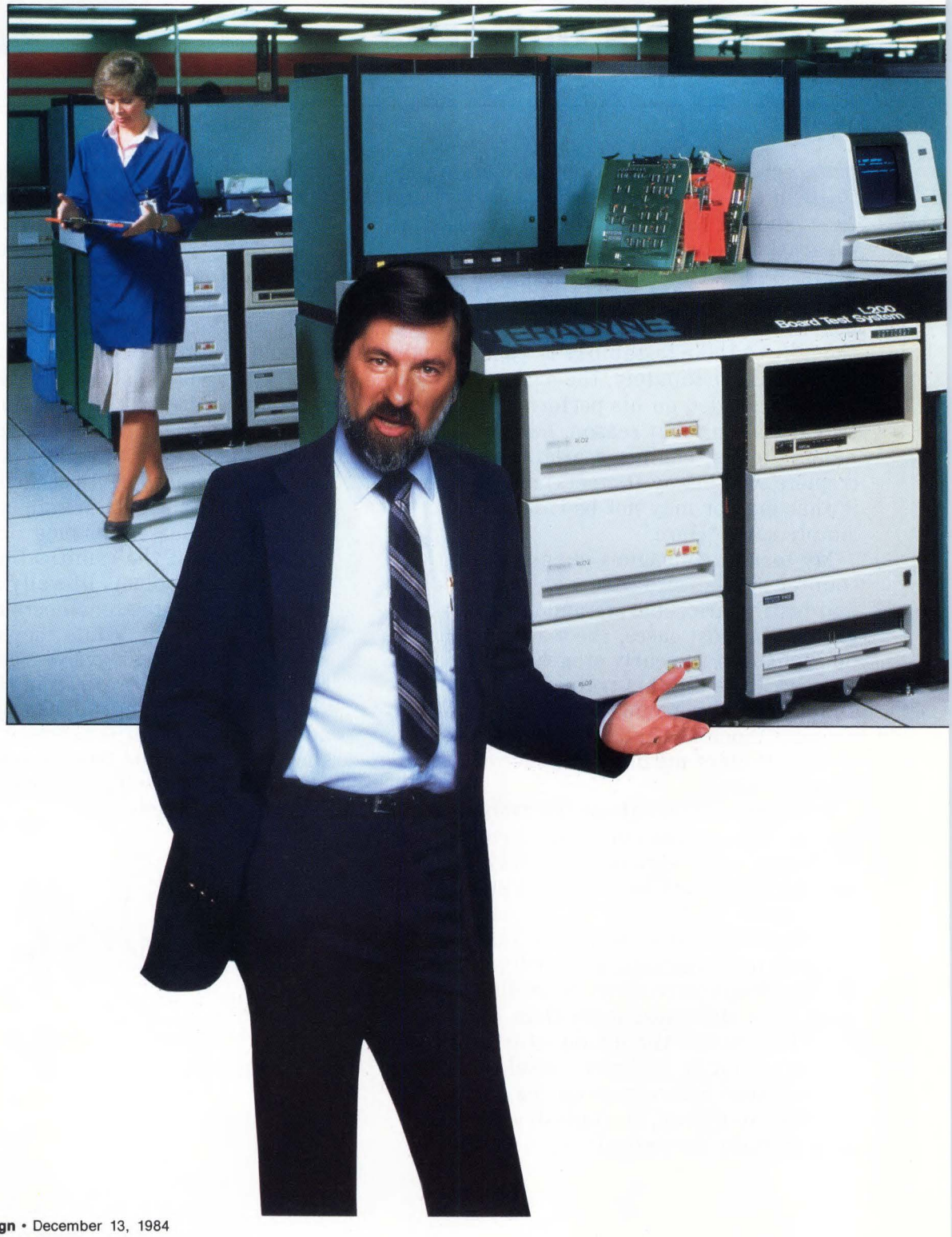
Spurred on by designers' need to verify performance before making the costly commitment to silicon, the industry is beginning to right its wasteful ways. With the help of the ATE segment, design and testing are undergoing substantial changes. For instance, a new generation of powerful digital simulators is proving a boon not only to designers but also to test engineers, who apply them to test program generation.

As worthwhile as such tools may be, in the end communication is even more valuable. With today's local networks, there is no reason why critical information culled during the design stage and stored in a data base cannot be accessed by test engineers. Adding the appropriate security measures ensures that the design stands no danger of unauthorized access or modification.

Just think of the ramifications: Instead of discovering problems literally after "the die has been cast," test engineers can diagnose troublespots early, while they can still be easily—and inexpensively—rectified. With the test engineer involved in the design stages, the test program can be debugged and prepared months before it is now. That shorter turnaround time is something that everyone agrees with—designer, test engineer, and manager.

Gary Elinoff

"ATE is important to us.
The company behind ATE is more important.
That's why we chose Teradyne." *Bob Dances*
Xerox Corporation



"With the costs involved in getting new products to market today, we couldn't afford to buy ATE the way we used to.

"We couldn't just settle for a good piece of test gear. We had to find an ATE company that would work with us, partner to partner, to solve our toughest testing problems.

"A company like Teradyne."

Bob Dances of Xerox understands that vendor-customer relationships are important in ATE. So do we. That's why we created our Test Assistance Group (TAG), a worldwide organization with a single charter: helping customers realize the full potential of their Teradyne systems.

TAG engineers will work with you to get your systems up and running fast. And when you hit the rough spots, they'll be there to help you through them.

They can also deliver special hardware and software for specific applications, including turnkey packages.

In the age of VLSI, testing is often a do-or-die proposition, with the success of a product line or even a company hanging in the balance. We can respond to this challenge because we've made production-line testing our business for almost a quarter century.

Whatever it takes to keep your test systems running productively, we're ready to deliver, through a team of dedicated professionals only a phone call away.

When Xerox says ATE partnerships are important, it's a thought worth copying.

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Bench users will like the way this counter speeds manual measurements. At the push of a button, you'll make waveform measurements such as peak, pulse width, rise and fall...automatically and fast. And its ability to store up to ten front-panel setups in its non-volatile memory will save you set-up time and trouble.

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You get a lot of performance in this counter bargain. Single-shot resolution of 2 ns, 100 MHz frequency operation is standard or 1.3 GHz C-channel optional. Fast, unformatted throughput of 150 measurements/second. There's even an optional 4-digit, autoranging, auto-polarity DVM. And naturally, it's fully compatible with the IEEE Recommended Practice for Code and Format Conventions of IEEE-728.

Whether you need precise measurements of oscillators, generators, transmitters, system clocks or other frequency or time-related applications, the HP 5334A comes up with the right numbers.

The quickest way to get our number.

For more information on the HP 5334A Universal Counter or the full range of solutions to your time interval or frequency measurement problems, request our data sheet and our complete counter brochure. Call your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

*U.S.A. list price only.

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CIRCLE 9

HEWLETT PACKARD

02014

READER FEEDBACK

Corrections

An extra zero in our Oct. 31 New Product story on Verbex's Series 4000 speech recognizer (p. 447) raised the price of the development software an order of magnitude. The correct price is $500.

The Nov. 15 NewsPulse item on the C-1 supercomputer (p. 37) omitted the name of the manufacturer: Convex Computer Corp. (Richardson, Texas).

Filling in a major omission

Your Product Report, "Focus on Monolithic Precision Op Amps," in the Oct. 31 issue [p. 337] is interesting but somewhat incomplete and not quite up to date: It overlooks the best monolithic FET operational amplifier on the market, Burr-Brown's model OPA111, which was featured as the cover article of your Feb. 9, 1984, issue [p. 97].

The OPA111, a DIFET (dielectrically isolated FET) amplifier, achieves an offset voltage of $\pm 250\ \mu V$ maximum, drift of $\pm 1\ \mu V$ maximum, an open-loop gain of 120 dB minimum, and common-mode and power supply rejection ratios of 100 dB minimum. What's more, noise is 100% tested and guaranteed (not just sample-tested) to be $8\ nV/\sqrt{Hz}$ maximum at 10 kHz, and the bias current is only ± 1 pA maximum. In addition, a low-cost version, the OPA121KP, is now available in an eight-pin plastic package.

Also, we thank the author for mentioning our new, enhanced version of the OPA27, but there are a few points that should be explained. Since we use the industry-standard grades in our OPA27 and OPA37, the minimum and maximum specifications remain unchanged, but performance has been improved in many areas. We now guarantee noise on the A and E grades by 100% testing. Furthermore, Burr-Brown is unique in providing 100% popcorn-noise screening on all OPA27 and OPA37 grades.

To avoid confusion when describing parameters on new products, I suggest you feature only minimum and maximum specifications. These guaranteed specs are what engineers must use for design—"typical" specs are provided only as a guide to help understand how a device performs.

Reputable manufacturers generate "typical" data from the mean performance of a large number of devices from many production lots, but there is always some unit-to-unit variation, and some manufacturers don't generate "typical" specs in this manner. It would therefore seem that the best standards for comparison would be the guaranteed minimums and maximum.

Neil P. Albaugh
Electronics Engineer
Burr-Brown Corp.
Tucson, Ariz.

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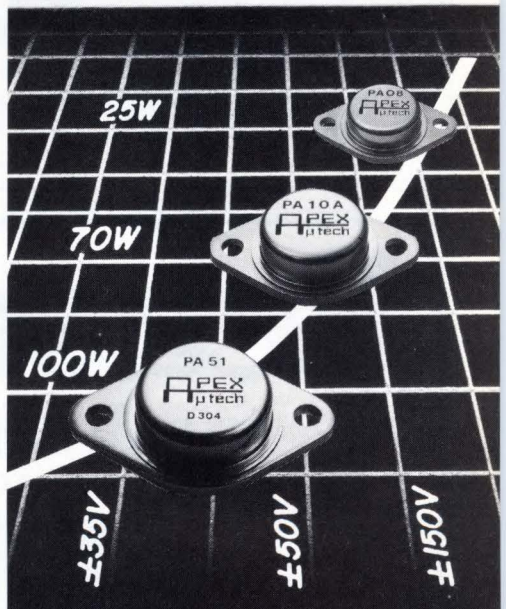

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CIRCLE 10

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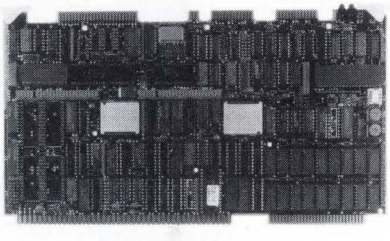
CIRCLE 11

Reason #34 to call Zendex 2nd

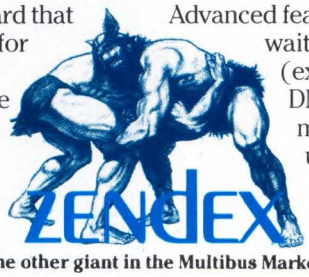
(If you insist on calling Intel first.)



ZX-186/30 CPU Board

An 80186-based CPU board that is an ideal replacement for the iSBC-86/30 or iSBC/86/12A. It is fully software compatible with the ZX-86 and the entire iSBC-86 family.

Advanced features: 256KB zero-wait-state on-board RAM (expandable to 1MB) two DMA channels, Dual multi-protocol USART, up to 128KB PROM and two iSBX connectors.



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CIRCLE 12

READER FEEDBACK

Engineers: Keep it clean

Reading Heather Bryce's recent On Reflection [Oct.4, p. 11] brings another issue to mind. Cleaning up a desk or a workstation is the first step in "cleaning up" our business and technical minds. I consider it amazing how few (even brilliant) people recognize that personal "housekeeping" is mandatory, as is an orderly file system. But remember, out of sight, out of mind—always keep clear "flags" before your face.

Errol A. Campanella
Component Engineer
Los Angeles Components
Alhambra, Calif.

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Editor-in-Chief, Electronic Design, 10 Mulholland Drive, Hasbrouck Heights, N.J. 07604. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.

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Motorola Reports

DECEMBER ISSUE 1984

256K DRAMs make speed/density waves

- ☐ Ultrafasts oust tradition
- ☐ Stepper drive simplifies
- ☐ MC68020 development support

MOTOROLA

Put four times the DRAM in the same slot...and still run faster.

Motorola's 256K MCM6257 dynamic RAM runs faster than the fastest 64Ks, and puts four times the memory in the same package.

It's a good thing. Demand for high-speed RAM is climbing astronomically, and forecasts project an industry shortfall of 256Ks despite the apparent number of suppliers. The world's systems crave more and more RAM, and the more they use the more they seem to need.

Motorola addresses these requirements with 256K dynamic RAMs that provide both flexibility and design freedom. All control and refresh lines are the same as with our 64Ks, and our 256Ks are also pin compatible with the 64Ks.

You get familiar architecture, technology and packaging, so ease of use is assured. The similarity stops there.

When we say the MCM6257 is fast, we're referring to the 100 ns maximum access time. Slightly slower versions are also available, at 120 ns and 150 ns. Even with 100 ns speed, power dissipation is very low. Supply Current is only 4.5 mA standby, and 70 mA active. Operation is from a single +5 V supply.

High-performance triple-poly silicon-gate technology permits fabrication of denser, faster memory...the secret to packing so much performance on one small chip. Laser fuse-redundancy and direct step-on-wafer manufacturing ensure maximum yields. A row and column address input multiplexing scheme holds address lines down to nine, so the standard 300 mil wide 16-pin package handles the 256K with ease. For surface-mount applications, however, alternative 18-pin JEDEC-standard plastic J-leaded chip carriers will be available, too.

In addition to $\overline{\text{RAS}}$-Only and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ automatic refresh modes, the MCM6257 offers Nibble mode, which allows serial access of up to four bits of data at very high rates... 20 ns access and 50 ns cycle times. Refresh is 256 cycle, 4 ms.

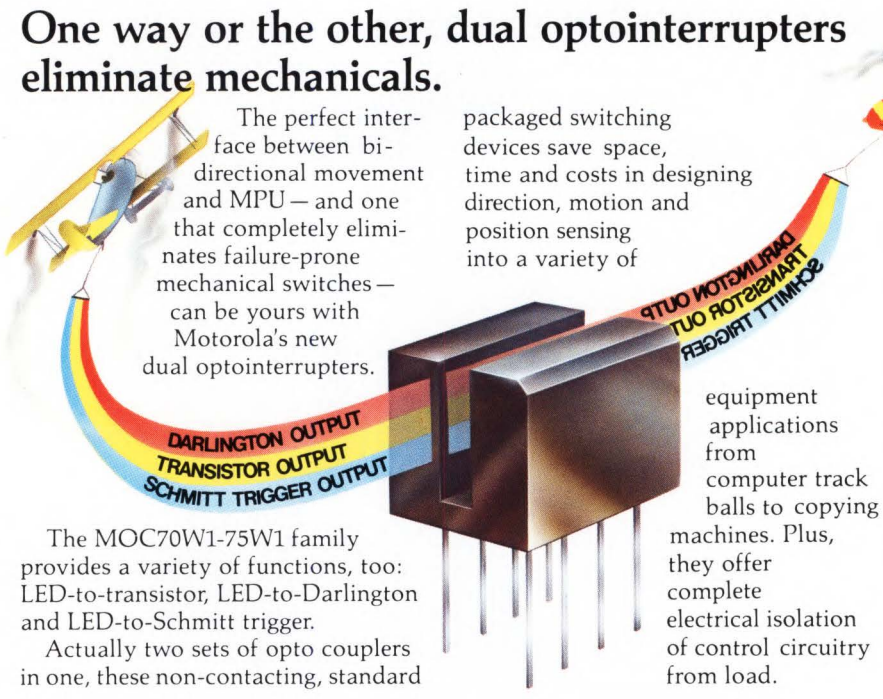
All MCM6257 inputs and outputs are TTL compatible, including clocks. Complete address decoding is performed on the chip with address latches incorporated. Data out is controlled by $\overline{\text{CAS}}$, enhancing system flexibility.

The MCM6257 is just the beginning. We also have a variety of 256K DRAMs in the works with different speeds and, of course, CMOS.

So as the need grows for greater density and higher performance in a cost-contained environment for any conceivable application, look for Motorola. We're there.

Check ☐ A for information.

One way or the other, dual optointerrupters eliminate mechanicals.



The perfect interface between bi-directional movement and MPU — and one that completely eliminates failure-prone mechanical switches — can be yours with Motorola's new dual optointerrupters.

The MOC70W1-75W1 family provides a variety of functions, too: LED-to-transistor, LED-to-Darlington and LED-to-Schmitt trigger.

Actually two sets of opto couplers in one, these non-contacting, standard packaged switching devices save space, time and costs in designing direction, motion and position sensing into a variety of equipment applications from computer track balls to copying machines. Plus, they offer complete electrical isolation of control circuitry from load.

The emitter-detector slot is 0.125" wide, big enough to easily accommodate a wide variety of tripping mechanisms.

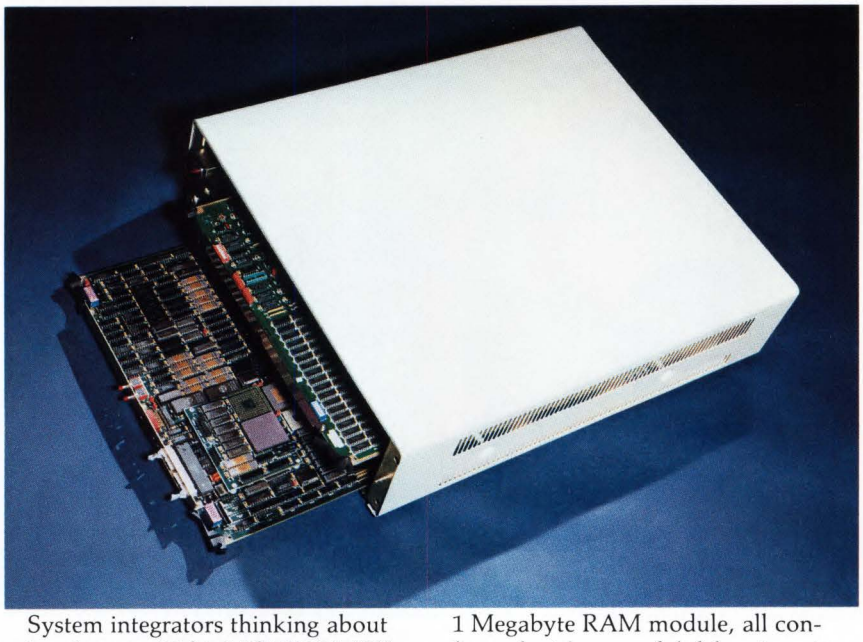
The high gain Darlingtons optimize applications calling for low-drive-current or larger output signal devices. The Schmitt trigger provides the fastest, cleanest signal sensing of all.

Narrow apperatures in front of each phototransistor allow strong signal transfer and shield the device from ambient light and crosstalk from the other LED and provide dirt and dust protection.

The standard dual optointerrupter package is designated by the "W" in the part number. Prices range from $2.55 to $3.55, 1K-up.

Check ☐ B for information.

Benchmark 20: First to evaluate. First to market.



System integrators thinking about using the new 32-bit MC68020 MPU now have an excellent testbed for system evaluation: Benchmark 20.

This MC68020-based system package provides a variety of hardware and software tools to allow streamlined 32-bit benchmarking, code development and debugging. Packing a lot of power into a small space, the Benchmark 20 system contains a single-board microcomputer with the MC68020 MPU, plus an auxiliary 1 Megabyte RAM module, all configured with powerful debug/monitor firmware in a 4-slot chassis.

The result? You reduce time-to-market for your new 32-bit system product. Benchmark 20 is configured and ready to use alongside an appropriate software development host to trim your schedule for MC68020 benchmarking and code debugging.

The VM04 VERSAmodule CPU board utilizes the capacity of this new 32-bit performance standard to achieve speeds in the 2-3 million instructions per second (MIPS) category. 4K long words of on-board instruction/data cache reduces off board memory accesses to insure top performance.

The companion dynamic RAM VM13 module provides 1Mbyte of random access memory dual ported with both RAMbus and VERSAbus. A perfect system mate for the VM04 32-bit monoboard, the VM13 RAM board has error detection and diagnostic capability.

To help you quickly evaluate the MC68020 and the VM04, the Benchmark 20™ system package incorporates the 020bug™ Debug/Monitor firmware package to allow you to de benchmarking and to debug code. The 020bug resident package allows full speed execution of system and user developed programs operating out of the Benchmark 20 system package. A powerful software and system debug command set allows access to all VM04 I/O, control, and memory facilities plus the full 4 gigabyte direct address range of the VERSAbus system bus.

Benchmark 20, 020bug, VERSAbus and RAMbus are trademarks of Motorola.

Check ☐ C for information.

Get rid of the bits and pieces with all-in-one stepper drive.

It's linear, it's low-cost and it's uniquely capable of handling all the functions to directly drive sustained stepper motor currents up to 1/4 amp per phase without any extra power drivers.

It's the MC3479P and you can hang your entire disc drive, or similar stepper-motor-drive application right on it to cut costs, time and space.

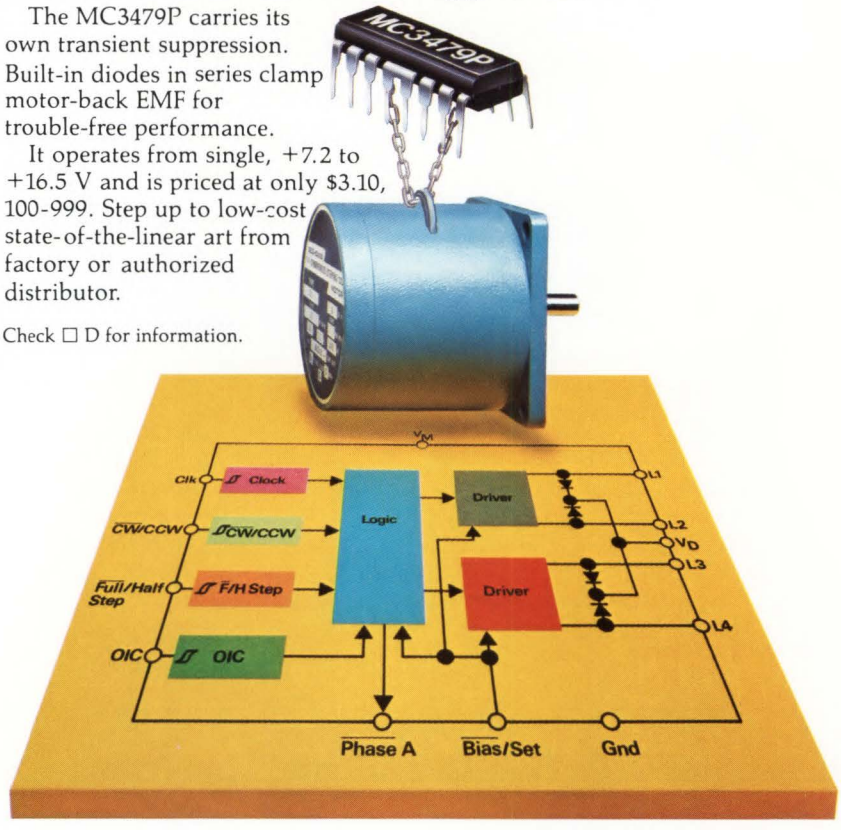
Optimized specifically for 2-phase (bipolar mode) steppers used in volume applications, the MC3479P package is a high (150°C junction) thermal dissipation version of the industry-standard 16-Pin DIP, chosen for ease of auto-insertion. Flexible operation controls include full/half step, CW/CCW and a high-impedance braking mode for high-speed micro-stepping.

All T^2L-compatible, logic control inputs are provided with 400 mV hysterisis for improved noise immunity. Control logic can be initiated to phase A and a phase A output status indication is provided for track zero indication or other similar applications.

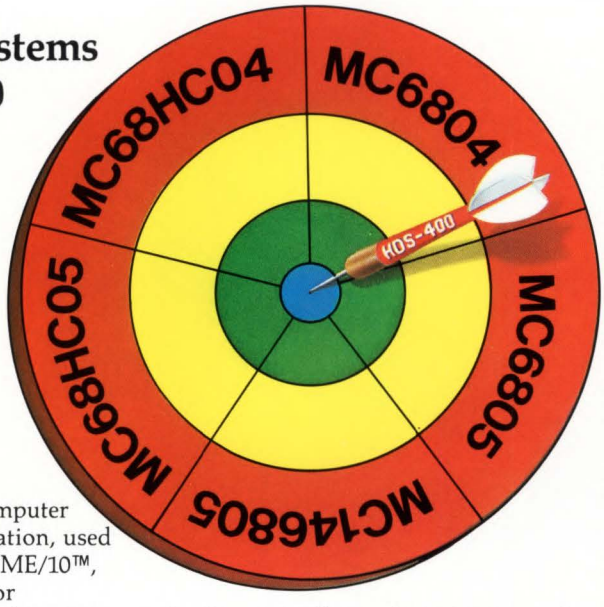
The MC3479P carries its own transient suppression. Built-in diodes in series clamp motor-back EMF for trouble-free performance.

It operates from single, +7.2 to +16.5 V and is priced at only $3.10, 100-999. Step up to low-cost state-of-the-linear art from factory or authorized distributor.

Check ☐ D for information.



Target your systems with HDS-200



The HDS-200 microcomputer hardware development station, used in conjunction with the VME/10™, EXORset®, EXORmacs® or EXORciser® software development system, or a personal computer, provides a complete hardware/software development system for the Motorola MC6804, MC68HC04, MC6805, MC68HC05, and MC146805 families of microprocessors.

The HDS-200 is a fully functional substitute for the selected MCU in the target system. By plugging the HDS-200 into the socket of the prototype hardware, it allows efficient testing of hardware as well as software debugging. It also supplies a powerful list of debugging commands. The easy-to-use, plain language commands enable the user to rapidly debug and integrate the target system and produce prototype systems.

By bringing the complicated hardware and software development processes together, it becomes economically feasible to test alternate design approaches in order to determine the best solution.

The HDS-200 has been designed to solve the problem of finding precise ROM patterns needed for optimum system performance by emulating the target MCU until its configuration has been fully proven. Changes and tests of the target configuration can be made quickly and easily.

The emulator can be applied and software run prior to availability of hardware. This allows an early start on the debugging process. As hardware changes occur, software updating and debugging is readily accomplished.

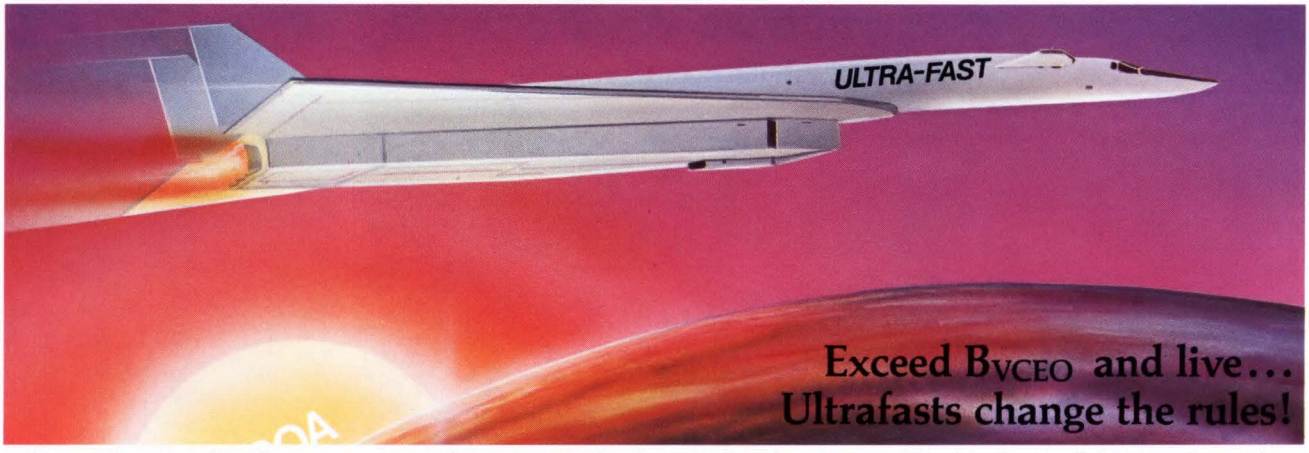
In providing systems integration and development, the HDS-200 provides real-time emulation of user code, sixteen prioritized breakpoints, a two-level help command and user-defined macro commands for quick execution.

The HDS-200 is compatible with the Motorola VME/10 host system and the EXORmacs, EXORciser and EXORset software development stations.

EXORmacs, EXORciser and EXORset are registered trademarks of Motorola. VME/10 and HDS-200 are trademarks of Motorola.

Check ☐ E for information.

We're on your design-in team.



Convention says bipolar power transistors can't switch above collector-emitter breakdown and last much longer than a microsecond or two.

Ultrafast rectifiers are sweeping that idea away, fast.

By using Ultrafasts as high-speed clamp diodes with sub-nanosecond recovery times, third-generation bipolars are switching rated currents from bus voltages up to bulk breakdown under test conditions. Safely.

A bipolar's sustaining voltage becomes of academic interest if transition turn-on occurs rapidly enough. And it does with Ultrafast rectifiers. Once turned-on, the ability of the transistor to sustain voltage above $B_{VCEO(sus)}$ is of little importance, since the objective is to reduce collector voltage as rapidly as possible. The only real concern is safe area. Nanosecond transitions avoid hotspotting phenomena because they just don't have time to develop. And without damaging hotspotting, bipolars can have considerably more capability than generally perceived. In fact, turn-on SOA up to collector-base breakdown, B_{VCEO}, is possible, and designable.

This can have a profound effect on conversion efficiency, cost and the relative merits of bipolars vs. other types of power semiconductors.

Not to mention improvement over "the old way" by a factor of 2, and perhaps more, in amount of power controlled, required base drive and switching speed.

And Motorola Ultrafasts have the specs to do it. The new 4 A, MUR870/880/890/8100 series of 700 to 1,000 V devices in economical, TO-220 packaging is ideal for today's big-power jobs in high-line switching power supplies, inverters, PWM motor controls, solenoid and hammer devices. They're also available in 1 A, axial-lead plastic.

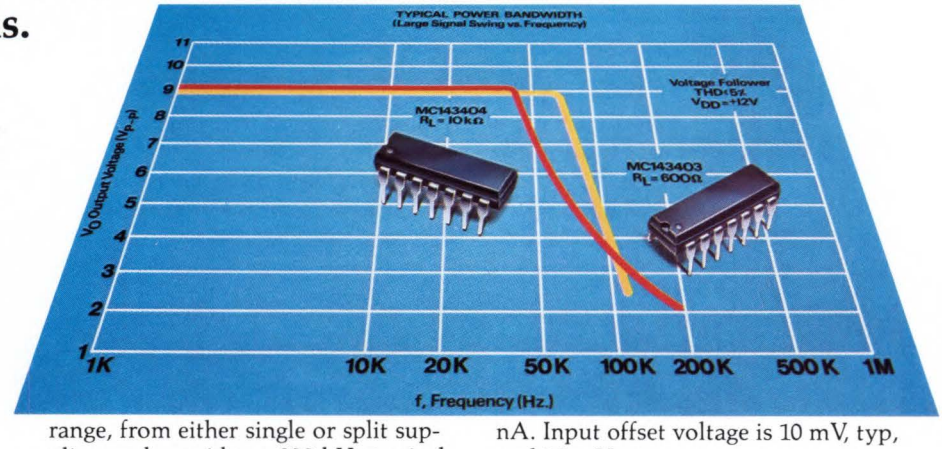
Less than 75 ns recovery times characterize the MUR130/140/150/160 family of 1 A units. Providing 300 to 600 V specs, they complement the MUR430/440/450/460, 4 A types, also in axial-lead.

And, the broadest lineup of its kind now extends to 200 A in the MUR20005CT/20010CT/20015CT PowerTap™ units. The sure-footed, labor-saving package design does away with variables in heatsinking, operates to 175°C and is easier, quicker and more convenient to install than equivalent DO-5s. Cooler, too.

We'll send you data sheets plus an eye-opening article reprint on what we found out about extending bipolar SOA with Ultrafasts.

Check ☐ F for information.

Low power is the difference in these CMOS Quad Line Drivers for telecomm applications.



Two new Motorola CMOS quad line drivers are electrically similar to the popular LM324 and MC3403, but there's a big difference between those standard operational amplifier types and our new MC143403/04.

Typically, the MC143403 draws a tiny 400 μA, and the MC143404 consumes a mere 1.5 mA.

Their characteristics make the MC143403 and 04 appropriate for a broad spectrum of industrial, consumer and instrumentation systems, but of all possibilities there is no question that they are ideal for low- and micro-power telecommunications systems....battery- or phone-line powered.

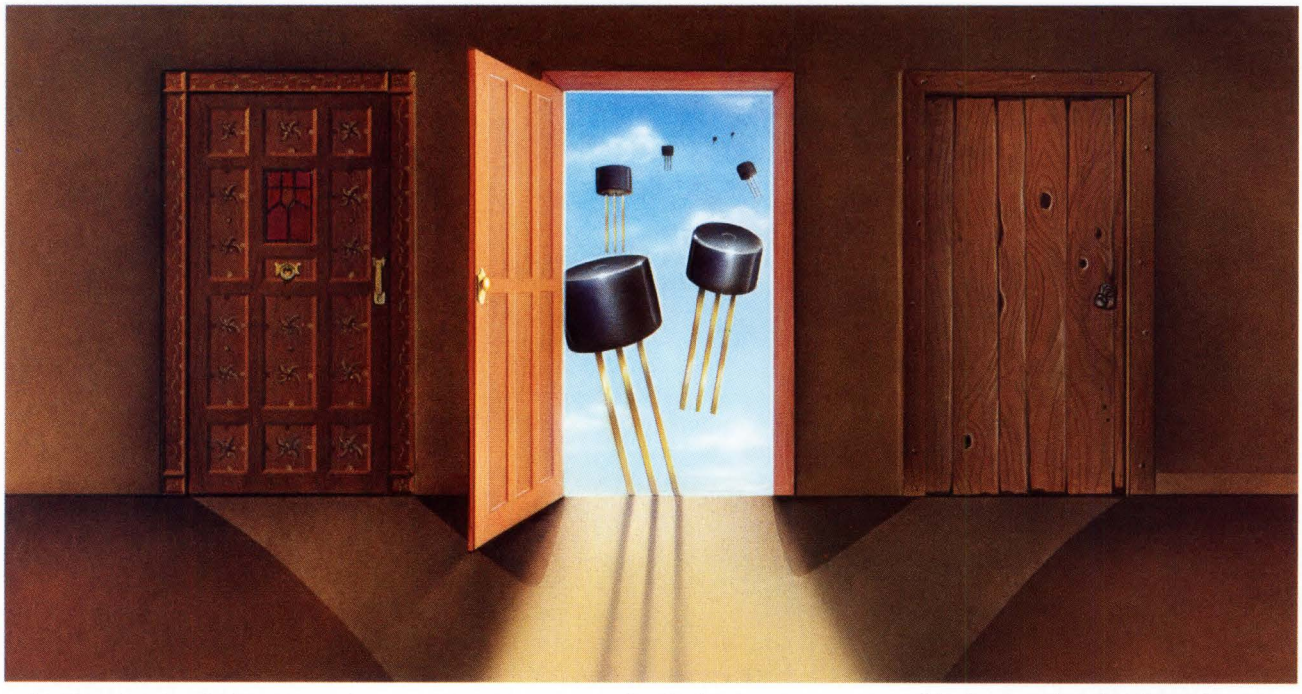
Both of these CMOS quad line drivers operate over a 4.75 to 12.6 V range, from either single or split supplies, and provide an 800 kHz typical small signal bandwidth. Four differential input op amps apiece give these devices true differential input stages.

Input impedance is a high 12 megaohms. Maximum input bias is 10 nA. Input offset voltage is 10 mV, typ, and 30 mV, max.

Whether you want samples or production quantities, you order, we deliver. Both devices are the same price of $1.47, plastic, and $1.64, ceramic.

Check ☐ G for information.

MOD-line fiber optics. Moderate price for moderate performance over moderate distance.



Moderation in all things — and therefore a wise choice for a large middle-ground of applications — characterizes these new fiber optics components.

The emitter/detector pair opens the door to typical 90 MHz performance at low prices for working distances up to 1/2 km, ideal for video transmission, digital computer peripheral interconnects, LAN and industrial controls.

Like standard TO-52 packaging, the small, rugged , plastic units fit into standard AMP, Amphenol, Deutsch, Radiall and similar connectors. Internal lensing enables efficient coupling to 100 micron or larger cable. The inexpensive cap has high transmission efficiency to IR and low to visible light; and the whole assembly costs less than half that of comparable, metal-and-glass, TO-52 setups.

The MFOE3200 850 nm LED has a 250 micron spot and launches up to 40 μW into 100/140 fiber at an If of 50 mA. Distances up to 1,500 feet are easily obtained with 200 micron, NA = .4 cable.

The MFOD3100 PIN detector loafs along with a 200 MHz analog bandwidth. It's compatible with all IREDs including the MFOE3100 in the same efficient plastic package.

Moderate prices brighten the eye: Just $4.58 for the MFOE3200 LED, and $4.58 for the MFOD3100 detector, 1K up.

Check ☐ H for information.

Volume-production levels of fast 16K SRAM cranked to new highs.

The 2016H is the fastest 2K x 8 SRAM available, but has not always been available in the desired time frames due to the limited number of manufacturers able to offer it.

To help alleviate this shortfall, Motorola has cranked run rates of the 50 and 70 ns versions to the highest levels ever. Now these MCM2016H 16K SRAMS are available through distribution as well as from the factory.

And, in case you may have missed it, be aware that in addition to the industry standard 600-mil wide dual in-line 24-pin packages, Motorola offers a space-saving 300-mil wide package with all the same pinouts and electrical specs inside. It saves a lot of board space.

Reviewing the part, the MCM2016H is fabricated in our silicon-gate HMOS II process to achieve the low power dissipation of 20 mA in standby, 120 mA active, and access times as low as 45 ns at the same time. The RAM stays in the power-saving standby mode as long as Chip Enable, which controls power down, is held high. Because the 2016H is fully static, no clocks or timing strobes are required.

Check ☐ J for information.

Suppress transients and prices with low-cost, TO-220 zeners.

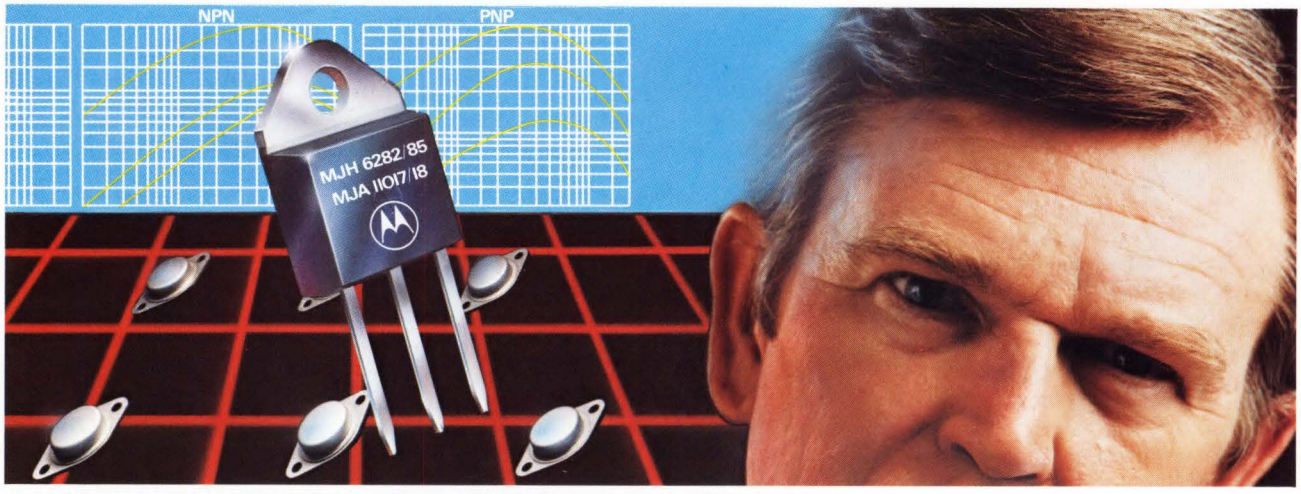
Throttle those surges, spikes and high-dollar demands of expensive DO-4s with what Motorola's become famous for — zener diodes and TO-220 packaging.

Our family of 10W and 50W MZT-series zener diodes give you everything an equivalent stud package does, except the high price.

All you have to do is think of the $5-$7 1N- number in stud packaging, translate to an MZT- prefix for these new TO-220s, and you've got 600 to 1,500W of peak power protection for sensitive communications systems, numerical and process controls, medical equipment, business machines, power supplies and anywhere else for as little as 75¢.

All the rest stays the same: 3.9 V to 200 V ranges, silicon oxide passivated junctions, low zener impedance, fast response, high heat dissipation and the knowledge you're receiving the highest quality and lowest cost in zener diodes. From Motorola, of course.

Check ☐ K for information.



MJH6282/11017 bipolar Darlington TO-218 series unique alternative to TO-3.

They're the first in TO-218 packaging to take advantage of what everyone knows is great about plastic TO-218s—lower cost and easier installation. And what's great about bipolar Darlingtons—Motorola sourcing.

It makes sense to save space, cost and time these days with PCB real estate becoming dearer and dearer.

And you can with the MJH- series of NPN/PNP complementary Darlingtons offering up to 160 W of power dissipation, replacing the old reliable, but more costly and hard to mount TO-3 in many sockets. You'll come out even in performance but way ahead in costs.

Simple, easy to design with and proven reliable, the growing popularity of the TO-218 power package will get its biggest boost from these top performers. They offer orders of magnitude higher gain than discretes, as high as 18,000 at 10 A, switch inductive loads in nanoseconds, operate to 3.75 kVA RBSOA, handle up to 20 A continuous and cost as little as $2.50 each.

Pricing ranges from $2.50 to $3.50 for the MJH6282 series and $4.40 to $6.32 for the MJH11017 series—both in 100-up quantities.

Complementary Darlingtons afford the equivalent of 10 circuit components in two packages. And being complementary you can use them in pairs in audio amplifiers.

And go from milliamperes to amperes directly, compatibly, easily using IC-driven supplies.

Driver, output device, base-emitter resistors and output diode are all on one monolithic chip in one package.

And more efficient packaging equals lower price paid. Less is more with Motorola TO-218 Darlingtons.

Check ☐ L for information.

Support MC68020 Development with HDS-400

The HDS-400™ microprocessor hardware/software development station provides low-cost emulation for the complete line of Motorola M68000 microprocessors including the 32-bit MC68020 MPU. The HDS-400, used in conjunction with a Motorola EXORmacs® development system, VME/10™ microcomputer system or a DEC VAX™ computer, provides tools for debugging and analyzing microprocessor system performance for both hardware and software.

The MC68020 emulator/analyzer uniquely combines the HDS-400 emulator module and the BSA personality module functions into a single enclosure, with a single cable/probe assembly to connect to the target system.

In addition to supporting higher clock speeds, the MC68020 emulator/analyzer gives unrestricted use of the full 4G-Byte available address space. Up to 16 breakpoints can be set in target RAM or emulation memory, even while the 4 longword instruction/data cache in the MC68020 is enabled.

An optional real-time bus state analyzer (BSA) may be integrated into the HDS-400, with personality modules to support each processor in the emulator system. Complex breakpoints and operation speeds up to 20 MHz with one wait cycle are supported by the real-time bus state analyzer with the MC68020 emulator/analyzer module.

With a processor-specific emulator, the critical functions and locations within the microprocessor can be observed, greatly enhancing the efficiency of system debugging and shortening the product development cycle. Emulators for the MC68000, MC68008, MC68010 and the MC68020 allow designers access into the memory, CPU and registers of the microprocessor for debugging purposes.

The HDS-400 provides emulation for clock speeds of 12.5 MHz for MC68000 MPUs, 8 MHz for the MC68008 and the MC68010 and 16.67 MHz for the MC68020 allowing you to get to market faster with faster speeds.

Added MC68020 development ability proves that the HDS-400's versatility protects against obsolescence.

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Check ☐ M for information.

MPX2050 transducer takes own temperature, keeps calm under pressure.

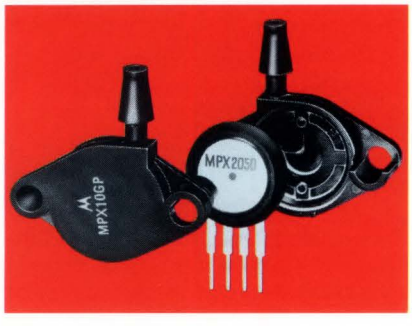
Stability without complexity best sums up the advantage of the unique new 0-7.5 psi MPX2050 pressure sensor family from Motorola.

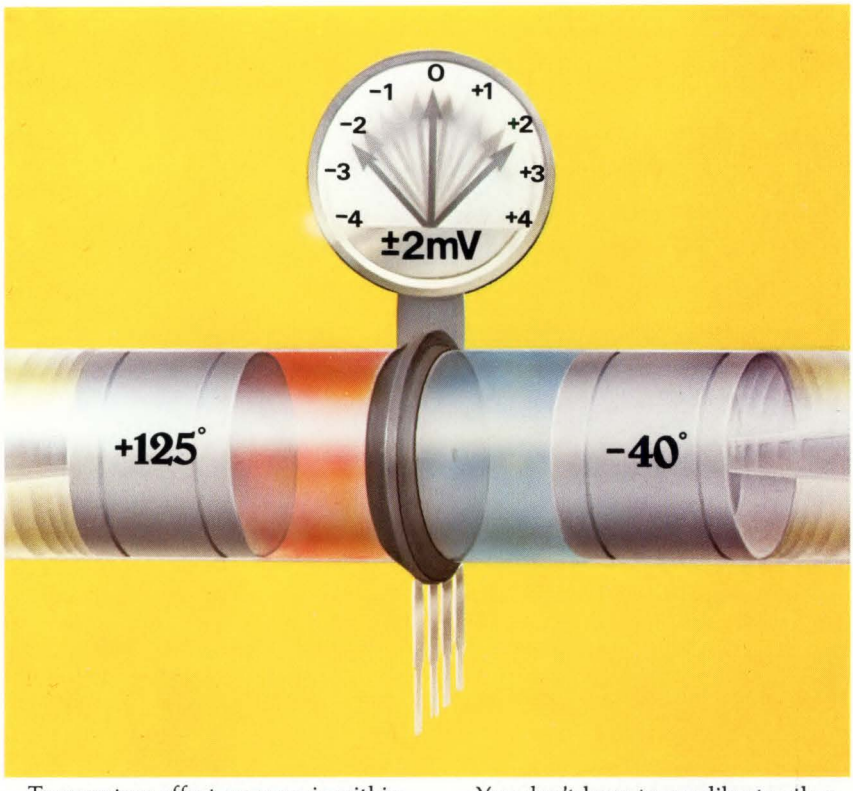
Offering the industry monolithic, on-chip temperature compensation for the first time, the silicon piezoresistive transducer offers the designer an all-in-one chip combining computer-controlled, ion-implanted, laser-trimmed resistors with the high linearity, accuracy and ease-of-use Motorola's MPX- family has become renowned for.

Result of all this technology: an easier, lower-cost design job for you.

Stable and accurate, the MPX2050 utilizes the same, single-element, design used extensively in automotive, industrial and medical applications. Nominal output is set at 40 mV with 10 V supplied, more than sufficient for driving external measurement and circuitry.

Variation of pressure offset over temperature is just ± 1 mV.





Temperature effect on span is within 2% of full scale over a −40° to +125° C operating range.

You can snap it into the economical, Motorola-developed, pressure-port housing that provides you with mounting flexibility and barbed hose connections.

Plus it's easy to mount (standard, 100-mil spacing), easy to connect (hoses slip right on), easy to customize (build your own ports), easy to measure (up to 90 mV output) and easy to apply. Easy to forget, too — years of use with no maintenance.

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Check ☐ N for information.

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Motorola Reports

Please send me information on:

- ☐ A. MCM6257 256K DRAM
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- ☐ C. Benchmark 20
- ☐ D. MC3479P stepperdrive
- ☐ E. HDS-200 development station
- ☐ F. Ultrafast rectifiers
- ☐ G. MC143403/04 Quad Line Drivers
- ☐ H. MOD fiber optics
- ☐ J. MCM2016H SRAM
- ☐ K. TO-220 Zeners
- ☐ L. Bipolar Darlingtons
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CIRCLE 13

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U.S. MEETINGS

IEEE First International Conference on Office Automation, Dec. 17–19. New Orleans Hilton, New Orleans, La. IEEE First International Conference on Office Automation, c/o Dr. Donald Kraft, Department of Computer Science, Louisiana State University, Baton Rouge, La. 70803; (504) 388-1495.

1985 International Winter Consumer Electronics Show, Jan. 5–8. Las Vegas, Nev. Dennis Corcoran, CES, 2001 Eye St. NW, Washington, D.C. 20006; (202) 457-8700.

PC Fab Expo '85, Jan. 8–10. Sheraton Twin Towers Hotel, Orlando, Fla. Julia Wilson, PMS Industries, 1790 Hembree Road, Alpharetta, Ga. 30201; (404) 475-1818.

Automated Test Equipment West Conference (ATE), Jan. 14–17. Anaheim Convention Center, Anaheim, Calif. Morgan-Grampian Expositions Group, 2 Park Ave., New York, N.Y. 10016; (212) 340-9780.

Caldon West '85, Jan. 14–17. Anaheim Convention Center, Anaheim, Calif. Morgan-Grampian Expositions Group, 2 Park Ave., New York, N.Y. 10016; (800) 782-0009.

1985 Measurement Science Conference, Jan. 17–18. Marriott Hotel, Santa Clara, Calif. Darlene Diven, Lockheed Missiles and Space Co., PO Box 3504, Sunnyvale, Calif. 94088; (408) 756-0270.

Uniform, Jan. 21–25. Infomart, Dallas, Texas. Pemco, Inc., 2400 E. Devon Ave., Suite 205, Des Plaines, Ill. 60018; (800) 323-5155.

1985 Society for Computer Simulation (SCS) Multiconference, Jan. 24–26. Bahia Hotel, San Diego, Calif. SCS, PO Box 2228, La Jolla, Calif. 94038; (619) 459-3888.

Communication Networks Conference and Exposition, Jan. 28–31. Washington Convention Center, Washington, D.C. Louise Myerow, CW/Conference Management Group, 375 Cochituate Road, PO Box 880, Farmingham, Mass. 01701; (617) 879-0700 or (800) 225-4698.

4th International Symposium on Semiconductor Processing. Jan. 28–31. San Jose, Calif. Dinesh Gupta, Siliconix Inc., 2201 Laurelwood Road, Santa Clara, Calif. 95054; (408) 988-8000 or Thomas Kochaba, ASTM, 1916 Race St., Philadelphia, Pa. 19103; (215) 299-5560.

Mini/Micro West, Feb. 5–7. Anaheim Hilton Exposition Center, Anaheim, Calif. Electronics Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

Conference on Optical Fiber Communication(OFC '85), Feb. 11–13. Town and Country Hotel, San Diego, Calif. Optical Society of America, 1816 Jefferson Place NW, Washington, D.C. 20036; (202) 223-8130.

IEEE International Solid-State Circuits Conference, Feb. 13–15. New York Hilton Hotel, New York, N.Y. Lewis Winner, ISSCC, 301 Almeria, Coral Gables, Fla. 33134; (305) 446-8393.

Integrated Machine Loading/Material Handling Systems Seminar, Feb. 19–21. Holiday Inn Livonia-West, Detroit, Mich. John R. McEachran, SME, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, Ext. 382.

Automated Design and Engineering for Electronics Conference and Exhibition (ADEE), Feb 26–28. Anaheim Hilton and Towers, Anaheim, Calif. Cahners Exposition Group, Cahners Plaza, 1350 E. Touhy Ave., PO Box 5060, Des Plaines, Ill. 60018; (312) 299-9311.

Nepcon West '85, Feb. 26–28. Convention Center, Anaheim, Calif. Nepcon West '85, 1350 E Touhy Ave., Des Plaines, Ill. 60018; (312) 299-9311.

American Institute for Design and Drafting (AIDD) Exposition, March 3–8. Albert Thomas Convention Center, Houston, Texas. Philip Nowers, AIDD National Headquarters, 901 N. Washington St., Suite 509, Alexandria, Va. 22314; (703) 548-1263.

(continued on p. 29)

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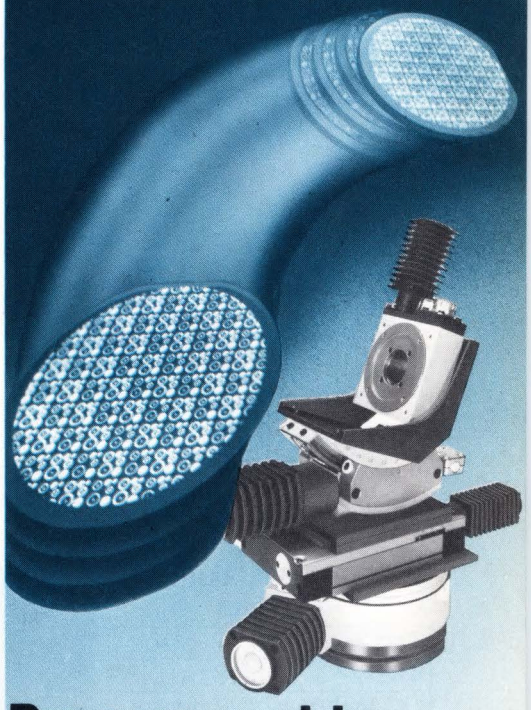

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CIRCLE 15

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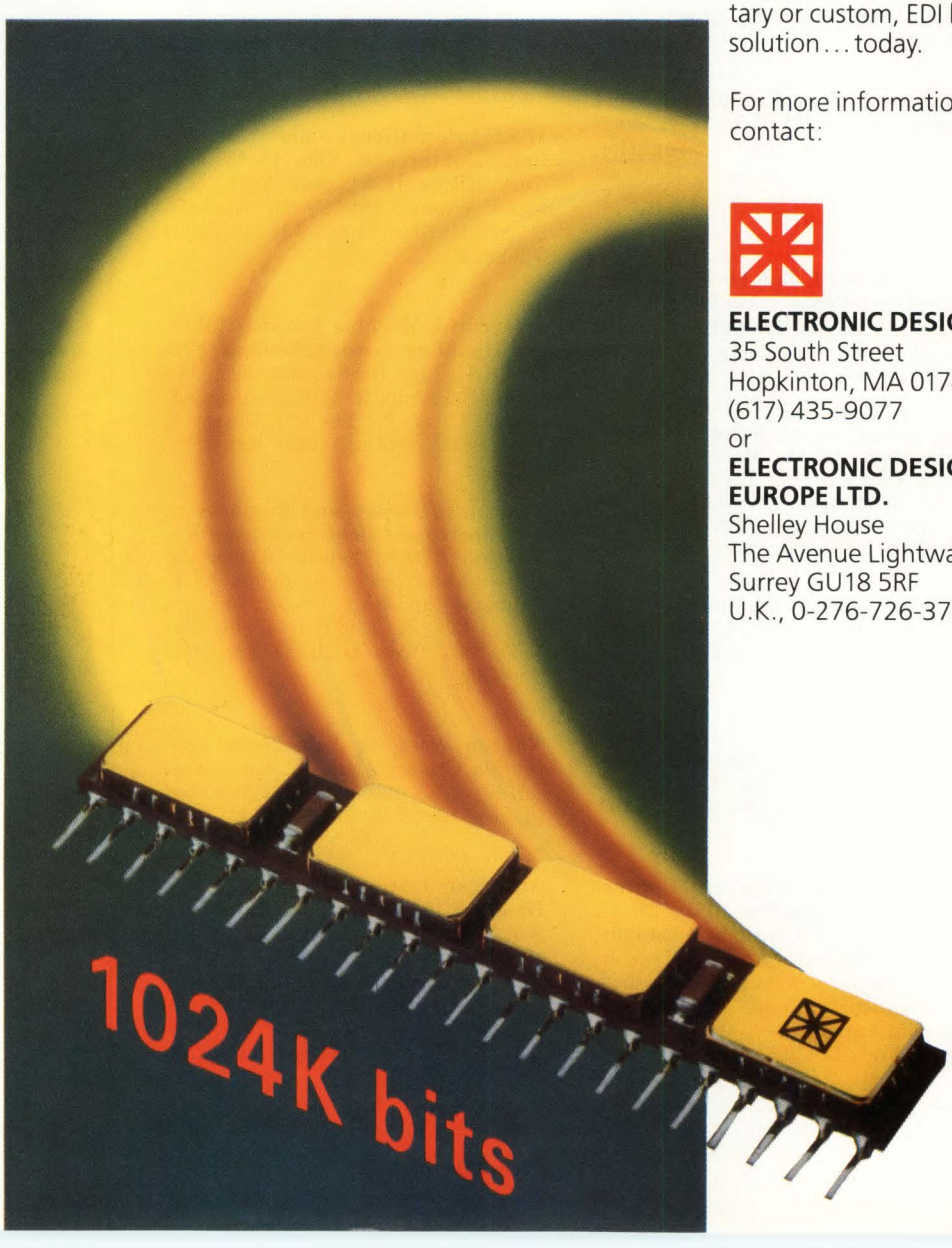

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U.S. MEETINGS

(continued from p. 27)

Interface '85, March 4–7. Georgia World Congress Center, Atlanta, Ga. The Interface Group Inc., 300 First Ave., Needham, Mass. 02194; (617) 449-6600.

Southcon '85 and Mini/Micro Southeast, March 5–7. Georgia World Congress Center, Atlanta, Ga. Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; (213) 772-2965.

Integrated Services Digital Networks Exposition (ISDN '85), March 6–8. Bally's Park Place Casino Hotel, Atlantic City, N.J. Joan Barry, Information Gatekeepers Inc., 214 Harvard Ave., Boston, Mass. 02134; (617) 232-3111.

1985 ACM 13th Annual Computer Science Conference (CSC), March 12–14. New Orleans Marriott Hotel, New Orleans, La. Della T. Bonnette, Computing & Information Services, University of Southwestern Louisiana, Lafayette, La. 70504; (318) 231-6306.

Picosecond Electronics and Optoelectronics Meeting, March 13–15. Hyatt Lake Tahoe, Incline Village, Nev. Optical Society of America, 1816 Jefferson Place NW, Washington, D.C. 20036; (202) 223-8130.

International Computer and Telecommunications Conference (Comtel '85), March 18–20. Infomart, Dallas, Texas. Comtel '85, 5080 Spectrum Drive, Suite 707E, Box 17, Dallas, Texas 75248; (214) 631-6482.

Robotic End Effectors: Design and Applications Seminar, March 19–20. Holiday Inn Livonia-West, Livonia (Detroit), Mich. John McEachram, SME, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, ext. 382.

Second Annual International Conference on Artificial Intelligence for Robotics, March 21–22. Stouffers Concourse, Crystal City, Arlington, Va. Dr. Diener, IIT Research Institute, 10 W. 35th St., Chicago, Ill. 60616; (312) 567-4376.

1985 Trends and Applications Conference, May 21–22. Sheraton NW Washington, Silver Spring, Md. Mark Skall, National Bureau of Standards, Room A265, Technology Building, Gaithersburg, Md. 20899; (301) 921-2431.

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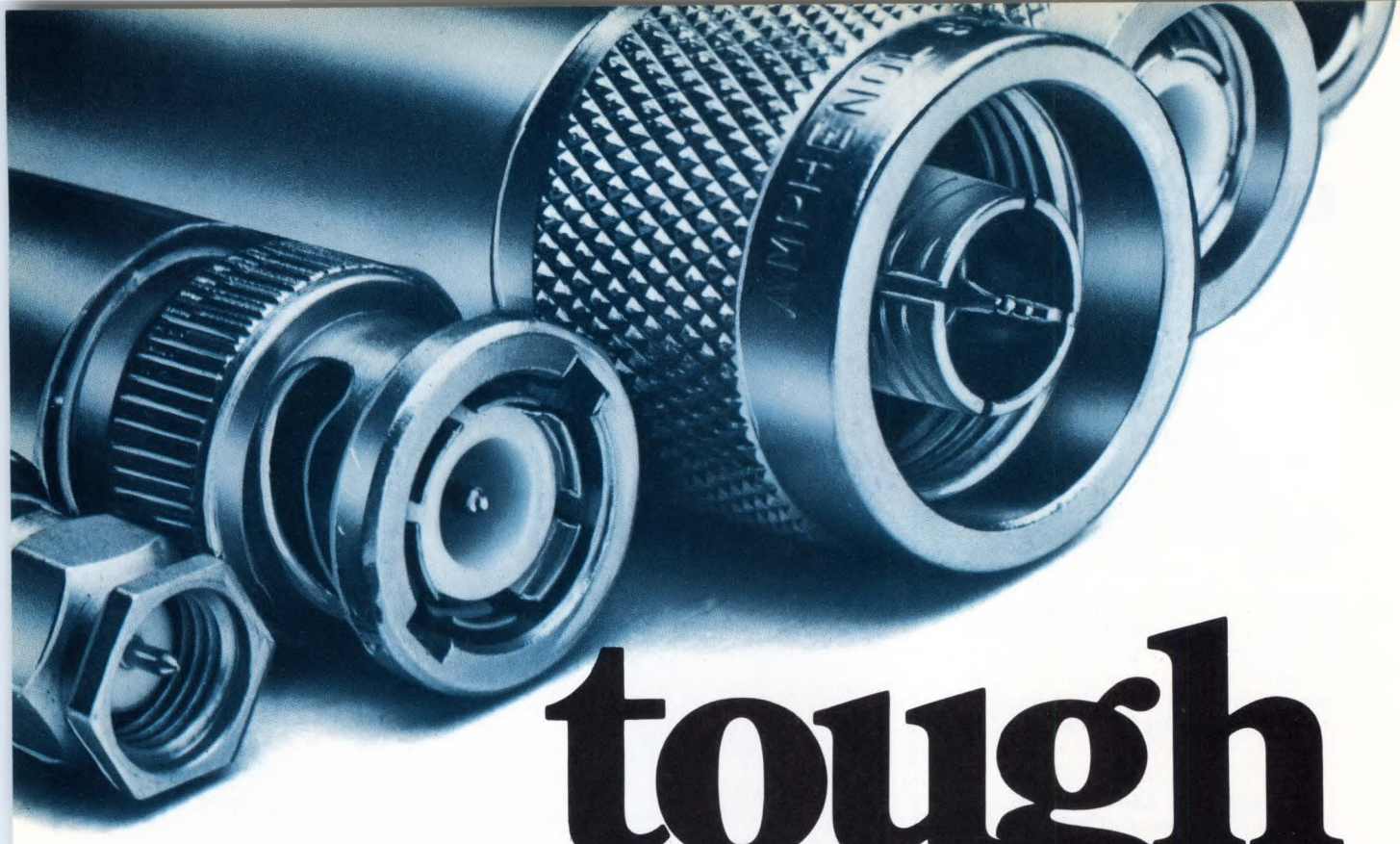
CIRCLE 17



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		DC–1000	1000–1500	DC–1000 MHz	1000–1500 MHz
DC-1500 MHz	±0.3	0.6	0.8	1.3	1.5

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■ denotes 75 ohms; add –75 to model no.
● denotes 50 ohms

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2	●			
3	●	●■	●	●
4	●			
5	●			
6	●	●■	●	●
7	●			
8	●			
9	●			
10	●	●■	●	●
12	●			
15	●			
20	●	●■	●	●
30	●	●	●	●
40	●	●	●	●

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CIRCLE 18

C 92 REV. A

PERSONALLY SPEAKING

Thin-film technology will redefine limits of Winchester disks

Thin-film technology may well be the best way to stay the growing appetite for external memory that plagues personal computers, high-resolution graphics workstations, local network file servers, and the host of other equipment that works with hard disks. Thus developing new approaches to disk coatings and head assemblies are top priorities for computer peripheral designers. Indeed, within the next two years we'll see many 5¼- and 3½-in. disks turn from their current oxide coatings to sputtered or plated thin films. Further, thin-film heads by then will have begun to replace their conventional ferrite counterparts. Estmates have it that by the decade's end thin-film technology will drive disks' areal density from a present high of 10 Mbits/in.^{2} to a whopping 50 Mbits/in.^{2}—or more.

As always, there is at least one fly in the ointment: Thin-film deposition—particularly sputtered coating—is in short supply. Moreover, thin-film heads are notoriously difficult to mass-produce. Consequently, the changeover will have to be taken in two steps.

The initial move will be seen in coatings, but it's still unclear whether plated or sputtered surfaces will capture the lion's share of the new designs. Based on many of the drives scheduled for 1985, sputtering looks to be taking the lead. Plating is a wet process, so its yield is inherently lower than sputtering's. And sputtering appears to be the more controllable of the two approaches.

Hewlett-Packard, working with a 3½-in. 10-Mbyte Winchester disk, found that sputtering produced higher and more consistent yields. On the other hand, NEC, which has been going with plating for many years, says it is still counting on mixing plated coatings and thin-film heads in its 1986 Winchester drives.

The second phase of the conversion, which should be well under way by 1988, demands that several challenges be met. The titanium carbide wafers that are used in thin-film heads are more difficult to work with than the silicon traditionally employed for semiconductors. All of the head's magnetic elements—coils, head arm, and slider—must be laid down on the wafer. Finally, very tight control of the head gap is crucial.

The move to thin-film technology carries another benefit: It guarantees that magnetic disks will be with us for some time to come. They have already survived challenges from alternative technologies—most notably magnetic bubbles and charge-coupled devices. And other developments should lock up their future, such as vertical recording and the work proceeding in VLSI to consolidate all of the electronic control circuitry.

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Martin Gold

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As for your schematic, it can be hand-drawn on paper or generated by an engineering work station. TI's standard-cell library is supported on leading work stations, such as Daisy, Mentor, and Valid, as well as on several PC systems. And TI supplies the translation software for automatic generation of the TI design-description language.

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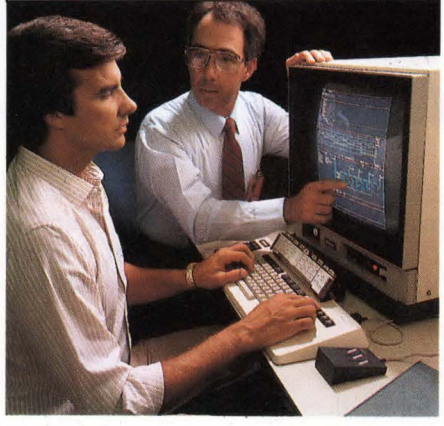

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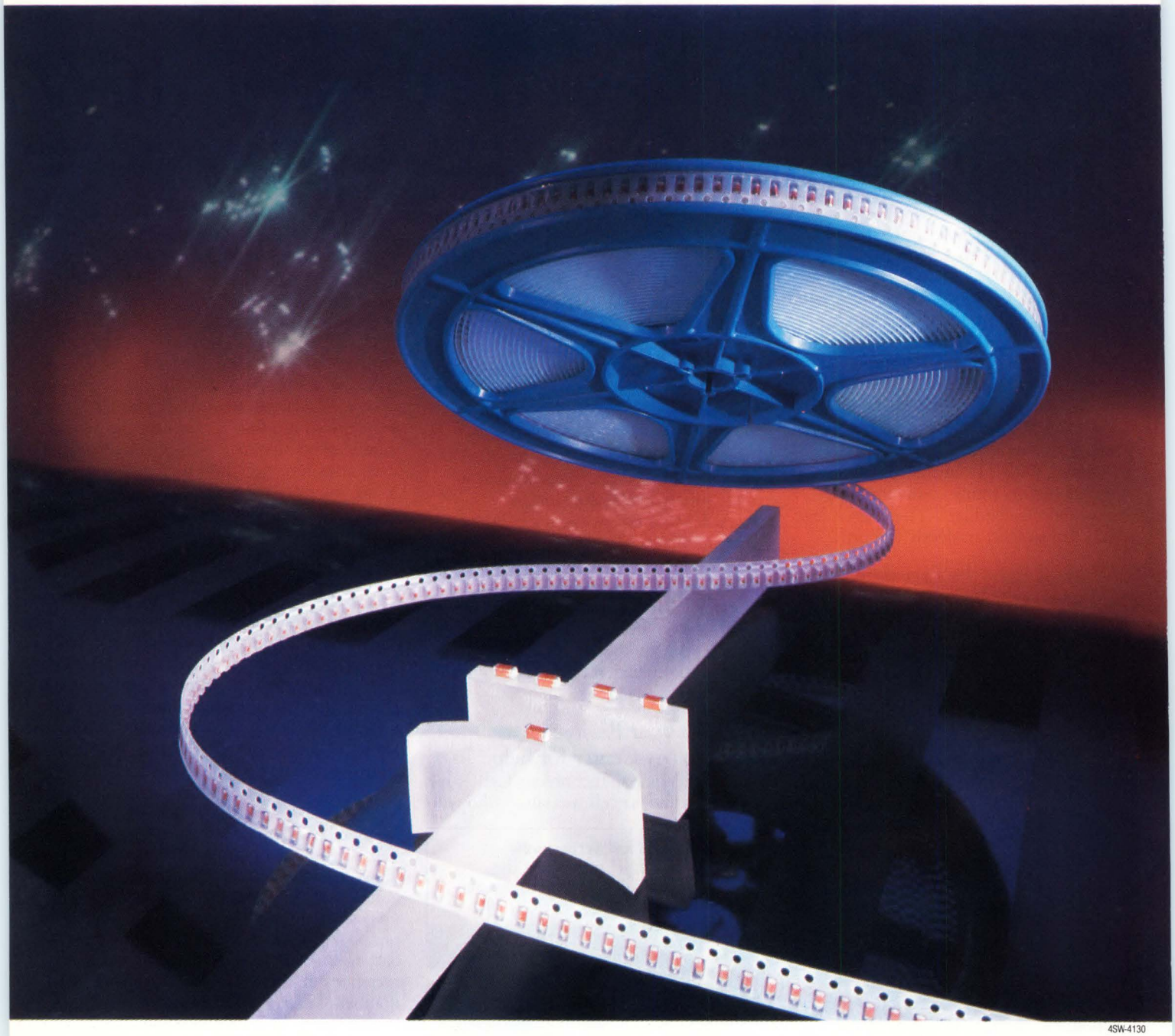

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CIRCLE 19

NEWSPULSE

32-bit CMOS microprocessor chalks up 5 MIPS

The new generation of 32-bit microprocessors will take a giant leap in speed with a CMOS chip that draws on a proprietary multitasking, multiprocessing architecture to execute an unprecedented 5 million instructions/s. Now in development at Hitachi Ltd.'s Central Research Laboratories (Tokyo), the chip, built with 1.3-μm design rules, packs demand-paged virtual-memory management, ROM, and RAM into 6.5 by 5.9 mm. Besides being code-compatible with the 68000–and as such, with existing 68000-based peripherals–it will run under Unix 4.2 and accept programs written in Pascal, C, and Fortran. Initial specifications for the chip, which will be housed in a surface-mounted package with more than 100 pins, spell out a clock rate of 20 MHz, a cycle time of 50 ns, and power consumption of 500 mW. First samples should appear some time in 1986.

Custom designs and fuse-programmable logic team up

Programmable logic devices normally do not fit into custom circuit design, but the combination of a high-level logic programming language and a sophisticated engineering workstation changes that situation. Valid Logic Systems Inc. (San Jose, Calif.) has bolstered its SCALDsystem I, II, and IV workstations with logic design software based on the Abel language, which was originally devised by Data I/O Corp. (Redmond, Wash.) for programming all types of fuse-programmable logic. Workstation users can now design fuse maps for programmable logic devices at the same time they enter the schematic, verify the timing, and simulate the logic of complex circuits. Abel actually does the job of compiling Boolean equations, truth tables, and state diagrams into fuse maps for any type of programmable logic, including PALs and PROMs.

½-in. tape committee tackles serial recording

Some of the confusion over ½-in. tape cartridges may be resolved when an ad hoc standards committee rolls into action. As part of its charter, the HI/TC working group will define a serial recording format, as well as a device interface, for tape drives using the recently released IBM 3480 cartridge. The parallel recording scheme now used by the IBM drive is considered by some to be impractical for small computer systems. Among the companies represented in the committee are Computer Peripherals (a subsidiary of Control Data), Kennedy, Pertec Peripherals, Wangtek, and Xebec.

First silicon for transputer gets a complete checkup

The 32-bit transputer chip has not only seen the light of day but is now being tested. The T424, which is 85 mm^2 and contains more than 250,000 transistors, is getting the once-over at Inmos Corp. (Colorado Springs, Colo.). The company plans to have an evaluation board ready by midyear, by which time a full-fledged software development system—including compiler, debugger, and

NEWSPULSE

operative system—should be ready. Fabricated with a 2-μm twin-well CMOS process, the chips internal memory has a cycle time of 50 ns. The transputer's sister chip, the 16-bit T222, is expected to appear in silicon within a few months.

DOD's software engineering institute finds a home

The U.S. Department of Defense's STARS (Software Technology for Adaptable Reliable Systems) project has taken an important step with the choice of Carnegie-Mellon University (Pittsburgh, Pa.) as the academic mentor for its proposed software engineering institute (ELECTRONIC DESIGN, March 3, 1983, p. 49). As an essential component of the STARS initiative, the institute will develop a showcase software design environment. Niko Haberman, who presides over Carnegie-Mellon's computer science department, is expected to serve as the institute's acting director.

Ada compiler for Unix, Ultrix systems makes the grade

Following an exhaustive series of tests, the first commercial Ada compiler for the VAX-11/700 series has been validated to comply with MIL-STD-1815A (identical to the ANSI Ada specification). The compiler, developed by Verdix Corp. (McLean, Va.), is meant for 11/700s running under Unix 4.2 BSD or Digital Equipment's Ultrix operating system. It was tested on a VAX—fitted with virtual memory—that executes 1 million instructions/s. The compiler processed about 1000 Ada statements a minute and cut through compiled code at 20,000 statements a minute. To facilitate developing programs, the compiler comes with library maintenance utilities, an error processor, a prelinker, and a symbolic debugger. The whole package, dubbed VADS (Verdix Ada Development System), needs about 1 Mbyte of physical memory to turn in its best performance.

Occam compiler works in Pascal machines

Moving into mainstream computing, a single-pass Occam compiler produces up to 2000 lines of code per minute on any computer that can compile Pascal. The recursive program, developed by researchers at Brunel University (Uxbridge, Middlesex, England), compiles p-code for a stack machine. An interpreter then runs that code to simulate concurrent execution of up to 64 processes, switching from one process to another after every Occam statement. The compiler and interpreter both are written in Pascal.

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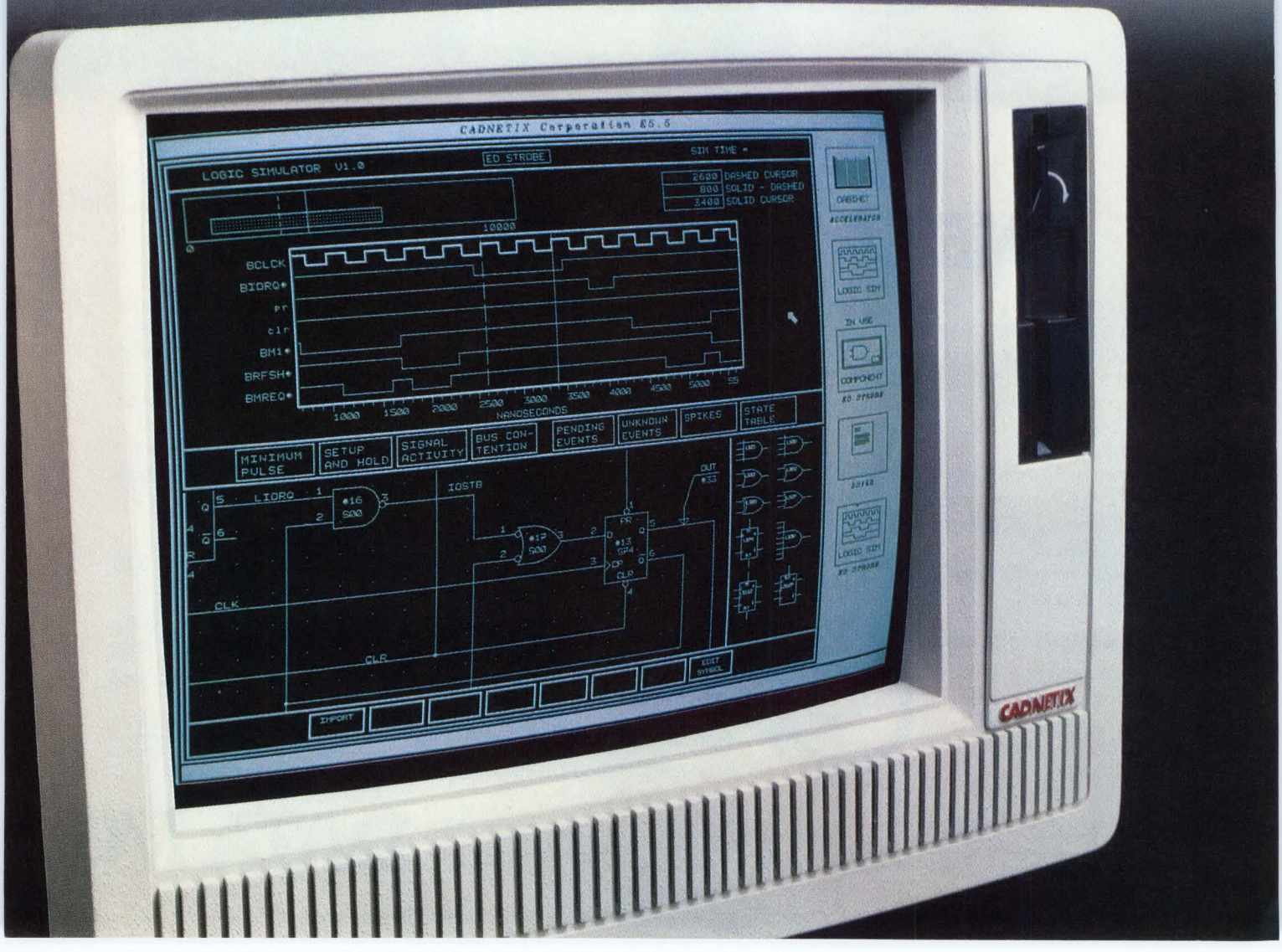

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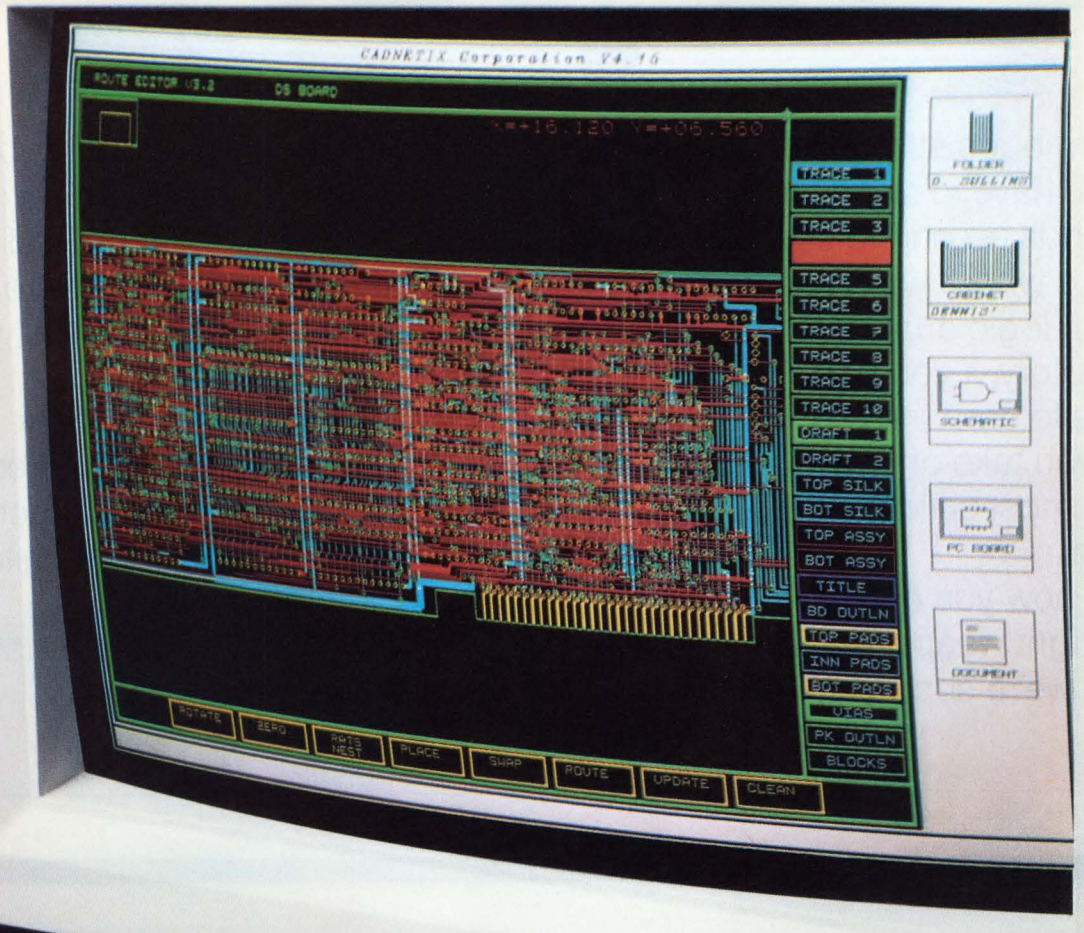

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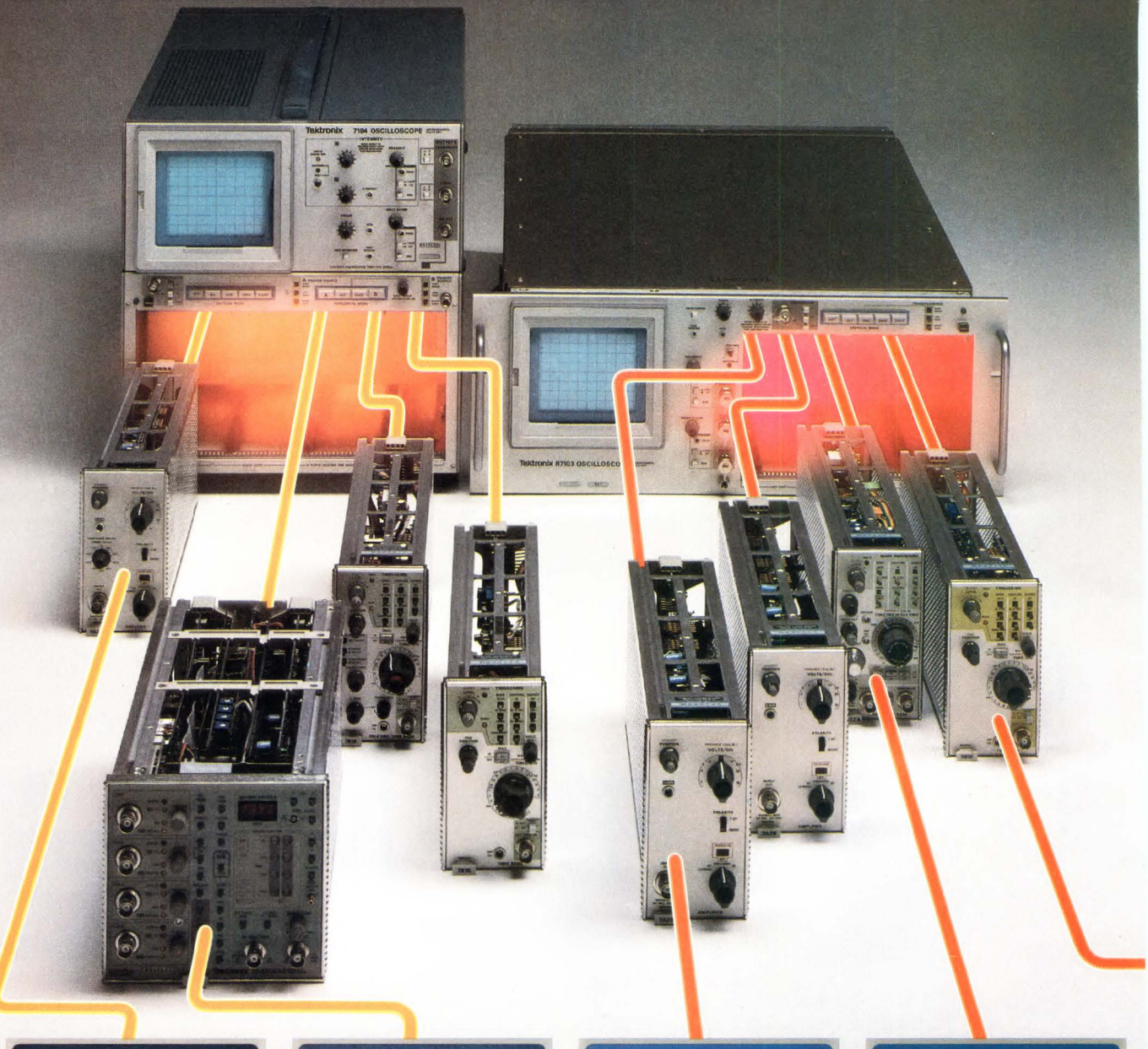
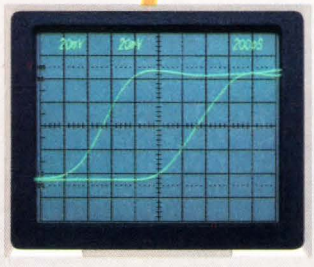
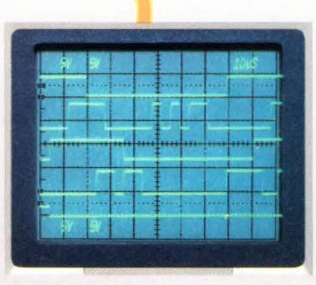
TEK 7104/R7103 OSCILLOSCOPE

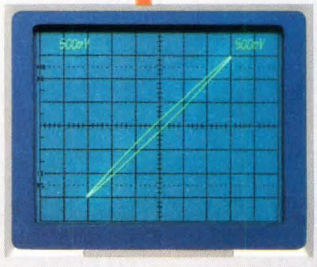




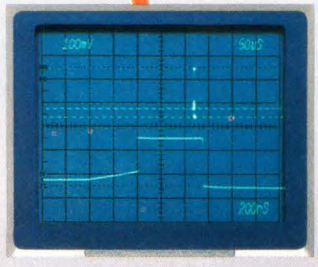
Precise Time Measurements —Variable signal delay permits display of true time relationship between 2 signals. **System:** 7104 with two 7A29 1 GHz Amplifiers and 7B15Δ Delaying Time Base.



Logic Triggering—displays digital signals in true analog form for high-resolution time and amplitude measurements. **System:** 7104 with 7A42 Logic-Triggered Vertical Amplifier.



X-Y Phase Measurements—Phase matching to 250 MHz enables direct, wide bandwidth phase shift measurements with high degree of accuracy. **System:** R7103 with two 7A29 1 GHz Amplifiers.



Microchannel Plate CRT—normalizes intensity so both low and high rep rates can be viewed simultaneously. **System:** R7103 with 7A29 1 GHz Amplifier, 7B92A Dual Time Base.

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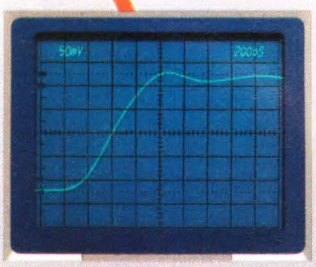

Single Shot Measurements —unmatched writing rate of 20 cm/ns provides bright display even at 200 ps/div. **System:** R7103 with 7A29 1 GHz Amplifier, 7B10 Time Base.

CIRCLE 23

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Harris Telecom ICs Product Summary

Part Number	Description	Highlights
HC-5502A	SLIC	Ring generator referenced to ground
HC-5504	SLIC	Ring generator referenced to negative battery supply
HC-5508	SLIC	Reconfigured and enhanced version of HC-5504
HC-5510/11	PCM CODECs	μlaw/A-law coding with signaling capabilities
HC-5512/12A	PCM Filters	Exceed all D3/D4 CCITT specifications
HC-5512D	PCM Filter	MIL spec
HC-5554/57	CODEC/Filters	μlaw/A-law COMBOs
HC-5541A	Dialer	Pulse-tone dialer
HC-55536/64	CVSD	Real-time speech processors
HF-10	UAF	Univ. Act. Filter, MIL Temp.

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CIRCLE 24

NEWSFRONT

Oxide isolation process builds RAM controller chip that needs no wait states

Besides obvious benefits in throughput, an advanced controller chip works with moderate-speed dynamic RAMs.

With microprocessor systems clipping along at 10 MHz or more, memory subsystems are forced to keep pace. Reaching those speeds without incurring wait states usually demands the use of high-speed components; both the dynamic RAMs and the controller logic. Now a merger between oxide isolation and clever design methods changes that: Together they produce a controller chip that operates at 10 MHz with no wait states. Moreover, the controller does not need dynamic RAMs that cycle blazingly fast; instead it can operate with cycle times of 150 ns, thus lowering the overall cost of the memory subsystem.

To reach such performance levels, National Semiconductor Corp. (Santa Clara, Calif.) entirely revamped the junction-isolation bipolar process with which it built its earlier 8409 dynamic RAM controller. The new process, based on oxide isolation, uses emitters that are about 70% smaller than those in the earlier process. Consequently, it produces transistors that occupy an area of 1.25 mils^2—about ½ the area of the junction-isolated transistors.

A washed emitter in the new structure eliminates any isolation spacing in the emitter region (see the figure). Junction isolation schemes usually insert a space to avoid emitter-to-base shorts when the metal contacts to the emitter are deposited. The oxide isolation approach turns the entire emitter into a contact, thus permitting the emitter region to be much smaller. Additionally, the scaling of the emitter is allowed because of self-aligned masking of the contact region to the emitter, which presents any misalignment.

Lower capacitance

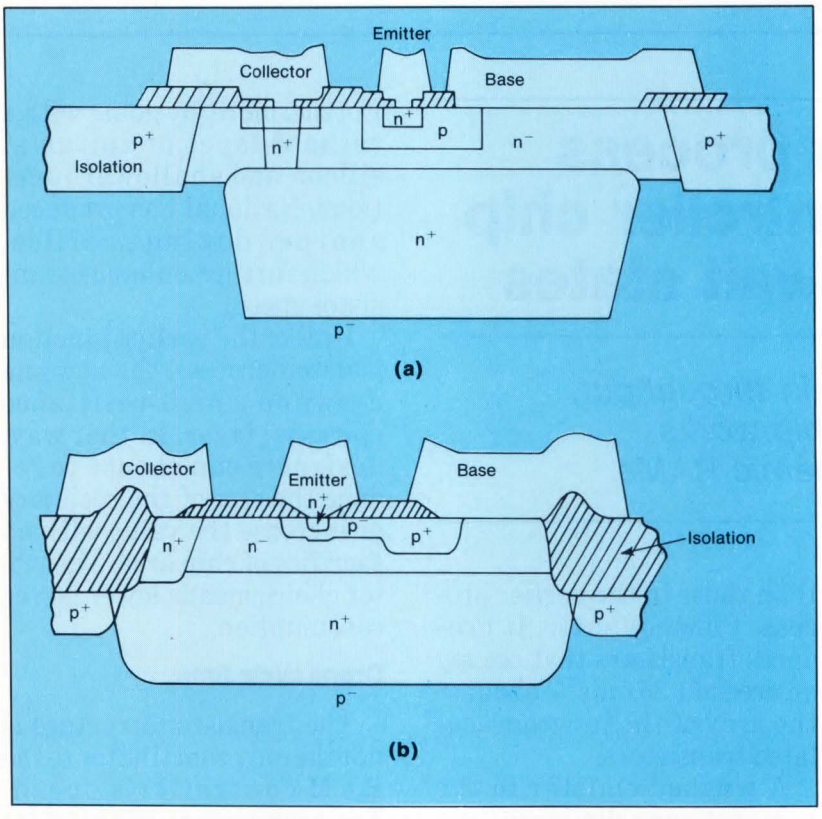
Besides smaller emitters, the oxide-isolation process produces lower parasitic capacitances, which translate into higher operating frequencies for the transistors. Furthermore, by going with a thinner layer of epitaxial silicon and shallower junctions, National has produced sharper doping profiles, which further enhance transistor speed.

Unlike the earlier junction isolated process, the new one draws on a high-resistance epitaxial layer. In that way, designers can choose to reduce the size of the resistors or increase the value with no sacrifice of chip area. The latter choice means lower power consumption.

Drops cycle time

The transistor structure is not the only contributor to the RAM controller's speed. The architecture of the older chip has been significantly trimmed, lowering system cycle time and enhancing circuit stability. For instance, the placement of a voltage regulator and a delay line on the chip boosts the accuracy of the system's timing. The regulator controls the internal power supply seen by the inverters in the delay line, thereby eliminating any changes in propagation delay caused by variations in the external power supply. In addition, extra circuitry compensates for the effects of temperature on the resistors and other elements.

The single-chip controller halves the number of operating modes of the 8409 eliminating those rarely used. In addition, it sports a new feature: a control pin that sets



To build its superfast dynamic RAM controller, National Semiconductor went from junction isolation (a) to oxide isolation (b), (4 times enlarged) yielding tighter packing densities and transistors that occupy about half the space of their predecessors. The older process needed overlapping spacing regions, the newer one self-aligns the contact region with the emitter.

the delay line to a row-address hold time (t_{RAH}) of either 15 or 25 ns. Since delay times differ with RAM organization, generation, and supplier, the ability to match the delay time to the RAM is a big step toward system optimization.

Physically, the dynamic RAM controller drops right into the socket filled by the 8409. *Dave Bursky*

Two-processor board brings flexibility to voice applications

A single-board subsystem calls on the resources of a general-purpose processor and a digital signal processor to handle not only speech recognition and synthesis, but storing and forwarding of voice signals as well. The hardware and software flexibility of the board will permit future software packages to tackle such jobs as converting text into speech, and eventually the board could serve as a 1200-bit/s modem. Designed by ITT Information Systems (Tempe, Ariz.), it can plug into a card slot in any IBM-compatible personal computer.

The trick lies in the programmability of the two processors. Since the board has its own 8088 processor, it can operate independently of the CPU in the host system. Thus, it can pull in files when it has to and eliminate many of the delays normally encountered when the host CPU is responsible for control.

The TMS320 digital signal processor performs most of the computations needed for matching templates and other functions. It has separate memory—PROM to store various routines and local RAM to hold parameters and data that must be accessed rapidly. The two processors communicate through a dual-port 512-byte RAM.

The three-tier software structure, designed specifically for this board, actually ties together the processors, the associated memory, and the logic. Typically it comes on a floppy disk and is loaded into a hard disk-based PC. Depending on the function desired, the appropriate routine and parameters are loaded into the local RAM on the board.

Layered functions

The software is divided into three basic layers (see the figure). The first resides on the disk and covers routines for vocabulary training, phone management, and I/O drivers. The middle layer encompasses the functional

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routines—voice recognition templates and feature extraction procedures, synthesis, and so forth—that are downloaded to the board. The third layer consists of the routines needed by the TMS320 digital signal processor for recognizing speech, digitizing it, playing it back and also for controlling the telephone.

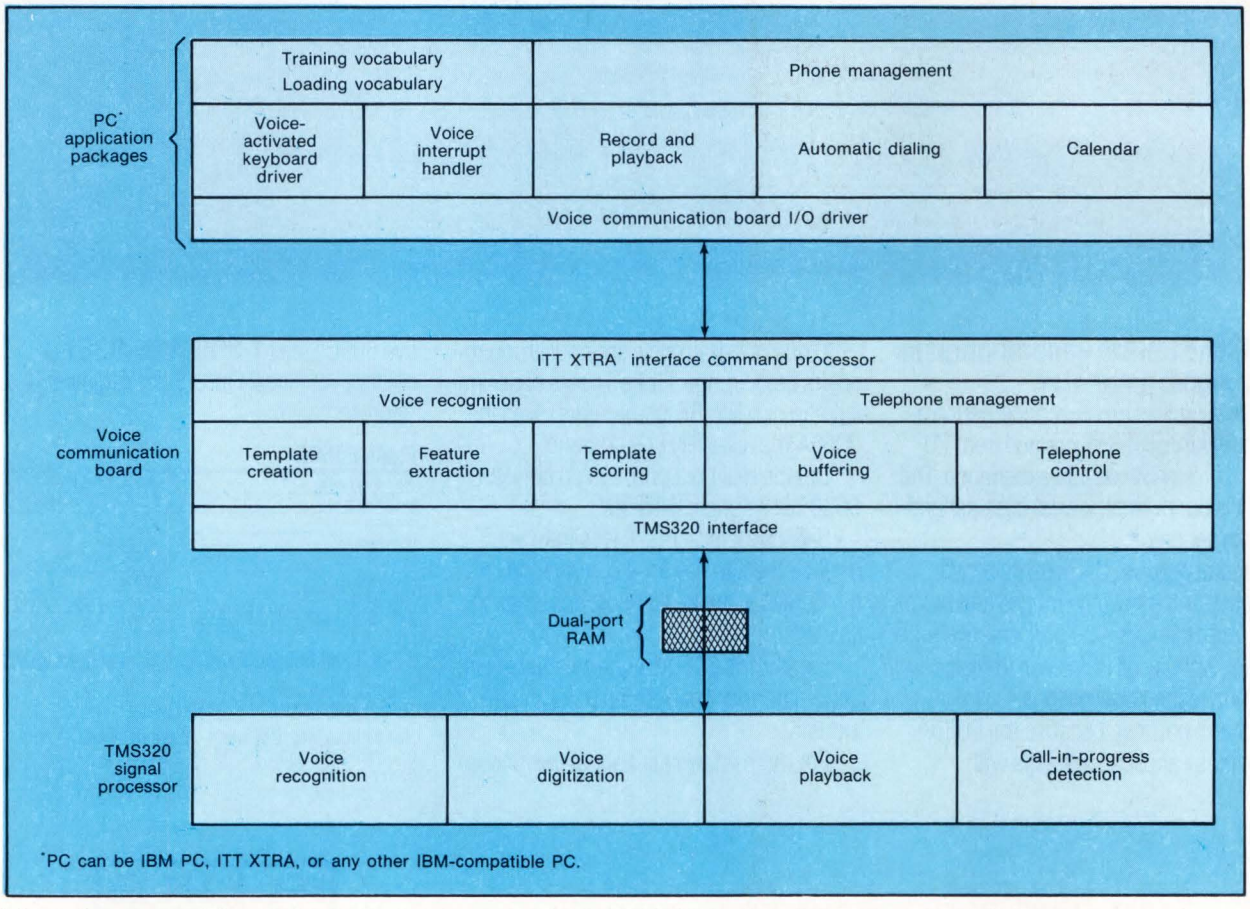
More robust

To perform voice digitization, ITT uses a scheme called residual excited linear prediction, which it feels is more robust than the more popular linear predictive coding technique. In this process, voice signals are sampled 8000 times per second, digitized into 8-bit samples, and then compressed, yielding a final data rate of 8 kbits/s. A word template requires about 1 kbyte of memory space.

As a speech recognizer, the card can handle a speaker-dependent vocabulary of 200 words, or a pooled-speaker vocabulary of 25 to 100 words, depending on the number of speakers. A vocabulary consisting of 200 templates can be matched in less than 300 ms, and that time can be shortened if smaller subsets are used to build word files.

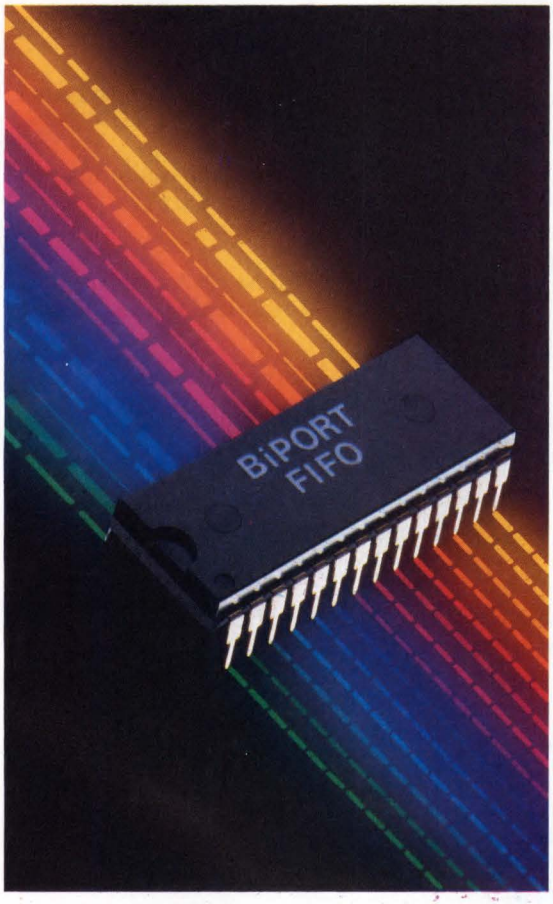
Initially, the system will come with programs that handle speech recognition, voice mail, appointment calendars, telephone directories, and automatic dialing and answering. The user will be able to "toggle" between the applications without having to exit from either routine. In the voice-mail mode, the system operates with a data rate of 9600 bits/s.

Aside from the two processors, the board consists of a local 128-kbyte RAM program and data space, separate PROM to hold the TMS



The voice recognition and synthesis processor from ITT Information Systems runs with three major software layers: a group of basic routines that reside on the personal computer's disk, another group that covers the general functions of the board, and the last group, which controls the operation of the TMS320 digital signal processor.

SYNC THE UNSYNCABLE



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UNITED TECHNOLOGIES MOSTEK

CIRCLE 26

320 routines, the 512 bytes of dual-ported RAM, and the telephone line interface, as well as tone generation and detection circuitry. To pack all the circuitry onto a single card, ITT designers densely populates a six-layer printed circuit board that routes all the signals. *Dave Bursky*

Pipelined structure ups tape controller's transfer rate by 30%

A pipelined architecture consisting of a FIFO buffer and three latches increases the bus communications rate of a Multibus-compatible tape controller card by 30%. Designed for streaming and start-stop ½-in. tape drives, the Multibus I board also attains a throughput high enough to accommodate cache tape drives.

The 16-bit latches allow the Tapemaster 1000 controller board, developed by Ciprico Inc. (Plymouth, Minn.), to exchange data with the tape drive at rates of up to 1.5 Mbytes/s. Latches 2 and 3 (see the figure) are used to match the bus data rate to the practical limits of the Multibus. The FIFO buffer stores data from the tape drive until the most efficient amount, as determined by the user, can be loaded onto the bus. When that level is reached, the card takes control of the bus and transmits the data at 4 Mbytes/s.

The controller board coordinates bus and buffer cycles by putting latches on either side of the buffer, thus allowing data to move in overlapping steps. The latches hold the data as it flows from the 260-ns memory, preloading the data for transmission to the bus. Without the latches, wait states would have to be added to synchronize the cycles, thus degrading throughput.

To maximize communication with the host, the Tapemaster 1000 lets users determine how long it will control the bus. Programmable throttling, as this feature is called, lets users select either a time period ranging from 1 to 40 μs or the transfer of from 2 to 256 bytes. Thus, the user can send large data blocks by holding the bus for longer periods or send several short bursts of data.

Handles new drives

To exchange data with the new generation of tape drives, the system uses latch 1. Most tape drives currently have maximum bit densities of 6250 bpi and streaming tape speeds of 125 ips, so transfer rates of about 750 kbytes/s are acceptable. However, new drives with cache buffers can handle more data flow, forcing controller boards to roughly double transfer rates.

The pipelined architecture lets the controller simultaneously access system memory while it reads from or writes to the tape drive. An example is scatter-gathering, a task that lets the board read one data block from the tape drive and store it in non-

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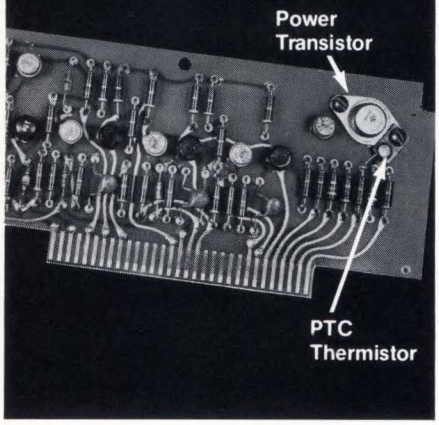

This PTC thermistor — acting as a solid-state switch — has been wired to a circuit board as a defense against transistor destruction due to overheating. Bonded to a tab, the PTC measures surface temperature of the transistor, and when reaching the critical point, shuts off the drive circuitry to the transistor. After cooling, the PTC automatically resets itself.

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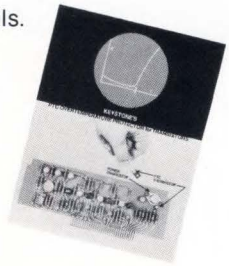

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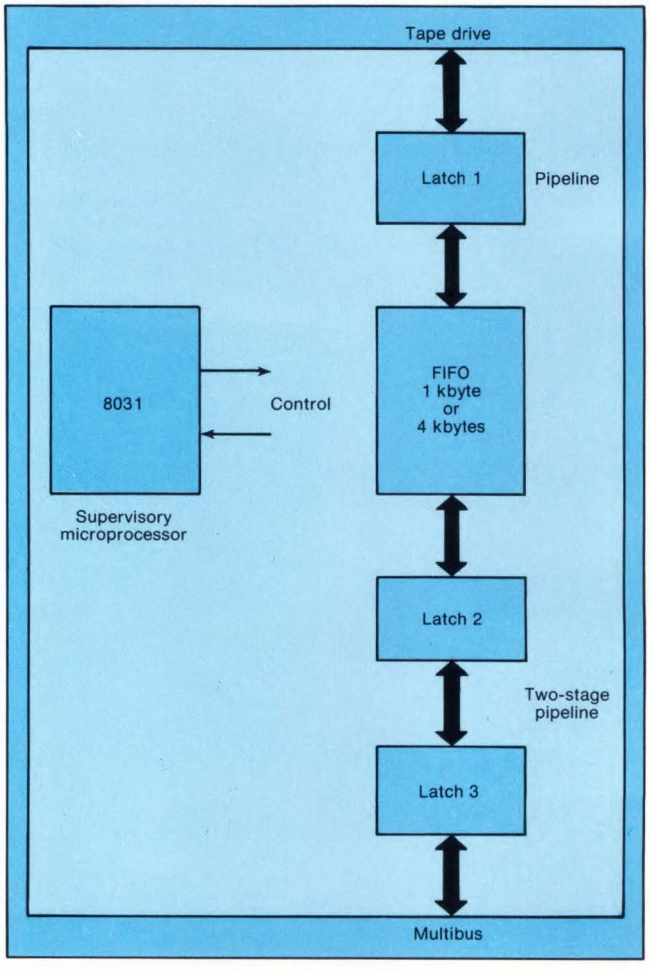
CIRCLE 27

contiguous memory locations. This feature is one of the commands which can be called into play using the controller's ring buffering technique. The ring buffering commands, stored in firmware, include pointers which lead to the next consecutive data block. This frees the host to perform other tasks since it no longer needs to determine the next consecutive data block which must be written or read. Alternatively, the controller can read noncontiguous blocks from system memory and group them into a single tape data block. These tasks, frequently called for in virtual memory applications, can be performed on-the-fly.

The pipeline also translates the 8-bit data coming from the buffer and tape drives into 16-bit words needed for Multibus systems. Though the board is controlled by an 8-bit microprocessor, it does not handle data because of its relatively slow speed.

Terry Costlow



A ½-in. tape controller board from Ciprico incorporates three 16-bit latches to form a pipeline that speeds data communication. The latches preload data for transfer to the bus or tape drive, thereby eliminating wait states.

New 4-bit raster DAC sharpens graphics

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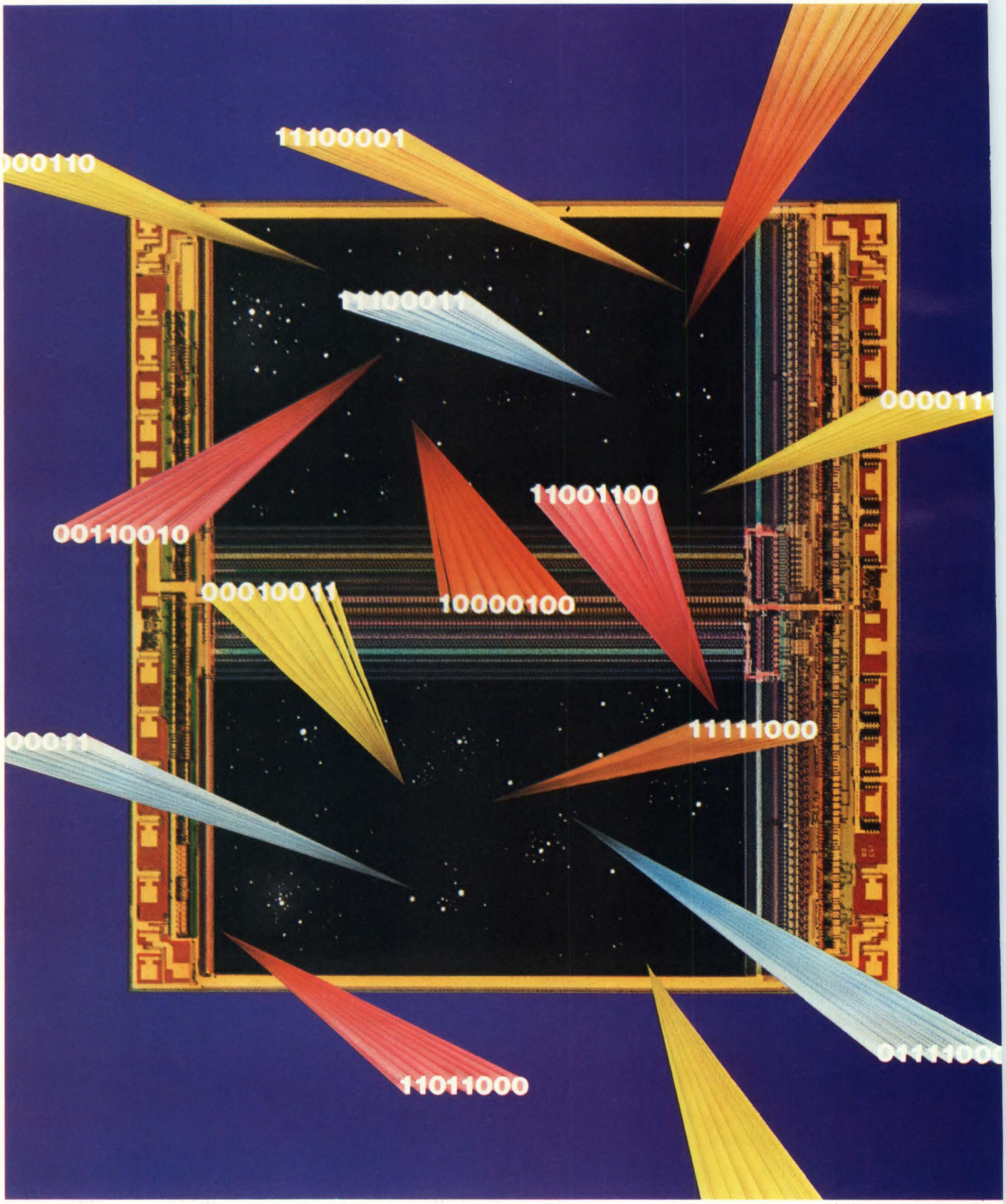
CIRCLE 28

Motorola's 256K ROMs or 50



give you 150 ns speed μA power. Pick a winner.

When you need the 256K ROM with state-of-the-art speed, Motorola has it—the 150 ns MCM63256.

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Get a lot. Trade-off little.

Whether your requirements run to super speed or ultra-low power, Motorola satisfies them. And you don't make severe trade-offs to get the performance you need most.

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Certainly speed is the biggest attraction of the high-performance N-channel HMOS MCM63256, yet maximum power dissipation is a low 15 mA, standby, and 100 mA active.

There's also a 200 ns version of the MCM63256, and matching high-speed 128Ks are available, too.

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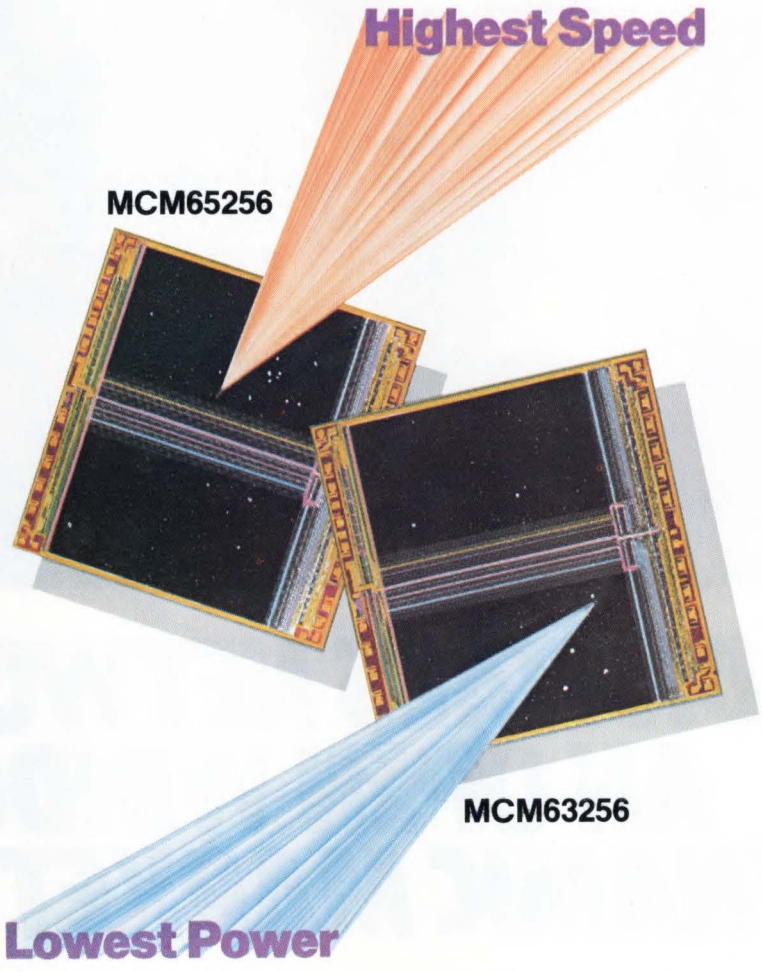

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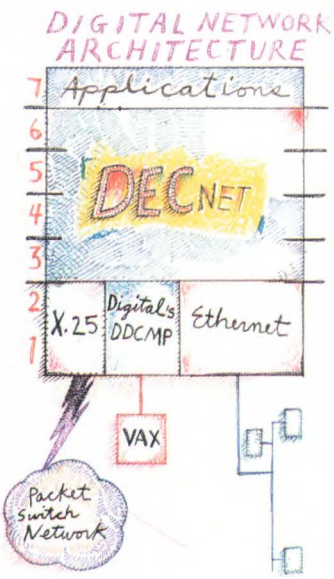

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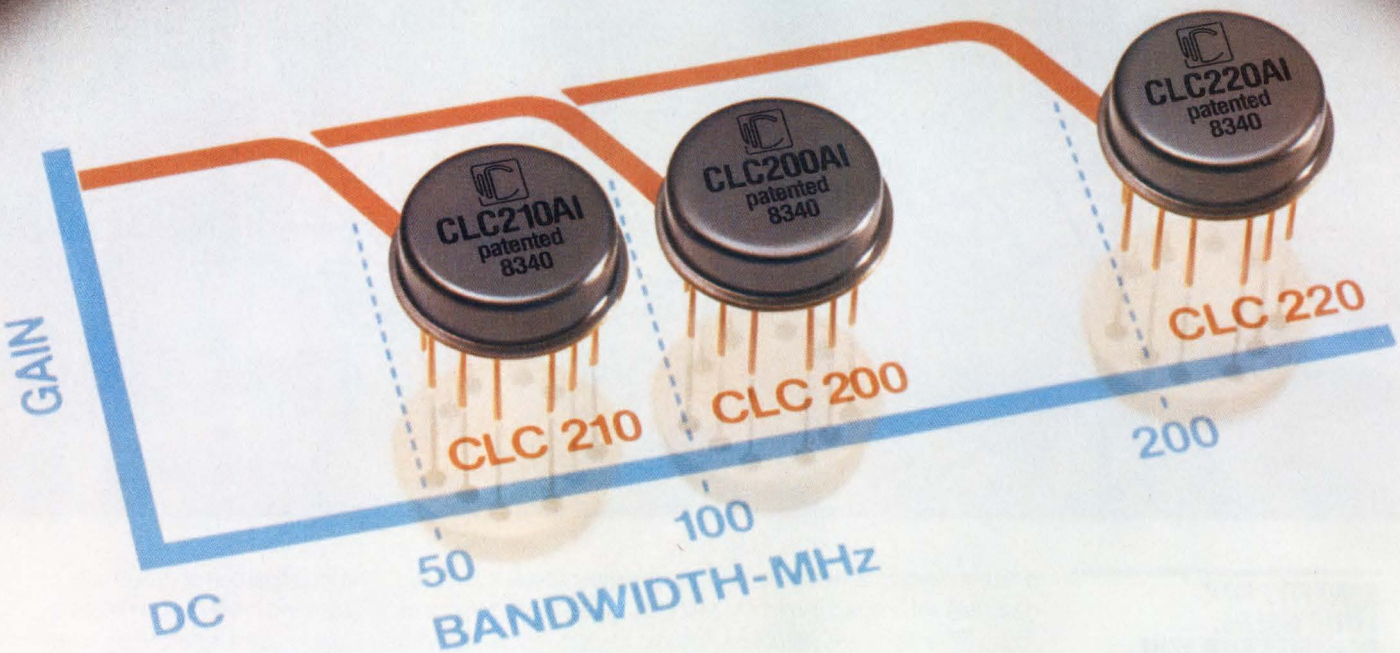

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CIRCLE 29

CONFERENCE PREVIEW

Application-specific ICs top the charts at February's ISSCC

Besides application chips, dynamic and static memories are the hot numbers; some analog favorites get an updated treatment.

As interest in application-specific circuits mounts, the density and speed of such chips is on the rise. The hottest of these ICs—memories and processors—can be seen at the International Solid-State Circuits Conference (New York City, Feb. 13-15). Also of major significance is the work that has been done to proliferate and boost the speed of 1-Mbit dynamic RAMs and 256-kbit CMOS static memories—devices considered rarities only a year ago.

More traditional circuits, of course, will not be left out in the cold, as the presence of an 8-bit, 500-MHz digital-to-analog converter shows. Other analog chips can also be seen. Additionally, the conference will play host to some of the latest in semicustom circuits and high-speed gate arrays will be unveiled.

Application-specific memories are showing up with an assortment of internal organizations, allowing engineers to choose the configuration best suited to their systems. One example is a dual-port RAM that is laid out as 64k by 4 bits.

From NEC Corp. (Kanagawa, Japan), the circuit is four times as dense as currently available devices and can be accessed in 35 ns. The memory handles graphics data from any node in a system. A 2k-by-9-bit circuit, developed by AT&T Bell Laboratories (Allentown, Pa.), demonstrates another possible layout.

Martin Gold

New tricks

Some of the memories to be covered at the conference integrate untraditional functions. For instance, a 128-kbit EPROM from Intel Corp. (Santa Clara, Calif.) carries a built-in pseudorandom number generator, as well as the requisite encryption circuitry to generate a security key.

Processors, like memories, are increasingly being designed with specific applications in mind. A case in point is a video signal processor for facsimile machines. It joins a 4-bit flash analog-to-digital converter with an offset canceller to clip along at 5 MHz. The 2.5-μm CMOS chip, from Hitachi Ltd.'s Central Research Laboratories and its Device Development Center (both in Tokyo), weighs in with 25,000 transistors and 840 bits of RAM and can control a CCD image scanner.

Another CMOS processor, this one for a computer-controlled telephone, employs a 5-bit logarithmic a-d converter and 46-db programmable gain amplifiers. The circuit, designed by Bell Northern Research and Northern Telecom (both in Ottawa, Canada), controls half-duplex speaker microphone signals.

The work being done with floating-point arithmetic processors should be of great interest to designers assembling systems built around the new generation of 32-bit microprocessors. High-speed arithmetic can be had on a single chip or on a board-level subsystem.

One of two floating-point math chips hustles along at 14 MHz. This IEEE standard coprocessor is aimed at 32-bit microprocessors. It is fabricated with 1.75-μm twin-tub CMOS and handles single-, double-, and extended double-precision math, as well as 32-bit integer and 18-digit BCD operations. The processor is the creation of AT&T Bell Laboratories (Holmdel, N.J.).

Another processor, this one from Nippon Telegraph and

CONFERENCE PREVIEW

Telephone Public Corp.'s Atsugi Electrical Communication Laboratory (Kanagawa), is built with 1.2-μm n-well CMOS. The 80-bit device contains 15 kbits of memory and 50,000 gates and executes a staggering 5.6 million floating-point operations/s.

Dynamic RAMs capable of retaining 1 Mbit and CMOS static RAMs storing 256 kbits were just emerging a year ago. They are not the rarities they were then and they are getting faster as well. Most impressive is a dynamic RAM that can be accessed in 85 ns and that fits in a low-cost plastic package. The 43.2-mm^2 chip, from NEC, adds an interconnection layer that enables it to be housed in a 300-mil plastic DIP.

Other 1-Mbit dynamic RAMs to come under scrutiny at the conference display some interesting new wrinkles. A 65-mm^2 chip from Mitsubishi Electric Corp. (Itami, Japan) is built around a shared sense amplifier and features a continuous nibble mode. The IC can be accessed in 90 ns and sports a test pin that allows it to be examined as if it were configured as 256k by 4 bits.

Joining a divided bit-line matrix and a 1.2-μm double-metal CMOS process has yielded a 1-Mbit dynamic RAM that runs off 5 V and has an unprecedented array area-to-die ratio of 56.6%. Its creator, Mostek Corp. (Carrollton, Texas), also points out that over 80% of the total die area is repairable using laser-programmed redundant rows and columns.

Clearly, fast static RAMs have arrived as well, as can be seen in three 256-kbit CMOS memories. Two of the ICs boast an access time of 45 ns. One, from the Central Research Laboratory of Hitachi Ltd.'s Musashi Works (Tokyo), is a 32k-by-8-bit circuit

ISSCC '85's evening agenda

As is traditional, the ISSCC's evening panel sessions will attempt to shed some light on the more controversial issues surrounding the leading integrated circuit technologies. One of the hot topics at the upcoming conference will be the impact of VLSI chips on the coming generation of artificial-intelligence computers. Other subjects that are likely to stir up some lively discussions are the limitations of submicrometer MOS, the future of custom and semicustom design, the challenges CMOS faces from high-speed LSI technologies, the role of CAE workstations, and the future of nonvolatile circuits.

Clearly, VLSI technology is one of the keys to creating machines specifically tailored to AI, which requires fast sorting of and searching through large data bases. These new computers will implement parallel processing in hardware and manipulate a range of data types.

The role that 32-bit microprocessors may play in AI-based computers will be analyzed by experts from the semiconductor industry, universities, and companies investigating artificial intelligence. VLSI's effect on AI will also be the theme of the conference's keynote address, which will be delivered by Raj Reddy, professor of computer science at Carnegie-Mellon University. This talk, and the presentations of other participants, will cover chips that could contain a hundred million or a billion elements sharing a common bus to a larger external memory. Obviously, the numerous processors involved will not be identical. Some may work with dynamically alterable PLAs, others may carry out on-chip analog-to-digital and digital-to-analog conversions, and still others may contain network interfaces.

The future of submicrometer MOS also will be given a good going-over. The technology has now reached the point at which design rules of 1 μm are possible. The question that remains to be answered is where to best concentrate industry efforts to achieve the projected twenty- to thirty-fold increase in device density that MOS now promises.

CMOS, meanwhile, is likely to be challenged on the high-speed front by such emerging technologies as gallium arsenide, aluminum gallium arsenide, and silicon bipolar. All are looking to demonstrate clear-cut performance advantages that will let them slip neatly into specific niches. This panel will discuss the potentials of these technologies in what is likely to be an era dominated by CMOS VLSI.

The explosion in workstations, CAD software and the proliferation of makers of gate arrays and standard cells reflect the tremendous impact of semicustom and custom ICs. One panel will look to the future of custom and semicustom designs, seeking to identify the tools that will be most useful in working with them. Another session will analyze the future of CAE workstations—from the user's point of view. Some of the questions to be addressed are the actual functions of the workstations, as well as their usefulness and their limitations.

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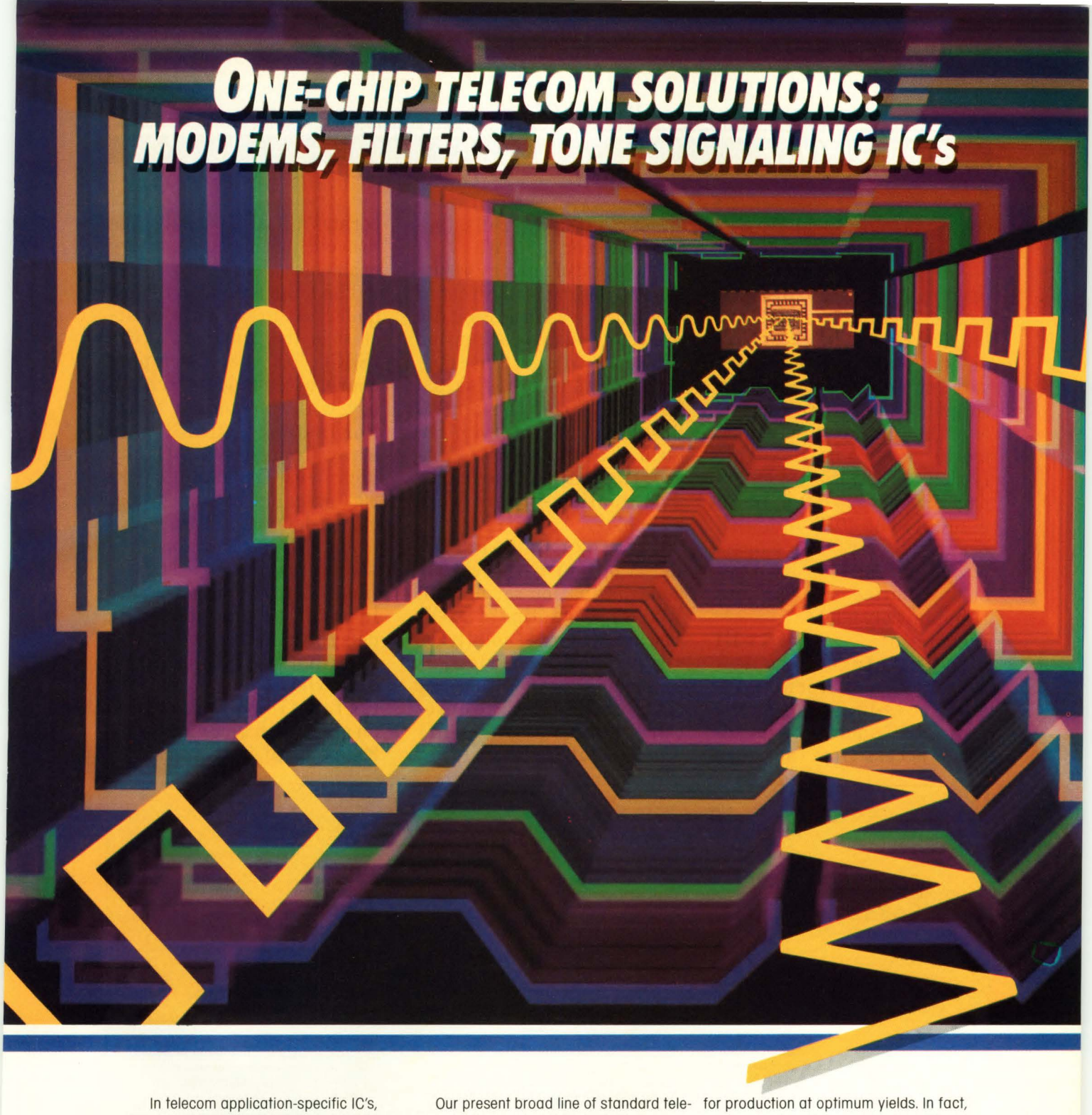

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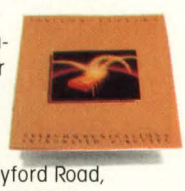

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that consumes 200 mW when running at 10 MHz.

The second RAM, developed by Mitsubishi, draws a peak current of 45 mA. That low drain is obtained by using an address-transition-activated circuit combined with a three-level word-line circuit.

Although the third static memory—at 55 ns—is slightly slower than its two kin, it draws merely 10 mW on standby. The 40.77-mm^2 die, created by NEC, uses optimized polysilicon load resistors, buried isolation, and titanium polycide.

Other static RAMS will also be featured. One is a 4-kbit gallium arsenide device. The 1k-by-4-bit memory, from NEC sports 2.4-ns address access time for cache memory. Its power dissipation, however, is 1.1 W.

The world of analog circuits is not standing still. Proof of this can be seen in an 8-bit d-a converter with a conversion rate of 500 MHz, a 2-ns settling time, and 0.6-ns rise and fall times. From the Central Research Laboratory of Hitachi's Takasaki Works (Tokyo), the chip is fabricated with shallow-groove VLSI technology.

Also to be unveiled is a 150-W op amp with a continuous dissipation rating of 90 W and a peak rating of 800 W. The amplifier was jointly devised by Robert Widlar, an independent consultant and National Semiconductor Corp. (Santa Clara, Calif). The 35-V, 10-A device incorporates a class B output stage to avoid quasicomplementary problems.

The huge amount of work under way in semicustom circuits is also apparent at the ISSCC. These chips employ nearly every process technology, with emphasis on speed. For instance, an ECL gate array, from Siemens AG (Munich, West Germany), packs 9000 gates and boasts a propagation delay of 99.6 ps.

An ECL field-programmable array developed by National Semiconductor comes in with a total propagation delay of 3.6 ns at 1 W. Further, working with gallium arsenide, Oki Electric Industry Co. Ltd. (Tokyo) has created an array with 1000 gates and a 390-ps speed. □

Some highlights of ISSCC '85

Memories

Dynamic

85-ns 1-Mbit RAM in plastic DIP (NEC)
90-ns 1-Mbit RAM with multiple-bit testing (Mitsubishi Electric)
1-Mbit CMOS RAM with divided bit-line matrix architecture (Mostek)
Experimental 4-kbit RAM with 16 coded levels per cell (Hitachi)

Static

45-ns 256-kbit CMOS RAM with 200-mW power dissipation at 10 mHz (Hitachi)
55-ns 256-kbit CMOS RAM with 10-μw standby power consumption (NEC)
45-ns 256-kbit CMOS RAM with three-level word line (Mitsubishi Electric)
GaAs 4-kbit RAM with 2.4-ns address access (NEC)

Nonvolatile

25-ns 16-kbit CMOS PROM (Cypress Semiconductor)
95-ns 256-kbit CMOS EPROM (Hitachi)
256-kbit EEPROM with three polysilicon layers (Toshiba)
100-ns 256-kbit CMOS EPROM (Intel, Sierra Semiconductor)
64-kbit EEPROM with extended temperature range (Advanced Micro Devices)

Other

35-ns 256-kbit dual port RAM (NEC)
1-Mbit ROM with error correction circuitry (Mostek)
2k-by-9-bit CMOS dual-port RAM (AT&T Bell Laboratories)
128-kbit EPROM with built-in encryption circuitry (Intel)

Processors

Floating-point

80-bit floating point processor in 1.2-μm n-well CMOS running at 5.6 million floating-point operations/s (NTT)
14-MHz IEEE standard floating-point coprocessor for 32-bit microprocessors (AT&T Bell Laboratories)

Signal

NMOS pipelined image processor using quaternary logic (Tohoku University)
digital signal processor with multiprocessing capability (Texas Instruments, ITT)
Programmable digital signal processor with 32-bit floating-point arithmetic (AT&T Bell Laboratories)

Semicustom arrays

80-ps 2500-gate bipolar macrocell array (NTT)
100-ps 9000-gate ECL arrray (Siemens AG)
3.6-ns ECL field-programmable array (National Semiconductor Corp.)
390-ps 1000-gate GaAs array using superbuffered FET logic (Oki Electric)

Analog circuits

8-MHz 8-bit CMOS subranging a-d converter (RCA)
10-bit CMOS a-d converter with sample and hold (Intersil) 8-bit d-a converter with 500-MHz conversion rate (Hitachi)
150-W op amp (National Semiconductor and Robert Widlar independent consultant)

Other

4-chip Integrated Services Digital Network line termination set (Bell Telephone Manufacturing)
2.56-Mbit/s digital local loop transceiver (Bell Northern Research and Northern Telecom)
350-μW fifth-order low-pass switched-capacitor filter (University of California)
480-by-400-element image sensor with a charge-sweep device (Mitsubishi Electric)
350-ps Josephson junction 4-bit parallel multiplier (NEC)

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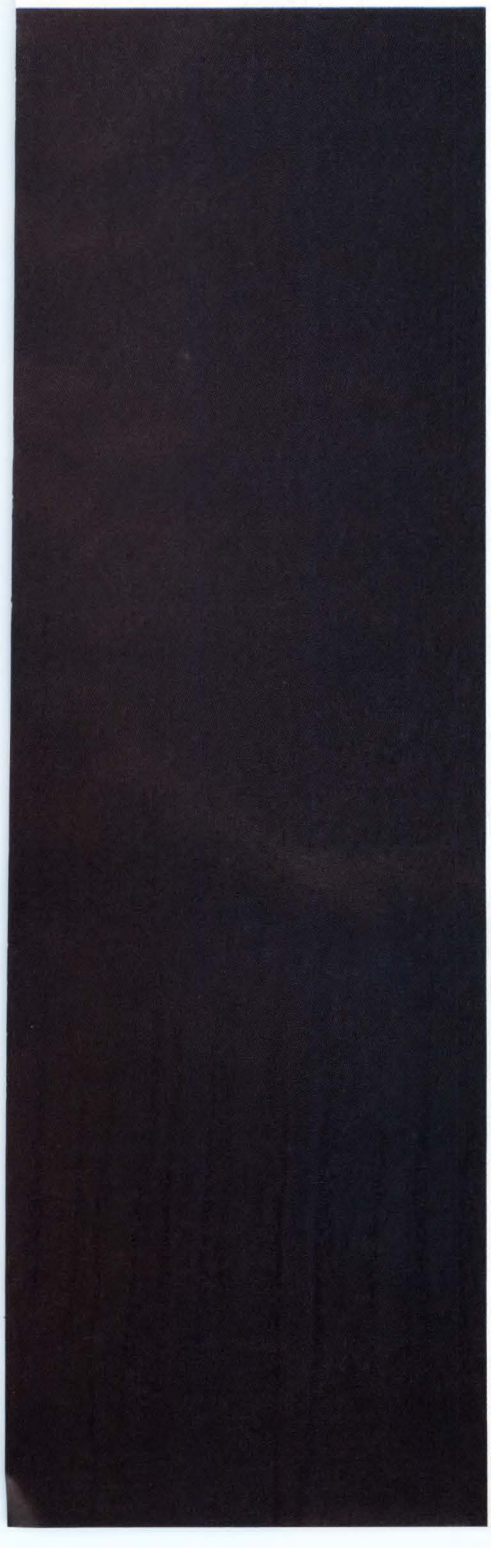

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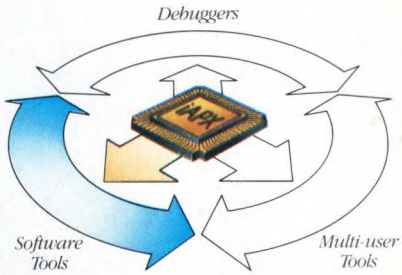

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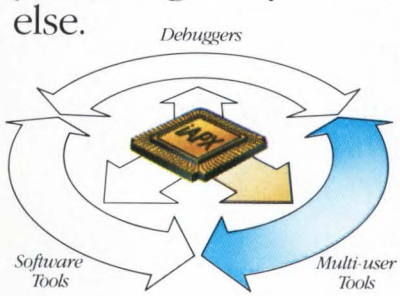

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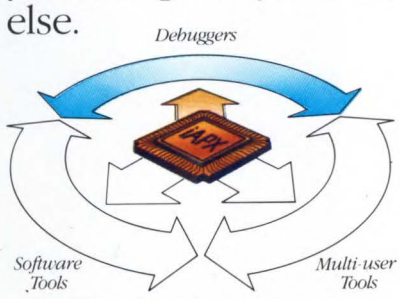

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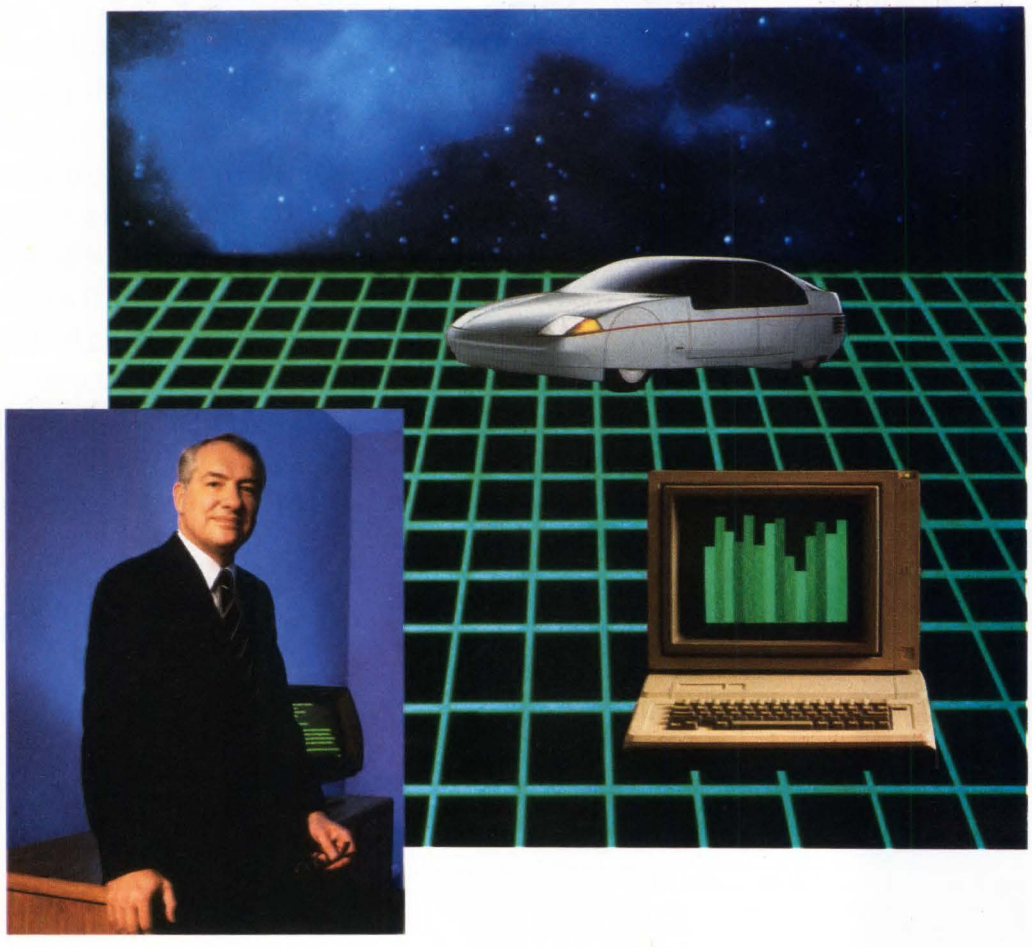

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NEWS ANALYSIS

Making logic programs execute in parallel is today's AI challenge

Fifth-generation hardware may already be defined, but getting the software to run in parallel is emerging as a tough problem.

Japan's announced goal to produce a fifth-generation computer by 1990 has spurred artificial-intelligence researchers worldwide to a feverish pitch of activity. In all likelihood, their primary challenge will lie not in building machines containing many processors operating in parallel—as the hardware has generally been defined—but rather in programming those machines in parallel.

Architecture, algorithms, and languages all influence each other in parallel systems, since multiple processors must grind away at separate slices of a problem. That intimate relationship represents one reason that parallelism has yet to pay off in areas other than linear algebra. Scientific programs running on vectorized supercomputers can calculate a pipeline full of additions in one clock cycle, but programs that simulate human logic—as the fifth-generation computers are expected to do—run sequentially for the most part.

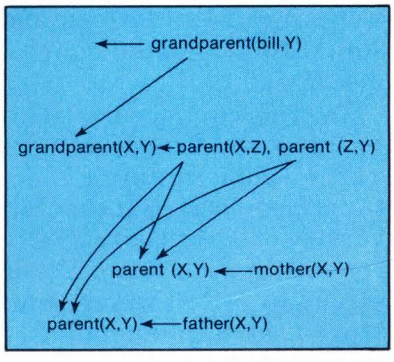
Carole Patton

The Japanese have targeted Prolog as the programming language of the fifth-generation computers. Because the language is not procedural, it is well suited to situations that prevent clear definitions of problems and solutions. Furthermore, it is a good compiler language, describes relationships well, and can be adapted to programming relational data bases.

Prolog does, however, have a significant drawback: Its basic mathematical operation, unification, is a sequential—not a parallel—process, which substitutes goals to make logic terms identical. Prolog converts formal logic, such as the phrase "All elephants have trunks," into a representation called a Horn clause—is an elephant (x)←has trunk (x). The equation reads as follows: For all x, if x has a trunk, then x is an elephant. Calculus notation is used, but as the process of reasoning proceeds in the program, that notation must preserve the truth.

But, the overall advantages of Prolog, are prompting companies and universities to explore ways of making its code—essentially, predicate calculus—parallel. One bit of unusual research looks for similarities between equations and logic languages. The concept, being tried out at the Research Institute of Electrical Communication at Tohoku University (Sendai, Japan), draws on algorithms that transform equation-oriented programs into logic programs using an extended version of Prolog.

The university bases its premise on the fact that a logic language, Prolog and Lisp included, employs recursive functions and other mathematical operations that are



Logic clauses are connected via pointers in a directed structure. Here the arrow heads record the order in which the terms should interact. The clauses now take on the aspects of a data-flow graph. Note that constants are bound to variables: At the top of the graph, the constant bill **is bound to the variable** Y.

NEWS ANALYSIS

special types. So, these particular kinds of problems can be formatted like an equation, and solved the way an algebra problem is solved—with reduction rules that match a left-hand expression to a right-hand one, and reduce each side successively until it can go no further.

Other avenues of research have identified two types of parallel logic programming structures in Prolog. OR and AND. OR problems find a value for the right-hand expression that will make the left-hand value true. Processing OR clauses in parallel is relatively easy, as one part of the problem does not depend on another part. But in an AND problem—like P:-Q, R, S—P is true only when Q, R, and S all are true.

One hardware-oriented scheme for extensive OR parallelism uses a number of processors constituting a parallel interface engine. That engine interfaces with two-level networks and uses TTL logic and some sophisticated control mechanisms.

To program the parallel interface engine, its developers at the Department of Electrical Engineering at the University of Tokyo essentially rewrote unification goals, or slices of OR clauses, and stored them independently in a pool. An optimization scheme subsequently reduced the pool's size. The university's results were conclusive: Test programs written in Prolog for a 256-node engine ran 170 times faster than did sequential Prolog versions.

An alternative scheme compiles logic clauses into single-execution graphs. Devised by the Department of Information and Computer Science at the University of California in Irvine, the technique essentially converts a logic program into a data-flow graph, which basically serves as the program. Data travels in arcs, and a node fires when the information arrives. Each node accepts, emits, and processes value tokens traveling asynchronously along the graph arcs. The tokens themselves identify devices for reassembling program parts.

The data-flow graphs are combined to form "templates," a sort of graphic family tree. Here, relationships between individuals, like "mother" and "father," are recorded as a list of assertions, and the problem might be as simple as understanding the question: "Who is the grandparent of Bill?" (see the figure).

The construct becomes a graph by representing the head of a clause—called its literal—as a directed arc, with arrows recording the order in which the terms are given. A simple assertion, "Bill's father is John," becomes more intricate as other clauses, connected by direction pointers, embellish the simple relationship. Terms are interpreted as nodes connected by arcs, producing the equivalent of a data-flow graph.

AND clauses are much harder to organize in parallel because they share variables. When variables (like X and Y) are shared, they must be bound to the same literal during execution. In this case, literals that share variables are grouped into clusters. In a relatively complex piece of restructuring, subtrees of clusters are filtered out for parallel processing.

A more restricted means of creating AND parallelism forwards information between literals that share the same variable. The processing scheme, devised by IBM Corp.'s Thomas J. Watson Research Center (Yorktown Heights, N.Y.), allocates terms for parallel or sequential treatment based on their type. For example, a ground term—that is, one containing no variables—would carry a type code preset by the compiler; terms with variables would carry other codes.

The scheme is developed to run on a tightly coupled parallel processor, with each element containing its own local memory and owning a copy of the entire program. Within each node are two expression stacks, a sequential stack and a parallel stack. User queries are read, converted into an execution graph expression, and placed on the sequential stack. As the processor draws on that stack for its next job, it tests for the subexpression type. If a subexpression proves suitable for parallel processing, it is placed in the parallel stack.

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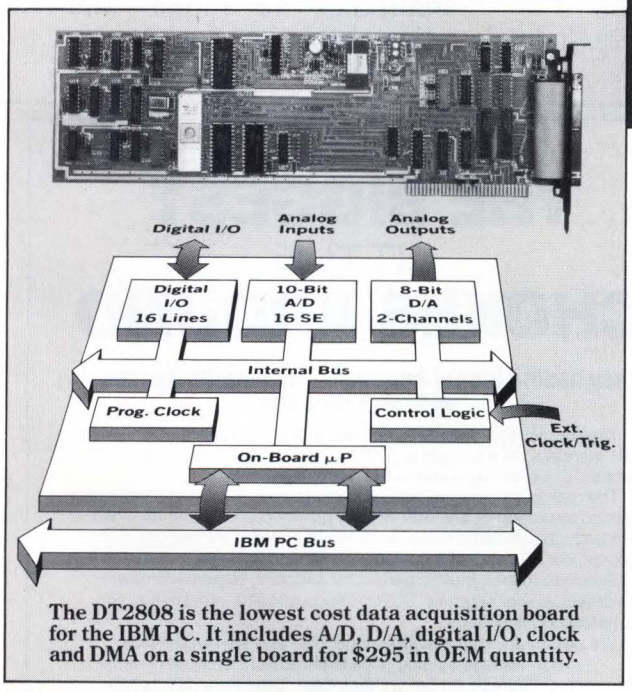

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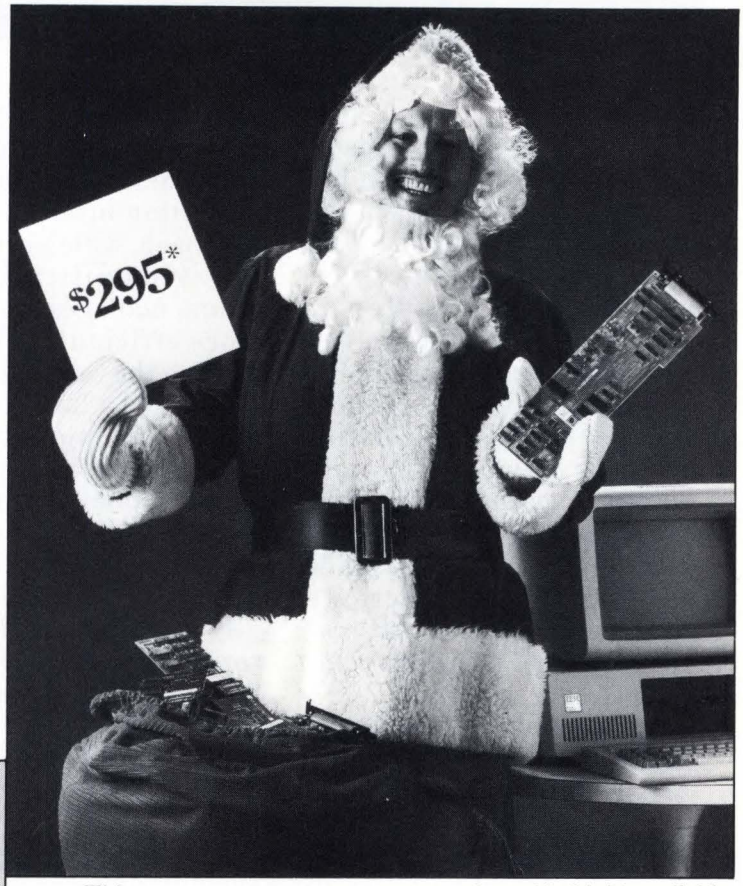

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NEWS ANALYSIS

stack.

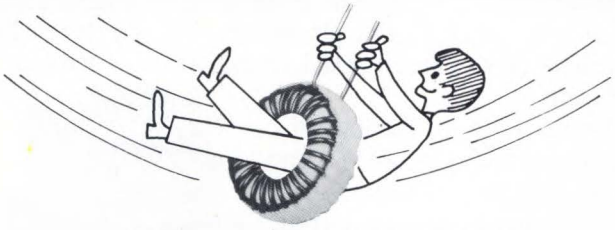
As one of its obstacles to parallel processing, Prolog uses logical terms whose structure cannot be changed. Thus when a variable is assigned in the first step, it must be referred to in the second and all subsequent steps; otherwise the machine does not know which variable has been assigned. To retain context in parallel, the variable could be replicated with each term, but these copies eat up memory and create storage problems. Literal substitution also raises communications overhead.

A software-oriented tack taken by the Royal Institute of Technology (Stockholm, Sweden) extracts parallelism through semantic domains, which describe the state of a definition interpreter. This approach, which uses a complicated unification algorithm, manages memory far more efficiently than does copying the variables.

To avoid a large number of non-local memory references, the Royal Institute created a model in which each parallel activity becomes a "process," and variables are stored in separate but formally specified context directories. So-called environment directories are linked to form a tree, with each one's processes being a "leaf."

Whenever a process begins, a corresponding environment directory is dynamically created and linked to the parent directory, but no reference to context is fetched. The idea is reminiscent of demand paging, because contexts are fetched only when needed; but once fetched, they can be accessed by the parent directory. Thus, all "siblings" in a relational construct have access to the context.

Prolog's base in predicate calculus is actually set-theoretical logic, the underpinning of relational theory. In fact, Prolog declarations look much like a record in a relational data base, a resemblance that Japan—and others hope to exploit.□



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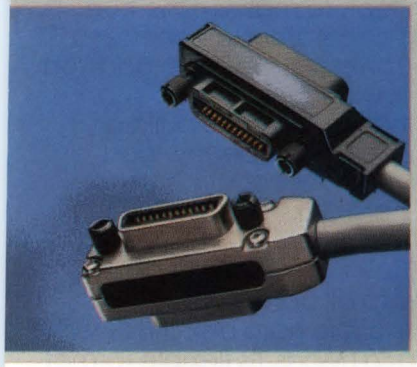

IEEE 488 versions, shielded or unshielded.

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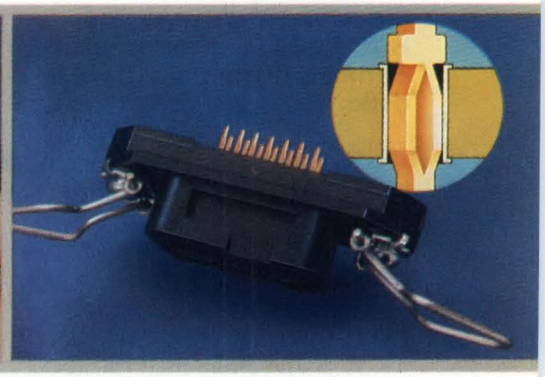

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Standard Microsystems' HDC 9224 is so advanced it controls hard disks, floppy disks and even tape backup.

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The cornerstone of an intelligent subsystem.

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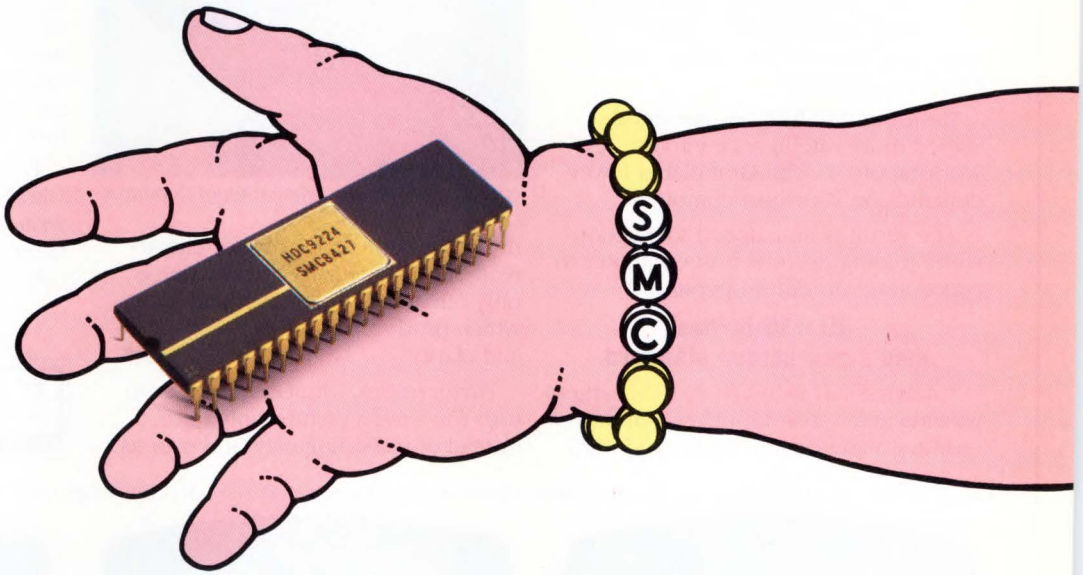
The HDC 9224 easily interfaces to all popular ST506-compatible hard disk drives with up to 16 heads. Its flexible format command lets you select hard disk sector lengths up to 16 kilobytes and can be used with both

disk controller.



interleaved and non-interleaved sector formats.

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The HDC 9224 Universal Disk Controller is an n-channel, silicon-gate MOS/VLSI circuit fabricated with Standard Microsystems' COPLAMOS technology. It's available for immediate delivery in a 40-pin ceramic or cerdip dual in-line package.

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At Lundy we don't develop technology for its own sake; we develop it to meet your needs. In the case of 3-D computer graphics workstations, you needed more speed, higher IQ, larger display and easier operation. UltraGraf delivers all four.

The Lundy UltraGraf is first when it comes to speed and IQ.

Keys to UltraGraf's instant response are a high speed microcomputer and a high resolution vector display, both developed by Lundy.

Besides these features, we've designed more intelligence into the workstation, so UltraGraf places fewer demands on your host computer.

The result is unmatched interaction while freeing up your host computer to concentrate on other operations.

19 × 15 inches sets a new screen standard.

UltraGraf's 21-inch CRT has the largest viewing area—19 × 15 inches—in the industry. Fast vector drawing and minimum operator time produce easy-to-read, flicker-free images. Spot size is only one ten thousandths of an inch, which produces remarkable crispness and clarity.

Lundy UltraGraf sets 3-dimensional standards.

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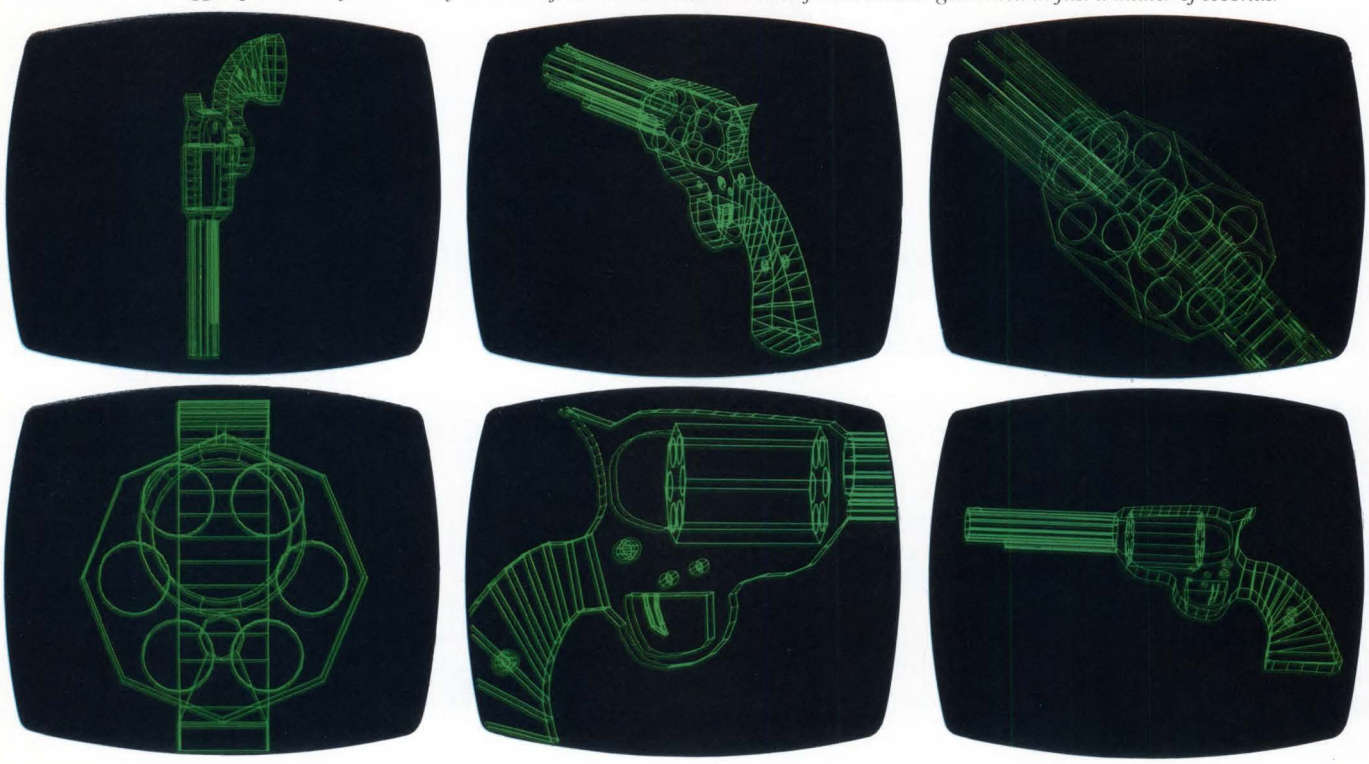


VIEWPOINT

The quest for a standard ½-in. tape cartridge may well be unnecessary

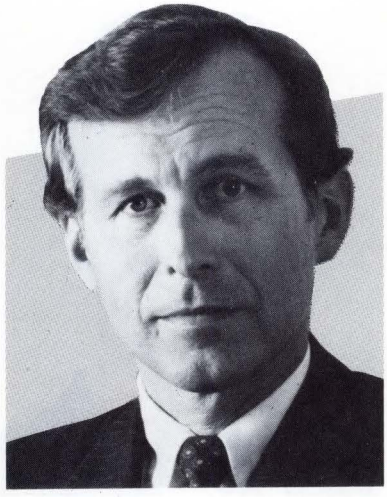
Raymond C. Freeman Jr.
Freeman Associates
Santa Barbara, Calif.

If a standard is to emerge for ½-in. tape cartridges," emphasizes Raymond C. Freeman, "it will almost certainly spring from the IBM e3480." He contends that IBM is already the clear-cut technological leader in high-performance ½-in. drives, giving it the needed authority to create a de facto standard. "In fact," he asserts, "manufacturers in a position to challenge this leadership have elected to wait and follow the company's lead."

As might be expected, Freeman's bold outlook is quite controversial. Some in the industry foresee a long hard climb ahead before standards emerge for ½-in. cartridges. Others believe just as fervently that manufacturers will endorse the smaller cartridge proposed by Digital Equipment and 3M. Despite such divergent opinions, Freeman sticks to his guns: "No one will successfully compete with IBM's package. It will be the standard for ½-in. tapes for the next decade."

Stephan Ohr

The 3480 cartridge, he explains, demonstrates how recording technology is moving in the same direction as computers and peripherals in general—toward smaller dimensions. Within its shell, which takes up only 4 by 5 by 1 in., it stores more data than a 10½-in. reel of ½-in. group-code recorded tape (200 Mbytes formatted compared with 180 Mbytes unformatted).



Since 1977 Raymond C. Freeman Jr. has headed up Freeman Associates, a consulting firm specializing in product and business strategies for manufacturers of storage peripherals. He also has worked at Applied Magnetics, Information Storage Systems, Honeywell Information Systems, and General Electric.

The cartridge comprises a single supply reel, with the take-up reel unconventionally mounted inside the drive itself. Its CrO_2 tape is split into 18 parallel tracks and has a density of roughly 19,000 bpi.

Though Freeman maintains that the IBM housing itself will be adopted as a standard, he readily admits that the drive—and even the type and composition of the tape—may be modified. Inevitably, he notes, OEM manufacturers will go with a serial or serpentine recording scheme, instead of taking the parallel path. Further, the special bias and head requirements of CrO_2 tape will probably make them opt for a more conventional coating.

As far as Freeman is concerned, other ½-in. cartridges, such as those proposed by Digital Equipment, MegaTape, and RossComp, are not really in the running to become standards. He backs his belief by pointing out that "in the high end of the industry, plug-compatible cartridge manufacturers have held off from making any commitments, waiting for IBM to make its move. Clearly, in the lower end also,

VIEWPOINT

they intend to follow its lead, thus effectively creating a standard.

"Their efforts will trickle down to the low-end OEMs who work strictly with serial recording and minis and supermicrocomputers." In fact, he believes that the high-end manufacturers will rapidly form a committee to adopt the standard, with makers of smaller drives quickly falling into line.

Freeman sees the 3480 tape drive as the "natural companion for 8-in. and high-capacity 5¼-in. drives." In the long run, its greater storage area "will edge out ¼-in. cartridges."

Thin-film LCD technology could be the key to large-area flat panels

Susumu Aizawa
Senior Managing Director
Epson Corp.
Nagano-Ken, Japan

Within the next five years," asserts Susumu Aizawa, "we'll see large-area liquid-crystal flat panels that display thousands of pixels side by side the CRTs now used with personal computers." The development, he states, may depend on devising active thin-film switching elements similar to those that are already at work in pocket-sized color LCD television receivers.

LCDs exhibit the lowest power consumption of any flat-panel technology and are the best bet for very slim full-color flat panels. "That's not to suggest," Aizawa concedes, "that there isn't still a lot of work to be done to boost display size, improve image quality, and cut manufacturing costs before LCDs with 80 characters and 25 rows become commonplace."

Since joining the Seiko Group's Epson Corp. in 1956, Susumu Aizawa has an impressive array of firsts. He developed the company's first analog quartz watch, its first digital printing mechanism, and its first thermal transfer printer. He holds a degree in precision mechanical engineering from Tokyo University.

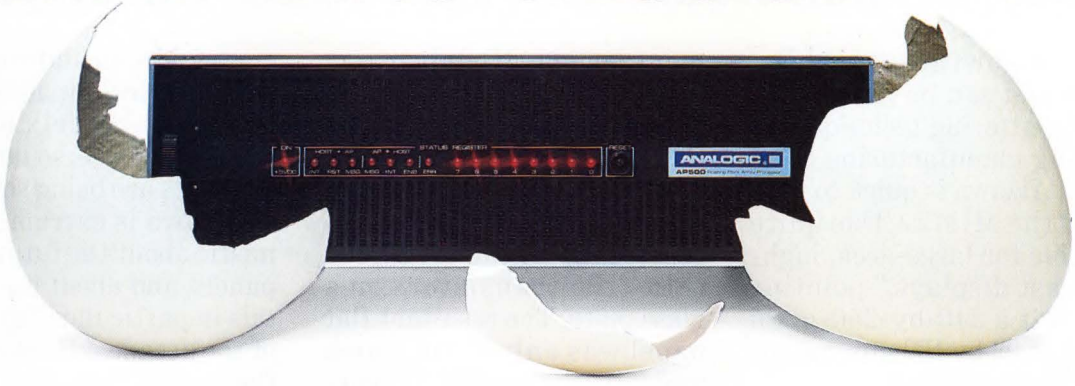
To lick one of the problems associated with LCDs will require an approach different from the conventional passive one. Aizawa amplifies on this idea: "The present multiplexing schemes are limited to scanning 100 lines. When a greater number must be handled, the contrast ratio and viewing angle suffer." Active elements, on the other hand, enable at least 500 lines to be scanned.

Two structures are under investigation. One works with thin-film transistors mounted directly onto a glass substrate. The other goes with a bidirectional diode structure. Although the first is more familiar, it is the second that Aizawa sees as holding out the greatest promise.

These so-called metal-insulator-metal (MIM) LCDs consist of a thin layer of tantalum pentoxide sandwiched between tantalum and chromium. The device requires

Martin Gold

THE BIRTH OF THE ARRAY PROCESSOR AGE



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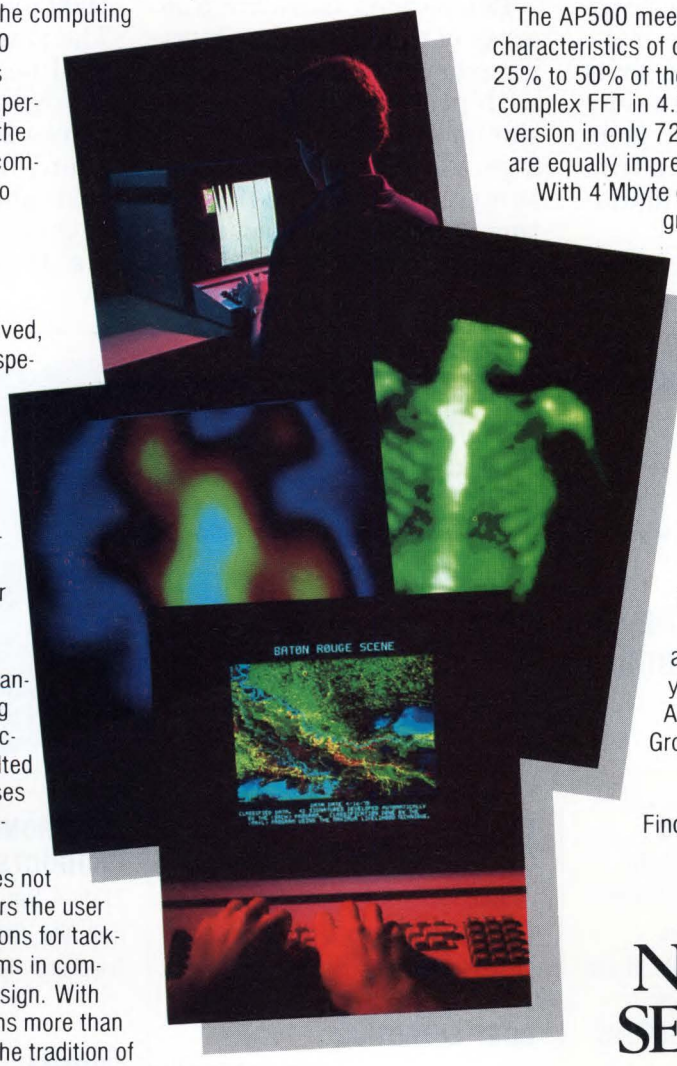
Now, the AP500 is here. It does not replace the AP400, rather it offers the user a new range of performance options for tackling increasingly complex problems in computer modelling, imaging, and design. With the AP500, state-of-the-art means more than computing speed. In continuing the tradition of cost-effective computing performance and innovative design, our engineers have even given the AP500 standalone capability.



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The AP500 meets or exceeds the performance characteristics of comparable array processors at 25% to 50% of their cost. It performs a 1024 pt. complex FFT in 4.68 ms, and a 50 X 50 matrix inversion in only 72 ms. Its other performance specs are equally impressive.

With 4 Mbyte of data memory, 384 kbyte of program memory, and high-speed bidirectional I/O capability, the AP500 can form the heart of a high-power computing work station. Its on-board co-processor means that it can even operate independently of a host computer for remote operations or applications which demand complex communication procedures, such as adding data block identifiers or handling packet protocols with incoming data.

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CIRCLE 37

VIEWPOINT

only two or three masking steps and can be fabricated with sputtering techniques—keeping manufacturing costs down. Aizawa is quick to note that "the MIM LCD is quite suitable for large-area, high-contrast displays," pointing out that a 240-by-250-pixel array of 99 by 100 mm has already been created.

Turning to the more traditional structure, Aizawa explains that when the active element in a thin-film transistor turns on, data is written into a pixel. When the element turns off, a charge is stored within that thin film device that drives the liquid-crystal materials.

Working with active elements, the LCD driver circuitry can be integrated onto the same substrate as the LCD, keeping a lid on cost. The secret of the pocket-sized color LCD TV was the successful formation of 57,600 thin-film transistors on a glass plate. The resultant flat panel was only 1/10 in. thick and 2 in. diagonally. It certainly could not have been produced with a CRT.

But, he adds, fabricating an array of thin-film transistors is no easy matter. It is created with processing techniques similar to those employed for 2-μm VLSI devices and is thus subject to the same limitations. That translates into a wafer with a maximum diameter of 6 in. In addition to the size restriction, assembling an active matrix array is quite expensive, so new active elements are being sought.

Aizawa is extremely optimistic about the future of flat panels, and about liquid crystals in particular. "By the end of the decade, I think we'll see flat panels that are the same size as today's CRTs and that resolve a maximum of 1000 by 1000 pixels—for graphics." The standard configuration will be a monochromatic 400-by-640-pixel array that shows 2000 characters. "By then," he concludes, "full-color and monochromatic arrays of 200 by 640 pixels will also be routine."□

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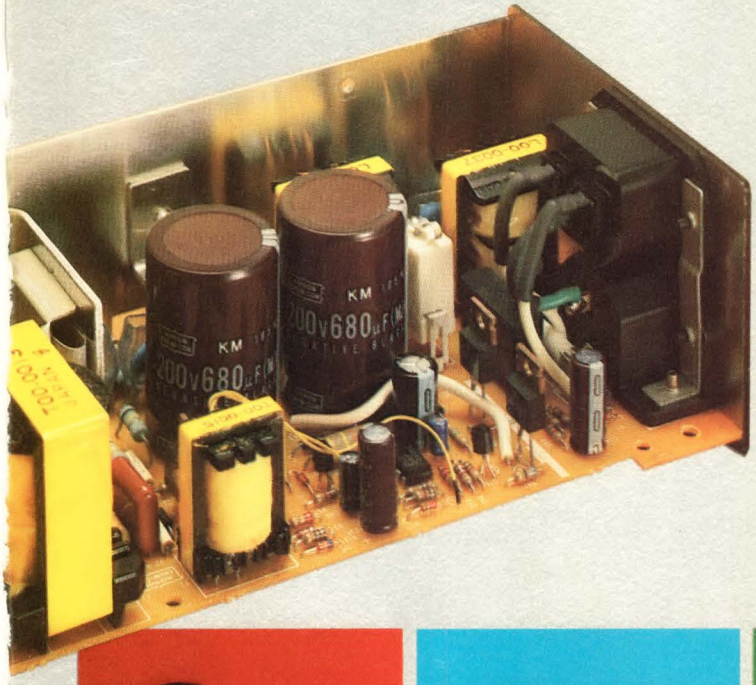

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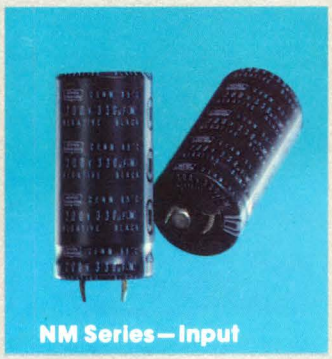
BK Series—Input

Low profile, high capacitance, high ripple in a small can.



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High capacitance in a low profile case size.

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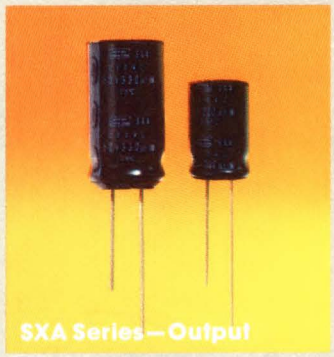
High ripple, up to 4 times the ratings of our general series.



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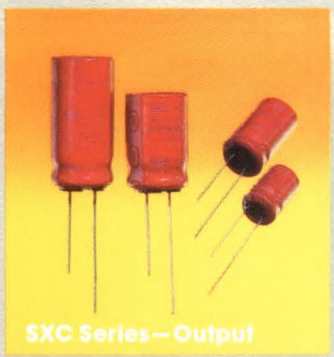
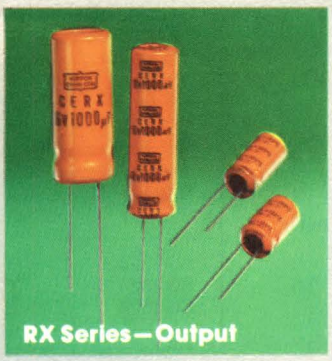
High performance, low impedance in a miniature size.



SXC Series—Output

Solvent-proof, low impedance, high ripple in a miniature size.



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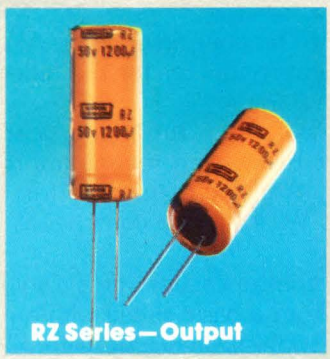
Low impedance, low ESR, long operating life in a small can.



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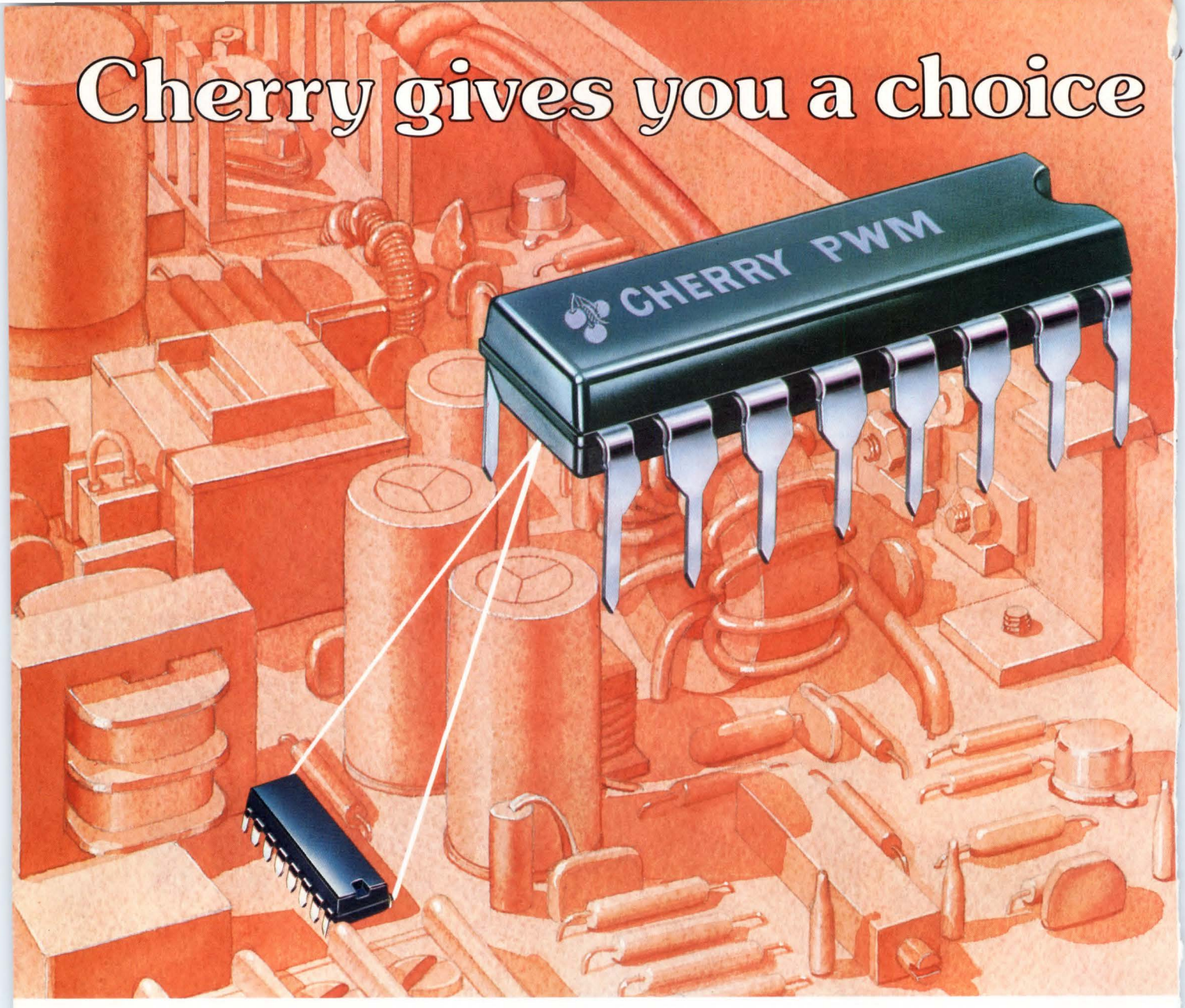

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SG1524 SG2524 SG3524	CS-1524 CS-2524 CS-3524		
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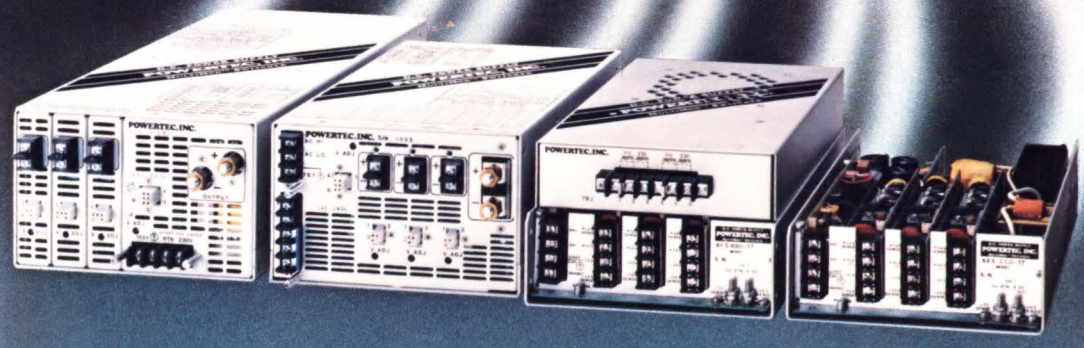

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MultiMod™ is a new concept in multiple output modular switching power supplies providing an alternative to costly customs. It allows you to choose your voltage/current combinations from a large selection of standard switching power supplies and standard auxiliary output modules, and we do the rest.

The MultiMod switchers have 2 to 7 fully regulated outputs, which consist of one main output and 1 to 3 fully isolated plug-in output modules. These output modules are off-the-shelf standards which the designer can select as building blocks to provide his ideal voltage/current combinations. He is assured of dependable delivery of supplies which exactly match his unique requirements. And MultiMods operate with proven field reliability because they are put together with standard building blocks produced in high volume.

Main outputs use only pure switch mode design. All auxiliaries are also available as fully switching. Thus, the designer can be assured of maximum efficiency and minimum thermal stress. Post-linear regulated auxiliaries are also available.

Multiple outputs are available from 2 through 48 volts with modules rated from 12 to 1000 watts. Total output ratings available are 300, 400, 600, 850, 1000, and 1200 watts.

MM7 October 1984

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Selector Guide–Multiple Outputs

See ValuSwitcher™ Family (19 Series) For Other Multiple Output Switchers.

The MultiMod™ is a new concept in multiple output switching power supplies providing 2 to 7 outputs. A building block approach using a selection of flexible "power packages" and standard plug-in output modules provides voltage/current outputs tailored to your specific requirements. The power supply is delivered totally assembled and tested, using the output modules you have selected to meet your needs.

- Select the "power package" that meets your total output power requirements (300 to 1200 watts) by referring to the "Power Package Selector Guide."
- Select the output with the highest output power by referring to the "Main Output Selector Guide."
- Select lower power outputs (auxiliary plug-in modules) by referring to the "Auxiliary Module Selector Guides."
- Each power package accommodates one main output plus space for up to three one-space-wide auxiliary modules.
- One-space-wide auxiliary modules are available with 1 and 2 isolated outputs.
- Column Two of the "Main Output Selector Guide" indicates the quantity of one-space-wide auxiliary modules that may be used with the main output indicated.
- "Auxiliary Spaces Occupied" column of the "Auxiliary Module Selector Guide" indicates the quantity of spaces each auxiliary module occupies (1 to 3 spaces).
- See "Order Information" (Page 3) for more details.

POWER PACKAGE SELECTOR GUIDE

Model Designation	Total Package Output Power[1,2,3]	Max. Power[1] 50°C		Max. No. Aux. Modules[13]	Number of Outputs[7]	Dimensions
		Main	Auxs[4]			
6E	300[5]	200[5]	200[5]	3	1 to 4	2.75" x 7.62" x 11.75"
6F	400	250	200	3	1 to 4	5" x 7.62" x 11.75"
6JA	600	384	250	3	1 to 6	5" x 8" x 11"
6JB	600	528	250	2	1 to 5	5" x 8" x 11"
6L	850	768	360	3	1 to 7	5" x 8" x 14.83"
6M	1000	768	360	3	1 to 7	5" x 8" x 14.83"
6MB	1200[17]	1000	360	3	1 to 7	5" x 8" x 14.83"

MAIN OUTPUT SELECTOR GUIDE

Model No.	Auxiliary[13] Spaces Available	Main Output Ratings				Load Regulation %	Ripple & Noise % P-P
		Volts[16]	Amps[1,2,3]				
			50°C	60°C	70°C		
6JA2-XXX-17	3	2	70	53	35	0.5	2.5
6JB2-XX-17	2	2	100	75	50	0.5	2.5
6L2-XXX-17	3	2	200	150	100	0.5	2.5
6M2-XXX-17	3	2	200	150	100	0.5	2.5
6E5-XXX-17	3	5	40[5]	30[5]	20[5]	0.2	2.0
6F5-XXX-17	3	5	50	37	25	0.2	2.0
6JA5-XXX-17	3	5	60	45	30	0.2	1.0
6JB5-XX-17	2	5	90	68	45	0.2	1.0
6L5-XXX-17	3	5	150	113	75	0.2	1.0
6M5-XXX-17	3	5	150	113	75	0.2	1.0
6MB5-XXX-17	3	5	200[17]	113	75	0.2	1.2
6JA12-XXX-17	3	12	28	21	14	0.2	1.0
6JB12-XX-17	2	12	42	32	21	0.2	1.0
6L12-XXX-17	3	12	62	47	31	0.2	1.0
6M12-XXX-17	3	12	62	47	31	0.2	1.0
6JA15-XXX-17	3	15	24	18	12	0.2	1.0
6JB15-XX-17	2	15	34	26	17	0.2	1.0
6L15-XXX-17	3	15	50	38	25	0.2	1.0
6M15-XXX-17	3	15	50	38	25	0.2	1.0
6JA24-XXX-17	3	24	16	12	8	0.2	1.0
6JB24-XX-17	2	24	22	17	11	0.2	1.0
6L24-XXX-17	3	24	32	24	16	0.2	1.0
6M24-XXX-17	3	24	32	24	16	0.2	1.0

NOTE: 3.3 volts main outputs and auxiliary outputs are available upon request. Contact Factory.

AUXILIARY MODULES SELECTOR GUIDE—SINGLE OUTPUTS

Module Designation[11]	Applicable Models[12]	Output Ratings				Load Regulation %[15]	Ripple & Noise % P-P	Aux. Spaces Occupied[8]
		Volts[16]	Amps[1,2,3]					
			40°C	50°C	70°C			
F	6E, 6F	2	6	6	3.0	0.2	3.0	1
K	6J	2	8	7	3.5	0.2	2.5	1
F	6J	2	11	10	5.0	0.2	2.5	1
K	6L, 6M	2	9	8	4.0	0.2	2.5	1
F	6L, 6M	2	15	15	7.5	0.2	2.5	1
M	6J	2	50	50	25.0	0.2	2.5	2
A	6E, 6F	5	6	6	3.0	0.2	2.0	1
L	6J	5	8	7	3.5	0.2	1.0	1
A	6J	5	11	10	5.0	0.2	1.0	1
L	6L, 6M	5	9	8	4.0	0.2	1.0	1
A	6L, 6M	5	15	15	7.5	0.2	1.0	1
B	6E, 6F	12	6	6	3.0	0.2	2.0	1
P	6J	12	8	7	3.5	0.2	1.0	1
B	6J	12	11	10	5.0	0.2	1.0	1
P	6L, 6M	12	9	8	4.0	0.2	1.0	1
B	6L, 6M	12	15	15	7.5	0.2	1.0	1
C	6E, 6F	15	6	6	3.0	0.2	2.0	1
U	6J	15	8	7	3.5	0.2	1.0	1
C	6J	15	11	10	5.0	0.2	1.0	1
U	6L, 6M	15	9	8	4.0	0.2	1.0	1
C	6L, 6M	15	15	15	7.5	0.2	1.0	1
D	6E, 6F	24	6	6	3.0	0.2	2.0	1
Y	6J	24	4	4	2.0	0.2	1.0	1
D	6J	24	8	8	4.0	0.2	1.0	1
Y	6L, 6M	24	4	4	2.0	0.2	1.0	1
D	6L, 6M	24	10	10	5.0	0.2	1.0	1
G	6E, 6F	48	3	3	1.5	0.2	2.0	1
G	6J, 6L, 6M	48	5	5	2.5	0.2	1.0	1

AUXILIARY MODULES SELECTOR GUIDE—DUAL OUTPUTS

Module Designation[11]	Applicable Models[12]	Output Ratings				Load Regulation %[15]	Ripple & Noise % P-P	Aux. Spaces Occupied[8]
		Volts[16]	Amps[1,2,3]					
			40°C	50°C	70°C			
R	6JA & 6JB	12	6/9 pk.	5/8 pk.	2.5	0.2	1.0	1
		12	6/9 pk.	5/8 pk.	2.5	0.2	1.0	1
T	6JA & 6JB	15	6/9 pk.	5/8 pk.	2.5	0.2	1.0	1
		15	6/9 pk.	5/8 pk.	2.5	0.2	1.0	1

NOTES:

1. Maximum continuous output power may not exceed the product of rated current and voltage (measured at the output terminals) specified in the Selector Guide at indicated temperatures.
2. Higher peak current ratings may be obtained. Contact Factory.
3. Maximum output power at 50°C of combined main and auxiliaries may not exceed the total package power indicated.
4. The combined power for all auxiliaries may not exceed power rating indicated.
5. Higher current and power ratings attainable with moving air (6E only).
6. "M" Auxiliary: Substitute "operating load current" for "rated max."
7. Number of outputs is determined by the output plug-in modules selected.
8. Numbers of spaces occupied by auxiliary module. Due to mechanical factors, 6JA and 6JB power packages are limited to no more than 2 "R" or "T" modules. Total number of outputs possible, including main, is therefore 6 and 5 outputs respectively.
9. 6J, 6L, 6M: Factory strapped for 230 VAC input. 6E, 6F: Factory strapped for 115 VAC input. Customer may change input strapping.
10. Class 1 Non-SELV: Meets European safety requirements except in cases where a system does not provide for grounding, or where the

All specifications are subject to change without notice.

Powertec Series 6 Specifications

See SuperSwitcher™ Family (9 Series) For Single Output Switchers From 400 to 1700 Watts.

ORDER INFORMATION/SPECIFICATION
Model/Product Description—Options

Standard Options

6 J A 5-B B D-1 7 X-B C D P G 2 3 4 5-SXXXX

- MultiMod™ Series Designation
- Package/Power
- Additional Designation Indicated on some main outputs
- Channel #1 Main Output Voltage 5V @ 60A
- Auxiliary Module[11] 12V @ 11A
- Auxiliary Module[11] 12V @ 11A
- Auxiliary Module[11] 24 V @ 8A

SAFETY SPECS (-1, or -2)

-1. Available all models
Meets UL 114, UL 478, UL 1012, CSA 22.2-143[14],CSA 22.2-154[14]
Hipot—Input to Output: 2100 VDC* 1500 VDC**
Input to Case: 2100 VDC* 1500 VDC**
Output to Case: 750 VDC* 500 VDC**
Creepage/Clearance—Primary to Secondary: 2.4 mm
Primary to Case: 2.4 mm
Case Grounded, Insulation Resistance—10MΩ
Leakage—1mA (3mA with Option B)

-2. Available all models
Meets all -1 specifications plus the following: Class I Non-SELV:
VDE 730[10],VDE 804[10],VDE 806[10],IEC 380[10],IEC 435[10]
Hipot—Input to Output: 3500 VDC* 1500 VDC**
Input to Case: 2100 VDC* 1500 VDC**
Output to Case: 750 VDC* 500 VDC**
Creepage/Clearance—Primary to Secondary: 3 mm
Primary to Case: 3 mm
Case Grounded, Insulation Resistance—10MΩ
Leakage—1mA (3mA with Option B)

*Qualification Type Test—May require disconnecting safety-agency-permitted components tied to case.

**Production Test

- Custom Options & Modified Standards
- 5: Parallel Option (Contact Factory)
- 4: Factory Wired 230 VAC (6E & 6F)[9]
- 3: CSA Logo[14]
- 2: Reverse Fan: 6J, 6L, 6M
- G: Power Good Option (6L & 6M only)
- P: Ball-bearing Fan
- D: Power Fail Option (all models)
- C: Cover Option: Applicable to 6E only, standard on others.
- B: EMI Filter—
  6E, 6F, 6J meet FCC 20780 Class A.
  6L and 6M (non-strappable 165-265 VAC input, version "3" only) meet FCC 20780 Class B and VDE 0871 Class A.
- X: Powertec assigned revision letter when applicable.
- 7: **INPUT VOLTAGES (3 or 7)**
  3. 165 to 265 VAC (47-63 Hz); 6L, 6M only
  7. 90 to 132 VAC (47-63 Hz) and 180 to 264 VAC (47-63 Hz) field selectable: 6E, 6F, 6J, 6L, 6M

Note: For 400 Hz operation contact factory.

SAFETY and INPUT VOLTAGE (See "Order Information" above.)

AC INPUTS

Brown Out—Regulates through short term line dips to at least 85 or 160 VAC.

Inrush Current—Limited to 4X operating current to prevent nuisance tripping of protective circuit breakers and fuses.

Turn On Time—0.2 sec. max. for power up.

Undervoltage Inhibit—Protected against malfunction due to AC undervoltage operation.

DC OUTPUTS

Adjustments—(± % of nominal voltage.)
All Main Outputs: ± 10%.
6J & 6M Auxiliaries; A, B, C, D, F, G: ± 10%.
6J & 6M Auxiliaries; K, L, P, U, Y: + 5%, − 2%.
All 6E, 6F & "M" Auxiliaries: ± 5%.

Line Regulation—6J, 6L, 6M: 5 mV or 0.1% over input range. 6E and 6F: ± 0.2% over input range.

Load Regulation—10 mV or 0.2% at any load up to 100% of rated load with remote sense connected; 0.2 mV/amp with internal sense; auxiliary modules with internal sense are 3 mV/amp.

Dynamic Response—A step load change of ± 25% of rated max[6] will cause a max. deviation of 3%. Output will recover to within 0.1% of nominal in 400 μsec.

Thermal Regulation— ± 0.02%/°C over operating range.

Ripple & Noise—See Selector Guide on page 2. Measured on 20 MHz scope via X1 probe having 4 inch maximum return lead.

Hold-up Time—Fully loaded outputs remain within regulation for 20 msec. minimum for the 6E and 6F following the last line voltage peak, measured from either 115 VAC or 230 VAC. Other values of hold-up are noted as follows:

HOLD-UP TIME vs. INPUT VOLTAGE (6J, 6L, 6M)

V_{in} CODE	7		3, 7			
NOMINAL VAC	90	115	165	180	208	230
HOLD-UP (msec.)	10	30	5	10	20	30

Efficiency—Exceeds 75% typically.

Loading vs. Temperature—100% rated load from 0 to 50°C. Derate linearly to 50% at 70°C.

Current Limiting—Foldback type, with automatic recovery upon removal of overload.

OVER VOLTAGE PROTECTION

OVP Inverter Shut-down (Standard)—All outputs: Initiates inverter shut-down and latches supply off. Trip point at output terminals are factory set within the following windows:

NOMINAL OUTPUT	2V	5V	12V	15V	24V	48V
TRIP WINDOW	2.8-3.2V	6.5-6.9V	14-16V	17-19V	27-29V	54-57V

Remove AC input for 30 sec. to restore operation.

OVP Crowbar—An SCR crowbar across the output terminals short circuits output to protect load against excessive voltage. 6E, 6F, 6L, 6M have crowbar on main outputs. 6E, 6F auxiliaries and 6J, 6L, 6M low current auxiliaries (e.g. P) also have crowbar. All others have inverter shut-down.

REVERSE VOLTAGE PROTECTION

Main outputs protected up to rated load. Auxiliary outputs protected to 50% rated load.

REMOTE SENSE

Separate sense terminals will accommodate a cable drop of 0.5 VDC. (See Note 1.) Internal circuitry protects load if sense lines are opened or shorted.

Margining: Fixed internal resistors can be installed to permit adjustments up to ± 10% for main output. Contact factory regarding auxiliaries.

POWER FAIL SIGNAL

(Option)—Following the loss of AC input, a TTL compatible signal referenced to the negative terminal of the main output will change from high to low at least 2 msec. before the loss of output.

POWER GOOD SIGNAL (Standard Option of 6L and 6M)

(Option)—A TTL compatible signal referenced to the main negative output terminal will change from high to low if the output voltage deviates more than ± 4% from nominal.

LOGIC INHIBIT

6J, 6L, 6M: A TTL high signal referenced to the negative output terminal inhibits the output; a TTL low, or open input, enables the output.

6E, 6F: TTL low inhibits output.

Total Power Supply: Shut-down all outputs when main output is inhibited. Standard on all models.

Auxiliary Output: 6L, 6M: Total shut-down of individual output.

6J: Less than 1 volt.

WARRANTY—1 year

possibility exists that an operator (maintenance personnel excepted) can come into physical contact with the power supply or its load terminals.

11. The Designation only represents the voltage and current output specs provided (NOT THE LOCATION). Powertec must determine the location of the auxiliaries.
12. Model (Power Package) in which the auxiliary module specifications are applicable.
13. Number of one-space-wide spaces available for auxiliary modules. Corresponds to "Auxiliary Spaces Occupied" column of the Auxiliary Module Selector Guide.
14. CSA logo added upon request. Powertec has been granted self-certification status by CSA.
15. When maximum auxiliary power is being used as shown in the Power Package Selector Guide, the load on the main output must be the following minimum percentage of the "Total Package Output Power" rating at 50°C: (6E: 8%), (6F: 6.5%), (6J: 10%), (6L, 6M: 7.5%). Lacking the above, auxiliary output voltages will decrease. Less minimum power on the main is required with reduced auxiliary loads.
16. Other voltages available on special order.
17. 40°C ratings. Hold-up time is 70% of specification. Minimum low line input voltage is 5% higher than specified.

MM7 October 1984

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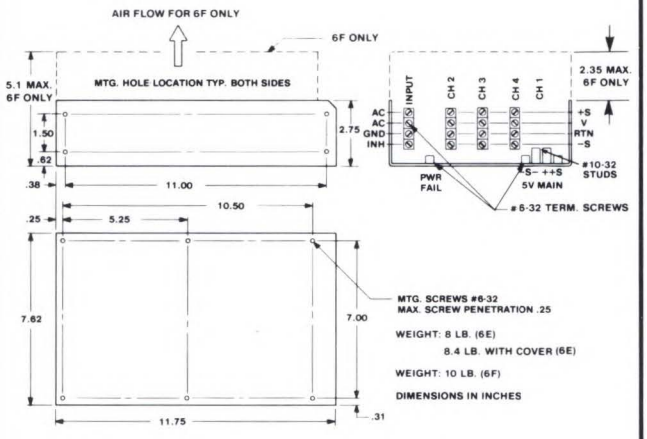
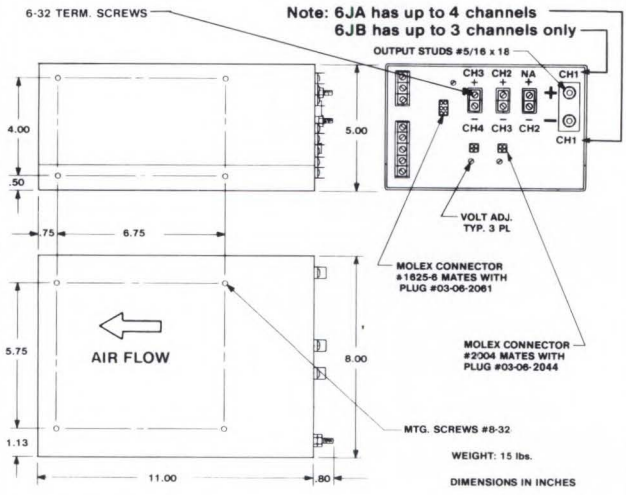
MultiMod Package Specifications

See SuperSwitcher™ Family (9 Series) For Single Output Switchers From 400 to 1680 Watts.
See ValuSwitcher™ Family (19 Series) For Other Multiple Output Switchers From 50 to 400 Watts.

MODEL 6E/6F

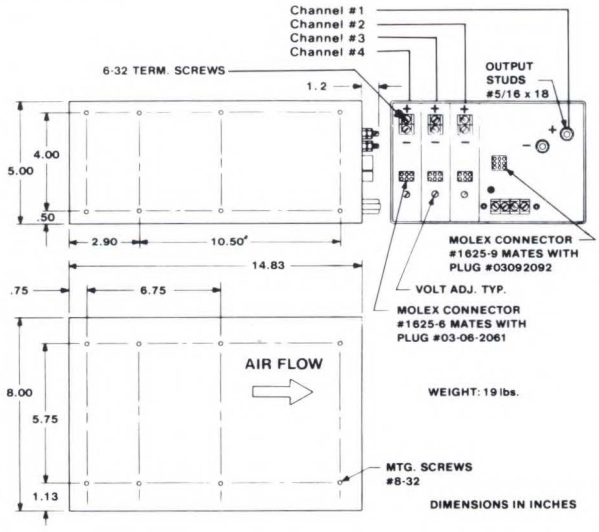


MODEL 6JA/6JB

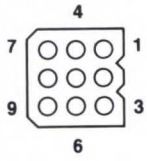


NOTE: The locations for the specified auxiliaries must be determined by Powertec.

MODEL 6L/6M



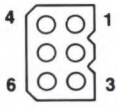
6L/6M MAIN



FUNCTION JACK (MOLEX) PIN-OUTS

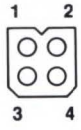
1. +Sense	4. –Sense	7. N/C
2. Program	5. N/C	8. N/C
3. Program	6. Inhibit	9. N/C

6J MAIN, 6L/6M AUXILIARIES



6J MAIN (CH.1)		6L/6M AUXILIARIES	
1. +Sense	4. –Sense	1. +Sense	4. –Sense
2. Program	5. N/C	2. N/C	5. N/C
3. Program	6. Inhibit	3. N/C	6. Inhibit

6J AUXILIARIES



1. +Sense	3. Inhibit
2. –Sense	4. N/C

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MM7 October 1984

POWERTEC
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"Fine Line" Circuitry: When You Need Conductors Finer Than A Human Hair.

Miniaturization marches on. When round wire became too heavy and bulky, flat cable and flex circuitry were developed. Now, density requirements can be too tough even for conventional flex circuitry. So that's where "Fine Line" takes over.

What it is. Circuitry, as shown above, with lines and spaces of less than .010. Our current production capabilities range down to .003. That's "Fine Line."

Where it's used. Satellite circuits, high-speed computer interconnects, cryogenic infra-red detectors, thermal imaging sights, mother board/daughter board interconnects, test equipment, and much more.

We're ready to work with you. Call your nearest Hughes rep, or phone us in Irvine. Our R&D people are at your service. Our circuitry is as fine as it comes. Today. The future? How about invisible conductors?

For more information phone Tony Piraino, 714-660-5788. Or write Hughes Aircraft Company, Connecting Devices Division, 17150 Von Karman Avenue, Irvine, CA 92714. In Europe, Hughes Microelectronics, Ltd., Clive House, 12-18 Queens Road, Weybridge, Surrey KT13 9XD, England.

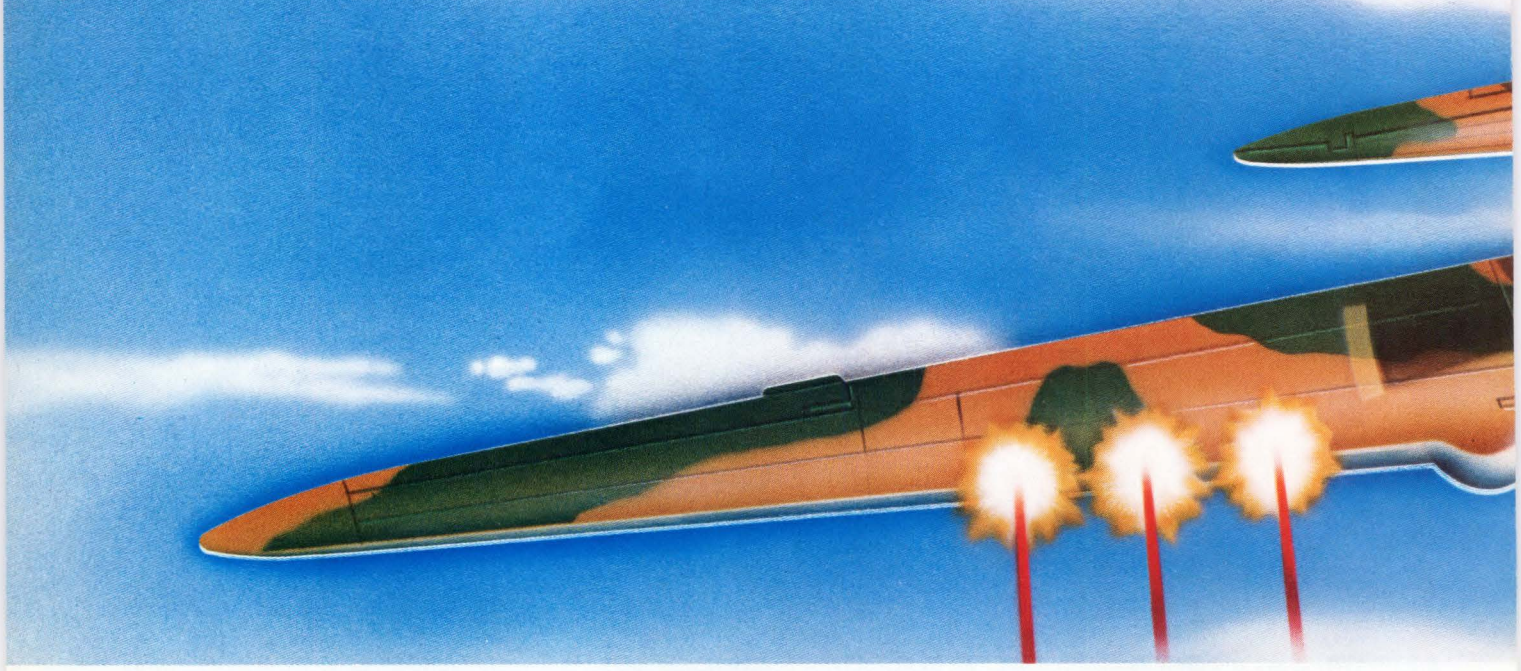
HUGHES
AIRCRAFT COMPANY

CONNECTING DEVICES DIVISION
Industrial Electronics Group

CIRCLE 42

1-800-5

Realism for your new entertainment



As an entertainment system designer, you know that today's electronics technology permits the generation of CRT-displayed graphics with all the fidelity of a first-quality color motion picture; but until now, not at a price economically feasible for low- and medium-priced entertainment equipment.

High-quality graphics generators have required a stack of printed circuit boards densely packed with SSI/MSI integrated circuits at a cost well beyond sensible budgets for low-cost microcomputer systems. This has caused the majority of graphics displays for popularly-priced entertainment systems to suffer from limited resolution and color selectivity.

New high-quality graphics at a remarkably low cost.

Entertainment systems can be vastly improved now with design-in support and low-cost technologies from Motorola. For colorful, high-resolution graphics in home video and computer games where realistic computer animation is needed, there's Motorola's cost-effective Raster Memory System (RMS). This available-under-$20 in-production-volume chip set at last makes professional, quality graphics affordable for your next entertainment system.

Using only two chips, the RMS, under MPU control, converts a graphics program stored in memory into the complex video stream that can produce high-quality displays on the CRT. At an astonishingly low cost. No longer is expensive static display RAM needed. The RMS utilizes system memory comprised of industry-standard DRAM with capacities ranging from 16K to 1M bytes.

With the RMS you can select 32 colors from a universe of 4096 shades to use on a virtual accommodating and smooth scrolling screen.

With the advent of the RMS, graphics quality is now primarily dependent on the sophistication of the software, the amount of memory available and the power of the MPU.

A range of MPUs for every entertainment application.

The RMS chip is designed to operate with a wide range of processors including three of Motorola's powerful MPUs: the 8-bit MC6809, the 8/16-bit MC68008 and the 16/32-bit MC68000.

Motorola's MC6809 MPU has the most complete set of addressing modes available on any 8-bit microprocessor today and interfaces with over fifty M6800 peripherals. In addition, you're never locked into a specific design with an upward source-code compatible instruction set.

The MC68008 MPU allows the design of cost-effective systems using 8-bit data buses while providing the system throughput benefits of a 32-bit microprocessor architecture. The performance of the MC68008 is greater than any 8-bit microprocessor and superior even to several 16-bit microprocessors.

The industry-leading MC68000 is a fully-implemented 16-bit microprocessor with 32-bit registers, a rich instruction set and versatile addressing modes.

With this line of compatible processors, you'll satisfy all the price/performance tradeoffs in your design requirements.

Modulators and encoders give the big picture.

For supplying signals to color monitors, Motorola supplies a full line of modulators and industry-standard encoder circuits.

The MC1374 is a TV modulator circuit that packs an FM audio modulator, sound carrier oscillator, RF oscillator, and RF dual input modulator all on one low cost chip. It is designed to generate a TV signal

21-6274.

design. Call now for design-in support.

from both audio and video inputs. The MC1374's wide dynamic range and low distortion make it particularly well-suited for applications such as video tape recorders, video disc players, TV games and subscription decoders.

The MC1377 is a color television RGB-to-PAL/NTSC encoder used to generate a composite TV signal from baseband red, blue, green and sync inputs. It is ideal for encoding signals from color cameras and graphics generators.

Opening new markets with AM stereo.

Radio designers are noting the significant advantages AM stereo has over FM in range of coverage and fade resistance.

Motorola's CQUAM® (Compatible Quadrature Amplitude Modulation) AM stereo decoder is a complete one-chip full-feature AM stereo decoding and pilot detection system. It employs full-wave envelope signal detection at all times for the L+R signal, and decodes L—R signals only in the presence of a valid stereo transmission. The MC13020P needs no adjustments, uses no coils and has few peripheral components.

In the absence of a good stereo signal, CQUAM® produces an undegraded monaural output for existing radios. When both channels are modulated the noise increase in stereo is a maximum of 3.0 dB . . . even less on program material.

Years of refinement have made Motorola's CQUAM® the leading contender in the race for a "world standard" in AM stereo systems. Even with four FCC approved competitors, Motorola's CQUAM® has captured more than 140 new AM stereo stations this year and leads in production with over nine major manufacturers.

Talk engineer to engineer.

Motorola has tripled the number of application engineers it has throughout the U.S. and Canada.

Each has the expertise in emerging semiconductor technologies that can electrify your new entertainment design ideas. Call 1-800-521-6274 and discuss your applications. Any time between 9 A.M. East Coast and 5 P.M. West Coast time, weekdays. Toll free. Talk to our specialists. They'll discuss your applications and get you in touch with a field application engineer who'll in person describe in depth how Motorola products can bring new excitement to your entertainment designs at minimum cost.

The RMS system can simultaneously display any 32 colors from its palette of 4096 colors in adjacent pixels. The above illustration is a continuous tone artist's representation.

CQUAM is a registered trademark of Motorola Inc.

1-800-521-6274

Wait'll you hear what we have in store for your new design. Be it in entertainment equipment, industrial or office automation, voice/data communication, or any other electronics-driven industry, we'll work with you at any level of chip, board or box integration through the industry's premier technical field organization.

A Motorola semiconductor field application engineer is in the right location with the right expertise to help you.

Call us on it.
One call. One source.
For all your semiconductor needs. Motorola Semiconductor Products, Inc.
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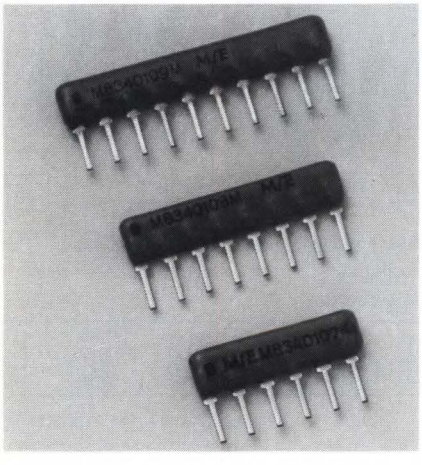
We're on your design-in team.

MOTOROLA

A New World of Products



Mil-Spec Approved
Low Profile Resistor Networks

- Mil qualification approval per MIL-R-83401 in all pin styles, /07 (6-pin), /08 (8-pin), /09 (10-pin)
- Both pull-up (C) and terminator (G) configurations
- Tolerances: F(±1%), G(±2%) and J(±5%)
- Temp coefficient // Resistance Range:
  K: ±100 PPM/°C // 47.5 to 1 MΩ
  M: ±300 PPM/°C // 10.0 to 1 MΩ

CIRCLE 135

Low ESR Computer Grade
Aluminum Electrolytic Capacitor–
Series 3189

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- Improved ripple current capability
- Operating life: 1000 hrs. at 85°C with full rated DC voltage
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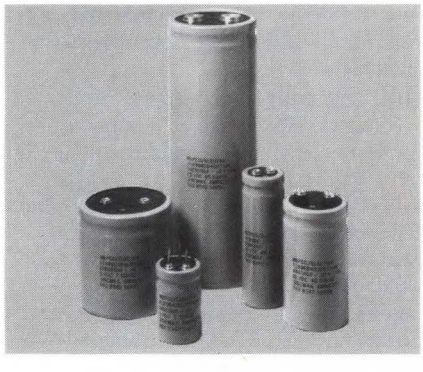
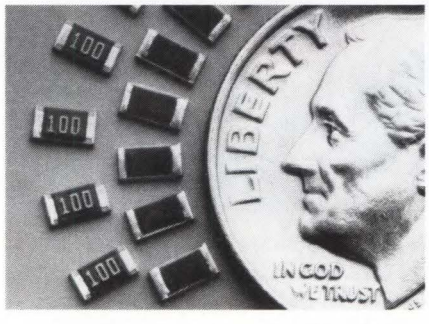
- Operating temp: −40° to +85°C
- Offered in PCB mounting configuration or with std. screw terminals
- A 2000 hr. long life version (Series 3190) also available

CIRCLE 136





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Array chip's eight cells build custom filters to eighth order and higher

In a method drawing on gate-array techniques, a switched-capacitor filter's properties can be spelled out during final metallization.

By specifying the separate parts of a switched-capacitor filter during the final metallization stage of a prediffused and prewired structure, an eight-cell CMOS array can create virtually any type of a filter—as high as the eighth order. A cascaded arrangement of the arrays can produce even higher-order filters.

The array chip drifts less and holds tighter tolerances than comparable filters, many of which depend on external resistors for the required filtering characteristics. Furthermore, unlike software-programmable filters, which demand registers and decoders, the cells also occupy far less chip space. Perhaps the most rewarding aspect, it slashes design time to one-fourth the six to eight months required for totally custom filters.

Developed at Thomson Semiconductors (Grenoble, France), the array chip can be cascaded in combinations of two basic cells: one for filters with an odd number of stages, the other for filters with an even number.

Mitch Beedie

With or without

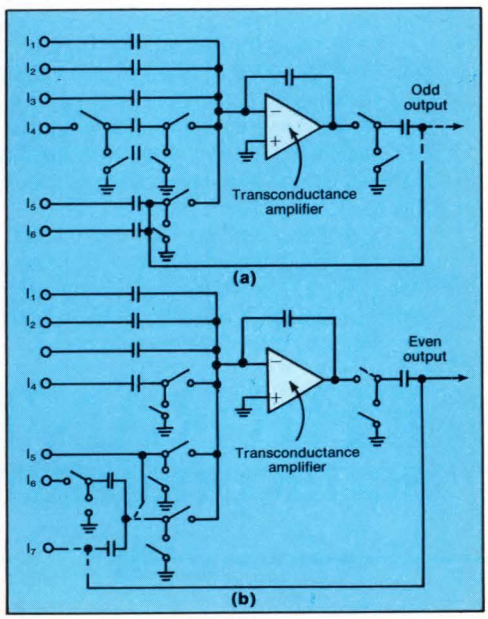
Each cell's inputs feed a CMOS transconductance operational amplifier and an integrating capacitor (see the figure). Inputs I_1, I_2 and I_3 can be weighted or added to or subtracted from one another. By connecting two clock phases from the on-chip generator to switches input lines I_4 through I_6 (or I_7 in even-stage filters), the inputs can be selected for inverting or noninverting integration, with or without a programmed delay.

A filter's cutoff frequency—ranging from a few hertz to about fifty kilohertz—is set by the ratio between the sampling frequency and the filter rate, both of which derive from an external oscillator. The internal clock generator is essentially a mask-programmable divider that converts the external clock into the filter's internal one. Internal level shifters work with TTL clock inputs.

Extra op amps

Two uncommitted op amps on the 8.5-mm^2 chip afford extra gain and output current. Alternatively, they can be used in prefiltering or postfiltering setups.

With the easily customized arrays, designers can create entire families of low-pass, high-pass and band-pass versions of Butterworth, Cauer, and Chebyshev filters. Thomson also plans to use the arrays for standard filters.□



To customize high-order switched-capacitor filters with an eight-cell array chip, designers can specify interconnections and capacitance value during final metallization of a cell for an odd number of stages (a) and for an even number (b). By connecting the chip's clock generator to switches, the outputs can be inverting or noninverting.

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BETTER BY DESIGN

CIRCLE 45

INTERNATIONAL MEETINGS

Cadcam International Show, Jan. 8–10. National Exhibition Centre, Birmingham, England. Peter Walker or Landy Hashimi, PWA, 32 Fitzroy Square, London W1P 5HH; (01) 388-9871.

Micro-Computer '85, Jan. 29–Feb. 3. Frankfurt, West Germany. Philippe Hans, German American Chamber of Commerce, 666 5th Ave., New York, N.Y. 10103; (212) 974-8856.

Middle East Electricity and Electronics Exhibition, Feb. 2–6. Jeddah Expo Center, Kingdom of Saudi Arabia. Len Bennett, Logistics, 237 Park Ave., 21st floor, New York, N.Y. 10017; (212) 551-3530.

AFIPS–Asia '84, Feb. 14–March 2. m.v. World Wide Expo, Tokyo, Osaka, Kitakyushu, Taipai, Hong Kong and Singapore. AFIPS, 1899 Preston White Drive, Reston, Va. 22091; (703) 620-8926.

Autotech Hong Kong '85, March 7–8. Hong Kong. Autotech Hong Kong '85, Hong Kong Productivity Center, 12th floor, World Commerce Center, 11 Canton Road, Tsimshatsui, Hong Kong; 3-7235656.

Componentes Electronicos '85, March 12–15. Mexico City, Mexico, March 19–22, Guadalajara, Jal., Mexico. Raquel Polo, United States Trade Center, Liverpool 31 Col., Juárez 06600, Mexico, D.F.; or PO Box 3087, Laredo, Texas 73044.

The Scottish Computer Show and Conference, March 12–14. Anderston Exhibition Centre, Albany Hotel and Holiday Inn Hotel, Glasgow, Scotland. Cahners Exhibitions Ltd., Chatsworth House, 59 London Road, Twickenham, London TWI 3SZ, England; (01) 891-5051.

China Tronic '85, March 14–19. Tianjin Exhibition Centre, Tianjin, Peoples' Republic of China. Asdale Exhibition Services, 109-111 Gloucester Road, 21st floor, Wanchai, Hong Kong; 5-8920511.

Comtel '85, March 18–20. Infomart, Dallas, Texas. Comtel '85, International Computer & Telecommunications Conference, 5080 Spectrum Drive, Suite 707E, Box 17, Dallas, Texas 75248; (214) 631-6482.

Automatic Testing and Test Measurement '85, March 19–21. Rhein-Main-Halle, Wiesbaden, West Germany. Network Events Ltd., Printers Mews, Market Hill, Buckingham, MK18 1JX, England; (0280) 815226.

Networking '85, March 23–31. Tokyo, Japan. Brad Ketchum, INC. Publishing Corp., 38 Commercial Wharf, Boston, Mass. 02110; (617) 227-4700 or Aki Tsurukame, Pacific Catalyst Group, 650 Grand Ave., Suite 1004, Los Angeles, Calif. 90017; (213) 614-0049.

IEEE Infocom '85, March 25–28. Washington, D.C. Celia L. Desmond, IEEE Infocom '85, Room 1855, 160 Elgin St., Ottowa, Ont., Canada K1G 3J4; (613) 239-4510.

Bit '85 Computer Show and Conference, March 26–29. National Exhibition Centre, Birmingham, England. Cahners Exhibitions Ltd., Chatsworth House, 59 London Road, Twickenham, London TW1 3SZ, England; (01) 891-5051.

Comdex In Japan, March 26–28. Tokyo International Trade Center, Tokyo, Japan. Milton Berns, The Interface Group Inc., 300 First Ave., Needham, Mass. 02194; (617) 449-6600.

32nd International Electronics, Energy and Aerospace Exhibition (Riena), March 26–31. Rome, Italy. Riena, Via Crescenzio 9, 00193 Rome, Italy; (06) 6569343/4/5.

Internepcon/Semiconductor International, March 27–30. Korea Exhibition Center (Koex), Seoul, Korea. Cahners Exposition Group, 7315 Wisconsin Ave., PO Box 7007, Washington, D.C. 20088; (301) 657-3090.

Unix Systems Expositions '85, April 2–4. Palais des Congres, Paris, France. Networks Events Limited, Printer Mews, Market Hill, Buckingham, MD18 1JK, England; (0280) 815226.

Electronics and Electrical Engineering Exhibition, April 17–24. Hanover, West Germany. Hanover Fairs, PO Box 338, Whitehouse, N.J. 08888; (800) 526-5978 or (201) 534-9044.

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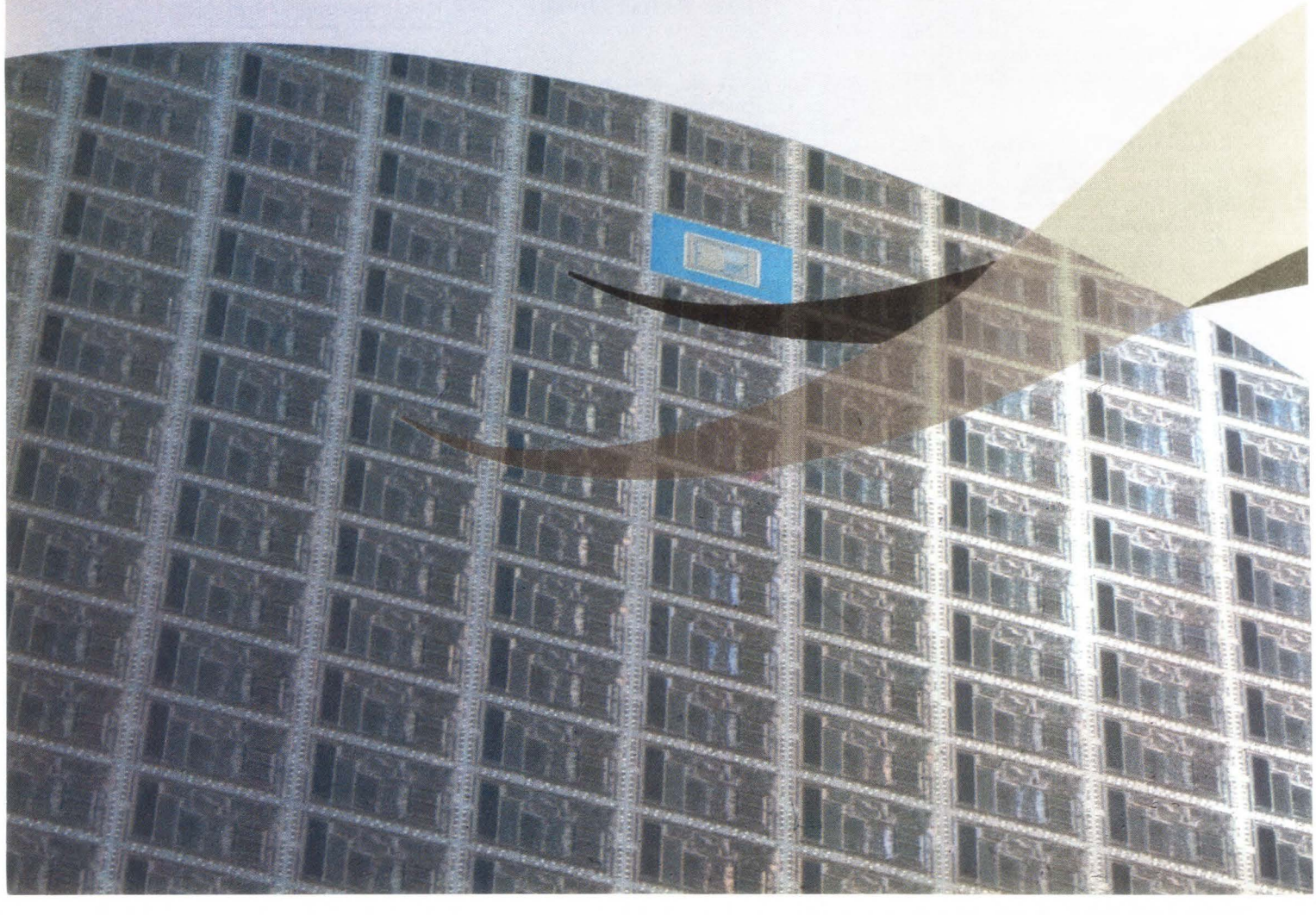

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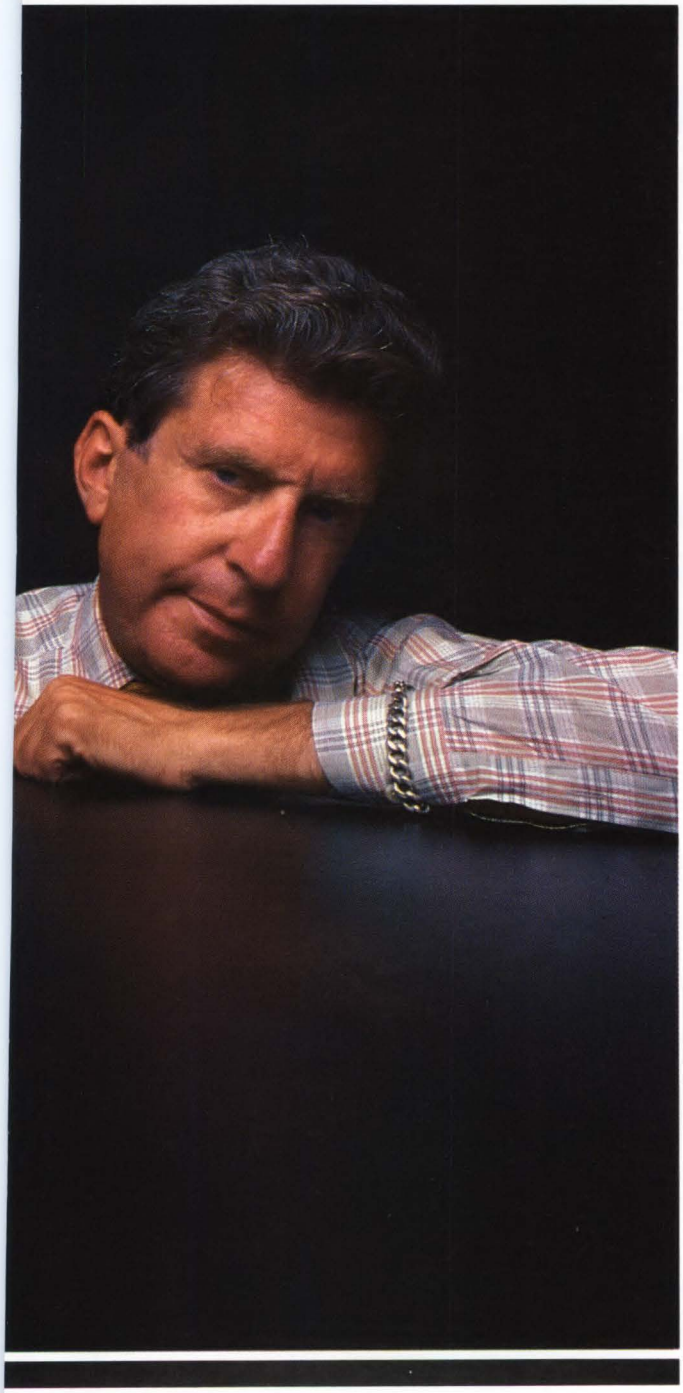

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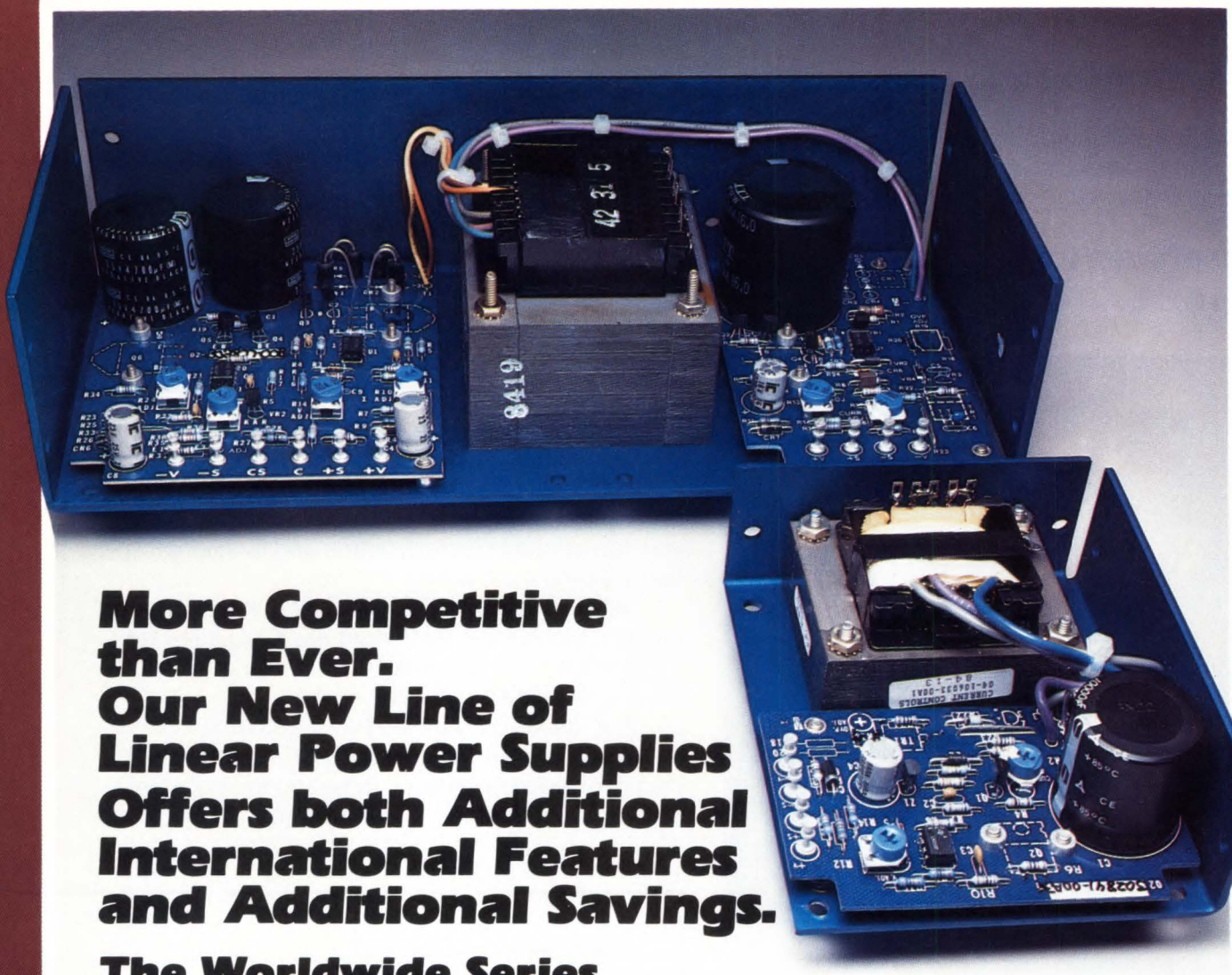

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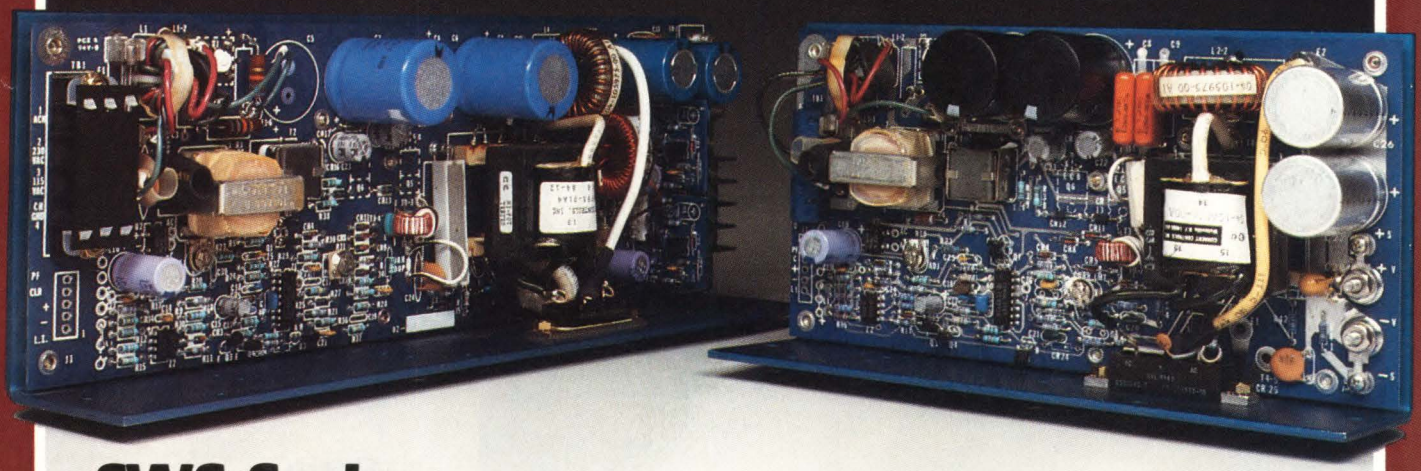

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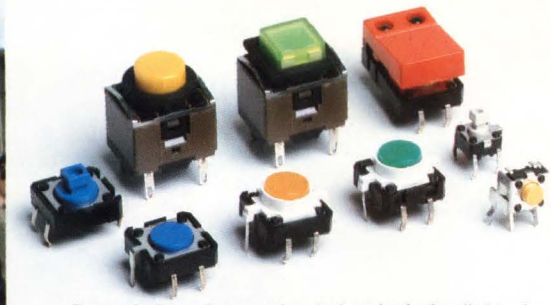

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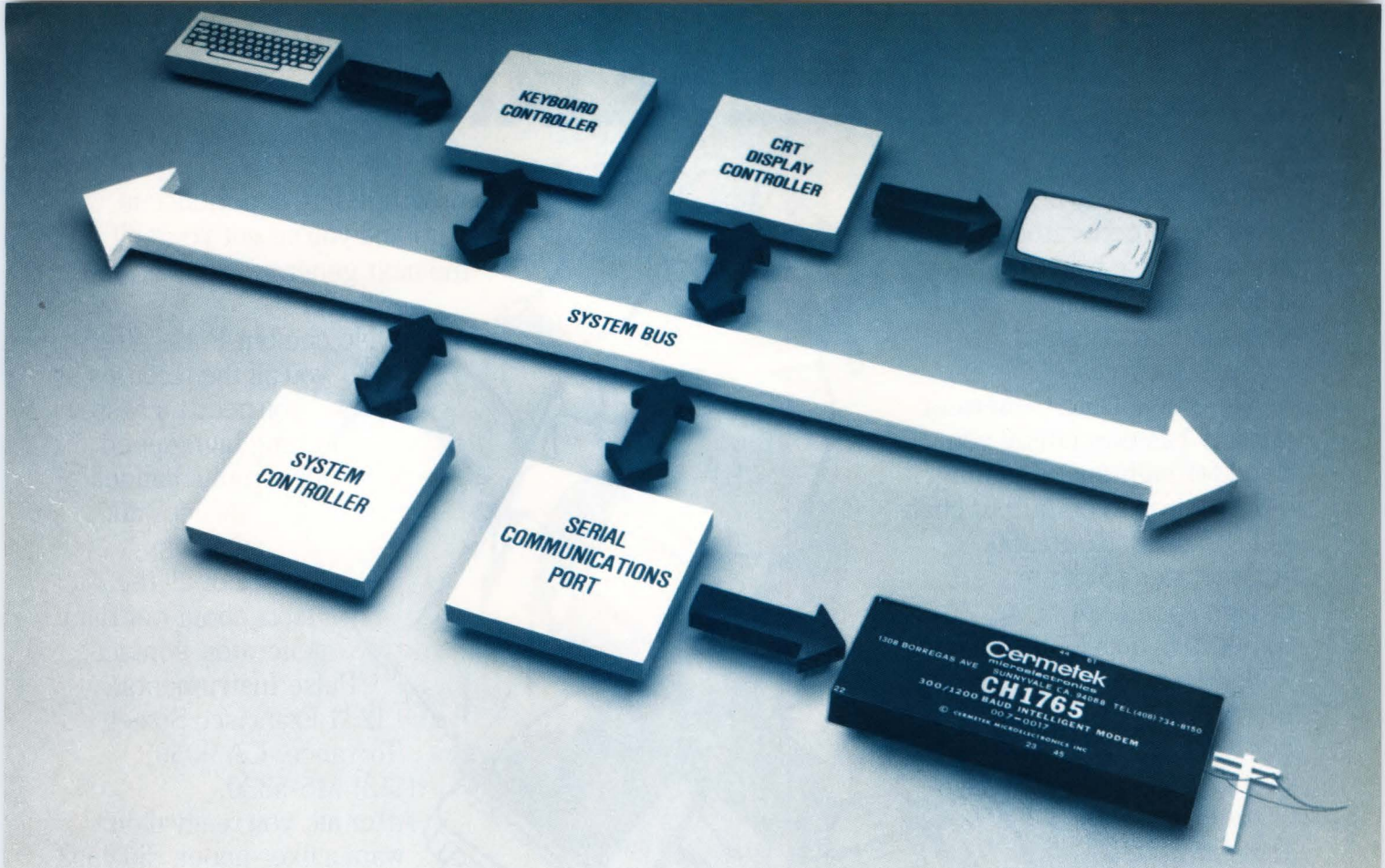

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CIRCLE 50

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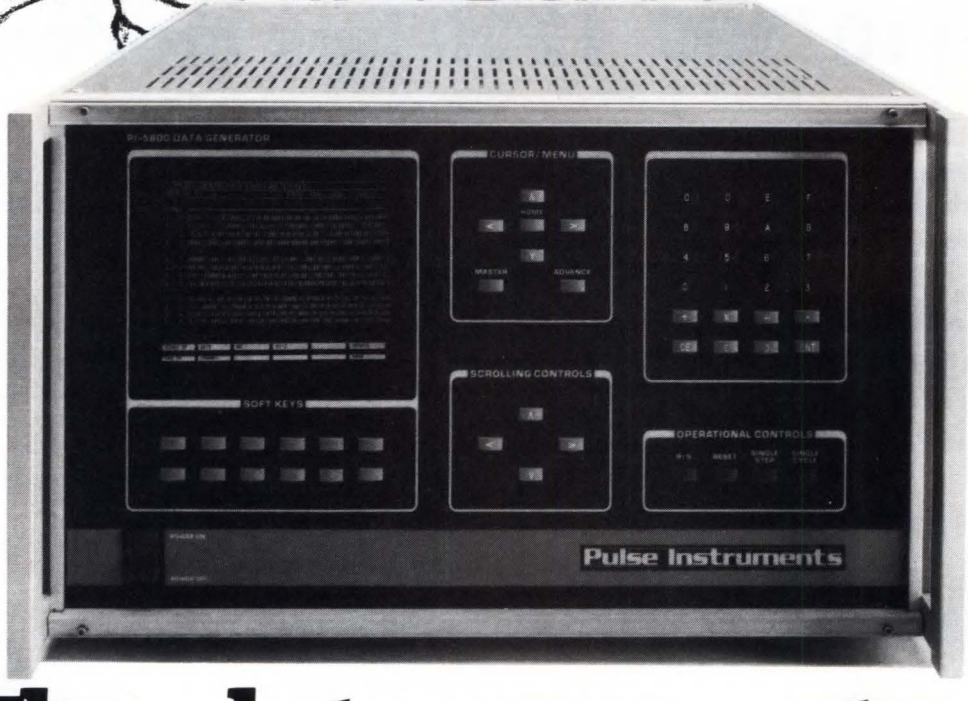

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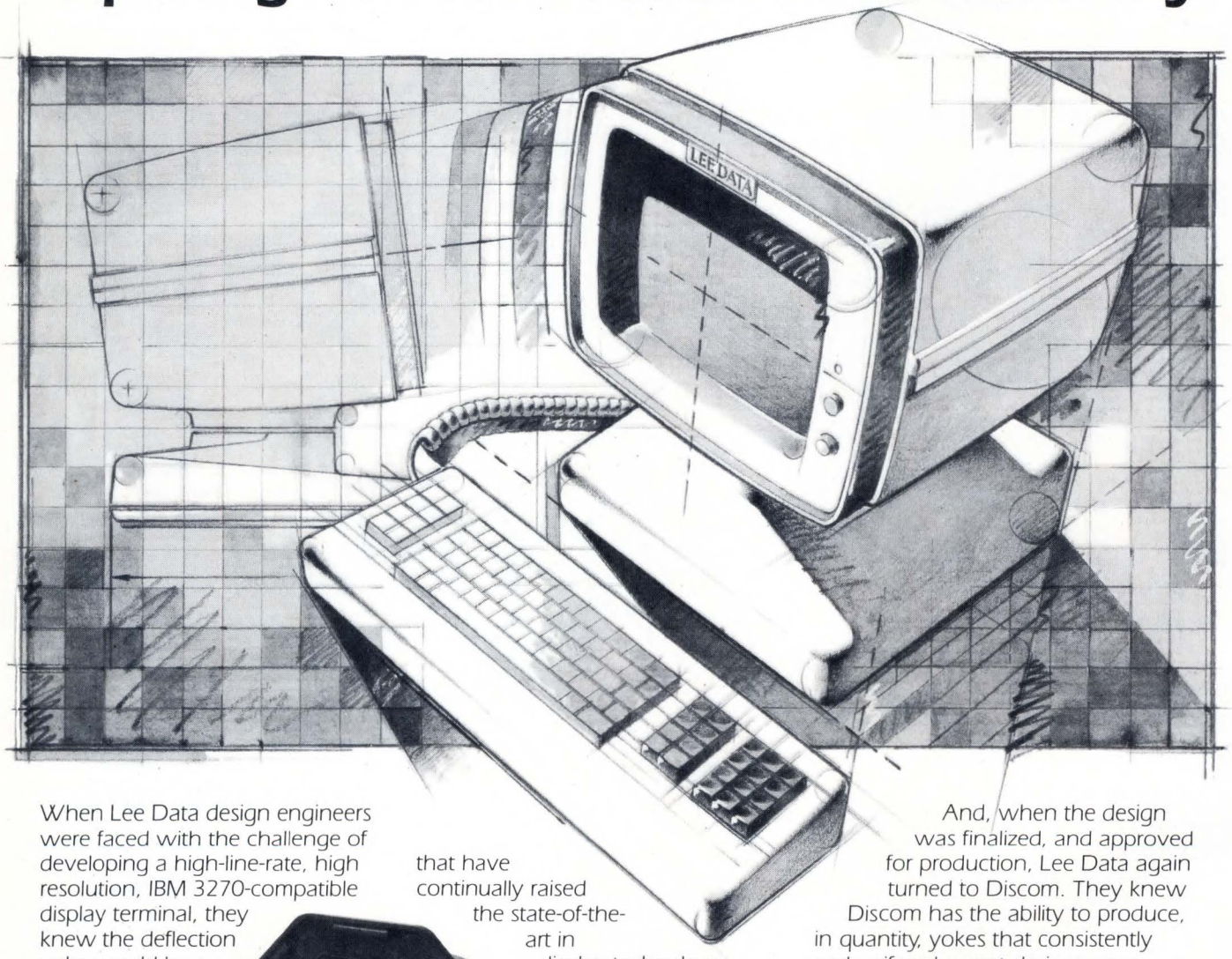
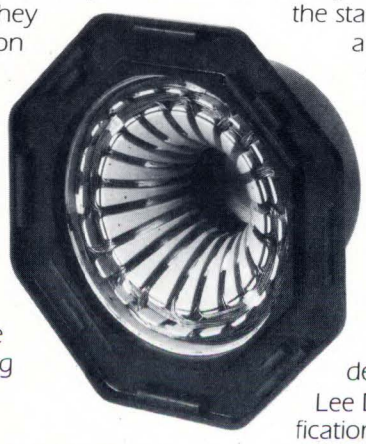


When Lee Data design engineers were faced with the challenge of developing a high-line-rate, high resolution, IBM 3270-compatible display terminal, they knew the deflection yoke would be a key component. They would require a yoke with geometry tolerance of less than 1% in production quantities. A yoke that would not require recorrection during final assembly in their plant.



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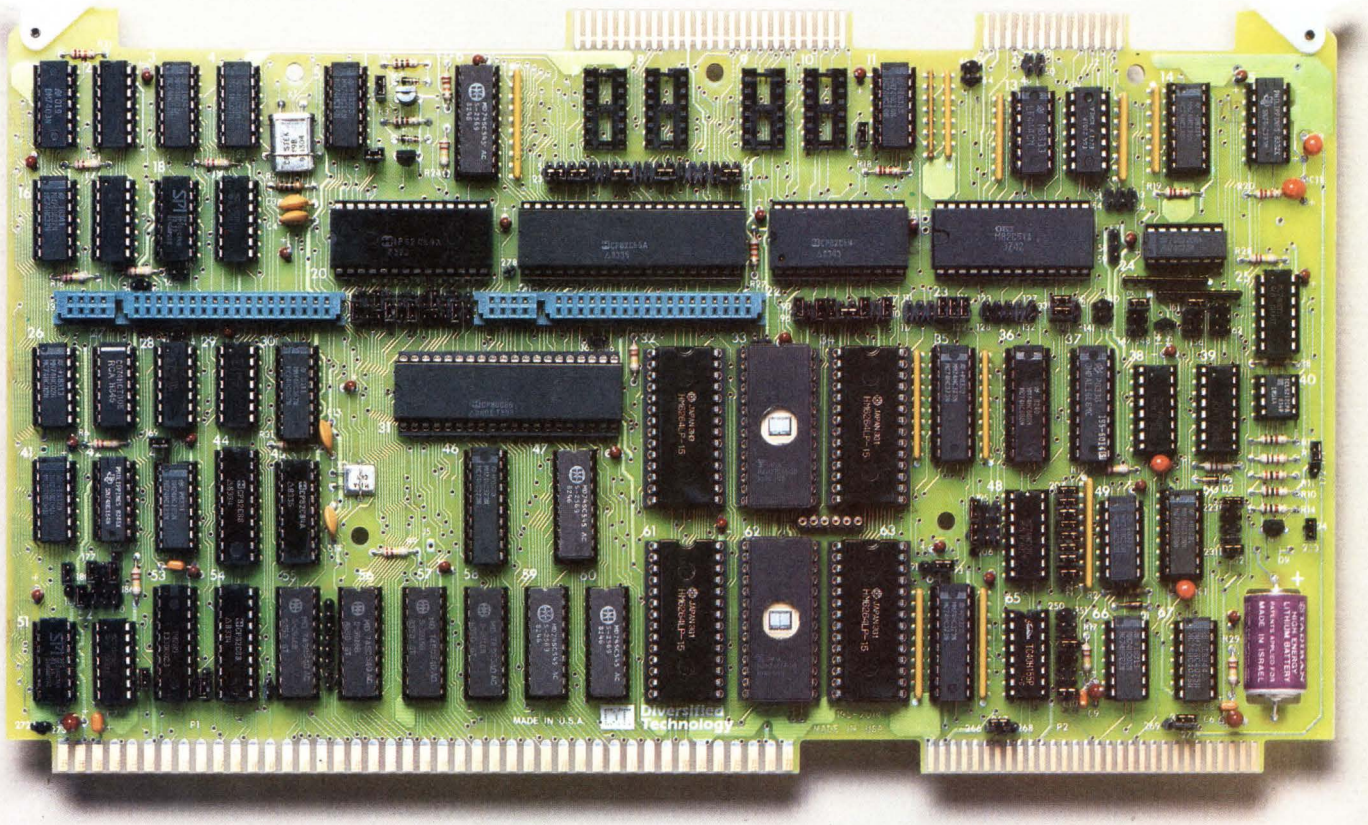

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	INTEL iSBC* 86/05	DIVERSIFIED TECHNOLOGY CBC 86C/05
Bus Type	MULTIBUS*	MULTIBUS*
CPU	8086	80C86
5V Operating Current	4.7 amps max.	200 milliamps max.
Operating Temperature	0°C to 55°C	0°C to 70°C
Supplied RAM (Bytes)	8K	16K
RAM Battery Back-Up On Board	No	Yes (2.5 yrs. data retention)

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CIRCLE 54

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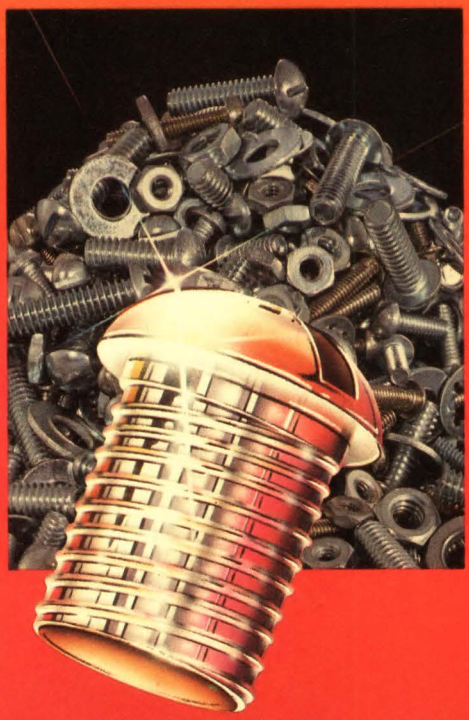

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CIRCLE 55

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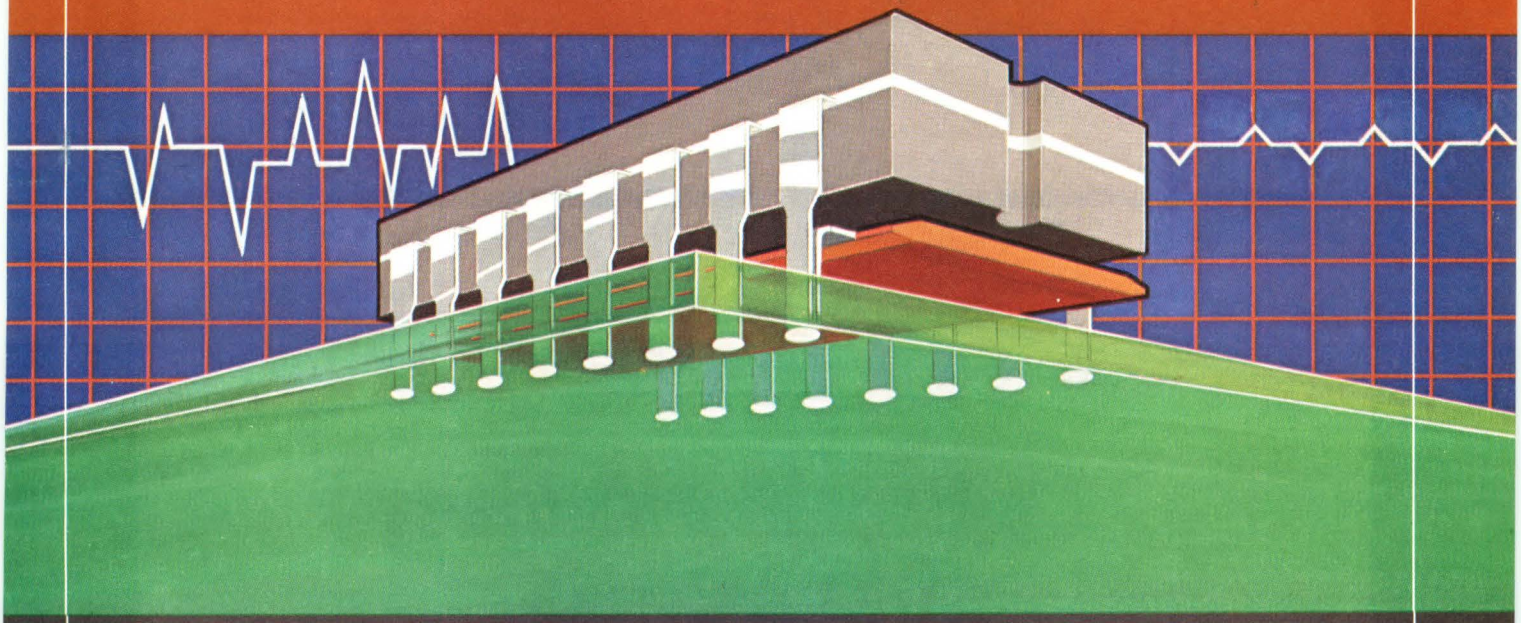

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CIRCLE 57

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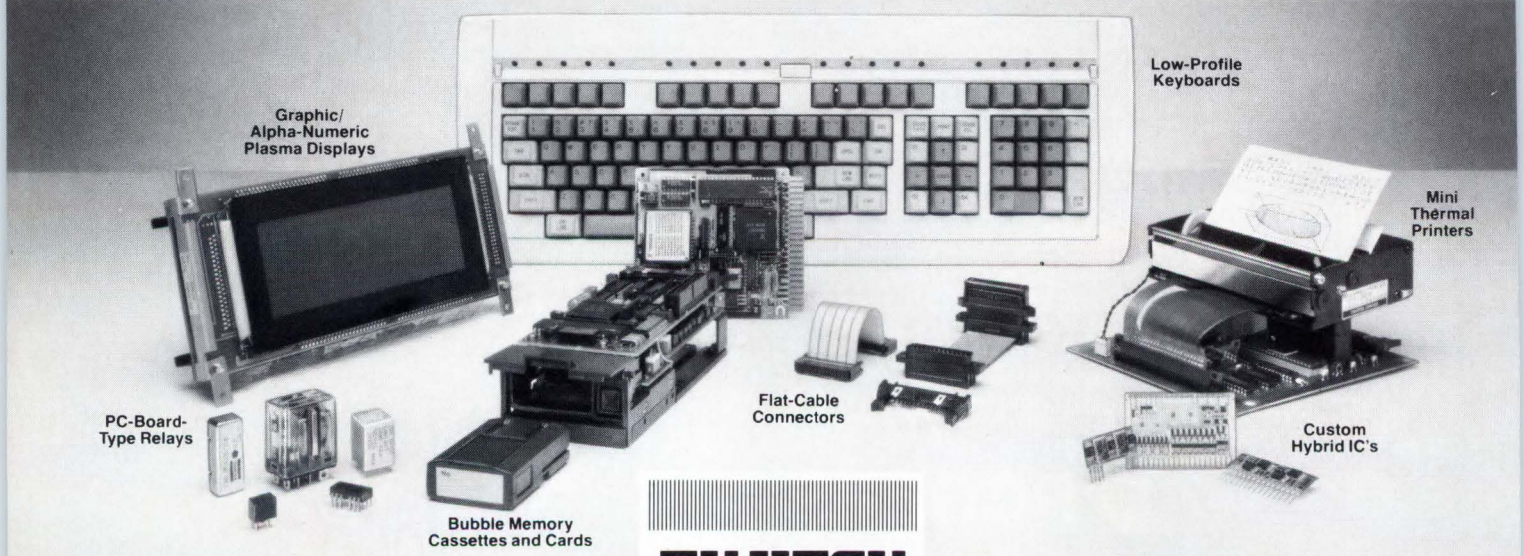

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TECHNOLOGY REPORT

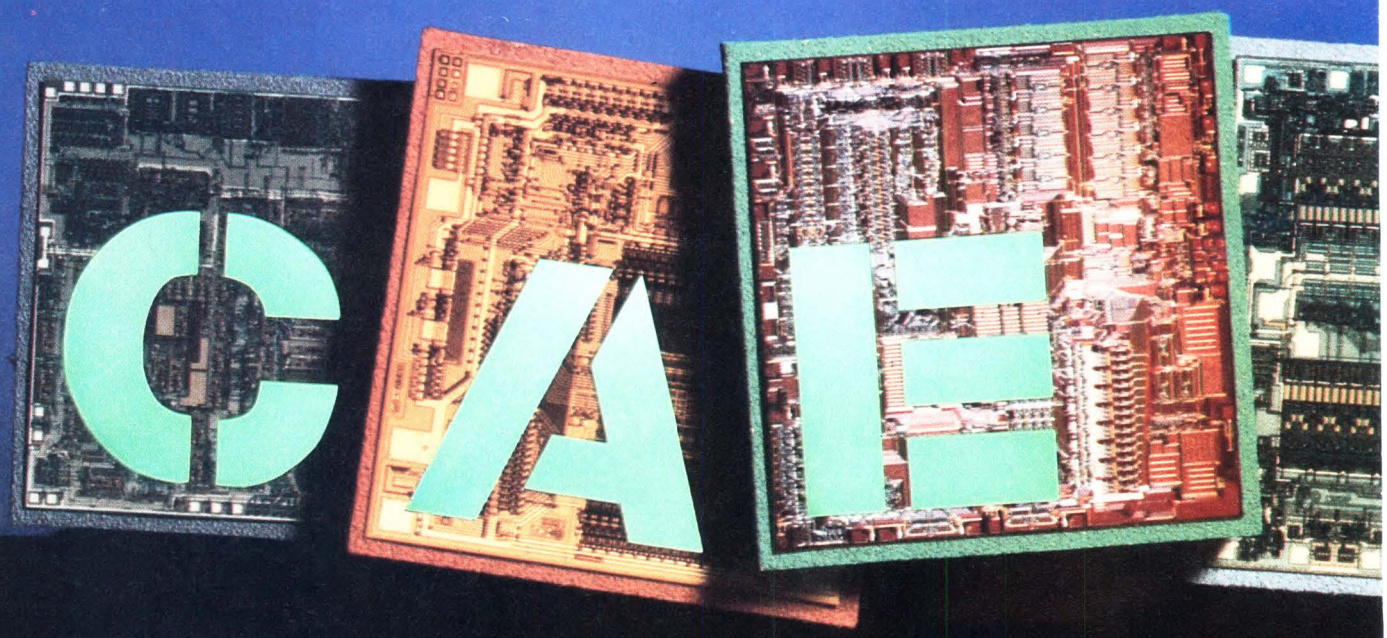
Transforming a simulated IC into silicon demands tools that unravel design decisions

This, the second of two reports on computer-aided engineering tools, picks up with the physical realization of application-specific ICs. The first part, which ran in the Nov. 15 issue (p. 128), explored design capture, simulation, and timing verification.

With the notable exception of some silicon compilers, IC design tools fall into two groups: those that help synthesize a chip's electrical design and those that help transform that design into silicon. The latter include software packages for automatic space allocation and routing, verification tools that check the layout against the simulator's net list, and circuit extractors that determine circuit parasitics and reannotate the simulation model with the corrected values.

The first IC design phase is completed when the circuit works properly on a simulator. Before the second phase can begin, however, a decision must be made on how to build the circuit in silicon. Usually the decision favors the least

Max Schindler

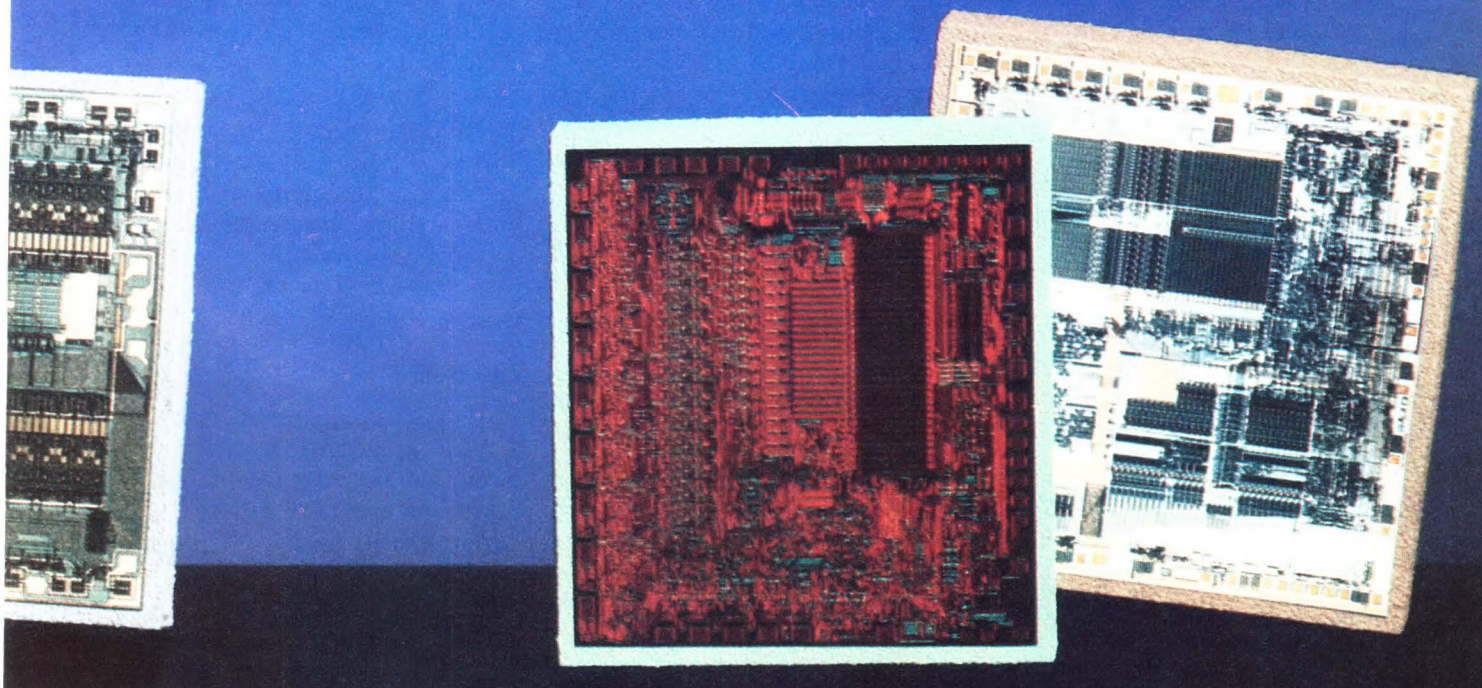


expensive alternative (Fig. 1), but the chip's specifications may dictate a costlier choice.

For example, if speed and chip size demand it, gate arrays must yield to standard or even custom cells. Economic considerations alone call for full-custom chips only in quantities of more than 50,000, but because only custom ICs can fully exploit advanced production technology, popular general-purpose chips will continue to be hand-optimized for another decade.

According to industry estimates, silicon compilation should become the best design choice for quantities under 10,000, but the technique is too young for hard and fast conclusions. Transistor density ranges somewhere between gate arrays and standard cells, although some designs have densities reaching 85% of custom chips.

For most OEMs, the alternatives narrow down to gate arrays or standard cells. Depending on the design and the technology, the crossover point between gate arrays and standard cells should be expected between a few hundred and a few thousand copies. But designers must keep in mind that gate arrays can rarely use all their gates — usually they provide only enough routing space to connect about 80% of them. When the designer is forced to go to the next larger size, silicon use can drop to 40% or so. Furthermore, if high speed is essential, more expensive double-metal arrays may be needed because they accommodate shorter routing paths. Some arrays also consist of uncommit-



ted transistors rather than gates; they permit the user to find the fastest combination for a given need.

For smaller systems, a type of hybrid technology is emerging as another alternative. It employs unpackaged ICs that are bonded to ceramic substrates. Space requirements average one-tenth of those for equivalent circuit boards, while costs run lower than those for gate arrays. Via Systems Inc. (North Billerica, Mass.) offers the SystemNode 120H especially for hybrid designers, and AutoMate Design Automation Systems (Palo Alto, Calif.) has developed an interface that adapts its hybrid design software, which normally runs on Data General hardware, to Daisy workstations (Fig. 2).

Because the software for pc board and hybrid design is quite similar to that for gate arrays, the same CAE systems can often be used for all three techniques, and even for standard-cell designs, as long as the cell shape remains fixed. However, because their connecting points are predetermined, hybrids and pc boards have another advantage: Designers need not worry about distributing bonding pads around the chip's periphery.

Down the auto route

Automatic routing packages usually consist of several programs for different levels of complexity. Usually, critical signals are routed first, which sometimes poses a problem in arrays having a single layer of metal, where contacts are often placed in fixed locations. The usual channel-routing algorithms also run into trouble with arrays that have no channels but that interconnect directly atop the active areas.

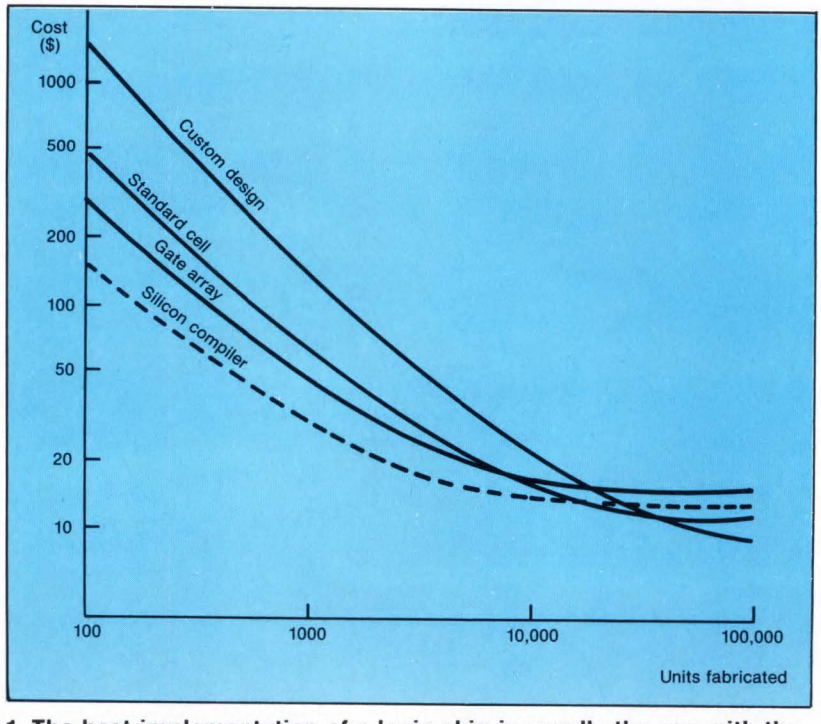
Start with the pins

Another algorithm used in first-pass routing starts with both pins to be connected and then searches in the X and Y directions until a connection is formed or an obstacle encountered. In the latter case, the "line search" algorithms retrace and try again in a direction perpendicular to the one just tried.

Remaining connections are completed by a "maze router" which propagates imaginary "waves" from one point to another, along rectangular approximations to polar coordinates. When the target point is reached, the router determines the wiring path along the unoccupied grid points that it found as the "wave" propagated.

Rip it up

If the maze router cannot find a path, the rip-up-and-retry program goes into action. After removing the blocking connection, this algorithm first routes the connection that was blocked and then tries to find another path for the link it ripped up. If that fails, it restores the original connection and asks for human intervention. The Cadisys software developed by Mentor Graphics Corp. (Beaverton, Ore.) permits

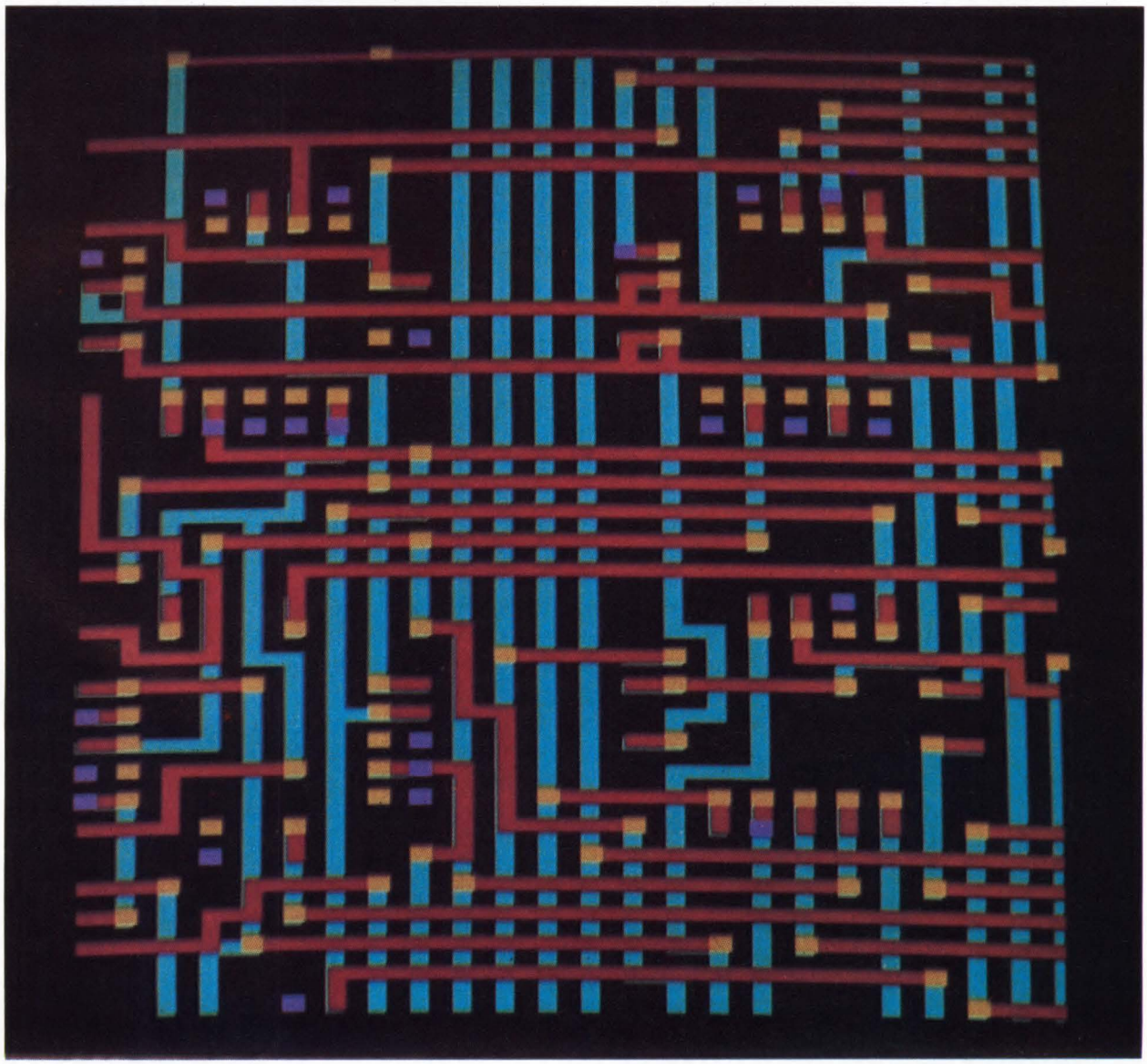


1. The best implementation of a logic chip is usually the one with the lowest cost. Standard cells and gate arrays now run neck to neck, but silicon compilers could make custom chips quite competitive.

such intervention either before or after autorouting—in the first case to assure preferred placement for the most critical cells, in the second to complete routing. Gould AMI Semiconductors (Santa Clara, Calif.) reports that Cadisys usually completes 95% of the networks in a typical 500-network circuit on single-metal gate arrays.

Because nearly all gate-array vendors offer layout support, the user can transfer the electrical design to the supplier if his or her own CAE system cannot handle routing. For example, LSI Logic (Milpitas, Calif.) executes its 400,000-line software on a mainframe that handles 5 million instructions/s—easily outrunning workstations. The lack of a circuit description standard complicates this step, but translation software from one supplier's net list to another's is usually available (see "EDIF Standard Running on Fast Track," p. 123).

Standard-cell design has been following gate arrays into today's singly powerful workstations. A system like



2. Hybrid technology links ICs in a manner similar to pc boards, but the interconnections are produced on ceramic substrates, to which the ICs are then bonded (magenta pads).

the Daisy Logician can indeed handle complex circuits (Fig. 3). But lack of in-house CAE need not deter an engineer—standard-cell design and layout can usually be done at a foundry's design center or on a simple workstation that acts as a terminal for the foundry's mainframe. In fact, with the number of standard-cell makers now at about 20, workstation users cannot expect to have even the major suppliers' offerings in their libraries. Still, the choices continue to proliferate—about half the standard-cell makers have not only parts with the common 3- to 5-ns gate delay, but also 1- to 2-ns parts. Others also list a line of cells with gate delays between 10 and 15 ns.

No experience needed

RCA Corp.'s Solid State Division (Somerville, N.J.) is one company that vows to turn engineers into standard-cell designers—in three days. In cooperation with Hamilton Avnet (Culver City, Calif.), a distributor of electronic components, the company plans to open 12 design centers within a year to assist designers throughout the country. By the way, several companies, including Texas Instruments Inc. (Dallas), RCA, and NCR Corp. (Dayton, Ohio), include analog cells in their libraries.

RCA's design process is straightforward (Fig. 4a). A user can develop the circuit on a workstation running a program that converts the design into the RCA format—for example, the Daisy Logician. After downloading, RCA's Mimic simulator goes over the circuit once more to make sure it complies with RCA requirements and to add fault coverage. If testability is inadequate, the user is notified. A separate fault coverage analyzer and the Scoap testability routine, the latter from Sandia National Laboratories (Albuquerque, N.M.), are available on RCA's workstations.

Under Mimic, rise and fall delays are expressed as functions of load capacitance, thereby assuring accurate timing. Components can either be called up from the library or described in the Mimic language (Fig. 4b).

After format conversion, the APRA automatic placement and routing system takes over. It either runs automatically or accepts preplacement inputs to improve density or keep critical signal paths short. Algorithms that automatically handle such preplacement may soon emerge, if work at Sandia Laboratories and elsewhere is successful. The designer can add circuitry from a Calma workstation, in which case a program called Critic performs a comprehensive electrical-rule check.

Working in concert

The next step—design verification—is perhaps the most critical in the whole design process. A program must check the final schematic for correctness and determine the actual interconnect loading for another simulation run. At RCA, this program is called Concert (Connectivity Certification) because it actually checks the current net list against the one on the Mimic file. Photomask generation then completes the design process.

An ideal system would go even further. Mitsubishi Electric Corp., for example, has developed in its Itami and Karakura laboratories the software to reconstruct the complete circuit from photomask patterns—not an easy job in any case. However, as fabrication technique approach the submicron region, parasitics become critical enough to warrant the extra step.

Mitsubishi calculates gate, diffusion, and junction capacitance from both the parallel and the perpendicular overlap of the (double-metal) geometry adjacent to each transistor. Toshiba Research and Development Center (Kawasaki) follows much the same path with its timing verifier, Mactis.

A circuit extractor, as such programs are called, was also developed at the Massachusetts Institute of Technology (Cambridge). Dubbed EXCL, it uses field equations to compute both resistance and capacitance. Not surprisingly, calculations for even a 100-transistor circuit, decomposed into 1500 rectangles, take about a minute on Digital Equipment's System 2060.

Such precautions will become especially important for cells with user-defined parameters, which are used, for example, by VLSI Tech-

EDIF standard: running on the fast track

While the number of players in the lucrative field of CAE keeps growing, more and more time—the engineer's, the CPU's—is spent converting one supplier's formats into another's. Recognizing the urgency of the problem, the leading contenders are delegating some of their brainpower to come up with the Electronic Design Interchange Format.

EDIF represents not so much a language in the sense of hardware definition languages, but a format that accommodates specific languages. It will cover all levels of application-specific IC design, from functional definition to geometric description. Version 1, though, specifically addresses gate arrays and standard cell, including macro libraries and technology information.

Logic and circuit models, macrocell layout, schematic symbols, and base arrays (including plug and socket information) all must be relayed in program form from the foundry to the user, before the design can start (Fig. A). The designer, on the other hand, must send the foundry—or a remote computer, if the design exceeds 3000 to 8000 gates—net lists and layout information (Fig. B).

Behavioral description will be tackled later, as will some aspects of full-custom IC design. After all, IC makers all have their in-house standards and few others design custom ICs at present.

The EDIF heavyweights did not start with a blank slate: The University of California at Berkeley's Lisp-like CIDF (common interchange description format), Daisy's Gail (gate-array interface language), and Texas Instruments' Tidal (TI design automation language) represented de facto standards for which a common denominator had to be found. Work on the EDIF has advanced so rapidly that some companies are planning to adapt the as-yet-unendorsed standard as early as next year. Right now, no official standards body has announced plans to review EDIF, but chances are that the IEEE will turn the current EDIF proposal into an official standard.

```
(Cell NAND2
 (View Topological Logic
  (Interface
   (Declare (INPUT PORT a b) (OUTPUT PORT z))
   (Body (Figure Group SchematicSymbol)
    (shape (20 0) (arc(40 0) (60 20) (40 40)) (20 40))
    (circle (60 20) (70 20))
      )
   )
   (PortImplementation a (Figure Group SchematicPort
                          (Path (0 30) (20 30))))
   (PortImplementation b (Figure Group SchematicPort
                          (Path (0 10) (20 10))))
   (PortImplementation z (Figure Group SchematicPort
                          (Path (70 20) (90 20))))
   (Permutable a b)
   )
   (Contents
   (Instance Nand2Primitive)
    )
   )
   (View Physical
    (Interface
    (Declare INPUT PORT a b) (OUTPUT PORT z)
    (Body (Figure Group MetalBlockage (Rectangle...)))
    (PortImplementation a (Figure Group Poly...))
    (PortImplementation b (Figure Group Poly...))
    (PortImplementation z (Figure Group Poly....))
    (Permutable a b)
    )
    (Contents
     (Figure Group Metal (Path...) (Polygon...)...)
     (Figure Group Poly (Path...) Path...)...)
    )
   )
)
```

(A)

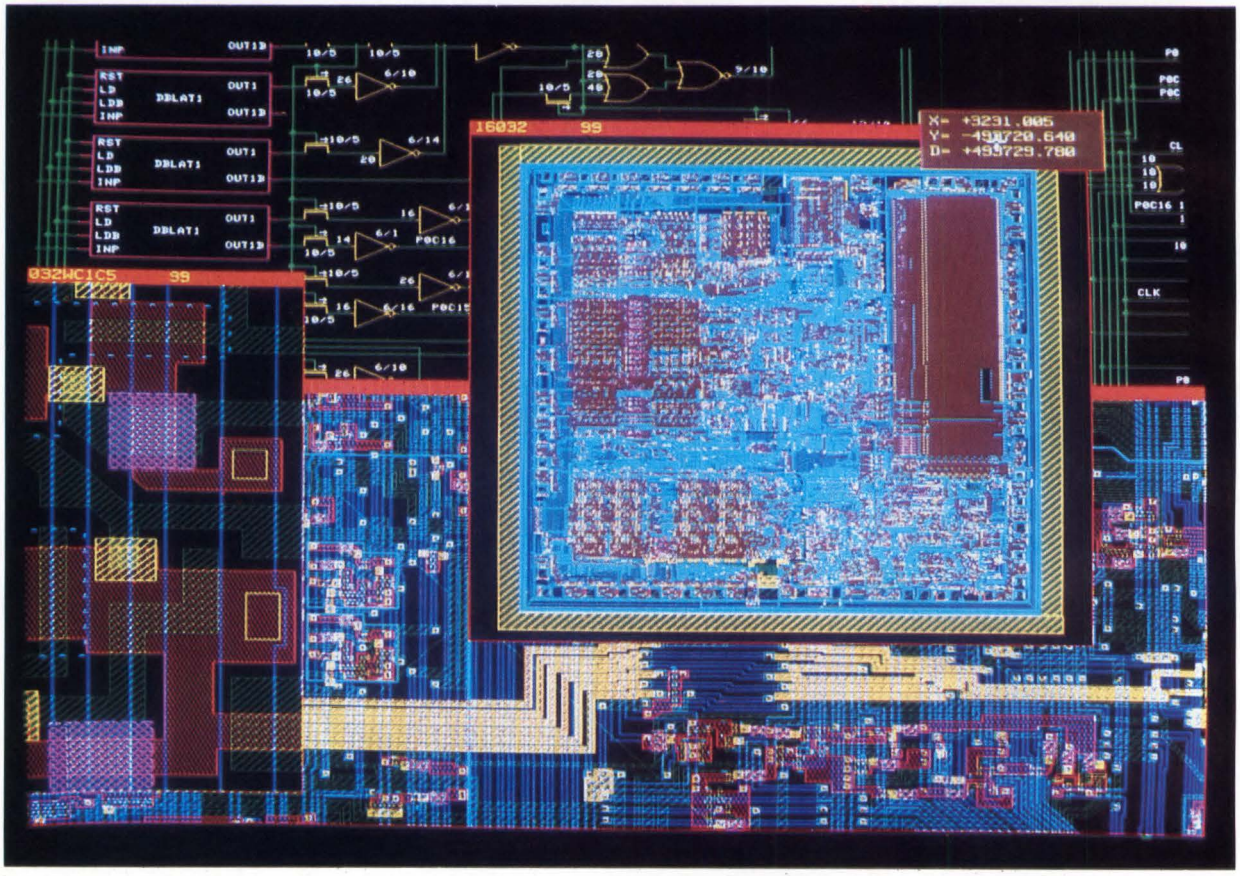
```
Netlist
Netlist
 (Contents
 (Instance Nand2 N1)
 (Instance Nand2 N2)
 (Joined N1:z N2:a)
 (Joined N2:z N1:b)
 )
```

(B)

nology Inc. (Santa Clara, Calif.) and Harris Corp. (Melbourne, Fla.). The latter calculates capacitance from layout geometry but uses the value only as lumped loading at each node.

For the currently employed 3- to 5-μm line widths, lumped capacitances have proven adequate, but below a micrometer, the rise and fall delays of the basic gates can change enough to necessitate simulating the real, distributed structure—no mean feat when tens of thousands of components are involved. The problem will become even more serious with silicon compilers, because no approximate geometry is known before the actual layout.

As compiled cells and even those that have their parameters defined by the user approach the complexity of custom cells, conventional layout software may have to be supplemented with custom layout techniques like compaction and ploughing. Compaction fits cells into a given space by compressing an originally loose layout to a desired aspect ratio. Ploughing makes space for, say, a via, by pushing aside existing lines under observation of the de-



3. Integrated workstations like Daisy's Logician can handle highly complex circuits from logic design to detailed layout. The ability to view several design steps in different windows helps the system engineer tackle the design of small circuit segments even at the mask stage.

sign rules (Fig. 5). This technique, like many other IC design advances, was developed at the University of California at Berkeley and gives routing algorithms some much needed freedom for standard and custom cells. Incremental design rule checking, essential to that technique, is accomplished by running the appropriate routine in the background during routing.

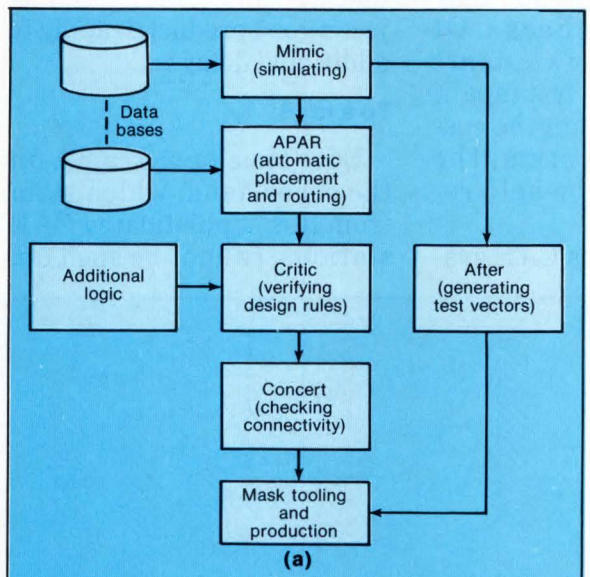
An experimental technique, stemming from AT&T Bell Laboratories (Murray Hill, N.J.), is known as virtual-grid symbolic layout. A program dubbed Mulga assembles cells that were defined in an intermediate language and laid out on a preliminary grid. The user describes a floorplan symbolically, and the program matches up adjacent cells by changing their preliminary (or virtual) grids.

Meet Freddy

From Europe comes another layout system that will shortly be distributed by Racal-Redac (Westford, Mass.). Running on a VAX-backed dedicated workstation, but scheduled for transfer to Apollo computers, the software was originally developed by Inmos Ltd. (Bristol, England) to design the transputer and has been nicknamed Fat Freddy. The user describes a circuit at a high level for two data bases, one graphical and the other functional. That duality flows throughout the hierarchical decomposition, down to the transistor level, where each physical component is checked against its functional definition and its simulated behavior. Because the system uses a transistor model with 25 second-order parameters, it can accurately reflect even such secondary characteristics as the drain pull effect.

Although meant for full-custom design, the software can certainly handle standard cells in an integrated environment. On the other hand, it comes so close to a silicon compiler that it will ease the transition for those wishing to switch from silicon compilation to custom design.

Assuming a chip design has passed all verification steps, an integrated CAE system should be able to produce a pattern-generation tape. This step, however, is sometimes performed by the foundry



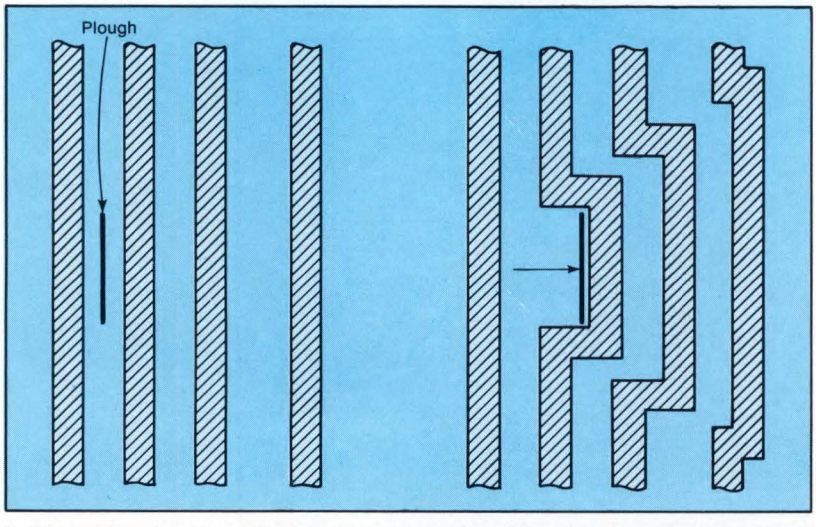
4. A foundry's CAE system for standard cells closely resembles those used on workstations, but the support of only one manufacturer's thoroughly tested cells simplifies matters (a). Cells are described here in the Mimic language, as demonstrated with a Johnson counter (b).

from net-list information, especially in the case of gate arrays. Often the deciding factor in establishing the designer-foundry interface rests not so much on technical consideration but on who will assume rsponsibility for the accuracy of the tests that determine whether a chip is labeled good or bad. Because production-quality automatic test equipment can cost over $1 million, the customer only performs spot checks. Of course, the foundry's tests are only as good as the test tape; if the tape comes from the customer's CAE system, the foundry cannot be held responsible.

Furthermore, as CAE systems proliferate, foundries cannot be expected to support all the different formats the workstations use, and at least one of them—Gould AMI Semiconductors—will only accept those from the major CAE suppliers. The company points out that only high-speed (10-MHz) test programs can find timing deficiencies. But they are hard to debug (eight weeks is not unusual) and, if faulty, can reject a good product, leading to additional delays.

To a fault

Low-speed programs, on the other hand, which stem from less sophisticated CAE stations, cannot be sped up:



5. Ploughing is a layout algorithm that simplifies local rerouting. Once a plough is inserted in, say, a set of interconnections, it can move them all while observing geometric design rules.

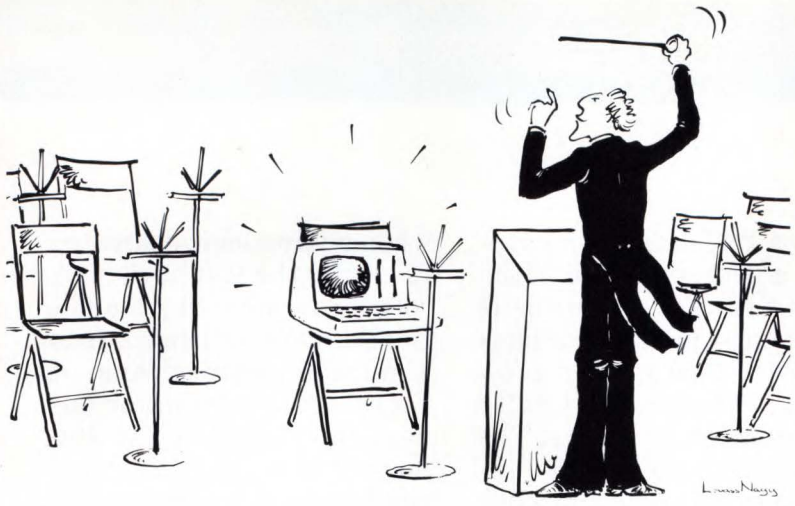
Test vectors that occur within the same cycle in a low-speed system may fall into different cycles in a faster system.

Truly integrated CAE software develops test vectors as a by-product of simulation and at least one—the Logician—actually integrates test generation with the circuit design and verification steps. Acting as a small expert system with knowledge about test procedures, the Daisy fault simulator program, DFS, warns the user early in the design cycle if the testability of his or her design might jeopardize future production. It not only tries out its test patterns by inserting faults in the design but also generates reports about the outcome of its scrutiny.

However, the currently used fault models—primarily stuck-at, bridge and open faults—are no longer adequate for VLSI chips, especially those implemented in CMOS. Stuck-at-open faults (where a gate output remains at logic 0 regardless of input) manifest themselves differently in CMOS from stuck-at-closed, so that the common but unspecified stuck-at mode becomes inadequate for gate-level circuit tests (see "Some Caveats in the Workstation Search," p. 128).

Risky assumption

Furthermore, most fault simulators assume that a single stuck-at check will catch multiple faults. That is not necessarily true when a single critical path is checked, because in complex chips it may be deeply buried in the



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Model 7128 Standard Programmer — Lower-cost version of 7228. Supports all PROM types except "A" versions of 2764 and 27128. Standard programming algorithm programs 2764 in 6.8 minutes.

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XASM04	*NEW*	6804	$ 250.00	$ 250.00
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XASM51		8051	200.00	250.00
XASM65		6502/65C02	200.00	250.00
XASM68		6800/01, 6301	200.00	250.00
XASM75		NEC 7500	500.00	500.00
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Model 7956 and 7956-SA Gang Programmers — Similar features to 7228, but program as many as 8 EPROMS at once. 7956-SA stand-alone version copies from a master EPROM. 7956 lab version has all features of stand-alone plus RS-232 interface.

EPROM: 2758, 2716, 2732, 2732A, 2764, 2764A, 27128, 27128A, 27256, 2508, 2516, 2532, 2564, 68764, 68766, 5133, 5143. **CMOS:** 27C16, 27C32, 27C64, MC6716. **EEPROM:** 5213, X2816A, 48016, I2816A, 5213H. **MPU (w/adaptor):** 8748, 8748H, 8749, 8749H, 8741, 8742, 8751, 8755.

7228	**Advanced Programmer**	**$ 549**
7128	**Standard Programmer**	**429**
7956	**Laboratory Gang Programmer**	**1099**
7956-SA	**Stand-Alone Gang Programmer**	**879**
GDX	**Driver Software**	**95**
481	**8748 Family Socket Adaptor**	**98**
511	**8751 Socket Adaptor**	**174**
755	**8755 Socket Adaptor**	**135**
CABLE	**RS-232 Cable (specify gender)**	**30**

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logic and thus hard to observe. For that reason, IC design techniques that simplify testing are gaining support.

A technique known as level-sensitive scan design partitions a chip and inserts register latches that capture the state of the signal path at the interface. Several IBM laboratories have cooperated in the development of a chip partitioning aid that formalizes the divide-and-conquer approach, but it is limited to logic systems that can be described as networks.

At AT&T Bell Laboratories, a system called Titus takes a similar approach. It inserts scan paths for designs of 2000 to 5000 gates in a few hours, then automatically generates test vectors. The lab reports a 10% to 15% increase in chip size and a 5% loss in speed. However, scan-designed chips elsewhere have been known to waste up to 40% of their area on test circuitry.

In practice, the logic designer still must rely on common sense and experience when adding logic dedicated to easing the test burden. A software system that simplifies the chore and amounts to a more grandiose form of Daisy's fault simulator has been developed at the Siemens Research and Technology Laboratories (Princeton, N.J.). Called Idas, it contains the Cadat logic and concurrent fault simulator; Hector, the actual testability analyzer; Pretest, which predicts testing costs; and Atwig, an automatic test pattern generator. All run on a Daisy workstation.

One more component, Edit, acts as the interface with the user, highlighting in different colors the observation and control paths. In addition, it automatically inserts flip-flops in areas where fault coverage is rather low, as determined by Hector's heuristic analysis.

Bottleneck in the making

Despite such efforts, the preparations for chip testing are rapidly turning into a bottleneck for application-specific ICs. When software tools make it possible to design VLSI chips in days, spending weeks if not months to test and debug that design is clearly not acceptable. The best bet to resolve the problem may well lie in fully integrated CAE systems that actually cover all the design functions—including full-speed test design and actual prototype testing—without costing a million.

One such system has recently been introduced by Mentor Graphics. It consists

Some caveats in the workstation search

Because a CAE system's fault simulation capability is both important and hard to observe, it typifies the difficulties in acquiring a CAE workstation. For each of the software components, the buyer must not only be ready to ask many questions but also be prepared to sample a range of circuits, designed to increasingly stress the system's abilities.

In addition to these major concerns, there are lesser ones that users of simulation packages must worry about. Some simulators, for instance, cannot handle system components running at different clock speeds. Others cannot manage variations in rise and fall time, and a few are even limited to one or two IC technologies.

Because each CAE system displays even the same simulator's output in a different way, it is essential to investigate the user interface. This is especially true because some displays have particular trouble with buses. Others cannot be caoxed into displaying functions that are not preprogrammed, even if the manufacturer is willing to part with the source code. In fact, even getting a gate-level net list can be excruciating or impossible. A good simulator should enable the user to view a circuit at different hierarchical levels and to make some changes—preferably without switching between editors that require different commands. Better still, if simulation runs as a background task when a circuit is being redesigned, the user can experiment more efficiently.

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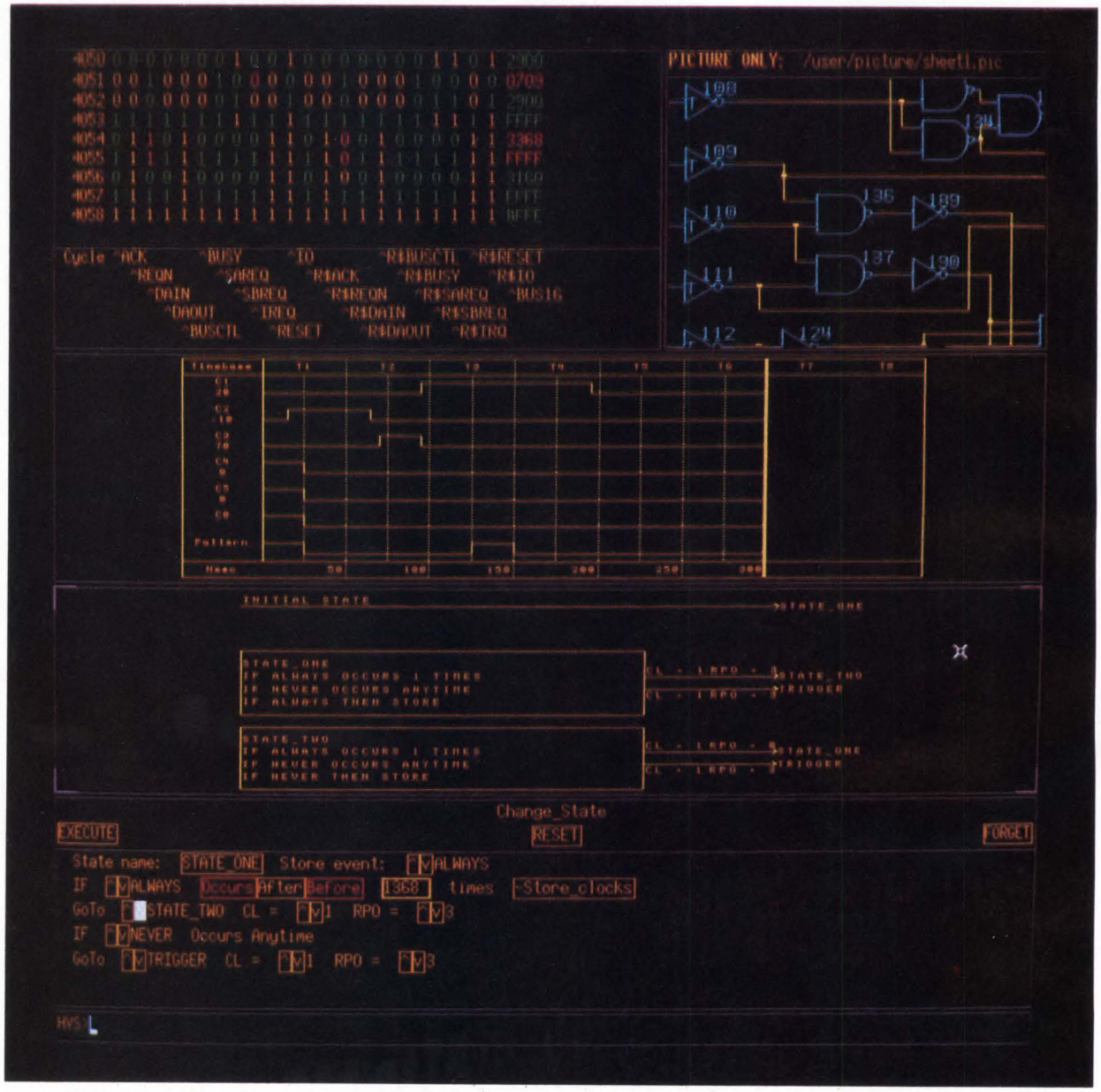
CIRCLE 61

of a software package, an Apollo node like the DN 300, and an extra chassis for the test hardware—a 160-channel pattern generator and logic state analyzer and 16 data acquisition channels). The hardware verification system not only permits the user to design testability into ICs and pc boards but actually to run developed test patterns at clock speeds up to 10 MHz (Fig. 6). Because the user is working with the same



6. Mentor's hardware verification system (HVS) serves either as a test pattern generator that highlights changes and problems (top left) or as a logic analyzer for a prototype (center). The user programs the pattern clocks according to current needs.

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graphics interface format and operating procedures as during earlier stages of the design, test generation and execution do not disrupt the continuity of the engineering cycle.

Better relations needed

While testability and testing are the most obvious shortcomings of present CAE systems, the most pernicious may well turn out to be the data-base organization. Completely hidden from the user, data-base management nevertheless determines the performance and the expandability of any data-intensive computer application.

Because hierarchical decomposition is widely accepted as the best approach to digital system design, most data bases in CAE systems are hierarchical, like Unix files. However, each component at most levels in the hierarchy has several aspects: A transistor, for example, has electrical attributes as well as geometric ones. One solution was mentioned in connection with the Inmos and RCA design systems—a dual data base with a 1:1 relationship among its components.

More often though, designers resort to a network schema, which can model interrelated hierarchical schemas. The price is a high processing overhead, because network nodes are interconnected via pointers that must be updated every time a relationship changes. On the other hand, homogeneous relational data bases are essentially flat, because each tuple—or record—contains a subsystem in each of the relation's attributes.

Texas Tech University (Lubbock) has worked out a schema that combines homogeneous and heterogeneous relations (where each item contains a subitem in only one of the attributes). While preserving relational algebra, this approach adds flexibility to the data base, since each item can be broken down either into subitems that must be ANDed (all must be present) or into others that can be ORed (only one need be present).

Because the data base is hard to change once a system has grown to substantial size, CAE system designers should start off with the most flexible concept they can find. Artificial intelligence has produced data model that fits the bill, because a class system—such as Smalltalk—accepts hierarchical object organization with inheritance rules while permitting the object to be seen with other views (also called attributes, flavors, or properties).

One reason for the absence of such data bases from CAE systems is their link with the Lisp language and its reputation for slow execution and large memory. However, alternative languages exist. Mainsail, for instance, has its origins in the Stanford artificial intelligence language (Sail) and Mainsail is extendable, portable, and permits dynamically binding. Intel uses it for its in-house CAE.

For these reasons, the CAE system under development at Cericor Inc. (Salt Lake City, Utah) is worth a closer look. It is called actor-based because each process requests actions from the data base that are specific to that task. The design guidance task, for example, which automatically checks loads, also displays errors culled from the data base while returning node-related results. As can be expected, Cericor's AI-inspired system pays a lot of attention to a consistent and cooperate user interface.

Dreaming of PC

The need for an extensive and extendable data base, as well as the need for high throughput, has so far eliminated personal computers from candidacy for integrated CAE systems. Simulation and fault generation in particular have proven prohibitive for 8088-based machines like the IBM PC—generally the preferred personal computer for engineering tasks—but the 80286-based IBM PC AT may change that. Daisy, whose Personal Logician has been capturing schematics for some time, has adapted the program to the PC AT and plans to extend it to simulation—an ambitious goal if the system is to digest more than a few dozen gates.

FutureNet Corp. (Canoga Park, Calif.) is taking a different—and perhaps more effective—approach. By adding a 16032-based coprocessor board that runs the Cadat simulator, the system packs the muscle of a full-fledged workstation where it counts the most.□

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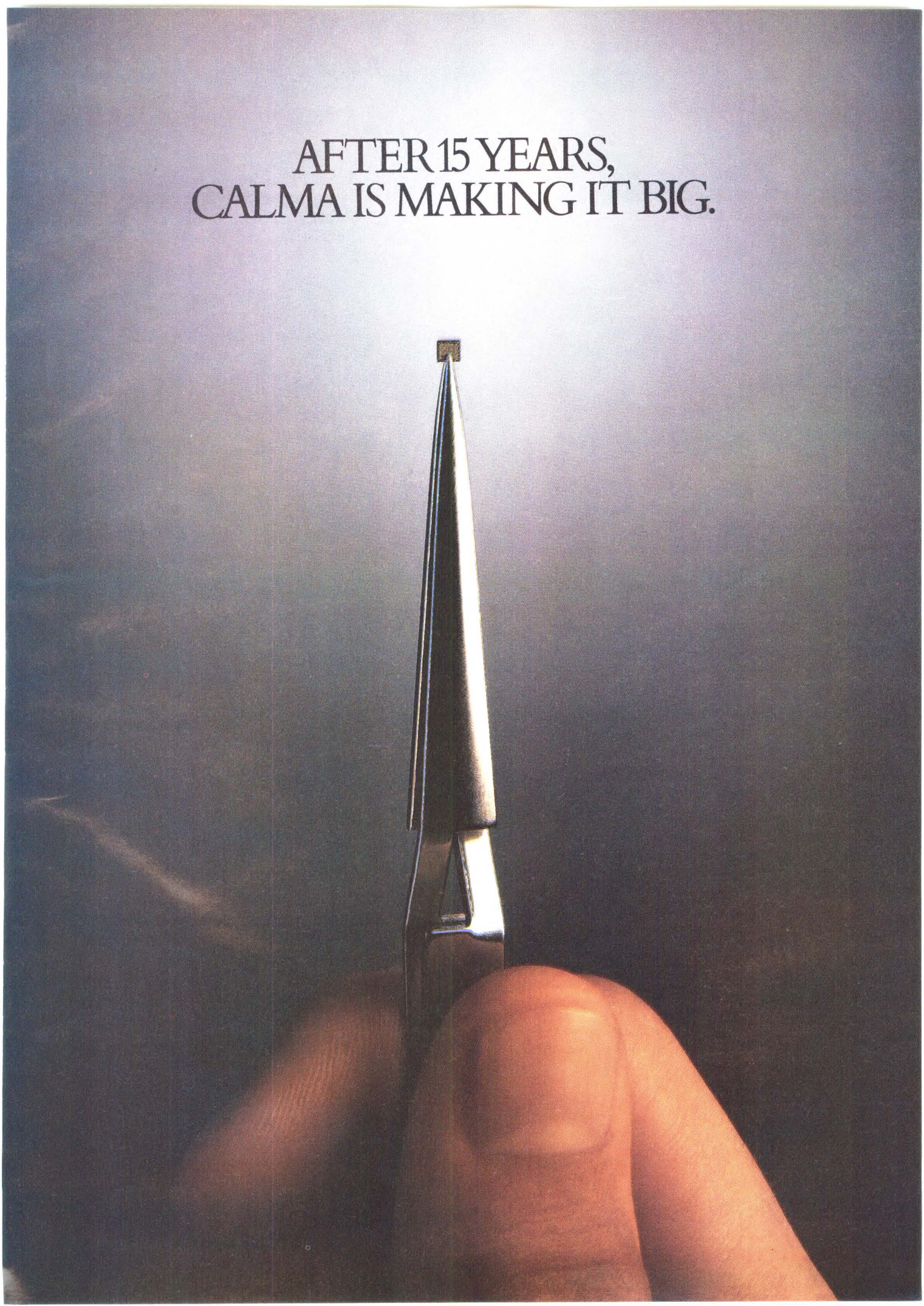

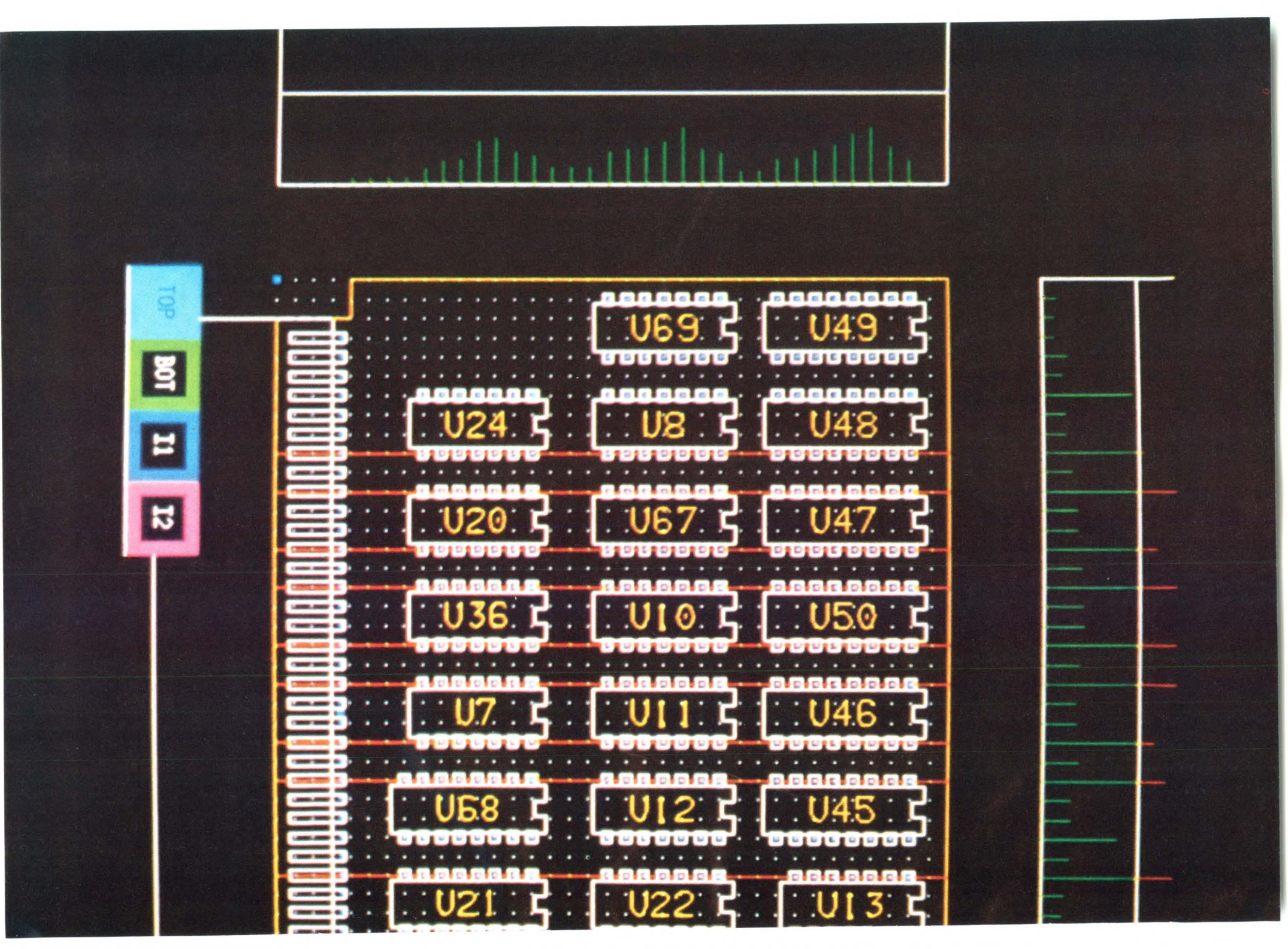
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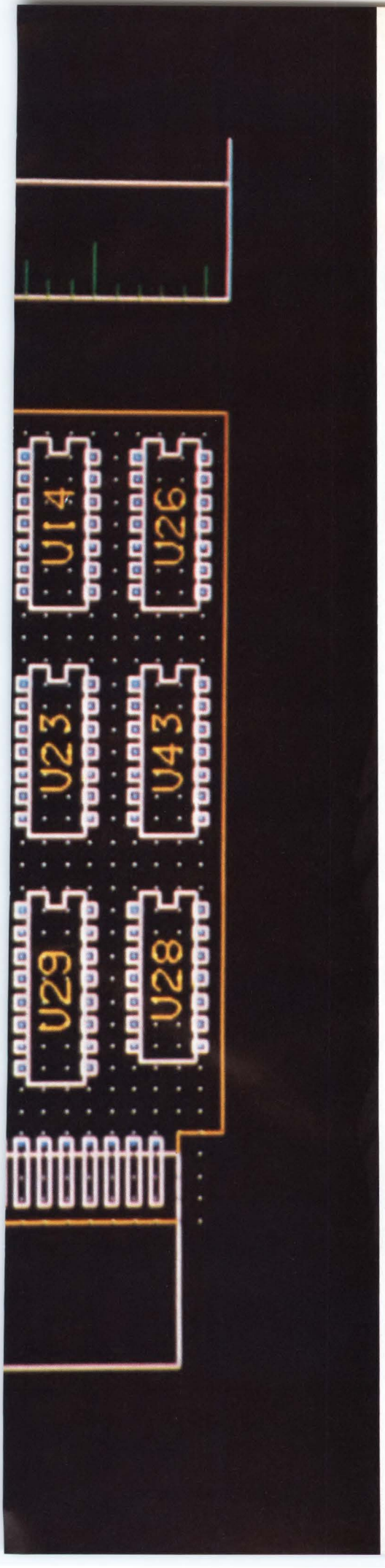

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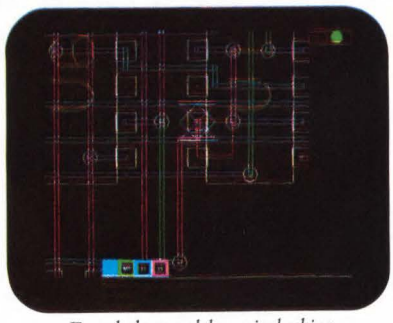
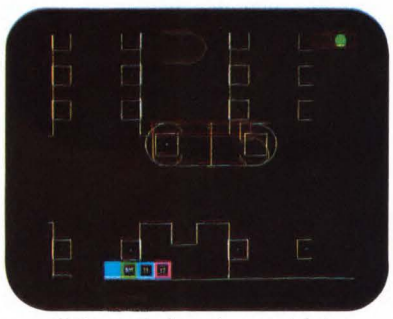


Error lockout and dynamic checking.



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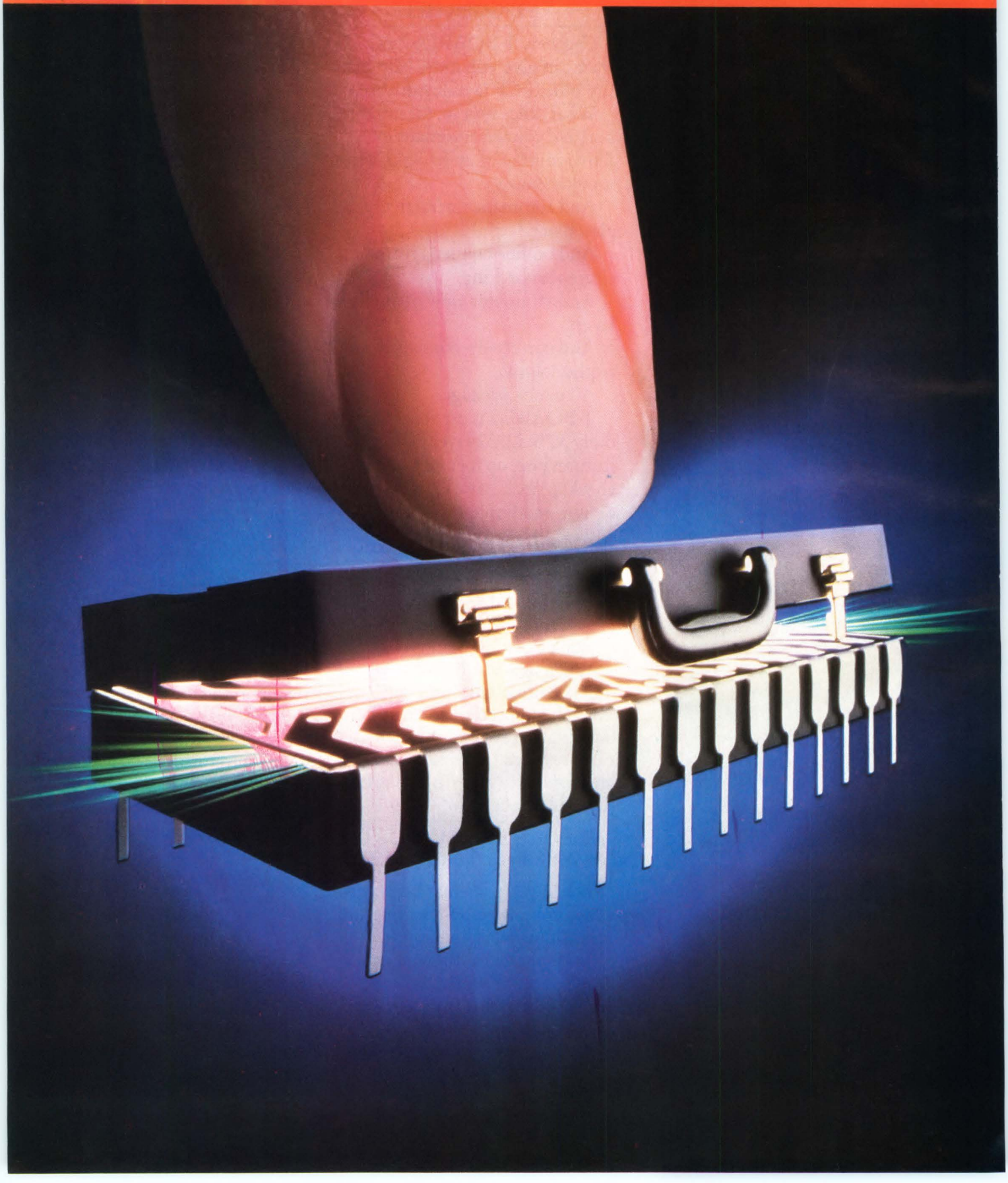

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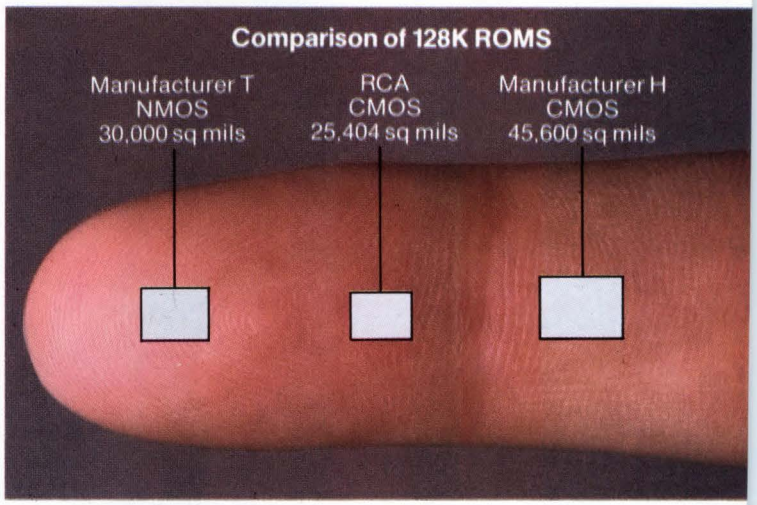

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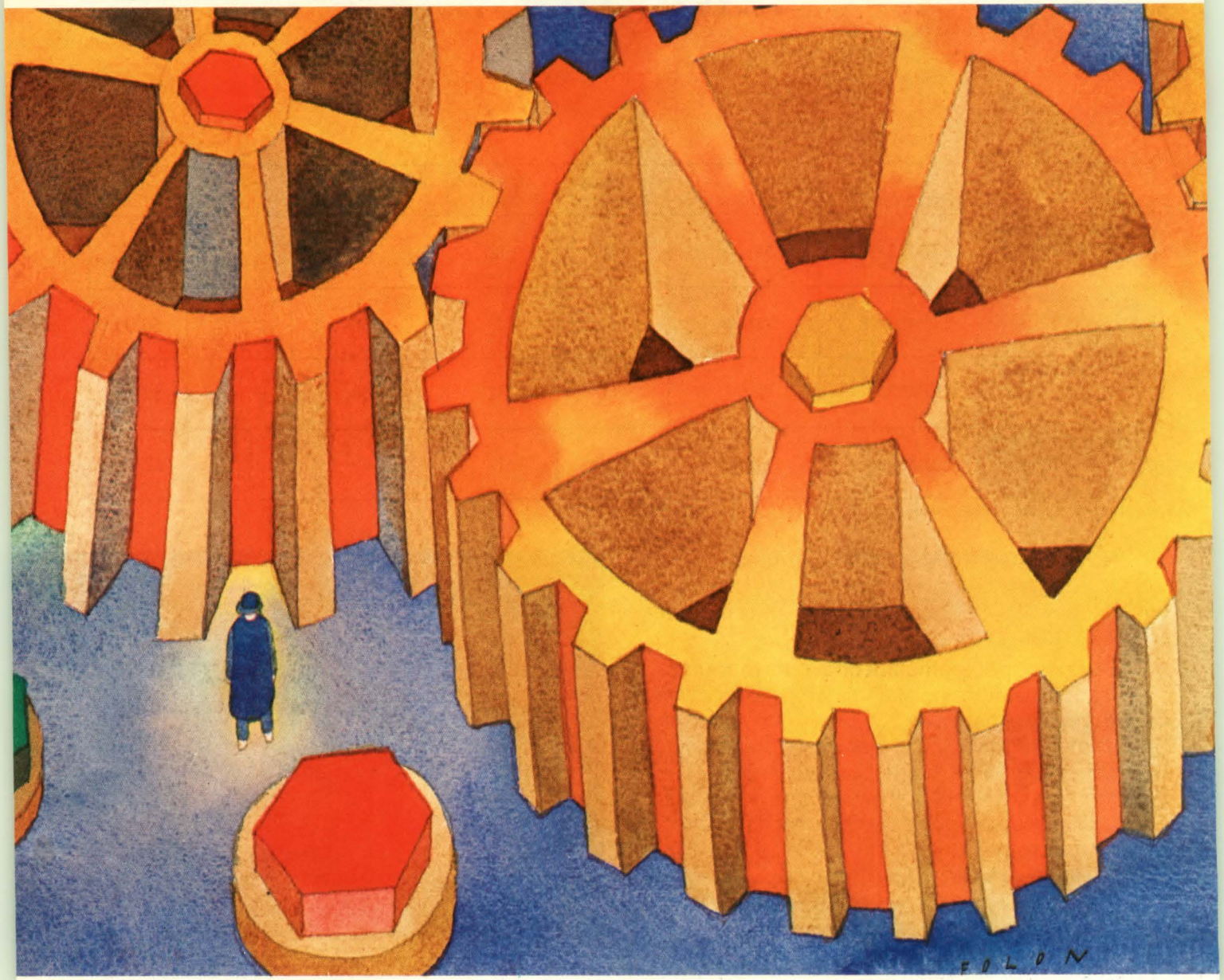
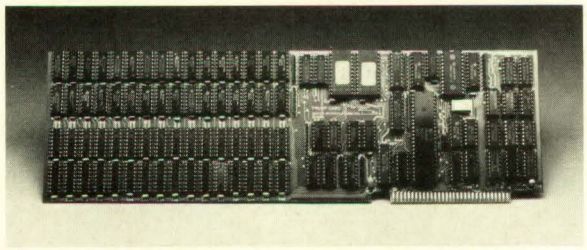


IBM® and other compatible PC computers are fast enough for general home and office use. But, for hardware and software development applications, the gears turn slowly.

What you need is a faster "gear" to co-process with the Intel 8088 inside IBM's PC. Like Zilog's Z8001® CPU. Now, there's a way to increase throughput for the IBM PC—as well as test the performance of the Z8001 CPU for your high-performance applications with a Z8001 CPU-based board called the "Trump Card" from Sweet Microsystems. And it proves dramatically how powerful Zilog's 16-bit CPU really is.

The new device is a peripheral board that plugs into any expansion slot on an IBM PC or compatible PC computer. Trump Card is addressed as an I/O device that communicates through the expansion bus. It is powered by Zilog's Z8001 CPU.

The Trump Card increases the computational power of the IBM PC, and provides maximum performance with a minimum of board space.



The Trump Card, shown from the front.The left side of the board contains 512 K-bytes of type-4164 dynamic RAM; the right side contains the Zilog Z8001 and an interface to the IBM PC I/O-expansion bus.

Z8001 COMPILER BASIC IS 80 TIMES FASTER THAN IBM INTERPRETIVE BASIC.

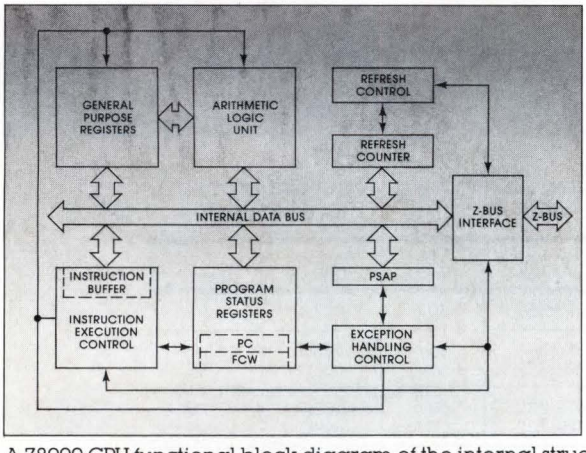
Essentially a monolithic minicomputer central processing unit, the Z8001 CPU is characterized by an instruction set more powerful than many minicomputers. As the programmer sees it, the Z8001 contains sixteen 16-bit general-purpose registers (for addresses or data) that may also be used in groups to form as many as eight 32-bit registers or four 64-bit registers. The low-order halves of the registers may be used for byte operations, thus the Z8001 CPU is able to manipulate data in 8-, 16-, 32-, and 64-bit pieces.

The Z8001 CPU, running at 10 MHz, can execute the same programs 4 to 10 times faster than the Intel 8088. What's more, the Z8001 CPU, with its large 8-megabyte memory range, makes the Trump Card's 512K bytes of memory easy to design with. (To use this memory in the card, you simply load a BASIC, CP/M-80, or C program from PC-DOS and type "RUN.")

Apple II	Apple III	TRS-80 Model II	IBM PC	IBM PC (with Trump Card)
224	222	189	190	2.4

A comparison of execution times (in seconds). Running on IBM's interpretive BASIC, a Sieve program takes 190 seconds to execute. Running the same program under TBASIC on the Trump Card Compiler takes only 2.4 seconds.

The eight addressing modes are register, indirect-register, direct-address, indexed, immediate, base-address, base-indexed, and relative-address. The instruction set utilizes data types ranging from single bits to a 32-bit long word. What's more, the processor executes 110 distinct instruction types that, when permuted by all the addressing modes and data types, create a set of more than 400 instructions.



A Z8000 CPU functional block diagram of the internal structure of the Zilog Z8000 family of high-performance microprocessors.

ALL THE PROPER SUPPORT FOR 512K BYTES OF MEMORY.

The wide range of software written for the Z8001 CPU is proven by all the programs you can run on the Trump Card. With the Z8001-based Trump Card, you can run the following software on your IBM or other compatible PC:

BASIC Compiler—TBASIC is PC BASICA-compatible. Most instructions are implemented without modification.

CP/M-80 Emulator—Allows you to run CP/M-80 Z80 assembly language programs directly. Just download your Z80 programs and run them.

C-Compiler—The industry standard version of C is available.

Debugger—Intended to aid in program development, you can examine and change memory and register contents and more.

Screen-editor—Has many word processing features, including ASCII text file development.

Multilevel Language Compiler—Allows Pascal-like control and data types, arithmetic expressions with automatic or specified allocations of registers, and more.

RAM Disk—Can allocate 128K to 387K bytes of on board memory to function as an intelligent RAM disk.

COPROCESSING IS JUST PART OF THE STORY.

The Z8001-based Trump Card is just one example of a successful application design for the Z8001 CPU. But there's far more to the Z8000 family than this.

Today, Z8000 CPU's are used in a wide range of applications, from industrial and medical products to computers and graphics imaging machines. And Zilog stands behind every application with service and software support that makes your Z8000-based products get to market on time.

Find out for yourself how much power Zilog packs into every Z8000 CPU by turning your IBM PC into a faster tool for modern times.

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For information about the Z8000 CPU, send for our complete overview or call our Literature Hot Line at 800-272-6560. For seminar dates and locations, or information on Zilog training, call 408-370-8091. Or write: Zilog, Inc., Technical Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008.

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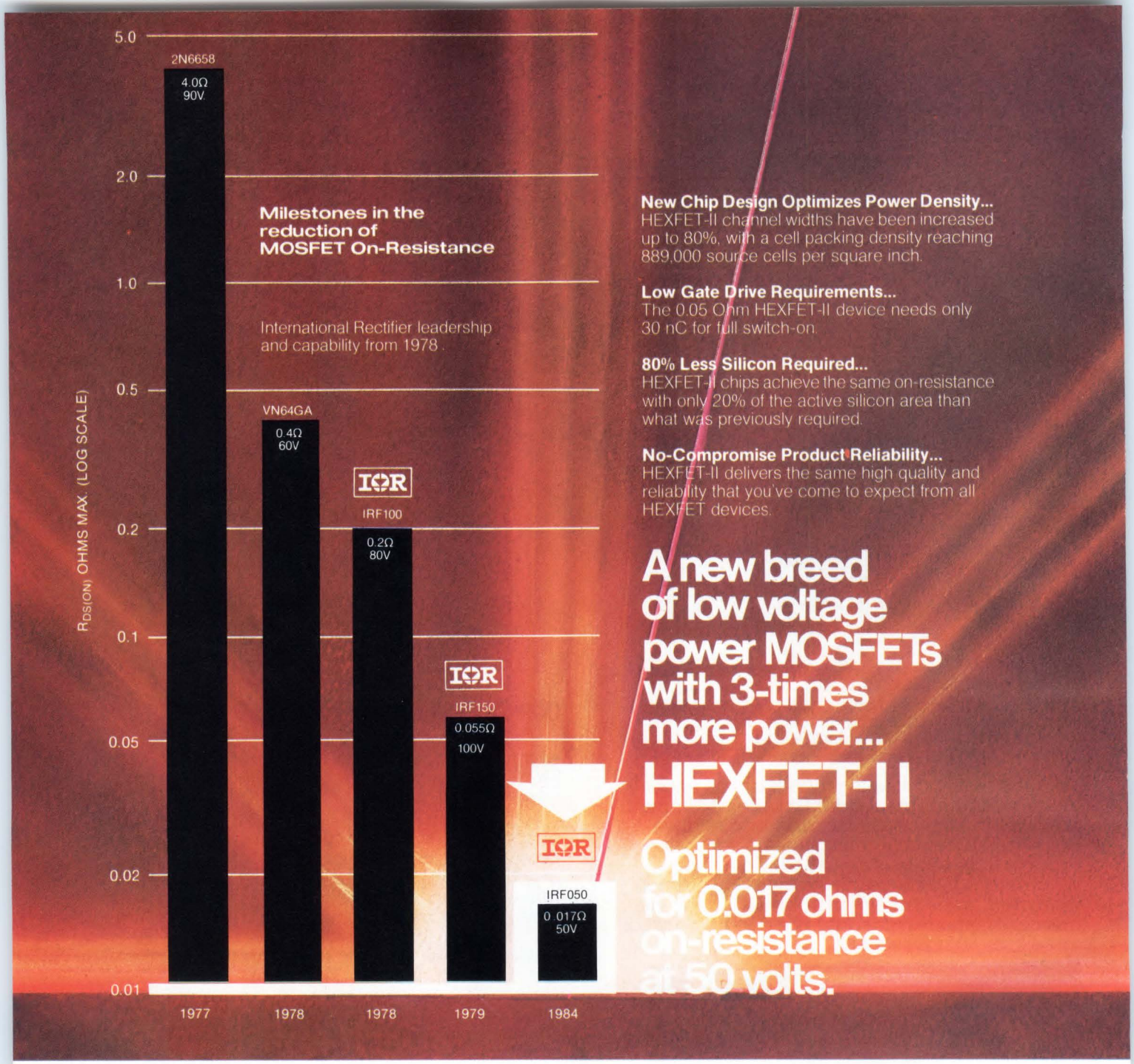

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CIRCLE 66

Monolithic controller builds PC network without toil or trouble

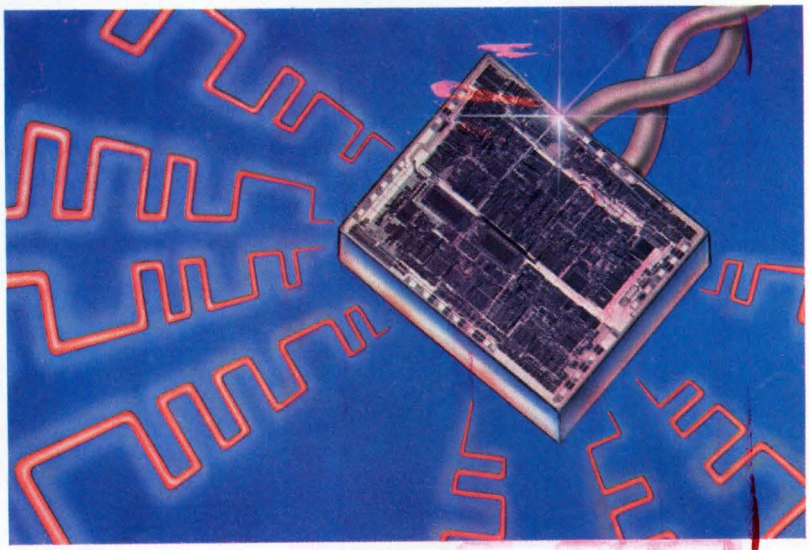
A controller chip puts CSMA/CD within the reach of personal computer networks, keeping a lid on parts count and simplifying software development.

Office automation promises to dramatically boost productivity. Personal computers are a step in that direction, and a giant one at that, forming a base of distributed intelligent machines. The next crucial advance is to link them in a network, so that each machine shares peripherals and information.

The 82588 is the first single-chip controller designed to join personal computers over a local network. Essentially a slave peripheral, the chip is fitted with a CSMA/CD controller, two logic-based collision detection mechanisms, and an encoder and decoder for both nonreturn-to-zero inverted (NRZI) and Manchester data encoding. Adding a simple transceiver line driver or an RF modem lets the controller implement all of the major hardware functions required by a local-area network.

Most of the chip's major duties, such as encoding and collision detection, can be programmed to meet the protocols of a particular network. And although its flexible system interface allows it to be employed with any popular microprocessor, the controller is optimized to work with the iAPX-186 and the iAPX-188 without TTL glue.

For the most part, local networks specifically designed for personal computers suffer from one of three major deficiencies. First, many are



Joseph Mazor and **Robert Galin,**
Intel Corp.

Joseph Mazor is a design manager for local-area network products at Intel's design center in Haifa, Israel. He is a participating member of the IEEE 802.3 working group for 1-Mbit/s star networks and holds a BSEE from Technion, The Israel Institute of Technology.

Since mid-1980 Robert Galin has been planning strategy for Intel's peripheral components operation in Santa Clara, Calif. He has a master's degree in engineering from the University of Michigan.

Cover: PC network controller

proprietary, forcing users to buy from one manufacturer. Second, with few exceptions, they lack collision detection, and therefore limit a network's efficiency for large offices (see "A LAN for All Reasons," below). Finally, industry-standard networks were originally designed for minicomputers. Thus, they are too expensive for personal machines. What is specifically lacking is an access scheme that is both efficient and cost-effective. In the past, carrier-sense multiple access with collision detection met the first requirement, but not the second. Conversely, approaches like collision avoidance meet the second specification but not the first.

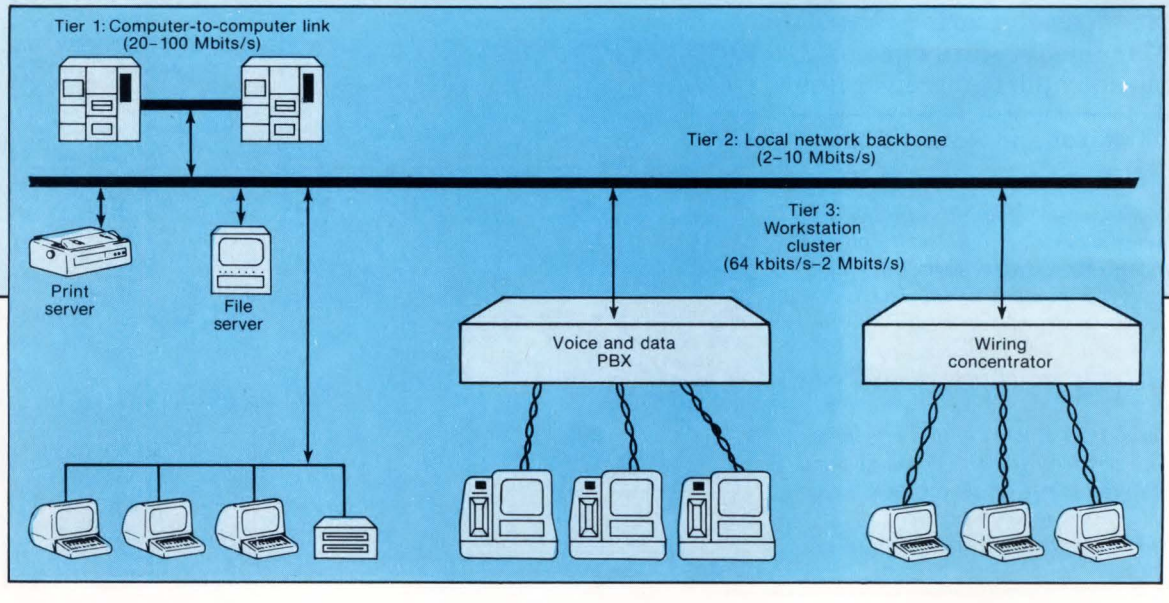
In contrast, the controller was designed with low-end systems in mind and makes possible inexpensive but efficient local networks in three ways. For the OEM, it reduces component count, board space, and development time. For the end user, its 1- or 2-Mbit/s data transfer rate (lower than that of networks based on minicomputers) allow the integration of controller, encoder-decoder, and collision detection functions, which lowers component cost. Also, lower bit rates imply cheaper, twisted-pair cabling that covers longer distances without expensive repeaters (Fig. 1).

The controller works with emerging stan-

A LAN for all reasons

The recent proliferation of personal computers in the workplace has led designers to realize that a single approach to local networks cannot answer all needs. A network for engineering workstations would be too expensive for personal computers. Instead, a network needs to be built as a hybrid, with portions within individual departments appropriate to the cost and performance needs of the applications they serve (see the figure).

To that end, there are four separate—though not competing—CSMA/CD network specifications in various stages of development. The first is Ethernet, which with its 10 Mbits/s data rate is best suited to local networks built around minicomputers or as a backbone connecting smaller clusters of networked personal computers. Another approach, dubbed Cheapernet, is a reduced-cost implementation of Ethernet that works well with personal computers in research and engineering settings where 10 Mbits/s performance is necessary. A third approach, IBM's recently announced PC network will connect personal computers that are located up to 5 Km apart. Being a broadband network, it has the advantage that it can carry several services (video and data) over a single coaxial cable. Finally, Starlan is a proposed IEEE 802.3 standard that is a 1-Mbit/s baseband system. It inexpensively links devices, such as personal computers, through already installed twisted pair wires used for telephones. Its major use is for the office environment where low cost and ease of wiring is extremely important.



dards for personal computer networks like American Telephone and Telegraph's Starlan (1-Mbit/s baseband) and the IBM PC network (2-Mbit/s broadband). The controller also can be coupled with an off-chip data encoder-decoder to handle up to 5 Mbits/s when higher throughput is needed.

At your command

The IC communicates with a host using a set of 16 high-level commands (Fig. 2). The Transmit, Retransmit, Configure, and Diagnose commands free the CPU from overseeing every step of each task that the controller undertakes. Instead, after the processor invokes a command, it is free to take on other jobs. The high-level commands simplify writing and debugging software for the controller and the network.

Another of the controller's important features is its efficient memory structure for receiving frames. A network carries a large number of relatively short control messages, like Open, Close, and Acknowledge, that direct its operation. In fact, typically 75% of all network messages may be less than 100 bytes long. As a result, a storage system that breaks memory down into large, equal-sized blocks would be vastly inefficient. Each block would be able to accommodate the largest possible frame but would be only partially filled most of the time. The controller avoids this problem by using a sophisticated approach that allocates multiple buffers to a frame.

Rather than retain a frame in a single, sequential block, the chip stores it in a number of smaller buffers. A 100-byte buffer, say, could hold a short frame, and multiple 100-byte buffers could store longer ones. To link individual buffers, the host processor creates a chained list of pointers that indicate where in memory the data is held. This multiple-buffer approach keeps the amount of memory needed to store received frames to a minimum, an extremely important consideration in personal computers, where RAM is at a premium.

Aboard the chip

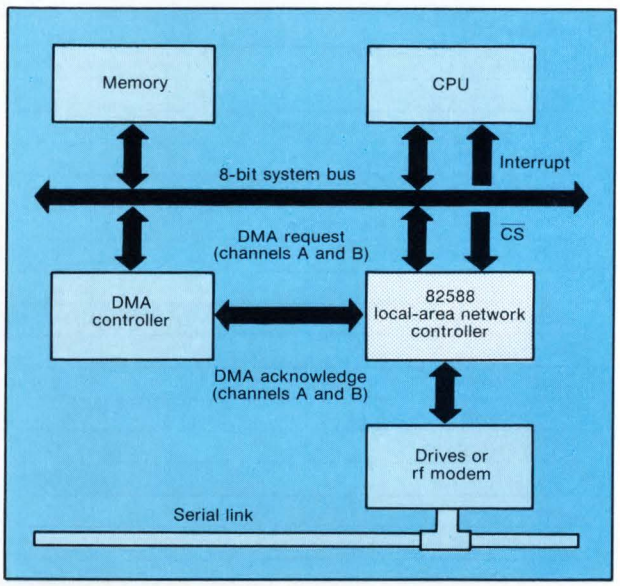
The controller itself consists of two main sections: a parallel system interface with the host and a serial interface to the network. Two built-in 16-byte FIFOs, one for transmitting and one for receiving, link the two (Fig. 3).

The first block consists of a bus interface unit and a group of registers. The bus interface contains an 8-bit data bus. It is responsible for all communications with the system CPU. In conjunction with an external DMA controller, the new chip takes care of all reading and writing to memory—at up to 4 Mbytes/s—as well as all CPU interrupts. Two DMA channels are recommended, one for transmitting and the other for receiving.

The parallel section also comprises three sets of registers: one for storing configuration information, one for writing commands to, and one for reporting the chip's status. To make rapid changes in the controller's operating parameters, the processor enters a block of data into RAM, and that data is loaded by DMA into the registers (Fig. 4).

Serial side

The chip's serial interface contains the CSMA/CD controller and converts parallel data into serial form, and vice versa. It also assembles each frame as specified by the configuration registers, computes the cyclic redundancy code (CRC) for each transmission, and



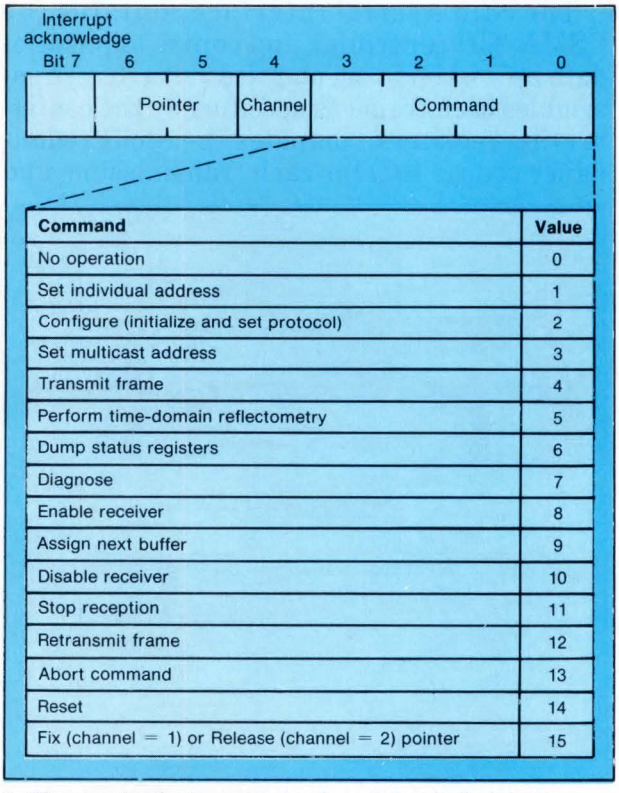
1. The 82588 local-area network controller connects directly to a network (through a driver or modem) without the need for an expensive transceiver tap. Intended for relatively low data rates of 1 to 2 Mbits/s, the chip allows networks to be built with twisted-pair wires instead of coaxial cables.

backs off and reattempts transmissions in case of a collision.

Since most of its major features are completely under user control, the IC's data-link controller subsection gives an enormous degree of freedom to the system developer. And the chip is right at home in a wide variety of networks. For baseband transmission, it handles end of carrier (IEEE 802.3) framing; for the IBM PC network it accommodates high-level data link control (HDLC) framing. Both techniques include a 32-bit CRC for error detection. The data controller also can be programmed with the length of the address field, station priority, framing, minimum frame length, spacing between frames, and slot time.

The two collision detection methods increase the controller's range of possible applications as well (see "Collision Insurance," p. 148). The code-violation detection mechanism is most useful in short-topology networks, such as a serial backplane. The bit-comparison technique is employed in systems with separate channels for transmission and reception, like a broadband network. Both can be used simultaneously to ensure reliable operation.

The chip presents a rich assortment of diagnostic and management functions: internal and external signal loopback paths, channel activity indicators, optional capture of all frames (regardless of destination address), and time-domain reflectometry for locating faults in the network cable. Moreover, the controller's Dump command gives the designer access to the contents of all of the chip's registers, which helps debug system software.



Command	Value
No operation	0
Set individual address	1
Configure (initialize and set protocol)	2
Set multicast address	3
Transmit frame	4
Perform time-domain reflectometry	5
Dump status registers	6
Diagnose	7
Enable receiver	8
Assign next buffer	9
Disable receiver	10
Stop reception	11
Retransmit frame	12
Abort command	13
Reset	14
Fix (channel = 1) or Release (channel = 2) pointer	15

2. The controller's command register is fed commands from the host CPU, which the chip executes for one of its two channels. The pointer field within the register identifies which status register is to be read, and the interrupt acknowledge field resets the controller's interrupt line to the CPU.

The time is right

A clock timing generator on the chip's serial side determines the data rate. It will accept up to a 16-MHz crystal for data transfers to 2 Mbits/s. (The parallel side has its timing set by the system's master clock.) The data encoder and decoder, also on the serial side, can transmit and receive information in any one of three formats: Manchester, differential Manchester, and NRZI. Manchester is used in Starlan. NRZI encoding is for broadband systems.

The transmit and receive FIFOs enable the parallel and serial sections of the controller to exchange data. These registers, each 16-bytes deep, improve data throughput between the controller and the host CPU. The controller's programmable FIFO threshold can be fine-tuned to a particular system's bus latencies.

The controller and the CPU talk to each other through main memory and the controller's on-chip registers. The processor uses the Chip Select (CS) line—along with the Write or Read signal—to gain the controller's attention. The controller communicates with the CPU over the Interrupt (INT) line. In addition, the two share an 8-bit data bus.

Two transfer types

Two types of transfers can take place via the bus. The first is a command and status transfer; the second, a data transfer. The former is always performed by the CPU. To initiate a Transmit or Configure command, for example, the processor issues the command to the con-

troller.At the completion of the command the controller issues an interrupt and the CPU reads the chip's status.

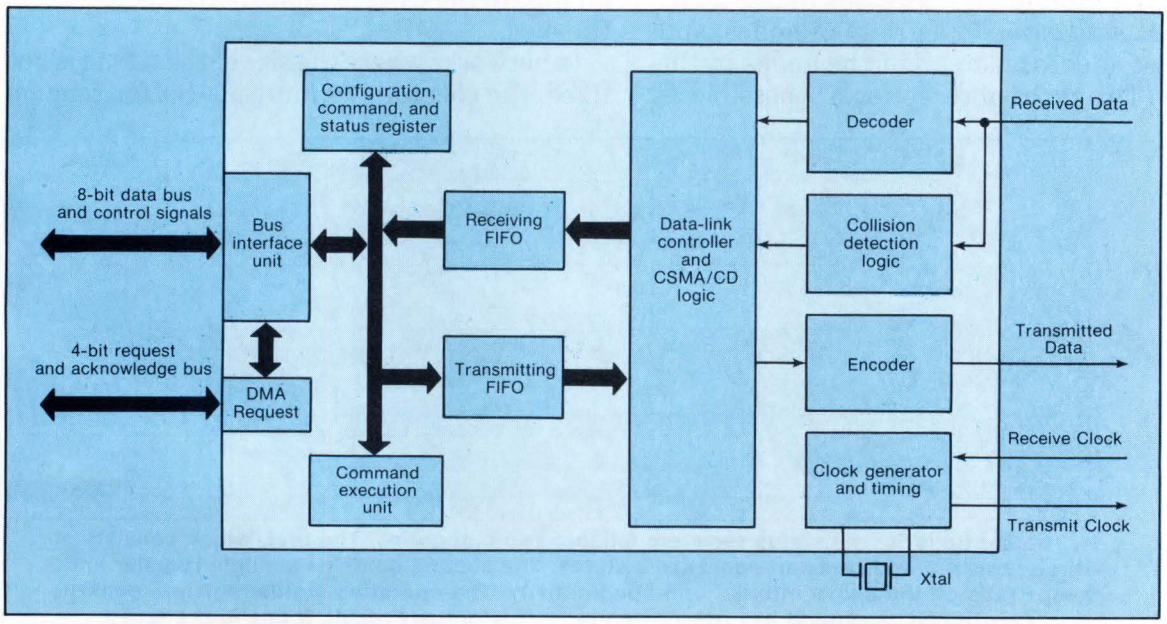
The host reads each of the four status registers, from the same port, in round-robin fashion. Any parameters or data associated with a command are transferred between the main memory and the controller using DMA. Data transfers, unlike command and status transfers, are requested by the controller and are most often carried out by an external DMA controller.

Dual DMA

The controller is fitted out with a pair of DMA channels, each with a Request and Acknowledge line. Typically, one channel receives data and the other transmits information and carries the chip's initialization and maintenance routines. The channels are identical, though, and can be used interchangeably. When the controller needs to transfer data to or from memory, it activates the DMA request lines and the DMA controller. When it is finished, it interrupts the CPU, which then reads the status of the controller to confirm the operation.

In order to transmit a frame, the CPU first prepares a data block in memory, which contains the network address to which the frame is to be sent and the information to be transmitted. The CPU programs the DMA controller with the address of the block, along with other control information. It then issues a Transmit command to the controller's command register.

At this point, the controller monitors the network link to determine whether the line is free. If it is, the IC starts transmitting the frame by inserting the preamble, beginning-of-frame flag, and the source address and fetching bytes from memory, loading them into the FIFO, and



3. The controller's two main blocks are linked by two 16-byte FIFO registers. The parallel section comprises a bus interface unit that connects the controller to the host and a register subsection that accepts commands and delivers information on the controller's status. The serial section contains a data-link controller subsection, decoder and encoder circuits, collision detection logic, and a serial-timing generator.

sending them out over the network. While the controller is sending the frame, it calculates a CRC, which it appends to the end of the data field. If a collision is detected during transmission, the controller sends out a jamming pattern and interrupts the CPU. The processor can then issue a Retransmit command, which works in the same way as the Transmit command, except that the chip keeps a record of the number of collisions that are detected. At the end of a transmission, the controller updates all of the status registers and sends an interrupt to the CPU, indicating that the transmission is complete.

When it is not transmitting a frame or doing housekeeping, the controller continually checks the network for any messages addressed to it.

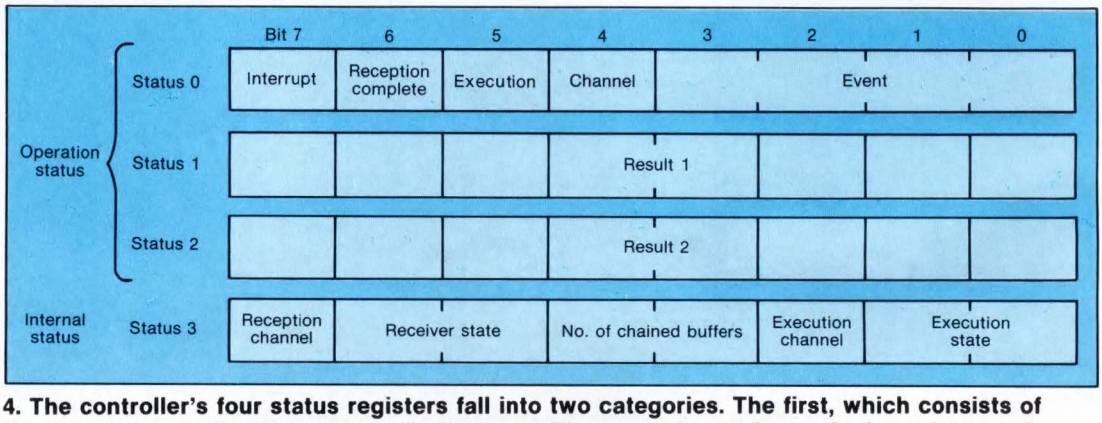
Calling all nodes

The controller can be addressed in one of three ways: individual addresses to one node, multicast addresses to a group of nodes, and broadcast addresses to all of the nodes in the network. Two types of reception are possible as well. In the "promiscuous" mode, the controller accepts any frame that is transmitted on the network regardless of its address. In the other, the device accepts only multicast and individual addresses that correspond to its own. The latter typifies normal operations.

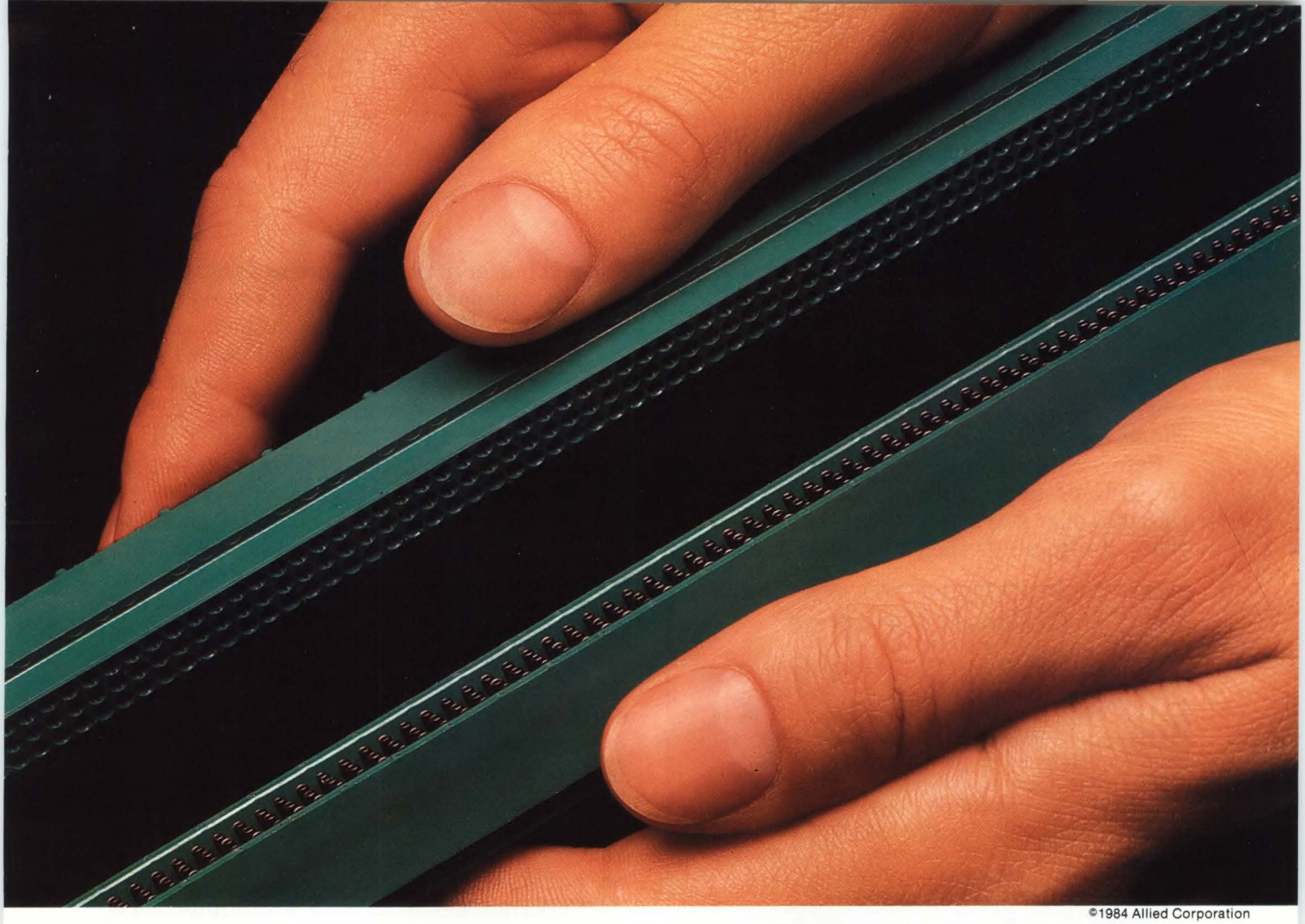
Before enabling the receiver, the CPU makes a memory buffer available and programs the DMA controller with the buffer's starting address. The received frame is then transferred to memory. This is known as single buffer reception, since the entire frame is sent to a continuous buffer.

When a frame is received, the network controller records the number of bytes that were written into the memory buffer in a status register. Also, the controller records the status of the reception—whether it was successful or not—and affixes that information to the received frame. Then the controller issues an interrupt to the CPU to indicate that reception is finished.

In networks where the size of the frame is not fixed, the controller's multiple-buffer scheme



4. The controller's four status registers fall into two categories. The first, which consists of three registers, indicates an operation's status. The second contains a single register and keeps tabs on the chip's internal operating activity. The operation status registers confirm that a particular command has been executed and store any result, if one is produced.



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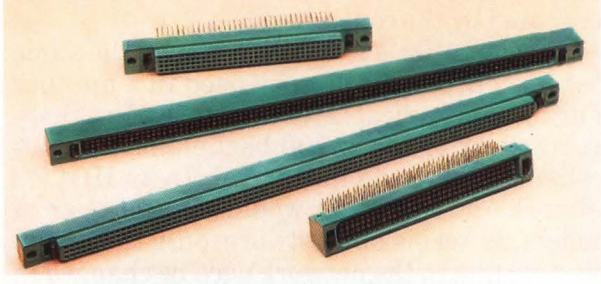

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CIRCLE 67

makes effective use of the memory. In multiple buffering, the controller alternately receives the contents of a given frame from one of the two DMA channels. This dynamic allocation of memory buffers makes particularly efficient use of available storage when frames are of widely differing sizes.

Before multiple-buffered reception begins, the CPU allots one buffer to the controller. As the controller starts receiving the buffer's contents, it interrupts the CPU and requests that the next buffer in the sequence be assigned. The processor responds by loading the second DMA channel with the information in the next buffer. In this way, the controller can immediately switch over to the second channel as soon as the first buffer is full. When channels are switched, the controller again interrupts the CPU to request another buffer, and information on that buffer is loaded into the unused channel.

The process of alternating between channels continues until the entire frame has been loaded. By the time that is accomplished, the received frame has been spread over a number of buffers, and the CPU has created a description of the buffer-chain in memory.

Connecting the controller to any of the industry's leading microprocessors is a straightforward task because the chip's system interface adapts easily to any processor that works with standard data bus and control signals. The chip works with no wait states on an 8-MHz system bus. Further, a system based on the chip and one of the 80188 and 80186 family of microprocessors exacts a minimum component count (Fig. 5).

Easy interface

In a system centered on the 8-bit 80188, for instance, the controller connects directly to the microprocessor's 8-MHz clock and data bus and to its Read, Write and Chip Select control signals. Although the controller needs two DMA channels to operate, these, too, are supplied directly by the processor. And the CPU's interrupt controller can service the interrupts generated by the controller.

The controller's flexibility allows the same system configuration to be used in a number of different physical layer interfaces. In a Starlan network or in a serial backplane, the controller would feed a line driver. In an IBM PC network, the controller would connect to an rf modem. In terms of hardware, only the actual physical link to the network need be changed in order to switch between these applications. All other necessary variants are easily implemented by commands that can be built into the system's firmware.

For baseband systems running at 1 Mbit/s and using unshielded twisted-pair or coaxial cable, the only external components needed are

Collision insurance

The efficiency of CSMA/CD was demonstrated in a 1979 study of Ethernet that linked about 120 host computers and network servers. The investigation showed that a network using some form of collision detection had a throughput of 98%, compared with 37% in systems that deferred while there was traffic on the channel, and 18% in those with no collision-regulating provision at all. Until recently, though, the relative sophistication of such collision detection schemes as CSMA/CD precluded them from low-ends networks.

The 82588 can be programmed in two ways to implement CSMA/CD collision detection. Both are logic-based. In code-violation detection, the controller looks to see if incoming bits violate Manchester or NRZI enoding standards. If that is the case, they are assumed to have been damaged by a collision. The second method, bit comparison, is useful in networks with separate transmission and reception channels such as Starlan or the IBM PC network. In this scheme, the device compares its transmitted CRC signature with that of the received signal while a transmission is taking place. Monitoring the network in this manner allows the chip to immediately backoff and try again when a collision is detected, without having to wait for an acknowledgement from the received mode. Hence, total data throughput is significantly increased.

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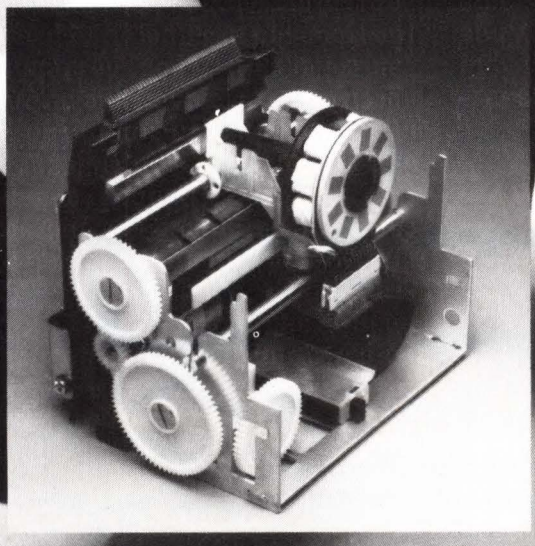

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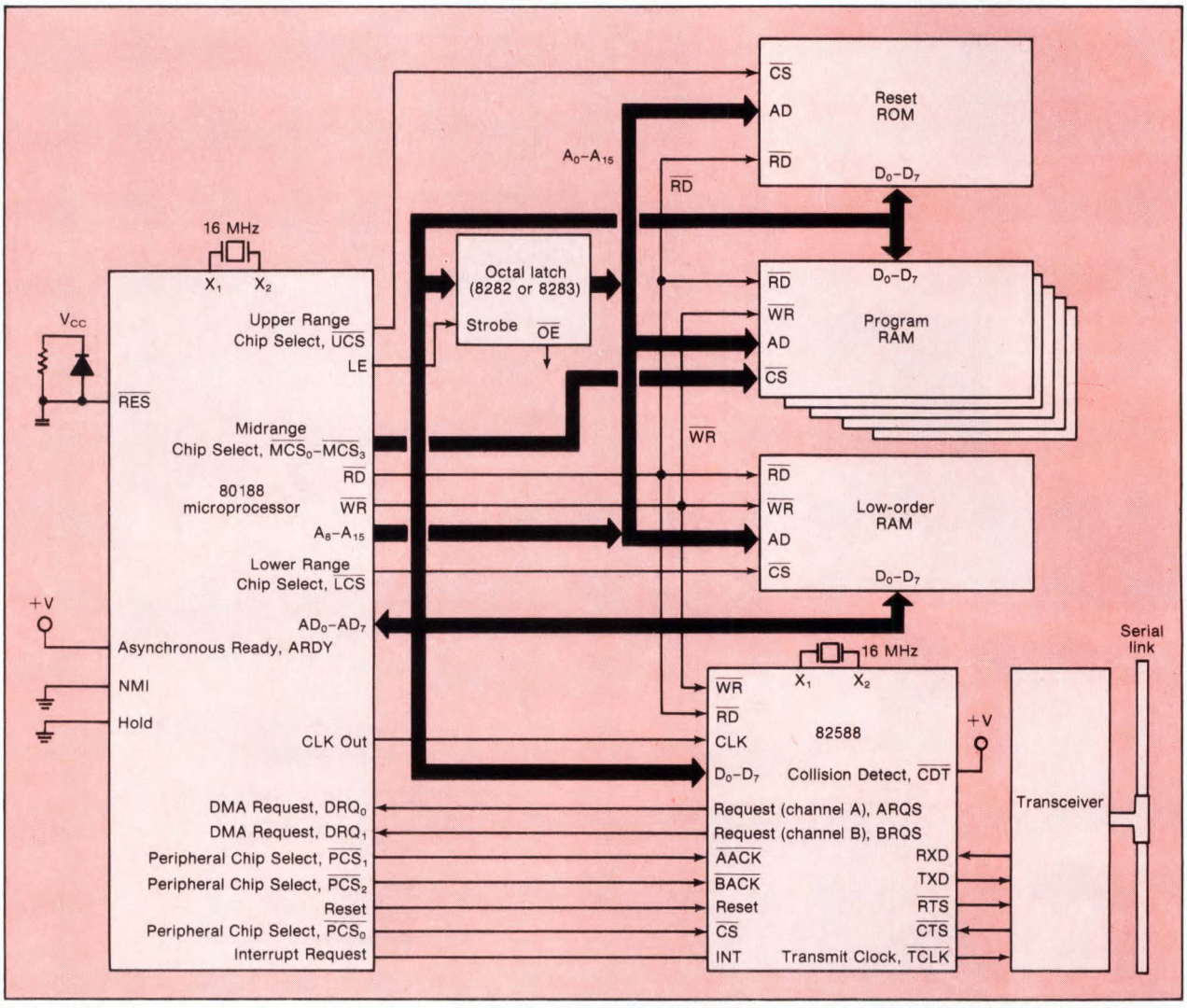
CIRCLE 68

Cover: PC network controller

an RS-422 driver and receiver and, possibly, one or two pulse transformers. The last supplies dc isolation. Together, these few components can fit onto an area that is 6 cm on a side. In contrast, traditional data-link controllers and their associated TTL glue and other logic demand an area that is at least 15 cm on a side.

In a Starlan configuration, the controller links to the network through low-cost RS-422 transmitter-receivers, one connected to Transmit Data, TXD, pin and the other to the Receive Data, RXD, pin. Each transmitter-receiver is joined to a separate pulse transformer and then to corresponding transmit and receive twisted-pair. Each station is connected to a hub over the two twisted pair drop cables,up to 800 ft. in length. Within the hub is a corresponding pair of transformers and RS-422 receiver-transmitters for each station. Transmitted signals from a number of nodes are ANDed on a short (less than 1m) bus and returned back to the controller through the receiver pair. The trans-



5. A minimum number of components marks the interface between the controller chip and an 80188 microprocessor. The controller IC links directly to the processor's 8-MHz clock, and Read, Write, and Chip Select control lines. Even the two DMA channels and the interrupt functions are handled by direct connections between the microprocessor and the LAN controller chip.

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mitting controller performs collision detection on the received data.

For broadband systems, such as the IBM PC network, NRZI-encoded data passes through an rf modulator and demodulator. In this case, the RTS and Clear to Send (CTS) signals from the controller are modem handshake signals. Here, the transmit and receive signals are modulated at different frequencies, or channels. A frequency translator on the network receives the signals from all the nodes and retransmits them at the system's receiving frequency. The receive and transmit channels of the IBM network each fits into the bandwidth of a 6-MHz TV channel.

Software for the controller is much simpler and easier to implement than for traditional data-communication chips. One reason is the controller's high-level commands, which speed software development, as well as offload the CPU. Another reason is the controller's ability to handle complete frames without the processor's assistance.

In a PL/M-86-language procedure for transmitting a frame, the CPU prepares a block in memory by loading the DMA controller with the starting address of the block and its byte count (Program 1). The central processor also enters the DMA parameters into temporary storage so that they can be reused in case a collision occurs. After loading the DMA controller, the processor issues the Transmit command to the controller. If the channel is clear, the frame is sent. Otherwise, the chip automatically defers to any activity on the data link and then transmits its signal. Ultimately, the controller interrupts the CPU, which determines from the status register whether or not the transmission was successful.

If a collision occurs, the CPU invokes the Retransmit procedure (Program 2). In this procedure, the DMA controller is reloaded with the parameters (taken from temporary storage) and the Retransmit command is issued. On receiving it, the controller again attempts to transmit the frame, but only after a back-off time (which begins counting on the last collision) has run out.

Finally, to receive a frame, the CPU prepares a buffer in memory, loads the DMA controller, and enables the receiver (Program 3). When a frame arrives, it is deposited into the memory using a DMA operation. Then the CPU is interrupted, letting it know that it can now determine the length and status of the received frame.□

Program 1. Sending the message

```
TRANSMIT: PROCEDURE (CHANNEL,BUFFER_LEN,BUFFER_
          POINTER):

   DECLARE CHANNEL BYTE;
   DECLARE BUFFER_LEN WORD;
   DECLARE BUFFER_POINTER POINTER;

   TX_BUFFER_588(00) = BUFFER_LEN MOD 256;
   TX_BUFFER_588(01) = BUFFER_LEN / 256;

   TX_BUFF_PTR =,
     BUFFER_POINTER;          /* TEMPORARYSTORAGE */
   TX_CHANNEL = CHANNEL;
   TX_BUFFER_LEN = 2048;      /* MAX. FRAME SIZE */

   CALL DMA_LOAD (TX_CHANNEL,1,TX_BUFFER_LEN,
     TX_BUFF_PTR);
   OUTPUT (CS_588) = 4 OR SHL (TX_CHANNEL,4);
                              /* TRANSMIT */
   RETURN:

END TRANSMIT;
```

Program 2. Try, try again

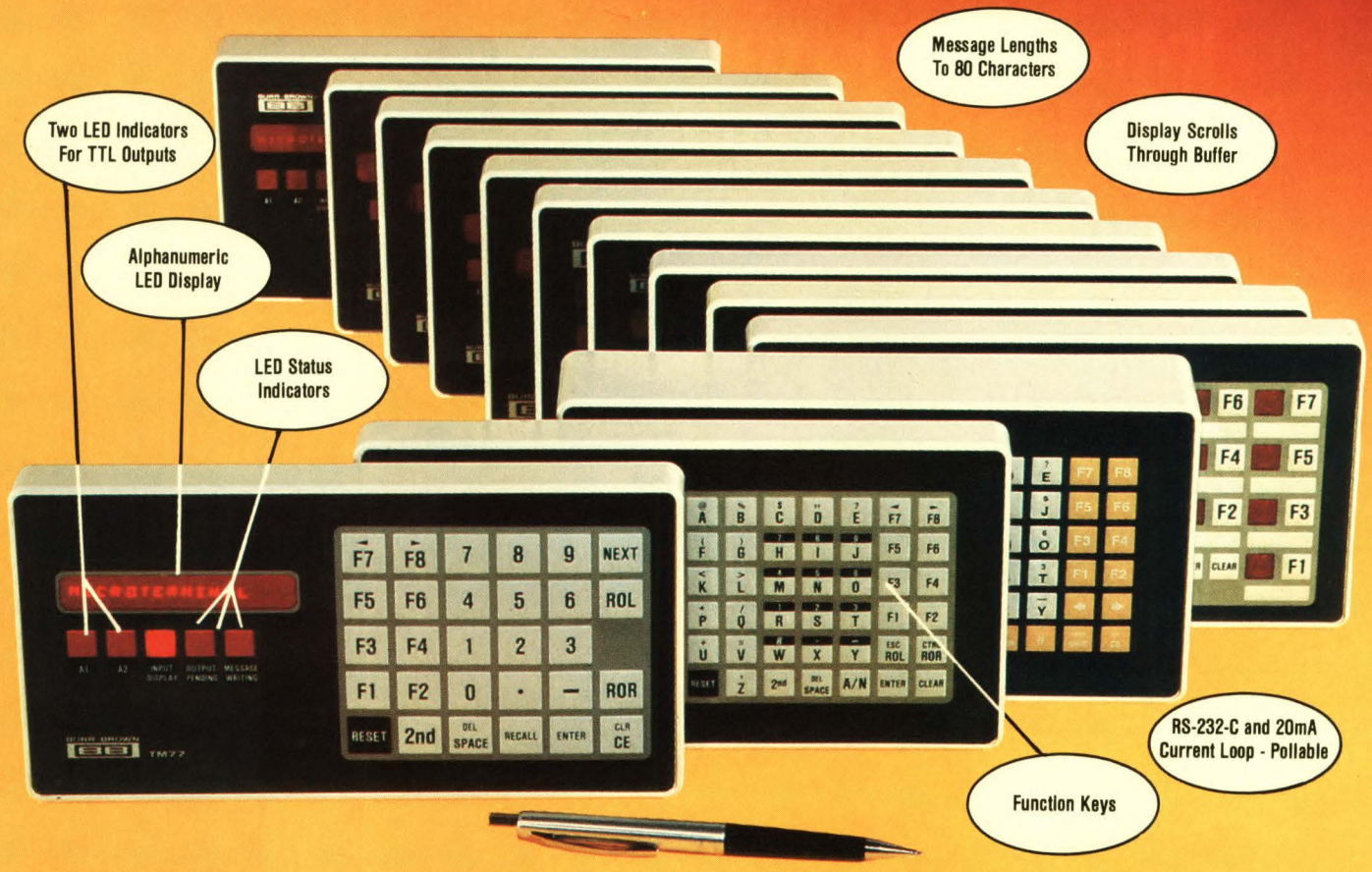
```
RETRANSMIT: PROCEDURE;

   /* PARAMETERS FOR THIS COMMAND ARE TAKEN FROM
      THE TEMPORARY STORAGE USED DURING THE LAST
      TRANSMIT COMMAND */

   CALL DMA_LOAD(TX_CHANNEL,1,TX_BUFFER_LEN,
      TX_BUFF_PTR):
   OUTPUT  (CS_588) = 12 OR SHL (TX_CHANNEL,4);
                              /* RETRANSMIT */
   RETURN;

END RETRANSMIT;
```

Program 3. Mission accomplished

```
RCV_ENABLE: PROCEDURE(CHANNEL,BUFFER_PTR);


   DECLARE CHANNEL BYTE;
   DECLARE BUFFER_PTR POINTER;

   CALL DMA_LOAD(CHANNEL,0,2048,BUFFER_PTR);
   OUTPUT(CS-588) = 8 OR SHL (CHANNEL,4);
   RETURN:

END RCV_ENABLE;
```

How useful?	Circle
Immediate design application	541
Within the next year	542
Not applicable	543

13 Small, Smart Solutions For Data Entry & Display



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TM77	16	110-19200	320(1)	Numeric	14	Larger keys	+5VDC
TM71-I/O	16	110-19200	320(1)	Alpha	14	TTL I/O	+5VDC
TM77-I/O	16	110-19200	320(1)	Numeric	14	Larger keys	+5VDC
TM71B TM71MS	16	110-19200	320(1) 5 x 50(2)	Alpha	16	Bar Code Wand	+24VAC/ DC
TM77B TM77MS	16	110-19200	320(1) 5 x 50(2)	Numeric	16	Mag Stripe Reader	+24VAC/ DC
TM71M	16	110-9600	320	Alpha	14	Military	+5VDC
TM70	12	300 & 1200	36	Alpha	8	Low cost	+5VDC
TM76	12	300 & 1200	36	Numeric	8	Larger keys	+5VDC
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CIRCLE 70

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GPIB	STD	STD	STD
Counter/Timer/Trigger-Word Recognizer	STD	STD	STD
P6131 (4 probes)	STD	STD	STD
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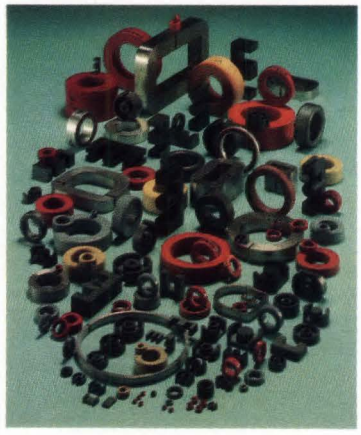

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CIRCLE 72

Controller chips pair up in S interface for ISDN systems

Two CMOS LSI chips, the chief building blocks of a system terminal and a PBX line card, simplify implementation of the S interface for ISDN links.

The emergence of all-digital telephone networks using packet- and circuit-switched data schemes will open the door to many new telecommunication services, including electronic mail, banking, alarm signaling, and the transfer of information via telex and facsimile facilities.

Already the International Telephony and Telegraphy Consultative Committee (CCITT) has recommended standards for an S interface on the premises of subscribers to the Integrated Services Digital Network (see "Interface Standard Ensures Compact Subscriber Networks," p. 158). This microprocessor-controlled interface to the ISDN will give subscribers simultaneous access to two 64-kbit/s voice or data channels and one 16-kbit/s control channel. Voice-band signals are to be digitized at the subscriber's terminal and transmitted over one of the 64-kbit/s channels. It will be possible to link all three channels to a main computer for central handling over pulse-code-modulated (PCM) highways.

Alan Clark, Advanced Micro Devices Inc.
Alan Clark, currently ISDN product marketing manager at AMD in Sunnyvale, Calif., joined the company in March 1983 as a development engineer. Before that, he designed microprocessor-based control systems for power stations at Babcock-Bristol Ltd. in the United Kingdom. He holds a BSc in mathematics and physics and a PhD in digital signal processing from the Polytechnic of Central London.

Although it will be some time before system specifications are completely defined, help in implementing the S interface is at hand in the form of two CMOS chips: the Am7930 digital subscriber controller and the Am7931 digital exchange controller. They are the first LSI circuits to meet the CCITT's basic design criteria for ISDN terminals and private branch exchange (PBX) line cards.

The subscriber controller chip is the heart of either a basic or an advanced ISDN terminal driven by an 8-bit microprocessor; it gives the customer access to the data-handling facilities on the S interface. For PBX design, the exchange controller chip is used to build the required number of S interfaces on the line card (one chip for each interface). Residing on the PBX line card itself, the device provides the exchange information function for one ISDN subscriber line.

Both chips allow full-duplex data transfer at 192 kbits/s over four wires between the subscriber's terminal equipment and the PBX line card. These ICs support the point-to-point and point-to-multipoint connections described in the CCITT recommendations, with the data framed on the 64-kbit/s voice and data (B1 and B2) channels and the 16-kbit/s control and data (D) channel.

The main blocks of the subscriber controller chip are a line interface unit, a data link controller, a multiplexer, a main audio processor,

and a microprocessor interface (Fig. 1a).

The line interface is connected to the four-wire S interface by a pair of isolating transformers, one for transmission and the other for receiving. The transmitter, which has a binary-to-pseudoternary encoder and a line driver, receives the B channel data from the multiplexer and the D channel data from the data link controller. It then couples these signals to the S interface.

The unit's receiver recovers data and timing from the S interface; it also presents data from the B channels (via the multiplexer) and the D channel (via the data link controller) to the subscriber. The receiver, in essence performing a function inverse to that of the transmitter, converts pseudoternary-coded signals into binary before delivering them to other blocks within the IC.

Data processing is coordinated by the data

Interface standard ensures compact subscriber networks

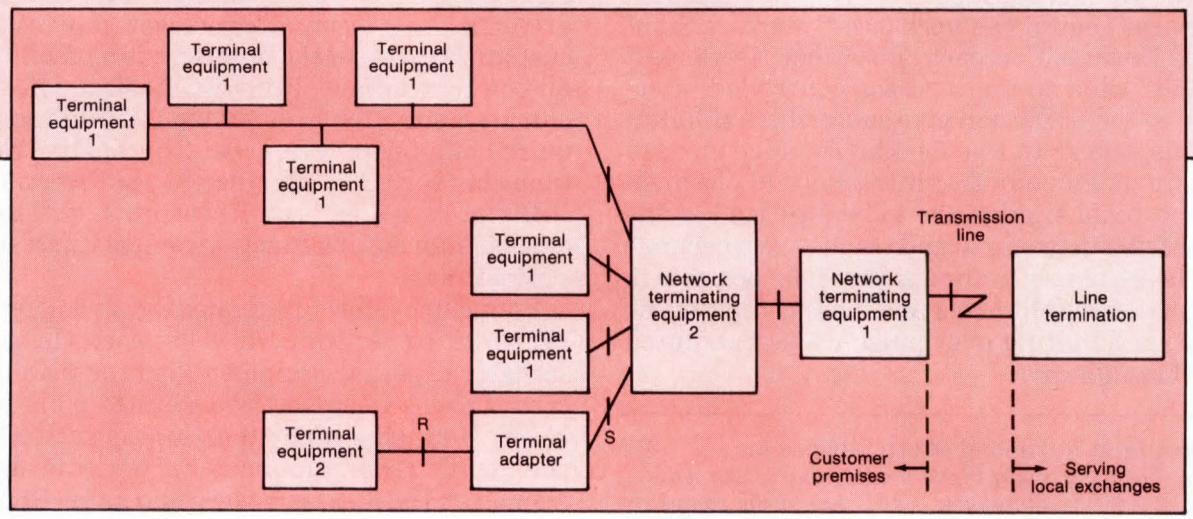
The CCITT's proposals for an interface standard ensure that a small set of ICs can meet the requirements of an evolving telecom network as it moves toward an all-digital state. Two main subscriber configurations—point-to-point and point-to-multipoint—have been recommended for use with the S interface, which is a four-wire module operating at 192 kbits/s (48-kbit data/control frame structure).

In the point-to-point setup, one telephone or terminal is connected via an S interface to a line card in the local exchange through cables no longer than 1 km. The point-to-multipoint configuration may join up to eight telephones or terminals with one S interface, and cable runs to the local exchange are 150 meters or less.

The function of the terminal equipment is virtually identical in both configurations. With the network terminating equipment, however, there is a difference; whereas some equipment would be tied into a single terminal on the subscriber's premises, in larger installations it would be in PBXs using multiple terminals.

In the latter case, network terminating equipment 1 (see the figure) would connect to the transmission line on one side and present the standard S interface at point T on the other side. Network terminating equipment 2 would be optional and would provide line termination for network terminating equipment 1. Terminals that operate with existing standards (like the RS-232) would attach at reference point R and use a terminal adapter for interface buffering.

The transmission line (for which there is yet no standard) would connect either to the line terminator or to a central office line card. The transmission line media, which vary from country to country, could be two-wire, four-wire, fiber-optic, microwave or satellite linkups.



link controller, which extracts the D channel information from the S interface and transmits the microprocessor-generated D channel information over the S interface. The controller also performs bit checking and frame checking for error detection, and it generates various detection flags when necessary.

In operation, the system's master, or external, microprocessor initializes the data link controller and performs the higher-level protocol processing. A random-number generator in the data link controller provides an address for the subscriber controller chip when the IC is powered up for operation on the S interface. When the chip is receiving, data flows via the D channel from the line interface unit through the microprocessor interface. This flow reverses when the chip is transmitting.

The device's protocol permits terminals in the point-to-multipoint configuration to access the D channel in an orderly way. When two or more terminals attempt to access the D channel simultaneously, one will always be successful in completing transmission of its information. This procedure also permits the terminals to operate in a point-to-point configuration.

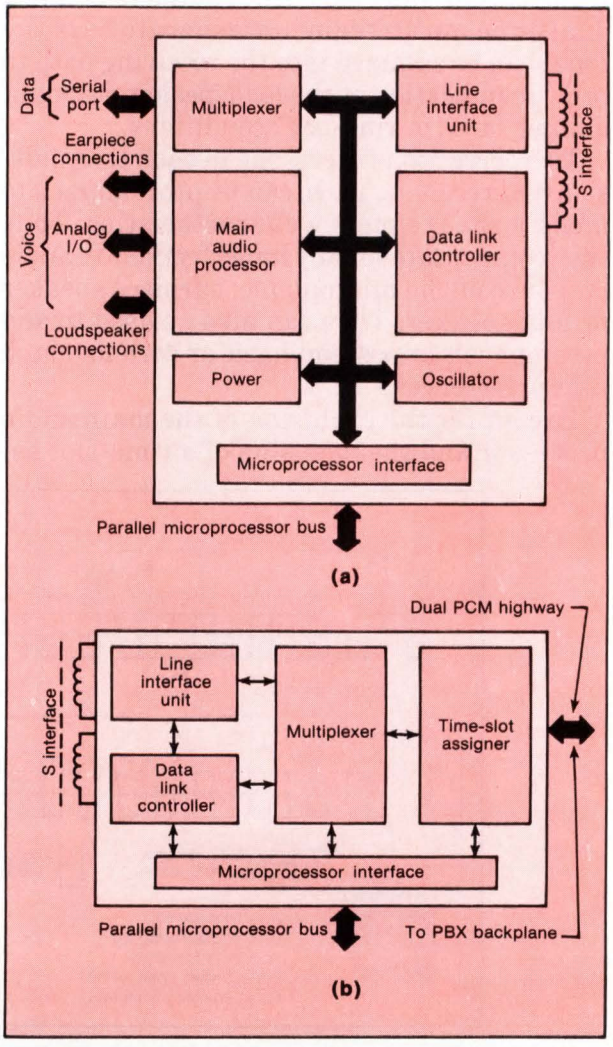
Selective response

The data link controller will recognize 1- or 2-byte addresses and the first 2 bytes in a longer address. This allows the user to program the chip to respond only to selected addresses. In this way the terminals interrupt their respective microprocessor only when their preprogrammed address is received. The data link controller can also be programmed to bypass the address-decoding phase and to pass the entire packet to the microprocessor.

As the data link controller receives the D channel information from the line interface unit, it alerts the external microprocessor by generating suitable interrupts (if there is no interrupt mask). The microprocessor determines the source of an interrupt by reading the interrupt register, and it then accesses the appropriate error or status registers.

The circuitry to access the subscriber controller's programmable, status, and error registers, as well as its transmitting and receiving buffers, is all in the microprocessor interface block. This section has the logic to interface the chip to an external 8-bit microprocessor. Controlling the multiplexing of the B1 and B2 channels to and from different sources is the job of the programmable multiplexer. Possible source and destination pairings include the line interface unit, the main audio processor, the microprocessor interface, and the serial port, with the port providing a serial interface to external peripherals.

Generating suitable audio responses and



1. The Am7930 digital subscriber controller for telephone systems contains circuitry for accessing the S interface defined by the CCITT (a). This device is on the subscriber's premises. The Am7931 digital exchange controller provides the S interface and line termination functions for the subscriber controller (b). The IC is on the private branch exchange (PBX) line card.

tones is the responsibility of the main audio processor block. In addition to digital filtering circuits, it has digital-to-analog and analog-to-digital converters. It will drive a handset earpiece or a loudspeaker, and its analog input accepts a handset mouthpiece, a separate microphone, or both.

The multitone generator in this block can provide a one- or two-tone signal with programmable frequency, amplitude, and cadence. One or more tones can be summed into the transmission (and side-tone) paths to create a dual-tone multifrequency generator. Or the tones can be summed into the receiving path to provide indication at the loudspeaker output of dialing, busy, or ring-back conditions.

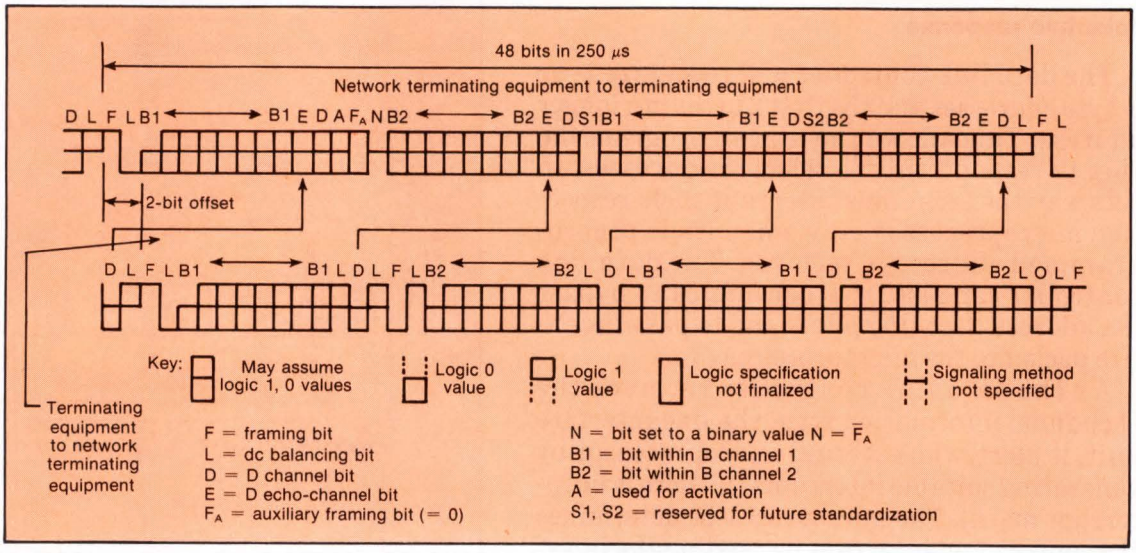
Two correction filters, one in each transmission and receiving path, can be programmed to modify the frequency characteristics. Thus they compensate for any imperfections in audio response of the microphone, earpiece speaker or loudspeaker. They can also be used to add preemphasis or postemphasis or both to match user preferences.

Except for the exclusion of the main audio processor and the inclusion of a time-slot assigner, the main blocks in the exchange controller chip are the same as those of the subscriber controller (Fig. 1b). There are, however, some operational differences within the blocks of the exchange controller.

First, the line interface unit can be operated in two modes: adaptive timing for point-to-point applications and fixed timing for point-to-multipoint. The mode is selected by an internal register that the local external microprocessor programs.

Also, the exchange controller's multiplexer can route data from the microprocessor interface and the B1, B2, and D channels to the time-slot assigner. The multiplexer performs these operations in addition to the routing options specified for the multiplexer in the subscriber controller chip. When the D channel is routed to the time-slot assigner, it bypasses the data link controller. Hence the central computer has direct access, over the dual PCM highway, to the B1, B2, and D channels to or from the S interface, as well as to the local external microprocessor.

Significantly, the exchange controller chip is compatible with the Am7901A subscriber line



2. The data frame structure with which the subscriber and exchange controllers communicate over the S interface operates at 192 kbits/s. During each 48-bit (250-μs) frame, two voice/data streams and one control/data stream are sent from the network terminating equipment to the terminal equipment. The identical format controls communications between terminal equipment and network terminating equipment after a check for line contention has been performed by the terminal equipment (D to E bit query). The CCITT ISDN recommendation gives a full definition of frame structure and bit polarities.

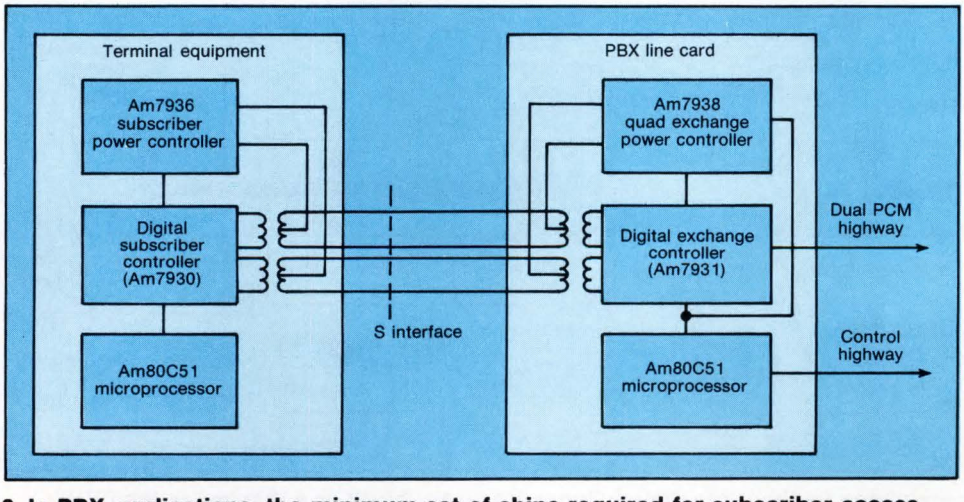
audio-processing circuit (SLAC) used in analog line cards, because both parts support a dual PCM interface. Therefore digital line cards can replace analog line cards on a one-to-one basis within the same PBX. The practical advantage is that an analog system can be gradually modified to an all-digital one. Most importantly, because of the backplane compatibility between the exchange controller chip and the subscriber line audio processing circuit (vis-à-vis the dual PCM highway), systems can be developed that connect the S interface point to analog trunk lines. This configuration befits public telephone communication.

Picking the right slot

The exchange controller's dual PCM interface has independent control of the transmission and receiving paths. The frame synchronization signal identifies the beginning of the frame and establishes a reference point for all time slots. The dual PCM interface can operate at up to 8.192 Mbits/s and therefore will be able to accommodate 256 time slots at 64 kbits/s. During each frame, two 64-kbit/s B channels (8-bit time slots) and one 16-kbit/s D channel (2-bit time slot) may be transferred to or from the dual PCM highway (Fig. 2). Time-slot assignment and highway selection is under program control of the line card microprocessor.

The on-chip time-slot assigner allows a number of the exchange controllers to be connected together and to the PBX backplane. The assigner can be programmed by the microprocessor to transmit or receive data to or from the B or D channels over the PCM highway. Or it can be programmed to send or receive data from the microprocessor. The local microprocessor may thus communicate with the central computer over the dual PCM interface.

When suitably configured with other available chips to create a simple PBX, the subscriber and exchange controller chips can be used in applications ranging from a simple voice telephone to a sophisticated voice/data terminal. In its simplest form, an ISDN terminal using the devices requires a microprocessor and keypad. The microprocessor scans the keyboard and constructs the signaling messages for the D channel. The only other circuits required (Fig. 3) are the Am7936 subscriber power controller and the Am7938 quad exchange power



3. In PBX applications, the minimum set of chips required for subscriber access over the S interface comprises a digital subscriber controller, a digital exchange controller, a subscriber power controller, a quad exchange power controller, and two 8-bit microprocessors. The rudimentary connection shown establishes standard telephone service.

ISDN controller chips

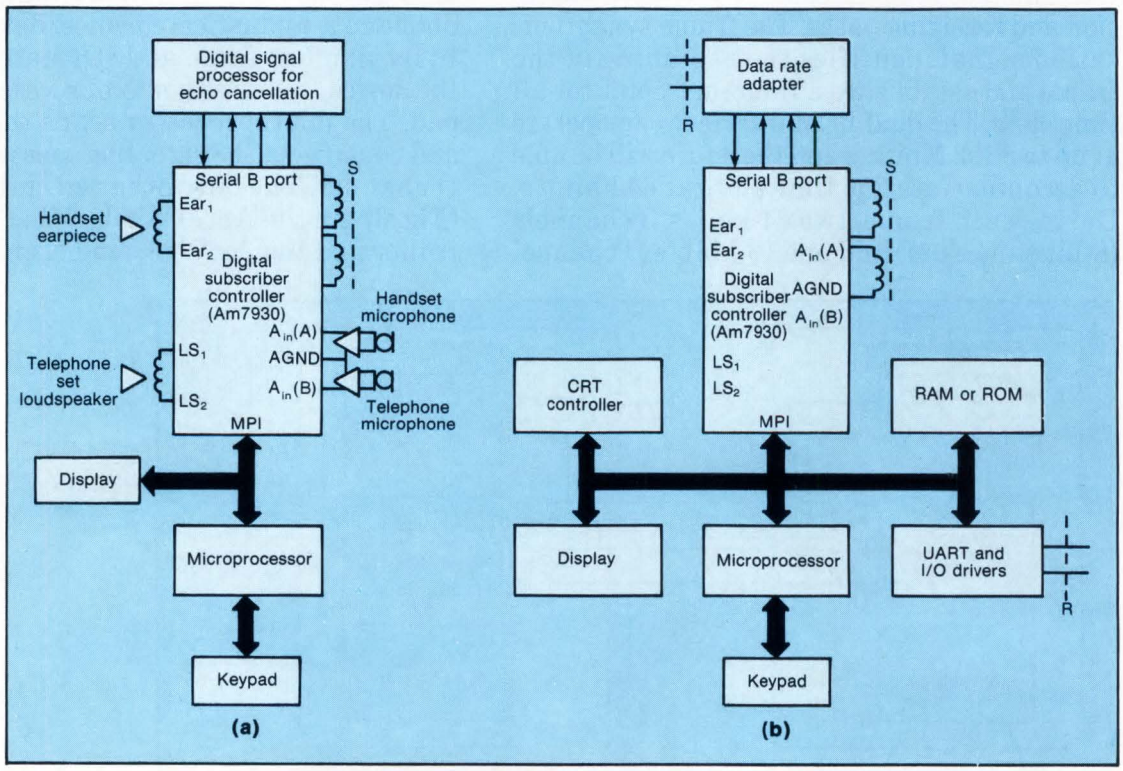
controller, plus two bipolar high-voltage ICs to supply the required voltage and power levels over the S interface.

In the PBX application, a 40-V input to the S interface from the quad exchange power controller is converted by the subscriber power controller into a 5-V dc output, enough to power the ICs in the terminal equipment. One quad exchange power controller can drive up to four S interfaces.

The subscriber controller chip can be used in a variety of terminal equipment, from simple voice-only setups and hands-free phones to a full workstation (Fig. 4). To connect ISDN circuits to existing equipment, the chip's serial or microprocessor ports can be used to access the CCITT's R interface point, which can be any interface—for instance, an RS-232.

Multiple exchange controller chips may be used on one PBX line card to provide the required number of S interfaces. One microprocessor can control up to eight S interfaces and can be linked to the line card's backplane via an Am8530 serial communications controller that connects to the parallel microprocessor bus. Or the microprocessor can communicate with the line card over the dual PCM highway of an exchange controller.

For practical implementation of an S interface on the ISDN, consider a telephone capable of supporting one analog line (one two-way conversation) and an RS-232 data link (Fig. 5). Ideally all the ICs would reside in the telephone, with a standard RS-232—compatible connector



4. The voice-only phone (without the digital signal processor block or a display) is the ISDN equivalent of the standard analog phone. A digital signal processor may be interfaced to the serial B port for echo cancellation and voice encryption, yielding secure hands-free operation (a) with on-hook dialing. In voice and data workstations, the subscriber controller chip combines with a number of peripherals, including memory, UART, CRT controller, and a microprocessor—all connected to the same microprocessor bus (b).

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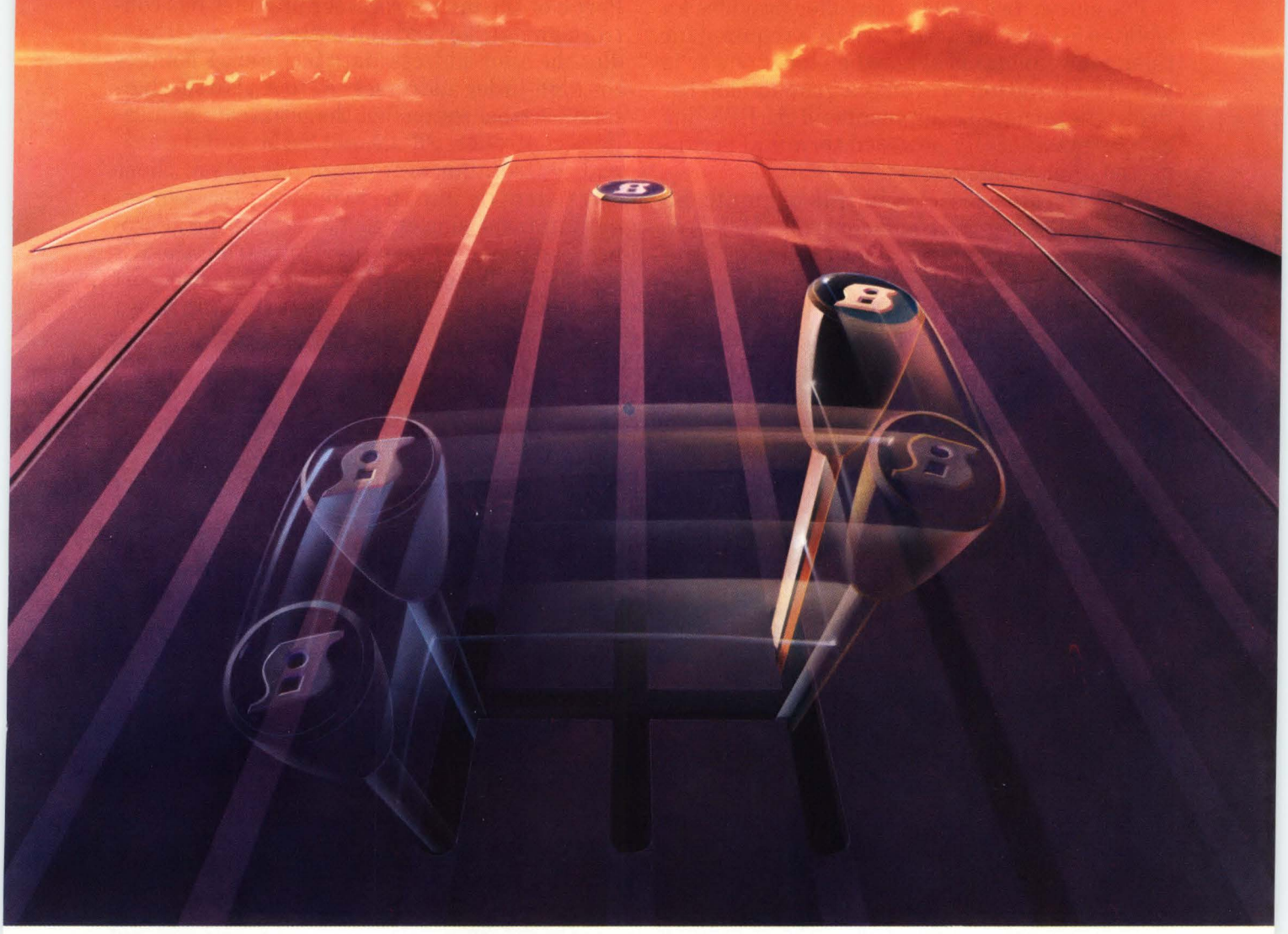

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Phone ( ) _____

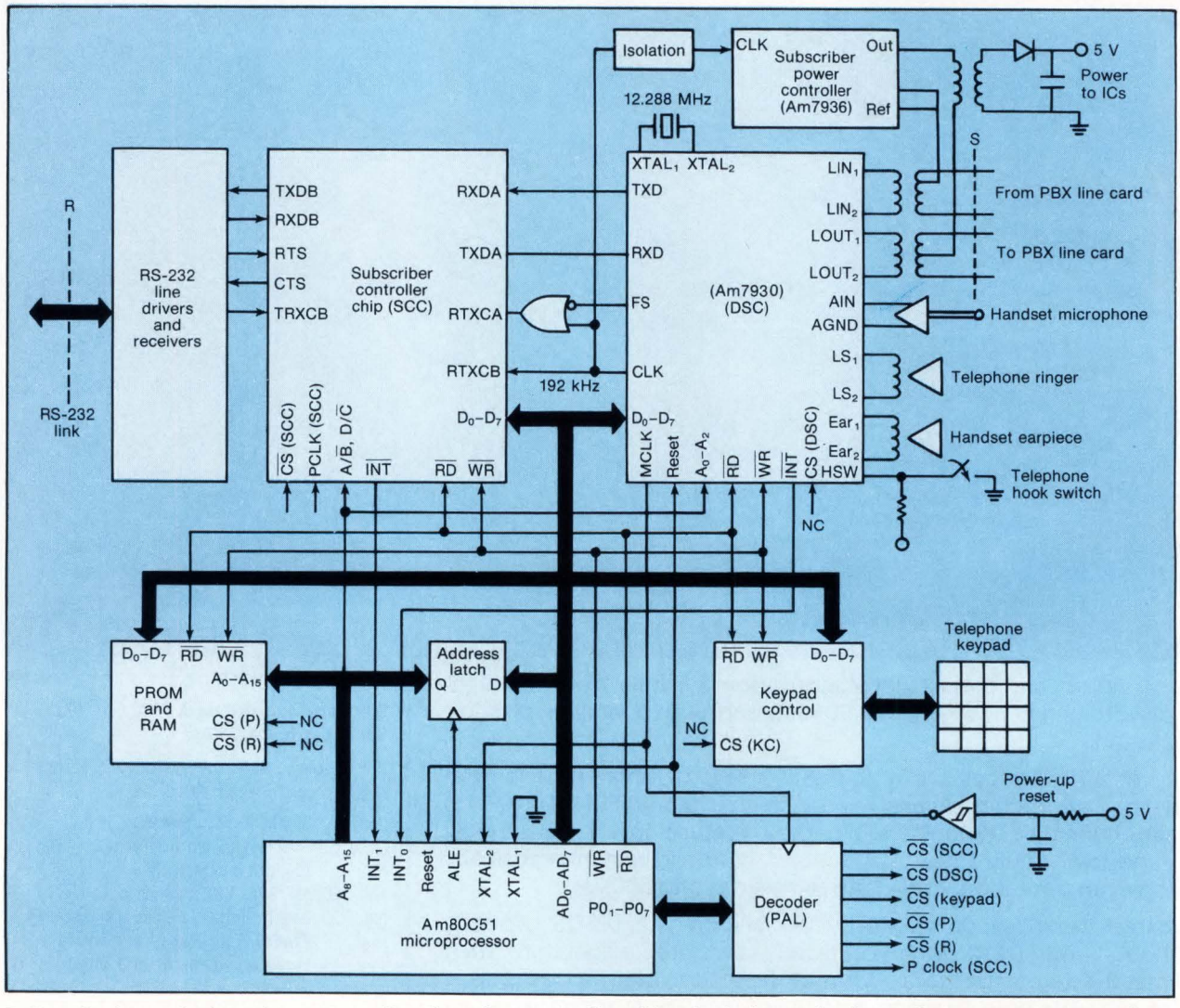
Expiration date 6/30/85

ISDN controller chips

built into the side of the telephone set.

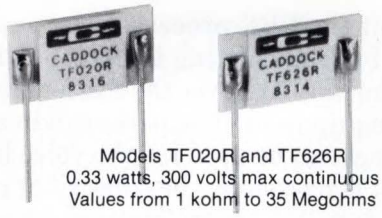
The subscriber power controller provides an isolated 5-V dc output to power ICs required for telephone functions even when local power is lost. The isolation prevents a ground loop between the terminal equipment and the PBX line card when a locally powered terminal is connected to the telephone set.

The microprocessor—in this example, an Am80C51—programs and controls the ICs in the terminal equipment, as instructed by commands generated by the PBX line card, keypad, or RS-232 link. This configuration allows the microprocessor to use its standard 8-bit bus. Port 3 of the microprocessor provides bus control signals (like read and write) and port 0 handles the 8-bit address/data bus. Port 2 handles the high-order addresses (A_8 to A_{15}) to the digital subscriber controller, the serial communications controller, PROM and RAM, and the keypad control. Both interrupt outputs of those controllers tie into the two microprocessor input interrupt pins on port 3, so that the microprocessor can service interrupts from the ICs separately. In addition, with a PAL device, port 1 on the microprocessor delivers the Chip Select



5. Practical terminal equipment applications for controller chips include a telephone that supports one voice line and one data link simultaneously. Memory devices—which should be large enough to accommodate expanded system telephone functions—contain the operating protocols and software for system initialization.

Type TF Ultra-Precision Film Resistors from Caddock: Absolute Tolerances to ±0.01% with TC's to 5 PPM/°C and Resistance Values from 1 kohm to 125 Megohms.



Models TF020R and TF626R
0.33 watts, 300 volts max continuous
Values from 1 kohm to 35 Megohms

Models TF050R and TF656R
0.75 watts, 1400 volts max continuous
Values from 10 kohms to 125 Megohms

Caddock's Tetrinox® resistance film technologies achieve unique ultra-precision resistor performance.

Tetrinox®—Caddock's advanced resistance film technology—combined with high-thru-put manufacturing technologies, results in a unique approach to the production of ultra-precision resistors.

The Type TF resistors utilize these technologies to provide a highly producible ultra-precision resistor with low temperature coefficients, high stability and an extended resistance range.

Resistance values up to 125 Megohms provide a new design element.

The exceptionally wide range of resistance values from 1 kohm to as high as 125 Megohms make the Type TF Ultra-Precision Resistors ideal for new design opportunities.

And in existing designs, Type TF resistors are widely used to replace ultra-precision wire-wound resistors. For purposes of price comparisons with ultra-precision wire-wound resistors, here are representative Type TF prices in 2500-unit quantities:

Model No.	Resistance	Tolerance	TC	Unit Price
TF 020 R-	1 k	-0.01%	-10 PPM/°C	$2.67
TF 020 R-	10 k	-0.01%	-10 PPM/°C	$2.67
TF 020 R-	100 k	-0.01%	-10 PPM/°C	$2.93
TF 020 R-	1 Meg	-0.01%	-10 PPM/°C	$4.94
TF 626 R-	10 Meg	-0.01%	-10 PPM/°C	$6.47

The high producibility and unit-to-unit consistancy of Type TF resistors also assures 6-to-8 week delivery on even large production quantities, and many resistance values are available from stock.

Seven Absolute Tolerances from ±1.0% to ±0.01%.

For maximum design flexibility, Type TF resistors are available in seven resistance tolerances:

±0.01%, ±0.025%, ±0.05%, ±0.1%
±0.25%, ±0.5% and ±1.0%

This wide range of absolute tolerances gives circuit designers optimum price-performance characteristics in all applications.

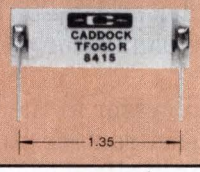
Type TF Resistance Range from 1 kohm to 125 Megohms

Model Number Radial Leads	Wattage @ +70° C.	Maximum Continuous Oper. Voltage	Resistance Min.	Resistance Max.	Dimensions Length	Dimensions Height
TF 020 R	0.33	300	1 K	2 Meg	0.75 ± .020	0.375 ± .020
TF 050 R	0.75	1400	10 K	10 Meg	1.50 ± .020	0.50 ± .020
TF 626 R	0.33	300	2.01 Meg	35 Meg	0.75 ± .020	0.375 ± .020
TF 656 R	0.75	1400	10.01 Meg	125 Meg	1.50 ± .020	0.500 ± .020

Models TF 020 R and TF 626 R

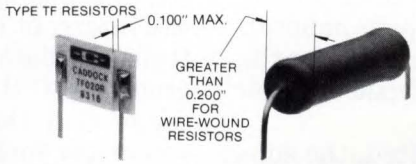
ALL DIMENSIONS IN INCHES

Models TF 050 R and TF 656 R



Thin-profile Type TF resistors save installation space.

The thin profile of the Type TF resistors make them an ideal replacement for the large-bodied wire-wound resistors.



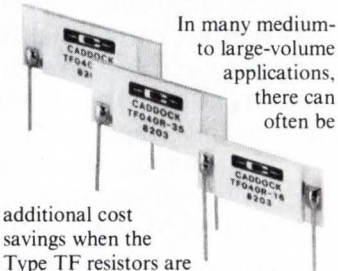
And the radial leads of the Type TF resistors also simplify their installation into PC boards.

Three Temperature Coefficients of 5 PPM/°C, 10 PPM/°C and 15 PPM/°C.

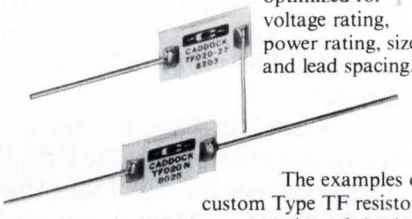
The choice of three Absolute Temperature Coefficients - 5 PPM/°C, 10 PPM/°C and 15 PPM/°C - in all models and values of Type TF resistors permits each circuit's requirements to be achieved on an efficient performance versus cost basis.

These temperature coefficients apply over the temperature range of -15° C to +105° C, referenced to +25° C.

Custom Type TF resistors with special performance and configurations can achieve optimum cost-effectiveness.



In many medium- to large-volume applications, there can often be additional cost savings when the Type TF resistors are optimized for voltage rating, power rating, size and lead spacing.



The examples of custom Type TF resistors shown here include the same choices of absolute tolerance, temperature coefficient and resistance value that are available in the standard radial-lead Type TF Ultra-Precision Film Resistors.

Discover how easily these problem-solving resistors can improve the performance and reliability of your equipment, too. For your copy of the latest edition of the Caddock 24 page General Catalog, and specific technical data on any of the more than 150 models of the 13 standard types of Caddock High Performance Film Resistors and Precision Resistor Networks, just call or write to -

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CADDOCK

HIGH PERFORMANCE FILM RESISTORS

CIRCLE 74

signal ($\overline{CS}$) to the ICs and a clock to the serial communications controller.

The amount of memory (PROM and RAM) needed depends on the sophistication of the terminal equipment. The PROM contains the LAPD (Link Access Protocol Type D) protocol, keypad, and initialization routines for the subscriber and communications controllers. The number of programs in the PROM—and hence its size—will grow as the local terminals that need the RS-232 link increase and as telephone functions are added to the system (for example, call forwarding, call holding, and automatic redialing). Therefore the PROM area should be upwardly compatible to accept EPROMs of 16 to 64 kbytes. The RAM is used by the microprocessor to store temporary information and to adapt the data rate of the information passed between the RS-232 link and the S interface.

The subscriber controller chip is connected to the telephone earpiece, ringer, microphone, and hookswitch, and, via the S interface to the PBX line card. The serial port on the device connects to one of the serial ports of the serial communications controller. The other serial port on that controller, connected to the differential line drivers and receivers, provides an RS-232 link to a local terminal from the connector on the side of the telephone set.

On power-up, the microprocessor in the terminal equipment enters a reset routine stored in the PROM. This routine initializes the subscriber and communications controllers, then disables them, and the microprocessor then scans the keypad (via the keypad controller) for activity. The terminal equipment can now begin transmitting and receiving to and from the S interface, RS-232 link, and telephone handset. It can be activated by the PBX line card over the S interface or locally, from the keypad or when the handset is lifted.

If the telephone handset is lifted, the subscriber controller chip will interrupt the microprocessor, which interrogates the device's interrupt register and establishes that a voice connection has been requested. The microprocessor then transmits a data packet over the D channel to the PBX, requesting that a B channel be made available for the telephone conversation. (This transmission is over the S interface via the on-chip data link controller.)

At this point the PBX processes the packet and responds by transmitting a corresponding packet from the line card over the S interface to the terminal equipment. The packet indicates which B channel can be used for the voice link, and the packet is passed by the subscriber controller, via its data link controller, to the microprocessor. The microprocessor decodes the packet and programs the chip to connect its main audio processor to the designated B channel on the S interface. With the telephone link thus established, the subscriber will hear the dial tone and be able to dial the telephone number.

The microprocessor scans the keypad for the number being dialed, then transmits it to the PBX on the D channel. The PBX decodes the number and makes the connection. The subscriber will hear the connected telephone ringing, and conversation can begin when the phone is answered via the designated B channel.

The microprocessor and the PBX line card interact similarly when a local terminal is connected to the RS-232 port and the subscriber requests data transmission via the keypad. Unlike voice transmission, however, the microprocessor in this case will program the subscriber controller to route the designated B channel to the serial port, thus providing a link to the serial communications controller. The microprocessor will also program that controller to process the data going to and coming from the subscriber controller's serial port.

A voice from beyond

On the other hand, when the PBX initiates a voice transmission, the subscriber controller will interrupt the microprocessor and pass the D channel data from the line card to the microprocessor. If the line card is requesting a voice connection, the microprocessor instructs the subscriber controller to activate the telephone ringer and make the B channel link, so that conversation can begin when the telephone is answered.

If the PBX requests a data link to the RS-232 interface, the microprocessor will program the subscriber controller accordingly, route the designated B channel to the chip's serial port, and monitor the data transfer. Since the S interface can support two 64-kbit/s B channels,

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CIRCLE 76

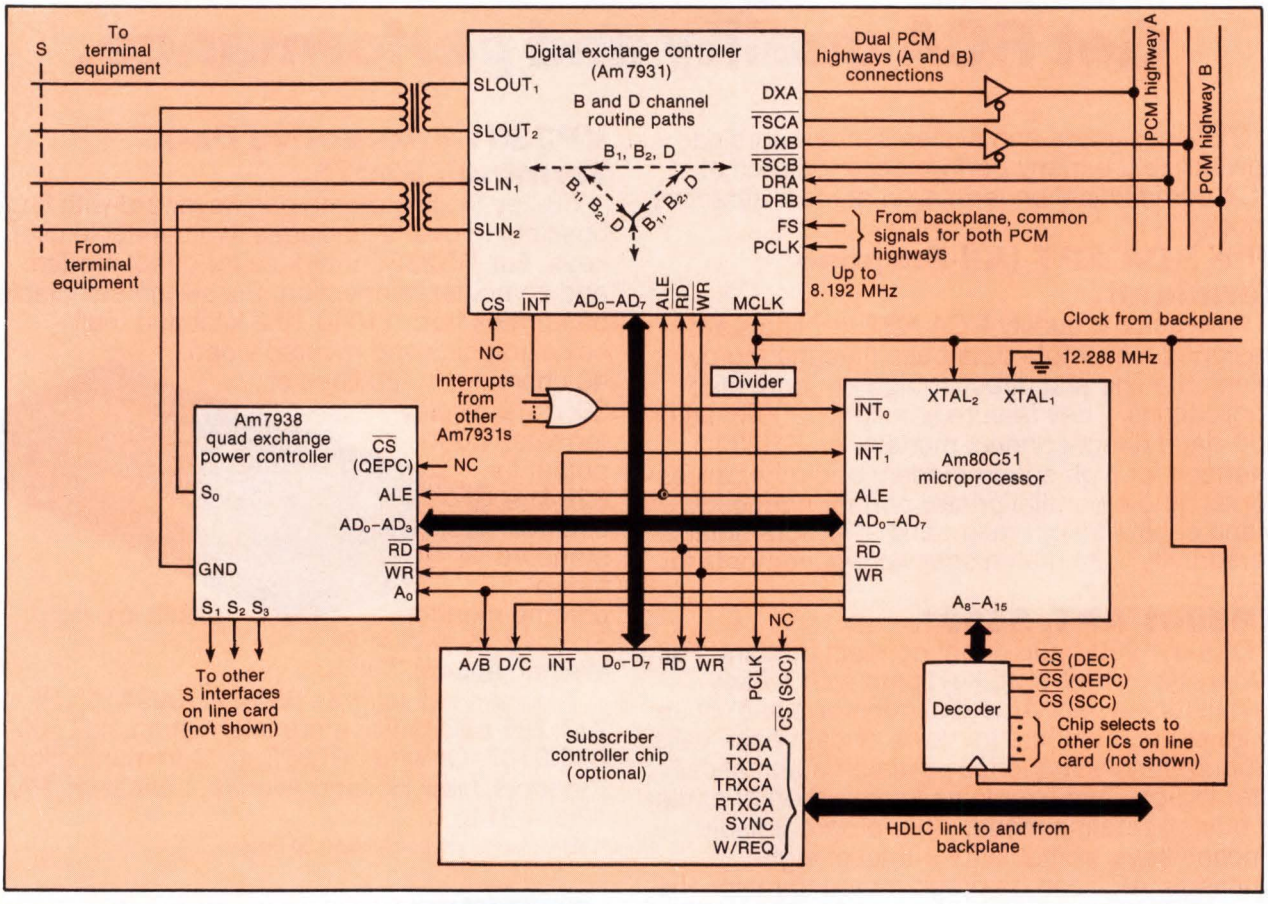
ISDN controller chips

voice and data links can be made and run simultaneously.

Whenever a data link is made, from either the subscriber or the PBX line card, the data flows from the local terminal via the RS-232 link through the subscriber controller into the RAM on the microprocessor bus. The data is stored in the RAM and retransmitted on the microprocessor bus through the other serial port on the communications controller. Then it enters the subscriber controller's serial port and passes through the S interface on the designated B channel.

For data coming from the S interface, the data is transmitted through subscriber controller's serial port into the communications controller, then into the RAM via the microprocessor bus. When the data is collected in the RAM, it is retransmitted over the microprocessor bus through the other communications controller serial port, then onto the RS-232 link, and finally to the local terminal.

When the SCC is in the HDLC (High-level Data Link Control) mode, packet data can be transmitted to and received from the local terminal over the S interface via the B channels. Use of the RAM for temporary storage of data coming from and going to the local terminal al-



6. The exchange controller chip is ideal for establishing a PBX, as shown on a section of the line card (only one S interface). The microprocessor would be common to all exchange controllers. The quad exchange power controller can provide power for up to four S interfaces.

NEW PRODUCT NEWS FROM TELETEK

Systemaster II. Responding to market demand for speed and increased versatility, Teletek is proud to announce the availability of the next generation in 8-bit technology — the new Systemaster II! The Systemaster II will offer two CPU options, either a Z80B running at 6 MHz or a Z80H running at 8 MHz, 128K of parity checked RAM, two RS232 serial ports with on-board drivers (no paddle boards required), two parallel ports, or optional SCSI or IEEE-488 port. The WD floppy disk controller will *simultaneously* handle 8" and 5¼" drives. A Zilog Z-80 DMA controller will provide instant communications over the bus between master and slave. Add to the DMA capability a true dedicated interrupt controller for both on-board and bus functions, and the result is unprecedented performance. Systemaster II will run under CP/M 3.0 or TurboDOS 1.3, and fully utilize the bank switching features of these operating systems.

SBC 86/87. As the name indicates, Teletek's new 16-bit slave board has an Intel 8086 CPU with an 8087 math co-processor option. This new board will provide either 128K or 512K of parity checked RAM. Two serial ports are provided with individually programmable baud rates. One Centronics-compatible parallel port is provided. When teamed up with Systemaster II under TurboDOS 1.3, this 5MHz or 8MHz multi-user, multi-processing, combination cannot be beat in speed or feature flexibility!

Teletek Z-150 MB. Teletek is the first to offer a RAM expansion board designed specifically for the Z-150/Z-160 from Zenith. The Teletek Z-150 MB is expandable from 64K to 384K. Bring your Z-150 up to its full potential by adding 320K of parity checked RAM (or your IBM PC, Columbia, Compaq, Corona, Eagle, or Seequa to their full potential). The Teletek Z-150 MB optionally provides a game port for use when your portable goes home or a clock/calendar with battery backup!

Evaluate the Systemaster II, SBC 86/87 or Teletek Z-150 MB for 30 days under Teletek's Evaluation Program. A money-back guarantee is provided if not completely satisfied! All Teletek products carry a 3-year warranty.

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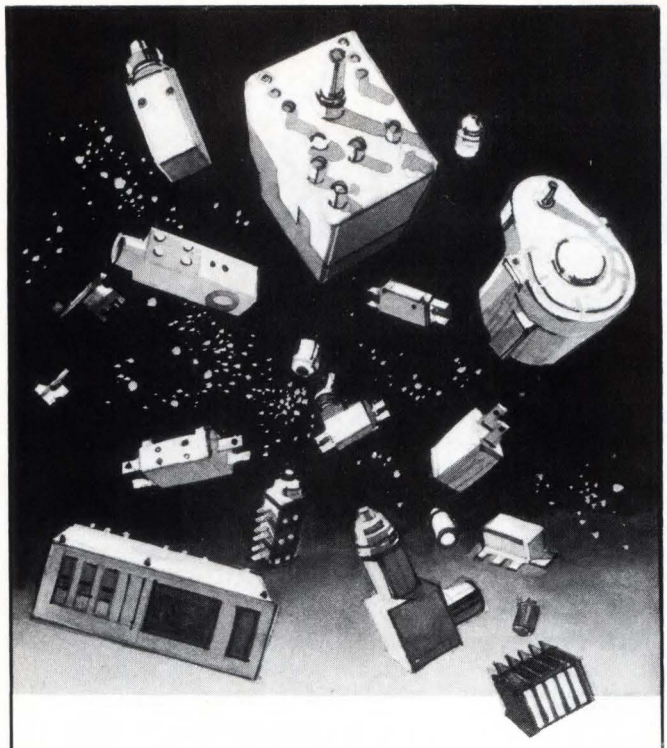

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CIRCLE 78

ISDN controller chips

lows these operations to occur at different rates. With this capability, data can be transmitted through the system at a fixed 64 kbits/s, required for the B channel, regardless of the rate at which it was originally received.

Extending the highway

Another example shows a portion of a typical PBX line card architecture and the connections and ICs associated with one S interface (Fig. 6). The microprocessor is common to all the exchange controller chips on the line card, and the quad exchange power controller provides the power for up to four S interfaces. The decoder provides the necessary chip select signals.

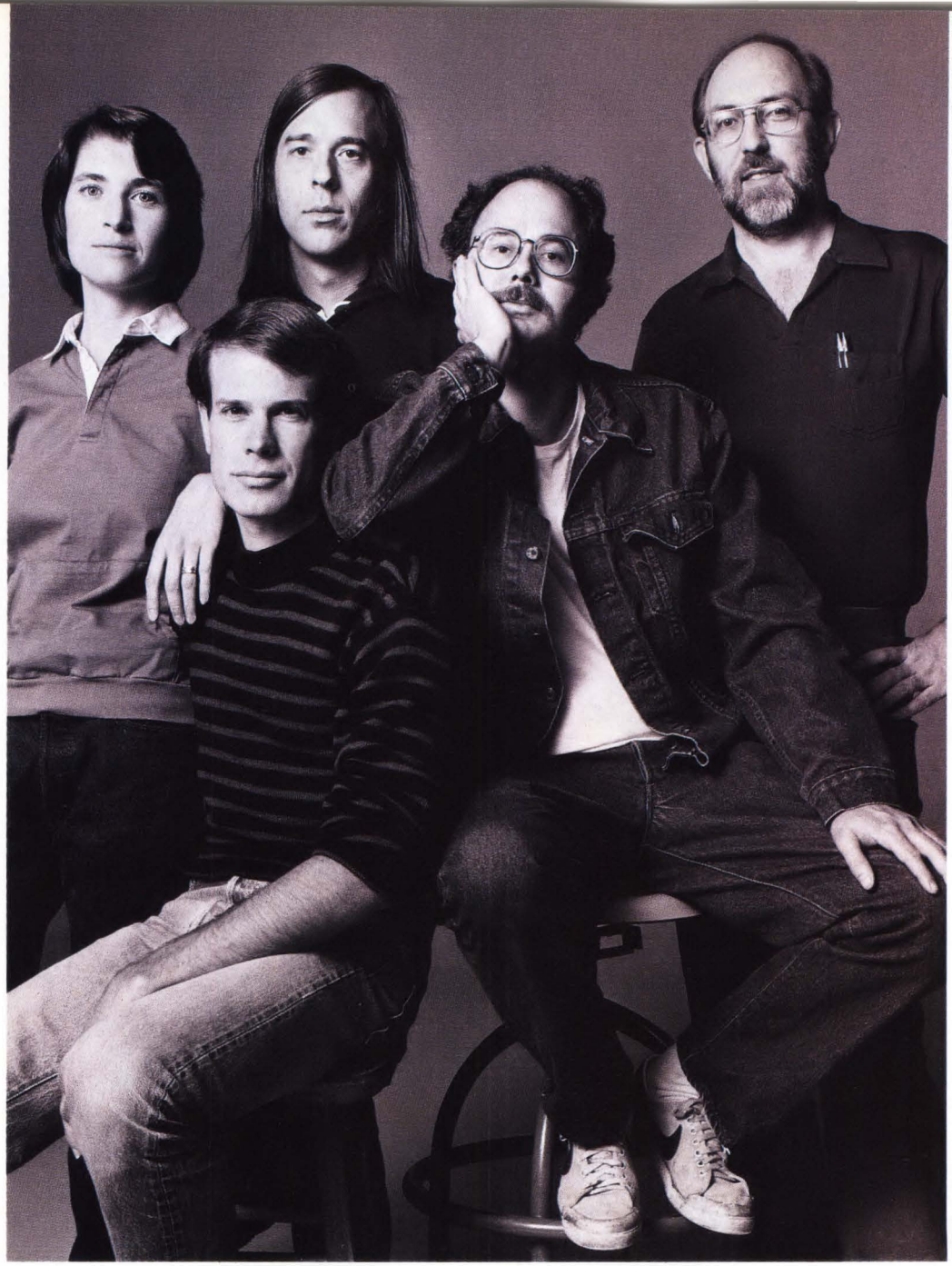
There are several possible routes for the B and D channels through the exchange controller chip. The B channels from the S interface, for example, can be routed directly to the microprocessor on the line card or over the dual PCM highway via the exchange controlller.

Such a line card configuration is very flexible. When a packet on the D channel is received from the terminal equipment, the exchange controller can pass the packet off the line card directly over the dual PCM highway. Alternatively, it can pass the packet, via its on-chip data link controller, to the microprocessor for processing on the line card.

Conversely, when a packet is transmitted over the S interface to the terminal equipment, it can pass directly to the exchange controller from the PCM highway or from the microprocessor on the line card. In the latter case, the packet is passed through the on-chip data link controller before being transmitted.

The microprocessor can communicate with the host computer controlling all the line cards in the PBX by transmitting and receiving data over the PCM highway (via an exchange controller). As an option, a serial communications controller can be interfaced to the microprocessor bus, so that communication can take place between the line card and the host computer over the controller's HDLC link.□

How useful?	Circle
Immediate design application	544
Within the next year	545
Not applicable	546



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CIRCLE 79

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And High Density Plus One goes one step further.

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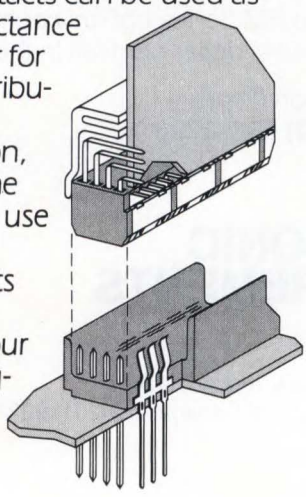

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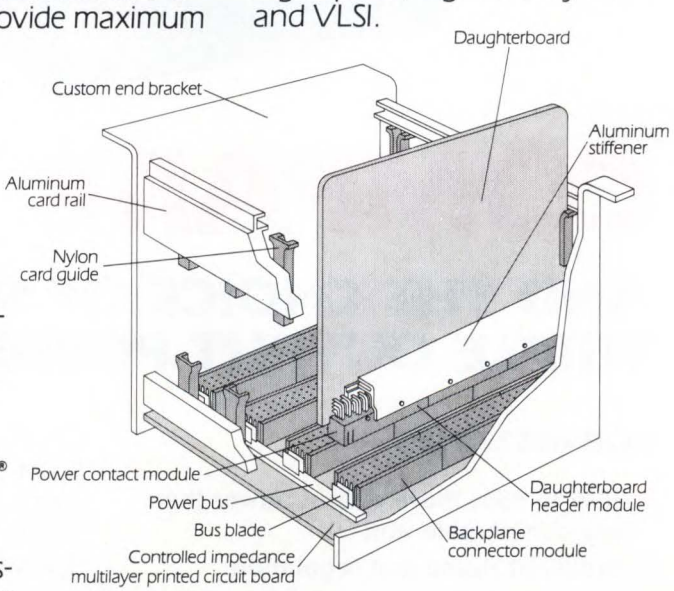

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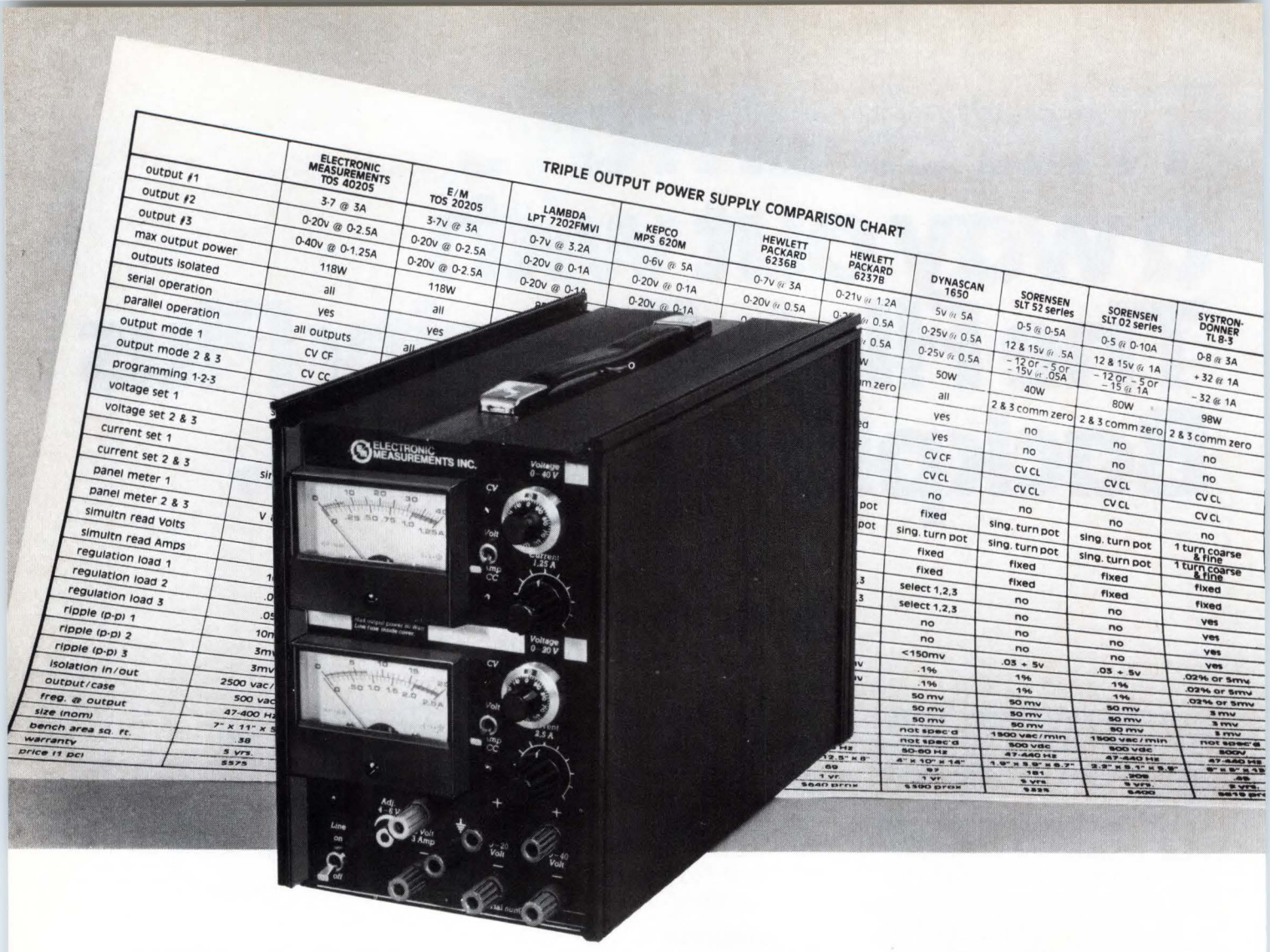

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CIRCLE 81

Built-in Basic interpreter turns controller chip into versatile system core

An extended set of Basic statements and operators transforms a chip into the foundation for a wide range of embedded real-time systems.

Single-chip computers have been popular for some time now, especially in embedded applications. But the phrase "computer on a chip" takes on a whole new meaning with the appearance of a software package that implements a version of Basic in silicon.

The 8052AH-Basic controller is aimed primarily at data acquisition, test instrumentation, and process control. Further, it is right at home in virtually any embedded environment and monitoring system.

Unlike so-called Tiny Basic interpreters, the chip's MCS Basic-52 software package is a full Basic interpreter. In addition, it can manipulate strings and handle logical operators (AND, OR, exclusive-OR, and NOT) and floating-point arithmetic. It is also able to accept and deliver numbers in floating-point, integer, or hexadecimal formats. Counted among its other features are built-in EPROM programming, mnemonic access to all on-chip I/O resources, and a built-in real-time clock with a resolution to within 5 ms. Moreover, its complete function library of routines can be accessed in assembly language (see the table, opposite). And the package supplements Basic's standard instructions with commands designed specifically for embedded systems. The package resides in the 8-kbit ROM of the 8052AH-Basic chip. Apart from the software, it is identical with the 8052AH and so features 256 bytes of RAM and three multiple-mode 16-bit timer-counters.

Although Basic is held in low regard by many computer scientists, one fact cannot be denied: It is by far the most popular microcomputer language. Not only is virtually every personal or home computer capable of running it, but the language has become a de facto standard for many applications, including laboratory and

John Katausky, Intel Corp.

John Katausky is technical marketing manager for Intel Corp.'s microcontroller operation in Chandler, Ariz.

Summary of Basic-52's features

Commands	Statements		Operators	
RUN	BAUD	INPUT	ADD (+)	ASC ( )
LIST	CALL	LET	DIVIDE (/)	CHR ( )
LIST#	CLEAR	ONERR	EXPONENTIATION (**)	CBY ( )
NEW	**CLEARS**	**ONEXT1**	MULTIPLY (*)	DBY ( )
NULL	**CLEAR1**	**ONTIME**	SUBTRACT (−)	XBY ( )
RAM	**CLOCK0**	PRINT	LOGICAL AND (.AND.)	GET
ROM	**CLOCK1**	**PRINT#**	LOGICAL OR (.OR.)	**IE**
XFER	DATA	**PH0.**	LOGICAL X-OR (.XOR.)	**IP**
PROG	READ	**PH0.#**	LOGICAL NOT	**PORT1**
PROG1	RESTORE	**PH1.**	ABS ( )	**PCON**
PROG2	DIM	**PH1.#**	INT ( )	**RCAP2**
FPROG	**DO-WHILE**	**PUSH**	SGN ( )	**T2CON**
FPROG1	**DO-UNTIL**	**POP**	SQR ( )	**TCON**
FPROG2	END	**PWM**	RND	**TMOD**
	FOR-TO-STEP	REM	LOG ( )	**TIME**
	NEXT	**RETI**	EXP ( )	**TIMER0**
	GOSUB	STOP	SIN ( )	**TIMER1**
	RETURN	**STRING**	COS ( )	**TIMER2**
	GOTO	**UI0**	TAN ( )	**TIME**
	ON-GOTO	**UI1**	ATN ( )	**XTAL**
	ON-GOSUB	**UO0**	=,>,>=,	**MTOP**
		UO1	<,<=,<>	LEN
	IF-THEN-ELSE		**PI**	FREE

Boldface statements have been added specifically for embedded systems.

Basic controller

office automation. Its popularity is easily explained by its simplicity and ease of use. A programmer can execute, edit, and debug short programs in minutes, without having to worry about compilation, linking, and locating.

Building up Basic

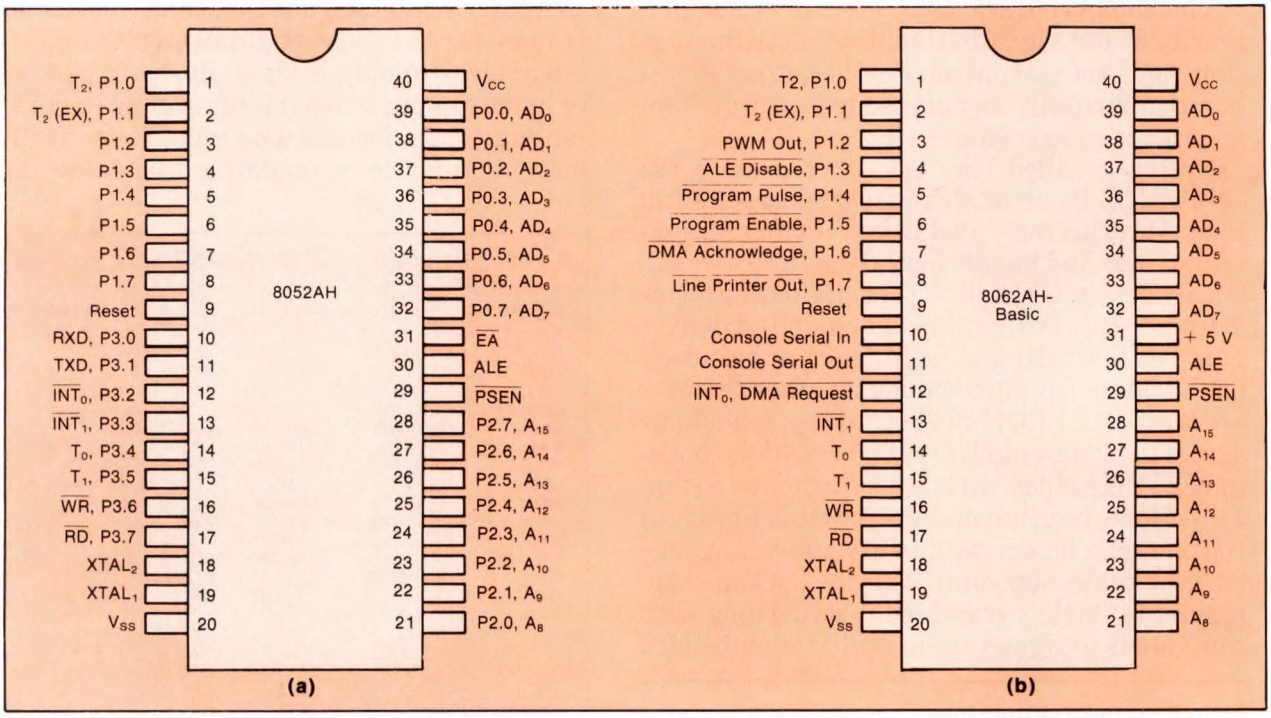
Like any language, Basic has its drawbacks, but the 8052AH-Basic's software package addresses many of them by beefing up its instruction set. These enhancements address three general areas: First, sophisticated programmers dislike the fact that Basic is an unstructured language. Because GO TO statements can be placed anywhere in a program, understanding and debugging it can become quite a chore. For that reason, the package contains the more structured DO-WHILE and DO-UNTIL statements, as well as the standard FOR-NEXT and IF-THEN-ELSE. These extensions furnish better ways to control the flow of a program.

Second, the fact that Basic uses global variables forces subroutines to use the same names for variables as the main program employs. Generally, this is an inconvenience because variables may need to be redefined every time a subroutine is called up. The package's function library, however, includes PUSH and POP statements that allow the user to pass variables to subroutines on a stack, making it easy to redefine variables in a subroutine. Additionally, PUSH and POP can be used to pass parameters to and from user-supplied assembly language routines.

Finally, interpreted Basic is usually a slow language. Although this is a legitimate complaint, many applications can still be adequately served by it. The package's fast token-based interpreter, though, puts an end to the problem, turning in execution speeds that compare quite favorably with those of popular 8- and 16-bit personal computers.

A quick turn around the pins

As mentioned, the software is stored in an 8052AH controller chip, which is itself housed in a standard 40-pin DIP (Fig. 1). Some of the pins' uses are predetermined. Of the four ports on the standard 8052AH, only port 1 still serves as an I/O port on the Basic version. Since the



1. The pin assignments of the 8052AH (a) and the 8052AH-Basic controller (b) differ primarily in that the second does not use lines AD_0 to AD_7 and A_8 to A_{15} as ports 0 and 2, respectively. Further, the Basic version needs +5 V on pin 31 to enable the 8052AH to execute from internal ROM.

8052AH-Basic requires external memory, Pins 32 through 39 and 21 through 28, which formerly served ports 0 and 2 respectively, are now used for their alternative function: addressing and exchanging data with RAM and ROM. Pins 10 through 17, which formed port 3, are putting in their time at their assorted alternative duties—with some slight revisions. The only other changes involve pin 31, $\overline{EA}$, which is now tied to V_{CC}, and port 1, whose pins have acquired a second set of functions.

Port 1 in detail

To start with, pins 1 and 2 of port 1 (P1.0 and P1.1) can also be used to clock and trigger timer-counter 2. Pins 3, 4, and 5 generate all timing and other signals necessary to program just about any EPROM or EEPROM—a simple way to save and retrieve programs without uploading or downloading. Pin 6, together with the INT_0 pin (pin 12), gives the user the option of implementing direct memory access. Finally, pin 7 takes care of direct serial output to a peripheral, such as a printer. All that needs to be done in this case is to invoke the LIST# command or the PRINT# statement.

In addition, the syntax of Basic-52 permits the user to read and write directly from and to port 1. For instance, the statement:

PORT1 = 55H

would place the hexadecimal value 55 on the appropriate pins, while:

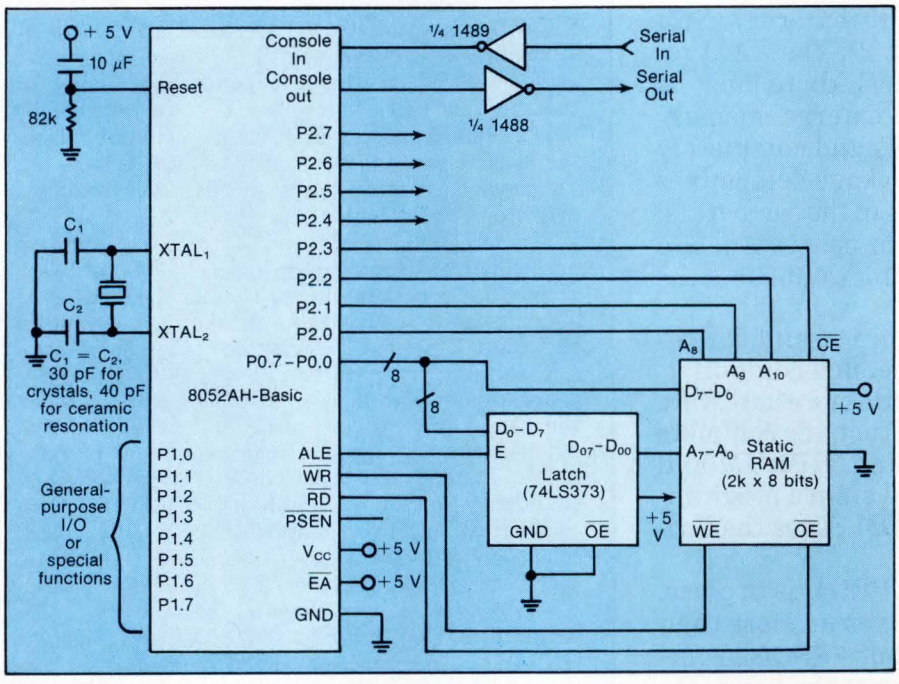
A = PORT1

would assign the value of variable A to the port 1 pins. Furthermore, some of the language's commands and statements manipulate those pins so that they furnish a number of useful and unique features. For example, P1.2 can also serve as an output for the pulse-width modulate (PWM) statement. Executing it generates a pulse train of varying duration, frequency, and duty cycle on the pin.

The statement:

PWM 50,100,1000

creates 1000 cycles of a signal that, assuming a 12-MHz clock, is high for 50 μs and low for 100 μs. The PWM statement also can generate audi-



2. A simple system based on the 8052AH-Basic microprocessor requires just three additional chips plus the serial-port driver. Port 1 could be used, for example, to sense switches, drive indicators, or a power printer.

ble feedback in process control and security systems.

To pin 9 (Reset) falls the job of initializing the system. It also furnishes power on reset when an external 8.2-kΩ resistor is connected from this pin to ground and a 10-μF capacitor is connected to V_{CC}.

Under the software package, all of the pins that formed port 3 are pressed into service in their alternative functions. One of the interrupt pins, $\overline{INT_0}$, now also handles DMA requests (pin 12), and the pins for transmitting and receiving data (pins 11 and 12) now handle serial inputs and outputs to the console. Their activities are integrated into a Basic application program. For example, an interrupt on the $\overline{INT_1}$ pin (pin 13) can be handled by the ONEXT1 statement:

```
10 ONEXT1 1000
```

which forces a GOSUB to line 1000 every time the $\overline{INT_1}$ pin is pulled to a logical 0. In the called subroutine, the user can process the interrupt, then use a RETI statement to exit from the interrupt handler.

To turn the Basic chip into a complete system, the user need supply only external RAM and serial port drivers (Fig. 2). The RAM requirements are few: At least 1 kbyte must be present, and it must start at external memory location 0 and be contiguous and completely decoded. After reset, the package determines how much memory is present in the system and initializes it, then waits for the user to type in a space character. That character establishes the baud rate automatically.

Although this system is quite useful, it does not represent an ideal embedded controller. Fortunately, adding just a little more hardware is all that is needed to construct one complete with automatic self-starting, EPROM and EEPROM programming, and simple program-file management (see "EPROM Saves the Program," opposite).

Once the desired type of EPROM is in place, starting up the system involves no more than entering either the PROG2 or FPROG2 command. Both commands preserve the baud rate information in exactly the same way as PROG1 or FPROG1 does. In addition, though, either causes the first program stored in PROM to ex-

EPROM saves the program

EPROM and EEPROM programming is certainly one of the most powerful features of the MCS Basic-52 software package. And it is simple to use; only three of the 8052AH-Basic microprocessor's control pins are needed to call it into play. In brief, after the user enters a program, it is stored in RAM, starting at location 512. When the user types PROG PROG or FPROG, the program that is stored in RAM is programmed into an EPROM or EEPROM whose address is 8000_{16}.

To start the process, the CPU first writes a logical 0 to the Program Enable pin, P1.5, thus supplying the higher voltage required to program the EPROM. Next, the processor reads the appropriate RAM location, starting at 512, and saves the byte of information.

Then, the CPU sends out the appropriate low-order PROM address to pins AD_0 to AD_7 and sets the ALE Disable pin to 0. That latches the low-order PROM address permanently into the system address latch—74LS373 (see the figure). Only one AND gate is required to do this. The processor then writes the high-order PROM address to pins A_8 through A_{15} and the data to pins AD_0 to AD_7. Finally, a 0 is written to the Program Pulse pin. Depending on the PROM used, that pin is held low for either 1 or 50 ms. After it returns to a logical 1, the CPU verifies the contents of the programmed PROM and then writes a 1 to ALE Disable.

The process continues until the entire Basic program is saved in PROM. When programming is complete, the CPU writes a 1 to the Progam Enable pin, leaves the programming routine, and returns to the Basic command mode. To prevent accidental programming during power-up, OR gates should be used (top left in figure).

The foregoing description of the programming naturally leads to two questions.

The first concerns the duration of the 0 state. A 50-ms pulse is required to program most standard EPROMs. The 1-ms pulse, on the other hand, permits the software package to program Intel's latest generation of high-density EPROMs, working with the company's programming algorithm, dubbed INTELigent. To apply it, the user simply types FPROG instead of PROG. The algorithm requires that the V_{CC} on the EPROM be increased to 6 V. One economical way to accomplish this is with a DIP relay. The software package also allows the user to specify programming pulses of any length.

The other question centers on the accuracy of the programming pulse versus that of the system clock frequency. To eliminate any dependency on the

system clock, the package actually calculates all critical timing parameters from a user-supplied variable, XTAL. After a reset, the package assumes a system clock frequency of 11.059200 MHz unless told otherwise. If the user enters the statement:

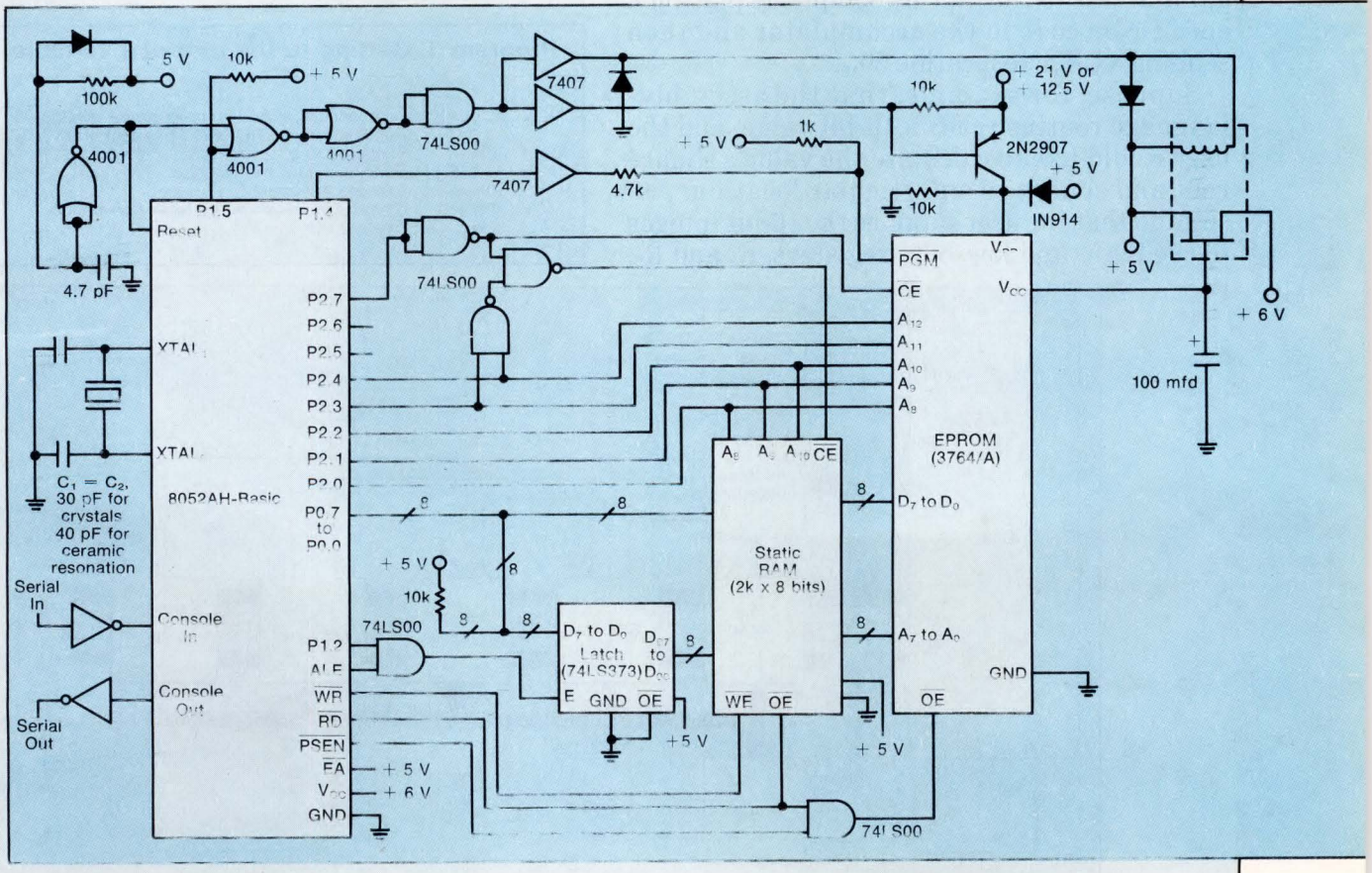
XTAL = 12000000

a 12-MHz system clock is assumed and the proper PROM programming time calculated. The real-time clock pulses and the baud rate for the line printer output port are also determined. This ability gives the designer the freedom to choose the desired system clock frequency without having to worry about the internal timing of the Basic software.

Another useful aspect of the software's PROM programming capabilities is that it stores up to 255 programs in an EPROM. PROM size, of course, limits the possible number of programs. Every time PROG (or FPROG) is typed, the software responds with the file number that has been assigned to that program. To call up a given program, the user simply types ROM X, and the package finds the appropriate one. Typing RUN starts program execution.

Suppose the user discovers an error in a program that is stored in EPROM—normally bad news because such programs cannot be edited. However, the package allows a program to be transferred from EPROM to RAM by typing XFER. Once XFER is entered, the program may be edited like any other. Typing PROG again saves the edited program.

Additionally, after reset, the software package waits for a space character, from which the baud rate is derived, to be entered on the serial port. As an option, the package can be made, on receiving the command PROG1 or FPROG1, to save the serial-port baud rate information in PROM. The next time the processor is reset, the package can sign on directly without the need to enter a space character.



ecute directly after reset, bypassing a RUN command. In fact, even the console is no longer needed in some embedded systems. Programs can be written and debugged with the aid of a terminal, and when the programmer is satisfied with the results, the hardware can be embedded in the design and the terminal disconnected.

On call

Aside from the features already noted, the package contains a host of others that are very attractive for embedded systems. The CALL statement, for instance, accesses assembly-language routines directly from the package, a handy way in which to meet speed requirements. Better still, assembly-language programs can take advantage of a complete library of routines that reside in the package. The user gains access to this library simply by placing a specific op code in the accumulator and then sending a CALL to location 30_{16}.

Suppose, for example, that the assembly-language routine reads a 16-bit value, and the user would like to calculate the value's square root and send it to a particular location. Assuming that the user supplies the 16-bit integer to the high- and low-byte registers, R_2 and R_0, respectively, the calculation can be made simply (Program 1). All told, over 60 routines can be invoked by assembly-language programs.

The software package also controls all of the system's I/O memory resources. To make things simple, all of these operations are symmetrical. For example, the operator DBY in the statement:

A = DBY (0FEH)

assigns the value located at $0FE_{16}$ in the chip's internal memory to variable A. The statement:

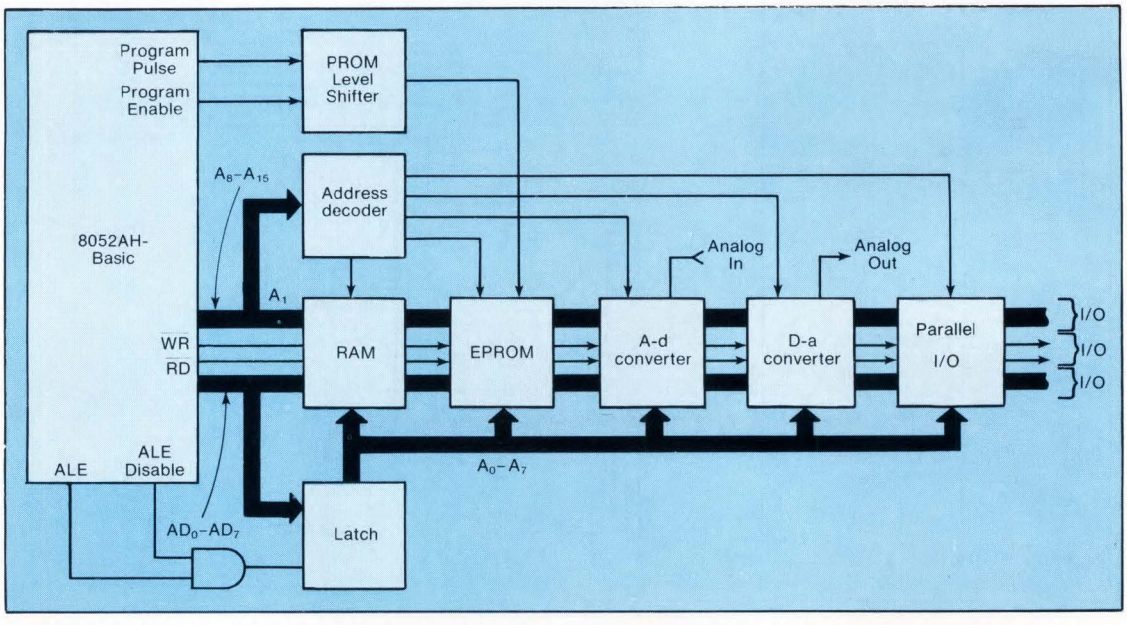
DBY (0FEH) = 22H

places 22_{16} in internal memory location $0FE_{16}$. The same symmetry holds for the interrupt registers, IE and IP, as well as the timers and the timer configuration registers.

Other special instructions are particularly

Program 1. Getting to the root of a variable

```
MOV  A, #9AH  ; Load accumulator with op code for placing
              ; Register pair R2:RO onto argument stack
CALL 30H      ; Execute the operation
MOV  A, #1FH  ; Specify square-root routine
CALL 30H      ; Execute the operation
MOV  A, #1H   ; Specify truncation and integer conversion
CALL 30H      ; Execute the operation
```



3. With the help of an address decoder, the I/O on a system built around the Basic chip can be expanded at will. One such setup converts analog into digital and digital into analog signals, and supplies a parallel I/O port for a console.

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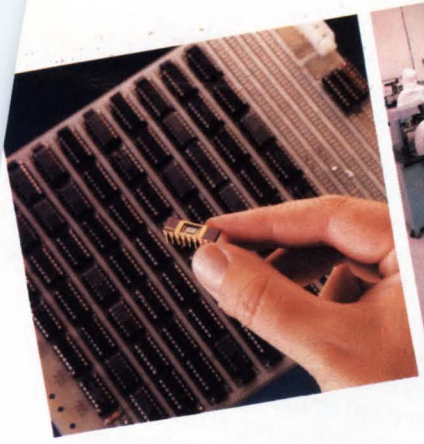

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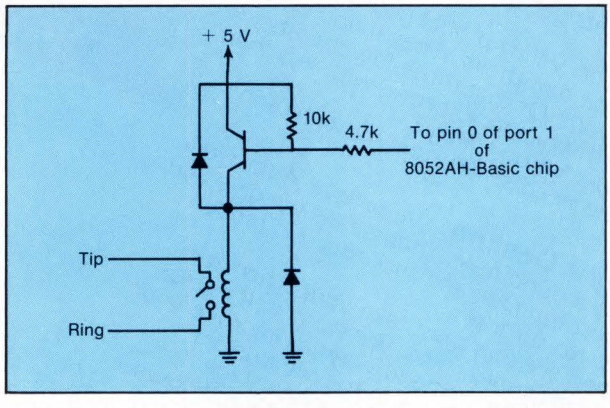
CIRCLE 116

Basic controller

helpful for the designer. Thus BAUD sets the baud rate for the line printer port. If the designer wants to transmit at 1200 bauds, he or she simply enters BAUD 1200. CLEARS is used to reset all of the package's stacks, and CLEARLI resets all interrupts, except the real-time clock. CLOCK1 enables the real-time clock, just as CLOCK0 disables it. The value of the clock can be read or assigned by using the TIME operator. ONTIME generates an interrupt when the TIME operator reaches or exceeds a specific value. ONTIME works in much the same way as the aforementioned ONEXT1 statement. Finally, the statements PH0 and PH1, when used together, ensure that outputs are given in hexadecimal notation. PH0 suppresses leading zeros, and PH1 always prints out four hexadecimal digits.



4. To function as an autopulse dialer, the Basic chip needs only a single-pole, single-throw, normally closed relay and an npn transistor to drive it.

Program 2. Placing a call with the software package

```
10   REM MCS BASIC-52 AUTO TELEPHONE DIALER
20   STRING 200,20 : REM ALLOCATE MEMORY FOR STRINGS
30   REM NAMES ARE STORED AS FOLLOWS -
40   REM      NO. OF DIGITS IN NAME - NAME -
               PHONE NUMBER
50   REM      THE "E" REPRESENTS THE END OF FILE
60   $(1)="3JOE1234567E"
40   $(2)="4BILL2345678E"
50   $(3)="3ANN3456789E"
60   INPUT "WHO WOULD YOU LIKE TO DIAL - ",$(4)
70   FOR I=1 TO 3 : REM LOOP TO FIND MATCH
80   REM READ THE NUMBER OF DIGITS AND STRIP
       OF ASCII BIAS
90   FOR J=1 TO (ASC($(I),1) .AND. OFH)
100  IF ASC($(4),J) = ASC($(I),J+1) THEN NEXT J ELSE NEXT I
110  CLEARS  : REM CLEAR THE STACK TO ELIMINATE
       THE I INDEX
120  REM I COUNTS THE NAME, J THE PHONE NUMBER
130  CLOCK1 : REM TURN ON THE REAL TIME CLOCK
140  DO : REM NOW LOOP TO DIAL
150  C = (ASC($(I),J) .AND. OFH)
160  IF C = O THEN C = 10
170  FOR Y = 1 TO C : T = TIME
180  PORT1 = PORT1 .AND. OFEH : REM OPEN THE LINE
190  IF TIME < T + .04 THEN 190: REM LOOP FOR 40 MS
200  PORT1 = PORT1 .OR. 1 : REM CLOSE THE LINE
210  IF TIME < T + .1 THEN  210 : REM LOOP FOR 60 MS
220  NEXT Y
230  J=J+1 : WHILE ASC($(I),J)<>ASC(E)
240  END
```

Addressing I/O

Building a functioning system around the Basic chip is a snap. The designer can link to virtually any standard peripheral chip simply by assigning some location to the peripheral in the 64 kbytes of external address available to the 8-bit device.

In fact, the software actually reserves the chip's upper 8 kbytes of memory (from 56 to 64 kbytes) for I/O. Accessing external peripherals is accomplished by using the XBY, or address, operator. For example:

```
A=XBY (0FFF0H)
```

reads a peripheral or external memory location that has been decoded for address $0FFF0_{16}$ and assigns its value to the variable A. Similarly:

```
XBY (0FFF0H) =55H
```

writes 55_{16} to a peripheral or memory location that has been decoded for address $0FFF0_{16}$. A system consisting of an analog-to-digital and a digital-to-analog converter plus an 8255 parallel port, all connected to the software package, is typical of process control, environmental monitoring, or energy management applications (Fig. 3).

An autopulse telephone dialer also demonstrates the versatility of the software package (Fig. 4). This application takes advantage of the logical operators as well as the real-time clock and string operations (Program 2). Such dialing could play an important role in many process control and remote environmental-monitoring systems where information must be periodically sent to a master computer over a phone link. Variations on the general software scheme could be devised to address a wide variety of automatic dialing and automatic answering settings. □

How useful?	Circle
Immediate design application	547
Within the next year	548
Not applicable	549

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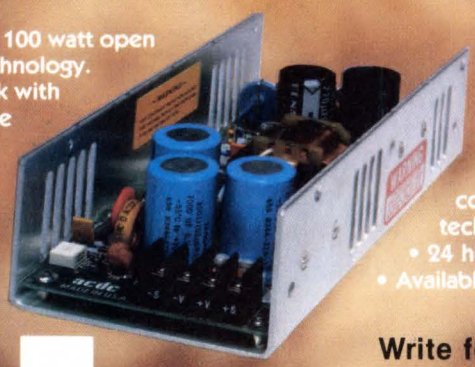

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Chip duo allows transfer of controller electronics to smallest disk drives

With the disk drive electronics now packed in tiny packages, placing controller boards in the host computer is a has-been approach.

Most personal computers have to control at least one floppy-disk drive, and usually the controller electronics for the drive are on a plug-in card. Moving the controller components into the drive would free an expansion slot in the computer, but ever-smaller disk drives severely restrict the area for the drive circuitry itself, let alone added control electronics. Instead of the standard 5¼-in. height for drives, designers now face 3½-in. versions, like the Sony floppy.

Two chips give the designer considerable leverage in overcoming the impossible. With the pair—the SSI 570 and the SSI 580—a designer can squeeze all the electronics for a disk drive into less than 2 in.[2] The space thus made available can be used to move a controller into the disk drive.

For example, an SA400 type of disk drive can interface with a host computer in a much simpler manner with the two chips, which incorporate most of the required circuitry (Fig. 1). Both satisfy the interface characteristics of all lines between the host and the drive, supply all interconnections with the read/write heads, and provide an interface with an on-board microprocessor.

When used with an 8048 microprocessor and a spindle-motor speed controller, the chip set makes up virtually all the circuitry required in a floppy-disk drive. The SSI 570 replaces the traditional MC3470 and MC3471, several 7414 input gates, and a handful of diodes. The SSI 580 replaces several SSI and MSI logic circuits, programmable logic arrays, integrated fuse logic devices, or gate arrays.

The SSI 570, known as the data path chip, provides the complete read/write and erase functions in a 28-pin package. It includes the write data flip-flop, as well as a write current source that can be set externally.

Erasing can follow either "straddle" or "tunnel" methods, which employ different erase heads. With the straddle method, the erase gap straddles the write gap; with the tunnel method, the erase gap follows the write gap. For tunnel erase heads, the SSI 570 erase current can be delayed at turn-on and turn-off to coincide with the position of the written information. The read data path—from the head to the read output—is characterized by low noise (5 μV rms), high gain (1000 V/V), and minimal peak shift (0.3%).

The SSI 580, which also comes in a 28-pin

Dan Brown and **Al Morton,** Silicon Systems Inc.

Dan Brown gained extensive experience in IC design before becoming computer products marketing manager at Silicon Systems in Tustin, Calif. He obtained his BSEE from the University of California in Irvine.

Al Morton is applications engineering manager at the same company and was previously a field applications engineer at Harris Semiconductor and Texas Instruments. His BSEE and MSEE are from California State University in Fullerton.

Disk drive control chips

package, is a special-purpose I/O port expander for an 8048 or similar microprocessor. It processes system data and controls the width and delay of the index sensor input. The inputs of all host interface lines have hysteresis, and the outputs meet the high-current (48-mA) and open-collector specifications required by the SA400 interface.

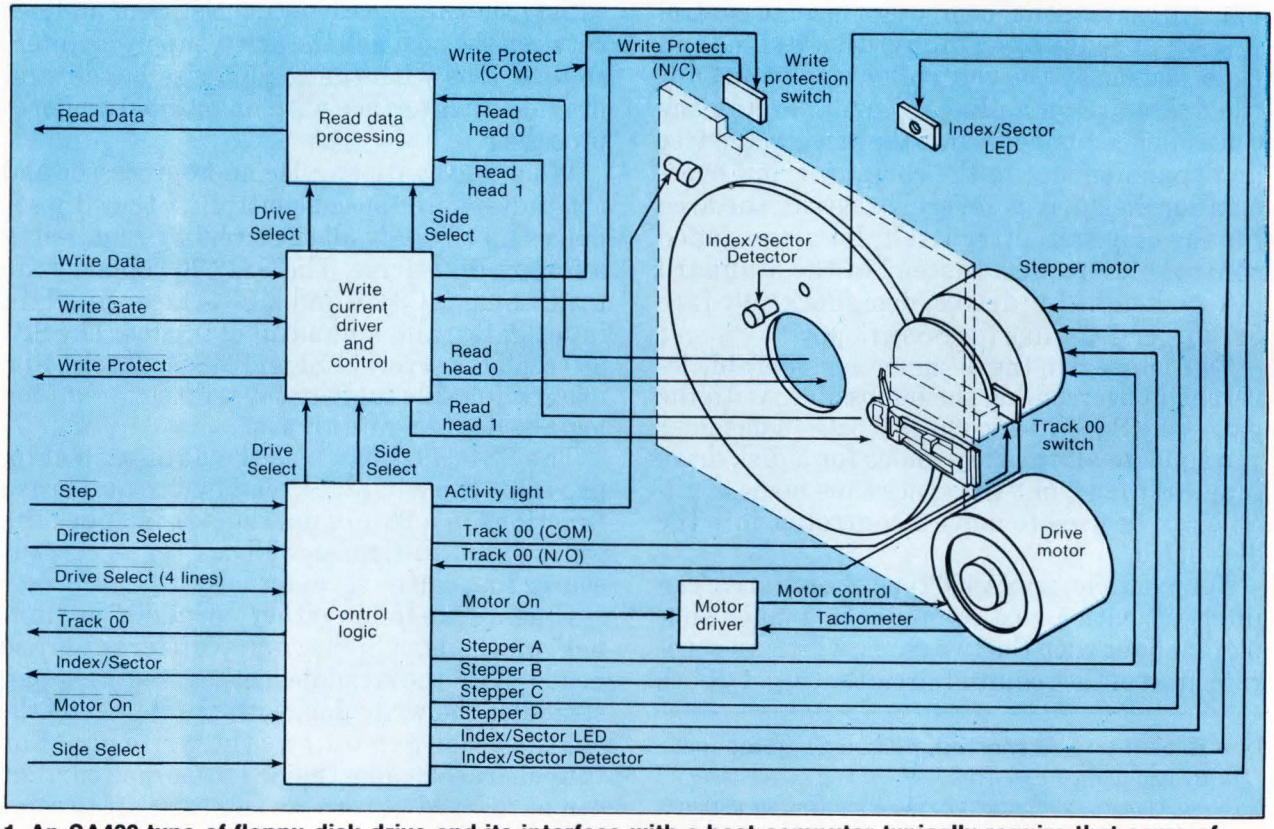
Easy layout

The designer still must use a few passive components to build a low-pass filter and to set the timing. However, there are no critical analog interconnections or layout problems, since that wiring is internal to the SSI 570. Since each chip occupies less than half an inch on a side in surface-mounted packages, the inherent space savings are obvious.

The controller board supplies a function needed by many magnetic media recording schemes. It turns data being sent to the drive into a serial stream, using modified frequency modulation (MFM) to encode it (see "Matching the Message to the Medium," opposite).

The read signal processing circuits on the data path chip consist of two differential preamplifiers, a summing amplifier, a postamplifier, an active differentiator, a zero-crossing detector, a time-domain filter, and an output one-shot (Fig. 2). When reading (R/$\overline{W}$ high), these circuits amplify and detect the read signals to produce uniform digital output pulses.

Each preamplifier input—for example, $+HD_1$ and $-HD_1$—is connected, in parallel with a write current driver, to each read/write



1. An SA400 type of floppy-disk drive and its interface with a host computer typically require that some of the interface electronics be placed on a plug-in controller board within the computer.

head. The inputs are protected from the large voltage transitions that occur during writing. The output of the selected preamplifier, defined by the state of the Head Select pin ($HS_0/\overline{HS_1}$), is fed to the summing amplifier.

The summing amplifier's outputs ($+A_0$, $-A_0$) are ac-coupled to the postamplifier through an external filter network. The input amplitude to the postamplifier (at pins +In, −In) should be maximized to reduce peak shift, meaning that the low-pass filter should have minimal attenuation in its passband. (Bessel or Thompson filters are typically used for their linear phase characteristics.) The passband corner is usually set above the third harmonic of the maximum frequency.

The postamplifier, which requires no external bias connections, can adjust the amplitude of a signal before sending it on to the differentiator. Maximum postamplifier gain is achieved with infinite impedance across gain pins G_1 and G_2. (An additional frequency- or phase-compensation network may also be employed here.)

The response characteristics of the differentiator are determined by an external capacitor (or more complex series network) between D_1 and D_2. The capacitor chosen should allow for a current of 2 mA peak to peak at maximum amplitude and frequency. If the internal 50-Ω resistance is insufficient to provide roll-off at 10 times minimum frequency, an external series resistor can be added. To attenuate higher frequencies, a series RLC network can be used, but the capacitor should still be selected as just described.

The peaks of signals entering the differentiator from the postamplifier become the zero crossings of the differentiator's output signal. A detector provides a unipolar output for each positive or negative zero crossing of the differentiator output.

The time-domain filter

To enhance peak detection, spurious inflection points between true signal peaks are suppressed with a time-domain filter. The filter rejects detected zero crossings if they are not sufficiently separated in time. The time period is set by an external RC network at the TD pin.

Uniform data output pulses, presented at the

Matching the message to the medium

Since the data that can be stored in a disk is limited by the number of flux transitions that can be produced on the magnetic surface, a self-clocking encoding scheme is often used to pack the most raw data into the flux transitions. The most popular scheme for floppies—though not necessarily the most efficient one—is modified frequency modulation (MFM) as follows:

If the serial stream of binary data is visualized as a sequence of bit cells, the rules for MFM recording can be summarized as follows:

- There is a flux transition for each 1 bit at the bit cell time.
- There is a flux transition between each pair of 0 bits.
- There is no flux transition between the bits of a 10 or a 01 combination.

In current floppy-disk drives, a controller tackles the encoding before the data is sent to the drive. What the drive receives is a serial stream of digital MFM-encoded data, which is then used to clock a toggle flip-flop. Each toggle on the output of the flip-flop causes the current to flow in a different leg of the read/write head, creating a change in the polarity of the magnetic field and therefore causing a flux transition. In the read mode, that recorded flux transition passes near the read/write head, inducing a low-level signal. Each flux transition corresponds to a pulse in the original data stream.

The challenge lies in faithfully replicating the original data stream. The key parameter is the spacing between the peaks of the detected signal. The signal is first amplified, then filtered to remove the unwanted frequency components. The low-frequency or dc components cause a signal offset, which becomes an asymmetry (or peak shift) in the output pulse position. The high-frequency components (noise) can cause jitter in the output pulse timing, which breaks up into small random variations in the zero-crossing location.

Differentiation changes the signal peaks into zero crossings. A comparator can detect the zero crossings, from which a bidirectional one-shot produces the data output pulses. Since the input to the differentiator is anything but a pure sine wave, the comparator may see "zero crossings" that do not indicate true flux reversals, but rather that are a result of noise or distortion in the signal processing path. However, valid zero crossings generate pulses from the comparator that are longer than a known minimum. If all pulses of less than that duration are ignored, some protection is afforded against false zero crossings. The SSI 570 data path chip employs this time-domain filtering scheme.

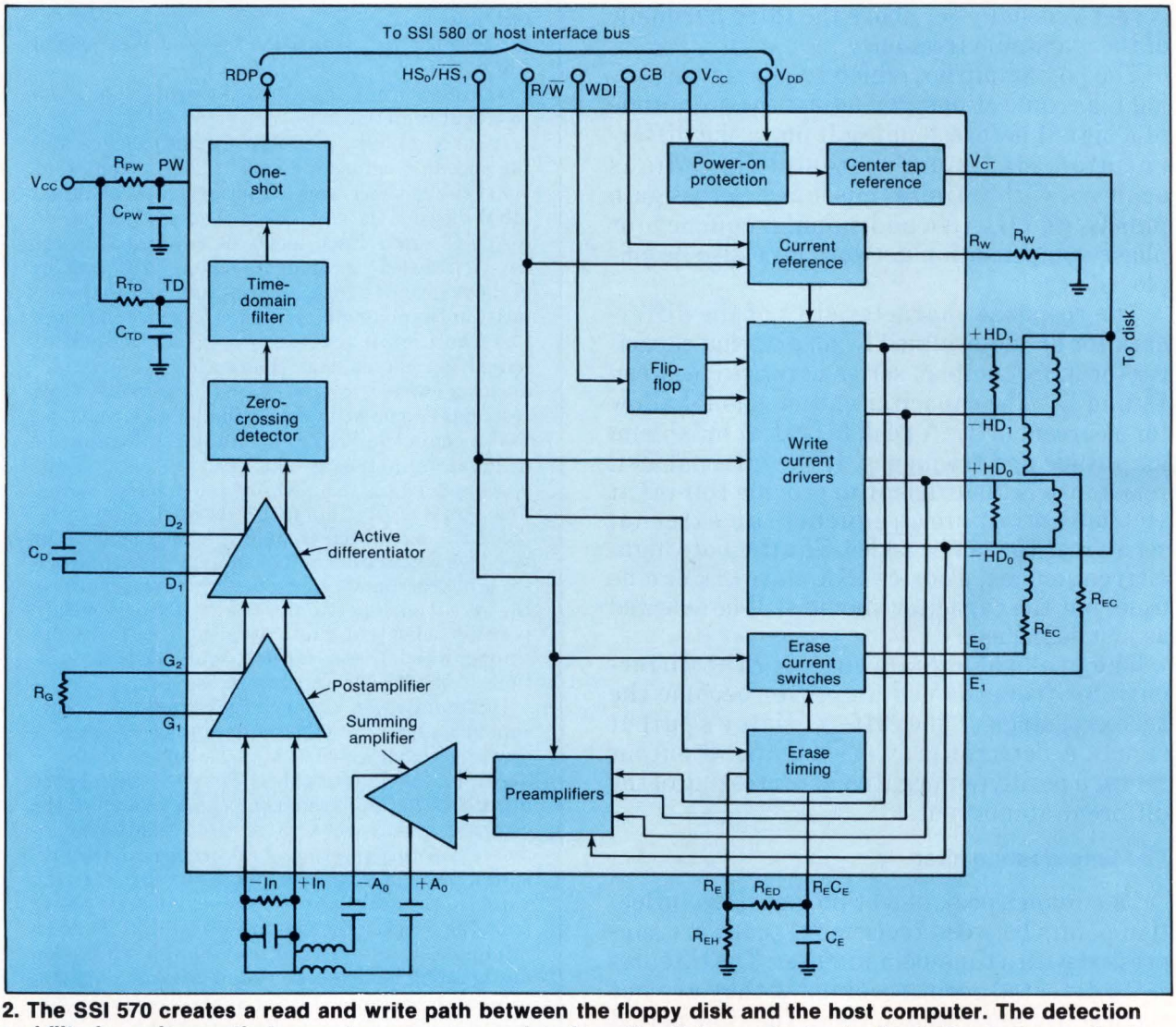
Disk drive control chips

Read Data Pulse pin (RDP), are provided by the output one-shot, which is triggered by the output of the time-domain filter. The duration of the output data pulse is determined by an external RC network at the PW pin. The output one-shot is inhibited when the device is in the write mode.

The SSI 570's write circuits (Fig. 2 again) consist of two differential write current drivers operated by a flip-flop divider stage, a center tap voltage reference, two erase current switches, and control circuits for head selection and erase timing.

In the write mode (R/$\overline{W}$ low), these circuits send controlled write and erase currents to either of two read/write heads. The value of the write current is set by an external resistor connected between the R_W pin and ground. Write current can be boosted 30% to compensate for the varying radial speed between the inner and outer track on the disk. This calls for a high input to the Current Boost pin (CB). The erase current is set by the external R_{EC} resistors in series with the erase coils and the erase current switches at pins E_0 and E_1.

The center tap voltage reference, V_{CT}, is a



2. The SSI 570 creates a read and write path between the floppy disk and the host computer. The detection and filtering schemes that accept or recover raw data from the disk are electronically similar to the methods used by standard multichip designs.

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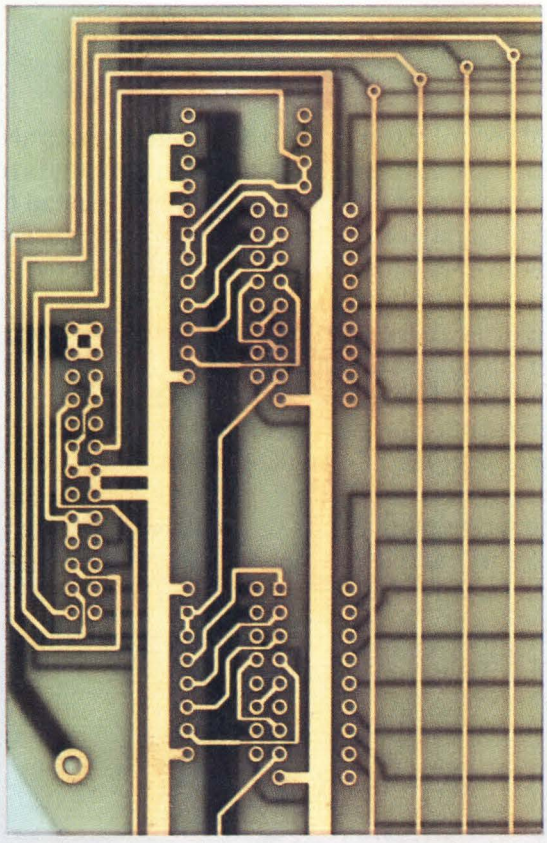

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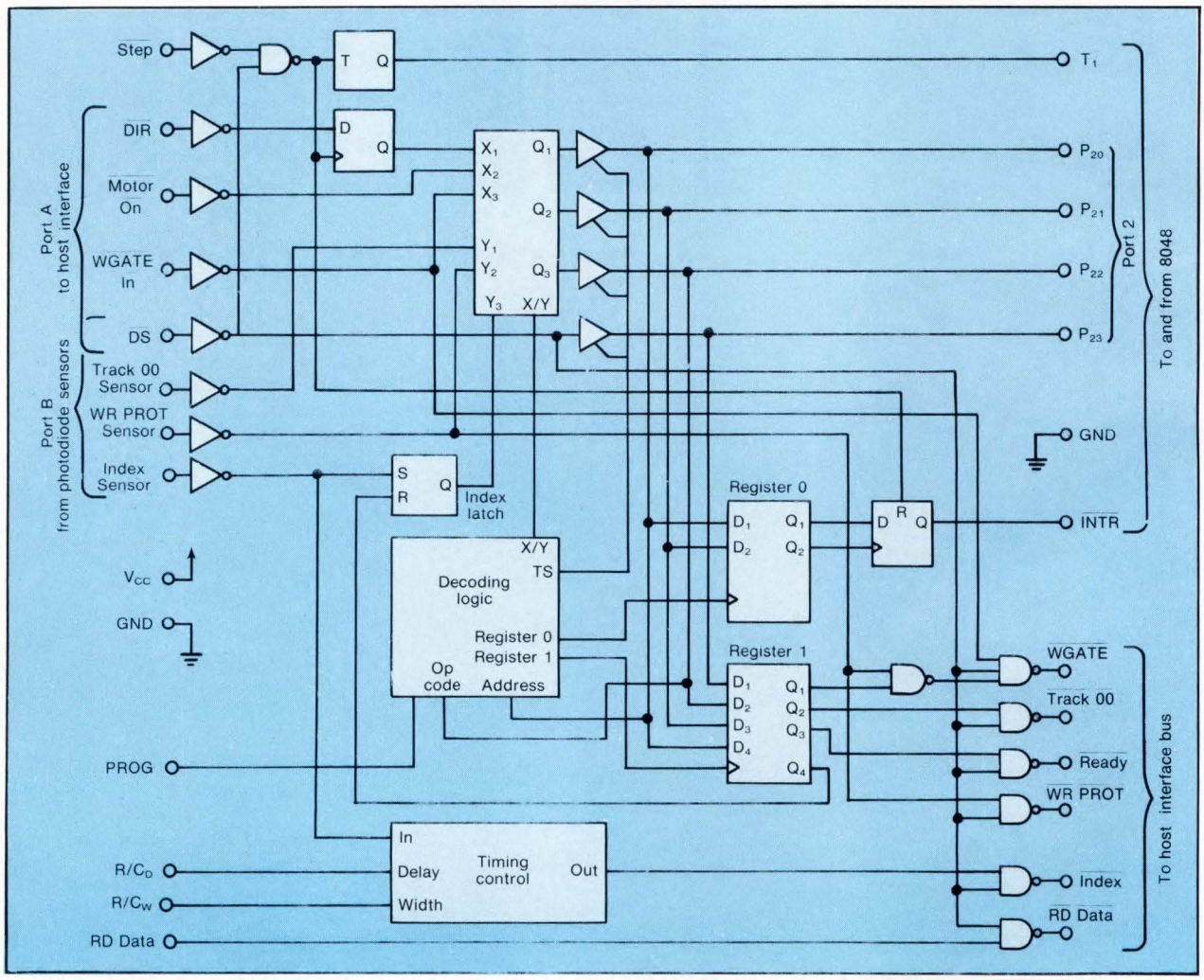
Disk drive control chips

switched source that supplies both the erase head and the write head current. In the write mode, the reference voltage is near the V_{DD} supply, minimizing power dissipation. In the read mode, the voltage is lowered to a value suitable for biasing the preamplifier inputs. To prevent undesired writing or erasure during power-up (or from a power-supply fault), the voltage reference is delayed until the supply voltages are within their operating ranges.

The write currents are controlled by two switching differential current drivers. When the data path chip is in the write mode, those drivers change output states at each negative transition of the Write Data In pin (WDI). The output impedance of the drivers is very high. External resistors connected across each read/write head damp the write current.

The erase current is activated when the write mode is selected, but its application may be delayed. The turn-on delay is created when the erase capacitor, C_E, is charged through the erase delay resistor, R_{ED}. Similarly, the erase current, after leaving the write mode, is held for a time by the discharge of C_E through the series R_{ED} and R_{EH}, which is the erase hold resistor. (For straddle-erase applications, C_E can be omitted, causing the erase current to be applied concurrently with the write current.)

The SSI 580 I/O port expander has one 4-bit



3. The SSI 580 is a special-purpose I/O port expander that complements the data path chip when both are used with an 8048 microprocessor. Ports A and B are 4-bit input ports; port 2 is a 4-bit bidirectional port.

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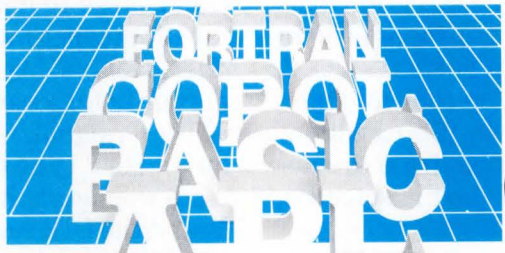

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Disk drive control chips

bidirectional port, port 2, and two 4-bit input ports, port A and port B (Fig. 3). Port 2 consists of pins P_{20} through P_{23}. The pins for port A consist of Disk Select ($\overline{DS}$), Write Gate In (WGATE IN), Motor On (Motor On), and Direction Select ($\overline{DIR}$). Port B consists of DS and three sensor inputs, one for the index, another for write protection, and the last for track 00.

An 8048 microprocessor communicates with the I/O port expander over bidirectional port 2, with timing provided on the Programming pin (PROG) from the microprocessor. Information is transferred in two nibbles: the first contains the op code and port address and the second, the four-bit I/O data. A high-to-low transition on PROG clocks in the op code or address, and a low-to-high transition reads or writes data as directed by the op code.

Reading and writing

In the read mode, the microprocessor can read each of the two 4-bit input ports via port 2. The processor loads the read op code and port address on pins P_{20} and P_{22} in the falling edge of PROG. When the op code and address are decoded, the appropriate input port is selected, and port 2 is configured as an output port (see the table). This operation is terminated by the rising edge of PROG, which returns port 2 to the input mode.

SSI 580 read and write modes

Mode	Op code (P_{22})	Address (P_{20})	Input (plus on-chip manipulation)	Output
Read	0	0	$\overline{DS}$	P_{23}
			Index sensor latch	P_{22}
			Write protection sensor	P_{21}
			Track 00 sensor	P_{20}
	0	1	$\overline{DS}$	P_{23}
			WGATEIN	P_{22}
			$\overline{Motor\ On}$	P_{21}
			$\overline{DIR}$ register	P_{20}
Write	1	0	$(P_{23} \cdot \overline{WR\ PROT\ sensor}) + (\overline{DS} \cdot WGATEIN$	$\overline{WGATE}$
			$(P_{22} \cdot \overline{DS})$	$\overline{TRACK\ 00}$
			$(P_{21} \cdot \overline{DS})$	$\overline{Ready\ latch\ reset}$
			P_{20}	Index
	1	1	(see text)	$\overline{INTR}$

In the write mode, the microprocessor passes system parameters to the I/O port expander for logic manipulation and transmission to the host system. The write op code and address are passed on the high-to-low transition of PROG. On the low-to-high transition, data on port 2 is loaded into the circuit.

The Interrupt signal ($\overline{INTR}$) is the output of a D flip-flop, which is reset every time the Step command is issued. The command forces $\overline{INTR}$ low, thereby interrupting the 8048 and causing it to execute an interrupt service routine. Typically that routine obtains information on the direction the heads should move and on the status of the track 00 sensor, and the information is used to generate phase-control signals for the stepper motor. Note that indeterminate operation will result from holding the Index Sensor Latch reset.

The T_1 signal, which drives the counter input on an 8048 type of microprocessor, changes state whenever the host sends a step command. T_1 and the $\overline{DIR}$ register input from port A monitor head position, so that a Current Boost command can be given to the data path chip when a specific track is reached.

The Index pulse width and delay are programmed by resistors and capacitors connected to the R/C_W and R/C_D pins, respectively. The $\overline{WGATE}$ output controls the change between read and write modes of the data path chip.

Since the chip set is intended to squeeze the floppy disk's electronics into as small an area as possible, the ideal situation would be to free enough space to put a disk controller on the same board. A suggested floppy-disk drive reduces circuit space (Fig. 4) by using a multilayer board and surface-mounted active and passive components (the 8048 is available as a surface-mounted device). The circuit meets all the controller signal requirements of the SA400 type of interface (Fig. 1 again). The chip set needs only half a square inch, and the rest of the circuitry, approximately 1 in.^{2} Thus the disk drive electronics fit in less than 2 in.^{2}

The reduction in IC count is obvious. Surrounding the data path chip are the passive

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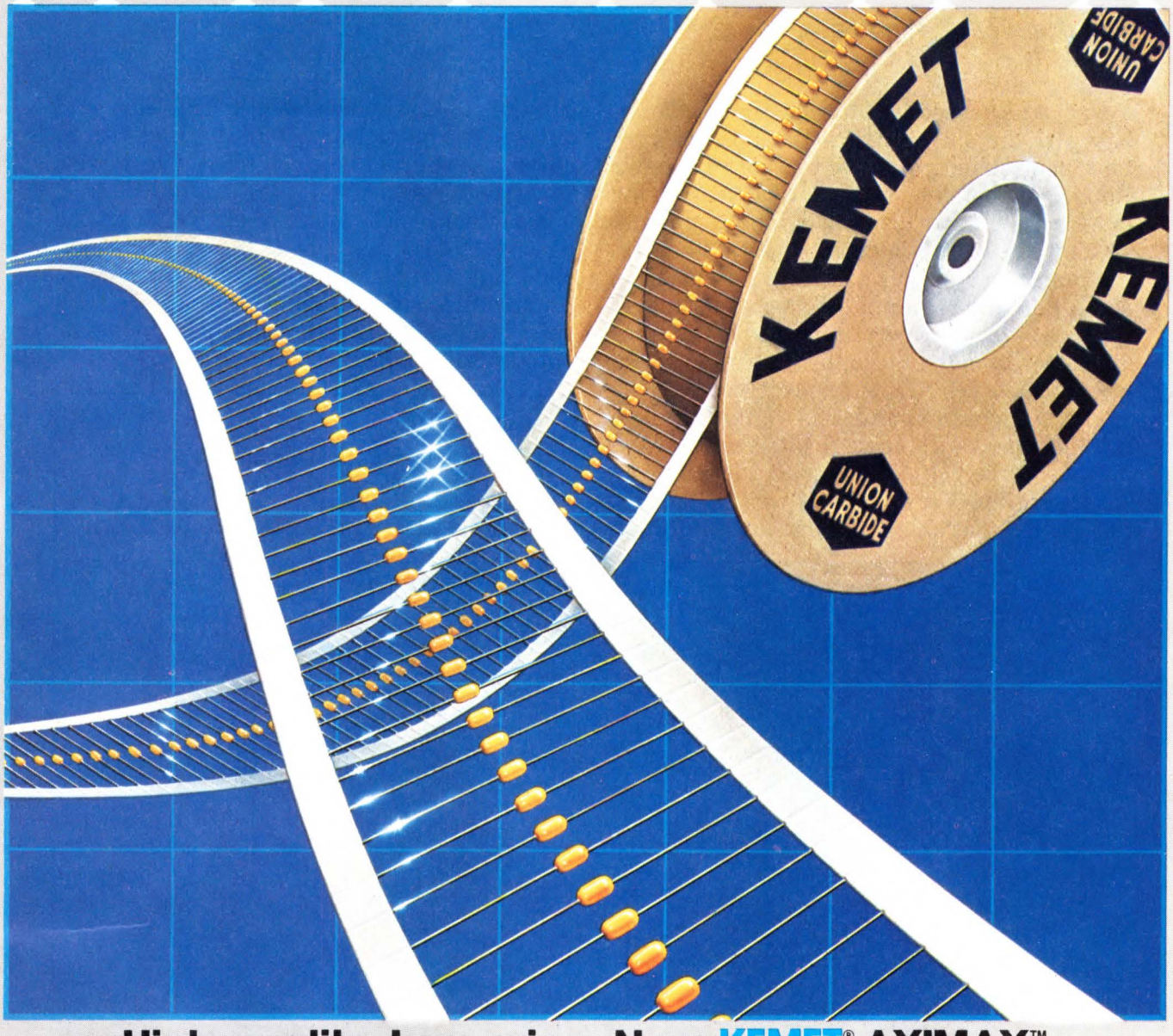

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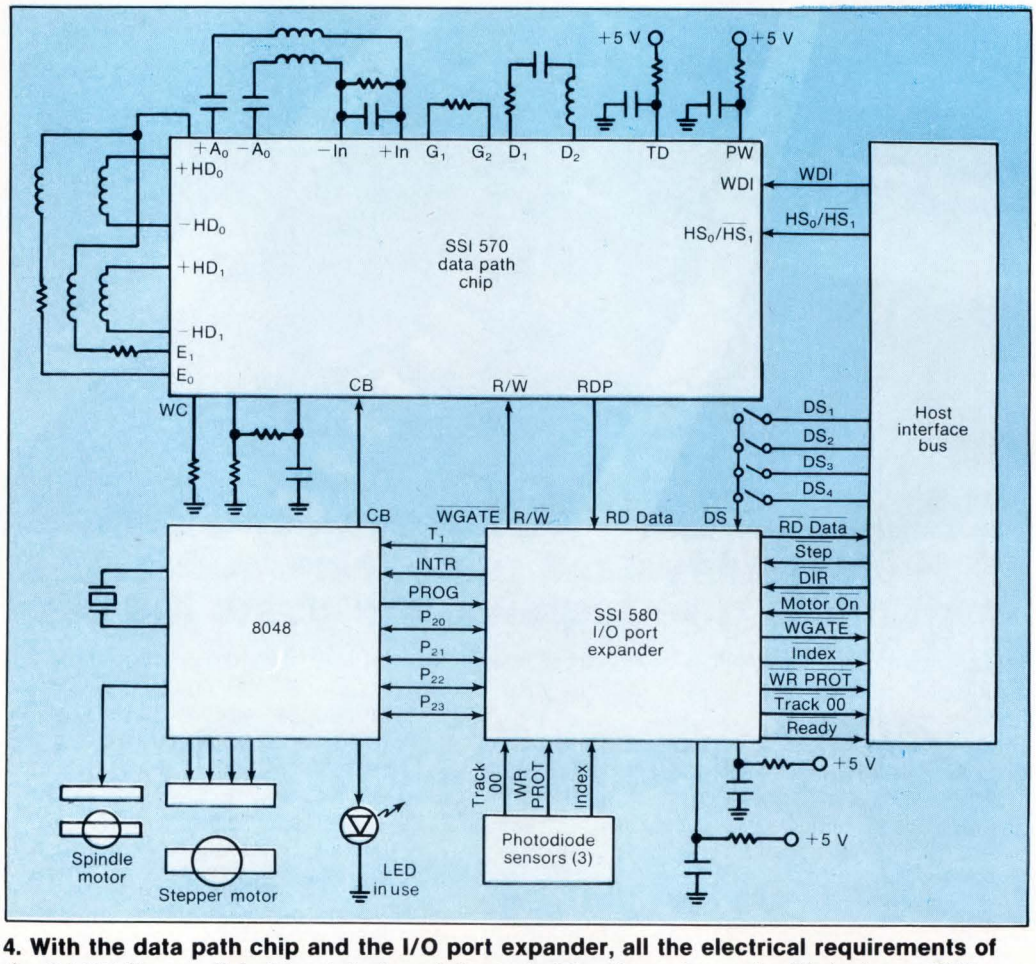
Disk drive control chips

components needed for filtering, timing, damping write current, setting write and erase current, and setting gain. The I/O port expander chip is supported by three optical sensors for the Track 00, Write Protect, and Index pins and by four passive timing components. The 8048 microprocessor needs a crystal for clocking, and it delivers commands to a stepper motor through external power transistors. The spindle motor brings the floppy disk up to speed when turned on by the microprocessor.

The I/O port expander is a bipolar chip, meeting the 48-mA drive requirements of the SA400 interface. But if the controller is incorporated in the drive, or placed very close to it, there will be no cable and thus no need for high currents and hysteresis. Then an SSI 580 type of circuit could be made in CMOS and used with an 80C48 microprocessor to reduce the drive's power requirements.

A further benefit could be derived from the change to CMOS if the designer combined 80C48 and SSI 580 functions on a single chip. That solution would reduce the required circuitry to two ICs, a handful of passive parts, opto-sensors, power drivers, and a crystal. □

How useful?	Circle
Immediate design application	550
Within the next year	551
Not applicable	552



4. With the data path chip and the I/O port expander, all the electrical requirements of the SA400 floppy-disk drive interface (shown in Fig. 1) can be met with just one 8048 microprocessor and a handful of discrete components. The chip set can be fit into 2 in.^{2}, thus allowing the plug-in disk controller card circuitry to be moved into the disk drive.

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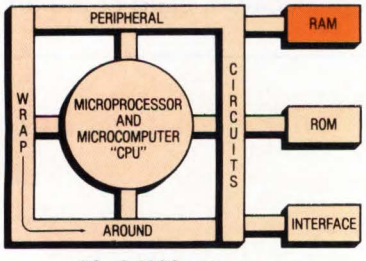

The S-MOS system

SRAM COMPARISON CHART

16K (2K×8) 150ns	OPERATING (1) CURRENT (TYP)	MAX	STANDBY (2) CURRENT (TYP)	MAX	STANDBY (3) CURRENT (TYP)	MAX
LEADER'S STD. 6116	35mA	70mA	5mA	15mA	20μA	2000μA
LEADER'S LP. 6116	30mA	60mA	4mA	12mA	2μA	50μA
S-MOS' STD. 2016	20mA	35mA	.3mA	2mA	1μA	50μA
64K (8K×8) 150ns						
LEADER'S STD 6264	60mA	110mA	1mA	3mA	20μA	2000μA
LEADER'S LP 6264	60mA	110mA	1mA	3mA	2μA	100μA
S-MOS' STD 2064	25mA	40mA	1.5mA	3mA	2μA	100μA

(1) AVERAGE: MIN DUTY CYCLE, $\overline{CS1}$ = VIH, CS2 = VIL (64K)
$\overline{CS}$ = VIH (16K)
(2) $\overline{CS1}$ = VIH OR CS2 = VIL (64K)
$\overline{CS}$ = VIH (16K)
(3) $\overline{CS1}$, CS2 ≥ VCC − 0.2V OR CS2 ≤ 0.2V (64K)
$\overline{CS}$ ≥ VCC (VDD) − 0.2V (16K)

Based on published data sheet parameters

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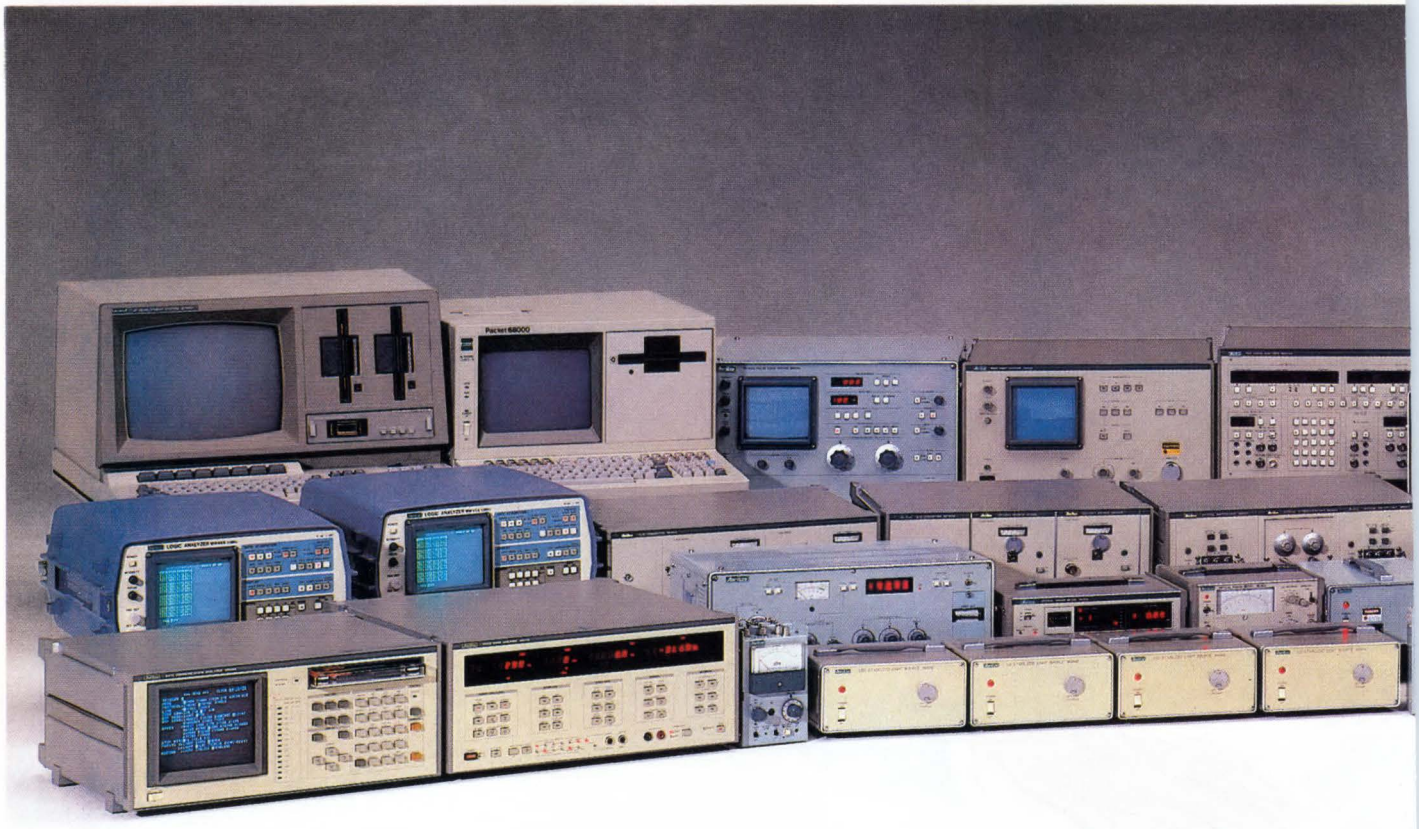

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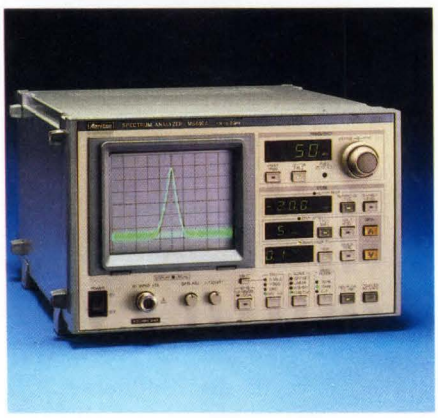

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CIRCLE 88

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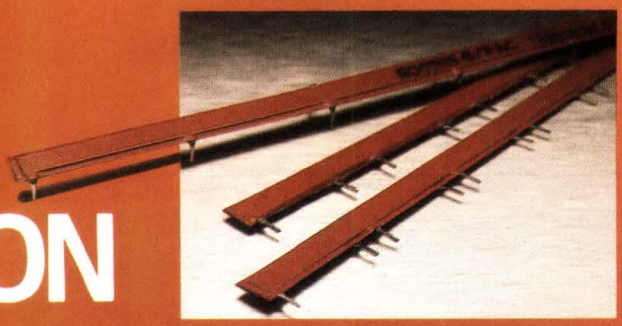

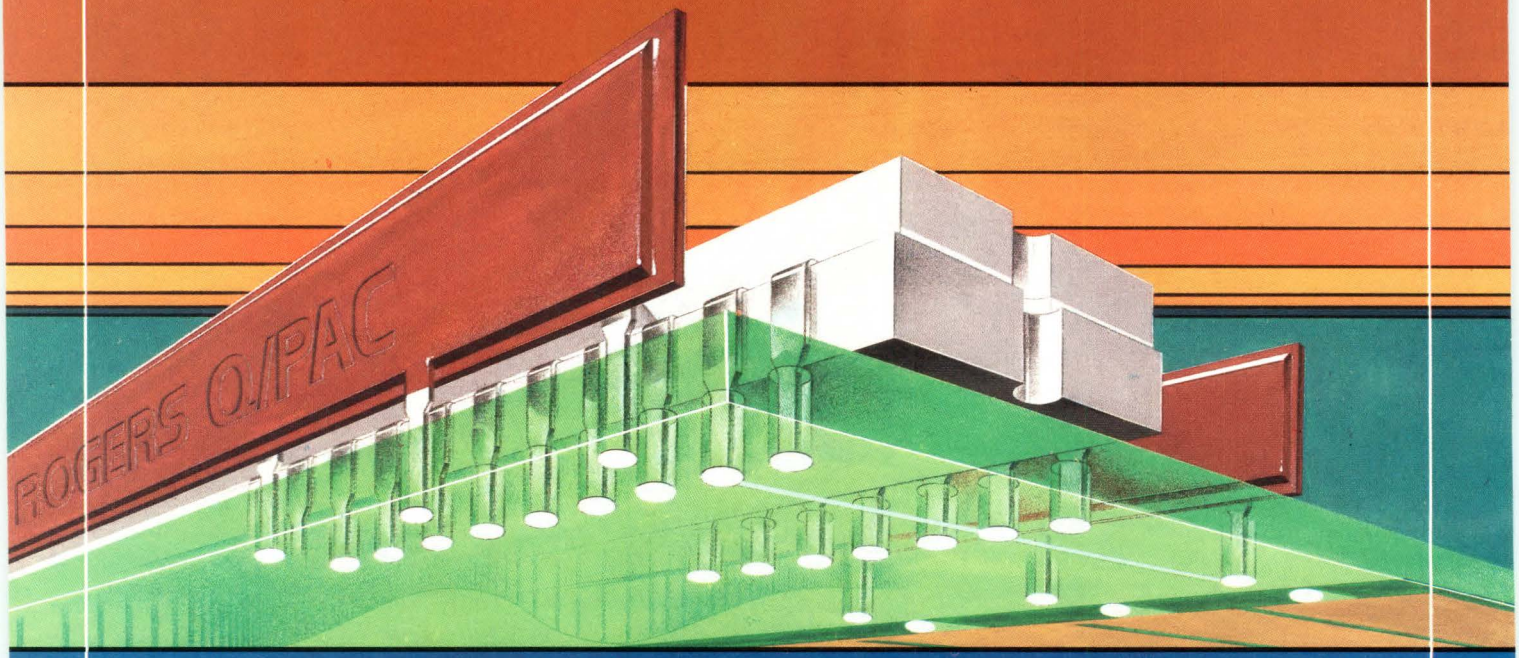

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On-chip EEPROM holds changing register data for 8-bit microcomputer

With a 32-byte EEPROM built into its main registers, a microcomputer chip lowers the risk of losing essential data, whether in multiprocessor or stand-alone setups.

Though some microcomputers incorporate electrically erasable PROM, they use it only for control and application programs, which rarely undergo changes. Ideally, systems should be able to apply that nonvolatile storage to the critical immediate data with which their main registers work.

Making a 32-byte EEPROM part of the main data registers, as does the 16E57 microcomputer chip, permits critical data to be placed in nonvolatile storage with no concern about loss during a scheduled or accidental power outage. Besides that as its main asset, the microcomputer can slip easily into multiple-processor systems or stand on its own.

Frank Gruppuso, Ranjit K. Verma, and **John E. Burgess,** General Instrument Corp.

As manager of logic design engineering at General Instrument's Microelectronics Division in Hicksville, N.Y., Frank Gruppuso works with semicustom, microcomputer, and digital signal-processing products. He holds an MSEE from the Polytechnic Institute of New York.

Ranjit Verma manages the worldwide applications organization, supervising support activities for microcomputers and semicustom, digital signal processing and standard logic products. He has an MSEE from the State University of New York at Stony Brook.

Product line manager John Burgess is responsible for the worldwide marketing and strategic planning for 8-bit microcomputer products. He received an MBA from the University of Rhode Island.

A self-contained oscillator generates the clock frequency, which is determined by an external crystal or ceramic resonator. The oscillator's output is internally divided by eight to set the instruction cycle time of the microcomputer. Thus, a 2-MHz crystal gives an instruction execution time of 4 μs.

The EEPROM is organized as 32 byte-wide words in a file register format. It operates in five modes: programming, erasing, bulk erasing, writing, and reading. The 21 V required for programming and erasing is derived on chip from the main 5-V supply and is completely transparent to the user.

In addition to its EEPROM, the microcomputer contains a mask-programmable control ROM, organized as 512 words by 12 bits. Also on chip are a RAM, arranged as 32 words by 8 bits and set up as a register file to store internally generated data, and 20 bidirectional I/O lines that afford the primary means of user access to the microcomputer.

Like the EEPROM and RAM, I/O is organized into groups of registers that appear to the CPU like any other group of on-chip registers. This arrangement grants the CPU a great deal of flexibility, since there are no specific user I/O instructions.

In keeping with the microcomputer's talents as an efficient control processor, its instruction set permits the user, directly or indirectly, to address, set, reset and test, or skip the status of

EEPROM-equipped microcomputer chip

any register bit or I/O line.

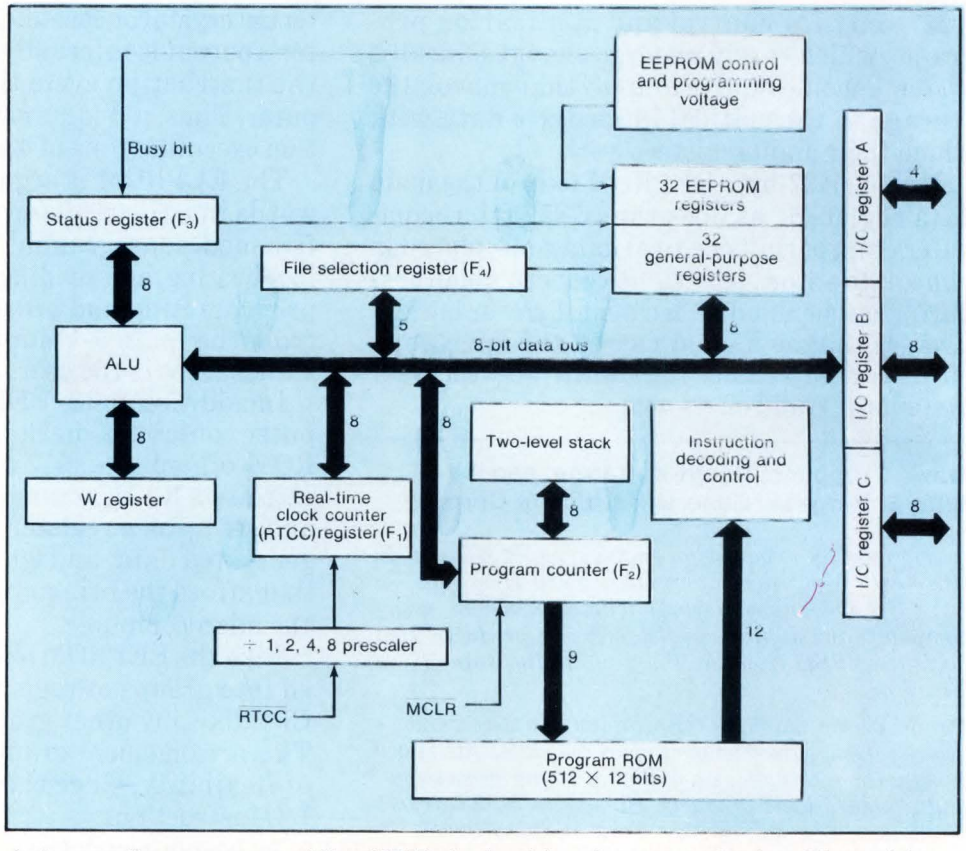
An 8-bit data bus connects the processor's main functional elements: a file of 32 addressable 8-bit registers; the user-defined program ROM containing 512 words that are each 12 bits wide; and of course an ALU (Fig. 1).

A register file concept

The file breaks down into operational and general-purpose registers. The former include F_1, a real-time clock counter (RTCC); F_2 the program counter; F_3, the status register; and the I/O registers. General-purpose registers hold data and control information under the command of the instruction set.

The program ROM contains instructions for all on-chip logic functions. Microinstruction sequencing is controlled through the program counter, which automatically increments when it is executing in-line programs. Program control operations are initiated by Bit Test, Skip, Jump, and Call instructions or by loading computed addresses into the program counter. The two-level stack handles subroutine nesting. The instruction decoding and control block receives the 12-bit instruction word from program memory, decodes it, and issues the appropriate control signals for the desired action.

Status register F_3 stores the condition of the most recent ALU operation. Bits in that register are set or cleared either by bit-level program instructions or by a Move instruction. An 8-bit up-counter, F_1, times or counts external events. Under program control, it can be set to any 8-bit binary value and thereby facilitate counting of 256 external events, either predetermined or undetermined. The contents of the real-time clock counter—that is, the number of events counted—can be interrogated under program control.



1. Among the resources of the 16E57 single-chip microcomputer is a 32-word-by-8-bit EEPROM that gives the device nonvolatile, user-programmable storage. The chip's registers are connected by an 8-bit data bus to an ALU. Included on chip is a 512-word-by-12-bit program ROM.

File selection register F_4, an addressable 5-bit register, indirectly addresses the register file. Although a full address can be written into this block from the internal data bus, only the low-order 5 bits are relevant to F_4. During indirect addressing, the microcomputer accesses the contents of the register pointed to by F_4.

The 20 bidirectional I/O lines are organized into three register groups for interfacing with external devices. Registers F_6 and F_7 are 8 bits wide, F_5 is 4 bits wide. All I/O registers are handled by the ALU in the same manner as any internal register. For example, an I/O port can be incremented and forced to count by direct command. To perform a counting operation, the ALU need not continually increment or decrement its accumulator and transfer the information to an I/O register. The I/O registers are essentially internal devices with pins that interface with the outside world.

An I/O port interfaces with either the input to a TTL circuit or the open-collector output of such a device (Fig. 2). When the microcomputer puts out data through the port, the data is latched and the output pin is connected directly to the TTL input. But when data is being received by the processor, the port latch is first set to a high level under program control. That turns off transistor Q_2 and allows the TTL open collector to be pulled up by Q_1, a transistor that can source a minimum of 100 μA. Thus, the TTL device either forces the latched output line low or keeps it high.

The ALU's register

The ALU contains one temporary working register—the accumulator, dubbed the W register—plus the gating logic needed to perform Boolean and arithmetic operations on data stored in the W register or in any file register. The various operations use one or two 8-bit operands. One of them is fetched from any of the file locations, or it may be a literal within the instruction. If needed, the other operand is held in the W register.

Using the operations singly or in combination, the ALU can add, subtract, multiply, and divide the 8-bit operands. It also performs BCD arithmetic, mask operations, and bit and field manipulations. Typically, the microcomputer executes an instruction in just 3 μs.

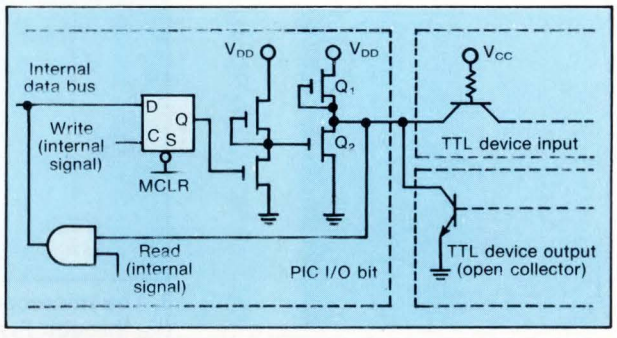
Resident data memory consists of 64 byte-wide words that are addressed in three register banks (Fig. 3). The first bank consists of 32 registers: F_0 through F_7 (octal)—among them the I/O registers, the program counter, and the real-time clock counter—plus registers F_{10} through F_{17}, which are general- and special-purpose RAM for storing program data. The 32 EEPROM registers are addressed as two banks of 16 each—F_{20} through F_{37} (also octal)—which are chosen according to the states of two bank selection bits, ESEL 1 and ESEL 2, which are located within status register F_3.

The first bank is selected when ESEL 1 is a logic 1 and ESEL 2 is a logic 0. The second bank is chosen with the reverse logic levels. All the preceding registers, from F_0 through F_{17}, are addressable, regardless of the states of ESEL 1 and ESEL 2.

The EEPROM compared

The 32 nonvolatile EEPROM registers operate very much like the general-purpose file registers. First, ESEL 1 and ESEL 2 are set for the appropriate bank and then the operation instructions—Erase/Write, Erase, Write, Read—are executed. To address the EEPROM registers, the ESEL bits are set to 10 or 01. If both bits are either 0 or 1, the standard registers are addressed.

The nonvolatile registers differ from the standard types in that only a logic 1 can be written to bit positions. To store a data pattern, the EEPROM must first be erased to all logic 0s and then 1s written to the appropriate bit positions. A program operation is performed automatically when either of the two banks is selected,



2. Users interface with the microcomputer through 20 bidirectional I/O lines, one of which appears here. The I/O ports are fully TTL-compatible.

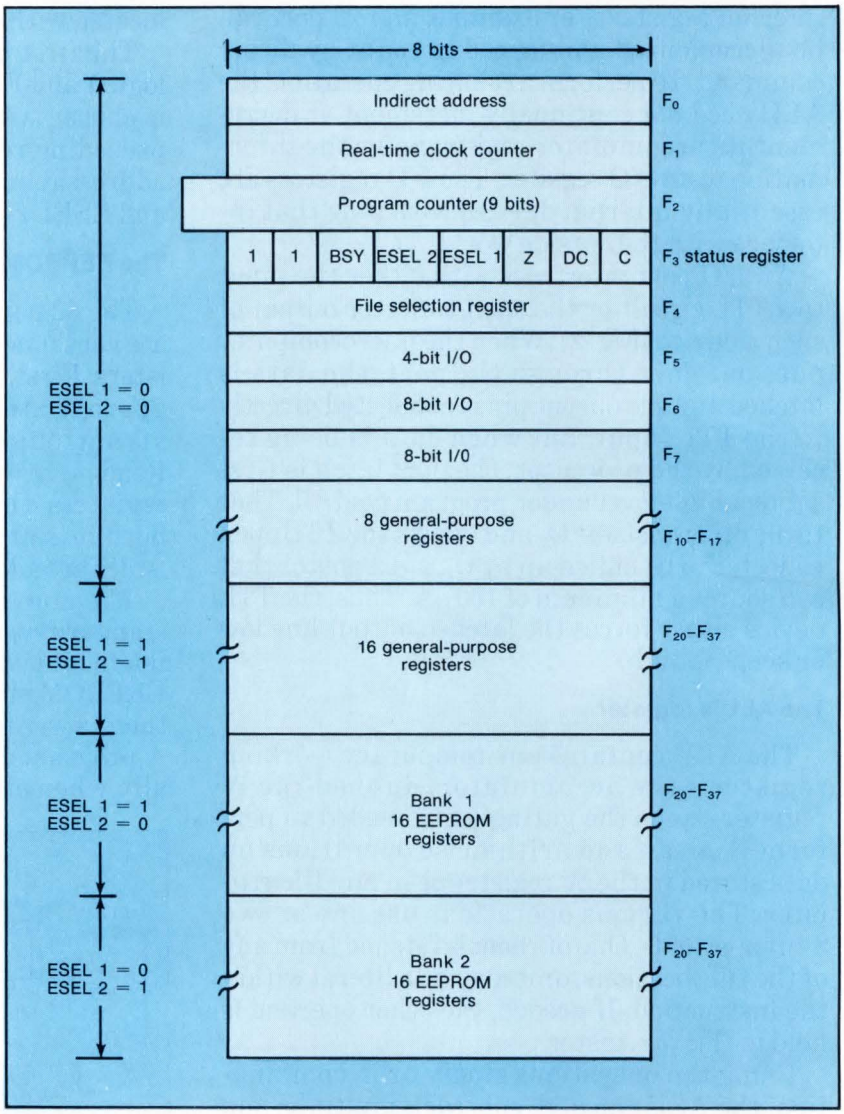
EEPROM-equipped microcomputer chip

and a MOVWF (Move W to F) instruction is executed on registers F_{20} through F_{37}. Erasing and writing take about 20 ms each, but they are automatic and transparent to the software.

Any one EEPROM register can be erased by selecting either bank and then executing a CLRF instruction on F_{20} through F_{37}. An entire bank of registers can be erased in a single 15-ms bulk operation. To do so, ESEL 1 and ESEL 2 are set to logic 1 and an ERAL instruction is executed on F_{20} through F_{37}.

To write into an individual EEPROM register, first a bank is selected and then an IORWF f, 1 (Inclusive-OR W and F) instruction is executed on F_{20} through F_{37}. If the register earlier was erased to 0, register W will be copied correctly into the register. If not, only the 1s will be written. To write a 1 to an individual register bit, the BSF instruction may be used. Data is read at the instruction cycle time of the microcomputer, or in this case, about 3 μs.

The microcomputer can perform other



3. The microcomputer's register file is divided into operational registers (F_0 through F_{17}) and working registers (F_{20} through F_{37}). The EEPROM registers are selected only when ESEL 1 and ESEL 2 are in opposite logic states; when the bits are in the same state, the operational registers are selected.

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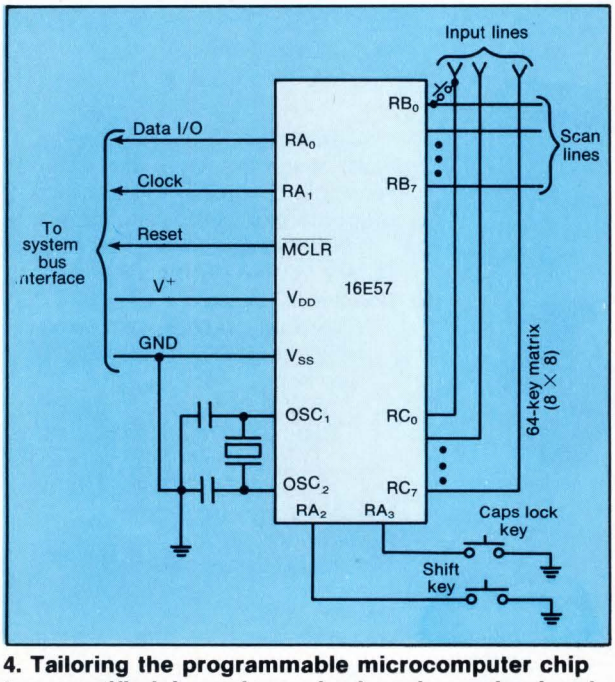
CIRCLE 90

system tasks while programming is in progress. The Busy bit in status register F_3 is a read-only bit that is polled by the software to determine whether programming is complete before attempting other operations on a EEPROM register. A logic 1 in that bit location indicates that programming is taking place. If another operation is attempted before the bit goes low, the microcomputer suspends execution.

A streamlined command set

Each instruction in the microcomputer's set is a 12-bit word that follows a powerful yet easy-to-use command structure. The single 12-bit instruction word provides several unique characteristics. Fetching the entire instruction word all at once greatly simplifies the microcode and enhances throughput by not requiring multiple fetches from program memory. The machine is also fault-tolerant. Should the program counter accidentally jump to a random location, the program will resume by always executing instructions and never data bytes, as would be the case if memory were organized in 8-bit data bytes. For simplicity, all instructions are single words and are confined to the microcomputer; that is, the instructions are not intended to address external memory chips or peripheral devices.



4. Tailoring the programmable microcomputer chip to a specific job, such as a keyboard encoder, is relatively simple. The keys, arranged in an 8-by-8 matrix, connect directly to the chip's bidirectional I/O lines. Software in EEPROM directs routine scanning, encoding, and debouncing.

The basic repertoire of 36 instructions is divided into four groups: byte-oriented register file operations, bit-oriented ones, literal and control operations, and byte-oriented EEPROM file register operations. Each instruction is further divided into an op code, which defines the command type, and one or more operands that provide additional operational characteristics.

For byte-oriented operations, f is a designator that specifies which of the 32 file registers the instruction will use. The destination designator, d, indicates where the result is placed. If d is 0, the result goes to the accumulator; if it is 1, the result returns to the file register specified in the instruction.

In bit-oriented instructions, b designates the number of the field bit affected by the operation. For control operations, k is an 8- or 9-bit constant; for operations on literals, it is a literal value. In addition to the basic instruction set, an extra set of about 40 commands—actually a superset—is upwardly compatible with the basic commands.

Because of its on-board EEPROM, the 16E57 can be easily customized for use in a variety of specialized control applications. Often those applications are similar except for certain information that varies from job to job. Keyboard encoders, for example, perform a like function in most terminals, but must handle slightly different function key assignments, serial port parameters, and other system attributes.

Rather than use different encoders, a generalized keyboard encoder can be built with the 16E57. Variable or specialized key attributes

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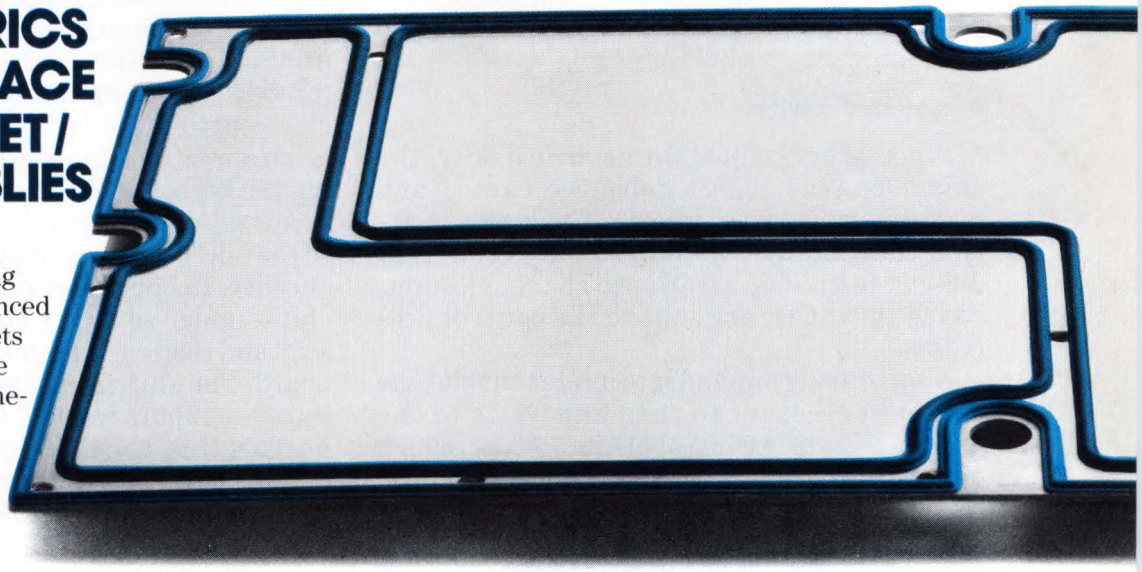

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CIRCLE 91

are simply stored in the chip's EEPROM. Aside from the cost advantage, the single-chip approach adds programmability to the end product.

A system overview

When programmed for keyboard duty, the chip must scan, detect, debounce, encode, and buffer key closures (Fig. 4). The keys are arranged in a 8-by-8 matrix and are connected directly to the chip's I/O lines. The key closures, coded in ASCII, are sent to the control processor.

A software command interpreter enables the control processor to read and write to the EEPROM under control of the 16E57. Such a design frees the control processor from the need to supervise the EEPROM's 20-ms erase/write timing specification. Also, the time to read data from the control processor and to program an EEPROM location does not interfere with key scanning or encoding. Instead, on-chip control logic performs an EEPROM program operation automatically, without bothering the keyboard encoding software.

A crystal or ceramic resonator must be added to the microcomputer chip to create a keyboard encoder. In operation, ports RB and RC of the chip—under software control—continuously scan and read a 64-key mechanical contact keyboard. The shift and caps lock keys appear as separate inputs to the RA port, with software performing the control key function on a defined key in the matrix. Internal pull-up resistors maintain a valid logic 1 on the ports during read operations, thus negating the need for external resistors.

Once a key is verified, debounced, and encoded, the key code is transmitted synchronously through one pin of the RA port to the bus interface logic. The clock signal is supplied through another pin of the RA port. In the same manner, commands and data from the control processor are sent over the serial data wire to the 16E57. In its simplest form, the serial-to-parallel interface is controlled by the microcomputer and an 8-bit bidirectional shift register.

The microcomputer scans the keyboard matrix by first selecting one of the eight rows and then reading the eight columns. If no keys are depressed in any row, the next is read. As the scan proceeds, a count is kept of the number of keys that have been checked.

When a key closure is detected, debouncing data is pulled from an EEPROM file and used by the debounce-delay timer. During the debouncing period, the clock line (pin RA_1) is checked for commands arriving from the host. After debouncing, the closure is verified and the count, generated during the scan, serves as an offset in a look-up table containing the various key codes.

If only one key has been depressed, the autorepeat timers are read from EEPROM and entered into the repeat-timer run registers that are used for counting down. The modified ASCII or other maskable codes are then sent to

Program 1. Sample code for writing data into EEPROM register

```
; Desired EEPROM bank selected
; FSR = Destination of byte to be written
; Count = Number of bytes to write
Next  Call    GETBYT       ; Get data byte from system bus
      MOVF    DATA,W       ; Put data byte in working register
      MOVWF   0            ; Save in EEPROM
      DECFSZ  Count        ; See if done yet
      Goto    Wait         ; No—wait for ready bit
      Goto    Save         ; Last file—exit
Wait  BTFSC   Status,Busy  ; Wait for busy bit to be cleared
      Goto    Wait
      INCF    FSR          ; Destination pointer to next location
      Goto    Next
```

Program 2. Sample code for putting out function key values from EEPROM

```
      MOVLW   Bytes        ; Put number of data bytes in counter
      MOVWF   Count
      MOVLF   Pointer      ; Get address of character string
      MOVWF   FSR          ; Put address into indirect
                           ; register
Next  MOVF    0,W          ; Pick up data byte
      MOVWF   Keynum       ; Put in file to be output
      Call    Output       ; Send file
      INCF    FSR          ; Point to second byte
      DECFSZ  Count        ; Decrement counter of
                           ; Bytes - skip if finished
      Goto    Next
```

the system bus.

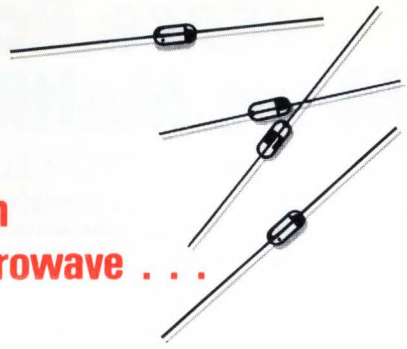
The bit corresponding to that key in the run bit map is set, indicating that the key has been registered. The next time the key is scanned, the bit map will be checked to see if it has already been sent to the host.

There are two methods for reading and writing EEPROM files in the keyboard application. The first is used by the control processor for such information as the terminal and user identification numbers, 50- or 60-Hz operation, serial port characteristics, and other system attributes. The process is initiated by pulling the clock line low and thus placing the 16E57 in its programming mode, so that it can read a command from the bus. A single-byte command is needed for setting the EEPROM's pointer byte count and starting location.

If the command indicates that data must be written into EEPROM, the first data byte from the system bus will be written into the location indicated in the command word. If only one byte is written, an EEPROM write-acknowledgment code is sent to the control processor. For several bytes, a check will be made to see if the Busy bit has cleared, indicating that 16E57 has completed writing at the location. The additional bytes of data are then written. After the last byte has been written, a verification code is returned to the control processor (Program 1). When an EEPROM file is read, the value at the location indicated by the file number is put out onto the bus.

Another program procedure designates specific keys for code-conversion chores. The feature is very handy for assigning a special character or character string to a specific function key. With that programming (Program 2), when the 16E57 detects the simultaneous closure of the Control, Shift, and Function key, the sequence of characters entered is written to the EEPROM and assigned to the function key. The next time the function key is depressed, the microcomputer will transmit those characters to the control processor. □

How useful?	Circle
Immediate design application	553
Within the next year	554
Not applicable	555



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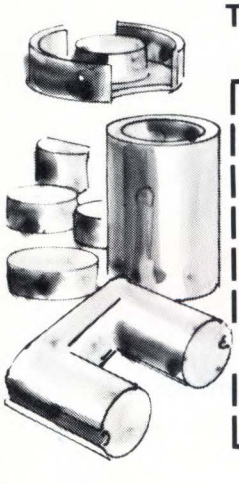

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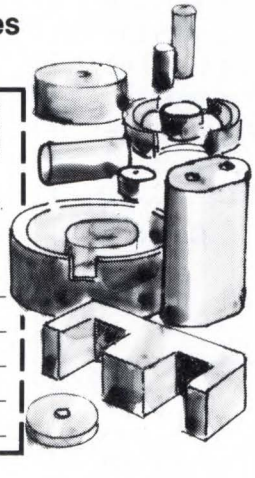

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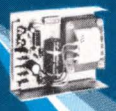

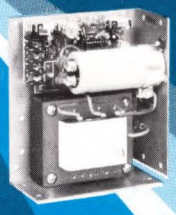

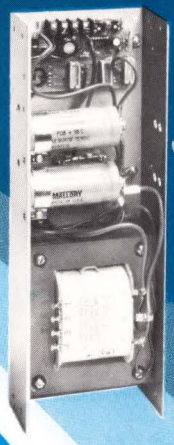

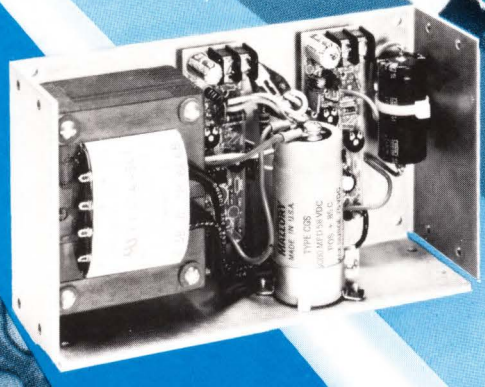

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- 1 to 3 Outputs
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Voltage/Current Ratings – World Series and Regular Models

SINGLE OUTPUT

REGULAR MODEL	WORLD SERIES MODEL	VOLTAGE VOLTS	CURRENT AMPS	CASE CODE
VQ5-3C	W100A	5	3	A
VQ5-6C	W101B	5	6	B
VQ5-9C	W102C	5	9	C
VQ5-12C	W103D	5	12	D
Q5-18C	—	5	18	F
Q5-27C	—	5	27	G
VQ12-1.7	W104A	12	1.7	A
VQ12-3.4	W105B	12	3.4	B
VQ12-5.7	W106C	12	5.7	C
VQ12-6.8	W107D	12	6.8	D
Q12-10.8	—	12	10.8	F
Q12-17.1	—	12	17.1	G
VQ15-1.5	W108A	15	1.5	A
VQ15-3	W109B	15	3	B
VQ15-4.8	W110C	15	4.8	C
VQ15-6	W111D	15	6	D
Q15-9.5	—	15	9.5	F
Q15-14.4	—	15	14.4	G
VQ24-1.2	W112A	24	1.2	A
VQ24-2.4	W113B	24	2.4	B
VQ24-3.6	W114C	24	3.6	C
VQ24-4.8	W115D	24	4.8	D
Q24-7.2	—	24	7.2	F
Q24-9.9	—	24	9.9	G
—	W116A	48	0.5	A
—	W117B	48	1.0	B
—	W118D	48	3	D

All 5 Volt single output units have a built in fixed crowbar overvoltage protector. World Series multiples also have this type of built in crowbar on output #1 when its voltage is specified as 5 Volts only. Crowbar protectors are optionally available on other models and are selected from the chart below.

Voltage Range	0-15 Amp	15-36 Amp
6-15	CB41	CB51
15-30	CB42	CB52

DUAL AND TRIPLE OUTPUTS

Corresponding ratings separated by slash marks are alternate field selectable ratings for the designated output.

STANDARD MODEL	WORLD SERIES MODEL	OUTPUT #1		OUTPUT #2		OUTPUT #3		CASE CODE
		VOLTS	AMPS	VOLTS	AMPS	VOLTS	AMPS	
CP20800	W208A	5/12/15	.4/1/.8	5/12/15	.4/1/.8	—	—	1/DA
CP20900	W209B	5/12/15	.7/1.7/1.5	5/12/15	.7/1.7/1.5	—	—	2/DB
CP21000	W210C	5/12/15	1.5/3.4/3	5/12/15	1.5/3.4/3	—	—	3/DC
CP20500	W205C	5	2	12	4	—	—	3/DC
—	W214A	5	2	24	.5/1.7p	—	—	1/DA
CP20000	—	5	3	5	3	—	—	1/DA
CP20100	—	5	6	5	6	—	—	3/DC
CP20200	—	5	2	5/9-15	.3/.6	—	—	1/DA
CP20300	—	5	3	5/9-15	.6/1.3	—	—	2/DB
CP20400	—	5	6	5/9-15	1.2/2.5	—	—	3/DC
CP20600	—	5	1.5	12	1.8/3.2p	—	—	2/DB
CP20700	—	5	.8	12	1.1/1.7p	—	—	1/DA
CP21100	—	18-20/24	.4/.6	18-20/24	.4/.6	—	—	1/DA
CP21200	—	5	.5/.7p	12	.9/1.8p	—	—	1/DA
CP21300	—	5	3	24	1.2	—	—	2/DA
CP300000	W300A	5	2	5/9-15	.2/.4	5/9-15	.2/.4	1/TA
CP301000	W301D	5	3	5/12/15	.4/1/.8	5/12/15	.4/1/.8	4/TD
—	W318D	5	6	5/9-15	.7/1.5	5/9-15	.7/1.5	4/TD
CP302000	W302E	5	6	5/12/15	.7/1.7/1.5	5/12/15	.7/1.7/1.5	5/TE
CP303000	W303E	5	8	5/12/15	.7/1.7/1.5	5/12/15	.7/1.7/1.5	5/TE
CP304000	W304F	5	12	5/12/15	.7/1.7/1.5	5/12/15	.7/1.7/1.5	6/TF
CP313000	W313F	5	6	12	1	24	4	6/TF
CP308000	W308E	5	3	5	.6	24	5/6p	5/TE
CP305000	W305G	5	12	5/12/15	1.5/3.4/3	5/12/15	1.5/3.4/3	7/TG
CP306000	—	5	1	5	.5	24	1.5/1.7p	4/TD
CP307000	—	5	2.5	5	.5	24	3/3.4p	5/TE
CP309000	—	5	9	12	.8	24	.5/4.5p	5/TE
CP310000	—	5	2	12	.4	12	.4	1/TA
CP311000	—	5	1.7/2.2p	5	.15/.2p	24	.2/3p	4/TD
CP312000	—	5	3	5	.6	24	4	5/TE

CP Models can be fitted with a crowbar OVP option on one or more outputs. A code number 1 in any of the positions following the root 5 character model designator defines this option.

Specifications – World Series and Regular Models

Input
100, 117, 220, 230, 240 VAC ±10%, 47-440 Hz.
Derate output current 10% for 50 Hz. operation.
Consult factory for 400 Hz. operation.
Regular models 115/230 VAC ±10%.

Output
See table of models. Outputs are adjustable ±5%.

Operating Temperature
0°C to 50°C full rated, derate linearly to 40% at 71°C.
Single output regular models derate to 50%.

Storage Temperature
−20°C to 85°C.

Dielectric Withstand Voltage

	World Series Models	Regular Models
Input to ground	3750 VAC	1250 VAC
Input to output	3750 VAC	1250 VAC
Output to ground	500 VAC	300 VAC

Leakage Current
5 microamps typical line to ground.
Regular models 20 microamps.

Creepage Distance
Greater than 6 mm line connected metal parts to dead metal.

Line Regulation
±.05% for a 10% line change.

Load Regulation
±.05% for a 50% load change.

Ripple & Noise
1 mv rms, 5 mv p-p.

Peak Currents
Numbers after a slash mark followed by a lower case "p" are surge ratings that units deliver for approximately 500 milliseconds.

Temperature Coefficient
0.03% per °C.

Stability
±0.1% typical for 8 hours after warm up.

Recovery Time
30 microsec typical for full line changes or 100% load increase.

Remote Programming
1000 ohms per Volt approximately.

Remote Sensing
Built in capability with loss of sense protection.

Overload & Short Circuit Protection
Adjustable auto-recovery foldback current limiting; time delayed with a second foldback loop in units with surge current capability.

Reverse Voltage Protection
Provided on outputs and pass elements.

Overvoltage Protection
All 5 Volt models have built in fixed crowbar.
Optional fixed crowbar OVP for other models.

Interface
Input solder lugs, output barrier block terminals.

Mounting
3 to 4 mounting surfaces, 5 orientations.

Mechanical
Refer to drawings for dimensions, parts locations and weight.

Vibration & Shock
Per MIL-STD-810C

World Series Models Meet Worldwide Safety Requirements, Regular Models Meet UL, CSA Requirements.

UL — **UNDERWRITERS LABORATORIES, INC.**
UL 1012 — Power Supplies
UL 478 — Electronic Data Processing Units and Systems

CSA — **CANADIAN STANDARDS ASOCIATION**
CSA 22.2, No. 143-1975 — Office Machines
CSA 22.2, 154-1975 — Data Processing Equipment

IEC — **INTERNATIONAL ELECTRO-TECHNICAL COMMISSION**
IEC 380 — Safety of Electrically Energized Office Machines
IEC 435 — Safety of Data Processing Equipment

VDE — **VERBAND DEUTSCHER ELECTRO-TECHNIKER**
VDE 0730, Part 2P — Business Machines
VDE 0804/3.77 — Telecommunications and Electronic Data Processing Equipment

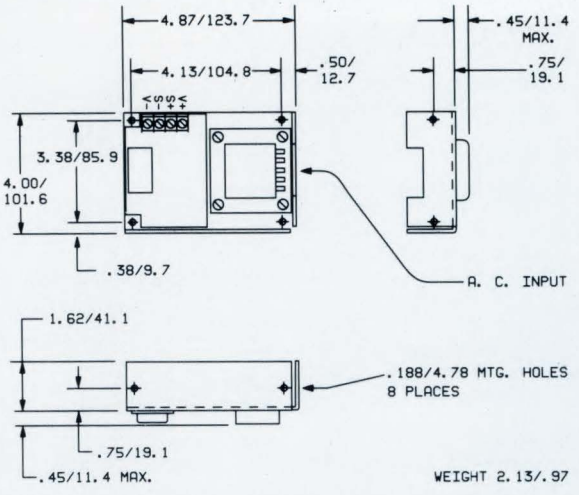
BPO — **BRITISH POST OFFICE TECHNICAL GUIDE No. 26**

ECMA — **EUROPEAN COMPUTER MANUFACTURERS ASSOCIATION**
ECMA – 57 — Safety Requirements for Data Processing Equipment

CEE — **INTERNATIONAL COMMISSION ON RULES FOR THE APPROVAL OF ELECTRICAL EQUIPMENT**
CEE 10, Part 2P — Specification for Business Machines.

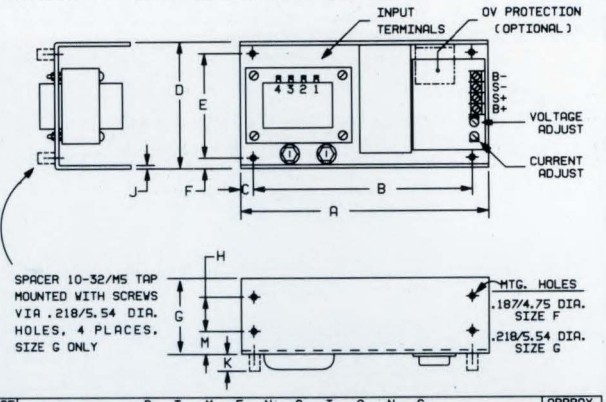
Dimensions – World Series and Regular Models (inches/mm)

SIZE A SINGLE OUTPUT



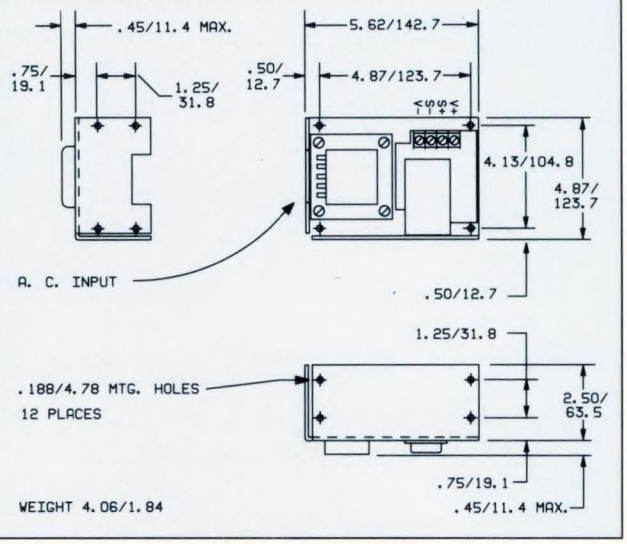
WEIGHT 2.13/.97

SIZES F & G SINGLE OUTPUT



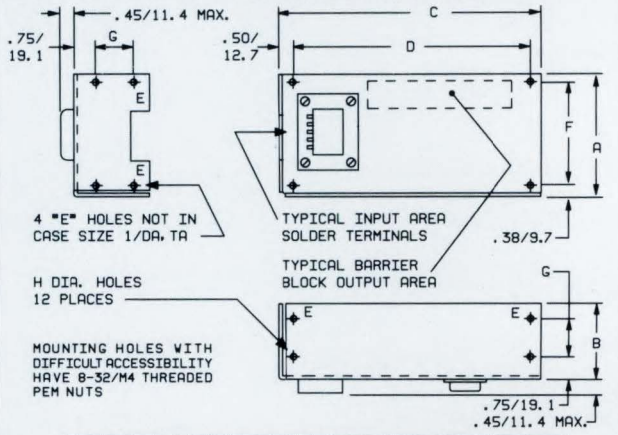
CASE SIZE	DIMENSIONS A	B	C	D	E	F	G	H	J	K	M	APPROX. WEIGHT
F	14.00 / 355.6	13.00 / 330.2	.50 / 12.7	4.87 / 123.7	4.13 / 104.8	.375 / 9.53	2.75 / 69.9	1.25 / 31.8	.13 / 3.2	.50 / 12.7	.75 / 19.1	14.00 / 6.35
G	16.75 / 425.5	16.00 / 406.4	.50 / 12.7	4.87 / 123.7	4.13 / 104.8	.375 / 9.53	4.13 / 104.8	2.50 / 63.5	.13 / 3.2	.75 / 19.1	1.06 / 27.0	21.00 / 9.53

SIZE B SINGLE OUTPUT



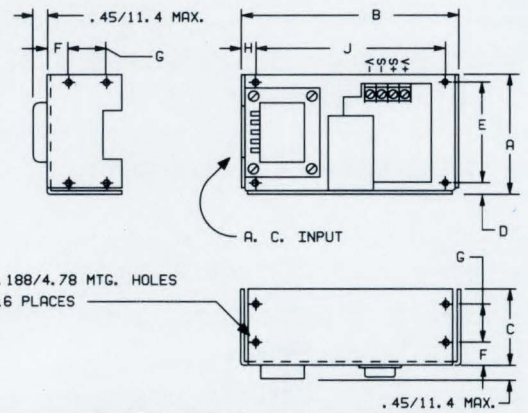
WEIGHT 4.06/1.84

SIZES A & B MULTIPLE OUTPUT



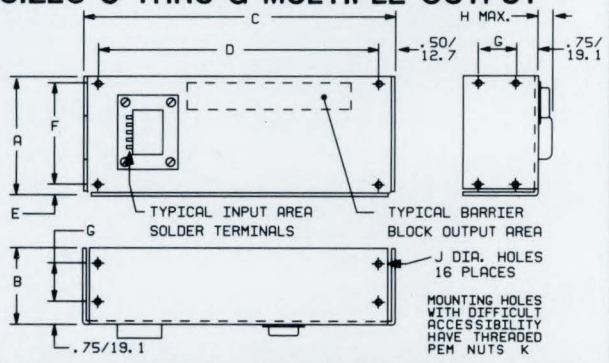
CASE SIZE	DIMENSIONS A	B	C	D	F	G	H	APPROX. WEIGHT
1/DA, TA	4.00 / 101.6	1.62 / 41.1	6.50 / 165.1	5.75 / 146.1	3.38 / 85.9	00	.213 / 5.41	2.00 / .91
2/DB, TB	4.87 / 123.7	2.50 / 63.5	7.00 / 177.8	6.25 / 158.8	4.13 / 104.8	1.25 / 31.8	.213 / 5.41	4.00 / 1.81

SIZES C & D SINGLE OUTPUT



CASE SIZE	DIMENSIONS A	B	C	D	E	F	G	H	J	APPROX. WEIGHT
C	4.87 / 123.7	7.00 / 177.8	2.75 / 69.9	.50 / 12.7	4.13 / 104.8	.75 / 19.1	1.25 / 31.8	.38 / 9.7	6.25 / 158.8	6.13 / 2.78
D	4.87 / 123.7	9.00 / 228.6	2.75 / 69.9	.50 / 12.7	4.13 / 104.8	.75 / 19.1	1.25 / 31.8	.50 / 12.7	8.00 / 203.2	7.88 / 3.57

SIZES C THRU G MULTIPLE OUTPUT



CASE SIZE	DIMENSIONS A	B	C	D	E	F	G	H	J	K	APPROX. WEIGHT
3/DC, TC	4.87 / 123.7	2.75 / 69.9	9.38 / 238.3	8.38 / 212.9	.50 / 12.7	4.13 / 104.8	1.25 / 31.8	.45 / 11.4	.213 / 5.41	8-32 / M4	7.50 / 3.40
4/ TD	4.00 / 101.6	2.50 / 63.5	10.25 / 260.4	9.25 / 235.0	.38 / 9.7	3.38 / 85.9	1.25 / 31.8	.45 / 11.4	.213 / 5.41	8-32 / M4	5.00 / 2.27
5/TE, QE	4.87 / 123.7	2.75 / 69.9	11.00 / 279.4	7.00 / 177.8	.50 / 12.7	4.13 / 104.8	1.25 / 31.8	.45 / 11.4	.213 / 5.41	8-32 / M4	9.00 / 4.08
6/ TF	4.87 / 123.7	2.75 / 69.9	14.25 / 362.0	8.75 / 222.3	.50 / 12.7	4.13 / 104.8	1.25 / 31.8	.62 / 15.7	.250 / 6.35	10-32 / M5	11.00 / 4.99
7/ TG	4.87 / 123.7	3.75 / 95.3	15.00 / 381.0	14.00 / 355.6	.50 / 12.7	4.13 / 104.8	2.50 / 63.5	.65 / 16.5	.250 / 6.35	10-32 / M5	12.00 / 5.44

Note: Flap cutout may be missing on regular models.

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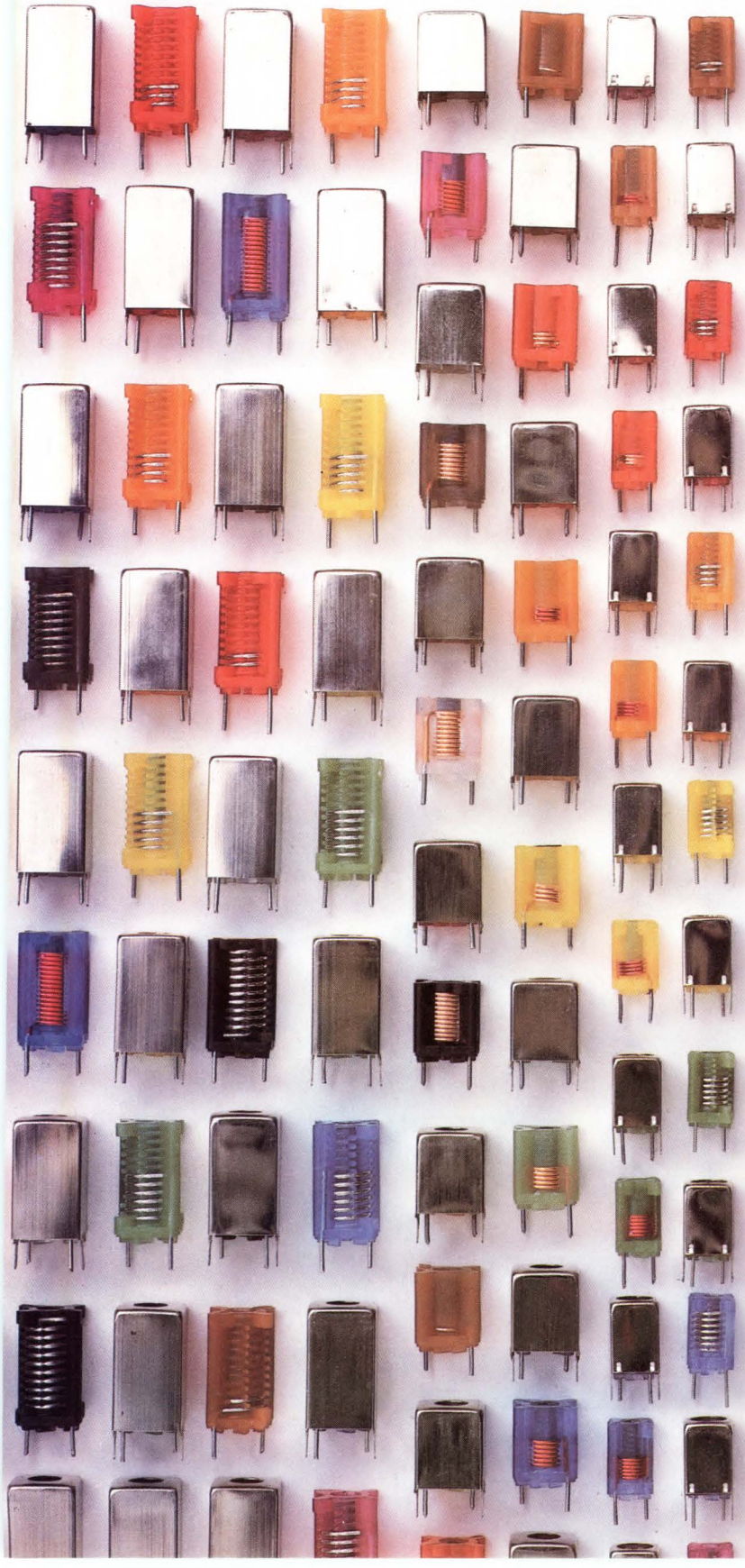

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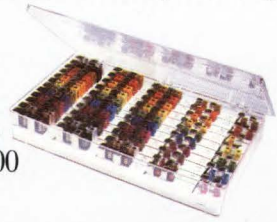
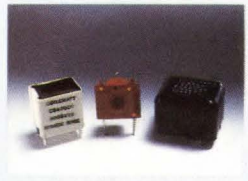


Chip Inductors



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CIRCLE 231

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CIRCLE 95

GOULD
Electronics

Associative memory calls on the talents of systolic array chip

A monolithic systolic array puts its on-chip memory to good use, first searching out the desired information and then processing it.

This is the fourth in a series of articles dedicated to the first commercial systolic array processor chip. The series began with the cover article in the Oct. 31 issue (p. 207) and has continued in every consecutive issue.

How to retrieve data from memory is a classic problem for designers. Theoretically, one of the simplest ways to get information is to match the memory contents with the desired key, much as an instructor calls upon pupils to volunteer an answer to a question. However, processors traditionally force programmers to call memory using addresses. That scheme often makes for relatively slow processing. Searching through a set of numbers for the one with the highest value, for instance, typically forces a von Neumann processor to examine each member in the set at least once.

An alternative is an associative memory system, which matches some part of the desired data within memory instead of requiring addresses. Known by a host of names, including content-addressable memory, data-addressed memory, parallel search memory, and search associative memory, the technique has been called into service a number of times in various applications. But such systems are usually fairly large and expensive.

The Geometric Arithmetic Parallel Processor, or GAPP, takes a new approach to this long-standing dilemma. The first systolic array processor chip, the device is not only well suited to associative memory but can be configured in a comparably small system as well. Further, since it performs logical and arithmetic operations, it also serves as an associative processor that works on the data found in a memory search.

The chip carries 72 single-bit processors that run in parallel as a single-instruction, multiple-data path system. Each processor element is fitted out with 128 bits of dedicated RAM. Also vital to associative memory is the IC's global broadcast function, which lets users transmit data, such as the search word, to all of the processor elements simultaneously.

The tremendous speed advantage of parallel processing over conventional methods is demonstrated in the relative time needed to perform associative memory searches. Searching for a single number in a set with N members, a traditional processor running an algorithm that lets it look just once at each number takes up to N cycles to locate the desired data. The associative processor, in contrast, needs M cycles, where M equals the number of bits in the target

Lyle Wallis, NCR Microelectronics

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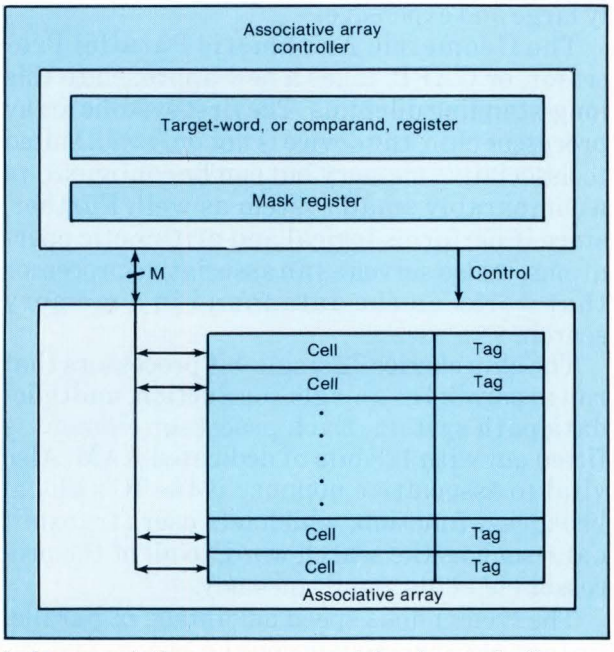
information. The device interrogates the memory entries in parallel, and once the proper information has been found, it can be either processed by the associated processor or passed directly to the host.

An associative memory unit can be broken down into two main components: an associative array and an associative array controller (Fig. 1). The arrangement is similar to traditional memories, which consist of an array of addressable cells and a controller.

Other functions

In addition to managing the memory, the controller also handles sequencing. It contains two registers: one holds the data that the host is looking for, called the "comparand"; the other contains a mask, which screens out unwanted bits during processing.

The associative array comprises a group of cells, each of which generally holds a single word. Each cell has a tag bit to notify the controller when its data matches the sought-after word. When there is a match, the tag bit is set and that cell is termed a responder. If the desired data is not in that cell, the tag bit remains unchanged and the cell is dubbed a nonresponder.



1. An associative memory consists of a controller and an array of memory cells. The first section manages the second and stores the target word—or comparand—and the mask, both of which come from the host. The tag bits attached to each cell denote what data is located at any one.

Every cell within an associative array also performs three tasks—compare, write, and read. The first and most fundamental task simply compares the masked target data with the contents of the cells, setting the tag bit if there is a match. The second then writes a data word to the responding cells. Read, the final function, shifts the contents of the responding cells to the output bus. If there is more than one responder, the output is the bit-by-bit logical OR of all the responding cells. These three functions are carried out only on data in the responding cells; nonresponding cells are untouched.

This architecture can easily implement the associative memory and handle associative processing tasks. The feature set of the systolic array chip performs all the operations needed to form an associative array, and when coupled with a programmable control circuit, it also serves as an associative processor.

Maintaining control

The GAPP chips themselves form the associative array. However, since these devices do not have any control features, an external controller must be used to sequence the array and to oversee the target-word and the mask register. It consists of a control store, address sequencer, and host computer (Fig. 2).

The associative array can be built in various sizes, since the chips can be ganged together to create larger arrays. Because each processor element within a grid of chips is a serial processor, word widths greater than one bit must be emulated serially. The on-chip RAM lets the elements handle a variety of word widths, as well as multiple words and multiple tag bits since every RAM location is individually addressable. Further, there will be some RAM left over that can be used as a scratchpad or for storing arithmetic operands and other data.

Input and output for the full array are handled via the communications (CM) bus. Input usually comes from traditional processors

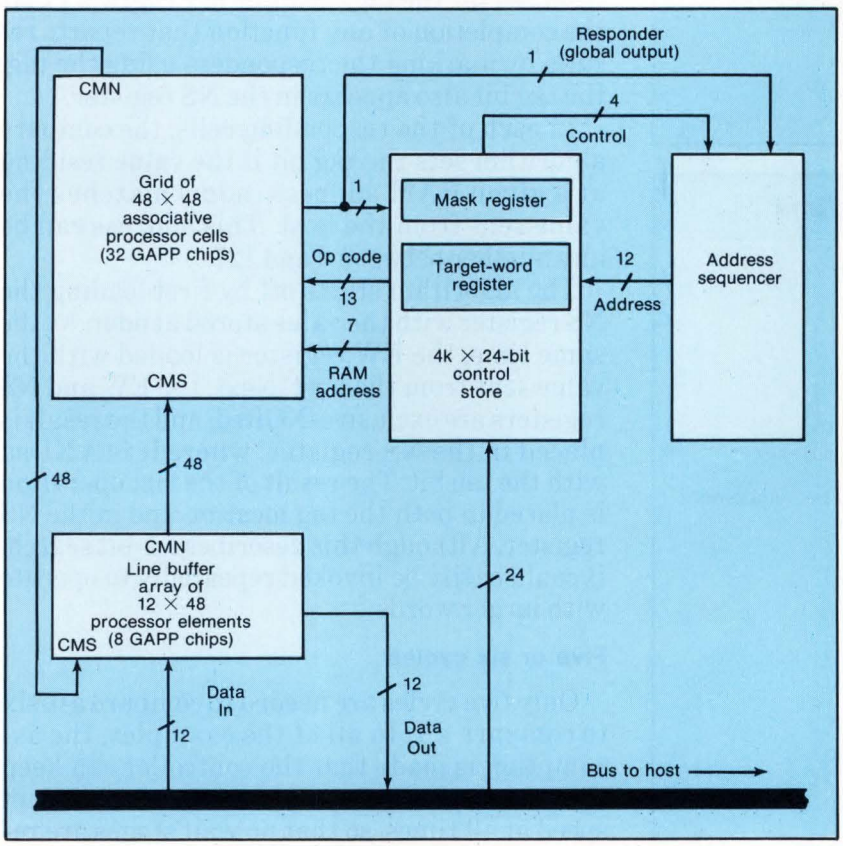
in word-serial and bit-parallel form. However, because processor elements accept only word-parallel and bit-serial data, incoming information must be reformatted. This job, often referred to as corner turning, can be implemented with GAPP devices or with special parallel-to-serial circuitry.

Doubling up

The north/south (NS) register of the chip pulls double duty, acting both as a place to store the tag bit and as an area to carry out various functions. The tags of all the processor elements can be quickly sent to the controller using the global output signal (see first article in series, ELECTRONIC DESIGN, Oct. 31, p. 207, for definition of global output). Several GAPP chips can then be combined in a wired-OR configuration to generate a responder signal for the control unit.

The control section can be set up in a number of ways, but the most effective is to use a programmable controller. Whatever route is taken, though, the controller remains responsible for generating instructions and addresses for the array and for sampling the output of the responder detection circuit. The control store receives its list of instructions from the host. Bit serial data can quickly be sent to all processor elements using the global input, which is easily accomplished by employing the op code lines to command the C register to load either a 1 or a 0.

Programming the associative processor is different from programming a conventional processor with RAM. That is due both to the different type of search involved and to the array's architecture. In operation, the instructions supplied by the control unit to the associative array are mnemonics for the chip. The control-



2. An associative memory controller (highlighted) consists of a control store, which holds commands coming from the host, and a sequencer. The sequencer can use data from responders to branch to another part of a program.

ler language in the algorithms used by the chip employs a syntax similar to that of the C language. References to the bits in the mask and target-word registers take the form of a bit number. The register's MSB is assigned a 0, and the LSB is designated M−1, where M equals the word length. The RAM associated with each processor element is similarly labeled, with the contents of the data word appearing in locations "Cell" through "Cell +M−1". Response bits are stored in additional RAM locations and are typically used by the algorithms.

Program 1. Making a comparison

```
/* Compare function */
/* Load the NS and EW Registers*/
if (value == 0)
  ew:=0, ns=ram (addr), c:=1;
else {
  c:=1;
  ew:=c, ns:=ram (addr);
}
/*EXNOR into NS reg*/

ns:=ram (temp),ram(temp):=sm;
/*AND result with TAG*/
ew:=ram(tag),c:=0, ns:=ns;
c:=cy;
/*place results in RAM and NS*/
ram(tag):=c, ns:=c;
```

Program 2. The match game

```
  /* TAG exists in NS */
  /*load tag into R*/
    c:=0, ew:=0;
    ram(R):=sm;

  /*Loop for every bit in the word*/
    for(i=0; i < M, i++){
    if(mask(i) == 1)then{

  /*Load ew and ns with the values to be compared*/
  if (comparand(i) == 0)then
    ew:=0, ns:=ram(cell+i); c:=0;
  else{
    c:=1;
    ew:=c, ns:=ram(cell+i), c:=0;
  }
  /*EXOR operands*/
  ns:=ram(temp), ram(temp):=sm;
  /*Update R bit and tag*/
  ew:=ram(R): c:=0;
  c:= cy;
  ram(R):=c, ns:=c;
  }
}
```

Time for our program

Since, as noted, a system consisting of GAPP chips is bit-serial, the most effective primitives are 1 bit wide. The bit-wide comparison primitive (Program 1) loads the comparand bit into all of the processor elements using one instruction, an important technique for parallel data input. This is accomplished by using the set 0 instruction of the East/West (EW) registers and the set 1 instruction of the C register.

The compare algorithm also makes use of a time-saving scheme concerning the tag bit. Since the NS register, which normally retains the tag bit, is needed for many other tasks, the bit is simultaneously written to a RAM location reserved for the tag (last line of Program 1). At the completion of any function that reports results by marking the responders using the tag, the tag bit also appears in the NS register.

In each of the responding cells, the compare algorithm sets the tag bit if the value residing at a given RAM address (addr) matches the value sent from the host. This address can be any number between 0 and 127.

The algorithm starts off by first loading the NS register with the value stored at addr. At the same time, the EW register is loaded with the value sent from the host. Next, the EW and NS registers are exclusive-NORed, and the result is placed in the NS register, where it is ANDed with the tag bit. The result of the last operation is placed in both the tag location and in the NS register. Although this describes a 1-bit search, it could easily be invoked repeatedly to operate with larger words.

Five or six cycles

Only five cycles are needed to compare a 0, six to compare a 1. In all of the examples, the assumption is made that the controller can keep the associative array operating at maximum speed at all times, so that no wait stages are required.

Primitives such as compare increase the power available for larger programming tasks and also simplify the programmer's chores. The

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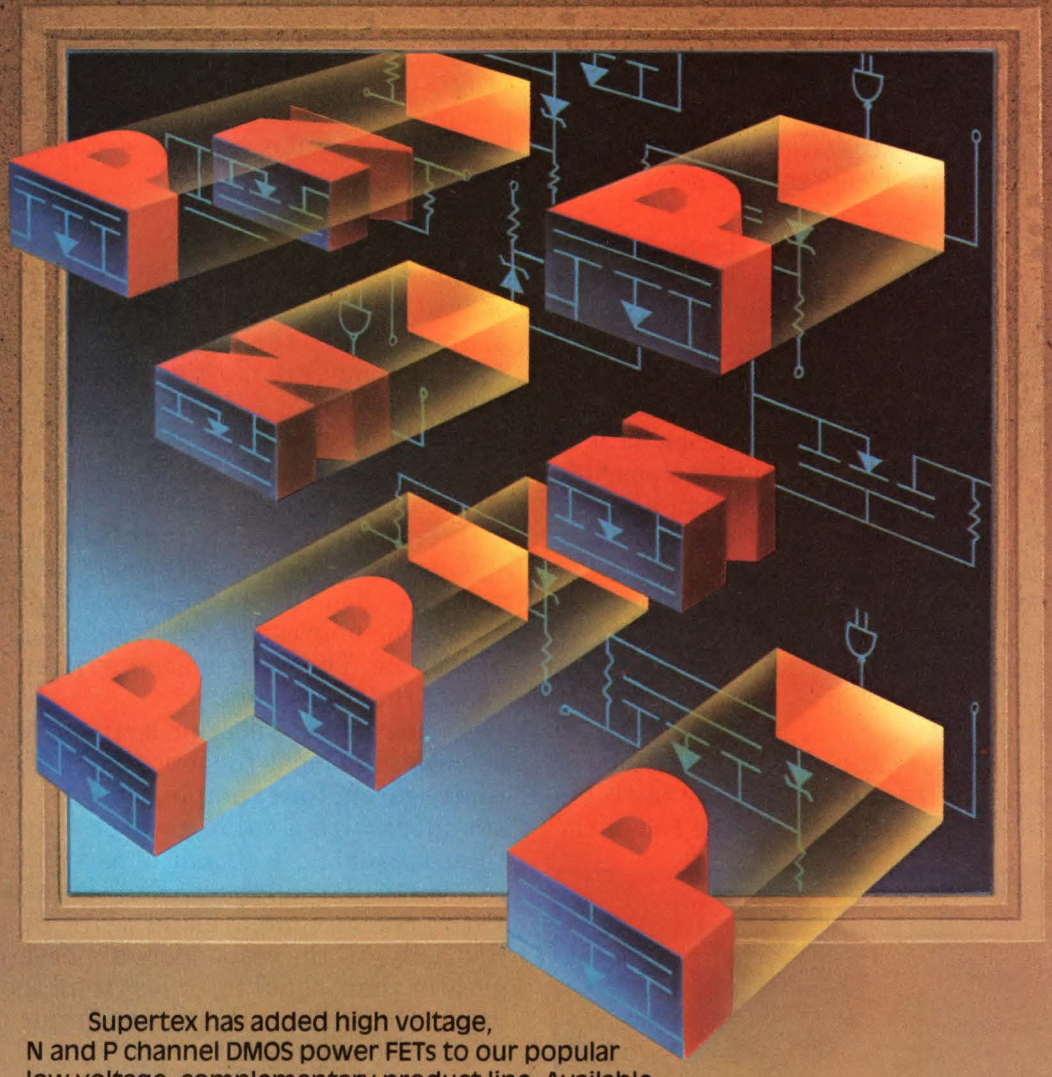

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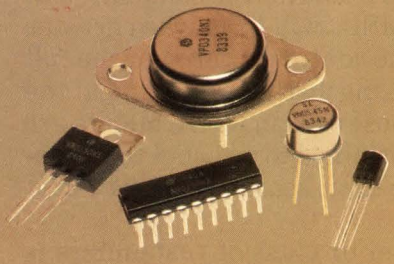

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ease of using primitives can be seen in the exact match function, which differs from the compare primitive only in that the latter emulates a bit-parallel machine by operating on a word bit by bit.

As in the foregoing example, the responders are searched for an exact match to the masked target-word register, with matches indicated by setting the tag bit. Specifically, a response bit is maintained at location R in the RAM (Program 2). If R is set, that particular cell contains a possible match to the broadcast data. If R is clear, that cell does not contain a possible match. At the end of the algorithm, all cells marked as possible matches are determined to be exact matches for the full word. This approach takes 5.5M+2 cycles, with M again representing the number of bits being compared. (This rate assumes that the number of 1s and 0s is equal.)

The write primitive is also handled with a bit-wide scheme. It, too, can be repeated for larger words. In this algorithm, the tag bit is restored to the NS register near the end of the program to ensure that multiple invocations will proceed smoothly. The restoration is combined with an OR operation, so no added cycles are demanded.

Program 3. A writing lesson

```
/* Write function */
/*Load contents of addr into ew*/
ew:=ram(addr), c:=0;
/*produce AND of not(tag),assumed to be in NS, with
contents of addr*/
c:=bw;
ram(temp):=c, c:=1;
/*load value into ew, tag assumed to be in NS*/
if(value==0)
  ew:=0, c:=0;
else
  ew:=c, c:=0;
/*AND value and tag*/
c:=cy;
/*Load intermediate values in anticipation of OR*/
ns:=c, ew:=ram(temp), c:=1;
/*perform OR and restore tag*/
c:=cy, ns:=ram(tag);
ram(addr):=c;
```

First, load the cells

The write algorithm begins by placing a Boolean value into each of the responder cells (Program 3). Since the chip treats all locations equally, some care must be taken to write only to the responders. To be sure that the nonresponding cells are not modified, the tag bit for each responder must first be inverted and then ANDed with the data in RAM.

Once this is done, the tag of the original responders is ANDed with the new value. The results are then ORed together; this effectively blocks the nonresponders from accepting the new value. The data is then written into the addr of the responders.

As mentioned, these primitives can be used as building blocks for more complex tasks. A limit search, for example, finds the set of responders with a value greater than, greater than or equal to, less than, or less than or equal to a particular number. All of this can be done with just the compare and write algorithms. Basically, all the responders are designated as greater than, equal to, or less than the desired value. Once that is done, it is simple to select any combination of sets.

Call and response

The three response bits, X, Y, and Z, all are held in RAM (Program 4). The first either indicates equality or denotes an undecided state that requires further processing. The second designates greater than, and Z signifies less than. Initially, all responding cells are set to the undecided state, or 100. If the MSB of the target number is a 1, then all the undecided elements have a 0 as their MSBs will be marked less than. If the target's MSB is a 0, all the elements that show a 1 as their MSBs will be marked greater than. This sequence continues through the full number of bits making up the target, and at the end of the word, those cells in which all bits are undecided are determined to be equal to the desired number. The limit search takes 24+29M cycles.

Once a responder or class of responders is

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identified, it is often important to interrogate the array to read its values. The most obvious way to accomplish this is to shift the contents of each cell out via the CM bus. The data words would have to be prefaced by the tag bit, so that the external circuitry can determine which of the words are responders. Obviously, this approach operates on both responders and nonresponders, but this will not matter in many applications.

Nevertheless, there are two drawbacks to this method. First, if a large array is chosen to increase throughput, the time needed to shift all the data out can be significant (see the table below). Second, the requisite external circuitry inherent to this scheme is substantial. However, in tasks like image processing, where large portions of the data are of interest, this still might be an effective technique.

Program 4. In search of limits

```
/*Mark all elements as undecided*/
WRITE(X, 1);
WRITE(Y, 0);
WRITE(Z, 0);

/*Loop through all bits*/
for(i=0;i<M,i++){
  /*Reset Tag*/
  ns=0;
  if(comparand(i) == 0){
  /*locate all undecided cells*/

  COMPARE(X, 1);
  /*locate greater than cells*/
  COMPARE(cell+i, 1);
  /*mark responders as greater than*/
  WRITE(X, 0);
  WRITE(Y, 1);
  }
  else{
  /*locate all undecided cells*/
  COMPARE(X, 1);
  /*locate less than cells*/
  COMPARE(cell+i, 0);
  /*mark responders as less than*/
  WRITE(X, 0);
  WRITE(Z, 0);
  }
}
```

Loading or reading time for a single-bit plane

Dimensions of array (processor elements)	Total number of processor elements	Total number of GAPP chips	I/O shift time (μs)
48 × 48	2304	32	4.8
132 × 132	17,424	242	13.2
516 × 516	266,256	3698	51.6
1032 × 1032	1,065,024	14,792	103.2

A question of comparison

A second approach simply employs the compare instruction to read the value of a bit using the responder signal. Comparing addr with a 0 effectively shifts the data in along with the responder signal, where it can then be shifted into the target-word register. A compare between the addr and 1 shifts the inverted data in with the responder signal. If there is more than one responder, the OR of all the data bits is positioned on the responder signal.

This method can be called into play when it is necessary, for instance, to establish the numbers of pixels that are at their maximum values. The algorithm for determining which of the words in memory has the highest value uses the responders first as decision-making data and then to read the maximum value. The first two steps of the following algorithm effectively amounts to an instruction that sets all the tag bits:

```
for (i=0;i<M, i++){
/*search for undecided cells*/
SET;
COMPARE(R,1);
COMPARE((CELL+i), 1);
if (RESPONDER)
    WRITEN(R,0);
}
```

The program first scans all the memory cells, looking at the most significant bits. If any cell has a 1 in that position, it is noted that it holds the highest value. All the cells with 0s are marked as storing less than highest. When the bits are all processed, the cells containing the highest value at each bit are determined to contain the maximum word value. This will take 14 cycles for each bit of the data.

Cutting down on overhead

The program uses the compare algorithm whether or not the data is to be read out. It is possible, though, to read the contents of a cell without incurring the overhead associated with the exclusive-OR used in a comparison. The

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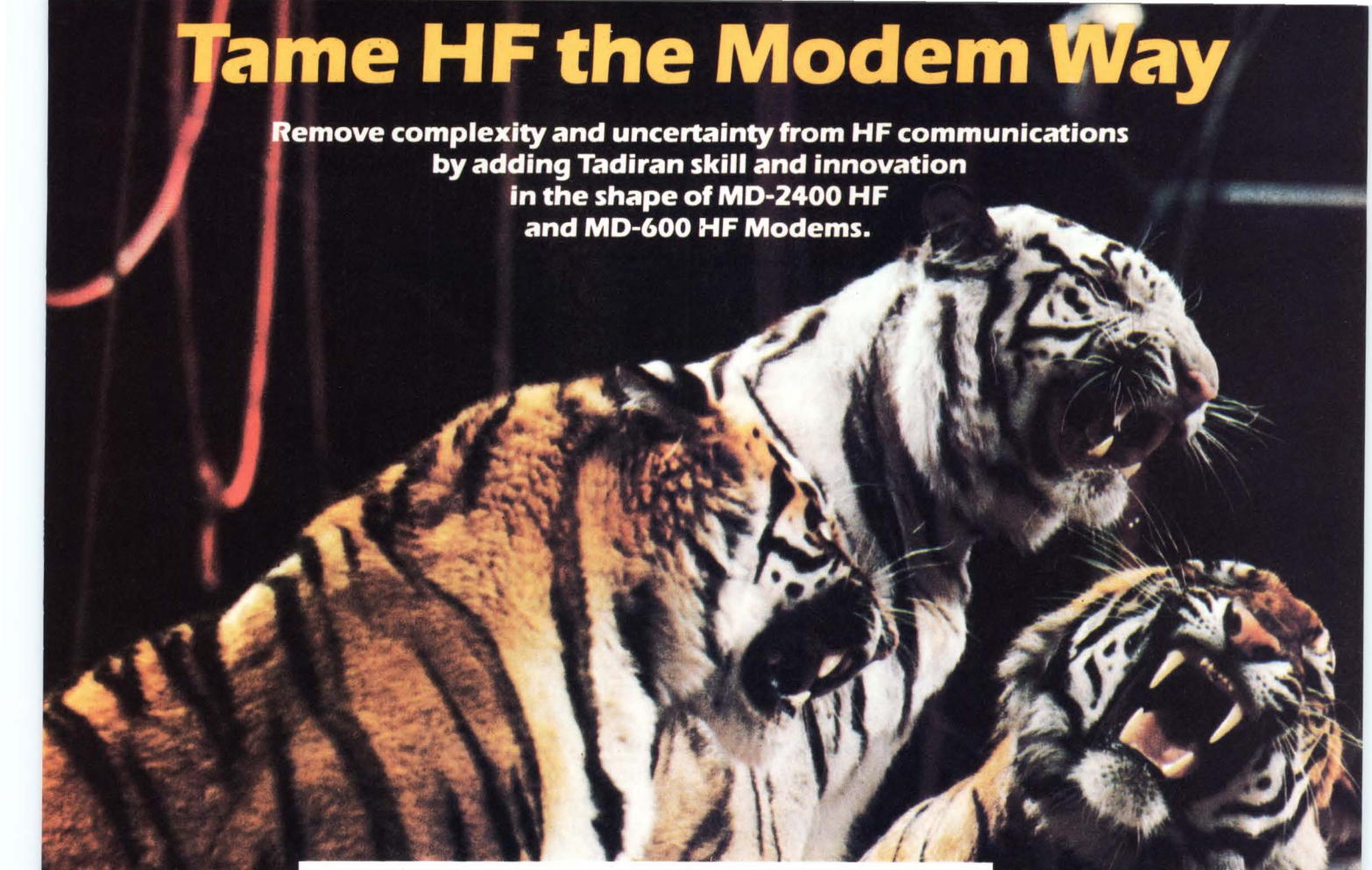

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third read does just that, employing the responder signal supplied by the associative array to read the value of the responding cells. Doing so places the data in the responding cells at addr in the NS register. The routine:

```
/*Load ns with TAG*/
ns:=ram(tag);
/*Load ew with data*/
ew:=ram(addr), c:=0;
/*AND tag and data*/
c:=cy;
/*Place results in NS*/
ns:=c;
```

makes good use of the fact that the tag bit is stored in memory, so it can be used consecutively a number of times. The read is called up by logically ANDing the tag at ram (tag) with the data at addr and then placing the results in the NS register.

A read of this type would be desirable whenever it is necessary to address portions of the array individually at a unique address—as with a conventional memory—instead of by the content of memory. This is done by loading the data words over the CM bus so that each elements holds a unique number in its RAM. An exact match search (using either primitives or the larger program) could then be executed and the cell contents read. On a grid of systolic arrays 516 elements on a side, the exact match would take a maximum of 114 cycles and the read would take 4 × M cycles.

Easing into associative processing

Once an associative memory has been built from GAPP chips, it is relatively simple to enhance it to create an associative processor. The primitives and techniques detailed permit a full range of searches, which can be combined with arithmetic or logical operations to further increase the system's capabilities.

As simple as it sounds, one of the functions most useful to associative memories is counting, or simply summing the number of responders. Its importance can be seen in a limit search, in which it might be vital to know how many bits fall within a set of limits. Doing so relies on the chip's ability to perform serial arithmetic, keeping track of the number of cells that have the tag bits set.

A related function, called first, lets users process the bits on an individual basis. Once it is determined that there are multiple responders, it becomes important to turn off all but the desired one, so that the others are not altered when the operation takes place.

One technique is to propagate a marker in the northwest corner cell of the array and carry it eastward along the top row until the eastern edge of the array is reached. It can then drop down a row and move in the opposite direction, continuing with its serpentine route across the full array. Since the marker resides in only one cell at a time, only that cell is on, so it is the only one being addressed at any given time. Sampling the responder after each shift of the marker makes it possible to know when the first responder has been reached. Another technique would be to prioritize multiple responders with the unique PE address.

A final algorithm takes advantage of some of the processor element's logical functions to calculate the number of bit positions by which the corresponding digits in each cell differ from those of the desired value. This number, or Hamming distance, forms the basis of numerous error correction codes. The algorithm:

```
/*Store Zero in COUNT field of all Candidates*/
for (i=0,i<M;i++)
    WRITE(COUNT+i, 0);
/*Compare all bits*/
for(i=0;i<M;i++){
    SET;
    COMPARE(CELL+i,COMPARAND(i));
    ADDONE;
}
```

is effectively a search for no match, which is followed by incrementing a count field in all responders. Once the Hamming distance is determined for each word in the associative array, a least-value search can be performed on the count field to find the word with the smallest distance. Every time no match is found, the counter is incremented by one.□

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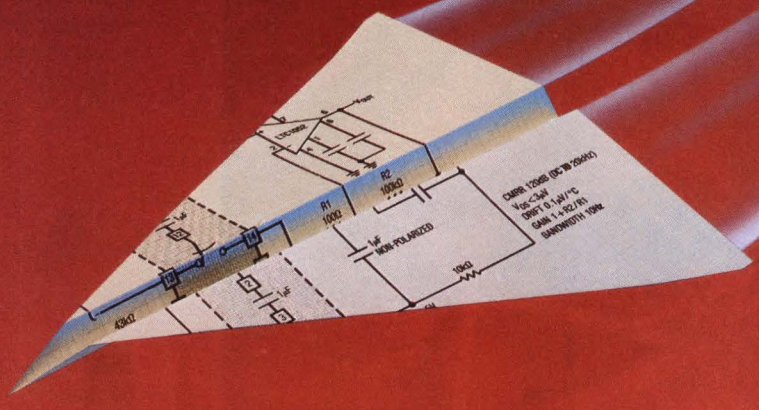

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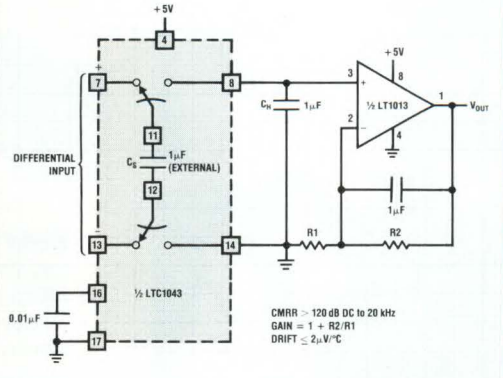

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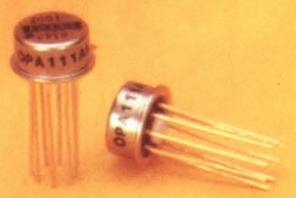

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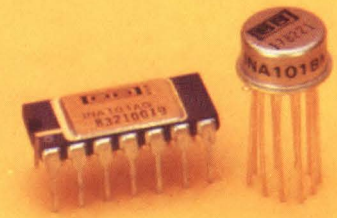
- Low offset voltage/drift... 250μV max, 1μV/°C max

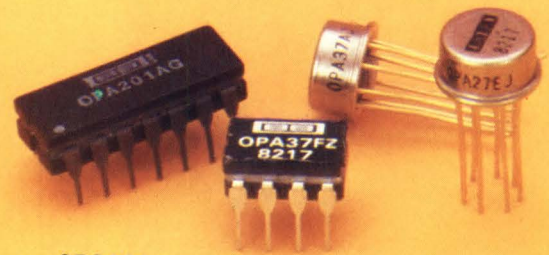
Circle reader service no. 100



INA101: A high accuracy monolithic instrumentation amplifier.

- Low offset voltage/drift..25μV max, 0.25μV/°C max
- Low nonlinearity..... 0.002% max
- Gain range ..... 1 to 1000V/V

Circle reader service no. 101



OPA201: Innovative low power monolithic op amp has two separate precision input stages (selected by TTL signal). Use in synchronous detector designs and for simplified autozeroing systems. A new extremely versatile, circuit "building block."

- Offset voltage/drift ..... 100μV max, 1μV/°C max
- Bias current ..... 25nA max

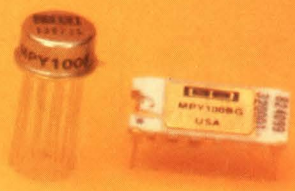
Circle reader service no. 102

OPA27/37: Precision grade op amps offering ultra-low noise. For transducer and pre-amp applications.

- Low noise ..... 2.7nV/$\sqrt{Hz}$ at 1kHz
  0.07μV, p-p, 0.1 to 10Hz
- Low offset voltage/drift.. 25μV max, 0.6μV/°C max
- High speed 1.9V/μsec (OPA27),
  11.9V/μsec (OPA37)

Circle reader service no. 103

To Condition



MPY100: Precision monolithic analog circuit performs four-quadrant multiplication, division, square root, and squaring.

- Multiplier error ..... 0.5% max
- Available in TO-100 and 14-pin DIP

Circle reader service no. 108

4302: Multifunction converter can multiply, divide, square, exponentiate, root, sine, cosine, $\tan^{-1}$, etc. mathematical functions accurately.

- Versatile ..... $E_O = V_Y(V_Z/V_X)^m$
- Small size ..... 14-pin DIP

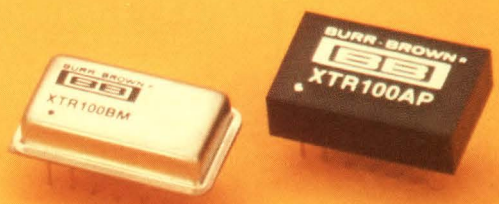
Circle reader service no. 109

DIV100: This analog divider is 100% tested over its full 40:1 denominator range.

- Low error ..... 0.25% max

Circle reader service no. 110

To Transmit

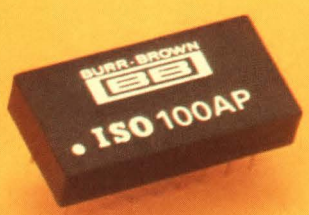


XTR100: 4-20mA two-wire current transmitter includes matched tracking current source to provide bridge excitation. Small enough to mount in thermocouple well.

- Instrumentation amplifier input:
  Low offset voltage/drift.. 25μV max, 0.5μV/°C max
  Nonlinearity ..... 0.01% max
- Wide supply range ..... +11.6V to +40V

Circle reader service no. 106

To Isolate



ISO100: Optically coupled monolithic isolation amplifier offers low drift, wide bandwidth and achieves isolation at lowest cost per channel available.

- Nonlinearity ..... 0.07% max
- Input offset voltage/drift.. 200μV max, 1μV/°C max
- Continuous isolation ..... 750VDC min
- Isolation test 2500VDC

Circle reader service no. 104

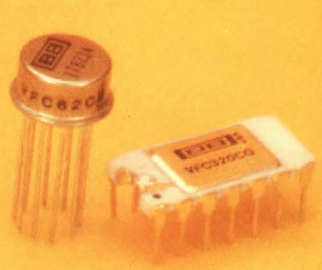
3656: Both signal and power isolation are provided by this 1" by 1" by 1/4" IC package.

Innovative transformer coupling has 3-port isolation.

- Isolation test ..... 8000VDC min
- Continuous isolation ..... 3500VDC min
- Leakage ..... 0.5μA max at 120V, 60Hz
- Isolation mode rejection ..... 125dB at 60Hz

Circle reader service no. 105

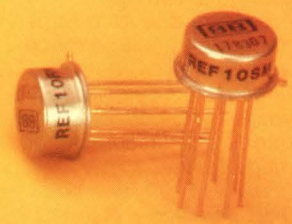
To Convert



VFC320/VFC62: High linearity—monolithic V-to-F converter; operates to 1MHz.

- 12 to 14 bit linearity
- Open collector output/active pull-up.
- 20ppm/°C max gain drift

Circle reader service no. 107



REF10: High stability +10V reference is fully specified over its complete temperature range.

- Low drift ..... 1ppm/°C max
- Very low noise ..... 6μV p-p

Circle reader service no. 111

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A/D and D/A converters, sample/ hold, power amplifiers, rms-to-DC converters, peak detectors, oscillators, and filters that give you solutions to your signal conditioning design problems.

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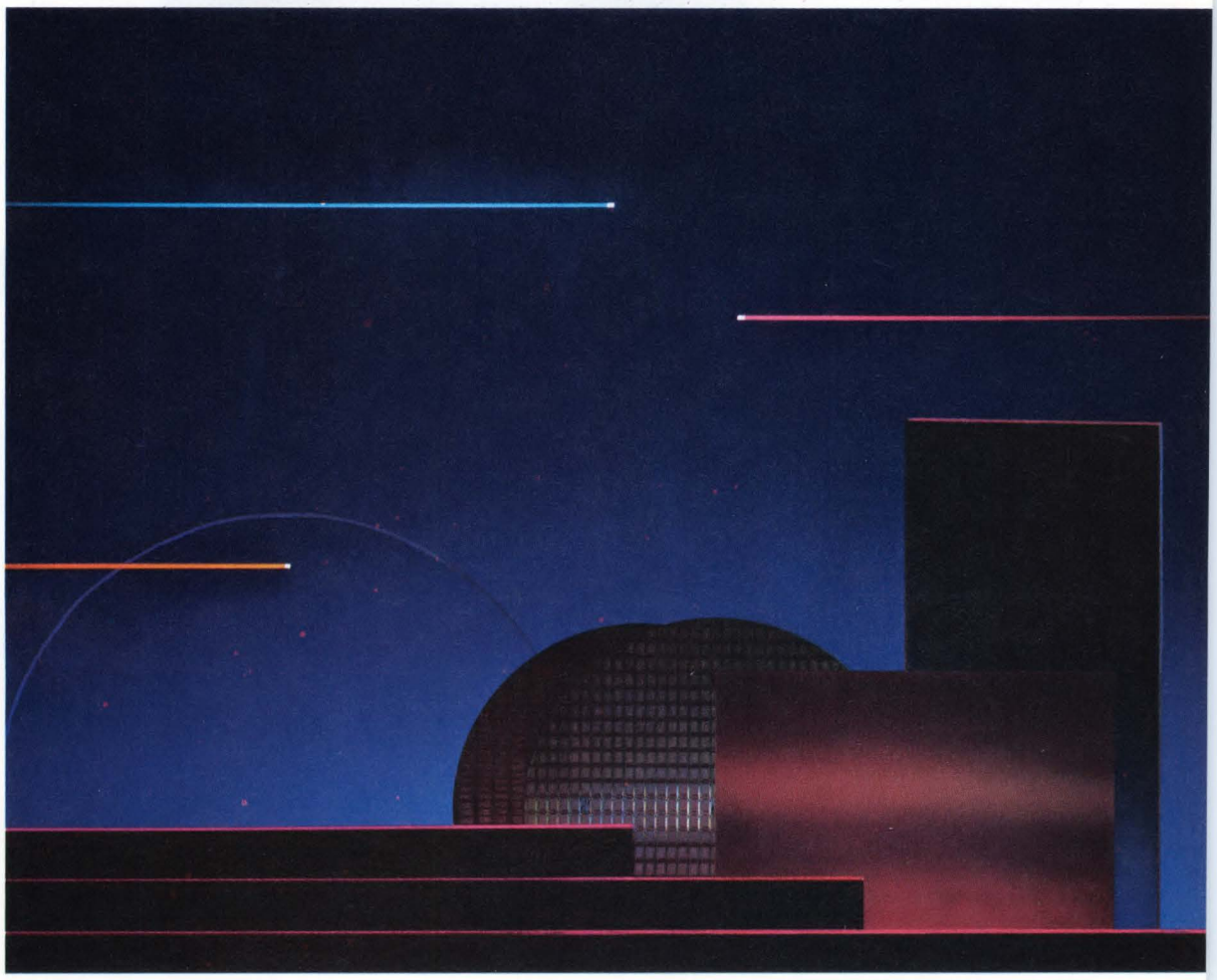
CIRCLE 112



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SYSTEMS

CIRCLE 113

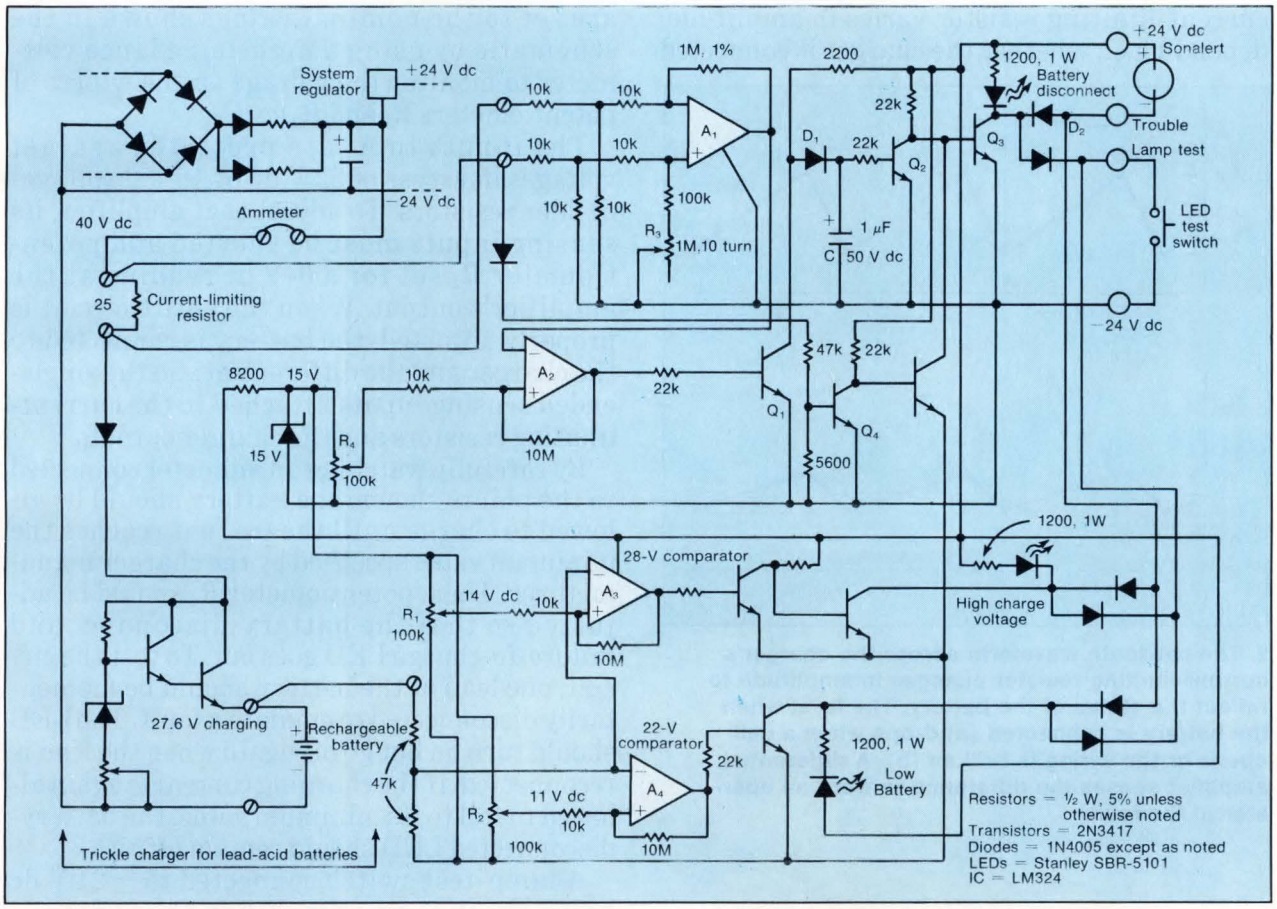
DESIGN SOLUTION

Add-on circuit monitors trickle-charging system

Kenneth J. Ciszewski
Design Engineer
1929 Hurstgreen St.
Overland, Mo. 63114

Sealed lead-acid batteries, especially those employed in standby power systems, are too expensive and important to be supervised by a simple trickle charger. A circuit that keeps tabs on both the battery and the charging system is a simple form of insurance against the loss of power and data due to an undercharged battery.

The circuit (Fig. 1) checks the charging system for a high-voltage condition, which would indicate an improper charger setting or the failure of the pass transistor. It also sets off an alarm if a low voltage is detected or if the battery fails to charge. The latter would suggest that the battery is disconnected, its wiring or



1. When added to a commercial trickle charger, this circuit monitors the condition of both the battery and the charger, keeping the user apprised of any faults.

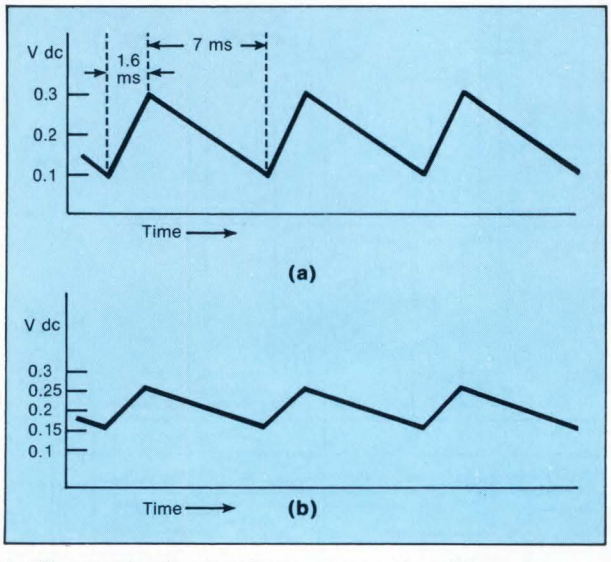
terminals broken, or that it possibly has an open cell.

An operational amplifier, the LM334, forms the core of the circuit's three basic sections. These consist of a differential amplifier, A_1, whose output is fed to comparator A_2, plus a separate window comparator made up of A_3 and A_4.

As long as the voltage output of the charger is between preset limits (here 22 and 28 V dc), no fault is indicated. If the voltage drops too low or goes too high, the appropriate LED lights. A common pull-down signal also is supplied for linking to an audible alarm, such as a Sonalert.

The voltage input to the comparator is halved by a voltage divider consisting of two 47-k Ω resistors. Consequently, the window comparator's voltage references are simply set to one-half of the desired high and low limits (in this case, 14 and 11 V).

The voltage waveform across the charger's current-limiting resistor varies in amplitude, depending on whether the charger is connected to the battery or not (Fig. 2). First, A_1 senses the voltage, and A_2 then compares A_1's output with a fixed reference that is set by a 15-V zener diode and a 100-k Ω potentiometer. When the peak value of the charger's sawtooth waveform exceeds the reference, A_2 charges capacitor C through transistor Q_1 and diode D_1. That, in turn, drives transistor Q_2, keeping transistor Q_3 turned off.



2. The sawtooth waveform across the charger's current-limiting resistor changes in amplitude to reflect the status of the battery. The level when the battery is connected (a) drops when a cell opens or the wiring is broken (b). A differential amplifier senses the difference to warn an operator of the fault.

If the battery fails to draw sufficient charging current, the comparator no longer charges the capacitor and Q_3 both turns on a fault LED and furnishes a common fault signal, through diode D_2, to the alarm. Transistor Q_4 inhibits the fault signal when no voltage is applied to the positive sensing input of the differential amplifier. That saves standby power when the battery is not being charged because of a power outage.

The window comparators' voltage references are set to the nominal values shown in the schematic by using a high-impedance voltmeter to monitor the voltage on the wipers of potentiometers R_1 and R_2.

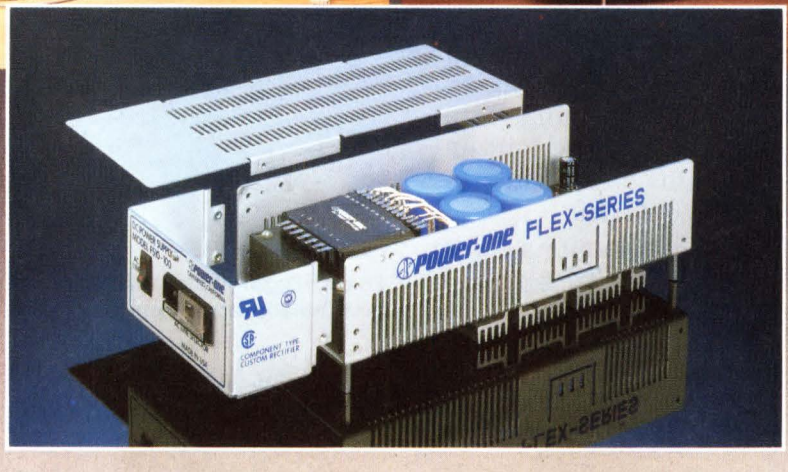
The inputs to A_1 are protected against voltages in excess of 32 V dc by 10-k Ω voltage-divider resistors. To adjust that amplifier, its sensing inputs must be shorted and potentiometer R_3 set for a 0-V dc reading at the amplifier's output. When the entire circuit is properly adjusted, the battery is connected to the charger and the differential and the single-ended sensing inputs attached to the current-limiting resistors and the charger outputs.

By carefully watching an ammeter connected to the points shown, the battery should be allowed to charge until the current reaches the minimum value specified by the charger manufacturer. Then, potentiometer R_4 should be adjusted so that the battery-disconnect and failure-to-charge LED goes out. To test the circuit, one lead of the battery should be momentarily disconnected to emulate a fault. The LED should turn on but go off again when the lead is reconnected. If the charging current is again allowed to fall to its minimum value, the battery-disconnected LED should remain off.

A lamp-test switch connected to −24 V dc helps check the LEDs. When the switch is pressed, all the LEDs should turn on and the alarm should sound.

BRAND-X *or* POWER-ONE FLEX?

"An Unfair Comparison"



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CIRCLE 114

Gate and instruction place nonmaskable interrupt under software control

Vittal Rao
Engineer
Digital Systems Section
ISRO Satellite Centre
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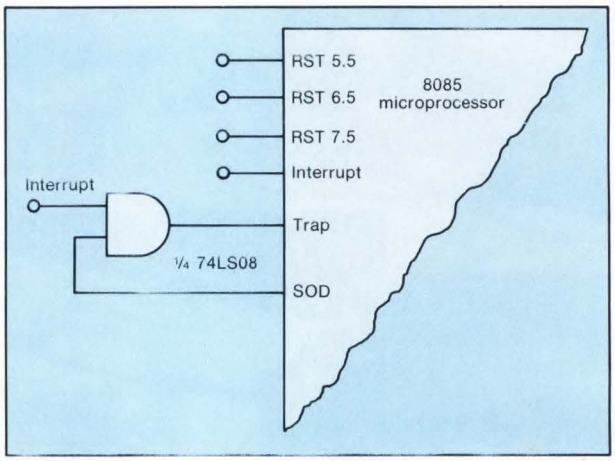
Bangalore: 560 017 India

If an application needs one more interrupt than is normally provided by an 8085 processor, the expense of an 8259 programmable interrupt controller may be unwarranted and unnecessary. A AND gate plus one of the processor's instructions can do the trick.

Most microprocessors have a nonmaskable interrupt, called Trap on the 8085. That pin cannot be masked by the designer but the simple AND-gate circuit (see the figure) places it under software control.

The gate's inputs connect to the external device and the processor's serial output data (SOD) line. The output goes to the Trap pin. By executing the Set Input Mask (SIM) instruction, the interrupt can be alternately enabled or disabled. If an interrupt occurs, the processor can branch to the NMI vector—24_{16}.



The AND gate helps place the 8085 processor's nonmaskable interrupt pin under software control.

Routines extend 8051 math—to negative numbers

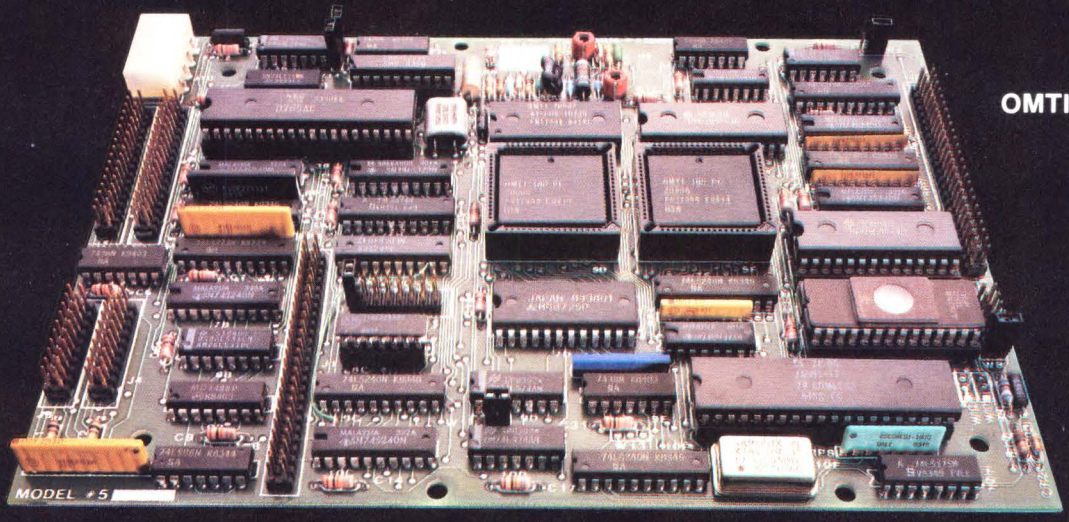
Israel Yuval
Electrical Engineer
ADA (Israel)
PO Box 2250, Haifa, Israel

Two routines extend the Multiply (MUL) and Divide (DIV) instructions of the 8051 microprocessor to signed numbers. In the routines, negative values are represented by their two's complement.

As defined by Intel, a MUL AB instruction multiplies an unsigned 8-bit integer in the accumulator by the contents of register B. The low-order byte of the 16-bit product is left in the accumulator and the high-order byte in B.

DIV AB divides the unsigned 8-bit integer in the accumulator by the integer in register B. The accumulator receives the integer part of

WINCHESTER, FLOPPY AND TAPE
All on one board



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Winchester

OMTI 5300
Winchester
plus Tape

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Our OMTI Series 5000 family of SCSI (SASI) controllers supports industry standard ST506/412 5¼" fixed and removeable Winchester disks, 5¼" and 8" floppy disks and QIC-02 compatible streaming tape. Each controller is SCSI (SASI) compatible to protect your software from change as you add next generation disk and tape technologies. And they are all second-sourced to guarantee availability.

HIGH PERFORMANCE
The Series 5000 controllers provide consecutive sector, non-interleaved data transfer and multisector buffering between host and peripherals. In addition, our data buffer supports simultaneous transfers between Winchester and streaming tape for fast image backup operation. No other manufacturer offers you performance like this!

EASY TO USE
Our high-level SCSI (SASI) command set off-loads your host CPU. Only one command is required to completely backup or restore Winchester data to and from tape, all without host intervention. Separate host-initiated commands allow selective file backup and restore. A sophisticated 32-bit ECC and automatic error retry means that reliable data is always available to the host. Finally, automatic Winchester flaw management handling prevents disk defects from corrupting your system.

To learn more about the OMTI Series 5000 data controllers, please contact us for additional information.

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CIRCLE 115

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Program 1. Routine MULT for multiplying negative numbers

```
LOC  OBJ           LINE     SOURCE

                      1     ;THIS PROGRAM MULTIPLIES CONTENTS OF ON-CHIP RAM ADDRESSES MUL1 AND MUL2
                      2     ;(8 BIT EACH). PROVIDED THAT NEGATIVE VALUES ARE REPRESENTED BY THEIR 2'S
                      3     ;COMPLEMENT. A TRUE FOUR QUADRANT MULTIPLICATION IS EXECUTED. RESULT (16
                      4     ;BITS) IS SENT TO PORTS A (M.S.BYTE) AND B (L.S.BYTE) OF AN I/O DEVICE, WITH
                      5     ;NEGATIVE VALUES REPRESENTED BY THEIR 16 BIT 2'S COMPLEMENT.
                      6
                      7
0000 E57A             8     MULT:   MOV     A,MUL1
0002 C3               9             CLR     C
                     10
0003 A2E7            11             MOV     C,ACC.7         ;TEST FOR POLARITY OF 1ST MULTIPLIER.
                     12
0005 5003            13             JNC     A1              ;(MUL1) IS POSITIVE.
                     14
0007 F4              15             CPL     A               ;(MUL1) IS NEGATIVE. FIND ITS 2'S
0008 2401            16             ADD     A,#1            ;COMPLEMENT.
                     17
000A F5F0            18     A1:     MOV     B,A
000C E57B            19             MOV     A,MUL2
000E C3              20             CLR     C
000F A2E7            21             MOV     C,ACC.7         ;REPEAT POLARITY TEST FOR 2ND MULTIPLIER.
                     22
0011 5003            23             JNC     A2
0013 F4              24             CPL     A
0014 2401            25             ADD     A,#1
                     26
0016 F57C            27     A2:     MOV     TEMP1,A         ;SAVE ACCUMULATOR.
                     28
0018 E57B            29             MOV     A,MUL2          ;AFTER EXCLUSIVELY ORING (MUL1) AND (MUL2),
001A 657A            30             XRL     A,MUL1          ;ACC.7 WILL INDICATE PRODUCT POLARITY.
                     31
001C A2E7            32             MOV     C,ACC.7
001E 9220            33             MOV     SIGN1,C         ;SAVE PRODUCT SIGN (CARRY BIT IS ALWAYS
                     34                                     ;CLEARED FOLLOWING MUL AB INSTRUCTION).
                     35
0020 E57C            36             MOV     A,TEMP1
0022 A4              37             MUL     AB
0023 A220            38             MOV     C,SIGN1
                     39
0025 500A            40             JNC     A3              ;BOTH MULTIPLIERS ARE EITHER NEGATIVE OR
                     41                                     ;POSITIVE. PRODUCT IS POSITIVE.
                     42
0027 F4              43             CPL     A               ;ONLY ONE MULTIPLIER IS NEGATIVE. HENCE
0028 2401            44             ADD     A,#1            ;PRODUCT IS NEGATIVE AND MUST BE REPRESENTED
                     45
002A C5F0            46             XCH     A,B             ;BY ITS 16 BIT 2'S COMPLEMENT.
002C F4              47             CPL     A
002D 3400            48             ADDC    A,#0
002F C5F0            49             XCH     A,B
                     50
0031 906502          51     A3:     MOV     DPTR,#PORTB     ;TRANSFER LOWER BYTE OF RESULT TO PORT B OF
0034 F0              52             MOVX    @DPTR,A         ;OUTPUT DEVICE.
0035 C5F0            53             XCH     A,B
0037 906501          54             MOV     DPTR,#PORTA     ;HIGHER BYTE TO PORT A.
003A F0              55             MOVX    @DPTR,A
                     56
003B 80FE            57     HALT1:  SJMP    HALT1
                     58
  007A               59     MUL1    DATA    7AH
  007B               60     MUL2    DATA    7BH
  007C               61     TEMP1   DATA    7CH
                     62
  0020               63     SIGN1   BIT     20H
                     64
  6501               65     PORTA   EQU     6501H
  6502               66     PORTB   EQU     6502H
                     67
                     68     END

XREF SYMBOL TABLE LISTING
---- ------ ----- -------

NAME    TYPE     VALUE AND REFERENCES

A1. .   L CSEG   000AH  13 18#
A2. .   L CSEG   0016H  23 27#
A3. .   L CSEG   0031H  40 51#
ACC .   N DSEG   00E0H  11 21 32
B . .   N DSEG   00F0H  18 46 49 53
HALT1   L CSEG   003BH  57# 57
MUL1.   N DSEG   007AH  8 30 59#
MUL2.   N DSEG   007BH  19 29 60#
MULT.   L CSEG   0000H  8#
PORTA   N        6501H  54 65#
PORTB   N        6502H  51 66#
SIGN1   N BSEG   0020H  33 38 63#
TEMP1   N DSEG   007CH  27 36 61#
```

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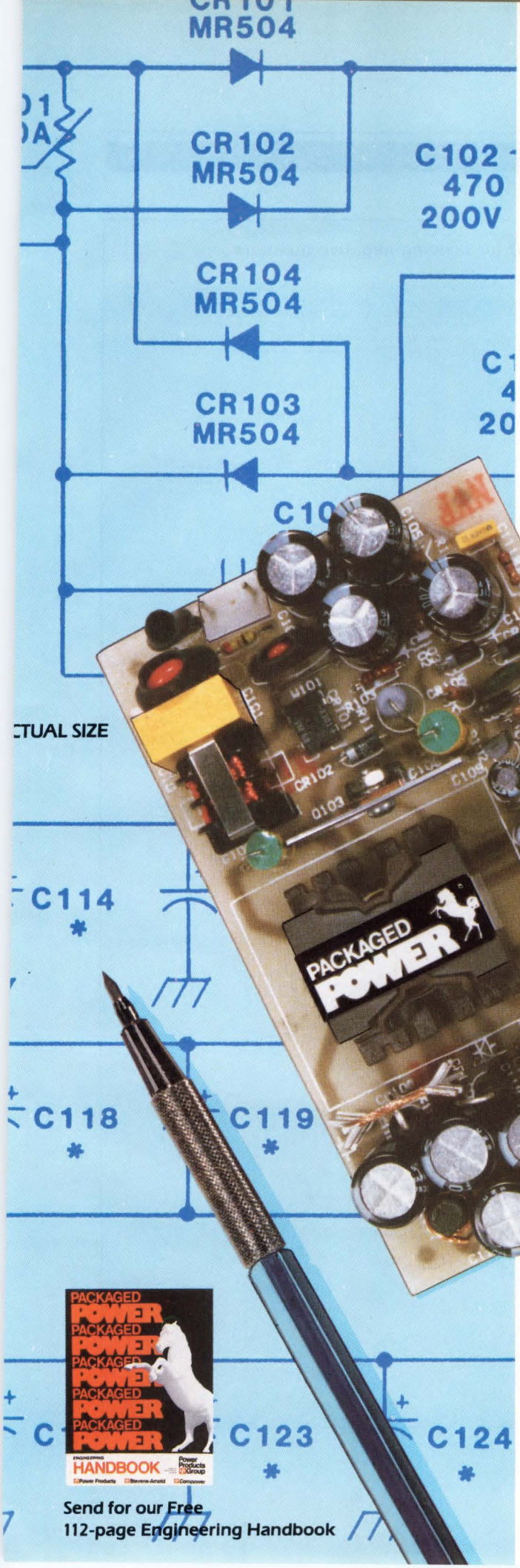

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CIRCLE 138

Program 2. Routine DVD for dividing negative numbers

```
LOC  OBJ           LINE     SOURCE

                      1     ;PROGRAM DIVIDES CONTENTS OF ON-CHIP RAM ADDRESS DIV1 BY THE CONTENTS OF
                      2     ;DIV2 (8 BITS EACH). PROVIDED THAT NEGATIVE VALUES ARE REPRESENTED BY
                      3     ;THEIR 2'S COMPLEMENT, A TRUE ALGEBRAIC DIVISION IS EXECUTED. QUOTIENT AND
                      4     ;REMAINDER (8 BITS EACH) ARE SENT TO PORTS A AND B, RESPECTIVELY, OF AN I/O
                      5     ;DEVICE, WITH NEGATIVE VALUES REPRESENTED BY THEIR 2'S COMPLEMENT.
                      6
                      7
0000 E57E             8     DVD:    MOV     A,DIV2
0002 C3               9             CLR     C
                     10
0003 A2E7            11             MOV     C,ACC.7         ;TEST FOR DIVIDE  POLARITY.
                     12
0005 5003            13             JNC     B1              ;(DIV2) IS POSITIVE.
                     14
0007 F4              15             CPL     A               ;(DIV2) IS NEGATIVE. FIND ITS 2'S COMPLEMENT.
0008 2401            16             ADD     A,#1
                     17
000A F5F0            18     B1:     MOV     B,A
000C E57D            19             MOV     A,DIV1
000E C3              20             CLR     C
000F A2E7            21             MOV     C,ACC.7         ;REPEAT POLARITY TEST FOR (DIV1).
0011 9221            22             MOV     SIGN2,C         ;SAVE DIVIDEND SIGN.
                     23
0013 5003            24             JNC     B2
                     25
0015 F4              26             CPL     A
0016 2401            27             ADD     A,#1
                     28
0018 F57F            29     B2:     MOV     TEMP2,A         ;SAVE ACCUMULATOR.
                     30
001A E57E            31             MOV     A,DIV2          ;AFTER EXCLUSIVELY ORING (DIV1) AND (DIV2),
001C 657D            32             XRL     A,DIV1          ;ACC.7 WILL INDICATE QUOTIENT POLARITY.
                     33
001E A2E7            34             MOV     C,ACC.7
0020 9222            35             MOV     SIGN3,C         ;SAVE QUOTIENT SIGN (CARRY BIT IS ALWAYS
                     36                                     ;CLEARED FOLLOWING A DIV AB INSTRUCTION).
0022 E57F            37             MOV     A,TEMP2
0024 84              38             DIV     AB
0025 A222            39             MOV     C,SIGN3
                     40
0027 5003            41             JNC     B3              ;BOTH DIVIDEND AND DIVIDER ARE EITHER
                     42                                     ;NEGATIVE OR POSITIVE.QUOTIENT IS POSITIVE.
                     43
0029 F4              44             CPL     A               ;EITHER DIVIDEND OR DIVIDER IS NEGATIVE.
002A 2401            45             ADD     A,#1            ;QUOTIENT MUST BE REPRESENTED BY ITS 2'S
                     46                                     ;COMPLEMENT.
                     47
002C A221            48     B3:     MOV     C,SIGN2         ;REMAINDER SIGN IS EQUAL TO THAT OF THE
002E 5002            49             JNC     B4              ;DIVIDEND.
0030 C5F0            50             XCH     A,B
0032 F4              51             CPL     A
0033 2401            52             ADD     A,#1
0035 C5F0            53             XCH     A,B
                     54
0037 906501          55     B4:     MOV     DPTR,#PORTA     ;TRANSFER QUOTIENT TO PORT A OF OUTPUT DEVICE.
003A F0              56             MOVX    @DPTR,A
003B C5F0            57             XCH     A,B
003D 906502          58             MOV     DPTR,#PORTB
0040 F0              59             MOVX    @DPTR,A         ;TRANSFER REMAINDER TO PORT B.
                     60
0041 80FE            61     HALT2:  SJMP    HALT2
                     62
                     63
  007D               64     DIV1    DATA    7DH
  007E               65     DIV2    DATA    7EH
  007F               66     TEMP2   DATA    7FH
                     67
  0021               68     SIGN2   BIT     21H
  0022               69     SIGN3   BIT     22H
                     70
  6501               71     PORTA   EQU     6501H
  6502               72     PORTB   EQU     6502H
                     73
                     74     END

XREF SYMBOL TABLE LISTING
---- ------ ----- --------

NAME    TYPE     VALUE AND REFERENCES
ACC . . N DSEG   00E0H  11 21 34
B . . . N DSEG   00F0H  18 50 53 57
B1. . . L CSEG   000AH  13 18#
B2. . . L CSEG   0018H  24 29#
B3. . . L CSEG   002CH  41 48#
B4. . . L CSEG   0037H  49 55#
DIV1. . N DSEG   007DH  19 32 64#
DIV2. . N DSEG   007EH  8 31 65#
DVD . . L CSEG   0000H  8#
HALT2 . L CSEG   0041H  61# 61
PORTA . N        6501H  55 71#
PORTB . N        6502H  58 72#
SIGN2 . N BSEG   0021H  22 48 68#
SIGN3 . N BSEG   0022H  35 39 69#
TEMP2 . N DSEG   007FH  29 37 66#
```

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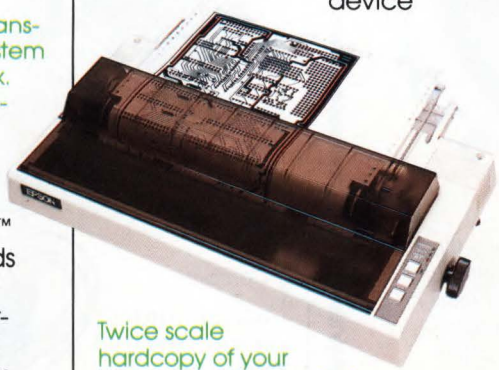

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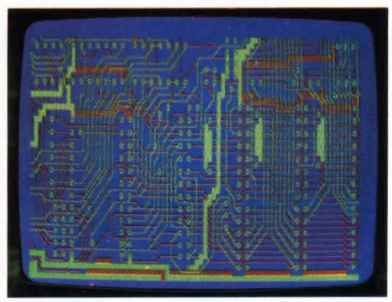

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- ☐ Houston Instrument DMP-41 pen-and-ink plotter (optional)
- ☐ Microsoft Mouse (optional)

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CIRCLE 117

the quotient, and register B receives the remainder.

The 8051 assembler represents negative numbers by their 8-bit two's complement. For example, −3 is represented in hexadecimal by FD; −100 would be shown as 9C. Negative and positive values can be distinguished by their most significant bit. The MSB for negative numbers, those ranging from −1 to −128 in the 8-bit two's complement representation, will be 1. For positive numbers that range from 0 to 127, the MSB will be 0.

The routine called MULT (Program 1) tests for the polarity of each multiplier, converts negative values into their two's complements, and then performs the multiplication. The result is the product of the absolute values of the two multipliers. The sign of the product is determined by exclusive-ORing the two original multipliers and checking the MSB of the result. A logic 1, for example, indicates that the product is a negative number.

If the product is indeed negative, its 16-bit two's complement value is calculated and the final result sent to an I/O device, such as an 8155 programmable I/O port device.

The routine DVD (Program 2) is quite similar to MULT except that the result consists of an 8-bit integer quotient and an 8-bit remainder. Each is represented by a two's complement if it is a negative value. The sign of the remainder will always be the same as that of the dividend.

Winner for October 31, 1984

Simple program finds parts values for phase-locked loop

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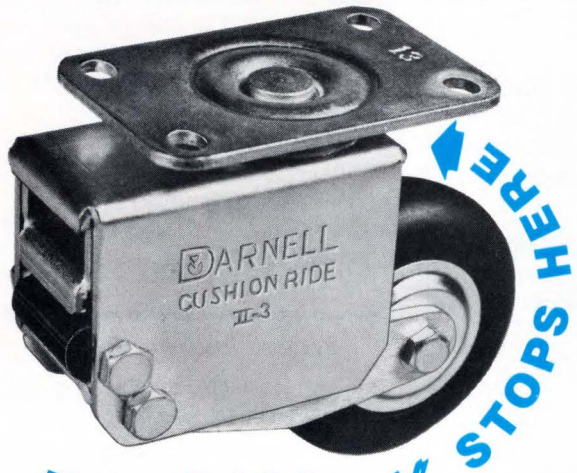

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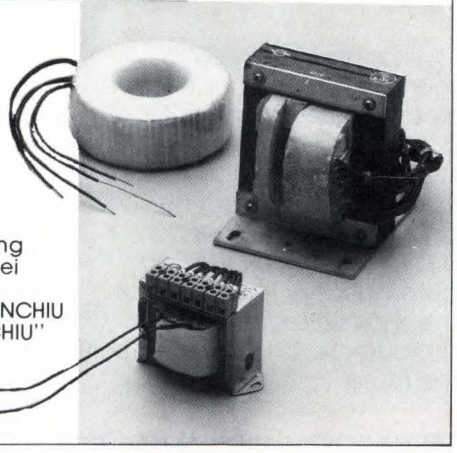

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CIRCLE 119

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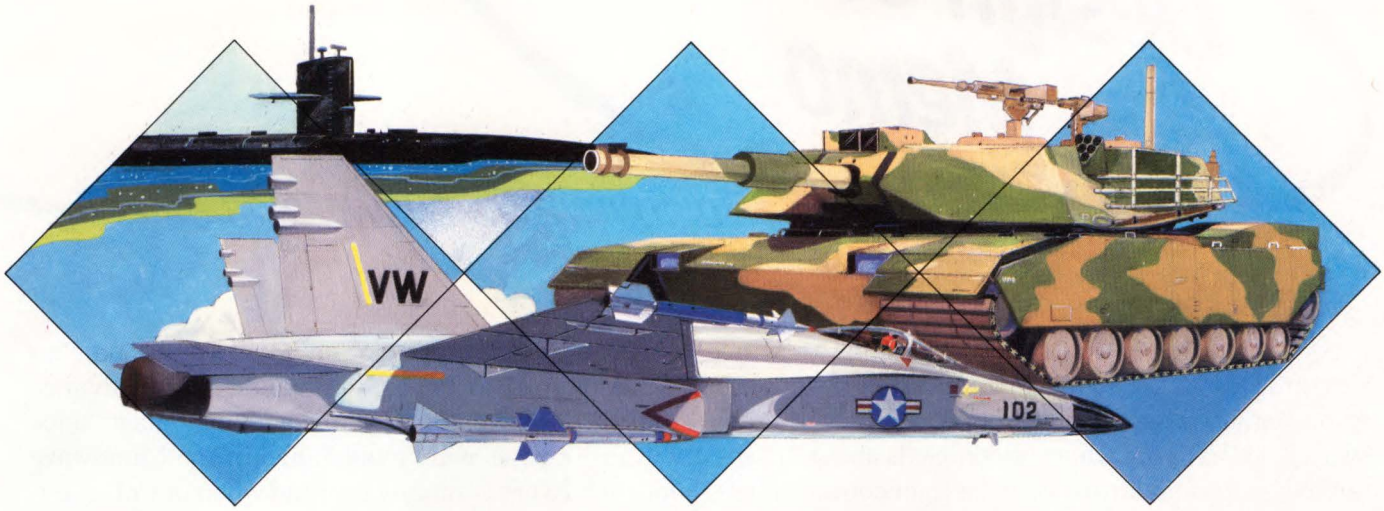

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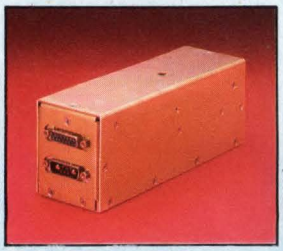
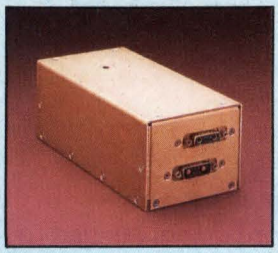
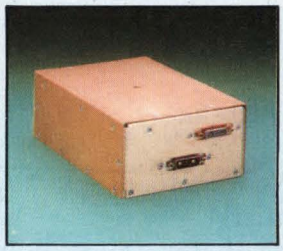


75W Single
5/12/15/24/28 VDC @
15/6.3/5/3.1/2.6A†
7″L x 2.25″W x 2.625″H

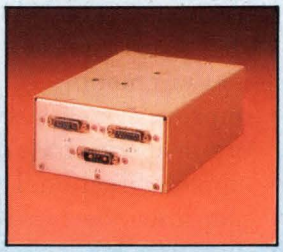


150W Single
5/12/15/24/28 VDC @
30/12.5/10/6.3/5.3A†
7″L x 3.5″W x 2.625″H



300W Single
5/12/15/24/28 VDC @
60/25/20/12.5/10.7A†
7″L x 5″W x 2.625″H

180W Dual
±12/15/24/28 VDC @
7.5/6/3.8/3.2A†
7″L x 4.5″W x 2.625″H



175W Triple
5 VDC @ 20A &
±12/15/24/28 VDC @
3/2.5/1.5/1.3A†
7″L x 5″W x 2.625″H

†Other V/A combinations available within the same power rating.

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And don't get up tight about writing style. The dreaded lab reports of your college years are behind you . . . for your contest entry, write in the same words you would use if you were describing your ideas to a couple of your engineering buddies during a coffee break. Be informal . . . the words will flow naturally.

Same with any drawings or schematics. Forget the T-square . . . neat, handwritten sketches are fine.

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- improve VSWR by changing LO drive
- use opposite rather than adjacent ports in a power splitter to achieve higher isolation for mixer IM measurements
- improve system performance by using a high-figure-of-merit phase detector
- employ directional couplers to measure VSWR of non-linear devices (such as class-C amplifiers)
- minimize RF leakage and systems bugs with pin diode switches with internal terminations
- isolate ground loops with a wideband RF transformer
- change logic state with a center-tapped balanced transformer

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Harvey Kaylie

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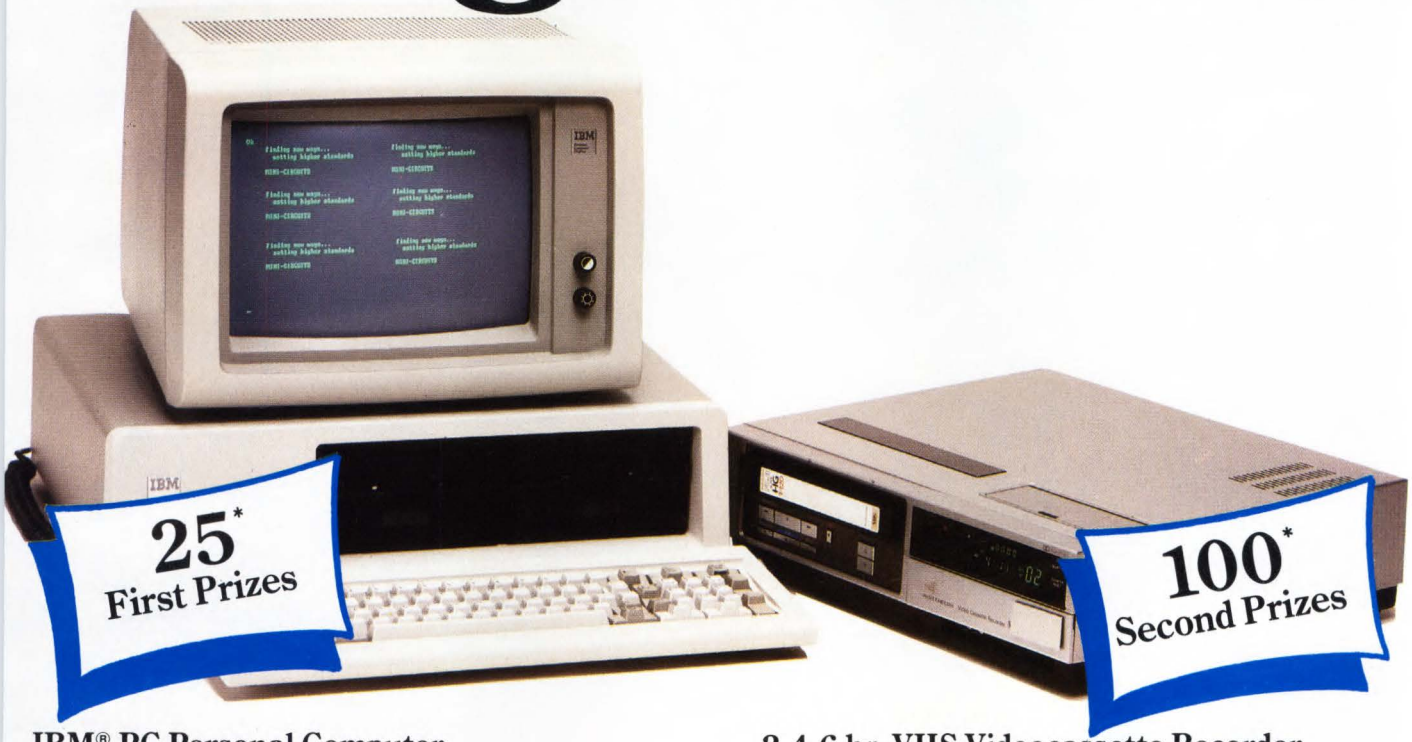

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Contest Rules

1. Submit as many entries as you wish.
2. Ideas should be original and non-proprietary. †
3. Entries will be judged by the editorial staff of Microwave Journal and their decisions will be final. The top 25 winning entries will be published in Microwave Journal.
4. All entries become the property of Mini-Circuits Laboratory and must be received by January 1985
5. Employees of Mini-Circuits Laboratory, Microwave Journal and their sales representatives, are not eligible.
6. Contest void where prohibited by law.
7. Make sure to include your business address and phone number. In addition, for non-U.S. entries, indicate AC power line voltage and frequency.
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†Winners may be asked to sign an affidavit of eligibility & release.

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CIRCLE 122 F89 REV. A-2

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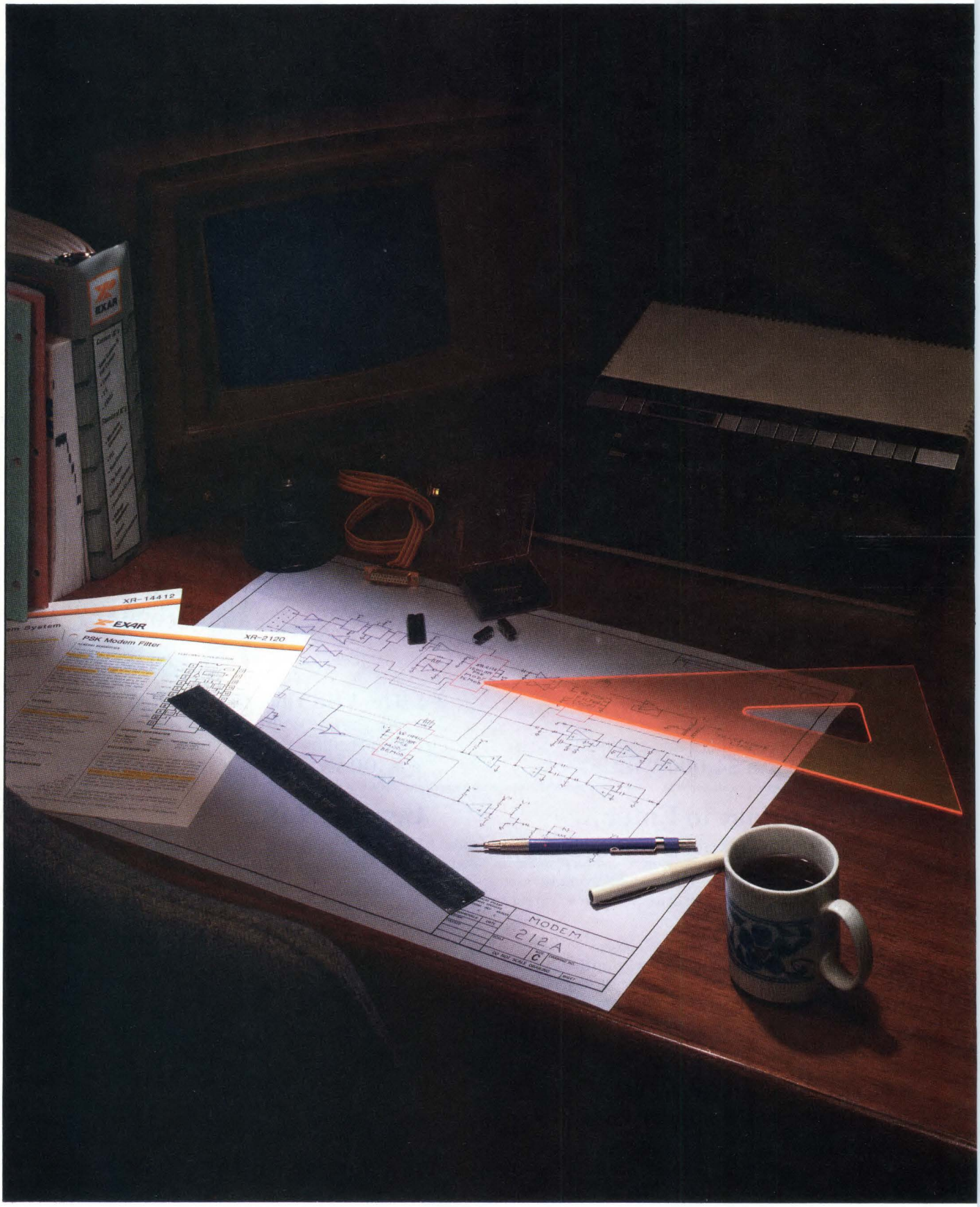

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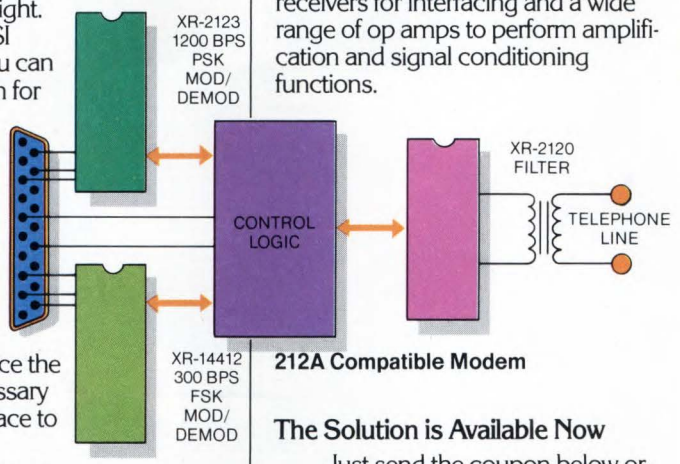

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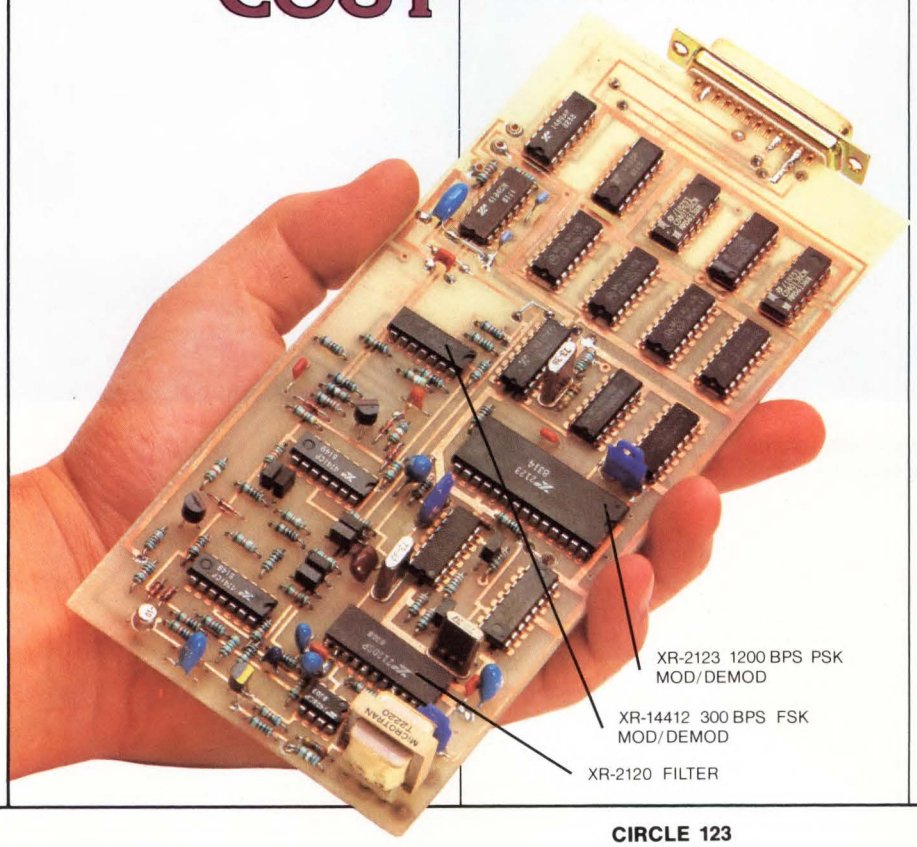

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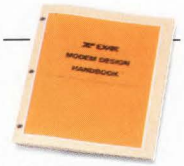

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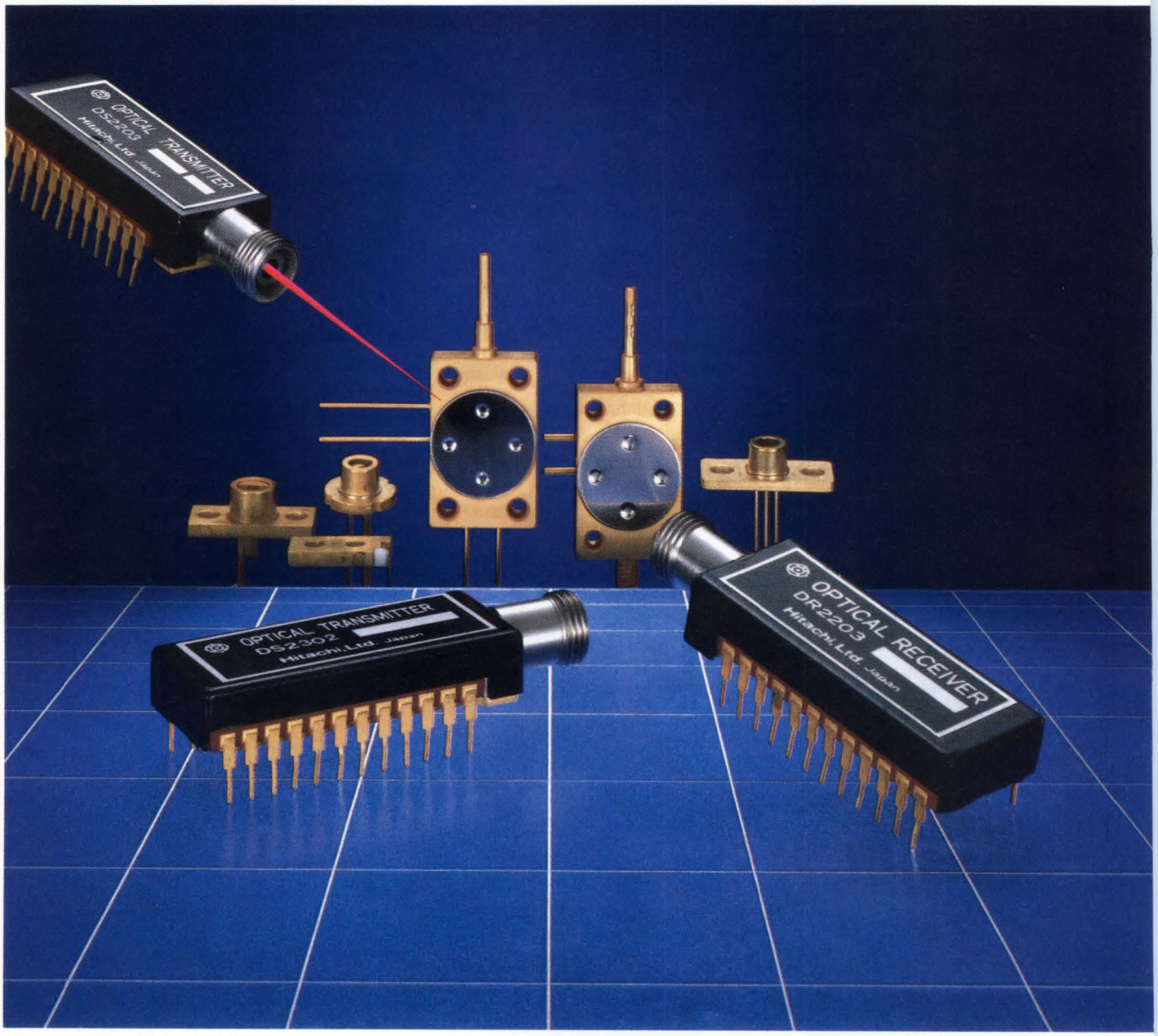

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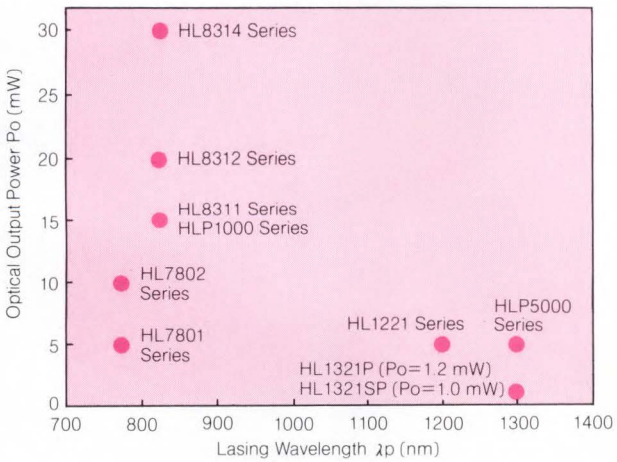

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CIRCLE 124

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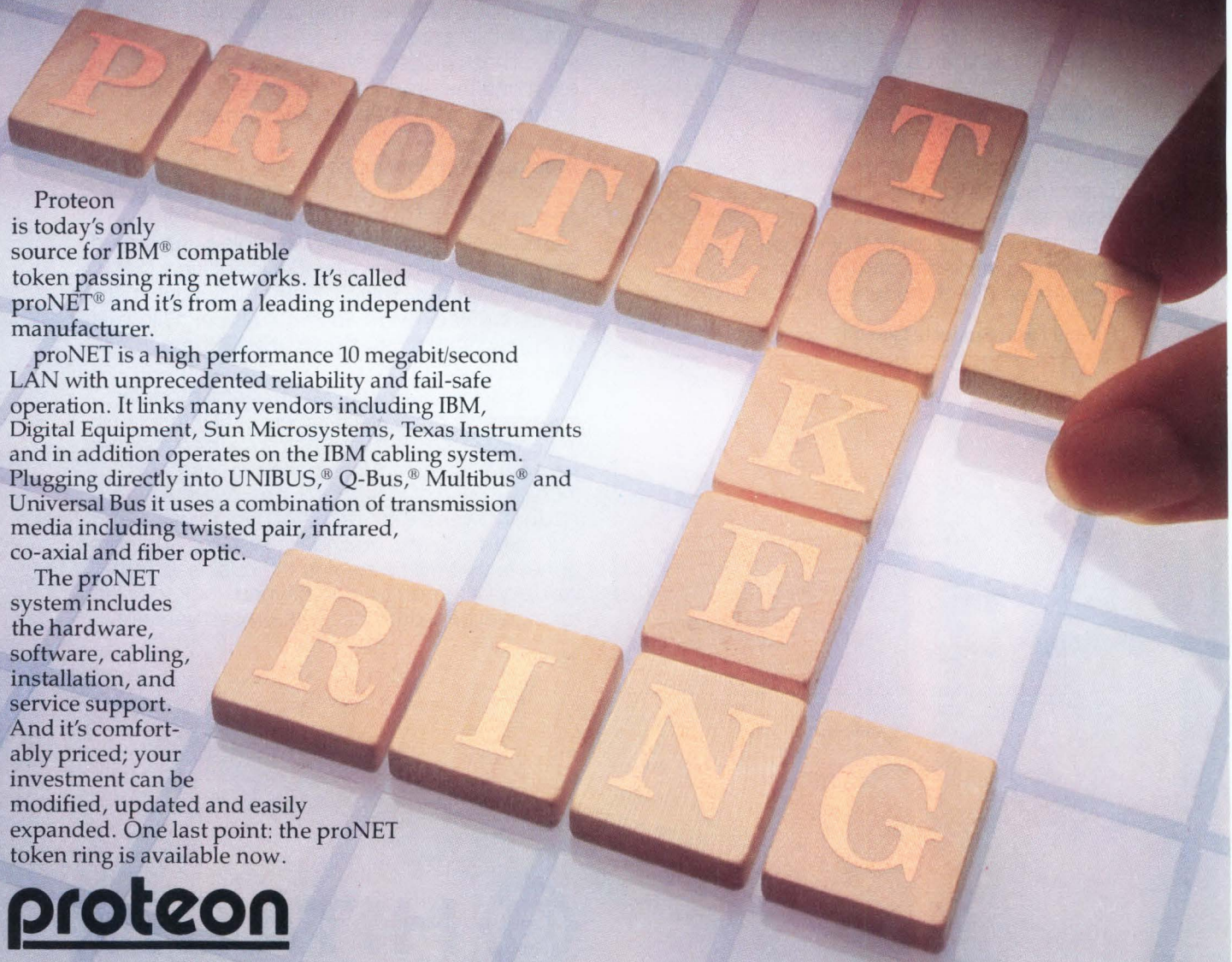

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CIRCLE 125

PRODUCT REPORT

FOCUS ON BOARD-LEVEL MODEMS

Pushed on by the influx of small computers, modem makers are successfully shrinking their boards, adding new features, and pressing the upper speed limits.

The same phone lines that stretch from coast to coast have long been recognized as the most efficient way of tying together remote computer systems. And as personal computers and other small machines show up more frequently, a modem's size, speed, and cost—plus the user's preferences—are more important than ever.

Increased portability has fueled the development of smaller boards, which simplify servicing and make it easy for an OEM to add or delete modems at the customer's whim. Unlike chips, which generally require some dedicated support circuitry, a board can be easily inserted into a socket on the CPU card when communications capabilities are desired.

As computers of all types become more powerful, their ability to create data, as well as their demand for data, increases. Typically, high-speed modems operate in conjunction with large high-speed computers. In addition, greater capabilities of personal computers are pushing users to higher transmission rates. It is no longer difficult to find 9600-bit/s modem cards, and even 14.4-kbit/s units are emerging.

Nevertheless, lower transmission rates translate into even lower costs. The 300-bit/s modems of a few years ago are still popular, and 1200-bit/s devices are rapidly emerging. Many of the latter cards maintain the 300-bit/s rate for the sake of compatibility. For example, the 212A standard specifies 1200 bits/s but incorporates 300 bits/s as a fallback rate.

One of the key areas of development focuses on letting modems talk over unconditioned lines. Although communications at 9600 bits/s and up require dedicated lines, eliminating the need for conditioning lowers line costs substantially in the long run. Greater value is prompting manufacturers to add features like voice and data transmissions, and rare is the card that does not give users the flexibility to work with either pulse or tone frequencies. Automatic dialing and answering solicit a "yes" from virtually all buyers of the typical card. In

Terry Costlow

addition, some manufacturers are making an effort to customize their modems, providing base features and then building in other functions at the user's request.

Obviously size plays an important part in portable computers. One card, designed by Racal-Vadic, measures just 5 by 5¼ in. (Fig. 1), small enough to fit into the short rack in the portable IBM PC personal computer, as well as desktop versions and compatible systems.

The 300PC, a member of Racal-Vadic's Maxwell modem line, handles both automatic and manual dialing and automatically determines whether tone or pulse signaling is needed. It can also report on call progress, so that users know if the line is busy, ringing, or answered.

The card also includes software that lets users keep track of unattended calls, recording the numbers dialed, how many times they were dialed, and the total number of completed calls. In addition, users can choose to vary the log-on sequence. That sequence includes time delays, message recognition, and fields to be transferred. With a text-editing feature, users can create or alter messages without leaving the communications program.

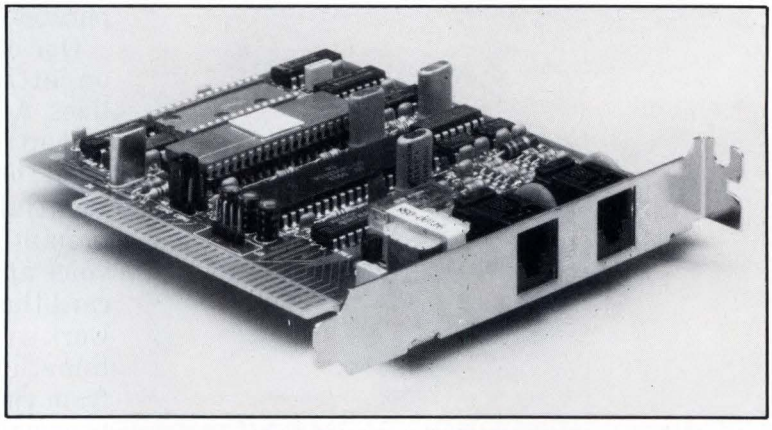
Half-size cards let users add communications capabilities without taking up a full-size expansion slot. One of the smallest cards, aptly named the Half Card by Ven-Tel, comes in at just 5¼ by 3⅞ in. The card is designed to fit into the short slots of the IBM PC XT, IBM portable, and many compatible systems, including Compaq. It operates at 1200 and 300 bits/s, with automatic speed detection assuring compatibility with other modems. In addition, it offers both half- and full-duplex transmissions and selects either tone or pulse dialing.

The Half Card comes with software that lets users store all information for a call, including files desired, call parameters, and the phone number. Thus, the user can do other tasks and later retrieve the data from a printer or disk.

AST Research has shrunk its 1200/300-bit/s modem to fit the half-card slot in IBM PCs and compatible systems. Dubbed Reach!, the card handles both voice and data, and it enables a user to interrupt a data transmission to talk with someone at the other site without losing the phone line. The card houses a loud-speaker (Fig. 2) that either gives audible indications of call progress or permits voice communications. Standard features include local and remote loopback diagnostics and full- or half-duplex communication.

Rockwell's R1212U modem transmits at 1200 bits/s using either the 212A or CCITT V.22 standards. The 4-by-4.7-in. card draws only 3 W during operation. The card features automatic adaptive equalization for maintaining low error rates even when operating over poor phone lines.

Small cards are also useful in terminals, workstations, and peripherals such as printers, so that users can transmit data to remote sites. CTS Data Communication's CTS212AT, which has dimensions of only 4 by 6 in., has a variety of features, including line status monitoring and



1. With dimensions of 5 by 5¼ in., the 300PC modem card from Racal-Vadic lets users of the IBM PC communicate at 1200 bits/s without taking a full-size slot in the computer.

built-in diagnostics, including local analog and digital loopback.

Full-size cards are still popular, and they, too, are adding features to keep their edge over other products in this crowded field. Multi-Tech's MultiModem PC card, which includes a floppy, is one of the first to fit the IBM 3270 personal computer (Fig. 3). The bundled package can store incoming data on disk or printer, a large number of phone numbers and setup instructions, the keys' programmable functions (for one-strike dialing), and optional passwords.

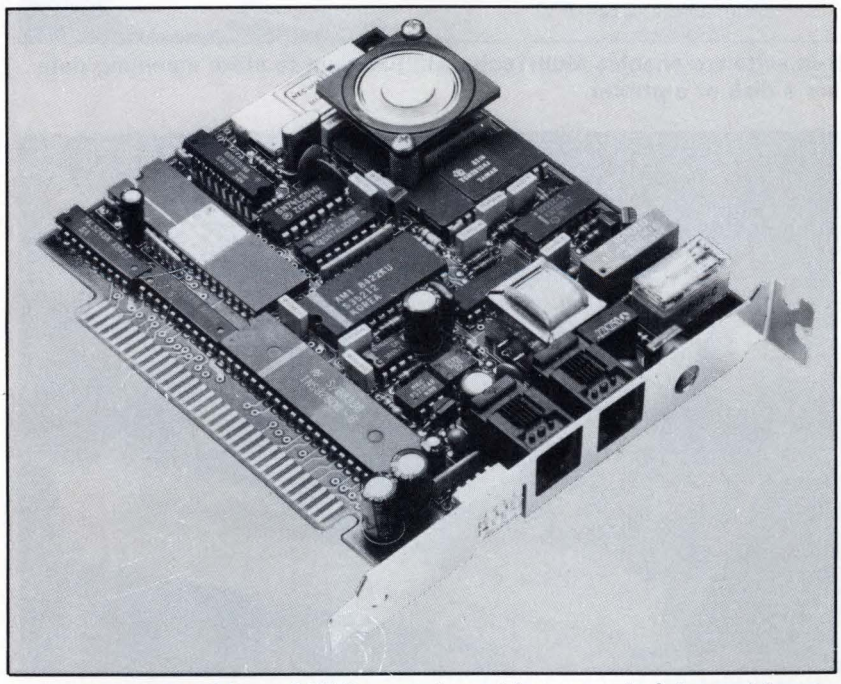
It also recognizes dial tones and busy signals, instead of simply dialing after a predetermined delay. If it detects a busy signal or if the call goes unanswered, the modem will automatically dial a second number or redial the same number. The card transmits at both 1200 and 300 bits/s.

High speeds

Currently, 14.4 kbits/s is the highest transmission rate for commercial modems. The Rixon R14.4 transmits at that rate in either full- or half-duplex operation, with synchronous transmissions. Its multiplexer accepts data from six channels, set at 2.4, 4.8, 7.2, 9.6 and 14.4 kbits/s, and transmits them at 14.4 kbits/s over dedicated four-wire telephone lines. The card, which features automatic origination and answering, can be mounted in standard 19- or 23-in. racks.

Although it communicates much faster than a 1200-bit/s modem, Rockwell's 9600-bit/s R96FT/2C modem—at 3.64 by 6.3 in.— takes up only slightly more space than the slower board (Fig. 4). The synchronous modem operates over unconditioned lines. The Fast Train card quickly adapts to the modem at the opposite end of the call, running through the training sequence in just 30 ms at 9600 bits/s or only 20 ms at the 4800 fallback rate, a particularly important feature in multipoint systems. The card, which will be introduced next spring, consumes only 4 W normally and is compatible with both V.29 and V.27 bis and ter specifications.

Universal Data's 9600-bit/s, V.29-compatible modem—designated UDS 2092108— has standard features like adaptive equalization and 7200- and 4800-bit/s fallback rates. Moreover, it puts great emphasis on simplifying testing and



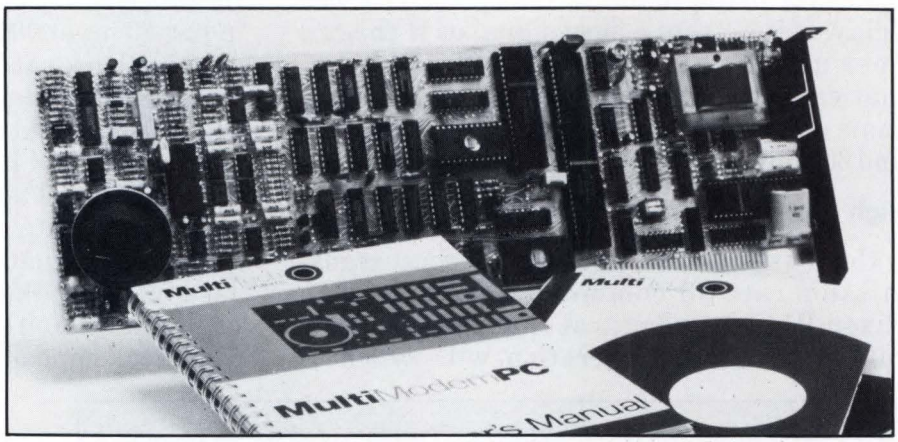
2. The Reach! card from AST Research enables users to interrupt transmissions to talk with someone on the other end. A loudspeaker enables them to monitor speech or data transmissions, the latter to let them know the message is being transmitted.

repair. Not only does it conduct analog and digital loopbacks, it can also tie into the company's eye-pattern generator, letting field personnel visually monitor its activity through a 26-pin test connector (Fig. 5).

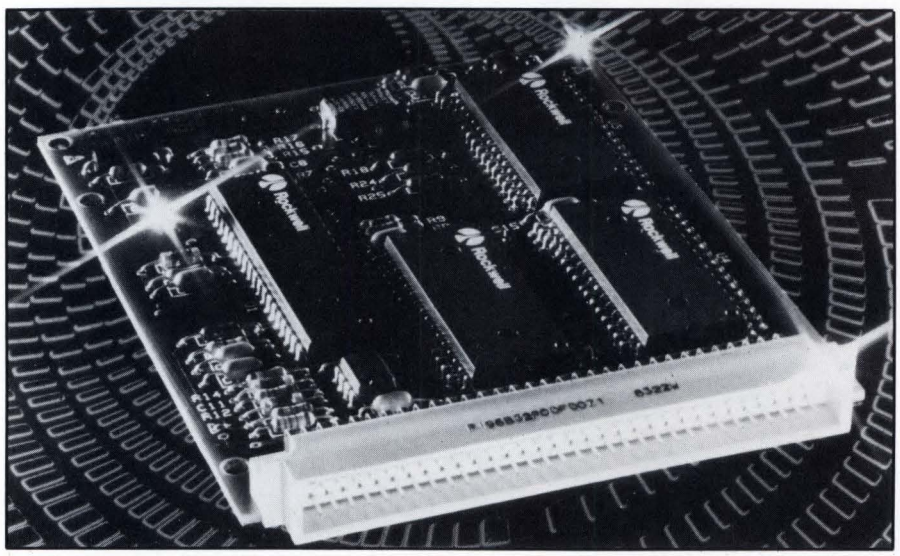
Since the cost of a modem generally rises with its transmission rate, users of high-speed systems are particularly interested in minimizing the number of cards. With that in mind, Micom has combined a time-division multiplexer with its 9600-bit/s card. The Model 4096/4+ can simultaneously transmit incoming data from up to four separate terminals, using any combination of rates that total 9600 or less. For instance, if all four channels are in use, each can transmit at 2400 bits/s. If two are used, they can each send at 4800 bits/s or one can operate at 7200 bits/s and the other at 2400 bits/s. If just one channel is active, it can use the full 9600 bits/s.

Medium speeds

Though high speed is on everyone's wish list, 2400-bit/s products are still the most widely available. One such modem, the 201BR from Develcon, is compatible with both the CCITT V.24 and Bell 201B standards. The rack-mounted card overcomes one of the key diffi-



3. Built-in software enables MultiTech's MultiModem to store incoming data on either a disk or a printer.



4. The Rockwell R96FT/2C sends and receives at 9600 bits/s, quickly adapting to line conditions and selecting the optimal speed. It adjusts to 9600 bits/s in 30 ms or to 4800-bit/s transmissions in 20 ms.

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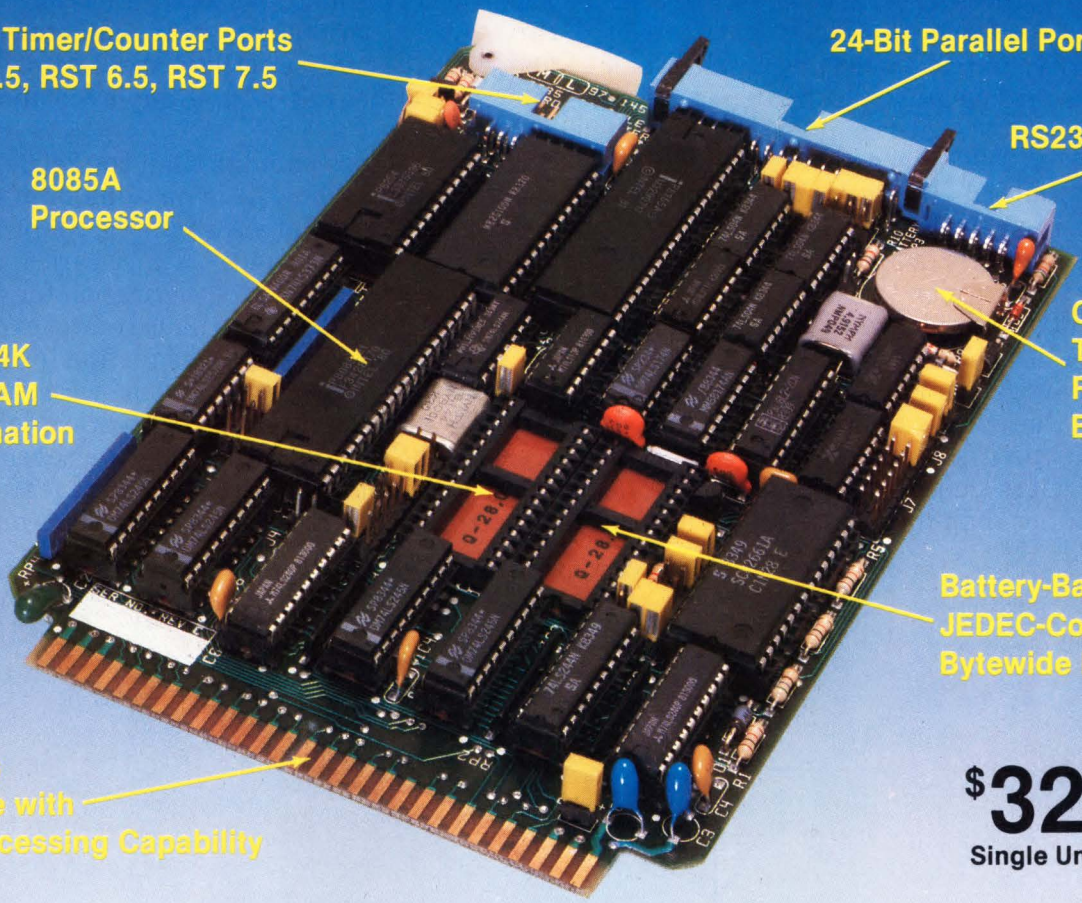

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CIRCLE 126

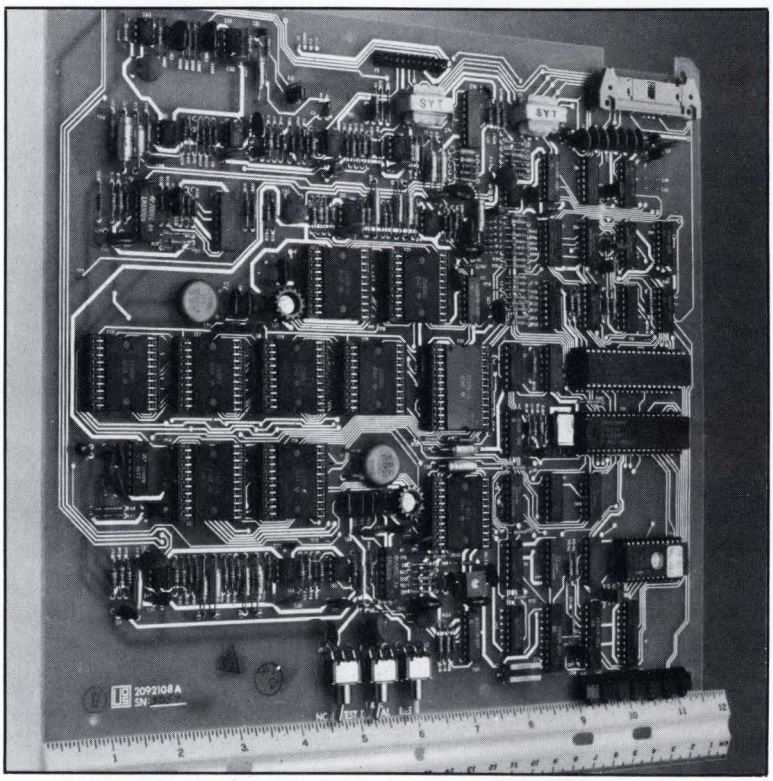
culties of modem communications with its antistreaming feature. When a board gets stuck in the transmit mode, the garbled information it sends can cause errors, jam up a network, and drive up costs by keeping the modem on line. A time delay option can disconnect the 201BR after a user-determined period whenever streaming is detected. The modem will transmit over any four-wire, unconditioned line in full or half duplex. The card measures 9½ by 10½ in.

Rockwell's R2424 card complies with CCITT standards for 2400 bits/s and with Bell 212A and 103 standards for fallback to 1200 and 300 bits/s, respectively. It meets CCITT V.22 bis and V.22 standards, addressing communications over the common two-wire public phone system. The full duplex card, occupying only 22 $in.^2$, uses VLSI circuits and signal processing to keep power consumption down to 3 W.

Like the Rockwell card, Penril's 2024 meets the V.22 bis specification, lowering overall cost by letting users tie into the public telephone network rather than the more costly four-wire lines. Standard features are automatic dialing; full diagnostics, including remote testing; and fallback to 1200 bits/s using either the Bell 212A or V.22 standards.

Rixon's R2424 communicates over the public phone network, as well as over private lines. Front-panel pushbuttons on the rack-mounted card enable users to run through diagnostics and set up the card, selecting either 1200 or 2400 bits/s and either full- or half-duplex communications.

Somewhat less popular than the 2400- and 9600-bit/s speed boards are a number of modems that transmit at maximum speeds of 4800 or 7200 bits/s. Micom's 4048/V.27+ card, for instance, meets the CCITT specification for 4800 bits/s. The 8-by-11-in. card quickly latches onto the best possible speed, transmitting for 9 ms before moving to 2400 bits/s, then increasing to 4800 bits/s after only 26 ms if errors are not excessive. The modem, which operates over unconditioned leased phone lines, also features antistreaming, so that a faulty modem cannot



5. The UDS 2092108 modem board takes servicing into account, providing a test connector so that users can tie into the Eye Pattern Generator feature and visually monitor activity.

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monopolize the leased line.

Penril's 1800 DED is compatible with the Bell 202 standard, which calls for 1800-bit/s full-duplex transmissions over a dedicated four-wire lines. A selective carrier detector speeds up the polling task by preventing noise from activating the modem when it is checking other modems for messages. The card also communicates over standard two-wire phone lines at the 212A standard's 1200-bit/s rate.

Low speeds

Despite the emphasis on 1200 bits/s, 300 bits/s is far from dead. Hayes, which has set industry standards for many basic commands and responses of personal computer modems, recently added feature-laden software to its Micromodem IIe card. Designed for the Apple IIe, the card has a top speed of 300 bits/s, with the fallback rate of 110 bits/s specified by the Bell 103 standard. Incorporating a loudspeaker for listening while the call is in progress, the board also offers pulse and tone dialing; automatic dialing, answering, and disconnecting; and full- and half-duplex communication. Program prompts let users create, display, and erase files, as well as easily adjust parameters, such as passwords.

Another 300-bit/s modem, from Universal Data Systems, is compatible with CMOS and TTL levels, easing the system integrator's tasks. Since the UDS 1032168, like most other 300-bit/s parts, is designed to keep costs low, its features are limited to automatic dialing and answering, using either pulse or tone dialing.

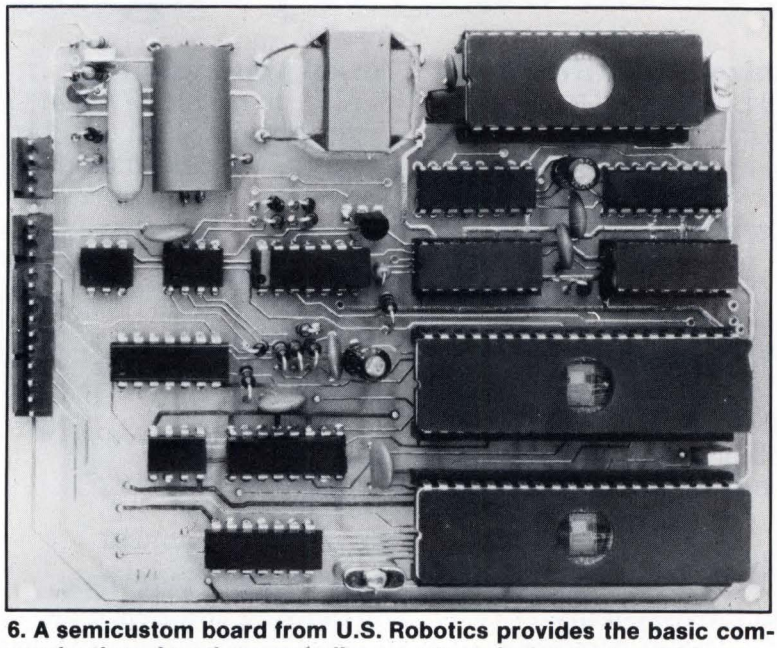
The Novation 103 Auto Dial card also aims at the low-speed Bell standard specified in its name. The 3-by-4-in. card draws only 110 mA maximum at 5 V, putting little drain on the system's power supply.

Although low-speed modems generally conform to the Bell standards set before the telephone company divestiture, modems transmitting at 2400 bits/s or higher typically follow standards set by the International Consultative Committee on Telephone and Telegraphy (CCITT).

Customization

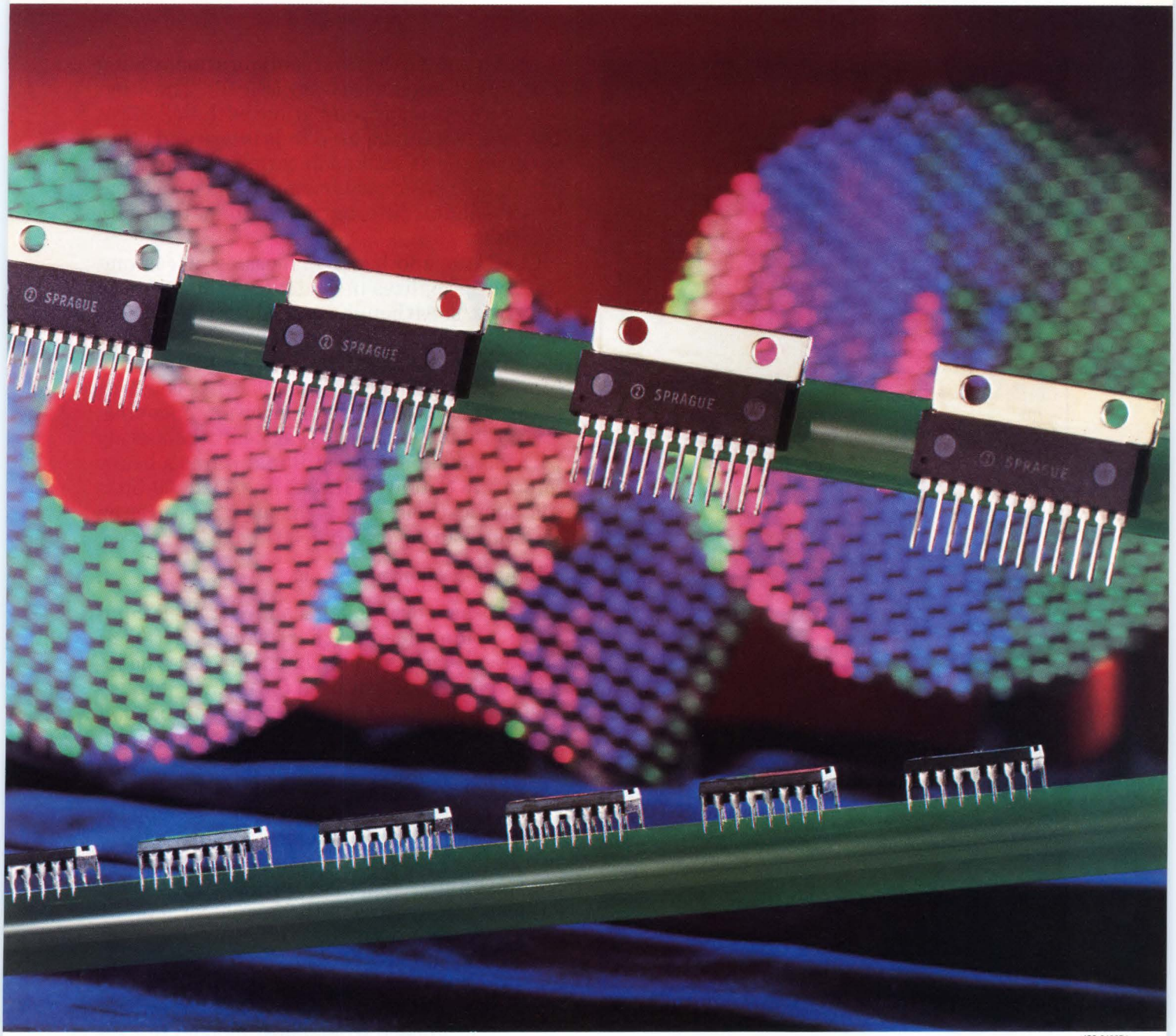
As with many OEM products, modem cards call for a degree of customization. While most manufacturers alter their standard products to fit the demands of large customers only, a few firms specialize in such adjustments.

U.S. Robotics has designed the Core, which incorporates the basic modem circuitry but lets



6. A semicustom board from U.S. Robotics provides the basic communications functions and allows system designers to add features at will. The Core card measures 3 by 4 in.

COMMANDING.



4SS-3133R1

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Directory of modem manufacturers

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AST Research Inc. Irvine, Calif. (714) 863-1333	★	★	452
Com Data Corp. Morton Grove, Ill. (312) 470-9600	★		453
CTS Corp., Datacomm Products Division Danbury, Conn. (203) 743-3681	★		454
Develcon Electronics Inc. Warmister, Penn. (800) 528-8423	★	★	455
Hal Communications Corp. Urbana, Ill. (217) 367-7373	★		456
Hayes Microcomputer Products Inc. Norcross, Ga. (404) 449-8791	★		457
Micom Systems Inc. Chatsworth, Calif. (213) 998-8844	★	★	458
MultiTech Systems Inc. New Brighton, Minn. (612) 631-3550	★		459
Novation Inc. Chatsworth, Calif. (818) 996-5060	★		460
Penril DataComm Gaithersberg, Md. (301) 921-8600	★	★	461
Racal-Vadic Milpitas, Calif. (408) 946-2227	★	★	462
Rixon Inc. Silver Spring, Md. (301) 622-2121	★	★	463
Rockwell International, Semiconductor Products Division Newport Beach, Calif. (714) 833-4700	★	★	464
S.I. Tech Geneva, Ill. (312) 232-8640	★		465
Timeplex Inc. Woodcliff Lake, N.J. (201) 391-1111	★		466
Universal Data Systems Huntsville, Ala. (205) 837-8100	★	★	467
U.S. Robotics Inc. Skokie, Ill. (312) 733-0497	★		468
Ven-Tel Inc. Santa Clara, Calif. (408) 727-5721	★		469

users determine the final configuration, adding features deemed necessary (Fig. 6). The 3-by-4-in. card, which is compatible with Bell 212A, 102, and 113, can be used in printers and other peripherals, as well as in terminals and computers. The basic card has voice and data capabilities, digital filtering, and automatic parity detection.

ComData, another firm focusing on customization, specializes in devices operating below 4800 bits/s. Although its cards can be configured to work with Bell standards, the company specializes in nonstandard cards that must be compatible with older modems that combine many standards or use proprietary encoding.

CTS, which until last year dealt exclusively with custom modems, still maintains a heavy interest in that area. Its 825 line, for 1200-bit/s communications, puts a variety of features on cards measuring less than 30 $in.^2$.

Addressing other needs

Whereas most modems address basic communications needs, others tackle different purposes. Penril's Auto Data addresses the increasingly important need for security protection against unauthorized access to important data bases. When the modem answers an incoming call, it verifies a user code by referring to previously stored data. If the caller is authorized, the modem calls back using a telephone number that is stored along with the verification code. Thus, even if an unauthorized caller has a valid code, there is no contact unless he or she also gains access to the telephone actually associated with that code.

The 1200-bit/s modem, which can be rack-mounted for large computer systems, has extensive remote capabilities. Phone numbers can be downloaded from a host modem to a remote modem, with up to 10 dialing sequences, each consisting of up to 20 numbers, stored on board. Additionally, the Auto Data card lets users key in numbers to be called from remote terminals.

A rather unusual IBM PC-compatible modem lets users communicate over either telephone lines or via shortwave radio. The PCI-2000 from Hal Communications lets users copy radio teleprinter information or relay data to seagoing vessels.□

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The first comparator with multiplexed inputs is also the first with a built-in d-a converter that acts as a digitally controlled reference. A CMOS chip from National Semiconductor, the ADC0854 has a serial input through which a command enters to select one of four analog inputs.

The selected analog signal is fed into one input of the chip's automatic-zeroing comparator. The other comparator input, the voltage reference, is fed from the 8-bit digital-to-analog converter, which is also programmed by commands through the serial input.

The comparator has a clocked output, updated at a 400-kHz rate, an offset error of 2.5 mV, and a typical output drive of 16 mA.

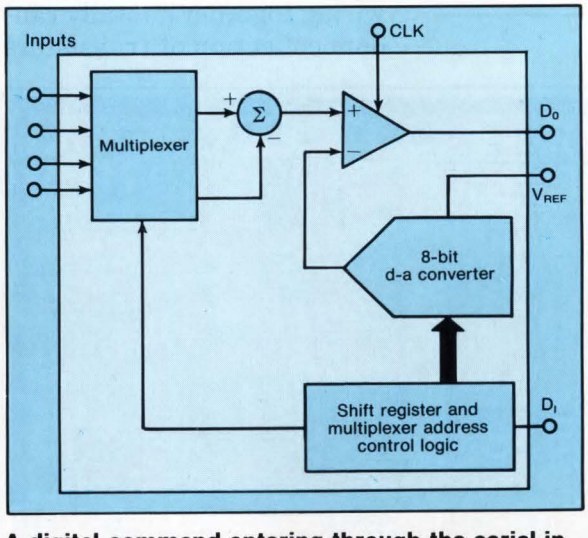
The serial input accepts a 13-bit command word consisting of a start bit, 4 bits to select the analog input (1 bit per input), and 8 bits to drive the d-a converter. The converter supplies the reference voltage for the comparator by dividing a voltage applied to an external pin down into 256 selectable levels accurately to within $\pm\frac{1}{2}$ LSB.

The chip can be used to detect when a voltage limit is reached by loading a command over the serial input to select one of the 256 reference voltage levels. If the comparator's input exceeds the reference level, the output pin will toggle. The chip can also be used as a pulse-width generator that would replace a 555 timer while allowing the pulse width to be adjusted with a serial command.

The comparator comes in a 14-pin DIP and is priced at $2.85 in 100-unit quantities. A sister chip, the ADC0852, has two multiplexed inputs and sells for $2.65 in the same quantities; it is available in an 8-pin DIP. Both parts operate from a single 5-V supply and draw 30 mA.

National Semiconductor Corp., 900 Semiconductor Drive, Santa Clara, Calif. 95051, Attn: Data Acquisition Marketing; (408) 721-5225.

CIRCLE 308



A digital command entering through the serial input (D_I) controls the ADC0854's two unique features: a multiplexer that handles several inputs (four for this chip, two for a sister chip) and a d-a converter that feels the voltage reference.

Curtis Panasuk

ANALOG

Analog array groups devices in like blocks for faster turnaround

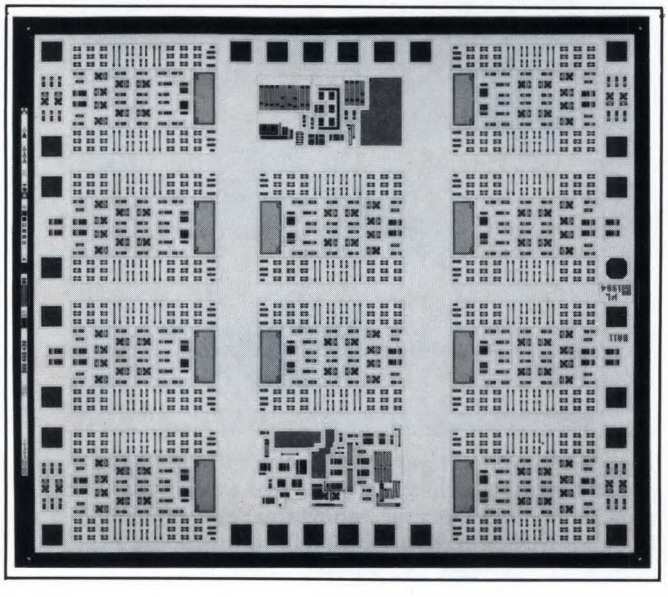
A prefabricated array of transistors groups its unwired components into blocks, or tiles, bringing to semicustom analog design much of the speed and convenience associated with the CAE approach based on gate arrays and cell libraries popular for digital chips. The tile approach cuts turnaround time to 6 weeks from the 12 typical with earlier transistor arrays.

Designed by Micro Linear, the FB300 Mosaic Array includes capacitors—one of the few arrays to do so—as well as resistors and diodes, plus the transistors. It lays out its tiles in a way that makes the chip look like a mosaic, giving rise to its name.

Curtis Panasuk

Each tile can be formed into a high-level analog function and will allow engineers to submit analog semicustom designs to Micro Linear in the form of a block diagram instead of in the traditional drawing of detailed transistor interconnections.

Previously, semicustom analog designs were done by wiring together a totally random collection of transistors and resistors. This approach is labor-intensive and unsuitable for offloading onto software.



It also sometimes results in very long connection paths; these paths create unwanted capacitances that interfere with circuit operation. The tile approach and the use of two layers of metal, in contrast, holds down connection lengths.

Of the four classes of tiles, the largest has over 135 components, and there are 10 of them on the chip (visible in the photograph). These tiles each have 19 npn and 13 pnp transistors. There are also 103 resistors ranging in value from 18 to 25 kΩ, as well as built-in capacitors, which eliminate the need for extra components on the pc board. The other types of tiles provide voltage references, general-purpose transistors, and power transistors for use in an output stage having a drive capability of up to 20 mA.

To speed the conversion of the block diagram submitted by the designer into a finished part, Micro Linear uses a library of different metalization patterns that can be applied individually to a tile to

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SDA 6020: Input slew rate 300V/μsec; accurately digitizes 25 MHz input signal at 50 MHz sampling rate.

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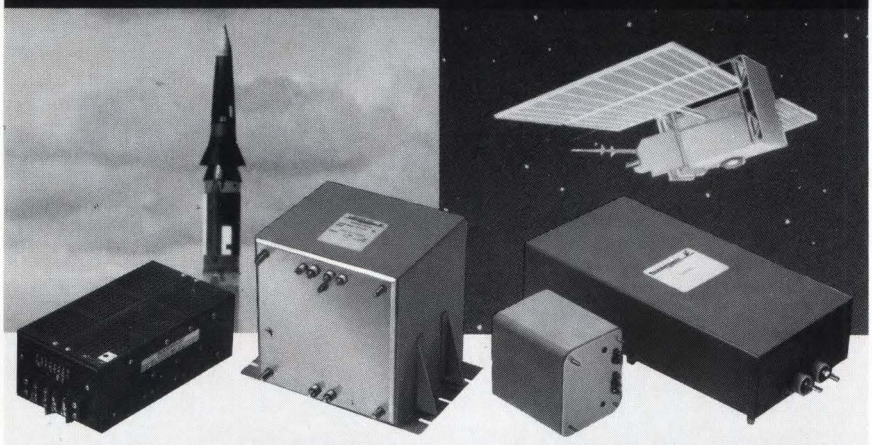

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CIRCLE 141

wire its components into a high-level function (or "macro") such as an op amp, an analog-to-digital or digital-to-analog convertor, or a timer (see the box).

The chip's transistors have an f_T of 1 GHz, making it possible to configure tiles into video amplifiers or modulators.

Some of the high-level functions available

- Pnp input op amp (LM324)
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- Operational transconductance amplifier (LM13600)
- Ground-sensing comparator (LM339)
- High-speed latching comparator (LM360)
- Video amplifier (LM592/LM733)
- Double-balanced modulator (LM1496)
- Timer (LM555)

In the future, each of the standard macros will be available separately in a DIP, for breadboarding. Furthermore, an engineer will be able to send in the description of any special macro he or she requires and the company will create the wiring pattern.

Micro Linear is now accepting designs for the chip. The nonrecurring engineering cost for an average design is in the range of $10,000 to $20,000. In high volume, the finished parts are available for under $5 each.

Micro Linear Corp., 2092 Concourse Drive, San Jose, Calif. 95131; (408) 262-5200.

CIRCLE 317

ANALOG

574 a-d converter slips sample-and-hold chip into its 28-pin package

Pin-for-pin-compatible with the industry-standard 574 analog-to-digital converter, the HS 9474 from Hybrid Systems also fits a sample-and-hold circuit into its 28-pin DIP. The 12-bit hybrid device has a maximum throughput of 31 kHz and the monolithic BiFET sample-and-hold circuit sports a 7-μs acquisition time (typical) with 0.01% nonlinearity for a full 10-V input swing.

The successive-approximation converter features a 25-μs conversion time and is followed by a three-state output buffer, which ensures easy interfacing with bus-structured microprocessor-based circuits. It is readily configured to perform self-triggered continuous conversions.

The device includes a 1000-pF hold capacitor and a 10-V reference. Through the use of external zero and gain calibration potentiometers, offset and full-scale gain errors are adjustable to zero, with the latter specification requiring the use of an external 50-Ω resistor.

The converter has an aperture time of 200 ns or less, and jitter is on the order of 10 ns. It is specified for either $\pm 0.025\%$ or $\pm 0.012\%$ nonlinearity at 25°C, with a drift of ± 0.5 ppm/°C maximum and with monotonicity guaranteed over 11 or all 12 bits.

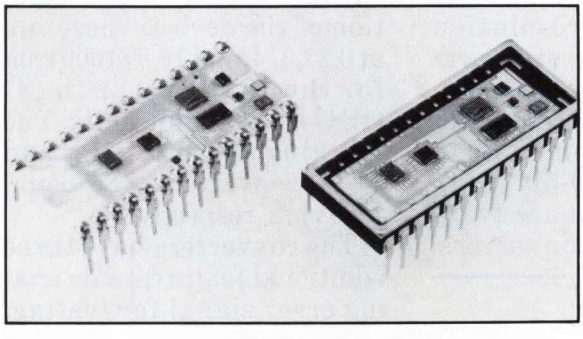
The converter is factory-set either for the 0-to-10- and ± 5-V ranges or for a single ± 10-V range. All versions require ± 15- and $+5$-V power supplies and typically dissipate 600 mW.

The device can be ordered in a hermetically sealed ceramic package, with processing to MIL-STD-883D, which guarantees an operating temperature range of $-55°$ to $+125$°C. A commercial package is offered for operation over 0° to 70°C.

An HS 9474 in a commercial package with 11-bit accuracy is priced at $47.50 apiece in 100-unit quantities. The same part in a military package costs $130 each for the same quantity. Availability is from stock to four weeks.

Hybrid Systems Corp., 22 Linnel Circle, Suburban Industrial Park, Billerica, Mass. 01821; Jack Worthen, (617) 667-8700.

CIRCLE 320



Gary Elinoff

ANALOG

Resolver-to-digital converters deliver accurate velocity, as well as position, data

A family of resolver-to-digital converters permits designers of velocity servo systems to replace either a combination of absolute optical encoder and tachometer generator or a similar mix of resolver, tachometer, and r-d converter with a single brushless resolver and an r-d converter. The result of the substitution, using a member of the 1S family of converters from Analog Devices, is a system that is more accurate, lower in cost, simpler, and more reliable.

The four members of the family range in resolution from 10 to 16 bits, or 21 arc-minutes to 20 arc-seconds, and they can track from 630 rpm (the 16-bit 1S64) to 40,800 rpm (the 10-bit 1S14), specifications that are available with other converters. However, it is when they are compared, from a system point of view, with a tachometer generator that they shine.

Whereas a low-cost tachometer ($150 to $300) has a nonlinearity, maximum error, and output ripple of 1%, 10%, and 5%, respectively, these specifications are 0.1%, 1%, and 0.5% + 200 μV for the converters, at a price of $183 to $294 for commercial units. Moreover, a tachometer to meet the 1S specifications costs about $4000.

The velocity outputs are dc voltages scaled to the resolution of the device. These run at 0.25, 1, 4, and 16 V/1000 rpm for the 10-, 12- (1S24), 14- (1S44), and 16-bit units. The tracking rate of the 12- and 14-bit converters is 8670 and 2550 rpm, respectively.

The converters have three additional features: a dc analog error signal for testing, for carry-overs, and to indicate the direction of rotation; an angle offset permitting a trimming potentiometer to move the output up to 32 LSBs; and an analog voltage output proportional to the distance between two adjacent code changes. This last feature permits the designer to stiffen, or increase, the gain of the servo.

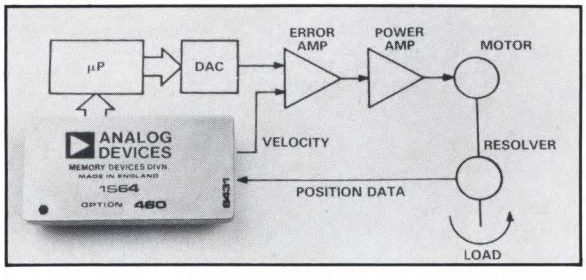
The accuracy of the units over their operating temperature range is ±25, ±8.5, ±5.3, and ±4 arc-min, respectively, for the 5YO 10-, 12-, 14-, and 16-bit versions. The 4YO version raises this to ±2.6 arc-min. for the 16-bit 1S64. Regardless of resolution, all units are monotonic, and their repeatability is to 1 LSB.

Commercial and military grades of each model are available in 40-pin ceramic and metal DIPs, respectively. For nine or fewer pieces, the unit cost is $183, $186, $199, and $294 for the 10- through 16-bit commercial models. The military units run $366, $372, $398, and $588.

Analog Devices Inc., Box 280, Norwood, Mass. 02062; Richard Parker, (617) 329-4700.

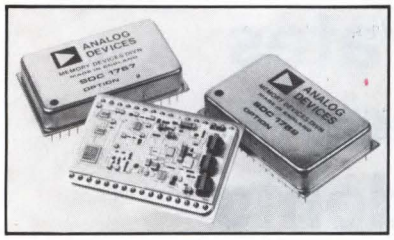
CIRCLE 310

Frank Goodenough



ANALOG

Two SDCs boast high tracking rates



Two hybrid synchro/resolver-to-digital converters deliver tracking rates that are 50% faster than competitive devices. The SDC/RDC1767 and 1768 combine a velocity output with a maximum tracking rate of 36 revolutions/s for the 12-bit 1767 and 18 revolutions/s for the 14-bit 1768.

The converters' internal transformers provide isolation to 350 V dc—making the devices particularly useful in military and aerospace applications. The units have a signal and reference frequency range of 400 Hz to 2.6 kHz. They produce parallel outputs with a load-driving capability of 6 TTL. Maximum error is guaranteed at ±8.5 and ±5.3 arc-minutes for the 1767 and 1768, respectively, over a range of −55° to +125°C.

Analog Devices Inc., 2 Technology Way, Norwood, Mass. 02062; (617) 329-4700. $471 and $503 for the 1767 and 1768, respectively (10 to 24 units); six to eight weeks.

CIRCLE 322

DAC specifications suit robotics

Designed for robotics and other precision servomotor applications, two 16-bit digital-to-analog converters provide a differential linearity error of +0.006%, −0.003% of full-scale reference—ensuring 15-bit monotonicity around bipolar zero over the entire specified temperature range of 0° to 70°C. The settling time (to within ±0.003% of FSR) is 350 ns for the DAC710KH and 4 μs for the 711KH.

Burr-Brown Corp., PO Box 11400, Tucson, Ariz. 85734; (602) 746-1111. $29 (100 units).

CIRCLE 323

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CIRCLE 142

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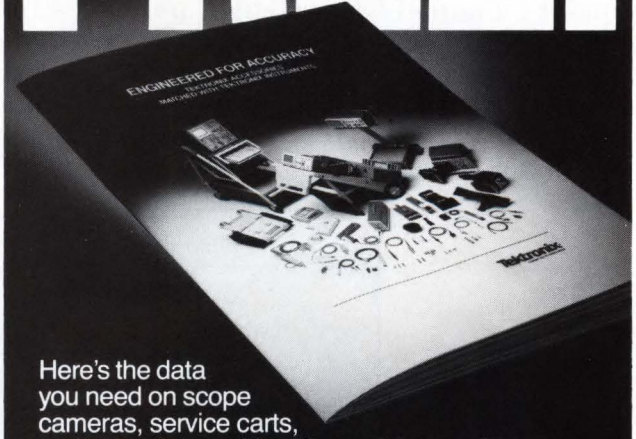

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CIRCLE 143

ANALOG

NMOS chip integrates all the filters needed by 4800-bit/s modems

A single NMOS chip is the first to contain all the filters needed by a 4800-bit/s modem. Reticon's R5637 is for use with Bell 208/CCITT V.27 modems operating either full duplex over four-wire cable or half duplex over two-wire cable.

The chip integrates four switched-capacitor filters: the receiver bandpass filter, a fixed compromise delay equalizer, a 75/150-baud secondary channel filter (Bell 202/CCITT V.23), and a 3000-Hz transmitter low-pass filter. It also includes two uncommitted op amps that can be used for gain control or clock or anti-aliasing filters.

The bandpass filter has a 1-dB bandwidth of 750 to 2800 Hz, a passband ripple of 1 dB, and an adjacent channel rejection ratio of 53 dB. Its stopband rejection ratio is −55 dB at 600 Hz and +50 dB at 3700 Hz, and its group delay variation from 1100 to 2500 Hz is less than 200 μs.

The delay equalizer compensates for the average group delay encountered in telephone systems in the U.S. It has a nominally flat amplitude response (0 dB). The transmitter filter prevents frequencies above 3000 Hz on the chip from getting on the line and causing aliases. It is connected between the modem's d-a converter and the telephone line.

The op amps need an external 3.6864-MHz clock input or a 3.6864-MHz crystal.

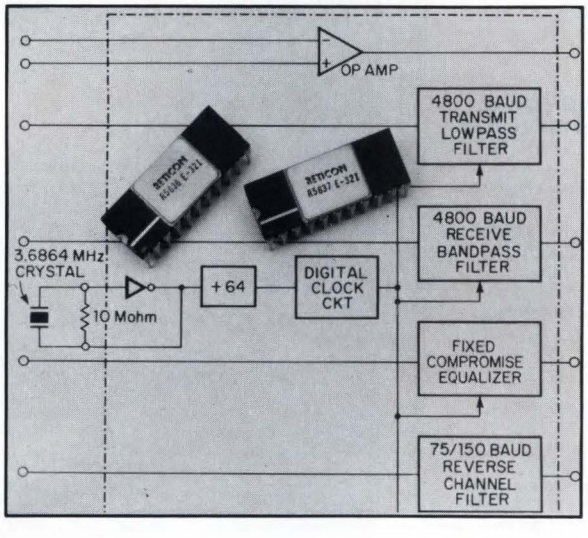
Also available is the R5936, for 2400-bit/s modems (Bell 201/CCITT V.26) operating full duplex over four-wire cable. It has a similar set of four filters but only one unconnected op amp. This chip's bandpass filter has a 1-dB bandwidth—760 to 2860 Hz; a lower passband ripple of 0.5 dB; and a stopband rejection ratio of −50 dB at 400 Hz and +60 dB at 4000 Hz. The adjacent channel rejection ratio and group delay variation remain the same.

Both chips operate from ±5- to ±10-V power and from 0° to 70°C; they come in a 22-pin plastic DIP. The R5637 costs $12.75 and the R5636 $14.75 in lots of 1000. Small quantities are available from stock.

EG&G Reticon, 345 Potrero Ave., Sunnyvale, Calif. 94086; Ken Small, (408) 738-4266.

CIRCLE 318

Frank Goodenough



ANALOG

14-bit DAC has deglitched output

With its low-glitch voltage output of 10 mV pk-pk and its 10-MHz update rate for small step changes, the DAC-02310 d-a converter is suitable for use in vector-stroke CRT displays, waveform generators, and automatic test equipment. The hybrid converter is available in linearity-error grades of ±0.006% and ±0.012%, each with 14-bit resolution. Settling time to within ±½ LSB for a full-scale ±2.5-V step change is 600 ns.

The DAC-02310 can be programmed for five output voltage ranges with a maximum output current of 5 mA. Specified for operation over the commercial and military temperature ranges, the price of the unit is $245 and $269, respectively.

ILC Data Device Corp., 105 Wilbur Place, Bohemia, N.Y. 11716; (516) 567-5600.

CIRCLE 324

Converter links LVDT with microprocessor

Suitable for industrial measurement and positioning applications, the 2S50 is an 11-bit ratiometric tracking converter that interfaces an LVDT with a microprocessor. The converter is specified for operation over the commercial and military temperature ranges, with accuracies to within 0.1% and 0.2% of full scale. Each version is available with one of two reference frequency options: 400 Hz or 1 kHz to 10 kHz.

Because the 2S50 converts the ratio of the excitation signal to the output signal, it is insensitive to changes in the excitation voltage amplitude, frequency, and waveshape.

Analog Device Inc., 2 Technology Way, Norwood, Mass. 02062; (617) 329-4700. From $92 (100 units); stock.

CIRCLE 325

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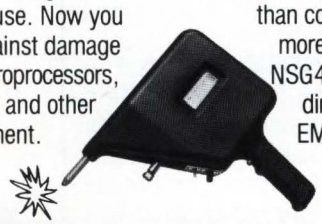

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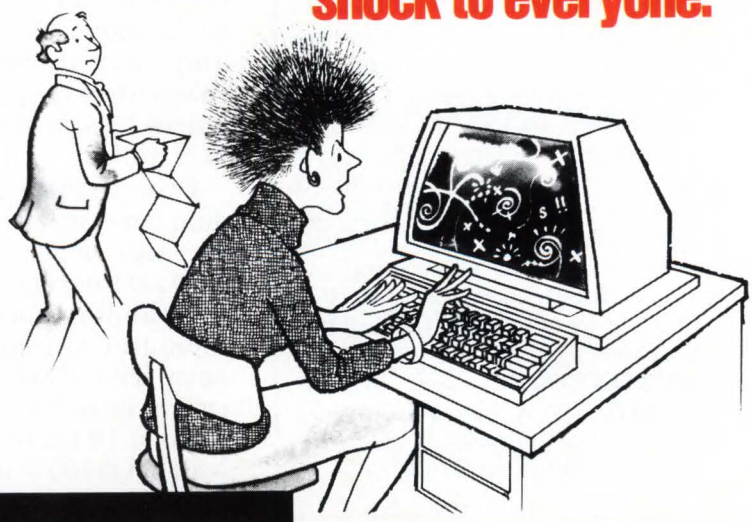

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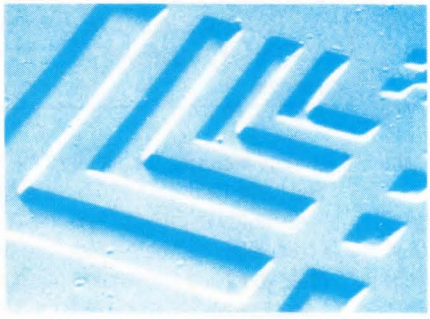
CIRCLE 144

Two new solutions to new product development.



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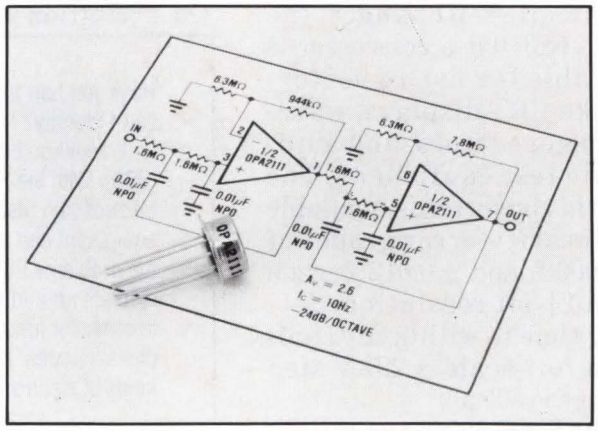
CIRCLE 145

Dual op amp chip sets performance marks



Based on the single-unit OPA111 introduced by Burr-Brown earlier this year (ELECTRONIC DESIGN, Feb. 9, p. 97), the OPA2111, also by Burr-Brown, is the highest-performing dual op amp ever. It costs about 20% less per op amp than its predecessor, takes up less space, and requires less production labor to install.

Even though, as with any dual version, there are some sacrifices in performance, the OPA2111 nevertheless boasts outstanding specifications, including the same voltage noise floor of $8nV/\sqrt{Hz}$ maximum over the frequency band of 10 Hz to 10 kHz (for which it is 100% tested).

Its bias current of 4 pA maximum, still impressively low, is necessarily higher than the 1 pA of its single version (because the quiescent current through two op amps is higher than through one, thus heating the chip slightly more and thereby increasing the bias current).

Similarly, it still sports a low offset voltage drift—2.8 μV/°C (vs 1 μV/°C for the OPA111). The low offset voltage of 500 μV maximum is twice that of the OPA111, owing to the compound yield of two devices over one. The dual unit also has a high open-loop gain of 114 dB minimum and a high common-mode rejection ratio of 96 dB minimum.

The OPA2111AM, which works over the temperature range of −25° to +85°C, costs $9.95; the slightly better-performing OPA2111-BM, for the same temperature range, is priced at $16.50; and the OPA2111SM, for −55° to +125°C, costs $16.75—all in 100-unit quantities. Delivery is from stock.

Burr-Brown Corp., PO Box 11400, Tucson, Ariz. 85734; (602) 746-1111.

CIRCLE 303

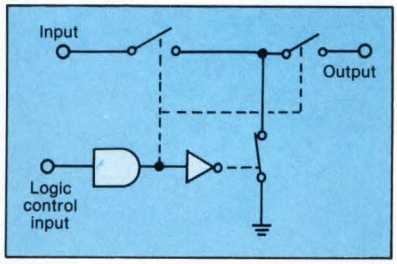
Heather Bryce

ANALOG

Quad CMOS chip switches 100-MHz signals

Designed to replace p-i-n diode switches at a tenth the price, as well as providing more isolation and needing no external parts, a four-channel CMOS chip handles 100-MHz signals with a flat response to within ±3 dB. When off, the four SPST switches on the IH5352 from Intersil feature an input-to-output isolation—achieved by the use of a series-shunt, or T, configuration—of 60 dB at 10 MHz, and cross-coupling between channels is more than 60 dB.

Moreover, the typical turn-on and turn-off times are under 150 ns and 80 ns, respectively. Also, break-before-make switching is guaranteed. Another major feature is the on-resistance—typically 75 Ω for matching transmission lines.



The switch on each of the CMOS IH5352's four channels uses a T circuit to achieve 60 dB of input-output isolation at 10 MHz.

The chip uses three supplies, a 5- to 15-V logic supply and analog supplies that can vary from ±4.5 to ±16 V. All draw a maximum of 10 μA.

The commercial IH5352-CPE comes in a 16-pin plastic DIP, and the IH5352IJE and IH5352MJE industrial and military units in 16-pin ceramic DIPs. In lots of 100, the commercial unit sells for $7.75 each. Small quantities are available from stock.

Intersil Inc., 10710 Tantu Ave., Cupertino, Calif. 94014; Paul Delazari, (408) 996-5273.

CIRCLE 309

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CIRCLE 146

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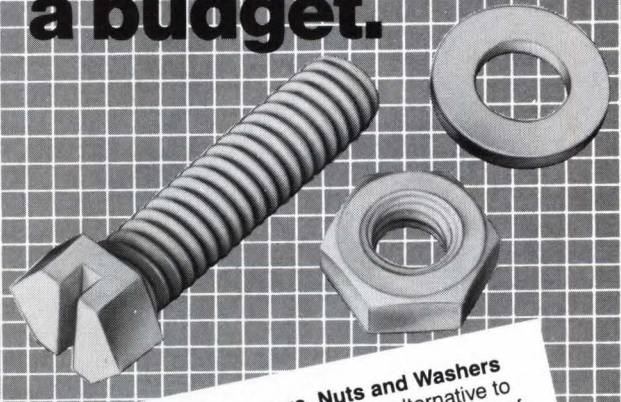

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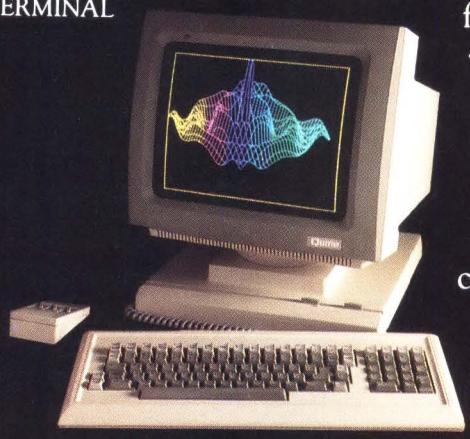

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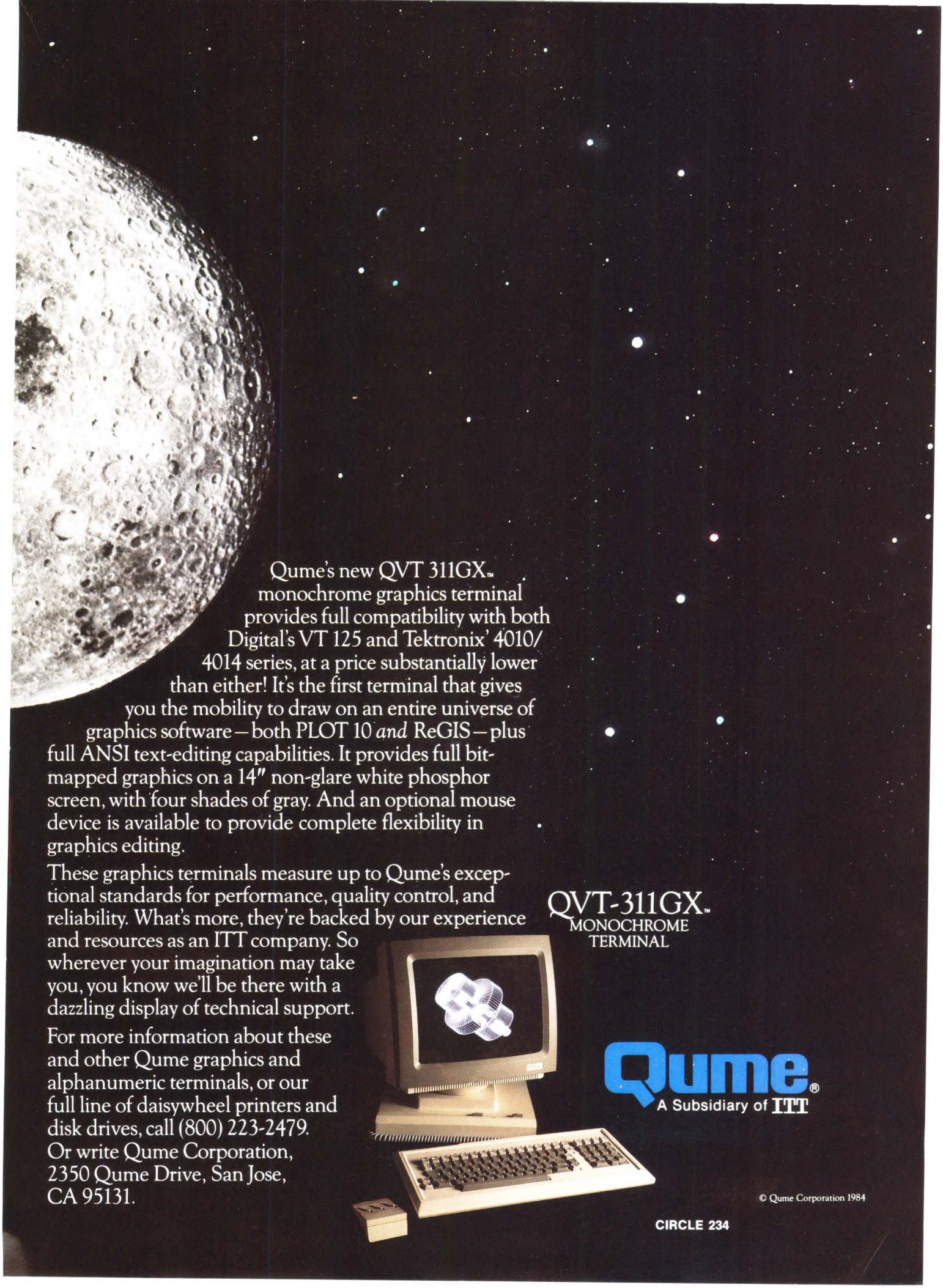

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CIRCLE 234

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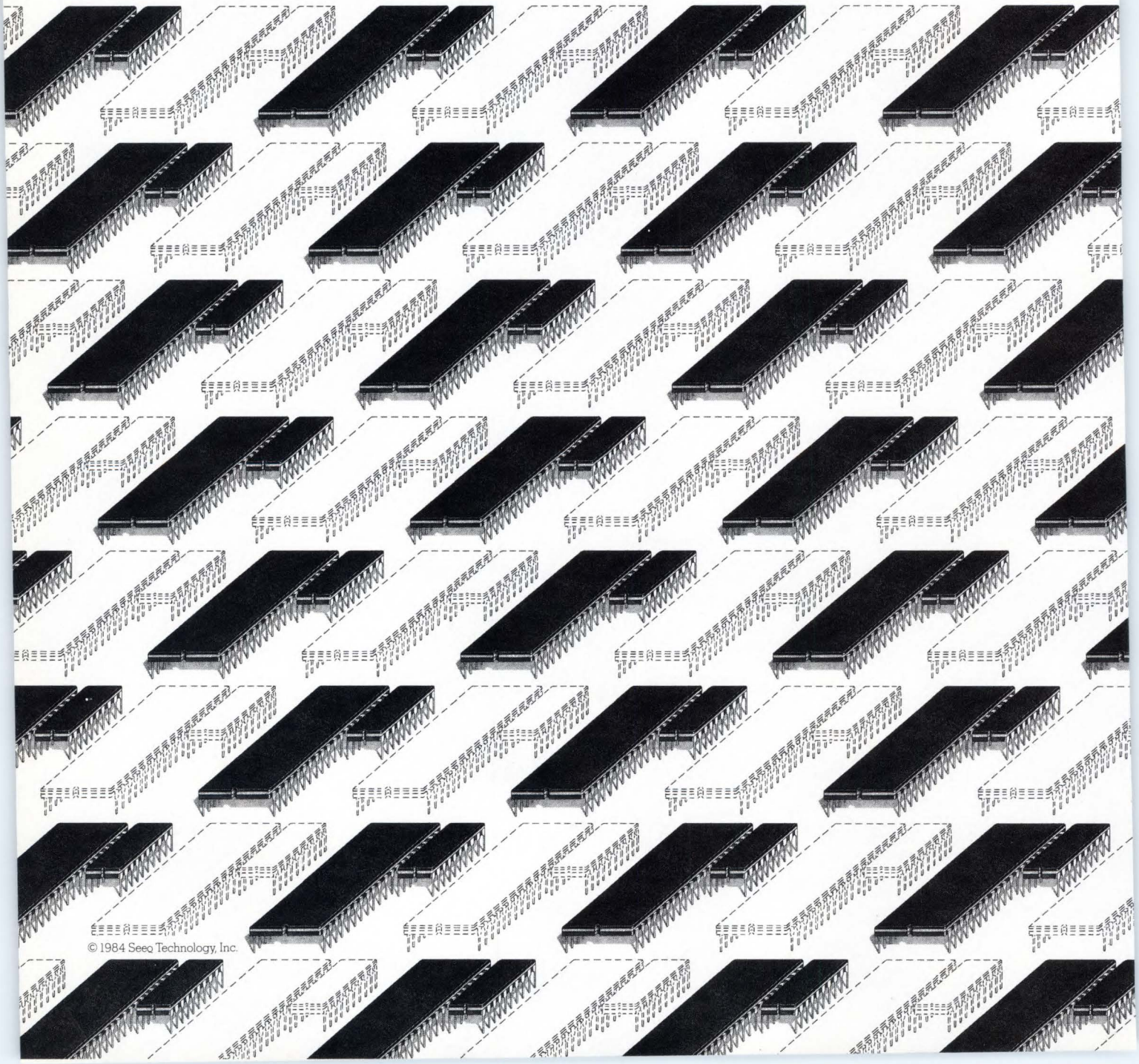

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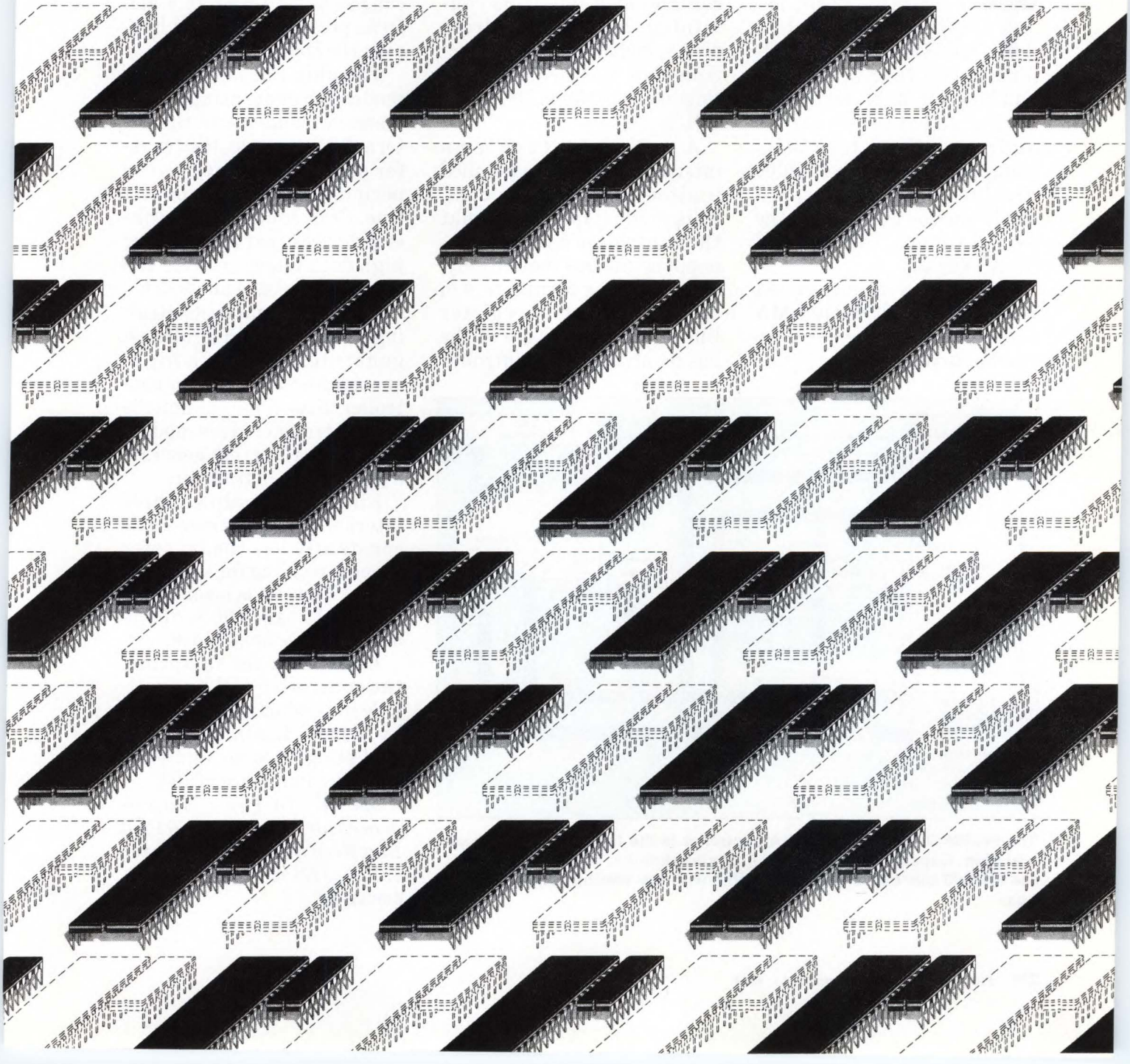


DIGITAL ICs

DMA controller chip addresses 4 Gbytes, works with 68000 family

The first full 32-bit peripheral, Motorola's MC68442 DMA controller has two 16-bit channels and handles 32-bit addresses giving 4 Gbytes of direct addressability. It is fully compatible with the M68000 bus, including all exception conditions, as well as with the asynchronous VMEbus and VERSAbus.

The chip is an enhanced version of the MC68440 DMA controller. Aside from containing the needed address pins, it includes an extra function code output that distinguishes between DMA and CPU bus cycles.

A unique feature is an internal transfer mode called limited-rate auto-request. This mode guarantees that the controller does not monopolize the bus indefinitely. Programming certain bits in the global control register limits the percentage of the bus bandwidth the controller can use to between 6.25% and 50%, preventing it from hogging the bus.

The chip has three other modes for generating direct memory requests. In the external burst mode, the transfer occurs for as long as the peripheral holds the request line. Consequently, peripheral devices that require very high data transfer rates can use all of the bus bandwidth.

In the external cycle-stealing mode, the peripheral must generate pulses of a high-enough frequency for the controller to continue holding the bus for transfer. This mode is used for devices that generate a pulse for each transfer.

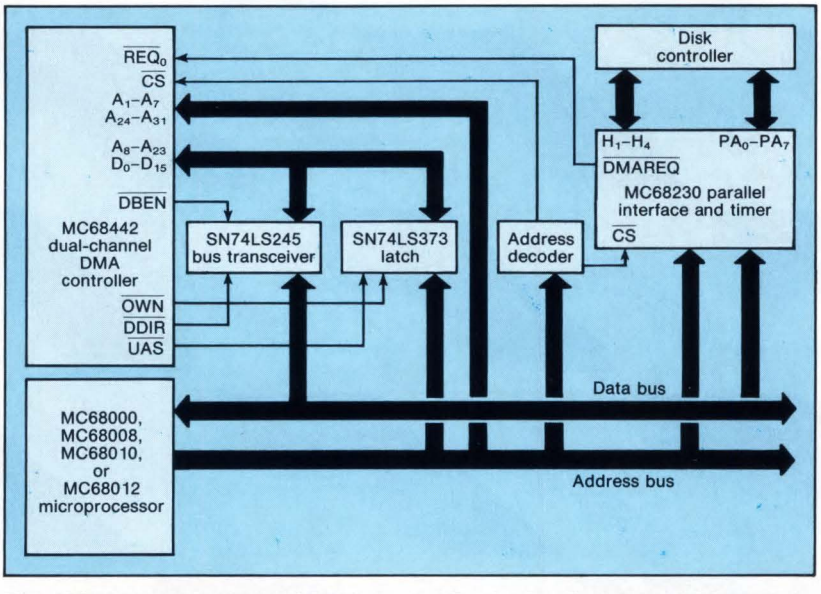
Finally, the chip's simple internal maximum rate mode constantly has the transfer request pending for a channel until all data has been transferred. It uses 100% of the available bus bandwidth.

Ready now for sampling, the controller will be available in production quantities by March. It comes in a 68-lead pin-grid array and costs $59.69 in quantities of 100.

Motorola Inc., Microprocessor Division, 3501 Ed Bluestein Blvd., Austin, Texas 79721; (512) 928-6860.

CIRCLE 307

Heather Bryce



The MC68442 two-channel DMA controller is the first full 32-bit peripheral chip. Capable of addressing 4 Gbytes directly, it is designed for the M68000 bus but is also compatible with the VMEbus and VERSAbus.

DIGITAL ICs

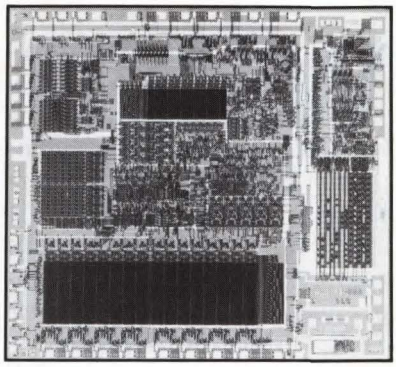
Floppy-disk controller chip has everything but buffers

Although a well-established chip, the 765A floppy-disk controller requires considerable support circuitry to function in a system. To cut that burden, the FDC9266 combines on one chip the control functions of the 765A with a digital data separator that handles both single- and double-density requirements.

Developed by Standard Microsystems, which manufactures NEC's 765A controller under license and makes a stand-alone data separator (the FDC9229), the FDC9266 eliminates the external adjustments previously needed and also permits variable write precompensation (track-selectable).

An excellent choice to help reduce the cost or size of IBM-compatible personal computers, the chip operates identically to the 765A from the host interface side. Additionally, it does not suffer from the occasional lock-up problem encountered with the 765A, caused by improper alignment of the falling edges of several timing signals.

Like the 765A, the new chip manages either 5¼- or 8-in. disk drives; handles data record lengths of 128, 256, 512, or 1024 bytes; can transfer multiple sectors and tracks; and controls up to four drives. Additionally, it can scan a single sector or an entire track's worth of data fields, comparing, on a byte-by-byte basis, data in the processor's memory with the data read from the diskette. Track stepping rate, head load time, and head unload time all are user-programmable.



The controller also includes an address-mark detection circuit, thus simplifying the circuitry required to read data. To use the controller in a system, just line buffers, a decoder, and a latch are needed.

Fabricated with the company's patented COPLAMOS n-channel silicon-gate process, the device operates from a 5-V supply and an 8-MHz clock and has a worst-case power rating of about 1 W.

The FDC9266 comes in a 40-pin DIP. It costs $25.10 in 100-unit quantities, and samples are available from stock.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N.Y. 11788; (516) 273-3100.

CIRCLE 304

Dave Bursky

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CIRCLE 148

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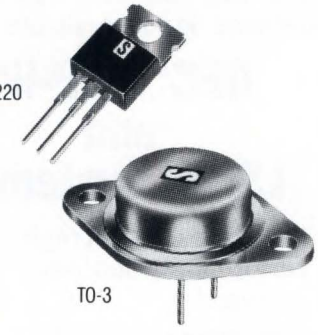

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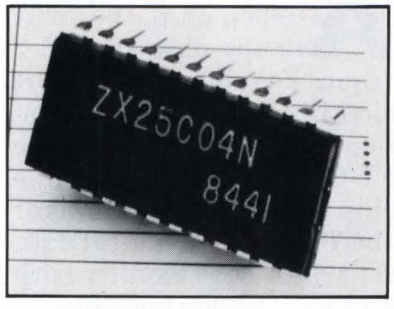
CIRCLE 149

DIGITAL ICs

SAR chip consumes 10% to 1% the power

With a power consumption of just a few milliwatts, a CMOS chip can directly replace the popular but power-hungry bipolar 2504 12-bit successive-approximation register. The first CMOS replacement for the bipolar SAR, the ZX25C04 dissipates just a tenth to a hundredth the power of its bipolar counterpart.



Developed by Zytrex, the chip is manufactured with the company's proprietary metal-gate, dual-layer-metal CMOS process, which provides high drive currents and performance equivalent to that of bipolar circuits.

The chip contains all the storage and control logic needed to build an analog-to-digital converter. Also, it has provisions for register extensions and truncations, and it can be operated in either a start-stop or a continuous-conversion mode, features that make it useful as the control and storage element for other recursive digital routines. Additionally, the chip can be set up to operate as a ring counter or as a serial-to-parallel counter.

Guaranteed to operate at a minimum clock frequency of 15 MHz, the device has a typical upper clock frequency of 60 MHz. At one clock pulse per bit, plus one bit per period for overhead, the 15-MHz clock frequency translates into slightly more than a 1-MHz conversion rate for a 12-bit a-d converter.

When the chip is not being cycled, the quiescent supply current is a mere 8 μA (all outputs open); that specification increases to several milliamperes when clocked. The register operates from a 4.5- to 5.5-V power supply and over $-40°$ to $+85°$C. The output voltage levels allow direct interfacing with other CMOS logic devices, as well as with TTL circuits.

Available in a 24-pin 300-mil DIP the SAR costs $6.90 apiece in 100-unit quantities. An unpackaged chip for use in hybrid circuits costs $6 each for a minimum order of 5000 units. Delivery takes six to seven weeks for packaged devices and less for bare chips.

Zytrex Corp., 750 E. Arques Ave., Sunnyvale, Calif. 94086; Orlando Gallegos, (408) 733-3973.

CIRCLE 305

Dave Bursky

DIGITAL ICs

Dual-port RAMS have largest byte-wide capacity

Available with either 8 or 16 kbits of storage space, a pair of dual-port RAMs offers the largest capacity of any byte-wide monolithic dual-port memories. What's more, the chips, made with Integrated Device Technology's CEMOS II 2-μm process, do not sacrifice access time for the low power of CMOS.

The best maximum access times are 90 and 100 ns for the commercial and military versions, respectively, and the typical power consumption is just 325 mW. When deselected, the standard version ("S" suffix) of either memory consumes just 200 μW; for even lower standby power requirements, an "L" suffix version draws only 50 μW.

Both chips—the 1-kbyte IDT7130 and 2-kbyte IDT-7132 have two independent address and data ports with separate control lines, thus permitting simultaneous read and write operations to any location in the memory. Each port also has its own chip-enable/power-down line, so that power can be saved if one port is not needed.

Busy output signals provide feedback to the host system by delaying access to one port when both ports try simultaneously to access the same location. If that occurs, an on-chip arbitration circuit will make a decision and set the Busy flag of the delayed port.

The IDT7130 includes interrupt output lines for each port. These lines make possible communication between ports or systems. However, they are not included on the 7132, since the pins are needed for the extra address line for each port.

The low-power version of the RAMs also permit them to retain data, even when powered by a 2-V battery. In that case, power consumption drops still further—to a bare 2.5 μW.

Both memories are available in models for the commercial, industrial, or military temperature range, with maximum access times of 90 or 100 ns (commercial) and 100 or 120 ns (military or industrial). The military units are 100% processed in compliance with MIL-STD-883, method 5004.

The chips come in either 48-pin DIPs or 48-contact leadless chip carriers. In 100-unit quantities and housed in a DIP, the 120-ns military parts cost $185 (8k chip) and $324 (16k chip). Samples will be available in the first quarter of 1985.

Integrated Device Technology Inc., 3236 Scott Blvd., Santa Clara, Calif. 95051; Sam McCarthy, (408) 727-6116.

CIRCLE 301

Dave Bursky

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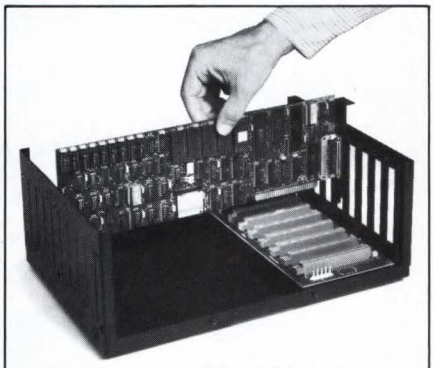

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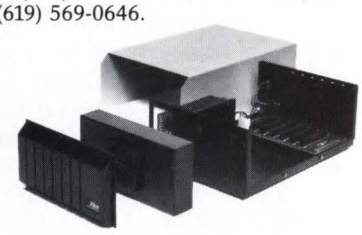

I-BUS SYSTEMS

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CIRCLE 150

DIGITAL ICs

Chip makes 80286 look like 8088

A single chip allows the 16-bit 80286 microprocessor to emulate the control signals and 8-bit transfer sequences of the 8-bit 8088 microprocessor. Thus the EL-286-88 processor converter chip, from Edsun Laboratories, gives 80286 systems designers easy access to the plethora of 8-bit IBM PC-compatible peripherals now available. It also serves the upgrading of 8088 systems by providing a ready link between the software-compatible 80286 and an 8088 bus and therefore speeding up the design time for such upgrades.

The converter translates data width, control signals, and circuit timing. Control inputs determine which memory address ranges and I/O devices the chip is to service and which are to be accessed directly by the 80286.

To the 80286, the converter appears as a 16-bit memory or peripheral device, and to the 8-bit peripheral it looks like an 8-bit 8086. Fully asynchronous operation allows the 80286 to run at its full 8-MHz clock rate and address peripherals designed for, and running at, typical 8088 data rates of 4.77 MHz.

The chip requires a single 5-V power supply. Implemented in CMOS, the TTL-compatible device dissipates 100 mW, with no heat sink required.

The converter will be available in sample quantities in January. It is housed in a 68-pin leadless chip carrier (the same as the 80286) and priced at $48 for orders of 10,000 units.

Edsun Laboratories, Inc. 7 Sears Road, Wayland, Mass. 01788; Steven Edelson, (617) 358-5667.

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CIRCLE 181

DIGITAL ICs

Phase controller comes in SO package

A phase controller IC, which includes a high triac drive suitable for a wide range of control applications, is housed in a space-saving small-outline package. The TDA2086, which is based on the TDA2085 16-pin dual-in-line-packaged controller, is approximately one-half the length and one-quarter the volume of conventional dual-in-line packages. In addition to its ability to drive high-power triacs, the chip features a 5-V supply for ancillary CMOS circuitry and a power consumption of 3.1 mA.

Plessey Solid State, 3 Whatney, Irvine, Calif. 92714; (714) 951-5212. $2.59.

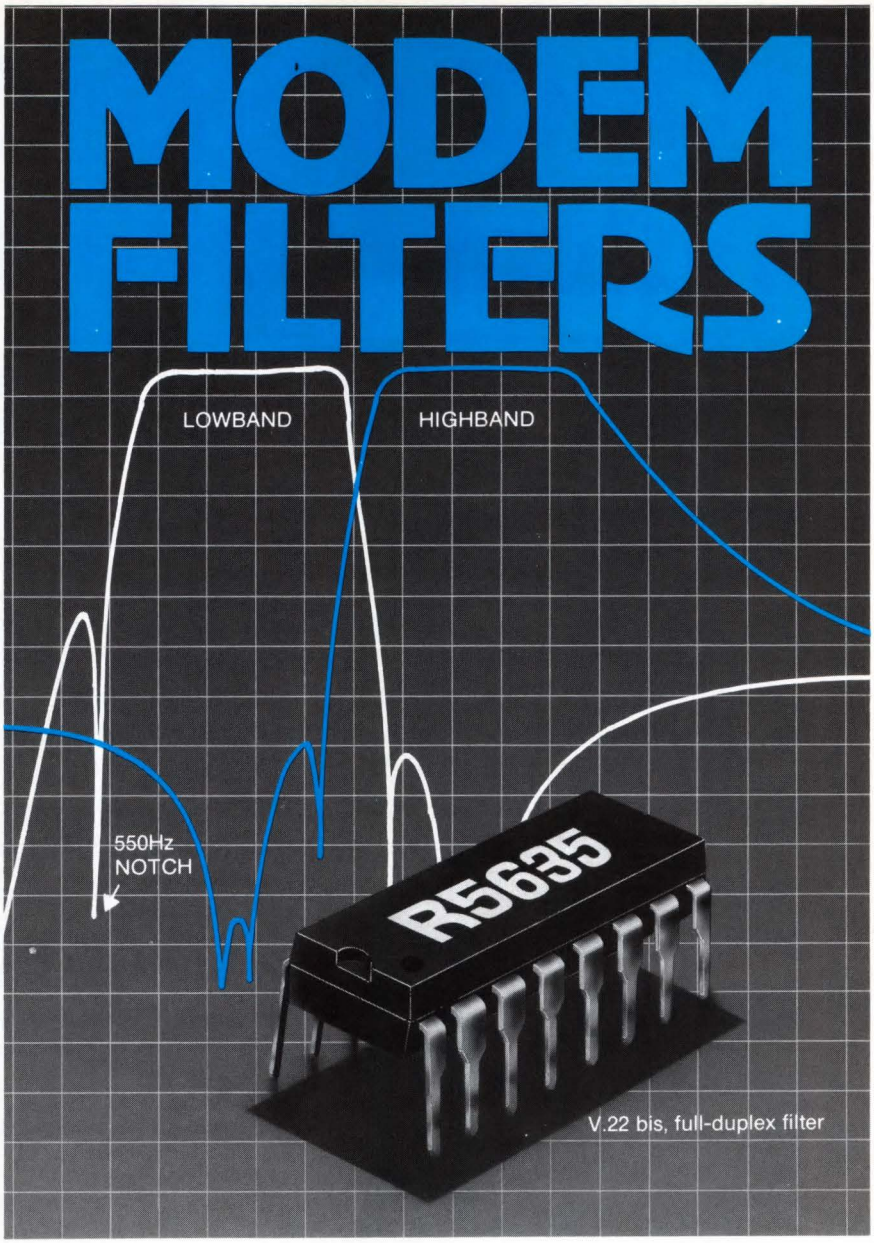
CIRCLE 326

Clock driver works at 2000 MHz

For driving high-speed GaAs circuits, the CD2.5A clock driver operates from dc to 2000 MHz, allowing random pulse trains of varying rates and duty cycles to be faithfully reproduced with a truly differential output of 2.5 V per side into 50 Ω. The output offset may be set anywhere between −4 and +2.5 V. The CD2.5A features rise and fall times (20% to 80%) of less than 75 ps and a gate on/off/on time of only 100 ps. A resistor divider can be used for ECL-compatibility.

Colby Instruments Inc., PO Box 84379, Los Angeles, Calif. 90073; (213) 450-0261; $2800.

CIRCLE 327



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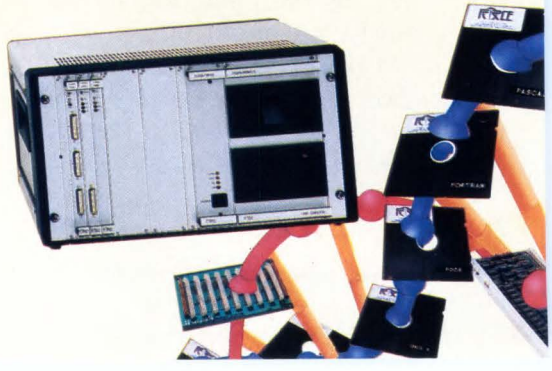
- Three CPU's for most applications from intelligent I/O controllers to multiuser/ multitasking environments with powerful UNIX* or real time operating software PDOS* and up to 1M byte of on-board memory: CPU-1B, CPU-2, CPU-3.
- Two DRAM Boards: 512KB and 2MB; two SRAM Boards: 128KB and 512KB. RAM/ROM Board: 512KB (max.); DRAM-1, DRAM-2, SRAM-1/2, RR-1/S/E
- Mass memory interface boards with either direct control of up to seven drives (WFC-1) or intelligent VMEbus interface to SASIbus with DMAC (SASI-1).
- Six-channel serial I/O board with Multi-Protocol-Communications-Controller (SIO-1).
- 32-channel parallel I/O boards either optically isolated (1000V) with DMAC (OPIO-1) or TTL-level with 64 mA drive capability signals (PIO-1).
- Intelligent high resolution graphics subsystem (master/slave) with resolution of 1024 x 1024 pixels and up to 12 bits of pixel depth. Powerful graphics operation through local 68000 MPU in parallel with 7220 graphics controller(s) GDC-1M/1S.
- Winchester/Floppy drive modules with up to 80M bytes: WFMOD-20/80.
- Auxiliaries: Backplanes, chassis, power supplies.
- A variety of Software Products, e.g.:
  PDOS* – Real-Time, Multi-Tasking, with Basic interpreter, Pascal, Fortran 77, and C Compilers.
  COHERENT* – UNIX* V.7 compatible with C Compiler, Pascal and Fortran 77 in preparation.
- UNIX* – System V, Multi-User, Multi-Tasking.
- In development: memory boards with byte parity and 32 bit addressing; dedicated LAN-Controller; high performance communication I/O.

Supported by a worldwide network of distributors and representatives, FORCE Computers is recognized by its customers (and competitors) as the leading supplier of 68000/VMEbus board products.

*PDOS is a TRADEMARK of Eyring Research, COHERENT is a TRADEMARK of Mark Williams Co., UNIX is a TRADEMARK of AT&T.

Consider, compare, and contact: FORCE COMPUTERS INC.



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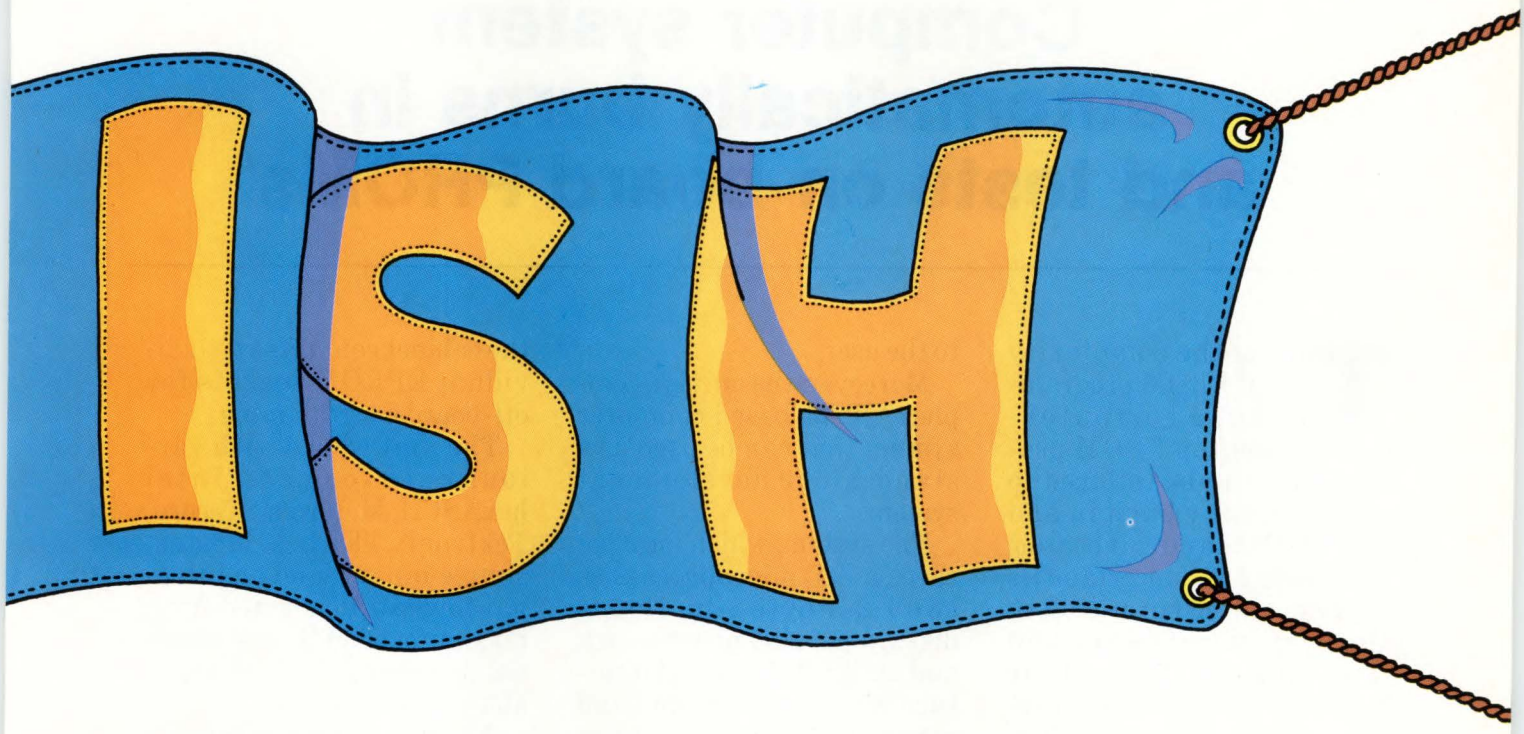

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A lot of PCB CAD/CAM systems may be able to get your PCB's to market. But only one can get you there before all the rest. Our MAXI DESIGN STATION. Partly because you won't have to struggle with start-up bugs. (MAXI has already designed *millions* of PCB's.) Partly because MAXI already has all the functionality others are promising. But mostly because MAXI will run 2-3 times faster than the others. So it can't help but finish first.

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CIRCLE 184

INSTRUMENTS

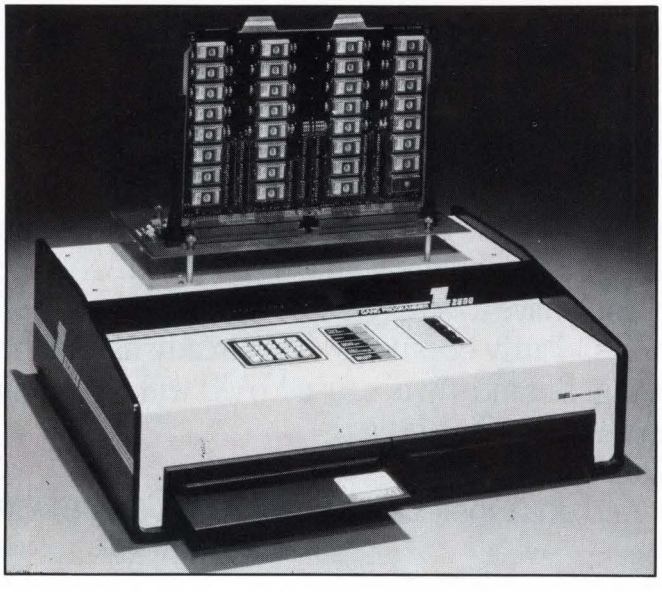
Computer system automatically burns in and tests on-board PROMs

Taking the complexity out of PROM programming, a computer-based benchtop PROM programmer can be tailored to automatically burn in and test PROMs on circuit boards, eliminating the uncertainties of premounting burn-in. Both the system software and mounting interfaces of the Z-2500 in-circuit memory programming system, from Sunrise Electronics, can be modified at the factory to meet special requirements, thereby delivering a turnkey system to the user.

Ray Weiss

Moreover, the unit is a complete CP/M-based computer system that can be used as a stand-alone development system.

The system, which incorporates a Z80 microprocessor, two 1.2-Mbyte 8-in. floppy disks, a parallel printer port, and an RS-232-C serial interface with a maximum baud rate of 19,200, can program multiple boards simultaneously and handles data paths of up to 32 bits. The interface adapter, mounted on a 96-pin connector, drives up to eight cards in parallel, and the cabinet contains two individual EPROM sockets for off-board programming.



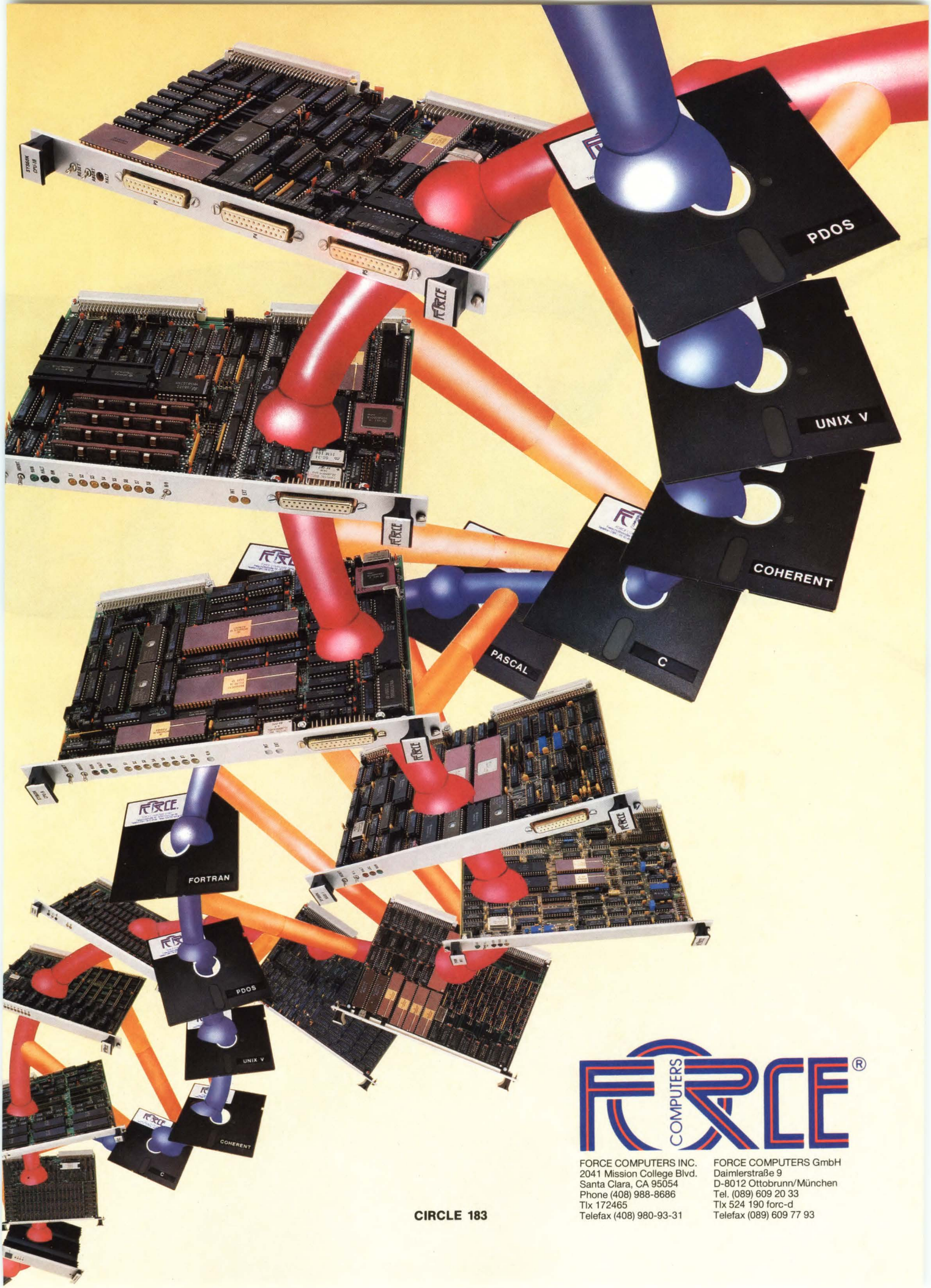
The unit works with various data formats: Intel hexASCII, Motorola S record, Tektronix TEKhex, Mostek, simple binary, and an internal format. It is rated for a maximum of 50 W, and external power supplies are available for more power.

A menu-driven interface lets the user direct the system and add or modify memory patterns. Source code is provided for the programmer's software, which is written in well-commented assembly language, so that the user can make modifications if desired. Also available is the assembler, as well as other CP/M-based software.

The programmer is available now, at a price of $16,500 for the base unit, with one-time modification costs of $2500 for a custom interface adapter design, $750 to $900 for the actual adapter, and $5000 to $7000 for a custom software package.

Sunrise Electronics Inc., 524 South Vermont Ave., Glendora, Calif. 91740; (818) 914-1926.

CIRCLE 315



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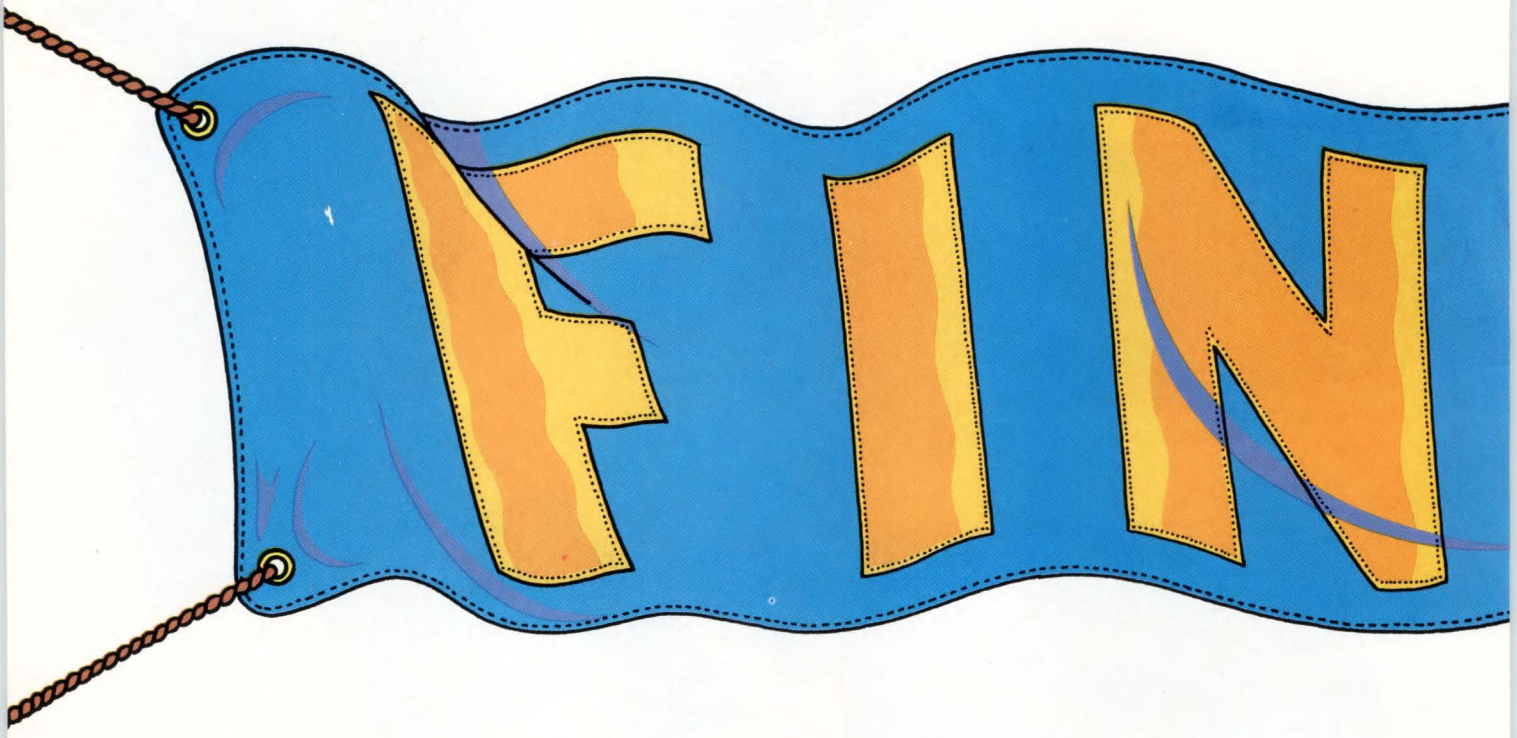
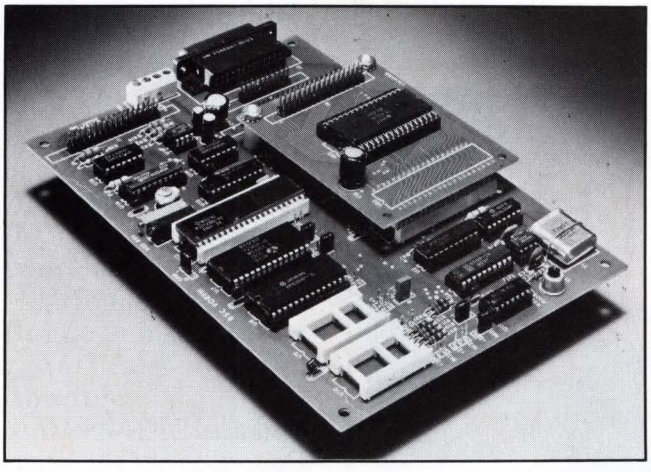

FIN

INSTRUMENTS

Board set aids programs for Forth μC chip



A simple board set eases the development of Forth programs for Rockwell's single-chip Forth microcomputer. The HE4TH-01-16K development system, built by Horne Electronics, provides a full programming environment for the R65F11 microcomputer, which contains in ROM the Forth-79 run-time routines.

The set uses Rockwell's R65010 microcomputer to emulate the more restricted chip, making possible the use of a full 16 kbytes of RAM for development. In addition, a development ROM and a Forth kernal ROM chip are used, creating a full Forth environment for the R65F11.

The main board contains a floppy-disk controller chip (the WD2793) capable of managing up to four quad-density, double-sided 5¼-in. floppy-disk drives. It also has a parallel printer port, an RS-232 port, a 40-pin connector for off-board expansion, a bank selection mechanism for off-board RAM, and a PROM burn-in capability.

The other member of the set is a piggyback board holding the R65010. It mounts onto the main board in a socket normally used for a R65F11.

The motherboard also can be used to develop Forth programs directly on the R65F11 processor.

The boards are available either as simple circuit cards or fully assembled and tested. All the necessary components to build a full development station are also available, including power supply, terminal, floppy disks, and cabinet. A single fully assembled and tested board set is priced at $585. Delivery is from stock.

Horne Electronics Inc., 8602 Bayonne Drive, Huntington Beach, Calif. 92646; (714) 963-4182.

CIRCLE 316

Ray Weiss

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CIRCLE 185 FOR LITERATURE ONLY

CIRCLE 186 FOR IMMEDIATE APPLICATION

INSTRUMENTS

Scope calibrator is fully mobile

Typically, oscilloscopes have to be removed from their working environment and brought to the laboratory for calibration. Now, thanks to the 4003A-Mod 101 mobile automated calibration system from Ballantine Laboratories, such operations can be carried out right on the production floor.

Capable of calibrating oscilloscopes with bandwidths as high as 1 GHz, the system features a sweep range of 5 s/cm to 500 ps/cm, an amplitude range of 40 μV to 200 V, and a rise time as fast as 200 ps. Dubbed Calcart, it is built around an IBM PC with a high-resolution full-color display, dual floppy-disk drives, 256 kbytes of RAM, and an IEEE-488 interface. Rounding out the hardware is a bidirectional 160-char/s printer and the company's 6127BN programmable oscilloscope calibrator.

Equally important is the company's Computest software that ties the system together. The software features color-coded, menu-driven operation for ease of use.

During calibration, the software analyzes error data and gives quick pass or fail responses. Moreover, it supplies instructions on the action needed to correct the fault. When an instrument passes the checks, a calibration certificate is printed out.

The system is priced at $29,950. Delivery is in 30 to 45 days after receipt of an order, and versions containing the necessary sources to fully calibrate digital multimeters also are available.

Ballantine Laboratories, Inc., PO Box 97, Boonton, N.J. 07005; (201) 335-0900.

CIRCLE 312

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Solve your telecommunications design problems with Teltone's complete family of telecom IC's. You'll find innovative, up-to-the-moment single-chip and hybrid generators, detectors, receivers and relays — all backed by Teltone's commitment to performance, reliability and quality.

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A reputation for telecom innovations. Rounding out our complete family of telecommunications components are the M-949 Line Sense Relay and the M-959 Dial Pulse Counter and Hook Status Monitor. The M-949 is a small PWB-mount loop current detector that, when connected to the tip and ring voice pair of an ordinary telephone line, responds to currents of 18-125 mA with a 1 form A relay closure. The CMOS M-959 features independent hook status monitoring and includes time-guarded dial pulse counting and pin-selectable dialing speeds of 10 or 20 PPS.

For more information on components from the leader in telecom technology, call Teltone today: **1-800-227-3800, ext. 1130.**

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CIRCLE 187

INSTRUMENTS

100-kHz signal analyzer is versatile

Users who work with frequencies between dc and 100 kHz can now avail themselves of a single instrument that excels at network, spectrum, and waveform analysis. The HP 3562A from Hewlett-Packard features an 80-dB dynamic range, built-in noise and sine-wave sources, an amplitude accuracy to within ±0.15 dB, and a frequency resolution of 25.6 μHz. What's more, its two input channels are matched to within ±0.1 dB for amplitude and to within $\pm 0.5^0$ for phase.

For network analysis, the analyzer offers three measurement techniques: linear-resolution FFT, logarithmic resolution, and true swept sine wave. Moreover, block-operation waveform math can be used to normalize network measurements or compute secondary functions.

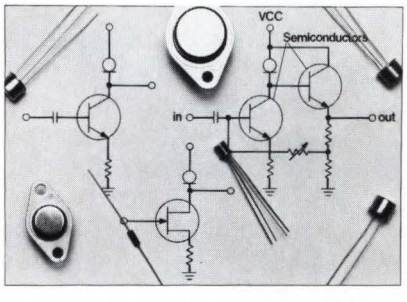
When spectrum analysis is needed, the unit's speed and accuracy permit on-line determination of distortion, drift, modulation, and phase noise. Furthermore, time and frequency traces may be displayed simultaneously, or one trace may be used to display a 100-kHz spectrum while the other trace zooms in on a portion of the spectrum.

Complete analysis of time waveforms and transients is simplified by two modes. Time capture uses the instrument's internal memory as a 20,000-sample buffer, and time throughput stores sampled data on an external disk drive.

The HP 3562A is priced at $23,900. Delivery takes 16 weeks.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Road, Palo Alto, Calif. 94303.

CIRCLE 311



Constant Current Sources

☐ Teledyne Crystalonics, the leading producer of constant current sources (CCS), offers a full range of two terminal devices, both standard and special.
☐ The array of devices includes the popular FET CCS's in the DO-7 package (1N5283-1N5314, also available as JAN, JANTX and JANTXV and CIL-250 series) which have values from 0.2 to 10 mA. Higher current FET CCS's, to 50 mA, are supplied in the TO-5 package.
☐ Other devices are offered in various TO packages from 1 μA to 1 amp current levels with peak operating voltages to 1000 V.

Some applications of these devices are:
- Active load, biasing and coupling resistors
- Waveform generators (triangle, square, sawtooth, stairstep)
- Low noise, low voltage, zero T/C voltage references
- Non-destruct fuses
- Two-step battery chargers

Send for free application notes and data sheets.

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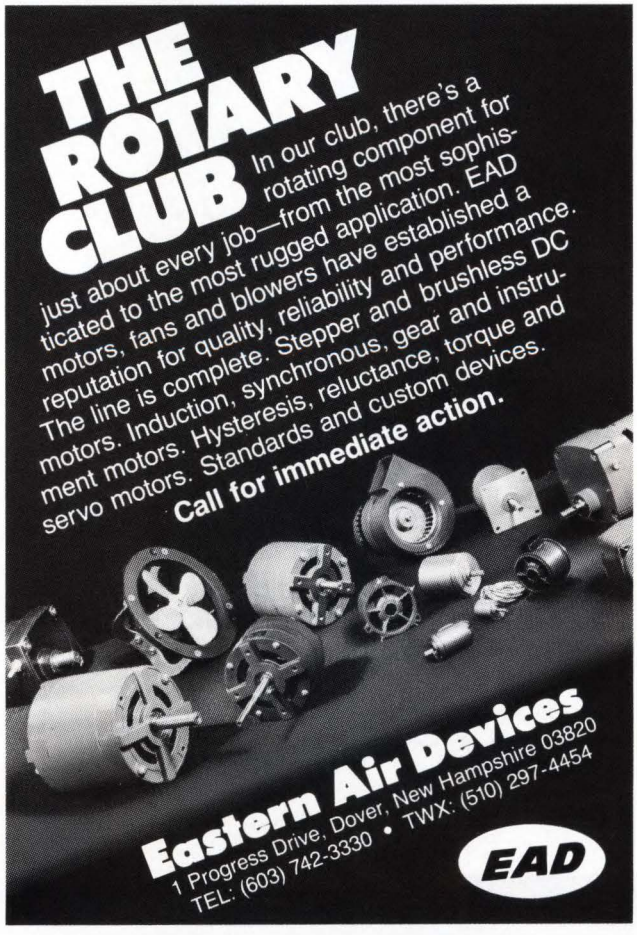
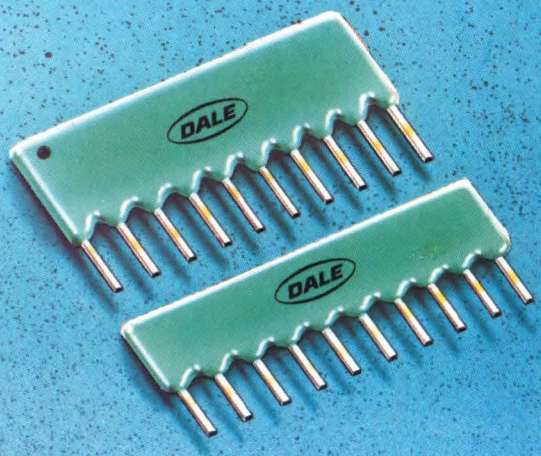


CIRCLE 189

Solutions



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Dale's CSC.

Low cost, plus the assured quality and delivery of Dale's ZIP program makes CSC thick film resistor networks tough to beat. These epoxy conformal coated networks are available in .195″, .250″ and .350″ aboveboard heights with 3 through 11 resistors (1 pin common) and 2 through 6 isolated resistors. Tolerances of 1%, 2%, 5%, 10% and 20% are available in a range from 10 ohms to 3.3 megohms. Evaluate the CSC…as part of Dale's ZIP program. It's guaranteed to give you problem-free delivery and quality. Contact: Dale Electronics, Inc., Box 26950, El Paso, TX 79926.

For more details, call: **915-592-3253**

CIRCLE 190

Hybrid clocks are ready from stock.

Dale's XO-43.

We're ready to match your timing requirements from a ready-to-ship stock of clock oscillators in 23 standard frequencies —1.0 to 50 MHz. Dale XO-43 clocks will drive up to 10 TTL gates and are available in accuracies from .005% to 1% over a temperature range from 0 to 70°C. Input voltage is +5 VDC. Their rugged, resistance welded metal case provides a hermetic seal and requires minimum board space (.225″H x .600″L x .515W). Grounding for EMI shielding is also provided. For information on the frequency you need, contact Dale Electronics, Inc., 1155 West 23rd St., Tempe, AZ 85282.

For more details, call: **602-967-7874**

CIRCLE 191

Dale makes your basics better.

DALE

from Dale

Ultra-precise, compact and ready to ship

Dale's PTF

PTF thin film resistors let you package tolerances down to .01% in spaces as small as .175″ L. x .070″ D. PTF's are designed to meet MIL-R-122, and they're available from stock in 1/20, 1/8 and 1/4 watt sizes in a range from 10 ohms to 1 Meg. Count on PTF's for low levels of reactance and noise combined with an absolute T.C. as low as ±5 PPM/°C. They're available in matched sets... are automatically insertable...and very competitively priced. For details and application assistance, contact: Dale Electronics, Inc., 2300 Riverside Blvd., Norfolk, NE 68701.

Call this number: **402-371-0080**

CIRCLE 192

Here's how to replace RCR carbon comps

Dale's RLR

Better performance. Better delivery. Competitive price. If you need more reasons to move from carbon comps to RLR (Dale type ERL) metal film resistors, give us a call. We can help you forget about tolerance problems due to moisture absorption while you gain the added stability of MIL-R-39017's more stringent requirements...all in a size and value range that will match your present -05, -07 and -20 needs. It's worth your time to get all the facts and find out how much better we can serve you. Contact Dale Electronics, Inc., 2300 Riverside Blvd., Norfolk, NE 68701.

For complete information: **402-371-0080**

CIRCLE 193

Dale makes your basics better.

DALE

INSTRUMENTS

Logic analyzer operates at 100 MHz

To acquire timing data, most logic analyzers use fast, dedicated input channels that are separate from those used for state acquisition. In contrast, all 48 channels of Gould's K205 can operate at 100 MHz.

Not only that, the analyzer is fast enough and wide enough to serve the needs of the hardware designer debugging bit-slice, ECL, and gate-array designs. What's more, an optional user-definable disassembler, the A12520, enables users to capture and disassemble code from any nonstandard microprocessor or algorithmic state machine.

Sixteen independent triggering decision levels, with four commands at each level, take advantage of the unit's speed. Four decisions can be made every 20 ns, permitting designers to locate difficult problems by selectively triggering on a unique event.

Moreover, the instrument has a unique feature that speeds analysis by comparing timing sequences with stored references. For intermittent fault isolation and reliability analysis, multiple measurements may be automatically stored on the unit's disk drives.

The analyzer also has a glitch mode that displays transient noise on all of its channels. When this mode is enabled, a latching scheme maintains full channel width and memory depth.

The K105 is priced from $14,000. Delivery takes six weeks. The A12520 costs $950 and is delivered in 30 days.

Gould Inc., Design and Test Systems Division, 4600 Old Ironsides Drive, Santa Clara, Calif. 95050; (408) 988-6800.

CIRCLE 313

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Single board UNIX™ — Battle Proven

Designed for maximum power at minimum cost, the HK68™ — UNIX™MASTER — is a proven leader providing Multibus™ users more space, more speed, and more flexibility to apply to difficult design problems.

Powerful and versatile, the Heurikon HK68™, sports 68000/68010 CPU (8Mhz or 10Mhz), quad channel DMA controller, MMU, 128K, up to 1M byte of dual access RAM with parity, up to 64K bytes of EPROM, four RS-232-C ports (optional RS-422 on one port), winchester I/F, streamer tape drive I/F, eight user definable LED's, four dipswitches, and two iSBX™ connectors for further I/O expansion — all on a single board. Other operating systems available include PolyFORTH™, CP/M-68K™, Regulus™, and VRTX™.

Make your tough decision an easy choice. Call Heurikon direct 1-800-356-9602, in Wisconsin 608-271-8700

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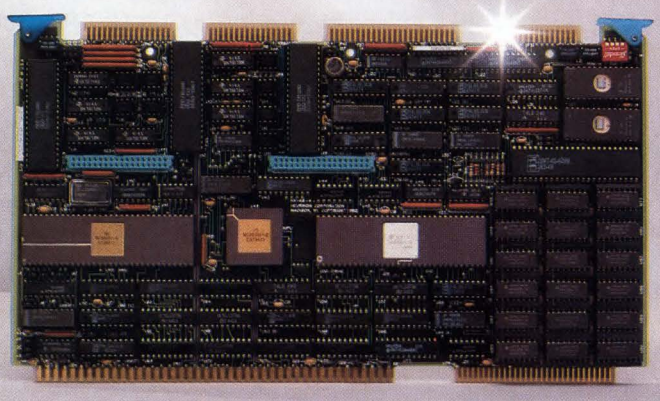

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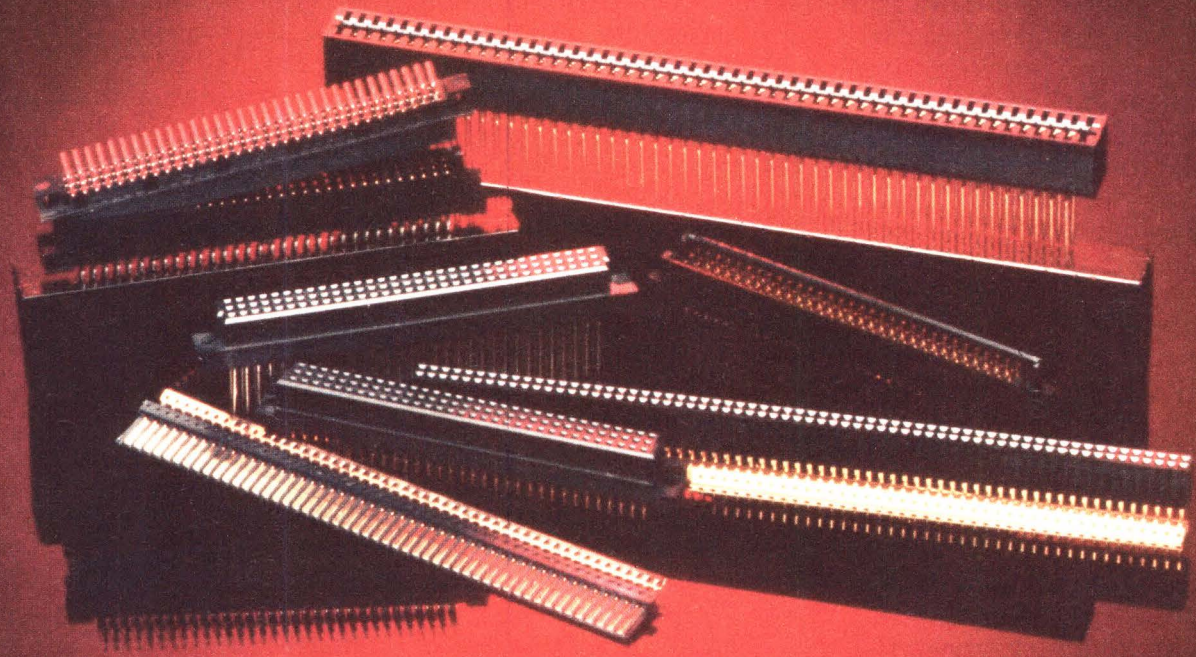

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CIRCLE 195

INSTRUMENTS

Scopes optimize industry-standard 2465

Improving on the powerful features of the industry-standard 300-MHz 2465 portable oscilloscope are three units that integrate five new measurement capabilities. In addition, the stand-alone scopes work equally well as controller-driven measurement packages. Designated the 2465 Special Editions, the instruments comprise a digital video system (DVS), a digital multimeter system (DMS), and a counter-timer system (CTS).

The DVS incorporates a talker/listener IEEE-488 interface bus, a counter-timer-trigger, a word recognizer, an autoranging digital multimeter, and television-waveform measurement capability. The DMS provides the same capabilities as the DVS, minus the TV function. Similarly, the CTS offers all but the TV and digital multimeter capabilities.

Tektronix Inc., PO Box 1700, Beaverton, Ore. 97075; (800) 426-2200 or (503) 627-9000. $8500, $7800, and $6600 for the DVS, DMS, and CTS, respectively.

CIRCLE 328

Port turns IBM PC into development system

An emulator port transforms the IBM PC XT into a universal development system for designing, testing, debugging, and implementing hardware and software for most popular microprocessor devices. The Kontron PC Interface (KPCI) package consists of hardware and a set of software development-support tools, including a cross assembler, a linker, and an emulator, as well as additional CP/M utilities. When an application program is completed, an optional Pascal compiler or assembler can process the edited source text. Once text editing is finished, the linker combines smaller modules into one main load module, which becomes an absolute binary module for loading and executing in the target system with the support of an emulator subsystem. The emulator connects to the IBM PC through the connector on the KPCI card.

Kontron Electronics, 630 Price Ave., Redwood City, Calif. 94063; (415) 361-1012. $1500; six weeks.

CIRCLE 329

Digital manometer has ±1.5% nonlinearity

Replacing basic hydrostatic models, a 3½-digit manometer measures pressure by means of a solid-state piezoresistive transducer. The unit achieves a full-scale accuracy to within ±1.5%, ±1 digit typical at 25°C. The primary measurement range is 0 to 10 in.H_2O, while other units of measure are transposed internally and displayed in kilopascals, mmH_2O, and mmHg—with respective ranges of 0 to 2.49, 0 to 254, and 0 to 18.7. Features include a zero-adjust calibration control, a hold function that freezes the display, and a continuity tester to verify circuit integrity.

Cleveland Controls Inc., Sensing Switch Division, 1111 Brookpark Road, Cleveland, Ohio 44109; (216) 741-9444.

CIRCLE 330

Portable calibrator works with IBM PC

Supplied with IBM PC-compatible software, the Model 4100 Portocal is an automatic calibration system designed for in-situ calibration of multimeters and automatic test equipment. The portable cart houses the Model 4000A (dc voltage, current, and resistance) and the Model 4200 (ac voltage and current) calibrators.

The system software provides menu prompts to guide the user through predefined calibration procedures. If the unit under test is one of Datron's Autocal series multimeters—or an IEEE-488-compatible instrument incorporating internal electronic calibration—the software automatically recalibrates it without removing the instrument cover.

Datron Instruments Inc., 3401 SW 42nd Ave., Stuart, Fla. 33494; (305) 283-0935.

CIRCLE 331

One of these Datel Sample-Holds can help you achieve your design engineering goals.

If your system's design calls for exceptionally accurate, high-speed sample and holds, then Datel has a precision device that can help you realize your design goals.

High Speed, High Accuracy

Our SHM-4860 is a 12-bit hybrid sample-hold that acquires a 10V input change to .01% accuracy in only 200 nsec.

The SHM-4860 is complete with internal hold capacitor and offers 60 nsec sample to hold settling time to .01% and an aperture uncertainty of only ±50 psec.

Applications Include: • Data Acquisition and Distribution Systems • Transient Recorders • Fourier Analyzers

Video Speed, Dual Output

Now you can order a new, low-cost sample-hold designed just for ultra-fast video data conversion. Our SHM-7 acquires a 2V input change to 0.1% in only 40 nsec with only 20 nsec hold-mode settling time, providing sampling rates of up to 17 MHz.

The SHM-7 features dual buffered outputs (±5V, 30mA, 13Ω). It's an ideal choice for two-stage conversion techniques.

Applications: • Parallel or Flash A/D Converters • Video Processing Systems • Radar Signal Sampling • Transient Analyzers

Low Cost, High Speed

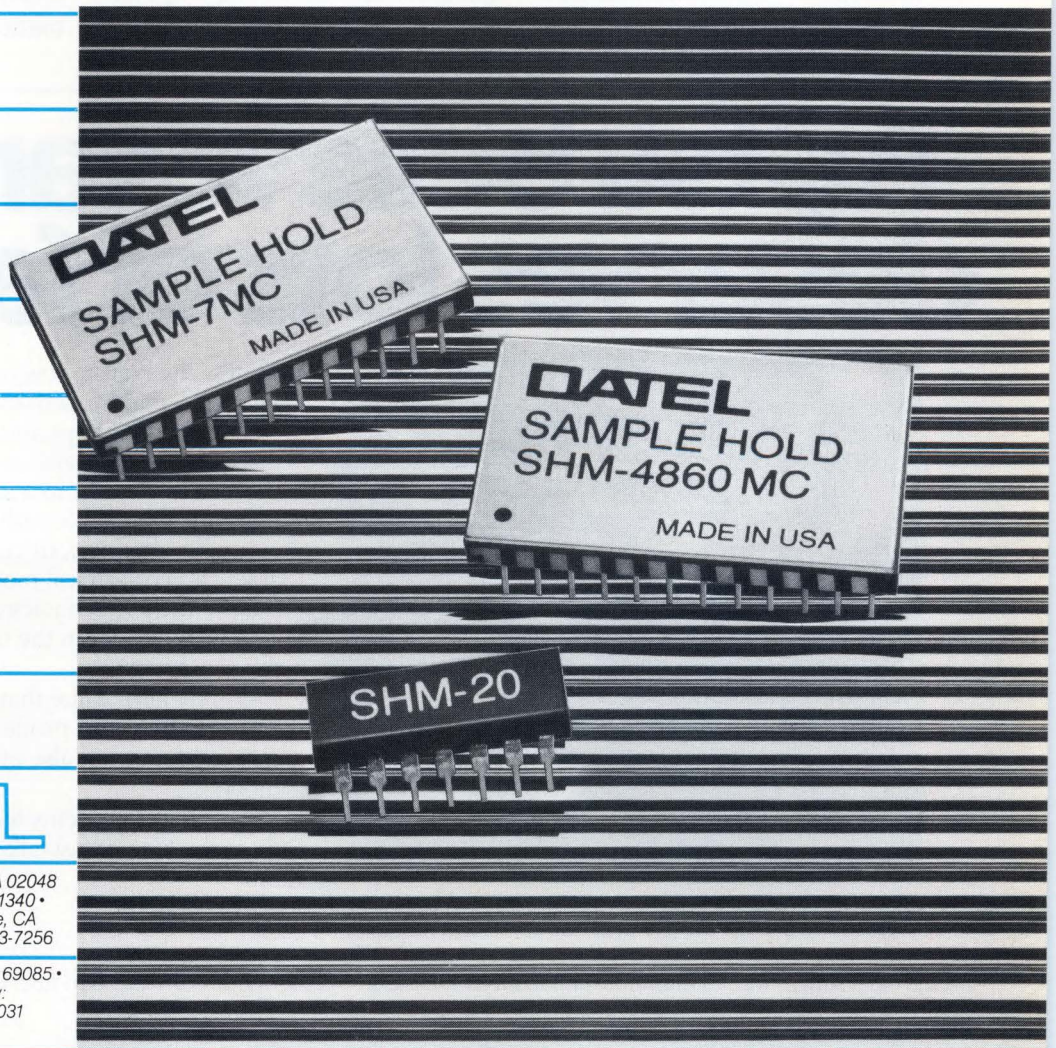
The SHM-20 is a low-cost, high-performance monolithic sample-hold designed for high-speed signal processing.

It features a typical 1.0 μsec acquisition time for a 10V step to .01%, with typical aperture uncertainty of 1.0 nsec.

Applications: • Data Acquisition and Distribution Systems • Deglitching Circuits • Auto Zero Circuits • Peak Amplitude Detectors

NOTE: For military and aerospace applications Datel's Sample-Holds can be subjected to rigorous screening procedures in accordance with MIL-STD-883, method 5008, Class B.

For your FREE Engineering Data Sheets call 617/339-9341 Extension 121, or write Mr. Bob Leonard, Applications Engineer, Datel, 11 Cabot Boulevard, Mansfield, MA 02048.



DATEL

USA: *11 Cabot Boulevard, Mansfield, MA 02048 617/339-9341 TWX 710-346-1953 TLX 951340 • Santa Ana, CA 714/835-2751 • Sunnyvale, CA 408/733-2424 • Los Angeles, CA 213/933-7256*

Overseas: *Datel/UK: Basingstoke (256) 69085 • Datel/France: 602-57-11 • Datel/Germany: (89) 530741 • Datel/Japan: (Tokyo) 793-1031 (Osaka) 354-2025*

CIRCLE 196

INSTRUMENTS

Unit performs digital, analog, discrete tests

The LTS-2020, a benchtop component test system, combines high-speed ac digital test capability with the ability to test analog circuits—including data converters—and discrete and passive components. The instrument executes instructions in approximately one-half the time of earlier LTS series testers, while maintaining 16-bit accuracy. It is programmed in Basic and can run programs developed on other LTS consoles. The LTS 2020 has 128 kbytes of memory—84 of which are available to the user.

Configured for ac digital testing with the LTS-2510 family board, the LTS-2020 costs $44,500 and is the only tester to offer ±1.5-ns accuracy and 500-ps resolution for under $80,000.

Analog Devices Inc., Component Test Systems Division, 10 Corporate Place, Burlington, Mass. 01803; (617) 273-4780.

CIRCLE 332

1-GHz scope aids high-speed logic design

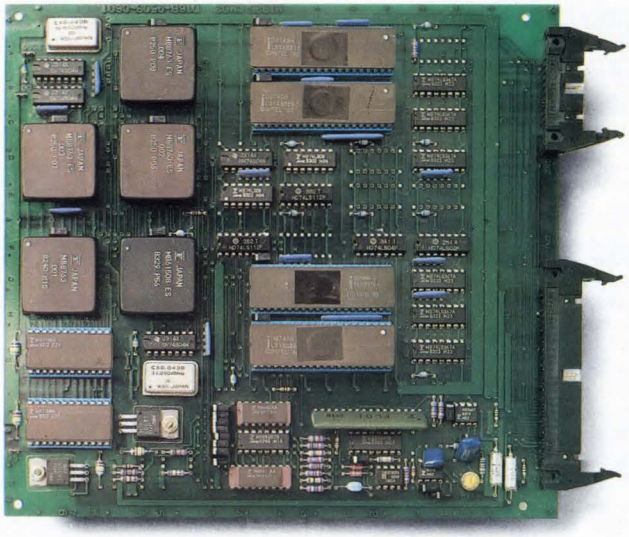
A fully programmable digitizing oscilloscope offers designers of high-speed logic circuits 1-GHz performance and 100-ps time-base accuracy.

The HP 54100 comes with two vertical channels and one or two trigger inputs, configured with removable pods. The scope automatically measures frequency, period, pulse width, transition times, and peak-to-peak amplitude. Sweep rates of 100 ps/division to 1 s/division allow the user to view both very fast and very slow events.

Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Road, Palo Alto, Calif. 94303; call local sales office. $17,600 (A) and $19,300 (D); four weeks (A) and eight weeks(D).

CIRCLE 333

Fujitsu believes an OEM deserves lots of fast talk.



The world's first 14.4 kilobit modem card; superior reliability in a compact package. 9,600, 4,800 & 2,400 bps core modems and stand-alone modems also available.

That's why Fujitsu now offers the world's *first* 14,400 bit per second modem card, along with companion 9,600 bps, 4,800 bps and 2,400 bps core modems. All three single PC boards employ custom digital signal processors. And from a standpoint of versatility, the units are compatible with *any* type of equipment.

By offering your customers the fastest, most reliable, and economical modem, you're not only offering state-of-the-art technology, but a product that is backed by a world leader in the telecommunications and computer industry.

We also realize that diversity sells your products and increases your profits. So, Fujitsu not only offers core modems, but also offers a full line of stand-alone modems.

Fujitsu modems meet the future head on. And that's the kind of fast talk you deserve.

FUJITSU

Fujitsu America, Inc. • Data Communications Division • 3055 Orchard Drive, • San Jose, California 95134 • (408) 946-8777

CIRCLE 197

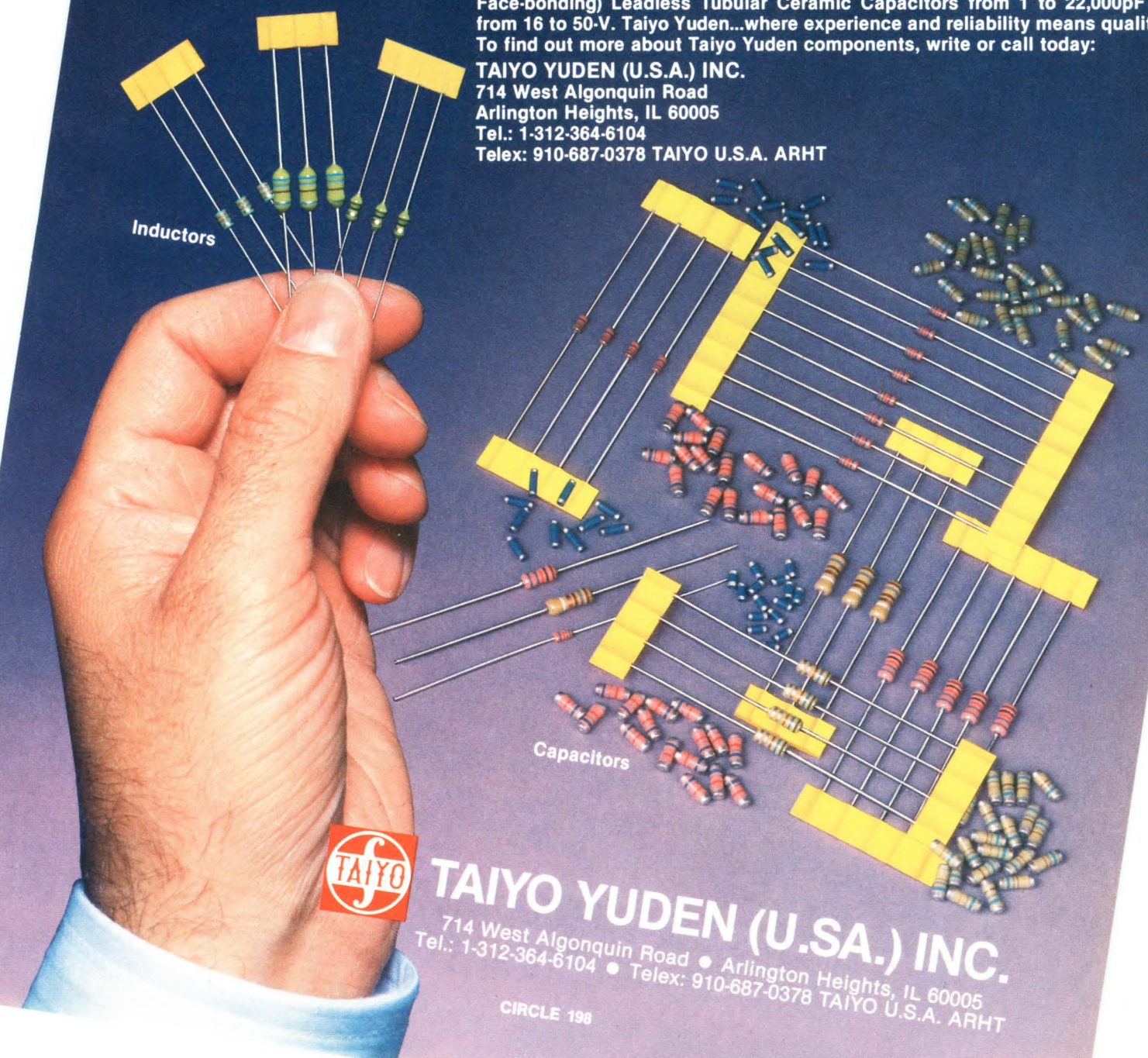
component reliability begins here

When you need Axial Leaded Tubular Capacitors with Single Layer Construction and Inductors...you want reliability and price. Taiyo Yuden provides both. And what's more, axial leaded components from Taiyo Yuden are available in three sizes with lead spacing as close as 200-mils.

Now manufactured in southern California to give you instant delivery, Taiyo Yuden components are specifically designed and sold for use in automatic insertion equipment.

No matter what your specs, Taiyo Yuden offers you the broadest range of product...axial leaded inductors from 0.22 to 1000μh...Axial Leaded Tubular Ceramic Capacitors from 1 to 33,000pF & 12 to 50-V...Melf (Metal Electrode Face-bonding) Leadless Tubular Ceramic Capacitors from 1 to 22,000pF & from 16 to 50-V. Taiyo Yuden...where experience and reliability means quality. To find out more about Taiyo Yuden components, write or call today:

TAIYO YUDEN (U.S.A.) INC.
714 West Algonquin Road
Arlington Heights, IL 60005
Tel.: 1-312-364-6104
Telex: 910-687-0378 TAIYO U.S.A. ARHT



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714 West Algonquin Road • Arlington Heights, IL 60005
Tel.: 1-312-364-6104 • Telex: 910-687-0378 TAIYO U.S.A. ARHT

CIRCLE 198

EHVQ™ SWITCHING POWER SUPPLIES WITH OPTIONAL BATTERY BACKUP

Optional battery backup in a switching power supply - a unique idea? Not according to our customers. With an EHVQ™ in your UNIX™ based system, lost data bases are a thing of the past. Our battery backup board has enough status signals to make interface with any operating system an easy job for hardware and software designers.

Other applications include industrial controls, point of sale systems, and medical electronics. Any system needing protection against brownouts or power failures can use an EHVQ™. Best of all, the battery backup is a field upgradeable option. The backup board plugs into your system's EHVQ™ as easily as adding more memory.

Write or call for information about our EHVQ™ evaluation kit. TII Electronics EHVQ™ switchers...

HELPING YOU BEFORE YOUR CHIPS ARE DOWN.™

170, 220, 360 Watt Models					
OUTPUTS					
MODEL NO.	MAIN	*AUX 1	AUX 2	AUX 3	SIZE
170 - 4	5V 15A	12V 4A	12V 4A	5V 1A	13.4 x 5 x 2.6
220 - 6	5V 25A	12V 6A	12V 4A	5V 1A	15 x 5 x 2.6
360 - 6	5V 45A	12V 10A	12V 5A	5V 1A	15 x 6.5 x 2.6
*AUX 1 capable of 4A surge for 20 seconds.					

Over 30 other single, double, triple and quad output models are available.
EHVQ™ Switchers are backed by a one year warranty.

TII® ELECTRONICS, INC.

226 Terminal Road, E. Setauket, New York 11733 516-751-6285

Circle **199** for literature Circle **200** to have applications engineer call

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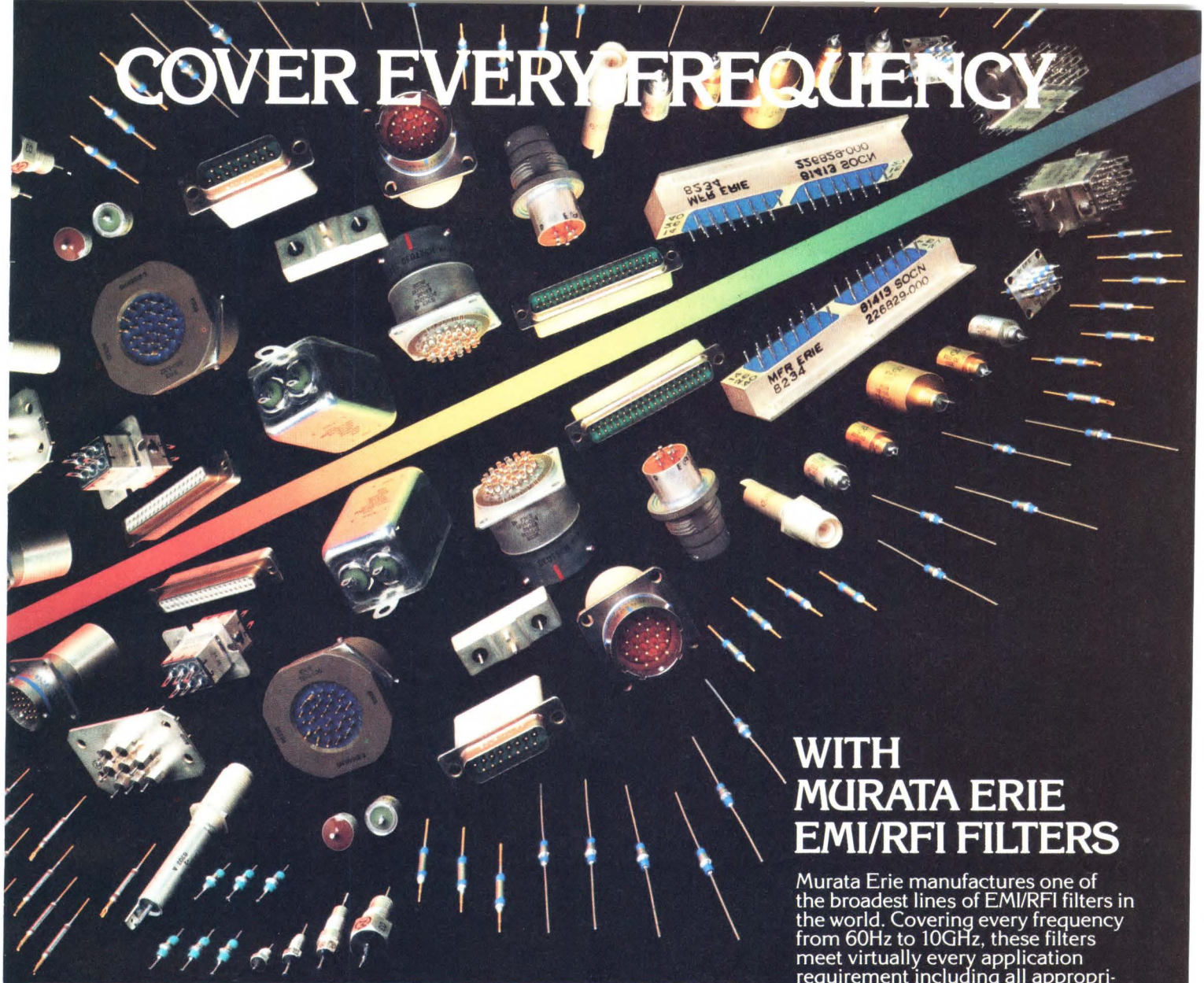
UNIX is a trademark of AT&T Bell Laboratories.

COVER EVERY FREQUENCY



WITH MURATA ERIE EMI/RFI FILTERS

Murata Erie manufactures one of the broadest lines of EMI/RFI filters in the world. Covering every frequency from 60Hz to 10GHz, these filters meet virtually every application requirement including all appropriate MIL specifications. Feed thrus, low pass and power line filters, as well as a complete line of filter connectors are all available. These filters are all backed by a Quality Assurance program that meets or exceeds the requirements of MIL-Q-9858 and DND-1015.

Murata Erie also specializes in custom-designed filters for special applications and maintains a complete in-house staff of experienced application engineers to aid in solving the most difficult EMI/RFI problems.

FILTER TYPE	MILITARY STANDARD	INSERTION LOSS PER MIL-STD-220				
		100KHZ	1MHZ	10MHZ	1GHZ	10GHZ
Feed-Thru	MIL-C-39014			5db	40db	60db
Solder-in Pi	MIL-F-15733		5db	50db	60db	60db
Threaded Bushing Pi	MIL-F-15733		5db	50db	60db	60db
Coaxial Feed-Thru	MIL-C-83439	19db	35db	55db	70db	70db
Coaxial LT	MIL-F-15733	27db	57db	70db	70db	70db
Coaxial LB	MIL-F-15733	28db	44db	60db	70db	70db
D Connector	MIL-C-24308		2db	20db	55db	50db
Multi-Network (6 line)	MIL-F-15733			10db	50db	50db
Multi-Network (12 line)	MIL-F-15733			5db	50db	50db
Cylindrical Connector	MIL-C-38999			20db	60db	55db

To receive complete technical information on Murata Erie's comprehensive line of EMI/RFI filters, write to Murata Erie North America, Inc., 1148 Franklin Road, SE, Marietta, Georgia 30067 or call 613-392-2581.

Regional Sales Offices:
West—714-835-4822
Southeast—305-644-0954
Central—312-297-5560
Northeast—617-245-7880
Canada—416-676-9484

CIRCLE 203

muRata ERIE

MURATA ERIE NORTH AMERICA, INC.

INSTRUMENTS

Low-cost unit programs wide range of EPROMs

The Model 21A programs over 120 different MOS and CMOS EPROMs and EEPROMs having densities of up to 256k. At $1450, the unit offers a variety of features that are commonly found only in higher-priced programmers.

The 21A features comprehensive test facilities to guarantee reliable programming. On power-up, a self-diagnostic routine checks the internal RAM and ROM, the front-panel display, the microprocessor, and the serial I/O port. Before programming, the 21A monitors devices for programmed bits and protects them from overvoltage, overcurrent, and incorrect insertion. After programming, the unit checks for V_{CC} margin and correct output polarity, as well as calculating a check sum of the programmed data.

Data I/O Corp., 10525 Willows Road NE, Redmond, Wash. 98073; (206) 881-6444. Two weeks.

CIRCLE 334

In-circuit emulator carries low price tag

Designed to provide engineers with a portable stand-alone instrument for developing, testing, and maintaining 6502-based hardware and software, the DA6502-B in-circuit emulator costs less than $600—considerably lower than comparable units. With the DA6502-B, the user can examine processor registers, read and modify memory locations, halt a program at a specific address, step through a program one instruction at a time, and stop a program at a location after a number of loops have been completed.

The unit comprises a 6¼-by-7½-by-3½-in. terminal with a keyboard and a display, emulator logic and program, a 6502 microprocessor, a bus switch that connects the emulator to the user's system, and a power supply. Its 24 functions are invoked by simple one- and two-keystroke sequences.

Da-Tech Corp., 92 Steamwhistle Drive, Ivyland, Pa. 18974; (215) 322-9410. $595 (OEM discounts available); 30 days.

CIRCLE 335

At last, benchtop accuracy and stability in a portable voltage calibrator.

The smallest, most dependable and most accurate microprocessor-based voltage calibrator on the market today is Datel's Model DVC-350.

Don't let its size fool you. The DVC-350 is a precision instrument. Its overall accuracy of 0.015% @ 25°C traceable to NBS is comparable to many expensive benchtop instruments.

The DVC-350 is ideal for remote site calibration and laboratory use for the calibration of DPMs, strip chart recorders, oscilloscopes, data acquisition systems, A/D and V/F converters, test set-ups, breadboarding and many other applications. Wherever accuracy and portability are required.

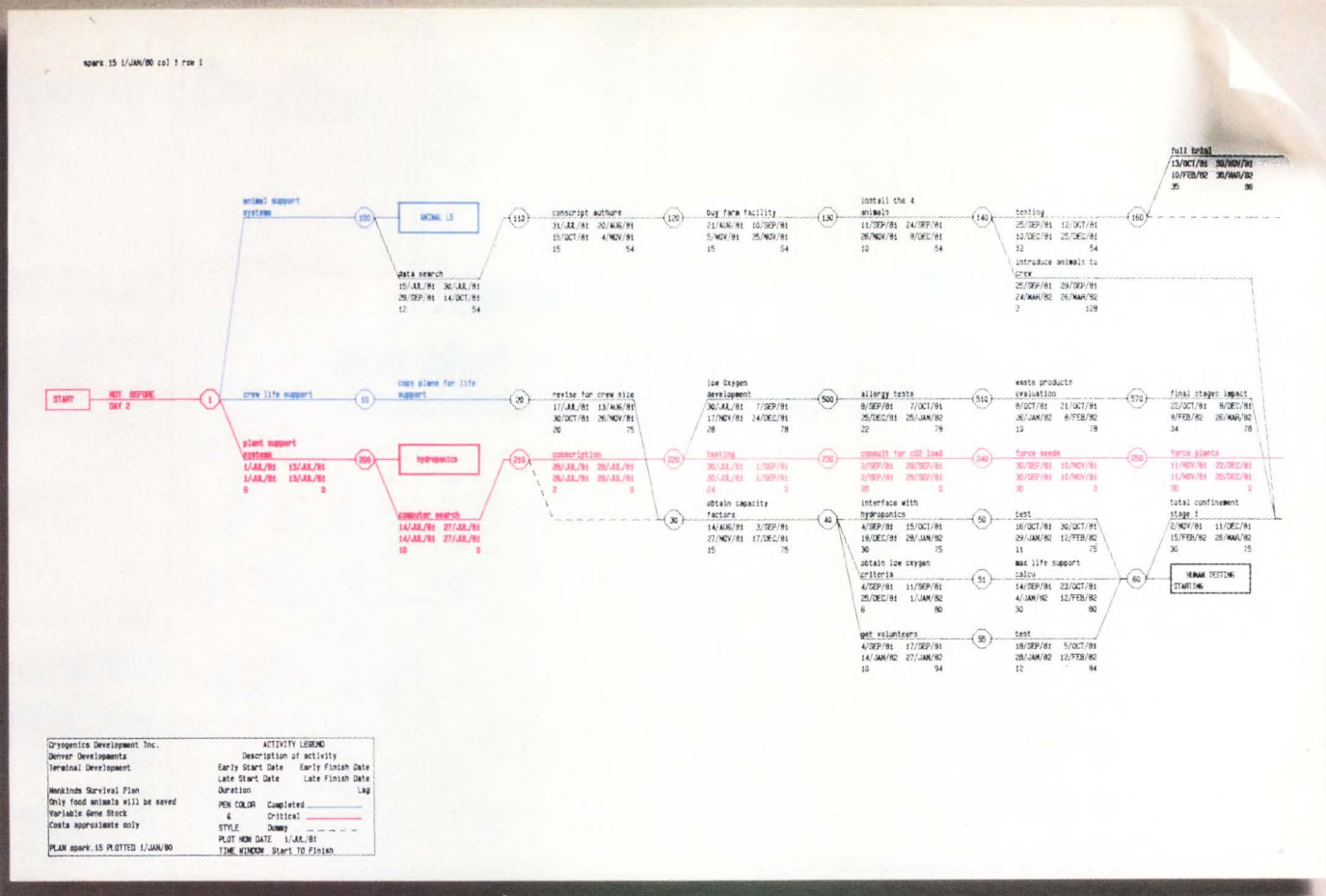
Why pay more for less performance? At $369.00, the DVC-350 offers...

- *True portability*
- *Battery operation*
- *Laboratory accuracy of ± .015%*
- *± 12.000 volt output range*
- *100 μV resolution*
- *20mA current limited drive capability*
- *Inherent isolation*
- *Microprocessor controlled functions*
- *Decimal and hexadecimal output modes*

If you're looking for true portability, but can't afford to sacrifice accuracy, Datel's new DVC-350 is the Voltage Calibrator you've been looking for. To order or for more information contact: Datel, 11 Cabot Blvd., Mansfield, MA 02048 (617) 339-9341.

DATEL

CIRCLE 204

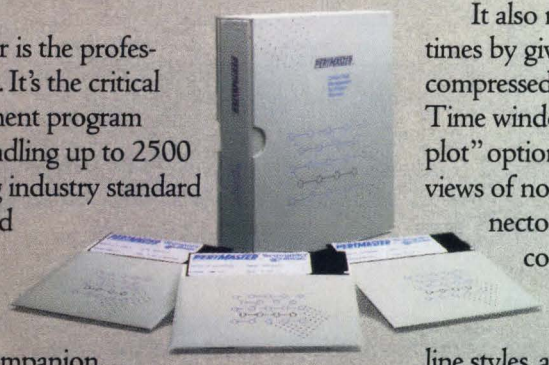


Tear along the plotted line.

And rip through deadlines in record time. With Pertplotter,™ the new network logic plotting program designed to complement Westminster's Pertmaster™ project management software.

Pertmaster is the professional's choice. It's the critical path management program capable of handling up to 2500 activities using industry standard notations. And Pertplotter is its logical extension and perfect companion.

That's because Pertplotter can plot and print logic diagrams of up to 500 activities in Arrow or Precedence notation. Using a variety of easy-to-follow colors that help monitor the progress of your projects from concepts to completion.



It also reduces plot times by giving you highly compressed logic diagrams. Time windowing. A "fast-plot" option for quick views of nodes and connectors. And full control of title block, activity data content, line styles, and much more.

And at $495.00, we don't think you can afford to wait. Just call us or

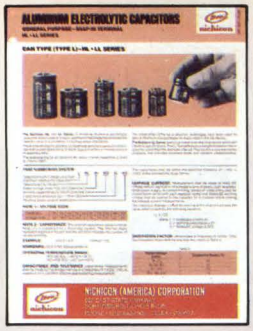
your local Pertmaster dealer for more information: *(415) 424-8300.*

PERTMASTER™
by Westminster Software

Westminster Software, Inc.
660 Hansen Way, Suite 2
Palo Alto, California 94304

**Pertplotter is compatible with the IBM™ PC graphics printer, most Epson™ and HP™ dot matrix printers and HP's 747X series pageplotters, with many more to follow.*
Pertmaster and Pertplotter are trademarks of Westminster Software, Inc.

CIRCLE 205



At Nichicon, we want to help you find your capacitor choice.

Miniature Aluminum Electrolytic Capacitors

Series Type	Feature	Operating Temp. (°C)	D.C. Leakage Current (μA)	Construction	Rated Voltage Range (V.DC)	Capacitance Range (μF)	Standard Capacitance Tol. (%)
LB	• Standard Size • General Purpose	−40~+85	0.03CV (A*) (4μA Min.)	Radial (U)	6.3~100	0.1~10,000	±20 (M)
				Axial (T)	6.3~100	0.47~33,000	±20 (M)
VX	• Smaller Standard Size • High CV Density • General Purpose	−40~+85	0.01CV (B*) (3μA Min.)	Radial (U)	6.3~100	0.47~10,000	±20 (M)
HU	• High Voltage	−25~+85	0.06CV + 10 (C*)	Radial (U)	160~450	1~100	−10~+50 (T)
				Axial (T)	160~450	1~470	−10~+50 (T)
BU	• High CV Products	−40~+85	0.02CV (C*) (3000μA Max.)	Radial (U)	6.3~100	1,000~3,300	±20 (M)
VS	• Low Profile Design	−40~+85	0.01CV (B*) (3μA Min.)	Radial (U)	6.3~50	0.1~4,700	±20 (M)
KB	• Low Leakage • Tantalum Replacement	−40~+85	0.002CV (B*) (0.4μA Min. − U) (1μA Min. − T)	Radial (U)	6.3~100	0.1~100	±20 (M)/±10 (K)
				Axial (T)	6.3~100	0.47~100	±20 (M)/±10 (K)
SA	• Super Miniature (7mm Height) • Tantalum Replacement	−40~+85	0.01CV (B*) (3μA Min.)	Radial (U)	6.3~50	0.1~100	±20 (M)
SL	• Super Miniature (7mm Height) • Tantalum Replacement • Low Leakage	−40~+85	0.002CV (B*) (0.4μA Min.)	Radial (U)	6.3~50	0.1~100	±20 (M)
SP	• Super Miniature (7mm Height) • Non-Polarized	−40~+85	0.05CV (B*) (10μA Min.)	Radial (U)	6.3~50	0.1~47	±20 (M)
MA	• Ultra-Miniature (5mm Height) • Tantalum Replacement	−40~+85	0.01CV (B*) (3μA Min.)	Radial (U)	4~50	0.1~220	±20 (M)
EB	• Non-Polarized	−40~+85	0.01CV (C*) (5μA Min.)	Radial (U)	6.3~100	0.47~1,000	±20 (M)
				Axial (T)	6.3~100	0.47~3,300	±20 (M)

Miniature High Temperature Capacitors

PC	• Standard Size • Wide Temp. Range • General Purpose	−55~+105	0.03CV (A*) (4μA Min.)	Radial (U)	6.3~100	0.47~10,000	±20 (M)
		−40~+105	0.03CV (A*) (4μA Min.)	Axial (T)	6.3~100	0.47~10,000	±20 (M)
BB	• High Temperature • High Reliability	−40~+105	0.002CV (C*) (2μA Min.)	Radial (U) Axial (T)	10~100	0.47~1,000	±20 (M)
BE	• High Temp. (+125°C) • High Reliability	−40~+125	0.002CV (C*) (2μA Min.)	Radial (U) Axial (T)	10~50	0.47~470	±20 (M)
ST	• High Temp. (+105°C) • Super Miniature (7mm Height)	−40~+105	0.01CV (B*) (3μA Min.)	Radial (U)	6.3~50	0.1~100	±20 (M)

Miniature Special Application Capacitors

PX	• Low ESR • Smaller Package • High Ripple	−55~+105	0.03CV (A*)	Radial (U)	6.3~63	22~2,200	±20 (M)
TM	• For Timing Circuits • Very Stable at High Temp.	−40~+85	0.001CV + 1 (B*)	Radial (U)	10~50	1~470	±20 (M) ±10 (K)
HA	• High Frequency, High Ripple	−25~+85	100 (C*)	Radial (U)	25	2.2~10	±10 (K)

Can Type Lytics

HL/LL	• Snap-in Terminal for P.C.B. Mount	−40~+85	$3\sqrt{CV}$ (C*)	Can (L)	16~100	470~22,000	−10~+30 (Q)
UB	• Snap-in Term., P.C.B. Mount • Smaller Size	−40~+85	$3\sqrt{CV}$ (C*)	Can (L)	16~100	1,000~15,000	±20 (M)
NW/NK/NS	• Computer Grade	−25~+85	$3\sqrt{CV}$ (C*) (10mA Max.)	Can (L)	6.3~450	120~1,000,000 (1F)	−10~+50 (T)
PS [LR]	• Snap-in Term, P.C.B. Mount • For Switching Regulators • [Smaller Size]	−40~+85 (160~250) −25~+85 (350~450)	$3\sqrt{CV}$ (C*)	Can (L)	160~450 [400]	47~1,000 [47~330]	±20 (M)
PK	• High Ripple, Switching Reg. • Extended Temp. Range • Snap-in Term., P.C.B. Mount	−40~+105	$3\sqrt{CV}$ (C*)	Can (L)	200~250	150~1,000	±20 (M)
GM [GF]	• High Ripple, Switching Reg. • Extended Temp. Range • Snap-in Term., P.C.B. Mount • [Smaller Size]	−40~+105 (160~250) −20~+105 (400)	$3\sqrt{CV}$ (C*)	Can (L)	160~400 [400]	47~1,000 [47~330]	±20 (M)
FL	• Low Profile (20mm Height) • Snap-in Term., P.C.B. Mount • For Switching Regulators	−40~+85	$3\sqrt{CV}$ (C*)	Can (L)	160~250	82~270	±20 (M)

Class III Semiconductive Ceramics

Series Type	Temperature Characteristics	Rated Voltage (V. DC.)	Capacitance (μF)	Standard Capacitance Tolerance	Insulation Resistance (MΩ)	Dissipation Factor (at 1kHz)
HET	Y5T	12	0.022~0.47	±20% (M) +80~−20% (Z)	12V: 0.022~0.1μF −1 Min. 0.22μF −0.5 Min. 0.33μF −0.33 Min. 0.47μF −0.25 Min. 25V: 0.01~0.22μF −1,000 Min. 0.47μF −500 Min. 50V: −1,000 Min.	12V: 7.0% Max. 25V: 5.0% Max. 50V: 5.0% Max.
		25	0.01~0.1			
		50	0.01~0.1			
HEV	Y5V	12	0.047~0.47			
		25	0.022~0.47			
		50	0.01~0.1			

Polyester Capacitors

Series Type	Rated Voltage (V. DC)	Capacitance (μF)	Standard Capacitance Tolerance	Insulation Resistance	D.F.
QYA	100	0.001~0.47	±5% (J), ±10% (K), ±20% (M)	9.00MΩMin.	1.0% Max. at 1kHz
QXM (Radial)	250, 400, 630	0.01~2.2	±5% (J), ±10% (K), ±20%(M)	≤0.33μF-9.00 MΩMin.	1.0% Max. at 1kHz
QAM (Axial)	250, 400, 630	0.15~10	±5% (J), ±10% (K), ±20% (M)	>.033μF-3,000 MΩMin	
QAL	125V AC	0.0047~.022	±10% (K), ±20% (M)	9,000MΩMin. at 100 V. DC 1 Min.	1.0% Max. at 1kHz

(A*) = Leakage Current after 1 minute (B*) = Leakage Current after 2 minutes (C*) = Leakage Current after 5 minutes

nichicon
The capacitor choice.

NICHICON (AMERICA) CORPORATION
927 EAST STATE PARKWAY
SCHAUMBURG, ILLINOIS 60195
PHONE • (312) 843-7500 TELEX • 20-6577

CIRCLE 206

SOFTWARE

Automatic translators aid Fortran users

FACT, for Fortran Automatic Conversion Tool, provides automatic translation and documentation of Fortran programs from one computer to another and from one dialect to another. The program is currently available for converting VAX-11 Fortran into Data General Fortran 77, HP-UX Fortran/9000, Apollo Fortran, Gould Fortran 77+, IBM PC Professional Fortran, and Microsoft Fortran. Also available are tools for converting IBM Fortran IV into HP-UX Fortran/9000 and Data General Fortran 5 into Data General Fortran 77.

The translators may be purchased as stand-alone tools or as an integrated transportation package, including the documentation of operating system dependencies, optimization assistance, and more.

Softool Corp., 340 S. Kellogg Ave., Goleta, Calif. 93117; (805) 964-0560.

CIRCLE 337

Graphics program creates scientific plots

Running on an IBM PC or PC-compatible computer, a general-purpose high-resolution graphics program makes screen and printer graphs for scientific and financial applications. With PCPLOT software, users can create linear, semilogarithmic, and full logarithmic plots in any combination of the X axis and the two Y axes. Forced scaling and automatic scaling is supported in any combination of the three axes. Up to four plots can be made on the same graph using optional legends. PCPLOT is completely menu-driven and program-prompted.

BV Engineering, 2200 Business Way, Suite 207, Riverside, Calif. 92501; (714) 781-0252. $62.95

CIRCLE 338

CIRCLE 207

SOFTWARE

Software tools let IBM PC talk

The SoundWare series of software not only allows an IBM PC XT to perform telephone answering and management activities, but it also permits software developers to write applications with voice communication capabilities. The series includes a voice communication card, VoiceMate telephone management software, and programming software called SoundTools.

Used in conjunction with VoiceMate, the Communicard records high-quality voice onto a hard disk. Once the telephone is plugged into the card's RJ11 connector and the card plugged into a half slot of the computer, the user need only speak into the handset to record a message.

For customizing applications, SoundTools offers function calls that include Record A File, Play A File, Receive A Touch Tone Digit, and Generate A Touch Tone Digit. It can be used with several programming languages, such as MS Basica, C, assembly, and MS Pascal.

Digital Pathways Inc., 1060 E. Meadow Circle, Palo Alto, Calif. 94303; (415) 493-5544. $449.

CIRCLE 339

Interface program guides Unix users

SoftShell, a simplified user interface, allows users to take full advantage of the Unix operating system's considerable capabilities. The program provides templates to facilitate choosing options for all major commands, a structured "walk" to traverse the many layers of the Unix file system, and context information to orient users at all times within the Unix system. SoftShell also serves as a screen handler and a menu driver.

SoftShell divides the CRT screen into two parts: a window and a scroll. The desired Unix command, including parameters and options, can be entered directly into the scroll. If the command is known, but not its arguments, the user can invoke a special template that appears in the window to prompt him for the correct information.

Logical Software Inc., 17 Mount Auburn St., Cambridge, Mass. 02138; (617) 864-0137.

CIRCLE 340

Program adds photos to data-base systems

Merging photographs with data-base management systems is a product called PhotoBase, an operating system extension that runs on an IBM PC or PC-compatible computer. The types of pictorial information incorporated into a data base might include photographs of people, signatures and fingerprints, components, charts and graphics, or laboratory setups. Any data-base system that writes to the display using the computer's BIOS will work with Photo-Base.

Photos are created using high-quality pictures captured from a VCR or video camera by the PhotoBase image manager and the PC-Eye video capture system (sold bundled for $690). A high-resolution graphics adapter ($695) and a composite monochrome monitor are also required.

Chorus Data Systems Inc., 6 Continental Blvd., Merrimack, N.H. 03054; (800) 624-6787 or (603) 424-2900.

CIRCLE 341

Development tools ensure reliability

Based on the standard real time language RTL/2, the microMagic system provides users of PDP-11, VAX, or Professional 350 computers with reliable development software for embedded 16-bit microprocessor applications. Its extensive set of tools performs checks at each stage of program development to ensure system integrity and keep development and debugging time to a minimum. The combination of a standard language and a run-time executive provides an easy transition path between different target systems.

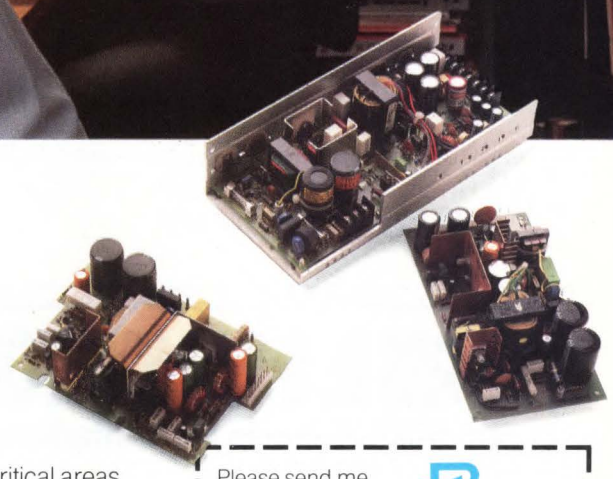
In addition to the RTL/2 compiler for the host machine, the microMagic system includes an RTL/2 cross compiler for 8086, 6809, 68000, LSI-11, or Falcon processors.

Intelligent Industrial Systems Inc., 300 Harmon Meadow Blvd., Secaucus, N.J. 07094, (201) 865-6550.

CIRCLE 342

"BOSCHERT'S FULL LINE OF HIGH PERFORMANCE POWER SUPPLIES BEGINS WITH HIGH PERFORMANCE ENGINEERING!"

Chuck Forge
Chief Engineer, Boschert Inc.



"A quality, long lasting product is not just an engineering objective at Boschert; it's a corporate directive. And has been ever since Boschert pioneered switching power supplies for OEM applications 10 years ago.

"In fact, each Boschert design must meet corporate guidelines for low failure rate, high performance and long life. *PLUS,* it must be manufacturable at a competitive cost.

"Meeting these objectives takes longer and costs more up front, but the end result is a more reliable product with a lower overall cost to the customer.

"That's why Boschert annually invests about eight percent of its revenues in engineering. And why we insist on having experts on staff in critical areas such as magnetics, materials, components and safety.

"It's also why every Boschert product undergoes a grueling series of product evaluations, design reviews, environmental tests and manufacturing engineering reviews. As well as reviews by worldwide safety and regulatory agencies, including UL, CSA, VDE, IEC, BT, and the FCC.

"Superior design, top people, and sound procedures mean a great product. A *Boschert* product."

For more information, send the coupon to Boschert Incorporated, 384 Santa Trinita Avenue, P.O. Box 3426, Sunnyvale, CA 94088-3426. Or call 408-732-2440.

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Boschert

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CIRCLE 208 "SEE US AT WESCON BOOTHS #3348 & #3350"

FACTORY AUTOMATION

Motion controller plugs into bus systems

Interfacing via a single serial port with any industrial board-level computer—including Multibus, VERSAbus, STD bus, or VMEbus systems—an intelligent single-board module offers high-performance motion control of ac or dc servomotor systems. Using an RS-422 serial bus, up to 32 devices can be connected with simple twisted-pair or mass-terminated cable.

Operating as an intelligent slave controlling velocity and position in response to high-level ASCII commands, the PCM-901 programmable controller eliminates the need for potentiometer adjustments by utilizing gain and compensation data stored in its nonvolatile memory.

Ormec Systems Corp., 19 Linden Park, Rochester, N.Y. 14625; (716) 385-3520. $848, including MPL (100 units).

CIRCLE 343

IBM PC controls Bitbus network

Interfacing the IBM PC with Intel's Bitbus is a line of distributed control modules for use in factory automation and industrial control. The DT2806 board links the PC with the Bitbus via the DTX344 daughter board, an intelligent Bitbus master controller.

The DT901, a stand-alone controller, interfaces the Bitbus network with iSBX modules for remote measurement and control. The DT901 may also be used as an I/O expansion device, collecting and transferring data to the host.

Each DT901 includes an onboard microcontroller and four iSBX connectors. The connectors support any combination of a-d (DTX311), d-a (DTX328), and digital I/O (DTX350) modules.

Data Translation Inc., 100 Locke Drive, Marlboro, Mass. 01752; (617) 481-3700.

CIRCLE 344

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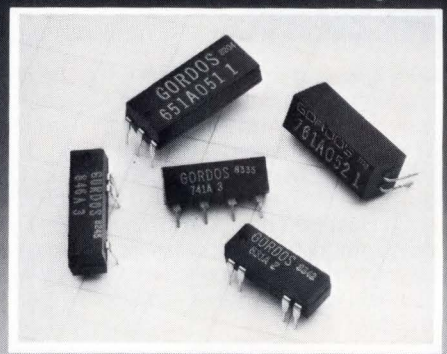
CIRCLE 209

HI-REL Relays



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CIRCLE 210

GRIMES SWITCHES: YANKEE INGENUITY AT AN IMPORT PRICE

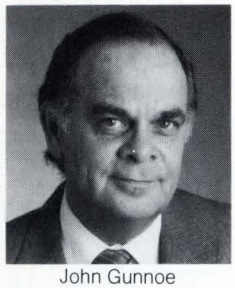
BREA, CA – Grimes Company may be the best kept secret in the electronics industry.

For years they have been the exclusive supplier of low-profile keyboard switches to one of the most successful personal computer manufacturers in the industry.

Aiming to produce the most inexpensive, high-quality American-made switch available, Grimes spent over $2 million perfecting the high-volume automated assembly equipment that can do it. These machines are capable of producing over 2.8 million switches per week.

This year the company tripled its total gross sales over last year's figures. Yet hardly anyone has heard of them.

Recently Grimes' management decided to let their secret out. And the industry may never be the same again.


John Gunnoe

Marketing and Sales Vice President John Gunnoe explained that after years of supplying one manufacturer with switches, joy sticks and monitor stands, Grimes felt it was time to expand their marketing base.

"We enjoy a very healthy relationship with that one manufacturer," Gunnoe said. "But you never want to put all your eggs in one basket."

Gunnoe declined to reveal the identity of that major manufacturer, but he did say "you can't turn around without seeing one of the ads in a magazine or on television."

As part of their aggressive new marketing strategy, Grimes Company will promote the advantages of their low-cost American-made switch over foreign competitors.

"Grimes' American-made switches cost less because of our high volume automated manufacturing process," said Operations Vice President Bruce Shepard.

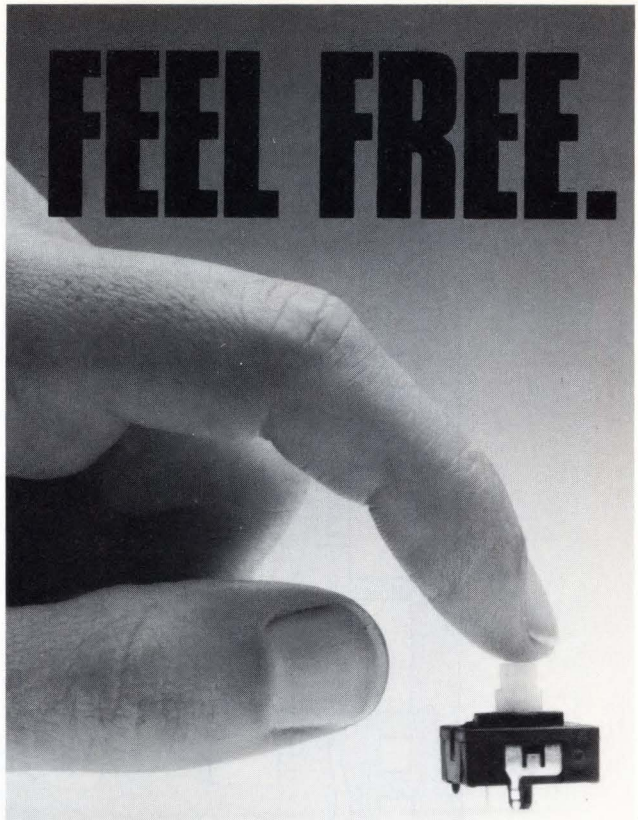
"And American-made means immediate delivery, immediate credit and no overseas freight charges," he added.

Shepard was quick to point out that Grimes didn't sacrifice high quality for their low price. Their switches are proven reliable for over 10 million cycles; most switches are good for only 100,000 cycles.

After establishing their presence in the electronics market, Grimes plans to continue researching and developing new products for the personal computer field. Recently Grimes Company purchased Track House, maker of the programmable IIe Tender keypad for the Apple IIe.

"We want to be able to supply our customers with new products, not just components or technology. The more services we can provide to our customers, the better," said Gunnoe.

For more information about Grimes' low-profile switches, (714) 671-3931.



Get a free sample of the American Switch

Are you ready to trade your Seoul supplier for some Yankee ingenuity? Switch to Grimes.

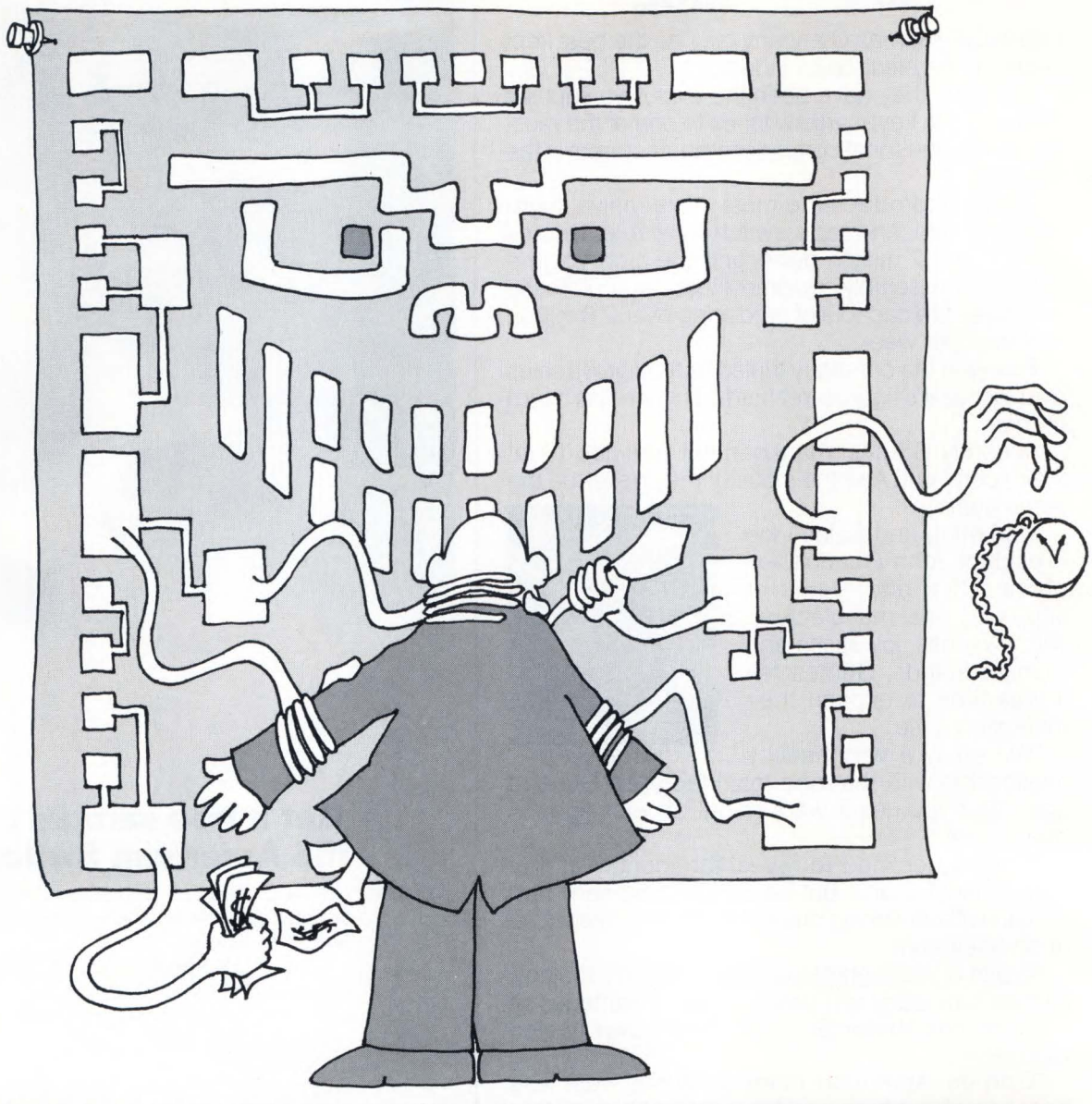
Grimes' low-profile, low-cost keyboard switches are used by one of the most popular personal computer manufacturers. And for good reasons: they're proven reliable at over 10 million cycles; stamped spiral springs control tolerances better than coiled springs; a built-in jumper eliminates the need for jumper wires and double sided circuit boards; and the unique bottom bearing reduces binding.

Grimes' switches cost less because their high-volume automated production reduces assembly costs. And American-made means immediate delivery, immediate credit and no overseas freight charges.

To get your free sample of Grimes' switches with and without tactile feel, call **1-800-671-3938** or circle the reader service number.

Feel for yourself why Grimes' high-quality low-profile keyboard switches will make you want to sell your Seoul.

GRIMES
THE AMERICAN SWITCH
115 S. Arovista Circle Brea, CA 92621



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CIRCLE 213

FACTORY AUTOMATION

Robot performs quick solder masking

Automatic masking of printed circuit boards for soldering and conformal coating is performed as much as 35 times faster than conventional methods with a robotic liquid-dispensing system. The special valve design of the ECLD 311's end effector, which dispenses both high- and low-viscosity maskants, virtually eliminates clogging. The valve's adjustable flow rate dispenses dots, lines, irregular patterns, and circles.

The robot system performs at a speed of 55 in./s, five times faster than nonrobotic automated systems. The liquid dispensing time is programmable; resolution is to within 1/1000 second.

Chad Industries, 1060-K N. Batavia St., Orange, Calif. 92667; (714) 997-4350. $40,000 to $45,000; six weeks.

CIRCLE 345

EPROM contains graphics symbols

When plugged into any IBM PC or PC-compatible color graphics board, an EPROM chip provides 86 graphics symbols for creating displays of control processes. The EPROM contains all of the standard ASCII control and printing characters. However, it replaces the foreign characters contained in the standard IBM ROM set with symbols for generating valve bodies and actuators, motors, pumps, pipes, corners, transmitters, orifice plates, ladder diagram symbols, bar graphs, and process vessels.

All of the characters are accessible with IBM Basic, as well as any other language. When the screen is used in color text mode, the EPROM provides graphics displays in 16 colors. The device comes with a diagnostic program.

Intellution Inc., 35 Perwal St., Suite F, Westwood, Mass. 02090; (617) 329-8188.

CIRCLE 346

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Anritsu's DMT2000 Streaming Magnetic Tape Drive

When you're saving that all-important data from a Winchester disk or other source, you need a dependable backup unit — the Anritsu DMT2000. A 1/2" streaming magnetic tape drive with an **MTBF of some 7,400 hours.** You can be sure every bit of your data will stay accurate.
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CIRCLE 214

MicroEnergy can make you a Power Supply that's smaller, cooler and more reliable.

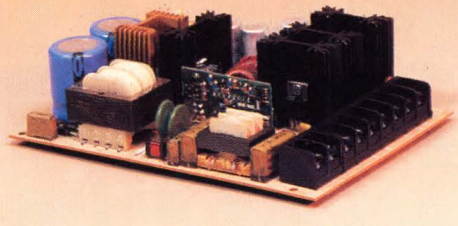
here's why: *Switching at high frequencies.*

Power supplies that switch above 100kHz give you significant savings in space, weight and thermal loading when compared to power supplies that switch under 50kHz.

Our MicroENERGY ME090™ series, for example, switches at 125kHz. It delivers over 2 watts/cubic inch and weighs only a pound. And with 70%-85% efficiency, its thermal loading is significantly reduced. The ME090 is one of the reasons MicroENERGY regularly provides customized power supplies for computer, telecommunication, automation and robotics manufacturers.

Customized from a family of power supplies.

The efficient cross-use of standard, proprietary modules and sub assemblies from within our family of power supplies lets us customize high frequency switching power supplies to your specifications. No need to compromise with off-the-shelf units. No need to pay the cost and invest the time for a total custom design.



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CIRCLE 215

MR62 Subminiature Relays

Leading reliability from a world leader in computers and communications.

When space is tight and conditions tough, specify MR62. It's the reliable DIP DPDT relay that really thrives on challenge. And delivers flawless performance in far-ranging applications.

MR62 relays—with nitrogen-gas-filled, twin crossbar contacts—come encased in impermeable armor. Their PBT shield scorns almost any attack—auto soldering, immersion cleaning, even chlorinated solvents.

Yet all this reliability stands only 0.45-inch high. And occupies a mere 0.31 square-inch of precious PC board real estate.

MR62 relays come in two series: standard and extra-high reliability.

We use our own relays in a full range of NEC computers and communications equipment. So we totally understand your need for reliability. Because our reputation, like yours, can rest on a single relay.

Contact form: 2C (DPDT).
Contact rating: 30W, 150VDC, 1.25A; 50VA, 125VAC, 1.25A.
Dimensions: H0.45" (+pins 0.13") ×W0.795"×D0.386".
Availabilities: Single Coil Latching Type; High Breakdown Voltage Version (Meets FCC Part 68).

NEC America, Inc.
Electromechanical Devices Department,
532 Broad Hollow Road, Melville,
New York 11747, USA. Tel: 516-752-9700.
Telex: 144658 NEC AMER MELV.

World Products, Inc., (U.S. distributor)
19678 8th Street East, Sonoma, CA 95476,
P.O. Box 517, USA. Tel: 707-996-5201.
Telex: WORLD PROD SNOM 171715.

NEC
NEC America, Inc.

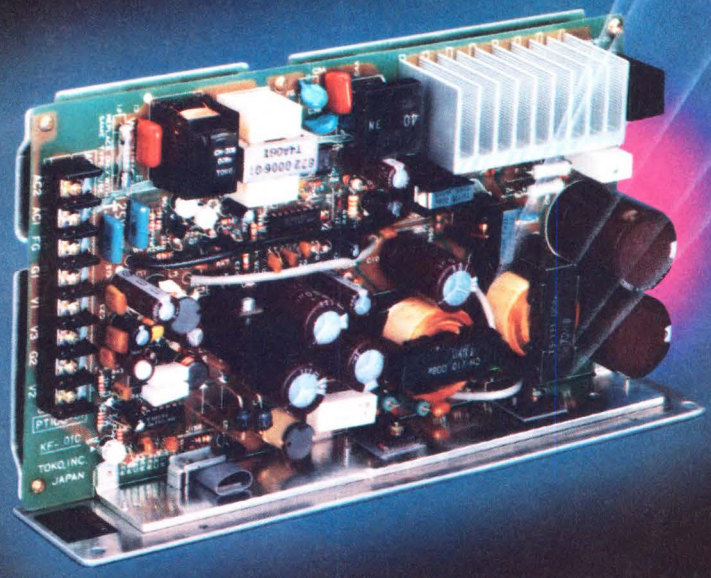
CIRCLE 216

This unique transformer gives Toko switching power supplies the edge on performance

When you select a switching power supply, your product's reliability and performance are on the line. Will the sample you approve be typical of OEM production? It will if you evaluate Toko. We reinvented the transformer to assure a consistent level of performance not possible with conventional transformer designs.

Unlike ordinary wire-wound transformers, Toko transformers are based on a better idea—inductive copper strips interwound with Mylar* insulation over a high-efficiency iron core. This design** significantly tightens performance tolerance limits and improves transformer reliability. The chances of a shorted winding are greatly reduced and the probability of an open winding is virtually eliminated.

For even greater performance assurance and added value we've derated our component specifications by 20%. Such steps combine with a very high level of quality control to let us offer a *two-year warranty*—twice the industry average.
All of these attributes, too, make Toko a better idea—not just a better power supply.



Toko also offers guaranteed delivery dates on standard supplies in virtually any quantity. We've made major investments in reserve plant capacity to easily handle your largest OEM orders.

We also meet every major testing standard for safety and EMI/RFI suppression.

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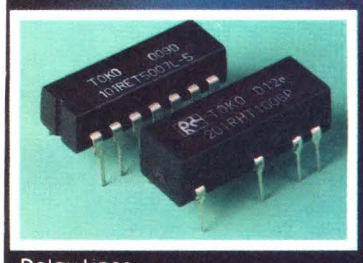
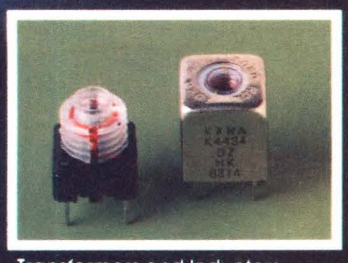
Toko America is the U.S. subsidiary of Toko, Inc., a large Japanese manufacturer of a broad range of high quality electronic products. Here's a sampling...



Delay Lines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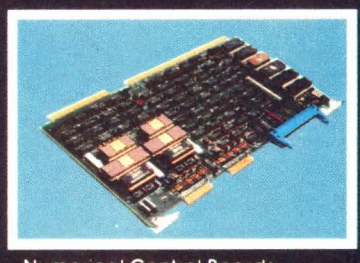
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* Reg. TM Dupont
**Patents pending

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CIRCLE 217

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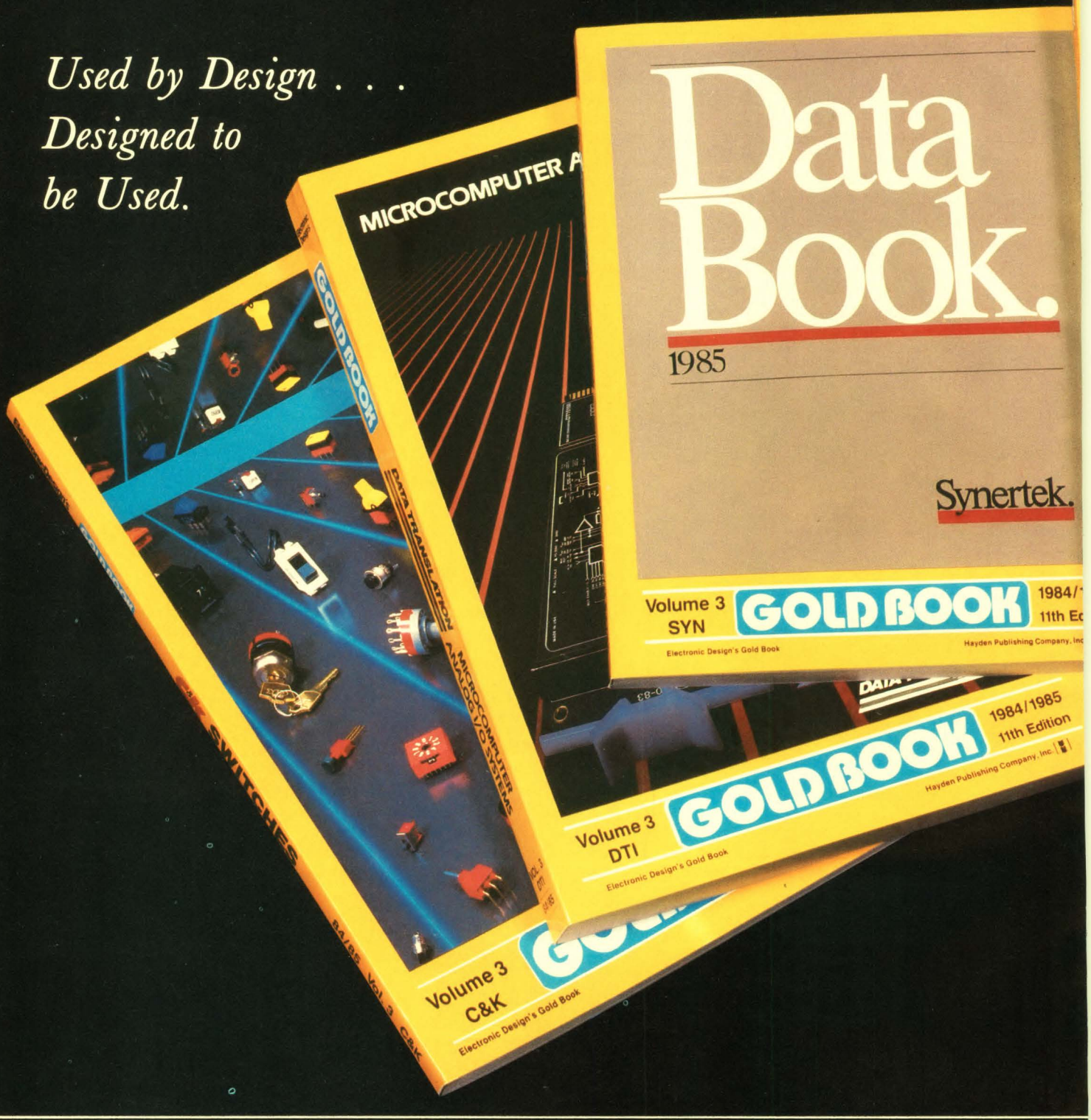

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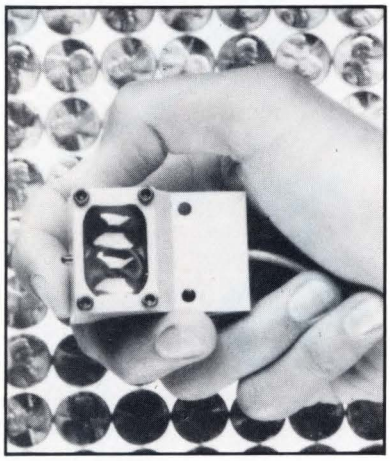


A photoelectric scanner with a self-contained amplifier and a visible light beam for easy alignment is one-third the size of conventional self-contained scanners. Called the Valu-Beam, the three-wire unit is only 2⅛ in. high by 1⅜ in. wide by 1⅜ in. deep. It is available in ac or dc models and operates in retroreflective, convergent, diffuse, and opposed scanning modes. In the retroreflective mode, the Valu-Beam's range is up to 15 ft. The device may be adjusted for sensitivity and for light or dark operation.

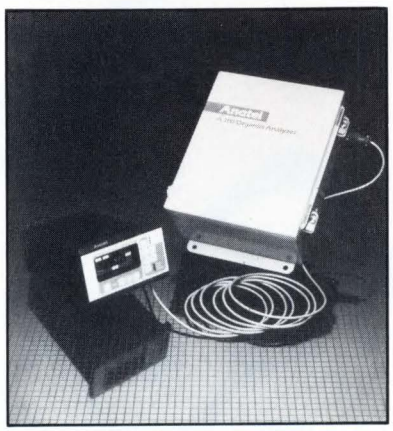
In addition to a visible beam, the scanner employs a second built-in system that indicates both alignment and exact signal strength. The Valu-Beam's low leakage current enables it to interface directly with all programmable controllers.

Banner Engineering Corp., PO Box 9414, Minneapolis, Minn. 55440; (612) 544-3164. Less than $40 in large quantities.

CIRCLE 347

Ultrapure-water monitor detects organic carbon

The A-100 TOC (total organic carbon) analyzer is an on-line monitoring system for measuring the organic contamination of VLSI process water. It eliminates the need for chemical reagents by using an ultraviolet light to break down the organic compounds. A conductivity measurement then determines the total concentration of organic carbon down to 10 parts/billion.



The A-100 consists of a 2½-by-5-by-7-in. control unit, a small power pack, and an 11-lb chamber, which is designed to be installed anywhere within the water purification and distribution system. Analysis parameters are programmed via the controller's front panel.

At less than $9000, the A-100 is priced considerably lower than current process systems, which range between $15,000 and $30,000.

Anatel Instrument Corp., 2200 Central Ave., Suite F, Boulder, Colo. 80301; (303) 442-5533.

CIRCLE 348

Announcing the new Marconi Instruments 1GHz Signal Generator at $3950.

If the brochure has been removed, please check reader service No. 120

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POWER

Trio of power MOSFETs has lowest on-resistance for 50- and 60-V devices

Three power MOSFETs fabricated with Motorola's new TMOS III process attain the lowest on-resistance per cell size of any available power MOSFETs rated for under 100 V. One, rated at 12 A and 60 V, has an $R_{DS}(on)$ of 0.15 Ω and is the least expensive device—only 60¢—for its specifications. Designated the MTP3055A, it aims at replacing the industry-standard bipolar 2N3055, which is priced about 25% to 67% higher. Its 50 μA of leakage current is almost 100 times better than that of the 2N3055's 5 mA.

The other two devices are the 14-A, 50-V MTP14N05A, which has an on-resistance of 0.10 Ω, and the 16-A, 50-V MTP16N05A, which at 0.08 Ω provides the lowest on-resistance and best performance for its die size—96 mils square—in the industry.

As is true of MOSFETs in general, switching speeds are superior: The MTP3055A has a turn-on delay time of 20 ns, compared with 150 ns for its bipolar counterpart. Its other relevant specifications are a rise time of 60 ns and turn-off delay and fall times of 65 ns each. The MTP14N05A and MTP16N05A are close behind at 30 ns, 80 ns, and 85 ns, respectively.

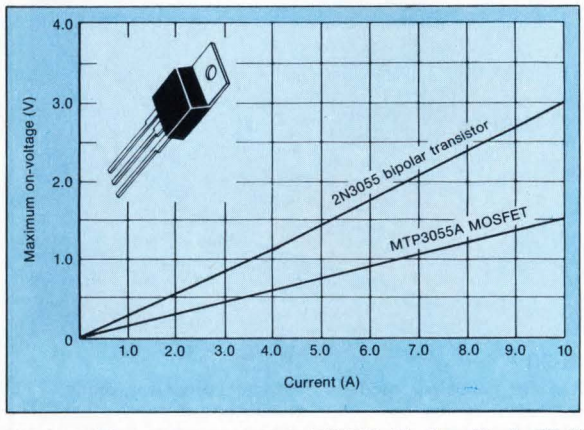
In addition, the MTP3055A has an input capacitance of 500 pF and reverse-transfer and output capacitances of 200 pF each.

Of course, all devices sport the other inherent advantages of MOSFETs over bipolar devices: an intrinsic source-drain diode with switching times comparable to the MOSFET itself, a voltage gain that is constant with increasing collector current, and higher efficiency because current is required only to switch the device.

The 60¢ price of the MTP3055A is for 100-unit lots. In similar quantities, the MTP14N05A and MTP16N05A cost $1.31 and $1.46, respectively. Samples and prototype quantities are available from stock; delivery of production quantities takes six to eight weeks.

Motorola Semiconductor Products Inc., PO Box 20912, Phoenix, Ariz. 85036; (602) 244-6786.

CIRCLE 321



Made with a new process, TMOS III, the 12-A, 60-V MTP-3055A has half the on-resistance, and hence losses, of its bipolar counterpart, the popular 2N3055, with an equivalent die size—and it also costs less.

Heather Bryce

POWER

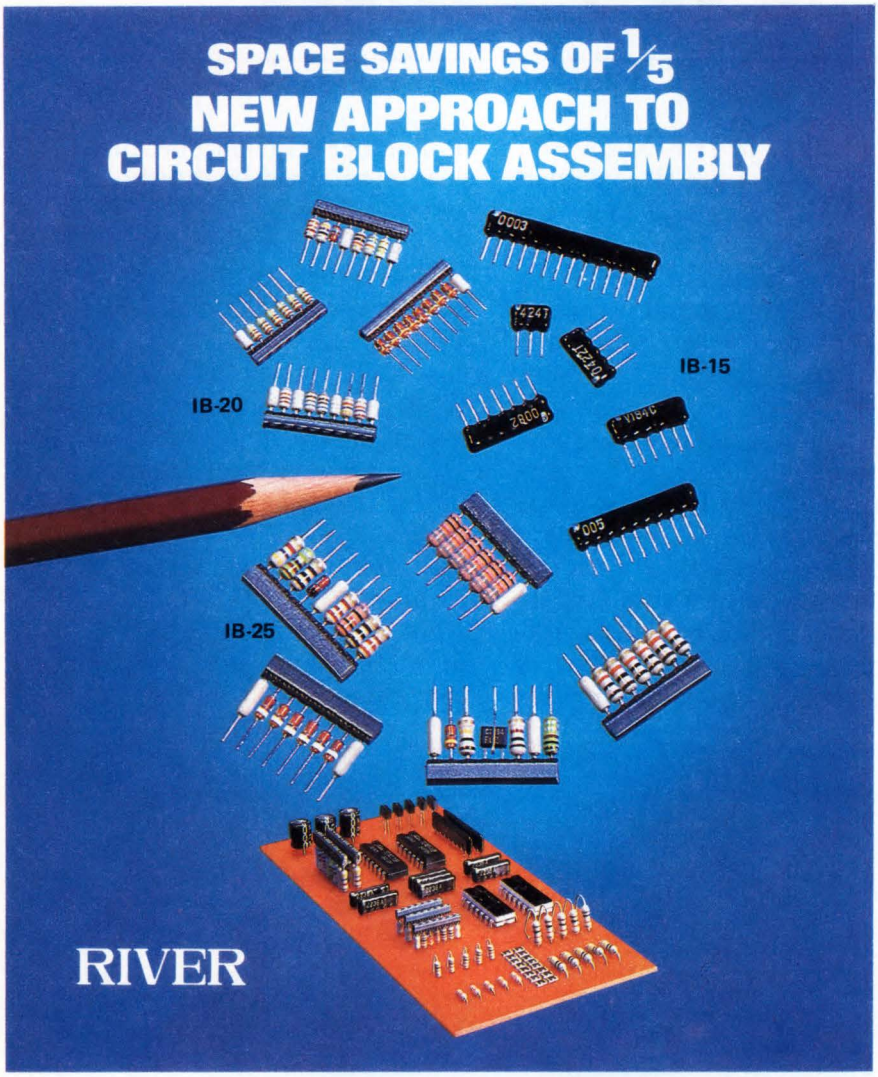
Power MOSFETs withstand up to 800 V

A series of high-reliability, fast-switching power MOSFETs offers drain-to-source voltages from 50 to 800 V and drain currents from 3 to 45 A. The devices are offered in eutectic-bonded, isolated TO-61/I, TO-111/I, and TO-228AA cases—designated the FNA-, FNB-, and FNC-15/80, respectively. Features include very low on-resistance, no secondary breakdown, and excellent temperature stability.

Solitron Devices Inc., 1177 Blue Heron Blvd., Riviera Beach, Fla. 33404; (305) 848-4311. $39.50 (1000 units); six to eight weeks.

CIRCLE 349

SPACE SAVINGS OF 1/5
NEW APPROACH TO CIRCUIT BLOCK ASSEMBLY



IB-15	IB-20	IB-25
Resistor conductor can be assembled freely	Resistor, capacitor, diode, conductor can be assembled freely	Resistor, capacitor, diode, transistor and conductor can be assembled freely
Connector pitch 2.0 mm	Connector pitch 2.0 mm	Connector pitch 2.5 mm
Height (MAX) 5.0 mm	Height (MAX) 7.5 mm	Height (MAX) 11.5 mm

Send inquiries to: **RIVER ELECTRONICS CORP.**
18321 S. Western Ave., Suite H, Gardena, CA 90248 USA
Tel: 213-329-6359 Telex: TWX910-346-6394

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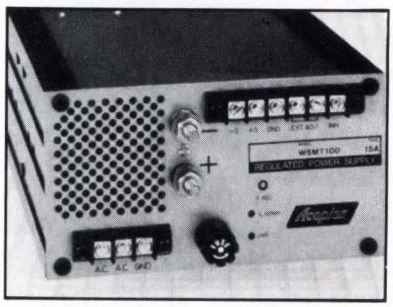
14-40, Nishi Shinjuku 4-chome, Shinjuku-ku, Tokyo, Japan
Tel: 03-377-5444 Telex: 232-2382

CIRCLE 218

Switching supply utilizes MOSFETs



Providing outputs ranging from 5 V dc at 100 A to 48 V dc at 12 A is the Series W switching power supply. The MOSFET switching circuitry, which operates at 55 kHz, reduces component count and increases efficiency compared with bipolar designs having comparable ratings. Efficiency for the Series W is typically 76%. Line and load regulation are ±0.05%.

The supply is housed in a compact 3.4-by-6.3-by-9.3-in. metal case. LED lamps indicate normal operation and shutdown due to latch-up of the overvoltage protection circuit. The unit also features soft-start operation and automatic shutdown in the event that input voltage is too low.

Acopian Corp., PO Box 638, Easton, Pa. 18044; (215) 258-5441. $950; two weeks.

CIRCLE 350

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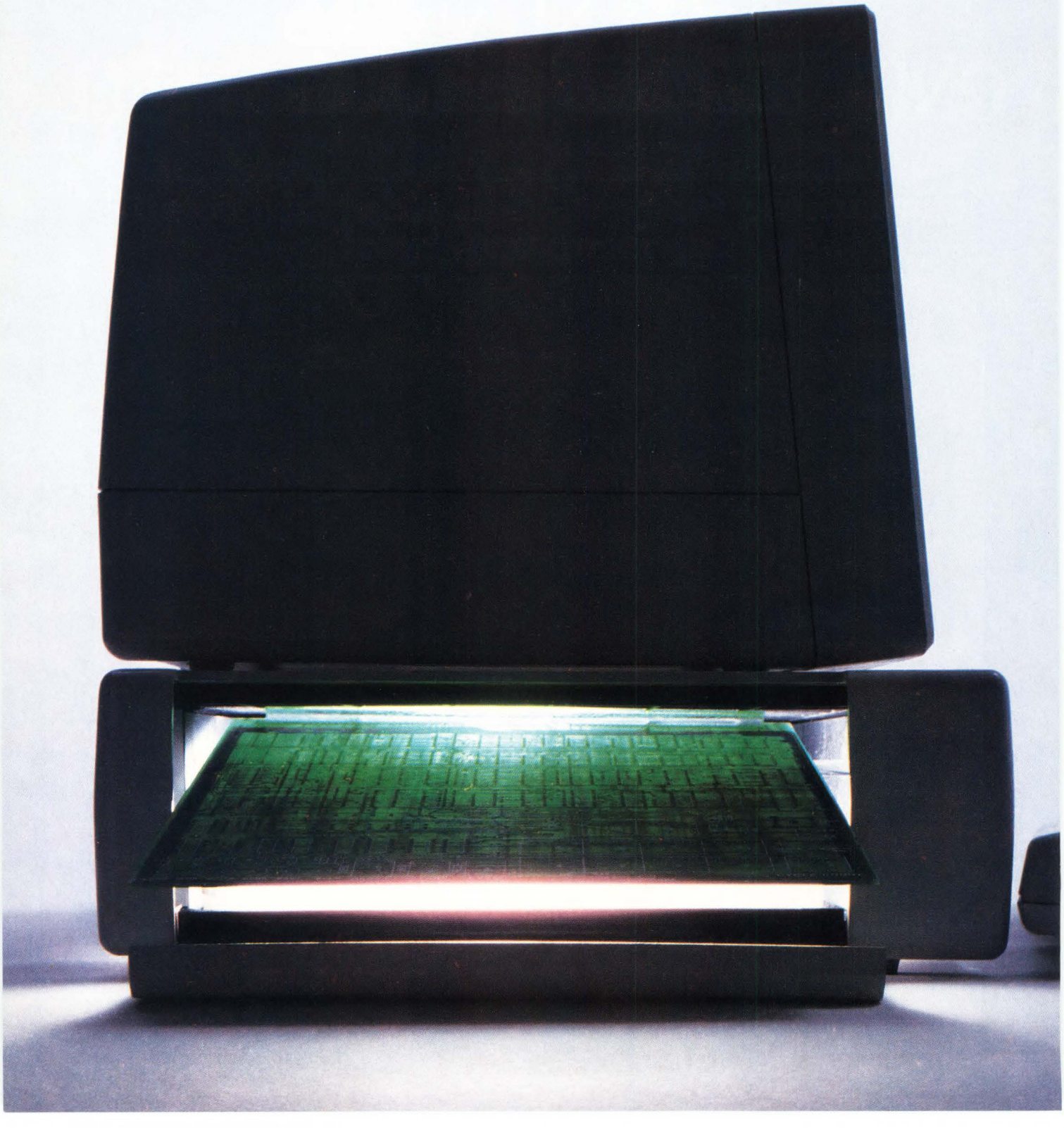

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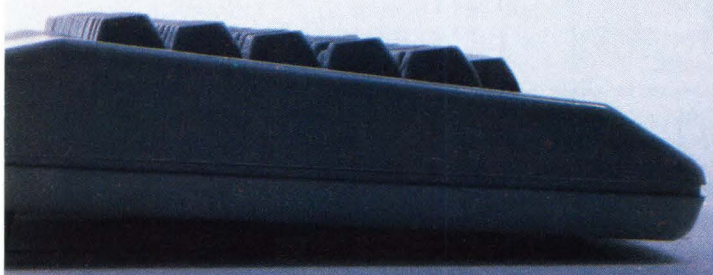


COMPUTER BOARDS

Slave processor puts distributed processing on the STD bus at low cost

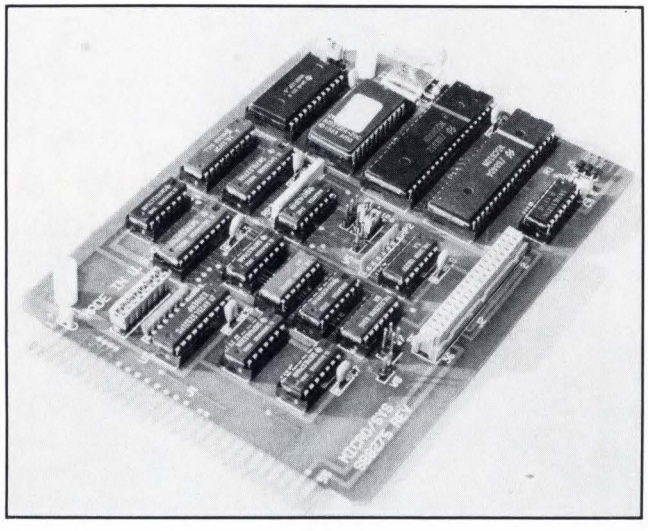
A piggyback combination of a slave processor and an I/O card brings low-cost distributed processing to STD bus systems. The slave processor board costs only $180, and the I/O cards from $95 to $680, for a total price much lower than that of adding a full-fledged STD bus system for greater processing power.

Developed by Micro/Sys, the SB8275 processor interfaces directly with the STD bus and one of a number of specially designed I/O boards that is mounted on it. The combination uses only one slot and can be dedicated to a single I/O application, such as monitoring analog lines.

Ray Weiss

In such a case, the slave performs the basic processing of the raw data. That increases system throughput by freeing the system CPU to concentrate on scheduling and higher-level processing and minimizing traffic on the STD bus. Similarly, individual application tasks can be served by dedicated slave processors running the application programs, again boosting system throughput.

All communication among processors is through the system CPU, to which the slave processor looks like four sequential I/O ports. Data passes through 8-bit mailbox registers on the slave processor.



The slave uses a National NSC800 and can hold up to 32 kbytes of PROM and 8 kbytes of RAM. It also contains two 16-bit timers.

The slave processor and I/O board interface is simple and general-purpose, and the physical connection is straightforward: The I/O board is mounted using standoffs and a board connector on the slave.

Three I/O boards are currently available: the SB8276, which has 32 bidirectional digital lines; the SB8277, which has 16 analog inputs and a 12-bit analog-to-digital converter; and the SB8278, which has 8 analog outputs plus a 12-bit digital-to-analog converter.

Deliveries are from stock. The prices for the cards in 50-unit lots are $180, $95, $495, and $680 for the processor and the SB8276, SB8277, and SB8278, respectively. Delivery is from stock.

Micro/Sys Inc., 1011 Grand Central Ave., Glendale, Calif. 91201; (818) 244-4600.

CIRCLE 314

COMPUTER BOARDS

64-Mbyte memory board expands to 2 Mbytes

Starting with as little as 64 kbytes of RAM, IBM PC users can expand to a full two Mbytes of memory on a single board. What's more, with MegaCache and MegaSpool software, speed improvements from three- to tenfold can be realized.

The board, dubbed the 2megaboard, provides up to 32 64-kbyte segments, eight of which may be mapped into a 512-kbyte region of the computer's memory. It performs parity checking and reporting, and any of the eight segments may be write-protected. The module requires less than 300 mA at +5 V dc when fully configured.

Datatron Inc., 12191 Mariners Way, Garden Grove, Calif. 92643; (714) 554-8214.

CIRCLE 354

Multiplexing controller works with Unibus

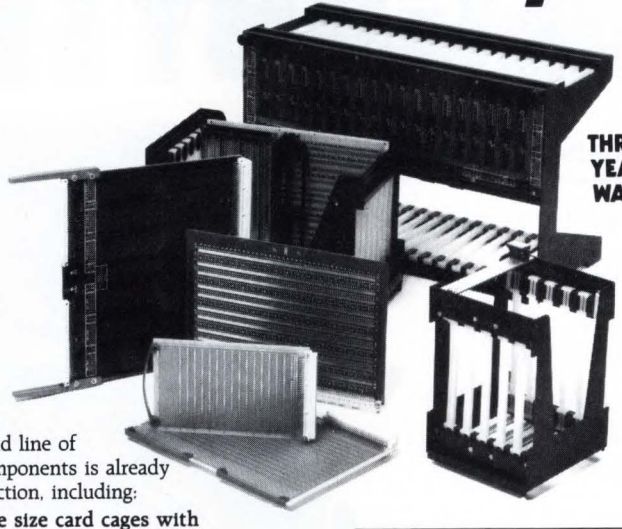
An asynchronous communications controller, the Optimux/16DMF+, is the first in a family of optimized Unibus-compatible multiplexers for use with PDP-11 and VAX computers. It performs all of the standard functions of Digital Equipment's DMF32 and DH11 subsystems, while permitting connection of 16 peripheral devices from a single backplane slot.

The Optimux/16DMF+ offers software-selectable data transfer rates from 50 to 34,800 bits/s—twice the maximum data transfer rate of most communications controllers. Moreover, during high-throughput operations its bidirectional data-flow control virtually eliminates data loss, and its multiword DMA burst mode significantly reduces Unibus overhead.

Distributed Logic Corp., 1555 S. Sinclair St., PO Box 6270, Anaheim, Calif. 92806; (714) 937-5700. $3000; 30 days.

CIRCLE 355

VME System Packaging: Electronic Solutions Makes it Easy.



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A broad line of VME components is already in production, including:

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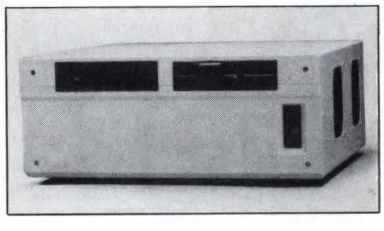
- ☐ Test sets



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Telex II (TWX): 910-335-1169

Multibus is a trademark of Intel Corp.

CIRCLE 221

COMPUTER BOARDS

Multibus SBC is iSBC-86/05-compatible

The ZX-86/05A, a Multibus single-board computer, is compatible with the iSBC-86/05 and features a 10-MHz 8086 processor for fast system throughput. The board's flexible memory section—consisting of eight 28-pin JEDEC sockets, each capable of supporting up to 512k EPROMs and 64k static RAMs—allows the user to tailor the board for many applications.

Enhancing the ZX-86/05A's I/O capabilities are dual USARTs and 24 parallel I/O lines, as well as three iSBX connectors. An onboard 8087 numeric coprocessor socket spares the expense of adding an expansion module when a coprocessor is required.

Zendex Corp., 6644 Sierra Lane, Dublin, Calif. 94568; (415) 828-3000. $1000 with 8 kbytes of RAM (100 units); four weeks.

CIRCLE 356

VME SBC with

ONE MEGABYTE

Performance Oriented

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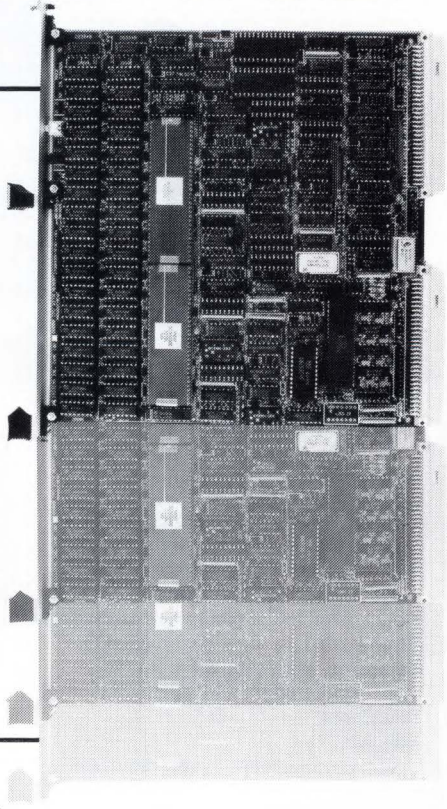
- Zero wait states
- 68000 CPU
- Multi-master capability
- System control functions
- Optional MMU
- Two RS-232C channels



The DVME-102 from DY-4 has proven its performance record in the field, and lends its features to ease of System Design. A full One Megabyte of on-board memory eliminates the need for data transfer across the VMEbus. Send for more on the DVME-102 and the entire line of VME modules from DY-4 Systems.

DY-4 SYSTEMS INC.

1475 S. Bascom Ave, Campbell, CA 95008, (408) 377-9822
888 Lady Ellen Place, Ottawa, Ontario, Canada K1Z 5M1 (613) 728-3711
Solbakken 48, DK-8450, Hammel, Denmark (06) 96-3624 TLX 60938 (Dendy DK)

CIRCLE 222

Single board employs dual processors

A single printed circuit board features a dual-processor architecture utilizing Intel's 80286 and 80186 microprocessors, each running dedicated environments. The board, designated the DPX86/ME, is available with three major operating systems: Xenix, iRMX-286, and PC-DOS.

A shared-memory feature allows I/O processing—including Ethernet, RS-232-C asynchronous, and either Centronics-type or SCSI disk communications—to occur simultaneously with 80286-controlled applications. The board can be configured with a total of up to 1 Mbyte of RAM and 400 kbytes of ROM.

Little Machines Inc., 4141 Jutland Drive, San Diego, Calif. 92117; (619) 483-3606. From $4000, not including software (100 units).

CIRCLE 357

COMPUTER SYSTEMS

Workstations speed pc board design

Three printed circuit board CAD workstations extend a line of design automation systems known for its price/performance ratio. The systems include the CDX-5000A, a cost-reduced version of the existing CDX-5000 workstation; the CDX-50000, a high-performance CAD system with a graphics accelerator engine; and the CDX-59000, a complete design and layout workstation with full CAE/CAD capabilities.

The CDX-5000A offers all the functionality of the CDX-5000, which sells for $74,500, at a cost of only $49,900. The CDX-50000, with its graphics accelerator engine, a hierarchical schematic editor, and automatic placement and routing software, allows the user to design very large boards (in the 700-IC range) with ease and speed. This system sells for $79,900.

At the top of the line, the CDX-59000 adds powerful design analysis software to the high-performance CDX-5000 configuration. It features the CADAT twelve-state logic simulator and a SCALD-based timing analyzer. A graphic waveform editor simplifies test pattern development. The $94,900 CDX-59000 takes the user from logic design and verification to pc board layout and manufacturing outputs in a single workstation.

Cadnetix Corp., 5757 Central Ave., Boulder, Colo. 80301; (303) 444-8075.

CIRCLE 336

CAE workstation builds on IBM PC AT for low cost

One of the first CAE workstations based on the new IBM PC AT, the Personal Logician AT, from Daisy Systems, provides many of the same functions, including schematic entry and logic simulation, and the same interactive graphics capabilities of larger workstations at a fraction of the cost—only $25,000.

Unlike other personal computers used for CAE, the workstation does logic simulation, as well as schematic entry. In addition, larger engineering tasks, such as design rule checking, can be uploaded to larger computers through an Ethernet local-network interface.

The IBM PC AT foundation of the Personal Logician AT uses an 80286 processor and 610 kbytes of local memory. The hardware also includes a 20-Mbyte hard-disk drive, a 1.2-Mbyte floppy-disk drive, serial and parallel I/O ports, and Daisy's high-resolution graphics subsystem. The last item consists of a specialized video controller and a monochrome monitor with a resolution of 1022 by 840 pixels—the same as the company's Logician workstation. (A color monitor is an option.)

A complete workstation, including the PC AT computer, the graphics subsystem, disk drives, and software costs $25,000. Existing PC ATs with at least 512 kbytes of memory and a 20-Mbyte hard disk can be converted into Personal Logician AT workstations by adding the graphics subsystem, additional RAM, and software, for $20,000. A color version of the system costs an additional $10,000, and an Ethernet capability adds $2500.

Daisy Systems Corp., 700 Middlefield Road, Mountain View, Calif. 94043; Robert Spivack, (415) 960-6956.

CIRCLE 306

Stephan Ohr

COMPUTER SYSTEMS

Off-line workstation supports color plotting

An off-line plotting workstation supports electrostatic color and high-resolution (200- and 400-point/in.) plotting on Versatec plotters from CalComp 921/925 tapes. The workstation performs all vector sorting and vector-to-raster conversion. It also accepts seven Versatec standard data formats. Plot processing from the workstation results in a 10:1 speed advantage over pen plotters for most drawings and maps. The system includes a microprocessor, 64 kbytes of memory, a video display, a 24-Mbyte Winchester disk, a magnetic tape drive, and a bipolar algorithmic processor.

Versatec, 2710 Walsh Ave., Santa Clara, Calif. 95051; (408) 988-2800. $46,000; 30 days.

CIRCLE 358

32-bit workstation joins VAX family

Enhancing the VAX family of computers is the VAXstation I, a true 32-bit single-user workstation system. Built around the MicroVAX I, the system features a 19-in. display, high-resolution graphics, and full VAX/VMS operating system resources. It supports GKS (Graphic Kernel System) as its first graphics application interface language.

The basic configuration includes the processor with 1 Mbyte of main memory, a 1k-by-2k bit-mapped video RAM, dual 400-kbyte floppy-disk drives, a 31-Mbyte 5¼-in. Winchester drive, a monochrome monitor, and a mouse. The VAXstation I can be connected to DECnet/Ethernet networks, enabling access to larger VAX computers, VAXclusters, and other VAXstation I workstations.

Digital Equipment Corp., 146 Main St., Maynard, Mass. 01754; (617) 897-5111. From $21,095.

CIRCLE 359

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CIRCLE 223

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WP350324	24V	0.1A
WP410412	12.6V	0.3A
WP410612	12V	0.5A
WP410614	14V	0.4A
WP410624	24V	0.25A
WP481012	12V	0.83A
WP481024	24V	0.42A
WP571616	16V	1.0A
WP571618	19V	0.84A
WP572012	12V	1.67A
WP572024	24V	0.83A
WP572408	8V	3.0A
WP572412	12V	2.0A
WP663021	21V	1.4A
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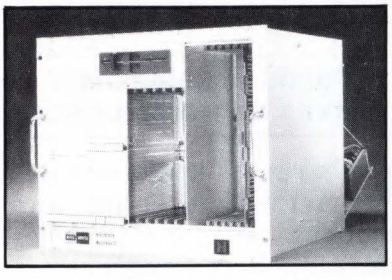
CIRCLE 224

PACKAGING & MATERIALS

Frame accepts Multibus II boards

Anticipating Intel's final specifications for Multibus II is a frame that will accept cards for the new bus structure. The Microrack, from BICC-Vero, has 10 double-Eurocard iPSB slots, 6 of which (the maximum number now permitted by the Multibus II specifications) also connect to the iLBX bus; it also has 4 user-definable



single-height card slots.

Since Multibus I will still be around for some time, the card frame has six Multibus I slots as well. The six-layer backplane has off-board terminations.

The 19-in.-wide rack comes in a standard 9U height and is 550 mm deep. The top 2U can house a full-height Shugart-compatible 5¼-in. disk drive; the 6U center is the Multibus section, conforming to the DIN 41494 standard; and the bottom 1U is allocated to cooling and front-panel controls.

A 400-W switching power supply is mounted on the frame's hinged rear panel, which also carries cutouts for four 25-way D shells and three 37-way D shells. Four integral fans beneath the card frame blow air across the boards, and an extractor fan is fitted to the rear panel.

The frame can be tailored to a customer's requirements.

BICC-Vero Electronics Inc., 171 Bridge Road, Hauppauge, N.Y. 11788; (516) 234-0400.

BICC-Vero Electronics Ltd., Hedge End Industrial Estate, Flanders Road, Southampton, Hants. SO3 3LG, England; (04892) 81424/5; Telex: 477984.

CIRCLE 302

Neo-iron magnet alloy delivers high energy

Crumax 30 is a neodymium-iron permanent-magnet material specifically developed for electric motor applications. The alloy has an energy product of 30 MGOe (megagauss oersteds) and is available in two subgrades: Crumax 30A, which has a retentivity (B_r) of 11,000 G and a coercivity (H_c) of 10,600 Oe; and Crumax 30B, with a B_r of 11,600 G and an H_c of 10,500 Oe.

Relatively inexpensive raw materials are used in Crumax 30, making it an economical high-energy permanent magnet for applications requiring straight-line demagnetization characteristics and operating temperatures of up to 150°C. Such applications include linear actuators and computer peripherals.

Colt Industries, Crucible Magnetics Division, RFD No. 2, Elizabethtown, Ky. 42701; (502) 769-1333.

CIRCLE 405

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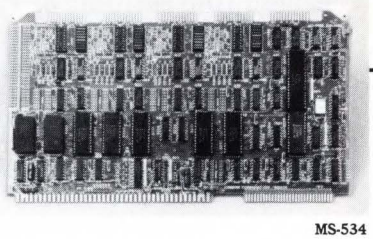
TEL: (303) 337-0220 TLX: 296472 SKYS UR

CIRCLE 225



MS-534

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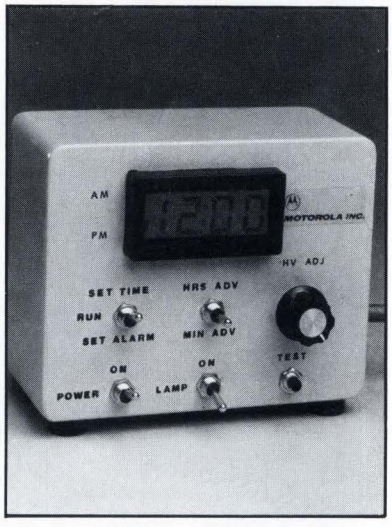
CIRCLE 226

PACKAGING & MATERIALS

Evaluation kit contains ceramic display



The latest benefits in display technology can be explored with the SCD solid ceramic display evaluation kit. SCD displays use a polycrystalline ceramic of PLZT (lanthanum-doped lead zirconate titanate) to provide a 160° viewing angle, a 500-μs response time, and operating temperatures down to −40°C without the use of heaters. Conductive patterns on the crystal surface create standard seven-segment digits when energized.

The SCD evaluation kit can exercise one of six displays in reflective, transflective, and transmissive viewing modes. The metal-enclosed unit includes a 12-hour chronograph with an alarm and a battery-backed clock memory. It operates from a 115-V ac supply.

Motorola Ceramic Products, Market Development, 4800 Alameda Blvd. NE, Albuquerque, N.M. 87113; (505) 822-8801. $990; stock.

CIRCLE 360

Quiet cable extends transmission distances

The latest addition to an extensive line of data cables, EDQ cable enables longer transmission distances and reduces EMI/RFI noise emissions. The cable's low capacitance of 12 pF/ft allows it to carry data signals for a longer distance than standard EIA cables without loss of signal integrity. RS-232-C signals are transmitted up to distances of 500 ft at 9600 bits/s without using modems, line drivers, or repeaters.

To reduce electronic noise interference, the EDQ cable has two shields—one of aluminum foil to suppress high-frequency emissions and the other of braided copper to reduce low-frequency emissions. The cable may be ordered with a molded-on connector hood, which includes a metallic shield, or with a removable metal hood. Both hoods extend suppression to the interface connector.

Black Box Corp., PO Box 12800, Pittsburgh, Pa. 15241; (412) 746-5500.

CIRCLE 361

Brushless fans are light, compact

The SJF series of brushless fans is available in two lightweight, compact sizes: 60 by 60 mm and 80 by 80 mm, each with a depth of 23 mm and weighing 75 and 100 grams, respectively. A noise level of 35 or 45 dB may be specified for models of either size. The eight models that comprise the series offer 12- or 24-V operation at various currents, ranging from 0.12 to 0.32 A. The fans deliver 0.40, 0.25, 0.80, and 0.55 m^3 of air per minute at respective pressures of 4.0, 2.0, 3.1, and 2.0 mmH_2O. Operating temperatures range from −10° to +60°C.

International Components Corp., 1740 N. Marshfield Ave., Chicago, Ill. 60622; (312) 772-4400.

CIRCLE 362

Conductive laminate serves as work surface

Charge-Guard is a material with electrical and mechanical characteristics developed and engineered specifically for electronic workstation surfaces. The hard laminate is a suitable surface on which all types of equipment containing static-sensitive electronic components can be handled. It consists of a rugged top layer and a conductive middle layer bonded to a bottom core material. It has a surface-to-ground resistance of 10^5 to 10^7 Ω. Charge-Guard resists solvents common to the electronics industry, and hot solder or solder flux will not damage its surface. It is available in 4-by-8- and 5-by-12-ft sheets and in cut form in three UV-resistant, semigloss colors (blue, beige, and gray).

3M Co., Static Control Systems Division, Department ST84-12, PO Box 33600, St. Paul, Minn. 55133; (612) 733-1186.

CIRCLE 363

Bivar introduces a new PCB Packaging Concept!

THE SOLUTION TO CARD GUIDE INVENTORY, SPACING AND COSTS.

CIRC-O-GIDEs™

Snap-in Anywhere...
...Any Spacing
...Any PCB Thickness
...Any PCB Length

patents pending

5 Thicknesses—
7 Diameters—
35 Standards

Can Be Used In Pairs
For Any Spacing

CIRC-O-GIDE™. It's a totally new method for spacing, guiding and giving firm retention for printed circuit boards that adds a new dimension of versatility to PCB packaging. These simple, easy-to-install by hand, button-style CIRC-O-GIDEs can be used just about anywhere a .172″ diameter hole can be made. Card cages, PCB retaining rails, drawers, etc.

REDUCES STOCKING REQUIREMENTS
Instead of worrying about the different sizes of PCBs you will use in your application, and the many corresponding lengths of conventional card guides you would need in your inventory, just identify spacing and quantity requirements. CIRC-O-GIDEs are available in a choice of 5 standard gripping thicknesses from .078″ to .187″ for maximum retention and 7 diameters for .312″, .400″, .500″, .600″, .750″, .800″ and 1.000″ spacing for the space that's just right for you. All are available from stock, and in many cases only one size may have to be stocked for all your applications.

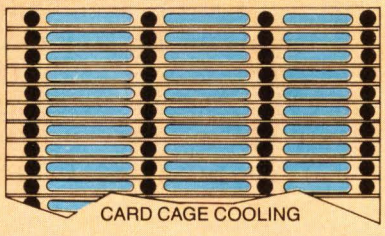
SAVES GUIDE USAGE
When used as pairs throughout, any spacing of .312″ and over can be used, giving the designer absolute license in choosing location, density and gripping action. When spacing is standard, CIRC-O-GIDEs also offer substantial economies by reducing the number of guides required. Aligned pairs are used for the first PCB, and single rows thereafter.

Made of durable black, glass reinforced NYLON per ASTM D4066, U.L. rated 94V-O, these little CIRC-O-GIDEs can take it. And you can take them for less because they're low in cost.

You can realize savings in time, space and in your PCB packaging costs today, without waiting. Call your nearest BIVAR Representative, stocking Distributor, or the factory for complete specifications.

BIVAR. We've just added to a growing family of over 4050 cost-saving aids. And this time, it's a snap.

IMPROVED CARD/SYSTEM COOLING
By eliminating the continuous length of the conventional card guide, CIRC-O-GIDEs afford added space for cooling slots in card cages, and substantially open otherwise confined, air-limiting space in assemblies where heat between printed boards is a continuing concern.



CARD CAGE COOLING

Thanks Bivar!

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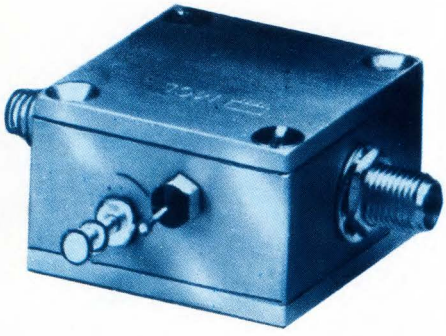
CIRCLE 227

miniature wideband amplifiers



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INTERCEPT POINT, 3rd order	25 dBm
VSWR, 50 OHMS	2:1
DC POWER	+15V, 100 mA

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CIRCLE 228

COMPONENTS

Slide switches come in micromini packages

Two families of slide switches—the MMS and SSJ series—boast high performance in an unusually small package. For example, the SSJ-12 SPDT switch is only 0.394 in. long by 0.157 in. wide and stands 0.26 in. high, including the actuator. The devices' standard silver-plated double-wipe contacts have a rating of 100 mA at 30 V dc. The shorting contacts also have a rated life of 10,000 operations.

The MMS family consists of one-, two-, and four-pole versions. The single-pole device has an upright actuator with a two-position on function. The two- and four-pole types are available with upright or side actuators, as well as two- and three-position on functions.

The SSJ series is available in single- and double-pole versions with upright or side actuators. The double-pole unit comes with a two-position on function, while the single-pole switch also offers three-position on-on-on.

Augat/Alcoswitch, 1551 Osgood St., North Andover, Mass. 01845; (617) 685-4371.

CIRCLE 364

¼-W resistor shrinks package size

The CCF-50, a compact metal-film resistor, gives designers ¼ W of power (at 70°C) in a package that is the same size as conventional ⅛-W resistors. The 0.150-in.-long resistor body has a diameter of 0.062 in. Its 0.020-in. leads make it suitable for use with automatic insertion equipment.

The CCF-50 has a tolerance of ±1% over a resistance range of 10 Ω to 1 MΩ. The resistance temperature coefficient is ±100 ppm/°C over the operating temperature range of −65° to +165°C. Maximum working voltage is 200 V rms.

Dale Electronics Inc., 2300 Riverside Blvd., Norfolk, Neb. 68701; (402) 371-0080. Approximately $0.05 (100,000 units).

CIRCLE 365

Dot-matrix print head boasts speed, low cost

Featuring high-resolution graphics output, the Model 900 radial dot-matrix print head is capable of operating at speeds of up to 150 char/s. It also offers one of the industry's lowest prices.

The 900 print head has a seven- or nine-dot yield. Graphics are enhanced by a fine needle diameter of 0.012 in. and dot diameters of 0.015 in. The head produces a vertical spacing of 72 dots/in. Horizontal resolution is 60 dots/in. for full-dot spacing and 120 dots/in. for half-dot spacing. Character height is 0.122 in. for the nine-wire array and 0.094 in. for the seven-wire formation.

Litton Industries, Westrex OEM Products Division, 51 Penn St., Fall River, Mass. 02724; (617) 676-1016. $48.

CIRCLE 366

Think Teledyne...For Fast Dual Power MOSFET Drivers.

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CIRCLE 235

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PRODUCT NEWS

Improved logic analysis for HP 64000

For high-speed logic design on the HP 64000 development system, **Hewlett-Packard Co. (Palo Alto, Calif.)** has developed a subsystem that provides state analysis rates of up to 125 MHz and timing analysis for up to 32 input channels at rates of 200 and 400 MHz. Designated the HP 64610S, the analyzer is an extension of and a replacement for the HP 64600S logic timing/hardware analyzer. The expanded feature set of the new subsystem is provided by a control board that accepts an external clock, new operating software, and two additional eight-channel data-acquisition boards. Existing HP 64600S subsystems can be upgraded to include the new features. Prices for the HP 64610S range from $7000 to $20,000, depending on the number of channels selected.

CIRCLE 371

Software speeds gate-array design

A software package that improves productivity in the design and test of CMOS gate arrays by as much as 50% has been released by **International Microcircuits Inc. (Santa Clara, Calif.)**. Called Easygate, the application utilities software permits the design of 2- to 4-μm arrays (from 240 to over 5000 gates) on Daisy or Mentor CAE workstations. Easygate features line delay corrections for fan-out, temperature, and voltage, and the user can run simulations using Sentry-compatible test vectors to verify both design and testability. Once completed, the final design can be sent to IMI on an 8-in. floppy disk. A Daisy Logician workstation, including the Easygate software, can be leased from IMI.

CIRCLE 372

8-in. Winchesters access 35% faster

The average access times of an entire family of 8-in. Winchester disk drives have been reduced by 35%. **MegaVault Memories (Woodland Hills, Calif.)**, the manufacturer of the disk drives, reports that access times have dropped from 38 ms to a minimum of 25 ms for all models, which range in capacities from 83 to 212 Mbytes. The faster access times are the result of replacing ferrite magnets with more powerful rare-earth magnets and incorporating a special iron housing to improve the magnetic circuitry, enabling the head actuator to achieve higher positioning speeds. Additionally, the microprocessor was reprogrammed.

CIRCLE 373

Card adds ac capability to analog IC tester

Developed by **Pragmatic Test Systems Inc. (Milpitas, Calif.)**, an expansion card adds ac functions and measurement capabilities to the dc parametric test capabilities of the company's TM-7A and TM-7B linear IC test heads. Up to four cards can be plugged into the expansion bus of the test systems to provide combinations of programmed sine, square, and triangle waves—0 to 12 V amplitude, with or without dc offset, at frequencies of 40 Hz to 100 kHz to any pin on the test head matrix. Additionally, the power supply voltages of the device under test can be modulated to evaluate device characteristics (such as noise immunity). Op amp slew rates (from 0.1 to 500 V/μs) can be measured by specifying the measurement parameters in a few lines of Basic-like code. Rms voltage measurements have 16-bit resolution.

CIRCLE 374

Z family μPs can be surface-mounted

SGS Semiconductor Corp. (Phoenix, Ariz.) is packaging its family of Z type microprocessors and peripherals in space-saving surface-mounted enclosures. Quad-in-line, J-bend-type chip carriers (plastic or ceramic) can be specified for the Z8, Z80, Z8000, and Z8500 product lines. The devices are available for the commercial, industrial, and military temperature ranges, as well as with a $\pm 10\%$ power supply range. Future prices of the surface-mounted devices in volume production quantities are expected to be nearly equivalent to that of their dual in-line counterparts.

CIRCLE 375

Software derives tests from design data

Jointly developed by **Daisy Systems Corp. (Sunnyvale, Calif.)** and **Factron/Schlumberger** (formerly Fairchild Test Systems), a software interface package links Daisy's CAE workstation with Factron's test systems to reduce the design-to-manufacturing cycle of complex VLSI-based boards. Information generated during the design phase is captured and translated into a test program, which is used for production testing or debugging through a guided-probe technique. By linking the design data base to the test system, the time required to develop the board test programs can be reduced by as much as 50%. The software package can be purchased from either company for $3800.

CIRCLE 376

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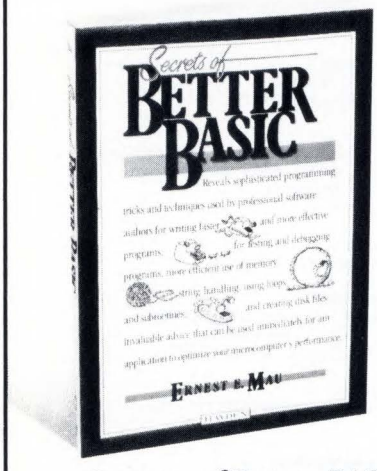

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APPLICATION NOTES

Digital voice and T-1 transmission

The first of a series of technical backgrounders, *Digital Voice and T-1 Facilities* is a 16-page booklet that examines concepts central to digitizing voice and the effective utilization of T-1 (1.544-Mbit/s) transmission facilities. Accompanying diagrams illustrate key points made in the text, while technical concepts are presented in a straightforward manner.

Timeplex Inc., 400 Chestnut Ridge Road, Woodcliff Lake, N.J. 07675; (201) 930-4600.

CIRCLE 377

Designing EMI shielding windows

Considerations of EMI shielding-window design are explored in a 40-page brochure, written to assist the designer in conducting a detailed review of transparent barriers used for viewing and EMI shielding of large window areas. Specific treatment of EMI shielding performance, optical performance, optically clear window substrates, contrast enhancement, and assembly and mounting techniques are among the topics covered. Characteristics of CRT phosphor screens and a glossary of terms are also included.

Tecknit, Corporate Communications, 129 Dermody St., Cranford, N.J. 07016.

CIRCLE 378

Optical encoder design guide

A 12-page pamphlet assists the design engineer in specifying the proper encoder to meet specific application requirements. The primer differentiates between absolute and incremental styles of encoders and explains the use of tachometer- and quadrature-type outputs. The literature also describes various count multiplication techniques and contains a glossary of terms and typical application examples.

BEI Motion Systems Co., Industrial Encoder Division, 7230 Hollister Ave., Goleta, Calif. 93117.

CIRCLE 379

Custom hybrid microcircuit design

Entitled *An Electrical Design Guide for Users of Hybrid Microcircuits,* this 20-page booklet focuses on cost-effective approaches to circuit design in order to optimize performance. The guide probes digital and analog circuit types, exploring a variety of design, packaging, and implementation considerations. Component selection, circuit partitioning, funneling, derating, and other subjects are discussed.

Teledyne Microelectronics, 12964 Panama St., Los Angeles, Calif. 90066; (216) 267-2700.

CIRCLE 380

Microwave, vibration, and rf test instruments

Containing descriptions, specifications, and applications data, a 334-page hardbound catalog presents instruments used for antenna measurements, determining radar cross section, telecommunciations, spectrum analysis, vibration testing, machine protection, and signal detection and analysis.

Scientific-Atlanta Inc., PO Box 105072, Atlanta, Ga. 30348; (404) 449-2075.

CIRCLE 387

Standard-cell library

Synertek's standard-cell library data book describes the basic functions and operating characteristics of approximately 200 pretested standard cells. TTL and CMOS cross-reference charts, packaging information, and a section on characteristics common to all cells precede each data sheet.

Synertek Inc., PO Box 552, Santa Clara, Calif. 95052; (408) 748-7047.

CIRCLE 388

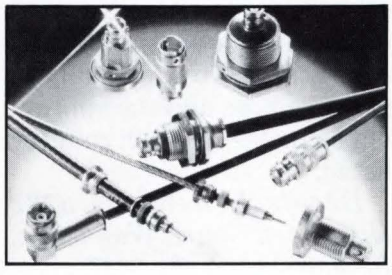
300-baud modem and filter chip set

Data sheets describe a low-power 300-baud modem and filter chip set. The eight-page document includes block diagrams, pin assignments, electrical characteristics, timing charts, interconnection diagrams, and package dimensions.

S-MOS Systems Inc., 50 W. Brokaw Road, San Jose, Calif. 95110; (408) 993-1212.

CIRCLE 389

Miniature coaxial connectors



The Nu-Lok 1200 series of miniature coaxial connectors, designed to meet the requirements of MIL-C-25516, is the subject of a 20-page catalog. The catalog covers the connectors' electrical, environmental, and physical performance characteristics.

TRW Electronic Components Group, Cylindrical Connector Division, 8821 Science Center Drive, Minneapolis, Minn. 55428; (612) 537-1010.

CIRCLE 390

Manufacturing software programs

Over 500 software programs for manufacturing are described in the *1985 Handbook of Manufacturing Software.* Programs include inventory control, CAD/CAM, robotics, and process control software. The book also covers the fundamentals of applying computers to the manufacturing environment.

SEAI Technical Publications, PO Box 590, Madison, Ga. 30650; (404) 342-9638.

CIRCLE 391

D-subminiature filtered connectors

More than 1500 D-subminiature connectors—preassembled with one of seven distributed element filters or one of four capacitor filters—are presented in a catalog. Also detailed are 10-, 26-, 34-, 40-, and 60-pin filtered headers, filtered adapters for circular plastic connectors, and filtered circular metal-shell connectors.

Amp Inc., PO Box 3608, Harrisburg, Pa. 17105; (717) 564-0100.

CIRCLE 392

Catalog describes computer books

A 16-page catalog contains detailed information—including chapter contents and pricing—for a wide variety of computer books. Publications include tutorials on operating systems (e.g., CP/M, iRMX, MS-DOS and Unix), language translators, and 8088 μP design.

Microcomputer Applications, 827 Missouri St., Fairfield, Calif. 94533; (707) 422-1622.

CIRCLE 393

NEW LITERATURE

STD bus cages and motherboards

Forty new STD bus card cages and eight new STD bus motherboards are highlighted in a 12-page brochure, which comes with a separate price sheet that lists prices for Matrix's entire line of STD bus products. Individual product features, mechanical drawings, and optional accessories are covered within the literature. The new introductions, designated group 11, offer systems engineers greater customization for STD bus systems and eliminate many of the previous packaging restrictions.

Matrix Corp., 1639 Green St., Raleigh, N.C. 27603; (919) 833-2837.

CIRCLE 381

Ac power sources and uninterruptibles

A wide range of manual, programmable, and microcomputer-controlled ac power sources and uninterruptible power systems are described in a 54-page catalog. The specification data is combined with pricing information and complemented by an informative piece on six major considerations to take into account when comparing the ratings of ac power supplies.

Behlman Engineering Corp., 1142 Mark Ave., Carpinteria, Calif. 93013; (805) 684-8311.

CIRCLE 382

Rocker switches

Internationally approved rocker switches are presented in a catalog that is packed with information. In this first edition, it gives electrical and mechanical specifications, dimensional drawings, and part-number selection codes. Also featured is a reference section listing the various international approval marks and the approving agencies for each country listed.

Dreefs Switch Inc., 3782 Hawthorn Court, Waukegan, Ill. 60085; (312) 662-7667.

CIRCLE 383

Linear supplies and dc-dc converters

A nine-page brochure features linear ac/dc power supplies and modular dc-dc converters. Pc board-mounted supplies range from 5 V at 250 mA to ±15 V at 150 mA; chassis-mounted versions range from 5 V at 1000 mA to ±15 V at 500 mA. Dc-dc converters span 5 V at 100 mA to 28 V at ±190 mA. Application notes discuss power supply test procedures, transients, and thermal derating. The brochure also illustrates grounding techniques for avoiding noise and oscillations.

Analog Devices Inc., Route 1 Industrial Park, PO Box 280, Norwood, Mass. 02062; (617) 329-4700.

CIRCLE 384

Display and control instrumentation

Display and control instruments are the subject of a 45-page catalog that provides complete specifications for a line of analog and digital panel meters, optical and solid-state meter relays, and microprocessor-based temperature controllers.

LFE Corp., Process Control Division, 55 Green St., Clinton, Mass. 01510; (617) 835-1000.

CIRCLE 385

Push-button switches

The 75 Series of push-button switches—manufactured by Rafi of West Germany and marketed through Ledex Inc.—is depicted in a 21-page bulletin (PB-5507). Technical data for each of the device configurations is given, as well as accessory information.

Ledex Inc., PO Box 427, Vandalia, Ohio 45377; (513) 898-3621.

CIRCLE 386

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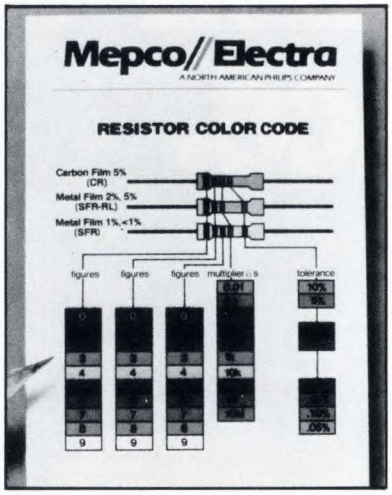
KEY SOLUTIONS FROM SMK

CIRCLE 232

NEW LITERATURE

Chart explains resistor color code



Explaining the part-marking systems used for Mepco/Electra's various resistor products is a four-page pocket-size chart. The chart defines the standard color code used on most carbon-film and metal-film resistors and explains the alpha-numeric systems used on military-screened devices. The chart also includes a table of standard resistance values for the 10-to-100 decade.

Mepco/Electra, Columbia Road, Morristown, N.J. 07960.

CIRCLE 394

X-Y and rotary positioning tables

Precision- and commercial-grade positioning tables for electronics manufacturing, robotics, and automated assembly are the subject of a 20-page brochure. In addition to selection and application data, the literature contains photographs and mechanical drawings of X-Y, single-axis, and rotary positioners. Also covered are positioning system components, options, and accessories.

Design Components Inc., 1 Kenwood Circle, Kenwood Industrial Park, Franklin, Mass. 02038; (617) 528-7300.

CIRCLE 395

Radiation-hardened bipolar ICs

An eight-page brochure contains 28 detailed graphs that demonstrate device tolerance to gamma radiation. The bipolar ICs that are evaluated for their radiation hardness include inverting op amps, instrumentation amps, low-noise op amps, and precision voltage references.

Micro Power Systems Inc., 3100 Alfred St., Santa Clara, Calif. 95050; (408) 727-5350.

CIRCLE 396

Visual microelectronic package inspection

A handy reference guide covers specifications for the visual inspection of microelectronic packages and covers. The data contained in the 34-page publication is based on the *JEDEC Solid State Products Engineering Council Standard No. 9* (published August, 1984). Topics covered include visual inspection criteria, glass insulators, brazing, lead frame, pins, and many others.

Airpax Corp., W. Johnson Ave., PO Box 8968, Cheshire, Conn. 06410; (301) 228-4600.

CIRCLE 397

Software for the Series 32000 μP

A comprehensive software catalog details the growing base of application, development, and operating system software available for the Series 32000 microprocessor family. The 138-page publication covers nearly 130 products and contains cross-referenced listings of software developed by National Semiconductor and approximately 50 independent software vendors (including addresses, telephone numbers, and availability).

National Semiconductor Corp., Literature Department, 2900 Semiconductor Drive, M/S 23-205, Santa Clara, Calif. 95051; (408) 721-4902.

CIRCLE 398

Special-function VLSI circuits

The *CMOS/NMOS Special Functions Data Manual* (DL130) is a complete compilation of product specification and application information for more than 60 special-function VLSI devices. Chapters for each family of devices include: a-d and d-a converters, decoders and display drivers, op amps and comparators, phase-locked loops and frequency synthesizers, and more.

Motorola Literature Distribution Center, Broadway Bldg. 1, 616 W. 24th St., Tempe, Ariz. 85282; (602) 994-6561. $1.60 (one to nine copies).

CIRCLE 399

NEW LITERATURE

Surface-mounted components

Various types of surface-mounted components are presented in a 24-page brochure, which provides device specifications and dimensional drawings. Products include multilayer ceramic and solid tantalum capacitors; resistor networks; discrete semiconductors, such as transistors and diodes; and integrated circuits, including linear and Hall-effect designs.

Sprague Electric Co., Technical Literature Service, 347 Marshall St., North Adams, Mass. 01247; (413) 664-4411.

CIRCLE 400

General-purpose and standard relays

Fully illustrated with photographs and outline drawings, a 20-page catalog provides technical data for general-purpose, midget, power, miniature power, low-profile, telephone-type, and automotive-type relays. A chart presents the specifications for each of the relay series for quick comparison.

Schrack North America Inc., 3 Westchester Plaza, Elmsford, N.Y. 10523; (914) 592-1305.

CIRCLE 401

Optical waveguides for local networks

The Light Brigade is a reprint of an article describing optical waveguides designed for local area networks. The article discusses the emerging local-access market for optical communications technology and describes the feasibility, component development, waveguide design choices, and the benefits of optical fiber in local-access applications.

Corning Glass Works, Telecommunications Products Division, MP-BH-5, Corning, N.Y. 14831; (607) 974-4432.

CIRCLE 402

Linear and switching power supplies

Over 400 linear, phase-controlled, and switching power supplies for laboratory, industrial, and OEM applications are described in a 100-page catalog. In addition to operating specifications, the catalog contains photos, dimensional drawings, and a matrixed power supply selection chart.

Sorensen Co., 676 Island Pond Road, Manchester, N.H. 03103; (603) 668-4500.

CIRCLE 403

Fiber-optic system testing

A pocket-sized guide covers testing procedures for fiber-optic cables, transmitters, receivers, and system data transmission. It also contains a power conversion chart (dB to W) and a dB-to-% transmission table.

Fotec Inc., 560 Harrison Ave., Boston, Mass. 02118; (617) 542-1719.

CIRCLE 404

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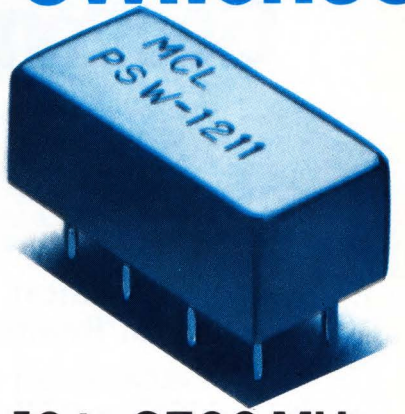
switches



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1000-2000 MHz	25 dB min.
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CIRCLE 229

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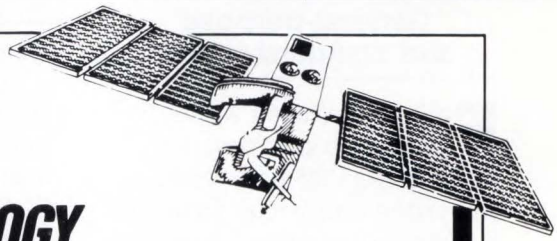

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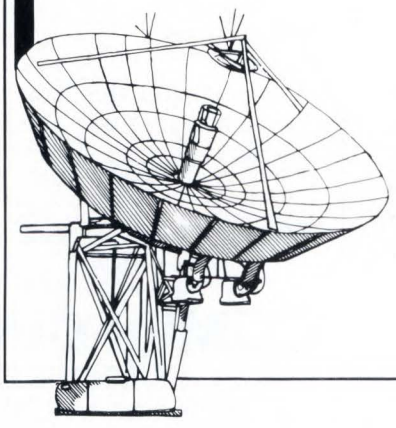

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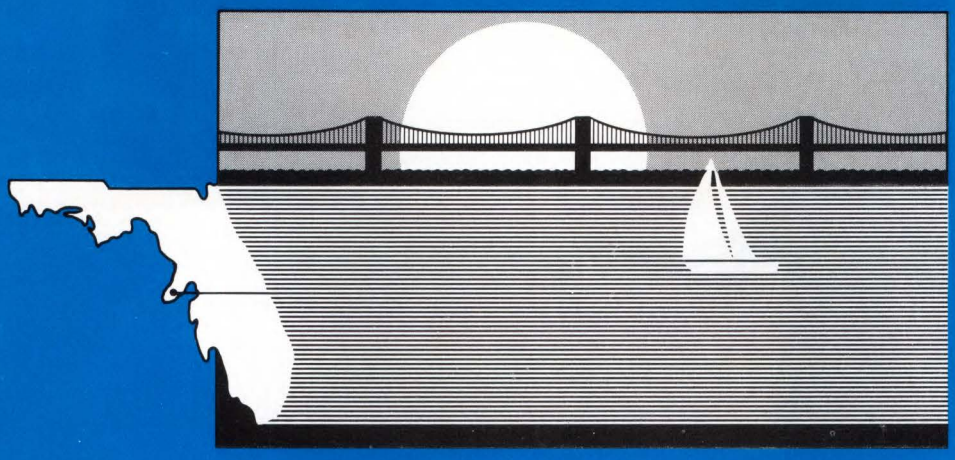

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And also by the technology we produce. At the ECI Division in St. Petersburg, we're involved in building military communications systems, including everything from satellite communications systems and space communications equipment to shipboard terminals, transmitters, receivers and amplifiers. Electronic data handling systems, including transmission systems, teleprinters and digital plotters. Microwave phased array antennas, conformal arrays and adaptive null steering antennas.

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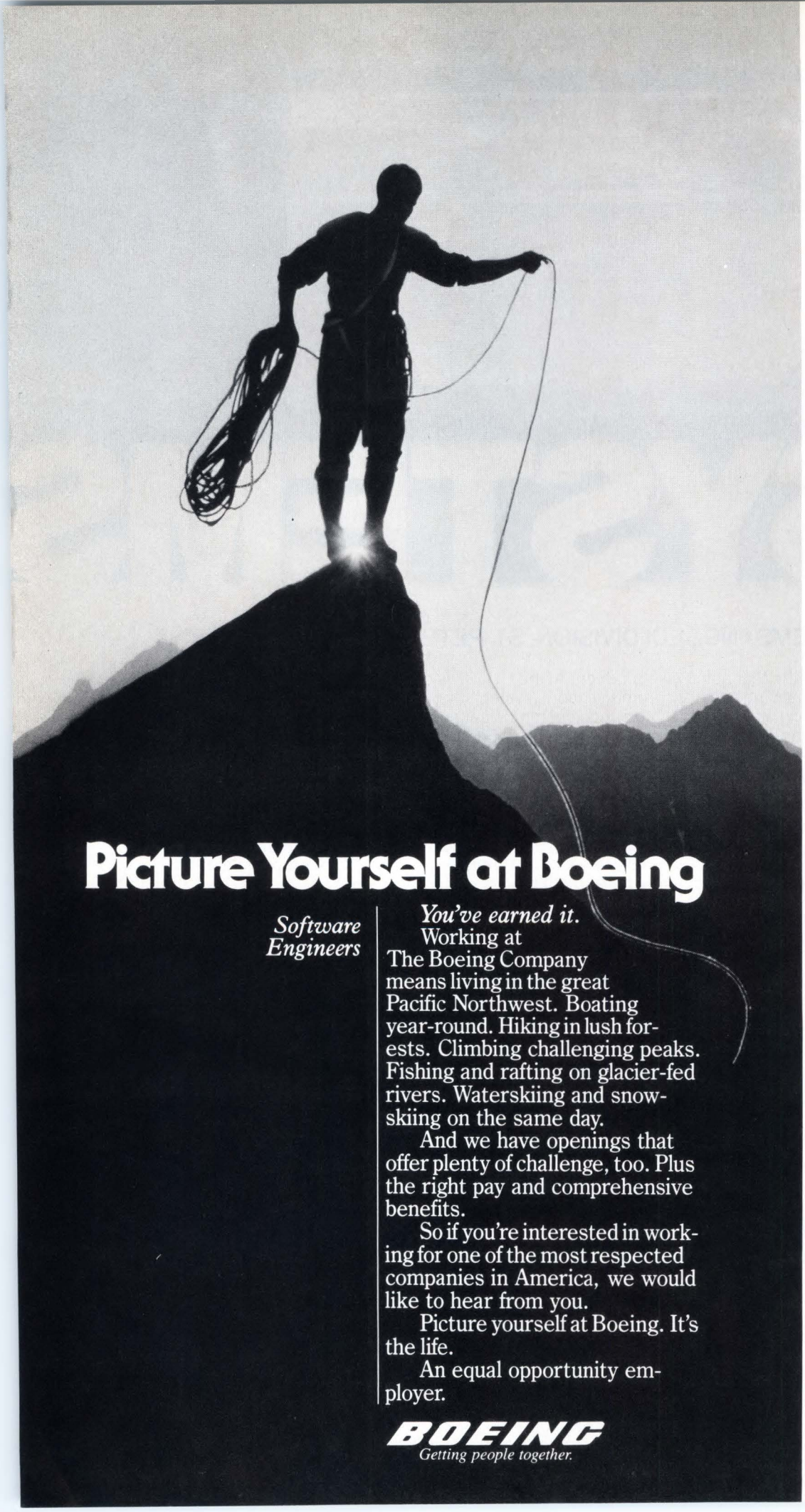

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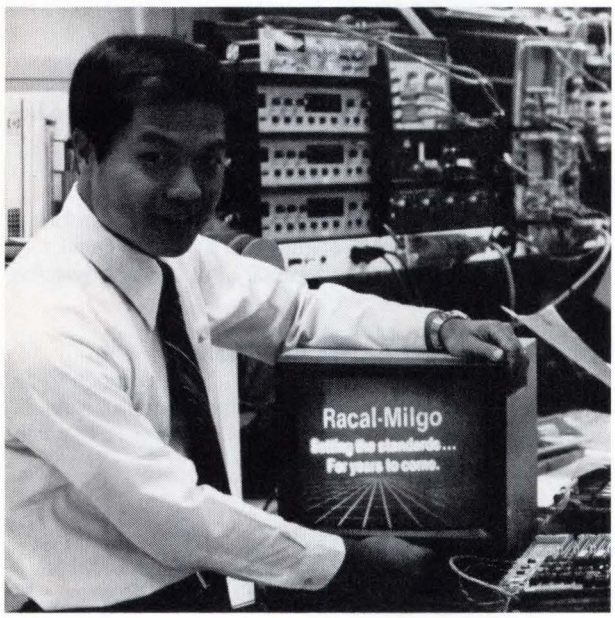

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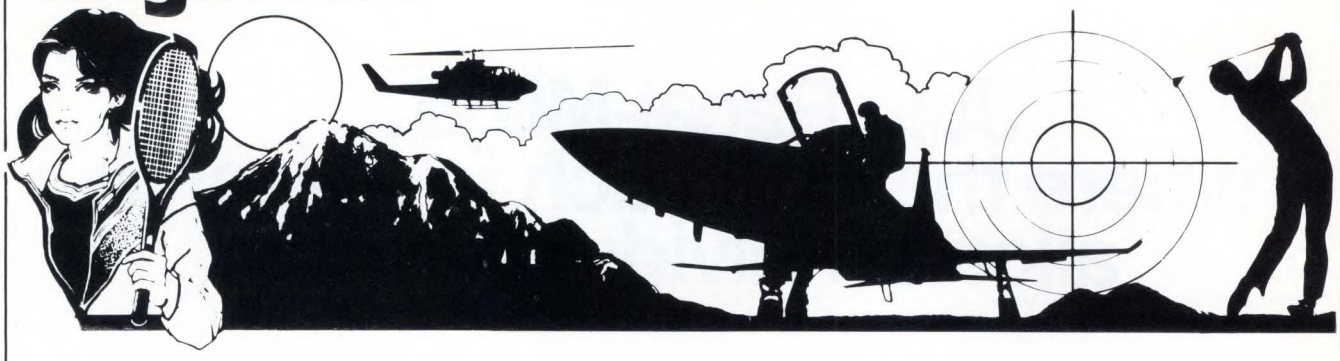

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- **Analog Design**
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- **Programmable Symbol Generators**
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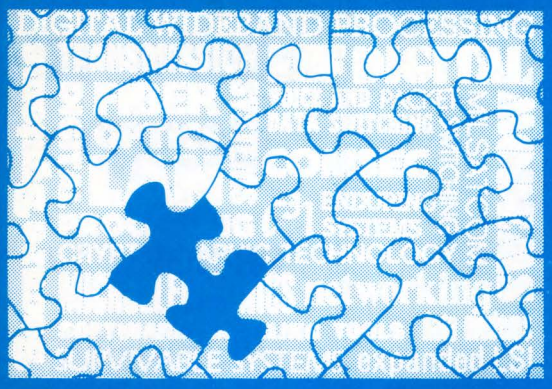

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Send your resume to: Sherry D. Huffer, Dept. ED 1213, GTE's Communication Systems Division, 400 Park Plaza, P.O. Box 13279 Research Triangle Park NC 27709. Or call us at 919-549-1111.

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Educational training must include:

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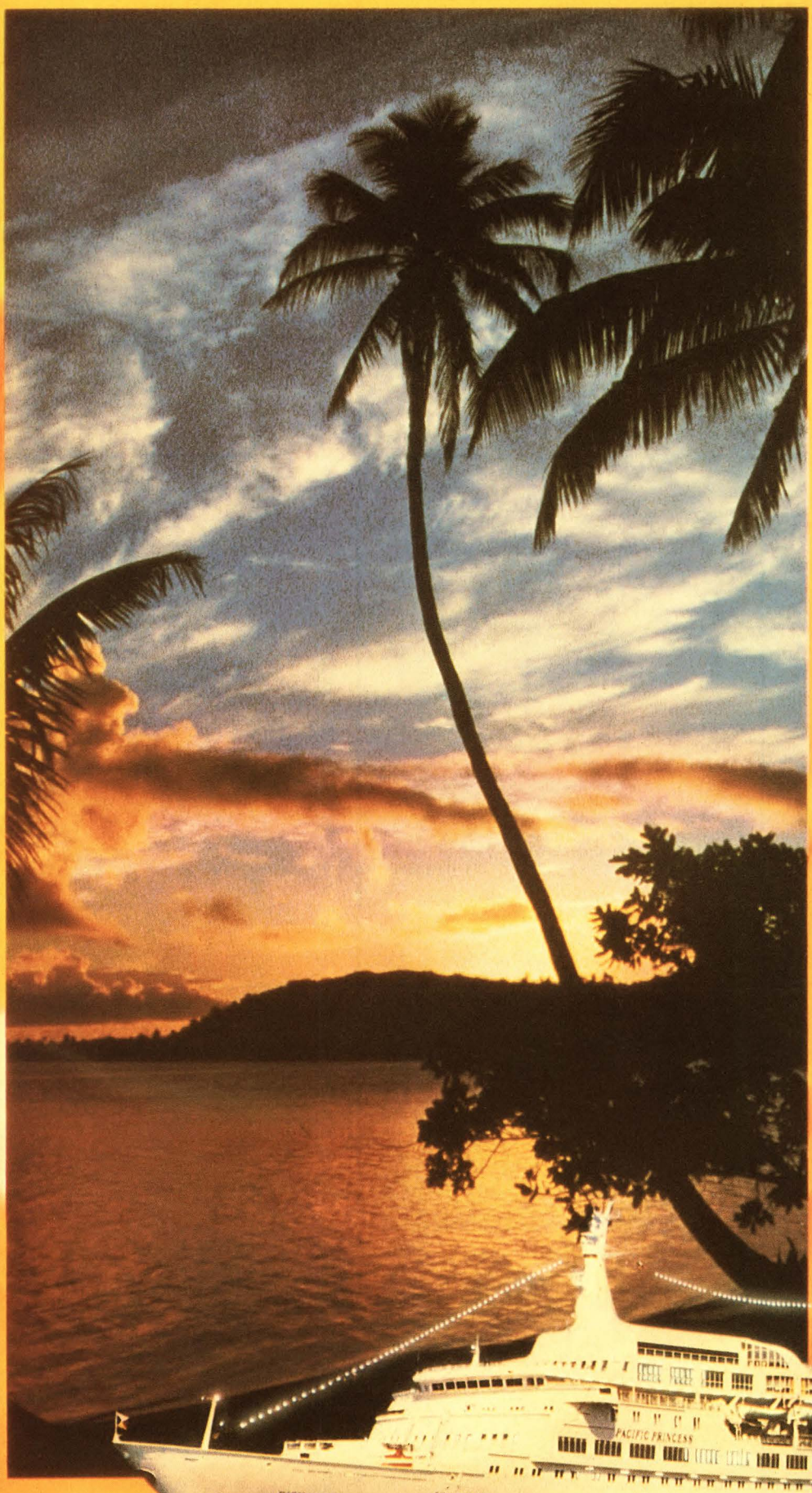

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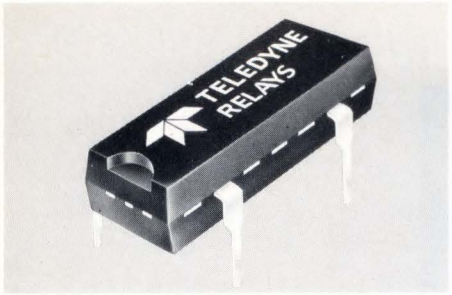

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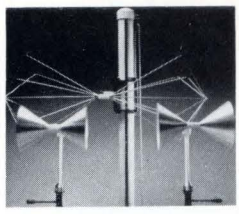

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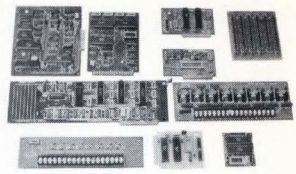

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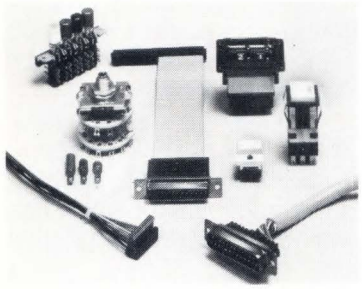

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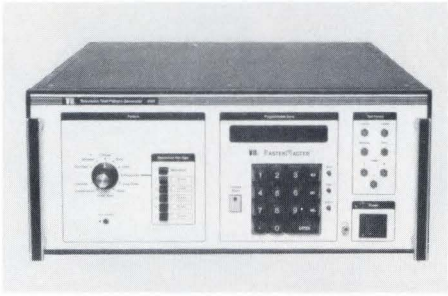

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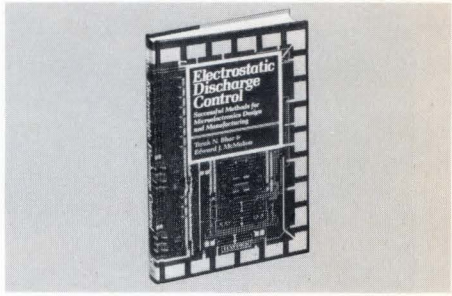

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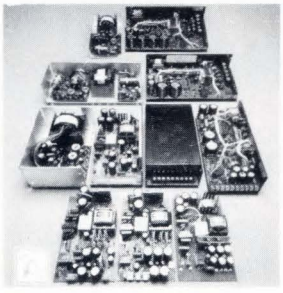

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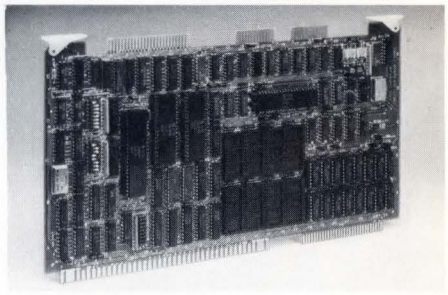

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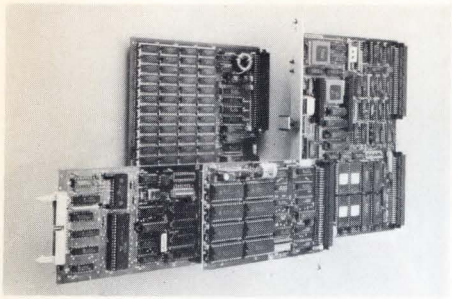

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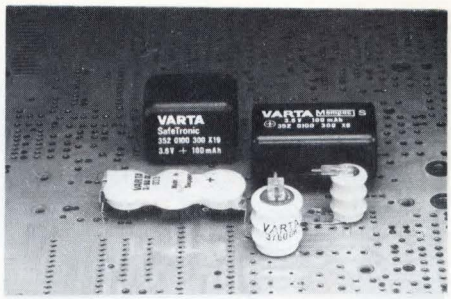

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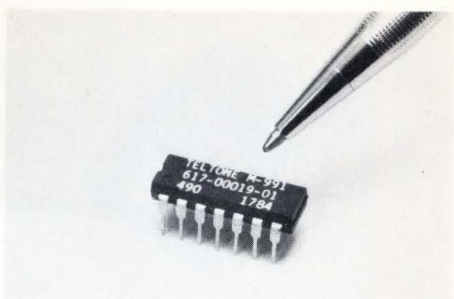

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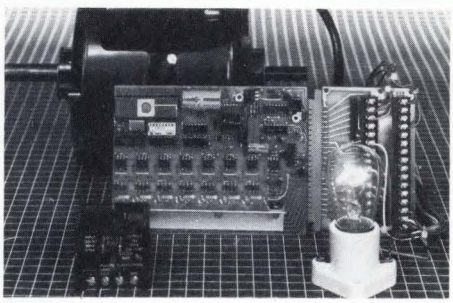

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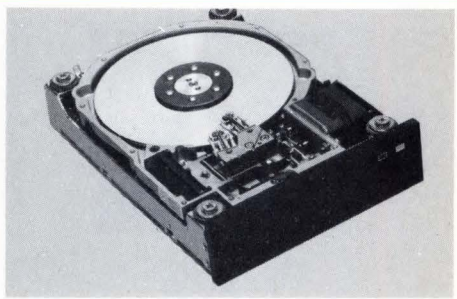

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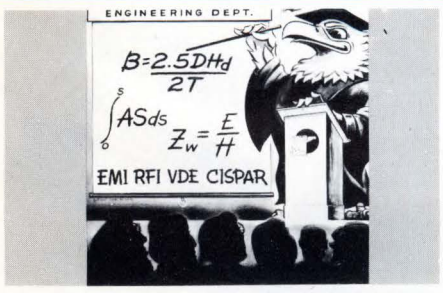

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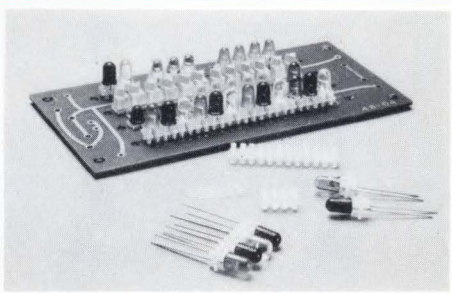

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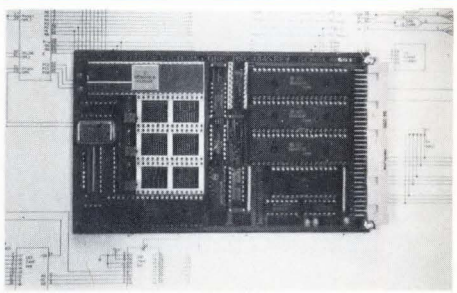

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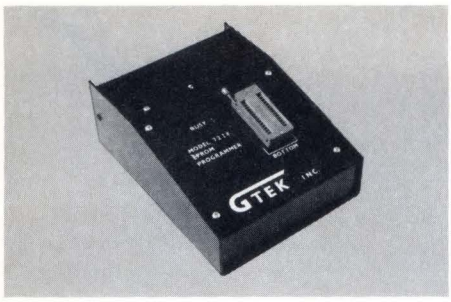

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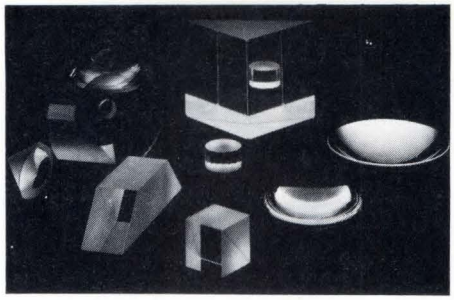

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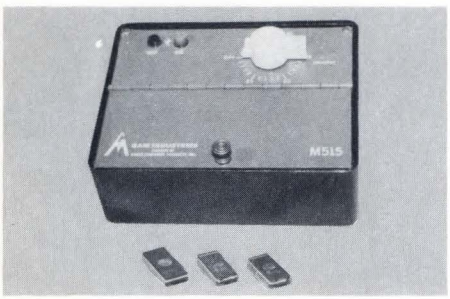

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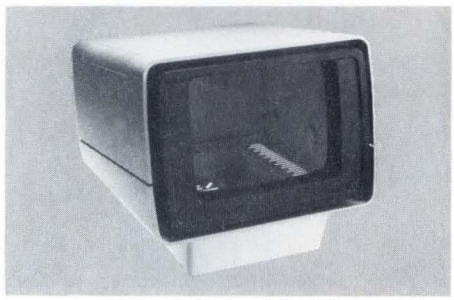

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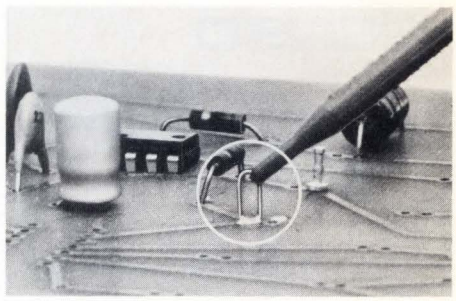

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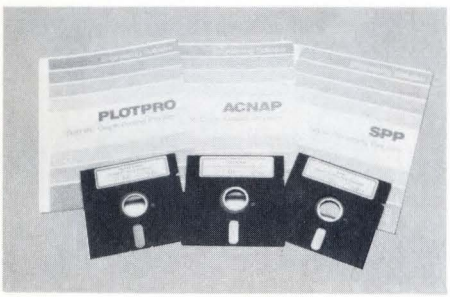

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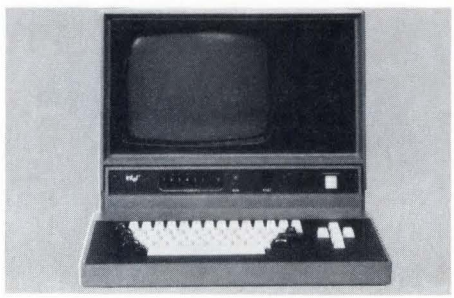

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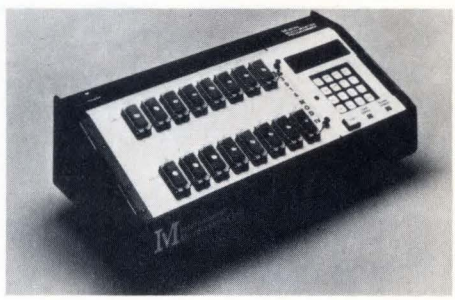

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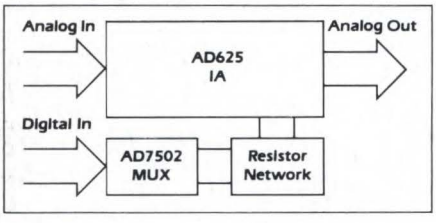

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