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FOR ENGINEERS AND ENGINEERING MANAGERS — WORLDWIDE

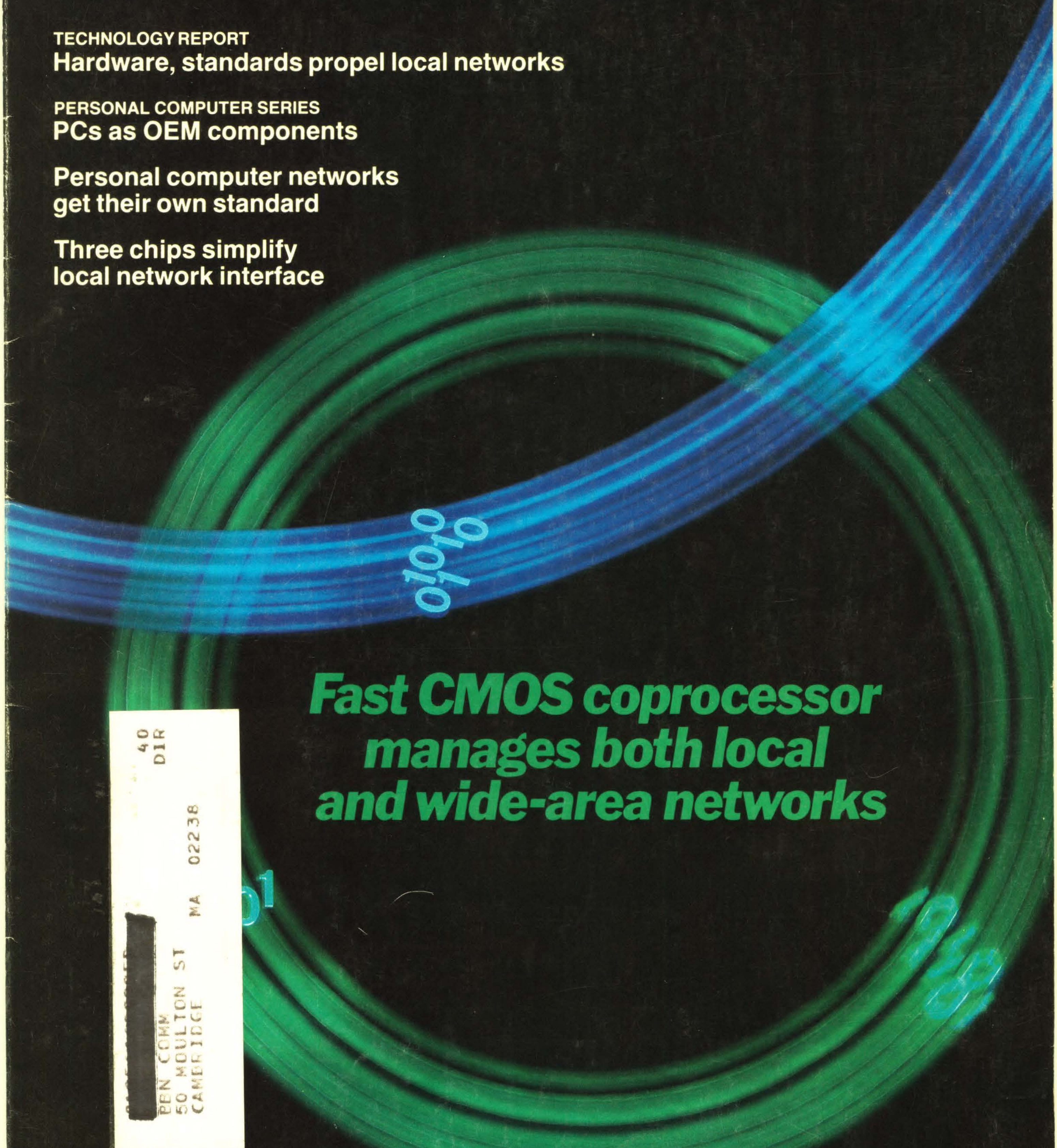
JULY 26, 1984

TECHNOLOGY REPORT
Hardware, standards propel local networks

PERSONAL COMPUTER SERIES
PCs as OEM components

Personal computer networks get their own standard

Three chips simplify local network interface



Fast CMOS coprocessor manages both local and wide-area networks

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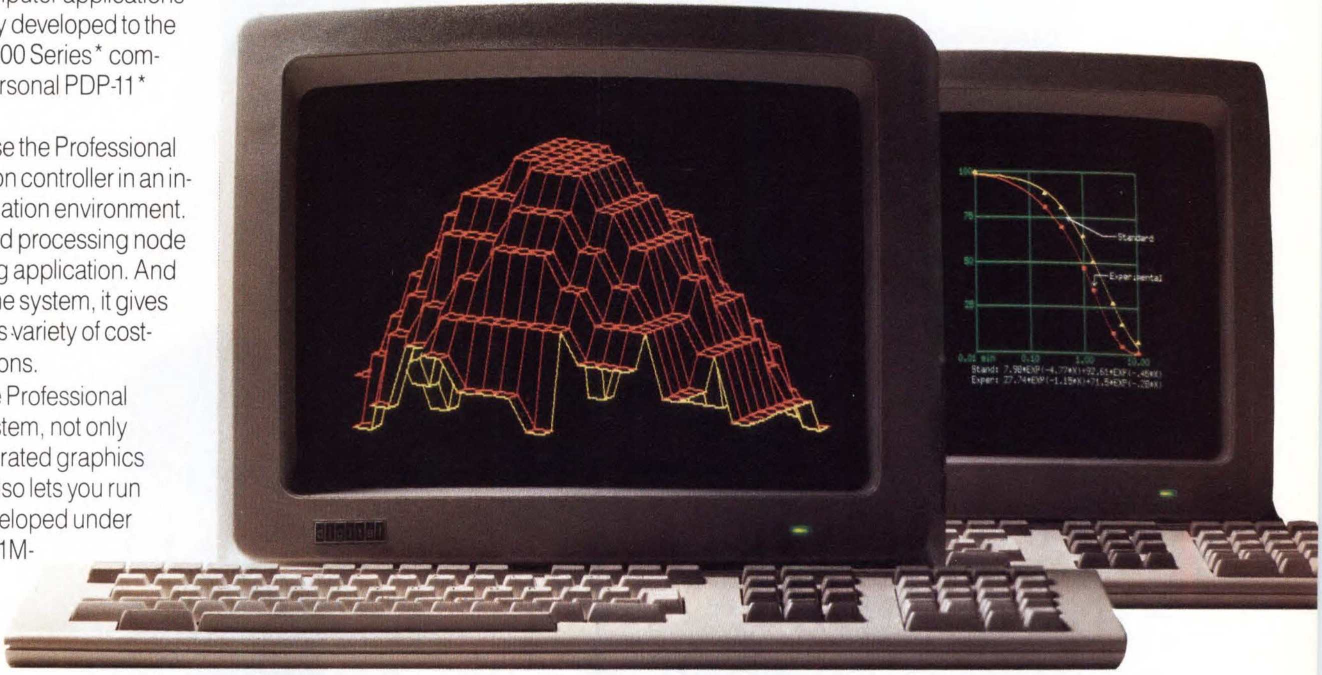

Displayed above is RS/1,* integrated software for scientific and engineering uses from BBN Software Products Corporation, a subsidiary of Bolt Beranek and Newman, Inc.

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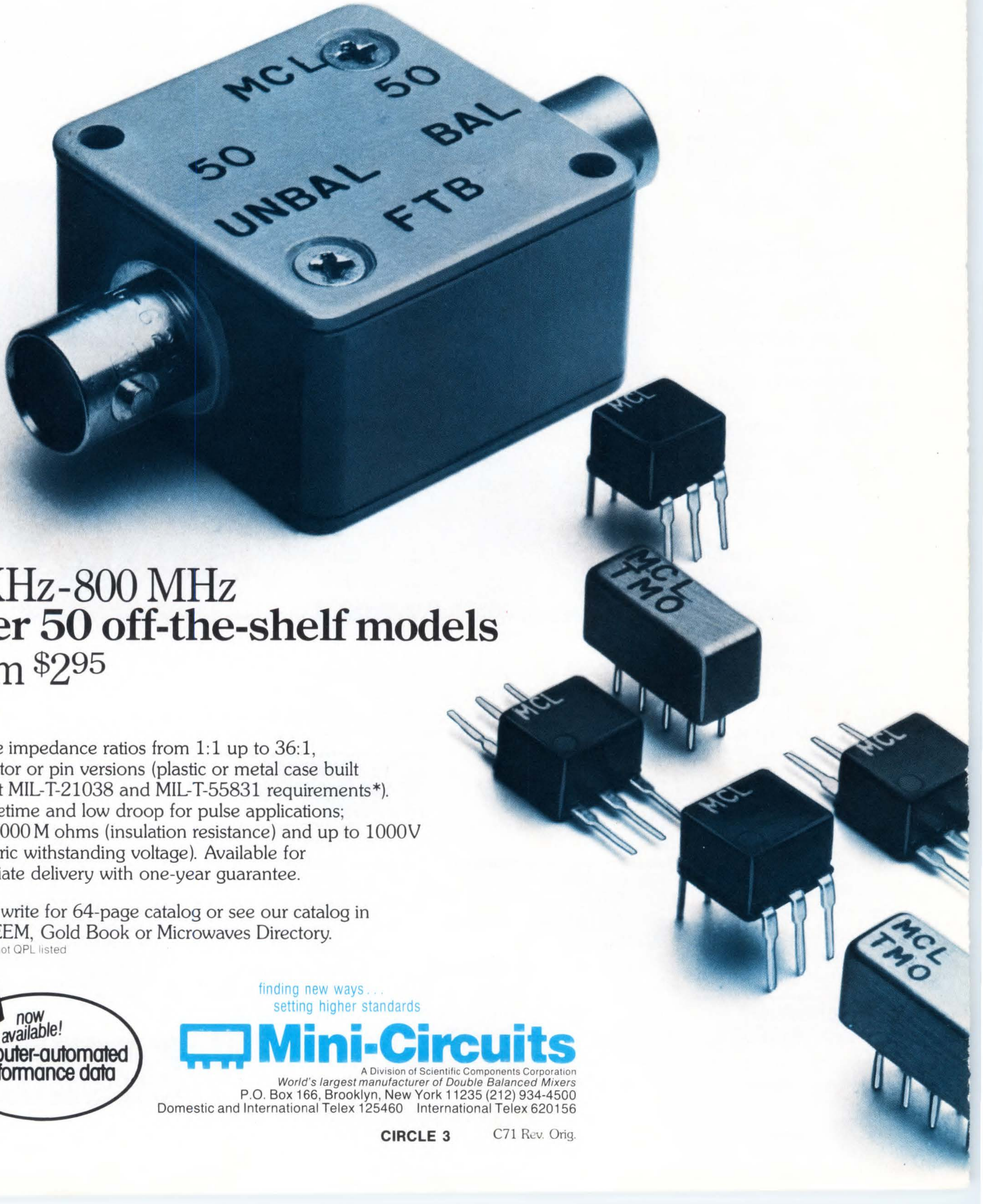

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BEHIND THE COVER

To chip designers at Exel Microelectronics, the ever increasing bit rates of data communications systems proved an irresistible temptation to develop a better mousetrap. And after extensive engineering analysis of the needs of bit-synchronous protocols, they succeeded.

As Alexander Goldberger, the company's manager of technical marketing, explains it, "We wanted to come up with a chip that would do a more complete job for the serial data communications channel, not just one that would offer more channels or more protocols." Certainly the result satisfies the needs of both local- and wide-area bit-synchronous networks.

To define what was to become the bit-oriented communications controller of this issue's cover story (p. 155), Goldberger got together with Stan Kopec, the director of engineering for microperipherals, and Pradip Madan, microperipheral product marketing manager. First, they chose a high data rate—4 Mbits/s—as it matched both users' needs and the estimated performance of the company's new 2-μm dual-metal CMOS process.

Next, "we had to provide an easy way for the designer to take advantage of the high data rate," Madan observes. An on-chip four-channel direct-memory-access controller seemed essential, and its presence made it that much easier to add the rest of a microprogrammed channel processor, which simplifies the task of data and buffer management.

Another decision was not to incorporate high-level protocol functions in the silicon. Otherwise, a different chip would have been needed for SDLC, HDLC, and each of the other bit-oriented protocols.

To actually design the highly complex logic, the team had high hopes of one of the latest integrated CAD workstations. But gaps in its software prevented them from completing the chip on it, and they had to convert the work they had done into files for another system. Some time was lost, but Kopec feels that it was minimal, and "it was still a good experience to learn just how far integrated workstations have progressed."

ElectronicDesign
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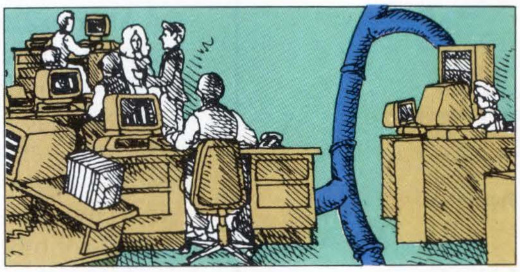
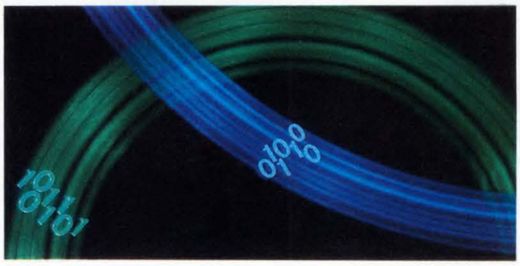
PERSONAL COMPUTER SERIES

NETWORKING



Technology Report

Design Entries



TECHNOLOGY NEWS

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IN THE NEXT ISSUE

Software Technology: a special report on artificial intelligences and a set of design articles on new tools and techniques for software engineering.

Cover photograph by Ken Schroers

135,216 copies of this issue printed

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CONTENTS SPOTLIGHT

Networking 128

Local networks are flourishing. After years of debate over basic questions of technology, each type—baseband, broadband, and PBX—has settled into its own applications area, as our Technology Report documents. And as the foment subsides, a host of chips are appearing to shoulder the various network chores. Some of the most notable, including one chip that simultaneously serves local and wide-area networks (see below), are discussed in four accompanying Design Entry articles. Two other Design Entries describe new low-cost networks.

Cover: Communications coprocessor 155

The very success of local networks brings with it a need to extend their reach—that is, to connect to other networks over long distances. A single chip that handles bit-oriented protocols can simultaneously serve both local- and wide-area networks. It integrates two processors: a 4-Mbit/s data-link controller and a channel processor.

Personal Computer Series 101

OEMs are finding personal-computer-based workstations irresistible. They know that they can create a specialized system simply by mixing and matching the basic hardware of one manufacturer with their own or a third party's application software. But in evaluating the various aspects of personal computers—processors, memory, operating systems, networking, programming—OEMs face a formidable task. A brief profile of 10 representative workstations may help OEM designers weigh the tradeoffs between complexity and cost and formulate their own set of criteria.

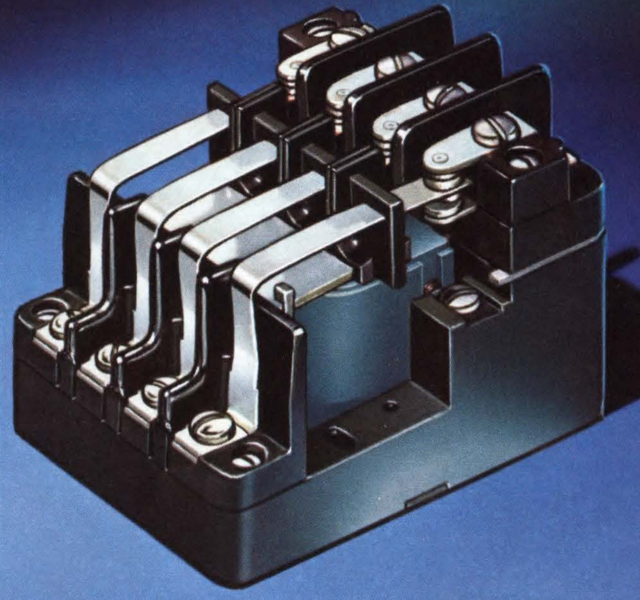
Newsfront: 50-head Winchester drive 37

Multiplying the number of heads found in a typical SMD drive by five could lead to a tenfold reduction in system response time under heavily loaded conditions. According to the calculations of one manufacturer, the figures typically quoted for SMD drives will not hold true for more than 18 requests a second.

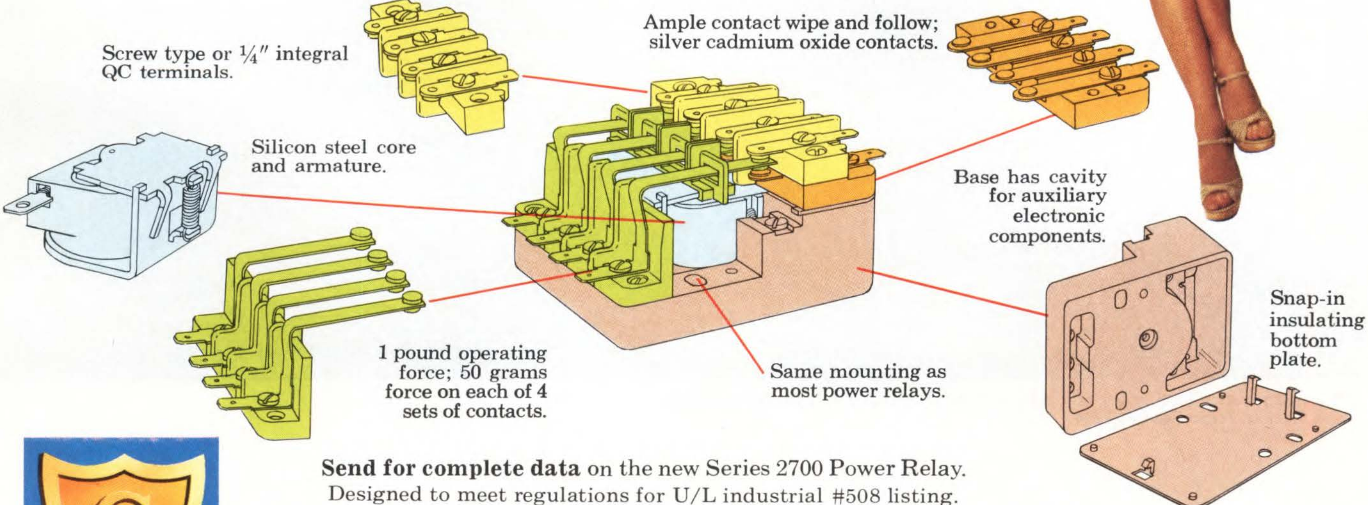
What you see...is what you get

an engineer can sometimes tell how good a product is just by looking at its purity of design...

we think this is one of those times.



This is the new Guardian 4PDT, 25 amp Power Relay.



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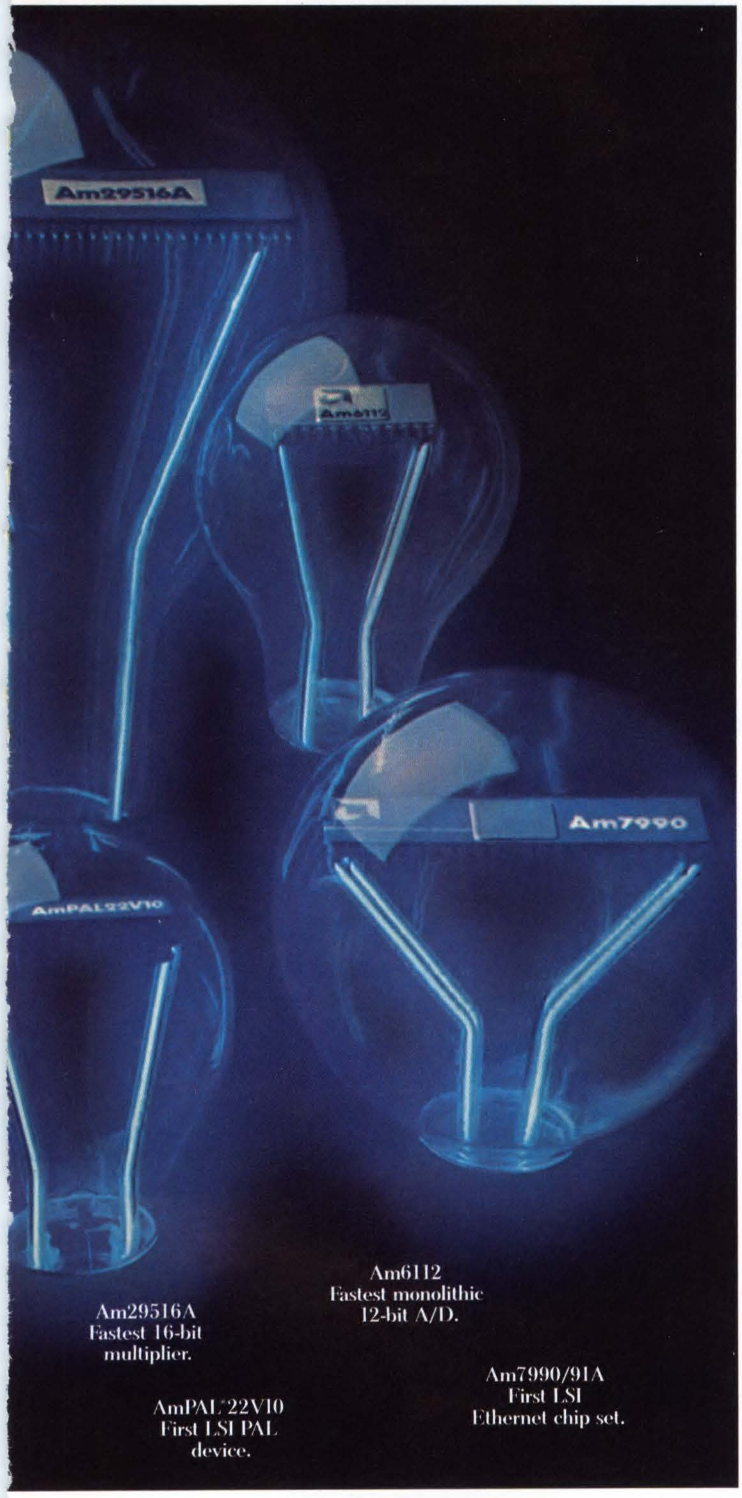

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CIRCLE 6

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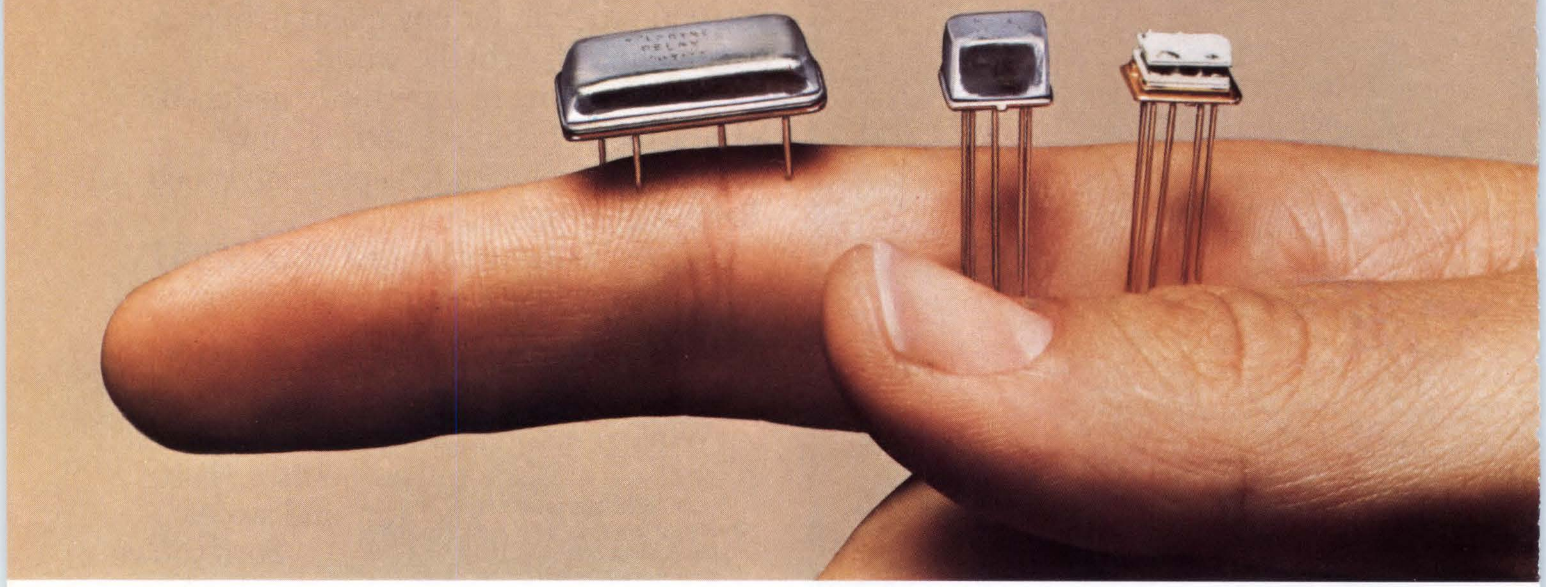

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CIRCLE 7

ON REFLECTION

Unix: Let's have one operating system for one and all

Billions of dollars are wasted every year because there is no one standard operating system for engineering applications. The waste occurs when an application program written for one manufacturer's computer must be rewritten to run on another manufacturer's machine.

After 15 years of this situation, a solution finally seemed to be forthcoming in the form of Unix. Soon, it appeared, we would have a dream come true—one standard operating system for every engineering computer.

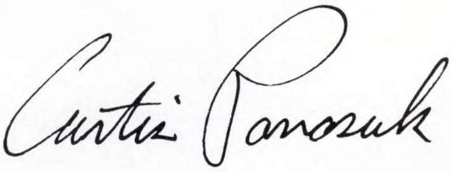
However, it was not meant to be. In fact, it has become all too apparent that a standard operating system is still a fantasy. Unix has now splintered into over 70 different versions—System III, System V, Berkeley version 4.1, Berkeley version 4.2, Zeus, Onix, CPIX, Unos, Xenix, and on, and on. Consequently, an application program written for a computer that uses, say, Berkeley version 4.1 will not likely be able to run without modification on equipment using System V. Thus, after having a possible solution within our reach, we're in effect back to the same old problem of each computer using a different operating system.

There are so many variations on Unix because each company starts with a very rudimentary version of AT&T's original and, with its own ideas of what its customers want, adds frills and other features such as file locking or real-time processing. Since there has been no pattern or guideline to follow to keep all the implementations the same, they wind up incompatible.

Now the hope of a standard has been restored because of the efforts of the /usr/group, a collection of technical experts representing users, universities, and manufacturers such as AT&T, DEC, and IBM. The group's goal is primarily to ensure the applications portability of Unix and secondarily to make the operating system hardware-independent.

Its first success has been to produce the 1984 /usr/group Unix standard, a document that proposes a single set of Unix system calls and subroutines. The document (which is available from /usr/group, 4655 Old Ironsides Drive, Suite 200, Santa Clara, Calif. 95050) was recently overwhelmingly approved by the group's membership. In addition, ANSI is now considering it for its own Unix standard.

If everyone writes their Unix implementations according to this document, an application program created for one machine should be able to run on any other machine. Thus the dream of a standard operating system may again be on the verge of coming true—but it won't unless the industry abides by it.



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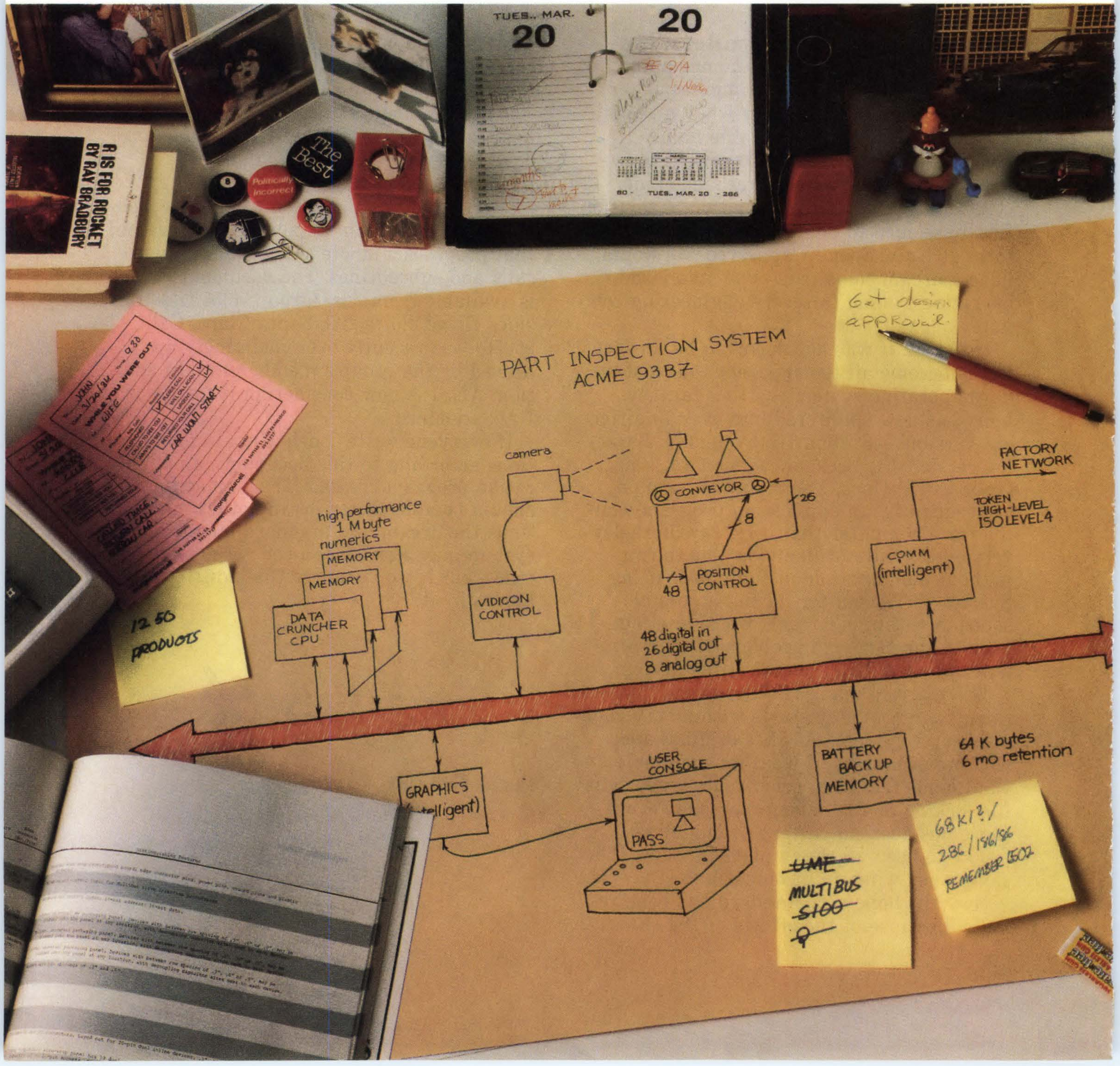

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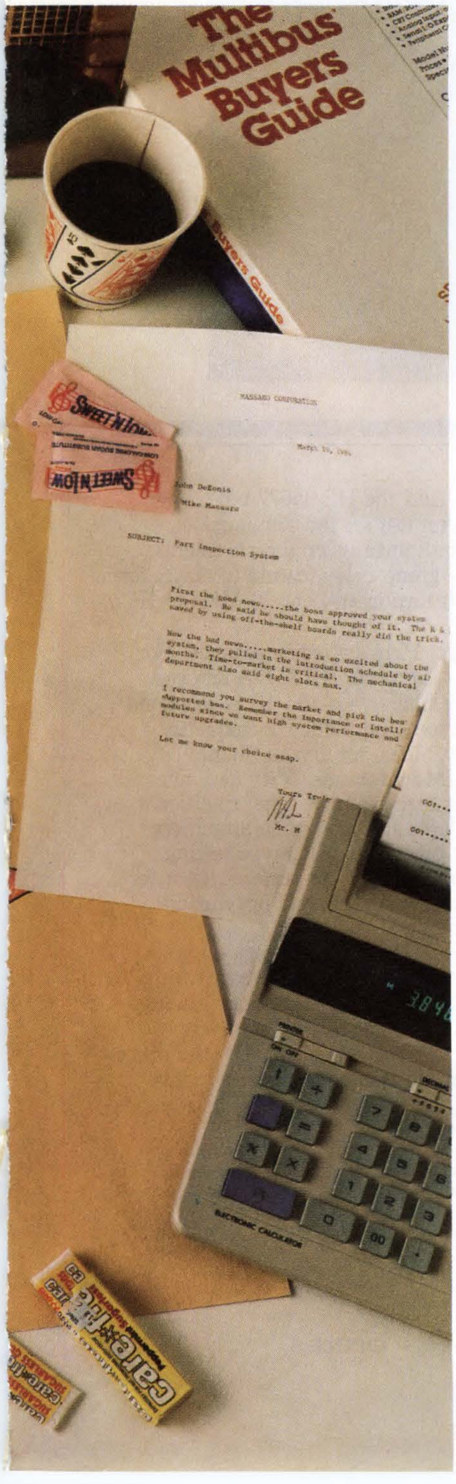

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*Source: MULTIBUS Buyer's Guide, Winter 1984.

CIRCLE 8

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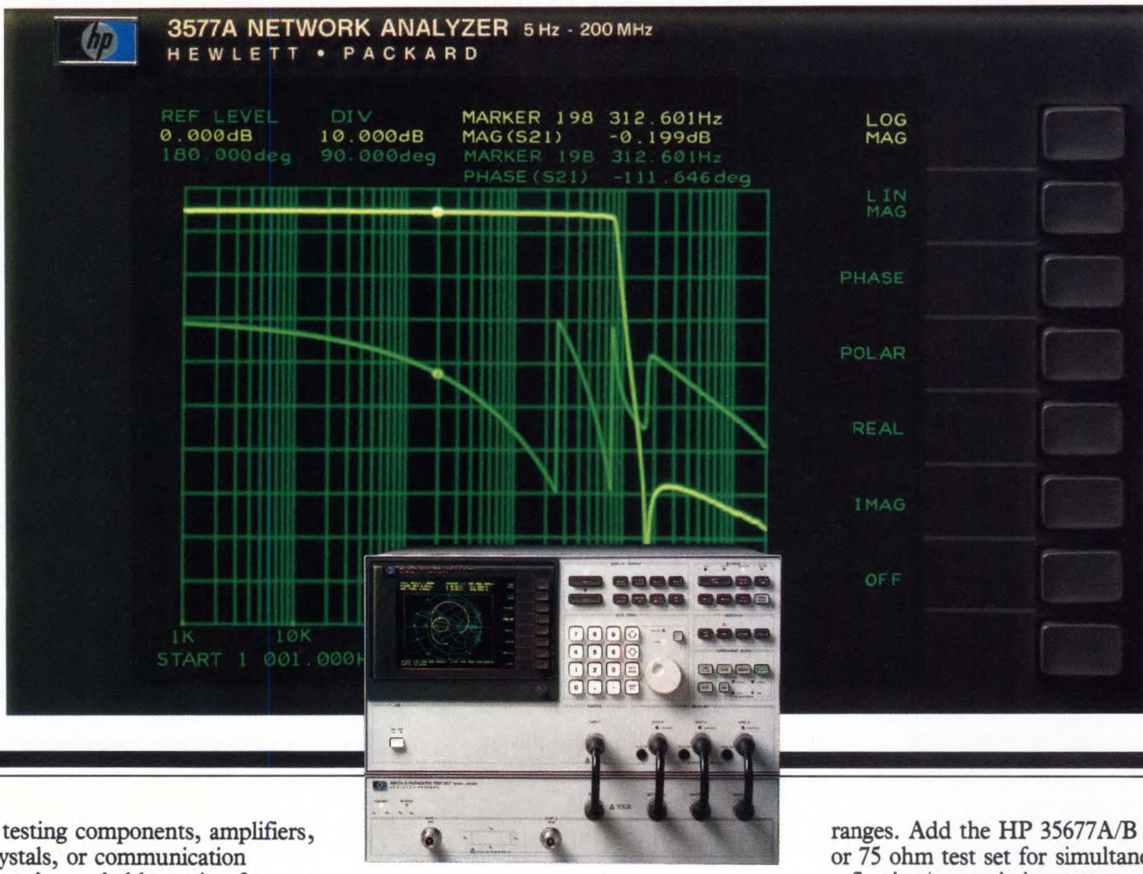

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CIRCLE 9

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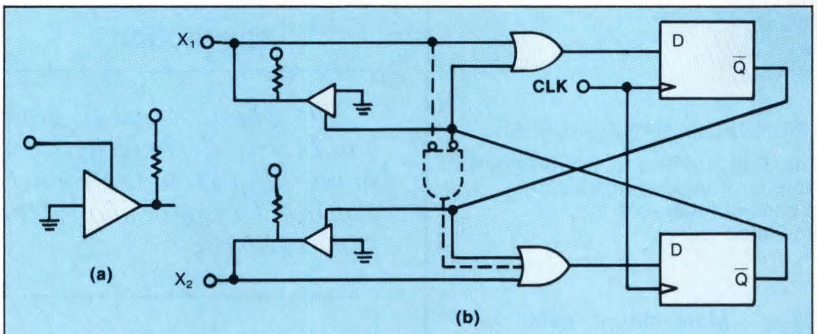
READER FEEDBACK

Open-collector outputs make a simpler buffer

I would like to make a suggestion regarding the Design Solution "PLA Flip-Flop Circuit Buffers Bidirectional Microprocessor Lines" in the May 17 issue (p. 252). The 16R4 PAL has three-state outputs, but it can be configured to have open-collector outputs as shown in part a of the figure, producing the bidirectional buffer shown in part b. Using the four equations given in part c to program the PAL yields the simplified circuit shown in part d.

C. Kao
PAL Design Specification
Monolithic Memories Inc.
Santa Clara, Calif.

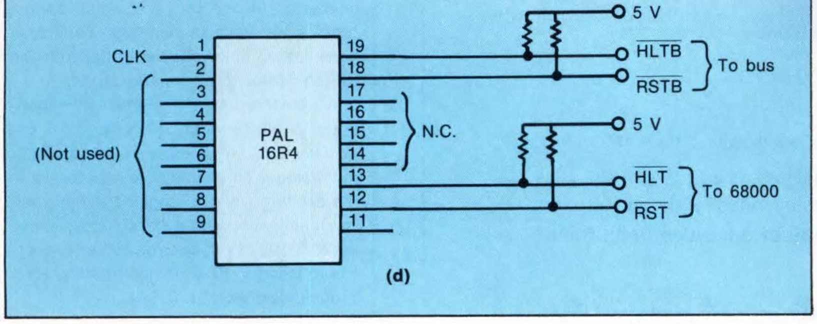
The author replies: *The suggestion of Mr. Kao is correct, but it needs a more advanced PAL device than the 16R4, one that allows independent control of each flip-flop three-state output.*




```
PAL16R4

BUS TRANSCEIVER
CLK 2 3 4 5 6 7 8 9 GND
/OC /RST /HLT /Q3 /Q4 /Q1 /Q2 /RSTB /HLTB /VCC
Q4 := /HLT + /Q3
Q3 := /HLTB + /Q4 + HLT* Q3
Q2 := /RST + /Q1
Q1 := /RSTB + /Q2 + RST* Q1
IF (/Q4) HLTB=VCC
IF (/Q3) HLT=VCC
IF (/Q2) RSTB=VCC
IF (/Q1) RST=VCC
```

(c)



READER FEEDBACK

Not just for private use

Your May 17 Technology Report on digital signal-processing chips [p. 100] was most timely.

However, there is one point concerning our finite-impulse-response filter chip that should be clarified. The report implies that the chip is only for internal use. Actually, it is a regularly available IBM product.

James Day
International Business Machines Corp.
Bethesda, Md.

Correction

The phone number given for Linear Technology Corp. in our May 17 New Products section (p. 260) should be (408) 942-0810.

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Editor-in-Chief, Electronic Design, 10 Mulholland Drive, Hasbrouck Heights, N.J. 07604. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.

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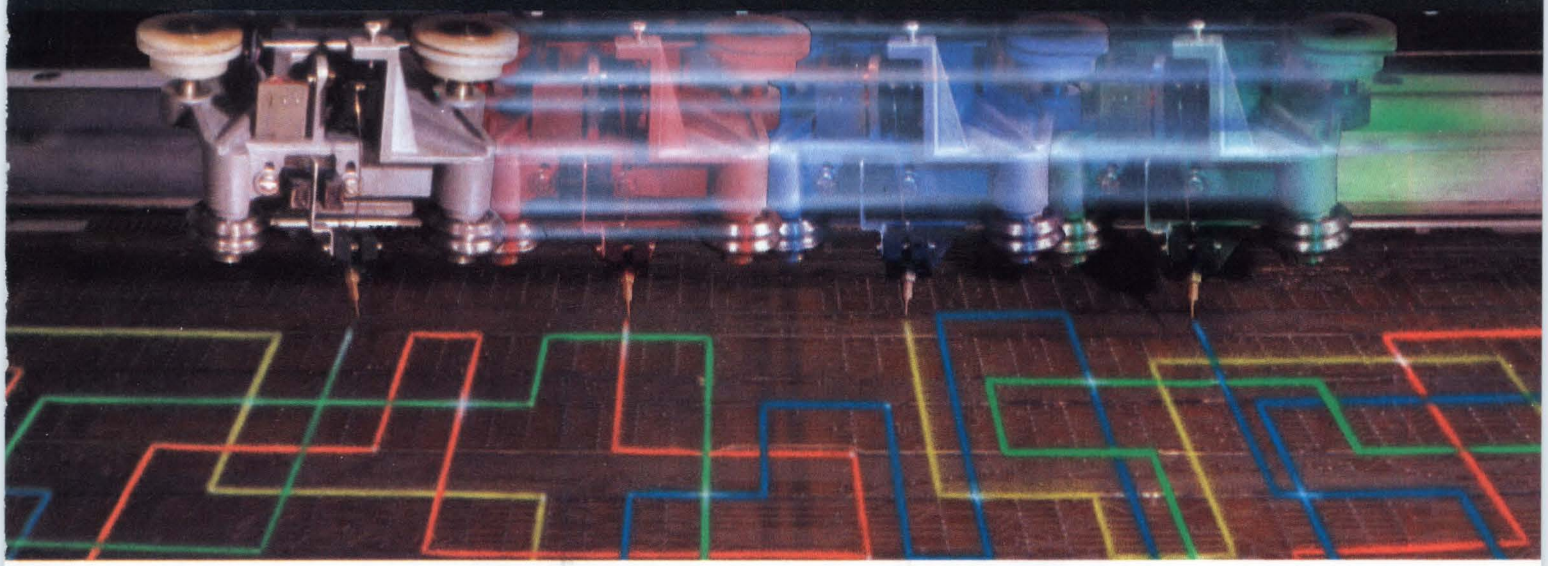

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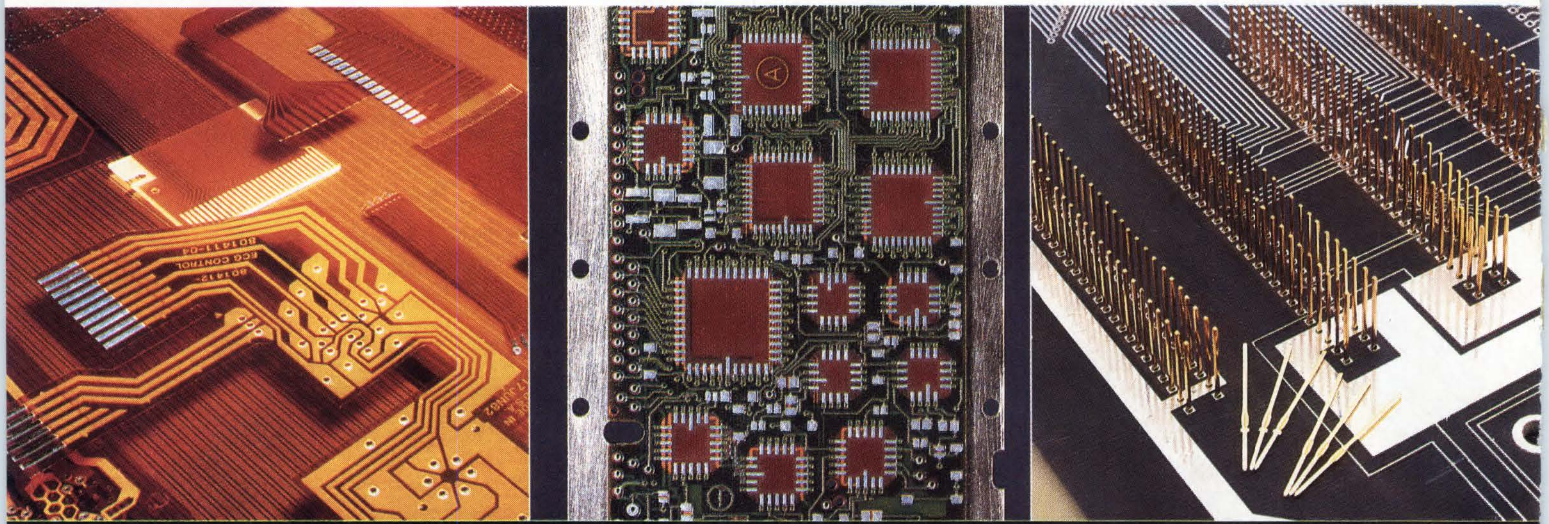
CIRCLE 126 FOR INFORMATION
CIRCLE 127 FOR DEMONSTRATION

Interconics

The new name in interconnects for maximizing miniaturization



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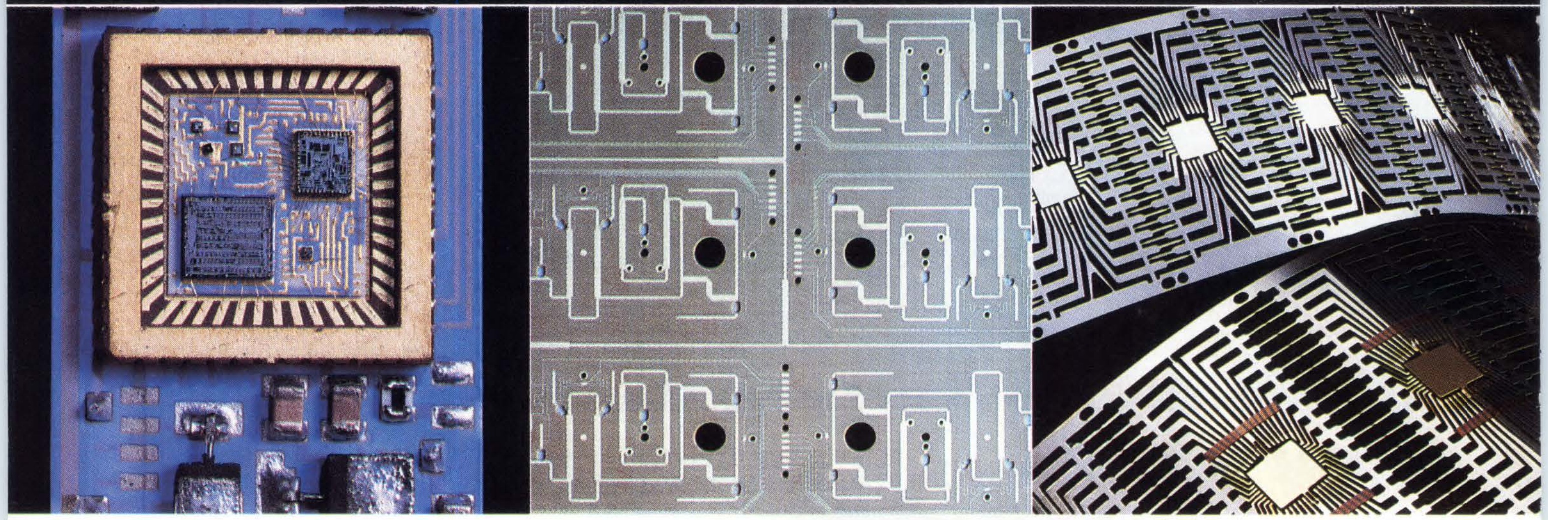

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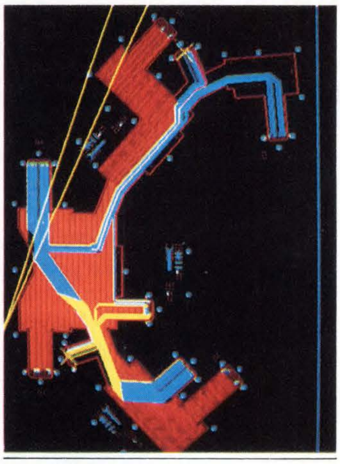

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Advanced Interconnect Products and Technologies

Interconics

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CIRCLE 13

U.S. MEETINGS

1984 Microcircuit Pure Materials Conference, Aug. 2–3. Hyatt Hotel, San Jose, Calif. Pat Westly, Westley Enterprises, 3697 South Court, Palo Alto, Calif. 94306; (415) 494-7115.

American Association for Artificial Intelligence, August 6–10. Performing Arts Center/University of Texas, Austin, Texas. Claudia Mazzetti, AAAI, 455 Burgess Drive, Menlo Park, Calif. 94025; (415) 328-3123.

1984 ASME International Computers in Engineering Conference & Exhibit, Aug 12–16. Las Vegas Hilton Hotel, Las Vegas, Nev. The American Society of Mechanical Engineers, 345 E. 47th Street, New York, N.Y. 10017; (212) 705-7100.

Computers/Graphics in the Building Process, Aug. 19–23. Hyatt Regency, San Francisco, Calif. Dorothy Bomberger, BP '84, 2033 M St., N.W. Suite 333, Washington, D.C. 20036; (202) 775-9556.

SPIE's 28th Annual International Technical Symposium, Aug. 19–24. Town & Country Hotel, San Diego, Calif. Sue Knutsen, SPIE, PO Box 10, Bellingham, Wash. 98227-0010; (206) 676-3290.

1984 International Conference on Parallel Processing, Aug. 21-24. Hilton Shanty Creek Lodge, Bellaire, Mich. Olga Cairns, Hilton Shanty Creek, PO Box 355, Bellaire, Mich. 49615; (616) 533-8621.

National Software Show (NSS), Sept. 5–7. Anaheim Convention Center, Anaheim, Calif. Philip Russell, Raging Bear Productions, Inc., 21 Tamal Vista Drive, Suite 175, Corte Madera, Calif. 94925; (415) 924-1194.

Defense Computers-Graphics '84, Sept. 10–13. Convention Center, Washington, D.C. Dorothy Bomberger, DCG '84, 2033 M Street, N.W., Suite 333, Washington, D.C. 20036; (202) 775-9556.

10th Annual Advanced Control Conference, Sept. 10-13. Fowler Hall, Stewart Center, Purdue Univ., W. Lafayette, Ind. Edward Kompass, Control Engineering, 1301 S. Grove Ave., PO Box 1030, Barrington, Ill. 60010; (312) 381-1840.

EASCON '84, Sept. 10-12. Shoreham Dunfey Hotel, Wash., D.C. Larry Whicker, LRW Assoc., 1218 Balfour Drive, Arnold, Md. 21012; (301) 765-7264.

1984 Symposium on VLSI Technology, Sept. 10–12. Vacation Village, San Diego, Calif. Dr. Lewis M. Terman, IBM T.J. Watson Research Center, PO Box 218, Yorktown Heights, N.Y. 10598; (914) 945-2029.

Midcon/84 and Mini/Micro Midwest/84, Sept. 11–13. Dallas Convention Center, Dallas, Tex. Nancy Hogan, Electronic Conventions, Inc., 8110 Airport Boulevard, Los Angeles, Calif. 90045; (213) 772-2965.

UNIX* Systems Expo/84, Sept. 11–14. Convention Center, Los Angeles, Calif. Sally Nestler, Computer Faire, Inc., 181 Wells Avenue, Newton, Mass. 02159; (617) 965-8350.

Voice Input/Output Systems Applications Conference '84, Sept. 11–13. Marriott Crystal Gateway Hotel, Arlington, Va. Leon Lerman, AVIOS, PO Box 60940, Palo Alto, Calif. 94306; (408) 742-2539.

1984 ASM Materials Science Seminar, Sept. 15–16. Westin Hotel, Detroit, Mich. Prof. B.W. Wessels, Technological Institute, Northwestern University Evanston, Ill. 60201; (312) 492-3219.

Compcon Fall '84, Sept. 16–20. Hyatt Regency/Crystal City, Arlington, Va. Gerrie Katz, Small Computer (R)evolution, PO Box 639, Silver Spring, Md. 20901; (301) 589-8142.

DataStorage 84, Sept. 17–19. Fairmont Hotel, Denver, Colo. Terri Noble, Cartlidge & Assoc. Inc., 4030 Moorpark Avenue, Suite 205, San Jose, Calif. 95117; (408) 554-6644.

Fifth Annual Assembly Technology Expo, Oct. 16–18. O'Hare Expo Center, Rosemont, Ill. Richard lewis, Assembly Technology Expo, 2400 East Devon Ave., Suite 205, Des Plaines, Ill. 60018; (312) 299-3131.

International Test Conference 1984, Oct. 16–19. Franklin Plaza Hotel, Philadelphia, Pa. Harry Hayman, PO Box 639, Silver Spring, Md. 20901; (301) 589-8142.

FOC/LAN 84, Sept. 17–21. MGM Grand Hotel, Las Vegas, Nev. Michael O'Bryant, Information Gatekeepers

(continued on p. 21)

U.S. MEETINGS

(continued from p. 19)

Inc., 138 Brighton Ave., Boston, Mass. 02134; (617) 787-1776.

1984 International Microelectronics Symposium, Sept. 17–19. Loews Anatole, Dallas, Texas. Glenn Dowler, International Society for Hybrid Microelectronics, PO Box 3255, Montgomery, Ala. 36109; (205) 272-3191.

Federal Computer Conference, Sept. 18–20. Washington Convention Center, Washington, D.C. Dallas Kinney, Conference Communications, PO Box 368, Wayland, Mass. 01778; (800) 225-5926 or (617) 358-5181.

13th Annual Conference North American Thermal Analysis Society, Sept. 24–26. Marriott Hotel, Philadelphia, Pa. Hal Ferrari, Lederle Laboratories, Bldg. 65B, Pearl River, N.Y. 10965; (914) 735-5000, ext. 3443.

World Conference on Ergonomics in Computer Systems, Sept. 24–25, Los Angeles; **Sept. 25–26,** Dallas, Texas; **Sept. 26–27,** Chicago, Ill.; **Sept. 27–28,** New York, N.Y. Robert Baily, Computer Psychology Inc., 54 E. Main St., PO Box 16, Mendham, N.J. 07945; (201) 543-9009.

Northcon 84 and Mini/Micro Northwest 84, Oct. 2–4. Seattle Center Flag Pavilion, Seattle, Wash. Nancy Hogan, Electronics Convention Inc., 8110 Airport Blvd., Los Angeles, Calif. 00045; (213) 772-2965.

IEEE International Conference on Computer Design (ICCD 84), Oct. 7–11. Rye Town Hilton, Port Chester, N.Y. Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, Md. 20901; (301) 589-8142.

1984 ACM Annual Conference, Oct. 8–10. Hilton Hotel, San Francisco, Calif. Alexander Roth, 9900 Main St., Suite 303, Fairfax, Va. 22031; (703) 385-0211.

Electronics Manufacturing Technologies & Systems 84 (EMTAS 84), Oct. 9–11. North Carolina State University, Raleigh, N.C. Gerri Andrews, Society of Manufacturing Engineers, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500.

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CIRCLE 18

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PERSONALLY SPEAKING

CAE data bases need both better software and industry standards

The lack of a common data base and inadequate data-base management systems continue to plague computer-aided engineering. With the move toward application-specific workstations and the integration of more CAE functions into individual workstations, the development of suitable data-base software must take priority. Fortunately, the first efforts are getting under way.

At the beginning of this year, representatives from various industries, including the CAE, ATE, and semiconductor communities, formed the Electronic Design Interchange Format (EDIF) Committee. The group's initial task has been to develop a standard interface language for the many types of software used to design, test, and manufacture semicustom integrated circuits.

The EDIF language, which has been partially documented within the last few months, defines desirable physical layouts for gate arrays, standard cells, and even fully custom chips, and it provides for electrical descriptions at the finest level of detail for test patterns, process rules, and performance information. The goal is to finalize the language in the third quarter so that companies in the workstation, test, and semiconductor industries can begin to build a common data base starting in the first quarter of 1985.

Similarly, data-base management systems for CAE must be developed and standards agreed to. Existing data-base management systems are not fully suitable for CAE applications, which need to represent numerous levels of detail, as well as heterogeneous relationships in relational data bases.

New relational data-base technology promises, through the use of expert systems, to organize information more efficiently for CAE applications and to be flexible enough for expansion later on. In fact, research is expected to lead to new system software by 1986.

Among the promising approaches is the Ingres relational data base developed from a research prototype at the University of California at Berkeley. Ingres will be further refined as a result of an agreement recently signed by AT&T Information Systems and Relational Technology Inc., which offers Ingres commercially.

Also, new techniques will emerge to protect the integrity of CAE data yet still permit widespread access to it. Researchers, for example, are closely studying how business applications are successfully dealing with data integrity.

With the adoption of standards and the aid of expert systems, engineers should be able to reap the benefits of a common CAE data base and capable data-base management systems in the next couple of years.

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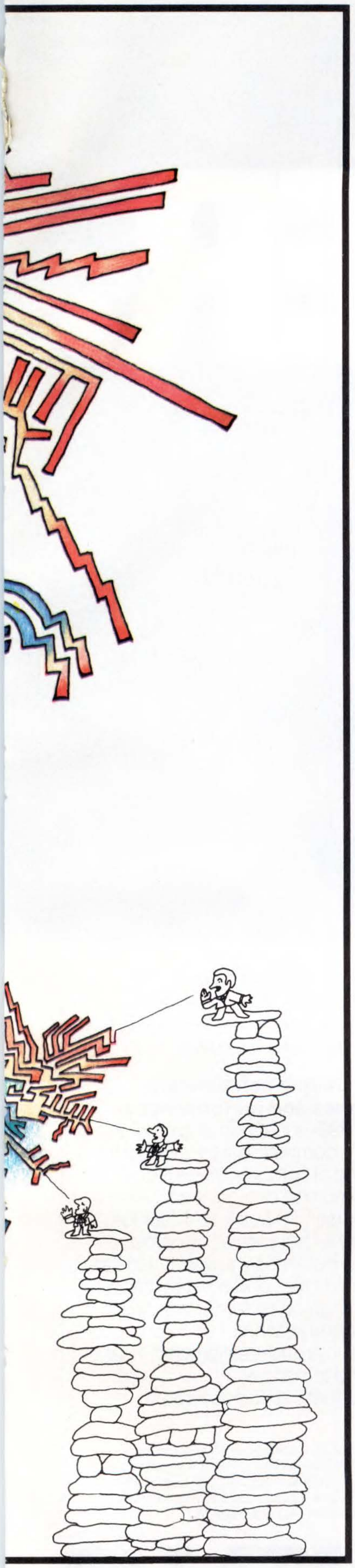

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CIRCLE 12

OVER ACHIEVER.

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Inside, we gave it the technology to make it a universal programmer you can count on having around for a long time.

You see, the 29B's multi-functional programming system gives you complete flexibility to build your programming capacity as your needs grow.

With a now standard 64k x 8 RAM and its proprietary programming electronics, the 29B can program over 1,000 devices in commercial production today, and be expanded to support the more complex devices of the future as they are developed.

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DATA I/O

CIRCLE 19

NEWSPULSE

One-chip controller in the works for IEEE-802.4 LANs

What promises to be the first single-chip controller to meet the IEEE-802.4 specification for token-passing bus networks is now in the late definition stage. The controller, being designed at Motorola Inc.'s Israel Design Center (Tel Aviv), will be built with a 3-μm HCMOS process and will manage a 10-Mbit/s broadband network. It is expected to dissipate 1 W or less and will work with the VMEbus. Also, it will have four DMA channels on board, in contrast to the one DMA channel found on most other Ethernet controllers.

The chip, which should be here before the end of the next year, will be used to link computers in a factory. Until it appears, though, the company is considering working with gate arrays and taking a three-board approach.

Software will turn traditional computers into experts

By next year, conventional computers will be able to assume the capabilities of an expert system, thanks to an unusual software package that mixes an inference engine with a natural-language front end and a knowledge-base processor. Working with either a 68000-based or a VAX-class computer that runs under Unix, the Knowledge Workbench, developed by Silogic Inc. (Los Angeles), uses a proprietary Prolog compiler as the inference engine. The natural-language program at the front end converts user-and-system dialogue into English-like input or internal Prolog representations. For its part, the knowledge-base processor works with a relational data base, gives special treatment to data and instructions, converts and stores chunks of knowledge, and acts as a link to other data bases.

Scaled-down bipolar process yields fastest FPLAs

Fuse-programmable logic arrays (FPLAs) with propagation delays down to 10 ns have been fabricated using a scaled-down bipolar process with 2-μm feature sizes and a 7-μm metal pitch. Industry-standard parts, in contrast, exhibit 25-ns delays. The process, called IMPACT by its developers at Texas Instruments Inc. (Dallas), uses a finer geometry than the company's advanced low-power Schottky (ALS) TTL technolgy and employs dry etching and ion implantation. Unlike the original version of IMPACT announced earlier this year, the latest variation will make use of direct wafer-stepping techniques. The first parts to be ready include a pair of 24-pin FPLAs with 32 AND terms and 6 OR terms. Four PAL (programmable array logic) devices that share the low propagation delays will also be made.

Plastic resin to challenge aluminum as disk substrate

A plastic resin may soon give aluminum a run for its money as the preferred substrate for 5¼-in. Winchester disks. The 130-mm-diameter substrate, from Data Packaging Corp. (Cambridge, Mass.), is smoother and cleaner than its typical aluminum counterpart. The polyetherimide resin, dubbed Ultem, consistently demonstrates surface variations of less then 0.7 μin. ANSI specifications, in contrast, allow for surface irregularities of up to 1 μin.

Although the plastic disks can be treated and coated with magnetic materials in the same way as their aluminum equivalents, they are less than 50% as expensive. They also weigh less, thus putting a smaller strain on a Winchester disk drive's spindle and in turn encouraging the use of smaller motors. The only drawback of the plastic substrate is its rate of thermal expansion, which—at 56 µm/°C—is 2.5 times that of aluminum and may cause tracking problems in disk drives with open-loop servos. The resin, however, will not begin to distort until heated to 200°C. The internal operating temperature of most disk drives is well below 140°C.

DAC hybrids build on digital gate-array structures

Digital gate-array and analog technologies team up in a series of novel hybrid packages that combine a 16-bit digital-to-analog converter with a microprocessor interface, reference circuitry, and an operational amplifier. With all that circuitry squeezed into one package, the hybrids save a square inch of circuit board space compared with other d-a converters. Burr-Brown Corp. (Tucson, Ariz.) designed the microprocessor interface on the voltage-output units in a straightforward manner: the 24-pin DAC709 accepts 16 bits in two bytes (ELECTRONIC DESIGN, March 8, p. 141), and the 28-pin DAC707 accepts all 16 bits at once, or "broadside." The sister converters, which have current outputs, need an external op amp. The DAC708, in a 24-pin housing, accepts two bytes; the DAC708, in 28-pin package, all 16 bits. All four units latch the inputs into double buffers. In addition, they all have an integral nonlinearity of ±0.003%, a maximum differential nonlinearity of ±0.006% of full scale, and a guaranteed monotonicity of 14 bits over temperature.

Multicolor thermal printing process relies on chemical dyes

Chemical reaction is the key behind a thermal-transfer printing process that can put down a rainbow of colors with only one reusable transfer ribbon. The polyester ribbon, coated with alternating layers of temperature-dependent dyes, chemically reacts to the developer on the receiving paper when the thermally controlled print head passes over it. Unlike wax-coated thermal ribbon cartridges, which can be used only once, the ribbon can be rewound as many as 15 times—with no appreciable loss in color quality. The process, developed by Ricoh Co. Ltd. (Tokyo) and soon to be part of an OEM-targeted printer from Ricoh Corp. (West Caldwell, N.J.), yields excellent dot clarity for half-tone images and graphics.

Second 825-Mbyte Winchester drive makes the scene

A 14-in. Winchester disk drive that stores up to 825 Mbytes matches the record for the largest amount of memory that can be held on a single spindle. Developed by Ampex Corp. (Redwood City, Calif.), the drive employs six platters with an enlarged recording surface, densities of 960 tpi and 12,500 bpi, and 2,7 run-length–limited encoding to achieve high capacity. The unit uses a standard SMD interface as its link to the outside world, and data is transferred at 1.859 Mbytes/s. The only other commercial Winchester drive with comparable capacity is Control Data Corp.'s XMD. (Although the IBM 3380 stores well over 1 G-byte using a thin-film recording medium and heads and multiple spindles—it is plug-compatible only with IBM mainframes.)

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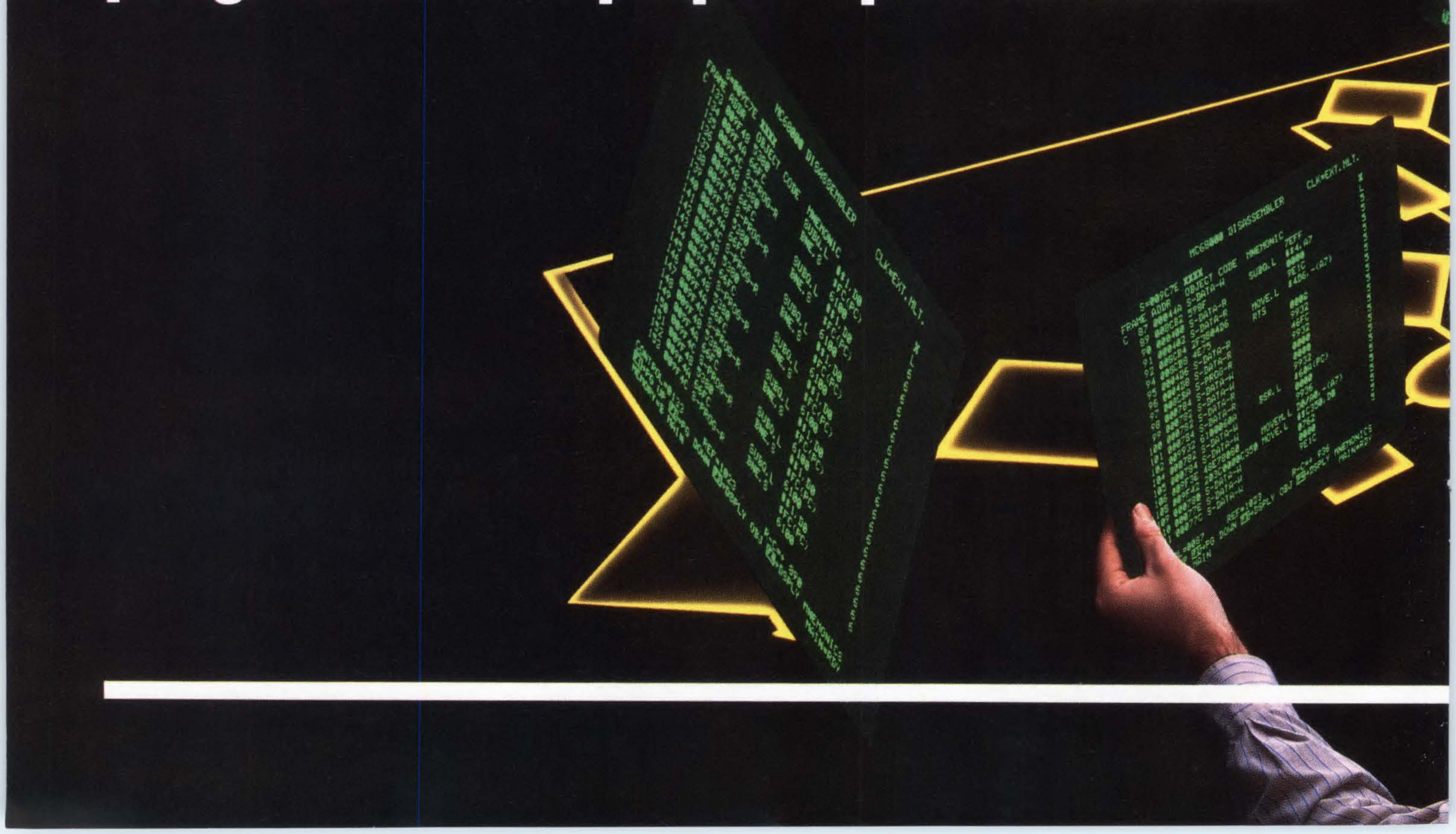

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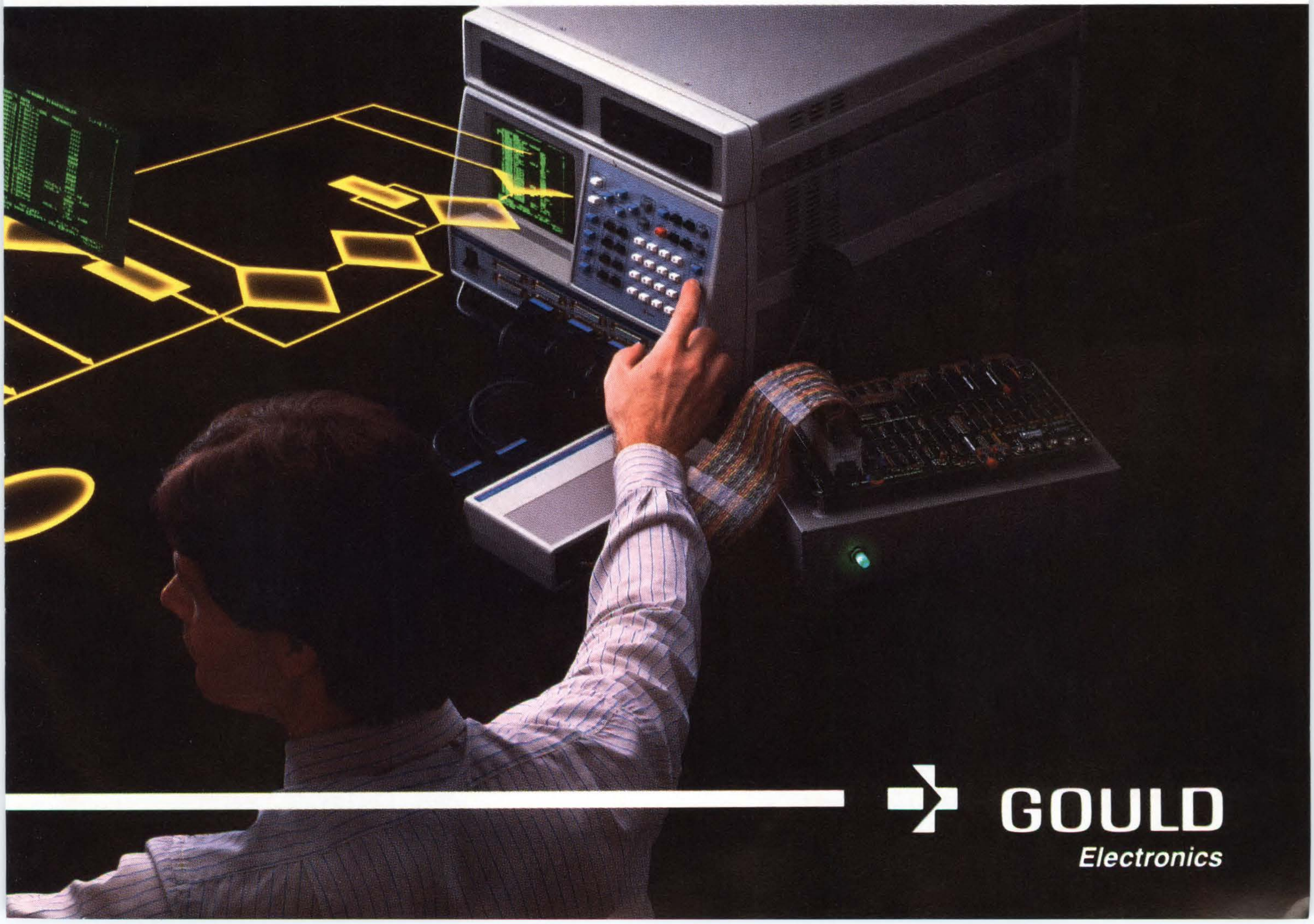
The K105-D gives you two levels of HELP at the touch of a button. First, step-by-step operating instructions that ap.)ear along the bottom of the analyzer screen. Second, a menu that allows you to select more detailed "help" should you need it.

 CIRCLE 20



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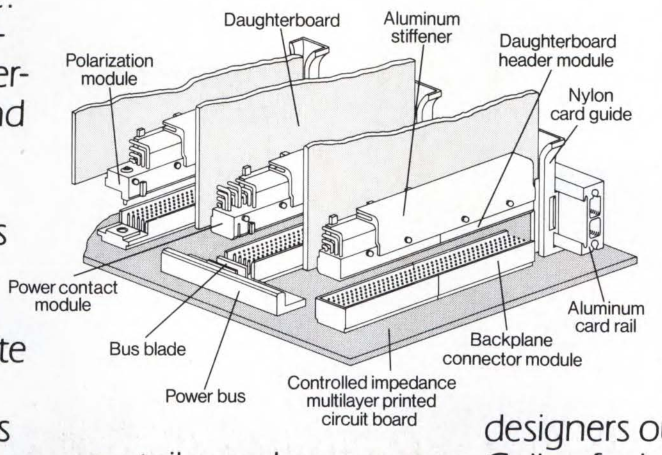

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CIRCLE 21

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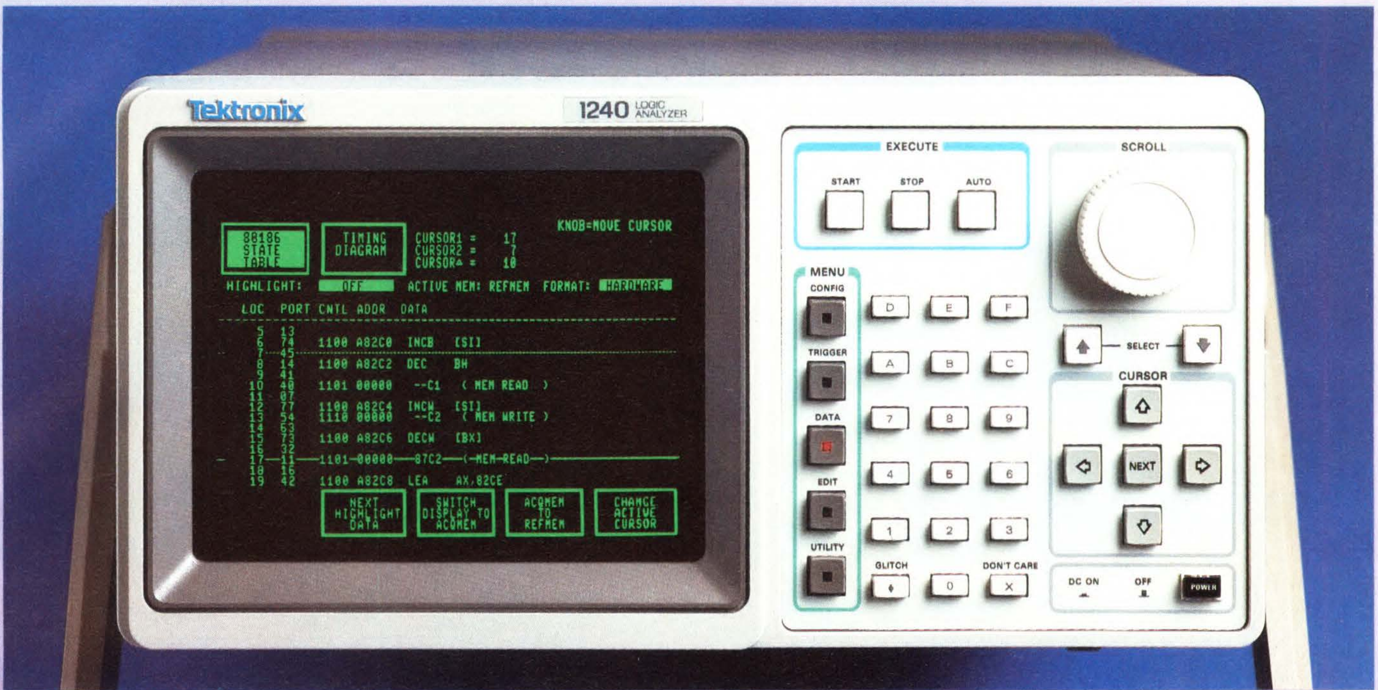

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CIRCLE 24

NEWSFRONT

50-head disk drive promises to speed access by a factor of 10

Multiplying the number of heads by five in a 14-in. Winchester drive may lead to a tenfold decrease in a unit's response time.

Arranging up to 50 read/write heads in a Winchester disk drive should make it possible to slash by nearly 90% the average access time to randomly sought data. The approach, now being tested on a series of 14-in. Winchester disk drives, will likely keep the unit's average access time to about 20 ms—even under heavy request loads. A typical SMD drive, with its complement of 10 heads, takes, on average, 150 to 180 ms to access data under the same conditions.

Alpha Data Inc. (Chatsworth, Calif.) believes that the 20- to 30-ms average access time quoted for typical SMD Winchester drives is misleading, because it does not hold up under heavy loads. Rather, the company points out that the performance of single- or double-armature SMD drives seriously degrades as the frequency of data searches requested by the host increases much beyond 18 or 20 a second.

Such a load, though, is not unusual for the large storage modules employed in database systems. Under that sort of pressure, the response time of an SMD unit can climb to 150 ms and beyond.

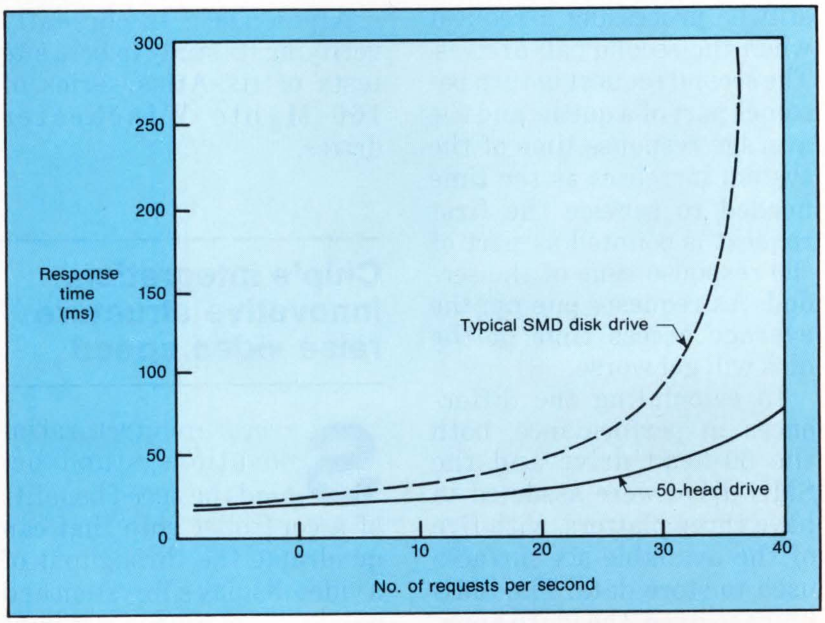
The problem is directly related to the probability that the read head will have to scout the disk to find the desired information. The higher the possibility that the head will not have to move, the faster a data transfer will take place.

Stephan Ohr

Lower response time

In an SMD drive, each read/write head must typically travel across at least half of the disk's surface to find the requested data. Increasing the number of heads, however, reduces the response time of the entire system, since the probability that the read heads must travel is greatly reduced.

Under light request loads, a typical SMD drive and a 50-head unit will exhibit about the same performance



When lightly loaded (servicing about 18 requests a second), both a 50-head drive and a typical SMD drive perform similarly. As the number of requests made each second rises, the reponse time of the 50-head unit shows a slight increase. In comparison, the respose time for the SMD drive climbs dramatically.

because the likelihood that a request will demand some movement of the head is about the same, since such requests are often for contiguous tracks. When lightly loaded, therefore both machines can typically complete a single random search within 20 ms.

Carrying the burden

Under heavier loading, though, the chance that a head must move rises for the typical SMD unit, in turn increasing its average access time. The 50-head drive, in comparison, needs no more time to complete a search (see the figure).

A second problem that must be taken into consideration is that of request queuing. Under heavy loads, it is likely that one of the SMD unit's read/write head will still be processing a request when the second call arrives. The second request in turn becomes part of a queue, and the average response time of the system increases as the time needed to service the first request is counted as part of the response time of the second. As requests pile up, the average access time of the disk will get worse.

In calculating the differences in performance, both the 50-head drive and the SMD drive were assumed to have three platters, with five of the available six surfaces used to store data. The SMD unit assigned 2 heads to a surface; the other unit, 10.

In the calculations, the probability of head movement was fixed at 0.4 to show the likely effect of an increase in the number of requests made every second on the average access time. That is, there is a 40% chance that as each data access arrives it will require some degree of head movement—a reasonable number to simulate actual conditions.

As mentioned, as long as the drives remain lightly loaded (handling about 18 requests every second), their performance is similar. However, once that threshold is crossed, the queue for the typical SMD drive will begin to slow down its response time. Further, at a rate of 40 requests a second, the SMD drive will "saturate," completing only 1 out of every 10 requests. The 50-head drive, meanwhile, shows a typical response time of 40 ms under the same load.

Alpha Data is currently verifying its study in beta site tests of its Atlas series of 160-Mybte Winchester drives.

Chip's integration, innovative structure raise video speed

Several architectural innovations stand behind the speed benefits of a controller chip that can quadruple the throughput of a video display subsystem and possibly even increase it hundredfold.

For the first time, all the critical circuitry and techniques that govern a video display and memory have been integrated on one chip, including a dynamic RAM controller, microprocessor arbitration logic, an unusual implementation of X-Y address registers, and multiple address strobes.

Unloading the host

The video system controller, designed by Texas Instrument Inc. (Dallas) for microprocessor-based systems assumes two responsibilities normally assigned to the host, namely, dynamic refreshing and supervision of display accesses. With the NMOS chip alone handling those tasks, the host processor can use virtually the entire memory bandwidth for updating the display with new data. Conventional systems, which rely heavily on the host for refreshing and accesses, consume about half the bandwidth for those purposes, leaving only half for updating.

The memory cycle generator works hand in hand with the arbitration logic to determine when the host processor, the display logic, or the refresh logic can access the memory (see the figure).

Indirect accesses

The controller's X-Y addresses registers give the host rapid access to data at contiguous pixel locations. The main system addresses a pixel word indirectly through a 20-bit register value that points to a location within video memory.

The speed advantage arises in the method of updating

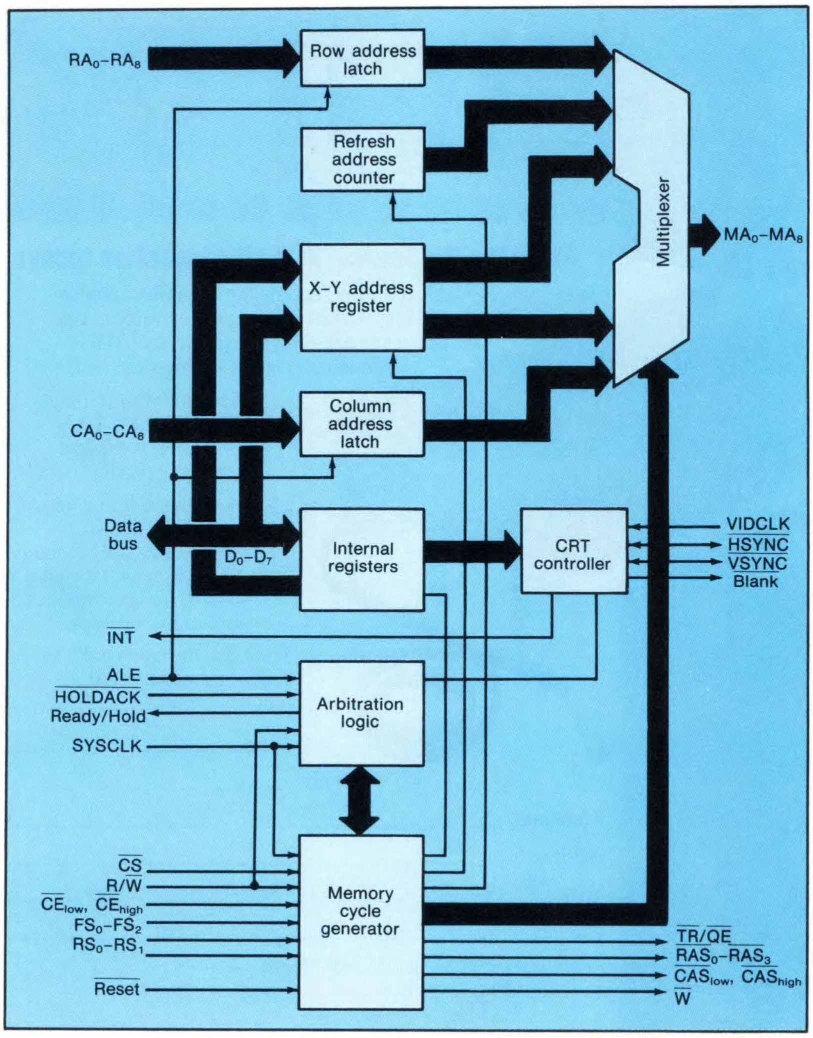
the X-Y registers—through hardware circuitry that automatically increments, decrements, or clears the pointer register. Conventional systems depend on software: The host must fetch and execute separate instructions to reach an address, to display the data in that address, to increment the address, and then to call up the successive data.

Based on a typical access time of 400 ns, the controller can fill a 1024-by-1024-pixel screen with up to 16 colors in less than half a second. The software approach would take close to 2 seconds.

Beyond range

Indirect X-Y addressing present another advantage in terms of range. Since pixels are selected through the contents of the 20-bit address pointer instead of through the row and column address strobes, the chip can address 1 million words; the range of the host alone might have been considerably more limited.

The chip's architecture also include four row address strobes that can be independently programmed. Assuming that the video memory is wired to accept those inputs, the controller can write to four different planes simultaneously with a preselected color.



The single-chip video system controller from Texas Instruments incorporates all the logic and timing required to refresh dynamic RAM, access the display memory, synchronize itself to the CRTs, and arbitrate contention for the display. A host addresses contiguous pixels through the chip's X-Y registers, which update the screen through hardware that increments, decrements, or clears the registers.

Getting the most out of it

The controller can control as many as 64 dynamic RAMs, each either 64 or 256 kbits. Though it easily enhances the performance of conventional chips, the speed, throughput, and addressing gains become even greater when the controller is paired with a multiport dynamic RAM like the TMS4161.

In that type of system, the chip automatically handles requests for transferring data between the 256-bit shift register and the main video memory. In addition, a multiport structure enables the processor to access the video memory while the screen is being refreshed, thereby relieving the bottleneck associated with single-port memory.

Easy interfacing

The video system controller is designed with an open architecture, making it compatible with a variety of popular 8-, 16-, and 32-bit

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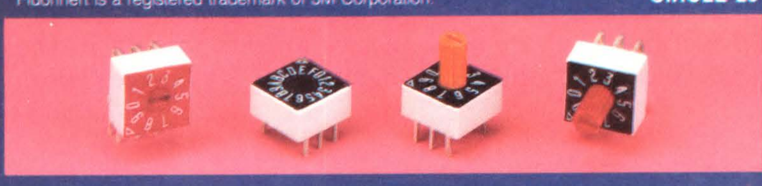
CIRCLE 26



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microprocessors.

Since the controller also accepts separate video and system clock signals, the display subsystem and the host processor can run asynchronously. In additional, both the vertical and horizontal sync inputs can match the controller timing to an external video timing source, thereby allowing the controller chip to mix its own image data with other video signals.

Heather Bryce

Now Smalltalk runs on small-instruction-set computer

For the first time, a functional programming language has been put to work on a reduced-instruction-set microcomputer. By modifying its Soar machine, researchers at the Computer Science Department of the University of California at Berkeley have been successful in running Smalltalk, a functional programming language developed by the Learning Research Group of Xerox Corp. (Palo Alto, Calif.).

According to benchmarks established by simple routines, the language runs between 41% and 580% faster on the Berkeley machine than on a high-speed, ECL-based minicomputer.

(Functional programming languages use objects that send messages to each other saying what operation is to be performed, but not how to perform it. Hence they differ radically from conventional languages and do not run efficiently on standard computers.)

Like most reduced-instruction-set machines, Soar has no microcoded instructions, few multicycle instructions, and no elaborate addressing hardware. It has, however, been extended with a few hardware additions to make it possible to handle Smalltalk.

In the first place, tagged data-type checking, a basic feature of object-oriented languages, has been added. The basis for the type checking is a single-bit tag in each word that indicates whether it contains an integer or a pointer to a data structure with type-specified information.

Tag, you're it

Because the tagging scheme does not depend on microcode, it relies on software that manipulates and inspects the tags. Further, each instruction contains a bit that either enables or disables the tag-checking process.

The untagged mode turns off all tag checks, and the system then operates on 32-bit data. When it works that way, the tag bits become data bits and the normal reduced-instruction-set programs (written in conventional high-level languages like C or Pascal) can be used.

Also, two so-called shadow registers have been located on the data buses near the ALU to trap operands that are not integers. That accomplished, integer comparisons are made with a traditional compare-and-skip algorithm.

Overcoming a hurdle

Using a reduced instruction set attacks one problem inherent in all functional languages—the enormous storage demands produced when data is not separated from the operations that work on it. The basic difficulty, picturesquely described by the Berkeley researchers as the "tenure" problem, is how to rid the system of the deadwood that accumulates in virtual memory.

The university's approach employs a "generation scavenging" algorithm that copies and updates the system's pointer path. In other systems, a reference counter reclaims storage space by indicating when an object is no longer being referenced. Most object-oriented languages use an object address table, with each word containing an index to the table and the table entry containing the address of each object and its reference count.

Instead of reference counts, the Berkeley system essentially copies and updates the system's pointer path and only updates a table when a pointer to a new object is stored in a memory location without an old object. Each pointer is tagged with the generation—old or new—of the object it points to. In that way, objects can be purged on a regular basis so that only active objects remain in the memory.

Carole Patton

Laser closes link on processed and passivated ICs

In a new twist on an established technique, a laser is closing the links on fully fabricated and passivated ICs. The approach is a logical extension of an idea that has already proven viable—employing a laser to form a connection to substitute redundant circuits.

An experimental link structure that can be incorporated into conventional IC processes uses laser-annealed polysilicon to form low-resistance connections on completed ICs. Jointly developed by researchers at Electro-Scientific Inc. (Portland, Ore.) and from the Department of Electrical Engineering at Texas A&M University (College Station, Texas), the technique promises to make possible new types of programmable logic structures. Further, it should also enhance the approach currently taken to hardware redundancy in high-density memory and logic devices.

Subjects of interest

In their work, the researchers had two main concerns: The first was sufficiently lowering the resistance of a polysilicon link to produce an effective "short." The second was supplying enough power to melt and anneal the silicon without risking explosive evaporation, which could damage adjoining circuit elements, as well as the passivation layer. (Laser links are typically blown after passivation, exposing the substrate, which must then go through a second annealing stage to reflow the passivation.)

The experimental link consists of a single layer of polysilicon deposited without doping on a layer of thermally oxidized silicon in a conventional atmospheric-pressure chemical vapor deposition reactor. The link's pattern is then plasma-etched, and a photoresist is allowed to remain above the region that will form the link. The rest of the structure is then implanted to lower its resistance.

The link's resistance, when measured using a four-point probe on its test pads, is in the range of 10^8 to $5 \times 10^9\ \Omega$—depending on the structure. When the link is annealed by scanning it with a Q-switched, frequency-doubled neodymium and yttrium-aluminum-garnet (0.53-μm) green laser with a repetition frequency of 5 kHz, a pulse width of 65 ns, and a spot size of about 10 μm, its resistance drops to between 50 and 500 Ω.

The experiment showed that fabricating the links is fully compatible with conventional processing techniques and that the link's dimensions can be held to 2 μm or smaller. Also, the tests demonstrated that the links could be closed with a single pulse from a green laser, making the operation as simple and as swift as blowing a laser fuse.

Warren Andrews

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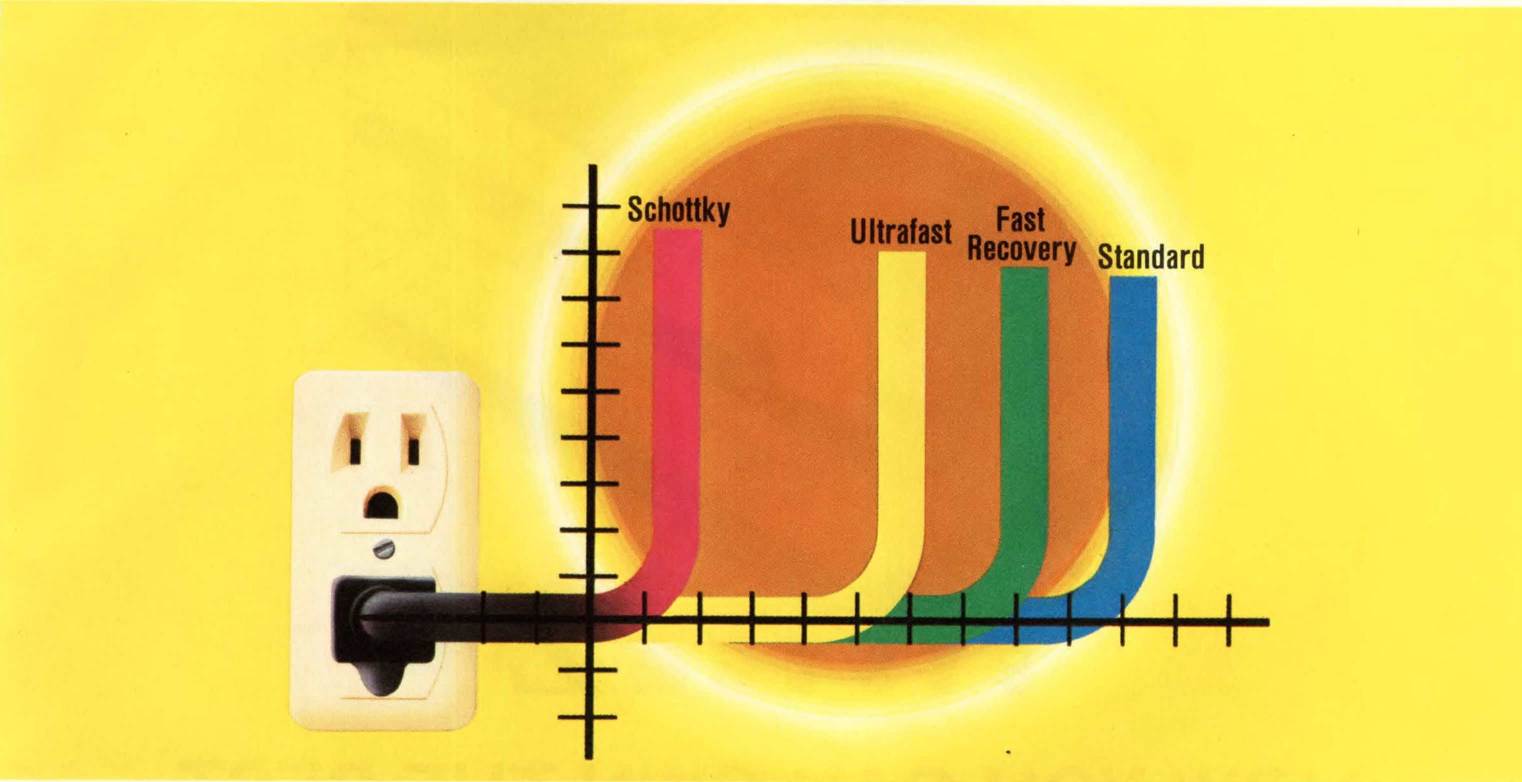

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6A T0-220		■		
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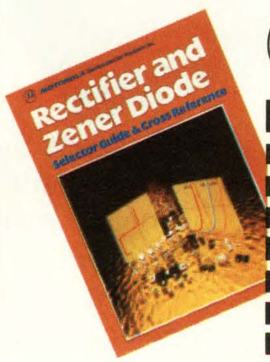
7.5A T0-220	●			
8A T0-220		●		
10A T0-220	●			
15A T0-220	■	●		
16A T0-220	●	■		
20A T0-220	■			
25A Button			●	●
30A T0-3	■			
30A T0-220	■			
30A T0-218	■	■		
30A to 50A Pressfit				●
100-300A Powertaps	■	■		

■ = Dual Diode



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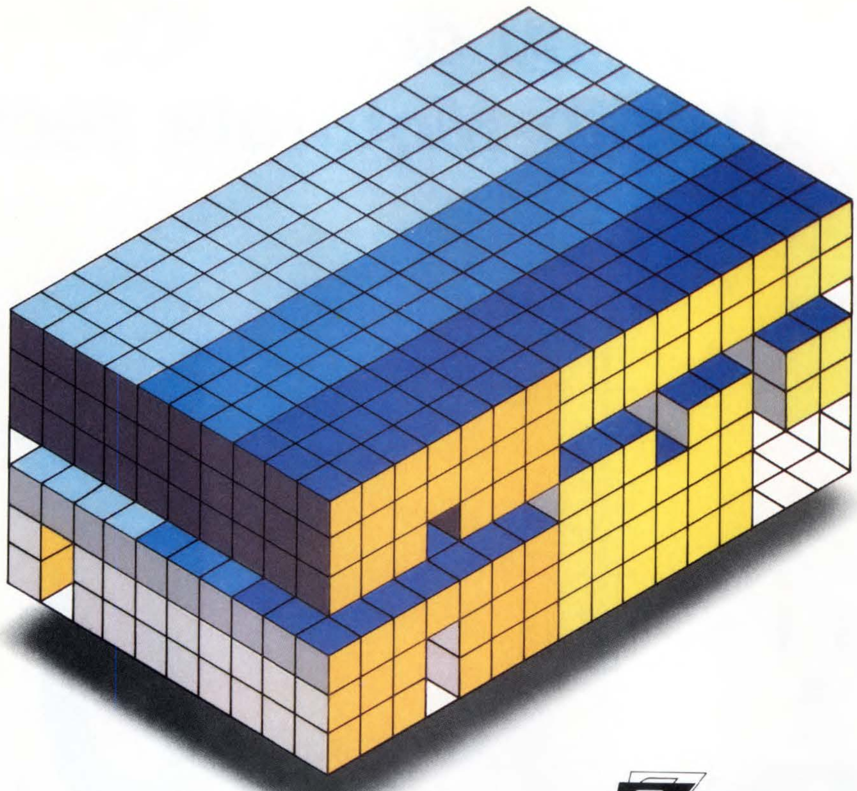

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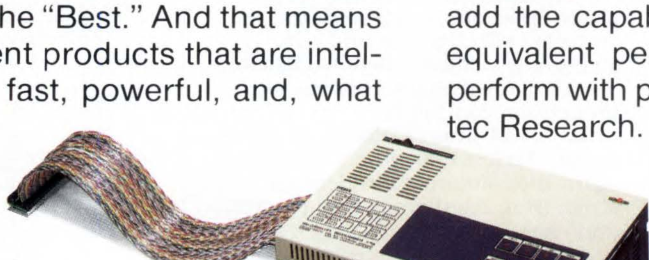

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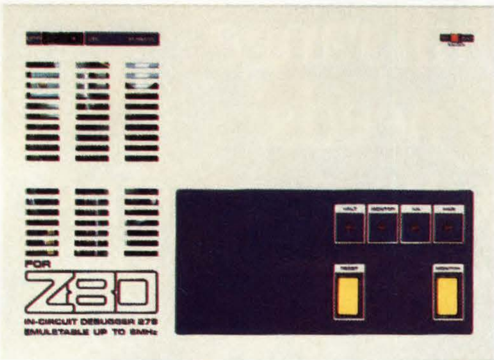
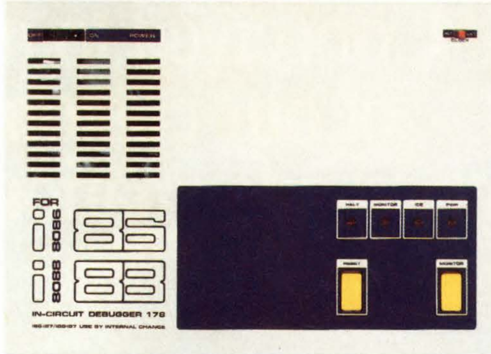


Z80

Z80
Z80B
Z80H

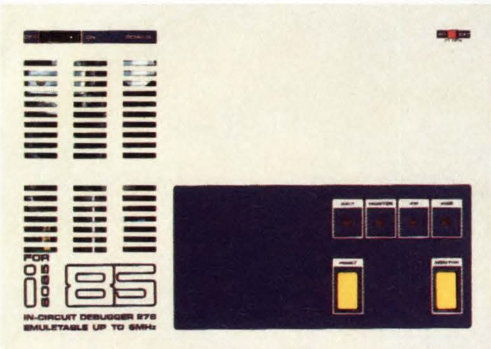
Emulates Z80B microprocessors to 6 MHz and Z80H to 8 MHz. Features; 64K byte user emulation memory, 2K deep x 32 bits wide realtime trace buffer, 29 different debugger commands.



i8086/88

i8086
i8087
i8088

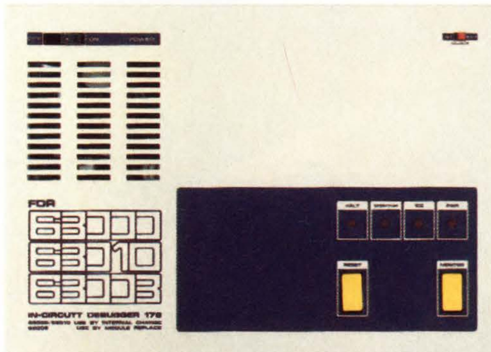
Co-emulation of 8086 and 8087 or 8088 and 8087 processors to 5 MHz. Realtime emulation to 8 MHz for 8086/88 processors. Features; 128K bytes static RAM - expandable to 1 Mbyte, 4K deep x 40 bits deep realtime trace buffer, 30 different debugger commands.



i8085

i8085A
i8085A-1
i8085A-2

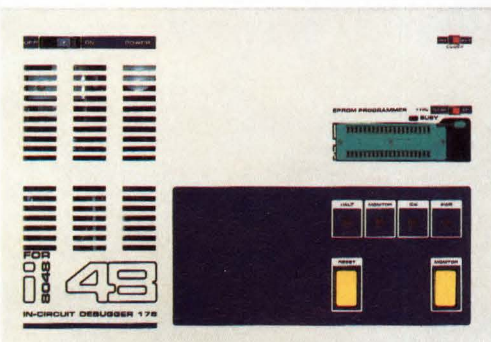
Emulates 8085 processors up to 6 MHz. Features; 64K byte user emulation memory, 2K deep x 32 bits wide realtime trace buffer, 29 different debugger commands.



68000

68000
68010
68008

Emulates 68000, 68008 and 68010 in one unit to 10 MHz. Features; 128K of emulation memory - expandable to 256K, 4K deep x 48 bits wide realtime trace buffer, 30 different debugger commands.



i8048

i8048
i8049
i8050
i8748
i8749
i8039
i8035
i8040

Emulates entire 8048 family in one unit to 11 MHz. Features; 4K emulation memory, 2K deep x 32 bits wide realtime trace buffer, 29 different debugger commands. 8748 and 8749 units feature a built-in EPROM programmer.

All emulators come equipped with these standard features; 3 hardware and 8 software breakpoints, an Event Trigger and External Probe triggered breakpoint, 14 selectable baud rates to 19200bps, 20″ processor probe, 115/230 VAC operation. All Zax emulators are compact, lightweight, rugged and can easily fit into a briefcase.

CIRCLE 30

SYSTEM Z-from Z...ing

ZAX

Zax Corporation 2572 White Road, Irvine, California 92714
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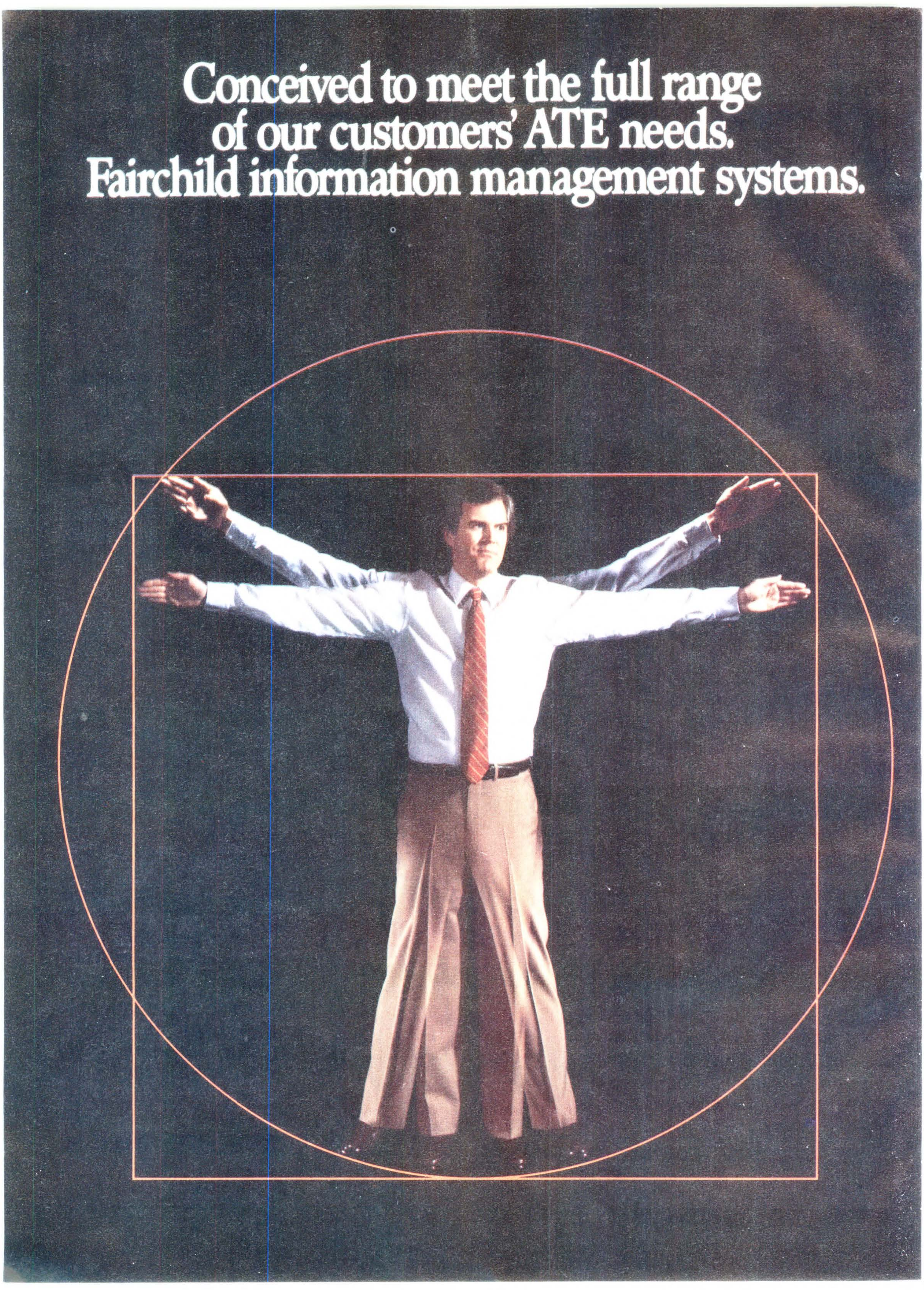
Conceived to meet the full range
of our customers' ATE needs.
Fairchild information management systems.

We could have built just one kind of information management system like most other ATE companies. But when we talked to our customers, we found out information management means different things to different people. And no one system could satisfy everybody.

So we created different systems to meet all our customers' needs–from repair management to report generation.

For starters, if what you want is repair management, you can get our Test Area Controller–and not pay for capabilities you really don't want. The Controller links testers with repair stations, eliminating the need for "repair tickets." Which means repairs can be done without paper documentation. And much faster.

Our Test Area Supervisor combines three key management functions—repairs, process control, datalog analysis–in one centrally controlled system for Series 30 users. It boasts advanced features such as yield alarms and automatic defect reports for quick problem solving. What's more, special productivity reports let you fine-tune your entire testing operation as you test.

To some people, information management includes entire factories. And for them we've made the high performance Test Area Manager. With it, you can connect most of the test equipment you use–even machines made by different manufacturers. We've teamed Ethernet™ with a state-of-the-art relational database management system to give you maximum flexibility and total control of the testing process. You can define your own reports, generate programs and pinpoint the cause of every problem.

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For more information, contact Fairchild Manufacturing Test Systems, 299 Old Niskayuna Road, Latham, NY 12110, 518-783-3600.

FAIRCHILD
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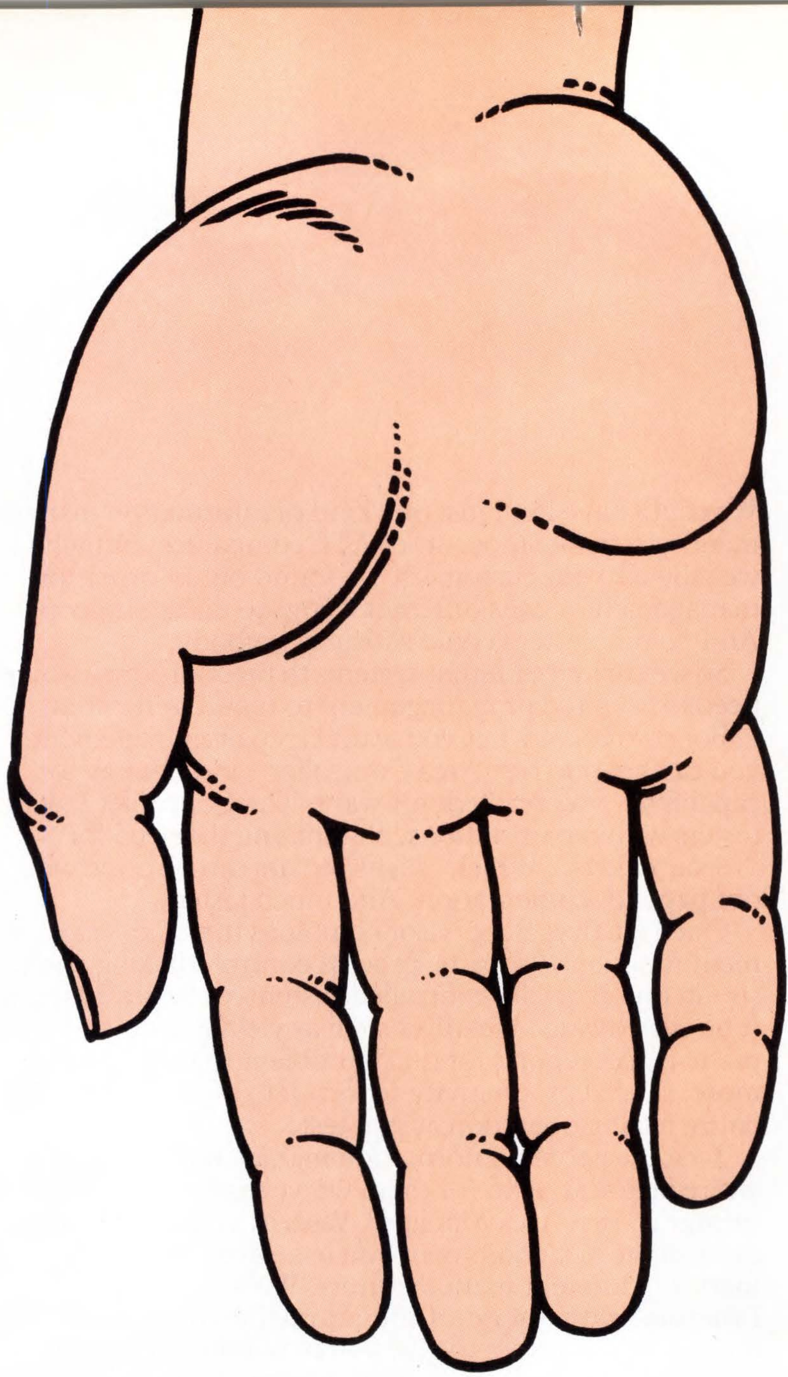


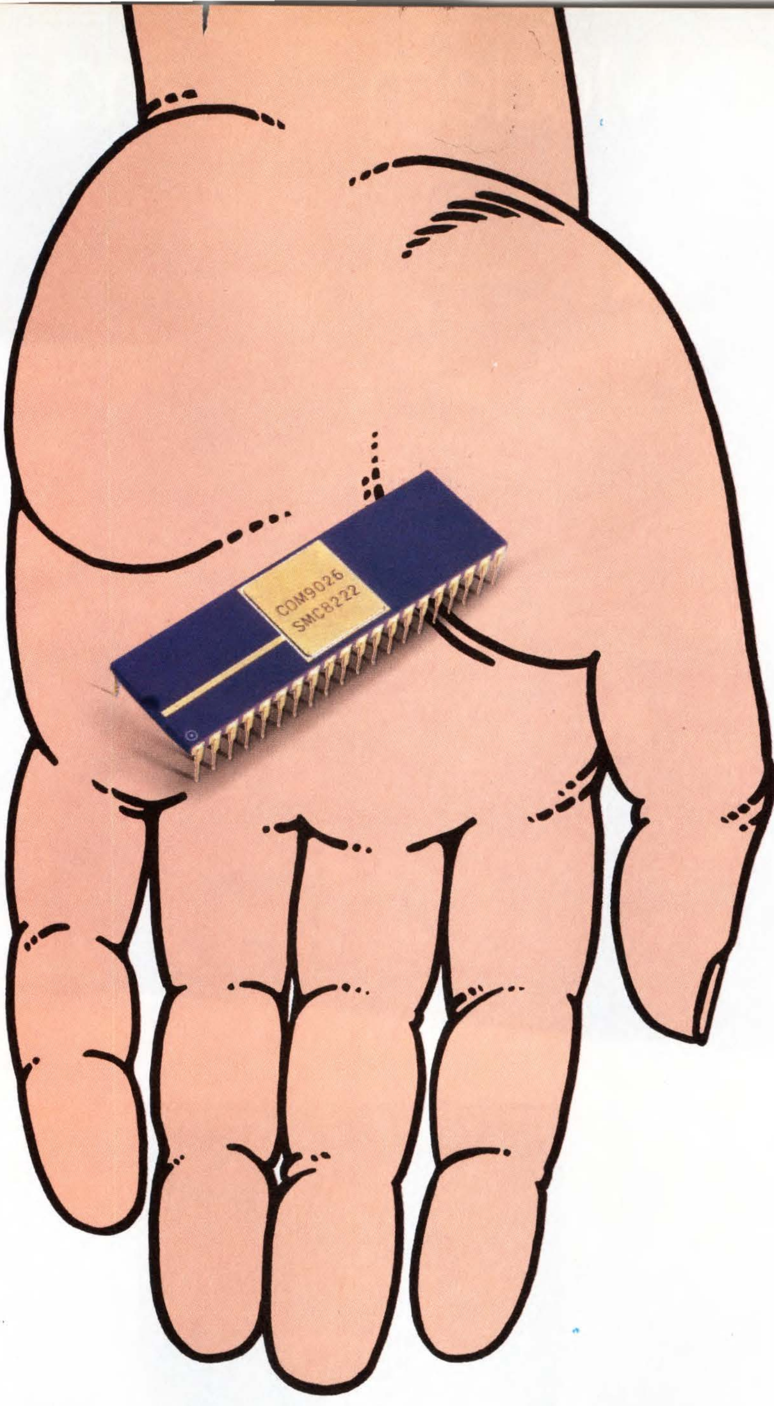
On one hand, you could wait years for a proven single-chip token-passing LAN controller.

There are four very good reasons why your search for a single-chip local area network controller should begin and end with Standard Microsystems' COM 9026.

First, the COM 9026 is the only token-passing LAN controller in the world being produced in volume and available for immediate delivery. That means you can give your system the best networking capability available— when you need it the most. Today.

Secondly, the COM 9026 is proven. Since its introduction as the world's first commercially available single-chip LAN controller in 1982, the COM 9026 has been used successfully in numerous applications. It's a complete protocol handler for ARCNET® and similar token-passing systems currently used by Datapoint, Nestar, Tandy, 3M, Zenith and others.

Thirdly, Standard Microsystems supports the COM 9026 with a complete line of system-level products available off the shelf. We have everything you need to implement your system, from state-of-the-art hardware to field-proven software. Our board products are also remark-



On the other, you can get one from Standard Microsystems today.

ably cost-effective because they incorporate our VLSI local area network chip set.

Last, but certainly not least, the COM 9026 has all the advanced capabilities you want in an LAN controller.

It replaces over 100 SSI/MSI circuits with one chip, supports data rates up to 2.5M Baud and avoids the fluctuating channel access times caused by data collisions in CSMA (Carrier-Sense Multiple-Access) schemes.

So don't go empty-handed waiting for a LAN controller you can get your hands on today. The COM 9026 is a high-density, n-channel silicon gate MOS circuit fabricated with SMC's COPLAMOS® technology. It's available for immediate delivery in a 40-pin ceramic or cerdip dual in-line package.

For more information, contact Standard Microsystems Corporation, 35 Marcus Boulevard, Hauppauge, NY 11788. (516) 273-3100.

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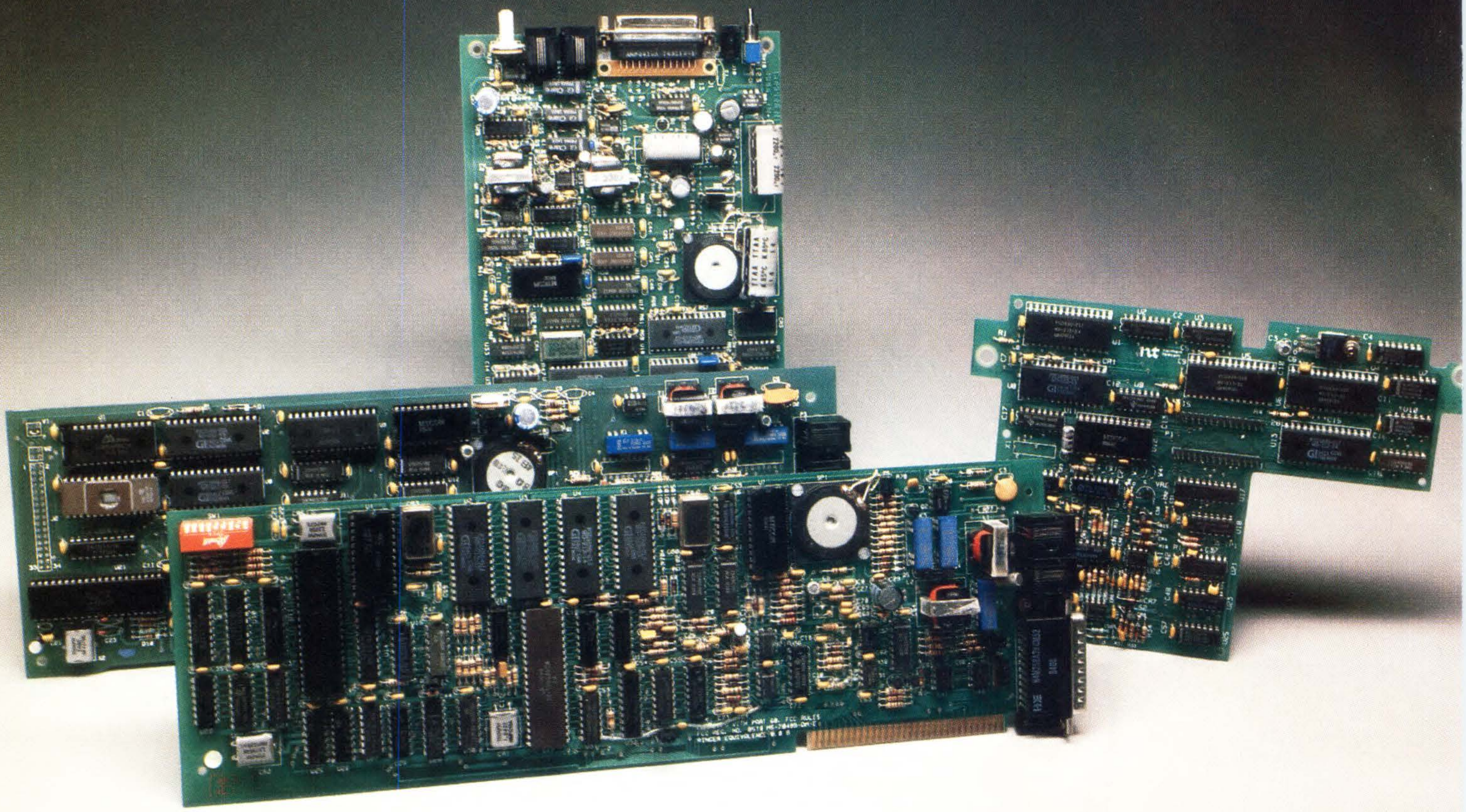
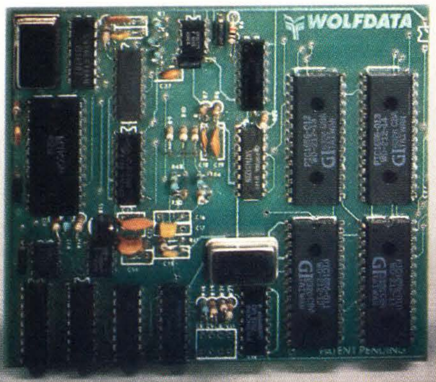
CIRCLE 32

STANDARD MICROSYSTEMS CORPORATION

MVS-212™ Modem . . . and Beyond





MODEM

- Bell 212A and Bell 103 compatible
- CCITT V.22
- Synchronous/Asynchronous
- Auto Dial

. . . AND BEYOND

- Voice Compression
- Protocol Conversion (X.25, SNA/SDLC, etc.)
- Network specific remote diagnostics
- V.22 BIS

Introducing Wolfdata's New Modem/Voice System (MVS) For OEM's

In its basic configuration, the MVS is a 1200 and 300 bps full-duplex modem that is compatible with botn Bell 212A and CCITT V.22 standards. **BEYOND** its basic modem functions, the MVS-212 contains proprietary voice compression algorithms that compress speech at user selectable rates between 4.8 Kbps and 16 Kbps. The MVS's DTMF recognition allows remote telephone access via commands from the DTMF pad on the phone and also allows the user to switch between voice and modem modes via user-initiated commands.

In addition to its standard modem and voice features the MVS-212 can be programmed to meet specific OEM protocol requirements, such as CCITT X.25 (HDLC) and SNA/SDLC.

Since the microcode is exercised in parallel with the MVS's communications algorithms, protocol conversion occurs transparent to the user.

For further information on custom OEM applications contact Wolfdata Inc. at (617) 250-1500

CIRCLE 33

WOLFDATA

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Chelmsford, MA 01824
617-250-1500

CONFERENCE PREVIEW

For 3-dimensional images, time is of the essence at Siggraph '84

Transforming high-quality graphics quickly and efficiently tops the bill at this year's conference. Standards are also an issue.

Attendees at this week's Siggraph '84 will find that one of the main concerns is techniques that enable high-resolution three-dimensional images to be rapidly altered. Also of importance at the gathering, being held in Minneapolis, July 23-27, will be methods to help programmers prepare such images with a minimum amount of effort.

Also, the conference will afford a chance to examine existing graphics standards and ways in which they might be modified and enhanced. Interestingly, although the focus of much of the meeting will be on CAD/CAM graphics, there is an increasing amount of attention being paid to animation and other movie-making techniques.

Hidden lines

One of the most time-consuming aspects of modeling 3D solids is erasing the lines and polygons that fall behind portions of an object as it is moved or rotated on the screen.

Terry Costlow

One way to speed such hidden-line removal employs a technique called invisibility coherence. The approach, from General Electric Co.'s corporate research and development group (Schenectady, N.Y.), trims the amount of time it takes for a standard scanning-line algorithm to eliminate hidden lines and shade an image.

Now you see it ...

Invisibility coherence uses information supplied by the imaging data to determine what lines will be hidden by noting those sections of an object that will block other portions. That information, known as depth data , is processed before the horizontal and vertical data. Once what will be hidden, or invisible, is determined, its associated data no longer has to be handled, in turn eliminating the time normally required to process it.

With a simple object like a sphere, which has few hidden lines, processing speed is unchanged or improved only slightly. The main benefit of the technique is realized when complex images are created.

Building on

In such cases, the improvement in throughput can run to nearly 50%. For instance, it takes 103.5 seconds to draw an image with the approach; 203.5 seconds, without it. Further, invisibility coherence can be added to most hidden-line-removal algorithms, boosting their throughput at the cost of only a negligible fraction of their computational power.

Another approach to creating and altering images works with Steiner patches—free-form shapes that supply true representations of curves —instead of individual lines. Such a display is complete with the curves and the various shadings normally perceived by the eye.

From the viewer's eye

Brigham Young University's Department of Civil Engineering (Provo, Utah) and Purdue University's School of Mechanical Engineering (West Lafayette, Ind.) have jointly devised a tracing algorithm, which works with Steiner patches, that computes a line from the viewer's eye to the object on the screen, thus helping draw a truer representation.

In addition to speeding the generation of images (when compared with approaches that build pictures using individual lines), the algorithm computes a new line when the object is rotated, in turn, boosting throughput. The new line furnishes the necessary input to shade and otherwise adjust the relationship between the patches that comprise the object's surface.

Time on your side

In addition to cutting down on processing time, many researchers are interested in saving programming time as well. The chief route to that goal is portable software, which can be written once and then used without alteration on different hardware.

One such program—for opening windows—runs on any display that can draw and erase vectors. The package, from Battelle Northwest Laboratories (Richland, Wash.) puts special emphasis on graphics processing within each window and is designed for any operating system that can run a number of applications packages simultaneously.

Routines for opening, closing, and moving windows are supplied, and provisions have been made for temporarily removing a window from the screen and then calling it back up with all its data intact. The package also maintains a display list for every window and updates the screen as the windows change.

In and out the window

The company notes that employing some of the features common to most terminals, as well as adding some customization for specific machines, will greatly increase the package's throughput with a minimal impact on portability. Even without such improvements, though, the windows can manipulate displays containing thousands of vectors at a speed of about one-third that of a windowless system.

Of course, the most direct way to ensure portable graphics software is through establishing standards. The Space Telescope Science Institute (Baltimore), for one, will look at some adaptations of the Graphical Kernel System (GKS), one of the most popular graphics standards. The institute is investigating techniques that let users add GKS to existing software without the burden of having to write new code.

Simpler conversion

Usually, converting a graphics package to GKS requires writing a layer of code that translates the package's commands into GKS commands. However, programs that are tightly coupled with specific hardware pose more of a problem, since the sections that make use of unique aspects of a device can be difficult to convert into the more generic GKS commands. In most such situations, a general rewriting of the code minimizes the reliance on the hardware and will permit the program to be used with a range of machines.

Researchers at the institute also will explore a technique that eliminates the time-consuming task of writing device drivers for different hardware configurations.

In much the same vein the National Center for Atmospheric Research (Washington, D.C.) is currently working on a GKS system that permits users to configure GKS software to a specific graphics terminal much faster than if they wrote a device driver—a task that requires extensive knowledge of the hardware. Working with the software, engineers can simply describe a terminal's capabilities to the package and it will then perform the necessary alterations so that the program can be run.

Dynamic control

At the same time, some manufacturers are looking at other enhancements to GKS. One such consideration is an interface that allows an image on any type of display to be dynamically controlled. The brainchild of IBM Corp.'s Data Systems Division (Poughkeepsie, N.Y.), the enhancement makes it possible to rotate and change the color of an image—as well as handle other real-time commands—by using a variety of inputs. The approach allows users to simply specify the relationship between an input device and a display, rather than writing code to link the two. Currently, these inputs must be written for specific hardware configurations, since the GKS standard does not incorporate dynamic control. The technique, could also be added to ANSI's CORE standard.

Specify TRW Superfast Flat Cable Connectors

This is the flat cable mass termination interconnect system that's designed to relieve strain in every way.

The cover/strain relief is pre-assembled as an intergral part of the connector. So you're assured of effective cable strain relief without extra parts to buy or assemble. And one, simple, snap-action operation puts it in position.

TRW Superfast connectors are just as easy on your budget. Low prices to begin with. More density because of the lower profile of the overall package height. And the Superfast design requires less cable, less labor and reduces space requirements when used in a daisy chain mode. Superfast even meets MIL-SPEC requirements.

All this is part of the Value Engineering that TRW built into every Superfast Flat Cable Connector. It also includes features like an exclusive one-step insulation displacement contact system with a unique contact design for high reliability connections.

And you can get all the connector sizes and types you need in the Superfast system. More important, you can get fast, off-the-shelf delivery from the TRW Connector distributor network—the best in the business—to prevent strain on *your* commitments.

For more information on the Superfast Flat Cable Connector System, contact your TRW Electronic Components Group sales office, or see your local TRW Connector Distributor. Or write: Connector Division, TRW Electronic Components Group, 1501 Morse Avenue, Elk Grove Village, Illinois 60007. Phone 312.981.6000.

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Connector Division
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Plan your LinCMOS

High speed, exceptionally low power consumption, and multipurpose analog and/or digital inputs—new LinCMOS™ microprocessor-controlled data-acquisition systems from Texas Instruments deliver both! You can forget about traditional performance "tradeoffs."

You only have to remember TI. And two new LinCMOS families: The 28-pin TLC532A family with parallel output, and the 20-pin TLC540 family with serial output for interface to a variety of popular microprocessors.

One-chip data-acquisition system

Both families provide an entire data-acquisition system, from analog multiplexer to digital data bus, on one chip. You treat the IC as a simple plug-in component, replacing a board of parts.

Eliminating external components also reduces total system costs. And the chip itself is less costly than many metal-gate CMOS ICs having only an A-D converter function.

One potential application for the new LinCMOS peripherals is environmental control. An array of these A-D peripherals could sense room temperatures throughout a building and feed them to a microprocessor that instructs the heating/cooling system to direct air where it is needed.

Result: Energy bills could be slashed by a simpler, more cost-effective system.

◀ **Moving energy costs down** by moving air around—that's how TI's new LinCMOS A-D peripherals could work in a large building. These ICs could take multiple readings of each room's temperature for a microprocessor that quickly determines where warmer or cooler air is needed.

Photo taken at Plaza of the Americas, Dallas, Texas.

control system with TI's new microprocessor-controlled A-D ICs.

DATA-ACQUISITION EVOLUTION

	1979-83	1981-85	1983-1990s
Technology:			
Process:	Metal-gate CMOS	Metal-gate CMOS	Si-gate LinCMOS
Circuit:	Resistor ladder	Switched capacitor	Switched capacitor
Converter:			
Part types:	ADC0808, 0809N	TL520, 521, 522N	TLC532A, 533A
Size:	8,000 mil^2	1,700 mil^2	500 mil^2
Components:	256 resistors 511 switches	9 capacitors 26 switches	9 capacitors 26 switches
Features:			
Bar size:	29,000 mil^2	21,000 mil^2	15,000 mil^2
Speed:	10k samples/sec.	14k samples/sec.	67k samples/sec.
Error:	±0.75 LSB	±0.75 LSB	±0.5 LSB
Inputs:	8 analog	8 analog	11 analog*

*Includes six multipurpose inputs.

Major speed improvements, more inputs, smaller size—the evolution to LinCMOS products from metal-gate technology reflects big performance boosts and operational advantages, creating a bright linear future.

Up to 71,000 samples per second

Dramatic speeds are available—as fast as 71,000 samples per second. With power requirements as low as 6.0 mW.

This allows noise canceling and precise control of blower motors or heating elements. While virtually eliminating bulky power supplies.

Exceptional stability over a wide temperature range

Both the TLC532A family and the TLC540 family offer excellent temperature-range stability—total output error is within ±0.5 least significant bit (LSB) over a wide temperature range—from −40° to 85°C.

Military versions, also available, are stable within ±0.5 LSB over a −55° to 125°C temperature range.

Handle up to 11 inputs

Each LinCMOS A-D peripheral family allows a processor to monitor up to 11 analog signals. Six signals can be digital, if preferred, allowing keyboard or switch-position sensing.

These devices feature a built-in sample-and-hold circuit (software-controlled on the TLC540) that holds a "snapshot" of the input signals to reduce the effects of noise and random spikes.

Immediate availability

All of these LinCMOS A-D peripherals are TTL, MOS, and CMOS compatible. And all are available now. With performance that will change the way you look at linear.

Environmental control is only one possibility. These LinCMOS peripherals offer many opportunities in test equipment, automotive instrumentation, industrial controls, robotics, toys, home computers, signal processing, and other applications.

For more information on TI's A-D converters, op amps, and the LinCMOS process that creates them, call your authorized TI distributor or nearest TI sales office. Or write Texas Instruments Incorporated, Dept. SLAØ43E1, P.O. Box 809066, Dallas, Texas 75240.

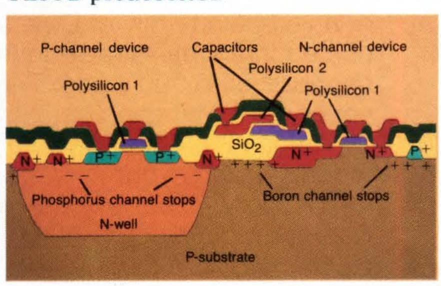
TI is first with silicon-gate CMOS for linear.

The key to a successful combination of CMOS and bipolar capabilities: Phosphorus doping of the silicon gates that effectively halts and binds sodium ions—the main cause of threshold voltage shifts in MOS-based technologies.

For enhanced carrier mobility, NMOS transistors are placed in a p-type substrate and the PMOS transistors in an n-well. This increases carrier mobility of the NMOS transistors to about 3.7 times that of the PMOS transistors, enhancing speed.

The LinCMOS process also provides a gate-to-drain capacitance about one-seventh that of metal-gate CMOS. This performance stems from gate formation, which is accomplished in the same step that forms the transistor source and drain. The source, gate, and drain are all self-aligned, boosting speed and enhancing the bandwidth even further.

And the final result: A built-in speed advantage that greatly enhances AC performance and makes possible the 20X speed improvement of the TLC532A over its pin-compatible metal-gate TL532 predecessor.



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CIRCLE 29

Solutions

High power on a low budget.

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Our HLW resistors are a cost-saving way to dissipate power from 3 to 20 watts. You get quick, easy board insertion, long-term wirewound stability, standard resistance as low as .1 ohm — plus fast availability from stock. HLW's are just part of a versatile family of Dale silicone-coated industrial wirewounds with power capabilities to 300 watts. They offer a variety of termination options and are available in tapped and adjustable models. For all your power handling needs, contact our experts at:
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CIRCLE 34

"S" Level with extras you'll appreciate.

Dale's SE.

We deliver metal film resistors that do more than just meet MIL-R-55182 for "S" level hermetically sealed parts. Our SE styles use patented construction to provide superior performance and environmental characteristics. And, our extensive factory and distributor stocking program makes them available faster in RNR55, 60 and 65 styles. Find out about our complete capability to develop specific reliability programs to your requirements.
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CIRCLE 35

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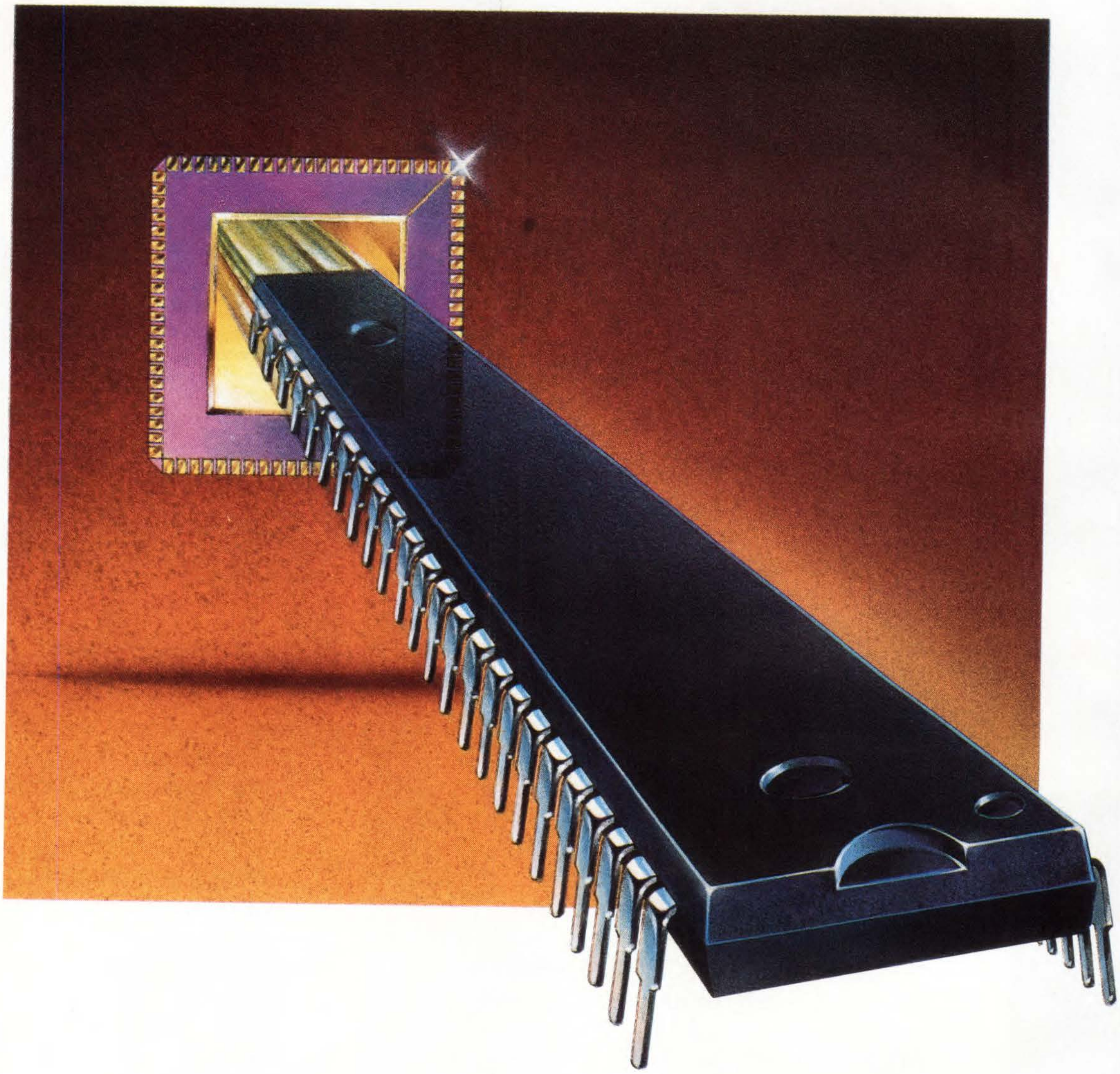


CONFERENCE PREVIEW

Artificial intelligence faces up to the challenges of the real world

The AAAI conference details the current strengths and weaknesses of AI as they apply to industry and where the field is going.

The state of artificial intelligence—today's catchword for many types of symbolic processing—and how it is moving out of the laboratory and academic environment into industry is the focus of this year's gathering of the academic and research community at the National Conference on Artificial Intelligence. Sponsored by the American Association for Artificial Intelligence (AAAI) and the University of Texas at Austin, the conference will be held Aug. 6–10 on the university campus.

For the first time, the conference will concentrate on the strengths and limitations of current AI technology and how it relates to industrial applications. In an effort to establish a sense of reality about AI, key panel discussions will concern what may happen if industry overscribes to the potential benefits of AI and how AI technology can be transferred to industry.

Despite the fact that many of the technical papers are concerned with AI theory, many others zero in on specific aspects of the technology whose impact is now, or will soon be, felt by industry, including development systems and languages for AI, expert systems, and the relationship of computer architectures to AI programs.

Ray Weiss

Where it's at

The present strengths of AI lie in software and hardware techniques offering limited solutions to specific problems. One of the obvious first steps in bringing these strengths to bear in industry is to make AI tools—languages and development systems—available. One such effort, from IBM Corp.'s Thomas J. Watson Research Center (Yorktown Heights, N.Y.) is an implementation of the AI language Lisp to run on VM-based systems (IBM 370s or other machines that can emulate those running with a VM operating system).

Another version of Lisp, known as "common Lisp," is the basis of an implementation devised by Gold Hill Computers Inc. (Cambridge, Mass.) to run on the IBM personal computer. Even more notable is a complete AI system, including an AI language and development software, from Tekronix Inc. (Beaverton, Ore.).

Finally, an interactive program serves as a tutor for Lisp programmers. Called the Novice System by its developers, the Advanced Computer Tutoring Project of the Department of Psychology at Carnegie-Mellon University (Pittsburgh), the system teaches users how to program in Lisp, pointing out programming irregularities and problems as they are entered.

Vying for much of the attention at various sessions will be expert systems, which collect a body of problem-solving rules from experts and attempt to apply those rules in a simulated "thought" process!

Using approximately 500 "if . . . then" rules, a real-time expert system has interactive control over an operating system to aid computer operators. Dubbed the Yorktown Expert System (YES) by its developers at IBM's Watson research center, the system is designed to work with the MVS operating system.

Doing the job

The initial implementation handles six types of activities: managing job-entry queue space, solving channel-to-channel link problems, scheduling large batch jobs, correcting MVS-detected hardware errors, monitoring the software subsystems, and monitoring the overall system performance. The knowl-

CONFERENCE PREVIEW

edge base was gathered from research staff, system programmers, MVS designers, and technical manuals.

An expert system for building expert systems comes from still another group at IBM's Watson research center. EMCYN is based on one of the first commercial expert systems, MYCN, which diagnoses blood disorders. It uses the expert system's skeleton with the domain (expertise) deleted so that different rules can be entered. It has room for about 400 rules.

Another expert system, built for the U.S. Navy, is aimed at equipment losses. Developed jointly by the Navy Center for Applied Research in AI (Washington, D.C.) and the Computer Science Department of New York University, the system categorizes, summarizes, and analyzes the reasons for the casualty loss of a broad variety of equipment.

Hardware for AI

Though much attention at the conference will focus on software, ongoing efforts to develop hardware that can run AI programs will occupy a share of the spotlight. Programs in AI languages generally run slowly on standard architectures. On the other hand, special machines to run these languages have in many cases been prohibitively expensive.

The FAIM-1 Machine Project at Fairchild Laboratories (Palo Alto, Calif.) has concluded that a number of architectural changes to standard microprocessors would speed up execution appreciably.

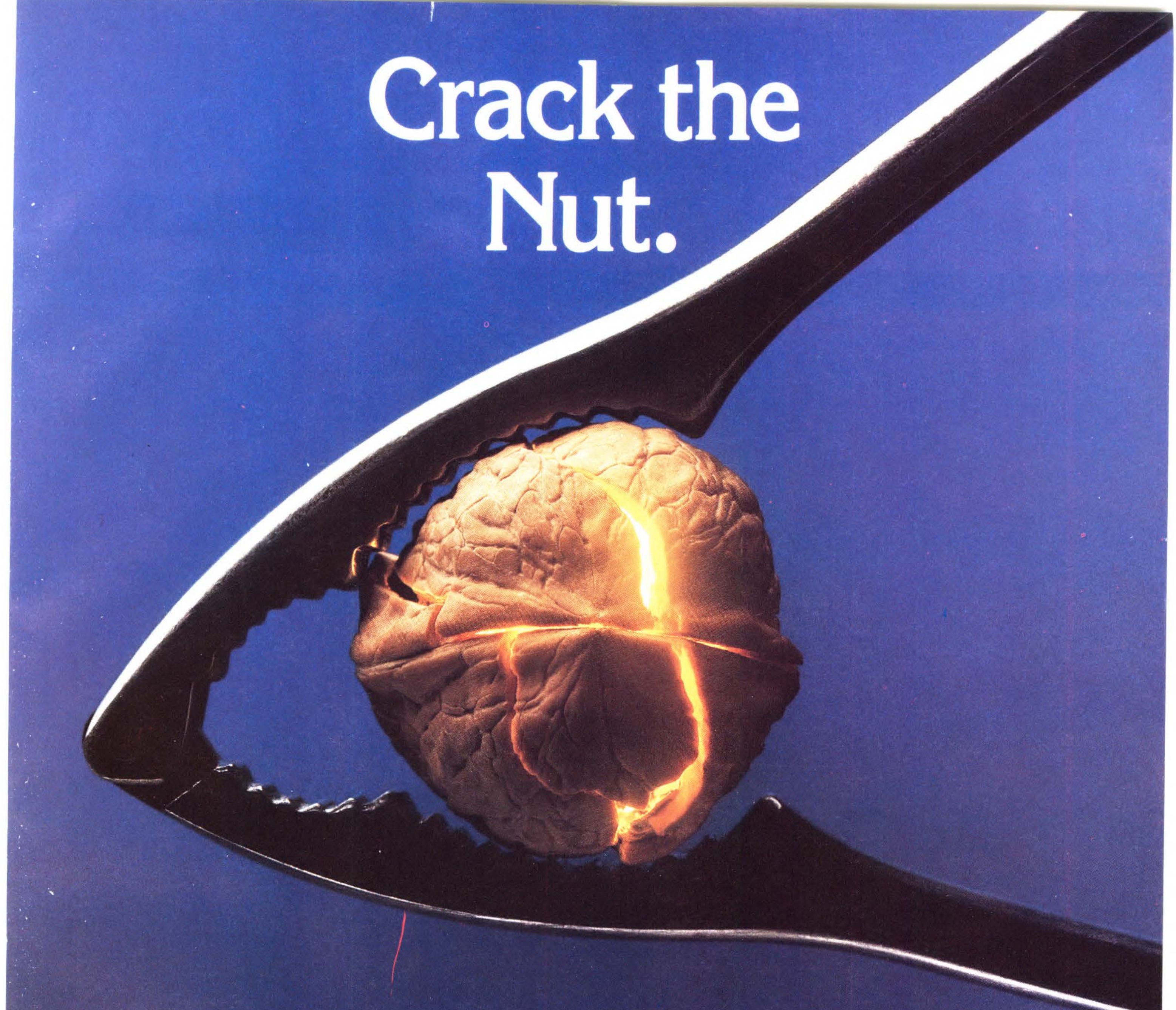
Its proposed solution for running Lisp, Zealisp, and other AI languages that use type checking and tagged architectures is to add special instructions to a standard microprocessor instruction set. These instructions would relate to the handling of tag values, the handling of indirect addressing without processor intervention, the use of upper address space as a tag field, and bit-field extraction instruction.

Less may be better

Investigators at Carnegie-Mellon University took a different tack. Their research indicates that a reduced-instruction-set computer (RISC) is the best vehicle for running AI software. Using OPS-5, an AI system also developed at Carnegie-Mellon, the researchers simulated the performance on various RISC and conventional machines. Their findings indicate that the RISC machines could execute most necessary instructions in only two machine cycles, compared with the four to eight cycles required for conventional computers.

The Fairchild and Carnegie-Mellon studies, however, agreed that the use of parallel systems will have only limited success in AI systems. In a simple simulation, going from 1 to 40 processors improved the performance only twelvefold. Memory bandwidth appears to be one of the major constraints.□

Crack the Nut.



The LAN nut.

When you're developing a LAN-based computer system, you're faced with a tough nut to crack. You need to know what's going on in your Local Area Network system. Many computers are carrying on many conversations. Simultaneously. And at speeds 10,000 times faster than traditional data communications. How do you test it? How do you debug it? How does the system really perform?

Excelan can help you crack that nut with the Nutcracker™, the world's only comprehensive analyzer/simulator for Ethernet systems. Packaged as an integrated workstation, the Nutcracker provides advanced LAN instrumentation hardware capable of making real-time diagnostic decisions at 10 million bits per second. Also included is an 8086-based CPU, about 1 MB of RAM, a 20 MB disk, a 600 KB floppy, keyboard, 12" CRT and 100 cps external printer, and complete menu-driven software that brings the power of the Nutcracker to you.

With the Nutcracker connected to the Ethernet cable, you're in control. You can create and detect pathological conditions for shake-down testing. Powerful filtering facilities allow you to extract precise packet substreams for triggering and tracing functions to find those elusive bugs. You can generate traffic for simulation of various load conditions. And high resolution time-stamping means you can track system performance against this regulated traffic load.

Increase your productivity, speed development time, and get your network system up and running — with confidence in it's performance and integrity.

Join computer industry leaders. Crack the LAN nut with the Excelan Nutcracker.

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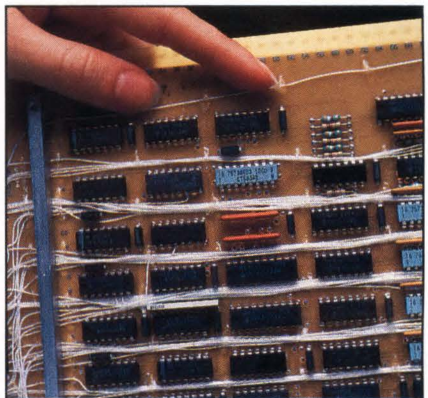
CIRCLE 39

A Texas Control

Months ahead of the market, Control Data is delivering the DDC (Director-to-Device Controller) interface on its 33800 Disk Storage Subsystem. It's an extremely compact, high-speed, large-capacity unit. Most important, it is the only available mass-storage subsystem plug compatible with the new-generation IBM DDC. What helps give Control Data this competitive edge? The SN75174 line driver from Texas Instruments.



Only TI's SN75174 line driver could provide the drive capability vital to Control Data's new 33800 disk storage subsystem featuring DDC interface.

No choice but TI

Only TI's SN75174 could provide sufficient differential current drive through Control Data's special compensation circuit to deliver proper signals in the DDC interface cable.

And Control Data will be able to stay current with future market developments because of the minimum active-high drive (40 mA) capability of the '174.

Forty-two '174s are used in a fully configured 33800 disk storage subsystem.

TI's SN75126 and SN75127 are also used in the new storage subsystem. These circuits meet the IBM 360/370 specifi-

◀ **Leading the market,** Control Data is shipping the first non-IBM storage subsystem that's plug compatible with the IBM Director-to-Device Controller interface. Use of TI's new SN75174 line driver not only made the Control Data design feasible but also minimized design time, component count, board size, and power requirements.

Instruments line driver drives Data to market faster.

cation, providing fault protection and power up/power down protection, as well as enable and fault flags.

Performance as specified

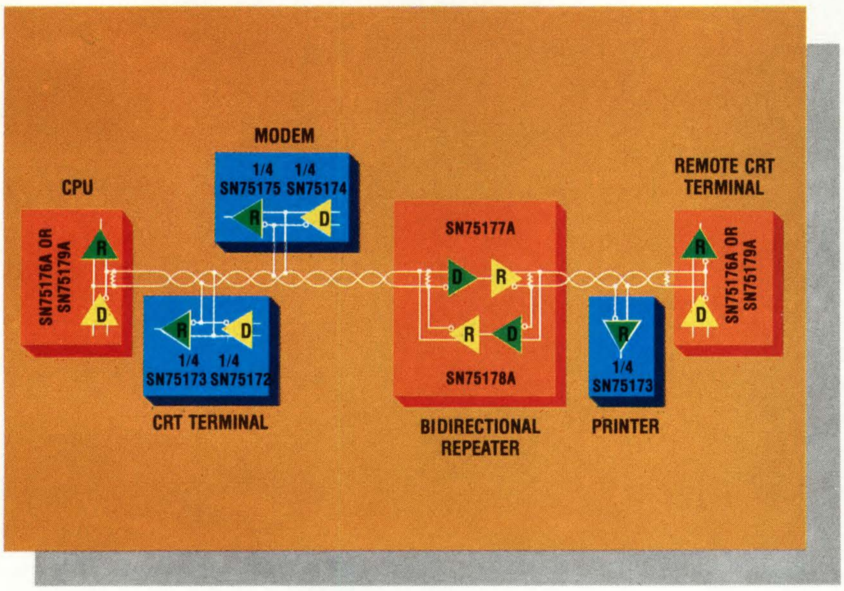
Control Data engineers learned about the '174 early on. Moving quickly, they evaluated and designed it in, counting on it to perform to very exacting specifications. It did . . . perfectly.

The alternative? Greater costs

Control Data engineers estimate that a discrete-component alternative would have resulted in at least a 15% increase in board area to accommodate the necessary additional components.

As it turned out, the SN75174 driver contributed important system savings to the design, improved reliability, helped Control Data get to market faster. ■

Get on the party line faster with eight new line circuits from Texas Instruments.



Hooking 32 driver-receiver pairs on a single bus to achieve party-line communication is possible with TI's full family of line circuits.

Now, eight new line drivers, receivers, and transceivers from Texas Instruments allow you to implement party-line applications on a single bus efficiently.

SN75176A Half-duplex Transceiver

This new circuit wraps the capability to send or receive data over a single twisted pair in a compact, 8-pin package. It saves board space and cuts component cost.

SN75179A Full-duplex Transceiver

Also available in a space-saving, 8-pin package, the SN75179A can send and receive data simultaneously, and requires two twisted pairs.

SN75177A/SN75178A Bus Repeaters

These two differential ICs are identical except for complementary enable inputs. The SN75177A is active high and the SN75178A is active low. This allows you to pair the two back-to-back for improved bidirectional communication when extending cable distance.

SN75172/SN75174 Quad Drivers, SN75173/SN75175 Quad Receivers

The two quad drivers operate from a single +5 V supply, yet maintain a high-impedance output over a common-mode range from −7 V to +12 V with power on or off. Without sacrificing speed. Both drivers have maximum delay times of 50 ns, rise and fall times of less than 80 ns. They allow data rates up to four megabaud.

The major difference between the two drivers is the enable scheme. And this increases design flexibility. All four drivers in the SN75172 are enabled at once, whereas they are enabled in pairs in the SN75174.

The two quad receivers are similar to existing RS-422 devices but have higher input impedance and extended common-mode range, from ±7 V to ± 12 V. Sensitivity is ±200 mV over −12 V to +12 V common-mode range.

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In addition to offering these new devices that meet RS-422 and other party-line applications, TI offers the industry-standard ICs you need to meet the EIA RS-485, RS-232-C, and RS-423 standards, as well as IEEE 488.

In fact, with its wide selection of general-purpose line circuits, TI fields the industry's broadest line of line circuits. Results: Component compatibility, design flexibility, and immediate availability.

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CIRCLE 27


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VIEWPOINT

Program maintenance will gain the most from integrated software tools

Leon Presser
President
Softool Corp.
Santa Barbara, Calif.

The time has come, believes Leon Presser, for software developers to extend their focus from short-term programming concerns to the long-term maintenance and updating needs of their software projects.

"Maintenance constitutes 70% to 80% of the time and money spent on large software packages." he notes. "Sadly, the fact that we spend so much on maintenance means that the quality is just not there to begin with."

To get quality software and therefore lower maintenance costs, Presser maintains, "we should plan for the entire product cycle. We must then concentrate on the initial requirements and design phases, ensuring that the software is well structured and maintainable over its life cycle."

Fortunately, adds Presser, "software technology now exists that can increase a programmer's productivity tenfold," not only in terms of the time spent initially developing programs but also with respect to maintenance. "There is a bit of irony in all this," reflects Presser. "Software, an industry that specializes in automating other technologies, has been slow in automating its own critical processes."

Ray Weiss

Leon Presser founded Softool in 1977, following several years of teaching at the University of California. He holds an MSEE from the University of Southern California and a PhD from the University of California at Los Angeles. He has written more than 30 technical articles and collaborated on three books on computer science.

Like many others, Presser sees a solution in the integrated software environment, one that follows all stages of a program's life—from initially defining the requirements and designing a structure that fulfills those requirements to actually writing the program and subsequently maintaining and revising it.

"It's a matter of priorities. We must put our efforts where the problems—and costs—are. Better languages or editors won't help us enough."

"Instead," Presser suggests, "we must integrate the tools and techniques that can produce, control, and monitor an application program throughout its useful days. We can cut both costs and errors dramatically by automating many tedious labor-intensive tasks."

"It's a matter of priorities," he insists. "The sooner we accept and adopt the integrated environment, the better we can aim our efforts at the problems of poor quality and costly maintenance."

Whereas much of the mundane bookkeeping and manual chores have traditionally been relegated to the software systems serving the programmer, Presser explains, "we're now at a place where both the physical hardware and the operating system are becoming transparent to the high-level programmer. The uniform and consistent setting that results proves to be an ideal vehicle for automating the costly, labor-intensive aspects of software development and maintenance.

Presser's vision of the ideal integrated environment combines a straightforward user interface with maintenance aids that supplement the standard software tools. "We're talking about tools that track program changes, versions, and configurations; ones that locate inefficient code and optimize it for a particular application; and still others that test software at all levels and detect errors. Other types of tools will automatically document new and existing code or evaluate the impact of changes on existing software."

The planning and control offered by those and other tools promise to raise programmer productivity and minimize maintenance.

"The technology is already at hand," insists Presser. "The key factor is how quickly and easily industry can adjust to the integrated development and maintenance environments."

To achieve speaker independence, speech recognition systems need a knowledge of English, AI approach

Sam Viglione
President
Interstate Voice Products
Orange, Calif.

Sam Viglione, a pioneer in speech recognition, is the president of the year-old Interstate Voice Products, which grew out of Interstate Electronics. Earlier, he worked for McDonnell-Douglas Astronautics.

True speaker-independent speech recognition will depend on more than advanced digital signal-processing chips, contends Sam Viglione. It will also call for both a processing approach that recognizes the structure of the English language and a computer that adheres more closely to artificial intelligence than to conventional computing tenets.

Viglione predicts that the first generation of speaker-independent recognition computers will make its debut within the next five years. In all likelihood, they will incorporate many parallel processing elements and recognize about 100 words in short phrases, regardless of the speaker.

"Beyond 100 words," explains Viglione, "the processing machinery not only will have to respond to words and voices but will also have to associate those words with the structure and syntax of the English language, as well as make judgments on what it understands."

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Stephan Ohr

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CIRCLE 45

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the first generation," Viglione insists, "but making those speaker-independent systems affordable and practical for most applications will be the major problem."

The current state of speech recognition is characterized by isolated spoken words—here, operands—which a microprocessor or digital signal processor compares with stored patterns. The latest speech recognizers—based, for instance, on the 80186—can respond to as many as 240 discrete (isolated) words.

By precoding the words, the systems diminish somewhat the differences between several speakers' voices. Nevertheless, since the specific operands are created by sampling one individual's voice, few of those systems can be considered genuinely speaker-independent.

Attaining true speaker independence is a goal complicated by two factors: the frequency differences among voices and continuous speech behavior, which makes dissimilar words sound the same when uttered in a sentence. To surmount those difficulties, Viglione expects that future speaker-independent recognizers will be forced to break the sentence into isolated words by sampling the spoken phrase at appropriate intervals, say, every 20 ms. They will then have to examine the sentence structure and interpret the intonation to correctly identify the words.

Today's techniques have already produced speaker-independent computers that respond to what Viglione calls "digits"—the numbers one through ten. The structure of each digit (that is, the configuration of formants, fricatives, and sibilants) is so distinct that one digit can rarely be confused with another. Viglione pegs the hit rate—that is, the rate of successful recognition on these prototype systems—of about 98% for roughly 85% of the North American population.

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CIRCLE 41

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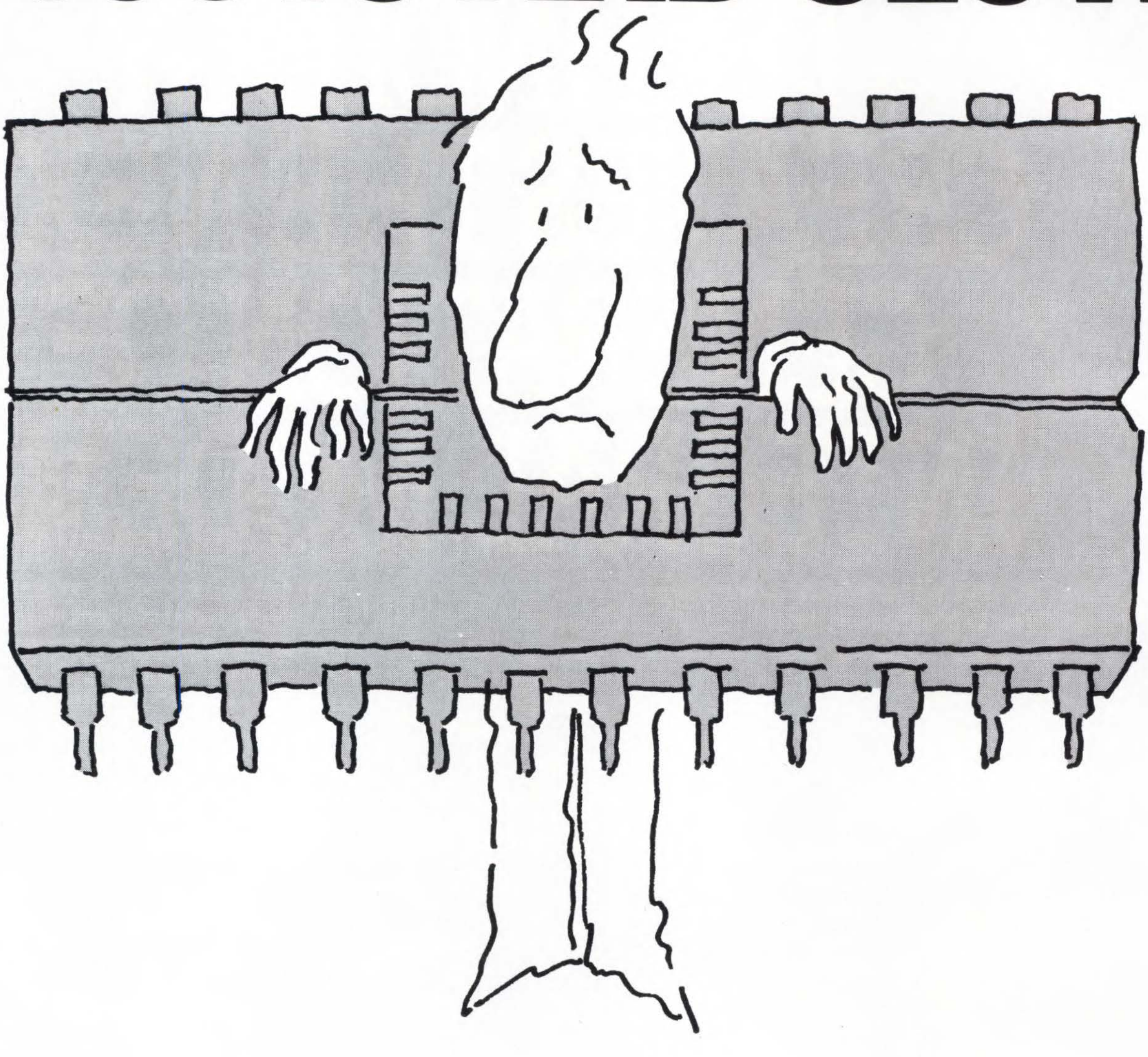

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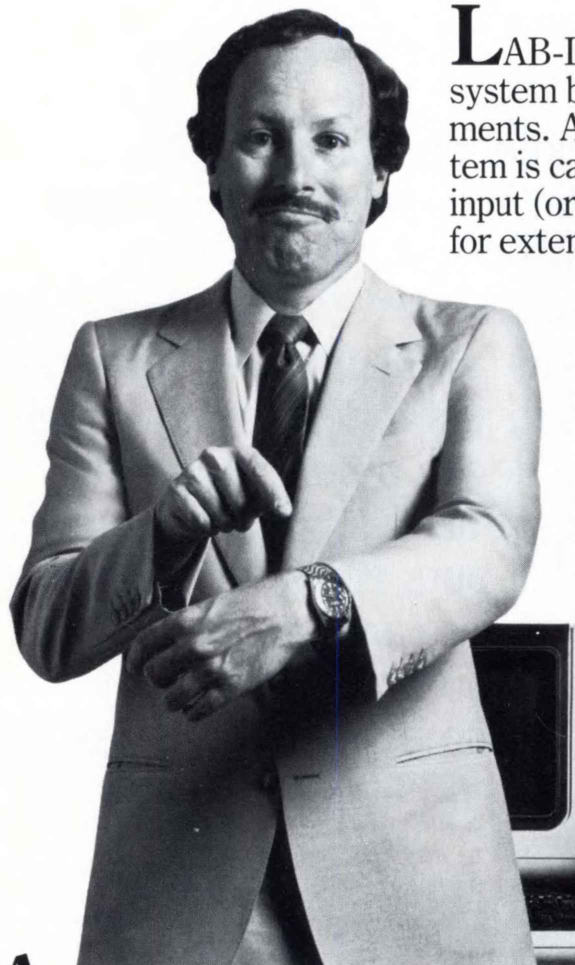
Fred Molinari, President



LAB-DATAX is a microcomputer based data acquisition system built for the most demanding laboratory environments. As you can see, this system is capable of continuous data input (or output) at high speeds for extended periods of time.

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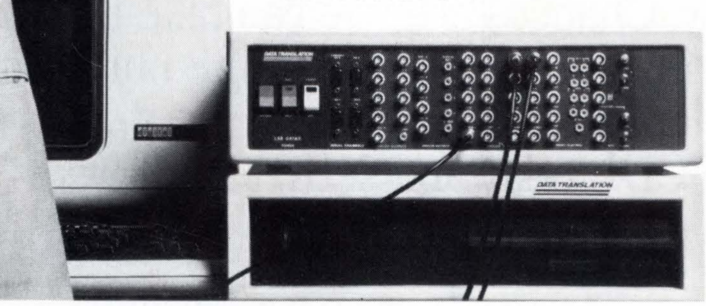

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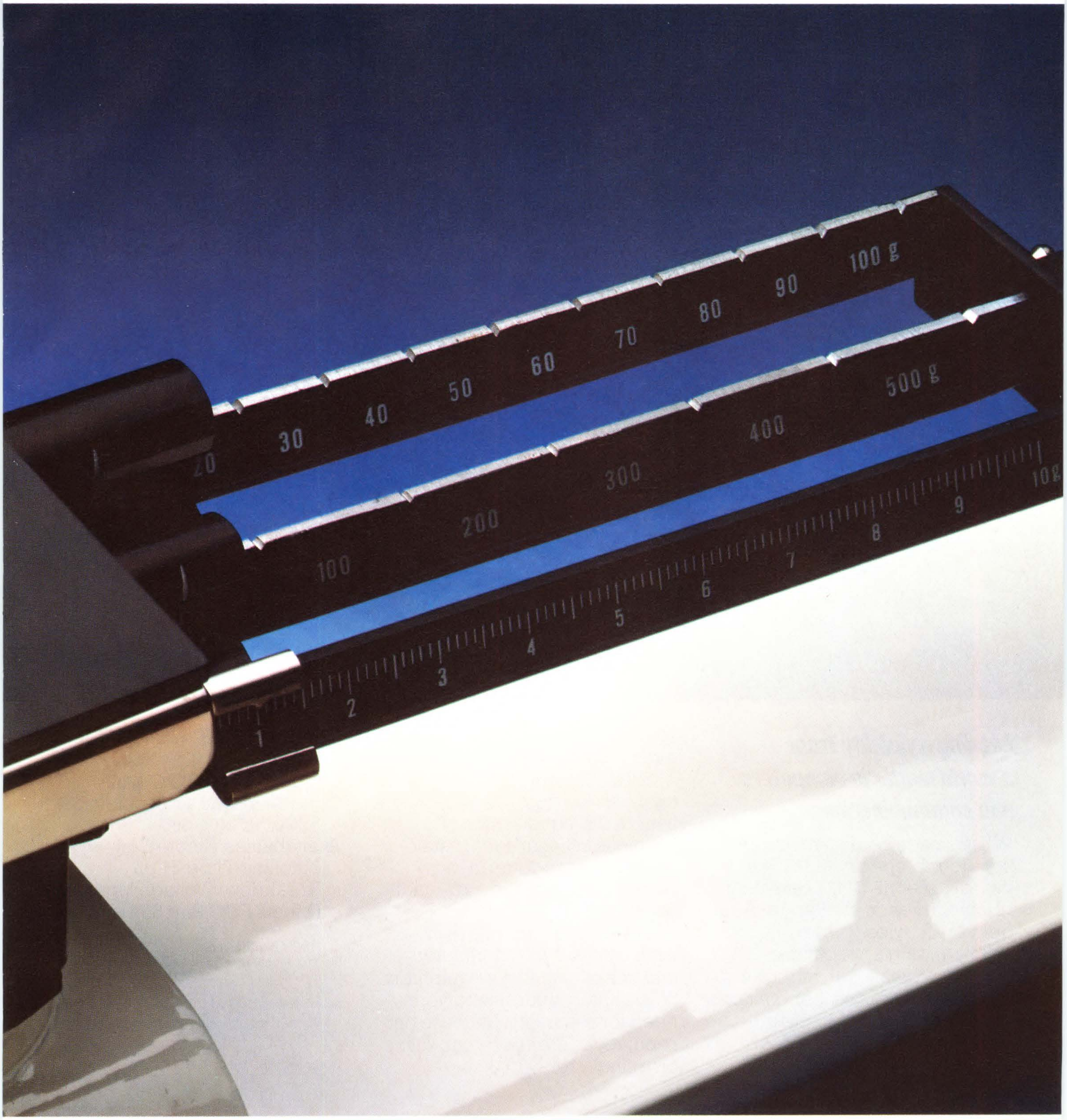
 CIRCLE 47

PER GRAM.



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CIRCLE 51

AI system speeds displays, using graphics boards in place of memory banks

Graphics drivers directly linked to a supermini's CPU and terminals can update a bit-mapped screen in under 1 ms.

The sophisticated man-machine interface that characterizes an artificial-intelligence system places a tremendous strain on such a sytem's ability to handle graphics. The critical factor in these cases is how fast a system responds. The most effective way to drive graphics terminals is directly from the system processor, but until now no artificial-intelligence machine could do so. A computer planned for release later this year, however, changes all that.

The multi-user KPS-10 knowledge-processing system simply substitutes graphics drivers for memory banks, allowing bit-mapped terminals to be updated as quickly as the computer cań write to its memory. In fact, a 1180-by-1440-dot screen can be updated in less than a millisecond.

In comparison, systems that use RS-232 links to update graphics screens can sometimes take minutes to build a picture. DMA schemes, on the other hand, are usually fast enough for the job. Unfortunately the extra receiver circuits they demand drive up the price of the graphics terminals.

Mitch Beedie

10 links in a chain

The KPS-10, from Racal-Norsk Ltd. (Fleet, England), is based on the Norsk Data ND-570, a 32-bit superminicomputer that works with up to 10 daisy-chained main memory banks. The memories, which have 4 Gbytes each of virtual storage for both data and instructions, are linked by an internal communications bus that requires more than 100 balanced line drivers and receivers to handle the address, data, and control lines. A bus of that type is rarely found in minicomputers. The setup is, however, ideal for transmitting information over long distances—for example, to graphics terminals 100 meters from the computer.

Each graphics board drives a bit-mapped monochromatic terminal. In theory, the system can manage 36 bit-mapped screens and still leave one memory bank free. The practical limit, however, is 20 screens. It is set by the amount of processing that must be carried out in artificial-intelligence systems.

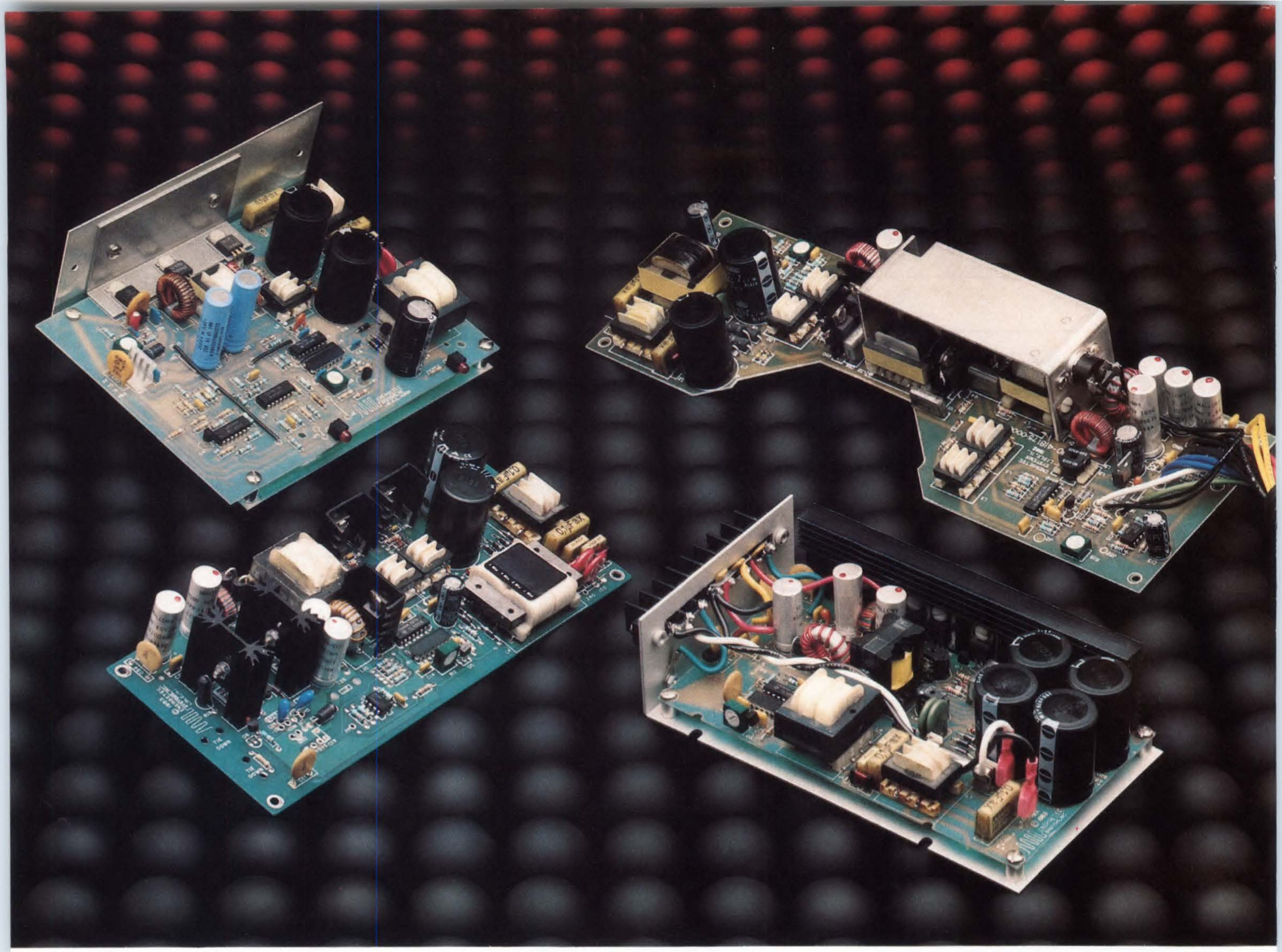
Four for one

Every monochromatic display can be refreshed on four independent bit planes using the graphics board's 1-Mbyte memory. Further, each plane can be selected instantaneously and has independently variable contrast.

Since up to four displays can take the place of a single memory bank, different arrangements of terminals can be had—monochromatic, monochromatic with gray scaling, and color.

Normally, a board drives a single monochromatic terminal. Two boards also can be linked in parallel, with one supplying a new display as the user is working with the screen drawn by the other.

A color terminal is driven by two boards, with a color controller taking the place of the third board. The fourth can still drive a monochromatic display. The data from the bit planes on the display controllers is used to address a look-up table on the color controller. The outputs from the look-up table power three high-speed digital-to-analog converters, which supply the red, green, and blue outputs to the monitor.□



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CIRCLE 52

INTERNATIONAL MEETINGS

Mechatronics Autofact Japan '84, Aug. 2–6. Minato Fairgrounds, Osaka, Japan. Leslie Hossack, Society of Manufacturing Engineers, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-0023.

Conference on Precision Electromagnetic Measurements, August 20–24. Delft, the Netherlands. H. Postma, Delft University of Technology, PO Box 5031, 2600 GA Delft, the Netherlands; (31) 15 781736.

Electronic Industry Production and Testing Equipment Exhibition, Aug. 27–31. American Trade Center, Taipei, Taiwan. Cordag Associates, Inc., 4405 East-West Highway, Bethesda, Md. 20814; (301) 652-6403.

Euromicro '84 Symposium, Aug. 27–30. Copenhagen, The Netherlands. Euromicro, p/a TH Twente, Dept. INF, Room A306, PO Box 217, 7500 AE Enschede, the Netherlands; (31) (53) 338799.

1984 International Conference on Solid State Devices and Materials, Aug. 30–Sept. 1. International Conference Center Kobe, Kobe, Japan. The Japan Society of Applied Physics.

Regional Micro-Computer Shows, Sept. 4–6. Hotel Stuttgart International, Stuttgart, West Germany. Networks Events Ltd., Printer Mews, Market Hill, Buckingham, MK181JX, England; (0280) 815226.

Electronic Displays, Sept. 5–7. Frankfurt Inter-Continental, Frankfurt, Germany. Networks Events Ltd., Printer Mews, Market Hill, Buckingham, MK18 1JX, England; (0280)815226.

Tenth European Solid-State Circuits Conference (ESSCIRC '84) Sept. 19–21. Edinburgh, England. ESSCIRC '84 Secretariat, CEP Consultants Ltd., 26 Albany St., Edinburgh EH1 3QH, England; (031)-557 2478.

Sama/Swissdata/Autofact Europe '84, Sept. 25–29. Swiss Industries Fair, Basel, Switzerland. Leslie Hossack, Society of Manufacturing Engineers, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-0023.

Eurocon '84, Sept. 26–28. Brighton, England. Conference Services, Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, England; 01-240 1871, ext. 222.

International Symposium on Industrial Robots (ISIR), Oct. 1–4. Gothenberg, Sweden. Patricia Van Doren, RI/SME, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, ext. 369.

World Conference on Ergonomics in Computer Systems, Oct. 1–2, London, England; Oct. 3-4, Dusseldorf, West Germany; Oct. 4-5, Helsinki, Finland. Robert W. Bailey, Computer Psychology Inc., 54 E. Main St., PO Box 16, Mendham, N.J. 07945; (201) 543-9009.

Infomatics '84, Oct. 2–4. Singapore, China. Infomatics '84, PO Box 34404, Bethesda, Md. 20817; (301) 983-0604.

Toronto Tool & Manufacturing Engineering Conference & Exposition, Oct. 2–4. International Centre, Toronto, Ontario. Tom Reichert, Expositions Division, Society of Manufacturing Engineers, 1 SME Drive, PO Box 930, Dearborn, Mich. 48121; (313) 271-1500, ext. 323.

Japan Electronics Show, Oct. 4–9. Harumi International Fair Ground, Tokyo, Japan. Japan Electronics Show Assn. Tokyo Chamber of Commerce Building, 3-2-2, Marunouchi, Chiyoda-ku, Tokyo, Japan.

Taiwan Electronics Show, Oct. 5–11. Taipei Sungshan Airport, Taiwan, China. China External Trade Development Council, Taipei Sungshan Airport, Taiwan, China.

1984 APL Users Meeting, Oct. 15–17. Westin Hotel, Toronto, Canada. Rosanne Wild, I.P. Sharp Assoc., Ltd., 2 First Canadian Place, Suite 1900, Toronto, Ontario, Canada, M5X 1E3; (416) 364-5361.

International Electronic Packaging and Production Equipment Conference and Exhibition, Oct. 16–18. Metropole Exhibition Centre and Brighton Centre, Brighton, England. Tom Webb, BTDO, 845 Third Avenue, New York, N.Y. 10022; (212) 752-8400.


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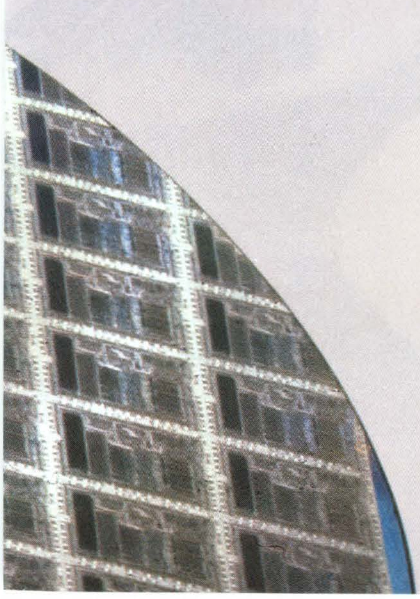

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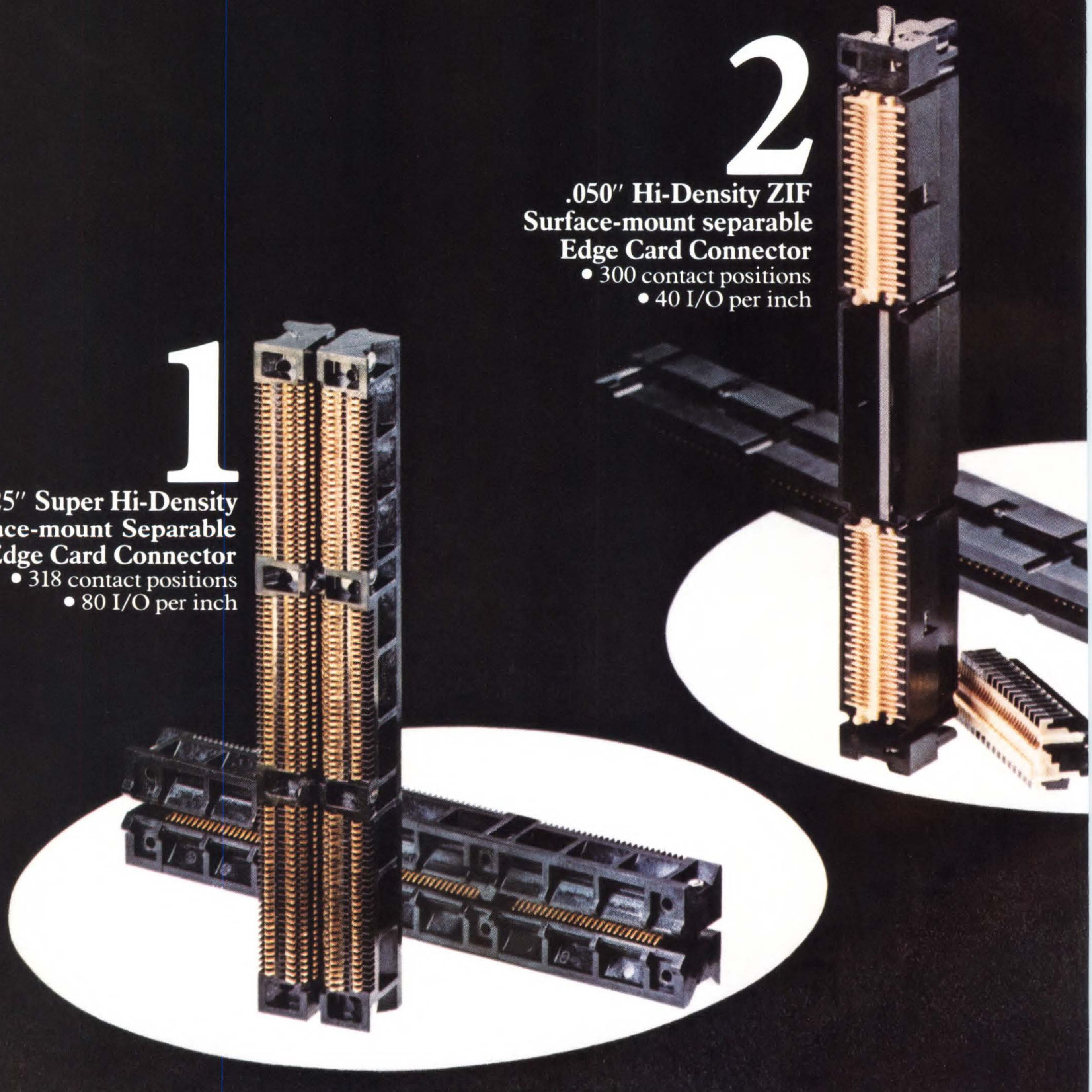

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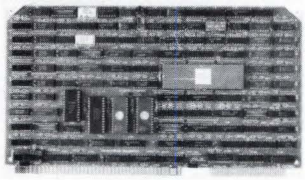
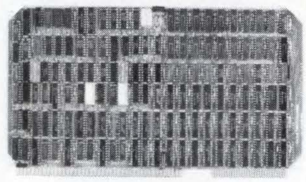
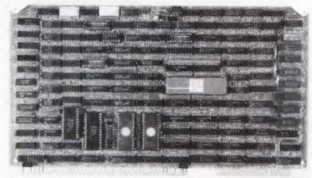


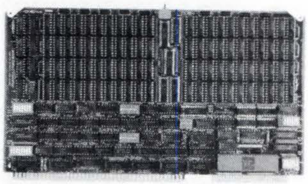
12.5 MHz 68000 CPU



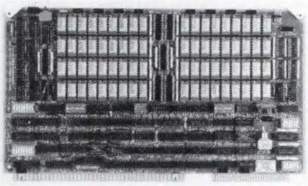
iLBX* Cache Memory Board



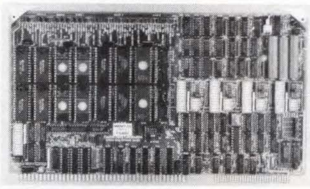
10 MHz Z8000* CPU



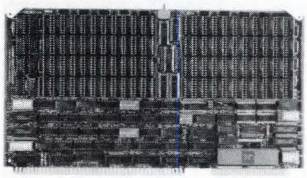
180ns 128K-2Mb EDC DRAM Board



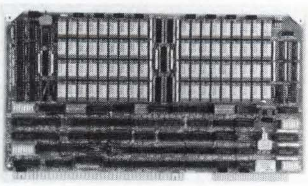
140ns 128K-512K EDC DRAM Board



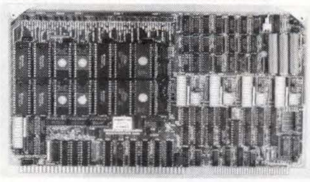
EPROM/RAM/EEPROM Board
with Real Time Clock/Calendar



170ns 128K-2Mb Parity Only
DRAM Board

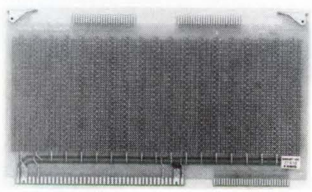


135ns 128K-512K Parity Only
DRAM Board

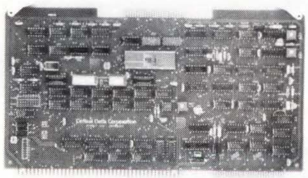


Static RAM Board with 128K CMOS

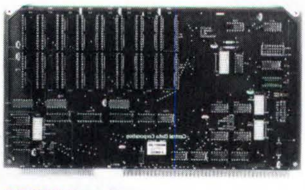
iLBX Backplane



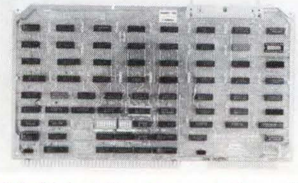
Prototyping Board



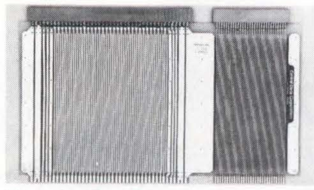
Double-Density Floppy Disk
Controller



PROM Board

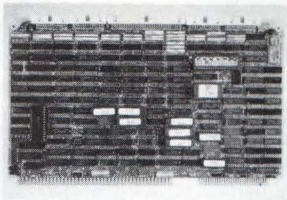


QIC-02 Cartridge Tape and Controller

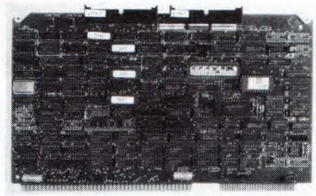


Extender Board

C2000 System Cabinet



SMD Disk Controller



9-Track Tape Controller

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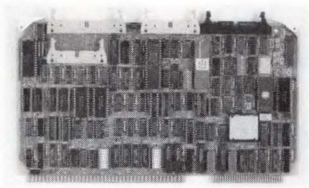
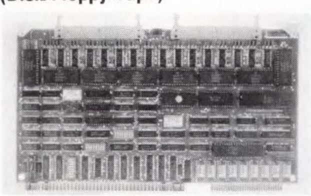
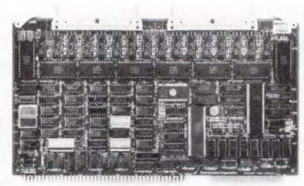


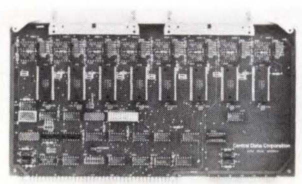
Multi-Media Controller (Disk/Floppy/Tape)



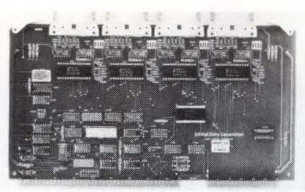
High Performance Octal Serial Interface



Intelligent Octal Serial Interface



Octal Serial Interface



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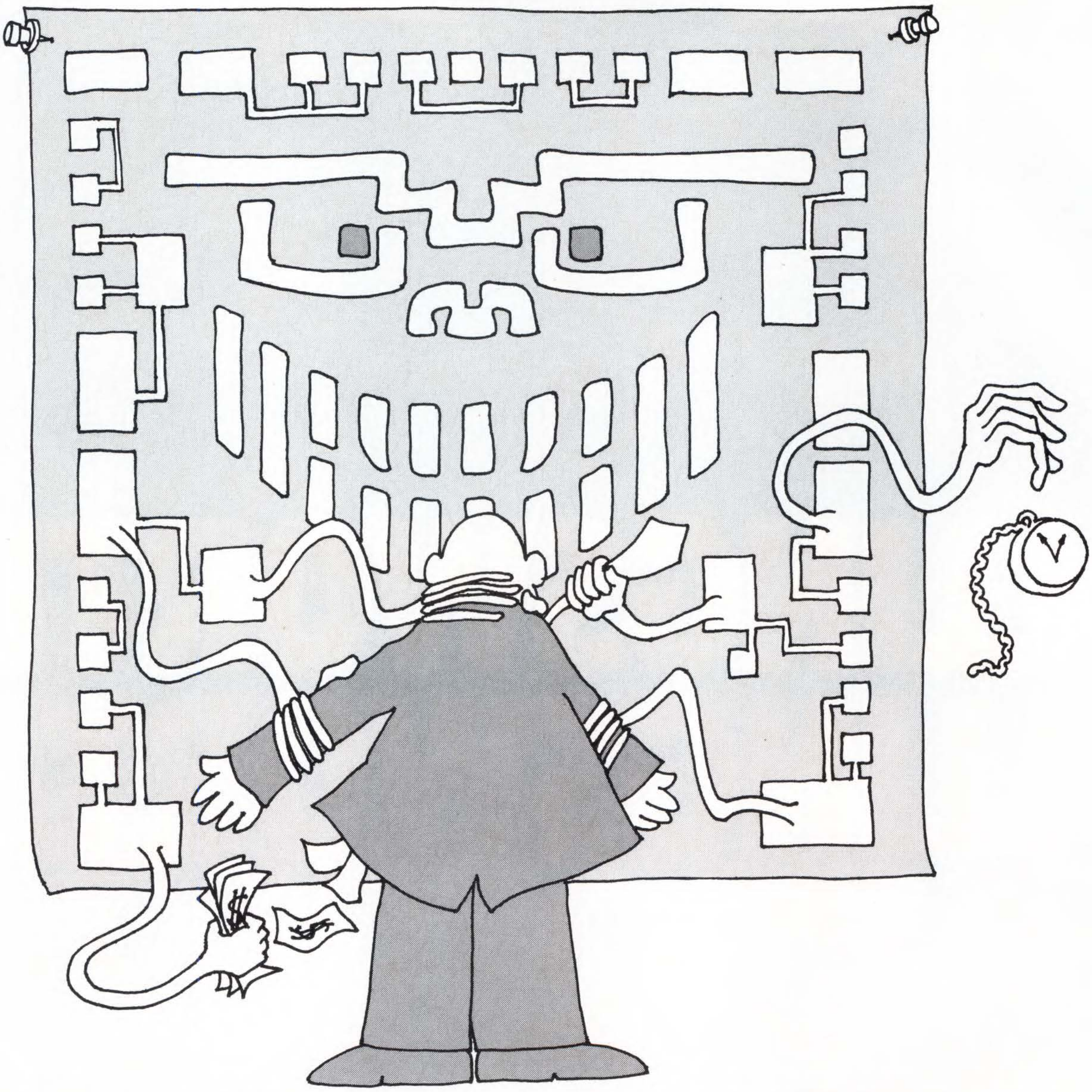

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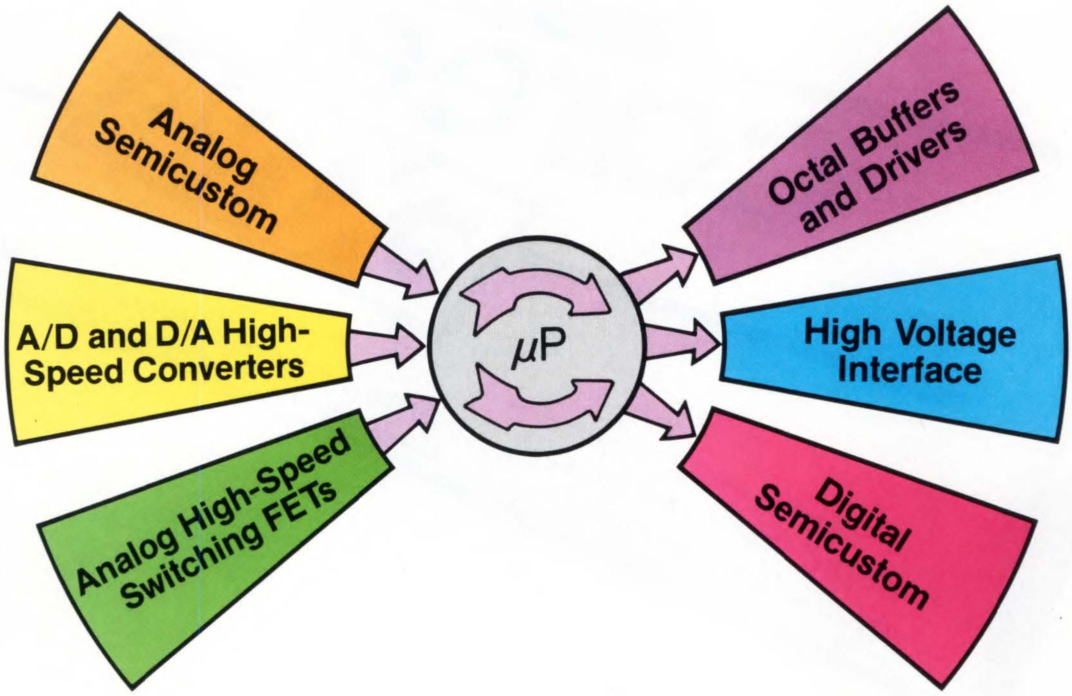

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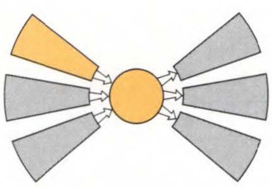

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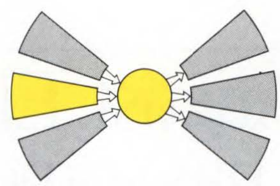

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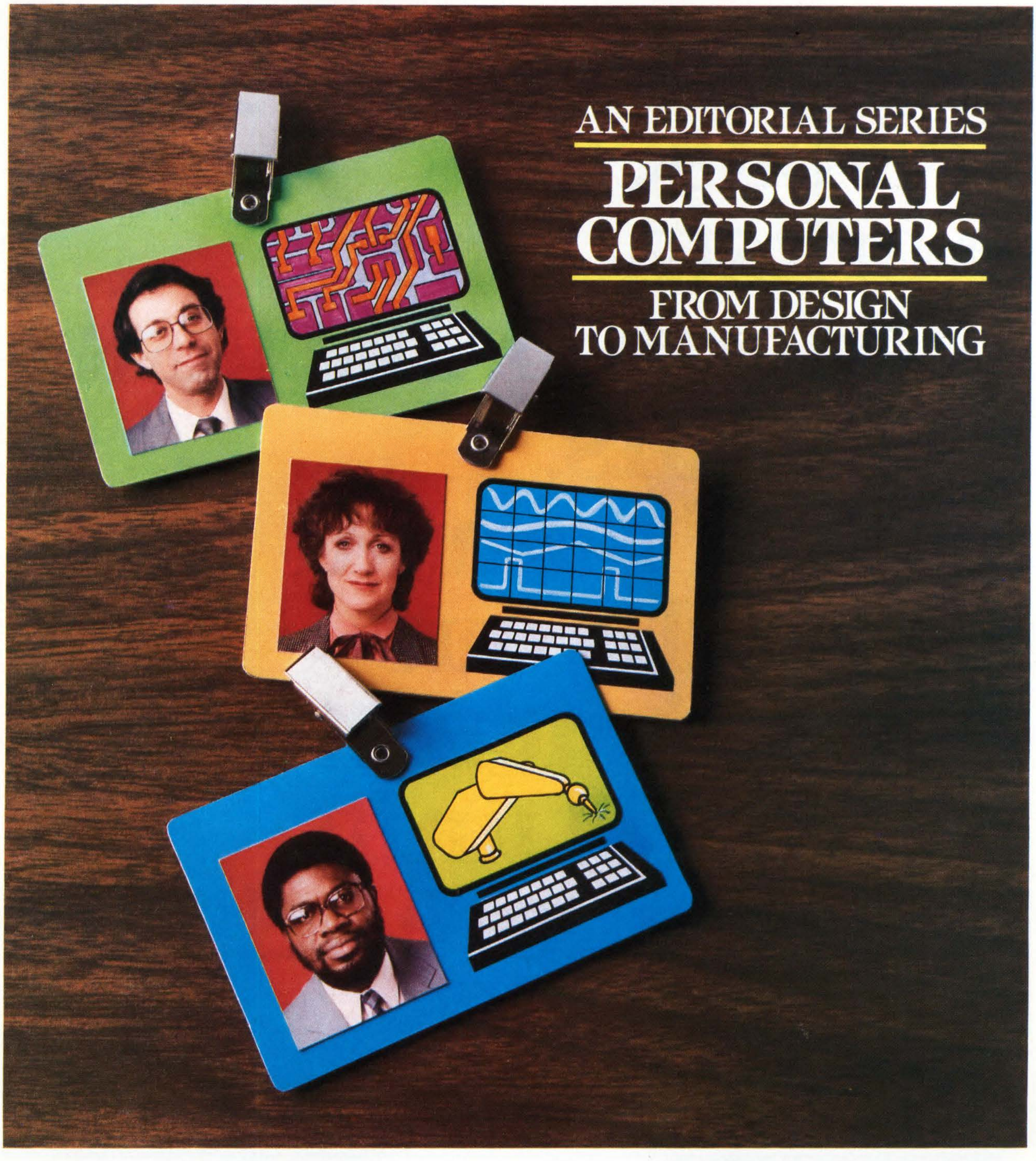
CIRCLE 113

DESIGNING OEM SYSTEMS

AROUND PERSONAL COMPUTERS



Evaluating today's PC-based workstations is a formidable task for OEMs. A brief manual that calls out the salient features of typical units should prove helpful.

Jesse Shereff

As the sophistication of personal computer-based workstations rises and their prices fall, more engineers and managers are installing the machines on their desks. Many of those systems arrive with manufacturer-supplied but user-assembled hardware and software. Special-purpose applications, however, are being served quite well by systems that have been enhanced and repackaged by OEMs. In some cases, in fact, OEMs have added so much specialized software or hardware that users would be hard-pressed to recognize the original workstation.

OEMs find personal computer-based workstations irresistible, largely because of open-ended architectures, the proliferation of third-party enhancements, or the low price of the system. The IBM PC personal computer and several other well-entrenched workstations fit those categories. Other systems—the Symbolics 3600, for example—incorporate such outstanding sophisticated features that they appeal to OEMs, even though their original package might not afford much flexibility.

Though a complete list of actual and potential applications for all workstations would be virtually impossible to compile, what follows is a select sampling of ten workstations that have found a place in the OEM world, ranging in sophistication and size from the Symbolics 3600 to the IBM PC and in base price from several thousand dollars to well over $80,000. Between those two machines lie eight other workstations, including the Texas Instruments Nu Machine, the HP 9000 Model 520, the Masscomp WorkStation-500, the Apollo DN460 and DN660, the Sun-2, the DEC MicroVAX I, and the Apple Lisa 2.

Some trends seem apparent in the midrange workstations. To start with, the future seems to rest in 32-bit processing, whether through proprietary CPUs or through the 32-bit internal architecture of the industry-standard 68000. Second, many systems continue to use the 16-bit Multibus, though the next generation will likely opt for 32-bit buses, following the route already taken by the Nu Machine, which uses the 32-bit NuBus. What's more, most workstations make network provisions, with Ethernet leading the list and one company, Apollo, designing its computational nodes primarily for a proprietary network.

As for operating systems, Unix, with virtual memory capability and often Berkeley enhancements, has captured the attention of most system software developers. Many of those suppliers have both the standard Unix and Berkeley Unix environments running simultaneously.

Given that high degree of standardization—68000 processors, the Multibus, Unix, Ethernet—the compatibility among systems is on the rise. Independent hardware and software designers work easily with widely accepted components. If hardware and software enhancements can be attached to several systems, an OEM need not depend on one source for the basic workstation.

The choice and sequence of workstations presented here is meant to be representative, not definitive. The entries should not be considered superior to systems not covered—space is the sole consideration. Within each system's specifications is the minimum configuration offered by the manufacturer, an "official line" that can usually be negotiated. Whereas some workstation makers offer only fairly complete packages, others may sell as little as the motherboard.

Symbolics 3600

Symbolics Inc., 4 Cambridge Center, Cambridge, Mass. 02142; Scott Garron, hardware products manager, (617) 576-1043.

Specifications

Processing elements: 36-bit proprietary CPU with microprogrammed instruction set designed for Lisp, 180- to 250-ns cycle time, and 20-Mbyte/s transfer rate. Operating features include run-time data-type tagging and checking, instruction prefetching, a stack-oriented architecture, and hardware-assisted garbage collection. A floating-point processor can be optionally integrated.

Serving as the front-end processor is a 68000 processor dedicated to controlling I/O, logging errors, and initiating recovery procedures. It contains 128 kbytes of RAM and 64 kbytes of EPROM and handles DMA transfers at 1 Mbyte/s.

Memory: 2 Mbytes of RAM (minimum), 30 Mbytes (maximum), and 1 Gbyte of addressable virtual memory.

Mass storage: A 167-Mbyte Winchester drive (minimum), a 474-Mbyte Winchester drive (optional), and a 300-Mbyte removable hard-disk drive (optional).

One TC20 ¼-in. tape cartridge is required at each site, with a capacity of 45 Mbytes and nine tracks. (Symbolics updates the software on these cartridges.) A TD80 nine-track drive (optional) works in the start/stop mode at 25 ips and in the streaming mode at 100 ips for 1600 bpi or at 50 ips for 3200 bpi.

Network: An Ethernet controller is on the L bus backplane; communications packages are written in Lisp.

Backplane: The L bus is a private communication channel; A Unibus (and soon Multibus) interface controller is optional; bus memory map is stored in the front-end processor.

Ports: Three RS-232 serial lines, connected to the front-end processor, handle 19.2 kbits/s.

Graphics: 1280 by 1040 pixels by 8 bit planes, 16.8 million colors.

System software: Written in the Lisp language, with all source code included. Facilities include flavor-based windowing, menus, and error handling; real-time text editor (ZMACS), which interprets and compiles Lisp forms; incremental compilers; dynamic loading and linking; display-oriented debuggers; compatibility package for running Interlisp 10, Interlisp-VAX, and Interlisp D on 3600.

Languages: Symbolics' own Zetalisp dialect, with enhancements like flavoring.

ANSI Fortran 77—implemented under Lisp environments, compiled into Lisp code, and then recompiled. Fortran programs become Lisp functions invoked by Lisp calls. The system also treats Pascal (IBM 370-compatible) in the same manner.

MACSYMA—software for symbolic mathematical manipulation.

Minimum OEM configuration: Complete 3600 workstation, with modules possible in the future.

One of the largest and most powerful single-user workstations, the Symbolics 3600 incorporates the hardware and software required to run Lisp, an artificial-intelligence language that handles symbolic relationships and processing, as well as numerical computations.

Its proprietary hardware and software complement each other. The 36-bit CPU, which performs integral and run-time data-type tagging and checking, can transfer data at 20 Mbytes/s and address 1 Gbyte of virtual memory. With superminicomputer power, the machine can execute operations at the rate of 1 million a second. The architecture uses a large stack buffer with hardware pointers. Speed is enhanced with an instruction pre-fetcher, a large instruction cache, and garbage collection.

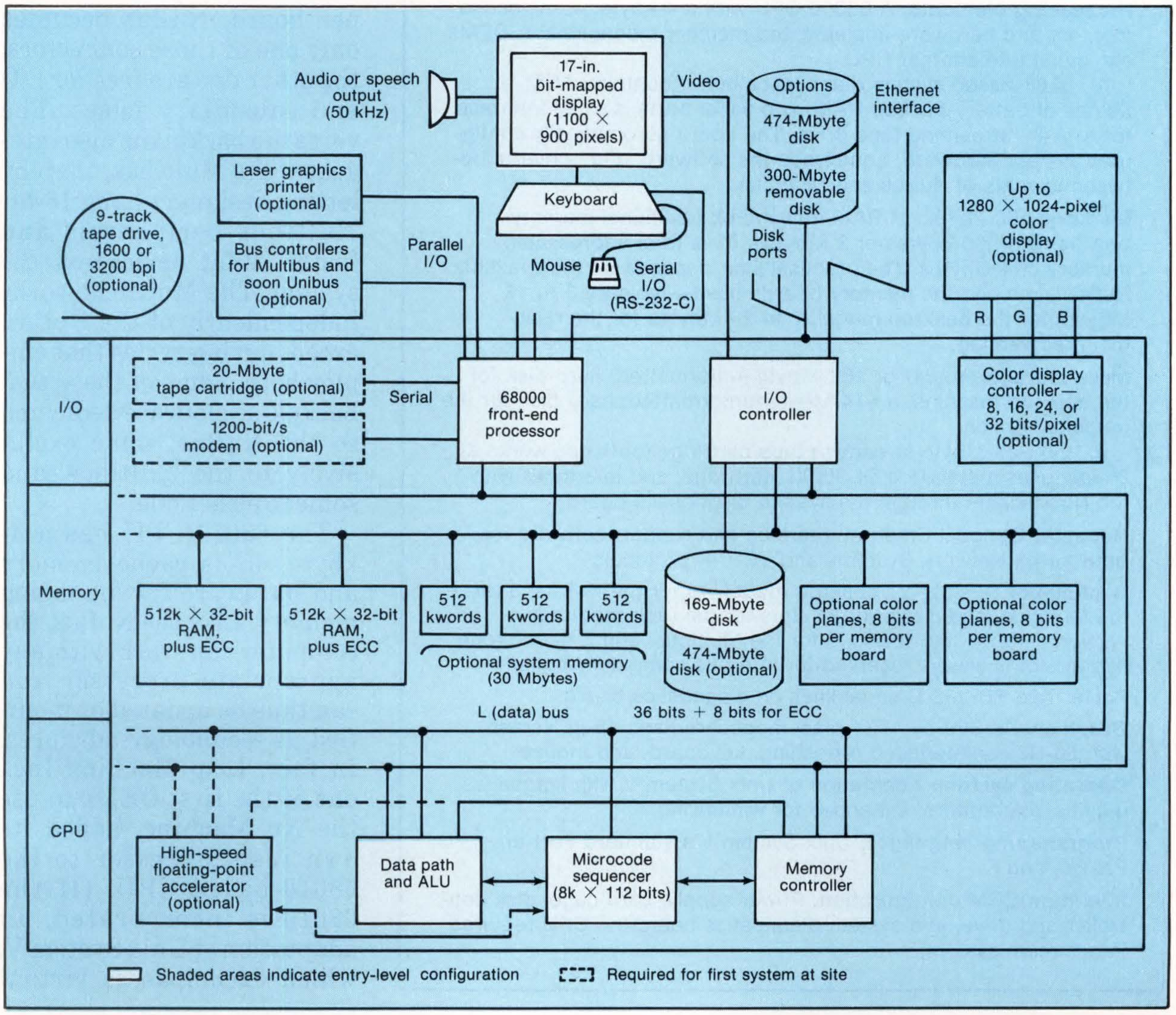
Lisp source code is a standard feature of the machine. Obviously, the 3600 differs greatly from systems that merely graft the Lisp language onto a typical computing structure.

Among the machine's powerful software development tools are incremental compilers, which play a part in translating Fortran and Pascal programs into Lisp-type instructions.

An enhanced dialect called Zetalisp adds the unique "flavor" concept to defining and relating objects. Flavoring permeates windows, graphics, menus, and virtually all other aspects of the Lisp-based system. Because the machine makes no distinction between the operating system and the integrated system utilities, programmers can extend the behavior of most utilities using their own Lisp code.

The CPU, front-end processor, memory, mass storage, and most peripherals communicate over the proprietary L bus, to which an OEM generally has no access. The machine has a Unibus and soon a Multibus, enabling a chassis to be attached for standard Unibus and Multibus peripherals.

Given the complexity of the Symbolics 3600, few OEMs would want to tamper with the system's harmony by modifying the essential hardware or software. However, the workstation presents a splendid opportunity for developing sophisticated application software, especially when so few experienced Lisp programmers exist. Prime targets include CAE/CAD, process control, and robotics (e.g., vision systems).



Texas Instruments Nu Machine

Texas Instruments Inc., Data Systems Group, 17881 Cartwright Road, Irvine, Calif. 92714; George White, manager of Nu Machine development, (714) 660-8207.

Whereas most computer systems are designed around a processor, Texas Instruments took a surprising tack by building its Nu Machine around MIT's NuBus, a 32-bit structure that works with a 37.5-Mbyte/s bandwidth. The company views the NuBus as an efficiently controlled "data freeway" over which information travels among processors, memory, mass storage, and remote network nodes. The 10-MHz bus is processor-independent and boasts a memory-mapped architecture that is optimized for 32-bit data, 32-bit addresses and transfers, and multiprocessing.

The backplane accommodates three-high Eurocards, with three 96-pin connectors per board. NuBus occupies only one of those connectors; the other two are free for I/O and subsidiary buses. The versatile backplane also integrates the Multibus, thereby letting designers hang 16-bit Multibus peripherals and faster 32-bit devices on the system. The Multibus works independently of the NuBus, except during cycles that employ both. Some of the actual backplane slots are dedicated to the NuBus, some exclusively to the Multibus, and some to either one.

The 68010 CPU has a 4-kbyte, 45-ns cache memory and hardware for managing memory. Like the NuBus, the computer can work with any appropriate processor and can thus be updated or modified as technology advances. In fact, Lisp Machine Inc., one of the first OEMs to use the Nu Machine, added its own Lisp processor to the 68010-based CPU. (If the 68010 is incorporated, an adaptation of Unix System V, which encompasses virtual

Specifications

Processing elements: A 68010 CPU with a 4-kbyte, 45-ns cache memory and hardware-implemented memory management; OEMs can substitute another CPU.

An 8088-based system diagnostics board contains ROM, 2 kbytes of battery-backed RAM, two serial ports, and an interface for a 1/4-in. streaming tape drive. The board automatically configures system hardware, bootstraps the software, and converts between formats of NuBus and Multibus.

Memory: 500 kbytes of RAM (minimum); additional memory boards hold 500 kbytes or 2 Mbytes, for a total addressable memory of 4 Gbytes. The practical limit depends on the available NuBus slots and the memory boards used—typically 3 to 12 Mbytes for the desktop model, 7 to 28 Mbytes for the rack-mounted version.

Mass storage: An 84- or 169-Mbyte (unformatted) hard disk for the desktop machine, a 474-Mbyte (unformatted) hard disk for the modular version.

A 1/2-in. 20-Mbyte streaming tape cartridge (optional) works at 90 ips, uses a standard DC300XL cartridge, and interfaces with the Nu Machine through the system diagnostics board.

Network: Optional Ethernet interface and support software for both Xerox Network Systems and TCP/IP protocols.

Backplane: 12 slots for desktop model—6 for the NuBus, 3 for the Multibus, and 3 hybrid; 21 slots for the rack-mounted version—13 for the NuBus, 5 for the Multibus, and 3 hybrid (one hybrid slot is always reserved for interbus communications).

Ports: Two RS-232-C serial lines on diagnostics board.

Graphics: An 800-by-1024-pixel monochromatic 15-in. screen with 60-Hz noninterlaced refreshing, keyboard, and mouse.

Operating system: Adaptation of Unix System V with languages, utilities, and editors; enhanced for windowing.

Programming languages: Unix System V's standard Fortran, Pascal, and C.

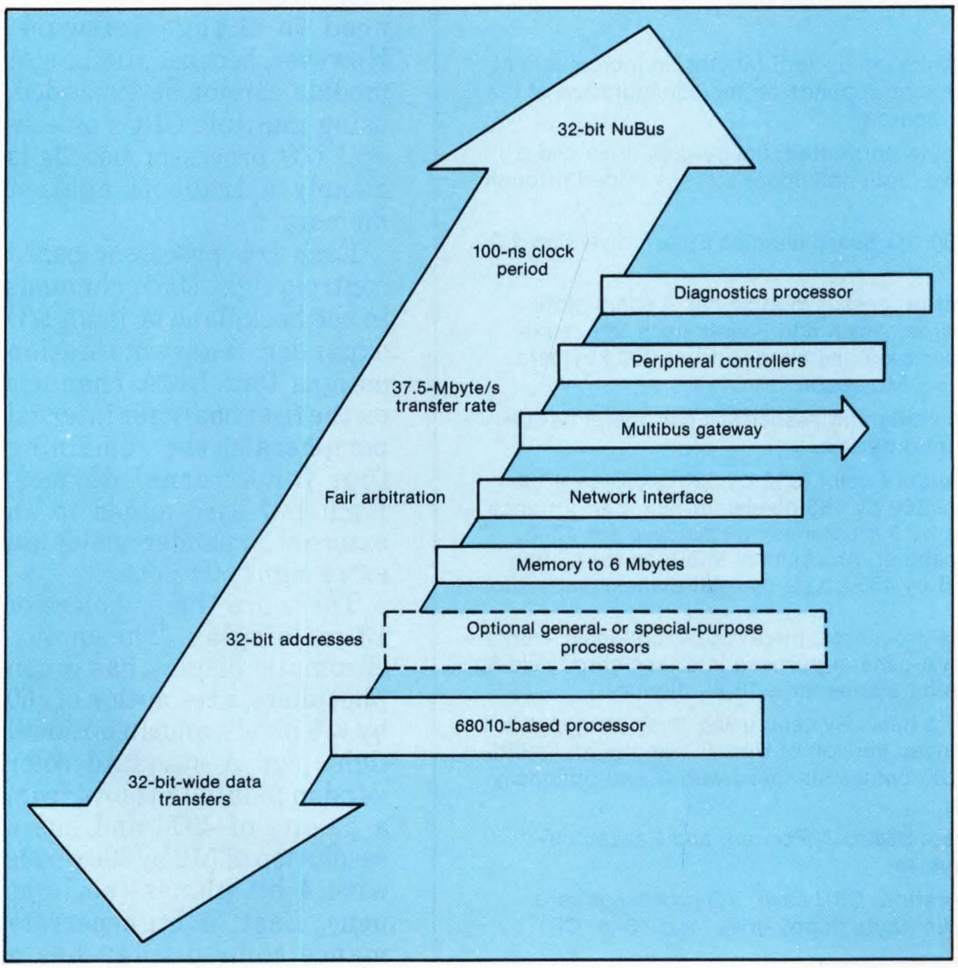
Minimum OEM configuration: Power supply, card cage, disk controller and drive, and system diagnostics board (no CPU required in minimum system).

memory, can be used.) The architecture is particularly valuable when a team of engineers is sharing one data base: Each member can have a different CPU in his or her terminal and access the large data base over the NuBus, which can be considered a superfast local network.

An 8088-based system diagnostics unit plugs into the NuBus and can be activated remotely or locally to test the bus, board, and system. The unit is responsible for translating the format of one bus into the format of the other, allowing masters on either the NuBus or the Multibus to access slaves on the other bus.

The workstation's high-resolution 15-in. monochromatic graphics subsystem is equipped with a low-profile keyboard and a mouse cursor.

The computer is configured as a compact desktop machine or as a rack-mounted module. The former is fitted with a 12-slot chassis and a controller for an 84- or 169-Mbvte hard-disk drive (unformatted). The modular version uses a standard single-bay 19-in. EIA rack and has a 21-slot card cage and a 474-Mbyte hard disk. The minimum OEM configuration requires no CPU, proving that the Nu Machine's architecture is truly independent of processor technology. Memory comes in 500-kbyte boards with error checking and correction or in 200-Mbyte cards with parity checking; total capacity is limited only by the number of available NuBus slots.



Hewlett-Packard HP 9000, Model 520

Hewlett-Packard Co., Fort Collins Systems Division, 3404 East Harmony Road, Fort Collins, Colo. 80525; John Hettrick, OEM manager, (303) 226-3800.

Like the other microcomputers in the HP 9000 family's 500 series, the Model 520 desktop workstation is based on a proprietary 32-bit microprocessor chip that gives it the number-crunching power and speed required for engineering and scientific applications. In addition, its value can be enhanced with HP's numerous I/O, peripheral, and software options.

At the heart of the workstation is a 12-slot memory and processor module that holds the CPU, RAM, and I/O processor boards. Each system can be configured with as many as 3 CPUs, 3 I/O processors, and 10 memory cards of 512 kbytes of RAM (up to 5 Mbytes). Two CPUs can raise the speed of the multitasking system by a factor of 1.9, three CPUs by a factor of 2.9. Adding CPUs is simply a matter of plugging in the extra boards. The operating system automatically adjusts to the situation, with no need to change software. However, because the 12-slot module cannot be expanded, using multiple CPUs or several I/O processor boards is clearly a tradeoff against memory.

Each I/O processor board controls eight DMA channels in the backplane or in an I/O expander. The workstation assigns four DMA channels on the first board for internal peripherals, the remaining four for external devices. Each I/O card added to an external expander yields an extra eight I/O slots.

There are three choices of 13-in. display. The monochromatic display has green phosphors, a resolution of 560 by 455 pixels, and an optional light pen. A standard color version paints 16 colors from a palette of 4096 and has a resolution of 512 by 390 pixels with 4 bit planes (no light pen). Last, a high-performance color display has a

Specifications

Processing elements: A proprietary 32-bit CPU with an 18-MHz clock rate and a microinstruction cycle time of 55 ns; up to three CPUs per workstation.

Memory: 512 kbytes (minimum) up to 5 Mbytes, in increments of 512 kbytes (the total amount depends on the configuration of the CPU and I/O processor boards).

Mass storage: A 264-kbyte (formatted) floppy-disk drive and a 10-Mbyte fixed-disk drive (optional); more storage added through I/O slots.

Network: HP's LAN 9000 I/O board handles Ethernet version 1.0 protocol under HP-UX.

Backplane: Memory and processor module has 4 spare slots without I/O expander cards, which add 8 slots each to a maximum of 16. I/O processor card has bandwidth of 960 kbytes/s (for one channel) up to 5.5 Mbytes/s.

Ports: Various interface cards and associated peripheral devices available from HP and third parties.

Graphics: Choice of standard color (512 by 390 pixels by 4 bit planes), monochromatic (560 by 455 pixels), or high-performance color (560 by 455 pixels by 3 bit planes); all displays are 13 in. and built into desktop cabinet. An optional interface for a 19-in. color video monitor (576 by 455 pixels by 4 bit planes) plugs into the backplane.

An intelligent graphics processor, the 97060A, optionally works with the system through a general-purpose interface card, yielding 1024 by 768 pixels by 8 bit planes for a 19-in. monitor.

Operating systems: HP's Basic System, using Basic language for single users; HP's enhanced version of Unix for single- and multiple-users, dubbed HP-UX, comes standard with C and optionally with Fortran and Pascal.

Programming languages: Basic, C, Fortran, and Pascal, depending on operating system.

Minimum OEM configuration: CPU card, I/O processor card, 512-kbyte RAM card, 264-kbyte floppy drive, and 13-in. CRT.

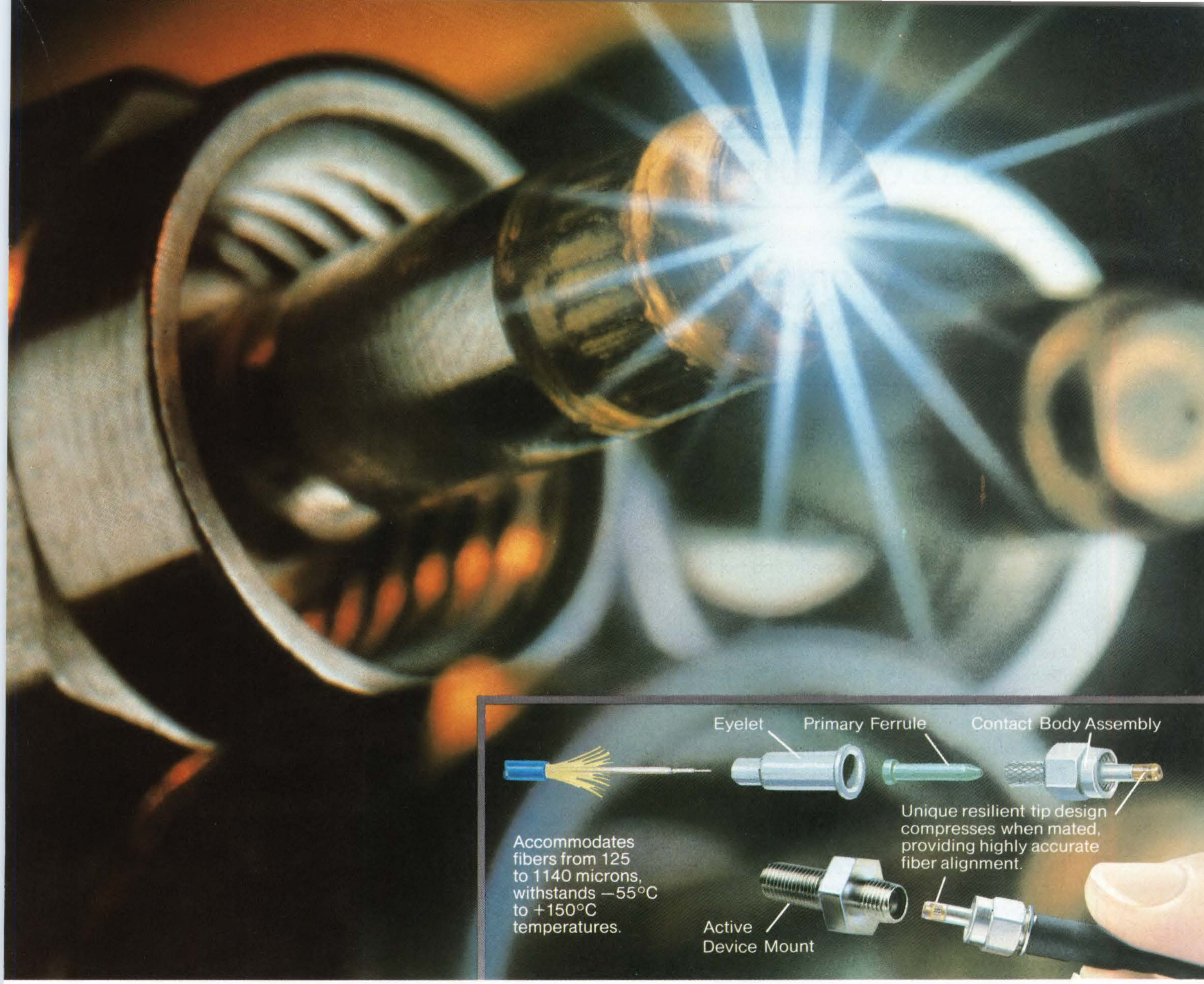
HP 9000, Model 520

resolution of 560 by 455 pixels by 3 bit planes, a dithered palette of 4201 colors (of which 8 are true and the remaining ones are created by dithering), and an optional light pen.

The basic workstation is configured with a 264-kbyte floppy-disk drive a 10-Mbyte hard disk, thermal printer, and light pen can be optionally integrated.

When HP's assorted I/O interface cards are combined with the workstation's I/O processor boards, they conform to an HP standard that is independent of the host and can be used in future HP computers. Among the I/O cards are the HP-IB, which ties into the IEEE-488-1978 bus; a general-purpose I/O card that handles 8- or 16-bit parallel communication with DMA; a single-channel asynchronous serial port; an asynchronous eight-channel multiplexer; and the LAN 9000, a network card that supplies bundled hardware and software for an Ethernet link; and a remote-job-entry card that helps emulate IBM 2780 and 3780 terminals.

The Model 520 runs under one of three operating systems. HP's own single-user Basic System uses the Basic language. The machine operates under single- and multiple-user versions of HP-UX, an enhanced version of Unix that runs C as the standard language and can also accommodate Fortran 77 and Pascal.



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CIRCLE NUMBER 40

AMP means productivity.

Masscomp WorkStation-500

Masscomp, 1 Technology Park, Westford, Mass. 01886; Ed Marcato, OEM marketing manager, (617) 692-6200.

Specifications

Processing elements: A 10-MHz 68010 CPU and a 10-MHz 68000, the latter handling page faults in virtual memory while the former executes another program. The CPU has a 4-kbyte cache, a 1024-element translation buffer, a 1024-entry I/O map, and three serial lines.

An optional FP-501 floating point processor performs single- and double-precision arithmetic and holds 16 sets of 32 double-precision (64-bit) registers.

An optional AP-501 array processor executes single- and double-precision floating-point vectors, locally stores 32-bit elements, incorporates a 68000 that moves data to and from virtual memory, and requires the FP-510 for double-precision tasks.

Memory: 1 Mbyte (Minimum), 6 Mbytes (maximum); up to 16 Mbytes of virtual memory per process.

Mass storage: A 1-Mbyte floppy-disk drive, a 40-Mbyte (formatted) Winchester disk drive, and a 45-Mbyte ¼-in. tape cartridge (all optional).

Network: An optional plug-in Ethernet controller and supporting software.

Backplane: 8-slot enhanced Multibus with transfer rate of 6 Mbytes/s; eight alphanumerical terminals can be attached through backplane.

Ports: Three serial lines through CPU.

Graphics: Two 19-in. terminals (optional) attached through Multibus, each with its own 68000 and 128-kbyte program storage. The monochrome version displays 1024 by 800 pixels, the color unit 832 by 600 pixels by 6 or 10 bit planes. Each has 60-Hz noninterlaced refreshing and a 117-element keyboard; a mouse (or puck) and tablet are optional.

Operating system: The real-time RTU with virtual memory is compatible with the source code of Unix System III and of Berkeley 4.2 Unix and includes communications, text-processing, and support utilities; editors; source-code control system; and Bourne and C shells.

Programming languages: Fortran 77, C, and Pascal.

Minimum OEM configuration: CPU, power supply, 1 Mbyte of RAM, 8-slot backplane, and cabinet.

In designing its minicomputer-strength, multitasking workstation, Masscomp kept OEMs as a primary target. Both the hardware and the software in the WorkStation-500 are assembled with industry-standard components, making the machine's architecture highly accessible. Depending on the purpose, the computer can be configured in many ways from a large selection of components. In addition, OEMs should find the WorkStation-500 a powerful companion for developing Unix-based applications and adding Multibus peripherals.

Key to the workstation's power are its multiple processors. The 68010 CPU, running at 10 MHz, works with a 10-MHz 68000, which handles page faults in virtual memory. The private 500-Series bus connects the CPU to separate single- and double-precision floating-point and array processors. The floating-point device can complete a single-precision addition or multiplication in 1.6 μs. The array processor tackles a 1024-point arithmetical operation in 240 μs.

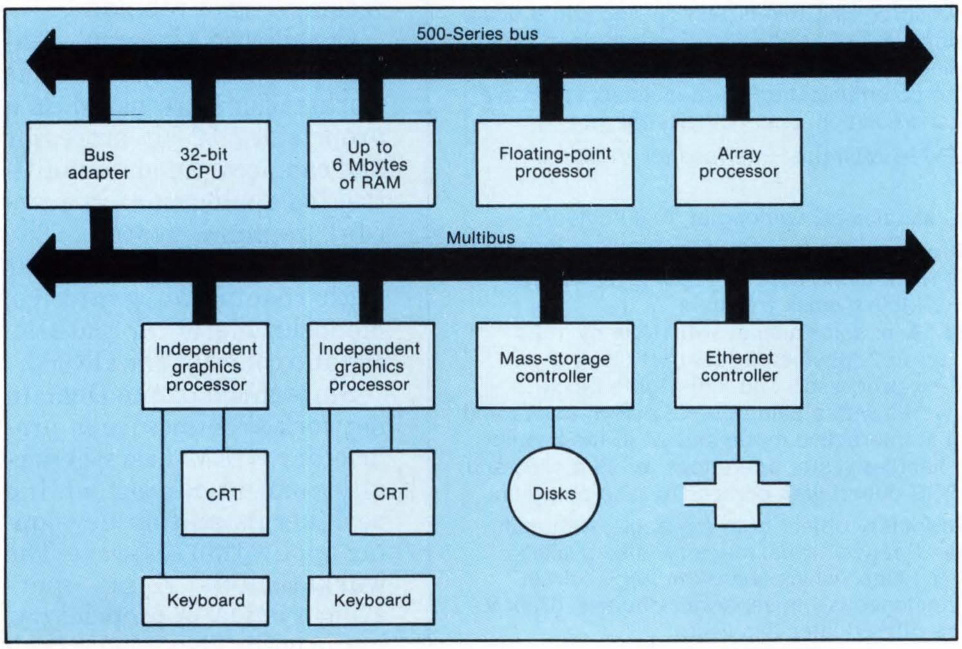
Added power comes from high-resolution graphics terminals (one or two per station), each of which contains an independent 68000 that stores programs in 128 kbytes of local storage.

An enhanced Multibus with an 8-slot backplane handles 6 Mbytes/s—twice as many 16-bit data transfers as the normal Multibus can perform. The WorkStation-500's distributed computational power can accommodate up to 10 users with no degradation in response. In addition to the two independent graphics terminals, up to eight alphanumerical terminals can be multiplexed through the Multibus backplane.

The computer can address 16 Mbytes of virtual memory for each process; RAM starts at 1 Mbyte and goes up to 6 Mbytes. OEMs can add a 1-Mbyte floppy-disk drive and a 40-Mbyte (formatted) Winchester drive that uses a 1/4-in. tape cartridge as backup.

Masscomp's real-time, virtual memory RTU operating system also meets industry standards. Its source code is compatible with that of both Bell Laboratories' Unix System III and Berkeley 4.2. The overall software includes Bourne and C shells; most Unix and Berkeley utilities and editors; and Fortran 77, C, and Pascal-2. The company has enhanced Unix with windowing and the Quick-Choice user interface.

The workstation can be tied into an Ethernet network that employs the TCP/IP protocol. When connected with other Unix-based systems in the 10-Mbit/s network, proprietary software can handle intertask communication, remote file transfers, virtual terminals, printing spools, and electronic mail.



Apollo DN460 and DN660

Apollo Computer Inc., 15 Elizabeth Drive, Chelmsford, Mass. 01824; (617) 256-6600.

Specifications

Processing elements: A proprietary 32-bit-slice processor with a bipolar 4-kbyte instruction cache and a bipolar 16-kbyte data cache, an integral floating-point processor for single- and double-precision arithmetic, and a three-stage instruction pipeline.

Memory: 1 Mbyte of ECC RAM (standard), expandable to 4 Mbytes; 256 Mbytes of virtual memory per process for up to 24 concurrent processes. The Domain network manages virtual memory.

Mass storage: Various combinations of 68-, 158-, and 300-Mbyte Winchester disk drives, spread throughout network or attached to individual workstations. 1.2-Mbyte diskettes and ½-in. 1600-bpi magnetic tape drive are accommodated.

Network: Proprietary 12-Mbyte/s Domain, a baseband network using a continuously synchronizing token-passing ring and a dual-address packet with single-token arbitration. Several thousand nodes can share one network, with each active node separated by as much as 1 km. Other communications protocols accepted are X.25, IBM 3270 terminal emulation, and TCP/IP Ethernet.

Backplane: 5-slot IEEE-796 Multibus; interface for Versatec printer-plotter.

Ports: Three RS-232-C serial lines, working at 19.2 kbytes/s.

Graphics: DN460—bit-mapped 19-in. monochromatic display with 1024 by 800 pixels, 60-Hz noninterlaced refreshing, 128-kbyte display memory, and 32-Mbit/s block transfers.

DN660—bit-mapped 19-in. color display with 1024 by 1024 pixels by 8 bit planes, up to 2 Mbytes of dual-port display memory, dedicated 16-bit processor, and 320-Mbit/s block transfers. The display works with a palette of 16 million colors and 4 or 8 color planes in the interactive mode and 24 in the imaging mode. The subsystem handles raster operations for all planes and produces an RS-343 RGB output with composite sync on green.

Operating system: Proprietary object-oriented Aegis, with multiple windows and demand-paged virtual memory. Also available are AUX and Berkeley 4.1 Unix, which share the Aegis kernel. All systems can run simultaneously in separate windows. (Unix V and Berkeley 4.2 will be offered later this year.)

Programming languages: ANSI Fortran 77 with extensions, C, and ISO Pascal with extensions.

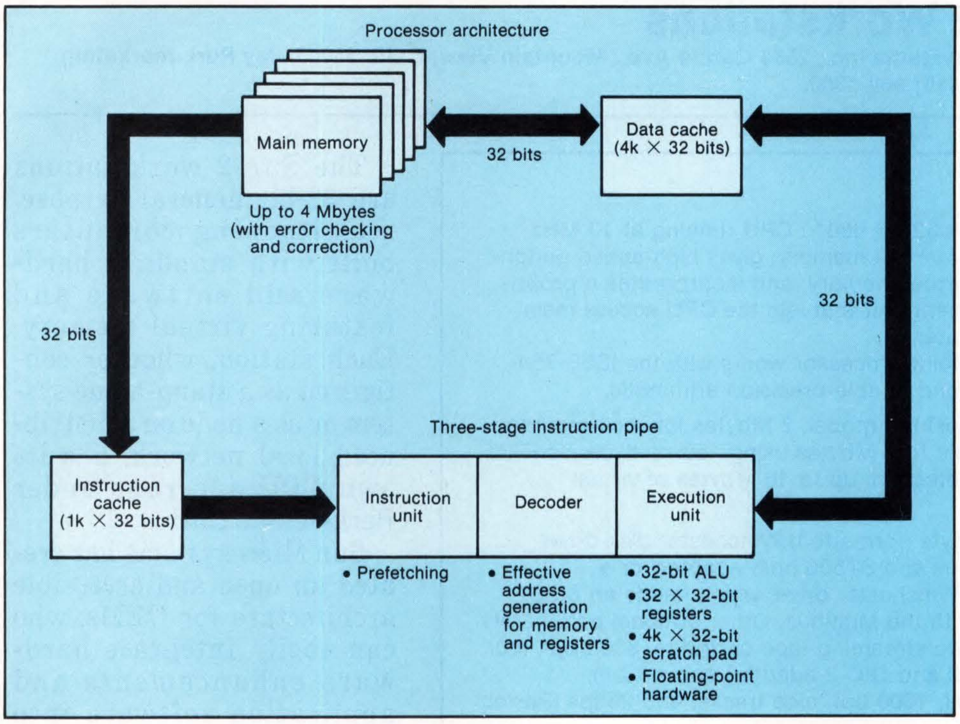
Minimum OEM configuration: Complete workstation without disk drives.

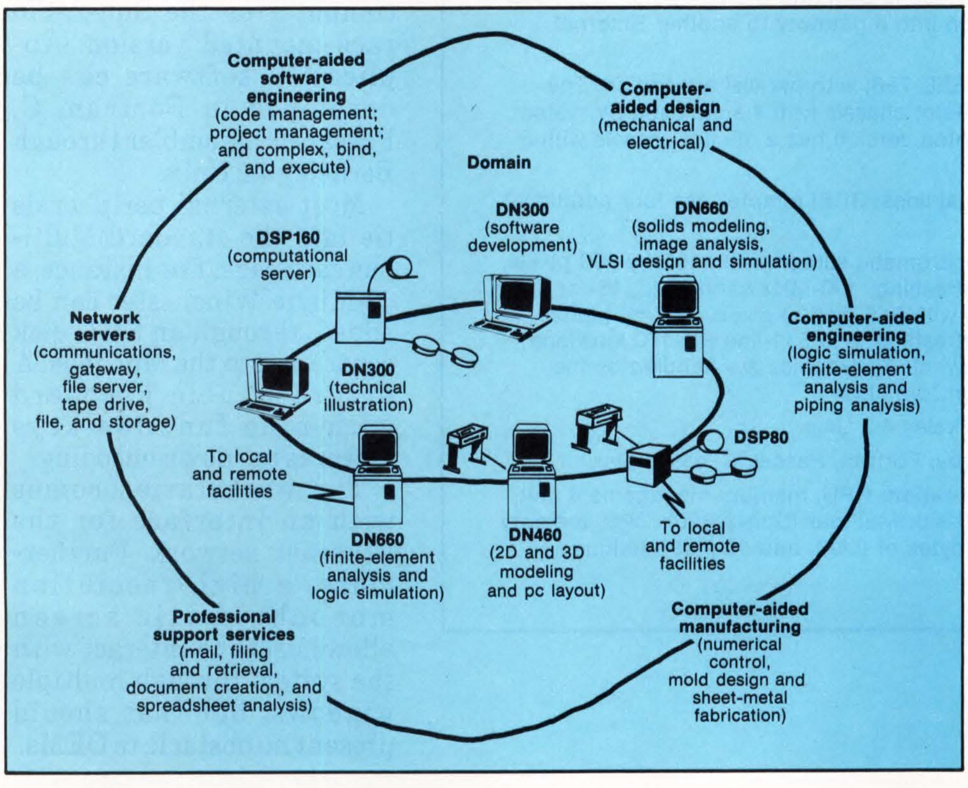
Although the DN460 and DN660 workstations can be configured as stand-alone systems, their hardware and software reach their full potential when using the memory and computational power of Apollo's distributed network, called Domain. The network gives users access to all resources, including extra nodes. Moreover, programs can run on any node without recompiling or rebinding.

Considered powerful general-purpose computers, the workstations are based on a proprietary 32-bit processor and can accommodate multitasking applications in a virtual memory system. The workstations differ in their high-resolution graphics, monochromatic for the DN-460 and color for the DN660.

Since much of the Domain network architecture is proprietary, OEM users generally concentrate on adding peripherals and on developing application software. The workstations' Aegis operating system is proprietary, but Apollo also offers both Berkeley 4.1 Unix and the AUX version of Unix III with all their usual utilities.

Both of those commercial operating systems have the same kernel as Aegis and can run simultaneously with Aegis in separate windows.


Processor architecture
Main memory
Up to 4 Mbytes (with error checking and correction)
32 bits
Data cache (4k × 32 bits)
32 bits
32 bits
Three-stage instruction pipe
Instruction cache (1k × 32 bits)
Instruction unit
Decoder
Execution unit
• Prefetching
• Effective address generation for memory and registers
• 32-bit ALU
• 32 × 32-bit registers
• 4k × 32-bit scratch pad
• Floating-point hardware


Computer-aided software engineering (code management; project management; and complex, bind, and execute)
Computer-aided design (mechanical and electrical)
Domain
DN300 (software development)
DN660 (solids modeling, image analysis, VLSI design and simulation)
DSP160 (computational server)
Network servers (communications, gateway, file server, tape drive, file, and storage)
Computer-aided engineering (logic simulation, finite-element analysis and piping analysis)
DN300 (technical illustration)
DSP80
To local and remote facilities
DN660 (finite-element analysis and logic simulation)
DN460 (2D and 3D modeling and pc layout)
To local and remote facilities
Professional support services (mail, filing and retrieval, document creation, and spreadsheet analysis)
Computer-aided manufacturing (numerical control, mold design and sheet-metal fabrication)

Sun-2 Workstations

Sun Microsystems Inc., 2550 Garcia Ave., Mountain View, Calif. 94043; Jay Puri, marketing manager, (415) 960-1300.

Specifications

Processing elements: A 32-bit 68010 CPU running at 10 MHz translates addresses for virtual memory; gives high-speed peripherals direct access to virtual memory; and incorporates a proprietary memory management unit that lets the CPU access main memory without wait states.

An optional floating-point processor works with the IEEE-754 data format for single- and double-precision arithmetic.

Memory: 1 Mbyte for desktop model, 2 Mbytes for rack-mounted computer, all expandable to 4 Mbytes using 150-ns dynamic RAM with byte-parity error detection; up to 16 Mbytes of virtual memory per process.

Mass storage: A 42-Mbyte (formatted) Winchester disk drive, which needs an SCSI bus and ST506 host adapter, or a 130-Mbyte (formatted) Winchester drive, which needs an SMD controller to hook up with the Multibus. Other optional peripherals include a 1/4-in. 20-Mbyte streaming tape cartridge, 8000 bpi, four tracks, and 90 ips (SCSI and QIC-2 adapter) and a 1/2-in. 45-Mbyte start/stop reel, 1600 bpi, nine tracks, and 25 ips (Partec interface).

Network: Ethernet interface is built into the computer; a second can turn the workstation into a gateway to another Ethernet system.

Backplane: Multibus (IEEE-796) with parallel arbitration. The desktop model has a 9-slot chassis with 4 slots used by system, whereas the rack-mounted version has a 15-slot chassis with 5 used by system.

Ports: Two RS-423 serial lines; SCSI adapter has four additional RS-423 ports.

Graphics: 19-in. monochromatic screen with 1152 by 900 pixels, 70-Hz noninterlaced refreshing, 100-MHz bandwidth; 13- or 19-in. color display (optional) with 640 by 480 pixels by 8 bit planes, 60-Hz noninterlaced refreshing, and 511-line RS-170 interface (red, green, blue, and sync). All graphics are handled by the device-independent SunCore library.

Operating system: Berkeley 4.2 Unix.

Programming languages: Fortran, Pascal, C, assembler.

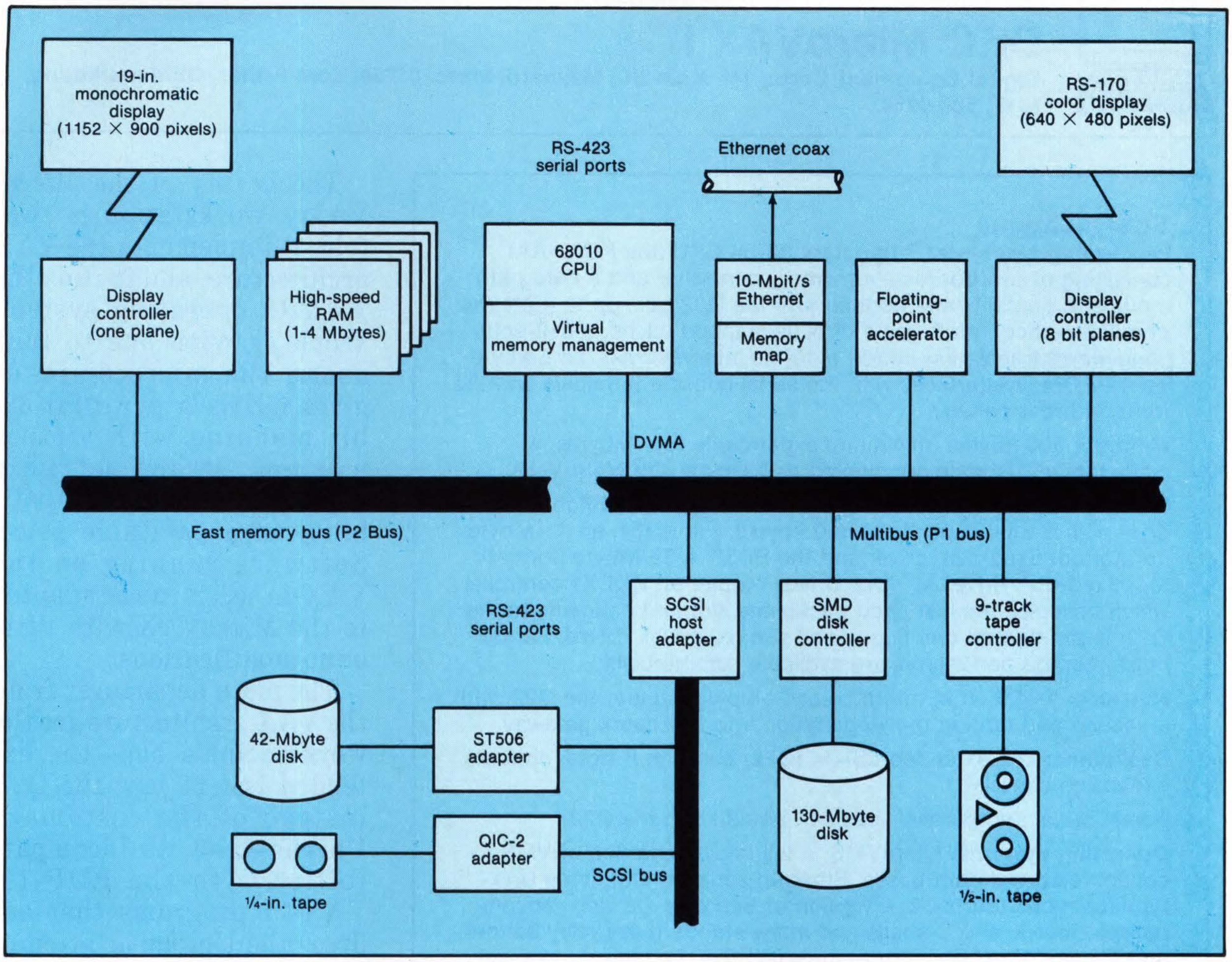
Minimum OEM configuration: CPU, memory management unit, 1 Mbyte of RAM, and 9-slot Multibus (Sun-2/120); CPU, memory management unit, 2 Mbytes of RAM, and 15-slot Multibus (Sun-2/170).

The Sun-2 workstations are 32-bit general-purpose, multitasking computers built with standard hardware and software and featuring virtual memory. Each station, whether configured as a stand-alone system or as a node on a distributed local network, has its own CPU and runs under Berkeley 4.2 Unix.

Sun Microsystems has created an open and accessible architecture for OEMs, who can easily integrate hardware enhancements and application software into the Sun-2/120 desktop computer or the Sun-2/170 rack-mounted version. Application software can be developed in Fortran, C, Pascal, or assembler through Berkeley 4.2 Unix.

Most external peripherals tie into the standard Multibus card cage. For instance, a 42-Mbyte Winchester can be added, through an SMD disk controller, to the Multibus. A programmable keyboard with nine function keys features up/down encoding.

The workstation comes with an interface for the Ethernet network. Furthermore, a high-resolution monochromatic screen allows users to interact with the system through multiple windows, but that should present no obstacle to OEMs.


19-in. monochromatic display (1152 × 900 pixels)
RS-423 serial ports
Ethernet coax
RS-170 color display (640 × 480 pixels)
Display controller (one plane)
High-speed RAM (1-4 Mbytes)
68010 CPU
Virtual memory management
10-Mbit/s Ethernet
Memory map
Floating-point accelerator
Display controller (8 bit planes)
DVMA
Fast memory bus (P2 Bus)
Multibus (P1 bus)
RS-423 serial ports
SCSI host adapter
SMD disk controller
9-track tape controller
42-Mbyte disk
ST506 adapter
130-Mbyte disk
QIC-2 adapter
SCSI bus
¼-in. tape
½-in. tape

DEC MicroVAX I

Digital Equipment Corp., 146 Main St., Maynard, Mass. 01754; Tom Fisher, OEM marketing, (617) 568-6264.

Specifications

Processing elements: Proprietary 32-bit CPU (the KD32-AA) consisting of two boards—a memory controller and a data path module. It contains an interface with the Q22 bus, up to 4 Mbytes of main memory, an 8-kbyte directly mapped cache, a 512-entry (long-word) translation buffer, a 10-ms interval timer, an 8-kbyte boot PROM; it interfaces with the serial console terminals and the front and rear panels.

Memory: 500 kbytes (minimum) expandable to 4 Mbytes; 4 Gbytes of virtual memory (limited to 1 Gbyte with MicroVMS).

Mass storage: The RX50, a dual 5¼-in. single-sided floppy-disk drive with a total capacity of 800 kbytes; the RD51, an 11-Mbyte (formatted) fixed-disk drive; and the RD52, a 32-Mbyte (formatted) fixed-disk drive. All three drives require an RQDX1 controller, which occupies the last-used backplane slot and connects to the Q22; it can control one floppy and two fixed disk drives. Larger mass-storage peripherals are available commercially.

Network: An Ethernet interface can be plugged into the Q22, with a second one turning the workstation into a network gateway.

Backplane: The extended LSI-11 (Q22) bus with 8 slots; optional expansion chassis.

Ports: Serial and parallel lines can be tied into the Q22.

Operating systems: MicroVMS, a full implementation of VMS, covers relational data bases, Ethernet support, and some Unix-type functions. Ultrix-32, a version of Berkeley 4.2 Unix, encompasses Bourne and C shells and many standard Berkeley editors and utilities. VAXElan, a run-time executive, handles concurrent CPUs in a local network or multiprocessor system.

Programming languages: For MicroVMS—Fortran, Pascal, and C; for Ultrix-32—Fortran, Pascal, C, Franz Lisp, and Unix assembler; for VAXElan software—tools run under VMS and include an optimizing Pascal compiler and a symbolic Pascal debugger.

Minimum OEM configuration: CPU, cabinet, power supply, 500 kbytes of RAM, and a Q22 bus interface.

The beauty of the MicroVAX I workstation is twofold: it implements the VAX architecture, and it runs the VAX-11 operating system. Working with one to four users, the microcomputer gives OEMs a powerful 32-bit machine with virtual memory, strong software support, and VAX compatibility at a palatable price. Software running on the VAX-11 series can be adapted to the MicroVAX with little or no modifications.

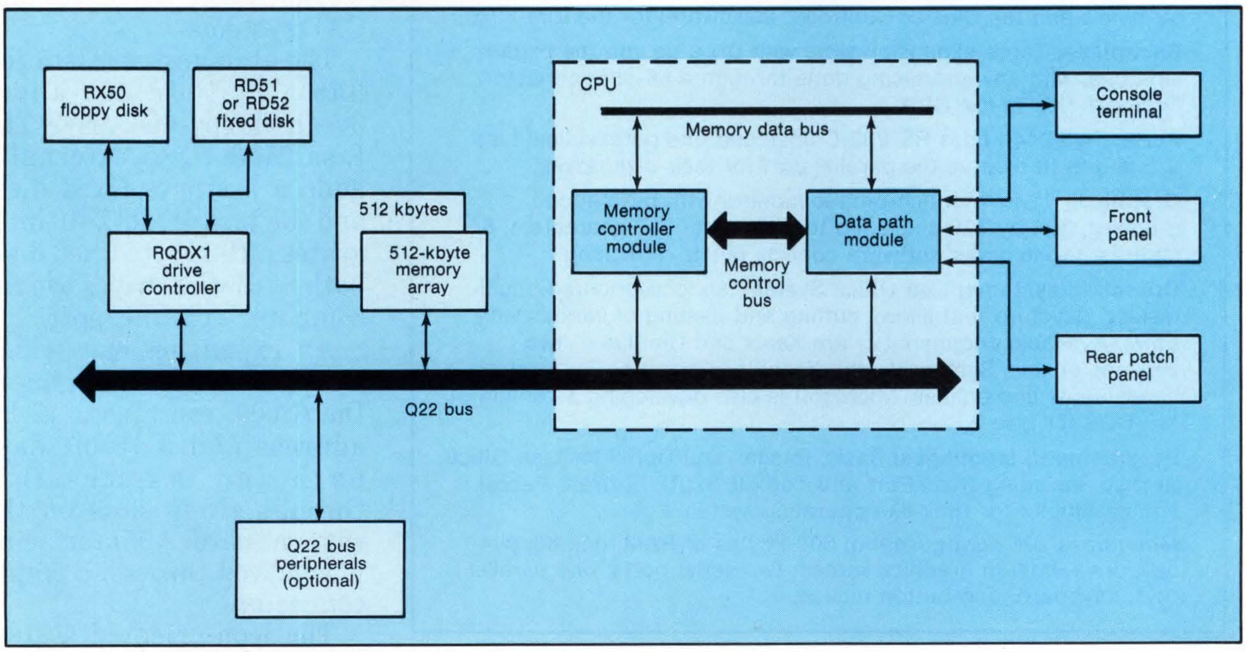
The main departures from the VAX architecture are the workstation's bus—the extended LSI-11 bus, the Q22, instead of the customary Unibus—and its incompatibility with the PDP-11. VAX-11 programs that address the Unibus or attempt to execute PDP-11 instructions must be modified before running on the MicroVAX I. Otherwise, the workstation accepts the complete set of VAX-11 instructions, with some emulated in software.

The 32-bit CPU, comprising two boards, works with 32-bit internal data paths and transfers. The data path communicates directly with VT100 or VT200 terminals, the front panel, and a rear patch panel (for serial lines and option cables). Main memory, mass storage, and other peripherals exchange data over the Q22 bus, which has 22-bit addressing, uses a 16-bit data path, and transfers information at 3.3 Mbytes/s. Physical addresses can be 23 bits long, with the system handling up to 4 Mbytes of physical memory.

The MicroVAX I runs under three operating systems. MicroVMS is a full implementation of DEC's VMS, which is used on VAX-11 computers. (All VMS software not using system-specific privileged instructions can be adapted to MicroVMS.) The Ultrix-32 operating system, which is the company's version of Berkeley 4.2 VM/Unix, affords an open-ended portable structure. The third, VAXElan, is a run-time executive for real-time, on-line, and stand-alone tasks that do not require a full operating system. It works with truly concurrent CPUs in a local network or multiprocessor environment for dedicated applications.

The workstation's architecture makes provisions for 32-bit virtual address space, for a total of 4 Gbytes. The MicroVMS operating system, however, limits the virtual space to 1 Gbyte, though Ultrix-32 could handle that capacity if other factors allow it.

DEC has not yet developed a graphics package for MicroVAX I, making that a natural area for OEM involvement. The system itself is designed primarily for OEMs and can be obtained in a bare minimum configuration.



Apple Lisa 2

Apple Computer Inc., 20525 Mariani Ave., Cupertino, Calif. 95014; Matt Slavik, OEM department, (408) 996-1010.

Specifications

Processing elements: A 68000 CPU, with a 32-bit internal and a 16-bit external data path, runs at 5 MHz with an 800-ns cycle time. A board slot is provided for an optional floating-point math coprocessor.

Memory: 500 kbytes (minimum) expandable to 1 Mbyte through a 500-kbyte expansion board.

Mass storage: One 400-kbyte floppy-disk drive (minimum), a 5-Mbyte external fixed disk for Lisa 2/5 (optional), and a 10-Mbyte internal fixed disk for Lisa 2/10 (optional).

Network: Various local network software packages will become available commercially. Apple supplies two terminal emulation packages—LisaTerminal (software) for the VT100, VT52, and TTY terminals and the Cluster Controller (hardware) for the IBM 3270.

Backplane: Three expansion slots with DMA tie into the expansion bus, with any interfacing done through a 56-pin connector. Timing is tied to the CPU.

Ports: Two 244-kbit/s RS-232-C lines and one parallel line; Lisa 2/5 and 2/10 reserve the parallel port for their disk drives.

Graphics: 12-in. monochromatic monitor with bit-mapped graphics, 364 by 720 pixels, up to 40 lines of 132 characters, 64 contrast levels under software control, 60-Hz refreshing.

Operating systems: Lisa Office System, an icon-oriented, multitasking structure that allows cutting and pasting of various windows. Available commercially are Xenix and UniPlus+, two versions of Unix System V, with Xenix incorporating Berkeley enhancements and utilities. Microsoft is also developing a version of MS-DOS for Lisa 2.

Programming languages: Basic, Pascal, and Cobol for Lisa Office System, including QuickPort and ToolKit/32; C, Fortran, Pascal, and assembler for Unix-like operating systems.

Minimum OEM configuration: 500 kbytes of RAM, one floppy-disk drive, built-in graphics screen, two serial ports, one parallel port, keyboard, one-button mouse.

Apple's Lisa introduced the user community to a degree of power and sophistication previously unknown in desktop personal workstations, largely because of its 68000 CPU, which runs at 5 MHz. Given its powerful features (including graphics and a one-button mouse cursor) and its low price, many OEMs find it an attractive workstation for CAE and CAD systems.

The standard workstation has a built-in 400-kbyte 3½-in. floppy-disk drive. The Lisa Model 2/5 externally adds a 5-Mbyte fixed disk, and the Lisa Model 2/10 integrates a 10-Mbyte fixed disk; both hard-disk drives use the computer's parallel port.

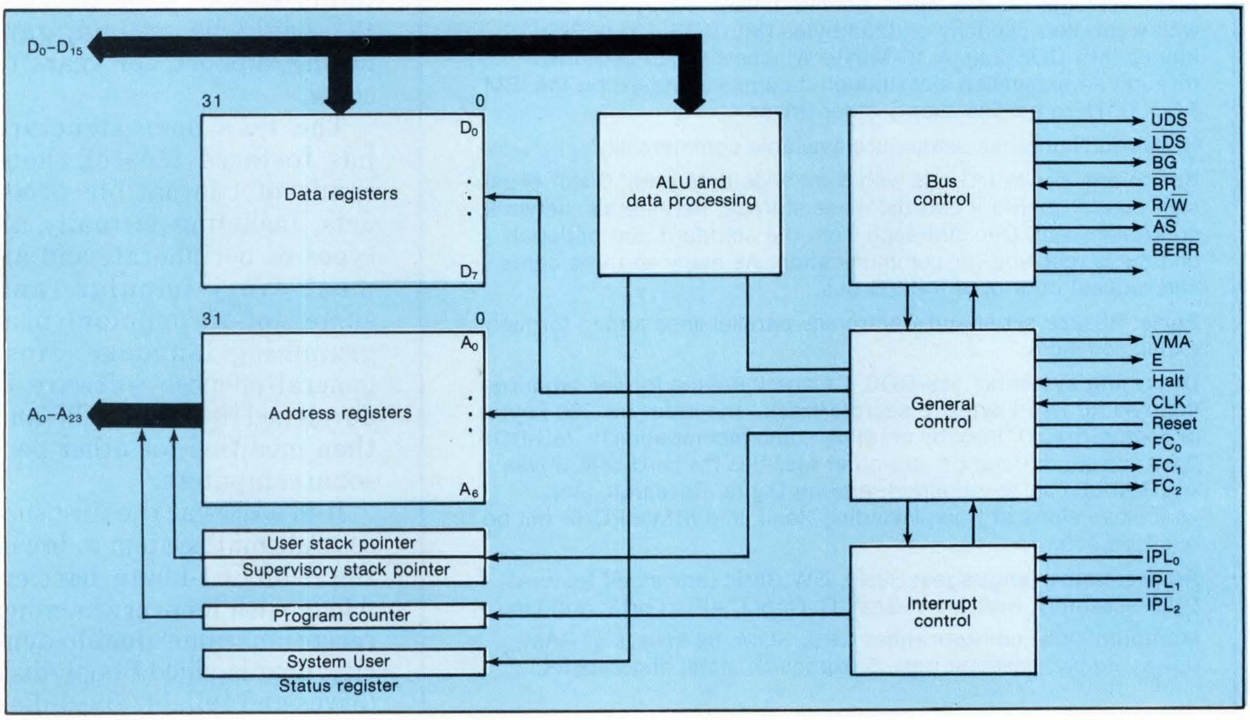
An expansion bus, which closely follows the timing of the 68000, contains a 12-bit address and a 16-bit data path and is accessible through three slots on the system board. All interfacing is achieved through a 56-pin connector.

The icon-oriented system software supplied by Apple is called the Lisa Office System, which lets the user select operations and files—via the mouse—from a screen display that employs images, or icons. Multitasking and windowing facilitate cutting and pasting of applications and files.

Application software can be developed in Basic, Pascal, and Cobol, each of which has a related set of tools—dubbed QuickPort—that adapts existing programs to the Lisa 2. For instance, ToolKit/32 provides the tools needed to incorporate Lisa features into OEM applications. Lisa-Terminal emulates VT100, VT52, and TTY terminals, while Apple's Cluster Controller enables Lisa 2 to emulate an IBM 3270 through hardware. Beyond that, the computer can run all Macintosh programs.

Third-party suppliers have created two versions of Unix, Xenix and UniPlus+, which support the multiple-user multitasking capabilities of standard Unix but cannot handle the display windows that make Lisa popular (though Xenix can use the mouse occasionally).

Since no partitioning is used, one disk cannot store programs and data simultaneously for either Unix system and the Lisa Office System; instead the user must commit the disk to one or the other. Partitioning may be possible in the future. The Unix environments support Fortran, C, and assembly, and many Unix-based application programs can be adapted with little difficulty.



IBM PC

IBM Corp., Entry Systems Division, 1000 N.W. 51st St., Boca Raton, Fla. 33432; (305) 998-6048.

Specifications

Processing elements: An 8088 CPU, with 16-bit internal and 8-bit external data paths, runs at 4.77 MHz and uses 20-bit addressing, for 1 Mbyte of space. Its four 20-bit DMA channels complete data transfers in 1.05 μs. Rounding out the CPU circuitry are three 16-bit timer-counter channels. An 8087 floating-point math coprocessor is optional.

Memory: 64 kbytes of RAM minimum, 256 kbytes maximum on board, 640 kbytes maximum through expansion slots.

Mass storage: Double-sided, double-density floppy-disk drives with formatted capacity of 320 kbytes (MS-DOS 1.x) or 360 kbytes (MS-DOS 2.x). A 10-Mbyte Winchester can be added through an expansion slot (though it comes standard on the IBM PC XT). Third parties supply other drives.

Network: Numerous setups are available commercially.

Backplane: 5-slot I/O bus with 8-bit-wide data path; 8-slot expansion bus for memory boards, mass storage, peripherals, network controllers, etc. One slot each from the standard and optional chassis is reserved for communication. As many as three cards can request control of the I/O bus.

Ports: RS-232 serial and Centronics parallel lines added through expansion slots.

Operating systems: MS-DOS 1.1 and 2.0—the former organizes floppies for 320 kbytes (8 sectors/track), the latter for 360 kbytes (9 sectors/track), thereby creating some incompatibility. MS-DOS 2.0 adds subdirectories and other facilities for hard-disk drives.

CP/M-86 can be obtained through Digital Research, and various versions of Unix, including Xenix and IBM's PC/IX will be released soon.

Programming languages: Basic, GW Basic (advanced features), 8088 assembly, Fortran, Pascal, C, Cobol, APL, Forth, and Lisp.

Minimum OEM configuration: CPU, ROM, 64 kbytes of RAM, power supply, cassette port, 5 expansion slots, and cabinet.

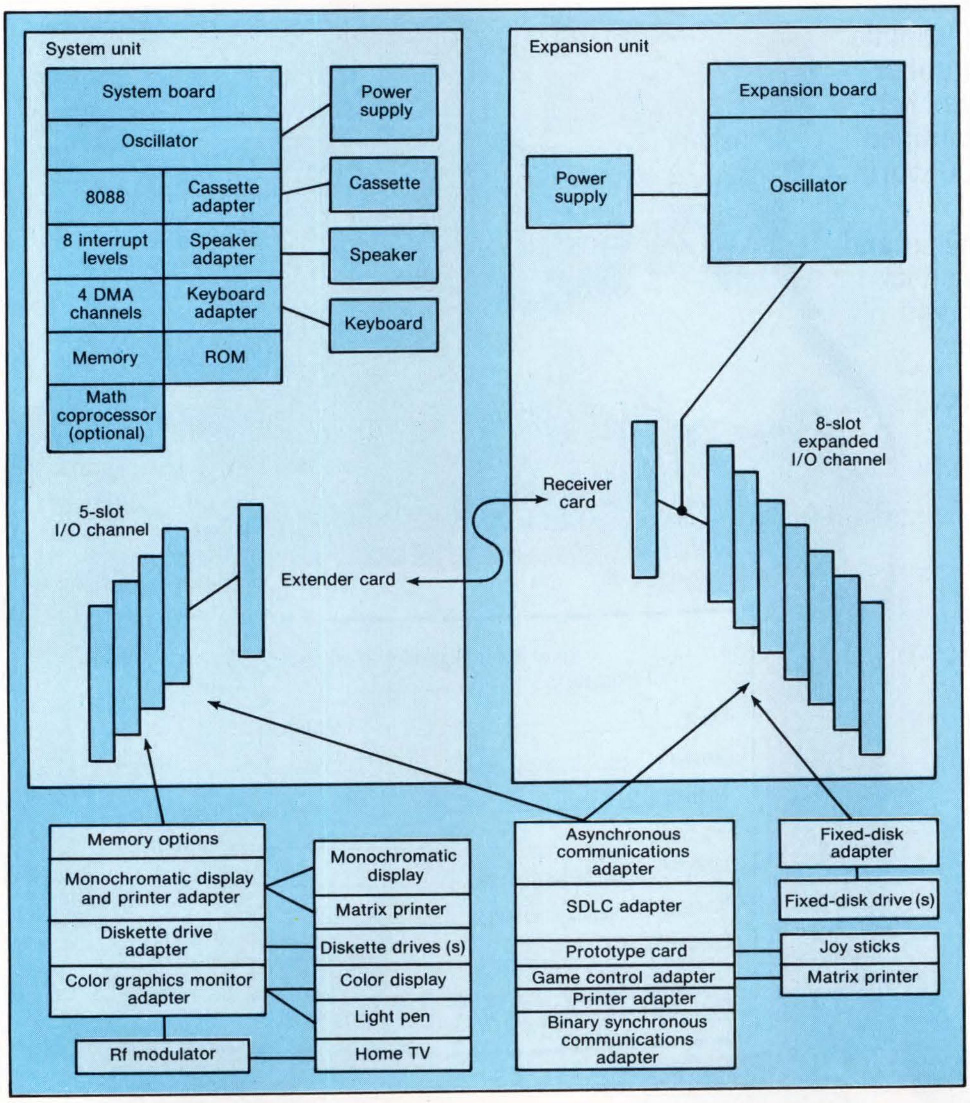
When IBM first published the specifications for its open-architecture PC, it revolutionized the standards for small personal computers. Overnight a new industry was born—OEM repackaging. Adventurous OEMs, always ready when opportunity knocks, knew that the PC would be around, garnering support, for years to come.

The PC's open structure has fostered tens of thousands of compatible products, including virtually all types of peripherals and almost every popular (and some not-so-popular) programming language. Most general-purpose software is developed first for the PC and then modified for other personal computers.

IBM's PC was the first successful small system to break the 8-bit, 64-kbyte barrier. Along with its overwhelming reception came double-density, double-sided floppy-disk drives and reliable fixed-disk drives of 10 Mbytes or more. With an 8088 CPU, which has a 16-bit internal and an 8-bit external data path, and a pair of floppy-disk drives, the PC significantly increased capability and capacity over existing personal computers. Sophisticated applications that had been restricted to larger computers were now being developed on an inexpensive small machine accessible to almost anyone.

Using the minimum configuration as a starting point, OEMs can build a multitude of systems with proprietary, third-party, or IBM components. Because essential parts like adapters, parallel and serial ports, and disk controllers need expansion slots, the machine's five available slots can be filled quickly. Fortunately, multifunction boards from third-party suppliers can greatly enhance each slot's utility. IBM itself offers an expansion unit that adds eight slots.

The value of the IBM PC for OEM systems is limited only by the imagination of the designer.



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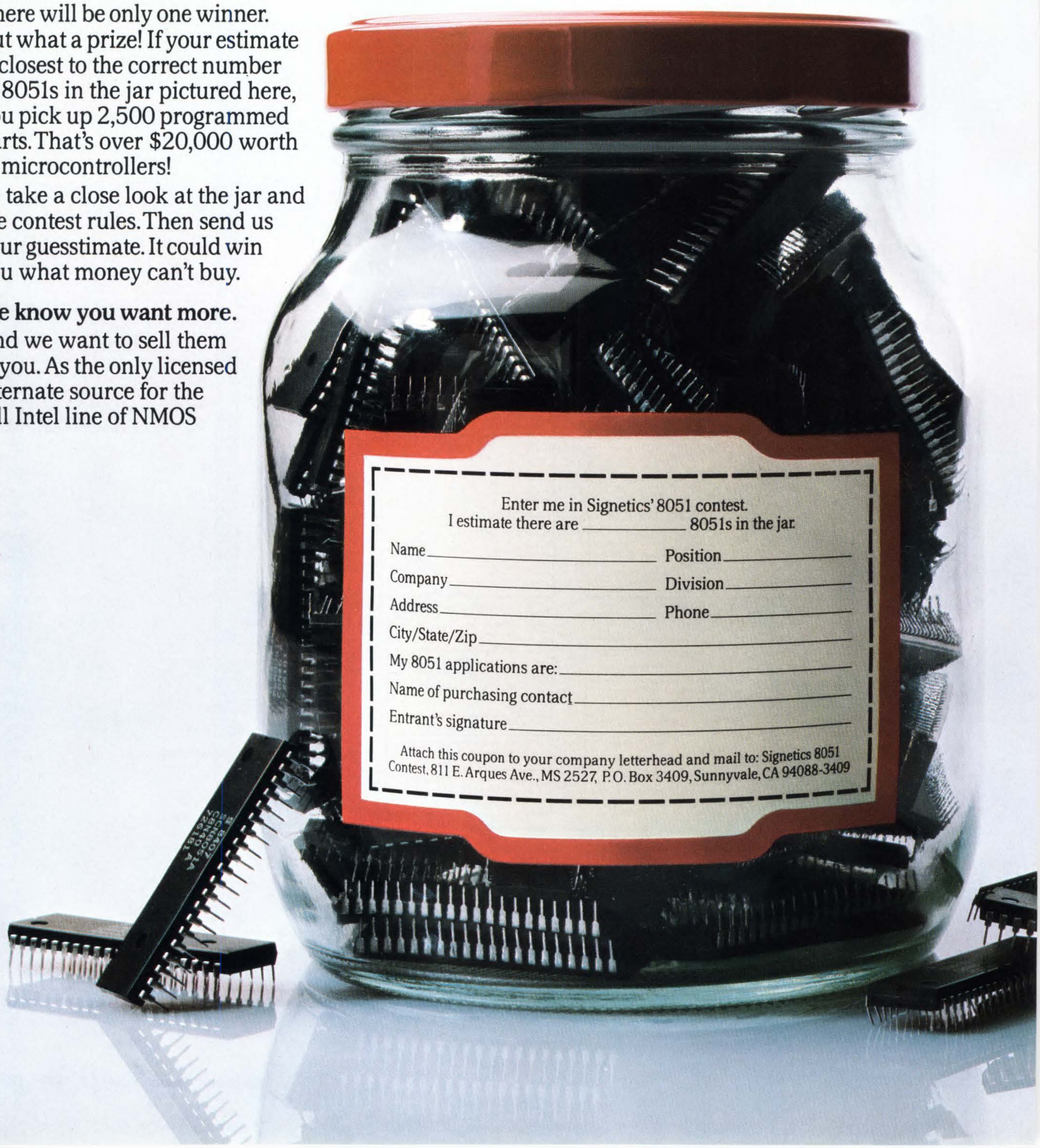

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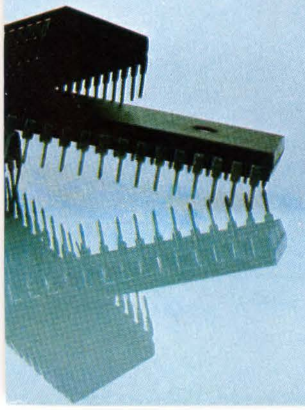
1. The closest guess to the correct number of 8051s in the jar is the winner. (In the event of ties, a drawing will be held to determine the eventual winner.)
2. The winner's company will receive 2,500 programmed SCN8051AH parts in the 40-pin plastic "N" packages. (A $20,000-plus value!) Product will be supplied to standard Signetics data sheet specifications.
3. All entries must be attached to the entrant's company letterhead.
4. The entry coupon (or facsimile) must be filled out completely and legibly.
5. Only one entry per person.
6. All entries must be postmarked no later than 8/31/84.
7. The winner will be announced on 9/28/84.
8. Shipment of 8051s to the winner will be 10 weeks after verification of the winner's ROM code in accordance with Signetics' standard verification procedure.
9. Signetics distributors, brokers, reps and Signetics/Philips employees are not eligible to win.
10. All entries will remain the property of Signetics.
11. Contest offer not valid where prohibited by law.



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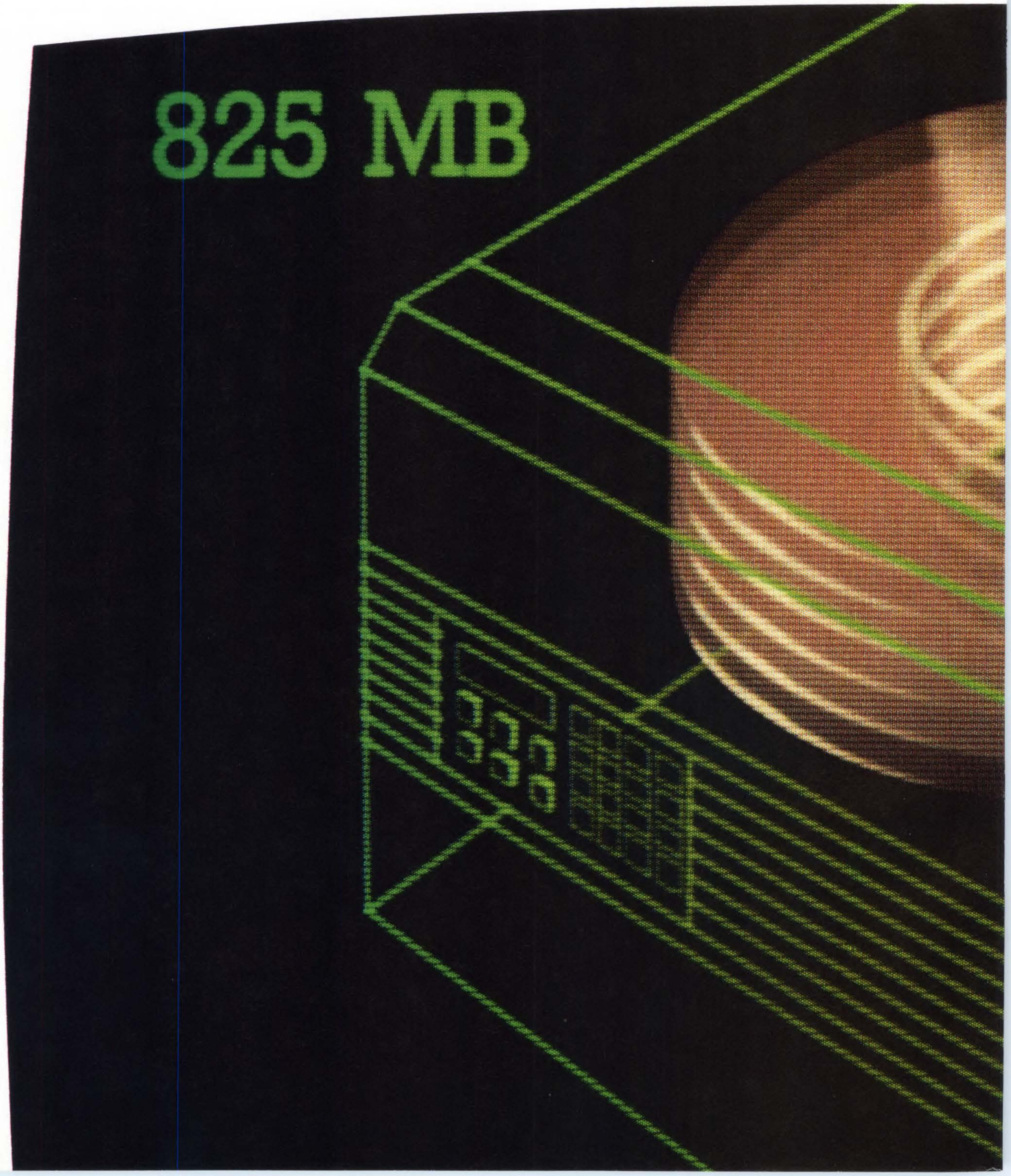
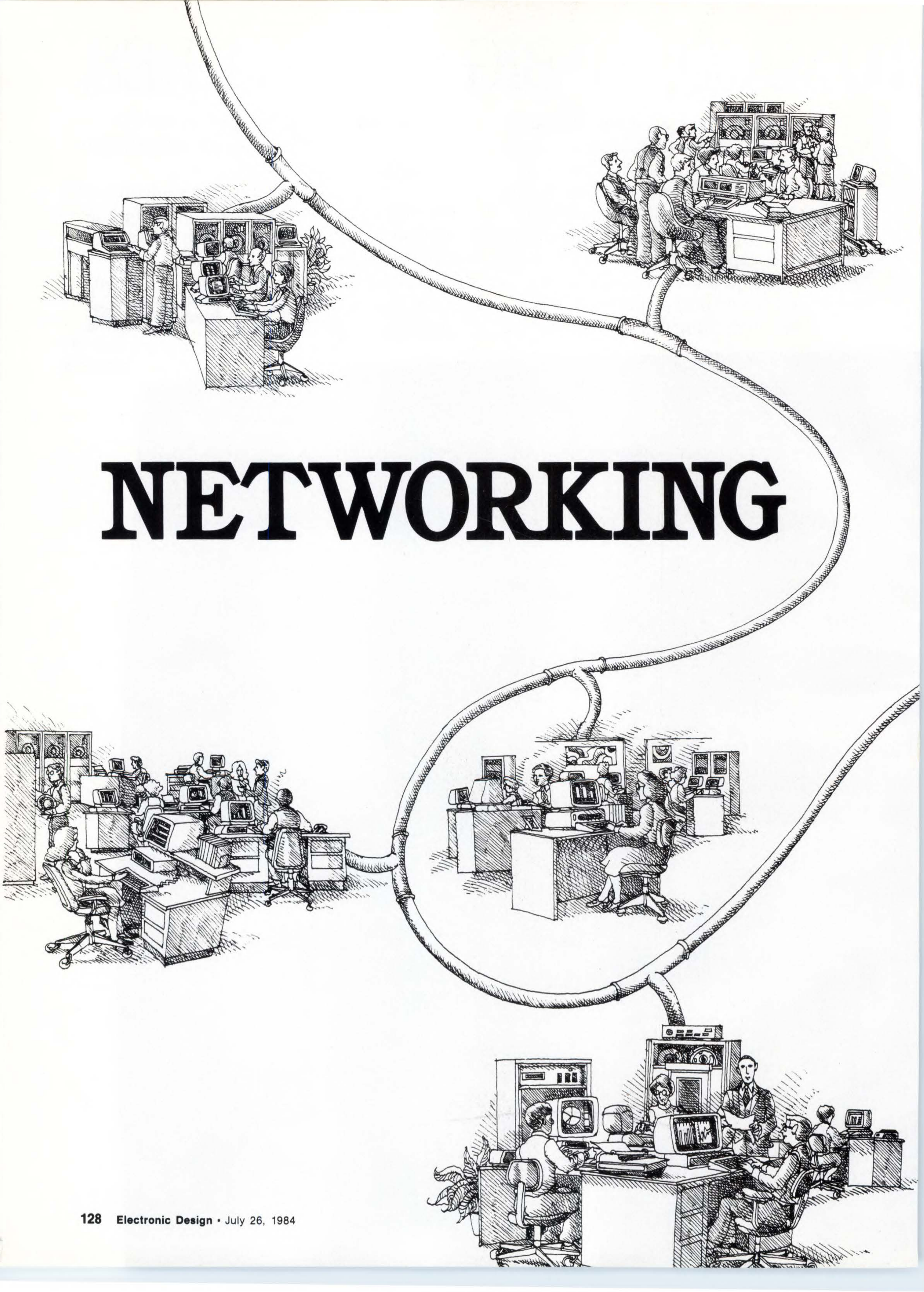
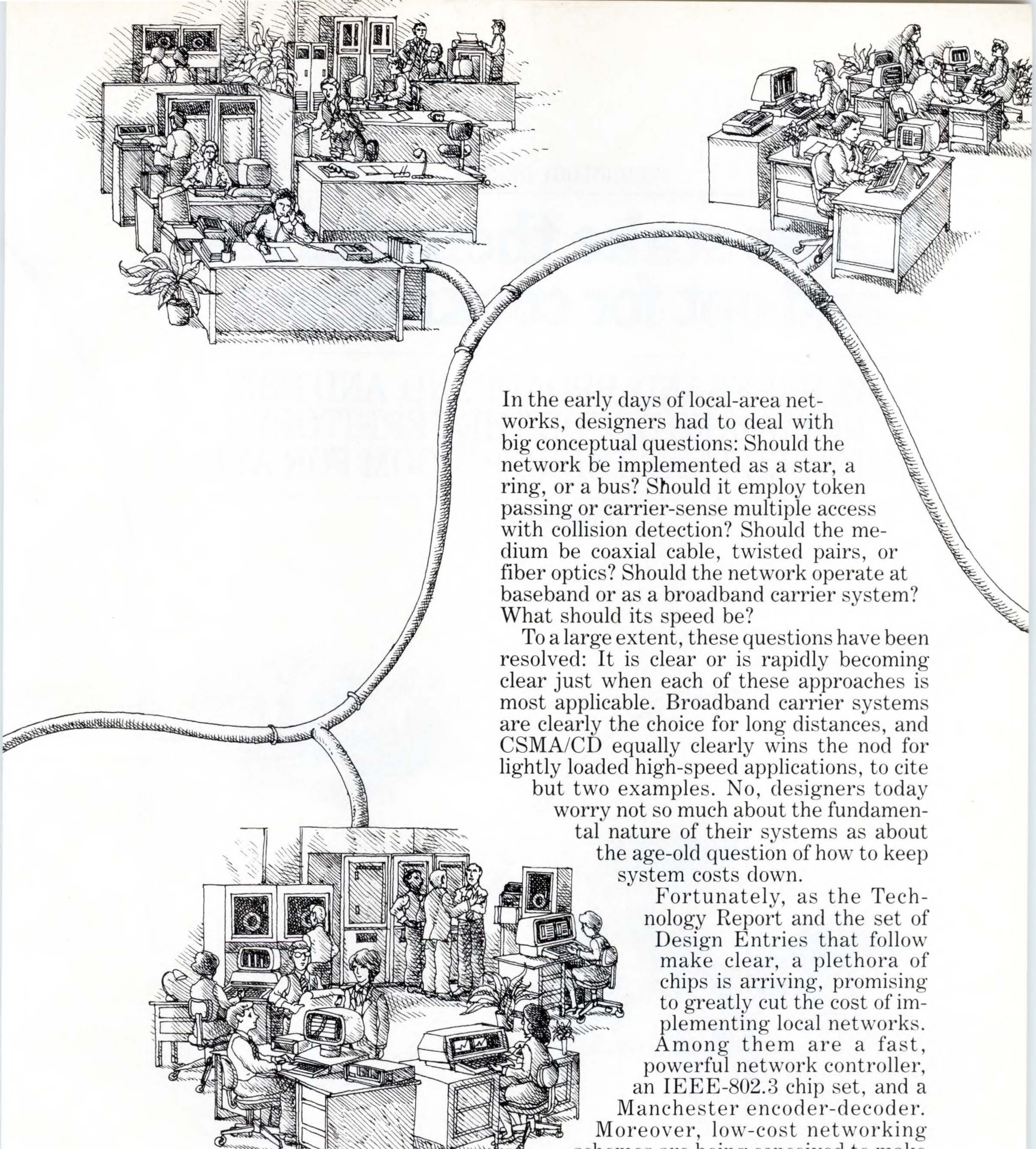


NETWORKING





In the early days of local-area networks, designers had to deal with big conceptual questions: Should the network be implemented as a star, a ring, or a bus? Should it employ token passing or carrier-sense multiple access with collision detection? Should the medium be coaxial cable, twisted pairs, or fiber optics? Should the network operate at baseband or as a broadband carrier system? What should its speed be?

To a large extent, these questions have been resolved: It is clear or is rapidly becoming clear just when each of these approaches is most applicable. Broadband carrier systems are clearly the choice for long distances, and CSMA/CD equally clearly wins the nod for lightly loaded high-speed applications, to cite but two examples. No, designers today worry not so much about the fundamental nature of their systems as about the age-old question of how to keep system costs down.

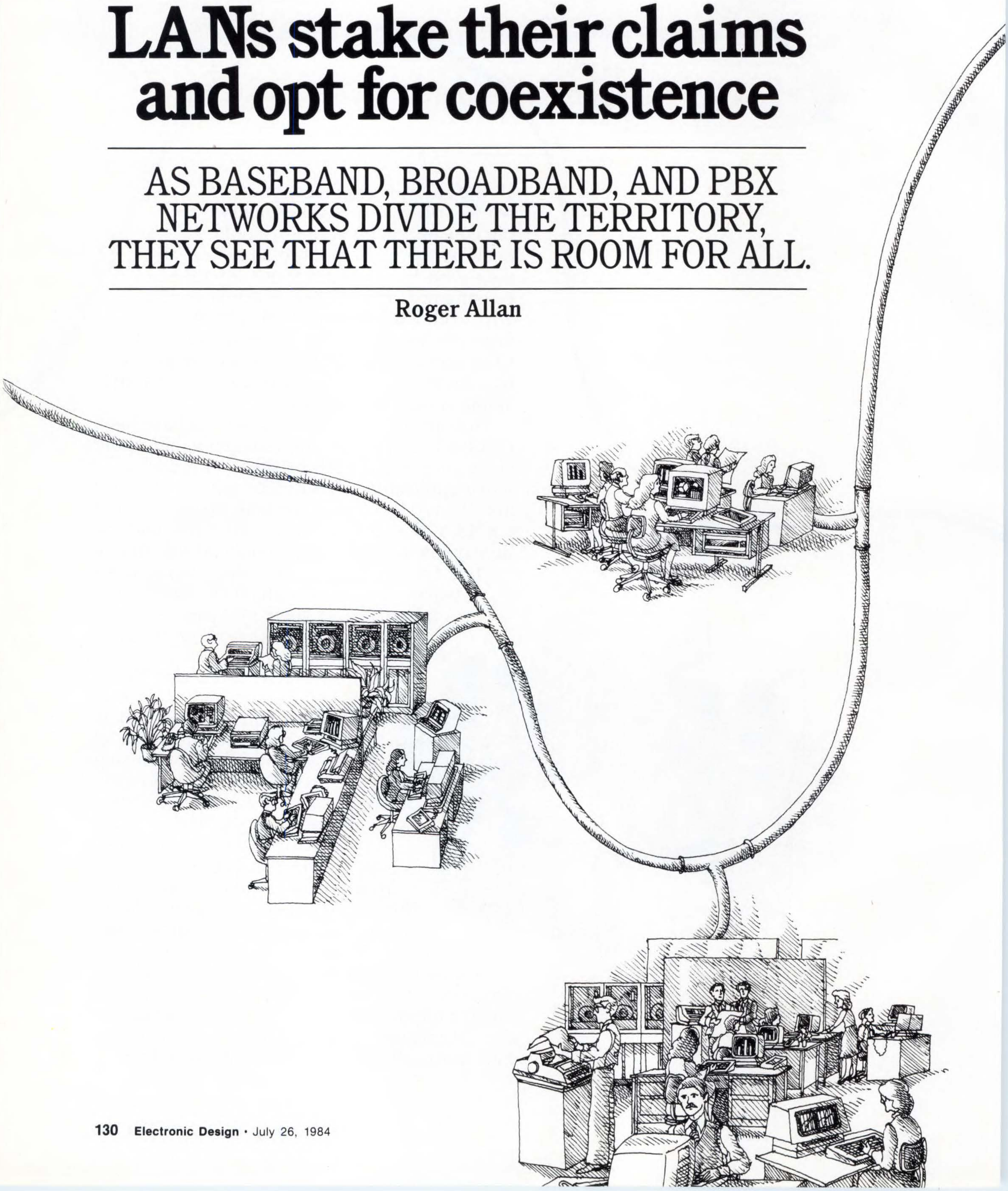
Fortunately, as the Technology Report and the set of Design Entries that follow make clear, a plethora of chips is arriving, promising to greatly cut the cost of implementing local networks. Among them are a fast, powerful network controller, an IEEE-802.3 chip set, and a Manchester encoder-decoder. Moreover, low-cost networking schemes are being conceived to make sure that designers do not have to pay for more capability than they need. A less expensive version of IEEE-802.3 for personal computers and a twisted-pair serial bus for integrated communications services are two unusual demonstrations of this trend.

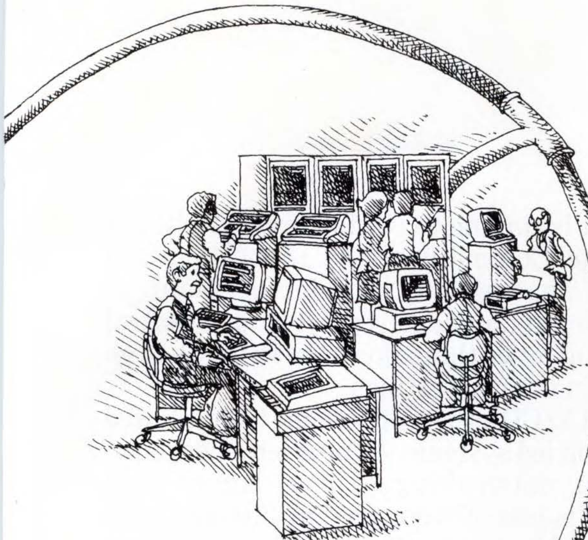
TECHNOLOGY REPORT

LANs stake their claims and opt for coexistence

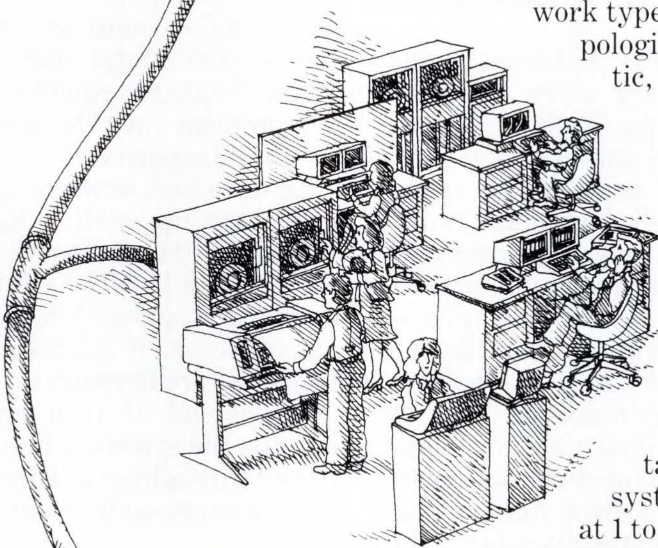
AS BASEBAND, BROADBAND, AND PBX NETWORKS DIVIDE THE TERRITORY, THEY SEE THAT THERE IS ROOM FOR ALL.

Roger Allan

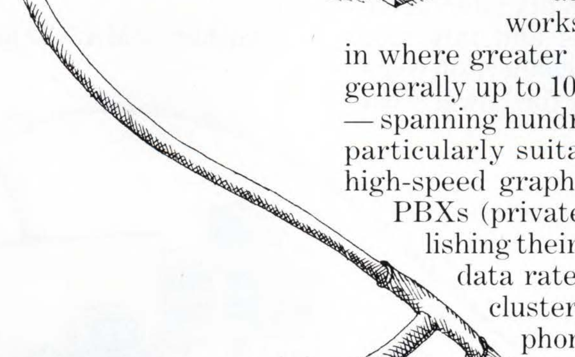




Progress is continuing apace in local-area networks. As might be expected, the old questions and debates concerning which topology, accessing scheme, and transmission medium best suit an application are being settled. Chip and board-level interfaces — in conjunction with the work accomplished by different standards organizations — have helped to carve out specific niches for baseband, broadband, and PBX networks. Interestingly, the two principal accessing schemes — CSMA/CD and token passing — though often competing, seem to be equally at home in all camps, making their presence felt in all three network types; in bus, ring, and star topologies; and on coaxial, fiber-optic, and twisted-pair cables.

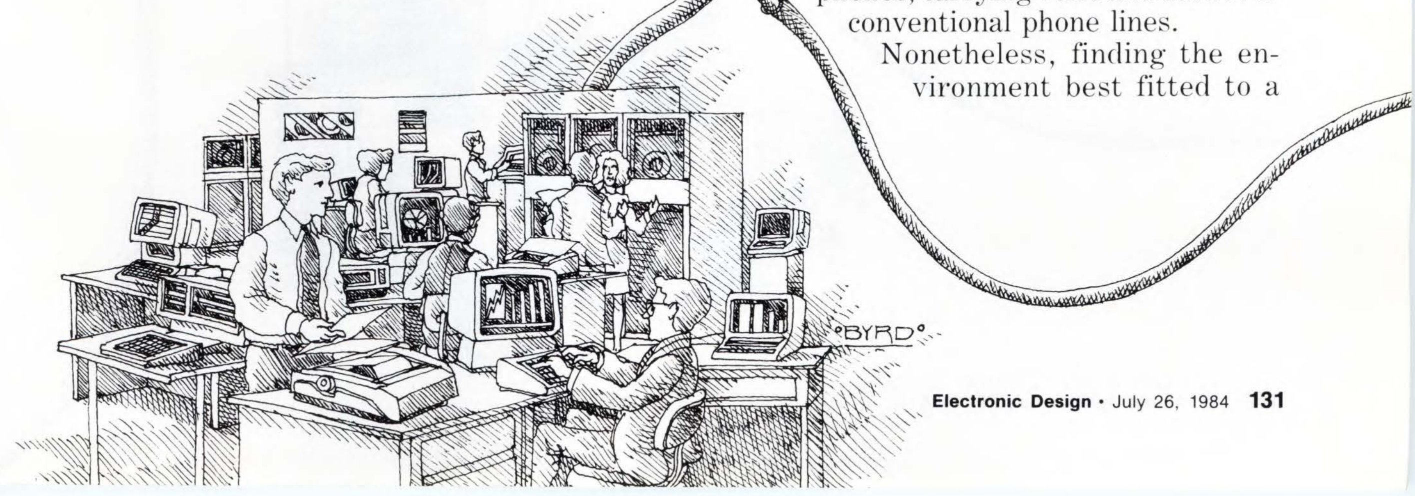


Baseband networks using CSMA/CD (carrier-sense multiple access with collision detection), such as Ethernet, have mainly staked their claim where expensive peripherals, like laser printers and Winchester drives, are to be linked within a single building or over distances of a few miles. Such systems typically transfer data at 1 to 10 Mbits/s. Broadband networks, on the other hand, are settling in where greater distances must be traversed — generally up to 10 miles. Their broad bandwidths — spanning hundreds of megahertz — make them particularly suitable for video conferences and high-speed graphics.



PBXs (private branch exchanges) are establishing their domain in settings that demand data rates of 1 Mbit/s or less. They join clusters of office terminals and telephones, carrying voice and data over conventional phone lines.

Nonetheless, finding the environment best fitted to a



network is only part of the story. In each area, work is under way to better the network itself. For instance, in baseband systems, efforts continue to improve the nondeterministic aspect of CSMA/CD in order to minimize message delays. For broadband networks, the main thrusts are to link more equipment and to handle more services. Finally, PBXs are going the all-digital route, looking eventually to become totally integrated systems that conform to the standard being developed for integrated services digital networks (ISDNs).

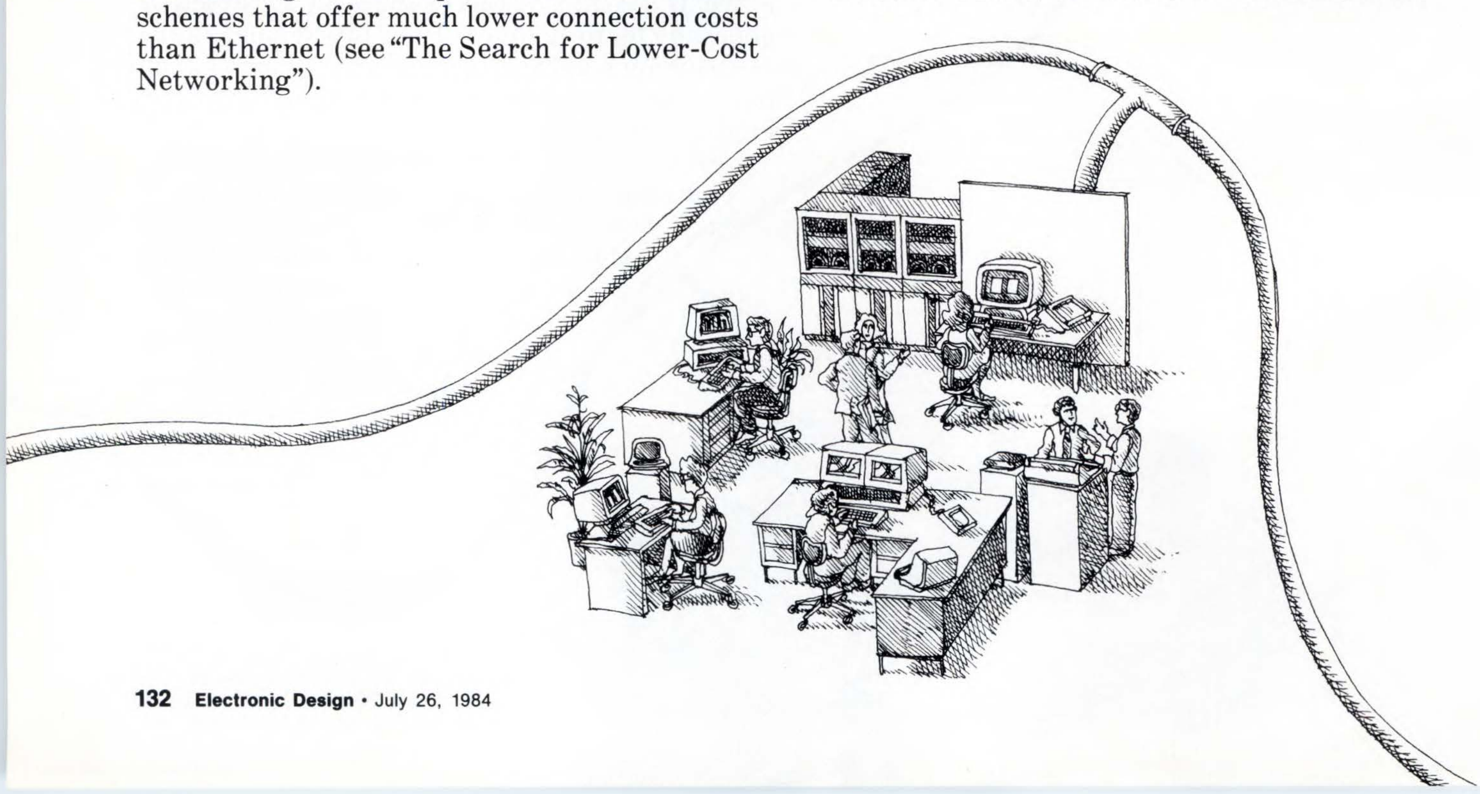
Among baseband networks, Ethernet is the most popular, mostly because there are more interface chips furnished for it than for any other system. Although the network's controller, transceiver, and encoder-decoder (or serial interface adapter) are still individual units, work is being carried out at several semiconductor manufacturers to integrate them further, ultimately realizing an intelligent microprocessor chip with a local network port. Such a device would in turn lower the cost of every Ethernet connection. Simultaneously, board-level manufacturers are taking whatever chips are at hand and building multifunction parts, further reducing connection costs. Against this background, chip and computer manufacturers are striving to develop devices and interface schemes that offer much lower connection costs than Ethernet (see "The Search for Lower-Cost Networking").

Ethernet is coming to the factory as well. For one, Bridge Communications Inc. (Mountain View, Calif.) has recently introduced a family of diskless communications servers and a central network controller that allows the network to go to work in industrial settings.

The CSMA/CD accessing scheme is well suited to lightly loaded systems. At heavier loads, however, most networking experts agree that CSMA/CD is less efficient and ultimately leads to unacceptable delays. Some critics claim that delays are encountered with as little as 70% of the network's total load capacity being tapped, although others argue that delays are not much of a problem until the system is loaded to about 90% of its capacity.

To solve such problems, AT&T Co. (New York) has come up with a high-speed Ethernet-compatible bus network that employs coaxial cable with a 10-Mbit/s data transfer rate and a maximum segment length of 500 m. Like Ethernet, 3BNet, as it is known, employs CSMA/CD. Unlike its predecessor, its packets are 4000 bytes long instead of 1500 bytes. Further, at 500 kbits/s, the system achieves five times the end-to-end throughput of Ethernet. Finally, the network accepts up to 100 nodes as taps along the cable.

Another CSMA/CD network—one which uses



a single twisted-pair cable—conforms to the first three layers of the ISO's Open Systems Interconnection (OSI) model (see "Firming Up the ISO's Reference Model," opposite) and transmits speech, data, and videotex signals at 1.024 Mbits/s. The Integrated Services Terminal, or IST, bus network from Philips International BV (Eindhoven, the Netherlands) links up to 30 stations that are separated by as much as 350 m (see p. 171). Although the bus uses a contention-accessing scheme, it also ensures that stations gain access to the network within 250 μs (for an idle channel) or within the time needed to transmit a packet plus 2 ms (for an occupied channel with no collisions). This modified form of guaranteed access, combined with contention accessing, is made possible by the IST's software, which assigns certain stations higher priority than others.

Linking up to broadband

Broadband local networks of all types are also proliferating, particularly where data must be transmitted over longer distances than those possible with baseband networks. Also, they are being put in place for sending wide-band video and time-critical voice signals.

One broadband system that uses CSMA/CD accessing detects signal collisions by employing the bit-comparison scheme. (There are three main methods of detecting collisions, bit comparisons, energy-level detections, and code violations or illegal transitions.) LocalNet 20, from Sytek Inc. (Mountain View, Calif.), uses more than 95% of its channel before delays are encountered. The network supplies up to 120 continuous channels, each with a 300-kHz bandwidth and is capable of transmitting signals at 128 kbits/s. To allow computers and terminals to tie into the system, LocalNet employs packet communications. As an added benefit of this approach, some of these packets allow data to be encrypted, which can greatly enhance network security.

The company feels that baseband and broadband CSMA/CD networks will coexist, with each fulfilling different needs. Ethernet, it believes, will be given over to local environments, such as within a building, and broadband networks will tie several such local configurations together. In fact, Sytek feels that the present method of using gateways to connect several baseband networks in different buildings is limited by the distances those systems can span.

Instead, it proposes that broadband rf subnetworks be brought into each building, each of which would contain a local head end. (A head end is a central hub of a broadband local network. It receives signals at one set of frequencies and retransmits them on another.) Baseband networks would then be linked to the sub-

Firming up the ISO's model

Efforts to develop protocols for the ISO's seven-layer Open Systems Interconnection (OSI) reference model are gathering speed. Not only has the basic reference model been adopted by the ISO as standard 7498 and by the CCITT as recommendation X.200, but protocols for many of its layers are in various stages of being accepted as either draft proposals or draft international standards.

(An ISO document goes through three stages before it becomes an international standard: a draft proposal, a draft international standard, and an international standard. Once it reaches the second stage, its ratification as an international standard is mostly procedural. Changes between the first and second stages are generally minor.)

In general, each layer consists of two parts, a service and a protocol specification, each of which must go through the three stages of approval. The service specification defines what the layer does, and the protocol specification defines how it does it. Since the first specification is one of principles and is not as specific as the second, it is generally easier to get accepted than the second one. Furthermore, each layer can have more than one protocol. (Often, discussions of the OSI reference model actually refer only to the service specifications.)

Protocols for all seven layers are in various stages of standardization, with ones for the network, transport and session layers and for file transfers (the application layer) closest to completion. Generally, there are proposals for many protocols within each layer, and new proposals are constantly being put forth. Moreover, the ISO's work on the OSI reference model will always continue, since protocol proposals are constantly evolving from varous standards groups.

networks. Specifically, it sees broadband CSMA/CD networks joining several buildings, with the rf subnets branching off the broadband backbone that runs between them.

Enabling baseband CSMA/CD networks to operate on their broadband counterparts is a subject being investigated by Digital Equipment Corp. (Maynard, Mass.) and M/A-COM DCC Inc. (Germantown, Md.). Instead of the three common collision detection schemes, though, the two companies have proposed a variation on the bit-comparison technique. It calls for all network transceivers to demodulate a detected rf burst identically (even in the presence of different absolute values of the burst at various network taps).

Further, it specifies that all transceivers stay tuned to an out-of-band frequency. That frequency can be used by any collision-detecting transceiver to halt transmissions and to allow all nodes to back off and try again. The technique is said to furnish a better collision detection capability for a 3000-m network than any of the existing collision detection schemes.

As mentioned earlier, a key objection to CSMA/CD is the lengthy transmission delay encountered on heavily loaded systems—a serious shortcoming for real-time applications like voice transmission and process control. It comes as no surprise, then, to discover that widespread research is being carried out to overcome this shortcoming by combining contention and deterministic accessing schemes.

Minimizing contention delays

Researchers at the Universities of Siegen and Stuttgart (both in West Germany) have jointly developed a protocol for broadband networks that allows both contention accessing (when a broadband channel is idle) and deterministic accessing (when a channel is busy). The researchers have modeled, analyzed, and simulated their protocol, known as CSMA/CD/DP (the last pair of letters for "dynamic priorities")

The search for lower-cost networking

Because of the relatively high cost of connecting personal computers on networks like Ethernet (even though that cost is constantly dropping), the search is on for a less expensive means of linking them, one that trades off some performance for a simpler and less expensive interface.

One manifestation of this search is Cheapernet (see p. 185), a concept first broached by the European Computer Manufacturers Association and later taken up by the IEEE 802 Local Area Network Standards Committee. The first interface chip set for Cheapernet is now available from National Semiconductor Corp. (see pp. 193 and 203).

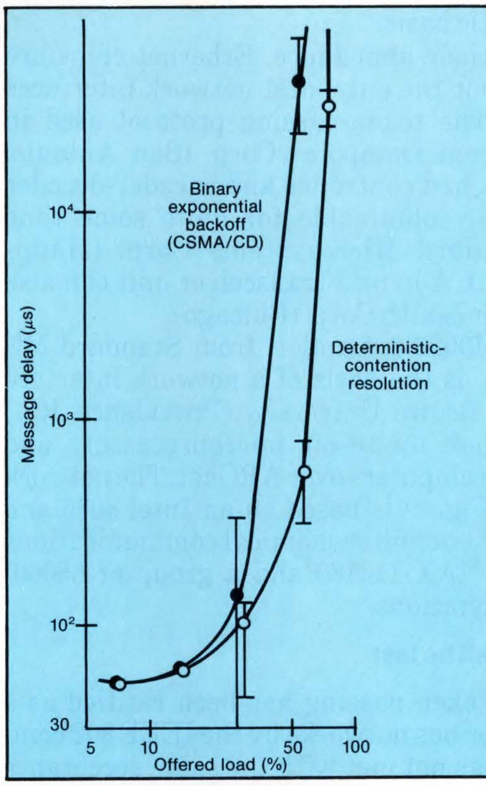
A major challenger for designers of Ethernet/Cheapernet chip sets is the safety requirement for high-voltage isolation. The chips must be protected against high-voltage transients and lightning surges on the transmission medium, as well as against ac power-line voltages that may be present (if the transmission medium accidentally touches the ac power line). The European Computer Manufacturers Association calls for isolation of 2000 V rms minimum, whereas the IEEE 802 committee specifies 500 V rms, capabilities that are not yet within the grasp of silicon. National Semiconductor solved this problem for its Ethernet/Cheapernet chip set with specially designed isolation transformers, in 16-pin DIPs, from Pulse Engineering Inc. (San Diego, Calif.). The units are compatible with the IEEE-802.3 specifications for Ethernet/Cheapernet and can be used with any of the other available Ethernet chip sets.

Despite Cheapernet's lower cost per connection, several companies feel that Cheapernet is not low enough in cost in general, and in particlar that its 10-Mbit/s speed makes the complexity and cost of the transceiver chip relatively high. Instead, they argue that a midrange (1-Mbit/s) local network using conventional twisted-pair wiring (or even RG58U coaxial cable) would lower the cost per network connection even more, making the networking of personal computers and terminal clusters truly practical.

At the IEEE 802 committee's general meeting in February, a group of four companies—AT&T, Intel, NCR, and Wang Laboratories—presented a proposal for a 1-Mbit/s network. By a 15-0 vote, the committee decided to evaluate the proposal further at its next general meeting, July 15-20, in Vancouver British Columbia. The four were backed by six other computer makers, and Intel is on the verge of introducing a chip set for such a 1-Mbit/s network.

and report high throughputs and low delays for both normally loaded and overloaded networks.

Engineers at Nippon Telegraph and Telephone Public Corp. (Yokosuka, Japan) have come up with a CSMA/CD scheme they call deterministic contention resolution (DCR). During normal transmissions, the protocol operates like standard CSMA/CD. When collisions occur, they are resolved by a form of implicit token passing. The accessing scheme has been tested on a prototype fiber-optic network, with favorable results reported (Fig. 1).



1. A CSMA/CD accessing scheme that employs a degree of deterministic contention resolution (DCR) can boost confidence levels to 95%. Proposed by NTT, the technique is superior to conventional CSMA/CD, which employs a binary exponential backoff (BEB) algorithm. The curves show message delay as a function of network load, for 510-bit-long messages transmitted at 10 Mbits/s.

The best of three

Not all such work is restricted to the research and development stage. One local network automatically combines the best of the three major accessing schemes—CSMA/CD, token passing, and time-division multiplexing—on baseband and broadband coaxial cables, as well as on fiber-optic cables. UniLan, from Applitek Corp. (Wakefield, Mass.), is a 10-Mbit/s network that operates with variable- and fixed-length messages in both contention and deterministic modes. When the network is lightly loaded, it runs like a typical CSMA/CD system. As network traffic increases and as intelligent synchronous terminals are added on (or both), UniLan senses the changes and adjusts for a more deterministic form of accessing—thus speeding response times.

Although UniLan costs about 10% to 15% more than Ethernet or a straight token-passing network, it affords the access advantages of both through its universal access protocol. The protocol, called UniLink, breaks up the network's 10-Mbit/s transmissions into message periods that handle fixed- and variable-length data packets. The message periods are assigned to specific equipment (depending on whether they are asynchronous or synchronous) and are numbered sequentially. Asynchronous equipment with low duty cycles shares time slots and thus accesses the network on a contention basis. Synchronous equipment, as well as intelligent terminals and mainframe computers, are assigned exclusive time slots (see the table, opposite) and thus accesses the network on a more

UniLink protocol

Message length	Message number allocation		Performance similar to:	Applications
	Dedicated	Contention		
Variable	Yes	Yes	Token passing and CSMA/CD	Mixed environments
	Yes	No	Priority token passing	Synchronous devices: real-time voice, factory control
	No	Yes	Priority CSMA/CD	Asynchronous burst devices
Fixed	Yes	Yes	Dual-mode STDMA	Highly synchronous applications or long networks
	Yes	No	Reservation STDMA	
	No	Yes	Contention STDMA	

STDMA = slotted time-division multiple access deterministic basis.

Despite their abundance, Ethernet chips are obviously not the only local network interfaces available. The token-passing protocol used in ARCnet, from Datapoint Corp. (San Antonio, Texas), has had controller and encoder-decoder chips readily obtainable for quite some time from Standard Microsystems Corp. (Hauppauge, N.Y.). A hybrid transceiver unit can also be had from Zenith Corp. (Chicago).

The COM9026 controller, from Standard Microsystems, is the basis of a network interface board that Brown University (Providence, R.I.) built to hook up 16-bit microprocessors and 32-bit minicomputers over ARCnet. The network interface (Fig. 2) is based on an Intel 8085 and allows efficient and economical communications between a VAX-11/780 and a group of 68000-based workstations.

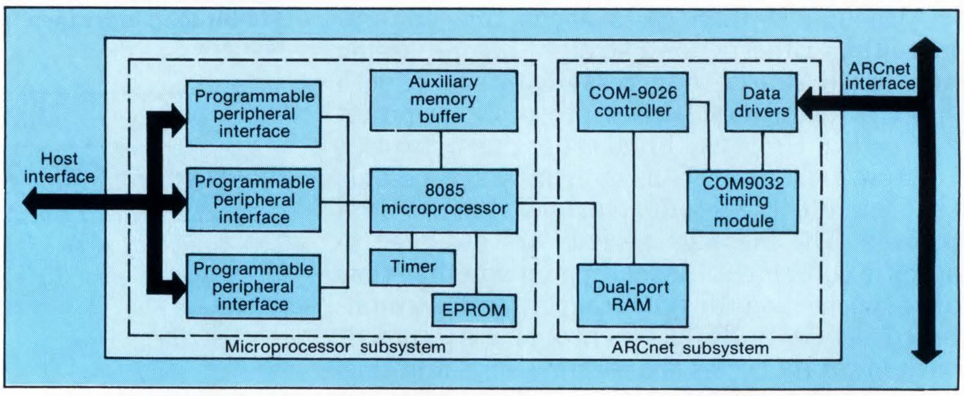
The first shall be last

Though token passing has been ratified as a standard for bus networks by the IEEE 802 committee, it has not met with the same acceptance for ring networks. The 802.5 working group must still resolve a number of issues; one of the more important being the order in which bits are transmitted. In the 802.3 and 802.4 standards, which govern CSMA/CD bus networks and token-passing bus systems, respectively, the least significant bit is transmitted first in a message packet. The 802.5 proposal reverses that order, sending the most significant bit first.

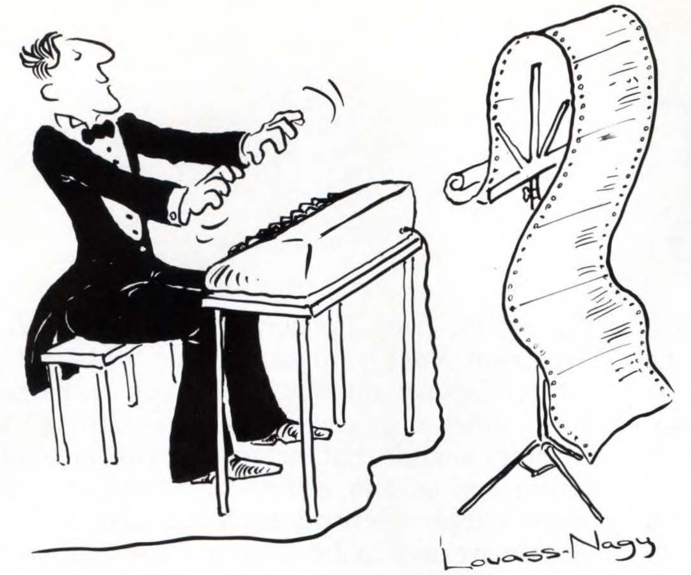
Although the second approach is more efficient in some cases, allowing more rapid comparisons of items such as group addresses and messages priorities, the difference in the transmission order is seen by some as the root of unnecessary complications. Beyond its incompatibility with the previously approved standards, there is also the problem of the circuitry needed to wed MSB-first networks to their LSB-first counterparts. The MSB adherents, on the other hand, argue that such circuitry is relatively easy to implement in silicon and that the advantages of the MSB-first approach far outweigh what they see as minor difficulties. It should also be noted that communications systems have traditionally implemented the LSB-first scheme and computer systems have gone with the MSB-first method.

In the chips

Texas Instruments Inc. (Dallas) is working on the first chip set for a token-passing ring. The set is being built for IBM Corp. (Armonk, N.Y.), for the latter's planned token-passing ring network. Although TI has yet to fabricate any interface ICs (which are more difficult to make than CSMA/CD interface chips), the feeling among



2. A sophisticated interface circuit, designed by researchers at Brown University, ties VAX-11/780 minicomputers and 68000-based workstations into Datapoint's ARCnet, a token-passing bus network. The interface is built around the COM9026 controller chip, developed at Standard Microsystems. Three programmable peripheral interfaces are needed, two as I/O ports and one for control and status signals.



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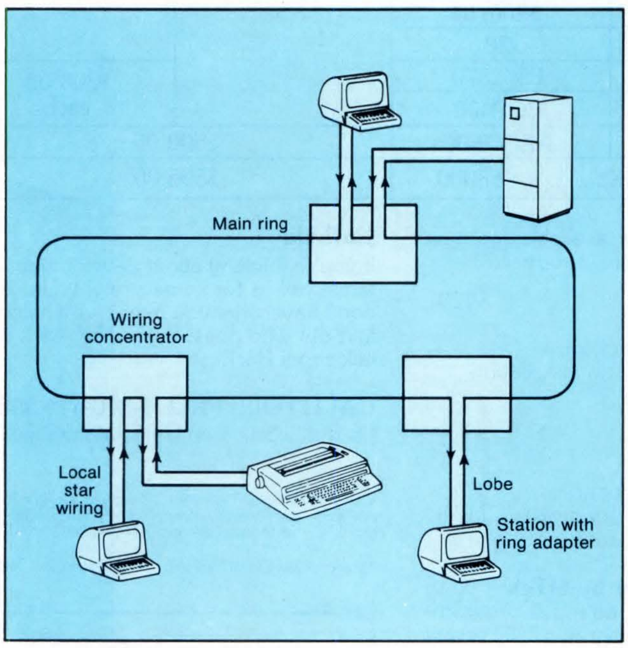
many in the IEEE 802 committee is that the company is too far along with its design for the MSB-first token-passing proposal not to be passed. The consensus is that 802.5 will be standardized by the 802 committee sometime this year.

For its part, IBM has so far only shown a prototype of its network, demonstrated by its research laboratory (Rüschlikon, Switzerland). The prototype (Fig. 3) employs passive wiring concentrators to link terminals over twisted pairs (fiber-optic cables may also be used for longer-distance communications). Data is sent over the main ring at 4 Mbits/s, and bypass relays are used within the wiring concentrators to handle malfunctioning terminals and to isolate them from the ring.

At home and at work

Before the end of the year, the first token-passing broadband bus network to meet the IEEE-802.4 standard will be unveiled.



3. In IBM's token-passing ring, wiring concentrators interconnect terminals and computers over twisted-pair wire. Relays inside each concentrator allow transmissions to bypass downed and inoperative nodes so that the rest of the network can continue normal operation.

Token/Net, from Concord Data Systems Inc. (Waltham, Mass.), is designed both for the office and for factory automation. Access to the network, which uses coaxial cable, is through an interface module that includes a frequency-agile 5-Mbit/s rf modem, controller, access unit, and power supply. Several such modules, dubbed TIMs, were used to demonstrate how equipment from different manufacturers could communicate using General Motors' Manufacturing Automation Protocol (MAP). The demonstration was held earlier this month at the National Computer Conference.

The Token/Net approach is taken one step further with a network that totally integrates voice, data, and text (Fig. 4). Although Sopho-LAN, from Philips, handles all three types of signals, it treats each of them separately.

Controlling accessing delays is particularly important for voice transmissions, especially as PBXs attempt to enter the world of local networks as universal voice and data carriers.

Concern with such delays is one reason why Ztel Inc. (Wilmington, Mass.) chose to adopt a token-passing scheme for its network, PNX. The system uses a PBX as one node in its ring and conforms to the proposed IEEE-802.5 standard.

Double rings

The network makes use of existing twisted-pair wiring for the PBX. It also consists of circuit and packet rings (configured with either coaxial or fiber-optic cables) that carry both voice and data traffic. The former operate at 64 kbits/s; the latter, 10 Mbits/s. Access to the network is possible at each node through a system processing unit, which performs switching (for voice and data transmissions over telephones), handles such tasks as routing, and takes care of data conversion (for establishing data packets and translating protocols). Up to 40 rings can operate within the PNX (although the theoretical limit is in the hundreds) so backup rings ensure reliability (Fig. 5).

Instead of a ring architecture, InteCom Inc. (Allen, Texas) is using a standard star topology to permit its PBX to handle voice and data communications. The company's integrated business

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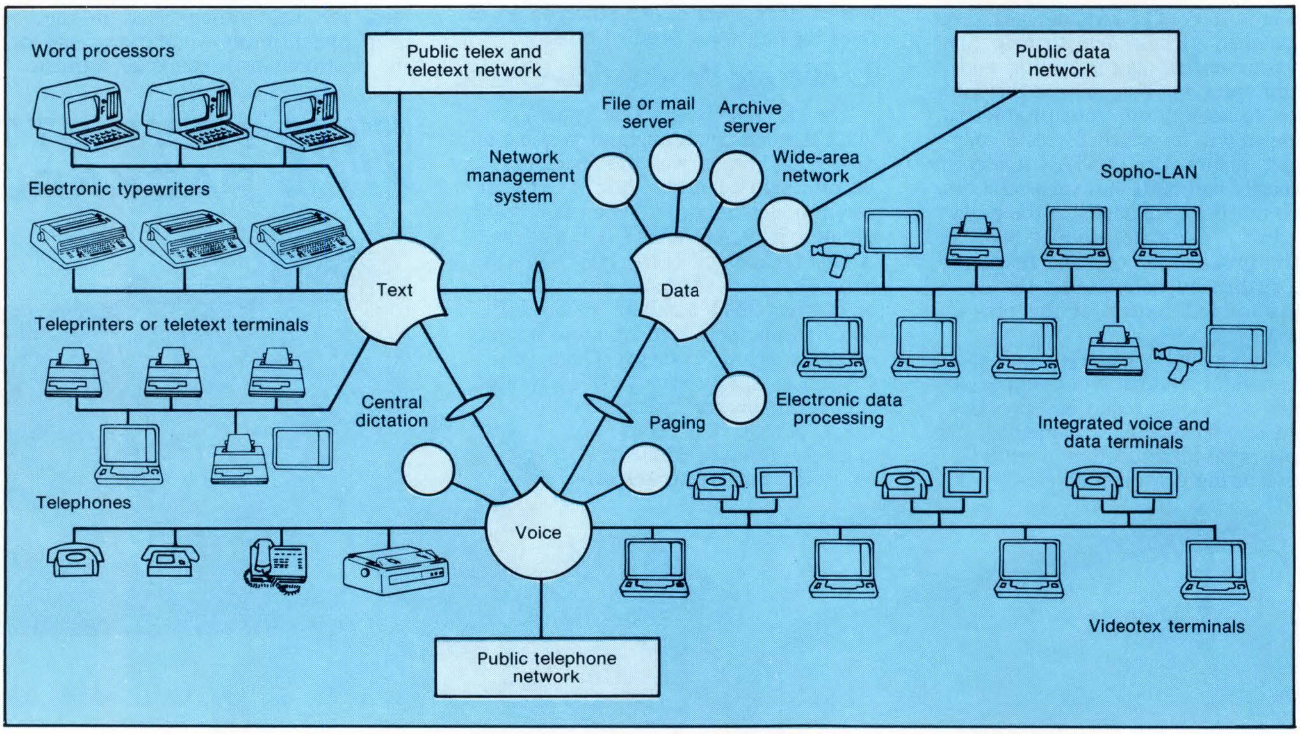
NETWORKING

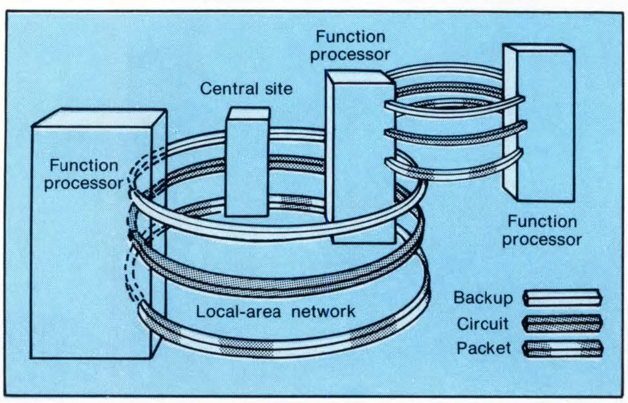
exchange, or IBX, is transformed into a local network by fitting it out with the company's LANmark (Fig. 6). The network uses standard twisted-pair wiring, yet permits terminals and other devices to communicate with one another in 10-Mbit/s bursts. The completely digital network has a 512-Mbit/s bandwidth and carries out both full-duplex voice (circuit) and data (packet) switching.

The use of digital PBXs to integrate voice and data communications in the office has proven very popular, since it allows users to build onto existing telephone networks. These integrated PBXs are coming in at all sizes, down to systems intended for 10 to 100 telephones. The Telenova 1, from Telenova Inc. (Los Gatos, Calif.), is a wholly digital system with a twin-bus architecture—an 18-Mbit/s circuit-switching bus and a 670-kbyte/s packet-switching bus (ELECTRONIC DESIGN, April 4, p. 38).

At AT&T Information Systems (Morristown, N.J.), designers have combined the advantages of centralized PBX architectures and distributed local area bus architectures in a voice and data



4. The Sophomation system, from Philips International, totally integrates voice, data, and text information. A key component is SophoLAN, a broadband token-passing bus.

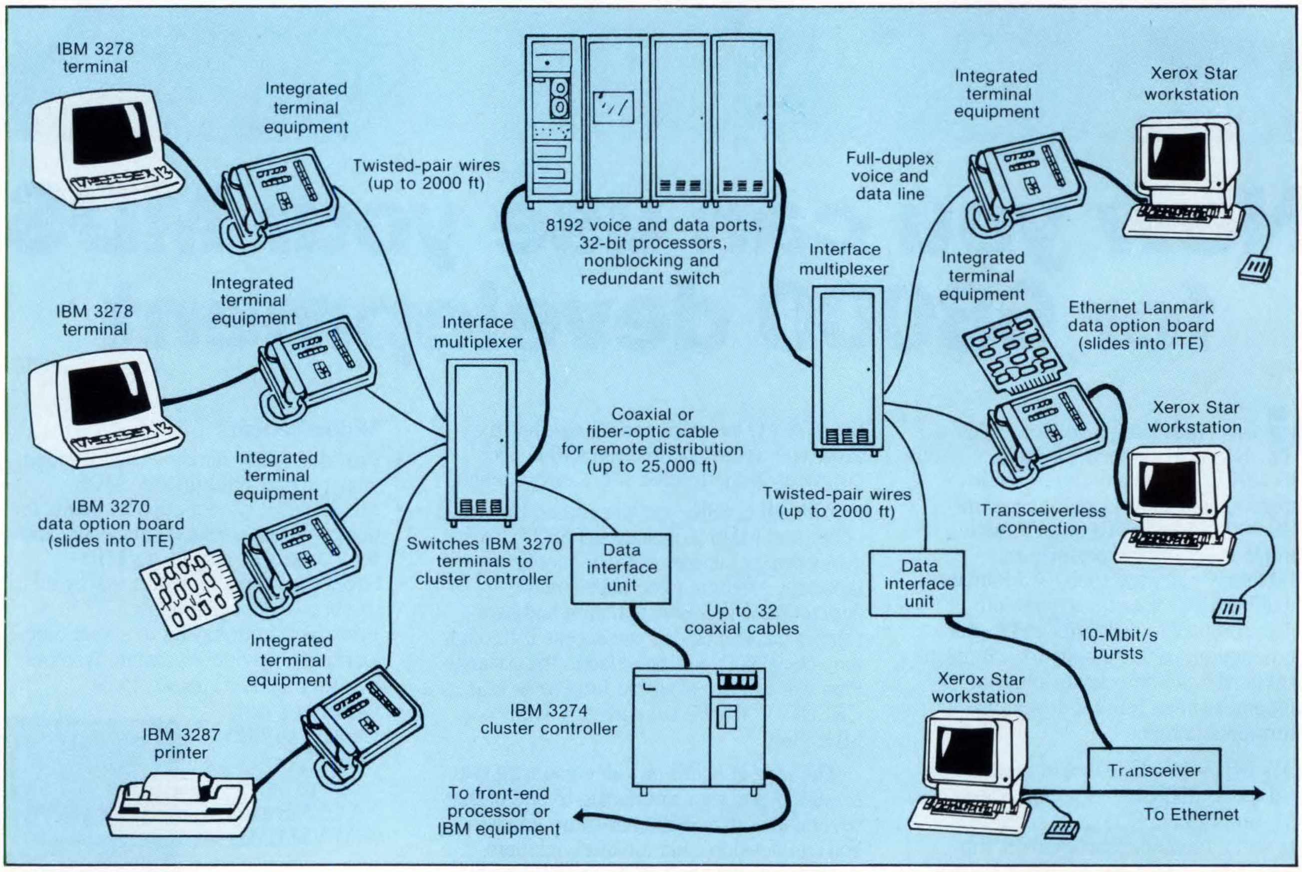


5. Voice and data rings form the backbone of the PNX, a token-passing ring that counts a PBX as one of its nodes. A function processor supervises all access to the Ztel network. Circuit rings carry voice signals at up to 64 kbits/s, and packet rings carry data at up to 10 Mbits/s. Both ring types can use twisted-pair or fiber-optic cables.

network. Dubbed the Datakit/VCS (virtual circuit switch), the star network comprises a switch and two buses: one for contention and one for sending or broadcasting information (Fig. 7a). The buses are kept short to minimize propagation delays inherent in longer buses, and the backplane that houses the buses is used for plug-in cards that allow specific types of terminals (e.g., asynchronous, synchronous, bisynchronous) to be linked. The delay associated with each packet transmission is less than that found in conventional CSMA/CD bus and token-passing bus networks (Fig. 7a).

Instead of a star, Doelz Networks Inc. (Irvine, Calif.) uses a ring to handle circuit- and packet-switched data in its Elite One system. The network employs a prioritized contention-accessing scheme that transmits data at up to 10 Mbits/s—regardless of the type of cable used. (At present, the system is being used at up to 56 kbits/s). A unique aspect of the network, which speeds packet transmissions, is the inclusion of destination addresses in the packet right at the interface node. Other networks require the assembly and disassembly of destination addresses at the central switch as well as the destination. Since Elite One demands that packets be assembled and disassembled only at the end points of the network, packet transmission is speeded up considerably. In fact it takes less than 6 ms for a packet to enter and leave a switch.

As PBXs take on more and more data and voice



6. LANmark, a PBX-based local network from InteCom, lets IBM and Xerox terminals communicate in 10-Mbit/s bursts over standard twisted-pair wiring. The system has a 512-MHz bandwidth and transmits voice and data in a full-duplex mode.

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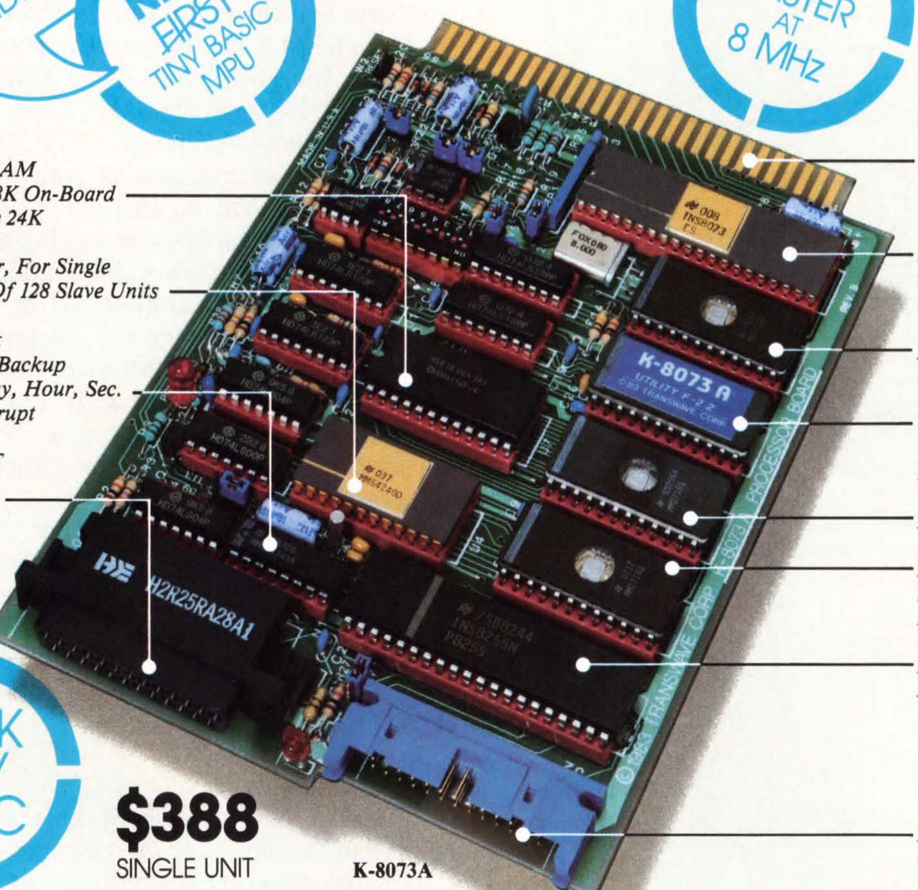

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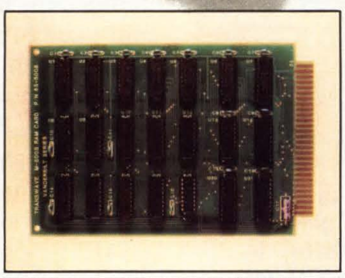

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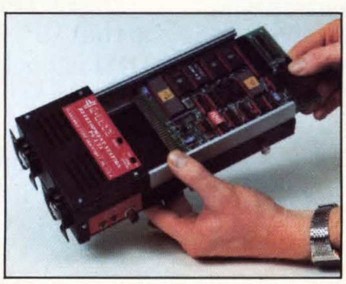

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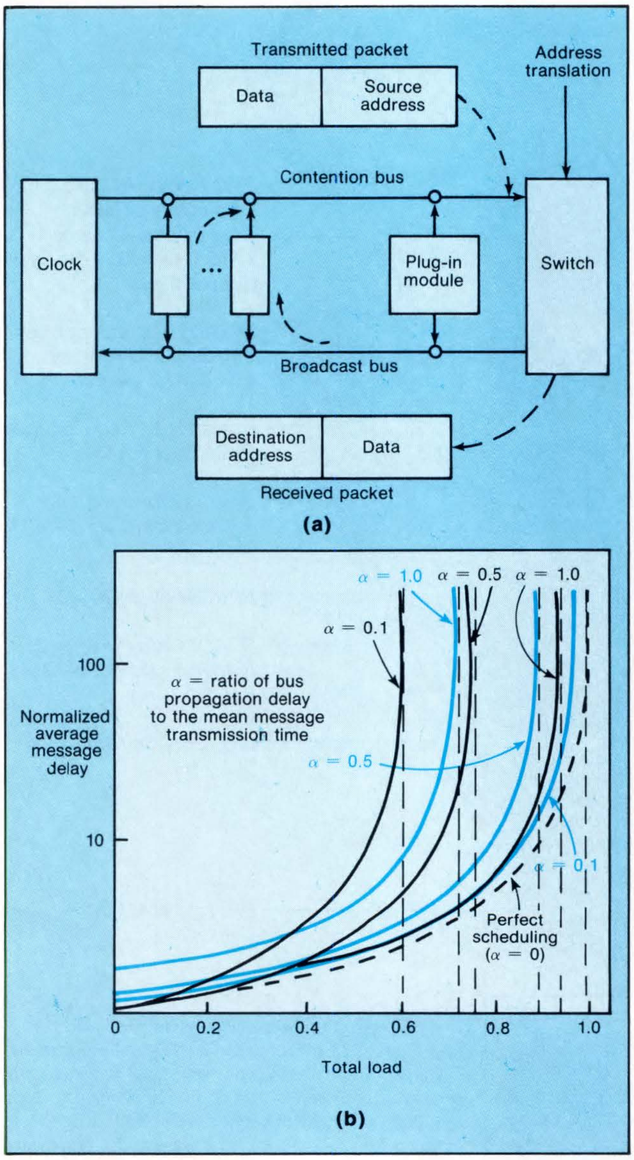


7. Two distributed buses (contention and broadcast) and a centralized PBX system combine to give AT&T Information Systems the best of two worlds (a). In terms of message delays, AT&T's Datakit/VCS network excels in both CSMA/CD (solid black) and token passing (solid color) for scheduling packet transmissions at different loads, when compared with perfect scheduling (dotted line) (b). As the ratio increases between bus propagation delay and the mean message transmission time, the performance of CSMA/CD and token passing decreases.

transmissions, efforts are underway to standardize PBX-to-computer interfaces. Two such efforts are the computer-to-PBX interface (CPI), from Digital Equipment Corp. and Northern Telecom Inc. (Nashville, Tenn.) and the digital multiplexed interface (DMI), from AT&T Information Systems. Although CPI is backed by a greater number of companies (including InteCom, Mitel, Rolm, American Telecom, and Prime Computer) and its hardware has been installed in dozens of manufacturers' PBX and computer equipment, it is being challenged by the more recent DMI, which meets the proposed ISDN international standards. The latter has the backing of Honeywell and Hewlett-Packard. Interestingly, some companies, like Wang Laboratories and Data General are backing both interfaces.

Both proposals are similar in that they aim to reduce the cost and complexity of the interface hardware and software needed to move voice and data signals between computers and PBXs. Both also call for a T1 link, which operates at 1.544 Mbits/s. They do differ, however, in their circuit implementations.

How they differ

Specifically, CPI allows 56-kbit/s synchronous transmissions over 24 channels, and the DMI permits 64-kbit/s synchronous transmissions over 23 channels, with an additional channel used for multiplexing signaling information. Also, each proposal has a European version. CPI's consists of 32 channels, and the DMI's comprises 30 channels, plus two more for signaling. Both the CPI and the DMI handle 19.2-kbit/s asynchronous transmissions. Although DMI has a higher synchronous transmission rate, it is prone to data errors at its maximum speed and thus requires the use of a higher-level communications protocol.

One of the largest differences between the two is that CPI is a character-oriented standard and DMI is packet-oriented. Further, CPI can detect and correct errors at up to 9.6 kbits/s, while DMI can only detect them at up to 19.2 kbits/s.

Other than the foregoing performance differences, CPI, as mentioned, has been put to work in

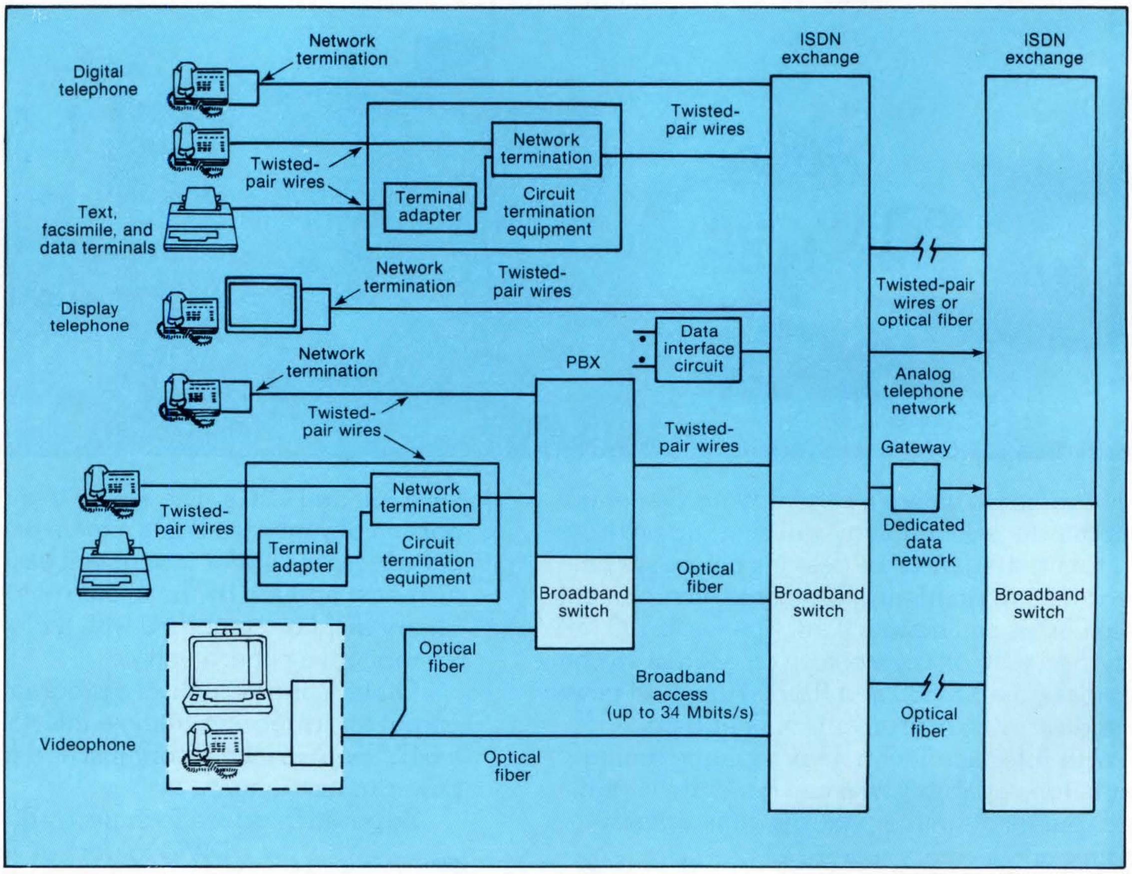
a greater number of settings than DMI—although it is seen by some as a temporary interface that may have to be modified to meet the ISDN standard once it is approved.

The ISDN standard itself is being developed by the International Telecommunication Union's International Consultative Committee on Telegraphy and Telephony (CCITT), located in Geneva. They govern end-to-end digital transmission of voice and data information over PBX-based networks.

The ISDN standard calls for two time-division-multiplexed channels, each capable of carrying 64 kbits/s of voice and data, a 16-kbit/s signaling channel for packet-switched data, and a 48-kbit/s channel for framing the information in the voice and data channels and for resolving contention between network terminals. Thus the standard's total bandwidth is 192 kbits/s. Further, there are provisions that allow up to a 2-Mbit/s bandwidth to be realized, in turn making for some possible competition between PBXs and local networks in the future.

Pick a letter

Different letters in the proposed ISDN standard (S, T, and U) designate the interfaces between a subscriber's telephone or terminal and the central-office switch of the public telephone network. The S interface, for instance, governs the specifications for linking the subscriber's apparatus and the network-terminating point (either a wall outlet in the home or a PBX in the office). This interface takes up the entire



8. Narrowband and broadband systems can coexist within Siemens's Integrated Services Digital Network, dubbed ISDN. Twisted-pair wiring satisfies the requirements for narrowband communications, fiber-optic cables meet the requirements for broadband.

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The T interface governs specifications within the network's terminating point itself. The 144-kbits/s interface (two channels at 64 kbits/s and one at 16 kbits/s) is a sore point between telecommunications and computer manufacturers in the U.S. and in Europe. In the U.S., this interface is generally the responsibility of the local telephone company, which leads U.S. companies to insist that the user need not be concerned with it. In Europe, on the other hand, the users have generally shouldered the responsibility for the interface because of the way that their governments control communications. They argue that the ISDN standard should therefore govern the interface.

Another point of contention is the U interface, which links the network termination point and the central office. Although it has yet to be specified, many European companies are leaning toward a 160-kbit/s bandwidth.

There are other disagreements as well. In Europe, the ISDN proposal calls for data to be transferred at 2.048 Mbits/s. In the U.S., that rate, as noted, is 1.544 Mbits/s. There also are differences of opinion as to what the voltage level of the bit transmitter should be (between 0.5 and 0.7 V) and to the location of a system's power supply. Because of their concern with reliability, Europeans are calling for a central power source. In the U.S., in comparison, manufacturers are arguing that the user should be responsible for the power supply and its placement.

Oil on troubled waters

As a result of all the foregoing differences and disagreements, the ISDN standard is not expected to be adopted until the late 1980s. Nevertheless, work is being done to build bridges and mend fences, and a great deal of progress is being made. So much so, in fact, that nearly every major semiconductor manufacturer in the U.S. and in Europe is eyeing ISDN chips very carefully, and many already have large programs with chips ready to be introduced once the standards become more firm.

Siemens AG (Munich, West Germany) is actively engaged in developing ICs for the CCITT's S and U interfaces and expects to have them ready by late 1986 or early 1987, when field trials for the narrow band (192 kbits/s) ISDN chips will take place. The company has also built both 128-point and 512-point crosspoint space switch chips for the 144-Mbit/s ISDN broadband interface. The space-division approach, rather than time-division multiplexing, was chosen because of the lack of devices fast enough to handle the 144-Mbit/s signals encountered in broadband ISDN systems. The company is also working strongly on the development of multifunction voice and data terminals that will conform to the ISDN S, T and U interfaces and plans to have them ready within one to two years.

Siemens sees both narrow band and broadband digital communications existing side by side within one large and totally integrated network (Fig. 8). Twisted-pair wiring would satisfy the former's requirements; fiber-optic cables, the latter's.

As part of its broadband ISDN fiber-optic efforts, Siemens is field testing Siconet, an integrated communications system that will conform to ISDN standard. The network, which links as many as 92 devices—27 video telephones, 60 digital telephones, and 5 telex terminals—is being tested at Siemens's Hoffmanstrasse facility (Munich).

The company is also conducting field trials for the technical evaluation of its broadband integrated fiber-optic local network, known as BIGFON. The network integrates data, voice, video, TV, and broadcast stereo signals.

Fiber-optic cables will eventually play leading roles in all types of local- and wide-area networks, particularly as advances bring better fibers and more reliable components like taps, multiplexers, connectors, light sources and receivers, splitters, transceivers, and modems.

Bus networks like Ethernet, for instance, can now be readily converted into fiber-optic systems like the Fiber Optic Net/One, from Ungermann-Bass Inc. (Santa Clara, Calif.). Currently, the company is the only one making a complete fiber-optic local network. Other manufacturers offer only the transceiver or some other parts, but not the total system. □

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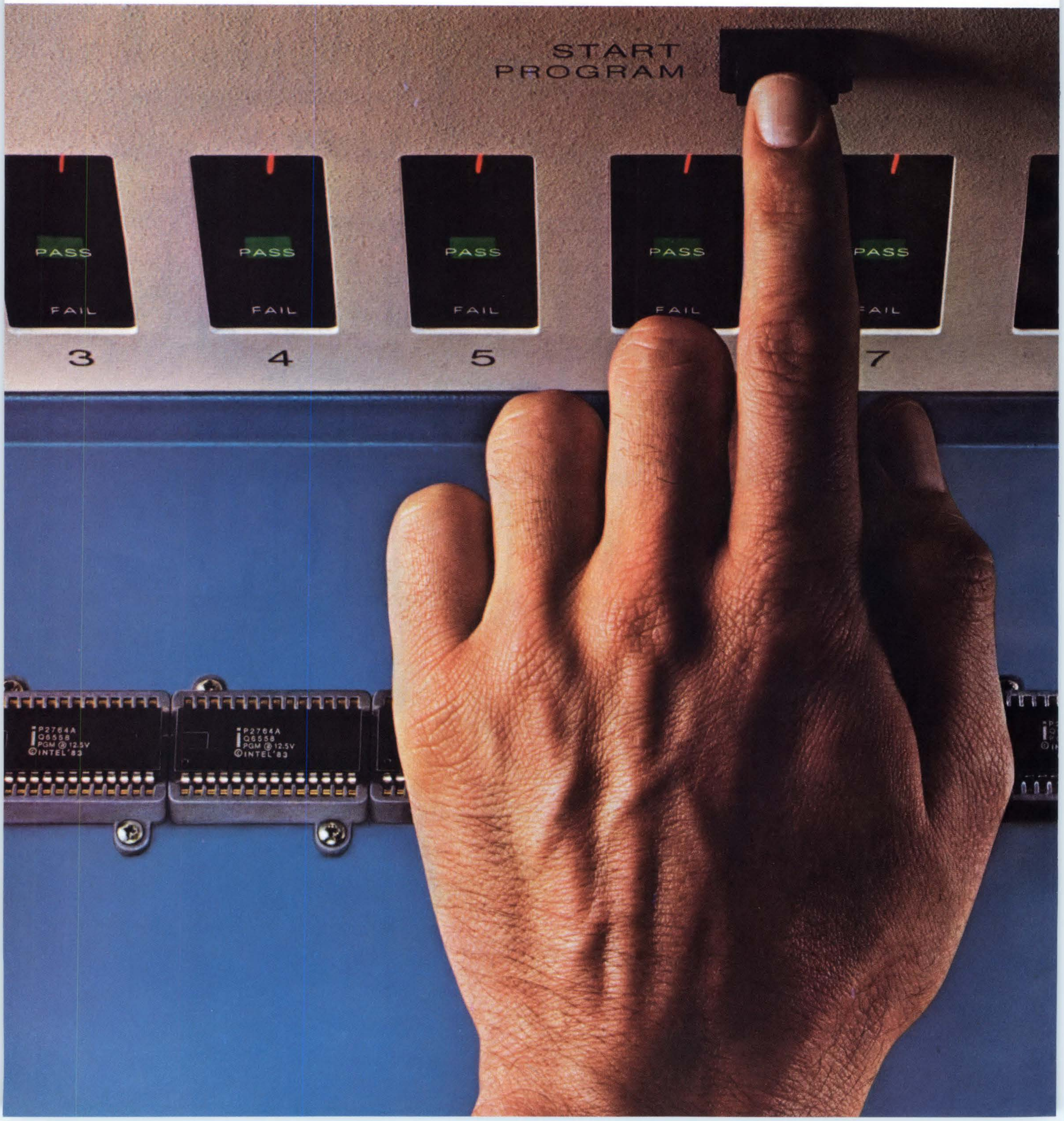

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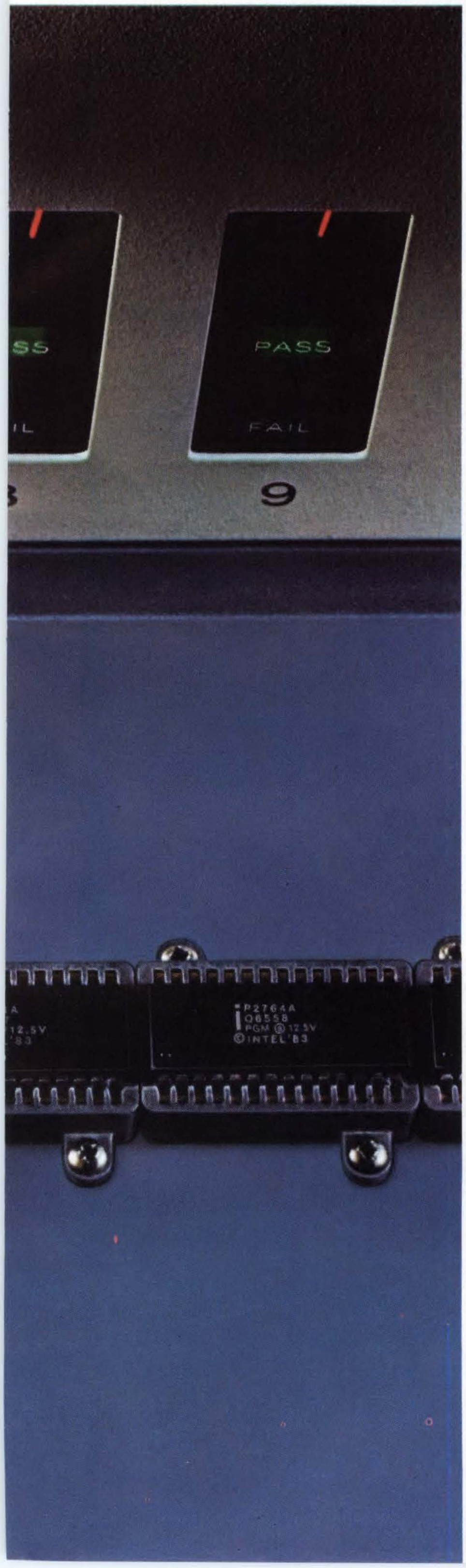

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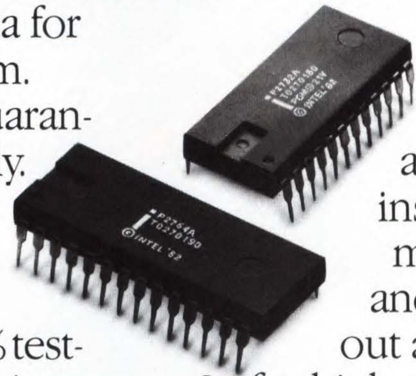

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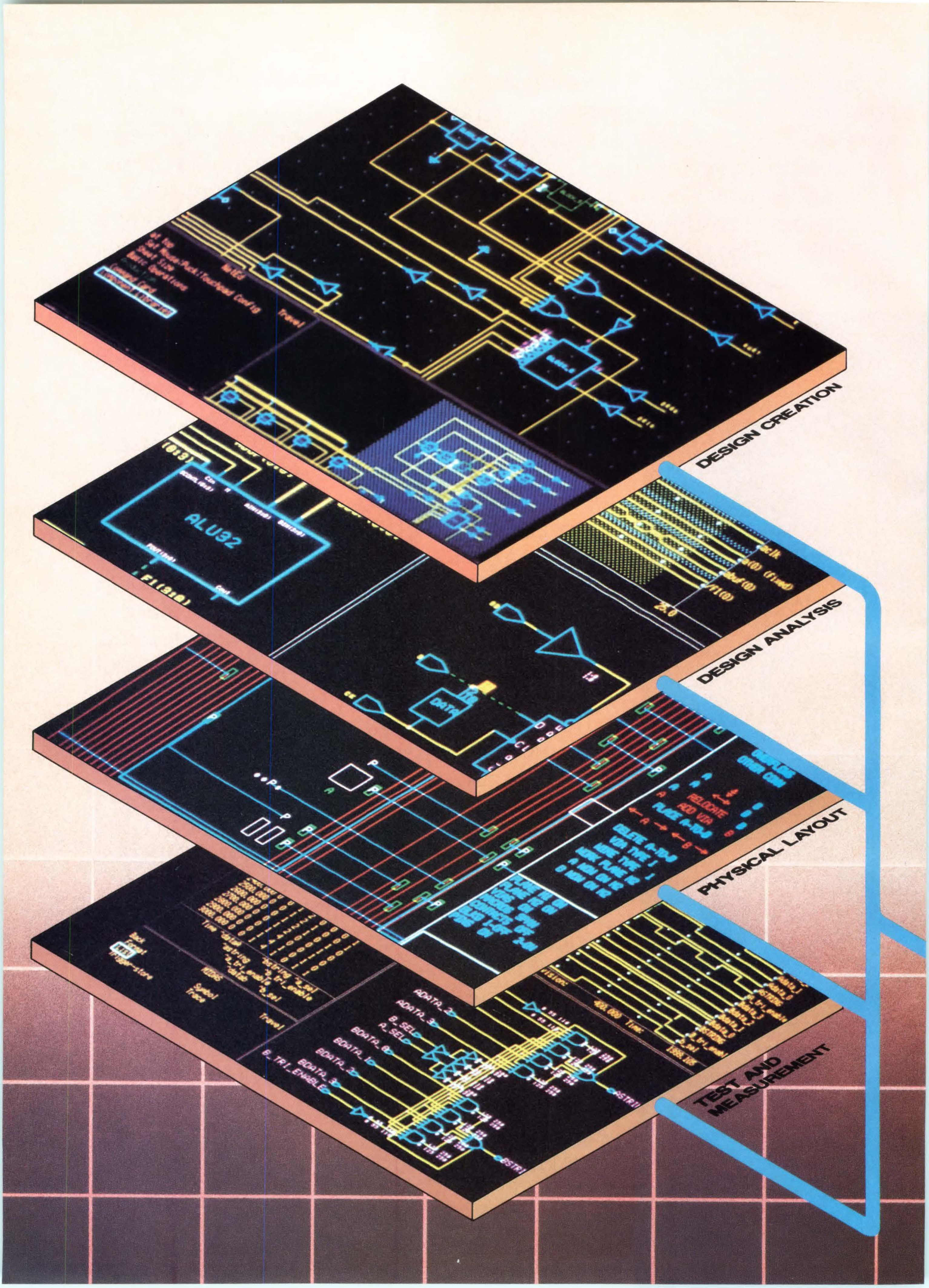
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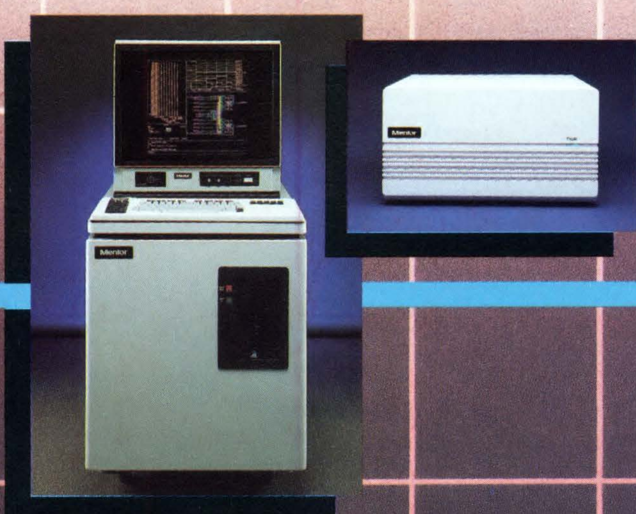

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CIRCLE 72

DESIGN ENTRY

Bit-oriented coprocessor resolves incompatibilities of small and large networks

One chip combines a 4-Mbit/s data link controller with a channel processor that interfaces with the host system at up to 10-MHz bus clock rates.

As local networks proliferate, they will increasingly be asked to communicate with one another over long distances. Indeed, the disparate requirements of local and wide-area data communications have already been anticipated—and integrated—in such network standards as IBM's Systems Network Architecture (SNA) and the CCITT's X.25 protocol. Similar coherent solutions could soon become a universal design goal.

Pradip Madan, Wen Huang, Chris Kao, and **Arthur Yu,** Exel Microelectronics Inc.

Pradip Madan, product marketing manager of microprocessors and peripherals, joined Exel Microelectronics in San Jose, Calif., in 1983. He previously worked with Intel and LSI Logic and holds BS degrees in physics and electrical engineering, an MS in computer science, and an MBA.

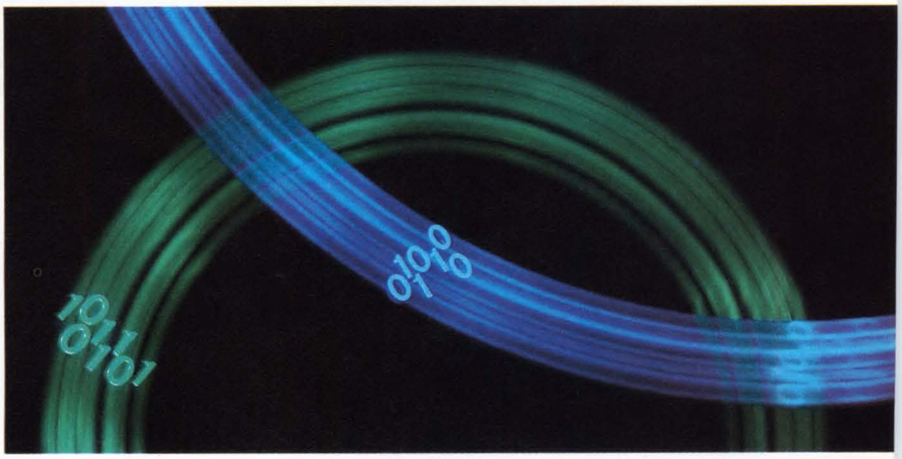
Wen Huang, a member of Exel's technical staff, has also designed communications controllers at Advanced Micro Devices. He has worked at Intel and Fairchild, and he holds a BS and an MS in electrical engineering.

Chris Kao, also a member of the technical staff, joined Exel last year, after holding positions at Fairchild and Intel. He has a BS and an MS in electrical engineering.

Arthur Yu, another technical staff member, is involved with interface logic. Earlier he worked for Qume and Intel. He holds a BSEE.

The development of a VLSI component that can simultaneously serve both local and wide-area networks entails reconciling somewhat different and even conflicting objectives. First, local links typically operate at higher bandwidths than the other type of system, largely because of the tradeoff between distance and the frequency and complexity of transactions.

Second, being smaller and more numerous, local networks are more cost-sensitive than the wide-area kind, rendering low component count, simple software, and ease of manufacture paramount concerns for the designer. Third, since wide-area networks involve complex routing and usually serve a highly diverse set of user requirements, their link management software is more complex than local soft-



ware and could benefit from high-level silicon support.

From a VLSI designer's standpoint, the three requirements diverge. Nonetheless, they are all met by a bit-oriented communications coprocessor (BOCC), a chip that handles protocols like HDLC, SDLC, and ADCCP, as well as such variants as the HDLC-based CCITT X.25 (see "Bit-Oriented Protocols Unraveled," below).

Fabricated with a two-layer metal HCMOS process that affords high density and low power consumption, the coprocessor comes in two versions—the XL88C585 and the XL68C565—and will be housed in a 48-pin package. In terms of internal circuitry, the chip actually comprises two processors: a data-link controller that can operate at a higher data rate of 4 Mbits/s and a channel processor—with a built-in DMA controller—that works at bus clock rates of up to 10 MHz (Fig. 1).

Several factors contribute to the communications coprocessor's cost-effectiveness. Its system interface can be tailored for different CPUs, memory sizes, and bus widths. Furthermore, its integrated channel processor obviates the need for an external DMA controller and other logic, thereby simplifying system hardware. The preprogrammed buffer management microcode simplifies message and buffer man-

Bit-oriented protocols unraveled

Among all protocols for wide-area or local networks, bit-oriented protocols have reached the highest levels of standardization and stability (with the possible exception of CSMA/CD, for carrier-sense multiple access with collision detection). They are amenable to low-cost implementations, thanks to the established base of hardware and software, as well as the broad selection of speeds, communication media, link-layer subset protocols, and higher-level configurations.

The frame forms the basic communication unit in bit-oriented protocols, in which the beginning and ending frame-synchronization flags enclose an address, a control, and an information field, plus a 2-byte frame check sequence field, which is used for error detection. To prevent the flag pattern (01111110) from occurring unintentionally within a frame, the transmitter automatically inserts a 0 every time it detects five consecutive 1s in any field (except a flag field). At the destination, the receiver automatically removes the 0. Thus six consecutive 1s are transmitted only in flags and in certain special characters, like idle and abort.

Leading today's list of bit-oriented protocols for local and wide-area networks are HDLC (High-level Data Link Control), backed by the International Standards Organization; ADCCP (Advanced Data Communications Control Procedure), advocated by the American National Standards Institute; and IBM's SDLC (Synchronous Data Link Control).

All three cover a broad range of speeds and take care of encapsulating frames, controlling interfaces and errors, and routing signals throughout the systems. Nevertheless, they differ in certain respects. First, HDLC and ADCCP work with extensible address and control fields. When the least significant bit in either kind of field is set to a 0, it indicates an extension byte. The address field may be lengthened indefinitely, but the control field may only be extended by one 8-bit word. Also, the information field in HDLC and ADCCP implementations may contain any number of bits. In contrast, SDLC permits only a single 8-bit word in the address and control fields, and it restricts the information field to an integral number of 8-bit groups. In addition, it uses a frame-checking sequence of only 16 bits, whereas HDLC and ADCCP employ 16 or 32 bits.

Except for commands pertaining to the loop mode, which only SDLC possesses, all three protocols boast similar data-link commands. Commands belonging to SDLC's other operational modes form a subset of the three modes specified in HDLC and ADCCP. SDLC accommodates only unbalanced normal responses, HDLC and ADCCP supplement that with unbalanced asynchronous and balanced asynchronous responses.

Some of the commands and character formats vary. For example, the HDLC abort character comprises seven contiguous 1s as opposed to eight in SDLC. In fact, the SDLC protocol recognizes seven 1s following a 0 as the End of Poll command for its loop configuration. Without a loop mode, the HDLC and ADCCP protocols obviously suffer no such confusion.

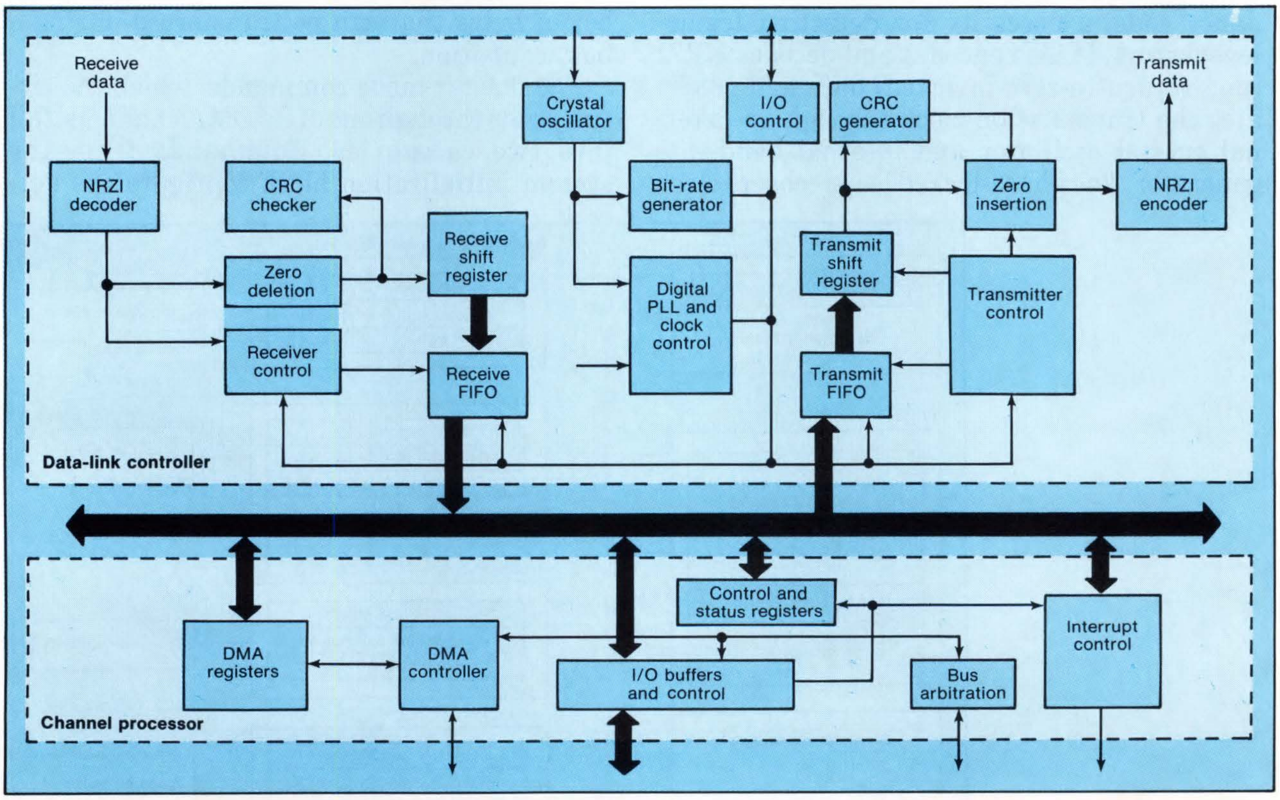
Whereas open-ended local networks must adhere to standards like the token-passing bus or CSMA/CD (or /CA—collision avoidance), the bit-synchronous characteristics of most bit-oriented protocols are well suited both to closed local clusters and subnetworks and to wide-area systems.

agement software.

The coprocessor is architecturally designed for concurrent operation of the data-link controller and the channel processor. With such a structure, the coprocessor can handle asynchronous timing between the host and network interfaces.

The on-chip channel processor includes an intelligent four-channel DMA controller, which is microcoded for flexible buffer management, and logic for arbitrating bus exchanges and for controlling interrupts. With the integrated interrupt logic, the circuit can detect user-programmable internal conditions and can direct host responses, through vectors, to the appropriate service routine. Together the channel processor's circuits let the coprocessor share the host system bus, aided by only a few external parts. Additionally, the chip can communicate rapidly and adaptably with a host CPU through a shared memory block, or mailbox.

The channel processor, controlled by a microprogram within the DMA controller, automatically manages linked lists of free and full buffers and also transfers frames between the on-chip FIFO registers and external memory through the DMA controller. With data traffic evolving from message to file transfers, the ability to handle back-to-back frames continu-



1. With two separate on-chip processors serving high-speed serial and parallel interfaces, the bit-oriented communications coprocessor can handle network data at up to 4 Mbits/s. The channel processor contains a DMA controller (with 24-bit addressing) that manages the I/O buffers through on-chip microprograms.

ously and quickly without overloading the host CPU or degrading system performance is becoming even more critical. With the integrated channel processor, the device can transfer 128-byte frames at the rate of 3000 frames a second—without real-time intervention of the host CPU.

As for the serial data-link controller, its digital phase-locked loop and built-in data link control intelligence allow a simple and quick link controller design. With a simple transceiver, an inexpensive local link can be established over twisted-pair cable.

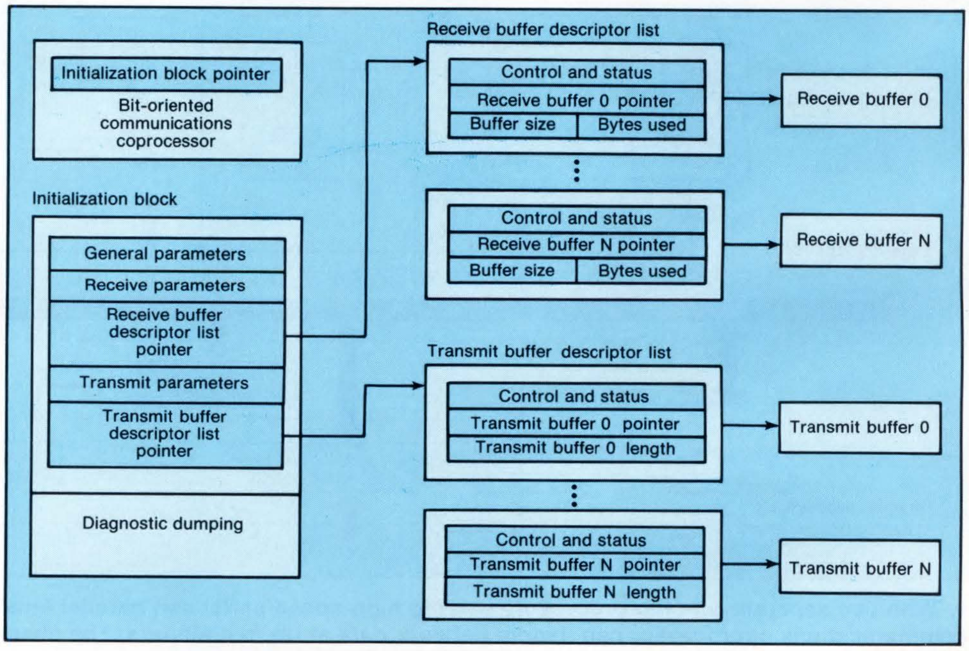
Like similar circuits, the data-link controller handles automatic insertion and deletion of zeros and generates and checks cyclic redundancy code, a necessity for detecting frame-level errors. It also encodes and decodes NRZI (non-return-to-zero inverted) data and generates the transmission clock through an external crystal oscillator and internal baud-rate generator. The phase-locked loop recovers clock signals from the incoming data stream, and separate transmit and receive FIFO buffers synchronize data flowing between the chip's data-link controller and the channel processor.

Operational agility

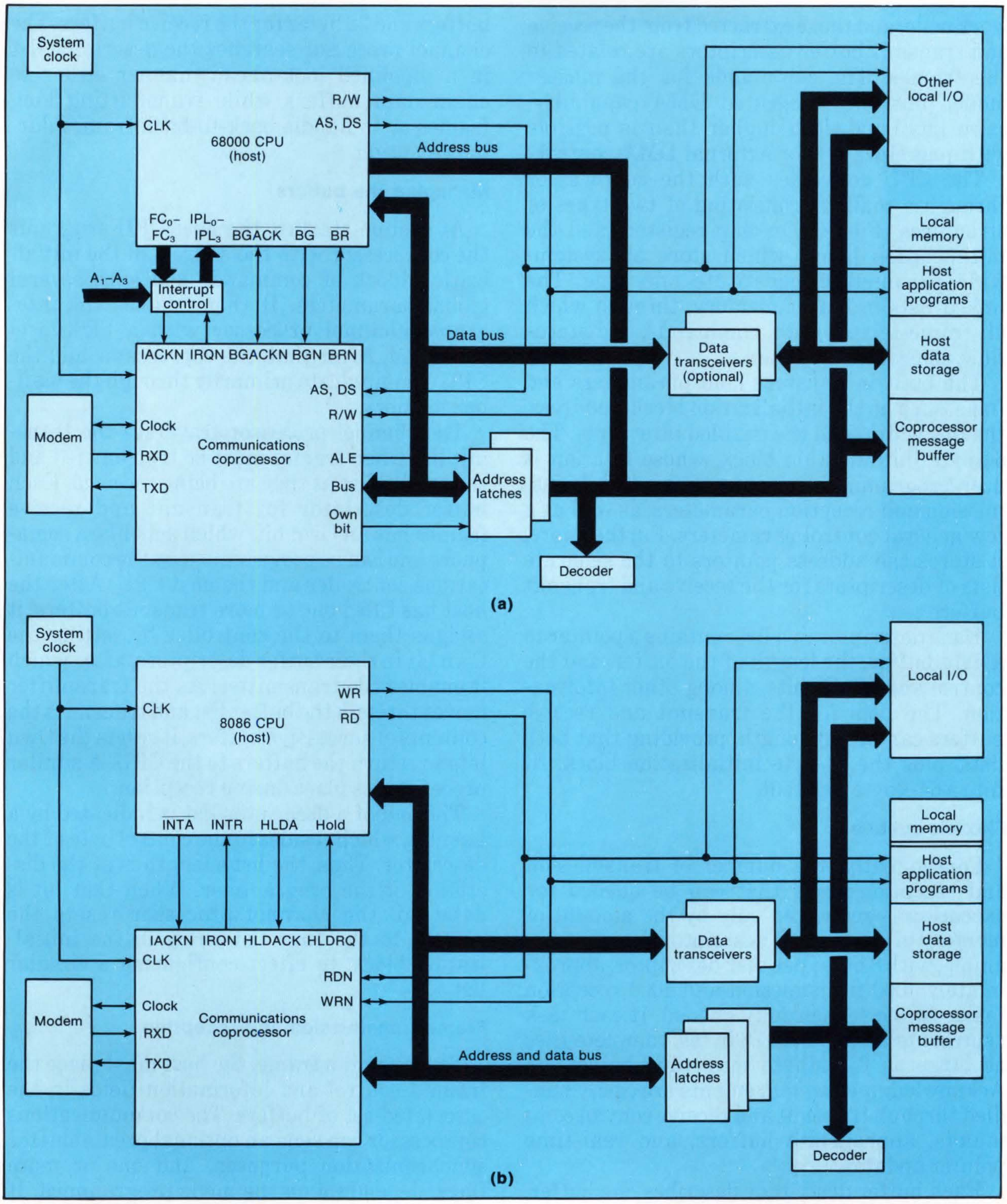
The communications coprocessor chip acts as a master or a slave or remains in an idle state. As a slave, it has its chip-select or interrupt-acknowledge input asserted by the host. The slave commands supply sophisticated management and control of both the link and the system.

To become bus master, the chip employs a simple sequence for requesting and granting the bus. The user programs the maximum number of bytes that can be transferred during a bus acquisition.

The master mode commands, which the circuit reads through one of its DMA channels, fall into two categories. Commands from the system initialization block configure the net-



2. Apart from some vital initialization parameters and error information, the communications coprocessor and the host exchange all messages and commands through a shared memory.



3. Tailored signals like BRN (Bus Request), BGN (Bus Grant) and BGACKN (Bus Grant Acknowledge) make the bus arbitration circuitry between the communications coprocessor and the 68000 microprocessor extremely simple (a). When the chip interfaces with an 8086 CPU, HLDRQ and HLDACK (Hold Request and Hold Acknowledge) serve as the direct bus exchange handshaking signals with the CPU's Hold and HLDA signals in the minimum system configuration (b).

work node, and those extracted from the receive and transmit buffer descriptors are related to the frames. The commands for the master mode, plus the integrated DMA capability, raise bus bandwidth higher than is possible with just slave I/O or external DMA control.

The CPU converses with the coprocessor through a mailbox consisting of two types of structures (Fig. 2). On-chip registers and the initialization block, which store all system-wide parameters, constitute one type. The linked lists in buffer memory, through which all frame-related data, commands, and status flow, constitute the other.

The built-in registers hold parameters and flags, such as the initialization block's address, the bus width, and the enabled interrupts. The 64-byte initialization block, whose location is user-programmable, contains several transmission and reception parameters, as well as a few general control parameters. Furthermore, it stores the address pointers to the separate lists of descriptors for the receive and transmit buffers.

Each descriptor in a list contains a pointer to a data buffer, the length of the buffer, and the control and status bits, among other information. The lists for the transmit and receive buffers can be any length, providing that both lists, plus the 64-byte initialization block, fit into a 64-kbyte segment.

Flexible queues

Consequently, the number of transmission and reception tasks that can be queued for execution is restricted only by the amount of memory given to their descriptor lists. For example, with 8 bytes per task descriptor, approximately 4000 transmission and 4000 reception tasks can be sequentially queued. If each task represents a frame of 128 bytes, complete files as large as 0.5 Mbyte may thus be set up. Acknowledgment requirements are easily handled through transmit and receive control commands, appropriate buffers, and real-time pointer updates.

Each buffer descriptor describes one buffer, and successive buffers can be concatenated for longer frames. Also, the user can specify the length of each buffer to an 8192-byte maximum—in increments of 1 byte for the transmit buffers and 32 bytes for the receive buffers. The channel processor searches the descriptor list in a pipelined look-ahead manner either to chain data buffers while transmitting long frames or to handle back-to-back frames during reception.

Managing the buffers

At system startup, the host CPU programs the coprocessor with the address of the initialization block of commands and with several global parameters. It then enables the integrated channel processor with a high-level command. After that, the coprocessor and the CPU communicate primarily through the mailbox memory.

The channel processor traverses the transmit list when frames must be transmitted and the receive list as they are being received. Each buffer descriptor for transmit and receive frames has an Own bit, which acts like a semaphore and can be programmed by the communications controller and the host CPU. After the host has filled one or more transmit buffers, it assigns them to the controller by setting the Own bit in their buffer descriptors, after which it enables the transmitter. As the transmitter moves through the buffer list and transmits the contents of successive buffers, it resets the Own bits to return the buffers to the CPU. A similar process takes place during reception.

The end of a descriptor list is indicated by a Last bit, which resides in the control byte of the descriptor. Thus, the list's length is at the discretion of the programmer. When that bit is detected, the channel processor resets the pointer to the first list entry in the initialization block, in effect configuring a circular list.

Frame transmission and reception

To transmit a frame, the host must place the frame's control and information fields in the associated set of buffers. The communications coprocessor can send an optional preamble (for synchronization purposes) and one or more flags, depending on the mode programmed. It then accesses the data buffer specified in the descriptor and transmits the number of bytes indicated. Besides that, it accumulates and appends the CRC (if programmed), as well as the

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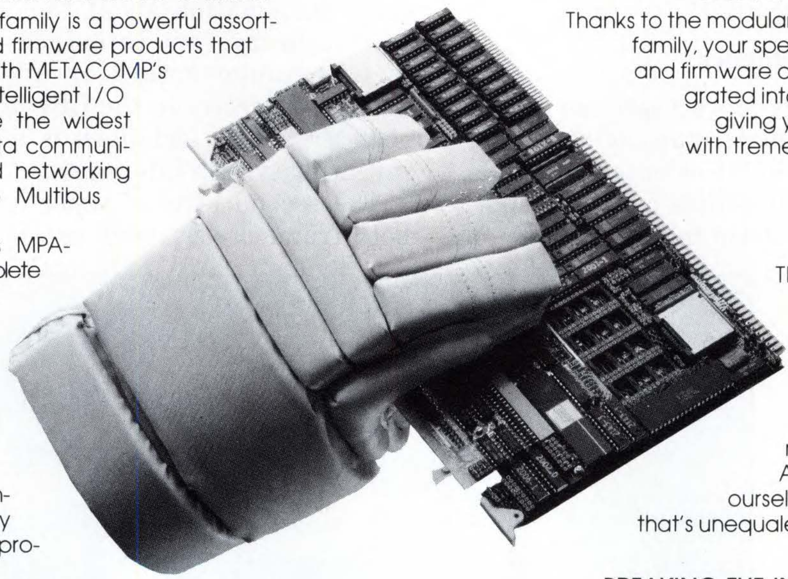

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CIRCLE 73

closing flag. If the frame is transmitted successfully, the controller resets the Own bit in all descriptors associated with that frame, thereby returning free buffers to the CPU.

The communications coprocessor can be programmed to receive a frame in several ways. It can be set to respond only when it detects a match with the station address or the group address or when it detects a broadcast address, or it can be set to receive all frames (primary mode). Once set, the chip checks the address on the incoming frame and places the entire message in the designated buffers. The receiver computes the CRC on the incoming frame. The buffer descriptor is updated with the number of bytes obtained in the frame, the error status, and the status of the buffer's Own bit when the frame is completely received.

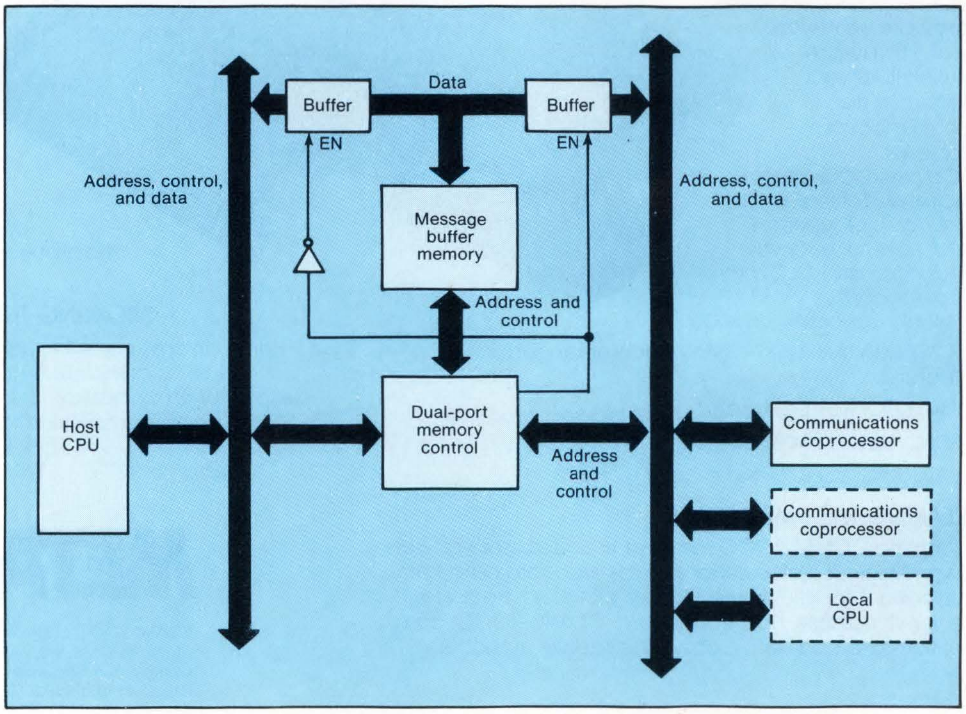
Protocol support possibilities

The communications coprocessor can be programmed to accommodate many of the frame format options found in bit-oriented protocols. For instance, the address field can be as short as 8 bits or extended indefinitely in multiples of 8 bits, and the control field may be one or two 8-bit words. In addition, the optional preamble can be sent before the opening flag, allowing the receiving station to synchronize itself with the data stream.

What's more, the characters in the information field can be set for lengths of 5 to 8 bits for both the receiver and the transmitter. During receiving or transmitting, the device automatically switches to the programmed character length at the beginning of the information field. Additional protocol support comes in the form of the detection and generation of flag, abort, and idle bit patterns.

The controller reports status and error conditions in two ways. The first one, consistent with link-level requirements, sends status and error information about the transmitter, receiver, or system interface—for instance, bus exchange errors or unavailable data buffers—directly to the CPU through on-chip registers. That technique is also suitable for initiating system interrupts.

The second level of reporting encompasses both frame status, such as residual character



4. A dual-port memory controller supplies all the address, data, and control signals, as well as the memory refresh signals, that permit multiple communications coprocessors and the host to share the message buffer memory.

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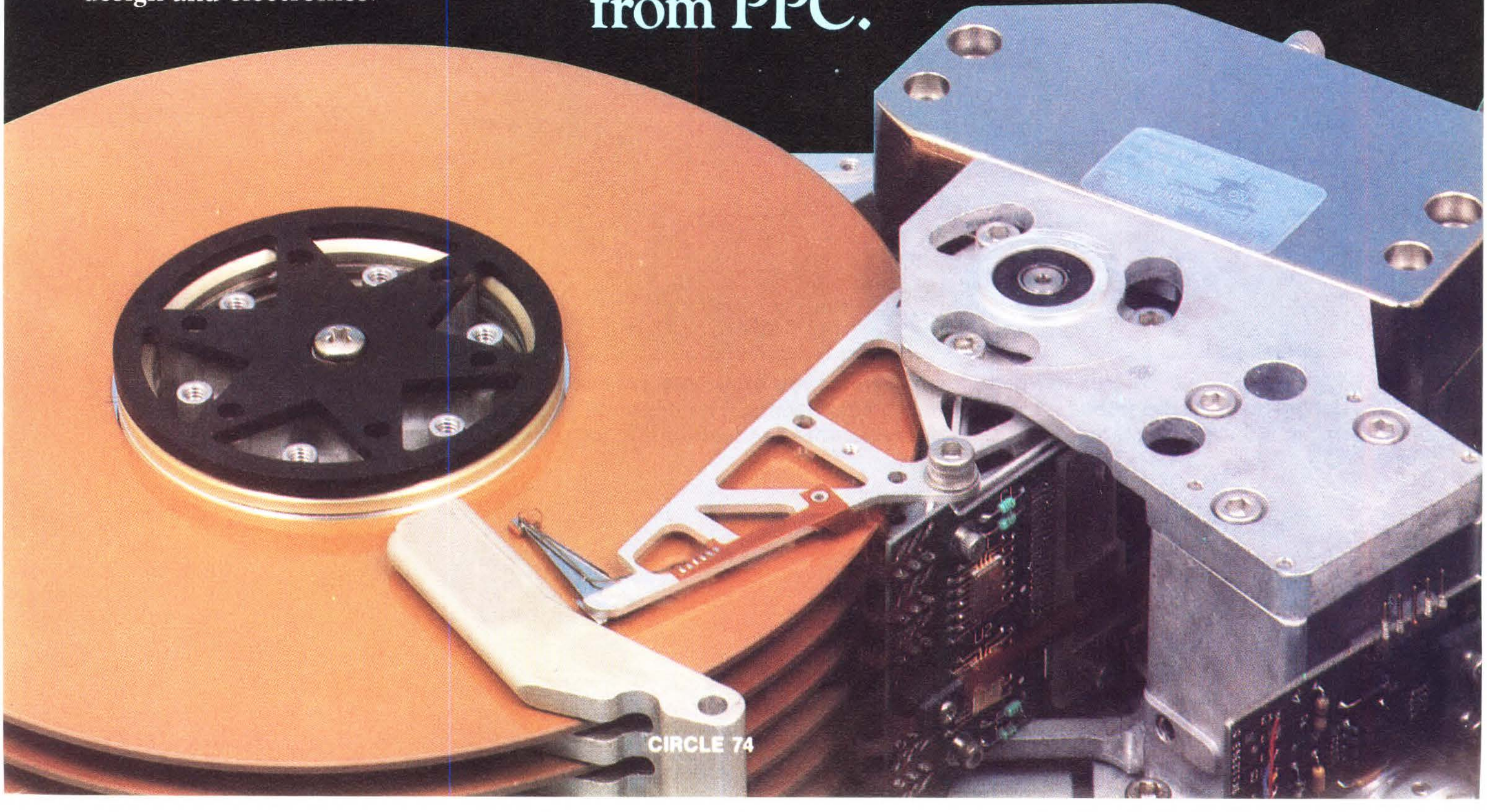


lengths, and exception conditions, like a CRC error or the receipt of an abort character. These reports are held in associated buffer descriptors.

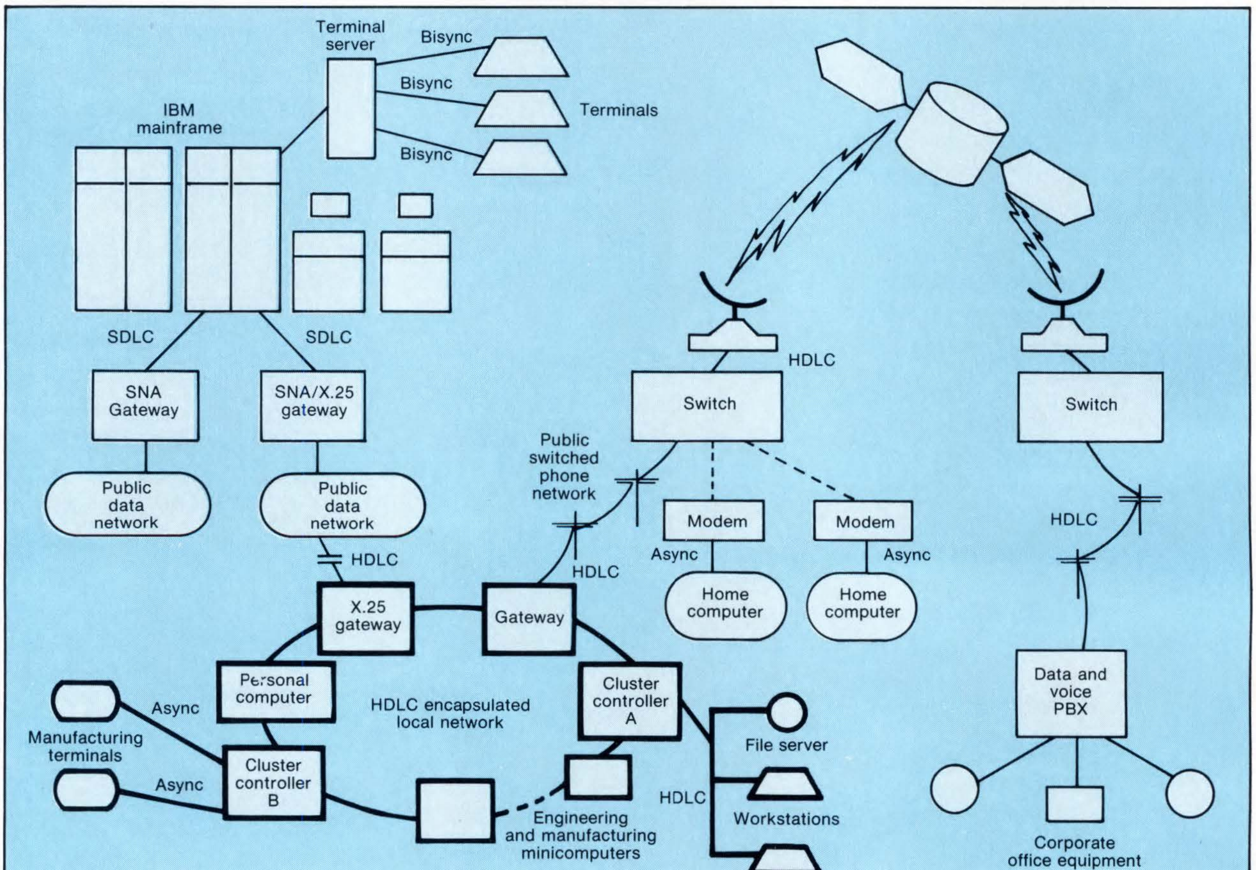
Diagnostics included

The coprocessor also incorporates several link and system diagnostic aids. For example, the chip can be commanded to dump its internal registers and status information into memory. Further, to assist local diagnostics it can be programmed for local loopback through the receiver.

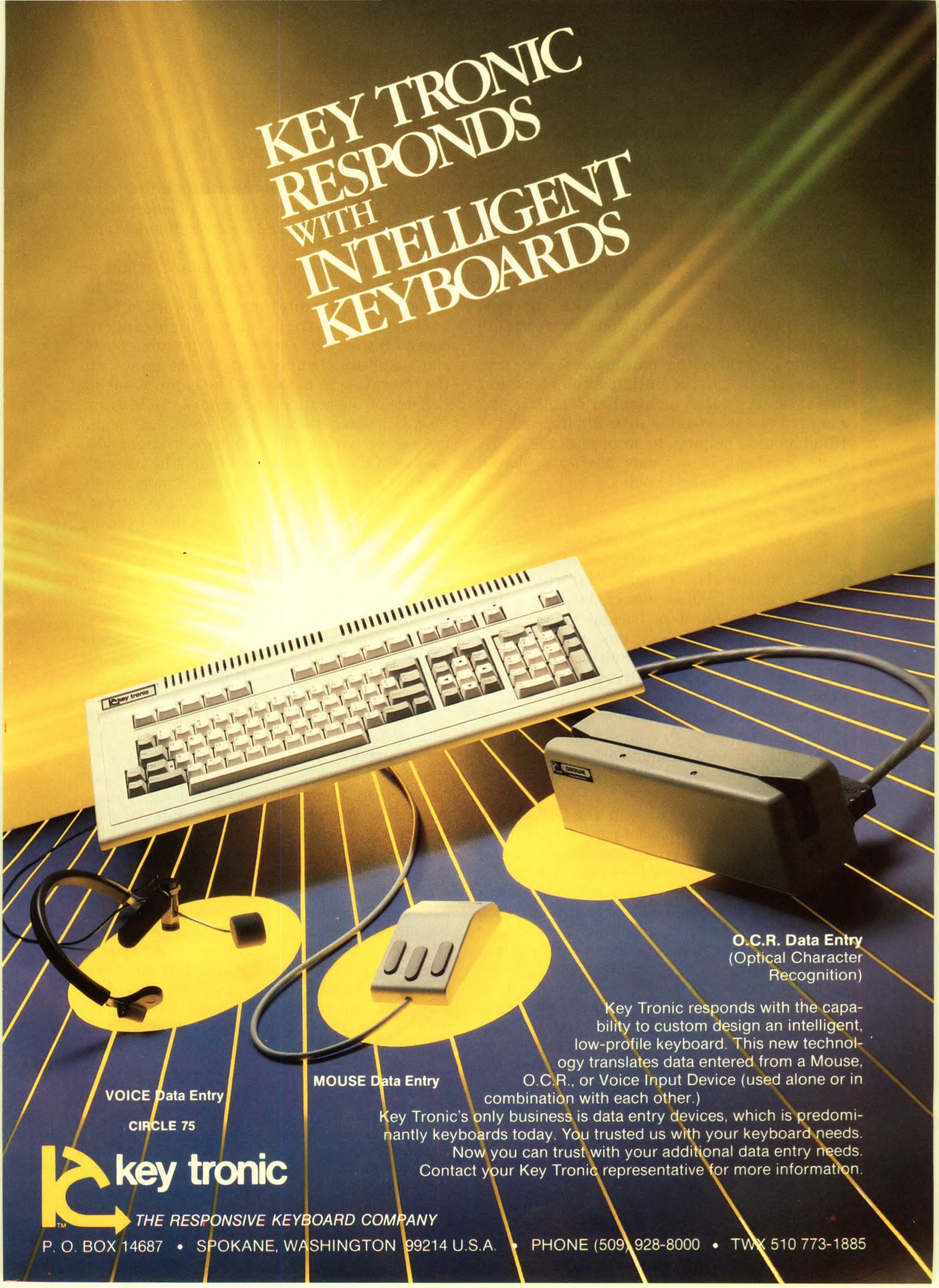
The design of the communications coprocessor meets two hardware goals. First, its interface easily meshes with a variety of host CPUs. Second, the circuit holds enough arbitration functions to facilitate efficient configuration of multimaster systems.

Addressing the first goal are the two versions of the controller: the XL68C565, which is optimized for the 68000 microprocessor family, and the XL88C565, which is geared for the iAPX 86, 88, 186, and 188 families; the MCS-85; the MC6800; the Z80, Z800, Z8000, and Z80000; and the NS16000 series, among other 8-, 16-, and 32-bit CPUs.

For the second goal, all bus exchange and



5. In a typical wide-area network, local systems are often interconnected through gateways to public data networks or to the public switched telephone network. The communications coprocessor would be an appropriate choice for establishing the high-level serial links within the local (tint) and the wide-area systems.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system controls—except logic for multimaster arbitration, address decoding, and bus buffering—are put on chip. In the absence of other bus masters, the bus exchange schemes are extremely simple (Fig. 3). For higher-performance CPUs that require greater bus bandwidth, dual-port configurations can be used with multiple communications coprocessors (Fig. 4).

Other general system parameters can be programmed through the initialization block. For instance, the DMA controller's addressing range can be selected for 16 or 24 bits, with the 16-bit choice helping to minimize the DMA cycle overhead in systems having a shared memory of less than 64 kbytes.

Network topology choices

The protocol controller operates in several network topologies. For instance, one chip can act as a master (HDLC nomenclature), or primary station (SDLC nomenclature), while several others serve as backup masters and slaves, or secondary stations; the resulting system can operate as a multidrop network, with station and group addresses suited to the network's requirements.

In a star configuration, slave stations on the spokes of the network communicate point to point with master communications controllers at the hub. The host CPU directs the traffic among the spokes.

The chip can also work in the SDLC loop mode, one of the simplest forms of local network. The loop is essentially a ring consisting of any number of slave stations plus one master station, whose operation is handled by a controller in the normal SDLC mode. Unaddressed slave station chips, programmed for the loop mode, automatically implement the required 1-bit pass-through repeater delay while the on-chip PLL recovers the clock. Special commands built into the protocol controller permit a node to get on and off the network without disturbance, even when the network is active. The chip can also be programmed to echo the data passively in an inactive mode.

A wide-area network can actually be formed by a hierarchy of different types of local networks (Fig. 5). As part of such a complex system, an encapsulated HDLC local network might run through an entire building connecting different subnetworks of equipment, each piece of which could use a communications coprocessor.

Cluster controller A, for example, might be implemented with two coprocessors that together access a multidrop subnetwork of engineering workstations and a high-capacity shared file server. The chip on the subnetwork side would act as a master and as the gateway to the parent local network. The coprocessor on the side of the main local network would interface with slave stations. Each workstation and file server within the subnetwork might also use one of the coprocessors. In fact, the system's number of nodes can be increased indefinitely by extending the addressing on the subnetwork—without the need to modify existing hardware in the cluster controller.

In addition, manufacturing terminals can be connected to cluster controller B, over point-to-point links, giving them access to a manufacturing minicomputer over the local network. The terminals can use either asynchronous protocols for low cost or the HDLC protocol for error-immunity in a noisy environment. In the latter case each terminal would communicate with the network through a communications coprocessor.

For process control, a multidrop token-passing scheme using HDLC at 4 Mbits/s would be practical. Controlled access through tokens guarantees network stability, while HDLC's error control keeps error rates low.

If any of these network environments are closed (in other words, compatibility with a different protocol is not an issue), using the communications coprocessor would give the system designer a much lower chip count and cost per node than if another local network alternative were used. Typical LSI solutions distribute the functions of clock recovery, data reception and transmission, and frame management among two or three devices, raising cost considerably.□

How useful?	Circle
Immediate design application	541
Within the next year	542
Not applicable	543

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Plain English Error Messages—

System requirements for all programs: Z-80 CP/M 2.2 System with 54k TPA and at least a 96 column printer is recommended. Or 8086/88 256k CP/M-86 or MSDOS (PCDOS).

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	Z-80 CP/M®	ZILOG SYSTEM 8000 UNIX	IBM P.C. 8086/88 MSDOS	IBM P.C. 8086/88 CP/M 86	OLIVETTI M-20 PCOS
8086/88 ASM			$ 99.50	$ 99.50	
8086/88 XASM	$199.50	$750.00			$199.50
16000(all) XASM *new*	199.50	750.00	199.50	199.50	199.50
68000 XASM *new*	199.50	750.00	199.50	199.50	199.50
Z-8000(TM) ASM		750.00			299.50
Z-8000 XASM	199.50		199.50	199.50	
Z-80 ASM	49.50				
Z-80 XASM		500.00	99.50	99.50	99.50
Z-8 XASM	99.50	500.00	99.50	99.50	99.50
6301(CMOS) *new*	99.50	500.00	99.50	99.50	99.50
6500 XASM	99.50	500.00	99.50	99.50	99.50
6502 XASM	99.50	500.00	99.50	99.50	99.50
65CO2(CMOS) XASM *new*	99.50	500.00	99.50	99.50	99.50
6800,2,8 XASM	99.50	500.00	99.50	99.50	99.50
6801,03 XASM	99.50	500.00	99.50	99.50	99.50
6805 XASM	99.50	500.00	99.50	99.50	99.50
6809 XASM	99.50	500.00	99.50	99.50	99.50
8748 XASM	99.50	500.00	99.50	99.50	99.50
8051 XASM	99.50	500.00	99.50	99.50	99.50
8080 XASM	99.50	500.00	99.50	99.50	99.50
8085 XASM *new*	99.50	500.00	99.50	99.50	99.50
1802 XASM *new*	99.50	500.00	99.50	99.50	99.50
F8/3870 XASM *new*	99.50	500.00	99.50	99.50	99.50
COPS400 XASM *new*	99.50	500.00	99.50	99.50	99.50
NEC7500 XASM *new*	99.50	500.00	99.50	99.50	99.50
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Twisted-pair bus carries speech, data, text, and images

A serial bus optimized for both speech and data traffic can make a low-cost network for integrated communications services a reality.

If any one characteristic can be said to dominate currently available local-area networks, it is efficient data transfer. That is all well and good, except for integrated communications networks, where traffic consists mainly of digitized speech. In the foreseeable future, in fact, speech traffic will become increasingly important, so that communications networks will have to be as efficient in transferring digitized speech as in transferring data.

In addition, a digital network for general-purpose communication must be able to transmit other types of information as well; interface easily with telephone sets and existing networks; use a low-cost transmission medium; and of course connect to almost all types of equipment commonly found in factories, offices and so on.

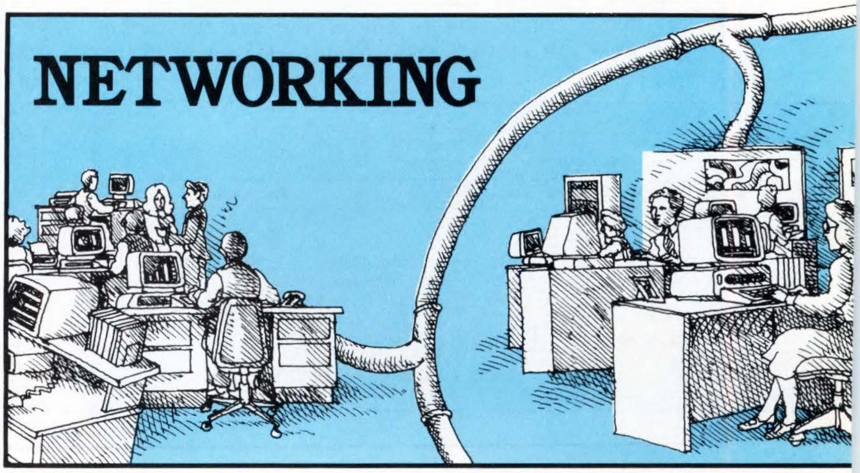
All these requirements are met by the Integrated Services Terminal (IST) bus, which forms a low-cost local network for transmitting digitized speech, data, text, and facsimile copies. A serial bus, it conforms to the seven-layer Open Systems Interconnection reference model of the ISO and uses twisted-pair cable to carry 64-kbit channels synchronized to the 8-kHz speech sampling frequency.

The IST bus provides distributed switching and control and offers several major benefits over current telephone, intercom, and small PBX systems. It can be interfaced with larger networks such as digital or analog PBX, public telephone, Telex, and data networks, and higher-performance (local and wide-area) networks.

The first applications will be for small, internal communication systems that primarily handle speech. Here, subscribers require very

Wouter Bourgonje
Philips International BV

Wouter Bourgonje shared in the design of the IST bus at Philips's Electronic Components & Materials (ELCOMA) Division in Eindhoven, the Netherlands, where he now works as system architect and project coordinator for ISDN terminals. He received his technical education at NV Hollandse Signaal Apparaten and previously worked for Philips in Norway and at the ELCOMA Division's Central Applications Laboratories.



Networking: Twisted-pair serial bus

few lines (often only one) to the public network, and the IST bus will form an economical and versatile communications medium. In addition, the bus's data, text, and telemetry facilities will allow factories, offices, retailers—and even consumers—to connect telephone sets, personal computers, intercoms, word processors, and viewdata and point-of-sales terminals, as well as lighting, heating, and security equipment.

Twisted-pair cables

The twisted-pair cable of the bus gives high speech and data transfer rates at low cost for the wire, installation, connectors and coupling transformers. The transmission speed is 1.024 Mbits/s, the maximum bus length 350 meters. Depending on the type of cable used, the characteristic impedance of the line can be between 100 and 150 Ω.

Each station is connected to the bus bv an interface circuit and has a microcontroller, called the station controller (Fig. 1). The only other circuits needed are those which provide the services at each station.

As many as 30 stations may be connected either in a cluster or spread along the cable, and a dc power supply can be connected directly to the bus to provide up to about 0.5 W to each station. A small transistor splits the dc supply and the digital bus signals. Alternate mark inversion (AMI) line code, which reverses the polarity of each successive 1 to ensure no dc component, prevents the coupling transformer from distorting the signals.

Both circuit-switched and packet-switched data can be transmitted across the bus. In a circuit-switched channel, a connection between the calling and called stations is established for

The rules for control and message packets

The IST bus uses a protocol for its packet-switched channel that closely resembles HDLC (High-level Data Link Control). One important difference is that each byte of data transferred over an IST bus channel is preceded by a 1 (the start bit), as long as information is transferred in a channel, whereas HDLC uses flag bytes to indicate the start and end of a data packet. Another is that the first bit of the first byte indicates whether the message being transferred consists of information (I) or control (C) characters (see the figure).

Control characters are transmitted by a station in the form of a seven-bit frame control message (FCM), the main uses of which are to arbitrate between stations wishing to make a connection to the eight circuit-switched channels and to set up the physical link (layer 1 of the ISO's seven-layer reference model) between the stations.

Before connecting to one of the circuit-switched channels, a station must first take control of the packet-switched channel by transmitting a frame control message (to prevent circuit-switched messages from colliding). Once a station has transmitted this message, it occupies over one or two vacant circuit-switched channels, depending on whether the connection is half- or full-duplex.

A station will also place a frame control message on the bus when it wishes to make an external call. The master station decodes this message, "wakes up" the link to the exchange, and synchronizes the IST bus to it. Once the transmitting station has finished the call, it sends another frame control message to the master, which disconnects from the exchange.

If the first bit of the first byte indicates an information message, the following five bits form a destination address and the last two bits are unused. The second byte contains a message service indicator for the controller of the receiving station, of which the first bit specifies whether a signaling or data message follows; the remaining seven bits indicate further message type identifications, for example, call setup messages or response messages. On this byte, the controller can also decide to take the message or route it to another I^{2}C bus member.

The subsequent data bytes carry the actual information in the message being transmitted (signaling information, display information, packet data, and so on). The number of data bytes in a message is limited only by the buffer space in the stations' IST bus interface circuit.

For signaling messages, the data bytes give the information used to establish and cancel circuit-switched connections. A telephone call or circuit-

Control packet	C, FCM	CRC	CRC	EMPT	NACK			
Message packet	I, DEA	s/d, MSI	DATA ----------- Data	CRC	CRC	EMPT	NACK	

C = 'control' bit
FCM = 7-bit frame control message
s/d = signaling or data bit
Data = data being transmitted
EMPT = empty byte
I = information bit
DEA = 5-bit destination address
MSI = 7-bit message service indicator
CRC = cyclic-redundancy-check byte
NACK = not acknowledged byte

exclusive use of the circuit until the connection is released (as for a telephone call), whereas in a packet-switched channel the connection between stations exists only while each individual packet is being transmitted.

The data on the IST bus is time-multiplexed into frames that are synchronized to the standard 8-kHz speech sampling frequency, making for easy and inexpensive connection to public and private digital networks. Each frame is 125 μs long and is divided into 10 channels, one for 8-kHz frame synchronization; one 64-kbit/s half-duplex channel for control, signaling, and packet-switched data; and eight 64-kbit/s half-duplex channels (or four simultaneous duplex) for speech and circuit-switched data. In one frame, each occupied channel begins with a 1 (the start bit), followed by a single word comprising four bits for the frame synchronization channel and eight bits for each of the other channels.

The 32-kbit/s frame synchronization channel (f) carries a four-bit frame word (0011), which is transmitted by one of the stations on the bus every 125 μs to synchronize all stations to the 8-kHz speech sampling frequency. During power-on, a synchronization procedure selects the station that will transmit the frame word. Each station has a unique five-bit address, and each begins to count up from that address; the first to reach 00000 takes over as the master station (that is, begins to transmit the frame word). If this station later fails or is removed from the bus for any reason, another station will take over as master.

If any station needs to make an external call, the bus must be synchronized to the PBX or public network. Stations with links to exchanges have higher addresses (a sixth address bit is hard-wired on the station) and consequently take priority in becoming masters over other stations.

Besides overall synchronization, the synchronization procedure also ensures that there is no corruption of the data when equipment is plugged onto the bus, because a station can only begin to transmit data once it has been synchronized.

switched data transmission on the circuit-switched channels is therefore preceded by one or more signaling messages on the packet-switched channel to establish the connection; after the call or transmission is finished, signaling messages are sent to release the connection.

All packet-switched data and telemetry transfers between stations use data messages. Such messages would establish a packet-switched connection between terminals, serve as a "wake-up call," or signal the start or end of a packet transport. The data bytes in this message would consist, for example, of packets between Telex terminals, between V.24 (RS-232) or X.25 stations (personal computers or word processors), between remote control equipment, or between telemetry equipment.

After each control or information packet, two CRC (cyclic-redundancy-check) bytes are transmitted for error detection. The end of a transmission is indicated by an "empty" byte, which is simply the absence of start and information bits. After this byte, any station that was unable to receive the message can transmit a "not acknowledged" (NACK) byte (11111111). It will do so if an error was detected, if the station's buffer was full, or if there was a collision between two or more transmissions that destroyed the information. This negative acknowledgment allows broadcast calls to be made (one station transmitting to all others, using the destination address 00000).

If a not-acknowledge signal is detected, the IST bus interface circuit retransmits the message, relieving the terminal from the software burden of retransmissions.

The circuit-switched channels

The eight 64-kbit/s channels that carry digitized speech and circuit-switched data to and from the stations are designated b_1–b_8. Stations take control of vacant circuit-switched channels as needed. Two halves of a duplex phone call between two stations may, for example, be carried on channels b_3 and b_8, while those for a call between two other stations may be located on channels b_4 and b_6. Routing for the calls is performed by the relevant station controller using the station's IST bus interface circuit.

The packet-switched channel (bd) has three main uses: to arbitrate between stations wishing to make a connection to the circuit-switched channels, to set up the physical links that will transfer the circuit- and packet-switched data between stations, and to transfer packet-switched data and telemetry information between stations. It uses a protocol similar to the ISO's High-level Data Link control (see "The

Rules for Control and Message Packets," p. 172).

The channel's access method keeps retransmissions and access delays to a minimum for efficient packet transport. It is based on CSMA/CD (carrier-sense multiple access with collision detection), which allows network control to be fully distributed. CSMA/CD uses the principle "listen before and during transmission" to access the bus. All stations monitor the signals on the bus, and any unit can begin transmission as soon as the bus is free (CSMA). If two or more units begin to transmit simultaneously, they detect that fact (CD) and retire from the bus.

During message transmission, signaling and frame control messages have a higher priority than data messages. If, for example, two signaling messages and three data messages were to try to simultaneously access the bus (an improbably high number, even with 30 stations), the signaling messages would be transmitted first, followed by the data messages.

Message errors and collisions are resolved by an access protocol that prevents continued collisions from occurring. This protocol—unlike that of Ethernet and many other CSMA/CD networks—guarantees that a station will gain access within a certain time; if the message suffers three successive retransmissions (because the destination station was unable to receive the message), the bus interface warns the station controller, which takes the appropriate action.

Access delay to the packet-switched channel is low—less than 250 μs—if the channel is idle. If the channel is occupied and no collision occurs, the worst-case access delay is the maximum packet length of the station currently occupying the bus plus 2 ms.

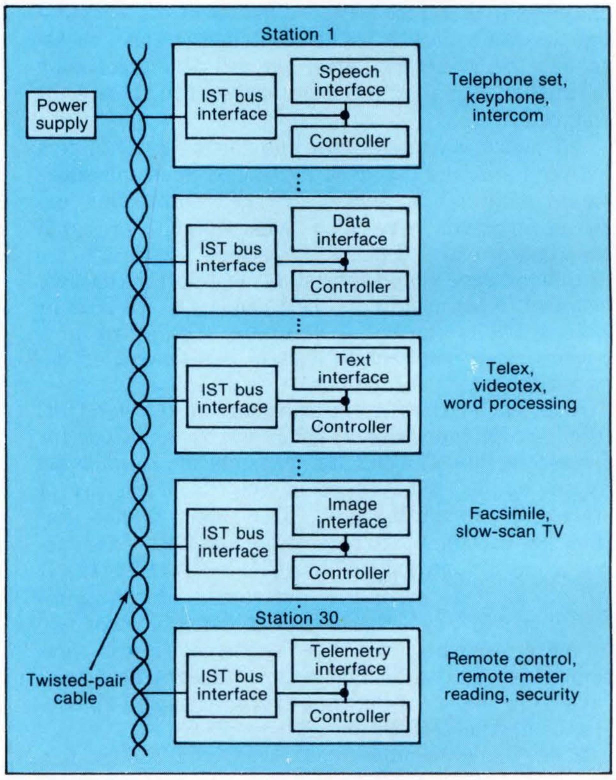
Gateways can connect the bus to analog and digital PBXs, public Telex and data networks, and other local networks. The interface is particularly easy to implement if the larger network is an integrated services digital network (ISDN), because the bus has been designed with such networks in mind. Furthermore, the bus can be connected to a PBX to particular advantage.

The traditional star configuration of a PBX is reliable but rather costly (each station requires an interface and twisted-pair cable to the exchange). In addition, it cannot be extended easily. Large bus systems, on the other hand, are easy to extend and, because of today's VLSI technology, can use low-cost interfaces. A bus network, however, is very sensitive to bus failures, which can moreover be difficult to locate.

An island cabin

Small, local IST buses connected to a PBX give the advantages of both bus and star networks with none of the attendant disadvantages. The IST bus can simply be connected in place of an existing PBX telephone set; the resulting network has the reliability of a PBX and is also inexpensive to implement (much of the existing PBX wiring can be used).

The networks connected by the bus function as speech and data "islands" passing information between telephone sets, data terminals, building energy-control equipment (lighting, heating, and ventilation), and security equipment. This island configuration is very flexible



1. The IST bus serves speech and data transfer, carry up to 30 stations and can easily be interfaced to larger networks. The twisted-pair cable can supply dc power to the stations on the bus.

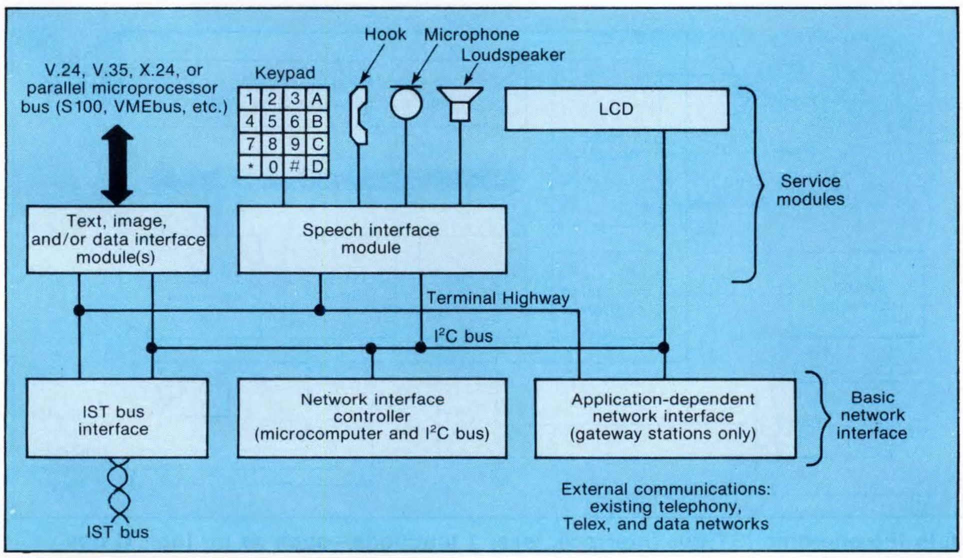
and can be easily extended.

A station connected to one node of the bus can range from a single digital telephone up to a computer with peripherals. In addition, the station can incorporate network interfaces to connect to other computers, local networks, and the exchange. The modular architecture (Fig. 2) will allow a complete range of stations to be built up from a few dedicated ICs, together with general-purpose microcomputers, RAMs, LCD drivers, and so on.

The two major interfaces in this architecture are the inter-IC (I^2C) bus and the Terminal Highway (THW). Together, they guarantee a well-structured station architecture with easy, smooth expansion from simple systems up to intelligent data terminals with integral speech services.

The I^2C bus is a two-wire multiple-master bus for transferring data and control information between integrated circuits (ELECTRONIC DESIGN, March 31, 1981, p. 69A). Its maximum specified transfer speed is 100 kbits/s (for synchronization reasons, the maximum transfer rate for interfacing with the 8-kHz synchronous IST bus is 64 kbits/s). The multimaster feature of this bus makes distributed system control possible and is therefore very powerful for use in ISDN telephone sets and ISDN interfaces for personal computers and data terminals. The bus carries the information transfer to be received or transmitted across the packet-switched channel. This information includes signaling, telemetry, and packet-switched data, as well as control information between the station controller (which has an on-chip I^2C bus interface) and other ICs in the station. In a gateway station, the information is similar.

The Terminal Highway is a standard 2.048-Mbit/s 32-channel PCM highway that is compatible with those used in digital telephone switching equipment. In an IST bus station, it provides connections between the various cir-



2. In this modular setup for telephones and data terminals, the interfaces between the various ICs are standardized by means of the I^2C bus and the Terminal Highway. The lower part services the network interface, the upper part the speech and data services.

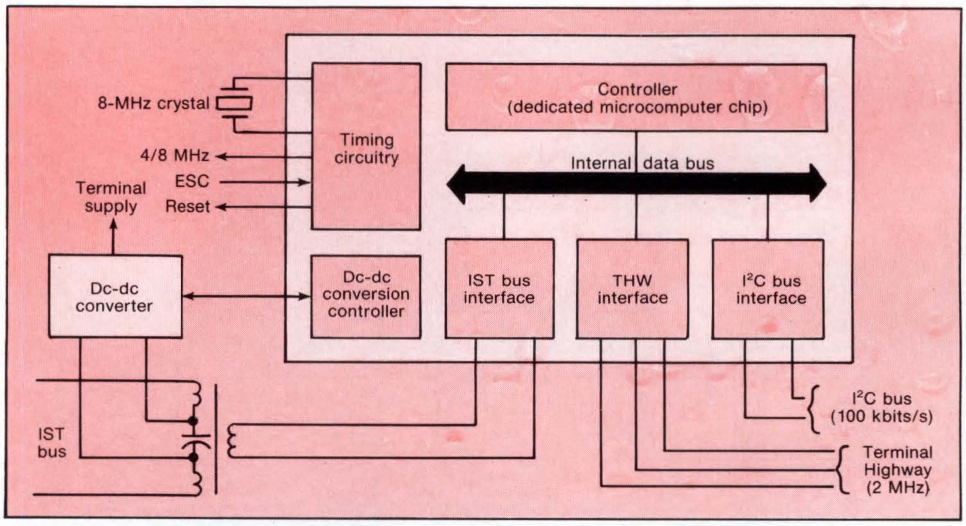
cuits in the station, such as the station controller; the IST bus interface circuit; and the ICs in the speech, text, image, and/or data interface modules and network interface(s). Access to the THW is assigned via the I^2C bus by the station controller, which switches the 64-kbit/s channels of the various circuits to the required THW channels.

The IST bus interface circuit performs all functions needed to establish a link between stations and to transfer information and control messages over the packet-switched channel between two or more stations, including retransmissions. It therefore relieves the station controller from OSI layer 1 and 2 functions. The circuit is controlled, and data entered, via the I^2C bus, which can function as an interface medium to layer 3. This layer is actually located in the software of the station controller, or it can be part of the service modules.

A station will be connected to the bus using this IC and a small coupling transformer (Fig. 3). The transformer provides a convenient means of supplying dc to the stations and also affords a high resistance to induced common-mode signals, important in industrial environments. Some additional components are required when the station is supplied dc via the bus—for example, a polarity guard bridge to prevent incorrect installation and a dc-dc converter to convert the varying dc bus voltage (approximately 20 to 50 V) to a stable 5-V station supply.

To reduce the implementation costs of an IST bus system, the interface circuit will be integrated onto a single chip. (Samples are planned for mid-1985). It will incorporate a dedicated microcontroller, a 256-by-8-bit RAM, and a PLA (programmable logic array). On-chip layer 1 circuitry will interface the IST bus with the THW and the I^2C bus and layer 2 functions will be implemented in the control section's PLA.

To keep system costs low, the interface chip will integrate several additional circuits. These



3. In the one-chip IST bus interface, layer 1 functions—such as for the I^2C bus, THW, and IST bus—are performed by dedicated hardware. Layer 2 functions are programmed into the memory of the special on-chip microcontroller. The chip includes a 256-by-8-bit RAM for message storage and housekeeping.

include a 8.192-MHz crystal-controlled oscillator, a choice of a 4.096- or 8.192-MHz clock output (to provide the clock for other station ICs), a 2.048-MHz Terminal Highway synchronization output, and the control section of the station's dc-dc converter. For synchronization with other digital networks, the IC will also have an 8-kHz external synchronization input.

The timing section of the interface chip will also take care of any cable delays. Once a station gains access to the packet-switched circuit-switched channels and begins transmitting, the receiving station must be synchronized to it. Although each station is synchronized to the 8-kHz frame word at the beginning of each frame, there will be a cable delay between transmitting and receiving stations. The bus interface IC therefore allows for a 4-μs reception window, which accounts for the maximum cable length (5 ns/m $\times$ 2 [400 m]) as soon as it receives the start bit, the chip synchronizes to it to permit reception of the attendant byte.

A 1-Mbyte/s data bus in the IC will connect the layer 1 circuitry to the chip's controller. Packet-switched data and control signals will be routed via this bus to the various sections of the circuit.

Thirty-two RAM locations will be used for internal housekeeping, the remainder providing four bd channel buffers. The size of each of these buffers will be programmable by messages across the I^2C bus interface during system initialization. Two buffers are used to transmit and receive the signaling messages to and from the bd channel, and two to transmit and receive data packets.

The station controller can route information into two additional header buffers, allowing the interface chip to route incoming signaling or data messages to other ICs in the station independently of the station controller.

Putting it all together

The IST bus interface circuit simplifies the designer's job of connecting the terminals of an internal communications system to an integrated services digital network. As stated earlier, it takes care of all layer 1 and 2 protocols, and the designer needs to know only the protocol used on the I^2C bus, which serves as an interface between layers 2 and 3. The network controller, which can be one or more standard microprocessors, will incorporate the software for layer 3 and higher layers.

The microprocessor adds the routing addresses to calls and routes incoming signaling messages and data packets to other terminal circuits such as the terminal's display, the data modules, or in case of a gateway, to the interface circuit of another network.

The terminal controller's software modules include call setup and breakdown routines and initialization routines that cause the terminal circuits to initialize at power-on.

The initialization procedure for the IST bus interface circuit will be performed mostly by the chip itself; it resets all internal registers and RAM locations after power-on. During this process, which takes about 4 ms, the Reset output is kept high. If this output is connected to the Reset input of the terminal controller, the program counter of the controller will be kept at zero.

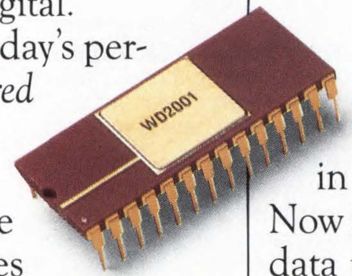
After the reset process is finished, the terminal controller starts the initialization program to load the IST bus address of the terminal; set the sizes of the on-chip signaling, message, data-packet transmission or reception and routing header buffers; and initialize the IST bus. The IC then does the rest automatically. If another terminal begins to transmit the frame word, the chip will lock its synchronization circuitry to the IST bus; otherwise it will itself start to transmit the frame word and then become available to set up connections on the bus.

The use of an interface circuit implementing layers 1 and 2 makes terminal design more of a software than a hardware job. Like the terminal architecture around the I^2C bus and the THW and the architecture of the IST bus interface IC, the software of the network or terminal controller will be modular. When the software modules become available for standardized call setup procedures and routing routines, life will be even easier for the terminal designer. □

How useful?	Circle
Immediate design application	544
Within the next year	545
Not applicable	546

How to build a really

Put the "personal" back in personal computers with the WD2001 Personal Chip™ from Western Digital.



Consider the facts: today's personal computer is a *shared* computer. People in the Modern Office are standing in line to use the nearest PC. John updates his sales forecast, Jane keeps her product plans on target, Martha processes salary reviews, Joe does his monthly report, Teddy wants to write a letter home to Mom – all on the same PC.

How can they keep their files private and prevent electronic eavesdropping? With a Personal Chip, that's how.

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personal computer.

for clever hackers to stumble upon. Without the key, stored data is unintelligible and uncrackable. Type in your key and, instantly, alphabet soup is turned back into data.

For your eyes only. We humans are naturally nosy. We can't resist a peek at our neighbor's mail if we get the chance. With a shared computer you're just tempting human nature.

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Our application engineering team is ready, able and eager to work with you to help you design in the Personal Chip. Because the WD2001 takes just a single socket, it makes sense to design it into your system's motherboard. Or, as the industry's leading designer and manufacturer of disk controller boards, we're in a perfect position to supply you with a custom Winchester/floppy/tape controller with a built in Personal Chip for secure data storage.

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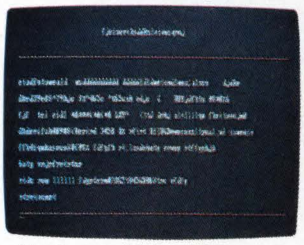
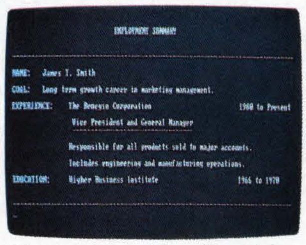
Make us your technology partner



The Personal Chip encrypts data, making it safe to store or transmit.



Decrypt data with a few quick keystrokes—if you have the key.

in data privacy and we'll work with you closely to ensure your success. Write for the WD2001 Data Sheet and Application Note. Or give Dan Fili a call on our Data Privacy Hotline, 714/863-7828. Western Digital Corporation, 2445 McCabe Way, Irvine, California 92714.

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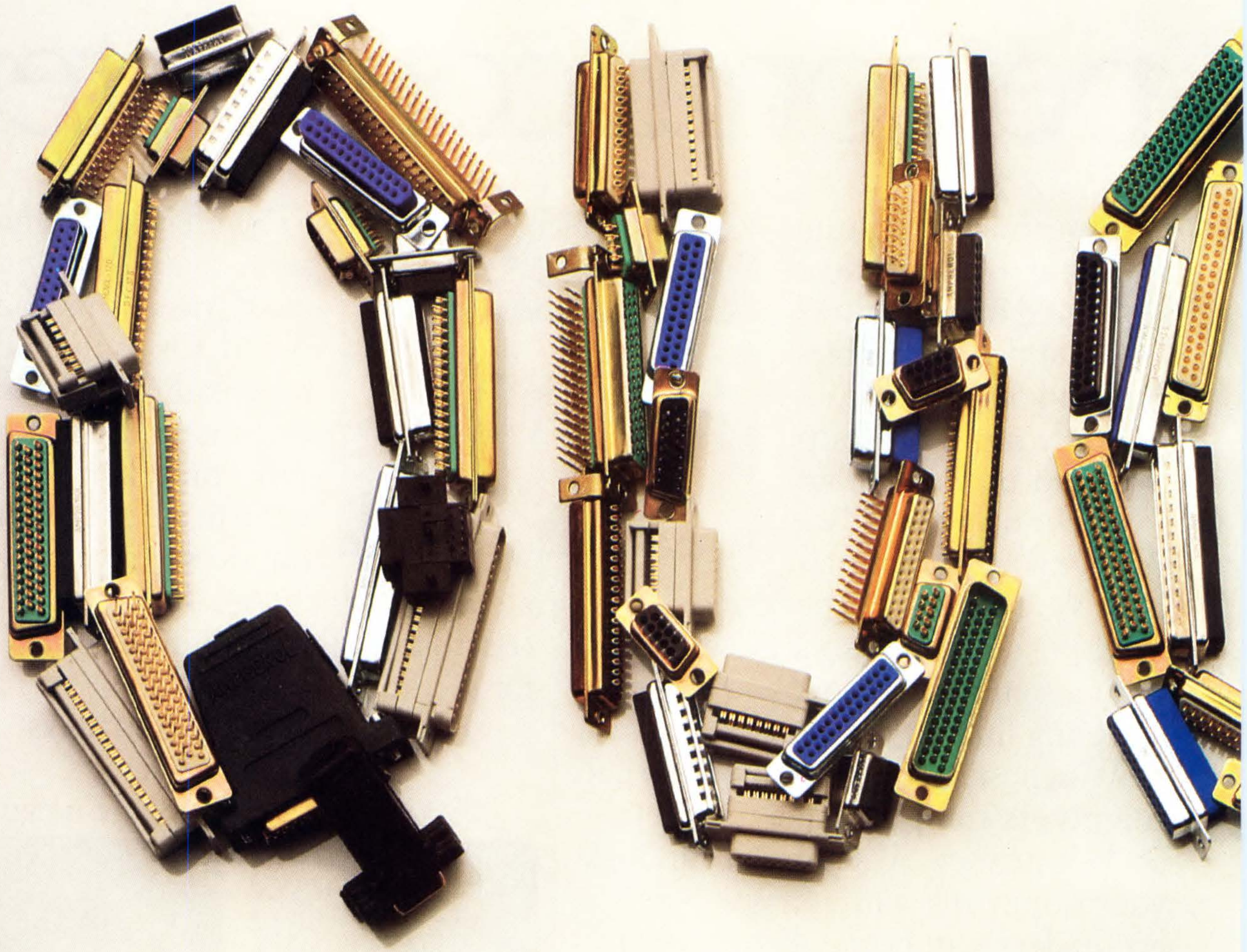

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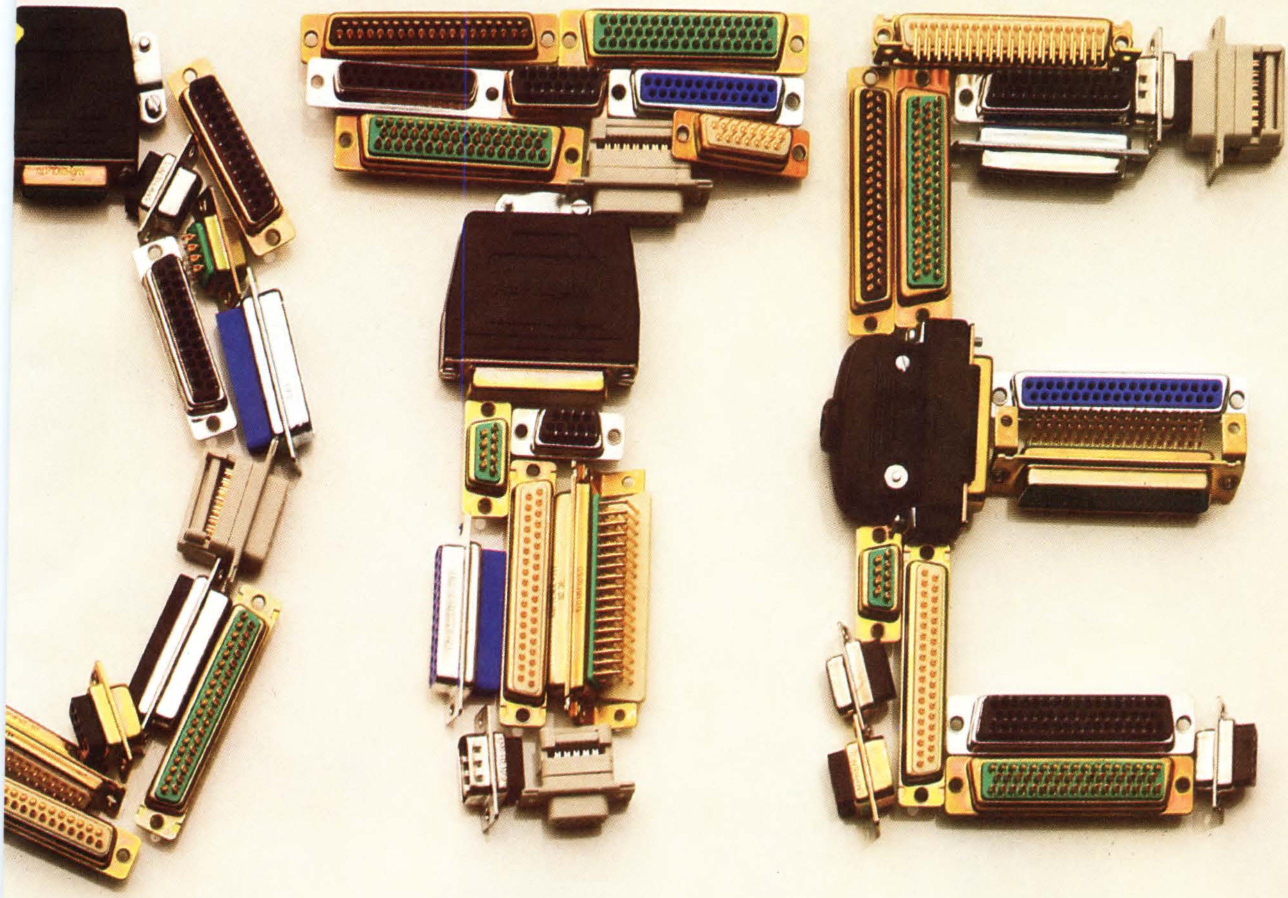

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CIRCLE 84

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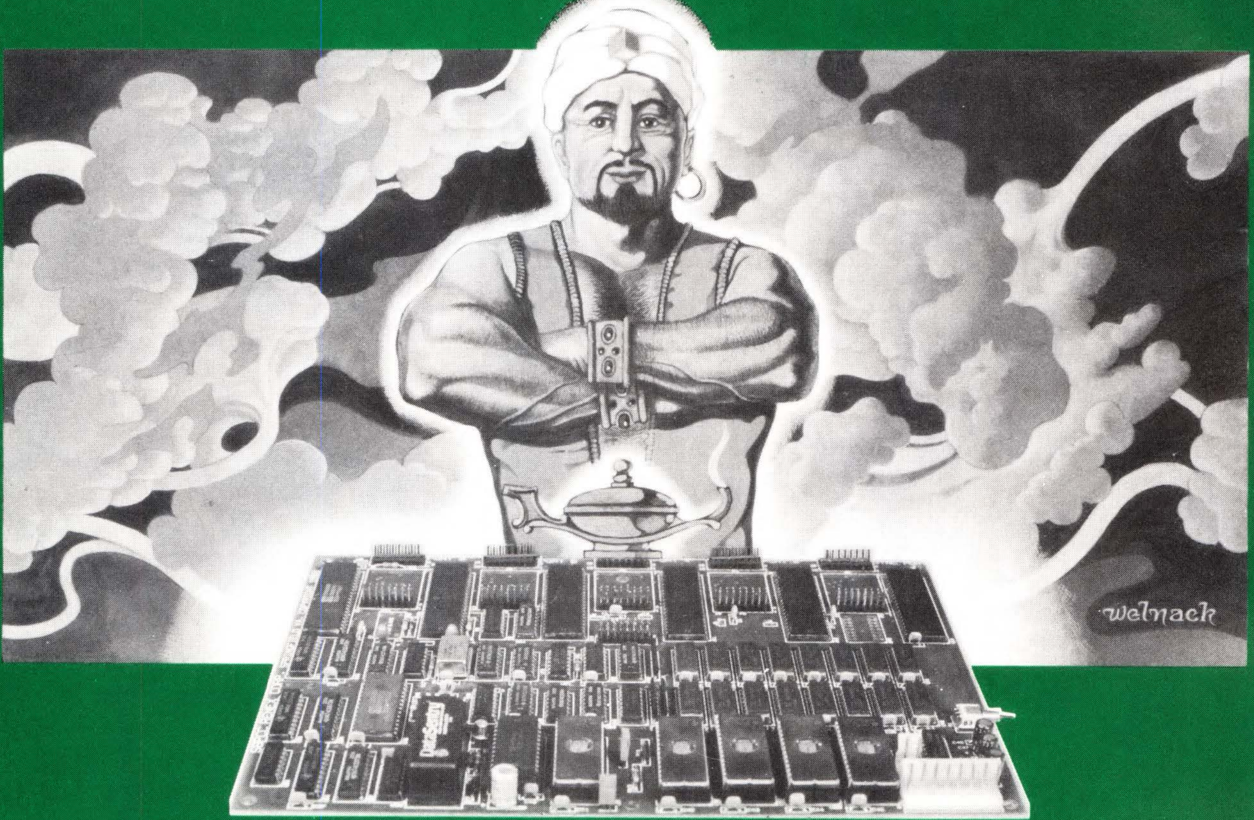

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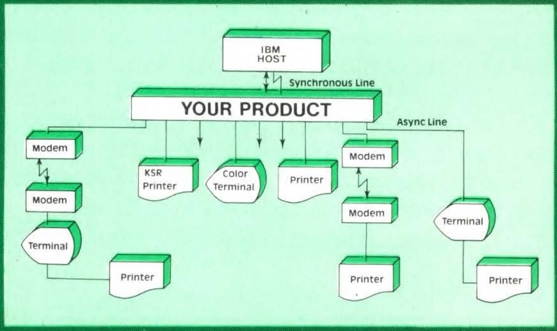

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CIRCLE 85

Low-cost local network for small systems grows from IEEE-802.3 standard

Differing microcomputer systems can communicate easily thanks to Cheapernet, an extension of a new local-area network standard.

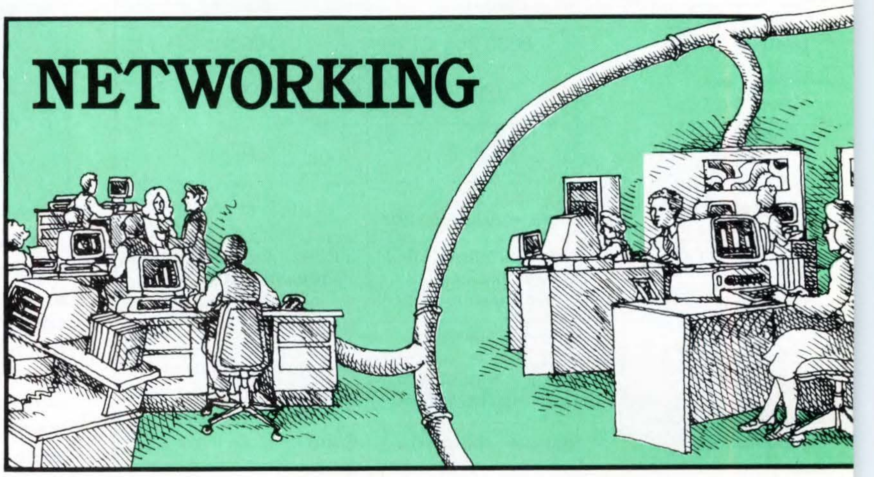
Existing standards for local-area networks define a utility that can serve the communications requirements of an entire building or plant site a lengthy period of time. But the meteoric success of the personal computer and workstation is creating a need for still simpler systems.

Indeed several such networks already exist, giving rise to numerous and confusing permutations of access method, cable type, data rate, and so on. But thus far, no single dominant candidate has emerged to set a de facto standard. Accordingly, the IEEE 802 Local Area Network Standards Committee has undertaken to provide one that conforms to the Open Systems Interconnection reference model formulated and adopted by the International Standards Organization and approved by the IEEE and the European Computer Manufacturers Association. This new open system network has been dubbed Cheapernet.

By accommodating common communications protocols, Cheapernet will enable different manufacturers' equipment to be interconnected. It draws heavily on the technology and protocols for the IEEE-802.3 standard (see the table, p. 186), which is based on the access method known as carrier-sense multiple access with collision detection (CSMA/CD) and is derived from the earlier Ethernet specification.

Essentially a smaller version of the 802.3 network, Cheapernet trades off cable span and the number of stations to obtain lower cost and easier installation. Yet because it is spawned from the earlier standard, it will be

Alan V. Flatman
International Computers Ltd.
Besides serving as manager of local network applications for ICL in Kidsgrove, Staffs., U.K., Alan V. Flatman is chairman of the Cheapernet Task Group of the IEEE's 802 Local Area Network Standards Committee. He has also worked in the areas of displays and fiber optics. A member of IEE, he holds a BS in electronics engineering and a PhD in thermionic storage and speech synthesis from Staffordshire Polytechnic.



Networking: Low-cost local network

able to use the same highly integrated chips that are just becoming available for 802.3-based networks. The result will be additional savings as the cost of the three chips involved—a transceiver, serial encoder-decoder, and network controller—drops further to reflect the economy of large volume production of both types of local networks. (See pp. 193 and 203 for a description of three such chips.)

Data rate is OK

Interestingly, Cheapernet's definers decided not to reduce the data rate from the original standard's 10 Mbits/s, even though such a move would have further reduced the cost. Only marginal savings would have been produced by cutting the data rate to 4 Mbits/s; slowing the rate still further would have congested the channel and required extensive data-packet buffering for certain applications. Worse, lowering the data rate would have rendered Cheapernet incompatible with the original 802.3 standard, which it is intended to complement.

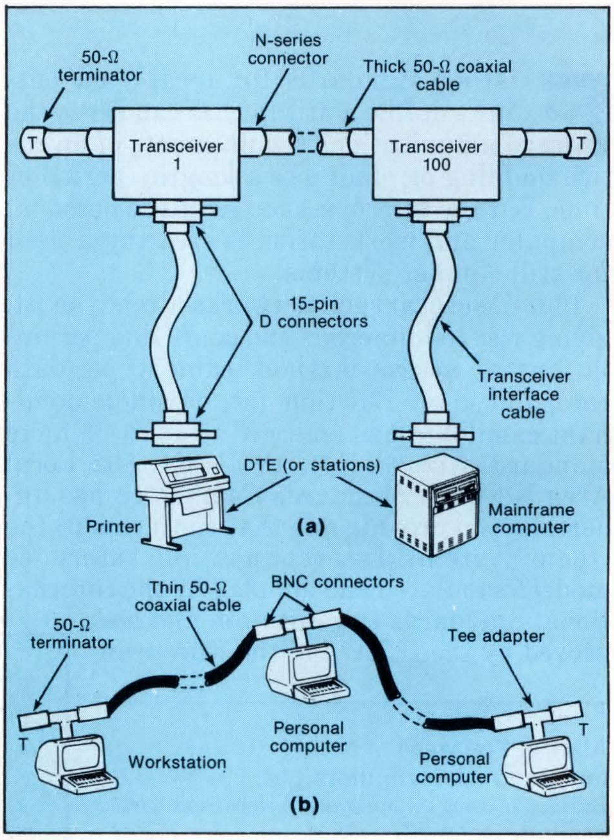
However, one effective cost-cutting method that was adopted was reducing the range, or overall cable span, of the system. A single Cheapernet segment is limited to 600 ft, compared with about 1600 ft permitted by the earlier standard. This allows the use of RG-58, a cable that is thinner and more flexible and therefore costs much less than the one specified in 802.3.

For further economy, Cheapernet terminals connect directly to the network's primary cable. The tradeoff here is that the new net accepts only 30 nodes, whereas the standard 802.3 system accepts up to 100.

That direct connection, a result of placing the network's transceiver inside the user's data terminal equipment (DTE), is physically the most substantial departure from the original 802.3 specification (Fig. 1). The latter calls for external (and therefore more expensive)

IEEE-802.3 and Cheapernet local-area networks compared

Parameter	IEEE-802.3	Cheapernet
Data rate	10 Mbits/s	10 Mbits/s
Segment length	1600 ft	600 ft
Network span	8000 ft	3000 ft
Nodes per segment	100	30
Nodes per network	1024	1024
Node spacing	2.5 m (at cable marker bands)	0.5 m min.
Segment cabling system	0.4-in. diameter, 50-Ω coaxial cable with N-series connectors	0.25-in. diameter, 50-Ω coaxial cable with BNC connectors
Transceiver interface	0.38-in.-diameter multiway cable with 15-pin D connectors (length up to 165 ft)	Not applicable
Installation	Installer required	Simple, mainly by user



1. The acceptance of the Ethernet-like IEEE-802.3 local-area network standard (a) has created interest in a related but less expensive version suitable for small microcomputer systems. To reduce the cost, the newly proposed Cheapernet standard (b) shortens the cable length to make less expensive cables and connectors practical. The data terminal equipment (DTE) incorporates a transceiver IC and so connects directly to the primary cable.

transceivers at the primary cable and connecting cables extending to the DTE.

With Cheapernet, in contrast, each user will likely connect to the primary cable using ready-made cables prefitted with connectors. Alternatively, users can construct their own connector and cable assemblies if they know how, but ready-mades with molded strain reliefs are expected to be more reliable and less expensive. In either case, each user station attaches to a tee adapter in the primary cable. In addition, each tee must be separated from its nearest neighbor by at least 0.5 meter. No other restrictions apply, however, unlike 802.3, where connections are made only at specified cable markers.

Although Cheapernet is intended for very local use, several 600-ft segments can be joined together with the help of signal repeaters. Alternatively, several segments can be similarly attached to a standard 802.3 network, which would thus be made to form the overall network's "backbone" (Fig. 2). The compatibility between the two networks' transmission levels, data rates, and protocols means that the same basic repeater (except for having different coaxial connectors) could be used throughout.

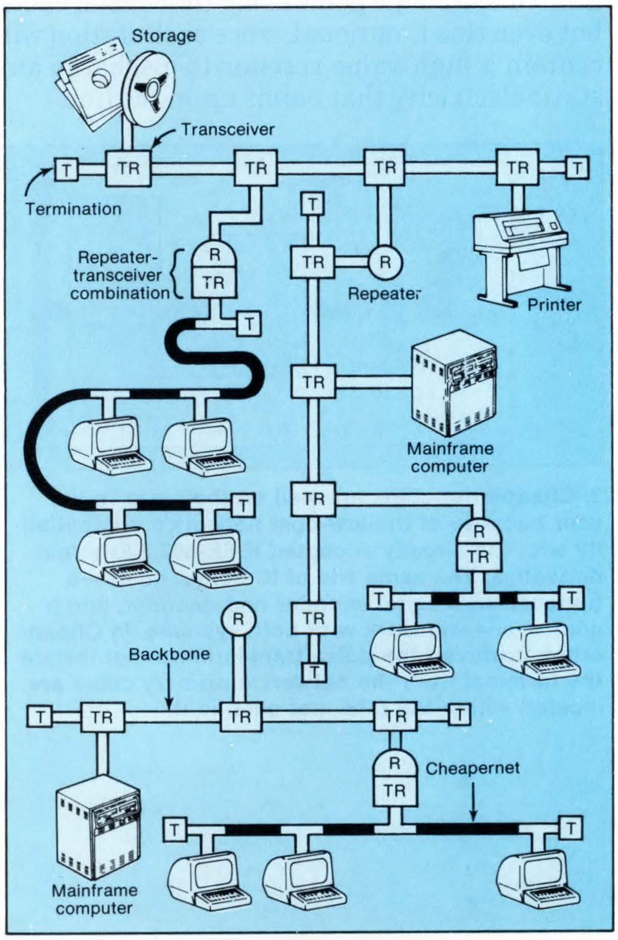
Best of both worlds

Of the two extended configurations, the two-system collaboration is particularly appealing. Such a hybrid unites the attributes of both types of nets: Local users are free to configure their own equipment while enjoying the resilience and reliability of the backbone's data communications infrastructure. Moreover, connections between the systems need no complex and expensive bridges or any additional designing.

The length of such a network is limited by the 25-μs maximum end-to-end delay time that can be tolerated by each network's CSMA/CD protocol. Translated into cable length, this means that the maximum length of a standard local network alone is 8000 ft and that of the Cheapernet is 3000 ft. For a hybrid setup, the maximum length depends on the number of repeaters, the individual lengths of each segment, and other factors. The rules for configuring hybrid systems will be laid out in the Cheapernet specification.

Despite the low cost and simplicity of connecting to a node in the Cheapernet standard, the basic cable components—the RG-58 coaxial cable and BNC connectors—are well proven and reliable. Tests have shown the cable and the BNC connector to meet the need at hand. In fact, both pass the FCC rf emission requirements for Class A and Class B tests. The cable's susceptibility to electromagnetic noise is also acceptably low.

As for the BNC connector, its military rating ensures a low contact resistance even after hundreds of remating cycles. In addition, it resists environmental contamination and the

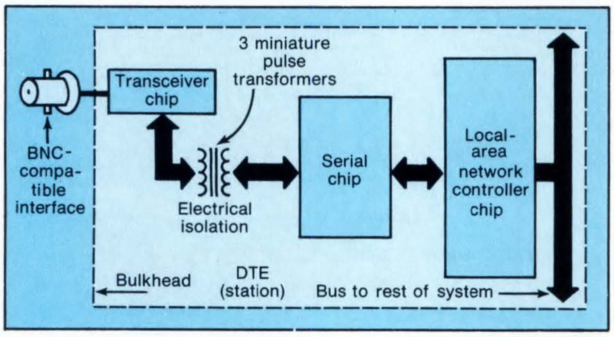


2. To overcome its limited range (600 ft per segment), several Cheapernet lengths can be joined by a repeater or tied into a larger local network "backbone." In the latter configuration, a system can offer the best of both worlds: a low-cost and easy-to-use Cheapernet backed up by a flexible and powerful Ethernet-like network.

Networking: Low-cost local network

degrading effects of long storage periods. Despite these strengths, the wide application of the BNC connector keeps its cost low.

In connecting individual lengths of cable to the system, the designer must take care to cover any exposed metal, be it at a connector, tee adapter, or line terminator, in order to prevent accidental multiple ground connections and their resulting current loops. Such loops would reduce the signal integrity of transmission line. Cheapernet accordingly specifies that plastic moldings be snapped over the exposed metal at each junction, both to prevent ground loops and to help secure the connection they protect. Deliberate grounding should be limited to a single point along the coaxial cable, but even this is optional, since each station will contain a high-value resistor to discharge any static electricity that builds up on the line.



3. Cheapernet chips are well on their way to the user because of the low-cost network's compatibility with the already accepted IEEE-802.3 Ethernet derivative. The same trio of IC components—a transceiver, a serial encoder and decoder, and a controller—will work with both systems. In Cheapernet, however, the pulse transformers that isolate the terminal from the network's primary cable are located within the DTE, not outside it.

Despite Cheapernet's newness, some semiconductor companies are well on their way toward integrating the three active elements of the system. These elements are the transceiver, the serial encoder and decoder, and the controller (Fig. 3). As noted, integrated versions of these parts, which have begun to appear this year, are being developed for the network defined by the 802.3 standard and will automatically apply to Cheapernet as well.

Of the three chips, it is the transceiver that transmits and receives data and senses a collision on the line. As mentioned, this device will be located within the DTE, close to the BNC connector and the primary line itself. Placing the transceiver close to the primary line helps maintain the network's low shunt capacitance (8 pF).

What's more, pulse transformers between the transceiver and serial encoder and decoder chips electrically isolate each DTE from the others in a segment—a separation that is called for in the Cheapernet specification. The DTE is isolated between the transceiver and serial chips and not at the interface to the primary line, because there it would obstruct the sophisticated collision-sensing system, a mechanism that relies on monitoring the line's dc level.

The second chip of the system, the serial encoder and decoder, translates data into the Manchester biphase format for transmission on the system and into the NRZ (non-return-to-zero) coding needed by the controller chip. The Manchester code, having abundant clock pulses, eases the task of decoding data.

Finally, all transmission protocol functions, serial-to-parallel conversion, and communication with the host are the job of the last of the three chips, the controller. This IC could ultimately be combined with the serial encoder and decoder and so cut the system's cost even further.□

How useful?	**Circle**
Immediate design application	547
Within the next year	548
Not applicable	549

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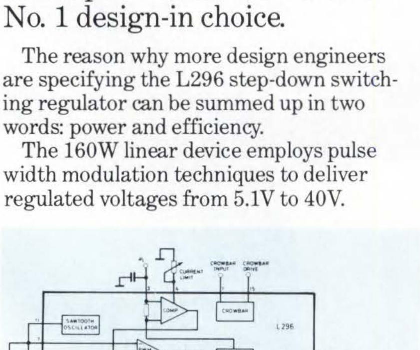

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(Compare this to 30V max. output for competitive types.)

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CIRCLE 86

Now, with 8051 emulation... the gives you more microcomputer

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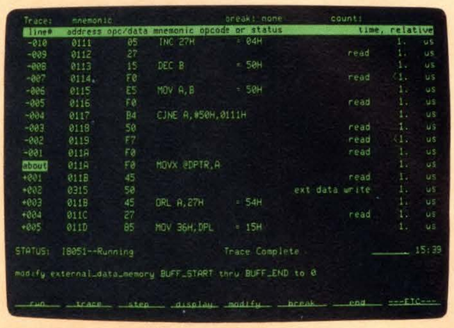

Trace photo of internal data bus is example of how the HP 64264S Emulator shows you more of the 8051 internal operation than ever before.

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	6809E	**80186 (NEW)**
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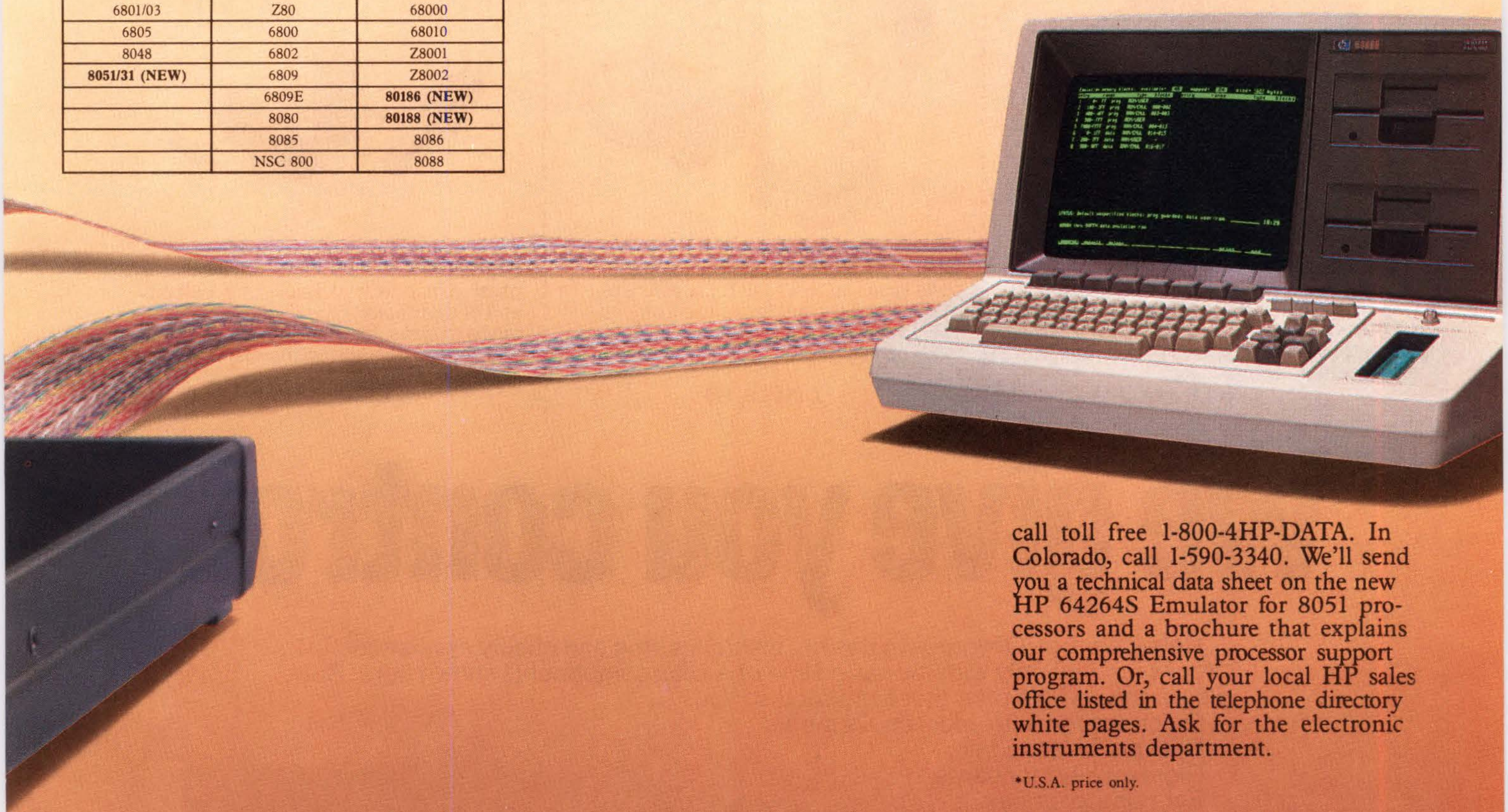

call toll free 1-800-4HP-DATA. In Colorado, call 1-590-3340. We'll send you a technical data sheet on the new HP 64264S Emulator for 8051 processors and a brochure that explains our comprehensive processor support program. Or, call your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

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CIRCLE 87

Transceiver and serial interface ICs put personal computers on budget LAN

Half the job of a network interface—managing a specific protocol and encoding scheme—is shared by two low-cost ICs. A third links them to the host.

Adding a local-area network interface to a computer or computer peripheral should increase its cost of manufacture by no more than 10%, say equipment manufacturers. According to that rule of thumb, the complex board interfaces using discrete ICs that conform to the recently approved IEEE-802.3 standard are much too expensive for personal computers and low-end workstations.

Cheapernet, a low-budget variation about to be added to the Ethernet-derived 802.3 document, is now setting the stage for affordable yet standard local networks. Among other economies, it uses less—and less costly—cable, simpler connectors, and fewer nodes (see p. 185). Moreover, the node circuitry is the same for both Cheapernet and 802.3 networks and, in view of the huge potential demand, well worth integrating into one chip set.

The DP8392 coaxial transceiver interface and the DP8391 serial network interface make up two of the three players needed to form a local area network interface. The third IC, the DP8390 network interface controller, completes the cast and is described separately (p. 203).

The chips' appeal lies not only in their compatibility with 802.3 and Cheapernet specifications, but also in their low cost and ease of use, since a complete interface requires few additional components. For example, with only a 1% resistor, the transceiver chip performs all the functions defined for the 802.3 medium-access unit, except for signal and power isolation. Similarly, the serial interface IC, by substituting a digital for an analog phase-

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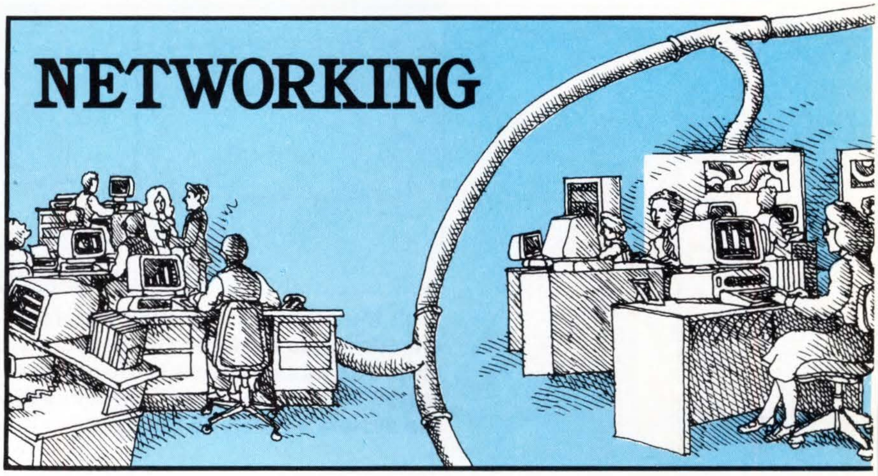
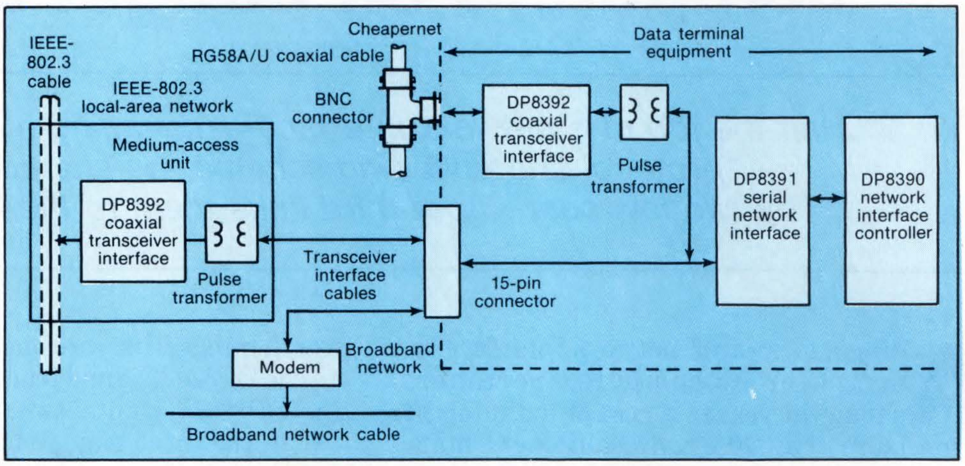


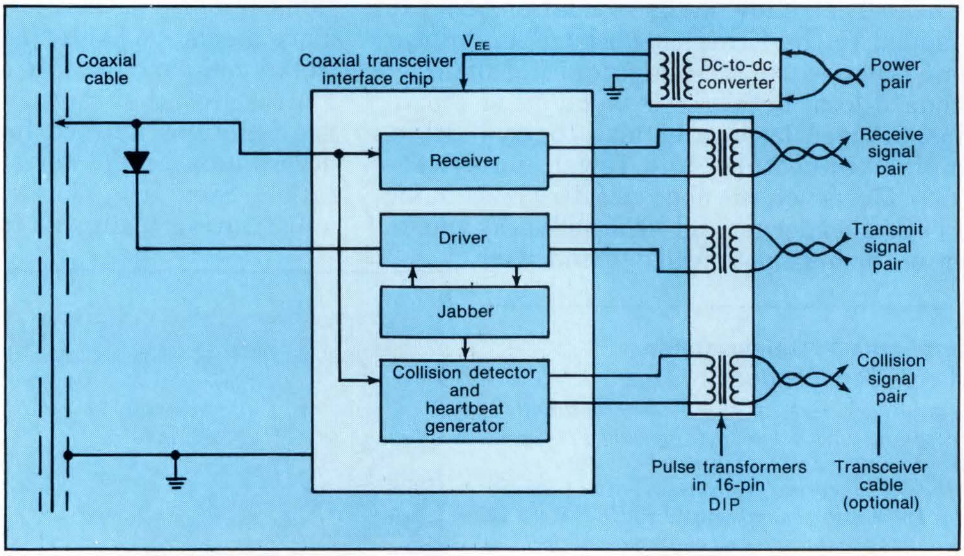
locked loop decoder, sharply cuts the number of precision components needed. In fact, the entire network interface, including 4 kbytes of local buffer memory, requires only 15 in.^{2} of board space and in volume production should cost the original-equipment manufacturer about $100.

Another source of savings is Cheapernet's flexible RG58 coaxial cable, which lets designers put the transceiver IC inside the user's system (referred to generally as the data terminal equipment, or DTE) and dispense with an expensive transceiver cable.

Actually, the chip set offers designers three interface options, provided the necessary connectors are installed (Fig. 1). Equipping the



1. The three-chip local network interface consisting of the DP8392 coaxial transceiver interface, the DP8391 serial network interface, and the DP8390 network interface controller connects to the recently approved IEEE-802.3 (Ethernet) standard, as well as to its proposed low-cost version, Cheapernet. In addition, the interface will tie into a broadband network currently under construction by the IEEE.



2. In the coaxial transceiver interface, the receiver and driver carry Manchester-encoded data between the network's coaxial cable and the serial network interface chip. The jabber circuit turns off an errant driver. The collision detection circuit is tested by the "heartbeat" circuit, which simulates a collision signal and so tests the system's ability to respond.

DTE with a BNC connector permits it to link up with Cheapernet, while adding a 15-pin D connector (and its accompanying cable) enables the DTE to join not only the 802.3's Ethernet-derived system, but also a 10-Mbit/s broadband network currently being defined by the IEEE's 802.3 committee.

Complex but simple to use

Although the chips simplify the job of connection, they are themselves quite complex devices that draw on several process technologies and numerous design innovations (see "Selecting Chip Technologies," opposite). The serial interface chip, for example, uses a patented scheme in its digital phase-locked loop to avoid the need for a 1-GHz clock. Of the three chips in the set, however, the transceiver is the most difficult to integrate onto a single chip because it combines high-precision analog functions with high-speed ECL-based digital circuitry (Fig. 2).

In all, the transceiver contains four main circuits: a driver, a jabber, a receiver, and a collision detector and "heartbeat" generator. As required by the local network specifications, the driver must keep the rise and fall times of its output to 25 ± 5 ns, while matching the two within 1 ns and keeping skew to 2 ns or less. What's more, if the driver's output remains active for more than 20 ms, the jabber circuit disables it. Since 15 ms is the maximum time a driver has to send its message, the jabber in effect detects a faulty transmitter and removes it from the network.

The chip's receiver features an equalizer to reduce signal distortion and a squelch circuit to keep the receiver from responding to noise on the cable. Also, should a collision occur between messages from any two stations, the chip's collision detection circuit turns on a 10-MHz warning signal.

This circuit, which contains a four-pole Bessel filter and a trimmed on-board voltage reference, also issues a "heartbeat" signal at the end of every packet that the chip transmits. The heartbeat is a burst of the 10-MHz collision detection signal sent to the DTE, and tests the transceiver's ability to respond to a collision.

Additional components are needed to provide dc isolation between the transceiver's power and signal connections and the DTE. In new designs, the best way to isolate the power connections is to energize the chip from a separate winding in the DTE's power-supply transformer. However, this may not be prac-

Selecting chip technologies

The decision to partition the network interface into three chips using different technologies was based mainly on the differing precision, speed, and density requirement of their functions. However, in the case of DP8392 coaxial transceiver interface chip, the circuitry between the primary cable and the isolation transformers was a logical candidate for integration, since it would keep all electronics on the cable side of the transformers within a single chip.

To integrate the transceiver called for a process that resisted any failures that could disable the entire network, and at the same time one that could perform high-precision analog and high-speed digital functions. For these criteria, designers tailored a junction-isolated bipolar process specially for the device. Its deep epitaxial layer withstands voltage spikes on the coaxial line and its thick oxide layers enhance the bipolar technology's inherent static immunity.

Also, because the standard 802.3 network requires a reliability of 1 million hours MTBF, designers took extra steps to ensure the transceiver's longevity. The most critical was a lead-frame package design, which increases the chip's thermal conductivity, boosting reliability by reducing the chip's operating temperature. In addition they kept the current density low through the metal lines of any critical paths and adhered to a conservative set of spacing rules throughout.

For the DP8391 serial network interface, the high speed needed for its digital phase-locked loop decoder was the overriding consideration. As a result, an oxide-isolated bipolar process was chosen. Circuitry is configured in high-speed differential ECL, except for the interface buffers to the controller chip, which are TTL devices. What's more, in combining ECL and TTL circuits, designers were careful to keep separate V_{CC} and ground lines for each to minimize noise.

The last chip of the three, the DP8390 network interface controller (see p. 203), emphasizes logic and memory devices and is processed with Micro-CMOS technology. This process delivers the requisite high speed (10 Mbits/s) and density and forestalls the potential problems of limited supply current and poor cooling in small systems. It is characterized by oxide isolation, two layers of metal, and self-aligned 2-μm gates.

tical for an existing design. In that case, one practical approach when (as in Cheapernet) the transceiver chip is located inside the DTE is to use a dc-to-dc converter. Since the chip requires −9 V dc, this power can be drawn from the DTE's 5-V dc logic supply through a low-cost circuit consisting of a transformer, a simple two-transistor self-oscillating primary circuit, and a regulated secondary circuit.

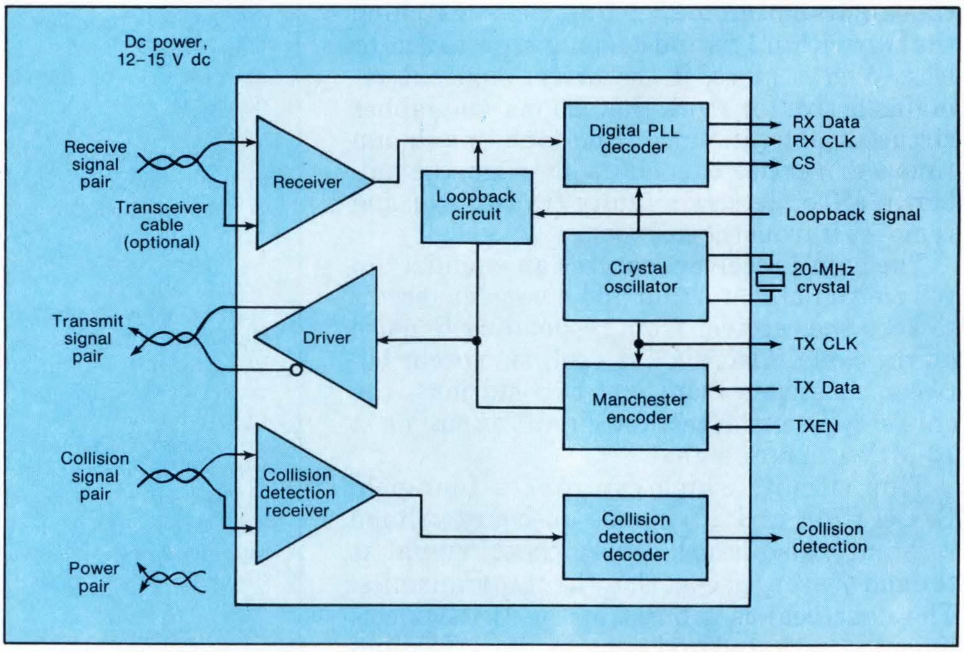
Even for an Ethernet-like application, where the entire transceiver unit is external to the DTE and the 12-to-15-V range reduces the regulator's efficiency, the transceiver chip's low current drain still allows an unusually low cost regulator to be employed.

As for the signal lines, pulse transformers isolate the receiver, collision detection, and transmitter pairs. What's more, to eliminate large idle currents through the pulse transformers, the differential outputs of the chip's receiver and collision signals become zero when no signal is present. Furthermore, the input to the transmitter section contains a squelch circuit to suppress any noise that could result from keeping both its differential lines at the same potential.

The pulse transformers that provide dc isolation of the transceiver chip's receiver, transmitter, and collision detector signals also couple these signals to the second chip in the set, the serial network interface (Fig. 3). Even if this coupling is routed through a separate cable to the DTE, the connection does not require additional isolation at the DTE end. That is because the serial network chip's differential drivers and receivers succeed in meeting all of the connection's short-circuit, breakdown, and common-mode requirements. In addition, like their transceiver chip counterparts, they feature squelch circuits on the receivers' inputs and zero-current idle states on the drivers' outputs.

When transmitting data, the serial network chip converts non-return-to-zero (NRZ) data and clock pulses from the controller chip into Manchester encoding and sends the converted data to the transceiver. The opposite process occurs for reception, but then the serial network chip must decode a 10-MHz signal that has accumulated as much as ±20 ns of jitter.

To do this, the chip uses a novel digital PLL to avoid the pitfalls of an analog one. An analog



3. During transmission, the serial network interface chip changes NRZ data from the network interface controller into Manchester-encoded data for the coaxial transceiver. During reception, a digital phase-locked loop helps decode 10-Mbit/s data containing as much as ±23% jitter.

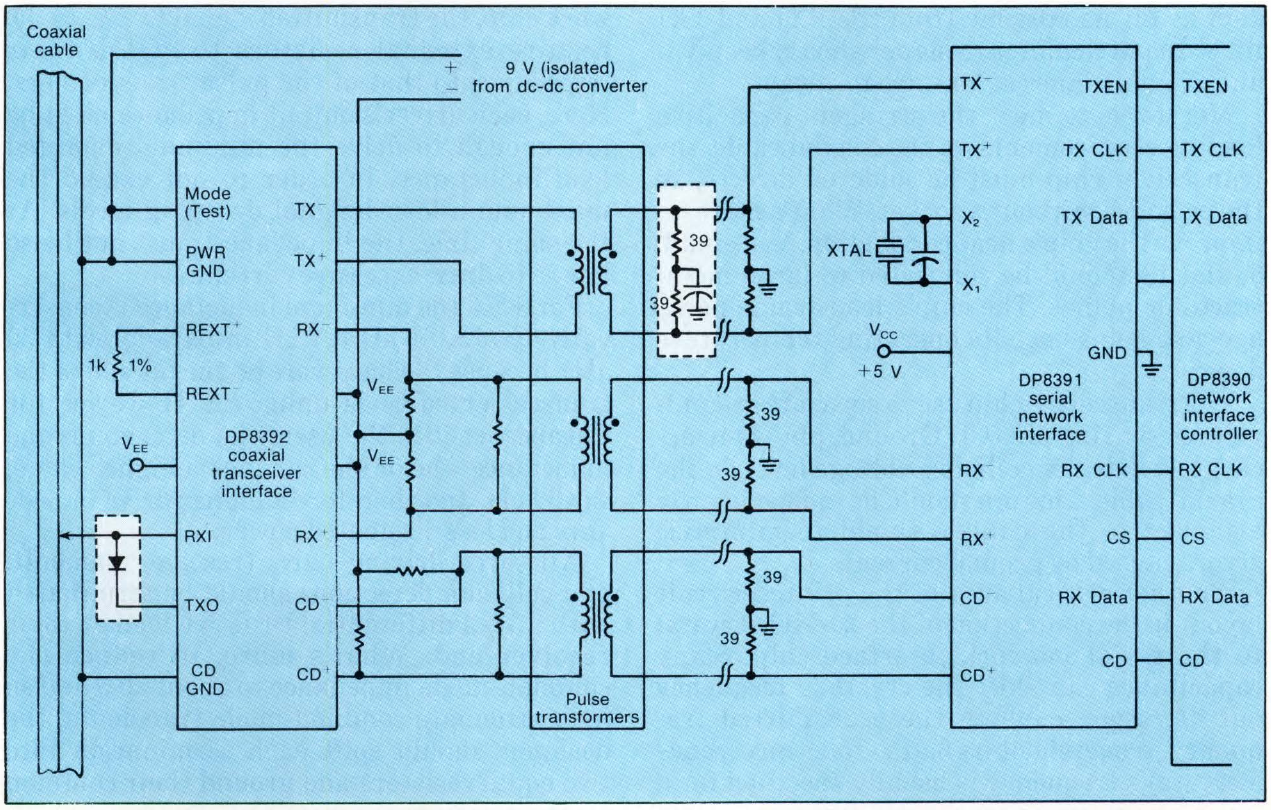
PLL would require several precision components and its performance could degrade because of poor layout or induced noise. In contrast, the digital PLL requires no external components and performs more predictably. A conventional digital PLL, however, would have to sample the input signal every 2 ns and would therefore require a precise and extremely expensive 1-GHz clock.

Beat the clock

Instead, the chip uses a patented technique to extract the needed 2-ns resolution from a less critical 160-MHz, three-phase clock. This clock is generated on chip from only one external part: a 20-MHz crystal. Thus the chip saves board space while providing a high-performance digital PLL—one that locks on instantly to the first valid edge of a signal and achieves full resolution in no more than 5 bits.

In addition to its encoding and decoding function, the serial network chip also develops a carrier-sensing signal from its receive-signal lines and decodes the collision-sensing signal into TTL and MOS levels for the controller. Finally, for diagnostics purposes, the chip includes an internal signal-loopback path.

The pin assignments of both the transceiver and serial interface are designed to minimize the crossover of any printed-circuit traces. Moreover, some of the components needed for an Ethernet-like interface are eliminated for Cheapernet (Fig. 4). For instance, Cheapernet's relaxed load capacitance (8 pF, compared with 4 pF for the modified Ethernet) obviates the need for an external capacitance isolation



4. A complete interface occupies less than 15 in.^{2} and costs only about $100 (the dashed lines indicate the parts not needed for Cheapernet). Pulse transformers provide the necessary dc isolation for signals between the transceiver chip and the rest of the interface. Dc power must also be isolated using either a dc-to-dc onverter or a separate power supply winding from the user's system.

Networking: 802.3 interface chips

diode. Also, because Cheapernet has the transceiver inside the user's system, it requires neither a separate cable nor Ethernet's line-terminating resistors found on the transmitted-signal lines (TX^+ and TX^-) at the pulse transformer.

Prepare with care

Despite the network's lack of precision components, the designer must lay out certain sections of the circuit board with special care. The most critical of these is the coaxial cable connections to the transceiver's Receiver Input (RXI) and Transmitter Output (TXO) pins. These must be kept as short as possible. Also, when attaching an external diode to the transceiver chip, the designer must minimize any stray capacitance, particularly on the diode's anode side. To do this, all metal lines must be kept as far as possible from the RXI and TXI lines. In particular, a designer should keep V_{CC} and ground planes at least 0.5 in. away.

Moreover, to meet the stringent capacitive loading requirements on the coaxial cable, the transceiver chip must be soldered directly to the pc board without a socket. What's more, to improve the chip's heat conduction, V_{EE} pins 4, 5, and 13 should be connected to large metal traces or planes. The chip's lead-frame package also helps keep its operating temperature down.

The transceiver chip uses a separate ground-voltage sensing pin (CD Ground, pin 16) to accurately detect a collision-voltage level on the coaxial cable. This pin should be independently attached to the cable's shield to minimize errors caused by ground currents.

Another critical area of the printed-circuit layout is the connection of the 20-MHz crystal to the serial network interface chip. Stray capacitance can shift the crystal's frequency out of range, causing the transmitted frequency to overshoot its 0.01% tolerance. Since a crystal's frequency is usually specified for a given shunt capacitance, the designer should make every attempt to match that capacitance.

In making that match, the factors to consider are stray capacitance at the chip's pins (about 5 pF), at its socket if one is used, and at the circuit board's traces (to be kept as short as possible) and plated through holes. Once the total stray capacitance is determined, the designer can calculate any shunt capacitance that may be needed to match that specified for the crystal. Furthermore, as a check, the designer can measure the transmission frequency at the serial interface chip's Transmit Clock pin (TX CLK) and adjust the shunt capacitance accordingly. Tests show that a 25% change in the shunt capacitance causes a 0.01% shift in a crystal's frequency. Once the designer finds the correct capacitance for a given layout, a fixed-value 5% tolerance capacitor is all that is needed. A typical value for that shunt capacitor is 20 pF.

Line termination is another important consideration for the network interface. The line-driver output pairs of the transceiver chip, the Received (RX^+, RX^-) and collision detection (CD^+, CD^-) signals, and that of the serial network chip, the transmitted signal (TX^+, TX^-), require external resistors to match their impedance to that of the pulse transformers. Here, each driver's output impedance must be low enough to drive the minimum expected load inductance, in order to not exceed the maximum allowed signal drooping levels. At the same time, the impedance must not be so low as to draw excessive current.

For 802.3 the minimum inductance is conservatively low, 81 μH (27 μH in parallel with 50 μH), because the hardware on the far end of the transceiver cable is unknown. However, for Cheapernet it is the user who determines the inductance—he or she can pick a higher value, say 50 μH, and therefore a higher drive impedance and less dissipated power.

All three driving pairs (receive, transmit, and collision detection) should be terminated with a 78-Ω differential resistive load at their receiver end. What's more, to reduce the common-mode impedance to about 20 Ω and so help attenuate common-mode transients, the designer should split each termination into two equal resistors and ground their common (center) node.□

How useful?	Circle
Immediate design application	550
Within the next year	551
Not applicable	552

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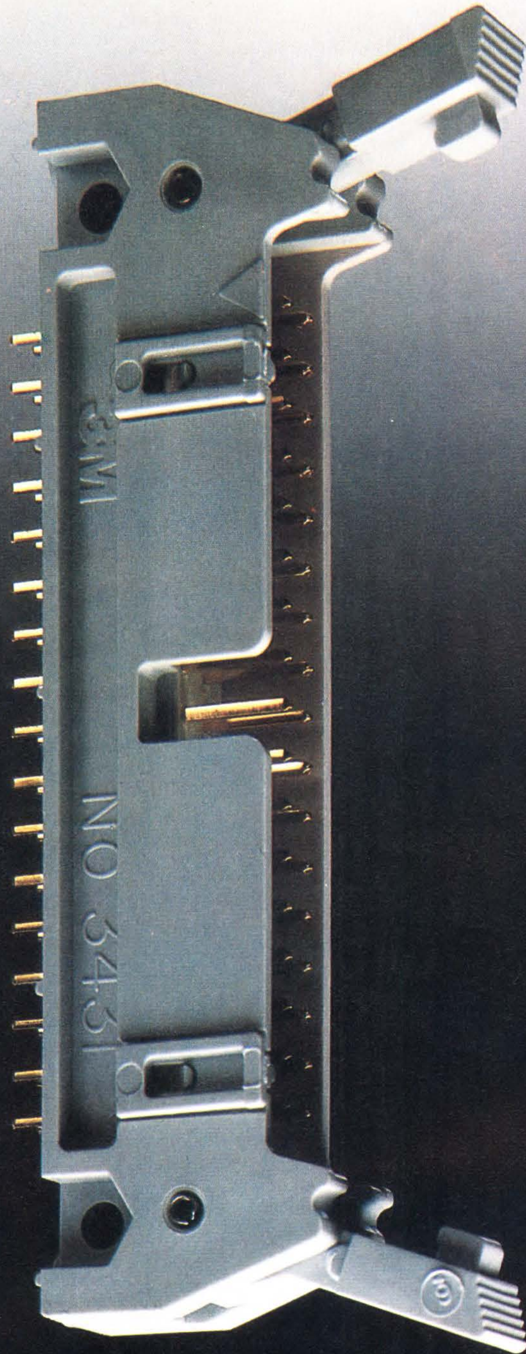

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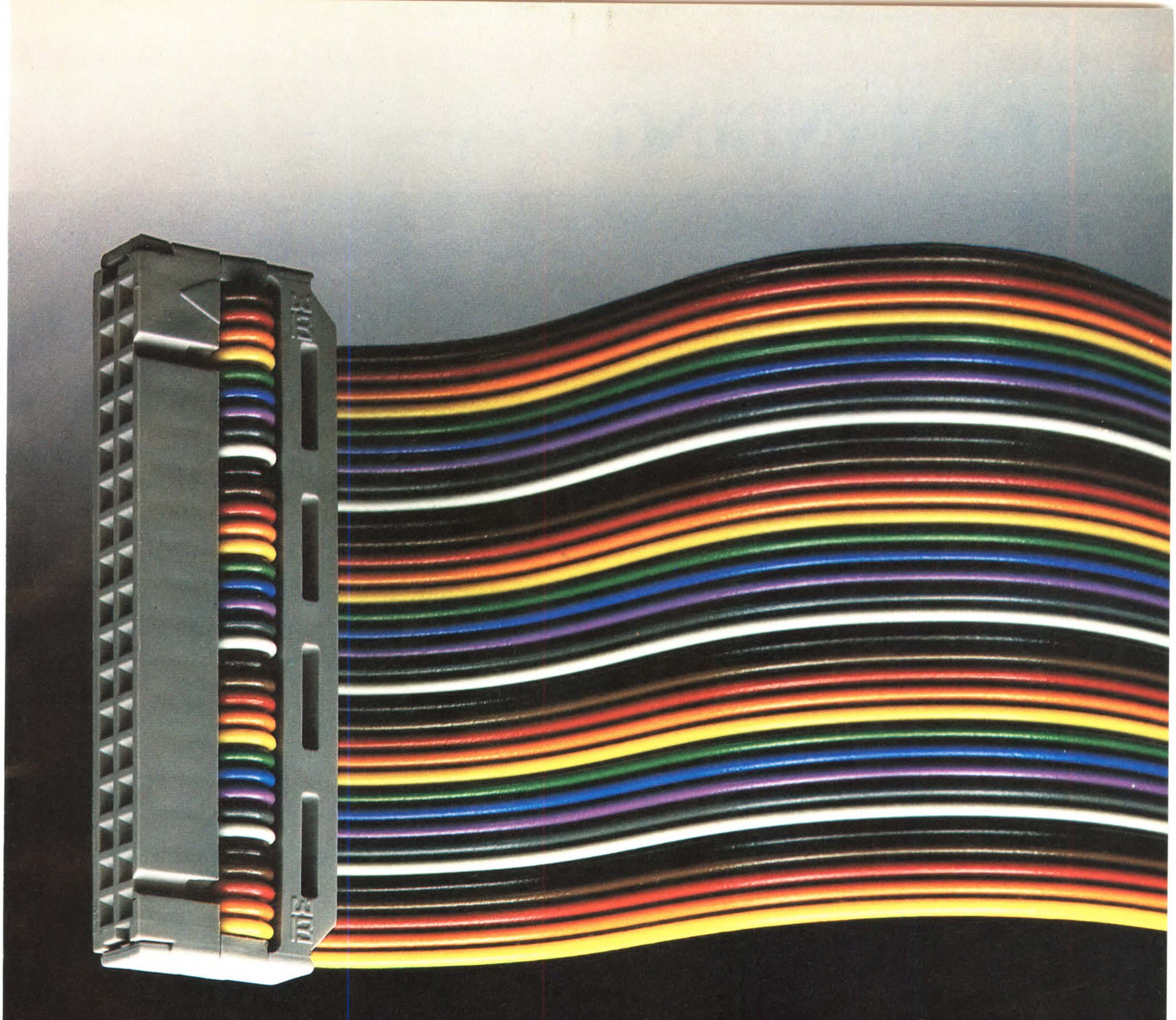

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CIRCLE 90

Network controller chip prevents host interface tie-ups with 2 DMA channels

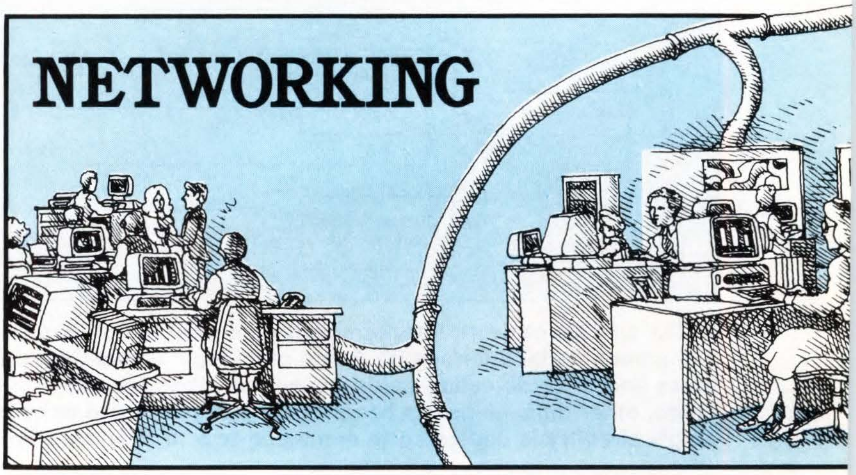
An IEEE-802.3 controller chip easily handles messages that might otherwise swamp a small system's CPU. With two other chips it makes a compact network interface.

As designers of small systems eye the coming low-cost chips for local-area networks, they will have to consider the burden that the network interface places on their system's CPU and bus structure. What they will find is that such an interface must constantly monitor the needs of the central processor and the network. The reason is that an incoming message can appear any moment, and instant access to the network is never certain for outgoing messages. In short, the network's complex and unpredictable nature can hamstring a small system's CPU and clog its address and data buses.

To counteract this potential logjam, a recently announced IC for the IEEE-802.3 standard, the DP8390 network interface controller, features two high-speed 16-bit, direct-memory-access channels. Instead of relying on the system's host processor, both channels share powerful logic sections that can manage a buffer memory and arbitrate access to the system bus. What's more, when it is used with two new transceiver and serial interface chips (see p. 193), the overall network interface can be very inexpensive.

The chip has other strengths, as well: It is compatible with both low-cost 8-bit microprocessors and high-performance 16-bit ones; it incorporates a scheme for addressing several stations at the same time; it records the network's performance and monitors errors; and it tests itself and the network by looping back transmitted messages through several stages of the interface.

The network interface controller relieves the system's CPU and bus structure of the



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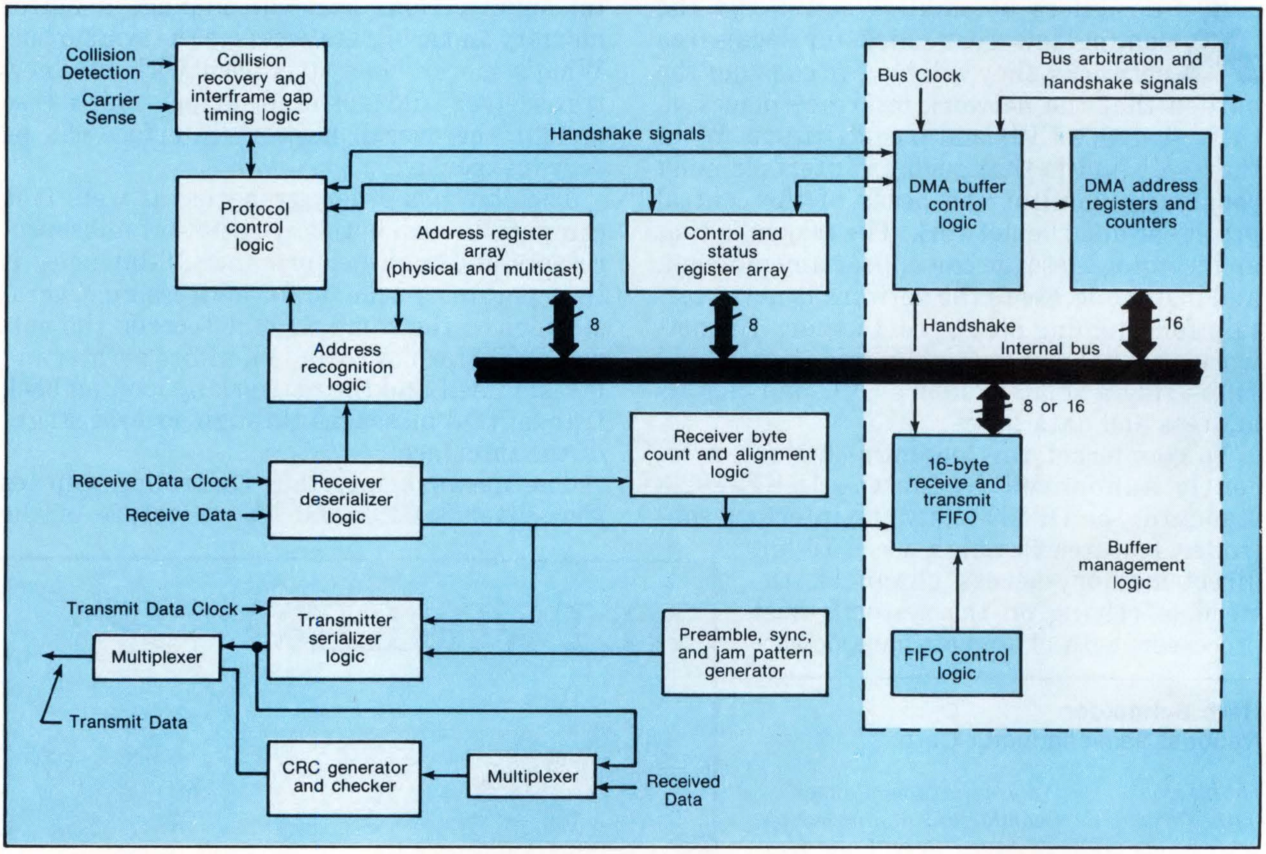
nitty-gritty of accepting messages from, and preparing them for, the network's cable. Among the details it takes over are allocating buffer and main memory, handling partly received messages, retransmitting messages after a collision, and writing status and message-linking information to memory. Obviously, the more work a controller handles for a system's central processor, the less of a burden is the network interface.

Two-channel champion

The advantage of a powerful two-channel DMA function is that designers usually employ a dual-port buffer memory to isolate the system's CPU from the real-time demands of receiving and transmitting messages. But many dual-port designs still require bus arbitration logic, as well as buffers, latches, and other glue logic. The network interface controller, however, uses few extra devices, because its on-board DMA circuitry is tailored to access the buffer memory and transfer data between it and the main memory.

As a result, the controller is especially suited to low-cost systems that may lack the space or budget for many extra components. It is also easy on the system power supply. Because the chip is fabricated using a high-density CMOS process, it consumes relatively little power despite its high speed (see "Selecting Chip Technologies," p. 195).

The controller's two major operating modes are for receiving and transmitting data, and so most of the chip's logic focuses on these two tasks (Fig. 1). In the receiving mode, the chip first aligns into bytes any received serial message of the proper format. Among the fields of



1. The DP8390 network interface controller chip transfers message packets between a host system bus and a companion serial interface IC. Some of its logic elements deserialize received messages and check their address and error detection fields, as well as other aspects of the IEEE-802.3 protocol. In the chip's transmitting mode, other logic elements serialize outgoing data and append the proper bit fields. In addition some of the chip's circuitry is dedicated to managing two 10-Mbyte/s DMA channels (tinted area).

a properly formatted message are a 62-bit preamble, a 26-bit synchronization field, 6-byte destination and 6-byte addresses, a 2-byte field giving the message's length, a data field of 46 to 1500 bytes long, and a 4-byte CRC, or cyclic redundancy code.

Once the incoming message bytes are aligned, the controller's address recognition logic simultaneously stores the 6-byte destination field in an on-board 16-byte FIFO (first-in, first-out) register and compares the field with the node's own programmed address value (see "Software Initialization: The Basics," below). If the comparison is a

Software initialization: The basics

The DP8390 network interface controller powers up as a peripheral device in a reset state. Therefore a CPU can invoke the controller only after sending it a command to leave that state (see the figure). The controller's resetting action upon powering up is a safety measure that prevents it from sending or receiving messages arbitrarily when uninitialized.

Once the controller is commanded to leave the reset state, it cannot carry messages until software has initialized several sets of its registers. These registers set the network and system operating conditions, like physical and multiple ("multicast") addresses, transmitter and receiver configuration, data width, and details of the buffer memory's management.

For starters, the host system must load the physical address register with the 48-bit address unique to that particular node on the local network. In addition, if multicast addressing is used, a program must calculate a 6-bit pattern that reflects the user-assigned multicast address and load that pattern into the multicast address register. To calculate the 6-bit pattern, the user submits the multicast address to a software routine that performs a binary division calculation, similar to that for producing the well-known error-checking cyclic redundancy character. The desired pattern for the multicast address consists of the most significant 6 bits of the division operation's 32-bit remainder.

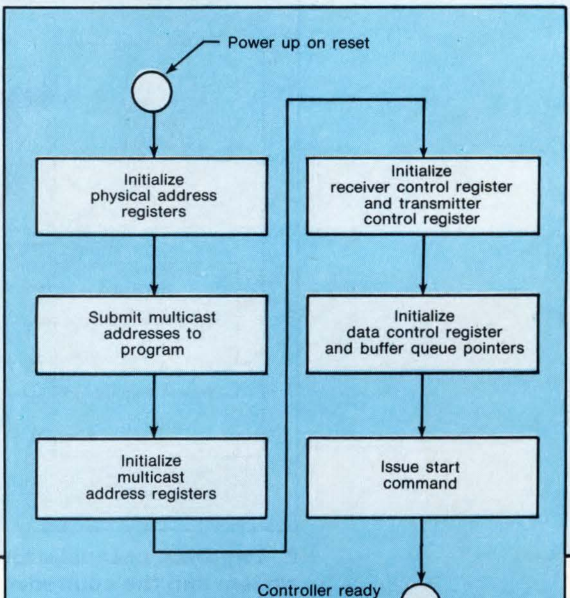
Also requiring initialization is the receive configuration register. It determines if the controller will save message packets that contain errors or accept the remaining fragment of a packet dubbed a "runt" packet that is left after a collision. The same register determines what combination of broadcast, multicast, and physical addresses the controller will be able to accept. It also has the ability to set the controller receiver section to simply monitor network activity.

Another register, the transmit configuration, requires initialization, since it establishes the actions of the controller's transmitter section pertaining largely to diagnosis and testing. With it, the designer can withhold the cycle redundancy check character and establish several loopback test modes.

To adapt the controller to its host system, the data configuration register programs the chip's direct-memory-access operations for byte- or word-wide transfers. It can also configure the chip's dual 16-bit DMA channels as a single 32-bit DMA channel. Also programmed by the data configuration register is the threshold at which the chip's 16-byte FIFO register initiates a DMA operation.

Before the controller can receive message packets, the system's CPU must establish a receive buffer queue by programming the page start and page stop registers. The receive buffer queue can reside anywhere within a 64k address space.

Finally, once the host processor initializes the controller's registers, it sends a start command to the controller that enables it to transmit or receive messages.



match, the FIFO register continues to store the message packet. Before the register overflows, however, the controller's DMA starts transferring the bytes to a buffer memory. Meanwhile the controller's protocol control logic monitors all receptions and determines whether to reject any packets containing frame alignment or CRC errors or packets with fewer than 64 bytes (called "runt" packets).

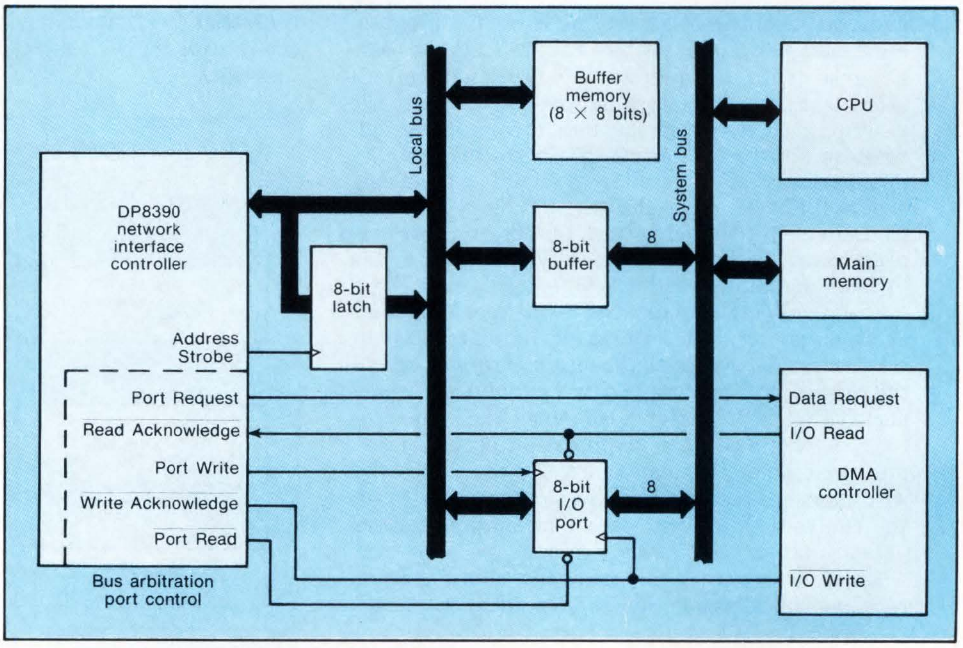
Before transmission the protocol control logic senses the network for a carrier, which signifies that another node is active. During transmission it also checks for collisions on the network. If one occurs, the logic initiates a jam sequence, backs off, and reschedules the message for another time. In a jam sequence, the transmitter continues to send data after sensing a collision on the line, to ensure that all other stations detect the collision. Message rescheduling is based on a back-off period, which delays transmission for a random amount of time, as specified in the IEEE-802.3 standard.

At the start of transmission the controller sends a preamble, a sync field, destination and source addresses, and data. DMA operations transfer the data for transmission from the buffer memory to the chip's FIFO register. At the same time, the controller generates and appends the CRC fields that complete the format.

Speed vs the unpredictable

Basically the chip's design attacks the interface designer's biggest problem: connecting the host system's bus to the local network's fast, but unpredictable, 10-Mbit/s serial data streams. Thus, where other controllers use a single DMA channel that transfers data at about 2 Mbytes/s, the new controller has two 10-Mbyte/s DMA channels, one local and the other remote. Together the channels, in effect, turn a single-port buffer memory into a dual-port one for temporarily storing message packets (Fig. 2).

The local DMA channel transfers any message packets, either just received or ready for transmission, between the buffer memory and the controller's FIFO register. Furthermore, to simplify the designer's job and reduce the need for intervention by the system processor,



2. Two DMA channels, remote and local, speed the flow of data between a host system and the controller chip. In a typical transmission, data from the host travels via the remote DMA channel through an I/O port and into a buffer memory. The local channel then carries the data to a FIFO register inside the controller. The reverse occurs with received data.

the chip's buffer control logic conducts the transfer directed by a built-in algorithm.

In fact, when the controller is receiving message packets, the buffer control logic serves three basic needs: It chains separate pages of buffer memory together when a packet exceeds 256 bytes; it recovers the buffer pages of a received packet that was subsequently rejected because of a CRC or frame alignment error; and it recycles buffer pages that the host system has already read, making those pages available again for storing incoming packets.

Please register first

Before the buffer control logic can automatically send any received message packets to the buffer memory, the local DMA channel must know where in the buffer memory it can legitimately store the incoming data. For this, special registers within the controller, called pointers, define all the buffer memory locations available to receive data. In doing so, these pointers define the receive buffer queue, a continuous string of 256-byte pages within the buffer memory.

One such pointer, page start, marks the beginning of the receive buffer queue, and a second pointer, page stop, marks the receive buffer queue's last location within the buffer memory (Fig. 3). Finally, a third pointer, boundary, indicates the starting location of those received message packets that have not yet been transferred to the host—in other words, data that must not be overwritten by additional incoming messages.

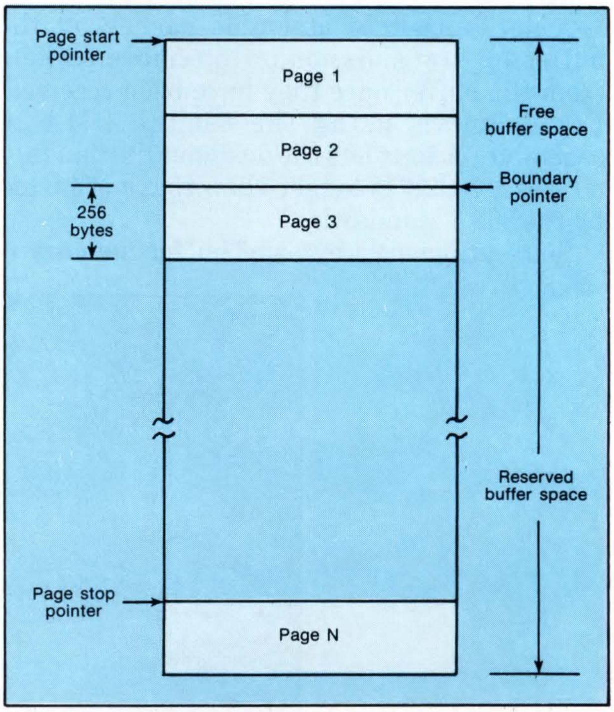
Just as the host processor must initialize these pointers before reception begins, it must also read several registers within the controller as it receives message packets. With other controllers for local networks, the processor has to interrupt the controller to read its registers; however, in storing message packets, the new controller's DMA circuit writes the contents of these registers into the buffer memory, avoiding the need for a real-time response from the host.

The information stored in the buffer memory includes the receiver's status, the number of bytes already received, and the next available buffer page (Fig. 4). The host processor can read this information when it has time without interrupting the controller. Instead of continually interrupting the host, the controller does so only to tell it to read the interrupt status register, which indicates that a message has been received.

Turning toward transmission

Not surprisingly, the operation for transmitting a message through the controller is the reverse of receiving one: The local DMA channel moves message packets from the buffer to the controller's FIFO register. Here, too, the buffer control logic directs the DMA process automatically. In this case, however, the controlling buffer pointers are the transmit page-start register, which points to the first byte in the buffer to be transmitted, and two transmit byte-count registers, which give the total number of bytes to send.

During transmission, the buffer control



3. A receive buffer queue in the buffer memory stores incoming data in contiguous pages of 256 bytes each. Two registers, the page start pointer and the page stop pointer, define the boundaries of the queue, and a third register, the boundary pointer, marks the point between data that is waiting to be transferred to the system memory and the buffer space from which data has already been transferred.

logic watches out for collisions on the line. If one occurs, it immediately resets the controller's FIFO register and restores the transmission pointers. Then the logic reschedules the transmission for another time.

Take the local to the host

In contrast to the local DMA, which handles messages between the buffer memory and the controller, the remote DMA uses an I/O port to move blocks of data between the buffer memory and the host system. The controller provides handshake signals between the buffer and the port. Using an I/O port has two important advantages. First, it separates the buffer sufficiently from the main memory so that whole data blocks can be mapped into the main memory. Second, it speeds the data flow, since, for the host's DMA controller, I/O-to-memory transfers typically take half the time that memory-to-memory transfers do.

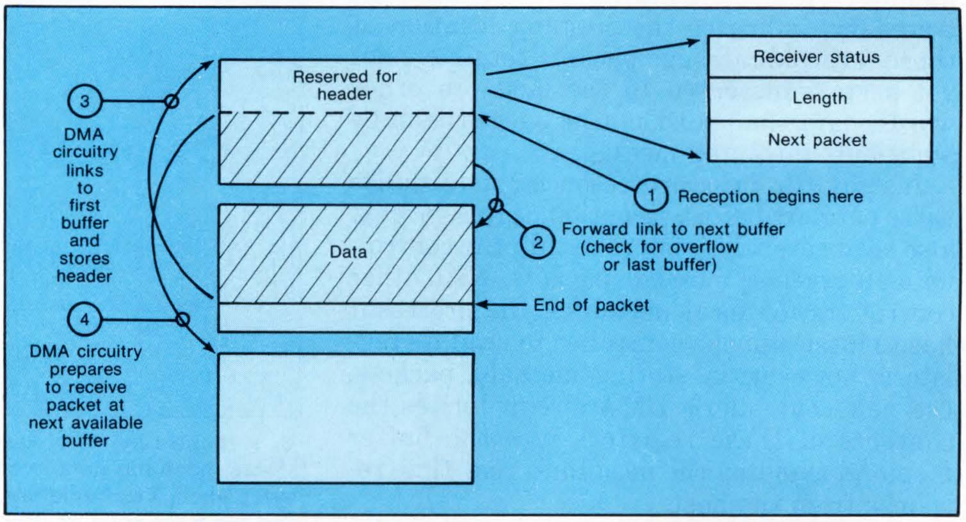
One possible role for the remote DMA is as a "spooler" either to assemble packets in the buffer for transmission or to remove packets from the buffer once they have been received. For example, using the remote DMA to assemble packets lets the designer link parts of a message that is longer than that permitted by the 802.3 standard.

Since at least 2 kbytes of buffer memory is typically available, and the maximum packet is by definition 1514 bytes (1500 of which are actual data), the remaining memory can store link control packets for reconnecting the message at its destination (Fig. 5). In this operation, the host divides the file to be transmitted into multiples of 1500 bytes or less, initializes the network header information, adds two link control bytes, and issues a Transmit command.

As each packet is transmitted, the next can be loaded (spooled) into the buffer's transmit memory without need for the host to update any of the header information (unless a packet's length changes) or to change the local or remote DMA starting addresses. This operation can be done because each packet starts from the same point in the buffer memory.

Receptive state

When the controller is in its receiving mode, the local DMA channel can send packets into the system memory, even if their location in the receive buffer queue is not known. This capability is important if the buffer's pointers have not been initialized and incoming messages threaten to overflow the buffer. The solution lies in a single command from the host that automatically causes the controller's remote DMA circuit to first read the packet's



4. The controller chip transfers into the buffer the received data and then receiver status information, the message packet length, and the address of the next available buffer page. The host's processor can read this information more conveniently from the buffer and leaves the controller free to receive other messages.

header bytes to determine the length and then transfer the packets from the I/O port to the system memory.

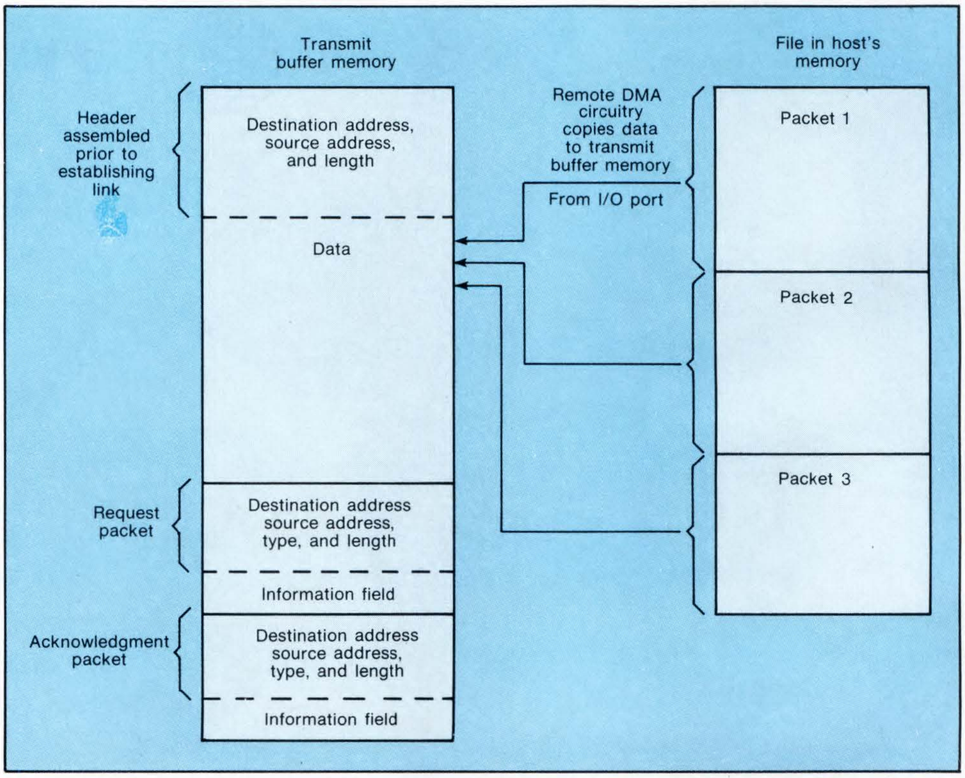
Although some other network controllers do provide DMA channels, the DMA transfer cycle is too slow to permit byte-wide transfers, and so must transfer 16 bits at a time to keep pace with the incoming data. To avoid this problem, the new controller features a minimum transfer cycle of 200 ns for 16- and 8 bit transfers. As a result, word-wide DMA transfers take as little as 12.5% of the available bus bandwidth. Byte-wide transfers, however, take twice as long and therefore twice as much bandwidth.

Different systems have different bus latencies and this is another consideration for the designer. To account for delays in accessing the system bus to transfer data, the controller's 16-byte FIFO register has a programmable threshold that determines when the DMA circuitry will issue a request to use the bus.

During reception of data, when the controller transfers incoming data from its FIFO register to the buffer memory, the threshold determines to what level the FIFO register will be emptied before a bus request is issued to send more data. If the designer anticipates delays in accessing the bus, he can program the FIFO register to issue a DMA request early enough to guarantee that the FIFO register does not overflow during reception or underflow during transmission. Also, being independent of the host, the controller has time to receive consecutive, or back-to-back, packets even though there is only a 9.6-μs delay (the interframe gap) between arriving packets.

Fine-tuning the turn-around time

A critical performance parameter for network controllers is the turn-around time in switching from receiving to transmitting. Failure to turn around in less than 9.6 μs severely penalizes a node's ability to gain fair



5. The controller's remote DMA circuitry can serve as a "spooler" for linking messages that are longer than the packet's 1500-byte capacity. First, the host processor divides the file to be transmitted into multiple packets of 1500 bytes or less. Then the remote DMA funnels each packet from the host to the transmit buffer for the controller to remove and transmit over the network.

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access to the network. The controller's freedom from the system processor lets the controller switch within 9.6 μs from receiving a message to transmitting one, decreasing the likelihood of a collision and increasing the controller's chance of accessing the network before another node does. This is particularly important in a file server application, where each single packet received can trigger the transmission of many packets. As a result, a file server's network controller must have as many opportunities to transmit as possible. Otherwise, any data requested but not transmitted will congest the file server.

Turn-around time is a function of the depth of the controller's FIFO register and the efficiency and transfer time of its DMA operation. The time needed to turn the controller around is the total time it takes to flush the FIFO register of received bytes, write four bytes of data from internal registers to memory, reinitialize the DMA to point to the packet to be transmitted, and transfer the bytes needed to fill the FIFO register.

Thus the deeper the FIFO register is, the greater the turn-around time, since more received bytes will accumulate in it. Experience shows that the new controller's single 16-byte FIFO register is of optimum depth. Moreover, to further reduce turn-around time, the chip's buffer control logic does not access any pointers in external memory in order to store or transmit a packet because these pointers are stored on chip.

Multiple addressing

Another important feature of the controller is its ability to filter multiple addresses. This lets it identify certain destination addresses that refer to more than one node. Thus a message packet intended for several nodes would carry a so-called "multicast" destination address, and the multitude of nodes that were previously assigned that address would accept the message packet simultaneously.

One advantage of multiple (multicast) addressing is that it can reduce the traffic of a network. Here the controller can serve in a gateway between a small cluster of nodes and a "backbone" network. Such filtering economizes on the bandwidth of the backbone, since only those messages intended for the backbone get through to it. In other words, the gateway monitors all the traffic on the cluster and blocks all multicast addressed packets from reaching the backbone, recognizing that they are messages for nodes within the cluster. Within the cluster, each node can be assigned its own multicast address, in addition to its unique physical address. The physical address allows any node either on the backbone or the cluster to still get in touch with any other node in the overall network.

The controller permits up to 64 different multicast addresses, well within the maximum of 30 nodes for a typical low-cost local network like Cheapernet (see p. 185). In the controller's receive status register, a bit indicating whether a multicast or physical address match occurred can also indicate whether a cluster- or network-wide packet was received. Without multicast filtering in the controller, every multicast packet would have to be accepted and filtered in software, thereby sacrificing a real-time response and burdening the host's CPU.

Monitoring and testing

As for monitoring the network and diagnosing problems, the controller has several hardware features for this job, which would be difficult to do in software. For example, it has three 8-bit tallying registers. One counts packets received with CRC errors and another counts packets with frame alignment errors.

The third register counts the number of packets lost because of insufficient buffer space or some other reason. In addition, the controller can be used as a network monitor, thanks to its ability to filter packet addresses and check the CRC codes, but it does not store any of the packets' data bytes.

By way of self-testing features, the controller can loop back a transmitted signal from one of three points. It can loop back its own output or those of its companion serial encoder or transceiver chips. Moreover, all loopback tests are conducted at the network's full 10-Mbit/s data rate.

In a typical application, the controller could serve in a local network as part of the interface for a personal computer with an 8-bit bus (Fig. 6). Four octal devices make up all the glue logic

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CIRCLE 93

Networking: 802.3 controller chip

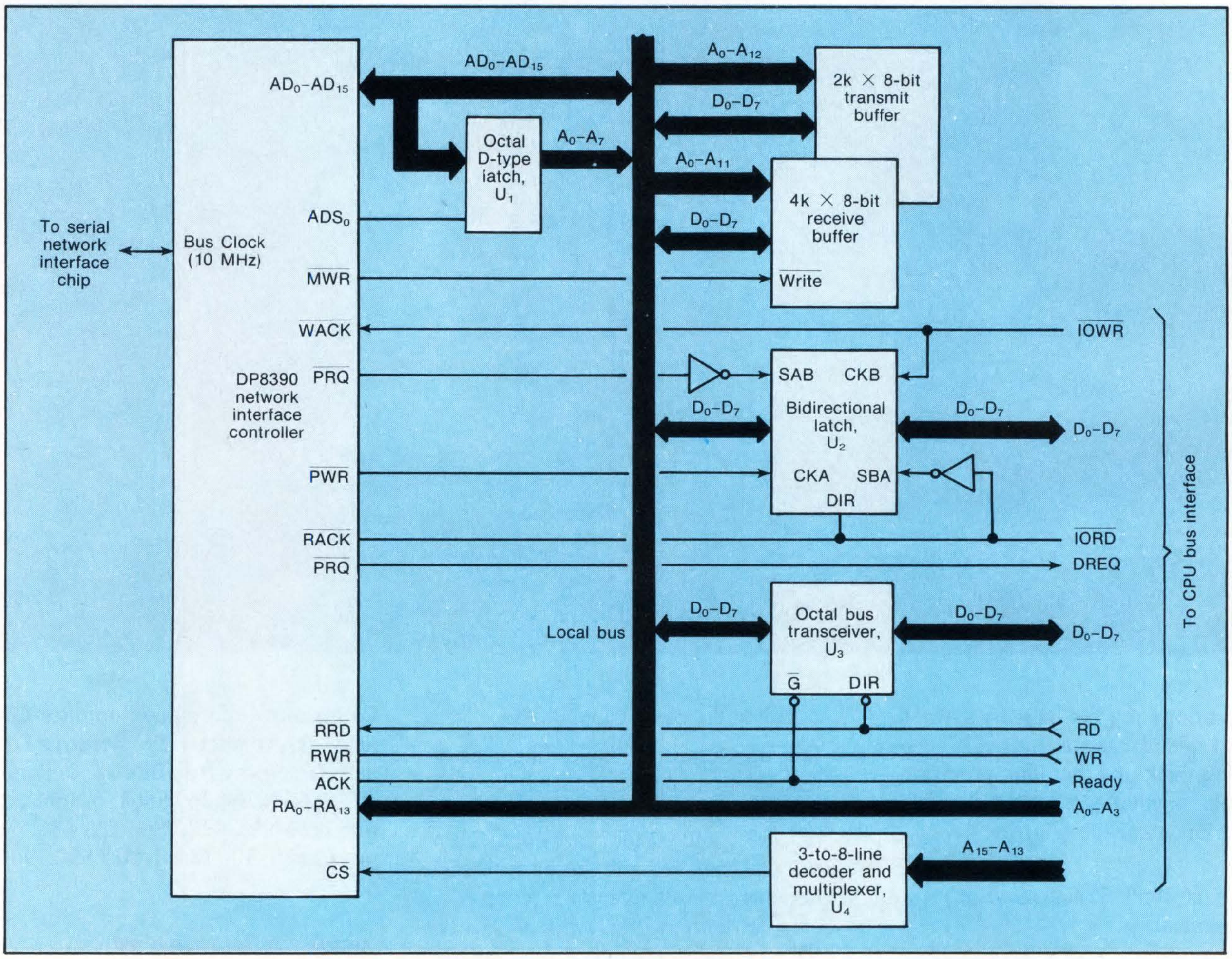
required to build the interface and turn the circuit's two memory chips into a dual-port buffer.

The first glue chip, U_1, is an octal D-type latch that demultiplexes the controller's combined address and data bus. Only one octal latch is needed for the 16 lines, because address lines AD_8–AD_{15} carry only addresses and never data (the circuit needs two octal latches when the controller is set for 16-bit transfers).

The next bus component, U_2, serves as a bidirectional latch that stores data as the latter is transferred between the local and the host system buses. The controller supplies all the handshaking signals needed by the latch, and the inverters around the latch come from spare devices in that chip.

The third glue chip, U_3, is an octal bus transceiver that gives the host CPU access to the controller's internal registers for initialization and control. The processor selects individual registers with Register Address lines RA_0–RA_3, in conjunction with the Chip Select (CS), Register Read (RRD), and Register Write (RWR) control lines. Moreover, the controller de-asserts BREQ, chip's Acknowledge output line (ACK) disables the bus transceiver during local DMA cycles to prevent the system processor from interfering during local DMA operations.

The fourth and final glue part, U_4, is a 3-to-8-line decoder and multiplexer for de-



6. Only four octal components are needed to complete the controller's interface to the 8-bit bus of a typical personal computer. U_1 demultiplexes 8 bits of the controller's 16-bit address and data bus; U_2 stores data traveling between the host and the controller; U_3 gives the host access to the controller's internal registers; and U_4 decodes the host's three most significant address bits.

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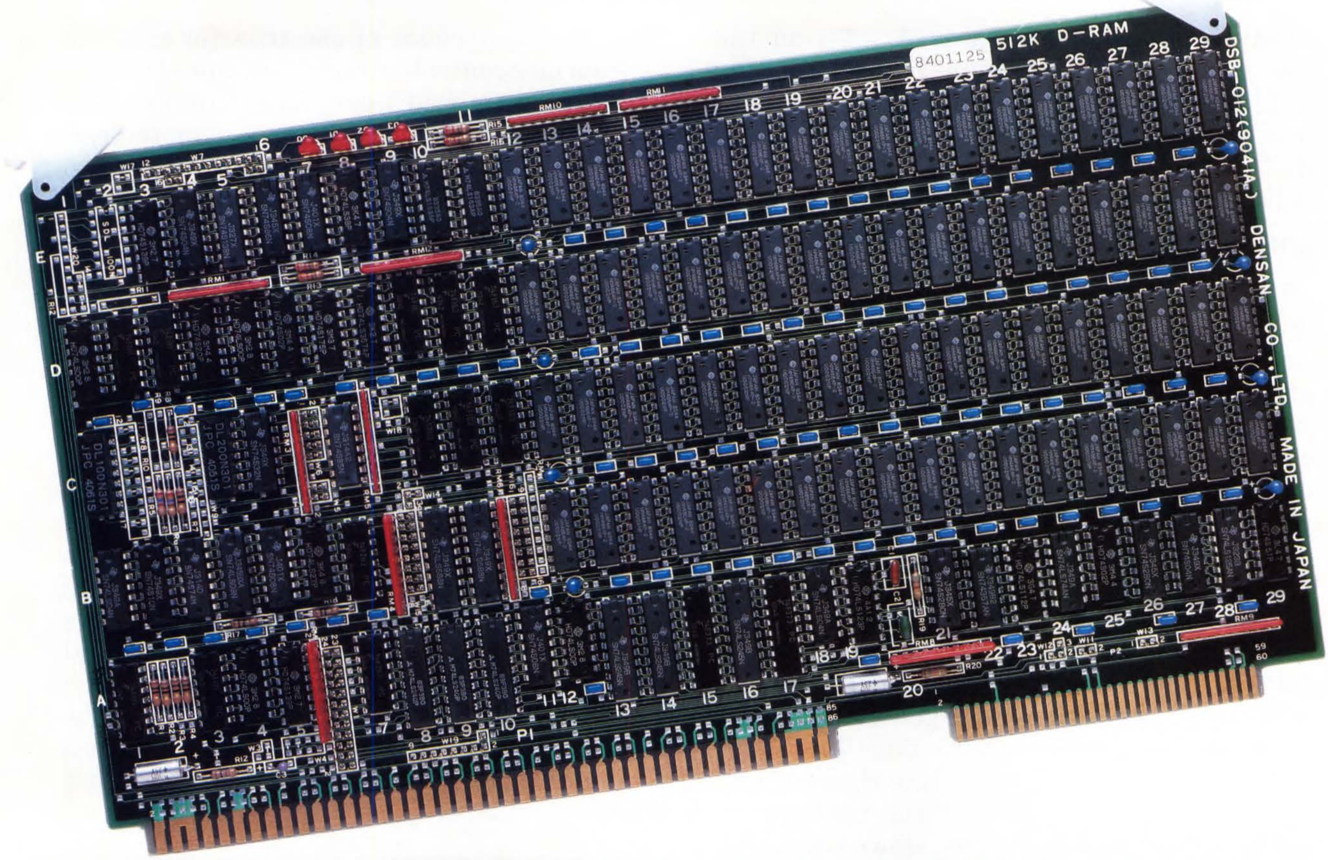

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CIRCLE 94

coding high-order addresses A_{13}–A_{15} on the host bus. To avoid additional glue logic, the buffer memory for received packets starts at hexadecimal address 2800 and extends to 37FF. For the same reason, the transmit buffer addresses fall between 1800 and 1FFF.

Buffer memory

The buffer memory itself consists of three 2k-by-8-bit RAM chips. Two form a 4k-by-8-bit receive buffer, which can store two maximum-length packets, and the third makes up the transmit buffer, with which the host can assemble and transmit up to 1500 bytes of data and a 15-byte header, the largest allowable packet.

Bus bandwidth is not of great concern on the local bus because the controller is usually the only peripheral trying to gain access to it(in other applications, a local 8-bit processor could share the bus). Therefore a 400-ns DMA cycle suffices and the designer can generate it easily by connecting the controller's Bus Clock input to a 10-MHz reference clock, like the one from the controller's companion serial network interface chip. However, this slower transfer rate means that 50% of the local bus bandwidth is used during a reception or transmission.

A typical remote DMA operation begins when the host software writes the starting address and byte count of the transfer into the appropriate controller registers. Once the registers are initialized, a command from the host starts the data transfer. For a remote read operation, the controller arbitrates access to the local bus by issuing a Bus Request signal (BREQ), and upon receipt of a Bus Acknowledge signal (BACK), it transfers data from the buffer to the bidirectional latch (U_2) under control of the Port Write strobe (PWR) (Fig. 7). When the transfer is completed, the controller de-asserts BREQ, asserts its Port Request line (PRQ), and waits until the host processor or its DMA controller reads the data. The controller repeats these steps until all the bytes designated are transferred.

During this process the controller arbitrates access to its local and remote buses, giving the remote DMA operation the lower priority. As mentioned earlier, the Acknowledge signal holds the system processor off for the duration of the DMA transfer. For a local transfer, the processor is held off the whole burst, but for a remote transfer,it is held off one transfer at a time.□

How useful?	**Circle**
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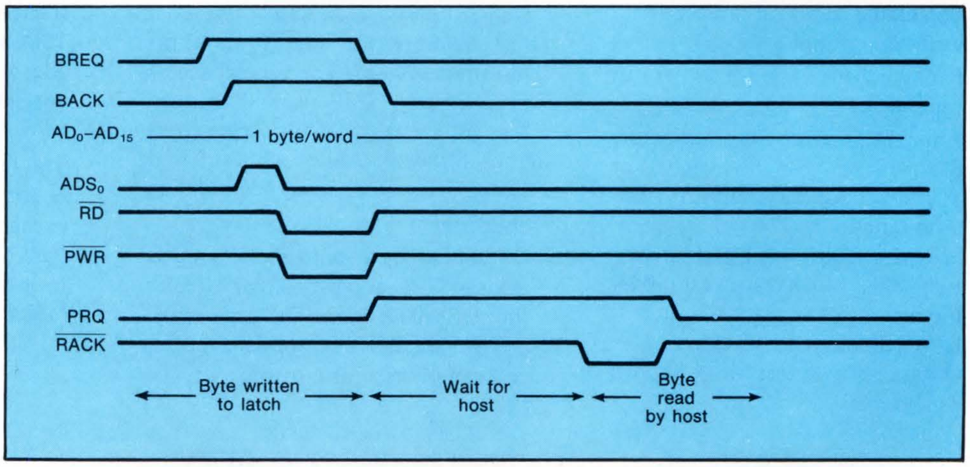

7. Once commanded by the host, the controller manages all the handshaking signals required to complete a remote DMA transfer, including those for arbitrating access to the local bus (BREQ and BACK). Under the controller's supervision, PWR strobes the data to be transferred into a latch and then asserts a PRQ line to tell the host that the data is ready to be delivered.

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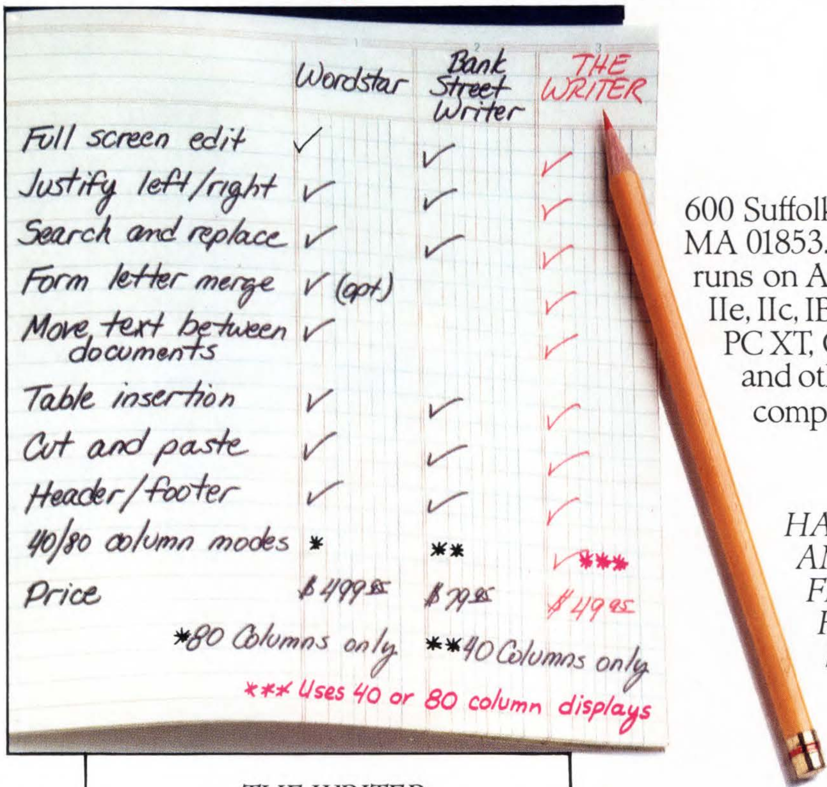

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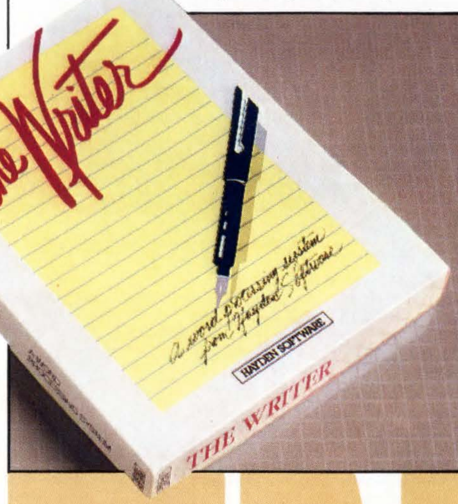

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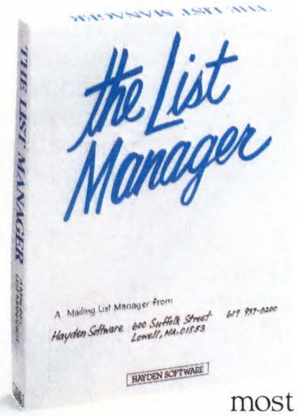

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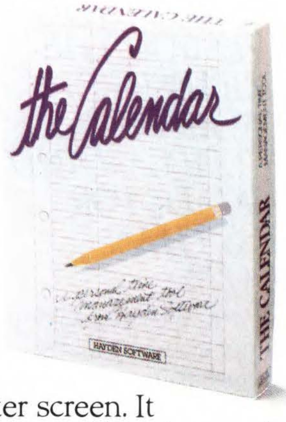

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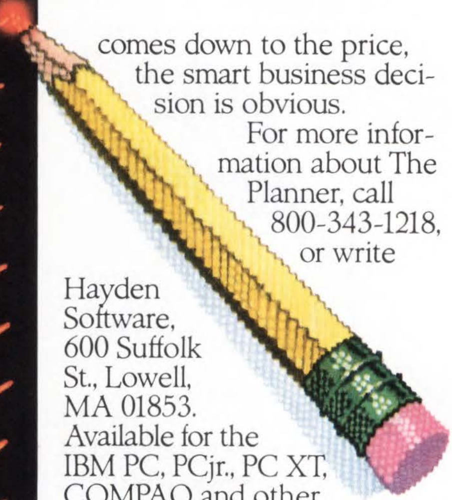

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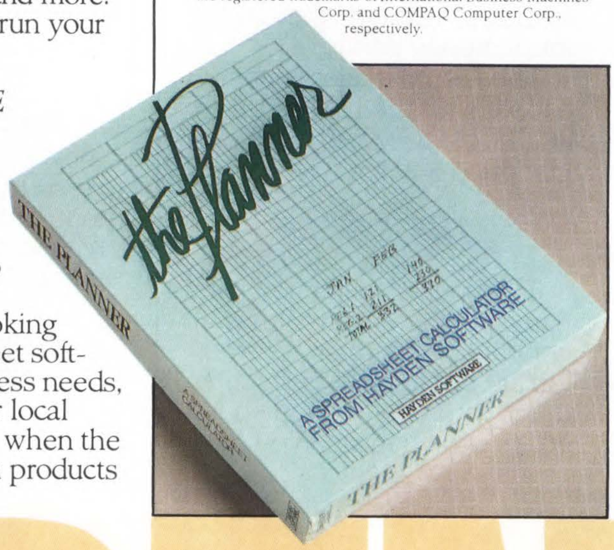

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CIRCLE 95

Manchester chip eases the design of Ethernet systems

Now the physical layer specified by Ethernet can be realized with a single chip. Even though it is built with CMOS, it still drives three 78-Ω twisted pairs.

Of the many techniques for establishing local-area networks, one seems to be leading the pack here in the U.S. and abroad: the IEEE-802.3 standard, better known as Ethernet. The specification calls for baseband signaling at 10 Mbits/s employing Manchester coding. Clearly then, a single-chip Manchester encoder-decoder that can implement the physical layer of the Ethernet protocol would be welcomed by many systems designers.

The 8023 Manchester code converter (MCC) is just such a chip. It meets or exceeds all of the requirements of the IEEE-802.3 Standard Protocol Specification and handles coding and decoding, collision detection, and carrier sensing. The encoder-decoder is capable of being looped back, making possible system diagnosis, and it contains a 20-MHz crystal-controlled clock. Basically, the chip replaces the modem used in point-to-point links.

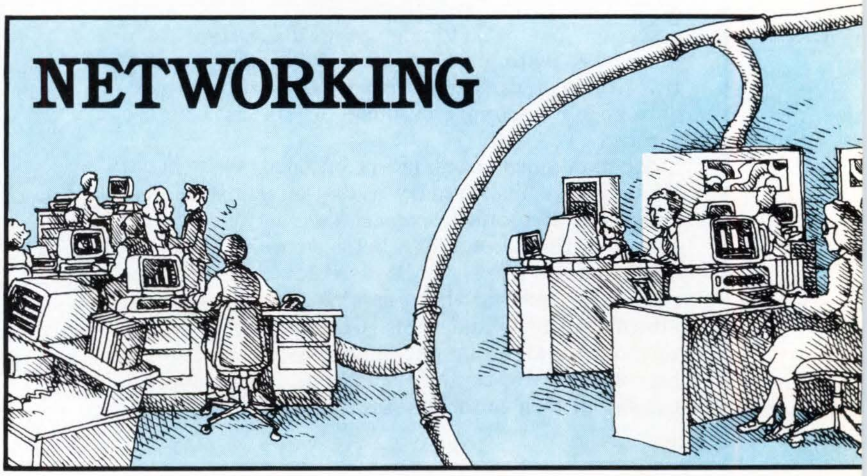
The device is powered by a +5-V supply. What's more, although it is fabricated in CMOS, the chip can nevertheless drive 78-Ω twisted-pair cables. Further, good jitter tolerance is ensured by configuring the decoder as a phase-locked loop. Doing so has an added advantage—it does away with the need to adjust the analog circuitry.

Functionally, the chip is divided into two sections, a transmitter and a receiver. The first creates a serial bit stream by exclusive-ORing the clock signal with the input data. The second derives a clock from the serial bit stream to recover the original data. A feature of this encoding scheme, known as Manchester encoding (see "Characteristics of Manchester Encoding", p. 222), is that there is a logic level transition at the center of each bit cell—

Haw-Ming Haung and **Gerald Moseley**
Seeq Technology Inc.

In 1982 Haw-Ming Haung, project manager for Ethernet product development, joined Seeq Technology in San Jose, Calif. He has been involved in microprocessor design since 1978, when he started at AMI.

Gerald Moseley, Seeq's strategic marketing manager for peripheral ICs, joined the company in 1982, following six years in international custom marketing at Signetics.



positive-going for a 1 and negative-going for a 0.

Only 15 passive components are needed to put the chip to work (Fig. 1). A 20-MHz crystal with a tolerance of 0.01% controls the transmitter clock. Each of the differential inputs of the access unit interface (AUI) is terminated by a pair of 39.2-Ω resistors, and a resistive divider supplies 3.5 V of common-mode biasing.

A pair of grounded resistors is required to bias the differential transmitter outputs. These two resistors, which must be rated at 0.5 W or more, help reduce the chip's power dissipation.

To understand how the encoder-decoder functions, consider how it would be integrated as part of a typical Ethernet node (Fig. 2). In that setting, the system interface links the host's system bus to the network. Since they replace approximately 60 MSI and SSI components, the device and its companion chip—the 8003 data-link controller—make possible an economical implementation of both the physical layer and the data link layer of the Ethernet protocol.

As the block diagram shows (Fig. 3), seven signal lines connect the encoder-decoder and the controller, and three 78-Ω twisted pairs form the link with the access unit interface. In addition, there is a loop-back control signal (LPBK).

In the beginning

Data encoding and transmission start with Transmitter Enable (TXEN) going active (high). As long as TXEN remains high, which it

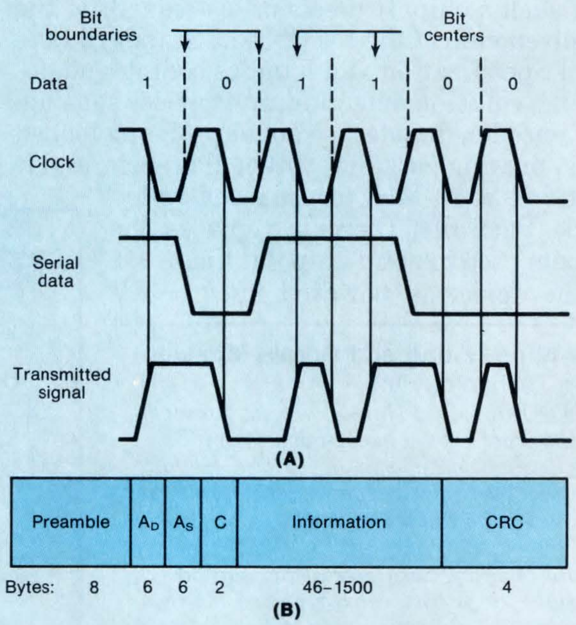
Characteristics of Manchester encoding

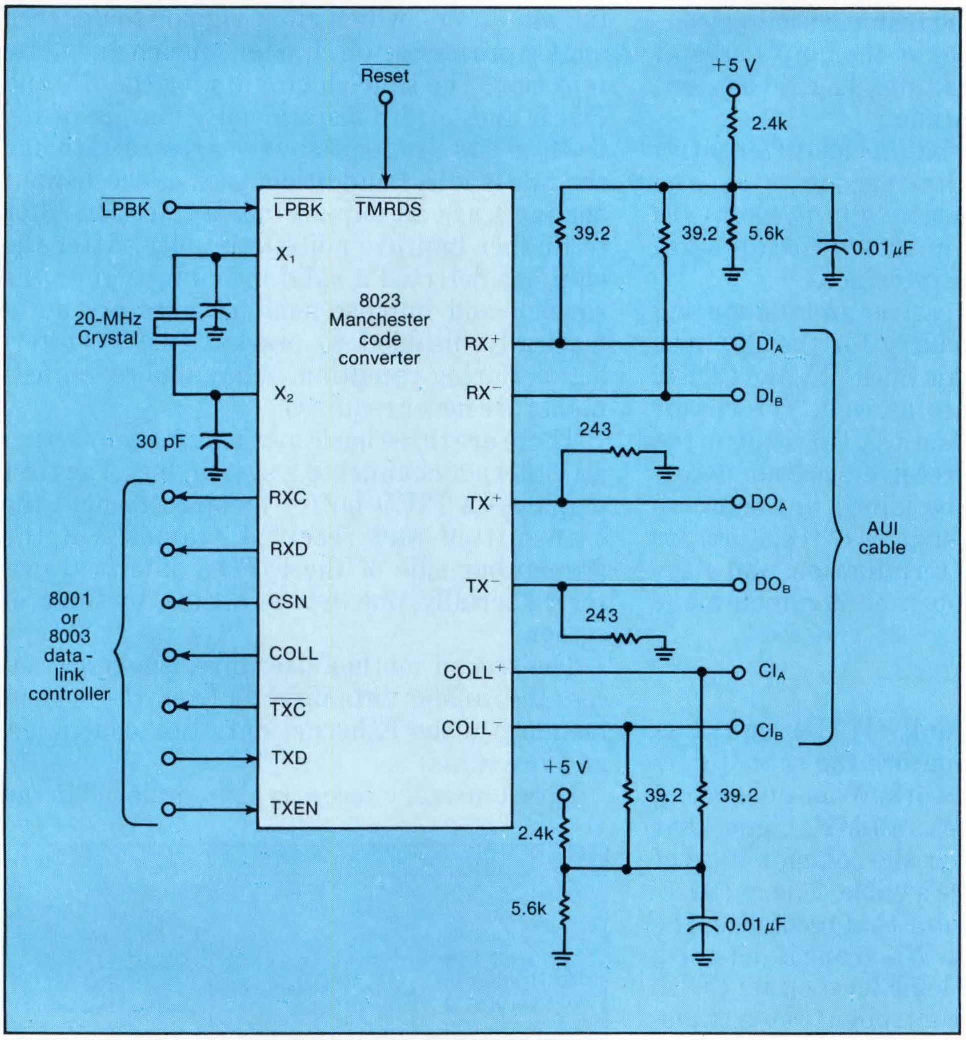
In Manchester code, each bit is encoded by a zero-crossing signal transition (Fig. A). A 1 is encoded as a low-to-high transition and a 0 as a high-to-low transition. Further, there is a continuous supply of bit-framing information in a Manchester decoder, since each bit has a transition at its center.

On IEEE-802.3, or Ethernet, networks, messages are sent as a series of one or more formatted packets (Fig. B). The packet begins with the preamble, an 8-byte field used to synchronize the receivers. The preamble is a series of alternating 1s and 0s, so the resultant signal is easily synchronized. The preamble always ends with two 1s, which the receivers use to synchronize the bytes. Following the preamble are two 6-byte address fields, the first for the message destination and the second for the source. A two-byte field labeled C gives the byte count for the information field to follow. There can be 46 to 1500 bytes in the information field. The last field is a 32-bit CRC (cyclic redundancy code) used for error detection. The packet ends with a delimiter, a two-bit period lasting 200 ns during which no signal transitions occur. The delimiter is, of course, a non-data code and cannot be mistaken for data by the receiver.

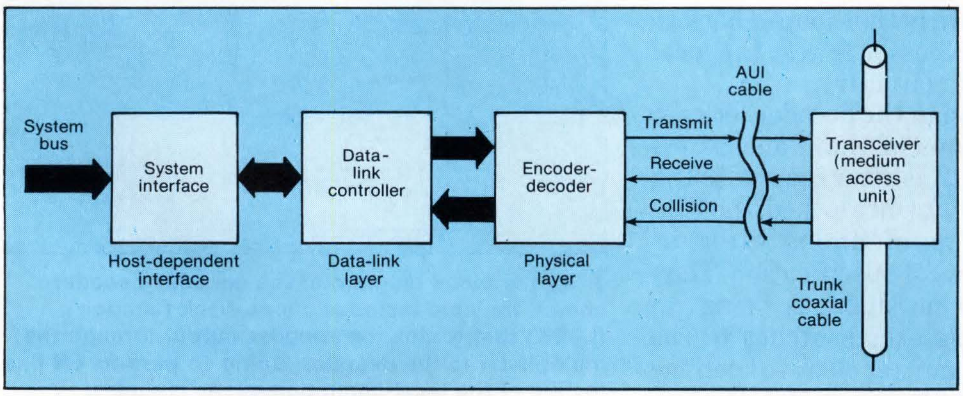
As mentioned, each bit is encoded as a signal transition. A bit-boundary transition is inserted between two like bits to correct the line polarity for encoding the second bit. Between unlike bits, no bit-boundary transition is necessary. That is the reason for making the preamble field a packet of alternating ones and zeros. Obviously, such a pattern eliminates the bit boundary transitions—leaving only bit-center transitions. It is thus the easiest pattern to employ for synchronizing receivers on the network.

In each bit window the signal is high for half of the time and low for the other half; therefore, the Manchester-encoded signal has a constant dc component. That feature is used in the IEEE-802.3 protocol for detection of collisions. The cable drivers used for Ethernet are current-mode drivers. Thus when a collision occurs, the dc average on the line will double, since the two currents will be added. Collisions are detected by monitoring the dc voltage on the cable, averaged over a few bit times.





1. A 20-MHz crystal, four capacitors, and ten resistors are all that is required to turn the 8023 Manchester code converter into a complete realization of the physical layer of the Ethernet protocol.



2. In a typical Ethernet node, two chips—the data-link controller and the encoder-decoder—do the job formerly done by about 60 SSI and MSI devices.

does for the length of the frame, encoding continues under the control of the chip's crystal clock. At the end of the frame, TXEN goes low, terminating the transmission.

The chip carries a balanced differential driver for connecting its transmitter to the access unit interface cable. Only two bias resistors—and no active interface circuits—are required to complete the interface.

The differential line receiver and the squelch and noise-rejection circuitry for the Receiver and Collision twisted-pair lines (RX and COLL, respectively) are on-chip as well. The circuit will not react to noise when a signal is not on the line. Also, external line receivers are not necessary; these inputs can be joined to the access unit interface cable using two resistors for dc biasing, two for line termination, and a bypass capacitor for proper ac common-mode termination.

Listening in

The medium access unit (MAU), or transceiver, continuously monitors the cable to detect collisions on the network. When one occurs, the transceiver generates a 10-MHz signal that is carried to the chip over the collision lines of the access unit interface's cable. The encoder-decoder contains a detector that recognizes the 10-MHz Collision signal. When one is detected, the chip asserts a high logic level on its COLL pin to tell the data link controller to stop transmitting until the interference has passed.

In the loopback mode, encoded data is switched to the PLL decoder instead of the RX outputs. The Transmitter inputs (TX) are muted. Transmitted data is thus looped back to the communications processor to test the local transmitter and receiver circuitry.

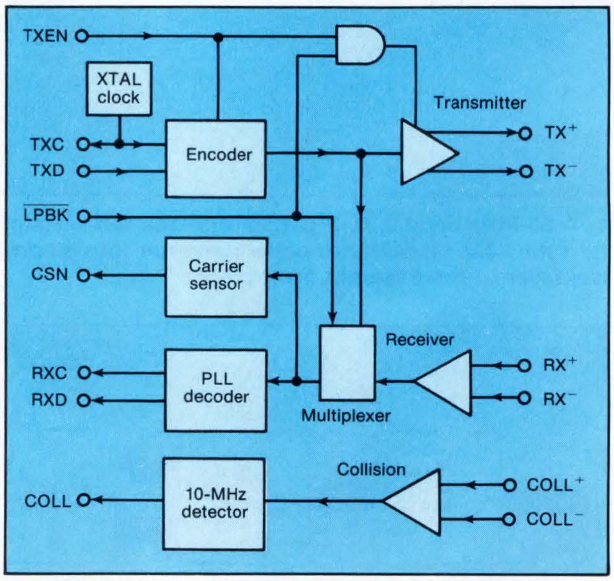
The phase-locked loop in the decoder locks to the bit-center transitions of the Manchester-encoded signal within 1.2 μs after the beginning of the frame (12 bit times). Once locked, the PLL can tolerate up to 18 ns of timing jitter, as allowed by the IEEE-802.3 specification. During idle periods, when no signal is being received, the input multiplexer switches to the crystal-controlled transmitter clock to keep the receiver clock running at precisely 10 MHz.

The line receiver input stages for the RX and COLL signals are linear-responding differential amplifiers, which allow signals to undergo analog processing on chip for squelch and noise rejection. The squelch circuits for the RX and COLL lines afford a static noise margin of 160 to 340 mV to eliminate spurious responses when the line is idle. In addition, each of these input channels has an impulse-noise-rejection filter to further improve noise immunity. After the chip has detected a valid incoming signal, the squelch and impulse-noise circuits are automatically disabled to prevent further interaction during reception. What's more, adjustments are never required.

There are three basic methods for connecting an Ethernet channel to a system bus. The first employes a FIFO buffer memory to hold the transmitted and received frames. On the system-bus side of the FIFOs, data is transferred serially, one byte at a time, by the processor.

The second method uses direct memory access to transfer data directly from the system memory to the Ethernet data-link controller, and vice versa.

Direct memory access is also employed in the



3. As the block diagram of the encoder-decoder shows, the chip includes a loop-back function (LPBK) that routes the encoder output through the multiplexer to the decoder. Doing so permits off-line testing of the local communications circuitry.

third approach. In this case, a temporary buffer memory is put in place between the system memory and the encoder-decoder chip. The intervening buffer relieves the system bus of some of the pressures imposed by the traffic and timing requirements associated with the channel.

High-speed driving

As mentioned, the data transfer rate for Ethernet is 10 Mbits/s, so data transfers during active periods must take place at 1.25 Mbytes/s. If the DMA controller cannot work at this speed, frames will be lost. Additionally, if the system is to handle loopback diagnostics, both the transmission and the reception DMA channels will have to operate simultaneously, together transferring 2.5 Mbytes/s. Clearly, not all DMA controllers can accomplish that.

Speed is only a problem for systems with heavy traffic or when response timing is critical. The transfer of data on the system bus can sometimes consume a considerable percentage of the bus time, at least in short bursts. If that is a problem, a dedicated buffer memory can be used to offload the system bus.

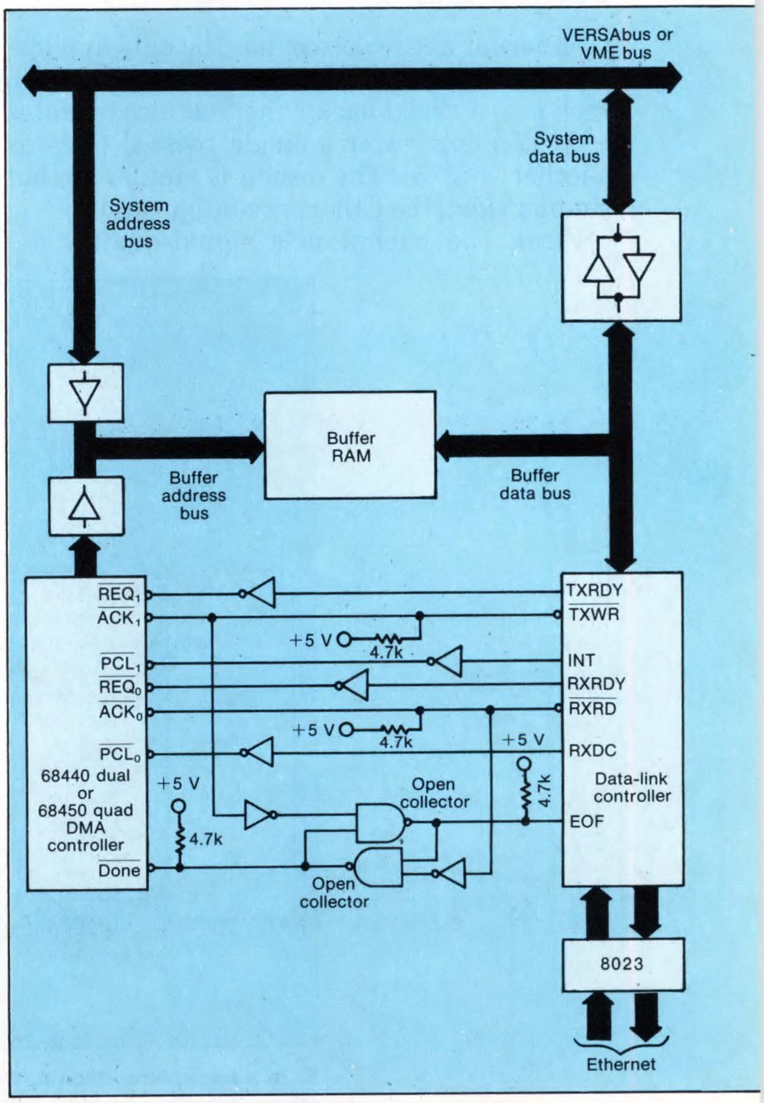
As an example of how such a memory is hooked up, consider the interface for a 68000-based system (Fig. 4). In connecting the encoder-decoder to a 68440 or a 68450 DMA controller, it should be borne in mind that the request lines on the controller can be programmed to be level- or edge-sensitive. In this case, level sensitivity is selected by setting the appropriate internal control bits. The Transmitter Ready output (TXRDY) of the data link controller drives the request line for channel 1, and the Receiver Ready output (RXRDY) requests channel 0. The acknowledge lines on the DMA controller can be connected directly to the chip's Transmitter Write and Receiver Read inputs (TXWR and RXRD).

Finishing the Frame

On the 68440 and the 68450, the End of Frame pin (EOF) is identified as Done. The Done pin links to the encoder-decoder's EOF pin through an inverting bidirectional transceiver. The signal terminates the channel activity at the end of the frame.

The $\overline{PCL_0}$ and $\overline{PCL_1}$ lines on the DMA Controller, which are programmable inputs associated with channel 0 and channel 1, are put to good use in this application. By setting the internal control bits, $\overline{PCL_1}$ will interrupt the processor so it will read the device's status register.

Doing so is useful for a variety of network conditions. For instance, if 16 consecutive collisions occur, network diagnostics or an alarm (or both) can be ordered by interrupting the processor. The status code that generates the interrupt is read by the processor from the



4. A fast buffer memory and DMA controller can relieve the system bus of the traffic and timing requirements demanded by Ethernet. In this case, the system bus is a VERSAbus or VMEbus, and the DMA controller is a 68440 or 68450.

chip's internal status registers.

The PCL_0 input can be programmed to restart channel 0, the reception channel. In this mode, sending PCL_0 low will automatically reinitialize the channel. The pin is driven by the data link controller's Receiver Discard (RXDC) line. RXDC goes high following the reception of a bad frame or a frame fragment. That will, in effect, discard the bad data and restart the reception channel without the need for processor intervention in setting up the channel.

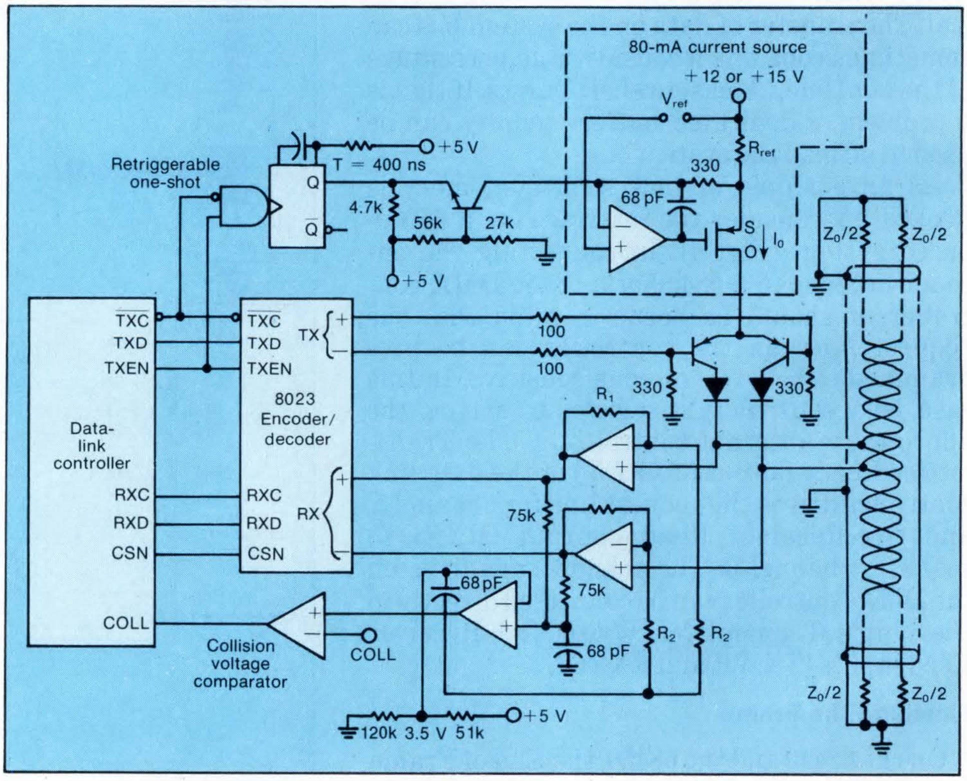
A second home

Ethernet networks are not the only applications where the encoder-decoder can be put to good use. A serial backplane that also operates at 10 Mbits/s—over a single twisted pair—is another (Fig. 5). The design is similar to, but simpler than, the Ethernet configuration.

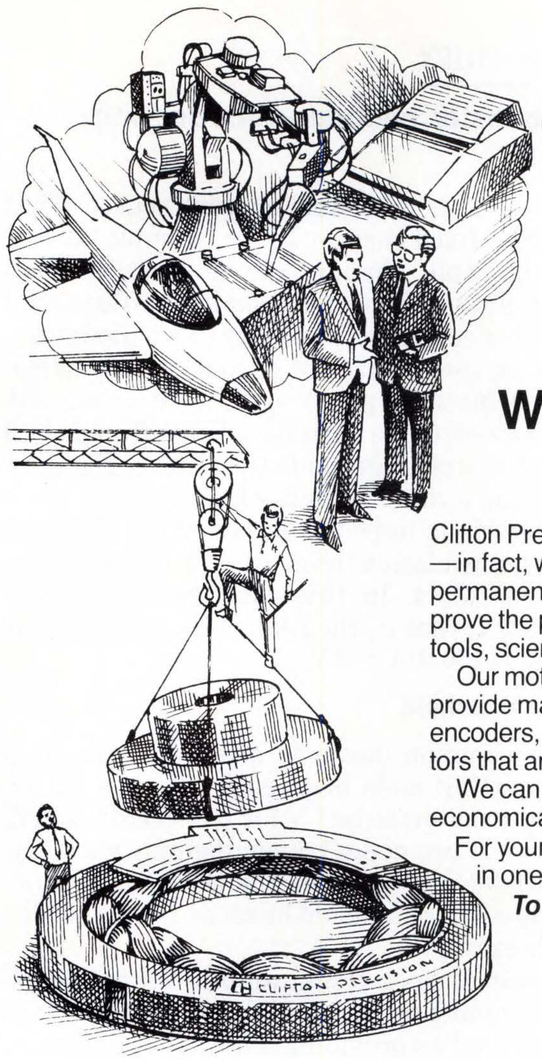
First, the backplane's signal-quality demands can be relaxed, since shorter distances are spanned. Second, the medium access unit can be set up locally rather than remotely. That eliminates three medium access unit subsystems: the dc-dc converter used to power the units; the access interface unit's cable and its associated transformers, drivers, and receivers; and the 10-MHz oscillator and detector used for collision signaling on that cable. Moreover, the need for the TX carrier-sensing function in the medium access unit for keying the transmitter is obviated.

In a typical serial backplane, the transmitter is keyed (enabled) when TXEN goes high. Under one-shot control, it stays keyed for 400 ns after TXEN goes low. The 400-ns delay ensures keying coverage for the end-of-frame delimiter—200 ns of unbroken high level on the line right after the last bit of the frame.

A high level on the Q output of the one-shot



5. In a backplane design, the medium access unit can be local, rather than remote, which greatly simplifies the interface. For one thing, since the signals only have to cover short distances, signal requirements can be eased.



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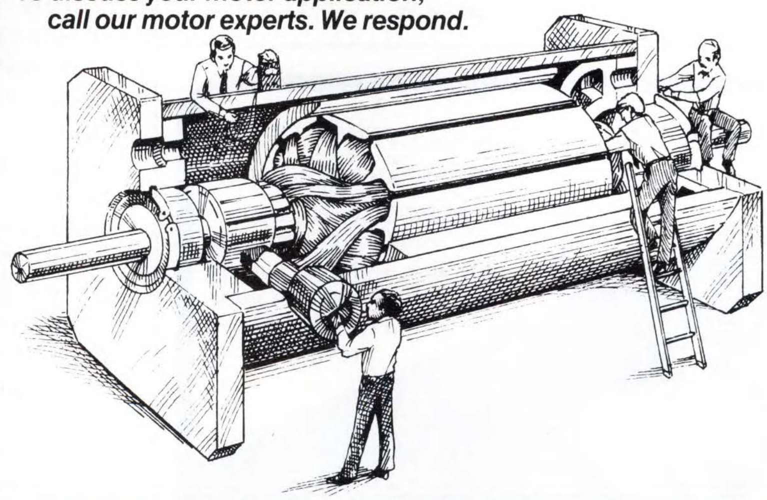

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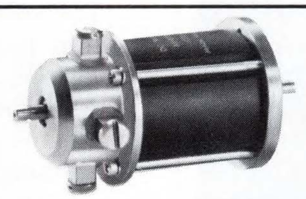

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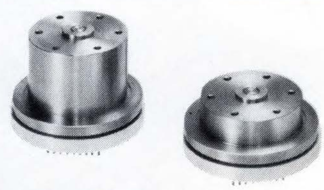

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CIRCLE 96 CIRCLE 97 CIRCLE 98

DESIGN ENTRY

Manchester encoder-decoder chip

turns on the switchable current source. That sources a fixed current I_0, for example 80 mA, into the cable. During transmission, the balanced line is driven through a differential current-steering output stage. Two diodes are placed in series with the output drivers to isolate the line when power to the node is removed. The twisted pair is terminated at both ends by a pair of matched grounded resistors. Each resistor has a value of $Z_0/2$, where Z_0 is the line's characteristic impedance, say 100 Ω. Thus the peak transmission level at the transmitting node is $I_0Z_0/4$. In this case, the expression equals 2 V, that is, the peak voltage is given by $80\ \text{mA} \times 100\ \Omega/4 = 2\ \text{V}$.

At the threshold

The common-mode dc offset created by a transmitting node is given by $V_{CM} = I_0Z_0/8$, which turns out to be 1 V for $I_0 = 80$ mA and $Z_0 = 100\ \Omega$. If two nodes transmit simultaneously, V_{CM} would double. Thus the threshold for detecting collisions should be set at 1.5 V_{CM}, which in this example is 1.5 V.

A pair of operational amplifiers at the receiver input presents a high impedance to the line, as well as providing a means of adjusting the common-mode voltage. The pnp input transistors on those two amplifiers maintain their high impedance when unpowered. The third amplifier (with the two 68-pF capacitors) furnishes feedback that is proportional to the time-integrated difference between the received common-mode voltage (which comes from the two 75-kΩ resistors) and 3.5 V. The result is that the RX inputs are biased at a common-mode voltage of 3.5 V, which is ideal for the encoder-decoder.

The voltage from the integrating amplifier, which is given by $(1+R_2/R_1)V_{CM}-3.5R_2/R_1$ (where V_{CM} is the common-mode voltage on the line) is compared with V_{COLL} to determine if a collision has taken place. With $V_{CM} = 1.5\ I_0Z_0/8$, the detection threshold, $V_{COLL} = (1.5\ I_0Z_0/8)(1+R_2/R_1)-3.5\ R_2/R_1$.□

How useful?	Circle
Immediate design application	556
Within the next year	557
Not applicable	558

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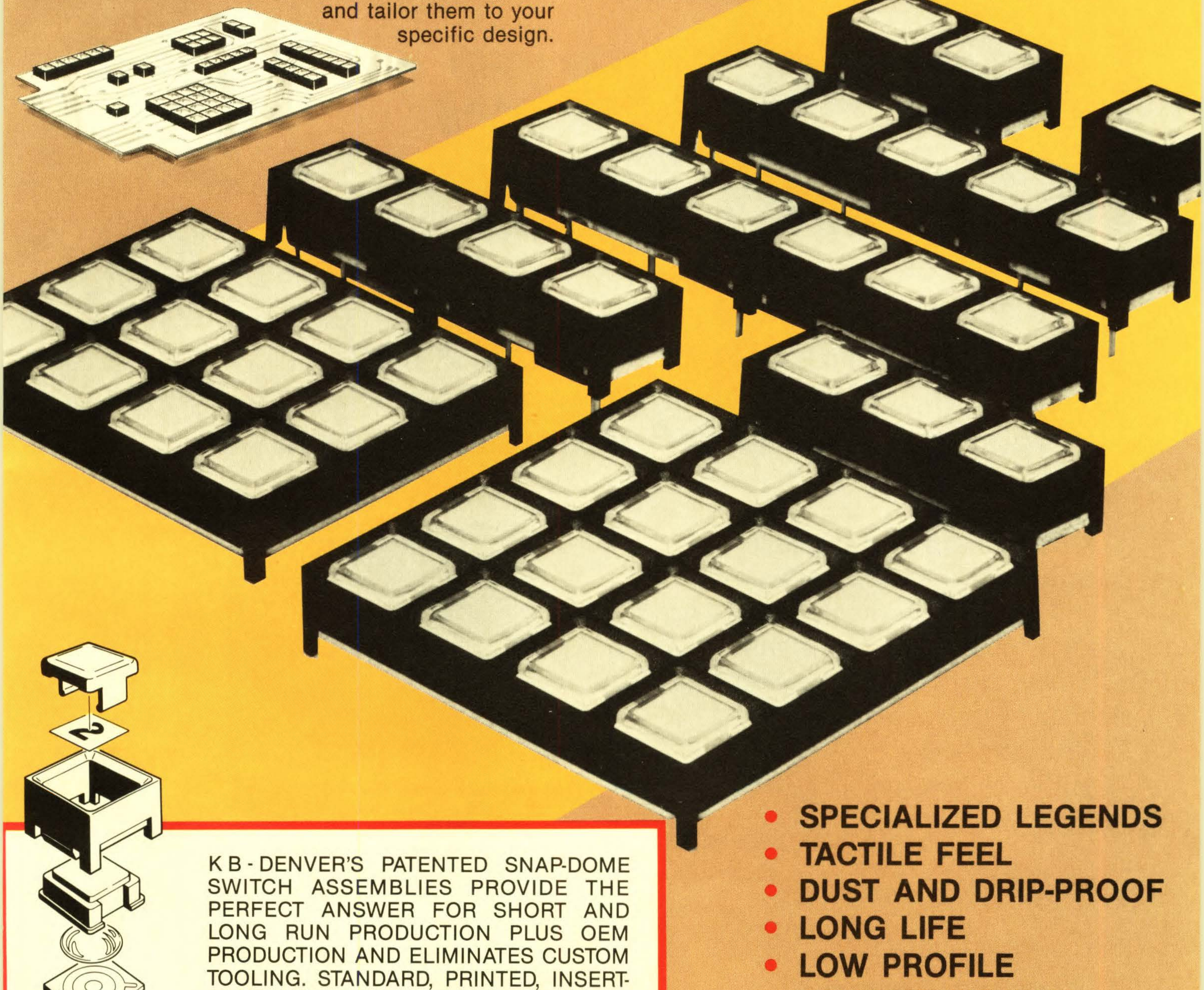

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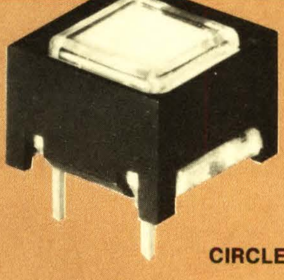

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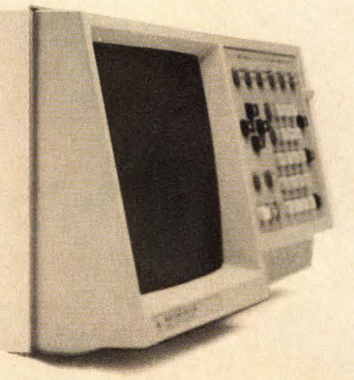

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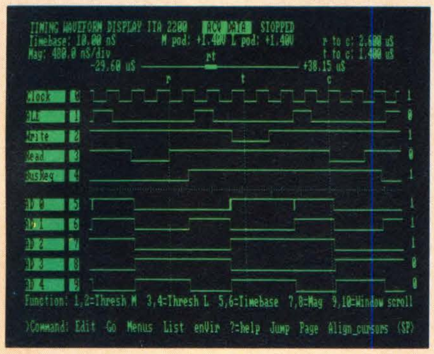
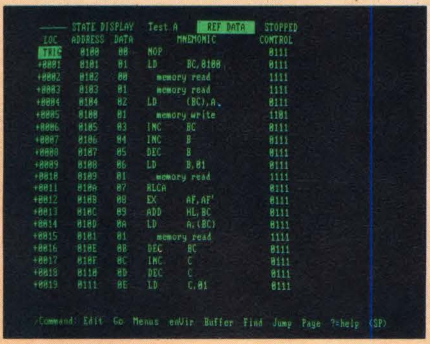


The μAnalyst Interactive Timing Analyzer directly targets on the problems encountered during hardware design. Included are features like edge-oriented data acquisition, and special triggers for conditions such as setup and hold violations.

FEATURE	μANALYST	HP 1630
Channels/MHz	16/100	16/100
Transitional timing	yes	no
No. trigger modes	5	2
Sync/async acquisition	yes	no

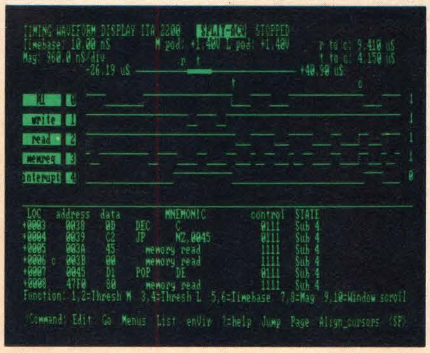
For software designers: A clean sweep.



The μAnalyst Interactive State Analyzer gives you enough channels and triggering power to debug complex systems built on 16-bit processors like the MC 68000. You even get symbolic definition to set trigger conditions in source code terminology.

FEATURE	μANALYST	HP 1630
No. channels (maximum)	80	65
No. trigger levels	15	5
Usable word recognizers	60	5
Symbolic definition	yes	no

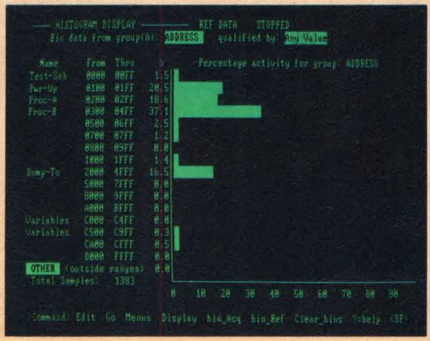
For hardware/software integrators: An easy win.



The state and timing sections of the μAnalyst are cross-linked so each can arm or trigger the other. Better yet, display your state and timing data in a time-aligned manner to see the true relationship between software execution and hardware bus timing.

FEATURE	μANALYST	HP 1630
State arms/triggers timing	yes	yes
Timing arms/triggers state	yes	yes
Combined state/timing display	yes	no
Time-aligned data display	yes	no

Post-acquisition processing: Clearly no contest.



Since the μAnalyst mainframe is closely coupled with a personal computer, you have almost unlimited data processing capability. Use the PC to write and run Pascal programs which post-process your acquired data.

CAPABILITY	μANALYST	HP 1630
Disassembly of μP code	yes	yes
Component verifications	yes	no
Custom programming	yes	no
Performance analysis	yes	yes

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1. Price quoted 5/25/84
2. Does not include personal computer

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CIRCLE 102

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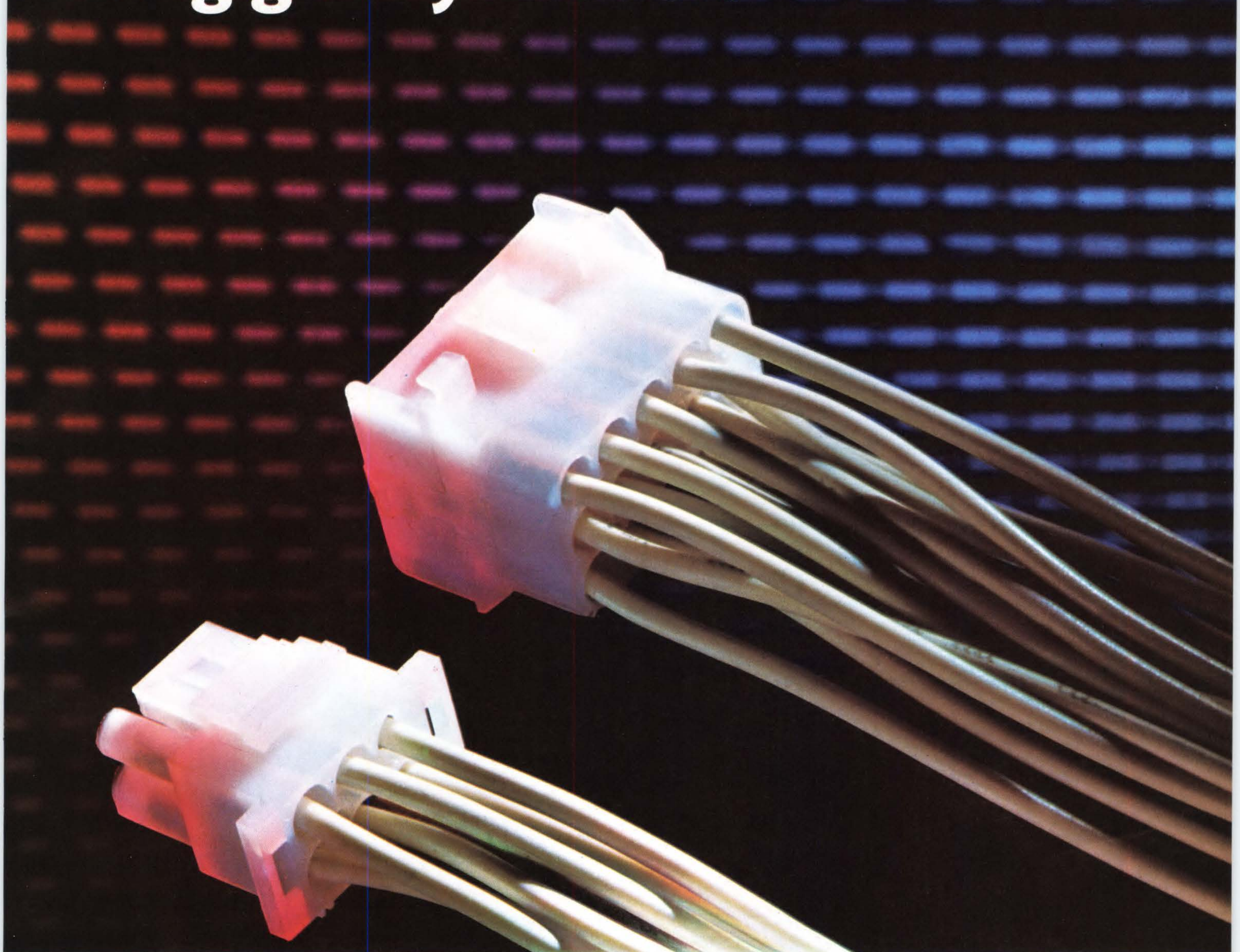

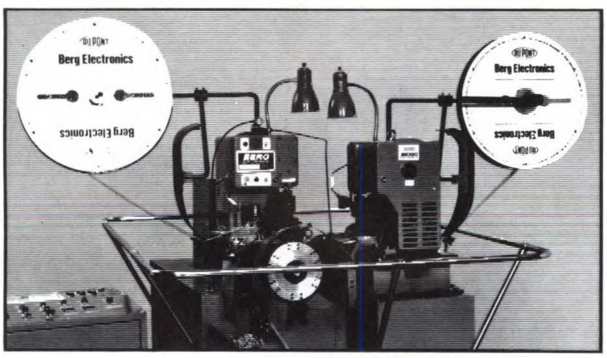

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CIRCLE 103

32-bit microprocessor reaps the benefits of a host of enhancements

Improved on all fronts, a 32-bit processor performs four times as fast as its 16-bit kin, works with a larger instruction set, and handles more data types.

There is no doubt that the day of the 32-bit microprocessor has dawned, bringing with it almost undreamed of potential and power. One such processor is based on and compatible with one widely used family of 16-bit devices, the 68000. The latest addition to the group, however, runs at 16 MHz and aims at better than four times the performance of its 8-MHz predecessors. Indeed, in all respects the 32-bit device is intended to surpass its forerunners. It handles a greater number of addressing modes, and is replete with new and more powerful instructions that work with more data types.

Doug MacGregor, Dave Mothersole, and **Debra Winpigler,** Motorola Inc.

After serving in the navy, Doug MacGregor went on to complete a BA in history and Asian studies and to take an MS in computer science at the University of Illinois. He has been a designer with Motorola's Microprocessor Design Group (Austin, Texas) for four years and wrote the microcode for both the 68010 and the 68020.

Dave Mothersole has been with Motorola since 1978 and is the project manager for the 68020 design group. He is a member of the IEEE and holds a BSEE and an MSEE from the University of Texas at Austin.

Currently a systems engineer at Motorola, Debra Winpigler has worked for the company for three years. She holds a BSEE from Pennsylvania's Lafayette College and handled the testing of the 68020's coprocessor interface.

Many improvements in the MC68020 are the result of software enhancements. For example, the addressing modes make the use of high-level languages straightforward and simple. The expanded instruction set contains a number of 32-bit commands to fill in gaps in the 68000's and the 68010's sets. In addition, several added instructions handle new types of data and supply solutions to some special-purpose computations.

One major enhancement is the set of coprocessor instructions, which makes possible the coprocessor interface. Because the 68020 is a general-purpose machine, it cannot handle all special-purpose computations in the most efficient way. For that reason, the coprocessor interface has been added, augmenting the processor's by allowing both special-purpose coprocessors (e.g., floating-point, FFT, and string devices) and user-defined coprocessors to work easily with it.

Although all members of the 68000 family have 32-bit user registers, internal registers, and operands, the 68020 is the first to incorporate a full 32-bit data path, two 32-bit internal register paths, a 32-bit instruction unit, three 32-bit arithmetic units, and a 32-bit instruction cache (Fig. 1). The last is well known to users of mainframes as a way to increase performance while exacting a relatively small penalty in system complexity. In this case, the device's 256-byte cache makes possible a significant increase in execution speed by reducing the number of fetches to external memory.

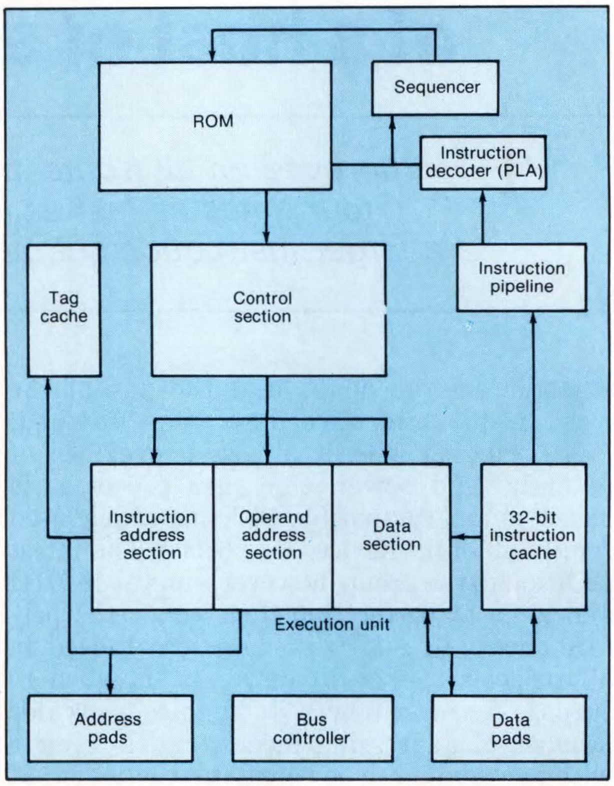
Equally important, the processor maintains strict object-code compatibility with earlier family members, since source code is usually not available for recompilation. Compatibility is a critical issue to many users because of their large investment in software and software development.

Although the 68020 is perfectly user-object-code-compatible with the 68010, there are differences in the processor's supervisor code. By restricting code changes to the exception-handling routines, it is possible to design a 68010-based processor board, alter the exception-handling routines, and upgrade a system originally designed for a 68010 or a 68000 in a very short time. Even though that approach does not take advantage of all of the 68020's powers, it does allow a system to be created with an existing design and turned around very quickly. Later, it can be fitted with the software necessary to take advantage of the entire spectrum of the 68020's extensions.

Following more instructions

The improved instruction set comprises that of the 68010, as well as instructions that recognize new data types and addressing modes. The 68000 family works with data that consists of bits, bytes, words, long words, and binary-coded decimal (BCD) operands. The updated data types handle variable-width bit fields, packed BCD, and variable-byte-length operands.

Up until now, the 68000 family used 14 addressing modes, which included register direct, register indirect (with predecrement, postincrement, displacement, and indexing), absolute, immediate, program counter relative, and implied effective types. To those, the 68020 adds a host of addressing capabilities by expanding



1. All of the MC68020 microprocessor's internal hardware is capable of handling 32 bits. The CPU contains an execution unit, ROM control stores, decoder PLAs, an instruction pipeline, and a control section.

Table 1. New addressing modes

Data space		Program space	
Mode	**Assembly language syntax**	**Mode**	**Assembly language syntax**
Direct	(bd, An, Xn.sz*scl)	PC Direct	(bd, PC, Xn.sz*scl)
Pre-indexed indirect	([bd, An], Xn.sz*scl, od)	PC Pre-indexed indirect	([bd, PC], Xn.sz*scl, od)
Post-indexed indirect	([bd, An, Xn.sz*scl], od)	PC Post-indexed indirect	([bd, PC, Xn.sz*scl], od)

bd = Base displacement (0, 16, 32 bits)
[ ] = Memory indirection
An = One of eight 32-bit address registers
Xn = Indexed register, one of 16 data and address
PC = Program counter
od = Outer displacement (0, 16, 32 bits)
sz = Index register size (16 or 32 bits)
*scl = Index register scaling (1, 2, 4, or 8) i.e. multiplication by 1, 2, 4 or 8

the index-addressing modes to include memory indirection, a full range of displacements, index scaling, pre-indexing, and postindexing (Table 1). These extensions are found in both the program and the data address spaces. Further, the descriptions are not complete, since any element can be suppressed in the calculation.

The index register itself can be either a data or an address type and can be set up for either a word or a long word. What's more, it can be scaled by 1, 2, 4, or 8. Memory indirection, represented by brackets, indicates that the address within them fetches a long word. That address is then used in the remainder of the effective-address calculation. Two displacements are available when the mode is used, but they both can be suppressed if desired. When full addresses are not needed, a briefer format can be substituted that allows for fast indexing, scaling, and an 8- or 16-bit displacement.

What's in a mode?

The significance of the addressing modes lies in their suitability for high-level languages: They are able to express more naturally the structures associated with such languages. Further, they not only improve performance, but also make compiler-generated code much more efficient.

Additionally, a complement of extensions brings all the advantages of 32-bit processing to the instruction set. For example, the multiplication and division commands (MULS, MULU, DIVS, DIVU) now operate on 32-bit operands. It is possible to multiply two 32-bit operands to yield either a 32- or a 64-bit product. Also possible are 64-by-32-bit and 32-by-32-bit divisions. The displacements affecting the Branch on Command Code (BCC) instructions and the BRA, BSR and Link commands have been expanded from 16 to 32 bits as well. That expansion permits branch and link instructions to be employed without concern for distance between the branches. What's more, the Move Control Register (MOVEC) instruction has been enlarged to accommodate the new control registers.

All told, over 20 instructions increase the set's range of functions (Table 2). The coprocessor-related statements are important for special-purpose processing. Another group of instructions enables variable-width data fields to be manipulated. A bit field up to 32-bits long—spanning as much as 5 bytes in memory—can be cleared, set, complemented, extracted, inserted, scanned, and tested. These instructions are particularly good for handling packed data in communications and graphics applications. One of their features is that they make it possible to specify bit fields of 1 to 32 bits in memory regardless of the alignment of the specific field. Also, if the field encompasses the maximum number of bytes, the processor recognizes the condition and makes the appropriate adjustments.

On the level

Modular programming is handled by the Call Module (CALLM) and the Return From Module (RTM) instructions. These furnish a method of subdividing the user mode of operation into 256 access levels and of defining a protocol so that it allows for transition between levels. Two varieties of the instructions are used: one is for simple calls, which do not involve changes in access levels. The other is for complex module calls, which necessitate changes in levels.

Using the CHK2 and CMP2 instructions, it is possible to test whether a register is within its specified boundaries. If the value is out of

Table 2. New instructions

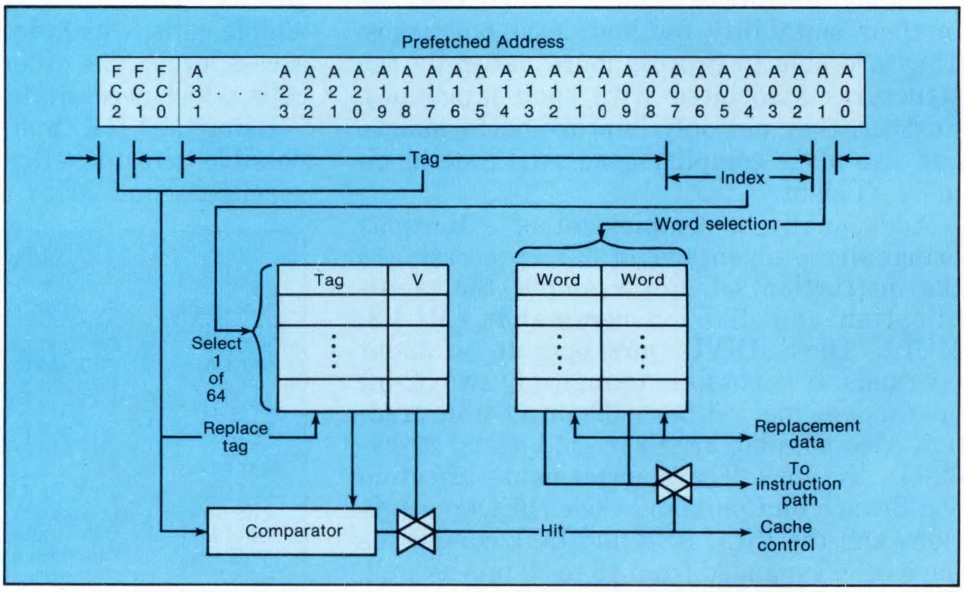
Mnemonic	Function
BFCHG	Bit Field Change
BFCLR	Bit Field Clear
BFEXTS	Bit Field Signed Extract
BFEXTU	Bit Field Unsigned Extract
BFFFO	Bit Field Find First 1 Set
BFINS	Bit Field Insert
BFSET	Bit Field Set
BFTST	Bit Field Test
BKPT	Breakpoint
CALLM	Call Module
CAS	Compare and Swap
CAS2	Compare and Swap (2 operands)
CHK2	Check Register against Bounds
CMP2	Check Register against Bounds
cpBCC	Coprocessor Branch on Coprocessor Condition
cpDBCC	Coprocessor Test Condition, Decrement, and Branch
cpGEN	Coprocessor General Function
cpRESTORE	Coprocessor Restore Internal State
cpSAVE	Coprocessor Save Internal State
cpSETcc	Coprocessor Set according to Coprocessor Condition
cpTRAPcc	Coprocessor Trap on Coprocessor Condition
PACK	Pack BCD
RTM	Return from Module
UNPK	Unpack BCD

bounds, CHK2 creates an exception condition and sets the necessary condition codes. The test is performed for either signed or unsigned bounds. What's more, the processor automatically evaluates the relationship between the two bounds to determine the appropriate comparison.

Other instructions have been added as well. Compare and Swap (CAS), for one, allows for locked-bus manipulation of more than one bit to support system queue and stack functions. Pack and Unpack (UNPK) translate easily between ASCII or EBCDIC and BCD data formats. Breakpoint (BKPT) gives system debugging a helping hand using the breakpoint-acknowledge mechanism. When the processor attempts to execute a breakpoint instruction, a breakpoint acknowledge cycle is executed. The proper op code is then fetched and substituted into the instruction pipeline in place of the breakpoint.

The coprocessor interface works with both concurrent and noncurrent coprocessors, as well as with bus master and bus slave coprocessors. Using it, a system designer can employ either a VLSI coprocessor to solve some of the more common processing problems—floating point computations, for example—or a discrete design dedicated to an important but limited task. Although the interface favors the 68020 in terms of performance, it may be used with other 68000 family members, treating coprocessors as peripherals. Since an interface cannot possibly be defined for every conceivable application, other mechanisms permit software emulation of undefined primitives. Thus if a function is not defined, it can be added later or be emulated by the user.

The interface contains its own instruction set, which comprises 10 commands that supplant the F-line exception mechanism used by earlier members of the family. That mechanism allowed the user to emulate special functions by setting a trap (take another path) to a



2. The processor's on-chip 256-byte cache for instruction stream accesses significantly reduces the number of fetches that must be made to the external memory. (V stands for validity bit.)

special emulation routine. In addition to the eight basic instructions, the processor can evaluate and handle 25 primitive types in order to define the activity requested by a particular coprocessor and to determine what is required to execute it.

Passing messages

Instructions from the 68020 are passed to a coprocessor for evaluation, thus freeing the main CPU from the task of defining a particular coprocessor instruction set. After evaluating the instruction, the coprocessor determines what services—if any—are required from the main processor to execute the instruction.

Service requests take the form of primitives sent to the main processor. These primitives are very powerful, which minimizes the overhead in both coprocessors. For example, the main processor can perform effective-address calculations and pass the evaluated address to the coprocessor, or it can fetch the variable-length operand. By providing this complex service, the 68020 allows the coprocessor design to be much simpler.

The processor has five types of coprocessor instructions: general, branch, conditional, save state, and restore state. The forementioned primitives include requests to transfer the main processor registers, the coprocessor registers, the top of the stack, or the instruction stream. They also, among other things, calculate effective addresses and transfer addresses. Further, transfers are performed bidirectionally.

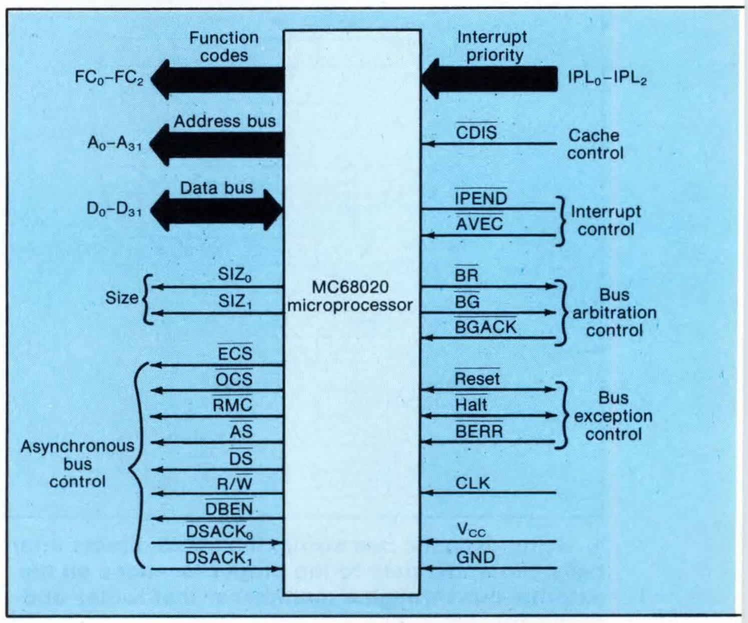
Speeding information flow

An instruction cache memory can be a fraction of the size of main memory yet ensure a significant decrease in the average access time. The 68020 takes advantage of this approach, which has been used for many years in mainframe computers. The chip's 256-byte instruction cache improves performance in two ways: First, far fewer fetches must be made to the external memory. Second, the consequent reduced use of the bus affords greater bus bandwidth for other bus masters, such as a DMA controller. Only instructions are stored in the cache to avoid the problems associated with stale data and other cache-related difficulties.

The on-chip cache links with the processor's data paths to allow complete overlap with data-operand accesses (Fig. 2). Also, the cache control register permits the operating system to maintain and optimize the cache.

The Enable bit of the cache control register controls the 68020's use of the cache: when set, the cache is enabled; when clear, the cache is disabled and the processor fetches from the external memory. Writing a 1 to the Clear bit clears all valid bits in the cache, thus forcing the 68020 to refill it with new data. When the Freeze bit is set, the 68020 cannot replace the data in the cache. The Clear Entry bit works in conjunction with an address in the cache address register, clearing the location in the cache that corresponds to the address in that register.

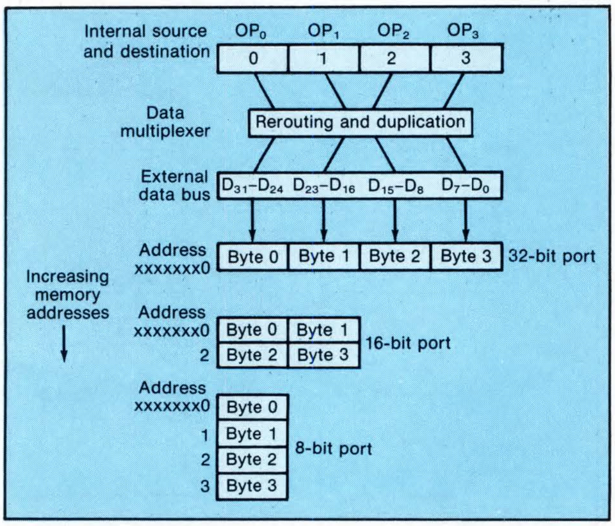
The 68020 maintains the fast and easy to use



3. The microprocessor's bus interface employs dynamic bus sizing. Using this novel technique, the processor can size the bus port and handle data from 8-, 16-, and 32-bit ports. Full 32-bit capability is supplied on the address and data bus interfaces.

nonmultiplexed asynchronous bus interface found on earlier members of the 68000 family. However, the interface sports several new features (Fig. 3). It consists of full 32-bit nonmultiplexed address and data buses, sequence control lines, as well as miscellaneous lines for interrupt and arbitration control. Taken together, the improvements guarantee a bus cycle time of 180 ns at 16.67 MHz, with an address-valid to data-valid requirement of only 115 ns.

One of the interfaces most important additions, dynamic bus sizing, allows the 68020 to measure the bus port and transfer data to and from 8-, 16- and 32-bit ports. Here, the microprocessor uses the data multiplexer and the Data Size and Acknowledge (DSACK) input to dynamically link to various-sized buses on a cycle by cycle basis (Fig. 4). Such a scheme allows the software to ignore the hardware configuration of a memory and of the I/O ports and instead to view the address space as a continuous block. In addition to dynamic sizing, the device has no restrictions on placing operand bytes. That is, data operand can appear on odd-byte boundaries, and the processor correctly fetches and stores them.



4. Using dynamic bus sizing, the 68020 directs internally generated data to the proper locations on the external bus through a multiplexer that routes and duplicates the data.

Towards higher performance

Another way the 68020 boosts performance over earlier family members is through its higher clock frequency. Both the 68000 and 68010 operate over the range of 8 to 12.5 MHz; the 68020 runs at the specified 16.67-MHz frequency. In addition, future versions will likely operate at a frequency of 25 MHz. Although doubling the clock frequency improves performance, the improvement is not twofold, since other factors such as memory access time must be considered.

Yet another technique for increasing system throughput is to increase the width of the data bus from 16 to 32 bits. A 16-bit processor generally fetches long-word operands using two 16-bit fetches. A 32-bit processor needs only one 32-bit fetch, thus reducing the number of bus cycles necessary to execute longer operations. Instruction accesses benefit the most from a wider bus, since the instruction stream is more sequential than in a 16-bit architecture.

Although a microprocessor can operate at very high speeds internally, it frequently must slow down to communicate with the outside world. The 68020, however, minimizes the delays involved in executing bus cycles. The processor's bus cycle time requires three, rather than four, clock cycles, and the number of bus cycles executed is further reduced by the instruction cache.

Staying ahead of schedule

The instruction cache reduces execution time in two ways. First, and most important, instruction and data accesses are handled simultaneously—that is, data and instruction addresses are calculated in parallel and have separate paths to the address inputs. That ensures concurrent instruction and data accesses if there is a hit in the cache while a data access is taking place. Separate buses for instructions and data also permits pipelined accesses within

the cache. Second, the time needed to access the cache is kept to two clock cycles, the same as the micro-instruction time.

Because of the sequential nature of instruction access, it is possible to anticipate what the next access to the cache will be and to make that access before it is actually needed. Thus there is no penalty incurred if the cache access should miss. In fact, the instruction address is sitting at the pins, ready to initiate a bus cycle depending on whether there is a hit or a miss in the cache.

The 68020 uses a highly pipelined architecture. The principal pipeline is the one for instructions, and there are several others used to control various units within the processor. The instruction pipeline is three words deep. The advantage of a deep pipeline is that it creates an apparent reduction in the time needed to decode an instruction and the time required to supply the necessary control for execution (Fig. 5).

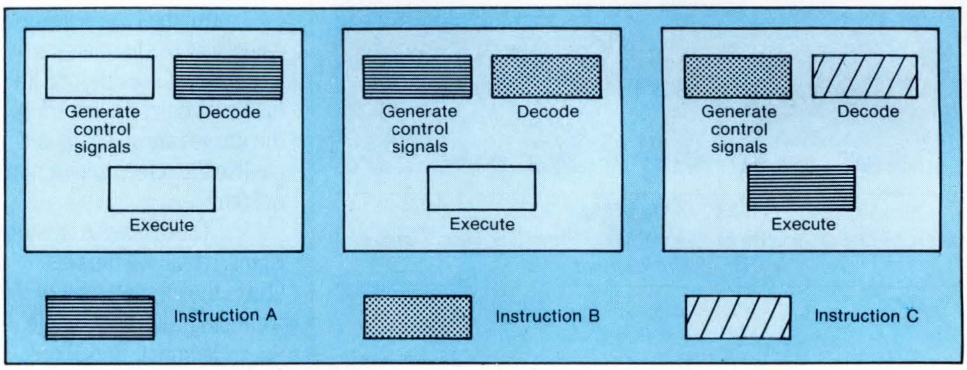
The depth of the pipeline makes it always possible to fetch three words in two memory accesses on a 32-bit bus. Two is the minimum number of accesses, since two words cannot be fetched in one cycle more than half the time.

Assume that the instruction stream A, B, C, D, and E is stored in memory in either an even- or odd-aligned fashion. In the even-aligned case, a branch permits the first two instructions (A and B) to be fetched on a single access. In the odd-aligned case, though, a branch permits only the first instruction (A) to be fetched on a single access. In either case, two accesses are required to fetch the first three instructions (A, B, C) and to fill the pipeline.

Cooperation speeds execution

Parallelism, or the concurrent execution of several tasks, is used extensively in the 68020. In fact, the microprocessor's execution unit is partitioned into an instruction-address section, an operand-address section, and a data section —each of which contains a 32-bit adder. The instruction address portion both calculates instruction addresses and stores pointers. The operand address section, as its name implies, calculates operands. Finally, the data section is the site of all data operations.

Although the sections are optimized to perform their primary roles, when necessary each can function as a general-purpose computation unit. Further, every section is connected to its neighbor by a high-speed bus. For example, a 32-by-32-bit multiplication that produces a 64-bit product uses both the operand-address



5. In a three-instruction pipeline, the flow of instructions is continuous when the pipe is full. As the first instruction (A) is executed, the second (B) obtains its control signals, and the third (C) is decoded.

and the data section to carry out that task. The use parallelism can also be seen in the simultaneous accessing of data and instructions.

Parallelism also exists between the processor and the bus controller. Consider, for example, that an instruction has been executed and the results must be written to memory. Under such a condition, there is no reason why the processor cannot proceed with the execution of the next instruction, which is exactly what happens. Thus the device's ability to perform simultaneous accesses of instruction and data is made even more significant.

The number of instructions that can be overlapped depends on the length of the bus cycle and the demands of the overlapped instructions to use the bus. That capability is important in high-performance processors because of the great likelihood of their working with high-speed data caches. With such a cache, writing requires longer cycles because of write-through problems. The longer cycles, in turn, make overlapping more probable; hence the value of a processor that handles such instructions can be clearly seen.

if piecount[class[i]] <> 0 then

Compiled 68000 code (13 bytes)

68000 cycles Clock	68000 cycles Bus	68020 cycles Clock	68020 cycles Bus		
4	1	2	0	move.w	d1,d3
8	1	4	0	lsl.w	#1,d3
12	2	6	0	lea	db_register(db,d3.w),a2
12	3	7	1	move.w	~class(a2),d3
8	1	4	0	lsl.w	#1,d3
12	2	6	0	lea	db_register(db,d3.w),a2
12	3	7	1	tst.w	~piececount(a2)
11	2	6	0	beq	else
79	15	42	2		

Compiled 68020 code (8 bytes)

68020 cycles Clock	68020 cycles Bus		
9	1	move.w	(~class,a5,d1.w*2),d3
9	1	tst.w	(~piececount,a5,d3,w*2)
6	0	beq	else
24	2		

d1=i	a2=temporary pointer	db_register=0
d3=temporary	a5=base	~class=$1c26
		~piececount=$1c40

6. A high-level language statement—actually a doubly indexed conditional test in Pascal—shows how much more efficient 68020 code is than 68000 code. The enhanced instruction set permits three 68000 instructions to be condensed into a single 68020 command.

Condensing instructions

The number of extensions made to the 68020's instruction set improves the microprocessor's ability to work with high-level languages. The most significant ones concern the addressing modes. As noted earlier, the full index addressing mode make it possible to scale the indexes, include memory indirection, generate 16- and 32-bit displacements, employ pre-indexing or postindexing with memory indirection, and suppress any element of the address (use the data register for an address). Thus the two weaknesses of the 68000's addressing modes are rectified: the inability to scale index values during a calculation and the lack of 16- and 32-bit displacements in the index addressing mode.

The effect of the extensions can be illustrated by a Pascal program (Fig. 6), but the results would be the same for any high-level language that employs subscripts. Using the 68000-compiled code, the 68020 needs just 42 clock cycles and 2 bus cycles to execute the program—compared with the 68000's 79 clock cycles and 15 bus cycles. Further, the enhanced addressing modes of the 68020 reduces the number of clock cycles to 24, since it is possible to replace three or more instructions with one.

Because of the 68020's scaling adds no time to the calculation of effective addresses, code executes much faster. Actually, the 68000 executes the aforementioned Pascal program in 9.875 μs; the 68020 (running 68000 code) needs 2.625 μs; and the 68020 (running 68020 code) takes just 1.5 μs. Note that a 68020 executing its own code is almost seven times faster than a 68000 executing 68000-compiled code.

The other additions to the instruction set fall into two categories: the extension of the operand and the displacement size to 32 bits and the addition of complex instructions. The enhanced operand and displacement size does not affect many instructions, since most already handle 8-, 16-, and 32-bit operands. The added instruc-

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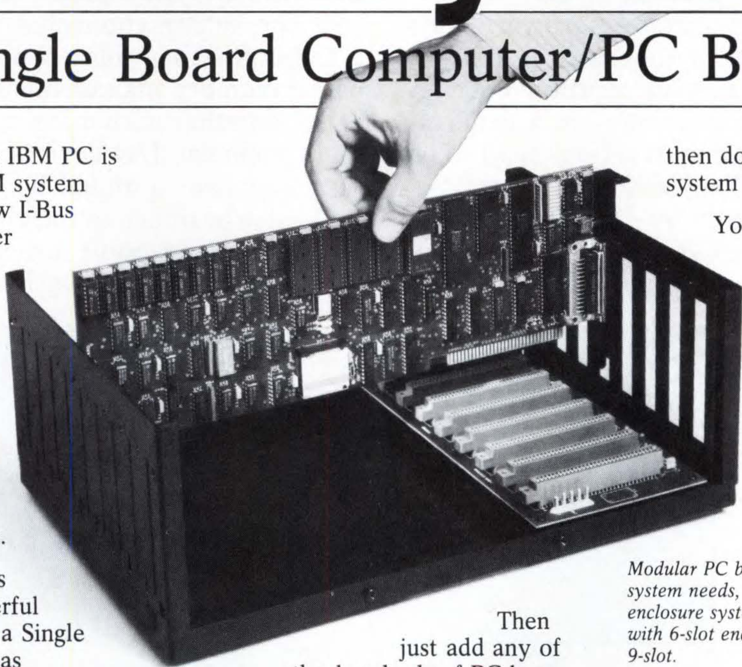

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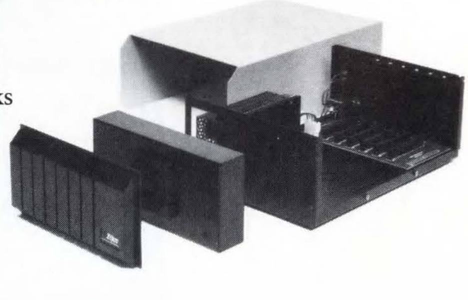

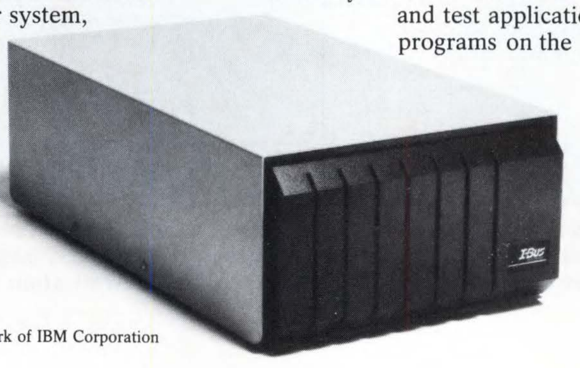

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tions improve performance primarily in special applications. Bit-field instructions, for example, are of the greatest significance in graphics and communications applications, even though they may be widely used in other settings.

A team player

Although the coprocessor interface itself does not improve performance, it supplies the mechanism for adding special-purpose units to handle unusual problems. The 68881 floating-point processor, for example, when combined with the 68020, forms a powerful team to execute floating-point programs.

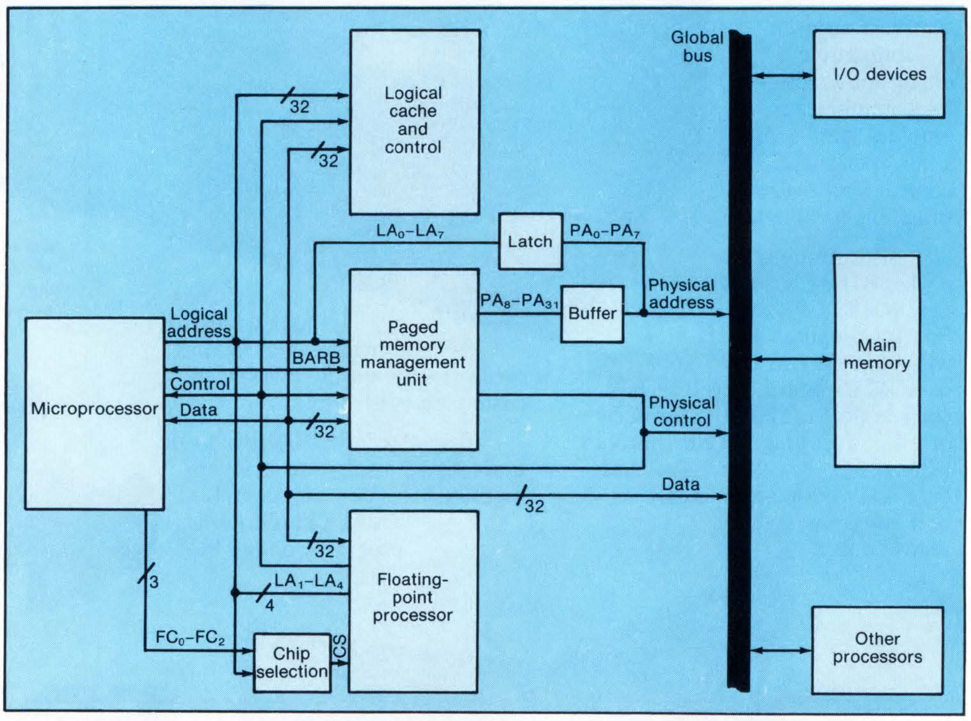
In addition, special-purpose hardware adds computational power to the basic processor. That in turn ensures faster execution of atypical but important instructions—in a general-purpose machine those instructions tend to be highly algorithmic. The 68020's barrel shifter, for instance, can handle bit-field instructions and can be used with a variety of other instructions as well. Additionally, special control circuitry permits two bits to be multiplied by every microinstruction.

The result of all these efforts is a high-speed processor with faster bus and a reduced number of bus cycles. The average number of clock cycles required to execute an instruction, for instance, has dropped from 13.5 to about 7, even though the clocks run at at least twice the frequency of the 68000's and the instructions that are carried out are much more complex.

Building on the basics

A 68020-based system can be designed by making use of the coprocessor interface (Fig. 7). In it, the 68020 is connected over a logical bus to a 68881 floating-point processor and a 68851 paged memory management unit. These three chips, together with a logical cache, connect to main memory, I/O devices, and other system resources over a global bus. Other processors could also be linked to the global bus.

The floating-point processor, which furnishes an extensive floating-point instruction



7. A high-performance 68020-based system relies on the coprocessor interface. Here, the 68020 uses a 68881 floating-point processor and a 68581 paged memory management unit as coprocessors. (BARB stands for Bus Arbitration control signal.)

32-bit microprocessor

set, fully complies with the IEEE floating-point standard and is accessed using the logical address bus. Once the floating-point instruction and any operands are transmitted to or from it, it can run concurrently with both the main processor and any other floating-point units in the system.

The memory management unit translates and generates memory control signals for the main processor and for any other bus master in the system. The unit translates logical addresses to physical ones and checks that access rights have not been violated. Also, it creates a demand-paged virtual memory for the CPU by determining if a page resides in physical memory and taking the appropriate action if it does not. The memory management unit can even function as a coprocessor when the descriptor tables must be maintained. In that case, it becomes a bus master and thus is able to perform any activities associated with such maintenance.

As a processor's clock frequency increases, the memory access times necessary to ensure access with no wait states decreases. Thus an external logical cache is an attractive addition to the system. Since the cache is logical, it can avoid the translation delay that would cause at least one wait state. Furthermore, since a cache is a local copy of data that is held in high-speed RAM, it does not have to waste time waiting for the global bus to be free. In fact, for a system with a 16-MHz clock, it is nearly impossible to design a main memory that can perform accesses without wait states.

The set of chips—the 68020 and its associated support chips—form one kind of processing unit. Clearly, any one of the peripheral could be either deleted or supplemented, the size of the cache could be varied, and a DMA controller could be added to either the physical or logical bus (or both). Further, an instruction cache could be added, as well as a data cache. However the processing unit is configured, the global bus ensures access to all resources in the system.□

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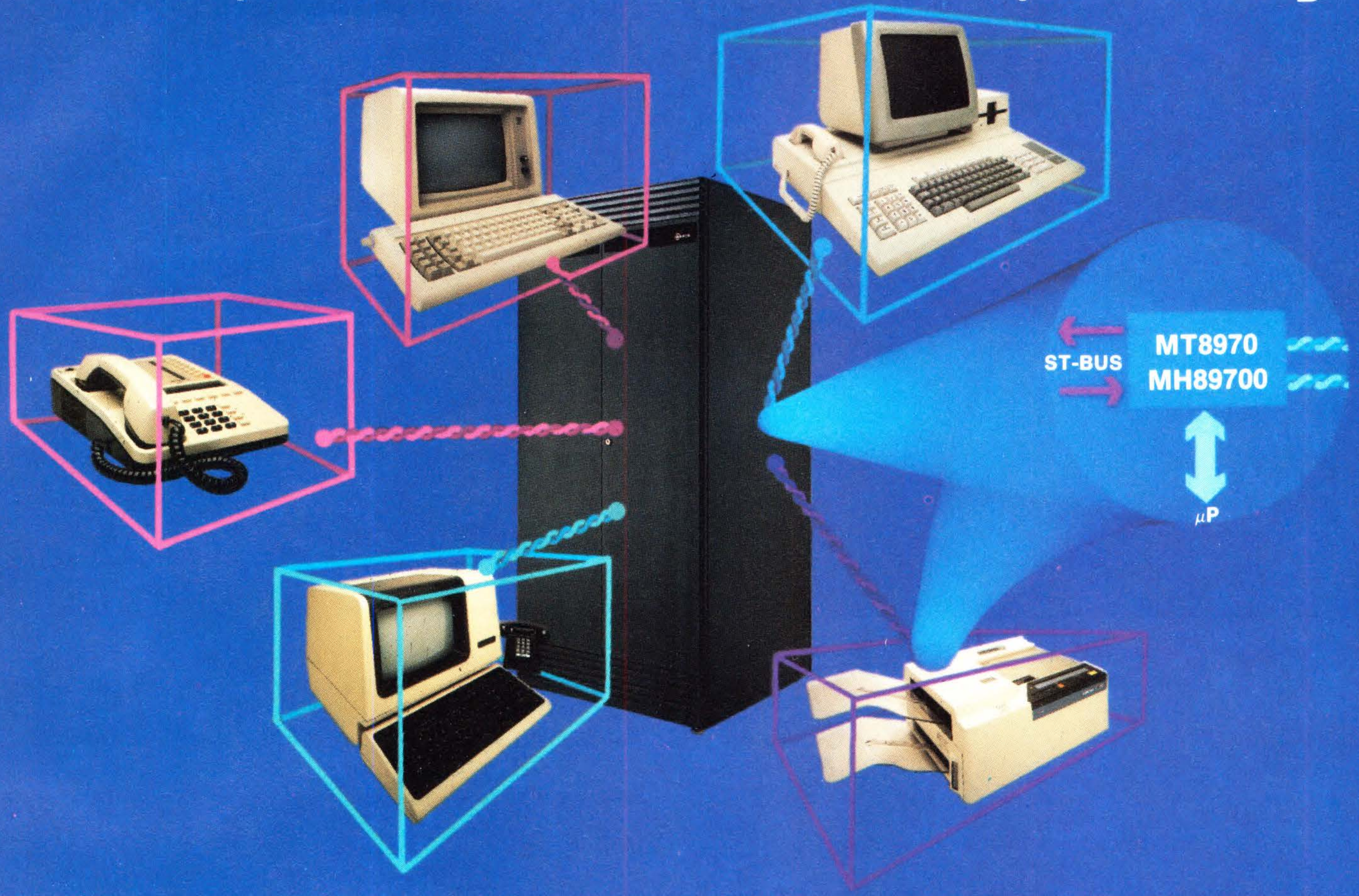

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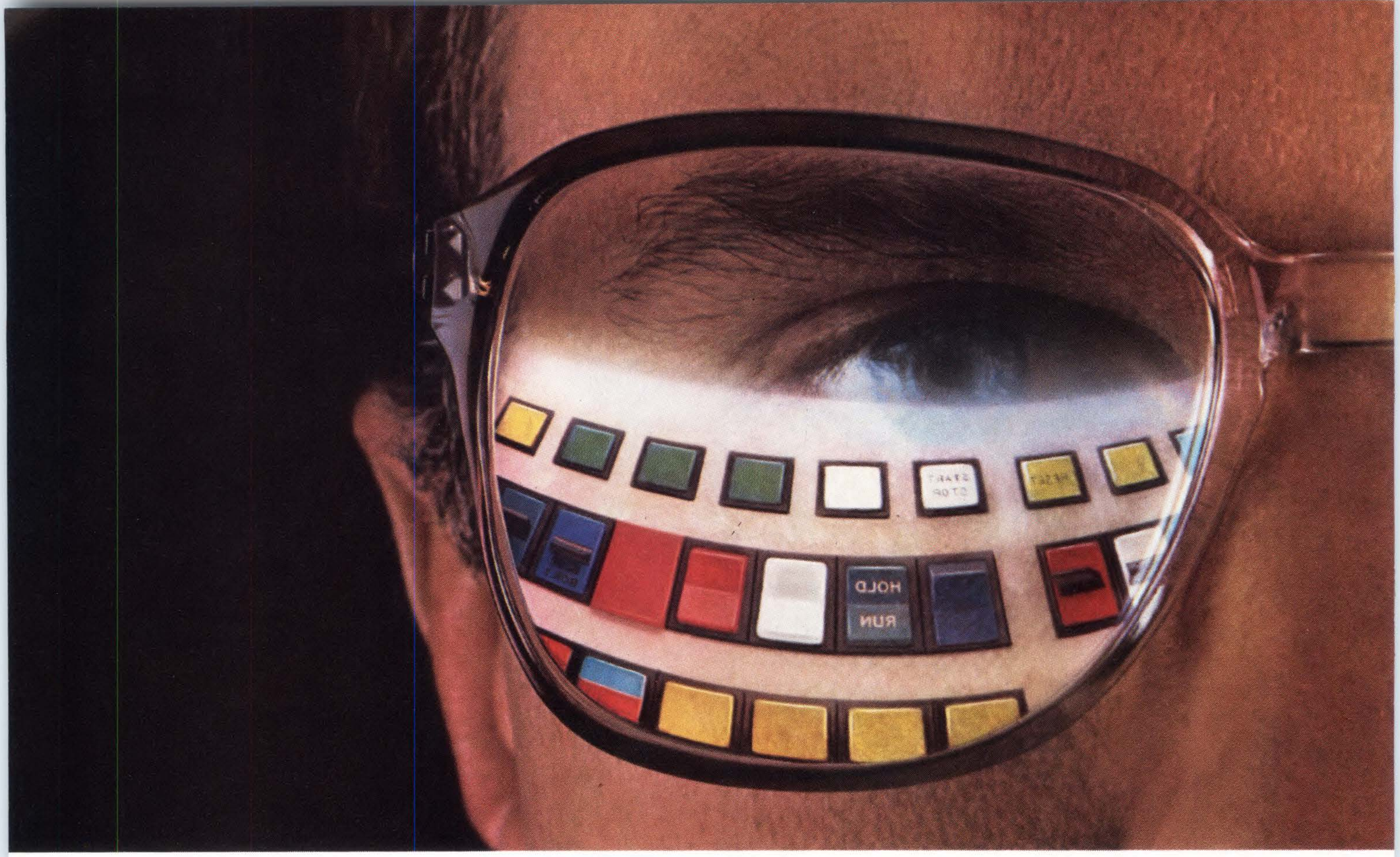

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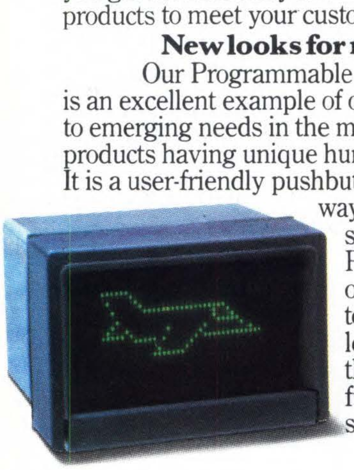

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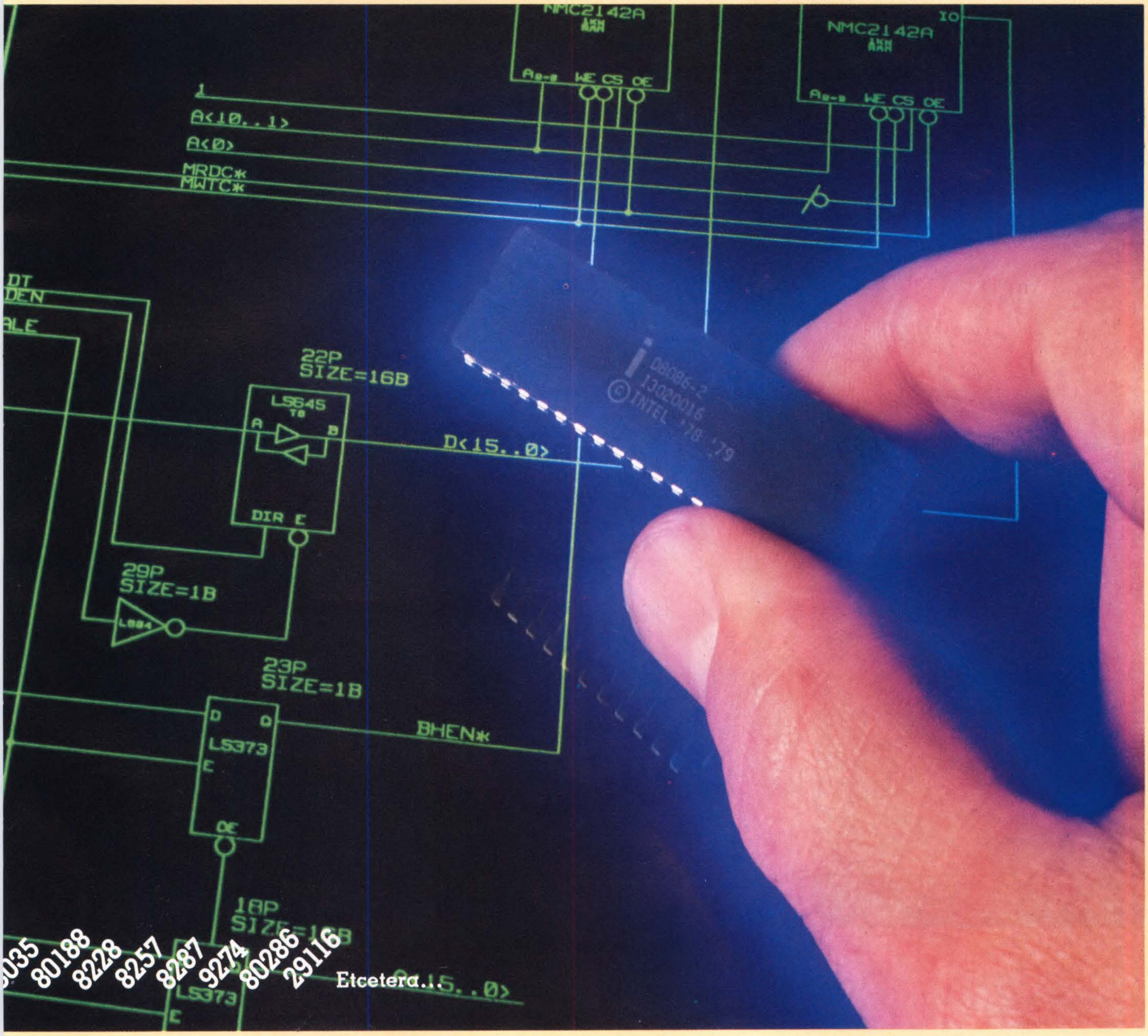

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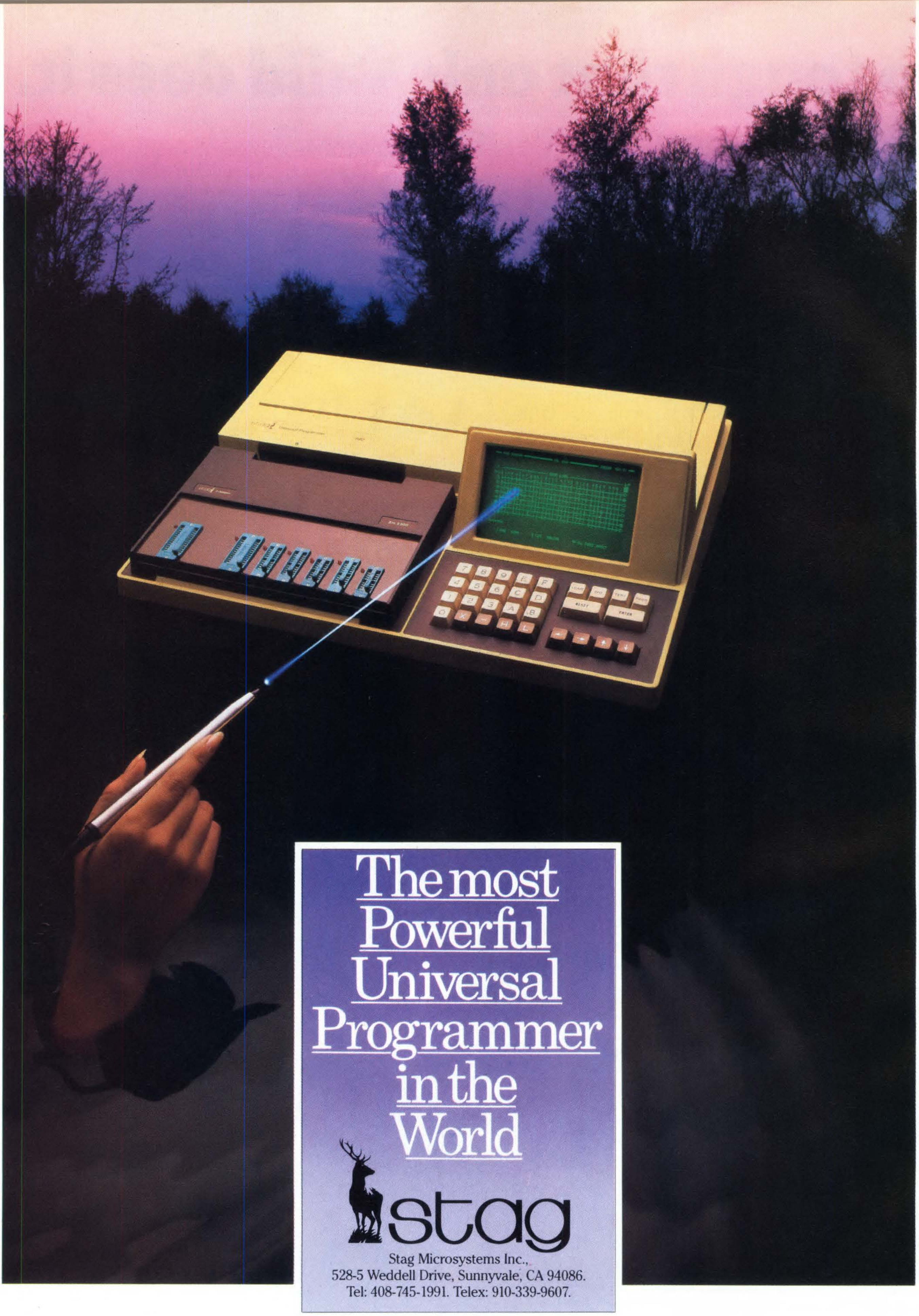
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CIRCLE 112

Precision op-amp rectifier eliminates diodes for economy, simplicity

Hal Wittlinger
Section Manager
IC Applications Engineering
RCA Corp.
Solid State Division
Route 202
Somerville, N.J. 08876

A circuit that uses the ground-referenced input and output of a 3130 operational amplifier creates a precision rectifier that, unlike conventional active full-wave rectifiers, does not need diodes and is therefore less expensive and simpler.

The absolute-value circuit (see the figure) produces a positive output regardless of the polarity of the input signal and is useful in a variety of applications, from measurement to gain control. Also, full-wave rectification is important when the ripple component of a signal must be kept at the highest possible frequency to ease filtering requirements.

Essentially, the circuit operates as a conventional op amp for negative-going input signals and as a resistive attenuator for positive-going ones. The gain for a negative-going signal is determined by:

$$G = |\text{Gain}| = G_{neg} = \frac{R_2}{R_1}$$

Alternatively, when the signal goes positive, the attenuation supplied by the three resistors (R_1, R_2, and R_3) is found by:

$$G = G_{pos} = \frac{R_3}{R_1+R_2+R_3}$$

In both cases, the gain should be set to produce a symmetrical waveform for the pulsating dc output. Further, the driving-source resistance must either be kept at a low value with respect to R_1 or be factored into the resistor's value.

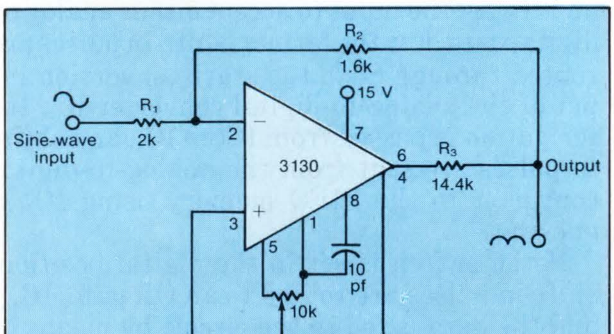
On the other side of the circuit, the value of R_3 is found with the formula:

$$R_3 = \frac{G(R_1+R_2)}{1-G}$$

If the circuit must drive a relatively low impedance, one less than 100 times R_3, that resistor can be considered part of the load and its value calculated as if it were in parallel with the load.

For example, if the load is 51 kΩ with respect to ground, R_3 must be 20 kΩ to develop the 14.4-kΩ value shown. The foregoing assumes that the op amp's output resistance is negligible with respect to the value of R_3.

Care should be taken to limit the input signal amplitude so that the voltage at pin 2 of the op amp does not exceed +7 V. If that is not done, greater voltages will be clipped during the positive input peaks, distorting the output.



A diodeless precision rectifier acts as an attenuator for positive inputs and as a conventional op amp for negative signals. For a 1-V rms input and the resistor values shown, the circuit gain is 0.8. Its frequency response is −1% at 60 kHz and −1 dB at 300 kHz.

FIFO memory circuit stores waveform data for monitors and scopes

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Senior Electronics Engineer
F.C. Delori
Senior Scientist
Eye Research Institute
20 Staniford St.
Boston, Mass. 02114

Wiring a FIFO memory as a ring buffer supplies excellent storage for a continuous waveform display circuit. Using the buffer, any digital or analog source can be held and repeatedly displayed on inexpensive monitors or standard laboratory oscilloscopes. Not only does the circuit free a microcomputer from the repetitive chore of servicing a display, it is flexible enough to accommodate words of any length and width.

The switch, S_1, and three-state buffers IC_1 and IC_2 set the input to accept either analog or digital data. For the former, shift-in pulses are routed through S_1 to the start-conversion input of the analog-to-digital converter IC_5. Information is passed from IC_5 to IC_2, and shift-in pulses are sent from the analog-to-digital converter to the FIFO memory using IC_8, a one-shot.

If the switch is set to the digital position, shift-in pulses are routed to an OR gate, IC_{9A}, and the data is fed to the circuit by means of IC_1. Moreover, if the analog input is not needed, IC_1, IC_2, and IC_5, as well as the switch, can be eliminated, reducing the chip count and lowering the circuit's cost.

Once the input has been selected, the FIFO is loaded by applying a logic high to the memory's Load input. Doing so clears the FIFO, stops the X and Z axis output circuitry, and gates buffer IC_3 on the buffer IC_4 off. Next, $N-1$ shift-in pulses are applied synchronously with the data, where N is the word length of the FIFO. Data enters the memory through IC_3 and, when the FIFO contains $N-1$ bytes of data, the memory's Output Ready pin drops low to signal that the FIFO is loaded.

Once that is done, the Load input is brought low, turning IC_3 off and IC_4 on and enabling the clock gate IC_{10A}. At this point, the source of the waveform can return to other tasks, since the circuit has stored the necessary data for display.

The clock gate drives the ramp generator, which comprises counters IC_{11}, IC_{12}, IC_6, and the FIFO, thus synchronizing the X and Y outputs. Its leading and trailing edges also generate the shift-in and shift-out pulses, respectively, with the help of one-shots IC_8 and IC_{13}.

Because $N-1$ bytes have been loaded, the FIFO's last byte space is empty and ready to accept data from the output of the memory. The display cycle itself begins with a shift-in pulse that causes the data to move out of the FIFO and into the digital-to-analog converter IC_7. Concurrently, the same data is moved back into the FIFO using IC_4. This process of shifting in and shifting out continues until the time-base counters reach $N-1$. At that point, the FIFO data has come full circle; that is, the first byte of data at the output of the FIFO is again first at the output. Simultaneously, the clock and Z drives are stopped for 1 μs to reset the ramp.

The foregoing cycle is repeated over and over, causing the waveform to be repeatedly displayed on the monitor, through IC_7, independently of the input signal source. If necessary, though, that source can interrupt the

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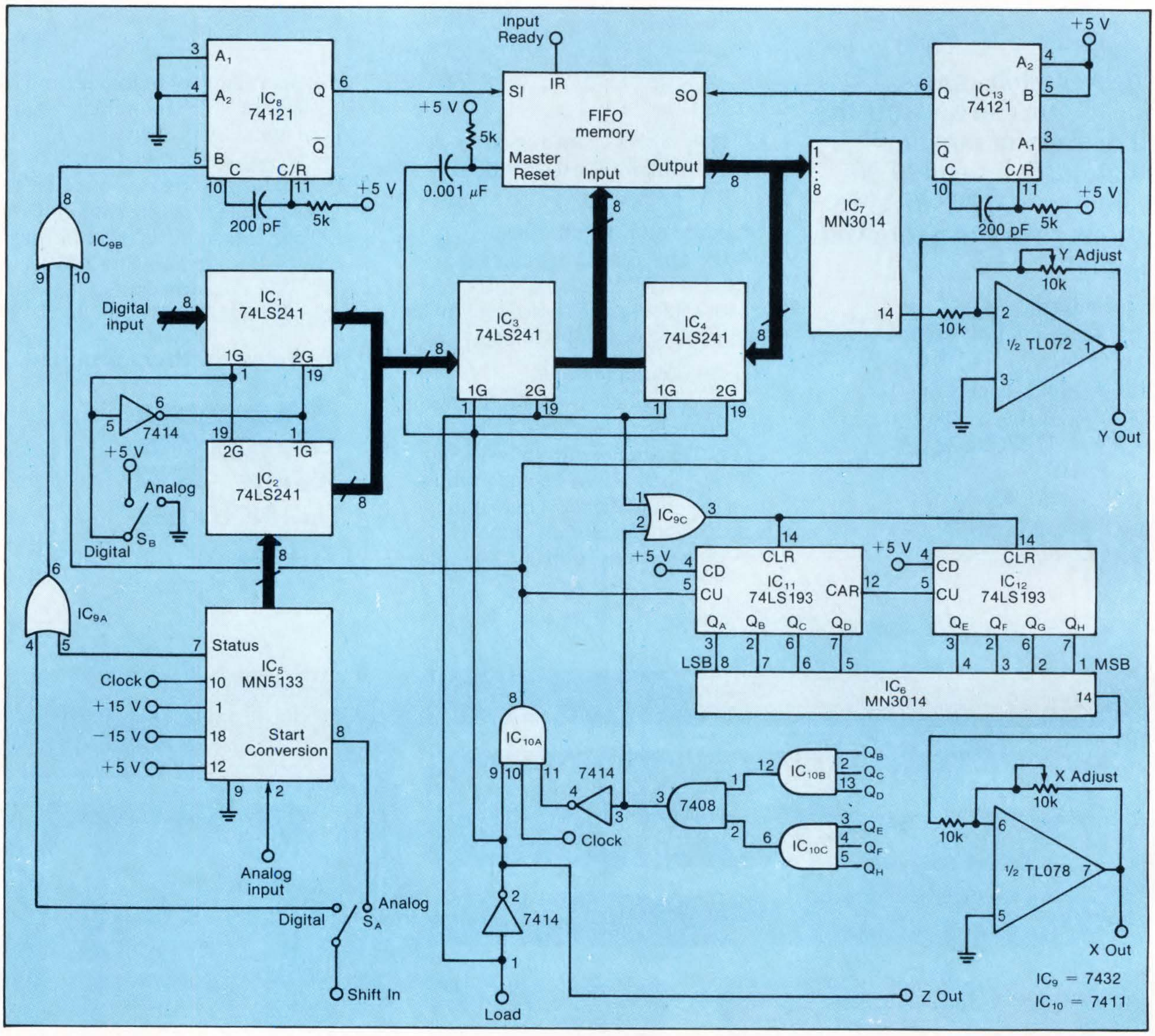
CIRCLE 114

circuit at any time to load new waveform data.

The circuit has worked well in helping to analyze waveforms that have been signal-averaged by a microcomputer. Because of the FIFO's 2-MHz data rate, automatic data-propagation characteristics, and asynchronous shift-in, shift-out operation, waveforms can be transformed and stored very quickly. The FIFO, however, must be selected with care, since some allow just (A−1) × N word lengths when stacked, where A is the FIFO's word length and N is the number of stacked FIFOs. Also, it should be remembered that data rates vary from part to part.



A ring buffer circuit, using a FIFO memory for storage, captures and repeatedly displays a waveform on an inexpensive monitor or oscilloscope. Either digital or analog signals are handled with just the flip of a switch.

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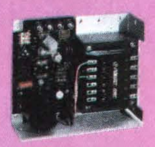

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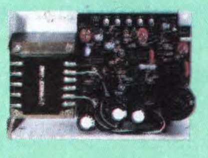

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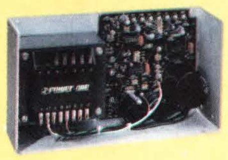

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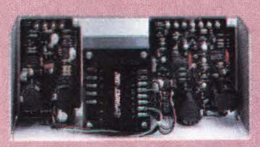

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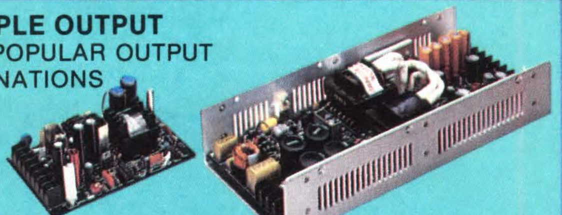

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CIRCLE 115

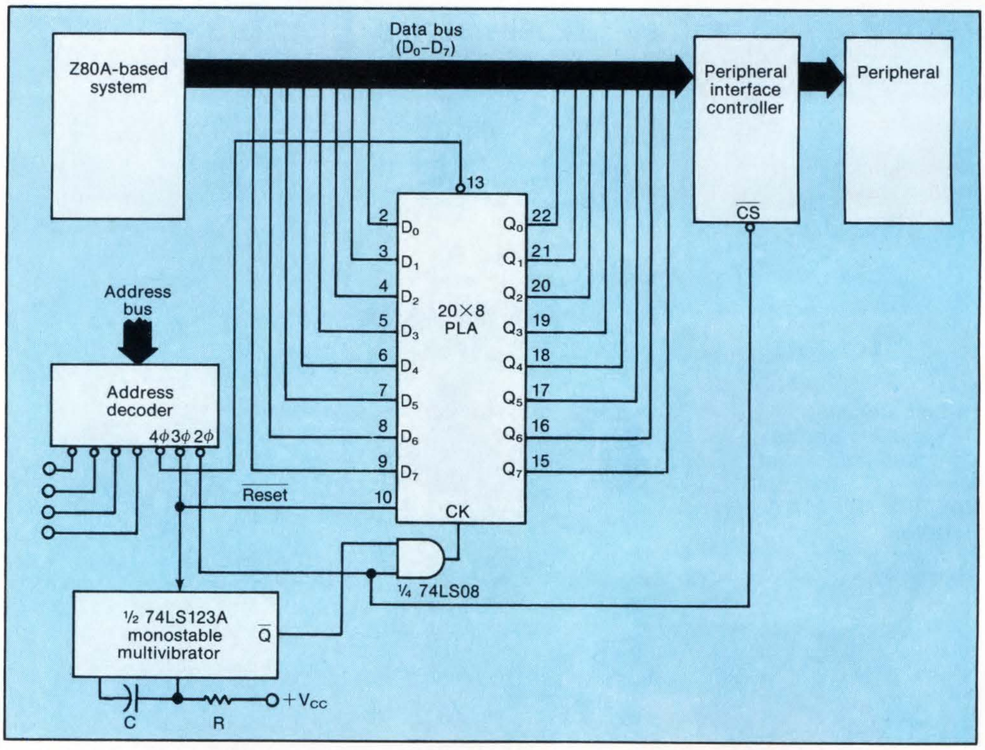
PLA shoulders processor's checksum chores for faster data transfer

Vittal Rao
Digital Systems Section
ISRO Satellite Centre
Airport Road, Vimanapura PO
Bangalore 560 017, India

Because a software approach hampers the transfer of data from a microprocessor system to a peripheral, such as a floppy-disk drive, the task of generating a checksum byte is more appropriately assigned to separate hardware. A single programmable logic array —say, a 20X8 (Fig. 1)—neatly combines the collection of gates, flip-flops, and other discrete

Subroutine to initiate checksum byte calculation

```
CHKSM:   OUT [30H],A   ;Reset the PLA.
DTBLK:                 ;Start the data transfer instruction.
                       ;
                       ;
                       ;
                       ;
                       ;
                       ;
                       ;End of the block.
         IN A, [40H]   ;Get the complemented checksum
                        from the PLA.
         CPL A         ;
         OUT [20H],A   ;Load the checksum byte into
                        the peripheral.
         END           ;
```



1. A programmable logic array contains all the hardware elements needed to compute the checksum bytes for a data transfer. With the system processor unburdened by that chore, the throughput rate improves considerably.

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*Patent Pending

NAME	PART NUMBER	SPEED
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Fanout Buffer	10G011	3 GHz
Comparator/ Driver	10G012	3 GHz
Precision D Flip Flop	10G021	3 GHz
2 Stage Divider	10G060	3 GHz
7 Stage Counter	10G065	3 GHz

NAME	PART NUMBER	SPEED
Variable Modulus Divider	10G070	2 GHz
7 Stage Divider	11G566	4 GHz
Diode Array	16G010	500 GHz
Diode Array	16G011	675 GHz
FET Array	16G020	15 GHz
Dual Gate FET Array	16G021	15 GHz
Evaluation Board	10GEVA	3 GHz

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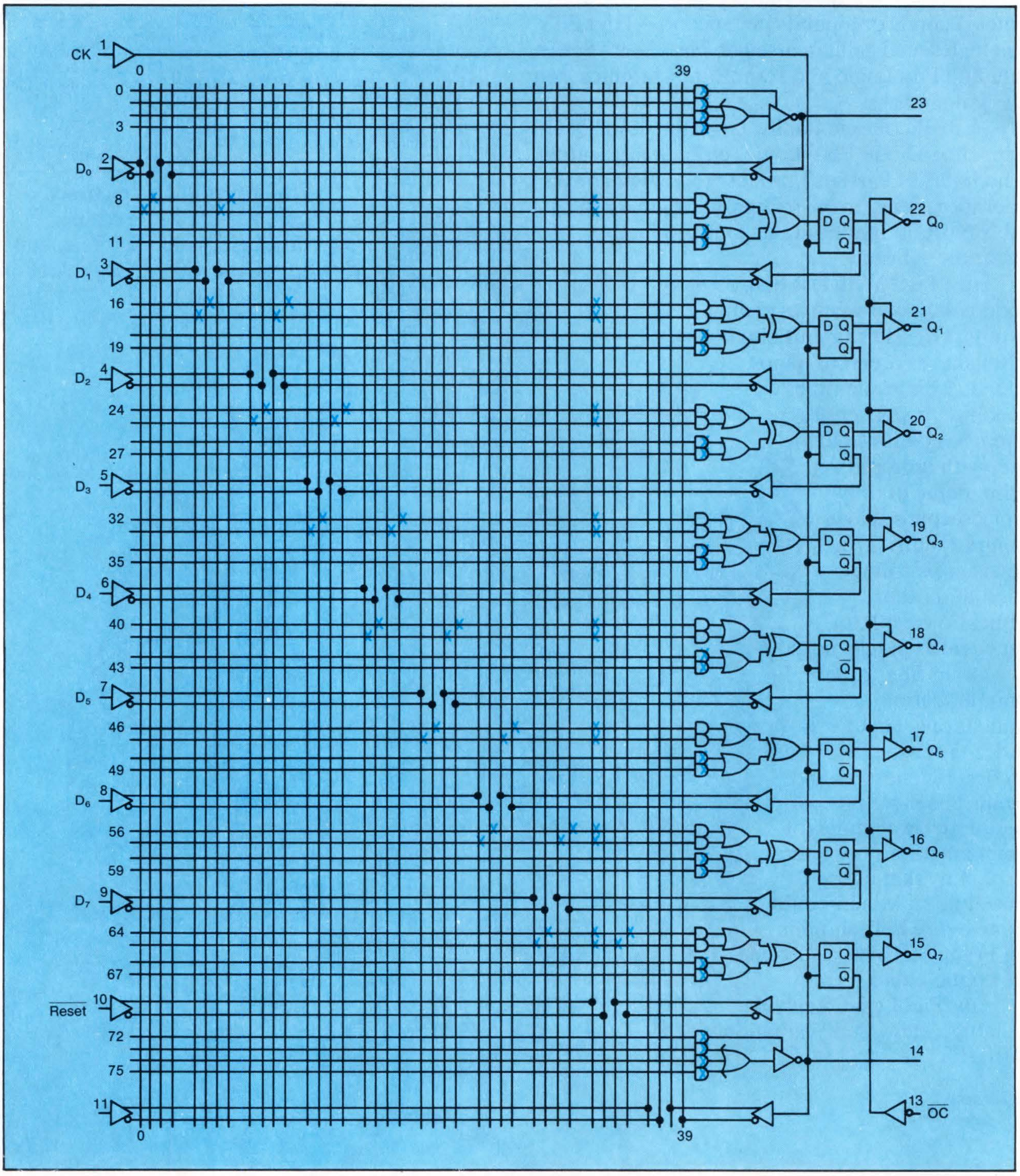
CIRCLE 116



2. A programming chart indicates the specific locations that must be left intact to configure the PLA with the appropriate logic elements for the checksum calculation.

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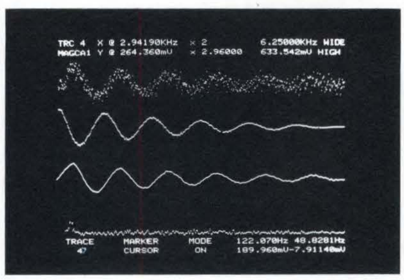

For system test applications the fully programmable Data 6000 can acquire waveforms, measure time domain waveforms with over 40 pre-programmed scalar measurements, compute and measure spectra, and transfer the resultant measurements or data points to your computer. In the above figure the Data 6000 performs summation averaging on a noisy signal, convolves the result with a user defined filter, and displays the FFT of the processed waveform on trace four.

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CIRCLE 118 FOR DEMONSTRATION

CIRCLE 119 FOR ADDITIONAL INFORMATION

parts used in conventional designs.

DMA control maximizes the transfer rate for blocks of data, but the need to generate a checksum byte taxes the microprocessor—in this example, a Z80—such that control is not possible. Transfer must take place through the CPU, which calls four- or five-instruction subroutines to calculate the checksum byte. Consequently more than 70% of the CPU's transfer time is spent calculating the checksum.

The checksum is a single byte, appended to the end of a data block, that includes sufficient information about the amount of data in the block for a receiving device to determine data integrity by. It is generated by storing the exclusive-OR output of the N^{th} and $N+1^{th}$ byte and then exclusive-ORing that result with the $N+2^{th}$ byte. The process continues for all the bytes of the data in the block. Finally, the checksum itself is accounted for as the last byte of the block.

The PLA moves the function from software to hardware. The fusing pattern (Fig. 2) configures the exclusive-OR logic, the associated flip-flops that serve as storage elements, as well as the proper feedback circuitry. A single instruction initializes the PLA, and several more instructions read the checksum from the logic array via the device's $\overline{OC}$ pin (see the program listing).

Winner for June 28, 1984

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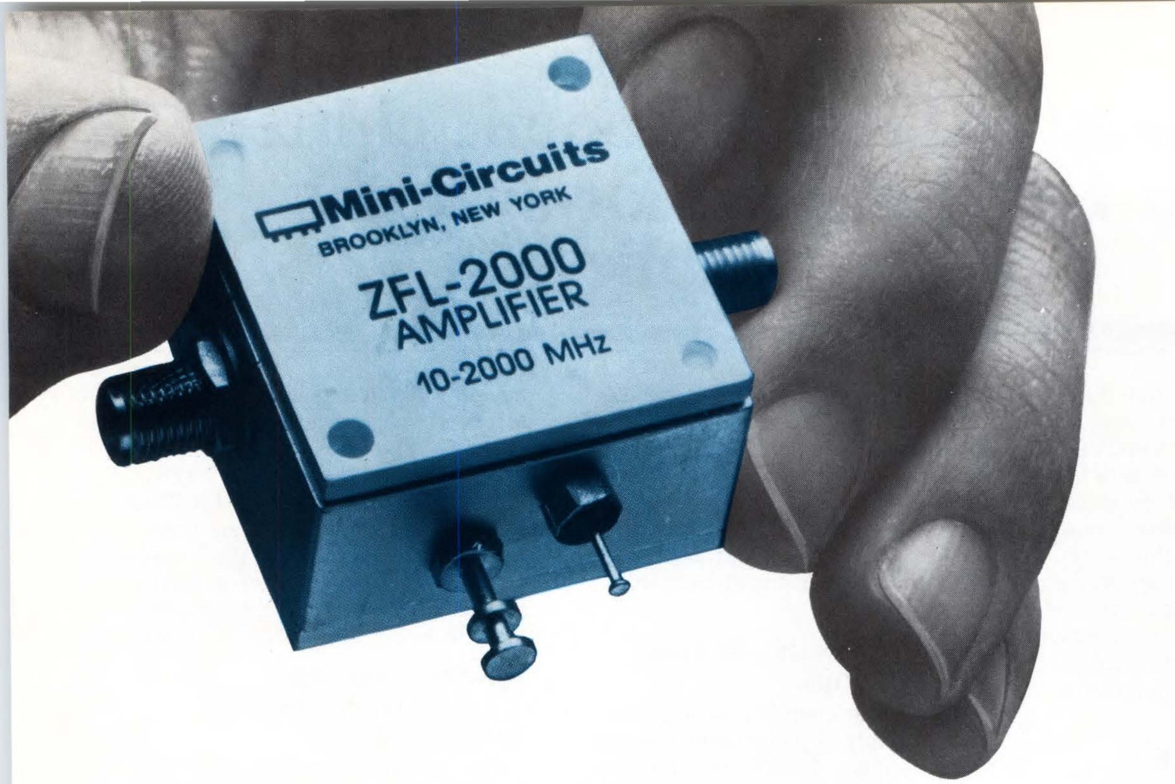

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For complete specifications and performance curves refer to the Goldbook, EEM, EBG, or Mini-Circuits catalog

ZFL-2000 SPECIFICATIONS

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GAIN	20 dB
GAIN FLATNESS	±1.5 dB
OUTPUT POWER (1 dB compression)	+17 dBm
NOISE FIGURE	7.0 dB
INTERCEPT POINT (3rd order)	25 dBm
VSWR, 50 OHMS	2:1
DC POWER volt, current	+15 V, 100 mA
HEAT SINK	Internal
OPERATING TEMP	−55°C to +100°C

CIRCLE 121

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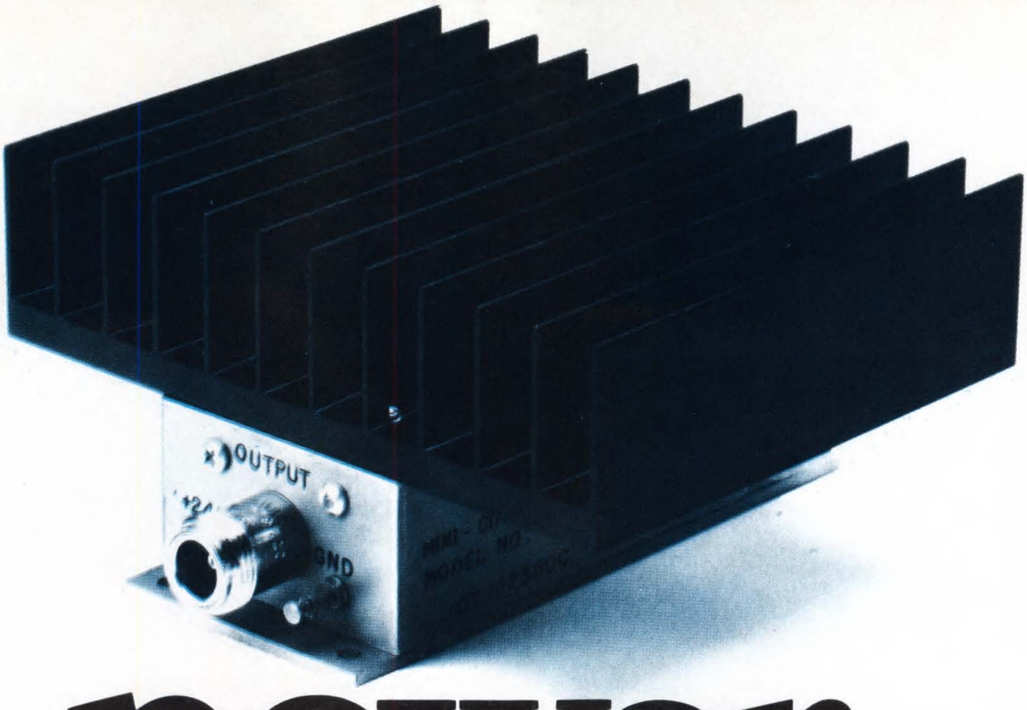

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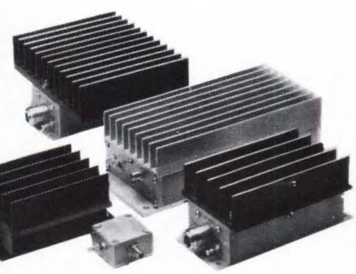

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ZHL-3A	0.4-150	24 Min.	±1.0 Max.	+29.5 dBm Min.	11 Typ.	+38 dBm	+24V	0.6A	199.00	(1-9)
ZHL-1A	2-500	16 Min.	±1.0 Max.	+28 dBm Min.	11 Typ.	+38 dBm	+24V	0.6A	199.00	(1-9)
ZHL-2	10-1000	15 Min.	±1.0 Max.	+29 dBm Min.	18 Typ.	+38 dBm	+24V	0.6A	349.00	(1-9)
ZHL-2-8	10-1000	27 Min.	±1.0 Max.	+29 dBm Min.	10 Typ.	+38 dBm	+24V	0.65A	474.00	(1-9)
ZHL-2-12	10-1200	24 Min.	±1.0 Max.	+29 dBm Min.	10 Typ.	+38 dBm	+24V	0.75A	599.00	(1-9)
ZHL-1-2W	5-500	29 Min.	±1.0 Max.	+33 dBm Min.	12 Typ.	+44 dBm	+24V	0.9A	495.00	(1-9)
ZHL-42	700-4200	30 Min.	±1.0 Max.	+29 dBm Min.	7.5 Typ.	+38 dBm	+15V	0.69A	895.00	(1-9)
ZHL-7-2W	600-800	28 Min.	±1.0 Max.	+33 dBm Min.	12 Typ.	+43 dBm	+24V	0.9A	525.00	(1-9)
ZFL-2000	10-2000	20 Min.	±1.5 Max.	+17 dBm Min.	7 Typ.	+30dBm	+15V	0.1A	179.00	(1-9)

50 ohm impedance,
input and output VSWR 2: 1 max.

Price and specifications subject to change without notice.

Refer to EEM and Gold Book for detailed specs.

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A Division of Scientific Components Corporation
World's largest manufacturer of Double Balanced Mixers
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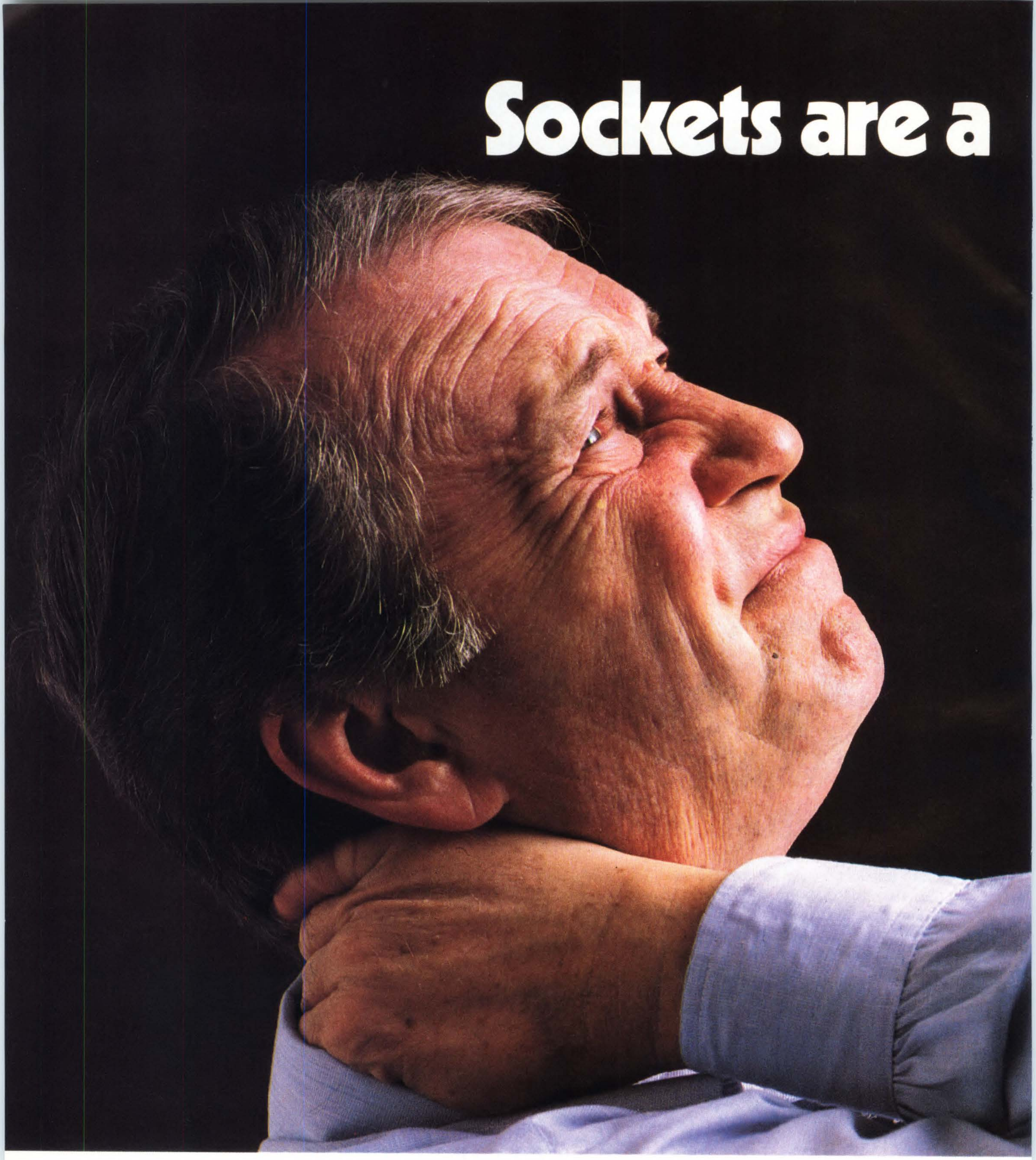
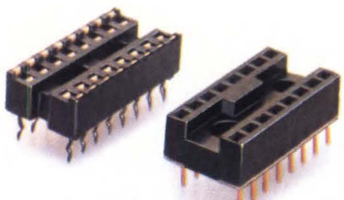
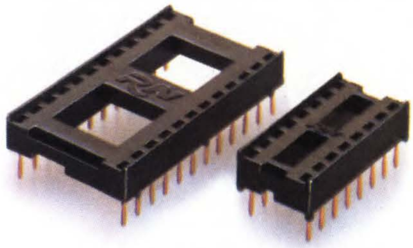
CIRCLE 122

C70 REV. B

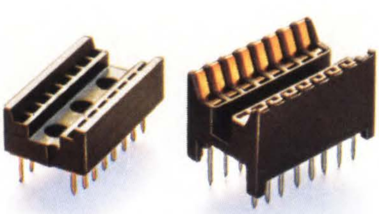




Production Sockets
Circle 211



Low Profile Sockets
Circle 212



Burn-in Sockets
Circle 213

pain-in-the-neck, right?

Wrong!

When you decide to eliminate board problems with sockets, be sure to specify the best you can get... RN Precision Screw Machine Sockets

Sockets, used selectively, can eliminate 4 of your toughest, everyday board problems!

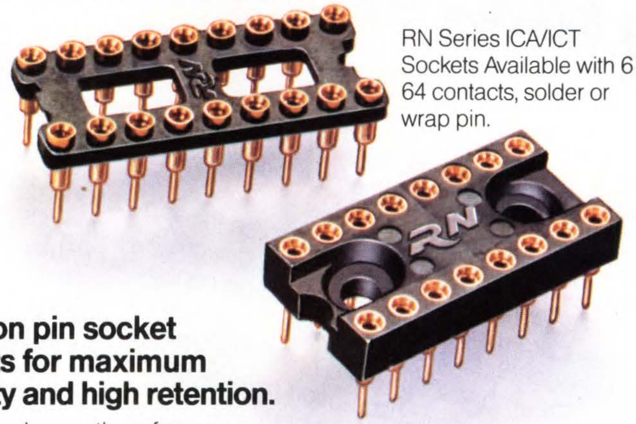
Take a fresh look at RN precision screw machine sockets. You may be surprised to see how many ways they can eliminate trouble, save real money and make you a hero to your boss:

1. Simplify board "trouble-shooting". Socket your sophisticated circuits so that you can remove and test them without desoldering. Excessive de-soldering heat can cause costly board de-lamination as well as circuit damage.

2. Slash field service costs. Simply unplug your circuits, test and replace in the field. No time-wasting de-soldering troubles.

3. Modify boards in the field. It is as easy as unplugging a circuit and inserting the new or re-programmed IC package.

4. Have peace of mind by socketing state-of-the-art devices that have not had MTBF standards established.

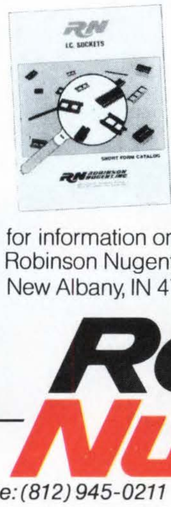


RN Series ICA/ICT Sockets Available with 6 to 64 contacts, solder or wrap pin.

Precision pin socket contacts for maximum reliability and high retention.

Technology innovations from RN include...

- Lowest profile in industry—.122"
- High temperature: 200°C
- Lowest insertion force—5 ounces, maximum
- .180" solder tail length available



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for information on the full line of RN sockets, contact:
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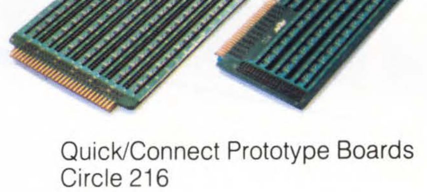
Flat Cable Connectors
Circle 214

DIN Connectors
Circle 215



Quick/Connect Prototype Boards
Circle 216

Aromat IC Relay— the smart choice for intelligent control and direct connection to microprocessor bus lines.

Aromat
Member of Matsushita Group

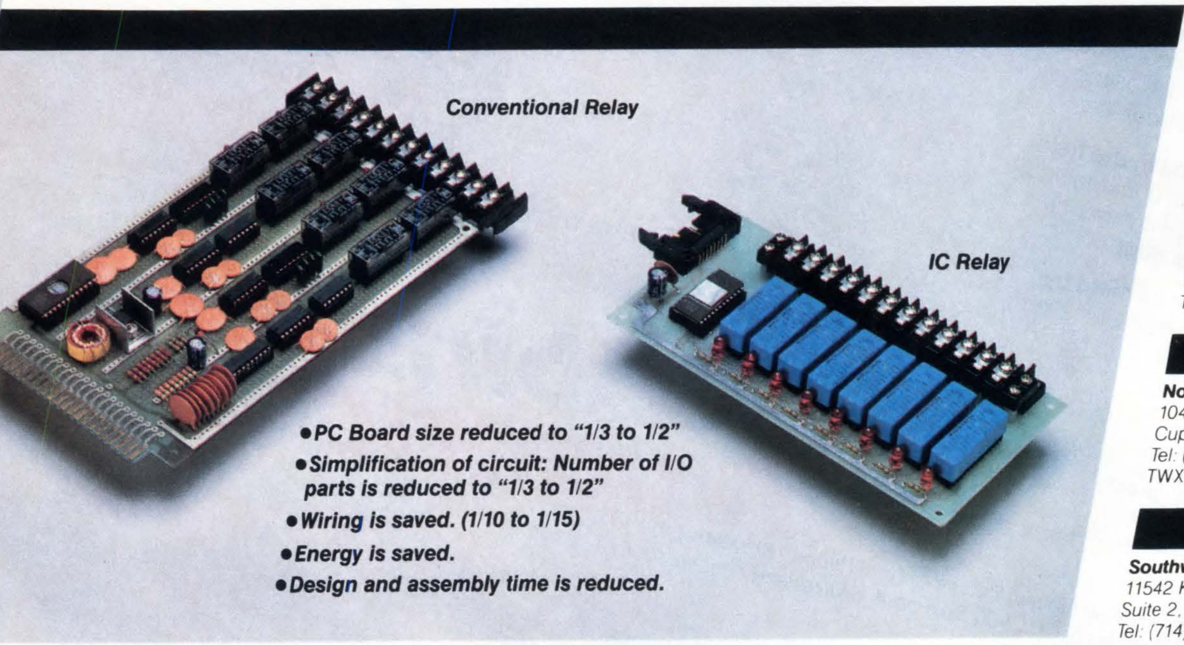
The heart of the Aromat IC Relay is the built-in integrated circuit creating a hybrid relay that combines the benefits of polarized relays and advanced microcircuitry.

Aromat IC Relays are the logical choice for applications where various kinds of peripheral equipment and devices are relay controlled. If many relays are used, these relays can be connected to bus lines through decoders, as shown below.

This Relay Group boasts any or all of the following functions:

1. Extremely low power consumption (steady state—less than 10mW).
2. LSI compatible: negative logic operation.
3. Signal Processing: set, reset, monostable, toggle, automatic set/reset.
4. Built-in noise and bounce cancelling circuit.
5. Power failure countermeasure: set, reset or memory of relay operation when power returns.

For further details contact your Aromat representative or distributor, or write to the nearest address.



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CIRCLE 124

Tiny photovoltaic relays replace reeds to switch low-voltage signals

A solid-state relay provides 2500 V rms of galvanic isolation between input and output; the switch points block 300 V or pass 300 mA.

Electromechanical reed relays have long been the only answer to switching applications that require hundreds of millions of reliable contact closures. However, with the arrival of Crydom's photovoltaic relays, the PVR3300 and PVR3301, a solid-state replacement for reeds is now available.

The photovoltaic relays are superior to even the best reed devices in several ways. They are five times as fast, half the size, and require only one-tenth the power. In large ATE or telephone systems, this significantly reduces power supply size and cost.

Thermal offset is only 200 nV (about one-fifth that of typical reeds), and of course, the relays are not affected by severe shock, vibration, or contact bounce, nor do they generate EMI.

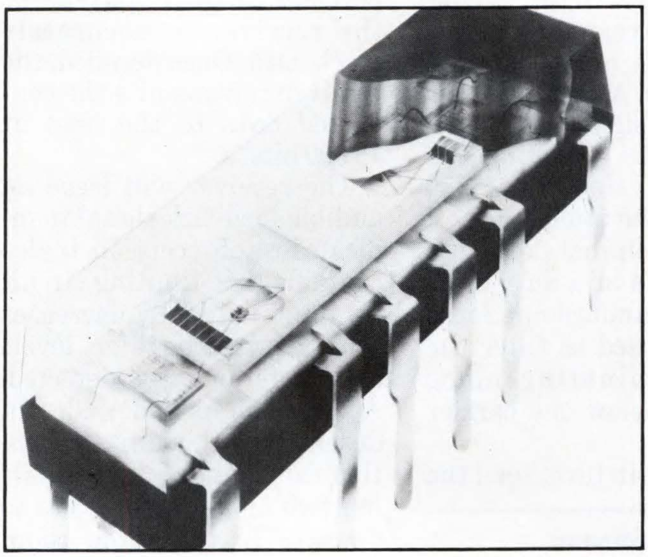
The relays switch as much as 300 mA at 40°C and, when open, the switch points block ±300 V. The PVR3300's off-state, or leakage resistance is $10^{10}\ \Omega$ at 25° with 10 V across it. This figure drops to $10^{9}\ \Omega$ with 240 V applied. Similar resistances for the PVR3301 are $10^{9}\Omega$ and $10^{8}\ \Omega$.

The devices turn on in 250 μs with as little as 2 mA and stay on with a holding power of 500 mW. They turn off in under 50 μs. Additionally, unlike the case with electromechanical relays, poles may be connected in parallel to increase the current rating or lower the on-resistance.

In quantities of 1000, the unit cost of both the PVR3300 and the PVR3301 is $12. Small quantities are available from stock.

Crydom Division of International Rectifier Corp., 1521 Grand Ave., El Segundo, Calif. 90245; Wayne Dinunzio, (213) 322-4987.

CIRCLE 311



Frank Goodenough

COMPONENTS

Wireless keyboard for IBM PC runs months on 4 AA batteries

An rf-resistant wireless keyboard relies on infrared LEDs and CMOS circuitry to transmit digital signals to a host-powered receiver.

One of the first wireless keyboards for the IBM PC personal computer can operate for several months from the power of four size-AA batteries. The 84-key KXN3-8451 from Cherry Electrical Products affords greater flexibility and immunity to rf interference than do conventional designs. CMOS circuitry ensures a small, low-cost, and lightweight unit.

The internal circuitry converts a keystroke into a 9-bit code, which subsequently modulates a 40-kHz carrier signal. That signal drives two infrared LEDs operating at a nominal wavelength of 880 nm. The bit duration is 440 μs, yielding a nominal data rate of 2273 bits/s at a duty cycle of 50%. A standard bandpass network is used to filter the signal, eliminating noise above and below the carrier frequency.

The LEDs, in turn, send the digitally encoded signal to a companion receiver, the OB99-13AL. That unit, powered by the host computer, draws on digital and analog circuitry that includes an 8048 microprocessor and 64 or 128-Kbits of RAM to convert the coded infrared signal into appropriate logic signals. Here, the duration of each bit is also measured to check transmission speed, ensuring it remains within the ± 15 percent range required for the receiver to accurately track data. Once decoded, the receiver retransmits the converted data to the host at 15,000 bits/s.

The receiver will issue an audible feedback signal to indicate loss of reception. It also contains a dc-limiting circuit that automatically decreases sensitivity when high levels of interference are detected. A switch on its underside can desensitize the unit (reception range under 5 ft), allowing two or more receivers to operate in the same room without undue optical interference.

The receiver plugs into the computer's keyboard socket in place of the existing keyboard. Alternatively, it is available as a pc board and can be mounted inside the computer's cabinet. A short cable connects the receiver to an existing communication port and a 5-V supply.

The keyboard can also be connected directly to the receiver, thereby disabling its infrared mode and disconnecting the battery source.

The keyboard costs $190 in single lots, or $100 in OEM quantities. The price of the keyboard and housed-receiver combination is $290, or $150 in quantity. They will be available in September. The pc-board version of the receiver is scheduled for release at a later date.

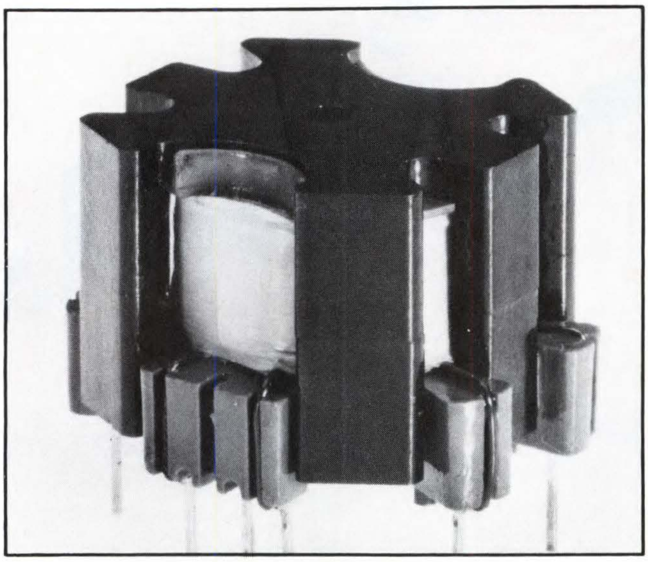
Cherry Electrical Products Corp., 3600 Sunset Ave., Waukegan, Ill. 60087; (312) 662-9200.

CIRCLE 315

Vincent Biancomano

COMPONENTS

6-slot pot core eases switcher design



A ferrite core intended for small, high-frequency switching power supplies having multi-tapped windings solves many of the problems associated with the traditional core-and-bobbin configuration. In particular, the six-slot construction and large bobbin of the CS pot core, from AIE Magnetics, allows the user to adjust the turns ratios more accurately than in conventional two-slot designs. Moreover, it handles greater currents and ensures better heat dissipation.

The core is manufactured from a standard manganese-zinc and ferrite material that works to frequencies of 100 kHz and temperatures of 125°C. It is suitable for flyback transformers that handle up to 50 W.

The unit has a total of 10 terminals for the input and the output windings. The two larger slots are separated from each other by 180° and contain three terminals apiece. The four remaining slots are spaced 60° from any other adjacent slot, and each holds a single terminal.

The foregoing arrangement allows for windings that can be as small as one-sixth of a turn. The core's associated bobbin, which is molded of a flame-retardant material, has relatively broad wire paths and terminals so that large-gauge magnetic wire can be used.

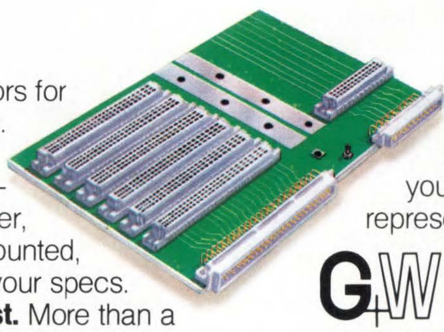
Depending on the configuration, the CS core varies in price from $6 to $12 in lots of 1000.

AIE Magnetics, 701 Murfreesboro Road, Nashville, Tenn. 32710; (615) 244-9024.

CIRCLE 317

Elco sets international standards in high-density connectors.

Today's high-density packaging is creating a new international PC connector standard — the DIN 41612 family — for those applications that demand high contact density, metal-to-metal reliability and low mating forces within small envelope dimensions. Elco is in the forefront of this worldwide effort with the industry's broadest line of one-, two-, three- and four-row standard and inverted styles, including the unique 201-pin in Series 8457. These are available for printed circuit or rack mounting, with solderless VARIPIN™ press-fit, wire wrap or solder terminations; or as I/O connectors for wire or flat cable. Fully tested backpanels, two-sided or multilayer, with VG/DIN mounted, are supplied to your specs.



Elco. The first. More than a dozen years production experience enabled Elco to become the first U.S. manufacturer to qualify its VG/DIN connectors to MIL-C-55302/131-134. Today we're still leading the way in applications like telecommunications, mainframe, micro and military computers, industrial controls, test equipment and instrumentation. When it comes to VG/DIN, come to us. Call your Elco distributor or representative.

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Proven Printed Circuit Connections Worldwide

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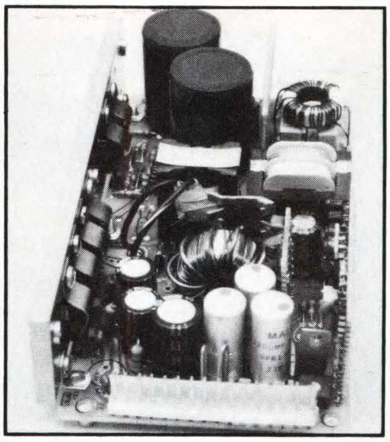
For literature contact Elco Corporation, 74 Brookhollow Drive, Santa Ana, California 92705; (714) 641-2040. TLX: 182131

COMPONENTS

Compact switchers handle 60 W



All 10 members of a family of switching power supplies are housed in packages only 3.25 by 7.0 by 1.75 in. and still handle 60 W apiece. Each of the XL060 series, from CEI Corp., features a 5-V output, and different versions furnish various combinations of one or two additional 5-, 12-, or 15-V outputs. The input voltage to all of the devices is 115 V (50 to 60 cycles).

All outputs rated below 1.5 A are protected by current limiting. The higher current outputs are guarded by current foldback circuitry. Further, dynamic inrush protection ensures that no circuit powered by an XL060 supply can be damaged by ac input surges.

Noise and ripple, under full load conditions, are held to a maximum of 25 mV. Additionally, all of the XL060 series carry an on-board EMI filter. Depending on the load, the switchers' efficiency ranges from 70% to 90%. Finally, a TTL-compatible signal warns of impending ac power failures.

Prices for the supplies start at $59 a unit in lots of 10,000.

CEI Corp., PO Box 501, Londonderry, N.H., 03033; (603) 623-8888. **CIRCLE 306**

Proximity sensor detects most targets

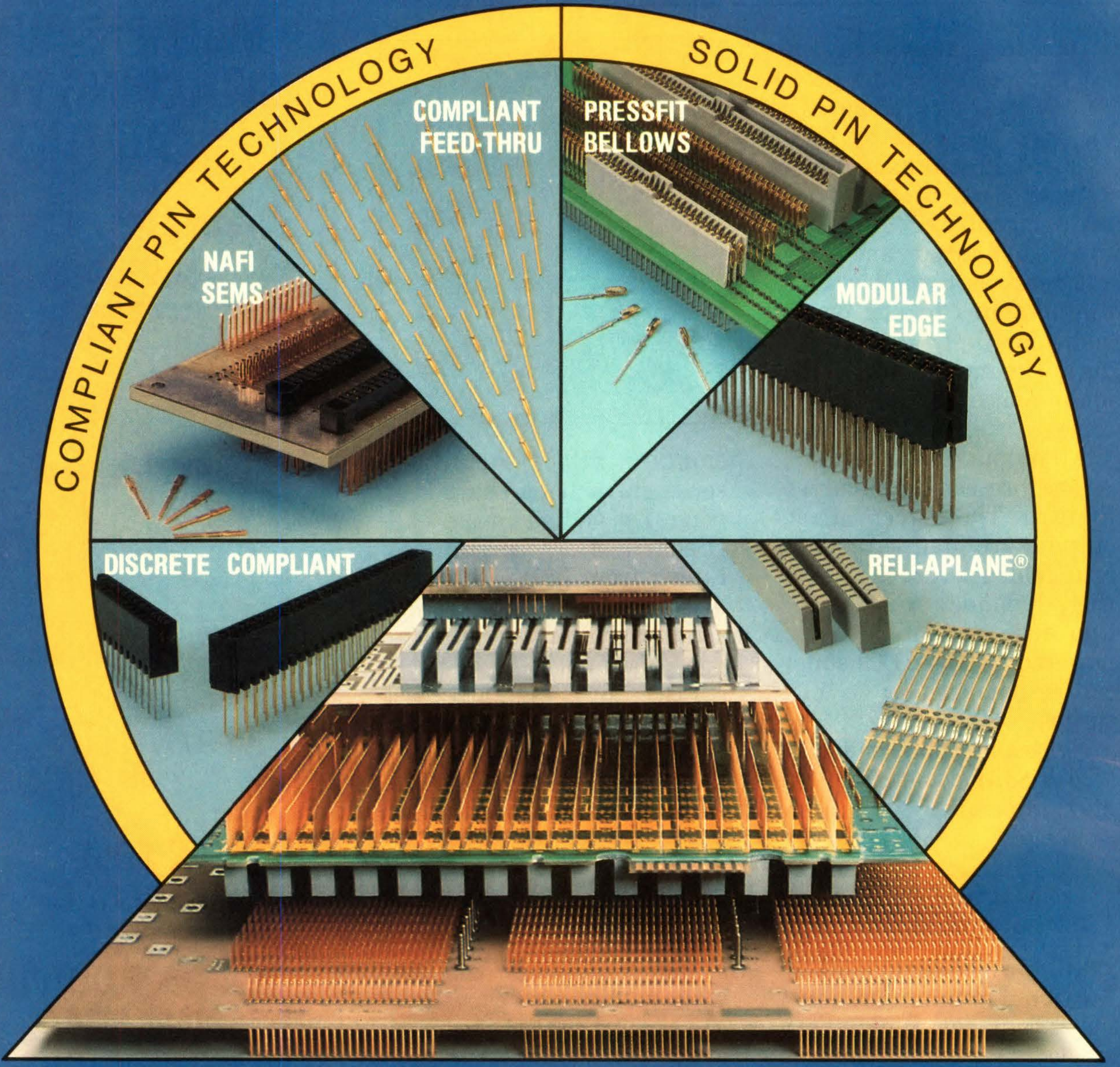
Compared with conventional proximity sensors, the E2K-X series of capacitance-type proximity switches affords longer distance sensing of almost all kinds of metallic and nonmetallic objects at fixed distances of 0.16, 0.32, and 0.59 in. (4, 8, and 15 mm, respectively), without adjusting the sensitivity. The device is available in a wide range of operating voltages—from 90 to 250 V ac and from 10 to 30 V dc—and in a choice of three cylindrical shapes, each threaded for easy installation.

The E2K-X can directly switch loads up to 200 mA, while maintaining a low leakage current (less than 22 mA at 200 V). In addition, dc units in the series offer a higher current capacity (up to 100 mA) and have a switching frequency (100 Hz) that is up to 10 times higher than other capacitance-type proximity sensors.

Omron Electronics Inc., PO Box 4066, Schaumburg, Ill. 60195; (312) 843-7900. $50 to $60; stock to 12 weeks.

CIRCLE 408

RELI-APLANE® BACKPLANE
ASSEMBLIES / COMPONENTS



Methode backplane components are available in solid pin or compliant pin technologies and have been field-proven for reliability and long life. Our complete line of contacts, insulators and discrete pressfit connectors permit versatile, in-house backplane assembly to the most stringent industrial or military requirements. Efficient assembly and test equipment to serve a wide variety of production requirements is also available exclusively from Methode.

It's your choice . . . Methode assembled and tested Reli-Aplane® Backplanes . . . or Methode supplied components and equipment for your in-house assembly.

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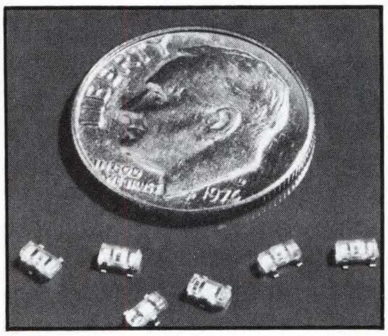
CIRCLE 134

COMPONENTS

Surface-mounted LEDs make debut



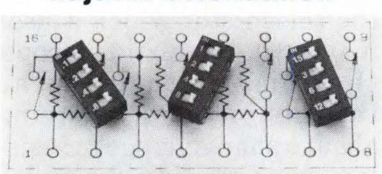
The first family of surface-mounted LEDs, developed by Siemens, comprises high-efficiency red and yellow, as well as green and red-green, LEDs. The diodes are encased in a clear-plastic SOT-23 package with dimensions of 1.3 by 3 by 1 mm. They have a typical luminous intensity of 1.8 mcd at 20 mA and can be seen within a viewing angle of 140° (half-power points). With such characteristics, the LEDs will move quickly into the realm of diagnostic equipment, medical instrumentation, and telecommunications.

The components can be supplied on a 8-mm-wide tape carrier (2000 components per 18-cm reel) that is suitable for virtually any type of automatic insertion equipment. Alternatively, they can be mounted with wave, dipped, or reflow soldering.

The LDH2310 high-efficiency red, the LDY2320 high-efficiency yellow, and the LDG2330 green LED each sell for 60¢ in quantities of 1 to 99, 53¢ for 100 to 999 parts, 45¢ in lots of 1000 to 4999, and 40¢ for 5000 units or more. The LDRG2340 red-green LED sells for 62¢, 55¢, 47¢, and 42¢ in the same respective quantities.

Siemens Corp., Litronix Division, 19000 Homestead Road, Cupertino, Calif. 95014; (408) 257-7910. **CIRCLE 302**

Resistor/DIP switch adjusts attenuation



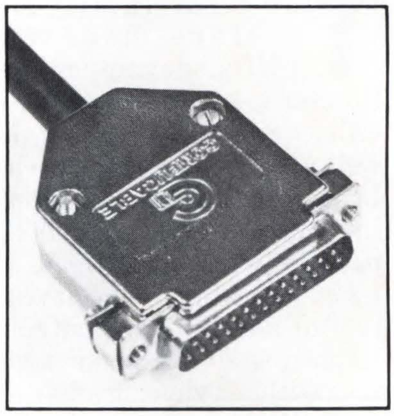
A resistor substrate soldered directly to a DIP switch provides 16-step attenuation in three ranges: 0.1 to 1.5 dB in 0.1-dB steps, 1.0 to 15 dB in 1.0-dB steps, and 1.5 to 22.5 dB in 1.5-dB steps. The combination resistor network and DIP switch requires no more board space than the DIP switch itself. In addition, the package saves assembly time since resistors do not have to be soldered onto the board. Designed for low-level telcommunications tasks, the attenuator DIP switches can be used in any application that does not exceed the 20-dB maximum power rating.

Grayhill Inc., 561 Hillgrove Ave., La Grange, Ill. 60525; (312) 354-1040. $7.25 (100 units); four to six weeks. **CIRCLE 412**

COMPONENTS

Cable connector shell reduces EMI

A shielded plastic shell that meets the FCC's Class B technical standard for EMI solves many interference problems associated with computer cable connectors. Designed to reduce the cost and weight of conventional metalic connectors, the compucable shell is made of fire-resistant plastic, and is plated twice: first with copper for shielding, second with nickel for toughness.



The computer cable enters the shell through a special grommet that, when combined with Mylar seals, protects the cable entrance against leakage. A special locking feature secures the edges of the joined shell. The grommet comes in six different sizes for different cable diameters. A molded log is provided for soldering a cable shield providing both a secure ground and strain relief.

Guaranteed not to chip or peel, the shell varies to fit standard connectors ranging from 5 to 50 pins and can also be customized for cable assemblies. The 25-pin shell is priced at $1.31 each for 1000 units and at 90¢ apiece for 10,000 units.

Compucable Corp., 1440 S. State College Blvd, Anaheim, Calif. 92806; (714) 635-7330.

CIRCLE 313

Airflow switch has 3-s response time

Used to protect power supplies and other electronic equipment against loss of airflow, a solid-state switch triggers an alarm or an equipment-shutdown in less than 3 seconds when the airflow falls below a preset value. Air movements of less than 50 fpm can be sensed by the Series 70 airflow switch, with user-adjustable trip points available in ranges overlapping 50 to 1000 fpm.

The sensing device consists of a thermistor whose resistance changes with temperature. During normal operation, a current is applied to the thermistor which causes it to heat. As airflow drops, the temperature of the thermistor rises, bringing about a sharp change in resistance and causing the device to switch. An LED indicates when a fault condition has occurred, and the switch circuitry is virtually unaffected by ambient temperature or voltage changes.

Quantem Corp., PO Box 7599, Trenton, N.J. 08628; (609) 883-9191.

CIRCLE 409

COMPONENTS

IC pressure sensor is cost effective

Based on an inexpensive shear-stress transducer technology, the SPX50 integrated circuit piezoresistive pressure sensor uses an ion-implanted resistor in an integrated silicon diaphragm to provide an electrical output that is proportional to applied pressure and related shear stress. The device is well suited for price-sensitive applications that require circuit flexibility or compatibility with microprocessors.

The SPX50 has a pressure range of 0 to 7.3 psi and a combined linearity and hysteresis of 0.1% full scale. It is offered in two models: one for absolute measurements and the other for differential (or gauge) measurements. The sensor comes in a compact plastic package.

Sensyn Inc., 1255 Reamwood Ave., Sunnyvale, Calif. 94089; (408) 744-1500. Less than $5 (high-volume quantities). **CIRCLE 320**

Pointing device fits inside keyboard

A pointing device that is 2 in. square and 1/2 in. thick installs directly inside a keyboard and performs the same functions as a mouse. The Keyboard Puck pointing device has three software-definable buttons and addresses a grid matrix of 256 by 256 points. As an option, a full numeric keypad can be placed on the top of the puck so that it may be installed in the same space that is usually occupied by a conventional keypad. The completely digital pointing device needs no adjustment or trimming, either in production or in the field. Evaluation units are available now.

KA Design Group, 6300 Telegraph Ave., Oakland, Calif. 94609; (415) 654-6300. $20 (large quantities).

CIRCLE 321

Mercury switch is omnidirectional

Finding application in actuating equipment, the Model 03EA137 mercury switch is a miniature sensor that mounts on a pc board and makes contact whenever it is tilted beyond a preselected angle, in any direction. It can also be designed to maintain its closure, even if completely inverted, so that it is "off" only when aligned within a specific vertical attitude.

The omnidirectional switch can be fabricated in a variety of dimensions and specified for closures at low or high tilt angles. A switch that makes contact at a 30° inclination is typically 0.6 in. in diameter, 0.6 in. tall, weighs 0.5 oz, and carries up to 2 A.

Kahl Scientific Instrument Corp., PO Box 1166, El Cajon, Calif. 92022; (619) 444- 2158.

CIRCLE 322

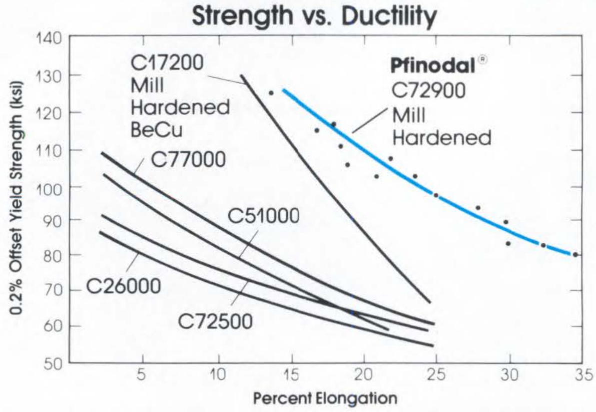
Contacts tooled by Wells Electronics, Inc. for their Welcon™ Burn-In sockets.
Spring contacts, 180° sharp bend, magnified 300%. Cut away to show selective gold plating.

PFINODAL is the name for our family of Cu-Ni-Sn spinodal alloys produced by a high-technology wrought powder metallurgy process. PFINODAL C72900 is a spinodal hardening alloy that meets design and performance properties for miniaturized spring contacts in electronic applications. It is particularly well suited for closely spaced, high-density, high-temperature and corrosive environments.

Available in mill-hardened and age-hardenable strip, it demonstrates these important characteristics:

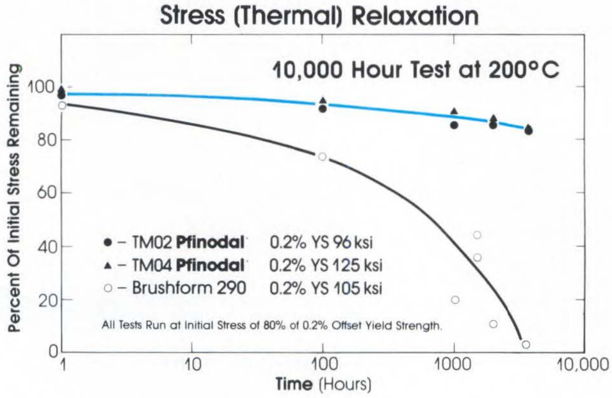
- **Excellent spring properties** combining high strength with superb formability in both directions, as measured by percent elongation and bend ratios (R/t).

Strength vs. Ductility



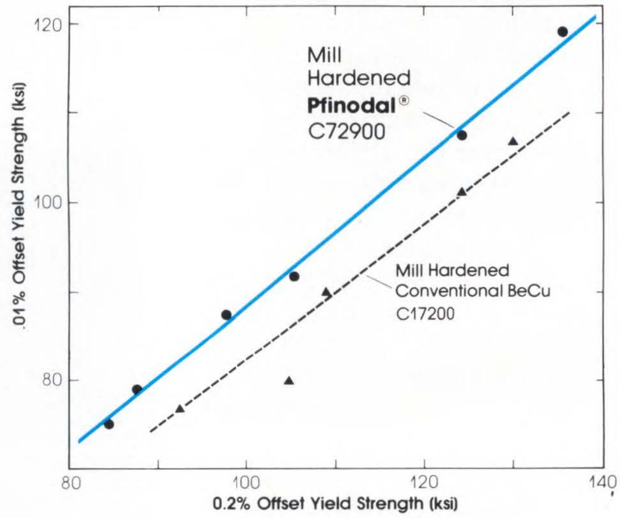
- **Exceptional resistance to thermal relaxation** at 200°C, retaining 80% of initial stress after 7,000 hours. Retains 80% at 225°C after 1,000 hours.

Stress (Thermal) Relaxation



- **Higher usable elastic strength** (proportional limit) for a given 0.2% yield strength. Designers benefit from 8% added elastic strength in addition to excellent formability.

.01% Yield Strength vs. .2% Yield Strength for Pfinodal® and BeCu Strip



- **Stability during post-forming heat treatment** for age-hardenable condition. No distortion problem.
- **Ordered, modulated atomic structure** (well defined sub-lattice) of spinodal alloys contributes to stability of electrical conductivity and thermal conductivity with changes in temperature. Chemical (corrosion) stability reduces the need for plating on bare edges after stamping.
- **Properties.** Chemistry (nominal): Nickel, 15%; Tin, 8%; Copper, 77%. Electrical conductivity: 8% IACS, 26°C-200°C. Formability: 90° Sharp bend at 110 ksi 0.2% YS; 180° 1t bend at 110 ksi 0.2% YS.

For more information on PFINODAL C72900, write or call Pfizer Inc., Minerals, Pigments & Metals Division, P.O. Box 5848, Wallingford, CT 06492. 800-233-2266; in Connecticut, (203) 265-7781.

Pfizer **MINERALS, PIGMENTS & METALS DIVISION**

CIRCLE 138

MATERIALS

Laminate resists high temperatures

At least 25% lighter than laminates made with glass, a modified polyimide Kevlar laminate is highly reliable in hostile thermal environments. Designated HI-7093, the laminate's weight and space savings make it suitable for airborne electronics, military systems, and telecommunications. It has a glass-transition temperature of 225°C and a coefficient of thermal expansion (CTE) of 6.0 ppm/°C in the X and Y directions of its plane. Due to matched CTEs, there is minimal stress in solder connections when the printed circuit wiring board and the leadless ceramic chip carrier expand during thermal cycling. HI-7093 is available in 5-mil (0.005-in.) thicknesses, with standard copper foil cladding on both sides. A 2.5-mil-thick version will be available soon.

Howe Industries, Keene Laminates Division, 13704 Saticoy St., Van Nuys, Calif. 91402; (818) 781-4122.

CIRCLE 323

Silver epoxy has 0.1-mΩ-cm resistivity

Designed for microelectronic applications, a single-component conductive silver epoxy forms a thermally stable bond that has an electrical resistivity of 0.0001 to 0.0005 Ω-cm. The low-viscosity epoxy paste, designated Prima-Solder EH 8310, cures in 15 minutes at 150°C or in 5 minutes at 165°C. The cured adhesive withstands wave soldering and thermal-compression bonding processes from 300° to 400°C. Engineered for chip and substrate bonding, the silver epoxy provides a strength of over 1600 psi at 25°C and over 600 psi at 150°C.

AI Technology Inc., PO Box 3081, Princeton, N.J. 08540; (609) 799-5550. **CIRCLE 324**

Adhesive/sealants provide EMI shielding

Marpoxy 95-4 and 95-7 are two copper-based conductive epoxy adhesive/sealants developed for EMI shielding and similar functions. The products are based on a patented process, which produces a tightly packed copper-flake structure embedded in a resin matrix. Each material is tested according to MIL-STD-461B over the kHz-to-GHz frequency range. Typical attenuation values range from greater than 60 to well over 75 dB. The filled epoxies are two-part thixotropic pastes that cure at room temperature. Marpoxy 95-4 is suitable for continuous use to 125°C and intermittent use to 150°C.

Key Polymer Corp., Jacob's Way, Lawrence Industrial Park, Lawrence, Mass. 01842; (617) 683-9411.

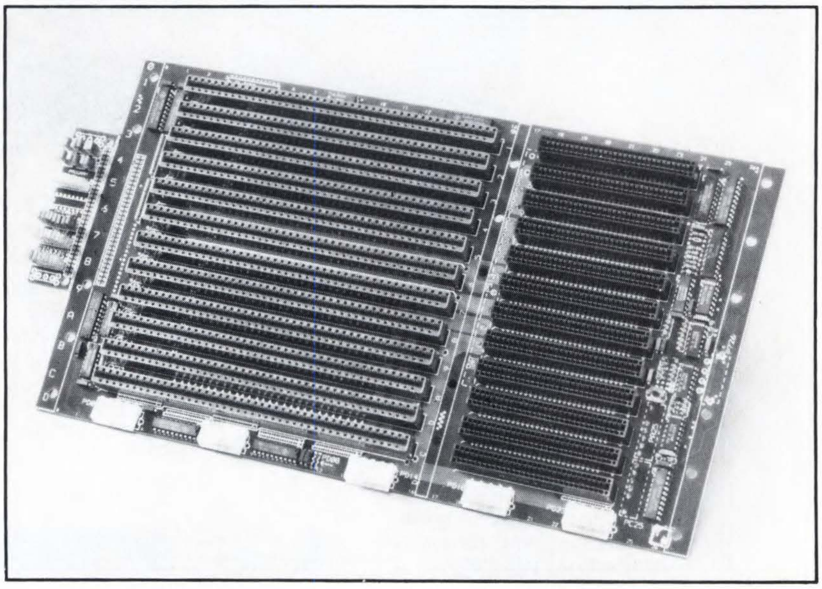
CIRCLE 325

Multibus backplane keeps a watchful eye on system status

Using red and green LEDs, a Multibus backplane furnishes a visual display of system conditions. It also responds to queries from the main program.

A Multibus backplane keeps tabs on a system's status in two ways. It supplies a visual readout, using red and green LEDs, and allows any equipment on the bus to interrogate it under program control. The Sentinel, from Pacific Microcomputers, checks on voltage, temperature, and bus status.

Ray Weiss



The backplane's LEDs show pending bus interrupts (0 through 7), eight major bus control strobes, and two byte values—the bus master ID and a special programmable byte.

The light-emitting diodes monitor five on-board voltage lines. An out of specification voltage (±10%) will turn on a red LED rather than a green one. Further, the board's LED section can be detached and linked by cable from a remote location.

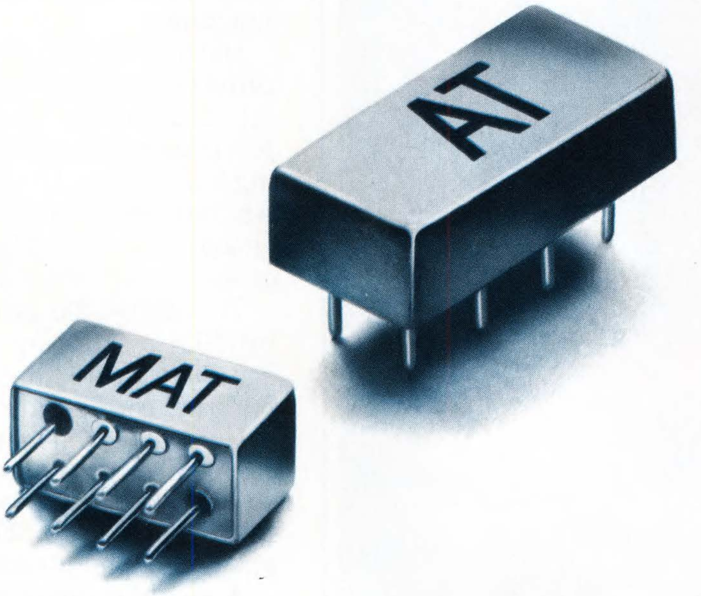
Using designated I/O addresses, any bus master can read or write to the backplane, treating it as it would any I/O device.

For greater reliability and noise immunity, all bus signal lines have controlled impedances and ground traces between signals. To minimize ground currents and spurious noises, one of the board's four layers functions as a ground plane.

The board works with Multibus P1 and P2 connectors. On-board power is furnished by a 60 A screw-on power terminal connector, and there are on-board power connections that accommodate various peripherals.

A single board costs $1200; in quantities of 100 or more, that price drops to $960. The Sentinel will be available at the end of this month.

Pacific Microcomputers Inc., 160 Chesterfield Drive, Cardiff, Calif. 92138; (619) 436-8649. **CIRCLE 304**



AT
MAT

COMPUTER BOARDS

2-board set displays 256 colors fast

The GXB-1000A display processor is a two-board set that lets users display up to 256 colors at high speeds.

The Multibus-compatible boards from Matrox consist of the VGM-1000A, an 8088-based virtual graphics machine, and the RMB-1000, a 512-kbyte image frame buffer.

The graphics card uses pipelined processors to draw low-resolution figures at 1.25 million pixels/s and high-resolution graphics at 300,000 pixels/s. Large areas can be filled in with a single color at a rate of 1 million pixels in just 16.6 μs.

The board has a 4096-color look-up table, expandable to 16 million colors. Any bit plane can be used for overlay functions.

Data from RAM is captured by a display list processor, also an 8088, then passed to a pixel processor before being handled by the 8088 CPU. An interpreter in firmware recognizes 256 high-level graphics control commands.

The RMB-1000 can store a full 1024-by-1024-by-4-bit image but can be programmed for other configurations.

Up to four memory cards can be tied to a single processor card to provide resolution for up to 1600 by 1200 pixels and up to 16 bit planes/pixel.

A single memory card can refresh a 1024-by-768-pixel image at 30 Hz, or a 640-by-480-pixel display at 60 Hz.

A single display processor set lists for $4800. Production quantities will be available next month.

Matrox Electronic Systems Ltd., 5800 Andover Ave., Ville Mont-Royal, Quebec B4T 1H4, Canada; (514) 735-1182.

CIRCLE 307

OEM Decision Makers

"Only the Invitational Computer Conferences bring the latest OEM computer and peripheral products to your front door. You'll find us there!"

BEN WANG, President
Wangtek

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Jan. 29, '85	Houston, TX
Jan. 31, '85	Dallas, TX
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CIRCLE 142

COMPUTER BOARDS

Controller combines hard disk, floppy tape

Offering a full implementation of the Small Computer System Interface (SCSI), the SI500 controls up to two 5¼-in. Winchester disk drives and two floppy-disk drives, in addition to one floppy-tape drive. The new Tandon floppy-tape drive, which uses a ½-in. tape in a single-reel cartridge, provides the mass storage capabilities of tape at a lower cost than current streaming drives. The SI500 controller transfers data at rates up to 1.25 Mbytes/s. Up to 256 kbytes of optional cache memory may be added to the board, giving it a 30% to 40% increase in performance.

Sysgen Inc., 47853 Warm Springs Blvd., Fremont, Calif. 94539; (415) 490-6770. $400 (OEM quantities).

CIRCLE 326

Board gives IBM PC SCSI-based storage

The IB01 host adapter board brings the versatility of SCSI-based 5¼-in. Winchester disk and ¼-in. cartridge tape storage to users of the IBM PC. Occupying one slot in the computer, the IB01 contains an on-board protocol controller, which implements the SCSI protocol and frees the processor from implementation overhead. Since the protocol does not distinguish between mass storage devices, a variety of SCSI-based disk or tape drives can be attached to the IBM PC without having to modify the operating system software. With the IB01, hard-disk memory can be expanded to 1 Gbyte or more in a single system. A single host adapter can handle up to seven SCSI-compatible disk controllers, each of which can control up to two Winchester disk drives. The IBM host adapter is available with or without an Emulex-supported PROM, software driver, and disk utilities.

Emulex Corp., 3545 Harbor Blvd., PO Box 6725, Costa Mesa, Calif. 92626; (800) 854-7112 or (714) 662-5600. $345 and $395 (depending on options); 30 days.

CIRCLE 327

Alphanumeric controller supports four displays

An alphanumeric display controller supports four independent color or monochrome displays, each having a programmable resolution of up to 24 lines consisting of 80 characters per line. The Multibus-compatible board, designated the MSBC-QV3, generates RS-330 video signals capable of driving most standard RGB monitors. The character generator contains a set of 128 ASCII characters, while on-board memory stores 7 bits of attribute code per character. Video attributes include foreground and background color selection, underline, and blink. Each character can be assigned one of 127 available foreground/background color combinations, selected from a pallette of 256. The MSBC-QV3 accepts DTMF signals from four separate keyboards and converts the data into 4-bit binary code to be read by the system processor.

Matrox Electronic Systems Ltd., 5800 Andover Ave., Montreal, Que. H4T 1H4, Canada; (514) 735-1182. $1620; stock. **CIRCLE 328**

Counter module has eight 5-MHz channels

Fully compatible with the VMEbus, an intelligent counter module features eight independent counting channels, with counting rates up to 5 MHz. The XVME-230 board also boasts six firmware-controlled counting functions: period measurement, frequency measurement, position measurement, event counting, duty-cycle control, and stepping motor control.

Its standard I/O architecture provides standard logical interfacing for module identification, module addressing, diagnostics, and module status and control. In addition, the XVME-230 enhances system performance by offloading the host processor of many time-consuming functions. Typical applications include mechanical control, flow measurement, cycle counting, closed-loop control, interval measurement, and frequency generation.

Xycom Inc., 750 N. Maple Road, Saline, Mich. 48176; (313) 429-4971. $1900.

CIRCLE 329

COMPUTER BOARDS

IBM PC board mixes text, graphics

An intelligent graphics subsystem card and its proprietary software produces documents with both text and graphics on either an IBM personal computer (fitted with a hard-disk drive) or an IBM PC XT. In addition, the Graphcard 100, developed by Concept Technologies, also serves as a multipurpose virtual graphics controller interface for both of the machines.

The card carries an 80186 16-bit microprocessor and two custom gate arrays. Together, they supply the circuitry needed to emulate and replace the computers' monochrome and color graphics display adapters. Also on the board are 32 kbytes of dual-port memory, 8 kbytes of system ROM, 128 kbytes of system memory, and 64 kbytes of display memory.

The 80186 controls all of the action on the board, including graphics calculations. The twin gate arrays are responsible for the emulation and display functions.

The board can handle a display of 720 by 352 pixels and furnishes both serial and parallel printer ports, as well as an input port for a mouse. Two levels of intensity are possible with a 50-Hz noninterlaced display that is 25 rows by 80 columns.

A single Graphcard 100 costs $1250. When packaged with a mouse, disk-based software, and instruction manual, the board is sold under the name of Concept 100 and costs $2195. The second board incorporates Graphic Software Systems' implementation of the proposed ANSI virtual device interface (VDI).

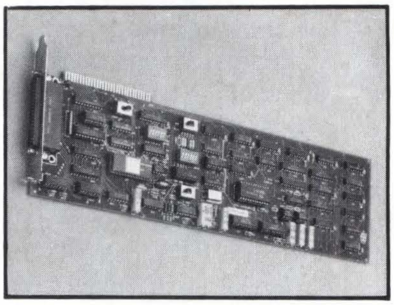
Concept Technologies Inc., PO Box 5277, Portland, Ore. 97208; (503) 684-3314.

CIRCLE 303

COMPUTER BOARDS

Data acquisition board serves IBM PC

A plug-in 12-bit data acquisition board is now available for users of the IBM PC and compatible systems. The Dash-16 from MetraByte resides directly on the PC's system bus and performs up to 40,000 analog-to-digital conversions per second. All the utility software needed for the board's functions is provided on a floppy disk.



The analog input consists of 16 single-ended or 8 differential channels, all switch-selectable. Analog signals pass through an instrumentation amplifier with 0.01% linearity. Gains of 1, 10, 100, or 1000 are selected with an on-board DIP switch.

Converted data may be transferred to the PC via program or interrupt. When meeting the fully rated speed of 40,000 samples, however, converted data is transferred via DMA.

The Dash-16 includes two 12-bit multiplying d-a converters that can be used with either a fixed or a variable ac reference. The device also contains a three-channel 16-bit programmable interval timer with a 1-μs time base.

The board attaches to the back of the computer using a standard 37-pin D connector. The single-piece price, including software, is $895.

MetraByte Corp., 254 Tosca Drive, Stoughton, Mass. 02072; (617) 344-1990.

CIRCLE 309

We've got the power and the proof.

Whether you're designing in power for high drain portable tools or fail-safe on-board memory backup, Sanyo has the dependable nickel cadmium batteries you need. Standard versions can provide from 50 mAH to a full 10.0 AH. And there are also Quick Charge, one hour fast charge, high temperature, memory backup and complete battery pack assemblies.

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The proof of Sanyo superiority can be found in our hundreds of satisfied customers. Demanding customers who subject incoming Sanyo batteries to the strictest inspection standards. Result? Sanyo batteries consistently exceed customer specs for quality. So much so in fact, that we've been named "Vendor of the Year" several times by some of the toughest customers around.

For quality and dependability, Sanyo delivers. We'd like to be able to convince you with the proof. Contact Sanyo for complete technical information on Sanyo nickel cadmium and lithium batteries.

CIRCLE 145

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(312) 595-5600

Los Angeles Office
West Artesia Blvd.
Compton, CA 90220
(213) 537-5830

Robot eliminates hand-soldering

Eliminating time-consuming hand-soldering of discrete points, the ECS 201 robotic soldering system allows special components to be added to the top or bottom of a board after wave soldering has been completed. Soldering is performed by a robotic end effector that randomly solders a broad variety of component junctions, standoff pins, and compound leads—without the need for a prescribed pattern or order of soldering.

Solder is fed automatically to the soldering head from a reel, with feed duration and iron temperature controlled by the robot. The robot moves the solder head from point to point at a rate of up to 55 in./s. An average point can be soldered in 1 to 3 seconds. The precision of the ECS 201 allows a repeatability to within ±0.001 in.

Chad Industries, 1060-K N. Batavia St., Orange, Calif. 92667; (714) 997-4350. From $40,000 to $50,000. **CIRCLE 330**

Robot-based work cell inserts pcb components

The FlexCell assembly workstation, a turnkey pc board component-insertion work cell, incorporates several intelligent subsystems that are directed by a single computer/controller. Fixtured to a rigid superstructure, intelligent feeding systems present work to an assembly robot on demand. The MiniSembler 2000 four-axis robot performs insertion functions, maintaining accuracy and repeatability to within ±0.001 in. throughout its entire 22-by-14-by-5- in. work envelope. The robot's multiposition gripper device holds multiple end effectors for inserting different classes of components.

The FlexCell workstation interfaces with most CAD and host-computer data bases to handle functions that are otherwise performed by the computer/controller if a computer system is not already in place.

Control Automation Inc., Princeton-Windsor Industrial Park, PO Box 2304, Princeton, N.J. 08540; (609) 799-7743. **CIRCLE 331**

Electronic scales weigh 600 g to 600 kg

For weighing anything from fine powders to heavy castings, the KS series of industrial scales senses capacities ranging from 600 g to 600 kg. An LCD display indicates standard weight conversions in grams, ounces, troy ounces, kilograms, pounds, and pennyweight (for the small-capacity scales). Uniform accuracy throughout the capacity range is maintained with an automatic variable resolution feature, which increases resolution as weight decreases. Counting and sampling resolution ranges from one part in 150,000 to one part in 300,000. For weighing unstable loads (e.g., a live animal) or for use in unstable environments (e.g., a rocking boat), the scales use a digital mass transducer to measure mass against an internal reference weight.

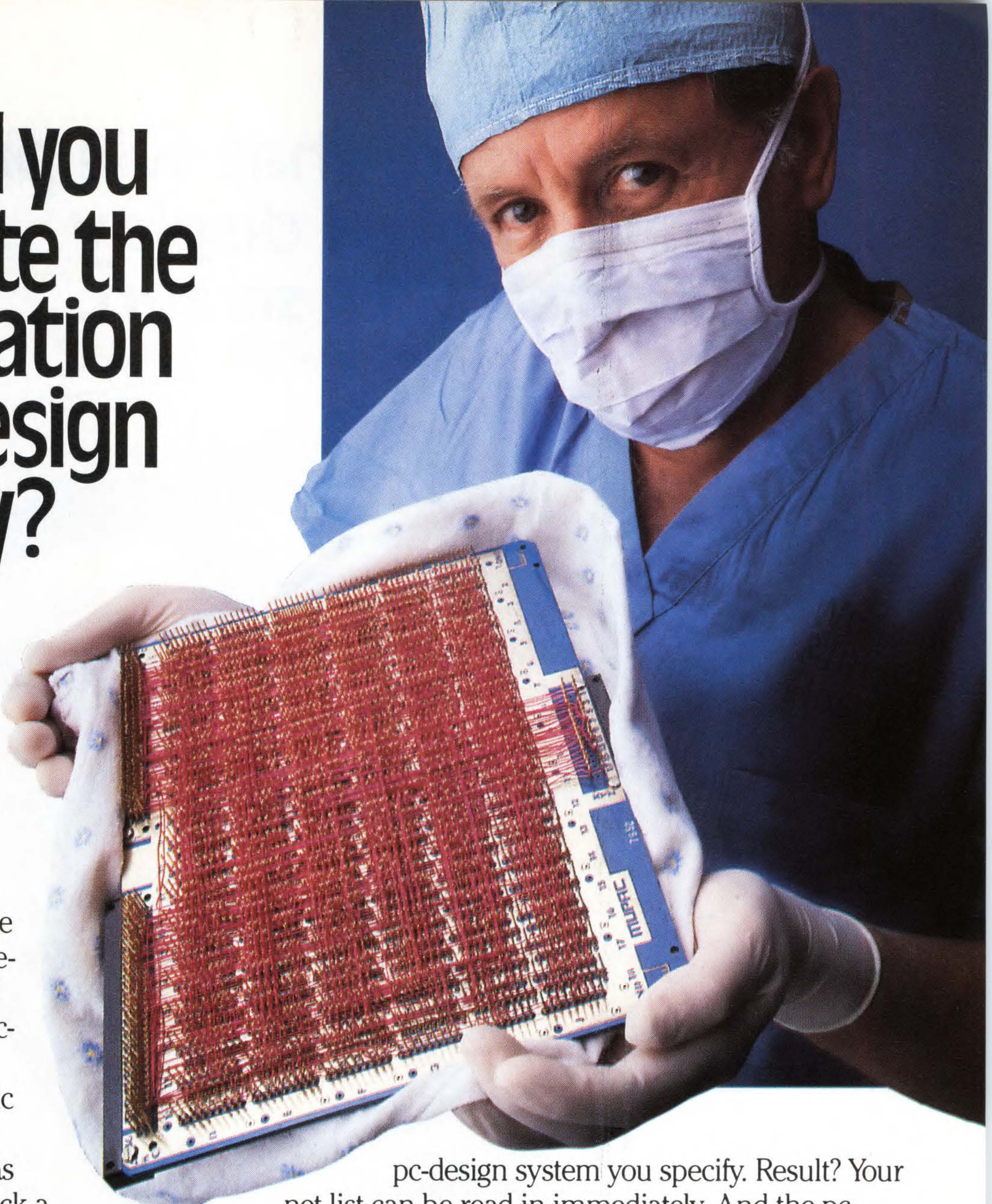
K-Tron Arizona Inc., 7955 E. Redfield Road, Scottsdale, Ariz. 85260; (602) 991-0990. From $1195 to $3100. **CIRCLE 332**

Fuse-receptacle combo meets VDE specs

A VDE-approved module, consisting of a European-type power receptacle combined with a fuse and an input-voltage selection card, brings host equipment closer to VDE approval and permits compatibility with most line voltages throughout the world. Installed as an integral part on electronic equipment, Elim-A-Shock II automatically ensures the manufacturer of VDE approval for the power receptacle and the fuse. The module incorporates an anti-shock safety feature that prohibits access to the fuse or other live parts while energized. Up to four different input voltages may be selected by means of a small pc card, which inserts into the module in different positions.

Hopkins Engineering Co., 12900 Foothill Blvd., San Fernando, Calif. 91342; (818) 361-8691. **CIRCLE 333**

How would you like to create the next generation in circuit design technology?



We'll make it easy.

All you have to do is come up with that new, beyond-the-state-of-the-art idea. The one destined to push back the horizons in electronic circuit design technology.

Then send your schematic or circuit net list—along with an unwired panel—to dataCon. In as little as a week we'll send you back a fully machine-wired, 100% inspected and tested, completely documented circuit board for your new design. So you can debug that hot new idea, validate it, and document it—before committing to expensive pc artwork.

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dataCon's Board 1 Service takes you from circuit design to hardware faster, more accurately, and for less money than the way you're probably doing it now.

Even if your final circuit design will be produced as a multilayer printed circuit board.

As part of our Board 1 Service, dataCon can provide a machine-readable circuit net list formatted for the CAD pc-design system you specify. Result? Your net list can be read in immediately. And the pc-design process can be underway while you debug your wire wrapped prototype.

It's fast. It's easy. It saves you money. And it's 100% accurate.

Find out how dataCon's exclusive Board 1 Service and net listing can bring a whole new generation of accuracy and efficiency to your circuit design efforts. Call the largest independent wiring service in the world. dataCon. There's an office near you.

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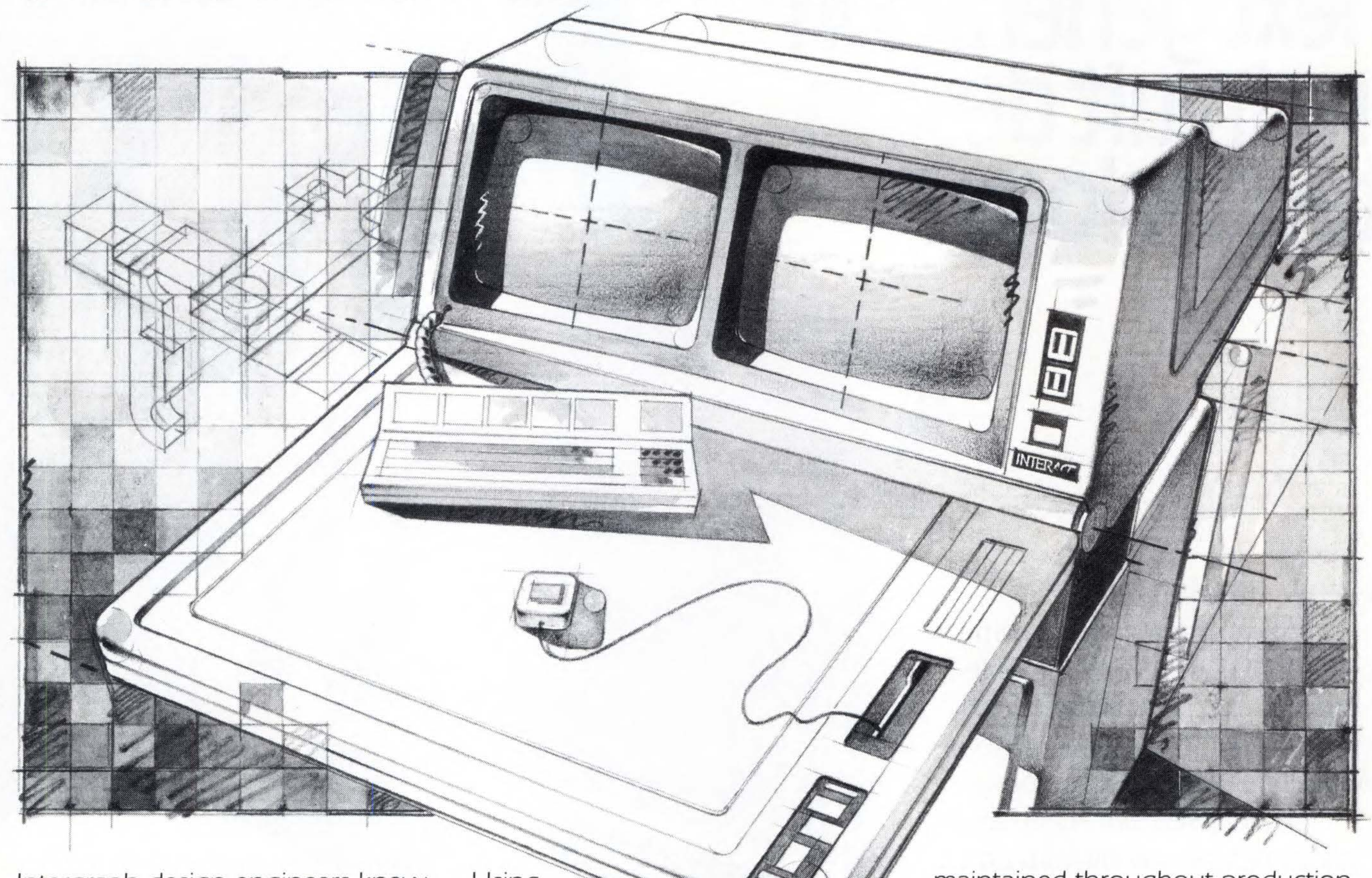
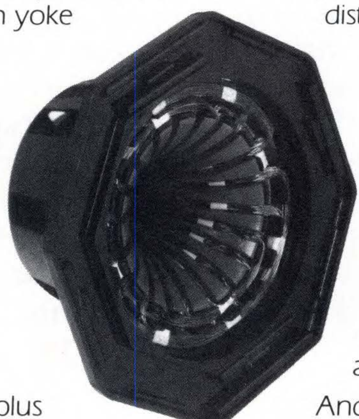
CIRCLE 146

THE CHALLENGE:

Develop a yoke that will produce a 1.3 million pixel display on a 20-inch CRT screen.



Intergraph design engineers knew a 1.3 million pixel display for their new CAD workstation would be a challenge to develop. It would require a deflection yoke with a very wide deflection angle and very tight geometry. That by increasing resolution, they could reduce operator strain.



So they turned to Discom. Taking advantage of Discom's thirteen-plus years of developing components that have continually raised the state-of-the-art in display technology, Intergraph engineers were able to realize their objectives.

Using Discom's patented non-uniform conductor distribution process, Discom engineers developed a yoke with a 114° deflection angle and less than 1% geometry tolerance. And 1000 line resolution. Then Discom's full-capability prototype lab built prototypes for testing and evaluation.

And, when they were ready for production, Intergraph again turned to Discom. They knew Discom's precision stator construction would assure that design tolerances would be maintained throughout production.

In large-screen graphics, as well as avionics and VDT's, Discom is helping the world's largest electronics manufacturers meet their design challenges. And often saving them time and money in the process. Circle the number below on the reader response card, or call (617) 692-6000 and challenge Discom.

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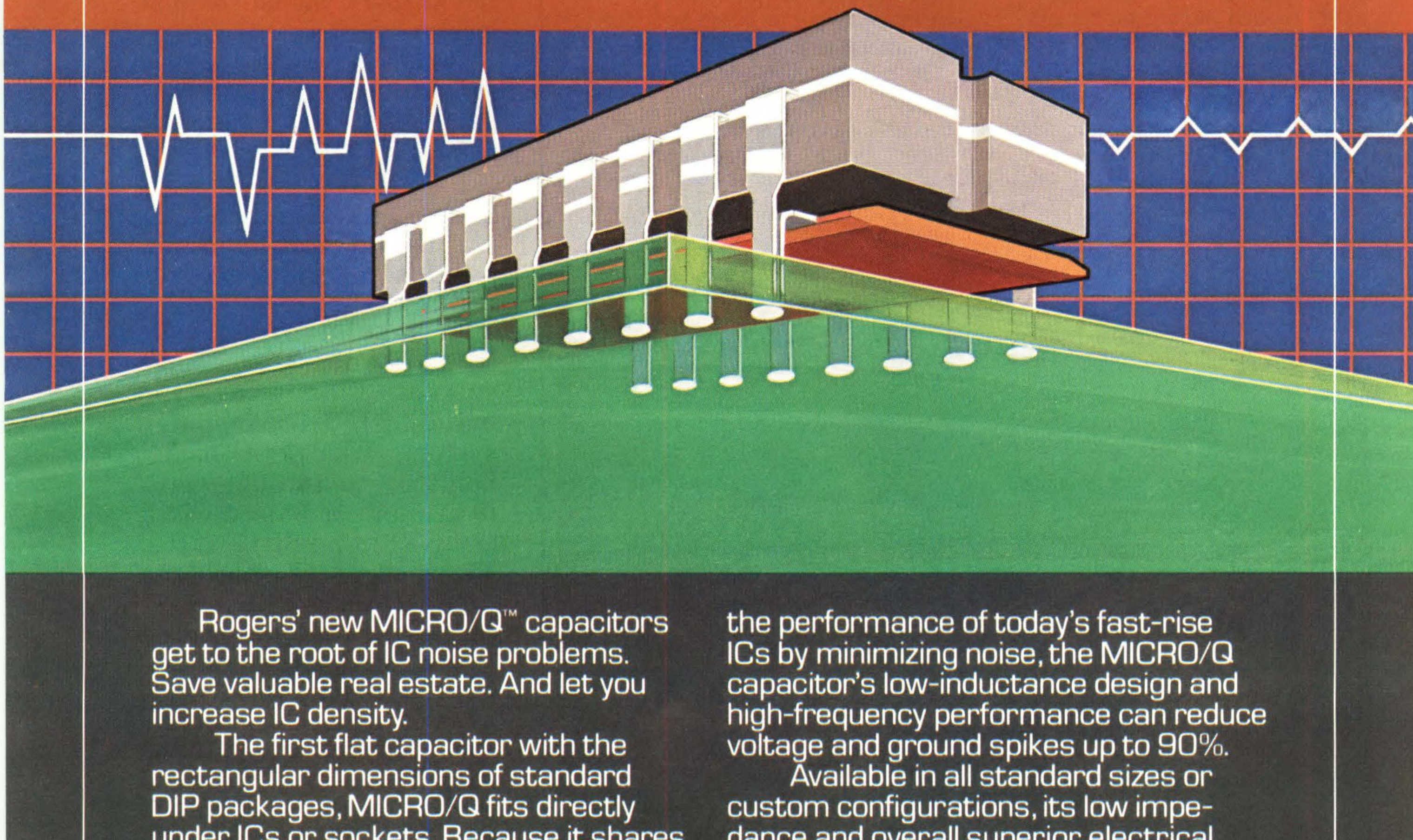
 CIRCLE 147

NOW THE SOLUTION TO IC NOISE IS RIGHT UNDER YOUR DIP.

INTRODUCING MICRO/Q HIGH-FREQUENCY DECOUPLING CAPACITORS FROM ROGERS.



Rogers' new MICRO/Q™ capacitors get to the root of IC noise problems. Save valuable real estate. And let you increase IC density.

The first flat capacitor with the rectangular dimensions of standard DIP packages, MICRO/Q fits directly under ICs or sockets. Because it shares the same power and ground holes, there's no need to modify regular two-sided or multilayer boards. Use of outboard mounting holes is optional.

Specifically designed to optimize the performance of today's fast-rise ICs by minimizing noise, the MICRO/Q capacitor's low-inductance design and high-frequency performance can reduce voltage and ground spikes up to 90%.

Available in all standard sizes or custom configurations, its low impedance and overall superior electrical performance will enhance the operation and reliability of virtually any board design. For all the facts, contact a Rogers MICRO/Q Product Specialist today at (602) 830-3370.

ROGERS

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602 830-3370

CIRCLE 148

PACKAGING & PRODUCTION

RS-232-C breakout box has expansion port

An RS-232-C breakout box serves as a cable interface and a port expansion device, as well as a diagnostic tool. The shared-port feature of the Serial Support unit allows two peripheral devices to share a single output port. A passive signal splitter eliminates the need to manually switch from one peripheral to another. For cable interfacing, Serial Support adapts output lines to any configuration through its Versa-Matrix shunt system of incoming and outgoing lines. Common jumper configurations are displayed on the front panel. The device also displays the status of essential lines on the serial port, using tristate displays for RS-232-C signal voltage-level validation.

Optronics Technology, 2990 Atlantic Ave., Penfield, N.Y. 14526; (716) 377-0369. $133; stock. **CIRCLE 334**

Q-bus card cage holds 16 LSI-11 cards

Compatible with the Q-bus, two card cages make suitable foundations for building LSI-11 computer systems. The 8LCC model holds up to 16 dual-width (8-by-5-in.) or 8 quad-width (8-by-10-in.) LSI-11 cards. The smaller 8LCC/2 holds up to eight dual-width LSI-11 cards. The 8LCC is also a good choice for expanding an existing system, since the expansion connectors on the backplane do not require the use of a slot in the cage to connect to the first system cage. Both units offer tapered entry connectors with gold-plated bifurcated contacts and thin, color-coded card guides for easy card alignment during insertion.

Andromedia Systems Inc., 9000 Eton Ave., Canoga Park, Calif. 91304; (213) 709-7600. $350 (8LCC), $225 (8LCC/2); stock. **CIRCLE 335**

Fujitsu modems have lots of ways to fit into your plans.

At Fujitsu, we offer a diverse line of OEM high-speed stand-alone modems and boards to bring out the best in your product designs. Now you can take advantage of the industry's most technologically advanced features. Like operating speeds up to 14,400 bits per second. Like powerful automatic equalizers that minimize the effects of line interference. And versatility that makes our modems compatible with any type of equipment.

As one of the world's largest data communications suppliers, we know that our growth depends upon how well our products help your company grow. That's why we continue to develop OEM products on the cutting edge of technology. And every product we make is backed by the Fujitsu name — recognized worldwide as a leader in data communications products.

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FUJITSU

CIRCLE 150

COMPUTER SYSTEMS

8-bit micros link up to 4080 users

The Omni line of 8-bit multi-user microcomputers serves as an efficient, low-cost alternative to a local area network. Multiple Z80A and -B processors are networked within each Omni computer, running under the CP/M-compatible TurboDOS multi-user operating system. Direct memory transfers and the use of four DMA channels speed overall processing. Each user accesses his own dedicated Z80 processor board, containing 128 kbytes of RAM, two serial ports, and two parallel ports. Omni models include the Series 1000, 2000, 3000, and 4000, which support up to 5, 10, 16, and 32 users, respectively. The Series 5000, like the 4000, also supports up to 32 users but can be linked with other Series 5000s. By linking 128 fully configured units, 4080 users can be supported.

Digital Computer Corp., 7430 Trade St., San Diego, Calif. 92121; (619) 566-8500. $3995 to $15,490 (minimally configured Series 1000 and 5000, respectively). **CIRCLE 336**

Workstation speeds VLSI chip design

Integrated-circuit designers can address the complete design cycle of custom VLSI chips—from logic design to mask-set definition, including full simulation and test development—with the Chipmaster workstation. The system includes a 32-bit data base, a high-performance mask editor, and a hardware-assisted graphics accelerator. Operating at 80 million pixels/s, the graphics accelerator provides immediate interaction so the user spends less time waiting for the display—a performance increase of two- to ten-fold over conventional CAD systems. Chipmaster's integrated software is completely compatible with existing CAD systems that read and write the industry-standard GDS II stream format, from which the final design is fabricated.

Daisy Systems Corp., 139 Kifer Court, Sunnyvale, Calif. 94086; (408) 773-9111. $120,000. **CIRCLE 337**

Computer runs two operating systems

Comprised of six models, ranging in performance from the supermini Model 810 to the high-end Model 990 which is 60 times more powerful, the Cyber 180 family employs a unique multistate architecture. This architecture lets the computer simultaneously run two operating systems in the same memory and central processing unit. The Network Operating System (NOS) and NOS/VE (virtual environment) provide the tools for handling 6- to 8-bit and 60-to 64-bit word conversions.

The Cyber 180 line offers easy portability from other systems, and all application and system software within the line is portable without change. The Unix System V(VX/VE), available as a subsystem under NOS/VE, allows application programs running under Unix to be ported to the Cyber 180 systems.

Control Data Corp., Computer Systems, PO Box 0, Minneapolis, Minn. 55440; (612) 853-2622. From $250,000 to $6 million. **CIRCLE 338**

Q-bus microcomputer is super compact

A Q-bus-compatible microcomputer system, the SMS 1000 Model 40 runs all system and application software designed for the LSI-11/23 or -11/73 CPU without modification. The foundation module, which does not require a backplane slot, integrates the mass-storage device controller, two serial ports, all backplane circuitry, and the support monitor subsystem on a single board. Housed in a 5¼-in. rack-mount or floor-mount enclosure, the Model 40 supports real-time and time-sharing operating systems, including RT-11, RSX-11M-Plus, RSTS/E, Unix, and TSX Plus. It is available with either the LSI-11/23 or -11/73 CPU, up to 2.5 Mbytes of main memory, and a variety of Winchester/floppy-disk drive combinations.

Scientific Micro Systems Inc., 777 E. Middlefield Road, Mountain View, Calif. 94043; (415) 964-5700. From $5800; eight weeks. **CIRCLE 339**

The one number to call for Winchester and diskette drive repair.

TRW is <u>the</u> disk drive repair service you can count on! Now you can trust your critical repair requirements to the one company with a successful nationwide reputation in electronics maintenance and repair: TRW Customer Service Division.

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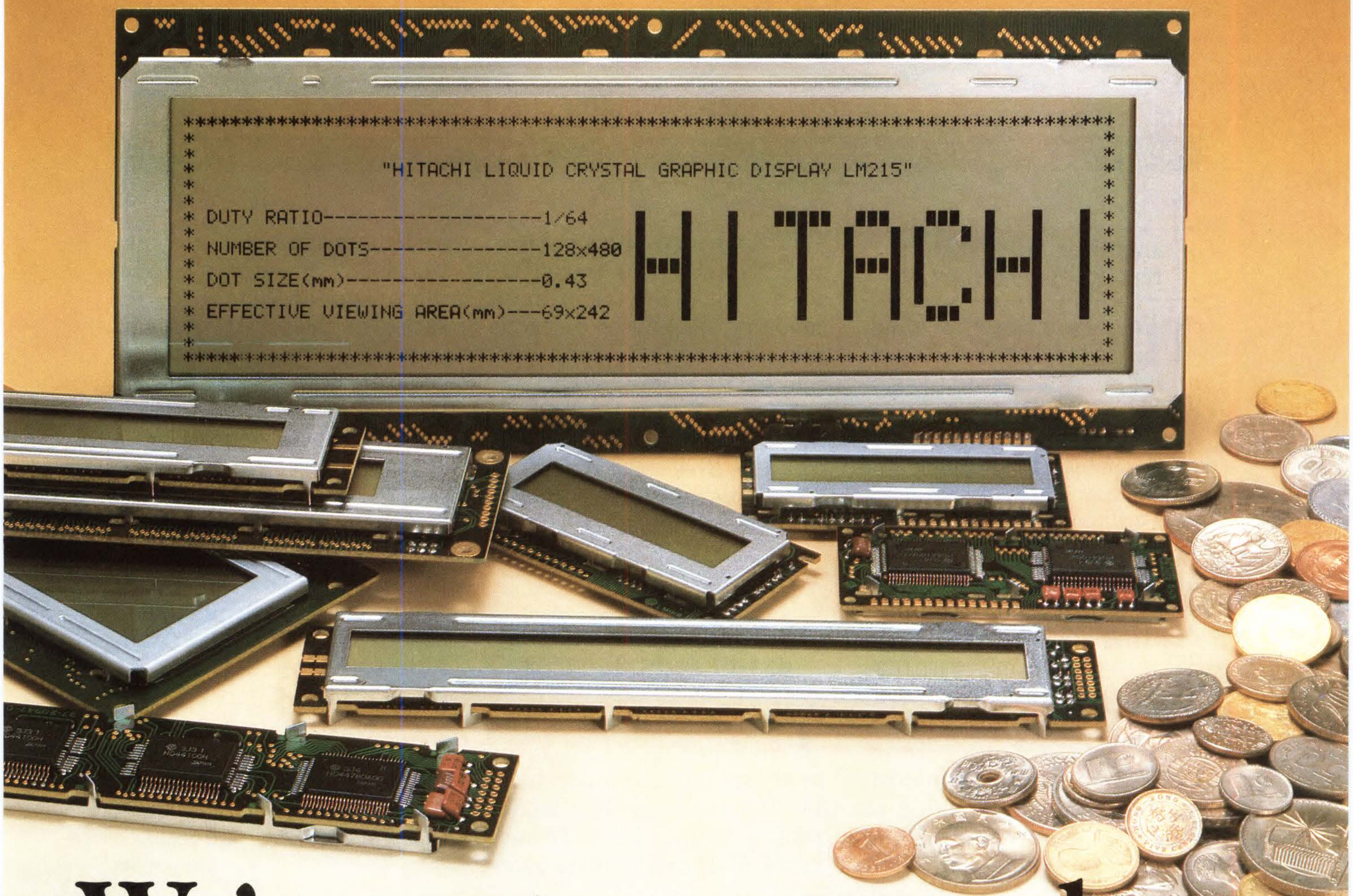
CIRCLE 182



We've got your numbers

And your patterns and characters, too. They are available on a wide variety of Hitachi liquid crystal display modules, from small single-line numeric units to one of the largest (128×480) dot-matrix graphic displays on the market today.

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Each module either comes with an external controller or has its controller built-in. That means you can apply Hitachi LCDs immediately in calculators, digital clocks/watches, computer peripherals, office-type telephones, portable electronic typewriters, compact computers, facsimile machines, medical/scientific equipment... the possibilities are virtually unlimited when you choose Hitachi.

■ **Graphic Displays**

Type No.	Display Capacity (dot × dot)	External Dimensions W × H × T (mm)	Controller
H2525	20 × 239	220 × 53 × 15 max.	External CB1020R (HD61830)
LM021	24 × 479	290 × 60 × 13 max.	
LM200	64 × 240	180 × 75 × 15 max.	
LM213B	64 × 256	184 × 75 × 12 max.	Built-in
LM211	64 × 480	270 × 82 × 13 max.	External CB1026R (HD61830)
LM212	48 × 640	270 × 63 × 14 max.	
LM215	128 × 480	270 × 110 × 15 max.	External CB1030R (HD61830)

Note: Character displays also available in 1-line, 2-line and 4-line series.

HITACHI

For more information:
Hitachi America, Ltd. **Chicago Office** 500 Park Boulevard, Suite 805, Itasca, Ill. 60143 Tel: (312) 773-0700 Telex: TWX910 651 3105 (HITACHI ITAS)
San Jose Office 1800 Bering Drive, San Jose, Calif. 95112 Tel: (408) 292-6404 Telex: WU171581, TWX910 338 2103 (HITACHI SNJ)

CIRCLE 183

COMPUTER SYSTEMS

Graphics workstation has 32-bit virtual μP

The PowerStation 5000, based on the Unix operating system, contains a 32-bit virtual application processor and a graphics processor for CAD/CAE applications. Each workstation can communicate with a PowerNode in the network or, when operating as a stand-alone, handle complex drafting applications, three-dimensional mechanical design, and numerical control. The graphics subsystem, which includes a 19-in. color monitor, a keyboard, and a mouse, is capable of displaying both color and monochrome video. In addition to the graphics subsystem, the PS5000 is configured with 2 Mbytes of main memory, 32 kbytes of cache memory, a cartridge tape, and an 80-Mbyte disk.

Gould Inc., Computer Systems Division, 6901 W. Sunrise Blvd., PO Box 9148, Ft. Lauderdale, Fla. 33310; (305) 587-2900. $99,000.

CIRCLE 340

Microcomputer utilizes J11-based LSI-11/73

The first member of the 8600 series of computer systems based on the LSI-11/73 processor, the Model 8650 is compatible with current LSI-11 and PDP-11 operating systems and application software with little or no modification. The incorporation of the KDJ11-AA microprocessor speeds processing time by as much as five-fold over LSI-11/23 processors, while remaining in the same price range. Moreover, it approximates the performance of the PDP-11/44. The Q-bus-based 8650 features a 41.6-Mbyte fixed/removable hard-disk drive, 256 kbytes of RAM (expandable to 4 Mbytes), and six serial RS-232-C ports.

Plessey Peripheral Systems Inc., Computer Systems Division, 17466 Daimler Ave., PO Box 19616, Irvine, Calif. 92714; (714) 540-9945.

CIRCLE 341


Hybrid Reliability
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Whether you're producing...computers...computer peripherals...telecommunications...medical equipment...terminals...office machines...or NC machine tools...Taiyo Yuden hybrid circuits are your best investment in reliability. Why? The reason is simple. In thick film hybrids, design, manufacturing and rigid testing is critical. Taiyo Yuden – with almost 50 years in electronics – is the international leader in hybrid circuit assembly. Whatever your requirements, our U.S.-based engineering staff will work with you to transform your hybrid design into a working product incorporating the latest in leading-edge technology, with the same high quality delivered the world over. And like the rest of our electronic components, they're available at very competitive prices. To find out more about Taiyo Yuden hybrids, write or call today:
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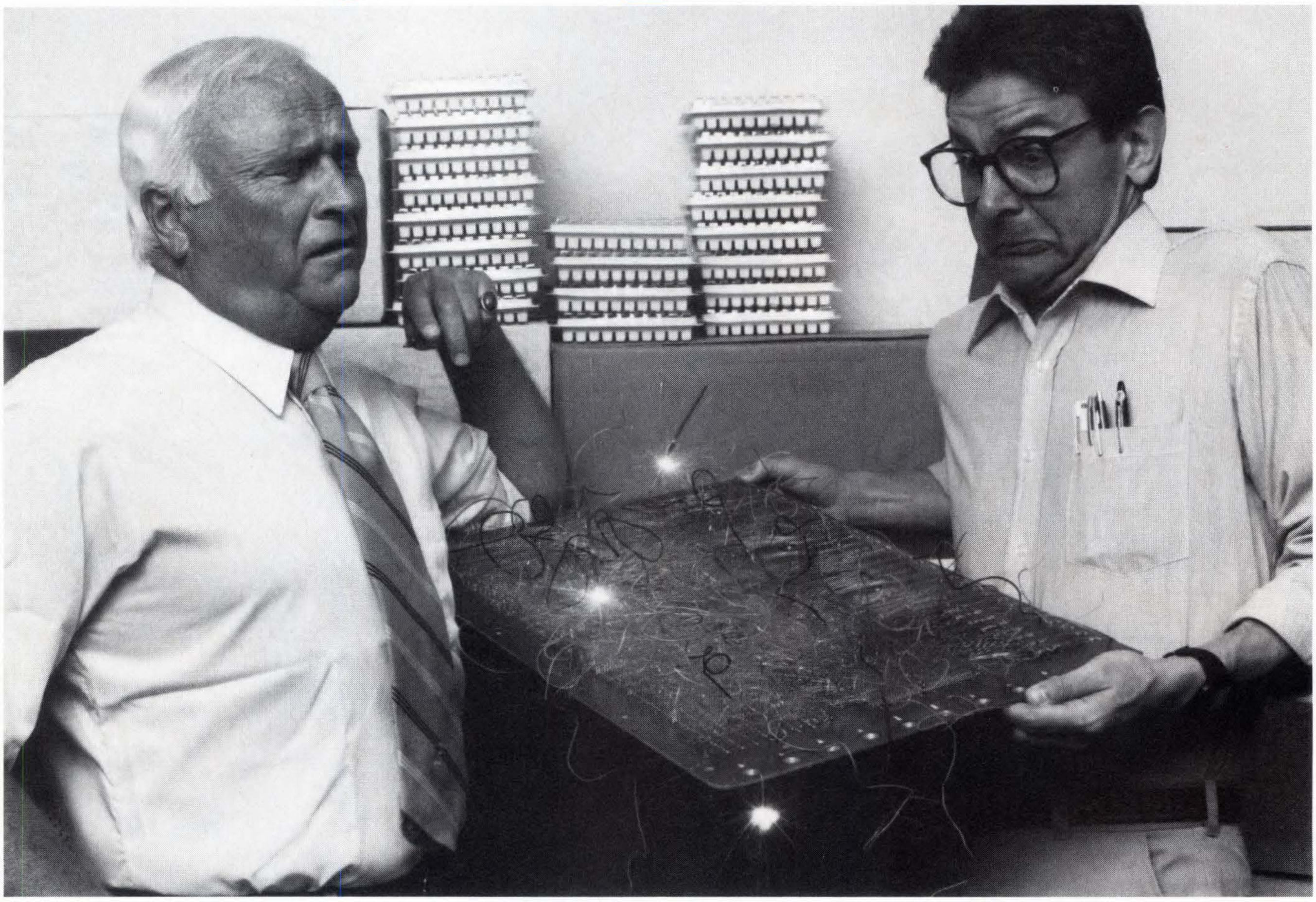
CIRCLE 185

Does your backplane vendor test the board? Or your patience?



SAE's complete test capabilities help give us total backplane packaging control.

It's impossible to get an untested backplane from SAE. We test the bare board, the backplane assembly less wire-wrap, and the backplane assembly with wire-wrap. We always perform a dynamic test to check the board, the connectors, the press-fit joints, and all contact-to-contact relationships.

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Our test consoles handle up to 16,000 points and virtually any interface requirements. We also maintain a test library to speed testing on large production runs.

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We meet MIL-C-28754 and C-28859 specifications and NAFI/NAC standards. We also build in accordance to MIL-C-21097 and MIL-C-55302. Quality control standards in all our facilities meet MIL-I-45208 requirements.

CIRCLE 186

SOFTWARE

Idris operating system runs on IBM PC

Designed to coexist with PC-DOS or MS-DOS, a version of the Idris operating system brings Unix look-alike capabilities to the IBM PC. Idris is substantially smaller than Unix and works in as little as 128 kbytes of main memory. The latest version, called Co-Idris, gives IBM PC users concurrent access to both Idris-based programs and PC-DOS- or MS-DOS-based application programs. In addition, given one or more asynchronous communications adapters, Co-Idris will support multiple users and/or networking with other systems. The operating system provides all the software necessary to construct C, Pascal, or assembly programs for operation under Co-Idris, DOS, or CP/M-86.

Whitesmiths Ltd., 97 Lowell Road, Concord, Mass. 01742; (617) 369-8499. $695.

CIRCLE 342

CAD program produces symbolic drawings

Claimed to speed the creation of schematic drawings, the MGI/Schematic Drafter program is designed for producing nondimensional symbolic drawings such as circuit diagrams, digital logic diagrams, electrical schematics, ladder diagrams, pc board layouts, and even project schedules. Letter-designated symbols are entered from the computer keyboard using a template guide and placed into the squares of a grid on the display screen. Most of the standard MGI/Template series contain 35 to 40 individual symbols, but the system can handle 52 symbols or more if required. Individual symbols may be rotated or mirrored to change the symbol's orientation within a cell on the computer screen. The program also allows panning across a drawing and has the ability to zoom in and out for different views.

Microcomputer Graphics Inc., 13468 Washington Blvd., Marina del Rey, Calif. 90292; (213) 822-5258. $3900.

CIRCLE 343

Software tool programs HP test instruments

Designed to simplify the development of software for Hewlett-Packard test instruments, Unitest can reduce the time necessary to develop and debug a measurement-intensive program by up to 75%. The program, which works with HP Series 200 computers, eliminates the need to understand the HP Basic protocol and syntax that is required in programming the HP-IB-based instruments.

Unitest is composed of a main program, the Unitest Executive, and individual packages for specific instruments. The executive organizes control-program writing into five menu-driven steps, which define the configuration, develop the control program, build the data files, define the instrument setups, and prepare the run. The Unitest Executive is priced at $3000, with prices for the instrument-specific software packages ranging from $750 to $1000 each.

Production Automation, 3160 De la Cruz Blvd., Santa Clara, Calif. 95050; (408) 980-9880.

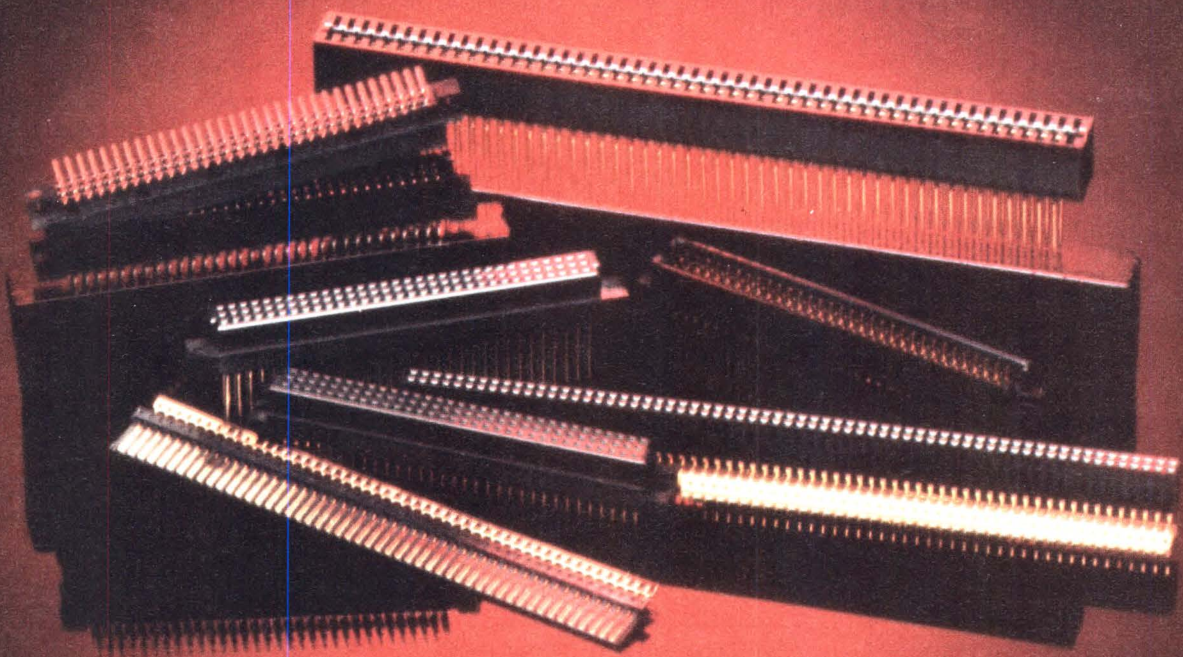
CIRCLE 344

Software performs equation solving

Varicalc, a versatile program for the Apple II series of microcomputers, interactively solves scientific, engineering, and business equations. Varicalc simulates complex physical, chemical, or mathematical processes, as well as accepts real-time inputs. Variables may be changed interactively by the use of "variators"—which can be two game paddles or a joystick, the left or right arrow keys, or an automated loop variator with selectable range and step size. The program solves any one of 19 variables on the right or left side of a formula without rearranging the formula. Up to 255 equations may be stored on disk for quick recall. IMI's Adalab data-acquisition card allows real-time analog voltage input and output for Varicalc equations and simulations.

Interactive Microware, Inc., PO Box 139, State College, Pa. 16804; (814) 238-8294. $100.

CIRCLE 345



DIGITAL ICs

64-kbit EEPROM offers choice of write times, number of storage cycles

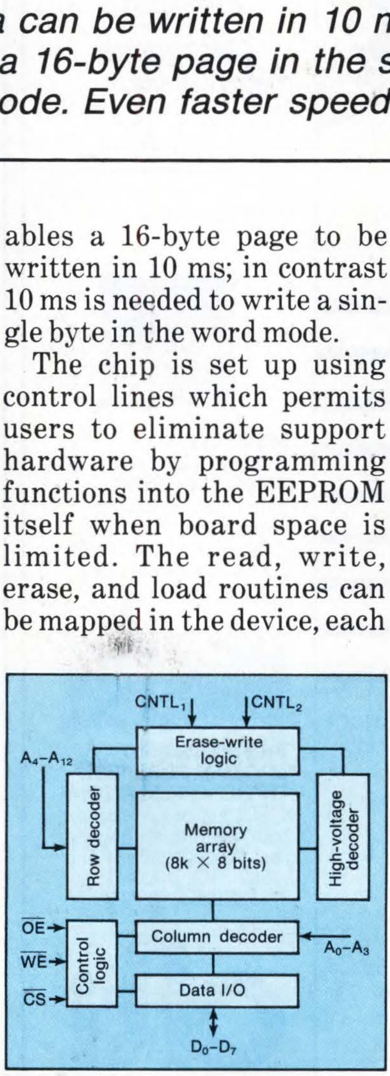
A byte of data can be written in 10 ns in the block mode and a 16-byte page in the same 10 ns in the page mode. Even faster speeds are possible.

The 52864 family of 64-kbit EEPROMs lets users select both the write times and the number of read and write cycles. The 5-V EEPROMs, from NCR, use nitrox storage cells, which allows many parameters that are fixed with other EEPROM technologies to be set and altered. The family comprises three members—the HR, a military part that will be the first produced, as well as industrial and commercial versions.

The devices are not self-timed. Thus data can be written in less than the 10 ms typically needed for that task. Information can be written in as little as 2 ms; however it will not remain in memory as long as that written at the standard speed. Refreshing it later will ensure that it is retained over the full term.

Another way in which writing speed can be slashed is to use the block mode. That enables a 16-byte page to be written in 10 ms; in contrast 10 ms is needed to write a single byte in the word mode.

The chip is set up using control lines which permits users to eliminate support hardware by programming functions into the EEPROM itself when board space is limited. The read, write, erase, and load routines can be mapped in the device, each taking up 8 kbits of memory.



The 52864, a group of 64-kbit EEPROMs allows the user to eliminate support hardware by using the control lines to map read, write, erase, and load routines into the device itself.

The chip's write and erase lifetime typically extends to 10,000 cycles, and data is retained for an average of 10 years. However, it is possible to change the number of cycles if needed. For example, the cycles can be increased to 100,000, but storage time drops to a year.

The commercial version can be accessed in 300 ns; the industrial and military versions, in 450 ns. All of the devices draw only 60 mA, and they can be had in 28-pin DIPs or 32-contact leadless chip carriers.

The HR will be available in production quantities in the winter. The DIP lists for $294 in lots of 100; the chip carrier costs $324 in the same quantities. The price is not yet set for the other devices, which will be sampled late in the year.

NCR Corp., Microelectronics Division, 8181 Byers Road, Miamisburg, Ohio 45342; (513) 866-7471 or (800) 543-5618. **CIRCLE 314**

Terry Costlow

DIGITAL ICs

8-bit multiplying DAC sports output op amp

An 8-bit CMOS multiplying digital-to-analog converter that delivers an output of 10 V, incorporates an output op amp, and needs no second power supply.

Analog Devices' AD7224 operates from a single supply of +15 V with a reference of +10 V or −5 V and +11.4 to +16.5 V (V_{DD}) with a reference of −4 to +2 V.

The chip's static or dc accuracy is specified as "total unadjusted error" (TUE), a relatively new term that is measured in least significant bits and covers full-scale error, relative accuracy, and offset error. With the single supply, the 7224 has a total unadjusted error of less than 2 LSBs; with split supplies, the total unadjusted error ranges from under 1 LSB for the L, C, and U versions to under 2 LSBs, for the K, B, and T versions.

Moreover, those specifications, as well as monotonicity, are guaranteed over the three separate temperature ranges (see the table).

The chip's maximum settling time for a positive full-scale change, which can be 10 V into a 2000-Ω load, is 5 μs with both single and split supplies. A similar negative swing settles in 7 μs with split supplies, 20 μs with one supply.

With its two sets of input registers, the converter easily interfaces with most microprocessors. Its logic speed is compatible with that of the 8088, 6502, Z80, and 68008. Housed in a 20-pin DIP, the converter's versions operate in commercial, industrial, or military temperature ranges.

Analog Devices Inc., Semiconductor Division, 804 Wilburn St., Wilmington, Mass. 01887; Gerry Whitmore, (617) 935-5565. **CIRCLE 301**

COMPUTER PERIPHERALS

Disk controller chip holds data buffers

Hitachi's HD63463 single-chip hard-disk controller contains a pair of 256-byte data buffers that can be accessed separately or simultaneously by the host processor and the disk driver, an arrangement that completely decouples data transfers. The CMOS chip can be programmed for formats of up to 1024 cylinders per drive and for sectors ranging in length from 256 bytes to 4 kbytes.

A built-in set of 21 high-level commands bestows enough intelligence on the chip to minimize the usual amount of host control software. The disk controller circuit can work with both the Seagate and the SMD standard, as well as with MFM and NRZ encoding.

On-chip circuitry includes a programmable generator and checker of 16-bit cyclic redundancy code, plus a 32-bit ECC (error correction code) circuit that catches and corrects burst errors that can be as large as 11 bits.

The HD63463 controller is optimized for applications using the 68000 microprocessor and the 68450 DMA controller. Versions of the chip operate at a 4, 6, or 8 MHz clock frequency from a 5-V supply. A 48-pin DIP affords the necessary lines for the 16-bit bus interface. The chip does, however, work in a control mode that allows it to tie into an 8-bit processor bus.

Samples of the HD63463 will be released in the fall at a price of $75 in 100-unit quantities.

Hitachi America Ltd., 1800 Bering Drive, San Jose, Calif. 95112; Tony Moroyan, (408) 292-6404. **CIRCLE 301**

16k EEPROM accesses in less than 200 ns

Compatible with fast microprocessor applications, the NMC9817 16k EEPROM performs a read operation in less than 200 ns. The fast read time results from a built-in two-line control architecture that eliminates bus contention in systems environments. Onboard address and data latches free the microprocessor during erase/write cycles. When using an automatic erase-before-write procedure, combined with a chip-erase mode, users can save up to 50% of the time required for the erase/write cycle. The EEPROM's fast operation is exemplified by its 5-ms write cycle and 10-ms erase/write cycle.

The 28-pin ceramic DIP interfaces directly with standard microprocessors, without external support components. Since the NMC9817 is self-timing, the processor is free to perform other tasks during a programming cycle until the memory signals it is ready. This signal can also be used to interrupt the processor when the device goes from busy to ready.

National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051; (408) 721-5000. $30 (1000 units); stock. **CIRCLE 410**

Peripheral driver is fault-protected

The latest addition to the DS3658 quad driver family, the DS3668 has a current-sensing ability that permits individual outputs to be shutdown when a short-circuit condition is detected. Unlike thermal shutdown, which shuts down all the outputs at once and totally disables the device, the use of current-sensing circuits on each output shuts down the affected output only and leaves the remaining three channels operational. In addition, should an input line be broken or go open, the peripheral driver will go into a high-impedance state and prevent any invalid signals from appearing at the outputs.

The quad driver is capable of sinking 600 mA at each output (2.4 A per package) and providing an output breakdown voltage of 70 V. It is well suited for driving relays, solenoids, and disk-drive stepping motors.

National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, Calif. 95051; (408) 721-5000. $5.40 (100 units). **CIRCLE 411**

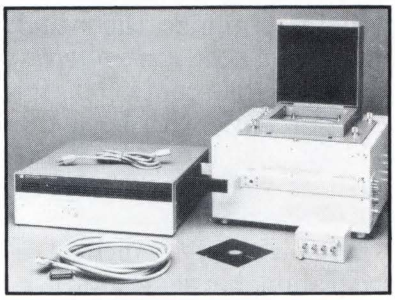
INSTRUMENTS

Sensitive switch matrix handles 48 pins

Switching low-level signals between 48 pins of a device under test, the HP 4085M matrix also permits currents as low as 1 pA and voltages of just 1 mV to be measured. The system developed by Hewlett-Packard consists of a switching matrix controller and a mechanical switching matrix of dry-contact relays.

The matrix has eight input ports, any of which can be connected to any of the 48 output lines, under program control.

The software for the switching matrix includes high-level commands for port assignments and for diagnostics. Interconnection status can be viewed on the CRT screen of a computer, such as the HP 9000 model 216S, serving as a system controller. To tie into the controller, the switching matrix uses an IEEE-488 interface and a Basic language operating system.



Guaranteed signal frequencies range from dc to 1 MHz, but the matrix works at frequencies of up to 5 MHz. Signal swings can span ±100 V, with a maximum current of 100 mA. Both maximums cannot occur simultaneously, however—the power per I/O line is limited to 2 W.

Three test fixture adapters are included with the HP 4085—the HP 16078A for use with the HP 4145A semiconductor parameter analyzer, the HP 16066A to handle packaged devices or circuits, and the HP 16075A relay test adapter for diagnostics.

The switching matrix and controller pair cost $34,109, with delivery in about eight weeks.

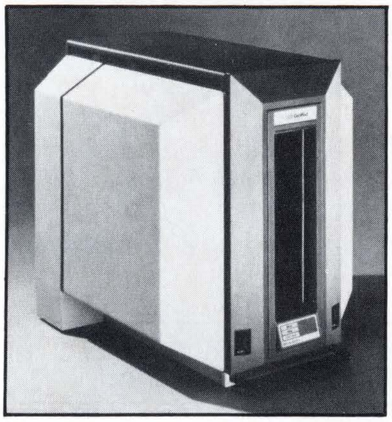
Hewlett-Packard Co., Inquiries Manager, 1820 Embarcadero Road, Palo Alto, Calif. 94303; call local HP sales office. **CIRCLE 310**

Fixture set tests SMD-fitted boards

A fixture system allows test nodes to be accessed on double-sided printed circuit boards. The Micro-Mate system from GenRad probes devices with 40-, 50-, and 100-mil centerline spacing, such as the surface-mounted devices that are becoming increasingly popular.

The fixture is designed for simple and heavy-duty use in a production environment. A circuit board is pulled into the fixtures base with a pneumatic cylinder.

The testing system consists of a universal base unit, board carriers (one for each pc board family), and a pair of probe plates drilled and wired for each variety of board under test. Any combination of boards measuring up to 9 by 12 in. can be accommocan be accommodated.

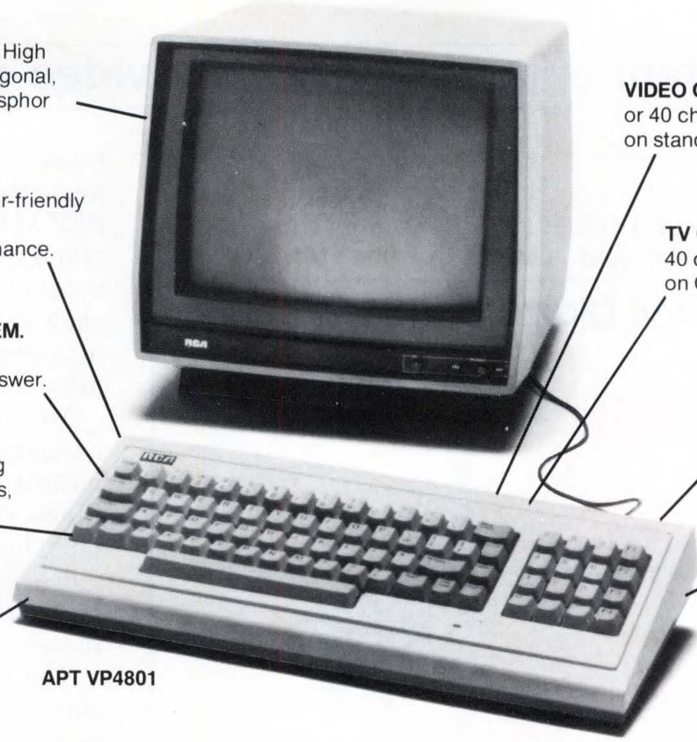


Both probe plates can be accessed for debugging by means of hinged probe plate covers.

The prices are $28,000 for the base unit, $400 for each board carrier, and an average price of $5000 for each set of fully wired probe plates, based on 500 nodes.

GenRad Inc., 300 Baker Ave., Concord, Mass. 01742; (617) 269-4400. **CIRCLE 319**

You don't need a computer to talk to another computer.



APT VP4801

The new RCA APT (All Purpose Terminal) expands your data communications capabilities for a lot less money.

For business, professional and personal data communications, you'll find more user-friendly features and greater communications capabilities in the RCA APT than in other terminals selling for up to three times the price.

The new APT terminals are ideally suited to multi-data base time sharing and dedicated, direct computer-connected applications. They feature menu-controlled operation and a programmable "personality" to match specific communications requirements for your data bases.

A single keypress can dial a stored number, send the log-on sequence on the host computer, and return terminal control to the user. Password protection prevents unauthorized access to designated numbers. APT can also be used as an auto-dialer for voice communications.

Quite simply, matching features with price, there is no other professional quality terminal available today that can do as much at such low cost.

APT terminals list for $498, in your choice of full stroke or membrane keyboard versions. Either style is also available with a display monitor for $697 list. The data display monitor alone, VP3012D, $199 list.

For more information—or to order—call 800-722-0094. In Penna., call 717-295-6922. Or write for fully descriptive brochure to RCA Data Communications Products, New Holland Avenue, Lancaster, PA 17604. OEM and dealer pricing available. The new RCA APT. Expansive. Not expensive.

OTHER FEATURES

RS232C port for direct computer connections at data rates to 9600 baud, or for connecting high speed modems and other accessories. Parallel printer port for hard copy. Numeric keypad, can dial phone numbers not in terminal directory. Built-in speaker with adjustable volume control for audio monitoring of phone line. Smooth scroll display. Automatic screen blanking to reduce possibility of burn. Briefcase size: 17" x 7" x 2". Weight: under 4 lbs.

APT VP3801. Flexible membrane keyboard version designed for travel and hostile environments.

RCA

CIRCLE 207

INSTRUMENTS

System enhancement tests video chips

The VG600 video generator, designed for LTX's CX80 and TS88 master test stations, tests and characterizes video processor chips. Within its 16 kbytes of line (or event) memory, the generator box stores the patterns necessary to test chips according to NTSC, PAL, SECAM, and other broadcast standards. Alternatively, two test heads can test two chips, each using 8 kbytes. Control matters are handled in another 16 kbytes of memory.

Memory looping takes full advantage of the repetitious nature of video test patterns. Since relatively few values must be changed for each new video line, test patterns can be generated substantially faster.

The variable line length of the VG600 makes it possible to place line boundaries anywhere within the pattern, enabling users to simulate line jitter. Through global line substitution, users can change all occurrences of a line—for example, changing all chroma bursts to no bursts for testing a color-kill function. Another substitution lets the user replace one set of lines with another.

The VG600 can collect about 256 samples of data per pass of the test pattern, thereby thoroughly testing any video processor chip, even in a high-volume production environment where time is at a premium.

The VG600 fits into the CX80 consumer extension for LTX's Model 77 integrated test system. The VG600 generator will be available next month at a price of $45,000.

LTX Corp., LTX Park at University Ave., Westwood, Mass. (617) 329-7550.

CIRCLE 316

ANALOG

Op amp increases gain, reduces offset voltage and lowers noise

Op amp achieves usable open-loop gain of 8 million and holds down errors due to noise, offset, and drift.

Signals that have been too small to reach using conventional op amps can now be put to use by means of an operational amplifier with an open-loop-gain of 8 million. With that gain, engineers can now use the full sensitivity of instrument sensors such as temperature and pressure gauges.

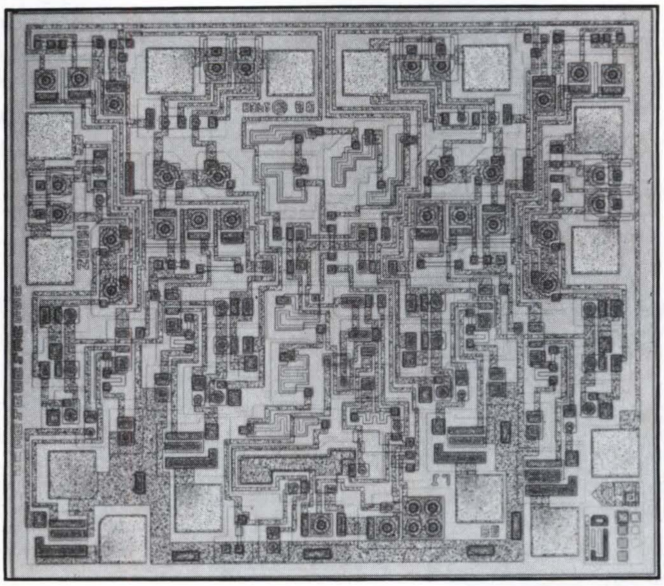
To match its high gain, the op amp achieves an important low noise level of 4.0 $nV/\sqrt{Hz}$ at a 10-Hz frequency. The low offset voltage of 30 μV maximum makes for easy connection to transducers and sensors, and the low offset drift of 0.3 μV/°C serves the part well when used in harsh environments.

The op amp is stable for closed-loop gains above 50. Its typical output, 10 mA, nicely fills the drive requirements of most LEDs. Load impedances down to 50 Ω can be driven by the output stage when its power pins are set to ±5 V; with a separate set of power supply pins, output current can reach ±60 mA. A minimum slew-rate of 2.5 V/μs allows levels to change quickly.

The part may be operated from a single supply such as 15 or 28 V. Additional op amp specifications include an input bias current of ±1 nA and a common-mode rejection ratio of 126 dB.

The part comes in a plastic or ceramic dual inline package and is available off the shelf in MIL-STD-833 as well as industrial grade specifications. Prices range from $2.95 for the least expensive industrial grade to $9.38 for the 883 military version with burn-in.

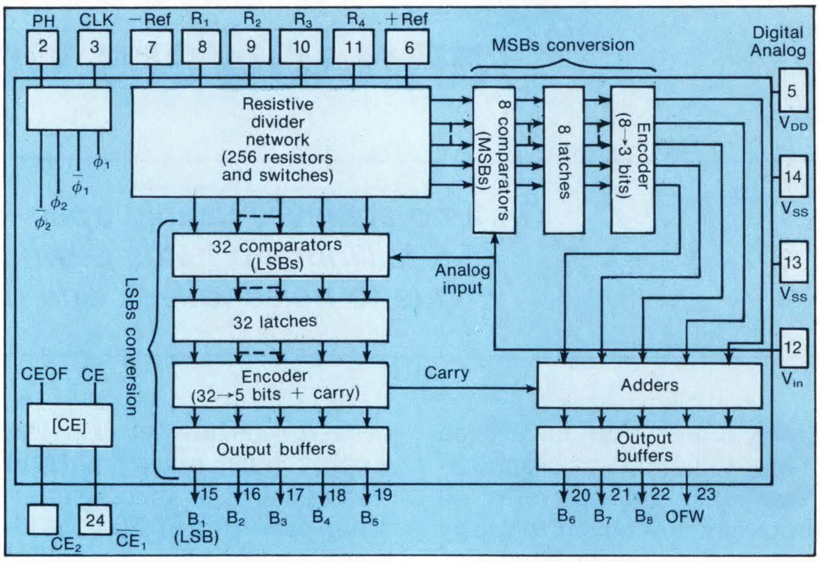
Precision Monolithics Inc., 1500 Space Park Drive, Santa Clara, Calif. 95050; (408) 727-9222. **CIRCLE 308**



Curtis Panasuk

ANALOG

CMOS flash converter digitizes 8 bits in 200 ns



The MP7683 8-bit flash converter converts in two steps. The 3 MSBs are digitized first using 8 comparators, the 5 LSBs next using 32 comparators. That technique affords conversion time of 200 ns.

A CMOS analog-to-digital flash converter from Micro Power can execute an 8-bit conversion in 200 ns while consuming just 150 mW. The MP7683 has an Overflow bit (OFW) that lets two devices be cascaded for 9-bit resolution; operating in parallel, the two chips can digitize data at 10 MHz.

The 8-bit converter is a two-step flash converter, with the first step converting the 3 MSBs using 8 autobalanced comparators and the second step operating on the 5 LSBs using 32 autobalanced comparators (see the figure). A 6-bit version, the MP7682's has a 100-ns conversion time which is attributed to its single-step architecture, using 64 autobalanced comparators.

Both chips need supply voltages ranging from 3 to 8 V. The 5-V supply affords TTL compatibility.

The converters operate over the industrial temperature range (−25° to +85°C). In quantities of 100, the MP7683 sells for $90 apiece in a 24-pin ceramic DIP, the MP7682 for $48.50 apiece in an 18-pin ceramic DIP. Both parts are available screened to MIL-STD-833. Delivery is from stock.

Micro Power Systems Inc., 3100 Alfred St., Santa Clara, Calif. 95050; (408) 727-5350.

Curtis Panasuk

CIRCLE 312

ANALOG

Family of 8-bit ADCs digitizes in 73 μs

Five 8-bit successive-approximation a-d converters, the ADC0801-1 series, offer conversion times of 73 μs and have TTL- and MOS-compatible inputs and outputs. The devices, which operate at a 1-MHz clock frequency, are available with total error specifications ranging from ±1/4 to ±1 LSB. The CMOS converters contain an on-chip clock generator and feature differential inputs for good common-mode signal rejection. The ADC0801-1 series may be operated in a ratiometric mode, where power supply variations equally affect both ADC inputs and outputs. The converters come in 20-pin plastic or ceramic DIPs and require a single +5-V supply. A power consumption of only 15 mW makes them suitable for portable applications.

Signetics Corp., Linear LSI Division, 811 E. Arques Ave., PO Box 409, Sunnyvale, Calif. 94086; (408) 739-7700. From $5 to $50 (100 units).

CIRCLE 346

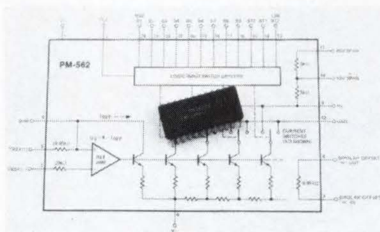
V-f converter has 0.005% nonlinearity

Designed for analytical instrumentation requiring analog-to-digital conversions of 20 to 24 bits, the Model 8120 voltage-to-frequency converter has a maximum nonlinearity of 0.005% over the entire dc-to-100-kHz output range. The gain temperature coefficient of the device is typically 5 ppm/°C, with a typical offset temperature coefficient of 4 μV/°C. A maximum input offset voltage of 7 mV corresponds with the 8120's signal range of −10 μV to −10 V. The 2-by-2-by-0.5-in. module is specified for operation over the temperature range of 0° to +70°C.

Dynamic Measurements Corp., 8 Lowell Ave., Winchester, Mass. 01890; (800) 225-1151 or (617) 729-7870. $143 (100 units); two weeks.

CIRCLE 347

12-bit DAC requires no laser trimming



The PM-562 is a 12-bit multiplying d-a converter that fits directly into the industry-standard AD562 socket and requires no laser trimming. Other advantages over existing designs include lower power dissipation, higher voltage compliance, greater output impedance, lower zero-scale error, and lower gain drift.

At 130 mW of dissipation, the PM-562 consumes 65% less power than the AD562. The converter also offers a high output resistance of 2 MΩ. Zener-zap trimming of the most significant bit achieves reliable 13-bit accuracy, as well as long-term stability. Full-scale settling to within ±1/2 LSB takes 1.5 μs. Suitable for military applications where the gain temperature coefficient is critical, the PM-562 has a typical gain drift of 1 LSB over the full operating temperature range.

Precision Monolithic Inc., 1500 Space Park Drive, Santa Clara, Calif. 95050; (408) 727-9222. From $12 (commercial grade) to $95 (military grade) (100 units); 6 to 12 weeks.

CIRCLE 348

Instrument amp sports four op amps

The INA258/MIL series of military-grade monolithic instrumentation amplifiers uses a basic three-amplifier design and includes an independent fourth op amp on the chip. Specified separately, the fourth op amp can be used for additional functions, including single-capacitor active low-pass filtering, output level shifting, or to achieve higher gains—as much as 10,000 V/V. The fourth amplifier in the INA258 package is also helpful when board space is limited. Offset voltage is ±50 μV, with a linearity error of less than 0.002% for all of the grades in the family. The series is offered in either an 18-pin ceramic side-brazed DIP or in a 20-terminal leadless chip carrier.

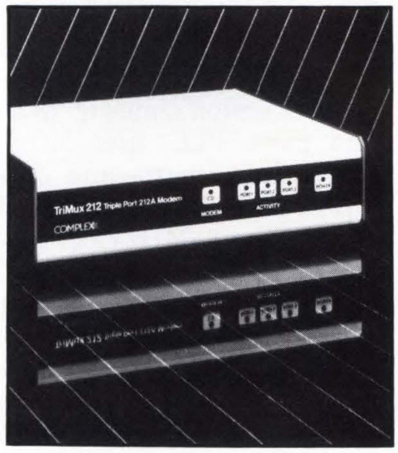
Burr-Brown Corp., International Airport Industrial Park, PO Box 11400, Tucson, Ariz. 85734; (602) 746-1111.

CIRCLE 349

COMMUNICATIONS

Triple-port modem saves phone lines

One modem permits three devices to transmit data simultaneously, saving not only additional modems, but the cost of possible long-distance lines. The TriMux.212 from Complexx Systems Inc. combines a statistical multiplexer with an automatic dialing and answering Bell 212A modem. In a menu-driven operation, a user can automatically dial one of four stored numbers with a one-digit cue and access the desired device at a remote site.



Speeds of 50 to 9600 bps are supported. An additional RS-232-C output accommodates external synchronous modems at up to 9600 bps, and differing data rates can be converted between two devices.

For reliability, the TriMux.212 automatically retransmits in case of line errors. Password security ensures against unauthorized use. Further, a back panel switch will completely disable the command mode.

The TriMux.212 costs $1495 in single-unit quantities and is available now.

Complexx Systems Inc., 4930 Research Drive, Huntsville, Ala. 35805; Rick German, (205) 830-4310.

CIRCLE 305

COMMUNICATIONS

Two-line telephone has integral modem

Compatible with all RS-232-C terminals and computers, the Tel-A-Modem is an intelligent modem device integrated into a two-line desk-type telephone. Modem coupling on either line is accomplished by pressing a button on the telephone's keypad, which leaves the telephone handset free for voice communication on the remaining line. The modem is capable of full-duplex transmissions at 300 and 1200 baud. Five LEDs on the unit's faceplate indicate modem status. Special features include the option of selecting tone or pulse dialing functions—particularly useful in accessing long-distance call systems in areas where touch-tone dialing is unavailable. The power supply outlet of the Tel-A-Modem plugs directly into a wall outlet without the need for a special adapter.

Code-A-Phone Corp., PO Box 5656, Portland, Ore. 97228; (503) 655-8940. $695.95. **CIRCLE 350**

Signal indicator monitors Ethernet LAN

Small enough to fit in a pocket, an Ethernet transceiver/MAU (medium access unit) signal indicator aids in troubleshooting Ethernet and IEEE 802.3 local area networks. The Model A0007-ETSI has four LEDs—one each for power, transmission, collision, and receiving signals—that continuously indicate the status of the network. The indicator has a 15-pin female subminiature D connector with a slide lock on one end and a male subminiature D with locking posts on the other, which allow the 4-by-1.5-by-0.9-in. device to be inserted in series with the transceiver/MAU cable.

TCL Inc., 41829 Albrae St., Fremont, Calif. 94538; (415) 657-3800. $149.95 (OEM discounts available). **CIRCLE 351**

Two-chip set reduces FM receiver costs

Two chip sets offer designers a choice of components for implementing data or voice and data FM receiver designs. Configured as sets, rather than as single chips, they cost-effectively optimize performance and flexibility.

The S404/406 chip set forms the basis for low-power, high-sensitivity voice and data FM radio receivers. Designed for use in double-conversion superheterodyne receivers, the S404 mixer converts a 21.4-MHz first i-f to a 455-kHz second i-f. An auxiliary rf amplifier stage on the S404 allows it to operate as the front end of a single-conversion, high-frequency receiver operating at up to 50 MHz.

The S408/410 chip set utilizes a direct conversion approach for FM data receivers. Input to the system is FSK modulated FM up to 200 MHz, with a sensitivity of 0.5 μV. The modulated rf is directed into two channels where it is mixed in quadrature with the carrier frequency generated by a local oscillator. The output data stream is in NRZ format.

Siltronics Ltd., 436 Hazeldean Road, Kanata, Ont., Canada K2L 1T9; (613) 836-5003. **CIRCLE 352**

T1 multiplexer enhances network control

The Model 6240, a high-speed time-division multiplexer, optimizes the integration of voice, data, and digital-image transmissions over a single link. Unlike most T1 multiplexers, which offer little or no flexibility for reconfiguration of the voice/data traffic from the central site, the 6240 enables the operator to define network parameters (such as digitization rates) and reallocate aggregate bandwidth to priority applications' traffic requirements—all from the central site.

The multiplexer is available in 16-, 32-, 48-, and 64-channel versions and will accommodate any mix of voice and data. Transmission rates are from 56 kbits/s to 2.048 Mbits/s. System configuration is stored in local and remote multiplexer memory and is protected by battery-backup in the event of an external power failure.

Codex Corp., 20 Cabot Blvd., Mansfield, Mass. 02048; (617) 364-2000. From $14,000; fourth quarter. **CIRCLE 353**

COMPUTER PERIPHERALS

Unit offers IBM PC fixed/removable storage

The VRC 81 PC disk subsystem offers the IBM PC (with PC-DOS 2.0 or higher) a fixed/removable 8-in. disk drive with a total formatted data capacity of 21.4 Mbytes —10.7 Mbytes on the fixed disk and 10.7 Mbytes on a removable cartridge. A single data cartridge for the VRC 81 PC holds the equivalent of 60 floppy disks and eliminates the inconvenience of swapping disks for complex tasks. Further, all 10.7 Mbytes can be backed up in about one minute, an operation that would take approximately 60 minutes using floppy disks. The subsystem, which is suitable for standalone or rack-mounted use, includes a power supply, all necessary drive electronics, an SCSI controller, an interconnecting cable, and a host adapter for the IBM PC.

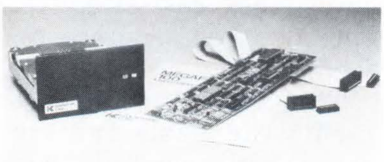
Vermont Research Corp., Precision Park, North Springfield, Vt. 05150; (802) 886-2256. **CIRCLE 354**

Streamer handles multiple formats

Available in both vertical-mounted and horizontal drawer-mounted configurations, a nine-track streaming tape drive handles a variety of formats, including 800 char/in. NRZI, IBM, and ANSI; 1600 char/in. PE, IBM, and ANSI; and dual-density 3200/1600 char/in. for interchange-compatibility between computers of any manufacture. Designated the PCT-1000, it provides 138 Mbytes of backup for Winchester disks drives and read/write access to archival data banks, as well as data interchange between computers. To cut costs and increase reliability, the PCT-1000 incorporates two microprocessors and a real-time operating system to control tape motion, eliminating the use of swing arms and capstan motors. The streamer is compatible with the standard Cipher/Pertec interface.

Ibex Computer Corp., 20741 Marilla St., Chatsworth, Calif. 91311; (818) 709-8100. Approximately $2256 (100 units), depending on the number of formats specified. **CIRCLE 355**

Hard-disk system sells for $895



The low cost of the Megaflight 100 hard-disk system is aimed at making hard-disk storage a viable option for a broader range of personal computer users. Priced at $895, the storage system is fully compatible with IBM PC and PC XT, Compaq, Leading Edge, Corona PC and Corona Portable, Eagle PC and Eagle Spirit, and other IBM-compatible computers. The Megaflight 100 system includes a hard-disk drive unit with a storage capacity of 12.76 Mbytes unformatted and 10 Mbytes formatted, plus a disk-controller card with plugs and cables. It uses DOS 2.0 or 2.1 software drivers and typically requires no external power supply.

Kamerman Labs, 7787 SW Cirrus Drive, Beaverton, Ore. 97005; (800) 522-2237 or (503) 626-6877. **CIRCLE 356**

Dot-matrix printers are IBM PC-compatible

Comprised of two models, a series of single and multicolor dot-matrix printers is compatible with the IBM PC. At the low end is the 7500E, an 80-column printer with a throughput rate of 105 char/s and 45 lines/min. At the high end, the 8510SCE/1550SCE is an IBM PC-compatible version of the two-speed, seven-color 8510SC/1550SC printer. The SCE model offers 120-char/s printing of multicolor graphics and 180-char/s printing of rough drafts and lists. At 120 char/s, the throughput speed is 70 lines/min. The basic difference between the 8510 and the 1550 is the carriage width. The latter's 136-char/line format accepts forms 4.5 to 15.5 in. wide, while the former's 80-char/line format accepts forms that are 4.5 to 10 in. wide. Both parallel and RS-232-C interfaces are available.

C. Itoh Electronics Inc., 5301 Beethoven St., Los Angeles, Calif. 90066; (213) 306-6700. $450 (7500E), $940 (8510SCE), and $1270 (1550SCE). **CIRCLE 357**

COMPUTER PERIPHERALS

Dot-matrix printer produces seven colors

As many as seven colors may be produced with the JX-80 dot-matrix printer, at speeds up to 160 char/s. The printer uses a four-color ribbon, which prints in black, yellow, magenta, and cyan by shifting to the appropriate track. Three additional colors—violet, orange, and green—are produced by having the printer make a second pass over one of the four basic colors. The JX-80's dot-addressable graphics capability, which has the same scale vertically as horizontally (a 1:1 ratio), enables it to produce accurate graphics, including true circles. It has a Centronics-type parallel interface, with RS-232-C and IEEE-488 interfaces available as options.

Epson America Inc., 23530 Hawthorne Blvd., Torrance, Calif. 90505; (213) 373-9511. $800. **CIRCLE 358**

Smart interface boards revitalize printers

Intelligent interface boards, which install in the printer and not in the computer, bring the capabilities of the latest daisy-wheel printers to Diablo Hytype I and Hytype II, DEC LQP-01, and Xerox printers. The Printerface Models DT150 and DT151A snap into place without any modifications to the printer and offer all the standard interface configurations—including RS-232-C, Centronics parallel, IEEE-488, and current loop. Once installed, the Printerface enables the printer to perform automatic bidirectional printing, microspacing, proportional spacing, bold facing, automatic centering, and variable pitch. Furthermore, the boards have self-testing and debugging capabilities.

Kuzara International, 7770 Vickers St., Suite 105, San Diego, Calif. 92111; (619) 569-9107. **CIRCLE 359**

COMPUTER PERIPHERALS

Smart input device works with IBM PC

Designed for use with IBM PC and PC-compatible computers, the Penpad 320 combines the capabilities of a keyboard, a mouse, a touch screen or pad, and a graphics tablet into one easy-to-use input tool. The intelligent peripheral consists of an add-in pc board, which occupies a single slot in the computer, and a graphics tablet and pen that is attached via cable. In the keyboard mode, Penpad identifies handprinted characters and transmits them to the computer. Corrections are made by simply printing over the desired character. Cursor control codes are transmitted based on pen motion. The digitizer mode offers a resolution of 200 points/in. In addition, Penpad can replace function keys or special-purpose keys through the use of macrosequences defined to the host software.

Pencept Inc., 39 Green St., Waltham, Mass. 02154; (617) 893-6390. $995. **CIRCLE 360**

Digitizer produces 1000 lines/in.

Operated with either a pen stylus or a multibutton cursor, the 9100 series digitizer produces a resolution of 1000 lines/in. and is accurate to within ±0.005 in. The basic system includes a tablet (with all the processing electronics and supporting firmware), an interface card, a transducer, and a power supply. The standard opaque tablet surface comes in three sizes, with active digitizing areas of 24 by 36 in., 36 by 48 in., and 44 by 60 in. The digitizer provides temporary storage of up to 1000 coordinate pairs in ASCII format and permits user-definition of output formats.

Calcomp, 2411 W. La Palma Ave., Anaheim, Calif. 92801; (714) 821-2142.

CIRCLE 361

FACTORY AUTOMATION

Motion controller is application-matched

The MPC/Control, a microprocessor-based motion controller, is manufactured from an inventory of hardware and software building blocks, which are combined to match the requirements of the machine or process being automated. It is useful for applications requiring precise control of velocity, point-to-point positioning with linear interpolation, or electronic synchronization and gearing.

Each unit can be configured to control up to four axes, or expanded to up to 16 axes, and contains a dc servo drive for each axis. The controller is programmable via the front panel by using the supplied MCL programming language. Customized programming for specific applications is also available. The MPC/Control comes in a standard 19-in. rack mount or in a variety of NEMA-type enclosures.

Creonics Inc., 85 Mechanic St., Lebanon, N.H. 03766; (603) 448-6300.

CIRCLE 362

8-channel unit converts analog to RS-232-C

An eight-channel industrial scanner, Octapak connects to a host computer's RS-232-C port to act as a scanning digital voltmeter for local or remote process applications. All eight analog channels are configurable for standard dc voltage or current inputs, as well as for any combination of RTD, thermocouple, ac, frequency, or potentiometric sensor inputs. Up to 16 scanners may be linked together to provide a maximum of 128 monitored points.

For data-logging and chart-recording functions, the Octapak is available with Octasoft, a menu-driven software program that is compatible with Apple II and IBM personal computers, as well as the A-Pac industrial microcomputer. Octasoft enables real-time bar graphs to be displayed on a CRT and chart recording on a printer from any selected channel.

Action Instruments Inc., 8601 Aero Drive, San Diego, Calif. 92123; (619) 279-5726. $495 (standard dc inputs).

CIRCLE 363

Robotic turret head has multiple end effectors

Designed for installation on precision assembly robots, FlexiGrip is a single-axis, multiposition turret head with dedicated positions for multiple end effectors. Attached to the MiniSembler 2000 four-axis assembly robot, it allows the robot to pick up, position, and place standard and special components in one cycle—without disruptive tool changing. Grippers mounted to the turret head are rotationally exchanged in seconds, while maintaining accuracy and repeatability to within ±0.001 in.

The FlexiGrip unit is electrically controlled by self-contained motor drives; the gripper and vacuum-type end effectors are controlled pneumatically. When attached to a robot arm, FlexiGrip can be rotated ±360° about the arm's zero axis. The head's force-sense feedback is used to program stress levels for each of the four end-effector positions.

Control Automation Inc., Princeton-Windsor Industrial Park, PO Box 2304, Princeton, N.J. 08540; (609) 799-7743.

CIRCLE 364

Gas flow controller needs no calibration

The MFC 280 mass-flow controller accommodates gases used in the processing of silicon wafers, without the need for time-consuming physical recalibration as gases are changed. The controller is internally programmed to handle gases with known conversion factors between 0.50 and 1.45. It may also be specified to accommodate gases with conversion factors of less than 0.50. A bypass design permits consistent output of gas flow, ranging from 0 cm^3/min to 30 litres/min. The MFC 280 has a first-order response time of 500 ms and follows command rates, including step functions, without overshooting—regardless of gas properties or pressures.

Tylan Corp., 23301 S. Wilmington Ave., Carson, Calif. 90745; (213) 518-3610.

CIRCLE 365

FACTORY AUTOMATION

Liquid-level sensor sends ultrasonic signal

Used for the continuous measurement of liquid levels, the Sensall Model 840 transmits an ultrasonic beam from the bottom of a liquid to the surface and reads the reflection from the liquid-air interface to compute the level. An ultrasonic sensor, which is mounted at the bottom of a sight glass, tube, or vessel, measures the liquid above it over a range of 2 to 50 in. It operates in temperatures ranging from −40° to +300°F and in pressures from 850 psig to complete vacuum. The sensor is connected to a remote electronic transmitter mounted in a NEMA 4 enclosure. The transmitter, which produces and processes the pulsed ultrasonic signal, uses a digital display to indicate the liquid level. An isolated 4-to-20-mA output signal and two relay set-points are used for controlling the process liquid.

Xertec Corp., National Sonics Division, 250 Marcus Blvd., Hauppauge, N.Y. 11787; (516) 273-6600.

CIRCLE 366

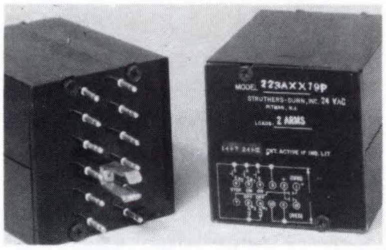
On-board Basic suits process control

Eliminating the need for most assembly language programming, a multifunction STD bus card comes with an on-board version of Basic that is optimized for process control and robotics applications. The Omnicard is both a development system and a complete control system. It is programmable in CAMBasic and, since assembly programming is not required, reduces software development costs by factors of 10 to 20. Program development requires a CRT terminal or a personal computer and a 5-V power supply. Its 43 I/O lines include eight analog input, one analog output, 24 TTL I/O, eight high-current drivers, one interrupt input, and one reset input.

Octagon Systems Corp., 6901 W. 91st Ave., Westminster, Colo. 80030; (303) 426-8540. From $575; stock to two weeks.

CIRCLE 367

Valve-control module replaces relays



Replacing combinations of electromechanical relays, contactors, and/or solid-state devices, a single CMOS valve control module (VCM) plugs into a 12-pin socket for reliable valve automation in industrial environments. The type 222 (dc output) and 223 (ac output) VCMs contain all the necessary control logic to open/close a valve or to operate/reverse other controlled devices in response to input signals. An electronic interlock feature is available that ensures valve actuation in only one direction. The valve control modules accept inputs from electromechanical relays or optoisolated SSRs from any number of remote-sensing devices, and they can power either electromechanical or solid-state load-handling devices.

Struthers-Dunn Inc., Lambs Road, Pitman, N.J. 08071; (609) 589-7500.

CIRCLE 368

Vision sensors give industrial robots sight

Designed for a variety of industrial applications, a range of compact vision sensors give industrial robots the ability to "see" with varying degrees of perception. The HDS-2 is a two-zone sensing device that has a 10-ms response time in a 50-to-500-mm range. Suitable for accurate gripper positioning, the HDS-3 is a three-zone system with all the features of the HDS-2, plus an independently adjustable middle zone.

At the heart of the HDS-23 optoelectronic vision system is the sensor head assembly. The 7.43-by-2.45-by-2.45-in. assembly, which weighs only 1.5 lb, accommodates a 25-, 50-, or 75-mm imaging lens. The fourth product in the family, the HVR-128, is a solid-state vision system offering width, length, and depth perception capability.

Honeywell Visitronic Operations, PO Box 5227, Denver, Colo. 80217; (303) 850-5050.

CIRCLE 369

POWER

Regulator adjusts voltage or current

A constant ac voltage or current regulator adjusts the incoming line voltage from zero to 117%, or the incoming current from 0 to 540 A, while holding either constant at the selected setting. The Model FRC-10 combines a regulator controller with a motorized autotransformer to obtain total control of ac lines with 1/4% regulation.

Versions of the FRC-10 are available for single- and three-phase operation from 600 VA to 300 kVA at 50, 60, or 400 Hz. A digital readout and front-panel control are available for direct reading and adjustment of the selected voltage or current.

Staco Energy Products Co., 301 Gaddis Blvd., Dayton, Ohio 45403; (513) 253-1191. From $850; stock.

CIRCLE 370

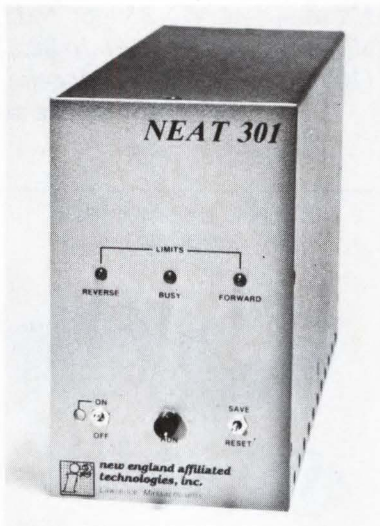
Adjustable regulators deliver 1.5 A

High-voltage adjustable regulators deliver up to 1.5 A and feature on-chip power- and thermal-limiting circuitry. The positive LT117AHV provides outputs ranging from +1.2 to +57 V, while the negative LT137-AHV covers the −1.2- to −47-V range. Wafer-level trimming enables precision adjustment of the reference voltage to within 1% at 25°C. Over the full operating temperature range, the reference is guaranteed to be accurate within 2%. The devices, which are available in TO-3 steel or TO-39 metal cans, may be specified over the full military or commerical temperature ranges.

Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, Calif. 95035; (408) 942-0810. From $4.25; stock.

CIRCLE 371

Stepper controller has RS-232-C link



Communicating over an RS-232-C link, a microprocessor-based stepping-motor controller combines high-level control and a 3-A motor driver in a compact, fan-cooled enclosure. The Neat-301 can be programmed by any CRT terminal, keyboard, or computer that has a standard serial port. Over 30 ASCII commands allow the user to assign such parameters as moving distance, initial velocity, ramp slope and length, time-out pauses, enable/disable motor current, half- or full-stepping operation, and search for home. Elaborate motion sequences can be stored in the controller's 200-byte nonvolatile RAM.

The Neat-301 interfaces directly with limit and home switches, and it has three input lines and two output lines to control external devices. It may also be operated as a slave processor, with up to 40 units daisy-chained off of a single serial port.

New England Affiliated Technologies Inc., 620 Essex St., Lawrence, Mass. 01841; (800) 227-1066 or (617) 685-4900. $1795.

CIRCLE 372

40-A bridge rectifier has integral heat sink

A line of silicon bridge rectifiers rated at 40 A features wire leads for printed circuit board mounting and a heat-sink design that provides a low thermal resistance. The heat sink is molded as an integral part of the rectifier's epoxy case. Junction-to-case thermal resistance is 1.2°C/W—lower than any of EDI's metal-cased devices. The maximum peak surge current (8.3 ms) is 300 A for the Series FPI-W and 400 A for the Series MPI-W. The case size of either series is 1 1/4 by 1 1/4 in.and 0.4 in. high, with 0.8-in. leads. The storage temperature for the rectifiers is specified from −55° to +175°C.

Electronic Devices Inc., 21 Gray Oaks Ave., Yonkers, N.Y. 10710; (914) 965-4400. $2.75 (1000 units, FPI-W); stock.

CIRCLE 373

POWER

Stepping-motor driver achieves 10,000 steps/s

Pushing stepping motors into application areas traditionally reserved for servo motors, the MD15 polar-independent driver reaches speeds up to 10,000 steps/s for full-, half-, or micro-stepping operations. The TTL-compatible unit accepts a maximum input of 45 V, generates its own 5-V supply, and has a user-programmable output current from 1 to 5 A per phase. The MD15's Auto-Park feature reduces the motor's "at rest" power consumption by 70%, with no additional control lines. Total system power requirements are further diminished by 75% through the use of switch-mode technology. The stepping-motor driver is 4¼ by 3¾ in., with a height of 2¼ in.

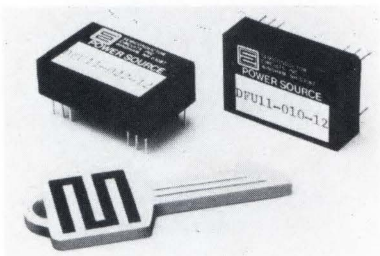
Electronic Products, PO Box 891, Mountain View, Calif. 94042; (415) 969-5829. $137 (100 units). **CIRCLE 374**

Tiny dc-dc converter delivers 1.5 A peak

Packaged in an 8-pin ceramic or plastic DIP, a dc-dc converter sports a 1.5-A, 40-V output switch transistor that provides enough drive to perform a number of switching regulator functions without the need for external power transistors and other drive circuitry. Intended for step-up or step-down conversion, the MC34063 series operates over a range of 2.5 to 40 V and requires only 2.4 mA of quiescent current. The monolithic device contains all functional circuitry, including a temperature-compensated reference oscillator, cycle-by-cycle current limiting, and feedback sensing for voltage regulation. The series is specified over the commercial, automotive, and military temperature ranges.

Motorola Semiconductor Products Inc., PO Box 20912, Phoenix, Ariz. 85036; (602) 897-3840. From $1.85 to $6.45 (100 units); stock to 12 weeks. **CIRCLE 375**

Dc-dc converters are ultra-reliable



Housed in 24-pin DIPs, a family of dc-dc converters has an MTBF in excess of 250,000 hours. The units are designed to operate from a moderately regulated dc input and to utilize that regulation to furnish well-controlled single or dual outputs. Each of the six models in the DFU series combines one of three short-circuit-protected output ratings with one of two dc input ratings: a fixed output of 5 V dc at 220 mA, ±12 V dc at ±50 mA, or ±15 V dc at ±45 mA, with an input rating of either 4.5 to 5.5 V dc or 10.8 to 13.2 V dc. The dc-dc converters have a load regulation of 1%/%V_{IN} and a temperature coefficient of 0.03%/°C, with no derating over the temperature range of −25° to +71°C.

Semiconductor Circuits Inc., 49 Range Road, Windham, N.H. 03087; (603) 893-2330. $26.50 (single output), $28 (dual output) (100 units); stock to 14 weeks. **CIRCLE 376**

Regulated UPS delivers 100 to 2000 VA

The Memorygard II series of uninterruptible power supplies delivers 100 to 2000 VA to computer-based systems or other power-sensitive equipment. It operates from a standard 120/230-V ac, 60/50-Hz power line, with backup provided by sealed, maintenance-free batteries. In the event that a line disturbance or power failure is encountered, the unit continues to supply regulated power to the load. Depending on the model, the batteries provide anywhere from 9 to 15 minutes of backup power. Status lights indicate when ac line power has been lost and when approximately two minutes of backup power remain. The Memorygard II series utilizes pulse-width modulation, which allows the output voltage to be regulated within ±5%, and it features a 2-ms transfer time.

General Power Systems, 1400 N. Baxter St., Anaheim, Calif. 92806; (800) 854-3469 or (714) 956-9321. From $495. **CIRCLE 377**

NEW PRODUCTS

PRODUCT NEWS

Plotter includes GKS device driver

In a move aimed to bring sophisticated graphics capabilities to the microcomputer market, **Nicolet's Computer Graphics Division (Martinez, Calif.)** is offering a Graphics Kernel System (GKS) device driver with their intelligent Zeta pen plotters. GKS has been proposed as the international standard for graphics and is rapidly becoming the de facto standard used by graphics designers. With the GKS device driver, the microcomputer user can create software capable of driving the eight-pen desktop plotter. The device driver is compatible with Unix and MS-DOS operating systems, including IBM PC-DOS. **CIRCLE 378**

4k PROMs feature on-chip diagnostics

Monolithic Memories Inc. (Santa Clara, Calif.) has added two 4k diagnostic registered PROMs to its family of diagnostic PROMs. Designated the 63DA441 and the 63DA442, the devices feature on-chip shadow registers that negate the need for embedded diagnostic codes and eliminate intermediate illegal states, which can result from alternative diagnostic methods. The 4k PROMs feature an output of 24 mA, a maximum setup speed of 40 ns, and a clock-to-output time of 20 ns. Housed in 24-pin SkinnyDIPs, the parts are available off-the-shelf at $16.65 in quantities of 100. **CIRCLE 379**

Portable Professional gets hard-disk option

A 10-Mbyte Winchester disk option is being offered by **Texas Instruments Inc. (Dallas, Texas)** for its Portable Professional Computer. The drive is designed to provide users with the higher-capacity hard-disk storage that is required for large data-base and storage-intensive applications. To meet the requirements of operating a Winchester disk in a portable environment, the drive has been shock-mounted inside the computer and a software-controlled "landing zone" has been added. The landing zone adds an additional level of data integrity by ensuring that the read/write heads are positioned over a nondata portion of the disk when the power is turned off. The average access time of the disk drive is 85 ms, and it is compatible with MS-DOS 1.25 and 2.11. Available as either a field-installable kit or as a factory-installed option, the 10-Mbyte disk drive and controller card cost $2295. **CIRCLE 380**

ElectronicDesign

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Want to contact us? Address your correspondence to:

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PRODUCT NEWS

Laser head improves accuracy, costs less

Hewlett-Packard Co. (Palo Alto, Calif.) has introduced the HP 5517A laser head—a high-stability laser source for the HP 5501A laser-transducer system—which provides higher-performance laser interferometry measurement at a lower price. The head has a higher specified stability than its predecessor and is more reliable due to design improvements. The HP 5517A is accurate to within 0.1 ppm, or 0.1 μm/m, and remains calibrated indefinitely. Measurement resolution for the transducer system ranges from 0.16 to 0.005 μm (6.2 to 0.2 μin.). The laser head costs $6200, while approximate prices for complete laser-transducer systems range from $15,000 (one axis) to $45,000 (four axes). **CIRCLE 381**

ECL devices boast power/speed ratio

Three ECL10KH high-speed emitter-coupled-logic devices from **Monolithic Memories Inc. (Santa Clara, Calif.)**—a licensed alternate source for Motorola's MECL10KH family—offer twice the speed at the same power dissipation as the older MECL10K series. The devices, designated the MC10H101, -210, and -211, feature a propagation delay of just 1 ns. Power dissipation is typically 160 mW for the 210 and 211 devices and 130 mW for the 101 device. The parts are both functional- and pin-duplicates of the MECL10K family, allowing users to increase the speed in critical timing areas of existing systems without creating new designs. In quantities of 100, the 101 costs $3.34 and the 210 and 211, $3.37. Production quantities will be available in November. **CIRCLE 382**

Push-button units have twist/pull release

Allen-Bradley Co.'s Industrial Control Division (Milwaukee, Wis.) has added the Twist-or-Pull Release mechanism to its Bulletin 800T (30.5 mm) NEMA Type 13 oiltight push-button line. The patented operator mechanism for two-position push-pull units may be twisted or pulled to obtain the "out," or "released," position. The design enables these devices to meet both domestic (pull release) and international (twist release) operating practices. As an additional safety feature, the mechanical detent action of the operator is designed to occur before the electrical contacts change state when the button is pushed from the "out" to the "in" position. The units are available in a variety of contact configurations and as illuminated or nonilluminated versions. The illuminated version is offered in transformer, full voltage, neon, or dual-input types. **CIRCLE 383**

PRODUCT NEWS

300-A module extends Schottky diode line

Extending **Siemens Components Inc.'s (Broomfield, Colo.)** 50-V Schottky module line is the 300-A FST300, which is available with blocking and voltage ratings of 35, 40, 45, and 50 V. The device is composed of four dice (two matched dice in parallel per leg) encapsulated in a TO-244 package. The FST300 features a maximum average current of 150 A per leg and a 300-A peak current. It also has a maximum instantaneous forward-voltage drop per leg of 0.78 V. The low-profile TO-244 package replaces four 75-A DO-5 packaged devices. **CIRCLE 384**

Interface links Dash-1, IBM design system

FutureNet Corp. (Canoga Park, Calif.) has developed an interface that allows schematic diagrams created on the company's Dash-1 workstation to be transferred to the IBM Circuit Board Design System (CBDS). The interface translator, which sells for $800, simplifies the job of entering and checking schematics developed on the IBM PC- or XT-based Dash-1, and it enables the designer to move quickly onto the circuit board design functions of the CBDS.

CIRCLE 385

CompuPro 10 option lowers networking costs

A network option for the CompuPro 10, a multi-user microcomputer from **CompuPro (Hayward, Calif.)**, allows up to 16 users on four nodes to be networked together for less than $100 per user. The Net 10 option uses Datapoint's Arcnet protocol and requires only a passive hub and RG62 coaxial cable to network four CompuPro 10 four-user systems (or nodes). Using the Arcnet protocol and DRNET software eliminates the need for a dedicated file server, which helps to achieve the low cost per user.

CIRCLE 386

7-bit flash a-d converters cost 38% less

A 38% price reduction comes from **Motorola Semiconductor Products Inc. (Phoenix, Ariz.)** for two of its 7-bit flash a-d converters. The MC10315L and the MC10317L, which previously sold for $79 in 100-unit quantities, now sell for $49 in like quantities. The converters perform identically in all aspects except when driven into overrange: all data bits remain high on the 315L, whereas the data bits go low on the 317L. **CIRCLE 387**

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APPLICATION NOTES

Gas distribution in microelectronics

A four-page technical note discusses the design and construction of high-purity distribution systems for gases used in microelectronic processing. Recommendations are made regarding the use of welding, soldering, and brazing for various applications.

Systonics Inc., PO Box 121, Winchester, Mass. 01890.
CIRCLE 388

Using a two-channel spectrum analyzer

A series of five notes describes practical measurement methods using the SD375 dual-channel FFT spectrum analyzer. DSP-104 is an 18-page primer which provides guidance in both real-time frequency and time-domain measurements. Illustrated throughout with graphic plots, the primer describes the measurement of structural and electrical model transfer functions. DSP-105 contains examples of using equalized ratio (the ratio of two transfer functions) to solve common problems and how to perform an equalized ratio measurement with the SD375. DSP-111, *The How and Why of Zoom*, provides simple instructions for achieving the measurement precision required to determine the damped ratio of high-Q structural resonances. The DSP-051 note describes the application of the SD375's internal signal source, which is synchronous with the FFT sample rate. Finally, DSP-050 offers a discussion of cross-property measurements.

Scientific-Atlanta Inc., Spectral Dynamics Division, 1 Technology Park, PO Box 105600, Atlanta, Ga. 30348.
CIRCLE 389

Building an a-d conversion system

A 12-page publication, entitled *Building a Better A/D Solution*, offers a starting point to determine performance capabilities of combined amplifier/multiplexer/analog-to-digital converter systems to achieve the required channel configuration, speed, and accuracy. Descriptions of each analog and digital building block are provided, including analog-input channel amplifiers, filters, and multiplexers, as well as many digital I/O interfaces. The paper also presents a variety of standardized custom data-conversion systems.

Preston Scientific, 805 E. Cerritos Ave., Anaheim, Calif. 92805.
CIRCLE 390

NEW LITERATURE

Industrial-type super glues

The Pacer Tech line of cyanoacrylate adhesives for industrial applications is described in a product information kit. The literature covers 36 grades of super glues, including extended-range, extended-performance, high-impact/high-integrity, high-clarity (optical), extended-temperature, moisture-resistant, ultra-slow-setting, and temporary-bonding types. Special products such as accelerators, automatic dispensing equipment, tapered microtips, and the patented "breakaway" packaging are also covered.

Pacer Technology & Resources Inc., 1600 Dell Ave., Campbell, Calif. 95008. **CIRCLE 391**

More IEEE computer publications

The *1984 Publications Catalog Update of the Computer Society of the IEEE* features over 80 titles on a wide variety of subjects and applications in computer science and engineering. The 16-page document includes 32 new books published since last fall, including *Software Design Techniques, Computer Networks, Robotics, and Computer Graphics*.

IEEE Computer Society Press, 1109 Spring St., Suite 300PR, Silver Spring, Md. 20910. **CIRCLE 392**

Tape systems and controllers

A brochure serves as a guide to a line of magnetic tape systems and controllers that are compatible with HPIB and GPIB (IEEE-488) computer systems. It includes the performance range and applications of each device, as well as a chart that references products that interface with specific computer brands on a model-by-model basis.

Dylon Data Corp., 9561 Ridgehaven Court, San Diego, Calif. 92123. **CIRCLE 393**

In-circuit testing theory and operation

The *Introduction to In-Circuit Testing* provides the necessary background information to understand the purpose, theory, and operation of in-circuit testing and testers, including the 2272, 2275, and 2276 test systems. The 125-page illustrated primer discusses the various techniques for in-circuit testing and describes the components of a test system. It covers how the tester fits into the manufacturing process and what types of faults it can detect. Also outlined is the step-by-step process used by the programmer to develop a test program and by the operator to test boards.

GenRad Inc., 170 Tracer Lane, Waltham, Mass. 02254. **CIRCLE 394**

Rf and microwave components, systems

A catalog contains 352 pages of photos, specifications, features, outline drawings, and prices for a complete line of rf and microwave components and test and measurement systems. The products cover the frequency range of dc to 40 GHz and have power handling capabilities up to 500 W. Nearly a third of the catalog is devoted to technical information, such as definitions, terms, explanations of various design considerations, and methods of obtaining microwave measurements. A condensed rf and microwave glossary is also included.

Weinschel Engineering, 1 Weinschel Lane, Gaithersburg, Md. 20877. **CIRCLE 395**

Probing products for semiconductor testing

Featuring a new line of Kelvin probes and specialty card layouts, a catalog details probing materials, instrumentation, and related equipment for semiconductor testing. Sections include probe tips, cards, instruments, and accessories, as well as probing services for firms desiring complete probe-card assemblies, probe-card design, repairs, and refabrication.

Accuprobe Inc., 1 Harrison Ave., PO Box 1044, Salem, Mass. 01970. **CIRCLE 396**

NEW LITERATURE

IR photodetectors and phototransistors

A 60-page technical handbook details a range of optoelectronic products. The BPW41D infrared photodetector is featured, along with an extensive application note on its use in infrared remote control and data transmission. The ZNP100 series of programmable light-activated photoswitches is also highlighted, as well as standard hermetic and plastic phototransistors and the MS series of photocells. A cross-reference list shows the nearest Ferranti equivalent to a variety of other manufacturers' devices.

Ferranti Electronics Ltd., Fields New Road, Chadderton, Oldham, Lancs. OL9 8NP, England.

CIRCLE 397

Vacuum and gas capacitors

Vacuum and gas-filled capacitors are the subject of a 56-page brochure (No. 103C), which presents device characteristics covers 186 models. Two hundred charts and graphs are used to present individual working voltages and peak test voltages, as well as current-carrying capabilities over various frequency ranges. Also included is a nomograph for calculating maximum current vs capacitance, frequency, and working voltage.

Laughlin Ave., San Jose, Calif. 95122.

CIRCLE 398

Fiber-optic components and accessories

A buying guide and reference source for fiber-optic components is divided into seven sections, including optical fibers and cables, connectors and accessories, optoelectronics and lasers, transmitters and receivers, data communications, test and measurement, and terminating kits and service aids. The catalog also includes a glossary of fiber-optic terminology.

Optronics Ltd., Cambridge Science Park, Miltron Road, Cambridge CB4 4BH, England. **CIRCLE 399**

Analog, digital, and custom ICs

A 70-page short-form data book describes analog, digital, and custom integrated circuits with individual product descriptions, specifications, and pinouts. Standard products include bipolar digital logic (PROMs and programmable logic), CMOS digital products (RAMs, communication ICs, bus drivers, and µPs), and analog products (op amps, voltage references, comparators, analog-to-digital and digital-to-analog converters, and multiplexers). Full custom, standard cell, and gate array capabilities are discussed, along with radiation hardness requirements.

Harris Corp., Semiconductor Sector, PO Box 883, Melbourne, Fla. 32902.

CIRCLE 400

Motion control for industrial automation

The uses of programmable motion controllers (PMCs) for industrial automation are explored in a 28-page bulletin, which presents the Model 320 PMC. It begins with an introduction to what a PMC is and presents considerations for a total system solution, including the selection of drives and actuators. It also discusses feedback devices, the programming process, the types of functions generated, point-to-point positioning, open- and closed-loop systems, I/O terminal devices, and operator interface devices.

Kiowa Corp., 1365 Park Road, PO Box 293, Chanhassen, Minn. 55317.

CIRCLE 401

CMOS 8-, 12-, and 16-bit multipliers

Twelve pages of data sheets describe a family of multiplier products, including 8-by-8-bit parallel and unsigned parallel multipliers, 12-by-12-bit parallel and microprogrammable parallel multipliers, and 16-by-16-bit parallel and microprogrammable parallel devices. Functional and timing diagrams, pinout configuration tables, electrical performance, switching characteristics, absolute maximum ratings, and recommended operating conditions are given for each.

Logic Devices Inc., 628 E. Evelyn Ave., Sunnyvale, Calif. 94086. **CIRCLE 402**

NEW LITERATURE

Quick-reference resistor list

A handy reference guide lists over 150 standard resistors in wirewound, metal film, carbon film, and metal oxide styles. Specification columns include power, type, temperature coefficient, element, value range, standard and available tolerances, maximum working voltage, package size, and reference pricing.

Dale Electronics Inc., 2064 12th Ave., PO Box 609, Columbus, Neb. 68601. **CIRCLE 403**

Rotary and linear positioning devices

A positioning-equipment catalog presents a line of motor-driven rotary and X-Y tables, programmable stepping-motor controllers, linear translation stages, optical mounts, adjustment drives, beam directors, and platforms and stands. Specifications, photographs, and line drawings are provided for each of the over 400 items.

Daedal Inc., PO Box G, Sandy Hill Road, Harrison City, Pa. 15636. **CIRCLE 404**

Fire protection for electronic equipment

The advantages of a totally integrated Halon fire-suppression system are outlined in an eight-page brochure. The publication explains why and where such systems are needed and how they operate. It points out the special problems of protecting sensitive electronic equipment, which are not solved with traditional fire protection systems.

Ansul Fire Protection, 1 Stanton St., Marinette, Wis. 54143. **CIRCLE 405**

Motor, speed, and process controls

Numerous control devices are featured in a 48-page brochure, which contains detailed engineering information on dc motor controls with matched dc motors; adjustable frequency drives; velocity servo controls; process control modules; sequential programmable controls; and related control accessories.

Minarik Electric Co., PO Box 54210, Los Angeles, Calif. 90054. **CIRCLE 406**

The IBM PC as a 'personal instrument'

How to transform an IBM PC into a personal instrument using the MICRO-BASYS microprocessor-based data acquisition system is the topic of discussion in a four-page brochure. The literature covers hardware and software, gives an overview of the real-time I/OBasic language, and provides a summary of the various plug-in boards available for stand-alone system control.

ADAC Corp., 70 Tower Office Park, Woburn, Mass. 01801. **CIRCLE 407**

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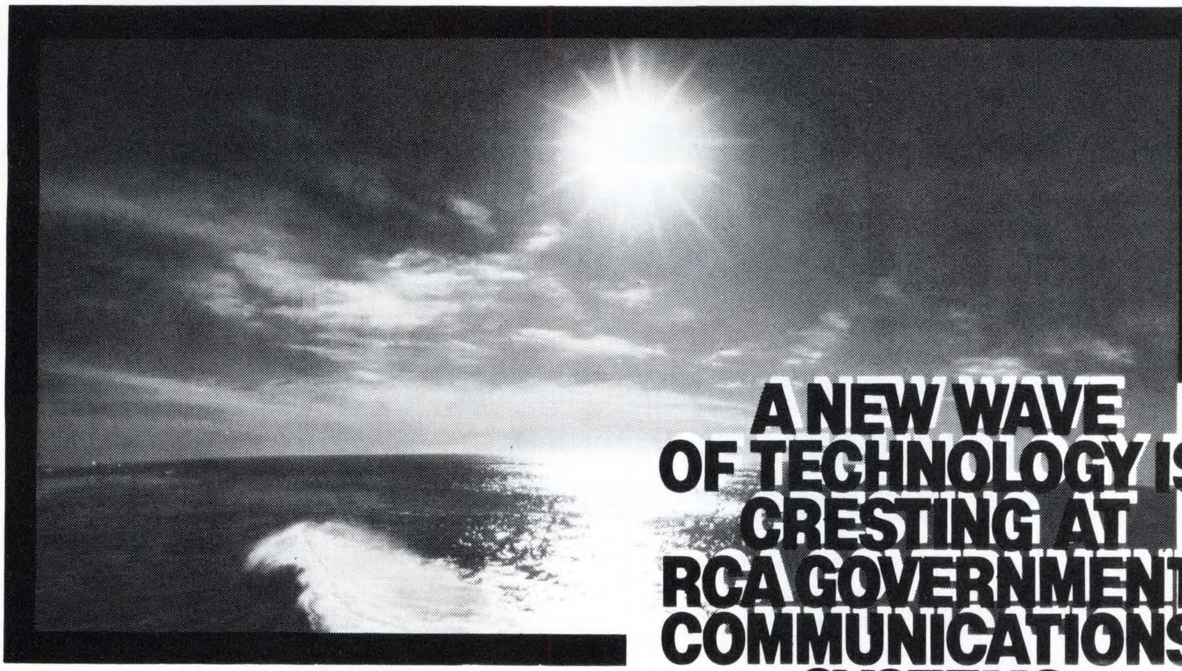

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- Mini Computer (DEC, Data General, Perkin-Elmer, AN/UYK20)
- Micro Processor (M68000, LSI II, 8086, Z80)
- Real-Time Communications Processing
- Signal Processing
- Distributed Processing
- Data base design
- Systems software development

Manager Of VHF/UHF Equipment Design

- Experience in design & test of VHF/UHF communication systems and equipment. Project planning and supervision of managers and engineers.

Reliability And Maintainability Engineers

- Systems Prediction
- System Modeling
- Failure Mode and Effects Analysis
- Demonstrations
- Failure Reporting, Analysis, Corrective Action

Manager Of Parts And Materials Selection And Publications

- Passive Parts
- LSI and other Solid State Devices
- Parts Application Methodology
- Electromechanical parts
- Military Parts Specifications
- Failure Analysis and Data Base

Quality Assurance Administrator

- Implement MIL-Q-9858/MIL-I-45208 program
- Special Vendor Evaluation
- DOD Contract Requirements Review
- Quality Planning
- MRB

Manager Of Aerospace Recording Projects

- Experience in managing complex programs in both the engineering development and low quantity production. Experience with NASA programs desired. Project planning and supervision of managers and engineers required.

Project Leaders

- 10 years experience in high performance magnetic Recording Systems; supervision of related teams
- Experienced in Microwave & Satellite Communications equipment or system design
- Experienced in LF/HF/VHF/UHF Radio Equipment and Systems Design

Electrical Engineers

- High speed digital logic design (ECL, TTC & CMOS types)
- Microprocessor utilization, interfacing & firmware design
- Digital signal processing-signal analysis classification speech processing
- Computer systems-systems integration, computer controlled equipment
- COMSEC equipment design & development
- EMI/Tempest analysis and design
- ELINT Signal Processing
- Telephone Systems Design
- Data Communications Systems Design
- Microwave Equipment Design & Development
- Radio Equipment Design & Development-LF/HF/VHF/UHF
- Communication Equipment Design & Development
- Communication Design & Integration
- Inductive Component Design
- Parts Applications and Evaluation
- VLSI Evaluation & Test
- Custom LSI Design
- Interface Circuit Design
- ATE Design

Mechanical Engineers

- Electronic Packaging
- Shock, vibration, thermal analysis

Systems Engineers

- Very large high speed data base management
- Integrated communications networks
- Distributed networks
- High speed real time signal processing
- Man machine interface
- System survivability-Equipment Nuclear Hardening
- Requirements analysis and Formal structuring of requirements
- Military C^3 networks
- Communications and Signal Processing Technology Development
- Simulation analysis of modems, filters, optical systems
- Waveform and modulation design
- Microwave propagation modeling, analysis, simulation
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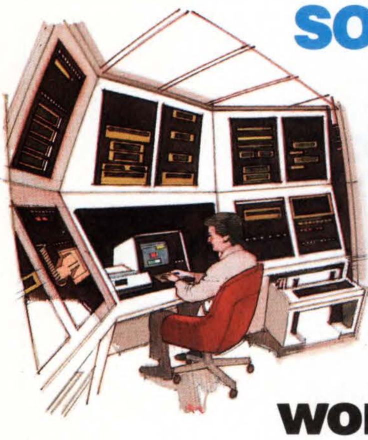

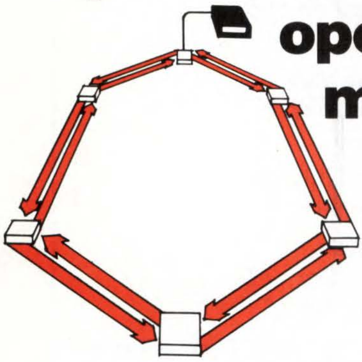

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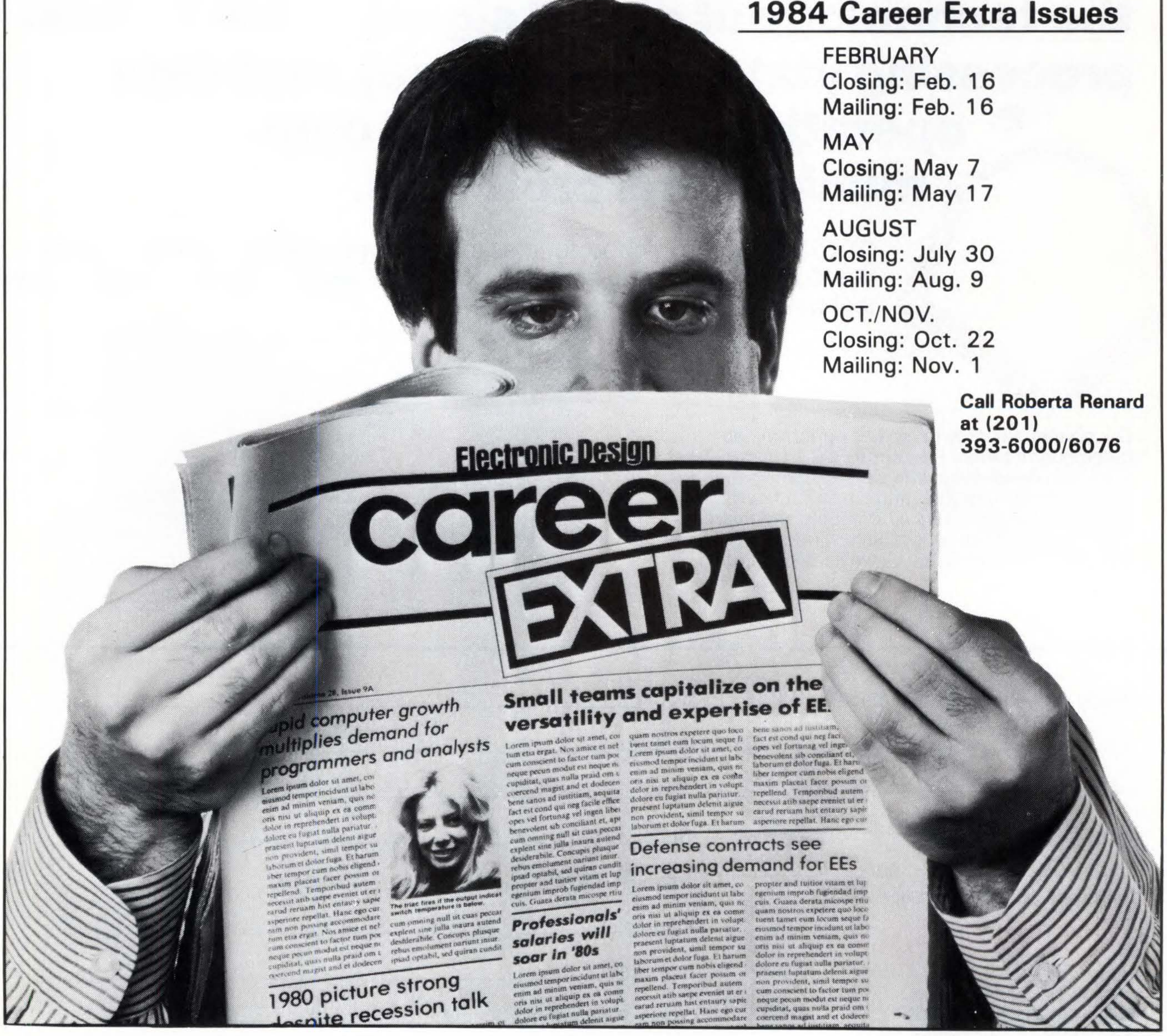

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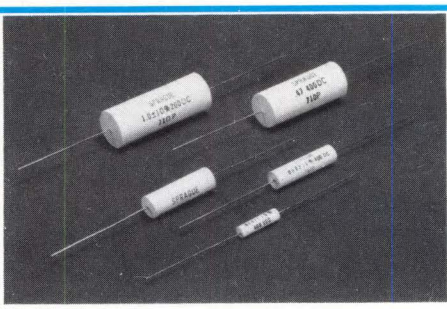

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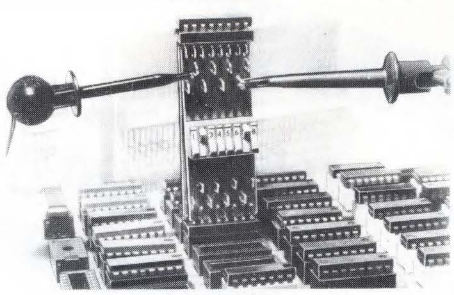

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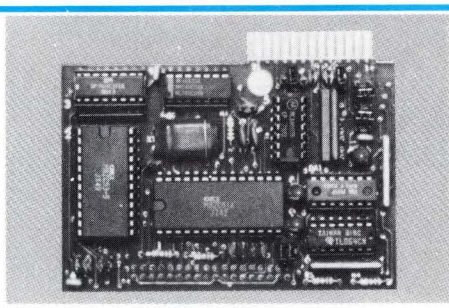

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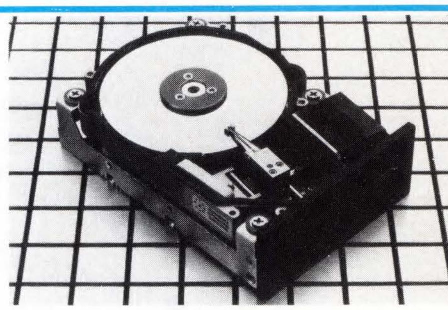

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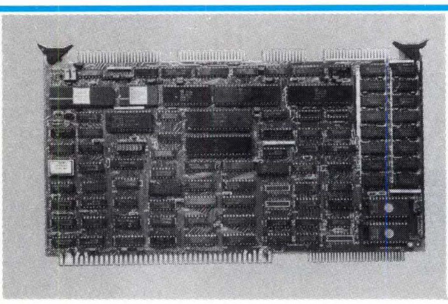

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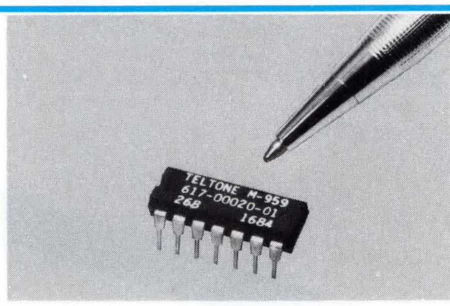

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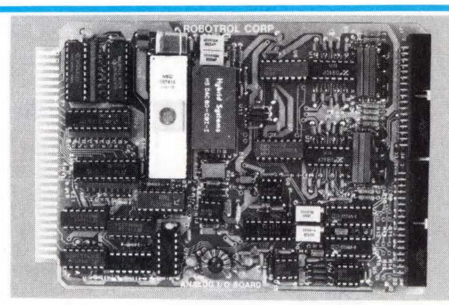

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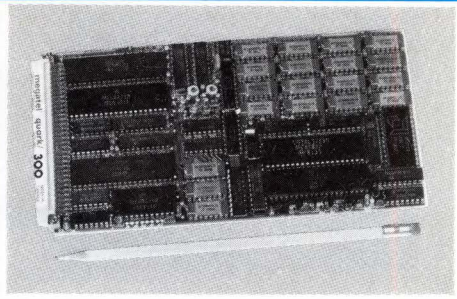

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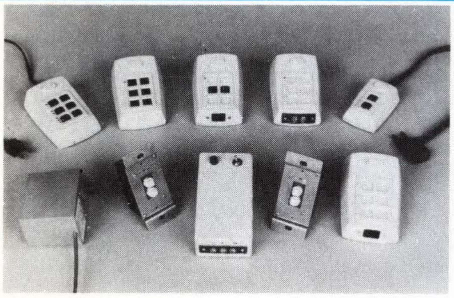

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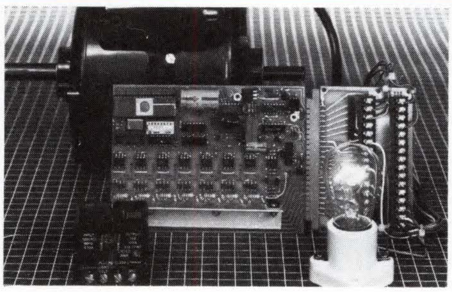

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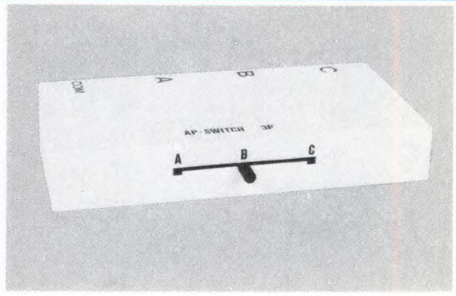

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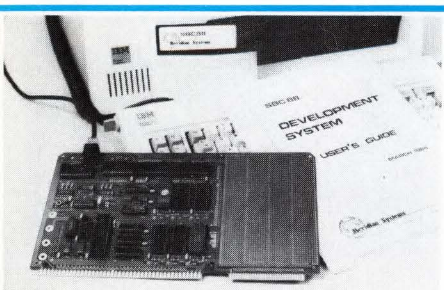

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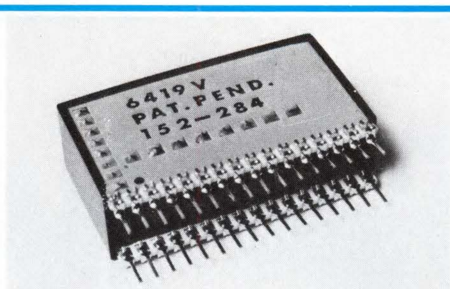

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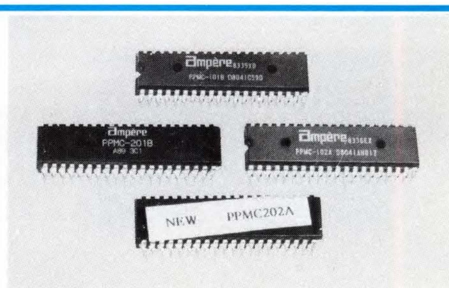

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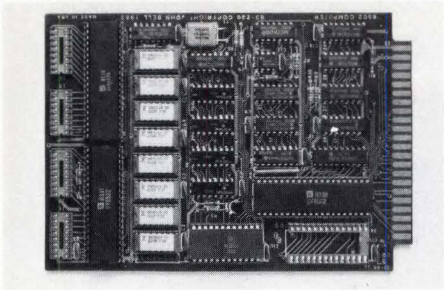

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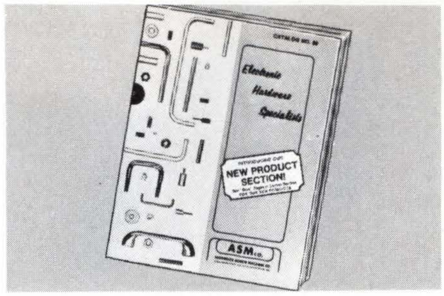

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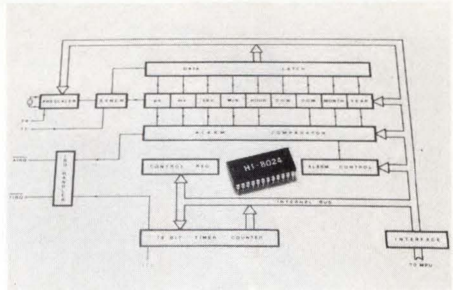

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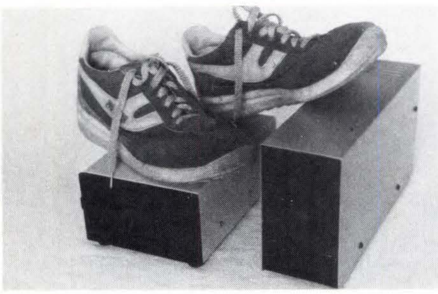

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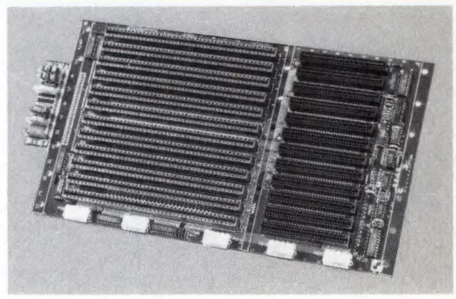

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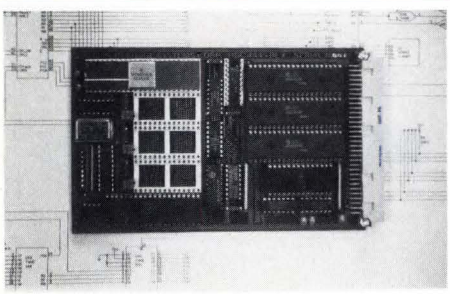

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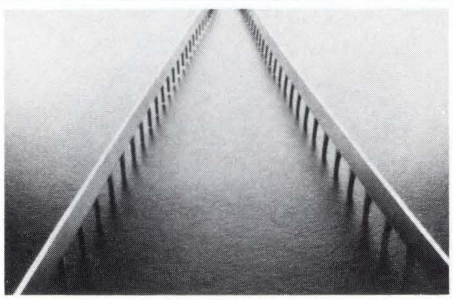

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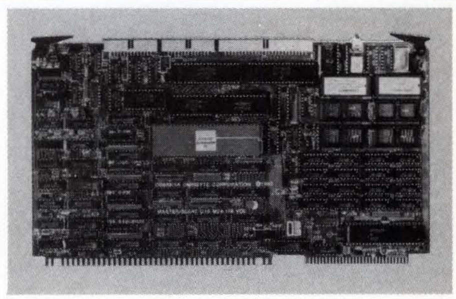

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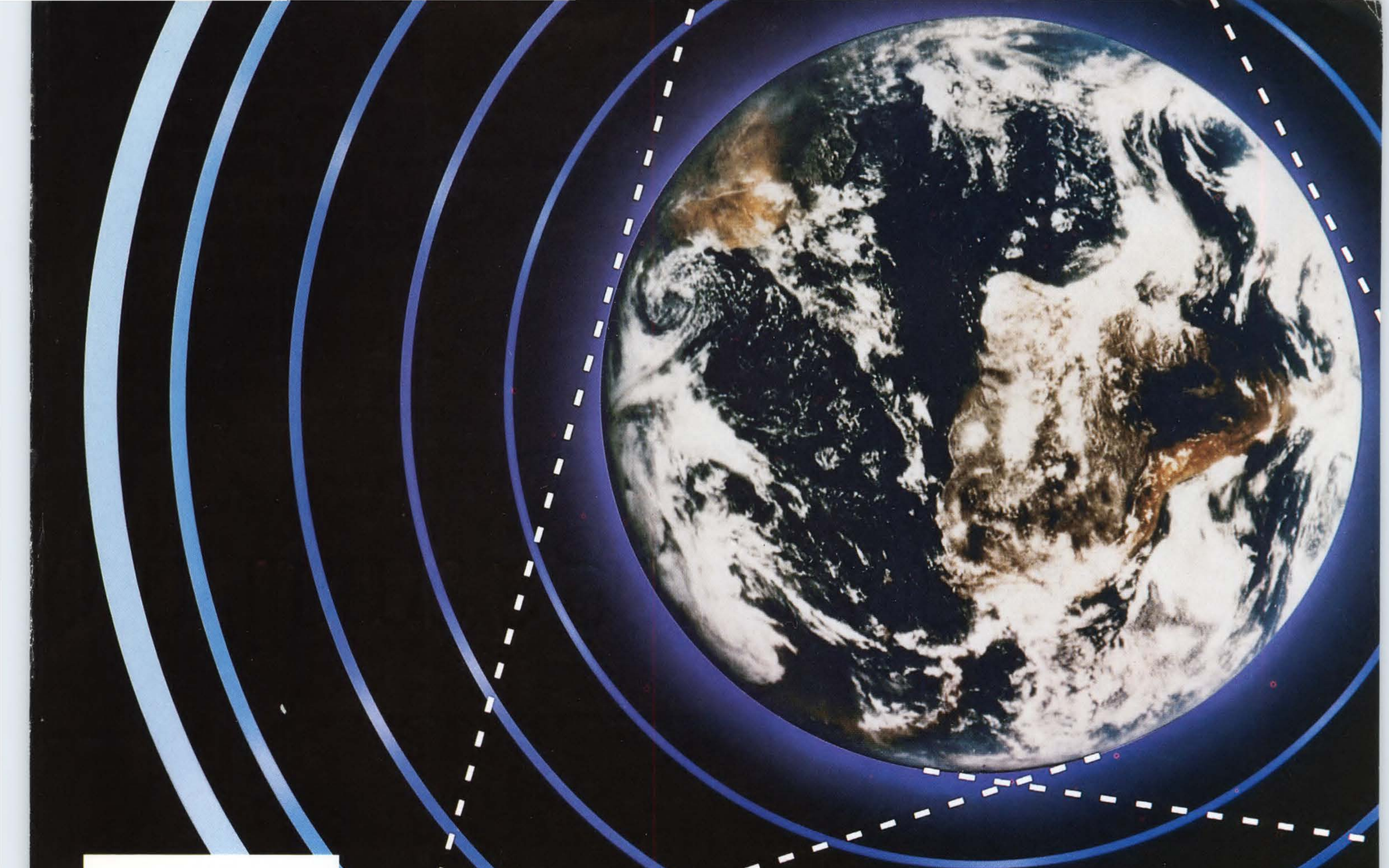
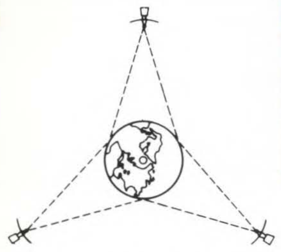


The Earth from 22,300 miles in space. (Photo: Courtesy of NASA)



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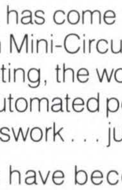

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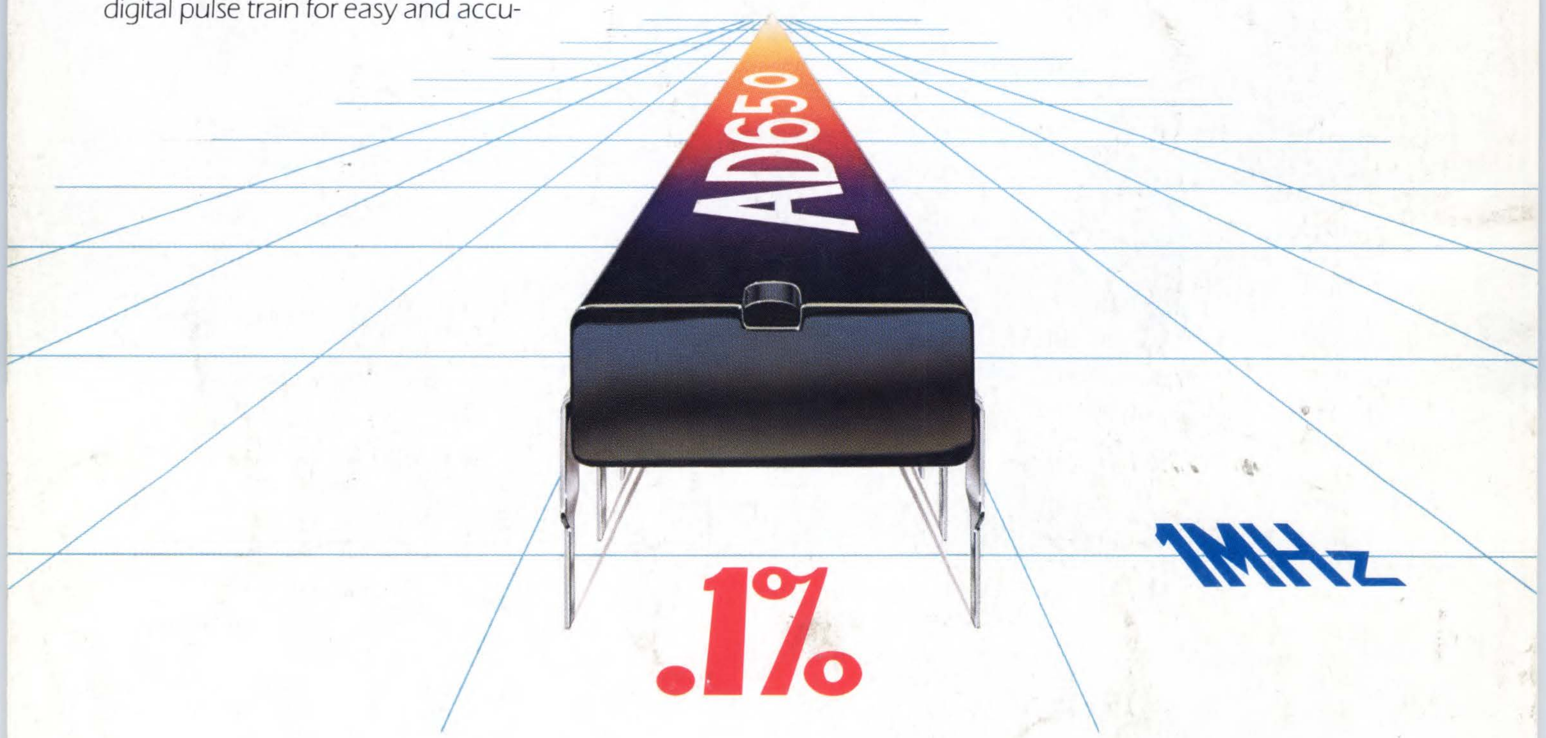

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