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OCTOBER 13, 1988

EDN®

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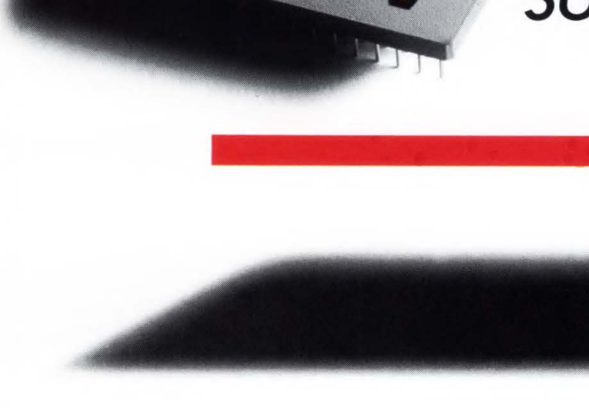

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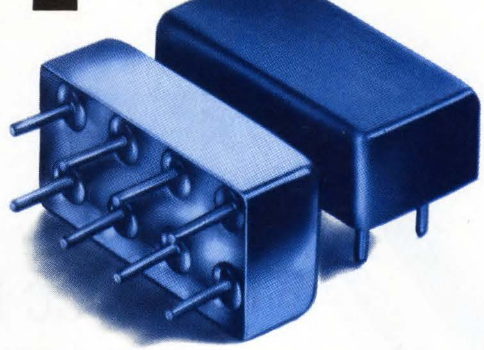

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MODEL	FREQ. RANGE (MHz) f_L to f_u	GAIN dB min	GAIN dB flatness††	MAX. OUT/PWR† dBm	NF dB (typ)	DC PWR 12V, mA	PRICE $ ea. (5-24)
MAN-1	0.5-500	28	1.0	8	4.5	60	13.95
MAN-2	0.5-1000	19	1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
★MAN-1AD	5-500	16	0.5	6	7.2	85	24.95

††Midband $10f_L$ to $f_{u/2}$, ± 0.5dB †ldB Gain Compression ◇Case Height 0.3 In.
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C118 REV. C

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absorptive... reflective

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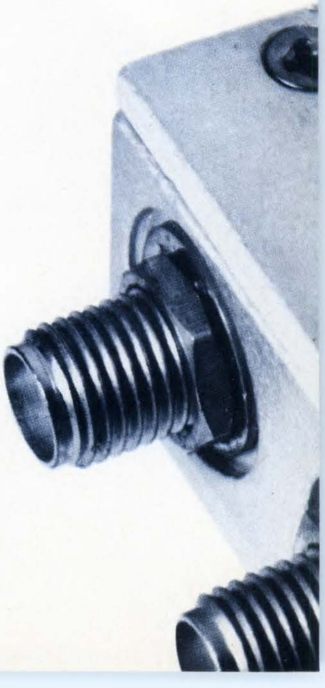
SPECIFICATIONS

Pin Model	**KSW-2-46**		**KSWA-2-46**	
Connector Version	**ZFSW-2-46**		**ZFSWA-2-46**	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec)				
rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	**-5V** on, OV off		**-5V** on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (1-24)	**$32.95**		**$48.95**	
	$72.95		**$88.95**	

C 117 REV. D



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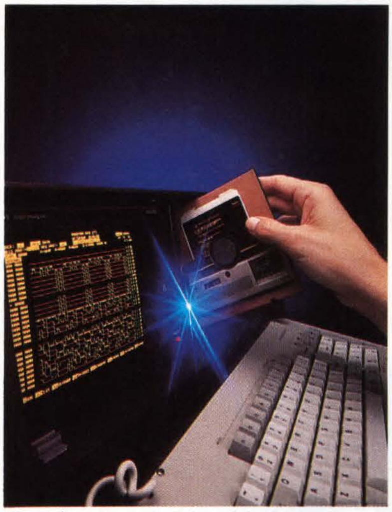
CIRCLE NO 22

EDN Magazine Edition

Volume 33, Number 21 — October 13, 1988

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *PC-based logic analyzers are assuming varied guises and offering a surprising variety of functions. See pg 134. (Photo courtesy John Fluke Mfg Co Inc)*

SPECIAL ISSUE: TEST & MEASUREMENT

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

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BPA ABP

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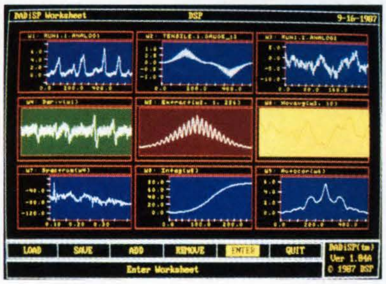

For test and measurement software, color graphics is here to stay (pg 59).

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

Express Request

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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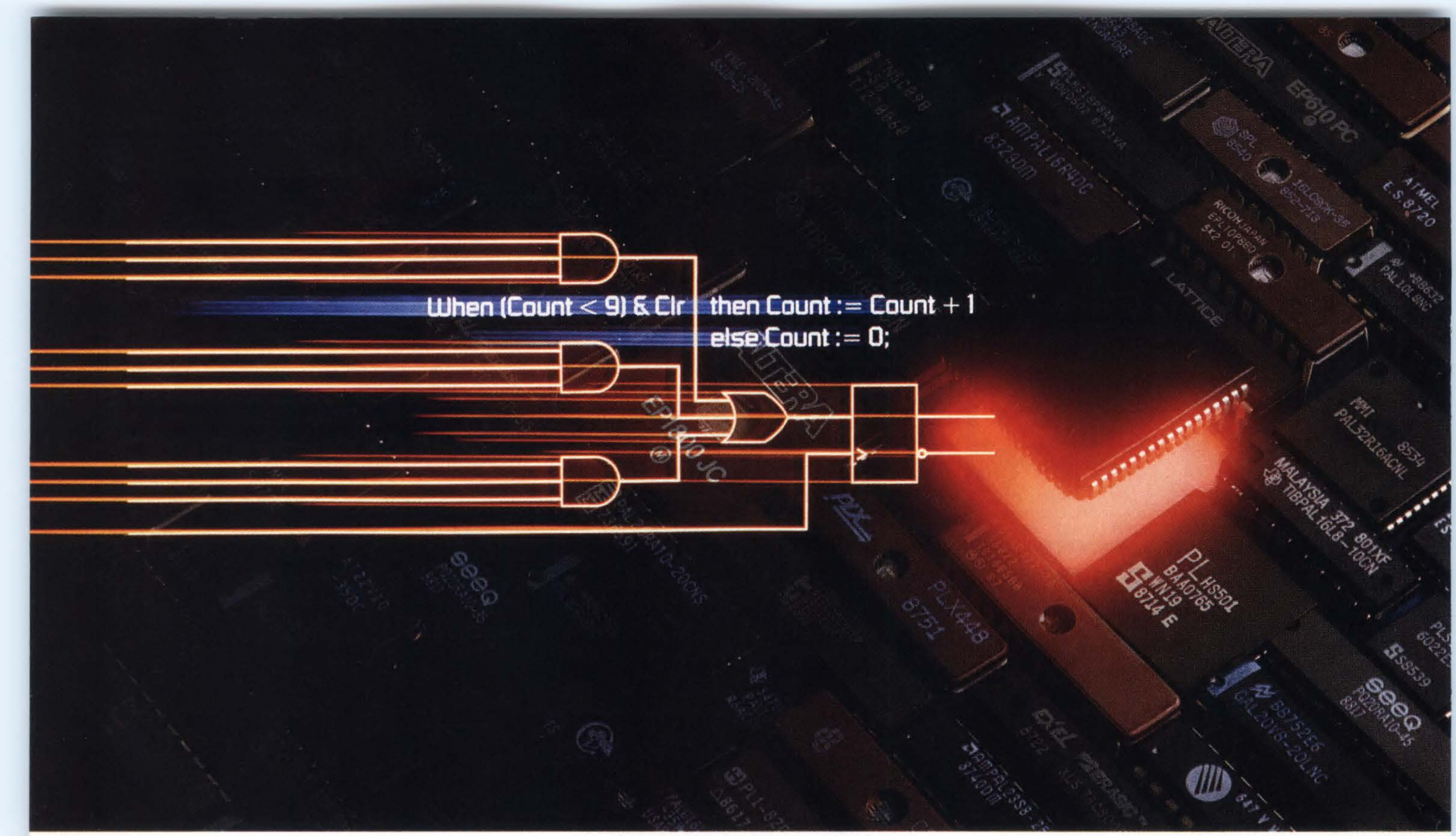

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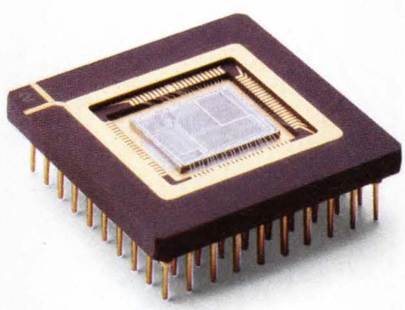
DESIGN ENGINEER, 1988



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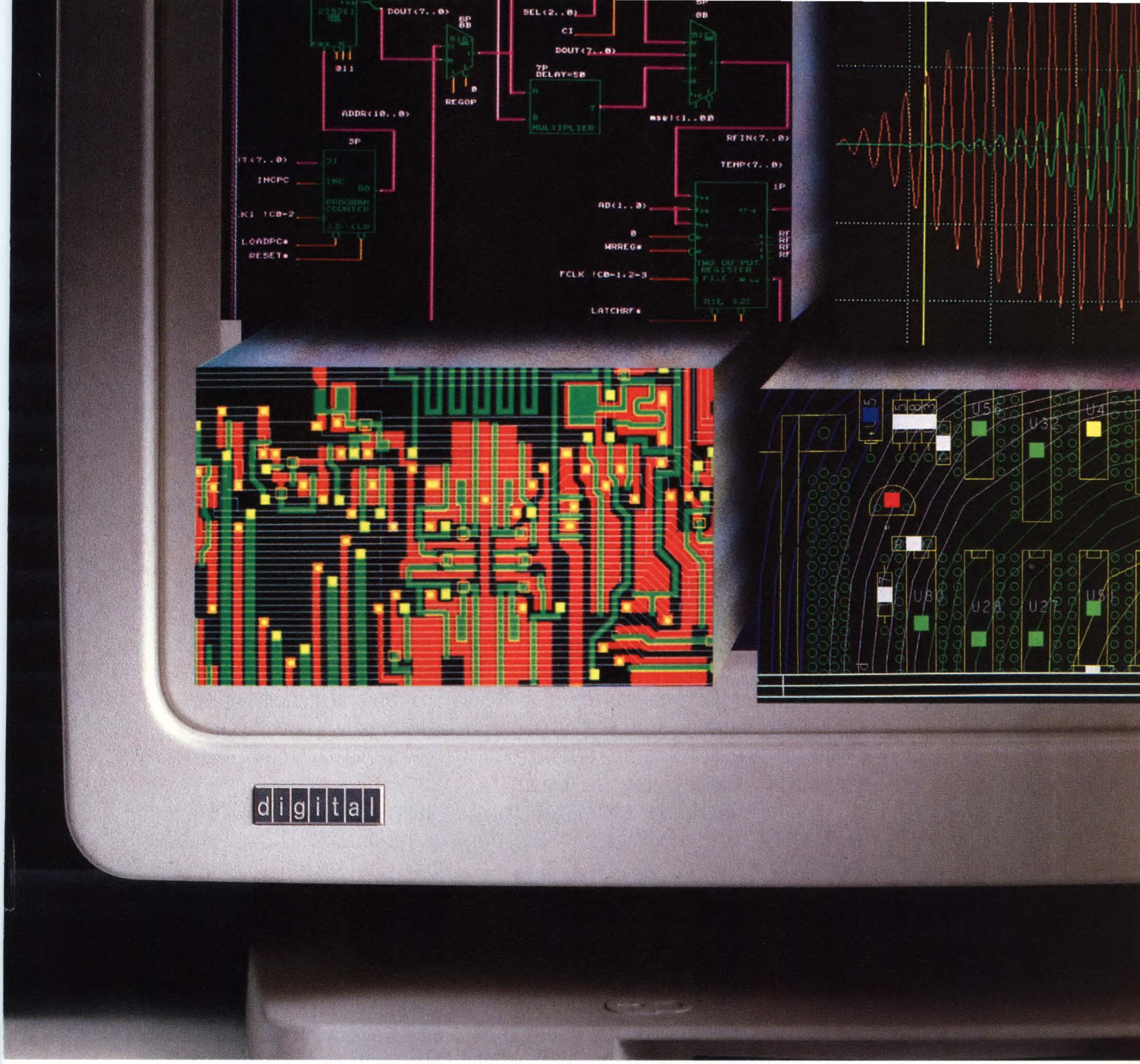

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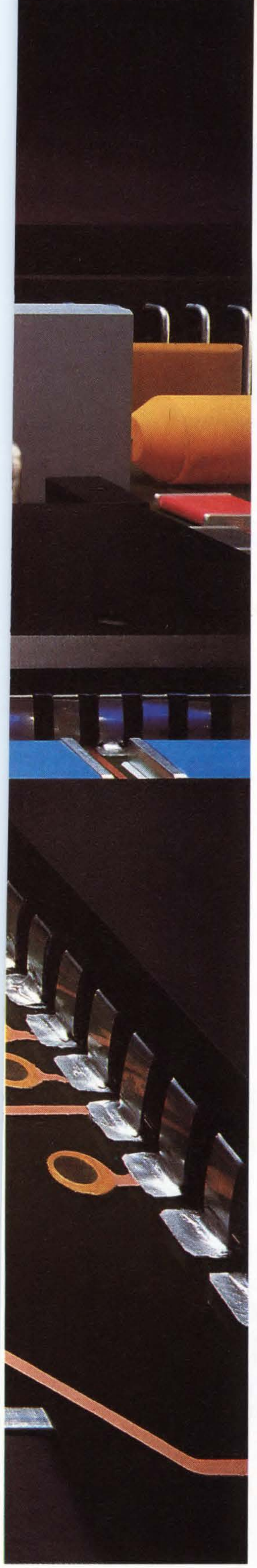

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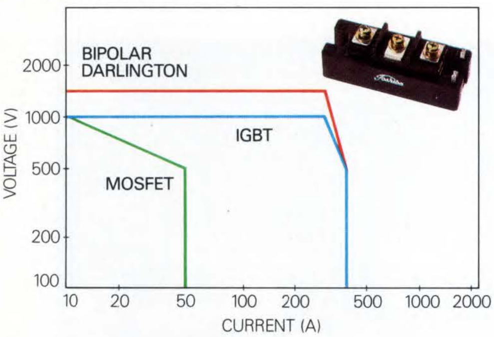

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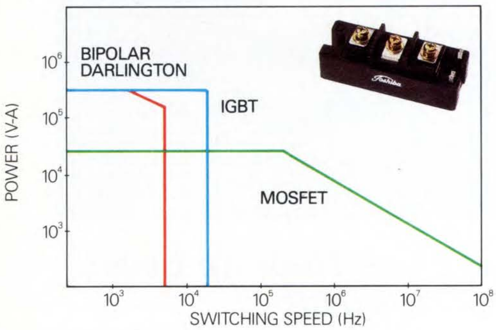

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Compare Selection

IGBT (Insulated Gate Bipolar Transistor) Selection Guide

CIRCUIT	SYMBOL	V_{CES}(V)	MAXIMUM RATING COLLECTOR CURRENT Ic (A) 8	15	25	50	75	100	150	200	300	400
	BS	500		GT15H101† MG15H1BS1	GT25H101† MG25H1BS1	GT50G101† (400V) MG50H1BS1	MG75H1BS1*	MG100H1BS1				
		1000	GT8N101†*	GT15N101† MG15N1BS1	MG25N1BS1	MG50N1BS1	MG75N1BS1*					
	US	500									MG300H1US1	MG400H1US1
		600									MG300J1US1*	MG400J1US1*
		1000								MG200N1US1*	MG300N1US1*	
		1200								MG200Q1US1*	MG300Q1US1*	MG400Q1US1*
	YS	500			MG25H2YS1	MG50H2YS1	MG75H2YS1	MG100H2YS1	MG150H2YS1	MG200H2YS1		
		600					MG75J2YS1*	MG100J2YS1*	MG150J2YS1*	MG200J2YS1*		
		1000		MG15N2YS1	MG25N2YS1	MG50N2YS1	MG75N2YS1	MG100N2YS1	MG150N2YS1*			
		1200			MG25Q2YS1*	MG50Q2YS1*	MG75Q2YS1*	MG100Q2YS1*	MG150Q2YS1*	MG200Q2YS1*		
		1400			MG25S2YS1*							
	JS	1000			MG25N1JS1							
	ZS	500				MG50H1ZS1						
		1000			MG25N1ZS1							
	ES	500		MG15H6ES1*								
		1000	MG8N6ES1*	MG15N6ES1*								

†Non Isolated Type TO-3P *Under Development

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SPD-88-003

CIRCLE NO 31

NEWS BREAKS

EDITED BY JOANNE CLAY

GaAs 22V10 PLD ATTAINS 7.5-NSEC PROPAGATION DELAY

Circuit improvements and a drop to 0.7-μm effective transistor gate lengths allowed Gazelle Microcircuits, Inc (Santa Clara, CA, (408) 982-0900) to chop 25% off the propagation delay of the GA22V10, the company's recently announced 10-nsec, laser-programmed, GaAs PLD (see EDN, June 23, 1988, pg 95). The $37 (10,000) GA22V10-7 sports a 7.5-nsec propagation delay and a 110-MHz max toggle frequency. The firm expects the device to cost $16 (10,000) in 1990.—Steven H Leibson

DSP-BASED MICROCONTROLLER OFFERS 160-NSEC CYCLE TIME

The DSC320C14 microcontroller from Microchip Technology Inc (Chandler, AZ, (602) 345-3287) combines 4k words of ROM, 256 words of RAM, and various I/O signals with a DSP320C10 DSP μP core; it executes multiply-accumulate operations in a single 160-nsec instruction cycle. The microcontroller's on-chip features include 16 bit-selectable I/O lines, 15 internal/external interrupt inputs, and 1 nonmaskable interrupt signal. The chip also includes four 16-bit general-purpose timers that have 160-nsec resolution. An on-chip serial port operates at 6.4 MHz synchronously or 400 kHz asynchronously. You can also configure the serial port to connect to the Bitbus. The chip will be available in a 40-pin DIP, a 44-pin PLCC, and a 68-pin PLCC. You can buy samples of the chips for $75; production quantities will be ready in the first quarter of 1989. Texas Instruments will act as an alternate source for the parts.—Maury Wright

SEDCO INKS PACTS WITH IBM AND SAE FOR DESIGNLIBS

Two recently announced agreements will assist pc-board designers in their jobs. First, Standard Engineering Data Company (Sedco, Scotts Valley, CA, (408) 438-7885) and Systems Effectiveness Associates Inc (SEA, Norwood, MA, (508) 762-9252) have agreed to jointly market their advanced-component libraries and analysis capabilities. You can now obtain compatible libraries for pc-board design and thermal, reliability, maintainability, and life-cycle analysis tasks. Sedco will provide component data libraries, organized by manufacturer's databook, for SEA's thermal and reliability programs. Second, Sedco announced that it's been accepted in IBM's Cooperative Software Program: IBM will offer Sedco's DesignLib libraries to its customers through the IBM sales organization. DesignLibs provide all the data necessary for schematic capture, place and route, and interactive layout on IBM's CBDS system. Additionally, DesignLibs supports Computervision, Mentor Graphics, OrCAD, P-CAD, Racal-Redac, and Zuken pc-board-design data formats.—Michael C Markowitz

ROM-BASED BIOS AND OPERATING SYSTEM RUN MS-DOS PROGRAMS

Award Software Inc (Los Gatos, CA, (408) 370-7979) has combined its BIOS (basic I/O system) ROM with an operating system to help system designers incorporate MS-DOS compatibility in their products. You can obtain the ROS (ROM operating system) package in two versions: One has both software components installed in a ROM; the other has the BIOS in ROM and the operating system on a floppy disk. The ROM version costs less than $100 (100), and the dual-media version costs less than $80 (500). The ROS BIOS is derived from the company's earlier BIOS products and operating system, DR DOS from Digital Research Inc (Monterey, CA). It's compatible with Microsoft Corp's (Redmond, WA) MS DOS 3.3. It also includes some enhancements, such as support for disk partitions as large as 512M bytes and both file- and record-level password protection.—Steven H Leibson

AI DEVELOPMENT SOFTWARE ADDS WINDOWS AND GRAPHICS

The Goldworks II software package lets expert-system developers include windows and graphics in their applications. This new version from Gold Hill Computers (Cambridge, MA, (617) 621-3300) lets you build AI-based applications that interface to conventional applications, spreadsheets, databases, and programming languages. The program is available for use with Sun workstations, IBM PC-compatible computers, and Apple Macintosh II computers. The Goldworks II system architecture includes a menu interface, an external interface, and a developer's interface with hooks for Lisp, C, Lotus 1-2-3, dBase III, and Microsoft Windows. The knowledge base uses frames to represent problems, forward- and backward-chaining rules for reasoning, and object-oriented programming for dividing large problems into manageable subsets. You also get a rule editor, a Multiple Assertion Representation System (Mars) inference engine, and the ability to browse through a graphical representation of your expert system as you develop it. For those who have Goldworks 1.1 and a current service contract, the upgrade to Goldworks II is free. For Goldworks 1.1 owners who don't have a service contract, the upgrade costs $1000. New customers pay $7500 for the first copy; the price drops to $5995 for two copies and $4995 for three copies.—J D Mosley

VIDEO-CONTROLLER BOARD DRIVES FOUR EGA MONITORS AT ONCE

The $1495 4-On-The-Floor EGA video-controller card from STB Systems Inc (Richardson, TX, 75081, (214) 234-8750) plugs into one IBM PC slot and drives as many as four independent IBM EGA (Enhanced Graphics Adapter) or variable-frequency CRT monitors. The full-length board's 1M-byte video memory allows you to put a different display on each monitor in the standard 16-color, 640×350-pixel EGA format as well as in the enhanced-resolution modes of 752×410 and 640×480 pixels. In addition, you can place a second video-controller board in a PC, allowing the computer to use eight monitors as independent information displays. The controller board incorporates firmware that performs monitor activation and switching, and the company supplies Microsoft Windows software drivers with the board for the enhanced-resolution modes.—Steven H Leibson

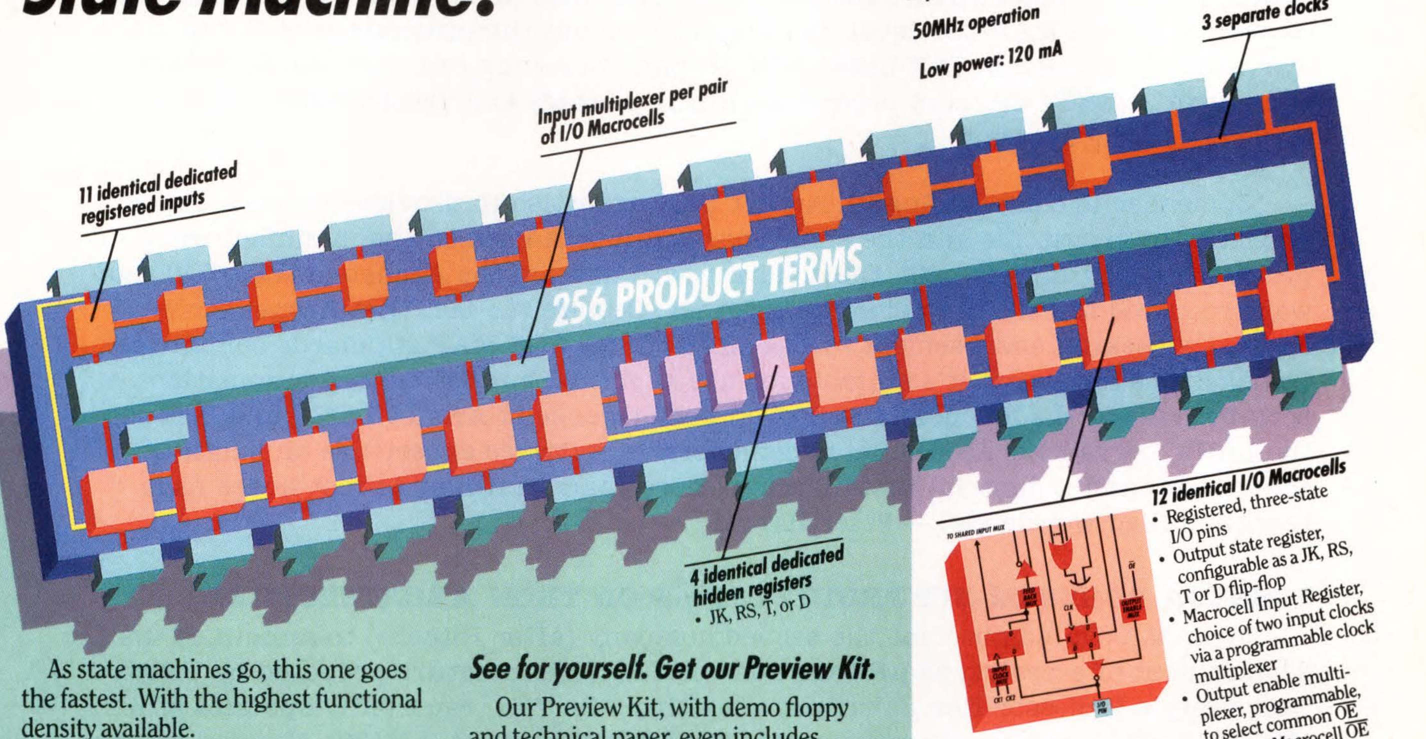
TAPE DRIVE STORES 86M BYTES ON A SINGLE DC2000 TAPE CARTRIDGE

Adding to its MCD series of minicartridge tape drives, 3M (St Paul, MN, (612) 733-1110) now offers the MCD-Series II drive, which can store 86M bytes on a DC2000HD cartridge. The drive records data on 32 serpentine tracks by using a GCR recording scheme. The tape drive owes its storage capacity to its modified QIC-100 data format, which also provides a 98.5k-byte/sec (6M byte/min) data-transfer rate. The drive employs a SCSI port and specs an error rate of less than one in 10^{12} bits. You can purchase evaluation units now; production units will be available in the first quarter of 1989 for $480 (500).—Maury Wright

HYBRID SYNCHRO-TO-DIGITAL CONVERTER HAS TWO CHANNELS

The HSD/HRD1606 16-bit synchro(resolver)-to-digital converter from Natel Engineering Co (Simi Valley, CA, (805) 581-3950) combines two independent Type-II servo-loop tracking converters in a 40-pin TDIP. The converter, accurate to 1.3 arc minutes, transfers data through two independently enabled 8-bit 3-state outputs. It costs $945.—Margery S Conner

Why high performance designers are so excited about the new PLD 7C330 State Machine:



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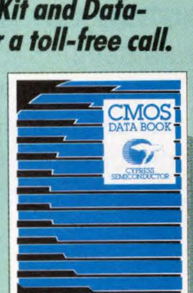

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NEWS BREAKS: INTERNATIONAL

ARCNET FINDS SUPPORT AS A FIELD BUS FOR MAP/TOP NETWORKS

A joint project among Computer Systems Development Ltd (London, UK, TLX 25122; in the US: Marlboro, MA, (617) 460-0330), Cimtel Ltd (Birmingham, UK, TLX 334535), and Comendec Ltd (Birmingham, UK, TLX 334535) is currently under way to develop a computer integrated manufacturing (CIM) system based on the MAP (Manufacturing Automation Protocol), TOP (Technical Office Protocol), and Arcnet networks. At the MAP/TOP level, the project involves the integration of Computer Systems Development's VAX-based MRP-II manufacturing-resource planning software with Cimtel's Cimplan process-planning package and preproduction and factory-scheduling systems.

Comendec is contributing its Arcnet LAN expertise to provide communication between these systems and the shop-floor equipment used in the manufacturing process. As part of this task, the company will develop the Arcnet-to-MAP/TOP gateways required to link the networks together. Despite the fact that Arcnet isn't currently seeking endorsement by the IEEE-SC65C/WG6 MAP standards committee, Comendec believes that it's suitable for use as a field bus for factory automation, both because of the low cost and proven performance of Arcnet LANs, and because the LANs' users have accumulated considerable software experience on existing commercial and industrial installations (more than 1 million Arcnet nodes have been installed worldwide).—Peter Harold

TOSHIBA BASES 32-BIT PROTOTYPE μP ON TRON ARCHITECTURE

Toshiba Corp has become the second company (after Hitachi) to announce the development of a prototype μP based on the TRON architecture proposed by Tokyo University's Professor Ken Sakamura. The chip, the TX1, reportedly operates at 5 MIPS (Hitachi's previously announced TRON device runs at 6 MIPS). Toshiba expects to make the first evaluation samples available by the end of 1988.

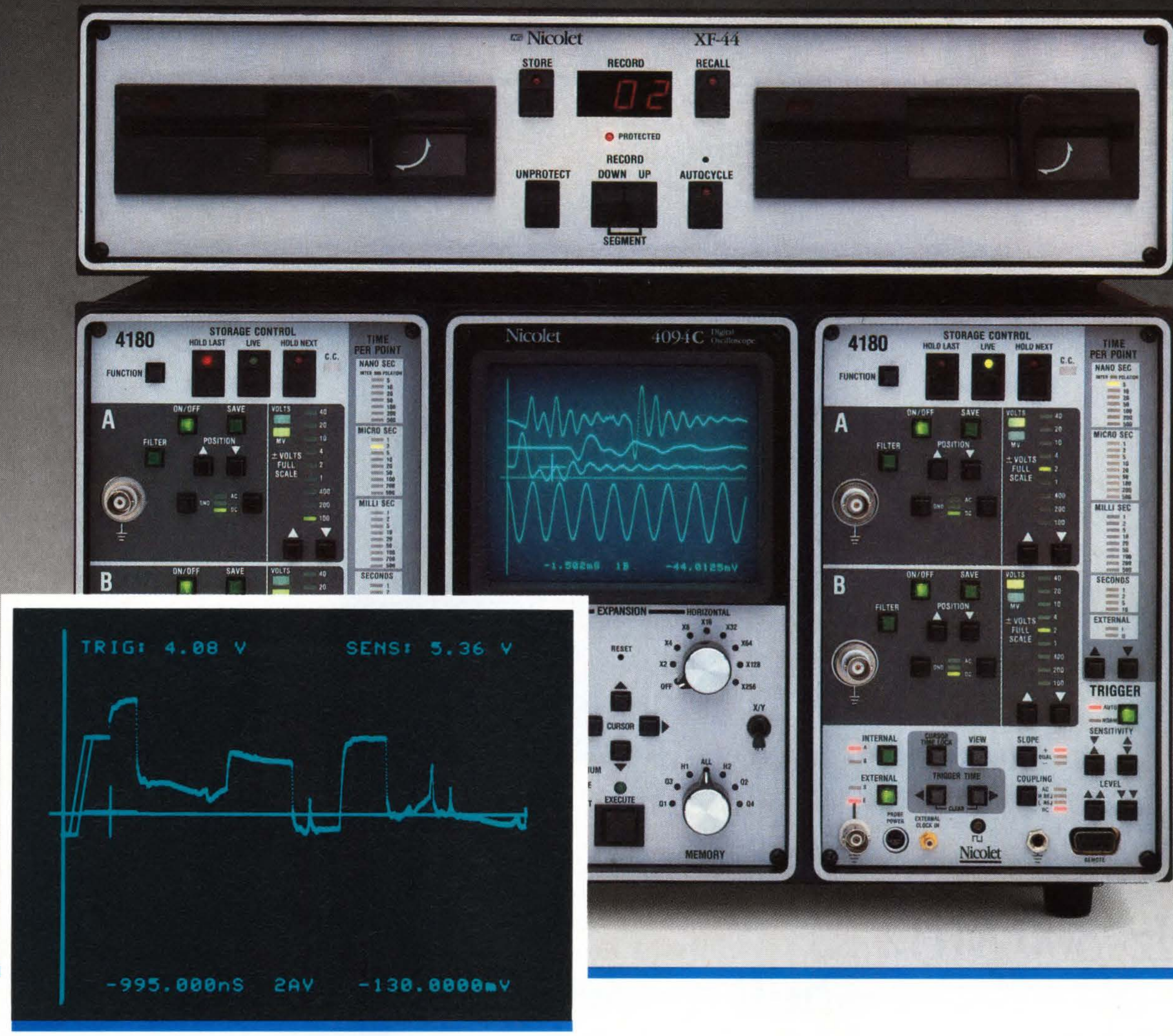
According to reports in the Japanese press, Japanese firms are developing chips based on the TRON architecture because US companies such as Motorola and Intel are reluctant to license Japanese firms to manufacture their μPs. The Japanese companies, therefore, aim to develop their own technology for future-generation microprocessors. Hitachi, Fujitsu, and Mitsubishi have reportedly teamed up to produce a series of TRON μPs to be named G-Micro. NEC, too, is said to have developed a proprietary series of TRON chips called V60 and V70, which have not been applied commercially.—Joanne Clay

77-mW LASER DIODE TARGETS LONG-DISTANCE COMMUNICATIONS

Mitsubishi Electric Corp has developed a 1.5-μm distributed-feedback-type laser diode capable of producing a 77-mW max output—about 1½ times the output of comparable devices. To create the laser diode, the manufacturer combined MOVD (metal organic-chemical vapor deposition) technology and a proprietary method that uses a printed-circuit board and a partially inverted hetero structure.

—Clare Mansfield

Flexible Triggering An Issue?



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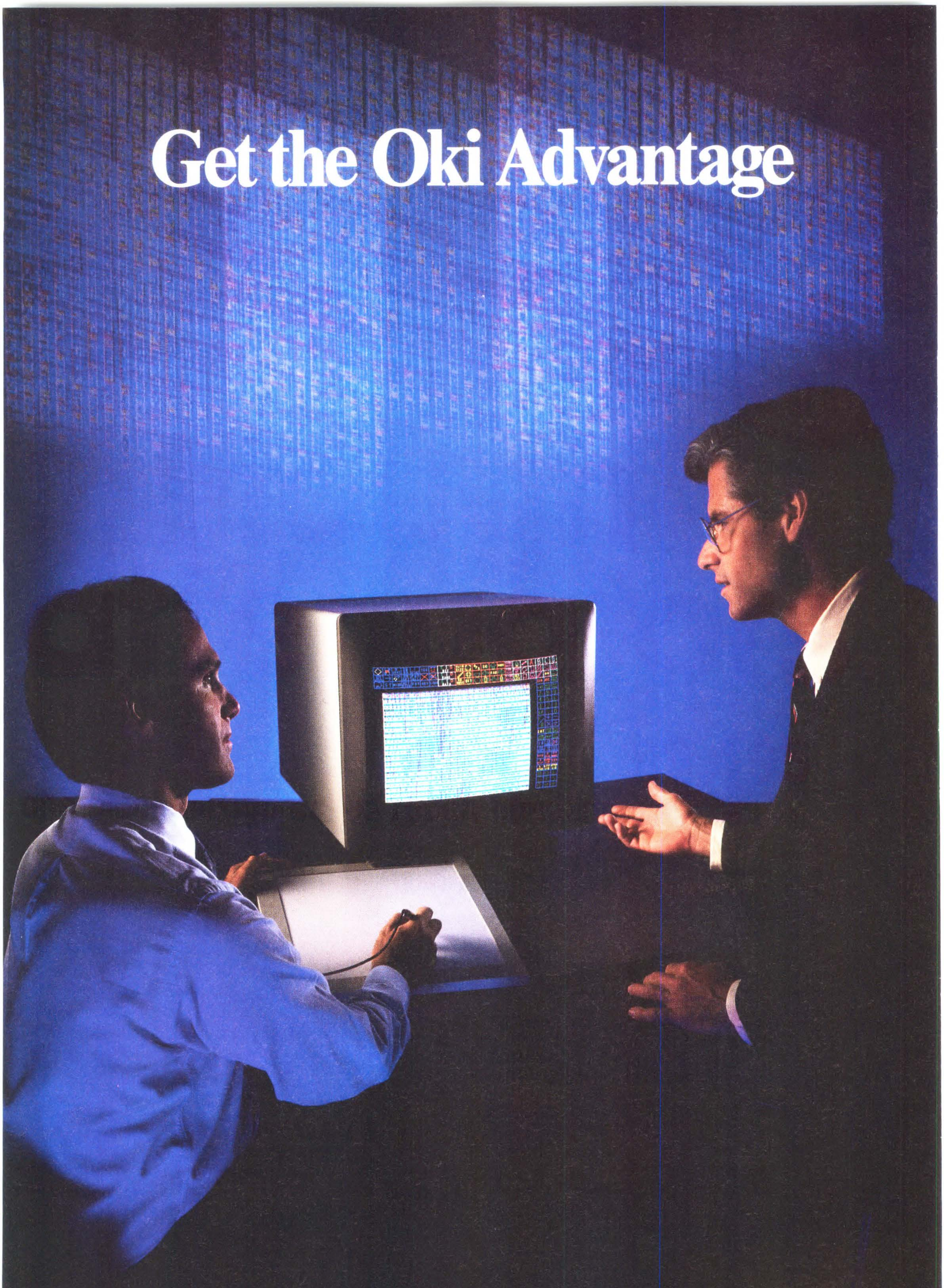

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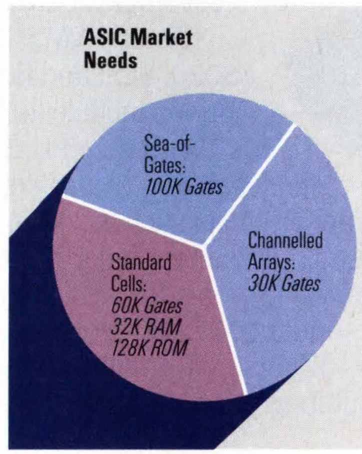

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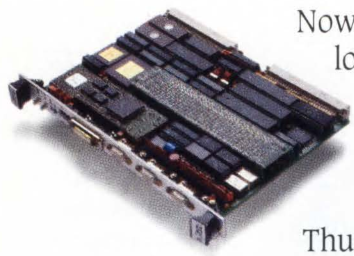

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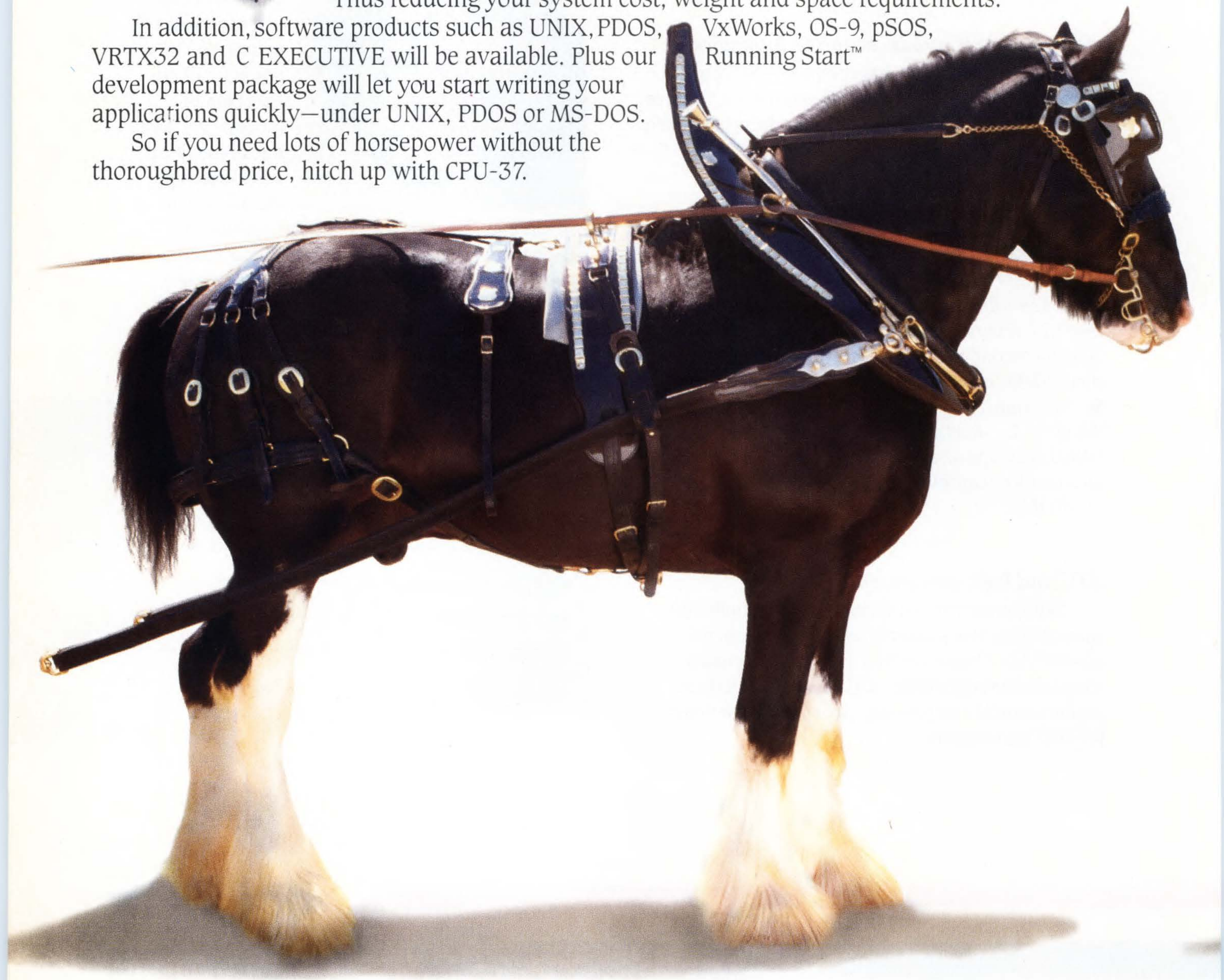

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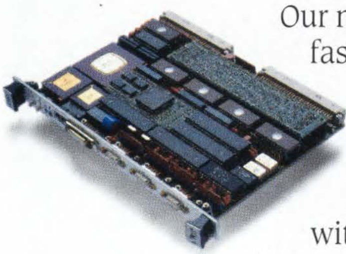

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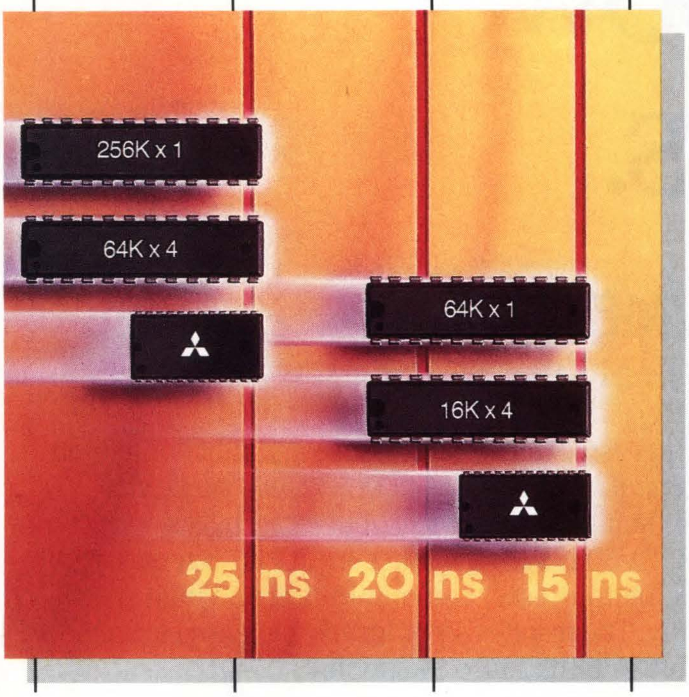

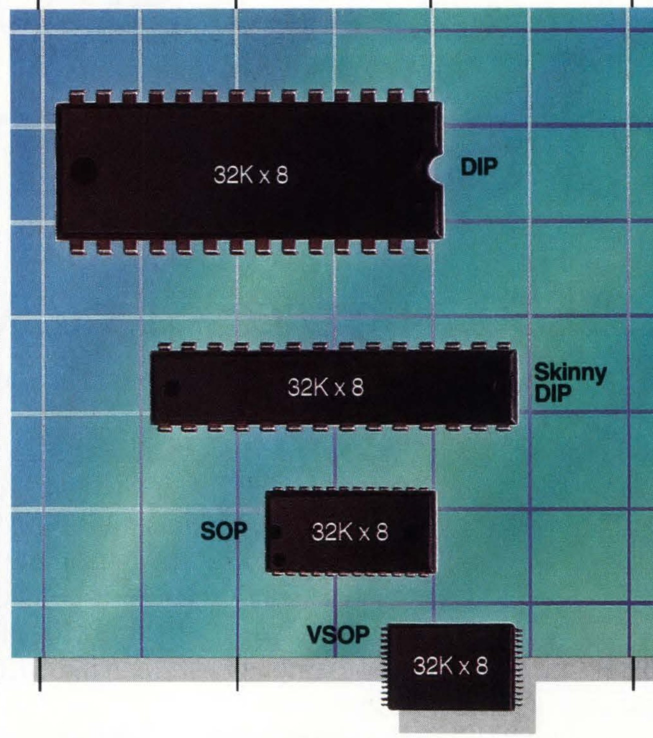

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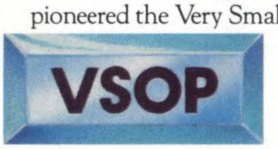

For high density choices and unparalleled speeds, Mitsubishi Electronics' technology leadership in SRAM performance can help you take your designs into the future. For more information, call or write: Mitsubishi Electronics America, Inc., Semiconductor Division, 1050 East Arques Avenue, Sunnyvale, CA 94086. (408) 730-5900.

MITSUBISHI STATIC RAMS			ACCESS TIME (ns)											PACKAGE OPTIONS*			
DENSITY	ORGANIZATION	PART NO.	15	20	25	35	45	55	70	85	100	120	150	PDIP	SOP	SOJ	VSOP
16K	16K x 1	M5M21C67					■	■						■			
	4K x 4	M5M21C68					■	■						■			
64K	64K x 1	M5M5187	■	■	■	■	■	■						■		■	
	16K x 4	M5M5188	■	■	■	■	■	■						■		■	
		M5M5189 ($\overline{OE}$)	■	■	■	■								■		■	
	8K x 8	M5M5165							■		■	■	■	■	■		
		M5M5178				■	■	■						■			
72K	8K x 9	M5M5179				■	■	■						■			
256K	256K x 1	M5M5257			■	■	■	■						■		■	
		M5M5260 ($\overline{OE}$)			■	■								■		■	
	64K x 4	M5M5258			■	■	■	■						■		■	
	32K x 8	M5M5255 (CS/$\overline{CS}$)							■	■	■	■	■	■	■		
		M5M5256							■	■	■	■	■	■	■		■

*PDIP: Plastic DIP SOP: Small-Outline Gull-Wing SOJ: Small-Outline J-Lead VSOP: Very-Small-Outline-Package
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SIGNALS & NOISE

DSO reaches 2G samples/sec

After reading the August 4, 1988, Product Update about the Tektronix 2440 digital oscilloscope (EDN, pg 90), I feel compelled to point out an error.

I am referring to the alleged statement by Tektronix that the Model 2440 has "the industry's highest real-time sampling rate—500M samples/sec."

In November 1986, Hewlett-Packard introduced the HP 54111D, which has a sample rate of 1G sample/sec on both channels. This rate is twice the sampling rate of the Tektronix 2440. Since the introduction of the 54111D, HP designers have devised a method for multiplexing both of the instrument's channels so that the instrument samples at 2G samples/sec on both channels. (Details of this method can be found in HP product note HP 54111D-1.)

Considering the importance of sampling rate, inasmuch as that single specification determines the single-shot performance of a digital oscilloscope, I think that it would be of great service to you and your readers to print a correction.

Thomas E Vos
General Manager
Colorado Springs Div
Hewlett-Packard
Colorado Springs, CO

(Ed Note: The error was EDN's: We inadvertently printed the Tektronix spokesman's statement out of context. The full statement was: "Tektronix believes that the 2440 has the highest real-time sampling rate of any portable, 8-bit-resolution DSO in its price class.")

A μP/memory wish list

I would like to make an appeal in your columns for semiconductor manufacturers to get their acts together. I mean in particular that those who specialize in making microprocessors should coordinate more closely with those who make memory chips.

I am sure many designers have the same frustrating experience when putting together a product that has a μP, a small boot ROM, and a lot of dynamic RAM, such as a personal computer.

It would be very nice if:

- 16- or 32-bit μPs could boot from a single byte-wide ROM.
- The same μPs could output addresses intended for dynamic RAM multiplexed to suit those DRAMs. It should not be difficult for the code that runs the boot ROM to set up the multiplexing for the present generation of 1M-bit DRAMs or for future ones of greater density.
- The μP could put out signals to time the DRAM address strobes (RAS and CAS).
- The μP could refresh the DRAM.
- The μP could take advantage of static-column RAMs, which can cycle very quickly through addresses on the same page.

It would be nice too if certain memory-chip makers could manage to reduce the deselect time to match that required by present μPs.

P S—EDN is the only electronics magazine that really seems interested in actual design engineering. I think that a section inviting "wouldn't it be great if someone would make . . . " letters would get a big response. It might also help advance the state of the art.

David Cockerell
London, UK

(Ed Note: Signals and Noise is a

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forum for whatever comments readers have about the electronics industry. Readers are invited to send their "wouldn't it be great if someone would make . . . " letters to the Signals & Noise Editor, EDN, 275 Washington St, Newton, MA 02158.)

HC- or AC-type logic solves ground bounce

The problem of ground bounce in high-speed CMOS logic is primarily due to the speed of the logic driving capacitive lines. The inductance of the lead from the chip to the ground plane is becoming significant in how it affects other outputs and perhaps inputs. One approach offered by some vendors is to offer similar parts with different pinouts to reduce this inductance. However, very few vendors and parts are available.

The problem is exacerbated by the adherence to logic levels initiated in the days of TTL (before LS) and single-layer boards. An alternative solution I have not seen in the trade literature is applicable to boards with GND and V_{CC} planes. The solution is to use HC- or AC-type logic, which has a wide range of parts, is easily interfaced, is often not any problem, and has a much wider noise margin and low logic levels. Also, this logic family is better for producing logic signals from analog waveforms—for example, oscillators and phase-locked loops—or doing other analog tricks.

Frank W Bell
World Research Institute for Science and Technology
Long Island City, NY

Kudos for the shirt-pocket DMM

The Technology Update entitled "Inexpensive, shirt-pocket DMMs are smaller and handier than ever" by Charles Small (EDN, June 9, 1988, pg 77) struck home. I have had a Radio Shack Micronta 22-171 shirt-pocket DMM for about a year now.

The small size and autoranging keep the instrument handy for quick checks on lithium batteries, power supplies, and auto accessories. The beep-continuity function tests RS-232C cabling quickly without my having to look at the meter.

Although it lacks "sophisticated" features, the instrument's simple controls, autoranging, and attached leads make this an extremely valuable tool for a mere $25 investment. It is now a necessity in my attaché case, along with a calculator, small tools, an ARRL repeater directory, and other essentials.

Thank you for the great magazine.

Courtland G Sandberg
Project Engineer
ARMTEC Ind Inc
Manchester, NH

Singing the big-business blues

Regarding the editorial "The service-economy myth" (EDN, December 10, 1987, pg 53), this swipe at small business is unbecoming. I have suffered considerable economic indignity at the hands of one of the world's largest manufacturing enterprises—GM. For the period of the warranty on one of its vehicles, it replaced *failed* defective parts with *known* defective parts until the warranty expired. Then it became my problem. That is outside the intent of any honorably drawn warranty—and I was unable to hold the company accountable. As you may have guessed, the company did not steal away in the dead of night, it simply stonewalled it and refused to hear my complaint.

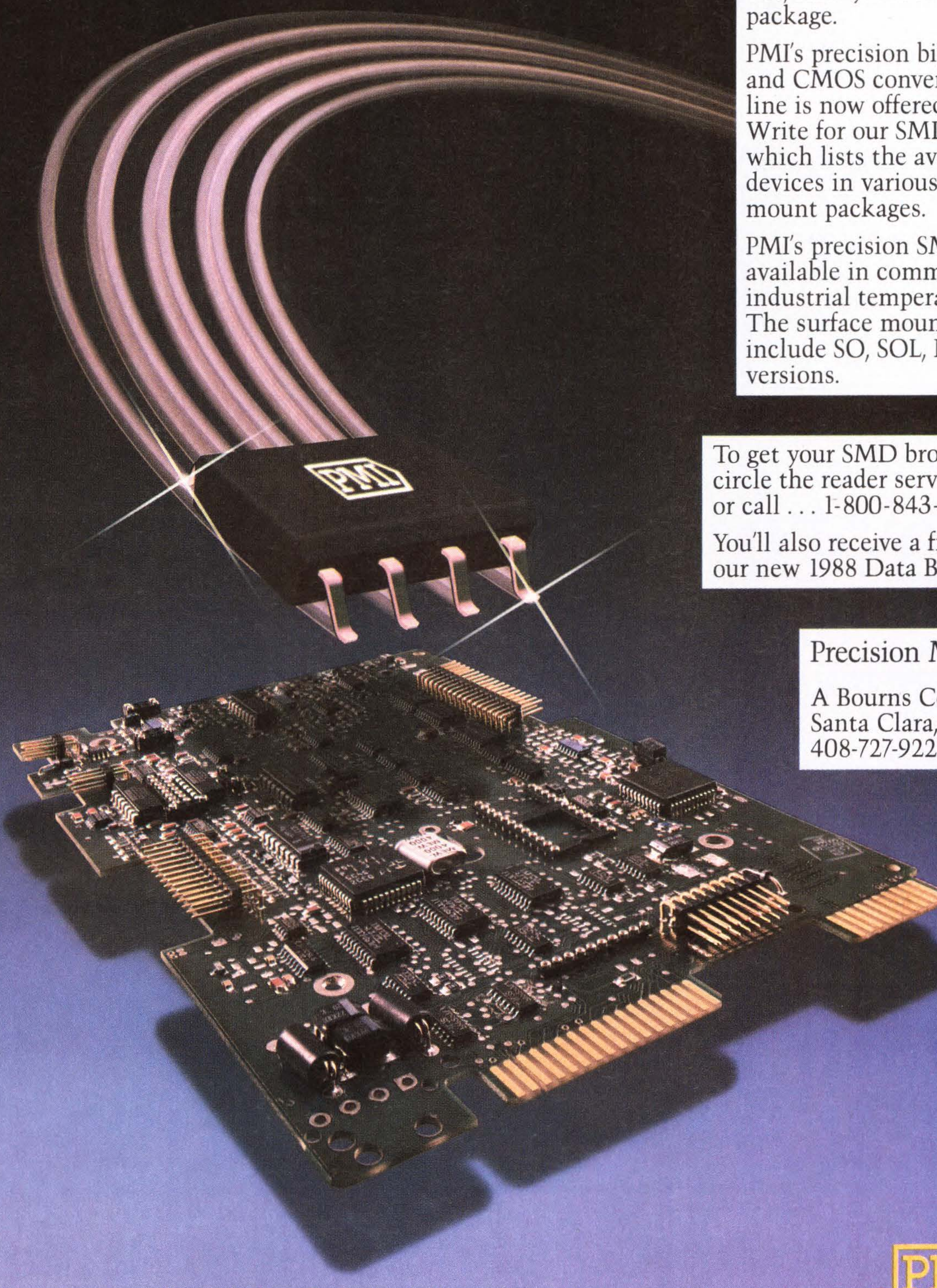
So how does one hold a mega-monolith like GM accountable, tell me?

Allen N Wollscheidt
Columbus, IN

WRITE IN

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

Finally . . . Precision In Surface Mount Devices



Yes, finally! Precision in a small package.

PMI's precision bipolar analog and CMOS converter product line is now offered in SMD. Write for our SMD brochure which lists the availability of 65 devices in various surface mount packages.

PMI's precision SMDs are available in commercial and industrial temperature ranges. The surface mount offerings include SO, SOL, LCC, and PLCC versions.

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The precision solution.

CIRCLE NO 42

INTRODUCING TEK'S 20 GHZ, MULTICHANNEL COMPREHENSIVE MEASUREMENT SYSTEM.

Imagine characterizing GaAs, ECL, or high-speed TTL circuits with 1 picosecond repeatability and .01 picosecond sample interval.

Or acquiring not one or two, but up to 68 channels of waveform data simultaneously. All under manual or program control.

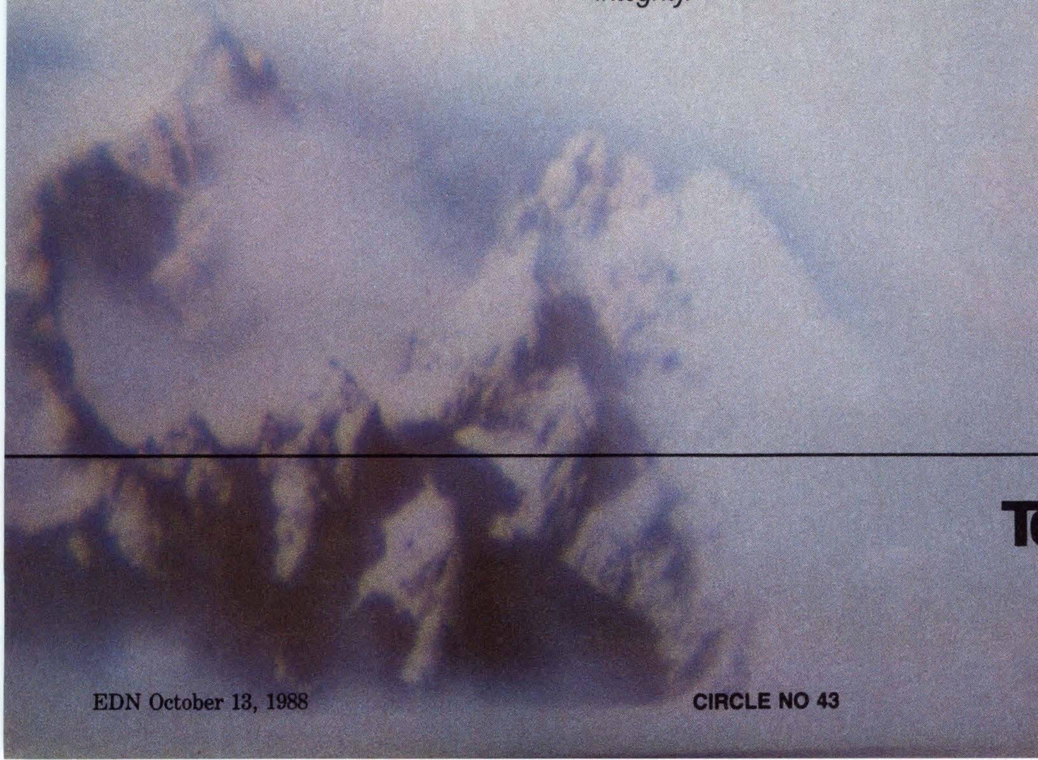
Imagine reducing propagation delay measurements to the push of a button. Or performing single-ended TDR and—for the first time—true differential TDR, *with unprecedented accuracy.*

Nothing else lets you work at the leading edge with so much confidence. *The new Tektronix 11800 Series makes previously difficult measurements routine. Even if you use it infrequently, you'll find its operation straightforward and unforgettable.*

Measurement readouts on the 11800 Series are continuous—not just misleading "snapshots." Mean and standard deviation statistics on each measurement give you a true picture of measurement integrity.

With its maximum 136 acquisition channels, complete programmability, extensive onboard waveform processing and unparalleled accuracy, the 11800 Series is the clear choice for designers and engineers working at the leading edge of technology.

When there's no room for error, count on Tek. *For more information on these and other Tek scopes, contact your local Tek sales representative, or call 1-800-835-9433, X170.*



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COMMITTED TO EXCELLENCE


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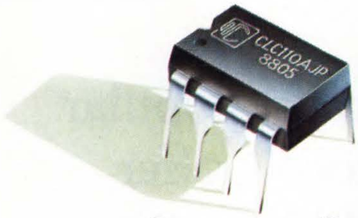
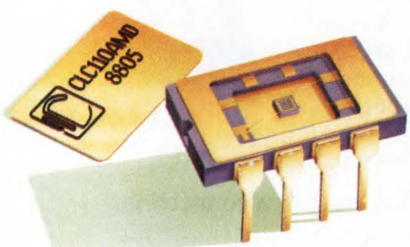


400ps rise time and −60dBc distortion at 50MHz. Suddenly, the buffer gets interesting!



This is a buffer breakthrough! Comlinear introduces the CLC110 Monolithic Buffer Amplifier for phenomenal speed *and* outstanding accuracy all in a single high-performance part.

The CLC110 features a *closed-loop* unity-gain design that's so unique, it's patented. This buffer is fast! The −3dB bandwidth is 730MHz (0.5Vpp) and the settling time is a mere 5ns to 0.2%. And it's accurate! With very low 2mV offset voltage, 20μV/°C drift and −60dBc distortion at 50MHz (2Vpp into 100Ω).

The CLC110 is ideal for high-speed line driving and video distribution. It's also a great choice for driving capacitive loads, especially in the newest 100 to 200MSPS flash A/D converters; its fast 750ps group delay, 800V/μs slew rate and 400ps rise time make it excellent for op amp feedback loops as well.

Try the CLC110 in your next design for both the speed and accuracy you need. Without compromise.

Comlinear Corporation

Solutions with speed

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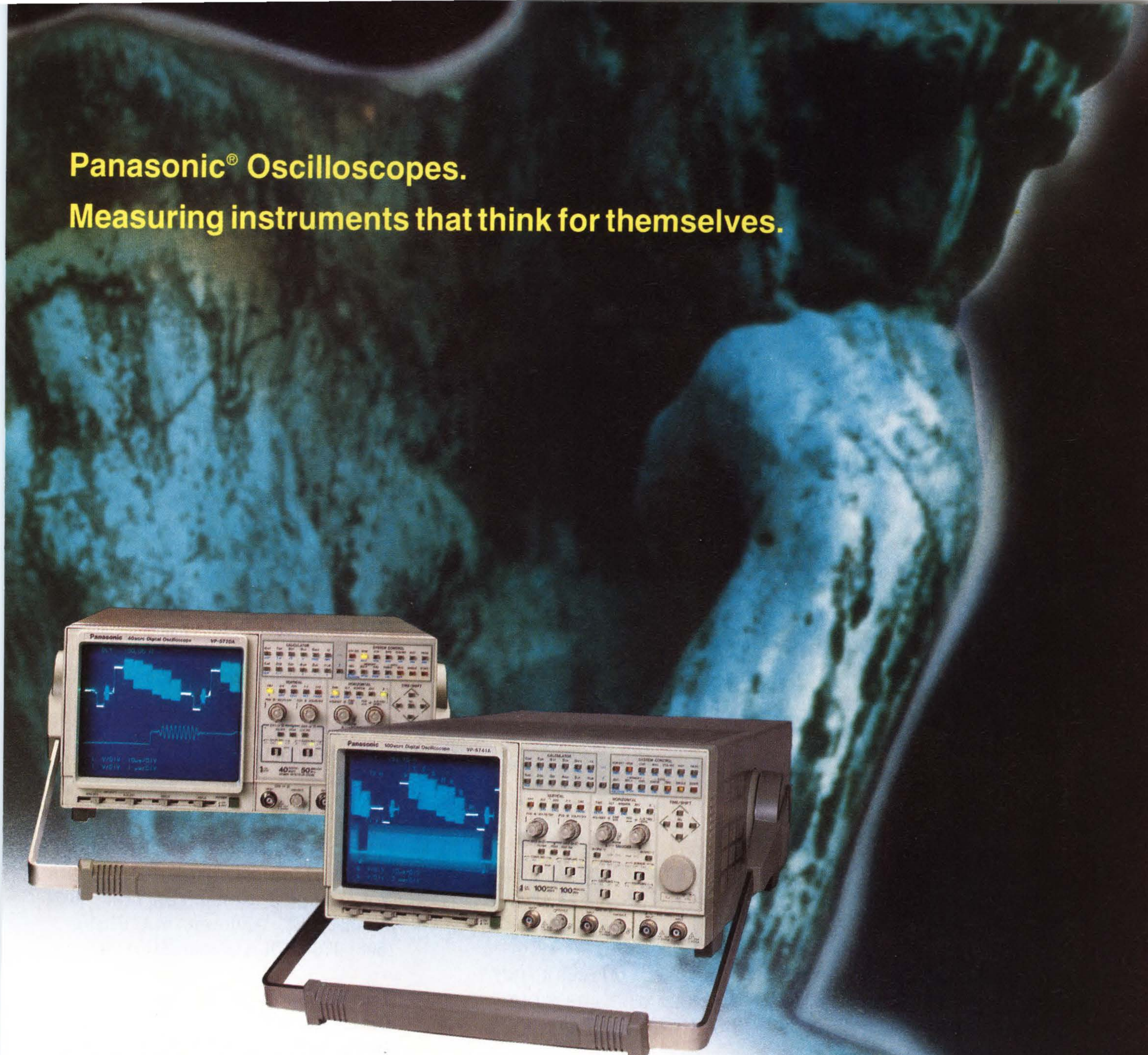
Fort Collins, Colorado 80525
(303) 226-0500

CIRCLE NO 45



If you're in the market for a smart scope, take a close look at two brilliant performers from Panasonic. The 40 MS/s VP-5720A and the 100 MS/s VP-5741A digital oscilloscopes share a penchant for hard work and the ability to do a lot of thinking on your behalf.

They have the intelligence to run a 1,000 step program and feature built-in math packs that make short work of even the longest calculations. And to help you see more of the good work they do, both models feature 7-inch CRTs that provide plenty of on-screen memory...up to 10K for the VP-5741A and up to 8K for the VP-5720A.

Both scopes are also engineered to handle a wide scope of applications – like high-speed measurement and analysis of electronic components and equipment, machines, production line, mechatronics and for research. For added versatility, each includes a standard GP-IB interface as well as yes/no functions.

Each scope also allows for 3 waveforms to be stored in memory. With an expansion option, you can store up to 20 and increase your programming ability from 10 programs to 45. And, in the analog mode the VP-5720A performs at 50 MHz, and the VP-5741A performs at 100 MHz.

Best of all, the VP-5720A and VP-5741A back their brainpower with Panasonic quality staying power. And they're engineered to deliver solid, dependable service over a wide range of applications. So they're very smart. And very strong.

For more information or a demonstration, contact your local Panasonic representative or: Panasonic Factory Automation Company, Instrumentation Dept., 50 Meadowlands Parkway, Secaucus, NJ 07094. (201) 392-4050.

Panasonic.
Factory Automation

CIRCLE NO 46

CALENDAR

Worst-Case Circuit Analysis (seminar), San Francisco, CA. Design and Evaluation, 1000 White Horse Rd, Suite 304, Voorhees, NJ 08043. (609) 770-0800. October 17 to 19.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Atlanta, GA. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. October 18 to 21.

Computer Graphics Invitational Computer Conference (ICC), Dallas, TX. Suzanne Hubner, B J Johnson & Associates, 3151 Airway Ave, C-2, Costa Mesa, CA 92626. (714) 957-0171. October 20.

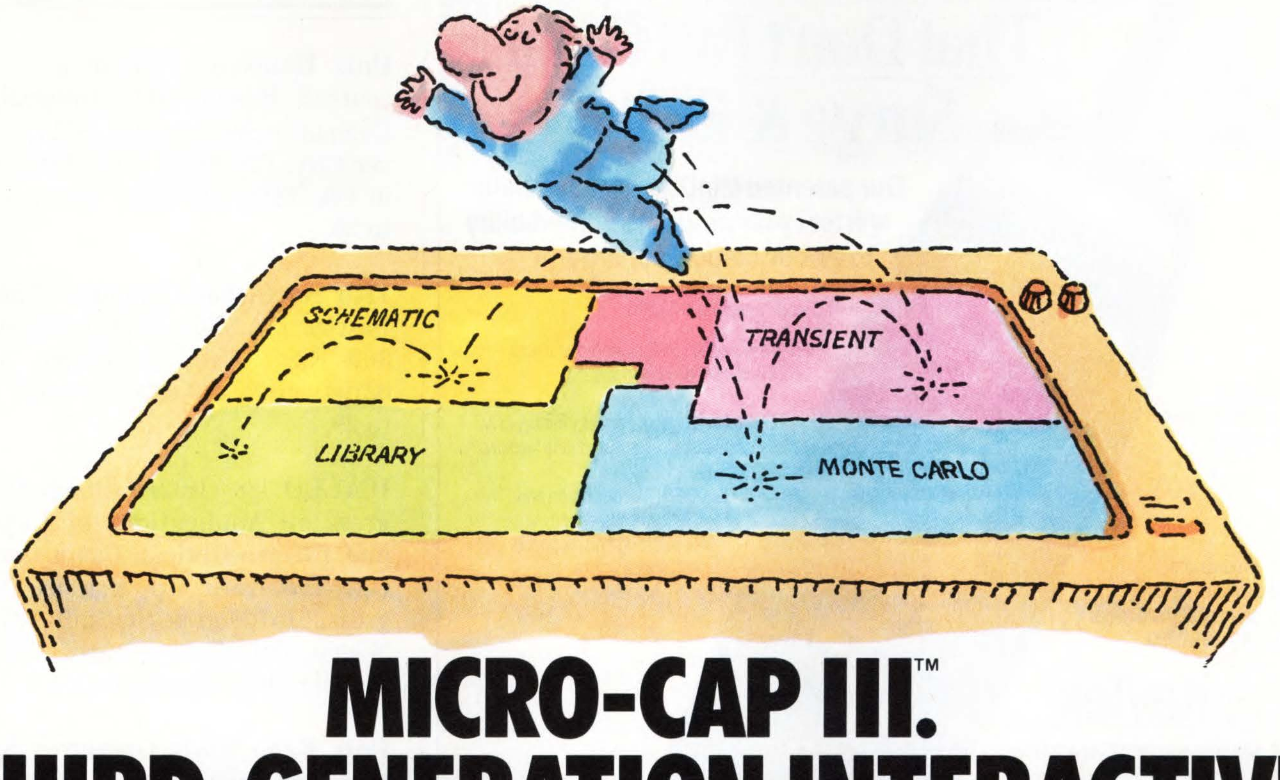
OEM Peripheral Invitational Computer Conference (ICC), Bloomington, MN. Suzanne Hubner, B J Johnson & Associates, 3151 Airway Ave, C-2, Costa Mesa, CA 92626. (714) 957-0171. October 20.

CASE Benchmarks: A Product Comparison Seminar, Boston, MA. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3870. October 24 to 26.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Atlanta, GA. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. October 24 to 27.

OEM Peripheral Invitational Computer Conference (ICC), Westlake Village, CA. Suzanne Hubner, B J Johnson & Associates, 3151 Airway Ave, C-2, Costa Mesa, CA 92626. (714) 957-0171. October 25.

11th Annual Newport Conference on Fiberoptics Markets, Newport, RI. Kessler Marketing Intelligence, America's Cup Ave at 31 Bridge St, Newport, RI 02840. (401) 849-6771. October 25 to 26.



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THIRD-GENERATION INTERACTIVE CIRCUIT ANALYSIS. MORE POWER. MORE SPEED. LESS WORK.

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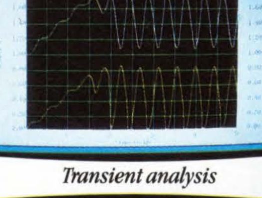
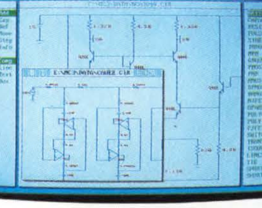
The program's window-based operation and schematic editor make circuit creation a breeze. And super-fast SPICE-like routines mean quick AC, DC, Fourier and transient analysis—right from schematics. You can combine simulations of digital and analog circuits via integrated switch models and macros. And, using stepped component values, rapidly generate multiple plots to fine-tune your circuits.

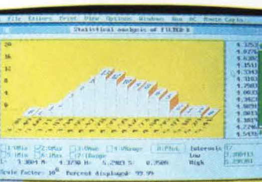
We've added routines for noise, impedance and conductance—even Monte Carlo routines for statistical analysis of production yield. Plus algebraic formula parsers for plotting almost any desired function.



Transient analysis



Schematic editor



Monte Carlo analysis

Modeling power leaps upward as well, to Gummel-Poon BJT and Level 3 MOS—supported, of course, by a built-in Parameter Estimation Program and extended standard parts library.

There's support for Hercules,® CGA, MCGA, EGA and VGA displays. Output for laser plotters and printers. And a lot more.

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CALENDAR

Unix Hands-on Workshop (short course), Boston, MA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. October 25 to 28.

11th Northeast Computer Faire, Boston, MA. The Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. October 27 to 29.

ICALEO '88 (International Congress on Applications of Lasers and Electro-Optics), Santa Clara, CA. The Laser Applications Congress, 5151 Monroe St, Suite 102W, Toledo, OH 43623. (419) 882-8706. October 30 to November 4.

Unix Expo (Unix Operating System Exposition and Congress), New York, NY. National Expositions, 15 W 39th St, New York, NY 10018. (212) 391-9111. October 31 to November 2.

CASE for Data Modeling (seminar), New York, NY. Technology Transfer Institute, 741 Tenth St, Santa Monica, CA 90402. (213) 394-8305. November 2 to 4.

1988 IEEE GaAs IC Symposium, Thousand Oaks, CA. John Selin, registration chairman, Raytheon Co, Equipment Div, MS E21, 430 Boston Post Rd, Wayland, MA 01778. (617) 440-5532. November 6 to 9.

GOMAC '88 (Government Microcircuits Applications Conference), Las Vegas, NV. Palisades Institute for Research Services, 201 Varick St, Rm 1140, New York, NY 10014. November 8 to 10.

Electronica, Munich, West Germany. Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450. (201) 652-7070. November 8 to 12.

ANALOG DEVICES

15μV max Offset Voltage Ultralow Drift Op Amp

AD707

FEATURES
Very High dc Precision
- **15μV max Offset Voltage**
- **0.1μV/°C max Offset Voltage Drift**
- **0.35μV p-p max Voltage Noise (0.1Hz to 10Hz)**
- **8V/μV min Open-Loop Gain**
- **0.32μV/V max CMRR**
- **1μV/V max PSRR**
- **1nA max Input Bias Current**
- **1nA max Input Offset Current**

Dual Version Available: AD708

PRODUCT DESCRIPTION

The AD707 is a low cost, high precision op amp with state-of-the-art performance that makes it ideal for a wide range of precision applications. The offset voltage spec of less than 15μV is outstanding for a bipolar op amp, as is the 1.0nA maximum input offset current. The top grade is the first bipolar monolithic op amp to offer a maximum offset voltage drift of 0.1μV/°C, and offset current drift and input bias current drift are both specified at 25pA/°C maximum.

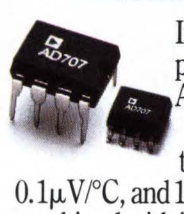
The AD707's open-loop gain is 8V/μV minimum over the full ±10V output range when driving a 1kΩ load. Maximum input voltage noise is 350nV p-p (0.1Hz to 10Hz). CMRR and PSRR are 130dB and 120dB minimum respectively.

The AD707 is available in versions specified over commercial, industrial and military temperature ranges. It is offered in 8-pin plastic mini-DIP, small outline, hermetic cerdip and hermetic TO-99 metal can packages. Chips and Mil Standard/883 parts are also available.

APPLICATION HIGHLIGHTS

1. The AD707's 13V/μV typical open-loop gain and 0.1μV/V typical common-mode rejection ratio make it ideal for precision instrumentation applications.
2. The precision of the AD707 makes tighter error budgets possible at a lower cost.
3. The low offset voltage drift and low noise of the AD707 allow the designer to amplify very small signals without sacrificing overall system performance.
4. The AD707 can be used where chopper amplifiers are required, but without the inherent noise and application problems.
5. The AD707 is an improved pin-for-pin replacement for the OP-07, OP-77 and the LT1001.

HERE'S THE MOST ACCURATE SOURCE OF INFORMATION ON THE WORLD'S MOST ACCURATE BIPOLAR OP AMP.



If your analog applications demand precision performance, then you should demand our new AD707 – the world's best dc precision op amp.

The AD707 is the first bipolar monolithic to offer a maximum offset voltage drift of only 0.1μV/°C, and 15μV maximum offset voltage. These features, combined with its ultralow 0.35μV p-p voltage noise, allow the AD707 to amplify extremely small signals without sacrificing system performance.

The AD707 also provides an open-loop gain of 13V/μV, which is the highest of any precision op amp, and unsurpassed 140dB CMRR and PSRR. So it's ideal for a wide range of precision applications, including instrumentation and automatic test equipment.

All this precision makes it easy for you to work within tight error budgets. And because the AD707 is available at a low cost, you can easily work within your design budget, too. Versions start at only $1.25 (in 100s).

For an even more accurate description of what the AD707 can do for you, call Applications Engineering at (617) 935-5565, Ext. 2628 or 2629.

Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

ANALOG DEVICES

Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; Headquarters: (617) 329-4700; California: (714) 641-9391, (619) 268-4621, (408) 559-2037; Colorado: (719) 590-9952; Maryland: (301) 992-1994; Ohio: (614) 764-8795; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094; Washington: (206) 251-9550; Austria: (222) 885504; Belgium: (3) 237 1672; Denmark: (2) 845800; France: (1) 4687-34-11; Holland: (1620) 81500; Israel: (052) 911415; Italy: (2) 6883831, (2) 6883832, (2) 6883833; Japan: (3) 263-6826; Sweden: (8) 282740; Switzerland: (22) 31 57 60; United Kingdom: (932) 232222; West Germany: (89) 570050

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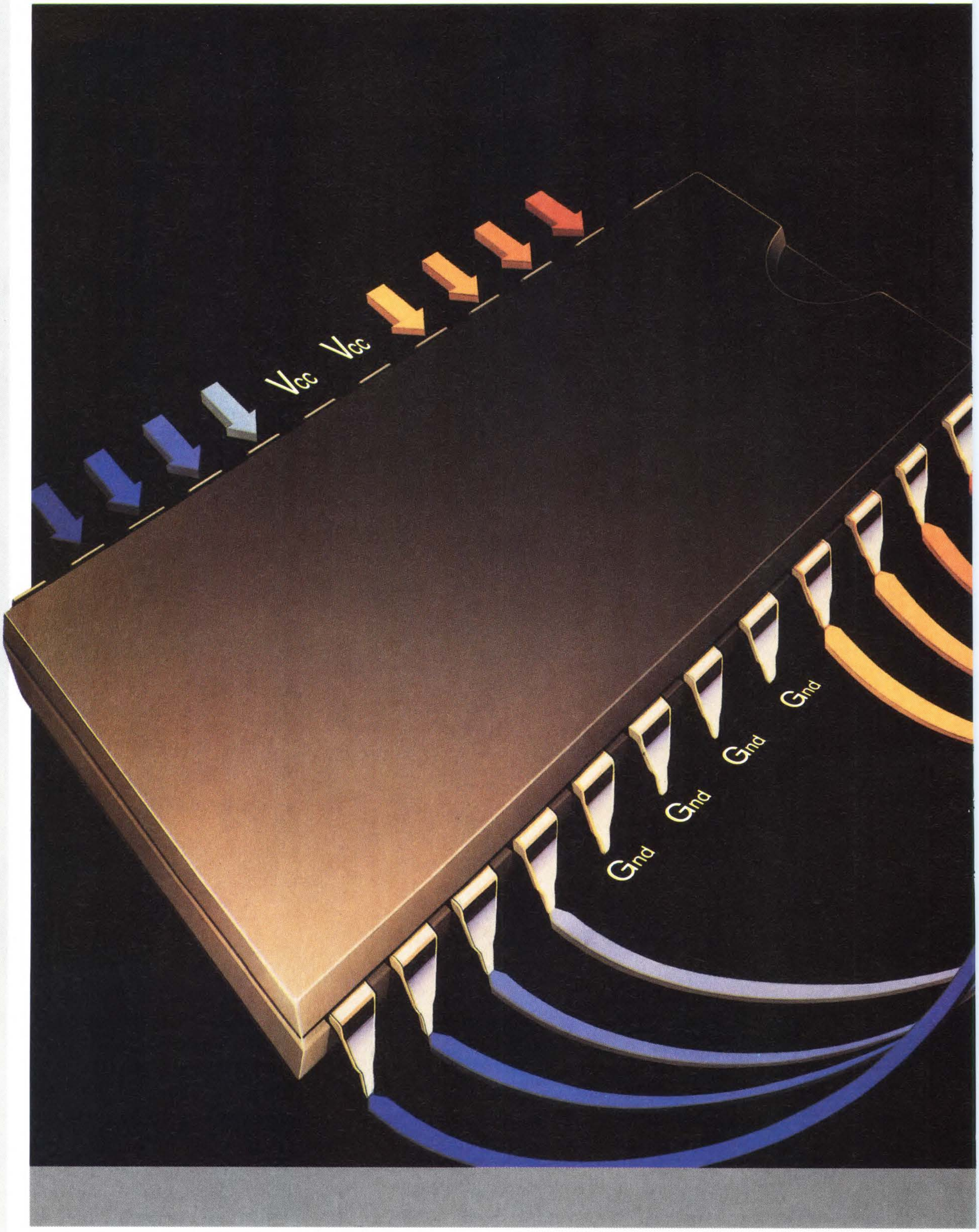

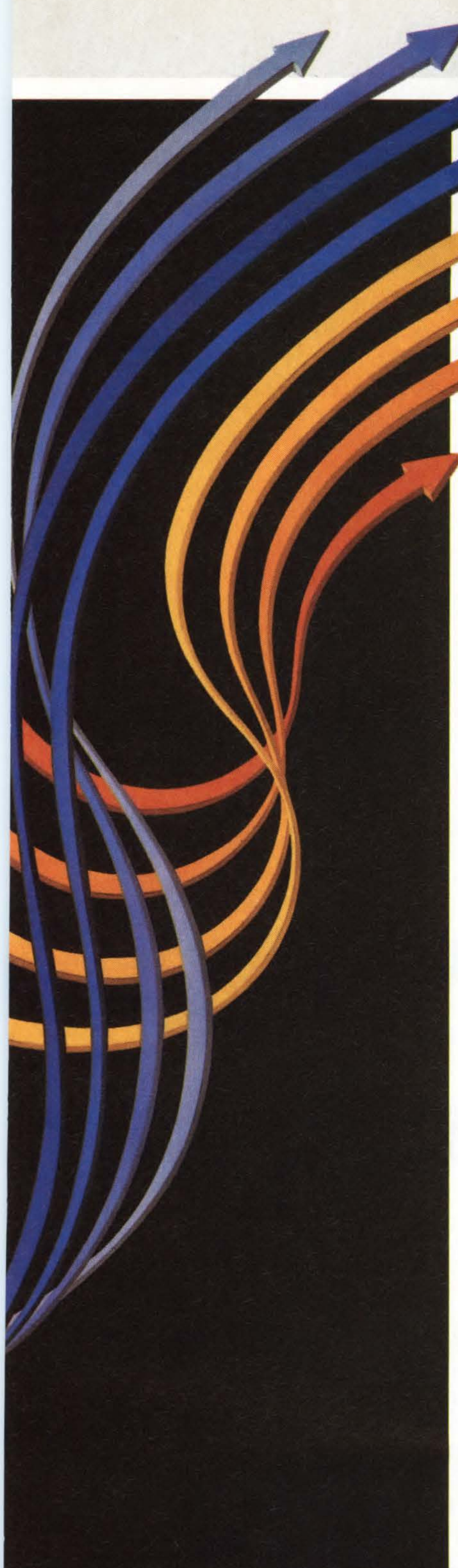

CIRCLE NO 53

Only HP can put real teeth into faster

Test development and execution speed. We know they're your top priorities. HP BASIC,* combined with our range of controllers and instrumentation, is the answer. Even if you're running on MS™DOS or the UNIX™ operating system. And of course, it's all backed by HP's measurement expertise, and the product reliability you've come to count on from an industry leader.

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It's no secret that a critical element of automated instrument control is fast development time. That's where HP BASIC really shines. With power, versatility and ease of use. We invite you to find a better instrument control language.

A few examples:

■ Fast program development with interactive editing, syntax checking and the ability to search and replace strings, or move blocks of code easily.

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■ Structured programming lets you make your program modular with independent subprograms which can be re-used in other applications. Constructs like CASE statements, IF-THEN-ELSE, WHILE, REPEAT-UNTIL and LOOP are useful for rapid program development and invaluable for program maintenance.

■ Powerful computation lets you take advantage of a full range of matrix manipulations such as multiplication, inversion and scalar operations. HP's complex number implementation allows for powerful arithmetic operations.

■ Graphic capabilities are simple to program, yet powerful. One program statement can draw axes or grids, a second will plot your data, a third will label your plot and a fourth will provide a permanent copy.

HP Controllers: The right horsepower for the job.

Hewlett-Packard provides a wide range of instrument controllers and operating systems to meet your performance needs, allowing you to choose the most cost effective controller for your job.

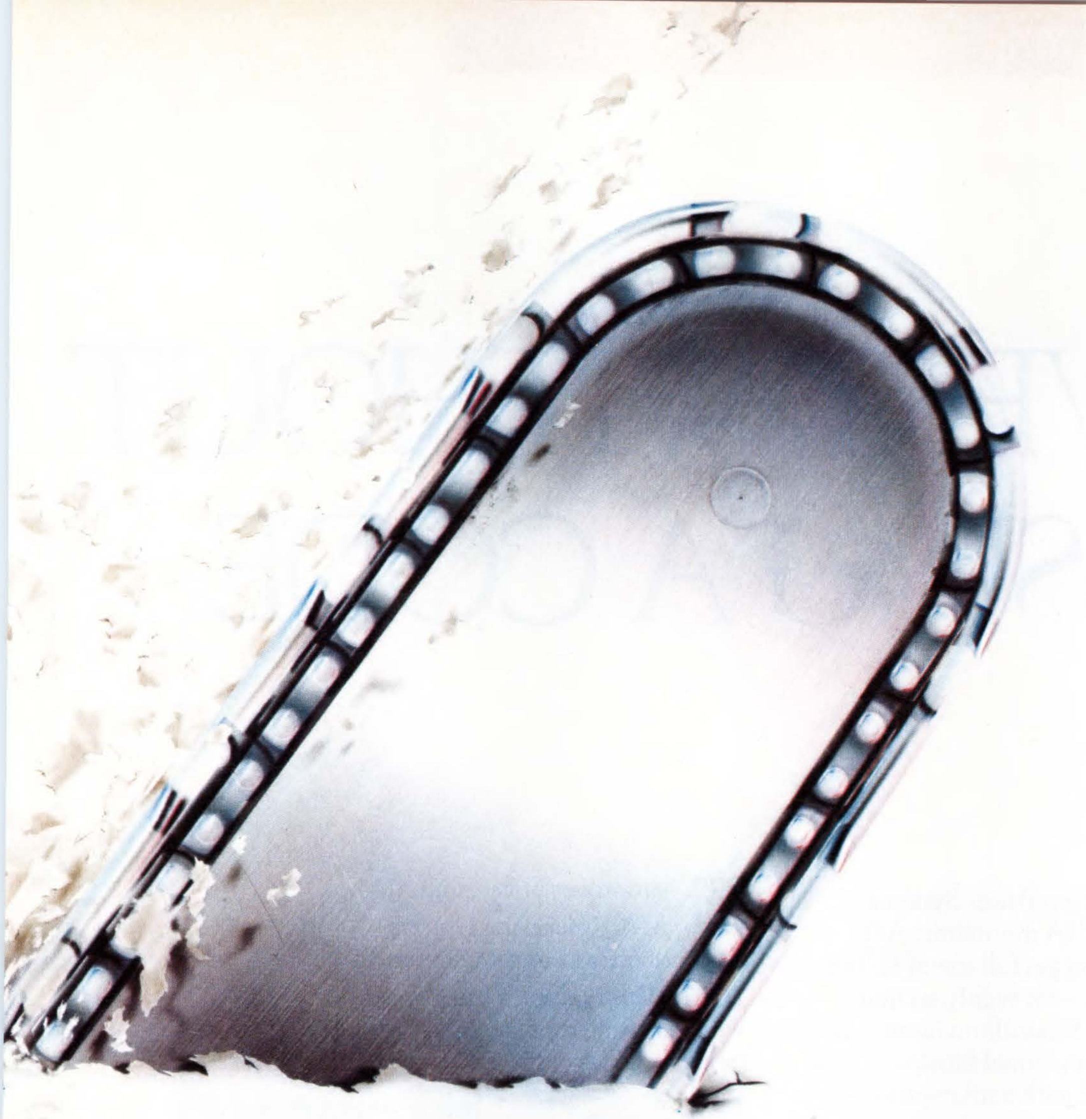
Just look:

■ Personal computers; the HP BASIC Language Processor allows you to use HP BASIC on the world's most prevalent operating system, MS DOS. It's available for the HP VECTRA or the IBM PC-AT.

*Sometimes called Rocky Mountain BASIC or BASIC 5.0.

we never stop asking

"What if...



test development.

■ Dedicated controllers up to 4 MIPS, HP's Series 300 controllers provide a dedicated, high performance system for maximum I/O throughput.
■ HP-UX workstations. HP BASIC will also be available for use in the Series 300 HP-UX environment. Our implementation combines the ease-of-use and performance of HP BASIC with the full networking, multitasking and windowing capabilities of the UNIX operating system.

No matter the controller demand, HP makes it in the optimum package.

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Ask for our free videotape on HP BASIC or a brochure on HP instrument controllers. Learn how Hewlett-Packard can help you cut test development time significantly.

HEWLETT PACKARD

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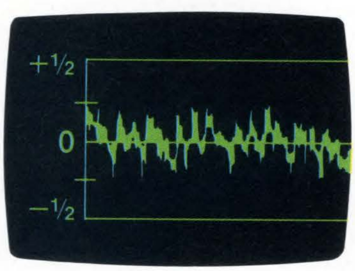
With Micro Power Systems' MP574A monolithic A/D converter, you get full use of 12-bits—for all grades—for highly accurate conversions. It stands on its own as a full A to D functional block or it may be interfaced with a microprocessor.

Our MP574A converter has 25μs guaranteed conversion time for faster throughput. It also has the linear performance and low power consumption of Bi-CMOS technology. No special selection is needed for ±12V to ±15 VDC supply operation. Convenient, off-the-shelf availability is also a plus. And Micro Power provides added values like application assistance and free, on-site, technical seminars.



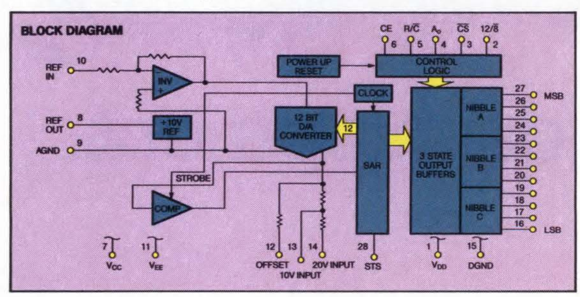
Differential Non-Linearity is less than ± 0.5 LSB over an analog input range of 0 to 10V, assuring no missing codes.

Additional features include:

Digital I/O Interfaces are True TTL—Improves noise immunity

10V, 5MA Reference Output—Easier to use as a system reference

200 ns Bus Access Time—Works with faster microprocessors



Onchip Clock, Reference—Requires no external components for most applications

3-State Output Buffer—For direct interface with 8- or 16-bit microprocessor bus

Don't miss out on full 12-bit performance. For A/D converters with the best cost performance, **call Micro Power Systems' Hotline, (408) 562-3615;** 3151 Jay St., Santa Clara, CA 95054. And ask about our technical seminars.

SEE US AT ELECTRONICA BOOTH 19B13

MICRO POWER SYSTEMS

CIRCLE NO 55

Let's make it English

Last year, Senator Steve Symms of Idaho introduced a bill to amend the Constitution so that English would be the official language of the US (S J Res 13). The bill didn't pass, but it will undoubtedly be reintroduced when Congress convenes in '89. It deserves our support. Years ago, English was the only language commonly used in schools and businesses. Thus many immigrants were forced to learn a new tongue before they could enter the melting pot of American society. In this way, using a single language helped unite the people of the United States rather than keep them linguistically isolated in separate communities.

Unfortunately, we now face demands by Hispanic groups that we recognize the US as a bilingual and bicultural country. However, according to former Secretary of Education William Bennett, after 17 years of federal involvement and a $1.7 billion investment in bilingual education, there's no evidence that children have benefited.

Canada provides an example of how bi- or multilingualism can affect a country. (Keep in mind, though, that Canada started nationhood as a country already deeply divided into English- and French-based cultures, so its situation isn't exactly parallel to the US's.) Today, Canadians may communicate in either French or English; both are official languages. But bilingualism extracts a price. Communities—even those that speak only one language—must translate old laws, rules, and regulations so that English and French versions are available. Likewise, new official business must take place in both languages, and schools must be available for instruction in both English and French. Now, other nationalities in Canada want the same treatment; they are pressuring national and provincial governments for schools that teach in other languages. Such moves further divide a country and keep groups separated.

The Soviet Union provides an example of another kind. In an attempt to homogenize its republics, the Communists dictated that Russian would be the only official language in the USSR. However, the movement to one language was also an attempt to destroy republican customs and identities—a move that continues to stir ethnic unrest.

Adopting an official language in the US doesn't mean destroying ethnic groups or cultures. We must recognize our diversity and respect others' heritages and cultures. Certainly people can speak any language they wish, and they can use it on radio programs and in newspapers and magazines. But when it comes to education programs, ballots, law books, documents, manuals, data books, and other commercial and official papers, spoken and written English should be our official language.

Jon Titus
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Editorial Achievement Awards
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1977, 1976, 1975

American Society of
Business Press Editors Award
1988, 1983, 1981

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THE FIRST FULLY PROGRAMMABLE GRAPHICS PROCESSOR WITH ON-CHIP ACCELERATION

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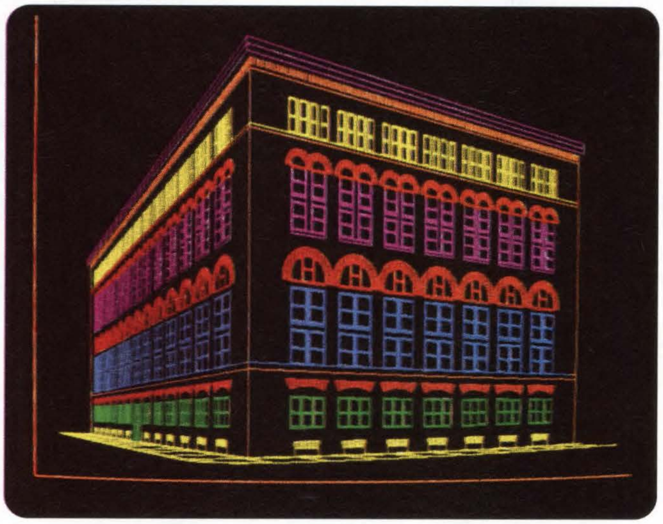
This 20-Mhz CMOS chip features a bus cycle time of 100 nanoseconds on back-to-back vector and block operations.

It gives you blazing speed in line drawing, BitBLT, fills, polygons, character drawing, and windowing — regardless of the number of bit planes. It also controls screen refresh.

COMPLETE FLEXIBILITY

The RGP gives you the programmability of a general-purpose processor, so you can optimize your system for specific applications. Or differentiate it from your competitors through proprietary algorithms.

The RGP, with our DP8511 BitBLT processing unit, is also the only



National DP8500 Raster Graphics Processor

graphics solution that effectively allows you to select either planar- or pixel-oriented operation on-the-fly. So you no longer have to lock yourself into one architecture or the other.

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It also gives you the right "hooks" and the right architecture for moving into 3D and solids modeling applications.

A COMPLETE SET OF CHIPS

Our Advanced Graphics Chip Set also includes

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- four video clock generators
- four video shift registers
- three video RAM controllers
- a growing list of video DACs

They're all part of National's unique modular approach — the only approach that addresses the complete graphics pipeline. And the only one with the performance and flexibility you need to carry you into the 1990s.

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Advanced Peripherals

CIRCLE NO 57

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MK	85-132	150W	1	3.8	6.7	2.4
MW	85-264	15W	3	1.0	4.3	2.4
MW	85-264	30W	3	1.0	5.9	2.4
MW	85-132/	50W	3	1.0	6.1	3.7
MW	170-264*	100W	4	1.6	7.8	4.4

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*Jumper selectable.

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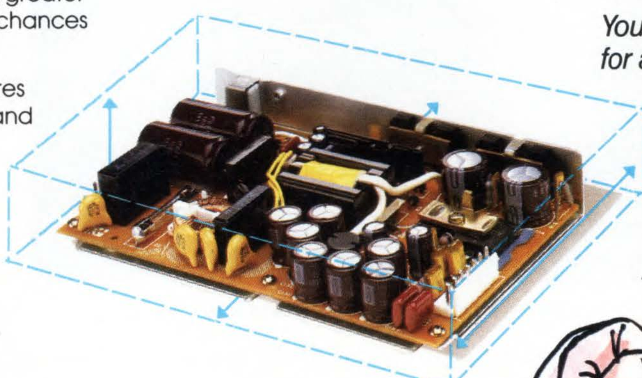
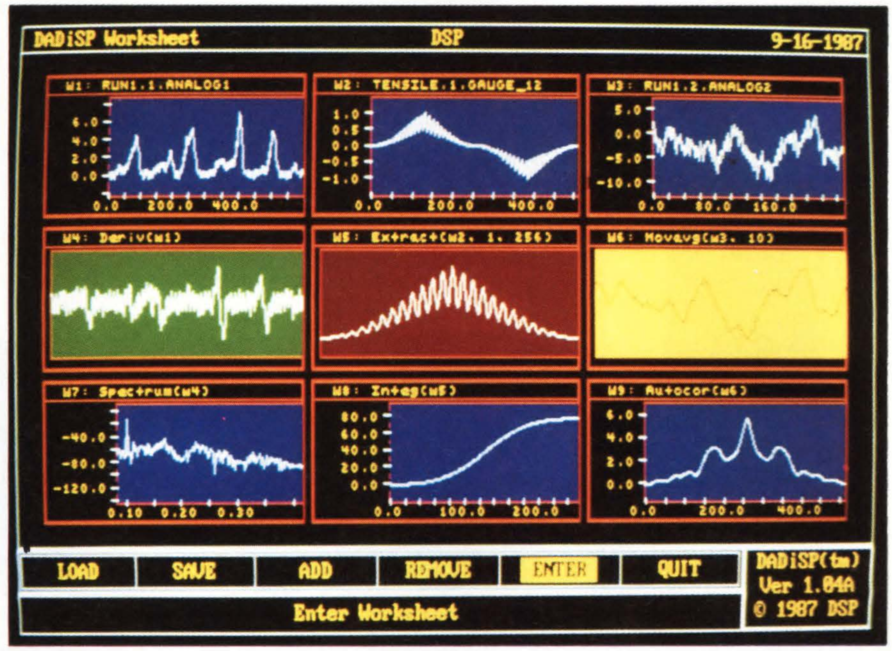


Toko's MW50, stands only 1" high. It's 85% smaller in total volume than Computer Product's PHB-719.

CIRCLE NO 58

Test and measurement software offers more than just another pretty interface

J D Mosley, *Regional Editor*



***You can work with a waveform instead of just numbers** if you use the Dadisp signal-analysis software from DSP Development Corp. The package also has a windowing capability.*

Vendors of test and measurement software are offering increasingly sophisticated user interfaces for their products as they strive to make more instruments that are both adaptable to computers and easy for test engineers to use. And in spite of the fact that some purists still insist that color graphics belongs in video games and not in serious engineering applications, it seems that color, at least for test and measurement software, is here to stay. Sophisticated options like color graphics don't necessarily make things more complicated—in fact, they can make instruments easier to use. But there can be a major tradeoff between performance and pretty pictures. Of course, given a powerful enough system and the right software, you can have it all.

While most instruments currently maintain the stand-alone option, others forgo hardware altogether, creating instruments that are purely software. In either case, the convenience of central control over several instruments at once is generally acknowledged, for such simplified control can significantly streamline your test and measurement tasks.

Performance isn't glamorous

One vendor who's opted for high performance and a more pedestrian interface is Test Systems Strategies, who uses an almost Spartan user interface for its Test Development Series (TDS) software. This program provides an automatic, rule-based interface between a design database and the test equipment by integrating VLSI chip design with test software.

TDS consists of three integrated programs: TDS Shell (the user interface), a CAE converter for simulator data input, and a Test Resource Allocation Manager for analyzing a design's testability. You can buy a fourth program, Pattern Bridge (P-Bridge), for reconstructing simulation waveforms and synthesizing functional test programs for the target equipment. TDS costs $15,000; P-Bridge starts at $16,000. In addition, a rules checker is available for $17,000.

The TDS Shell interprets a designer's or a test engineer's command and invokes one or more TDS programs that are associated with either a test instrument or a CAE logic simulator. You supply the program with the names of the CAE and ATE tools; the software then automatically develops the programming that links the two tools most effectively. And although the screen output is no more exciting than an oscilloscope's waveforms or the text of an error report, the information is concise and, for those accustomed to oscilloscope output, it's easy to understand. The programs run on an Apollo, Sun, or VAX host.

Integrated Measurement Systems' Characterization and Timing Analysis (CTA) software also makes chip testing more user-friendly without resorting to a graphics user interface. The CTA software has menu-driven routines for making ac and dc measurements of prototype devices and for plotting test results. You can use the package to measure the propagation delay, or to plot the interaction of any two device variables.

The CTA software collects the results of any Logic Master verification system and compiles those measurements in a spreadsheet for-

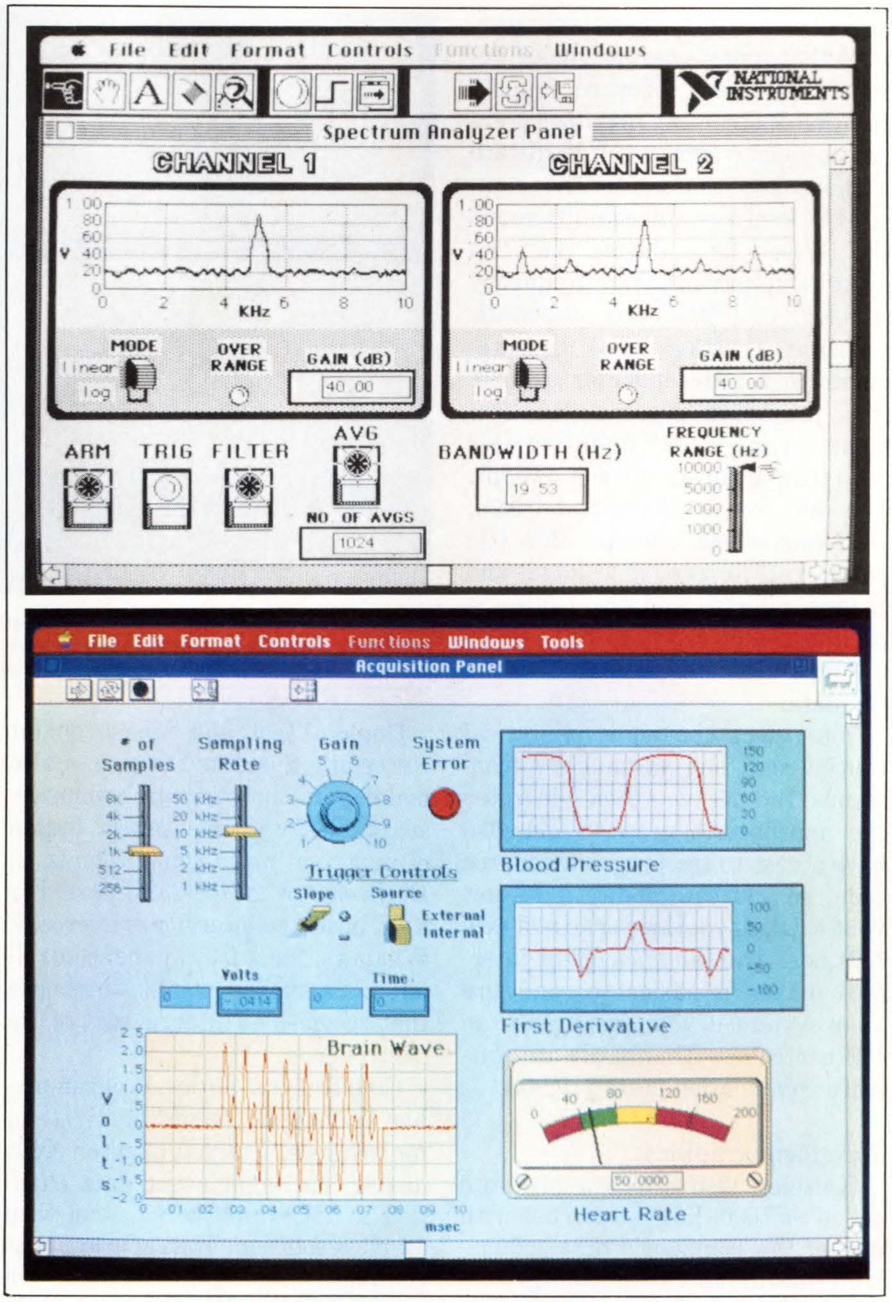
mat. (CTA is based on Lotus 1-2-3, so its plots, graphs, and data screens are familiar to anyone who uses spreadsheets.) If you want to create custom analysis routines, you can tap more than 30 preprogrammed CTA functions to define your device and to create a data sheet with annotated graphs, tables, and charts. The CTA also lets you order the tests in a sequence to develop automated-test programs. Prices for the PC-based package start at $3000.

Another test and measurement tool that uses the spreadsheet format is DSP Development Corp's Dadisp. This package has its own windowing capability and combines more than 150 functions for displaying and analyzing waveforms. It differs from other packages because it lets you work with waveform data in graphics windows and later convert the images to numbers, rather than forcing you to start with numerical values.

Dadisp provides data-processing functions such as signal editing, waveform generation, Fourier analysis, and peak finding, as well as real and complex signal arithmetic and calculus. You can define macros and then use them to tailor any of the functions. You can also create individual signal-processing steps by typing a formula into a Dadisp window. An optional software module called Dadisp-488 lets you add the IEEE-488 commands to your Dadisp worksheet, so that you can control and transfer data from IEEE-488 instruments.

Available for use with Sun workstations, the HP 9000 Series 300, Masscomp, the MicroVAX II, the VAX 2000, and IBM PCs, Dadisp ranges in price from $795 to $4995, depending on the host computer. Dadisp-488 sells for $195.

Developed by Lotus, who then sold the rights to National Instruments, Lotus Measure is a package you can run on your PC to take readings from IEEE-488 and RS-232C instruments. You can then put the results into a spreadsheet format. The package costs $495.



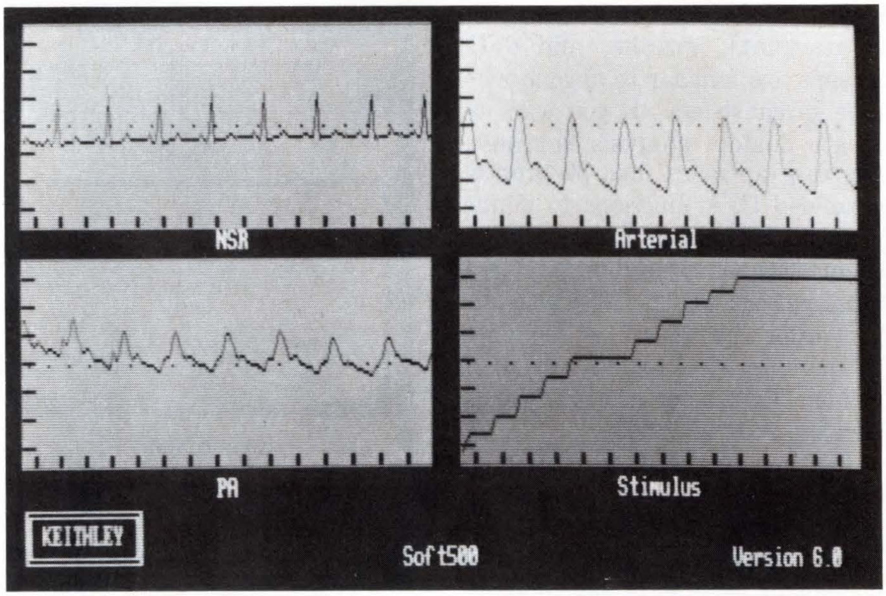
A comparison of the black and white screen *of Labview Version 1.0 with the color screen of version 2.0 highlights the enhancements of the later version. Version 2.0 also offers compiled run times that are 10 times faster than previous versions could muster.*

Software makes the difference

More and more, engineers are choosing their hardware based on the quality of available software. So, rather than continue to leave the programming aspects of test and measurement to third-party vendors, instrument manufacturers are now providing hardware and software accessories to make their units fully adaptable to computers. Fluke, for example, sells a $2200 Helios-I Computer Front End and a $295 Helios Toolbox library of Basic subroutines. If you still want to know what's available in third-party software, the company also offers a Helios-I software guide.

Keithley has adopted a similar approach. Better known for its hardware than for its software interfaces, Keithley does acknowledge that today's test engineer demands extensive software support and that instrument manufacturers can no longer simply sell hardware without such support. The company's Package 82 Simultaneous CV System is a device that can make simultaneous high-frequency (100-kHz or 1-MHz) and quasistatic capacitance-voltage (CV) measurements in a semiconductor sample, thus providing greater measurement accuracy and requiring less time than separate voltage sweeps. The unit comes with menu-driven, DOS-compatible software that lets you correct for system leakages and cabling effects, find the oxide capacitance and settling time, make CV measurements, and analyze the CV data.

You select the right analytical routine and set parameters from menus; the package then generates the appropriate graphs. You also have access to the program's source code, so you can modify it to suit your existing routines or to add new routines. And the Package 82 interface makes it easier to configure your system if you already use an HP controller. This hardware-software combination costs $19,995.



Although its output display is rather plain, *Keithley Instruments' Soft500 Version 6.0 software outperforms its prettier competitors with data-acquisition speeds of 50,000 samples/sec and a 16-bit resolution for as many as 32 channels.*

Waveform graphics

Keithley also offers a program called Soft500 that you can use with any of the company's data-acquisition mainframes. Although its graphics are limited to waveforms, the program outperforms its prettier competitors by taking 50,000 samples per second with a 16-bit resolution across as many as 32 channels. Soft500 Version 6.0 lets you configure your data-acquisition system with one command. A calibration feature offers sequential calibration for multiple instrument cards. If you have an old version of Soft500, you can trade it in and get version 6.0 for $100. The program is free if you purchase a Keithley hardware system or one of its AMM2 analog measurement cards.

Gould's Test and Measurement Recording Systems Division is also making its instruments computer-adaptable by giving you the option of plugging into a computer via an IEEE-488 or an RS-232C port. For a PC host, the interface is Microsoft Windows; for a front-panel controller, it's a similar graphics interface that becomes an integral part of the controller.

Gould's 5300 Series Programmable Waveform Recording System, for instance, lets you monitor eight analog and eight event data channels at 1M sample/sec/channel with 12-bit resolution. You can use a host computer to program the 5300 via its RS-232C or IEEE-488 port. Or you may order an optional Intelligent Front Panel (IFP) with an electroluminescent screen that comes with menu-driven software for system setup and waveform display. The IFP attaches to the front of any 5300 chassis and has a dedicated bus for controlling as many as eight 5300 units.

Define parameters to capture

Using a tool called the Event Manager, you can define the particular type of data you wish to capture (eg, spikes); thereafter you receive only that captured parameter instead of whole waveforms. The Event Manager has a 21-input, dual-trigger tree system that uses logical AND and OR functions to discriminate among more than 500,000 transient events.

Another software tool called the Memory Manager lets you optimize the 5300's use of memory. You can define the channel depth of its memory from 256 to more than 2 million samples per acquisition in increments of 256 samples. The 68000-based 5300 has two independent clock functions; you use the unit's 10-MHz master clock to program the two clock functions in 100-nsec increments.

For a more sophisticated user interface, you may want to purchase the ACQ5300 software. It simplifies the system setup and data acquisition with interactive, pop-up panels. This program also lets you edit all the text, the prompts, the help messages, and the colors; you can also develop and run macros for automatic configuration or for querying a system operator. ACQ5300 runs on the IBM PC/AT and sells for $1200. Pricing for the 5300 begins at $15,000.

Even more fascinating than soft-

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☐ **Low-power ECL arrays:** The ECL products available from Raytheon have densities comparable to 1.5 µm CMOS arrays and I/Os compatible with ECL, TTL (10K or 100K), and CMOS. These ECL arrays also deliver the industry's lowest power dissipation per gate. Their superior speed/power performance—<0.1pJ—provides the ASIC designer with state-of-the-art semicustom capabilities.

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Where quality starts with fundamentals.

CIRCLE NO 60

ware-driven instruments is the idea of software-generated instruments. National Instruments recently introduced a new version of its graphics-oriented Labview software. Labview 2.0 runs ten times faster on average than previous versions, and it has a dazzling color interface. This version also provides editing features like rubberbanding, graphics controls such as panning and zooming, and support for integer data elements. Best of all, the company will give Labview 2.0 free to all version 1.2 owners.

Labview is a colorful, icon-based, graphics programming system that simplifies engineering and scientific programming on Macintosh computers by permitting you to design instruments generated by, and based purely in, software. Instead of writing lines of code, you produce these instruments by drawing block diagrams that represent test and measurement functions. You then control these instruments via onscreen representational images of the types of switches, dials, and levers you would find on hardware versions of such equipment.

The rubberbanding feature lets wires remain attached to (and move with) an icon as you relocate it within a block diagram. You can select multiple objects for group manipulations. Or you can cut and paste icons, front panels, and block diagrams from one part of a software instrument to another area in the same device or to a different instrument.

Graphics compiler lends speed

Version 2.0 owes its impressive speed to a graphics compiler that generates machine code from the block diagrams of your software instrument. The result is that computationally intensive applications developed under the new software may run as much as 60 times faster, while I/O intensive applications can go about three times as fast as they did on the earlier version. (Version 1.2 interpreted the graphics programming language as it ran.) Labview 2.0 can also run all the applications you've developed under version 1.2.

To reduce memory requirements and to further increase execution speed, Labview 2.0 adds multiple integer and floating-point data formats to the old version's extended precision floating-point data type. And for embedded Labview applications, the manufacturer provides a run-time system for end-user functions composed entirely of fixed code. The program's object-oriented open-architecture and dynamic linking mechanism lets you write C code and insert it into Labview without recompiling the Labview code.

If you don't have Labview 1.2, you can buy version 2.0 for $1995. The company also plans to distribute libraries of Labview instrument drivers via its Macnet electronic bulletin board and on fourteen 3.5-in. floppy disks. Access charges for Macnet vary from $4 to $8/hour; the disks cost $50 each.

Flowchart programming arrives

Wavetek's Wavetest is a Windows-based program for automatic testing. It runs on an IBM PC/AT and uses icons and flowcharts to provide you with a text-free programming environment. A software bus analyzer comes in the package as well as an automatic-documentation feature for your test programs. A library of more than 50 instruments is also included, as well as an instrument-library generator, a test-program generator, Basic, a GPIB interface card, a tutorial, and reference manuals. The test-pro-

For more information . . .

For more information on the test and measurement software described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Asyst Software Technologies Inc
100 Corporate Woods
Rochester, NY 14623
(800) 348-0033
In NY, (716) 272-0070
Circle No 705

DSP Development Corp
One Kendall Sq
Cambridge, MA 02139
(617) 577-1133
TLX 324168
Circle No 706

John Fluke Manufacturing Co Inc
Box C9090
Everett, WA 98206
(206) 347-6100
TLX 185102
Circle No 707

Gould Inc
Test and Measurement Div
3631 Perkins Ave
Cleveland, OH 44114
(216) 361-3315
TLX 196113
Circle No 708

Integrated Measurement Systems
9525 SW Gemini Dr
Beaverton, OR 97005
(503) 626-7117
Circle No 709

Keithley Instruments Inc
28775 Aurora Rd
Cleveland, OH 44139
(216) 248-0400
Circle No 710

National Instruments Corp
12109 Technology Blvd
Austin, TX 78727/(512) 250-9119
TLX 756737
Circle No 711

Summation, Inc
11335 NE 122nd Way
Kirkland, WA 98034
(206) 823-8688
TLX 152219
Circle No 712

Test Systems Strategies Inc
8205 SW Creekside Pl
Beaverton, OR 97005
(503) 643-9281
TLX 4992633
Circle No 713

Wavetek
9045 Balboa Ave
San Diego, CA 92123
(619) 279-2200
TWX (910) 335-2007
Circle No 714

gram generator lets you set as many breakpoints as you need to debug your program. You can single-step through the program, trace variables, and create cross-reference lists. The package costs $3990.

Summation's $2950 Testwindows 3.0 also runs under Microsoft Windows on an IBM PC, but you use text rather than graphics to control IEEE-488 instruments. This program automatically takes advantage of your PC's expanded memory and offers keyboard control for harsh environments or industrial applications, where a mouse may prove impractical.

Although you have to learn the Testbasic language to run Testwindows, the company's Sigma Users Group provides program support and a library of Testbasic routines. An initial window lets you know what modules and instruments are available, and a device window simulates front panels to simplify instrument control. Using the Testbasic editor, you can cut, paste, copy, search, and replace code. Once you've completed your program, you can save it for later use and duplicate it for multiple devices.

Are Windows too restrictive?

One drawback ought to temper the current fervor for the graphics user interface with its icons and windows: a lack of flexibility. In eliminating any need for programming, a graphics shell also eliminates any chance for adapting the shell to a user's particular requirements. As a consequence, a number of scientific software manufacturers borrow features such as pop-up menus from the world of Windows, but keep the flexibility of a menu-driven interface to increase the end-user's options.

Asyst Software Technologies sells one such data-acquisition product. Asystant GPIB is a scientific number-crunching program that interfaces with IEEE-488 instruments. The program can control and monitor as many as 12 instruments. It automatically gathers instrument data; processes or generates waveforms; plots, scales, and labels your screen graphics; and generates tables. The package offers both algebraic and reverse-Polish notation for real and complex arithmetic and trigonometry.

Asystant GPIB also performs polynomial operations, solves differential equations, and performs statistical analysis (including curve fitting). When you issue commands to the instruments, you receive real-time feedback. Using menus and a command line, you can configure instruments, execute bus and device commands, and build and run GPIB routines. The program runs on an IBM PC and costs $695.

Cognitive instruments are next

Expert systems may form the basis for the next generation of test and measurement software. Although no AI packages are now commercially available for test instruments, you can buy field-service software for remote error analysis that hints of things to come. Digital Equipment Corp sells a Standard Package for Error Analysis and Reporting (Spear) that can identify a cracked read/write head in a disk drive, present the probable cause of the fault, and offer an explanation for why the problem occurred. Once the same types of functions are developed for instrumentation, you may be able to completely automate the analysis of test data. EDN

Article Interest Quotient
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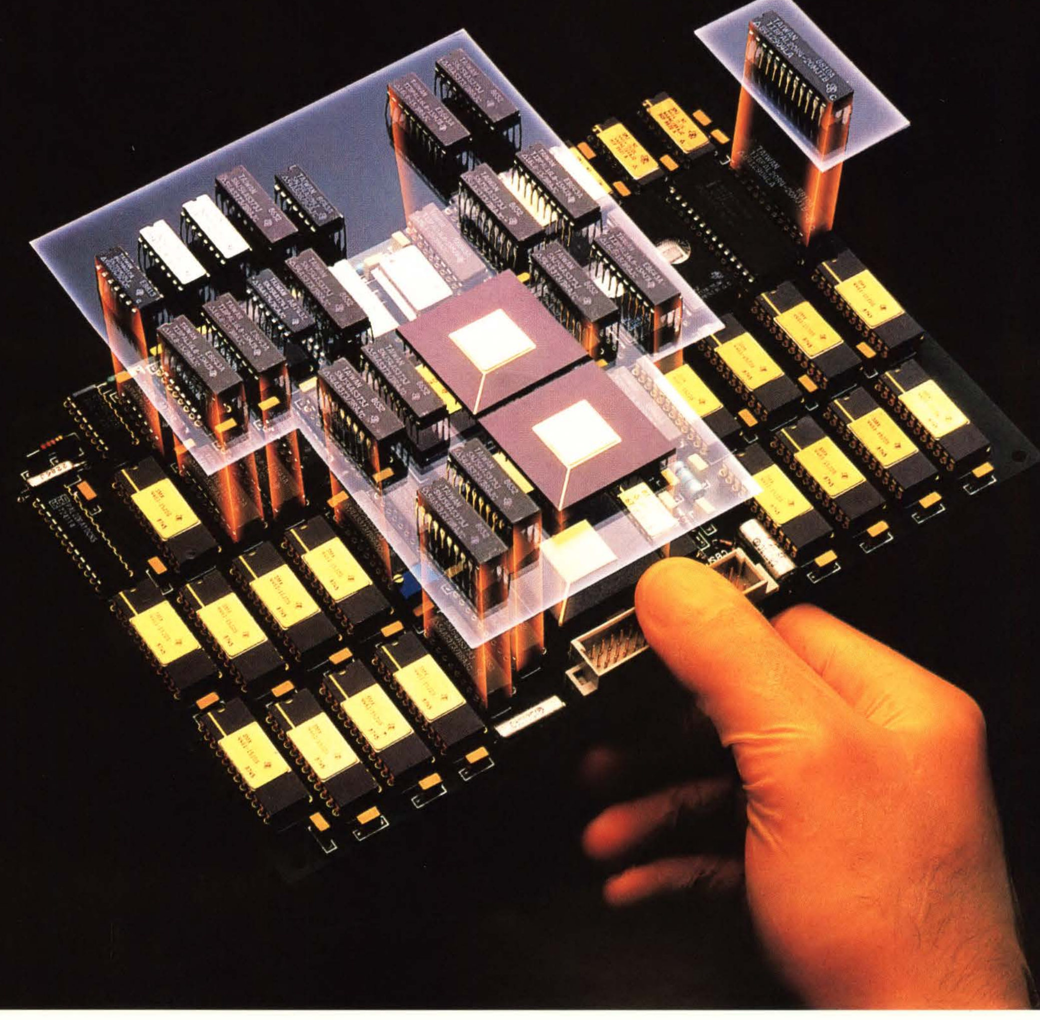
TEXAS INSTRUMENTS REPORTS ON

SYSTEMS LOGIC

IN THE ERA OF

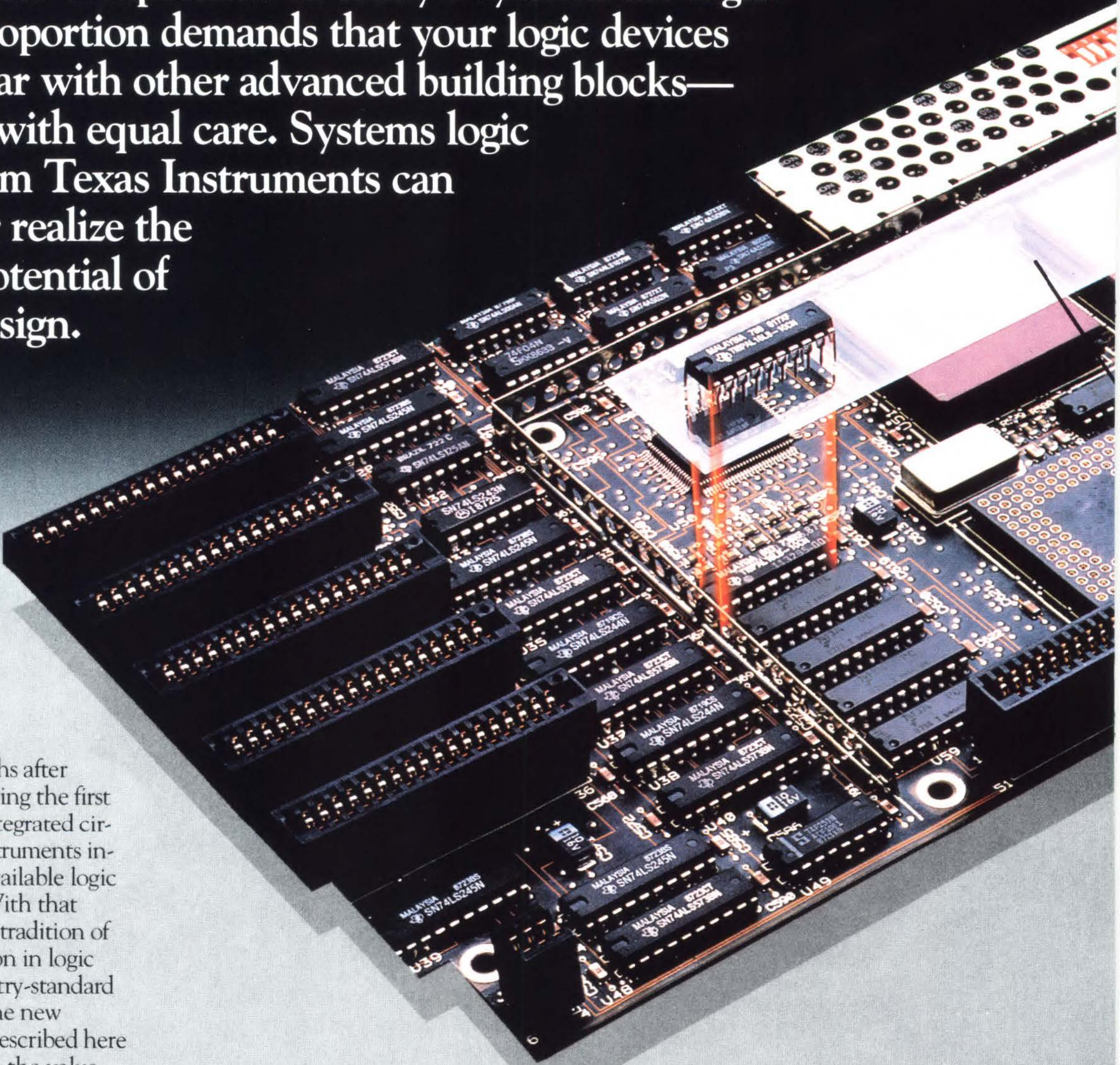
MegaChip TECHNOLOGIES



Systems logic in the Era of MegaChip Technologies:

No system should ever be limited by its to help your design perform at its best.

Up to 65% of the components in today's systems are logic. Such a large proportion demands that your logic devices perform on a par with other advanced building blocks— and be chosen with equal care. Systems logic alternatives from Texas Instruments can help you better realize the performance potential of your system design.



Within months after demonstrating the first working integrated circuit 30 years ago, Texas Instruments introduced a commercially available logic function, an RS flip-flop. With that beginning, TI established a tradition of development and innovation in logic that encompasses the industry-standard SN54/74 Series TTL and the new families of advanced logic described here that can add significantly to the value and performance of your overall system.

For example, for systems that require off-the-shelf flexibility with a degree of customization, TI's Programmable Logic Devices (PLDs) include popular 10-ns PAL® ICs available in high volume. And, to keep pace with today's high-speed microprocessors, TI plans to continue to drive PLD performance to sub-10-ns speeds.

TI's Advanced CMOS Logic (ACL) supports the design goal of high performance combined with low-power operation, while TI's new BiCMOS bus-interface family delivers very high drive current at very low power compared to bipolar circuits.

TI's MegaChip Technologies

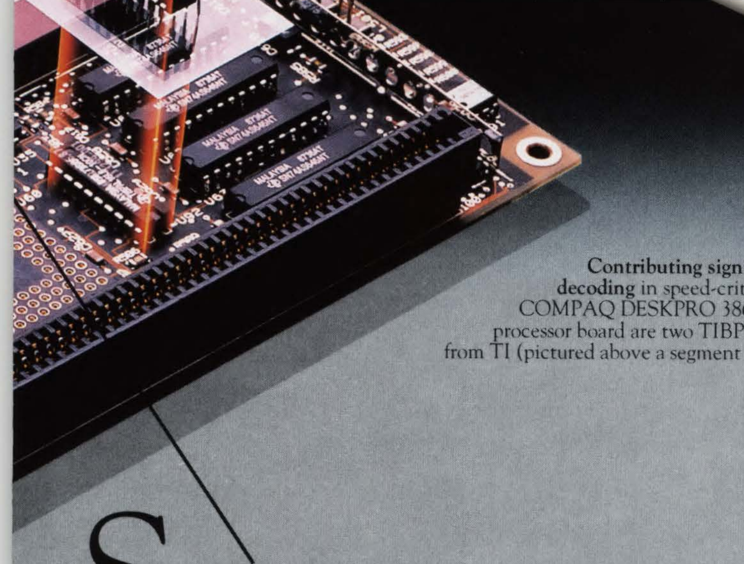
Our emphasis on high-density memories is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies, and they are the means by which we can help you and your company get to market faster with better products.

For systems requiring moderate densities and fast prototype cycle times, TI offers a new series of one-micron CMOS gate arrays. When you need higher levels of integration plus increased design flexibility, TI's one-micron CMOS standard cells provide the means for system consolidation.

And for military applications, TI offers a wide choice of high-reliability logic functions.

On the following pages are details of what you can expect from TI's range of logic options:

ON THE COVER: Suspended above the board, provided by Rockwell International, Missile Systems Division, are military versions of TI advanced logic devices.



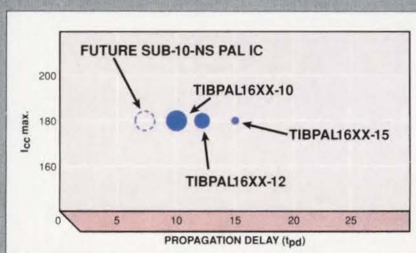
Contributing significantly to fast address decoding in speed-critical paths of the COMPAQ DESKPRO 386/20™ personal computer processor board are two TIBPAL16L8-10 PAL circuits from TI (pictured above a segment of the board).

Speed your system to market with TI's superfast PLDs.

PLDs are a functional alternative to standard logic ICs and gate arrays or standard cells.

Because TI's PLDs are off-the-shelf items you program yourself, you avoid the longer design cycle times of custom ICs and move on to market faster. These PLDs offer very attractive performance advantages. Consider these:

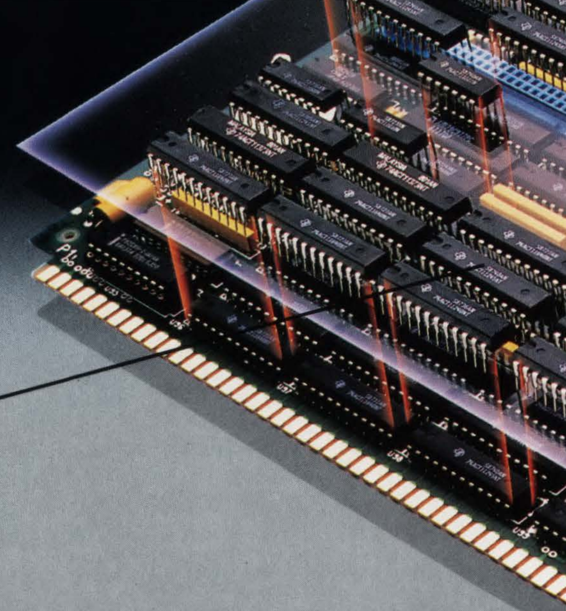
- **TIBPAL16XX-10 PAL ICs** from TI deliver a 10-ns propagation delay and are available in quantity. Clock-to-Q time is 8 ns, and output-registered toggle frequency is 62.5 MHz. IMPACT-X™ technology gives these PAL ICs their superior speed; they are well suited for use with high-speed processors such as the Motorola 68030, the Intel 80386, and RISC-based architectures. The 10-ns performance brings a higher level of integration to speed-critical paths.
- **TI's TIEPAL10H16P8-6 IMPACT™ ECL PAL circuit** delivers even faster operation: 6-ns propagation delay max. You can now streamline-conventional ECL designs by consolidating several discrete components into a single custom function.
- **TI's new 7-ns Programmable Address Decoder** is intended to help you squeeze more performance out of memory interface systems. By performing address decoding much faster than conventional PAL architectures—in 7 ns—the TIBPAD16N8-7 allows you to take advantage of the new processors to increase overall system performance.



TI's PAL IC road map shows consistent power and consistently higher speeds, with even faster versions on the way.

- **TI's 50-MHz Programmable State Machines (PSMs),** TIB82S105B (16 x 48 x 8) and '167B (14 x 48 x 6), are ideal for use in high-performance computing, memory interface, telecommunications, and graphics. These PSMs may be used to implement custom sequential logic designs such as peripheral I/O controllers and video-blanking controllers.
- **The TIBPAL22VP10-20,** with a 20-ns delay, is 20% faster than the competition's "A" version and much more flexible. A programmable output macrocell allows two extra, exclusive output configurations, for a total of six.
- **TI's TICPAL16XX Series 20-pin CMOS PAL ICs** are the cure for power problems. They operate at virtually zero standby power and are reliable, high-performance replacements for conventional TTL and HCMOS logic. The devices can be erased and reprogrammed repeatedly.

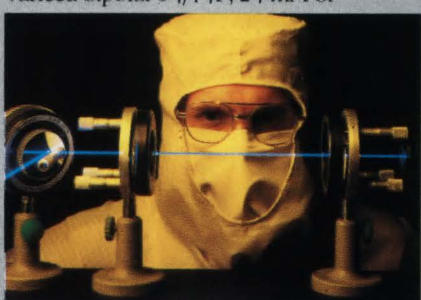
Turn page for more information



Get high speed, low power, and low noise with TI's broad ACL family.

It's an extensive family that includes gates, flip-flops, latches, registers, drivers, and transceivers. It's a readily available family in DIP and SOIC packages. It's TI's high-performance EPIC™ ACL family, bringing with it an important bonus—major reductions in noise.

Family speed is comparable to advanced bipolar 54/74F; 24 mA of sink/source current will drive 50-ohm transmission lines; and low power is characteristic of TI's EPIC technology. All this with "ground bounce" substantially reduced compared with end-pin ACL. The reasons are innovative packaging and a circuit-design technique called OEC™ (Output Edge Control) which softens the transition states that cause simultaneous switching noise. In fact, EPIC ACL noise levels are typically 10% less than those of bipolar devices.



When every nanosecond counts, TI's new high-performance ACL family can help you significantly improve system speed.

The rapidly increasing customer acceptance of TI's ACL family confirms its noise-reduction advantages and its ease of use.

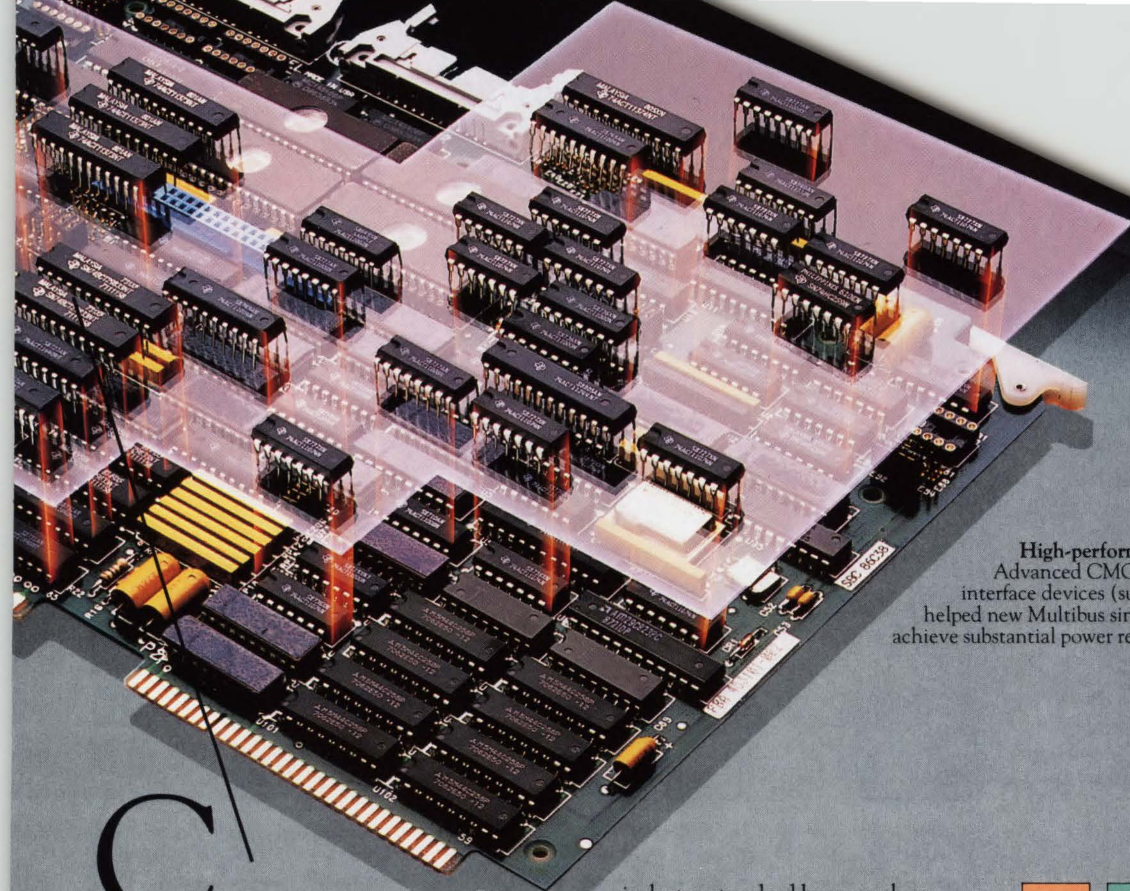
System design advantages

A unique "flow-through architecture" simplifies board design, layout, and troubleshooting. Inputs surround power pins on one side, outputs on the other, and control pins are strategically located at the package ends.

From a systems perspective, TI's arrangement offers the lowest-cost design when compared to end-pin ACL. Because in circumventing noise problems, end-pin designs can require additional components that take up to 32% more board area and slow system performance.

There are 146 functions, in both AC and ACT versions, currently announced in TI's ACL family, including such innovative, highly complex functions as advanced transceivers, line drivers, latches, feedback registers, multiplexers, and counters.

This ACL family, developed in cooperation with and supported by Philips/Signetics, fully meets JEDEC industry-standard No. 20 specifications for Advanced CMOS Logic.



High-performance, low-power EPIC Advanced CMOS Logic and BiCMOS bus-interface devices (suspended above the board) helped new Multibus single-board computer achieve substantial power reductions.

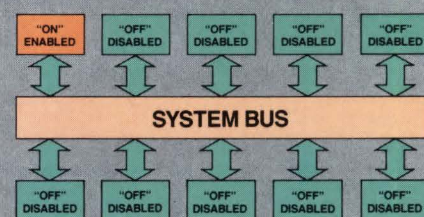
Cut power, not speed or drive, with TI's BiCMOS bus-interface ICs.

This new family is a simple, effective means to reduce system power consumption without compromising advanced performance.

As the BiCMOS name implies, TI combines bipolar IMPACT and CMOS processing to achieve switching speeds comparable to advanced bipolar products and provide the 48/64-mA drive current needed for high-capacitive loads and backplanes. In particular, family members meet the drive requirements of industry-standard buses such as Multibus® and VMEbus™

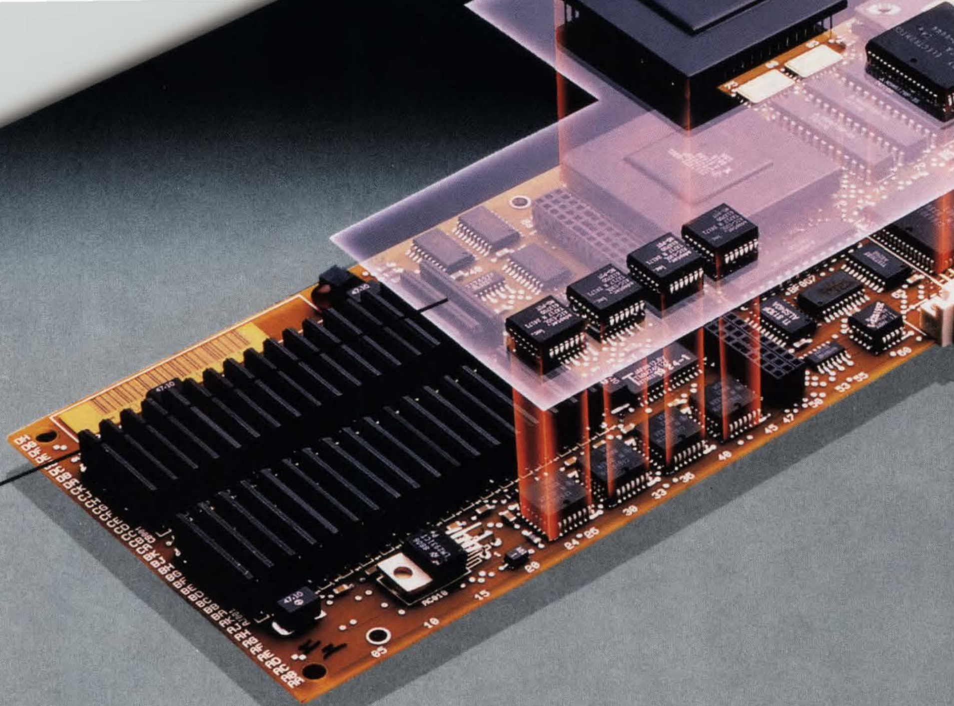
In addition, TI's BiCMOS devices can reduce disabled currents by 95% and active currents by 50%-80% compared to bipolar equivalents. Result: System IC power savings can be more than 25%.

There are more than 60 functions comprising TI's BiCMOS bus-interface family. Included are 8-, 9-, and 10-bit latches, buffers, drivers, and transceivers—a wide choice that means you can easily find what you need to implement high-performance bus-interface designs.



An innovative circuit design in TI's BiCMOS bus-interface logic helps lower disabled currents. This is key to overall power savings because in a typical bus network only one device is enabled at a time.

Turn page for more information



Achieve higher integration more confidently with TI's new one-micron ASIC family.

Now, you can integrate more of your systems logic using TI's new one-micron CMOS ASIC (application-specific integrated circuit) family—the TGC100 Series gate arrays and the TSC500 Series standard cells. Each offers different degrees of design flexibility and system integration. The result is significantly reduced component count which cuts board size and system cost while improving reliability and performance.

And TI is supporting the family with comprehensive kits that help minimize design cost, risk, and time by providing a comfortable, easy-to-use design environment.

Efficient logic consolidation

Using TI's new TGC100 Series gate arrays, you can sweep major chunks of "glue logic" into a single device while realizing fast design and prototype cycle times. Array densities currently range to more than 8K usable gates and 142 bond pads; the Series will be extended to more than 16K usable gates and 216 bond pads in a major production release planned for late 1988. Prototype delivery is typically two to three weeks from approval of postlayout simulation results.

The TGC100 Series Design Kit gives you complete autonomy and control over the design process. It is a comprehensive set of the tools required for successful gate-array design and validation *(see last page for details)*.

Standard packages for the TGC100 Series range from 28-pin DIPs to 84-pin PLCCs, with optional packages up to 144 pins.

System consolidation on a chip

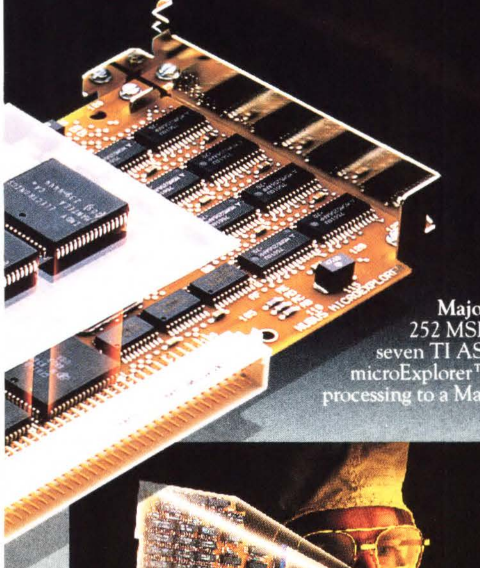
For applications requiring maximum design flexibility and higher levels of integration, TI has disclosed its third-generation standard-cell family, the TSC500 Series.

Complex system designs can be implemented using a growing core of basic SSI/MSI functions, as well as scan cells for testability and MegaModule™ building blocks such as register files. FIFOs, bit-slice family functions, RAM, and ROM are other aids to implementation. Output cells with drive capability up to 64 mA are available.

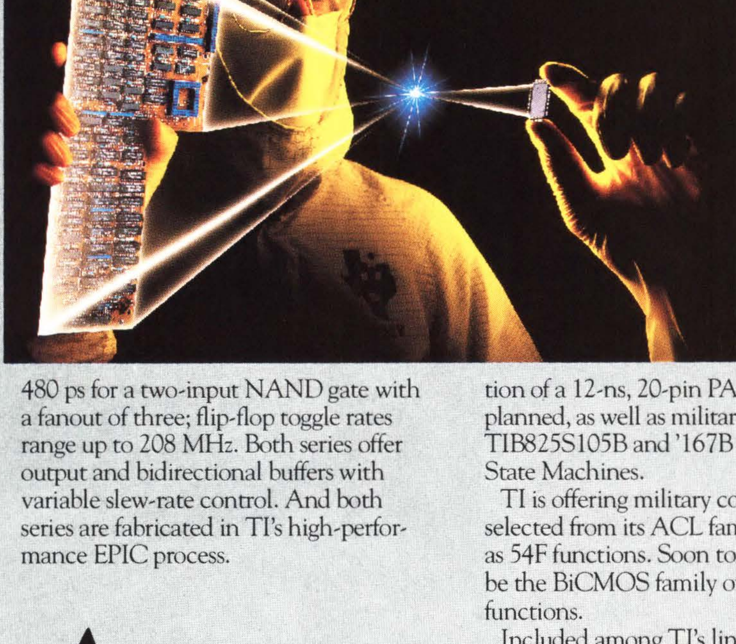
Package options include conventional through-hole DIPs, surface-mount PLCCs, and plastic quad flatpacks (QFPs) in both JEDEC and EIAJ standards, as well as high-pin-count plastic pin-grid arrays.

Both the TGC100 and TSC500 Series have a typical propagation gate delay of

logic. TI offers advanced logic families



Major logic consolidation, the equivalent of 252 MSI and LSI devices, was possible using the seven TI ASIC functions shown above the microExplorer™ board which brings symbolic processing to a MacIntosh II® desktop computer.



480 ps for a two-input NAND gate with a fanout of three; flip-flop toggle rates range up to 208 MHz. Both series offer output and bidirectional buffers with variable slew-rate control. And both series are fabricated in TI's high-performance EPIC process.

Apply TI's advanced logic to improve the performance of military systems.

Among TI's broad selection of logic devices produced to military requirements is a large PAL family. Propagation delays as fast as 15 ns are available over the military temperature range. The introduction of a 12-ns, 20-pin PAL circuit is planned, as well as military versions of the TIB82S105B and '167B Programmable State Machines.

TI is offering military counterparts selected from its ACL family, as well as 54F functions. Soon to come will be the BiCMOS family of bus-interface functions.

Included among TI's lineup of military ASICs are versions of the one-micron TGC100 Series gate arrays discussed at left, as well as two-micron standard cells.

TI's logic devices are among the more than 800 military functions offered compliant to MIL-STD-883C, Class B. Of this total, TI provides more than 200 to DESC-standard military drawings and is qualified to supply 285 JM38510 Class B devices (QPL 75).

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- First commercially produced transistor radio (1954)
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- First integrated-circuit computer (1961)
- First hand-held calculator (1967)
- First single-chip microprocessor (1970)
- First single-chip microcomputer (1970)
- First single-chip speech synthesizer (1978)
- First advanced single-chip digital signal processor (1982)
- First video RAM (1984)
- First fully integrated trench memory cell (1985)
- First gallium arsenide (GaAs) LSI on silicon substrate (1986)
- First single-chip Artificial Intelligence microprocessor (1987)

Turn page for more information.

Comprehensive support from TI helps you improve your design performance as you improve system performance.

To enable you to excel in designing the logic portion of your system for maximum performance, TI has compiled or is making available a wide range of design tools and aids:

PLDs: The TI PLD data book (472 pages) contains design and specification data for 78 device types. Four application notes are incorporated as a reference tool. A qualification book is available, and a state-machine design kit is forthcoming.

ACL and BiCMOS Bus Interface: TI's ACL data book (348 pages) contains detailed specifications and applications information on the members of the one-micron ACL family. The ACL designer's handbook (299 pages) spells out the technical issues confronting advanced-logic design engineers and describes methods for handling the issues. A qualification book (358 pages) features extensive reliability and characterization data, die photos, and application derating factors. Customer evaluation capability is enhanced by TI's system evaluation board (available for demonstration through TI field sales offices) and third-party characterization boards.

Data sheets are available on each member of TI's BiCMOS bus-interface family.

ASICs: The TGC100 Series Design Kit gives you the tools needed to successfully complete a gate-array design: A macro library for Daisy or Mentor engineering workstations containing the graphic symbol and functional and simulation models for each macro; a software library of TI-specific software tools that streamline and simplify the design process; a design manual that answers "how to" questions about designing with the TGC100 Series; a two-volume data manual providing detailed specifications for each macro in the TGC100 Series software library; and a software user's manual.

An equally comprehensive design kit for the TSC500 Series is currently in development.

Extensive design support available for TI's systems logic families includes that for the new TGC100 Series gate arrays *(at top)*, Programmable Logic Devices *(at left)*, and Advanced CMOS Logic.

For more information on TI's advanced systems logic ICs and their support tools, complete and return the coupon today. Or write:

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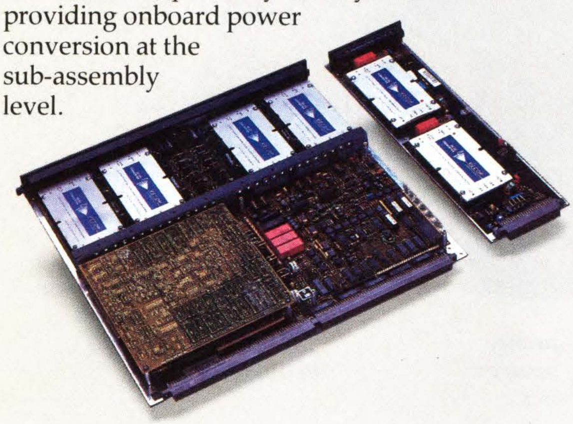

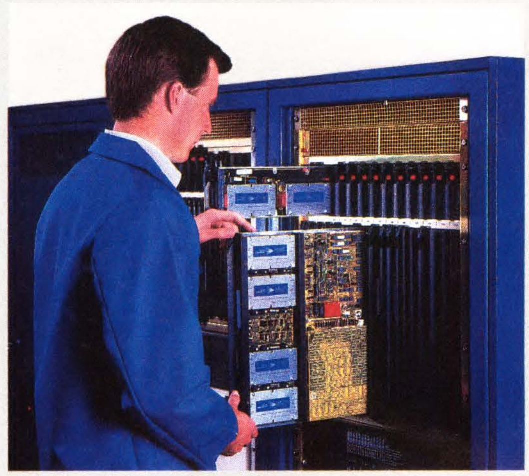

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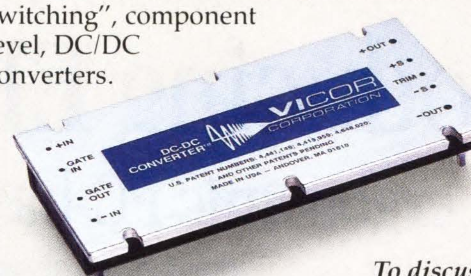

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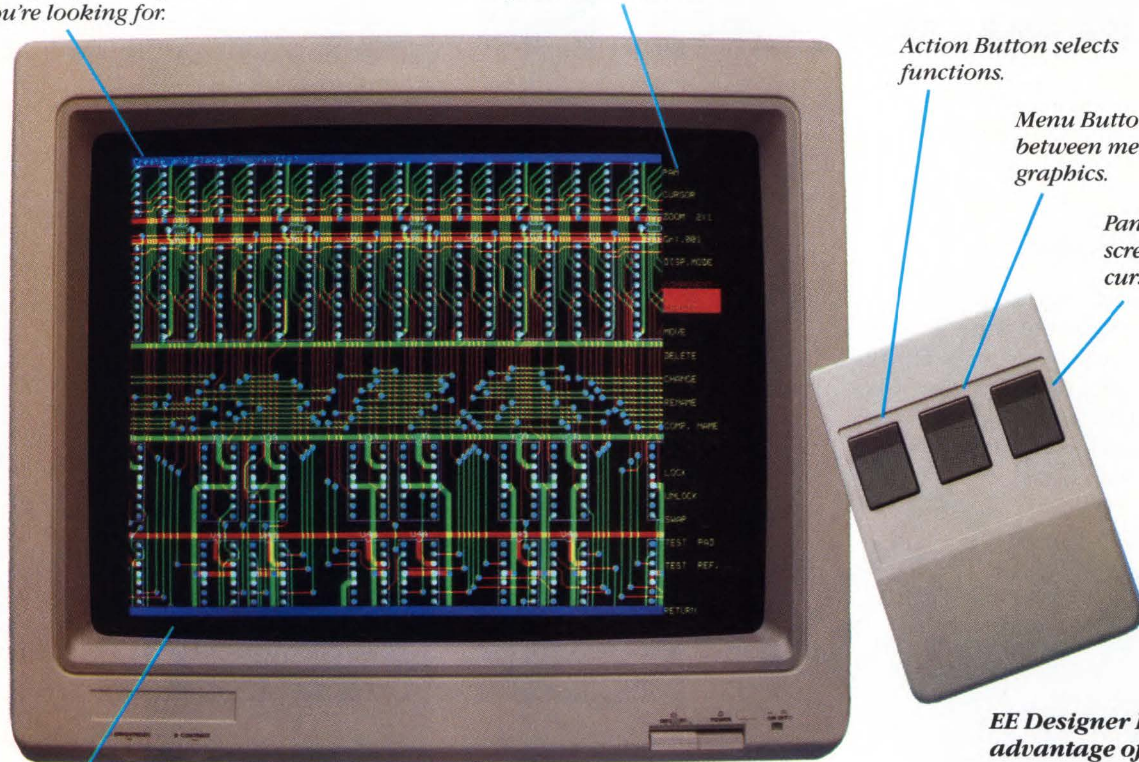

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CIRCLE NO 200

Dielectrically isolated ICs move into high-performance applications

Richard A Quinnell,
Regional Editor

A wide range of high-performance analog ICs now use dielectric-isolation techniques. Precision amplifiers, video circuits, analog switches, circuits with high input voltages, and even analog ASICs currently benefit from dielectric-isolation technology. These ICs can boost the performance of your most demanding systems.

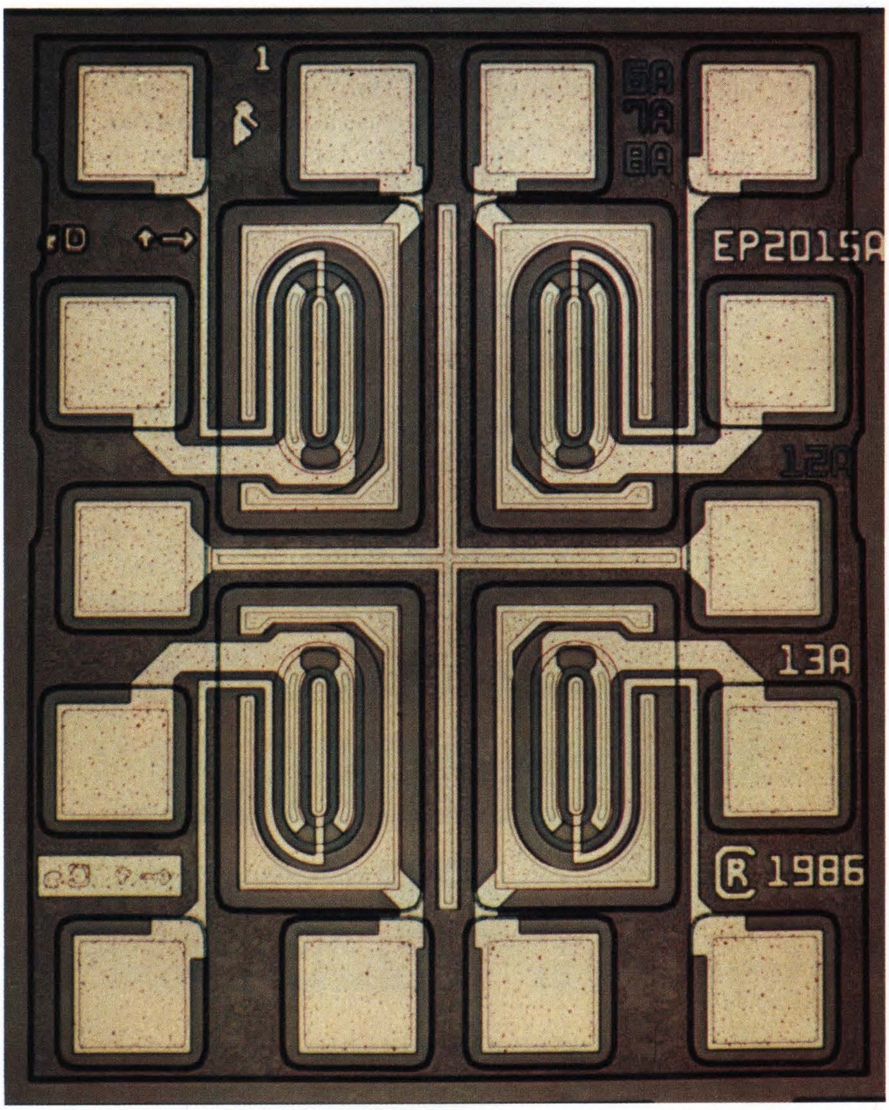
Dielectric isolation, which was first introduced commercially in the 1960s by Harris Semiconductor, was originally developed to improve the radiation tolerance of ICs. Three other companies—Burr-Brown, Elantec, and Sipex's DataLinear Div—have since joined Harris in the ranks of suppliers of dielectrically isolated ICs. In fact, two of the four entered the field only very recently: Elantec began producing the devices in 1985, and Sipex began offering standard products in January 1988.

DI benefits high-speed ICs

From its origin in radiation-hardened devices, dielectric-isolation technology expanded to high-speed circuits (see **box**, "Dielectric isolation yields performance advantages"), for which it offers several advantages over junction isolation. One advantage is that dielectrically isolated devices have relatively low parasitic capacitance: It's typically one-tenth that of junction-isolated devices. This fact translates into both a higher frequency response and lower power consumption. In other words, less time and current are needed to charge the capacitors.

Advances in digital technology are the principal reason that dielectrically isolated ICs are moving into high-performance applications. It's now the analog portions of systems that are the limiting factor in system performance. System designers are therefore demanding higher performance from analog circuits, and one of the ways that IC manufacturers are responding is to develop new dielectrically isolated devices.

At present, however, the premium you pay for dielectric isolation—the price is at least 30% more than that of comparable junction-isolated devices—restricts its use in less-demanding applications. That's the bad news. The good news is that the additional cost is principally due to the manufacturing process, and



***You can see the isolation barrier** as dark rings around the transistors in this quad transistor array from Elantec. The glass forms a cup underneath the transistor, separating it from the substrate.*

manufacturers are already making efforts to lower the cost of manufacturing the ICs by improving the process.

High-speed devices such as the popular Harris 2500 Series op amps were the first type of analog IC to benefit from dielectric-isolation technology. Both Sipex and Elantec are alternate sources for many of the products in the series, including the 2500/02/05, the 2510/12/15, and the 2520/22/25.

Precision and speed

Op amps that combine speed and precision were the next type of device to adopt dielectric-isolation technology. Two recent examples are the Harris HA-5147A and the Burr-Brown OPA-602P. The HA-5147A has a slew rate of 35V/μsec. Its gain-bandwidth product is 120 MHz, its minimum stable gain is 10, and its output settles to 0.01% of the final value within 400 nsec.

The HA-5147A's speed doesn't require you to sacrifice precision. The device's offset voltage is 10 μV; its typical bias current is ±10 nA. It consumes only 3.5 mA of supply current, and it costs $6.21 (100).

The Burr-Brown OPA-602P also offers a combination of precision and speed. This part is unity-gain stable and has a bandwidth of 6.5 MHz and a slew rate of 35V/μsec. Its offset voltage is ±1 mV typ and its bias current is 1 pA. It sells for $2.80 (100).

Circuits for video

Speed is not the only advantage that dielectrically isolated ICs can offer for your applications. For example, these ICs' capacitance is independent of the strength of the signal, a feature that's advantageous for high-quality video applications.

One recent dielectrically isolated device that's specifically intended for video applications is the Harris HA-2544, which offers a typical differential gain of 0.23% and differential phase of 0.05° for a load resistance of 1 kΩ. It also features a 65° phase margin and a gain-bandwidth product of 50 MHz. The device's slew rate is 150V/μsec, and it settles to 0.1% in 120 nsec. It costs $4.83 (100).

Another video device that capitalizes on the advantages of dielectric isolation is the Elantec 2003 video line driver. This unity-gain device offers a 100-MHz bandwidth and can handle as much as ±100 mA of output current with resistive loads. It features a typical slew rate of 1200V/μsec for a 1-kΩ load, differential gain of 0.1%, and differential phase of 0.1°.

Isolation and high voltage

The glass insulator used in dielectric-isolation techniques contributes to the isolation between channels in the Harris HI-222 video switch. The switch features 35Ω on-resistance, and its typical leakage current is

Dielectric isolation yields performance advantages

The key to understanding the performance of dielectrically isolated ICs is to examine the processes that produce them. Although the different manufacturers' processes vary somewhat, the companies all use the same four basic steps **(Fig A)**.

The first step is to etch the silicon to produce islands. The angle and depth of the etching determines the size of the transistors that can be produced and their spacing.

The next step is to oxidize the surface of the silicon. This oxide becomes the insulator that isolates the transistors from the substrate and each other. It also accounts for the high voltage tolerance of dielectrically isolated devices: Because it's made of glass, rather than a semiconductor junction, the barrier undergoes breakdown at several hundred volts instead of several tens of volts.

The third step is to grow polysilicon on top of the oxide layer. The new polysilicon layer is as thick as the original wafer. This layer will serve as the substrate for the final circuit; it must be rugged enough to tolerate handling after the silicon layer has been removed. Much of the extra cost of dielectric-isolation technology comes from this step—it takes time and care to grow the layer and at the same time make sure it doesn't curl up like a potato chip.

The fourth step is to flip the wafer over and remove silicon until the bottoms of the etched wells

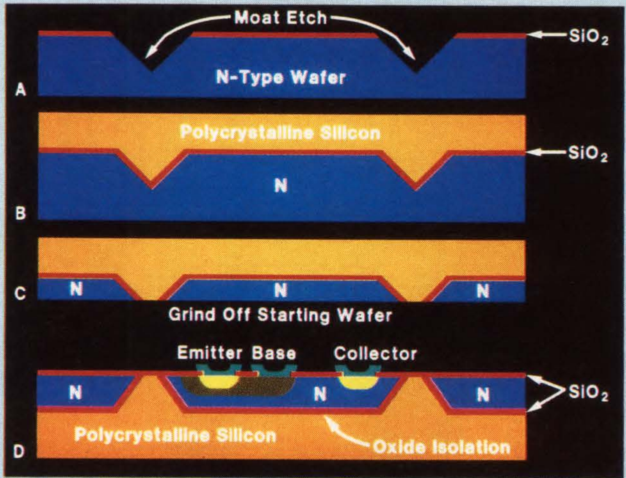
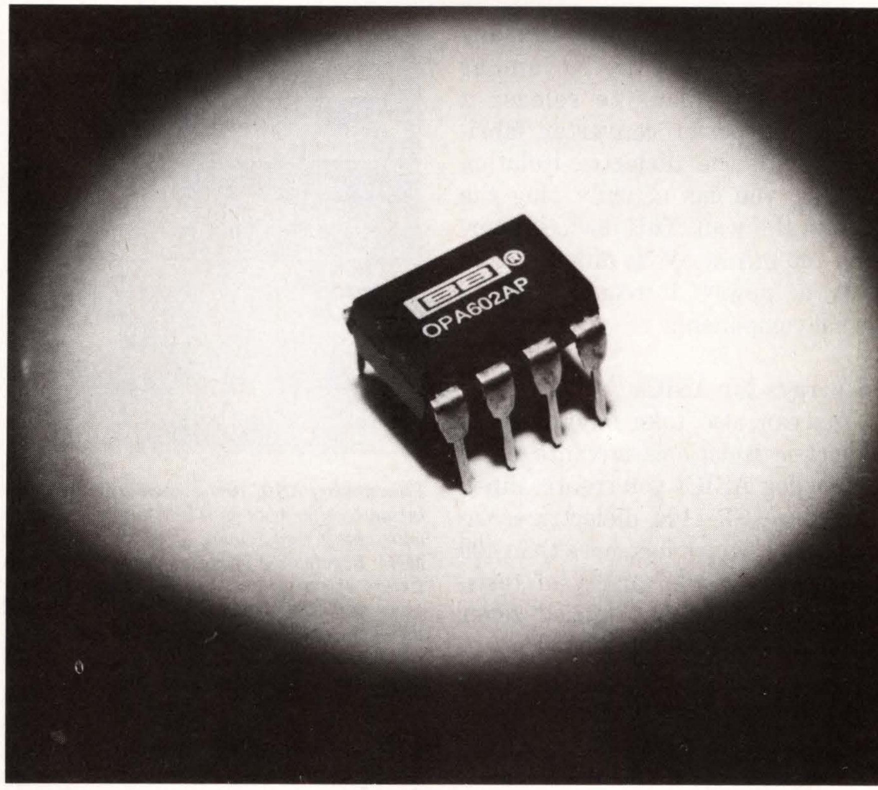


***Fig A—Dielectric isolation includes four preliminary steps** that other semiconductor processes don't use: You etch the silicon **(a)**, oxidize its surface **(b)**, grow a polysilicon layer on top of the oxide layer **(c)**, and finally mill away the original silicon **(d)**.*

0.2 nA at 25°C. The isolation between channels is 84 dB; the off-isolation is 72 dB at 5 MHz. The device also features a 200-MHz bandwidth and exhibits differential gain of 0.02% and differential phase of 0.02°, specs that tailor it for video applications.

The presence of an insulator around the transistors allows dielectrically isolated devices to tolerate much higher input voltages than junction-isolated devices can; the oxide's breakdown voltage is typically greater than 800V. This tolerance allows the Harris HC-5502B subscriber-line interface circuit (SLIC) to interface directly with the bell-ring signals, which are typically over 100V, without needing an external transformer. It also helps to protect the device from surge voltages, which commonly occur in telephone lines. The device can withstand surges as great as 1000V.

Dielectrically isolated ICs' ability to tolerate high voltage on the in-



***This dielectrically isolated precision op amp** (the OPA-602 from Burr-Brown) features a 35V/nsec slew rate, a 6.5-MHz bandwidth, and a 2-pA bias current. The device is available in a plastic DIP for $2.80 (100).*

are exposed. What were pillows of silicon covered with glass are now tubs of glass filled with silicon. The precision with which the manufacturer performs this fourth step determines the depth of the silicon tubs and the yield of the wafer. If the milling is not parallel to the original wafer surface, too much of the material will be removed from one edge of the wafer. The accuracy of the milling depth is important, too. This accuracy determines how shallow you can make the tubs and still get an acceptable yield. The size of the tubs determines the transistor density.

The remainder of the process for dielectrically isolated chips is the same as for chips fabricated in other technologies. The most commonly used technique is bipolar processing, which produces structures containing both npn and pnp transistors. Unlike junction-isolation techniques, dielectric-isolation techniques allow manufacturers to fabricate both types of transistors with equal facility, so dielectrically isolated devices can use a complementary structure made from high-speed vertical transistors. Junction-isolation devices either use slower planar transistors for one of the types or use designs having only one transistor type. Either technique exacts a speed and performance penalty.

Separating the transistors with an oxide layer has many other advantages as well. An isolation junction is, essentially, a reverse-biased diode. This diode allows current to leak to the substrate and presents a parasitic capacitive load at the collector. The leakage current increases with temperature and under irradiation, causing the circuit to fail at high temperatures and radiation levels. The parasitic capacitance increases the power dissipation at high frequencies, limits the frequency response, and varies as a function of the signal voltage, causing signal distortion.

A dielectrically isolated device has no isolation diode. Its substrate's parasitic capacitance is only a tenth that of junction-isolated circuits and is virtually independent of the signal level. Its leakage current is almost nonexistent, and it's unaffected by radiation and temperature. Because an insulator surrounds every transistor, the performance of a dielectrically isolated device is comparable to that of a hybrid circuit with discrete transistors mounted on a ceramic substrate.

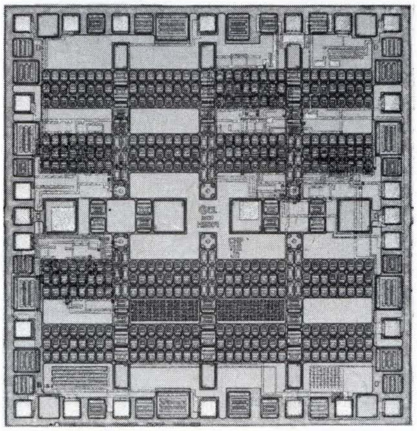
puts is also proving useful in many new applications. In November 1988, Harris plans to release a monolithic power converter fabricated with the dielectric-isolation process; you can actually plug the IC into the wall. This device generates 100 mA at 5V dc directly from 120V ac power. It requires no external components.

DI arrays for ASICs

You can also take advantage of dielectric isolation's advantages in the analog ASICs you create. Sipex offers the SP-1104 dielectric-isolation array, which has more than 400 transistors and a variety of resistors, capacitors, and buried zener diodes in a 4×4 matrix of tiles.

Each tile of the SP-1104 gives you 24 small-geometry transistors—12 pnp and 12 npn types. The pnp transistors offer a β of 150 and a transition frequency (f_T) of 600 MHz. The npn types have a β of 200 and an f_T of 1 GHz. The array offers transistors in four sizes. Their collector currents range from 10 nA to 100 mA, and you can obtain complete Spice models for the transistors.

The other components lie between the transistor tiles. You have a choice of three capacitor sizes—5, 8, and 18 pF—and enough clear field area for 800 kΩ of thin-film resistors. You tailor both the thin-film resistors and the capacitors during fabrication.



This analog ASIC array uses dielectric isolation *to offer both npn and pnp transistors with cutoff frequencies of greater than 600 MHz. Besides including more than 400 transistors of varying sizes, the Sipex SP-1104 gives you programmable capacitors and thin-film resistors, zener diodes, and pinch resistors, so you can create a variety of designs without using external components.*

The array also offers low-precision pinch resistors for applications that require higher resistance; for example, you can use them as bleeder resistors. These resistors offer a 20% tolerance and a breakdown voltage of 8V. There are 36 of these resistors, in groups of six, each with a nominal value of 35 kΩ.

Integration support

You can use either CAD tools or manual layout techniques to complete your design, then submit it to Sipex for integration. The company's integration service includes a design review, layout verification, testing, packaging, and delivery of 25 functional prototypes, and it costs $19,750. You can obtain additional prototypes at $1000 for 25 units if you order them with the integration service.

Future dielectrically isolated devices may cost less than current ones. The premium you must currently pay for dielectrically isolated devices is due to the special processing steps the technology requires. Manufacturers are actively investigating ways to cut the cost of such process steps as polysilicon deposition and milling.

For example, the manufacturers are examining alternatives to polysilicon deposition, because the polysilicon layer takes time to grow, and because it sometimes causes the wafer to curl up like a potato chip rather than remaining flat. An economical alternative to polysilicon deposition is wafer bonding, the technique of attaching a second wafer to the first to provide silicon support.

Manufacturers are also examining ways to improve the accuracy of their milling techniques. The best milling accuracy they've achieved so far is ±3 μm, which leaves behind an average of 25 μm of the original silicon. To produce finer geometries for dielectrically isolated ICs will require milling accuracies closer to ±1 μm. EDN

For more information . . .

For more information on the dielectrically isolated ICs described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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Access Time Range	15-25ns	55-70ns	65-200ns	65-200ns
Depth Expandable	x	—	x	x
Width Expandable	x	x	x	x
Packaging	300 mil 24/20 Pin DIP	300 mil 24 Pin DIP	600 mil 28 Pin DIP	600 mil 28 Pin DIP 32 PLCC
Status Flag E, Empty. F, Full. HF Half Full. AF, Almost Full. AE, Almost Empty.	E, F HF, AF AE	E, F AF AE	E F HF	E F
Availability	***	*	***	**

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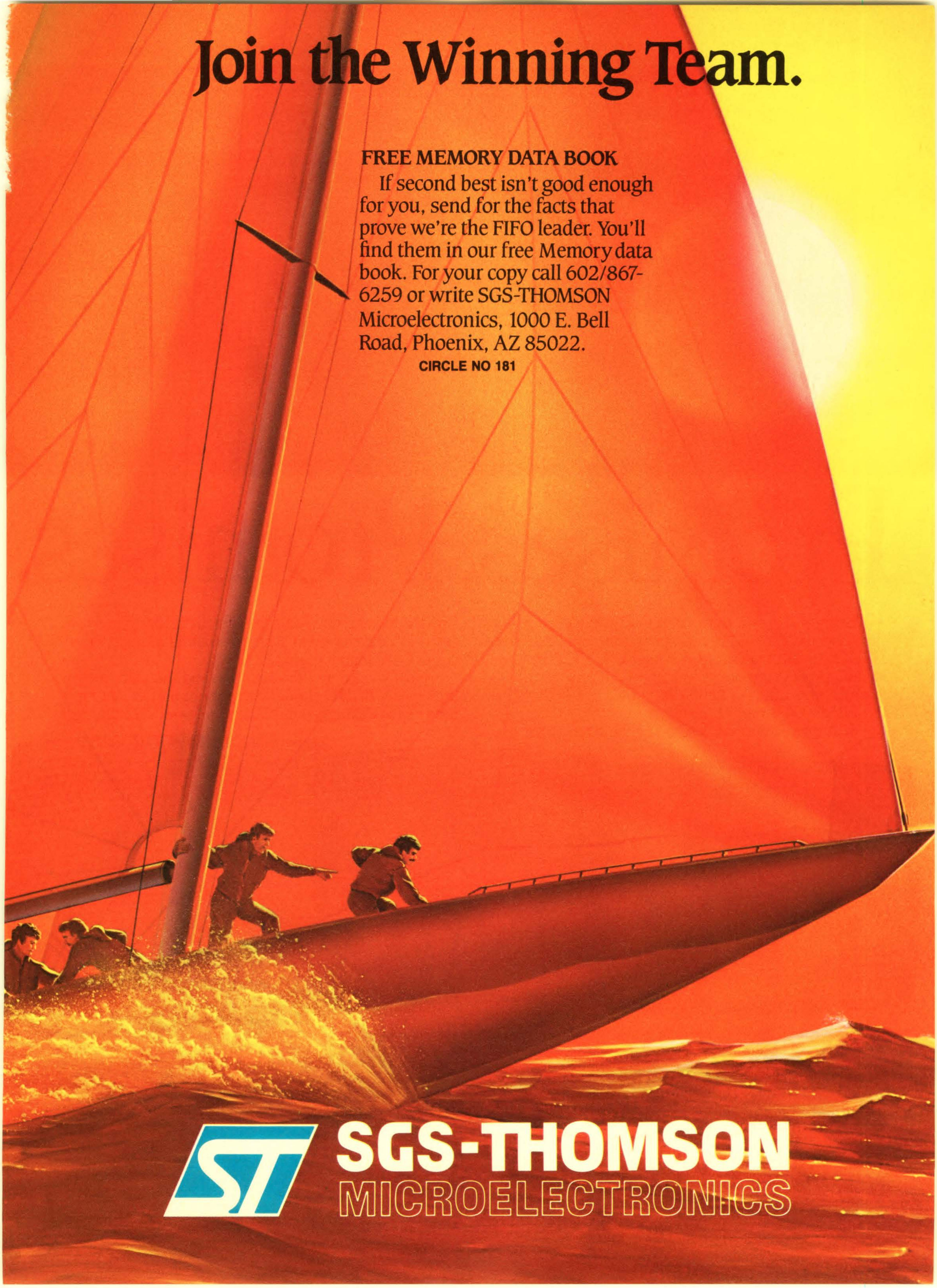
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CIRCLE NO 181
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PM 3065 100 MHz, dual channel, third-channel triggerview, delayed timebase oscilloscope

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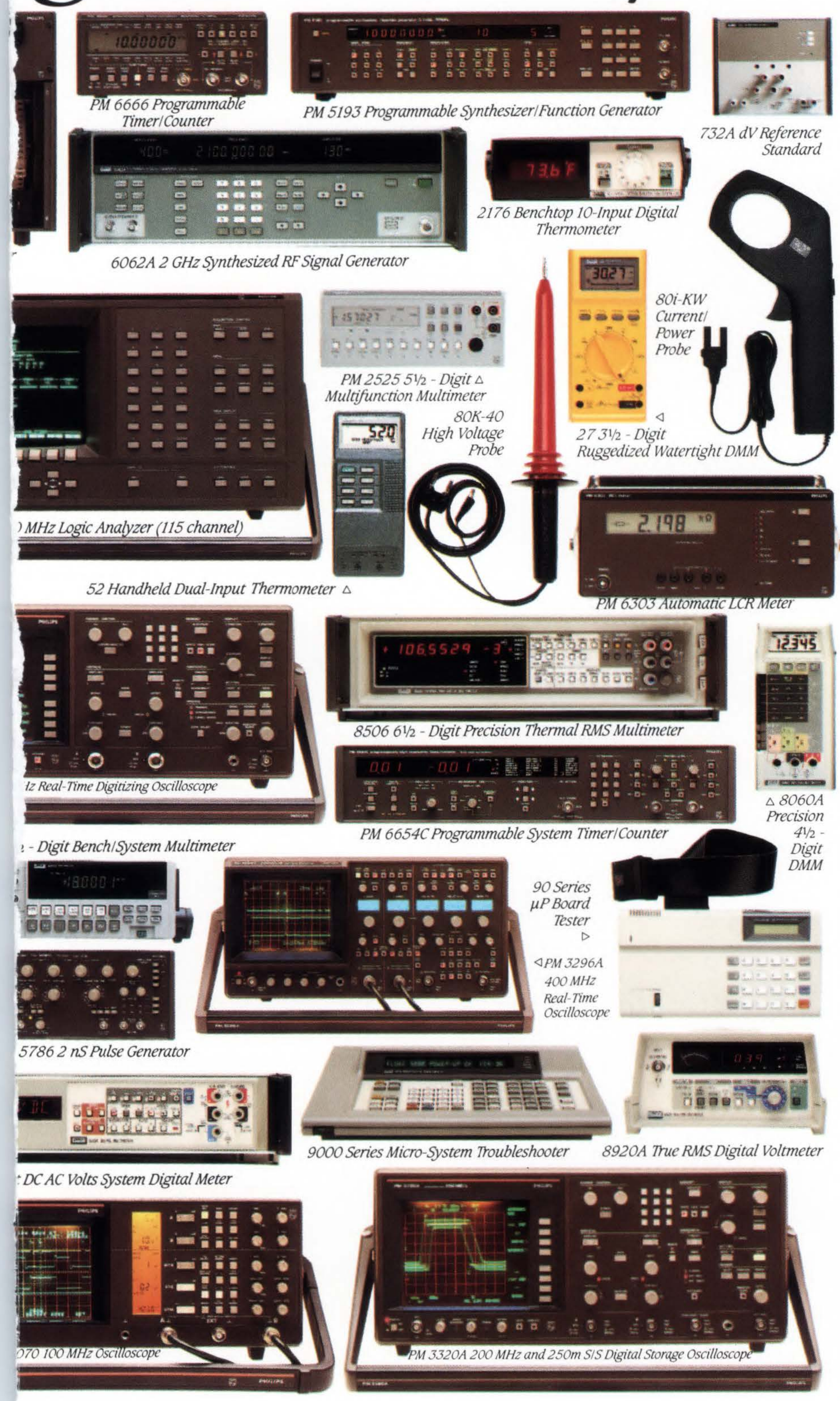

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☐ True ☐ False

2. I am aware that Fluke now sells, services and supports Philips test and measurement equipment in North America.

☐ True ☐ False

3. I don't buy out of habit, or because the salesman bought me a terrific lunch.

☐ True ☐ False

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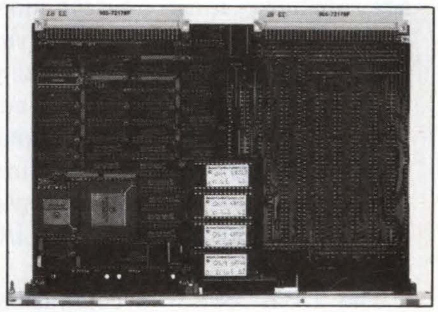
CPU card adds I/O channel to VME Bus systems



The VSC020 CPU card provides a bridge *between the VME and STE Buses. By implementing industrial I/O on the STE Bus, you can dramatically reduce I/O costs.*

The VSC020 CPU card features both VME Bus (IEEE-1014) and STE Bus (IEEE-1000) interfaces, allowing you to use STE Bus boards to implement low-cost industrial I/O in VME Bus systems. Compared to using VME Bus I/O cards, an I/O subsystem based on STE Bus cards reduces I/O costs by as much as 50%. You can also use the CPU card simply to add 32-bit processing power to an STE Bus system. Because both VME and STE Bus cards are based on Eurocard footprint boards with DIN-41612 connectors, it's easy to integrate both buses into the same packaging.

The CPU card includes a 12.5- or 16-MHz (or, optionally, a 20-MHz) 68020 µP, 1M or 4M bytes of onboard dynamic RAM, two serial I/O channels, and a 16-bit counter/timer. The 32-bit VME Bus interface, which occupies the card's P1 connector and the center row of pins on the P2 connector, allows the CPU to operate in a multiprocessor VME Bus environment.

The STE Bus interface occupies the two outer rows of pins on the card's P2 connector. The 1M byte of STE Bus memory space and 4k bytes of STE Bus I/O space appear as fixed locations in the 68020's address map. The CPU can send or receive interrupts on the STE Bus Attention Request signal lines and has a control register that allows you to mask out unwanted interrupts. The CPU can also perform STE Bus Vector Acknowledge cycles to accept an interrupt vector from an interrupting device.

An onboard STE Bus arbiter allows you to add additional bus masters on the STE Bus. For mailbox-type communication between the CPU and other STE Bus masters, you can use a 16k-byte area of the CPU card's dynamic RAM, which is dual-ported to the 68020's local bus and to the STE Bus. The base address of this 16k-byte area is programmable. In addition, the board has STE Bus system controller functions, including STE Bus clock generation, power-on or software-controlled system-reset generation, and a bus time-out function.

The company supports the CPU card with the OS-9/68k real-time multitasking operating system and supplies software drivers for its wide range of STE Bus I/O cards. The VSC020 comprises a VME Bus CPU card manufactured by Io Inc (Tucson, AZ) and a daughter board that carries the STE Bus interface. However, the CPU and daughter-board combination still fits into a single VME or STE Bus slot. £1380.

—Peter Harold

Arcom Control Systems Ltd, Unit 8, Clifton Rd, Cambridge CB1 4WH, UK. Phone (0223) 411200. TLX 94016424. FAX 022-341-0457.

Circle No 729

STD Bus boards provide IBM PC/AT compatibility for industrial applications

Touted by the manufacturer as the first STD Bus controller to offer full IBM PC/AT compatibility with 18 times the performance speed of a standard PC/XT, the STD-AT comprises a set of three plug-in boards that meet the standard 4.5×6.5-in. STD Bus form factor for card cages. The LPM-286AT card contains an 80286 CPU that runs as fast as 16 MHz, with a 20-MHz version scheduled for release next month. The LPM-Video card provides both monochrome and color video processing, and the LPM-Disk board controls your system's hard- and floppy-disk drives.

The LPM-286AT is actually a tightly coupled 2-board set that is joined by a local bus, and if you don't require video and mass-storage capability, it can function independently. Its μP is buffered to the STD Bus, and a dynamic bus-sizing feature automatically determines whether an 8- or a 16-bit signal transfer should occur. An asynchronous I/O bus controller ensures system compatibility with slower I/O cards.

The LPM-286AT is compatible with STD Bus I/O boards, and it comes with 512k bytes of zero-wait-state RAM, Chips and Technologies' New Enhanced AT (NEAT) chip set, two RS-232C ports, a Centronics parallel port, a battery-backed real-time clock, a keyboard controller, an 80287 coprocessor socket, three 16-bit timer/controllers, a BIOS (basic I/O system) ROM with a setup program, and a speaker. The 20-MHz version will have 2M bytes of RAM.

Providing 80286-based PC/AT compatibility on STD Bus cards, *the 16-MHz STD-AT registers an 18.7 performance index relative to an IBM PC/XT computer, based on the Norton benchmark speed test.*

You get 256-color VGA compatibility with resolution as high as 800×600 pixels when you add the LPM-Video card to your system. Supporting a variety of monitors, including monochrome, color, TTL analog, PS/2, and multifrequency, this video controller comes with 9- and 15-pin interfaces and also meets the EGA, CGA, and Hercules standards.

The LPM-Disk card lets the system control rack-mounted mass storage devices storing as much as 100M bytes of data, including 3½- and 5¼-in. floppy-disk drives. You can also add other high-capacity disk drives to your system by connecting them externally.

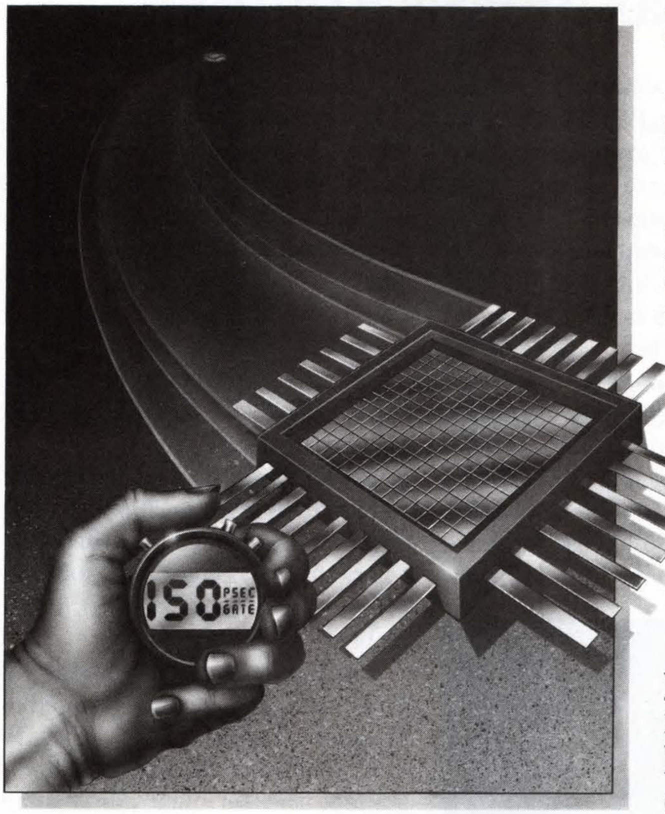
These boards require a 5V power supply and operate over a 0 to 70°C temperature range. Presently available with a 10-, 12-, or 16-MHz CPU, the LPM-286AT pricing begins at $1495. The LPM-Video board costs $525, and the LPM-Disk card sells for $295.

—J D Mosley

WinSystems Inc, Box 121361, Arlington, TX 76012. Phone (817) 274-7553. FAX 817-548-1358.

Circle No 728

SONY'S ECL GATE ARRAY TAKES ON GaAs SPEED.



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And if that's not enough, Sony also offers you free access to our 150-cell library. Augmented by our customer design support center, where we custom design ECL gate-array routines on the Mentor Graphics™ system. Complete with rapid turn-around—typically just eight weeks.

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Number of equivalent gates	210 (3 gates per one internal basic cell)
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For full details, call (714) 229-4197 today. Or write Sony Corporation of America, Component Products Division, 10833 Valley View Street, Cypress, California 90630. FAX (714) 229-4271.

SONY®

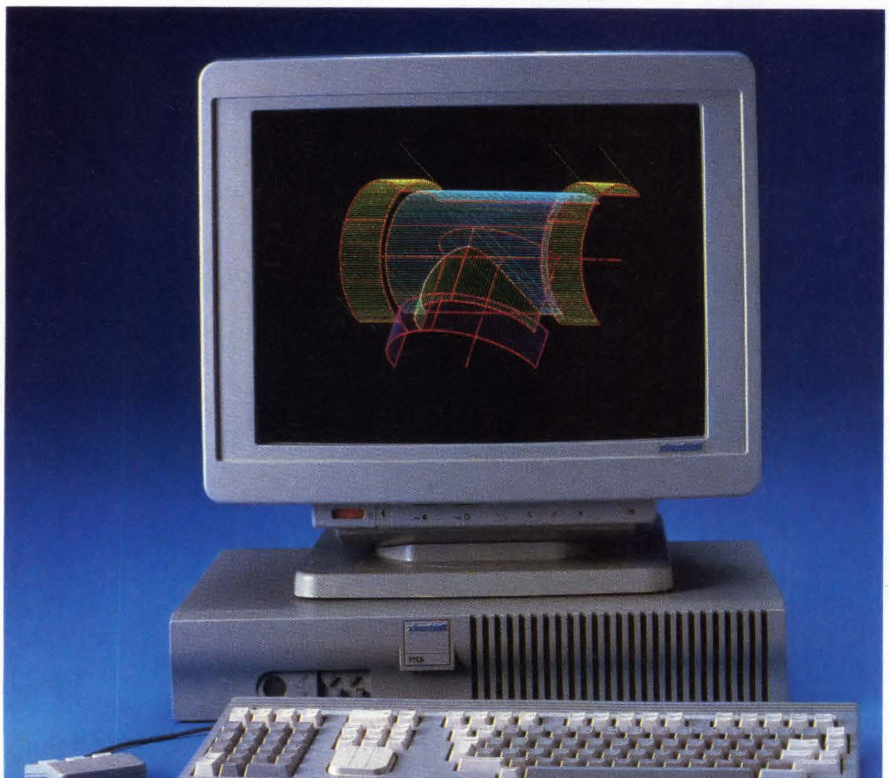
CIRCLE NO 165

Graphics terminal offers RS-232C, TCP/IP-based LAN, and IBM coax interface options

The Model 4211 Graphics Netstation includes a dedicated graphics engine and can interface to host computers via RS-232C ports, a TCP/IP-based (Transmission Control Protocol/Internet Protocol) Ethernet LAN, or an IBM 3270 coaxial connection. The graphics engine features a redraw rate of 40,000 transformed and clipped 2D vectors/sec. You can specify your choice of a 15- or a 19-in. color monitor for the graphics terminal.

The Graphics Netstation employs a dual-processor architecture to attain the graphics performance and the flexible connectivity it offers. A TI TMS34010 μP and three gate arrays handle the graphics-processing tasks. The gate arrays implement functions such as dedicated transformed and clipped ALUs. An Intel 386SX μP handles I/O and data-management tasks.

Although it offers a fivefold increase in redraw rate compared with the company's 4111 terminal, the 4211 maintains compatibility with the older product. Therefore you can use the Graphics Netstation with more than 100,000 software applications developed for 4111 and 4200 terminals.



A ***redraw rate of 40,000 vectors/sec*** *and the flexible connectivity scheme make the 4211 graphics terminal as functional as many workstations.*

The graphics terminal runs applications from the company's Plot 10 family and from many third parties. For hardcopy output, the terminal supports all of the company's inkjet and thermal wax printers, the HP Laserjet and Thinkjet, and Epson printers.

The basic configuration includes three RS-232C ports, a parallel port, a keyboard, and 0.75M bytes of RAM. The standard 15-in. monitor features a 1024 × 768-pixel resolution. The terminal can display 16 colors from a palette of 4096 and offers four dedicated dialogue planes.

The communications options cost $750 each and come packaged on modular plug-in boards. With the IBM 3270 coaxial-cable option installed, the terminal can manage five 3270 sessions and one ASCII host session simultaneously. The LAN option consists of a TCP/IP-based Ethernet interface. The TCP/IP implementation includes the Telnet virtual-terminal facility. And, you can use the LAN-equipped 4211 as a terminal to any TCP/IP-based host on a network. The basic configuration sells for $6495, and an optional 19-in. monitor costs $1500. Volume shipments are scheduled for November.

—Maury Wright

Tektronix Inc, Box 14689, Portland, OR 97215. Phone (800) 225-5434.

Circle No 727

SRAMs' on-chip address and data latches boost throughput in pipelined systems

You can easily place the TR9C1640 and TR9C1643 16k×4-bit static RAMs (SRAMs) into your existing designs, because they are compatible with the operation of unlatched SRAMs and employ industry-standard pinouts. However, these SRAMS also incorporate address and data latches that enhance the system performance of the memories. The integral address latch frees the system address bus after the device has been enabled, and the transparent data latch gives your system extra time to accept previously fetched data while the SRAM executes a new read cycle.

Both SRAMs employ a common bus for the four DQ data I/O lines. The TR9C1640, packaged in a 22-pin DIP, has two control lines: $\overline{E}$ (enable) and $\overline{W}$ (write). The falling edge of the enable signal initiates a memory cycle and freezes the address in the SRAM's address registers. After this falling edge on the $\overline{E}$ input, your system can change the state of the address lines without affecting the current memory cycle. Pipelined memory systems frequently need this extra latitude on address-line timing.

During a read cycle, the write control line remains high, which turns on the SRAM's data output drivers. When the read cycle ends, the data retrieved during the cycle is latched in the device's output data latch by the rising edge of the $\overline{E}$ signal. Note in **Fig 1** that the enable line has no control over the SRAM's data output drivers. Thus, the data lines will stay valid even after the read cycle completes. This extra hold time eases data-bus tim-

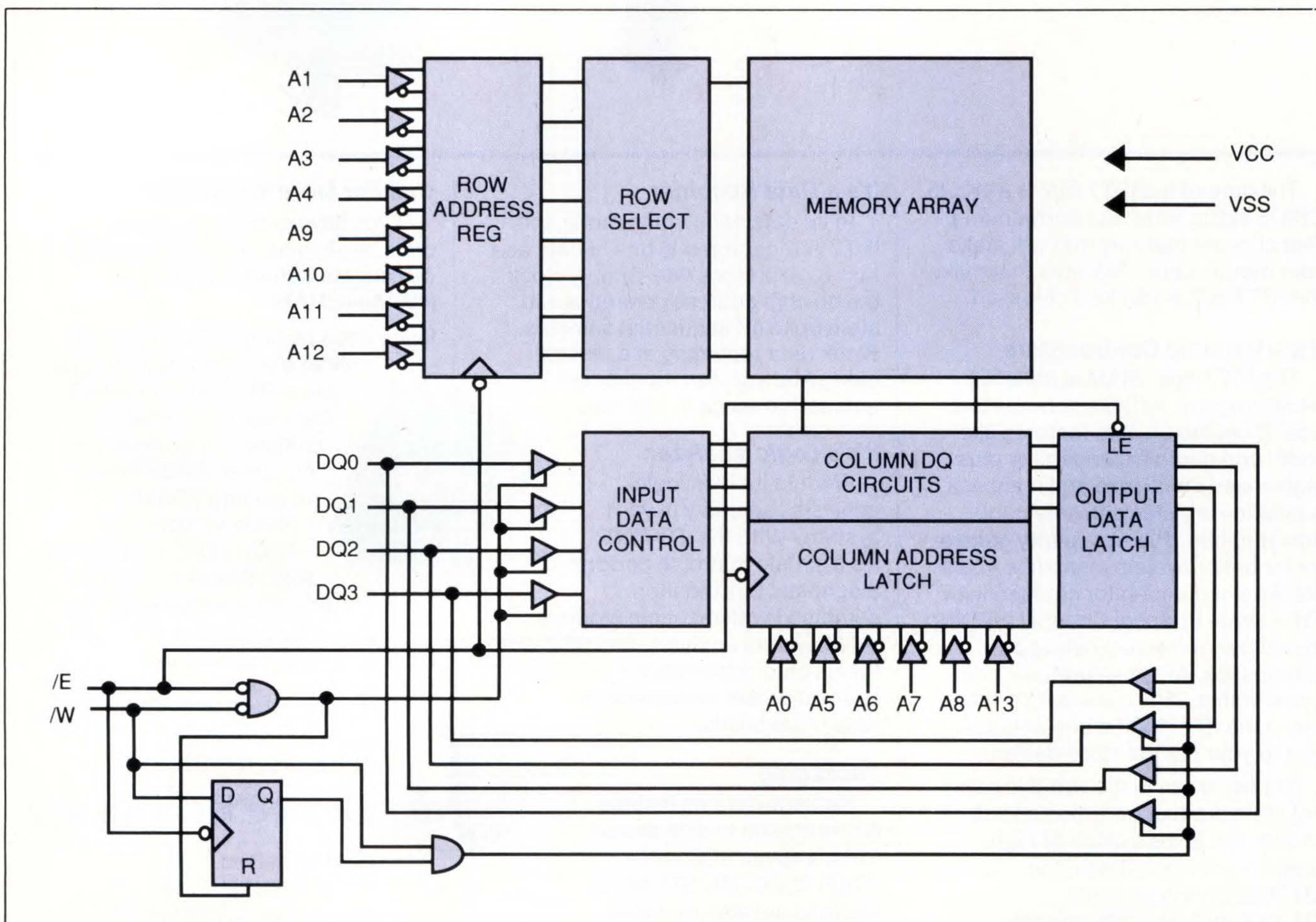


Fig 1—Integral address and data latches *on a pair of SRAMs ease timing problems in high-speed, pipelined applications.*

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Silicon General PWM's are offered in voltage mode, current mode, and voltage and current modes. They are available in ceramic, plastic and surface mount. The General processes PWM's and supervisory circuits to 883B, Rev. C and S Level. All standard package types are offered including SOIC, PLCC, LCC, and flat pack.

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SG1524B	SG3524B
SG1525A	SG3525A
SG1526	SG3526
SG1526B	SG3526B
	SG3526A
SG1527A	SG3527A
SG1529	SG3529
Current Mode	
SG1825	SG3825
SG1842	SG3842
SG1843	SG3843
SG1844	SG3844
SG1845	SG3845
SG1846	SG3846
SG1847	SG3847
Current and Voltage Mode	
SG1528*	SG3528*
SG1530*	SG3530*

*Available January 1989

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SILICON GENERAL

CIRCLE NO 178

ing in high-speed systems.

Both the enable and the write control lines can initiate or terminate a write cycle. The last falling edge on either $\overline{E}$ or $\overline{W}$ starts the write operation. Likewise, the first rising edge on $\overline{E}$ or $\overline{W}$ terminates the write cycle. Data set-up and hold times are referenced to the signal edge that terminates the write operation.

During a TR9C1640 write cycle initiated by the write control line ($\overline{E}$ is asserted first), the SRAM will drive the DQ lines until $\overline{W}$ is asserted. The assertion of $\overline{W}$ causes data-bus conflicts in some systems, so the TR9C1643 adds a $\overline{G}$ control line that gives you an extra way to shut off the SRAM's output drivers. Because the $\overline{G}$ output enable adds an extra pin, the TR9C1643 is packaged in a 24-pin DIP.

The company offers both the TR9C1640 and the TR9C1643 in 25-, 35-, and 45-nsec versions for \$15.75, \$12.75, and \$9.25 (1000), respectively.—***Steven H Leibson***

Triad Semiconductors, Inc, 5575 Tech Center Dr, Suite 120, Colorado Springs, CO 80919. Phone (719) 528-8574. FAX 719-528-8875.

Circle No 726

42 favorite PLD flavors. Now in two 12 ns GAL® parts.

It's not uncommon to crave extra speed from a standard PLD. But until now it's been nearly impossible to find a device in your favorite flavor with the speed you really need.

That's why Lattice Semiconductor offers the GAL16V8A and GAL20V8A. Together they give you 42 standard PLD types, including most PAL® devices. All at 12 ns. The largest selection of high-speed PLDs.

Bipolar speed at half power.

These two GAL devices don't just give you 12 ns gate delays. With Lattice's E²CMOS™ technology, they give you 12 ns at half the power of bipolar PLDs.

Lattice GAL devices also help you reduce inventory–without sacrificing design options. Stocking two flexible GAL devices is like stocking 42 standard PLDs.

This unique flexibility comes from Lattice's proprietary Generic Array Logic (GAL) architecture. With output logic macrocells (OLMC), it's an architecture that lets you configure outputs to emulate a wide variety of PLDs.

Near-perfect quality.

Unlike other PLDs which are statistically tested, Lattice tests every characteristic on every part. Repeatedly. As a result, functionality, AC/DC performance, programmability and specifications are guaranteed.

The benefit of all this testing is near-perfect quality. Combined with GAL device programmability and reuseability, this significantly reduces the cost of PLD ownership.

Standard tool support.

Since GAL devices are pin-for-pin compatible with standard 20 and 24 pin PALs, you can continue using the same fuse maps you've used all along. And standard programming tools as well.

So order your free copy of the Lattice GAL Data Book today. Then, next time you need fast PLDs, be sure to specify GAL devices. In just two parts you'll discover 42 favorite flavors. From Lattice Semiconductor, of course. With more fast PLDs than anyone else.

Lattice Semiconductor Corporation™

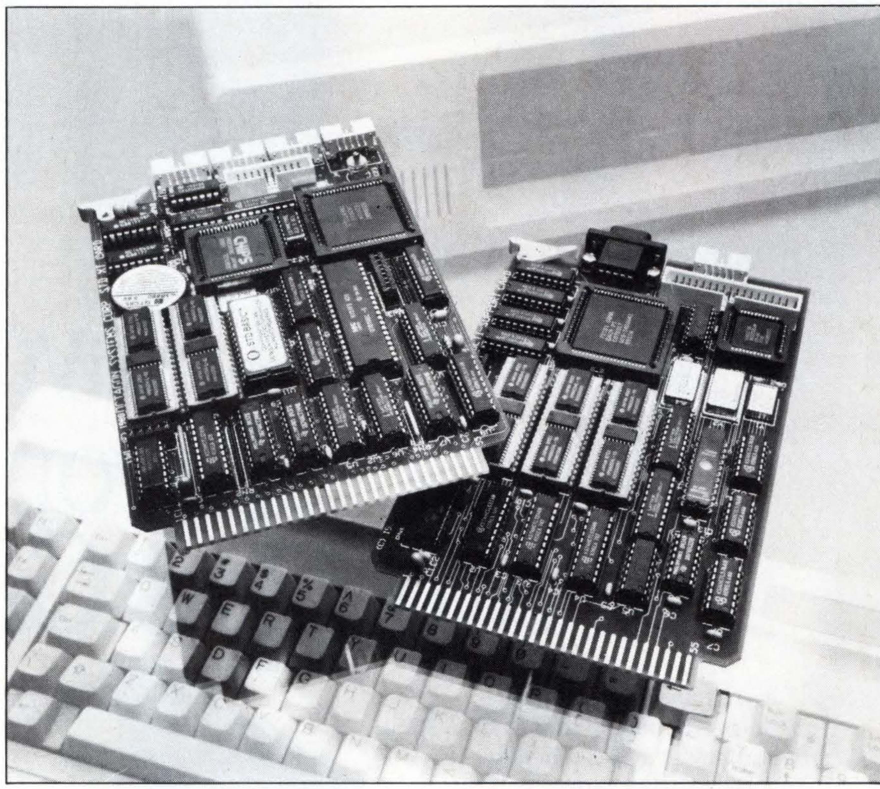
5555 N.E. Moore Ct. • Hillsboro, OR. 97124

For Literature Circle 13
For Employment Information Circle 14

The GAL Revolution Starts Here℠

Single-board computer for the STD Bus combines IBM PC features and ROM Basic

The XT-7 card set brings IBM-PC compatibility to the STD Bus by incorporating into its design several ICs originally created for IBM-PC-clone mother boards. The $795 XT-7 CPU card features an NEC V20 μP running at 7.15 MHz, two serial ports, a parallel printer port, 128k bytes of static RAM (SRAM) with room for an additional 128k bytes, a standard PC keyboard interface, a real-time clock, and a battery to maintain the state of the RAM and clock when the system is turned off. You can build an STD Bus system using just the XT-7 CPU card or you can replicate the entire repertoire of IBM PC features by plugging in the $495 XT-7 support card, which adds a floppy-disk controller, a color-graphics-adapter (CGA) video controller, 128k bytes of battery-backed SRAM, and room for an additional 256k bytes of SRAM.



ICs created for clone mother boards and a standard BIOS ROM *allow this 2-card computer for the STD Bus to use any software developed for the IBM PC.*

A chip from Western Digital (Irvine, CA) supplies the XT-7 CPU card with components of the IBM PC mother board, including the keyboard interface, interrupt and DMA controllers, timers, and clock generator. A second IC, from Chips and Technologies Inc (San Jose, CA), adds the serial and parallel I/O ports and the real-time clock. These two ICs are commonly used by a variety of manufacturers to build IBM PC-clone mother boards.

Both XT-7 cards employ only CMOS devices to minimize power consumption—the CPU card dissipates 1.8W and the support card only 1.4W. In addition, the company offers a 3½-in. floppy-disk drive that requires only 1W, bringing the total power dissipation of an XT-7 system to 4.2W. This low power consumption brings two key benefits: it boosts component reliability by reducing the system's operating temperature, and it allows you to place the XT-7 card set in a sealed enclosure without creating heat problems.

Phoenix Software Associates Ltd (Norwood, MA), a company that specializes in BIOS ROMs for IBM PC-compatible machines, supplied the BIOS (basic I/O system) software for the card set. Phoenix accommodated the addition of the STD Bus interface with only minor changes to its standard software package. The standard hardware and BIOS incorporated into the XT-7 CPU card allows the company to offer the following guarantee of software compatibility: it will refund your money if your software runs on an IBM PC/XT but won't run on the XT-7.

The XT-7's ROM also contains STD Basic III, the company's latest incarnation of its extended Basic language for industrial-control applications. STD Basic III incorporates a disk operating system that is compatible with the MS-DOS file structures and several specialized statements for applications that require real-time control. For example, the STD Basic III function "Interval" returns the time interval between successive pulses and works with any bit of any input port in the system. The function can return the value of this period as a frequency (Hz), a tachometer reading (RPM), or as a pulse width.

The language also implements

UPDATE

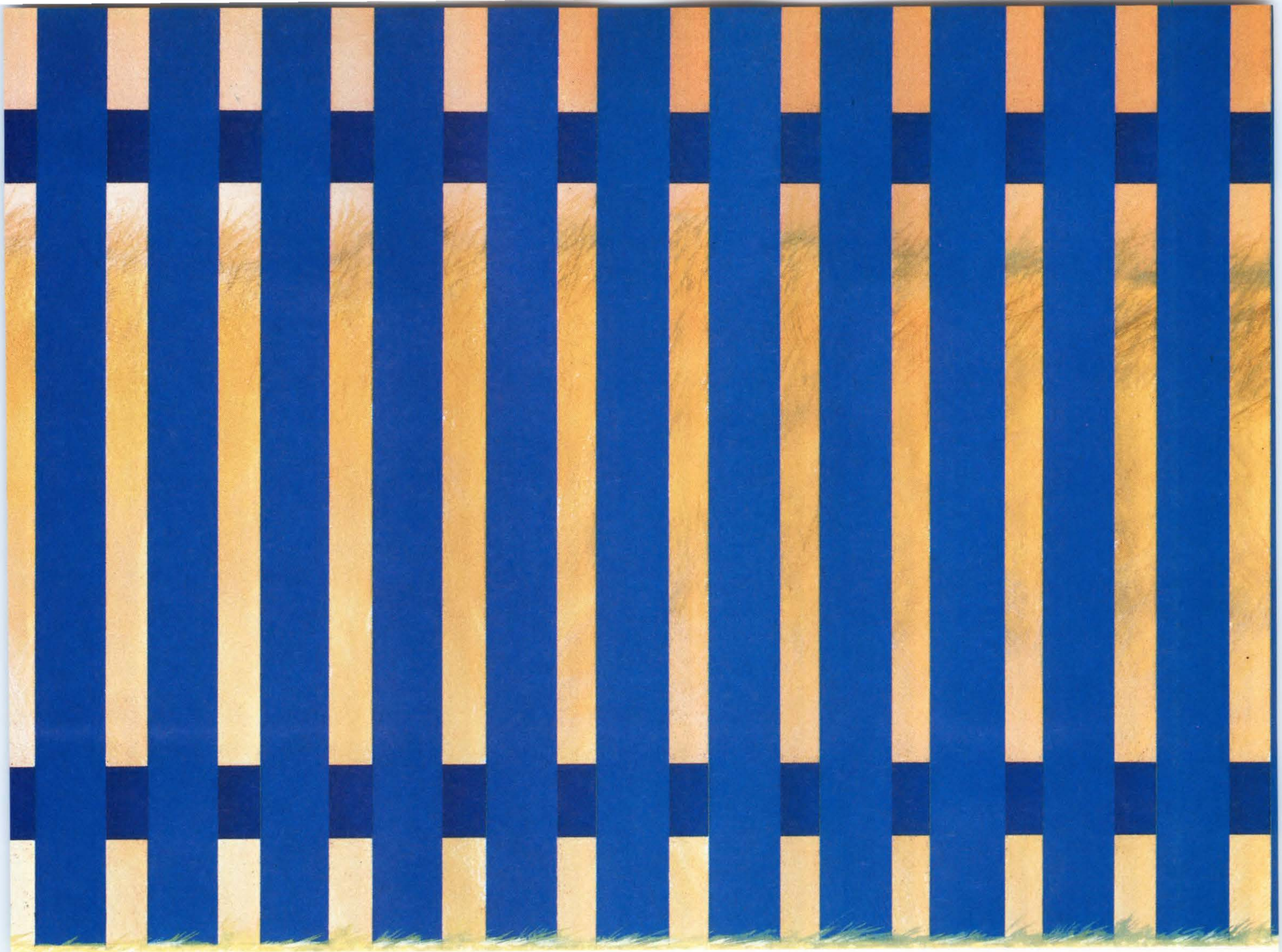
hardware-interrupt-driven routines and event-driven multitasking. A hardware interrupt causes STD Basic III to set a software flag. You link interrupts to flags with a program statement. If a flag is set at the completion of a line of code, STD Basic III executes the appropriate interrupt subroutine. You write the subroutines in Basic.

Event-driven multitasking switches execution from one subroutine to the next if preset conditions, which you define in an "Event" statement, occur. Once you define an event condition, STD Basic III polls the status of the events after executing a user-defined number of lines of program code. If an event occurs, program execution jumps to the designated routine. The company claims that event-driven multitasking produces far more efficient multitasking programs than time slicing, because only tasks that require service consume processor time.

In addition to the STD Basic language, you can write programs for the XT-7 using any MS-DOS programming language designed to run on an IBM PC. You can store your program on a floppy disk, using the floppy controller on the XT-7 support card, or put your program into ROM, using the STD-DOS utility routines supplied with the XT-7 CPU card.—***Steven H Leibson***

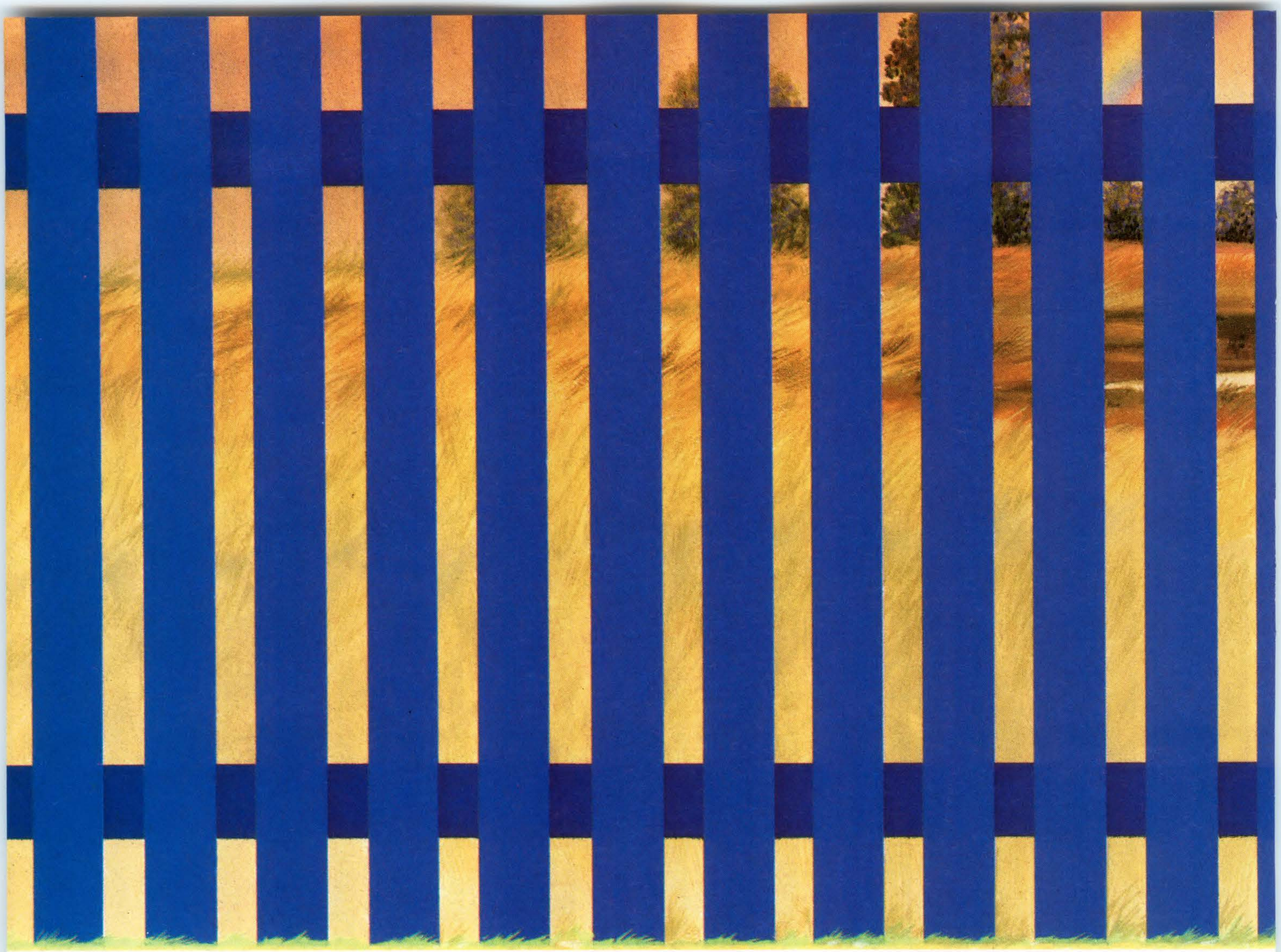
Octagon Systems Corp, 6510 W 91st Ave, Westminster, CO 80030. Phone (303) 426- 8540.

Circle No 725



VGA

Others promise 100% register-level compatibility.



Only the CHIPS/450™ family gives you VGA™ compatibility at the gate level.

Everyone claims their VGA-compatible chips offer 100% compatibility with the industry standard. Which only means they've implemented VGA functions at the register level, right out of the IBM® reference manual.

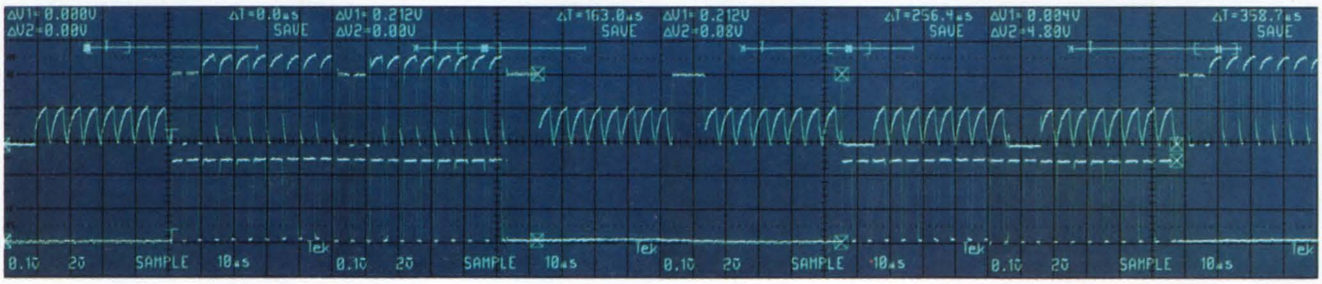
But to achieve *real* VGA compatibility, it takes a much sharper focus. Down to the individual silicon gates used to build each and every register. Only one family of VGA CHIPSets™ does that: CHIPS/450.

That's why only the CHIPS/450 family can guarantee 100% VGA hardware compatibility, including implementation of hidden modes and other functions not thoroughly described in IBM's PS/2® Technical Reference. Features like a high-resolution mode, special zoom functions and readable CPU latches. Features that IBM and software developers might make use of in the future. Sending your design back to the drawing board if your "VGA-compatible" chip set isn't *gate-level* compatible.

Leave others at the starting gate.

Besides uncompromising compatibility, the CHIPS/450 family gives you gate-crashing graphics performance. Especially when tightly coupled with our industry leading system logic CHIPSets. Both our VGA and Super VGA controllers offer a proprietary 16-bit interface and *fast* VGA cycles—delivering *twice the performance* of the industry standard. Both include enhanced backward compatibility with all the popular video modes, and special protection

Digital scopes with a

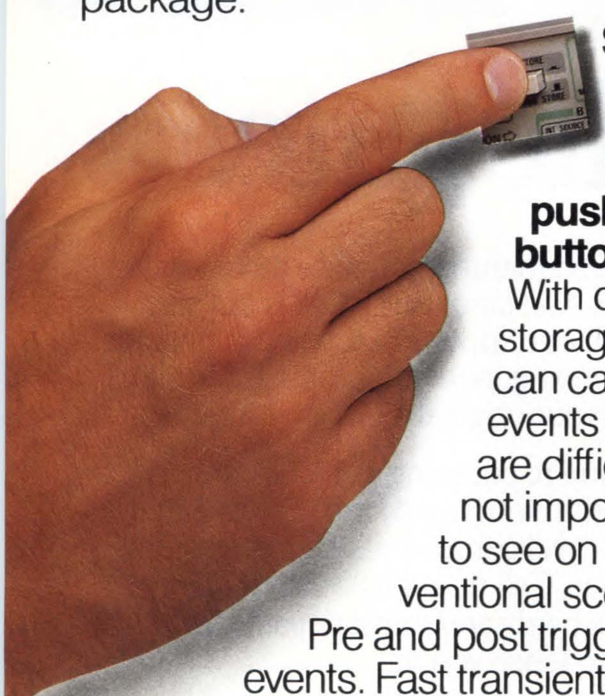


Four screen photos spliced end to end illustrate the benefit of full four-screen capture using the 2230's 4K record length.

Give up real-time capability for storage? Not with Tek!

That's because analog capability is integral to low-cost Tek digital storage oscilloscopes. So you need only one instrument to make all your measurements efficiently. With no trade-offs.

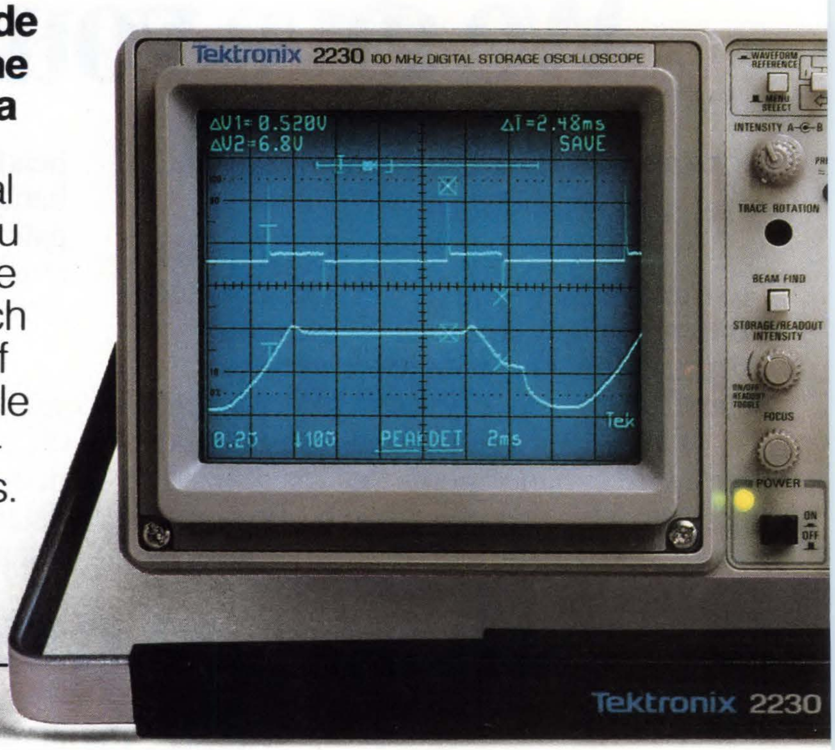
It's another Tek advantage: analog and digital in one familiar, affordable package.



Select either mode at the push of a button.

With digital storage you can capture events which are difficult if not impossible to see on conventional scopes. Pre and post trigger events. Fast transients. Single-shot events. Elusive glitches. Low-speed phenomena.

Any waveform can be viewed for as long as you like. Or stored in 4K of memory for later analysis or comparison to other waveforms. And if there's a question about a digital measurement, just push a button for real-time display analysis.



real-time advantage.

The affordable portables.

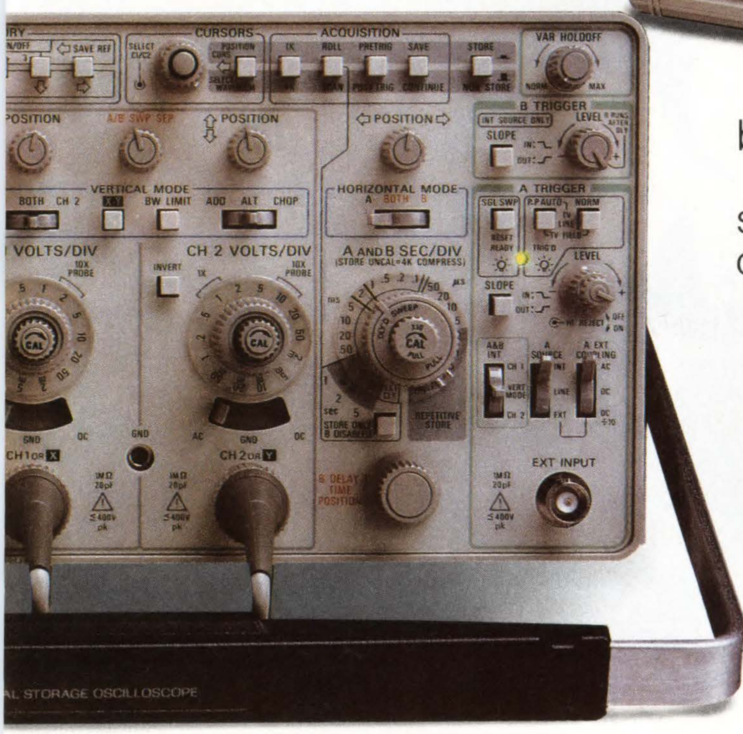
These are the world's best-selling digital storage oscilloscopes. And with the new 50 MHz Tek 2210 joining the family, there's now an even better selection—in bandwidth, performance and price.

Select for advanced features such as 100 ns glitch capture at any sweep speed, CRT readout, measurement cursors, multiple acquisition modes and hardcopy output, plus optional GPIB or RS-232C interfaces and software.

These scopes are perfect for first-time digital users. And seasoned operators will appreciate even more their versatility, convenience and value. All backed by Tek quality and a 3-year warranty.

Features	2230	2221	2220	2210
Bandwidth	100 MHz	60 MHz	60 MHz	50 MHz
Max. Sampling Speed	20 MS/s	20 MS/s	20 MS/s	20 MS/s
Vertical Resolution	8-12 bits	8-10 bits	8 bits	8 bits
Record Length	4K	4K	4K	4K
Glitch Capture	100 ns	100 ns	100 ns	No
CRT Readout/ Cursors	Yes	Yes	No	No
GPIB/RS-232-C Options	Yes	Yes	Yes	No
Warranty	3-years on labor and parts including CRT			
Price	$4995	$3995	$2995	$2395

Each scope offers a range of capabilities you'd expect to find only in much more expensive instruments.



Discover the potential. Let Tek show you what you're missing... without making you give up analog to see it. That's the real-time advantage of Tek digital storage.

For easy ordering or more information call Tek Direct:

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VISA, MasterCard

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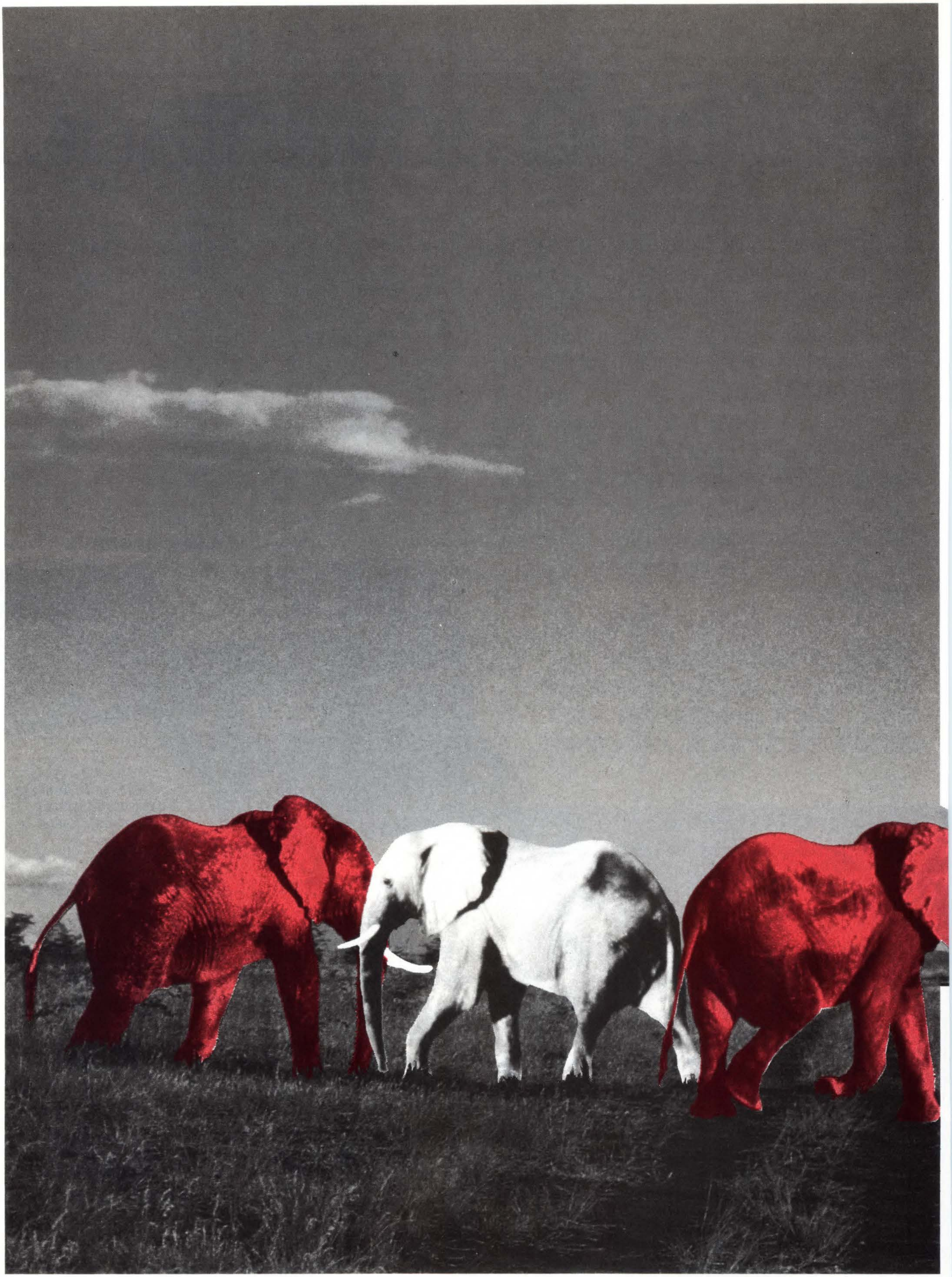
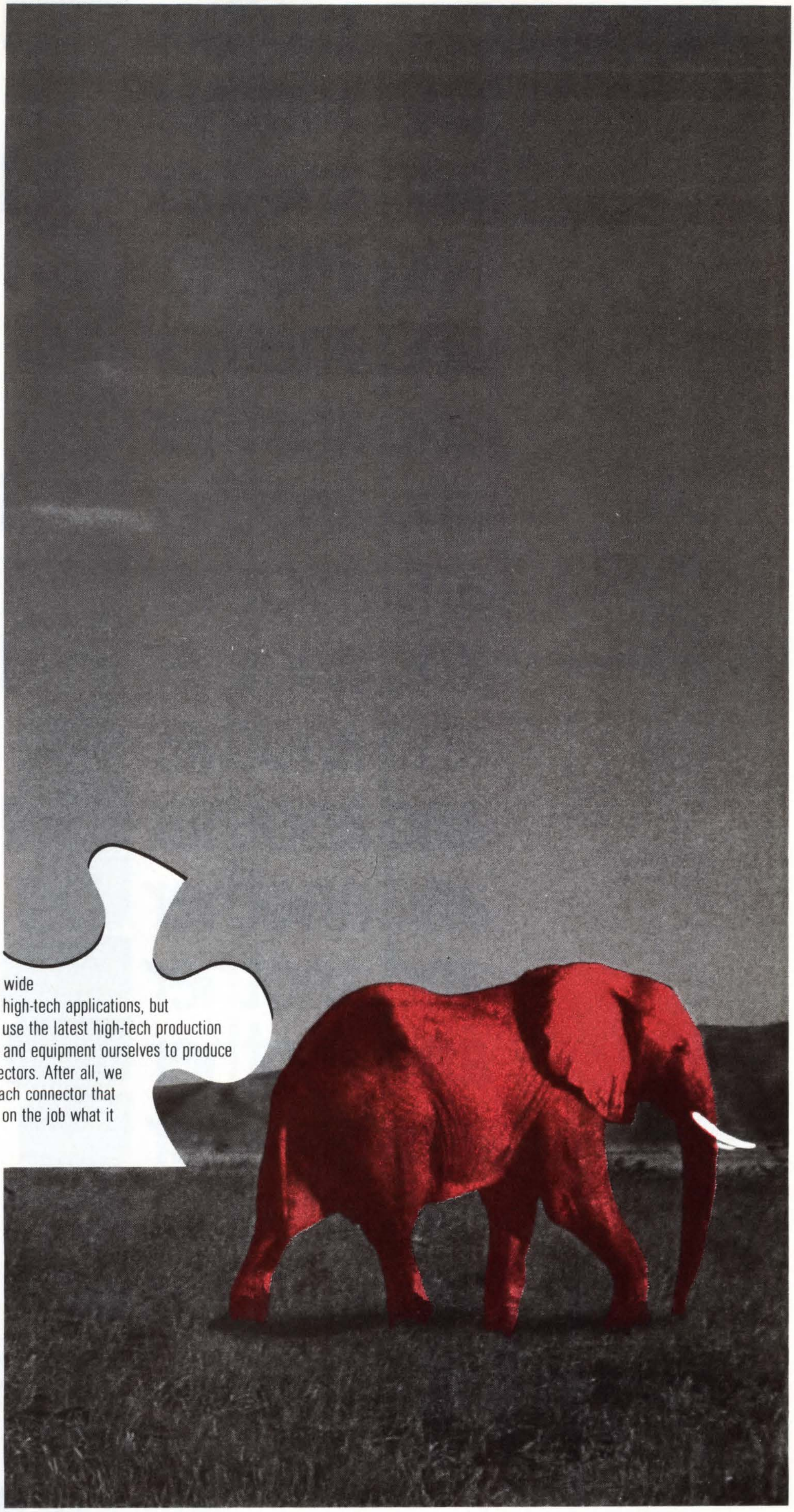
CIRCLE NO 187





Sorry, no checks for Intel ICE.

	AMC	Intel
▶ Supports the new 16 MHz 80C186 and 80C188 as well as other Intel CPUs at full speeds with no wait states	✓	
▶ VALIDATE/Soft-Scope is a complete in-circuit source level debugger that shows variables, data structures and assembly instructions	✓	
▶ VALIDATE/Soft-Scope has in-circuit source level debug capability in 286 protect mode	✓	
▶ Tool chain supports Microsoft C (Also other versions of C and Pascal, FORTRAN, PL/M, Assembler, Jovial)	✓	
▶ Add processor support by merely adding emulator board and probe module	✓	
▶ Has unlimited breakpoint capability	✓	
▶ Over a megabyte of overlay memory is available	✓	

Just because you've bought one of those great Intel chips is no reason to buy Intel development tools.

Why? Because Applied Microsystems is better. That's a fact. Our checklist proves it.

Intel chips are state-of-the-art, but their development tools aren't. Compared to ours, Intel's ICE is limited, slow and awkward.

If you want to design, debug and integrate your target system faster, easier and more completely, you need to turn to Applied Microsystems. It's the only comprehensive solution in the business. Which includes not only the most complete and most reliable tool chain, but also all the help you need from our field applications engineers and sales engineers.

What's more, we keep adding more checks to our list. Like dynamic trace that lets you review performance while the target is still running. And we use an SCSI interface that downloads code at disk speeds 20 times faster than RS232 connections. We offer performance measurement capability without making you spend an extra $10,000.

As you can plainly see, there's only one development environment really worth checking out.

To find out more, call toll free (800) 426-3925. (In Washington (206) 882-2000.) Or write Applied Microsystems Corporation, P.O. Box 97002, Redmond, Washington, USA 98073-9702.

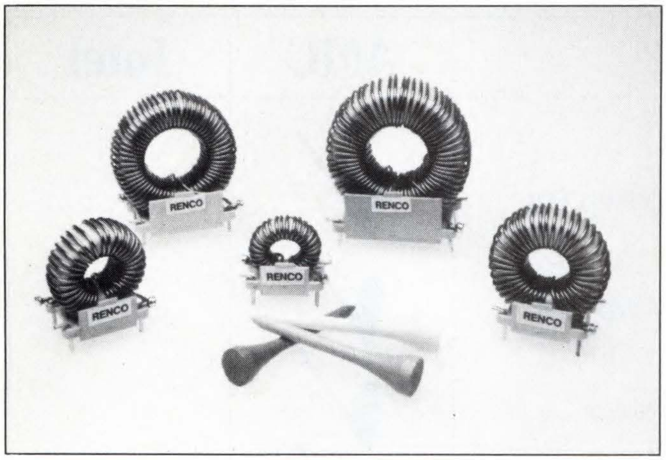
Applied Microsystems Corporation

In Europe contact Applied Microsystems Corporation Ltd., Chiltern Court, High Street, Wendover, Aylesbury, Bucks, HP22 6EP, United Kingdom. Call 44-(0)-296-625462.
In Japan contact Applied Microsystems Japan, Ltd., Nihon Seimei Nishi-Gotanda Building, 7-24-5 Nishi-Gotanda Shinagawa-KU, Tokyo T 141 Japan. Call 03-493-0770.

CIRCLE NO 66

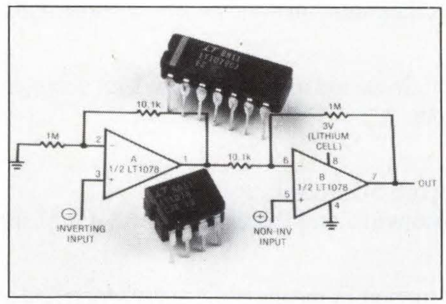
READERS' CHOICE

Of all the new products covered in EDN's **June 23, 1988,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, refer to the indicated pages in our **June 23, 1988,** issue, or use EDN's Express Request service.



◄ INDUCTORS

RL5118 Series controlled-saturation toroidal inductors are available in five core sizes that range from 1 to 5600 μH with current ratings of 2 to 22A (pg 188).
Renco Electronics Inc.
Circle No 602

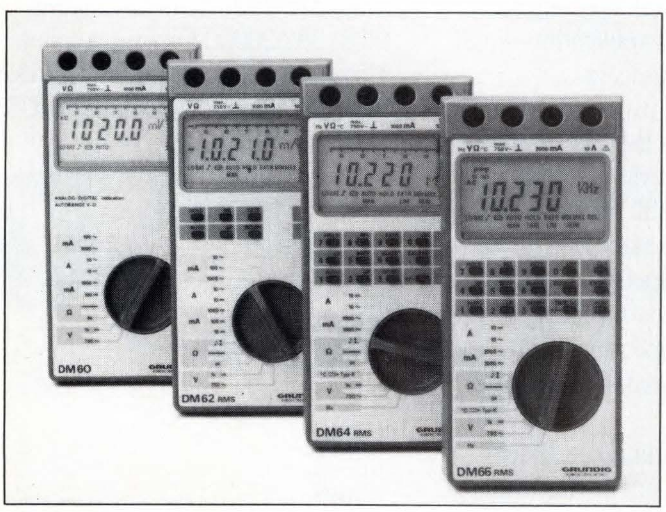


OPTICAL-DISK DRIVES

The 3½-in. Fiji disk drive and the 5¼-in. Tahiti I disk drive employ erasable magneto-optic recording technology and store 160M and 1G bytes of information, respectively (pg 98).
Maxtor Corp.
Circle No 601

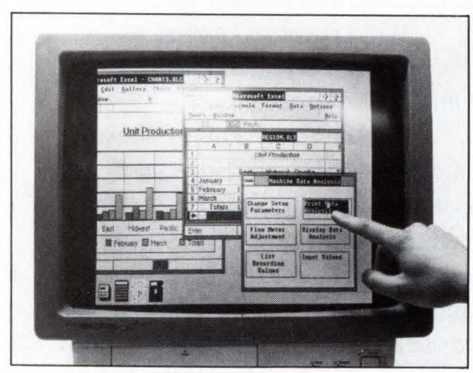
▲ PRECISION OP AMPS

The dual LT1078 and quad LT1079 op amps operate from a 5V supply and consume only 50 μA per amplifier (pg 222).
Linear Technology Corp.
Circle No 603



▲ HANDHELD DMMs

The DM Series handheld autoranging digital multimeters comprise four models that provide 4- or 4½-digit resolution (pg 258).
Grundig AG.
Circle No 605



▲ TOUCHSCREEN DRIVER

Touch WindowsDriver lets you use a touchscreen instead of a mouse to operate any software that runs under Microsoft's Windows (pg 244).
Micro Touch Systems Inc.
Circle No 604


Finally,
a really important
phone message.

AMD and Siemens have signed an agreement to work together on ISDN. They'll co-develop, manufacture, and offer support for a line of components for terminals and switching applications. All the parts are second sourced. And that should make your life a lot easier.

ISDN for people who aren't professional gamblers.

One of the most important things about any system is the right standard, agreed?

And any company can develop a standard.

But Siemens and AMD will meet the IOM™-2 standard. IOM-2 is Siemens' implementation of the General Communications Interface. It gives you a cost effective way of interconnecting chips into any ISDN application.

This interface was jointly defined and supported by lots of system manufacturers including companies like Alcatel, Italtel, Plessey, and of course, Siemens.

And it's a safe bet none of these companies make a decision lightly.

Besides representing a widely accepted standard, our devices are proven. The majority of the ISDN designs in the field or in progress are based on components from either Siemens or AMD.

And this is the first complete line of ISDN components with second sourcing. So you'll never have to worry about finding parts.

Hitachi's Hi-BiCMOS™ Process Makes High-speed, Energy-efficient Performance a Reality

Hummingbirds are light, agile, and incredibly fast. They consume energy efficiently as they dart from flower to flower, beating their wings faster than the human eye can follow. This kind of high-speed, power-efficient performance has not been available in a semiconductor—until now. Finally, no compromises.

Hitachi brings you second generation Bi-CMOS—Hi-BiCMOS—the advanced process technology that delivers ECL-like speed with power consumption comparable to CMOS. Hi-BiCMOS transcends generic Bi-CMOS by intermixing bipolar and CMOS structures at the basic cell level, for power-efficient, high-speed performance.

Hitachi has more than three years' experience fabricating Hi-BiCMOS parts. We've refined Hi-BiCMOS into a reliable, high-yield process. You're assured of a dependable supply of devices, in production quantities—all with Hitachi's legendary quality.

A broad variety of mainstream devices, with leading edge performance, is now available as a result of Hitachi's Hi-BiCMOS process. Hitachi's newest 1M DRAMs use Hi-BiCMOS to achieve a fantastic 35ns access time. These fast memories feature high-performance with non-multiplexed addressing. They come in cool-running plastic packaging, and perform at half the access time of standard high-speed DRAMs.

Hitachi's Hi-BiCMOS SRAMs deliver 256K densities, with TTL I/O and 20ns access speeds.

No Compromises

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	34	33	33	0	0	**8.7**	**8.3**
Pot-Core	0	13	61	13	13	0	**10.5**	**8.1**
Laminate (power)	0	18	64	18	0	0	**8.4**	**9.5**
CONNECTORS								
Military panel	0	0	83	17	0	0	**9.2**	**12.9**
Flat/Cable	10	50	30	10	0	0	**5.4**	**6.6**
Multi-pin circular	13	13	48	13	13	0	**9.5**	**11.3**
PC (2-piece)	0	60	20	20	0	0	**6.4**	**7.8**
RF/Coaxial	0	33	58	9	0	0	**7.0**	**6.5**
Socket	8	38	38	16	0	0	**6.6**	**6.3**
Terminal blocks	20	40	33	7	0	0	**4.9**	**3.6**
Edge card	8	46	38	8	0	0	**5.6**	**6.7**
D-Subminiature	21	50	21	8	0	0	**4.4**	**5.2**
Rack & panel	11	33	23	33	0	0	**7.9**	**8.4**
Power	22	44	12	22	0	0	**5.6**	**6.3**
PRINTED CIRCUIT BOARDS								
Single sided	0	60	40	0	0	0	**4.9**	**5.3**
Double sided	0	50	50	0	0	0	**5.4**	**5.9**
Multi-layer	0	20	80	0	0	0	**6.9**	**8.5**
Prototype	0	94	6	0	0	0	**3.3**	**3.2**
RESISTORS								
Carbon film	29	35	24	12	0	0	**4.8**	**4.2**
Carbon composition	35	24	29	12	0	0	**4.9**	**5.4**
Metal film	33	27	33	7	0	0	**4.5**	**4.6**
Metal oxide	33	22	33	12	0	0	**5.1**	**5.0**
Wirewound	25	13	49	13	0	0	**6.3**	**6.4**
Potentiometers	22	17	44	17	0	0	**6.6**	**6.5**
Networks	14	50	21	15	0	0	**5.5**	**6.2**
FUSES	25	44	31	0	0	0	**3.8**	**3.6**
SWITCHES								
Pushbutton	7	53	33	7	0	0	**5.3**	**5.8**
Rotary	15	38	31	16	0	0	**6.1**	**7.5**
Rocker	0	58	33	9	0	0	**5.7**	**5.9**
Thumbwheel	10	50	20	10	10	0	**7.1**	**8.6**
Snap action	0	43	43	14	0	0	**6.9**	**6.2**
Momentary	11	56	22	11	0	0	**5.1**	**6.1**
Dual-in-line	0	56	33	11	0	0	**6.0**	**6.1**
WIRE AND CABLE								
Coaxial	0	58	42	0	0	0	**5.1**	**3.7**
Flat ribbon	13	67	20	0	0	0	**3.6**	**3.5**
Multiconductor	13	53	27	7	0	0	**4.8**	**3.4**
Hookup	29	47	24	0	0	0	**3.3**	**2.4**
Wirewrap	36	36	28	0	0	0	**3.3**	**4.1**
Power cords	18	29	41	12	0	0	**6.0**	**4.7**
POWER SUPPLIES								
Switcher	0	40	40	20	0	0	**7.4**	**10.4**
Linear	0	44	44	12	0	0	**6.6**	**7.8**
CIRCUIT BREAKERS	9	45	18	18	10	0	**8.1**	**7.1**
HEAT SINKS	33	25	25	17	0	0	**5.3**	**5.8**
BATTERIES								
Lithium coin cells	18	36	36	10	0	0	**5.5**	**5.1**
9V alkaline	27	37	36	0	0	0	**3.9**	**3.6**
Real-time clock back-up	0	33	67	0	0	0	**6.3**	**7.6**
RELAYS								
General purpose	13	47	20	20	0	0	**6.1**	**6.2**
PC board	0	44	25	31	0	0	**8.1**	**8.6**

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
Dry reed	0	22	56	22	0	0	**8.5**	**7.2**
Mercury	0	17	33	50	0	0	**10.8**	**7.6**
Solid state	9	10	36	45	0	0	**10.1**	**8.7**
DISCRETE SEMICONDUCTORS								
Diode	26	32	26	16	0	0	**5.5**	**6.1**
Zener	25	37	19	19	0	0	**5.5**	**5.4**
Thyristor	14	36	29	21	0	0	**6.6**	**6.8**
Small signal transistor	33	33	7	27	0	0	**5.7**	**7.7**
MOSFET	25	17	25	33	0	0	**7.6**	**8.7**
Power, bipolar	30	20	20	30	0	0	**6.8**	**7.4**
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	21	7	43	29	0	0	**8.1**	**9.0**
CMOS	11	32	46	11	0	0	**6.3**	**7.5**
TTL	35	18	41	6	0	0	**4.7**	**6.7**
LS	29	24	41	6	0	0	**4.9**	**7.1**
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	0	44	23	33	0	0	**8.2**	**7.5**
OP amplifier	8	15	46	31	0	0	**8.9**	**6.2**
Voltage regulator	19	31	25	25	0	0	**6.8**	**5.7**
MEMORY CIRCUITS								
DRAM 16K	0	20	0	80	0	0	**12.9**	**13.3**
DRAM 64K	0	13	0	87	0	0	**13.8**	**12.1**
DRAM 256K	0	8	0	54	23	15	**19.1**	**15.2**
DRAM 1M-bit	0	12	11	22	44	11	**19.2**	**17.9**
SRAM 4K × 4	0	17	17	33	33	0	**15.3**	**16.7**
SRAM 8K × 8	0	9	15	38	23	15	**17.8**	**18.6**
SRAM 2K × 8	0	13	0	74	13	0	**15.1**	**16.1**
ROM/PROM	0	14	0	86	0	0	**13.7**	**12.5**
EPROM 64K	8	25	17	50	0	0	**9.8**	**13.3**
EPROM 256K	0	15	15	62	8	0	**13.2**	**15.3**
EPROM 1M-bit	14	15	0	57	14	0	**12.8**	**18.5**
EEPROM 16K	0	17	17	66	0	0	**12.0**	**15.8**
EEPROM 64K	0	15	14	71	0	0	**12.5**	**16.9**
DISPLAYS								
Panel meters	0	20	50	20	0	10	**10.8**	**8.9**
Fluorescent	0	13	38	49	0	0	**11.0**	**11.1**
Incandescent	0	25	25	50	0	0	**10.4**	**5.3**
LED	14	43	22	21	0	0	**6.3**	**5.9**
Liquid crystal	10	10	40	40	0	0	**9.6**	**8.1**
MICROPROCESSOR ICs								
8-bit	0	50	20	30	0	0	**7.7**	**8.2**
16-bit	13	37	13	37	0	0	**7.8**	**9.4**
32-bit	0	22	33	33	12	0	**11.4**	**13.3**
FUNCTION PACKAGES								
Amplifier	0	25	37	38	0	0	**9.5**	**7.1**
Converter, analog to digital	0	18	55	27	0	0	**9.1**	**8.6**
Converter, digital to analog	0	25	37	38	0	0	**9.5**	**8.6**
LINE FILTERS	8	54	15	23	0	0	**6.3**	**6.6**
CAPACITORS								
Ceramic monolithic	24	29	29	18	0	0	**5.9**	**7.3**
Ceramic disc	18	29	29	24	0	0	**6.9**	**7.0**
Film	27	27	13	33	0	0	**6.9**	**6.5**
Aluminum electrolytic	19	25	19	37	0	0	**8.0**	**8.4**
Tantalum	17	22	27	28	6	0	**8.6**	**7.8**
INDUCTORS	8	30	31	31	0	0	**8.1**	**9.3**

Source: Electronics Purchasing Magazine's survey of buyers.

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CIRCLE NO 154

FLUKE

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A L L I A N C E   I N   T E S T   &   M E A S U R E M E N T

PHILIPS

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The most complete multifunction calibrator ever made.

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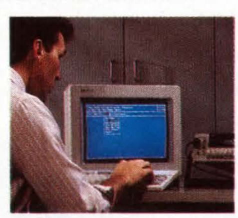
Simplified support with Artifact Calibration.

You might expect an instrument with the accuracy of the 5700A to be difficult to support. But it's not. You need only three Artifact Standards — a 10V direct voltage standard, and 1Ω and 10kΩ resistance standards — to calibrate all ranges and functions of the calibrator. Front panel messages prompt you through the process. And it all takes just over an hour, compared to the eight hours or more you'd expect for such a calibrator. Internal Check Standards and the Cal Check feature enhance your confidence in the 5700A's performance between calibrations. External verification may be extended to two years.

Covers your complete DMM workload.



The 5700A will calibrate virtually every DMM in your workload. It outputs direct voltage to 1100V. Alternating voltage from 220μV to 1100V (10 Hz to 1.2 MHz). Cardinal resistances from 1Ω to 100 MΩ in x1 and x1.9 decades, plus a short. And direct and alternating (10 Hz to 10 kHz) current to 2.2A. To calibrate higher current ranges or high ac voltages at high frequencies, select the companion 5725A Amplifier. To extend the 5700A's calibration workload coverage to RF voltmeters, order the Wideband Voltage option.

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FLUKE

PC-based logic analyzers

Logic analyzers that incorporate or depend on personal computers have added a new twist to selecting the most appropriate instrument for a specific application. No longer are performance and cost the only issues you must consider. Now, you need to factor in who will be using the analyzer, how often, and for what purpose.

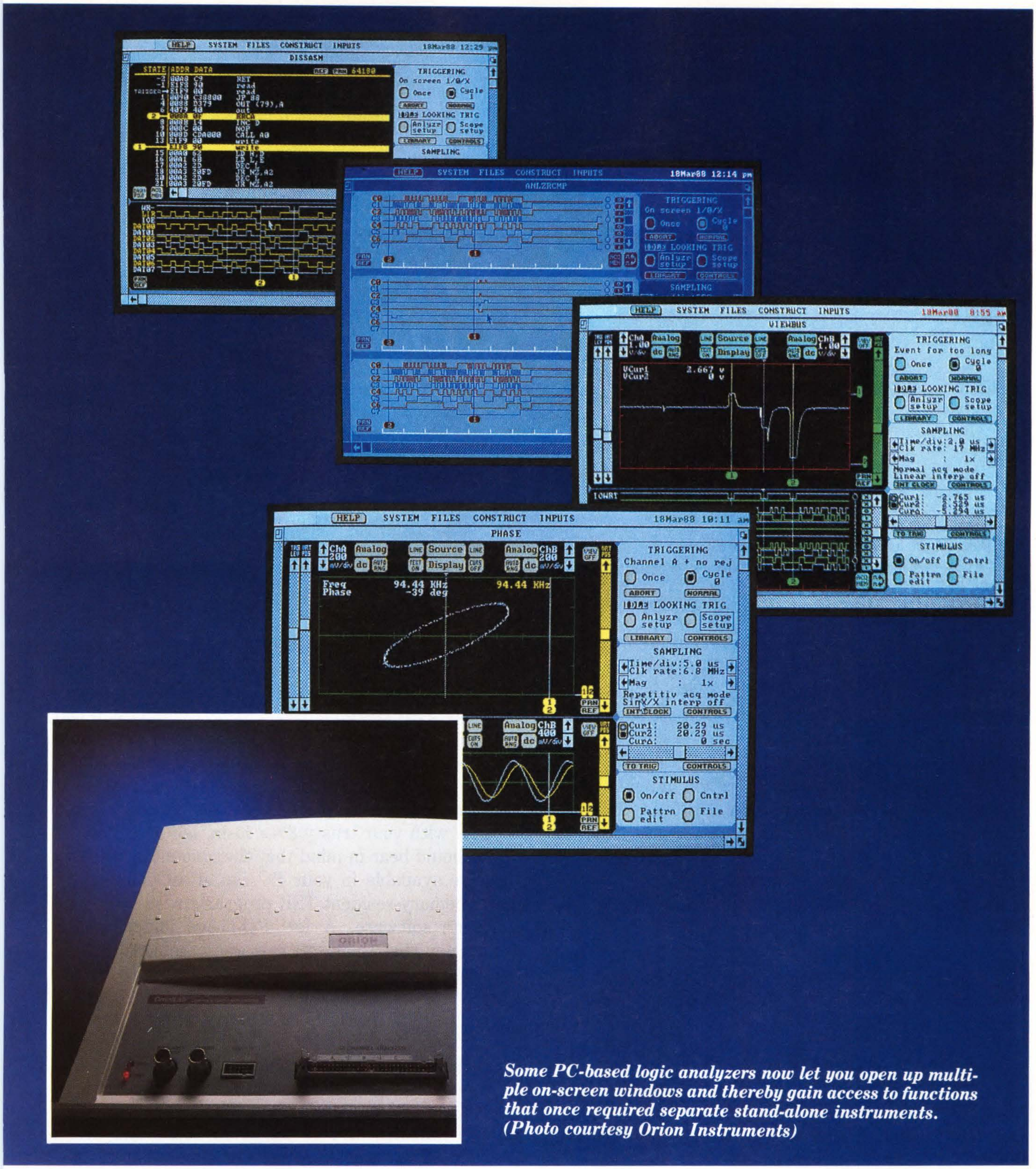
Dan Strassberg, *Associate Editor*

If the term "PC-based logic analyzer" conjures up an image of a low-cost instrument on a card, perhaps you aren't aware of the varied guises that a PC-based logic analyzer can assume. To be sure, many analyzers that can't function without a personal computer—or that incorporate a fully functional PC—are available as plug-in boards for less than $2000 (a figure that's only half the cost of low-end stand-alone units). But there's also a collection of expensive, specialized products with features you'd be hard pressed to find in non-PC-based instruments. The least expensive PC-based analyzers, BitWise Design's Logic-20/8 and Advanced Microcomputer Systems' PCLogic 108, sell for $495. At the other end of the spectrum, Gould's K450M, configured with an awe-inspiring 40M words of data memory on 64 channels (the equivalent of nearly ⅓G bytes of RAM), carries a price tag of $287,000.

Although there are plenty of suppliers of PC-based logic analyzers to choose from, you may be surprised by the logic-analyzer vendors that *don't* currently offer PC-based products. In this latter group, you'll find the industry's major players, Hewlett-Packard and Tektronix. You'll also find Arium Corp of Anaheim, CA, a company whose low-cost, stand-alone units have helped to transform logic analyzers from intimidating, infrequently used departmental resources to tools that many logic designers routinely employ. You should be aware, however, that Arium's most recent offering, the ML4400, albeit not designed to depend on a PC, can team up with a PC if you so desire.

They've put PCs *inside* logic analyzers

Stand-alone analyzers that incorporate PCs—like Fluke/Philips' PM 3655 and Kontron's PLA-286-02—may appear to offer the advantages of both worlds, but only you can evaluate how well their performance, features, and price meet the needs of your application. (Actually, PC-based logic analyzers trace their roots to antecedents of the Fluke/Philips and Kontron products. For a brief look at the history of PC-based analyzers, refer to the **box,** "PC-based logic analyzers: past and present," and for a glimpse of what may be in store, see the **box,** "Make way for Mac-based analyzers.")



Some PC-based logic analyzers now let you open up multiple on-screen windows and thereby gain access to functions that once required separate stand-alone instruments. (Photo courtesy Orion Instruments)

The PC's open architecture and the mix-and-match versatility it engenders provide a partial insight into the reasoning behind the development of PC-based logic analyzers—and other PC-based instruments. First of all, every logic analyzer includes a microprocessor and memory; every logic analyzer requires some sort of keyboard or panel controls; and every logic analyzer needs a display with alphanumeric and graphic capabilities. Because these items are part of a PC, they are "free" to designers of PC-based instruments.

A PC also includes a power supply, which may or may not prove adequate for powering a logic analyzer. And, it incorporates one or more disk drives that can be useful for storing and recalling data. In addition, most PCs' real-time clocks can, with appropriate software, record the time at which you acquire a block of data. For communication with other computers,

Bundling a logic analyzer on a PC bus card with a "luggable" PC, as Dolch does with its Cobra-PA480, creates a portable system with lots of expansion potential.

whether for postprocessing of files or for archival storage, personal computers have RS-232C ports and, optionally, IEEE-488 ports. All of these features are ones that users of logic analyzers often request.

Help is on the way

PCs don't just represent a collection of useful hardware. From a user's point of view, PC-based software also possesses often-sought-after ease-of-use features. Context-sensitive help, for instance, is a characteristic of much software that runs on PCs.

Because the earliest logic analyzers were anything but easy to use, they acquired—and have never really been able to shake off—a reputation for user hostility. Manufacturers of PC-based logic analyzers believe that built-in context-sensitive help screens are the key to helping infrequent logic-analyzer users quickly feel at ease. The vendors also believe that the PC-based analyzers' user friendliness, coupled with generally low prices, will create a mushrooming demand for the products. They envision increasing numbers of engineers losing their fear of logic analyzers and requisitioning units for their own lab benches.

Vendors of stand-alone units, on the other hand, assert that a PC isn't necessary to display context-sensitive help screens. They back up their contention with the fact that several stand-alone logic analyzers contain such help facilities in their firmware.

Software that was developed for purposes quite different from engineering has also played a role in the acceptance of PC-based instruments. PCs are, without a doubt, invaluable for writing reports, making calculations, and developing software. In system-debugging applications, your collection of notes documenting exactly what you did to achieve a specific result are also invaluable. With a PC-based logic analyzer, you can use many TSR (terminate-and-stay-resident) notepad programs to jot down test conditions and save them to disk—alongside the files that contain the actual data. You can make the TSR utilities pop up on screen at the press of a "hotkey" (ALT-F7, for example), and dispense with your trusty $8\frac{1}{2} \times 11$-in. lab notebook.

You should bear in mind that the amount of memory you have available in your PC can affect your ability to use memory-resident TSR programs with your logic analyzer's software. A few PC-based logic-analyzer vendors say that their software requires considerably less than the 640k bytes of RAM that MS-DOS normally supports (an amount that nearly all MS-DOS-based PCs now possess), but many require the full 640k bytes. Very little of the logic-analyzer software in **Table 1** can make use of memory beyond 640k bytes.

There are two standards that enable MS-DOS to support more than 640k bytes of RAM: the *extended*-memory schemes of PCs based on 80286 and 80386 μPs, and the *expanded*-memory schemes that all MS-DOS-based PCs can use. To use either of these standards, however, the memory must be present and the software must support it. The current standard that governs the design of expanded memory and the way that software accesses it is LIM EMS 4.0 (Lotus/Intel/Microsoft expanded memory specification version 4.0). The earlier standard that formed the basis for LIM EMS 4.0 was EEMS (enhanced expanded memory specification).

Of course, context-sensitive help screens and pop-up

The rationale behind some companies' decisions not to offer PC-based logic analyzers is significant—as is that of the companies that do offer them.

PC-based logic analyzers: past and present

The name "logic analyzer" is, of course, a misnomer. Like most instruments whose names contain the word "analyzer," a logic analyzer doesn't do the analysis—you do. The instrument provides you with the data you need in a form you can (you hope) interpret.

The idea of combining a personal computer and a logic analyzer really isn't new. In 1981, Kontron offered a logic analyzer combined with a personal computer that used the CP/M operating system. Today, however, as a class of product, PC-based logic analyzers are still probably only at the same stage of evolution as were PC-based analog data-acquisition systems two years ago. In the last two years, the PC-based architecture has begun to dominate data-acquisition technolgy. The jury is still out on whether something similar will occur with logic analyzers.

***A not-too-distant forebear** of Kontron's PLA-286-02 was the first PC-based logic analyzer. This unit runs under MS-DOS. Seven years ago, the operating system was CP/M.*

In fact, instrumentation vendors and users may even witness the coalescence of several trends into a new class of multifunction instrument that could cause single-function logic analyzers to disappear: It is the rule rather than the exception to use a logic analyzer in conjunction with other instruments. Often, an oscilloscope, a digital pattern generator, a voltmeter, and a frequency counter (and sometimes an analog waveform generator) sit on a lab bench beside the logic analyzer. Such a large collection of stand-alone, single-function instruments is both bulky and expensive.

To address this problem, many of the analyzers listed in **Table 1** of the accompanying article provide additional built-in or optional capabilities. Indeed, Orion Instruments has combined all of the often-needed, previously described instruments as well as an RLC (resistance/inductance/capacitance) meter with a 48-channel, 34-MHz-sampling logic analyzer. The $4800 Omnilab 9420A is expandable to 96 channels and can, in multiplexed mode, operate to 204 MHz. It measures just 15×11.5×5.4 in.

In theory, if you begin with many of the PC-based logic analyzers listed in **Table 1,** and add the right instrumentation cards, you should be able to devise your own multifunction instrument. However, in many cases, the software will force you to use the different functions one by one; it will deny you simultaneous access.

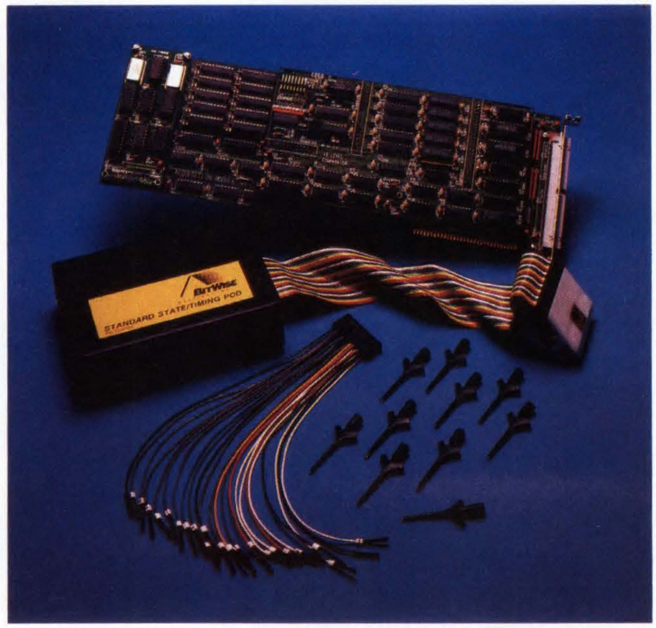
One of the beauties of the Omnilab is its user interface. The windowed display, developed completely by in-house programmers, allows simultaneous access to multiple functions. You can, for example, view dynamically changing analog waveforms in one window while the logic analyzer's state or timing displays appear in another.

Stand-alone analyzers that incorporate PCs appear to be ideal, but compare them against other analyzers to see if they are the best choice for you.

TSR notepad programs aren't the only kinds of software available to simplify the use of PC-based logic analyzers. Setting up a logic analyzer, for instance, especially for timing analysis, can be a rather painful experience. Connecting a large number of probes to the correct circuit nodes is a time-consuming, error-prone operation. Outlook Technology, whose T-100A timing analyzer is one of the specialized PC-based instruments listed in **Table 1,** recently introduced its Logic Probe software **(Ref 1)**. Using Logic Probe, you can obtain a lot of information about the probe setup at a glance. Logic Probe's goal is to reduce setup time and to minimize setup errors, particularly those you don't discover until you start to review your data—after you think you've completed data acquisition.

Unfortunately, one of the tools that helped to make PC-based analog data acquisition so popular is not yet available for PC-based logic analysis. Asyst Technologies' (Rochester, NY) Asyst and National Instruments' (Austin, TX) Lab Windows are examples of third-party software that controls the acquisition of data *and* processes it afterwards. To the best of this author's knowledge, there aren't any logic-analyzer vendors who offer software packages for postprocessing of logic-analyzer data that has been captured in disk files.

According to Hewlett-Packard, logic-analyzer users at this point in time simply aren't demanding prepackaged postprocessors. If users did want such software, they'd have a problem. Each logic-analyzer vendor uses a different file format for storing data on disk. Such a lack of standardization inhibits third-party software development, even though, if the demand were strong, vendors *would* respond.



Putting a 40-channel logic analyzer *on a single PC bus card is no small feat, as BitWise Designs' LAC shows. You can add RAM to capture 64k-word samples and add cards to achieve as many as 320 channels.*

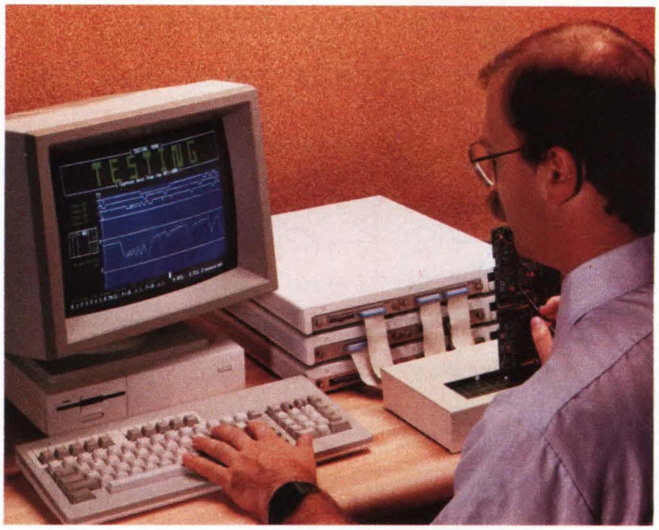
When deciding whether a PC-based logic analyzer is right for your application, you can't just think about the advantages that the software offers. Packaging can be very important to an instrument's usability. For example, if you're likely to use the analyzer for debugging physically large systems in a production test area, you should be concerned about size and portability.

Make way for Mac-based analyzers

Judging from the popularity of the Macintosh, you'd expect that there would be Macintosh-based logic-analysis products for sale. Inexplicably, such is not the case. Out of the more than 60 companies surveyed for this report, none was willing to talk for attribution about Mac-based logic analyzers. But early in 1989, the situation should change.

There are two obvious ways to build a logic analyzer based on a Mac. One approach would be to package the analyzer in an external box that talks to any Macintosh via its RS-422 port. The other approach—placing the analyzer or a proprietary analyzer interface on a Nubus I/O card—would work only with the Macintosh II and any slotted Macs introduced in the future.

Because the Macintosh line is popular with many users of low-end electronic CAE, there appears to be a ready-made market among these individuals for Macintosh-based logic-debugging tools. If this hypothesis is correct, a year from now Macintosh-based logic analyzers will be starting to proliferate. Nevertheless, you probably still won't find as many Macintosh-based logic analyzers as ones based on IBM PC- and PS/2-compatible machines.



A PC allows the addition of artificial intelligence *to a logic analyzer. Array Analysis' Expertest 1000 "learns" how to diagnose faults in boards.*

Even though most logic analyzers—stand-alone or PC-based—use pods that connect to the instrument via a ribbon cable, you can think of a stand-alone logic analyzer as consisting of a self-contained portable unit. When housed in a conventional desktop PC, even logic analyzers residing on a single PC bus card aren't portable.

You can put a logic analyzer in your PC

You may, however, be able to house such card-level instruments in a sewing-machine-size "luggable" PC having an LCD or an electroluminescent display. You need to check with the logic-analyzer vendor to make sure that you can procure software driver modules for the type of display you want to use. Most flat-panel displays of this type have resolutions different from those of the standards to which MS-DOS-based PCs conform when driving CRT displays.

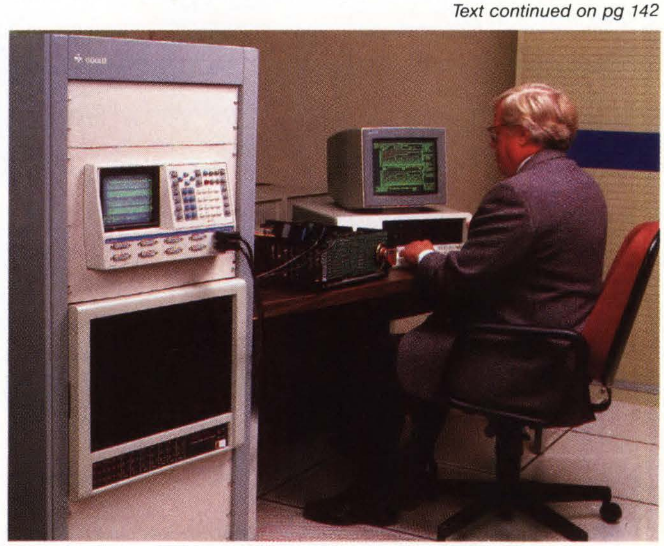
If you buy the logic analyzer and the portable PC as a single package, you should be able to forget about such potential incompatibilities. Dolch American's Cobra-PA480 and BitWise Design's System-40 are good examples.

Fluke/Philips, with its PM 3655, and Kontron, with its PLA-286-02, take a somewhat different tack in resolving PC-based logic-analyzer packaging issues. Instead of designing their logic analyzers to mount in existing PCs, Kontron and Philips designed fully functional, MS-DOS-based PCs with expansion slots to spare around their logic analyzers. (In the world of MS-DOS, a fully functional PC is one that can run a specific ensemble of programs, thus verifying the compatibility of the hardware with commonly used software.) With this approach, Kontron and Philips have more room for the logic-analyzer circuitry. They can size the power supply and the enclosure's cooling to accommodate the logic analyzer rather than designing the logic analyzer to work with the PC's power supplies and fans. And, they can more easily shield the analyzer against the rather hostile, noisy environment within a PC.

If your department decides to opt for a single-unit logic-analyzer-cum-PC and use it not only for logic analysis but also for conventional PC tasks (word processing or manipulating spreadsheets, for example), the problem of contending for use of the instrument will surface. The issue of who gets to use the shared resource is not confined to PC-based logic analyzers packaged as single units, though. Unless a PC-based logic analyzer is housed in an enclosure separate from the PC's and is connected to the computer through a standard port (such as an RS-232C port), or unless you're willing to disassemble the PC to liberate a single-card logic analyzer or a proprietary logic-analyzer interface card buried inside, you won't be able to use the analyzer while someone else is using the PC. And even if you can free up the analyzer, you'll need to connect it to *another* PC to make it work. **Table 1** indicates how each logic analyzer interfaces to its host PC.

Although perceptions may be changing, several vendors have expressed the opinion that many of their

Text continued on pg 142



PC-based logic analyzers *such as Gould's K450M can accommodate 40M 64-bit words of RAM.*

TABLE 1—REPRESENTATIVE PC-BASED LOGIC ANALYZERS

COMPANY	MODEL	BASE PRICE (US)	INCLUDES COMPUTER?	BASE CHANNELS	MAX CHANNELS	MAX PRICE (US)	OPTIONAL PODS	TRIGGER LEVELS	CPU[1]	CAN USE RAM PAST 640k BYTES?	TYPE OF INTERFACE (ANALYZER TO CPU)	GRAPHICS SUPPORTED[2]	SUPPORTED DISK FORMATS (BYTES)	HARD DISK REQUIRED?
ARRAY ANALYSIS	EXPERTEST 1000	$6725	NO	32	192	$14,155	NONE	14	8 MHz	NO	IEEE-488, RS-232C	EGA, HGC	360, 720k	NO
BITWISE DESIGNS	LOGIC-20/8	$495	NO	8	8	$495	20-MHz DSO, $395	1	512k BYTES	NO	PC BUS	CGA, EGA, HGC	360, 720k, 1.2 1.44M	NO
	LOGIC-20	$1295	NO	16	32	$2190	8-CHANNEL/ 40-MHz, $225; 20-MHz DSO, $395; 25-MHz DSO, $450; DISASSEMBLY, $395	1	512k BYTES	NO	PC BUS 16 CHANNELS: 1 SLOT; 32 CHANNELS: 2 SLOT	SAME AS ABOVE	SAME AS ABOVE	NO
	LOGIC-100	$1745	NO	16	32	$2895	4-CHANNEL/ 100 MHz IS STANDARD	1	512k BYTES	NO	SAME AS ABOVE	SAME AS ABOVE	SAME AS ABOVE	NO
	LAC	$2400	NO	40	320	$67,200	1-GHz EQUIVALENT-TIME SAMPLING, $1800	SEE TEXT		YES PER EMS 4.0 (SEE TEXT)	PC BUS	CGA, EGA, HGC, VGA	SAME AS ABOVE	SUGGESTED
	SYSTEM-40	$2995	YES	40	120	$7800	THE SYSTEM 40 IS THE MODEL LAC PACKAGED IN A SEWING-MACHINE-SIZE PORTABLE COMPUTER WITH							
DOLCH AMERICAN	COBRA-PA480	$3940	YES	48	48	$3490	8- OR 16-BIT DISASSEMBLY, $495; GENERAL PURPOSE	16	8 MHz	YES	PC BUS	CGA, EGA	1.2M	NO
EL TORO SYSTEMS	PC-29	$749	NO	24	24	$749	NONE	1	320k BYTES	NO	PC BUS	MDA, CGA, EGA	360, 720k, 1.2M	NO
	PC-52	$1299	NO	24	24	$1299	NONE	1	320k BYTES	NO	PC BUS	SAME AS ABOVE	SAME AS ABOVE	NO
	PC-27100	$1599	NO	24	96 4 BOARDS IN 1 PC	$6396	NONE	16	320k BYTES	NO	PC BUS	SAME AS ABOVE	SAME AS ABOVE	NO
JOHN FLUKE MFG/PHILIPS	PM 3655	$4500	YES	24	96	$9500	DISASSEMBLY PODS: 8-BIT, $1000; 16-BIT, $2000	4	4.7/8 MHz; 256k BYTES	NO	PC IS WITHIN ANALYZER	HGC	360k	NO
GOULD	K450M	$104,000	YES	32	64	$287,000	NONE	14	10 MHz	NO	CUSTOM	EGA	1.2M	130M-BYTE INCLUDED
HEATH/ ZENITH	ST-4800	$2850	NO	16	32	$3800	NONE	1	360k BYTES	NO	PC BUS	CGA	360k	NO
HILELVEL	DT3700	$9475	NO	16	256	$89,500	N/S	16		NO	IEEE-488, RS-232C, PARALLEL	CGA, EGA	360k	NO
KONTRON	PLA-286-02	$9900	YES	48	112	$15,500	HIGH IMPEDANCE, TTL	14	10-MHz, ZERO-WAIT '286	NOT FOR LOGIC ANALYSIS	PC/AT BUS	HGC	720k	NO
	KSA-64	$14,495	NO	64	64	$17,495	N/S	14		NO	KONTRON KPI, $1000	N/S	360k, 1.44M	YES, 10M-BYTE
LINK COMPUTER	LA 27100	$1299	NO	24	72	$3597	N/S	16	384k BYTES	NO	PC BUS	MDA, CGA, EGA, HGC	360k OTHERS ON REQUEST	NO
	LA 27200	$1899	NO	24	72	$5247	N/S	16	384k BYTES	NO	PC BUS	SAME AS ABOVE	SAME AS ABOVE	NO
METRABYTE CORP	PCIB-DLA	$1295	NO	16			8-CHANNEL/ 40-MHz, $225	1	512k BYTES	NO	PC BUS	CGA, EGA, HGC	360, 720k, 1.2, 1.44M	NO
MICROCASE[6]	LAW-8IU	$6450	NO	48: 16 TIMING; 32 STATE	96	$9370	µP-SPECIFIC, $495 TO $2865	15		NO	MICROCASE PARALLEL INTERFACE INCLUDED	CGA	360k	NO
	THE LAW-16IU (BASE PRICE $7985) IS SIMILAR TO THE LAW-8IU EXCEPT THAT THE BASE CONFIGURATION INCLUDES 48 STATE-ANALYSIS CHANNELS. THE LAW-32IU													
NCI	PA480	$1595	NO	48	96	$4310	GENERAL AND µP-SPECIFIC, $450 TO $795	16		N/S	PC BUS	CGA, EGA, HGC	360k	NO
OMNILOGIC INC	2020C	$1995	NO	16	32	$2845	TTL/CMOS, $275; VARIABLE, $375; RELAY-LOGIC, $375	7		NO	RS-232C	CGA, EGA, HGC	360k, 1.2M	NO
	4000B	$1995	NO	32	64	$3450	SAME AS ABOVE			NO	PC BUS	CGA, EGA	SAME AS ABOVE	NO
ORION	9210A	$4800	NO	48	96	$8200	VARIABLE 8-CHANNEL, $190	4	'286 SUGGESTED	YES, EMS, EEMS	PC BUS	EGA, HGC	1.2M	SUGGESTED
	9420A	$8900	NO	48	96	$12,300	SAME AS ABOVE	4	SAME AS ABOVE	SAME AS ABOVE	PC BUS	SAME AS ABOVE	1.2M	SAME
OUTLOOK TECHNOLOGY	T-100A	$32,500	NO	16	32	$34,700	FIXED- AND VARIABLE-LEVEL PATTERN GENERATOR	3 TO 500 MHz	'286 BASED	N/S	PC/AT BUS, IEEE-488	EGA	360k, 1.2M	YES, 20M-BYTE
RAPID SYSTEMS	R3000	$2195	NO	16	32	$4495	CMOS, $275; TTL, $275; PATTERN GENERATOR, $995	N/S		N/S	RS-232C	CGA	360k	NO
	R3200	$1995	NO	24	24	$1995	NONE	4	256k BYTES	N/S	PC BUS	MDA, CGA, EGA	360k	NO
	R3400	$1995	NO	32 STATE; 8 TIMING	32 STATE; 8 TIMING	$1995	NONE	16		NO	PC BUS	CGA, HGC, EGA, VGA, MCGA	360, 720k, 1.2, 1.44M	NO
STEP ENGINEERING	STEP-40	$25,000	NO	32	512	$60,000	N/S	16	'286 BASED	YES, NEEDS 1.5-BYTE EMS	PARALLEL INTERFACE INCLUDED	MDA, CGA, EGA	360k, 1.2M	YES, 20-BYTE
	STEP-50	$14,000	NO	80	80	$14,000	N/S	4	SAME AS ABOVE	SAME AS ABOVE	SAME AS ABOVE	CGA, EGA	SAME AS ABOVE	SAME AS ABOVE

KEY: N/A = NOT APPLICABLE; N/S = NOT SPECIFIED

NOTES: 1. MAJOR ATTRIBUTES OF THE COMPUTER SUPPLIED, IF APPLICABLE, OR THOSE OF THE MINIMUM-ACCEPTABLE COMPUTER, IF THE ANALYZER VENDOR DOES NOT SUPPLY THE COMPUTER. UNLESS NOTED, ALL UNITS WILL FUNCTION WITH AN 8088-BASED CPU OPERATING AT 4.77 MHz AND POSSESSING 640k BYTES OF RAM. IF THE COMPUTER HAS NO HARD DISK, IT SHOULD HAVE TWO FLOPPY-DISK DRIVES.

2. MDA = MONOCHROME DISPLAY ADAPTER; CGA = COLOR GRAPHICS ADAPTER; EGA = ENHANCED GRAPHICS ADAPTER (COLOR); VGA = VIDEO GRAPHICS ARRAY (COLOR); HGC = HERCULES GRAPHICS CARD (MONOCHROME); MCGA = MULTICOLOR GRAPHICS ARRAY.

MAX SAMPLE RATE[3] (MHz)	MAX POSSIBLE SAMPLE RATE (MHz)/ CHANNELS	THRESHOLD COMPATIBILITY AND VARIABLE RANGE (V)	TRANSITIONAL TIMING?	MEMORY DEPTH (WORDS) BASE	MEMORY DEPTH (WORDS) MAX	CHANNELS USABLE WITH MAX MEMORY	MAX TIMING SKEW (nSEC)	GLITCH CAPTURE MIN WIDTH CAPTURED (nSEC)	GLITCH CAPTURE REDUCES CHANNELS USABLE?	GLITCH CAPTURE REDUCES MEMORY DEPTH?	DIMENSIONS (IN.)[4]	ADDITIONAL FUNCTIONS PERFORMED	NO. OF µPs VENDOR SUPPORT WITH DISASSEMBLERS
50 (25 WITH 192 CHANNELS	200/192[5]	TTL, ECL, -3 TO 3	NO	1k	2k	96	1	3	YES	NO	1.5×14.2× 16.6	SCOPE; PATTERN AND WAVEFORM GENERATOR.	24 PLUS 3 BUSES
20	20/8	TTL, CMOS	NO	255	255	8	1	50	NO	NO	3×4×0.75	SCOPE (WITH ANALOG POD).	NONE
20	40/8 WITH 40-MHz POD	SAME AS ABOVE	NO	256	512 WITH 40-MHz POD	8	1	25 WITH 40-MHz POD	NO	NO	3×5×0.75	32k-WORD MEMORY DEPTH FOR LOW-SPEED ACQUISITION.	6 FAMILIES
25	100/4	SAME AS ABOVE	NO	256	1024	4	1	10	NO	NO	SAME AS ABOVE	SAME AS ABOVE.	SAME AS ABOVE
25 WITH 40 CHANNELS; 20 WITH 320 CHANNELS	125/8	SAME AS ABOVE	YES	4k	64k	8 WITH 320k WORDS	2	8	NO	NO	5×6×1	TIME STAMPING; MORE FUNCTIONS DESCRIBED IN TEXT.	N/S
DUAL FLOPPY-DISK DRIVES. PRICES INDICATED ARE FOR SYSTEMS WITH 4k WORDS OF ANALYZER MEMORY. DESKTOP VERSIONS AND UNITS WITH DEEPER MEMORY ARE AVAILABLE.													
25	100/12	-5 TO 5	NO	4k	16k	12	2	5	NO	NO	N/S	SCOPE; PATTERN AND WAVEFORM GENERATOR; LINE MONITOR.	AT LEAST 7
50	50/24	TTL	NO	1k	1k	24	2	N/A	N/A	N/A	3 PODS: 3×4	NONE	NONE
25	100/6	-6 TO 10	NO	1k	4k	6	2	N/A	N/A	N/A	4×5	NONE	NONE
50	100/6	-10 TO 13	NO	4k	16k	6	2	N/A	N/A	N/A	3 PODS: 3×4	NONE	NONE
100	100/96	TTL, ECL, -6.3 TO 6.3	NO	2k	2k	96	3	5	NO	NO	CABLE TO POD DISTANCE IS >4 FT	IEEE-488, RS-232C PORTS ARE INCLUDED; TWO HALF LENGTH AND TWO FULL-LENGTH PC BUS SLOTS.	10 N/S
100	200/32	-9.9 TO 9.9	NO	2.5M	40M	64	1	5	NO	NO	5-FT-HIGH RACK	NONE	NONE
50	50/32	TTL	NO	4k	4k	32	N/S	N/A	N/A	N/A	6.5×2.25× 9.7	NONE	NONE
STATE ONLY	STATE ONLY	TTL, ECL, -3.5 TO 6.4	N/A	4k	16k	256	1	N/A	N/A	N/A	7×23×18	PERFORMANCE ANALYZER; PATTERN-GENERATOR INTERFACE.	USER-DEFINABLE DISASSEMBLY
20	200/8	TTL, ECL, -5.0 TO 12.5, HIGH-IMPEDANCE	NO	4k STATE; 8k TIMING	SAME AS BASE	96 STATE; 16 TIMING	4	5	NO	NO	APPROXIMATELY 1×2×0.5	PATTERN GENERATOR.	14
50	100/32	-12.7 TO 12.7	YES	2k	16k	32	2	5	YES, ×1/2	YES, ×10	17.3×19.3× 7	SOFTWARE-PERFORMANCE SERIAL DATA ANALYZER	29 PLUS 1 BUS
50	100/6	TTL, ECL, -8 TO 14	YES	4k	16k	18	2	N/A	N/A	N/A	3 PODS: 3×4.25× 0.75; 32 IN. CABLE	N/S	N/S
50	200/6	SAME AS ABOVE	YES	4k	16k	18	2	N/A	N/A	N/A	SAME AS ABOVE	N/S	N/S
20	40/8 WITH 40-MHz POD	TTL, CMOS	NO	256	512 WITH 40-MHz POD	8	1	25 WITH 40-MHz POD	NO	NO	3×5×0.75	32k-WORD MEMORY DEPTH FOR LOW-SPEED ACQUISITION.	6 FAMILIES
100 TIMING; 10 STATE	100/16	TTL, ECL, -5.5 TO 5.5	YES	508 TIMING 4k STATE		80 STATE; 16 TIMING	5	5	NO	NO	13×7.5×15	PATTERN GENERATOR.	29
(BASE PRICE $9370) INCLUDES 80 STATE-ANALYSIS CHANNELS IN ITS BASE CONFIGURATION.													
25	100/12	TTL, -5 TO 5	NO	4k	16k	12	2	5	YES	NO	3.5×7.5	DIGITAL STORAGE SCOPE.	14
20	20/16	TTL, 0 TO 15	NO	1k	1k	16	±1 INTERVAL	10	NO	NO	6×8×14	SIGNATURE ANALYZER; 20-MHz PATTERN GENERATOR OPTIONAL.	N/S
25	100/16	SAME AS ABOVE	NO	8k	8k	16	SAME	N/A	N/A	N/A	2.5×16×15	PATTERN GENERATOR.	N/S
34	204/8	TTL, -3 TO 3	YES	4k	96k	8	1.5	5	YES, BY 1 CHANNEL	NO	15×11.5× 5.4	FREQUENCY COUNTER; RLC METER; WORD GENERATOR	OVER 150
34	204/8	SAME AS ABOVE	YES	4k	96k	8	1.5	5	SAME	NO	SAME AS ABOVE	SAME AS ABOVE PLUS DIGITAL SCOPE AND FUNCTION GENERATOR.	SAME
500	2000/4	TTL, ECL, -10 TO 10 IN 10-mV STEPS	YES	4k	32k	4	0.1	1.5	SEE NOTE 7	NO	7×16.75× 25	250-MHz PATTERN GENERATOR; SETUP-AND-HOLD VIOLATION DETECTOR; 16-GHz SYNCHRONOUS HARMONIC SAMPLING	NONE—TIMING ANALYZER ONLY
20		TTL, CMOS	NO	1k	1k	32	35	10	NO	NO	8×8×18	PATTERN GENERATOR.	NONE
25	100/8	TTL, ECL, -10 TO 10	NO	2044	8176	8	10	N/A	N/A	N/A	6×8×3		N/S
25	100/8	TTL	NO	2047	8116	8	2	6	SEE NOTE 8	NO	11×6, PLUS 6 PODS: 4×2		10
SYNCHRONOUS ONLY — STATE ANALYZER	512/25	TTL	NO	4k	16k	512		N/S	N/S	N/S	15×22×9	PERFORMANCE ANALYZER; ROM/PROM EMULATION; BIT-SLICE SUPPORT; CLOCK CONTROL.	USER-DEFINED DISASSEMBLY (SEE TEXT)
SAME AS ABOVE	80/20	TTL	NO	4k	4k	80		N/S	N/S	N/S	19×25×5	SAME AS ABOVE EXCEPT FOR CLOCK CONTROL.	SAME AS ABOVE

3. WITHOUT REDUCING NUMBER OF USABLE CHANNELS.
4. PORTION EXTERNAL TO COMPUTER.
5. USING EQUIVALENT-TIME SAMPLING.
6. FORMERLY NORTHWEST INSTRUMENT SYSTEMS, INC.
7. THERE ARE TWO GLITCH-CAPTURE MODES: "GLITCH-ONLY" REDUCES CHANNELS BY 1/2; "GLITCH + DATA" DOES NOT REDUCE CHANNELS.
8. ANALYZER SUPPORTS GLITCH DETECTION ON FOUR CHANNELS WHILE SAMPLING EIGHT CHANNELS.

The open architecture and "mix-and-match" versatility of the PC provide only a partial insight into the reasoning behind the development of PC-based logic analyzers.

***It's possible to design a PC** around a logic analyzer, as Philips has done with the PM 3655—sold in the US by John Fluke Mfg Co.*

customers view logic analyzers as insurance. If you regard a logic-analyzer purchase as a type of insurance policy, you should buy as much capability as you can afford, regardless of what you think you need right now: Beware of foregoing insurance that you may well need for future perils. If you consider the spectrum of instruments that qualify as PC-based logic analyzers, you can probably find one that meets your performance requirements, no matter how demanding they are, without going over your department's budget.

Nonetheless, when evaluating logic-analyzer specifications, you should understand the techniques that marketers employ to make their products look good on paper. This caveat applies to all logic analyzers—not just PC-based ones.

For example, data sheets generally list a maximum acquisition speed and a channel capacity. Be sure to find out how many channels you can use when you are acquiring data at the maximum rate. To sample data at speeds higher than their normal maximum, many analyzers multiplex channels. Invoking an analyzer's multiplexed mode reduces its channel capacity. (By the way, most logic-analyzer vendors express their instruments' sampling rates in MHz. Technically, MHz is the wrong unit, and Megasamples/sec is correct. A logic-analyzer sampling-rate spec expressed in MHz isn't likely to cause confusion, however. This is in contrast to digital-oscilloscope specs, where both sampling rate—translated into Megasamples/sec—and analog bandwidth—correctly expressed in MHz—are pertinent.)

If you want glitch-capture capability

Logic analyzers are sampled-data systems, and therefore they will miss events that occur between the instants when they sample. Glitch capture enables an analyzer to recognize spikes of a specified minimum width regardless of the sampling speed. If you're in the market for a logic analyzer with glitch-capture capability, find out if you can use all the channels or all the memory when using that feature. The use of glitch capture may force you to sacrifice channels or memory depth. Moreover, the way the analyzer displays the presence of a glitch can be misleading **(Ref 2)**.

When it comes to evaluating the sampling rate, take note of the instrument's specs in *both* state- and timing-analysis modes. Very often, you'll find that, when an analyzer is performing state analysis, it can only ac-

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Circle 17 for literature only

Circle 18 for demonstration

Vendors believe that the PC-based analyzers' user friendliness, coupled with generally low prices, will create a mushrooming demand for the products.

An external cabinet *housing Microcase's Logic-Analysis Workstation (LAW) Series connects to the PC bus through a proprietary parallel interface.*

quire data at a small fraction of its maximum rate. This limitation doesn't apply to all logic analyzers, however; you'll find both low-cost and high-performance units that sample just as rapidly in the state mode as in the timing mode.

In addition to reading between the lines of an analyzer's data sheet, you'll also need to evaluate your need for specialized techniques and extra-cost options. Transitional timing, for instance, is a technique that some analyzers use to increase their effective memory depth without increasing the amount of memory they use. Instead of storing the logic state of each channel at each sampling point, an analyzer that employs transitional timing identifies and stores only those samples of a signal where a state change occurs. Not only does transitional timing reduce the amount of memory an analyzer requires to store samples of a given depth, it also reduces the size of the disk files that store the captured data.

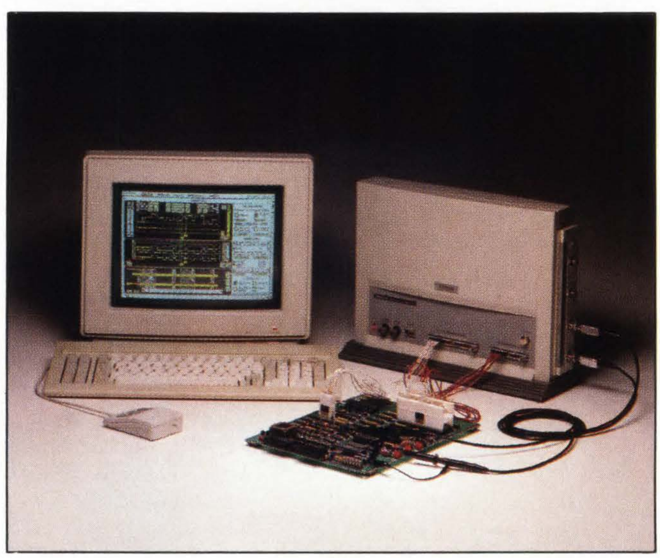
You'll uncover many analyzers that can recognize words and trigger-on complex word sequences. Some analyzers can also filter data—that is they can avoid storing data that is of no interest. This ability, in effect, increases an analyzer's memory. It also allows the analyzer to display only relevant data and thus simplifies the interpretation of the displayed information (especially in the state-analysis mode). The number of trigger levels listed in **Table 1** is, for all intents and purposes, the number of states that the trigger-control state machine can assume.

Some analyzers—BitWise Designs' LAC and System-40, for example—use a RAM-based state machine rather than one based on a counter. At any state, a counter-based state machine can only hold its current state, move to the next state, or reset. A RAM-based state machine, on the other hand, can hold its state

TABLE 2—NUMBER OF STATE-ANALYSIS CHANNELS (WORD WIDTH)

PROCESSOR	FOR DISASSEMBLY	ADDITIONAL	RECOMMENDED
INTEL			
8085	19	7	26
8086	22	11	33
8088	22	11	33
80186	26	22	48
80286	42	9	51
80386	73	12	85
MOTOROLA			
6800	25	6	31
6809	26	5	31
68000	51	2	53
68010	51	2	53
68020	76	6	82
68030	78	21	99
ZILOG			
Z80	26	5	31
Z8001	28	11	39

(COURTESY OF JOHN FLUKE MFG CO AND PHILIPS TEST AND MEASUREMENT)



This briefcase-size unit *may provide a glimpse of PC-based logic analyzers' future. Orion's Omnilab 9420A contains, besides the analyzer, a scope, an RLC meter, a pattern generator, and an arbitrary-waveform generator.*

Because the earliest logic analyzers were difficult to use, the instruments acquired—and have never really shaken off—a reputation for user hostility.

or branch to any other state. Vendors of analyzers that contain RAM-based triggering logic claim that their trigger schemes offer greater flexibility than do those that do not.

Many vendors provide pods that simplify the chore of interfacing their logic analyzers to specific microprocessors. These pods are almost always extra-cost options, and the cost can be significant. Sometimes the pods perform rather sophisticated functions—for example, flushing pipelined instructions that fail to execute or demultiplexing address and data onto separate signal lines—capabilities that come in especially handy for state analysis. Most vendors bundle disassemblers with the pods; you'll find that the disassemblers' capa-

Manufacturers of PC-based logic analyzers

For more information on PC-based logic analyzers such as those described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Advanced Microcomputer Systems
1321 NW 65th Pl
Fort Lauderdale, FL 33309
(305) 975-9515
FAX 305-975-9698
Circle No 650

Array Analysis Inc
200 Langmuir Lab
Brown Rd
Ithaca, NY 14850
(607) 257-6800
FAX 607-257-2445
Circle No 651

BitWise Designs Inc
297 River St, Suite 501
Troy, NY 12180
(518) 274-0755
TWX 710-110-1708
Circle No 652

Dolch Logic Instruments
2029 O'Toole Ave
San Jose, CA 95131
(408) 435-1881
TWX 910-338-2023
Circle No 653

El Toro Systems
23702-B Birtcher Dr
El Toro, CA 92630
(714) 770-1474
TWX 910-240-7216
Circle No 654

Gould Design and Test Div
19050 Pruneridge Ave
Cupertino, CA 95014
(408) 988-6800
FAX 408-988-1647
Circle No 655

Heath/Zenith Electronics Inc
Hilltop Rd
St Joseph, MI 49085
(616) 982-3721
Circle No 656

Hilevel Technology Inc
31 Technology Dr
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TLX 655316
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Kontron Electronics
630 Clyde Ave
Mountain View, CA 94039
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TWX 910-378-5207
Circle No 658

Link Computer Graphics Inc
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Livingston, NJ 07039
(201) 994-6669
TWX 910-240-9305
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MetraByte Corp
440 Myles Standish Blvd
Taunton, MA 02780
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TLX 503989
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MicroCase Inc
(formerly Northwest Instruments)
Box 1309
Beaverton, OR 97075
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NCI
Box 11025
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FAX 205-837-5221
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Nobel Systems
Box 13083
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Circle No 663

OmniLogic Inc
350 Sunset Blvd N
Renton, WA 98055
(206) 271-2000
Circle No 664

Orion Instruments
702 Marshall St
Redwood City, CA 94063
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Outlook Technology
200 E Hacienda Ave
Campbell, CA 95008
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TLX 350479
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Philips Test & Measuring Instruments
Bldg HKF
5600MD, Eindoven
The Netherlands
Phone local office
Circle No 667
In the US:
John Fluke Mfg Co Inc
Box C9090, MS 250C
Everett, WA 98206
(800) 443-5853
TLX 185102
Circle No 668

Rapid Systems Inc
433 N 34th St
Seattle, WA 98103
(206) 547-8311
TLX 205017
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bilities vary widely. When you evaluate logic analyzers, you obviously need to know whether an instrument has (or can expand to contain) enough channels to handle the processors you are using or are likely to use. **Table 2** contains a partial listing of processors and the number of channels that they require. In addition, you must find out if the vendor can furnish pods and disassemblers for the processors you have in mind; or, if not, if there's a configurable disassembler that you can customize for your needs.

Until the day arrives when logic designs produced on CAE workstations perform flawlessly the first time you build them (and every subsequent time), debugging tools will be an important part of a digital design engineer's arsenal. Although a logic analyzer often won't get you to the bottom of a problem without the help of additional instruments, it's a very important tool. A PC-based logic analyzer may or may not be the best solution for you, but if performance, versatility, and economy are what you're looking for, you owe it to yourself and your company to take a close look at PC-based analyzers. **EDN**

References

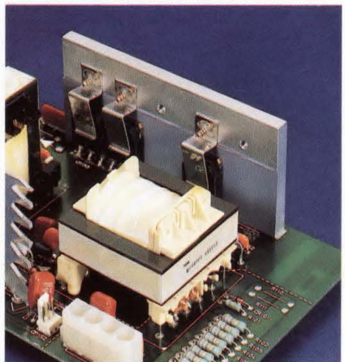
1. Strassberg, D, "Software tool for logic timing analyzer eliminates setup confusion," *EDN*, June 9, 1988, pg 88.
2. Schweitzer, W, "Proper glitch capture requires knowledge of logic-analyzer limits," *EDN*, January 7, 1988, pg 157.
3. *The ABCs of Logic Analysis*, John Fluke Mfg Co Inc, Everett, WA, and Philips Test and Measurement, Eindoven, The Netherlands, 1988.

Article Interest Quotient (Circle One)
High 497 Medium 498 Low 499

How to shrink a high power switcher and be SELV*

* "SELV" stands for "**S**afety **E**xtra **L**ow **V**oltage".
To qualify, a power supply has to meet strict VDE/IEC standards.
(The 48V models are, of course, not SELV)

Start by using FETs that switch at 150 KHz.



Then use your own advanced ferrite, TDK-H7C4, in your power transformer. This is a material that can handle 150 KHz with very little loss. Then you can take advantage of the higher frequency, and make your power transformer smaller and lighter and still meet the SELV requirements of VDE 0806. The power transformer in our new 300-Watt RAX 5-60K is just 1.63″H x 1.84″W x 1.75″D.

Use a low noise d-c fan to keep things cool.

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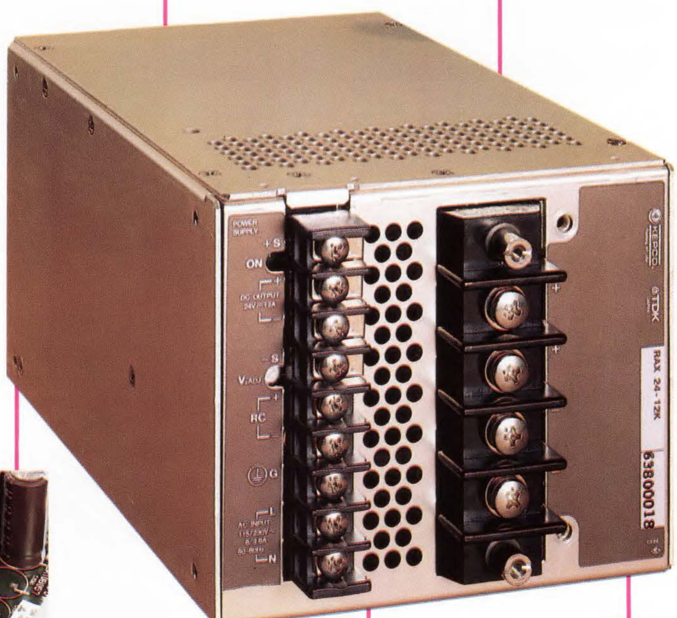
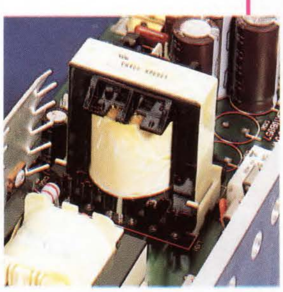
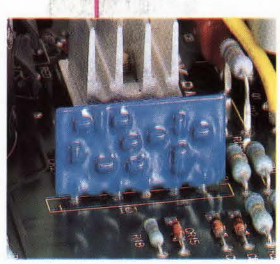


Shown:
300-Watt Model RAX 24-12K (24V/12A), supplied fully enclosed for industrial applications.



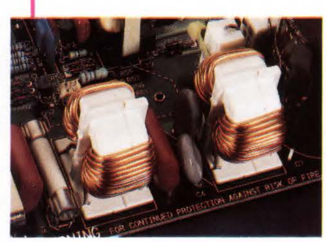
Your forward converter choke will also be smaller with advanced materials.

For example, the 1500 Watt switcher uses a new amorphous-core output choke.



Save a lot of space with your own custom-made hybrid microcircuits,

employing advanced surface mount technology. These hybrids also add to reliability by cutting parts population.



If you *also* want to meet the strict conducted EMI limits of FCC Class A and the leakage current of VDE 0806, install a dual-choke input EMI filter (which also uses the new advanced ferrite).

NEW

KEPCO/TDK INDUSTRIAL GRADE 150KHz FET-BASED SWITCHING POWER SUPPLIES, SERIES RAX

146-1616

NEW KEPCO/TDK INDUSTRIAL GRADE 150KHz FET-BASED SWITCHING POWER SUPPLIES

SERIES RAX

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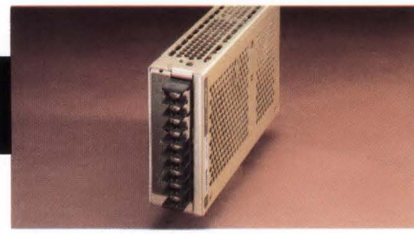
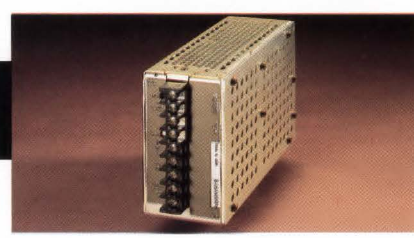


50 WATT MODELS

Model Number		RAX 5-10K	RAX 12-4.2K	RAX 15-3.4K	RAX 24-2.1K	RAX 48-1K
Output Volts		5V	12V	15V	24V	48V
Adjustment Range		4.0~5.5	8.4~13.2	12.0~16.5	16.8~26.4	32.6~52.8
Max. Output Ratings Amps/Watts	50°C	10.0/50	4.2/50	3.4/50	2.1/50	1.0/50
	60°C	7.0/35	2.9/35	2.4/35	1.5/35	0.7/35
	71°C	4.0/20	1.7/20	1.4/20	0.8/20	0.4/20
Current Limit (Amps)		10.5~11.0	4.5~4.8	3.6~3.9	2.3~2.5	1.1~1.3
OVP Setting (Volts)		6.0~6.9	13.7~15.7	17.0~19.5	27.0~30.5	55.0~63.0
Ripple and Noise (mV, p-p)						
source	(typ)	5mV	15mV	15mV	25mV	35mV
	(max)	10mV	30mV	30mV	40mV	90mV
switching	(typ)	25mV	25mV	25mV	25mV	25mV
	(max)	40mV	50mV	50mV	60mV	60mV
spike noise	(max)	100mV	170mV	200mV	290mV	530mV

Input Current (at 25°C, with nominal input voltage, power rating at 50°C), 115/230V a-c input:
- typical — 1.2/0.6A
- maximum — 1.6/0.8A
- input fuse value — 3.15A
- typical surge current: First: 17A/34A; Second: 5A/3A
- Leakage current: UL method, 120V: 0.5mA; UL/VDE, 240V: 0.75mA

Typical efficiency: 75%
Size: 1.8″W x 4.3″H x 7.5″D/45 x 110 x 190 mm
Weight: 1.5 lb./0.7 kg.
Price: $199



100 WATT MODELS

Model Number		RAX 5-20K	RAX 12-8.3K	RAX 15-6.6K	RAX 24-4.2K	RAX 48-2K
Output Volts		5V	12V	15V	24V	48V
Adjustment Range		4.0~5.5	8.4~13.2	12.0~16.5	16.8~26.4	32.6~52.8
Max. Output Ratings Amps/Watts	50°C	20.0/100	8.3/100	6.6/100	4.2/100	2.0/100
	60°C	14.0/70	5.8/70	4.6/70	2.9/70	1.4/70
	71°C	8.0/40	3.3/40	2.6/40	1.7/40	0.8/40
Current Limit (Amps)		22.0~24.0	9.1~10.0	7.3~8.0	4.7~5.1	2.3~2.5
OVP Setting (Volts)		6.0~6.9	13.7~15.7	17.0~19.5	27.0~30.5	55.0~63.0
Ripple and Noise (mV, p-p)						
source	(typ)	5mV	15mV	15mV	25mV	35mV
	(max)	10mV	30mV	30mV	40mV	90mV
switching	(typ)	25mV	25mV	25mV	25mV	25mV
	(max)	40mV	50mV	50mV	60mV	60mV
spike noise	(max)	100mV	170mV	200mV	290mV	530mV

Input Current (at 25°C, with nominal input voltage, power rating at 50°C), 115/230V a-c input:
- typical — 1.8/0.9A
- maximum — 2.5/1.3A
- input fuse value — 5.0A
- typical surge current: First: 17A/34A; Second: 12A/10A
- Leakage current: UL method, 120V: 0.5mA; UL/VDE, 240V: 0.75mA

Typical efficiency: 78%
Size: 2.6″W x 4.3″H x 7.9″D/65 x 110 x 200 mm
Weight: 2.4 lb./1.1 kg.
Price: $289

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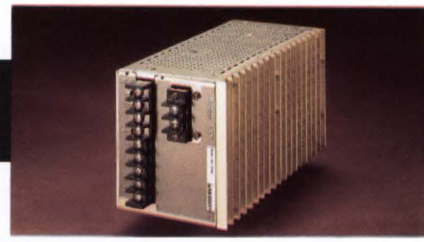
175 WATT MODELS

Model Number		RAX 5-35K	RAX 12-14K	RAX 15-11K	RAX 24-7.2K	RAX 48-3.6K
Output Volts		5V	12V	15V	24V	48V
Adjustment Range		4.0~5.5	8.4~13.2	12.0~16.5	16.8~26.4	32.6~52.8
Max. Output Ratings Amps/Watts	50°C	35.0/175	14.0/175	11.0/175	7.2/175	3.6/175
	60°C	24.5/122	9.8/122	7.7/122	5.0/122	2.5/122
	71°C	14.0/70	5.6/70	4.4/70	2.9/70	1.4/70
Current Limit (Amps)		36.8~38.5	14.7~15.4	11.8~12.1	8.0~8.3	4.3~4.5
OVP Setting (Volts)		6.0~6.9	13.7~15.7	17.0~19.5	27.0~30.5	55.0~63.0
Ripple and Noise (mV, p-p)						
source	(typ)	5mV	15mV	15mV	25mV	35mV
	(max)	10mV	30mV	30mV	40mV	90mV
switching	(typ)	25mV	25mV	25mV	25mV	25mV
	(max)	40mV	50mV	50mV	60mV	60mV
spike noise	(max)	100mV	170mV	200mV	290mV	530mV

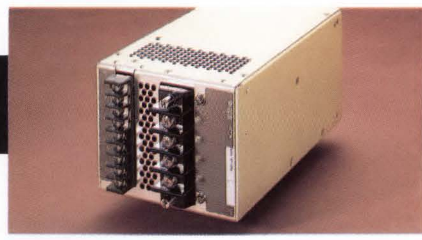


Input Current (at 25°C, with nominal input voltage, power rating at 50°C), 115/230V a-c input:
- typical — 3.4/1.7A
- maximum — 4.2/2.2A
- input fuse value — 6.3A
- typical surge current: First: 17A/34A; Second: 20A/15A
- Leakage current: UL method, 120V: 0.5mA; UL/VDE, 240V: 0.75mA

Typical efficiency: 79%
Size: 3.9"W x 4.3"H x 8.7"D/100 x 110 x 220 mm
Weight: 3.3 lb./1.5 kg.
Price: $380

300 WATT MODELS

Model Number		RAX 5-60K	RAX 12-25K	RAX 15-20K	RAX 24-12K	RAX 48-6K
Output Volts		5V	12V	15V	24V	48V
Adjustment Range		4.0~5.5	8.4~13.2	12.0~16.5	16.8~26.4	32.6~52.8
Max. Output Ratings Amps/Watts	50°C	60.0/300	25.0/300	20.0/300	12.0/300	6.0/300
	60°C	42.0/210	17.5/210	14.0/210	8.4/210	4.2/210
	71°C	24.0/120	10.0/120	8.0/120	4.8/120	2.4/120
Current Limit (Amps)		65.0~70.0	28.0~30.0	22.0~24.0	13.2~14.4	6.8~7.4
OVP Setting (Volts)		6.0~6.9	13.7~15.7	17.0~19.5	27.0~30.5	55.0~63.0
Ripple and Noise (mV, p-p)						
source	(typ)	5mV	15mV	15mV	25mV	35mV
	(max)	10mV	30mV	30mV	40mV	90mV
switching	(typ)	25mV	25mV	25mV	25mV	25mV
	(max)	40mV	50mV	50mV	60mV	60mV
spike noise	(max)	100mV	170mV	200mV	290mV	530mV



Input Current (at 25°C, with nominal input voltage, power rating at 50°C), 115/230V a-c input:
- typical — 4.6/2.8A
- maximum — 6.0/3.6A
- input fuse value — 10A
- typical surge current: First: 20A/40A; Second: 15A/10A
- Leakage current: UL method, 120V: 0.5mA; UL/VDE, 240V: 0.75mA

Typical efficiency: 77%
Size: 5.1"W x 4.3"H x 8.7"D/130 x 110 x 220 mm
Weight: 4.8 lb./2.2 kg.
Price: $520

1500 WATT MODELS

Model Number		RAX 5-300K	RAX 12-125K	RAX 24-65K	RAX 48-30K
Output Volts		5V	12V	24V	48V
Adjustment Range		4.0~5.5	8.4~13.2	16.8~26.4	32.6~52.8
Max. Output Ratings Amps/Watts	50°C	300.0/1500	125.0/1500	65.0/1500	30.0/1500
	60°C	210.0/1050	87.5/1050	45.5/1050	21.0/1050
	71°C	120.0/600	50.0/600	26.0/600	12.0/600
Current Limit (Amps)		315.0~350.0	130.0~140.0	68.0~72.0	32.0~35.0
OVP Setting (Volts)		6.0~6.9	13.7~15.7	27.0~30.5	55.0~59.0
Ripple and Noise (mV, p-p)					
source	(typ)	5mV	15mV	25mV	35mV
	(max)	20mV	30mV	40mV	90mV
switching	(typ)	50mV	60mV	60mV	70mV
	(max)	120mV	150mV	150mV	150mV
spike noise	(max)	200mV	250mV	300mV	500mV

Input Current (at 25°C, with nominal input voltage, power rating at 50°C), 115/230V a-c input:
- typical — 25/16A
- maximum — 32/18A
- input fuse value — 50A
- typical surge current: First: 20A/40A; Second: 130A/160A
- Leakage current: UL method, 120V: 1.0mA; UL/VDE, 240V: 2.0mA

Typical efficiency: 80%
Size: 8.0"W x 4.3"H x 12.6"D/203 x 110 x 320 mm
Weight: 16.5 lb./7.5 kg.
Price: $1450

Input Characteristics

Source Voltage: 85-132V a-c or 170-264V a-c, jumper selectable.

Source Frequency: 50/60Hz single phase.

Brownout Voltage: 80-160V a-c.

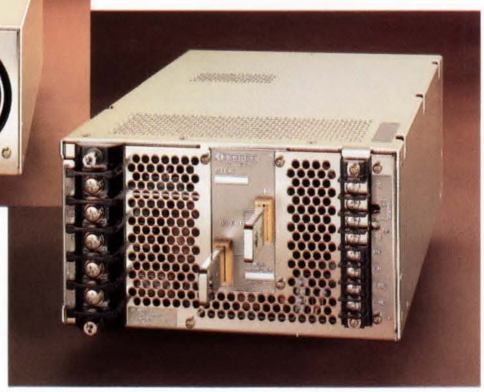
EMI (conducted): Meets FCC Class A

Holding Time: For the nominal input voltage and 50°C loading current — 30 msec typical, 20 msec minimum.

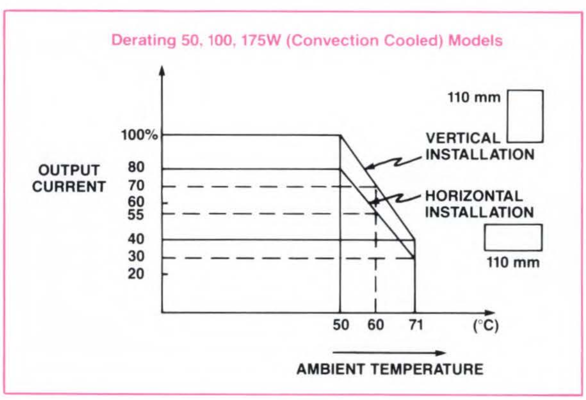
Output Characteristics

Current Limit: Fixed by an internal resistor with the threshold of the current limit within the tabulated limits. Recovery is automatic. Current limit change is less than 10% for rated changes in temperature and source voltage.

Recovery Characteristics: A step load change from 50% to 100% produces less than 4% output excursion. Recovery to within 1% of original setting occurs within 1.0 msec.



1500-Watt RAX model showing low noise d-c self-monitoring dual cooling fans to maintain optimum temperature for high reliability.



Stabilization

INFLUENCE QUANTITY	50, 100, 175, 300W Models		1500W Models	
	Typical	Maximum	Typical	Maximum
Source effect (mini-max)	0.8%	1.5%	0.2%	1.0%
Load effect (10%-100%)	0.8%	1.5%	0.3%	1.0%
Temp. effect (0.71°C)	1.0%	2.0%	0.7%	1.5%
Combined effect envelope	2.0%	4.0%	1.2%	3.0%
Time effect (0.5-8 hr.)	0.1%	0.5%	0.1%	0.5%

General

Ambient operation temperature range: 0-71°C (see model table)

Storage temperature range: −20 to +75°C

Isolation:
Input to case: 2KV a-c for 1 minute.
Input to output (Y-capacitor removed): 3.75KV a-c for 1 minute.
Output to case: 500V a-c for 1 minute.
Insulation resistance, output to case: 100 megohms minimum at 500V d-c.

Vibration: 5-10 Hz: 10mm amplitude, 3 axes, 10-55 Hz: 2g, 3 axes.

Shock: 20g, 3 axes (11 ms ± 5 ms pulse duration).

Safety: Under evaluation to become UL 478 recognized, CSA bulletin 1402 certified, VDE 0806 certified by TÜV Rheinland and IEC 380 certified by TÜV Rheinland.

Case material: Aluminum. 1500W: Ni-plated steel.

Mounting: 8-32 threads.

Certified to meet MIL STD 810D Environment:

500.1 Procedure I
Low pressure

501.1 Procedure I, II
High temperature

502.1 Procedure I
Low temperature

503.1 Procedure I
Temperature shock

504.1 Procedure I
Temperature — altitude

507.1 Procedure I
Humidity

508.1 Procedure I
Fungus

514.2 Procedure I, X
Vibration

516.2 Procedure I, III
Shock

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TEAR ON DOTTED LINE TO REMOVE AND SAVE.

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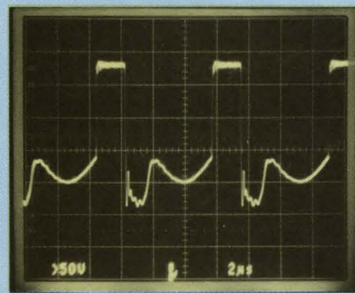
KEPCO/TDK SERIES RAX SWITCHING POWER SUPPLIES IN ACTION:

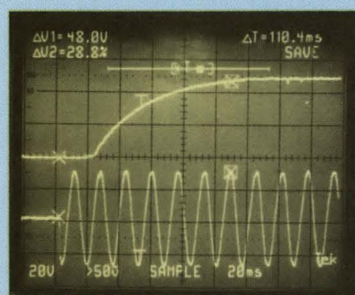
Actual scope photos of new Kepco/TDK 175-Watt Model RAX 48-3.6K (48V/3.6A)

SWITCHING WAVEFORM



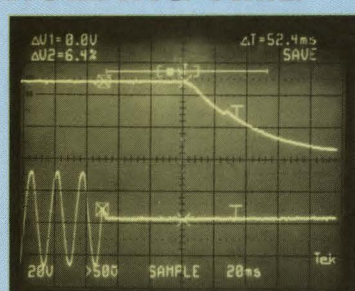
See how the fast rise and fall time of FETs contribute to the 79% efficiency of this 175 Watt model.

TURN-ON DELAY



Turn-on occurs without any overshoot.

HOLDING TIME

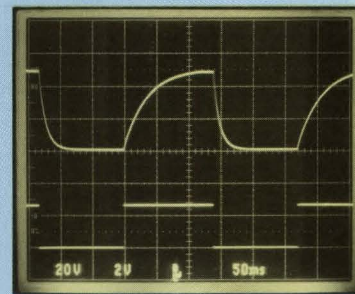


Power continues undiminished for a minimum of 20 milliseconds (30 ms typical) after loss of a-c power. Test sample measured for this photograph held up for more than 50 ms.

TRANSIENT RECOVERY TIME

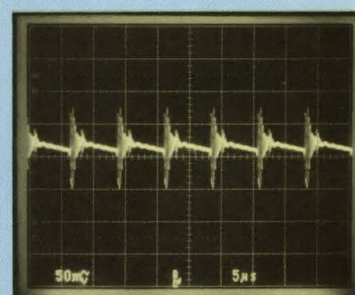
The fast switching frequency allows recovery within 1.0 msec.

REMOTE TURN-ON/ TURN-OFF



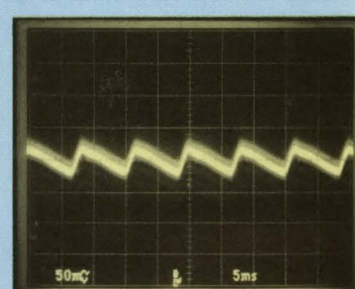
No delay at turn-on, no holding at turn-off. This remote control (RC) feature allows the output to be cycled on and off with TTL logic signals *without* any input current surges.

SWITCHING RIPPLE



25mV typical, 60mV maximum.

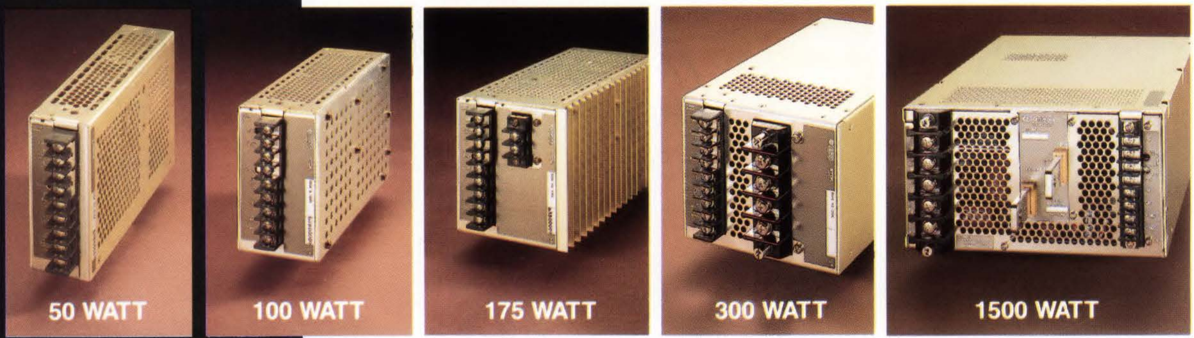
SOURCE RIPPLE



35mV typical, 90mV maximum.

SURGE LIMITING CIRCUIT

Limits turn-on current to a safe 17A at 115V a-c, 34A at 230V a-c.



NEW KEPCO/TDK INDUSTRIAL GRADE 150KHz FET-BASED SWITCHING POWER SUPPLIES

SERIES RAX

These new single output a-c to d-c modules take full advantage of all the benefits conferred by 150KHz switching, advanced technology, and hybrid microcircuitry using the latest surface mount technology: greater power in smaller sizes; higher efficiency; and lower parts count, hence higher MTBF.

They also offer loads of features, including:

— **power-on LED.**

— **remote on/off:** TTL compatible signal applied to the optically isolated "RC" terminals.

— **selectable 115/230V a-c input.**

— **active (triac) soft start circuit:** limits a-c turn-on surge.

— **remote error sensing:** compensates for voltage drops up to 0.4V per wire (0.25V in 5V models).

— **voltage adjustment:** see model tables.

— **undervoltage protection in 300W and 1500W models:** if output voltage falls below 70% of normal for any reason (including overload) and stays there for 20 seconds, power is shut off.

— **overvoltage protection:** if output voltage is forced beyond the OVP threshold, power is shut off.

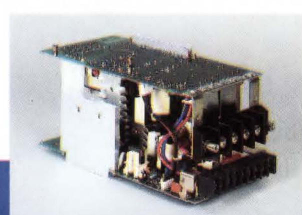
— **current balance, in the 1500W models:** allows up to 3 units to be paralleled. Current range is 20-90%.

— **holding time 20msec min., 30msec typ.:** allows for orderly shutdown of logic circuits if a-c power is lost.

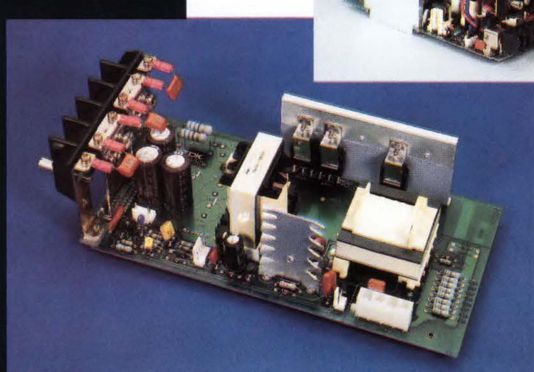
— **fan cooling in 300W and 1500W models:** monitor circuit maintains optimum temperature.

— **EMI filters:** meet conducted noise requirements of FCC Class A (industrial products).

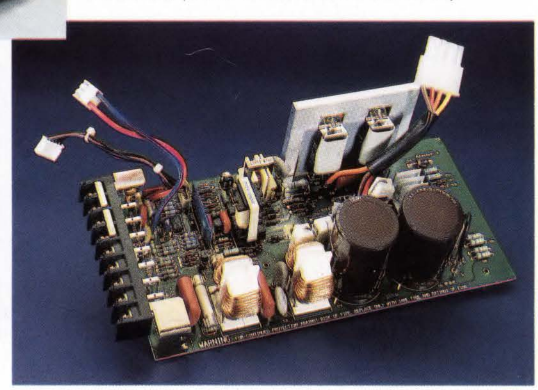
— **safety:** All models are under evaluation to become recognized by UL, certified by CSA, approved by TÜV Rheinland to VDE 0806/IEC 380, and are certified to meet the MIL STD 810D Environment.



Achieving a high MTBF takes more than simply keeping parts population low. It also takes good thermal design, which means an open, uncluttered layout. We met this goal in all the RAX models, most ingeniously in the 300-Watt models with two PC boards, as illustrated. (Cover removed to reveal details).



Top PC board showing power transformer and rectifiers.



Bottom PC board with FET switches and input EMI filters.

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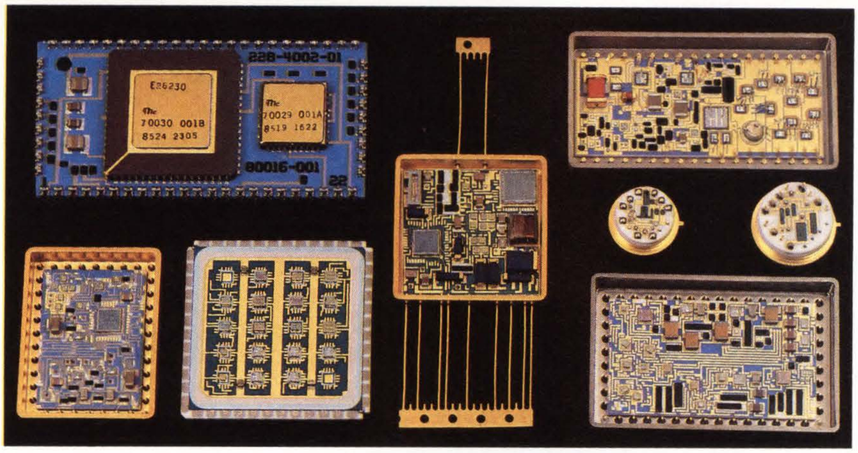
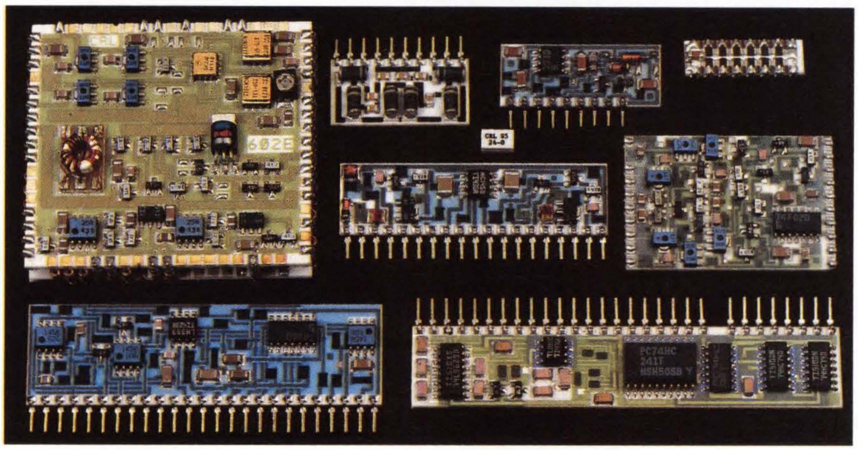
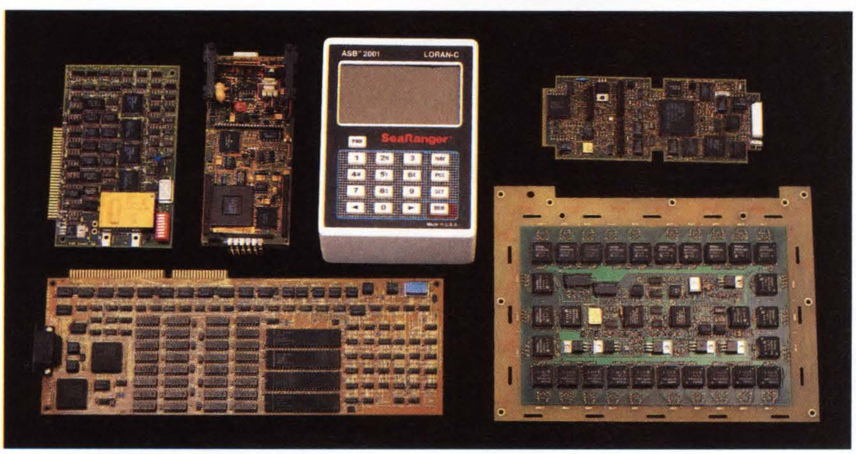
Total Contract Electronic Manufacturing Has A New Name:

PHILIPS CIRCUIT ASSEMBLIES

PHILIPS







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Philips Circuit Assemblies

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Engineering Support

The Philips Circuit Assemblies engineering team can work with you from the outset of your project to answer key questions about layout, placement and testing. We optimize your designs for peak manufacturing efficiency and performance. And provide size reductions at the lowest cost.

Quality Control

The Total Quality Control (TQC) program at Philips Circuit Assemblies is based on building products right the first time. All employees receive ongoing training aimed at developing their skills to meet Philips' high standards of quality workmanship.

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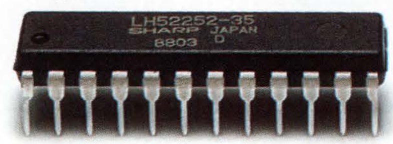

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Stringent testing ensures immunity to power-line disruptions

To be reliable, any equipment that uses mains power needs to pass certain tests that prove it's immune to power-line disturbances. And to be accurate, such tests should use rigorous test methods in a tightly controlled test setup.

Peter Green, *Stratus Computer Inc*

When equipment that uses mains power must be completely reliable, you need to be able to test the system thoroughly for its tolerance to power-line disturbances. But you need to know how and why these disturbances occur before you can set up a good test and develop some rigorous methods for qualifying your system. You also need to take international standards into account. What's more, you ought to customize your test to a particular system, so you need to know how your particular system tolerates disturbances.

Disruptions in power lines can damage your electronic system in several ways, including component failure, computer crashes, memory loss, program damage, and media destruction. Studies done at Stratus engineering labs have recorded over 30 power-line disturbances per year (including surges and low lines) during the last two years in a suburban area of Massachusetts. Daily voltage fluctuations of ±15% of the nominal line voltage are common, even daily, occurrences in most European countries. Testing for power-line disturbances is a necessary part of the development of any system where you can't afford to lose data during a power disturbance.

Disruptions in power lines have four main causes: geography, heavy-machinery operation, power-line switching, and accidents. **Table 1**, "Power-line disturbances defined," outlines the spectrum of possible disruptions. Actual disturbances usually consist of variations and multiple occurrences of these phenomena.

Many power-line disturbances stem from geographic considerations. Severe weather, such as blizzards, thunderstorms, tornadoes, and hurricanes, can disrupt power lines in many ways. Geological events like earthquakes or volcanic activity contribute to power-line disturbances. And heavily populated areas where large businesses place varying, sometimes seasonal, demands on the power lines create their own problems.

The second most common cause of power-line disturbances is heavy machinery operating in the immediate area of your system. The machinery might be an elevator, large manufacturing machinery, or another large system using the same power line as your system. Heavy machinery turning on and off produces both a sag (brownout) in the line and an inductive kick (surge).

Power-line switching causes the third type of power disturbance. Such switching is a common practice of power utilities for sharing loads by switching power-station grids during lull or peak loading hours. Power-line switching results in deformed wave shapes arising

Severe weather, such as blizzards, thunderstorms, tornados, and hurricanes, can disrupt power lines in many ways.

from frequency and voltage changes, or from high-frequency, EMI disturbances.

The fourth category, accidental causes, is a mixed bag. Their causes can be a vehicle striking a power pole or a worker switching off the wrong breaker while reconfiguring another system in the general area of your system. This category normally results in local blackouts.

Generally, power-line disturbances don't last very long. A study done by Stratus Computer's field-service group determined that 90% are less than 90 seconds in duration. Despite the frequency with which power-line disturbances occur, most have no effect because systems usually incorporate enough internal capacitance into their dc supplies for uninterrupted operation. The internal capacitance in the Stratus computer, for example, can continue to power the computer for 20 msec—or 2½ cycles—before the computer calls on the backup battery for help.

Simulating the real world in lab

A clean, controlled setup is essential for consistent power-line-disturbance test results because the power received from a wall plug is itself susceptible to the entire spectrum of power-line disturbances. Testing with such power gives unreproducible results.

A common test for simulating brownouts, for instance, uses a variac to manually vary the voltage supplied to a device under test. A variac is fine for bench-testing power supplies and devices but cannot yield reproducible, real-world tests. Manually attempting to time brownouts or blackouts using a variac is therefore imprecise.

TABLE 1—POWER-LINE DISTURBANCES DEFINED

VOLTAGE IMPULSE	POSITIVE AND NEGATIVE SPIKES, 2500V, <50 μSEC
VOLTAGE SURGE	1.5×LINE VOLTAGE, <0.16 SEC
OVERVOLTAGE	10% OVER LINE VOLTAGE, >10 SEC
UNDERVOLTAGE	10% UNDER LINE VOLTAGE, 16.6 mSEC TO 5 MINUTES
BROWNOUT	>10% UNDER LINE VOLTAGE, 16.6 mSEC TO 5 MINUTES
CYCLE DROPOUT	0V, 8.3 mSEC TO 10 SEC
BLACKOUT	0V, >10 SEC
FREQUENCY FLUCTUATION	±5% NOMINAL LINE FREQUENCY

Furthermore, manual variac swings and power-line disturbances have different characteristics; power-line disturbances are not linear. Their rates are related to a particular frequency (50 or 60 Hz). For example, a true brownout starts and finishes in a half cycle, not on a gradual decline or rise as achieved with a manually operated variac.

Pulling the plug doesn't always fill the bill

Another simple, but inadequate test method, is the one that attempts to simulate a blackout by manually pulling the system under test's ac plug. Although this method is acceptable for blackouts of durations greater than four seconds, it cannot produce consistent results for outages of less than four seconds. For example, it can't simulate the commonly encountered half-cycle dropout.

Manual power-line-disturbance testing can't mimic the complexity of normal power-line disturbances. Surges normally follow brownouts and blackouts. Power-line disturbances have different variations and multiple effects. Frequently, power lines fail, return for a few seconds, then fail again.

The electronics market is international, and many power standards exist. To develop a comprehensive test setup, you must understand power standards and power needs throughout the world. You must test approximately 10 to 15 power configurations to validate a given system's suitability for worldwide applications (see **Table 2,** "International power standards"). Therefore, a test setup must provide different voltage and frequency test stimuli. In addition, a power-line-disturbance test setup must provide different voltages for a main chassis and a peripheral cabinet, as well as test all components simultaneously.

To provide clean power, precise timing, characteristic testing, and various power configurations, you need a test setup and software specifically tailored to the job **(Fig 1)**. To do this, you must first understand the hardware and software that make a particular system

TABLE 2—POWER STANDARDS BY COUNTRY

100V, 50 AND 60 Hz	JAPAN
120V, 60 Hz	USA, CANADA
200V, 50 AND 60 Hz	JAPAN
208V, 60 Hz	USA, CANADA
220V, 50 Hz	EUROPE
240V, 50 Hz	EUROPE
240V, 60 Hz	USA, CANADA

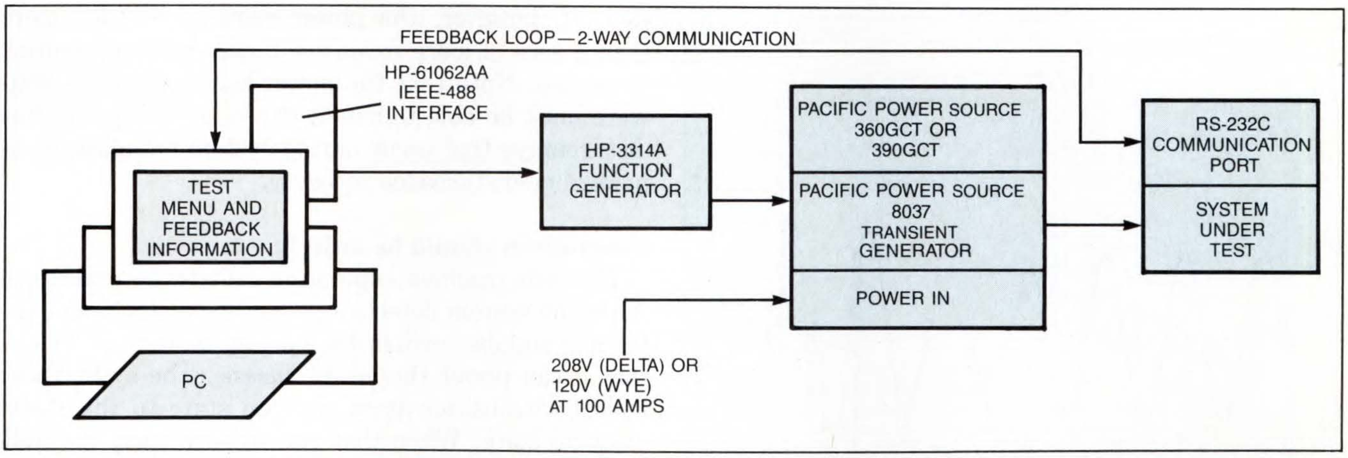

Fig 1—This test setup provides clean power, *precise timing, characteristic testing, and simulates various worldwide power configurations.*

fault-tolerant. Proper handshaking between software and hardware is critical for system recovery. Consider, for example, the Stratus Model 50. The basis for its fault-tolerant architecture is redundant logic. Its power-line-disturbance tolerance and recovery schemes guarantee that no data loss occurs, no processes are destroyed, and no hardware fails during or after power-line disturbances.

In the chassis of the Model 50, its duplicate, redundant components are separated into odd and even slots. Even its ac power comes into the even and odd ac bulk supplies on separate line cords as an option. The ac bulk supplies are the source for the dc power supplies, which power odd and even slots in the main chassis. In this main chassis, all CPUs, memory units, I/O peripheral controllers, and peripherals (excluding tape drives) are duplicated.

In addition to redundancy, the Model 50 architecture has three other safeguards against power-line disturbances: EMI suppression, voltage tolerance, and timing tolerance. These features are built into the ac and dc bulk power supplies. The ac bulk power supplies are the system's first line of defense against power-line disturbances. They monitor the voltage level of the ac line and notify the CPUs if that level drops below 83% of nominal. The ac bulk supplies also provide surge suppression. Line filters suppress conducted EMI and low-energy spikes. (High-frequency radio or television transmissions generally cause these low-energy spikes.)

The ac bulk power supplies step down the mains voltage to 24V ac and control power-on and -off sequencing for the peripheral cabinets. That sequencing prevents local brownouts and surges that occur when you try to power up all the chassis at once. In this way, the ac bulk supply prevents self-induced line disturbances.

Constant-voltage transformers are pivotal

The greatest electrical protection against power-line disturbances are the ac bulk supplies' step-down constant-voltage transformers (CVTs). The CVTs are ferroresonant transformers that hold their secondary voltages constant in the face of input-line fluctuations between ±20%. The ferroresonant transformers also have a low primary-to-secondary capacitance and a high inductance that act as good surge and noise suppressors.

The ferroresonant transformers have tertiary windings that lie between the primary and secondary windings for load regulation. If input fluctuations exceed 20%, the ferroresonant transformers saturate. In this mode, they shut down their secondary outputs, taking the dc power supplies off line. The power supplies then smoothly handle the power-line disturbance without internal damage. If the resulting voltage surge lasts for less than a few cycles, the system's internal capacitance holds the dc levels constant. If, on the other hand, a brownout occurs, an input relay disconnects the transformers after an approximately 17% drop. The supplies then send an ac-fail signal to the CPUs, which activate the system's battery backup.

Another aspect of the design anticipates the power fluctuations that occur after a power-line disturbance. The system waits for two seconds after the ac-fail signal is inactive before turning the input relay back on. That interval allows adequate time for the power line to settle, and protects the CVTs from surges that often

In electronic systems, power disruptions can cause component failure, computer crashes, memory loss, program damage, or media destruction.

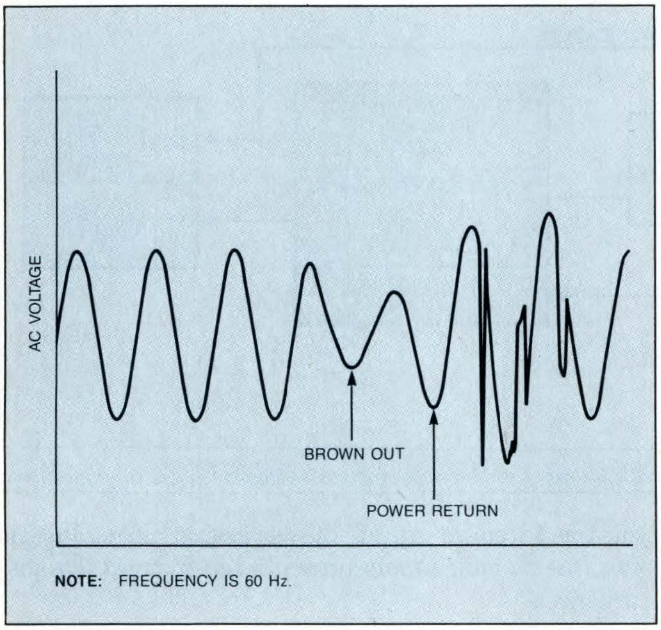

Fig 2—Fault-tolerant systems need to wait *for the power line to settle before resuming mains power to protect themselves from surges that often occur at the end of many power-line disturbances.*

occur at the end of power-line disturbances **(Fig 2).**

The two dc bulk power supplies receive 24V ac, convert it to 24V dc, communicate with the CPU, and act as a rudimentary UPS (uninterruptable power supply). The logic built into the dc bulk supplies monitors the ac-line voltage, backup-battery, and fan status. The CPUs can command the dc bulk supplies to change their state in response to various events. A 5-part state machine controls the bulk supplies' power-fail sequence **(Fig 3).** The supplies' five states are:

- Run—normal operation
- Store—ac failure of less than 6 seconds (ride-through)
- Hold Memory—ac failure of greater than 6 seconds
- Battery Lasted—ac recovery successful
- Off—ac recovery unsuccessful, shutdown.

The dc bulk-supply state machine involves handshaking between the hardware and software. The state machine's design allows for two lengths of power failures. The system can survive a 6-sec interruption without any change in state. Therefore, if the power returns within 4 secs (leaving a 2-sec safety margin), the system remains uninterrupted. This type of power-line disturbance recovery is known as a system ride-through. It allows the system to handle 20% of all real-world power-line disturbances without interruption. If, however, the power remains bad for more than 4 secs, a more extensive power-recovery routine is needed. Note that the power-line-disturbance software must be able to handle the repetitive power-line disturbances that occur during system initialization or power-line-disturbance recovery.

Power-down should be orderly

The state machine's operation includes several steps. After the system detects a power-line disturbance, the dc bulk supplies switch the backup battery on line so that it can power the entire chassis. The system also makes a transition from the run state to the store-machine state. When that transition occurs, the bulk supplies set the ac-fail signal. This signal goes to the CPUs in the odd and even slots. The bulk supplies remain in the store state, waiting for the CPU to complete its power-fail routine or for the line voltage to return. One advantage to this method is that the bulk supplies provide battery power for the entire chassis throughout the ride-through period, which means that the I/O controllers need not be reinitialized when power returns; the system only needs to restart any ac-powered peripherals (eg, disk drives).

If the line disturbance continues for a longer period than the ride-through time-out, the system goes into a full power-failure condition. In this mode, all CPUs get notified of the power-failure and they then save their current machine state. All except one designated CPU now halt, and then the designated CPU branches to the power-fail entry point in its PROM.

CPU generates record

Part of the designated CPU's power-failure routine entails generating a table of the current CPU and memory configuration. This table, along with certain information on the current virtual-memory mapping, gets stored in physical memory. The CPU then commands each on-line memory to put itself into the battery-backup mode (a mode where power goes only to the RAM chips and their refresh circuitry).

Then the CPU commands the bulk supplies to switch from supplying power to the entire chassis to supplying power only to the memories in the battery-backup mode. After issuing this command, the CPU loses power and cannot continue processing, although memory is maintained.

When the power-line disturbance ends, assuming the disturbance was not long enough to completely drain the battery, the bulk-supply state machine switches

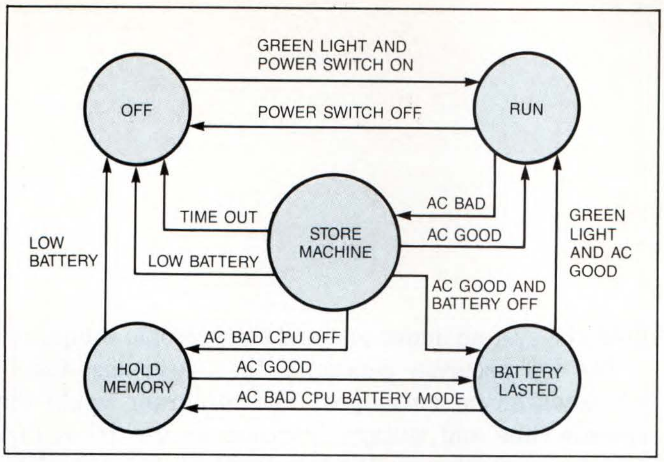

Fig 3—This state machine *controls the operation of the fault-tolerant computer.*

to the "battery lasted" state, and the bulk supplies start supplying dc power to the entire system once more.

Upon regaining its power, the designated CPU starts running its start-up code from its PROM—a routine similar to its normal power-up procedure. During this bootstrap process, all I/O controllers are reset and onboard self-tests run. Prior to initializing the RAM chips, the CPU checks the bulk supplies' status; if the bulk supplies are in the "battery lasted" state, the CPU PROM branches to its power-fail recovery procedure.

Checking the system as it starts to run

During the PROM power-fail recovery procedure, the CPU checks selected memory locations to verify that no errors exist within the memory (any errors would indicate that the memory did not survive the power failure). The CPU tests each memory against the memory and CPU configuration table that it built (and stored) prior to losing power. The CPU then reconfigures the memories to match their conditions prior to the power-line disturbance. If no memory error exists, the memory configuration remains unchanged.

At this point in the sequence, the virtual-memory mapping information gets restored, and the CPU then returns to the operating system. Upon receiving control, the operating system starts up all of the disk drives. The disk controllers have built-in routines to enable primitive I/O operations to start the disk drives and perform file-system read operations. This primitive disk firmware is necessary to begin power-line disturbance recovery and system restarts.

Once the disk drives are operating, each I/O controller is reloaded with its respective drivers and are notified of the power-failure. This notification allows the I/O controllers to perform any cleanup work necessary as the result of the power failure. All additional CPUs now restart, and they all have access to the internal information that was stored during the power failure. The system is now back running in normal mode once more.

Testing a machine such as the System 50 is complicated because the system has both software and hardware for power-line-disturbance recovery. To get a complete picture of the system's tolerance to power-line disturbances, you need to test isolated components as well as the system as a whole; furthermore you need to be able to simulate system usage and diagnose the status of the system at any given time.

Power-line-disturbance testing should first test the peripheral cabinets and the main chassis individually. After you run these individual tests, you can test the complete system. Isolation testing is important because different power circuits are wired throughout the same lab. Often power-line disturbances affect a particular chassis because loading or an accident occurs on a particular circuit.

You should define both maximum and minimum configurations for all modular components of the system, but testing the maximum configuration is more important. In CPUs, for example, testing the system with its maximum number of CPUs means testing bus activity and various other processes very thoroughly. Furthermore, testing the maximum memory configuration also tests the ability of the battery to maintain data integrity for a specified power-line-disturbance duration.

Avoid data loss at all costs

Testing maximum configurations is particularly important for peripheral and communications devices because these devices are the most susceptible to power-line disturbances—they must survive without a glitch, or data losses could result. And data loss in a fault-tolerant system is a contradiction in terms.

Another important aspect of power-line-disturbance testing is simulating normal system usage during testing. Diagnostic tests running on the system under test's CPUs should exercise all major system components, such as the CPU, bus, disks, network, and memory. System activity exercises the operating-system software's and hardware's ability to recover under adverse conditions.

In addition to diagnostic software that runs on the system under test, you also need software for the power-test equipment so that the transient generator and the system under test can communicate. The software should do three things:

- It should provide a flexible test script that can simulate the full spectrum of power-line disturbances.
- The software should be able to detect system-

Heavy machinery operating in the immediate area of your system can disturb the power.

under-test inconsistencies or defects.

- The programs should also permit the operator to intercede if necessary for isolating problems that routine, automated tests don't uncover.

Macro initiates testing

To start the diagnostic tests, you use a macro that runs under the operating system of the test-system computer and that initiates the diagnostics (see **box**, "Creating your own universe of predictable power"). One such diagnostic program monitors the system under test's battery status, ac failures, and board configurations. The macro also controls data files from which it produces power-line-disturbance test sequences for the power-test equipment. A communications package links the system under test and the personal computer.

The PC program generates the power-line disturbance-waveform envelopes. This program sends the specific time and voltage functions to the HP-3314A function generator via the HP-61062AA PC controller. The HP-3314A function generator in turn outputs ±5V dc signals that the 8037 transient generator uses to create a specific power-line disturbance.

When the test is over, control returns to the command macro. It waits a specified amount of time for the unit under test to recover. The power-line-disturbance diagnostic program, which runs on the system under test's computer, monitors the test system during its recovery period.

The power-line-disturbance diagnostic program de-

Creating your own universe of predictable power

The ac-line test setup used at Stratus requires a 390GCT or 360GCT programmable power supply and an 8037 Transient Generator, which are both manufactured by Pacific Power Source Corp (Huntington Beach, CA), and an HP-3414A function generator. With this setup, you can qualify products under all forseeable power conditions. It also improves troubleshooting of field problems because adequate testing of the system has already been done. **Fig 1** shows the power test system's setup.

The 390GCT ensures reliable voltage and frequency. It also provides all specified international voltages simultaneously (see **Table 2**). In addition, the 390GCT allows variable frequency for normal operation from 47 to 500 Hz. For maximum-configuration testing, it's capable of 13.8 kVA.

The 8037 Transient Generator allows manual control of voltage and frequency outputs. Its external mode features a ±5V programmable interface for voltage or frequency. In conjunction with an HP-3414A function generator, the transient generator can create power-line disturbance waveforms via the IEEE-488 bus and an IBM or compatible PC.

The power test setup used at Stratus has two parts. The first part regulates voltage and frequency, and the second utilizes the programmable features and feedback from the unit under test to inform the test program after recovery.

The 390GCT generates the desired voltage and frequency, provides clean power, and adequately powers a main cabinet with two full peripheral cabinets. The 8037 transient generator is wired to the 390GCT cabinet. The transient generator creates cycle dropouts, brownouts, and surges. A ±5V dc signal controls the programmable 8037 transient generator. The Pacific Power Source transient generator does not produce spikes—other test equipment does.

An HP-3314A function generator drives the programming input to the PPS 8037 transient generator. The HP 3314A can create a ±5V dc output wave with 150 variations. Each variation (or test vector) can be at a different dc level, and thus a given set can create complex power-line disturbances when applied to the transient generator.

You can program the HP-3314A via the IEEE-488 bus. You can load a series of test vectors into the 3314A's local memory. An IBM PC compatible with an HP 61062AA IEEE-488 interface card and command library loads the test vectors into the HP 3314A. The PC also monitors the unit under test via an asynchronous port (RS-232C) and recognizes when the unit under test has recovered from a power-line disturbance. The PC and its system software accomplish the programmable portion of this power test setup.

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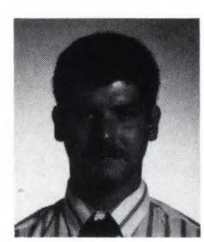
tects changes in controller and peripheral configurations or in the system's internal registers that are necessary to power-line disturbance recovery. These control signals monitor the battery, fan, and ac status. Battery status is checked because if the battery is not charged, successful recovery from the power-line disturbance is impossible. If no fans are running, a meltdown may occur. The ac status is important for the operating-system control; the test system must be signalled if the system under test did not properly recognize the power failures. If any error exists in these three areas, the diagnostic program signals the command macro running on the PC to stop the test sequence.

Direct intervention is a necessary option

You need to be able to intervene directly and you also need to log errors in order to recognize and diagnose various system failures during power-line disturbances. Even if your test setup is totally automated, only the human eye can receive the messages from the power supplies and the system console. Understanding the hardware and software allows you to interpret failures.

Disk peripherals, for instance, can be in the act of reading or writing as a power-line disturbance occurs, and disk-read and -write errors can result. These errors are acceptable as long as the disk recovers and registers a CRC error; if not, you must note that the disk failed to log the error. EDN

Author's biography



Peter Green is a supervisor in the Tools Group of the System-engineering Division at Stratus Computer Inc (Marlboro, MA). In that position, he deals with power architectures and signal-integrity issues. Before joining Stratus, Peter worked for Onkilogic (formerly Mosaic Technologies) and Digital Equipment. He graduated from Blackstone Valley Vocational Technical school and the University of Massachusetts, and sits on the Blackstone Valley Advisory Committee. Peter is married and has one daughter. His hobbies include gardening and cars.

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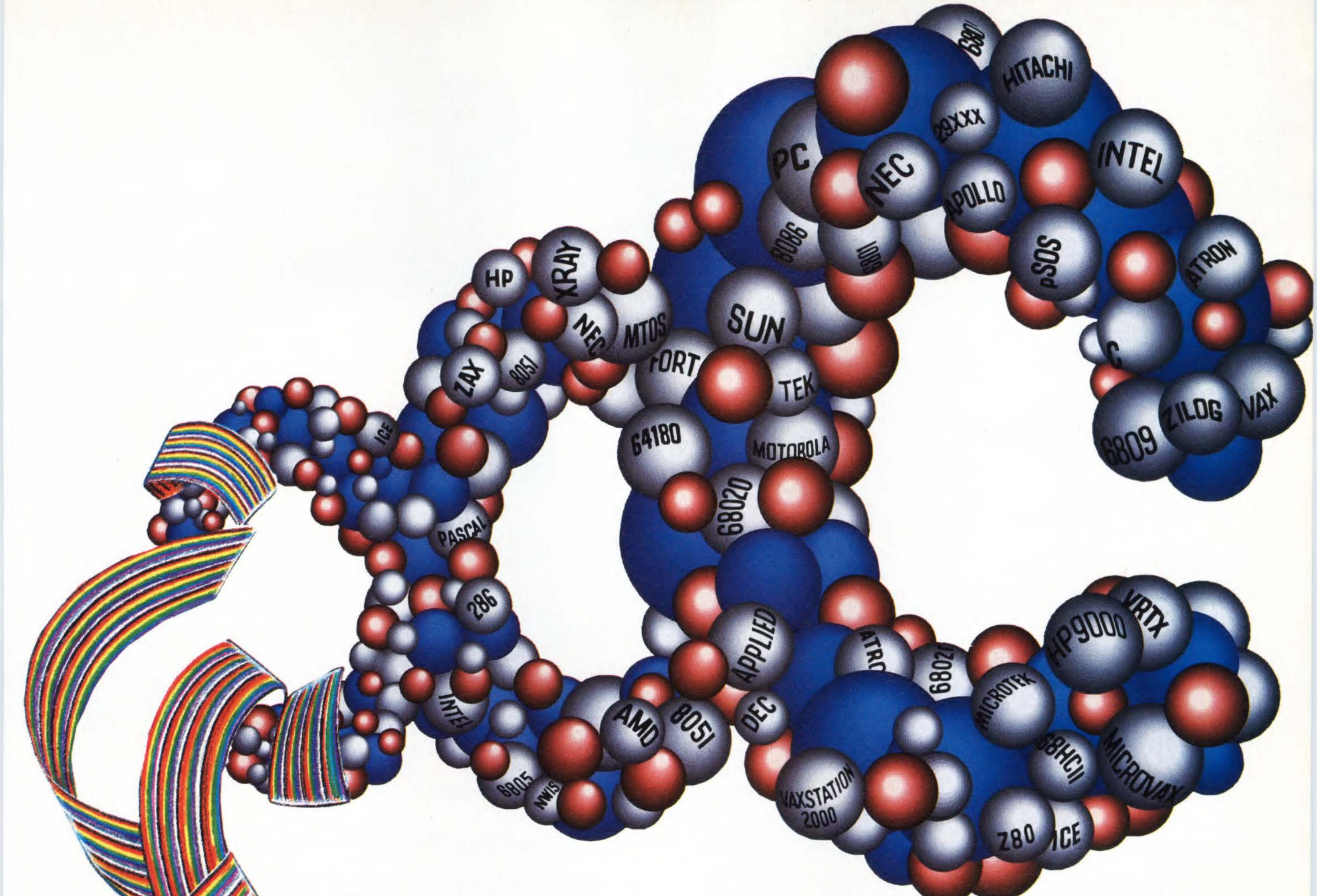

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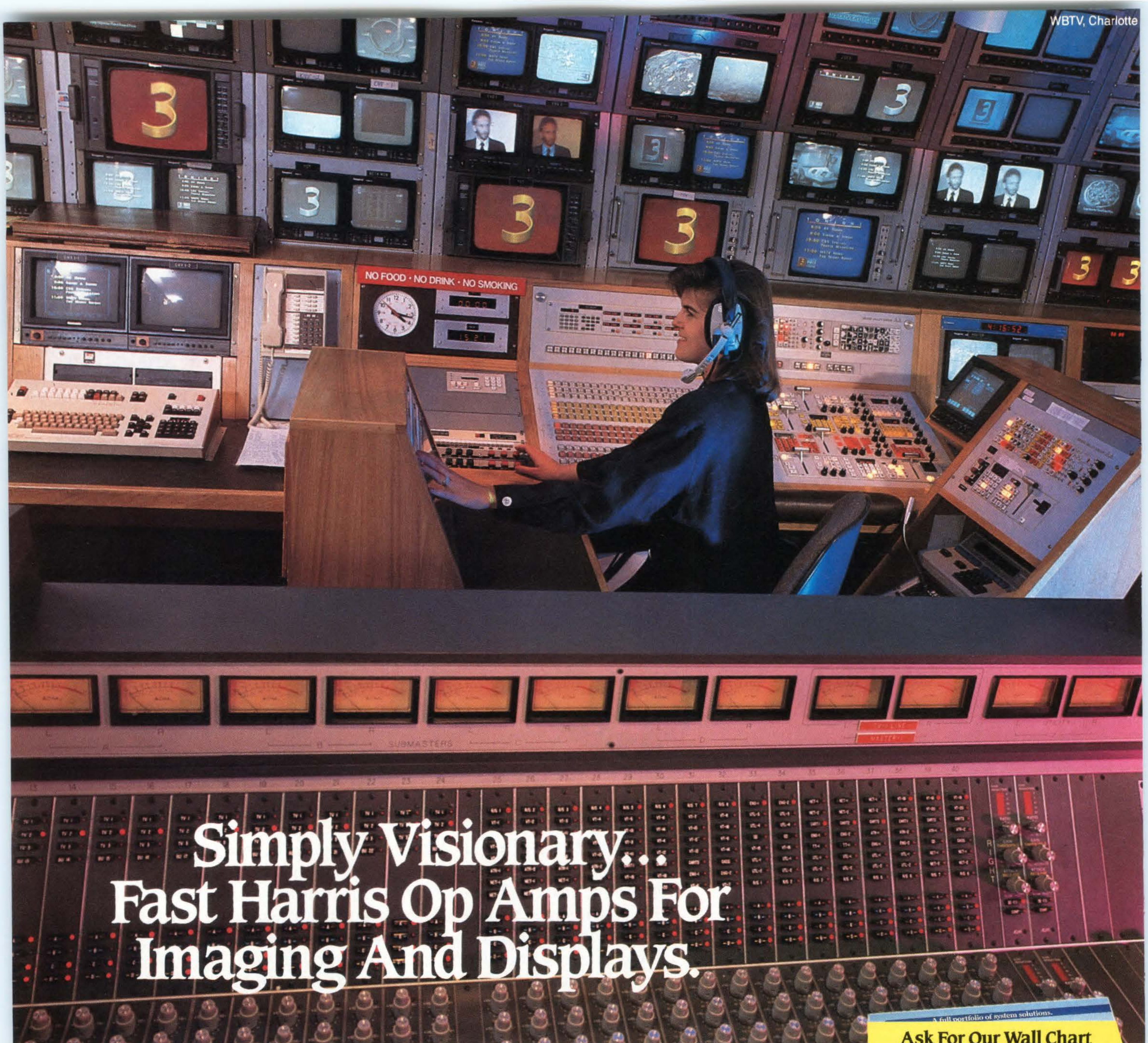

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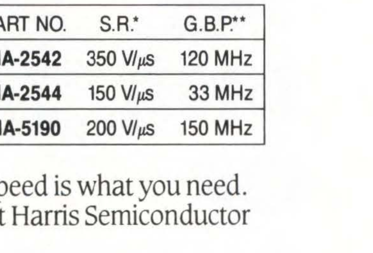

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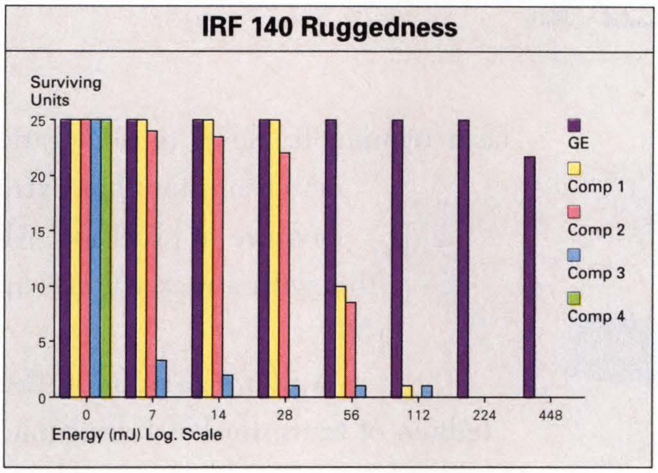

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Precise converter designs enhance system performance

DC/DC converters find application in a wide range of systems, from battery-driven circuitry to ac-line-powered systems. This article, part 1 of a 4-part series, demonstrates the design of the ubiquitous 5- to ±15V dc/dc converter. Parts 2 through 4, respectively, will show how to use instrumentation to design micropower quiescent-current converters, how to design dc/dc converters for power conservation, and how to replace inductors with switched-capacitor approaches in dc/dc-converter designs.

Jim Williams and Brian Huffman,
Linear Technology Corp

When evaluating dc/dc converters, designers often place far too much emphasis on efficiency and size. Although these parameters are significant, they are often of secondary importance. Other system-oriented requirements—low quiescent current, wide allowable-input ranges, reduced wideband output noise, and cost effectiveness—are more urgent. With the procedures presented here, you can design cost-effective 5 to ±15V dc/dc converters that have low current drain and low noise.

The case for 5 to ±15V converters

Logic supplies (5V outputs) have been popular since the introduction of diode transistor logic (DTL) over 20 years ago. Preceding, and during, DTL's infancy, modular-amplifier manufacturers made ±15V rails standard. Following tradition, early monolithic amplifiers also ran from ±15V rails. The 5V supply offers process, speed, and density advantages for digital ICs; the ±15V rails provide a wide signal-processing range for the analog components. Because of these divergent needs, 5 and ±15V supplies have also become standard for mixed digital-analog systems.

In systems with large analog-component populations, the ±15V supply was, and still is, usually derived from the ac line. This scheme, however, is definitely undesirable in predominantly digital systems. The inconvenience, difficulty, and cost of distributing analog rails in such systems makes local power generation attractive. The 5 to ±15V dc/dc converter fills this need.

Fig 1a is a conceptual schematic of a typical converter. The 5V input provides the source for a self-oscillating configuration made up of transistors, a transformer, and a biasing network. The transistors conduct out of phase, switching each time the transformer saturates. The transformer saturation develops a fast, high-current spike at the transformer's base-drive winding, which switches the transistors. The transformer current drops abruptly and then rises slowly until saturation again forces the transistors to switch. This alternating operating sets the transformer's duty cycle at 50%. The transformer's secondary signal is rectified, filtered, and regulated to produce the ±15V outputs.

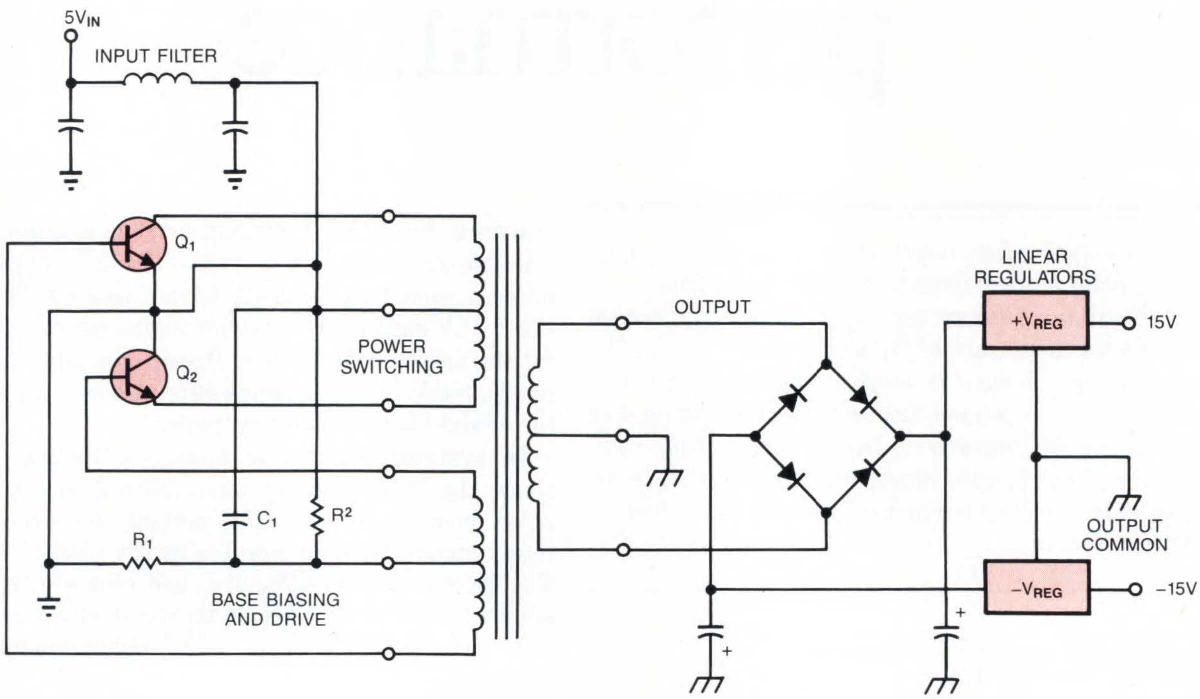
This configuration has a number of desirable features. The complementary, high-frequency (typically 20 kHz) square-wave drive makes efficient use of the

In systems that are heavily populated with digital circuitry, it makes sense to generate ±15V for analog circuits locally.

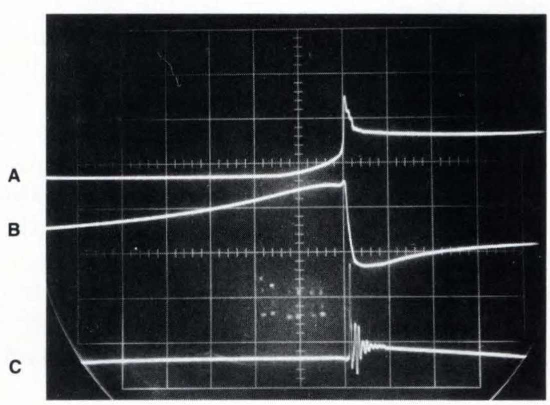
transformer and reduces the size of the filter capacitors. The self-oscillating primary drive tends to collapse under overload, providing desirable short-circuit characteristics. The transistors switch in a saturated mode, improving efficiency.

This scheme of hard switching, in combination with deliberate transformer saturation, does have one drawback, however. The significant, high-frequency current spike developed during the saturation interval develops noise at the converter outputs. The spike also draws significant current from the 5V supply—a minor disturbance, because the converters' input filter partially smooths the transient, and because 5V supplies are typically noisy anyway. The noise spikes at the output (typically 20 mV high) are a more serious problem. **Fig 1b** clearly shows the relationship among the transformer current (trace B), the transistor collector current (trace A), and the output spike (trace C).

As the transformer current rises, the transistor begins to come out of saturation. When the current



(a)



(b)

TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	500 nSEC/DIV
B	2A/DIV	500 nSEC/DIV
C	10 mV/DIV	500 nSEC/DIV

Fig 1—Although its efficiency and short-circuit characteristics are good, *this converter* ***(a)*** *suffers from poor noise performance. The waveforms* ***(b)*** *show that a current spike (trace C) generated during the switching sequence is the problem source.*

reaches a high enough level, the circuit switches and generates the characteristic noise spike. The second transistor's concurrent switching complicates the problem, causing both ends of the transformer to conduct current to ground. You can use certain design techniques, including the proper selection of transistors and output filters, to reduce spike amplitude, but this converter's output is inherently noisy.

Spike-related noise troubles analog systems

Such noisy operation can cause difficulties in precision analog systems. IC power-supply rejection at the high-harmonic spike frequency is low, and it frequently causes analog-system errors. A 12-bit successive-approximation A/D converter is a good candidate for spike-related noise problems. Sampled-data ICs (such as switched-capacitor filters and chopper amplifiers) often show apparent errors that are induced by spikes. Even simple dc circuits can exhibit baffling instabilities that are actually spike-related problems masquerading as dc shifts.

The drive scheme creates another problem—high quiescent-current consumption. Base biasing always supplies full drive, ensuring that the transistors will saturate under heavy loads, but wasting power at lighter loads. Adaptive bias schemes can minimize this problem, but they increase circuit complexity, and this type of converter rarely employs them.

The noise problem is the main drawback in this approach to 5 to ±15V conversion. Careful design techniques can minimize the converters' noise problem, but they can't eliminate it. One technique **(Fig 2)**, for example, uses a bracket pulse to warn the host system when a noise spike is about to occur. The host system ceases any noise-sensitive operations during the bracket-pulse interval. The bracket pulse drives a delayed-pulse generator, which triggers the flip-flop. The flip-flop's output biases the switching transistors in such a way that the noise spike occurs during the bracket-pulse interval. Clocked operation can also prevent transformer saturation, thereby reducing noise even further. This scheme works well, but presumes that the host can tolerate periodic intervals of inactivity when it is performing critical operations.

Low noise is important for analog circuits

The converter in **Fig 3** supplies a ±15V output from a 5V input. Its wideband noise measures 200 μV p-p—a 100% reduction over that of typical designs—and its efficiency for a 250-mA output equals 60%. The circuit achieves its low-noise performance by minimizing high-speed harmonic content in the power-switching stage. This result requires that you make the tradeoff in efficiency noted earlier, but the penalty is small in comparison with the benefit.

The 74C74 flip-flop divides the 74C14-based, 30-kHz oscillator into a 15-kHz, 2-phase clock. The 74C02 gates and the 10k/0.001-μF delay networks condition this 2-phase clock into a nonoverlapping, 2-phase drive at the emitters of Q_1 and Q_2 (traces A and B, respectively, in **Fig 3b**). These transistors act as level shifters to drive emitter followers Q_3 and Q_4. The 100Ω/0.003-μF filters loading the emitters of Q_3 and Q_4 slow the drive to output MOSFETs Q_5 and Q_6. The filter's effects appear at the gates of Q_5 and Q_6 (traces C and D, respectively).

Q_5 and Q_6 are configured as source followers. Therefore, the gate terminal's filtered slew rate limits the transformer's rise time, resulting in well-controlled waveforms at the sources of Q_5 and Q_6 (traces E and F, respectively.) The complementary, slew-limited drive source for T_1 eliminates the high-speed harmonics normally associated with this type of converter. After rectification, filtering, and regulation, T_1's output be-

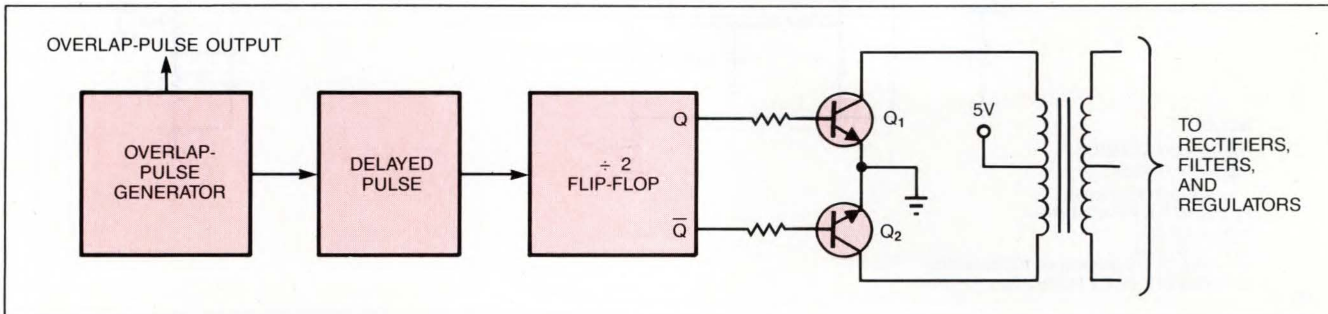


Fig 2—By sending an overlap pulse to indicate an impending noise pulse, *this circuit allows the system being powered to stop any critical operations, avoiding converter noise-related problems.*

Quiescent current, allowable input range, wideband output noise, and cost are important issues in converter design.

comes the converter's final output. The 470Ω/0.001-μF damper in T_1's secondary winding maintains loading during switching to enhance low-noise performance. The ferrite beads in the gate leads of Q_5 and Q_6 eliminate the parasitic RF oscillations associated with follower configurations.

The source-follower configuration makes it easy to control T_1's edge rise times, but complicates gate biasing. You'll require special design steps to turn the MOSFETs fully on and off. Source followers Q_5 and Q_6 require voltage overdrive at the gates, because the 5V primary supply can't provide the 10V gate-channel bias necessary for saturation. Similarly, you must pull the gates well below ground to turn the MOSFETs off, because T_1's behavior pulls the sources negative when the devices turn off.

The negative side of Q_6's source waveform provides turn-off bias. Q_3 and Q_4 pull down to the −4V level developed by D_1 and the 22-μF capacitor. A 2-stage boost loop generates the turn-on bias. The 5V supply feeds to the LT1054 switched-capacitor voltage converter via D_3. The LT1054, configured as a voltage doubler, initially provides about a 9V boost to point A at turn-on. When the converter begins operating,

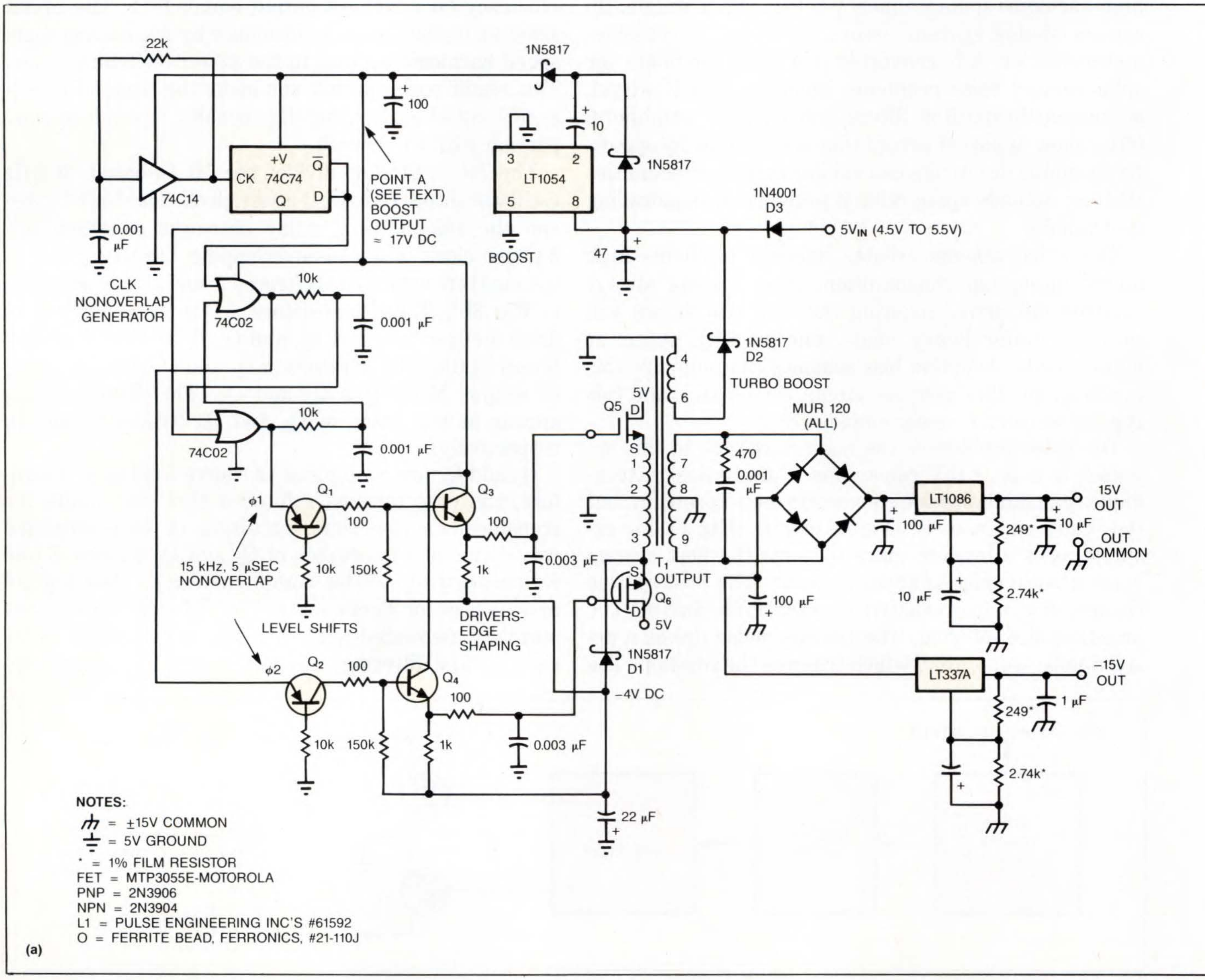
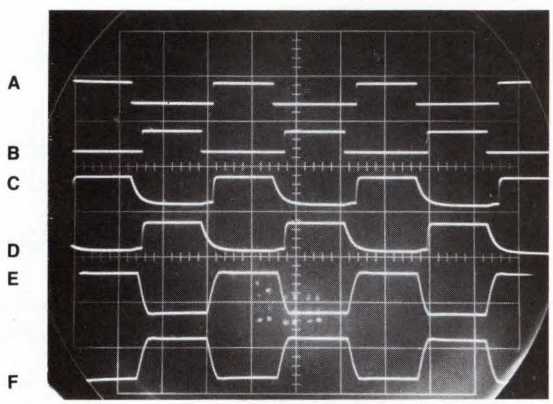


Fig 3—By minimizing high-speed harmonic content in the power-switching stage, *this converter design* ***(a)*** *achieves a 100× reduction in wideband output noise. As the waveforms* ***(b)*** *show, all the switching transitions are clean. The output noise* ***(c)*** *is only 200 μV p-p.*

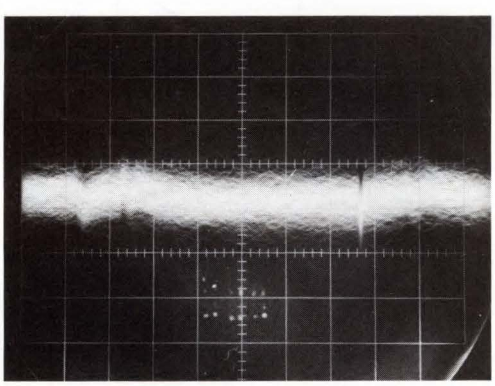
T_1 produces a turbo-boost output at pins 4 and 6. D_2 rectifies this output, which raises the LT1054's input voltage and further increases the boost at point A to approximately 17V.

These internally generated voltages allow Q_5 and Q_6 to receive the proper drive, minimizing losses despite the source-follower connection. An ac-coupled trace of the converter's 15V output **(Fig 3c)** shows 200-μV p-p noise at full power (250-mA output). The converter's switching characteristics compare in amplitude to the noise characteristics of linear regulators. You can reduce switching-related noise even further by slowing the rise times of Q_5 and Q_6. To slow the rise times, however, you must reduce the clock rate and increase nonoverlap time to maintain available power and efficiency. The arrangement shown in **Fig 3** represents a favorable compromise among output noise, available power output, and efficiency.



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	20 μSEC/DIV
B	20V/DIV	20 μSEC/DIV
C	20V/DIV	20 μSEC/DIV
D	20V/DIV	20 μSEC/DIV
E	10V/DIV	20 μSEC/DIV
F	10V/DIV	20 μSEC/DIV

(b)



VERTICAL	HORIZONTAL
100 μV/DIV	5 μSEC/DIV

(c)

Satisfy high-resolution circuits' needs

Residual switching components and regulator noise set the performance limits for the converter in **Fig 3.** Analog circuitry operating at the very highest resolution and sensitivity levels may require a converter with even less noise. **Fig 4's** converter uses a sine-wave transformer drive to reduce harmonics to negligible levels. The transformer drive combines with special output regulators to produce less than 30 μV of output noise. This value is also seven times lower than that of the previous circuit, and, in comparison with conventional designs, it approaches a 1000× improvement. If you use this circuit, you'll have to make a couple of tradeoffs, however: In comparison with **Fig 3's** circuit, **Fig 4's** circuit will be more complex and will sacrifice some efficiency.

IC_1 of **Fig 4** is configured as a 16-kHz Wien-bridge oscillator. The design uses a special bias level to prevent IC_1's output from saturating at the ground rail. Returning the undriven end of the Wien network to a dc potential derived from the LT1009 reference establishes this bias. IC_1's output is a pure sine wave (trace A in **Fig 4b**) biased off ground. To maintain the sine-wave output, IC_2 compares IC_1's rectified and filtered positive output peaks with an LT1009-derived dc reference. IC_2's output biases IC_1 and servocontrols its gain. The 0.22-μF capacitor provides temperature compensation for the loop, and the thermally mated diodes minimize errors caused by rectifier temperature drift. These provisions stabilize IC_1's ac and dc output terms against supply and temperature changes.

IC_1's output ac-couples to IC_3. The 2-kΩ/820Ω divider rebiases the sine wave, centering it inside IC_3's input common-mode range even with supply shifts. IC_3 drives a power stage consisting of Q_2 through Q_5. This stage's common emitter outputs are biased to provide a 1V rms drive for T_3—even for a supply voltage of 4.5V. With full converter loading, the power stage delivers 3A peaks, but the waveform is clean (trace B) and shows little distortion (trace C).

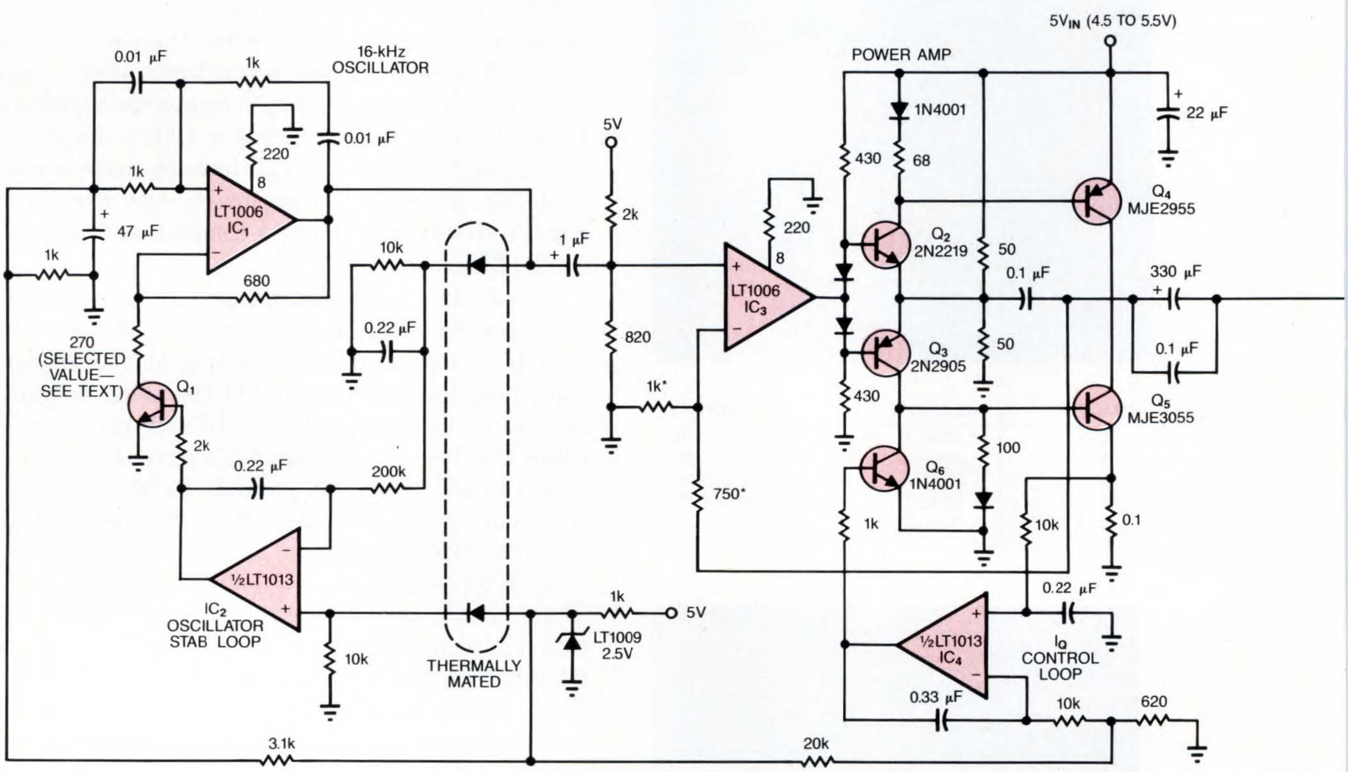
The 330-μF coupling capacitor strips dc voltage from the power-stage output, so T_3 has a pure ac input. The Q_4 and Q_5 collectors provide a feedback signal for IC_3.

Analog circuitry operating at very high levels of resolution and sensitivity may require the lowest possible converter-noise levels.

The 0.1-μF capacitor at the feedback source point suppresses local oscillations, and the RC network in T_3's secondary winding adds additional high-frequency damping.

Without quiescent-current control, the power stage will experience thermal runaway and destroy itself. IC_4 measures the dc output current across Q_5's emitter resistor and servocontrols Q_6 to establish quiescent current. A divided portion of the LT1009 reference sets the servo point at IC_4's negative input, and the 0.33-μF feedback capacitor stabilizes the loop.

T_3's rectified and filtered outputs drive regulators designed for low-noise operation. IC_5 and IC_7 amplify the LT1021's filtered 10V output to 15V, and IC_6 and IC_8 provide the −15V output. The LT1021/amplifier combination provides better noise performance than do 3-terminal regulators. The zener diode eliminates overvoltages caused by start-up transients. L_1 and L_2 combine with their respective output capacitors to minimize noise problems. These inductors are outside the feedback loop, but their low copper resistance doesn't significantly degrade regulation. Trace D, the 15V output at full load, shows less than 30 μV (2 ppm) of noise. The most significant tradeoff in this design is efficiency. The sine-wave transformer drive exacts a substantial power loss. At full output (75 mA), the



NOTES:
L_1, L_2 = PULSE ENGINEERING #92100
= 1N4148
L_3 = PULSE ENGINEERING #65064
= 1N4934
UNMARKED NPN = 2N3904
* = 1% METAL-FILM RESISTOR
+ = THF337K006P1G-MALLORY
= +5V GROUND
= ±15V COMMON

(a)

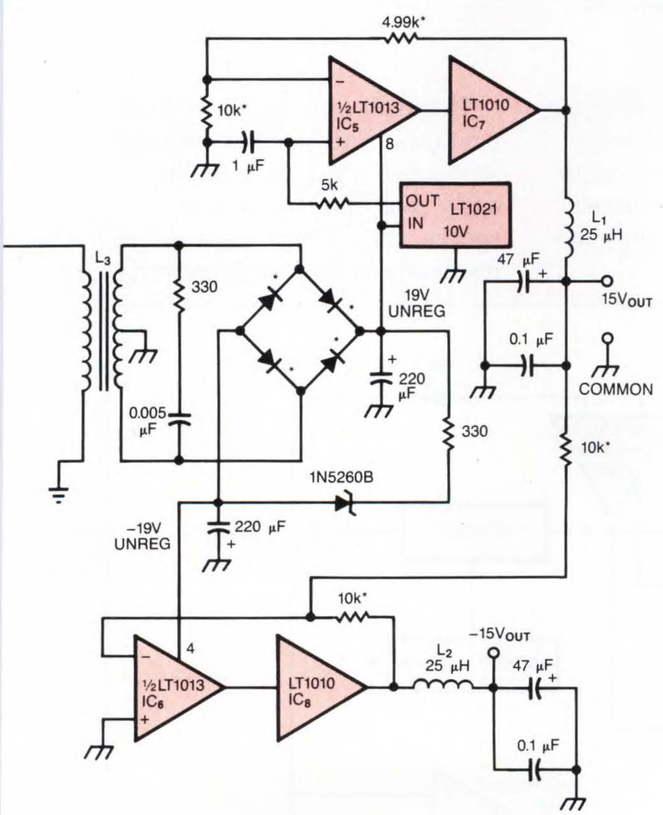
Fig 4—To improve noise performance by 1000× *over that of conventional designs, this converter **(a)** uses sine-wave transformer drive to reduce harmonics to negligible levels. As the waveforms show **(b)**, the 15V output (trace D) has less than 30 μV of noise at full load.*

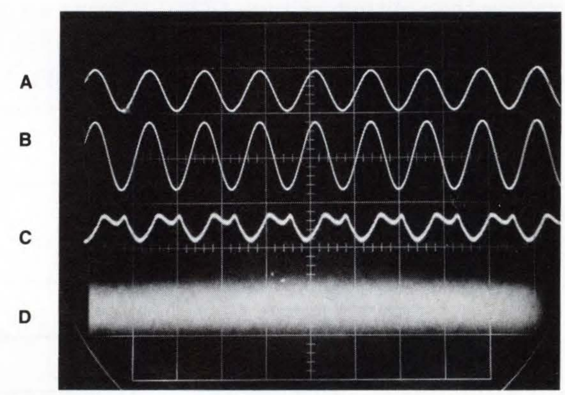
efficiency is only 30%.

Before operating the converter, you should trim the circuit for lowest distortion (typically 1%) in the sine wave at the input of T_3. You can perform this trimming by selecting the resistance value indicated at IC_1's negative input. The 270Ω value shown is nominal and can vary by ±25%. The sine wave's 16-kHz frequency represents a compromise between the op amp's available gain/bandwidth, magnetics size, audible noise, and wideband harmonic levels.

Simplicity and economy are other important considerations in 5 to ±15V converter designs. In these converters, the transformer is usually the most expensive component. The unusual drive scheme in **Fig 5**'s converter leads to significant cost savings—it uses a simple 2-terminal inductor in place of the usual transformer. The design tradeoffs are the loss of input-to-output galvanic isolation and lower power output. In addition, this circuit's isolation technique develops about 50 mV of clock-related output ripple.

Fig 5's circuit operates by periodically and alternately allowing each end of the inductor to fly back. The resulting positive and negative peaks are rectified and filtered. Controlling the number of flyback events during the respective output's flyback interval regulates the converter.





TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	50 µSEC/DIV
B	2V/DIV	50 µSEC/DIV
C	1% DISTORTION	50 µSEC/DIV
D	20 µV/DIV	50 µSEC/DIV

(b)

Simplicity and economy are important converter-design goals; you can achieve both by using a simple inductor to replace the transformer.

Inverter IC_{2A} develops a 20-kHz clock signal (trace A in **Fig 5b**), which feeds a logic network composed of additional inverters, diodes, and the 74C90 decade counter. The counter output (trace B) combines with the logic network to present alternately phased clock bursts (traces C and D) to the base resistors of Q_1 and Q_2. When ϕ_1 (trace B) is inactive, it resides in its high state, and it biases Q_2 and Q_4 on. Q_4's collector effectively grounds the bottom of L_1 (trace H). During this interval, ϕ_2 (trace A) sends clock bursts into Q_1's base resistor. If the −15V output is too low, servocomparator IC_{1A}'s output (trace E) is high and Q_1's base can receive pulsed bias current.

If the converse is true, the comparator's output will be low and will gate the bias away through Q_1's base diode. When Q_1 is open to a bias input, Q_3 switches and produces a negative-going flyback event at the top of L_1 (trace G). The flyback event is rectified and filtered to develop the −15V output. IC_{1A} regulates the number of clock pulses that switch the Q_1/Q_3 pair. The LT1004 serves as a reference.

The ac-coupled −15V output (trace J) shows the effect of IC_{1A}'s regulating action. The output stays within a small error window set by IC_{1A}'s switched control loop. As input-voltage and loading conditions change, IC_{1A} adjusts the number of permissible clock pulses to bias Q_1/Q_3 and maintain loop control.

When the ϕ_1 and ϕ_2 signals reverse state, the operational sequence reverses. Q_3's collector (trace G) pulls high, and IC_{1B}'s servo action controls Q_2/Q_4's switching

LT1070: The inside story

The LT1070 is a current-mode switcher whose duty cycle is controlled directly by switch current rather than output voltage (**Fig A**). The switch turns on at the start of each oscillator cycle and turns off when the switch current reaches a predetermined level. The output of a voltage-sensing error amplifier sets the current trip level to control the output voltage.

This technique has several advantages. First, unlike ordinary switchers, which have notoriously poor line transient response, the LT1070 responds immediately to input-voltage vari-

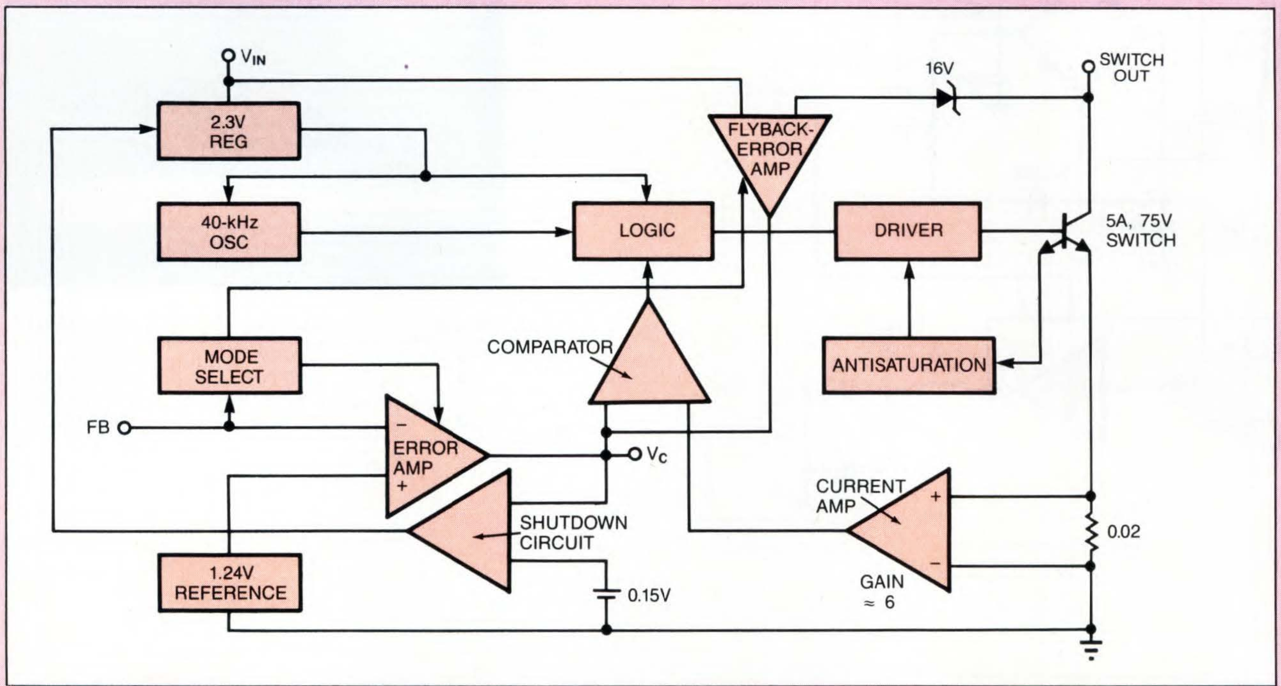


***Fig A—The LT1070 is a current-mode switcher** whose duty cycle is controlled directly by switch current rather than output voltage. Unlike ordinary switchers, which have notoriously poor line transient response, it responds to input-voltage variations immediately.*

to produce similar output waveforms. Traces F, H, and I illustrate IC_{1B}'s output, Q_4's collector signal (L_1's bottom), and the ac-coupled 15V output, respectively.

Although the two regulating loops share the same inductor, they operate independently, so no performance degradation is caused by asymmetrical output loading. The inductor sees irregularly spaced shots of current (trace K), but is unaffected by this multiplexed operation. Clamp diodes prevent Q_3 and Q_4 from reverse-biasing during transient conditions. The circuit provides ±25 mA of regulated current at 60% efficiency.

Reduced quiescent current is another aspect of 5 to ±15V converter design. Typical coverters draw 100 to 150 mA of quiescent current—a value that's unacceptably high for many low-power systems. **Fig 6's** converter design supplies ±15V at 100-mA outputs while consuming only 10 mA of quiescent current. The LT1070 switching regulator (see **box,** "LT1070: The inside story") drives T_1 in a flyback mode; the damper network clamps excessive flyback voltages. Half-wave rectification and filtering of T_1's secondary signals produces positive and negative output across the 47-µF capacitors.

A simple loop regulates the positive 16V output. Comparator IC_{1A} balances a sample of the positive output with a 2.5V reference voltage from the LT1020. When the 16V output (trace A in **Fig 6b**) is too low, IC_{1A} switches high (trace B) and turns off the 4N46 optoisolator. Q_1 turns off, and the LT1070's control pin

---

ations. Second, the current-mode configuration reduces the 90° phase shift in the energy-storage inductor at middle frequencies. This reduction greatly simplifies closed-loop frequency-compensation tasks under widely varying input-voltage or output-load conditions. Finally, the current-mode technique can use simple pulse-by-pulse current limiting to provide maximum protection for the switch under output-overload or short-circuit conditions.

A low-dropout internal regulator provides a 2.3V supply voltage for all of the LT1070's internal circuitry. Because of this low-dropout design, input-voltage variations from 3 to 60V have virtually no effect on the LT1070's performance.

A 40-kHz oscillator serves as the basic clock for all the switcher's internal timing. The oscillator uses the logic and driver circuitry to turn on the output switch. Special adaptive circuitry monitors the output switch and instantaneously adjusts the driver current to limit switch saturation.

A 1.2V bandgap reference biases the error amplifier's positive input. The amplifier's negative input is available at a pin on the package, so you can use it for output-voltage sensing. This feedback pin has a second function: When it's pulled low by an external resistor, the pin programs the LT1070 to disconnect the main error-amplifier output and connects the flyback amplifier's output to the comparator input. The LT1070 then regulates the value of the flyback pulse with respect to the supply voltage.

This flyback pulse is directly proportional to the output voltage in the traditional transformer-coupled, flyback-topology regulator. By regulating the flyback pulse amplitude, you can regulate the regulator's output voltage with no need for a direct connection between the input and the output. The output is fully floating for values as high as the breakdown voltage of the transformer windings. A special delay network in the LT1070 improves output regulation by ignoring the leakage-inductance spike at the leading edge of the flyback pulse.

The error signal developed at the comparator input comes out to an LT1070 terminal. This V_C pin provides four different functions—frequency compensation, current-limiting adjustment, soft-starting, and total regulator shutdown. During normal regulator operation, the V_C pin sits at a voltage between 0.9V (low output current) and 2V (high output current). Since the error amplifiers are current-output types, you can clamp V_C externally to adjust the current limiting. A capacitor-coupled external clamp will provide a soft-start capability.

If you pull the V_C pin to ground through a diode, the switch duty cycle will go to zero and put the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown.

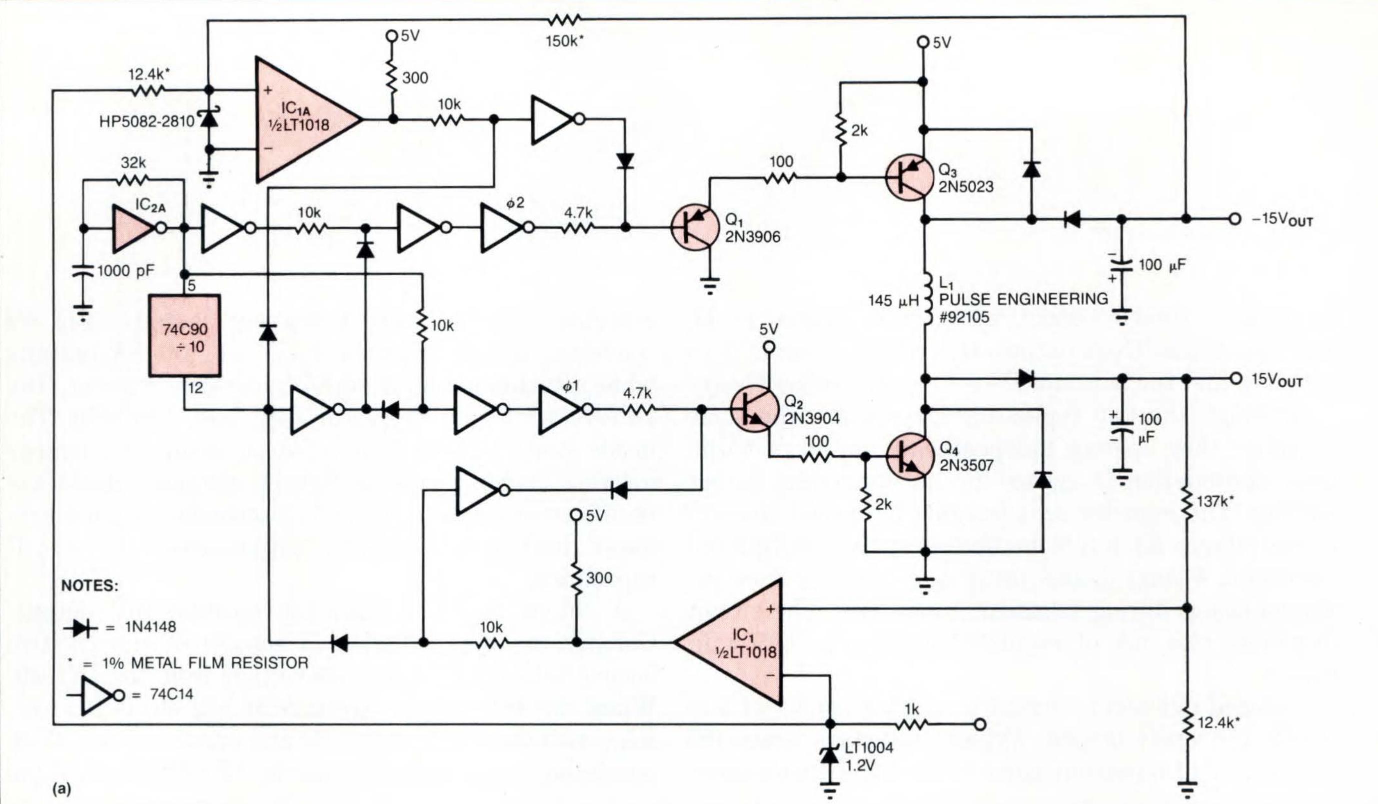


Fig 5—For circuit simplicity and economy, the drive scheme in this converter (a) uses a 2-terminal inductor in place of the usual transformer. The waveforms (b) show that although the inductor sees irregularly spaced shots of current (trace K), the multiplexed operation has no effect on the inductor's performance.

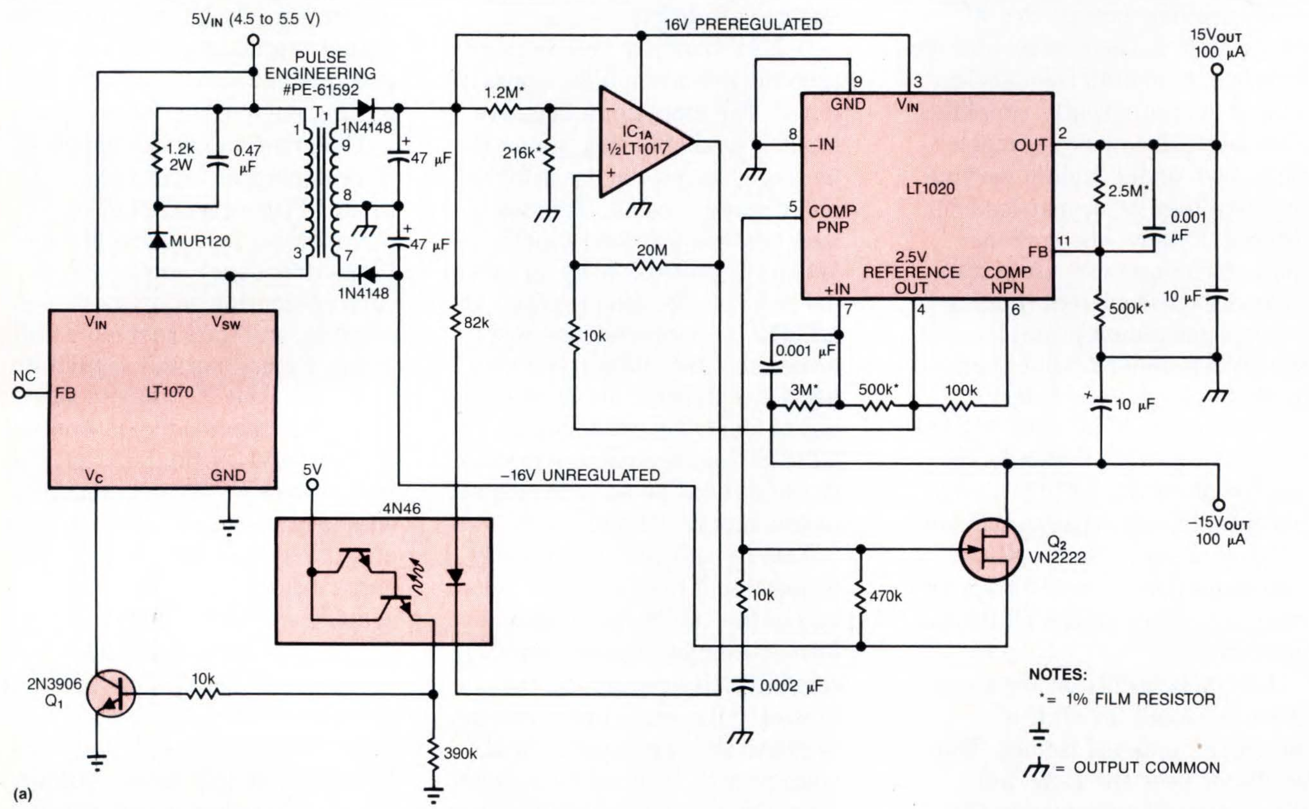
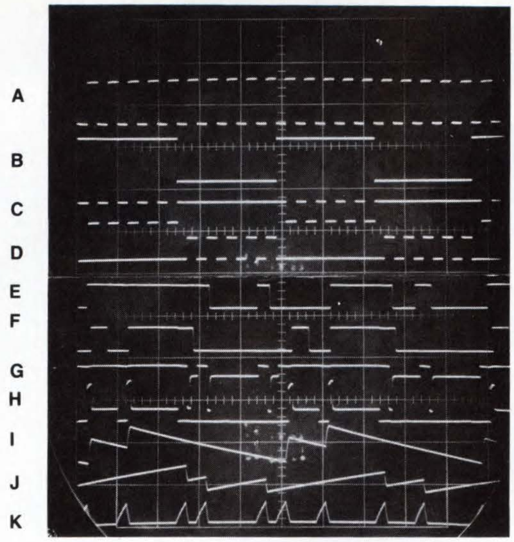
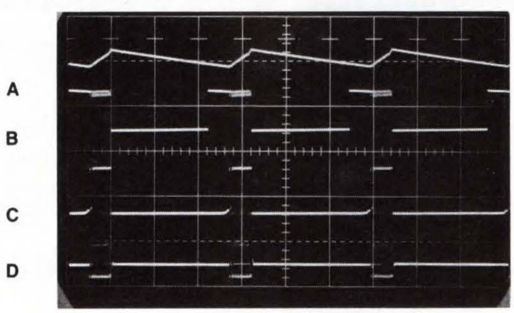


Fig 6—To satisfy the needs of many low-power systems, this converter design (a) supplies ±15V outputs at 100 mA while consuming only 10 mA of quiescent current. As trace D of the scope photo (b) illustrates, the converter has a 40-kHz switching frequency. Compared to conventional designs, this converter's efficiency (c) is far superior at light loads.



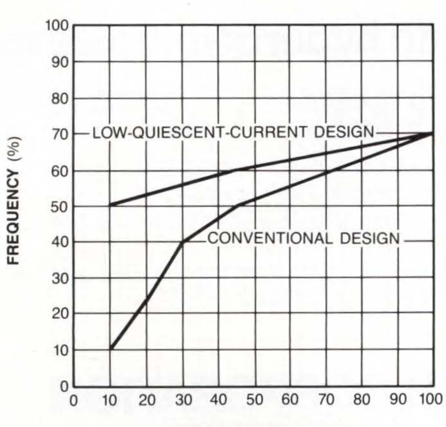
TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 μSEC/DIV
B	5V/DIV	100 μSEC/DIV
C	10V/DIV	100 μSEC/DIV
D	10V/DIV	100 μSEC/DIV
E	10V/DIV	100 μSEC/DIV
F	10V/DIV	100 μSEC/DIV
G	20V/DIV	100 μSEC/DIV
H	20V/DIV	100 μSEC/DIV
I	0.05V/DIV	100 μSEC/DIV
J	0.05V/DIV	100 μSEC/DIV
K	1A/DIV	100 μSEC/DIV

(b)



TRACE	VERTICAL	HORIZONTAL
A	100 mV/DIV	5 mSEC/DIV
B	20V/DIV	5 mSEC/DIV
C	2V/DIV	5 mSEC/DIV
D	20V/DIV	5 mSEC/DIV

(b)



(c)

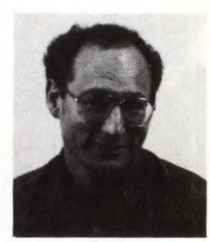
(V_C) goes high (trace C). This action generates full-duty-cycle, 40-kHz switching at the V_{SW} pin (trace D). The resulting energy into T_1 forces the 16V output to ramp quickly positive and turn off IC_{1A}'s output. The 20-MΩ resistor, combined with the slow response of the 4N46 (note the delay between IC_{1A}'s going high and the V_C pin transition) provides about 40 mV of hysteresis.

The LT1070's on/off duty cycle is load dependent, so it saves a significant amount of power when the converter operates with a light load. This characteristic is largely responsible for the 10-mA quiescent-current figure.

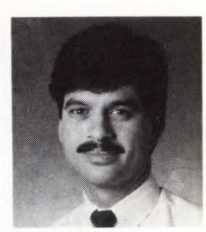
The optoisolator preserves the converter's input-to-output isolation. The LT1020, a low-quiescent-current regulator, further regulates the 16V line to develop the 15V output. This linear regulation eliminates the 40-mV ripple and improves transient response.

The −16V output tends to follow the regulated −16V line, but the regulation is poor. The RC damper at pin 5 allows the LT1020's auxiliary onboard comparator to function as an op amp. This op amp linearly regulates the −16V line. MOSFET Q_2 provides low-drop-current boost and sources the −15V output. The op amp stabilizes the −15V output by comparing it with the 2.5V reference via the 500k/3M summing resistors. The 1000-pF capacitors frequency-compensate each regulating loop. **Fig 6c** plots this converter's efficiency versus that of a conventional design for a range of loads. Although the results are similar for high loads, the low-quiescent-current circuit is superior at light loads. EDN

Authors' biographies



Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.



Brian Huffman is an applications engineer at Linear Technology Corp. A member of the IEEE, he holds a BSET dgree from Indiana State University and an MSEE from Santa Clara University. In his spare time, Brian enjoys plays, concerts, and the beach, and he likes to travel.

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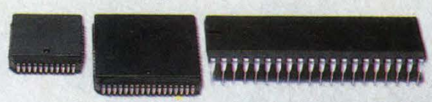

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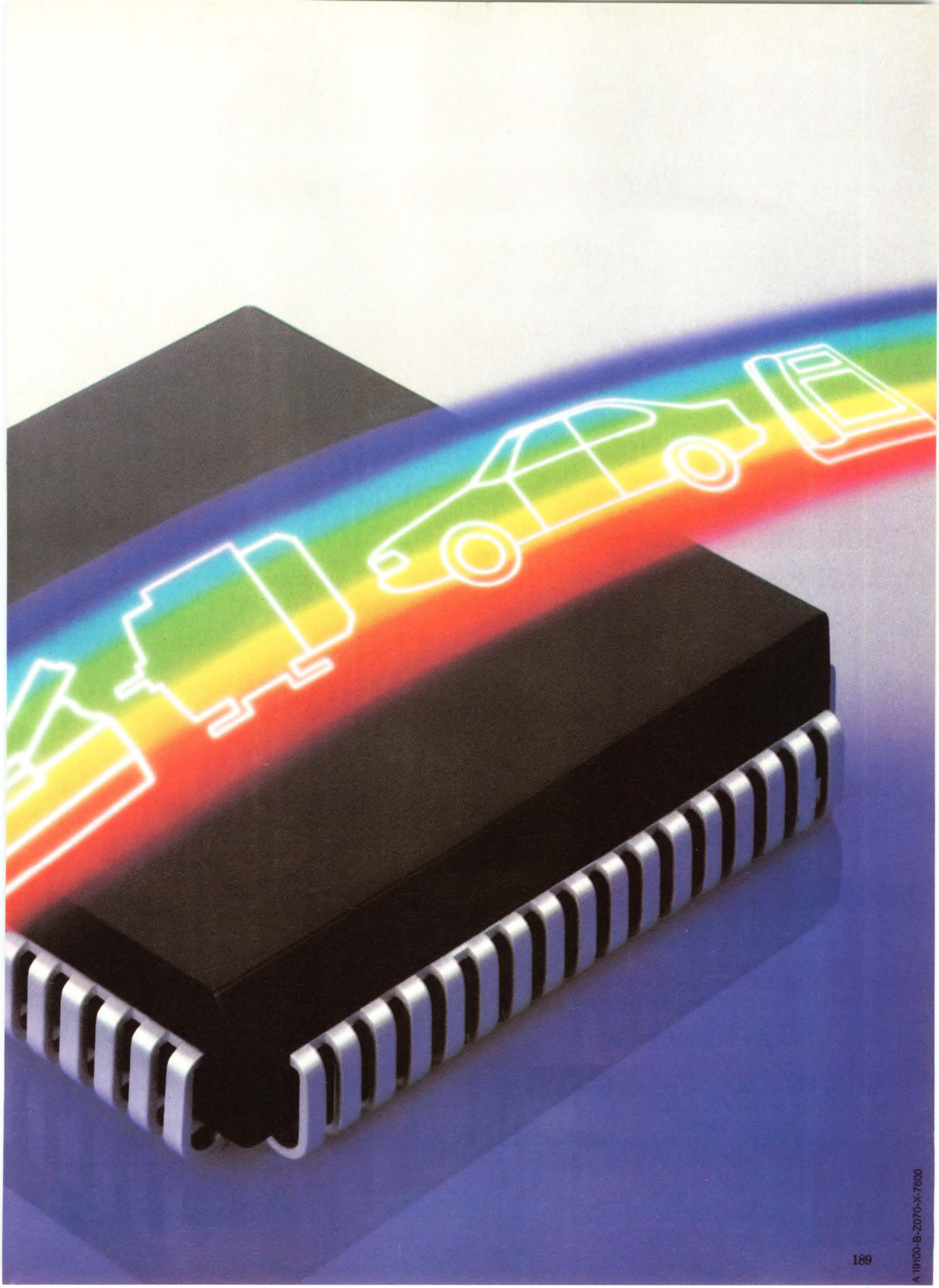

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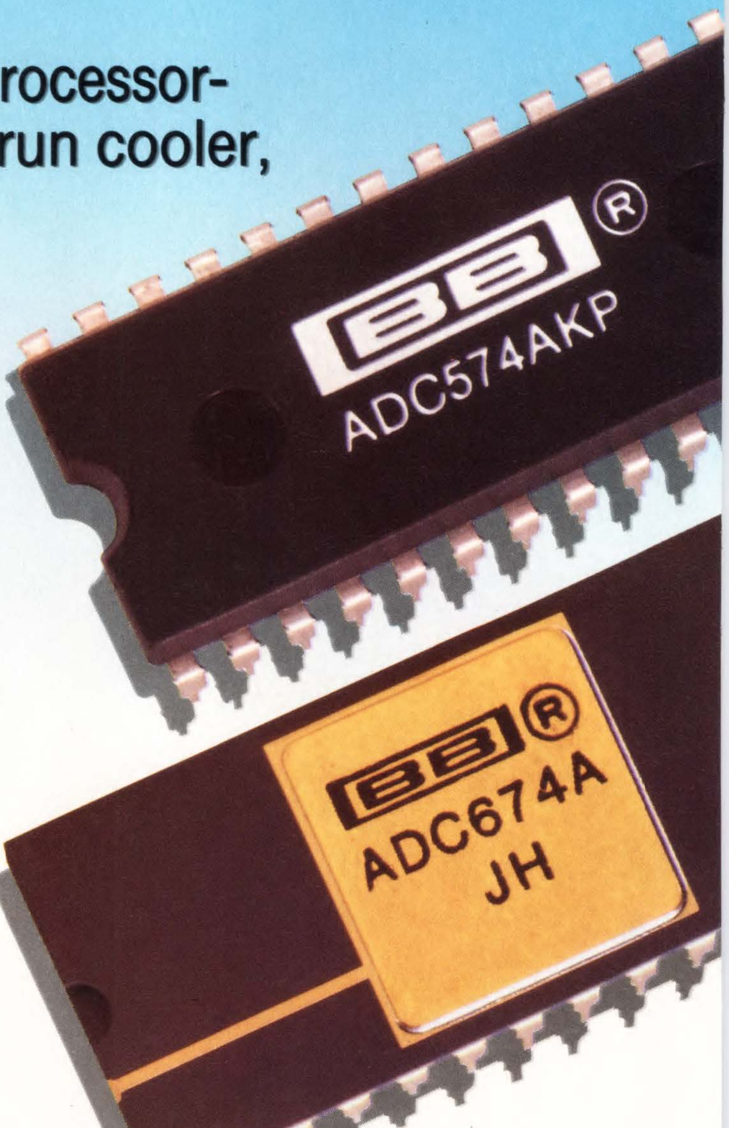

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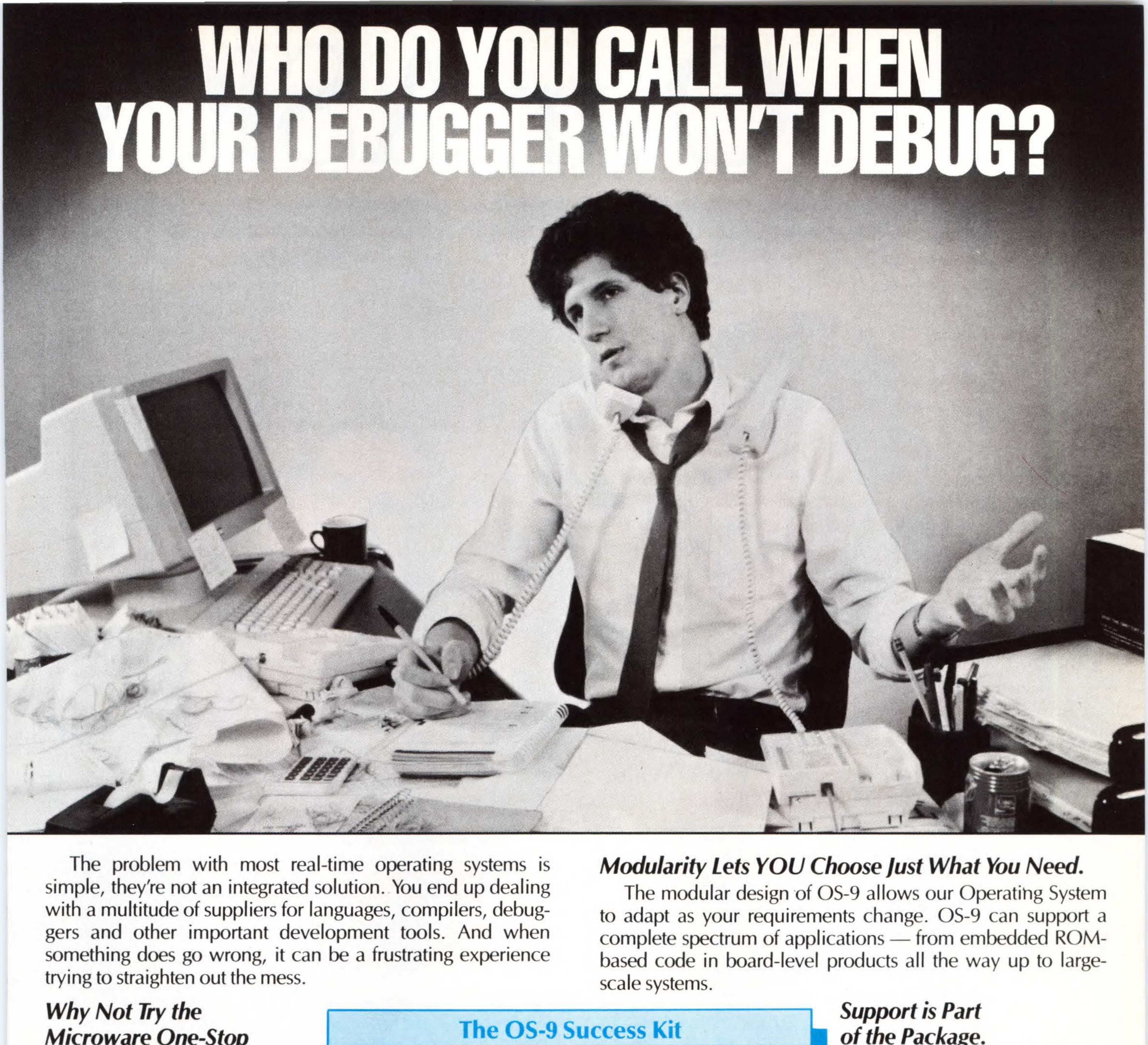

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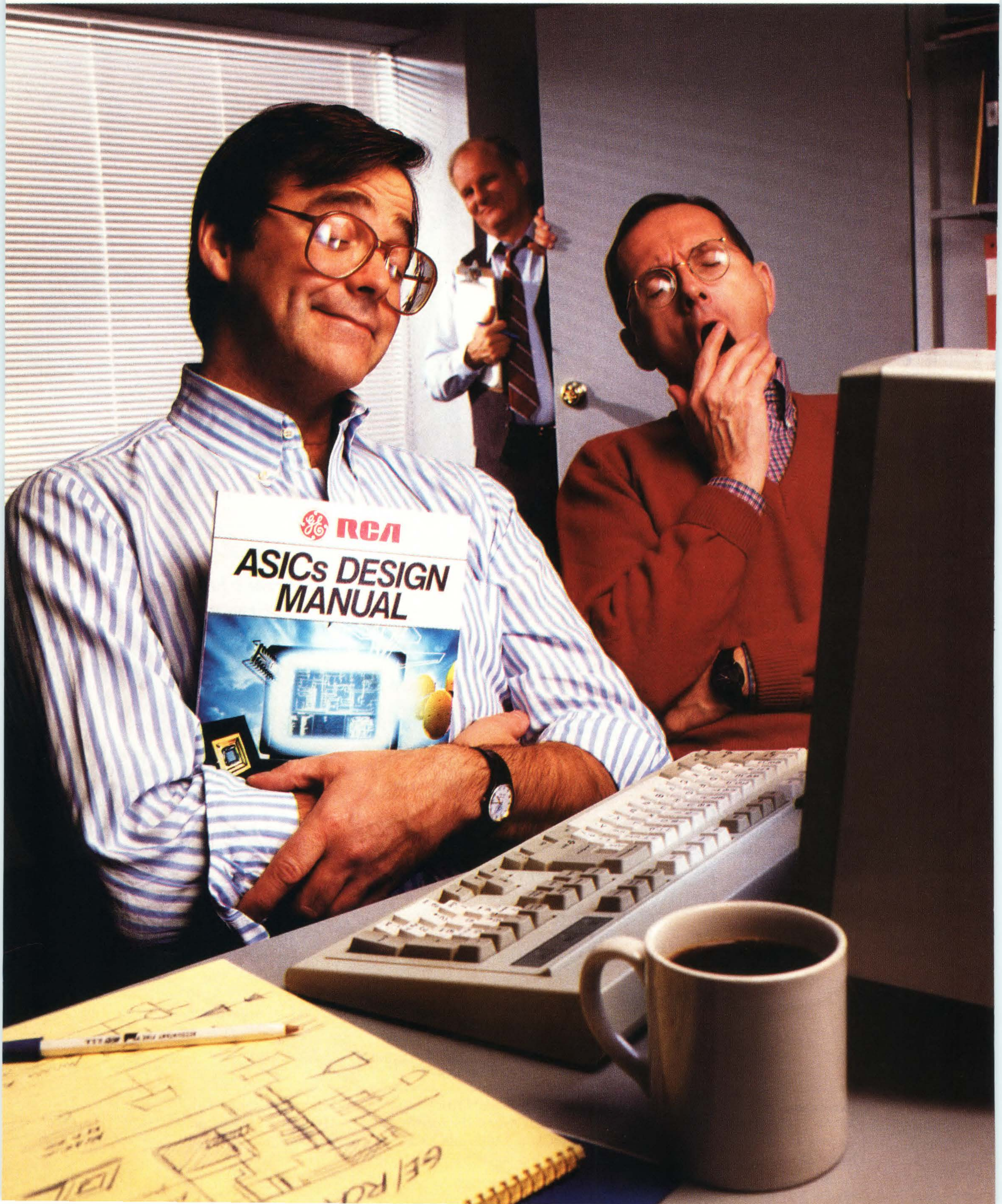

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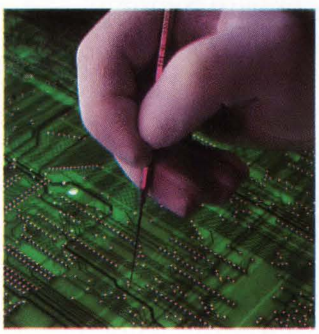

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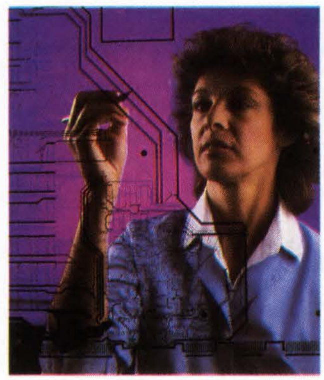

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DESIGNER'S GUIDE

PC-based analog pc-board design Part 1

Choosing a PC-based CAD package requires careful scrutiny

Designing analog pc boards poses special problems that some CAD tools don't handle well. Part 1 of this 2-part series helps you to evaluate PC-based, pc-board design tools and presents a checklist of features desirable for analog board design. Part 2 will offer some techniques for circumventing the analog deficiencies of PC-based software.

Kimberley F Quirk, *Engineering Services Group*

If you're a digital designer, you can buy inexpensive software that runs on inexpensive hardware and that will automatically place and route your multilayer board without requiring you to think much about the process. Unfortunately, most companies have been writing CAD software with *only* the digital user in mind; consequently, many of the problems associated with analog board design have not yet reaped the benefits of computerization.

Before the introduction of computer-aided design tools, all the artwork required for pc boards was created manually with tape on Mylar. As digital circuitry became more and more complex, it seemed only natural to make computers create this artwork because of their ability to do tedious work fast and accurately. Although expensive at first, hardware and software for CAD have now come within the financial grasp of small companies and individuals and have made a digital designer's task relatively easy.

The same does not hold true for an analog designer, however, and even for a digital designer, complications may still arise. For instance, what happens if an engineer slips something new into the circuit? A little ECL, say, or a high-frequency oscillator? What about an input A/D converter, a telephone-line interface, or RF circuitry? In these cases, the board design will require some thought. Certain incoming traces may require shielding, and extra grounds may prove necessary. Perhaps a full ground plane may need to be added—or even a split ground plane (distinct ground planes for analog and digital residing on the same layer).

For the purposes of this article, "digital" will refer to circuits that operate at relatively slow speeds: less than 20 MHz. TTL circuits are typical examples. "Analog" will mean everything else. The reason for this simplified definition is that there are some analog concerns in almost any circuit today. Speeding up a digital circuit or trying to meet FCC requirements may mandate more complicated grounding or guarding techniques, which once were needed only for microvolt-level analog signals.

When evaluating any software package, it's imperative to first determine your own needs and priorities. Don't let a salesperson make these decisions for you

Speeding up a digital circuit may force you to consider better grounding or guarding techniques, which once were needed only for microvolt-level analog signals.

because most salespeople don't have a strong enough background in analog board design. Furthermore, demonstrations and sales literature usually don't paint an accurate picture of a system's analog capabilities. Some sales reps will promise you the world without fully understanding what you need. When you get the system in house, it may be incapable of generating the artwork you desire. On the other hand, you may find software vendors who don't understand the full capabilities of their product. A vendor may say that its software can't create unusual ground planes, yet, if you get a chance to work with the program, you may discover that you can make it do what you want without too much difficulty.

Until a much greater emphasis is placed on the needs of analog designers (including sales, marketing, and technical support), you should be wary of salespeople. Instead, try to find analog designers who use the software. Their comments will provide insight into a product's true capabilities and deficiencies.

Don't sacrifice features of digital software

The design packages traditionally used for digital design provide many valuable features that you shouldn't have to sacrifice because you want a package with an analog specialty. You shouldn't have to lower your standards or make too many tradeoffs to achieve the analog features you want. The **box,** "Software checklist for analog users" (pg 200), should help you ascertain which features you do or do not need and should ensure that you don't overlook any important capabilities. Although your personal preferences may diverge from items on this checklist, the list will serve as a starting point for your evaluation. And you can modify it to suit your own practices.

One digital option that you should probably avoid is the autorouter. An autorouter can be helpful on some digital boards or some sections of boards, but it's not very adept when it comes to analog designs. Don't let someone talk you into this option unless you're convinced you have enough digital circuitry on the board to make it worthwhile.

One of the first limitations you'll find when you begin evaluating software is the limit on the number of parts that you can include in a design. The reason is that analog boards require many more physical parts than digital ones. You can cram five or six discrete parts into the space occupied by one 14-pin IC and many more into the space of a 48-pin microprocessor. Thus, you may very well run into memory limitations on an analog board much sooner than you would on a digital one. However, most analog boards don't need nearly as many physical connections per component as a digital board.

If you plan to design only small- to medium-size boards, you may never encounter problems with memory limitations. However, if you plan to design any large boards at all, make sure the software can make use of extended or expanded memory.

Another possibility is to break the board into sections that you can recombine before or during photoplotting. It's improbable that you would even consider such a procedure for a digital board; usually many traces run between any two areas. On an analog board, though, you may find it very easy to determine a separation line across which only a few signals pass.

You may want drawing/copying capabilities

Drawing capabilities may be very important to you if you like interesting silkscreen shapes or if you need strangely shaped pads. A freehand-drawing feature, for instance, allows you to define a pad in the shape of a strip-line inductor so that you can assign to it the attributes of a physical part. You could then store this part in the library and treat it like all the other components for parts-list generation and design-rule checking.

Most pc-board programs give you a choice of pad shapes but don't allow you to define them. Make sure that all the pad shapes you want to use are available in the software package you have in mind.

You may also be interested in area-copying capabilities. Area-copying capabilities permit you to define an area of parts and traces to be copied as a group rather than as individual items. For example, having laid out 1 of 15 A/D channels, you could save a good deal of time by copying the entire channel 14 times. Be aware that you'd almost certainly have to manually change the reference designators and signal names in each new copy of the channel to ensure correct information in the net lists and the design-rule checks.

Some aspects of analog design require that you measure a trace length or width. Even in a digital design, situations may arise when you want to know the distance between two components. It's a great help if the software provides a measure of absolute distance or relative X and Y coordinates.

Unlike IC chips, discrete analog parts (inductors, transformers, capacitors) do not use standard 100-mil spacing between leads. A basic rule for analog CAD software is that it must allow you to specify grid spacing with a resolution as fine as 1 mil (or better), and this rule applies to the definition of parts as well as the routing of traces. To design some of the most common connectors, a 1-or 2-mil grid is necessary.

In addition, you should have the ability to define trace widths to the same resolution as the grid. Some inexpensive software packages give you a choice of only five or six different widths. For instance, my personal preference is to use 20-mil traces for many analog signals, but 8, 12, 50, 80, 100, 150, and even 200 mils are necessary for some applications. Defining an inductor or coupling coils in etch would require a custom trace width as well. **Fig 1** shows an inductive trace between resistors R1 and R2. A good rule of thumb is to use a width of 8 to 12 mils for digital signals. **Fig 2** shows a 12-mil trace between pins 5 and 6 of U2 (which has standard 60-mil pads), as well as two 8-mil traces between pins 7 and 8 of the same chip.

You may also need to be able to change the width of a trace in midstream. To illustrate this, **Fig 2** shows a 50-mil trace that narrows down to 20 mils in order to pass between R1 and R2 on the way to U3.

Finally, be sure you can create whatever angles you'll need when routing a trace. Some systems may allow only 90° and 45° angles, whereas others will allow any angle. If most of your traces will be routed along 45° angles, verify that the system will allow a default setting of 45 so you don't have to set it for each trace—or worse, guess by looking at it.

For analog engineers, probably the most important characteristic of a CAD software package is its ability to handle grounding and guarding signals. You have a choice of three types of grounding schemes: creating copper areas of any size or shape; creating full-layer ground planes that also include signal traces; and creating customized or split ground planes.

The capability to add copper areas is vital if you like (or need) to fill in open spaces with as much ground as possible after routing the signal traces. You may also want to guard sensitive signals by running ground traces on both sides of each such signal trace. **Fig 1** shows an example of copper added in a user-defined shape as well as a guard around the signal coming off Q2's pin 3.

Some CAD packages allow only certain shapes of copper; other packages do not have the ability to add extra copper at all. With many packages, you'll be able to add arbitrary ground shapes but you'll be limited as to the amount of copper you can lay down. In digital designs, you don't usually need to add much extra copper, so software vendors don't allocate much memory for this purpose. Every software package has made tradeoffs regarding the way it allocates a limited amount of memory to various functions. Techniques to circumvent memory limitations may exist, but be aware that you might run into problems if you tend to reinforce ground or power traces and to add extra copper for shielding.

Creating power and ground planes is important in digital designs as well as analog—they are usually the first things a digital engineer adds when a design ex-

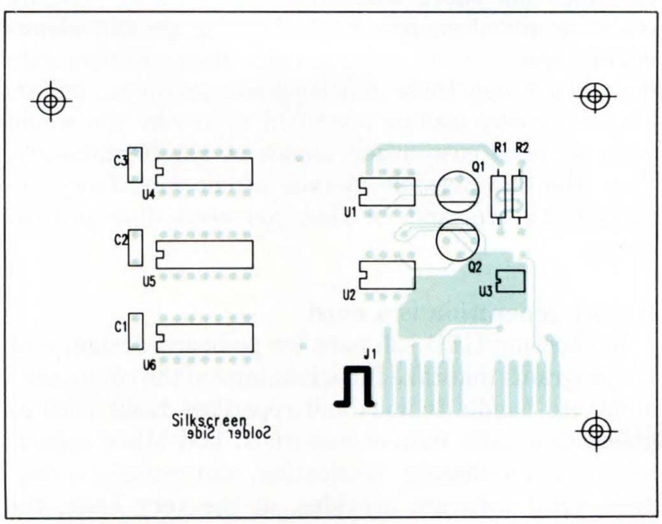

***Fig 1—Grounded copper areas and guarded traces** can help to eliminate noise problems in analog circuits.*

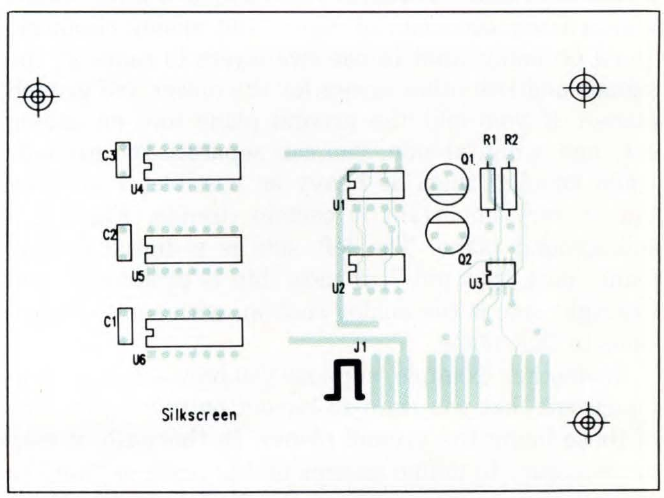

***Fig 2—Analog circuits usually require** a greater variety of trace widths than digital circuits. The trace from the top end of R1 was narrowed to pass between the pads for R1 and R2.*

Don't let a salesperson determine your needs and priorities: Most salespeople don't have a strong enough background in analog board design.

ceeds two layers. For this reason, some of the good, inexpensive software packages today can handle a simple ground plane quite well. Other, less-desirable types of software packages require you to define new library parts that include thermal relief pads for each ground- or power-plane level. If the design uses standard digital chips, you can rely on a standard pin (7, 8, or 10, for example) being connected to a ground plane, and the diagonally opposite pin (14, 16, or 20) being connected to a power plane. But this approach doesn't take into account your standard resistor. You may find that every analog part you create must come in at least two versions—one with thermal pads and one without. This requirement also implies that you must modify (or at least inspect) a schematic-capture-program net list to be sure that it calls out the correct version of the resistor in question.

Oftentimes, an analog design will have only two layers, one of which must be the ground plane. In such a situation, you may discover that it's necessary to run signal traces on the ground plane as well. Ask the software vendor's advice on how you can achieve this—and don't be too surprised if no one completely understands what you're talking about. To the best of this author's knowledge, no software packages are available that can easily incorporate signals on ground planes.

Even if the vendor doesn't know how to run signals on ground planes, however, you may be still able to do so by persevering. It just takes some work and planning.

In a number of situations, customizing a ground plane is critical. Perhaps you have a 4-layer board with a fairly even mix of digital and analog circuitry. You'd probably want to use two layers to route all the signals and two other layers for the power and ground planes. If you split the ground plane into an analog side and a digital side, you can separate the grounds while keeping them as heavy as possible, something that is very important in certain circuits. **Fig 3** is a split-ground plane. The left side is a digital ground plane (note that pin 7 of each chip is grounded), and the right side is the analog section, with some connections to that plane.

As another example, suppose you have a mostly analog circuit that you want to lay out on two layers (one of these being the ground plane). In this case, it may be necessary to define an area on the plane as "not the ground plane" where you run the digital signals. Many different combinations of ground planes with and without signals may be important to you, depending on your application. Bear these requirements in mind when evaluating a software package.

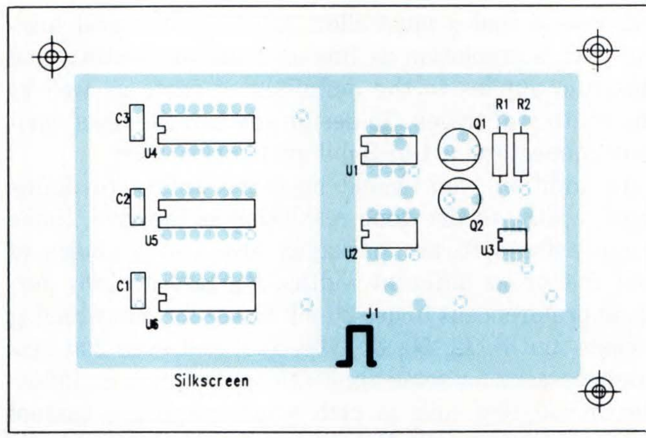

***Fig 3—You should be able to create** a split ground plane that isolates the analog and digital grounds and provides maximum grounding capabilities.*

If you do decide that you want or need custom planes, you'll need to be able to check your work before committing it to photoplotting or artwork generation. At present, you won't find any software package that will let you see a negative image, or a composite negative and positive image, on the screen. Most packages will let you print or plot each layer individually as positive images, however.

Many vendors provide error-checking facilities with their packages—that is, a way to check the spacing between pads and traces as well as a way to match net-list input to net-list output. Nevertheless, these packages fall short when it comes to automatically checking added copper or to checking ground planes against traces, pads, and net lists. Most software vendors do not view these deficiencies as problems, either. They may very well be mystified as to why you would want or need customized planes at all. Realistically, then, the only feasible method of checking fancy designs is by eye, and for that you need time and patience.

Report generation is a must

In choosing CAD software for pc-board design, look for programs that take full advantage of the computer's ability to handle tedious and repetitive tasks such as generating lists, bills of materials, and other reports useful for purchasing, fabrication, and manufacturing. Most CAD software provides, at the very least, the ability to generate a net list and a parts list from a completed board design. Other helpful reporting fea-

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CIRCLE NO 85

An autorouter can be helpful on digital boards, but it doesn't handle analog designs very well.

Software checklist for analog users

Analog Concerns	*General Concerns*
☑ **Memory limitations**	☑ **Input**
__ Number of parts	__ Is modification of net list required before it can be used?
__ Amount of free standing copper	☑ **Reporting features**
__ User-allocatable memory	__ Net list from pc board
__ Expandable memory	__ Parts list/Bill of materials
☑ **Drawing and copying facilities**	☑ **Fabrication drawings**
__ Limited pad sizes	__ System statistics (memory usage)
__ Limited access to layering scheme	__ Change-order information
__ Copy, delete, rotate by area or individual parts	☑ **Output**
☑ **Relative X, Y positioning**	__ Dot-matrix printer
☑ **Trace and grid sizes**	__ Plotters
__ 1-mil grid for defining part shapes	__ Quality artwork plotting
__ 1-mil resolution for trace widths	__ Fab/drill drawings
☑ **Grounding**	__ Gerber files
__ 1-mil grid for laying down copper	__ Drill tape (Excellon compatible)
__ Any shape for copper grounds	☑ **Checking features**
__ Ease of creating ground planes	__ Schematic net list vs board net list
__ Signals on ground planes	__ Spacing checks
__ Split and custom ground planes	☑ **Other**
☑ **Routing**	__ Ease of interactive routing
__ Ability to change trace width in the middle of a route	__ Ease of parts placement
__ 45° corners	__ Modifying traces, parts, text
__ Rounded traces (no corners)	__ Library management
☑ **Checking**	__ User interface
__ Ground-plane-checking features	
__ Copper-to-trace checking	

tures relate to job statistics (equivalent ICs and board area, number of holes, number of vias, number of routed and unrouted traces), bills of materials, and ECOs (engineering change orders).

The program you choose should automatically generate fabrication, drilling, and photoplotting information in the appropriate formats. A computer can count holes faster and more accurately than a person can. If the program doesn't make it easy to get a hole-count or a table of hole sizes (for fabrication drawings), be wary. Many software packages can generate information in the Excellon drill format, which is becoming an industry-wide standard for transferring drill-size and hole-location information to fabrication houses. In the photoplotting domain, Gerber has defined a standard. Virtually every CAD software vendor offers this format, but it may cost extra.

Another task that computers do very well is determining the spacing between traces and pads. Find out what space-checking features the software package includes, especially if it has the analog features you want. Most packages have some means of telling you if traces are too close together or too close to a pad, but many have trouble determining whether space problems exist near copper grounds or guard traces.

Two particularly important characteristics to look for are the program's ability to check any areas of the board that are ordinary (mostly digital) and its ability to avoid crashing when it's checking the special analog sections. Obviously you don't want the program to blow up, lose data, or otherwise cease to function just because it is attempting to check an analog board or area. Ask yourself the following questions: What will the program do when it finds an error? Will it hang or abort, or will it continue to find other errors? How many errors is it willing to ignore?

Some checking programs die after too many errors, albeit many engineers wouldn't consider them to be

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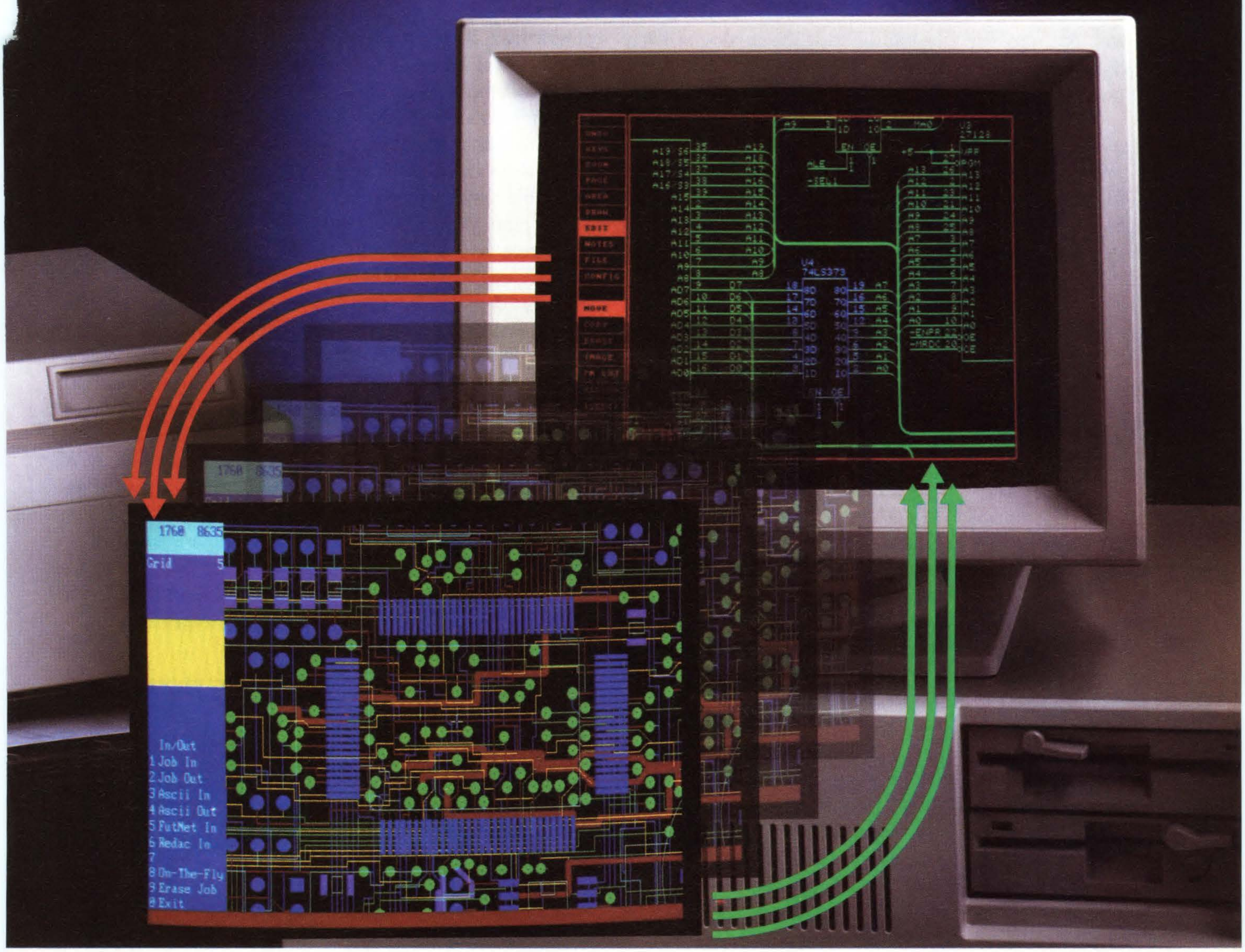

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CIRCLE NO 146

You may run into memory limitations much sooner on analog boards than on digital boards. Analog boards often require far more parts (though fewer connections).

errors. You may have to hand-check the analog section of a board, but the program should perform a complete and automatic check of any digital sections.

Should engineers design their own boards?

In today's world, it is very important for design engineers to get involved in the layout process to some degree. Most layout houses do not employ people who can really understand all of the complex issues affecting analog and RF circuits. When an outside service bureau does the work, you'll often find, to your dismay, that large parts of the design have to be redone.

In most instances, a service bureau takes your schematic, along with some instructions, and returns to you a finished layout. You may then have to remind them—again—that they must keep the 80-MHz signal away from the sensitive analog input, and they may then charge you extra to perform the modification.

A possible remedy is to educate the pc-board designers as to the electronics and potential parasitics of the boards they are designing. Unfortunately, designers aren't telepathic and often aren't even engineers. In most cases, only the analog design engineer is familiar with the very detailed demands of a layout, and therefore it is the engineer who must become involved in the layout.

From this perspective, a circuit designer who can perform board layout is at a distinct advantage. Nevertheless, pc-board layout is a difficult discipline in its own right, and many believe that an engineer's time is better spent designing circuits than learning the art of pc-board design. As is true when mastering any new software program of great complexity, you have to devote a significant amount of time to climbing the learning curve.

Think about some possible solutions

One way to work with a service bureau is to set up comparable hardware and software in the engineering facility (assuming it's not too expensive), thereby allowing some engineer involvement in the layout process. The service bureau would install and set up the system, making sure that the interfaces work and that defaults are set to the same standards they use. The design engineers could then learn enough to lay out parts to their individual specifications and to modify the work done by the service bureau's draftsmen.

Such an arrangement would, in all likelihood, be the first step toward bringing the entire process in house. Although it would require hardware and software expenditures, it might not necessitate the hiring of someone full time to run the system.

The ultimate solution would be to bring a computer system in house and to hire someone to run it. Unless there's enough work to keep the system manager and the system constantly busy, however, most people will view this arrangement as too costly.

In some ways, these inexpensive pc-board design programs are giving the world the false impression that all engineers should have board-design software on their desks. The low cost of such systems doesn't imply simplicity, nor does it imply that engineers should, in fact, be designing their own boards. On the other hand, many analog engineers end up doing their own parts placement and much of the layout, so they definitely need some basic layout experience. As time goes on, more vendors will recognize the number of analog users and how best to address the shortcomings of the currently available pc-board-layout software. Until that time, engineers need to learn how to overcome the deficiencies of those products that are available. The conclusion of this 2-part series will provide some tips on how to deal with these imperfections.

EDN

Author's biography

Kimberley F Quirk is founder and president of Engineering Services Group in Westford, MA, a company that specializes in analog and RF pc-board design and consulting. Kim holds an AB from Dartmouth College and a BSEE and an MSEE from Thayer School of Engineering at Dartmouth College. In her spare time she enjoys tennis, racquetball, and music (both electronic and acoustic).

Article Interest Quotient (Circle One)
High 485 Medium 486 Low 487


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Test Requirements
Document # 8-704
Analog Control Module
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4 WKS.
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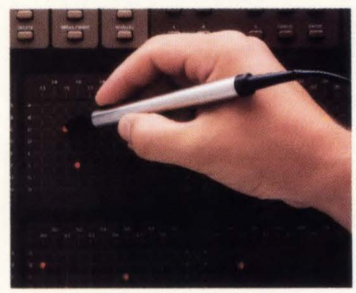

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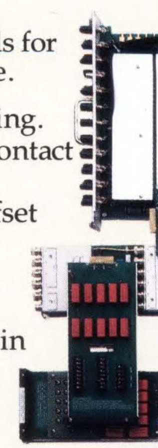
Here's your choice from the 21 switching cards for either the Model 705 or Model 706 mainframe.



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SHORTEN YOUR DESIGN TIME

With the Models 705 and 706, you can pretest switch set-ups using the manual operating or the 706's Inspect modes. You can mix and match cards for the most efficient topologies. And, with the 706 memory, you can store up to 75 matrix set-ups.

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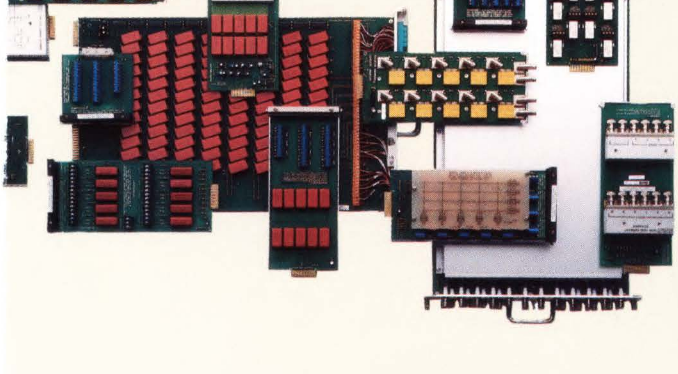
With the 705 and 706, you can switch channels at rates up to 100 per second. You can also control testing without tying up a controller by using the mainframe's own interval timer, hardware triggers, and external digital I/O lines.



You can generate precise stimuli to the DUT (Device-Under-Test) with Keithley DC Voltage and Current Sources which provide high resolution over wide dynamic ranges (50μV-100V and 0.5pA-10A) with 0.05% basic accuracy. They also sink power (up to 100W) as an active load. You can program 100 memory steps with output level, compliance, and step time duration.

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When you work with Keithley, you have one source for support — on the hardware, software, interfaces, and test fixtures. And, if ever needed, we offer a 24-hour Replacement Loaner program.

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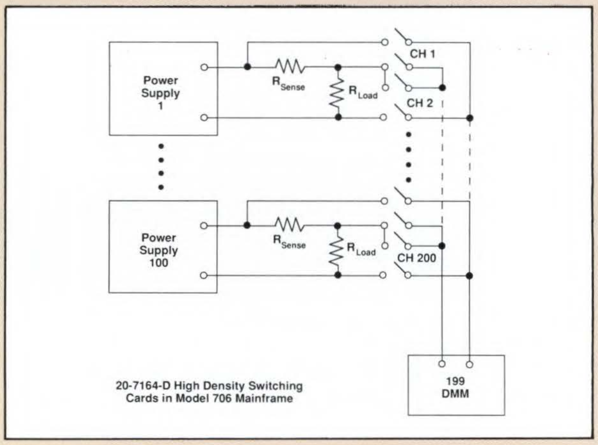
CIRCLE NO 86

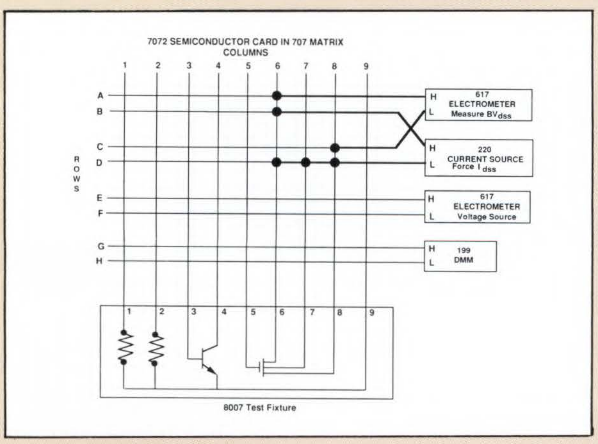
Some Typical Applications

Burn-in Testing — Economical and Reliable High Density Scanning

Keithley has the capacity for high density switching which is essential when large quantities of devices must be monitored over long time periods. The diagram illustrates a configuration that provides 200 channels in one mainframe. Such high densities offer the lowest cost per channel; a major consideration in large systems.

When maximum system reliability is required, we recommend mercury-wetted relays (long life / bounce-free contacts). Reliability is further enhanced and labor costs are reduced by the use of standard multi-pin connectors which mate with Keithley accessory cables.





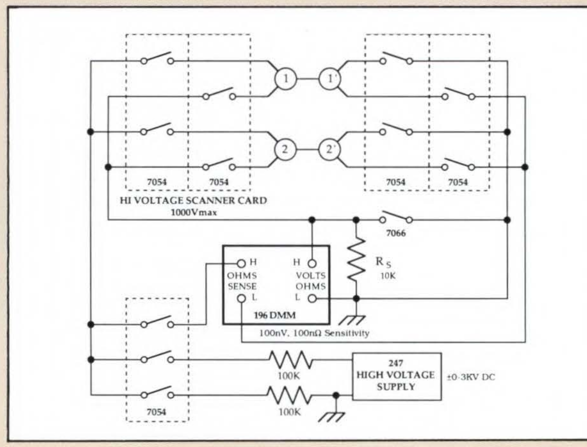
IC Testing — Cost-effective Test System Modification Using a Matrix

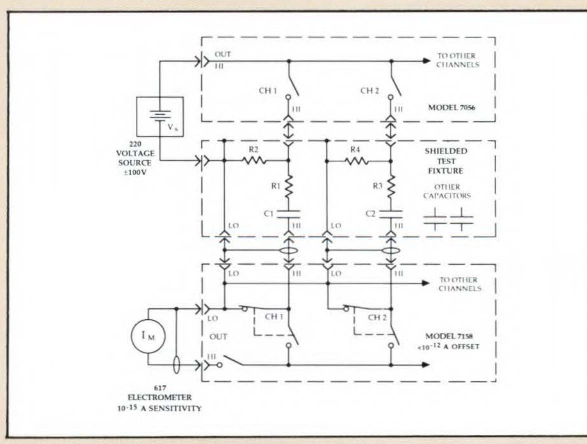
Fast test development is the name of the game where requirements change daily. That's where the flexibility of a matrix switching system is most advantageous. The Model 707's programming light pen and crosspoint display assure system designs which can be adapted quickly, visually verified, and transferred to the computer for tomorrow's run.

Keithley test fixtures and cables also enhance quick adaptability by providing convenient interfaces to DIP packages with up to 48 pins.

Insulation / Contact Resistance Testing — Low Resistance Measurement and High Resistance Measurement in One Economical System

A low resistance system needs switching cards with low thermal offsets and a micro-ohmmeter; while a high resistance system has entirely different requirements; low offset current switching cards and a picoammeter. As independent systems, those approaches are good solutions. However, the diagram shows one innovative, economical method of testing both parameters in one system. Four-wire switching eliminates errors in the low resistance measurements, while the high voltage source generates sufficient leakage current for measurement of a suitable voltage by a DMM.





Capacitor Leakage Current Testing — Maximizing Speed and Throughput in a Sensitive Measurement System

Speed and throughput do not have to be sacrificed to make good low level measurements. You cannot neglect shielding, low offset current switching, and measurement time necessary for accurate pA-level capacitor leakage measurements. However, you can interleave the application of the soak voltage, the leakage current measurement, and the device handler loading for the highest throughput.

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PMA–020

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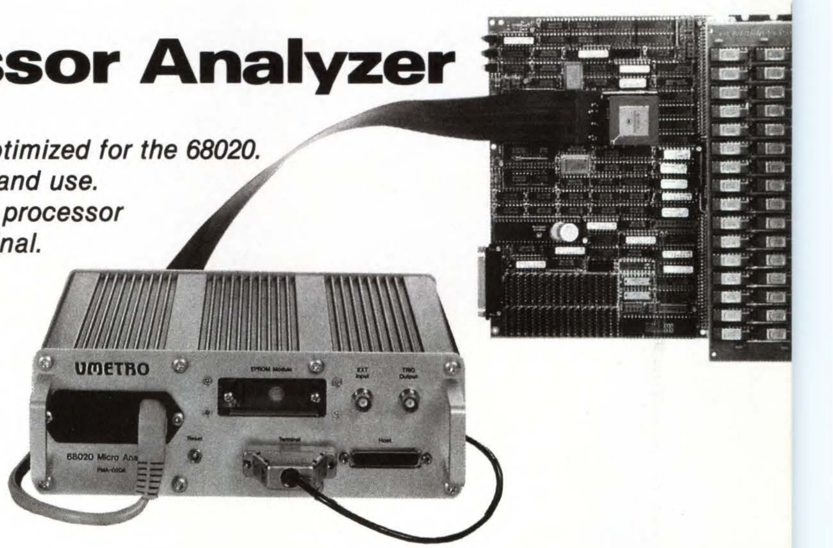

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Logic State analysis

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- Disassembler for 68020 program code.
- Powerful triggers and store qualifiers, Trig Output signal.
- Powerful search in trace memory.

```
                    68020 PROGRAM TRACE. STORED ALL CYCLES

LINE !  ADDRESS   DATA                IPL MODE INSTRUCTION
------!--------------------------------------------------------------------
  32 !  FF0003D8  0C8000000001         1  SP   CMPI.L #$1,D0
  33 !  FF0003DE  66000008             1  SP   BNE.W $FF0003E8
  34 !  FF0003E2  ........             1  SP   --- Cache hit ---
  35 !  FF0003E8  ........             1  SP   --- Cache hit ---
  35 !  FF0003EA  60000006             1  SP   BRA.W $FF0003F2
  36 !  FF0003EE  60000002             1  SP   BRA.W $FF0003F2
  37 !  FF0003F2  4CEE2000FFFC         1  SP   MOVEM.L -$4(A6),A5
  39 !  FF0003F8  4E5E                 1  SP   UNLK A6
  39 !  FF0003FA  4E75                 4  SP   RTS
  42 !  FF0003FC  4E56FFF4             4  SP   LINK A6,#-$C
  47 !  FF00041C  4A80                 4  SP   TST.L D0
  47 !  FF00041E  66000006             4  SP   BNE.W $FF000426
  48 !                                 4  CPU  IACK on level  4 (Vector 108)
  49 !  FF000426  1E14                 4  SP   MOVE.B (A4),D7
  50 !  FF000414  00034EB9             4  SP   ORI.B #$B9,D3
  51 !  FF000418  FF00                 4  SP   DC.W

Scroll:‹,›,+,-  Group:1,2  Jump:J  Mode (with/WITHOUT data):M  Print:^P  Quit:Q
Add start mark:A  Remove start mark:R
```

Performance analysis

- Address distribution of eigth user defined ranges.
- Cache Hit Rate Indication, total and distributed over eigth address ranges.
- Interrupt levels distribution.

```
************  V M E T R O  68020  MICRO ANALYZER     ACTIVITY MODE  ***********

Trig position    : START OF TRACE
Store qualifier  : NONE
                                                 Total # of samples :  20480
                                                 Activity  mode     :  CACHE

INSIDE  ADDRESS WINDOW (00000000,FFFFFFFF)             DATA D31-D00 : XXXXXXXX

Total Cache Hit Rate:  66% *********************************  .    .    .    .

0: 00000000-1FFFFFFF  12% ******  .    .    .    .    .    .    .    .    .
1: 20000000-3FFFFFFF   0%    .    .    .    .    .    .    .    .    .    .
2: 40000000-5FFFFFFF   0%    .    .    .    .    .    .    .    .    .    .
3: 60000000-7FFFFFFF  15% *******  .    .    .    .    .    .    .    .    .
4: 80000000-9FFFFFFF   0%    .    .    .    .    .    .    .    .    .    .
5: A0000000-BFFFFFFF  25% ************  .    .    .    .    .    .    .    .
6: C0000000-DFFFFFFF  14% *******  .    .    .    .    .    .    .    .    .
7: E0000000-FFFFFFFF   0%    .    .    .    .    .    .    .    .    .    .

PMA: ‹Command Line›
```

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CIRCLE NO 199

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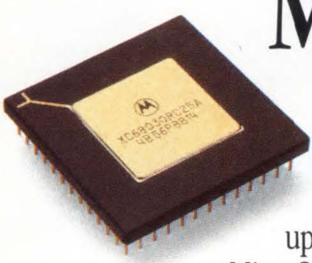

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Logic simulators exhibit different levels of device characterization

When selecting a logic simulator, you need to evaluate a number of criteria. One of the most important is the method that the simulator uses to model devices and to characterize their performance. You'll find many dramatically different approaches to device characterization.

Richard S Gogesch, *OrCAD Systems Corp*

By eliminating traditional breadboarding, logic simulation offers designers the potential to reduce design cycle time. Simulators possess significant differences, however, and you'd be well advised to understand and evaluate these differences before deciding upon a simulator for your application. The CAE requirements of any one engineering department vary as widely as do an engineer's preference for a particular design methodology, and simulation tools reflect these differences.

Categorize the types of logic simulators

You'll find several logic-simulator types available, but the different kinds are not mutually exclusive. A gate- or switch-level simulator can also employ functional and/or behavioral models. By convention, a simulator assumes the name of the lowest level at which it operates.

For strictly switch-level and gate-level simulators, the modeling of components takes the same form. A model is specified as the interconnection of the lowest level of primitives, the basic modeling elements within the simulator—n- and p-channel transistors in a switch-level simulator and NAND gates, NOR gates, and flip-flops in a gate-level simulator.

Some switch-level simulations have the capacity to yield a more detailed output than gate-level simulations at the expense of design capacity and simulation speed. Modeling a particular component requires a greater number of switch-level primitives than gate-level primitives, and therefore the capacity (simulation design size) of a switch-level simulator is less than that of its gate-level counterpart. Because more primitives are processed in a switch-level simulation, a switch-level simulation runs at a slower speed than that of a gate-level one.

Functional simulations, on the other hand, mimic the *function* of a primitive rather than the actual behavior of each of the constituent gates or transistors. A functional flip-flop, for instance, is modeled as the sum of each of its setup, hold, and propagation-delay times rather than a collection of transistors. The disadvantage of functional modeling is that there isn't a direct correlation of a model to its constituent gates.

Behavioral simulation allows the designer to simulate models created with a high-level programming language—Pascal or C, for example. The language may have built-in constructs for items such as delays, 3-state elements, and resistors, which ease the develop-

Timing-based simulators are useful for evaluating the speed of your design; non-timing-based simulators are better suited for fault simulation.

ment of simulation models. Using behavioral modeling gives you the capability to simulate very complex models, such as controllers and microprocessors, as long as the internal states of the model aren't important. If you need to use a microprocessor in your design, it is an arduous task to completely specify the μP from its constituent components. Functional simulators can suffer from the same drawback as behavioral simulators—there may not be a direct correlation between the model and the gates.

Because of the increasing need to simulate complex models as primitives within a larger circuit, both switch- and gate-level simulators are now capable of behavioral-language integration. Designers can use behavioral models to integrate complex, black-box functions into their designs while otherwise maintaining detailed simulation capability.

Timing-based simulator does verification

You also have a choice of either a timing or non-timing-based simulator. Nontiming-based simulators are primarily used for fault simulation. Typically, a design is fully verified with a timing-based simulator prior to the initiation of fault simulation; as a result, timing-based fault simulation is unnecessary.

If you want to try to find timing problems with a nontiming-based simulator, you can use a timing analyzer. If you opt for this approach, then logic verification is all that is required of the simulator. The disadvantage of using a separate timing analyzer is the additional step of performing the timing analysis each time the design changes.

Nontiming-based simulators are useful in evaluating circuit logic without regard to propagation delays. A zero-delay simulator, for instance, is one in which functional simulation is performed without timing verification. A unit-delay simulator, in contrast, assigns one time-unit of delay to each parameter with an assignable delay. The result is, again, a strict logic verification of the design without any timing analysis. The unit-delay simulator offers the advantage of being able to detect feedback that would be indistinguishable by the zero-delay simulator.

A primary advantage of timing-based simulators is that you can examine critical paths during simulation. Timing-based simulators fall into two categories: fixed timing and minimum/maximum timing. Fixed-timing-based simulators assign a selectable, fixed delay to each timing parameter that has an assignable delay. Minimum/maximum-timing-based simulators assign a range of delays to each parameter.

Considerable controversy surrounds the merits of minimum/maximum-timing-based simulators vs fixed. Advocates of minimum/maximum simulation contend that these types of simulators allow for a worst-case simulation whereas nonminimum/maximum simulations do not. Fixed-timing-based advocates argue that, with few exceptions, the usage of a maximum fixed delay is the worst-case scenario for synchronous designs. The argument continues that, for both types of simulators, asynchronous design is very difficult to simulate with any accuracy; as device manufacturers continue to reduce geometries, device characteristics change, thereby rendering previously used minimum/maximum delays inaccurate.

Component modeling differs quite a bit

The approach to component modeling among timing-based simulators is quite diverse, reflecting differences in modeling-language primitives and device characterization. You'll find the greatest variation in the area of primitive-based device modeling because modeling languages are developed to optimize the type of primitive used.

As explained earlier, a simulator may allow modeling only at the gate level. In such a case, all models are constructed as a combination of gates, buffers, and delay elements. In addition, you could use some delay elements to properly model parameters like setup and

TABLE 1—FLIP-FLOP CHARACTERIZATION PARAMETERS

LOW-TO-HIGH PROPAGATION DELAY FROM CLOCK TO Q_{OUT}
HIGH-TO-LOW PROPAGATION DELAY FROM CLOCK TO Q_{OUT}
SETUP TIME FROM D INPUT TO CLOCK SIGNAL
HOLD TIME FROM CLOCK SIGNAL TO D INPUT
MINIMUM PULSE WIDTH THAT CLOCK SIGNAL HAS TO BE LOW
MINIMUM PULSE WIDTH THAT CLOCK SIGNAL HAS TO BE HIGH
LOW-TO-HIGH PROPAGATION DELAY FROM RESET TO Q_{OUT}
HIGH-TO-LOW PROPAGATION DELAY FROM RESET TO Q_{OUT}
MINIMUM PULSE WIDTH OF RESET SIGNAL (ACTIVE STATE)
REMOVAL TIME OF ACTIVE-RESET SIGNAL TO CLOCK SIGNAL

hold times. This type of parameter modeling is a difficult and tedious process, so modeling languages often resemble programming languages, making it easier to define often-used collections of primitives as macro-definitions.

Functional simulators typically have a more diverse set of primitives than pure gate- or switch-level simulators. A functional simulator might have primitives for all types of gates and flip-flops, latches, and even ROM and RAM. Because such primitives are at a fairly high level, modeling languages are typically net list oriented. Functional models allow a designer to specify parameters such as setup and hold times directly without being burdened by the implementation of these characteristics.

Behavioral languages for all simulators are alike because they resemble high-level programming languages, but their implementation does differ. The Department of Defense has spearheaded a drive to create a standard for behavioral languages, which it calls VHDL (VHSIC hardware definition language), and which it has mandated for all future DoD designs. Most simulation vendors are adopting a subset of VHDL as their behavioral language. Anyone selecting a simulator capable of behavioral modeling should only choose a vendor who has made a commitment to some form of VHDL.

Device characterization is crucial

Device characterization involves the operational characteristics of the primitives. You'll find that it varies greatly from simulator to simulator. Consider a device as simple as a gate, which models propagation delay from high to low and low to high. If a signal is applied to an input for a period of time greater than the propagation delay of the device, all simulators will identically simulate the device. However, if a signal is applied to an input for a period of time that is less than the propagation delay of the device, different simulators will characterize it differently. Some simulators will ignore the input. Others will propagate a defined state equal to the glitch width. Another will analyze the device's high-to-low and low-to-high propagation delays and propagate the glitch as an undefined state for a period of time dictated by the analysis. Because this last approach most closely approximates the actual performance of a gate, it offers the best characterization. For the case of an open-collector gate with a high-to-low 5-nsec propagation delay and a low-to-high 50-nsec delay, an input glitch of 3 nsec would

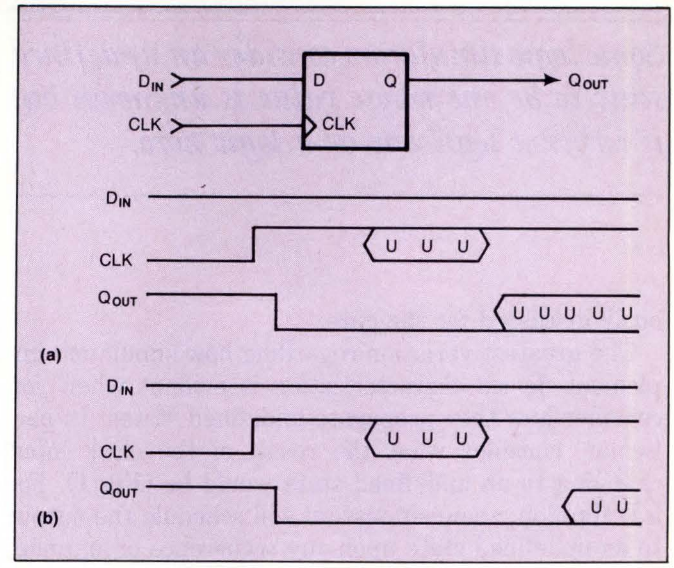

Fig 1—Simulators have different ways of propagating an undefined state. On simulator A, an unknown clock state causes the flip-flop's output to go undefined after a CLK-to-Q_{OUT} propagation delay. The same input condition on simulator B causes the flip-flop's output to become unknown only after the CLK signal, which has become undefined, has a potential rising edge.

have no effect on the output if the gate were in a low state. If, however, the gate was initially high, it would exhibit a glitch 5 nsec after the input spike.

How an undefined state applied at the input of a gate is propagated to the output of that gate also results in varying device characterizations. Most simulators will propagate an undefined input signal to the output only if the logical evaluation warrants the propagation, as when an AND gate has all its input signals (other than the undefined input) at a logic high level. The primary difference in undefined state propagation is the time delay used in processing. Some simulators immediately set the output to undefined. Others wait the minimum interval of the low-to-high or high-to-low delay before setting the output to undefined. Another type uses the average of the low-to-high and high-to-low delay. A fourth type utilizes either a high-to-low or low-to-high delay based on the present state of the output. A design engineer needs to assess the validity of these approaches in light of a particular application.

As you can see from the previous example of the gate, device characterizations can have dramatic differences. The parameters in **Table 1** represent what it takes to completely characterize a D flip-flop with asynchronous-reset capability. Most simulators characterize such a flip-flop with most of these parameters, but only a few employ *all*. Even simulators that model the same parameters differ widely in the implementation of the characterization, leading to some disparity in the output results.

In the event of a setup- or hold-time violation, most simulators will schedule the Q output to an undefined state. The time at which the Q output changes to the undefined state may vary from simulator to simulator because of design considerations similar to those previ-

Some logic simulators consider an undefined state to be one whose value is unknown but is either a logic one or a logic zero.

ously discussed for the gate.

The greatest variation regarding how simulators implement device characterization is evident when you consider how they propagate undefined states. In particular, consider what the result of the clock input changing to an undefined state would be **(Fig 1)**. For a D flip-flop, some simulators will schedule the output to an undefined state upon any occurrence of an undefined input applied to the clock signal present state of the clock input to determine if Q_{OUT} should be scheduled to an undefined state. Assuming that the flip-flop is a positive-edge device, these simulators will schedule Q_{OUT} to an undefined state only if the initial state of the clock signal is low, reasoning that this is the only time that the undefined state can generate a positive edge **(Fig 1b)**.

This example reflects a philosophical variation in simulators. The simulator of **Fig 1a** assumes that the undefined state could potentially be an oscillation. The simulator of **Fig 1b** reasons that an undefined state is either a low or a high level. Vendors of both kinds of simulators pose credible arguments as to why the approach they use is the correct one. In this particular case, both approaches have some validity. The difference in the two approaches is the time at which the output goes to an undefined state. The more conservative first case forces the output to an undefined state immediately. The second case requires a subsequent change of the clock input before it schedules the output to an undefined state. It is important to note that both methodologies achieve the same result—the detection of an error.

Benchmarks vary from vendor to vendor

The simulator world offers a number of good and not-so-good simulator products. Unfortunately, though many vendors discuss benchmarks, you'll find little consistency among these benchmarks. You should be aware of certain discrepancies while you are sifting through the performance data.

Most often, when simulator vendors discuss gates, they are referring to 2-input inverting gates, like NAND or NOR gates. However, some vendors mean single-input inverters when they talk of gates. It is critical, when comparing simulators, that the primitives being used for the benchmark are equivalent. A simulator benchmark using a single-input inverter as its gate definition would have a higher capacity and greater speed than would the same benchmark using a 2-input NAND gate.

Running a benchmark on different types of simulators for purposes of comparison is tricky. You should be aware that an incremental simulation, normally associated with a unit-delay simulator, will advance the simulator engine one time-unit after each evaluation pass through the simulator. An event-driven simulator, on the other hand, is one in which the simulator only processes the circuit at times that events, or changes, are scheduled. The simulator engine time is advanced from scheduled event to scheduled event, ignoring the circuit when no changes occur. Virtually all timing-based simulators are event driven.

The cause of most of the confusion among both vendors and purchasers of simulators are the two benchmarks, events/sec and gate evaluations/sec. Almost every vendor has its own way of measuring or defining these benchmarks, and benchmarks between vendors are often incompatible for purposes of comparison.

Events/sec is a measure of how many times per second the simulator can change the input to a gate and propagate the result to the output. Some simulators can post the change of a gate and reschedule the gate in one pass through the simulator; others require two passes to perform this function. It is important to recognize that simulators that can post and reschedule a gate can be tweaked to give unrealistic benchmark results.

Gate evaluations/sec is a measure of how quickly the simulator can evaluate the gates in the circuit when the inputs do not cause a change in the outputs.

Events/sec is a measure of performance for timing-based simulators, whereas gate evaluations/sec is useful for measuring the performance of nontiming-based simulators. It should be obvious that, because events/sec and gate evaluations/sec are different benchmarks, comparisons between the two are meaningless.

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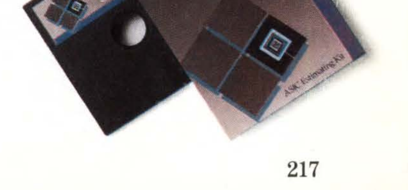

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CIRCLE NO 180

You'll find that how a simulator performs device characterization will vary greatly from product offering to product offering.

As you can see, device characterization is the most important variable when it comes to evaluating a logic simulator (for other important features, see **box,** "Don't forget to evaluate other logic-simulator characteristics"). A designer should first determine which parameters are characterized and then examine how they are characterized. If the simulator doesn't model the reset-to-clock-signal removal time, and it is important to your design, obviously the simulator won't meet your requirements. Nonetheless, because so many different types of simulators are available, it's probable that several of these offerings will meet the needs of any individual user. It should be the simulation vendor's responsibility to accurately describe the features of the product in question, but you'll be better off if you're knowledgeable about the specs in question (see **box,** "Benchmarks vary from vendor to vendor"). In addition, you, as a prospective buyer, should carefully scrutinize the product's capabilities and restrictions.

Author's biography

Richard S Gogesch is both director of simulation products for OrCAD Systems Corp (Hillsboro, OR) and president of Gogesch Micro Systems Inc (Thousand Oaks, CA). Rich obtained his BEEE and MSEE from Youngstown (Ohio) State University. When he can find some free time, Rich would like to become reacquainted with his boat and fishing rod.

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Don't forget to evaluate other logic-simulator characteristics

Once you've found a simulator that meets your device-characterization criteria, the task of choosing a logic simulator isn't over. Other important considerations remain. The relative importance of these features depends on the specific design and the preferences of the engineer or engineering group.

- Breakpoints—The ability to utilize breakpoints in a simulation is useful because the detection of a set of conditions is oftentimes valuable during design debugging.
- Hierarchy—Because the majority of ASIC designs are created hierarchically, you'll probably want a simulator that supports this design methodology.
- Mixed-mode simulator—If you need a simulator capable of evaluating both analog and digital logic within the same simulation run, you'll want what is called a mixed-mode simulator.
- Modeling language—Simulators that include a modeling language allow you to create devices not found in the vendor-supplied library.
- Platform support—Each simulator supports one or more platforms. If your engineering group is predisposed to a particular platform, either because they already have the necessary hardware in house or because of cost considerations, you'll gain an advantage if the simulator you decide upon also supports this hardware.
- PLD support—If PLDs are going to be used during the design process, an automated mechanism for the generation of simulation models should be in place. The only universal output from PLD compilers is a JEDEC (Joint Electron Device Engineering Council) file. In these situations, a utility that transforms the JEDEC fuse map to a timing-based simulation model is a requirement.
- Test vectors—Most organizations require test vectors in an ASCII text-file format. If this is true of your organization, you'll probably want a simulator that accepts ASCII text-file input and generates ASCII text-file output in test-vector format.
- User interface—Because first-time simulation users often have difficulty with many of the concepts and the implementation of simulation, some organizations require that both simulation and schematic-capture systems employ the same user interfaces to shorten the learning curve.

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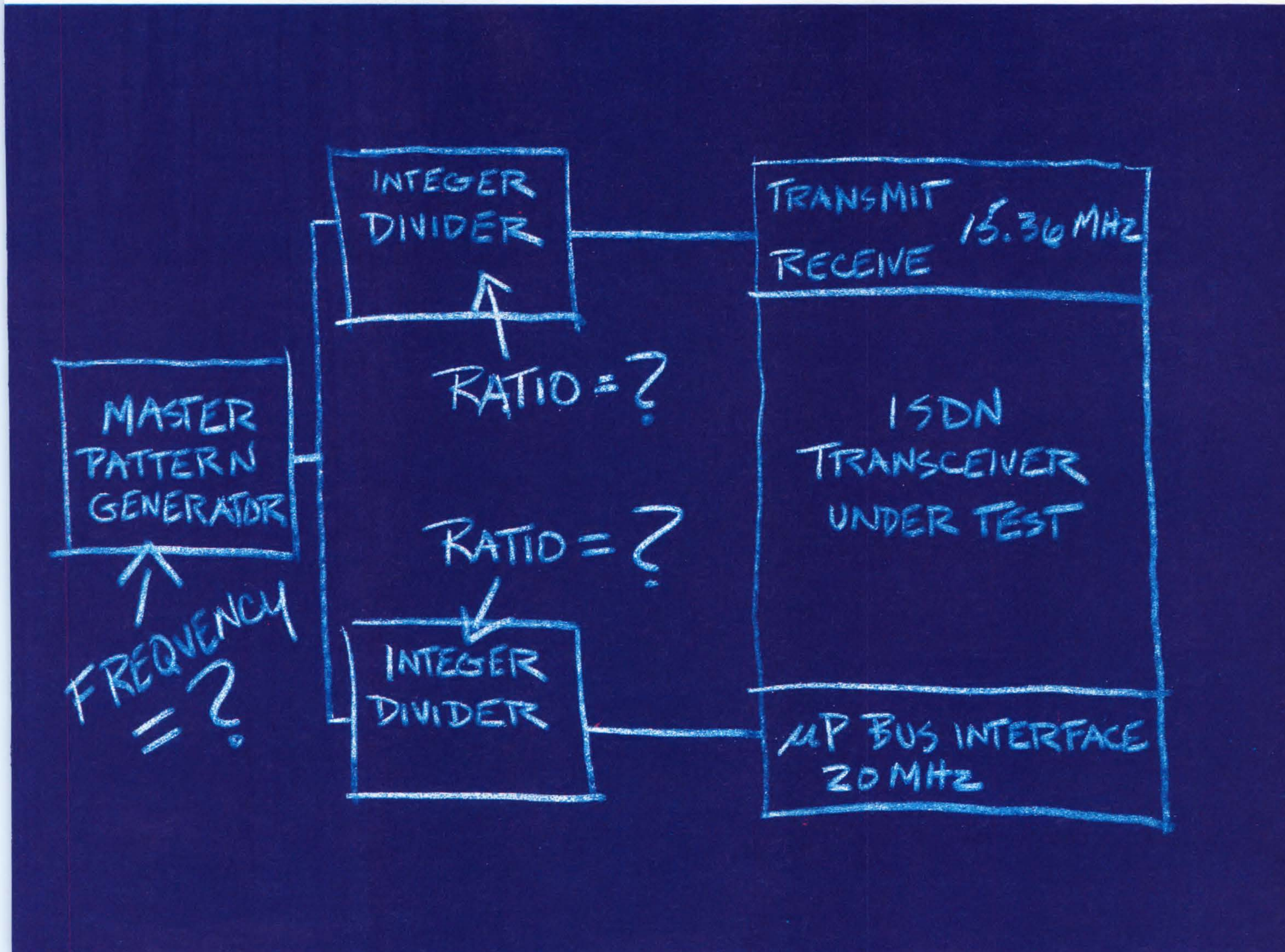

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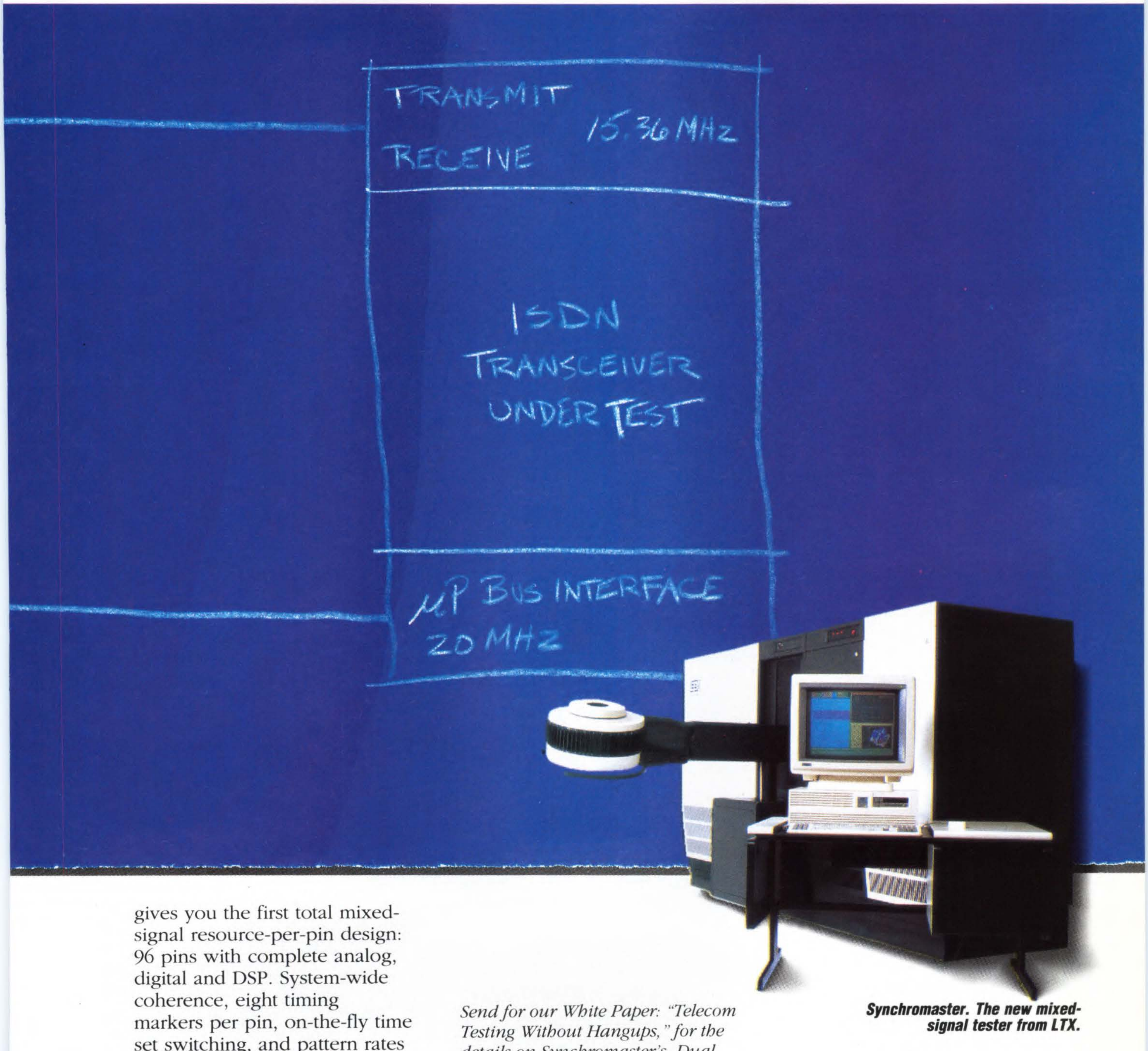

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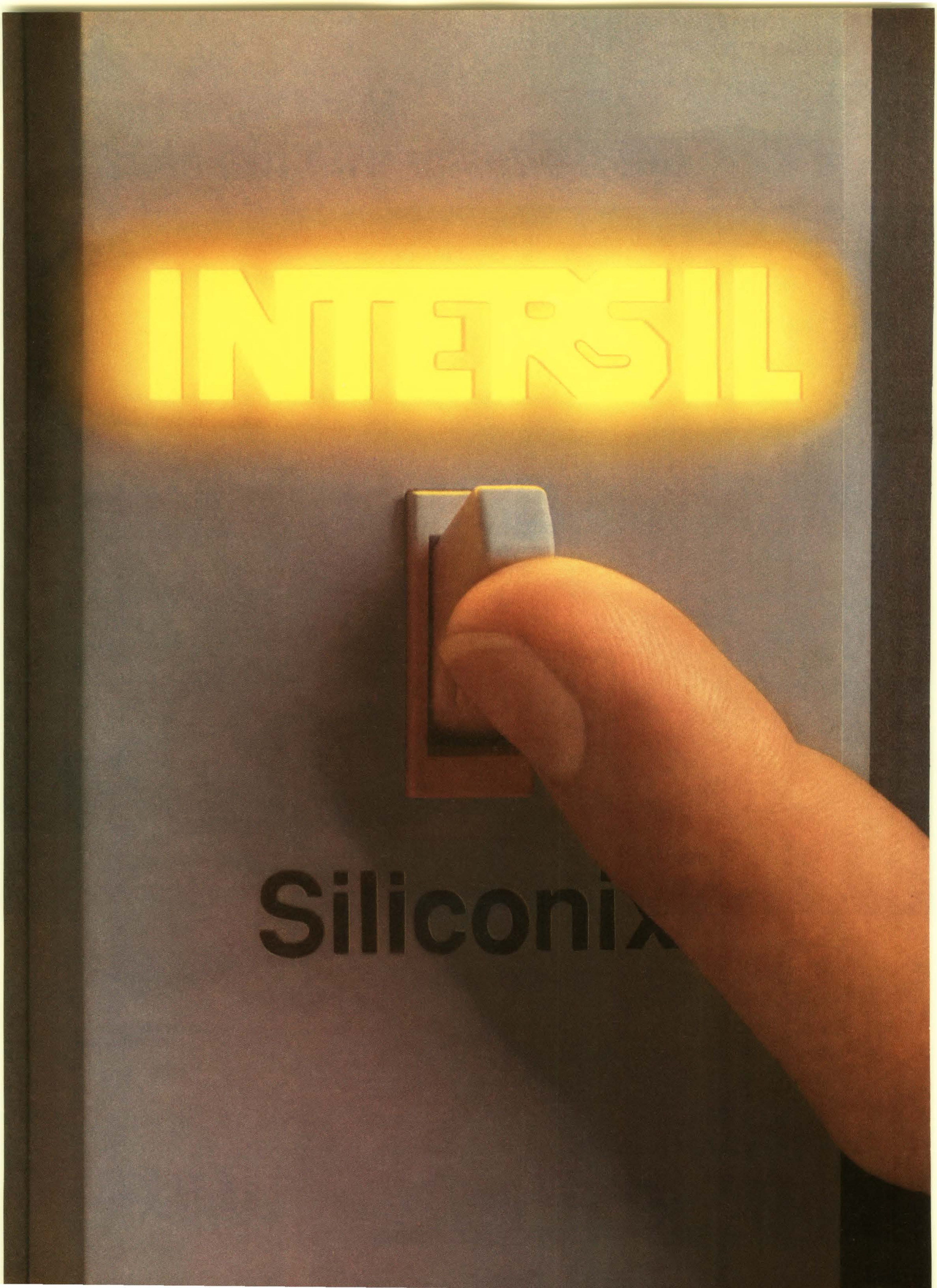

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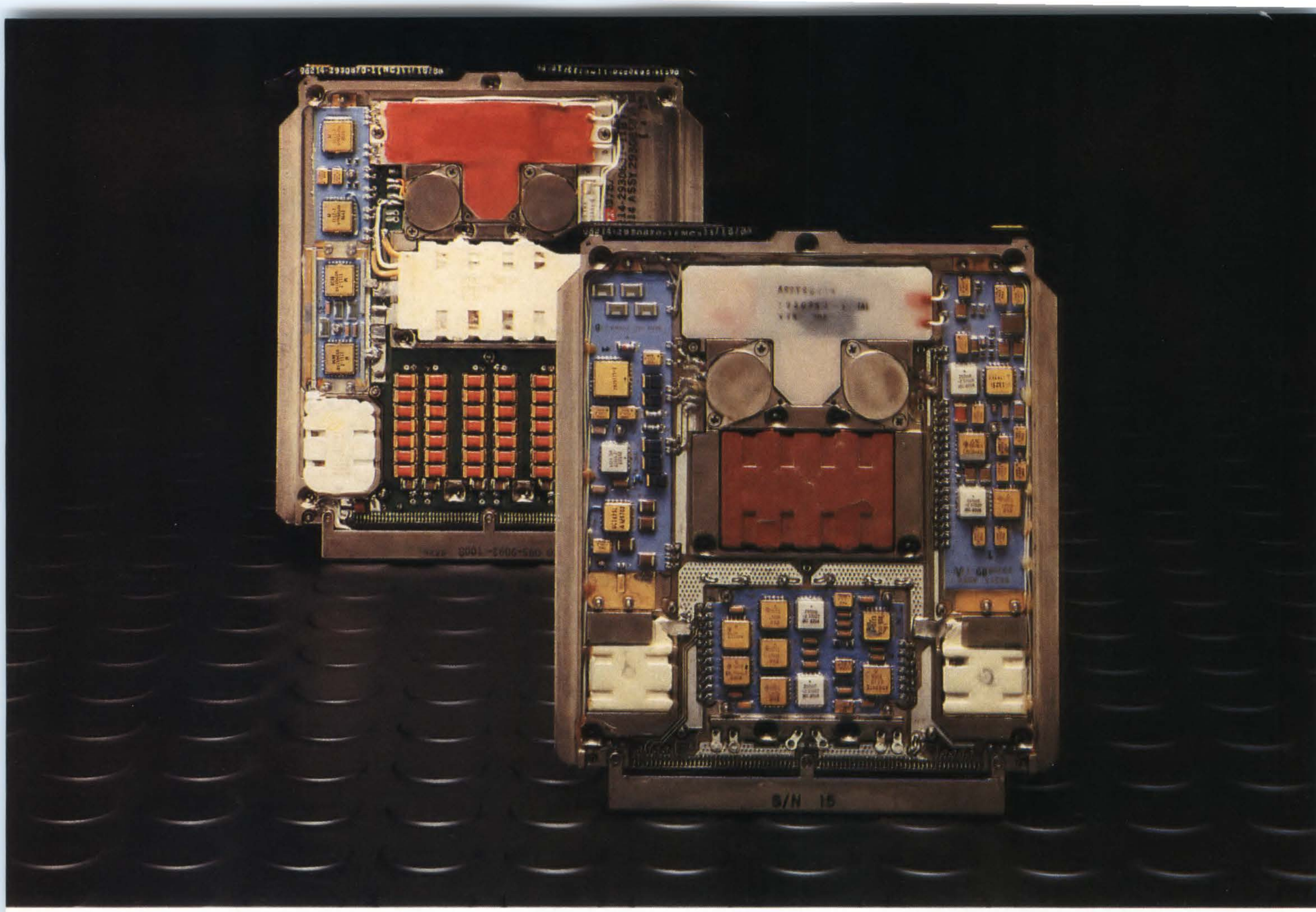
S/N 15

Design innovations make 1553 controller more flexible

Although MIL-STD-1553 bus controllers reduce overhead for communication over an interface, they can result in I/O boards that are hard to adapt to different systems and sometimes difficult to test. You can, however, go beyond the controllers' manufacturers' recommendations to make more versatile and testable boards.

Steven W Rider, *Westinghouse ILSD*

MIL-STD-1553 bus controllers provide an easy way to design an interface ranging in capability from a single-channel remote terminal, a dual-channel bus controller/monitor, or another remote terminal. To build a flexible, testable system that demands a minimum of system overhead, you should venture beyond the manufacturers' application recommendations. And to best understand how to improve your designs in these ways, you must also take a look at them within the context of particular applications.

These bus controllers incorporate two types of CPU interfaces: DPMA (dual-port memory access) or DMA (direct memory access). For the purposes of this article, the DDC Bus-66300/Bus-65600 is a DPMA chip set; the UTMC UT1553 Bus Controller/Remote Terminal is a DMA device. (Although both controllers offer DMA and DPMA capabilities, the UTMC UT1553 example discussed here uses only the chip's DMA mode because its DPMA mode does not handle interrupted 1553 communications in a way that suits the application.)

DPMA vs DMA

DPMA, in this context, means that both the CPU and the 1553 bus controller can access the memory located on the interface (I/O) board. DPMA controllers arbitrate CPU access to the interface board's local memory. The CPU requests access to the I/O board's local memory through either memory or I/O read/write cycles, depending on the system architecture. The 1553 bus controller grants access to the CPU as soon as the I/O board's local bus is free.

Thus the major system consideration when designing an interface board that has a DPMA controller is the available space for either system memory or I/O-addressing. For new systems, either approach is feasible, but for existing systems, where memory space may be at a premium, I/O addressing offers the better alternative.

Like DPMA controllers, DMA controllers provide the DMA handshake signals necessary to gain control of the CPU bus and access to system memory. Unlike DPMA schemes, I/O boards using DMA can access the system memory directly and lock the CPU out of that memory for the duration of the I/O operation.

Therefore, when planning a DMA I/O-board design, you must consider not only how much memory space

You may well want to make your I/O boards more versatile than the manufacturers' specifications allow.

is available in the system but also how the CPU's idle time affects the general operations of the system, and also whether or not the system can handle DMA at all. CPU idle time includes not only DMA transfer time but also DMA-handshake delays. When designing a new system, these considerations may present few or no problems. For existing systems, however, adding a DMA interface board could be impractical—or even impossible—if the system was not initially designed for DMA.

DPMA is more adaptable

Of the two approaches, then, DPMA is clearly the easier one to adapt to various exisiting systems. For one thing, the DPMA requires less system overhead than does DMA. Furthermore, its only demand on the precious system resources is some I/O addressing space (I/O addressing space is often at less of a premium than memory addressing space).

Although a DPMA interface board is more versatile from an application viewpoint than a DMA board, a DPMA board using the DDC chip set has a major fault: It's hard to test because it is inherently unfriendly to fault isolation.

The Bus-66300, if configured as recommended by DDC (**Ref 1**), arbitrates CPU access to the I/O board's local memory with its $\overline{\text{IOEN}}$ signal (see **box,** "Signal definitions"). This signal is an output from the Bus-

Signal definitions

$\overline{\text{DMACK}}$: DMA Acknowledge. Active low, this UT1553 (pin 58) signal confirms the receipt of a DMA Grant; it stays low until memory access is complete.

$\overline{\text{DMAG}}$: DMA Grant. Active low, this input to the UT1553 (pin 57) allows the UT1553 to access memory.

$\overline{\text{DMAR}}$: DMA Request. Active low, this signal comes from the UT1553 (pin 56) when it requires access to memory. It goes inactive following the receipt of a $\overline{\text{DMAG}}$ signal.

$\overline{\text{HPINT}}$: High Priority Interrupt. Active low, this signal comes from the UT1553 (pin 70) upon the occurrence of events enabled in the High Priority Interrupt Register.

$\overline{\text{INT}}$: Interrupt. Active low, the output from Bus-66300 (pin 45) provides an interrupt pulse to CPU.

$\overline{\text{IOENBL}}$: same as $\overline{\text{IOEN}}$

$\overline{\text{IOEN}}$:Input/Output Enable. Active low, the output from the Bus-66300 (pin 42) to enable external latches or buffers connecting the Bus-66300 to the CPU's address and data buses.

$\overline{\text{IRQ}}$: Interrupt Request. Active low, the output to the CPU, G64 I/O pin B16, for requesting a CPU interrupt.

$\overline{\text{MEMCSO}}$: Memory Chip Select Out. Active low, the output from the UT1553 (pin 54) to enable memory.

$\overline{\text{MEMCS}}$: Memory Chip Select. Active low, output from Bus-66300, pin 16, to enable memory.

$\overline{\text{MEMWR}}$: Memory Write. Read = 1, Write = 0. The output from Bus-66300, pin 57, specifying data-flow direction during memory access.

$\overline{\text{MEM/REG}}$: Memory/Register. Input to Bus-66300 (pin 10) selects memory or register data transfer: $\overline{\text{MEM/REG}}$ = 0 selects Bus-66300 registers; $\overline{\text{MEM/REG}}$ = 1 selects memory.

$\overline{\text{RDYD}}$: Ready Data. Active low, the output from Bus-66300 (pin 3) that indicates that data has been received from, or is available to, the CPU.

$\overline{\text{RDY}}$: Ready. Active low, the output from board (G64 I/O pin A15) used by the CPU to generate wait states.

$\overline{\text{RESET}}$: Reset. Active low, the input from CPU (G64 I/O pin B14) for system reset.

$R\overline{W}R$: RAM Write. Read = 1, Write = 0. The output from UT1553 (pin 52) specifies the direction of the data flow during a memory access.

$BR/\overline{W}$: Buffered Read/Write. Read = 1, Write = 0. The input from CPU (G64 I/O pin A17) indicating direction of data flow.

$\overline{\text{SELECT}}$: Select. Active low, The input to Bus-66300 (pin 1) that selects the Bus-66300 for operation.

$\overline{\text{STD INTL}}$: Standard Interrupt (Level). Active low, the UT1553 (pin 68) asserts this signal when one or more events enabled in the standard Interrupt Enable Register, RT Descriptor, or BC Command Block occur.

$\overline{\text{STRBD}}$: Strobe Data. Active low, the input to Bus-66300 (pin 41) in conjunction with $\overline{\text{SELECT}}$, indicates a data transfer to or from the CPU.

$\overline{\text{VPA}}$: Valid Peripheral Address. Active low, the input from the CPU (G64 I/O pin A14) that indicates that the CPU bus-address lines contain an I/O address.

66300 that enables the external latches or buffers connecting the Bus-66300 to the CPU's address and data buses. Because the signal is an output from the Bus-66300, the proper operation of the $\overline{\text{IOEN}}$ signal depends on a variety of conditions. They include the health of the Bus-66300, the timing relationships between CPU-generated inputs ($\overline{\text{STRBD}}$ and $\overline{\text{SELECT}}$), the CPU's recognition of Bus-66300 outputs ($\overline{\text{RDYD}}$, $\overline{\text{INT}}$), the health of the discrete logic circuits that carry these signals, and the general design and assembly of the board.

If a failure occurs that inhibits $\overline{\text{IOEN}}$, the Bus-66300's data and address buffers remain inoperative, preventing CPU access to the I/O board's internal bus. Therefore, in the event of any malfunction that prevents the Bus-66300 from granting CPU access to the board, the board is electronically isolated from the system. Thus, you cannot use just software for fault isolation, and this limitation makes hardware development and debugging unnecessarily difficult.

Adding circuitry for putting the Bus-66300 under CPU control lets you verify your design sequentially and also debug (**Fig 1**). You can then diagnose the faults that would have isolated the board, if it were set up per DDC's configuration, by placing the board under CPU control. At that point, you can test the G64 I/O-control circuitry, data and address lines, memory, and control circuitry independently from the Bus-66300.

For new designs, this independence means you can test the CPU-interface circuitry without having either the Bus-66300 or Bus-65600 installed on the board (you must place pullup resistors on Bus-66300 outputs $\overline{\text{MEMWR}}$, $\overline{\text{MEMCS}}$, $\overline{\text{IOENBL}}$, $\overline{\text{INT}}$, and $\overline{\text{RDYD}}$ (pins 57, 16, 42, 45, and 3, respectively). For normal operation, the CPU returns board arbitration to the Bus-66300, but maintains the power, via software or system reset, to regain control.

Fig 1 shows the block diagram for a G64 Bus to a MIL-STD-1553 bus-interface board, using the DDC Bus-66300/Bus-65600 chip set. The CPU's control lines connect to the Bus-66300 via the G64 I/O. But unlike DDC's layout, the control lines must first pass through the I/O board's CPU-control circuitry. This circuitry determines whether the Bus-66300 or the CPU has control of the I/O board's local bus and memory.

Figs 2 and **3** show the details of the CPU control

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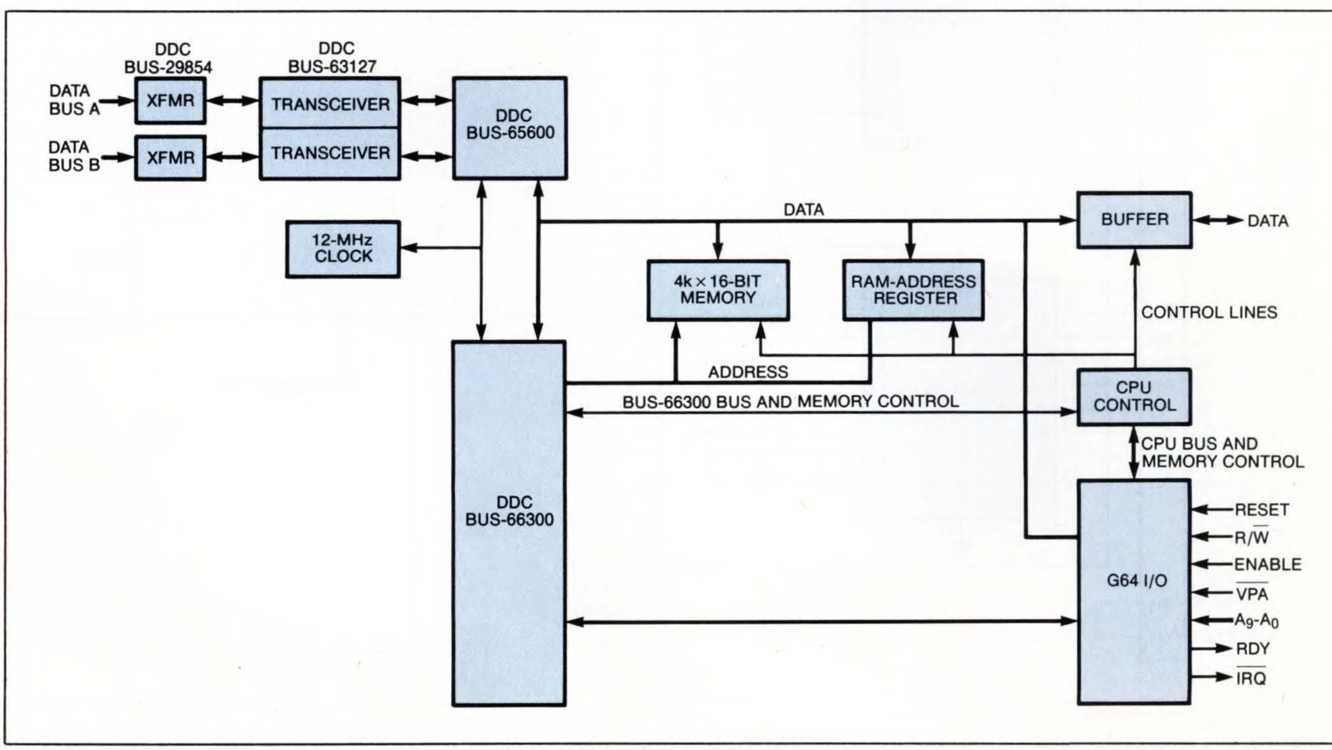


***Fig 1—Adding the CPU-control circuitry to its** manufacturer's application recommendations allows the system CPU to set up and test the 1553 interface.*

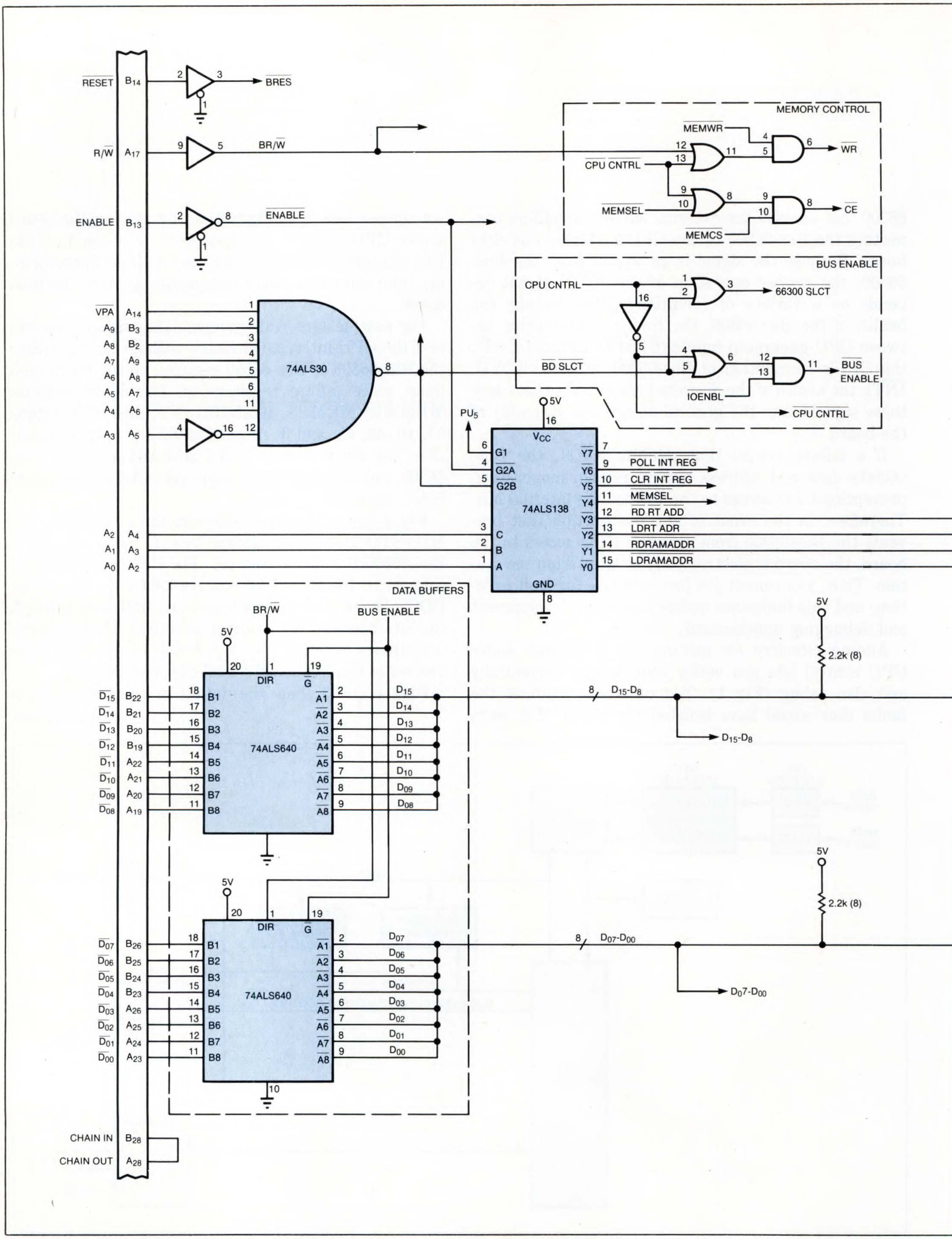
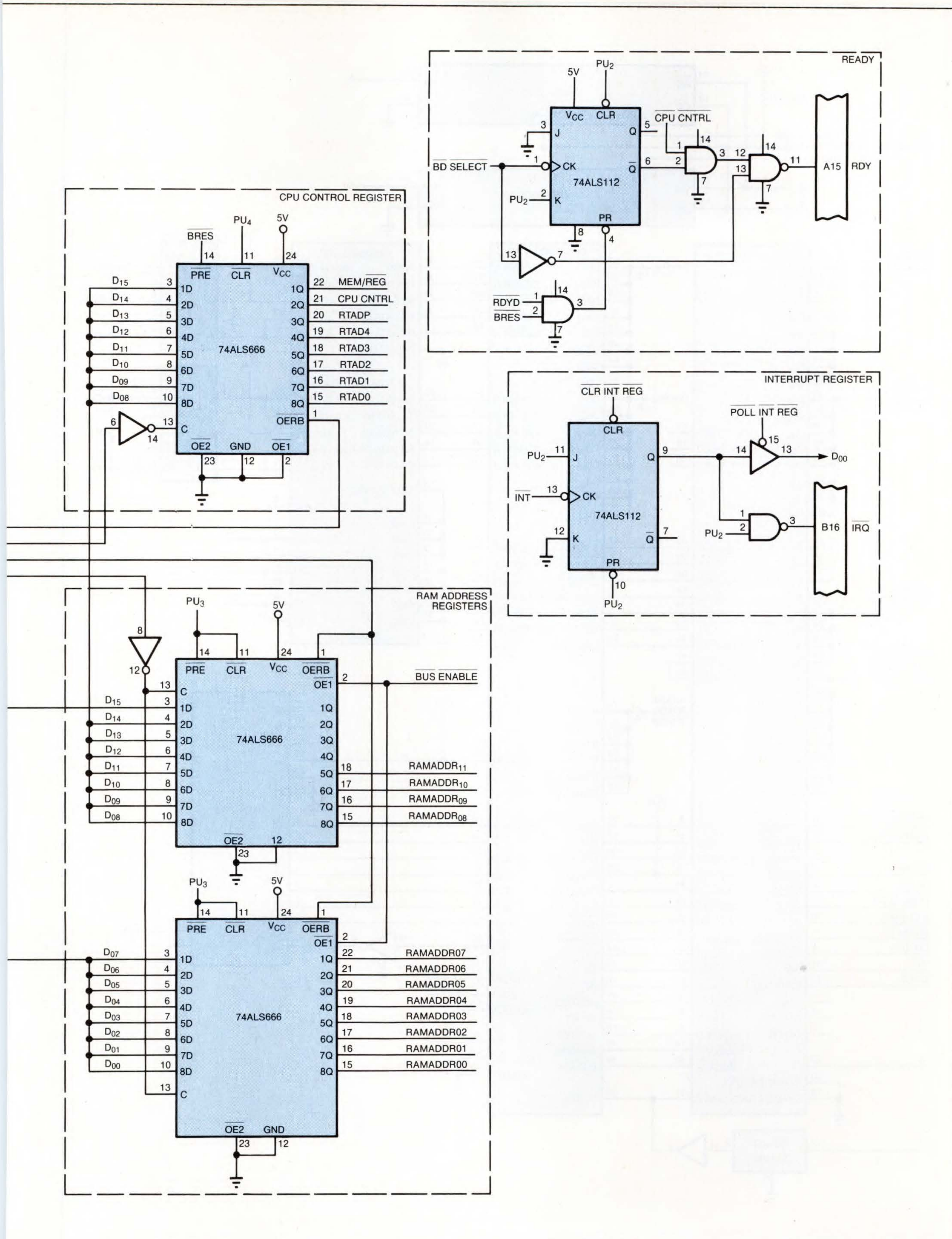


Fig 2a—The memory-control, bus-enable, *CPU-control register, ready, and interrupt circuits of this diagram form the CPU-control circuitry, while these data buffers and address demultiplexers form the heart of the design's dual-port memory.*


READY
5V
PU2
VCC
CLR
J
CK
K
Q
74ALS112
PR
BD SELECT
PU2
CPU CNTRL
A15
RDY
RDYD
BRES
CPU CONTROL REGISTER
BRES
PU4
5V
PRE
CLR
VCC
74ALS666
1D
2D
3D
4D
5D
6D
7D
8D
C
OE2
GND
OE1
OERB
MEM/REG
CPU CNTRL
RTADP
RTAD4
RTAD3
RTAD2
RTAD1
RTAD0
D15
D14
D13
D12
D11
D10
D09
D08
INTERRUPT REGISTER
CLR INT REG
POLL INT REG
PU2
INT
D00
B16
IRQ
RAM ADDRESS REGISTERS
PU3
BUS ENABLE
RAMADDR11
RAMADDR10
RAMADDR09
RAMADDR08
D07
D06
D05
D04
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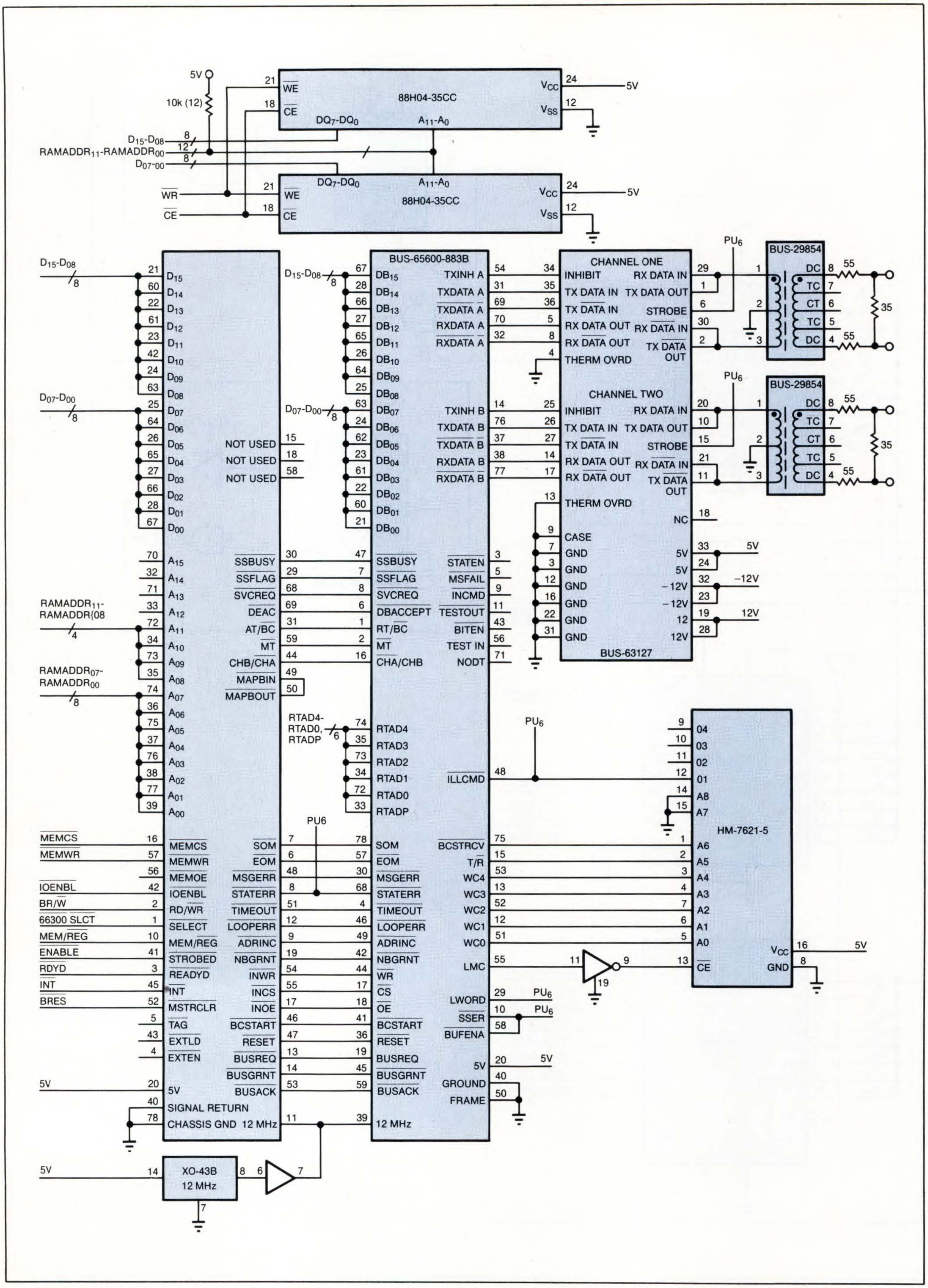

Fig 2b—The Bus-66300 and its associated chips *can handle 1553-bus transactions to and from local memory.*

DPMA controllers arbitrate CPU access to the interface board's local memory.

circuitry and timing, respectively. This circuitry is specific to the Gespac G64 Bus, the DDC Bus-66300 1553 controller, and the Electronic Designs 88H04C-35CC memory. Furthermore, system specifications require I/O mapping of the board's local memory and disallow hard-wired CPU interrupts.

During normal operation, a software command or system reset ($\overline{\text{RESET}}$) initializes the board to the CPU-control mode. The CPU loads parameters into the Bus-66300's internal registers and the I/O board's local memory for 1553 data transfers. After the CPU enters all parameters, it grants bus arbitration and memory access to the Bus-66300. The CPU then commands the Bus-66300 to begin 1553 data transfers.

When a 1553 data transfer is complete, the Bus-66300, operating under the assumption that the CPU initialized the Bus-66300 in order to generate interrupts, produces an interrupt ($\overline{\text{INT}}$). The interrupt sets the interrupt register (system specifications didn't allow using the G64's $\overline{\text{IRQ}}$ line). The CPU polls the interrupt register (I/O address $3F6_{HEX}$) to check its status. When an interrupt occurs, the CPU can then either access the Bus-66300's internal registers and the I/O board's local memory using the Bus-66300 as arbitrator, or the CPU can place the board under its control and access the I/O board's local memory directly.

The CPU-control circuitry includes the bus-enable, memory-control, and ready circuitry as well as the CPU-control register. During power-on initialization, the CPU generates a System Reset ($\overline{\text{RESET}}$), which, by default, puts the board under CPU control (CPU-control-register output 2Q, CPU CNTRL = 1). The CPU communicates with the I/O board by addressing it as a peripheral device ($\overline{\text{VPA}}$) Valid Peripheral Address), at locations $3F0_{HEX}$ through $3F7_{HEX}$ (for example address $3F0_{HEX}$ = Load RAM Address, see the I/O addresses in **Table 1**).

When the CPU addresses the I/O board, $\overline{\text{BD SELECT}}$ and one output of the 74ALS138 3:8 decoder go low. For example, if the CPU initiates a read or

TABLE 1—BUS-66300 BOARD I/O ADDRESSES

ADDRESS (HEX)	FUNCTION
3F0	LOAD RAM ADDRESS
3F1	READ RAM ADDRESS
3F2	LOAD REMOTE TERMINAL ADDRESS, MEM/REG, CPU CONTROL
3F3	READ REMOTE TERMINAL ADDRESS, MEM/$\overline{\text{REG}}$, CPU CONTROL
3F4	RAM MEMORY SELECT
3F5	CLEAR INTERRUPT REGISTER
3F6	READ CONTENTS OF INTERRUPT REGISTER
3F7	NOT DEFINED

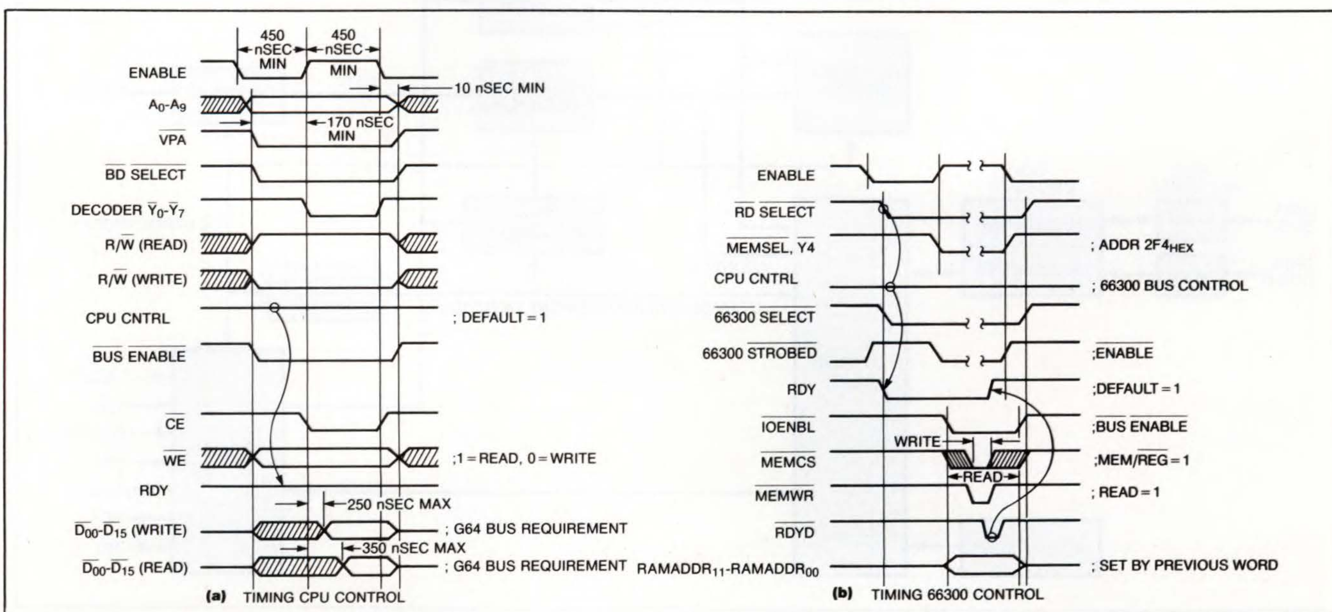

Fig 3—The I/O board's circuitry *must meet MIL-STD-1553 timing specifications.*

If you use a DMPA controller, your only major system concern is either the space in the system memory or in I/O addressing subsystem.

write memory cycle (I/O address $3F4_{HEX}$), then the 74ALS138 3:8 decoder's output Y4 (MEMSEL) goes low. With CPU CNTRL = 1, 66300 SLCT (input to Bus-66300 pin 1, SELECT) remains high, thus preventing the Bus-66300 from generating its data-bus and memory-control signals (IOENBL, MEMWR, and MEMCS). These signals remain high, and the Bus-66300 data and address lines go to the high-impedance state. Also, the bus-enable circuitry's BUS ENABLE signal goes low, enabling both the data buffers and RAM-address registers.

When the CPU sets the Y4 output of the 74ALS138, MEMSEL, it enables the I/O board's local memory (CE). The CPU also specifies read or write operations (WR) by generating R/W. The I/O board's RDY output from the ready circuitry remains high, which signals the CPU that the I/O board requires no wait states to complete this operation. The CPU reads from, or writes to, the memory location specified by the contents of the RAM-address registers.

Normal operation sets CPU CNTRL low

For normal I/O operation, the CPU relinquishes control of the I/O board to the Bus-66300 by setting CPU CNTRL low. The CPU accomplishes this setting by writing $8XXX_{HEX}$ into the CPU-control register (I/O address $3F2_{HEX}$. The 74ALS138 3:8 decoder's output (Y2, LDRT ADDR,) strobes CPU CNTRL low (this sequence also sets the CPU-control register's 1Q output, (MEM/REG) high, selecting access to onboard memory).

When the CPU requests memory access (I/O address $3F4_{HEX}$) with the Bus-66300 in control of the board (CPU CNTRL = 0), BD SELECT sets 66300 SLCT low, selecting the Bus-66300 for operation. RDY goes low anticipating the need for the CPU to generate wait states. The Bus-66300, responding to the setting of its SELECT input via the 66300 SLCT line, stops its present task and generates the IOENBL, MEMWR, and MEMCS signals (depending on the state of the BR/W—or RD/WR—and MEM/REG lines).

The Bus-66300's IOENBL sets BUSENABLE low via the bus-enable circuitry, enabling the data buffers and RAM-address registers. The Bus-66300's MEMWR and MEMCS signals generate the memory control signals WR and CE, respectively, via the memory-control circuitry. The contents of the RAM-address registers specify the location from which data is read, or to which it is written. The Bus-66300 pulls its RDYD signal low, driving RDY high and indicating to the CPU that the operation can be completed without additional wait states.

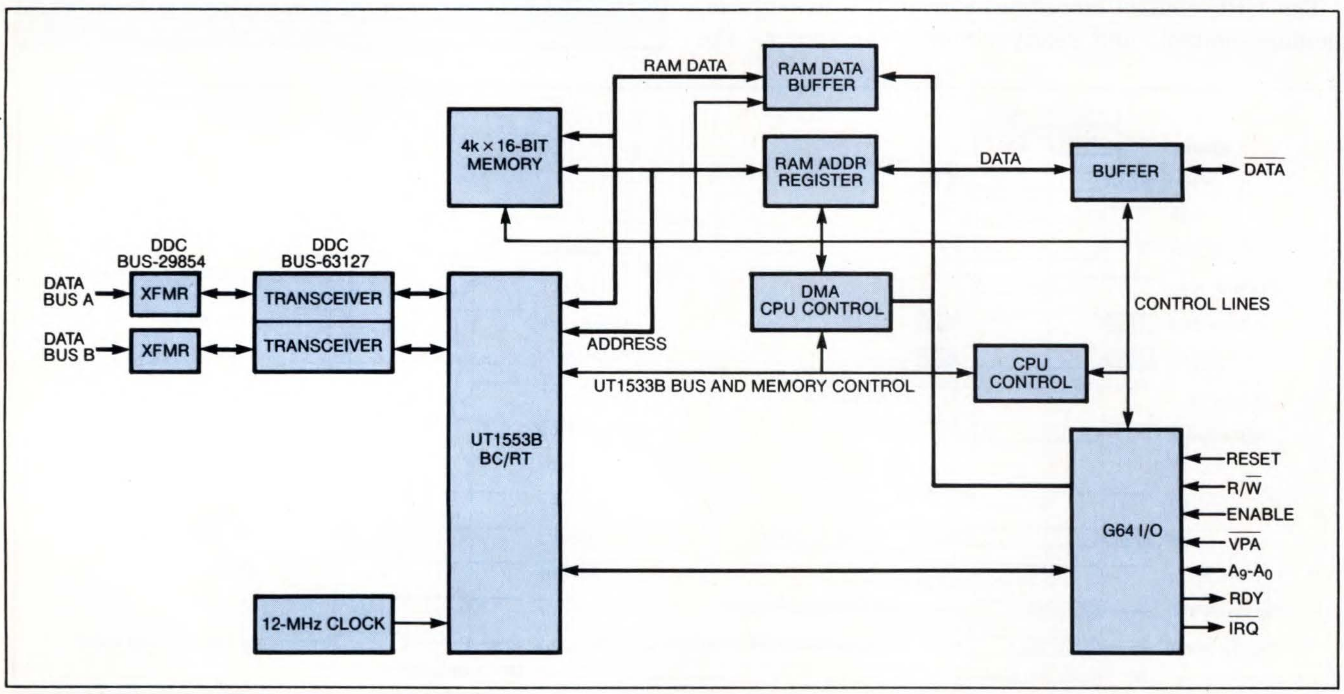

Fig 4—Like Fig 1, this block diagram has extra *circuitry to transform a DMA bus controller into a DPMA bus controller that can be put under CPU control at will.*

CIRCLE NO 192

You must consider the effects of the CPU idle time and also whether or not the system can handle DMA at all.

Note that if the CPU had previously written $0XXX_{HEX}$ into the CPU-control register (at address $3F2_{HEX}$) instead of $8XXX_{HEX}$, the CPU-control register's MEM/$\overline{\text{REG}}$ output would have been low, and the previous cycle of operation would have accessed the Bus-66300's internal registers instead of I/O-board's local memory.

You can adapt DMA controllers to DPMA

Although DPMA is a practical—and perhaps the preferred—method of CPU interfacing, the majority of 1553 bus controllers perform only DMA. The controllers work well with systems that support DMA devices. Configuring a DMA controller to look like a DPMA device requires a special design. An onboard CPU simulator can make an I/O board with a DMA controller look like one that uses a DPMA device. **Fig 4** uses the UTMC UT1553 Bus Controller/Remote Terminal to illustrate such a design.

Using CPU control improves the I/O board's testability. You can independently verify the workings of the CPU interface with or without the UT1553 installed on the I/O board. And the CPU can perform better software-directed tests of the I/O board's functions. With the added circuitry that makes the DMA device function as a DPMA device, the I/O board adapts more easily to a variety of systems because the only system resource it needs is a small range of I/O address space.

The CPU gains access to the board's bus and memory via the CPU-control circuitry **(Fig 4).** The CPU simulator simulates the DMA-CPU handshake without CPU involvement. Upon a DMA request, the UT1553 accesses onboard memory as if it were system memory.

Fig 5 shows the board's schematic. This circuit's CPU-control circuitry is similar to that used for the Bus-66300 **Fig 3,** because the CPU bus, memory, and system requirements are identical. The differences between the two circuits stem directly from the differences between the UT1553 and Bus-66300 controllers.

Major system differences

Some major differences between the two designs result from the UT1553 being set up as a DMA controller; thus this device would normally arbitrate CPU access to the I/O board's bus and memory. The UT1553 must be set up as a DMA controller because it doesn't operate as the Bus-66300 does. In the Bus-66300, the CPU can access status and control registers; in the UT1553, such direct access would interfere with the controller's handling of 1553 communication.

TABLE 2—UT1553 BOARD I/O ADDRESSES

BOARD ADDRESS (HEX)	FUNCTION
3F7	BC RT REGISTER SELECT
3F0	LOAD RAM ADDRESS
3F1	READ RAM ADDRESS
3F2	LOAD $\overline{\text{CPU CONTROL}}$, $\overline{\text{EXT OVR}}$
3F3	READ $\overline{\text{CPU CONTROL}}$, $\overline{\text{EXT OVR}}$
3F4	RAM MEMORY SELECT
3F5	CLEAR INTERRUPT REGISTER
3F6	READ INTERRUPT REGISTER & CPU RAM CONTROL REGISTER

To allow uninterrupted operation of the UT1553 while the CPU accesses the board, this design adds RAM data buffers and modifies the memory-control and bus-enable circuitry. These changes allow the CPU to access the board at any time, independently of any UT1553 operation and without the board being in a CPU-control mode. In the Bus-66300-based I/O board, the CPU could access the board, independently of any Bus-66300 operation, only with the board in CPU-control mode.

The CPU-control circuitry includes the memory-control circuitry, RAM data buffers, and CPU-control register. The onboard CPU simulator consists of the DMA and DMAG registers, which latch the DMA handshake signals used by the UT1553.

During power initialization, the CPU generates a system reset ($\overline{\text{RESET}}$), which, by default, places the board under CPU control (CPU-control register 1Q output, $\overline{\text{CPU CNTRL}}=0$; DMA register $\overline{\text{Q}}$ output $=0$; $\overline{\text{CPU RAM CNTRL}}=0$). With $\overline{\text{CPU CNTRL}}=0$, the DMA and CPU-control simulator circuitry prevents the UT1553 from generating its memory-control signals ($\overline{\text{RWR}}$ and $\overline{\text{MEMCS0}}$).

The CPU communicates with the I/O board by addressing it as a peripheral device ($\overline{\text{VPA}}$ Valid Peripheral Address) at locations $3F0_{HEX}$ through $3F7_{HEX}$ (see I/O addresses in **Table 2.** When addressed, $\overline{\text{BD SELECT}}$ goes low, enabling the data buffers and setting one output of the 3:8 decoder low.

If the CPU has initiated a read or write memory cycle (I/O address $3F4_{HEX}$), for example, $\overline{\text{MEMSEL}}$ goes low. A $\overline{\text{MEMSEL}}$ signal produces the RAM data buffers' enable signal ($\overline{\text{RAM DATA EN}}$) and memory-enable signal ($\overline{\text{CE}}$). The CPU then generates the read-write signal, BR/$\overline{\text{W}}$, which produces the onboard-memory write signal ($\overline{\text{WR}}$). The CPU can then read

Text continued on pg 238

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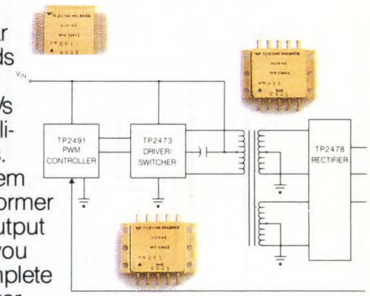

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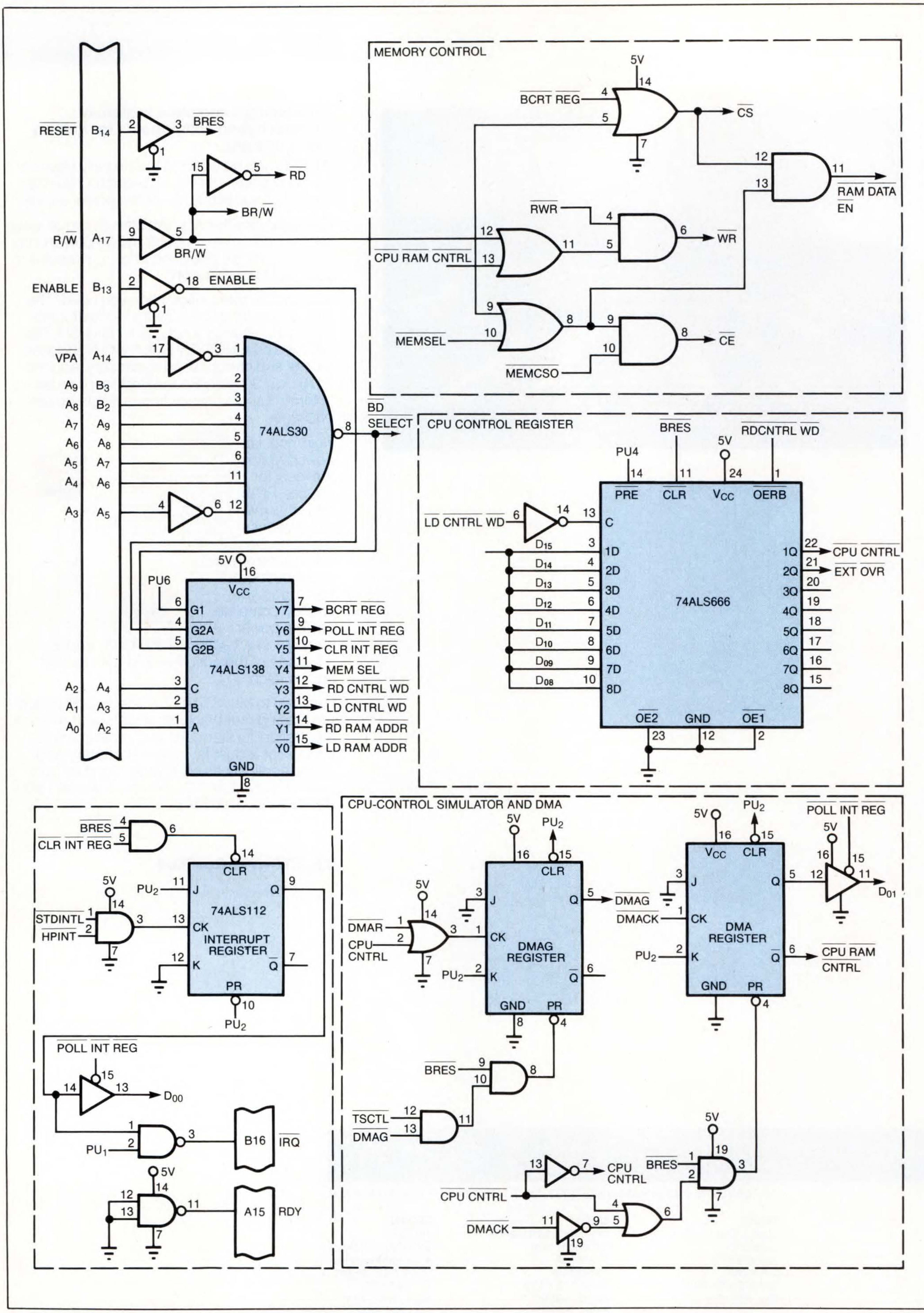


***Fig 5a—The control registers** of this design are similar to the ones in **Fig 2** except for the added CPU simulator circuitry.*

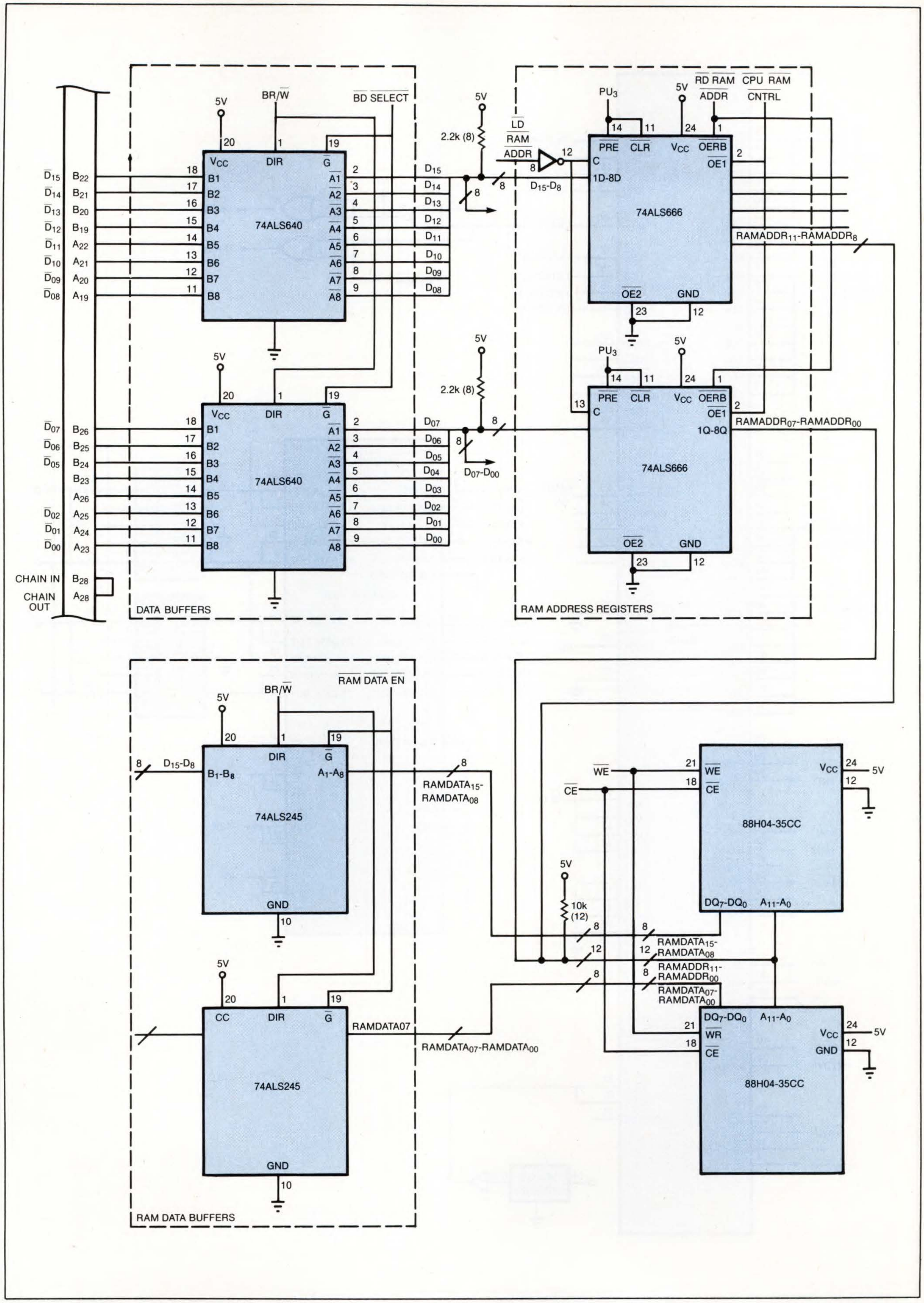


***Fig 5b—Like the cirucit in Fig 2, this** design uses buffers and latches to couple the local memory to the system bus under CPU control.*

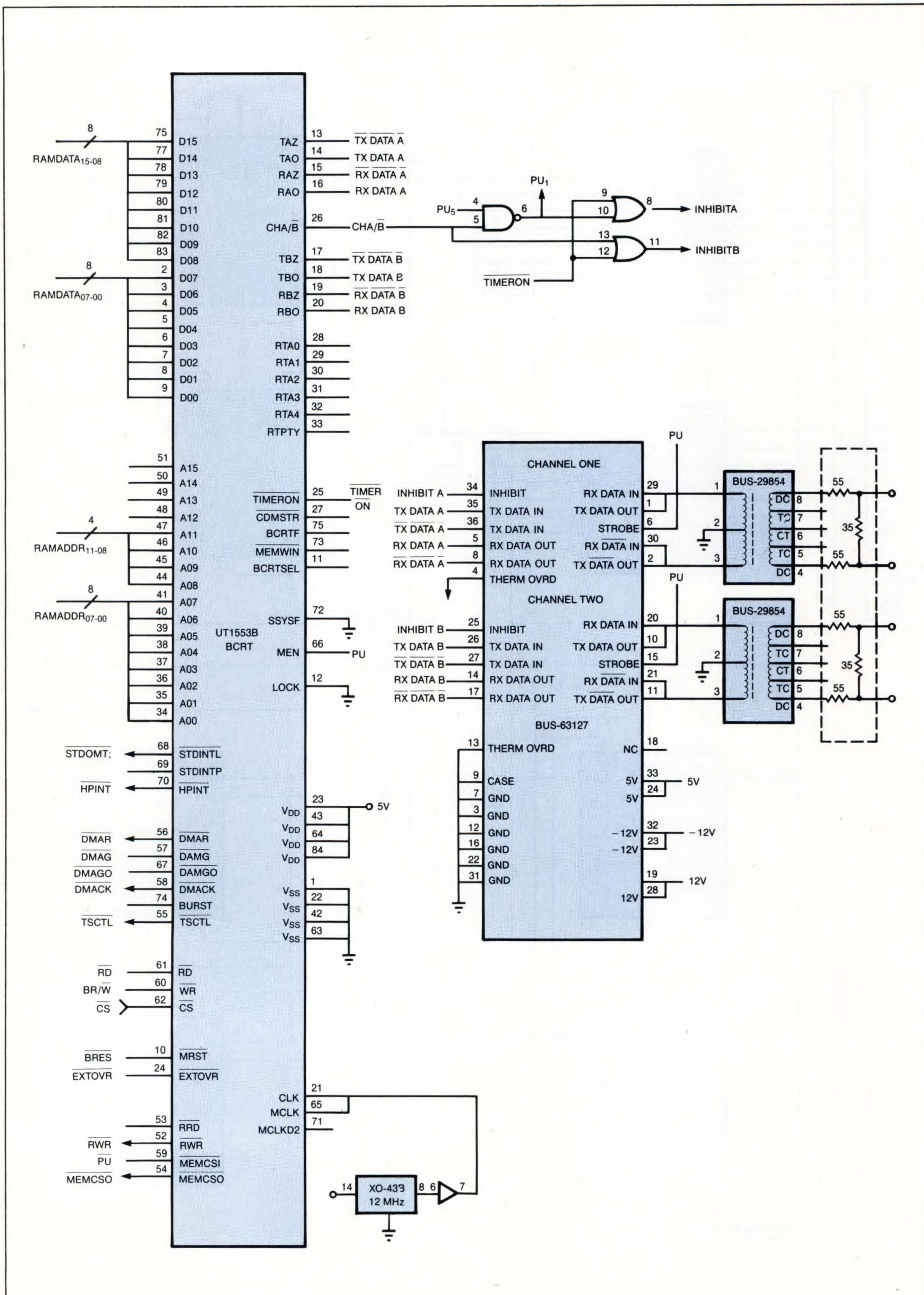


Fig 5c—The 1553-bus interface chip performs DMA to local memory instead of system memory.

For existing systems, where memory space may be at a premium, I/O addressing offers the better alternative.

to or write from the memory location specified by the contents of the RAM-address registers.

CPU releases I/O board from its control

The CPU releases the I/O board from CPU control by setting $\overline{\text{CPU CNTRL}}$ high. The CPU sets $\overline{\text{CPU CNTRL}}$ high by writing CXXX_{HEX} into the CPU-control register (I/O address 3F2_{HEX}; 3:8 decoder output $\overline{\text{Y2}}$, $\overline{\text{LD CNTRL WD}}$ high).

Taking the board out of CPU control ($\overline{\text{CPU CNTRL}}$=1) allows the CPU-control and CPU-simulation circuitry to process memory requests from the UT1553. The UT1553 requests memory access by asserting its DMA request signal ($\overline{\text{DMAR}}$) **(Ref 2)**.

The DMAG register's Q output, $\overline{\text{DMAG}}$, goes low, producing a DMA grant, which in turn allows the UT1553 to begin accessing memory. The UT1553 responds to the DMA grant by asserting a DMA acknowledge ($\overline{\text{DMACK}}$). The first $\overline{\text{DMACK}}$ sets the DMA register's Q output low, indicating to the CPU that a DMA has begun. The DMA register's $\overline{\text{Q}}$ output, $\overline{\text{CPU RAM CNTRL}}$, goes high, making the RAM data buffers go to the high-impedance state, and preventing CPU access to the memory-control signals ($\overline{\text{WR}}$ and $\overline{\text{CE}}$). The UT1553 asserts $\overline{\text{TSTCL}}$ when it is actually accessing memory. A $\overline{\text{TSTCL}}$ signal presets the DMAG register ($\overline{\text{DMAG}}$=1) in preparation for another DMA request.

CPU retains access

Although the UT1553 has control of the onboard memory, the CPU still retains access to much of the I/O board's circuitry. Specifically, it can access the RAM-address registers (address 3F0_{HEX} and 3F1_{HEX}), CPU-control register (address 3F2_{HEX} and 3F3_{HEX}), and interrupt and DMA registers (I/O address 3F5_{HEX} and 3F6_{HEX}). During UT1553 memory operations, CPU access to either memory (I/O address 3F4_{HEX}) or the internal registers of the UT1553 (I/O address 3F7_{HEX}) is illegal. A high $\overline{\text{CPU RAM CNTRL}}$ signal blocks these two operations.

The UT1553 retains uninterrupted access to memory until the CPU places the I/O board back under CPU control (writes 4XXX_{HEX} to I/O address 3F2_{HEX}). If the CPU requests control during a DMA cycle, $\overline{\text{CPU RAM CNTRL}}$ remains high, preventing CPU access to memory, until $\overline{\text{DMACK}}$ goes high, indicating the end of the DMA cycle.

During normal operation, a typical operating sequence might begin when the CPU initializes the I/O board to the CPU-control mode via a system reset or writing to the CPU control register. The CPU loads parameters into the UT1553's internal registers and memory for a 1553 bus data transfer. Then it grants memory access to the UT1553 and commands the UT1553 to begin 1553 data transfers.

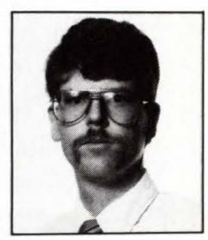
The interrupt register latches the interrupts generated by the UT1553 ($\overline{\text{STDINTL}}$ or $\overline{\text{HPINT}}$). Upon completion of 1553 bus data transfers, the UT1553 sets the interrupt register (interrupt-register Q output=1). The CPU polls the the interrupt register (I/O address 3F6_{HEX}) for status. When an interrupt occurs, the CPU places the board into the CPU-control mode, reads data from memory, and re-initializes the board for more 1553 bus data transfers. **EDN**

References

1. *MIL-STD-1553 Designer's Guide*, ILC Data Devices Corp, Bohemia, NY.

2. *UT1553-BCRT-1-4-86-TR Data Book*, United Technology Microelectronics Center, Colorado Springs, CO.

Author's biography



Steven W Rider has worked for Westinghouse in its Integrated Logistics Systems Div for seven years. He is presently responsible for developing depot-level test equipment for B1B and F16 radar systems. Steven graduated from Cornell Univsersity in 1981. In his spare time, he enjoys horseback riding, camping, and softball.

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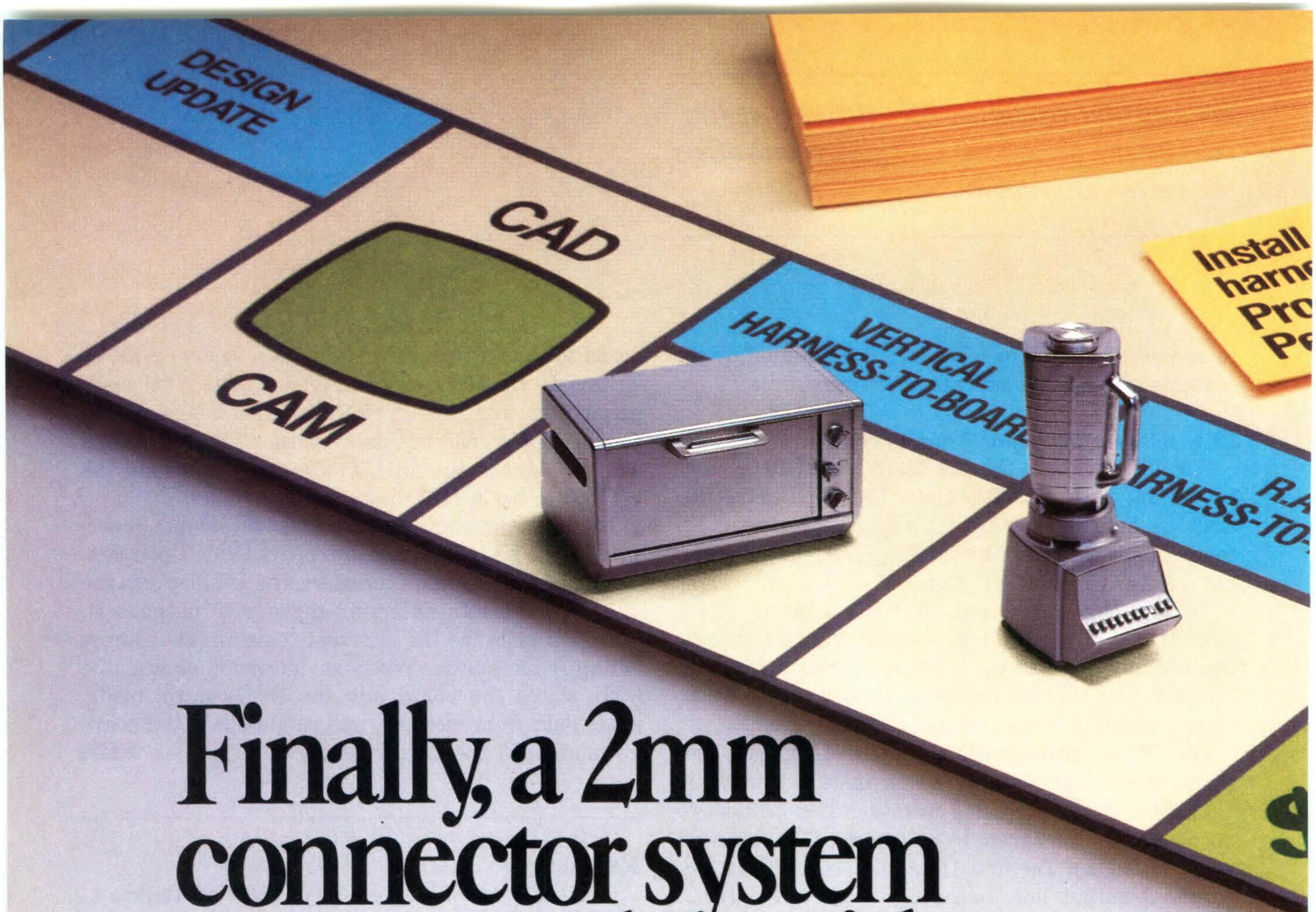

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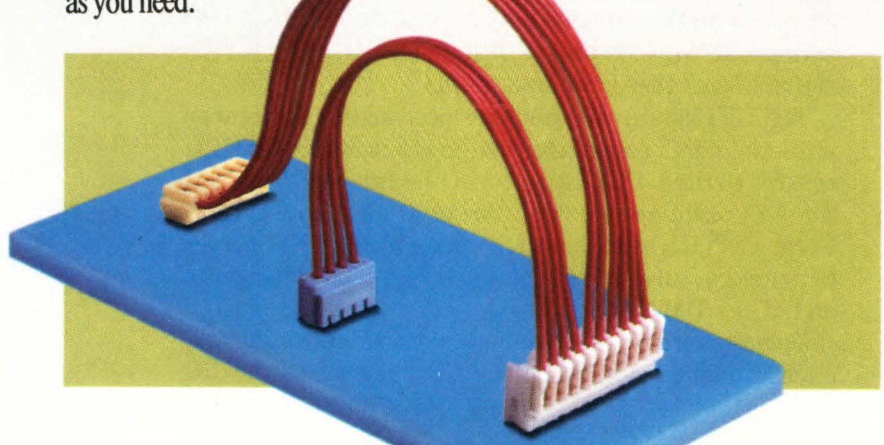

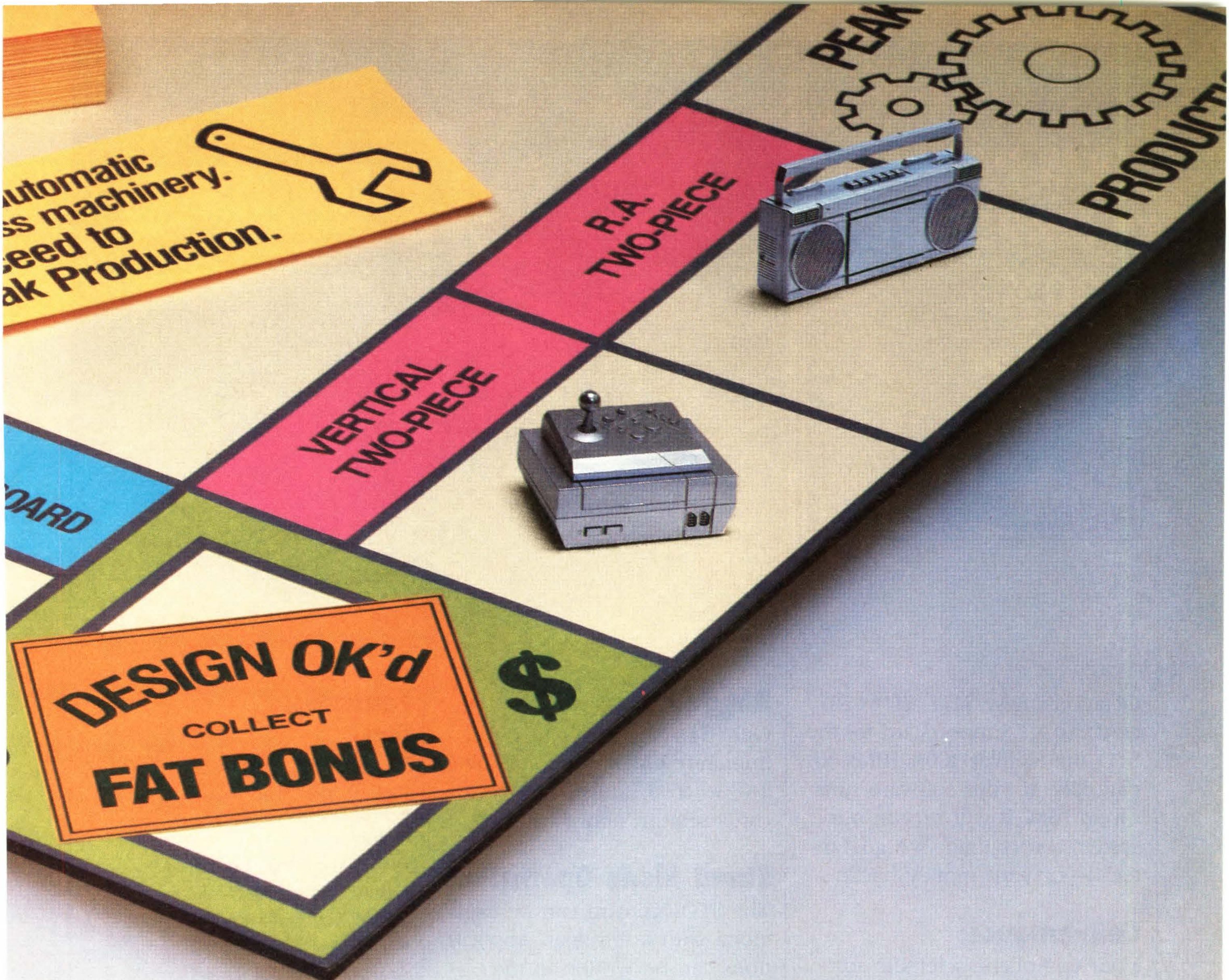

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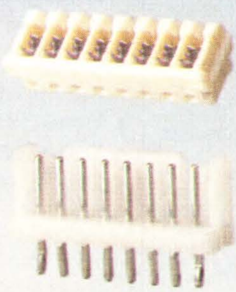

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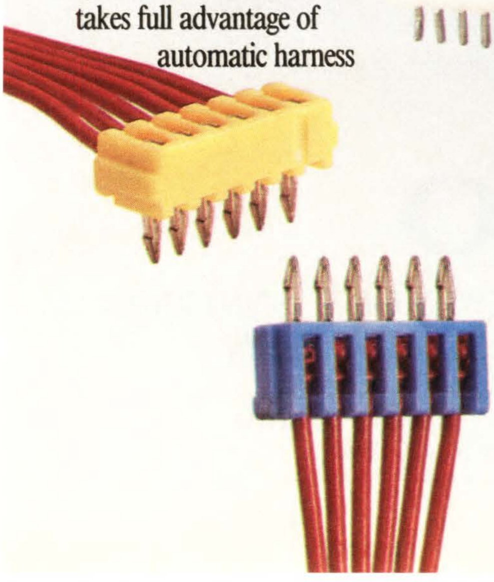

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CIRCLE NO 145

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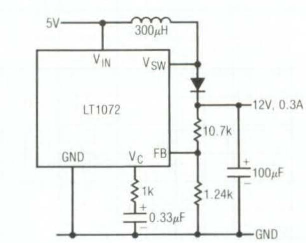
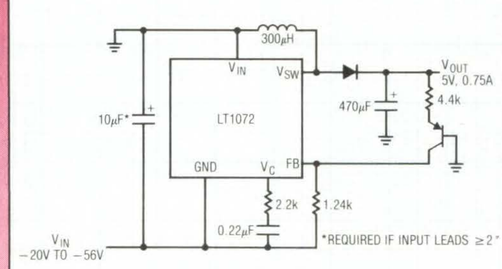


Telecom Converter (−48V to 5V)



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EDITED BY CHARLES H SMALL

Serial port controls parallel device

John McGowan
Advanced Micro Devices, Santa Clara, CA

The serial-to-parallel converter in **Fig 1** can transform your IBM PC into a controller. The circuit suits low-speed applications that require no more than one byte of data per second. A simple Basic routine (**Listing 1**) writes to the converter by using a PRINT statement.

The falling edge of the start bit of the serial data triggers half of the LM556 dual timer, which is configured as a one-shot. This one-shot enables the other half of the LM556, which functions as a 300-Hz clock. The 300-Hz clock serially shifts the 300-baud data from the PC into the 74HC164 serial-in, parallel-out register. The one-shot's period is just long enough to enable nine clock pulses. These nine pulses shift in a full byte of data and shift out the start bit.

LISTING 1

```
10  OPEN "COM1:300,N,8,1,CSO,DSO" AS #1
12  FOR J=0 TO 255
13  A$=CHR$(J)
20  PRINT #1,A$;
25  PRINT "just sent # "J" in count sequence. . ."
30  FOR I=1 TO 100:NEXT I
40  NEXT J
50  GOTO 12
```

The rising edge of the inverted output from the one-shot latches the parallel data into the 74HC273. The circuit has a power-up reset function, which prevents the output port from coming up in a random state.

EDN

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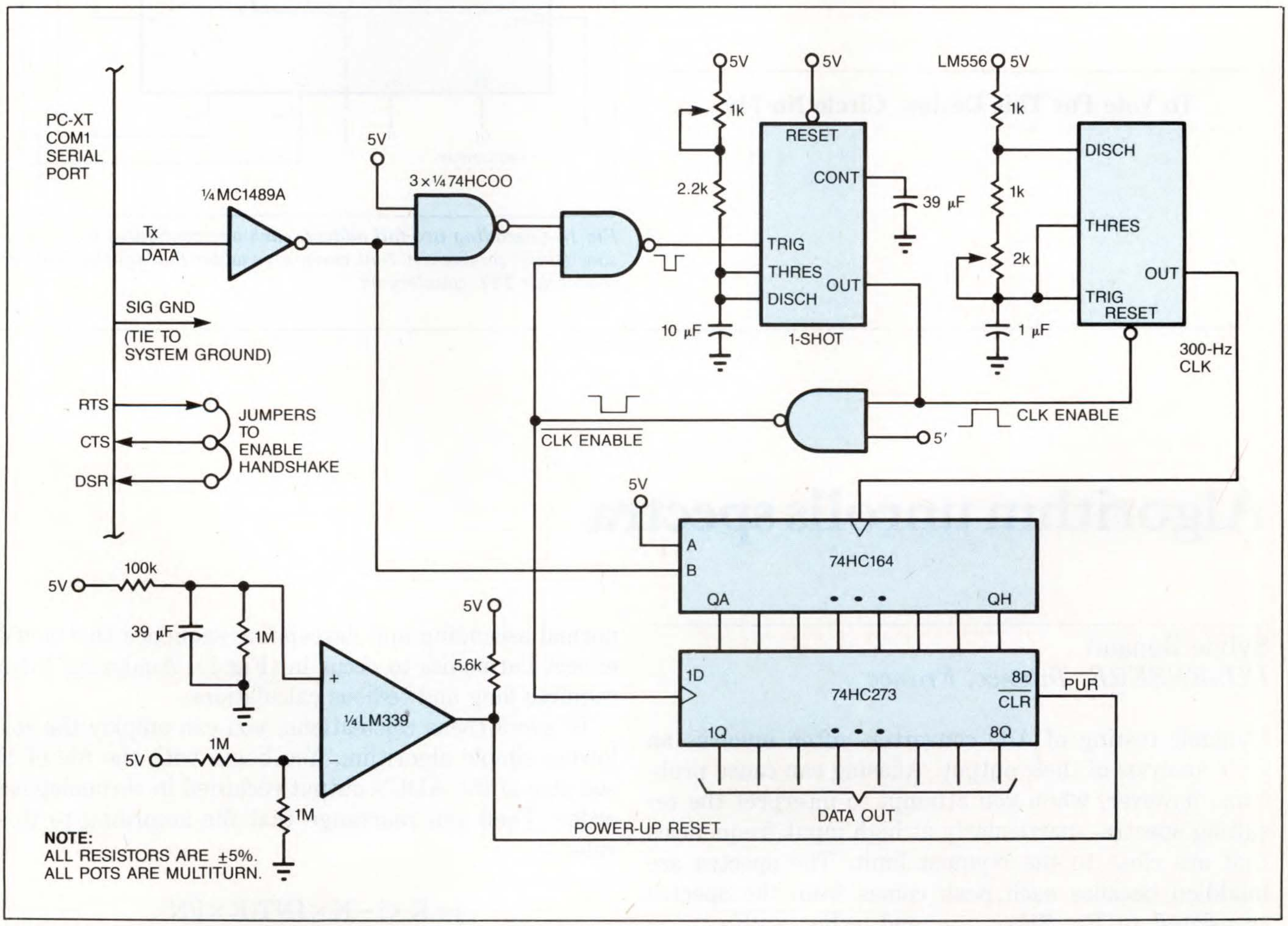

*Fig 1—**This serial-to-parallel converter allows** your IBM PC's serial port to control low-speed (1 byte/sec) processes.*

Full adders form 7-input carry-save adder

Shantha Fernando
Arthur C Clarke Centre for Modern Technologies, Katubedda, Sri Lanka

Building on an earlier design for configuring a 4-bit full adder as a dual carry-save adder ("Adders enable detection of multiple inputs," EDN, April 28, 1988, pg 240), **Fig 1** shows two such adders operating as a 7-bit carry-save adder. Configured this way, the 74LS283s produce their sum and carry outputs with a delay of less than 24 nsec—outperforming the 74LS183 dual carry-save adder.

In **Fig 1,** IC_1 adds three bits (a, b, and c) and produces two single-bit outputs, S_{abc} and C_{abc}. Similarly, one-half of IC_2 generates S_{def} and C_{def}. The other half of IC_2 adds these intermediate sum and carry outputs, together with the seventh input, g, and generates the final outputs, C_2, C_1, and S (S is the LSB). EDN

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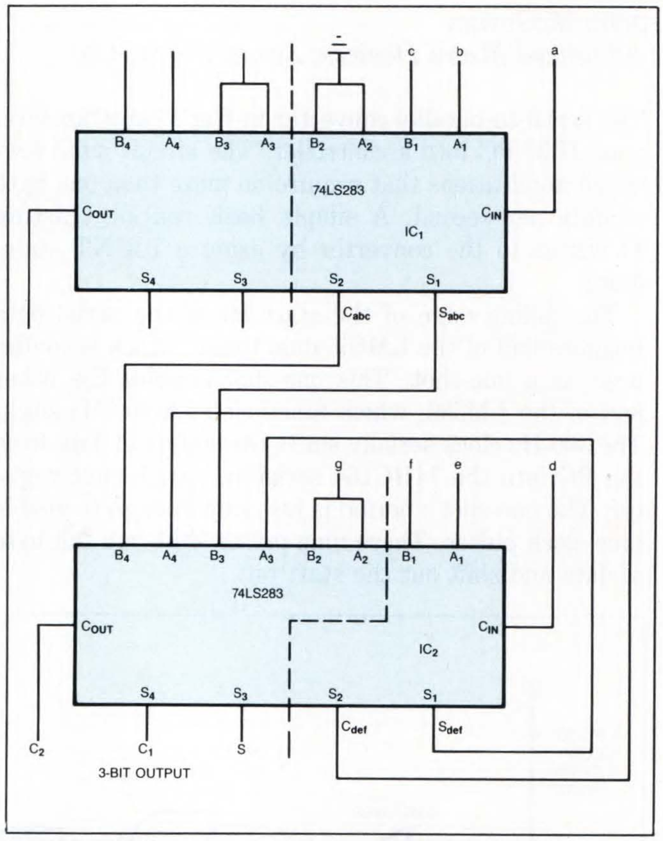

Fig 1—Cascading two full adders, each one configured as a carry-save adder, produces a 7-bit carry-save adder that's faster than its monolithic TTL counterpart.

Algorithm unrolls spectra

Sylvie Renaud
IXL-ENSERB, Talence, France

Dynamic testing of A/D converters often involves an FFT analysis of their output. Aliasing can cause problems, however, when you attempt to interpret the resulting spectra—particularly at high input frequencies that are close to the Nyquist limit. The spectra are muddled because each peak comes from the spectra translated to F_S, $2F_S$, . . . , and $-F_S$, $-2F_S$, ... The problem is that these peaks do not occur in the normal ascending and descending sequence that you'd expect harmonics to occur in **(Fig 1)**. Analyzing them requires long and tedious calculations.

To avoid these calculations, you can employ the following simple algorithm. You begin with the file of N samples of the ADC's output recorded in chronological order. Then you rearrange that file according to this rule:

$$j = R \times i - N \times INT(R \times i/N),$$


low pass
HIGH PASS
low pass
HIGH PASS

where i is the index into the original file, j is the corresponding index into the transformed file, and R is an integer.

Note that you must perform the test with coherent sampling. That is, $m \times F_S = N \times F_{IN}$, where m and N are integers and also coprimes. To maintain coherence, the integer R must be a submultiple of m.

In other words, index j is the result of modulo-N multiplication between the input index and integer R. This somewhat mysterious process has the effect of multiplying the number of samples by R, and thereby generating an artificial oversampling at an effective rate that's R times greater than the actual sampling rate. This oversampling enables you to "unroll" the spectrum, making it more intelligible (**Fig 2**).

In the example in **Fig 2**, the artificial-oversampling algorithm reveals a defect in the A/D converter by isolating spectral components X and X′, which are located at $(F_S/2 - F_{IN})$ and $(F_S/2 - 2F_{IN})$, respectively. In the direct FFT in **Fig 1**, these components are mixed with harmonics and are difficult to detect.

EDN

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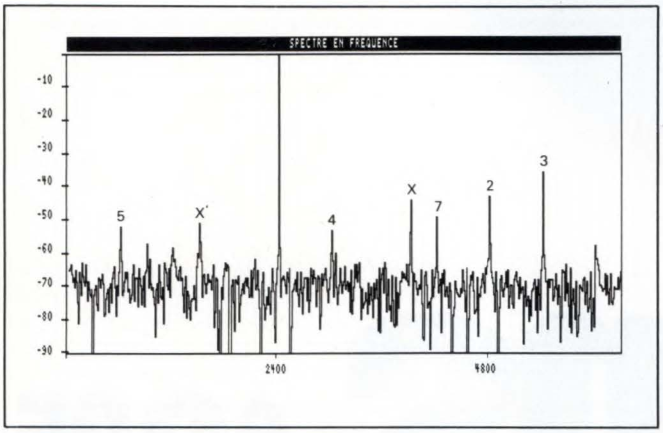


Fig 1—This FFT of an A/D converter's output *has some spectra, X and X′, that indicate a bad converter, buried among other, out-of-order spectra.*

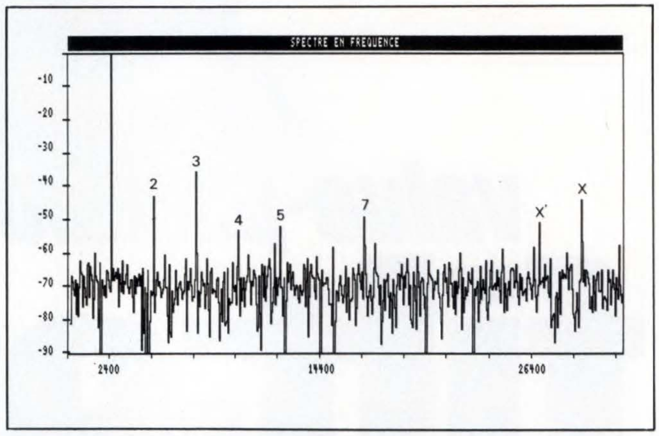


Fig 2—After performing the artifical-oversampling *transformation of the A/D converter's output, a second FFT unrolls the spectrum and isolates the error components clearly.*

Single MACD performs IIR filtering

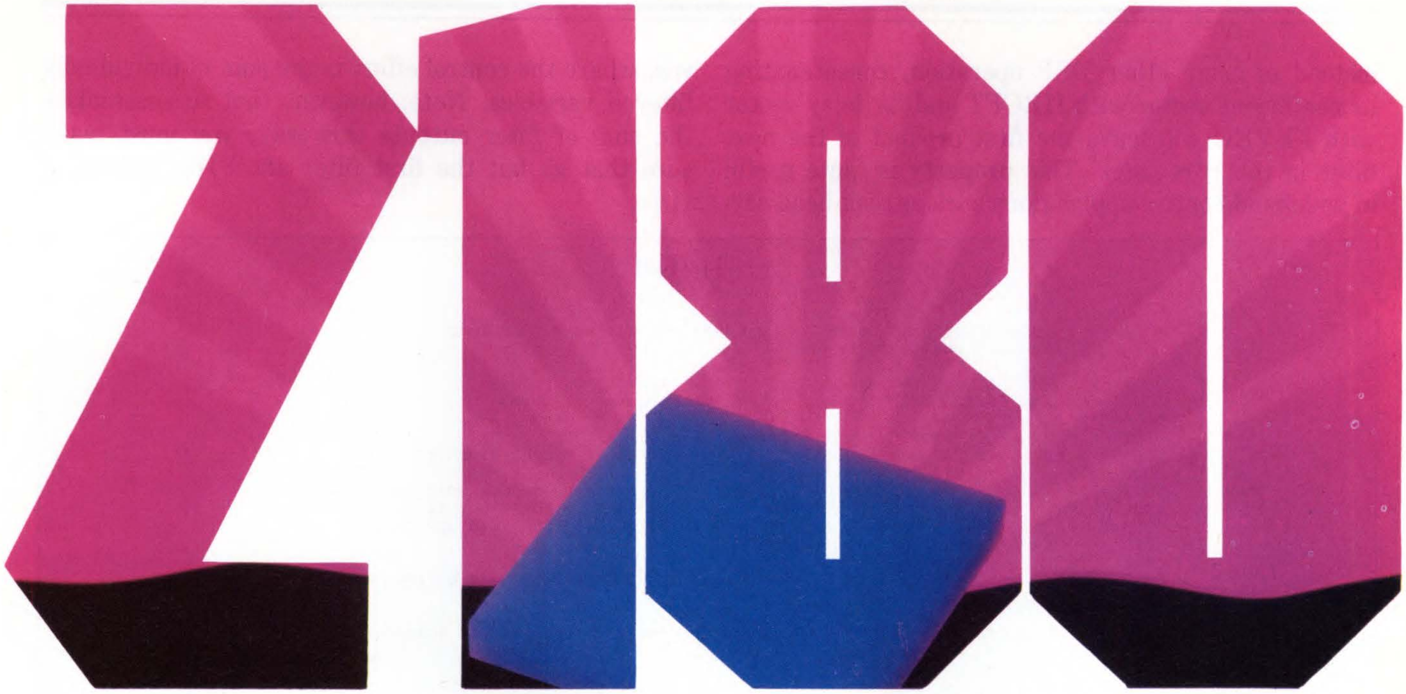
Richard H Neubert
Vermont Research Corp, North Springfield, VT

By concatenating your data vectors, you can program the TMS32020 DSP chip to perform an IIR-filter calculation using only one MACD instruction; the IIR filter can have an arbitrary number of poles and zeros. You need to set up the chip's multiplier, accumulator, and repeat counter only once for each execution of the filter. Assuming you have preinitialized the CNF, SXM, and OVM bits in the status register (you can initialize the ARP bit with the CALL instruction), the subroutine in **Listing 1** will execute an IIR filter with two poles and two zeros in 18 cycles (3.8 μsec at 5 MIPS).

To use only a single MACD instruction in your filter loop, you must make sure the filter output is also the feedback value. You can concatenate the two delay vectors in any order; however, you must store the filter coefficients in the reverse order of the corresponding input-vector elements, because the DMOV operation in the MACD instruction addresses them in reverse order. Using the order for INPVEC shown in **Listing 1**, the DMOV operation on the last word of INPVEC overwrites the first word in FBVEC and the first word in FBVEC, and then is rewritten after the MACD loop. Likewise, the word at the beginning of INPVEC, which the last execution of the MACD loop overwrites, is rewritten at the beginning of the next filter operation with the new input sample.

The last execution of the MACD loop leaves, in the P register, the product of JUNK0 multiplied by the last word of IIRCFT. Setting the coefficient to 0 conveniently clears the multiplier for the next calculation, if necessary. If the next calculation is another filter

Z I L O G



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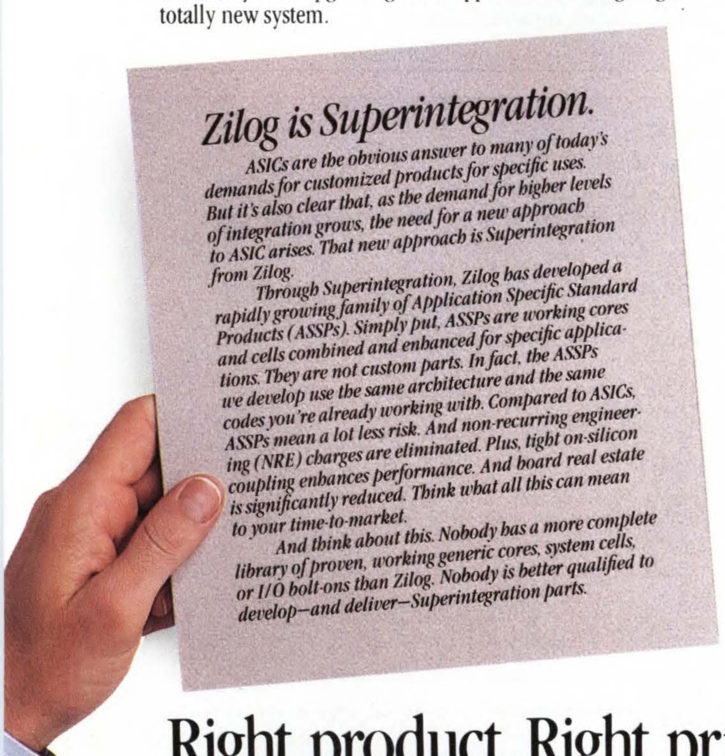

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CIRCLE NO 203

instead of some other DSP operation, concatenating its coefficient vector with IIRCFT and its delay vector with FBVEC will leave the first product of the next filter in the P register. This property is quite useful in wideband control applications such as disk-head servos, where the control effort is the sum of individually filtered variables. Note, however, that to accumulate the sum of filter outputs this way, you must make sure that all but the first filter are FIRs instead of IIRs.

LISTING 1

```
          TMS32020 program to perform an IIR with a single MACD loop
          Feedback coefficients are Q14.

          0002 NPOLES EQU  2                 (number of poles)
          0002 NZEROS EQU  2                 (number of zeros)
               *
          0006 VECPAG EQU  6
          0300 VECPAD EQU  >300              Internal memory block B1
0000                  DORG 0
0000           JUNKO  BSS  1                 An internal memory word for last MACD
0001           INPVEC BSS  NZEROS+1          Delay line for input data
0004           FBKVEC BSS  NPOLES            Delay line for feedback data
          0005 IIRLEN EQU  $-INPVEC
          0005 VECEND EQU  $-1
0006           JUNK1  BSS  1                 Catches data DMOV'd by 1st MACD.
               *
               *
               *      Coefficient storage in block B0 (use TBLW to initialize):
               *      All Q15.
               *
FF00                  DORG >FF00             Internal memory block B0
FF00           IIRCFT BSS  IIRLEN+1
               *
               *                        IIR FILTER SUBROUTINE
               *
0400                  AORG >400              (subroutine start address)
               *
0400 C806      FILTR1 LDPK VECPAG            Call with ARP=AR1, SXM, CNFP and Overflow Mode.
0401 6901             SACH INPVEC,1
0402 CA00             ZAC                    ACC := 0
0403 A000             MPYK 0                 P := 0
0404 CE09             SPM  1                 Select 1 bit left
0405 D100             LRLK AR1,VECPAD+VECEND       shift (for Q14 feedback coefficients)
0406 0305
0407 CB05             RPTK IIRLEN            Note, 1 extra cycle to accomplish final APAC.
0408 5C90             MACD IIRCFT,*-
0409 FF00
040A 6904             SACH FBKVEC,1          Store feedback value, replacing data DMOV'd
               *                             from INPVEC.
040B CE26             RET                    Output value returns in ACC.
NO ERRORS, NO WARNINGS
```

LISTING 2

```
          Same subroutine with Q15 feedback coefficients
          First coefficient must be reduced by 1.

0400 C806      FILTR2 LDPK VECPAG            Call with ARP=AR1, SXM, CNFP and Overflow Mode.
0401 6901             SACH INPVEC,1
0402 A000             MPYK 0                 P := 0
0403 2F04             LAC  FBKVEC,15         ACC := 1 * FBKVEC[0]
0404 CE08             SPM  0                 Select 0 shift (for Q15 feedback coefficients)
0405 D100             LRLK AR1,VECPAD+VECEND
0406 0305
0407 CB05             RPTK IIRLEN            Note, 1 extra cycle to accomplish final APAC.
0408 5C90             MACD IIRCFT,*-
0409 FF00
040A 6904             SACH FBKVEC,1          Store feedback value, replacing data DMOV'd
               *                             from INPVEC.
040B CE26             RET                    ACC returns output value.
NO ERRORS, NO WARNINGS
               *                  Second section:
               *
040E 2F07             LAC  FBK2,15           ACC := 1 * FBK2[0]
040F CB03             RPTK IIRLEN-1          IIR2[0] term already in P from above.  Last MACD
0410 5C90             MACD IIR2+1,*-         copies output of 1st section to INP2[0].
0411 FF05
0412 6907             SACH FBK2,1            Store feedback value, replacing DMOV'd INP2[1].
               *
               *                  First section:
               *
0413 2F03             LAC  FBK1,15           ACC := 1 * FBK1[0]
0414 CB03             RPTK IIRLEN-1
0415 5C90             MACD IIR1+1,*-         IIR1[0] term already in P from above.
0416 FF09
0417 6903             SACH FBK1,1            Store feedback value, replacing DMOV'd INP1[1].
               *
               *
0418 CE04             CNFD                   Needed if block B0 is used elsewhere for data.
0419 2F0B             LAC  FBK3,15           ACC := Output from last section,
041A CE26             RET                          same scaling as input.
NO ERRORS, NO WARNINGS
```

You need not scale FBVEC and INPVEC identically. However, you must constrain the feedback vectors with scale factors such that the total shift from FBVEC back to itself is zero when the vectors are shifted with available P modes and output shifts.

In this design, as with any direct form of IIR realization, coefficient scaling can be a limitation for filters with more than two poles. You may have to add extra instruction cycles to handle the integer parts of some coefficients in order to scale them for the required precision—especially if your filter has low-frequency poles. You can reduce a stored coefficient by one if you change the ZAC instruction to LAC FBVEC,14. This change will effectively add the integer 1 to the first feedback coefficient. You can use this trick to permit Q15 scaling of feedback coefficients for 2-pole filters **(Listing 2)**. Note that in **Listing 2**, the Q15 scaling changes the required shift to 15 for the LAC instruction.

In some applications, such as speech synthesis, designers often cascade lower-order filter sections. If delay is not important, you can easily cascade filter sections if you use the value moved out of one FBVEC (by the DMOV instruction) as the input to the next INPVEC **(Listing 3)**. Note that the routine in **Listing 3** initializes AR1 and the multiplier only once for the chain of filters. Note also that the routine executes the low-order filter section in reverse order, and the outputs of all but the last section are taken from the ends of the feedback delay lines. This arrangement adds a propagation delay that's equal to the sample period times the total number of feedback taps (minus those in the last section), but minimizes execution time per sample. The memory requirements for code and data space are also minimal. **EDN**

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LISTING 3

```
                Example of cascading 3 IIR filter sections
                Feedback coefficients are Q15.

           *      For this example, number of poles and zeros in each section is the same.
           *      This is not a requirement.
           *
     0002  NPOLES EQU    2                Number of poles per filter section
     0001  NZEROS EQU    1                Number of zeros per filter section
     0003  NSECT  EQU    3                Number of filter sections
     0004  IIRLEN EQU    NPOLES+NZEROS+1  Length of each coefficient vector
           *
     0006  VECPAG EQU    6
     0300  VECPAD EQU    >300             Internal memory block B1
0000              DORG   0
0000       JUNK0  BSS    1                An internal memory word for last MACD
0001       INP1   BSS    NZEROS+1
0003       FBK1   BSS    NPOLES
0005       INP2   BSS    NZEROS+1
0007       FBK2   BSS    NPOLES
0009       INP3   BSS    NZEROS+1
000B       FBK3   BSS    NPOLES
     000C  VECEND EQU    $-1
000D       JUNK1  BSS    1                Catches data DMOV'd by 1st MACD.
           *
           *      Coefficient storage in block B0, all Q15.
           *      Use TBLW to initialize coefficients.  Should clear data memory also to
           *      avoid any large output transients on startup.
           *
FF00              DORG   >FF00            Internal memory block B0
           *
FF00       IIR3   BSS    IIRLEN           -b2, -b1-1, a1, a0       for 3rd section
FF04       IIR2   BSS    IIRLEN           -b2, -b1-1, a1, a0       for 2nd section
FF08       IIR1   BSS    IIRLEN           -b2, -b1-1, a1, a0       for 1st section
           *
FF0C       JNKOCF BSS    1          = 0 if desired to clear P reg. upon completion.
           *
           *
           *                        3 SECTION FILTER SUBROUTINE
           *
0400              AORG   >400             (subroutine start address)
           *
0400 C806  FILTR3 LDPK   VECPAG           Call with ARP=AR1.
0401 6901         SACH   INP1,1           Store input value in first input vector.
0402 CE07         SSXM
0403 CE05         CNFP                    Needed if block B0 is used elsewhere for data.
0404 CE03         SOVM
0405 CE08         SPM    0                Select 0 shift (for Q15 feedback coefficients)
0406 A000         MPYK   0                P := 0
0407 D100         LRLK   AR1,VECPAD+VECEND
0408 030C
           *
           *                        Start with last (3rd) section:
           *
0409 2F0B         LAC    FBK3,15          ACC := 1 * FBK3[0]
040A CB04         RPTK   IIRLEN           Note, extra cycle does final APAC, DMOV's output
040B 5C90         MACD   IIR3,*-          of 2nd section into INP3[0] and initializes
040C FF00
           *                              P reg. to FBK2[1] * IIR2[0].
040D 690B         SACH   FBK3,1           Store feedback value, replacing DMOV'd INP3[1].
           *
```

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Circuit divides by 2 or 3

Dinesh Venkat
Zymos Corp, Sunnyvale, CA

The circuit in **Fig 1** produces a symmetrical waveform when dividing by either 2 or 3. The Divide Select input controls the division factor. When Divide Select is high, flip-flops IC_1 and IC_2, along with associated gates, form the classical divide-by-3 circuit.

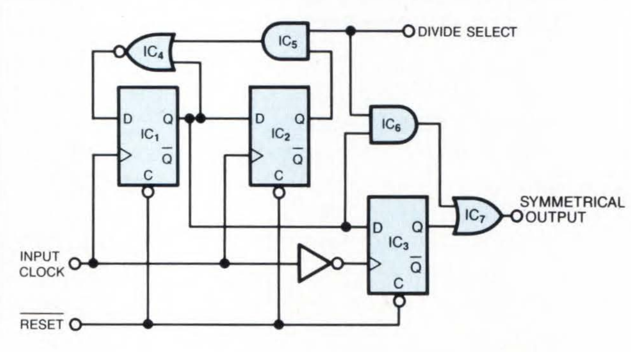

***Fig 1—This circuit produces selectable, symmetrical** divide-by-2 and divide-by-3 outputs.*

When Divide Select is low, however, the output of the And gate, IC_5, goes low. Consequently, the Nor gate, IC_4, inverts the feedback signal and passes it to the D input of the flip-flop, IC_1. Now IC_1 acts like a toggle flip-flip and produces a divide-by-2 output.

IC_3, which is in effect a negative-edge-triggered flip-flop, provides symmetrical output signals. When you select division by 2 (Divide Select is low), the output of And gate IC_6 is low, and IC_3 simply clocks out the divider's output delayed by one clock period. When you set Divide Select high, the path to the output through the And and Or gates, IC_6 and IC_7, is enabled. This path means that the output goes high on the leading edge of IC_3's input—not its output—producing a symmetrical divide-by-3 output. EDN

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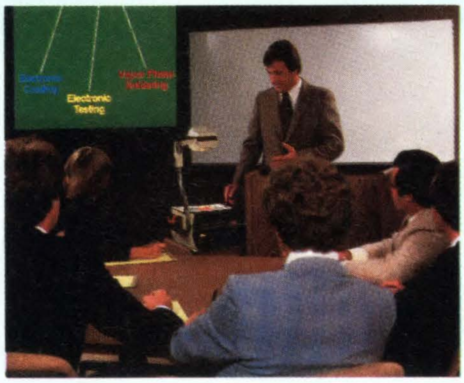
*Fluoronics Resources:

An exclusive 3M combination of innovative products backed by research and development, manufacturing expertise, technical data and service assistance built on more than 35 years' experience of pioneering in fluorochemistry.



3M has had a whole generation of experience in the development, manufacture and refinement of perfluorinated liquids. We first introduced these versatile liquids to electronics design, testing and production professionals in the fifties. Since then, Fluorinert Liquids have become the mainstays in electronic cooling, high reliability testing and vapor phase soldering.

Fluorinert Liquids, used as a direct contact heat transfer medium, offer a range of physical properties that make them particularly suitable for electronic uses. They are non-polar and exhibit no solvent action. They are colorless, low in toxicity, non-flammable and offer exceptionally high dielectric strength plus thermal and chemical stability. Most important, they have almost no chemical reactivity and they evaporate without leaving a residue on parts.

Buy the numbers

Our FC™ numbers — FC-40, FC-70, FC-77, etc. — are used to identify Fluorinert Liquids that offer certain physical characteristics to meet specific application needs. These FC numbers are solely 3M designations for various fluorochemical products.

Fluorinert Liquids are being used cost-effectively in cooling, high reliability testing and vapor phase soldering operations. When you are interested in applying these versatile liquids in your own production, 3M can provide an abundance of technical information and support.

Technical assistance: the main benefit of Fluoronics Resources

3M offers prompt assistance to help you solve many production and testing problems. We provide comprehensive technical recommendations for specific fluids. We consult with you on the proper application equipment and help you evaluate production methods and results. Our service bulletins bring you up to date on the most recent advances in vapor phase soldering and high reliability testing. Ask us about 3M's audiovisual materials and on-site application training seminars.

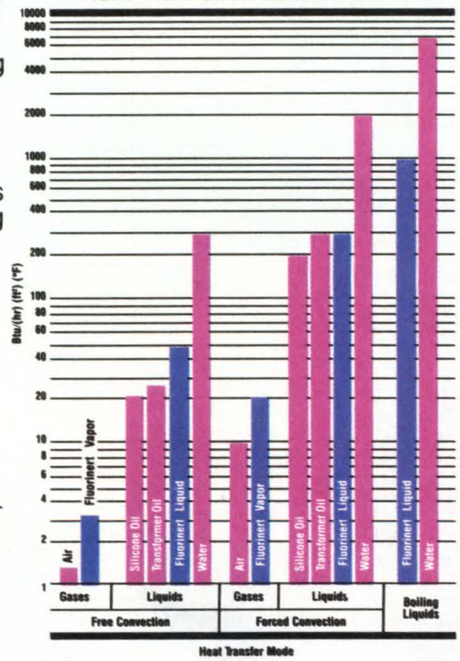
Discover Fluorinert™ Liquids' heat transfer capability

What are your needs? A precise degree of temperature control? Fast, uniform heat transfer? High dielectric strength? Fluorinert Liquids offer the broad range of physical characteristics required in most applications.

Fluorinert Liquids are an effective direct contact heat transfer medium whether used in a liquid or vapor state. Their unique properties enable you to use them in contact with sensitive components and substrates.

Major differences between the various products in the Fluorinert Liquids family can be seen in their boiling points. These can range from 56°C to 253°C. Should you need products with intermediate boiling temperatures, the 3M staff will work with you to fashion a product especially for your needs. It's an example of how 3M's Fluoronics Resources provide you with "customized" service to solve special problems.

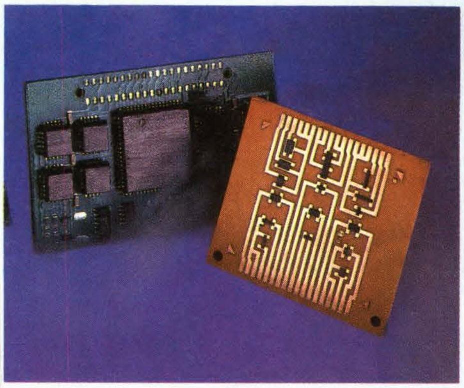
COMPARATIVE
HEAT TRANSFER COEFFICIENTS



Fluorinert™ Liquids achieve accurate high reliability testing

It's a small world you work in. Where time ticks in nanoseconds and dimension is measured in Angstrom units. And as circuitry becomes more complex, a greater demand is placed on testing capability — not only in speed, but in higher reliability and accuracy.

Fluorinert Liquids meet those requirements by providing a controlled temperature environment and a high degree of electrical protection. They offer maximum compatibility between



the heat transfer medium and the device under test. Fluorinert Liquids reduce testing costs by reducing testing time substantially. They do this by rapidly reaching test temperature and providing precise and uniform temperature control. You'll minimize the number of faulty units by detecting defects before they become rejects.

These liquids provide cost-effective tests such as gross leak, thermal shock, liquid burn-in, ceramic crack detection, electrical environmental, temperature calibration and failure analysis/short detection.

Fluorinert Liquids are specified in the MIL-STD's for thermal shock and gross leak testing.

THERMAL SHOCK TEST CONDITIONS

Military Standard 883-1011			Military Approved Fluorinert Liquids	
Test Condition	**Hot Test Step 1**	**Cold Test Step 2**	**Hot Test Step 1**	**Cold Test Step 2**
A	100°C	– 0°C	Water, FC-40	Water, FC-40, FC-77
B	125°C	– 55°C	FC-40, FC-70, FC-5311	FC-77
C	150°C	– 65°C	FC-40, FC-70, FC-5311	FC-77
D	200°C	– 65°C	FC-70, FC-5311	FC-77
E	150°C	– 195°C	FC-40, FC-70, FC-5311	Liq. N_2
F	200°C	– 195°C	FC-70, FC-5311	Liq. N_2

GROSS LEAK TEST CONDITIONS

	Military Approved Fluorinert Liquids		
Military Standards	**Indicator Fluids**	**Detector Fluids**	**Absorption Fluids**
MIL-STD 883-1014	FC-40, FC-43	FC-72, FC-84	Do not apply
MIL-STD 750-1071	FC-40, FC-43	FC-72, FC-84	FC-43, FC-75, FC-77
MIL-STD 202-112	FC-40, FC-43	FC-72, FC-84	Do not apply

Discover higher yields in vapor phase soldering

Fluorinert Liquids have been the industry's fluid of choice since the vapor phase reflow soldering (VPS) process was introduced in 1975. There are a number of good reasons for this universal acceptance. VPS with Fluorinert Liquids produces highly reliable solder joints. The system reduces reject rates, increases production, and lowers production costs. With Fluorinert Liquids, you can be assured that your products will never be exposed to a temperature higher than the selected liquid's boiling point. (See above)

You'll avoid those problems usually associated with other systems — shadowing, uneven heating, and overheating. The liquids are non-flammable. Their low surface tension helps them evaporate quickly from the work pieces without leaving a residue.

VPS with Fluorinert Liquids is especially suited for boards with high mass or complex geometries. The liquid vapors completely surround the assembly and penetrate remote recesses to heat all surfaces evenly. The vapors are 15 to 20 times heavier than air so they can be contained easily within the work area. The system offers an oxygen-free, non-corrosive environment to minimize rejects from oxidation contamination.

Some typical applications using Fluorinert Liquids in VPS include surface mounted leaded or leadless components, through-hole leads and wire-wrap pins, lead frame attachment, reflow of electroplated solder or tin and miscellaneous metal joining.

VPS SELECTION GUIDE

Fluorinert Liquid	Boiling Point	Typical Solders
FC-43	174°C/345°F	70 Sn/18 Pb/12 In 100 In 58 Sn/42 In 58 Bi/42 Sn
FC-70, FC-5311 FC-5312	215°C/419°F	63 Sn/37 Pb 60 Sn/40 Pb 62 Sn/36 Pb/2 Ag
FC-71	253°C/487°F	100 Sn 95 Sn/5 Ag 60 Pb/40 Sn

Discover the unique cooling benefits of Fluorinert™ Liquids

As the package size decreases, your need for more efficient heat dissipation increases in proportion. 3M Fluorinert Liquids are very efficient as a direct contact heat transfer medium, with the added advantage of having the high dielectric characteristics needed to meet stringent demands of the diversified electronics industry. We offer 11 liquids with boiling points that range from 56°C to 253°C.

These stable liquids allow you to maximize power density and miniaturize your package. Yet they reduce failure rates and increase reliability.

Fluorinert Liquids are used in such demanding applications as:
• Radar transmitters • Power supplies
• High voltage transformers • Lasers
• Radar klystrons • Computer modules
• Computer memories • Fuel cells

Typical properties of Fluorinert Liquids used in cooling are:

Fluorinert Liquid FC-77 (English Units)	Liquid		Vapor
	Room Temp. (77°F)	**Boiling Point (207°F)**	**Boiling Point 207°F @/ATM**
Density lb./ft³	111	100	0.85
Thermal Conductivity Btu/(hr) (ft^2) (°F/ft)	0.037	0.033	0.008
Specific Heat Btu/(lb.) (°F)	0.25	0.28	0.23
Viscosity c.p.	1.42	0.46	0.02
Coefficient of Thermal Expansion $ft^3/(ft^3)$ (°F)	0.0008	0.0009	0.0015

Discover heating/curing with Fluorinert™ Liquids

Because they maintain their vapor temperature with absolute precision, Fluorinert Liquids can be used in many heating and/or curing operations. They serve as heat transfer media in solder mask and polymer thick film applications and for polymer processing. The non-corrosive vapors will not support oxidation. Ideal where solvent flash-off is a problem.

3M

Discover Fluoronics Resources

3M presents a unique short course in the use of Fluorinert™ Liquids for the electronics industry.

3M is now offering a series of "Applied Fluoronics" tapes demonstrating how Fluorinert Liquids are used in a number of applications. See first hand how these remarkable products can improve overall electronic production.

Three cassettes are available:

1. "Applied Fluoronics: High Reliability Testing"
2. "Applied Fluoronics: Vapor Phase Soldering"
3. "Applied Fluoronics: Direct Contact Cooling"

These informative VHS format tapes are available to qualified personnel in the electronics industry. Specify which cassette(s) you would like to view.

Write on your company letterhead, describing your general interest. Mail to: Fluoronics Resources, Industrial Chemical Products Division/3M, Building 223-6SE-04, 3M Center, St. Paul, MN 55144-1000.

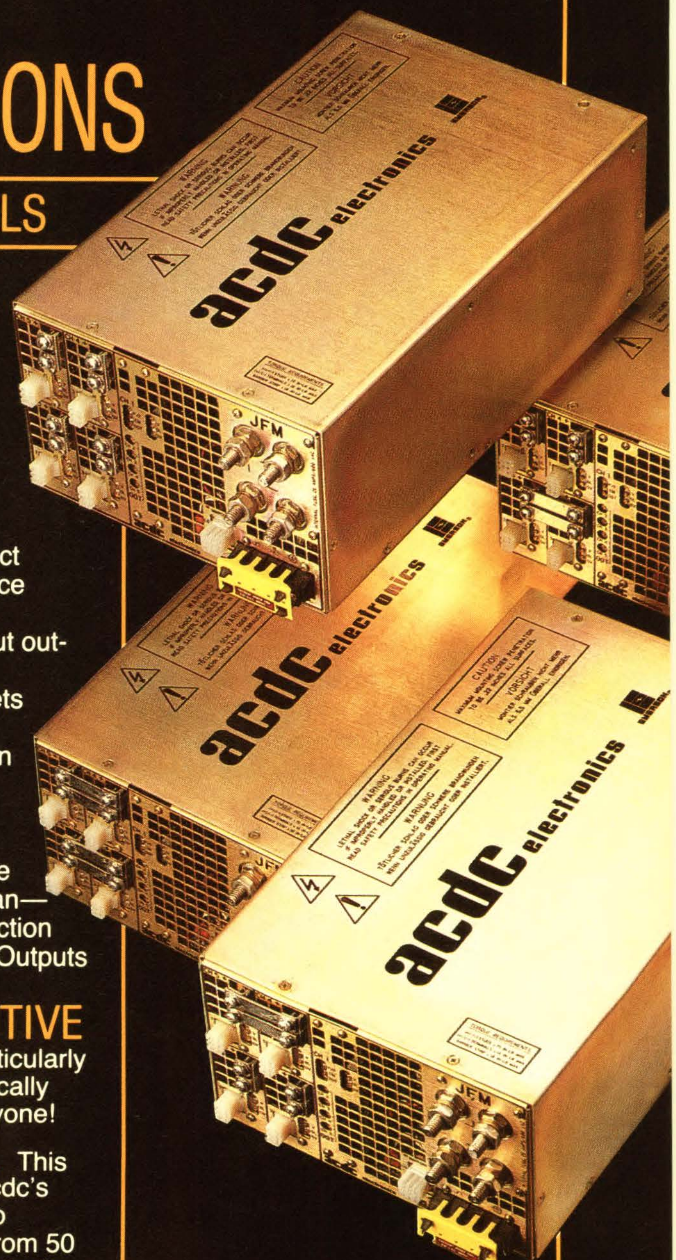
For technical information or assistance on High Reliability Testing and Cooling, call 612/733-6282; for Vapor Condensation Heating assistance, call 612/733-7424.

3M

CIRCLE NO 208

THE ONLY 1600w POWER SUPPLY WITH UNLIMITED OUTPUT VOLTAGE COMBINATIONS

AND FULL SAFETY AGENCY APPROVALS



THE MOST FLEXIBLE

The most Flexibility? Absolutely!

Check out these charts for the output configurations available:

1600w MULTI

MAIN OUT	CH2	CH3	CH4	CH5
5V/200A	A or B	A or B		
5V/200A	A or B*	B	A or B*	
5V/200A	B	B	B	B

**Table A may be used for one channel only (CH2 or CH4)*

TABLE A AUX'S	TABLE B AUX'S
5V/60A	5V/30A
12V/30A	12V/15A
15V/24A	15V/12A
24V/15A	24V/7.5A

If your needs change during the design phase you can still use the same power supply—with different output voltages. If your system is upgraded - this supply can accommodate almost any new voltage or current requirements.

MOST RELIABLE

Reliability is our forte. This unit passed MIL STD 810C Shock and Vibration tests; Design Maturity and Life Testing; and 24 Hrs. Burn-In.

And meets FCC 20780, part 15, Level A for EMI.

And complies with MIL I 45208A Quality Standards.

UNBEATABLE FEATURES

- UL/CSA/VDE Approvals
- Current Mode Control
- Electronic Soft Start
- 100% Computer Final Tested
- Comprehensive Product Applications and Service Manual provided
- LED's to indicate output out-of-tolerance
- Internal EMI Filter meets FCC & VDE Class A
- Maintains full regulation at No Load
- Single-wire paralleling
- Current monitor
- 30 Ms holdover storage
- Ambient and locked Fan—overtemperature protection
- Independent Auxiliary Outputs

COST COMPETITIVE

This power supply is particularly cost effective and empirically cost competitive with anyone!

50w TO 1600w. This power supply extends acdc's product offering. We also feature a complete line from 50 to 1600 Watts including single and multi output units.

CALL . . . For more information call 619/439-4200. We have a nationwide network of Sales Engineers to answer your questions. Plus, a full color catalog of our entire product offering.

ACDC's POWER OFFERING

1600w 1500w 1000w 800w 750w 500w 400w 300w 220w 175w 135w 70w 40w 15w

acdc electronics

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TEL: 619/757-1880. TLX: 350227.
FAX: 619/439-4243

CIRCLE NO 75

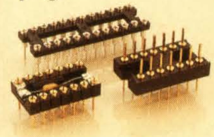
If your Samtec catalog looks like this...

You're in good company.

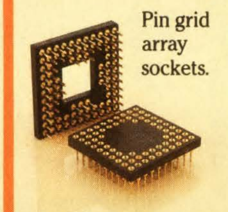
Our customers say our electronic interconnect catalog is one of the most informative, easiest-to-use in the industry.

And, after a short while, their Samtec catalog often looks as though the Samtec tiger had played with it. But there is help on the way. Our new enlarged 100-page catalog will make your job easier than ever. It has complete specs on every page...shows what parts mate with each other...includes more charts to determine board heights ...has conversion charts as well as a PGA cross reference guide. You'll find a full range of DIP sockets as well as the broadest line of strip connectors.

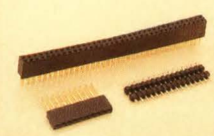
DIP Sockets, capacitor sockets, adaptor plugs.



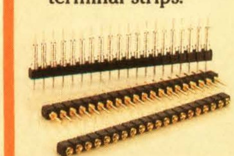
Pin grid array sockets.



Square post socket strips, board spacers.



Machined sockets, terminal strips.

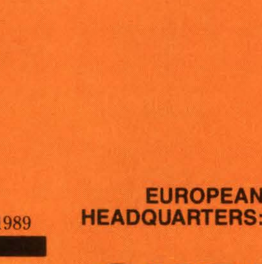


Shrouded IDC terminal strips, matching cable strips.

.025″ sq. terminal strips, single/double row shrouded.

Write or call today for a crisp, new 100-page Samtec catalog. We'll also include our New Interconnect Guide that provides valuable reference for the latest interconnect applications. Plus, Samtec's International Board-to-Board Inteconnect Selector—just off the press.

CIRCLE NO. 000



SUDDEN SERVICE really makes Samtec a different breed of cat!

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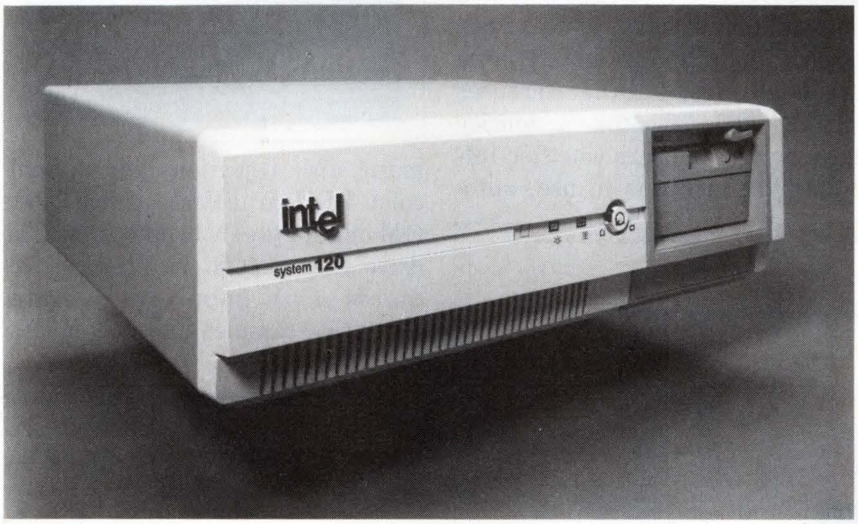
samtec SUDDEN SERVICE

WORLDWIDE HEADQUARTERS: **SAMTEC, Inc.** P.O. Box 1147, 810 Progress Blvd., New Albany, IN 47150 USA Phone: (812) 944-6733 TWX: 810-540-4095 TXL: 333-918 FAX: 812-948-5047

CIRCLE NO 176

COMPUTERS & PERIPHERALS



COMPUTER SYSTEMS

- *Run the iRMX II operating system on an IBM AT bus platform*
- *Applications are upgradable to Multibus I and II systems*

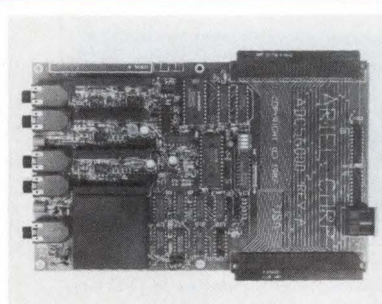
Based on the 80386 CPU, the System 120 family runs the iRMX II real-time operating system on the System 301, an IBM AT bus platform. You can upgrade applications developed on the systems to Multibus I- and II-based systems. The computers come in either a development- or target-system configuration. OEMs sell the target system after developing real-time applications and adding the appropriate peripherals. The development system comes with 2M bytes of RAM, a 40M-byte hard-disk drive, and a 360-byte floppy-disk drive. It also comes with a developer's tool kit consisting of compilers, a debugger, and a text editor. Target systems, from $3800 (50); development systems, from $9250.

Intel Corp, Dept W464, Box 58065, Santa Clara, CA 95052. Phone (800) 548-4725.

Circle No 351

ANALOG I/0

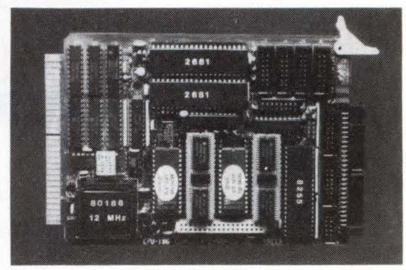
- *Board for Motorola's DSP56000 development system*
- *Has two 16-bit analog input and output channels*



The ADC56000 analog I/O board for Motorola's DSP56000 Application Development Module (ADM) features two analog input channels that feed differential input amplifiers. Each input channel has an adjustable gain stage (trimming potentiometer), an optional antialiasing filter, and an S/H amplifier. The antialiasing filter is an eleventh-order elliptic filter with a −3-dB cutoff frequency of 20 kHz. An analog multiplexer drives a 16-bit A/D converter with a 5-μsec conversion time. Two 16-bit D/A converters, which settle in 5-μsec, generate analog signals for two analog output channels. The interface for the input and output channels takes place through standard phone jacks. The board draws 1A from the system's 5V supply, and it develops the ±15V supplies for the analog ICs on board. The 9×6-in. circuit card connects to the ADM via a 96-pin right-angle connector. $995.

Ariel Corp, 110 Greene St, Suite 404, New York, NY 10012. Phone (212) 925-4155. TLX 4997279. FAX 212-966-3981.

Circle No 352



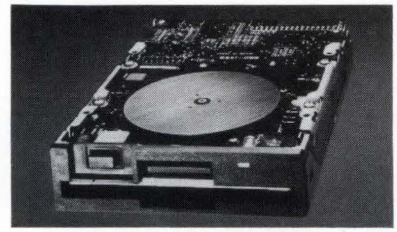
STD BUS SBC

- *Uses the Intel 80C186 CPU running as fast as 12 MHz*
- *Has as much as 512k bytes of battery-backed static RAM*

The CPU-186 single-board computer (SBC) for the STD Bus contains an Intel 80C186 CPU running at speeds as high as 12 MHz and providing as much as 512k bytes of battery-backed static RAM. The card also contains space for as much as 256k bytes of EPROM that lets you download an MS-DOS program from a PC. The program can be debugged on the SBC, using the PC console. In addition, the board has 24 parallel I/O lines, 4 RS-422/485 channels, an SBX interface, a watchdog timer, a battery-backed real-time clock, and 4 counter/timers. The board uses 100% CMOS construction to minimize power drain. A daughter board is also available with an 8087 math coprocessor. $476.

Computer Dynamics Inc, 107 S Main St, Greer, SC 29651. Phone (803) 877-8700.

Circle No 353



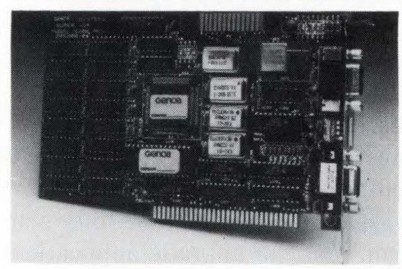
3½-IN. DISK DRIVE

- *Can withstand a nonoperating 60g shock test for 11 msec*
- *The drive uses 1M- or 2M-byte microfloppy media disks*

The MD3611 3½-in. microfloppy disk drive can withstand severe shock environments. The drive can withstand a 60g shock test for 11 msec. It has an oil-damping mechanism, which hydraulically cushions the head and increases reliability. A dual operating mode, which uses phase-correction circuitry and a wide gap-length head, lets you use both conventional 1M- and 2M-byte microfloppy disks. Other features include a dust shutter, a density sensor to inform users whether 1M- or 2M-byte media is in use, automatic disk rejection, and a dual-color LED to indicate which mode (1M or 2M byte) is in operation. The drive uses CMOS circuitry and requires a 5V supply to operate. Evalution samples and documentation, $100.

Canon USA Inc, Components Div, 1 Canon Plaza, Lake Success, NY 11042. Phone (516) 488-6700, ext 4958.

Circle No 354



VGA BOARDS

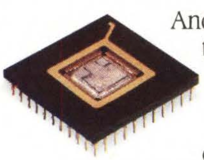
- *Are EGA, CGA, MDA, MCGA, and Hercules compatible*
- *Can interface with multifrequency and analog monitors*

The SuperVGA and the SuperVGA HiRes are two video-graphics-array (VGA) boards for IBM PS/2 computers. Both cards feature complete hardware and BIOS to support VGA and EGA operation. In addition, the cards support the MCGA, CGA, MDA, and Hercules standards. They also have CGA double-scan capability and come with utility software. Each board has connectors for interfacing with TTL multifrequency and analog monitors. They have 10 text modes for spreadsheet and desktop publishing applications, including 80×66, 100×75, and 132×60 resolutions. The SuperVGA HiRes has a resolution of 1024×768 pixels with 16

Text continued on pg 266

First You Dress Like An Engineer...

...Then You Climb Aboard The Real Time Express.™



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Harris' Real Time Express™ offers you microcontroller integration and RISC processor speed – 15 MIPS (typical) at 10 MHz – all for a fraction of the power dissipation of conventional designs.

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HARRIS
SEMICONDUCTOR

CIRCLE NO 107

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You have been warned... the Model 1281 from Datron is so good, it's hard to resist!

The 1281 is the world's most advanced DMM of its kind; bringing you the ultimate in electrical measurement via its accuracy, functional capability and ease of use.

Take advantage of user selectable resolutions up to 8½ digits backed up by accuracies and repeatabilities to suit the longest scale length. And DCV performance from 10nV to 1000V with 1 year specifications to ±3ppm, coupled with true RMS ACV providing 1 year accuracies of ±80ppm. High accuracy resistance, current and ratio measurements are also yours with this superb instrument.

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For more information, call us today. Our fact filled 1281 brochure will take you through, detail by detail, specification by specification, the world's most advanced DMM.

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Suffern, N.Y. (914) 357-5544

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Norwich (0603) 404824

datron
INSTRUMENTS
A WAVETEK COMPANY

colors and 512k bytes of video memory, and it is compatible with IBM's 8514 monitor. The SuperVGA offers 640×480- and 800×600-pixel resolution with 16 colors and 320×200- and 512×512-pixel resolution with 256 colors. The SuperVGA, $445; the SuperVGA HiRes, $645.

Genoa Systems Corp, 75 E Trimble Rd, San Jose, CA 95131. Phone (408) 432-9090. TLX 172319. FAX 408-434-0997.

Circle No 355

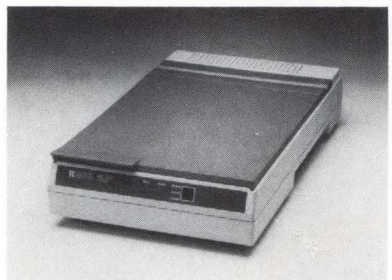


IMAGE SCANNER

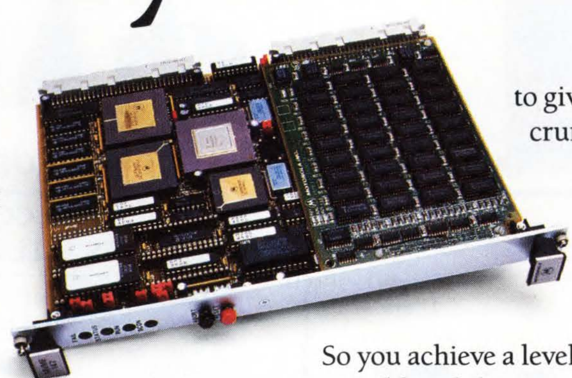
- *Provides resolutions from 60 to 360 dots/in.*
- *Scans a document at 18 sec/page for 300 dots/in.*

Capable of scanning sheets, cards, or books at resolutions ranging from 60 to 360 dots/in., the RS320 desktop scanner can scan a letter-size document at 18 sec/page with 300-dot/in. resolution. It can scan US letter-size and index-card-size papers as well as international A4, A5, B5 and B6 formats. You can designate variable-size scanning in either millimeters, or bytes and line counts. The unit has a bidirectional Centronics interface and a recommended service life of five years or 30,000 scannings. The unit occupies 11.4×19.5 in. of desktop space, stands 3.7 in. tall, and weighs 13.2 lbs. $1100. PC Interface Kit, including PC software, an interface board for the IBM PC computer, and a cable, $395.

Ricoh Corp, 5 Dedrick Pl, West Caldwell, NJ 07006. Phone (201) 882-2077. FAX 201-882-2506.

Circle No 356

"Their new 030 board isn't really a single-board computer. It's a single-board system."



OEMs weren't prepared for the level of *functionality* our new MVME147 processor module delivers. On one standard VME card, it packs virtually all the functions you need to build a small, multi-user system.

How? Mainly through ASICs like the single-chip VMEbus interface and Peripheral Channel Controller. Plus high-density on-board DRAM (4 or 8 Mbytes), SCSI interface and Ethernet chip set. To even come close in functionality, it would take as many as *five* conventional modules.

Besides which, the 147 outperforms everything in sight. It takes maximum advantage of Motorola's new 32-bit MPU—the MC68030—coupled with a floating-point coprocessor. Both running at up to 25 MHz, to give you outstanding number-crunching power.

And since the 147 features both UNIX® and real-time operating system support, you can plug it into your existing 020-based architecture and software base. So you achieve a level of integration never before possible, while protecting your existing investment. All of which gives you unprecedented price/performance advantages for just $3747 in OEM quantities of 100.

To get an idea of what the future of VME looks like, call us today—toll free: 1-800-556-1234, Ext. 230; in California, 1-800-441-2345, Ext. 230. Or write: Motorola Microcomputer Division, 2900 Diablo Way, Tempe, AZ 85282.

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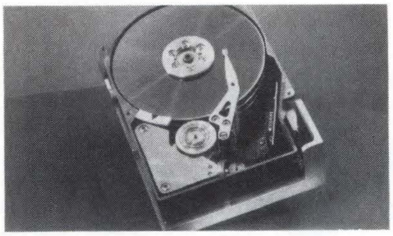


3½-IN. DISK DRIVES

- *Offer 44M to 110M bytes of formatted capacity*
- *Come with ST406, AT, ESDI, and SCSI ports*

The models 5100, 6100, and 7100 are three members of a 5-member family of 3½-in. disk drives with ESDI, SCSI, and AT ports, respectively. They provide 110M bytes of formatted capacity on four platters and seven recording heads. The drives can handle data-transfer rates to 10M bps. The 7040 and 4050 are the other two members of the family with 47M and 44M bytes of formatted capacity, respectively. The 7040 has an AT interface and uses two platters; the 4050 has an ST506 interface and uses three. All the drives have average access times of less than 18 msec. The entire head disk assembly of each drive, including the in-hub spindle, is shock-mounted to withstand a non-operating shock of 75G. Each drive has an MTBF of 36,000 hours. $650 to $1295.

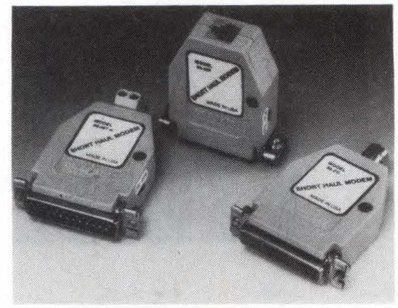
Microscience International Corp, 305 N Mathilda Ave, Sunnyvale, CA 94086. Phone (408) 730-5965.

Circle No 357

MODEMS

- *Operates full duplex at 19.2k bps over a 1500-ft cable*
- *Can also operate at 9600 bps over a 2500-ft cable*

The 86T/P/C Series short-haul modems provide full-duplex communications over a single pair of wires



or a single coaxial cable. They can operate at 19.2k bps over a distance as long as 1500 feet. In addition, they can operate at 9600 bps over a distance as long as 2500 feet. Each modem has a DTE/DCE switch that allows you to reverse pins 2 and 3 on an RS-232C connector. The 86T has screw terminals for connecting a 2-wire line, and the 86P has an RJ-11 modular connector. The 86C has a coaxial connector that lets you use coaxial cable in place of the wires. The units receive their operating power through any available

Text continued on pg 272

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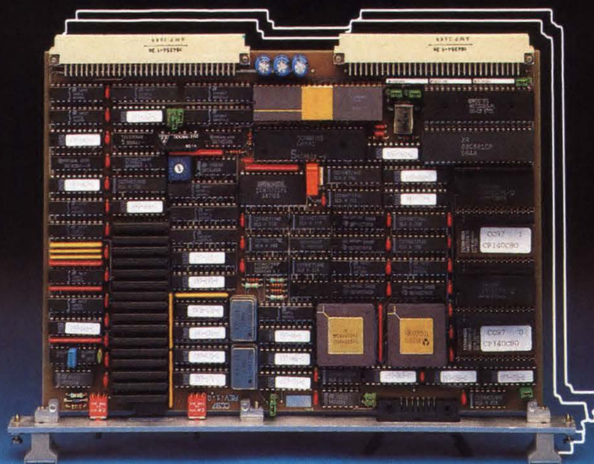
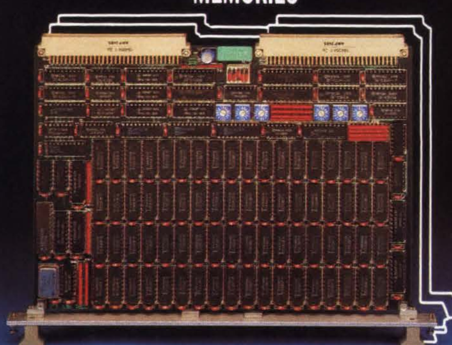


68000 - 68010 - 68020 - 68030 - specials

MEMORIES



EPROM, SRAM and DRAM upto 16 Mbyte

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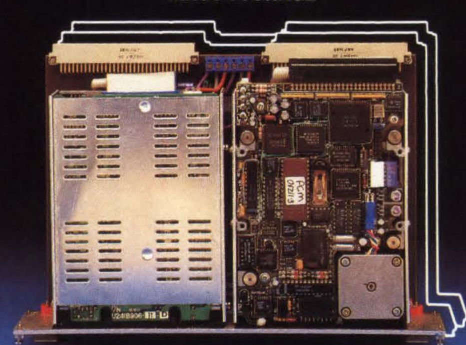

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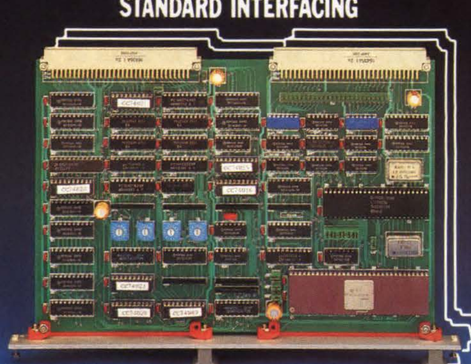

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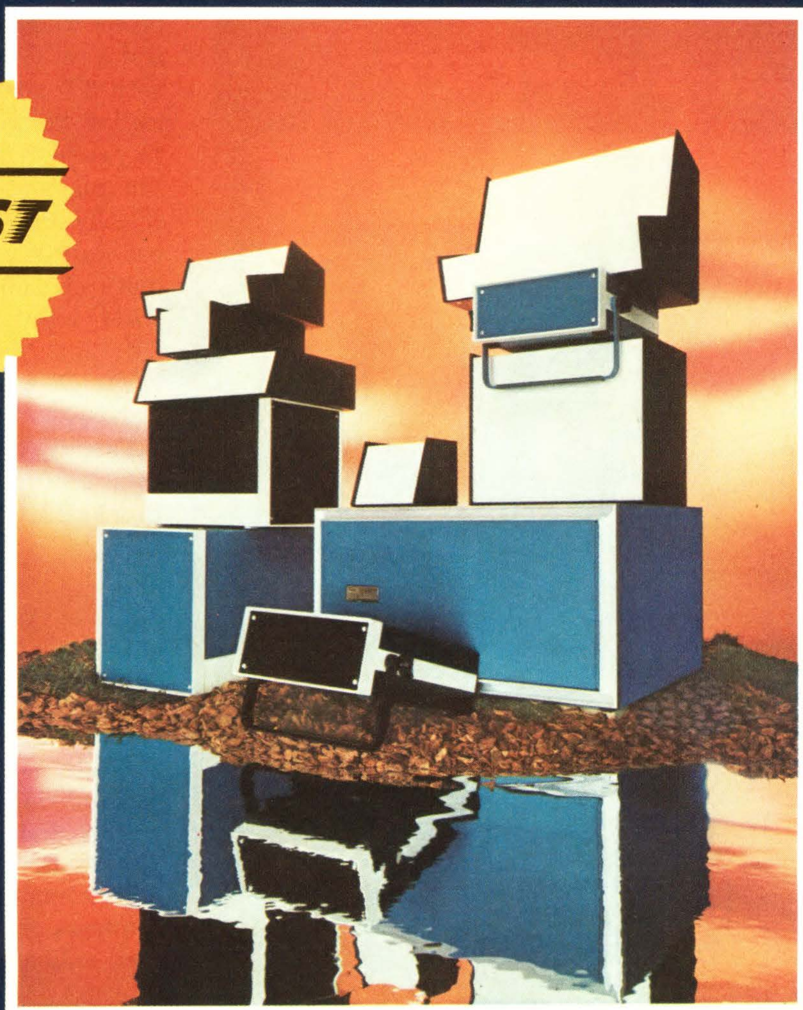

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CIRCLE NO 80

control pin on the RS-232C connector. The modems come in a DB-25 connector hood, and you can order them with a male or female RS-232C connector. $58 (100).

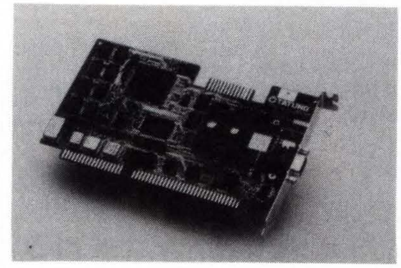
Telebyte Technology Inc, 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (800) 835-3298; in NY, (516) 385-8080.

Circle No 358

VGA CARD

- *VGA register-compatible with IBM PC systems*
- *Guaranteed software compatibility*

The Tatung VGA card for IBM PC, PC/XT, and PC/AT computers is 100% VGA register compatible, according to the vendor. It's compatible with OS/2 and MS-DOS and



provides a resolution of 800×600 pixels with 16 simultaneous colors and a resolution of 640×400 pixels with 256 simultaneous colors. The card works with all VGA analog displays and multifrequency monitors. The manufacturer provides a specifically stated 1-year parts and labor warranty period. The card also features 256k bytes of dynamic RAM, 16-bit access to memory and I/O, and compatibility with the EGA, CGA, MDA, and Hercules standards. $399.

Tatung Company of America Inc, 2850 El Presidio St, Long Beach, CA 90810. Phone (213) 979-7055.

Circle No 359

DIAL-UP MODEM

- *Handles 19,200-bps communication over phone lines*
- *Conforms to PEP 2, V.22bis, V.22, and Bell 212 specs*

The 736DSP dial-up modem provides communication between synchronous or asynchronous devices over ordinary phone lines. It can transmit data at a speed of 18,000 bps without data compression. It also can transmit at 19,200 bps using the Pacetized Ensemble Protocol 2 (PEP 2), which organizes the telephone bandwidth into hundreds of channels. In addition, the modem supports the V.22bis, V.22, Bell 212A, and Bell 103L protocols. The modem has a provision that supports the SDLC protocol for high-speed communications over an IBM Systems Network Architecture network. The Microm Networking Protocol from Microcom provides error detection and correction. The unit also runs under communication software such as Kermit, UUCP, Xmodem, and Ymodem. It is available in either a rack-mount or stand-alone version. $1495.

ITS Inc, 9 Heritage Oak Lane, Battle Creek, MI 49015. Phone (800) 999-9487.

Circle No 360

LAN CARD

- *Handles IEEE-802.3 TCP/IP locally*
- *Maximizes data throughput using dual-port RAMs*

The VLAN single-height, single-slot VME Bus board provides an IEEE-802.3 (Ethernet) LAN interface. The board is based on an AMD 7990 LAN controller and includes an onboard 68000 μP. The 68000, which runs the VIOXROM real-time multitasking operating-system kernel, handles the TCP/IP locally. Two 64k-byte dual-port RAMs, one between the μP and the LAN controller and the other between the μP and the board's VME Bus interface, maximize the board's throughput. Data transfer to or from host CPUs on the VME Bus is via a mailbox facility in the μP/VME Bus dual-port RAM. Mailbox interface software drivers are currently available for the OS-9/68k and PDOS 3.3 operating systems. Link-level access, TelNet, and file-transfer protocol are available as options. The board has a 15-pin attachment-unit interface for connection to the LAN. You can add a media-attachment unit for Ethernet or Cheapernet. DM 4500 (OEM qty).

Pep Modular Computers GmbH, Am Klosterwald 4, 8950 Kaufbeuren, West Germany. Phone (08341) 81001. TLX 541233. FAX (08341) 40422.

Circle No 361

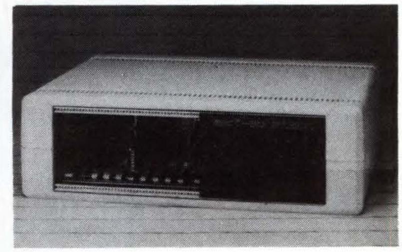
Pep Modular Computers Inc, Carnegie Office Park, 600 N Bell Ave, Pittsburgh, PA 15106. Phone (412) 279-6661. TLX 6711521.

Circle No 362

COMPUTERS

- *Provide 16- and 32-bit industrial μP systems*
- *Allow for system expansion using Eurobus boards*

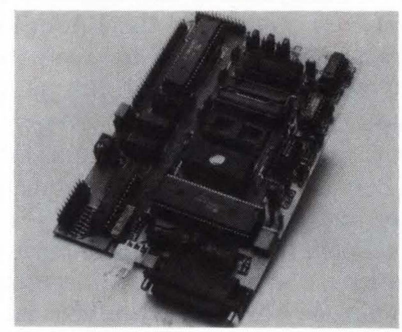
Using single-Eurocard computer boards, the 20800-EDS Series industrial computers are housed in 19-in., 3U-high enclosures. The basic computers run either a 16.7-



MHz 68020 32-bit μP and 68881 math coprocessor or a 12.5-MHz 68HC000 16-bit μP. They contain a minimum of 512k bytes of zero-wait-state RAM, two serial I/O ports, 40 TTL-level digital I/O lines, and a SCSI host-adapter interface. Standard mass-storage devices consist of a 40M-byte hard disk and a 5¼-in. floppy disk. For system expansion the computer has an 8-bit IIOC (intelligent I/O channel) backplane that accepts commercially available I/O boards. The OS-9 Professional operating system is supplied with the computer. DM 10,000.

EKF-Elektronik GmbH, Weidekampstrasse 1a, D-4700 Hamm 1, West Germany. Phone (02381) 12630. TLX 828621. FAX (02381) 15067.

Circle No 363



MICROCONTROLLER

- *Features a CMOS 64180 μP and 16k bytes of RAM*
- *Contains floating-point Basic in ROM*

The Vitrax stand-alone microcontroller card for digital control and data acquisition features a CMOS 64180 μP that runs Z80-compatible code. The single card contains floating-point Basic in ROM; as much as 16k bytes of EPROM for user code; 16k bytes of static RAM, which is expandable to 32k bytes; and a built-in EPROM programmer for code generation. In addition, the unit has 24 bidirectional I/O lines; two full-duplex asynchronous RS-

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Dynamic Range	96dB	96dB	96dB	108dB	90dB
Total Harmonic Distortion + Noise	−94dB	−92dB	−92dB	−100dB	−88dB
Conversion/Settling Time	350ns (I_{OUT}) 3μs (V_{OUT})	350ns (I_{OUT}) 3μs (V_{OUT})	350ns (I_{OUT}) 1.5μs (V_{OUT})	200ns (I_{OUT})	4μs
Packages	Plastic DIP	Plastic DIP, SOIC	Plastic DIP	Plastic DIP	Plastic DIP
Price*	$12.15	$10.90	$12.00	$31.80	$39.90

*U.S. prices only, in 100s.

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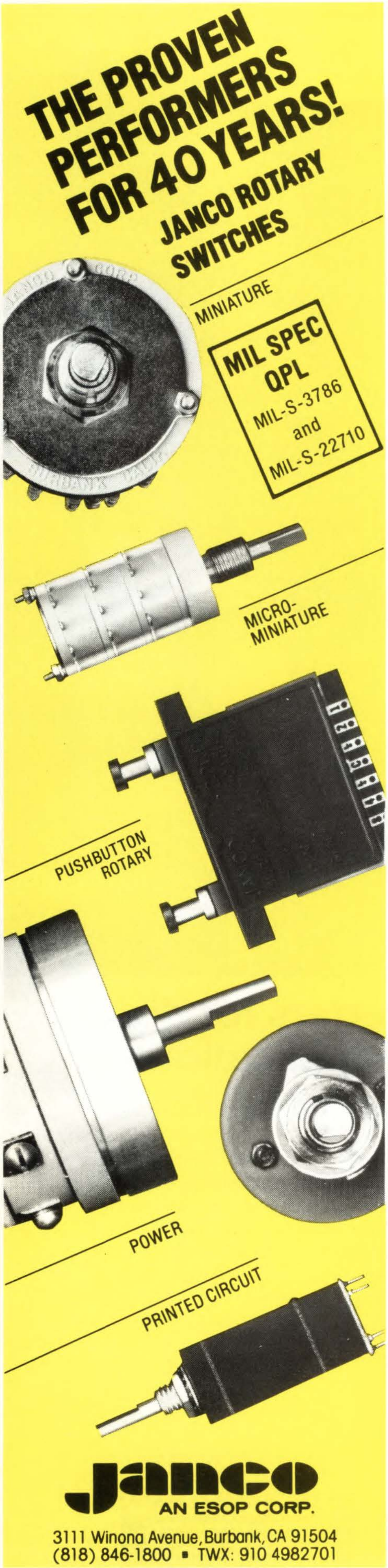
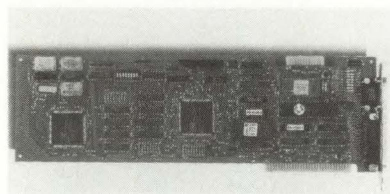
CIRCLE NO 83



232C channels that can communicate at 18.2k baud; a Centronics parallel port; and an 8-channel, 10-bit CMOS A/D converter. The unit contains a real-time calendar clock and operates from a 5V supply with <150-mA current drain. $295 including A/D converter and manual.

Sintec Co, Box 410, Frenchtown, NJ 08825. Phone (800) 526-5960; in NJ, (201) 996-4093.

Circle No 364



VGA CARD

- *Has an 8-bit connector that fits IBM PC/XTs and PC/ATs*
- *256k bytes of dynamic RAM with 120-nsec access times*

The PII-154A VGA card comes with an 8-bit connector that fits both the 8-bit and 16-bit slots of the IBM PC/XT and PC/AT, respectively. The card is designed around the VLSI chipset from Cirrus Logic to provide VGA compatibility at the register level. In addition to providing a 640×480-pixel resolution and a palette of 256k colors, the card is backward compatible with the EGA, CGA, MGA, MDA, and Hercules graphics standards. The board comes with 256k bytes of dynamic RAM with 120-nsec access times and three oscillator chips for the different frequencies of the various graphics modes. Interface ports include a DB-15 connector, a parallel-printer port, and a light-pen port. The board can perform flicker-free scrolling and split-screen imaging, and it's compatible with Windows, AutoCAD, and Symphony graphics modes. $375.

DTK Computer Inc, 15711 E Valley Blvd, City of Industry, CA 91744. Phone (818) 333-7533.

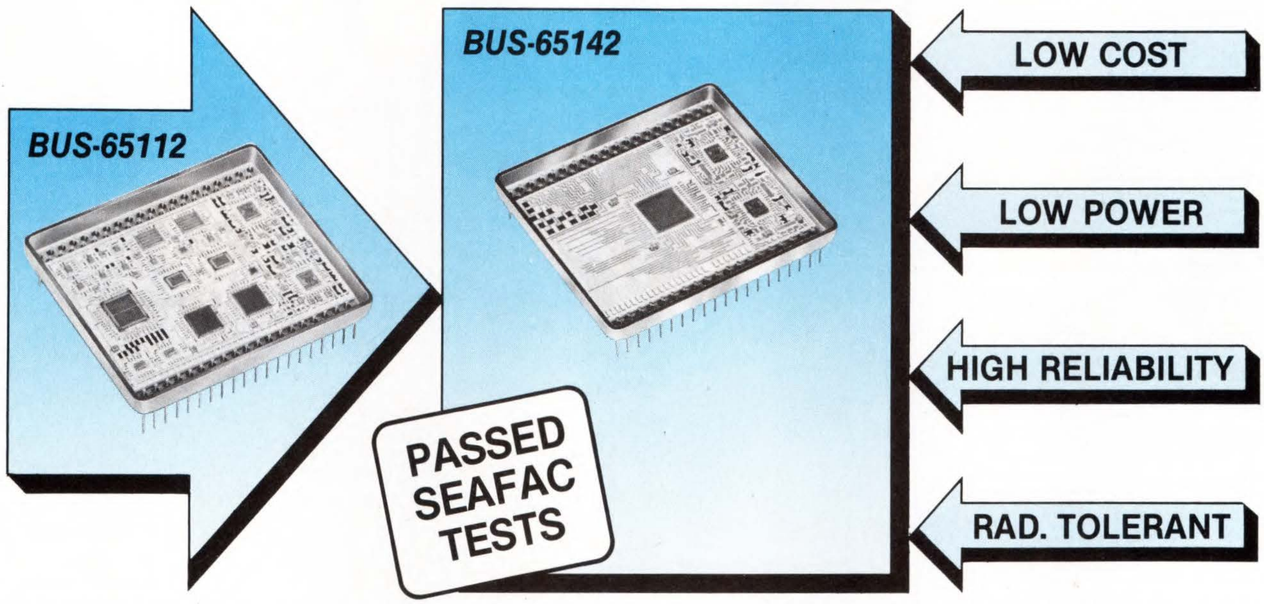
Circle No 365

DDC NEWS

ABOUT SYNCHRO-CONVERSION • A/D & D/A CONVERSION • 1553 BUS DEVICES • POWER & CUSTOM HYBRIDS

PUBLISHED BY **ILC DATA DEVICE CORPORATION** OCTOBER 1988

NEW LOW COST 1553B REMOTE TERMINAL HYBRID



DDC is pleased to announce the new, low cost BUS-65142 MIL-STD-1553B Dual Redundant Remote Terminal Hybrid featuring a single chip CMOS/SOS monolithic RTU protocol and Bipolar low power Mark II transceivers. Incorporating small size (1.9" x 2.1") with low power and high reliability, the low cost BUS-65142 is ideal for most MIL-STD-1553 applications requiring hardware or microprocessor subsystems.

The BUS-65142 supports 13 mode codes for dual redundant operation, any combination of which can be illegalized by an external prom.

Parallel data transfers are accomplished with a DMA type handshaking, compatible with most CPU types. Data transfers to and from memory are simplified by the latched command word and word count, outputs. Error detection and recovery are enhanced by BUS-65142 special features. A 14 bit built-in-test word register stores RTU information and sends it to the BUS Controller in response to the Mode Command Transmit Bit Word. The BUS-65142 performs continuous on-line wrap-around self-test and provides four error flags to the host CPU. Inputs are provided for host CPU control of 6 bits in the RTU Status Word.

The BUS-65142 is pin for pin compatible with the BUS-65112 which has been in production for over three years and has successfully passed the SEAFAC RT Validation Test Plan. The only difference in the parts is that the BUS-65142 uses a 16 MHz clock for decoding.

The 16 MHz decoders offer improved noise rejection and zero crossing detection tolerance.

The DMA interface is proportionally faster for the BUS-65142 since it uses a 16 MHz clock instead of the 12 MHz used on the BUS-65112.

The components incorporated in the BUS-65142 (low power MARK II Transceivers and CMOS/SOS Protocol Chip have passed the SEAFAC RT Validation Test Plan as part of the test performed on the BUS-61553 (Report Available).

In addition, since the transceivers are bipolar technology and the protocol chip is CMOS/SOS, this unit has radiation tolerance to Tactical Levels and also has excellent SEU (Single Event Upset) tolerance.

Learn how to improve your reliability with the smallest possible size RTU, all at a low cost, with the BUS-65142 from DDC. **For additional information call toll-free 800-DDC-1772.** □

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CIRCLE NO 117

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The Honeywell HFD3400 series are fiber optic receivers assembled in the new Fiber-DIP plastic housing. Our HFD3400 series also offers a wide product selection including:

- The HFD3401, an analog integrated receiver, DC to 35 MHz operation with a guaranteed minimum responsivity of 4mV/μW.
- The HFD3402, a differentiating integrated receiver, DC to 10Mbit digital data rates with a guaranteed sensitivity of 0.6 μW [−32 dBm]. The output is an inverted TTL level.
- And the HFD3403, a direct coupled integrated receiver, DC to 5Mbit digital data rates with a minimum guaranteed sensitivity of 2.8 μW [−25.5 dBm]. Again, the output is an inverted TTL level.

So remember, not only will you find our new Fiber-DIP series the one choice for a wide range of fiber optic transmitters and receivers–you'll also find us *the one choice for all your fiber optic needs.* That's because Honeywell Optoelectronics is one of the world's leading designers and manufacturers of fiber optic data communication components. With our proven track record and the experience of the over 100 year old, multinational Honeywell corporation you can rest assured we'll be there when you need us. Now. And in the future.

For additional information and data sheets of these products contact Honeywell Optoelectronics, 830 E. Arapaho Road, Richardson, Texas 75081. Or call **1-800-367-6786.** In Texas call 214-470-4271.

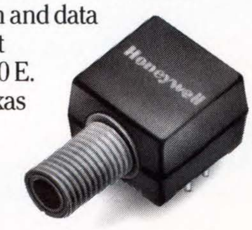

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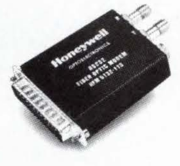
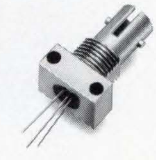
Photo Diodes	Photo Diodes		Photo Diodes	Photo Diodes





CIRCLE NO 112

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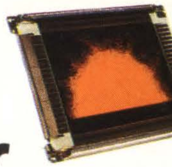

The only way our bright new 8050 display looks anything like the others is through a pair of sunglasses.

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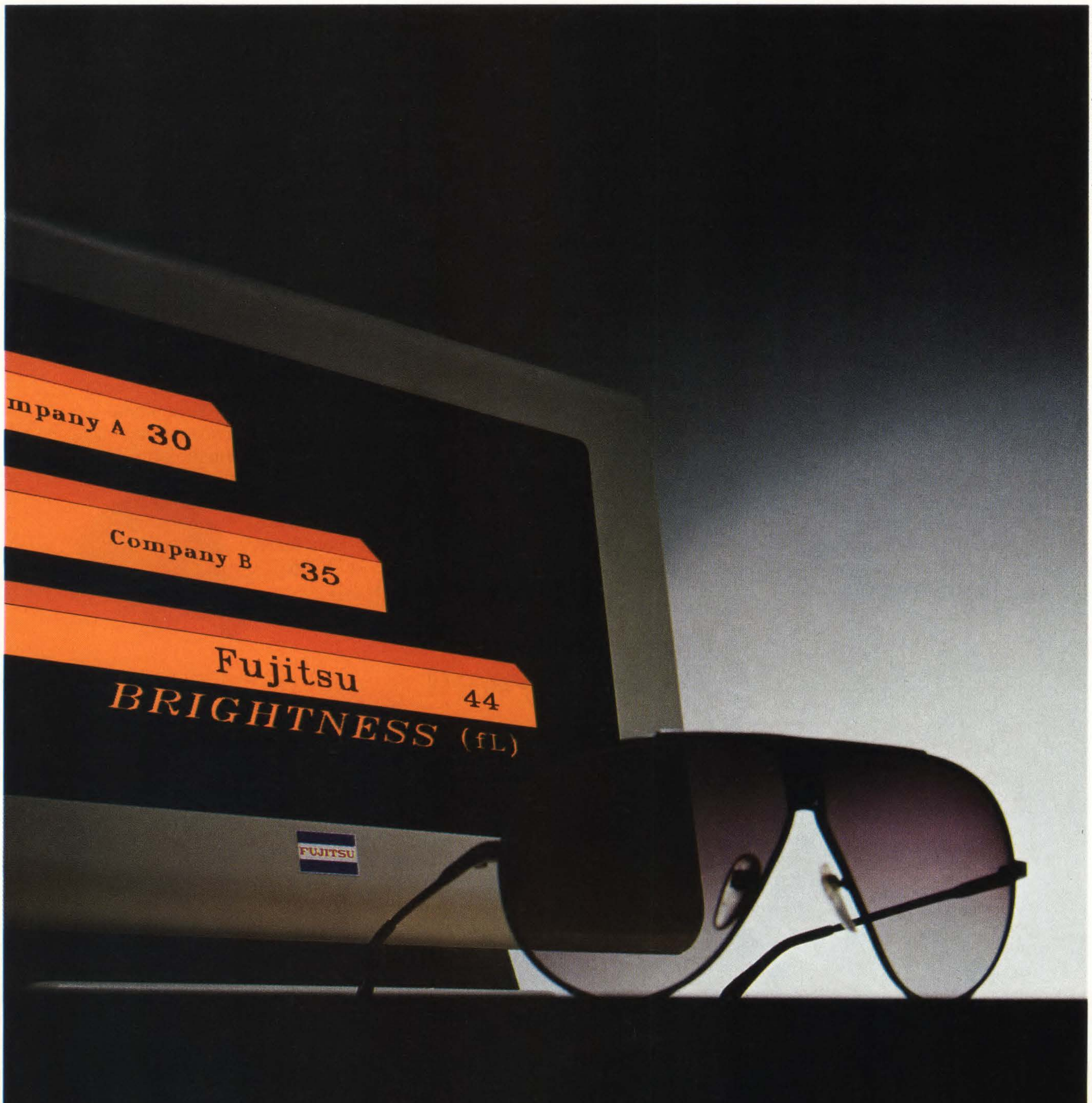
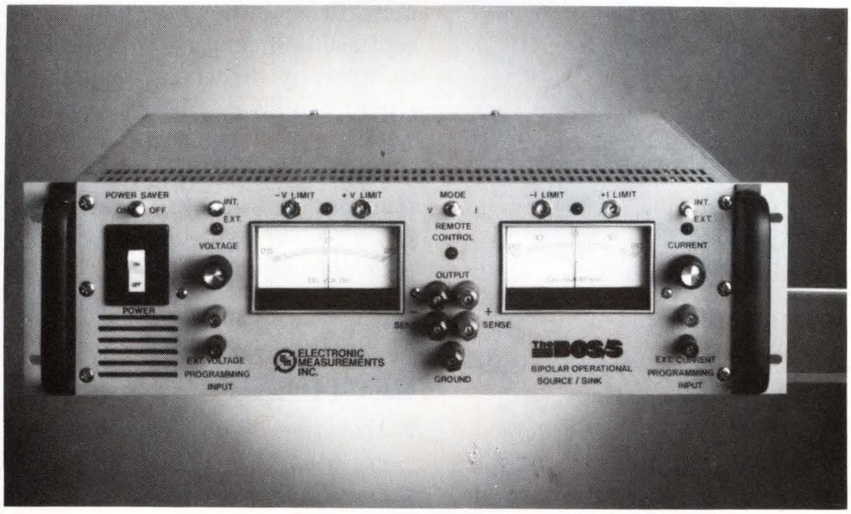


CIRCLE NO 244

POWER SUPPLY

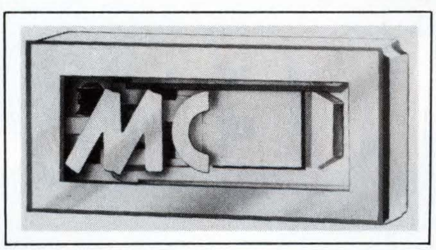
- *Provides more than a dozen functions*
- *Is programmable via IEEE-488 or RS-232C parallel buses*



The BOS/S performs the functions of dc power supply, electronic load, voltage source, power-pulse generator, current source, power-function generator, direct-coupled amplifier, variable-gain amplifier, fast-slewing power supply, dc amplifier, ac power supply, differential amplifier, and signal-invertering amplifier. The current or voltage output is controlled via a front-panel mode switch. Control may be internal or external. A 10-turn potentiometer controls the output over a min to max range. An external ±10 source provides identical external control. An optional digital control board allows you to program most of the units' functions via the IEEE-488 bus or an RS-232C parallel data-transfer bus. Talk and listen functions have 12-bit resolution. Voltage and current regulation is 0.005%. TC is 0.01%/°C in the voltage mode and 0.03%/°C in the current mode. RMS ripple equals 3 mV in the voltage mode and 0.05% in the current mode. Voltage and current output changes over 8 hours are 0.02 and 0.03%, respectively. Standard features include adjustable output limiting, indications of mode and remote operation, and analog or digital voltage and current meters. $1095 to $1995.

Electronic Measurements Inc, 405 Essex Rd, Neptune, NJ 07753. Phone (201) 922-9300.

Circle No 370



CRYSTALS

- *Withstand vapor-phase, IR, and wave-solder operations*
- *Feature an 8- to 35-MHz frequency range*

The CX-AT-HT, AT-cut, surface-mountable quartz crystal features an extended 8- to 35-MHz frequency range. The units can withstand vapor-phase, infrared, and wave-solder operations at temperatures to 260°C for 20 sec. Tolerances down to ±0.0005% are available. The units have a 5-ppm max aging rate and are available in versions that operate over −40 to +85 and −55 to +125°C. The hermetically sealed ceramic package is available in 16-mm tape on a standard 7-in. reel. The crystal is also available in leaded versions. $3.20 to $5.45 (1000).

Micro Crystal Div, 35 E 21st St, New York, NY 10010. Phone (212) 505-5340.

Circle No 371

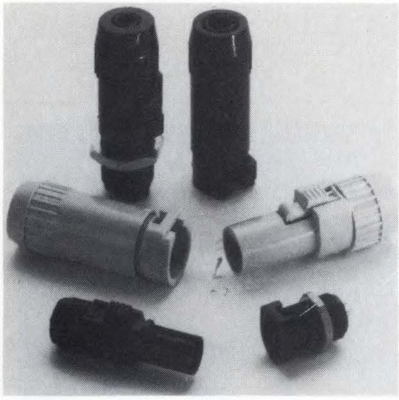
KEYPAD LEGENDS

- *System includes numbers, letters, and symbols*
- *Feature a wear-resistant design*

This legend label system is available for the company's Series 89 keypads. The labels are available in sheet form with numbers, letters, symbols, and standard key inscriptions. You can easily peel the self-adhesive, die-cut, legend label from the sheet and place it on the selected button area on the keypad. Using these labels, you can easily develop a customized keypad for immediate use to satisfy prototype or small-quantity requirements. The legends are printed on the label's second surface to prevent wear. $3.50 per sheet.

Grayhill Inc, Box 10373, LaGrange, IL 60525. Phone (312) 354-1040. TLX 6871375. TWX 910-683-1850. FAX 312-354-2820.

Circle No 372



CONNECTORS

- *Available with both solder-cup and crimp contacts*
- *Feature a shock-proof design*

DO2 Series high-density, 12-position circular connectors are designed for cable-to-chassis and cable-to-cable applications. The polycarbonate housing can accommodate either solder-cup or crimp contacts in a compact 3×0.85-in. envelope. The housing features a novel push-button-style plug-to-receptacle latching system, which eliminates field problems and reduces down time. The pin or socket contacts fit in either the plug or receptacle. All contacts are shrouded to prevent electrical shock. $16 (1000). Delivery, 12 to 18 weeks ARO.

Hypertronics Corp, 16 Brent Dr, Hudson, MA 01749. Phone (800) 225-9228; in MA, (508) 568-0451. FAX 508-568-0680.

Circle No 373

RECTIFIERS

- *Feature a 50-nsec reverse recovery time*
- *Handle frequencies in excess of 20 kHz*

The USC110X and USC130X hermetically sealed axial-lead power rectifiers have 2A and 5A ratings, respectively, and 50-nsec reverse recovery times. Both are available in versions that handle 200, 300, and 400V (where X designates 4, 5, or 6 for 200, 300, or 400V, respectively). The units are specifically designed for switching power supply circuits operating at frequencies in excess of 20 kHz. Both lines are available in commercial and high-reliability versions. From $4 (OEM qty).

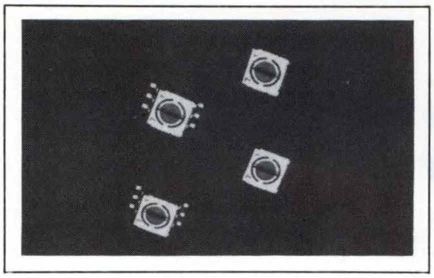
Semtech Corp, Box 367, Newbury Park, CA 91320. Phone (805) 498-2111. TWX 910-336-1264. FAX 805-498-3804.

Circle No 374

ROTARY SWITCHES

- *Available in gull-wing or J-hook versions*
- *Handle standard soldering and washing procedures*

Designed for surface mounting applications, CS-4-22 dpdt rotary selector switches are available in gull-wing or J-hook styles in either bulk



or tape-and-reel packaging. The units are housed in packages measuring 4.5×5×2.5 mm. The units withstand standard soldering and washing procedures, because they incorporate an O-ring seal. The seal prevents leakage even when the units are immersed in low viscosity liquids, such as Fluorinert FC-40. A high-temperature housing allows the switches to survive infrared and vapor-phase soldering cycles as long as 3 minutes at 215°C. The contact rating is 0.5 VA for a dc resistive load; the contact resistance is 100 mΩ max at 1 kHz and 20 mV. Maximum voltage and current ratings measure 100 mA and 16V, respectively; and the operating range is -25 to +70°C. Rotational life equals 200 cycles min. $1.30 (5000).

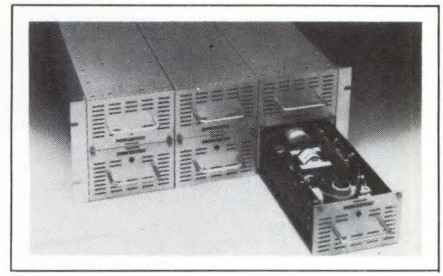
Mepcopal Co, 11468 Sorrento Valley Rd, San Diego, CA 92121. Phone (619) 453-0332. FAX 619-481-1123.

Circle No 375

POWER SUPPLIES

- *Feature five isolated and floating outputs*
- *Spec ±0.2% line and load regulation*

Featuring ratings to 300W, the 11 models in the 29D Series all have five isolated and floating output voltages ranging from 5 to 24V. You can develop an N+1 redundant power system by connecting multiple, current-shared outputs in parallel. Standard features include field-selectable inputs of 90 to 132 or 180 to 264V, line and load regula-



tions of ±0.2% at 100% rated load, current limiting, overvoltage protection, a fault indicator, and overtemperature shutdown. Input/output signals include remote sense, input power fail, output good, undervoltage, and inhibit (total or individual output). Isolation diodes, active preload, an EMI filter, and an overvoltage crowbar are available as options. $508 (25) for units with automatic preload, isolation diode, and EMI filter options.

Powertec, 20550 Nordhoff St, Chatsworth, CA 91311. Phone (818) 882-0004. FAX 818-998-4255.

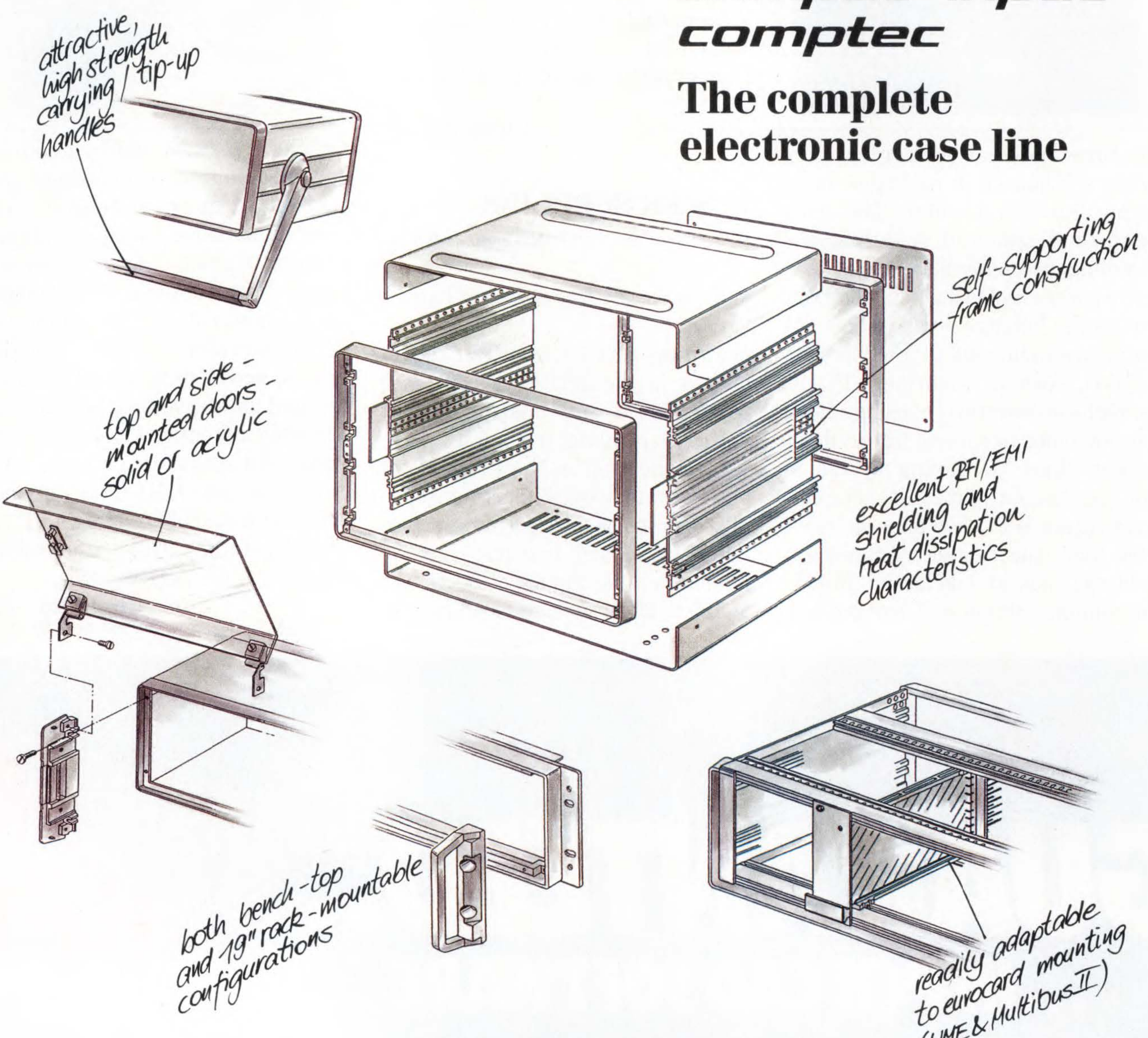
Circle No 376

Text continued on pg 286

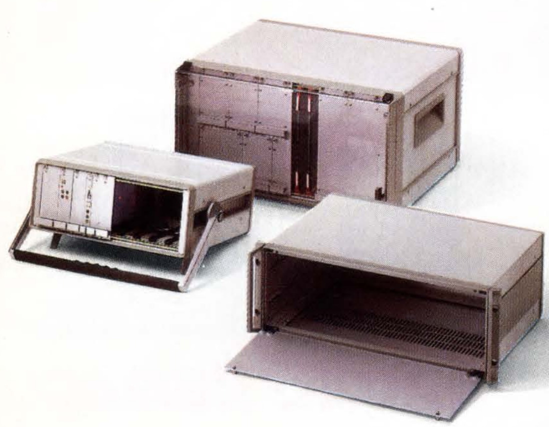
Schroff®

compac inpac comptec

The complete electronic case line



Schroff offers you over 100 different case configurations directly from stock.



Schroff is the industry leader in engineered electronic case systems. Cases with features that allow economical creativity. Cases enhanced by a range of accessories that fill over 70 catalog pages. Schroff offers you over 25 years of enclosure design experience. Experience that enables us to customize Schroff cases to your exact requirements – while meeting your budget and lead time needs.

CIRCLE NO 160

Please call 1-800-451-87 55 for your 270 page full line catalog and price list.

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MANUFACTURING FACILITIES
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R. I. 02886
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Telefax (401) 738-7988

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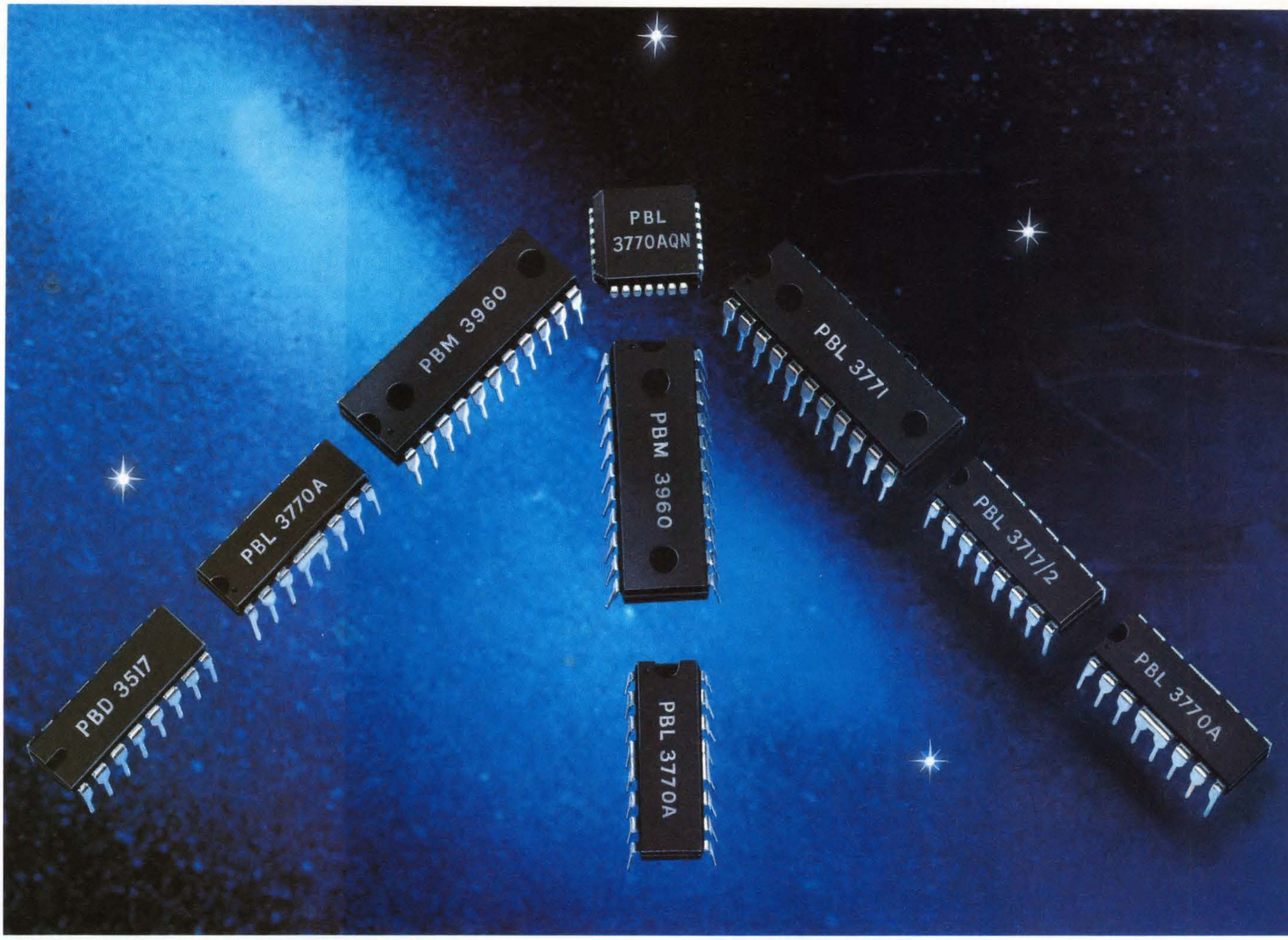
Stepper Motor Drivers.



Choose RIFA and discover how the world's leading family of motor control devices gives you more choice, more applications, more innovation and much more performance for your space and money.

PBL 3717/2.
Latest version of our industry-standard PBL 3717. Constant current switchmode control uprated to 1.0A continuous output current from previous 0.8A. High, medium, low (park) and true zero output; half- and micro-stepping capabilities; all with the utmost efficiency and performance. Widely copied – come to the source for the brightest and best.

PBL 3770A.
Our brilliant new star. 1.5A continuous, 1.8A peak current. Drives all kinds of motors. Low heat dissipation, high packing density. 16-pin DIP version is pin-compatible with 3717; also 28-pin PLCC version.

PBD 3517.
Low-cost driver for unipolar motors. Economical, reliable, complete – you only need one small driver per motor.

PBL 3771 + PBM 3960.
The new, sophisticated micro-stepping system. Dual precision chopper-driver with dual 7-bit-plus-sign D/A converter. Output 600mA per phase, automatic slow/fast current decay, plus very good low-current linearity – this is the universal leader in micro-stepping performance.

Note: All our stepper motor drivers (except PBD 3517) are available in DIP or PLCC packages. PBL 3717/2, 3770A, and 3771 all have a special lead-frame for heat-sinking through ground pins to the pc board copper.

We're in the lead

RIFA Inc.

403 International Pkwy
Richardson, TX 75085-3904
Telephone (214) 480-8300
Telefax (214) 680-1059

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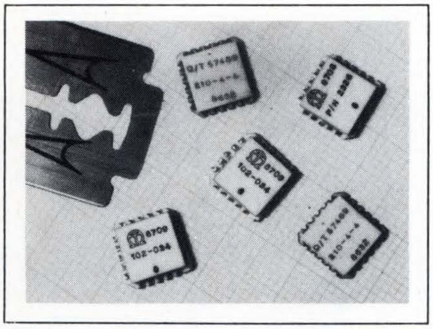
CIRCLE NO 99



RESISTOR NETWORKS

- *Conform to MIL-R-83401*
- *Are packaged in surface-mounting chip carriers*

These chip-carrier-packaged resistor networks are available in standard and custom circuit configurations with resistor values ranging from 10Ω to 1 MΩ. Absolute resistor tolerance can be as low as ±0.1% and relative tolerance as low as 0.01%. The networks' temperature coefficient of resistance (TCR) is ≤±50 ppm/°C, and TCR tracking between resistors in the same package is 2 ppm/°C. Long term stability over a period of 1000 hours at 70°C and at a power dissipation of 0.5W is less than 0.05%. Conforming to MIL-R-83401, the resistor networks are packaged in 16-, 20-, 24-, or 28-pin hermetic or non-hermetic chip carriers. They have an operating temperature range of −55 to +150°C. A typical network costs around $7 (1000).

Sfernice, 199 Blvd de la Madeleine, 06021 Nice Cedex, France. Phone 93446262. TLX 470261. FAX 93862726.

Circle No 377

Ohmtek, 2160 Liberty Dr, Niagara Falls, NY 14304. Phone (716) 283-4025. TLX 710-524-1653. FAX 716-283-5932.

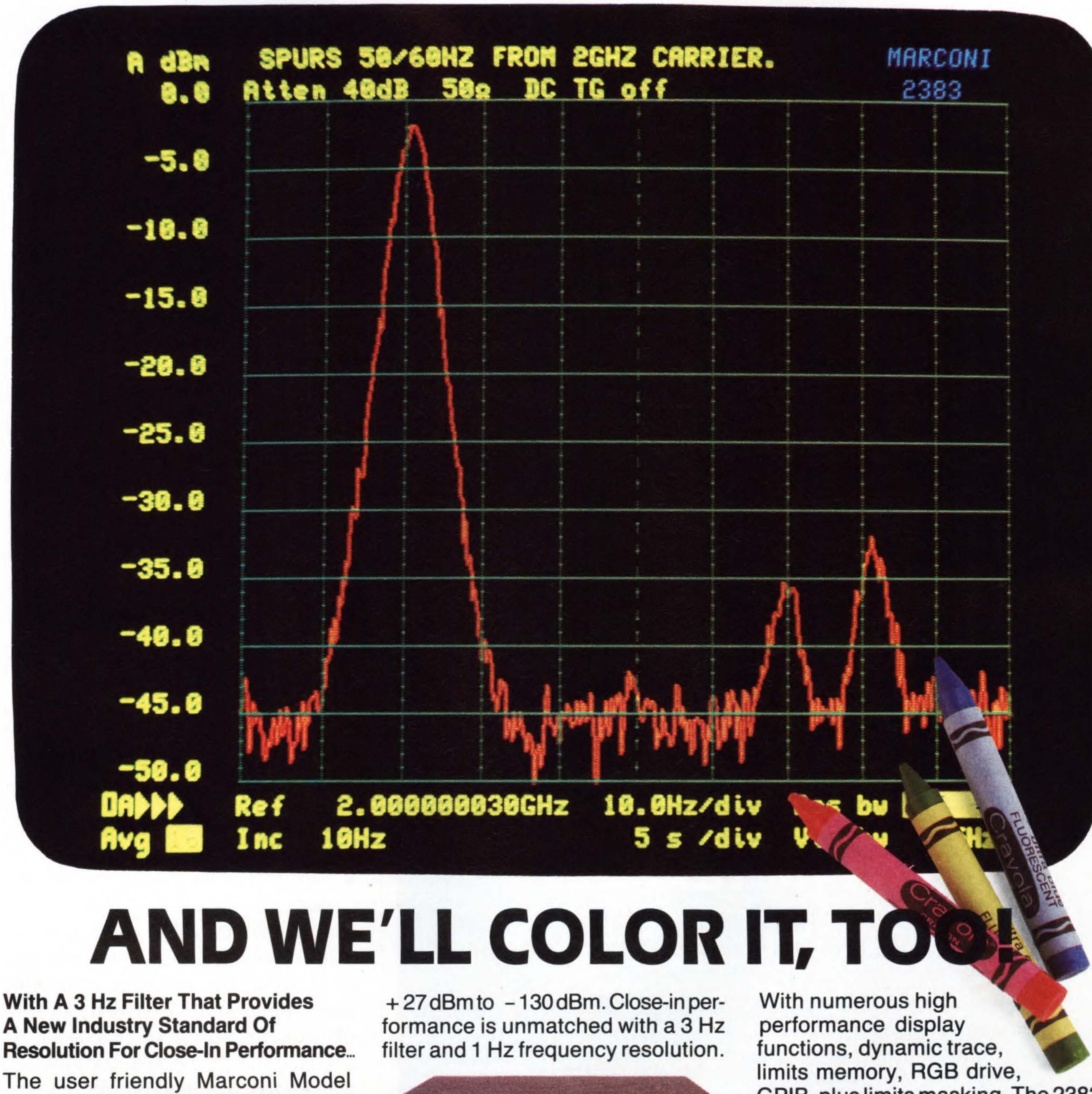
Circle No 378

HEAT SINKS

- *Maximize heat-sink surface area*
- *Designed to cool PGAs*

With a fin-ratio (fin height:fin spacing) of 12:1, the 2380 heat sink provides over 100% more surface area than conventional extrusions of the same size. Designed to cool 15×15-pin grid arrays (PGAs) in forced convection applications, the unit measures 1.5×1.5×1 in. At 400 ft/min airflow, the case-to-ambient

WE'LL SHOW YOU WHAT NO ONE HAS EVER SEEN BEFORE



AND WE'LL COLOR IT, TOO!

With A 3 Hz Filter That Provides A New Industry Standard Of Resolution For Close-In Performance...

The user friendly Marconi Model 2383, 100 Hz to 4.2 GHz Spectrum Analyzer with built-in tracking generator establishes a new standard of high accuracy, resolution and stability of measurements. The automatic self calibration routine provides exceptional RF level accuracy of ±1.5 dB at 4.2 GHz from +27 dBm to −130 dBm. Close-in performance is unmatched with a 3 Hz filter and 1 Hz frequency resolution.

4.2 GHz Spectrum Analyzer–Model 2383

With numerous high performance display functions, dynamic trace, limits memory, RGB drive, GPIB, plus limits masking. The 2383 is at your command for demanding spectral analysis requirements.

For a demonstration or details contact: Marconi Instruments, 3 Pearl Ct., Allendale, NJ 07401.
• (800) 233-2955 • (201) 934-9050
• In Canada (514) 341-7630

Marconi
Instruments

thermal resistance is 1.5°C/W. You can use epoxy to bond the heat sink to the PGA or use the company's E-Z mount mechanical attachment device. $1.56 (1000).

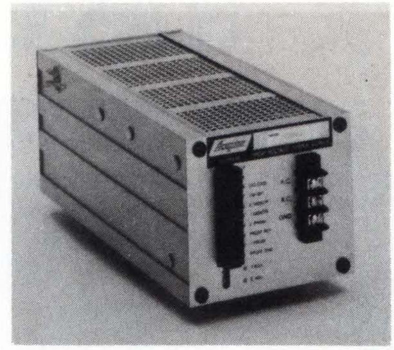
Thermalloy Inc, Box 810839, Dallas, TX 75381. Phone (214) 243-4321. TLX 203965. FAX 214-241-4656.

Circle No 379

POWER SUPPLIES

- *Operate on ac inputs*
- *Feature ±0.05% line and load regulation*

Unlike many high-voltage power supplies, these units have a 105- to 125V ac standard input range; 210 to 250V ac is optional. Outputs range from 0 to 1 kV at 30 mA to 0 to 30 kV at 1 mA. Standard features include constant-voltage/constant-current crossover, remote programming of both voltage and current, and arc/short-circuit protection. Line and load regulation are each ±0.05%, and ripple measures ±0.05% p-p. A flying lead at the rear serves as the output connection. All control connections are through a pluggable terminal block that serves as a connector. The ac input connections are on a separate terminal strip. Current and voltage adjustments are located on the front panel. $590 to $890.



Acopian, Box 638, Easton, PA 18044. Phone (800) 523-9478.

Circle No 380

RF RELAYS

- *Meets MIL-R-39016 requirements*
- *Features a magnetically latched design*

The RF120 TO-5 RF relay features a hermetically sealed construction. At 1 GHz, the unit has a 0.19-dB insertion loss, a 1.2 VSWR, and 42-dB isolation across the contacts. At 3 GHz, the respective parameters are 0.3 dB, 1.5, and 33 dB. The relay is designed and built to meet the requirements of MIL-R-39016. The magnetic-latching feature of the relay provides a nonvolatile memory capability—after the contacts transfer, there are no holding-power requirements. $96.95 (100).

Teledyne Relays, 12525 Daphne Ave, Hawthorne, CA 90250. Phone (213) 777-0077. TWX 910-321-4610. FAX 213-779-9161.

Circle No 381

DESIGNING POWER SUPPLIES
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HAS GIVEN
COMPUTER PRODUCTS
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At Computer Products, we are committed to understanding the needs of our customers. No other power supply company is so sensitive to the issues that are central to you. And no other power supply company is so responsive to those issues. Computer Products. Your partner in power.

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Over 1900 people throughout North America, Europe and Asia. $100 million in power supply sales. And 187 distributor locations worldwide – the strongest distributor network of power supply products in the world.

It means one-stop shopping. It means reliable, scheduled delivery anywhere, anytime. And it means a resource you can depend on from Minneapolis to Munich.

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A major benefit of Computer Products is that we are the source for the industry's widest selection of power supply products.

Open frame linears, open frame switchers, encapsulated power modules, cased switchers, high-power switchers, and DC/DC converters. Including a wide selection of Mil-Spec switching power supplies and DC/DC converters. 2400 standard models to choose from – plus modified standard or custom versions which are derived from our proven designs.

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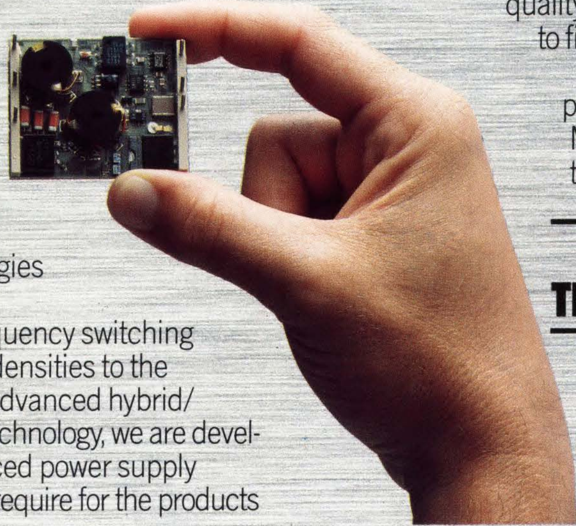
Computer Products concentrates on the big picture in power supply technology. You benefit from products that are precision-engineered using the most advanced and reliable technologies available.



From high frequency switching and high-power densities to the industry's most advanced hybrid/surface-mount technology, we are developing the advanced power supply designs that you require for the products of tomorrow.

QUALITY AND RELIABILITY YOU CAN TRUST.

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It's part of our total company commitment to being a world class manufacturer. We believe in never-ending improvement in the quality of our products and processes. From Statistical Process Control (SPC) through Just-In-Time (JIT) production we are improving every phase of the manufacturing process.

Unlike many power supply companies, our offshore manufacturing facilities are our own. Not those of hard-to-control subcontractors. Our uniform worldwide quality standards can be strictly controlled from start to finish by our own program of quality at the source.

We deliver an unrivaled level of reliability in power supply performance. Including units with MTBF's over 400,000 hours and conformance to the stringent Mil-Q-9858A requirements.

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Designed-in reliability, attention to scheduling requirements and exceptional after-sale servicing. All natural outgrowths of our awareness of the critical issue of cost of ownership.

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Your Partner in Power SM

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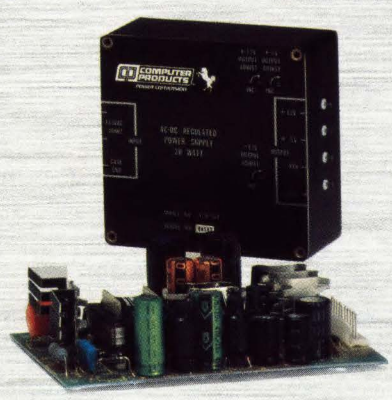

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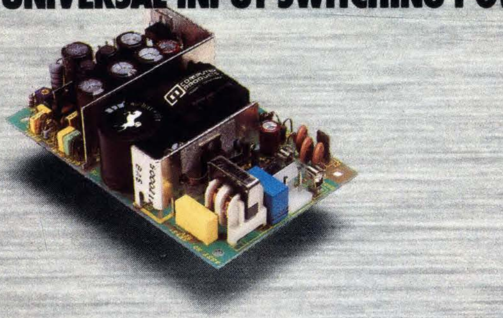
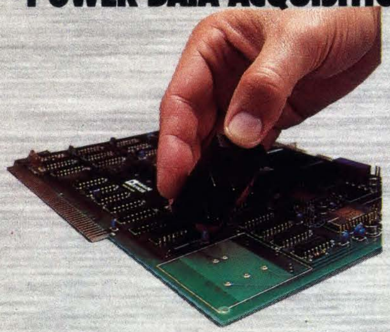
UNIVERSAL INPUT SWITCHING POWER SUPPLIES



Power your system from any worldwide line voltage without changing jumper wires or switches. The NFS Series universal input switchers provide single or multiple outputs for 40 watt, 50 watt, or 110 watt applications. Check out the NFS40 series, which measure a mere 5" x 3" x 1.2". The NFS50-7608 directly replaces the industry standard 6.3" x 3.9" 40 watt supply and offers a bonus of 10 additional watts for system extras. And the NFS110 series will deliver 110 watts from a small 7" x 4.25" x 1.8" package. Its +12V output will deliver up to 9A peak current to start disk drives.

ISOLATED AND REGULATED DC/DC CONVERTERS POWER DATA ACQUISITION CIRCUITS



The H, EA and AF Series are isolated and regulated DC/DC converters having the same industry standard footprint to provide flexibility for your design. Ideally suited for powering analog and digital circuitry such as OP Amps, A/D and D/A converters, logic and microprocessors. Packaged in 1.0" x 2.0" x 0.38" non-conductive cases, these 1 to 4.5 watt converters are available for a variety of input and output voltages. All units feature isolation of 500V, setting accuracies to ±2% max. and fully regulated output to ±1% max.

HIGH EFFICIENCY 100 WATT DC/DC CONVERTER

The WS Series is your logical choice when it comes to selecting high power density DC/DC converters. Packaged in a low profile 3.5" W x 5.5" L x 0.91" H case, these 100 watt units feature 18-36 and 36-72 VDC input ranges, single, dual and triple outputs, 500 VDC isolation and efficiencies up to 84%. Ideal for telecom and computer applications, and now a new dual +5 and +12 VDC output version with peak current capability for power disk drives. Chassis mounting with screw terminations or PCB mount with heat sink versions available.

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1. NFS 40/50/110 Series
2. H, EA, AF Series
3. WS Series
4. Mil-Spec Catalog
5. Engineering Handbook
6. Have a Sales Person Call

Name ______________________ Title ____________

Company ____________________ Dept/MS __________

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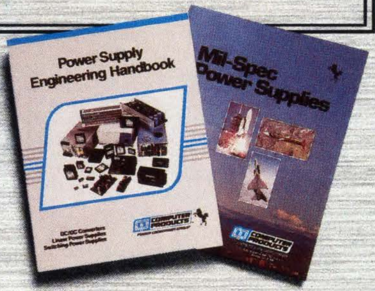

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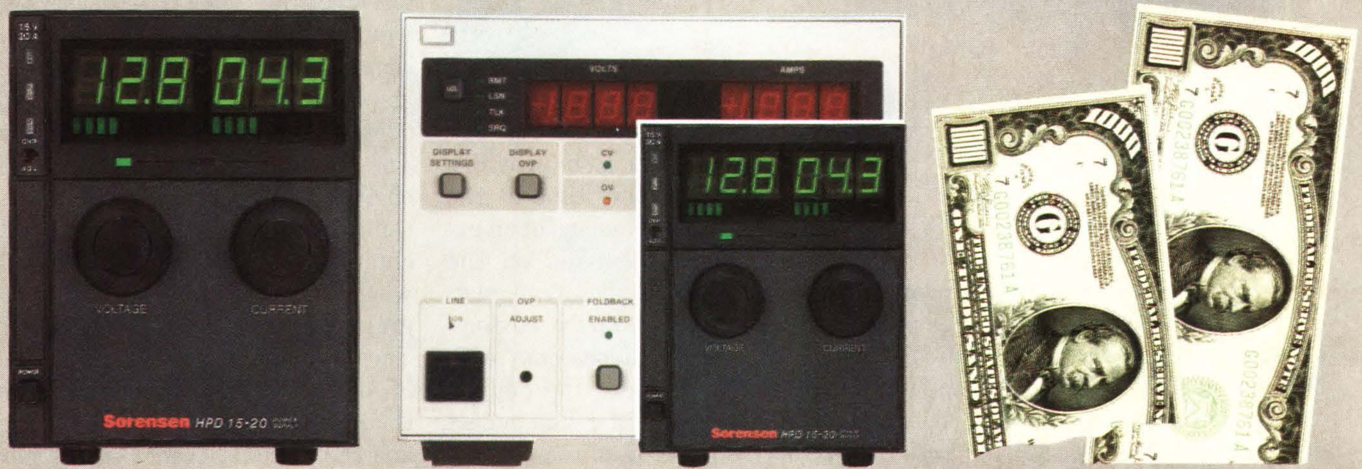


The 300 Watt **HPD** Series Programmable DC Power Supply From Sorensen

Hard to believe? It's true—the Sorensen 300 watt Model HPD (High Power Density) delivers *three times more power* than most other 1/4 rack power supplies. And at $1195, the HPD is the lowest priced power supply in its class.

The HPD incorporates a linear post regulator to achieve 5 mv ripple RMS, a typical 500 μsec transient response for a ±50% load change, and a .02% +4 mV line and load regulation. Full rated current available at all voltages eliminates the guesswork associated with power curves. The HPD has been certified to meet FCC Part 15 subpart J Class A for reduced conducted and radiated emissions.

An internal IEEE 488 interface card (Option M9) provides overvoltage protection (OVP), 12-bit programming resolution, and 8-bit digital readback resolution of voltage and current, and is priced at $450. An alternative option (M5) features OVP, remote programming, TTL inhibit, rear panel terminals, and is available for $150. A standard 19" rack adapter is available for one to four units, providing up to 1200 watts of DC power.

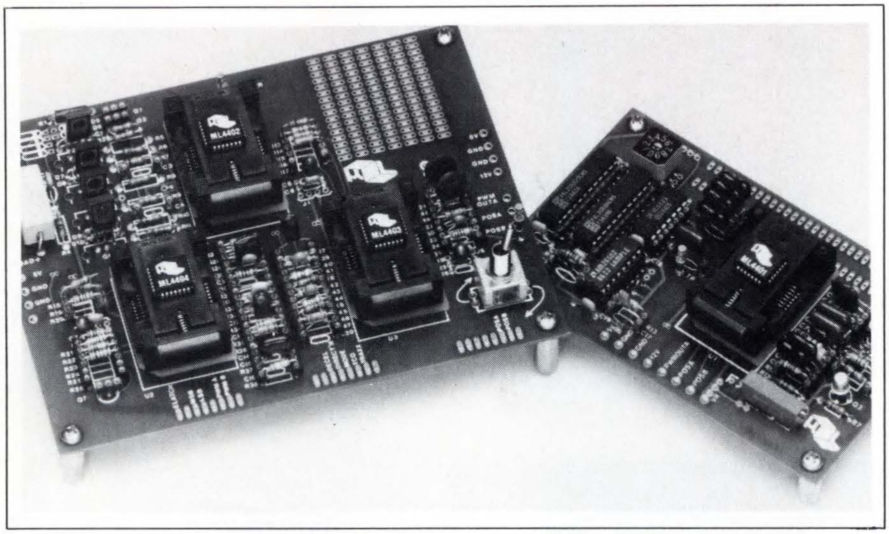
The facts are clear. The choice in power supplies is Sorensen. Call or write our applications engineering staff for additional data on the revolutionary HPD series.

Sorensen
A **Raytheon** Company
5555 N. Elston Ave.
Chicago, IL 60630
(312) 775-0843 Ext. 269

Volts		0-15V	0-30V	0-60V
Amps		0-20A	0-10A	0-5A
Sorensen Model		HPD15-20	HPD30-10	HPD60-5
Ripple & Noise	V	5 mV RMS, 50 m V P-P		
	I	20 mA P-P		
Line Regulation	V	.01% + 2 mV		
	I	.01% + 1 mA		
Load Regulation	V	.01% + 2 mV		
	I	.01% + 1 mA		
Transient Response		+/- 50% Load changes in range of 25 - 100% of rated load in less than 500 μsec.		
IEEE Interface		12 Bit Resolution Programming V + I 8 Bit Resolution Readback of V + I		
Size	*US*	5.2 H × 4.3 W × 11.7 D	5.8 lbs.	
	Metric	132 mm H × 109 mm W × 297 mm	2.6 Kg	

EDN 10-13-88

CIRCLE NO 166



SERVO CONTROL CHIP

- *Generates a velocity profile*
- *Optimizes track-access speed of disk drive*

The ML4404 trajectory-generator chip optimizes the track-access speed of head-positioning servos for high-end disk drives. The chip generates a velocity profile that produces the optimal velocity for positioning the Read/Write heads on 3½- and 5¼-in. disk drives. The ML4404 features an anticipate function, which modifies the trajectory curve to eliminate the overshoot problem. The chip also provides control of the settling time at the destination track by means of an external resistor. Designed on the company's FB3620 tile-array platform, the ML4404 can be customized to specific requirements with minor modifications to the double-layer metal masks. The chip is part of a four-chip set that is available on evaluation boards. $7.40 (1000).

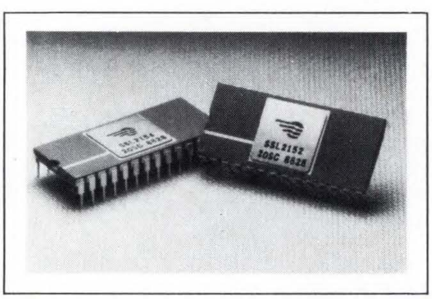
Micro Linear Corp, 2092 Concourse Dr, San Jose, CA 95131. Phone (408) 433-5200.

Circle No 385

CACHE TAG MEMORIES

- *Feature 17- to 30-nsec operating speeds*
- *Include parity-checking 9th bit*

The SSL2152 and SSL2154 are 2k×9-bit cache address comparators that feature address compare-to-match output times as fast as 17 nsec. According to the manufacturer, the devices are the fastest cache-tag memories available in this density and organization and are 100% functionally compatible with the TACT2152/54 from Texas Instruments Inc. The SSL2152/54 also feature a 9th bit to handle parity checking, which is gaining popularity in high-performance, 32-bit



CISC and RISC systems. The ICs have TTL-compatible inputs and outputs and are cascadable in memory depth and word width. The SSL2152 has a totem-pole output; the SSL2154 has an open-drain output. Available packages include DIPs and PLCCs. Prices, which depend on the speed selection and package, range from $35 to $56 (100).

Saratoga Semiconductor, 10500 Ridgeview Court, Cupertino, CA 95014. Phone (408) 864-0500. FAX 408-446-4416.

Circle No 386

FIBER-OPTIC CHIPS

- *Available in three-chip sets*
- *For 50M- and 200M-bit systems*

Designed for fiber-based LANs as well as standard telecommunications, the company offers two three-chip sets for use at data rates to 50M- and 200M-bits, respectively. The 50M-bit set operates as a Manchester biphase mark-encoded system. The transmitter section includes an LED driver (SP9960), which features drive-current programmability from 15 to 150 mA. The receiver section contains the SL9901, a transimpedance amplifier that interfaces with a PIN diode, and the SP9921 decoder, which performs the functions of clock and data recovery. The 200M-bit set operates over the 100M-to 200M-bit spectrum, which includes the FDDI (Fiber Optic Distributed Data Interface) standard. The SP9954 transmitter can drive an LED or a laser diode and features external-resistor programming of the operating current. The receiver consists of the SL9904 transimpedance amplifier and the SP9944 data-slice circuit, which converts the output from the SL9904 to a true ECL-level signal. A programmable threshold-detect function directly supports the requirements of the FDDI standard. The 50M-bit chip set, $39.03; the 200M bit chip set, $60.01 (1000).

Plessey Semiconductors, 1500 Green Hills Rd, Scotts Valley, CA 95066. Phone (408) 438-2900. TLX 4940840. FAX 408-438-5576.

Circle No 387

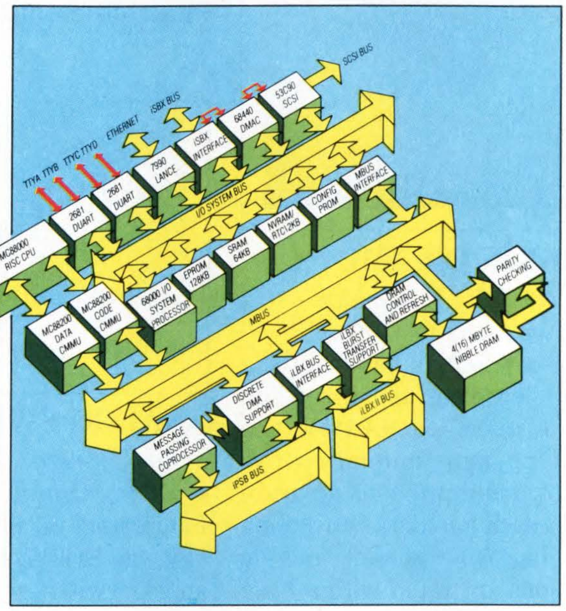
The MC88000 RISC Multibus II Single Board Computer

The TP880M from Tadpole

•The Philosophy•

The TP880M design brings together the outstanding performance of the Motorola MC88000 RISC processor set, the power of the full MultibusII/iLBX II interfaces, an MC68000/68440 I/O subsystem with SCSI and Ethernet, and the specially designed Tadpole 88000 RISC optimising C Compiler. The result is an outstanding product that offers users the very best of current SBC technology.

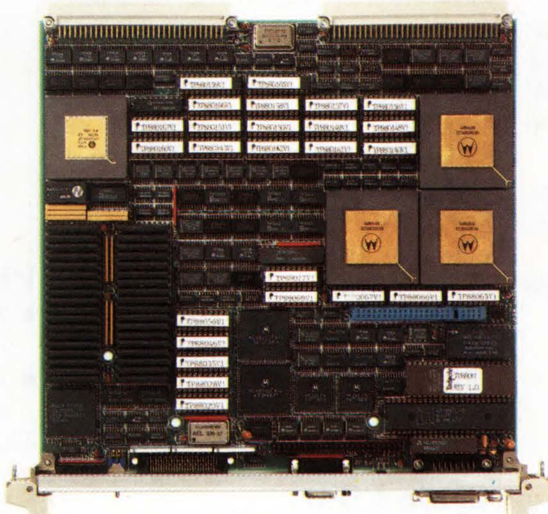
•The Design•



•The Specification•

- MC88100 RISC processor (20-33MHz)
- 16Kb MC88200 cache/MMU instruction cache
- 16Kb MC88200 cache/MMU data cache
- 4-16Mb Nibble mode parity-protected DRAM
- iPSB interface implemented using the Intel Message Passing Coprocessor (MPC)
- iLBX interface and iSBX connector
- I/O Subsystem MC68000/68440 CPU/DMA provides SCSI 4 RS232 ports • Up to 128Kb EPROM
- 64Kb SRAM and optional ETHERNET networking
- TP-IX V.3.1*
- TP-CDS/88K advanced C development environment
- T-Mon 88K Monitor with extensive SCSI support

•The Evidence•



Tadpole Technology

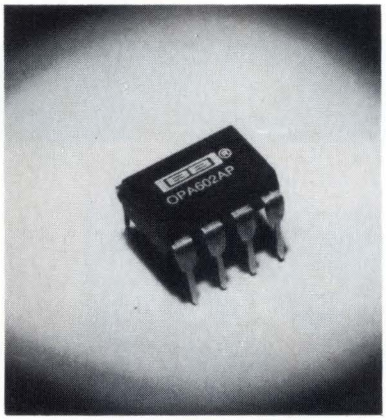
the driving force in 32-bit design

Tadpole Technology plc
Titan House, Castle Park,
Cambridge, CB3 OAY, UK
Tel: 0223 461000
Fax: 0223 460727

Tadpole Technology Inc
Reservoir Place,
1601 Trapelo Road, Waltham,
Massachusetts, 02154, USA
Tel: 0101-617-890-8898
Fax: 0101-617-890-7573

Tadpole Technology Inc
2157 O'Toole Avenue
Suite F, San Jose,
California, 95131, USA
Tel: 0101-408-435-8223
Fax: 0101-408-435-8482

T A D P O L E



PRECISION OP AMP

- *Has a 6.5-MHz bandwidth*
- *Can drive loads to 1500 pF*

Featuring a 6.5-MHz bandwidth, a 35V/μsec slew rate and a settling time of 1 μsec (to 0.01%), the OPA602P op amp minimizes dynamic errors and provides accurate signal processing in data conversion applications. All dynamic and dc specifications are rated with a 1-kΩ resistor in parallel with a 500-pF load. The OPA602P can drive capacitive loads to 1500 pF in unity gain. Other features include an offset voltage of ±1 mV (max), a bias current of ± 2 pA (max), and low noise (12 nV/$\sqrt{Hz}$). The OPA602P comes in an 8-pin plastic DIP. $2.80 (100).

Burr-Brown, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491. TWX 910-952-1111.

Circle No 388

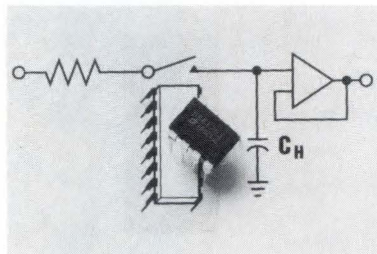
MATH COPROCESSOR

- *32-bit chip runs at 33 MHz*
- *Breaks two-million Whetstone barrier*

The 68882 second-generation, 32-bit floating-point math coprocessor has a speed of 33 MHz. This high-performance coprocessor is used with the company's 68000 family of μP's. The 68882 conforms to the IEEE Standard for Binary Floating-Point Arithmetic and offers software- and pin-compatibility with its predecessor, the 68881. According to the company, the chip is the first to break the two-million Whetstone barrier—a standard benchmark that tests a processor's ability to perform mathematical operations). $708. Delivery, 60 days ARO.

Motorola Inc, Technical Info Ctr, Box 52073, Phoenix, AZ 85072. Phone (512) 440-2839.

Circle No 389



ANALOG SWITCHES

- *Low on-resistance*
- *Fast switching speed*

Fabricated in silicon-gate technology, the DG417, DG418, and DG419 analog switches provide a low on-resistance of 35Ω and a fast switching speed (t_{on}) of 175 nsec. In addition, the devices feature low power-dissipation of 35 μW and low leakage-current of 250 pA. The devices operate from a single supply, which eases the design of unipolar systems. The devices are available in 8-pin plastic DIPs and small-outline packages for industrial applications and in 8-pin ceramic DIPs for military use. Prices range from $1.45 to $9.84 (100).

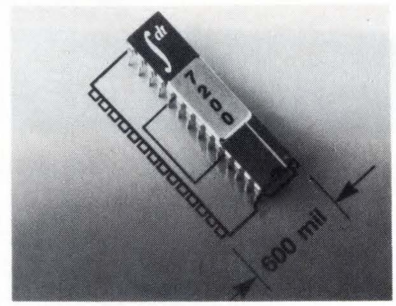
Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 390

CMOS FIFO

- *Features 25-nsec access time*
- *Features three flag outputs*

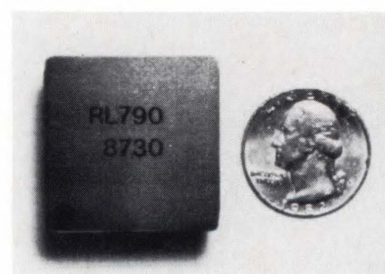
Fabricated in CMOS, the IDT7200 is a 256×9-bit FIFO register that features a 25-nsec access time. The register offers three flag outputs: full, half-full, and empty. The chip's 9-bit wide data array is useful for systems that require byte-wide parity. The device has a re-transmit capability, which can re-read data



from the first read location. You can cascade the FIFO in depth and width by means of two connections. Maximum supply current is 80 mA for commercial versions and 100 mA for military versions. The IC comes in a 32-pin PLCC, a 32-pin CLCC, or a 28-pin 300-mil DIP. Prices start at $50.90 (100).

Integrated Device Technology Inc, Box 58015, Santa Clara, CA 95052. Phone (408) 727-6116. TWX 910-338-2070.

Circle No 391



PREAMPLIFIER

- *Employs hybrid cascode microcircuit*
- *Delivers high-gain and low-noise at −200°C*

The RL-790 charge-sensitive preamplifier can amplify signals at −200°C. It employs a hybrid microcircuit utilizing JFETs in a cascode configuration to deliver high-gain and low-noise performance. The RL-790 has a sensitivity of 0.2 V/pC and an equivalent noise charge of 240 electrons. The hybrid has an input capacitance of 25 pF and a 10-nsec rise time with an 95Ω impedance. The 1.25×1.25×0.25-in package withstands liquid argon radiation detectors. You can interface

43K+ Dhrystones. 17+ MIPS. 7+ MFlops. 4Mb DRAM. 1 SCSI. One VME Board.

The TP880V from Tadpole

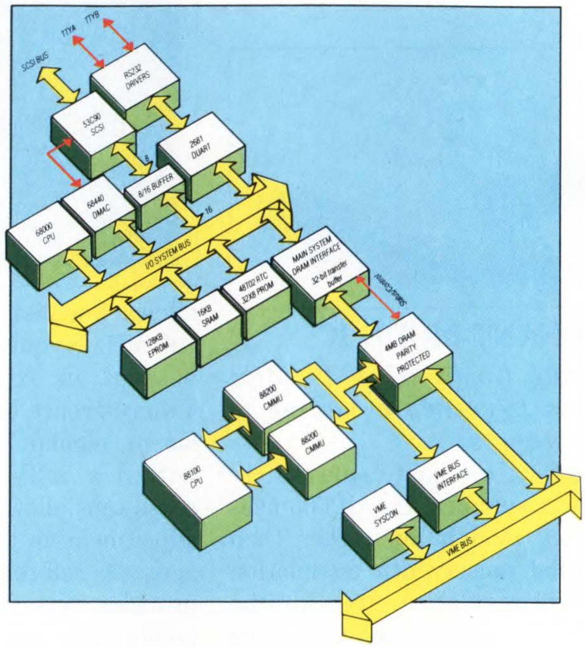
• The Philosophy •

The TP880V is a high performance Single Board Computer for VME based systems. Designed round the Motorola 88000 RISC architecture, the TP880V offers 17MIP, 6MFlop performance at 20MHz and provides a very high level of integration of processing and I/O features on a single card. Tadpole's 88K C Compiler was specially developed to take full advantage of the 88000 RISC architecture.

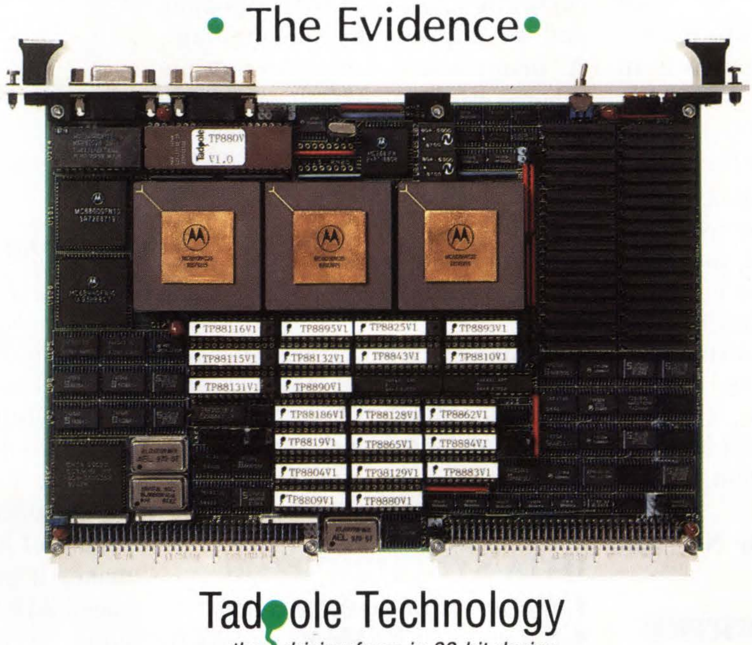
• The Specification •

- MC88100 RISC processor (20-33MHz)
- 16Kb MC88200 cache/MMU instruction cache
- 16Kb MC88200 cache/MMU data cache
- 4-16Mb Nibble mode parity-protected DRAM
- I/O Subsystem MC68000/ 68440 CPU/DMA
- 53C90 high performance sync/asynchronous SCSI
- 2 RS232 Ports • 128Kb-1Mb EPROM
- Extensive diagnostics capabilities
- Full VME Interface Rev C.1 IEEE 1014
- DTB Master-DTB Slave Syscon interrupter/handler
- 64Kb SRAM battery-backed RTC
- TP-CDS/88K advanced C development environment
- T-Mon 88K Monitor with extensive SCSI support
- TP-IX*

• The Design •



• The Evidence •



Tadpole Technology

the driving force in 32-bit design

Tadpole Technology plc
Titan House, Castle Park,
Cambridge, CB3 OAY, UK
Tel: 0223 461000
Fax: 0223 460727

Tadpole Technology Inc
Reservoir Place,
1601 Trapelo Road, Waltham,
Massachusetts, 02154, USA
Tel: 0101-617-890-8898
Fax: 0101-617-890-7573

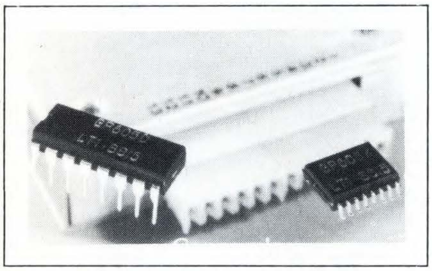
Tadpole Technology Inc
2157 O'Toole Avenue
Suite F, San Jose,
California, 95131, USA
Tel: 0101-408-435-8223
Fax: 0101-408-435-8482

T A D P O L E

*UNIX is a trademark of A T & T *TP-IX V.3.1 is derived from UNIX V.3.1* the unit with vacuum photodiodes and all standard semiconductor detectors. $125.

REL-Labs Inc, 30 Midland Ave, Hicksville, NY 11801. Phone (516) 935-7272.

Circle No 392



RESONANT-MODE IC

- *Operates from 1 kHz to 1.2 MHz*
- *Varies frequency according to load changes*

Designed for resonant-mode switching power supplies, the GP605 uses frequency modulation rather than traditional pulse-width modulation to control regulation. It holds the pulse width constant and varies the frequency according to load changes. The device reduces power-supply size, component stress from zero-current switching, switching losses, and EMI. It features a frequency range from 1 kHz to 1.2 MHz and a duty-cycle capability of 60% at 1 MHz. The IC is available in commercial, industrial, and military versions, and comes in 16-pin DIPs and 16-pin small-outline IC packages. From $3.19 (1000).

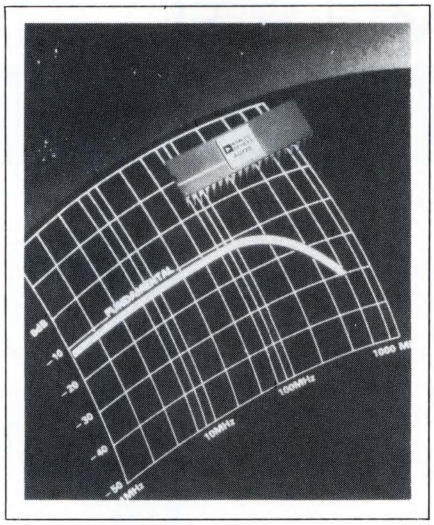
Gennum Corp, Box 489, Station A, Burlington, Ontario, Canada L7R 3Y3. Phone (800) 263-9353; in Ontario, (416) 632-2996. TLX 0618525.

Circle No 393

FLASH A/D CONVERTER

- *Provides 8-bit output*
- *Features a 400-MHz bandwidth*

Featuring a flash architecture, the monolithic AD770 A/D converter provides an 8-bit output at 200M samples/sec. It has a 250-MHz full-power bandwidth and a 400-MHz small-signal bandwidth. The AD770



allows low-distortion sampling of 100-MHz Nyquist-frequency signals without an external S/H circuit. Two reference inputs set the unipolar or bipolar analog-input range within a ±2V span. Force and sense taps allow accurate end-point adjustment for these reference voltages. A reference resistor ladder provides taps at mid- and quarter-points. You can use these taps to curve the ADC transfer function and to improve RF decoupling. A proprietary error-correction scheme reduces erroneous output sparkle codes that are typical of flash converters. All digital outputs are ECL compatible. The AD770 is available in a 40-pin ceramic DIP for either the commercial or military temperature range. From $175 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 329-4700. TLX 924491. TWX 710-394-6577.

Circle No 394

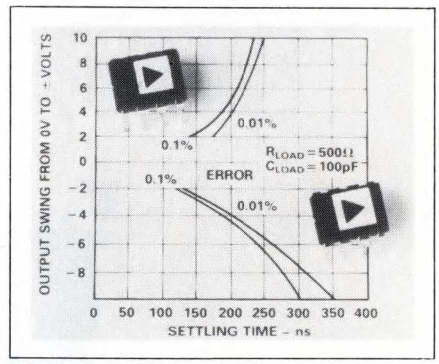
DATA SYNCHRONIZER

- *Features PLL window control*
- *Supports GCR, MFM, and RLL codes*

The DP8459 data synchronizer includes a phase-locked loop that lets designers reduce bit-error rate through improved window accuracy. The device features synchronized window generation and a digital window-strobe control with 5-bit resolution. The IC is capable of addressing the needs of hard disks, floppy disks, optical disks, and tape-drive memory systems. The DP8459 accomodates the preambles used with Group Code Recording; Modified Frequency Modulation; and 1,7 and 2,7 run-length-limited codes. The data-rate range extends from 250k bps to 24M bps with 2,7 code and beyond that range with the 1,7 code. All digital input and output signals are TTL-compatible. The device operates from a single 5V supply and is available in a 28-pin plastic leaded chip carrier. $20 (1000).

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-6725. TLX 346353. TWX 910-339-9240.

Circle No 395



FET-INPUT OP AMP

- *Has a 350-nsec settling time*
- *Offers harmonic distortion of less than 0.0001%*

The AD845 FET-input op amp features a typical settling time of 350 nsec to 0.01% (for a 10V step) into a 500Ω, 100-pF load. The op amp has a total harmonic distortion (THD) of less than 0.0001%, which makes it suitable for driving high-speed ADCs and DSP-system front ends. Dynamic performance includes a 100V/μsec slew rate, a 16-MHz small-signal bandwidth, and 1.75-MHz full-power (±10V into 500Ω) bandwidth. The input offset voltage is 250 μV max with drift of less than 5 μV/°C. Open-loop gain is typically 250V/mV into a 500Ω load, the minimum CMRR is 94 dB,

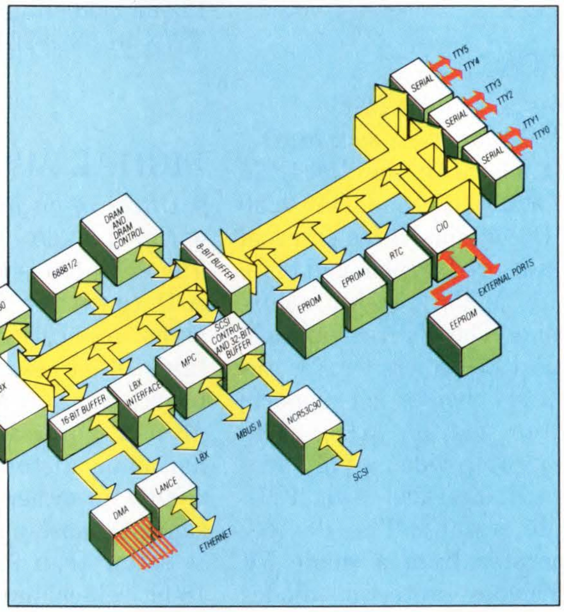
68030 UNIX® or VRTX® Multibus II Single Board Computer

The TP33M from Tadpole

• The Philosophy •

The TP33M is designed to bring together on a fully configured single board computer the outstanding performance of two leading edge technologies: INTEL Multibus II and the 16-33 MHz MC 68030 CISC processor.

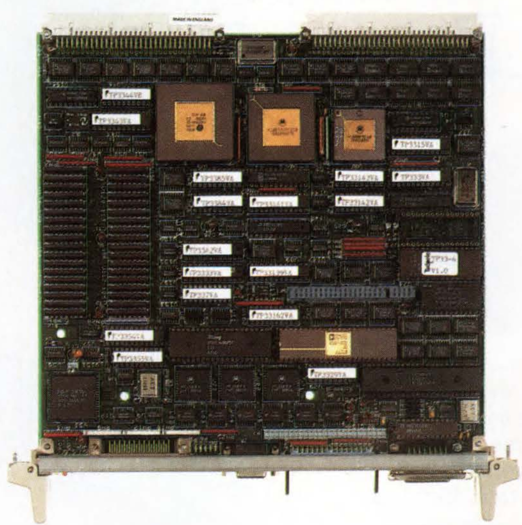
• The Design •



• The Specification •

- MC68030 processor 16-33MHz
- 4-16Mb Nibble mode DRAM
- Custom 32-bit DMA controller
- NCR 53C90 DMA-driven synchronous or asynchronous SCSI interface
- AMD Lance IEEE 802.3 Ethernet with DMA
- 6 x RS232 ports
- Multibus II/iSBX/iLBX II interfaces
- Battery backed-up real time clock
- 2Kb SRAM • 256Kb EPROM
- TP-IX V.3.1* • VRTX
- VRTX - TP-IX* communications software
- Intel transport layer protocol drivers

• The Evidence •



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Tadpole Technology plc
Titan House, Castle Park,
Cambridge, CB3 OAY, UK
Tel: 0223 461000
Fax: 0223 460727

Tadpole Technology Inc
Reservoir Place,
1601 Trapelo Road, Waltham,
Massachusetts, 02154, USA
Tel: 0101-617-890-8898
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2157 O'Toole Avenue
Suite F, San Jose,
California, 95131, USA
Tel: 0101-408-435-8223
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T A D P O L E

CIRCLE NO 185

and the maximum peak-to-peak noise is 4 μV from 0.1 to 10 Hz.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565. TWX 710-394-6577.

Circle No 396

VIDEO DAC

- *Contains three 6-bit DACs*
- *Meets VGA graphics standards*

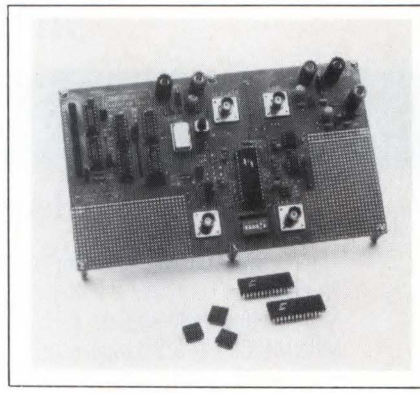
Pin-compatible with the IMSG176 industry standard, the DAC0630 video DAC contains three internal 6-bit DACs for red, green, and blue, along with a 256×18-bit color-lookup table. The VGA-compatible IC can select 256 colors from a palette of 262,144 choices and supports pixel rates to 50 MHz. The DAC0630 also provides a fully synchronous μP interface with TTL-compatible inputs. The device, which operates from a single 5V supply, includes protection diodes on each pin that eliminate latch-up problems and provide ESD protection to 2000V. The IC is available in 28-pin DIP and CERDIP packages. From $9 (1000).

National Semiconductor, Box 58090, Santa Clara, CA 95052. Phone (408) 721-7158. TLX 346353. TWX 910-339-9240.

Circle No 397

DIGITAL AUDIO ADC

- *Offers 16-bit performance*
- *Has a 92-dB dynamic range*



The CSZ5126 is a monolithic stereo A/D converter for use in digital audio applications. The chip features 16-bit resolution, a 92-dB dynamic range in a stereo mode (95 dB in 2× oversampling mode), and harmonic distortion of less than 0.001% in either mode. The chip's signal-to-noise-plus-distortion ratio is better than 92 dB. An internal 18-bit self-calibration circuit, which maintains bit weights and ensures no missing codes, provides a differential nonlinearity (DNL) of 0.25 LSB (typ) over the life of the device. The CMOS device, which features a sleep mode for portable operation, is packaged in a 28-pin DIP and dissipates less than 240 mW. $27.20 (1000).

Crystal Semiconductor Corp, Box 17847, Austin, TX 78744. Phone (512) 445-7222. TLX 910-874-1352. FAX 512-445-7581.

Circle No 398

68030 - VME
The Real *Single* Board Computer

The TP32V from Tadpole

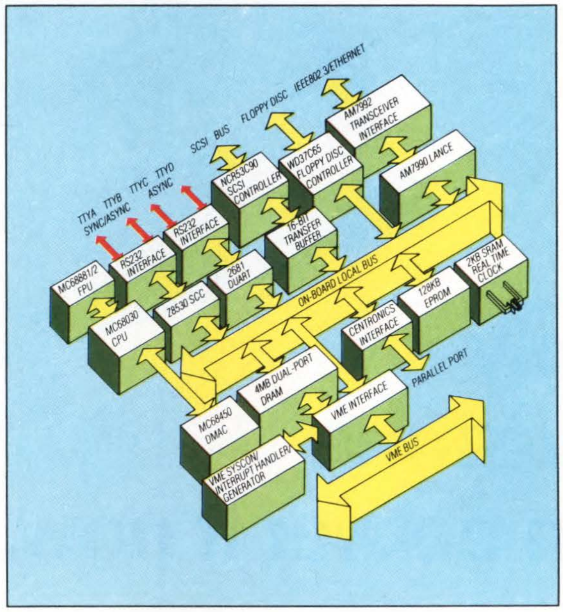
•The Philosophy•

Designed for optimum system performance from a single full IEE 1014 VME board, the TP32V needs no other cards, piggybacks or mezzanines to deliver the full potential of the 16-33 MHz MC68030. To maximise overall throughput, all the on-board I/O facilities were designed to take advantage of hardware transfer buffers, DMA facilities and advanced DRAM arbitration techniques between competing resources.

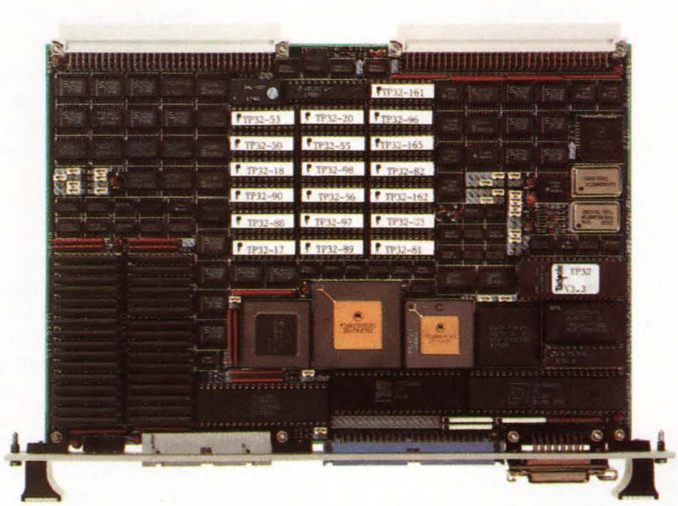
•The Specification•

- MC68030 16-33MHz
- MC68450 4-channel DMA controller
- 4Mb multi-ported nibble-mode DRAM
- AMD Lance IEEE 802.3 Ethernet with DMA
- Z8530 SCC giving two DMA-driven RS232 sync/asynchronous ports and two further RS232 asynchrous ports
- NCR 53C90 DMA-driven synchronous or asynchronous SCSI interface • Floppy disk controller
- Full VME Rev C.1 IEEE 1014 interface
- 64-512Kb EPROM • Battery-backed RTC/SRAM
- Full debug monitor • Optional MC68881/2 FPU
- TP-IX/68K version of UNIX V.3.1* • NFS, RFS, TCP/IP

•The Design•



• The Evidence•



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Titan House, Castle Park,
Cambridge, CB3 0AY, UK
Tel: 0223 461000
Fax: 0223 460727

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Reservoir Place,
1601 Trapelo Road, Waltham,
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Tadpole Technology Inc
2157 O'Toole Avenue
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T A D P O L E

A lot of companies claim complete VME capability.

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Radstone Technology is the *only* company in the world that delivers proven VMEbus board and system level products for every application from commercial to full Military Specification...and everything in between. Plus more than 30 years of solid computer experience—more than *anyone* in the OEM board level computer market.

Commercial VME...highest performance, low cost, ready to plug and play.

Radstone's commercial VMEbus product line includes:
- 16 and 32 bit processor boards, including a complete family of 68030-based boards
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- The world's fastest and most popular SCSI boards; parallel, serial and analog I/O boards; and much more
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- SCSI and 1553B interface boards
- MPCC, Ethernet and serial and intelligent communications boards
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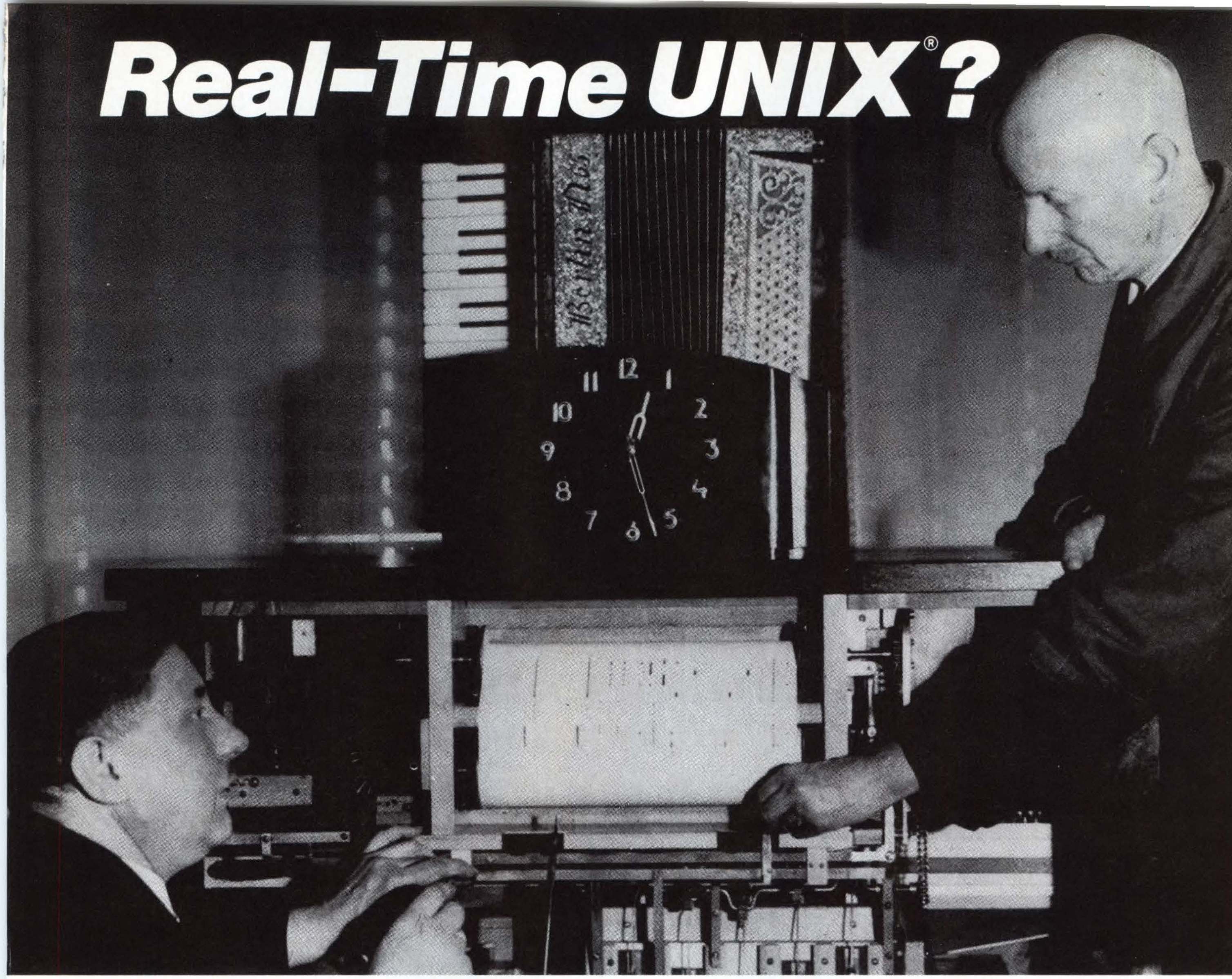
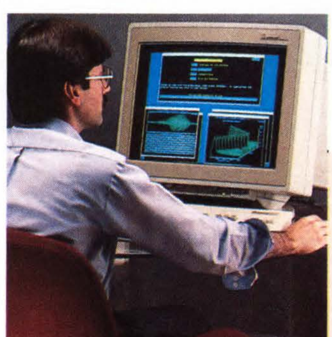
CIRCLE NO 158

Real-Time UNIX®?



Everyone's talking about it now, but we've been shipping it since 1982. And we've continued to set the real-time standard every year since. RTU™, our real-time enhanced UNIX operating system, provides guaranteed response *plus* the flexibility and compatibility of AT&T System V and 4.2 BSD.



Scientists, engineers, systems integrators, and OEMs can choose from a family of MC68030/020-based multiprocessor computers, from 3 to 25 MIPS, with VMEbus™ and Multibus.™ They're designed for high-performance applications in data acquisition, digital signal processing, imaging, C³I, and real-time simulation.

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CIRCLE NO 131

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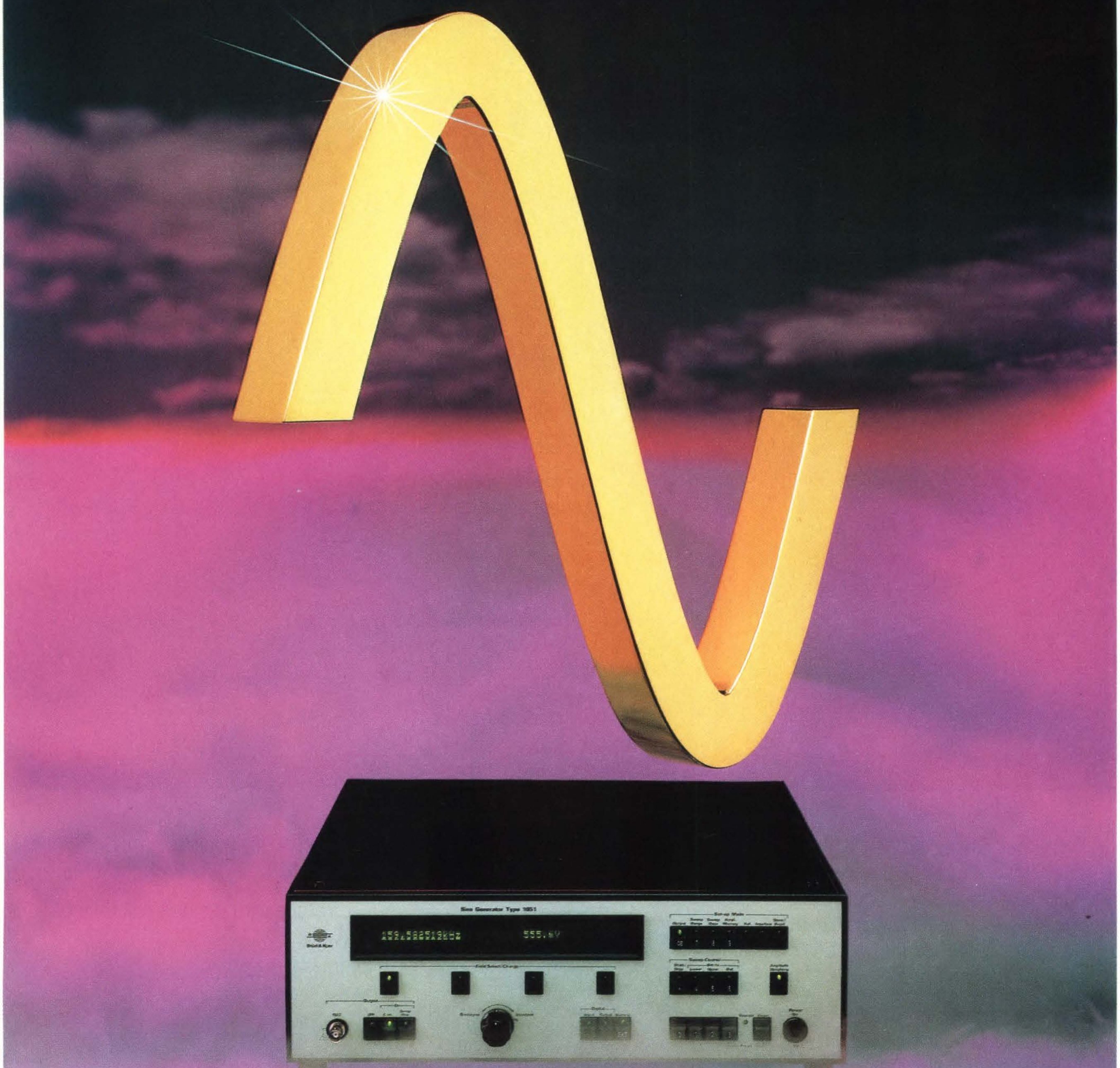
EDN101388

The Sine of a Good Generator



Purity • Precision • Speed

- typically 0,0006% (–105 dB) distortion in the audio range
- ±0,1192 mHz frequency accuracy throughout the 0,2 Hz to 200 kHz range
- precision attenuator with ±0,026 dB (±0,3%) accuracy across the entire 100 μV to 5 V range
- very fast response time for *all* functions via IEEE-488 interface
- heterodyne synthesis gives "instantaneous" settling (<0,1 ms) of frequency and amplitude
- memory sweep feature with pre-defined amplitude weighting
- two models: Sine Generator Type 1051 and Sine/Noise Generator Type 1049

Brüel & Kjær

Brüel & Kjaer Instruments, Inc. 185 Forest Street · Marlborough, MA 01752 USA · Telephone 617/481-7000

WORLD HEADQUARTERS: DK-2850 Nærum · Denmark · Telephone: +45 2 80 05 00 · Telex: 37316 bruka dk

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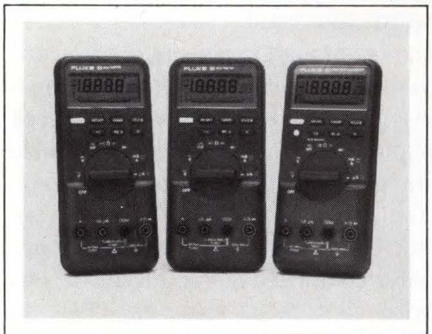
Taiwan (02) 713 9303 · USA (617) 481-7000 · Local representatives and service organisations world-wide

88-059



HAND-HELD DMMs

- *Provide 3¾-digit display*
- *Measure frequency, duty cycle and capacitance*

The models 83, 85, and 87 meters are environmentally sealed, hand-held units with 3¾-digit (4000-count) liquid-crystal displays. In addition to dc and ac voltage and resistance, the meters measure frequency, duty cycle, and capacitance. The 83's dc readings are accurate to within 0.3%; those of the 85 and 87 are accurate to within 0.1%. The meters also provide an analog readout in the form of a bar graph on the 83 and 85 and a pointer on the 87. This readout updates 40 times each second—60% faster than the analog readout on the vendor's 70-series instruments. For visibility in dimly lit locations, the 87 can provide back lighting for its display. The 87 also has a 4½-digit (20,000-count) display mode. The units withstand 1000V overloads in ohms and diode-test modes. In addition to functioning as a normal tilt stand, the flexible stand can suspend the meters from doors and pipes. 83, $189; 85, $219; 87, $259.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 443-5853, Ext 33.

Circle No 400

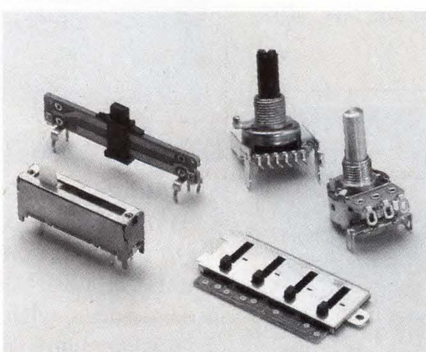
Philips Test and Measurement, Building HKF, 5600 MD Eindoven, The Netherlands. Phone local office.

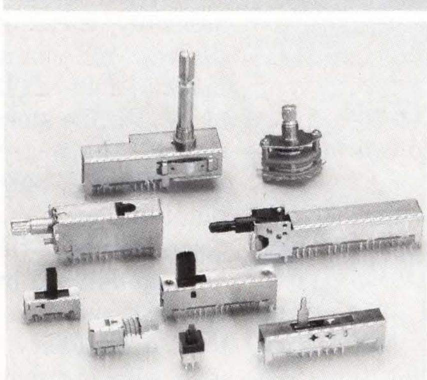
Circle No 401

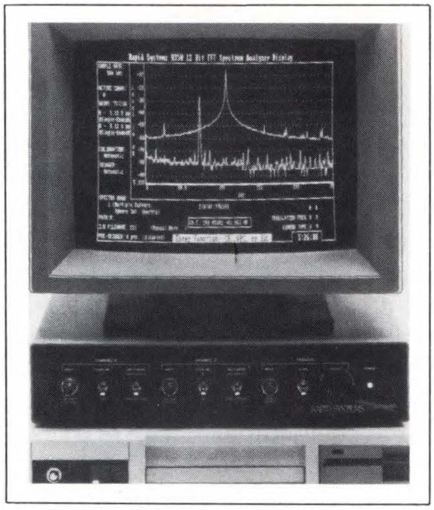
TRANSIENT RECORDER

- *Includes assembly-language drivers*
- *Two 12-bit ADCs provide simultaneous input*

The R1240 hardware/software package lets you use your IBM PC, PC/XT, PC/AT, or compatible as a transient recorder system. It employs two 12-bit ADCs with a 1-MHz rate for simultaneous input. Using the package, you can analyze signals with frequency components



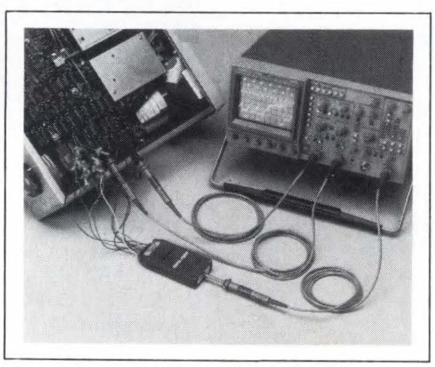




from dc to 250-kHz signals. It features software-selectable gains from 2 mV to 32V, and pretrigger and post-trigger capabilities. The 32k-byte memory/channel—expandable to 64k bytes—and the turnkey operation of the software provide the programming facilities. You access the software from C, Turbo Pascal, or Basic. The vendor provides samples of data-acquisition and data-display software with source code. $2995.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. TLX 265017.

Circle No 402



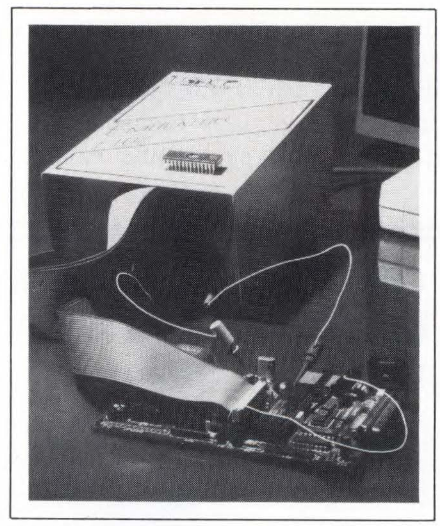
WORD RECOGNIZER

- *Converts scopes into logic-analysis tools*
- *Decodes words as wide as 16 bits*

The P6408 word-recognizer/trigger probe converts any oscilloscope into a logic-analysis tool. The probe works with TTL. It has a high threshold of 2V and a low threshold of 0.7V, and it gets its power from any 5V supply. To use the probe, you set dip switches to define the word you want recognized. When the incoming signals equal the word you set up, the probe issues a scope-trigger signal. If you supply a clock signal, the probe will synchronize its trigger output with the clock. You can attach the supplied grabber tips—which are on 20-cm-long, color-coded leads—to circuit nodes with centers as close as 0.050 in. $350.

Tektronix Inc, Box 3500, C1-820, Vancouver, WA 98668. Phone (800) 835-9433, Ext 170.

Circle No 403



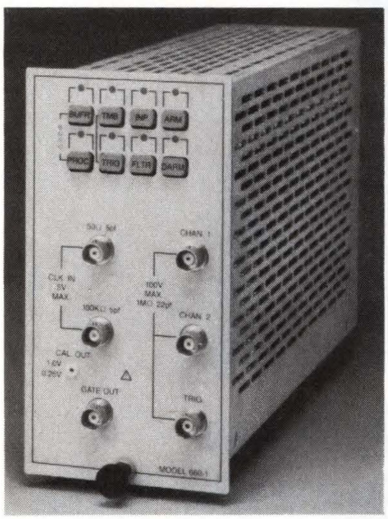
EPROM EMULATOR

- *Emulates ROMs to 1024k bits*
- *Allows program control and tracing as an option*

The E102 EPROM emulator emulates devices with 16 to 512k bits of storage; using an optional probe assembly, it can emulate 1024k-bit devices. You can also expand it to emulate four EPROMs simultaneously. For file storage and operator control, the instrument interfaces with IBM PCs and compatible computers via an RS-232C port. An unusual feature is the unit's ability—with an optional breakpoint card—to break and trace program execution, a capability normally associated with in-circuit emulators, not with ROM emulators. The trace buffer is 4k words deep. The unit accesses CPU control signals to allow you to define a 256-byte "window" in EPROM space that you can treat as system RAM. From $825.

Adams-Macdonald Enterprises Inc, 800 Airport Rd, Monterey, CA 93940. Phone (800) 777-1202; in CA, (408) 373-3607. TLX 882141.

Circle No 404



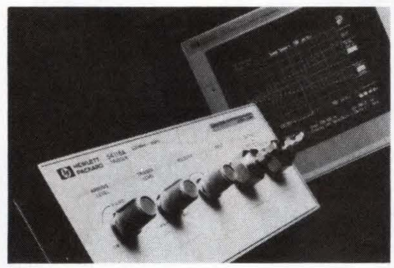
WAVEFORM SAMPLER

- *Digitizes to 9 bits at 250M samples/sec*
- *Stores 128k samples*

The 660-1 waveform sampler plugs into the vendor's Data 6100 mainframe. The plug-in unit has a single A/D converter that digitizes one or two channels of analog data. It can perform a total of 250-million conversions/sec to a resolution of nine bits; the unit's RAM can retain 128k samples. The memory can store data from one or both channels. When operating as a 2-channel instrument, the unit has single-ended inputs. When you use it as a 1-channel device, you can connect signals differentially. The instrument offers several unusual trigger modes. In one of these modes, you can define a voltage "window" and trigger a sweep when the signal either enters or leaves the window. For repetitive waveforms, the unit has a random equivalent-time sampling mode with a maximum effective sampling rate of 25G samples/sec and a bandwidth of 125 MHz. $7995. Delivery, 60 days ARO.

Analogic/Data Precision, 8 Centennial Dr, Peabody, MA 01961. Phone (617) 246-0300. TLX 6817021. FAX 617-531-4502.

Circle No 405



EVENT-TRIGGER UNIT

- *Triggers DSOs from events occurring at 18 GHz*
- *Allows trigger-point definition by level and slope*

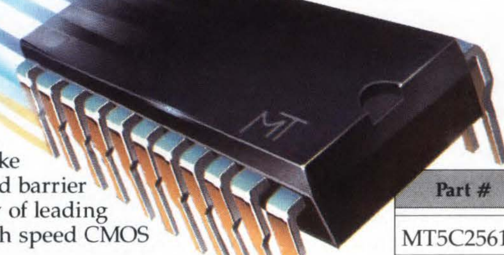
The HP 54118A event-trigger unit is an accessory to digital-storage oscilloscopes (DSOs), such as the vendor's HP 54120T. It allows you to trigger the scopes on signals that are not continuous waves (CW) and whose frequencies lie above the normal trigger range. The unit enables stable triggering on radar-pulse carriers, CW signals with large noise components, and radio-frequency bursts. Countdown synchronizers do not allow stable triggering from such signals. The unit allows you to define the trigger point based on the trigger signal's level and slope as you do when triggering from lower frequency sources. The unit covers a 0.5-to-18-GHz range; it provides hold-off delays of 50 to 200 msec. The output jitter is less than 3% of the input-signal period, and the output delay from the trigger edge is 4 nsec. $8925, including cables and accessories for viewing the trigger signal. Delivery, six weeks ARO.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local sales office.

Circle No 406

Text continued on pg 306

SUPER FAST SRAM



Available Now
256K 25ns/64K 15ns

Micron just broke the SRAM speed barrier with our family of leading edge, super high speed CMOS SRAMs.

We've applied the same state-of-the-art design and process technology used for our high quality DRAMs in development of our fast static RAMs — with some amazing results.

At an incredible 25ns for 256K and 15ns for 64K, our SRAMs are breaking speed records. And we're not just sampling product, we're shipping production volumes.

Choose from a wide variety of components in DIP, SOJ and LCC packages, with densities from 16K to 256K and organizations of x1, x4 and x8.

And like all Micron memory products, our SRAMs are backed by the type of strong sales, customer service and technical support that keeps you on the leading edge.

For additional information on how you can break the SRAM speed barrier, call 208-386-3900.

Micron, it's a name worth remembering.

Part #	Organization	Speed*	Packages
MT5C2561	256K X 1	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C2564	64K X 4	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C2565	64K X 4 $\overline{OE}$	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C2568	32K X 8	**25ns**	PDIP, CDIP, SOJ, LCC
MT5C6401	64K X 1	**15ns**	PDIP, CDIP, SOJ
MT5C6404	16K X 4	**15ns**	PDIP, CDIP, SOJ
MT5C6405	16K X 4 $\overline{OE}$	**15ns**	PDIP, CDIP, SOJ
MT5C6406/7	16K X 4 S.I/O	**15ns**	PDIP, CDIP, SOJ
MT5C6408	8K X 8	**15ns**	PDIP, CDIP, SOJ, LCC
MT5C1601	16K X 1	**15ns**	PDIP, CDIP, SOJ
MT5C1604	4K X 4	**15ns**	PDIP, CDIP, SOJ
MT5C1605	4K X 4 $\overline{OE}$	**15ns**	PDIP, CDIP, SOJ
MT5C1606/7	4K X 4 S.I/O	**15ns**	PDIP, CDIP, SOJ
MT5C1608	2K X 8	**15ns**	PDIP, CDIP, SOJ

*Slower speeds also available.

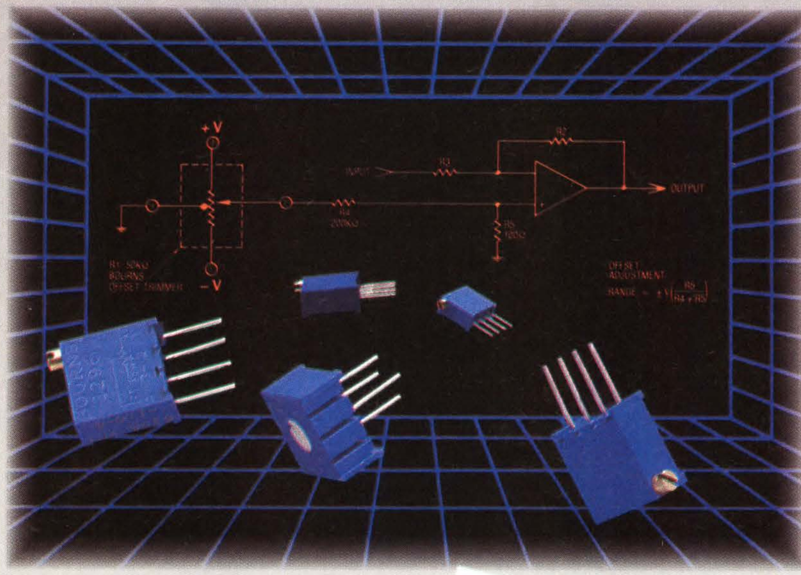
MICRON
TECHNOLOGY, INC.

MICRON TECHNOLOGY, INC., 2805 E. COLUMBIA ROAD, BOISE, IDAHO 83706 208-386-3900

BOURNS

Vos COMPENSATOR

IMPROVE OP AMP ADJUSTMENT WITHOUT ALL THE TRIMMINGS.



Bourns Trimpot simplifies the whole process of trimming op amp circuits. The new OT1 offset trimming potentiometer improves op amp circuit performance. It cuts component count. It saves board space. There's nothing else like it, anywhere!

Better Circuit Performance

This op amp offset voltage adjustment component isolates both op amp power supplies to reduce the negative effects of drift. By using a center tap design, the OT1 effectively separates the two power supplies, resulting in up to a 10X improvement in voltage offset error caused by power supply drift.

FREE SAMPLES
Try the new OT1 in your own design at no cost. Send for this application synopsis and product guide today, which includes a FREE sample offer. Just circle the reader service number below.

Parts/Space Reduction

The OT1 cuts component count, too. Until now, you needed a trimming potentiometer, various fixed resistors and diodes to adjust most op amp offset voltages accurately. Now with the OT1, most diodes can be eliminated and fixed resistor count can be reduced. Circuits can be simplified, and board space can be reduced while improving the operating accuracy of the op amp circuit.

Application Specific

The new OT1 is the most recent example of this Bourns commitment to offer products that satisfy real life design problems, like yours. Application specific products require an unending search for ways in which to serve you better. We call it "Customerized Technology," and you'll see the advantages.

Contact us today for all the details.

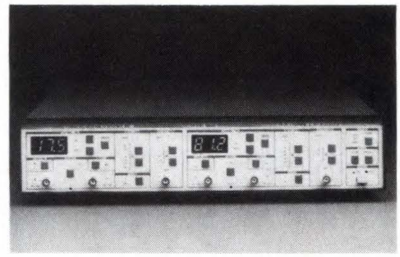
BOURNS®

BOURNS TRIMPOT

After 40 years, there's still no equivalent.

Bourns, Inc., 1200 Columbia Avenue, Riverside, California 92507; (714) 781-5050; TLX: 676-423; TWX: 910-332-1252; FAX: 714-781-5700. European Headquarters: Zugerstrasse 74, 6340 Baar, **Switzerland:** 042-333333; TLX: 868722; FAX: 042-319017. **Benelux:** 070-874400; TLX: 32023. **France:** 01-40033604; FAX: 01-40033614. **Germany:** 0711-22930; FAX: 0711-291568. **Ireland:** 021-357001; FAX: 021-357443. **United Kingdom:** 0276-692392; FAX: 0276-691037. Asia Pacific Headquarters: 1401 Citicorp Centre, 14th Floor, 18 Whitfield Road, **Hong Kong:** (852) 5-702171; TLX: 82953 BAPHK HX; FAX: 852-5-664341; CBL: BOURNSASPA HONGKONG. **Singapore:** (65) 339-3331; FAX: (65) 339-1116.

CIRCLE NO 84



PROGRAMMABLE FILTER

- *Lets you store 10 instrument configurations*
- *Features a 1- to 100-kHz frequency range*

Employing programming capabilities, the SR640 dual-channel filter lets you optimize signal-processing applications. It features an 8-pole, 6-zero elliptic filter and a 1- to 100-kHz frequency range. With a 0.1 dB/octave roll-off, the filter has an 80-dB stopband attenuation. It provides a 60-dB prefilter gain with a 20-dB postfilter gain. You can bypass the filter and leave both the prefilter and postfilter gains active, according to the vendor. You can store a maximum of 10 instrument settings in a nonvolatile RAM. All μP components are optically isolated from the filter. IEEE-488 and RS-232C interfaces are standard. $2990.

Stanford Research Systems Inc, 1290D Reamwood Ave, Sunnyvale, CA 94089. Phone (408) 744-9040. TLX 706891.

Circle No 407

SYNTHESIZER

- *Covers 10 MHz to 18.4 GHz with 0.4-Hz resolution*
- *Switches frequencies in <1 μsec*

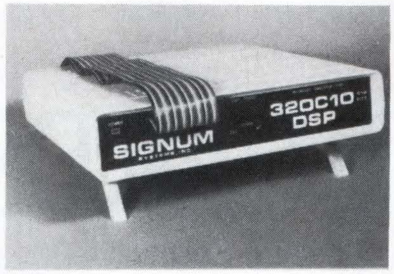
The FS-2000A-18 direct frequency synthesizer covers a 10-MHz-to-18.4-GHz range with 0.4-Hz resolution. You can program it by supplying parallel BCD signals. It switches between any two frequencies in <1 μsec. With the carrier frequency set to 18.4 GHz, noise is less than −108 dBc/Hz at a frequency of 20 kHz from the carrier. Spurious signals are less than −70 dBc up to 2.3 GHz and less than −52 dBc at 18.4 GHz. Frequency stability is better than 5×10^{-9}/day after 24 hours. Output power is 10 dBm into 50Ω and is flat within 2 dB across the frequency range; harmonics remain less than −25 dBc. The unit occupies 5¼ in. in a standard 19-in. rack. $89,500. Delivery, 16 to 20 weeks ARO.

Comstron Corp, 10 Hub Dr, Melville, NY 11747. Phone (516) 756-1100.

Circle No 408

DSP EMULATOR

- *Supports TMS320C10 family to 32 MHz*
- *Operates nonintrusively and transparently in real time*



The ICE Model E-232-DSP-10 emulates the TMS320C10 family of DSP microcontrollers at 32 MHz interactively, nonintrusively, and transparently. According to the vendor, competitive instruments cannot emulate the full range of processor capabilities in real time or they usurp target-system resources, such as one or more stacks. The unit allows you to define three sets of events that, when recognized, break program execution or control tracing. These events consist of recognition of any 8k addresses or address ranges; recognition of data that matches, exceeds, or is less than a pattern whose length can be 8k bits; occurrence of CPU operations such as read, write, I/O, DMA, or opcode fetch; and occurrence of external inputs of programmable polarity qualified by programmable expressions. $5995.

Signum Systems Inc, 1820 14th St, Santa Monica, CA 90404. Phone (213) 450-6096.

Circle No 409

GENERATOR

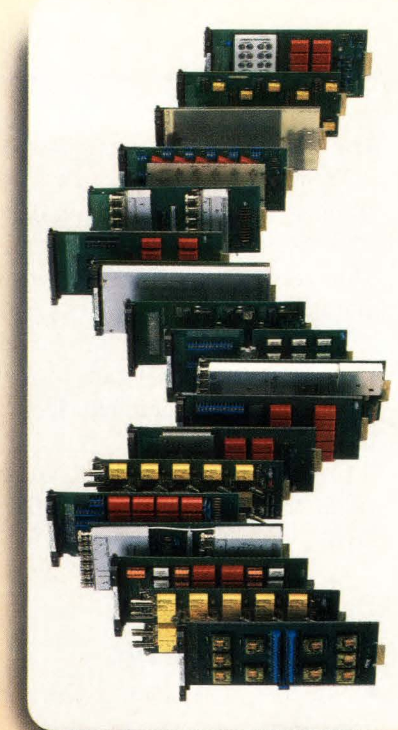
- *Produces sine, square, and triangular waves*
- *Sweeps 1000:1 ranges from 0.2 Hz to 2 MHz*

The 3017 sweep/function generator produces sine, square, and triangular waves, as well as CMOS- and

KEITHLEY ON SWITCHING:

IT'S IN THE CARDS

Our line of 18 signal switching cards is the widest variety anywhere, so you can configure a system to match your signal types without sacrificing system performance▲



SIGNAL INTEGRITY

To get the most from your test system, you must make sure your signals are switched without attenuation, distortion or alteration by the switching and interconnect▲Since Keithley has more switching cards than anyone, you can be assured of signal integrity, no matter what the test▲ Choose from:

Matrix	Most flexible
Scan/Multiplex	1, 2, or 4 pole switching
Sensitivity	Currents to 40fA, voltages to 30nV
High Level	Currents to 5A, voltages to 1000V
Bandwidth	Frequencies to 500MHz
Temperature	Thermocouple cards with $<1\mu V$ offset and built-in reference
Special Applications	Hall effect, nanovolt switching, Kelvin switching, universal adapter

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Keithley switches let you customize applications by mixing cards in two or 10-slot mainframes▲ For larger systems, you can connect up to five mainframes and program them at one IEEE-488 address▲

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SOURCE • MEASURE • CONNECT

KEITHLEY

TTL-compatible pulse trains, at frequencies from 0.2 Hz to 2 MHz. Using an external or internal sweep source, you can obtain swept-frequency outputs with a 1000:1 max:min frequency ratio. The internal source allows you to set the sweep time from 0.5 to 30 sec. The unit also contains a dc-bias voltage source whose output you can add to the waveforms. Multiple sets of terminals enable you to obtain several types of output simultaneously. Sinewave distortion is less than 1%; squarewave symmetry (at 100 kHz) and triangular wave linearity are better than 98%. $319.

B&K Precision, 6470 W Cortland St, Chicago, IL 60635. Phone (312) 889-1448.

Circle No 410

ACOUSTIC TESTER

- *Provides chirp, impulse, or tone stimulus*
- *Records, averages, and analyzes system response*

The Sysid is a PC-based acoustic-measurement system built around the vendor's 16-bit DSP board. It simultaneously acquires data on two channels with 16-bit resolution at 50k samples/sec. It also stimulates the system under test with a chirp, impulse, or tone, and analyzes the system response. The measurement system makes ratiometric measurements and saves data on disk or prints it. $2995.

Ariel Corp, 110 Greene St, Suite 404, New York, NY 10012. Phone (212) 925-4155. TLX 4997297. FAX 212-966-3981.

Circle No 411

IEEE-488 INTERFACE

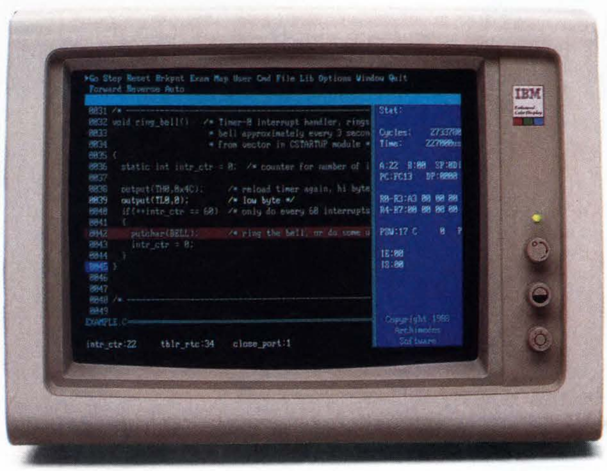
- *Features data-transfer rates to 500k bytes/sec*
- *Provides 24-bit addressing*

The GPIB-S3/4 kit helps you control instrumentation in VME-based, multitasking environments. The kit consists of an interface board, an adapter bracket, a cable, a Unix software handler on a Sun cartridge, and documentation. With 500k-byte/sec max data-transfer rates and 24-bit addressing, this interface provides full DMA. You can perform several tasks concurrently with different devices. The kit provides IEEE-488 synchronization detection. Over 30 IEEE-488 functions and an interactive program with a C interface let you troubleshoot devices. With an adapter bracket and Unix software, $2745; without an adapter bracket, $1945.

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (800) 433-3488. TLX 756737.

Circle No 412

Code and debug micro-controllers in C without ever leaving your PC



Now you can run, debug, and test Archimedes Microcontroller C code right on your PC, and you don't even need any prototype hardware. Combined with Archimedes C, SimCASE allows you to speed up software development. You can test-run your software ideas before you even commit to a micro-controller design. It's like having a microcontroller built into your PC.

You'll have every traditional debugging tool at your fingertips, including trace, step and break-points. So you can fully debug microcontroller code at the C source level. Of course, you can use SimCASE to debug at the Assembly level too, if necessary.

Speed up software development on all of today's most popular microcontrollers. Archimedes Microcontroller C and SimCASE are available for a wide variety of microcontrollers, including: Motorola's 6801 and 68HC11, Intel's 8051 and 8096/196, Zilog's Z80/Z180, Hitachi's 6301 and 64180.

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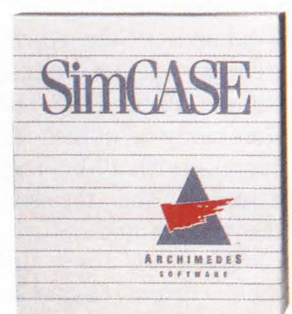
With the Input Stimulus Generator you can simulate real-time I/O intensive applications right on your PC.

Then use the Performance Analysis Tool to get the execution time of every block and line of code and identify any performance bottlenecks in your design. You can run this assessment for worst-case scenarios, including hardware tolerances.

All before you even commit to hardware.



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CIRCLE NO 67

NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

DATA MANIPULATOR

- *Reads and plots an unlimited number of data points/set*
- *Can import data from spreadsheets*

TECH*GRAPH*PAD integrates the data-retrieval, data-manipulation, and data-output requirements of engineers and scientists. Among the major enhancements of release 3.0 are a worksheet "browse" mode that brings up Lotus 1-2-3, Symphony, or Quattro spreadsheets and lets you retrieve data from them; an improved user interface; user-controllable color control for both on-screen display and hard-copy output; and drivers for HPGL-compatible laser printers and color printers. This release lets you read an unlimited number of data points/set; provides error bars, superscripts, and subscripts; and can create both Lotus and HPGL .PIC graphics files that you can use in conjunction with word-processing or desktop-publishing software to integrate text and graphics. The program runs on IBM PCs and compatibles, PS/2s, Apollo Series 3000/4000 workstations that have an MS-DOS emulator, and VAX/VMS machines that have MS-DOS services. $395; upgrade for current users, $99.

Binary Engineering, 100 Fifth Ave, Waltham, MA 02154. Phone (617) 890-1812.

Circle No 415

SOFTWARE MANAGER

- *Provides change- and version-control under Xenix*
- *Provides complete audit trail of all modifications*

The Aide-de-Camp (ADC) software-management system provides change-control, version-control, configuration-management, and information-management facilities for microcomputer systems, running under the Xenix operating system. It can automatically create structural documentation and build or back up a software system from the appropriate modules. The system provides a complete audit trail of all modifications to the modules that compose a given system. According to the vendor, ADC is the only configuration-management system that tracks the relationships between software entities at each release. It stores changes as separate, program-related entities that you can include in, or delete from, subsequent releases; this feature facilitates the management of parallel versions, and the migration of enhancements and bug fixes from one program path to another. The system has been available for workstations since 1982, and this version for microcomputer systems that run under the Santa Cruz Xenix operating system is now available. Xenix version, $2500; workstation and minicomputer versions, $5800 to $15,200, depending on the host configuration.

Software Maintenance & Development Systems Inc, Box 555, Concord, MA 01742. Phone (508) 369-7398.

Circle No 416

FAX SOFTWARE

- *Lets you send CAD drawings from a PC to a FAX machine*
- *Can handle E-size drawings and can add a header message*

CAD-Fax is a communications package that consists of menu-driven software and a half-size fax modem card that plugs into IBM PCs, PS/2s, and compatibles. You can transmit any CAD file that is written as a plot file in HPGL or AutoCAD PRP format. The system automatically converts the file to CCITT Group III fax format and sends it over the PSTN at 9600 bits/

sec. If line quality is poor, the modem automatically drops its transmission rate to 7200, 4800, or 2400 bps to obtain error-free transfer. When sending drawings that are too large for a fax machine to handle, the system automatically divides each drawing into the appropriate number of 8½-in. strips and inserts alignment markers so that the recipient can easily reconstruct the full-sized drawings. You can also prefix each drawing with a customized header message of as many as 400 characters—no header sheet is needed. Because the system eliminates the need to cut up drawings at the sending end as well as the scanner, it not only saves time but takes full advantage of the 200-dots/in. resolution of the receiving fax machine. It produces clean output, unmarred by the spots and blurring that you often find on letters received by fax machines. Complete hardware/software package, $1995.

GammaLink, 2452 Embarcadero Way, Palo Alto, CA 94303. Phone (415) 856-7421. TLX 4992108. FAX 415-494-7042.

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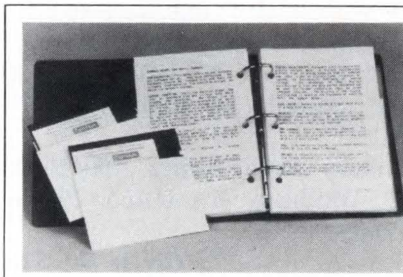

DATA ANALYZER

- *Lets you analyze data as you acquire it*
- *Analyzes both single data points and waveforms*

SNAP-CALC is a general-purpose software package that allows you to perform both concurrent processing of data during acquisition and postprocessing of data stored in a file. You can use postprocessing to perform automatic analysis of multiple files without operator intervention. The software is menu-driven to make setup easy. Mathematical operations include the calculation of arithmetic, trigonometric, calculus, logic, correlation, and statistical functions. You can analyze single data points or as many as eight waveforms with as many as 32,000 data points. The package works alone or in combination with the vendor's Snapshot Storage Scope or Snap-FFT packages. $495.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. TLX 503989. FAX 617-880-0179.

Circle No 418

8051 DEVELOPER

- *Lets you program in assembly language or Forth*
- *Lets you use an IBM PC to develop 8051 software*

chipFORTH 8051 is an interactive software cross-development package that runs on an IBM PC or compatible and includes a real-time, multitasking executive for embedding in an 8051-based target system. The package includes an editor, a compiler, an assembler, and a debugger. You can write programs for the target system in 8051 assembly language or in high-level Forth and download the executable object code to the target system via a serial link. A 200-byte removable "talker" program also uses the serial link and allows you to execute and interact with the software on the target, using the host PC as a virtual terminal. This talker program eliminates the need for an in-circuit emulator. The real-time executive can handle a virtally unlimited number of tasks; creation and assignment of these tasks is under complete control of the programmer. The executive allows tasks to use a real-time clock (if one is present in the target system) for timing events asynchronously. The software comes with a Cavendish Automation CA-7030-CPU/A prototyping board, which has 16k bytes of memory that you can configure either as RAM or as EPROM. The board also has 8k bytes of static RAM and multiple I/O ports. $3750.

Forth Inc, 111 N Sepulveda Blvd, Manhattan Beach, CA 90266. Phone (213) 372-8493.

Circle No 419

RISC DESIGN TOOLS

- *Includes simulator for UT1750AR µP*
- *Assembler and linker are written in C for portability*

The UT1750 design toolkit allows you to develop software for the vendor's UT1750AR RISC µP on an IBM PC or compatible. The RASM assembler translates RISC mnemonic syntax into relocateable UT1750AR machine-language modules and provides macro facilities as well as a full complement of standard assembler directives (including EXTERNAL and PUBLIC). You can partition your programs into manageable segments and then link these to each other and to library routines to form a complete, executable program. The RLNK linker lets you declare specific memory segments as RAM or ROM, produces a complete table of symbols, and converts the output to Intel Hex format for downloading to a PROM programmer. The RASM/RLNK package also includes a monitor that lets you read and change the µP's internal registers and external memory via the processor's built-in serial port. IRSIM is an interactive hardware/software simulator that allows you to develop application software before the target hardware is available. It performs critical-timing analysis, symbolic disassembly of RISC code, and reassembly/relinking of programs without leaving IRSIM. The simulator is also available with a debug tool that both communicates with and controls the target RISC processor via the chip's built-in serial port. RASLN package (RASM, RLNK, and monitor), $1000; IRSIM, $1750; SIMDB (IRSIM with debug tool), $2195; UT1750 toolkit (RASLN and SIMDB), $2995.

United Technologies Microelectronics Center, 575 Garden of the Gods Rd, Colorado Springs, CO 80907. Phone (719) 594-8158.

Circle No 420

REAL-TIME ADA OS

- *Allows both multitasking and multiprocessing*
- *Can handle a mixture of CPUs in the 68000 family*

MTOS/UX-Ada is a real-time Ada executive for embedded systems that can run as many as 16 tightly-coupled CPUs in the same system. The CPUs can be any mix of 68000, 68010, 68020, or 68030. The executive supports all features of Telesoft's TeleGen2 Ada system; Ada primitives that have real-time aspects (Rendezvous, Delay, File I/O, Text I/O) are handled transparently by MTOS-UX. All other features, such as event flags, signals, semaphores, memory pools, and variables used for coordination and synchronization, are available as Ada packages. You can also integrate application tasks that are written in languages other than Ada, such as C or assembly language. $45,000 to $115,000.

Industrial Programming Inc, 100 Jericho Quadrangle, Jericho, NY 11753. Phone (516) 938-6600.

Circle No 421

DATA-SAMPLING TOOL

- *Lets you sample and store 15M data points in one stream*
- *Allows sampling at rates as high as 100,000 samples/sec*

SNAP-STREAM is a menu-driven software package that runs on IBM PCs and compatibles and can sample, and store to disk, as many as 15 million data points in one continuous stream. The amount of free space on the storage device (hard disk, RAM-disk, or floppy disk) de-

termines the upper limit on the number of data points acquired. Automatic sensing predicts and displays the probable disk-throughput limit, which depends on the processor speed and storage efficiency of the disk drive. This limit is maximized if the free space is contiguous; fragmentation caused by deleted files may considerably reduce it. If the selected sampling rate approaches the predicted maximum, the program pretests the actual streaming rate to ensure that the system will perform satisfactorily and to avoid overrun errors and loss of data during the run. The package includes a disk optimizer utility that packs existing files so that all free space is contiguous. To run the program you need an IBM PC or compatible that has at least 640k bytes of RAM, the vendor's SNAPSHOT Storage Scope software, and an Analog Devices I/O board in the RTI-800/815 or RTI-850/860 series. SNAP-STREAM and SNAPSHOT together, $840; SNAP-STREAM alone for SNAPSHOT users, $445.

HEM Data Corp, 17336 Twelve Mile Rd, Suite 201, Southfield, MI 48076. Phone (313) 559-5607.

Circle No 422

C CROSS-COMPILER

- *Lets you develop C programs for 68000-based machines*
- *Supports ANSI extensions to the C language*

Two C cross-compiler packages let you use an IBM System/370 running VM/CMS to develop software for target systems that are based on the Motorola MC68000 family of µPs. Both packages generate code that works with 68000, 68008, 68010, 68020, and 68881 processors. The first package lets you develop software that will run on embedded systems and consists of the optimizing cross-compiler, runtime libraries, command driver, and source-level debugger. You'll need a Motorola-style assembler/linker package to convert the assembly-language output of the compiler to executable code. The other package is self-contained and lets you develop C programs for 68000-based machines that run under the Unix operating system. It consists of the cross-compiler, a listing cross-assembler, a linker, program-support utilities, ANSI libraries, and support for the Common Object-File Format. From $10,000 for the embedded-system package; from $15,000 for the Unix package.

Whitesmiths Ltd, 59 Power Rd, Westford, MA 01886. Phone (800) 225-1030; in MA, (508) 692-7800. FAX 508-692-3561.

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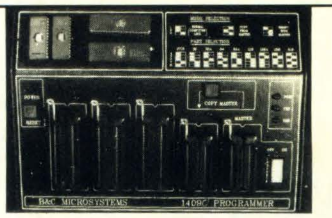

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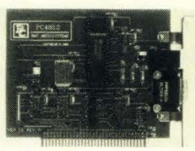

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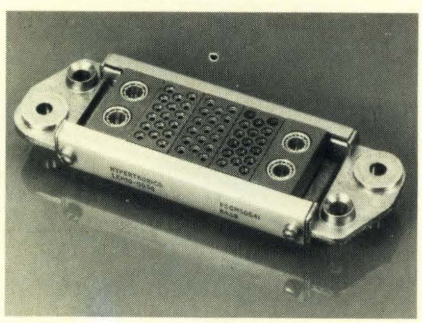

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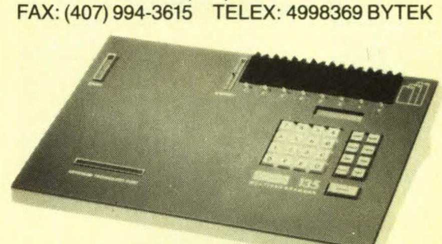

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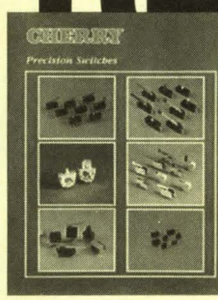

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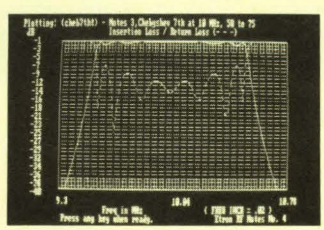

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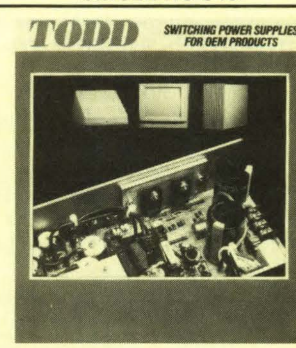

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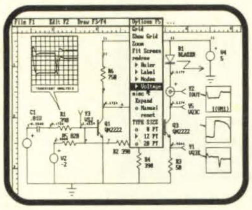

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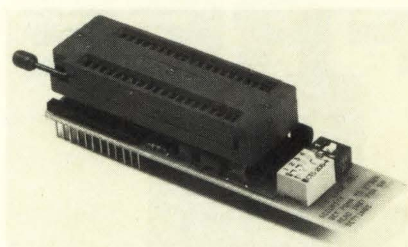

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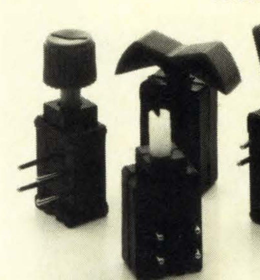

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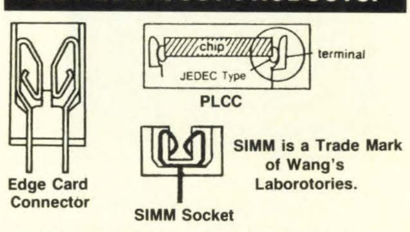

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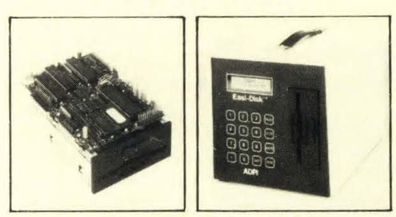

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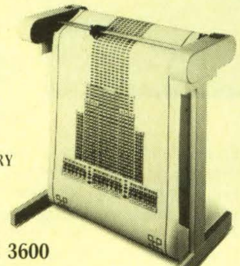

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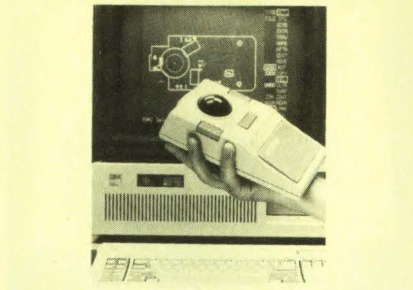

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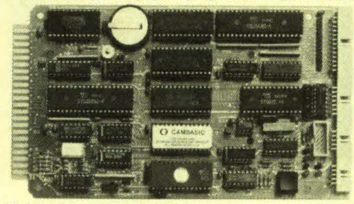

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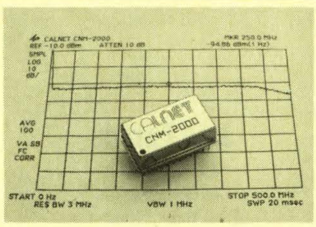

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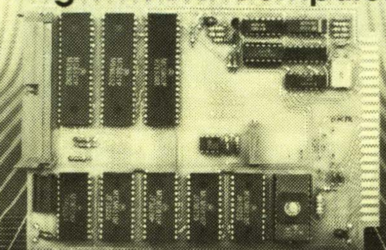

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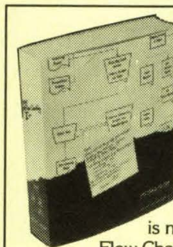

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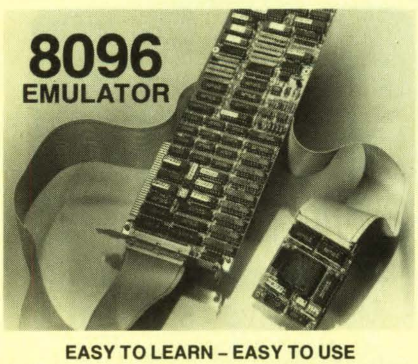

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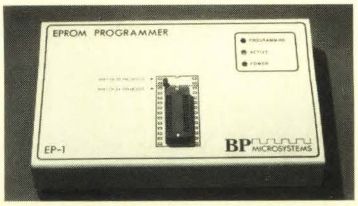

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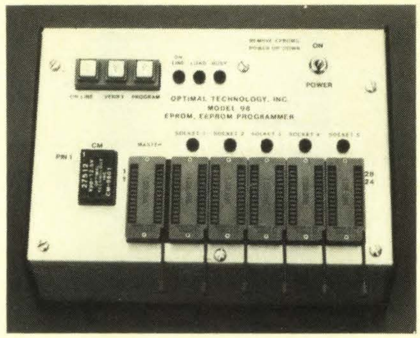

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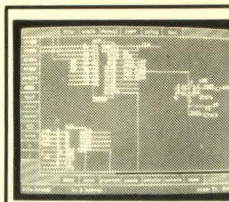

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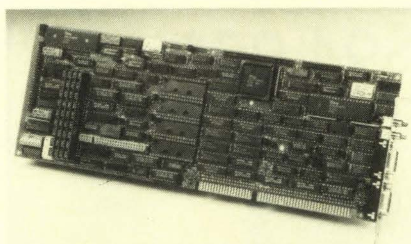

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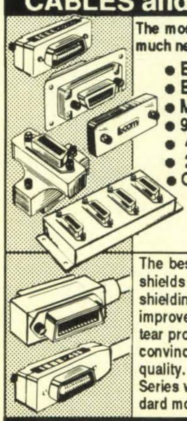

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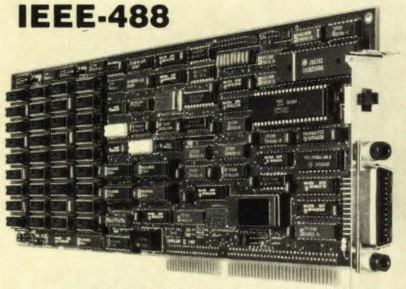

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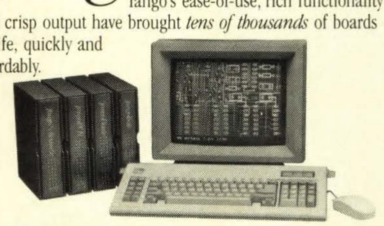

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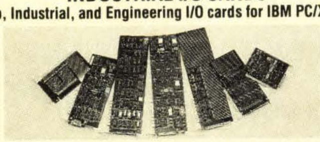

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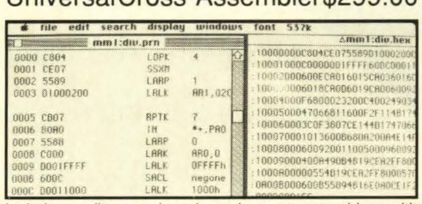

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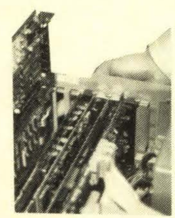

- Allows card insertion and extraction without power on/off cycles
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RS232 Downloadable PROM
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RS232

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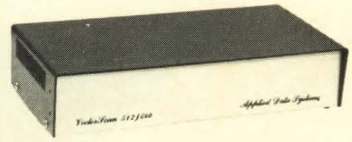

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CIRCLE NO 784

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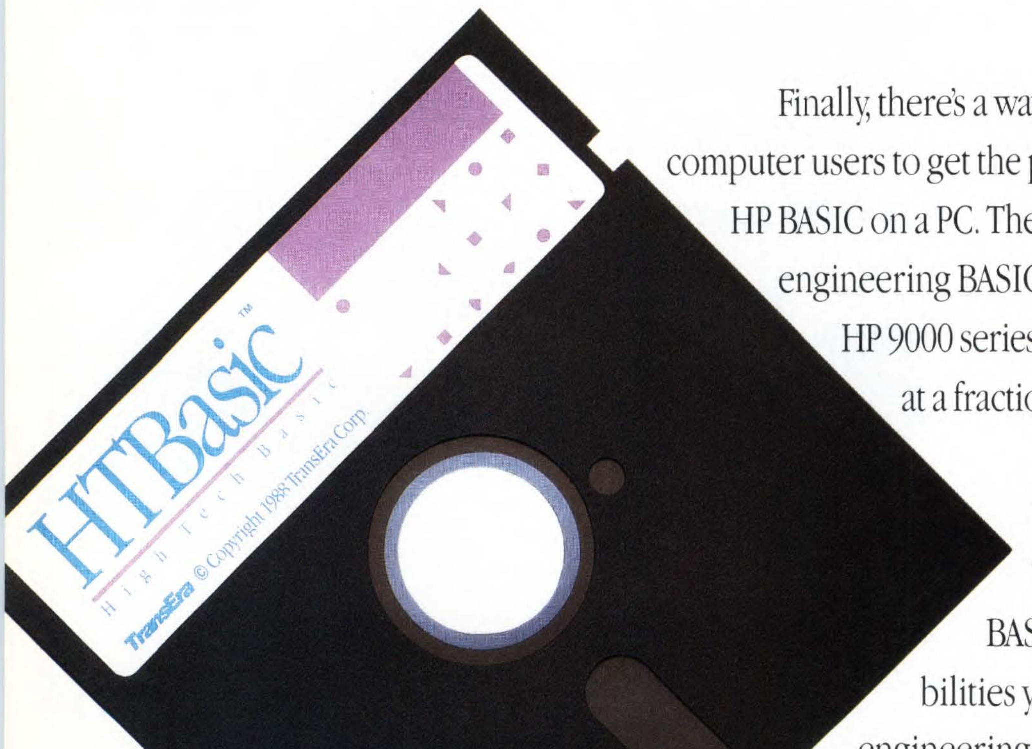
Feed this to your PC and it'll think it's an HP BASIC workstation.



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CIRCLE NO 163

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But, that's not all. Seiko Instruments line thermal printers are renowned for their quiet-as-a-feather operation. Since the entire LTP Series is small and compact, requiring less power than the competition, they're ideal for mobile applications, and fit easily into your most space-saving designs.

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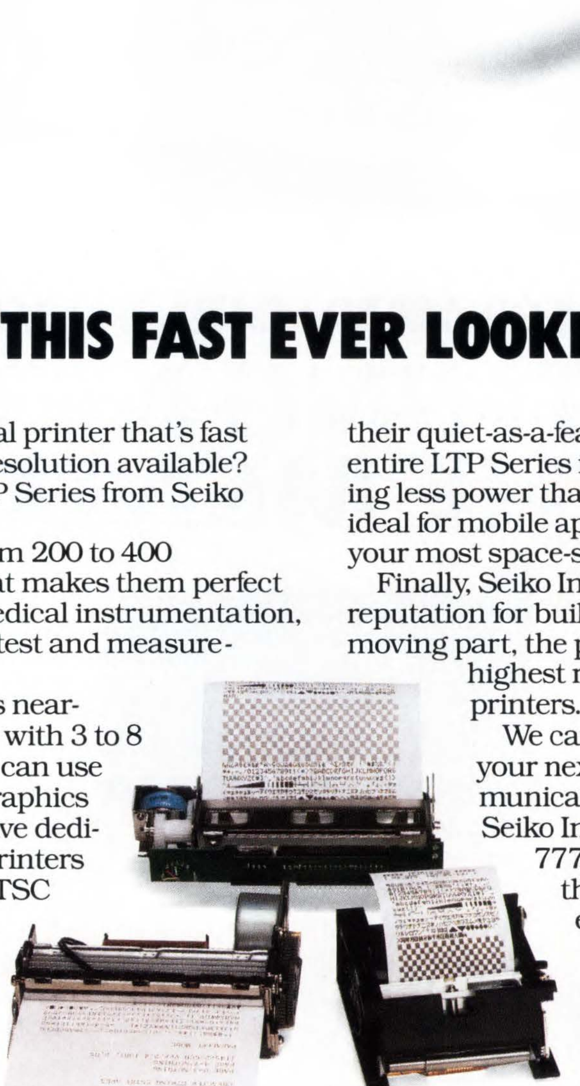

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CIRCLE NO 175

IEEE announces advanced 488 standards

Digital Interface for Programmable Instrumentation (ANSI/IEEE Std 488.1) and *IEEE Std 488.2 Standard Codes, Formats, Protocols, and Common Commands for Use with ANSI/IEEE Std 488.1-1987* (ANSI/IEEE Std 488.2) offer higher productivity, improved test quality, reduced costs, and more flexible performance and configuration of the test system. The first document updates the 1978 IEEE-488 Standard, specifying the basic communications link between as many as 14 devices and a controller, such as a personal computer. The other publication covers the syntax and protocols of messages sent between the devices and the controller in an IEEE-488 bus system and explains how to handle status, error reporting, and high-level programming. ANSI/IEEE Std 488.1, nonmembers, $30; members, $21. ANSI/IEEE Std 488.2, nonmembers, $52; members, $36.40.

The Institute of Electrical and Electronics Engineers Inc, Standards Office, 345 E 47th St, New York, NY 10017.

INQUIRE DIRECT

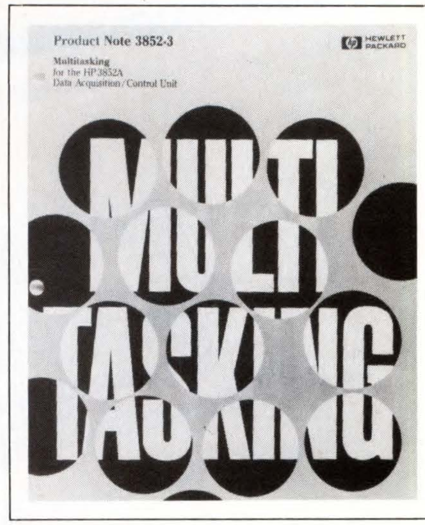
Sampling analog data at a 2G-sample/sec rate

The vendor's Product Note HP 54111D-1 explains how to sample analog data at a rate of 2G samples/sec, using the HP 54111D digitizing oscilloscope. After introducing the device in a general description, the note describes how to implement the HP 54111D, using Basic software. A section on theoretical performance goes on to explore what level of performance can be expected from interleaving two channels. The publication concludes with a description of the typical performance you can expect when you use this instrument.

Hewlett-Packard, 19310 Pruneridge Ave, Cupertino, CA 95014.

Circle No 426

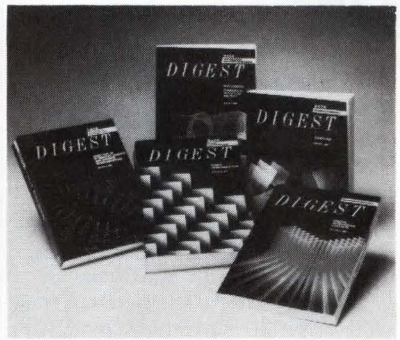
Note documents data acquisition/control system



In addition to providing programming examples, Product Note 3852-3 describes how the multitasking features of the HP 3852A data acquisition/control system let you space time-critical decisions in relation to the application. It explains how you can prioritize, download, and run tasks independently under four different conditions. The note examines each of these conditions and gives examples of how you can implement the programs.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014.

Circle No 427



Simplify selection of ICs and discrete semiconductors

The vendor continues to release its complete line of five integrated-circuit and five discrete-semiconductor digests. The improved format design helps to simplify the device-selection process. These references offer the following features: consistent device pinout information; product identification by function, generic part number, and specific manufacturer's part number; electrical characteristics for every part number in each of the five digests; discontinued device identification; and alternate sources for every device. Each IC Digest, $110 annually; optional quarterly updates, $60; total annual subscription with quarterly updates, $170; each Discrete Semiconductor Digest, $100 annually; optional semiannual updates, $25; total annual subscription with semiannual updates, $125. The digests are also available on magnetic tape.

DATA Business Publishing, Box 26875, San Diego, CA 92126.

INQUIRE DIRECT

Disk describes C support tools

This demonstration disk presents the Micro/C programming-language support tools for single-chip μCs. It also details MS-DOS-based cross-compilers for the 8051 and the Z8 and Super8 processors. The disk spotlights standard and enhanced features of C. Further, it provides examples of Micro/C support for memory maps, interrupts, and on-

LITERATURE

chip peripherals; sample C and assembly-code listings are included.

Micro Computer Control, Box 275, Hopewell, NJ 08525.

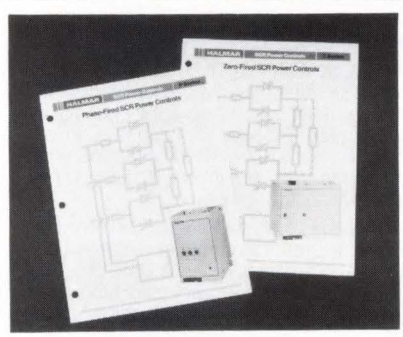
Circle No 429

Source book categorizes DPMs and printers

This 48-pg industrial source book highlights numerous applications, wiring diagrams, 4- to 20-mA process loop schemes, suggestions for use, and prices for a wide variety of products. A listing of an expanded line of digital panel meters includes a battery-operated high-speed counter, a portable LCD voltage-input DPM, and a micro-size RTD-input DPM.

Acculex, 440 Myles Standish Blvd, Taunton, MA 02780.

Circle No 430

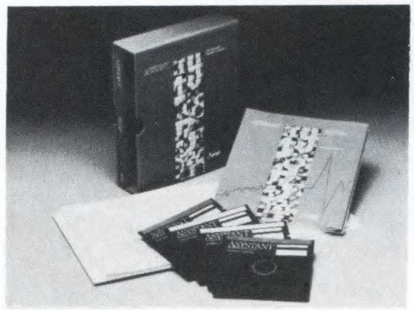


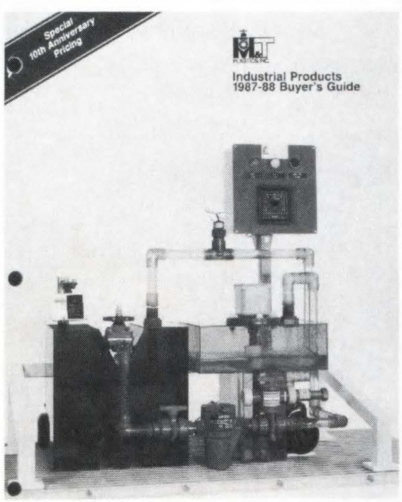
Pamphlets detail SCRs

These two brochures highlight the features of the company's zero- and phase-fired SCRs. These features include digitally controlled firing circuits, variable-time-base control, phase-locked-loop synchronization, and P Series control options. Dimensional drawings and tables, model tables with output power ratings, and ordering information complete the publications.

Halmar Electronics Inc, 900 N Hague Ave, Columbus, OH 43204.

Circle No 431





Buyer's guide focuses on industrial products

The vendor presents its 10th anniversary issue of the Industrial Products 1987-88 Buyer's Guide. The 170-pg catalog contains listings with specifications and prices for a wide selection of industrial thermoplastics, pipes, fittings, and valves. Other listings include flow and analytical instruments, recorders, and metering pumps.

M&T Plastics Inc, 6715 Joy Dr, East Syracuse, NY 13057.

Circle No 432

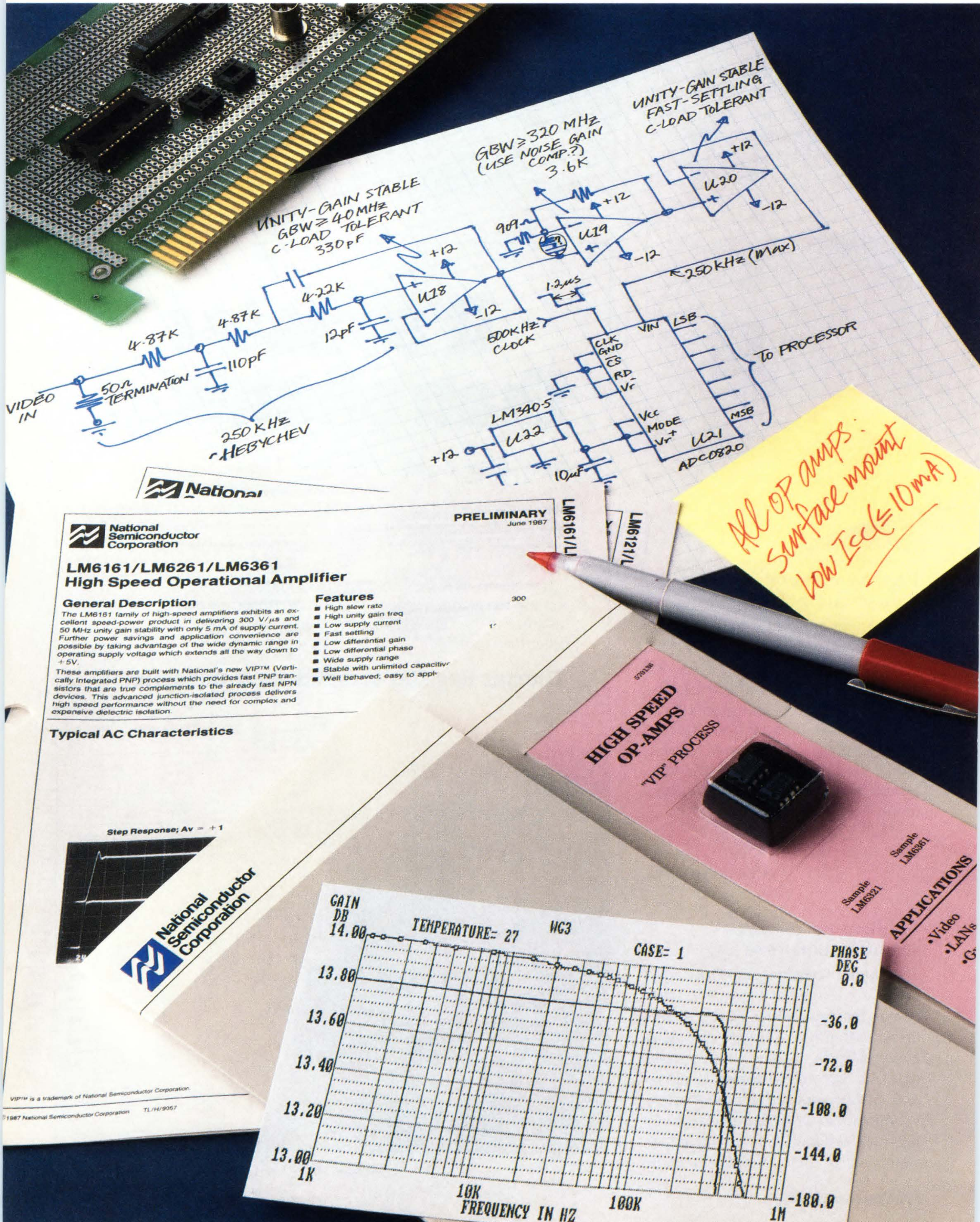
Publication features scientific software

The 6-pg brochure, *Asystant, The Scientific Number Cruncher,* discusses the capabilities of the menu-driven scientific software for data analysis and graphics. It describes data file I/O and processing, array and matrix operations, statistics, waveform and signal processing, polynomials and differential equations, curve fitting, built-in utilities, and graphical presentation. The illustrated pamphlet also lists system specifications. Descriptions of the vendor's products and support services complete the brochure.

Asyst Software Technologies Inc, 100 Corporate Woods, Rochester, NY 14623.

Circle No 433

National Semiconductor



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1988 Editorial Calendar and Planning Guide

Issue Date	Recruitment Deadline	EDN Editorial Emphasis	EDN News
Nov. 10	Oct. 20	Programmable Logic Devices, Integrated Circuits, Test & Measurements, Wescon '88 Show Issue	Closing: Oct. 27 Mailing: Nov. 17
Nov. 24	Nov. 3	Microprocessor Technology Directory Graphics, CAE	
Dec. 8	Nov. 16	Product Showcase—Vol. I, Power Sources, Software	Closing: Nov. 21 Mailing: Dec. 15
Dec. 22	Dec. 1	Product Showcase—Vol. II, Computers & Peripherals, Test & Measurement	

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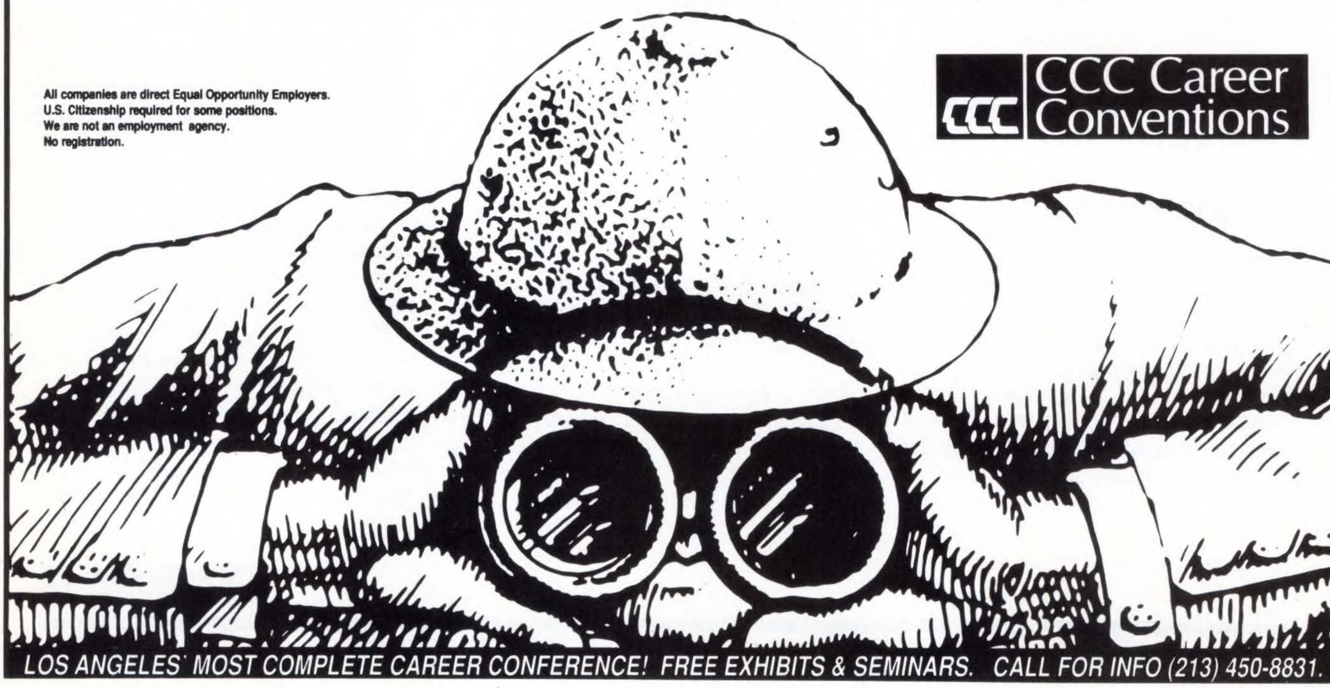

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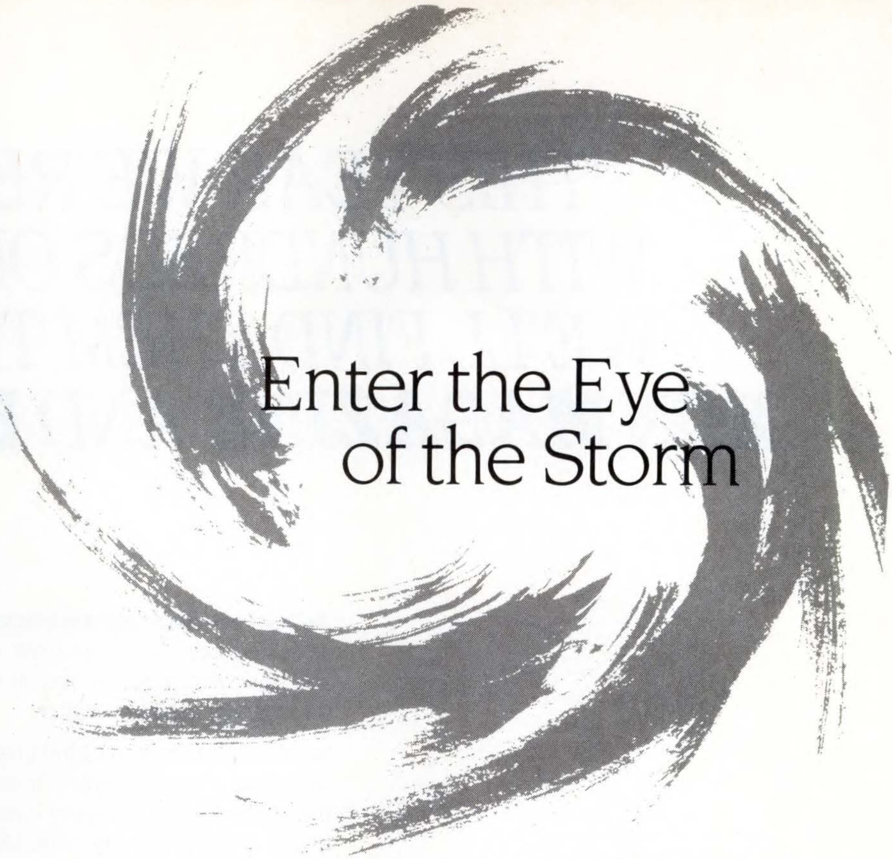

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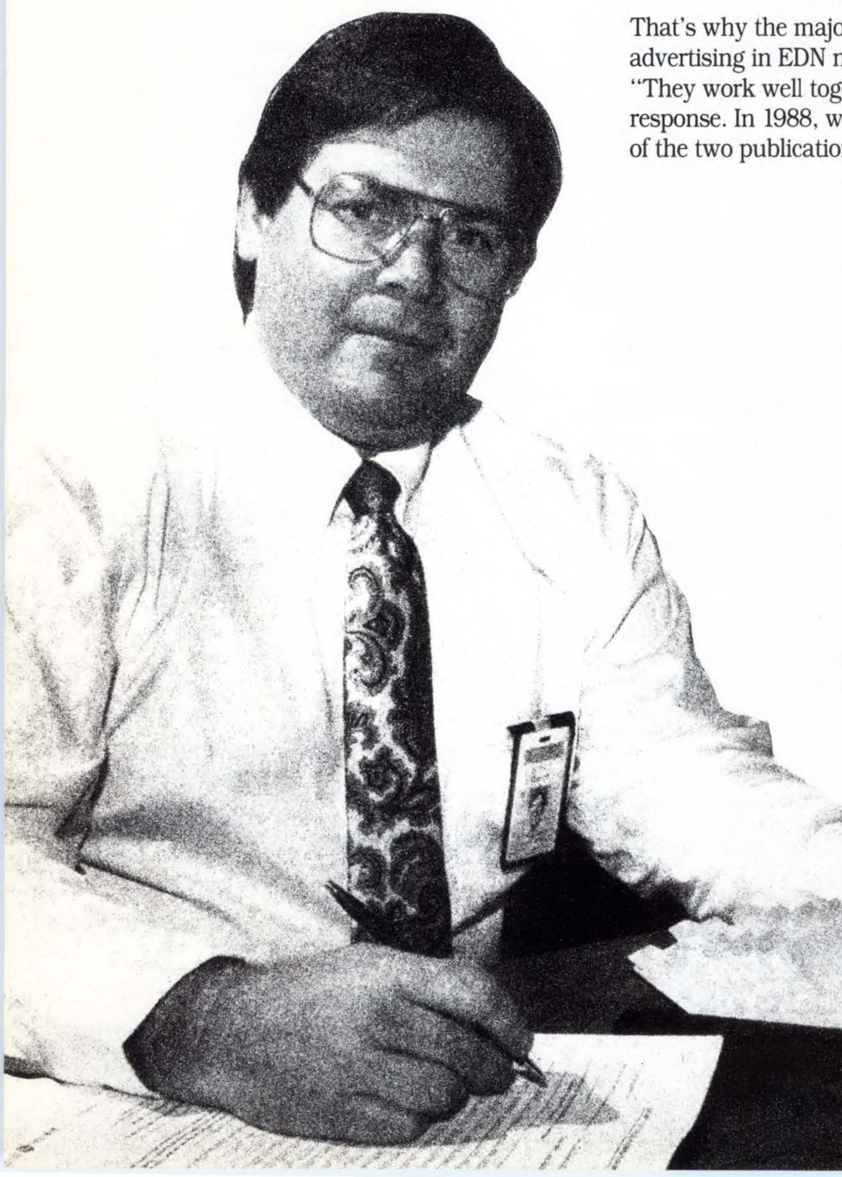

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BUSINESS/CORPORATE STAFF

Peter D Coley
VP/Publisher
Newton, MA 02158
(617) 964-3030; Telex 940573
Ora Dunbar, Assistant/Sales Coordinator

Deborah Virtue
Business Director
Newton, MA 02158
(617) 964-3030

Mark J Holdreith
Advertising Sales Director
Newton, MA 02158
(617) 964-3030
Heather McElkenny, Assistant

NEW ENGLAND
John Bartlett, Regional Manager
Chris Platt, Regional Manager
199 Wells Ave
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Philip J Branon, Regional Manager
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Jim McErlean, Regional Manager
18818 Teller Ave, Suite 170
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(714) 851-9422

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1750 SW Skyline Blvd, Box 6
(503) 297-3382

UNITED KINGDOM/BENELUX
Jan Dawson, Regional Manager
27 Paul St
London EC2A 4JU UK
44 01-628 7030
Telex: 914911; FAX: 01-628 5984

SCANDINAVIA
Stuart Smith
27 Paul St
London EC2A 4JU UK
01-628 7030
Telex: 914911; FAX: 01-628 5984

FRANCE/ITALY/SPAIN
Alasdair Melville
27 Paul St
London EC2A 4JU UK
01-628 7030
Telex: 914911; FAX: 01-628 5984

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Wolfgang Richter
Sudring 53
7240 Horb/Neckar
West Germany
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EASTERN BLOC
Uwe Kretzschmar
27 Paul St
London EC2A 4JU UK
01-628 7030
Telex: 914911; FAX: 01-628 5984

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Mary Beth West
Manager
18818 Teller Ave. Suite 170
Irvine, CA 92715
(213) 826-5815

Maria Cubas, Production Assistant
(201) 228-8608

Wendy A Casella, *Advertising/Contracts Coordinator*
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EDITED BY CYNTHIA B RETTIG

Contamination control crucial for IC manufacturers

To achieve any kind of sustained growth, US semiconductor manufacturers must work closely with semiconductor-equipment and -materials suppliers in addressing and solving the problem of contamination in the the fab area, according to The Information Network (San Francisco, CA). Contamination and particulates in the fab area significantly affect the production yield for semiconductors. What's more, as device dimensions decrease, the issue of particulate contamination grows even more significant.

The researchers recommend the goal of a zero-contaminant environment for US manufacturers. Achieving this goal would require stringent clean-room standards, and managers would have to encourage their employees to be diligent in promoting the cause. Companies should also scrutinize their suppliers. Another problem to be solved is the lack of standards. The Information Network points out that a lack of standard guidelines creates confusion in the industry. Class 10 clean-room air, for example, contains 0.00035 particles larger than 0.2 μm per ml. On the other hand, standard-grade processing chemicals contain 100 to 100,000 particles larger than 1.0 μm per ml. Low-particulate chemicals, which can cost four times more, contain 10 to 500 particles per ml.

The cost of R&D—and of the equipment necessary to properly test and then correct faulty conditions—mandates management involvement. The cost of a Class 1 clean room, for example, entails a substantial commitment: One 15,000-sq-ft clean room with a capacity of 15,000 6-in. wafers per month and located within a 60,000-sq-ft fab building costs $15M—unequipped.

Purification methods must be the best available. Current methods include catalysis, chromagraphy, distillation, electrostatic precipitation, and molecular sieve. And the kind of testing equipment usually found only in the research laboratory should be used in the manufacturing process. Manufacturers should test incoming chemicals and materials on a lot-by-lot basis.

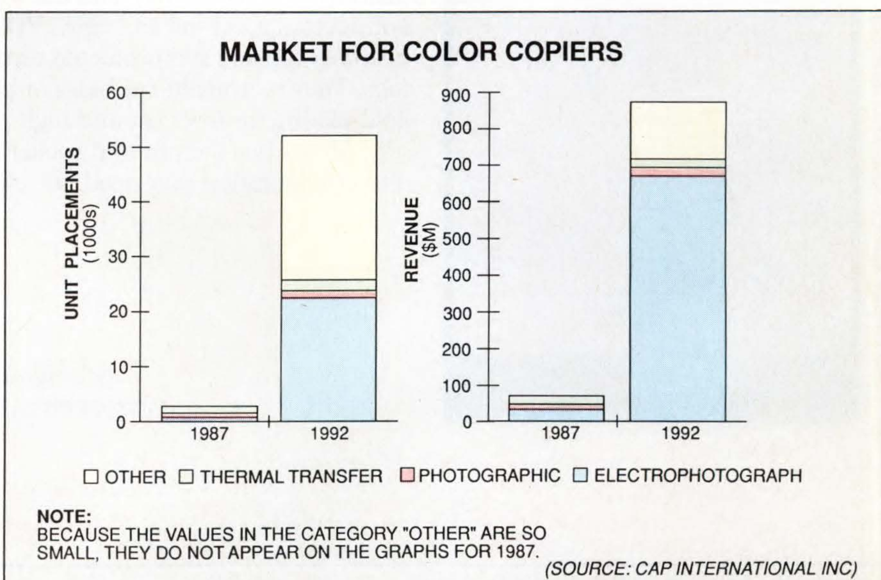
The Information Network recommends that manufacturers benchmark their suppliers. Pricing, for one thing, involves more than the bottom line. To find the best buy, manufacturers should rate the full price-support package, including field support, process support, and supplier stability.

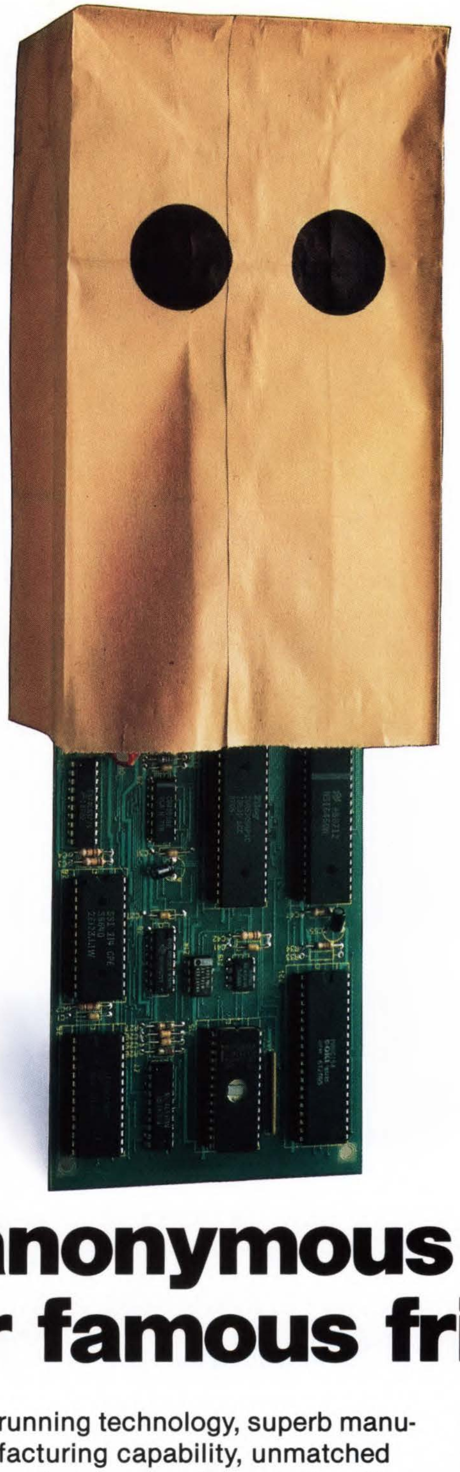
Manufacturers should also consider each supplier's attitude and look at the reputation of the company, its willingness to negotiate, and its repeat-customer base. The benchmarking process should also include checking out how responsive the supplier was to proposed changes during the beta testing of its system, and whether the company has the staff to make its promises of support into a reality.

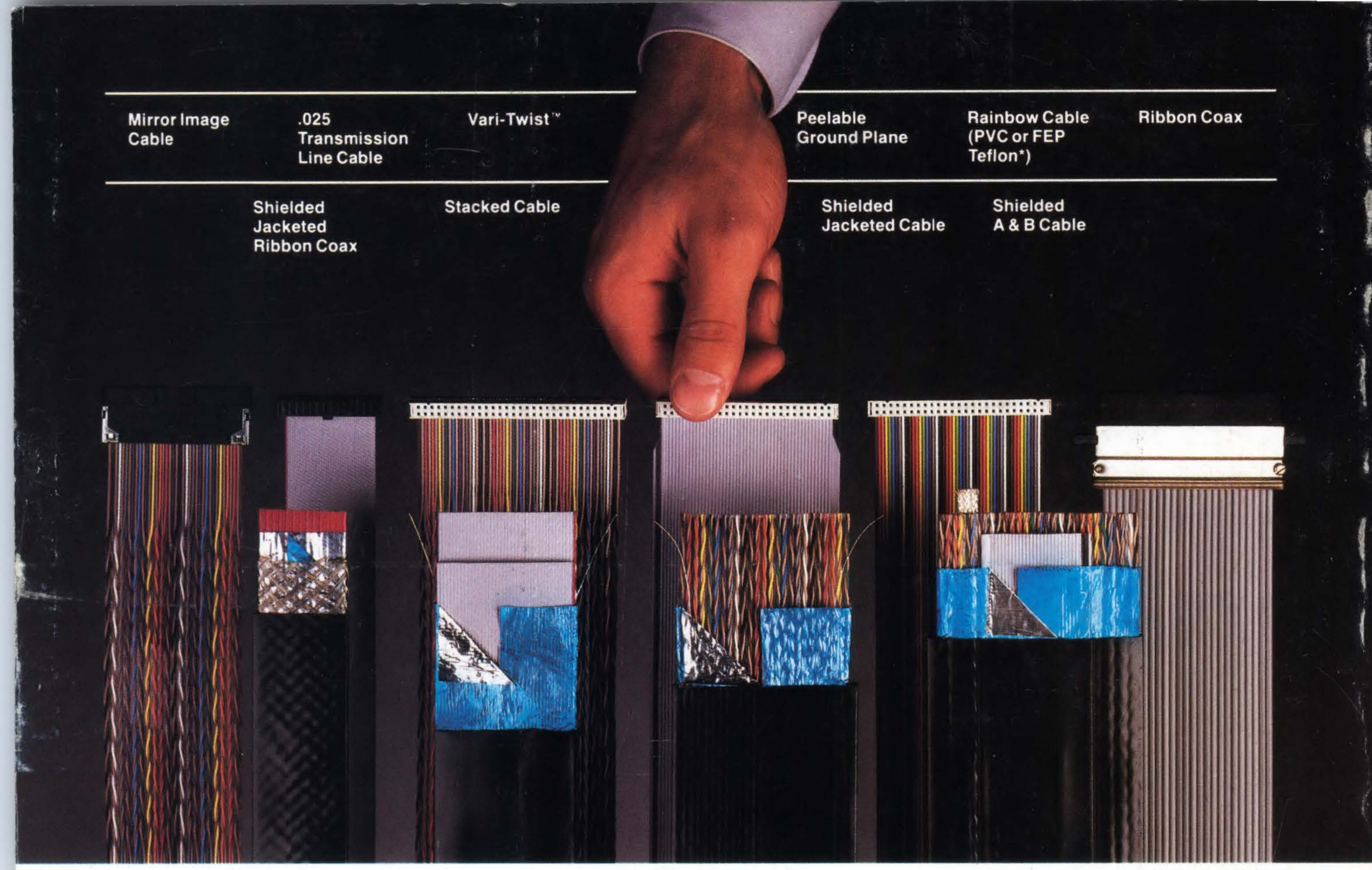
Understanding the sources of contaminants—such as the particulates a machine can generate—is crucial to understanding lower device yields. Finally, in addition to sophisticated monitoring and rigorous calibration methods, a simulation of the production mode for multiple wafer processing is necessary for complete testing and control.

Color-copier market to see $860M in revenues in 1992

As the use of color hard copy increases, so does the need to reproduce multiple copies of color originals. Consequently, within the next few years, full-color copiers will become standard equipment for offices, predicts CAP International Inc (Norwell, MA). It projects that the total color-copier market will reach $860 million by 1992, a dramatic rise from the 1987 figure of $65 million. CAP predicts that electrophotographic copiers will be the fastest-growing segment of the market during the forecast period. More and more electrophotographic color copiers are entering the marketplace with improved speeds and lower prices.







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