SEPTEMBER 1, 1988

# EDN ®

Digital synthesizer eases
testing of complex circuits

SCSI host adapters

Instrumentation amplifiers

Technology Feature:
Parallel processing

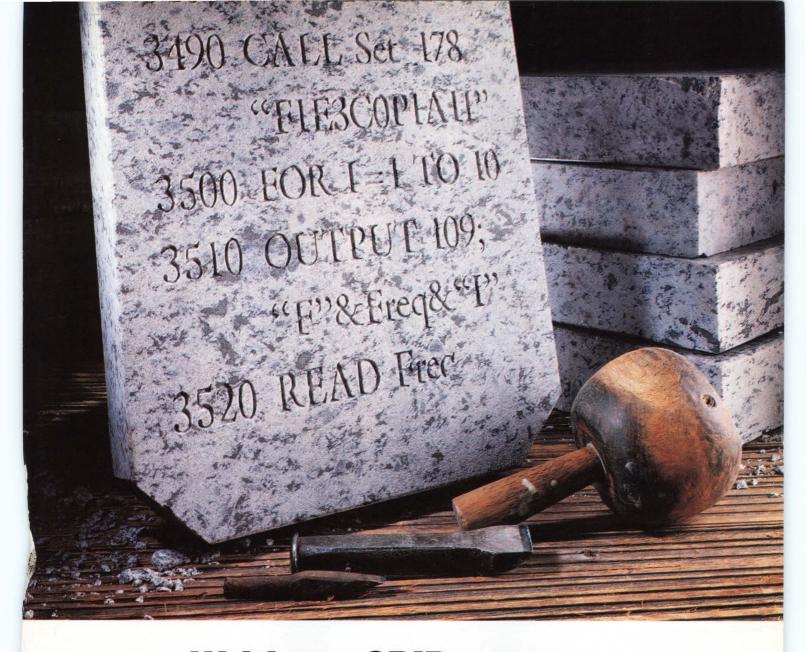## ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

1988
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**1**

# Instruments cross over to the virtual domain

# horns?

For the ultimate in AT-compatible designs, our 286/NEAT™ and 386/AT CHIPSets dominate. They're the result of four years experience building integrated CHIPSets now used in over 5 *million* microcomputers. While other chips hit the wall at 12 MHz, only CHIPSets support a full range of processors and clock speeds.

Why take a chance with partial solutions which might box you in? CHIPSets solve your system-level design problems today. Providing tightly-coupled subsystem solutions for VGA graphics, mass storage and communications, too. And our unique Design Services Organization offers assistance ranging from technical consultation to the design of entire systems.

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**CIRCLE NO 134**

# Or by the

**There's only one thing tougher than getting ahead of the industry standard these days. *Staying* ahead.**

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When it comes to competition
in the compatibles marketplace,
are you going to grab
the bull by the tail?

*On the cover:* It's not a mirage—computer-controlled instruments on a card that connect to industry-standard backplanes are finally materializing. By combining these cards with personal computers or single-board computers, you can create virtual instrumentation. See pg 120. (Photo courtesy National Instruments)

▽BPA ABP Φ

# This meter has what you need most – Superb accuracy and proven reliability

**The Fluke 8840A is your best choice for accuracy, readability and overall performance in a 5½ digit multimeter.**

The Fluke 8840A is the world's best selling 5½ digit DMM. For good reason. Basic dc accuracy is 0.005% at one year. Basic ac accuracy at one year is 0.16%, and one year basic resistance accuracy is 0.013%. With users discovering their 8840A's typically exceeding these specs at each one-year calibration cycle.

The specs are even better for the 8842A. It offers 0.003% basic dc accuracy and 0.08% basic ac accuracy at one year. Resolution is 100 nV on dc readings, and 100 $\mu\Omega$ resolution on resistance readings. Plus a two year calibration cycle and warranty.

Nothing in its class can match the 8840 Series for field-proven reliability: 60,000 hours MTBF for the 8842A, and nearly 70,000 hours for the 8840A.

And nothing can match the 8840 Series for ease of operation. The vacuum fluorescent display is the most readable you've ever seen. True-RMS ac and IEEE-488 interface options let you configure the unit the way you need, so you aren't stuck with features you don't want.

An adjustable tilt-stand for bench use is standard. But rack mounting is quick and trouble free. Closed-case calibration reduces maintenance time. And throughput can be set for 2.5, 20, or 100 readings per second, making the 8840A the fastest in its class.

Put the world's most popular 5½ digit multimeters to work for you today. For your nearest distributor call **1-800-44-FLUKE, ext. 33.**

## FROM THE WORLD LEADER IN DIGITAL MULTIMETERS

| FLUKE 8840A | | FLUKE 8842A | |
|---|---|---|---|
| 0.005% basic dc accuracy (1 Yr.) | | 0.003% basic dc accuracy (1 Yr.) | |
| 0.16% basic ac accuracy (1 Yr.) | | 0.08% basic ac accuracy (1 Yr.) | |
| 0.013% basic ohms accuracy (1 Yr.) | | 0.008% basic ohms accuracy (1 Yr.) | |
| Resolution to 1 $\mu$V, 10 $\mu$A, 1 m$\Omega$ | | Resolution to 100 nV, 1 $\mu$A, 100 $\mu\Omega$ | |
| One year warranty | | Two year warranty | |
| 8840A | $795 | 8842A | $995 |
| 8840A-05K IEEE-488 option | $170 | 8842A-05K IEEE-488 option | $170 |
| 8840A-09K AC True-RMS option | $205 | 8842A-09K AC True-RMS option | $270 |

FLUKE ®

*SCSI **host adapters** open the door to disk-transfer rates of 1M byte/sec and faster (pg 59).*

## EDITORIAL  51

Before committing money to the Superconducting Super Collider project, engineers and scientists should debate its merits.

## NEW PRODUCTS

## LOOKING AHEAD  253

Hardware outpaces software in information technology. . .Growth in UPS market spawns new strategies.

## DEPARTMENTS

A 386 µP.
155 supporting chips.
And no time
to breadboard.

# No one can sol but we solve

Everyone thought gate arrays would be a great solution to their semi-custom design needs. Then they designed one and discovered that "semi-custom" translated into "expensive," "time consuming" and "risky."

PGAs let you spot system problems before they become a real headache. No more risking large sums of money and time to verify your design in hardware. And if you need to change your design you can do it in a matter of minutes. Not months. And you won't have to spend any more money.

### The solution to the solution.
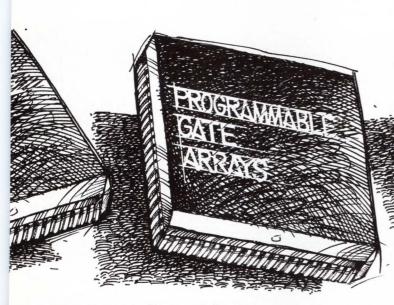
Meet the Logic Cell™ Array— the first Programmable Gate Array. It's a high density CMOS chip of unmatched technology that's user programmable where it's easiest for you to program—in software.

Your development cycle is cut to a week or two instead of six months. So you can get your product to market that much sooner.

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The Am2000 series has densities from 1000 to 2000 usable gates and the Am3000 series has densities from 2000 to 9000 usable gates. With those densities (we'll have even higher densities later), you need fewer parts to get the same functions as

# ve the problem, d the solution.

EPLDs or discrete logic.

There is no other PGA technology available today. And over 5000 designers are already using it.

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Your investment is minimal. You don't have to finance months of NRE. You can get started for the price of a PC (which you probably already have) and some software.

PGAs are the epitome of the just-in-time product. They are the only gate arrays stocked in production quantities at your distributor. And they're programmable instantly. Which means you can go from design to production as fast as you need to.

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Contact us for a free diskette that gives you a detailed product overview, an interactive session where you can plug in your own design criteria and find out how PGAs can help your design. Part of the PGA development software is included so you can get started saving time and money right away.
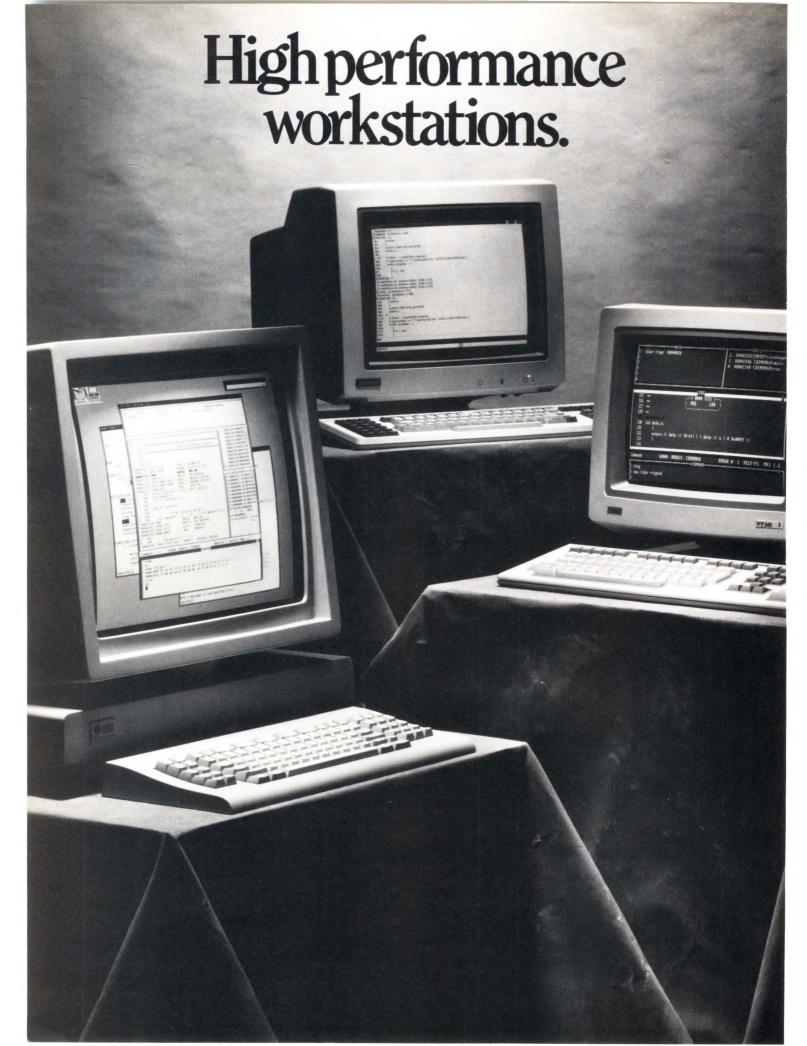
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## Advanced Micro Devices ↗

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# The highest performance development tools.



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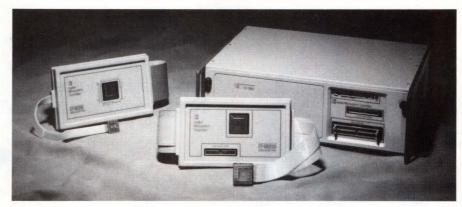
Now you can build a high performance development environment around the engineering workstation you already own. And get your embedded microprocessor designs completed more quickly and with less effort than ever before.

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in a closely coupled development environment. What's more, VALI-DATE is supported by a rich library of linkers, loaders, compilers and assemblers.

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| Operating Environment | | Microprocessors/ | Software Utilities | | Emulation Link | Debuggers |
|---|---|---|---|---|---|---|
| Host | Operating System | Microcontrollers | Languages | Tools | | |
| VAX | VMS | **Intel:** | **C** | Compilers | **ES 1800** | **VALIDATE** |
| MicroVAX | ULTRIX | 8048 family, 8051 family | **Pascal** | Assemblers | (16 & 32-bit) | and other soft- |
| Apollo | UNIX® | 8080, 8085, 8086/8, | **FORTRAN** | Linkers | **EC 7000** | ware products |
| Sun | MS-DOS | 80186/188 and 80286 | **PL/M** | Locators | (8-bit | for source |
| PC | | **Motorola:** | **Assembler** | | microcontrollers) | and symbolic |
| PC XT | | 68HC11, 6800/2/8, | **Jovial** | | **EM Series and** | debugging |
| PC AT | | 6809/9E, 68000/08/10 | **ADA (VERDIX)** | | **EL 800** | |
| PC Compatibles | | and 68020 | | | (8-bit | |
| | | **Zilog:** | | | microprocessors) | |
| | | Z80, Z80H, MK 3880/4 | | | | |
| | | and Z8001/2 | | | | |
| | | **NSC:** NSC 800 | | | | |
| | | **Hitachi:** 64180 | | | | |

*We offer debug and development tools with a difference: they are integrated solutions for virtually any development environment.*

## Source or symbolic debugging for Intel, Motorola, and Zilog. Plus the best emulation.

The VALIDATE family of source and symbolic debuggers and host control software has been specifically tailored by Applied Microsystems to work with our emulators

1800 Series of 16-bit and 32-bit emulators, and you have the most powerful emulation system anywhere. The high speed SCSI interface option lets you upload and download files more than twenty times faster than with RS 232. Our Advanced Event Monitor System lets you precisely control emulation with logical statements of system conditions. The ES 1800 also gives

# Applied Microsystems Corporation

**CIRCLE NO 124**

"Listen, the future of this product line is riding on my next design automation decision. Not to mention my job."

"I hear you. So tell me more and let's figure out how HP can help you make some of those decisions."

"Well, first, we're feeling enormous pressure to get products out faster. The key is designs that'll go through manufacturing the first time. If we're going to stay competitive, we've got to tackle the overall product development process—and it starts right here in design."

Look, HP's gone through the same thing. Our own divisions deal with the same problem daily. We came up with a solution called DesignCenter. It combines our electronic design automation tools with the rest of the process to produce a high degree of manufacturability right from the start—in design."

"That's exactly what we need. A single data path from design right on through production and out the door. If we could somehow combine electronic design with microprocessor development and mechanical engineering and tie it into manufacturing and test, we'd be a lot happier. Are you saying HP can do that for us now?"

"We're not there 100% yet. Nobody is. But that's the whole idea behind our DesignCenter. Right now, we've got the broadest set of EDA tools there is. Match them up with the HP test and measurement tools you've used for years, and you'll be way ahead of the game."

"We've always counted on HP test equipment. But how does that relate to your EDA tools?"

"We were able to bridge the gap between design and prototype test. Now you can create higher quality tests—faster, too—by transferring data directly between our logic analyzers and simulation. And the design and layout tie directly into HP board test systems."

"That's terrific. But testing is only one part of the process. We're making decisions on everything from ASICs and PLDs to microwave hybrids to multi-layer PCBs. And they all have different parts and technologies. I'll tell you, it's impossible to keep up."

"We agree, it's a big problem. But that's the reason we have digital, analog, and microwave CAE tools for design, simulation, and layout. We even support it all with information management to handle the tough tradeoffs your team has to make in choosing between all the technologies and complex interactions."

"There's one thing that's always a concern. We've got systems in here from some of your competitors. If we go with HP, can you fit into our existing environment?"

"Absolutely. Using either off-the-shelf or customized interfaces, we'll help you integrate HP tools into your existing systems. And, since HP supports EDIF and IGES standards, you'll have the flexibility you need down the road."

"Speaking of standards, tell me about your platforms."

"Well, HP is among the industry leaders in standardization because the marketplace is demanding it. Our family of workstations and servers supports UNIX and networking standards. They thrive in a multi-vendor environment, making it easier to get your job done right the first time. That's the bottom line these days."

"I get the feeling you understand that we're interested in a lot more than just tools. I mean, you seem to be talking about more than hardware and software."

"I am. HP is totally committed to this idea of getting more correct-by-design products through your plant. We *are* talking about a lot more than the tools. We'll sit down with you and help create a system that meets your needs...not ours or somebody else's. And I mean we'll get right down to solving problems and training your people. That's what we do better than anyone else."

"I want to keep talking about this whole thing. And I want to include some other engineers, too. What are you doing next Wednesday?"

"I've got a feeling I'll be back here."
"Right."

"Name a time."

*The dialogue continues...*

More and more project managers are talking to HP about EDA tools and DesignCenter. Start a dialogue today. Call toll free. Ask for information on HP Electronic Design Automation and bridging the gap from design to prototype test: 1-800-752-0900, **Ext.** C215.

*we never stop asking* "What if..."

**CIRCLE NO 123**

**HEWLETT PACKARD**

# This chip enabled us to process signals of the past.

**The Rosetta Stone**, discovered in 1799, was the key to deciphering the hiero-glyphics that had been incom-prehensible for centuries.

Signal processing, when you come right down to it, is multiplication, addition, subtraction and storage. Doesn't sound very exciting.

But put together a set of building blocks that do those simple operations with almost unimaginable digital speed and precision. Then add A/D converters that bring in information from the world around you. Plus D/A converters that restore the digitally processed signals to a form your senses can understand.

And you've built a signal processing system that will enable you to do things that couldn't be done before, see things that couldn't be seen before and understand things that could never be understood before.

*That's* exciting. And we can help make it happen.

## Complete systems solutions.

Our approach to signal processing is simple.

We've taken our unparalleled experience in data conversion and added to it a set of signal processing chips that perform operations that used to require entire circuit boards.

Here's a sample of what they can do for you:

*ISP 9110 12-Bit Microprogram Sequencer:* expanded 33 word stack, 50 ns minimum cycle time.

*ISP 9119 FIFO RAM Controller:* uses standard RAMs to build FIFOs up to 64K deep, 15 MHz operation.

*ISP 9128 FIR Filter Controller:* implements 16-bit filters to 128 Taps, 128 Tap sampling rate of 100kHz.

*ISP 9210 16x16 Multiplier Accumulator:* innovative high-speed architecture (65 ns commercial, 75 ns military), low-power operation.

*ISP 9216 16x16 Multiplier:* low-power, industry-standard compatible to AM29516 and MPY016.

*ISP 9520/21 Pipeline Register:* high-speed access,

# These are the chips you need to process signals of the future.

**Our DSP building blocks,** combined with our data conversion know-how, will help you design systems that depict reality more clearly than ever before possible.

output selectable from any resistor.

With devices like these, we can give you a total integrated signal processing solution. Plus the added benefits of single-vendor support and package pricing.

## Position yourself for the future.

Signal processing is changing every day.

That's why you need more than a signal processing supplier who has a few good parts.

You need a long-term partner who has a commitment to signal processing, and the resources in every area that signal processing calls upon.

For example, the chips of tomorrow will very likely combine signal processing, data conversion and high-speed logic. When you work with us, you'll get our Intersil expertise in processing and conversion. Plus our RCA Advanced CMOS Logic capabilities. Plus the more than 20 years of GE

experience in radar, sonar, medical imaging and other demanding DSP applications.

If worries about complexity and cost have deterred you from taking the exciting step into digital signal processing, call us. Together, we'll step into the future.

For more information, contact your local GE Solid State sales office or distributor. Or call toll-free, 800-443-7364, extension 30.
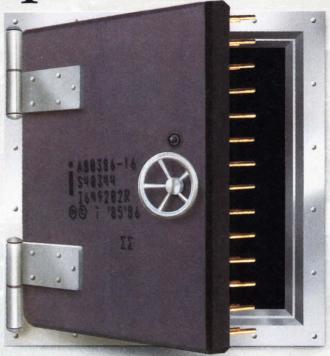
In Europe, call: Brussels, (02)246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.

General Electric Company, U.S.A.

## GE Solid State

# How to crack 386 protected mode.

Unlock selectors and descriptor tables. Break open task state segments (TSS) and call gates. Microtek's In-Circuit-Emulator (MICE) cracks 80386 protected mode with real-time, non-intrusive emulation to 20 MHz.

MICE unravels all the intricacies of the 80386, so you harness its full potential. Internal registers, including GDT and IDT base values are all directly accessible. And MICE also provides decoded access to all selector and descriptor bits, like privilege level, segment type and page accessed bits.

Use MICE as a stand-alone device, or integrate it into your development environment. MICE easily interfaces with the IBM® PC/XT/AT, VAX® Apollo® and Sun® computers.

And the 80386 emulation system is just one of our many embedded software development tools.

Our Software Analysis Workstation (SAW) delivers hardware-based, real-time software analysis in a source code environment. For source code development, our Microtec® Research products provide you with C and Pascal cross-compilers, cross-assemblers and debuggers for many popular microprocessors.

And MicroCASE™ backs all of its products with solid applications support, both at the local and factory level.

Microtek enjoys a long track record of being first to market with quality support for many major microprocessors. We were the first alternative for 80386 emulation. We're first to provide non-proprietary support for 80386 protected mode.* And you can count on the same support in the future.

**For more information and product literature on our full line of MICE, call us at (408) 253-5933.**

Crack 80386 protected mode, and open the door to exciting design possibilities—with the best 80386 emulation system now available. From MicroCASE.

## Micro CASE

Formerly Northwest Instrument Systems, Inc.

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*Without the use of a proprietary "bond-out" chip.

IBM is a registered trademark of International Business Machines. VAX is a trademark of Digital Equipment Corporation. Apollo is a trademark of Apollo Computer, Inc. Sun is a trademark of Sun Micro Systems.

Processors supported by Microtek: 80386, 80286, 80186, 80188, 8086, 8088, 68020, 68010, 68008, 68000, 6809, 6809E, 6502, Z80, NSC800, 8085, 8032, 8051, 8031, 8344, 8048, 8049, 8050, Z8, SUPER 8, 68HC11, 64180, 80515.

Circle No. 128 for demonstration

Circle No. 129 for literature

# NEWS BREAKS

EDITED BY JOANNE CLAY

## WORM DRIVE DELIVERS WINCHESTER-LIKE PERFORMANCE

The APX-4000 Series 5¼-in. WORM (write-once, read-mostly) optical disk drives from Maximum Storage Inc (Colorado Springs, CO, (719) 531-6888) store 488M bytes of data on double-sided media and achieve an effective access time of 28 msec. The manufacturer arrived at this access-time spec by pitting its WORM-drive subsystem against Winchester hard-disk subsystems in speed tests that transferred large files. In these tests, the APX-4000 achieved overall transfer rates similar to those of hard disks that had an average access-time rating of 28 msec.

The company is initially offering APX-4000-based WORM-disk subsystems for the IBM PC. The APX-4100, an internally mounted subsystem, costs $4250; the APX-4200, a version for external use that adds a power supply and cabinet, costs $4450. Each subsystem includes a controller card that adapts the PC's bus to the WORM drive's modified ESDI interface, cables, and software. Instead of merely providing hardware-driver software, the company's Maxsys software package implements a complete hierarchical file manager. The company plans to port this same file manager to other operating systems, starting with Unix. This approach allows any operating system to read files written by other operating systems.—Steven H Leibson

## SOFTWARE ALLOWS PROCESS-INDEPENDENT ASIC DESIGN

The Avid (ASIC vendor-independent designer) software package from Mentor Graphics (Beaverton, OR, (503) 626-7000) allows you to proceed through the early stages of an ASIC design before selecting your ASIC vendor. You can develop a schematic and functionally simulate the design before selecting the process. After functional simulation, you'll need to choose the ASIC process to perform an accurate timing simulation. Using Avid also means you won't have to spend time learning the process-dependent constraints of each ASIC process. Avid translates your design into a format compatible with the ASIC processes you select. Companies that have formally committed to supporting Avid include Fujitsu, GE Solid State, Gould, Intel, and Toshiba. Avid is available this month; a site license costs $27,500.—Doug Conner

## C-LANGUAGE LIBRARY AVAILABLE FOR NEURAL NETWORKS

A C-language library of neural-network software from Olmsted & Watkins (Escondido, CA, (619) 746-2765) lets you develop your own neural-network application programs. The software runs on an IBM PC, PC/XT, PC/AT or compatible computer with Microsoft C 5.0 or higher. Priced at $349, the application package supports the following network topologies: back propagation (with any number of layers), adaptive resonance, brain-state-in-a-box, Hopfield, adaptive BAM (bidirectional associative memory), and the Boltzmann machine. A networks package priced at $849 provides the source code for all networks in the applications package, allowing you to modify or create custom networks.—Doug Conner

## ELECTROMECHANICAL RELAYS SWITCH HIGH VOLTAGE AND CURRENT

You can switch at least 270V dc at 10A with the KP2A series of electromechanical vacuum relays from Kilovac (Santa Barbara, CA, (805) 684-4560). Because the contact elements are enlosed in a vacuum, there's no air in the gap to ionize and allow arcing. (This lack of arcing is important in military applications that require no EMI radiation.) The gap between the contacts is smaller than in a relay that's open to the air, so it results in a smaller actuating coil and overall package outline: The KP2A

# NEWS BREAKS

measures 2.63 × 1.74 × 1.81 in. Note that a semiconductor switch may have a smaller package outline, but the heat sink it requires gives the semiconductor relay a considerably larger overall size. The KP2A costs $125 (OEM qty).—Margery S Conner

## NEURAL-NETWORK SIMULATOR SOFTWARE TEACHES CONCEPTS

For those who've always wanted to investigate the AI concepts of neural networks, but didn't know where to start, NeuralWare Inc (Sewickley, PA, (412) 741-5959) offers the NeuralWorks Explorer. This $199 program runs on IBM PC-compatible computers equipped with a hard-disk drive and at least 512k bytes of RAM. Developed with the novice user in mind, this neural-network simulation program provides 13 network paradigms and comes with more than 580 pages of indexed documentation.—J D Mosley

## C COMPILER GENERATES PROGRAMS FOR CONCURRENT DOS

Containing functions that take advantage of Concurrent DOS's multitasking capability, the Lattice C Compiler (Lombard, IL, (312) 916-1600) generates native-mode programs so that your applications won't require PC-mode emulation when running under the Concurrent DOS operating system. Although this compiler contains all the functionality of the manufacturer's previous version, its new features include library functions for file passwords and file sharing, alternate end-of-file treatment, multisector I/O, and shared peripherals. The compiler also offers you the option of generating code that multiple copies of a program can share when running simultaneously; this method reduces memory requirements. The compiler lists for $500 and comes with a disassembler, sample programs, and documentation.
—J D Mosley

## ASIC TESTER USES SCAN-PATH TECHNIQUES
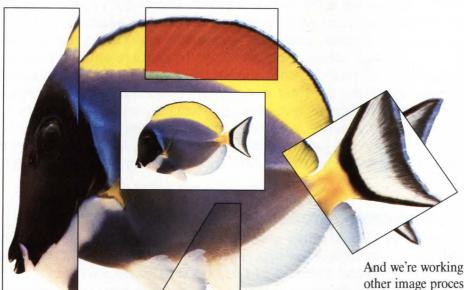
The DV-6005 design verifier from Gillytron (San Jose, CA, (408) 435-3043) allows designers to test products that were designed for scan-based testing. The basic unit offers logic testing, dc parametric testing, and an ac ring frequency test for measuring propagation delays. The unit has a modular design that's expandable to allow for the testing of pc boards and entire systems with scan-based techniques. The unit operates under menu-driven software. It lets you use a proprietary language based on C to generate test programs. The basic unit costs $125,000 and is available within 60 days ARO.—Richard A Quinnell

## FIFO DEVICES OFFER PARALLEL/SERIAL CONVERSION

Four FIFO devices from Integrated Device Technology (Santa Clara, CA, (408) 727-6116) are simplifying data buffering for high-speed serial applications. The IDT72131/72141 devices have 2048 × 9/4096 × 9-bit organization with parallel input and serial output. The IDT72132/72142 devices offer serial input and parallel output. You can connect the devices to handle serial word lengths of 7, 8, 9, 16, 17, 18, and 32 bits, and you can expand their depth without using external components.

All four devices feature a 35-nsec parallel-access time and a 50-MHz serial shift rate. They feature zero fall-through time and provide five status flags: full, almost-full (7/8), half-full, almost-empty (1/8), and empty. The devices are available in 28-pin ceramic or plastic DIPs, 32-pin LCCs, and 32-lead PLCCs. Prices start at $65 for the 72131/72132 and $95 (100) for the 72141/72142.—Richard A Quinnell

# NEWS BREAKS: INTERNATIONAL

## WINDOWS LET YOU TRACE PROGRAMS AT ALL SOFTWARE LEVELS

In conjunction with the company's PC-based in-circuit emulators, the ViewFinder and PathFinder software packages from Ashling Microsystems Ltd (Limerick, Ireland, TLX 70357) provide a windows environment in which you can simultaneously trace programs at both the assembler and the source-code level. ViewFinder is supplied free of charge when you purchase one of the company's development systems. Owners of existing systems can obtain the package as a $275 upgrade. ViewFinder allows you to display standard or user-defined screen windows containing trace information. You can also establish virtual windows; although they're not displayed, the virtual windows are continuously updated as you trace through a program, and they can be brought onto the screen as required. In addition, you can control the emulator's operation from the windows environment. By adding the PathFinder software package (which sells for between $1250 and $1500) and a suitable compiler, you can trace program activity at all software levels. For example, you can display the high-level-language source code that relates to a real-time program trace, so you can compare intended and actual program flow. To capture elusive program bugs, PathFinder allows you to perform continuous trace-and-compare operations, automatically storing any errors for later examination. PathFinder is currently available for use with a PL/M-51 compiler, but versions that run with C compilers for 8051, 68HC11, Z80, and 64180 μPs are scheduled for release between now and the first quarter of 1989. As part of a joint marketing agreement, ViewFinder and PathFinder will be available in the US from Microcosm Inc (Beaverton, OR, (503) 626-6100). —Peter Harold

## PERSONAL VOICE-INPUT WORD PROCESSOR IS JAPAN'S FIRST

The first Japanese personal word processor with voice-input capability hails from Sharp Corp, which plans to sell the system for ¥400,000 to ¥500,000 (around $3000 to $3900)—far less than the $18,500 to $23,000 that users shell out for Sharp's and NEC's current business voice-input systems. The company plans to release the personal voice-input system in early 1989. The system is speaker-dependent, but takes only about 10 minutes to register the user's voice. It accepts complete sentences as well as individual words, and it generates mixed kanji and kana text. Users can make corrections on a keyboard. Including the time needed for manual corrections, the system can produce 40 wpm.—Joanne Clay

## SOLID-STATE LASER USES LASER DIODE AS EXCITATION SOURCE

A solid-state laser device from Asahi Glass Co uses a laser diode instead of the conventional electrical-discharge lamp as the excitation light source, according to reports in the Japanese press. Using a laser diode as the excitation light source makes the laser system much smaller than its predecessor, which used the electrical-discharge lamp. The new system is $1/20$ of its former length and $1/1600$ of its former volume. The yttrium aluminum garnet laser absorbs almost 100% of the excited light. The company increased the laser's conversion efficiency to light from 1% to 15.5%, which greatly reduced the heat produced by the system. When they're used as excitation light sources, semiconductor lasers often exhibit poor spectral purity and the inability to achieve high peaks in Q-switch operation. Asahi employed a proprietary optical monocrystalline technology to solve these problems in the solid-state laser system. Applications for the solid-state laser include optical measuring systems and optical communication systems. Including the power source, the laser system costs ¥1,000,000 (about $7700).—Joanne Clay

EDN September 1, 1988                                                                25

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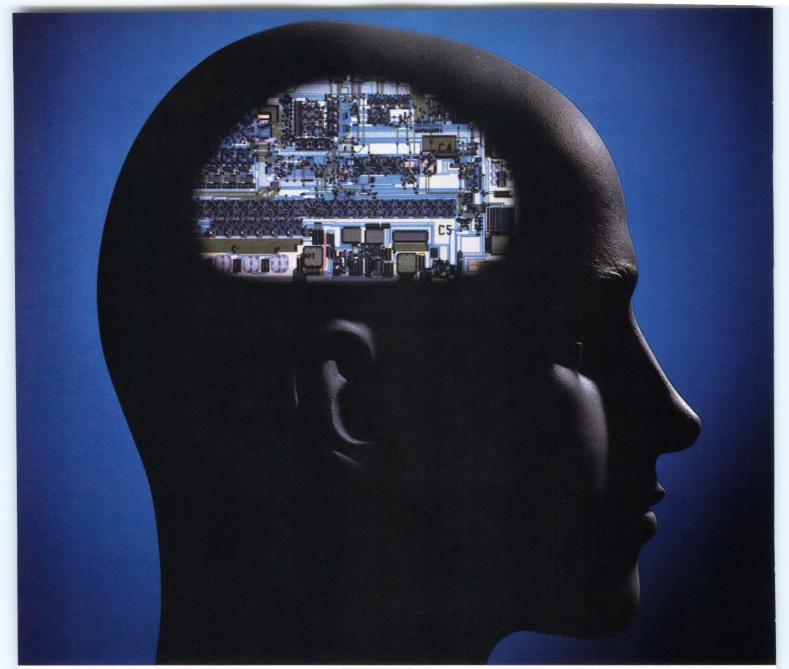
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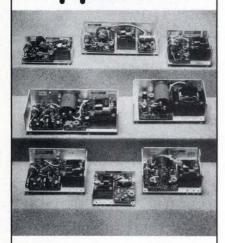
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# SIGNALS & NOISE

### Thermocouple misconceptions are common

Jim Williams's fine article "Clever techniques improve thermocouple measurements" (EDN, May 26, 1988, pg 145) is sadly flawed by a basic misunderstanding of the physics of thermocouples. It is a common misconception that the voltage of a thermocouple is generated across the junction. This is simply not true. The voltage is generated along the wires and is driven by the temperature difference between the sensing junction and the reference ("cold") junction. For a given temperature difference, the two dissimilar wires generate unequal voltages. The voltage appearing across the thermocouple circuit at the reference junction is the difference between these unequal voltages.

The more technical explanation is that for a given temperature gradient $dT/dx$, an electric field $dV/dx$ is generated. This electric field is a function of both $dT/dx$ and absolute temperature. The local value of the difference $dV/dT$ for a given alloy pair at a particular temperature is called the Seebeck coefficient. If the integral of the Seebeck coefficient is evaluated between the sensing junction and the reference junction, the thermoelectric voltage results.

Thermal voltages in thermocouple circuits are always the result of thermal gradients. If a section of a thermocouple circuit has an unknown or undesirable Seebeck coefficient, then its influence can be diminished by suppressing thermal gradients in that section. For example, when you make a connection in a thermocouple circuit, it's best to thermally anchor each of the wires to a common temperature before they reach the electrical connection point. The connection point should also be thermally anchored to this temperature. This procedure tends to suppress thermal gradients across the oxides, unknown alloys, etc, that make up the connection. If the thermal gradients are suppressed, spurious thermal voltages will be reduced.

I hope this explanation will help clear up some of the misconceptions about the physics of thermocouples. Jim Williams is not alone in his misunderstanding—I have seen a remarkably similar treatment of thermocouples in a high-school physics text that is currently being used by the Denver School Dept.
*Bill Dubé*
*Mechanical Engineer*
*Denver, CO*

### Jim Williams responds:

Some friends and I have reviewed Bill Dubé's comments and found them to be quite correct. As such, I find myself corrected, educated, and apologizing for any confusion I may have caused EDN's readers. Although Bill's distinctions are subtle, they are still the more correct interpretation, and I appreciate his remarks.

### Circuits cannot live by breadboarding alone

I must take issue with the impression created by both Jim Williams's guest editorial "Should Ohm's law be repealed?" (EDN, March 3, 1988, pg 47) and Forrest M Mims III's supporting letter "CAD systems can't replace breadboards" (EDN, May 12, 1988, pg 32). Both Williams and Mims seem to long for a return to pre-CAE days.

Analog-circuit simulation must be used in conjunction with breadboarding. Neither is sufficient on its own. How many times has an engineering breadboard functioned correctly, meeting all performance specifications (even over temperature), and then a team of engineers has had to "live" in the assembly line because the first production boards couldn't be built? CAE is simply the only viable method we have of performing worst-case, tolerance, and stability analysis in an economic and timely fashion. Sometimes the

# SIGNALS & NOISE

worst possible scenario is the one in which the breadboard works!

An analog engineer must be capable of using all the tools available in a balanced and thoughtful way. Only the judicious use of CAE together with physical breadboarding will result in robust, produceable circuits.

*Philip E Teicher*
*Vice President of Engineering*
*MICRA Corp*
*Hauppauge, NY*

(Ed Note: Jim Williams's editorial clearly stresses the use of breadboards and CAE tools instead of blind reliance on CAE tools alone.)

## Sorry, this one's taken

I'd like to inform you of the inadvertent use of our registered trademark within a listing for another company's product in EDN's New Products section (May 26, 1988, pg 257). The paragraph used the phrase "C Executive" to describe a part of Microware Systems Corp's C compiler control program that calls each successive phase of the compiler. In fact, "C EXECUTIVE" is a registered trademark for our real-time, multitasking operating-system kernel, which currently runs on 15 architectures, including everything from the 8080 to the Clipper. It has frequently been mentioned in the New Products section of EDN and in other trade magazines.

*Edward J Rathje*
*Vice President*
*JMI Software Consultants Inc*
*Spring House, PA*
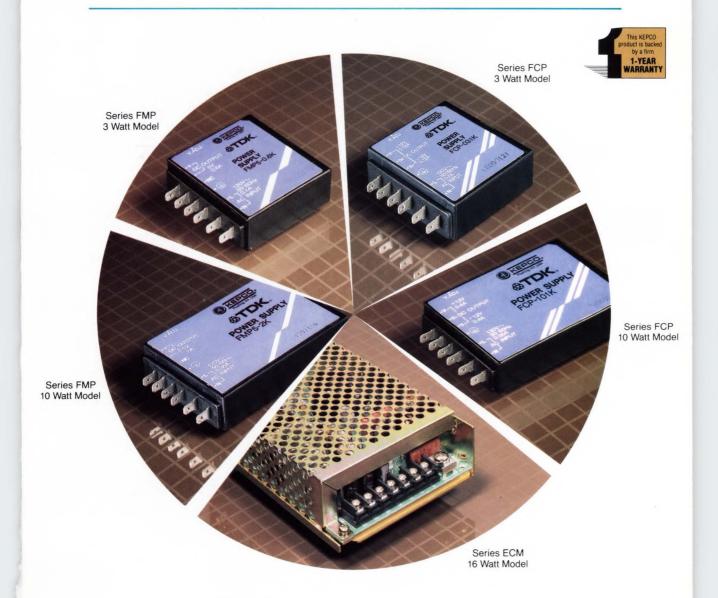
## WRITE IN

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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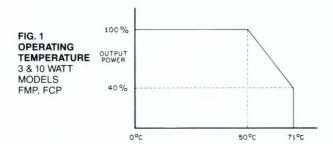
## SERIES FMP, FCP, ECM POWER SUPPLIES

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Series FCP
3 Watt Model

Series FMP
3 Watt Model

Series FMP
10 Watt Model

Series FCP
10 Watt Model

Series ECM
16 Watt Model

## INPUT CHARACTERISTICS
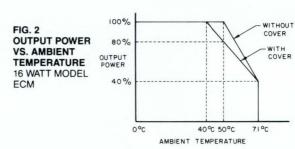
| Specification | Condition | FMP, FCP | ECM |
|---|---|---|---|
| Voltage | | 85-132V a-c, 110-170V d-c | |
| Current (rms typ) | At 120V a-c | 3W: 0.08A<br>10W: 0.25A | 0.5A |
| | At 85V a-c | 3W: 0.1A<br>10W: 0.35A | 0.6A |
| Fuse value | | External 125V fuse recom.<br>3W:<br>0.16A ~ 1.6A<br>10W:<br>1A ~ 8A | Internal fuse, wire lead 125V, 2A |
| Frequency | | 47-440Hz | |
| Switching frequency | | 80 ~ 300KHz (depending on load) | 35 ~ 185KHz (depending on load) |
| Brownout voltage | Low operating limit | 80V a-c/105V d-c | |
| Initial turn-on surge, first ½-cycle | 120V a-c, rated load 25°C cold start | 16A max | 20A max |
| EMI | Conducted | FCC Class B | |
| Leakage current | At 25°C, (UL method) | 0.5mA rms max | |
| Startup time | 25°C, nom input, max load | 100msec | 50msec<br>to reach 90% nom. |
| Holdup time | 25°C, nom. input, max load | 20msec min | |
| Circuit type | | FMP: flyback<br>FCP: Output #1 flyback<br>Output #2: flyback plus linear post regulators | Output #1: flyback<br>Outputs #2 & #3: flyback plus linear post regulators |

## GENERAL SPECIFICATIONS

| Specification | Condition | FMP, FCP | ECM |
|---|---|---|---|
| Temperature | Operating | 0-50°C; See Fig. 1 | 0-40°C See Fig. 2 |
| | Storage | −40°C to 85°C | |
| Humidity | Operating & storage | 95% RH non-condensing | |
| Shock | non-operating | 20 g peak, ½ sine pulse, 3 shocks each axis ± 5 msec duration | |
| Vibration | non-operating | 5–10Hz: 10mm amplitude 10–55Hz: 2g acceleration each axis | |
| Isolation | Output to ground | 500V d-c, 100MΩ, 1 min | |
| Dielectric strength | Input/ output to gnd | 2KV a-c, 1 min | |
| Dimensions | inch: | 3W: 2.17 x 1.97 x 0.75<br>10W: 2.17 x 3.15 x 0.75 | 3.6 x 4.72 x 1.28 |
| | mm: | 3W: 55 x 50 x 19<br>10W: 55 x 80 x 19 | 91.5 x 120 x 32.5 |
| Weight | ounces/ grams | 3W: 2.82/80<br>10W: 3.53/100 | 13/370 |
| Mounting (see dwg) | | 2 blind–threaded brass inserts 4–40 | 2 surfaces; 4–40 thread |
| Max screw penetration | inches/mm | 0.24/6 | |
| Connectors | | AMP Faston series 187 or equivalent | Barrier strip (M3; gnd M4) |
| Safety | | UL 478 recognized CSA 1402 certified | |
| Package material | | Plastic UL 94V-1 or 94V-0 | Chassis: 1mm Cover: 0.5mm steel, zinc plated, yellow chromate wash. |
| Type of construction | | Unencapsulated, repairable | Printed circuit cards, enclosed |

## OUTPUT CHARACTERISTICS

| Specification | Source effect | | Load effect | | Temperature effect | | Combined effect | | Time effect | Recovery characteristics (50 to 100% load change) | | Overvoltage protection |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Condition | min–max input | | 10–100% load | | 0–50°C | | Source, load, & temp. | | ½ hr–8hr max | Excursion | Recovery to within ± 1% | |
| | typ | max | typ | max | typ | max | typ | max | | | | |
| FMP, FCP | 0.1% | 0.5% | 0.8% | 2.0% | 1.0% | 3.0% | ± 1.0% | ± 3.0% | 0.5% | < ± 4% | <1msec | zener diode |
| ECM Output #1 | 0.5% | 1.5% | 1.0% | 3.0% | 1.5% | 3.5% | ± 2.0% | ± 4.0% | 0.5% | < ± 4% | <2msec | NA |
| Outputs #2 & #3 | 0.5% | 1.5% | 0.5% | 1.5% | 1.0% | 3.0% | ± 1.5% | ± 4.0% | | | | |



**FIG. 1 OPERATING TEMPERATURE 3 & 10 WATT MODELS FMP, FCP**



**FIG. 2 OUTPUT POWER VS. AMBIENT TEMPERATURE 16 WATT MODEL ECM**

# SERIES FMP

These are plastic encased (not encapsulated) 3– and 10–Watt, single output a-c to d-c flyback voltage stabilizers, producing 5V, 12V, 15V or 24V.

Output is adjustable ± 10%. Voltage is limited by a zener diode across the output. Current is limited with a rectangular OC characteristic so that units may be connected in series and in parallel, and can drive both capacitive and nonlinear loads.

# SERIES FCP

These are plastic encased (not encapsulated) 3– and 10–Watt, flyback a-c to d-c switchers producing a dual output (± 12V or ± 15V).

The principal (*plus*) output is adjustable ± 10% of nominal, and the auxiliary (*minus*) output tracks it with an accuracy of ± 2% using a 3–terminal (linear) regulator. Both outputs have a rectangular current limiter to protect against overloads.

# SERIES ECM

These are triple output, 16 Watt, metal enclosed power supplies featuring simplicity and high reliability. Their principal output is stabilized by a flyback switching circuit, while their auxiliary outputs employ linear post regulators for stabilization.

**In all models,** input a-c range is 85–132V (brownout operation down to 80V a-c); input d-c range is 110-170 (nominal 145). Because of an input bridge rectifier, the d-c may be applied to the inputs with either polarity.

Input EMI filters attenuate conducted noise to below limits of the FCC Class B (0.45-30MHz., 48dB max.)

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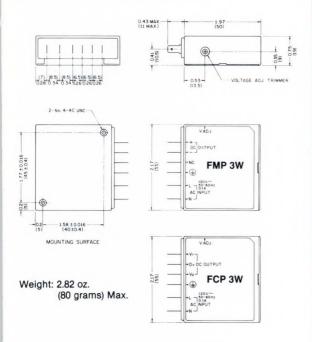
## SINGLE OUTPUT PLASTIC ENCASED SERIES FMP

| Specification | Output Voltage | | Output current | Current limit | Ripple (source & switching) | Noise (spike) | Efficiency |
|---|---|---|---|---|---|---|---|
| Units | Volts | | Amps | Amps | mV | mV | percent |
| Condition | Factory set, nom input, max load 25°C | Adjustment range | 0–50°C | Setting at 25°C nom input | Nom input max load p-p max | d-c to 50MHz nom input, max load p-p max | Nom input max load typ |
| **3 WATT MODELS** | | | | | | | |
| FMP 5-0.6K | 5.1 | 4.5– 5.5 | 0–0.6 | 0.7 ~1.2 | 50 | 100 | 68 |
| FMP 12-0.25K | 12.1 | 10.8–13.2 | 0–0.25 | 0.3 ~0.5 | 80 | 150 | 70 |
| FMP 15-0.2K | 15.1 | 13.5–16.5 | 0–0.2 | 0.25~0.4 | 80 | 150 | 70 |
| FMP 24-0.13K | 24.1 | 21.6–26.4 | 0–0.13 | 0.15~0.3 | 100 | 150 | 74 |
| **10 WATT MODELS** | | | | | | | |
| FMP 5-2K | 5.1 | 4.5– 5.5 | 0–2.0 | 2.2 ~3.3 | 50 | 100 | 75 |
| FMP 12-0.85K | 12.1 | 10.8–13.2 | 0–0.85 | 0.9 ~1.4 | 80 | 150 | 78 |
| FMP 15-0.7K | 15.1 | 13.5–16.5 | 0–0.7 | 0.75~1.2 | 80 | 150 | 78 |
| FMP 24-0.45K | 24.1 | 21.6–26.4 | 0–0.45 | 0.5 ~0.8 | 100 | 150 | 81 |

## DUAL OUTPUT PLASTIC ENCASED SERIES FCP

| Specification | Output Voltage | | Output current | Current limit | Ripple (source & switching) | Noise (spike) | Efficiency |
|---|---|---|---|---|---|---|---|
| Units | Volts | | Amps | Amps | mV | mV | percent |
| Condition | Factory set, nom input, max load 25°C | Adjustment range | 0–50°C | Setting at 25°C nom input | Nom input max load p-p max | d-c to 50MHz nom input, max load p-p max | Nom input max load typ |
| **3 WATT MODELS** | | | | | | | |
| **FCP 031K** | | | | | | | |
| Output #1 | + 12.1 | 10.8-13.2 | 0–0.12 | 0.14~0.25 | 80 | 150 | 64 |
| Output #2 | – 12.1[1] | [2] | | | | | |
| **FCP 032K** | | | | | | | |
| Output #1 | + 15.1 | 13.5-16.5 | 0–0.1 | 0.12~0.2 | 80 | 150 | 64 |
| Output #2 | – 15.1[1] | [2] | | | | | |
| **10 WATT MODELS** | | | | | | | |
| **FCP 101K** | | | | | | | |
| Output #1 | + 12.1 | 10.8-13.2 | 0–0.4 | 0.45~1.0 | 80 | 150 | 77 |
| Output #2 | – 12.1[1] | [2] | | | | | |
| **FCP 102K** | | | | | | | |
| Output #1 | + 15.1 | 13.5-16.5 | 0–0.32 | 0.35~0.9 | 80 | 150 | 77 |
| Output #2 | – 15.1[1] | [2] | | | | | |

(1) Output #2 is ± 2% of the Output #1 setting.    (2) Output #2 tracks ± 2%.

## TRIPLE OUTPUT METAL ENCLOSED SERIES ECM

| Specification | Output Voltage | | Output current | | Current limit | Ripple (source & switching) | Noise (spike) | Efficiency |
|---|---|---|---|---|---|---|---|---|
| Units | Volts | | Amps | | Amps | mV | mV | percent |
| Condition | Factory set, nom input, max load 25°C | | 0–50°C min   max | | Setting at 25°C nom input | Nom input max load p-p max | d-c to 20MHz nom input, max load p-p max | Nom input max load typ |
| **16 WATT MODELS** | | | | | | | | |
| **ECM 021K-CB** | | | | | | | | |
| Output #1 | + 5 | | 0.5 | 2.0 | 2.2 | 120 | 2% of output voltage + 50mV | 67 |
| Output #2 | + 12 | | 0.0 | 0.3 | 0.4 | 60 | | |
| Output #3 | – 12 | | 0.0 | 0.2 | 0.3 | 60 | | |
| **ECM 022K-CB** | | | | | | | | |
| Output #1 | + 5 | | 0.5 | 2.0 | 2.2 | 120 | 2% of output voltage + 50mV | 67 |
| Output #2 | + 15 | | 0.0 | 0.3 | 0.4 | 60 | | |
| Output #3 | – 15 | | 0.0 | 0.2 | 0.3 | 60 | | |
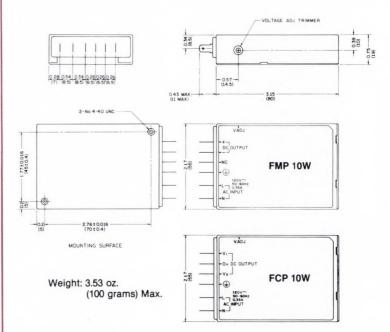
Contact factory for OEM discounts

## 3 WATT MODELS FMP/FCP



**FMP 3W**

**FCP 3W**

Weight: 2.82 oz.
(80 grams) Max.

## 10 WATT MODELS FMP/FCP



**FMP 10W**

**FCP 10W**

Weight: 3.53 oz.
(100 grams) Max.
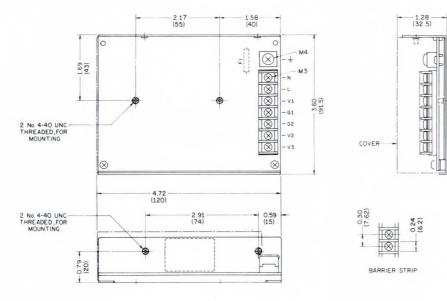
NOTES:
1. Material: phenylene oxide.
2. Dimensions in parentheses are in millimeters, others in inches.
3. Tolerance: ±0.03 (±0.7) unless noted otherwise.

4. AC & DC terminals: 0.187 inch series tabs.
5. AC & DC mating receptacles: AMP, Inc., Faston 187 series or equivalent.
6. Maximum mounting screw penetration: 0.24 (6).

## 16 WATT MODELS ECM



Weight: 13 oz.
(370 grams) Max.

NOTES:
1) Dimension in parentheses are in millimeters, others are in inches.
2) Tolerances: ±0.015 (0.4mm) between mounting holes; ±0.03 (±0.7 mm) all other dimensions.
3) Mounting screw penetration: 0.24 (6mm) maximum.
4) Material and finish:
A) Chassis: 1mm steel, cadmium plated, yellow chromate wash.
B) Cover 0.5mm steel, cadmium plated, yellow chromate wash.

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# CALENDAR

**Modern Electronic Packaging** (seminar), Santa Clara, CA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. September 7 to 9.

**International Test Conference,** Washington, DC. Doris Thomas, ITC, Box 264, Mount Freedom, NJ 07970. (201) 267-7120. September 12 to 14.

**Worst-Case Circuit Analysis** (seminar), Boston, MA. Design and Evaluation, 1000 White Horse Rd, Suite 304, Voorhees, NJ 08043. (609) 770-0800. September 12 to 14.

**C Programming Workshop** (short course), Seattle, WA. SSC, Box 55549, Seattle, WA 98155. (206) 527-3385. September 12 to 15.

**12th International Fiber Optic Communications and Local Area Networks Exposition,** Atlanta, GA. Information Gatekeepers, 214 Harvard Ave, Boston, MA 02134. (800) 323-1088; in MA, (617) 232-3111. September 13 to 16.

**Unix Hands-on Workshop** (short course), Montreal, Canada. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 13 to 16.

**Troubleshooting Microprocessor-Based Equipment and Digital Devices,** Atlanta, GA. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. September 19 to 22.

**Unix Hands-on Workshop** (short course), Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 20 to 23.

**34th IEEE Holm Conference on Electrical Contacts,** San Francisco, CA. IEEE Holm Conference Registrar, 345 E 47th St, New

## CALENDAR

York, NY 10017. (212) 705-7405. September 26 to 29.

**Troubleshooting Microprocessor-Based Equipment and Digital Devices,** Chicago, IL. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. September 27 to 30.

**Unix Hands-on Workshop** (short course), San Diego, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 27 to 30.

**Connector and Interconnection Technology Symposium,** Dallas, TX. Electronic Connector Study Group, 104 Wilmot Rd, Suite 201, Deerfield, IL 60015. (312) 940-8800. October 3 to 5.

**IEEE International Conference on Computer Design: VLSI in Computers and Processors,** Port Chester, NY. Gail Clanton, IEEE, 1730 Massachusetts Ave NW, Washington, DC 20036. (202) 371-1013. October 3 to 5.

**Autotestcon,** Minneapolis, MN. Steve Palmer, Unisys, 3333 Pilot Knob Rd, Eagan, MN 55121. (612) 456-2349. October 4 to 6.

**Buscon/88 East,** New York, NY. Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856. (203) 852-0500. October 4 to 6.

**Electronic Imaging Conference East,** Boston, MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. October 4 to 6.

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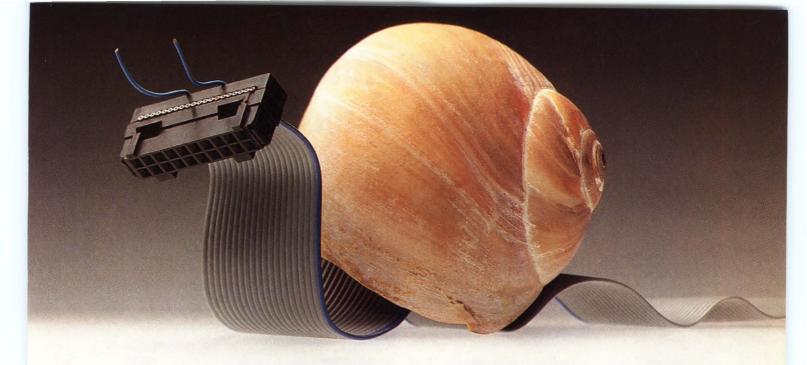
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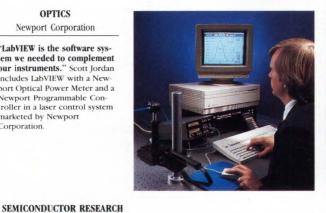
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# EDITORIAL

## Spend a lot, get a little

It looks as though preliminary work on the Superconducting Super Collider project will get underway next year. Because scientists describe the project as a 20-trillion electron-volt proton synchrotron, most people just call it the SSC or Super Collider. The project will require a particle-accelerator ring that is about 13 miles in diameter, so the SSC will be large, both in size and cost. Early next year, the Super Collider project will receive $100 million in seed money; $16 million is budgeted for equipment, and the remainder is targeted for site selection and day-to-day operations. The seed money may seem like a small amount, but the Department of Energy—the project's sponsor—puts the SSC's final price at over $5 billion. That figure doesn't include the $500 million per year necessary to run the project.

For such a big project, however, there has been little public debate within the engineering and science communities about whether we should build this massive device. That's unfortunate, because building the SSC will affect government-funded science and engineering for many years.

On one hand, the SSC's supporters provide promotional literature that describes the Super Collider's construction and operation. The basic premise is that much interesting research will be done at the SSC, and that many practical benefits will "spin off." There is a subtle message here: Our national pride and scientific stature—future Nobel prizes—are tied to this project, so let's do it. Also, backers hope that such a large project will rekindle the public's fascination with science, and that it will draw bright students to scientific careers.

On the other hand, some critics wonder if the project isn't a massive physics and construction relief project. The project would fund research for a small number of particle physicists and would create about 5000 temporary construction jobs. Certainly, equipment and service suppliers would benefit, but spending over $5 billion on a project that meets the research needs of only a few scientists seems wasteful. Even without the SCC, science will continue to fascinate the public, who has little understanding of subatomic particles. Also, few among us can name even three or four recent winners of Nobel prizes that were awarded for scientific research.

It's safe to assume that the billions of dollars of *tax money* needed for the SSC must come from other programs' budgets rather than from new tax revenues. So, it's time to decide whether the Super Collider is worth the price. If we must take money from existing and planned projects, let's consider refurbishing and rejuvenating college and university laboratories with it. The payoff would be quick. We'd still be buying equipment, supporting research, and doing some construction. And, we would fortify a broad range of engineering and scientific fields instead of waiting for potential spinoffs from particle physics.

Jon Titus
Editor

# How the fa

Our new 7.5ns PAL® device is fast enough to prove that standard logic shouldn't set the standard anymore.

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How fast would you like your standard logic?

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| Decoder | | | | |
| 74151 | tPD | 11.0 | 15.0 | 7.5 |
| Mux | | | | |
| Register/Latch | | | | |
| 74374 | tCO | 10.0 | 9.0 | 6.5 |
| Octal Register | | | | |
| 74373 | tPD | 8.0 | 6.0 | 7.5 |
| Octal Latch | tLEO | 13.0 | 11.5 | 7.5 |
| Counters | | | | |
| 74161 | tS | 5.5 | 8.0 | 7.0 |
| Four bit Ctr | tCO | 11.0 | 13.5 | 6.5 |
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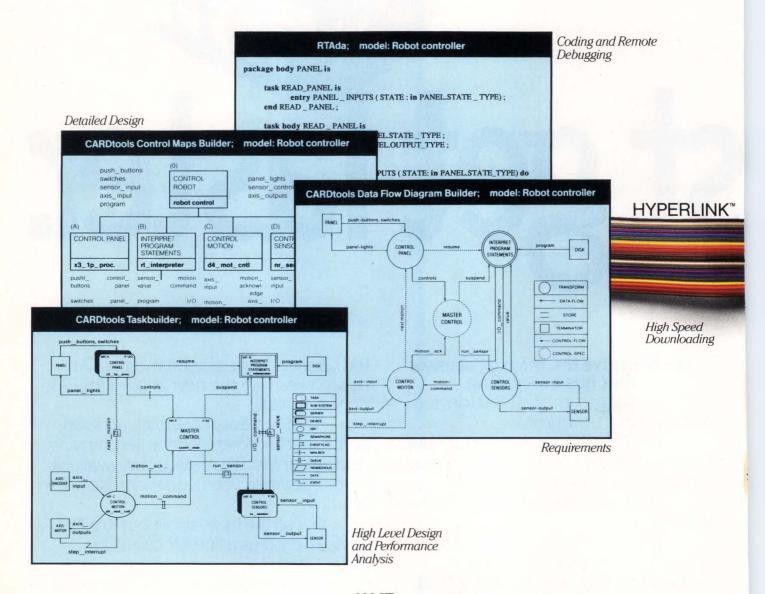
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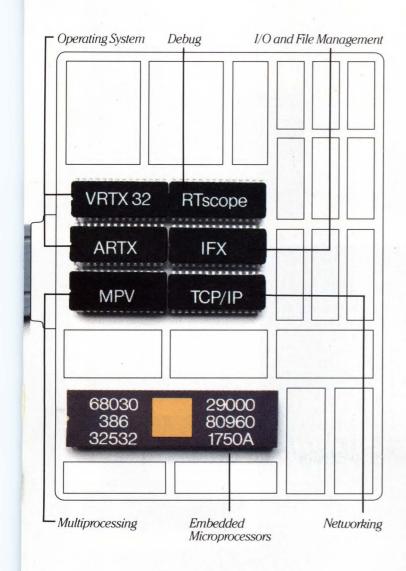
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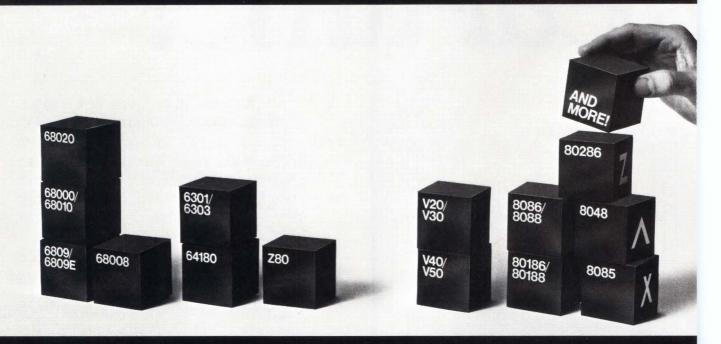
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# TECHNOLOGY UPDATE

## SCSI host adapters offer superspeed to personal-computer I/O subsystems

Maury Wright, *Regional Editor*

Personal-computer I/O performance —particularly the disk throughput —has not kept pace with the processing power offered by 80286-, and 80386-based systems. But IBM PC/AT- and Micro Channel-compatible SCSI (Small Computer Systems Interface) host adapters can provide interfaces to the highest performance 5¼-in. disk drives available. These adapters thus open the door to disk data-transfer rates of 1M byte/sec and faster. Furthermore, a single host adapter can give you a great deal of flexibility by connecting a variety of other peripherals, such as tape and optical-disk drives, printers, scanners, and communication controllers, with your personal-computer system.

As it evolved out of SASI (Shugart Associates Standard Interface), which was a simple intelligent disk interface, SCSI developed into a truly intelligent universal systems interface. Theoretically, its 8-bit parallel bus can connect with any peripheral. The SCSI specification committee, which is a standing ANSI group, is in the process of defining device command sets for software interfaces to various peripheral types, each of which requires a completely different command set. The committee defined a command set for disk and tape drives several years ago.

Manufacturers of ¼-in.-cartridge-tape drives have adopted SCSI as the interface of choice. According to Emulex's product manager Kevin Drum, at least half of the sales of the company's IB02 host adapter for the PC/AT bus have been to customers that use the product strictly as a tape-drive interface. The adapter is



*The Micro Channel SCSI host adapter from Future Domain, Model MCS-350, supports both bus POS and arbitration schemes, and is compatible with optical and tape drives as well as disk drives.*

currently compatible with the company's dedicated tape and disk controllers. And the company has recently been working to ensure the compatibility of the adapter with tape and disk drives that have the SCSI and its controller embedded. The IB02 costs $325.

### SCSI proliferates

The committee working on SCSI didn't stop with tape and disk command sets. It has also written command sets for optical disks and printers, and for communications between multiple SCSI hosts. In fact, many optical-disk products now use SCSI exclusively. Moreover, the committee plans to eventually write command sets for image scanners, communication controllers, and other devices. A number of companies have already introduced

such products with proprietary command sets that work with the SCSI bus, even though no standard set yet exists.

Integrators and system designers can use a SCSI host adapter as a cost-effective interface to connect as many as seven different peripherals to a personal computer. NCL America, for example, sells its 5109 host adapter for $95 (100). The product only performs 8-bit host-bus transfers, but it can still outperform typical personal-computer disk controllers.

### Data rate is key

While SCSI can give you versatility in the number and types of peripherals your system can use, it can go even further when it comes to disk drives—it can increase disk throughput somewhat dramatically.

# TECHNOLOGY UPDATE

Increasing throughput means reducing the time required to transfer data from system memory onto the disk drive, or the time required to transfer data from the disk into system memory. The SCSI specification sets the maximum rate for asynchronous data transfers at 1.5M bytes/sec, and the maximum rate for synchronous data transfers at 4M bytes/sec.

In most MS-DOS-based systems, a combination of a disk's seek time and its data-transfer rate directly determine a disk's throughput (other factors such as multithreading affect disk throughput in multitasking environments like Unix systems and networks). Today most personal computers, even 80386-based systems, come equipped with an ST-506 controller and disk drive.

Average seek times on high-end ST-506 drives have dropped to less than 30 msec. Most ST-506 controllers, however, use MFM encoding that results in a 5M-bit/sec disk data rate. RLL encoded drives are becoming increasingly popular; they can produce 7.5M and sometimes 10M bits/sec (albeit not always reliably).

## New drives seek in 20 msec

State-of-the-art drives with embedded SCSI controllers, by comparison, have average seek times of less than 20 msec, and transfer rates ranging from 1M to 1.5M bytes/sec. Granted, the intelligence inherent in a SCSI subsystem does result in a small amount of command overhead not found in ST-506 subsystems. The embedded controller must decode SCSI commands, and the consequent overhead can be as much as 5 msec on older drives, but is typically less than 1 msec on newer products. The **box**, "The SCSI advantage," provides an example of how a SCSI system can improve a computer's performance.

### Adapter for Micro Channel

IBM recognized the problem of poor disk throughput, and on its high-end Micro Channel personal computers offers an ESDI (Enhanced Small Device Interface) controller and drive. ESDI drives include a data separator and typically generate a 10M-bit/sec serial data stream from the disk drive to the controller. Some new ESDI drives even operate at 15M bits/sec. Other companies, such as Compaq, ship

## The SCSI advantage

A number of disk-drive and controller manufacturers and technical publications have run a variety of benchmarks on personal-computer I/O implementations. Unfortunately, different benchmarks yield dramatically different results. To evaluate the SCSI-based disk I/O in a personal computer completely, you should test an I/O subsystem in your intended application. But some simple tests do provide an example of the potential performance of SCSI-based systems compared with ST-506-based systems.

Measuring the time it takes to load a standard set of office-automation programs into memory, for example, is one simple test of disk I/O. I tried loading the Wordperfect Library Shell, Wordperfect 4.2, and the Library companion programs. For a second test, I loaded Windows/286 and the Calendar, Cardfile, Clock, and Control Windows' application programs.

I ran the tests on a 10-MHz IBM PC/AT compatible with an EGA monitor and MS-DOS, version 3.2. I tested two SCSI host adapters, the Adaptec AHA-1540 and the Future Domain TMC-830, and two disk drives, a Maxtor (San Jose, CA) 280M-byte XT3280 drive and a Priam (San Jose, CA) 280M-byte Model 728 drive. For comparison, I tested a Western Digital ST-506 controller with a 40M-byte Micropolis ST-506 drive.

The Maxtor and Micropolis drives specify an average seek time of 28 msec; the Priam drive specs 20 msec. I conducted all of the tests after a fresh disk format, so the disks held only the test programs. I measured the load times with a manual stopwatch.

Predictably, all combinations of a SCSI host adapter and SCSI disk produced virtually identical results. Using the SCSI components, the computer loaded the Wordperfect programs in times ranging from 2.5 to 2.75 secs (my manual measuring probably accounts for the variation). The SCSI subsystems loaded the Windows/286 program and applications in times ranging from 8 to 9 secs. The system, when accessing the ST-506 controller and drive, required 4 to 4.25 secs to load the Wordperfect test, and 11 to 12 secs to load the Windows test.

Don't just take these figures at face value. The addition of the SCSI components may actually enhance performance more than those figures strictly say. For example, the system spends a some portion of the time required to load Windows/286 and its applications setting up the EGA graphics. So in the Windows test, the 3-sec improvement represents exclusively the advantage gained in the time it takes to read data off the disk into memory because the time it takes to set up the EGA graphics remains constant.
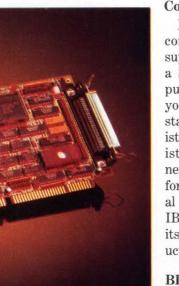
ESDI controllers with IBM PC/AT-bus systems. In fact, Western Digital, Adaptec, NCL America, and Scientific Micro Systems all offer such controller products.

SCSI and ESDI disk drives feature equivalent mechanical seek times—average seek times can be as fast as 16 msec. The magnetic-recording technology limits the read-channel data rate on either type of drive to 15M bits/sec at the present

tomatic configuration. Adaptec and Western Digital have also introduced Micro Channel SCSI host adapters and will start shipping them in volume later this fall. SCSI supports faster data rates than ESDI does. And although the SCSI maximum transfer rates exceed disk read-channel data rates, the intelligent interface provides ways to take advantage of the higher rate.

Quantum (Milpitas, CA), for example,

you must first buy a SCSI adapter. Surprisingly, price isn't a critical issue because you can buy even the highest performance host adapters for prices competitive with the prices of the other types of controllers. Within a year or two, drives with embedded intelligent controllers will be the lowest-cost drives available—the intelligent interface lets drive manufacturers mask defects and so increase yields.



*Capable of a maximum 10M-byte/sec data rate across the IBM PC/AT bus, the Adaptec AHA-1540 includes a local μP and supports synchronous and asynchronous SCSI transfers.*

## Consider compatibility first

Instead of price, performance and compatibility, including software support, should guide your choice of a SCSI adapter for personal computers. In terms of compatibility, you should keep in mind that no standard for SCSI host-adapter register sets or software interfaces exists, primarily because IBM has never offered a SCSI host adapter for its personal computer. For several years, rumors have hinted that IBM would offer a SCSI board for its personal computers, but no product has appeared.

## BIOS handles MS-DOS disks

Achieving compatibility between MS-DOS and hard disks is relatively easy for host-adapter manufacturers. They either include BIOS software that emulates the standard interrupt-13 interface used by MS-DOS with the ST-506 controllers, or they include an installable device driver. Some do both. The problem is that MS-DOS presently includes no facilities to control tape drives, optical disks, or other peripherals such as scanners.
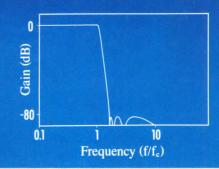
The picture becomes cloudier when you consider other operating systems and network environments. If you're an OEM, you can write driver and application software for any type of SCSI device, and for any operating system, but this option requires extra time and money for software development. Generally then you should want to select an adapter that has sufficient software support as well as compatibility.

time. And neither a SCSI host adapter or ESDI controller has an inherent advantage in data-transfer rate across the system bus. Using SCSI does impose the minimal command overhead time of the embedded controller. But SCSI host adapters provide a potentially higher performance alternative.

Future Domain offers one of these potentially higher-performance alternatives to an ESDI controller for Micro Channel. The $390 MCS-350 Micro Channel SCSI host adapter supports the maximum 1.5M-byte/sec SCSI transfer rate. The host adapter supports Micro Channel arbitration, DMA, and the POS (Program Option Select) scheme for au-

ample, includes a read-ahead cache on embedded controllers for its disk drives. On cache hits, the SCSI interface can operate at maximum speed, reading out of the cache semiconductor memory rather than from the disk. And the cache hit eliminates mechanical seek time. Most manufacturers of high-end drives will have introduced a similar feature by the end of this year. SCSI also allows schemes such as simulating a single drive with an array of drives operating in parallel. Micropolis (Chatsworth, CA) offers a 5-drive array that can effectively quadruple data-transfer rates.

To take advantage of the higher performance rates that SCSI offers,

*A 16k-byte read-ahead cache created in system memory by the driver software supplied with Western Digital's 7000-FASST2 board eliminates disk-access and data-transfer delays on consecutive disk reads of contiguous data.*

Of all the packages available, Future Domain currently offers the most comprehensive hardware-software combination by far for its host adapters. The TMC-800 family of host adapters for the IBM PC and PC/AT buses and for the MCS-350 Micro Channel bus feature a common SCSI architecture and system software interface. The TMC-800 boards range in price from $198 to $220; some include standard floppy-disk-drive controllers.

A kit including a cable and a menu-driven installation software for MS-DOS, Xenix, and Netware, adds $90 to the basic board price.



*An MS-DOS software driver for WORM drives available with the Rancho Technology RT10-AT host adapter installs the optical drive for use as a standard disk.*

The kit contains partitioning software that breaks the 32M-byte disk volume limit of MS-DOS. The boards are compatible with virtually all MS-DOS software, including third-party disk-partitioning packages and several optical-disk and tape-drive control packages. The company also has established an OEM interface module that allows you to easily integrate new peripherals with its adapters.

Adaptec introduced its AHA-1540 host-adapter board about a year ago. It's compatible with MS-DOS, Xenix, Unix, and Netware, and sells for $349. In addition, Sytron's (Londonderry, NH) tape-backup package supports the board. For normal MS-DOS use, you can install the board by simply accessing onboard firmware with the operating system's Debug utility.

The RT10-AT from Rancho Technology is MS-DOS compatible and includes a proprietary tape-backup package ($299). A Unix or Xenix driver costs $35 for 80286-based machines and $65 for 80386-based machines (both in 100-unit quantities). A Netware driver costs $45 (single-unit price). An optical-disk package is also available for an extra $450.

Western Digital includes MS-DOS, Xenix, Unix, and Netware drivers with its 7000-FASST2 host adapter for $495. It's also compatible with the Sytron tape-backup system. The boards should be available in quantity this month.

## OS/2 causes logistic problems

Every manufacturer of PC add-in boards plans to offer OS/2 compatibility, although none has finalized its plans. The operating system is only available to OEMs, however, and it will not accept installable device drivers as boot devices. The host-adapter manufacturers therefore can't offer a generic OS/2 driver.
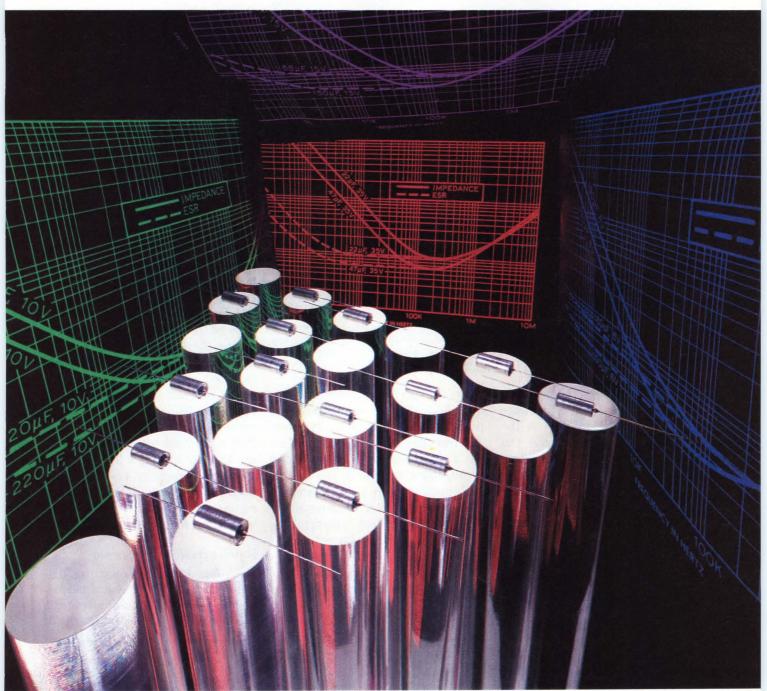
For typical MS-DOS applications, any of the products discussed in this article will perform equally well. Keep in mind that MS-DOS is a single-tasking operating system— the CPU performs no other task while disk I/O takes place.

All of the host adapters discussed here offer transfer rates faster than a typical disk can accomplish. And all of them can transfer data across the system bus faster than the SCSI bus operates. Therefore, the physics of the disk drive actually define the performance limits of the I/O system.

There are some exceptions to this general rule. A cache-based controller, for example, can exceed the standard asynchronous SCSI data rate. If you plan to use a drive with a cache, you should consider the Adaptec and Western Digital boards. Both boards can operate in the faster synchronous SCSI mode. Western Digital also offers a cache feature with its host-adapter board. The MS-DOS driver supplied with the board establishes a 16k-byte read-ahead cache in system memory. On cache hits, the driver never even accesses the SCSI bus.

For applications in multitasking or networked systems, you should compare performance specifications

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*Menu-driven MS-DOS, Netware, and Xenix installation software, and compatibility with other third party application programs, I/O managers, and operating systems are key features of Future Domain's IBM PC/AT-compatible host adapters for turnkey applications.*

much more carefully than you do with MS-DOS systems. Because multitasking can occur both at the SCSI-bus and host-bus levels, the transfer rates of both buses become more critical in these environments. For instance, while a SCSI host adapter transfers a block of data into memory, a network controller has to wait to use the system bus. Therefore, a fast host-bus transfer rate frees the bus sooner.

The IBM PC/AT bus lacks sophisticated features such as multimaster arbitration; the bus also has to be cleared regularly for a refresh cycle. The host-adapter manufacturers have made every attempt to speed this bus up, but they all have different ideas about which host-adapter architecture is the best.

Future Domain, for example, does not use DMA to move data. The company's host adapters depend on the CPU to perform memory-mapped I/O. Company president Jack Allweiss believes you obtain better performance if you let the 80286 or 80386 handle the I/O rather than giving it to a less powerful processor. Allweiss points out that it takes 2 μsecs of overhead to start a DMA operation. And in 80386 and protected-mode 80286 environments, the data is typically fragmented in physical memory, which adds additional overhead to some DMA operations.

### Mailboxes provide interface

Bruce Bonner, marketing manager at Western Digital, and Ed Turner, marketing manager at Adaptec, both claim that the CPU is best utilized performing other tasks during I/O operations. Both Western Digital and Adaptec include a μP on its host adapters, and both use mailboxes for passing messages between the CPU and the host adapter.

Adaptec, Western Digital, and Rancho Technology host adapters all use first-party DMA to move data. In a first-party DMA operation, the host adapter takes control of the bus and performs the DMA operation independently of the mother-board DMA controller. The Rancho Technology R10-AT, however, does not include a local μP. According to company vice president John Fobel, a local μP and firmware restricts the flexibility you have in writing drivers for a host adapter.

### Rates exceed 5M bytes/sec

All four of the architectures discussed result in impressive performances. All of the boards transfer data across the host bus at speeds in

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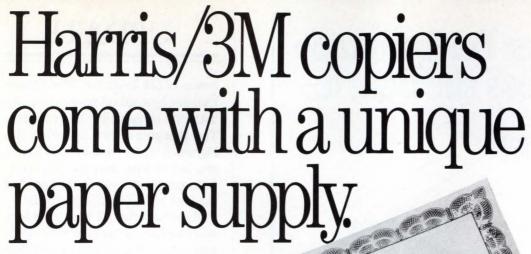
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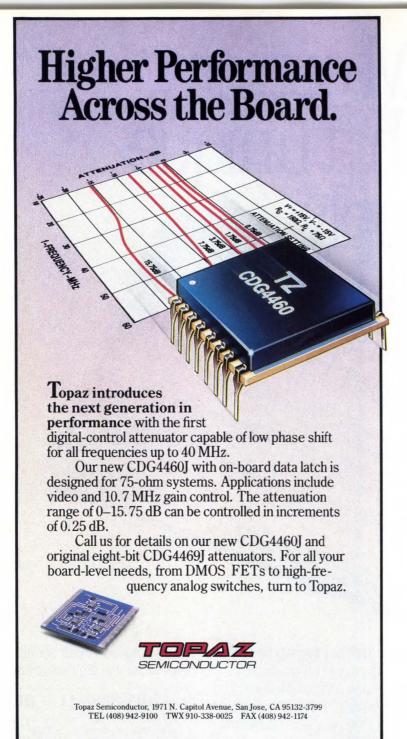
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excess of 5M bytes/sec. The Future Domain host adapters achieve the data rate using only 8-bit transfers. The Adaptec board specifies the highest transfer rate at 10M bytes/sec, but all host-bus data-rate specifications are subject to the speed of the host IBM-PC/AT compatible.

Manufacturers of host adapters will continue to improve their products in the areas of both compatibility and performance, since each manufacturer would like to establish a defacto standard for SCSI in IBM-compatible personal computers. And other vendors will soon join the fray. Scientific Micro Systems, for example, plans to ship a host adapter that matches the performance of the boards discussed here. The board should be available this fall, and the company plans to offer it at a price lower than the competition.

Don't rule out IBM. It can establish a standard flavor for SCSI on personal computers with a single product introduction. Although IBM is not very likely to introduce an IBM PC/AT bus product now, a Micro Channel host adapter could still establish a register set and software interface.　**EDN**

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Wright, Maury, "SCSI ICs simplify I/O-bus configurations, but options entail extra design effort," *EDN*, Sept 18, 1986, pg 97.

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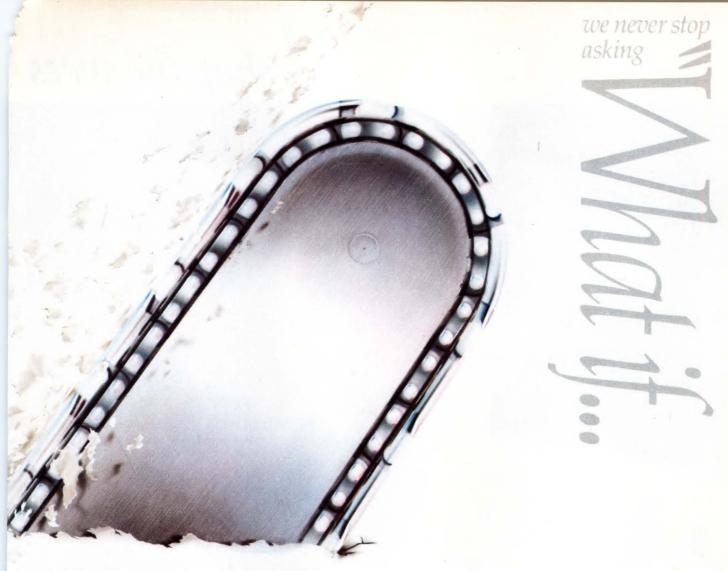
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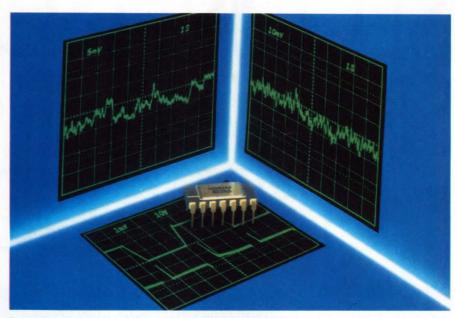of Quantum Corporation.

**CIRCLE NO 59**

# IAs pull low-level signals out of noisy environments

David Shear, *Regional Editor*

Unwanted noise can contaminate electronic signals and complicate their acquisition in various ways, so if you need to acquire a differential signal that is mixed with unwanted common-mode noise and voltage, consider using instrumentation amplifiers (IAs). They are high-gain dc-coupled differential amplifiers characterized by three traits: a single-ended output, high input impedance, and high common-mode rejection (CMR). Generally designers use these devices to amplify small differential signals coming from transducers that may generate large common-mode signals (**Ref 1**).

**Fig 1** shows the noise sources that can affect a system. The $e_s$ voltage is the desired signal from a transducer. The $e_c$ voltage is any common-mode voltage or signal; it could be a 60-Hz signal from a bad ground or ground loop; $e_c$ could also be a dc bias voltage that the transducer requires. The $e_n$ voltage is any radiated noise such as the ubiquitous 60 Hz or any signal picked up by nearby digital circuitry. If you assume that the physical properties of the cable connecting the transducer to the IA are identical for both inputs, then you can also assume that any radiated noise ($e_n$) is equal in magnitude and phase at the inverting and noninverting inputs of the IA. Therefore, the infinite common-mode rejection of an ideal IA would eliminate the effects of $e_n$. Similarly, the signal from $e_c$ would be equal on both of the inputs to the IA and would also be eliminated.

But in reality, an IA's common-mode rejection is finite. CMR defines how well an amplifier rejects common-mode signals. The ratio of



*Low noise, fast settling time, and high CMR highlight the instrumentation amplifiers that are available today. The AD624 from Analog Devices also offers 0.001% nonlinearity for precision transducer applications.*

the change in output voltage to a change in common-mode input voltage represents the common-mode gain. The ratio of the differential gain to the common-mode gain is the common-mode rejection ratio (CMRR). The general equation for this relationship is logarithmic: $CMR = 20\log_{10}CMRR$. When the CMR is high enough, you can reduce the unwanted signals to the point where they no longer affect your measurements.

### Three kinds of IAs

IAs come in three flavors: the differential amplifier, the classic 3-op-amp voltage-feedback IA, and the current-feedback IA (also called the differential transconductance amplifier). The differential amplifier is a single op amp with a feedback network that accepts a differential signal (**Fig 2**). You can make a differential amplifier yourself very easily with an op amp and four resis-

tors. Getting resistors that are matched and that track each other over the temperature range, however, is not so easy.

To solve the problem, Burr-Brown offers a series of differential amplifiers that have the resistors on board. The INA105 is a precision unity-gain differential amplifier that combines a precision op amp and a laser-trimmed low-drift resistor network on a single chip. The device has a maximum gain error of 0.01% and a maximum nonlinearity of 0.001%. Prices start at $3.50 (100). For those applications that require higher gain, consider the INA106, which has a gain of 10 (from $5.15, 100). The INA117 is a unity-gain differential amplifier that can accept as much as ±200V of common-mode voltage. It costs $4.20 and up (100).

Differential amplifiers have some drawbacks: The feedback network is connected directly to the source. As a result, the input impedance of the

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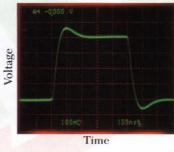
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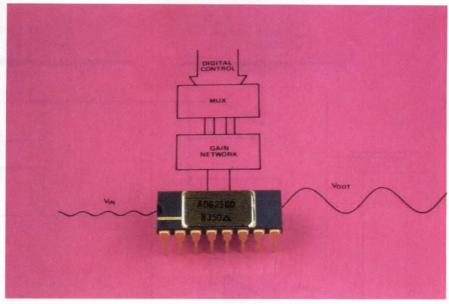
# SIGNAL PROCESSING EXCELLENCE

**CIRCLE NO 101**

# TECHNOLOGY UPDATE

differential amplifier depends on the value of the input resistor, which usually isn't very high. With a rather low input impedance, the two source resistances of the transducer being measured must be very low and extremely well matched, or both the gain accuracy and the CMR suffer. Also, for many measurements, you need a 100- to 120-dB CMR, and the differential amp's CMR of about 80 dB just isn't quite high enough. Thus for many applications, the differential amplifier will not meet your needs.

## Beyond the differential

For those applications where the differential amplifier can't quite cut the mustard, consider a classic 3-op-amp voltage-feedback IA (**Fig 3**). This IA has two op amps (IC$_1$ and IC$_2$) that buffer the input and present a very high impedance to the source. Further, IC$_1$ and IC$_2$ provide high differential gain for the desired signal but only unity gain for the common-mode signal. This combination improves the amplitude of the differential signal relative to the common-mode signal and thus results in a higher CMR than is possible when using a differential amplifier. The output of the first stage (IC$_1$ and IC$_2$) goes to the differential-amplifier stage (IC$_3$); the result is a single-ended signal with very high CMR.



*Software-selectable gains are useful for software-controlled data acquisition. The AD625 from Analog Devices allows you to add external gain switches and a resistor network without the added errors caused by the on-resistance of the switches.*

Many of the voltage-feedback IAs have extra terminals to improve the precision of the IA even further. A sensing terminal can compensate for any drop between the output and the load, and the reference can compensate for any differences in ground potential between the IA and the load. The guard terminal allows the use of a shielded cable on the input without increasing the parasitic capacitance from the shield.

The AD524 (from $9.90, 100) and the AD624 (from $11.90, 100) from Analog Devices are two 3-op-amp voltage-feedback IAs that are pin-programmable for gains of 10, 100, or 1000, and of 1, 100, 200, or 500, respectively. Or you can use a single external resistor to select the gain for these devices within a range from 1 to 1000. At a gain of 1000, the CMR is 130 dB for the AD624 and 120 dB for the AD524.

For gains from 1 to 10,000, consider the AD625 (from $6.95, 100). Three external resistors set the gain of this IA. Using the AD625, you can program the gain via external switches. Generally, employing those switches for gain control can
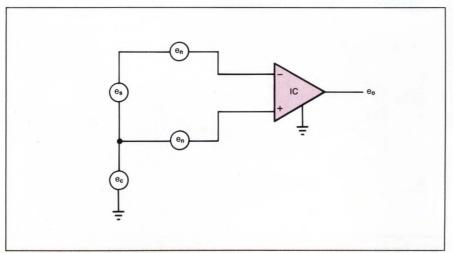


*Fig 1—A sufficiently large CMRR can virtually eliminate the noise sources that can affect your desired signal.*
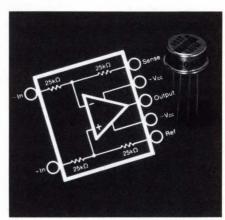


*Fig 2—The differential amplifier includes an op amp and feedback resistors. The INA105 (Burr-Brown) has matched and stable resistors built on the device so you don't have to worry about them.*
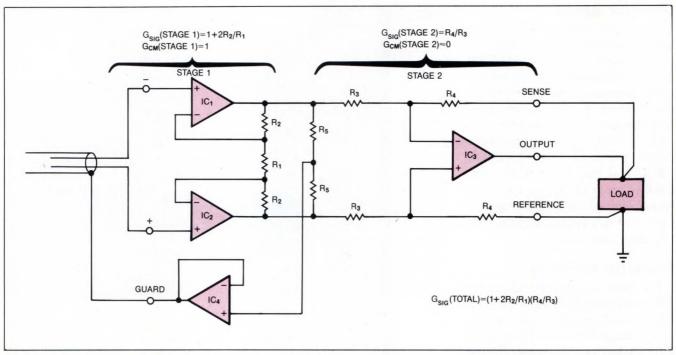
*Fig 3—The classic 3 op-amp voltage-feedback IA* has excellent CMR along with very high input impedance. You can use the fourth op amp (IC₄) to drive the guard.

In the figure: $G_{SIG}(\text{STAGE 1})=1+2R_2/R_1$, $G_{CM}(\text{STAGE 1})=1$, $G_{SIG}(\text{STAGE 2})=R_4/R_3$, $G_{CM}(\text{STAGE 2})\approx 0$, $G_{SIG}(\text{TOTAL})=(1+2R_2/R_1)(R_4/R_3)$

cause inaccuracies because of the on-resistance of the switch. The AD625 is designed to eliminate this error source.

Burr-Brown's INA101 is a 3-op-amp IA that costs $5.35 (100). It's also available in a military version—the INA101/883B—for prices starting at $40.50 (100). The INA104 (from $15.55, 100) has a fourth op amp on board to allow gains as high as 10,000; or you can use the extra op amp for filtering, shifting the output level, or driving the guard. Prices start at $15.55 (100). For low-power applications, you can use the INA102 (from $5.65, 100). Its quiescent current is 1 mA; it has pin-programmable gains of 1, 10, 100, or 1000.

## Another option for IAs

Current-feedback IAs (**Fig 4**), such as the AMP-01 from Precision Monolithics, differ from the classic IAs, which use voltage feedback. Two resistors set the gain over a range of 0.1 to 10,000. The ratio of a scale resistor ($R_{SCALE}$) and a gain-set resistor ($R_{GAIN}$) determines the gain. Current sources control the flow of internal currents, developing

the input voltage across $R_{GAIN}$. This current flows through $R_{SCALE}$ and produces an output voltage that is proportional to the input voltage. Prices start at $9.90 (100).

Precision Monolithics' AMP-05 is similar to the AMP-01 except it also has JFET inputs, dual guard-drive

circuitry, and a 100-μA current source for transducer excitation. In comparison with the AMP-01, the AMP-05 doesn't have as high an output-drive capability or as low an input offset and drift.

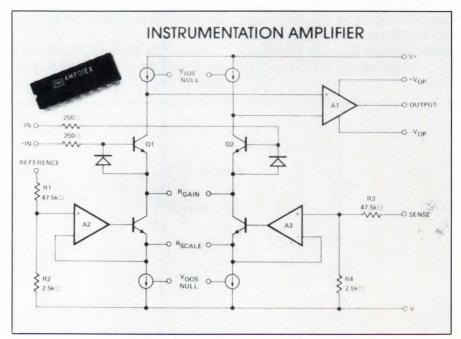The current-feedback IA is also known as a differential transcon-



*Fig 4—The current-feedback instrumentation amplifier* uses a different circuit topology to achieve the same goal as the classic 3-op-amp voltage-feedback IA. This current-feedback IA has the advantage of nearly constant bandwidth with changing gain.

ductance amplifier. A popular term at present, current-feedback has become synonymous with the capability of varying the gain without changing the bandwidth of the IA. The INA110 from Burr-Brown is an FET input IA with pin-programmable gains of 1, 10, 100, 200, or 500. Prices start at $6.20 (100).

## IA in an 8-pin DIP

The Precision Monolithics AMP-02 current-feedback IA is available in an 8-pin DIP for even more space savings than you normally have with IAs (from $5, 100). One resistor sets the gain of this IA from 1 to 10,000. For a gain of 1, no resistor is needed.

The PGA200/201 from Burr-Brown is a programmable-gain IA that is controlled by a 2-bit TTL input. The PGA200 provides gains of 1, 10, 100, and 1000; the PGA201 offers gains of 1, 8, 16, 64, and 512. For gain selection, these 3-op-amp IAs feature an onboard latch along with a multiplexer and a resistor network. Prices start at $39.40 (100).

National Semiconductor's LH0084 (from $33.50, 100) allows a gain of from 1 to 100. The first stage is software controllable for a gain of 1, 2, 5, or 10; you jumper-select the second stage for a gain of 1, 4, or 10.

If you want to have an on-chip T/H amplifier for use with A/D converters, you might consider the Analog Devices AD365 programmable-gain IA. Two unlatched digital inputs set the gain of this IA to 1, 10, 100, or 500. Pricing begins at $61.95 (100). Another combination device is the XTR101 from Burr-Brown. This device combines an IA front end with a 4- to 20-mA 2-wire transmitter. Prices start at $6.35 (100).

Even if you decide you must build your own IA, you don't have to start from scratch. You can use a differential amplifier as the difference amplifier in a 3-op-amp design. The LTC1043 from Linear Technology, which starts at $2.95 (100), is a dual, precision-instrumentation switched-capacitor building block. With this device and one op amp, you can make an IA that has CMR of 120 dB to well beyond 10 kHz and that runs off a single 5V supply.

## Some typical problems

IAs create some common problems. One is the potential for saturating the input without knowing it. To avoid saturating the input, make sure that the input voltage doesn't exceed the common-mode voltage range (CMVR). You can calculate the CMVR for linear operation from:

$$CMVR = \pm(IVR - (V_{OUT}/(2G)),$$

where IVR is the data-sheet specification for input-voltage range, $V_{OUT}$ is the maximum output signal, and G is the chosen voltage gain.

You must also always make sure you refer the input to common ground—otherwise you end up with a floating output. If the source resistance is more than 1 k$\Omega$, you must use two 1-M$\Omega$ resistors to ground at the input. To avert another potential problem, you should add the settling time of the IA to the acquisition time when you use an IA with a multiplexer.

Lately, the op-amp industry has been bustling as long-awaited processes and designs are finally entering the market. These same advances will soon begin to show up in the IAs, too. You can expect to see single 5V and low-power devices and more combination devices with adjustable frequency response. And you can also expect to encounter some IAs that begin to approach the ideal in CMR, bandwidth, and input-bias currents. **EDN**

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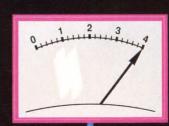3. Graeme, Jerald, "Instrumentation amps begin to challenge op amps," *Electronics*, April 28, 1988, pg 125.

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# Parallel processing ushers in a revolution in computing

John Gallant, *Associate Editor*

Parallel processing is not a new idea—it's been around at least since the 1960s. Back then, however, it couldn't be implemented practically. For one thing, there were no compilers that could use parallelism efficiently. Neither was there any way to transport large programs running on giant von Neumann computers to parallel machines. Now, both these problems have been solved: The programs are transportable, and parallel compilers are commercially available. You can now design powerful, efficient parallel-processing computers by using a variety of parallel-computing techniques.

Parallel processing can take many forms, but in essence, it spreads computing tasks over more than one processor. The goal is either to speed up a given application by running different tasks in parallel or to solve more-complex problems. Several recently developed computer architectures increase computational power over that of earlier architectures by replicating the elements that process the data. The elements are connected to some type of network, so that the multiple tasks can communicate with each other.
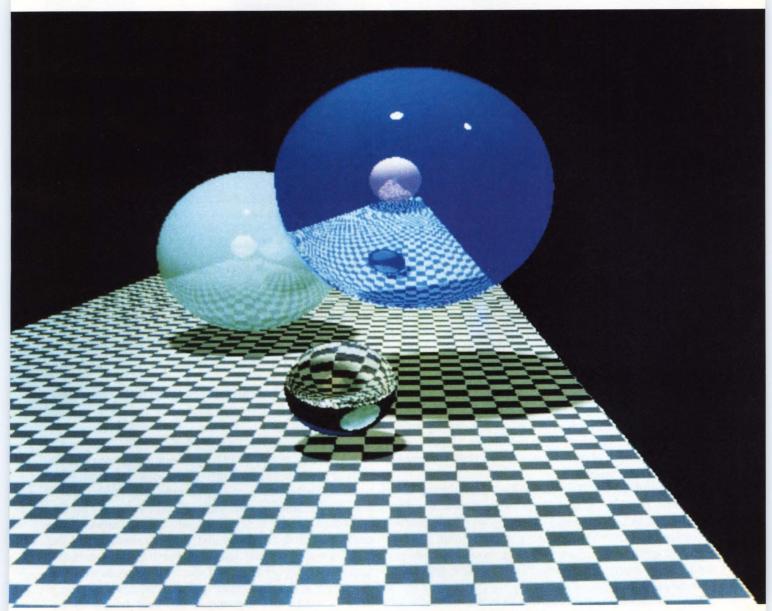
The parallel architectures attempt to break through the speed limitations imposed by the traditional von Neumann architecture. The von Neumann machine, which was conceived more than 30 years ago and is the basis for most single-processor machines, consists of one processing element (PE), a number of storage registers, a program-sequence control unit, and a glo-

bal memory. The machine executes programs by fetching instructions from memory, reading an operand, executing the instruction, and storing the result.

The various parallel architectures are designed to break through the von Neumann bottleneck. This bottleneck occurs because the single processor must access the global memory sequentially, so the memory-access time limits the speed at which a program can execute. The early parallel machines used a combination of multiple processors and vector-processing units to solve specialized matrix problems. The supercomputers, such as the Cray II and the Cray X-MP/48, are outgrowths of this activity. These supercomputers use expensive hardware technologies, such as ECL (and, in some cases, GaAs) to deliver hundreds of millions of floating-point operations per second (M flops), and their prices start at $2 million.

Computer systems whose performance is in the VAX to Cray range take advantage of less-expensive technologies and innovative system architectures to achieve performance figures approaching those of the supercomputers while maintaining prices in the $100,000 to $2 million range. These computers owe their increase in performance to a variety of parallel-processing architectures. It is this class of computers that affords the most representative view of the various parallel-processing techniques.

Because a von Neumann machine operates on each piece of data in a sequential manner, it's considered to

*For years, parallel-computing architectures existed merely as university research projects. Now these architectures are commercial realities. Today's parallel processors, techniques, and languages can help you create powerful minicomputers whose processing capabilities equal or exceed those of supercomputers.*



***Ray-tracing techniques produced this 1024×1024-pixel image*** *in approximately five seconds on the DAP 510 computer from Active Memory Technology.*

The parallel architectures attempt to break through the speed limitations imposed by the traditional von Neumann architecture.



*Iterated function codes* reproduced this representation of a fern on Active Memory Technology's DAP 510 computer.

be a single-instruction single-data (SISD) architecture. Parallel machines are classified as either single-instruction multiple-data (SIMD) or multiple-instruction multiple-data (MIMD). In an SIMD machine, a single instruction operates on many data elements. Examples include vector and array processors that perform the same mathematical operation on each element of a vector or an array. Most of the parallel-processing machines, however, are MIMD structures, so they can perform multiple tasks or processes in parallel.

Three interconnected factors characterize the various parallel-processing architectures **(Ref 1)**. The first factor is the topology of the interconnections between the parallel-processing elements (PEs) and the system memory. Parallel-computing architectures range from tightly to loosely coupled networks. A tightly coupled network results when each PE and the global memory share an address space. The elements communicate with each other via addressing on a word-by-word basis. A loosely coupled network dosen't share any address space; therefore, the elements must communicate by message passing.

The second factor is granularity. Granularity is a qualitative measure of the computational power of the PEs. PEs with lots of computational power have coarse granularity; PEs with limited computational ability have fine granularity. Commercially available systems range from many single-bit PEs to a few powerful general-purpose PEs.

The third factor is the control and synchronization of the various processes that each of the elements performs. The balanced distribution of tasks is essential for



*The Symmetry Series computers have a shared-memory architecture,* which can have as many as thirty 32-bit processing elements. These systems, from Sequent, can deliver from 6 to 81 MIPS.

efficient parallel processing. The time required for communication among processes also affects the system's efficiency: The overall program control must synchronize all the tasks. To design a parallel-processing computer, therefore, you must take into account the relationship among the system architecture, software parallel-control features, and the specific application.

### Shared-memory architectures are tightly coupled

Taking a look at the architectures for some parallel machines will help to explain these three factors. The most tightly coupled topology for a parallel machine is one in which multiple PEs are connected to a shared memory via a single high-speed bus. Examples of machines with this topology include the Encore Multimax family, the Sequent Balance and Symmetry series, and the Alliant FX Series of computers. These MIMD machines can dynamically distribute tasks to any of the PEs by using a Unix-based operating system that's symmetrically distributed over all processors. The operating system's kernel queues the processes on a priority basis and maximizes the load balancing between PEs.

The PEs in both the Encore and the Symmetry

machines are coarsely granular; the PEs in the Alliant machine are moderately and coarsely granular. The Multimax 320 can interconnect as much as 128M bytes of shared memory with as many as 20 CPUs (the NS32332 µP) operating on a 100M byte/sec bus (the Nanobus). The system can deliver from 4 to 40 MIPS performance. Similarly, Sequent's Balance and Symmetry series of computers use a system bus capable of an 80M byte/sec transfer rate. The Symmetry Series can connect as much as 240M bytes of shared memory to as many as 30 CPUs (the 80386 µP) operating on the bus. The system can deliver 6 to 81 MIPS performance.
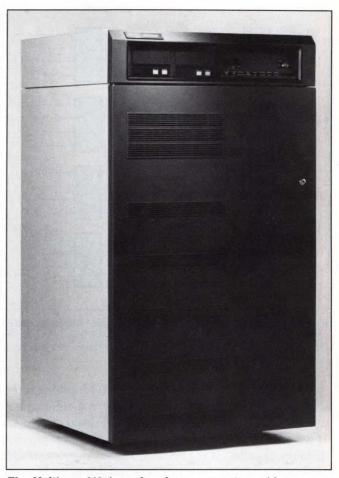
The FX/80 has as many as eight 64-bit vector processors that are capable of providing a peak perfomance rating of 188.8M flops. In addition, the computer has 12 scalar PEs that handle the data transfer to 12 independent I/O channels. The system has as much as 256M bytes of memory and a 188M-byte/sec bus.

How many PEs a single high-speed bus architecture can accommodate is determined by the bus bandwidth. Although the shared-memory systems use high-speed coherent cache memories to reduce the bus traffic, the high-speed bus architecure probably can't support more than 50 processors. To scale a program over a much larger array of processors, the interconnection topology must be looser.

### The scale for shared resources is limited

Shared memory systems that connect the PEs and global memory through switches stand at the crossroads of tightly coupled and loosely coupled architectures. Even though these systems transfer data through an address mechanism, additional information is required to route the data through the switch network. In addition, the cost of the switching elements places a practical limit on how many nodes you can have.

Systems are available that connect the elements through crossbar switches. The C240 computer from Convex, for example, connects four tightly coupled processors to a global memory through a crossbar switch constructed on an 800M-byte/sec bus. Although there's no physical limitation on how many processors you can connect in this manner, the cost for a large number of switches can become prohibitive. System configurations that have a PE and a portion of the global memory at each of the N nodes require a crossbar switch that has $N^2$ switch points. To date, commercially available systems that use crossbar switches have been limited to less than 20 nodes.



*The Multimax 310 is a shared-memory system* with two to 10 processing elements. The system supplied by Encore computer delivers from 4 to 20 MIPs.

A butterfly switch is a practical alternative to the crossbar switch for increasing the nodes in the system. The number of switch points required for a butterfly switch is $Nlog_4N$. Because this function increases more slowly as you increase N than does the square function, it's a more economical switching method for connecting a large number of nodes. BBN's Butterfly GP1000 computer is an example of a shared-memory system connected by a butterfly switch.

The butterfly switch resembles the butterfly operation found in FFT calculations. The GP1000 computer can have one to 256 nodes connected through a butterfly-switch network. Each of the coarse-grained nodes contains 4M bytes of memory. Each node has a Motorola 68020 µP for a PE, a bit-slice µP that acts as a memory controller, and a memory-management unit (MMU) that translates a virtual address into a physical address.

Parallel-processing architectures can be characterized by three interconnected factors: topology, granularity, and synchronization.
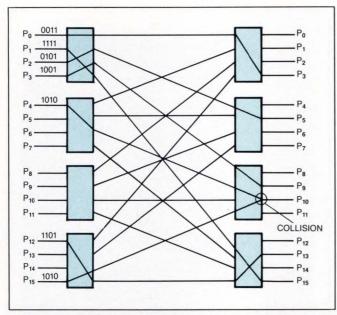


*Fig 1—This block diagram shows a 16-node butterfly switch (organized as eight 4×4 switches) that decodes addresses for routing data. The diagram shows a collision occuring between two packets at node $P_{10}$. (Courtesy Intertext Publications)*

When one of the PEs in the GP1000 computer references a virtual address, the memory controller interprets it to see if the memory location is local or remote. If it's local, the MMU translates it to the local physical memory location. If it's remote, the memory controller packages a remote node address and a remote physical address location into the address word being sent to the butterfly switch. The butterfly-switch elements are custom ICs that can interpret the remote-node address bits.

The butterfly switch decodes the address bits by using packet-switching techniques to create a path through the switch to the remote node (**Fig 1**). If multiple messages collide, the system creates redundant paths to transmit the messages. The extra switching overhead makes the system less tightly coupled than the high-speed bus architecture. The bandwidth of the switch interface is 4M bytes/sec for each node; a 256-element system can deliver 250-MIPS performance.

### Distributed-memory systems use message passing

Loosely coupled architectures have the greatest range of granularity. You can scale coarse-grained distributed-memory systems to a large number of nodes containing lots of computational power and dedicated memory. Array processors and pipeline processors have specialized processors at each node with
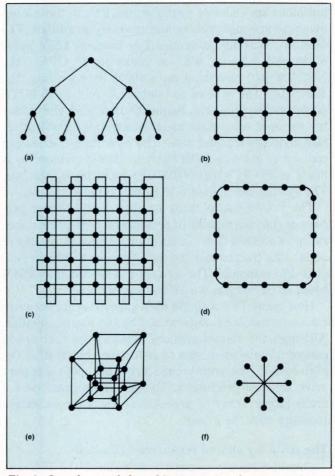


*Fig 2—Loosely coupled architectures can have a variety of topologies, such as a tree network (often used in sorting algorithms) (**a**), a 2-dimensional mesh (**b**), a torus (**c**), a ring connection (**d**), a 4-dimensional hypercube (**e**), and a star connection (**f**).*

very little or no memory. These fine-grained parallel machines must be attached to a central processor. They all have one thing in common, however: Communications take place via message passing.

The loosely coupled architectures can be connected in a variety of ways to fit particular applications that are implicitly parallel (**Fig 2**). Messages passing among processors that aren't directly connected to each other must pass through intermediate processors. Because a processor can pass messages more quickly to its neighbors than to a processor that's not connected to it, you'll want to implement an interconnection scheme that minimizes the number of intermediate processors. The n-dimensional hypercube is such a scheme.

An n-dimensional hypercube computer has N processors interconnected as an n-dimensional binary cube, where $N = 2^n$. You can map the nodes for all
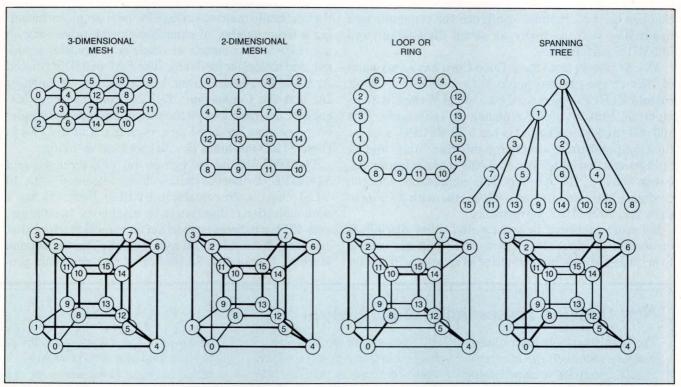
*Fig 3—The flexibility of a hypercube computer lets the programmer choose different topologies for different applications. For example, by using number coding, you can treat a 16-node hypercube as a 3-dimensional mesh, a 2-dimensional mesh, a ring, or a tree.*

dimensional meshes and trees to the nodes of the hypercube, so that communications occur only between neighboring nodes. By number-coding each node, you can map the implicit parallelism of an application to the hypercube with minimum communication overhead (Fig 3). It is this feature that makes the hypercube a good candidate for large-scale general-purpose parallel processing.

The Transputer is an example of a PE that can be readily connected as a 4-dimensional hypercube. Inmos developed the Transputer as a processor for loosely coupled parallel processing. The T800 has a 32-bit CPU, a 64-bit floating-point unit, 4k bytes of on-chip RAM, a 32-bit external memory interface, and four bidirectional serial communication links. The four links allow you to construct a 16-node, 4-dimensional hypercube.

Meiko's Computing Surface computer uses the T800 as a PE at each node. The mainframe has a high-speed backplane that houses a number of computing boards with different degrees of granularity. A board with four PEs can have from 256k to 8M bytes of memory per PE; one with two PEs can have 16M bytes of memory per PE; and one with one PE can have 48M bytes. The four data links, which can transmit data at 5M, 10M, or 20M bps, are sent to an electronic telephone exchange network. The user can arrange the topology of the network to suit the explicit parallelism of a particular application.

A local host, such as a VAX or Sun computer or one of the PEs, builds a physical map of the entire Computing Surface computer for the particular problem. The host supervises the network topology under software control, manages the I/O interfaces and coordinates the program by sending different tasks to each node. A task scheduler at each node monitors all incoming messages to determine whether the task is to be performed at this node. If so, the task is buffered and queued for work; otherwise, the scheduler forwards the task to the next node. When a task is complete, the scheduler forwards the task to the host as a result.

Intel's iPSC/2 family and the NCube/10 hypercube are examples of loosely coupled MIMD computers capable of hypercubes with dimensions greater than 4. The iPSC/2 family has a maximum of 128 coarse-grain nodes with an 80386 CPU, an 80387 coprocessor, and as much as 16M bytes of memory at each node. A direct-connect routing network permits messages to be passed at 2.8M bytes/sec over eight bidirectional links. This combina-

The most tightly coupled topology for a parallel machine is to connect multiple PEs to a shared memory via a single high-speed bus.

tion lets the programmer configure the computer as a hypercube with as many as seven dimensions and 512-MIPS performance.

The NCube/10 from the NCube Corp has a maximum of 1024 coarse-grained nodes with a VAX-like, 32-bit custom VLSI chip and six dynamic-RAM chips with as much as 512k bytes of memory at each node. The 160,000-transistor VLSI chip has a 32-bit CPU, a 64-bit floating-point unit, a memory-interface unit, and 11 bidirectional serial I/O channels for communication between nodes at 1M byte/sec. This combination lets you configure the computer as a hypercube with 10 dimensions and 2000-MIPS performance.

So many problems in science and other disciplines involve the manipulation of arrays that it seems natural to arrange the PEs in a computer as an array. Problems

that naturally map into arrays include: problems including a large number of equations, image processing on the row×column matrix of pixels on a graphics terminal, and molecular modeling. The DAP 510 (Distributed Array of Processors) from Active Memory Technology Inc and the Connection Machine from Thinking Machines Corp have a large number of fine-grained single-bit processors arranged as arrays. Each of the PEs in these SIMD machines has its own local memory.

The DAP 510 has 1024 single-bit PEs arranged as a 32×32-PE, 2-dimensional mesh implemented with 16 VLSI chips, each containing 64 PEs. Each PE has a communication connection to its neighbors. In addition, each PE has a direct connection to its local memory that can range from 32k to 1M byte per PE. The Connection Machine has 16,384; 32,768; or 65,536 single-bit pro-

## New thinking revises limits of parallelism

The highly scalable distributed-memory architectures offer the greatest promise of approaching the ideal parallel-processing machine. In the ideal parallel-processing machine, each process runs in parallel, and the processes don't communicate with one another. Also, the ideal par-

allel-processing machine can have an infinite number of processes running in parallel, and for each added PE there should be a linear increase in processing speed. In practice, however, each process must be capable of some interprocess communication so that the tasks can be synchronized to the overall program. Eugene Amdahl proposed

his now-famous law back in 1967 to show that the serial communication between tasks places an upper limit on how many processors can be used efficiently in a system (**Ref 1**).

Amdahl's argument runs like this: Certain portions of a fixed-sized problem running on a uniprocessor can be run in parallel on a parallel machine, and some



*Fig A—According to Amdahl's law, the speed-up factor of a fixed-size problem running on a parallel-processing machine is eventually limited by the communication time between processors. (Courtesy Sandia National Laboratories)*
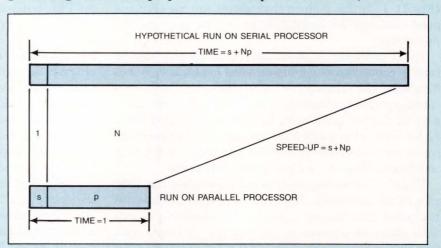


*Fig B—For a problem with a fixed run time running on a parallel-processing computer, the speed-up continues to increase as you add processing elements. (Courtesy Sandia National Laboratories)*

cessing elements arranged as 14-, 15-, or 16-dimensional hypercubes. A router allows data to be sent among any PEs in the system. Each PE has 4k bytes of local memory that is upgradable to 64k bytes. These SIMD machines connect to a host computer that sends a single instruction to be performed on the data at each PE.

### A pipeline runs parallel problems in series

Some classes of problems exhibit a sequence of steps whose execution can be overlapped in the fashion of a pipeline. In a pipeline processor, the execution unit consists of a number of stages that perform a function within a specified time period. Each stage routes its data to the succeeding stage in a serial fashion. The pipeline decreases the overall execution time by overlapping the execution time for each stage. Because data from each stage can only be transferred after the slowest task is complete, efficient pipelining requires that the execution time be evenly balanced between stages. The granularity at each stage can be moderate to fine.

The Pipe System from Aspex Inc is a pipeline processor that has as many as eight stages for low-level image processing. Low-level processing consists of finding the features in raw images—such as edges, texture, and the direction and velocity of motion. The tasks consist of performing repetitive processes on a regular data structure, so they lend themselves to a pipeline. The stages in the pipeline have a feedforward pathway, a pathway for each stage back to its input, a pathway from each stage back to the previous stage, and six video buses that can transfer data to any combination of

portions must run serially to coordinate the overall activity. Let s represent the portion of the time spent in serial communication and let p represent the time for parallel operation. For algebraic simplicity, set the total program run time to unity so that $s+p=1$ (**Fig A**). If the parallel portion of the program is divided over N number of PEs, the run time on a parallel machine is $s+p/N$. Therefore, the speed-up factor (the ratio of the time taken on a uniprocessor machine to that of a parallel machine) for running a fixed-sized problem on a parallel machine is:

$$\text{speed-up}=1/(s+p/N)$$

As the program is scaled over more PEs, the speed-up is asymptotically limited to 1/s and, therefore, the serial component places a limit on the efficiency of a parallel machine.

Sandia National Laboratories has recently published a differ-ent view of the scaleability issues (**Ref 2**). Working on an NCube/10 hypercube machine with 1024 PEs, the laboratory observed that problems running on a more powerful machine generally expanded to make use of the increased facilities. Users could adjust such parameters as the number of time steps, the grid resolution, and the complexity of difference operators to allow the program to run in a desired amount of time.

The speed-up factor, the lab concluded, should be calculated on the basis of constant run time, not constant problem size. It could well be that the newly scaled problem can't run on a serial processor, because of insufficient memory. Instead of asking how long it would take to run a fixed-sized serial problem on a parallel machine, you should ask how long the newly-scaled parallel problem will take on a serial machine.

**Fig B** shows the speed-up of a problem that's scaled for a constant run time on a parallel machine. The run time on the parallel machine is set to unity $(s+p=1)$. The time to run the same scaled problem on a serial machine is $s+Np$. The speed-up factor, therefore, is $s+Np$, which increases continually as more PEs are added to the system.

### References

1. Amdahl, G M, "Validity of the single processor approach to achieving large scale computing capabilities," *Proceedings of the AFIPS Computing Conference*, Volume 30, 1967.
2. Gustafson, John L, Garsy R Montry, and Robert E Benner, "Development of parallel methods for a 1024-processor hypercube," *SIAM Journal on Scientific and Statistical Computing*, Volume 9, No 4, July 1988.

Loosely coupled architectures can be connected in a variety of topologies to fit the implicit parallelism of a particular application.
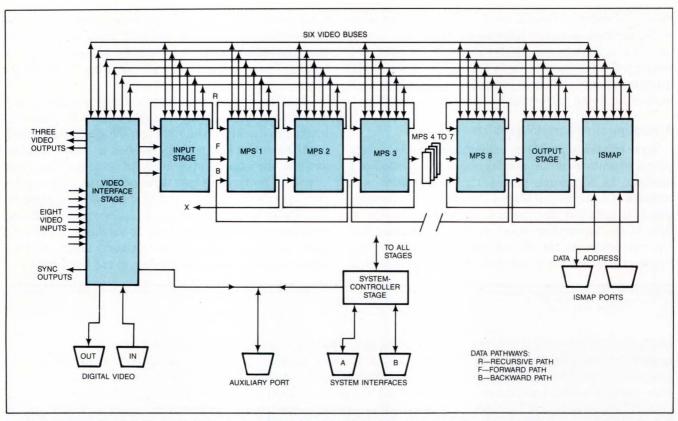


*Fig 4—This block diagram shows the eight pipeline stages found in the Pipe/800 from Aspex Inc. The pipeline can transmit data through three data pathways and six video buses.*

other stages. **Fig 4** shows a block diagram of the Pipe 1/800. Each stage is controlled by a 256-bit word which can be downloaded from an IBM PC/AT computer or a more-powerful host.

Data-flow architectures are unique MIMD parallel machines in that a sequence of data—not instructions—controls the execution of the machine. The Cydra 5 from Cydrome computers is a commercial example of a data-flow computer; for the most part, however, these machines are still in the research stage at various universities. The underlying principle behind these machines is that they operate on data when it becomes available. Data flows from one instruction to another, and the order of execution does not depend on the location of the instruction in memory.

The basic data-flow computer architecture consists of a circular pipeline **(Fig 5)**. Program graphs define the data-flow operations. The graphs consist of links and actors that perform an operation when the operands (called tokens) are present on the links **(Fig 6)**. When an actor completes its operation, it produces a new token. Each newly generated token is assigned an

operation, some control information, and destination information. The newly created tokens are sent to a matching network, which gathers the tokens for a particular operation. When all the tokens for a particular operation are present, they go to the next available PE for processing. You can design the data-flow machine to be tightly or loosely coupled and to have fine- to coarse-grained PEs.

### Take a systematic approach to parallel design

Although the hardware architecture for a parallel machine is largely an issue of topology and granularity, program synchronization and control is primarily a software issue. The software must contain primitives that coordinate the tasks and must provide locks to ensure that a resource is used only for one process at a time.

Locks are necessary in a parallel machine. When more than one PE operates on a data structure, the possibility that two processes can simultaneously access the same data can cause erroneous results. Consider two processes, running in parallel, that must update a

# Glossary of parallel-processing terms

As with most new disciplines, parallel computing introduces a number of new terms to the computing lexicon. The following is a list of some specialized terminology used in parallel processing.

**Array processor**—a parallel-processor architecture characterized by a 2-dimensional rectangular grid of processing elements (PEs). Each PE is connected to its neighbors to the north, south, east, and west.

**Butterfly Switch**—a communication switch whose configuration is based on the butterfly operation of an FFT.

**Concurrent execution**—pertains to the simultaneous processing of two or more instructions, as opposed to the sequential execution of the same instructions.

**Crossbar switch**—is a rectangular grid that contains a switch at each of the grid intersections and connections to communicating components along the grid edges.

**Data flow**—is a mode of operation where the availability of data and operands—rather than a series of instructions—controls the execution.

**Distributed memory**—refers to memory that is allocated for use by one of the nodes in a multi-node parallel system.

**Efficiency (of a computer)**—the ratio of the output computational power to its theoretical computational power. In the ideal parallel computer, all computations take place in parallel without communication between processes. Any communication between processes would reduce the overall computational efficiency of the machine.

**Explicit parallelism**—occurs when sections of a program are run in parallel even though the sections aren't naturally parallel.

**Granularity**—the qualitative measure of the computational power of a processing element. A coarse-grained processor has a large amount of computational power while a fine-grained processor has a small amount of computational power.

**Hypercube**—an architecture that results when a cube architecture is extended to more than three dimensions. Each node in an n-dimensional hypercube has n connections to its neighbors.

**Implicit parallelism**—occurs when certain sections of a program run in parallel because of the parallel nature of the sections in the problem.

**Lock**—a mechanism that grants exclusive access of a resource to one of the processing elements.

**Loose coupling**—an interconnection topology characterized by message-passing communication. The processing elements do not share the same address space.

**Multiple Instruction Multiple Data (MIMD)**—a class of computer organization in which several different instructions operate simultaneously on several different data structures within a single computer.

**Pipeline parallelism**—a class of parallelism that operates on the elements in a data structure in stages. In a pipeline, several elements are at various degrees of completion at the same time.

**Processing element (PE)**—is one of a set of processors in a parallel-processing computer.

**Scalability**—refers to how many processing elements a particular architecure can have. Shared-memory schemes are generally restricted to fewer than 50 PEs; a massively parallel machine has over 1000.

**Shared memory**—a global memory scheme for a parallel machine in which each processing element has direct access to all of the memory.

**Single Instruction Multiple Data (SIMD)**—a class of computer organization in which a single instruction operates on several different data elements simultaneously.

**Single Instruction Single Data (SISD)**—is a class of computer organization in which a single instruction operates on one data element during an instruction cycle time.

**Tightly coupled**—an interconnection topology characterized by a shared address space for all the processing elements. Communication takes place on a word-by-word basis.

**Token (in a data-flow machine)**—an operand or data that is waiting to be executed or matched.

**Transportability**—the ability to transport an application from one machine to another. Because of the wide variations in architectures, most applications require some reprogramming when they are transported from one architecture to another.

So many problems in science and other disciplines involve the manipulation of arrays that it seems natural to arrange the PEs in a computer as an array.
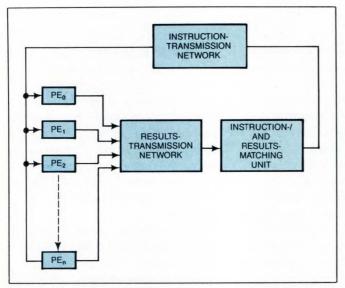


Fig 5—A data-flow machine consists of a circular pipeline in which the results of an operation are sent to a matching unit. The matching unit collects the results assigned to the next instruction. When the data is available, it's sent through a transmission network to the next available PE.



Fig 6—A data-flow graph consists of a number of nodes called "actors," which fire whenever an operand is present. The data-flow diagram shown in b executes the code shown in a. (Courtesy Intertext Publications)

universal counter after the completion of a task. Each process must execute the following pseudo-machine instructions at the end of each task:

```
LOAD        COUNTER
ADD         1
STORE       COUNTER
```

The following interleave of instructions for two simultaneous processes places the wrong value in the counter:

```
LOAD        COUNTER        (PROCESS 1)
LOAD        COUNTER        (PROCESS 2)
ADD         1              (PROCESS 2)
STORE       COUNTER        (PROCESS 2)
ADD         1              (PROCESS 1)
STORE       COUNTER        (PROCESS 2)
```

Parallel machines, therefore, require some method of mutual exclusion to avoid these critical sections in a program. One method is the use of semaphores. A simple Boolean semaphore is an integer variable that can only take the value 0 or 1. A P operation causes the semaphore to decrease by 1, providing it's not already 0. A V operation causes the semaphore to increase by 1, providing it's not already 1.

The programmer ensures the mutual exclusion of a critical section in the program by bracketing it with P and V primitives. When a process enters a critical section, it monitors whether the semaphore is a 1 or a 0. If it's a 1, the process sets the semaphore to 0 to lock out the other processes. When the critical section is completed, it sets the semaphore to 1. If the semaphore is initially 0, the process must continually sample the semaphore until another process resets it to a 1. A process must spin on a small section of code while it's locked out; this operation is called spin locking.

## Go till you get to the end and then stop

Synchronization of processes in a parallel machine takes place primarily through message-passing primitives in high-level languages. Although you can obtain compilers that can detect some implicit parallelism in a serial program, these compilers usually don't provide maximum efficiency for every application. Generally, a programmer must recognize portions of a program to run in parallel and insert message-passing primitives so that the machine can reach maximum efficiency. Essentially, processes pass messages to each other when they wish to communicate.

In 1978, C A R Hoare proposed an experimental parallel language called Communicating Sequential Processes (CSP), which is the basis of many of today's high-level parallel languages. For example, a process called SENDER might send information to the process

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---

RECEIVER by executing an output command in the form

$$\text{RECEIVER ! LINK (expression)},$$

where "!" indicates output and LINK identifies the type of message being sent. The process RECEIVER enters information from the process SENDER in the program by executing an input command in the form

$$\text{SENDER ? LINK (variables)},$$

where "?" indicates input and the variables receive the data being sent.

Occam, a parallel-programming language developed by Inmos for the Transputer, is based on CSP. Occam contains primitives such as "par," which indicates that the following statements should be performed on parallel PEs, and "alt," which can send a message to several alternative processes. Ada, Modula-2, Pascal Plus, and various versions of Fortran for parallel processors have similar constructs for synchronizing processes.

The stumbling block that has prevented the widespread use of parallel processing has been transportability. Moving existing code from a conventional single-processor machine to a parallel machine or moving code among parallel machines usually requires some reprogramming. A parallel language called Linda, which is currently under investigation at Yale University, may help resolve some of the differences among the many parallel languages.

Linda consists of a few simple primitives that can be added to a standard language such as C or Fortran. To overcome the synchronization constraints of the send and receive operations, the Linda model creates an n-tuple space in memory. Instead of exchanging messages with other processes, a process that wishes to communicate data adds it to the n-tuple space, and a process that needs to receive data searches the space and reads it. For example, the statement

$$\text{out(“P”,5,false)}$$

adds the data "5" and "false" to the tuple with the logical name P. The subsequent execution of the statement

$$\text{in(“P”,int i, bool b)}$$

withdraws the tuple from the space and assigns "i" to

"5" and "b" to "false." The statement

read("P", inti, bool b)

is the same as the "in" statement, except that the tuple remains in the space. Because these primitives are machine independent, you can add them to languages operating on different classes of machines. Linda has been implemented in shared-memory parallel computers such as the Multimax, the Balance Series, and the FX/8, and on distributed-memory computers such as the iPSC hypercube.

### A revolutionary age is dawning

Although the largest variety of parallel-processing structures currently under investigation is for mini-supercomputers, board-level parallel-processing products are available for many popular host computers, such as the IBM PC, the Macintosh, and the Sun family of workstations (**Ref 2**). Most of the boards contain Inmos Transputers. In addition NCube offers an IBM PC/AT board containing as many as four of the VLSI CPU chips that are found in the NCube/10. Many computing professionals believe that parallel processing is the programming wave of the future. These board-level products offer an economical way of trying your hand at parallel-processing computer design. **EDN**

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**CIRCLE NO 120**

# Interactive test-generation software eases complex instrument programming

As computer-controlled test instruments proliferate, so do their various command sets. This ever-increasing conglomeration of differing command mnemonics creates big headaches for test engineers. The E2000A Interactive Test Generator (ITG), a mouse-driven software package that runs on specially equipped IBM PC/ATs and compatible computers as well as on the company's HP 9000 workstations, helps you manage this problem by creating Basic test programs that are independent of the measurement instruments. ITG software drivers, which are tailored to specific instruments, then link the device-independent test program to a particular test system.

At its most basic level, the ITG gives you interactive control over the state of an instrument. The instrument-specific software driver produces a window that appears on your computer's screen (**Fig 1**). When you move a mouse-controlled pointer onto a function box within the instrument window and click the mouse's button, the ITG pops up another window, providing you with all of the possible selections relating to that function. The software sends the appropriate command string to properly configure the instrument when you click the mouse on the desired setting.

The ITG software maintains a copy of the instrument's current state in a state vector. When you are satisfied that the instrument is correctly set up for a particular measurement, you can save the instrument's state in a file on your computer's disk. A test program can then use this file to set the instrument to the proper configura-
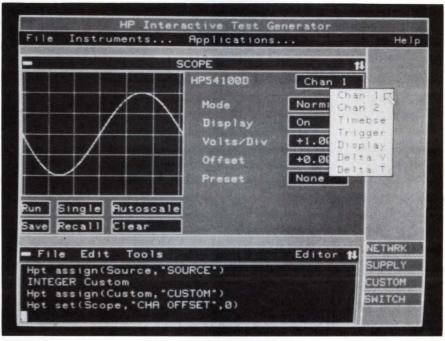


*Fig 1—An on-screen window* allows you to control the state of a computer-controlled test instrument through the Interactive Test Generator's mouse-driven user interface.

tion during a test. Though the initial release of the ITG generates Basic programs, the state-vector files contain ASCII descriptions and can be read by any programming language.

If you must change an instrument's state during a test sequence, the ITG's automatic incremental state-programming feature can reduce program execution time compared with more conventional programming methods. Because the software maintains a copy of the instrument's current state, it can calculate the minimum number of commands necessary to bring the instrument to a new state and send only those commands. This feature shrinks test times because test instruments receive fewer commands to interpret and act upon, and bus traffic between the computer and

the instruments is reduced.

The ITG writes test programs in Basic. Usually, it does not use instrument-specific commands to control the devices in a test system. Instead, the ITG employs a unified set of measurement commands that call instrument-specific software drivers. Thus, you can convert a test program written by the ITG from one multimeter to another, for example, simply by changing the program's instrument-driver specification to the software driver for the new instrument.

In the same manner, you can change a program so that it takes voltage readings with a digital sampling oscilloscope instead of a digital voltmeter. The software drivers mask the differing instrument command sets. If you prefer to use explicit instrument command strings

in your program, you can instruct the ITG to use those strings in conjunction with Basic's "Output" and "Enter" statements.

The ITG runs on IBM PC/AT and compatible machines that are equipped with the company's Basic Language Processor card. In addition, the product works on the company's Model 9000 workstations, running the company's Basic Rev 5.11. For either configuration, the Interactive Test Generator costs $995. The E2001A, a bundle of all available ITG software drivers, costs $495. The initial release of the driver package contains approximately 20 drivers for IEEE-488-based instruments. The company plans to add more drivers for additional IEEE-488 devices and for modules based on the VXI instrumentation bus. Through February 28, 1989, you can order both the ITG and the software drivers for $995.—*Steven H Leibson*

*Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office. TWX 910-373-1267.*

**Circle No 711**

# Graphics processor upgrades TMS34010, maintains software compatibility
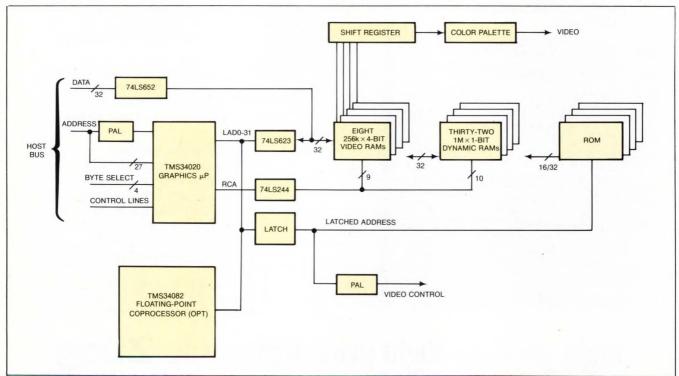
The TMS34020 graphics processor performs floating-point calculations, software graphics primitives, and software windowing three to 20 times faster than its predecessor, the first-generation TMS34010 chip. The 34020 has a 32-bit data bus and a 512-byte instruction cache. (The 34010 had a 16-bit external data bus and a 256-byte instruction cache.) Object code developed for the 34010 is upwardly compatible with the 34020.

Although it still lacks on-chip floating-point hardware, the 34020 can make use of the manufacturer's TMS34082 floating-point math coprocessor to accelerate graphics functions such as coordinate transformations. Such hardware floating-point capability will become in-creasingly important in graphics applications because of the trend toward using world coordinates (coordinates that are not specific to any particular graphics adapter) in graphics-application software. Integer arithmetic alone is usually sufficient for programming with screen coordinates (coordinates that are specific to a particular display resolution), but graphics-application software developers are increasingly using world coordinates to create general-purpose software interfaces. When you program with world coordinates, you'll require many transformations, so you'll need a chip, such as the 34082, that has fast floating-point capability. The 34082 operates at 40M flops and interfaces directly to the 34020's data and address buses. You can connect as many as eight 34082 chips to each 34020.

The 34020 has 25% more microcode than the 34010, reflecting the greater number of graphics primitives the 34020 implements in hardware. For example, the chip now performs trapezoidal and seed fills in hardware. In addition, the microcode now supports 3-operand and 2-operand pixel block transfers (PixBlts), which are arithmetic BitBlts, or bit-block transfers. In a 2-operand PixBlt, for example, the first operand is ANDed with the second, and the result is stored in place of the second. In a 3-operand PixBlt, the first operand is ANDed with the second and is stored in a third place. Keep in mind that if



You can use the TMS34020 graphics processor to perform all the graphics processing for this 1024 × 1024 × 8-pixel display controller; for applications that require intensive numerical processing, you can gain speed by adding a TMS34082 floating-point unit.

EDN September 1, 1988

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# UPDATE

you need to customize any hardware primitives, you still have the option of writing your own graphics functions.

The 34020 supports window clipping/picking, which is the removal of line segments or display elements that lie outside a window's boundaries. The 34010 was slower at windowing than graphics coprocessors, such as Intel's 82786, that are optimized for hardware windowing. The 34020's window-clipping/picking capability gives the chip windowing speeds that are competitive with coprocessors that have hardware windowing capabilities.

The 34020 can take advantage of the manufacturer's 1M-bit video RAM, the TMS44C251. The manufacturer claims the 34020 is the only processor that can use the video RAM's block-write, write-per-bit, enhanced-page-mode, and split-register-reload functions. (For definitions of these terms, see "1M-bit video RAMs offer speed for high-resolution graphics displays," EDN, March 31, 1988, page 79.)

The 34020 comes in a 144-pin pin-grid array (PGA). Samples will be available in the fourth quarter of 1988 for $500; you can expect the price to drop by an order of magnitude within 18 months. Samples of the 34082 will also cost $500, but that price will probably not drop as far or as fast.—*Margery S Conner*

*Texas Instruments Inc, Box 809066, Dallas, TX 75380. Phone (800) 232-3200 ext 700.*

**Circle No 712**

# PRODUCT UPDATE

## Multibus I 32-bit CPU card hosts a 33-MHz 68030 μP

With the introduction of the SM31 board, users of Multibus I systems can upgrade their systems to use the 68030 μP. The card includes either a 20- or 33-MHz CPU and a 68882 math coprocessor. And, it features a 32-bit extension to the Multibus I standard, called Multiplus, which it implements on unassigned P2 connector contacts.

Another feature of the single-board computer is a SCSI port that is capable of synchronous operation at 4M bytes/sec. The card hosts a minimum of 4M bytes of dynamic RAM, but you can expand the memory bank to 40M bytes via a local bus. It also includes 2M bytes of EPROM and five 16-bit timers.

Although the 68030 has an on-chip MMU based on a descriptor cache, the SM31 board includes a custom MMU compatible with the SUN (Stanford University Network) MMU. The SUN MMU features a 256M-byte address range and 64,000 descriptors, and it is suitable for applications that require frequent switching between a large number of tasks.
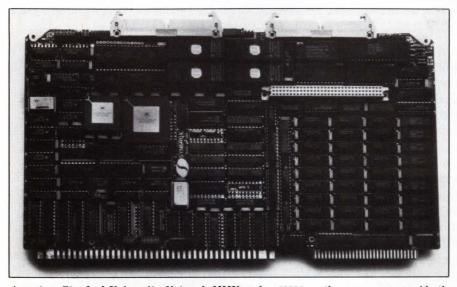
You can add extra functions to the single-board computer using daughter cards. Available add-on modules, for example, include a 20M-flops math processor, a $1660 \times 1280$-pixel video controller, an Ethernet interface, and a keyboard and mouse interface.

Multiplus offers full compatibility with the original Multibus I specification. The extension provides dynamic bus sizing, burst-data transfers, and a maximum data-transfer rate of 40M bytes/sec.

For software development, you can choose from the Unix, OS-9, and PDOS operating systems. In addition, the board includes a Forth interpreter and a monitor program in firmware. Configured with a 20-MHz processor and 4M bytes of RAM, the board costs $4575 (100).—*Maury Wright*

*Synergy Microsystems, 179 Calle-Magdalena, Encinitas, CA 92024. Phone (619) 753-2191.*

**Circle No 713**



*A custom Stanford University Network MMU and a 68882 math coprocessor provide the 68030-based SM31 Multibus I board with the power to execute workstation-class software.*
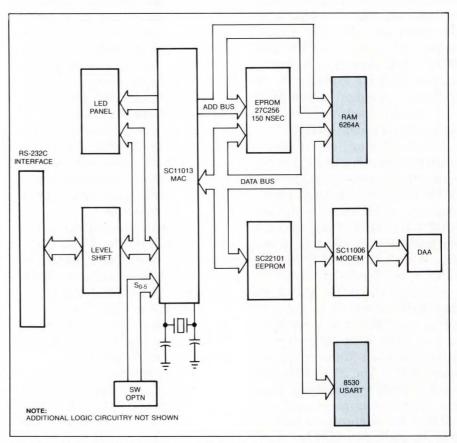
# Modem processor implements networking protocol for error-free communication

If you're including a 2400-bps modem in a design, consider implementing the Microcom Networking Protocol (MNP) along with the modem. The MNP provides full-duplex, error-free communication over phone lines. The SC11013/SC11006 chip set implements the MNP for you. By using the chip set, in effect, you'll be able to build a modem that implements the MNP for less than $11 over the cost of producing a standard 2400-bps modem.

When sending instrument data or new software versions that update equipment in the field, you need error-free data. Slipped digits in data or in programs can cause expensive problems. As a result, you'll need a protocol that checks data at the receiving end. Often, block-transmission protocols similar to Xmodem or Kermit can provide the solution. With this method, the modem sends data in blocks with headers that describe the blocks and contain error-checking information. The error-ridden block gets retransmitted until no errors surface. Unfortunately, both receiving and transmitting systems have to run the same program.

With the MNP, the entire transmission service is performed by the modem at each system. This approach removes the need for each system to run the same protocol program. You can then connect any system to a modem and automatically send error-free data. In addition, the protocol compresses data, offering rates to 2900 bps with a 2400-bps modem. Other software-driven protocols transmit at less than 2400 bps because of block-header overhead.



*By adding some additional components* (shaded) to those required for a standard 2400-bps modem, you can implement the Microcom Networking Protocol (MNP) to obtain error-free modem communication.

A modem based on the chip set will provide two modes of operation. The direct mode allows the modem to function as a standard 2400-bps, Hayes-compatible modem. And, in the autoreliable mode, the modem can communicate with modems that don't have the MNP implemented. After the modem-handshake sequence is completed, an answering modem looks for the protocol's characters from the originating modem. If the modem detects the error-correction characters within 8 sec, the MNP begins to control data transmission. If the characters are not detected, the modem makes a normal connection.
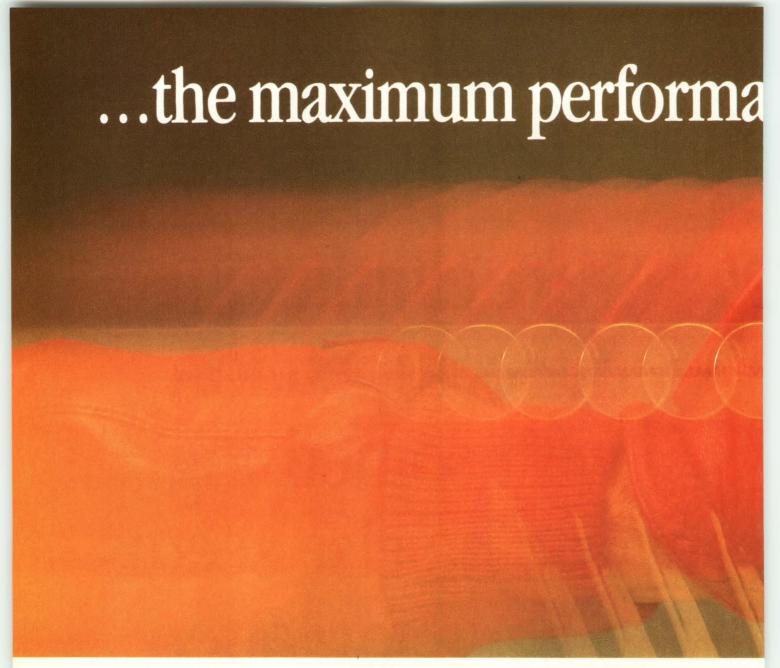
To implement the MNP in a standard modem, you'll need an 8k-word×8-bit static RAM; an 8530-type USART; and 4053, 74HC08, 74LS74, and 74HC27 logic circuits. All the chips required to build a standard 2400-bps modem cost $36 (25,000); with the MNP implemented, they cost $46.85 (25,000). The SC11013/SC11006 chip set alone costs $33.50.—*David Shear*

*Sierra Semiconductor, 20 N Capitol Ave, San Jose, CA. Phone (408) 263-9300. TLX 384467.*

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|---|---|---|---|
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| High voltage | 200MHz | $20\mu m$ | 1 |
| High speed linear | 4.5GHz | $4\mu m$ | 2 |
| High speed digital | 6GHz | $3\mu m$ | 2 |
| Ultra-high speed | 14GHz | $0.6\mu m$ | 3 |

### MOS

| PROCESS FAMILY | fCLOCK | MINIMUM FEATURE | VSUPPLY |
|---|---|---|---|
| KC Industry standard CMOS | 20MHz | $4\mu m$ | 3-10V |
| JG Double SiGate NMOS | 10MHz | $6\mu m$ | 9-18V |
| VB High speed CMOS | 40MHz | $2\mu m$ | 3-5V |
| VJ Very fast CMOS | 50MHz | $1.5\mu m$ | 3-5V |
| VQ Ultra fast CMOS | 75MHz | $1.2\mu$ | 3-5V |

### BIPOLAR (CDI)

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|---|---|---|---|---|---|
| ORIGINAL CDI | $5\mu m$ | | | | |
| CDI FAB I | $3.75\mu m$ | $11.5\mu m$ | 10ns | 2.4pJ | 1.5pJ |
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| Geometry change (utilizing multi-level differential logic-DML) | | | | | |
| CDI FAB IIb | $2.5\mu m$ | $8\mu m$ | 800ps | 0.8pJ | 0.54pJ |
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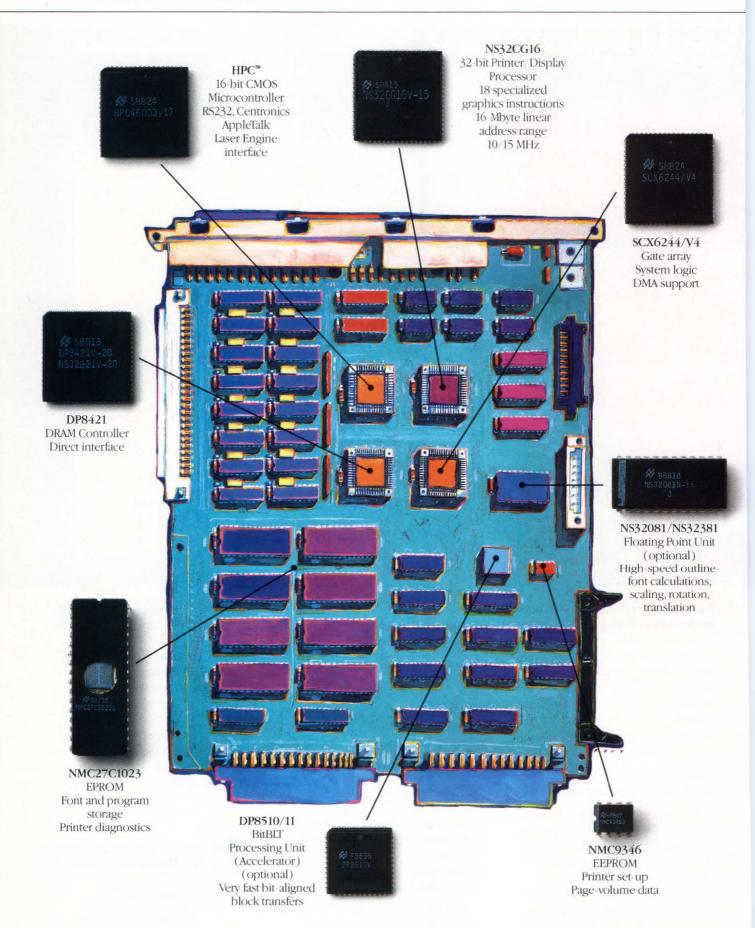
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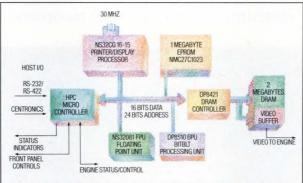
*The NS32CG16 is the heart of a high-performance, cost-effective systems solution for applications like this page-printer controller.*

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- interrupt controllers with timers and parallel I/O ports.

## ALL TOGETHER: THE TOOLS

The NS32CG16 is also supported by a full range of development

tools, available now:
- add-in cards to turn your PC/AT® or compatible into a powerful, multiuser development host
- a full set of language tools, including
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  — optimizing compilers for C, Pascal, FORTRAN 77, and Ada®
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- National's In-System Emulator (ISE™) for complete hardware/software integration
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Not only can virtual instruments simulate many conventional instruments, they can function as unique, specialized instruments as well. Once uniform, easy-to-use software interfaces are introduced, virtual instruments will allow design engineers to export their instrumentation expertise to others.



*Realizing the concept of virtual instrumentation* promises to unleash a whirlwind of products. (Photo courtesy Colorado Data Systems)

# Virtual instruments

Charles H Small, *Associate Editor*

Finally, computer-controlled instruments on a card that connect to industry-standard backplanes are emerging. Combining these instruments on a card with powerful, low-cost personal computers or single-board computers, design engineers will now be able to create virtual instrumentation. Although the capability for producing virtual instruments has existed for many years, previous attempts generally failed to gain widespread acceptance because of the high cost of the hardware and the lack of easy-to-use software. Realizing the concept of virtual instrumentation promises to not only automate the design engineer's measurement tasks, but also to allow him to export his instrumentation expertise far beyond the narrow confines of his lab. Unfortunately, though the hardware is now affordable, the available software still leaves something to be desired.

### The promise of virtual instrumentation

Virtual instrumentation borrows its name from the computer engineer's lexicon. In computerese, virtual contrasts with physical, real, or logical (which is not to say that "virtual" equates with "spiritual," "unreal," or "illogical"). All engineers are familiar with real instruments: They come in cases and have front-panel controls that can be manipulated directly.

Engineers use virtual instruments, on the other hand, much like a programmer uses virtual memory. The computer's hardware allows the programmer to read and write to virtual memory at will, using a single set of commands, regardless of where the computer actually stores the data. The programmer doesn't care if his data resides in CPU registers, cache memory, main memory, or off-line storage.

Similarly, an engineer using virtual instrumentation works with a uniform software interface—perhaps a simulated front panel displayed on a CRT—to set up the instrument, capture and analyze data, and display or record readings. If you have multiple instruments in one system, the software can also oversee cross-triggering and stimulus-response coordination.
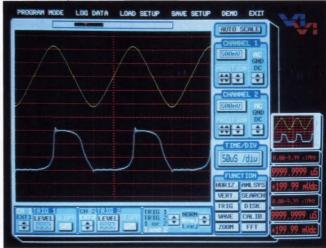
The physical instruments that the software drives *could*, strictly speaking, take many forms. They could be general-purpose, high-speed digitizers backed by appropriate analysis software; they could be stand-alone IEEE-488 instruments; or they could be instruments on a card plugged into the computer's backplane or a special instrumentation chassis.

The high-speed digitizer will serve to illustrate the concept of virtual instrumentation quite clearly. The analysis software can mimic several classical real instruments by reducing the same set of captured data in different ways. For example, by simply scaling and displaying the data points, the virtual instrument can function as an oscilloscope, or, by performing an FFT on the data, it can duplicate the working of a spectrum analyzer.

### ATE spawns virtual instrumentation

Although virtual instruments will undoubtedly have a great effect on design engineers, the impetus behind virtual instrumentation is coming from the ATE com-

Virtual instruments have as yet failed to gain widespread acceptance because of the high cost of hardware and the lack of easy-to-use software.

*The control software for* Virtual Instrument's $2995 virtual CAT multifunction instrument, which plugs into an IBM PC/AT, provides *virtual front panels for an oscilloscope, function generator, frequency counter, and DMM.*

munity. Two broad trends in electronics underlie the new virtual instruments based on instruments on a card, and ATE users are embracing both of these: powerful μP-based personal and single-board computers and advances in electronics miniaturization.

The ATE community has always tried to incorporate each emerging class of computer—mainframe, mini, scientific desktop, board-level, and personal—into its ATE systems. Lately, the ATE industry has been taking advantage of newer, more powerful personal computers and board-level computers as instrument controllers to replace the more-expensive scientific desktop computers and minicomputers. Also, advances in ASIC and surface-mount technology are allowing instrument makers in many cases to put an entire instrument on a single card. These two trends have made it possible for ATE makers to assemble low-cost, compact, and powerful test systems as substitutes for the more expensive and cumbersome "rack-and-stack" systems.

### Designers have different goals
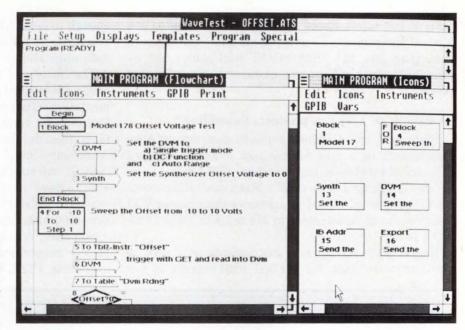
Without question, design engineers will begin to emulate their ATE colleagues and employ virtual-instrument systems based on instruments on a card for automated testing in the design lab. Nevertheless, restricting these devices solely to laboratory ATE is taking too narrow a view of their possible applications. Rather than merely following the ATE community's practice of putting computers into instrument systems, design engineers can now also think of putting virtual

instruments into the computerized systems that they have to design. Moreover, with these instruments on a card and appropriate software, design engineers can capture and then export their instrumentation expertise. The eventual destination of their computerized expertise can conceivably span all phases of electronics, from incoming inspection and prototype testing to manufacturing, field service, and customer use.

After all, to a design engineer, these new instruments on a card that plug into standard backplanes are another type of computer peripheral. The ATE community has done design engineers quite a favor. Perhaps Thomas Carlyle was right. As you may recall, it was the Victorian-era historian who said, "Technologists are little men in black coats who do something important while trying to do something else."

### Digital designers appear receptive

Instrument makers report that digital designers— particularly those who perform computer simulations— are already clamoring for virtual instrumentation. Digital engineers want to use virtual instruments to perform reality checks on their computer simulations. They want to be able to feed data derived from component characterization and prototype testing back into their circuit-design simulations. This data allows the engineers to adjust the fudge factors in their simulations so that the simulator will produce more accurate results in the future. Similarly, design engineers want to import the results of environmental testing, quality control, and field-service repairs to refine their thermal

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│  File  Setup  Displays  Templates  Program  Special                      │
│ Program (READY)                                                      ↑   │
│                                                                      ↓   │
│ ☰          MAIN PROGRAM (Flowchart)           ┐ ☰  MAIN PROGRAM (Icons)┐ │
│  Edit  Icons  Instruments  GPIB  Print          Edit  Icons  Instruments │
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│  │1 Block  │                                    │Model 17│  │R│Sweep th│ │
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│  │2 DVM    │      a) Single trigger mode                                 │
│  │         │      b) DC Function                                         │
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│  ├─────────┤  Set the Synthesizer Offset Voltage to 0  │Synth │ │DVM   │ │
│  │3 Synth  │                                   │ 13   │   │ 14   │       │
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│  │End Block│                                   └──────┘   └──────┘       │
│  ├─────────┤  Sweep the Offset from -10 to 10 Volts                     │
│  │4 For -10│                                   ┌──────┐   ┌──────┐       │
│  │  To  10 │                                   │IB Addr│  │Export│       │
│  │  Step 1 │                                   │ 15   │   │ 16   │       │
│  ├─────────┤  5 To Tbl2-Instr "Offset"         │Send the│ │Send the│     │
│  │6 DVM    │      trigger with GET and read into Dvm └───┘ └──────┘      │
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*Writing test programs with Wavetek's Wavetest test-program generator is a 2-step process. First, you embed an instrument setup in an "icon" using a virtual front panel. Then, you embed the icons in a flow chart. You need not write any lines of conventional program-language code.*

and environmental simulations.

Analog engineers, on the other hand, seem likely to remain satisfied with their existing real instruments. Indeed, certain instruments do not lend themselves to the instrument-on-a-card approach. Instruments based on scan-converter tubes and microwave instruments that use wave-guides, for example, are simply too bulky to fit on a card in a backplane. Such instruments will probably always be packaged in their own enclosures.

Whatever their discipline, all engineers, both analog and digital, could use virtual instruments exactly as they presently use real instruments while developing products in the lab. If virtual and real instruments were merely equivalent, though, design engineers would have no particular reason to switch to virtual



*Virtual instruments such as these from Heath Zenith plug into a chassis that is an extension of the IBM PC/AT bus. The chassis also accommodates the instruments' signal connectors.*

instruments for lab use. Virtual instruments *do* have significant advantages over real instruments, however.

First of all, a virtual-instrument system can learn and remember instrument setups and test procedures. Saving instrument setups benefits not only individual design engineers, but also allows several engineers to share an instrument system more easily because the system can be switched quickly from one engineer's job to another's. Further, an engineer can automate routine or repetitive tests. In some cases, these automated routines can later prove useful to manufacturing, quality-control, and field-service personnel.

And, depending on how well the control software performs its job, virtual instruments can include uniform, easy-to-learn controls so that engineers can use a variety of instruments without having to undergo a tedious learning or relearning period for each device. Lastly, virtual instruments are tightly coupled to a computer, which eases the task of analyzing and reducing data (see **Ref 1** for a roundup of analysis software). Many conventional real instruments, despite having names such as "spectrum analyzer" or "logic analyzer," do not, in fact, analyze anything—they merely capture and display data.

At present three classes of instruments on a card exist. These plug into, respectively, proprietary buses, personal-computer buses, and industry-standard instrumentation buses. Proprietary instrument-on-a-card buses have been around the longest. Examples are the products that Summation and Colorado Data Sys-

tems (CDS) offer. Rapid Systems, Heath Zenith, and Virtual Instruments Corp make instruments on a card that plug into the IBM PC/AT backplane, but no standardization efforts are underway for PC-based buses.

### Avalanche of VXI Bus products impending

Right now, only CDS and National Instruments have instruments on a card for the new industry-standard VXI instrumentation bus (see box, "VXI Bus standardizes instruments on a card"). Many other instrument makers, however, intend to announce their line of VXI instruments at Autotestcon in Minneapolis, MN, October 4 to 6.

Regrettably, having new instruments on a card as the hardware base for virtual instruments is not enough to ensure that such instruments will be widely accepted. The real key to the acceptance of virtual instrumentation is software.

The history of software for IEEE-488 bus instruments offers some parallels for VXI Bus virtual-instrumentation software and may indeed portend the future. The original version of the IEEE-488 standard did a fairly thorough job of defining its hardware interface. After some initial confusion, which resulted in refinement of the standard, instrument manufacturers were able to develop instruments that complied with the standard's electrical requirements for handshaking, timeouts, interrupts, and response to polls.

Software, on the other hand, was left almost completely unspecified. Engineers found the task of programming IEEE-488 instruments annoying, frustrat-

## VXI Bus standardizes instruments on a card

Both the US Air Force, through its MATE (modular automatic test equipment) program's IAC (instrument on a card) Subcommittee, and engineers, via the IEEE P1155 Committee, are determined to shrink test instruments down until they fit on a single card. Their goal is to make possible smaller, faster, and less-expensive test systems.

Last year, five test-equipment manufacturers, Colorado Data System, Hewlett-Packard, Racal Dana Instruments, Tektronix, and Wavetek, set up the VXI consortium and proposed the VXI Bus as the standard for instruments on a card. The VXI Bus is, literally, an extension of the VME Bus (IEEE 1014). Standard VME Bus cards can plug into a VXI Bus backplane because the VXI Bus is a superset of the VME Bus. Like VME Bus pc boards, VXI Bus pc boards can be Eurocard A or B size and have the P1 and P2, 96-pin connectors. VXI Bus pc boards are also available in the larger C- and D-size boards, which measure approximately 13×9 in. and 13×14 in., respectively.

The D size is a triple-height Eurocard that sports an additional P3 connector. The P3 connector carries high-speed instrumentation signals. These signals include a 100-MHz clock and sync signal, additional power-supply feeds, additional ECL trigger lines, and 24 additional daisy-chained, local-bus lines.

### Wide open spaces

The VXI Bus opens up the VME Bus's card spacing from 0.8 in. to 1.3 in. to allow the VXI Bus pc boards to be individually shielded. You can accommodate 20 VXI Bus boards in a standard 19-in. rack. Unlike the VME Bus spec, the VXI Bus specification dictates allowable levels of noise, EMI, and power dissipation because sensitive instruments need an electrically clean and thermally stable environment.

A VXI Bus system can have as many as 256 devices. A single pc board can contain several devices or a single device can be spread over several pc boards. A system comprises a central-timing pc board (called the slot 0 board) and a maximum of 12 additional pc boards. The slot 0 board usually also has a controlling computer along with the system-timing circuitry.

The VXI Bus device protocols define how the various VXI Bus devices in a system divide up the system's address space. Each device gets a minimum of 64k bytes of address space for control and communication. Simple devices can get by with register commands; more-complicated devices use character strings similar to the existing IEEE-488 instruments' character strings for passing commands and data.
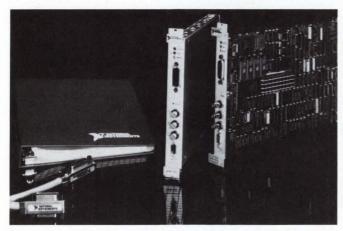
ing, and time consuming. Each instrument had its own pecularities—many of which could be found only by painful trial and error. No uniformity existed for common commands among all instruments or among command sets for a given class of instruments.

For example, many types of instruments have a trigger function that initiates a measurement. The IEEE-488 standard specifies a GET (group execute trigger) command that supposedly simultaneously triggers all instruments linked by an IEEE-488 bus. But some manufacturers programmed their instruments to respond to GET commands by stepping through a sequence of front-panel settings.

System DMMs are another example of a source of confusion. All system DMMs are very much alike, and a knowledgeable instrument user can generally operate an unfamiliar DMM almost immediately merely by inspecting the DMM's front panel. Such is not the case when operating these instruments over the IEEE-488 bus. Each manufacturer's system DMM has its own syntax for command strings.

### Test generators ease pain

Finally instrument makers such as Wavetek, National Instruments, Hewlett-Packard, and Tektronix developed a class of general-purpose IEEE-488 software-development aids that run on common personal computers and, in some cases, on mainframes. (**Ref 2** provides a roundup of existing IEEE-488 software tools. Note that Hewlett-Packard in Loveland, CO, has introduced similar software since the roundup appeared; for information on this product, see the Product
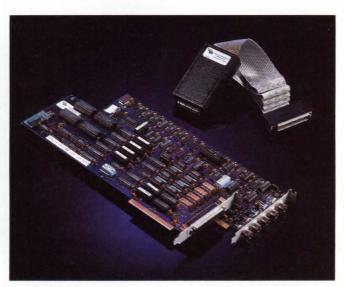
Update on pg 105.) The makers of these software tools, all of whom belong to the VXI consortium (see **box,** "VXI Bus standardizes instruments on a card"), can easily adapt them to other virtual instruments besides IEEE-488 systems—particularly VXI Bus systems which, by design, can use the same command-string techniques as IEEE-488 instruments.

The IEEE-488 bus software tools work on the player-piano principle. To make a piano roll, a master pianist plays a special recording piano whose keyboard mechanism cuts the master roll, or program, as the pianist plays. From then on, untrained musicians can use copies of the master piano roll to play the piano without spending years mastering the intricacies of piano technique. Similarly, the IEEE-488 tools allow an expert to set up programming aids that follow a uniform, easy-to-use format so that less-sophisticated users can operate and program the instrument system painlessly.

Typically the tools offer two general types of programming aids. One, they present the end user with a software simulation of an instrument's front panel, and two, they provide a high-level, pictorial method of structuring programs. To operate the IEEE-488 tools, you first summon a virtual front panel for each instrument you plan to use. With a mouse, or some other graphic-entry tool, you manipulate (sometimes called "mouseing" or "mousageing" in virtual instrumentation jargon) various CRT simulations of knobs, sliders, dials, and pushbuttons to set up the instruments. Then you export these setups to the program-development



*Unlike most VXI Bus instrument makers, National Instruments is not waiting until Autotestcon in October to introduce its first VXI Bus card. The $3000 GPIB-VXI is a slot 0 VXI Bus controller that communicates with the outside world via the IEEE-488 bus.*



*This two-board set for the IBM PC, available from Virtual Instruments Corp, replaces four conventional benchtop instruments.*

tool and structure the sequence in which your test program will use these setups. Some tools can analyze the instrument's captured data; others merely put the data into formats that common data-analysis programs can accept (**Ref 1**).

## Panel conceals detail

Hidden beneath this high-level, graphically oriented software layer is a rat's nest of nitty-gritty detail. The virtual-front-panel software, for example, has to parse your manipulations of the virtual-front-panel controls and translate them into corresponding command strings for a particular instrument. If you were to program such an instrument with a conventional language, you would have to manually compile each command string yourself and insert them into function

calls. Thus, the virtual front panel is, in effect, a subroutine-call generator.

The tools also provide the experienced user with an elaborate set of routines for constructing the virtual-front-panel graphics and linking the graphics to the proper command string. In addition, they provide equally elaborate utilities for formatting the data obtained from the instruments.

## Tools suit ATE users, not designers

As useful and powerful as these IEEE-488 program generators are, they are targeted for ATE users, not design engineers. The tools' goal is to make it easy for a test engineer to concoct a program that an untrained line worker can use repetitively for production testing or incoming inspection.

Design engineers' needs are not exactly congruent with those of ATE engineers. For example, because test engineers doggedly remain faithful to Basic (which many others consider obsolete), most of the IEEE-488 tools use an "enhanced" Basic as a programming language. These test-Basic languages have been extensively enhanced to meet the real-world needs of test engineers. As long as an engineer's purpose is to generate no more than a canned test program, using these tools means no more inconvenience than learning the pecularities of an enhanced Basic.

If, however, you plan to integrate virtual instrumentation with other software-driven peripherals in your computer system or run the machine under some other operating system than DOS, then you will be more

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## Manufacturers of virtual instruments and software

For more information on virtual instruments and software such as those described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

**Colorado Data Systems**
3301 W Hampden Ave, Unit C
Englewood, CO 80110
(303) 762-1640
**Circle No 650**

**Heath Zenith**
Heath Co
Benton Harbor, MI 49022
(616) 982-3200
**Circle No 651**

**Hewlett-Packard**
Measurement Systems Operation
Box 301
Loveland, CO 80539
(303) 667-5000
**Circle No 652**

**Hewlett-Packard**
New Jersey Div
150 Green Pond Rd
Rockaway, NJ 07866
(201) 627-6400
**Circle No 653**

**National Instruments**
12109 Technology Blvd
Austin, TX 78727
(512) 250-9119
FAX (512) 250-0382
TLX 756737
**Circle No 654**

**Rapid Systems**
433 N 34th St
Seattle, WA 98103
(206) 547-8311
FAX (206) 548-0322
TLX 265017
**Circle No 655**

**Summation Inc**
11335 NE 122nd Way
Kirkland, WA 98034
(206) 823-8688
FAX (206) 823-7994
TLX 152219
**Circle No 656**

**Tektronix Inc**
Box 1700
Beaverton, OR 97075
(800) 835-9433
TLX 151754
**Circle No 657**

**Virtual Instrument Corp**
32 Portland Ave
Georgetown, CT 06896
(303) 544-9801
**Circle No 658**

**Wavetek San Diego Inc**
Box 85265
San Diego, CA 92138
(619) 279-2200
**Circle No 659**

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*Test generators such as* HP's Interactive Test Generator can mix *readings from several instruments at once on a single screen.*

likely to program the peripherals in C or Pascal. In this case, the program-generation tools would be of limited utility. You could use them to generate the command strings and subsequently save the strings in a file. Then you could boot your regular program-development software, read the command strings, and insert them in the appropriate subroutine calls.

These tools reveal their ATE orientation in the way they interface with programming languages other than the enhanced Basic versions. They also perhaps indicate what could be a deficiency as far as virtual-instrumentation software for the VXI Bus is concerned. Most of the IEEE-488 software aids can call a library subroutine that you had previously compiled using a different language. But that path cannot easily be reversed—that is, you cannot call a test program generated by the IEEE-488 program-generation tools from a program written in another language. Therefore, unless instrumentation-software vendors integrate their products with common languages and operating systems, such as C and Unix, design engineers will probably devise their own programming schemes for virtual instruments when incorporating these instruments in their designs.

**EDN**

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1. Leibson, Steven H, "Laboratory-automation software," **EDN**, June 9, 1988, pg 114.
2. Harold, Peter H, "Program-generation tools for PCs ease IEEE-488 system integration," **EDN**, April 14, 1988, pg 71.

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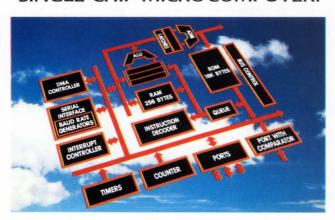
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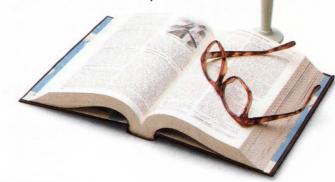


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# No Compromises

# Video op amps find use in RF and active filters

*Video op amps designed for radio frequencies offer relatively high output current and low power consumption in comparison with conventional op amps. They can work well in various high-frequency analog-signal-processing applications, including driving flash converters and active antialiasing filters.*

Ken Schaefer and John Shier, *VTC Inc*

You can use some operational amplifiers designed specifically for RF purposes in several typical high-frequency analog-signal-processing applications. Conventional operational amplifiers are fabricated with slow high-voltage processes differing little from those in use in the late 1960s (**Ref 1**). These conventional amplifiers offer excellent accuracy, large signal swings, moderate output drive capability, and limited frequency response. By comparison, the op amps discussed here are made using a fast process and offer high current outputs. Designed to supply 50 mA of output current, their complementary class AB push-pull output stage uses fast PNP transistors (**Fig 1**). The scaled bipolar linear-IC process provides NPN transistors with $f_t$ of 6 GHz and vertical PNP transistors with $f_t$ of 1.5 GHz.
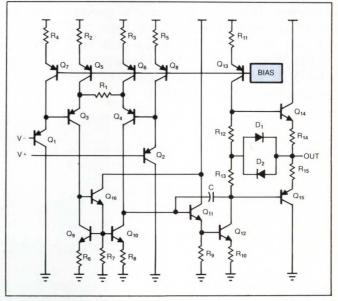


*Fig 1—A simplified schematic for the VA705 video op amp shows the complementary class AB push-pull output stage.*

Although the push-pull output is typical for op amps, it has not previously been available in an RF version because the output transistors in conventional RF amplifiers are not fast enough to track a high-frequency signal throughout its full excursion, as is required for AB operation. In complementary class AB operation, the base bias on the output transistors allows them to operate in their nonlinear region part of the time. The result is lower signal fidelity but also less power con-

*Complementary class AB operation results in lower signal fidelity but also less power consumption.*

sumption. At any given instant one of the output driver transistors $Q_{14}$ and $Q_{15}$ puts out only the actual current needed by the load, without the excess bias current needed in class A amplifiers. Your power requirement can thus decrease dramatically in comparison with the power needed by conventional class A amplifiers built with discrete components.

These video op amps achieve their high frequency by sacrificing the high breakdown voltages that conventional analog ICs offer; the video op amps operate with nominal supply voltages of ±5V, with typical signal swings to ±2.5V. These supply voltages and swings are usually not a serious limitation for RF applications, in which load impedances tend to be low (eg, 50 and 75Ω transmission lines), since the amplifiers are designed to supply ±50 mA output currents.

The basic amplifier is available in seven versions, including a unity-gain compensated version (VA705) and two decompensated versions (VA708; VA707, $A_V$). Also available are dual and quad versions with identical properties. DIP, SOIC, and PLCC packages are offered. For applications requiring more precision, you can use the VA701. Two unity-gain video buffers (VA033, VA003) provide ±100 mA of output current and a 300-MHz bandwidth. The amplifiers' basic parameters are summarized in **Table 1.**
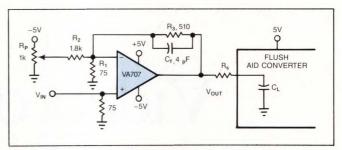


*Fig 2—This video op amp is configured to drive a flash A/D converter. The small element values are characteristic of video circuits, and the VA707 has ample drive capability for these low impedances.*

Three prototype models of these amplifiers illustrate how well they work for RF signals in the 5- to 80-MHz region. Two of these come from the increasingly popular area of video-frequency sampled-data systems; the third example shows how to use them in high-speed instrumentation applications.

### Op amps drive flash converters

CMOS flash A/D converters have become popular building blocks for digitizing video signals. The proper input-signal conditioning for these flash converters requires an input amplifier with enough speed not only to minimize settling time to a given accuracy but also to

**TABLE 1—BASIC PARAMETERS OF VTC OP AMPS AND VIDEO BUFFERS**

| OP AMP MODEL | OPEN-LOOP GAIN (dB) | CLOSED-LOOP GAIN (TYP V/V) | SLEW RATE (V/μSEC) | GAIN BAND-WIDTH (MHz) | OFFSET VOLTAGE (mV) | INPUT BIAS | POWER (mW) |
|---|---|---|---|---|---|---|---|
| VA705 | 80 | UNITY-GAIN STABLE | 35 | 25 | 3 | 650 nA | 75 |
| VA708 | 80 | DECOMPEN-SATED $A_V>3$ | 85 | 100 | 3 | 650 nA | 75 |
| VA707 | 80 | DECOMPEN-SATED $A_V>12$ | 100 | 300 | 3 | 650 nA | 75 |
| VA701 | 120 | PRECISION UNITY-GAIN STABLE | 8 | 30 | 0.05 | 25 nA | 80 |
| VA711 | 120 | DECOMPEN-SATED $A_V>5$ | 30 | 100 | 0.05 | 25 nA | 80 |
| VA033 | 0 | VIDEO BUFFER $A_V=1$ | 2000 | 300 | 8 | 15 μA | 280 |
| VA003 | 0 | VIDEO BUFFER $A_V=1$ | 700 | 300 | 8 | 15 μA | 350 |

(a)

(b)
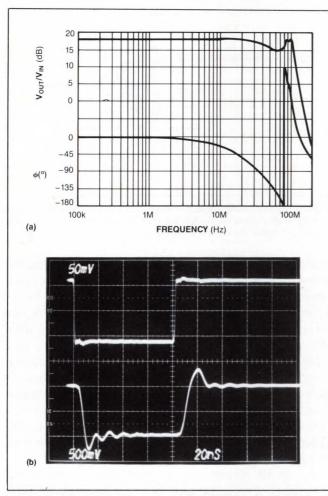
*Fig 3—The Fig 2 circuit was measured without any series damping ($R_S=0$) and with a load capacitance of $C_L= 50$ pf; **a** shows the frequency-domain measurement, and **b** shows the time-domain response.*

minimize harmonic, intermodulation, and phase distortions of the input signal. In general the amplifier should have a bandwidth three to six times that of the video input signal. For video signals, the bandwidth should be within 15 to 30 MHz. The amplifier must also be capable of driving capacitive loads up to 60 pF with no instability problems. Also, some voltage gain is often desirable.

Users of flash converters often find that the input amplifier is the most challenging part of the design. Instead of resorting to an expensive hybrid or discrete design to solve the problem, however, you could use a video op amp (**Fig 2**).

When designing an input amplifier for a flash converter, you usually want to be able to set not only the gain but also the bandwidth to a value that is optimum

for performance specifications such as signal fidelity and antialiasing. For a simple bandwidth adjustment, you could use a plain capacitor with a value of 40 to 60 pF because the input resistance is generally greater than 100 kΩ. For example, you might want to design an amplifier with a gain ($A_V$) equal to 8 (V/V), according to the formula:

$$A_V \approx 1 + \frac{R_3}{R_1 \| \left( R_2 + \dfrac{R_P}{2} \right)}.$$

The summing resistor $R_2$ serves to level-shift the output level to the commonly used flash converter's full-scale input level of 0 to 1V or 2V. Although the VA707 amplifier is specified for gains of 12 V/V or greater, you can use it at lower gain levels by keeping impedance levels small (500Ω) and by using a phase-recovery capacitor ($C_f$) across the feedback resistor.

### Step response reflects large bandwidth

The measured frequency response of the prototype circuit is shown in **Fig 3a**. Here the frequency response shows a 3-dB bandwidth point at 70 MHz with a peak in the 90- to 100-MHz range. The corresponding 1V step response in **Fig 3b** reflects this large bandwidth with a fall time of 4 nsec, while the 90- to 100-MHz peak is seen as ringing in the step response at this same frequency. The rising edge is somewhat slower than the falling edge and also exhibits a larger overshoot because the amplifier is at the edge of the slew-rate limit of about 100 V/μsec.

Assume that a 3-dB bandwidth of 30 MHz has been chosen as suitable for the 5-MHz video signal bandwidth. Because the basic amplifier bandwidth goes far beyond the 30-MHz requirement, you can add a series damping resistor ($R_S$) to the output to set the desired bandwidth. Thus if $f_{-3\ dB}$ is equal to 30 MHz, then $R_S$ equals $1/(2\pi f_{-3\ dB} C_L)$, or 106Ω. The response of the prototype circuit is shown in **Fig 4** with $R_S$ equal to 100Ω. The bandwidth is a flat 30 MHz, and, as expected, the high-frequency ringing has been eliminated. The accumulated phase error in the 5-MHz signal band is less than 25°. Again there is positive overshoot caused by the amplifier being at the edge of its slew-rate limit at 100 V/μsec. For smaller step amplitudes, the positive and negative overshoots are identical and less than 2% (**Fig 5c**). The amplifier's settling time is under 60 nsec.

Antialiasing filters are necessary to maintain base-

*Users of flash converters often find that the input amplifier is the most challenging part of the design.*



(a)

V_OUT/V_IN (dB) vs FREQUENCY (Hz)



(b)



(c)
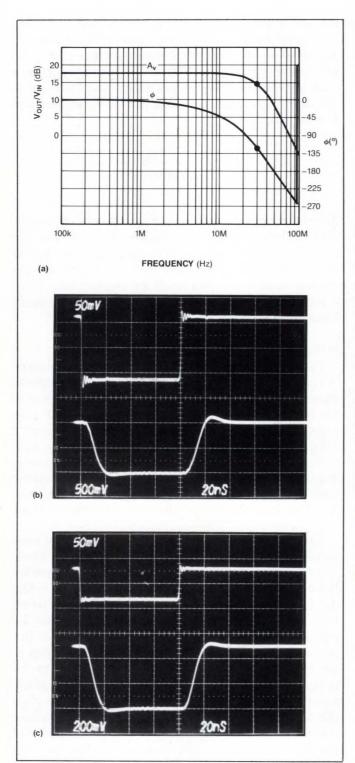
**Fig 4—The Fig 2 circuit was also measured** with series damping ($R_S=100\Omega$) to reduce the bandwidth and a load capacitance of 50 pF. The frequency-domain measurement is in **a**. The 1V step response is in **b**; the 0.5V step response is in **c**.
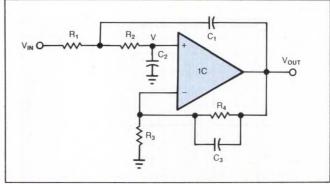


**Fig 5—You can configure the op amp** in this basic 2-pole Sallen-Key amplifier at a fixed noninverting gain, generally from 1 to 3. The equations define the circuit's voltage transfer function.

band signal integrity in any sampled-data system. For video signals, because the critical specification is phase linearity, the filter of choice is generally the Bessel type, which in its ideal form produces a delayed replica of the input signal. However, because a Bessel filter doesn't have the sharp rolloff characteristics of a Chebyshev filter or the passband flatness of a Butterworth type, you may need a filter with more than six poles to meet the passband and/or stopband requirements. A single high-speed quad op amp provides a cost-effective solution to this problem. You can cascade filters with 1, 2, or 3 poles per stage in any combination to produce filters as high as the twelfth order.

Active RC filters are not new; what is new is the possibility of realizing such filters economically at video frequencies. In this example, the prototype implements the Sallen-Key type circuit (or $V_{CVS}$), a popular method for active filters (**Ref 2**). In this type of circuit, you configure the op amp at a fixed noninverting gain, generally from 1 to 3 V/V. **Fig 5** illustrates the basic 2-pole section. The equation defining this circuit is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{K}{R_1 R_2 C_1 C_2}}{s^2 + \left(\dfrac{1}{R_1 C_1} + \dfrac{1}{R_2 C_1} + \dfrac{1}{R_2 C_2} - \dfrac{K}{R_2 C^2}\right)s + \dfrac{1}{R_1 C_1 R_2 C_2}}, (1)$$

where K is the voltage gain of each gain block, given by

$$K = V_{OUT}/V+ = 1 + (R_4/R_3).$$

The noninverting stage should have gain flatness (less than 1 dB) and minimal phase-error accumulation (less than 45°) to well beyond the passband. The degree to which the VA4708 meets these requirements when K

## TABLE 2—NORMALIZED RESISTOR VALUES FOR THE FILTER SECTIONS OF AN 8-POLE BESSEL FILTER

| FILTER SECTION | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | | 2 | | 3 | | 4 | |
| $R_1$ | $R_2$ | $R_1$ | $R_2$ | $R_1$ | $R_2$ | $R_1$ | $R_2$ |
| 0.0892 | 0.350 | 0.176 | 0.117 | 0.114 | 0.241 | 0.0962 | 0.306 |
| $R_1$ | $R_2$ | $R_3$ | $R_4$ | $R_5$ | $R_6$ | $R_7$ | $R_8$ |

equals 2 V/V is shown in **Fig 6**. In the passband, the gain flatness is less than 0.15 dB, and phase-error accumulation is less than 10°. Stopband attenuation starts to soften at 28 MHz, however, because the phase passes through 45° here, and the approximation of K at 2 at 0° is no longer valid (**Fig 6**). The 6-dB peak at 120 MHz is far enough beyond the frequencies of interest to be of only secondary importance.

For this active-filter design, you can simplify **Eq 1** by making K equal to 2 and $C_1$ and $C_2$ both equal to C. Therefore, you have only the resistor values to manipulate to make the circuit act like a Bessel filter.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\left(\frac{2}{R_1 R_2 C^2}\right)}{s^2 + s\left(\frac{1}{R_1 C}\right) + \frac{1}{R_1 R_2 C^2}}.$$

Now you must find resistor values for each stage such that the denominators correspond to the Bessel polynomial, which for an 8-pole filter is:

$$B_n = (s^2 + 11.2s + 32) \times (s^2 + 5.68s + 48.4)$$
$$\times (s^2 + 8.74s + 36.2) \times (s^2 + 10.4s + 34).$$

(**Ref 3**). Thus for each stage:

$$s^2 + bs + c = s^2 + \frac{s}{R_1 C} + \frac{1}{R_1 R_2 C^2}$$

where

$$b = \frac{1}{R_1 C}$$

$$c = \frac{1}{R_1 R_2 C^2}.$$

To solve the equations for $R_1$ and $R_2$, normalize to C=1. Then



(a)

(b)
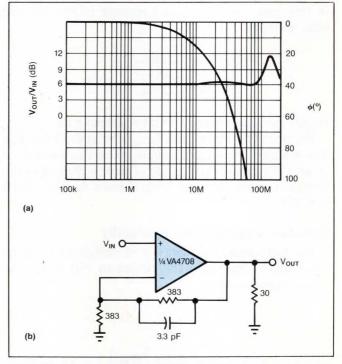
**Fig 6—The frequency response of the VA4708** when the voltage gain is 2 **(a)**. The figure in **b** defines the circuit measured.

$$R_1 = 1/b \quad R_2 = b/c.$$

**Table 2** lists the resultant normalized resistance values for each filter section.

To find the actual component values for the design, multiply the normalized R values ($R_n$) by $1/\omega_0 C$, where $\omega_0$ is the desired bandpass frequency, and C is a value large enough (generally 50 pF) to swamp out package and board parasitics and consistent with keeping resistor values in the range from 50Ω to 1 kΩ (see **Ref 3** for the definition of $\omega_0$). Note that whereas $\omega_0$ for a Butterworth filter defines the −3-dB point independent of degree n, the Bessel filter attentuation at $\omega_0$ decreases from −3 dB at n=1 to fractions of a dB as n gets larger.

For example, with an $F_{-3\text{ dB}}$ bandwidth of 5.5 MHz, calculate R values for the first Bessel section of an eighth-order filter. First, choose a capacitance value of 100 pF (±2%). From the Bessel curves, $f_0$=2 MHz (**Ref 3**). Then:

$$R_1 = \frac{R_n}{2\pi f_0 C}$$

$$= \frac{0.0892}{(6.28)(2 \times 10^6)(10^{-10})}$$

$$= 70.7\Omega.$$

*For video signals, because the critical specification is phase linearity, the filter of choice is generally the Bessel type.*

In this case, choose a 71.5Ω resistor (±1%). By the same method,

$$R_2 = \frac{R_n}{2\pi f_0 C}$$
$$= 277\Omega.$$

In this instance, choose a 281Ω resistor (±1%).

The prototype filter has a $f_{-3\,dB}$ point at 6.5 MHz (**Fig 9a**), which is reasonably close given the sources of error. For example, one source of error is the lack of flatness assumed for gain K=2; K has a peak of 0.2 dB at 6 MHz.

### Calculate input impedance carefully

The filter input impedance is of considerable importance and is based on the circuit in **Fig 8** and the following equations:

$$Z_i = \frac{V_{IN}}{i_i}$$
$$= R_1\left(\frac{V_{IN}}{V_{IN} - V_1}\right)$$
$$V_2 = \frac{V_1}{sCR_2 + 1}$$
$$V_1 = \frac{(sCR_2 + 1)V_{OUT}}{K}.$$

Substituting **Eq 1** for $V_{OUT}$ and letting $\omega_0 = 1/(R_1 R_2 C_2)$ and $s = j\omega$, you obtain, by algebraic manipulation, an
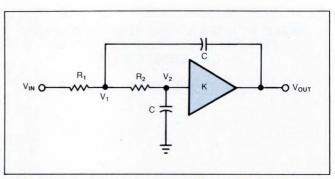


*Fig 8—This circuit of the Sallen-Key filter section relates the basic values used to determine input impedance.*

equation for input impedance:

$$Z_i = (\omega_0/\omega)^2 R_1\left[-(\omega/\omega_0)^2 + j(\omega/\omega_0)\frac{\sqrt{R_1 R_2}}{R_1} + 1\right].$$

You can approximate this equation for various frequency limits (**Table 3**).

**Fig 7** is an example of an 8-pole video Bessel filter using the VA4708 quad op amp. The amplifier contains four cascaded Sallen-Key type 2-pole sections that result in an overall low-frequency gain of 8 V/V (2 V/V per section). The RC products of each section satisfy the coefficients of the Bessel polynomial. The prototype filter has a passband of 6.5 MHz (−3 dB), a group delay of 97 nsec, phase linearity of less than 2.5%, and a stopband rejection of more than 40 dB from 22 to 80 MHz.
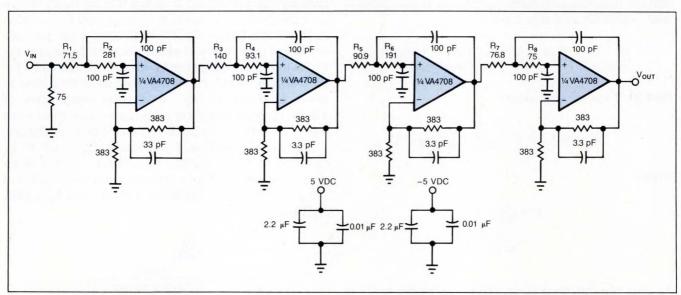


*Fig 7—If you use a video op amp that has cascaded Sallen-Key circuits, you can obtain this 6-MHz, 8-pole low-pass Bessel filter.*

Fig 9 shows the measured response of the prototype for the **Fig 7** circuit. Based on an equivalent input spot noise of 35 nV/$\sqrt{\text{Hz}}$ for each amplifier and a bandwidth of 6 MHz, the dynamic range of the input signal extends from 125 $\mu$V rms to 147 mV rms at 6.5 MHz (1.18V rms at the output) based upon a slew rate of 85 V/$\mu$sec.

You can model the filter's input impedance as a frequency-dependent RC series. Because of the controlled positive feedback of the Sallen-Key amplifier, the R value is actually negative at the passband frequencies. The Smith chart and adjoining table in **Fig 10** show the filter's input impedance with a 75$\Omega$ input-termination resistor. Note that in the passband, although the termination resistor determines the input impedance for the most part, the effective R value goes

## TABLE 3—APPROXIMATING IMPEDANCES FOR VARIOUS FREQUENCIES

| FREQUENCY RANGE | $Z_i$ | RESPONSE |
|---|---|---|
| IN GENERAL: | | |
| LOW FREQUENCIES: $(\omega/\omega_0)^2 \leq 0.1$ | $\approx -(\omega_0/\omega)^2 R_1$ | NEGATIVE RESISTANCE |
| RESONANCE: $\omega = \omega_0$ | $= -j\sqrt{R_1 R_2}$ | CAPACITIVE |
| HIGH FREQUENCIES: $(\omega/\omega_0) \geq 10$ | $\approx R_2$ | POSITIVE RESISTANCE |
| WHEN USING **FIG 8** | | |
| $(f/f_0)^2 = 0.01$ $f = 0.32f_0 = 36$ MHz | $\approx -(f_0/f)^2 R_1$ $\approx -715\Omega$ | |
| $f = f_0 = 11.2$ MH$_z$ | $= -j\sqrt{R_1 R_2}$ $= -j142\Omega^*$ | |
| $(f/f_0)^2 = 10$ $f = 3.2f_0 = 35$ MHz | $\approx R_1$ $\approx 71.5\Omega$ | |

**NOTE**
$^*C_{eff} = 1/2 \pi f_0 X_C$
$= 100$ pF

# High-frequency caveats

One feature of high-frequency circuits not always appreciated by designers of conventional analog ICs is the high level of output current required. To produce useful signal swings, a typical 50 or 75$\Omega$ load draws 20 to 50 mA. The typical load capacitance (measured in tens of picofarads) then draws additional large signal currents. Driving a 50-pF capacitor at 4V p-p, for instance, would require another ±32 mA at least.

Circuit packaging and construction techniques are equally important because parasitic elements can have a decisive effect on RF-circuit behavior. Conventional DIPs, for instance, can behave like lowpass filters and thereby compromise circuit performance for frequencies as low as 50 MHz. Miniature SOIC and LCC packages, however, have reduced parasitics that lead to better RF performance. As an added bonus, the surface-mount boards used with these packages usually permit reduced lead

## TABLE A—TYPICAL PARASITIC ELEMENTS FOR IC PACKAGES*

| INPUT CAPACITANCE (TO ADJACENT PINS AND TO GROUND) | 3 TO 10 pF (DIP) ~1 pF (28-PIN LCC) |
|---|---|
| PIN SELF-INDUCTANCE | 8 TO 25 nH (DIP) ~4 nH (28-PIN LCC) |
| CHIP BONDING-PAD CAPACITANCE | 0.3 TO 0.5 pF |
| CHIP WIRE-BOND INDUCTANCE | 1 TO 2 nH |

*THE VALUES VARY WIDELY FOR A DIP, DEPENDING ON THE PIN POSITION. THE CORNER PINS HAVE SEVERALFOLD MORE CAPACITANCE AND INDUCTANCE—ESPECIALLY FOR BIG DIPs LIKE 40-PIN TYPES.

lengths and smaller foil capacitances.

**Table A** lists the typical parasitic inductance and capacitance found in a DIP and an LCC, plus the bonding-pad capacitance and bond-wire inductance common to both packages. Bear in mind that pin parasitics vary widely with pin position. The corner pins have several times as much capacitance and inductance as the others—particularly for a large 40-pin DIP.

The **Table A** data shows that LC parasitics for the pins of a large DIP can cause resonance at a few hundred megahertz, whereas surface-mount packages offer typical LC resonances at 1 GHz and above. Well below these resonances, however, are the package parasitics that can alter impedance levels, create phase shifts, and cause undesirable peaks in gain. Because even the SOIC and LCC packages can limit signal bandwidth below that inherent in the video-amplifier chip, you must consider hybrid construction for the very highest circuit performance.

*Active RC filters are not new; what is new is the possibility of realizing such filters economically at video frequencies.*

to values larger than 75Ω, which indicates a negative input resistance for the filter itself.

The filter passband extends to video frequencies, and if you are going to keep the capacitor values large enough to minimize parasitic effects, you need resistors that are one to two orders of magnitude smaller than

are customary in active filters. This smaller size causes no power-dissipation problems, however, because the signal levels are generally less than 4V (p-p), and the amplifiers can deliver output currents of only ±50 mA.

You can also use video op amps as quad op amps in standard instrumentation amplifier (IA) configura-
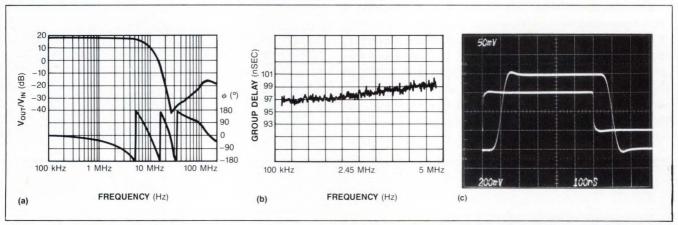


**Fig 9—The prototype filter in Fig 7** was measured for the frequency-domain response, which shows a 3-dB bandwidth of 6.5 MHz and a 40-dB stopband from 22 to 80 MHz **a**; group delay **b**; and time-domain response **c**.



| f (MHz) | R | $X_C$ |
|---|---|---|
| 0.1 | 75 | − 0.15 |
| 0.2 | 75 | − 0.15 |
| 0.4 | 75 | − 0.15 |
| 0.8 | 75 | − 0.30 |
| 1.0 | 76 | − 0.45 |
| 2.0 | 78 | − 1.9 |
| 4.0 | 83 | − 12 |
| 8.0 | 63 | − 33 |
| 10.0 | 52 | − 81 |
| 20.0 | 38 | − 14 |
| 40.0 | 36 | − 4.3 |
| 80.0 | 38 | − 4.3 |
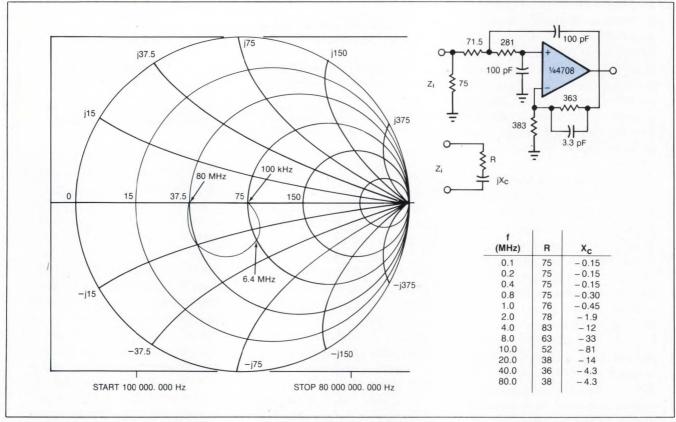
**Fig 10—This Smith chart** and the adjoining table illustrate **Fig 7** filter's input impedance with an input termination resistor of 75 Ω.

*An amplifier that contains four cascaded
Sallen-Key type 2-pole sections results in an
overall low-frequency gain of 8.*
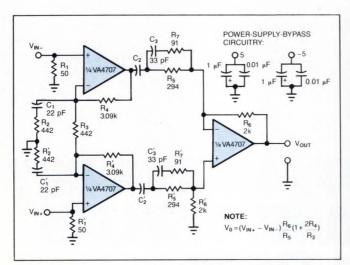
**Fig 11—You can use a quad op amp** to build an instrumentation
amplifier. The amplifier shown is ac-coupled.



**Fig 13—In the instrumentation amplier in Fig 11,** an input signal
of 20 mV (p-p) at 10 MHz is contaminated by 2V (p-p) at common-
mode signal at 1 MHz.



**Fig 12—The ac-coupled** instrumentation amplifier in **Fig 11** shows
this measured frequency response. The small-signal bandwidth is 20
MHz with less than 3 dB of peaking.
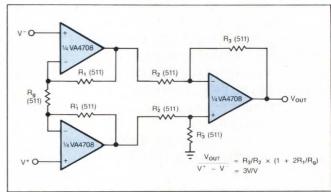


**Fig 14—Using a quad video op amp,** a dc-coupled instrumentation
amplifier can achieve a gain of 3.

tions. Conventional op amps perform this function quite well to the 1-MHz level, at which point operation becomes difficult. Video op amps can extend IA operation to the 10- to 40-MHz range, depending upon the overall gain requirement.

The IA shown in **Fig 11** is designed to yield an overall gain of 100. The small-signal bandwidth (**Fig 12**) is 20 MHz with less than 3 dB of peaking. The power bandwidth with a 3V p-p output signal is 10 MHz. Because of the cascaded nature of the IA, the gain-bandwidth product of 2 GHz extends well beyond that of an individual op amp, which is about 300 MHz.

The circuit in **Fig 11**, uses the $C_1$, $C'_1$, $R_2$, $R'_2$ network to insure input amplifier stability while the lead network $C_3$, $C'_3$, $R_7$, $R'_7$ maximizes the overall

bandwidth. Capacitive coupling $C_2$, $C'_2$ minimizes the output offset voltage to insure the maximum ac dynamic range. The lowest frequency that must be processed determines the $C_2$ value. For example, when $C_2=1$ $\mu F$, then $f_L=\frac{1}{2}\pi R_5 C_2=540$ Hz.

An IA can extract signals embedded in large amounts of common-mode noise. In **Fig 13**, an input signal ($V_{IN+}$ and $V_{IN-}$) of 20 mV (p-p) at 10 MHz is contaminated by 2V (p-p) of common-mode signal at 1 MHz. Since the IA's common-mode rejection is in excess of 60 dB at 1 MHz, the dominant output-signal component is the amplified version of the 10-MHz differential input signal.

The overall gain of the dc-coupled IA in **Fig 14** is 3

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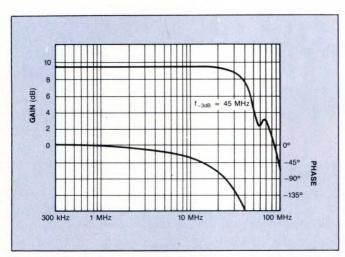


*Fig 15—The response of the circuit in Fig 13 extends from dc to a −3-dB point at 45 MHz.*

### TABLE 4—MEASURED PROPERTIES OF THE DC-COUPLED INSTRUMENTATION AMPLIFIER

| PARAMETER | VALUE |
|---|---|
| GAIN @ 50 kHz | 2.99 |
| GAIN @ 1 MHz | 3.00 |
| GAIN @ 10 MHz | 3.07 |
| GAIN TEMPERATURE STABILITY AT 1 MHz (REFERRED TO $T_A$ =25°C) | −0.56% ($T_A$ =+125°C) −0.33% ($T_A$ =−55°C) |
| BANDWIDTH | 45 MHz |
| GAIN FLATNESS | <0.3 dB (0 to 24 MHz) |
| INPUT IMPEDANCE | 4 MΩ ‖ 4 pF |
| CMRR | 60 dB @ 1 MHz |
| COMMON-MODE RANGE | ± 3V WITH ± 5V SUPPLY |
| OUTPUT VOLTAGE SWING | ± 3V INTO 2 kΩ ± 2V INTO 50Ω |

V/V; it uses the VA4708 as its basic building block. (The frequency response is shown in **Fig 15.**) The amplifier was tested over the full military temperature range **(Table 4)**. Note that the gain flatness is less than 0.3 dB with a −3 dB bandwidth of 45 MHz. Gain variations at 1 MHz are less than 0.6% over the military temperature range.

You can see from these examples how you can extend most of the standard op-amp techniques to the video region by using video op amps. Often the biggest problem is the less-than-ideal characteristics associated with the discrete components, the package parasitics, and the stray ground capacitance rather than the active elements. If you use these amplifiers with chip-and-wire hybrid construction, you can obtain even better performance. **EDN**

### References

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### Authors' biographies

*Ken Schaefer is a linear applications engineer for VTC. He received a BSEE from Marquette University in 1963. Prior to joining VTC in 1985, Ken worked in analog-circuit design for Ball Electronics, CDC, Raytheon, and General Motors. Ken's design experience includes CRT displays, switching regulators, and servomechanisms. In his leisure time, he races bicycles.*
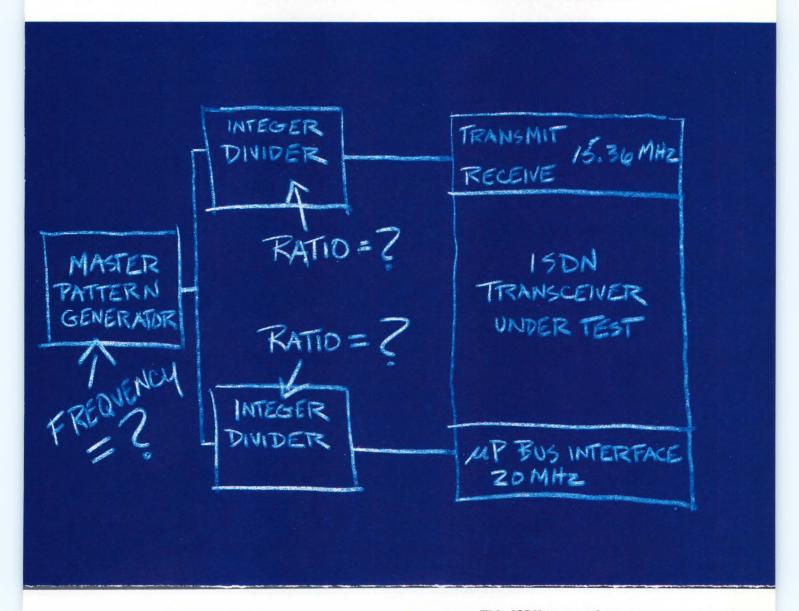
*John Shier is the strategic marketing manager for VTC, and was heavily involved in planning VTC's analog products. He received a BS in physics from the California Institute of Technology in 1960, and an MS and PhD in physics from the University of Illinois in 1962 and 1966. He was a postdoctoral fellow at the Los Alamos Scientific Laboratory and a solid-state researcher for NASA before taking up IC work in 1970. John has held IC processing and design positions at Signetics, AMD, Intersil, Sperry Univac, and CDC before joining VTC. He is a senior member of the IEEE, and is currently the general chairman of the IEEE Bipolar Circuits and Technology Meeting. John is the author of 18 technical papers and holds 3 patents. In his spare time, he enjoys reading, sailing, and gardening.*
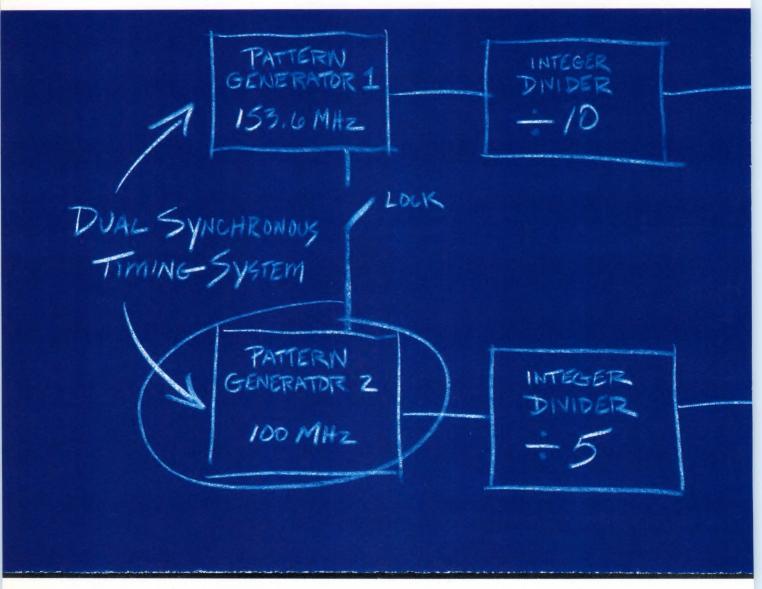
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LOCK

DUAL SYNCHRONOUS TIMING-SYSTEM

PATTERN GENERATOR 2
100 MHz

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| IH5140-IH5145 | Improved High-level CMOS |
| IH5148-IH5149 | High-Level CMOS |
| IH 5341/5352 | CMOS Dual/Quad/Video/RF |
| IH6108/6208 | CMOS 8-/4-Channel Differential Mux |
| IH6116/6216 | CMOS 16-/8-Channel Differential Mux |
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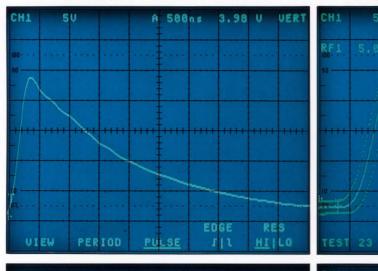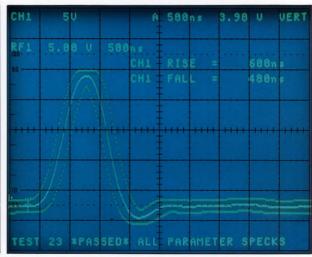


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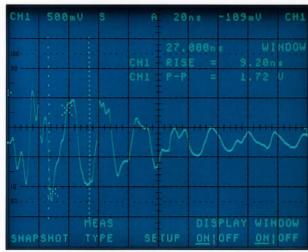
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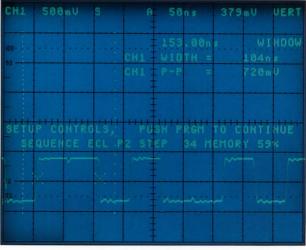
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# Use a single-chip μC as the heart of your position controller

*A single chip can be the basis of a computer-based position controller. This article provides enough detail about hardware and microcode to allow you to design your own position controller—even if you have little experience with motion control.*

William C Warner, *Consultant*

You can design a position-loop controller by using a single-chip microcomputer (μC). You must choose a μC that possesses the following characteristics:

- a minimum of 2k bytes of internal ROM,
- a minimum of 128 bytes of internal RAM,
- an internal timer that can request interrupts,
- an external interrupt-request pin,
- serial transmit and receive pins,
- 11 digital output pins, and
- four digital input pins.

The Motorola 68701 or the Intel 8751 is suitable.

## A position-loop controller has a lot to do

**Fig 1** depicts a general dc servomechanism. The position-loop controller (hereafter known as the controller), on the left side of the figure, receives commands to move a table from one position to another at some speed. In response, the controller indicates the required motor speed and direction to a dc motor drive.

The drive employs a reading of actual motor velocity, provided by a tachometer, in an effort to make the motor run at the speed commanded by the controller. The motor turns a leadscrew clockwise or counterclockwise, causing the table to move right or left. As the leadscrew turns—and the table moves—an encoder emits pulses and the controller notes them. In this way the controller tracks table movement and knows when the table is in position.

The controller is aware of all pulses from the encoder, even those that occur when the leadscrew is supposed to be at rest but for some reason turns anyway. When the controller sees this uncommanded motion, it directs the motor drive to run the motor and put the table back into position. The controller must always automatically oppose unexpected motion; you can think of this opposition as a "reflex" of the controller.

The controller must respond to requests to suspend motion ("feedhold"), to resume motion, and to make emergency stops. Finally, the controller must accelerate and decelerate the motor and table in a way that does not overstress the mechanisms, waste time or cause the table to overshoot its destination.

## The feedback unit—the system's resolution

An encoder rotates with the leadscrew; the encoder reports the motion of the leadscrew by sending signals on two channels. When the leadscrew turns with constant speed, the signals are square waves that are 90° out of phase. The controller detects the direction of the motion by noting which of the signals is leading; it determines the extent of the motion by counting the cycles.

*The controller must always automatically oppose unexpected motion; you can think of this opposition as a "reflex" of the controller.*
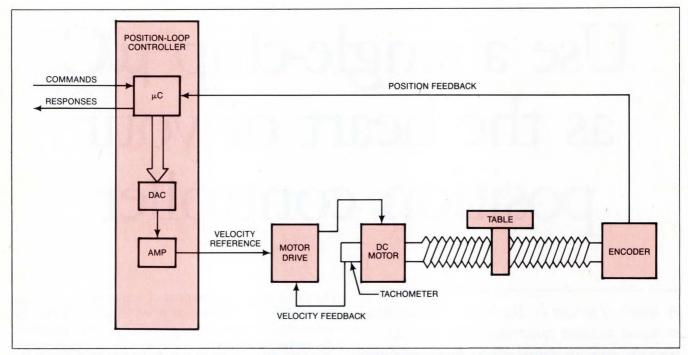


Fig 1—**This block diagram of a generalized servomechanism** shows an overall position-feedback loop with feedback supplied by an encoder, and an inner velocity-feedback loop, in which a tachometer supplies the feedback.

Resolution, or positioning accuracy, is equal to the distance the table travels in one encoder cycle. Suppose that in 1 in. of table travel the encoder generates 100 cycles. The resolution of the position loop—the positioning accuracy—is, then, 0.01 in. (10 mils). This distance is called a "feedback unit;" it's the smallest distance over which the controller can move the table. The controller measures all larger departures in feedback units.

**"Go" commands initiate motion**

A "Go" command is an output from the controller intended to cause a move of one feedback unit. Suppose that the table in **Fig 1** is at rest and you tell the controller to move it 5 in. to the right or the left. Under the assumptions of the previous paragraph, a 5-in. move is 500 feedback units. Therefore, the controller must issue 500 Go commands. A Go command simply acts to increment or decrement an "error count;" it increments the count when it commands clockwise leadscrew rotation and decrements the count when it commands counterclockwise rotation. RAM in the μC records the error count. The magnitude and sign of the error count determine the speed and direction of table motion.

The required table velocity determines the frequency of the Go commands. Suppose that the 5-in. move must

occur at 10 in./sec. The controller must issue 500 Go commands in 0.5 seconds, or one Go command every 0.001 sec. The table's speed is called "feed rate." Ordinarily, you'd specify feed rate in inches per second or centimeters per second, but the controller converts the rate to feedback units per second, thus calculating the required frequency of Go commands. (Feedback units per second equals Go commands per second.) To achieve the desired feed rate, the μC's internal timer generates periodic interrupts at the calculated frequency. These interrupts invoke a routine that increments the error count (for clockwise motion) or decrements it (for counterclockwise motion) once for each interrupt.

**Multiple mechanisms keep the controller informed**

The leadscrew turns the encoder, and the encoder provides position feedback to the controller. The feedback consists of signals on two channels, A and B. These signals indicate the direction of rotation of the leadscrew (and hence the direction of table movement), and they also indicate whether the leadscrew has turned far enough to move the table one feedback unit.

**Fig 2a** shows the signals on channels A and B. At constant velocity they are square waves; during acceleration they contract and during deceleration they stretch out. One complete cycle on channel A is called
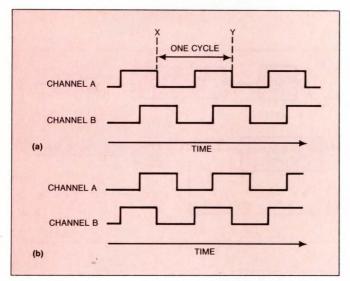
*Fig 2—When the motor velocity is constant, the encoder produces square waves. The controller can tell the direction of motion by determining which of the encoder's two output signals leads the other.*

an encoder cycle. In the figure, one cycle exists between the markers X and Y. The encoder rotates through one complete cycle while the table moves one feedback unit.

If you term the controller output that causes movement a "Go command," you can call an encoder cycle (the encoder's response to movement) a "Gone cycle." The μC senses Gone cycles and adjusts its knowledge of where the table is and decrements or increments the error count accordingly. Usually, Gone cycles work against Go commands; Go commands build the error count, positive or negative, and Gone cycles, resulting from leadscrew rotation, drive the error count back toward zero. (However, Gone cycles don't always occur in response to commanded motion, nor do they always act to count the error back to zero, as demonstrated below.)

The μC knows that one complete encoder cycle corresponds to one feedback unit of table movement, but it must take further action to determine the table's direction of motion. Notice that the two waveforms in **Fig 2a** are shifted one quarter cycle (90°) relative to each other. If you follow the signals from left to right, they progress as they would during clockwise motion. Note that signal A rises, then B rises, then A falls, then B falls, and so on. Signal B does what signal A does, except it does so one quarter cycle later; signal A is said to lead signal B. Channel A leads channel B during clockwise rotation. If you scan the signals from right to

left in **Fig 2a**—or from left to right in **Fig 2b**—they progress as they would in counterclockwise rotation: Channel B leads channel A.

**Fig 3** shows channel A connected to a functional block labeled "Encoder-signal edge detection." This block represents circuitry that interrupts the μC every time the state of channel A changes. In response to the interrupt, the μC reads the states of the two encoder channels. If channel A is low, a falling edge on channel A must have caused the interrupt. If channel B is high at that time, the μC knows that a partial clockwise cycle has occurred. If channel B is low, the μC concludes that a partial counterclockwise cycle has occurred.

From time to time, an encoder will stop turning very near a point where the state of channel A changes. When it does, small vibrations in the mechanism can cause the signal to jitter (to rapidly alternate states). Were the μC to regard every transition of the signal as marking the boundary of a feedback unit, it would rapidly change its signal to the motor drive—an undesirable effect. The μC notes every transition in signal A, but it does not consider that the table has crossed a feedback-unit boundary until a complete cycle has taken place. The μC recognizes the occurrence of a complete cycle when it senses two transitions on channel A without a reversal in leadscrew direction. This requirement introduces hysteresis that keeps the μC from rapidly changing its signal to the motor drive while the encoder jitters around an edge in signal A. A consequence of the way the controller handles the jitter is that the boundary of a feedback unit shifts one quarter cycle after a reversal. After noting a complete encoder cycle, the μC updates both the error count and its understanding of the table position.

**Error, following error, and velocity reference**

RAM in the μC holds the error count. Go commands and Gone cycles increment and decrement that count. The error-count value is called "following error" or simply "error." It has magnitude and sign. The magnitude of the error is the number of feedback-unit moves that have been commanded but not taken, or the number of moves that have been taken but not commanded. The sign of the error indicates the direction in which the table is out of position.

The number 128 represents zero error. One count of error in the clockwise direction is 129. The maximum clockwise error is 255, which corresponds to 127 feedback units out of position in the clockwise direction.
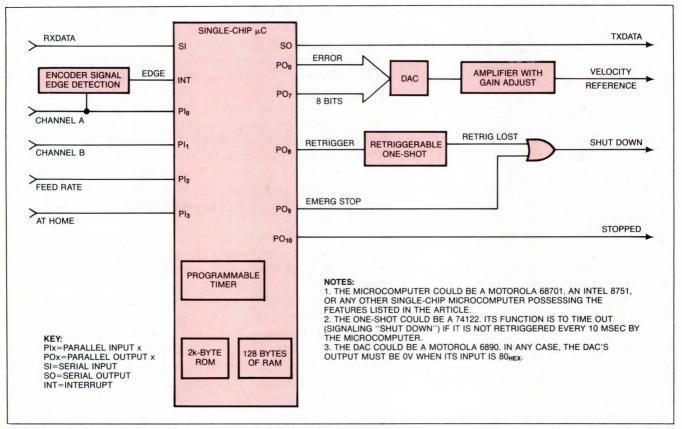
**Fig 3—The main position-loop-controller element** *is a single-chip microcomputer. Any of several types will do—the main requirements are that the chip incorporate a programmable timer and adequate ROM and RAM.*

One count of counterclockwise error is 127. Maximum counterclockwise error is zero, which represents 128 feedback units out of position in the counterclockwise direction.

An error greater than 128 means one of two things. Either Gone cycles are lagging behind Go commands in a clockwise move, or the leadscrew has moved counterclockwise without a command to do so, as when the table overshoots its destination or drifts out of position. When the error is 127 or less, Gone cycles are lagging behind Go commands in a counterclockwise move, or the leadscrew has moved clockwise without a command.

Any time the error count changes, the μC writes the new value to a D/A converter (DAC) (**Fig 3**). The amplified output of the DAC is the Velocity Reference signal to the motor drive. This signal normally has a range of approximately −10 to +10V. When the error is zero (the error count is 128), Velocity Reference is 0V. Maximum clockwise error, written to the DAC, produces a +10V Velocity Reference signal; maximum counterclockwise error results in a −10V signal. A positive signal indicates that the motor should turn clockwise; a negative signal indicates that it should turn counterclockwise.

The magnitude of Velocity Reference is proportional to the required motor speed. A large value means "run fast," a small value means "run slowly." Because there are 256 steps in the error count from 0 to 255—full-speed clockwise to full-speed counterclockwise—the velocity reference signal can take on 256 values from −10 to +10V.

An amplifier with adjustable gain amplifies the output of the DAC to produce the Velocity Reference signal. The amplifier's gain serves as the gain for the position loop. At any particular gain setting, the velocity reference signal and, hence, the speed of the motor, are proportional to the error's magnitude. The amplifier's gain is the constant of proportionality:

$$\text{Velocity} = \text{gain} \times \text{error}.$$

The position-loop gain amplifies the effect of a given
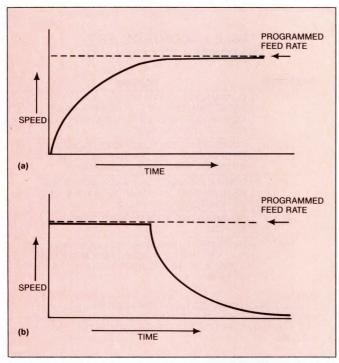
*Fig 4—Adjusting the gain that multiplies the velocity-feedback signal affects the servo's damping. You normally won't want overshoot, and you must limit the response speed to avoid overstressing the mechanical components. You'll usually want exponential response, like that shown here.*

amount of error. When you set the gain very high, even a small error produces a large velocity. When you set the gain low, the error must be larger to produce the same velocity. In effect, the position-loop gain determines how seriously the motor drive treats an error. The higher the gain, the faster the motor will accelerate as the error grows, and the faster it will decelerate as the error falls. You must be able to adjust the gain to prevent damage to the system's mechanical components —different servomechanisms tolerate differing degrees of acceleration and deceleration.

## Exponential acceleration and deceleration

Imagine the motor at rest with zero error. A 5-in. move begins. Go commands begin to increase the error (positively if the motor is going clockwise, negatively if it's going counterclockwise). The error grows because the motor and masses do not start to move immediately. As the error grows, the Velocity Reference signal grows. Eventually the leadscrew begins to turn and the encoder produces Gone cycles. The motor is just beginning to move, so the Gone cycles do not occur as fast as the Go commands do. The error continues to mount, but

not as fast as at first. As the error climbs, Velocity Reference climbs. Motor speed increases, increasing Gone-cycle frequency. The error grows more slowly still. Finally, the motor is up to speed, and every Go command is answered by a Gone cycle. Error remains constant and, consequently, so does motor speed. The table rides along at the programmed feed rate, and its position is a fixed number of feedback units behind the commanded position. This kind of acceleration, increasing speed at a decreasing rate, is exponential (**Fig 4a**).

Deceleration at the end of the move is also exponential. It happens like this: Once all of the Go commands have been issued, nothing further augments the error. But because there is still following error, the controller continues to drive the motor and the resulting Gone cycles begin to diminish the error. As the error count falls, Velocity Reference, motor speed, and Gone-cycle frequency all fall, so that although the error count is diminishing, it's doing so at a decreasing rate. The error continues to decline until, finally, the table is in position and error count and Velocity Reference are zero. At this point, as many Gone cycles have occurred as Go commands, so the table is at its final destination (**Fig 4b**). The motion of the motor after Go commands have stopped is called "taking up the error."

## Overshoot, drift, and other unexpected motion

The encoder produces Gone cycles whenever the leadscrew rotates—even when the controller produced no Go commands. A nonzero error count, therefore, is not always the result of unanswered Go commands; sometimes it stems from uncommanded Gone cycles. No matter . . . error is error. Any nonzero error count creates a nonzero velocity-reference signal, which works to eliminate the error. If the table overshoots its destination, drifts, or is forced out of position, the resulting Gone cycles produce a nonzero error count and a velocity-reference signal that opposes the uncommanded movement. The motor fights to bring the table back into position and, as it succeeds, Gone cycles count the error down to zero.

## When you have to stop the table, use feedhold

Note the Feedhold signal to the μC in **Fig 3**. Ordinarily this signal comes from a pushbutton. An operator presses the button to stop the table. When the μC senses a request to feedhold, its response is simple; it stops issuing Go commands. The motor will take up the error in exponential deceleration and stop. When the operator presses the button again, cancelling the re-

*The resolution of the position loop is called a "feedback unit." It is the smallest distance that the controller can move the table.*

## TABLE 1—CONTROLLER'S COMMAND SET

| COMMAND CHARACTERS[1] | DESCRIPTION |
|---|---|
| F | FEEDHOLD. SUSPEND TABLE MOTION. |
| C | CONTINUE. RESUME A SUSPENDED MOVE. |
| Hdnnnn | GO HOME. THE SECOND CHARACTER—d—IS "C" IF THE TABLE WILL ENCOUNTER THE HOME SENSOR BY GOING CLOCKWISE; IT IS "W" IF THE LEADSCREW MUST ROTATE COUNTERCLOCKWISE TO DRIVE THE TABLE HOME. THE "nnnn" ARE FOUR ASCII-CODED HEX DIGITS REPRESENTING THE MAXIMUM NUMBER OF FEEDBACK UNITS TO MOVE IN A SEARCH OF HOME. THE CONTROLLER ADOPTS THIS VALUE AS THE MAXIMUM TRAVEL ALLOWED TO THE TABLE. |
| Inn | SET FEED RATE. THE "nn" ARE TWO ASCII-CODED HEX DIGITS REPRESENTING THE HIGH AND LOW NIBBLES OF A BYTE THAT INDICATES THE FEED RATE VALUE. FEED RATE IS SPECIFIED IN FEEDBACK UNITS PER 50 MSEC. MINIMUM FEED RATE IS ONE (20 FEEDBACK UNITS/SEC) AND MAXIMUM IS 50 (1000 FEEDBACK UNITS/SEC). THE NEW FEED RATE REMAINS IN EFFECT UNTIL A SUBSEQUENT SET-FEED RATE COMMAND CHANGES IT OR UNTIL YOU CHANGE IT IN THE MIDDLE OF A MOVE. |
| R | RE-ENABLE CONTROLLER. YOU USE THIS COMMAND TO RE-ENABLE THE CONTROLLER AFTER SHUTTING IT DOWN OR TO ENABLE IT INITIALLY WHEN YOU APPLY POWER. |
| Mnnnn | MOVE. THE "nnnn" ARE FOUR ASCII-CODED HEX DIGITS THAT REPRESENT THE ABSOLUTE POSITION (NUMBER OF FEEDBACK UNITS FROM HOME) TO WHICH THE CONTROLLER MUST MOVE THE TABLE. THE POSITION MUST BE LESS THAN OR EQUAL TO THE MAXIMUM TRAVEL SPECIFIED IN A PRECEDING HOME COMMAND. IF, DURING FEEDHOLD, YOU ABORT THE SUSPENDED MOVE, THE CONTROLLER ACCEPTS THE NEW MOVE BUT DOES NOT START IT UNTIL IT RECEIVES A CONTINUE COMMAND. |
| Sbb | SEND BYTE. THE "bb" ARE TWO ASCII-CODED HEX DIGITS THAT REPRESENT THE ADDRESS OF A BYTE IN THE CONTROLLER'S RAM. THE μC RESPONDS BY SENDING THE SPECIFIED BYTE AS TWO ASCII-CODED HEX DIGITS. THE FIRST NINE BYTES OF THE RAM (bb=00 TO bb=08) HOLD THE CONTROLLER'S STATUS TABLE (SEE **TABLE 3**). |

NOTE:
1. THE CONTROLLER RECOGNIZES THESE COMMANDS. COMMANDS ARE STRINGS OF ASCII CHARACTERS SENT TO THE CONTROLLER THROUGH THE SERIAL PORT.

## TABLE 2—CONTROLLER'S RESPONSES TO COMMANDS

| RESPONSE[1] | MEANING |
|---|---|
| C | COMMAND REJECTED BECAUSE OF A COMMUNICATION ERROR. A CHARACTER IN THE COMMAND STRING SUFFERED A PARITY, OVERRUN, OR FRAMING ERROR. |
| S | COMMAND REJECTED BECAUSE IT WAS OUT OF SEQUENCE. THE COMMAND IS NOT ALLOWED UNDER THE CURRENT CONDITIONS. |
| Y | COMMAND REJECTED BECAUSE IT WAS NOT WELL FORMED OR PARAMETERS WERE OUT OF RANGE (SYNTAX ERROR). |
| D | COMMAND HAS BEEN CARRIED OUT OR INITIATED. |
| Bnn | RESPONSE TO THE SEND-BYTE COMMAND; "nn" ARE TWO ASCII-CODED HEX DIGITS THAT REPRESENT THE VALUE OF A BYTE IN THE μC'S RAM. |

NOTE:
1. THE CONTROLLER GIVES THESE RESPONSEES TO COMMANDS. THE RESPONSES ARE STRINGS OF ASCII CHARACTERS THAT ARE SENT THROUGH THE SERIAL PORT BY THE CONTROLLER.

quest for feedhold, the μC resumes issuing Go commands, the error builds, and the motor accelerates. The controller remembers how many Go commands were left to go at the time of the feedhold request, and issues only that many more.

### Error limits avert disaster

You must impose a limit on the clockwise and counterclockwise error. If the error count reaches a limit, the μC stops issuing Go commands and waits for the table to catch up. As the table does catch up, error falls below the limit and the controller resumes issuing Go commands.

By respecting an error limit, the controller can detect when the motor is out of control and running away. If the error count continues to grow beyond the error limit, even after Go commands have ceased, the motor is out of control and the controller must shut it down.

The motor will also run away if you connect it—or the encoder—backward. If you connect the motor backward, when you tell it to turn clockwise, it will turn counterclockwise. When you connect either the motor or the encoder backwards, Gone cycles will not diminish the error; in fact they will augment the error, adding to the Go commands. With nothing to diminish it, the error will grow without bound. Unless the controller shuts the motor down when the error count reaches a

value that's a few counts greater than the limit, the motor will run away.

To ensure agreement among all the components in the system, and to lessen the chance of connecting something backward, you can adopt the following conventions or their equivalent:

- View the motor from the shaft end when deciding which way is clockwise and which way is counterclockwise;
- Connect the motor to the drive so that a positive velocity-reference signal will cause the motor to turn clockwise;
- Connect the encoder to the controller so that the controller will see channel A leading channel B during clockwise rotation.

**You *can* go home; sometimes you have to**

The controller handles commands to move the table from position to position. But it does not always know the absolute position of the table. It only knows how many feedback units the table has moved from some starting point. In order to translate that information into knowledge of absolute position, the table must have a "home" location near one end of its travel. A sensor, tied to the µC, indicates the presence of the table at home. Whenever the controller is in doubt about absolute position (such as on power-up), it must refuse all commands to move the table until after it has received and executed a command to move the table to home.

The command to go home must include parameters that tell the controller which way to move and how many feedback units to go in search of home. The controller moves the table toward home at some slow speed. When the signal from the home sensor indicates that the table has arrived at home, the controller stops issuing Go commands. The motor takes up the error and the table comes to rest. The controller then sets its internal representation of table position to zero.

If, during the move toward home, the table hits the home sensor before accelerating fully, or if the table is activating the home sensor when the controller receives the "go home" command, the controller must move the table, at some low speed, far enough away from home to ensure that, during its move toward home and before it hits the home sensor, the table reaches its "homing speed." A table that is accelerating when it arrives at the home sensor will not come to rest at the place it would have if it had reached homing speed. When the table actuates the home sensor before reaching maxi-

**TABLE 3—BYTES THAT DESCRIBE KEYSYSTEM PARAMETERS**

| RAM ADDRESS | CONTENTS |
|---|---|
| 00 | STATUS BYTE 0 |
| 01 | STATUS BYTE 1 |
| 02 | CURRENT FOLLOWING ERROR |
| 03 | MOST SIGNIFICANT BYTE OF GREATEST ERROR THAT OCCURRED IN LAST MOVE |
| 04 | LEAST SIGNIFICANT BYTE OF GREATEST ERROR THAT OCCURRED IN LAST MOVE |
| 05 | MOST SIGNIFICANT BYTE OF TABLE POSITION |
| 06 | LEAST SIGNIFICANT BYTE OF TABLE POSITION |
| 07 | MOST SIGNIFICANT BYTE OF FEEDBACK UNITS LEFT IN A MOVE THAT IS UNDERWAY OR HAS BEEN SUSPENDED |
| 08 | LEAST SIGNIFICANT BYTE OF FEEDBACK UNITS LEFT IN A MOVE THAT IS UNDERWAY OR HAS BEEN SUSPENDED |

mum speed, the controller can't position the table at home correctly.

If the controller were to fail while controlling the position of the table, it might not respond to encoder signals. Whatever error was presented to the D/A converter at the time that the controller failed would remain there. The table would ride along at the speed corresponding to that error to the end of its travel.

The watchdog circuitry pictured in **Fig 3** stops the motor when the controller fails. This circuitry times out if the controller does not retrigger it often enough. The controller ought to be able to retrigger every 10 msec. If it doesn't, the controller has probably failed. (Maybe a software bug has caused it to lock up.) So the watchdog circuitry times out and stops the motor.

A position-loop controller can very easily signal when the table is at rest. Whenever the error is zero, the table is stopped and the microcomputer drives the Stopped output true **(Fig 3)**.

**Converse with the controller in its native tongue**

The controller receives commands through a serial port as ASCII characters. Because the controller must spend most of its time responding to timer and encoder interrupts, the commands must be short and simple; they must be transmitted relatively slowly (1200 bps max). Commands begin with a single command character that identifies the command. They end with a single end-of-command character, such as a carriage return.

## TABLE 4—INFORMATION CONTAINED IN THE SYSTEM STATUS BYTES

| BITS | CONDITIONS THAT SET BITS | |
|---|---|---|
| | STATUS BYTE 0 | STATUS BYTE 1 |
| 0 | ALL GO COMMANDS HAVE BEEN ISSUED | EMERGENCY-STOP COMMAND RECEIVED |
| 1 | TABLE IS STOPPED | ERROR WENT ABOVE ERROR LIMIT |
| 2 | TABLE IS "LOST" (MUST HOME) | ENCODER PULSES OUT OF SEQUENCE |
| 3 | IN FEEDHOLD | ENCODER INTERRUPTS COMING TOO FAST |
| 4 | SHUT DOWN; MUST RE-ENABLE (SEE BYTE 1) | COULDN'T FIND HOME |
| 5 | TABLE IS AT HOME | COULDN'T LOSE "AT HOME" SIGNAL |
| 6 | NO FEED RATE ESTABLISHED | (NOT USED) |
| 7 | (NOT USED) | (NOT USED) |

Some commands include parameters, represented by ASCII characters between the command and end-of-command characters. **Table 1** details the commands.

The controller carries out a command and sends a response that tells the outcome. A response is one or three ASCII characters transmitted through the serial port. The response may indicate that the command has been carried out or initiated; it may indicate that the command was improperly formatted or illegal at the time it was received, or it may say that command characters have suffered transmission errors. **Table 2** explains the controller's responses. A "success" response to a command that causes motion (move or go home) means only that the move has begun. You must poll the controller with send-byte commands until its status indicates that a move has been completed.

### Table position and maximum error

The controller keeps track of the table's absolute position (feedback units from home). When it is at home, the table is in position zero. One feedback unit away from home is position one, and maximum travel away from home takes the table to position $FFFF_{HEX}$. By definition, there is only one permissible direction away from home. The home command establishes whether the direction toward home is clockwise or counterclockwise.

The controller also saves the largest error that occurs during a move. This information is useful in setting the gain of the position loop. A large error means that the

table did not accelerate quickly. When the maximum error equals the error limit, the table did not even reach programmed feed rate during the last move.

The controller keeps these values in its status table (**Tables 3** and **4**); send-byte commands can read them out.

### Emergency stop and re-enable commands

The controller must be able to tell the motor drive to stop the motor immediately when some dangerous situation exists. It uses the signal Emerg Stop (**Fig 3**) for this purpose. The controller asserts Emerg Stop when any of the following is true:

- the controller has detected encoder signals out of sequence,
- encoder interrupts have occurred faster than the controller can service them,
- the error has grown past the error limit,
- the controller has received the emergency-stop command,
- or the controller has just been turned on.

While asserting Emerg Stop, the controller makes no attempt to control or track the position of the table. It sets error and position to zero. It rejects all commands to move the table until it receives the re-enable command. When the controller receives that command, it stops asserting Emerg Stop and sets an internal "table-must-be-homed" flag. It begins to monitor the encoder signals and to update the error count. **Listings 1** through **8** contain pseudocode that represents the major routines embedded in the position controller's μC firmware. **EDN**

### Author's biography

*Will Warner runs his own consulting business in Ann Arbor, MI. He specializes in the application of microcomputers to instrumentation and automation. He holds a BS in mathematics from Michigan State University. Before becoming a consultant, he worked for General Electric Co and Machine Vision International. Will's favorite spare-time activity is reading.*

Article Interest Quotient (Circle One)
High 488 Medium 489 Low 490

## LISTING 1

```
/*
** Power-up initialization and main control logic.
**
** After performing power-up initializations, the program enters
** an endless loop from which it controls the operation of the
** motor controller.
*/

initialize parallel I/O
shut down motor due to power-up
clear status table
initialize variables
initialize serial I/O
clear serial-receive queue
clear serial-transmit queue
indicate "lost"
indicate "disabled"
table position = 0
indicate not in feedhold
indicate not homing
allow serial-receive interrupt

DO FOREVER
    retrigger watchdog one-shot
    update status table
    IF (emergency-stop input true) THEN
        shut down motor due to emergency-stop input
    IF (feedhold input true) AND (not disabled) THEN
        indicate in feedhold
    IF (a complete command has been received) THEN
        process the command
    IF (error = 0) THEN
        make table-stopped output true
    ELSE
        make table-stopped output false
    IF (serial transmit is ready to transmit again) THEN
        IF (a character is in the transmit queue) THEN
            dequeue a character and transmit it
    IF (homing in progress) THEN
        continue homing process
END
```

## LISTING 2

```
/*
** Service serial-receive interrupt.
**
** Queue command characters to be analyzed by background code.
** Flag communication errors and end of command.
*/

disable serial-receive and Go-command interrupts
allow encoder interrupt if it is not disabled

read character from serial-receive register

IF not (unprocessed complete command in serial recv queue) THEN
    IF (character suffered parity or framing error) THEN
        remember communication error occurred
    ELSE
        queue character in serial-receive queue
        IF (character is end-of-command character) THEN
```

## LISTING 3

```
/*
** Process a command received through the serial port.
**
** Queue a response to the command.  If the command is
** acceptable, carry it out or set it in motion.
*/


IF (a communication error occurred) THEN
    queue "C" to send (report communication error)
IF (no communication error) AND (command character is invalid) THEN
    queue "Y" to send (report syntax error)
IF (no communication error) AND (command character valid) THEN
    IF (command is send-byte command) THEN
        format specified byte into two ASCII-coded hex characters
        queue "B" and the two characters to send
IF (no communication error) AND (command character valid) THEN
    IF (not disabled) THEN
        DO CASE (command character)
            re-enable command:
                queue "S" to send (report command out of sequence)
            feedhold command:
                indicate in feedhold
                queue "D" to send (report success)
            continue command:
                IF (feedhold input false) THEN
                    indicate not in feedhold
                queue "D" to send (report success)
            emergency-stop command:
                shut down motor due to emergency-stop command
                queue "D" to send (report success)
            set-feed-rate command:
                calculate new feed rate from cmd parameter characters
                IF (new feed rate within range) THEN
                    adopt new feed rate
                    queue "D" to send (report success)
                ELSE
                    queue "Y" to send (report syntax error)
            move command:
                IF lost THEN
                    queue "S" to send (report command out of sequence)
                ELSE IF (end point of move is out of range) THEN
                    queue "Y" to send (report syntax error)
                ELSE IF (a move underway) AND (not stopped in feedhold) THEN
                    queue "S" to send (report command out of sequence)
                ELSE
                    start move to end point specified in the command
                    queue "D" to send (report move begun)
            home command:
                IF (a move underway) THEN
                    queue "S" to send (report command out of sequence)
                ELSE
                    initiate homing process: home stage = 1
                    indicate "lost"
                    queue "D" to send (report homing begun)
        END
```

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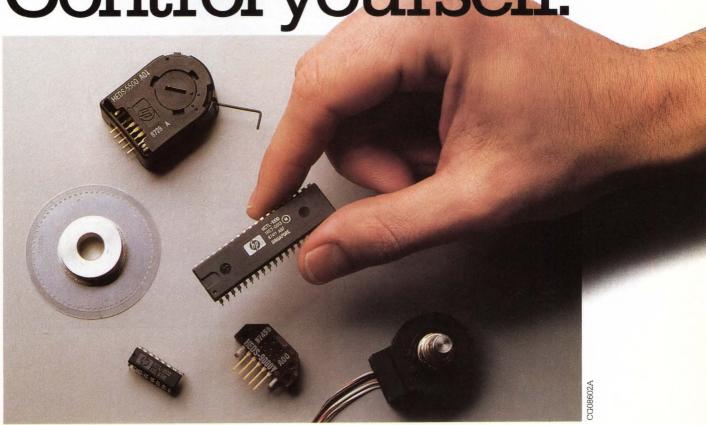
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# Control yourself.

## LISTING 3 *(Continued)*

```
IF (no communication error) AND (command character valid) THEN
    IF disabled THEN
        DO CASE (command character)
            feedhold command:
            continue command:
            emergency-stop command:
            home command:
            move command:
            set-feed rate command:
                queue "S" to send (report command out of sequence)
            re-enable command:
                read and save initial states of encoder signals
                allow encoder interrupt
                make emergency-stop output false
                queue "D" to send (report success)
        END


clear "communication error" indication
clear "command awaiting processing" indication
```

## LISTING 4
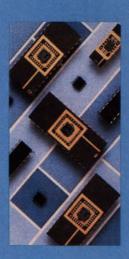
```
/*
** Start a move
**
** Pass this routine the end point (in feedback units from home)
** of a move to be made. It calculates and saves the number of
** Go commands that must be issued to get to the end point from
** the present position. This routine calculates the frequency at
** which the Go commands must be issued in order to achieve the
** desired feed rate.
*/


IF (end point of move not equal present position) THEN
    IF (end point of move further from home than present position) THEN
        Go commands to issue = end point of move - present position
        IF (home is found moving CW) THEN
            indicate direction of move is CCW
        ELSE
            indicate direction of move is CW
    ELSE
        Go commands to issue = present position - end point of move
        IF (home is found moving CW) THEN
            indicate direction of move is CW
        ELSE
            indicate direction of move is CCW

    greatest error this move = 0
    calculate timer interrupt period needed to produce desired feed rate
    set up timer to interrupt after calculated time
    allow timer interrupt


Note:  In the above, "present position" is where the table is with zero
error; that is, where Go commands have moved it.
```

## LISTING 5

```
/*
** Service timer (Go-command) interrupt.
**
** This routine runs in response to timer interrupts.  It issues
** Go commands by augmenting the error count.  This routine is
** invoked at a frequency which was calculated to produce the
** desired feed rate.
*/

disable Go-command interrupt
start timer counting ticks to next interrupt
allow serial-receive interrupt
allow encoder interrupt if it is not disabled

IF (not in feedhold) THEN
    IF (direction is CW) AND (error < CW error limit) THEN
        increment error
    ELSE IF (direction is CCW) AND (error < CCW error limit) THEN
        decrement error
    write new error out to D/A
    decrement count of Go commands left to issue

IF  (in "toward home" stage of homing process) THEN
    IF (at-home input true) THEN
        Go commands to go = 0

IF (Go commands to go > 0) THEN
    enable Go-command interrupt

allow all interrupts not disabled
return from interrupt
```

## LISTING 6

```
/*
** Service external (encoder) interrupt.
**
** This routine runs in response to edges in one signal from an
** encoder. It diminishes the position-loop error if motion is
** commanded; it augments the error if motion is uncommanded.
*/

IF (being re-entered) THEN
    shut down for encoder interrupts coming too fast

ELSE
    indicate executing encoder interrupt handler (to catch re-entry)
    disable serial-receive and Go-command interrupts
    allow encoder interrupt

    read encoder signals channel A and channel B

    IF (channel A is low) AND (channel B is high) THEN
        IF previous states of channels were high/low THEN
            a CW encoder cycle has occurred: decrement error
            IF (home is CW) THEN
                decrement table position
            ELSE
                increment table position

        ELSE IF (channel A is low) AND (channel B is low) THEN
            IF previous states of channels were high/high THEN
```

## ANALOG DEVICES
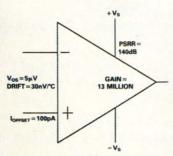
### 15µV max Offset Voltage
### Ultralow Drift Op Amp

### AD707

**FEATURES**
**Very High dc Precision**
  15µV max Offset Voltage
  0.1µV/°C max Offset Voltage Drift
  0.35µV p-p max Voltage Noise (0.1Hz to 10Hz)
  8V/µV min Open-Loop Gain
  0.32µV/V max CMRR
  1µV/V max PSRR
  1nA max Input Bias Current
  1nA max Input Offset Current
**Dual Version Available: AD708**

$+V_S$

$V_{OS} = 5\mu V$
$DRIFT = 30nV/°C$

PSRR = 140dB

GAIN = 13 MILLION

$I_{OFFSET} = 100pA$

$-V_S$

### PRODUCT DESCRIPTION
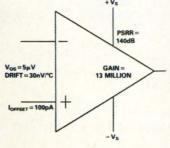
The AD707 is a low cost, high precision op amp with state-of-the-art performance that makes it ideal for a wide range of precision applications. The offset voltage spec of less than 15µV is outstanding for a bipolar op amp, as is the 1.0nA maximum input offset current. The top grade is the first bipolar monolithic op amp to offer a maximum offset voltage drift of 0.1µV/°C, and offset current drift and input bias current drift are both specified at 25pA/°C maximum.

The AD707's open-loop gain is 8V/µV minimum over the full ±10V output range when driving a 1kΩ load. Maximum input voltage noise is 350nV p-p (0.1Hz to 10Hz). CMRR and PSRR are 130dB and 120dB minimum respectively.

The AD707 is available in versions specified over commercial, industrial and military temperature ranges. It is offered in 8-pin plastic mini-DIP, small outline, hermetic cerdip and hermetic TO-99 metal can packages. Chips and Mil Standard/883 parts are also available.

### APPLICATION HIGHLIGHTS

1. The AD707's 13V/µV typical open-loop gain and 0.1µV/V typical common-mode rejection ratio make it ideal for precision instrumentation applications.

2. The precision of the AD707 makes tighter error budgets possible at a lower cost.

3. The low offset voltage drift and low noise of the AD707 allow the designer to amplify very small signals without sacrificing overall system performance.

4. The AD707 can be used where chopper amplifiers are required, but without the inherent noise and application problems.

5. The AD707 is an improved pin-for-pin replacement for the OP-07, OP-77 and the LT1001.

# HERE'S THE MOST ACCURATE SOURCE OF INFORMATION ON THE WORLD'S MOST ACCURATE BIPOLAR OP AMP.

If your analog applications demand precision performance, then you should demand our new AD707 – the world's best dc precision op amp.

The AD707 is the first bipolar monolithic to offer a maximum offset voltage drift of only 0.1µV/°C, and 15µV maximum offset voltage. These features, combined with its ultralow 0.35µV p-p voltage noise, allow the AD707 to amplify extremely small signals without sacrificing system performance.

The AD707 also provides an open-loop gain of 13V/µV, which is the highest of any precision op amp, and unsurpassed 140dB CMRR and PSRR. So it's ideal for a wide range of precision applications, including instrumentation and automatic test equipment.

All this precision makes it easy for you to work within tight error budgets. And because the AD707 is available at a low cost, you can easily work within your design budget, too. Versions start at only $1.25 (in 100s).

For an even more accurate description of what the AD707 can do for you, call Applications Engineering at (617) 935-5565, Ext. 2628 or 2629.
Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

### ANALOG DEVICES

**LISTING 6** *(Continued)*

```
            a CCW encoder cycle has occurred: increment error
        IF (home is CCW) THEN
            decrement table position
        ELSE
            increment table position

    IF (error > error limit + 2) THEN
        shut down motor because motor out of control
    ELSE
        write error out to D/A
        save encoder signal states for next time
        IF (error > greatest error this move) THEN
            save error as greatest

indicate not executing encoder interrupt
allow interrupts that were enabled on entry and not disabled by shut down
return from interrupt
```

## LISTING 7

```
/*
** Control homing process
**
** While attempting to "home" the table, the main program loop
** calls this routine over and over (once per loop) until
** this routine indicates that the homing process is complete.
** This routine advances the homing process through several
** stages.
*/

DO CASE (homing stage)
    stage 1:
        IF (table is already on home switch) THEN
            start a small, slow move away from home
            home stage = 2
        ELSE
            start a slow move toward home
            home stage = 3
        return

    stage 2:
        IF (move away from home is done) THEN
            start a slow move toward home
            home stage = 3
        return

    stage 3:
        IF (move toward home is done and zero error) THEN
            IF (table not activating home switch) THEN
                shut down motor due to failure to find home switch
            ELSE
                table position = 0
                IF (move toward home didn't reach homing speed) THEN
                    home stage = 1
                ELSE
                    homing done:  home stage = 0
                    indicate not "lost"
        return
END
```

# ANALOG DEVICES

## Wide Bandwidth, Fast Settling Operational Amplifier

## AD9611

### FEATURES
Unity Gain Stable
Small Signal Bandwidth 280MHz
Full Power Bandwidth 220MHz
Settling – 13ns to 0.1%
Offset Voltage ±0.5mV
Bias Current ±1µA
Power Dissipation Independent of Load

### APPLICATIONS
Driving Flash Converters
High Speed DAC I-to-V Conversion
Radar, IF Processors
Baseband and Video Communications
ATE/Pulse Generators
Imaging/Display Applications

*AD9611 Functional Block Diagram*

BOTTOM VIEW
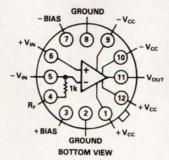
### PRODUCT DESCRIPTION
The AD9611 is a fast settling, wide bandwidth, low distortion, dc coupled operational amplifier that combines exceptional ac and dc specifications to establish a new standard of excellence. The combination provides designers with a unique solution when system speed and signal fidelity are critical.

Rise and fall times are 1.3ns. The –3dB bandwidth is 280MHz (G = ±5); full power bandwidth is 220MHz. The AD9611 settles to 0.1% in 13ns and has flat frequency response over the rated bandwidth. The design is optimized to provide low distortion over the full bandwidth, which means "clean" amplification for driving high speed flash A/D converters.

Input offset voltage is ±0.5mV with 5µV/°C drift; bias currents are typically ±1µA, and drift 75nA/°C. In most current-feedback amplifiers, bias current drifts are random. In the AD9611, inverting and noninverting bias currents drift in the same direction over temperature; this allows traditional resistor nulling for reducing effective output voltage drift.

The AD9611BH is rated for case temperatures from –25°C to +85°C; the AD9611TH is guaranteed from –55°C to +125°C. Contact the factory for information about 883 grade parts. All units are built and tested in a MIL-STD-1772 certified facility.

### PRODUCT HIGHLIGHTS
1. The current-feedback architecture which is used instead of voltage feedback makes bandwidth relatively independent of gain. With G = 0, –3dB bandwidth is 310MHz; at G = ±5, bandwidth is 280MHz; at G = ±20, bandwidth is 210MHz.

2. Extremely low distortion and noise are hallmarks of AD9611 performance. A 60MHz input tone is used for 100% testing of 2nd and 3rd harmonics; they measure –54dBc and –58dBc, respectively. With a 20MHz input, they measure –67dBc and –69dBc. Exceptionally low 3rd order two-tone intermodulation distortion (IMD) makes the AD9611 an ideal choice for communications/IF applications.

3. The AD9611 requires ±5V power supplies and has an innovative current-steering output stage that keeps total circuit power dissipation essentially constant regardless of output drive (for loads ≤100Ω). *Circuit power dissipation does not increase as the load is increased;* the unit can be operated up to +110°C in still air without heat sinking.

## LISTING 8

```
/*
**   Shut down the motor for some reason
*/

disallow all interrupts
make emergency-stop output true
disable Go-command (timer) interrupt
disable encoder (external) interrupt
set error equal to zero and write it out to D/A
indicate "lost"
indicate "disabled"
indicate not in feedhold
Go commands left to go = 0
table position = 0
indicate not "homing"
indicate reason for shutdown
allow serial-receive interrupt if it was enabled on entry
```

EDN September 1, 1988          **CIRCLE NO 135**          179

# ANALOG DEVICES

## AD840 Series

|  | AD840 | AD841 | AD842 | AD843 | AD844 |
|---|---|---|---|---|---|
| Gain Bandwidth<br>Min Stable Gain | 400MHz<br>10 | 40MHz<br>Unity | 80MHz<br>2 | 35MHz<br>Unity | 60 to 430MHz<br>Unity |
| Settling Time<br>(10V Step) | 100ns<br>to 0.01% | 110ns<br>to 0.01% | 100ns<br>to 0.01% | 110ns<br>to 0.01% | 100ns<br>to 0.05% |
| Slew Rate | 400V/$\mu$s | 300V/$\mu$s | 375V/$\mu$s | 300V/$\mu$s | to 2,000V/$\mu$s |
| Quiescent<br>Current (max) | 12mA | 12mA | 14mA | 12mA | 6.5mA |
| Comments | HA2540<br>Improved<br>Replacement | 50mA min<br>Output<br>Current | 100mA min<br>Output<br>Current | FET-Input,<br>Replaces FET-<br>Input Hybrids | Current Feedback,<br>2nV/$\sqrt{\text{Hz}}$ Noise<br>at 1kHz |

# THE REVOLUTION IN
# STARTS RI

Introducing our AD840 Series with ten new op amps – and the start of a revolution. Because now you can go to just one vendor and get more high speed op amps with higher precision and lower power than from anywhere else.

The AD840 Series, which includes high accuracy, low noise, low cost, FET-input and current-feedback amps, is the result of a major breakthrough we've made in analog process technology. A breakthrough that has not only led to such diversity, but has also made each op amp a performance leader.

For example, several of the products in the AD840 Series offer gain-bandwidths greater than 400MHz, while others offer slew rates up to 2,000V/$\mu$s. And all AD840 products offer precision at high speeds, with unprecedented settling time performance as fast as 100ns to 0.01% (10V step) and offset voltage down to 75$\mu$V maximum.

180

### AD840 Series

| AD845 | AD846 | AD847 | AD848 | AD849 | |
|---|---|---|---|---|---|
| 16MHz Unity | 46 to 600MHz Unity | 50MHz Unity | 175MHz 5 | 750MHz 25 | Gain Bandwidth Min Stable Gain |
| 350ns to 0.01% | 100ns to 0.01% | 120ns to 0.1% | 100ns to 0.1% | 80ns to 0.1% | Settling Time (10V Step) |
| 100V/μs | 450V/μs | 300V/μs | 300V/μs | 300V/μs | Slew Rate |
| 12mA | 6mA | 5.7mA | 5.7mA | 5.7mA | Quiescent Current (max) |
| FET-Input, Drives Cap Loads | Current Feedback, 75μV max Offset Voltage | Excellent Flash ADC Buffer | Stable into any Cap Load | Low Noise Pre-Amp | Comments |

# HIGH SPEED OP AMPS
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This high performance isn't at the expense of power. In fact, each AD840 product consumes 25-50% less power than comparable amps, without sacrificing load drive current. Plus all parts operate with ±15V or ±5V supplies.

The high performance doesn't come at a high cost, either. You'll find that whether you use the AD840 Series op amps to bring a new standard of performance to your designs, or as replacements for industry standards, they're all competitively priced.

If you'd like more information on why the AD840 Series makes us the new revolutionary leader in high speed op amps, call Applications Engineering at (617) 935-5565, ext. 2628 or 2629. Or write to Analog Devices, P.O. Box 9106, Norwood, MA 02062-9106.

## ANALOG DEVICES

**CIRCLE NO 125**

# National Design

## CAN THIS BE DONE?



## A COMMUNICATION DEVICE FOR THE SPEECH - DEAF

EXECUTIVE AUDIAL REHABILITATION SOCIETY....

the EARS design competition

**FIRST PRIZE - $100,000**
PLUS A % OF ROYALTY

**SECOND PRIZE - $50,000**
PLUS A % OF ROYALTY

**THIRD PRIZE - $25,000**
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**HUBERT W. UPTON**, Arlington, Texas, Electronics Engineer — Alternate
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### WINNERS 1986 SUGGESTION CONTEST

**MILDRED CRUICKSHANK**, Telephone connection
**ED POTTHARST**, Multichannel memory

# Competition

## WE THINK **YOU** CAN!

T HERE ARE 17,000,000 speech-deaf persons, i.e. do not understand speech, in the U.S. The objective is to provide a communication device that will allow one-on-one communication. The final EARS design, incorporating all possible operational advantages and economies of production, may be the composite of the prize winners' designs and may also incorporate features of the designs submitted by non-prize winners. Winners will be accorded cash and royalties. **All royalties negotiated by EARS will be passed through to the contestants**. The royalties will be apportioned by the Judges on the basis of their evaluation of the importance of each element submitted by any contestant which is included in the Final Production Design.

Those desiring to participate should apply (by mail or phone) for a registered entry blank to the Executive Audial Rehabilitation Society shown. Each entry shall include design, programming instruction and an operating "bread board" model which need not conform to the size goals. EARS will compensate those contestants (whose entries are adjudged to be operationally feasible) for the current cost of the components used to build the bread board operational model. The entries will be evaluated by the Judges on the basis of merit, i.e. operationally effective that can be produced at a reasonable cost.

**Detailed conditions of the competition will be set out on the entry form. DEADLINES: Entry forms must be procured and returned to EARS not later than October 31, 1988. Designs and bread board models must be received by 5 P.M. on May 1, 1989.**
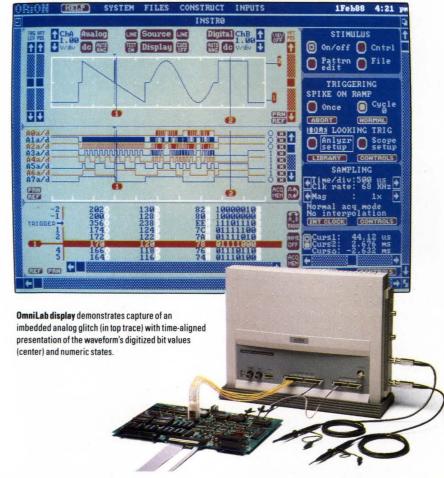
All designs submitted and accepted by the Judges shall be the property of EARS. No essential conceptual element of a design shall constitute a conflict with an existing patent. Conceptual protection of the device has been established as of date of origin. Formal application for patents on pertinent features will be applied for by EARS. A firm of patent attorneys specializing in electronics is retained. All decisions by the Judges as to the award or non-award of prizes or royalty shall be final and shall not be subject to change, review or amendment by EARS., its Officers, Executive Committee or the design contestants.

### DESIGN GOALS

1 The goal is a design for a hand-held, lightweight real time communication device capable of being produced at economical cost. The design should allow a speaking person to communicate on a one-on-one real time basis with the hearing-impaired person in any situation where normal conversation occurs and will provide for filtration of extraneous noise. The goal is a device contained in approximately 6" x 8" x 1½". A 5" x 7" screen will be on one side. The speech-deaf person can place it on a desk or hold it in hand. The speaker will first read a text identifying his phonetic alphabet in the memory. A multi-position switch would allow storage of the phonetic alphabets of different persons. For telephone calls, the speech of a person (whose phonetic alphabet is in one of the memory channels or who reads the text into a new channel) will enter the communication device through a standard telephone plug. The device will be battery-powered with rechargeable batteries but provide for alternative operation with a voltage converter. Intensive electronic speech analysis combined with the personal phonetic alphabet of the speaker will result in the "real-time" production of the spoken words on the screen. The speech of the hearing-impaired person not fitting the phonetic alphabet of the memory should be filtered out automatically if possible, otherwise manually.

2 Equally important is a design for this device that can be manufactured economically so that the cost is within the means of this group of people, many of whom may be economically disadvantaged.

**CIRCLE NO 80**
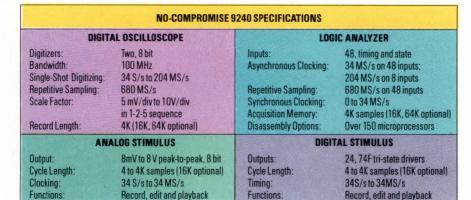
# Introducing OmniLab 9240.
# Totally Integrated Scope-Analyzer-Stimulus.

■ Combine a 100 MHz digital oscilloscope with a time-aligned, 200 MS/s 48-channel logic analyzer. Next add synchronized analog **and** digital stimulus generators. Then a remarkable new triggering system. What you have is the 9240 — a whole **new class** of instrumentation. Expressly designed to speed challenging analog and digital analysis. And get you from concept to product faster.

■ The 9240 is based on an innovative new instrument architecture that merges high-speed universal hardware and seamlessly-integrated software to create high-performance capabilities not available in separate instruments. Analog and digital traces are always time-correlated in a unique, single screen display. SELECT™ triggering bridges scope and analyzer techniques. And OmniLab's stimulus generators can playback captured or edited signals.

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■ OmniLab™ is a generation ahead of conventional digital scopes that often hide rarely occurring faults because they only show you a few cycles out of millions. With its continuous monitoring, you can use SELECT triggering to quickly catch every occurrence



**OmniLab display** demonstrates capture of an imbedded analog glitch (in top trace) with time-aligned presentation of the waveform's digitized bit values (center) and numeric states.

of rare events like metastable states, bus contentions, missing pulses, and buried noise glitches.

■ The 9240 is like having a complete benchtop of instruments integrated with your PC/AT or compatible. Which you can easily customize for digital development, analog development, or a combination of both.

■ With OmniLab, your productivity will soar. Because you achieve results with fewer instruments. And in fewer steps than ever before. By no means least, the 9240 delivers the best price/performance you'll find anywhere, costing just $8900 fully outfitted. And most importantly, without compromising a single high-performance spec. Not a one.

■ For more information, call **toll free 800/245-8500.** In CA: 415/361-8883. Or write for complete literature.

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| NO-COMPROMISE 9240 SPECIFICATIONS | | | |
|---|---|---|---|
| **DIGITAL OSCILLOSCOPE** | | **LOGIC ANALYZER** | |
| Digitizers: | Two, 8 bit | Inputs: | 48, timing and state |
| Bandwidth: | 100 MHz | Asynchronous Clocking: | 34 MS/s on 48 inputs; |
| Single-Shot Digitizing: | 34 S/s to 204 MS/s | | 204 MS/s on 8 inputs |
| Repetitive Sampling: | 680 MS/s | Repetitive Sampling: | 680 MS/s on 48 inputs |
| Scale Factor: | 5 mV/div to 10V/div | Synchronous Clocking: | 0 to 34 MS/s |
| | in 1-2-5 sequence | Acquisition Memory: | 4K samples (16K, 64K optional) |
| Record Length: | 4K (16K, 64K optional) | Disassembly Options: | Over 150 microprocessors |
| **ANALOG STIMULUS** | | **DIGITAL STIMULUS** | |
| Output: | 8mV to 8 V peak-to-peak, 8 bit | Outputs: | 24, 74F tri-state drivers |
| Cycle Length: | 4 to 4K samples (16K optional) | Cycle Length: | 4 to 4K samples (16K optional) |
| Clocking: | 34 S/s to 34 MS/s | Timing: | 34S/s to 34MS/s |
| Functions: | Record, edit and playback | Functions: | Record, edit and playback |

**CIRCLE NO 81**

# Digital synthesizer aids testing of complex analog, digital circuits

*A digitally based signal synthesizer (DSS) provides the test engineer with a high degree of flexibility in the generation of test signals. When used with a digitizing scope, the DSS greatly simplifies the testing of complex analog and digital circuits such as those found on pc boards for hard-disk-drive applications.*

Al Kovalick, *Hewlett-Packard Co*

Tester versatility is particularly important for the test engineer dealing with boards containing both analog and digital circuits. In the production environment, a test engineer normally has the choice of four primary approaches to board testing:

- In-circuit testing. Technicians in the actual target environment test and debug the boards. No actual tester is involved. In-circuit testing is low cost.
- Universal board testing. Universal board testing means a complete, integrated system for complex, general applications. Primarily used for device testing, these types of testers can also handle some functional tests. A universal board tester is expensive.
- Custom, one-of-a-kind, functional testing. Usually dedicated, one-of-a-kind testers don't see much use. They are moderately priced.
- Semicustom functional testing. Semicustom types of testers can usually handle several board types, see medium use, and feature programmable signal stimulus. The cost is moderate.

The choice of a tester depends on several factors. Among these are board complexity, board type (analog, digital, or mixed), frequency range (low, RF, or microwave), production volume, margin-testing requirements, and device or function-level testing requirements. Furthermore, if board adjustments are necessary, a functional test environment is usually required. Testing the boards over a range of input parameters—rather than simply at typical values—adds the assurance of product robustness. For these cases, a functional tester with wide control over input parameters is useful.

## Testing mixed analog and digital circuitry

The semicustom functional tester is especially useful in situations where both analog and digital circuitry need to be tested—in disk-drive systems, for example. It provides a nondedicated, functional test system adaptable to board changes or to entirely new boards with the same board test system. You won't find a hard and fast definition for the semicustom tester, but it usually includes a digital multimeter (DMM), an analog signal source, a digitizing scope, and a digital word source and analyzer.

Most test engineers are keenly aware of the measurement flexibility that digitizing scopes offer. The more recently introduced DSS presents a flexible means of generating programmable analog signals. The combina-

*As a complement to the digitizing scope, the digital signal synthesizer offers test engineers a flexible means of generating complex analog and digital signals.*

tion of a digitally based source and analyzer provides a still higher order of flexibility.

The inclusion of a digital synthesizer in a semicustom tester lets you generate a wide range of signals. You can tailor these signals with a selectable level of added noise, jitter, offset, and other characteristics. And, with carefully controlled anomalies superimposed upon the ideal signal, you can test the board's performance with a superior degree of integrity. As an aid to board adjustment and calibration, digital synthesizers offer calibration-quality signals. For example, synthesizers can easily generate precision reference signals with AM, PM, FM, phase shift, and noise. The quality of the reference signal depends only on the spectral purity of the synthesizer's output.

To better understand the digital signal synthesizer,

consider its similarity to the compact disk (CD) player:

- The CD player has a rotating disk, which contains information that the laser reads. The information —in this case, music—is imprinted on the disk in the form of digital data. In a digital synthesizer, very fast memory replaces the rotating disk. The memory contains digital words that are played back in a sampled system.

- In a CD player, the sample data rate is 44.1 kHz, which corresponds to a sample every 22.6 $\mu$sec. In the DSS, the sample rate is 125 MHz, or a new sample every 8 nsec.

- CD players feature two 16-bit DACs, one for each stereo channel. The DSS employs one 12-bit DAC, largely because 16 bits is neither required at these extremely high rates nor possible given the

## Testing disk-media certifiers

Both manufacturers of disk media and drive manufacturers who buy disk media need a way to test the quality of the drives' magnetic surfaces. There are established industry specifications for testing the media, and several manufacturers supply media certifiers.

Many tests are performed before a disk surface passes a quality check. Two tests that are usually needed to qualify a surface are the missing- and extrabit tests. **Fig A** shows a portion of a 16.66-msec code-bit sequence with two transitions reduced by 50%. The sequence is at a transition rate of 20 MTPS (million transitions per second). This signal has about 333,000 transitions per disk rotation.

You can input the missing-bit signal to the certifier hardware to verify its integrity over a range of reduction levels and a range of missing bits per revolution. Certifiers can be programmed to detect missing bits

at a user-defined level. A good test of the certifier's ability to detect such missing bits is to send it a succession of signals, each with bit-reduction levels near the desired setting. In practice, the certifier will mark some bits as missing and some as not missing.

For example, assume that the certifier's missing-bit threshold is set to 50%. Now, send it several signals, each having a dif-

ferent, but known, bit reduction between 45 and 55%. You can determine the certifier's accuracy by noting its response to each signal.

Also of interest are the extrabit test, positive- and negative-modulation tests, the peak-shift test, and the AGC test. A well-designed digital signal synthesizer can produce signals for all of these tests.



Ch. 1     = 100.0 mvolts/div
Timebase  = 150 ns/div
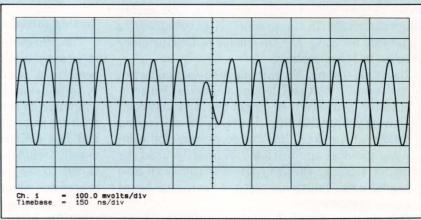
*Fig A—This waveform shows two missing bits at 50% reduction. This type of signal is suitable for calibrating disk certifiers.*

present state of the art.

- Most CD players have a sequencer that lets you play back the tracks in any order. The DSS has a sequencer that permits the playback of waveforms in any order.
- Both the CD player and the DSS use lowpass filters to reject all the sampling energy, and both have output amplifiers.

## Testing disk-drive boards

As mentioned, DSSs are ideal for applications such as rigid-disk-drive testing. Disk-drive circuits require analog signals that are impossible to produce using conventional signal synthesizers or function generators. The addition of a DSS to a test system lets you create these signals and also provides more versatility than is otherwise possible.

Traditional Winchester-type drives have two types of read channels—data and servo. A companion read-data or read-servo board processes each channel. The servo system positions the read head exactly over the desired track. The read-data channel includes a mix of analog and digital circuitry (**Fig 1**). Because the read-data signals are not trivial in nature, a digital synthesizer is a perfect candidate as a source of such signals. The servo-channel signals are also quite complex. Typically, the test engineer has to develop signals with varying

data patterns, dropouts, jitter, and bit shift. You can use these signals for board-calibration adjustment as well.

The basic read-head signal results from changing media flux. If the signal is derived from a conventional ferrite head, the voltage-vs-time response to a flux change is a Lorentzian or modified Lorentzian pulse, which is best approximated by the $\sin^3$ waveform of **Fig 2**. (A DSS generated all the waveforms of **Fig 2** through **Fig 7**.) The $\sin^3$ waveform needs a third harmonic for sufficient fidelity. For thin-film heads, the $\sin^3$ may be an insufficient approximation and other pulse models may be needed. Alternatively, a digital synthesizer



Ch. 1 = 500.0 mvolts/div
Timebase = 20.0 ns/div
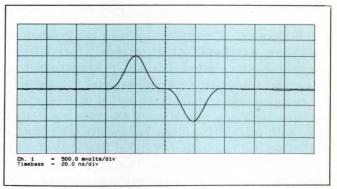
*Fig 2—In this waveform of two isolated read-head transitions, the signal is modeled with a sin³ pulse doublet.*
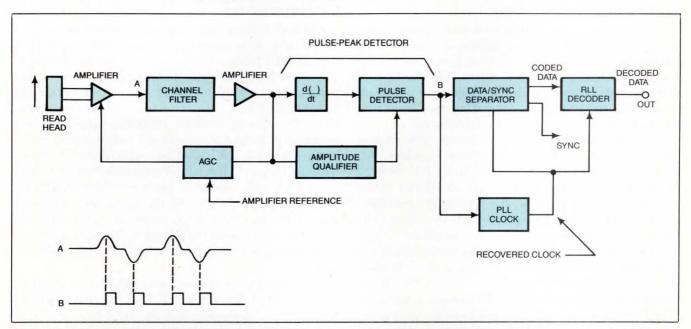


*Fig 1—This typical read channel of a Winchester disk drive shows the functional blocks required for processing the complex signals from the read head.*

*The DSS can easily generate precision reference signals with added AM, PM, FM, and phase-shift characteristics.*
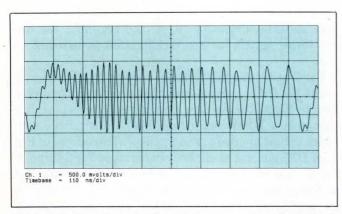


**Fig 3—This filter-test waveform** *plots 50 tones of equal amplitude spanning dc to 50 MHz. To generate a composite signal with a small-amplitude peaking factor, each tone is phase compensated.*



**Fig 4—Following the rules for RLL (2,7) coding,** *this waveform shows the typical coded data from the read head. Each transition is treated as a logic 1; no transition is treated as a 0. After any transition, at least two logic 0s follow—to a maximum of seven.*

with 512k points of waveform memory can generate a 4-msec-long waveform that is completely user defined (the sampling-clock rate is 125 MHz). Using the memory-sequencer function within the digital synthesizer, you can generate a 16.66-msec signal that typically corresponds to one revolution of the rotating media. Also, with a 50-MHz output bandwidth, the digital synthesizer can generate a 2f signal (the highest data rate) of approximately 16 MHz. The third harmonic for a $\sin^3$ signal would be 48 MHz, very near the band edge of 50 MHz.

### Testing the read channel filter

Next, consider a few examples of read-channel waveforms. (All the following read-channel waveforms were generated with the HP Waveform Generation Language (WGL).) For long waveforms, the duration of which exceeds 4 msec, the memory sequencer was used. Under these circumstances, generating waveforms that last hundreds of milliseconds is relatively easy.

Referring back to **Fig 1**, the channel filter usually consists of a lowpass filter with a phase equalizer. You can test the filter characteristics using a synthesizer, a digitizing scope, and a software-driven Fourier transform algorithm. In this case, the synthesizer generates a special signal that passes through the filter. The generated signal has about 50 equal-amplitude tones, which are uniformly spaced across the desired measurement bandwidth. This signal has special merit because of its unique phase characteristics. It is a broadband signal with the phase of each frequency component selected so as to minimize the peak-to-peak range of the composite signal (see **Fig 3**). The DSS is the ideal instrument to generate such a signal.

Next, the scope captures the filter output and converts the result into a frequency-domain representation using a Fourier transform (that is, time-to-frequency) software algorithm. The frequency-domain information contains the filter amplitude and phase characteristics. The input to the filter under test is a signal with known-amplitude and -phase characteristics vs frequency. Any deviation from this signal at the filter output defines the transfer function. This method achieves the same result as a network analyzer would produce.

### Data patterns vary

Although a discussion of coding is beyond the scope of this article, it is important to note that run length limited (RLL) codes are the rule in today's disk drives. The use of RLL codes has enabled disk-drive designers to pack data very efficiently onto the platter surface. As an example, **Fig 4** shows an RLL (2,7) code sequence. Here, the spacing between magnetic transitions is a minimum of 2 and a maximum of 7 code-cell positions—hence the RLL 2,7 identifier. All transitions occur within a code cell, but not all code cells contain transitions. Code cells mark the locations where transitions *may* occur, but not necessarily where they *do* occur. Part of the beauty of RLL coding is that transitions cannot be too close or too far apart. Transition density is intelligently traded for transition-position information.

The DSS easily defined and generated the data stream of **Fig 4**. You can modify data patterns at will for testing the RLL decoder and for worst-case testing of frequency tolerance levels of the phase-locked loop. The loop oscillator output is the recovered clock source. The
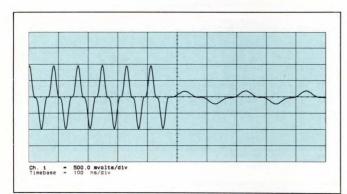
*Fig 5—This AGC-test waveform has a 5:1 amplitude reduction and a 2.5:1 frequency reduction. The amplitude step serves to test the AGC attack time.*



(a)



(b)

*Fig 6—The pulse stream shown in **a** has pulses A and B shifted in time by 3.5 nsec compared to all other pulses. The small shift is difficult to see. The signal in **b** results from the shifted-minus-unshifted operation. The result, E(t), has a peak amplitude of 128 mV, as predicted for a 3.5-nsec shift. Also, for all pulses other than A and B, E(t) is zero. E(t) provides proof that pulses A and B are indeed shifted.*

loop must stay locked to the desired frequency without drift, even though the input data pattern varies wildly. Initially the loop is locked to a sync sequence. A thorough test of the channel filter and the phase-locked loop would require a sync frame, which consists of a series of pulses onto which the loop locks. It is usually located in the preamble to the data block. For margin testing, you can design the sync frame with aberrations on the individual pulses.

Besides testing filter characteristics, you also need to test **Fig 1**'s AGC block. Using the code sequence of **Fig 5**, you can test three important AGC parameters: amplitude dynamic range, attack time, and amenity to frequency deviations. As shown. the amplitude changes by a factor of 5:1 during an abrupt step. You can use one of the DSS markers to indicate the amplitude change and to trigger a scope to measure the AGC response.

## Checking bit-shift susceptibility

Another area of interest is the window margin, or phase margin. The window in question is the width of the code-cell detection window in which a head transition is detectable with a high degree of certainty. Ideally, the transition will occur in the center of the window. The phase-locked-loop clock is used to identify the center of the detection span. All physical systems, however, have bit shift. This shift locates the detected bit off the ideal center. If too much shift occurs, the system will generate a read error.

Although a complete window-margin test needs the head disk assembly, a DSS can assist in testing the read channel for bit-shift susceptibility. **Fig 6a** shows 10 transitions isolated from a long bit stream that the DSS generated. Pulses A and B are shifted by 3.5 nsec compared to the other peaks. This small shift is difficult

to detect visually. Even smaller bit shifts make the shifted bit stream that much more difficult to observe.

One method for proving that the selected pulse or pulses have been shifted by the desired amount compares an unshifted sequence with a shifted one. The comparison takes the form of a subtraction: E(t)=unshifted sequence−shifted sequence. The difference error signal, E(t), is a direct function of the shifted sequence.

If you model the transition pulse stream as a $\sin^3$ shape and the shift is accomplished by phase shifting only the desired pulse by an amount $\alpha$, then

$$E(t)=(\sin\Omega t)^3-(\sin\Omega t+\alpha)^3, \qquad (1)$$

where $\omega$=pulse rate in rads/sec, $\alpha=\alpha_0$ phase shift in rads during the shifted pulse, and $\alpha=0$ during the unshifted portions.

You can expand E(t) by using trigonometric identi-

*Although a complete window-margin test needs the drive's head-disk assembly, a DSS can assist in testing the read channel for bit-shift susceptibility.*

ties. Assuming that $\alpha$ is $\leq 18°$, which is 10% of a pulse width, E(t) reduces to

$$E(t)=4/3\alpha\,(-\cos\Omega\,t+\cos3\Omega\,t). \qquad (2)$$

For larger pulse time shifts, you can calculate E(t) directly from **Eq 1**. It is obvious from **Eq 2**, however, that E(t) is a direct function of $\alpha$. The maximum amplitude of E(t) is a direct measurement of the time shift between the unshifted and shifted pulses in the sequence. By differentiating **Eq 2** and solving for its peak amplitude, you get a value that can be conveniently measured on a scope. Solving for the positive peak voltage yields $E(t)_{max}=1.16\alpha$.

To measure E(t) in a real system, though, you must first generate the unshifted sequence, and then capture it on a digitizing scope. The waveform is stored in waveform memory 1. Next, the shifted version is generated and stored in waveform memory 2. If the scope has sufficient vertical resolution, say eight bits, and you use digital averaging, then E(t)=waveform memory 1−waveform memory 2, as viewed on the scope.

**Fig 6b** displays E(t) as computed by the above method, with a 3.5-nsec time shift on pulses A and B (see **Fig 6a**). The $\alpha$ (time shift) for that pulse equals 0.11 rads, and $E(t)_{max}=127$ mV. Measuring E(t) in **Fig 6b** yields 128 mV. So indeed, pulses A and B have shifted by the desired amount. Note that E(t) equals 0 for all other pulses, indicating no time shift other than where it is required.

Using this method, you can successfully measure differential time shifts down to 100 psec. Also, by choosing a proper alpha ($\alpha$), it's possible to generate pulse time shifts with 10 psec of resolution, despite the fact that DSS systems have discrete sampling rates. For example, although the HP 8770A has a sampling clock of 8 nsec, you can achieve very small time shifts (less than the sample clock) using this method. To achieve this extremely fine time-shift resolution, a DSS with a spectrally clean passband (low spurious content) and good amplitude resolution (12 bits) is required. Moreover, nonlinear phase response in the DSS may severely distort $\sin^3$ pulses. In fact, the $\sin^3$ pulse sequence is an excellent waveform for observing the effects of passband phase nonlinearity. Any non-symmetry around a pulse peak is a result of phase nonlinearity. Besides testing the read data board for bit-shift susceptibility, you can use time-shifted sequences to test the phase-locked loop's transient response to either an impulse or a step in phase shift.



Ch. 1 = 500.0 mvolts/div
Timebase = 750 ns/div
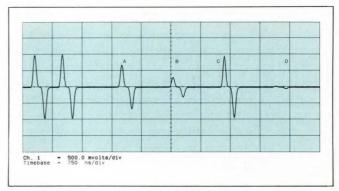
*Fig 7—This servo pattern shows two sync pulses followed by four additional pulses. Pulses A, B, C, and D serve to achieve head-track alignment.*

As mentioned earlier, the disk-drive servo system's function is to achieve good track-head alignment. Servo signals in Winchester disk drives are quite complex. The waveform of **Fig 7** shows a portion of a servo read signal. The two left-most pulses are sync pulses. The heights of the other four pulses—labeled A, B, C, and D—are a function of the track-head alignment.

One particularly useful signal is the servo-head output during a track-seek operation. The head moves perpendicular to all tracks as it travels toward a final destination track. As the servo head seeks, the A, B, C, and D pulses move up and down in amplitude, somewhat like the pistons in a 4-cylinder car. In fact, the A, B, C, D pulse-set repeats its 4-banger motion after every four tracks.

By selecting a DSS that has a full-feature memory sequencer, you can generate a servo signal that exhibits complex crossing characteristics, such as the long-duration (25 msec) signals necessary for track-to-track seek operations. This type of signal is useful in testing the servo system's ability to find the desired destination track. At no time is the head disk assembly needed. Signal characteristics may include acceleration, deceleration, constant velocity, and A-B-C-D pulse profiles. In addition, you can determine open servo-loop transfer-function characteristics using a DSS as a complex signal source.

Part of the beauty of a DSS-based test system comes from its inherent repeatability. Over time and from tester to tester, system specifications change minimally. The tester-to-tester specification match is very good. Test engineers who must specify systems that are built offshore find this feature indispensable. Of course, to guarantee the tester's integrity, you must choose a DSS with a completely specified output passband—that

is, both the amplitude and phase vs frequency should be specified, as well as any harmonics and spurious signals.

Semicustom tests, such as those described here, will likely find wider acceptance as engineers become familiar with the advantages of digital signal synthesizers. In addition to disk-drive-board testing, for example, a test system using digital signal synthesis lends itself to many other applications, including streaming-tape drives, video processors, adaptive filters, radar processors, and high-speed modems. **EDN**

## Author's biography

*Al Kovalick is a research and development engineer with the Stanford Park Div of Hewlett Packard. He has been with HP for the past 14 years and currently works as a systems architect and hardware designer. Al has a BSEE from California State University at San Jose and an MSEE from the University of California at Berkeley. He studies and teaches bible topics, and he enjoys sailing in San Francisco Bay.*

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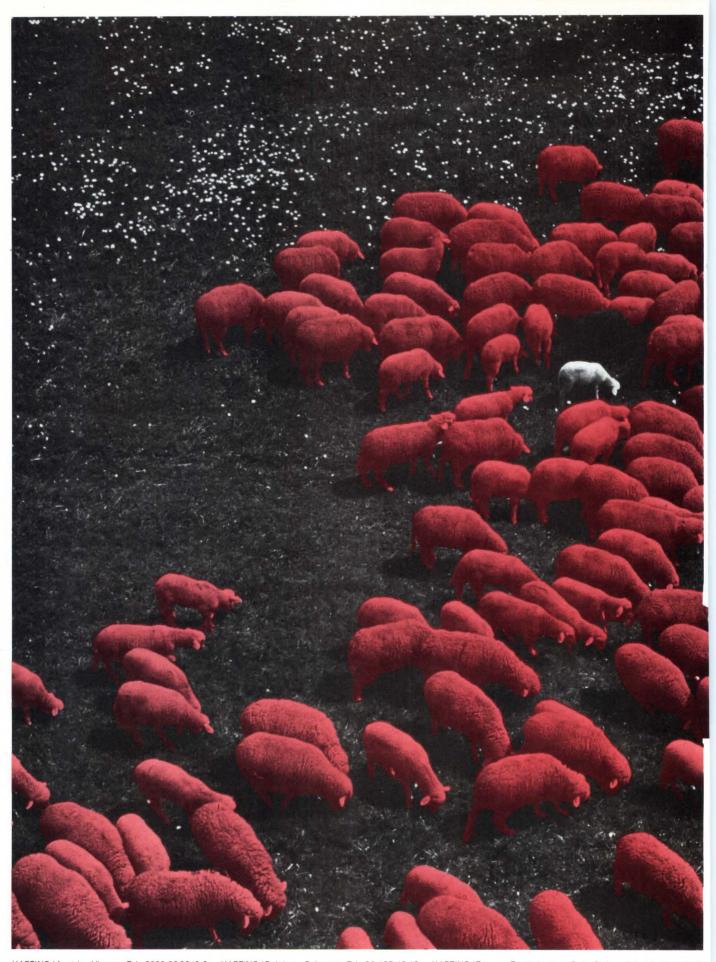
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# DESIGN IDEAS

# Dual potentiometer controls up/down counter

Kenneth W Robbins
*ANRO Engineering Inc, Lexington, MA*

The circuit in **Fig 1** uses what would normally be a miswired potentiometer to control both the counting rate and direction of a counter. Note the wiring scheme of the section of the dual linear-taper potentiometer connected to the 7555 timer. This section controls the 7555's pulse rate. The values shown in **Fig 1** ensure that the timer will not output pulses when the potentiometer is at its midpoint; turning the potentiometer in either direction from its midpoint raises the voltage at the 7555's pin 7 and allows the IC to operate. Thus the potentiometer functions as an analog fine-tuning control for circuits that need a digital input.

At the potentiometer's midpoint, its other section does not upset the biasing of the inverter $IC_{2C}$, which is in its linear region. As long as this inverter is in its linear region, it, along with $IC_{2D}$ and the 1.0-$\mu$F capacitor, forms a low-repetition-rate oscillator. While this portion of the circuit oscillates, it alternately blinks the up and down LEDs (which indicate to the operator that the counter is not counting).

Turning the potentiometer in either direction from its midpoint changes the biasing on the inverter, taking it out of its linear region. Depending on the direction of turning, either the up or down LED will light. Further rotation causes the timer to begin emitting pulses, which flash the clock-pulse LED. The RC values shown and the dead band between lighting the up or down LEDs and lighting the clock LED allow an operator to produce just a single up or down count.

Because of potentiometer tolerances, you may need to connect a high-value resistor between the inverter potentiometer's wiper and ground or 5V, as appropriate, to achieve symmetrical control action; this unit required the 470 k$\Omega$ shown.   **EDN**

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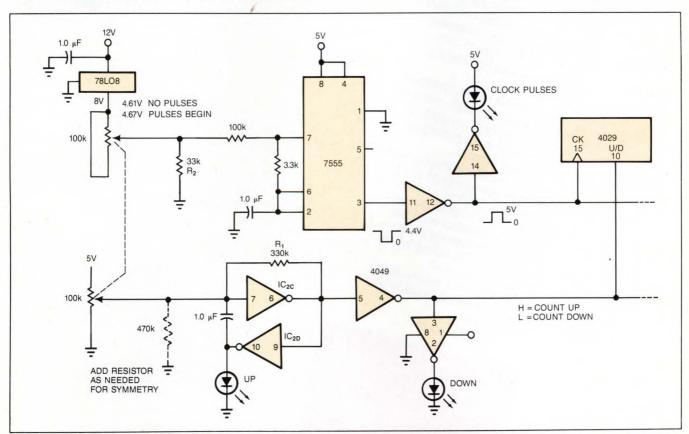


*Fig 1—The dual-section potentiometer* controls both the direction and count rate of the 4029 counter. When the potentiometer is at its midpoint, the 7555 timer is biased off, and the inverters driving the up and down LEDs function as a low-repetition-rate oscillator to alternately blink the LEDs, which signals that the counter is not counting.

# DESIGN IDEAS

# Circuit lowers photodiode-amplifier noise

Rod Burt and R Mark Stitt
*Burr Brown, Tucson, AZ*

Adding two passive components to a standard photodiode amplifier reduces noise (**Fig 1a** and **b**). Without the modification, the shunt capacitance of the photodiode reacting with the relatively large feedback resistor of the transimpedance (current-to-voltage) amplifier creates excessive noise gain.

The improved circuit (**Fig 1b**) adds a second pole, formed by $R_3$ and $C_2$. The modifications reduce noise by a factor of 3. Because the pole is within the feedback loop, the amplifier maintains its low output impedance.

If you place the pole outside the feedback loop, you have to add an additional buffer, which would increase noise and dc error.

The signal bandwidth of both circuits is 16 kHz. In the standard circuit (**Fig 1a**), the 1-pF stray capacitance in the feedback loop forms a single 16-kHz pole. The improved circuit (**Fig 1b**) has the same bandwidth as the first circuit, but exhibits a 2-pole response.

If you set $C_1R_2 = 2C_2R_3$, the transimpedance transfer function is a 2-pole Butterworth (maximally flat in passband) type. At dc, both circuits' gain is 140 dB or 10V/μA. The frequency response of both circuits is 3 dB down at 16 kHz. The conventional circuit rolls off at 20 dB/decade; the improved circuit rolls off at 40 dB/decade.

**Fig 2** shows the noise gain of both circuits. The noise zero occurs at

$$f_Z = \frac{(R_1+R_2)}{2\pi\,R_1R_2(C_0+C_1)},$$

about 673 Hz for this example. Both curves do, indeed, show peaking at about 673 Hz because of the zero formed by the photodiode shunt capacitance. The added pole of the improved photodiode amplifier rolls off the



*Fig 1—The standard photodiode transimpedance amplifier circuit* in **a** *exhibits excessive noise because of the shunt capacitance of the photodiode. The improved circuit in* **b** *adds a second pole in the feedback loop to roll off the circuit's noise gain above its signal band limit.*
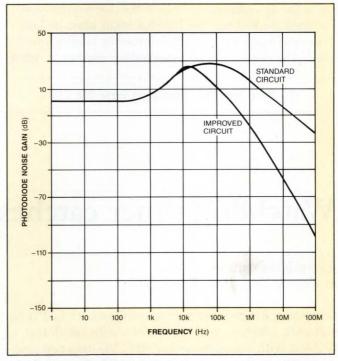


*Fig 2—The improved circuit in 1b has one-third as much noise as the circuit in Fig 1a.*

# DESIGN IDEAS

noise above 20 kHz—well above the circuit's signal bandwidth of 16 kHz.

Another advantage of the improved circuit is its ability to drive a capacitive load. Because the output of the circuit connects to a large-value capacitor, driving a little extra capacitance presents no stability problems. Although the output has low dc impedance, the load affects the ac transfer function. But with reasonable loads, the effect is minimal. With the values shown in **Fig 1,** a load of 10 kΩ in parallel with 100 pF has little effect on the circuit's response. **EDN**

**To Vote For This Design, Circle No 749**

# XOR gates add up/down function

Dil Sukh Jain
*National Remote Sensing Agency, Hyderabad, India*

You can transform an ordinary binary counter, such as a 7493, into an up/down counter with mode control by adding XOR gates (7486) to the counter's outputs (**Fig 1**). The circuit in **Fig 1** counts up when the DN/UP line is low and down when the DN/UP line is high.

To use the 7493 counter to count out its maximum count length (0-15), connect the $Q_A$ output to the $B_{IN}$ input and apply clock pulses to the $A_{IN}$ input. The RESET input, when high, inhibits the count inputs and simultaneously returns the ouputs $A_O$ through $D_O$ to low in the up-count mode or 15 in the down-count mode. For normal counting, the RESET input must be low.

You can easily cascade this counter by feeding the $Q_D$ line to the clock input of a succeeding counter. **EDN**

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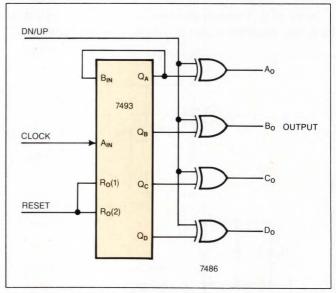


*Fig 1—Adding XOR gates to a counter's outputs transforms an ordinary binary counter into an up/down counter with mode control. This circuit counts up when the DN/UP line is low and down when the DN/UP line is high.*

# Watchdog timer catches I/O-chip crashes

Barry Kaufman
*Multipath Inc, Pine Brook, NJ*

Common watchdog-timer circuits will restart a μP if its software crashes, but the timers will not detect a problem with a programmable chip. I/O lines can inadvertantly serve as antennas to outside disturbances such as power surges, lightning hits, or even cosmic rays. These disturbances can disrupt the control registers of programmable I/O ICs such as UARTS, disk controllers, and RS-232C or RS-488 interfaces without crashing the main program.

You can use two methods to extend your watchdog timer's coverage to include programmable ICs. You could strobe the watchdog timer via an unused I/O line rather than directly from the μP. That way, if the I/O

chip malfunctions, the watchdog timer will time out and restart the µP. Naturally, you must include a subroutine to reinitialize the I/O chip in the watchdog-timer routine.

Or you can take advantage of most I/O ICs' control-register readback function. The Z80 routine in **Listing 1** periodically reads the control registers, compares their present contents to their initial contents, and branches to the initialization code if there is a difference. A convenient location for this type of routine is right after the code that generates the watchdog timer's strobe.

**EDN**

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**LISTING 1 — Z80 ROUTINE**

```
        EXAMPLE OF RE-INITIALIZING I/O IC CONTROL REGISTERS IF AN
        UNKNOWN CHANGE IS DETECTED.  FOR THIS EXAMPLE, ONE INTEL
        82C55 IS PROGRAMMED SO ALL 24 I/O LINES ARE INPUTS AND A
        SECOND 82C55 IS PROGRAMMED SO ALL I/O LINES ARE OUTPUTS.


* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*                                                               *
* ; PART OF INITIALIZATION ROUTINE THAT IS RUN ONCE WHEN        *
* ; THE PROGRAM IS STARTED, AFTER A HARDWARE RESET.             *
* ;                                                             *
* INIT:                          ; Start of initialization code.*
* ;                                                             *
* ;                                                             *
* ALLIN:     EQU  9BH            ; Mode 0, all pins are input.   *
* ALLOT:     EQU  80H            ; Mode 0, all pins are output.  *
* INPOR:     EQU  03H            ; Port address for input I/O    *
*                                ; IC control register.          *
* OTPOR:     EQU  0BH            ; Port address for output I/O   *
*                                ; IC control register.          *
* WDPOR:     EQU  10H            ; Port address to strobe        *
*                                ; watchdog timer IC.            *
* ;                                                             *
*            LD A,ALLIN          ; Load accum. with control byte.*
*            OUT (INPOR),A       ; Send it to input IC.          *
*            LD A,ALLOT          ; Load accum. with control byte.*
*            OUT (OTPOR),A       ; Send it to output IC.         *
*                                                               *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *


* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*                                                               *
* ; PART OF THE MAIN PROGRAM LOOP.  THIS CODE MUST BE           *
* ; RUN OFTEN ENOUGH TO KEEP THE WATCHDOG TIMER FROM            *
* ; RESETTING THE CPU.                                          *
* ;                                                             *
*            OUT (WDPOR),A       ; Strobe the watchdog timer.    *
* ;                                                             *
*            IN A,(INPOR)        ; Read input IC ctrl. register. *
*            CP ALLIN            ; Compare with what it should be.*
*            JP NZ,INIT          ; NZ = not same so reinitialize.*
*            IN A,(OTPOR)        ; Read output IC ctrl. register.*
*            CP ALLOT            ; Compare with what it should be.*
*            JP NZ,INIT          ; NZ = not same so reinitialize.*
* ;                                                             *
*                                ; Continue with main program loop.*
*                                                               *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
```

# DESIGN IDEAS

# Spare flip-flop forms inverter

Gary San Giacomo
*Electro-Biology Inc, Parsippany, NJ*

The circuit in **Fig 1** uses one-half of a dual D flip-flop as an inverter. When the input goes low, the flip-flop resets, and its $\overline{Q}$ output goes high. When the input goes high, the reset line is released and $\overline{Q}$ gets clocked low.
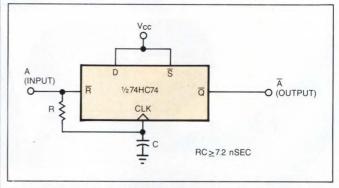


*Fig 1—Adding a simple RC delay line to a spare flip-flop transforms it into an inverter with a maximum frequency of 10 MHz.*

The RC delay between applying the input signal to the flip-flop's reset input and its clock input enables clocking the flip-flop on the input's positive edge. A 74HC74 dual D flip-flop, for example, requires a minimum recovery time of 5 nsec after releasing the reset input before strobing its clock input. Therefore, specing RC at ≥7.5 nsec provides adequate margin. The slight slowing of the clock edge presents no problem, because the clock input's maximum allowable rise time is a much longer 500 nsec. To prevent skewing of the output's symmetry, you should limit the maximum input frequency to less than 10 MHz.  **EDN**

**To Vote For This Design, Circle No 747**

## Extending the Applications of 5V Powered RS232 Transceivers

### High Speed Operation

Although the EIA RS232 specification is for a relatively slow communications protocol, many applications require RS232 transceivers to operate at higher frequencies. Devices such as the LT1080, LT1081, and the LT1130 series share a common design for the drivers and receivers and are capable of operating over 100 kilobaud.

Although the slew rate is controlled for all of the Linear Technology series of RS232 communications devices, for output levels limited to ±6V the transition time is fast enough to allow high baud rates. With a slew rate of approximately 10V per microsecond, it only takes 1.2 microseconds for a 12V excursion. The two photos (Figure 1 and Figure 2) show the output waveform and delay associated with a 75kHz square wave input and a 100kHz square wave. Delay times are in the order of 0.5 microseconds and the total slew time is approximately 1.2 microseconds. Output load is 3k. Receivers are much faster and can handle these baud rates with no problem. For higher communication rates, a differential signal is recommended.

### Power Supply Tricks

The power supply generator on 5V powered devices is a charge pump circuit which generates approximately ±9V from a single 5V supply. Parallel operation of the supply charge pumps for 5V powered transceivers is easily achieved to minimize component count. The positive and negative supply have approximately 1μF of holding capacitance for energy storage. If several devices with charge pumps are used in the same system, the output supplies may be paralleled into a single pair of common energy storage capacitors.
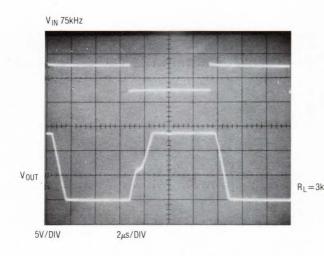


Figure 1. Operation at 75kHz
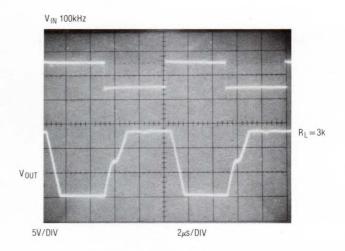


Figure 2. Operation at 100kHz

Figure 3 shows two LT1080's with common power supply capacitors for energy storage. Twice the output current is available for external use. This eliminates two capacitors from the system. Individual charge pump capacitors are still needed on each of the devices.

## Operation with +5V and +12V Supplies

The charge pump circuitry takes the input 5V and doubles it. The doubled voltage is then inverted to obtain a negative output. The only reason for doubling the input is to ensure adequate positive and negative output voltage to meet RS232 specifications. In PC systems, where +12V is available, the internal voltage doubler does not need to be used. The device may be connected directly to a +5V and a +12V supply. The +12V is then inverted to obtain approximately −11V. This eliminates one charge pump capacitor and one holding capacitor for the 12V output. Figure 4 shows an LT1080 connected to a 12V and 5V power supply. The +12V is connected into one of the charge pump capacitor pins rather than the 12V output pin. Supply current also decreases to about 9mA.
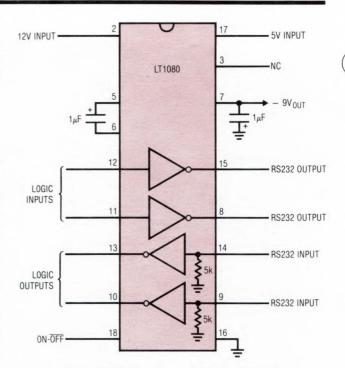


**Figure 4. Operation with +12V and +5V Supplies**
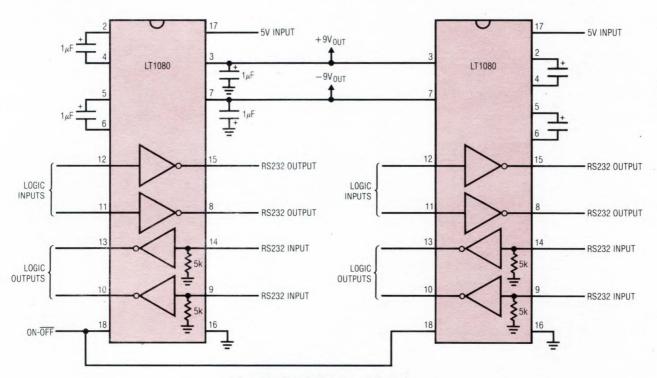


**Figure 3. Paralleling Power Outputs**

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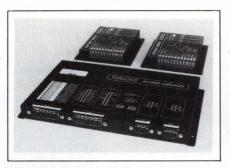
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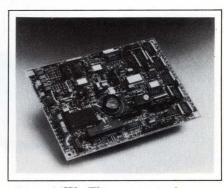
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sumes 14W. The converter's accuracy is ±0.05% FS. The pc board that holds the converter measures 35in². $2534 (25).

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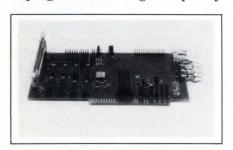
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- *Provides a 14-bit ADC and DAC*

The DSP/AIB board provides data acquisition for an IBM PC, PC/XT, or PC/AT that uses TI's TLC32040 (or TLC32044) analog I/O chip. It features an ADC and a DAC, each

with a 14-bit dynamic range. The board directly replaces a codec chip or interface. It can sample up to 20 kHz synchronously and asynchronously. The board interfaces with most DSP boards through a serial interface. Acquisition can occur at 20 kHz in single-channel mode and at 10 kHz in dual-channel mode. In addition, the board provides a 50-pin parallel interface for I/O. You can connect up to five boards to the parallel bus for a 10-channel max sampling at 10 kHz or 5-channel max sampling at 20 kHz. The analog input has an antialiasing filter with a programmable high-frequency

cut-off from 3.6 to 10 kHz. The analog output has a SinX/X filter with a 10-kHz cutoff. $495.
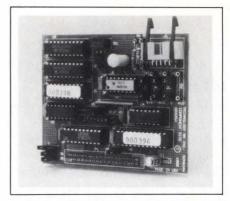
**Sonitech International Inc,** 83 Fullerbrook Rd, Wellesley, MA 02181. Phone (617) 235-6824. TWX 650-328-1622.

**Circle No 354**

### SBX MODULE

- *Decodes outputs from an incremental quadrature encoder*
- *Provides a 4-stage digital filter*

The Model 4324 SBX bus expansion module for interfacing an incremental quadrature encoder accepts either TTL or CMOS inputs. It has a presettable 24-bit synchronous up/down counter for pulse counting or for quadrature pulse decoding. The maximum input rate is 333 kHz in the quadrature decode mode and 2 MHz in the count mode. The module can generate interrupts for an index

pulse, an overflow or an underflow condition, or when the count value matches a presettable value. In addition, the board has a 4-stage digital filter for noise reduction in an industrial environment. The module mounts directly on the company's model 4312 quadrature input card for the STD Bus. $220.

**Technology 80 Inc,** 658 Mendelssohn Ave N, Minneapolis, MN 55427. Phone (800) 328-4827, ext 1680; in MN, (612) 542-9545.

**Circle No 355**

## DAUGHTER BOARD

- *Provides a TMS320C17 development system*
- *Features 256k words of on-chip memory*

The 320/PC-17 daughter board, when used with the vendor's algorithm development package (ADP), lets you develop software and hardware with the Texas Instruments' TMS320C17 DSP microcomputer. The board features a 256k-word, on-chip RAM; a 4k-word ROM; and an 8k-byte program RAM. The board's DSP features a serial port

with a timer and a coprocessor interface and lets you access off-chip RAM. The board's utility software includes a debugger, a line-by-line assembler, a signal editor, and other utility tools. $895.
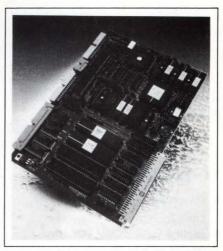
**Atlanta Signal Processors Inc,** 770 Spring St, Atlanta, GA 30308. Phone (404) 892-7265.

**Circle No 356**

## DSP BOARD

- *Employs both scalar and vector processors*
- *Computes a 1024-point FFT in 1.070 msec*

By employing a hybrid architecture containing a 12.5-MHz ADSP2100 scalar processor and two 25-MHz ZR34161 vector processors, the DBSVSP-1 digital-signal-processing board can compute a 1024-point FFT spectral analysis (including windowing and magnitude calculations) in 1.070 msec. As a result,



you can use the board to analyze analog signals with bandwidths of approximately 0.5 MHz in real-time applications. To increase throughput, you can operate multiple boards in serial or parallel. The board has an onboard FIFO buffer and dual-port RAM, and it offers direct interfaces for 12-bit ECL- or 16-bit TTL-level data. Interfaces to either the VME Bus or the AT bus

are available on a separate card that can control as many as four of the DSP boards. From £3500.

**Data Beta,** Unit 7, Chiltern Enterprise Centre, Theale, Berkshire RG7 4AA, UK. Phone (0734) 303631. TLX 849021.

**Circle No 357**

## I/O BOARDS

- *Provide industrial I/O for Multibus II systems*
- *Incorporate 2500V isolation from the Multibus II system*

The FAB410 and FAB420 are respectively an optically isolated digital input board and a relay isolated output board for Multibus II systems. The FAB410 provides you with two groups of 16 digital inputs. The first four inputs of each group can generate system interrupts on either their rising or falling edges. The inputs accept 24V inputs, but can be optionally reconfigured to operate with 12 or 48V inputs. Optocouplers on the inputs provide 2500V isolation between the inputs and the Multibus II system, and a programmable digital filter with a time constant of between 10 μsec and 300 msec is provided after the optical isolation. Built-in self-test facilities allow you to apply standard voltages to the inputs and disconnect the input ground line. The FAB420 output board provides four groups of eight outputs. Each output comprises a 120V/1A relay, which provides 2500V isolation from the Multibus II system. Both boards incorporate displays that allow you to monitor the states of their inputs or outputs. FAB410, Fr 6800; FAB420, Fr 8500.

**Centralp Automatismes,** 16 rue Gabriel Péri, 92120 Montrouge, France. Phone (1) 42533617. TLX 632380.

**Circle No 358**

## DISK DRIVES

- *Have capacities of 374M, 689M, and 840M bytes*
- *Furnish data-transfer rates to 2.4M bytes/sec*

The R8600 Series disk drives are compatible with IBM RT/PC computers. They contain disk controllers and have SMD interfaces. You can configure the controllers to control any combination of four drives. You can transfer data to the drives at a 2.4M-byte/sec max rate. They have a 15-msec average access time and come in three disk capacities: 374M, 689M, and 840M bytes. They are compatible with IBM PC/AT-Bus computers. In addition, the drives provide compatibility with DOS, SCO Xenix, and Novell 2.1 operating systems. $5900 to $9900 (OEM).

**CFN Industries,** 30-A Lindbergh Ave, Livermore, CA 94550. Phone (415) 443-1672. TLX 821892.

**Circle No 359**

## MEASURING UNIT

- *Uses ultrasound to locate objects 30 ft away*
- *Communicates with a computer via an RS-232C link*

The UDM-RMU (remote measurement unit) distance-measuring device communicates with a controller over an RS-232C link. It uses two Polaroid ultrasonic transducers to locate objects from 0.5 to 30 ft away with an accuracy of ±1% and a resolution of .05 in. The unit calculates the distance to an object and sends the data via a 60-ft RS-232C cable as two ACII numbers delimited by a space character (20H) and terminated with a carriage return (0DH). Communications take place at 9600 baud with no parity and 1 stop bit. A wall-mount power supply powers the unit. The unit weighs 1.8 lbs and four mounting screw holes let you attach the remote unit to a flat surface. It operates from 0 to 70°C with a humidity of 5 to 95%. $495.

**Contaq Technologies Corp,** 15 Main St, Bristol, VT 05443. Phone (802) 453-3332.

**Circle No 360**

## COMPUTER BOARD

- *Has an 80C196 µP with two timer/counters*
- *Provides an 8-channel, 10-bit ADC*

The CP-196 CMOS single-board computer offers a 16-bit 80C196 µP. It features two parallel ports; a serial port; and an 8-channel, 10-bit A/D converter. In addition, the processor provides eight high-speed I/O lines and two 16-bit timer/counters. The board provides up to five 8-bit parallel ports. It has buffered RS-232C and RS-422 ports, and a third serial port operates as both an RS-232C and an RS-422 port. All three ports are brought out to $2 \times 20$ header connectors. The board's memory features a 60k-byte EPROM and RAM on four JEDEC 28-pin ICs. The board measures $5.375 \times 8$ in. and requires a 5V supply. Bare board, $100; assembled with 32k-byte EPROM and 28k-byte RAM, $500.
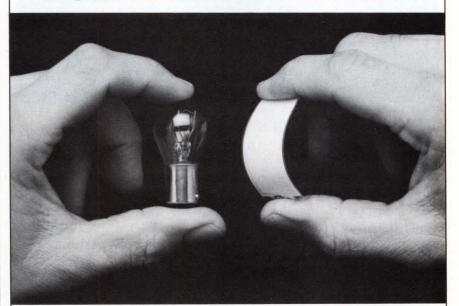
**Allen Systems,** 2151 Fairfax Rd, Columbus, OH 43221. Phone (614) 488-7122.

**Circle No 361**

# NEW PRODUCTS

## INTEGRATED CIRCUITS



### VIDEO SHIFT REGISTER

- *Features 40-bit, 250 MHz capability*
- *Provides integration for systems running at over 125 MHz*

Adapting to a variety of frame buffers and RAM-DAC structures, the Bt424 video shift register reduces component count in high-resolution graphics systems. Because it employs both TTL and ECL circuitry, the register provides a low-to-high speed interface that simplifies system timing. With a 40-bit multitap architecture, the register works with systems running at rates of 125 MHz or faster. You can use the device with other high-speed bipolar products in the vendor's line. The chip operates from a single 5V supply or 5V and −5.2V supplies. It consumes 1.25W and comes in a 68-pin PGA package. $62(100).

**Brooktree Corp,** 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 452-7580. TLX 383596.

**Circle No 365**

### INTERFACE CHIPS

- *Provide transmit and receive functions for T1 or CEPT lines*
- *Convert signals to TTL level*

Providing the interface for T1 and CEPT digital lines, two single-chip bipolar ICs perform receive, transmit, and loop-back functions. The SSI-78P233 transceiver conforms to North American T1 standards; the SSI-78P234 to worldwide CEPT standards. The receiver extracts data from the incoming bit stream and converts it to TTL-level signals. The ICs employ a trimmed, analog, phased-locked loop and a precision external resistor. No other tunable or precision compo-



nents are required. The transmitter accepts TTL data and clock signals, converts them to an alternate-mark-inversion bit stream, and lets you equalize and shape outgoing pulses according to the line length. The ICs require only a single 5V supply. The 78P233 comes in 24-pin DIP and SO packages; the 78P234 in 20-pin DIP and SO packages. $10.68 (100).
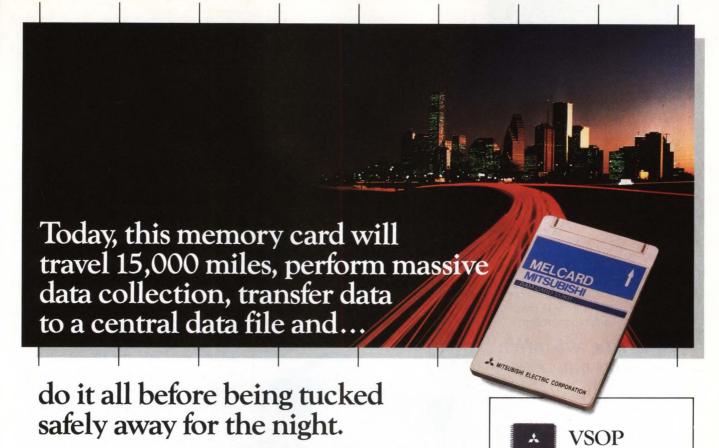
**Silicon Systems,** 14351 Myford Rd, Tustin, CA 92680. Phone (714) 731-7110.

**Circle No 366**

### CMOS MAC CHIP

- *25-MHz multiply-accumulate rate*
- *TTL-compatible inputs and outputs*

Featuring an $8 \times 8$-bit parallel architecture, the TMC2208 has a 40-nsec cycle time (25-MHz multiply-accumulate rate). You can specify the input data as two's complement or unsigned magnitude, yielding a full-precision 16-bit product. You can accumulate products to a 19-bit result. The chip features selectable accumulation, subtraction, rounding, and accumulator preload. The inputs and outputs are registered and TTL compatible. The device operates from a single 5V supply and comes in a 48-pin ceramic DIP or plastic package. Ceramic DIP, $21; plastic package, $15 (1000).

**TRW LSI Products Inc,** Box 2472, La Jolla, CA 92038. Phone (619) 457-1000.

**Circle No 367**

### PULSE DETECTOR

- *Features embedded servo circuit*
- *Wide-bandwidth amplifier eliminates gain adjustment*

The DP8468B disk-pulse detector meets the requirements of 3.5- and 5.25-in. hard-disk drives. The chip, which has a maximum storage capacity of 200M bytes, works with standard drives or with drives that employ RLL codes. The device features an on-chip embedded servo circuit that allows it to position the disk head at the true center of a track. The chip's wide-bandwidth differential amplifier provides auto-

# Today, this memory card will travel 15,000 miles, perform massive data collection, transfer data to a central data file and…

**MELCARD MITSUBISHI** RAM CARD 512KB

MITSUBISHI ELECTRIC CORPORATION

## do it all before being tucked safely away for the night.

Now, with Mitsubishi's transportable memory cards, you can have the flexibility of carrying 32K Bytes to 2M Bytes of SRAM, OTPROM or masked ROM in your pocket. That means read/write capability (without a disk drive), remote from central data storage, plus the flexibility to interchange memory types (SRAM, OTPROM, masked ROM), upgrade and downgrade memory density, and change data width (8 bits, 16 bits). All with an extremely rugged device that's the size of a credit card (86mm x 54mm x 3.4mm).

### The Applications Are Virtually Endless.

From personal computers to printers, portable equipment to telecommunications, the applications are as creative and endless as the imagination. Anywhere transportable memory and massive data storage are required, Mitsubishi's transportable cards offer the highest memory densities available on a device this small.

### Save On Systems Design Costs.

Mitsubishi's transportable memory cards offer standardized card connectors and pin assignments for easy memory interchange and density upgrade, without designing multiple host system models. Plus, future system redesign is simplified or eliminated.

### Extremely High Density Memory.

The key to Mitsubishi's extremely high density memory cards is the VSOP (very-small-outline-package). Pioneered by Mitsubishi, the VSOP is over four times smaller (in overall volume) than its equivalent pin count, standard surface mount package. In fact, the VSOP is smaller than the footprint of the equivalent chip-on-board technology making it possible to pack up to 16 memory ICs, plus standard interface circuitry on one card.

**VSOP**
13.8 mm x 8.0 mm x 1.0 mm = 110.4 mm³

**Chip-On-Board**
15.4 mm x 9.8 mm x 1.0 mm = 150.9 mm³

**SOP**
17.5 mm x 12.2 mm x 2.2 mm = 469.7 mm³

### "Transportable" Means "Rugged."

Mitsubishi designed its memory cards specifically for transportable applications. And, that means cards that are rugged and reliable. Even if a card is dropped, loss of valuable data is virtually eliminated, due to Mitsubishi's flexible, four-layer PCB and enhanced soldering techniques.

Additionally, the cards are ESD protected to 25K volts, with connectors guaranteed for 10,000 insertions.

If you want to design–in massive, transportable data storage with the flexibility to interchange memory types and densities, Mitsubishi memory cards give you the maximum memory mileage. For more information call or write today: Mitsubishi Electronics America, Inc., Semiconductor Division, 1050 East Arques Avenue, Sunnyvale, CA 94086. (408) 730-5900.

## Quality Through Commitment.

## MITSUBISHI ELECTRONICS

**Regional Offices:**
NORTHWEST, Sunnyvale, CA (408) 730-5900
SOUTHWEST, Torrance, CA (213) 515-3993

SOUTH CENTRAL, Carrollton, TX (214) 484-1919
NORTHERN, Minnetonka, MN (612) 938-7779
NORTH CENTRAL, Mt. Prospect, IL (312) 298-9223

NEW ENGLAND, Woburn, MA (617) 938-1220
MID-ATLANTIC, Piscataway, NJ (201) 981-1001
SOUTH ATLANTIC, Norcross, GA (404) 662-0813

SOUTHEAST, Boca Raton, FL (305) 487-7747
CANADA, St. Laurent, Quebec, (514) 337-6046

matic gain control, which eliminates the need for factory gain adjustments. The gating channel uses a differential comparator with hysterisis to avoid problems caused by false signals. The DP8468B functions with data rates to 15M bps. Available in a 28-pin plastic leaded chip carrier, the device costs $10 (1000).

**National Semiconductor Corp,** Box 58090, Santa Clara, CA 95052. Phone (408) 721-6725. TLX 346353.

**Circle No 368**

## A/D CONVERTERS

- *15- and 25-$\mu$sec conversion*
- *150-mW (max) power consumption*

The SP674A and HS574A are 12-bit monolithic A/D converters that are pin-compatible with Harris's two-chip HI674A and Analog Devices' AD574A. The SP674A and HS574A contain an internal 10V reference, a clock, and 3-state output buffers for direct interfacing to 8-, 12-, or 16-bit $\mu$P buses. The SP674A has a typical conversion time of 12 $\mu$sec (15 $\mu$sec max); the HS574A's typical conversion time is 15$\mu$sec (25 $\mu$sec max). Both converters offer standard bipolar and unipolar input ranges of ±5V, ±10V, 0 to 10V, and 0 to 20V. Maximum linearity error is ±0.5 LSB. The company guarantees no missing code to 12 bits over the specified temperature range. Both ADCs operate from 5V and 12 to 15V supplies and feature a maximum power consumption of 150 mW. Packaging options include a ceramic 28-pin DIP and a ceramic 28-pin LCC. The converters are available in the commercial, indus-

trial, and military temperature ranges. Depending on grade and screening, $25 to $160.

**Sipex Corp,** Hybrid Systems Div, 22 Linnell Circle, Billerica, MA 01821. Phone (617) 667-8700. FAX 617-667-8310.

**Circle No 369**

## WATCHDOG IC

- *Provides sequenced reset signals*
- *Has a programmable time-out period*
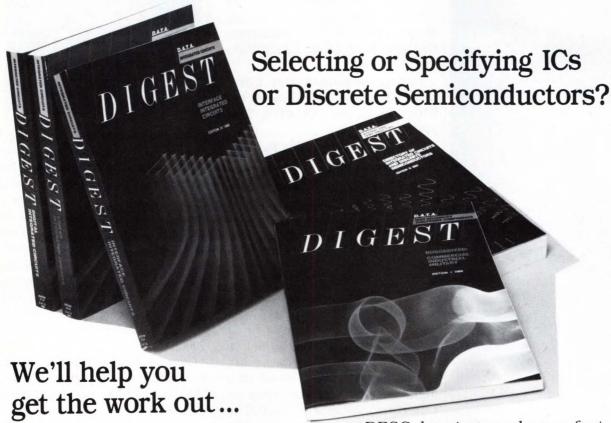
Incorporating voltage comparators, a programmable timer, and reset sequencing logic, the H6060 can act as a power supply monitor or as a reset generator for $\mu$P systems. It generates reset outputs of both polarities. You can program the length of the recovery interval from 3 msec to 3 minutes. The IC generates a low-voltage alarm output prior to the reset. The device can function with a minimum of 3.5V; its output signals remain in a defined state even when the device's supply voltage falls to zero. The IC monitors 5 or 3.5 to 5.5V supplies. The vendor can program the device's voltage thresholds for other applications. Around $2.50.

**EM Microelectronic-Marin SA,** H-2074 Marin, Switzerland. Phone (038) 352141. TLX 952790.

**Circle No 370**

## CMOS PLDs

- *Feature 12-nsec propagation delay*
- *Maximum current is 115 mA*

The GAL16V8A-12 and GAL20-V8A-12 are 20- and 24- pin PLDs, respectively. They employ electrically erasable CMOS technology to provide a 12-nsec propagation delay. The E$^2$CMOS technology allows complete ac, dc, and functional testing during manufacture. The PLDs feature a data-retention life of more than 20 years, according to the vendor. The PLDs let you replace any common 20- or 24-pin

programmable logic device. Both models operate at a current of 115 mA max. The vendor offers develoment tools, such as programming and software packages. GAL16V8A-12, $8.32; GAL20V8A-12, $9.51 (100).

**Lattice Semiconductor Corp,** 5555 NE Moore Ct, Hillsboro, OR 97124. Phone (503) 681-0118. TLX 277338.

**Circle No   371**

## 12-BIT HYBRID ADC

- *1-µsec conversion time*
- *Pin-programmable inputs*

The ADC-511 12-bit A/D converter features a maximum conversion time of 1 µsec and a typical power dissipation of 925 mW. It is packaged in a 24-pin DIP. The ADC-511 contains an internal clock and an internal reference that supplies 10V at 1.5 mA externally. Based on a digitally-corrected subranging architecture, the hybrid's digital inputs and 3-state outputs are CMOS and TTL compatible. You can select straight/offset-binary or complementary-binary/-offset output coding. A pin-programmable feature lets you select either unipolar analog inputs from 0 to 10V or bipolar analog inputs from −5 to +5V. The ADC-511 operates from ±15 and +5V dc power supplies over the 0 to 70°C temperature range. $99 (1000).
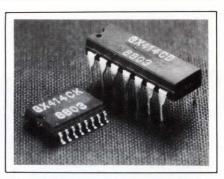
**Datel Inc,** 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-3000. TLX 951340.

**Circle No 372**

## VIDEO SWITCH

- *Low standby power*
- *8-MHz bandwidth*

Designed for broadcast-quality switching matrices, the GX414 video crosspoint switch has frequency response that is flat within ±0.075 dB from dc to 8 MHz. The chip has a standby power consumption of only 5.7 mW when disabled.



The GX414 is configured as a 4×1 switch containing 4 analog video switches and a 2-to-4 decoder. An enable input lets you parallel GX414s and operate them in a switching matrix with multiple inputs and a common output. When enabled, the switch makes a fully buffered unilateral transmisssion path with a typical off-isolation of 100 dB at 10 MHz. Available in DIP and SOIC packages, the GX414 costs $5.73 and $6.21, respectively (1000).

**Gennum Corp,** Box 489, Station A, Burlington, Ontario, Canada L7R 3Y3. Phone (416) 632-2996. TLX 0618525.

**Circle No 373**

## MICRO-CHANNEL CHIP

- *Provides decoding and logic functions*
- *Has DMA arbitration*

The 88C01 chip provides a microchannel interface. It reads configuration information when the power is turned on. The chip provides programmable decoding for extended memory, expanded memory, I/O ports, and ROM. It lets you define registers and address memory lines. The chip provides DMA and burst-mode DMA. The pinouts are optimized for micro-channel board layout. The device meets the micro-channel drive requirements without buffering, and has multiplexed memory address lines for direct connection to 1M-bit DRAMs. $27.50 (100).

**Capital Equipment Corp,** 99 S Bedford St, Burlington, MA 01803. Phone (617) 273-1818.

**Circle No   374**

# NEW PRODUCTS

## COMPONENTS & POWER SUPPLIES

### POWER SUPPLIES

- *Available with power outputs of 100W*
- *Switching frequency ranges from 80 to 200 kHz*

MW Series switching power supplies are available in 15, 30, 50, and 100W versions. Standard outputs are 5, 12, 15, and 24V. The 15, 30, and 50W models are available with triple outputs, and the 100W version provides four outputs. Input voltage specs at 85 to 264V dc. Power density ranges from 1.52 to 2.21W/in.$^3$, and efficiency is as high as 65%. Switching frequencies span an 80- to 200-kHz range. All versions offer overcurrent and overvoltage protection. The supplies meet FCC Class B noise standards



as well as UL478 and CSA requirements. The operating range is 0 to 60°C. Custom variations, such as output voltage and current, are available at no charge. $85 to $235.

**Toko America Inc,** 1250 Feehanville Dr, Mount Prospect, IL 60056. Phone (312) 297-0070. FAX 312-699-7864.

**Circle No 380**

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### PROXIMITY SENSOR

- *Features a dual-range capability*
- *Provides a wide sensing beam*

The Model 9501A proximity sensor is designed to help the automated guided vehicles (AVGs) used in industrial settings to avoid collisions. Unlike other sensor designs, the 9501A creates a wide fan-shaped sensing region that has two sepa-

rate detection ranges. This dual-range capability allows the AGV to have a slow-down zone as far as 10 feet ahead and a stop zone as close as 4 feet ahead. The unit's sensing technology provides high gains in the sensing region and a sharp cutoff beyond the maximum range. As a result, the sensor will detect both light and dark objects while it ignores backgrounds. The 9501A features built-in test capability (self-diagnostics) and is unaffected by other sensors operating nearby. $325.

**Opcon Inc,** 720 80th St NW, Everett, WA 98203. Phone (206) 353-0900.

**Circle No 381**

### DPMs

- *Feature ±0.1% accuracy*
- *Handle ±20V dc inputs*

DP-1350 Series 3½-digit DPMs employ a dual-slope integrating A/D converter and full-differential inputs. The -1350 and -1354 models



have ±2- and ±20V dc full-scale input ranges, respectively. Both models feature LED displays with 14.3-mm-high characters, a hold function, an 86-dB CMRR, and ±0.1% accuracy. They draw only 1W (5V at 200 mA). The internal reference can be replaced by an external reference to accommodate ratiometric measurements. The meters feature user-selectable decimal-point placement, automatic polarity changeover, full autozeroing, and overrange indication. The operating range is 0 to 50°C, and the temperature coefficient is ±100 ppm/°C. $79.

**Acculex,** 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3660. TLX 503989.

**Circle No 382**
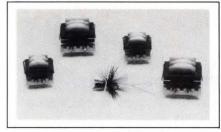
## CHOKES

- *Windings balanced within 1%*
- *Meet UL and CSA reqirements*
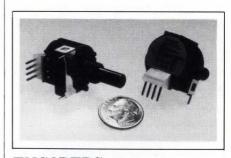
RL1361-1 and RL1361-2 common-mode chokes are designed with out-of-phase windings that are balanced within 1%. When used at power-line inputs, they can cancel or suppress EMI transients sufficiently to meet industry specifications. Standard units meet UL and CSA requirements. Units can also be manufactured to VDE specifications. Operating temperature is −55 to +130°C. All units will withstand a 2500V ac hipot test for winding-to-winding and winding-to-core. More than 80 standard models, designed for pc-board mounting, are available. Current ratings range from 100 mA to 5.5A. MIL-spec and encapsulated models are also available. From $0.95 (10,000). Delivery, stock to eight weeks ARO.

**Renco Electronics Inc,** 60 Jefryn Blvd E, Deer Park, NY 11729. Phone (516) 586-5566. FAX 516-586-5562.

**Circle No 383**

## ENCODERS
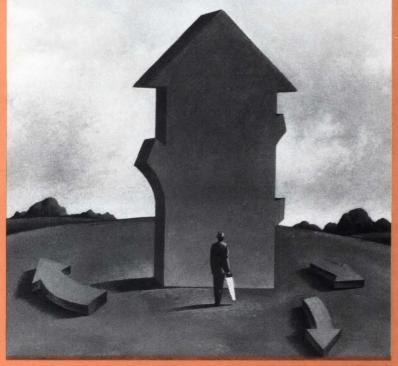
- *Noncontacting direct rotary-to-digital converters*
- *Operate from one 5V supply*

Softpot Models SPM-50 and SPM-100 optical shaft encoders convert shaft angle, speed, and direction into real-time digital information. A torque-loaded shaft provides the feel of a limitless potentiometer for front-panel man-to-machine interface applications. The -50 and -100 encoders respectively provide 50 and 100 cycles to generate 200 and 400 quadrature codes per revolution. The internal electronics, which draw only 50 mA from a 5V supply, include two solid-state light sources. The miniature encoders are housed in a package that measures only 0.8 in. in diameter. $22 (100).

**U S Digital Corp,** 12371 Kensington Rd, Los Alamitos, CA 90720. Phone (213) 594-0094. FAX 213-594-6091.

**Circle No 384**
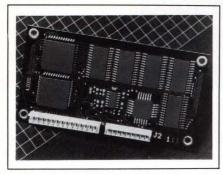
## VOICE MODULE

- *Provides solid-state answerphone facilities*
- *Interfaces to mobile or cellular radio equipment*

Employed in the audio stages of mobile or cellular radio systems, the CXM1380 voice store-and-retrieval module provides facilities similar to those of a conventional answering machine. However, instead of using audio tape, the module uses a delta-modulation codec and static RAM to provide a totally electronic system. You can record the answer message using the existing mobile radio or cellular phone handset, and a message-skip facility allows you to rapidly review recorded messages. The module, which is housed on a $3.8 \times 1.97$-in. pc board, requires only one 5V supply and logic-level, call-progress control signals from the phone set. £153 (100).

**Consumer Microcircuits Ltd,** 1 Wheaton Rd, Witham, Essex CM8 3TD, UK. Phone (0376) 513833. TLX 99382.

Circle No   385

**Mx-Com Inc,** 4800 Bethania Station Rd, Winston-Salem, NC 27105. Phone (919) 744-5050.

Circle No   386

## TRANSFORMERS

- *Connect modem terminals to the telephone lines*
- *Meet international standards for creepage and clearance*

TH Series coupling transformers are designed to meet European/International standards, such as VDE, BSI, and Australian Telecom, as well as FCC Part 68 requirements. Despite their $0.81 \times 0.66 \times 0.75$-in. size, the pc-board-mountable units meet the creepage and clearance requirements of international standards. Designed to interconnect voice/data modem terminals to the telephone lines, the TH2104 and TH2106 transformers are rated at 600:600Ω at 0 mA dc. Both windings of the 2106 are center-tapped. Typical insertion loss is 1.0 dB, and minimum return loss at 300 Hz measures 22 dB. $5.75 (500) for the TH2104.
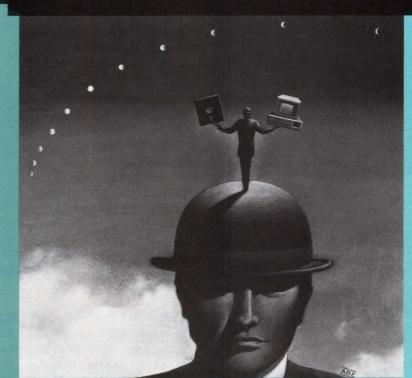
**Microtran Co,** Box 236, Valley Stream, NY 11582. Phone (516) 561-6050. TWX 510-225-8412.

Circle No 387

CIRCLE NO 35   227

# NEW PRODUCTS

## CAE & SOFTWARE DEVELOPMENT TOOLS

### C LIBRARY FOR OS/2

- *Lets you port your programs from MS-DOS to OS/2 and back*
- *Manages the entire user interface*

C-Worthy Interface Library is a system of pretested functions for creating and managing the user interface of your application programs. The user interface can resemble that of the OS/2 Presentation Manager or of Lotus 1-2-3, or it can be uniquely adapted to meet the needs of your application. The library contains more than 350 functions for on-line help, error handling, screen displays, and data input. The documentation includes examples of how to use the functions, a detailed description of each function, and indexes. A Forms Interface package for designing reports is also available. The libraries are compatible with version 5.1 of the Microsoft C compiler, and you can order the libraries for either MS-DOS or OS/2 (prices are the same for both). C-Worthy library,
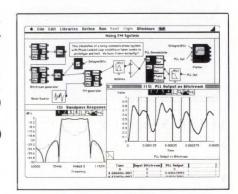
$195; with Forms Interface Library, $295; with source code for both libraries, $495.

**Solution Systems,** 541 Main St, Suite 410, S Weymouth, MA 02190. Phone (800) 821-2492; in MA, (617) 337-6963.

**Circle No 390**

### SIMULATOR

- *Library includes models of many DSP and digital functions*
- *Runs on Macintosh computers*

Extend is a modular, behavioral-simulation program that runs on Apple's Mac II, Mac SE, and Mac Plus computers. It lets you build block diagrams, insert the function of each block in the form of a script, and then connect the blocks together to form a system model. When you run a simulation, the results are both plotted as waveforms and presented as tabular data. The scripting language (ModL) provides more than 60 functions for plotting,



math, queuing, statistics, and diagnostics. The simulator works with the vendor's advanced electronics engineering libraries, which provide icons and scripts for a wide variety of both analog and digital functions, including A/D and D/A converters, amplifiers, filters, VCOs, and phase-locked loops. Extend, $495; libraries, free with Extend until 1 September, 1988, and $95 thereafter.

**Imagine That!** 7109 Via Carmela, San Jose, CA 95139. Phone (408) 365-0305.

**Circle No 391**

### EPLD DESIGN TOOLS

- *Allows you to design EPLDs on an IBM PS/2*
- *Makes full use of the VGA graphics features*

A-PLUS lets you enter an EPLD (erasable programmable logic device) design as a schematic, in state-machine language, or in Boolean or netlist formats. You can create macrofunctions or use TTL functions from the vendor's macrofunction library. The program performs logic minimization and automatically fits the logic into the smallest EPLD that will hold the design. You can use the program with the vendor's EP series of EPLDs. The SAM+PLUS package performs a similar series of functions with the EPS family of function-specific EPLDs. These EPLDs use a microsequencer architecture to create
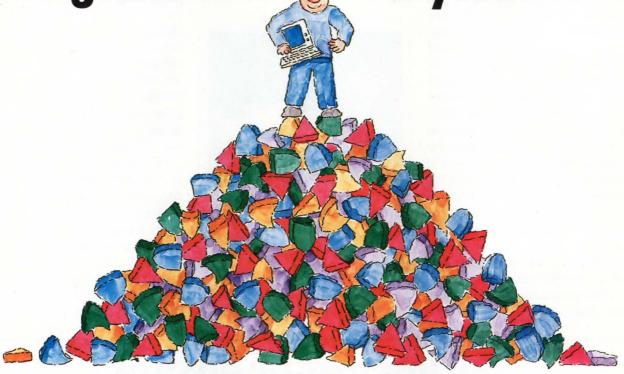
complex state machines and high-performance controllers. They are available from the vendor and from WaferScale Integration Inc. A-PLUS software, $1750. The vendor also supplies a complete hardware/software development system that

includes A-PLUS, related CAE software options, and programming hardware for $5995.

**Altera Corp,** 3525 Monroe St, Santa Clara, CA 95051. Phone (408) 984-2800.

**Circle No 392**

## ASIC ANALYSIS

- *Allows ac and dc measurements of prototype ASICs*
- *Offers Shmoo-plotting of test results*

The Characteristic and Timing Analysis (CTA) package allows you to automate any Logic Master measurement, collect and format the test results for analysis, and control the Logic Master from a spreadsheet program. CTA is compatible with any product contained in the vendor's Logic Master ASIC-verification family. The program provides menu-driven routines for making ac and dc measurements of prototype ASIC devices and for the Shmoo-plotting of the interaction of any two device variables. One of the menus lets you measure propagation delay, setup time, and hold time. You can also create your own analysis routines using any of the 30 preprogrammed CTA functions. Prices start at $3000 for the Logic

Master ST workstation.

**Integrated Measurement Systems,** 9525 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 626-7117.

**Circle No 393**

## DATA LINK

- *Transfers files between DEC and Datapoint computers*
- *Uses an ArcNet LAN*

The Daft file-transfer package allows you to transfer data between DEC VAX minicomputers and Datapoint Corp computers, using the Datapoint high-speed ArcNet network facility. The package provides transfer of text files between Datapoint machines running either Datapoint RMS or DOS, and VAX computers running VAX/VMS. The package comprises a file transfer server program for the Datapoint computer, a VAX/VMS driver to drive the ArcNet interface, user interface and transfer protocol programs for the VAX computer, and a Q Bus or Unibus ArcNet interface card. To speed data transfers, they are performed in binary mode wherever possible. Utilities are provided that allow you to perform off-line conversion between VMS and Datapoint formats. You can also automate data transfers and format conversions. On-line help facilities are included in the user interface. A Q Bus version for a MicroVAX sells for $7800. The Unibus version costs ap-

proximately $9200.

**Comendec Ltd,** Aston Science Park, Love Lane, Aston Triangle, Birmingham B7 4BJ, UK. Phone 021-359-0981. TLX 33435.

**Circle No 394**

## LINKING SOFTWARE

- *Speeds transfer rates with data-compression algorithm*
- *Allows 15 simultaneous communications exchanges*

Relay Gold version 3.0 enables personal-computer communications and micro-to-mainframe linking. It employs a data-compression algorithm that speeds transfer rates. The software lets you communicate asynchronously and maintain 15 simultaneous sessions. It lets you download data without leaving the application. An IBM PS/2 Adapter/A support facility gives you access to IBM PS/2 computers. You can use the software with 160k bytes in resident mode. It emulates the IBM 3101; VT220; VT240; 3278 Models 2, 3, 4, 5; and 3279 Models 2 and 3. The software can run at 38,400 bps max. $295; upgrade from an earlier version, $75.

**Relay Communications Inc,** 41 Kenosia Ave, Danbury, CT 06810. Phone (800) 847-3529; in CT, (203) 798-3800.

**Circle No 395**

## OS-9 SHELL

- *Provides a Unix-like shell for the OS-9/68k operating system*
- *Includes high-level language commands*

The SH software package provides you with a programmable shell-command interpreter for the OS-9/68k operating sytem. Acting as a user interface to the operating system, the package provides a shell that is fully compatible with a standard Unix operating system shell. Its features include parameter passing, string substitution, and definition of variables. The control-flow primitives allow bidirectional communication between the operating system shell and invoked processes. You can use return codes or standard command outputs as arguments or inputs to the shell to determine control flow. You can also perform calculations and check files and shell variables for their type and state. In addition to AND and OR command groupings, the shell includes high-level commands such as if-then-else, do-while, and case statements. The SH package is supplied on an OS-9 diskette. $650.

**EKF Elektronik GmbH,** Weidekampstrasse 1a, 4700 Hamm 1, West Germany. Phone (02381) 12630. TLX 828621. FAX 023-811-5067.

**Circle No 396**

# NEW PRODUCTS

## TEST & MEASUREMENT INSTRUMENTS

### HANDHELD DMM/SCOPE

- *Features dual-channel operation*
- *Stores three waveforms/channel in battery-backed memory*
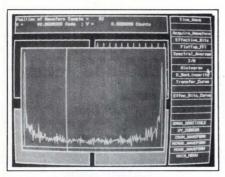
The Model 200 portable 2¹/2-lb DMM/oscilloscope provides dual-channel operation. It samples at 3M samples/sec max and offers autoranging. The unit lets you store three waveforms/channel in a battery-backed memory. You can also use ac power to run the unit. The display lets you set sensitivity, time-base, trigger source and slope, and mode parameters. The unit features manual override and an overload indicator. A printer interface lets you evaluate data and document your work on hard copy.



$1645.
**Leader Instruments Corp,** 380 Oser Ave, Hauppauge, NY 11788.

Phone (800) 645-5104; in NY, (516) 231-6900.

**Circle No 420**

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### ADC EVALUATOR

- *Tests 10-bit ADC working at 20M samples/sec*
- *Employs an 80386 μP and an 80387 coprocessor*

The PTS101 A/D characterization system evaluates ADC performance. The system targets applications such as high-speed data acquisition and image processing. Employing an 80386 μP and 80387 coprocessor, this evaluator can test ADCs working at 20M samples/sec with a 10-bit resolution. If your ADC has tighter specs, the evaluator provides IEEE-488 ports that let you drive high-performance generators and acquisition units. Using two internal cards, the system controller generates arbitrary and data-acquisition functions. Matching probes are also provided. The vendor's software package is menu-driven and features a 5-color display. $18,950.

**Tektronix Inc,** Measurement Systems Div, Jack Murdock Industrial Park, Box 3500, M/S C1-894, Vancouver, WA 98668. Phone (800) 835-9433, ext 170.

**Circle No 421**

### DSP EMULATORS

- *Support TMS32020 and TMS320C25 processors*
- *Allow real-time no-wait-state execution to 40 MHz*

The HP 64786A performs emulation-bus analysis and in-circuit emulation of systems based on the TMS32020 DSP. The HP 64786AL adds state and timing analysis. All units perform real-time no-wait-state emulation. In some systems that use the TMS320C25, you can operate without wait states at clock rates to 40 MHz max. The emulators include 64k words of dual-ported memory that you can allocate in



1k-byte blocks. You can configure the memory as emulation or target RAM or ROM, or as guarded memory. The units provide 8-level sequencing, time tags, prestore, and hardware-implemented code-coverage analysis. For developing multiprocessor systems based on any of 40 8-, 16-, and 32-bit μPs, a coordinated-measurement bus links to the vendor's 64000-UX-intermodule bus. This connection allows the cross-triggering of as many as 32 HP 64700-series analyzers. $13,300 to $16,500.

**Hewlett Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local sales office.

**Circle No 422**

# SIMPSON UNIVERSAL FREQUENCY COUNTERS.
# COUNT ON US FOR ACCURACY.

Simpson's new high precision, eight digit frequency counters give you an eye into the world of critical clock signals, RF oscillators and data communications.

Readings of frequency (to *1.3 GHz*), frequency ratio (A/B), period, time interval (A to B) and totalized count combined with multi-channel triggering let you find circuit problems that might otherwise go unnoticed.

Simpson's *Professional Series* frequency counters allow for accurate measurements to be

taken on complex and noisy wave-forms by using the variable trigger controls and built-in, low pass filter. One model even offers you selectable attenuation and

AC/DC coupling, allowing the inputs to accommodate a range of signal characteristics. For more complex measurement situations involving two interdependent frequencies, an external clock can be substituted for the internal oscillator. This feature enables you to investigate a wide spectrum of frequencies—from computer circuitry to satellite communications.

Try the new lineup of *Professional Series* frequency counters from Simpson. It all adds up to accuracy and reliability.

## DATA LOGGERS

- *Record 200 readings/sec on internal floppy disk*
- *Handle 600 channels, using slave scanners*

Data loggers in the 3531 series can store 200 measurement results/sec on a floppy disk in an internal drive. The ASCII files created are compatible with MS-DOS and Hewlett-Packard LIF (Logical Interchange Format). Without an expansion chassis, and without additional signal conditioning, the loggers can support 200 inputs, which can be a mixture of voltages (including those derived from thermocouples), currents, resistances (including the output of resistance thermometers and strain gauges), and binary phenomena (including on/off events, frequencies, and time intervals). The units also provide analog and digital outputs for control of machinery and processes. With the addition of slave chassis, you can expand these loggers to 600 channels. An RS-232C port is standard equipment; RS-422 and IEEE-488 ports are optional. Unit with keyboard, display, thermal printer, disk drive, and optional ports, $9950; unit without options or peripherals, $5150. Delivery, eight weeks ARO.
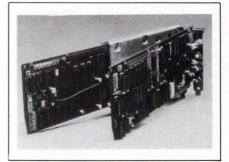
**Schlumberger Instruments,** 20 North Ave, Burlington, MA 01803. Phone (617) 229-4825.

**Circle No 423**

## PC-BASED SCOPE

- *Stores 4k or 16k samples*
- *Has 10-step software-controlled attenuators*

The SDS-5000 digital storage oscilloscope plugs into the IBM PC bus or the vendor's instrument chassis. It includes dual A/D converters with a maximum sampling rate of 20M samples/sec; it stores 4k samples or an optional 16k samples. The unit's 10-step software-controlled attenuators allow you to set full-scale input sensitivity from 4 to 40 mV. The software lets you pretrigger and post-trigger, zoom, delay sweeps, add, subtract, and average signals. In addition, it allows you to make cursor measurements and store or retrieve waveforms on disk. $1995.

**Heath/Zenith,** Hilltop Rd, Saint Joseph, MI 49085. Phone (616) 982-3200.

**Circle No 424**

**CIRCLE NO 38**

# SMALL NEWS



## PC-based 8051 emulation priced to fit any engineer's desk...MicroICE. From $1495.*

Need full in-circuit emulation capability for your 8051-family applications? We've got small news for you:

MicroICE™ emulators from MetaLink.

MicroICE **fits your budget—and fits on your desk.** They're the world's smallest, full-featured 8051 ICE units.

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The MicroICE line offers you the same high performance (compared to

our existing MetaICE specialized emulators) with even more features for about half the cost. So, you stretch your budget and give your designers more full-time emulation access—critical when you have multiple projects.

Why MetaLink? We're the 8051 experts. We understand how to maximize your design time—and get you the best performance from your 8051 application—so you can control your development deadlines.

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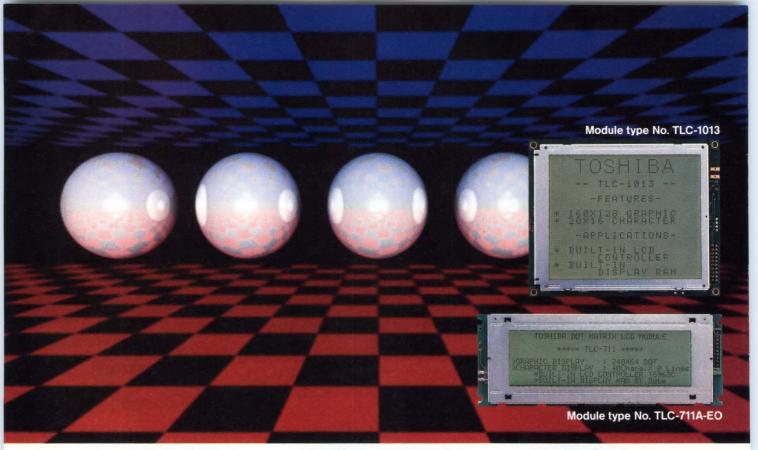
MetaLink Corporation
P.O. Box 1329 Chandler, Arizona 85244-1329
(602) 926-0797 TELEX: 4998050 MTLNK
FAX: (602) 926-1198

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## Books for calculator applications

The vendor is offering profession-specific solution books for the HP-27S and the HP-28S. The five books available for the HP-27S are titled Real-Estate, Banking, and Leasing; Business Finance and Accounting; Marketing and Sales; Personal Investment and Tax Planning; and Technical Applications. For the HP-28S calculator, the titles are Algebra and College Math; Calculus; Electrical Engineering; Probability and Statistics; Vectors and Matrices; and Mathematical Applications. $9.95 each.

**Hewlett-Packard,** Corvallis Div, 1000 NE Circle Blvd, Corvallis, OR 97330.

**INQUIRE DIRECT**
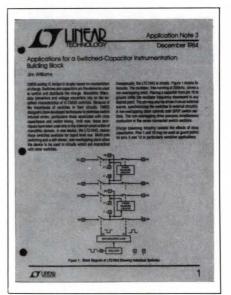
## Brochure covers μP development products

The 12-pg brochure, *Microprocessor Development Environments*, presents an overview of the vendor's in-circuit emulation products and software development tools. It provides development-tool solutions for embedded μP designs, as well as product information. Photographs and charts complete the publication.

**Applied Microsystems Corp,** Box 97002, Redmond, WA 98073.

**Circle No 400**

## App note explains switched-capacitor filters

*AN3: Applications for Switched-Capacitor Building Blocks* discusses part values for a variety of tested circuits using switched-capacitor building blocks. Among the circuits detailed are a ±5V precision instrumentation amplifier, a variable-gain amplifier, relative-humidity signal conditioners, an LVDT (linear variable differential transformer) signal conditioner, and A/D and V/F converters. It also provides complete schematics.

**Linear Technology Corp,** 1630 McCarthy Blvd, Milpitas, CA 95035.

**Circle No 401**

## Summary and comparison of ADC performances

The 2-pg application note, *AD7578 and AD7582 Performance with Reduced $V_{DD}$ Supply (12V ±10%)*, summarizes typical performance at 12V $V_{DD}$ for 100-μsec, 12-bit ADCs and compares it with the data-sheet specifications for 15V operation. Among the topics included are accuracy, timing, power-supply current, and logic inputs and outputs. Also included are a table showing accuracy results and a diagram illustrating the interfacing of the ADCs to an IBM PC.

**Analog Devices,** Literature Center, 70 Shawmut Rd, Canton, MA 02021.

**Circle No 402**

## Report helps you evaluate communications technologies

The 390-pg volume, *The Impact of Evolving Communications Technologies*, helps you assess the impact of major communications developments on public and private networks. The table of contents provides a single-source reference to subjects ranging from artificial intelligence to voice synthesis and recognition. The report presents applications, economic and technical considerations, and technical comparisons. Each section of the book details a technology, such as local area network/metropolitan area network (LAN/MAN) and wide-band services, fiber optics, ISDN, and virtual networks. Tables, diagrams, and flow charts illustrate the text.

**Bellcore Licensing,** 290 W Mt Pleasant Ave, Livingston, NJ 07039.

**Circle No 403**

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## 32-BIT PRODUCT MANAGER

Responsible for the success of the 32-bit Product Line. Duties include forecasts, price strategy, competitive analysis, cost analysis, new product introduction, first level technical contact with customers and intra company representation. Requires BSEE and 3+ years experience in computer systems; MBA helpful.

## PRODUCT ENGINEERS

Responsible for yield/cost management and improvement, characterization of products to support design, manufacturing and quality improvements, and customer interface. Requires BSEE and 1-5 years experience with knowledge of microprocessor functions and characteristics.

## SOFTWARE ENGINEERS

Design, implement and maintain operating systems, compilers, assemblers, simulators and run-time support packages for the M68000 and M88000 product families. Requires BSCS, BSEE or equivalent and programming experience in a UNIX C environment and/or Graphics.

## CAD/CAE ENGINEERS

Design, develop and maintain the CAD/CAE tools for integration to design engineering system. Requires strong knowledge of related tools and standards.

## SYSTEMS DESIGN ENGINEERS

Responsible for definition/development of 16/32 bit microprocessor and peripheral elements/various combinations and development of design methodology for ASIC based design. Requires BSEE/BSCS and 3-5 years experience or MSEE/MSCS and 1-3 years experience including strong background in computer architecture and High Level Language. Experience in ASIC software tool development is a plus.
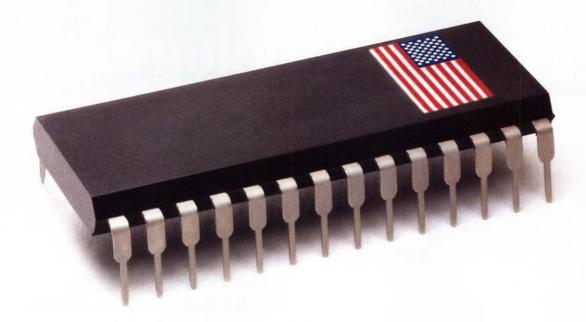
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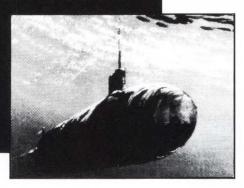
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275 Washington St
Newton, MA 02158
(617) 964-3030

# BUSINESS/CORPORATE STAFF

**Peter D Coley**
VP/Publisher
Newton, MA 02158
(617) 964-3030; Telex 940573
Ora Dunbar, Assistant/Sales Coordinator

**Deborah Virtue**
Business Director
Newton, MA 02158
(617) 964-3030

**Mark J Holdreith**
Advertising Sales Director
Newton, MA 02158
(617) 964-3030
Heather McElkenny, Assistant

**NEW ENGLAND**
John Bartlett, Regional Manager
Chris Platt, Regional Manager
199 Wells Ave
Newton, MA 02159
(617) 964-3730

**STAMFORD 06904**
George Isbell, Regional Manager
8 Stamford Forum, Box 10277
(203) 328-2580

**NEW YORK, NY 10011**
Daniel J Rowland, Regional Manager
249 West 17th St
New York, NY 10011
(212) 463-6419

**PHILADELPHIA AREA**
Steve Farkas, Regional Manager
487 Devon Park Dr, Suite 206
Wayne, PA 19087
(215) 293-1212

**CHICAGO AREA**
Clayton Ryder, Regional Manager
Randolph D King, Regional Manager
Cahners Plaza
1350 E Touhy Ave, Box 5080
Des Plaines, IL 60017
(312) 635-8800

**DENVER 80206**
John Huff, Regional Manager
44 Cook St
(303) 388-4511

**DALLAS 75243**
Don Ward, Regional Manager
9330 LBJ Freeway, Suite 1060
(214) 644-3683

**SAN JOSE 95128**
Walt Patstone, Regional Manager
Bill Klanke, Regional Manager
Philip J Branon, Regional Manager
James W Graham, Regional Manager
3031 Tisch Way, Suite 100
(408) 243-8838

**LOS ANGELES 90064**
Charles J Stillman, Jr
Regional Manager
12233 W Olympic Blvd
(213) 826-5818

**ORANGE COUNTY/SAN DIEGO 92715**
Jim McErlean, Regional Manager
18818 Teller Ave, Suite 170
Irvine, CA
(714) 851-9422

**PORTLAND, OREGON 97221**
Pat Dakin, Regional Manager
Walt Patstone, Regional Manager
1750 SW Skyline Blvd, Box 6
(503) 297-3382

**UNITED KINGDOM/BENELUX**
Jan Dawson, Regional Manager
27 Paul St
London EC2A 4JU UK
44 01-628 7030
Telex: 914911; FAX: 01-628 5984

**SCANDINAVIA**
Stuart Smith
27 Paul St
London EC2A 4JU UK
01-628 7030
Telex: 914911; FAX: 01-628 5984

**FRANCE/ITALY/SPAIN**
Alasdair Melville
27 Paul St
London EC2A 4JU UK
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**WEST GERMANY/SWITZERLAND/AUSTRIA**
Wolfgang Richter
Sudring 53
7240 Horb/Neckar
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**EASTERN BLOC**
Uwe Kretzschmar
27 Paul St
London EC2A 4JU UK
01-628 7030
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18818 Teller Ave, Suite 170
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**HONG KONG**
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1613 Hutchison House
10 HGarcourt Road
Central Hong Kong
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Won Chang Bldg, 3rd Floor 26-3
Yoido-dong, Youngdungpo-ku
Seoul 150, Korea
Tel: 785-6665; FAX: 784-1915
Telex: K32487 BIZKOR

**SINGAPORE/MALAYSIA/INDONESIA/THAILAND/
THE PHILIPPINES/AUSTRALIA/NEW ZEALAND**
Asia Pacific Media House PTE Ltd
Peter Cheong
100 Beach Rd
#24-03 Shaw Tower
Singapore 0718
Tel: 2915354; Telex: RS 50026 MESPLY

**TAIWAN**
Acteam International Marketing Corp
6F, No 43, Lane 13
Kwang Fu South Rd
Mailing Box 18-91
Taipei, Taiwan ROC
760-6209 or 760-6210
Telex: 29809; FAX: (02) 7604784

**PRODUCT MART**
Joanne Dorian, Manager
249 West 17th St
New York, NY 10011
(212) 463-6415

**CAREER OPPORTUNITIES/CAREER NEWS**
Roberta Renard, National Sales Manager
(201) 228-8602
Janet O Penn, Eastern Sales Manager
(201) 228-8610
103 Eisenhower Parkway
Roseland, NJ 07068

Ellen Sherwood, Western Sales Manager
12233 West Olympic Blvd
Los Angeles, CA 90064
(213) 826-5818

Maria Cubas, Production Assistant
(201) 228-8608

Susan M Campanella, *Advertising/Contracts Coordinator*
Nan Coulter, *Advertising/Contracts Coordinator*
(617) 964-3030

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# ADVERTISERS INDEX

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*Advertiser in US edition
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# "EDN MAGAZINE'S PRODUCT MART SECTION IS HELPING US BECOME A LEADER IN OUR MARKETPLACE."

Raymond J. Schnorr
Vice President of Marketing
ACCEL Technologies

**As Vice President of Marketing, Ray Schnorr** is responsible for marketing ACCEL Technologies' affordable, professional software that meets the design needs of electrical engineers. He operates on a fixed budget and demands results. "When it comes to buying media, I'm interested in two things: performance and price. With EDN's Product Mart section, I pull high-volume sales leads and meet my budget," says Schnorr.

In nineteen months, ACCEL has sold 5000 software packages to 3000 sites. "Our 1/9-page Product Mart ads in EDN magazine are allowing us to reach our target audience." And Schnorr sees more for EDN and ACCEL. "We have significant growth plans for ACCEL, and running bigger ads in EDN will be part of the strategy to get there.

"The power and prestige of EDN is helping us grow into a leading design software company."



EDN magazine works for
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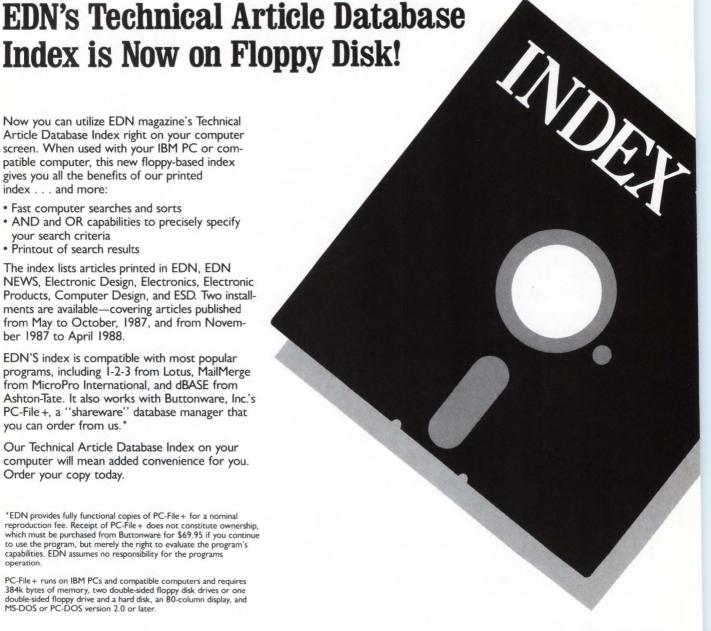
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# LOOKING AHEAD

EDITED BY CYNTHIA B RETTIG

## Hardware outpaces software in information technology

Consistent gains in the price/performance ratio for computerized-information hardware products allow workers at all levels to access more data at lower costs and explore more possibilities in shorter periods of time, thus speeding the decision-making process, according to The Diebold Group Inc (New York, NY). However, the consulting firm found that the development of new kinds of software, like expert systems or new generations of integrated applications, is increasingly expensive and slow to reach the market. Software products thus appear to retard qualitative changes.

During the last two years, Diebold points out, vital improvements or breakthroughs have changed products in nearly every major branch of hardware-based information technology. For most hardware components, manufacturers are using two or more feasible technologies in their products, and other promising technologies are in different stages of research or development. For digital circuitry, the firm points out, the number of basically distinct options has been

### SOME EXPECTED ADVANCES IN INFORMATION TECHNOLOGY

| YEAR | GENERIC TECHNOLOGY COMMERCIALIZED |
|------|-----------------------------------|
| 2000 | 3-DIMENSIONAL SCENE SIMULATION WITH COMPUTER GRAPHICS |
| 2000 | AUTOMATED SIMULTANEOUS TRANSLATION OF MULTILINGUAL CONVERSATIONS |
| 1995 | 16 M-BYTE DYNAMIC RAM SUPER CHIPS |
| 1995 | HEAD-MOUNTED STEREOSCOPIC DISPLAY |
| 1992 | "VISIBLE MEMORY" DISPLAY SCREEN: SURFACE IS DISPLAY MEMORY |
| 1990 | ALL-OPTICAL DIGITAL LOGIC CIRCUITS SUPERCONDUCTIVE CERAMIC LOGIC CIRCUITS |
| 1989 | VOICE-ACTIVATED WORD PROCESSOR, 20,000-WORD VOCABULARY |

*(SOURCE: THE DIEBOLD GROUP INC)*

increasing at the rate of one or two per year. For system and application software, on the other hand, the rate of change is much slower—and the number of viable alternatives far fewer.

One major result of the disparity in the technological-growth rates of hardware and software technology is the steady increase in the ratio of the cost-of-use to the cost-of-acquisition. Today a personal computer has a greater computational power and storage capacity than a mainframe of the mid-sixties or a minicomputer in the mid-seventies, but it costs about 1000 times less. Yet, except for word-processing

and spreadsheet programs, a personal computer demands almost as much time for program development as its more expensive ancestors.

Hardware products are also becoming more reliable and adaptable. For software, increasing functions and speed can mean a reduction in reliability and adaptability. Diebold does point out that software is showing improvements in some areas. Better user interfaces, for example, are reducing the cost of use, and a new generation of integrated tools are appearing for software development.

## Growth in UPS market spawns new strategies

The strong demand for uninterruptible power supplies (UPSs) in the US has captured the attention of both domestic and foreign manufacturers, according to Venture Development Corp (Natick, MA). The 1988 UPS market in the US is estimated to be $789.1 million; it's expected to grow rapidly and reach $1.3 billion by 1991.

Foreign manufacturers have approached the US market both di-

rectly and indirectly. Some foreign companies have established their own marketing and service organizations. Others, such as Fuji Electric and Merlin-Gerin, have legal agreements with US companies that let the domestic companies manufacture and/or market products on behalf of the foreign concern. Only a few foreign UPS manufacturers have actually established themselves as important participants in the US market.

VDC found that, in order to com-

pete in the UPS market, a company has to establish a local presence. Generally, UPS manufacturers don't succeed very well in any distant markets against strong local competition. The market research company concludes that companies must know their markets well, do some research on foreign markets, and perhaps build local production facilities—as well as marketing and service organizations—if they want to offer competitive pricing.