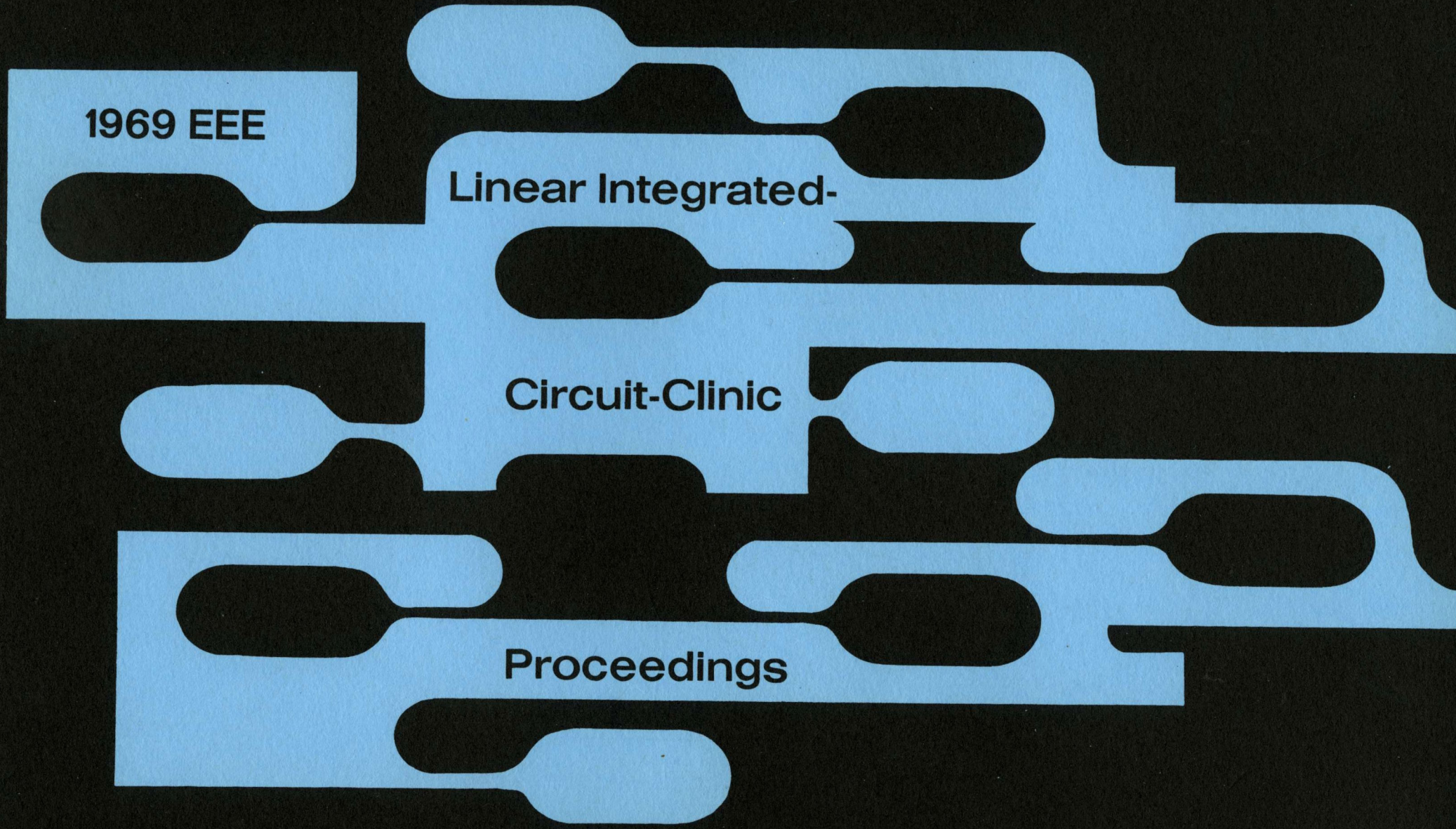

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Staff

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Typing: Carolyn Neilsen
Layout: Carol Verlaan
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1
Factors to Consider In Selecting A Linear Integrated Circuit

by Jerry Eimbinder
EEE Magazine

In choosing a linear integrated circuit (particularly if it's an operational-amplifier IC), finding one that meets your requirements can be only half the job (1). Often there will be many ICs available that you can use. In this case, narrowing down to the one IC best suited for your application can be a truly difficult task.

First of all, the specifications on the data sheet aren't the whole story. Factors often not readily obtainable from the data sheet which can affect your choice include reliability, acceptability and compatibility of the package and the supply requirements, capability to withstand the application's environmental stresses and degree to which the device is accident-proof.

Then, of course, there's price. Prices are rarely, if ever, present on data sheets. But if the device you're looking at is subjected to a lot of tests that you don't need, it's a good bet you'll do better price-wise if you look somewhere else. Ditto if the package is metal and you can get by with plastic, or if the allowable operating temperature range exceeds your requirements.

The rules presented in the following paragraphs can help in selecting that one IC which is right for your application. They are, of course, general rules but applied in conjunction with a little common sense, they can be very helpful.

1.1 RULE 1: DON'T OVERSPECIFY

Decide which specs are critical and which are not. If you're building a voltage regulator with op-amp ICs and there is a large differential voltage during turn-on, you'll have to consider this a very critical parameter. If you're working with a very-high-gain, high-source impedance amplifier, you'll want to consider offset current more critical than offset voltage. If you specify both very tightly, you'll be sending up the cost of the amplifier needlessly.

There are many parameters that can be given for an op-amp IC (for example: input offset voltage and current, input bias current, input impedance, input common-mode range, slew rate, common-mode and power-supply rejection, bandwidth, output drive capability, open-loop gain, drift, noise, dissipation and so on). Certainly, which of these parameters are optimized will vary from IC type to IC type. How the parameters are optimized will depend on the markets at which the IC's manufacturer is aiming (2).

There is usually enough compromise involved in designing a linear IC so that it can fit a variety of applications. Siegel warns, however, that some of the miscellaneous applications suggested on a manufacturer's data sheet, while technically feasible, may be financially ludicrous (3). Gifford indicates which parameters are the key ones for various applications and suggests typical values in "Designing With Linear Integrated Circuits" (4).

1.2 RULE 2: CHECK THE SAFETY FEATURES

Besides selecting which specs you want and which you don't need, you may have to do some choosing regarding safety factors, too. So as part of your elimination procedure, you'll want to check the safety features. One question that should be asked is: can this IC get me into trouble? Problems that will arise under fault conditions should be considered. Will the output become seriously distorted? Will the whole system go up in smoke? Some ICs are more goof-proof than others and this is a factor not to be taken lightly.

For example, op-amp ICs can be bought with or without output short-circuit protection and input overvoltage protection. Since the emitter-to-base junctions of input transistors are sensitive to damage by large applied voltages, some form of input protection may be desirable. Ungrounded soldering irons, excessive input signals and static discharges are all apt to challenge the input of the IC.

1.3 RULE 3: WEIGH COST AGAINST PERFORMANCE

Of course, when you add any features, even ones concerned with safety, you've got to consider how they'll affect the overall cost--not just the immediate cost of the chip. Reducing the cost of building or maintaining the system, however, should justify adding to the chip cost.

Cost, understandably, keeps getting into the picture during the evaluation of an IC. Throughout the elimination process you must continually weigh cost against performance. From an economical standpoint, a designer today, should be looking at operational-amplifier ICs that require little or no compensation. The prices of resistors and capacitors are bottoming out; to save money in the future, you'll have to eliminate these components by incorporating them on the chip. But, on the other hand, if you're planning to use a fully compensated op-amp IC right now, better make sure you're not limiting yourself frequencywise.

Judging cost is complicated by the fact that determining the overall system cost involves guesswork. Nevertheless, it shouldn't be too difficult to decide, for example, if using a dual op-amp IC instead of two separate units or a high-gain amplifier instead of two low-gain amplifiers are economical moves. Although if, as in the case of the dual op-amp IC, the close temperature tracking of two circuits on one chip is especially desirable, the weighing becomes more complex.

Reducing "can count" (the number of packages used) is generally a good idea from a reliability standpoint but the designer should make sure that this doesn't adversely affect flexibility and performance.

1.4 RULE 4: CONSIDER FREQUENCY COMPENSATION

The frequency compensation that will be required differs widely among commercially available op-amp ICs. At one time, in fact, opponents of op-amp ICs cited the need for frequency-compensation networks as the prime reason for not using op-amp ICs.

The discrete components required for frequency compensation do add to the space requirements and assembly cost. Various arrangements used for commercially available op-amp ICs can require from zero to seven components[5] depending on the IC and application. Certainly, it is of key importance for the designer to consider frequency compensation. He should look at the op-amp IC and attempt to determine how prone it is

to oscillation if the supply is not exactly bypassed properly. The IC should be evaluated to see how prone it is to oscillation with varying capacitive loads and how probable it is that stray capacitance around the circuit will send it into oscillation.

Too much bandwidth in an amplifier can work against you. Extra capacitors may be needed across the feedback resistors to prevent oscillation.

1.5 RULE 5: COMPARE THE SPECIFICATIONS OF VARIOUS VENDORS

It's essential to understand the nature of the input signal and to spell out what the worst-case conditions will be in terms of voltage swing, noise, supply variations, etc. If this is done, you're in a good position to compare the specs of various vendors. In working with the data sheets of IC manufacturers, care should be exercised in checking to see if the test conditions of both manufacturers are the same for a particular characteristic.

For example, if you're comparing offset voltages, see if the source impedances specified by both manufacturers are the same. If you're looking at slew rate, make sure both manufacturers are doing their measuring at the same gain.

Op-amp specifications are evolved from nonlinear characteristics and as Stata warns (6), it's not surprising if the circuit doesn't "play the first time around."

It's common practice for a semiconductor-device manufacturer to spec his product under favorable operating conditions. Therefore the user must also attempt to relate the data sheet information to his own application.

Widlar points out (7) that it's difficult to get the whole story on any IC from a data sheet. He notes that the IC must also be designed so that it's operation isn't erratic under certain conditions.

He also points out that it's not difficult to design an IC that will satisfy the requirements of a specific application and that can be manufactured with reasonable yield. The real trick, he says, is to design an IC which can be used in hundreds of different applications without complaints from the users.

Examples of IC assets that may not show up on the data sheet, cited by Widlar, include continuous short-circuit protection, capability not to latch up or perform erratically when the inputs are driven outside their operating range, ease in determining correct compensation and reliability.

1.6 RULE 6: CHECK THE PRODUCT's HISTORY

A lot of people think that IC manufacturers leave reliability information off their data sheets for these two reasons: IC reliability doesn't vary much from manufacturer to manufacturer and customers won't put much stock in the IC makers' figures. Actually the real reason for the absence of this information on the spec sheet is rather simple: the IC makers just don't have it when they publish the spec sheet.

Spec sheets are prepared just before ICs are announced and there's insufficient time to run lifetest programs. Even after new ICs come out, the IC manufacturers are constantly modifying their masks and processing procedures to improve yields or performance.

For example the manufacturer may reduce the size of an individual die to increase the number of die per wafer. Conversely, he may find that there is some interaction

between active elements because the transistor locations on the chip are too close to each other. Possibly he may want to reduce the length of extra long metal interconnection patterns.

So how do you judge the reliability of competitive ICs? Some engineers believe that there is a relationship between noise and reliability. This has been disputed, however, and discounted by several top semiconductor-device authorities, including National Semiconductor's Bob Widlar.

There's a good possibility that you won't have enough time to run your own lifetests and even if you do, the manufacturer may change the device six times during the course of your test program. Instead you'll be better off if you check the product's history. Find out if there are other applications similar to yours in which the same device has been used with success. For that matter, see how successful the manufacturer has been with products of this type. Is this his first attempt at it or does he have a long history of developing such devices?

Some designers refuse to use any ICs that aren't available from several sources. While this policy will usually keep you out of trouble if your main source of supply dries up, it has one drawback. It could be a year or two before you can take advantage of advancements in the state-of-the-art (8).

If a new IC looks good and you decide to use it, you're gambling that either it's so good other companies will add it to their lines or the original supplier can be depended upon to continue supplying it. There's an American washing-machine manufacturer who guarantees to make every part used in his products available for 35 years. You won't get any such warrantees in the semiconductor business.

Some IC manufacturers will hold units in bonded stock for possible future purchase; however a higher price per unit is usually paid as a premium. Depending on the terms of the contract, the customer may wind up paying for the whole inventory even if he doesn't use it (8).

1.7 RULE 7: SEE IF THE IC LENDS ITSELF TO MASS PRODUCTION

But if that new IC really looks good and it can put you one step ahead of your competition, then see if the circuit lends itself to mass production. This isn't easy to determine, but if the circuit is very complex, the chip is large and the vendor has had delivery problems in the past, you may have reason to be nervous.

You might keep in mind that the more complex the chip, the greater the cost, and, quite possibly, the lower the yield. This doesn't mean that you should shy away from complex chips; but if the chip's crammed with a wide variety of tight-tolerance, difficult-to-make components, look out.

1.8 RULE 8: CONSIDER THE PROBABILITY OF WIDE ACCEPTANCE OF THE IC

At this point of your evaluation, you could also consider the probability of wide acceptance of the IC. If the volume won't be significant, obviously the cost isn't going to drop measurably in the future. However, if the IC's versatile, the chances of its being second-sourced are much improved.

The prices of newly announced ICs are based primarily on developmental costs, anticipated yield and projected sales volume. But even the best guesswork by an IC

manufacturer can't accurately determine what his competition is going to do. If a number of his competitors jump in, the price will go down.

It's wise to keep in mind that if a new IC appears to have characteristics that could limit its appeal (such as inconvenient supply requirements or elaborate compensation-network requirements), it could be a poor choice even though it meets the application's needs.

1.9 RULE 9: CHECK FOR APPLICABLE LITERATURE

One factor, sometimes overlooked, is evaluating your own capability to work with a product. First of all, is your knowledge of the product adequate for you to design it into your application? In this area, it's important to check for availability of application literature published by the IC manufacturer. This will not only help you engineer the product into your circuit, it'll also give you a good indication of how much the IC maker knows about the use of his own product.

The publishing of applications literature on linear ICs, fortunately, has been extensive. However, because of the rapid progress of the IC industry, some of the material that has been published suggests design solutions that are no longer economically feasible. Care should be exercised in using older linear IC literature as design criteria.

1.10 RULE 10: EVALUATE THE TESTING ASPECTS

Finally, if you can understand and design with the IC, can the rest of your company handle it? Will special assembly rigs have to be built to accommodate the package? Undoubtedly you'll have to evaluate the testing aspects. With IC manufacturers going to more and more complex chips, incoming inspection and testing are becoming more involved.

Questions which arise concerning inspection are: is the plant facilitated to thoroughly check out the devices? Can existing test equipment be modified and used or must new equipment be obtained? The IC user will have to test the devices when they arrive and he'll also have to determine how they'll be tested in completed systems by field maintenance personnel (9).

Every application has its own unique problems, but, regardless of the specific problems being encountered, the ten general rules mentioned in this chapter shouldn't be overlooked. By applying them, deciding which op-amp IC to use should become an easier chore.

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2
Interpreting Operational-Amplifier Specifications

by Ray Stata
Analog Devices

Operational amplifiers are complicated. They have many specifications, and most are only approximations of what's happening in the black box. Most parameters like voltage drift, current drift and open-loop gain are nonlinear functions of temperature; others, like common-mode rejection and common-mode impedance, are nonlinear functions of input voltage. And almost all parameters depend on supply voltages. Therefore, when you use a single number to specify a parameter, you must qualify the conditions of the measurements. Comprehensive graphs would be necessary to define performance completely.

Confronted with 50 more-or-less mysterious numbers, most engineers tend to select an op amp in terms of familiar values and to forget about the rest. An engineer who wants to replace a sensitive relay with a low-cost amplifier might simply concern himself with the output-current rating and neglect such factors as drift or gain.

2.1 THE LACK OF STANDARDS

Then there's the lack of standards for op-amp specs. Though various efforts have been made to unify terms throughout industry, this has not yet been done, so manufacturers have loopholes for specsmanship.

Along with real, honest-to-goodness specsmanship, we find the inadvertent errors of omission. The holes in the spec, or usually, the lack of additional information, is not revealed until the engineer has assembled umpteen amplifiers into his product and the whole batch is waiting to be shipped.

In one case, a customer purchased a diff amp with a 5 $\mu V/^{o}C$ drift spec. The data sheet said that this number meant maximum voltage drift. What the sheet neglected to say was that the specs held only for steady-state temperature conditions. What happened during thermal transients was another kettle of fish that no numbers covered.

Though we were able to show that this point had been covered in an early application note, we certainly hadn't referred to it in spec sheets for any amplifiers. Actually we didn't know how to specify this mode of operation quantitatively. And some competitors had omitted the point.

Now, let's take a closer look at some of the major specifications and see how these problems come up.

2.2 VOLTAGE DRIFT

It can help to go back to first principles. We all know that a transistor's base-emitter voltage varies at roughly 2400 microvolts for every degree C change. This variation develops an output, or offset, exactly as if a true input of equal magnitude were driving the transistor. The use of differential pairs enables the net voltage offset to be drastically reduced because both transistors can be matched so their offsets track within a few microvolts over the temperature range. This is how the amplifier comes to have a drift spec of 5 $\mu V/^{o}C$ instead of 2400 $\mu V/^{o}C$; the transistors track within 5 μV for every 2400 μV of base-emitter drift, that is, for every $1^{o}C$ rise.

But there's a flaw here. What happens if the base-emitter junctions are not at the same temperature? The spec states a figure for maximum drift, but this is really a tracking spec for base-emitter junctions at the same temperature.

2.3 THERMAL CONSIDERATIONS

Obviously, thermal gradients caused by adjacent heat-dissipating components can make nonsense of such specifications by making one junction hotter than the other. It only takes 0.1°C differential between the two junctions to develop 2400/10 = 240 microvolts offset. To say the least, this is a substantial offset for an op amp with a 5 μV/°C max drift spec.

In fact, offsets are caused not only by such obvious temperature-gradient sources as adjacent heat-dissipating elements and room-air drafts, but also by changes in the amplifier's own load current. Altering the output current from 2 mA to 20 mA produces an internal temperature transient that develops an offset due to unequal heating of the input transistor pair until temperature equilibrium is re-established. And when the amplifier has settled to its new output level, the input signal will invariably set the load current back to 2 mA, starting the problem all over again.

Offsets due to warmup and changes in operating conditions can be particularly annoying when an instrument or system is being adjusted. It takes only finger heat on one side of a differential amplifier to produce a distinctly-measurable offset error. How does one put performance specifications on such nebulous factors?

One way to sidestep the temperature-gradient error is to avoid the differential amplifier. A chopper-stabilized amplifier corrects automatically for transient offsets of this kind. Its error-sensing circuit is independent of mismatches between the transistors. But sometimes the chopper unit won't win. Apart from being twice as big and costly as a differential amplifier, the chopper-stabilized unit has only a single input terminal. (The other terminal is "used up" in the stabilizing circuit.) A single-ended amplifier can't easily be used in noninverting or differential circuits. So what you gain on the roundabouts breaks the rope on the swings.

Fortunately, some diff amps are inherently less susceptible to temperature gradients. Single-chip dual-transistor front-end circuits cut down thermal inertia and reduce physical spacing between base-emitter junctions of each differential pair. Monolithic IC op amps are generally good on this score because of the small spacing between junctions.

Consequently, temperature transients never pull the two junctions more than a few hundredths of a degree apart. Such amplifiers offer a meaningful steady-state maximum voltage drift of about 1 μ/V°C, with a short-lived and worst-case offset of about 75 microvolts for 40°C thermal shock.

While an amplifier with a dual input transistor exhibits a considerable improvement in offset stability, there is no way to discern this fact in comparing the usual published offset-drift specifications. A user can get some idea of comparative thermal-gradient performance by making thermal shock tests, like dropping the amplifier in an oil bath 40°C above ambient. He'll get a response like the one shown in Figure 2.1.

Okay, so we've raised one straw man and then beaten it down. But aren't there other problems that only specsmanship has solved thus far?

2.4 ZEROING CAN HIDE SECOND-ORDER DEFECTS

What happens when you adjust an amplifier's offset potentiometer to zero its output at the selected working temperature? Not surprisingly, there's more to the process than meets the eye. And it's not always easy to tie up the sources of error in neat, crisp numbers.

The offset pot is frequently a variable resistor in series with a collector load resistor. The amplifier's output is zeroed by altering collector current to change voltage balance between the two front-end transistors.

So what? Well, it turns out that there's a second-order effect that causes interaction between the actual value of collector current and the rate at which the transistor's base-emitter voltage drifts with temperature. Adjust collector current in one transistor of a matched differential pair and it no longer tracks the other as temperature varies. True, the adjustment modifies the base-emitter drift by only 0.7 $\mu V/^{o}C$ for each 250 μV change in emitter-base voltage or initial offset voltage.

But such differences can swamp the carefully-designed tracking specs of today's state-of-the-art differential amplifiers. For example, some chopperless differential amplifiers have better than 1 $\mu V/C^{o}$ maximum voltage drift. To zero an initial offset voltage of 1 mV with the internal balance pot in one of these amplifiers would introduce a change in temperature drift of 2.8 $\mu V/^{o}C$. And that really screws up the works.

Some manufacturers neglect to point out the second-order effects caused by trimmer adjustments, but as op amp specs improve these effects can no longer be ignored. One must really know the condition of the balance resistor to specify voltage drift uniquely. We get around this by eliminating provisions for an internal offset trim on low-drift amplifiers and by recommending external offset biasing circuits.

2.5 AVERAGE DRIFT

Average drift is a trap. Remember the man who drowned while wading through a stream with an average depth of only four feet? Neither voltage drift nor current drift are linear functions of ambient temperature. Accordingly, the numbers published for voltage drift and bias-current drift can refer only to average values, or to values at specific operating conditions. For example, an amplifier's total change in voltage offset for a temperature excursion from -25 to $+85^{o}C$ might be 2200 microvolts (referred to the input). The average drift rate over this interval works out to $2200/110^{o}$ or 20 $\mu V/^{o}C$. But when you look at the actual drift curve you see that the drift rate at the extremes of temperature can exceed the specified average drift rate by a substantial amount (see Figure 2.2).

You have a special problem when the drift curve changes slope - a real live possibility. Here the average slope calculated by subtracting end points is entirely meaningless. Nonetheless, some manufacturers have taken advantage of this golden opportunity for specsmanship (see Figure 2.3).

Perhaps trickier to interpret than the voltage-drift figures are the nonlinear errors caused by exponential variation of bias currents in FET and varactor-bridge amplifiers. Usually, the bias current at a given temperature is specified, and the spec reader is reminded that the bias current doubles for approximately 10°C temperature rise as illustrated in Figure 2.4.

If a value of bias-current drift is given, it is usually quoted at room temperature, where the slope of the bias current versus temperature curve (i.e., drift) is shallowest. But at 85°C, the bias current and drift slope will be 64 times worse than at room temperature, making the FET amplifier a worse choice for high-temperature applications than some bipolar transistor types. This is not really a question of specsmanship, but it certainly requires that the user know his way around a spec sheet.

2.6 OUTPUT

An amplifier output rating of ±10 volts, ±20 milliamps implies that the user can drive a 500-ohm load at the full signal swing of 10 volts, 20 milliamps. For discrete-component op amps this is usually what such specs mean. But some integrated circuit manufacturers have a different interpretation. "Sure you can get 10 volts output; certainly it will develop 20 milliamps," they say, but they often forget to add, "so long as you don't ask for them simultaneously." In fact, it is not unusual for an IC amplifier labeled as having a ±10 V, ±5 mA output to have a maximum power rating of only a fraction of the product of the VI figures given.

If an engineer needs an op amp with a relatively high output, he generally wants to know what gain he's getting at that current level. If 20 mA is the amplifier's full-load rating, it would be nice and simple if the manufacturer stated the amplifier's open-loop dc gain at this full load. Not all manufacturers do.

The op-amp user should know his amplifier's roll-off curve in order to build a circuit with adequate gain stability over the working frequency range. The manufacturer may be perfectly justfied in departing from the conventional 6 dB/octave frequency compensation to achieve desirable features like fast settling time, high slew rate, fast overload recovery, or increased gain stability over a wide range of frequencies.

But to obtain these improved features generally requires fast roll-off characteristics and therefore a propensity toward oscillation. Key to preventing instability, of course, is knowing that you have this kind of amplifier. You can then use one or more well known circuit techniques to tame the oscillations.

The great crime occurs when manufacturers use fast roll-off compensation to obtain improved published specs without giving an open-loop response curve or some other indication of what's going on.

2.7 COMMON-MODE SPECIFICATIONS

To many users the common-mode rejection ratio of an amplifier is a rather mysterious number that they'd like to forget. Many op-amp manufacturers feel the same way. In fact, if a particular amplifier has a poor common-mode spec, some manufacturers thoughtfully omit it from the data sheet.

Low-cost FET amplifiers are the worst culprits, with typical common-mode rejection ratios around 1000. This is exactly the kind of number that manufacturers would like

to lose. They often do. For a noninverting amplifier circuit, the common-mode error is 1/CMRR, which works out to 0.1% for an amplifier with CMRR of 1000, or 60 dB. Recently, new circuit tricks have enabled manufacturers to overcome this fundamental limitation of low CMRR, but a FET amplifier with 100,000 CMRR tends to cost more than $100.

Picking a typical CMRR spec from measured op-amp data is great sport. The numbers vary over an enormous range -- from 500:1 to as high as 100,000 for FETs -- all seemingly at random. A reasonable way for a manufacturer to select a typical common-mode figure for his data sheet is to pick a value that is met by 70 or 80% of all units of that particular type. Some manufacturers, with considerable ingenuity, average all the test numbers to find a "typical" value. Tweaking up a few samples to get 100,000 CMRR can do great things for averages of this kind and can, of course, lead to very respectable-looking common-mode rejection figures.

As with drift, an amplifier's common-mode-rejection performance can vary with operating conditions, notably with the value of common-mode input voltage as we can see in Figure 2.5. This leaves room for some really fancy footwork. For example, some well known FET types boast a common-mode voltage range of $\pm$10 volts. But the common-mode rejection figures are specified for a $\pm$5-V common-mode range. It's possible for the CMRR to degrade by as much as a factor of ten when the applied common-mode voltage is raised from 5 to 10 volts (see Figure 2.5).

Another difficulty with CMRR is that, since it's a nonlinear function of input common-mode voltage, a single spec number can at best give an average value over the test-voltage range. For small input-signal variation about some large common-mode voltage, the specified "average" CMRR gives little indication of the actual errors you can expect due to the steeper error slope at high voltages.

2.8 FULL-POWER RESPONSE

We all know that an amplifier rated at, say, 10-MHz unity-gain bandwidth, doesn't give full output-voltage swing at this frequency. Invariably, distortion caused by internal slew-rate limiting induces the manufacturer to specify the maximum full-power frequency several decades lower.

Generally, an amplifier with 10-MHz unity-gain bandwidth would have a full-power response of about 1 MHz or maybe as low as 100 kHz. At the "small signal" unity-gain bandwidth, the achievable output-voltage swing is usually related to the swing at the full-power bandwidth by the ratio of the full-power response, f_p, to the unity-gain bandwidth, f_t. Thus, for example, you get only a 100-mV swing from a 10-V amplifier at unity-gain bandwidth for an amplifier with an f_p of 100 kHz and an f_t of 10 MHz.

One large problem with full-power-response specs is that no one really says what he means by the published minimum number. For one thing full-power response has nothing to do with amplitude vs frequency as the term "response" normally implies. Instead it is a measure of output distortion caused by slew-rate limiting.

But there can be monstrous difference depending on whether you set 1% or 10% as the acceptable distortion level. We have evaluated some amplifiers where the output looks a triangle at the specified full-power response. Where do you draw the line on the

acceptable distortion level?

Distortion is only one consideration in setting the criteria for the full-power-response spec. A subtle, but very often more important side effect, is dc offset error due to rectification. Feedback signals developed by an unsymmetrical, distorted output, will not counter-balance the input signal at the amplifier's summing junction. So, the error signal is rectified by the amplifier's input stage, generating an undesirable offset voltage.

But how can such application factors be reasonably prevented? Should each data sheet be turned into a thesis, or may the manufacturer assume that his customers are already aware of the difficulties awaiting them? There is no easy answer for either the manufacturer or the customer.

Slewing rate for the most part is just another way of looking at rate limiting of the amplifier's circuitry. The slewing-rate specification applies to transient response while full-power response applies to steady state or continuous response. For a step-function input, slewing rate tells how fast the output voltage can swing from one voltage level to another. Fast amplifiers will slew at up to 300 V/μs, while amplifiers designed primarily for dc applications often slew at 0.1 V/μs or less.

Maximum slew rate, S, is related to full-power response f_p by

$$S=2 f_p E_o. \qquad (2.1)$$

As the voltage swing is reduced below the peak output, E_o, the operating frequency can be proportionately increased beyond f_p without exceeding the slewing rate. For many amplifiers the slewing rate may differ in the inverting and noninverting configurations -- a fact that is not always apparent from published specs. Moreover, there is almost always a difference in slewing rate between fall time and rise time, and between positive and negative output signals. Opportunities for specs-manship arise here since many possible slopes can be measured.

A recurrent complaint by customers is that an amplifier does not meet its slewing-rate spec. Closer inquiry typically shows that the customer is trying to obtain 100 V/μs slew rate with a circuit like the one in Figure 2.6.

The problem here is that the inevitable 1 pF of stray capacitance must be charged by the 10-μA signal current. This limits theoutput slew rate to 10 V/μs regardless of how fast the op amp may be. With an input impedance of 10 KΩ or less, the customer would obtain the desired 100 V/μs slewing rate. In other words, you cannot get fast response from an inverting amplifier when using high input impedance owing to the slugging effect of stray capacitance.

2.9 SETTLING TIME

Settling time is a parameter of increasing interest. This spec defines the time required for the output to settle within a given percentage of final value in response to a step-function input. Common accuracies of interest are settling time to 0.1% and 0.01%. Heretofore, engineers have been forced to use slewing rate and unity-gain bandwidth as rough indicators of relative settling-time performance when comparing or choosing amplifiers, since no other data are given. As it turns out, these two specs have little bearing on settling time, particularly to 0.01%.

Manufacturers now realize this and are beginning to publish settling-time figures.

The hooker here is that settling time is really a closed-loop parameter (while all other op-amp specs are open-loop parameters), and therefore depends on the closed-loop configuration and gain. Fortunately, even when published for only one gain, usually unity gain, it serves as a realistic yardstick for comparing amplifier performance.

The few examples I've shown illustrate the tremendous difficulties in specifying op-amp performance and the many pitfalls confronting the user. In the long run the user and manufacturer are on the same side in seeking unambiguous communications.

There's one further point that can be most important of all. An engineer should breadboard his critical circuits instead of relying totally on paper designs.

FIGURES

Figure 2.1. Offset voltage characteristic after subjecting amplifier to oil bath at a temperature 40°C above ambient.

Figure 2.2. Curves illustrating that average drift values can conceal the presence of larger actual drift values.

Figure 2.3. Curve illustrating that average slope calculated by subtracting end points can be meaningless.

Figure 2.4. Bias current as a function of temperature.

Figure 2.5. CMRR is a nonlinear function; a single spec number at best gives only an average value over the test-voltage range.

Figure 2.6. In the circuit shown regardless of the op amp's speed, the slew rate is limited by the 1 pF of stray capacitance. As a result, the slew rate is limited to 10 V/μs.

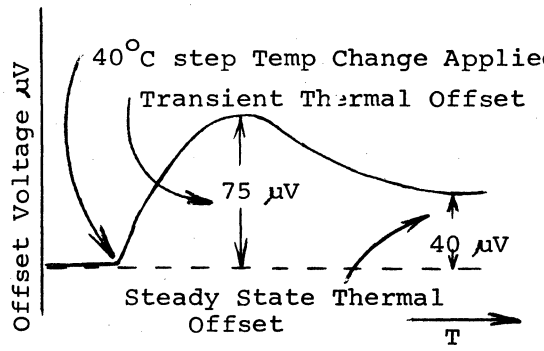

Figure 2.1. Offset voltage characteristic after subjecting amplifier to oil bath at a temperature 40°C above ambient.

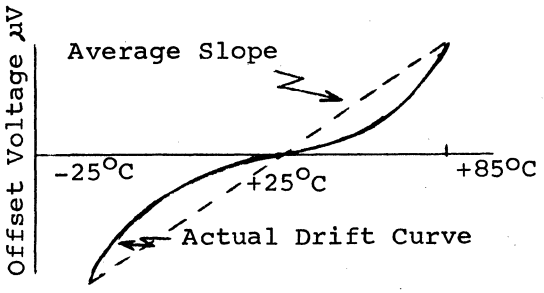

Figure 2.2. Curves illustrating that average drift values can conceal the presence of larger actual drift values.

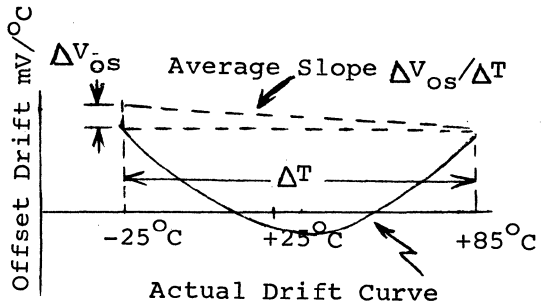

Figure 2.3. Curve illustrating that average slope calculated by subtracting end points can be meaningless.

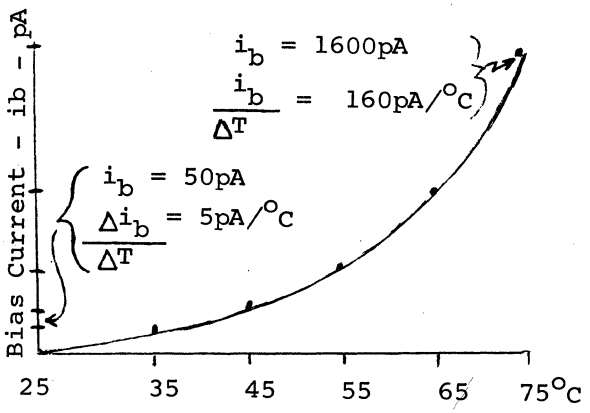

Figure 2.4. Bias current as a function of temperature.

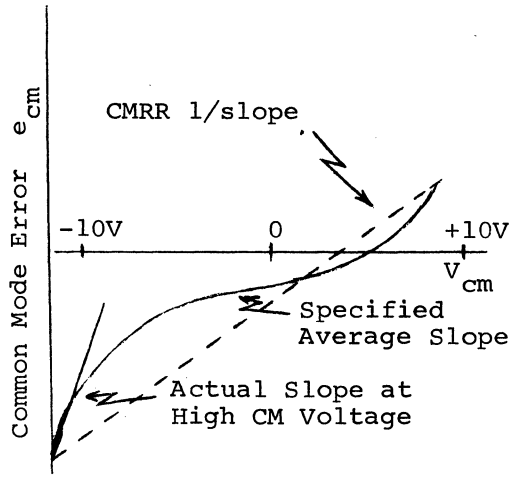

Figure 2.5. CMRR is a nonlinear function; a single spec number at best gives only an average value over the test-voltage range

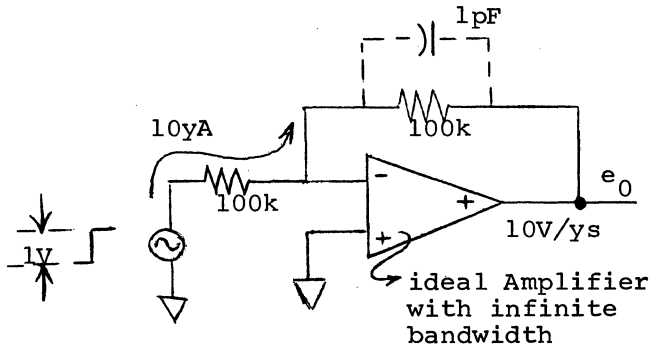

Figure 2.6. In the circuit shown regardless of the op amp's speed, the slew rate is limited by the 1 pF of stray capacitance. As a result, the slew rate is limited to 10 V/μs.

3
Applications for Operational Amplifiers

By William Routh
National Semiconductor

The usefulness of the operational amplifier is derived from the fact that it can be used in a feedback loop whose feedback properties determine the feed-forward characteristics of the amplifier and the loop combination. To suit it for this use, the ideal operational amplifier would have infinite input impedance, zero output impedance, infinite gain and an open-loop 3-db down point at infinite frequency rolling off at 6 db per octave. Unfortunately, the cost, in quantity, of such an amplifier would also be infinite.

Intensive development of the operational amplifier, particularly in integrated form, has resulted in circuits which are quite good approximations of the ideal for finite cost. Quantity prices for the best contemporary integrated amplifiers are low compared with transistor prices of five years ago. The low cost and high performance provided by these amplifiers permits their being designed into equipment and systems functions impractical with discrete components. An example is a low-frequency function generator which may use 15 to 20 operational amplifiers in generation, wave shaping, triggering and phase-locking.

The availability of the low-cost integrated operational amplifier makes it mandatory that systems and equipment engineers be familiar with operational-amplifier theory (1-4). This chapter will present amplifier applications ranging from a simple unity-gain buffer to relatively complex generator and wave-shaping circuits, all taking advantage of the operational amplifier's characteristics.

The discussion is shaded toward the practical; amplifier parameters will be discussed as they affect circuit performance, and application restrictions will be outlined.

The applications to be covered are arranged in order of increasing complexity in five categories: simple amplifiers, operational circuits, transducer amplifiers, wave shapers and generators, and power supplies. The integrated amplifiers shown in the circuit diagrams are for the most part internally compensated so frequency stabilization components are not used; however, as the discussion will show, other amplifiers may be used with stabilization components in many of these circuits to achieve greater operating speeds.

3.1 THE INVERTING AMPLIFIER

The basic operational-amplifier circuit is shown in Figure 3.1. This circuit, as the name implies, inverts. It offers a closed-loop gain of R_2/R_1 provided that this ratio is small compared with the amplifier open-loop gain. The input impedance is equal to R_1; the closed-loop bandwidth is equal to the unity-gain frequency divided by one plus the closed-loop gain.

The only precautions to keep in mind when using this circuit are 1) that R_3 should be chosen to be equal to the parallel combination of R_1 and R_2 (to minimize the offset-voltage error due to bias current), and 2) there will be an offset voltage at the amplifier output equal to the closed-loop gain times the offset voltage at the amplifier input.

Offset voltage at the input of an operational amplifier is comprised of two components, these components are identified in specifying the amplifier as input offset voltage and input offset current. The input offset voltage is fixed for a particular amplifier, however the contribution due to input offset current is dependent on the circuit configuration used. For minimum offset voltage at the amplifier input without circuit adjustment the source resistance for both inputs should be equal. In this case the maximum offset voltage would be the algebraic sum of the amplifier offset voltage and the voltage drop across the source resistance due to offset current. Amplifier offset voltage is the predominant error term for low-source resistances and offset current produces the main error for high-source resistances.

In high-source resistance applications, offset voltage at the amplifier output may be set by adjusting the value of R_3 and using the variation in voltage drop across it as an input-offset-voltage trim.

Offset voltage at the amplifier output is not as important in ac coupled applications. Here the only consideration is that any offset voltage at the output reduces the peak-to-peak linear output swing of the amplifier.

The gain-frequency characteristic of the amplifier and its feedback network can team up to cause oscillation. To avoid this condition, the phase shift through the amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is a situation of conditional stability. Obviously the most critical case occurs when the attenuation of the feedback network is zero.

Amplifiers which are not internally compensated may be used to achieve increased performance in circuits where feedback network attenuation is high. As an example, the LM101 may be operated at unity gain in the inverting amplifier circuit with a 15-pF compensating capacitor since the feedback network has an attenuation of 6 dB; this IC however requires 30 pF in the non-inverting unity-gain connection where the feedback network has zero attenuation. Since amplifier slew rate is dependent on compensation, the LM101 (op-amp IC) slew rate in the inverting unity gain connection will be twice that for the non-inverting connection and the inverting-gain-of-ten connection will yield ten times the slew rate of the non-inverting, unity-gain connection. The compensation trade-off for a particular connection is stability versus bandwidth; larger values of compensation capacitor yield greater stability and lower bandwidth and vice versa.

The preceding discussion of offset voltage, bias current and stability applies to most amplifier applications and will be referenced in later sections. A detailed treatment has been given by Paynter (4).

3.2 THE NON-INVERTING AMPLIFIER

A high input impedance non-inverting circuit is shown in Figure 3.2. This circuit gives a closed-loop gain equal to the ratio of the sum of R_1 and R_2 to R_1 and a closed-loop 3-dB bandwidth equal to the amplifier unity-gain frequency divided by the closed-loop gain.

The primary differences between this circuit arrangement and the inverting circuit are 1) the output is not inverted and 2) the input impedance is very high and is equal to the differential input impedance multiplied by loop gain. (Open-loop gain/ Closed-loop gain.) In dc coupled applications, input impedance is not as important as the input current and the voltage drop across the source resistance.

Application cautions are the same for this amplifier as for the inverting amplifier with one exception. The amplifier output will go into saturation if the input is allowed to float. This may be important if the amplifier must be switched from source to source. The compensation trade off discussed for the inverting amplifier is also valid for this connection.

3.3 THE UNITY-GAIN BUFFER

The unity-gain buffer is shown in Figure 3.3. The circuit gives the highest input impedance of any operational-amplifier circuit. Input impedance is equal to the differential input impedance multiplied by the open-loop gain, in parallel with common-mode input impedance. The gain error of this circuit is equal to the reciprocal of the amplifier open-loop gain or to the common-mode rejection, whichever is less.

Input impedance is a misleading concept in a dc coupled unity-gain buffer. Bias current for the amplifier will be supplied by the source resistance and will cause an error at the amplifier input due to its voltage drop across the source resistance. Since this is the case; a low-bias-current amplifier such as the LH102 (6) should be chosen as a unity-gain buffer when working from high source resistances. Bias current compensation techniques have been covered by Widlar (5).

Three important considerations in the use of this circuit are 1) the amplifier must be compensated for unity gain operation, 2) the output swing of the amplifier may be limited by the amplifier common-mode range, and 3) some amplifiers exhibit a latch-up mode when the amplifier common-mode range is exceeded. The LH101 if used in this circuit eliminates these problems; for faster operation, the LM102 may be chosen.

3.4 SUMMING AMPLIFIER

The summing amplifier, a special case of the inverting amplifier, is shown in Figure 3.4. The circuit gives an inverted output which is equal to the weighted algebraic sum of all three inputs. The gain of this circuit for any input is equal to the ratio of the appropriate input resistor to the feedback resistor, R_4. Amplifier bandwidth may be calculated as in the inverting amplifier shown in Figure 3.1 by assuming the input resistor to be the parallel combination of R_1, R_2, and R_3. Application cautions are the same as for the inverting amplifier. If an uncompensated amplifier is used, compensation is calculated on the basis of bandwidth as is discussed in the section describing the simple inverting amplifier.

The advantage provided by this circuit is that no interaction occurs between inputs, operations such as summing and weighted averaging are implemented very easily.

3.5 THE DIFFERENCE AMPLIFIER

The difference amplifier is the complement of the summing amplifier; it allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to the two inputs. This circuit is shown in Figure 3.5 and is useful as a

computational amplifier, in making a differential to single-ended conversion or in rejecting a common-mode signal.

Circuit bandwidth may be calculated in the same manner as for the inverting amplifier, but input impedance is somewhat more complicated. Input impedance for the two inputs is not necessarily equal; inverting input impedance is the same as for the inverting amplifier of Figure 3.1 and the noninverting input impedance is the sum of R_3 and R_4. Gain for either input is the ratio of R_1 to R_2 for the special case of a differential input single-ended output where $R_1 = R_3$ and $R_2 = R_4$. The general expression for gain is given in the figure. Compensation should be chosen on the basis of amplifier bandwidth.

Care must be exercised in applying this circuit since input impedances are not equal for minimum bias current error.

3.6 DIFFERENTIATOR

The differentiator is shown in Figure 3.6 and, as the name implies, is used to perform the mathematical operation of differentiation. The form shown is not the practical form, it is a true differentiator and is extremely susceptible to high-frequency noise since ac gain increases at the rate of 6 dB per octave. In addition, the feedback network of the differentiator, R_2C_1, is an RC low-pass filter which contributes 90° phase shift to the loop and may cause stability problems even with an amplifier which is compensated for unity gain.

A practical differentiator is shown in Figure 3.7. Here both the stability and noise problems are corrected by the addition of two components, R_1 and C_2. R_2 and C_2 form a 6 dB per octave high-frequency roll-off in the feedback network and R_1C_1 form a 6 dB per octave roll-off network in the input network for a total high-frequency roll-off of 12 dB per octave to reduce the effect of high-frequency input and amplifier noise. In addition R_1C_1 and R_2C_2 form lead networks in the feedback loop which, if placed below the amplifier unity gain frequency, provide 90° phase lead to compensate the 90° phase lag of R_2C_1 and prevent loop instability. A gain-frequency plot is shown in Figure 3.8 for clarity.

3.7 INTEGRATOR

An integrator is shown in Figure 3.9. This circuit performs the mathematical operation of integration. It is essentially a low-pass filter with a frequency response decreasing at 6 dB per octave. An amplitude-frequency plot for the circuit is shown in Figure 3.10.

The circuit must be provided with an external method of establishing initial conditions as shown in the figure by S_1. When S_1 is in position 1, the amplifier is connected for unity-gain and capacitor C_1 is discharged, setting an initial condition of zero volts. When S_1 is in position 2, the amplifier is connected as an integrator and its output will change in accordance with a constant multiplied by the time integral of the input voltage.

Precautions to be observed with this circuit are: the amplifier used must in all cases be stabilized for unity-gain operation and R_2 must equal R_1 for minimum error due to bias current.

3.8 SIMPLE LOW-PASS FILTER

A simple low-pass filter is shown in Figure 3.11. This circuit has a 6 dB per octave roll-off after reaching a closed-loop 3-dB point defined by f_c. Gain below this corner frequency is defined by the ratio of R_3 to R_1. The circuit may be considered as an ac integrator at frequencies well above f_c; however, the time domain response is that of a single RC rather than an integral.

The value of R_2 should be chosen so that it is equal to the parallel combination of R_1 and R_3 thus minimizing errors due to bias current. Either the amplifier should be compensated for unity-gain or an internally compensated amplifier should be used.

A gain-frequency plot of the circuit response is shown in Figure 3.12 to illustrate the difference between this circuit and the true integrator.

3.9 THE CURRENT-TO-VOLTAGE CONVERTER

Current may be measured in two ways with an operational amplifier. The current may be converted into a voltage using a resistor and then amplified or the current may be injected directly into a summing node. Converting into voltage is undesirable for two reasons: first, an impedance is inserted into the measuring line causing an error; second, amplifier offset voltage is also amplified with a subsequent loss of accuracy. The use of a current-to-voltage transducer avoids both of these problems.

The current-to-voltage transducer is shown in Figure 3.13. The input current is fed directly into the summing node and the amplifier output voltage changes to extract the same current from the summing node through R_1. The scale factor of this circuit is R_1 volts per ampere. The only conversion error in this circuit is I_{bias} which is summed algebraically with I_{IN}.

This basic circuit is useful for many applications other than current measurement. For example, it can be employed as a photocell amplifier.

The only design constraints that come into play are that scale factors must be chosen to minimize errors due to bias current, and since voltage gain and source impedance are often indeterminate (as with photocells) the amplifier must be compensated for unity-gain operation. Valuable techniques for bias current compensation have been covered by Widlar (5).

3.10 PHOTOCELL AMPLIFIERS

Amplifiers for photoconductive, photodiode and photovoltaic cells are shown in Figures 3.14, 3.15, and 3.16 respectively.

The voltages of all photogenerators have some dependence on both speed and linearity. It is obvious that the current through a photoconductive cell will not display strict proportionality to incident light if the cell terminal voltage is allowed to vary with cell conductance. Somewhat less obvious is the fact that photodiode leakage and photovoltaic cell internal losses are also functions of terminal voltage. The current-to-voltage converter neatly sidesteps gross linearity problems by fixing a constant terminal voltage, zero in the case of photovoltaic cells and a fixed bias voltage in the case of photoconductors or photodiodes.

Photodetector speed is optimized by operating into a fixed low load impedance. Currently available photovoltaic detectors show response times in the microsecond

range at zero load impedance and photoconductors, these speeds are slow but faster speeds can be obtained at low load resistances.

The feedback resistance, R_1, is dependent on cell sensitivity and should be chosen for either maximum dynamic range or for a desired scale factor. R_2 is elective: in the case of photovoltaic cells or of photodiodes, it should equal R_1; in the case of photoconductive cells, it should be chosen to minimize bias current error over the operating range.

3.11 PRECISION CURRENT SOURCE

A precision current source is shown in Figures 3.17 and 3.18. The configurations depicted sink or source conventional current, respectively.

Caution must be exercised in applying these circuits. The voltage compliance of the source extends from BV_{CER} of the external transistor to approximately 1 V more negative than V_{IN}. The compliance of the current sink is the same in the positive direction.

The impedance of these current generators is essentially infinite for small currents and the generator outputs are accurate so long as V_{IN} is much greater than V_{OS} and I_O is much greater than I_{bias}.

The source and sink illustrated in Figures 3.17 and 3.18 use a field-effect transistor to drive a bipolar output transistor. It is possible to use a Darlington connection in place of the FET-bipolar combination in cases where the output current is high and the base current of the Darlington input would not cause a significant error.

The amplifiers used must be compensated for unity-gain and additional compensation may be required depending on load reactance and external transistor parameters.

3.12 ADJUSTABLE VOLTAGE REFERENCES

Adjustable voltage reference circuits are shown in Figures 3.19 and 3.20. The two circuits have different areas of application. The basic difference between the two is that the circuit in Figure 3.19 illustrates a voltage source which provides a voltage greater than the reference diode while the circuit in Figure 3.20 represents a voltage source which provides a voltage lower than the reference diode. The figures show both positive and negative voltage sources.

High-precision extended-temperature applications of the circuit in Figure 3.19 require that the range of adjustment of V_{OUT} be restricted. When this is done, R_1 may be chosen to provide optimum zener current for a minimum zener temperature coefficient. Since I_Z is not a function of V^+, the reference temperature coefficient will be independent of V^+.

The circuit of Figure 3.20 is suited for high-precision extended-temperature service if V^+ is reasonably constant since I_Z is dependent of V^+. R_1, R_2, R_3, and R_4 are chosen to provide the proper I_Z for minimum T. C. and to minimize errors due to I_{bias}.

The circuits shown should both be compensated for unity-gain operation or, if large capacitive loads are expected, should be overcompensated. Output noise may be reduced in both circuits by bypassing the amplifier imput.

The circuits shown employ a single power supply; this requires that common-mode range be considered in choosing an amplifier for these applications. If the common-mode range requirements are in excess of the capability of the amplifier, two power supplies may be used. The LH101 operational amplifier may be used with a single power supply since the common-mode range is from V^+ to within approximately 2 volts of V^-.

3.13 THE RESET STABILIZED AMPLIFIER

The reset stabilized amplifier, a form of chopper-stabilized amplifier, is shown in Figure 3.21. The amplifier is operated closed-loop with a gain of one.

The connection shown is useful in eliminating errors due to offset voltage and bias current. The output of this circuit is a pulse whose amplitude is equal to V_{IN}. Operation may be understood by considering the two conditions corresponding to the position of S_1. When S_1 is in position 2, the amplifier is connected in the unity-gain connection and the voltage at the output will be equal to the sum of the input offset voltage and the drop across R_2 due to input bias current. The voltage at the inverting input will be equal to the input offset voltage. Capacitor C_1 will charge to the sum of the input offset voltage and V_{IN} through R_1. When C_1 is charged, no current flows through the source resistance and R_1, so there is no error due to the input resistance.

S_1 is then changed to position 1. The voltage stored on C_1 is inserted between the output and inverting input of the amplifier and the output of the amplifier changes by V_{IN} to maintain the amplifier input at the input offset voltage. The output then changes from $(V_{OS} + I_{bias}R_2)$ to $V_{IN} + (V_{OS} + I_{bias}R_2)$ as S_1 is switched from position 2 to position 1. Amplifier bias current is supplied through R_2 from the output of the amplifier when S_1 is in position 2 or from C_2 when S_1 is in position 1. Resistor R_3 serves to reduce the offset at the amplifier output if the amplifier must have maximum linear range or if it is desired to dc couple the amplifier.

An additional advantage provided by this connection is that the input resistance approaches infinity as the capacitor C_1 approaches full charge, eliminating errors due to loading of the source resistance. The time spent in position 2 should be sufficiently long with respect to the changing time of C_1 to permit maximum accuracy.

The amplifier used must be compensated for unity-gain operation and it may be necessary to overcompensate because of the phase shift across R_2 due to C_1 and the amplifier input capacity. Since this connection is usually used at very low switching speeds, slew rate is not normally a practical consideration and overcompensation does not reduce accuracy.

3.14 ANALOG MULTIPLIER

A simple analog multiplier is shown in Figure 3.22. This circuit circumvents many of the problems associated with the log-antilog circuit and provides three-quadrant analog multiplication which is relatively temperature insensitive and which is not subject to the bias-current errors which plague most multipliers.

The circuit operation may be understood by considering A_2 as a controlled-gain amplifier, amplifying V_2, with the gain dependent on the ratio of the resistance of

PC_2 to R_5 and by considering A_1 as a control amplifier which establishes the resistance of PC_2 as a function of V_1. In this way it is seen that V_{OUT} is a function of both V_1 and V_2.

A_1, the control amplifier, provides drive for the lamp, L_1. When an input voltage, V_1, is present, L_1 is driven by A_1 until the current to the summing junction from the negative supply through PC_1 is equal to the current to the summing junction from V_1 through R_1. Since the negative supply voltage is fixed, this forces the resistance of PC_1 to a value proportional to R_1 and to the ratio of V_1 to V^-. L_1 also illuminates PC_2 and, if the photoconductors are matched, causes PC_2 to have a resistance equal to PC_1.

A_2, the controlled gain amplifier, acts as an inverting amplifier with a gain which is equal to the ratio of the resistance of PC_2 to R_5. If R_5 is chosen equal to the product of R_1 and V^-, then V_{OUT} becomes simply the product of V_1 and V_2. Resistor R_5 may be scaled in powers of ten to provide any required output scale factor.

PC_1 and PC_2 should be matched for best tracking over temperature since the temperature coefficient of resistance is related to the resistance match of cells with the same geometry. Small mismatches may be compensated by varying the value of R_5 as a scale-factor adjustment. The photoconductive cells should receive equal illumination from L_1; this can be accomplished by mounting the cells in holes in an aluminum block and placing the lamp midway between them. This mounting method provides controlled spacing and also provides a thermal bridge between the two cells to reduce differences in cell temperature. This technique may be extended to use FETs or other devices to meet special resistance or environment requirements.

The circuit as shown provides an inverting output whose magnitude is equal to one-tenth the product of the two analog inputs. Input V_1 is restricted to positive values, but V_2 may assume both positive and negative values. This circuit is restricted to low-frequency operation by the lamp time constant.

Resistors R_2 and R_4 are chosen to minimize errors due to input offset current as previously mentioned for the photocell amplifier. Resistor R_3 is included to reduce the in-rush current when L_1 starts to turn on.

3.15 FULL-WAVE RECTIFIER AND AVERAGING FILTER

The circuit shown in Figure 3.23 is the heart of an average-reading, rms-calibrated ac voltmeter. As shown, the circuit is a rectifier and averaging filter. If C_2 is deleted, the averaging function is removed and the circuit becomes a precision fullwave rectifier; deletion of C_1 provides an absolute value generator.

The circuit operation may be understood by following the signal path first for negative, then for positive inputs. For negative signals, the output of amplifier A_1 is clamped to +0.7 V by D_1 and disconnected from the summing point of A_2 by D_2. A_2 then functions as a simple unity-gain inverter with input resistor, R_1, and feedback resistor, R_2, giving a positive going output.

For positive inputs, A_1 operates as a normal amplifier connected to the A_2 summing point through resistor, R_5. Amplifier A_1 then acts as a simple unity-gain inverter

with input resistor, R_3, and feedback resistor, R_5. The gain accuracy of A_1 is not affected by D2 since it is inside the feedback loop. Positive current enters the A_2 summing point through resistor R_1, and negative current is drawn from the A_2 summing point through resistor R_5. Since the voltages across R_1 and R_5 are equal and opposite, and R_5 is one-half the value of R_1, the net input current at the A_2 summing point is equal to and opposite from the current through R_1, and amplifier A_2 operates as a summing inverter with unity gain, again giving a positive output.

The circuit becomes an averaging filter when C_2 is connected across R_2. Operation of A_2 is then similar to the simple low-pass filter previously described. The time constant R_2C_2 should be chosen so that it is much larger than the maximum period of the input voltage which is to be averaged.

Capacitor C_1 may be deleted if the circuit is to be used as an absolute-value generator. When this is done, the circuit output will be the positive absolute value of the input voltage.

The amplifiers chosen must be compensated for unity-gain operation and R_6 and R_7 must be chosen to minimize output errors due to input offset current.

3.16 SINE-WAVE OSCILLATOR

An amplitude-stabilized sine-wave oscillator is shown in Figure 3.24. This circuit provides high-purity sine-wave output down to low frequencies with minimum circuit complexity. An important advantage of this circuit is that the traditional tungsten-filament-lamp amplitude regulator is eliminated along with its time constant and linearity problems.

In addition, the reliability problems associated with a lamp are eliminated.

A Wien-Bridge oscillator takes advantage of the fact that the phase of the voltage across the parallel branch of a series and a parallel RC network connected in series, is the same as the phase of the applied voltage across the two networks at one particular frequency and that the phase lags with increasing frequency and leads with decreasing frequency. When this network--the Wien Bridge--is used as a positive feedback element around an amplifier, oscillation occurs at the frequency at which the phase shift is zero. Additional negative feedback is provided to set the loop gain to unity at the oscillation frequency, to stabilize the frequency of oscillation, and to reduce harmonic distortion.

The circuit presented here differs from the classic form only in its negative feedback stabilization scheme in the circuit; negative peaks in excess of -8.25 V cause D_1 and D_2 to conduct, charging C_4. The charge stored in C_4 provides bias to Q_1, which determines the amplifier gain. C_3 is a low frequency roll-off capacitor in the feedback network and prevents offset voltage and offset current errors from being multiplied by amplifier gain.

Distortion is determined by the amplifier open-loop gain and by the response time of the negative feedback loop filter, R_5 and C_4. A trade-off is necessary in determining amplitude stabilization time constant and oscillator distortion. Resistor R_4 is chosen to adjust the negative feedback loop so that the FET is operated at a small negative gate bias. The circuit shown provides optimum values for a general-

purpose oscillator.

3.17 TRIANGLE-WAVE GENERATOR

A constant-amplitude triangular-wave generator is shown in Figure 3.25. This circuit provides a variable-frequency triangular wave whose amplitude is independent of frequency.

The generator contains an integrator which functions as a ramp generator and a threshold detector with hysterisis which is the reset circuit. The integrator has been described earlier in this chapter. The threshold detector is similar to a Schmit Trigger in that it is a latch circuit with a large dead zone. This function is implemented by using positive feedback around an operational amplifier. When the amplifier output is in either the positive or negative saturated state, the positive feedback network provides a voltage at the non-inverting input which is determined by the attenuation of the feedback loop and the saturation voltage of the amplifier. To cause the amplifier to change states, the voltage at the input of the amplifier must change polarity by an amount larger than the amplifier input offset voltage.

When this occurs, the amplifier saturates in the opposite direction and remains in that state until the voltage at its input again reverses. The complete operation of the circuit may be grasped by examining its operation with the output of the threshold detector in the positive state. The detector positive saturation voltage is applied to the integrator summing junction through the combination R_3 and R_4 causing a current I^+ to flow. The integrator then generates a negative-going ramp with a rate of I^+/C_1 volts per second until its output equals the negative trip point of the threshold detector. The threshold detector then changes to the negative output state and supplies a negative current, I^-, at the integrator summing point. The integrator now generates a positive-going ramp with a rate of I^-/C_1 volts per second until its output equals the positive trip point of the threshold detector where the detector again changes output state and the cycle repeats.

The triangular-wave frequency is determined by R_3, R_4 and C_1 and the positive and negative saturation voltages of the amplifier A_1. The amplitude is determined by the ratio of R_5 to the combination of R_1 and R_2 and the threshold detector saturation voltages. The positive and negative ramp rates are equal, and positive and negative peaks are equal if the detector has equal positive and negative saturation voltages. The output waveform may be offset with respect to ground if the inverting input of the threshold detector, A_1, is offset with respect to ground.

The generator may be made independent of temperature and supply voltage if the detector is clamped with matched zener diodes as shown in Figure 3.26.

The integrator should be compensated for unity-gain and the detector may be compensated if power supply impedance causes oscillation during its transition time. The current into the integrator should be large with respect to I_{bias} for maximum symmetry, and offset voltage should be small with respect to V_{OUT} peak.

3.18 TRACKING REGULATED POWER SUPPLY

A tracking regulated power supply is shown in Figure 3.27. This supply is very suitable for powering an operational amplifier system since positive and negative

voltage track, eliminating common-mode signals originating in the supply voltage. In addition, only one voltage reference and a minimum number of passive components are required.

The power supply's method of operation may be understood by first considering the positive regulator. The positive regulator compares the voltage at the wiper of R_4 to the voltage reference D_2. The difference between these two voltages is the input voltage for the amplifier and since R_3, R_4, and R_5 form a negative feedback loop, the amplifier output voltage changes in such a way as to minimize this difference. The voltage reference current is supplied from the amplifier output to increase the power supply line regulation. This allows the regulator to operate from supplies with large ripple voltages. Regulating the reference current in this way requires a separate source of current for supply start-up. Resistor R_1 and diode D_1 provide the start-up current. Diode D_1 decouples the reference string from the amplifier output during start-up and R_1 supplies the start-up current from the unregulated positive supply. After start-up, the low amplifier output impedance reduces reference current variations due to the current through R_1.

The negative regulator is simply a unity-gain inverter with input resistor R_6 and feedback resistor R_7.

The amplifiers must be compensated for unity-gain operation.

The power supply may be modulated by injecting current into the wiper of R_4. In this case, the output voltage variations will be equal and opposite at the positive and negative outputs. The power supply voltage may be controlled by replacing D_1, D_2, R_1 and R_2 with a variable voltage reference.

3.19 PROGRAMMABLE BENCH POWER SUPPLY

The complete power supply shown in Figure 3.28 is a programmable positive and negative power supply. The regulator section of the supply comprises two voltage followers whose input is provided by the voltage drop across a reference resistor of a precision current source.

Programming sensitivity of the positive and negative supply is 1 V per 1000 Ω of resistors R_6 and R_{12}, respectively. The output voltage of the positive regulator may be varied from approximately +2 V to +38 V with respect to ground and the negative regulator output voltage may be varied from -38 V to 0 V with respect to ground. Since LH101 amplifiers are used, the supplies are inherently short-circuit proof. This current limiting feature also serves to protect a test circuit if this supply is used in integrated-circuit testing.

Internally compensated amplifiers may be used in this application if the expected capacitive loading is small. If large capacitive loads are expected, an externally compensated amplifier should be used and the amplifier should be overcompensated for additional stability. Power supply noise may be reduced by bypassing the amplifier inputs to ground with capacitors in the 0.1 to 1.0 μF range.

3.20 CONCLUSIONS

The foregoing circuits are illustrative of the versatility of the integrated operational amplifier and provide a guide to a number of useful applications. The pre-

cautions mentioned cover the more common pitfalls encountered in amplifier use.

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6. Widlar, R.J., "A Fast Integrated Voltage Follower With Low Input Current," Microelectronics, Vol. 1 No. 7, June 1968.

FIGURES

Figure 3.1. Inverting Amplifier. Output voltage V_{OUT} is equal to $-(R_2/R_1)V_{in}$. For minimum error due to the input bias current, $R_3 = R_1//R_2$.

Figure 3.2. Non-inverting amplifier. Output voltage V_{OUT} is equal to $[(R_1 + R_2) / R_1] V_{IN}$. For minimum error due to input bias current, $R_1//R_2 = R_{SOURCE}$.

Figure 3.3. Unity-gain buffer. Output voltage V_{OUT} is equal to V_{IN}. For minimum error due to input bias current, $R_1 = R_{SOURCE}$.

Figure 3.4. Summing amplifier. Output voltage V_{OUT} is equal to $-R_4[(V_1/R_1) + (V_2/R_2) + (V_3/R_3)]$.

Figure 3.5. Difference Amplifier. Output voltage V_{OUT} is equal to $[(R_1 + R_2) / (R_3 + R_4)][(R_4/R_1) V_2] - (R_2/R_1)V_1$. For $R_1 = R_3$ and $R_2 = R_4$, $V_{OUT} = (R_2/R_1) (V_2-V_1)$. For minimum error due to input bias current, $R_1//R_2 = R_3//R_4$.

Figure 3.6. Differentiator. Output voltage V_{OUT} is equal to $-R_1C_2 [d/dt(V_{IN})]$. For minimum error due to input bias current, $R_1 = R_2$.

Figure 3.7. Practical Differentiator. Corner frequency $f_c = 1/2\pi R_2C_1$; $f_h = 1/2$ $f_h = 1/2\pi R_2C_2$; $f_c \ll f_h \ll f_{unity\text{-}gain}$.

Figure 3.8. Differentiator frequency response.

Figure 3.9. Integrator. Output voltage $V_{OUT} = -(1/R_1C_1)\int_{t1}^{t2} V_{IN}\, dt$; $f_c = 1/2\pi R_1C_1$. For minimum offset error due to input bias current, $R_1 = R_2$.

Figure 3.10. Amplitude-frequency plot for the integrator circuit.

Figure 3.11. Simple low-pass filter: $f_e = 1/2\pi R_1C_1$; $f_c = 1/2\pi R_3C_1$; $A_e = R_3/R_1$.

Figure 3.12. Gain-frequency plot for low-pass filter.

Figure 3.13. Current-to-voltage converter. Output voltage V_{OUT} is equal to $I_{IN}R_1$.

Figure 3.14. Photoconductive-cell amplifier.

Figure 3.15. Photodiode amplifier. Output voltage V_{OUT} is equal to $R_1 I_D$.

Figure 3.16. Photovoltaic-cell amplifier. Output voltage is equal to $I_{CELL} R_1$.

Figure 3.17. Precision current sink: $I_o = V_{IN}/R_1$; $V_{IN} \geq 0$ V.

Figure 3.18. Precision current source: $I_o = V_{IN}/R_1$; $V_{IN} \leq 0$ V.

Figure 3.19. Voltage references: (A) positive, (B) negative. Voltage source provides a voltage greater than the reference-diode voltage.

Figure 3.20. Voltage references: (A) positive, (B) negative. Voltage source provides a voltage less than the reference-diode voltage.

Figure 3.21. Reset stabilized amplifier.

Figure 3.22. Analog multiplier. Output voltage V_{OUT} is equal to $V_1 V_2/10$; $V_1 \geq 0$ V; $R_5 = R_1 (V^-/10)$.

Figure 3.23. Full-wave rectifier and averaging filter.

Figure 3.24. Wien-Bridge sine-wave oscillator.

Figure 3.25. Constant-amplitude triangular-wave generator.

Figure 3.26. Threshold detector with regulated output.

Figure 3.27. Tracking power supply. Output voltage V_{OUT} is variable from ± 5 V to ± 35 V. Negative output tracks positive output to within the ratio of R_6 to R_7.

Figure 3.28. Programmable positive and negative power supply for testing integrated circuits.

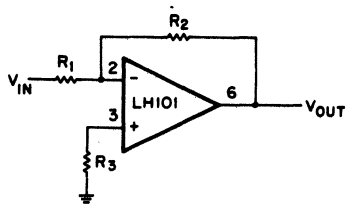


Figure 3.1. Inverting Amplifier. Output voltage V_{OUT} is equal to $-(R_2/R_1)$ V_{in}. For minimum error due to the input bias current, $R_3 = R_1 /\!/ R_2$.

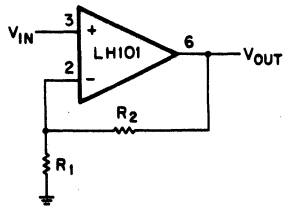


Figure 3.2. Non-inverting amplifier. Output voltage V_{OUT} is equal to $[(R_1 + R_2) / R_1]V_{IN}$. For minimum error due to input bias current, $R_1 /\!/ R_2 = R_{SOURCE}$.

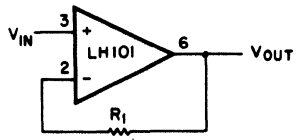


Figure 3.3. Unity-gain buffer. Output voltage V_{OUT} is equal to V_{IN}. For minimum error due to input bias current, $R_1 = R_{SOURCE}$.

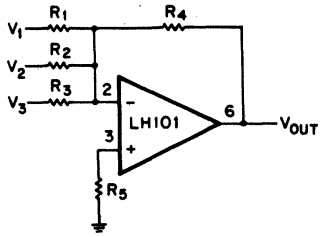


Figure 3.4. Summing amplifier. Output voltage V_{OUT} is equal to $-R_4[(V_1/R_1) + (V_2/R_2) + (V_3/R_3)]$.

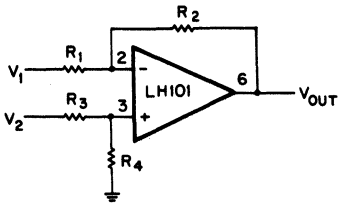


Figure 3.5. Difference Amplifier. Output voltage V_{OUT} is equal to $[(R_1 + R_2) / (R_3 + R_4)][(R_4/R_1) V_2] - (R_2/R_1)V_1$. For $R_1 = R_3$ and $R_2 = R_4$, $V_{OUT} = (R_2/R_1)(V_2-V_1)$. For minimum error due to input bias current, $R_1 /\!/ R_2 = R_3 /\!/ R_4$.

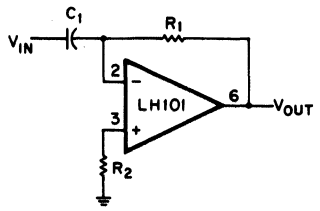


Figure 3.6. Differentiator. Output voltage V_{OUT} is equal to $-R_1C_2[d/dt(V_{IN})]$. For minimum error due to input bias current, $R_1 = R_2$.

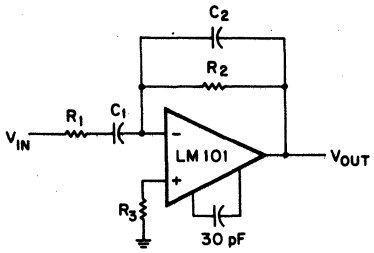


Figure 3.7. Practical Differentiator. Corner frequency $f_c = 1/2\pi R_2C_1$; $f_h = 1/2\ f_h = 1/2\pi R_2C_2$; $f_c \ll f_h \ll f_{unity\text{-}gain}$.

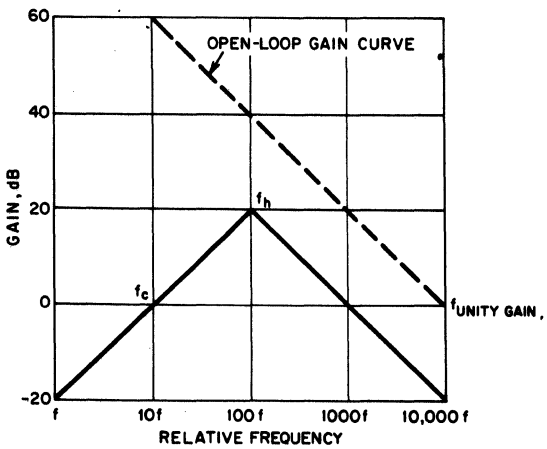


Figure 3.8. Differentiator frequency response.

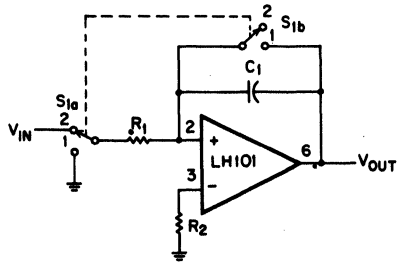


Figure 3.9. Integrator. Output voltage $V_{OUT} = -(1/R_1C_1)\int_{t1}^{t2} V_{IN}\,dt$; $f_c = 1/2\pi R_1C_1$. For minimum offset error due to input bias current, $R_1 = R_2$.

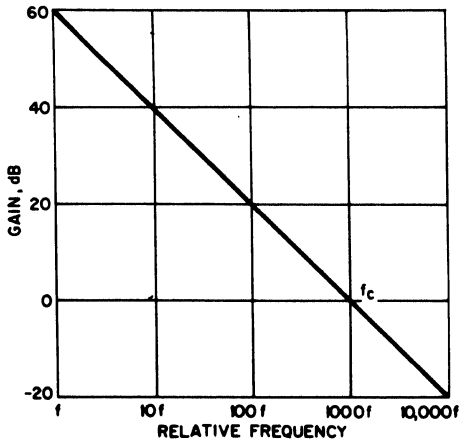


Figure 3.10. Amplitude-frequency plot for the integrator circuit.

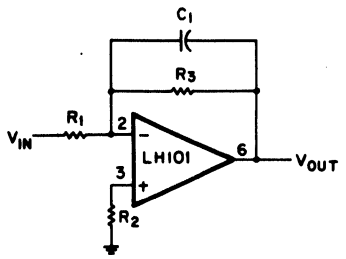


Figure 3.11. Simple low-pass filter: $f_e = 1/2\pi R_1C_1$; $f_c = 1/2\pi R_3C_1$; $Ae = R3/R_1$.

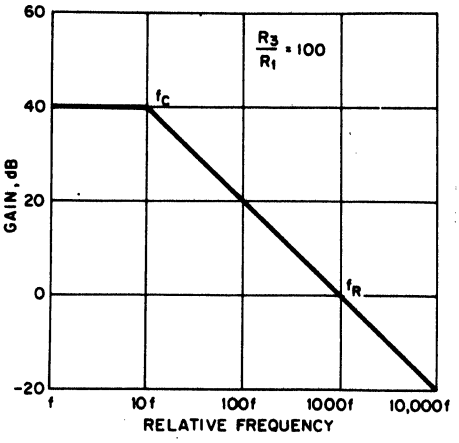


Figure 3.12. Gain-frequency plot for low-pass filter.

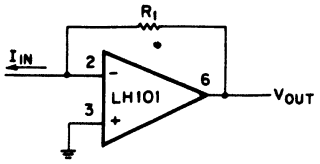


Figure 3.13. Current-to-voltage converter. Output voltage V_{OUT} is equal to $I_{IN}R_1$.

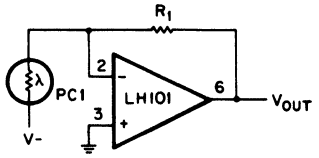


Figure 3.14. Photoconductive-cell amplifier.

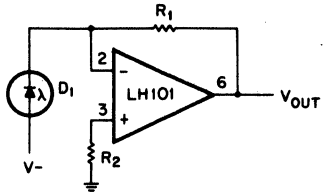


Figure 3.15. Photodiode amplifier. Output voltage V_{OUT} is equal to R_1I_D.

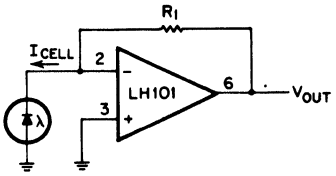


Figure 3.16. Photovoltaic-cell amplifier. Output voltage is equal to $I_{CELL}R_1$.

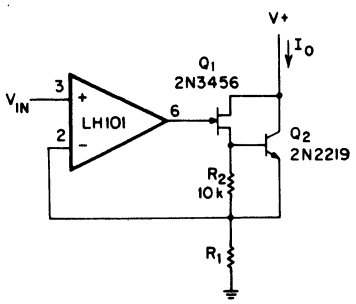


Figure 3.17. Precision current sink: $I_O = V_{IN}/R_1$; $V_{IN} \geq 0$ V.

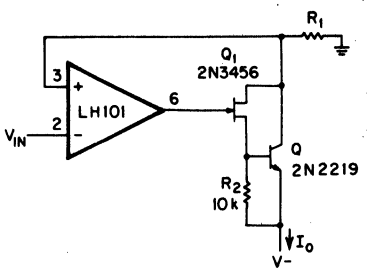
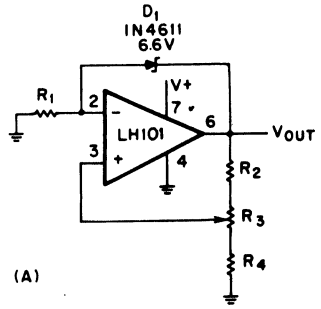


Figure 3.18. Precision current source: $I_O = V_{IN}/R_1$; $V_{IN} \leq 0$ V.



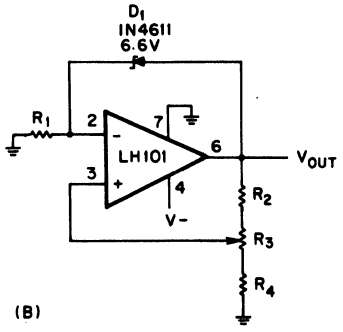


Figure 3.19. Voltage references: (A) positive, (B) negative. Voltage source provides a voltage greater than the reference-diode voltage.

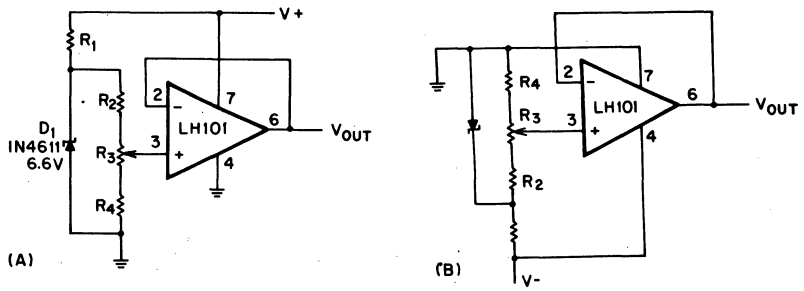


Figure 3.20. Voltage references: (A) positive, (B) negative. Voltage source provides a voltage less than the reference-diode voltage.

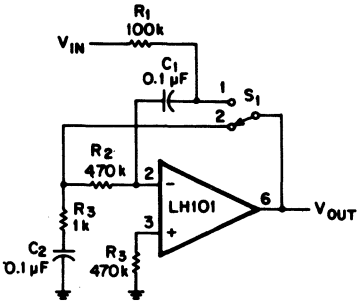


Figure 3.21. Reset stabilized amplifier.

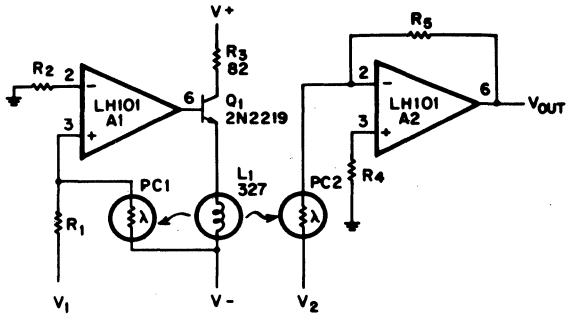


Figure 3.22. Analog multiplier. Output voltage V_{OUT} is equal to $V_1V_2/10$; $V_1 \geq 0$ V; $R_5 = R_1(V^-/10)$.

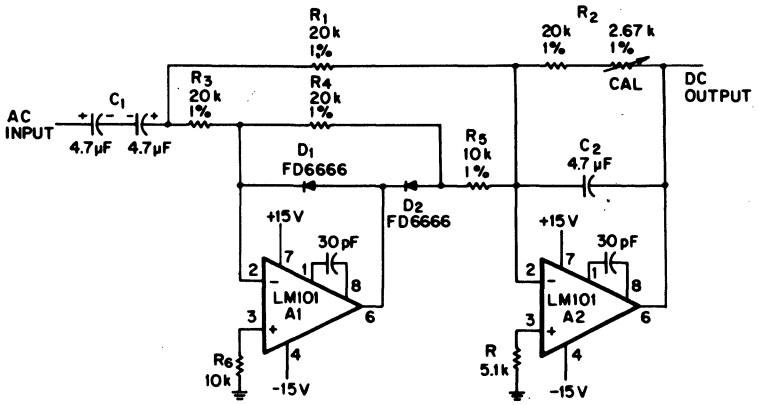


Figure 3.23. Full-wave rectifier and averaging filter.

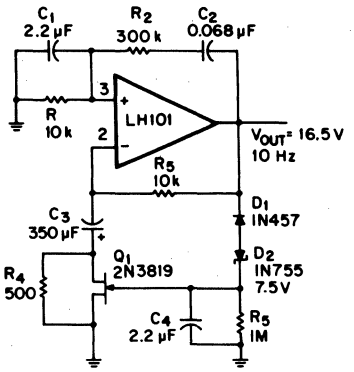


Figure 3.24. Wien-Bridge sine-wave oscillator.

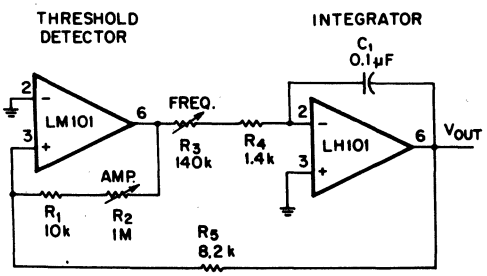


Figure 3.25. Constant-amplitude triangular-wave generator.

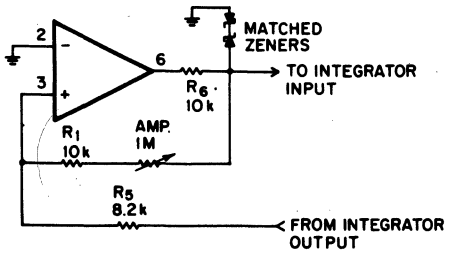


Figure 3.26. Threshold detector with regulated output.

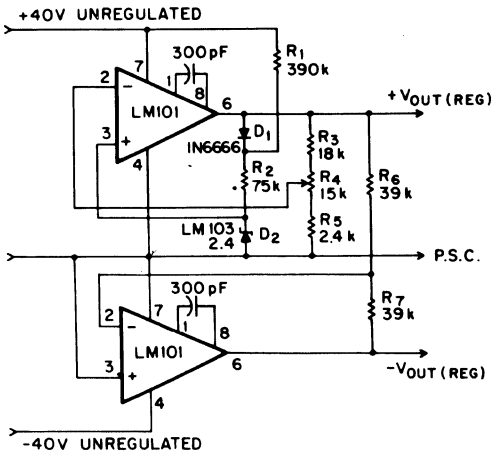


Figure 3.27. Tracking power supply. Output voltage V_{OUT} is variable from ±5 V to ±35 V. Negative output tracks positive output to within the ratio of R_6 to R_7.

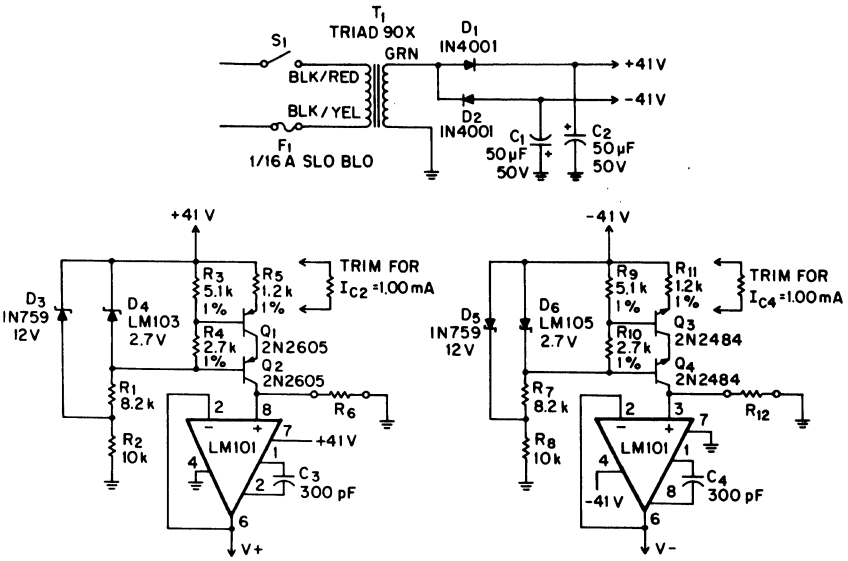


Figure 3.28. Programmable positive and negative power supply for testing integrated circuits.

4
Applications For Fully Compensated Operational Amplifiers

by Michael English
Fairchild Semiconductor

Fully compensated operational-amplifier ICs, available since 1968, have changed some of the design rules for IC users. The following paragraphs cover some of the more important considerations that come into play when incorporating these ICs into equipment.

4.1 VOLTAGE REGULATOR

The voltage follower is frequently used as a buffer amplifier to reduce voltage error caused by source loading and to isolate high impedance sources from following circuitry. A circuit diagram for the follower is shown in Figure 4.1. The gain of this circuit is essentially unity. The output duplicates, or follows, the input voltage, hence the name voltage follower.

The voltage follower is a "worst case" for stable operation as maximum feedback is applied. Normally, external components are required to reduce the gain below unity at high frequencies to prevent oscillation. A fully compensated op-amp IC, of course, does not require external stabilizing components as it has an internal monolithic compensation network.

Voltage follower are also subject to "latch-up." Latch-up may occur if the input common-mode voltage limit is exceeded. If the input transistor at the inverting input saturates, then the input to this transistor is fed directly to its collector circuit through the collector-base junction. Thus, the inverting input becomes non-inverting if the common mode limit is exceeded. This results in positive feedback holding the IC in saturation.

The input stage of a fully compensated op-amp IC should be designed to prevent latch-up. If it is, no external protective circuitry will be required. The μA741, for example, couples this protection with a larger common-mode range than most monolithic operational amplifiers and is therefore capable of larger output voltage excursions. The worst case common-mode range of the μA741 is typically $\pm$ 12 V, thus allowing voltage-follower output swings up to $\pm$ 12 V.

The accuracy of a voltage follower is determined by the open-loop gain of the operational amplifier and by its common-mode rejection ratio.

The expression for the accuracy is:

$$\frac{e_{OUT}}{e_{IN}} = \frac{1 + \frac{1}{CMRR}}{1 + \frac{1}{A}} \qquad (4.1)$$

where the common-mode rejection ratio in dB is given by $CMRR_{dB} = 20 \log_{10} CMRR$

Using typical figures from the μA741 data sheet, A_{OL} = 75,000 CMRR = 90 dB; the dc accuracy of the voltage follower turns out to be better than .003%.

4.2 INTEGRATOR

The integrator, shown in Figure 4.2, provides an output that is proportional to the time integral of the input signal. The gain function for the integrator is given by:

$$e_o = -\frac{1}{R_1C_1}\int e_{IN}\, dt . \tag{4.2}$$

R_1 and C_1 are labeled in the figure. As an example, consider the response of the integrator to a symmetrical square-wave input signal with an average value of zero volts. If the input has a peak amplitude of A volts then the peak-to-peak output can be calculated by integrating over one-half the input period giving:

$$\left| e_o\ (p\text{-}p) \right| = \frac{1}{R_1C_1}\int_o^{T/2} A\ dt = \frac{A}{R_1C_1}\left(\frac{T}{2}\right). \tag{4.3}$$

The waveshape will be triangular and will correspond to the integral of the square wave. For the component values shown in Figure 4.2 and assuming A = 5 V and T = 1 ms, equation 4.2 yields:

$$e_{o\ (p\text{-}p)} = \left(\frac{5}{10^{-3}}\right)\left(\frac{10^{-3}}{2}\right) = 2.5\ V_{\ (p\text{-}p)}.$$

Resistor R_2 is included to provide dc stabilization for the integrator. It limits the low-frequency gain of the amplifier and minimizes drift. The minimum frequency at which the circuit will perform as an integrator is given by:

$$f = \frac{1}{2\ R_2C_1}\ \text{Hz} . \tag{4.4}$$

For best linearity, the frequency of the input signal should be at least 10 times the frequency calculated using equation 4.2. The linearity of the circuit illustrated is better than 1% with an input frequency of 1 kHz.

Although it is not immediately obvious, the integrator, if it is to operate reliably, requires both large common-mode and differential-mode input voltage ranges. There are several ways that the input voltage limits may be inadvertently exceeded. The most obvious is that transients occurring at the output of the amplifier can be coupled back to the input by the integrating capacitor, C_1. Thus, either common mode or differential voltage limits may be exceeded.

Another less obvious problem can occur when the amplifier is driven from fast rising or falling input signals, such as square waves. Because the output of the amplifier cannot respond to an input instantaneously during the short interval before the output reacts, the summing point at pin 2 of the amplifier may not be held at ground potential. If the input signal change is large enough, the voltage at the summing point can exceed the safe limits for the amplifier. Fully compensated op-amp ICs with large differential input voltage ranges obviously offer greater protection against this occurring. The range for the μA741 is ±30 V.

4.3 DIFFERENTIATOR

The differentiator circuit of Figure 4.3 provides an output proportional to the derivative of the input signal. The gain function of the differentiator is given by:

$$e_o = -R_2C_1\frac{de_1}{dt} \tag{4.5}$$

As the differentiator performs the reverse of the integrator function, a triangular input will produce a square-wave output. For a 2.5 V peak-to-peak triangle wave with a period of 1 ms we have, for the circuit illustrated:

$$\frac{de}{dt} = \frac{2.5}{0.5} = 5 \text{ V/ms}$$

$$e_o = - (10/K) \ (0.1) = 5 \text{ V/ms}$$

$$= 5 \text{ V}_{(p-p)}$$

The resistor R_1 is needed to limit the high-frequency gain of the differentiator. This makes the circuit less susceptible to high-frequency noise and assures dynamic stability. The corner frequency at which gain limiting comes into effect is given by:

$$f = \frac{1}{2 R_1 C_1} . \tag{4.6}$$

This frequency should be at least 10 times the highest input frequency for accurate operation. A maximum value for the corner frequency is determined by stability criteria. In general, it should be no larger than the geometric mean between $\frac{1}{2} R_2 C_1$ and the gain-bandwidth product of the operational amplifier. Since the μA471 has a gain-bandwidth product of approximately 1 MHz, its limit for f is given by:

$$f < \sqrt{\frac{1 \times 10^6}{2 R_2 C_1}} . \tag{4.7}$$

The differentiator is subject to damage from fast-rising input signals as is the integrator and, as has been discussed, the circuit is also susceptible to high-frequency instability. The wide range of input voltages and the built-in frequency compensation of the μA471 are particularly important when the amplifier is used as a differentiator.

4.5 VOLTAGE-REGULATOR REFERENCE AMPLIFIER

Operational amplifiers are frequently used as reference amplifiers in voltage-regulated power supplies. A typical circuit with variable output voltage, is shown in Figure 4.4. The purpose of the amplifier is to isolate the voltage reference, a zener diode in Figure 4.4; from changes in loading at the supply output. This results in lower supply output impedance and hence improved load regulation. Also, because of the high gain at the μA741, the voltage applied to the inverting input of the amplifier from the output voltage divider is always maintained within a few millivolts of the reference.

Thus, the output voltage may be varied by changing the divider. The 800-kilohm input impedance of the μA741 keeps loading of the reference zener to a minimum. The output impedance of the circuit shown is less than 0.1 Ω and the line regulation is approximately 0.4% for input voltages varying from 20 to 30 V.

4.6 HIGH-VOLTAGE REGULATED POWER SUPPLY

The μA741, with proper biasing, can be used to control regulated power supply voltages many times its normal operating voltage. Figure 4.5 shows a 100-V regulated power supply using the μA741 as the control amplifier.

Zener diodes D_1 through D_3 supply proper operating voltages to the IC. The diodes

reference the amplifier voltages to the power supply output so the bias levels can follow the output voltage over a wide range of adjustment. D_1 keeps the positive supply terminal of the IC about 6 V greater than the regulator output. D_2 holds the inverting input about 10 V below the output voltage, while D_3 maintains a 30 V drop across the amplifier's supply terminals. One of the SE7040 transistors, biased by a zener resistor network, acts as a current source, supplying operating current to the amplifier and part of the biasing network.

The regulator output is fed back to the IC amplifier through a voltage divider. The division ratio is obtained by first selecting the desired output voltage and calculating the division ratio required to make the divider output 10 V less (D_2 is a 10-V zener diode) than the output from the regulator. For the circuit shown, the desired output is 100 V and D_2 is a 10-V diode giving:

$$e_{OUT}\left(\frac{R}{R_{total}}\right) = e_{OUT} - V_{D2}$$

$$100\left(\frac{R}{R_{total}}\right) = 100 - 10$$

$$\left(\frac{R}{R_{total}}\right) = 0.9 = \text{division ratio}$$

The regulator is short-circuit-protected by the 2N944 transistor and the 5-Ω resistor in series with the output. As the output current increases, the voltage drop across the 5-Ω resistor increases, turning on the 2N4944. The transistor thus shunts base current away from the SE7040 pass transistor. If output current is further increased, the voltage output drops rapidly to zero. With a 5-Ω resistor, the output current limits at approximately 100 mA. Proportionally, larger and smaller resistor values give other current limits, such as 2.5 Ω for a 200 mA limit. It should be remembered that the pass transistor must be capable of dissipating the power generated by the maximum unregulated input voltage and the short circuit current, as it is essentially connected across the input terminals under short circuit conditions.

The circuit shown provides line and load regulation of approximately 0.06% for input voltages ranging from 120 to 170 V and an output voltage of 100 V at 0 to 100 mA. Higher output currents are possible by using a higher power transistor in place of the SE7040 pass transistor or by excluding the possibility of output short circuits.

4.7 CLIPPING AMPLIFIER

Occasionally, it is desirable to limit the output swing of an amplifier to within specific limits. This can be done by adding nonlinear elements to the feedback network as shown in Figure 4.6.

The zener diodes quickly reduce the gain of the amplifier if the output tries to exceed the limits set by the zener voltages. When the zeners are not conducting, the gain is determined by the feedback resistors R_1 and R_2.

It is often overlooked that an amplifier used as a clipper must be frequency compensated for a gain of unity. This is because the gain of the circuit passes through unity as the zeners begin their clipping action. The μA741 poses no problems

in this respect as it is internally compensated for unity gain.

4.8 COMPARATOR

Many control functions require that a comparison be made between two voltages and that an output be supplied indicating which of the two is greatest. The μA741 can be used as a comparator in many applications where high speed is not a prerequisite. It cannot complete with comparators designed for high-speed operation, such as μA710 types, as the internal compensation network limits the response time.

A typical comparator circuit is shown in Figure 4.7. The zener bonding voltage may be selected to be compatible with high level DTL micrologic or normal CCSL logic levels, or with MOS device thresholds, or the amplifier can be used open loop.

FIGURES

Figure 4.1. Unity-gain voltage-follower arrangement.

Figure 4.2. Integrator circuit provides an output which is proportional to the time integral of the input signal.

Figure 4.3. Differentiator circuit provides an output which is proportional to the derivative of the input signal.

Figure 4.4. Variable-voltage regulated power supply.

Figure 4.5. High-voltage regulated power supply.

Figure 4.6. Clipping amplifier circuit.

Figure 4.7. Comparator circuit.

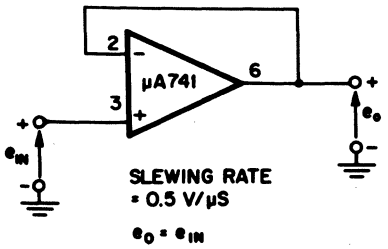


Figure 4.1. Unity-gain voltage-follower arrangement.

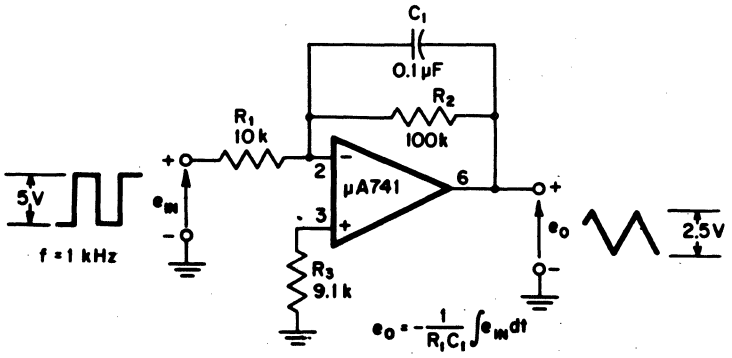


Figure 4.2. Integrator circuit provides an output which is proportional to the time integral of the input signal.

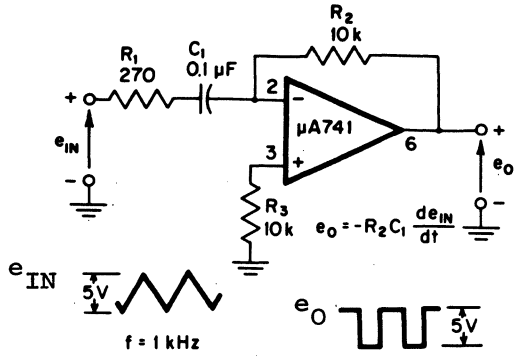


Figure 4.3. Differentiator circuit provides an output which is proporsional to the derivative of the input signal.

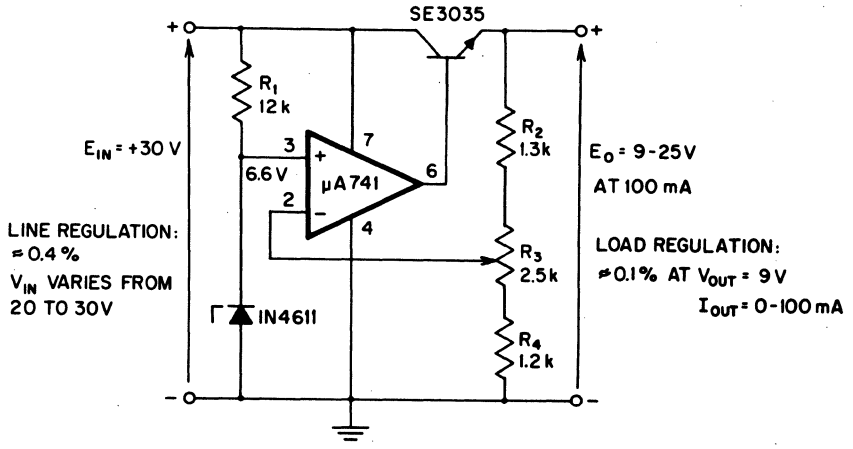


Figure 4.4. Variable-voltage regulated power supply.

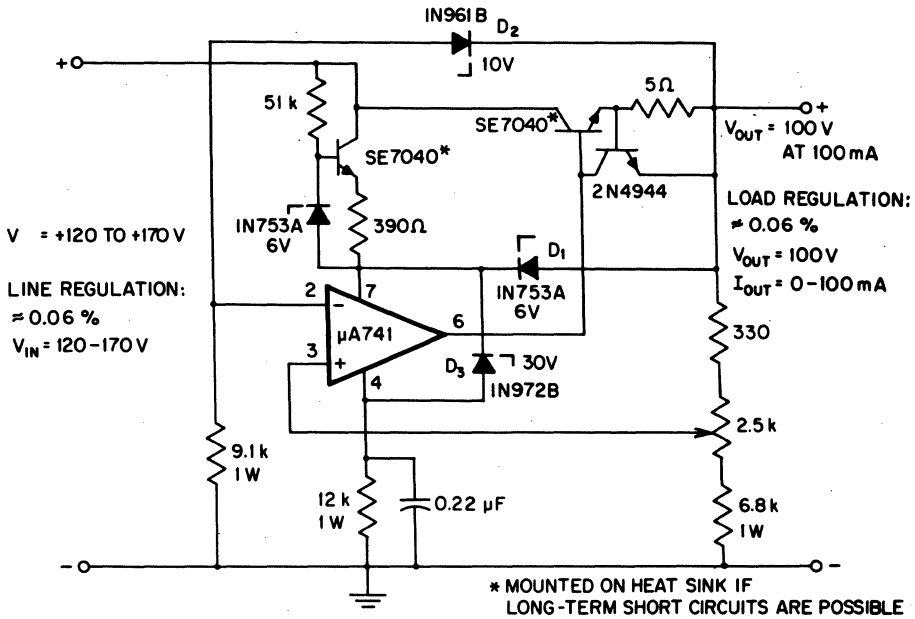


Figure 4.5. High-voltage regulated power supply.

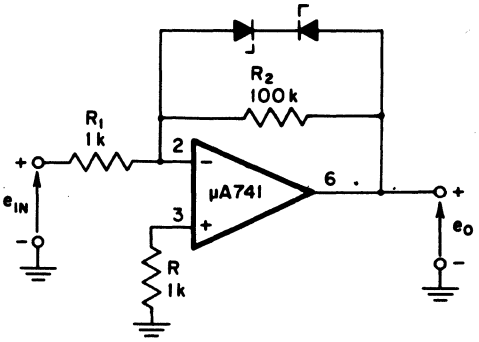


Figure 4.6. Clipping amplifier circuit.

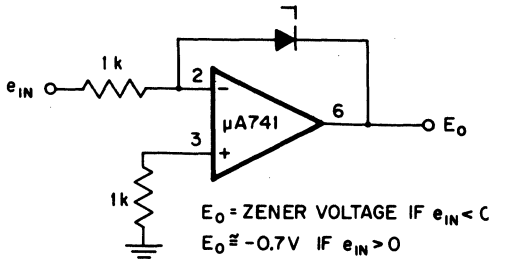


Figure 4.7. Comparator circuit.

5

Understanding Fully Compensated IC Operational Amplifiers

by Harry Gill
Raytheon Semiconductor

The present generation of monolithic operational amplifiers includes fully frequency compensated ICs which are short-circuit proof, may be easily balanced, and are not prone to go into oscillation when used with capacitive loads.

The design concept on which today's fully compensated op-amp ICs is based was first applied in 1967 in National Semiconductor's LM101. The key to this approach is the employment of current sources as collector loads (See Figure 5.1). Previously, in the first-generation 709-type monolithic operational amplifiers resistive collector loads had been used (See Figure 5.2). Op-amp ICs which use the current-source-as-collector-load technique include the RM4101, shown in Figure 5.3 and the 741, shown in Figure 5.4. The 741 is the internally compensated version of the 101.

The 709 has a typical open-loop voltage gain of 45,000; its total diffused resistance is 171 kΩ. The 741 has a typical open-loop voltage gain of 125,000; its total diffused resistance is 56 kΩ and it includes short-circuit protection as well as a 30-pF metal-oxide-semiconductor frequency compensating capacitor which eliminates any need for external hardware. The die sizes of both the 709 and 741 are identical at 55 mils square.

The 709 has three gain stages and most of the 171 kΩ of diffused resistance is in the ac signal path, whereas only 12 kΩ of the 56 kΩ of the 741 is in the ac signal path. Liberal use of lateral pnp transistors is made in the 741 and 4101 but their use is restricted to areas where their inherently poor frequency characteristics will not hamper the amplifier's frequency response.

5.1 THE INPUT STAGE

In the second-generation (741,4101) op-amp ICs, the input transistors Q_1 and Q_2, in effect, are emitter followers which drive the emitters of Q_3 and Q_4 differentially (See Figure 5.5). Since Q_3 and Q_4 are lateral PNP transistors, they are used as common-base amplifiers; this permits their poor frequency characteristics to be circumvented. Transistors Q_5 and Q_6 are a current source and provide the load for Q_4. A not-so-obvious advantage of this configuration is that it allows the full differential current gain to appear single ended at the collector of Q_4. Should I_4 increase, (I_3 will decrease by the same amount) and this decrease will produce a similar decrease in I_6 ($I_4 = I_6$ in the balanced condition). The net effect will be an output current equal to $I_4 - I_6$. Since I_6 is always equal to I_3, the output current will be $I_4 - I_3$.

Several advantages are obtained by using this unlikely looking circuit. These are:

1. The necessary level shifting is accomplished differentially in the first stage using transistors in a configuration which minimizes the effect of their poor frequency characteristics.
2. An extremely high output impedance (2 MΩ) is provided for driving the second stage and a node is available where frequency compensation can be accomplished easily.

3. High-voltage gain is achieved since the collector of Q_4 sees only the input impedance of the second stage as a load.
4. The ac input impedance is doubled because of the two additional base-emitter junctions between the input pair.
5. Because of the uniformly doped epitaxial base of the lateral pnp transistor, BV_{CBO} equals BV_{EBO}, at a value of 80 - 90 volts. With this type of input configuration, a circuit designer can use a differential input voltage range equal to the supply voltage, without destroying the device. If conventional pnp transistors were used in place of the laterals, the input voltage range would be limited to $\pm$ 14 volts.
6. The output is conveniently located so that a simple npn common-emitter amplifier can be used as the second stage.

5.2 THE SECOND STAGE

The second stage, or driver (Figure 5.6) is a standard Darlington-configured npn common-emitter amplifier with a pnp current source as the collector load impedance. The compensation capacitor is usually applied around this stage to obtain a constant 6 dB/octave roll off out to unity gain. The advantages of placing the feedback here are that a very high impedance (1 MΩ) is seen at the input and high current gain (2×10^4) is available from this stage. In this manner a relatively small (30 pF) capacitor can limit the open-loop bandwidth of the amplifier to 7 Hz.

5.3 THE OUTPUT STAGE

The output (Figure 5.7) is usually taken from a complementary emitter follower operated near or at class-B operation. A small amount of standby current (100μA) is maintained thru the output pair to eliminate crossover distortion. The main advantage of this output configuration is the large amount of output current available in the positive and negative direction. However, to get this current gain we need another PNP transistor. There are two methods of obtaining a pnp transistor at the output: (1) Use a vertical or substrate pnp which uses a p base diffusion as the emitter, the n epitaxial layer as the base and the p substrate as the collector. This method can only be applied when the collector is connected directly to the most negative voltage in the circuit. However, this device leaves much to be desired as a transistor. It's current gain is usually low because of the wide base width and the gain falls off rapidly above 1mA collector current. (2) Connect a lateral pnp and a standard npn transistor together as shown in Figure 5.8. This configuration provides an equivalent pnp current gain equal to the product of the pnp and npn current gains. The beta cutoff frequency for this device will be the same as for the pnp transistor alone.

The standby current for the output stage is usually developed by inserting either a resistor or diffused junctions (diodes, base-emitter junctions) between the bases of the output pair transistors and in series with the driver's collector load. The use of resistors is usually not desirable because of poor thermal matching as compared with diodes. Active diodes ($V_{CB} = 0$) or transistors are generally used to develop the necessary turn-on voltage required for the proper standby current.

5.4 BIASING CIRCUITS

Second-generation op amps are not restricted to a narrow range of supply voltages. Most amplifiers can be operated successfully over a 5:1 supply-voltage range. This

gives the user great flexibility in designing circuits. Again, the reason is the simple current source shown in Figure 5.1. For a given input current, the output current will be maintained for output voltages from near saturation to BV_{CEO}; the output impedance will equal h_{oe}.

Biasing of operational amplifiers can be accomplished in several ways. The simplest method is used in the 741 (Figure 5.9). Here the main bias supply is simply a resistor (R_5) with one reference diode connected at each end and current sources Q_{11} and Q_{13} connected to the diodes. The current that flows thru R_5 equals the collector current of Q_{13}. The current through Q_{10} is less than the current thru R_5 because of the addition of R_4 to the emitter of Q_{10}. It's value can be determined by calculating the ratio of the current through R_5 to the current required through Q_{10}. Since $V_{be}/\Delta I_c$ = 18 mV/ octave (60 mV/decade) the voltage across R_4 can be determined and this allows the determination of R_4 ($R_4 = \Delta V_{be}/I_e Q_{10}$). Q_{10} collector current will change relatively little with large changes in R_5 current due to the logrithmic relationship of the currents.

A more sophisticated circuit is used in the 4101 (Figure 5.10). In this circuit, a constant collector current is maintained through Q_{19} while the supply voltage is varied over a wide range. A relatively constant current through Q_{19} is obtained because the V_{be} of Q_{18} changes by only 18 mV/octave of the collector current. For a 4:1 change in supply voltage, the collector current of Q_{18} will also change by 4:1 (since almost all the current through R_1 becomes the collector current for Q_{18}). Since R_1 is a buried FET resistor, it's value is voltage dependent, increasing with increasing voltage, so that the actual change in Q_{18} collector current will be less than the supply voltage change.

For Q_{19} to properly bias Q_{18}, it must also supply current through R_9. At an operating current of about 100 μA the V_{be} of Q_{18} will be approximately 600 mV, and the current thru R_9 will be 60 μA. Thus, when the V_{be} of Q_{18} changes 36 mV for a 4:1 (2 octave) change in supply voltage, the current Q_{19} has to supply to R_9 changes by only 6%; Q_{19} also has to supply the base current of Q_{18} but this need is small compared to the current thru R_9. Although the 300-kΩ resistor R_1 in Figure 5.10 looks as though it would require a large amount of die area, it is in fact a buried epitaxial field-effect-transistor used as a resistor and it consumes less die area than the 39-kΩ resistor of Figure 5.9.

Another bias circuit which bears attention is the one required to supply the input pnp transistors with base drive. Here, to maintain the proper operating current for the first stage, the base drive to Q_3 and Q_4 must change because the current gain of Q_3 and Q_4 is process and temperature dependent.

The 101 uses the circuit shown in Figure 5.11. As mentioned in the previous discussion of Figure 5.10, Q_{20} has a constant emitter current supplied to it by Q_{19}. Because of the common process and temperature conditions that exist, the current gain of Q_{20} will track the current gains of Q_3 and Q_4. The base current of Q_{20} is used as the base drive for Q_3 and Q_4. This is accomplished by using Q_{21} and Q_{22} as a current source to transfer the base current of Q_{20} to the base of Q_3 and Q_4. This scheme requires that Q_{20} and Q_3, Q_4 track and as a result, this is an open-loop approach.

The 741 uses the circuit of Figure 5.12 to bias it's input stage. This circuit is a

closed-loop system which does not require matching or tracking of current gains (except for Q_3 and Q_4, of course). The circuit is designed so that I_{10} equals the sum of the input pair (Q_1, Q_2) collector currents. As an example, as temperature increases, less base drive (I_{34}) is required to maintain I_3 and I_4 constant; therefore if I_9 does not change, I_3 and I_4 will increase. However, $I_3 + I_4 + I_{34}$ passes thru the reference diode Q_8. As the current thru Q_8 increases, it causes an equivalent increase in the collector current of Q_9. Increasing I_9 will then reduce the base drive to Q_3 and Q_4, restoring the original collector currents. Mathematically the argument can be presented as follows:

$$I_{10} = I_{34} + I_9 \text{ and } I_9 = I_3 + I_4 + I_{34} \tag{5.1}$$

since the collector current of Q_9 equals the collector current of Q_8.

$$\text{If } I_3 = I_4 = I_c \text{ and } I_{34} + \frac{2I_c}{h_{fe}} \text{ then } I_{10} = 2I_c \left(1 + \frac{2}{h_{fe}}\right) \tag{5.2}$$

This analysis has neglected Q_9's current gain. In reality the base current of Q_9 also contributes to the collector current of the first stage (which means not all of this current flows thru Q_8). This modifies the solution slightly. Assuming the h_{fe} of $Q_9 \approx h_{fe}$ Q_3 - Q_4 because of the identical processing and geometries (not the case with the 101) and that the V_{be} matching of Q_8 and Q_9 always maintains equal emitter currents, then:

$$I_8 + \frac{I_9}{h_{fe}} = I_3 + I_4 + I_{34}; \quad I_9 + \frac{I_9}{h_{fe}} = I_8 \tag{5.3}$$

and $I_{10} = I_9 + I_{34}$ as before. Simplifying,

$$I_3 = I_4 = I_c \text{ and } I_{34} = \frac{2I_c}{h_{fe}}$$

Then:

$$I_9 \left(1 + \frac{2}{h_{fe}}\right) = 2I_c + \frac{2I_c}{h_{fe}}$$

$$I_9 = I_{10} - I_{34} = I_{10} - \frac{2I_c}{h_{fe}}$$

$$\left(I_{10} - \frac{2I_c}{h_{fe}}\right)\left(1 + \frac{2}{h_{fe}}\right) = 2I_c \left(1 + \frac{1}{h_{fe}}\right) \tag{5.4}$$

Solving for I_{10} yields:

$$I_{10} = 2I_c \left(1 + \frac{2}{h_{fe}^2 + 2h_{fe}}\right) \tag{5.5}$$

For an error of $<10\%$ in $I_{10} = 2I_c$, $h_{fe} > 3.5$.

A current gain of greater than 3.5 is easily achieved with proper geometry and processing.

5.5 FREQUENCY COMPENSATION

Second-generation fully compensated operational amplifiers apply frequency compensation to one stage only, the driver. The reason the driver is selected is the high input and output impedances associated with it; the driver has high current gain and is isolated from outside influences by the input and output stage. The high input

impedance and high gain of the driver stage provide the designer with the means of achieving a low roll-off frequency (6 Hz) using a relatively small 30-pF capacitor. The capacitor is placed at a point in the circuit where a pole already exists due to the C_{ob} (2 pF) of the driver transistor.

The driver can be considered to be a 60-dB amplifier with an input and output impedance of 1.4 MΩ and 90 kΩ which is driven from a 2.5 MΩ source impedance.

The open-loop bandwidth can be obtained from the formula:

$$BW_{(-3dB)} = \frac{1}{2\pi(1 + A_{V2})\ (C_{comp} + C_{ob})\ \left[(R_{01} \,//\, R_{IN2}) + R_{02}\right]} \qquad (5.6)$$

Applying the values of Figure 5.13 yields:

$$BW_{-3dB} = 6 \text{ Hz}$$

You may ask why compensate at all? Because a second pole exists at 3 to 5 MHz where the amplifier still has 10 to 20 dB gain. By the time the gain falls to 0 dB, the amplifier's phase margin would be approaching 0 . In reality, a negative phase margin would exist due to substrate and various stray capacities. Enough compensation is applied so that the gain margin is 10 to 20 dB.

5.6 DERIVATION OF GAIN

The 741 amplifier can be analyzed to indicate how this type of op-amp IC derives its high gain from just two gain stages. The 741 has been chosen for analysis because of its straight forward design. (Refer to Figure 5.4).

5.6.1 DETERMINING THE DC BIAS CURRENTS:

The amplifier's bias current is determined by R_5 and R_4. At ±15 volts the current thru R_5 is:

$$I_5 = \frac{V^+ + V^- - V_{be12} - V_{be11}}{R_5} \qquad (5.7)$$

where $V+ = V^- = 15$ V, $V_{be12} = V_{be11} = .6$ V, and $R_5 = 39$ kΩ

Substituting these values, $I_5 = 740$ μA.

Since Q_{12} is the reference diode for the driver current source Q_{13}, and assuming the h_{fe} of Q_{13} is about 5, the collector current of Q_{13} will be approximately $I_5 - I_5/h_{fe}$ or 600 μA.

The determination of I_{10} must be arrived at graphically or by successive approximations. The designer of the circuit does not have this problem since I_{10} is known to him and his only problem is finding the value of R_4. Incidentally, the actual value of R_4 is about 2800 Ω not the 5000 Ω which appears on the schematic.

To solve for I_{10} graphically, take a sheet of 3-cycle semi-log graph paper. Plotting ΔV_{be} 0 to 180 mV along the linear axis and I_c, 1 μA to 1000μA along the log axis, draw a straight line from the coordinate 0 mV - 1μA to 180 mV - 1000μA (60 mV/decade). This line represents the movement of V_{be} - VS - I_c for Q_{11}. Now plot a curve of $(\Delta V_{be} + R_4 I_c)$ - VS - I_c for Q_{10}. For example, at $I_c = 1$ μA, $V_{be}' = \Delta V_{be} + R_4 I_c = 0$ mV + 2.8 kΩ (1μA) = 2.8 mV. At $I_c = 10$μA, $V_{be}' = \Delta V_{be} + R_4 I_c = 60$mV + 2.8 kΩ

(10 μA) = 88 mV.

Repeat this procedure for 2, 5, 20, 50 and 100 μA Using a french curve, connect the points calculated. Draw a line along the I_c = 740 μA line until it meets the Q_{11} line. Draw another line perpendicular to the 740 μA line, joining it at the intersection of the Q_{11} line (about 172 mV). Continue the 172-mV line until it reaches the $Q_{10} + R_5$ line. Read the current (I_c) at the intersection (about 27 μA).

We now have established that the driver is operating at 600 μA and the input stage is operating at about 27 μA (13.5 μA each side) based on the discussion of the 741 input-stage bias scheme.

5.6.2 DETERMINING THE INPUT STAGE GAIN

The gain (g_m) of the input stage is determined by its operating current and is given by the formula $g_m = \frac{I_c}{V_{be}} = q\ I_c/kT$ or $I_c/26$ mV at room temperature. However, only 1/4 of the input signal voltage (V_i) appears across either input of Q_3 or Q_4 (a total of 4 V_{be} junctions appear across V_i). Since $V_i = 4\Delta V_{be}$, then the output signal current for each side is 1/4 g_m V_i. The circuit of Q_5, Q_6, and Q_7 translates Q_3 signal current to the output of Q_4, thus doubling the output signal current. The output current (I_o) is $\Delta I_3 + \Delta I_4$ (from previous discussion) or (1/2) g_m V_i. At I_c = 13.5 μA, g_m = 500 μmhos; therefore the output current $I_0 = V_i$ 250 μmhos. At 13 μA for I_c, the hoe of Q_4 and Q_6 is 0.2 μmho. The output impedance of the input stage is thus:

$$R_{01} = \frac{1}{hoe_4 + hoe_7} = 2.5\ M\Omega$$

5.6.3 DRIVER STAGE GAIN AND IMPEDANCE LEVELS

Knowing that Q_{17} is operating at 600 μA collector current (almost all of Q_{13}'s collector current flows through Q_{17}) and Q_{16} operates at 15 μA ($V_{be\ 17}/R_{12}$) + I_{b17} and assuming the current gains of 150 for Q_{17} and 100 for Q_{16}, input impedance can be calculated.

$$R_{IN2} = (h_{fe16} \times h_{fe17})\ (R_{11} + r_{e17})$$

If $r_{e17} = \frac{26}{.6(mA)} = 43\Omega$ and $R_{11} = 50\ \Omega$, then

$$R_{IN2} = 1.40\ M\Omega$$

$$R_{02} = \frac{1}{hoe_{17} + hoe_{13}}\ ;\quad R_{L_2} = h_{fe_{14}} R_L$$

Then: $R_{02} = 125\ k\Omega$ $R_{L_2} = 300\ k\Omega$

where $hoe_{17} = 4\mu$ mho, $hoe_{13} = 4\mu$ mho, $R_L = 2\ K\Omega$, and $h_{fe_{14}} = 150$.

For a total collector impedance (R'_{L_2}) of $R_{02}/\ /R_{L_2} = 88.5\ k\Omega$:

$$A_{V2} = R'_{L2}/(r_{e_{17}} + R_{11}) = 950 = 59.6\ dB$$

Since the input impedance (R_{IN2}) of the driver has been found, the voltage gain (AV_1) of the input stage can be calculated.

$V_{01} = I_o (R_{01} \,//\, R_{IN_2})$ and $I_o = (1/2)\, g_m\, V_i$

$$A_{V_1} = \frac{Vol}{Vi} = (1/2)\, g_m\, (Ro_1 \,//\, R_{in_2}) = 225 = 46.1 \text{ dB}$$

where gm $\doteq$ 500 μmhos

R01 - 2.5 MΩ.

$R_{IN2} \doteq$ 1.4 MΩ.

Overall amplifier gain $A_V = A_{V1} + A_{V2}$. Therefore:

A_V = 59.6 dB + 46.1 dB = 105.7 dB (172,000)

5.6.4 CALCULATION OF OPEN-LOOP BANDWIDTH:

Refer to Figure 5.13. In the discussion on frequency compensation it was shown that the bandwidth is determined by the gain and input impedance of the driver, the output impedance of the input stage and the value of compensation capacitor used. The bandwidth may be expressed by:

$$BW(f) = \frac{1}{2\pi(A_{V2} + 1)\,(C_{ob} + C_{comp})\,(R_{01} + R_{IN_2})}$$

where: $A_{V2} \doteq 950$, C_{ob} = 2.5 pF, C_{comp} = 30 pF, R_{0_1} = 2.5 MΩ, and R_{IN_2} = 1.4 MΩ. Using the above values, BW(f) = 5.8 Hz. Knowing BW and A_V, the 0 dB gain frequency may be found as follows:

f (0 dB) = BW (A_V)

f (0 dB) = 5.8 HZ (1.72×10^5) = 1 MHz.

REFERENCES

Lin, H. C., et. al., "Lateral Complementary Transistor Structure for Simultaneous Fabrication of Functional Blocks," Proc. IEEE, Dec. 1964, pp. 1491-95.

FIGURES

Figure 5.1. Current-source collector load first used in LM101.

Figure 5.2. Operational amplifiers of the 709 type use resistive collector loads.

Figure 5.3. Complete circuit diagram for 101 op-amp IC.

Figure 5.4. The 741, like the 101, uses the current-source-as-collector-load approach. The 741 includes a 30-pF capacitor which eliminates the need for external compensating elements.

Figure 5.5. Input stage for 101 and 741 type op-amp ICs.

Figure 5.6. Driver stage used in 741 ICs.

Figure 5.7. Complementary output stage can provide considerable positive or negative output current.

Figure 5.8 Use of a lateral pnp transistor in conjunction with a vertical npn device provides an equivalent pnp current gain which is equal to the product of the pnp and npn current gains.

Figure 5.9. Bias supply arrangement for 741 IC.

Figure 5.10. Simplified diagram representing 101 bias supply.

Figure 5.11. Input-pair bias supply used in 101 IC.

Figure 5.12. Input-stage bias supply of 741.

Figure 5.13. Equivalent circuit for driver stage.

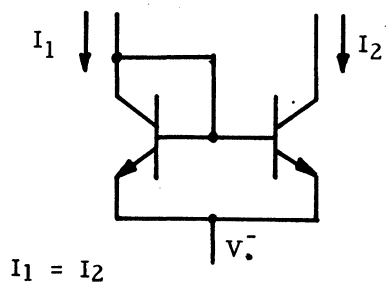


Figure 5.1. Current-source collector load first used in LM101.

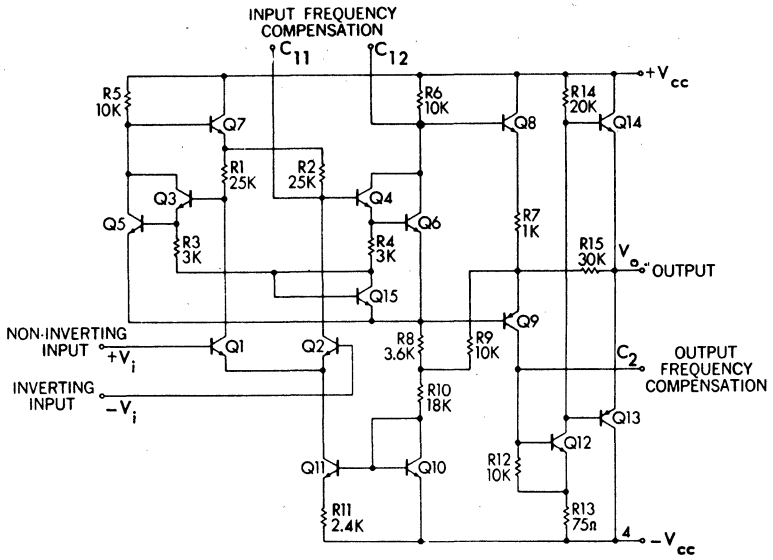


Figure 5.2. Operational amplifiers of the 709 type use resistive collector loads.

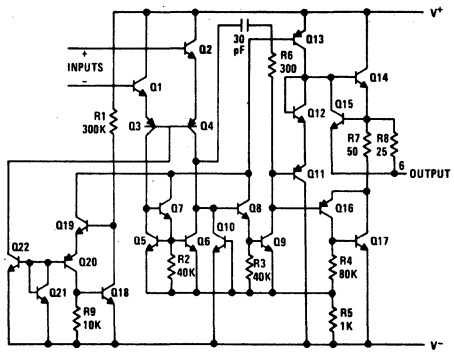


Figure 5.3. Complete circuit diagram for 101 op-amp IC.

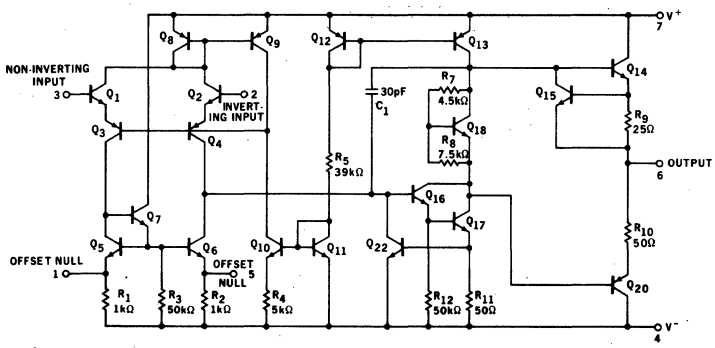


Figure 5.4. The 741, like the 101, uses the current-source-as-collector-load approach. The 741 includes a 30-pF capacitor which eliminates the need for external compensating elements.

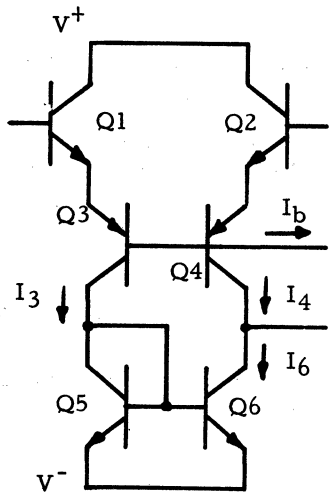


Figure 5.5. Input stage for 101 and 741 op-amp ICs.

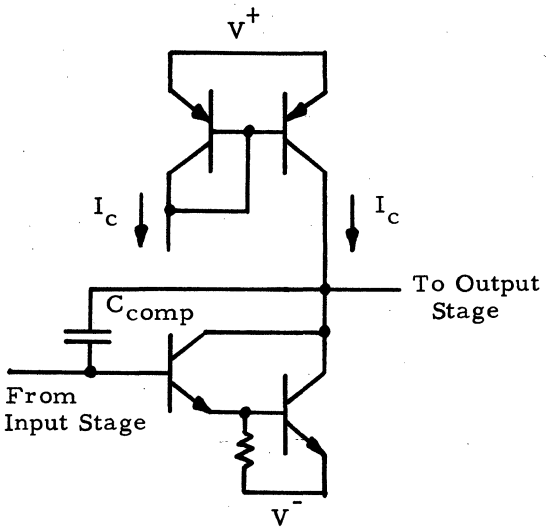


Figure 5.6. Driver stage used in 741 ICs.

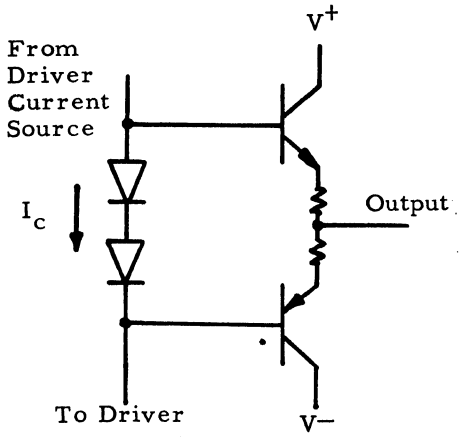


Figure 5.7. Complementary output stage can provide considerable positive or negative output current.

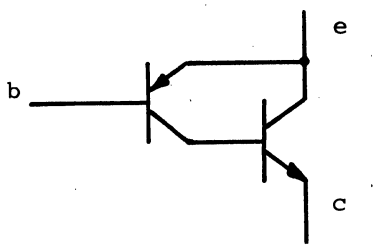


Figure 5.8. Use of a lateral pnp transistor in conjunction with a vertical npn device provides an equivalent pnp current gain which is equal to the product of the pnp and npn current gains

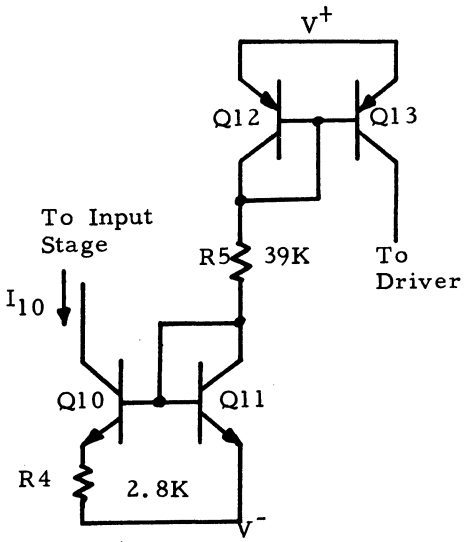


Figure 5.9. Bias supply arrangement for 741 IC.

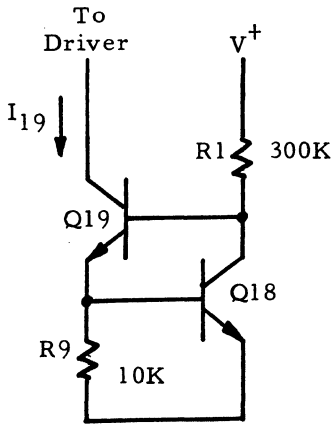


Figure 5.10. Simplified diagram representing 101 bias supply.

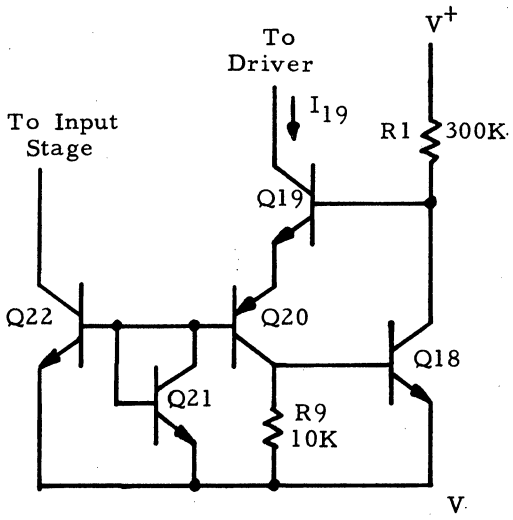


Figure 5.11. Input-pair bias supply used in 101 IC.

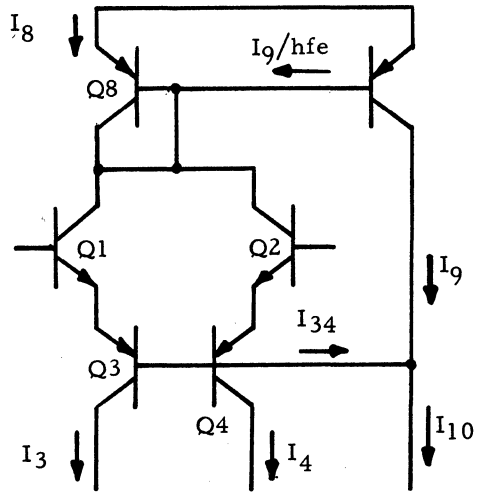


Figure 5.12. Input-stage bias supply of 741.

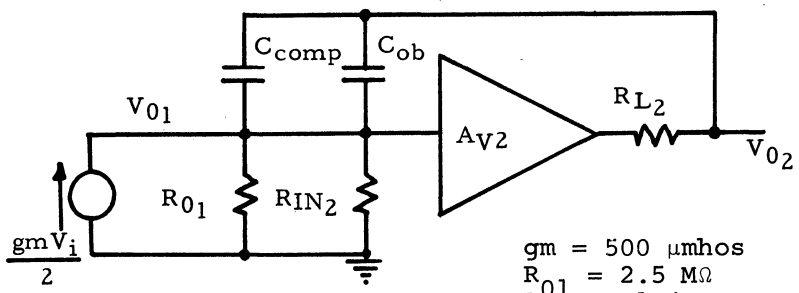


Figure 5.13. Equivalent circuit for driver stage.

gm = 500 μmhos
R_{01} = 2.5 MΩ
R_{IN2} = 1.4 MΩ
C_{ob} = 2 pF
C_{comp} = 30 pF
A_{V2} = 59.6 dB
R_{L2} = 88.5 kΩ

6

High-Frequency Characteristics Of Wideband Inverter Op-Amps

by Heinrich Krabbe
Zeltex

Amplifier characteristics such as frequency response, slew rate, and settling time are often misunderstood in high-frequency applications of wideband, inverter op amps. Frequency response and slew rate in general, are independent amplifier characteristics. They must be dealt with independently when predicting and analyzing the closed-loop response of an amplifier. For most cases, amplifier limitations in wideband applications are caused by frequency response rather than slew rate.

In the following paragraphs, general formulas are used to describe methods which allow the designer to quickly predict the performance of an amplifier in a given configuration.

Calculating frequency response, open and closed-loop transfer functions, beta, settling time, and slew rate limits are covered. A method of improving the frequency response of amplifiers is also described.

6.1 CALCULATING FREQUENCY RESPONSE

The frequency response of an amplifier can be calculated using a simple formula.

The basic frequency response of an amplifier depends entirely on its open-loop roll-off rate (normally -6 dB/octave), its gain-bandwidth point, its input impedance and the closed-loop gain configuration.

Since it is essential to know the roll-off characteristics of an amplifier to derive expressions for calculating frequency response, the 145 and 147 op amps made by Zeltex will be used as examples. The 145 is chopper-stabilized; the 147 is not.

The high-frequency sections of both amplifiers are identical; consequently, the Bode plot of each amplifier (See Figure 6.1) is identical above 30 or 40 Hz. The open-loop characteristics of the 147 may be considered a perfect single-order system (See Figure 6.2) for which the open-loop transfer function is:

$$\frac{e_{out}}{e_{in}} = \frac{-A}{\tau s+1} \qquad (6.1)$$

where A is the open-loop dc gain, τ is the time constant of the open-loop amplifier and s is the Laplace operator.

The closed-loop transfer function of a simple amplifier system is shown in Figure 6.3. The function can be expressed as:

$$\frac{e_{out}}{e_{in}} = \frac{\frac{-A}{\tau s+1}}{1+\frac{A\beta}{\tau s+1}} = \frac{-A}{(\tau s+1)+A\beta} \qquad (6.2)$$

where β is the attenuation ratio for the feedback voltage. It can be assumed that $A\beta$ is always greater than one since the amplifier is never operated at the open-loop dc gain in a closed-loop configuration. Thus:

$$\frac{e_{out}}{e_{in}} = \frac{-A}{\tau}\ \frac{1}{s+\frac{AB}{\tau}} \qquad (6.3)$$

The Bode plot for the 145 and 147 leads to the conclusion that

$$f_c = \frac{f_{GBW}}{A} \quad \text{or} \quad w_c = \frac{w_{GBW}}{A} \qquad (6.4)$$

where f_c is the desired closed-loop corner frequency (-3 dB bandwidth). Since:

$$\tau = \frac{1}{w_c}, \qquad (6.5)$$

Eq. 6.5 can be combined with Eq. 6.4 resulting in

$$T = \frac{A}{w_{GBW}} \qquad (6.6)$$

Substituting this term into Eq. 6.3 provides:

$$\frac{e_{out}}{e_{in}} = -w_{GBW}\left[\frac{1}{s+B\ (w_{GBW})}\right] \quad \text{or} \quad -\frac{1}{\frac{s}{w_{GBW}}+\beta} \qquad (6.7)$$

Since s is j_w (Laplace operator), Eq. 6.7 can be rewritten as:

$$\frac{e_{out}}{e_{in}} = -\frac{1}{\frac{j_w}{w_{GBW}}+\beta} \qquad (6.8)$$

Thus the e_{out}/e_{in} term represents a complex quantity of which the amplitude response is simply:

$$\frac{e_{out}}{e_{in}} = -\frac{1}{\sqrt{\left(\frac{w}{w_{GBW}}\right)^2+\beta^2}} \qquad (6.9)$$

Or:

$$\frac{e_{out}}{e_{in}} = - \frac{1}{\sqrt{\left(\frac{f_x}{f_{GBW}}\right)^2 + \beta^2}} \qquad (6.10)$$

where w is replaced by f_x, w_{GBW} by f_{GBW} and f_x is the variable frequency. From the previous expression it can be seen that the -3 dB point of any close-loop amplifier depends only on β (providing the amplifier rolls-off at -6 dB/octave).

As long as the GBW of the amplifier is known, the -3 dB bandwidth can be calculated as follows:

$$\frac{f_{-3\ dB}}{f_{GBW}} = \beta \text{ or } f_{-3\ dB} = \beta f_{GBW} \qquad (6.11)$$

However, β has not been completely defined. As previously stated, B is the attenuation ratio for the feedback voltage. To derive β, the circuit of Figure 6.4 may be used.

The part of e_{out} which appears at the amplifier junction in the circuit of Figure 6.4 is:

$$e_{out} = \frac{R_{in} // Z_{in}}{R_f + R_{in} // Z_{in}} \qquad (6.12)$$

Therefore:

$$\beta = \frac{R_{in} // Z_{in}}{R_f + R_{in} // Z_{in}} \qquad (6.13)$$

For the 145 and 147 amplifiers, Z_{in} is expressed as R and is a fixed 10-kΩ resistor (provided the bandwidth terminal is open). For example if $R_f = R_{in} = 10$ kΩ then β is: $\frac{5K}{10K + 5K} = 1/3$. Substituting β equals 1/3 in Eq. 6.11, the frequency response of the 145 and 147 is found to be:

$$f_{-3db} = \beta f_{GBW} = 1/3 \times 10 \text{ MHz} = 3.3 \text{ MHz}$$

It should be kept in mind that excessive stray capacitance (expecially in the feedback

loop) can cause a high frequency shunt across R_f and consequently cause a change in β.

The frequency response can be improved to approximately 5 MHz using a 1:1 inverter configuration. That is, if $R_{in} = R_f = 1K$, then β approaches its limit of 1/2 because the value of Z_{in} remains unchanged; consequently, its shunting effect on R_{in} becomes less significant.

6.2 IMPROVING FREQUENCY RESPONSE

Generally, low impedances must be used to improve the high-frequency response of an amplifier. Since the 145 and 147 amplifiers have closed-loop integrator over-all compensation (See Figure 6.5), an ideal way of increasing the frequency response is readily available. By shunting the resistance of Z_{in}, the input impedance is decreased and the gain-bandwidth product is increased. This increase in GBW can be employed to obtain a higher frequency response; however, R_{in} and R_f must also be decreased. The following discussion explains how the frequency response of the 145 and 147 amplifiers can be increased from 5 MHz at a closed-loop gain of 1 to 10 MHz at a closed-loop gain of 10.

In Figure 6.5, with R_{BW} shorted, the extreme gain-bandwidth of the amplifiers is obtained. Figure 6.6 shows the Bode plots of the 145 and 147 amplifiers with a bandwidth terminal shorted. The dashed line represents the interpreted response curve. As shown in Figure 5.6, the amplifiers are no longer perfect single-order systems and must be handled very carefully. Since the -6 dB/octave roll-off slope continues to approximately 15 MHz, it is imperative to keep the loop closure defintely under 10 MHz if a generally stable amplifier is desired. Higher frequency loop closures can be obtained whenever needed for special circuit configurations.

If the -6 dB/octave slope continues to 100 MHz, β cannot be larger than 1/10 to assure a -3 dB point (loop-closure) at or below 10 MHz. Furthermore, a Z_{in} of 500 ohms must be assumed in the β calculations (the input impedance of the amplifier with the BW terminal shorted is approximately 500 ohms at 10 MHz.) Any intermediate resistor value can be substituted and will change the gain-bandwidth between limits of 10 MHz to approximately 100 MHz. The 100-MHz figure is approximated as shown by a dashed line in the Bode plots of Figure 6.6.

For closed-loop gain of 10 and a -3 dB point at 10 MHz, it is essential to have a gain bandwidth of at least 100 MHz. With the bandwidth terminal shorted, the resulting gain bandwidth at 10 MHz is 100 MHz. This means that β equals 1/10 of this figure (β = 1/10 x 100 MHz - 10 MHz). With Z_{in} equal to 500 ohms, R_{in} must be very small or less then 50 ohms in which case the loading of Z_{in} or R_{in} becomes equal to or less than 10%. Therefore, R_f becomes fixed at 500 ohms and β equals approximately 1/11, and the desired gain bandwidth cannot be realized. However, since most of the amplifiers have a typical gain bandwidth of at least 120 MHz, the desired bandwidth can still be obtained.

6.3 SETTLING TIME

In certain applications, it is necessary to know the settling time of an amplifier. Settling time is simply a specific definition of frequency response. The settling

time can be easily computed to any desired accuracy if the frequency response of the closed-loop system is known, provided the amplifier is a perfect single-order system and has no internal charge-discharge non-linearities.

Above the -3 dB point, the response of the closed-loop system must necessarily follow the open-loop response of the amplifier (-6 dB/octave). Thus the closed-loop has the response of an RC integrating network or single-order system with a time constant of $1/2\ f_c$. This is approximately 50 ns in the previously calculated 3.3 MHz response. Thus if the 10K/10K inverter configuration of the 145 or 147 is driven with a perfect rise square wave the output rises to 63% in 50 ns; the rise time (10 % to 90 %) is approximately 110 ns, or 2.2 time constants.

The closed-loop time constant ($1/2\ f_c$) is used as the basis for finding the theoretical settling time. Since an accuracy of 1 % requires approximately five time constants (seven time constants for 0.1 % and ten for 0.01 %), the closed-loop constant is simply multiplied by the number of constants to obtain the desired accuracy. The settling time to this accuracy may then be calculated. Care must be used in making actual measurements since settling times to 0.01 % within 2 microseconds are very difficult to measure. The circuit shown in Figure 6.7 is recommended for measuring settling time.

The values of resistors connected to point e_e must be kept low because of the input capacity of the oscilloscope (the oscilloscope must have a fast overload recovery time) Also the input signal must be a clean, fast rising square wave since ringing on the leading and trailing edges greatly impairs the reading. The waveform at point e_e for $R_{in} = R_f$ is a differentiated impulse representing 1/2 the difference between e_{in} and e_{out}. Therefore, if a 20 V peak-to-peak squarewave, is used on the input, the time for a 0.01% accuracy reading must be measured to where the error signal at e_e is less than 1 mV.

6.4 SLEW RATE

Frequency response seldom influences or limits the slew rate. Slew rate limitations are mainly influenced by internal phase-compensation networks, current-drive capabilities in output or driver stages, and output loading.

The maximum rate of rise of output voltage which the amplifier can sustain, regardless of the rise time of the input signal, is known as the slew rate. However, the rise time of the output voltage of fast amplifiers is usually limited by the amplifier's frequency response rather than by slew rate.

This can be proven by noting that the minimum slew rate of the 145 and 147 amplifiers is 250 V/μs; however the maximum slew rate required for passing a 10 V peak-to-peak square wave is 200 V/μs (using the calculated time constant of 50 ns, i.e., 10 V/50 ns). This maximum slew rate is well below the slew rate limit. Moreover, as Figure 6.8 reveals, the maximum slope is required only for a very small portion at the beginning of the slope curve. Even for a 20 V peak-to-peak signal there is no visible slew rate limitation because the amplifier has ample recovery time over the full rise time of the waveform.

This slew rate limit may also be expressed in terms of maximum frequency for full

output. To do this, the maximum slope of a sine wave is found by differentiating the expression $v = A \sin wt$ with respect to t. Thus:

$$\text{slew rate} = \frac{dv}{dt} = wA \cos wt \tag{6.14}$$

and since the maximum slope of the sine wave occurs at 0°:

$$\cos wt = 1 \tag{6.15}$$

and:

$$\frac{dv}{dt} = wA \tag{6.16}$$

Since A is the peak amplitude and is normally 10V, the derivative becomes:

$$\frac{dv}{dt} \doteq 10w \tag{6.17}$$

With a slew rate of 250 V/μs, this provides:

$$w = 2.5 \times 10^7$$

and,

$$f = \frac{2.5 \times 10^7}{6.28} = 4 \text{ MHz}$$

which assures that a 4-MHz sine wave of 1- V (peak) can be sustained by the amplifier without distortion.

An amplifier may not meet slew rate specifications if the output current capability is exceeded. Care must be taken when capacitive loading is present and fast rise times are expected. The current necessary to charge a certain capacitance can be easily found by the expression,

$$\frac{dv}{dt} = \frac{i}{c} \tag{6.18}$$

or

$$i = c \frac{dv}{dt} \tag{6.19}$$

6.5 LOOP GAIN VS. CLOSED LOOP ACCURACY AT HIGH FREQUENCIES

At dc, the loop gain of an amplifier (the portion eliminated by feedback) is the

reciprocal of its given closed-loop accuracy; that is, an accuracy of 1% indicates a loop gain of 100. However this is not true at high frequencies where the open-loop gain of the amplifier rolls-off at -6 dB/octave. At high frequencies, the loop gain required to obtain a specific amplitude accuracy is significantly decreased because of the 90° phase shift between the amplifier input and output. The gain equation of the single-order system may be used to determine the necessary loop-gain for a given accuracy at high frequencies (vector quantities due to 90° phase shift are represented by the gain equation).

For example, the loop-gain required at a point where the accuracy is 1% or the total amplitude is 0.99, is determined by the gain equation:

$$\text{Amplitude} = \frac{1}{\sqrt{(1)^2 + \frac{F_x}{F_{3\ dB}}^2}} \tag{6.20}$$

Solving for $F_x/F_{3\ dB}$:

$$(0.99)^2 \left[(1)^2 + \left(\frac{F_x}{F_{3\ dB}} \right) \right]^2 = 1$$

and

$$\left(\frac{F_x}{F_{3\ dB}} \right)^2 = \frac{1 - (0.99)^2}{(0.99)^2}$$

or

$$\frac{F_x}{F_{3\ dB}} = \frac{1}{7}$$

Consequently, the loop gain required for a 1% amplitude accuracy at high frequencies is much smaller than that required at dc. However, it must also be mentioned that for a dynamic accuracy of a given percentage, the loop gain must be the same as given for dc. Dynamic accuracy means instantaneous accuracy which includes amplitude and phase.

FIGURES

Figure 6.1. Open-loop Bode plot for 145 and 147 operational amplifiers.
Figure 6.2. Simple open-loop amplifier.
Figure 6.3. Amplifier with feedback loop.
Figure 6.4. Closed-loop amplifier showing components used in deriving β.
Figure 6.5. Block diagram representing the 147 op amp.
Figure 6.6. Open-loop Bode plot showing 100 MHz gain.
Figure 6.7. Circuit for measuring setting time.
Figure 6.8. Risetime in single-order system.

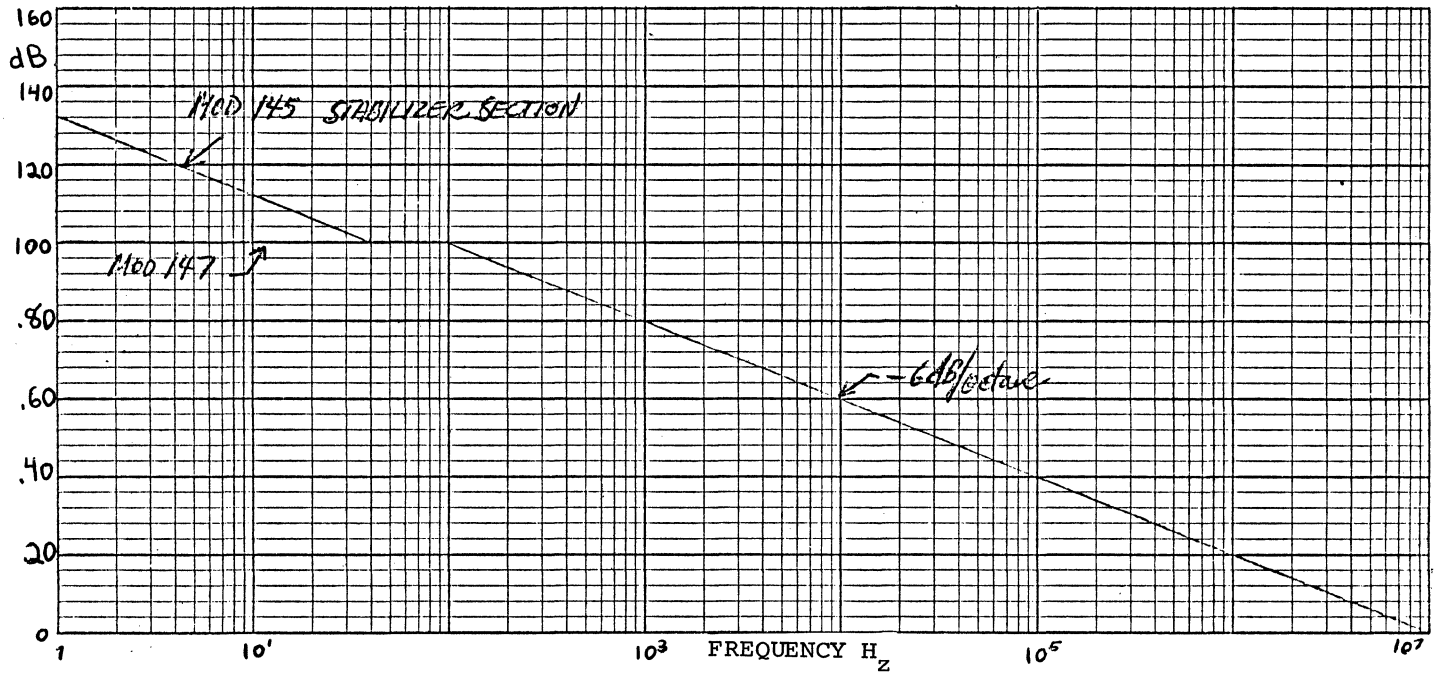


Figure 6.1. Open-loop Bode plot for 145 and 147 operational amplifiers.

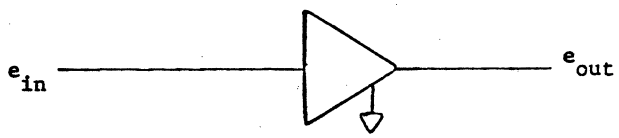


Figure 6.2. Simple open-loop amplifier.

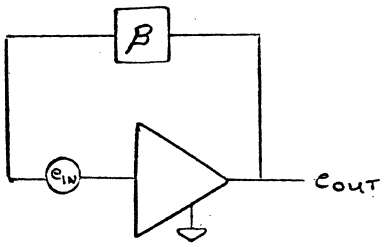


Figure 6.3. Amplifier with feedback loop.

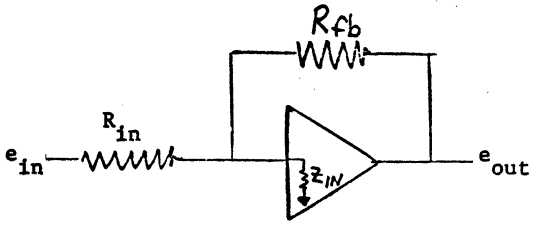


Figure 6.4. Closed-loop amplifier showing components used in deriving B.

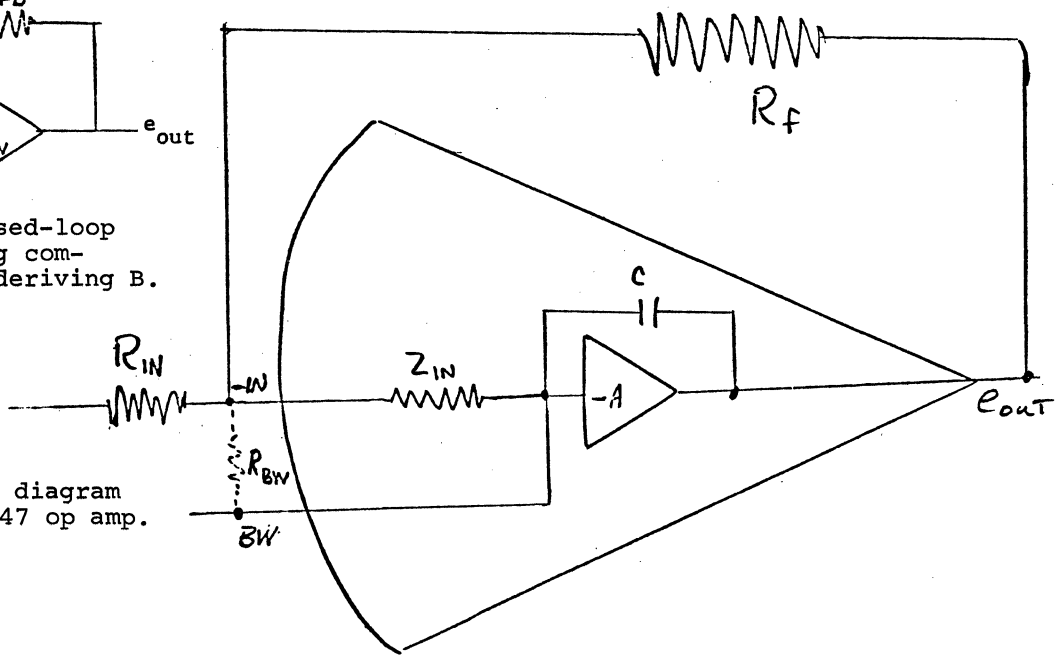


Figure 6.5. Block diagram representing the 147 op amp.

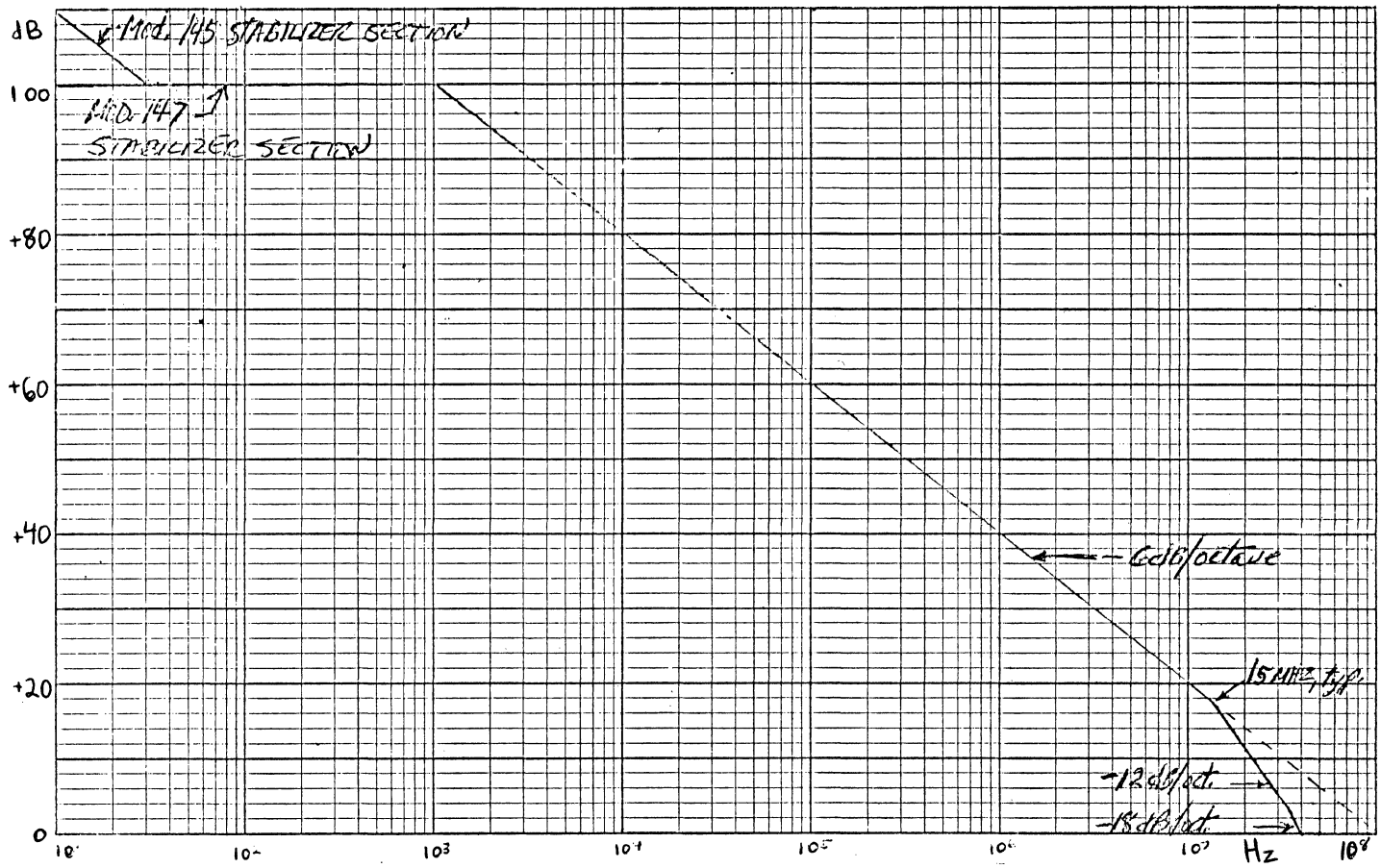


Figure 6.6. Open-loop Bode plot showing 100 MHz gain.

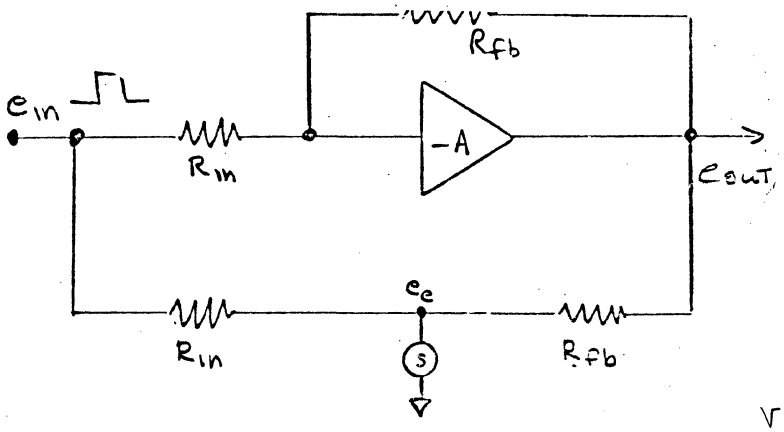


Figure 6.7. Circuit for measuring settling time.

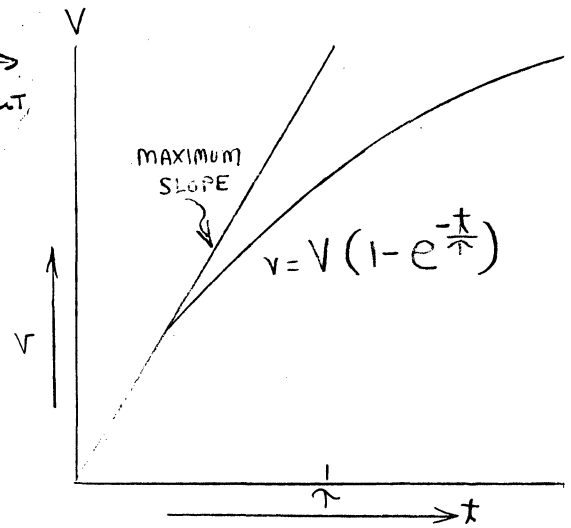


Figure 6.8. Rise time in single-order system.

7
Popular Linear Integrated-Circuit Applications

by Leonard Brown
and Ralph Seymour
Signetics Corp.

Linear integrated circuit applications historically have been performed using operational amplifiers in a "gain block" approach. This has led to the universal acceptance of the integrated-circuit op amp in just a few years and the resulting sales volume of operational amplifiers has led to a marked reduction in the price of the devices.

Nevertheless, not all applications are best suited to this approach either from an economic or a design integrity viewpoint. As a result some of the applications discussed in this article do not use operational amplifiers.

7.1 LONG TIME CONSTANT MONOSTABLE (ONE SHOT)

The circuit shown in Figure 7.1 can provide ramp durations in the 0.1-to-1.0 second range. If built with a 515 differential amplifier, it requires only a single 5-V power supply for both the amplifier and the control logic.

As illustrated, the 515 is connected as an integrator with a fixed input voltage set by the resistor divider chain (R_1, R_2, Z_1). The charging current available for the capacitor is therefore set by this fixed reference voltage and the input resistor R. The slope of the ramp voltage at the output of the amplifier is thus controlled by the resistor R and the capacitor C. With C = 5.0μF, the duration of the ramp will vary from 0.1 sec. to 1.0 sec as R is changed from 1 kΩ to 10 kΩ.

In the quiescent or stable state the $\bar{Q}$ output is high, which forces the output A low, clamping the summing junction of the amplifier around ground and causing the output of the 515 to be high. The $\bar{Q}$ output is not affected by the amplifier's "high" output as it is controlled by the "low" input from the cross-coupled Q terminal. On receiving an input pulse the flip flop changes state and the Q output goes "high". In turn, the summing junction of the amplifier is released and the amplifier integrated the dc input voltage causing a negative going ramp at the input to the cross-coupled latch. When the ramp reaches the threshold voltage of the 8481 gate, the latch changes state and resets the integrator.

In this application, the equation for the timing is approximate as it includes non-linear effects due to exceeding the 515 negative common-mode voltage.

7.2 RAMP GENERATOR

Operation of the 515 from a single supply is again illustrated in the circuit of Figure 7.2 which is a triggerable ramp generator. The amplifier is connected as an integrator with a fixed dc bias applied to its inputs through the input resistor divider bias chain. Transistor Q_1 is required to discharge the capacitor and hence reset the integrator, and is triggered through Q_2. In the quiescent state, the output sits at approximately +6 V as determined by the resistor chain R_1R_2.

Applying a positive pulse to the input turns on Q_2 and causes the transistor (Q_1) to conduct discharging C and returning the output voltage to approximately +2 V, as

determined by the input bias chain. At the end of the pulse, the base of Q_1 returns to approximately +6 V and Q_1 is reverse biased. The integrating capacitor now commences to charge through the 2.2 kΩ input resistor and the output will describe a ramp function until it is clamped by the +6 V of the bias chain (R_1,R_2) or is reset by a following input pulse.

The ramp timing (slope) is controlled by the 2.2 kΩ input resistor and the value of the integrating capacitor. Capacitor C may be calculated to a first-order approximation by the expression:

$$C = 10^{-4}/\text{Operating frequency} \qquad (7.1)$$

7.3 AUDIO PREAMPLIFIER WITH RIAA/NAB COMPENSATION

The high open-loop gain of operational amplifiers makes them natural candidates for applications requiring precision frequency-shaped characteristics at audio frequencies. An example, illustrated in Figure 7.3, is an audio preamplifier with switched equalization networks corresponding to the RIAA and NAB compensation requirements (See Figure 7.4).

The amplifier is connected in the non-inverting configuration with the frequency shaping performed in the negative feedback loop. The low-frequency response (below 10 Hz) is controlled by R_1 C_1. Capacitor C_1 is required to make the dc gain equal to unity to avoid having an excessive output offset voltage. Resistor R_{S1} should be selected to match the required transducer loading.

7.4 TONE CONTROL CIRCUIT

The circuit in Figure 7.5 is intended for use in conjunction with the circuit of Figure 7.3 to provide the bass and treble controls of a complete audio preamplifier. The IC employed is a 516 operational amplifier with unity-gain compensation in a conventional feedback configuration.

In Figure 7.5, Amplifier "A" may be a 5709 or 516. Frequency compensation as would be used for unity gain non-inverting amplifiers must be used. The turn-over frequency is 1 kHz. At 20 kHz, as can be seen from the response curve (Figure 7.6), the circuit provides 20 dB of bass boost and bass cut; at 20 kHz, there is 19 dB of treble boost and 19 dB of treble cut.

7.5 CRYSTAL OSCILLATOR

An extremely useful and simple square-wave oscillator that can be crystal controlled from 1 to 10 MHz may be constructed using only three capacitors and a 501 wideband amplifier. The availability of an external interstage connection (pins 3 and 4) on the IC simplifies the design and minimizes the number of external components required. The output drive may be increased by the addition of a 156 logic gate as illustrated in Figure 7.7.

The value of C can be calculated from:

$$C = \frac{2.12 \times 10^{-3}}{f} \text{ Farads.}$$

Depending on the specific crystal type used, the output (pin 6) of the 501 may not be high enough to drive the following logic (156). If this is the case, decreasing the value of the two capacitors will increase the output drive. If a 501A is used instead of a 501, modification of the pin numbers shown is necessary.

7.6 DOUBLY BALANCED MODULATOR

A doubly balanced modulator, useful in phase comparators, fm detectors, synchronous demodulators and balanced mixers, is shown in Figure 9.8. A 510 dual differential amplifier is employed in an ac coupled configuration.

Although the transistors display excellent matching thanks to the monolithic construction, additional circuitry is required to optimize the carrier and/or modulation balance.

For low distortion the modulation input levels should be in the order of 50 mV or less. However, if square-wave operation is satisfactory the 510 can handle input signals of up to 5 V before the device ratings are exceeded. In the higher-voltage mode of operation the load impedance should be selected to insure that the output transistors do not saturate.

In the circuit shown in Figure 7.8, greater than 50 dB signal suppression can be achieved and an output swing of 6 Vp-p is attainable. The frequencies of the carrier and modulating signal were 22 KHz and 1 KHz respectively under test conditions. Satisfactory operation can be achieved with carrier frequency up to 30 MHz.

FIGURES

Figure 7.1. Monostable multivibrator. Time constant T = 20 RC (covers 0.1 to 1 second range with C = 5 μF for 1 kΩ ≤ R ≤ 10 kΩ. Duty cycle ≤ 95%; input pulse width, 0.5 μs. Timing period starts on positive transition of input pulse.

Figure 7.2. Ramp generator. For best linear operation, use a low-loss type capacitor (such as a Mica type) for C. Q_1 can be a 2N2907 or a 2N3638. A 2N2222 or a 2N3642 can be used for Q_2 (Q_2 and its associated circuitry may be replaced by a DCL gate such as the 1/4 8841)[2].

Figure 7.3. Audio preamplifier with RIAA/NAB compensation. Output noise 0.8 mVrms (with input shorted).

Figure 7.4. RIAA and NAB compensation.

Figure 7.5. Tone control circuit.

Figure 7.6. Response curve for tone control circuit.

Figure 7.7. Crystal-controlled square-wave oscillator.

Figure 7.8. Doubly balanced modulator.

Figure 7.1. Monostable multivibrator. Time constant T = 20 RC (covers 0.1 to 1 second range with C = 5 μF for 1 kΩ R - 10 kΩ. Duty cycle - 95%; input pulse width, 0.5 μs. Timing period starts on positive transition of input pulse.

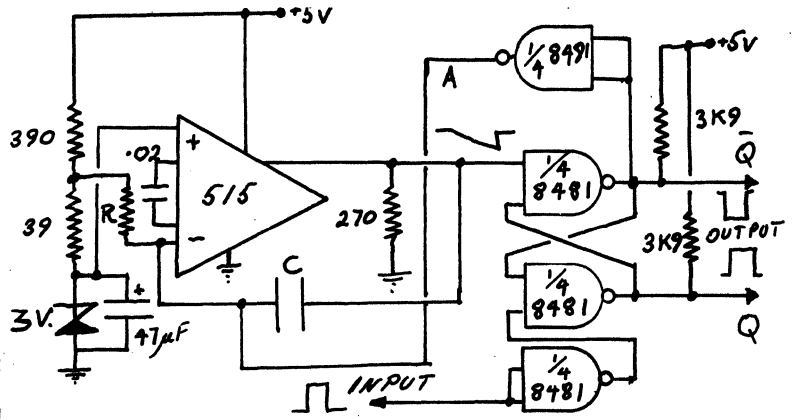
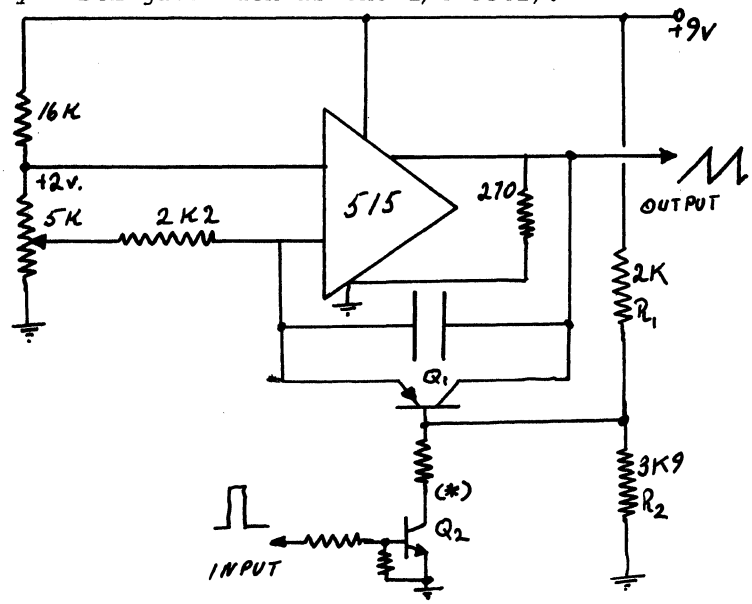


Figure 7.2. Ramp generator. For best linear operation, use a low-loss type capacitor (such as a Mica type) for C. Q_1 can be a 2N2907 or a 2N3638. A 2N2222 or a 2N3642 can be used for Q_2 (Q_2 and its associated circuitry may be replaced by a DCL gate such as the 1/4 8841).



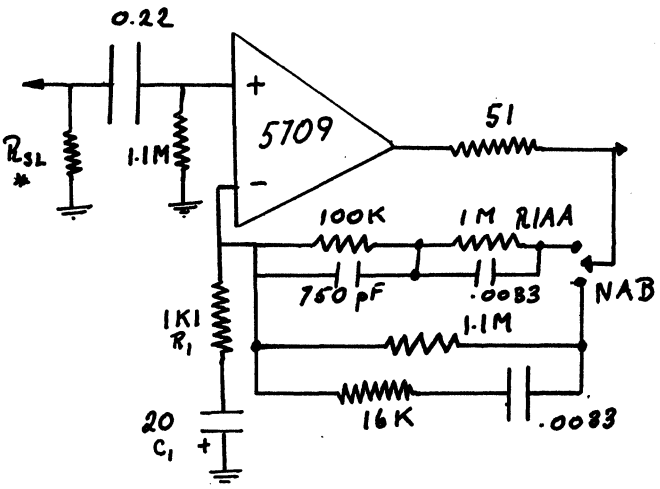


Figure 7.3. Audio preamplifier with RIAA/NAB compensation. Output noise 0.8 mVrms (with input shorted).

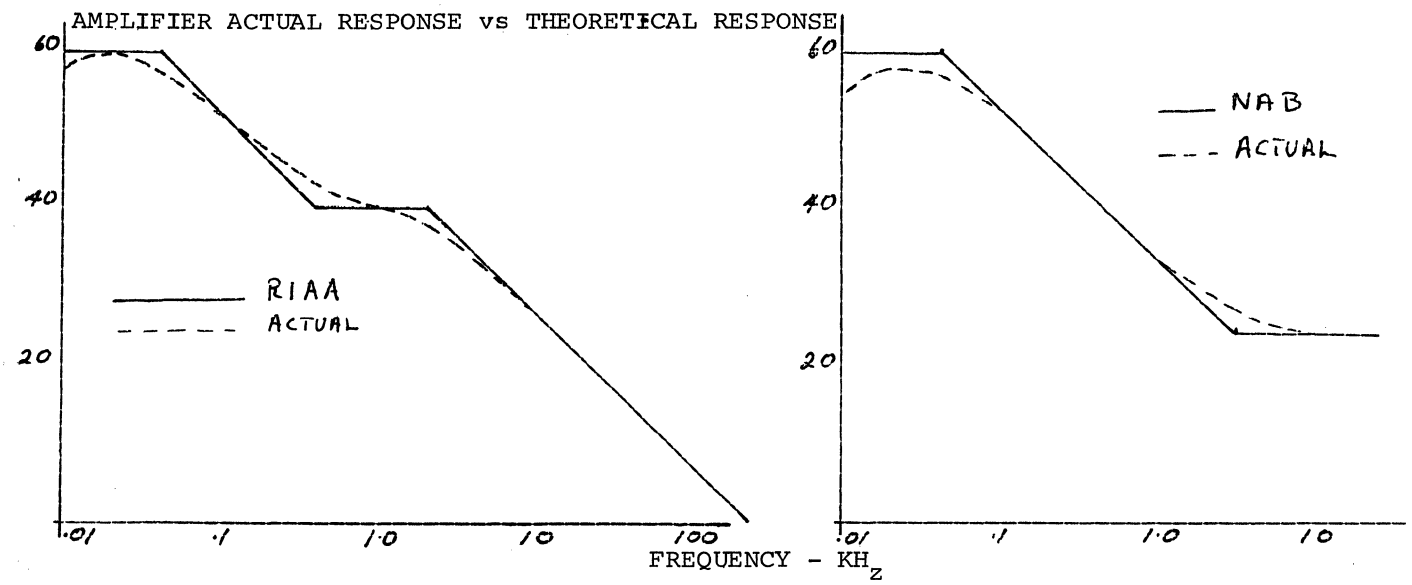


Figure 7.4. RIAA and NAB compensation.

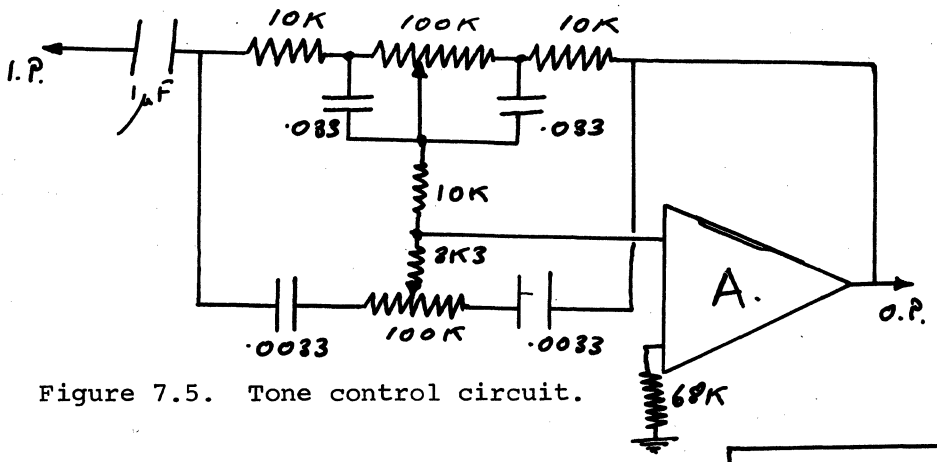


Figure 7.5. Tone control circuit.

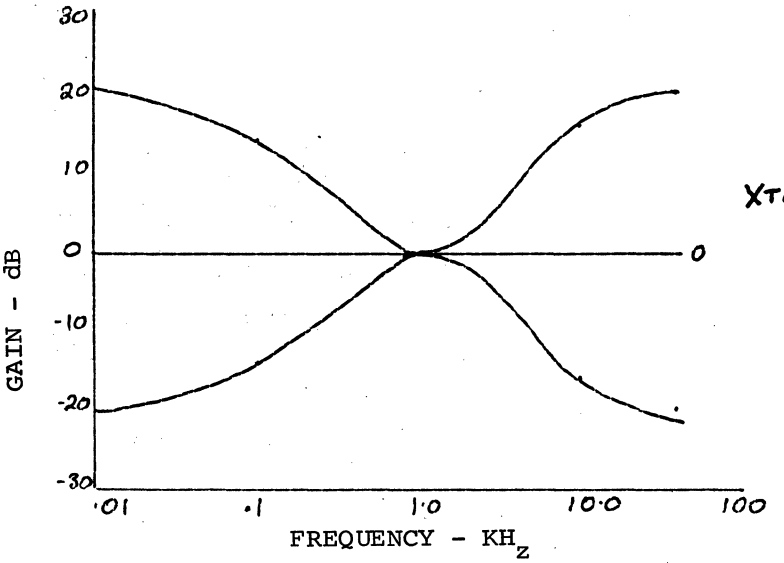


Figure 7.6. Response curve for tone control circuit.

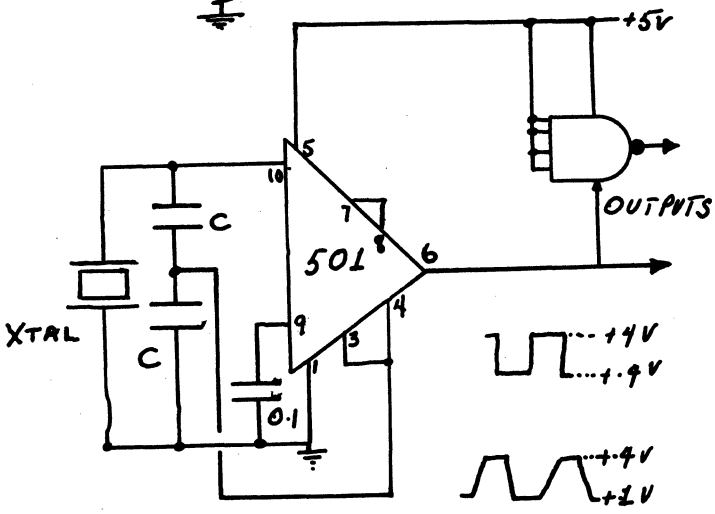


Figure 7.7. Crystal-controlled square-wave oscillator.

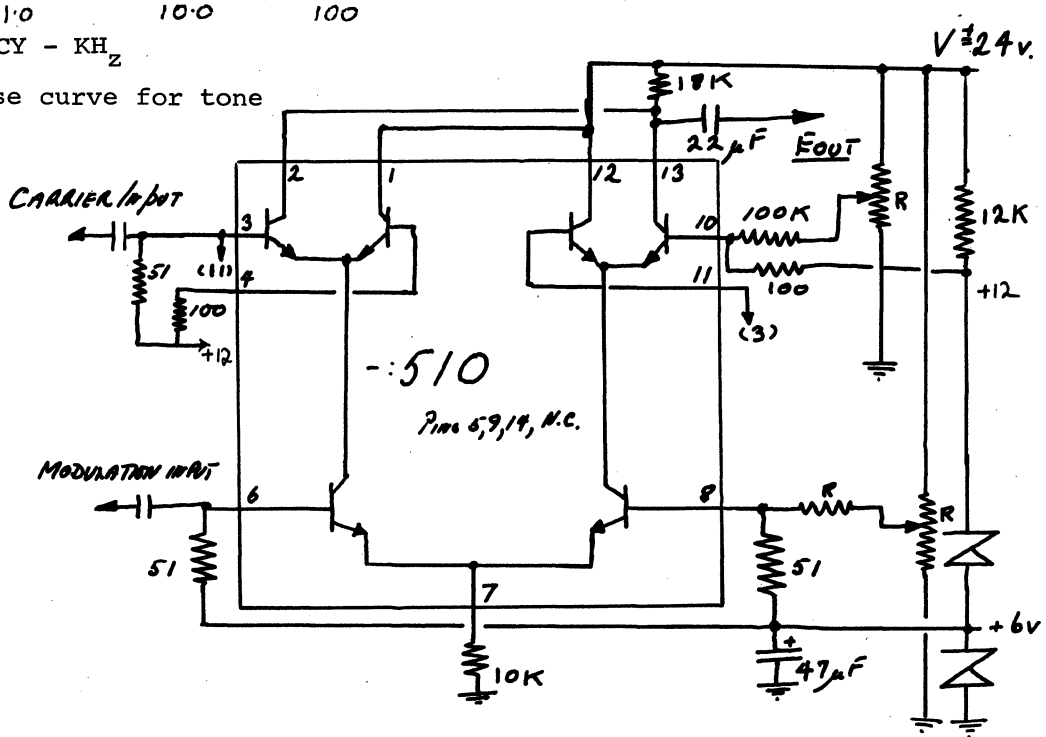


Figure 7.8. Doubly balanced modulator.

8

The Versatile Wideband IC Amplifier

by Brent Welling
Motorola

For economic reasons, a monolithic wideband amplifier should be designed so that it can fit into a wide variety of applications. In this chapter, the use of the MC1545, a wideband amplifier, will be described in applications such as a gated video switch, a preamplifier for a core-memory sense amplifier, a balanced modulator, a frequency shift keyer, an amplitude modulator, a pulse amplifier, multiplexing circuits, and others.

8.1 CIRCUIT DESCRIPTION AND OPERATION

Before moving on to the applications, a look at the MC1545 will help to clarify the discussion of its use. The circuit diagram is shown in Figure 8.1 (pin numbers correspond to the G-suffix TO-5 package). The circuit basically consists of a constant-current-source transistor Q_7 and a switching differential amplifier, Q_5 and Q_6, which splits a constant current between two differential amplifiers, or channels, composed of transistor pairs Q_1, Q_2 and Q_3, Q_4; the amount of current depends on the voltage applied at pin 1, the gating pin. The collectors of both channels are tied together and connected to a common-load resistor (1kΩ). By using this technique, the amount of current flowing through each of the 1k load resistors is constant and independent of which channel, Q_1,Q_2 or Q_3, Q_4, is conducting. As a result, there is essentially no dc level shift at the output when one channel is turned off and the other channel is turned on. The steady state measured change in the differential output voltage when switching from one channel to the other is typically 15 mV. The amplified signal which appears at the collectors of the input channels is transferred to the output via Darlington emitter followers to provide a low output impedance and at the same time buffer the input differential amplifiers from any capacitive loading which would tend to lessen the frequency response.

Common-mode feedback is provided from the emitter of the first emitter follower back to constant-current source Q_7 to stabilize the dc operating point of the circuit and provide excellent common-mode rejection.

Either of the two input channels can be selected as follows: Bias the MC1545 so that there is sufficiently positive voltage applied to the gating pin (pin 1 on the "G" package); or leave the gating pin open, so that the voltage at the base of transistor Q_6 is more negative than the voltage at the base of transistor Q_5. As a result, transistor Q_5 will be "on" and transistor Q_6 will be "off". Under this condition, all of the constant current which is established in the collector of Q_7 passes through transistor Q_5 and establishes a bias current in the differential amplifier composed of Q_3 and Q_4. Hence, any signal applied to these transistors is amplified and will appear differentially at the output. However, if the gating pin is connected to ground or some negative value, the voltage at the base of transistor Q_5 becomes more negative than the voltage at the base of Q_6, which causes the constant

current to flow through Q_6 and establishes the bias current in the differential amplifier composed of transistors Q_1 and Q_2. In this state, any signal which is applied to transistors Q_1 and Q_2 will be amplified and will appear at the output, while any signal that is applied to transistors Q_3 and Q_4 will be gated off. The voltage required to perform this gating function at pin 1 is compatible with all standard forms of saturated logic (for example: RTL, DTL, TTL).

Since either of two signals can be gated through the amplifier depending upon the application of a logic signal to the gating pin, applications which arise include a video matrix cross-point switch, a frequency shift keyer for FSK systems, a gated video amplifier, a gated oscillator, a preamplifier for core-memory sensing and a channel selector for data aquisition. In addition to these obvious uses, a number of other possible uses exist. These include the amplitude modulator and the balanced modulator.

Figure 8.2 shows a plot of voltage gain versus frequency for temperatures of -55°C, 25°C and 125°C. These curves indicate that the MC1545 is a good wideband device and can serve as a pulse amplifier. In addition to its wide bandwidth, the MC1545 is dc coupled and can provide a differential output when a signal and its complement are required as inputs to drive logic functions. Rise time, fall time, and propagation delay are typically 6 ns for this device, which makes it compatible with modern, second-generation logic systems.

As was explained earlier, the amount of attenuation which is given to an input signal when the amplifier is gated "OFF" is a function of the dc voltage at the gating pin. A curve showing this attenuation versus gate voltage is given in Figure 8.3. As would be expected, the amount the input signal is attenuated is a function of the input frequency. This characteristic is shown in Figure 8.4. The curve indicates that above 30 KHz, the amplifier begins to show a certain amount of capacitive feedthrough, primarily due to the physical closeness of the pins; performance could be improved by the use of proper shielding between pins. However, even at an input frequency of 10 MHz, a channel separation of better than 60 dB can be achieved.

Another important parameter of a wideband amplifier is common-mode rejection, which again is a definite function of frequency. This is shown in Figure 8.5 which demonstrates the reduction which occurs in common-mode rejection capability for the MC1545, as frequency increases.

8.2 VIDEO SWITCH

Figure 8.6 shows the MC1545G connected as a gated analog switch. The number of external components required for this type of application is very small. In this particular case only one resistor is required.

In this application, a signal (analog or digital) is applied to the amplifier at pin 4. With the logic signal at pin 1 at a logic 1 state (positive voltage) the input signal is amplified and passed through the amplifier. However, if the logic signal at pin 1 is at a logic 0 state, the amplifier is turned "off" and no signal will pass through the device. If it were required that the opposite logic levels pass or block the signal, the input signal can just as easily be applied to pin 2 or 3 with pins 4 and 5 grounded. In this case, a high logic level would block transmission and a

low logic level would pass the signal.

Hence, the use of inverters is not necessary. If "channel select time" is considered as the time delay from the 50% point of the gate pulse to the 50% point of the full output swing, it is approximately 20 ns. During the time that the gating logic is in the low state, the circuit which gates the MC1545 must sink a maximum of 2.5 mA, which most forms of saturated logic can do easily. When the gating logic is in the high state, the circuit which gates the MC1545 must source only the leakage current of a reverse biased diode, which is 2 μA maximum. These requirements are quite similar to the input requirements of a standard DTL or TTL logic gate.

8.3 FREQUENCY SHIFT KEYER

Rather than grounding pins 2 and 3 as was done in the circuit of the previous example, it is possible to apply a second frequency to these input pins and select which of the two frequencies, either F_1 or F_2, will be passed through the amplifier. This is illustrated in Figure 8.7. In the circuit shown, frequency F_2 will be passed when the voltage at pin 1 is greater than +1.5 V and F_1 will be passed when the voltage at pin 1 is approximately 0 V.

The MC1545 can be used as a gated sense amplifier-preamplifier in core-memory systems. By being able to strobe independent of the systems read signal, the sense amplifier can be gated on after the large common-mode pulse has passed, to sense the low-voltage level differential signal stored in the core. This reduces the sense amplifier recovery time from microseconds to nanoseconds, since the channel select propagation delay time is of the order of 20 ns.

In addition to this preamplifier application, another use can be made of this design by paralleling and cascading a number of MC1545's to form a One-of-N data selector for data processing. A simple example of this is shown graphically in Figure 8.8.

8.4 WIDEBAND DIFFERENTIAL AMPLIFIER WITH AGC

The gate characteristics of the MC1545, shown in Figure 8.3, also make it useful as an AGC amplifier. With a dc voltage applied to the gate pin, as much as 100 dB of AGC can be obtained. Since there is essentially no dc level shift with AGC, the output waveform will collapse symmetrically about zero with little or no distortion. The circuit configuration is shown in Figure 8.9.

8.5 AMPLITUDE MODULATOR

Figure 8.10 shows the gate characteristics of the MC1545 with gain plotted on a linear scale. By biasing the gate at approximately 1.025 V (Point B) and impressing an audio signal on the bias, the gain of the channel varies quite linearly between the points "A" and "C" on the curve, giving very little distortion on the output. Using the gate characteristics shown in Figure 8.10, the up-modulation (M_U) and down-modulation (M_D) may be calculated. The waveform is depicted in Figure 8.11.

The up and down modulation factors are defined as:

$$M_U = \frac{E_{max} - E}{E} \quad \text{(upward modulation)}, \tag{8.1}$$

$$M_D = \frac{E - E_{min}}{E} \text{ (down modulation)} \tag{8.2}$$

Where E = peak amplitude of the unmodulated carrier, E_{max} = maximum amplitude attained by the modulated carrier envelope E_{min} = minimum amplitude of the modulated carrier envelope.

Constraining the gate voltage to vary around the point "B" with a maximum occurring at point "A" and a minimum at point "C" and letting the rf carrier input be e_{in}, (See Figure 8.12), then

$$e_o = e_{in} A_{V_1}. \tag{8.3}$$

Thus the values of E, E_{max}, and E_{min} are

$$E = e_{in} (A_{V_1})_B \tag{8.4}$$

$$E_{max} = e_{in} (A_{V_1})_A \tag{8.5}$$

$$E_{min} = e_{in} (A_{V_1})_C \tag{8.6}$$

Substituting in Equations 8.1 and 8.2 provides:

$$M_U = \frac{(A_{V_1})_A - (A_{V_1})_B}{(A_{V_1})_B} \tag{8.7}$$

$$M_D = \frac{(A_{V_1})_B - (A_{V_1})_C}{(A_{V_1})_B} \tag{8.8}$$

Next, inserting the values of $(A_{V_1})_A$, $(A_{V_1})_B$, and $(A_{V_1})_C$, from Figure 8.10 into Equations 8.7 and 8.8:

$$M_U = 0.58$$

$$M_D = 0.54$$

These are the values of up and down modulation which can be expected without appreciable distortion.

When the circuit shown in Figure 8.12 was breadboarded and the resistor adjusted to

give the proper bias point, the results for a carrier frequency of 25 MHz and an audio frequency of 5 kHz were $M_U = 0.54$; $M_D = 0.52$.

From Figure 8.10 it is seen that the audio signal required to perform this modulation is approximately 350 mV peak-to-peak. The output waveform for this circuit is shown in Figure 8.13. As can be seen, the distortion is very low.

8.6 BALANCED MODULATOR

The MC1545 can be connected as shown in Figure 8.14 to function as a balanced modulator. The circuit operation here is quite similar to the operation previously discussed for the amplitude modulator except that the input differential amplifiers have been connected with their collectors cross-coupled. This is easily seen in Figure 8.15 where the input stage has been redrawn to reflect its actual operation. If the carrier level is sufficient to completely switch the top differential amplifier pairs, the circuit will function as indicated by the approximately equivalent circuit in Figure 8.15. Here the modulation signal is alternately switched between differential amplifiers at the carrier rate. The result is that the modulation input signal is multiplied by a symmetrical switching function which shifts the spectrum of the modulation input and places it symmetrically about the odd harmonics of the carrier. This is demonstrated in Figure 8.16.

Mathematically the switching function can be expressed as

$$S(t) = 2 \sum_{n=1}^{\infty} A_n \mathrm{Cos} n\omega_c t \tag{8.9}$$

where

$$A_n = \left[\frac{\mathrm{Sin}\left(\frac{n\pi}{2}\right)}{\frac{n}{2}} \right] . \tag{8.10}$$

Only the odd harmonics are present since $\mathrm{Sin}\ (n\pi/2) = 0$, for even values of n. If the input modulation is given by

$$e_m = E_m \mathrm{Cos}\, \omega_m t \tag{8.11}$$

then the output will be given by

$$e_o = 2\, E_m \sum_{n=1}^{\infty} A_n \mathrm{Cos} n\omega_c t \mathrm{Cos}\, \omega_m t \ . \tag{8.12}$$

By use of the following trigonometric identity:

$$\mathrm{CosACosB} = \tfrac{1}{2} \left[\mathrm{Cos}(A+B) + \mathrm{Cos}(A-B) \right] \tag{8.13}$$

the final result is expressed in the desired form:

$$e_o = E_m \sum_{n=1} A_n \left[\mathrm{Cos}(n\omega_c + \omega_m)t + \mathrm{Cos}(n\omega_c - \omega_m)t \right] \tag{8.14}$$

Hence, the output is composed of only the sum and difference frequencies (sidebands), and the carrier is suppressed. When the circuit of Figure 8.14 was evaluated, the carrier rejection that could be achieved was 62 dB with f_c = 15 kHz and f_m = 3 kHz; 47 dB with f_c = 455 kHz and f_m = 10 kHz; and 36 dB with f_c = 30 MHz and f_m = 10 kHz.

8.7 PULSE AMPLIFIER

Pulse amplifiers are used in many applications such as pulse radar intermediate-frequency circuitry, pulse-width modulation, and pulse-amplitude modulation systems.

Integrated circuits like the MC1545 are a good choice for pulse-amplifier applications because of their large bandwidth (See Figure 8.2), and dc coupling (which provides low-frequency response and therefore no droop). Also, since the IC has differential input and output, common-mode signals, such as noise, are greatly attenuated.

Figure 8.17 shows a typical pulse-amplifier connection for the MC1545 giving a voltage gain of 10V/V (20dB).

FIGURES

Figure 8.1. Circuit diagram for the MC1545G. Pin numbers shown are for the IC package in G-suffix TO-5 case.

Figure 8.2. Plots of single-ended voltage gain vs. frequency at $V_{CC} = \pm V$.

Figure 8.3. Voltage gain as a function of gate voltage.

Figure 8.4. Channel separation vs. input frequency. Channel separation = 20 log A_v - 20 log (e / e_{in}).

Figure 8.5. Common-mode rejection vs. frequency.

Figure 8.6. Video switch requires only one external resistor.

Figure 8.7. Multiplexer (frequency shift keyer).

Figure 8.8. One-out-of-four data selector and truth table.

Figure 8.9. Wideband amplifier with AGC.

Figure 8.10. Gain of amplitude-modulator circuit varies linearly between points A and C.

Figure 8.11. Amplitude-modulated waveform.

Figure 8.12. Amplitude modulator.

Figure 8.13. Output waveform for circuit in Figure 8.12 with 25 MHz rf signal and 5 kHz audio signal.

Figure 8.14. Balanced modulator. Operation of this circuit is similar to that of the amplitude modulator except that the input differential amplifiers are connected with their collectors cross coupled.

Figure 8.15. Balanced modulator model.

Figure 8.16. Balanced modulator waveforms.

Figure 8.17. Pulse amplifier.

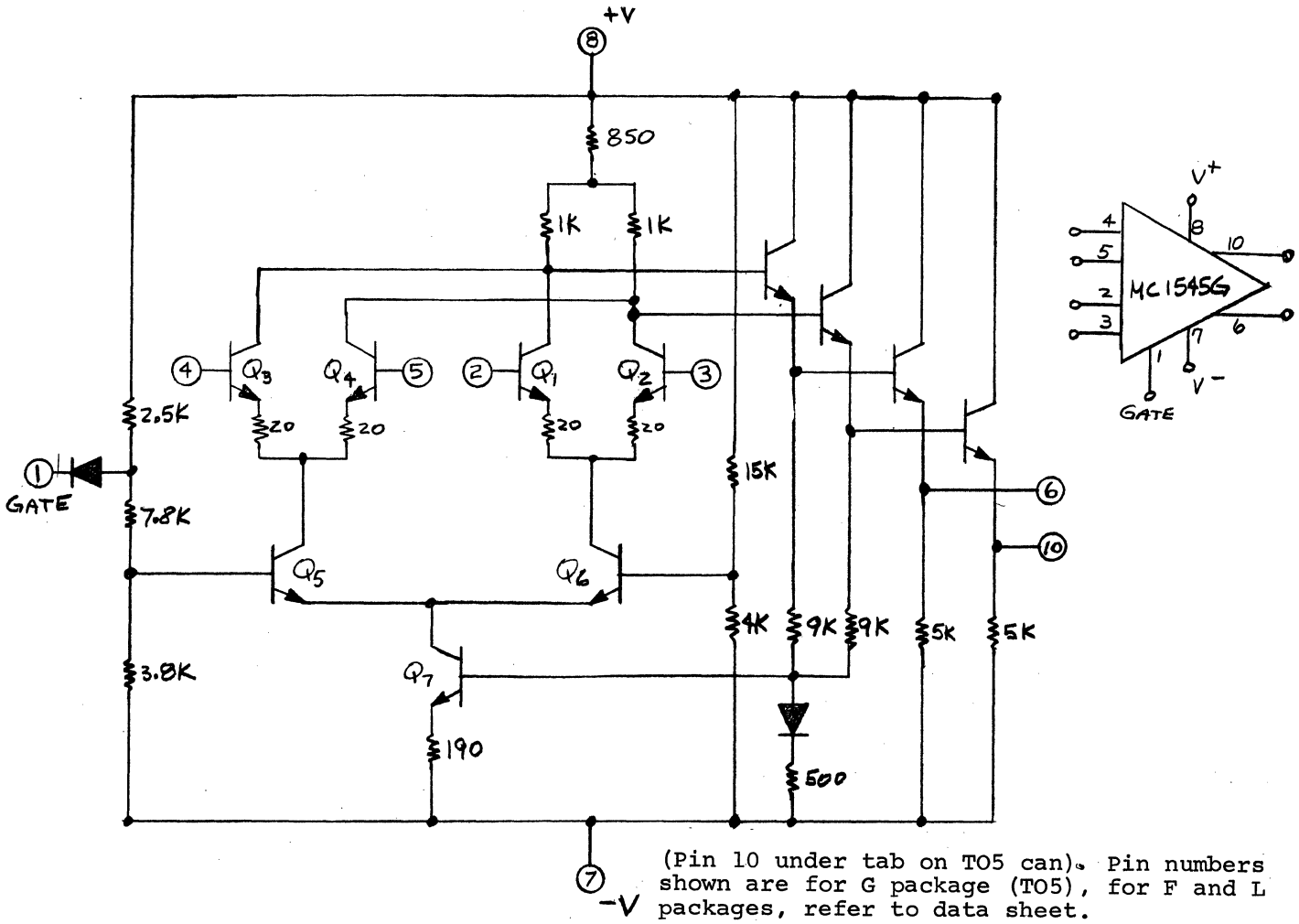


Figure 8.1. Circuit diagram for the MC1545G. Pin numbers shown are for the IC package in G-suffix TO-5 case.

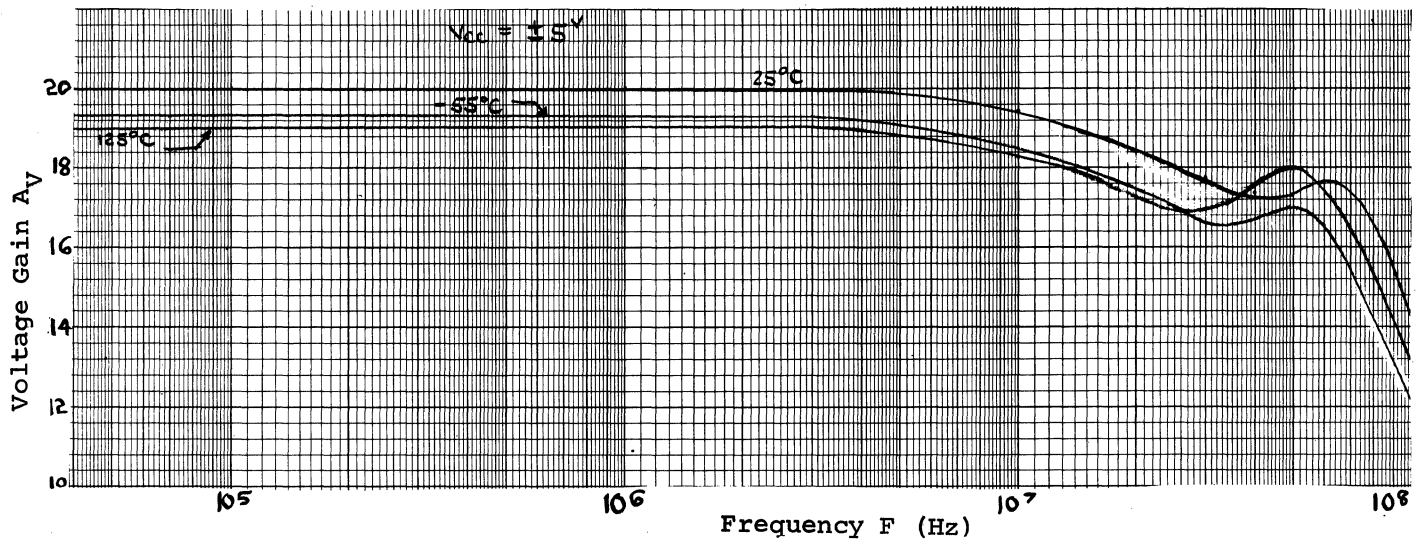


Figure 8.2. Plots of single-ended voltage gain vs. frequency at $V_{CC} = \pm V$.

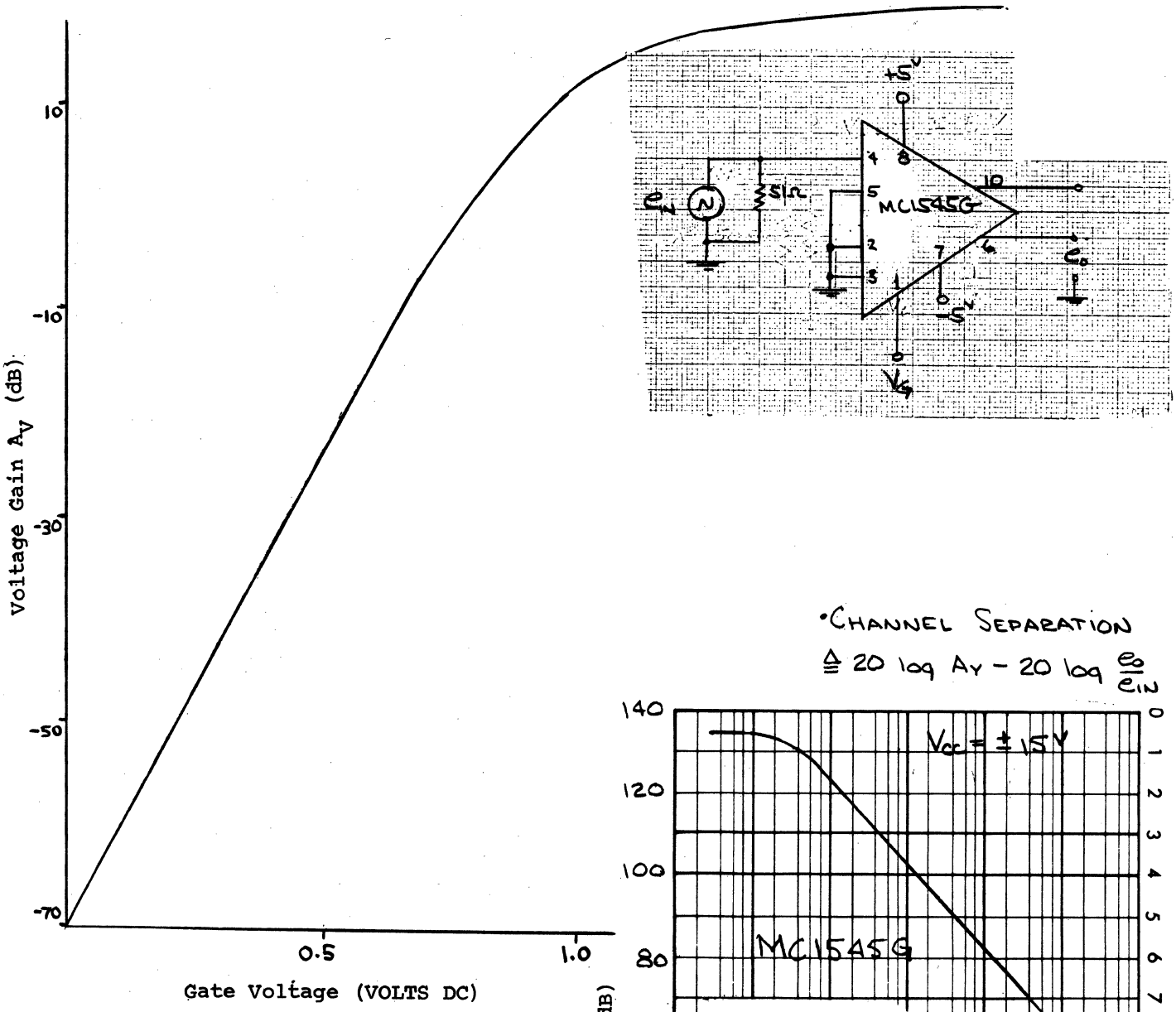


Figure 8.3. Voltage gain as a function of gate voltage.

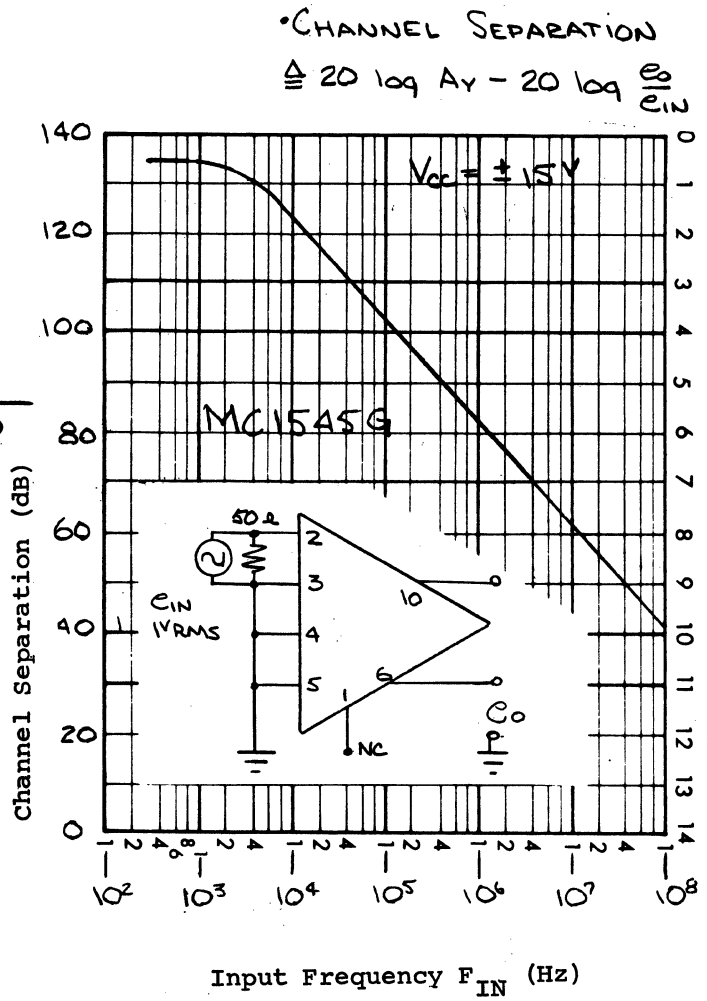


Figure 8.4. Channel separation vs. input frequency. Channel separation = 20 log A_V - 20 log (e_o / e_{in}).

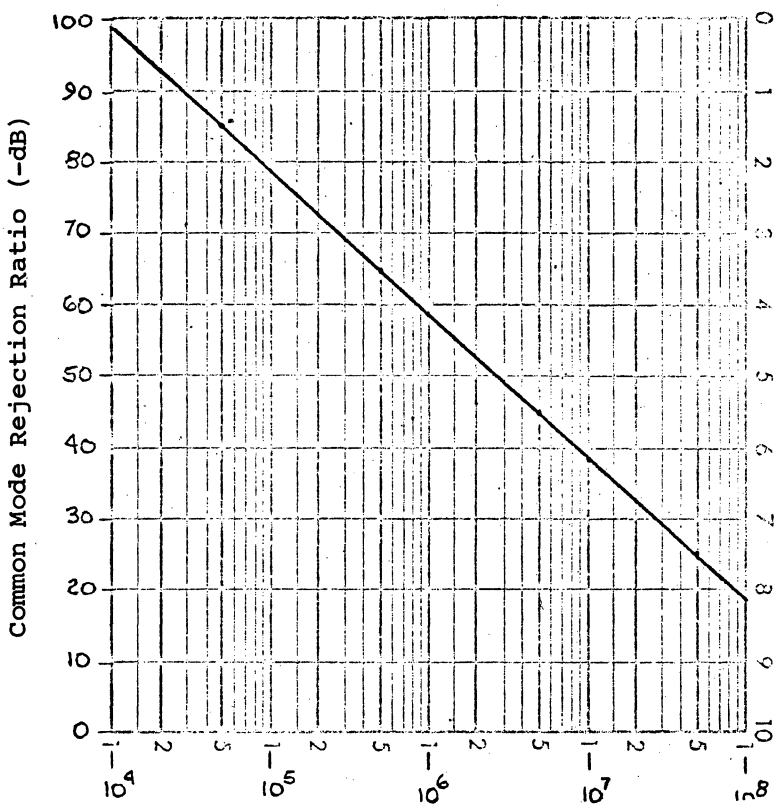


Figure 8.5. Common-mode rejection vs. frequency.

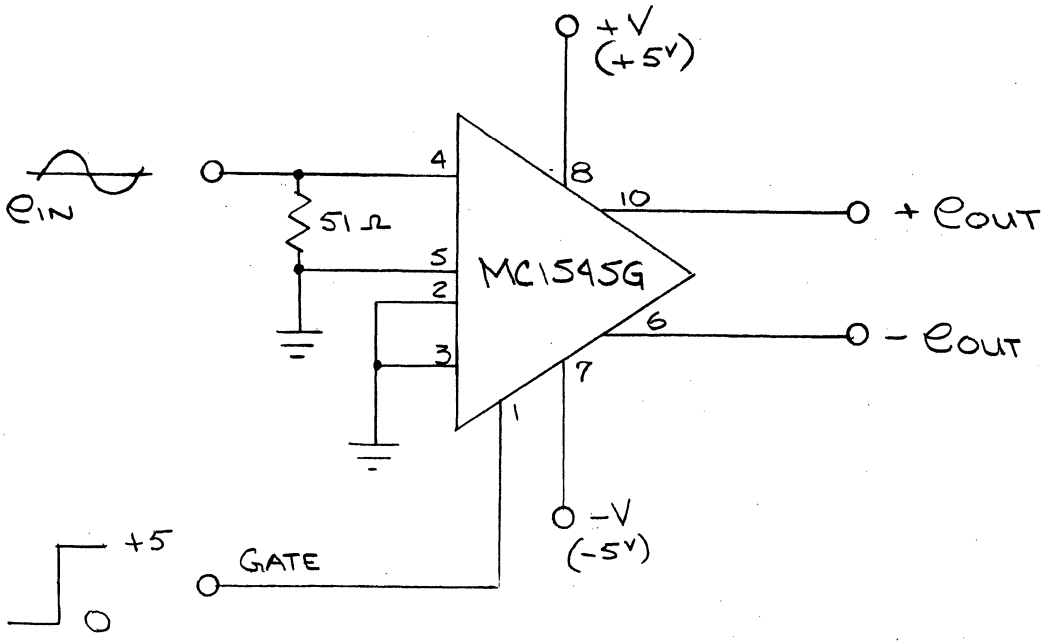


Figure 8.6. Video switch requires only one external resistor.

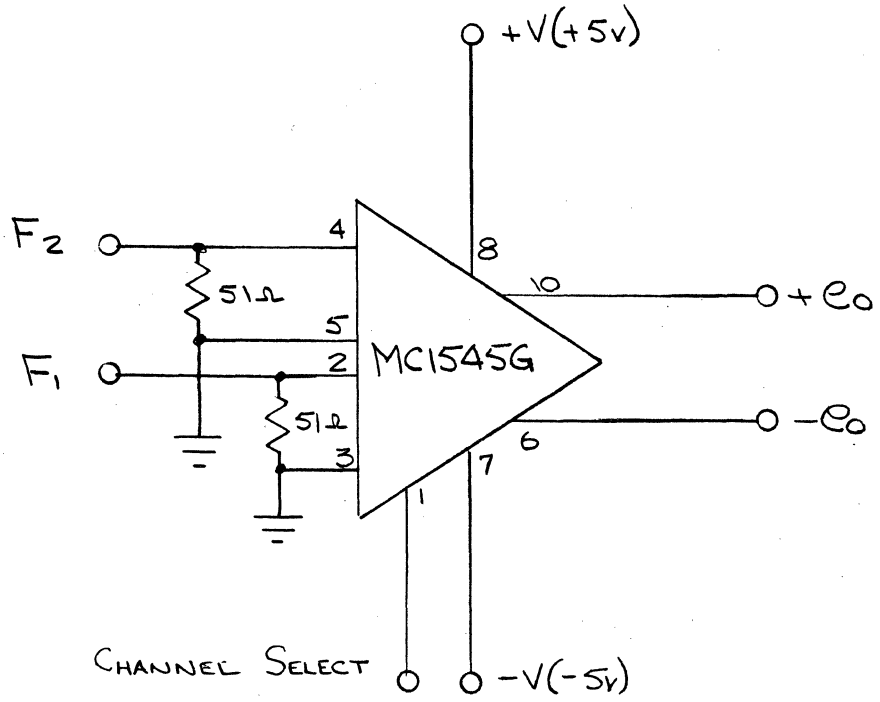
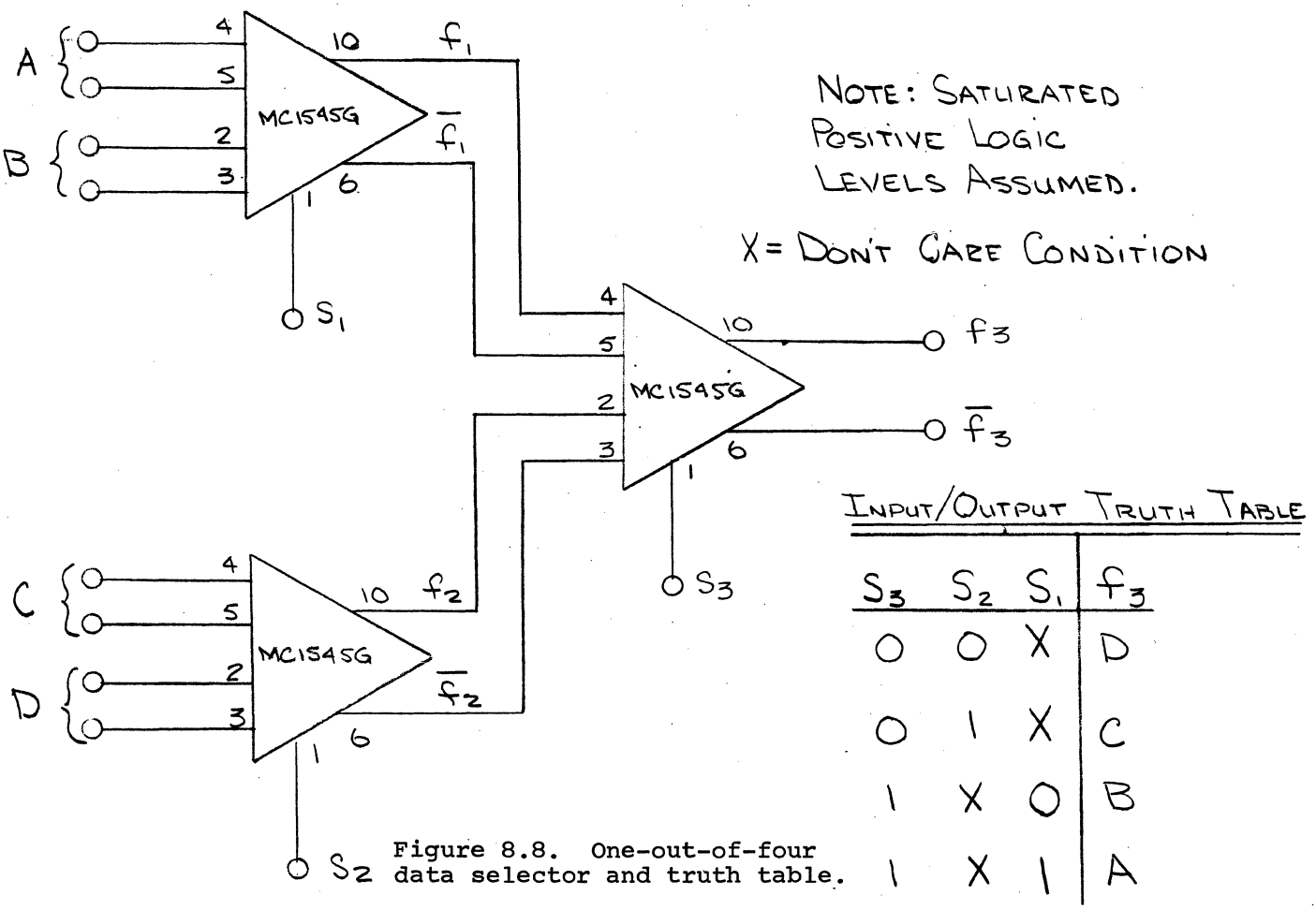


Figure 8.7. Multiplexer (frequency shift keyer).



INPUT/OUTPUT TRUTH TABLE

S_3	S_2	S_1	f_3
0	0	X	D
0	1	X	C
1	X	0	B
1	X	1	A

Figure 8.8. One-out-of-four data selector and truth table.

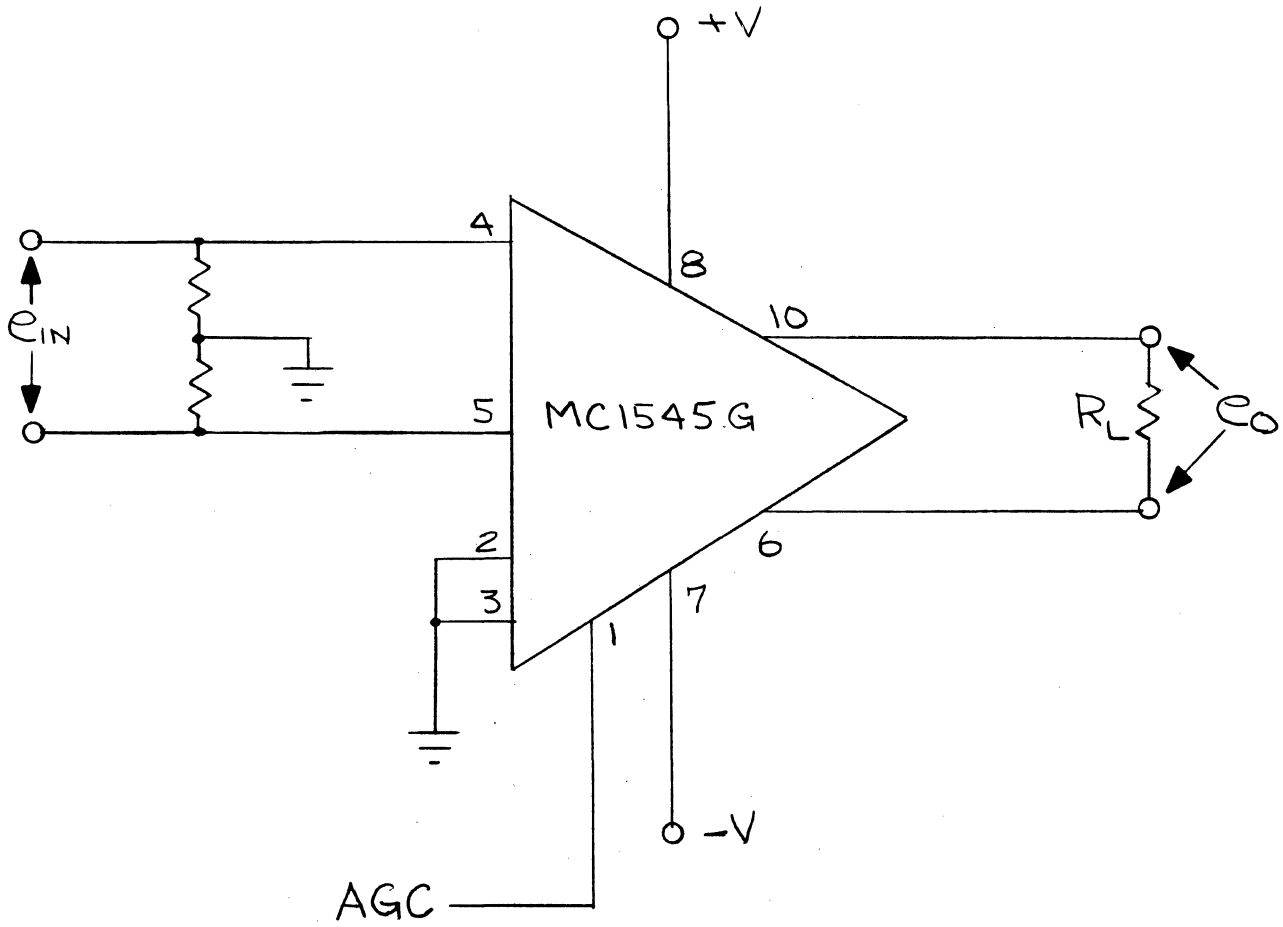


Figure 8.9. Wideband amplifier with AGC.

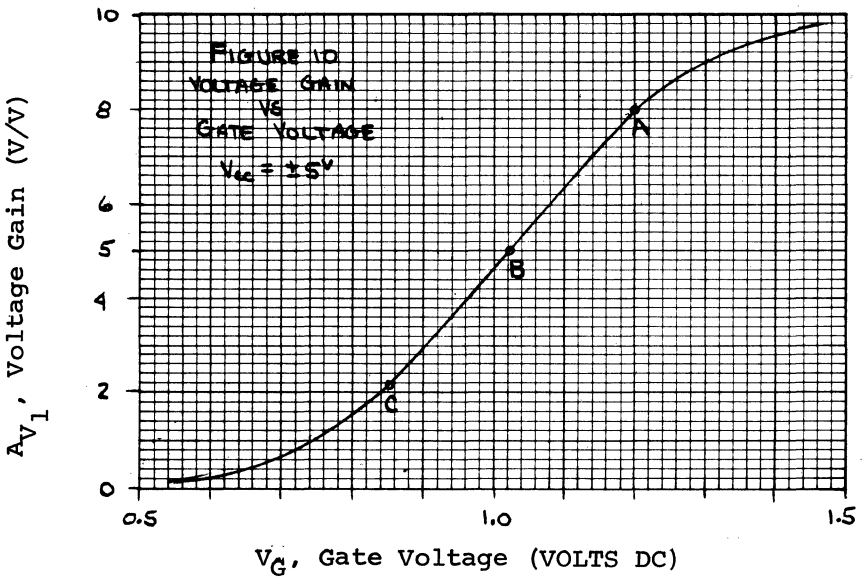


Figure 8.10. Gain of amplitude-modulator circuit varies linearly between points A and C.

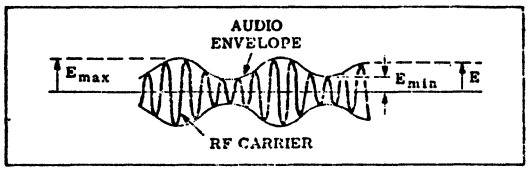


Figure 8.11. Amplitude-modulated waveform.

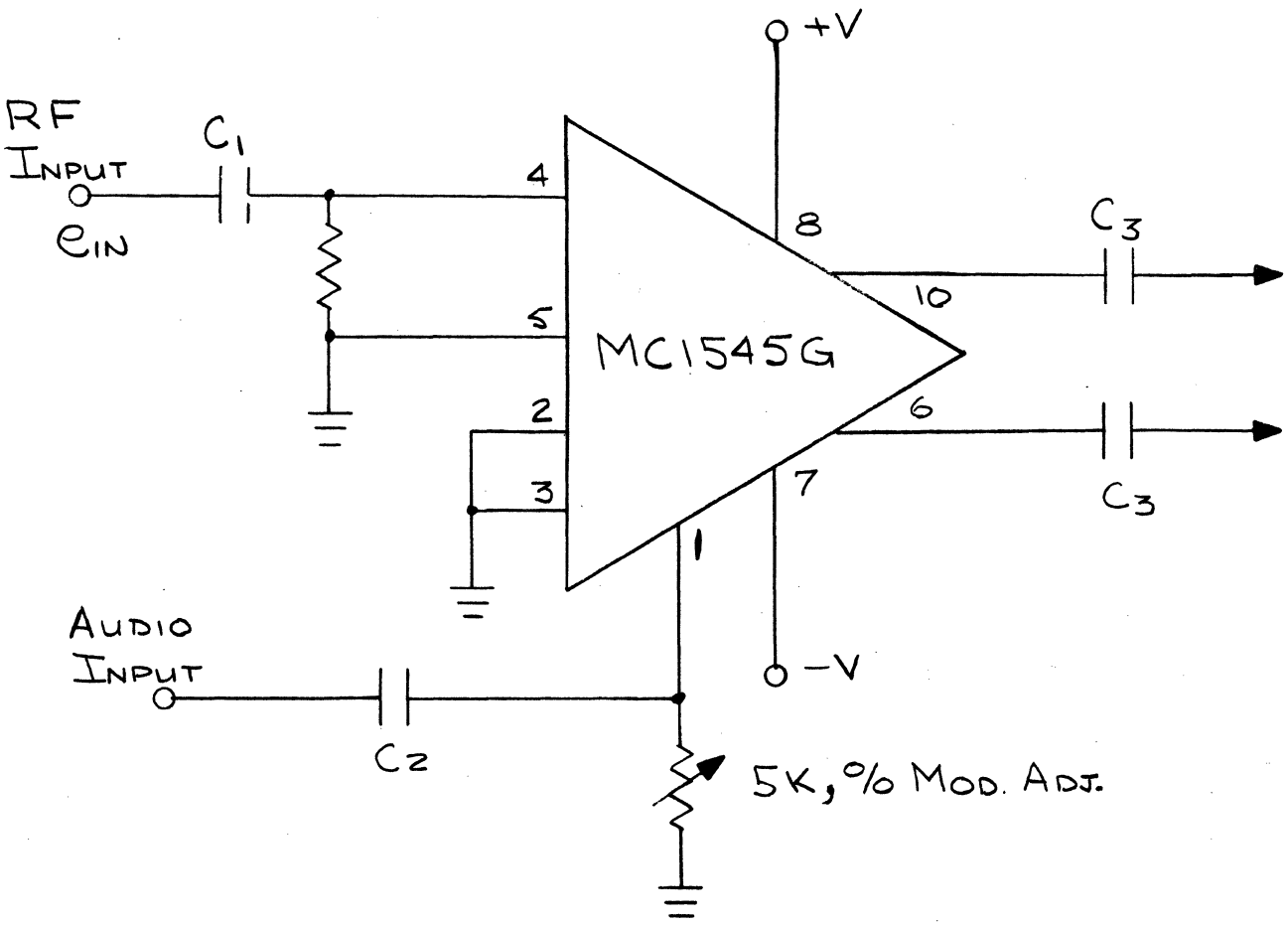


Figure 8.12. Amplitude modulator.

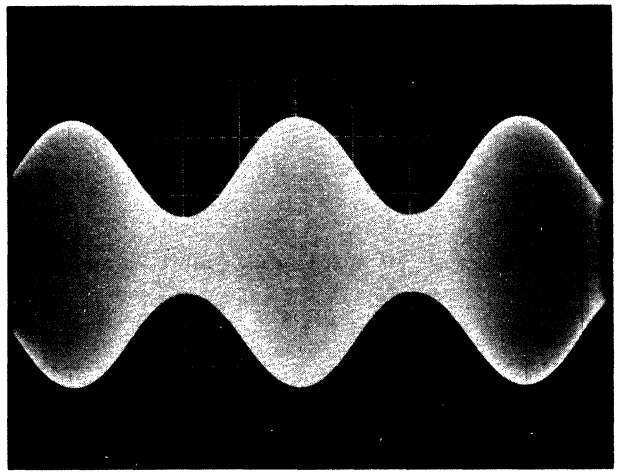


Figure 8.13. Output waveform for circuit in Figure 8.12 with 25 MHz rf signal and 5 kHz audio signal.

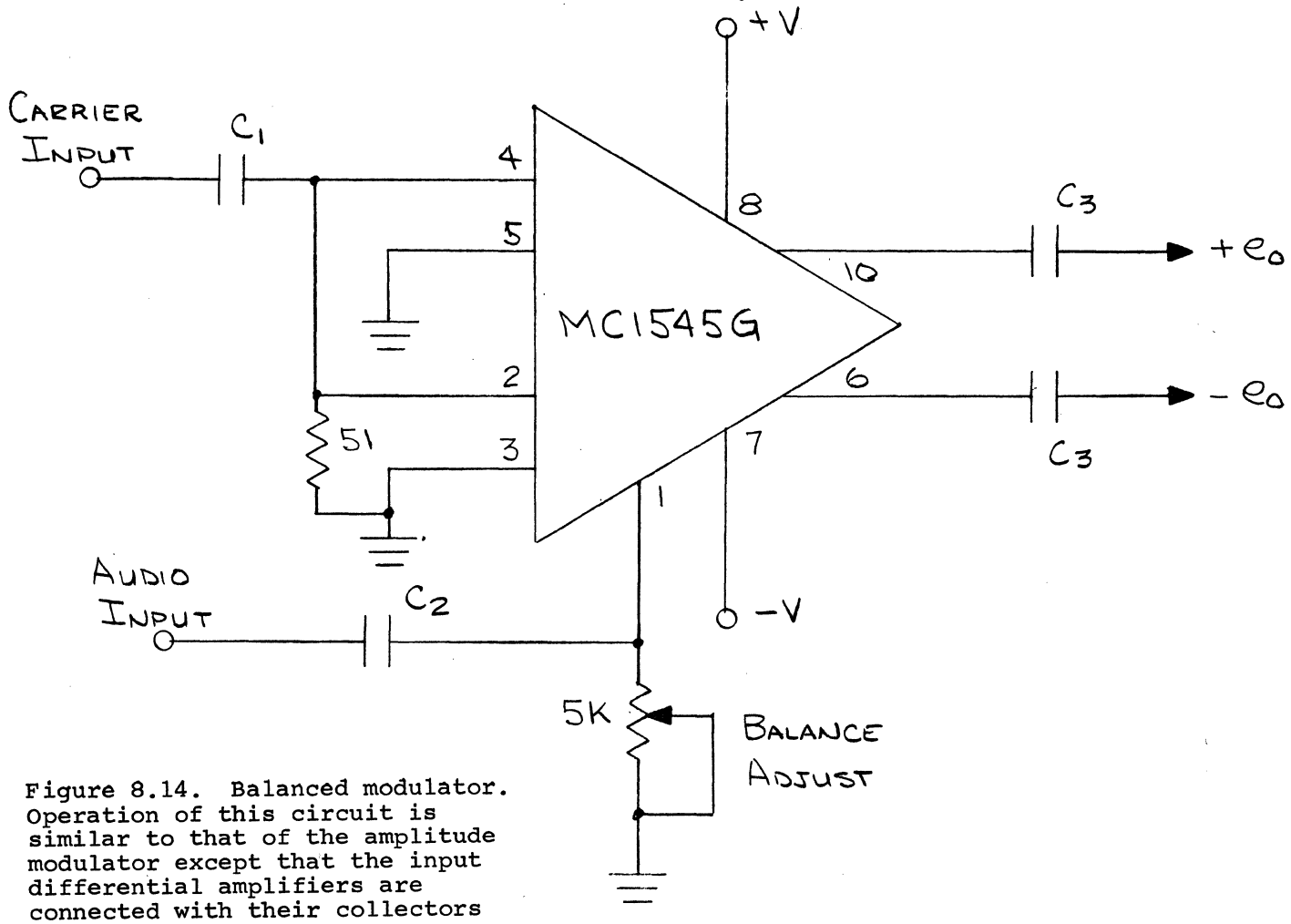


Figure 8.14. Balanced modulator. Operation of this circuit is similar to that of the amplitude modulator except that the input differential amplifiers are connected with their collectors cross coupled.

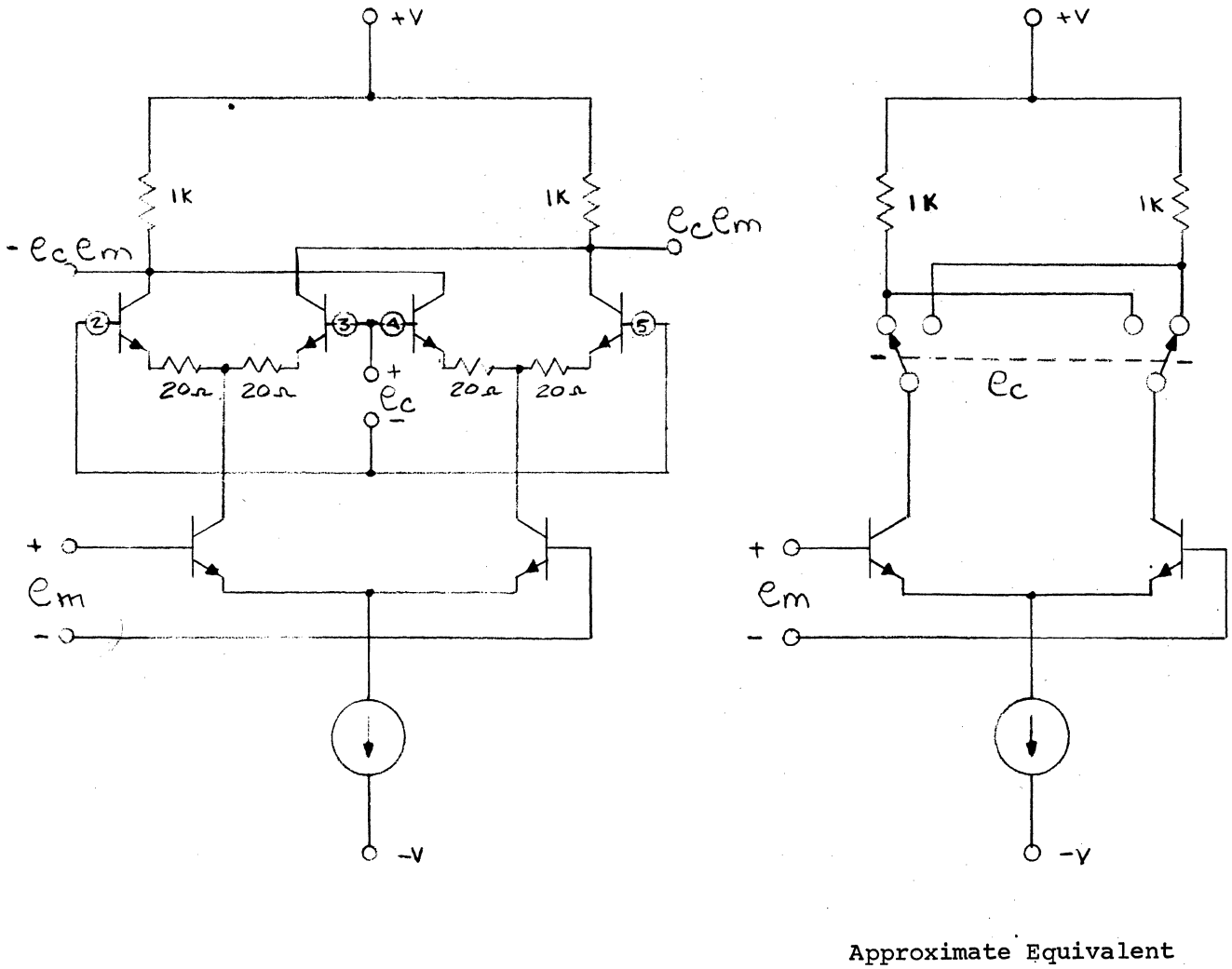
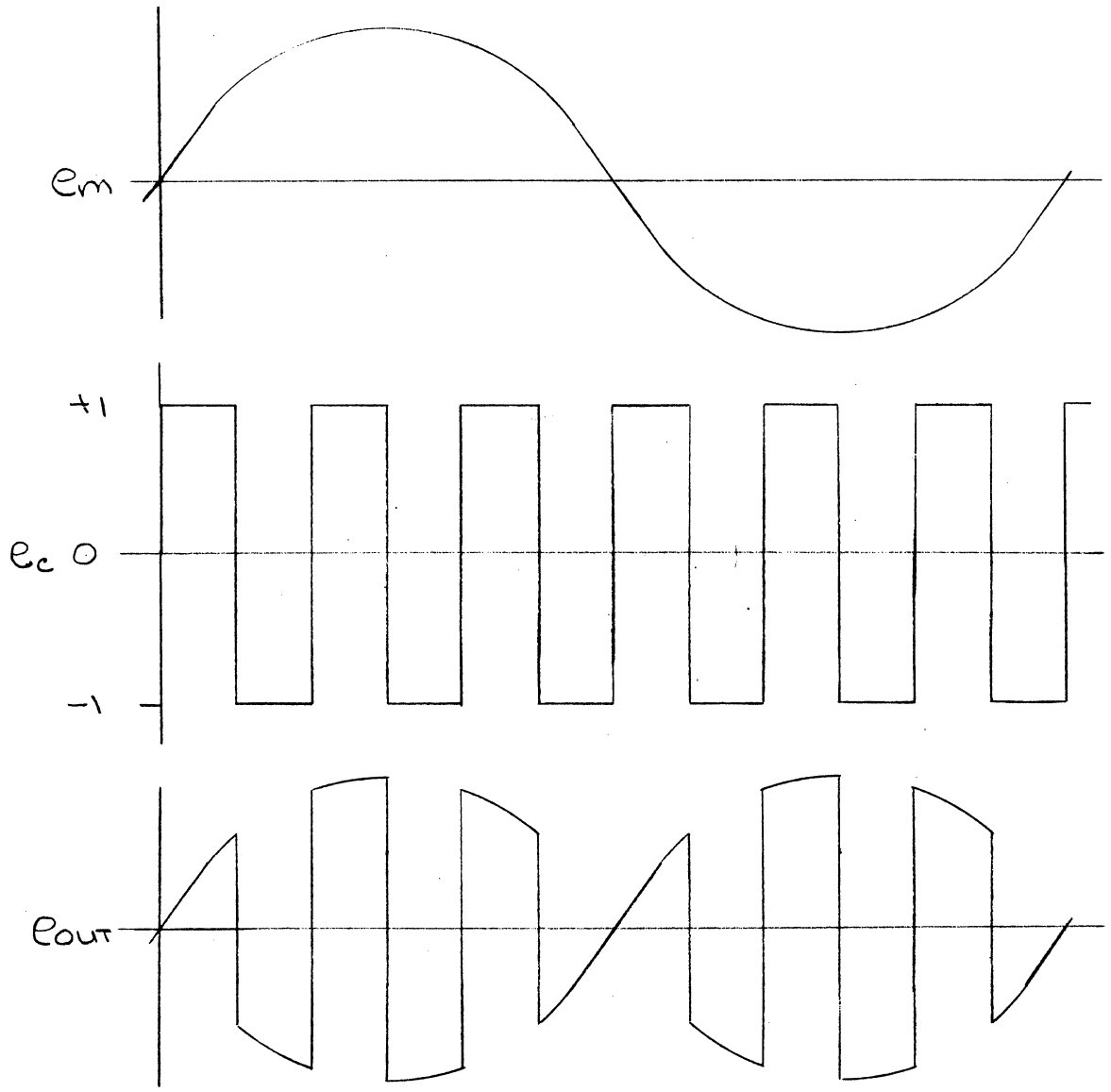


Figure 8.15. Balanced modulator model.



e_c = Switching Function S(t)

Figure 8.16. Balanced modulator waveforms.

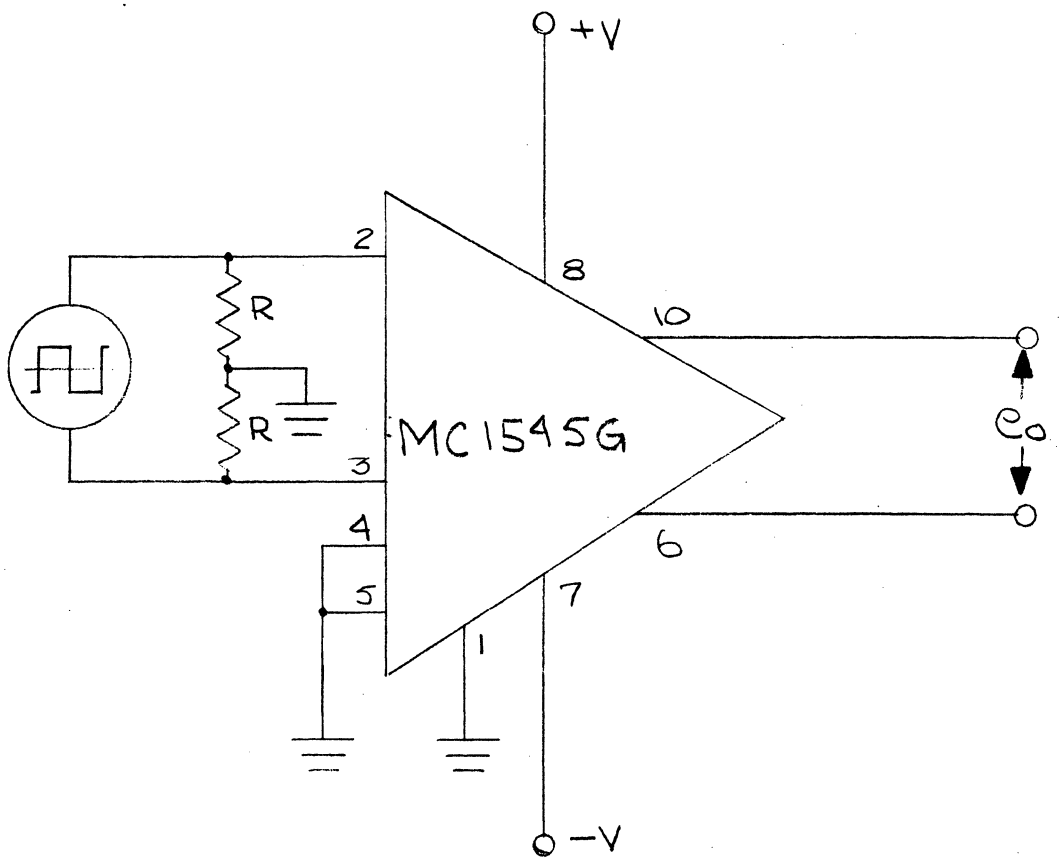


Figure 8.17. Pulse amplifier.

9

Applying Integrated Circuits To FM Detector Applications

by W. F. Allen, Jr.
and L. H. Hoke, Jr.
Philco-Ford Corp.

Economic considerations made it mandatory that integrated circuits be high-volume production items. For this reason, linear circuit activity to date has been dominated by operational amplifiers, comparators and, more recently, voltage regulators. Numerous other types of linear circuits have been developed, but because of the widely differing requirements of linear applications, none of these circuits has enjoyed the volume required for the manufacturer to sell them profitably at a low price.

Another circuit which has the potential of becoming a high-volume item is the limiter-detector portion of an fm receiver; commercial television and fm receivers, as well as military fm receivers, can use the circuit.

As has been the case in the implementation of other circuits in IC form, careful analysis of the application and environment is necessary to determine the particular detector which is to be used. Discrete-component fm detectors have relied extensively on specially designed transformers for their operation. In consumer products applications where size is not a consideration, this approach is acceptable. In military applications where miniaturization is essential, more suitable circuits are available which take advantage of the low cost of active components.

Because the economic factors involved in selecting ICs are rapidly changing, selection of the right IC for a particular application is no easy matter; a number of circuits are discussed in this chapter so that designers can weigh the variables which relate to their particular application.

9.1 INTEGRATED-CIRCUIT CONSIDERATIONS

When inductive elements are used in conjunction with integrated circuits, care must be exercised to insure against the generation of induced voltages more negative than the substrate.

A liability of p-n isolated integrated circuits is the device-substrate parasitic capacitance associated with diffused transistors, diodes and resistors. In the frequency range of interest, this parasitic capacitance is not usually a problem except in certain applications which require precise balance. The diodes which are available in p-n isolated IC's have, in addition to parasitic capacitance, parasitic diode and transistor action which must be taken into account. Voltage breakdown conditions must also be considered.

Three configurations used for monolithic integrated-circuit diodes are shown in Figure 9.1. The simple base-emitter structure of Figure 9.1A has a typical forward conduction voltage of approximately 0.7 V and a reverse breakdown voltage of about 6 V.

A second configuration, the base-collector diode shown in Figure 9.1B, displays a forward conduction voltage of approximately 0.7 V and reverse breakdown of 30 V or more depending upon the collector material. The isolation diode formed by the

collector-substrate junction becomes a critical factor with this configuration. A negative 0.7 V on the cathode terminal (collector) of the main diode causes the parasitic isolation diode to conduct. Forward biasing of the main diode at a potential above ground converts the entire device into a grounded-collector pnp structure. Such a configuration has about unity beta.

A third monolithic diode configuration is shown in Figure 9.1C. The collector and base of a transistor are used as the anode and the emitter as the cathode. This connection displays a higher perveance than the simple base-emitter diode described earlier. Reverse breakdown of the diode-connected transistor occurs at about 6 V. The isolation diode associated with this structure conducts when the anode of the main diode goes more negative than 0.7 V with respect to the substrate. This problem is avoided by using a large negative bias on the monolithic substrate.

9.2 FOSTER-SEELEY DISCRIMINATOR

The Foster-Seeley discriminator is a popular, often-used circuit (1,2). A representative diagram is shown in Figure 9.2. In the interest of component reduction, the high-frequency choke which in the classical design is usually included between the secondary winding center-tap and the diode load resistors has been eliminated. Consequently, the primary will be loaded more heavily.

The sensitivity of the Foster-Seeley discriminator has been given by Sturley (3):

$$S = \frac{dE}{d\Delta f} = \frac{2\, g_m\, e_g\, r_{D1}\, n_d}{fm} \qquad \frac{Q_2 \quad (E_2/E_1)}{(1 + Q_1\, Q_2\, k^2)\left[1 + 1/4\ (E_2/E_1)\right]^{1/2}} \tag{9.1}$$

where S is the static change in output voltage for a frequency off-set of ΔF, $g_m\, e_g$ is the current driven into the primary winding by the transistor preceding the discriminator; r_{D1} is the resonant impedance of the primary circuit; n_d is the diode conduction efficiency; Q_1 and Q_2 are the quality factors of the primary and secondary circuits, respectively; E_1 and E_2 are the primary and secondary voltages at the mid-frequency f_m; and K is the coupling coefficient. The value of K is obtained from:

$$K = \frac{M}{\sqrt{L_1\ L_2}}$$

The Foster-Seeley discriminator has several disadvantages when considering converting it to integrated circuit form. First, the double-tuned transformer is a bulky component which has no integrated equivalent. Second, the diode load resistors are limited in size to 10 to 20 kΩ, thereby causing a compromise in the discriminator design, especially for narrowband cases. Third, the diodes which are fabricated by monolithic p-n function isolation techniques can severely reduce the sensitivity of the discrimination by virtue of their low reverse breakdown characteristic and their parasitic elements. There are a number of variations of the Foster-Seeley discriminator, and several types of double-tuned-circuit slope detector discriminators which, as far as integrated components are concerned, have similar characteristics.

9.3 RATIO-DETECTOR

The ratio-detector circuit has several distinct features not found in the Foster-Seeley discriminator (4). First, and most important, is the use of a stabilizing capacitor or battery across the diode loads for the suppression of amplitude-modulation components in the output. This stabilizing component can be eliminated if the receiver system contains a limiter stage just ahead of the detector, which will normally be the case in IC designs. This approach is imperative from a miniaturization viewpoint.

A second modification, as can be seen by comparing Figure 9.3 with Figure 9.2, is that the diodes are reversed and the recovered audio is taken from a tertiary winding which is tightly coupled to the primary of the transformer. Diode load resistor values are generally selected to be much lower (about 5 kΩ to 10 kΩ) than for the Foster-Seeley discriminator circuit. These values are easier to fabricate in integrated monolithic circuits.

The sensitivity of the ratio-detector is one-half that given by the equation for the Foster-Seeley discriminator. In general, however, the design values for Q's, primary-secondary coupling, loads, etc., will differ greatly because of the different operating conditions.

In the ratio detector, as in the discriminator circuit, special attention must be given to the monolithic design. The problems from parasitics associated with the diodes, discussed earlier, are also of concern in the ratio detector circuit. In Figure 9.3, the anode of diode D_1 (collector-base node) must be biased at a voltage sufficiently positive with respect to the monolithic substrate to prevent the isolation diode from conducting. From a practical point, this means that either a relatively large negative voltage be placed on the substrate, or that the reference point for the secondary circuit be a virtual ground rather than actual ground.

A second problem associated with the reversed diode connection is that of capacitive unbalance. The isolation diode capacitance, in the range of several picofarads, exists between collector and ground, while the stray capacitance between emitter (cathode) and ground is at least an order of magnitude smaller. For diode D_1 of Figure 9.4, the parasitic capacitance is manifested from one side of the secondary winding to ground while for diode D_2 it is in parallel with the load filter capacitor. In monolithic circuit form, this situation is easily corrected by connecting an additional collector-isolation junction capacitor to the cathodes of both D_1 and D_2 as shown in Figure 9.4.

The substrate bias problem previously mentioned can be solved by rearranging the diodes and loads as shown in Figure 9.5. In this case, the recovered output voltage is referenced to ground, thereby providing an AFC source. In addition, base-collector junction diodes having reverse breakdown voltages of 30 V or more can be used thus leading to larger secondary voltage and high sensitivity. The grounded cathode (collector diffusion) of diode D_1 has no parasitic element. The parasitic diode associated with diode D_2 is in parallel and has the same polarity as D_2, thereby contributing to the perveance. To balance this, the area of diode D_1 can be increased slightly.

The performance of the ratio detector is very good, and in applications which can tolerate the transformer, the circuit should be considered.

9.4 COUNTER DETECTOR

The counter type detector demodulates an fm wave by counting the zero (or other fixed level) crossings of the wave. The demodulation is accomplished by generating a fixed area pulse for each zero crossing, and integrating the energy content of the pulses. The detection method is illustrated by the exaggerated fm wave of Figure 9.6 which shows the generated pulses corresponding to the positive-going zero crossings. The resulting pulses are integrated by an RC filter whose output is the recovered information. The sensitivity of the system is determined as follows:

First, consider that the pulse is "on" Y % of the period of the carrier frequency. If the frequency is increased to the point where the pulse is always on, the output of the integrator is AV_{in}, where A is a constant of the integrator; V_{in} is defined in Figure 9.6. At the carrier frequency, the output is YAV_{in}. As the frequency of the input decreases to zero, the output of the integrator also goes to zero. Therefore, the discriminator sensitivity (%) is:

$$S = \frac{YAV_{in}}{100\ f_m} \tag{9.2}$$

where f_m is the carrier center frequency. The discriminator curve is shown in Figure 9.7.

Equation 9.2 points out that the sensitivity is related inversely to the carrier frequency, and directly to the generated pulse width. Obviously, sensitivity is directly related to the integrator efficiency. Equation 9.2 also shows that a system with a predetermined output frequency should be operated with the widest possible pulse consistent with the period of the highest frequency expected. At 11.5 MHz, the period is 87 ns. Since an actual generated pulse will not be perfectly rectangular, it is desirable to provide a safety factor in determining the largest pulse width which can be safely used. Why conversion to a lower frequency is desirable is immediately apparent.

As an example, let A = 1, Y = 50 %, V_{in} = 5.75, and f_o = 11.5 MHz. Then S = 0.25 mV/kHz. Converting to 455 kHz, and using the same conditions as above, the sensitivity is improved by a factor of 25, giving a sensitivity of 6.25 mV/kHz.

A considerable number of circuits can be used as counter detectors. Blocking oscillators, delay lines, multivibrators, charge storage devices, and saturated inductors are a few. A counter detector which uses a monostable multivibrator is shown in Figure 9.8. One feature of this circuit is that its output pulse can be maintained "on" over the majority of the period, giving the maximum sensitivity obtainable at the operating frequency and the available supply voltage. The circuit is completely integrable.

A similar circuit shown in Figure 9.9 uses a NAND gate and a delay line (6). The time-delay device can be a transistor or another NAND gate. In this circuit, a

pulse whose output equals the supply voltage and whose duration equals the delay line time delay occurs for every negative excursion of the fm signal, so the filtered output represents the recovered audio signal.

A circuit which uses a charge storage principal (7,8) is shown in Figure 9.10. A type PA7703 monolithic amplifier is used as a limiter. When the limiter output stage is cut off, C charges through D_1 to V_{cc}, with the diode end of C being negative. During this time, D_2 is reverse biased, and does not conduct. During that part of the cycle when the collector potential of the limitier swings toward its lowest value, capacitor C discharges through diode D_2 in series with its load R_o; thus, one current pulse flows through the load R_o of diode D_2 for each cycle of operation.

The total charge acquired by capacitor C during each cycle is $C(Vcc - V_D)$. The portion of this total charge which passes through diode Q_2 and R_o once each cycle is equal to $C(Vcc - Vc_{min} - 2 V_D)$ where Vc_{min} is the most negative excursion of the limiter output. As long as Vcc and Vc_{min} remain constant, and the time constants of the charge and discharge circuits are sufficiently small compared to the period of the input signal, the total quantity of current which flows through R_o in each cycle is constant, and the average value of current through R_o is dependent on the repetition rate of the input signal.

The sensitivity of the circuit in Figure 9.10 can be computed on the basis of a discharging capacitor having a current equal to a pulse of peak value V and a pulse duration equal to one time constant. If five time-constants are allowed for the complete discharge of the capacitor and an equal amount of time for charging the capacitor, then Y in equation 9.2 is 10 %, and the sensitivity is:

$$S = \frac{AV_{in}}{10\ f_m} \tag{9.3}$$

where

$$V_{in} = (Vcc - Vc_{min} - 2V_{BE}) \left(\frac{R_o}{R_L + R_o} \right)$$

Equation 9.3 shows that the sensitivity of the charge transfer counter detector is less than that of the previously mentioned monostable multivibrator circuit.

The counter-detector circuit has several problem areas. First, it's sensitivity is a function of Vcc and V_D. Therefore, the power supply must be well regulated.

Variations with temperature of the components, especially of the diodes, can significantly affect the circuit operation. To minimize such effects, the capacitor should be charged to much greater than 0.7 V. Internal voltage regulators can be used to minimize the effects of power-supply variations. In addition, the value of capacitor C (in conjunction with other inherent circuit capacitances) is determined by the maximum permissible time constants in the charge and discharge circuits. A practical viewpoint is that the voltage across the capacitor should rise to greater than 99 % of V_{cc} during one half of the cycle, and fall to within 99% of the minimum value during the next half cycle. This is a severe limitation on the frequency

sensitivity of this circuit. Also, the af filter must be designed so that it does not bias D_2. This is the reason for the inductor in Figure 9.10. A circuit which does not require an inductor is given in Figure 9.11.

In the circuit of Figure 9.11, transistor Q_1 has its base connected to the output and controls the amount of charge transferred by capacitor C_1, resulting in a linear detector characteristic. In addition to the previous considerations concerning the time constant of the charging path, the output filter capacitor C_2 must be much larger than C_1, and R_o must be much smaller than the reactance of C_1 at the carrier frequency. The tapped resistor at the limiter output slows the charging rate of Q_1 to prevent switching spikes.

The charge-storage detector derivation has assumed a square-wave output from the limiter. This allows the capacitor to fully charge and fully discharge. Some deviation from a square wave is tolerable since charge will alternately be stored and transferred, but a sine-wave input to the detector is intolerable, since the capacitor begins discharging the moment it is fully charged, and the frequency of the input wave then influences the amount of charge stored.

9.5 RC PHASE SHIFT DISCRIMINATOR

The RC phase-shift discriminator is similar in operation to the conventional Foster-Seeley discriminator. Both circuits rely on a phase shift network to sense the change in frequency of the fm signal: the Foster-Seeley circuit uses a double-tuned transformer for this sensing, whereas the RC phase shift discriminator uses an RC network.

An RC phase-shift discriminator we have investigated is shown in Figure 9.12. This circuit can best be analyzed by considering it in three functional parts: 1) a phase-shift network, 2) a phase-splitter network, and 3) a detector network. The output of the phase-shift network is the signal shifted in phase 90° at carrier center frequency, greater than 90° at a frequency higher than center frequency, and less than 90° at a frequency lower than center frequency. Inspection of the transfer function (9) given by:

$$\frac{V_o}{V_1} = \exp(2j \arctan RC\omega) \tag{9.4}$$

shows that R and C must be chosen to satisfy the relation $\omega_o = 1/RC$ where ω_o is the carrier radian center frequency. Note that the amplitude of the transfer function is constant. The output of the phase-shift network is fed to a differential amplifier which functions as an amplifier and phase splitter, with its outputs always 180° out of phase and varying as the carrier frequency varies. The phase conditions at the output of the phase splitter are analogous to those present in a Foster-Seeley discriminator, and are likewise compared to the input signal across the detector network. The discriminator phase conditions are graphically illustrated in Figure 9.13.

Although the phase relationships in the RC phase-shift discriminator are similar to

those in the Foster-Seeley discriminator, inspection of the transfer function shows that the resistor-capacitor phase shift network has unity "Q" factor. Therefore, low sensitivity and a large linear discriminator range would be expected. This was confirmed in a breadboard layout of the circuit of Figure 9.12, which has a sensitivity of 0.4 mV/kHz, at 11.5 MHz. Because of the large peak-to-peak separation, the circuit alignment is not critical.

More elaborate phase-shift networks could be used to give higher sensitivity, but the added complexity would make the circuit more critical, probably to the point of requiring external components for tuning. Since attenuation is inherent in the phase shift of an RC network, an additional gain stage would be required either in the phase-shift network or in the phase splitter. This added complexity negates the advantages of the phase-shift discriminator, and the simpler circuit of Figure 9.12 appears to offer more promise in the wideband, high deviation systems.

A different approach to RC fm discriminators has been given by Lemke (10). His technique uses two distributed RC null networks with null frequencies situated on either side of the carrier input. The output from the distributed RC networks are then rectified and subtracted. Amplifiers are used to boost the output of the RC network prior to rectification. Lemke's work was done using thin-film techniques, but the principal can be extended to monolithic form. The most obvious problem is that of adjusting the center frequency point of the discriminator curves.

9.6 QUADRATURE DETECTOR

The quadrature detector uses a phase detecting principle to recover information from an fm signal. The incoming fm signal is applied directly to one port of a phase detector, and through a phase sensitive network to the second port. Several types of quadrature detector circuits have been developed (11-14), the simplest requiring but a single transistor stage. A simple circuit which illustrates quadrature detector operation is shown in Figure 9.14. The circuit was described by Sziklai (11).

The circuit makes use of the condition that the transistor emitter-to-collector path is essentially an open circuit when the base is negative relative to the emitter, and a short circuit when the base is positive relative to the emitter. The transformer secondary is tuned to the carrier frequency. At center frequency, the secondary voltage is 90° out of phase with the primary. As the signal frequency is changed, the secondary voltage lags the primary voltage by an angle less than 90° if the signal frequency is increased; and lags by an angle more than 90° if the frequency is decreased. Therefore, the amount of time that the base is positive with respect to the emitter is directly related to the incoming signal frequency, and the voltage developed across the load varies accordingly. This detector has the advantage of simplicity. However, it has poor sensitivity, and does not operate well at higher frequencies, because the emitter-base junction is heavily saturated during the "on" period, causing signal distortion. For this reason the circuit is not often used. These operational deficiencies can be largely eliminated by extending the principle of operation to emitter-coupled circuits.

Before discussing quadrature detectors which use emitter-coupled transistors, we'll review the operation of a simple emitter-coupled amplifier.

In Figure 9.15, for balanced conditions, since $R_1 = R_2$, and Q_1 and Q_2 are matched, the currents through the two transistors are equal under no-signal conditions. If a positive voltage of sufficient magnitude is introduced at the base of Q_1, it turns "on" and a current of amount I flows through Q_1. Q_2 is turned "off". A negative voltage of the same magnitude at the base of Q_1 has the opposite effect, causing a current of magnitude I to flow through Q_2 and R_L. The resulting output voltage is also shown in Figure 9.15. The desirable feature is that the stage is current limited and so is not driven into heavy saturation with large amplitude signals.

The operating characteristics of the emitter-coupled pair are used to make a slightly different quadrature detector as shown in Figure 9.16. Again, a transformer could be used to obtain the 90° phase shift; however, a different scheme is used to achieve this function in microminiature form. In this circuit, C_1 is made large and couples the input signal into Q_1 without phase shift. C_2 is selected so that its reactance is large compared with the tuned circuit impedance of C_3L at resonance. With this choice of values; the signal frequency is shifted 90° by C_2 at resonance. There is no phase shift produced by the tuned circuit at resonance. As the fm signal deviates from the resonant frequency, the phase shift across C_2 remains a constant 90°, whereas the phase varies across the tuned circuit. This phase variation, when properly applied to an emitter-coupled amplifier, results in quadrature detector operation. This is graphically illustrated in Figure 9.16. Examination shows that for a phase shift of "B" with respect to "A", the pulse width of the output signal will be directly proportional to the time coincidence of the negative portions of the two input signals. The output pulse width is therefore directly related to the variation of the input signal about the carrier frequency.

The circuit of Figure 9.16 is satisfactory and in discrete component form would probably offer the best, more economical approach to a transistor quadrature detector. There is some interaction of the two inputs at the base of Q_1; however, this can be eliminated by using an additional transistor in an emitter-coupled triplet configuration (15) as shown in Figure 9.17. The operation of this circuit is similar to the operation previously described except for the isolation of the inputs with a transistor. The isolation resistors, R_1 and R_2, are made smaller in value for the circuit of Figure 9.17. Consequently, there is better isolation with less signal attenuation, and the space required for the transistor on the integrated circuit chip is offset by the decreased space required by the resistors R_1 and R_2

The sensitivity of this type circuit for a simple tuned-circuit phase shift network is given by

$$S = \frac{R_L I_1 \left(\frac{\phi}{360}\right)}{\tan \phi \frac{(f_\phi)}{2Q}} \quad V/Hz \qquad (9.5)$$

where ϕ = Phase shift across tuned circuit at a particular frequency, F_o = Carrier frequency, Q = Phase-shift tuned-circuit Q loaded, R_L = Collector load resistor, and I_1 = Total available output current.

The Q of the phase-shift network is adjusted to provide a linear phase shift over the information bandwidth, with approximately 0.32% deviation from linearity occurring at 6% phase shift, and 1% occurring at 10% phase shift.

With the exception of the tuned circuit C_3L, the quadrature detector can be integrated, and the integrated component values are not critical. The most important requirement for operation is that the resonant frequency of the tuned circuit not be influenced by the input signal level or by ambient conditions. The most practical way of accomplishing this is to swamp the circuit capacitance with a large capacitor, which thereby requires a small value inductor for resonance. For instance, if a 600-pF capacitor is used, the required inductor is approximately 0.4 μH at 11.5 MHz. Compatible microminiature components with these values are avilable.

This type of circuit should find widespread use since all of the components are readily integrated except for the tuned circuit which can be implemented with simple microminiature parts. In addition, the circuit has acceptable sensitivity and is easily tuned.

9.7 CRYSTAL DISCRIMINATOR

Crystal discriminators provide good performance and can be purchased to complement the crystal filter preselector of systems which use them. However, the filters are voluminous, and in some respects defeat the purpose of microminiaturization.

The crystal discriminator circuit of Figure 9.18 has been investigated (16). The electrical characteristics of this circuit are excellent. The circuit requires three nonintegrable components, an inductor, a variable capacitor, and a series resonant crystal. By using ultraminature components and thin-film techniques, this circuit has been assembled in a TO-5 package. The resistors, capacitors and diodes are integrable, and could readily be fabricated in monolithic form.

9.8 APPLICATIONS

Two examples can illustrate the application of the ratio detector and the quadrature detector. Figure 9.19 shows the diagram of the Philco-Ford CP1053, which contains a limiter, a ratio detector, and audio preamplifier. A photomicrograph of the chip which measures 44 by 40 mils is shown in Figure 9.20. The circuit was designed specifically for application in consumer television and fm receivers. Pertinent specifications include: intermediate-frequency gain, 76 dB at 4.5 MHz, 57 dB at 10.7 MHz; limiting threshold, 500 μV at 4.5 MHz, 1.6 mV at 10.7 MHz; recovered audio (25 kHz deviation) -- 120 mV rms, (75 KHz deviation) -- 360 mV rms, power dissipation, 80 mW.

For this application, the ratio detector was selected because it provided an excellent AFC reference which is necessary in high-quality fm receivers. The linearity, bandwidth and sensitivity are comparable with existing systems, thereby making the conversion from current transistor practice to IC's rather straight forward. The physical size of the transformer required by this approach is not

prohibitive in the consumer industry.

A second example is shown in Figure 9.21. This circuit was developed for a military application. It contains two emitter-coupled limiter stages which are internally capacitively coupled, a quadrature detector, and two balanced diodes which can alternately be used in a ratio detector. A photomicrograph of the IC chip is shown in Figure 9.22. Parasitic capacitance compensation, as shown in Figure 9.4, is included. The quadrature detector shown in Figure 9.17 was used in this case primarily because microminiaturization was a system objective. The counter and RC discriminators were not used because of their low sensitivity. Circuit specifications include: intermediate-frequency gain at 11.5 MHz, 25 dB; recovered audio (8 kHz deviation), 80 mV p-p; power dissipation 63 mW. The rather low limiter gain of this circuit is due to the system partitioning which resulted in 50 dB limiter gain on a previous circuit in the system.

9.10 CONCLUSIONS

Several fm demodulator circuits have been discussed in terms of their capability to be integrated and their operation when fabricated in p-n junction isolated monolithic circuit form. The object has been to examine the circuit capability, the size considerations, and the economic factors associated with circuits commonly used in discrete-component designs and those which can be fabricated in monolithic form.

There is no one optimum choice for a demodulator but satisfactory choice for many applications are available in integrated circuit form. This was illustrated by the two applications described earlier. Both circuits have potential for high-production volume. It should be further noted that systems haveing low i-f levels (approximately 1 MHz) can use the counter detector to advantage and thus employ a completely integrated circuit.

ACKNOWLEDGEMENTS

Some of the work described was sponsored by USAECOM Contract No. DAABO 7-67-C-0406. Russell Gilson and Andrew Saldutti of USAECOM offered many valuable suggestions.

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FIGURES

Figure 9.1. Types of monolithic diodes, their structure and associated parasitics: (A) Base-Emitter, (B) Base-Collector, (C) Diode Connected Transistor.

Figure 9.2. Foster-Seeley discriminator.

Figure 9.3. Ratio detector.

Figure 9.4. Ratio detector with diodes to compensate parasitic capacitance.

Figure 9.5. Modified ratio detector with AFC reference.

Figure 9.6. FM signal and resulting pulses for pulse counter detector.

Figure 9.7. Counter detector frequency to dc characteristic.

Figure 9.8. Multivibrator counter detector.

Figure 9.9. NAND gate counter detector.

Figure 9.10. Charge transfer pulse counting detector.

Figure 9.11. Charge transfer pulse counting detector with simplified filtering.

Figure 9.12. RC phase shift discriminator.

Figure 9.13. RC phase shift discriminator phase relations.

Figure 9.14. Single-transistor quadrature detector.

Figure 9.15. Emitter-coupled amplifier.

Figure 9.16. Emitter-coupled quadrature detector circuit.

Figure 9.17. Emitter-coupled triplet quadrature detector.

Figure 9.18. Crystal discriminator circuit.

Figure 9.19. Schematic diagram of CP1053.

Figure 9.20. Photomicrograph of CP1053.

Figure 9.21. Schematic diagram of CP1058.

Figure 9.22. Photomicrograph of CP1058.

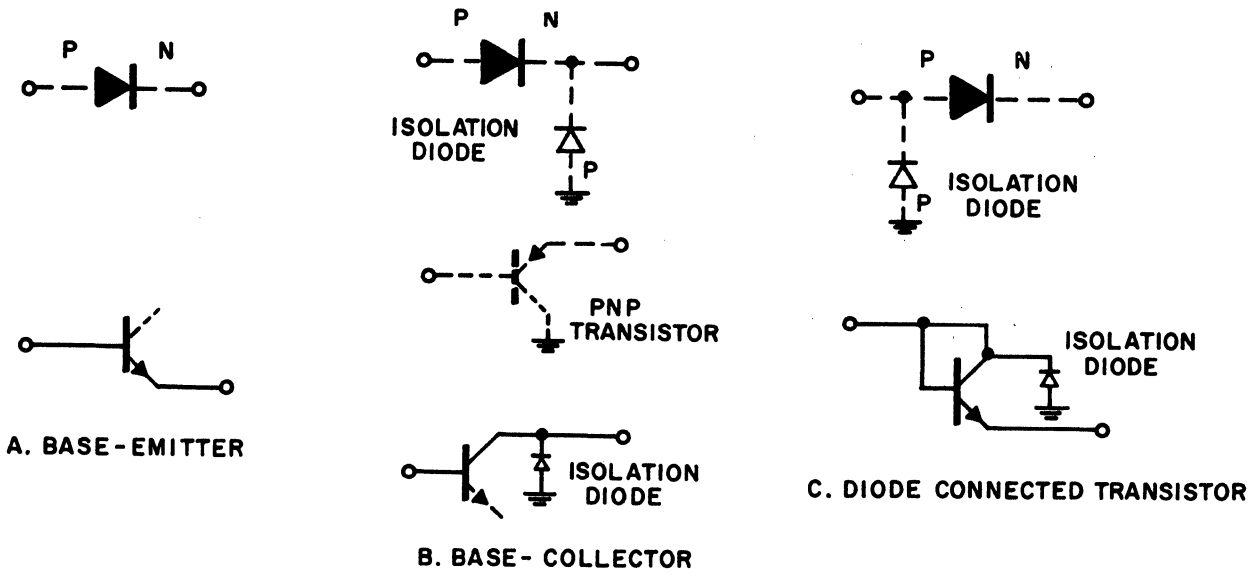


Figure 9.1. Types of monolithic diodes, their structure and associated parasitics.

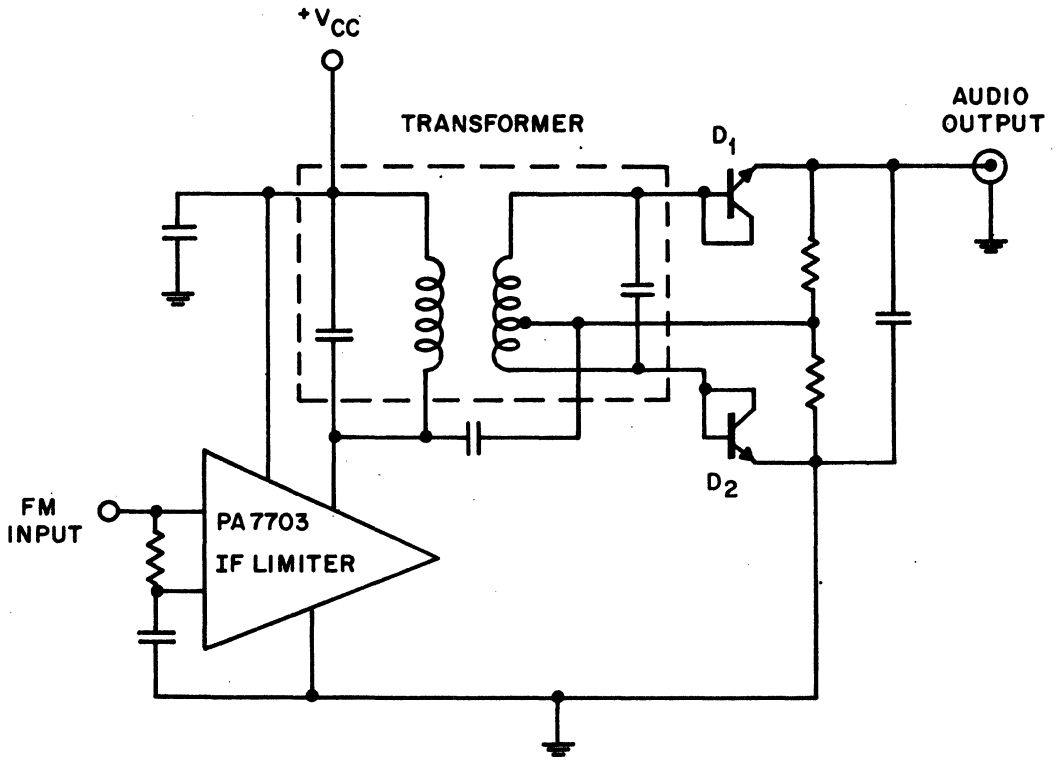
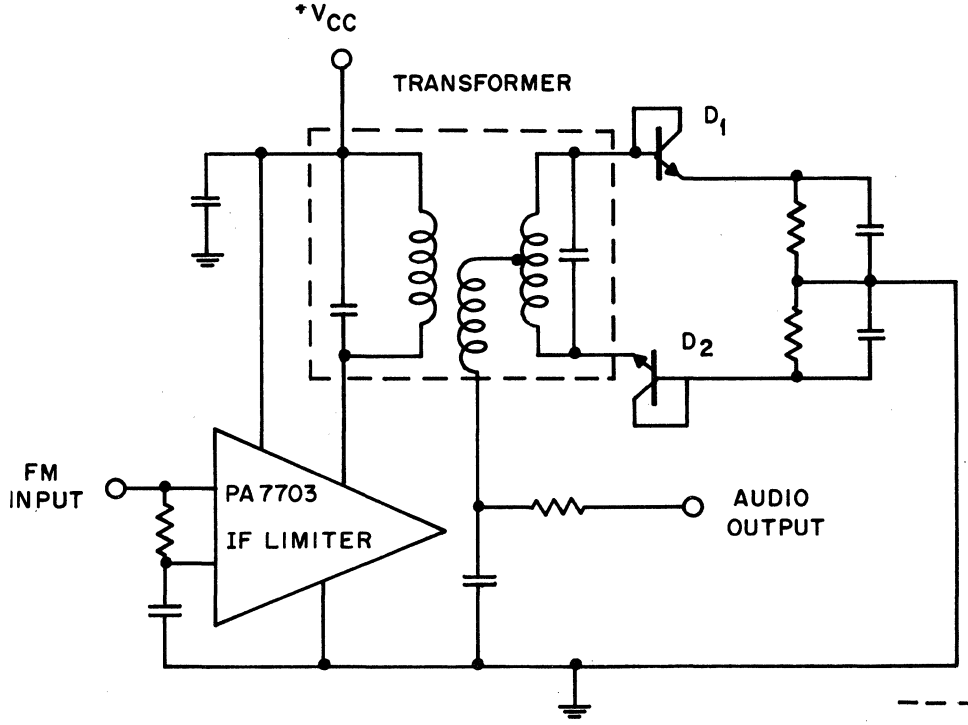


Figure 9.2. Foster-Seeley discriminator.



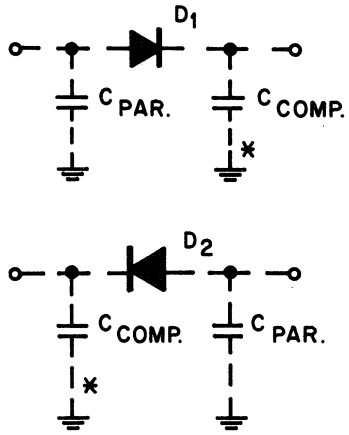


Figure 9.3. Ratio detector.

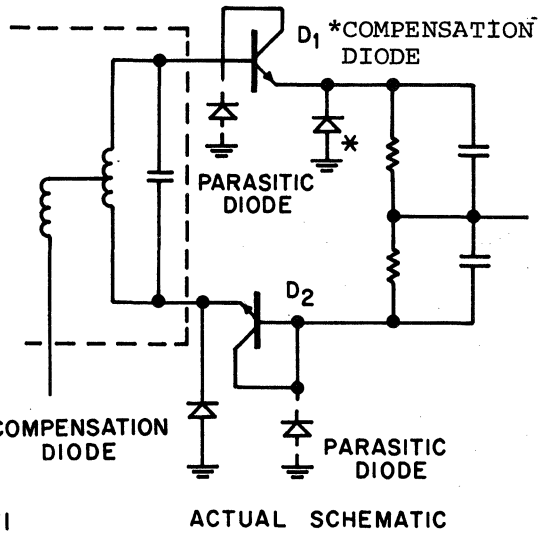


Figure 9.4. Ratio detector with diodes to compensate parasitic capacitance.

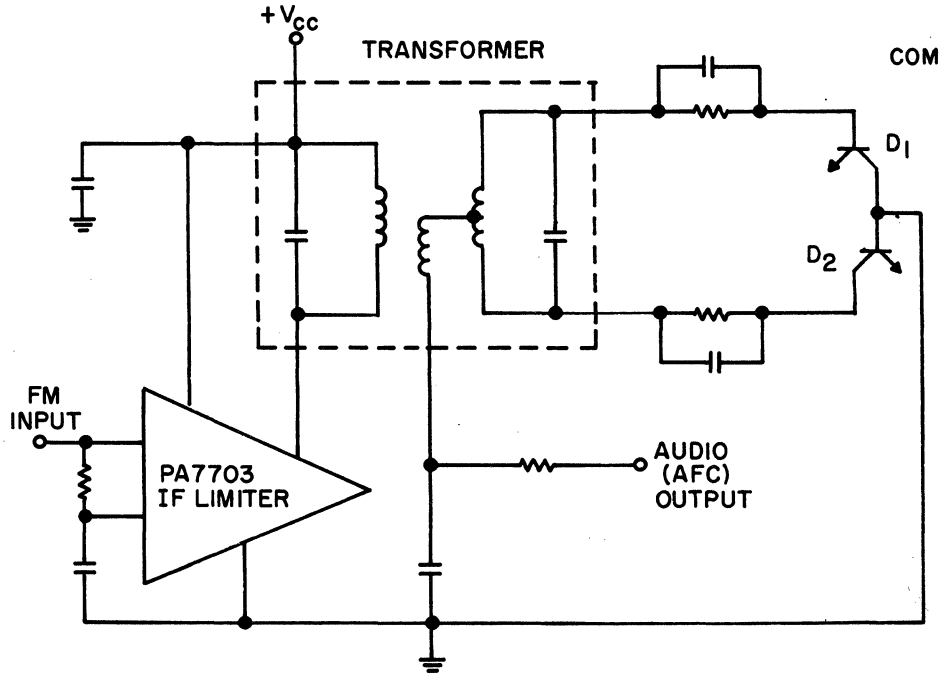


Figure 9.5. Modified ratio detector with AFC reference.

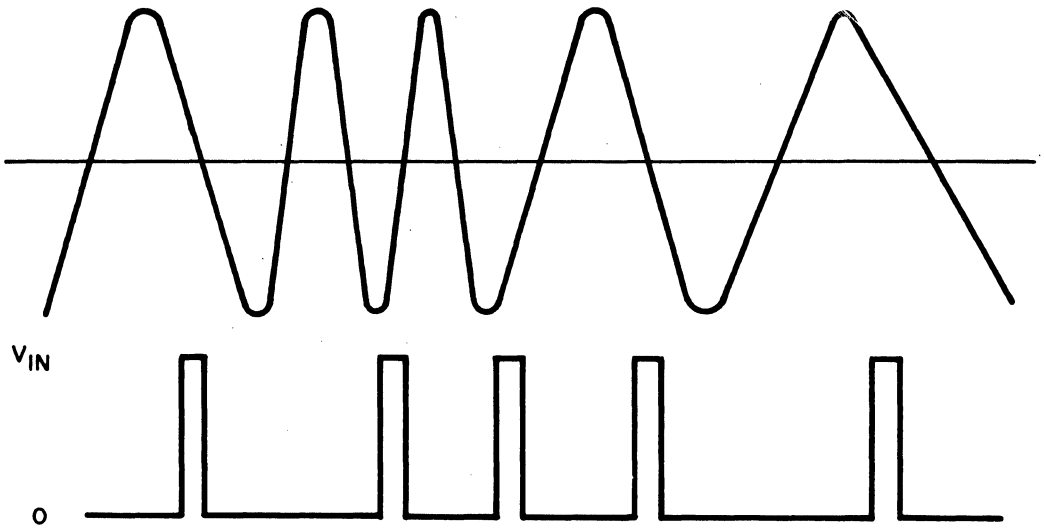


Figure 9.6. FM signal and resulting pulses for pulse counter detector.

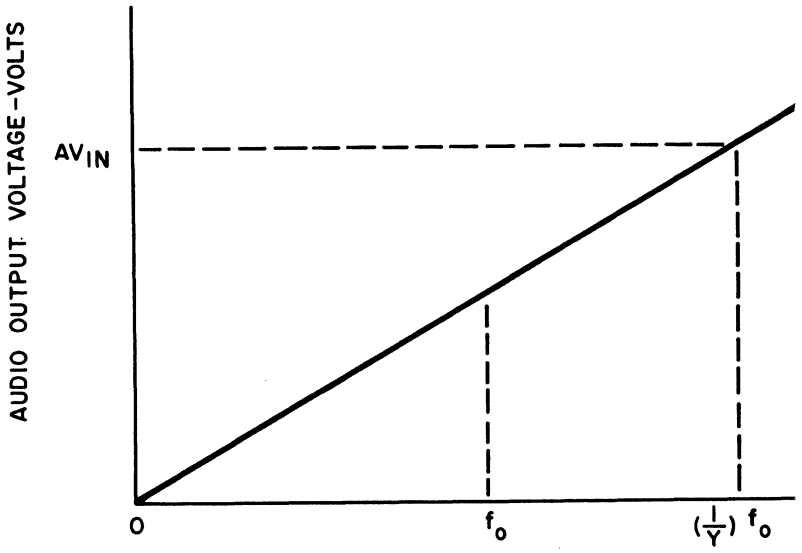


Figure 9.7. Counter detector frequency to dc characteristic.

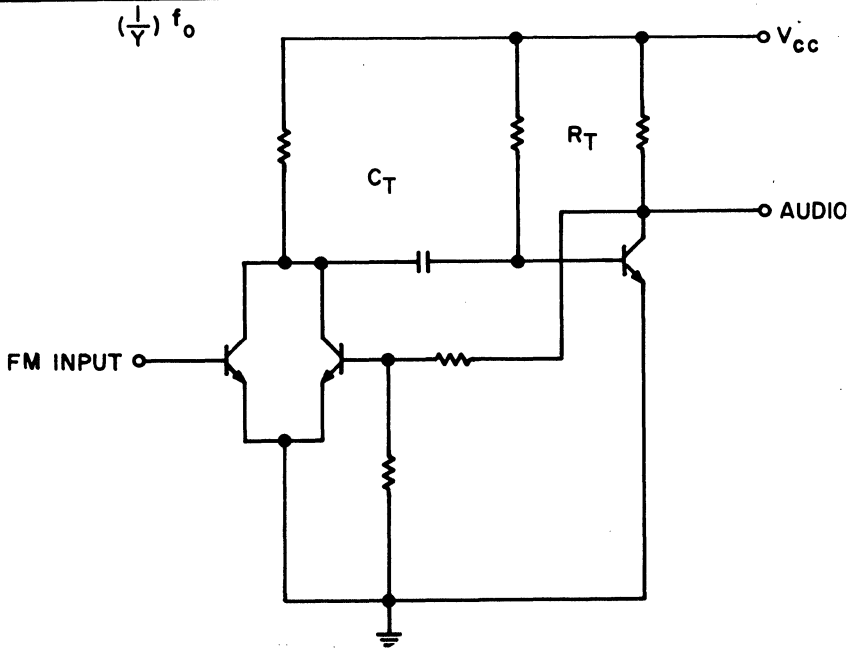


Figure 9.8. Multivibrator counter detector.

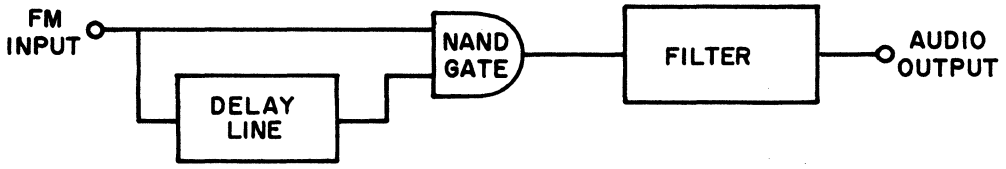


Figure 9.9. NAND gate counter detector.

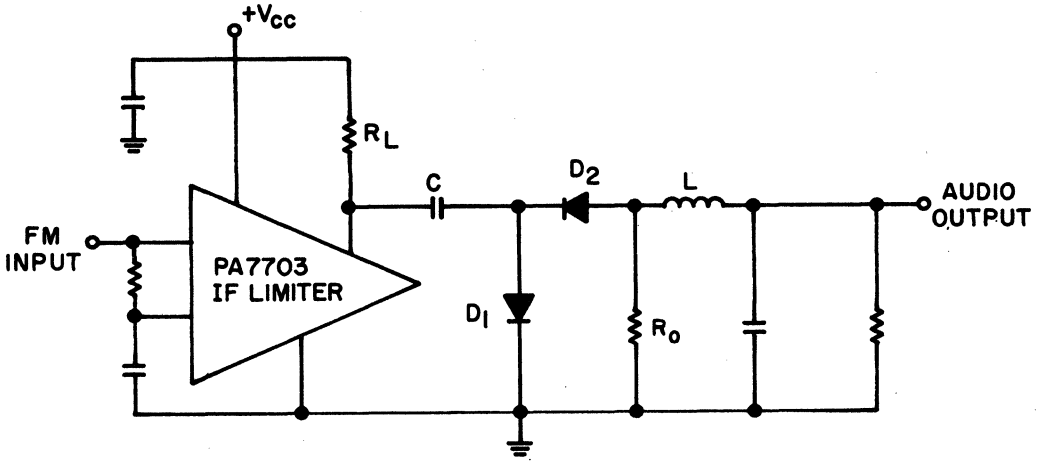


Figure 9.10. Charge transfer pulse counting detector.

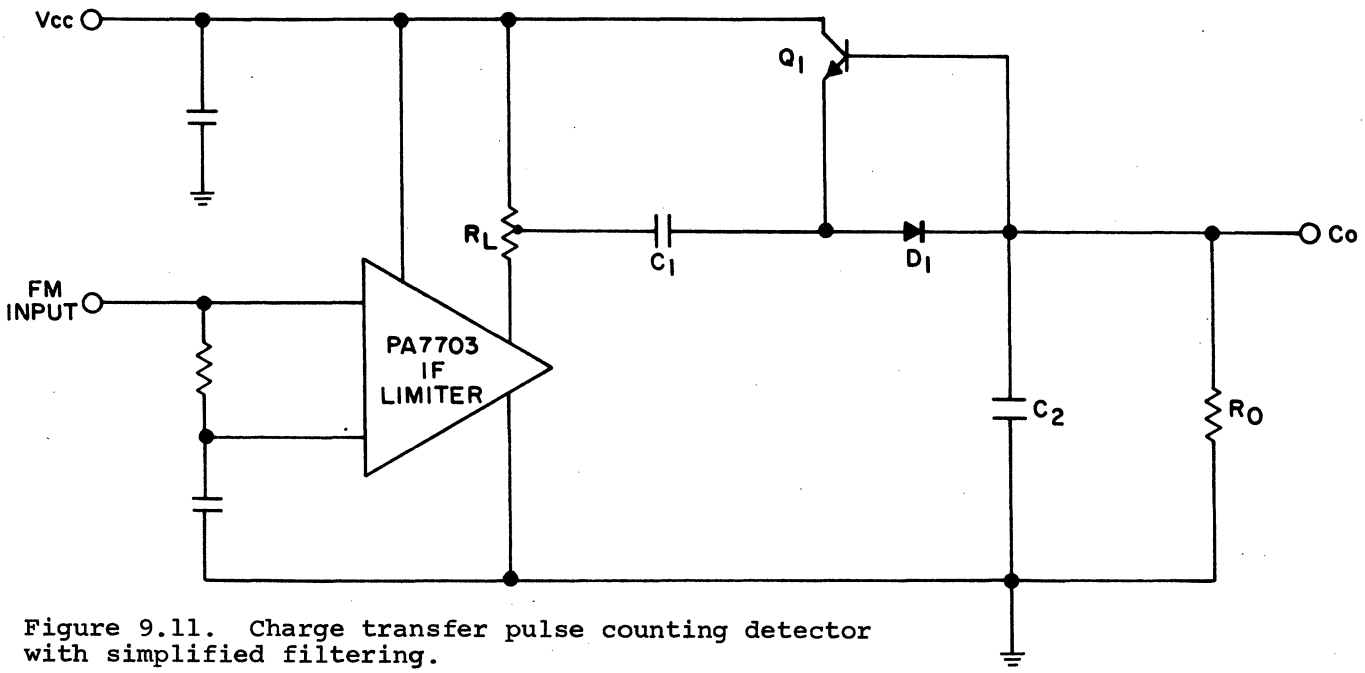


Figure 9.11. Charge transfer pulse counting detector with simplified filtering.

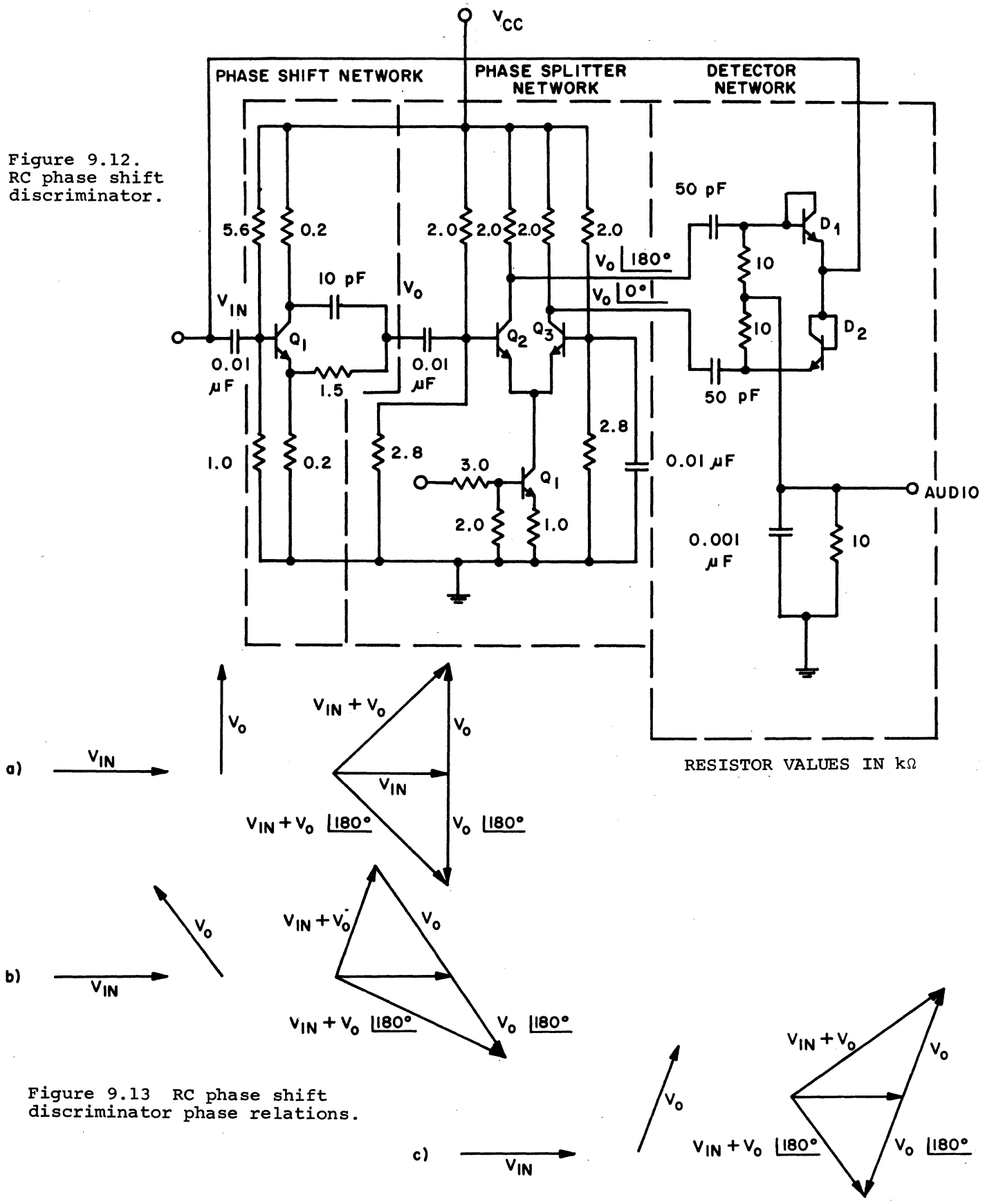


Figure 9.12.
RC phase shift
discriminator.

Figure 9.13 RC phase shift
discriminator phase relations.

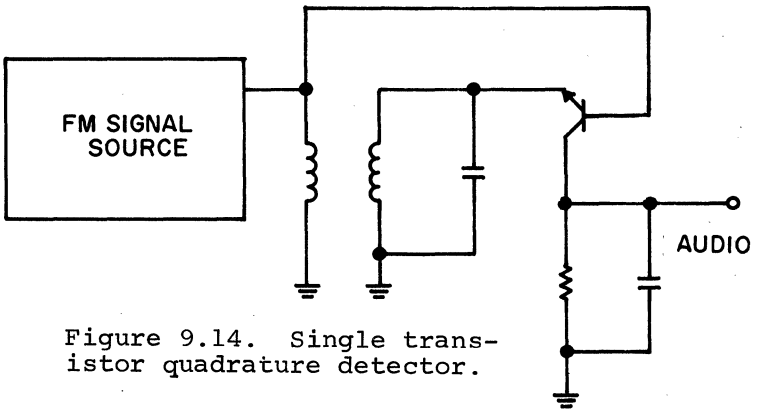


Figure 9.14. Single transistor quadrature detector.

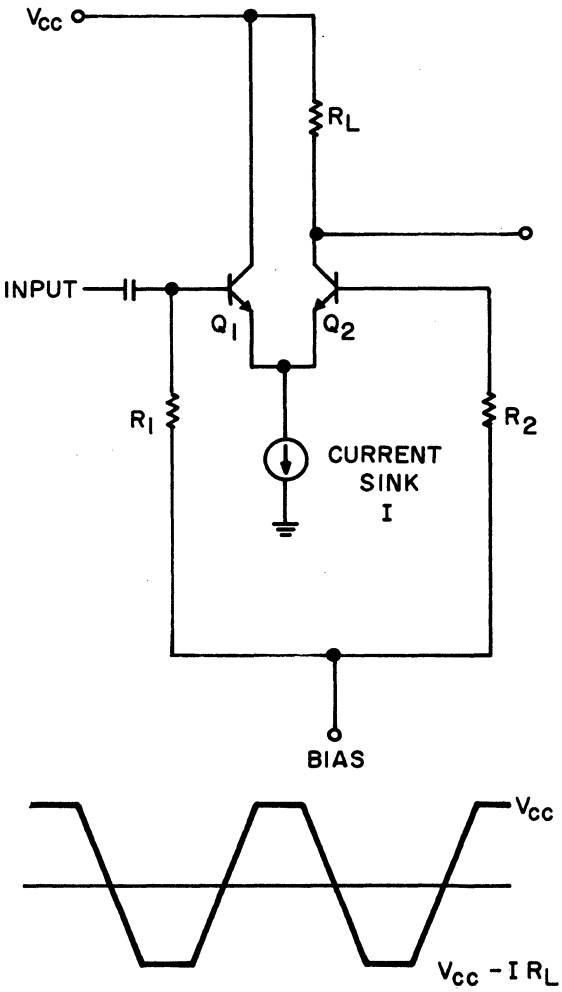
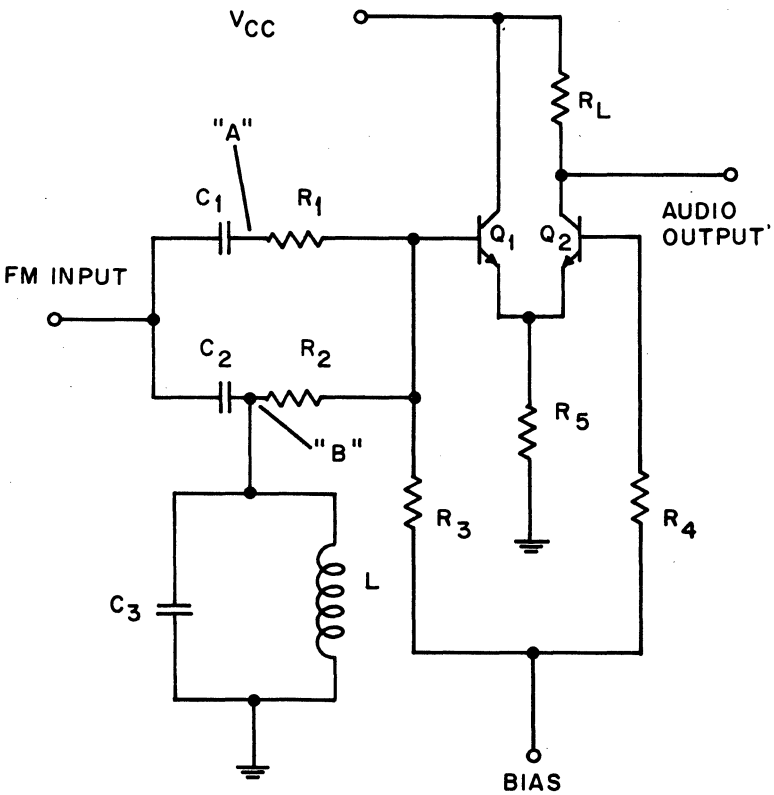


Figure 9.15. Emitter-coupled amplifier.



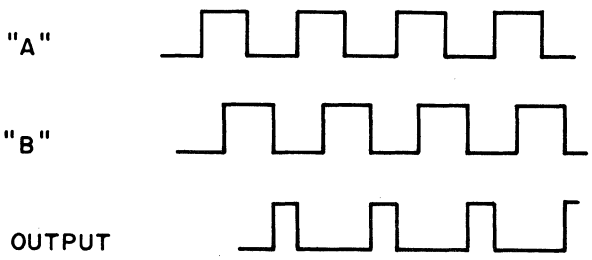


Figure 9.16. Emitter-coupled quadrature detector circuit.

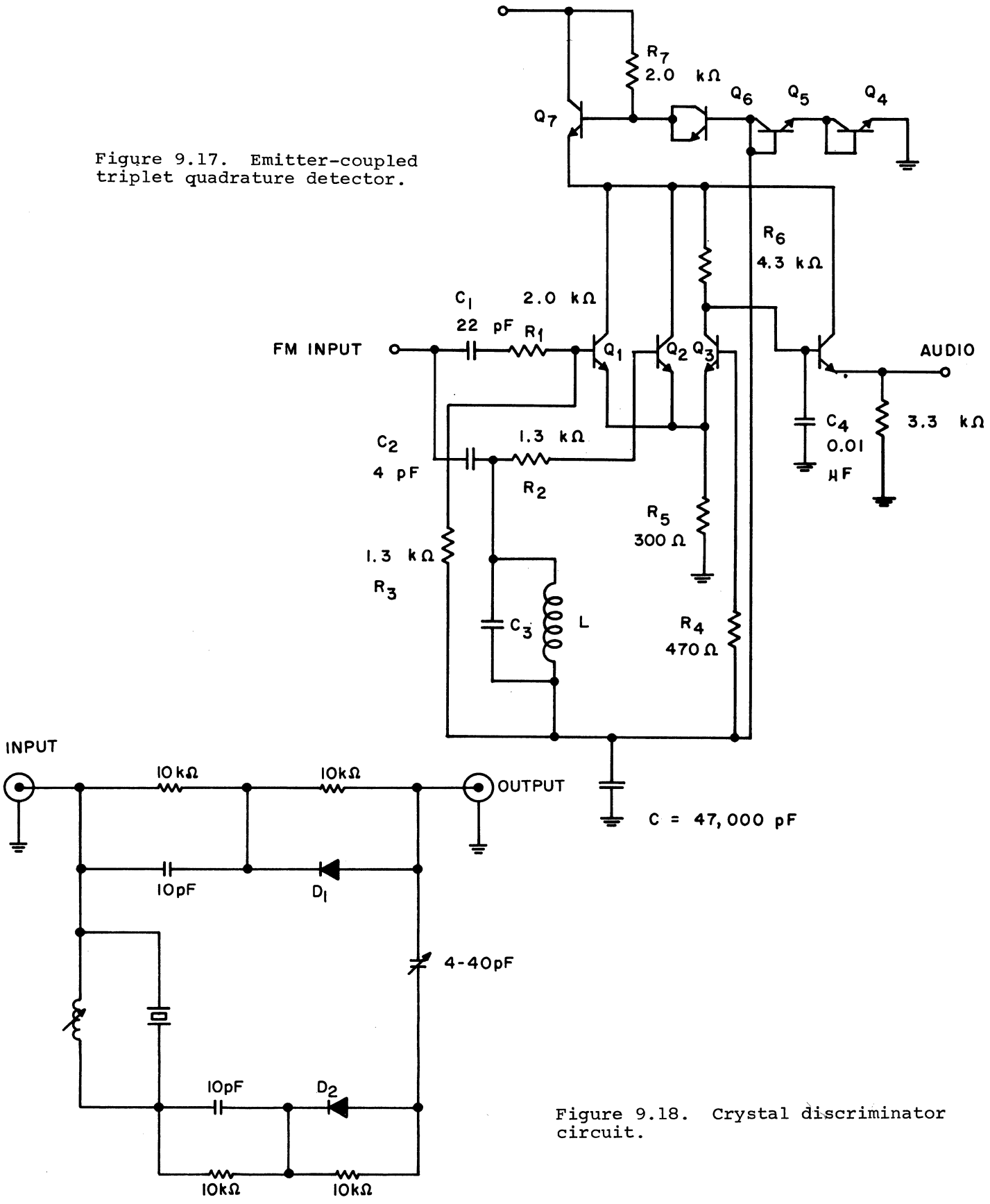


Figure 9.17. Emitter-coupled triplet quadrature detector.

Figure 9.18. Crystal discriminator circuit.

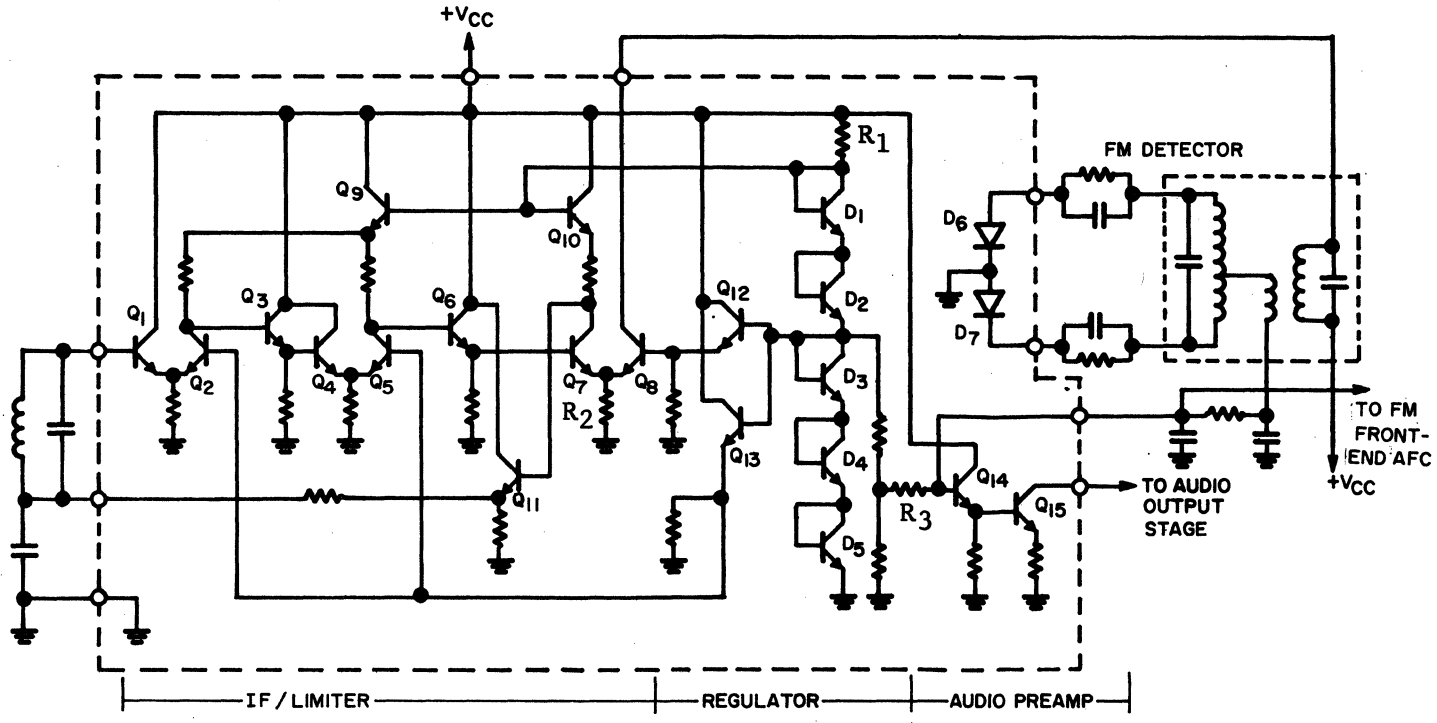


Figure 9.19. Schematic diagram of CP 1053.

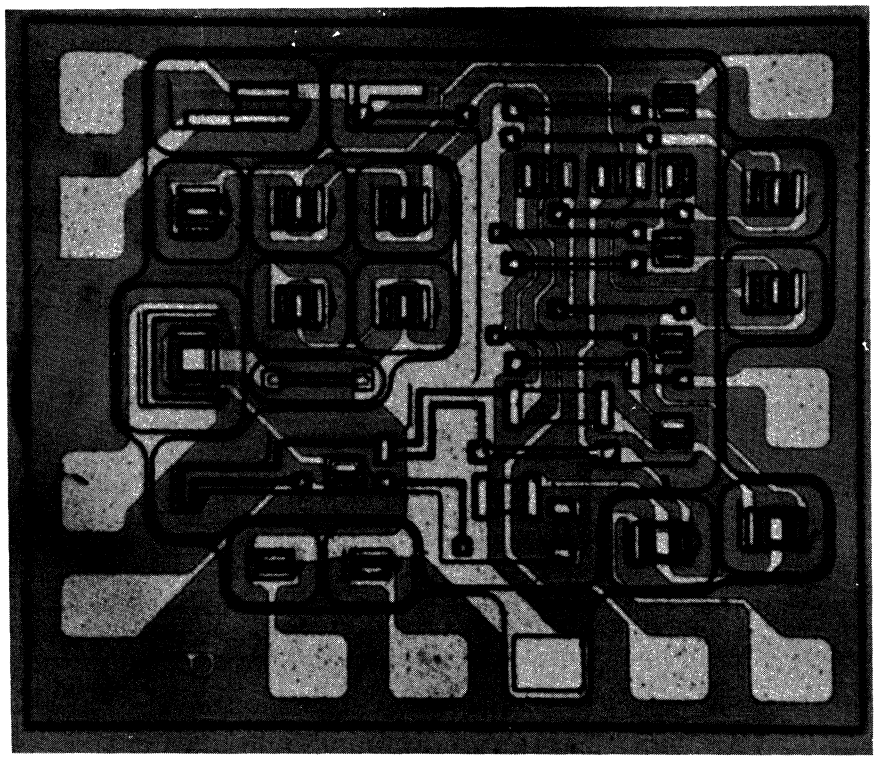


Figure 9.20. Photomicrograph of CP 1053.

Note: Terminal numbers refer to leads of 14-lead metal-bottom flatpack.

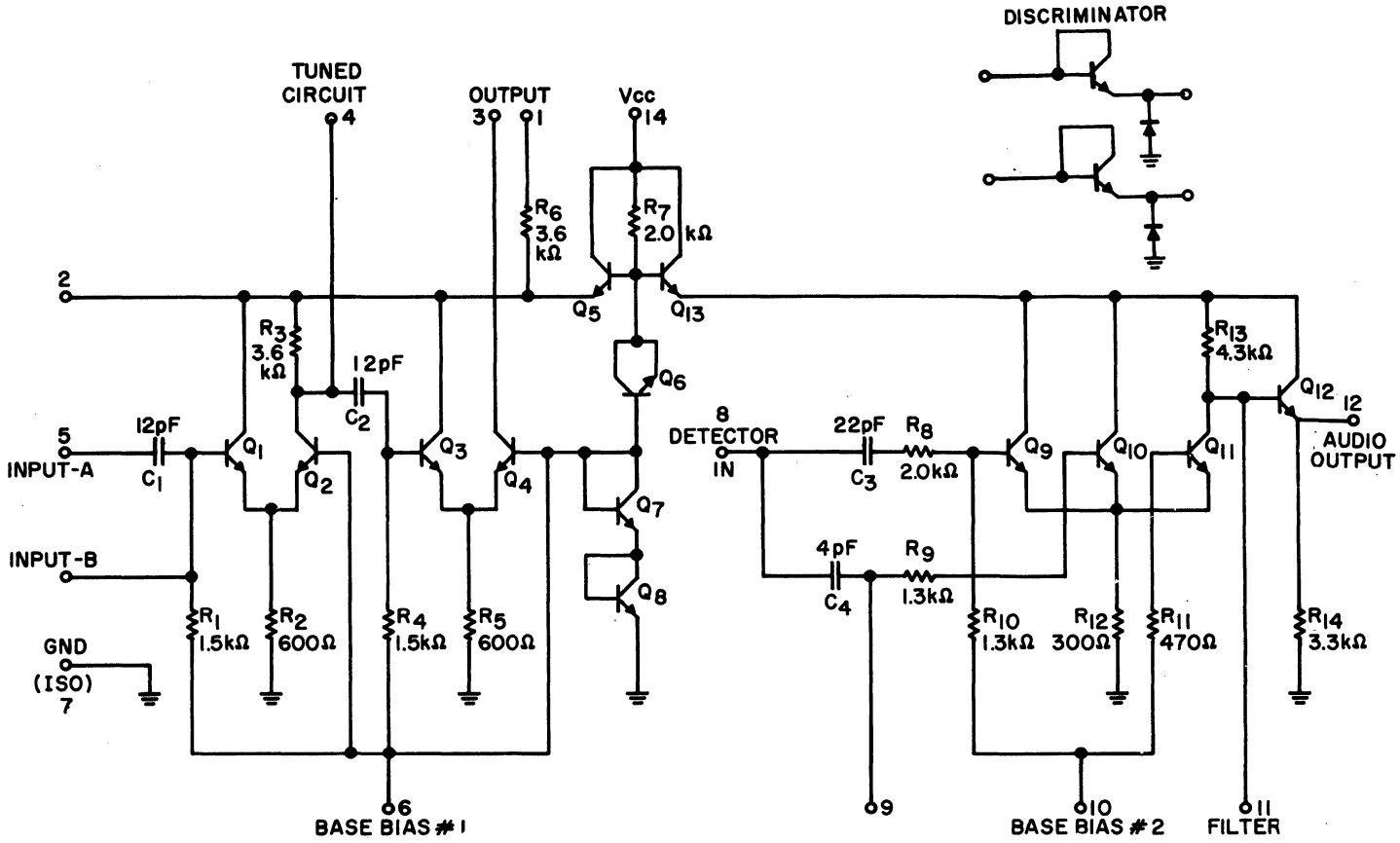


Figure 9.21. Schematic diagram of CP 1058.

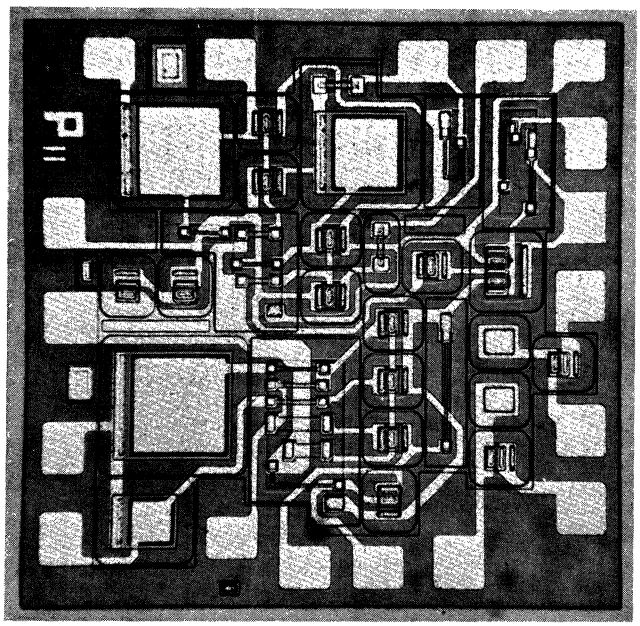


Figure 9.22. Photomicrograph of CP 1058.

10

The Dual Operational Amplifier

by David Long
and David Campbell
Fairchild Semiconductor

The use of an IC having two identical operational amplifiers on a single chip will be covered in this chapter. The IC employed to demonstrate the advantages of this design approach is the μA739, a device intended for use in low-noise industrial signal-processing equipment and in preamplifiers of consumer home-entertainment equipment.

In designing low-level amplifiers there are two major requirements: (1) The equivalent input noise of the circuit must be as low as possible; (2) The output dynamic range should be large enough to handle the variations in input signal level encountered in a broad range of applications. If the circuit adequately meets these two conditions the IC user can move along to look at dc circuit performance, low-frequency characteristics, power consumption, noise, short-circuit protection, amplifier isolation, and required compensation techniques.

10.1 DC CIRCUIT PERFORMANCE

Usually a dual op-amp IC consists of two identical operational amplifiers on a single chip, sharing a common bias supply. Each amplifier is a mirror image of the other. First, we will consider the bias circuit and one amplifier.

The amplifier shown in Figure 10.1A is the μA739. It consists of three gain stages: a differential input stage; a differential-in, single-ended-out second stage; and a Class-A composite pnp/npn output stage.

With a 30-V supply, the output stage will saturate when the collector of Q_5 drops 1.8 V below V^+. This requires that 200 μA flows through R_5. A reserve current of 150 μA is made available from the current source to provide for worst-case resistor values, the base current of Q_7 and a maximum load current of 9 mA. This ensures that the collector potential of Q_5 cannot fall below its base potential.

Level translation is achieved in the output stage, which is composed of the composite pnp combination Q_7 and Q_8. A single pnp device cannot be used here since an integrated lateral pnp cannot provide adequate h_{FE}. The addition of Q_8 to the circuit permits achieving the necessary gain without changing the basic structure of the Class-A common-emitter output stage. Figure 10.1B shows how this increase in h_{FE} is obtained. Resistor R_7 is added to the collector load of Q_7 in order to reduce the loop gain and phase shift in the local feedback loop of the composite pnp device. This inclusion of R_7 also increases the slew rate.

10.2 LOW-FREQUENCY GAIN

The output stage gain is given by the ratio of R_8 to R_6; for the circuit values shown, this ratio is 5000/200 or 25.

The gain of each of the first two stages is given by $g_m R_L$ where $g_m = 40$ Ie (in mA), and R_L is the parallel combination of the load resistance and the input impedance of the next stage. For the first stage, $I_e = 0.1$ mA, therefore $g_{m1} = 4.0$ mA/V. The differential input impedance of the second stage is approximately $2\beta re_2 \approx 16$ kΩ.

Therefore, R_L = 6.2 kΩ and the differential voltage gain of the first stage is 25.

The input impedance to the third stage is approximately $\beta(Q_7, Q_8) \times R_6 \approx 40$ kΩ. The effective load on the second stage is 7.4 kΩ. The emitter current is 0.175 mA; therefore g_{m2} = .7 mA/V. The voltage gain A_{V2} of the second stage is equal to 26. Transistors Q_1 and Q_2 form a differential input pair with Q_3 acting as a current source. Bias for the base of Q_3 is obtained from the combined V_{BE} drops of D_5 and D_6. If it is assumed for the moment that V_{BE} = 0.6 for all transistors and diodes, then the voltage across R_3 is 0.6 V. The current through it must, therefore, be 200 μA. This current divides equally between the collector loads R_1 and R_2 causing a voltage drop of 1 V across each load resistor. The collector voltages of Q_1 and Q_2 are, therefore, V_A-1 volts.

The transistor differential pair, Q_4 and Q_5, is supplied by the current source Q_6, which derives its bias from the same point as Q_3. This current source supplies 350 μA.

Again, assuming perfect matching and neglecting the Early effect (basewidth modulation) the current being supplied by Q_6 is divided equally between Q_4 and Q_5. If the base current of Q_7 can be neglected, the collector voltage of Q_5 will be V^+-1.6 V.

Now consider the worst-case collector-base reverse-bias voltages on Q_4 and Q_5. If a large positive differential voltage is applied to the amplifier input, the entire current from Q_3 (200 μA) will pass through Q_1, and Q_2 will be off. The collector voltages of Q_1 and Q_2 will then be:

$$V_{C_1} = V_A - 2V \tag{10.1}$$

$$V_{C_2} = V_A \, . \tag{10.2}$$

Q_5 will be turned fully on, since its base will be 2 V higher than the base of Q_4. Under these conditions, saturation of Q_5 is prevented by the four diodes, D_1 through D_4. The highest voltage that appears on the base of Q_5 is V^+-2.4 V.

To summarize, the low-frequency gain values obtained are: A_{V2} = 25; A_{V2} = 26; A_{V3} = 25.

The total gain from input to output is:

$$A_{VO} = A_{V1} A_{V2} A_{V3} \, . \tag{10.3}$$

$$A_{VO} = 25 \times 26 \times 25 = 16{,}250 \text{ or } 84 \text{ dB} \, .$$

The total gain is relatively constant for wide variations in absolute value of the individual resistors in the circuits. In the first two stages, g_m has a proportional relationship with emitter current, which, in turn, is inversely proportional to the resistor in the emitter of the current source. Therefore, the ratio of the current-source resistor value to the collector load resistance determines the gain. The gain

of the output stage is also dependent upon resistor ratios.

The calculation of the full-temperature and supply-voltage dependence on gain is a long procedure and is not included here. The variation of voltage gain measured for changes in temperature and supply voltage is shown in Figure 10.2A and 10.2B.

10.3 BIAS STABILITY AND SIGNAL-HANDLING CAPABILITY

Offset voltage is also a function of temperature and supply voltage. How input bias current and offset current vary with temperature and supply voltage is shown in Figures 10.3 and 10.4. The bias scheme used in the μA739 IC was selected for gain stability over a wide operating range; it enables the amplifier to be used at supply voltages between 9 and 36 V. The common-mode range is limited to the base voltage at Q_3 ($2V_{BE}$) and the collector voltage of Q_1 and Q_2 ($V^+ - 4V_{BE} - 1$). Thus, for operation at $\pm$15 V, the common-mode range is approximately +11.5 V to -13.8 V. At $\pm$4.5 V, this range reduces to +1.0 V to -2.8 V. In either case, the common-mode range may be exceeded without causing latch-up. The common-mode range is shown in Figure 10.5.

The output swing is limited in the positive direction by the saturation voltage of Q_8 and the voltage across R_7 to within 2.5 V of the positive supply; i.e., +12.5 V for +15-V supply. Negative output swing is limited by the load on the output. The output swing is shown in Figures 10.5, 10.6A and 10.6B.

10.4 POWER DISSIPATION

The typical dissipation for the μA739 with a 30-V supply is 350 mW. Figure 10.7A shows the typical supply current with various loads as a function of supply voltage; Figure 10.7B depicts the variation of supply current with temperature; and Figure 7C gives the device dissipation under the same conditions. These specifications are for an output voltage halfway between the positive and negative supplies -- the normal quiescent mode in a linear amplifier circuit. The maximum permissible dissipation for the package is 500 mW derated linearly at 7.7 mW/°C above 60°C.

10.5 SHORT CIRCUIT PROTECTION

Short-circuit output current is limited by the available drive. Consider the case where the output terminal is shorted to the negative supply. Maximum output current exists when the entire collector current of Q_6 passes through R_5. This assumes infinite h_{FE} for the output composite pnp, a worst case for this mode. The voltage across R_5 will be 4.1 V and the voltage across R_6 will be 3.4 V. The maximum current through R_6 and into the short circuit is therefore 17 mA. The dissipation in Q_8 when operating from $\pm$15 V will be approximately 460 mW -- close to the maximum for the package. A continuous short circuit would raise the temperature about 60°C.

No damage will occur to the device under these conditions with operation at normal ambient temperatures. Simultaneously shorting both outputs however, could raise the chip temperature above the maximum allowed for the package.

10.6 CHANNEL ISOLATION

Figure 10.1C shows how the second channel of the μA739 is added. Any signal emanating from one channel to the bias circuit will have been attenuated by the common-mode rejection. It will then be further attenuated by the low impedances at X and Y (Figure 10.1C) and will appear at common-mode points in the other channel. The

isolation at 1 kHz will be at least equal to the combined common-mode rejections of the two amplifiers. At very high frequencies, coupling between the device leads and the accompanying circuit wiring will be the major source of coupling. At low frequencies, inadequate power supply and bias decoupling may reduce the isolation. Finally, at very low frequencies, thermal coupling across the chip will cause some slight interaction.

These effects are illustrated in Figure 10.8. Channel isolation is so dependent upon external circuit and signal conditions, that it is difficult to give a precise specification for this parameter. Figure 10.8 demonstrates that the isolation is entirely adequate for most operations. Figure 10.9 shows common-mode rejection as a function of frequency.

10.7 NOISE

The choice of the input-stage collector current depends upon the source impedance for which the circuit is to be optimized. High source impedances call for low collector currents in order to keep noise current down; low source impedances require low emitter resistances and, therefore require higher collector currents to obtain low noise voltage. For best signal-to-noise ratio, the noise figure is optimized for low-impedance sources (500 Ω to 5 kΩ). Spot noise voltage and current are plotted in Figure 10.10A and 10.10B, and wideband noise voltage and current are plotted in Figures 10.11A and 10.11B.

Other sources of noise are 1/f noise and "popcorn" noise. In particular, popcorn noise (also termed "burst" noise or "multi-state" noise) is most objectionable. This kind of noise, frequently encountered in bipolar semiconductor devices, is characterized by discrete pulses superimposed on the normal wideband noise. The amplitude of these pulses is generally constant, while the frequency and length are completely random. The noise is probably caused by recombination effects at the silicon chip surface and is most prevalent at low temperatures with high source impedances. IC processing improvements have been reducing burst noise and 1/f noise.

10.8 COMPENSATION

Compensation of the μA739 can be customized to the individual circuit. For a given application, the output voltage swing and the closed-loop gain will determine the compensation required.

The open-loop gain and phase responses are plotted in Figure 10.12. The dominant pole at 600 kHz is caused by the transit delay in the lateral pnp. Two other major poles at 1 MHz and 2 MHz are caused by the phase shift at the collectors of the differential gain stages. For very high source impedances, the input capacitance will add a pole as shown by the dashed line in Figure 10.12. The variation of 180° phase-shift frequency with supply voltage is shown in Figure 10.13. The compensation networks given apply over the voltage range of 8 to 30 V.

For many applications, a single capacitor is sufficient to ensure stability of the circuit. Single-component compensation can be accomplished between pin 1 and ground, between pins 3 and 4, and from pin 2 to either supply or ground. If compensation is used shunting pin 2, it should be placed between pin 2 and pin 14 (V^+) rather than

between pin 2 and ground. Examination of the output circuit indicates the reason for this. If the capacitor is grounded, signals on the power supply are amplified through the output stage as a common-base circuit. This degrades the amplifier sensitivity to high-frequency power supply noise. If the capacitor is placed between pins 2 and 14, high-frequency power-supply signals become a common-mode input to the output stage. Frequency response for various capacitor values are shown in Figure 10.14A, 10.14B and 10.14C.

Feedback compensation can be used to control the amplifier frequency response; the capacitors can be placed between pins 1 and 2, or 2 and 3. Compensation around the output stage is similar to lag compensation from pin 2 to pin 14; the capacitor value needed is smaller and the pole caused by the output stage is better controlled in the region from 0.1 MHz to MHz. Second-stage feedback compensation converts this stage to a voltage follower. An advantage of this compensation is that it produces both a pole and a zero in the forward response. The amount of attenuation inserted is equal to the second-stage gain plus 6 dB. Frequency response of the μA739 for feedback compensation is shown in Figure 10.15A and 10.15B.

Unity-gain compensation for phono preamplifiers, integrators, and most dc applications requires compensation around more than one stage for adequate phase margin. For applications where slew rate is not a factor, output compensation combined with second-stage feedback compensation (Figure 10.16A) can be used to keep the number of components used to a minimum. For maximum output swing, input compensation and feedback compensation around the output stage will give 60° of phase margin with 3 V/μs slew rate. Phase lead must be included in the input compensation as shown in Figure 10.16B.

The slew rate can be predicted for any value of capacitor. Figure 10.17 shows slew rate versus capacitance for the compensation networks indicated. The slew rate may be calculated from:

$$S = \frac{I}{C} A \tag{10.4}$$

where I is the available current to charge the compensating capacitor, C is the capacitor value, and A is the gain from the compensating point to the output. For example, if .01 μF is used between pins 3 and 4 and I = 200 μA, A = 25.7 x 25, and $S^{'}$ = 12.8 V/μs.

10.9 OPERATING SAFEGUARDS

When connecting the μA739 in a circuit, observing proper lead orientation is important. If the μA739 is installed in reverse, V^{+} and V^{-} will be interchanged, excessive currents will flow in the substrate diode, and the IC may be damaged.

When using the μA739, bypass capacitors should be connected from the supply terminals to ground to eliminate the effects of power-supply lead inductance. A 0.01 μF disc capacitor mounted close to the IC pin provides enough decoupling to eliminate the effects of this inductance.

FIGURES

Figure 10.1A. Amplifier "A". One of the pair of amplifiers in the dual op-amp μA739. Bias source is included with amplifier circuit.

Figure 10.1B. Composite pnp configuration. When the low-h_{FE} lateral pnp Q_1 is combined with a high-h_{FE} npn, a high-gain pnp equivalent structure results. $I_{B2} = I_B h_{FE1}$; $I_c = (1 + h_{FE2})\ I_{B2} = I_{B2} h_{FE1}\ (h_{FE2} + 1)$; $I_c/I_B = h_{FE1}\ (h_{FE2} + 1) \approx h_{FE1} h_{FE2}$.

Figure 10.1C. Circuit diagram for the μA739.

Figure 10.2. Uncompensated open-loop voltage gain (A) as a function of temperature, (B) as a function of supply voltage.

Figure 10.3. Input offset current and bias current as functions of temperature.

Figure 10.4. Input offset current and bias current as functions of supply voltage.

Figure 10.5. Common-mode range as a function of supply voltage.

Figure 10.6A. Output voltage capability as a function of supply voltage.

Figure 10.6B. Typical output voltage swing as a function of supply voltage.

Figure 10.7 Total supply current (A) as a function of supply voltage, (B) as a function of temperature.

Figure 10.7C. Total dissipation as a function of supply voltage and load.

Figure 10.8. Channel separation as a function of frequency.

Figure 10.9. Common-mode rejection as a function of frequency.

Figure 10.10A. Input noise voltage as a function of frequency.

Figure 10.10B. Input noise current as a function of frequency.

Figure 10.11A. Wideband noise voltage as a function of temperature.

Figure 10.11B. Wideband noise current as a function of temperature.

Figure 10.12. Uncompensated open-loop operation: (A) frequency response, (B) phase shift.

Figure 10.13. Opon-loop 180° phase-shift frequency as a function of supply voltage.

Figure 10.14. Frequency response with (A) output compensation, pin 1 to ground, (B) second-stage lag compensation, pin 2 to ground, (C) input compensation, pin 3 to pin 4.

Figure 10.15. Frequency response with (A) second-stage feedback compensation, pin 2 to pin 3, (B) output stage feedback, pin 1 to pin 2.

Figure 10.16. (A) Low slew-rate unity-gain frequency response.
(B) Maximum slew-rate unity-gain frequency response.

Figure 10.17. Maximum slew rate for various compensation techniques.

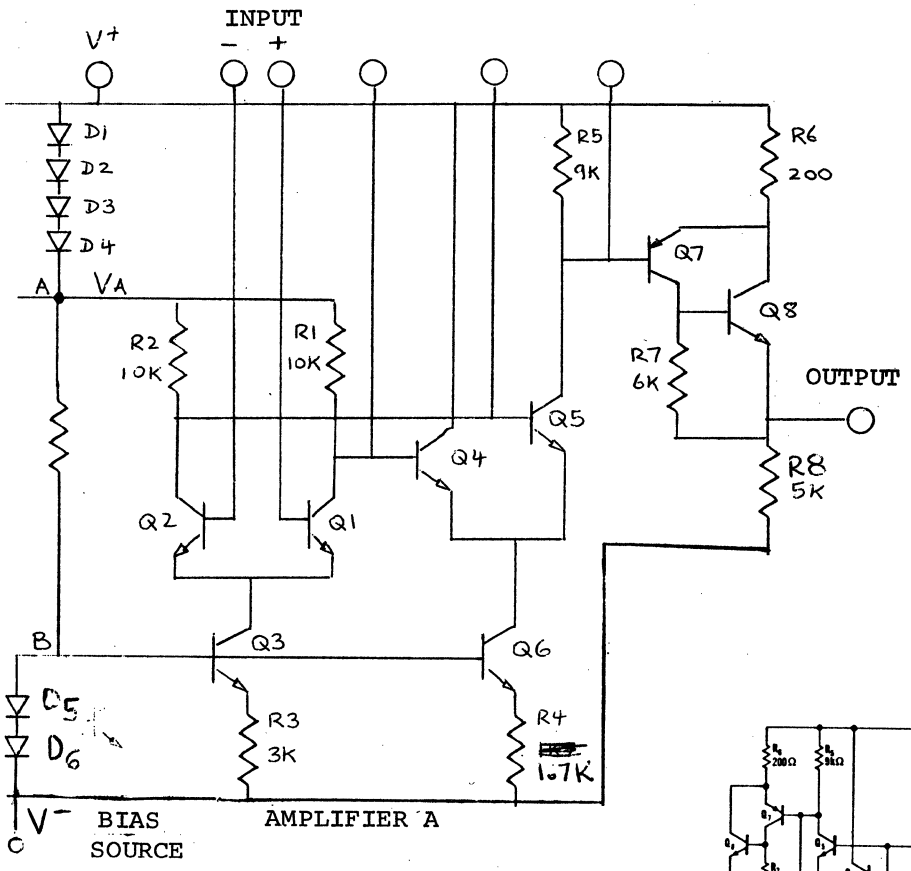


Figure 10.1A. Amplifier "A" One of the pair of amplifiers in the dual op-amp μA739. Bias source is included with amplifier circuit.

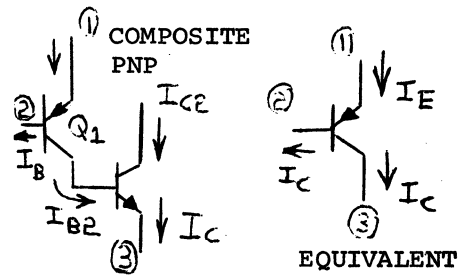


Figure 10.1B. Composite pnp configuration. When the low-h_{FE} lateral pnp Q_1 is combined with a high-h_{FE} npn, a high-gain pnp equivalent structure results. In this circuit:

$$I_{B2} = (I_B)\ (h_{FE1})$$

$$I_C = (1 + h_{FE2})\ I_{B2}$$

$$= I_B h_{FE1}\ (h_{FE2} + 1)$$

$$I_C/I_B = h_{FE1}(h_{FE2} + 1) \approx h_{FE1} h_{FE2}$$

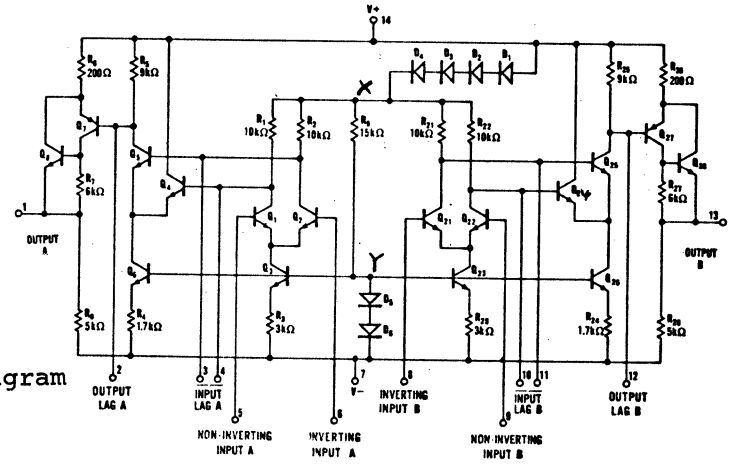


Figure 10.1C. Circuit diagram for the μA739.

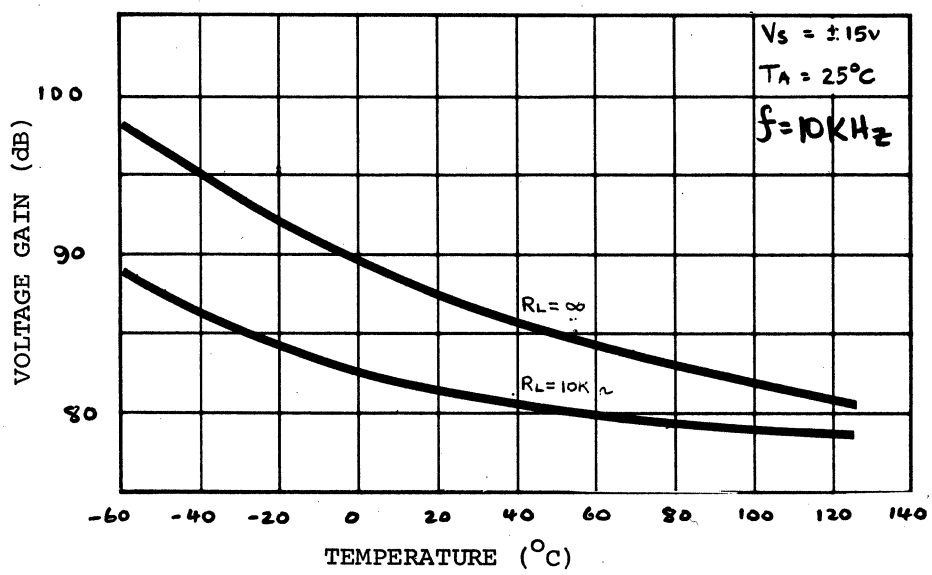


Figure 10.2A. Uncompensated open-loop voltage gain as a function of temperature.

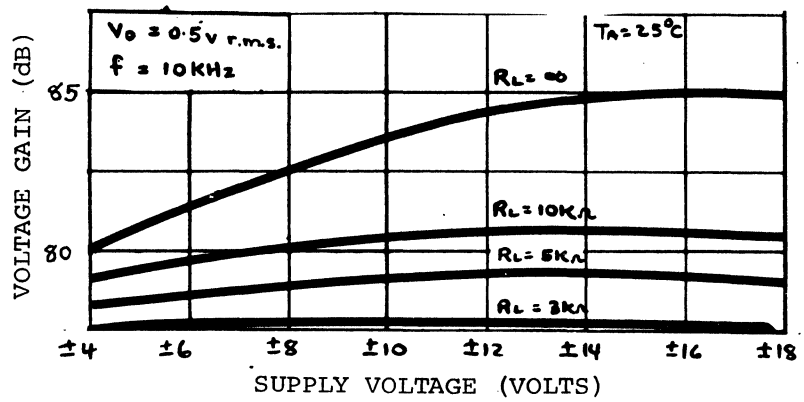


Figure 10.2B. Uncompensated open-loop voltage gain as a function of supply voltage.

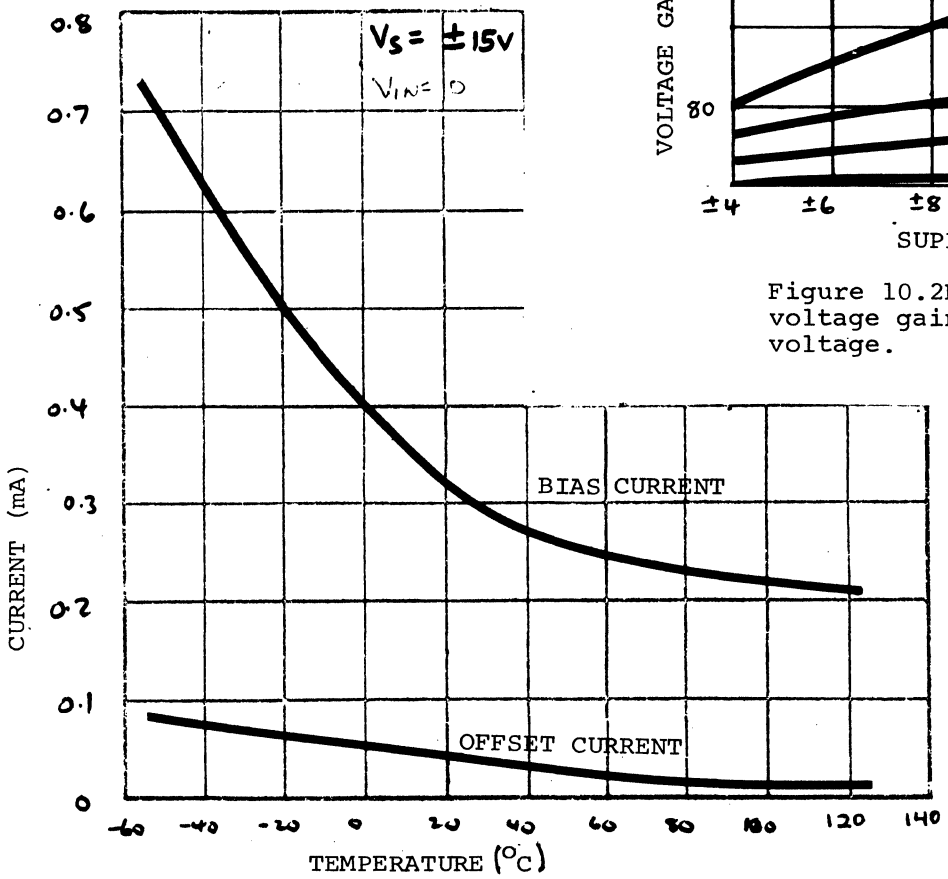


Figure 10.3. Input offset current and bias current as functions of temperature.

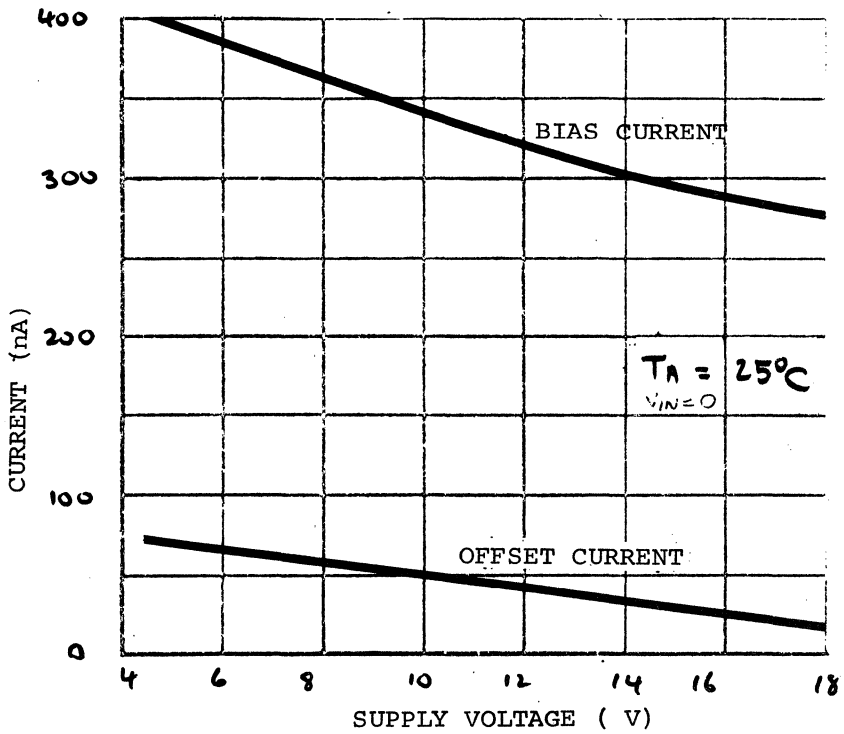


Figure 10.4. Input offset current and bias current as functions of supply voltage.

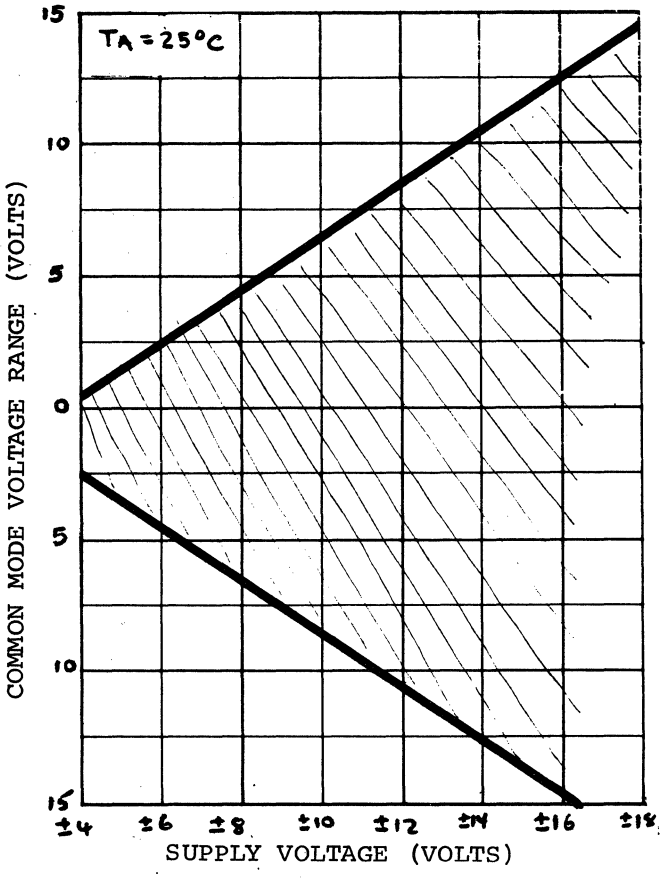


Figure 10.5. Common-mode range as a function of supply voltage.

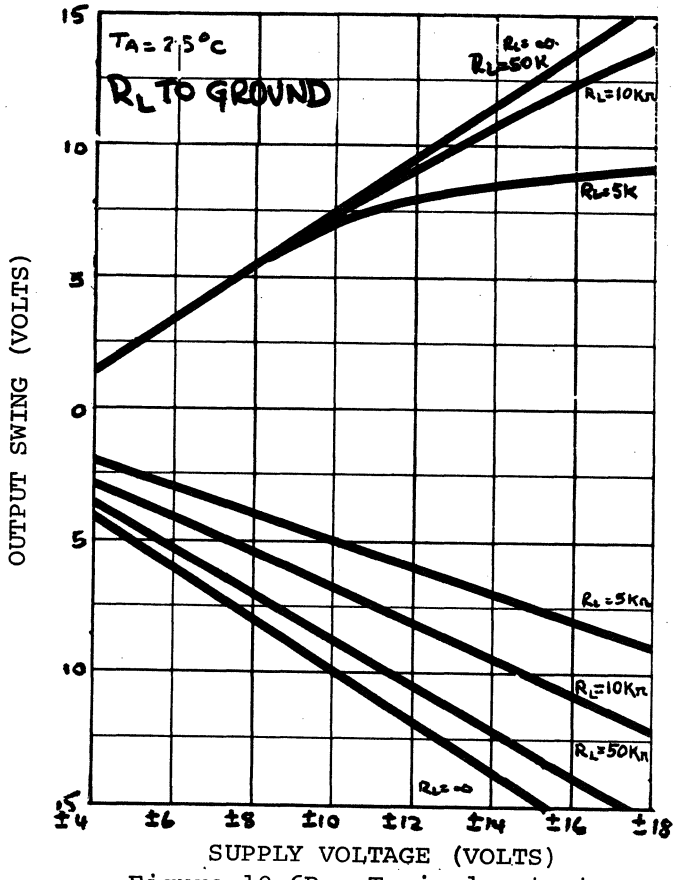


Figure 10.6B. Typical output voltage swing as a function of supply voltage.

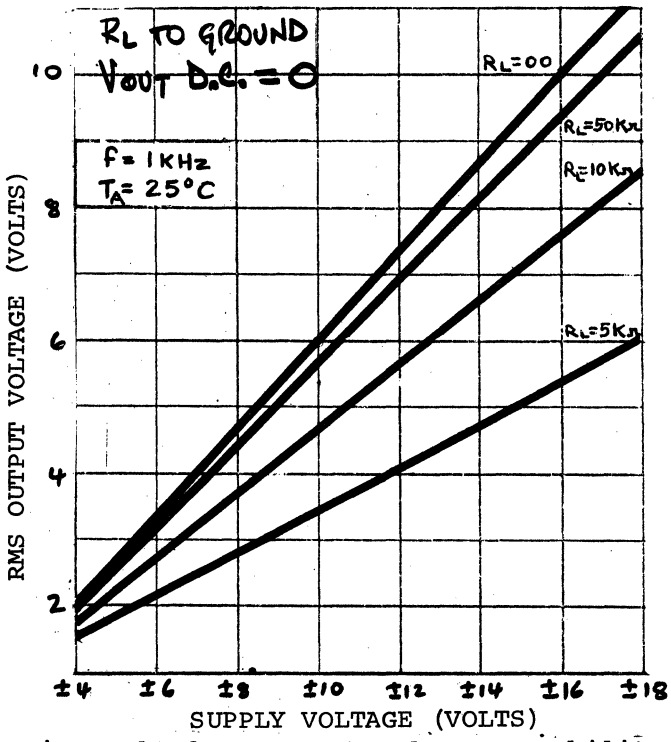


Figure 10.6A. Output voltage capability as a function of supply voltage.

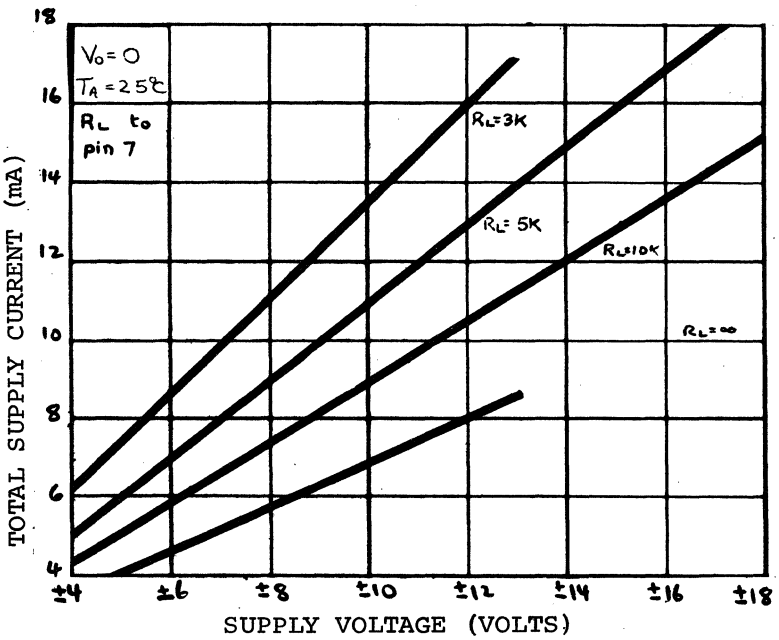


Figure 10.7A. Total supply current as a function of supply voltage.

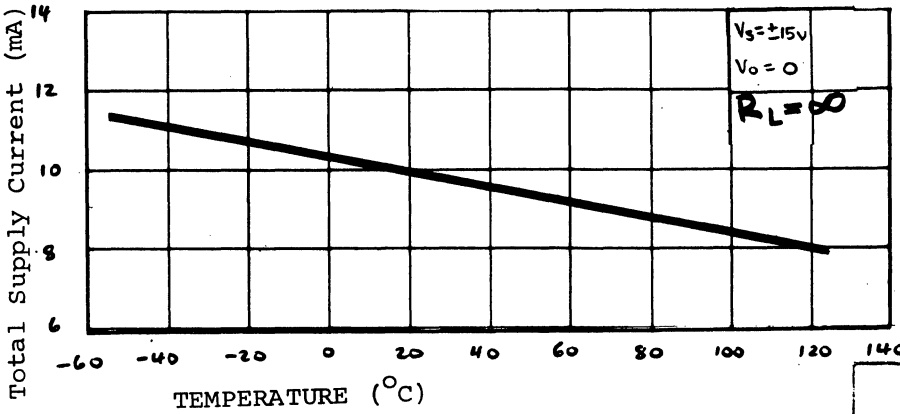


Figure 10.7B. Total supply current as a function of temperature.

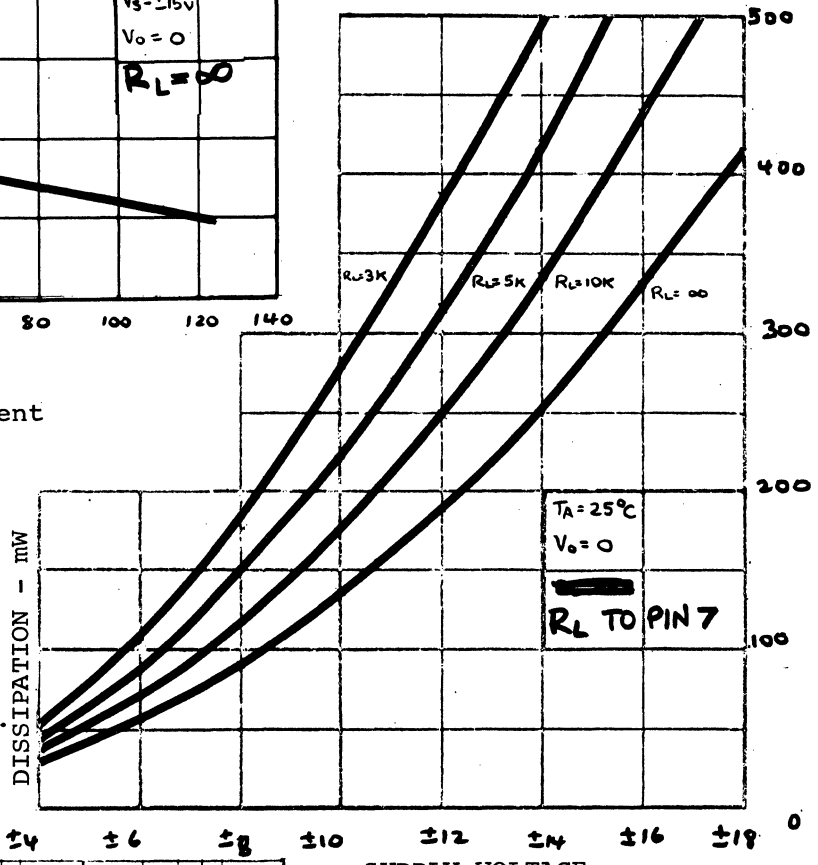
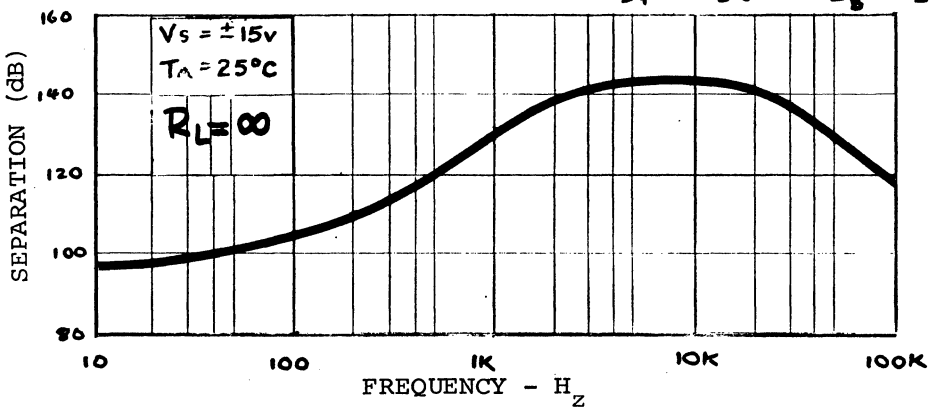


Figure 10.7C. Total dissipation as a function of supply voltage and load.



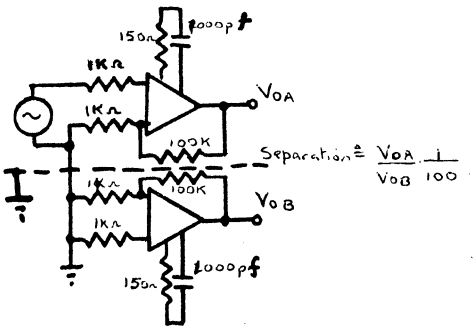
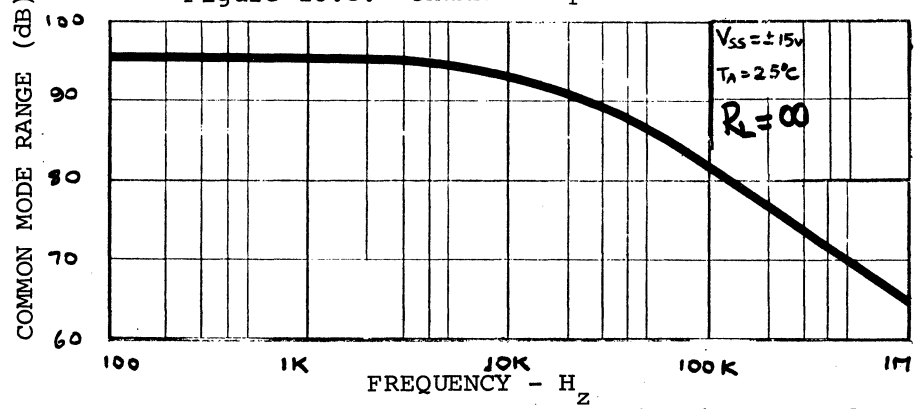


Figure 10.8. Channel separation as a function of frequency.



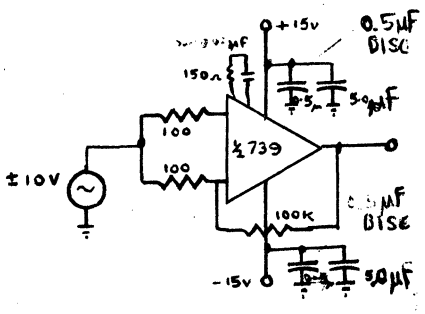


Figure 10.9. Common-mode rejection as a function of frequency.

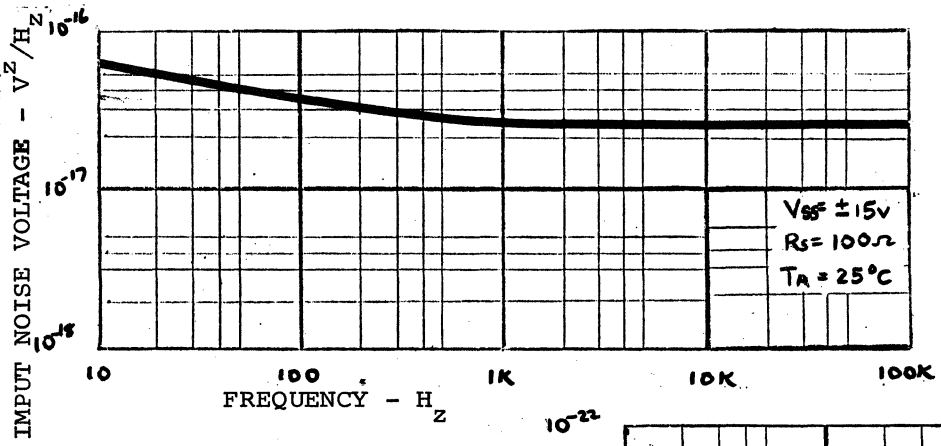


Figure 10.10A. Input noise voltage as a function of frequency.

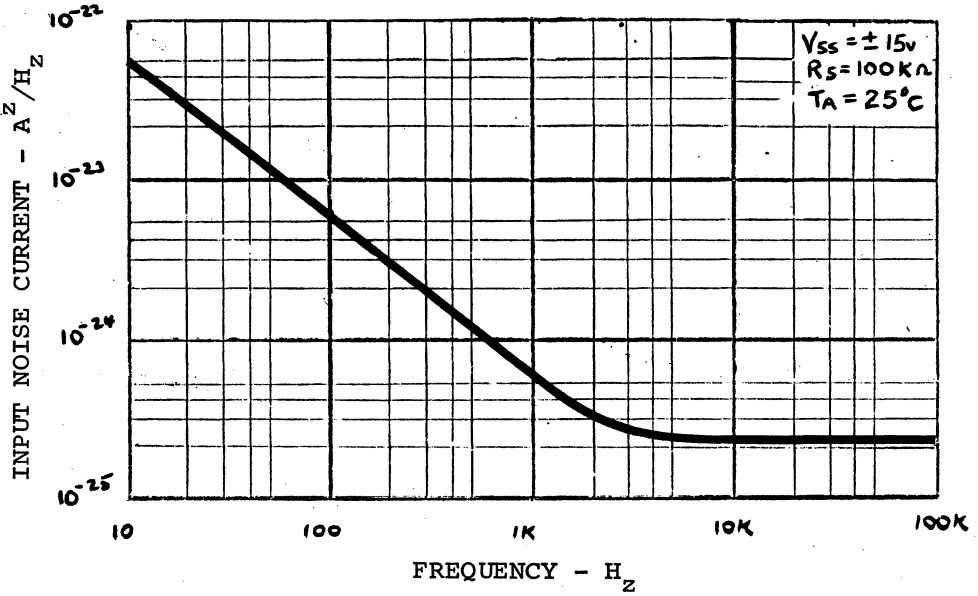


Figure 10.10B. Input noise current as a function of frequency.

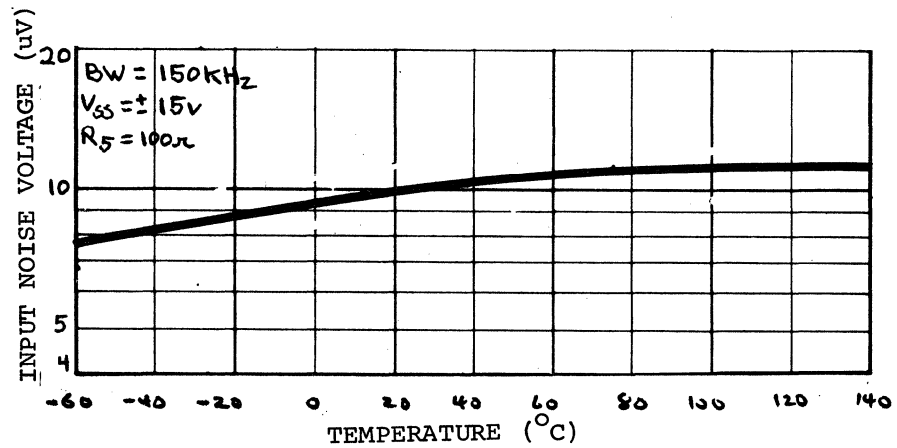


Figure 10.11A. Wideband noise voltage as a function of temperature.

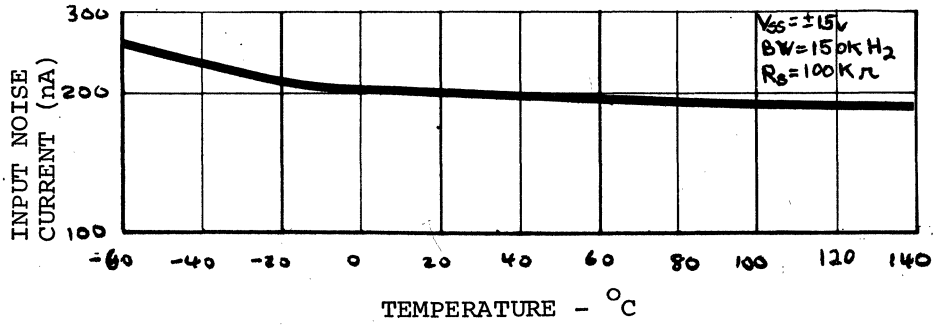


Figure 10.11B. Wideband noise current as a function of temperature.

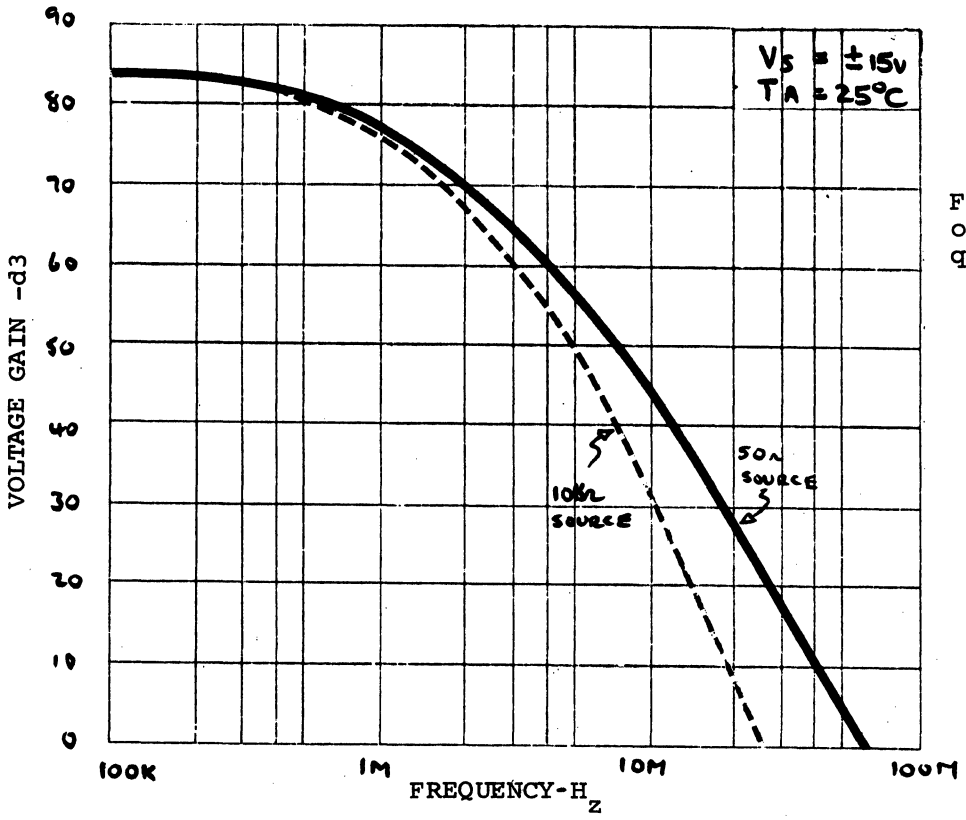
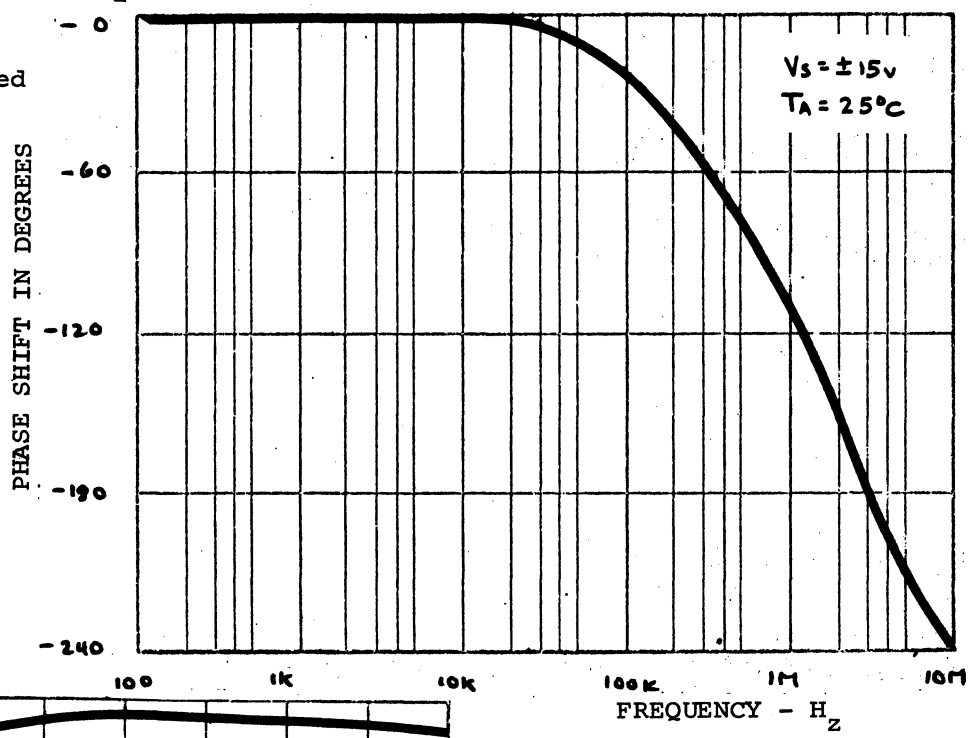


Figure 10.12A. Uncompensated open-loop operation: frequency response.

Figure 10.12B. Uncompensated open-loop operation: phase shift.



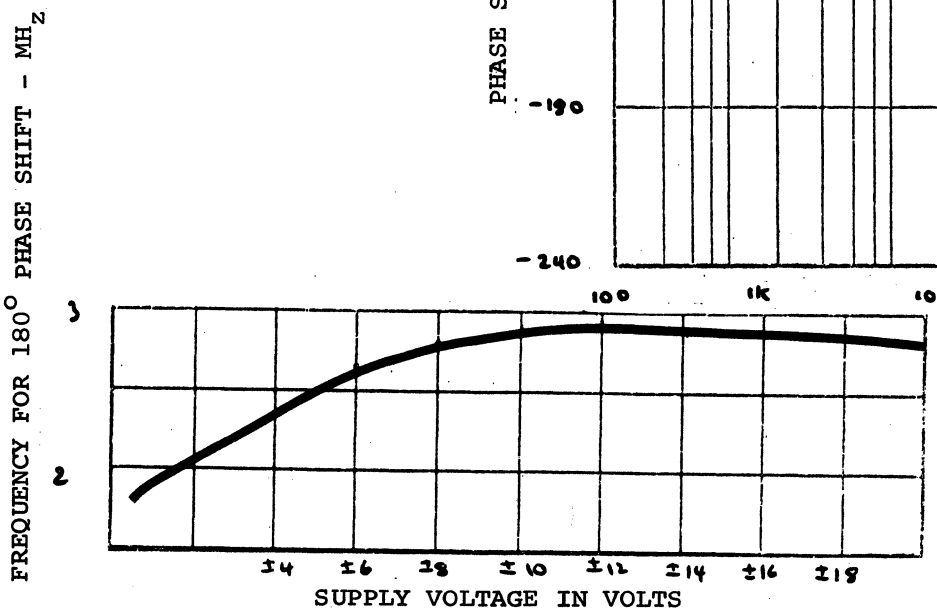


Figure 10.13. Open-loop 180° phase-shift frequency as a function of supply voltage.

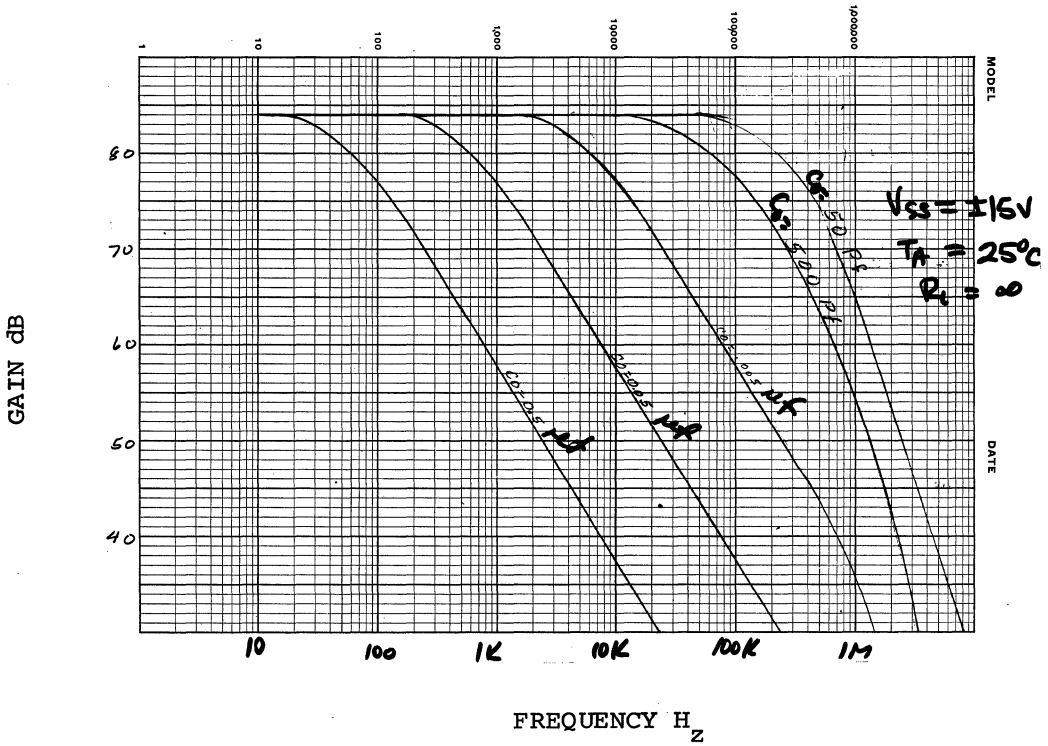


Figure 10.14A. Frequency response with output compensation, pin 1 to ground.

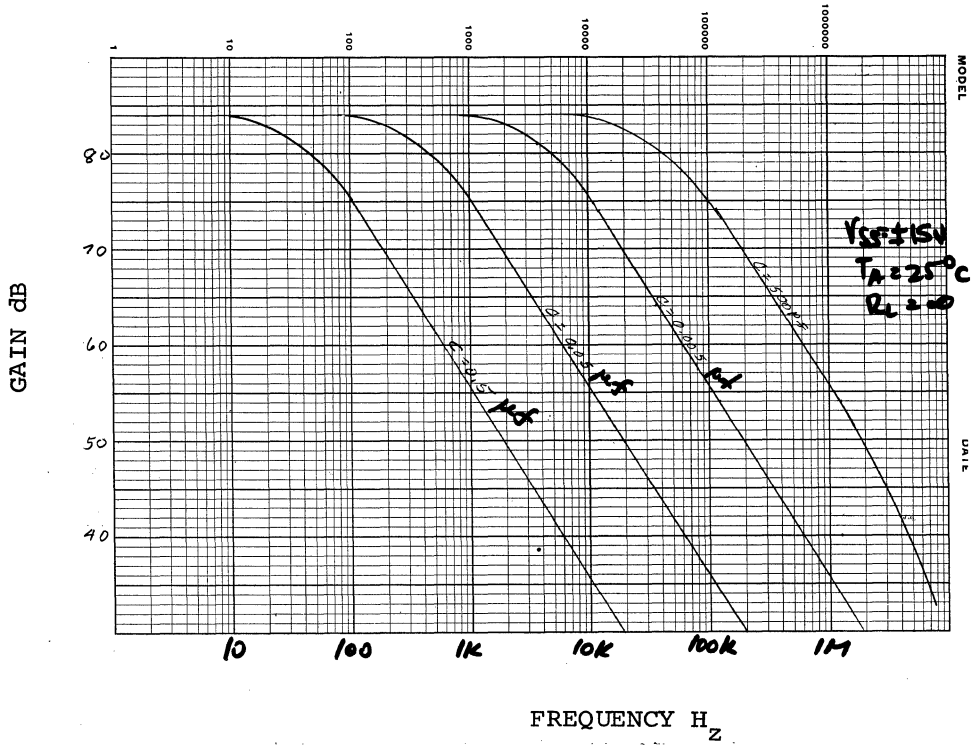


Figure 10.14B. Frequency response with second-stage lag compensation, pin 2 to ground.

Figure 10.14C. Frequency response with input compensation, pin 3 to pin 4.

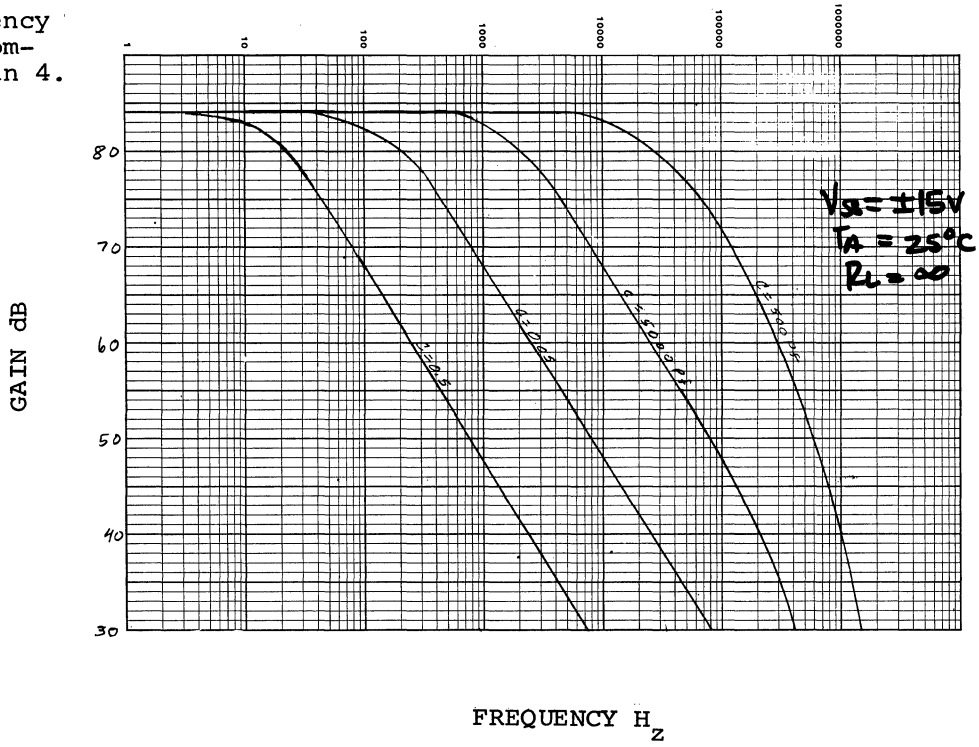
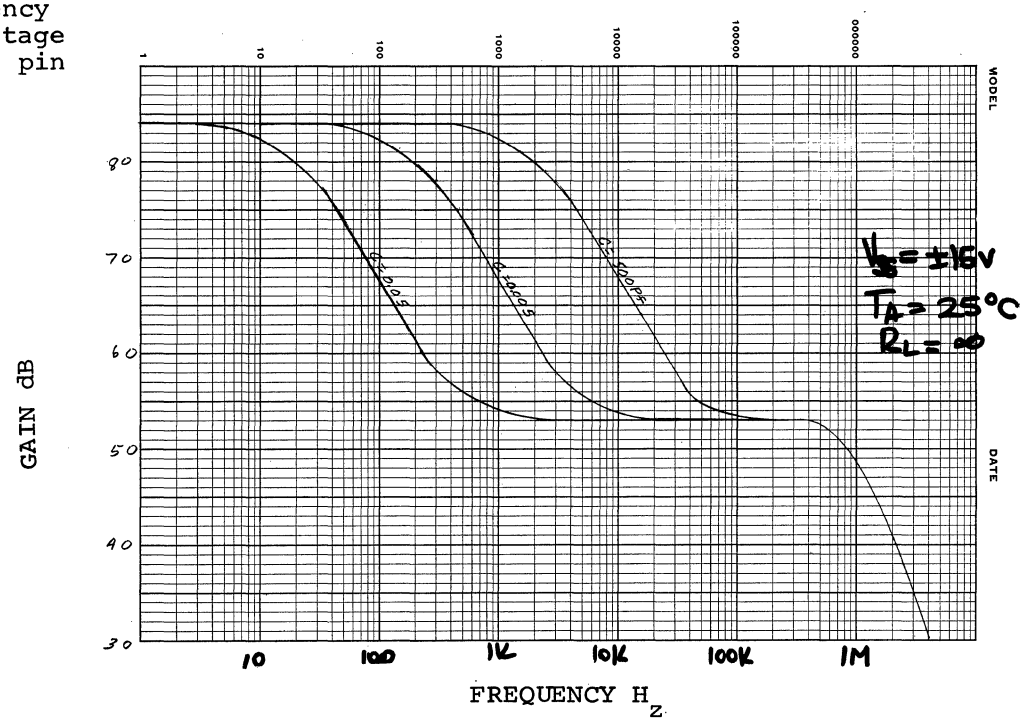


Figure 10.15A. Frequency response with second-stage feedback compensation, pin 2 to pin e.



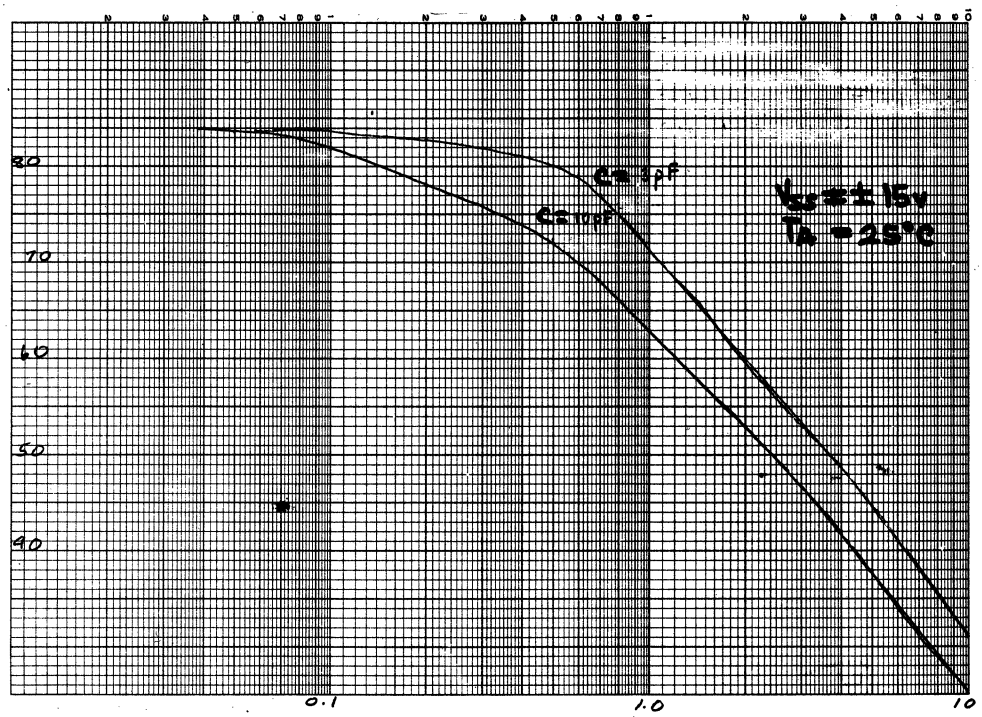
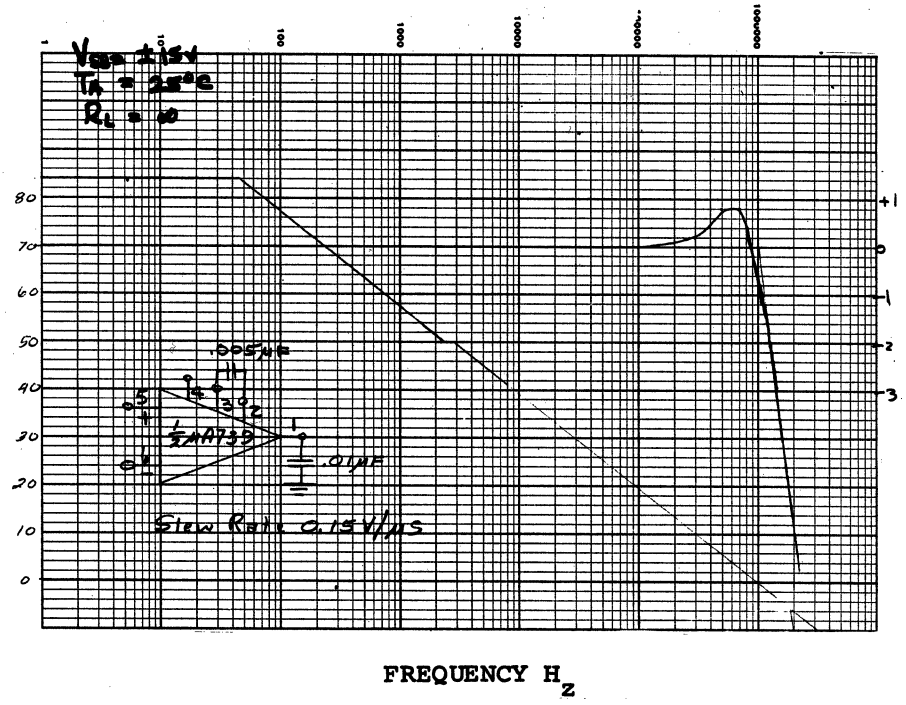


Figure 10.15B. Frequency response with output stage feedback, pin 1 to pin 2.

Figure 10.16A. Low slew-rate unity-gain frequency response.



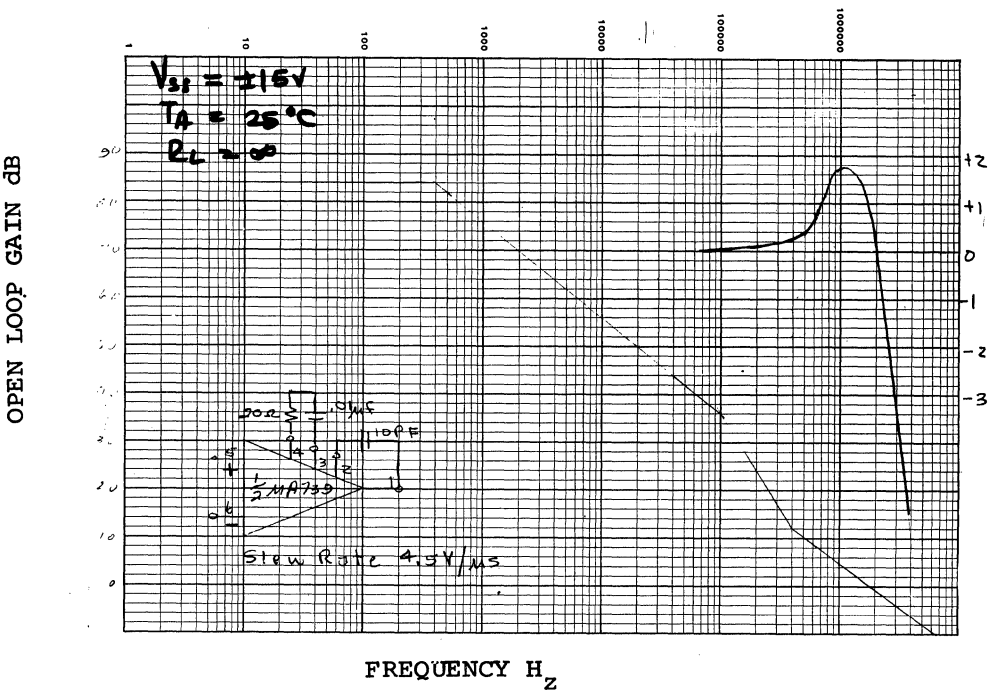


Figure 10.16B. Maximum slew-rate unity-gain frequency response.

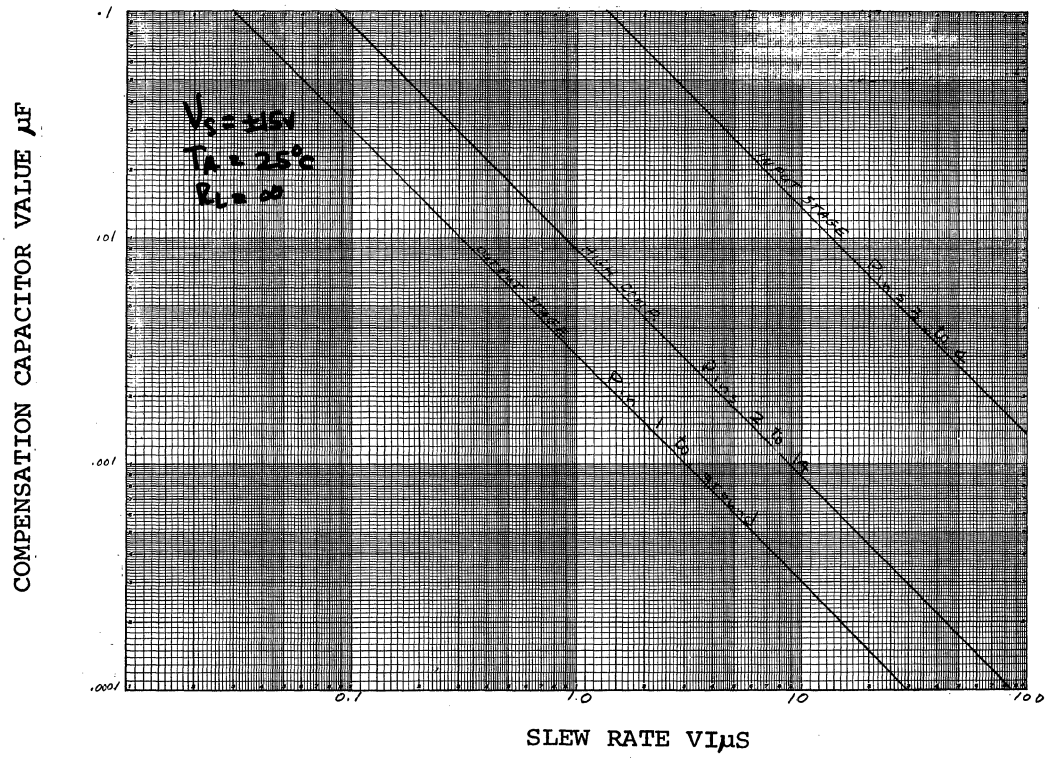


Figure 10.17. Maximum slew rate for various compensation techniques.

11

FM Detector-Limiter Integrated Circuits

by Peter H. Mack and
Norman S. Palazzini
Sprague Electric Co.

Integrated circuits can simplify designing of the limiting and detecting functions in an fm system provided the designer accepts a few changes in philosophy. The basic considerations governing the use of an integrated approach to fm detector limiter circuitry will be covered in this chapter.

The IC to be used in the design examples is the ULN-2111A, a monolithic circuit designed primarily for application in television sound systems or fm radio receivers. The main feature of its design is a quadrature detection scheme in which a simple single adjustment of the phase-shift network is all that is required to get satisfactory operation.

11.1 THE DETECTOR-LIMITER IC

The ULN-2111A uses a three-stage wide-band limiter and a full-wave balanced coincidence detector. The circuit is shown in Figure 11.1. In discussing the circuit, it is convenient to discuss the limiter, the phase-shift network and its buffering, and the FM coincidence detector.

The limiter is comprised of three identical differential-amplifier stages (1, 2 and 3 in Figure 11.1) which are direct-coupled through emitter followers. The direct coupling of the three-stage limiter is possible by using an internal stabilized voltage reference (a five-diode series string), dc level shifting between stages and overall d-c negative feedback. The external capacitors C_2 and C_3 eliminate the strong negative feedback in the frequency band of interest (4.5 to 10 MHz), and provide dc stabilization. For flexibility in driving the different phase-shift networks, two limiter outputs are made available. The full square-wave voltage output of 1.4 v_{pp} is applied directly to gate 4 of the coincidence detector. The other output provides a -20 dB replica of the signal.

In the configuration shown in Figure 11.1, the signal from the amplifier is picked off at pin 9 and applied through a small capacitance, to a parallel tuned circuit.

The bias reference voltage for balancing the upper detector pairs is obtained by tying one side of the tuned quadrature network to pin 2. The signal is applied to the detector at pin 12 and is maximum at resonance of the tuned circuit.

In operation, the tuned circuit serves to apply a varying phase shifted signal of $\pm 90^{\circ}$ as the fm carrier deviates around the designated center frequency. The detector is double balanced at lower and upper detector pairs, thus insuring repeatability of the dc "S" curve center voltage value.

The detector is also designed to operate as a full-wave detector, thus providing higher conversion efficiency.

The complete monolithic circuit is contained on a 60 by 60 mil silicon chip. The circuit consists of 19 transistors, six diodes and 18 resistors. Of the 19 transistors used, 11 operate with a maximum collector-emitter supply of 2.8 V; the remaining

transistors operate in the common-collector mode and therefore do not require an isolated region.

11.2 APPLICATION IN FM AND TELEVISION CIRCUITRY

The basic design philosophy behind the ULN-2111A is that the function of balance should be placed in the active portion of the system rather than in the passive portion. The major difference proposed by this philosophy to preceding design approaches is that balance need not be adjustable and, consequently, restrictions associated in the design and adjustment of balanced coil detectors (such as the ratio detector) is greatly relieved.

In any system using a balanced discriminator, the major figures of merit include: audio recovery, AMR, dynamic range, and THD. Of these characteristics, only audio recovery must be adjusted to the circuit externally.

Audio recovery is effected primarily by the resonant simple-LC network and the injection value at the detector input. To obtain a proper value for audio recovery, specific characteristics of the "S" curve must be selected. Primarily, these characteristics resolve to a choice of slope of the "S" curve giving a specified value for $\Delta V/\Delta F$ which is the basic expression of audio recovery. Two values must be chosen: (1) the peak-to-peak separation desired, and (2) the peak-to-peak voltage required at the nodes of the "S" curve.

The peak-to-peak separation is usually defined by the service for which the system is intended. For fm, this value is 550 kHz and for television, it is 150 kHz. Once the choice is made, and the center frequency, as well as the peak-to-peak separation is known, an approximation of the circuit Q can be made, by using:

$$Q = \frac{F}{FO}, \quad Q = \frac{F_O}{\Delta F} \tag{11.1}$$

For television applications, the value of the circuit Q is approximately:

$$Q = \frac{4.5 \times 10^6}{150 \times 10^3} = 30$$

Although the desired circuit Q is fairly low (indicating a high-L network), it is desirable to use a high-C network. The input to the detector will introduce some variable capacitance. This can be minimized through the use of at least 100 pF as the C part of the resonant circuit. The inductor chosen along with this capacitance value will yield a network with a Q somewhat higher than desired. This should be reduced through use of a parallel resistor across the network. Figure 11.2 shows complete quadrature networks for television and fm circuitry. Optimum component values are given in the figure.

The final component required is a small decoupling capacitor placed between the network and the low amplifier output. To insure linear detector operation, the reactance of this capacitor should be substantially large as compared to the impedance of the tuned circuit at resonance.

The other factor governing the audio output is the injection value at the input to the detector. The optimum value is 60 mV rms at the resonant frequency of the network. Figure 11.3 shows a normalized plot of V_{inj} vs. V_f where V_f represents a normalized output for any simple LC network. Note that the output (V_f) has a linear relationship with V_{inj} up to approximately 50 mV. Above this value, the function breaks into a curve, then flattens out, indicating that the detector is in a switching mode.

Figure 11.4A and 11.4B demonstrate the detector operation in the linear (low injection) mode and the switching (high injection) mode. Note that in the linear mode, a greater portion of the "S" curve is linear, thus producing lower distortion than in the switching mode. For best operation, the low injection mode is recommended with V_{inj} set as high as possible. The optimum injection value is 60 mV_{RMS}.

To complete the circuit, it is necessary to select a de-emphasis capacitor and several bypass capacitors. The de-emphasis capacitor should have a time constant of 75 μs. Satisfactory results will be obtained with a value in the range of 0.01 μF to 0.05 μF. The bypasses are not critical and any value from 0.05 μF to 0.1 μF will do. As with any bypass capacitor, the objective is to keep the reactance as low as possible. A noninductive, ceramic capacitor is best in this application. The amplifier and detector inputs are designed to operate at dc bias levels provided by a part of the diode divider chain in the device. In both cases (See Figure 11.2), it is intended that a coil, or part of a transformer, be used as a low dc resistance path between the bias source and the respective input connection, thus providing the bias level required. For best operation, the dc resistance value should be as low as possible. Values of 100 to 300 Ω are quite satisfactory.

The amplifier will tolerate a considerable dynamic range at the input. The minimum level of input is approximately 1.0 mV for good AMR rejection and effective clipping. The maximum input swing is limited by the collector-base diode of the input transistor. In the circuit of Figure 11.2, the maximum peak swing should be limited to about 1.5 V. The dynamic tolerable range will then in excess of 60 dB, which is more than adequate for satisfactory performance.

The detector output loading is not critical. The source resistance is quite low (on the order of 200 Ω). To prevent clipping at the output when the a-c load impedance is less than 2000 Ω, a 1000-Ω resistor should be added between the output and the ground.

Tuning the device in a system is quite simple. Two alternatives are available: (1) Tune the receiver to a strong station and then tune the quadrature coil to maximum audio output, or (2) Apply an fm generator to the amplifier input through a small decoupling capacitor, and tune as above.

The circuit layout should be carried out with reasonable care inasmuch as the device has an inherent high gain and high bandpass characteristics. It is important to separate the input and output components to prevent undesired coupling which may cause oscillation.

The ULN-2111A is a simple circuit to use. Balance and symmetry are a function of the monolithic circuit, thus relieving the system designer of many restrictions normally found in other methods of detection.

Tuning adjustment has been simplified to the point where special equipment is not required in the field to give the desired results. Operation can be assured after any maintenance cycle with reasonable confidence.

11.3 TWO-BLOCK FM IF STRIP

An i-f strip for use in fm Receiver Applications can be designed by using a pair of ULN-2111A ICs. The availability of inexpensive ceramic filters has generated considerable interest in fixed tuned nonadjustable i-f strips. The advantages of such i-f strips are simplicity, smaller space requirements and lower production costs. The circuit diagram for the ULN-2111A is shown in Figure 11.1. Figure 11.5 shows the same circuit but with certain modifications to improve its gain for use as the first of two series gain blocks. The connections shown are wired externally. Since the detector section is not required in the first gain block, conversion of the detector to an additional stage of gain will increase amplification available by 10 dB. This is accomplished by unbalancing the detector by grounding pin 12 and broadbanding by reducing the collector load from 10 kΩ to 1 kΩ. The two blocks in series will produce a maximum of 130 dB of gain which represents a net 100 dB gain after insertion losses of approximately 30 dB are subtracted for filtering.

Figure 11.6 shows output waveforms for signal input levels from 3 μV to 200 μV. The source generator is a Boonton 202H developing a low-distortion sine-wave-modulated fm signal of 75 kHz deviation. Note that at low levels of signal, a white-noise component will appear indicating that a high noise level will appear when the incoming signal disappears. A simple solution to this problem will be to include in the receiver a squelch switch controlled by detected noise. Figure 11.7 shows a diagram for a two-block i-f stage. The second block is hooked up as a standard quadrature detector. De-emphasis of 75 μs is supplied by a .001 μF capacitor at pin 14. Filtering at this point will be required even for stero applications to prevent the strip from oscillating. For stero, however, this capacitor may be reduced to 100 pF which is sufficiently small to maintain satisfactory bandpass.

No provision has been made in the strip for AGC. Due to the limiting action of the amplifier and the wide dynamic input range of permissible signal range, no AGC is required for fm receiver service.

Other applications for the ULN-2111A range from supressed carrier and pulse modulation to wideband amplifiers. The following discussion will treat each of these applications separately.

11.4 SUPPRESSED CARRIER MODULATION

Suppressed carrier modulation can be provided using the ULN-2111A. The test circuit for this application is shown in Figure 11.8; the waveforms sampled at the output, are shown in Figure 11.9. In the waveform in Figure 11.9A the carrier frequency is 50 kHz and the modulator frequency is 3 kHz. At this low frequency, the feedback capacitor is changed to 6.7 μF as shown in Figure 11.8. This value is necessary so that a 55 dB gain is realized in the amplifier section at low frequencies.

At higher frequencies, as shown in the waveform of Figure 11.9B, the carrier frequency is 5 MHz and the modulating frequency is 5 kHz. At these frequencies, the

value of C_f can be 0.05 μF. A plot of frequency vs. gain for different values of C_f is shown in the wideband amplifier illustrations, Figures 11.19 and 11.20.

In the circuit diagram in Figure 11.8, the modulating signal input is at pin 12. A phase-shift network is not a requirement. Instead, a 50-Ω resistor is placed between pins 2 and 12 to insure proper bias to the input of the gate detector. By adjusting the dc bias of the gate where the modulation is applied, full carrier suppression is achieved. The 0.1-μF capacitor placed between pin 2 and ground decouples the limiter supply. Since the input to the limiter is floating, consequently requiring a dc reference, a 50-Ω resistor is used between pins 4 and 6. This resistor can be of any value from 50 to 200 Ω. This dc reference is provided by the diode supply line which must be decoupled by an external capacitor from pin 6 to ground. This avoids regeneration between bases through insufficient base-source impedance.

11.5 PULSE MODULATION

A pulse modulation circuit is illustrated in Figure 11.10; the waveforms are given in Figure 11.11.

In data transmission systems, for which service the circuit in the figure is designed, the pulse is applied to pin 12. No phase-shift requirement exists. The value of C_f is 0.05 μF and a 3000-Ω resistor is placed between pin 14 and V_{cc} to increase the bandwidth. Figure 11.11A and 11.11B show the waveforms produced by the following conditions: F_1 = 20 MHz, F_2 = 1 MHz, Pulse Width = 20 μs and F_1 = 20 MHz, F_2 = 1 MHz, Pulse Width = 200 Ωs.

11.6 BALANCED PRODUCT MIXER

Figure 11.12 and 11.13 show the circuit diagram and waveforms for a balanced product mixer. Mixing between two signals at 10 MHz and 11 MHz was tried with the results shown in Figure 11.13A and 11.13B. The actual video bandwidth after conversion is limited to 2.6 MHz and can be increased to 10 MHz by simply adding a 3000-Ω external resistor between pin 14 and V_{cc}.

11.7 SYNCHRONOUS AM DETECTION WITH CARRIER RECOVERY

Figure 11.14 shows the circuit diagram for the synchronous a-m detector. When the carrier reference is available, the ULN-2111A can be operated directly as a synchronous detector. As such, it can recover the envelope of an a-m signal either with or without the carrier, and with double sideband or single sideband.

When the pilot carrier is absent, the envelope should be recovered by operating on the sidebands. One application is the color demodulator in color television sets. In the case of a double sideband signal with carrier, the carrier has been recovered by simple symmetrical limiting. The modulated signal is applied to both inputs simultaneously. One channel will limit the signal providing the zero crossing reference, while the other operates linearly, preserving the envelope.

The recovered envelope for a 90-percent signal of 100 mV rms at different frequencies, is shown in Figure 11.15. The dips are due at 90° and 270° phase shifts in the limiter. Photographs of the recovered envelope for different frequencies are shown in Figure 11.16. This type of detector has many advantages over the envelope detector in current television receivers. For example, elimination of the distortion due to the single

sideband transmission, elimination of sound buzz, chroma beats, etc., are a few of the advantages of this detection system.

11.8 PHASE COMPARATOR

The coincidence-gated detector is actually a phase comparator. It can be used for a variety of servo-loops with automatic phase controlling, such as in chroma and horizontal synchronization processing. Figure 11.17 shows the circuit diagram for measuring the output voltage when e_{in_2} is phase-shifted from e_{in_1}. A plot of the output voltage vs. phase shift is given in Figure 11.18. The frequency employed is 4.5 MHz. The voltage input to e_{in_2} must be at least 0.2 V RMS to insure proper operation of the detector network.

11.9 WIDEBAND AMPLIFIER

The three-stage limiter can be used as a wideband amplifier. Figure 11.19 shows the effects of C_{fb} on gain and frequency. The circuit diagram and curves for C_{fb} = 0.05 μF and 6.8 μF are also shown. The normal output voltage at pin 10 would be 0.3 V rms. Figure 11.20 illustrates the effects of increasing C_{fb} to 47 μF. In both cases, good, symmetrical limiting will result.

FIGURES

Figure 11.1. Circuit diagram for ULN-2111A fm detector and limiter integrated circuit.

Figure 11.2. Quadrature network for television and fm receivers: (A) circuit diagram; (B) chart of component values for operation at 4.5 MHz, (television) and 10.7 MHz (fm).

Figure 11.3. Conversion efficiency V_F as a function of injection voltage V_{ij}.

Figure 11.4. Transfer characteristics (fm) operation for (A) low injection voltage and (B) high injection voltage.

Figure 11.5. ULN2111A modified for use as wideband amplifier.

Figure 11.6. Output waveforms for two-block i-f strip.

Figure 11.7. Diagram of two-block i-f strip.

Figure 11.8. Circuit diagram for suppressed carrier modulator .

Figure 11.9. Suppressed carrier modulator waveforms for operation with V_{cc} = +12 V: (A) carrier frequency = 50 kHz, modulator frequency = 3 kHz; (B) carrier frequency = 5 MHz, modulator frequency = 5 kHz. Amplitude = 1 V/cm.

Figure 11.10. Pulse modulator circuit diagram.

Figure 11.11. Pulse modulator waveforms: (A) F_1 = 20 MHz at 20 mV, F_2 = 20 MHz at .5 V, pulse width = 2 ns; (B) F_1 = 20 MHz at 20 mV, F_2 = 1 MHz at .5V, pulse width = 200 ns.

Figure 11.12. Balanced product mixer circuit diagram.

Figure 11.13. Waveforms for balanced product mixer: (A) V_1 = 11 MHz at 80 mV (upper waveform, V_2 = 10 MHz at 30 mV (lower waveform); (B) V_{out} = 1 MHz. Amplitude = 1.5 V/cm.

Figure 11.14. Circuit diagram for synchronous a-m detection with carrier frequency.

Figure 11.15. Output voltage vs carrier frequency.

Figure 11.16. Waveforms for synchronous a-m detection with carrier recovery:

(A) modulating frequency = 400 Hz, carrier frequency = 1 MHz, input amplitude = 600 mVp-p, output amplitude = 2 Vp-p; (B) modulating frequency = 400 Hz, carrier frequency = 4.5 MHz, input amplitude = 600 mVp-p, output amplitude = 2 Vp-p.

Figure 11.17. Phase comparator circuit diagram.

Figure 11.18. Phase shift vs output voltage for phase comparator circuit.

Figure 11.19. Wideband amplifier circuit and waveforms.

Figure 11.20. Wideband amplifier operated with C_{fb} = 47 mF.

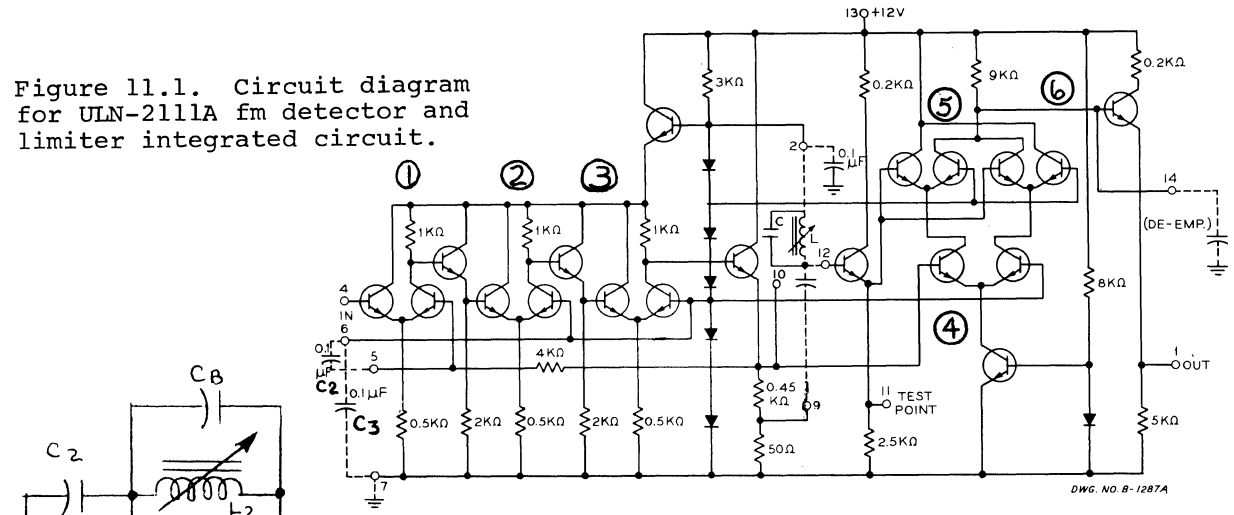


Figure 11.1. Circuit diagram for ULN-2111A fm detector and limiter integrated circuit.

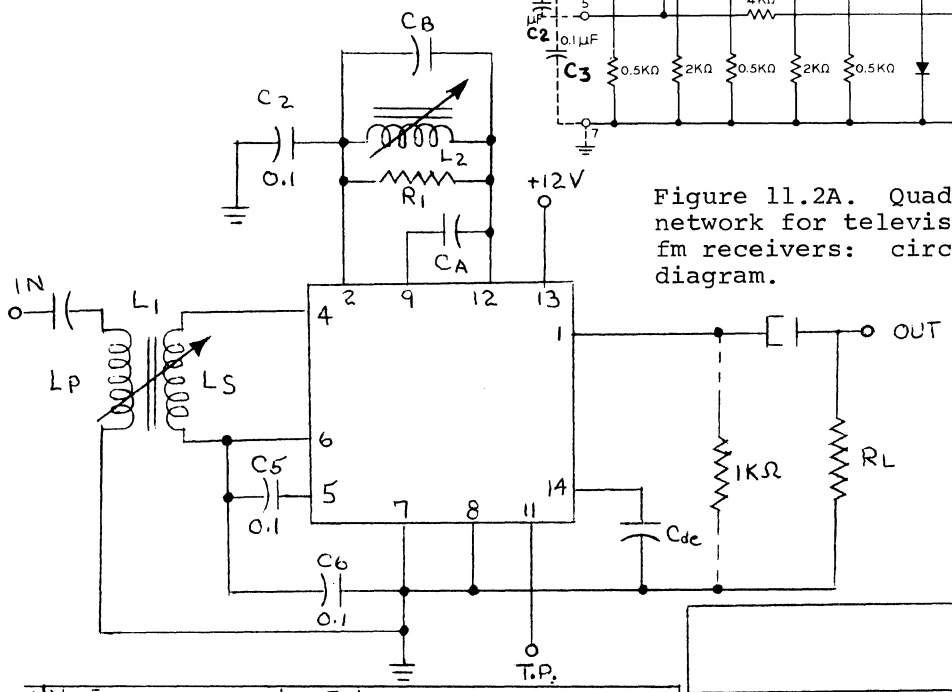


Figure 11.2A. Quadrature network for television and fm receivers: circuit diagram.

Figure 11.2B. Quadrature network for television and fm receivers: chart of component values for operation at 4.5 MHz, (television) and 10.7 MHz (fm).

	Component Value		
	T.V. (4.5 MHz)	FM (10.7 MHz)	Notes
L_2 Inductance	7-14 μH	1.5-3 μH	1
L_2 Nom. Unloaded Q	50	50	—
L_2 Nom D-C Resistance	50 Ω	50 Ω	—
C_A	3.0 pF	4.7 pF	—
C_B	120 pF	120 pF	2
R_1	20 KΩ	3.1 KΩ	—
Loaded Network Q	30	20	—
C_5 and C_6	0.1 μF	0.1 μF	—
C_2	0.1 μF	0.1 μF	—
C_{de}	0.01 μF	0.01 μF	—

Component values for Figure 11.2B

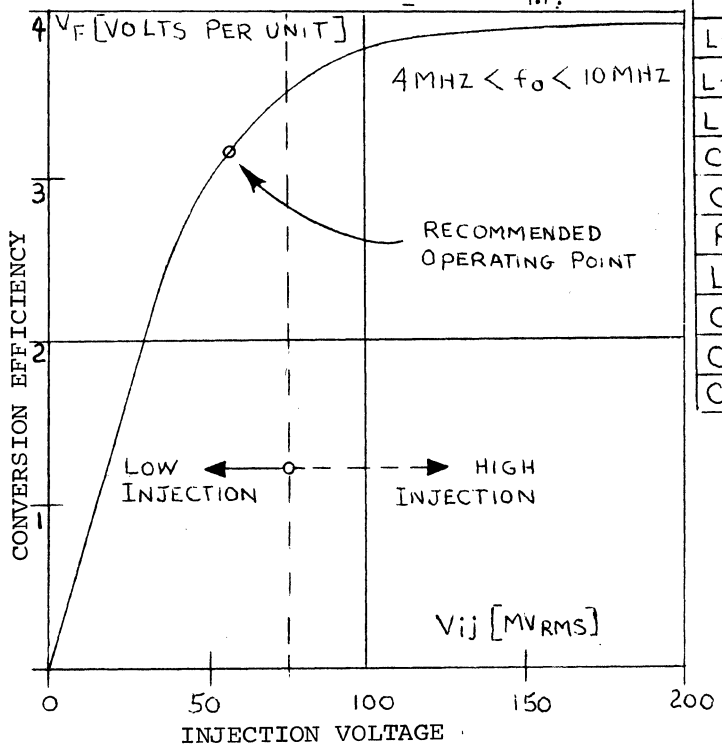


Figure 11.3. Conversion efficiency V_F as a function of injection voltage V_{ij}.

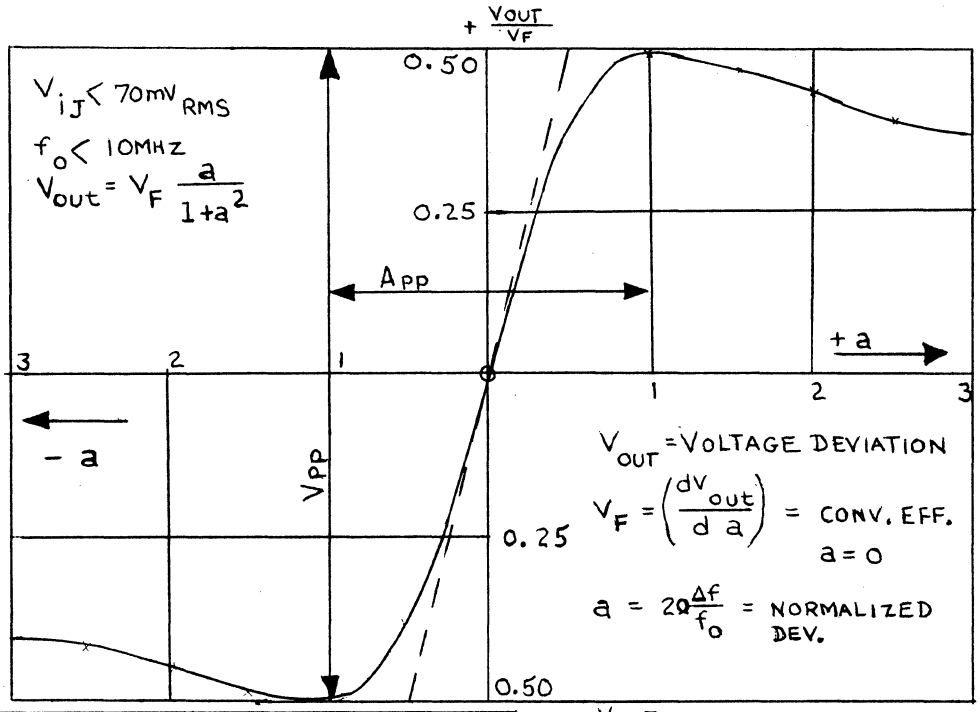


Figure 11.4A. Transfer characteristics (fm) operation for low injection voltage.

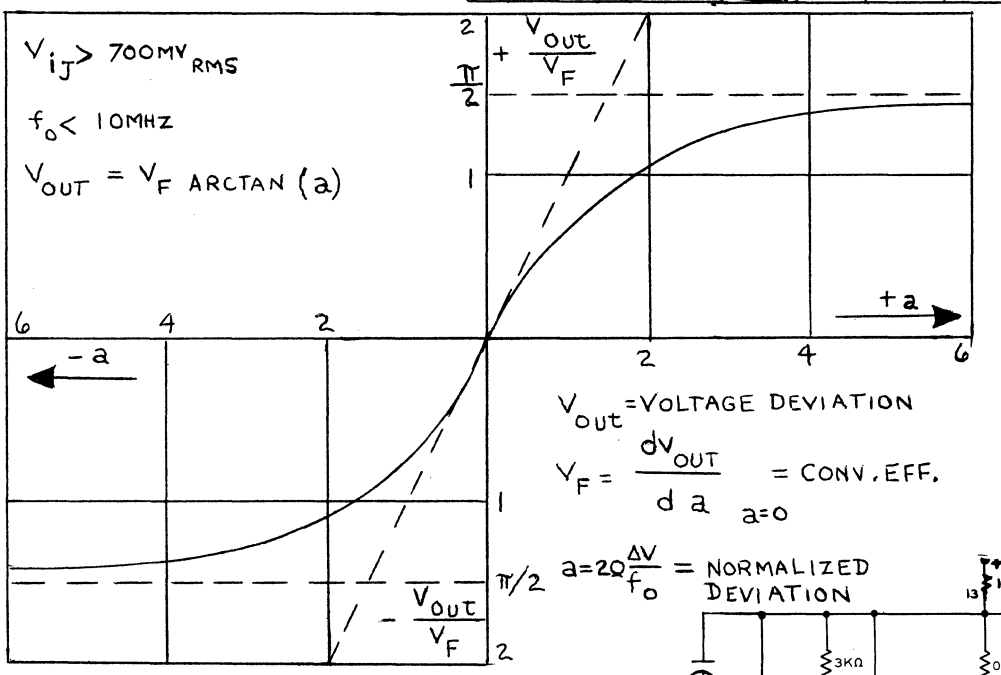


Figure 11.4B. Transfer characteristics (fm) operation for high injection voltage.

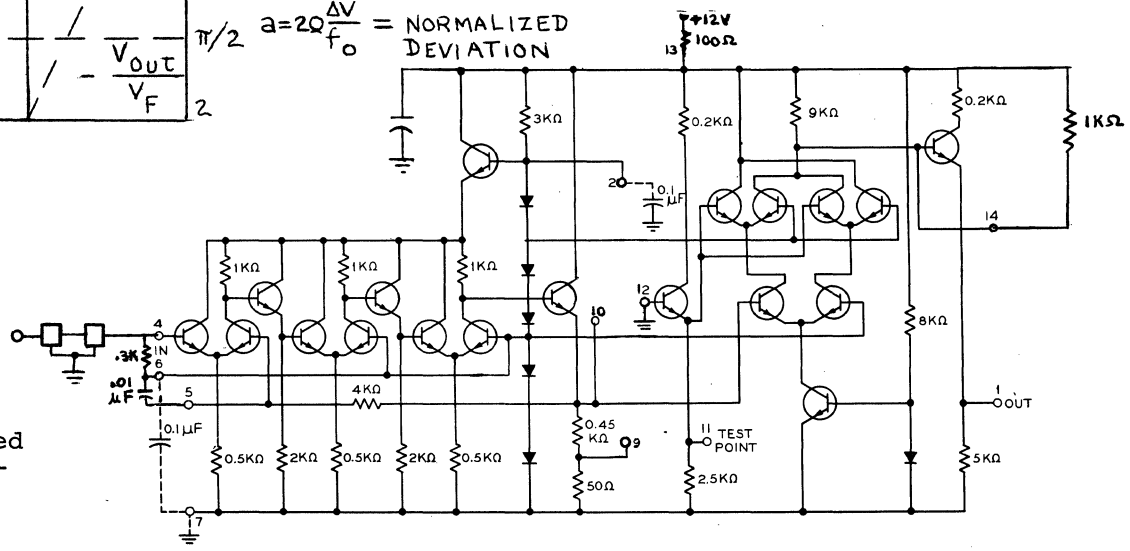
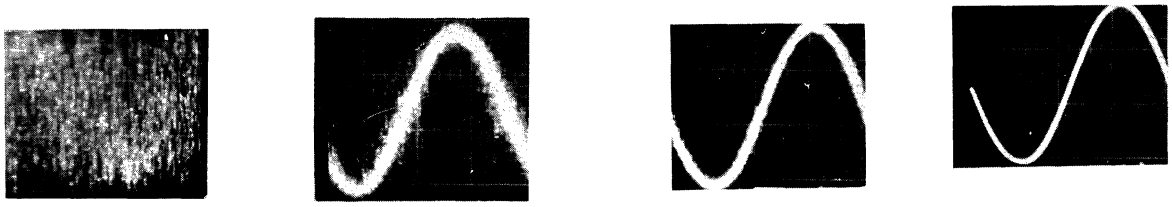


Figure 11.5. ULN2111A modified for use as wide-band amplifier.



Vin = 3uV Vin = 10uV Vin = 20uV Vin = 200uV

Figure 11.6. Output waveforms for two-block i-f strip.

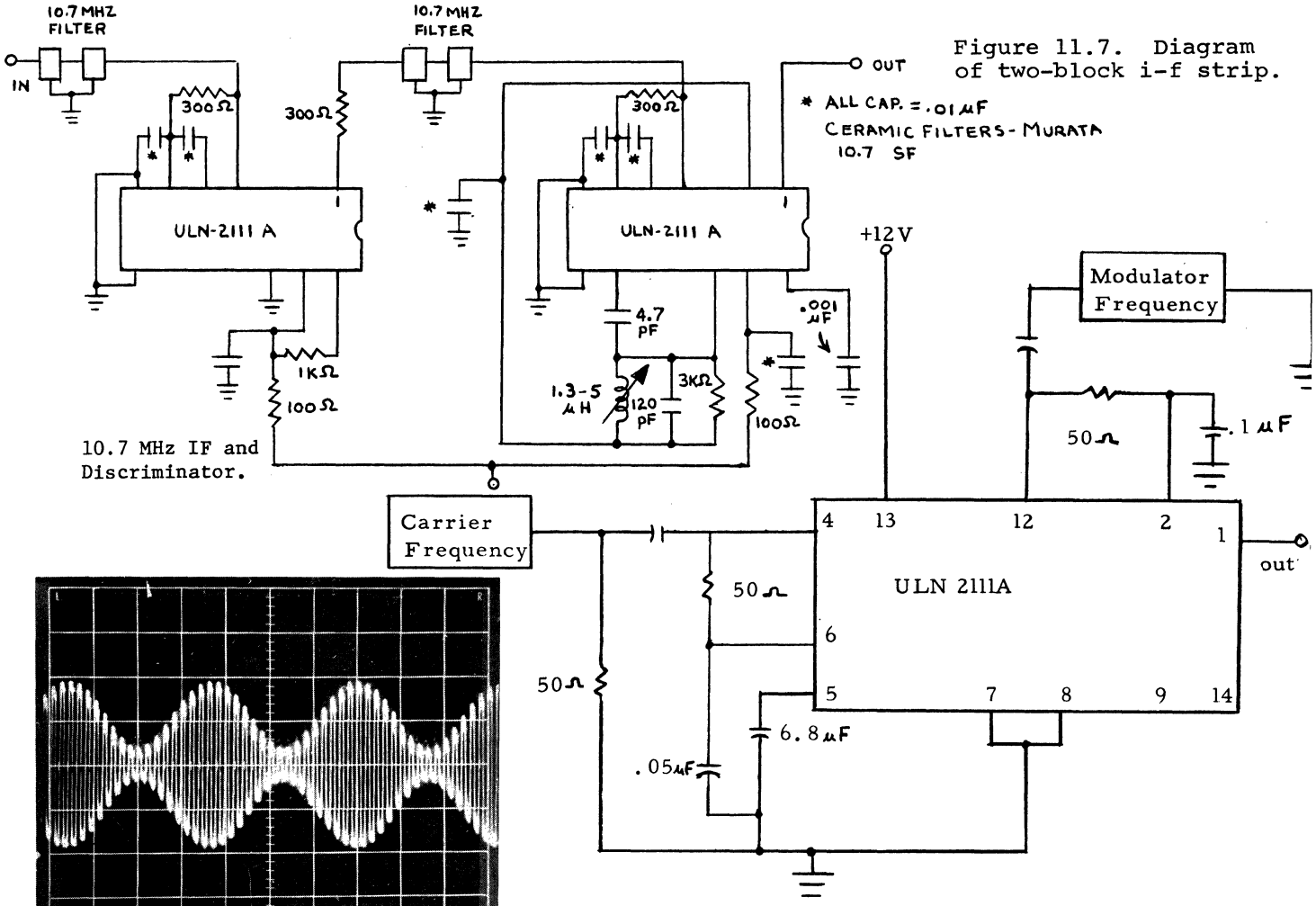
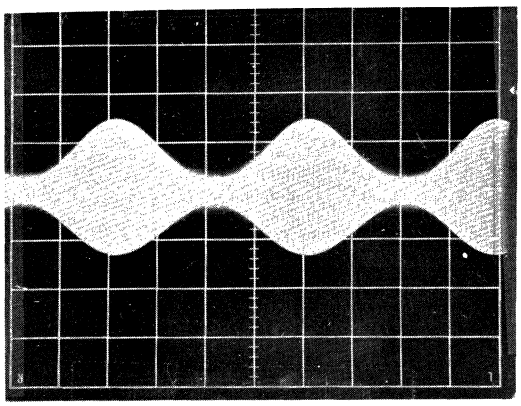


Figure 11.7. Diagram of two-block i-f strip.

(A)

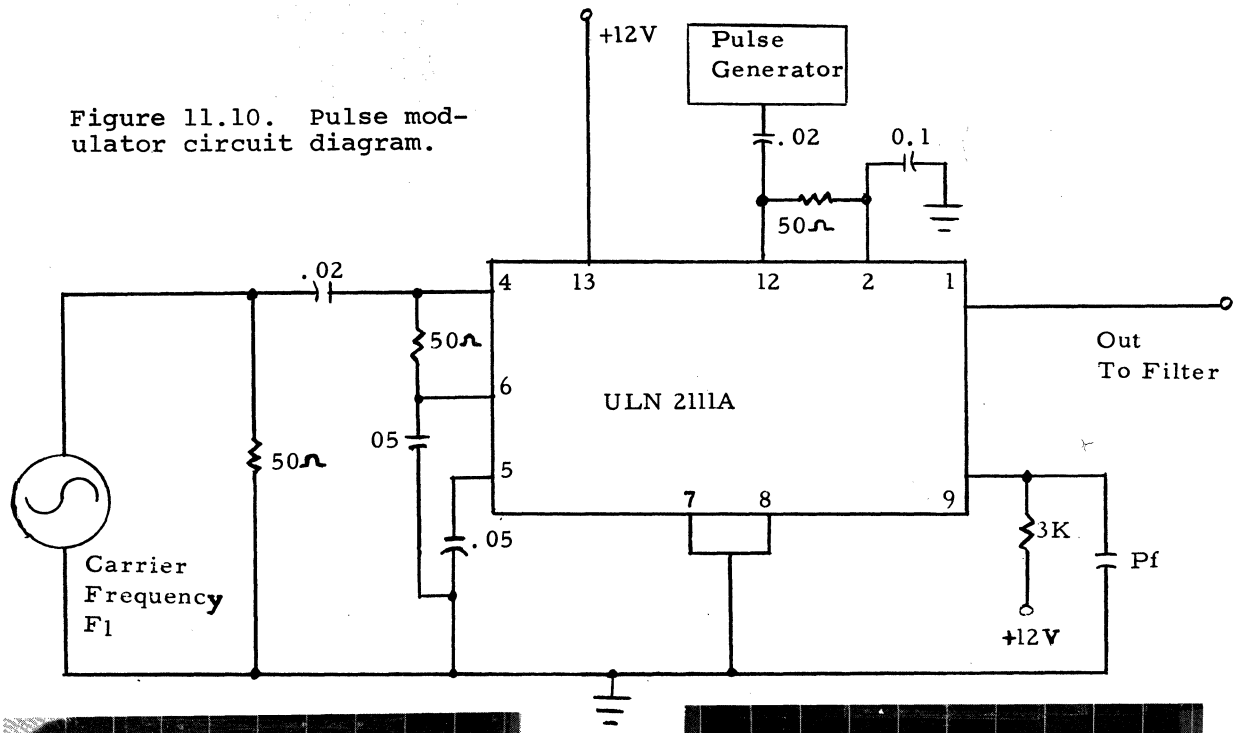


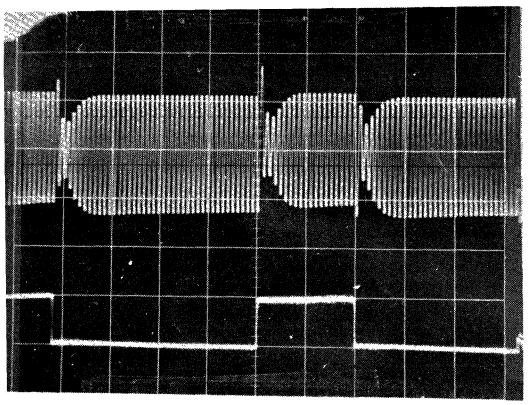
(B)

Figure 11.8. Circuit diagram for suppressed carrier modulator.

Figure 11.9. Suppressed carrier modulator waveforms for operation with V_{cc} = +12V: (A) carrier frequency = 50 kHz, modulator frequency = 3 kHz; (B) carrier frequency = 5 MHz, modulator frequency = 5 kHz. Amplitude = 1 V/cm.

Figure 11.10. Pulse modulator circuit diagram.





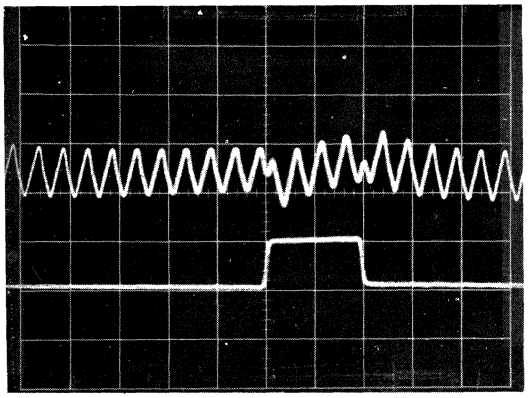


Figure 11.11. Pulse modulator waveforms: (A) F_1 = 20 MHz at 20 mV, F_2 = 20 MHz at .5V, pulse width = 2 ns; (B) F_1 = 20 MHz at 20 mV, F_2 = 1 MHz at .5V, pulse width = 200 ns.

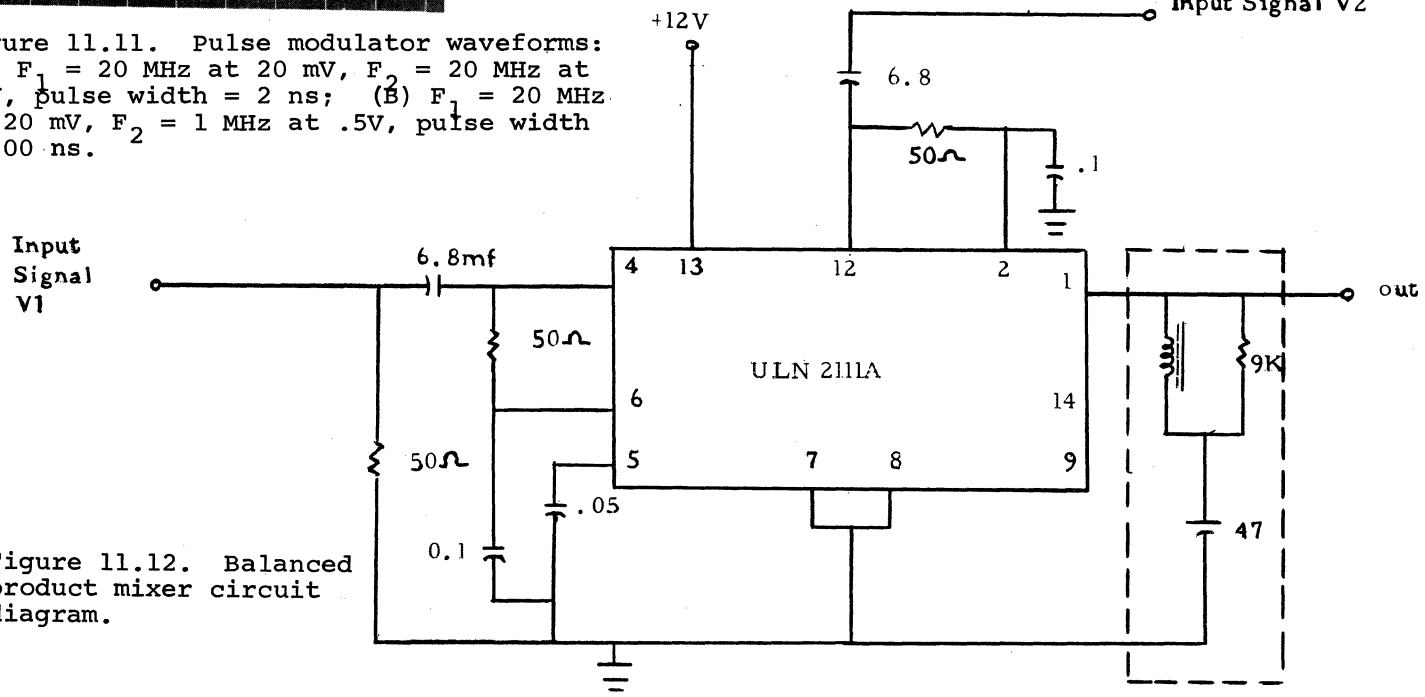
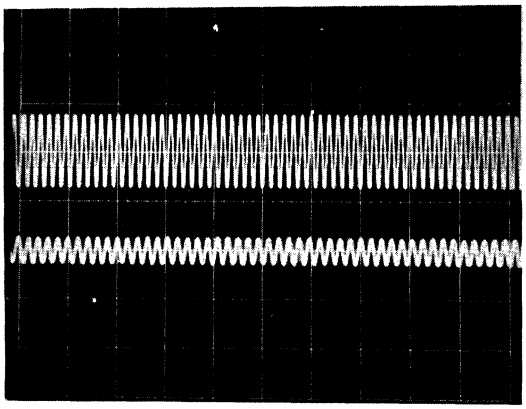


Figure 11.12. Balanced product mixer circuit diagram.



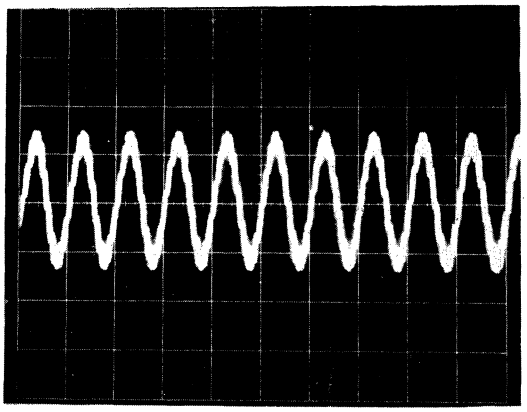
(A) V_1 = 11 MHz at 80 mV (upper waveform), V_2 = 10 MHz at 30 mV (lower waveform).

Figure 11.13. Waveforms for balanced product mixer:

V_1

V_2

V_{out}



(B) V_{out} = 1 MHz. Amplitude = 1.5 V/cm.

Figure 11.14. Circuit diagram for synchronous a-m detection with carrier frequency.

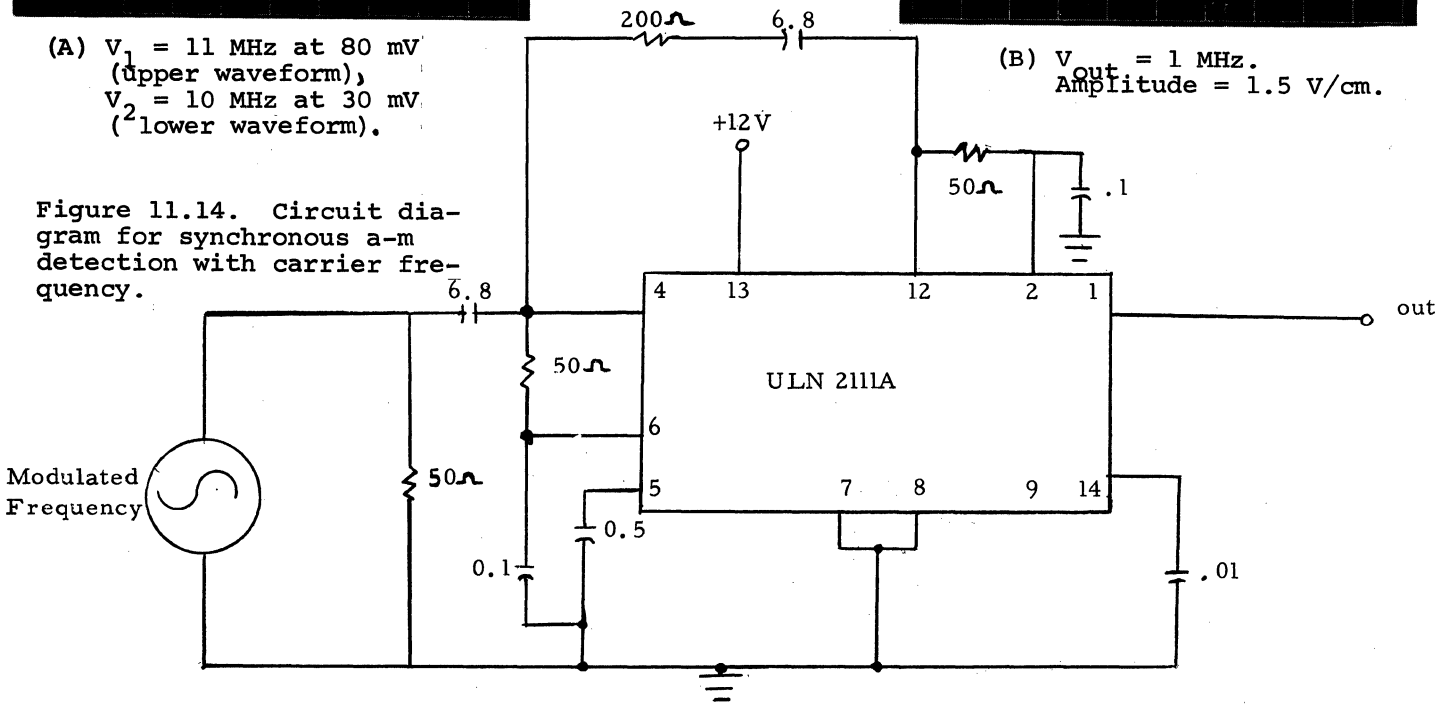
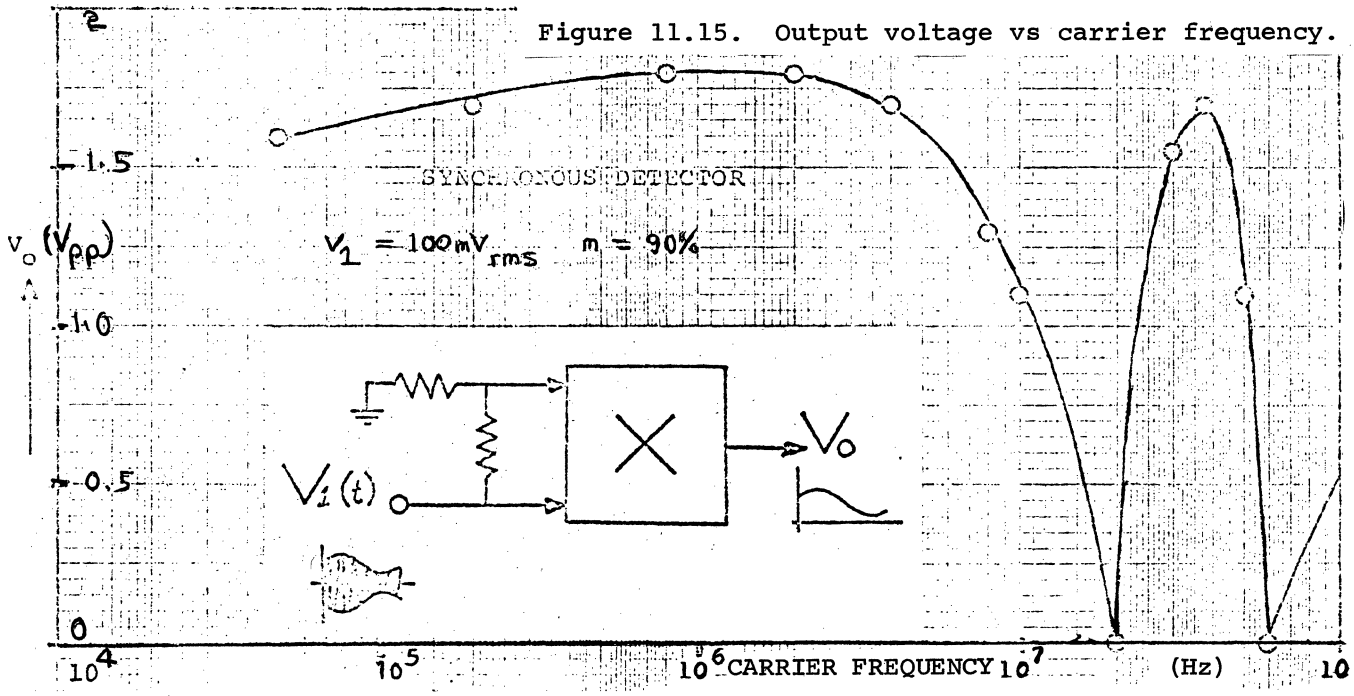


Figure 11.15. Output voltage vs carrier frequency.



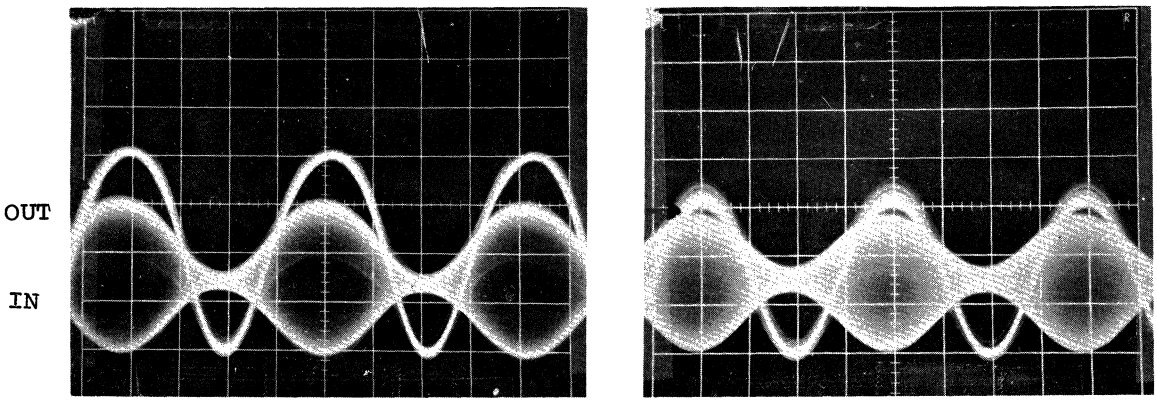


Fig. 11.16B
modulating frequency
= 400 Hz
carrier frequency
= 4.5 MHz
input amplitude
= 600 mVp-p
output amplitude
= 2 Vp-p

Figure 11.16. Waveforms for synchronous a-m detection with carrier recovery:
(A) modulating frequency = 400 Hz
carrier frequency = 1 MHz
input amplitude = 600 mVp-p
output amplitude = 2 Vp-p

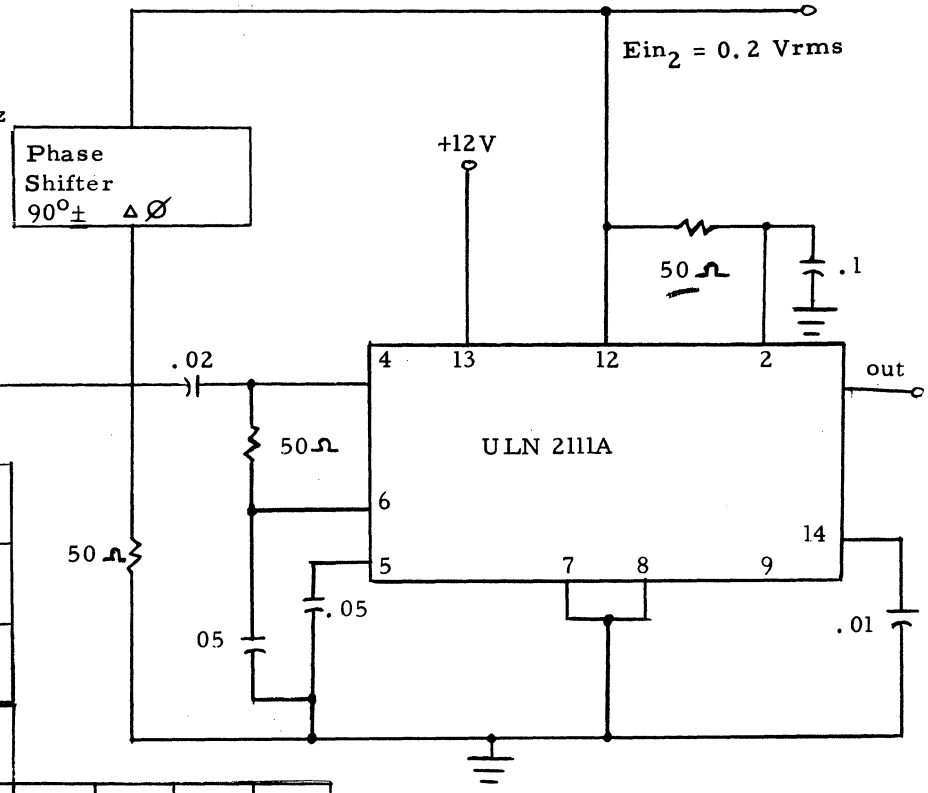


Figure 11.17. Phase comparator circuit diagram.

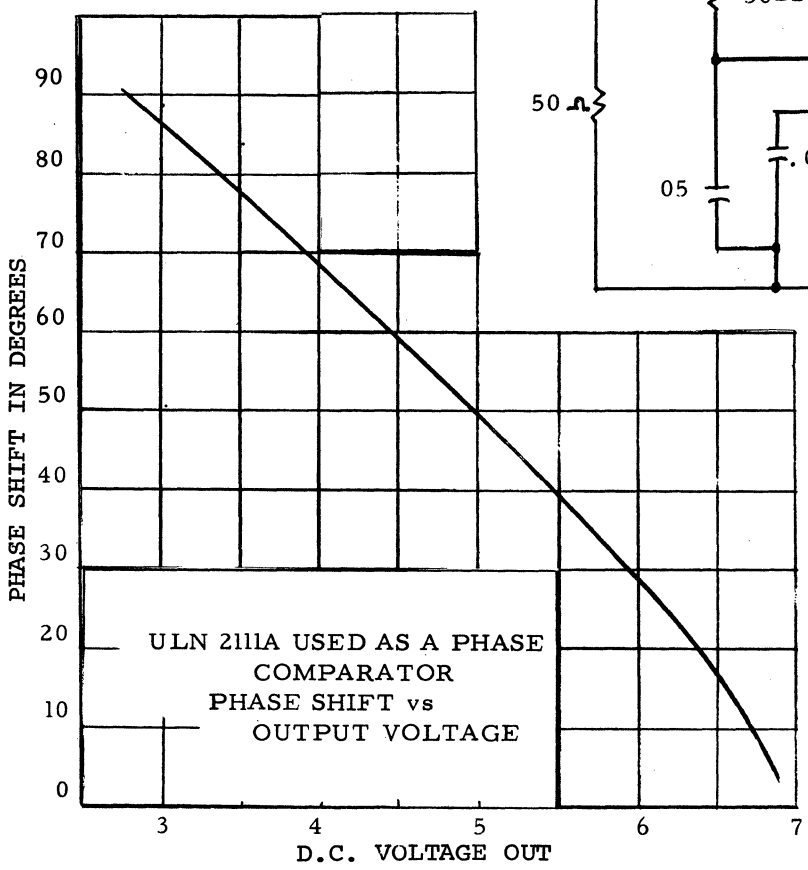


Figure 11.18. Phase shift vs output voltage for phase comparator circuit.

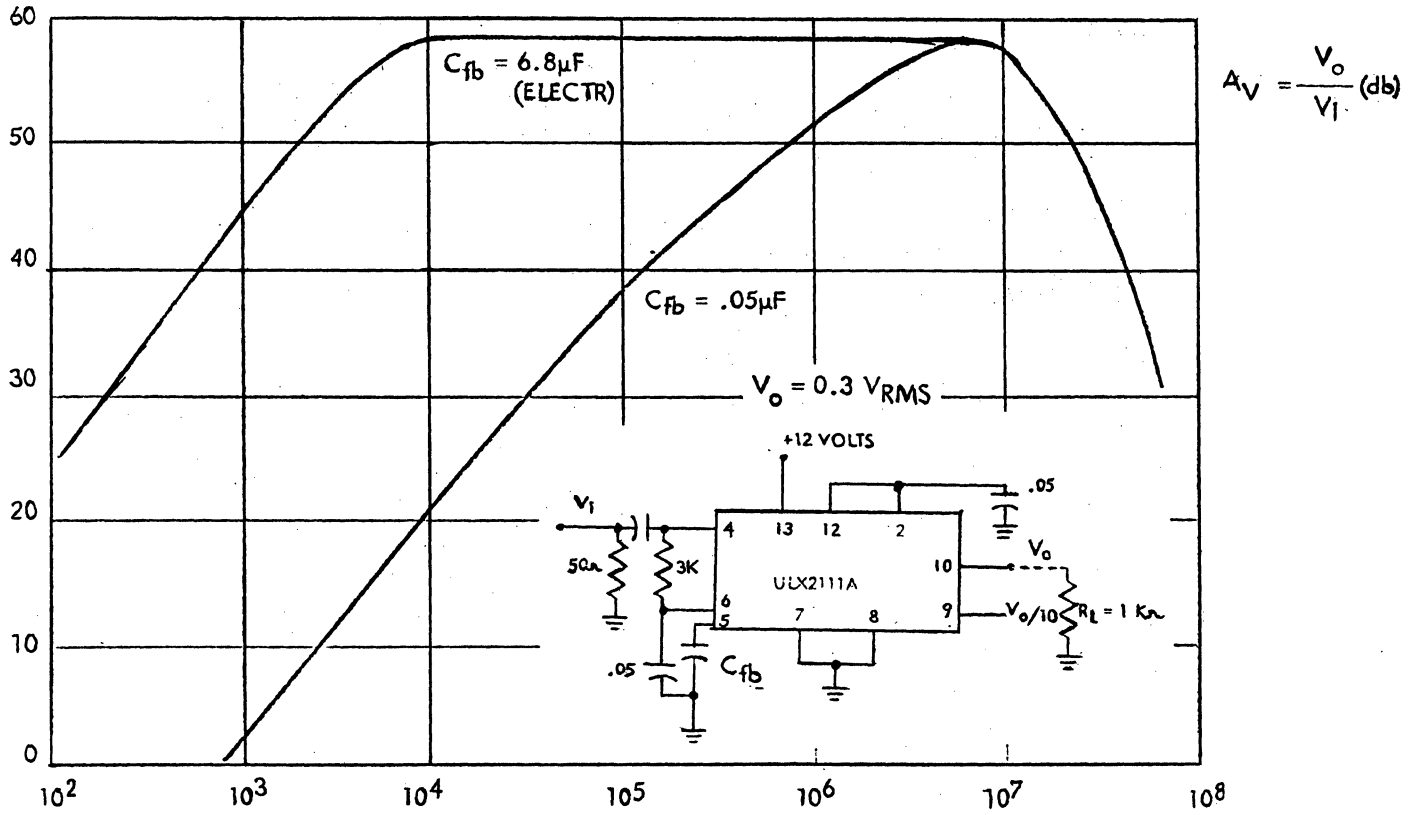


Figure 11.19. Wideband amplifier circuit and waveforms.

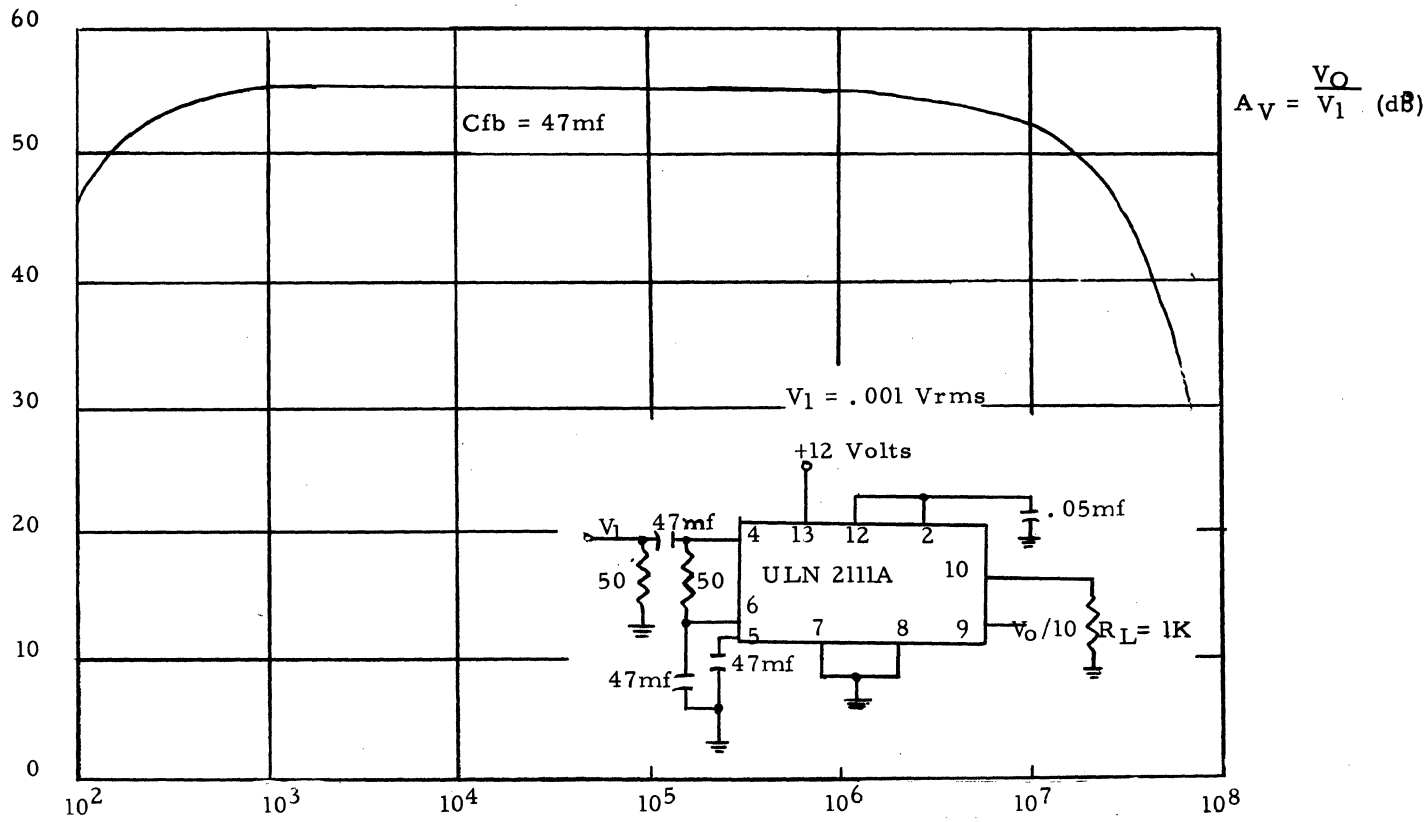


Figure 11.20. Wideband amplifier operated with C_{fb} = 47 mF.

12

The Linear Four-Quadrant Multiplier

by Ed Renschler
Motorola Semiconductor

At the 1968 EEE Linear IC Clinic (March 21, 1968, New York City), Jim Solomon of Motorola made two predictions. First, he forecast that 1968 would be "the year of the multiplier," and, second, he predicted that the mutliplier would become the second basic analog building block (the operational amplifier was really the first basic building block for purely analog work).

With respect to his first prediction Jim spoke very wisely. 1968 was indeed a good year for packaged analog multipliers. More than a half-dozen companies introduced a four-quadrant multiplier, all with a price under $100 (1). Some vendors offered monolithic four-quadrant multipliers, taking advantage of the improved reliability and temperature characteristics offered by monolithic construction.

Solomon's second prediction, that the multiplier will become the next analog building block, seems to be rapidly becoming a reality. With the price of the multiplier coming down and the number of available devices becoming larger, more and more designers are taking advantage of the capabilities offered by the multiplier. The near future should surely prove out Jim Solomon's second prediction.

This chapter will first cover the development and analysis of a linear circuit exhibiting four-quadrant multiplier properties which are suitable for monlithic construction. After the development and analysis of the circuit has been discussed, some basic applications will be presented to demonstrate a few possible uses. Although the applications of a four-quadrant linear multiplier are virtually unlimited, it is hoped that the few applications to be covered will encourage the designer to "think multiplier".

12.1 METHODS OF ANALOG MULTIPLICATION

There are many methods by which analog multiplication can be performed (2). The following is not intended to be a complete list; it is offered as a brief comparison of techniques:

1. Hall Effect. The principle on which the Hall-Effect multiplier is based is that the voltage across a conductor is proportional to both the current through it and the strength of the magnetic field across it.

2. Magnetoresistance. A magnetoresistance multiplier is basically a Wheatstone bridge made up of flux-sensistive resistors where the two variables to be multiplied are the current in the coil producing the flux, and the voltage across the bridge.

3. Variable Transconductance. In a multiplier of the variable transconductance type, the output of a transistor amplifier depends upon the signal and the magnitude of the effective emitter resistance (common-emitter configuration assumed) which can be controlled by the emitter current magnitude. Hence, the output at the collector is proportional to the input signal times a function of the emitter current.

4. Quarter Square. This technique makes use of the mathematical identity:

$$XY = \frac{1}{4}\left[(X + Y)^2 - (X - Y)^2\right].$$

Diodes are generally used to generate the square-law functions required.

5. Pulse Height/Width. Here, an oscillator generates a train of rectangular pulses; one input modulates the height of the pulses and the other input modulates the width. The area of the pulses is then proportional to the product of the two inputs.

6. Triangle Averaging. This is a variation of the quarter-square method. Instead of the square-law functions used in the quarter-square method, quadratic functions are generated by integration of clipped triangular waveforms.

7. Logarithmic Sum. This is the technique by which an ordinary slide rule operates.

$$XY = \text{antilog}\left[\log X + \log Y\right]$$

Log and antilog functions can be easily generated using a nonlinear element in conjunction with an operational amplifier (3).

12.2 VARIABLE TRANSCONDUCTANCE

Of these seven methods of performing analog multiplication, the third (Variable Transconductance) is best suited to monolithic implementation. The concept of variable transconductance will be used in the design of analog multipliers in monolithic form.

Keeping the variable transconductance technique in mind, let's recall the classical example of analog multiplication from communication systems--that of amplitude modulation as illustrated in Figure 12.1. In Figure 12.1, ω_o represents a carrier frequency and ω_s the frequency of the modulating signal. The product as shown is

$$e_o = KE_1 \cos \omega_s t \cos \omega_o t \quad . \tag{12.1}$$

By using a trigonometric identity, Equation 12.1 becomes the familiar sum and difference spectra:

$$e_o = \frac{KE_1}{2}\left[\cos(\omega_o + \omega_s)t + \cos(\omega_o - \omega_s)t\right] . \tag{12.2}$$

Note that only the frequency characteristics and not the amplitude of the carrier is being maintained. You may recall from communication system theory that the carrier-signal zero crossings are often used to generate the switching function $S(t)$ as shown in Figure 12.2. Since the switching signal can be conveniently represented in Fourier series form as

$$S(t) = 2\sum_{n=1}^{\infty} A_n \cos n\omega_o t \tag{12.3}$$

where the Fourier coefficients are

$$A_n = \left[\frac{\text{Sin } \frac{n\pi}{2}}{\frac{n\pi}{2}} \right] \tag{12.4}$$

The product signal can be expressed as

$$\begin{aligned} e_o &= 2Ke_1(t)S(t) \\ &= 2KE_1 \text{Cos } \omega_s t \sum_{n=1}^{\infty} A_n \text{Cos } n\omega_o t \end{aligned} \tag{12.5}$$

The switching function introduces all of the odd harmonics of the carrier frequency with the harmonic amplitudes decreasing as the harmonic order increases, as shown by Equations 12.3 and 12.4. A simple model of this switching function is shown in Figure 12.3, where the switching action of S(t) is produced by a single-pole double-throw transistor switch controlled by $e_2(t)$. The switches use transistor current-mode gates with collectors so that full-wave balanced multiplication results between an input voltage $e_1(t)$ and the switching voltage $e_2(t)$.

Figure 12.4 demonstrates the basic multiplier circuit, which accomplishes the desired modulation function. As mentioned previously, the carrier signal (e_2) is best represented mathematically by the Fourier series expansion of the switching function S(t), given in Equation 12.3. In most applications an output filter is used with the multiplier to eliminate all terms in the Fourier series beyond the first. This is illustrated in Figure 12.5. After filtering, the output voltage e_o contains only the product of the two input sinusoids, with amplitude information contained in e_1 only.

The sum and difference frequencies are seen in the expression for the output by applying a trigonometric expansion. Theoretically, e_1 and e_2 appearing in the output are zero. The extent to which the e_1 and e_2 outputs are zero is a measure of how well-balanced the circuit is. In practice, a rejection of 40 to 60 dB is achieved, depending upon the frequency and the signal amplitude (4). There are many applications for a multiplier of this type; however, the circuit developed thus far does not yet truly multiply $e_1(t)$ times $e_2(t)$ since amplitude information is removed from $e_2(t)$ in the generation of the switching function, S(t). This circuit can be modified, however, to respond linearily to both inputs as illustrated in Figure 12.6. In this figure, the input voltages, x and y, are linearily multiplied to produce the product, xy, at the output.

Until recently, the fabrication of a circuit which performs this multiplication and retains reasonable linearity has not been possible using other-than-digital techniques. The reason for this is, in order to multiply, the inputs must be processed nonlinearily, and the nonlinear processing usually distorts at least one input. In the multiplier discussed here, the basic configuration described earlier is used, but the e_2 input is first nonlinearily conditioned with the complement of the nonlinearity later used in multiplication. This e_2 signal conditioning is developed, as shown in Figure 12.7,

where we first consider the collector response of a transistor to input base-emitter voltage.

In Figure 12.7, for two identical transistors as shown, an input I_1 is seen to produce an output I_2, which is approximately equal to I_1. This is achieved by first converting the input current into a voltage ϕ_1 which is logarithmically related to I_1, and then converting ϕ_1 into a current I_2, which is exponentially related to ϕ_1. Since the transistors are identical, the logarithmic operation cancels the exponential operation, and the output I_2 responds linearly to the input I_1. But note that I_1 has been processed nonlinearly through the transistor junctions. Thus, the possibility of multiplying but obtaining a linear response is quite good with monolithic processing.

Figure 12.8 shows a modified version of the balanced multiplier; here the e_2 input has been processed through a diode-transistor network to produce a linear response despite the use of nonlinear processing techniques. The original circuit responded linearly to the e_1 input, so the output is now linearly dependent upon both e_1 and e_2.

Realization of this complete multiplier circuit in monolithic form is shown in Figure 12.9, where it can be seen that the input emitter degeneration and operating currents are adjustable by the user in order to accommodate a variety of input signals and applications.

By comparing the circuits of Figure 12.4 and 12.9, it can be seen that the modulator-demodulator function shown in Figure 12.4 could easily be obtained from IC described in Figure 12.9. This can be accomplished by using a different metalization pattern and bringing out just that portion of the multiplier necessary to perform the modulation-demodulation function. The IC represented in Figure 12.9 is being produced under the designation MC1595.

12.3 ANALYSIS OF THE IC

Figure 12.10 will be used as the equivalent model for the integrated multiplier. For the purposes of this analysis, conventional assumptions have been made for simplification: (1) devices of similar geometry within a monolithic chip are assumed identical and matched, (2) transistor base currents are ignored with respect to the magnitude of collector currents; therefore, collector and emitter currents are assumed equal.

From the model of Figure 12.10, the following equations are obtained:

$$I_e + y = I_6 + I_4 \tag{12.6}$$

$$I_4 - y = I_5 + I_7 \tag{12.7}$$

$$I_A = I_6 + I_7 \tag{12.8}$$

$$I_B = I_4 + I_5 \tag{12.9}$$

$$I_4 = \frac{I_3 + y}{1 + e^{\left(\frac{\phi_1 - \phi_2}{V_T}\right)}} \tag{12.10}$$

$$I_5 = \frac{I_4 - y}{1 + e^{\left(\frac{\phi_2 - \phi_1}{V_T}\right)}} \tag{12.11}$$

$$I_6 = \frac{I_3 + y}{1 + e^{\left(\frac{\phi_2 - \phi_1}{V_T}\right)}} \tag{12.12}$$

$$I_7 = \frac{I_4 - y}{1 + e^{\left(\frac{\phi_1 - \phi_2}{V_T}\right)}} \tag{12.13}$$

where $V_T = \frac{kT}{q} \approx 26$ mV at +25°C.

For simplicity, let us define

$$m = \frac{\phi_1 - \phi_2}{V_T} \tag{12.14}$$

Substituting equations 12.10 and 12.11 into 12.9, and solving for I_B:

$$I_B = \frac{I_3(1 + e^{-m}) + I_4(1 + e^{m}) - y(e^{m} - e^{-m})}{(1 + e^{m})\ (1 + e^{-m})} \tag{12.15}$$

In a similar manner, by combining Equations 12.12 and 12.13 with 12.8, I_A can be expressed as:

$$I_A = \frac{I_3(1 + e^{m}) + I_4(1 + e^{-m}) + y(e^{m} - e^{-m})}{(1 + e^{m})\ (1 + e^{-m})} \tag{12.16}$$

Let us define a differential current as:

$$\Delta I = I_A - I_B \tag{12.17}$$

which can be rewritten as:

$$\Delta I = \frac{(e^{m} - e^{-m})\ (I_3 - I_4 + 2y)}{(1 + e^{m})\ (1 + e^{-m})} \tag{12.18}$$

Next, for diodes D_1 and D_2 in Figure 12.10 we can write the following current relationships:

$$I_1 + x = a_{11}\ (e^{\frac{\phi_1}{V_T}} - 1) \approx a_{11} e^{\frac{\phi_1}{V_T}} \tag{12.19}$$

$$I_2 - x = a_{11}\ (e^{\frac{\phi_2}{V_T}} - 1) \approx a_{11}\ e^{\frac{\phi_2}{V_T}} \tag{12.20}$$

where the approximate equivalence is justified by assuming that the diodes are sufficiently forward biased. Further, it can be observed that:

$$\frac{I_1 + x}{I_2 + x} = e^{\left(\frac{\phi_1 - \phi_2}{V_T}\right)} = e^{m} \tag{12.21}$$

which when substituted into Equation 12.18 yields

$$I = \frac{(I_1 - I_2 + 2x)\ (I_3 - I_4 + 2y)}{(I_1 + I_2)}\ . \tag{12.22}$$

For the desired case where $I_1 = I_2$ and $I_3 = I_4$ (which can be controlled quite well on a monolithic chip),

$$\Delta I = \frac{2xy}{I_1}\ . \tag{12.23}$$

The currents x and y are given by

$$x = \frac{V_1}{R_{E_1} + 2r_{e_1}}\ , \tag{12.24}$$

$$y = \frac{V_2}{R_{E_2} + r_{e_2}} \tag{12.25}$$

where r_{e_1} and r_{e_2} are the bulk emitter resistances in the V_1 and V_2 diff-amp pairs.

Therefore, the output can be written as a product of the input voltages:

$$\Delta I = \frac{2V_1V_2}{I_1(R_{E1} + 2r_{e_1})\ (R_{E2} + 2r_{e_2})} \tag{12.26}$$

from which it is seen that the multiplier operates in all four quadrants, giving sign and magnitude with respect to each input linearily.

12.4 EVALUATION OF THE MULTIPLIER

To initially set up the multiplier for evaluation, the following fairly straight forward procedure can be used.

In the equivalent model, the current source value $I_3 = I_4$ is determined by the biasing on pin 3, and the value of $I_1 = I_2$ is determined by the biasing on pin 13. Let us call these two values I_3 (for pin 3) and I_{13} (for pin 13).

With resistors R_L inserted in the differential collectors where ΔI is felt, the output voltage is expressed as $2\Delta IR_L$, or

$$V_{out} = \frac{2V_1V_2R_L}{I_3\left(R_x + \frac{2kT}{qI_{13}}\right)\left(R_y + \frac{2kT}{qI_3}\right)} \tag{12.27}$$

$$= KV_1V_2$$

where $kT/q \approx 26$ mV at $+25^{\circ}C$, and $R_x = R_{E_1}$, $R_y = R_{E_2}$ which is obtained from equation 12.26. The scale factor, K, can be adjusted by proper selection of I_3, R_x, and R_y, and is usually set to 1/10 so that the input and output dynamic ranges will be compatible.

As an example, let us assume that the multiplier is to provide

$$V_{out} = \frac{V_xV_y}{10} \tag{12.28}$$

for $-10\ V \leq V_x \leq +10\ V$ and $-10\ V \leq V_y \leq +10\ V$.

Currents I_3 and I_{13} can be set to any convenient value, for example 1 mA, knowing the potential at pin 7 and inserting the proper size resistor from pins 3 and 13 to ground. If the negative supply is chosen to be -15 V, the 1 mA current sources can be set up as

$$R + 500\ \Omega = \frac{15\ V - 0.7\ V}{1.0\ mA}$$

$$R = 13.8\ k\Omega \tag{12.29}$$

Since the magnitude is not critical, the value of 13 kΩ is chosen for convenience. The emitter resistors R_x and R_y can now be determined by considering the input signal handling requirements

$$V_x = I_{13}R_x \tag{12.30}$$

$$V_y = I_3R_y \tag{12.31}$$

for $V_x = V_y = 10$ V.

$$R_x = R_y = \frac{10\text{ V}}{1\text{ mA}} = 10\text{ k}\Omega. \tag{12.32}$$

Since: $R_x \gg \frac{2kT}{qI_{13}}$; $R_y \gg \frac{2kT}{qI_3}$

the scale factor, K, can be approximated by:

$$K = \frac{2R_L}{I_3R_xR_y} \tag{12.33}$$

For K = 1/10 as discussed previously, R_L is found to be:

$$R_L = \frac{KI_3R_xR_y}{2} \tag{12.34}$$

$$= \frac{(10^{-1})\ (10^{-3})\ (10^4)\ (10^4)}{2}$$

$$= 5\text{ k}\Omega\ .$$

Since 5.1 kΩ is a standard-size stock item, this value can be selected; this allows an output swing of 5.1 V. Since each load resistor will reflect this output swing in a differential manner:

$$V_o = 10.2\text{ V} \tag{12.35}$$

which is adequate for the example. From the MC1595 data sheet curve for input voltage (V_x or V_y) vs supply voltages (at pins 1 and 7) it is seen that for a 10 V swing, the voltage at pin 1 must be at least +12 V and at pin 7, it must be at least -13.5 V (the previous choice of -15V is now seen to be valid). The voltage supplied to pin 1 can be direct from a power supply or it can be obtained from the supply connected to the load resistors by a dropping resistor.

The positive supply is:

$$V_{CC} = \left| V_{in}(max) \right| + V_{pin_1} + I_{13}R_L + 2\ V \tag{12.36}$$

$$= 10 + 12 + (10^{-3})\ (5.1 \times 10^{3}) + 2$$

$$= 29.1\ V.$$

Therefore V_{CC} = 30 V is a reasonable selection. The resistor needed to develop the voltage at pin 1 is given by:

$$R = \frac{V_{CC} - V_{pin\ 1}}{2I_3} \tag{12.37}$$

$$= \frac{30-12}{2 \times 10^{-3}}$$

$$= 9\ k\Omega$$

so the selection of 8.2kΩ is again convenient and reasonable.

One might think that a choice of -30 V would be more convenient for pin 7, however, more than 30 V cannot appear across the chip (V_{in} to pin 7) at anytime, and if the input can be +10 V the voltage at pin 7 cannot be -30 V.

A number of methods can be used to adjust the multiplier. Two simple methods are:

Method 1. Refer to the circuit in Figure 12.11.

A. Set V_x = 0 V, V_y = 0 V and adjust the output offset so that the differential output offset is zero volts.

B. Set V_x = 0 V, V_y = 5 V and adjust the x offset for a differential output of zero volts.

C. Set V_y = 0, V_x = 5 V and adjust the y offset for a differential output of zero volts.

D. Set V_x = ±5 Vdc, V_y = ±5 Vdc and adjust gain pot (I_3) for correct scale factor.

Method 2. Refer to the circuit in Figure 12.12 (squaring mode).

A. Set V_{in} = 0 and adjust the voltage at pin 8 (V_{adj}) until the differential output voltage is zero.

B. Apply an input voltage to V_{in}, for example +10 V, and adjust the gain pot for the correct scale factor.

C. Apply the reverse polarity input in Step B and read the same output voltage that was found in Step B. If the reading is different repeat Step B.

12.5 APPLICATIONS

The applications for a four-quadrant linear multiplier are almost limitless. Any control or instrumentation problem where the product of two or more quantities is needed is a potential application for the device. The following discussion will cover

some of the more basic uses of the four-quadrant multiplier, from which more specific applications can be derived.

Figure 12.13 illustrates four basic uses--that of multiplication, division, taking the square root, and obtaining the means square. In the divide and square root applications, the multiplier is used as a feedback element around an operational amplifier in such a way that the Z-input is forced to equal the negative of the multiplier output. The circuit accuracy is somewhat worse in the divide and square root modes than in the multiply or square modes. For a multiply accuracy of 1% of full scale (this means that, if the maximum multiply output is $\pm$10 V, an error of $\pm$0.1 V is obtained regardless of input), the divide error can be several percent of full scale as the divisor decreases below a few volts.

Three additional applications are shown in block diagram form, in Figure 12.14. The frequency doubler operates on the principle that

$$(\text{Cos}\,\omega t)^2 = \tfrac{1}{2}(1 + \text{Cos}\,2\omega t) \tag{12.37}$$

which results in a dc offset portion and the doubled frequency signal. The linear phase detector operates on the principle that:

$$K\text{Cos}\,\omega t\text{Cos}\,(\omega t + \phi) = \tfrac{K}{2}\text{Cos}(2\omega t + \phi) + \tfrac{K}{2}\text{Cos}\phi \tag{12.38}$$

and with the insertion of a low-pass filter (LPF), the output Cos ϕ is easily obtained. This differs from flip-flop phase detectors or sample-hold phase detectors in that conventional phase detectors produce a voltage proportional to the phase difference, where the multiplier approach produces a voltage proportional to the cosine of the phase difference. The roots or powers block diagram is relatively self-explanatory. The log and antilog functions can be obtained by taking advantage of the exponential relationships found in a transistors base-emitter junction when used with an operational amplifier (3).

The final two figures offer a small glance at the performance of this device. Figure 12.15 illustrates the error characteristics of the MC1595 by relating the output error in millivolts to the magnitude of the input in volts. Worst-case error is about 0.5% (V_X = 5.0 V, V_Y = $\pm$10.0V, V_E = 28 mv). Restricting both inputs to less than $\pm$5 V, a worst case error of about 0.2% results. Figure 12.16 demonstrates the multiplier's excellent bandwidth characteristics. The curve in Figure 12.16 shows a very flat response to 1 MHz; the 3dB down point is at 4.6 MHz.

ACKNOWLEDGMENT

The author wishes to acknowledge and thank Brent Welling and Jim Solomon for their interest, suggestions and encouragment.

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FIGURES

Figure 12.1. Amplitude modulation in a communications systems is the classical example of analog multiplication.

Figure 12.2. Carrier-signal zero crossings are often used to generate the switching function S(t).

Figure 12.3. Simple model of switching function.

Figure 12.4. Basic multiplier circuit for accomplishing modulation function.

Figure 12.5. Balanced modulator. Output filter is used with the multiplier to eliminate all terms beyond the first one in the Fourier Series.

Figure 12.6. Linear four-quadrant multiplier.

Figure 12.7. Multiplier preconditioning.

Figure 12.8. Modified version of previous linear four-quadrant multiplier.

Figure 12.9. Monolithic realization of linear multiplier.

Figure 12.10. Equivalent model of the integrated multiplier.

Figure 12.11. Arrangement for adjusting output of multiplier. Method one.

Figure 12.12. Arrangement for adjusting output of multiplier (squaring mode operation). Method two.

Figure 12.13. Four basic applications: multiplication, taking the square root, division and obtaining the means square.

Figure 12.14. More applications; frequency doubling, linear phase detection and obtaining roots and powers.

Figure 12.15. Output error as a function of input voltage.

Figure 12.16. Multiplier bandwidth. Response to 1 MHz is flat.

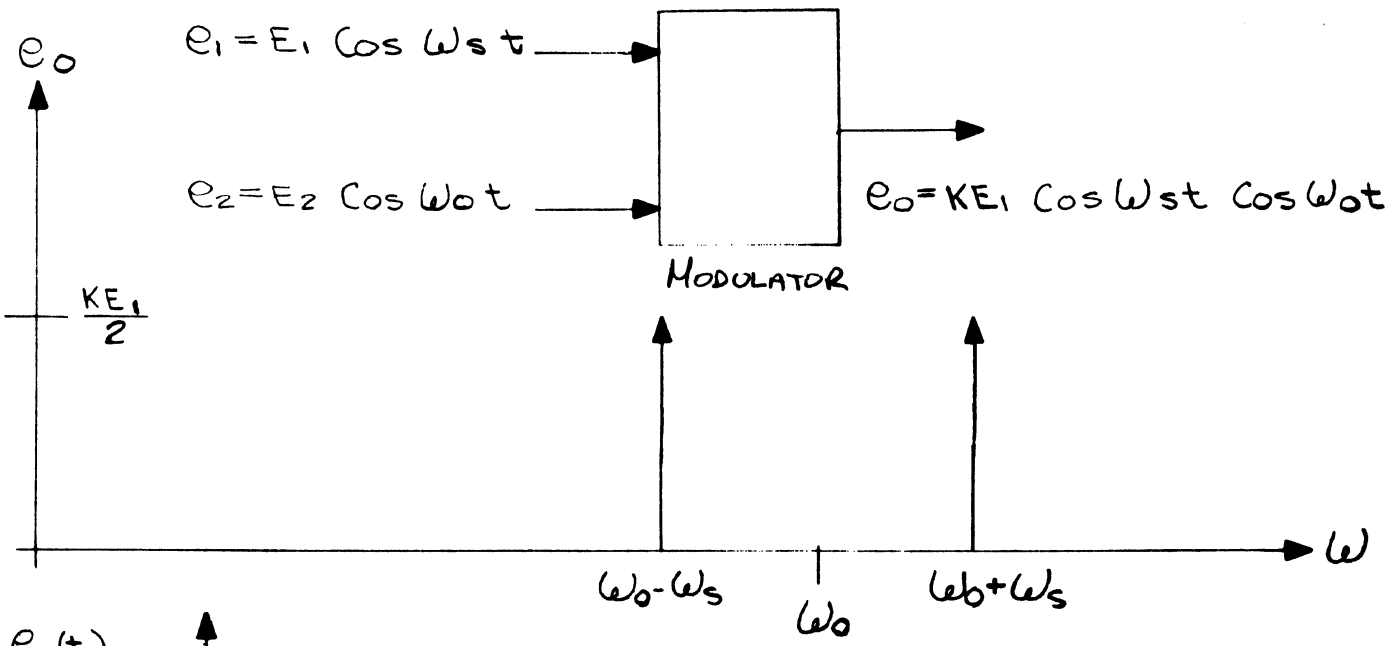


Figure 12.1. Amplitude modulation in a communications systems is the classical example of analog multiplication.

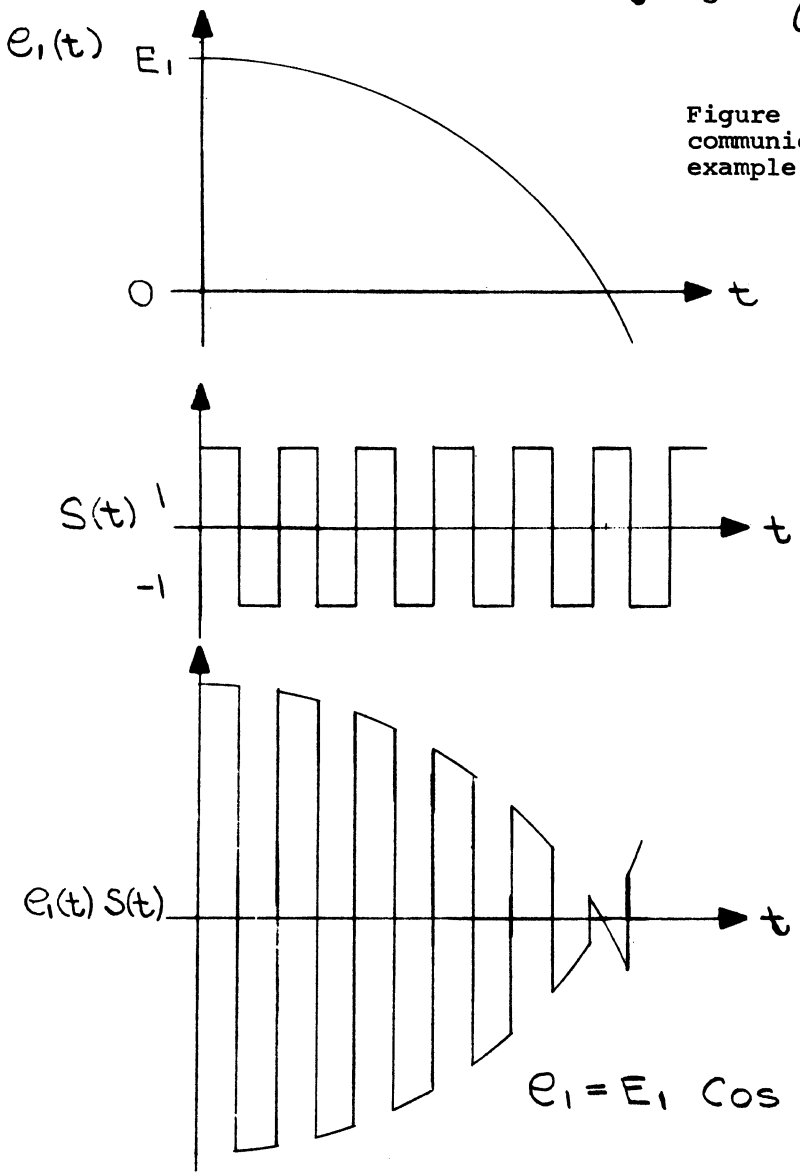


Figure 12.2. Carrier-signal zero crossings are often used to generate the switching function A(t).

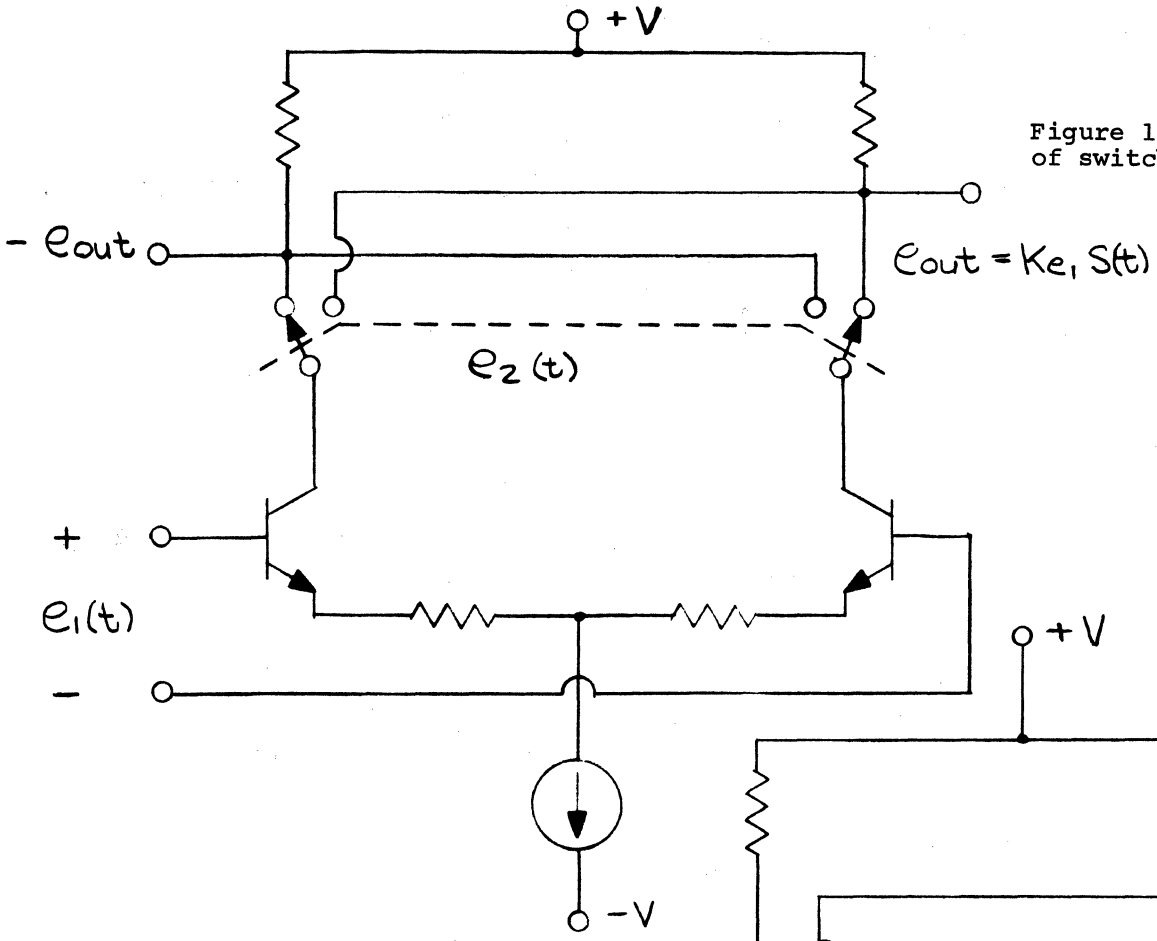


Figure 12.3. Simple model of switching function.

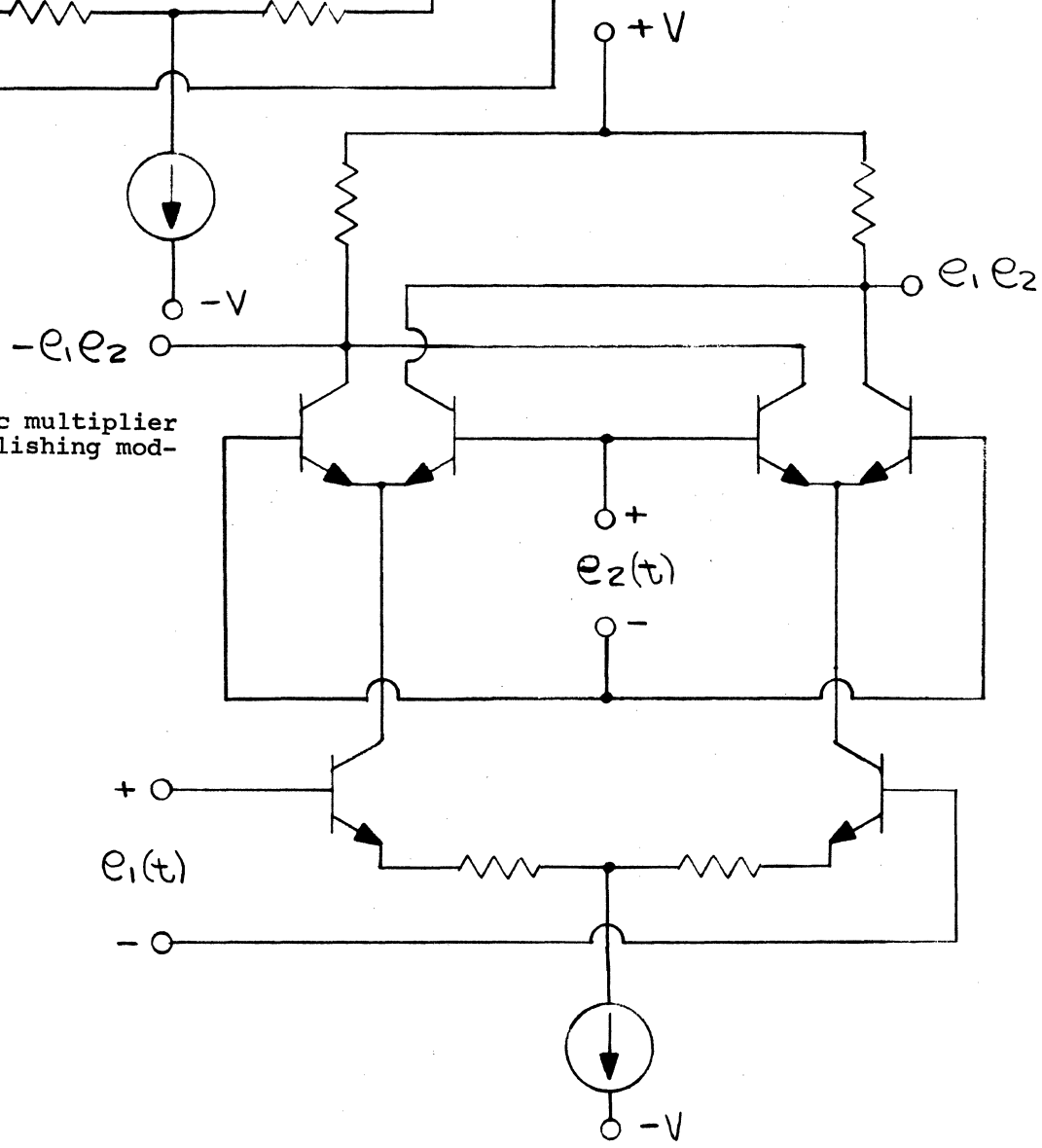


Figure 12.4. Basic multiplier circuit for accomplishing modulation function.

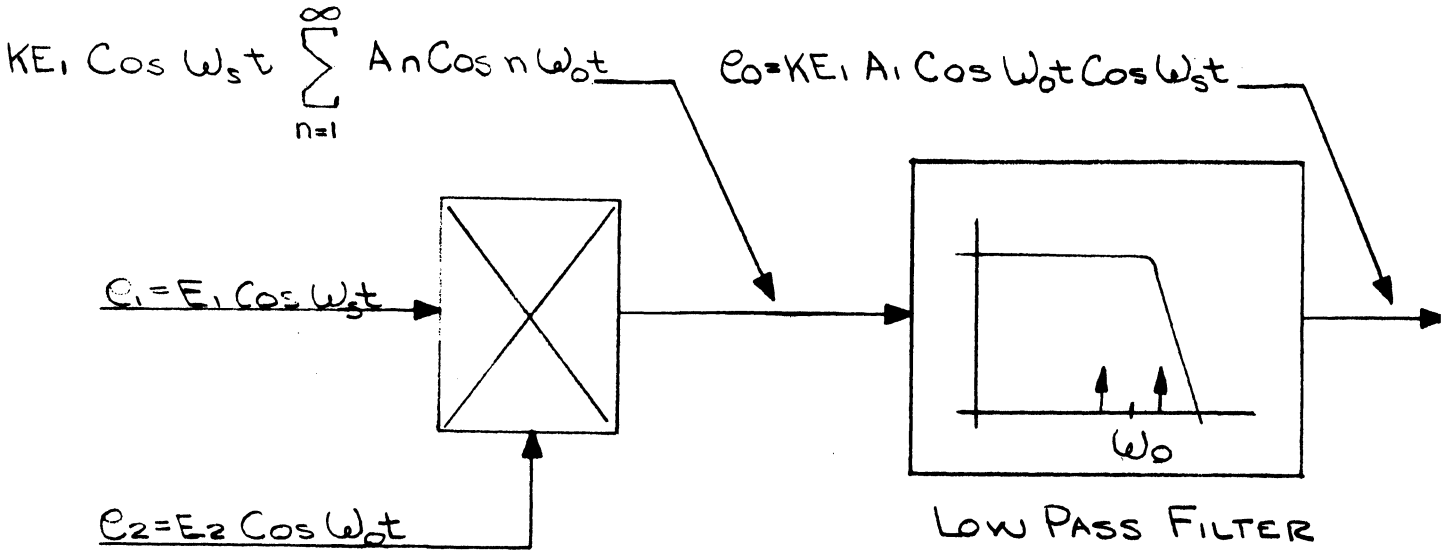


Figure 12.5. Balanced modulator. Output filter is used with the multiplier to eliminate all terms beyond the first one in the Fourier Series.

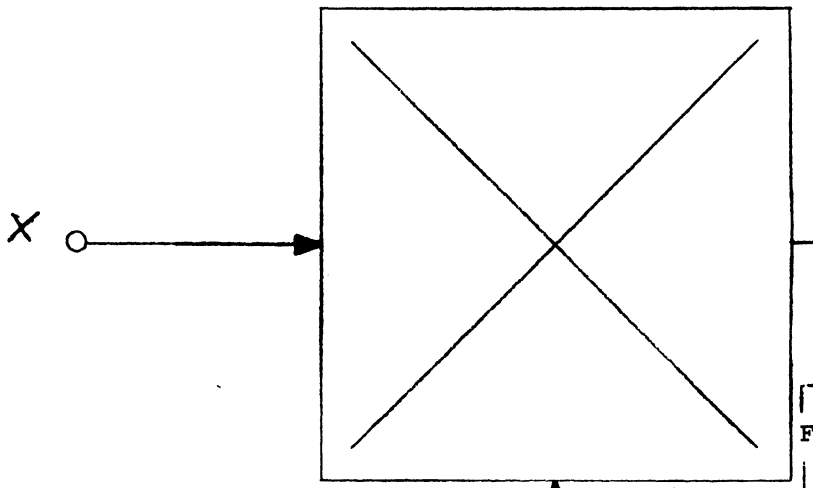


Figure 12.6. Linear four-quadrant multiplier.

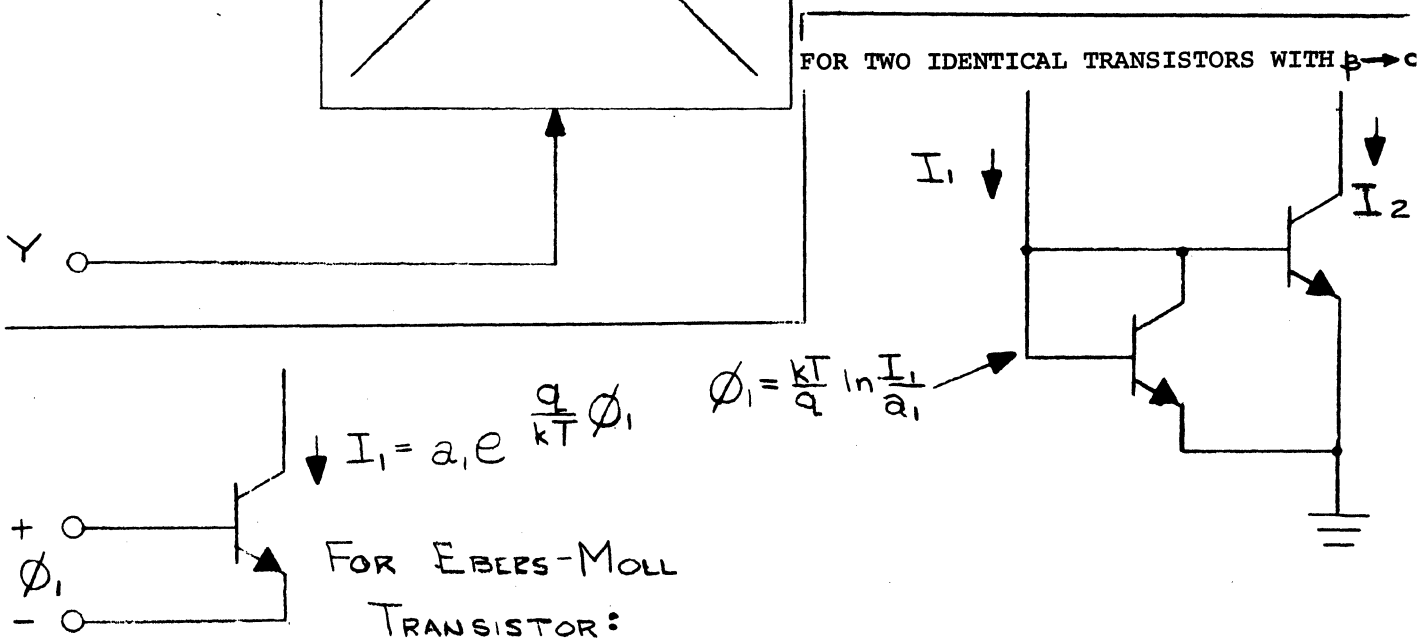


Figure 12.7. Multiplier preconditioning.

$$I_2 = a_1 e^{\frac{q}{kT}\phi_1} = a_1 e^{\frac{q}{kT}\left[\frac{kT}{q} \ln \frac{I_1}{a_1}\right]} = I_1$$

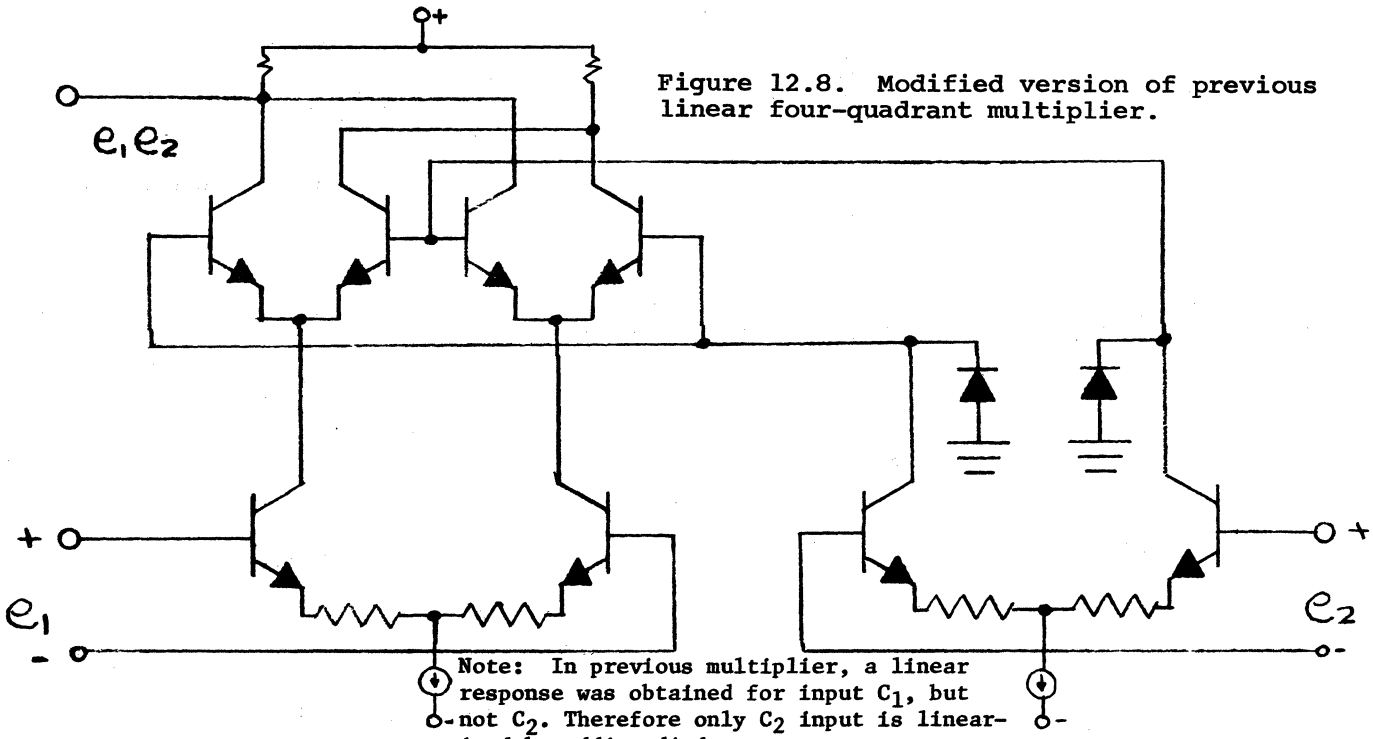


Figure 12.8. Modified version of previous linear four-quadrant multiplier.

Note: In previous multiplier, a linear response was obtained for input C_1, but not C_2. Therefore only C_2 input is linearized by adding diodes.

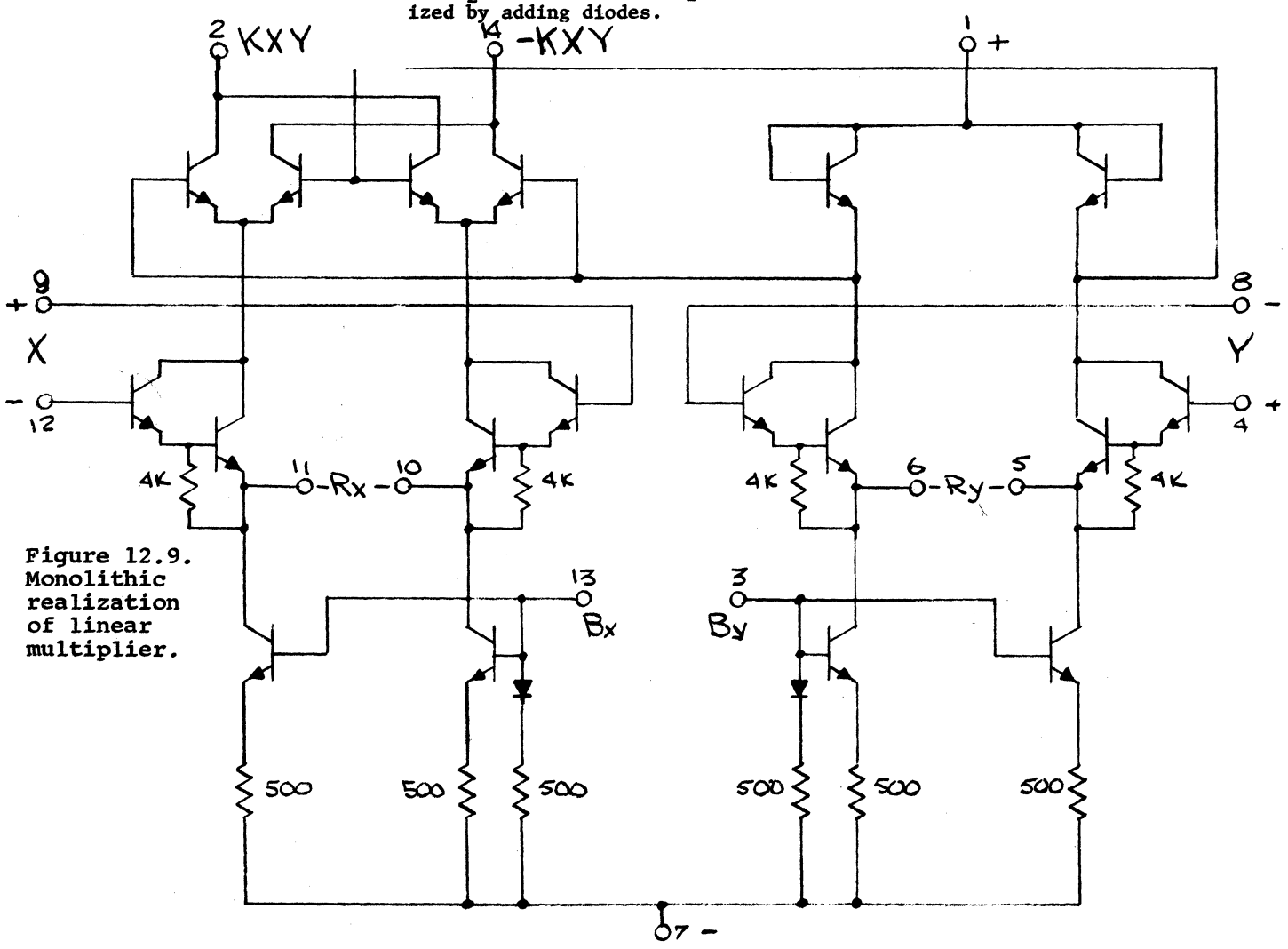


Figure 12.9. Monolithic realization of linear multiplier.

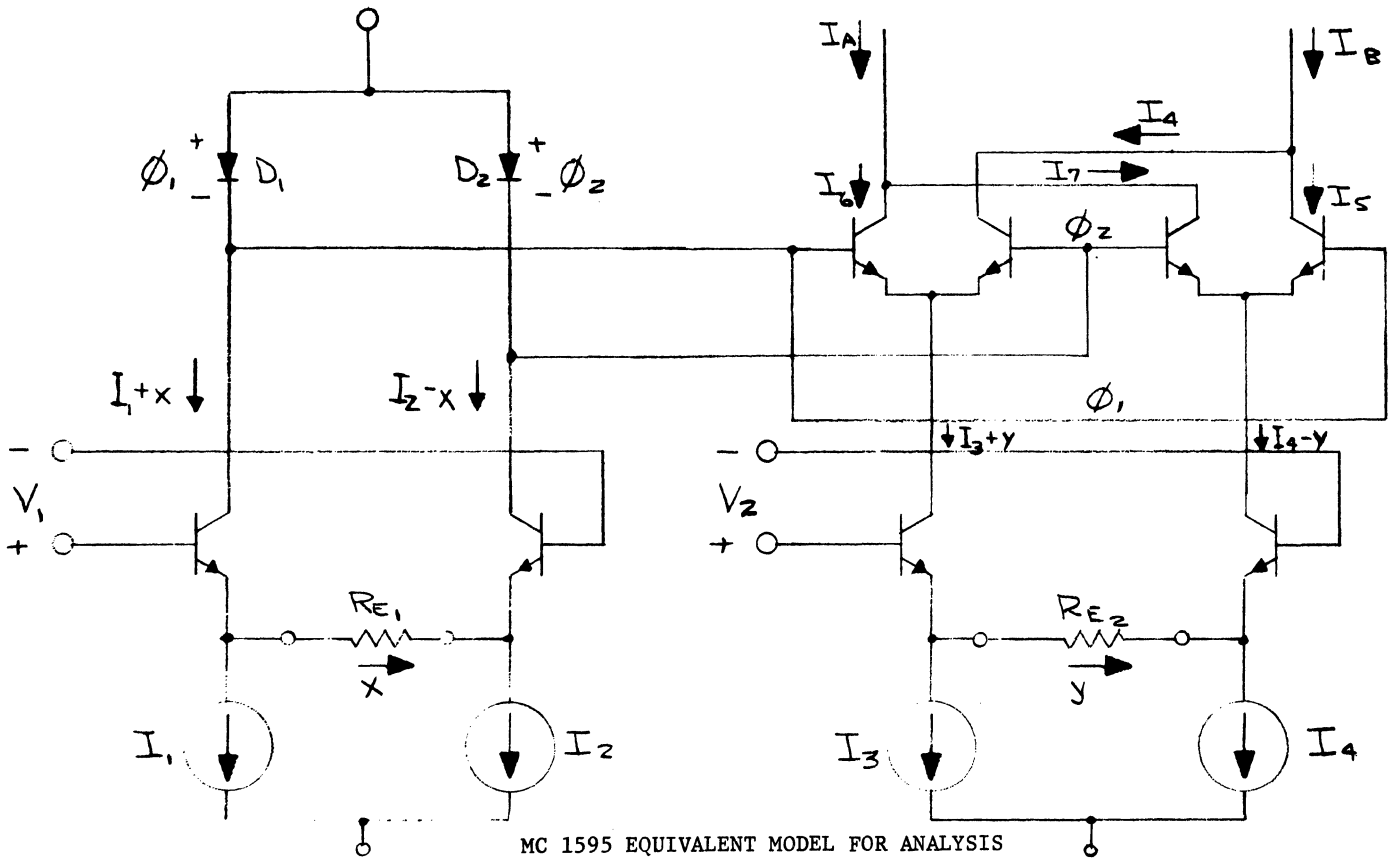


Figure 12.10. Equivalent model of the integrated multiplier.

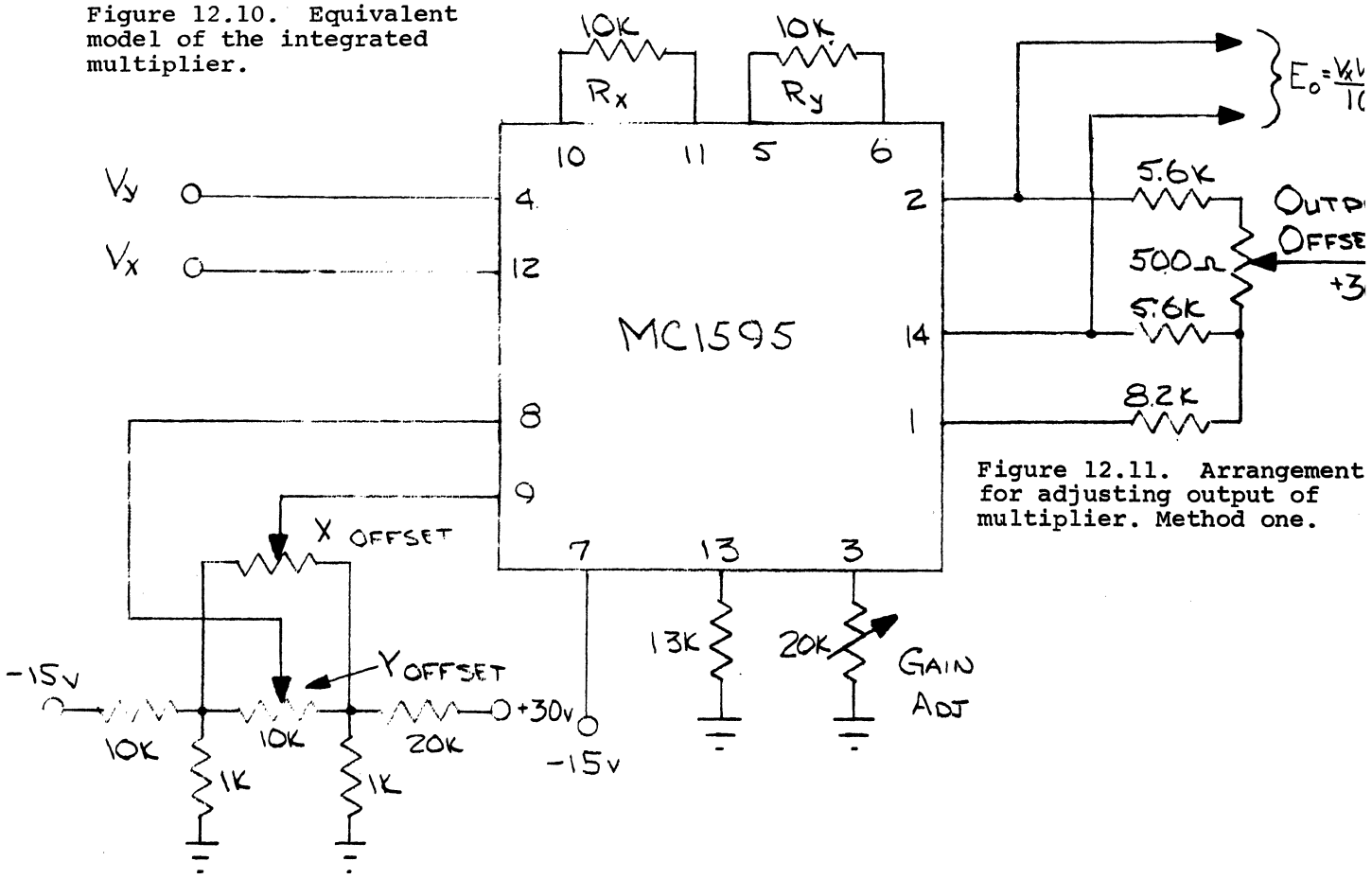


Figure 12.11. Arrangement for adjusting output of multiplier. Method one.

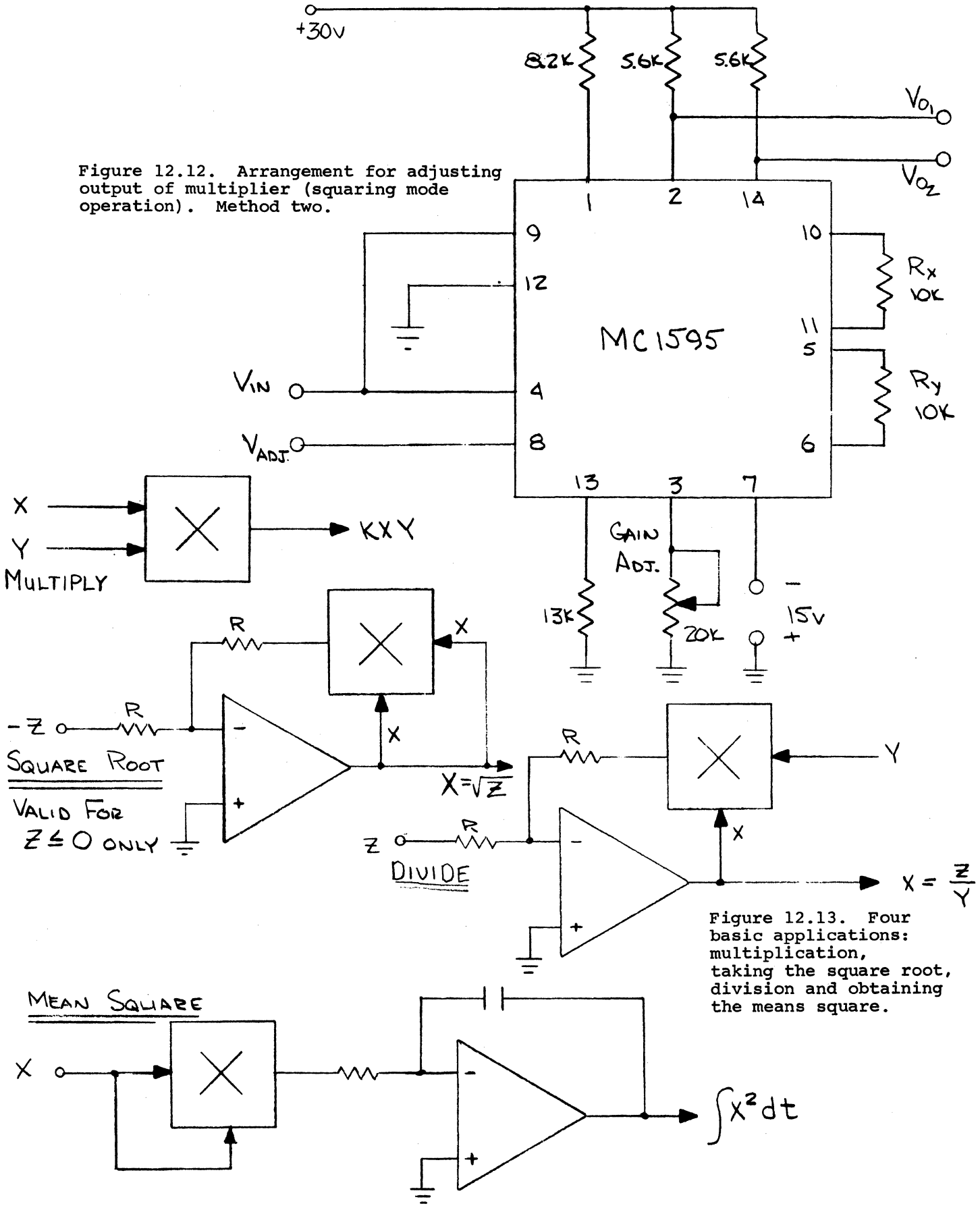


Figure 12.12. Arrangement for adjusting output of multiplier (squaring mode operation). Method two.

Figure 12.13. Four basic applications: multiplication, taking the square root, division and obtaining the means square.

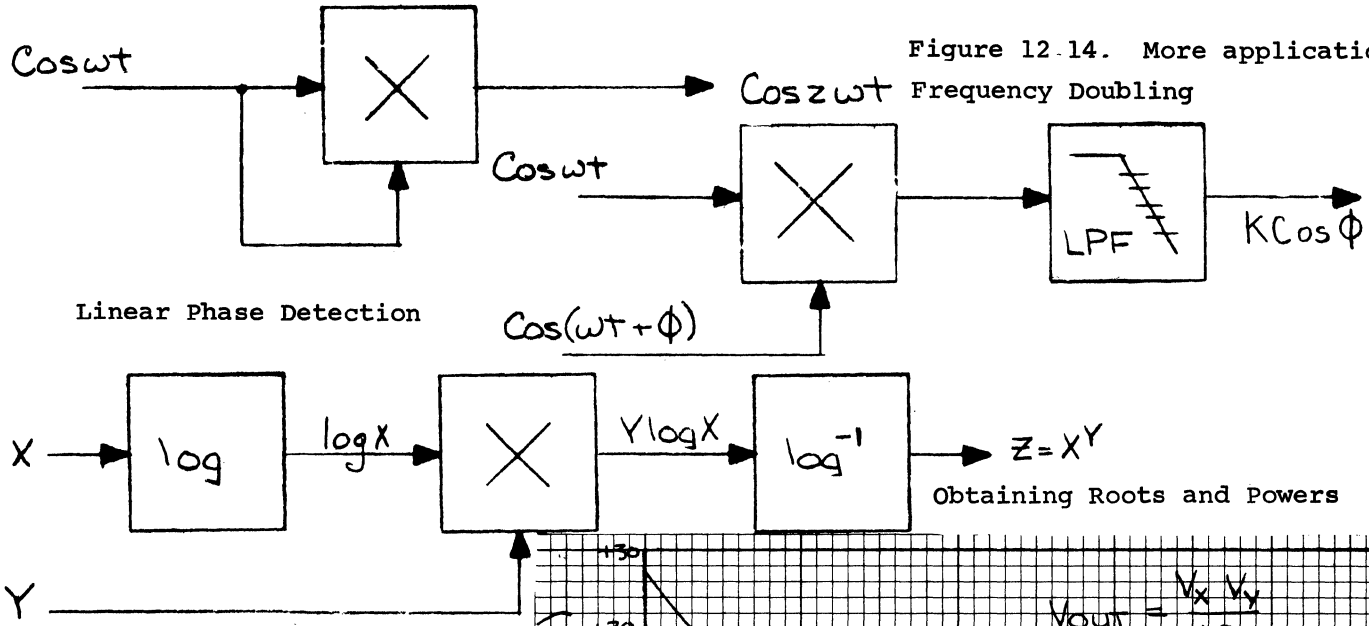


Figure 12.14. More applications; Frequency Doubling

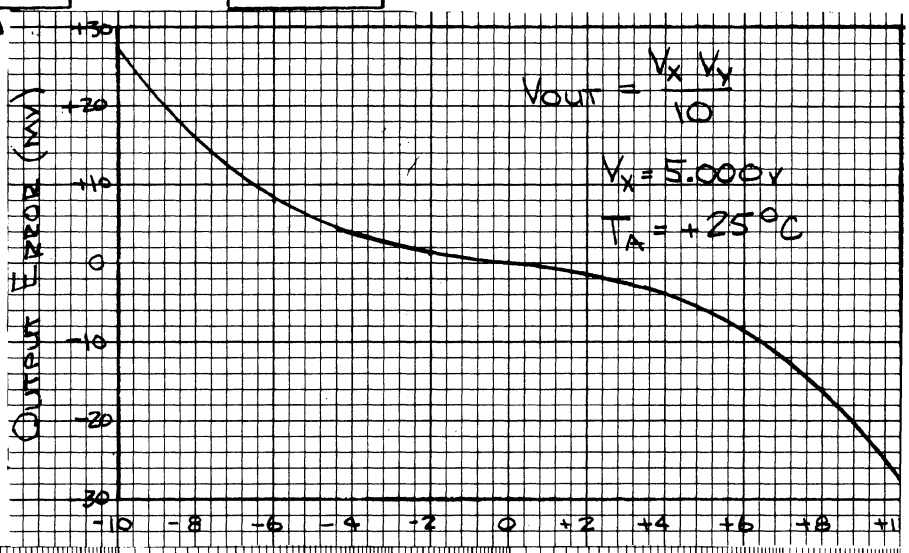


Figure 12.15. Output error as a function of input voltage.

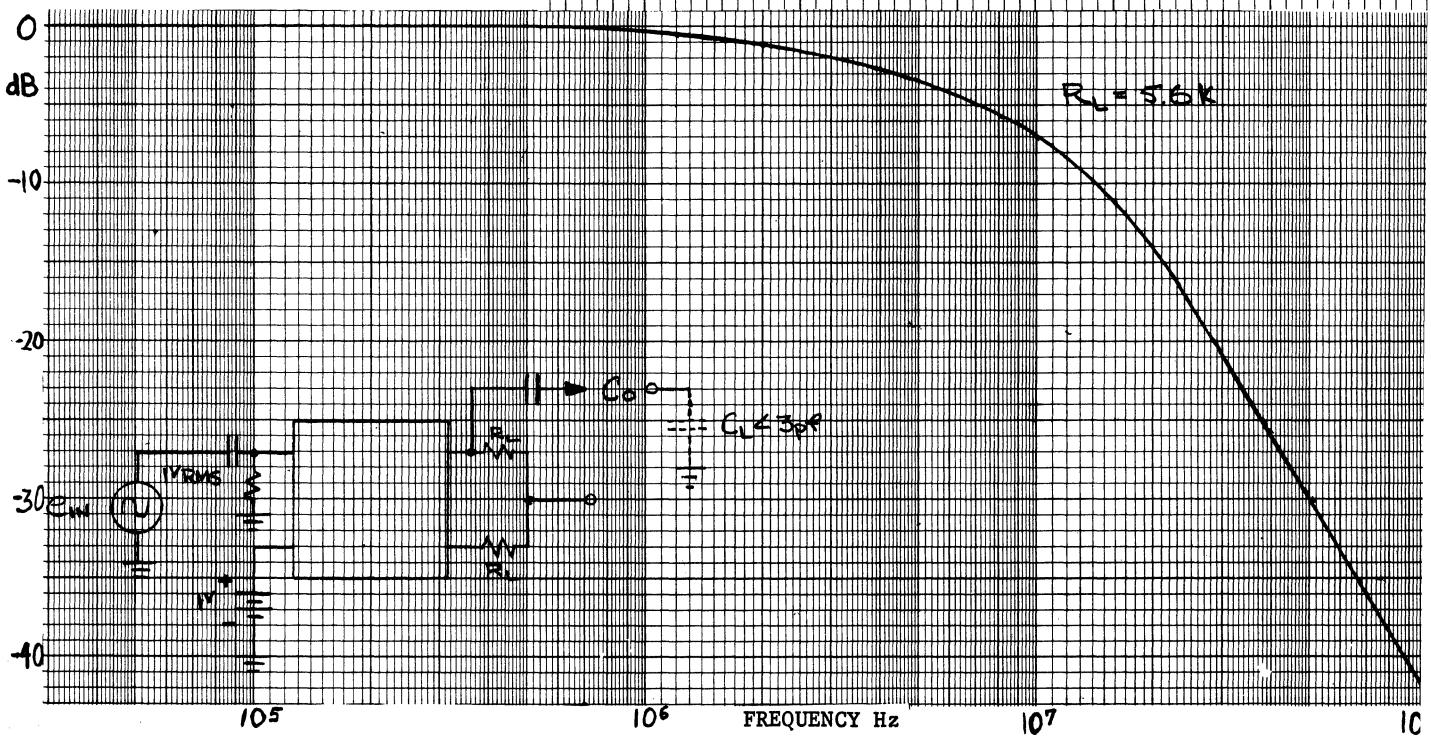


Figure 12.16. Multiplier bandwidth. Response to 1 MHz is flat.

13

Mutiplexing With Complementary MOS Integrated Circuits

by R. L. Sanquini and
A. A. Ahmed
Radio Corp. of America

Although the p-type MOS switch is replacing bipolar-transistor and mechanical-relay counterparts, it will in turn eventually be replaced by the complementary MOS switch because the latter device offers many performance advantages without sacrificing any of the advantages of p-type MOS switches. The advantages of complementary MOS (COS/MOS) switches include the ability to operate with control-signal amplitudes compatible with conventional forms of logic gates, micropower power consumption, and minimum transients in the signal output when the channel is switched. In this chapter, a monolithic complementary MOS 4-channel multiplexer, developed for switching analog or digital signals in analog-to-digital converters, telemeters, control systems, and multiple-channel data transmissions will be described.

13.1 COS/MOS CONSTRUCTION

The cross-sectional view of the complementary switch, shown in Figure 13.1, illustrates the COS/MOS construction. A p-type diffusion forms a so-called "well" to isolate the n-channel transistor from the p-channel transistor. With zero bias applied from gate to source, few carriers are available for conduction. As the gate-to-source voltage is increased (made more positive on the n-channel units and more negative on the p-channel units), charges are induced near the silicon-oxide interface that form an ohmic path between the source and the drain, and current flow increases rapidly.

The COS/MOS process permits design of a multiplexer which operates at conventional logic voltage levels with high absolute noise immunity, good linearity, low ON resistance, high OFF resistance, and low capacitance.

13.2 BASIC MULTIPLEXER CHANNEL

Each channel of the multiplexer consists of a simple inverter and a switch, as shown in Figure 13.2. The inverter section is shown in Figure 13.3 along with its transfer characteristics. The circuit consists of one p-channel and one n-channel MOS transistor, both sharing a common drain electrode. When the input is high (+V), the n-channel transistor is turned on, the p-channel transistor is off, and the output is low. When the input is low, the n-channel device is turned off, the p-channel device is on. and the output is high.

In either state, the power consumed is low (in the order of picowatts) because one of the two devices connected in series is turned off. The small static power dissipation does not change if the circuit is used to drive other insulated-gate stages because the stages draw no average gate current as a result of their extremely high input impedance (10^{12} ohms). During switching, when the capacitance at the output must be charged to the high level through the ON p-channel transistor, some power is dissipated in the p-channel unit. The charge stored in the capacitor is dissipated in the n-channel transistor when the input becomes high. The dynamic power P required for switching is equal to $C_o V_o^2 f$, where C_o is the output capacitance in farads, V_o is the supply voltage

in volts, and f is the frequency in hertz.

Power dissipation as a function of frequency is shown for the inverter circuit in Figure 13.4.

13.3 P-CHANNEL MOS SWITCH

A review of the p-channel MOS switch will be helpful in evaluating the COS/MOS mutliplexer. An elementary p-channel signal switch is shown in Figure 13.5. When V_{in} is negative, the input terminal becomes the drain, and the device is in the source-follower mode. If the gate is biased to a negative voltage (ON condition), the channel resistance is low as long as the source remains more positive than the gate by an amount equal to the threshold voltage. This limit sets a boundary condition for the maximum permissible negative signal swing.

When the signal swing is positive, the device remains in the low-channel-resistance condition and operates in the common-source mode. With this polarity the limit is no longer set by the above mechanisms. Both regions of operation are shown in Figure 13.6.

In the OFF condition, the gate is set to a positive voltage (on a p-channel device) and the channel resistance is high. In the common-source mode, the device turns on again when the signal is more positive than the gating signal by an amount equal to the threshold voltage. There is another mechanism, however, by which the device may turn on, involving parasitic bipolar transistor action with the substrate. (Generally, the MOS action occurs first.)

It is clear from the previous discussion that the signal swing is restricted in one polarity to a voltage considerably lower than that of the gating signal. It is also apparent that any abrupt change in the gating signal produces a transient in the signal path as a result of the gate-channel capacitance. These disadvantages may be largely overcome by the use of a complementary symmetrical system.

13.4 COMPLEMENTARY SWITCH

If complementary p- and n- channel units are connected in parallel and gating voltages are applied in complementary fashion, the composite characteristics shown in Figure 13.7 are obtained. In this arrangement, the transfer characteristic is no longer restricted by the source-follower effect, and the signal may swing up to the gate voltage in both polarities. The OFF condition is subject to the previous limits set by the gating voltages. Because complementary gating is used, the transients in the signal circuit cancel out if the gate-to-channel capacitances in the p- and n- channel units are equal. These characteristics may be modified to some extent by practical limitations. In the central portion of the transfer characteristic, it is apparent that both channels are in parallel. If the load resistance is not large compared with the channel resistances, some variation in the transmission loss may occur over the range. However, this condition is not usually encountered in practice. Another cause of slight nonlinearity in the characteristic is the effect of the substrate on the threshold level. Instead of overlapping, as shown in Figure 13.7, the characteristics may exhibit a gap, as illustrated in Figure 13.8, as a result of shifting of the threshold levels by substrate action. However, results obtained in practice indicate that this problem is not serious at the levels normally used.

13.5 PERFORMANCE CHARACTERISTICS

The TA5460 multiplexer, shown in Figure 13.9, illustrates some of the advantages of using complementary-symmetry MOS in a multiplexer. As in the case of most complementary MOS devices, the quiescent power consumption is very low; typical current drain is 100 nA for all four units on the chip. Perhaps the most significant advantage over single-gate systems is that the signal-swing capability is equal to the switching logic levels, normally $\pm$ V or 0 to 10 V. The ON/OFF signal ratio, shown in Figure 13.10 obviously improves at lower frequencies because the feedthrough is almost purely capacitive. A lower load resistance also increases this ratio but increases transmission nonlinearity as well. With a 10-kΩ load, for example, audio distortion is 1%, which is adequate for many applications.

In the case of other analog signals, it is not always easy to relate percentage distortion to a useful parameter. For this reason, TA5460 devices are characterized for nonlinearity of the transmission characteristic. This nonlinearity is measured as a deviation from an optimum straight-line approximation; the test circuit used is similar to the one shown in Figure 13.1. Basically, the transmitted signal is reduced to some extent in amplitude by a voltage divider and is then compared to the input signal. The resulting difference signals are amplified, and the peak negative swing is set to ground potential. The resulting wave is peak-detected, and the value is indicated on the meter M_1. Resistor R_1 is then adjusted for a minimum value on M_1, and the value of the minimum total positive and negative deviation from a straight line is read on the meter. The value of R_1 used is equal to the dynamic ON-channel resistance.

The meter M_2 is used for calibration or, if desired, for finding the straight-line characteristic approximation which matches the actual characteristic at zero voltage and peak positive excursion.

13.6 SUMMARY

The complementary MOS multiplexer offers several advantages over the p-channel circuit.

Although the No. TA5460 (developmental type number) is restricted in maximum frequency capability to about 0.2 MHz, this limitation is not fundamental to the design. COS/MOS multiplexers will be available in the near future which extend the present frequency by more than an order of magnitude.

FIGURES

Figure 13.1. Cross-sectional diagram of complementary MOS switch.

Figure 13.2. Basic multiplexer channel.

Figure 13.3. Basic MOS inverter circuit.

Figure 13.4. Typical dissipation characteristics of MOS inverter.

Figure 13.5. Diagram of p-channel MOS switch.

Figure 13.6. Transfer characteristic of p-channel switch.

Figure 13.7. Transfer characteristic of COS/MOS switch.

Figure 13.8. Effect of substrate potential on threshold level of COS/MOS switch.

Figure 13.9. TA5460 four-channel COS/MOS multiplexer.

Figure 13.10. Typical ON-OFF output signal ratios of TA5460 as a function of signal frequency.

Figure 13.11. Multiplexer linearity test circuit.

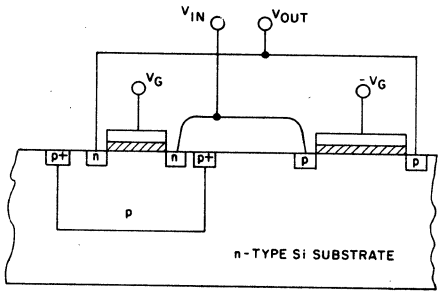


Figure 13.1. Cross-sectional diagram of complementary MOS switch.

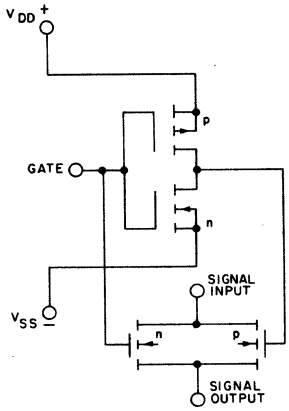


Figure 13.2. Basic multiplexer channel.

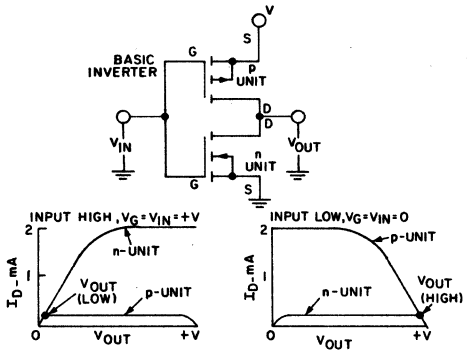


Figure 13.3. Basic MOS inverter circuit.

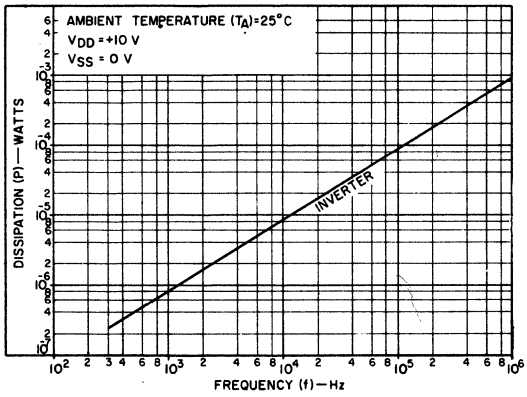


Figure 13.4. Typical dissipation characteristics of MOS inverter.

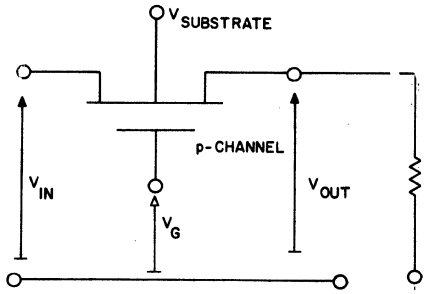


Figure 13.5. Diagram of p-channel MOS switch.

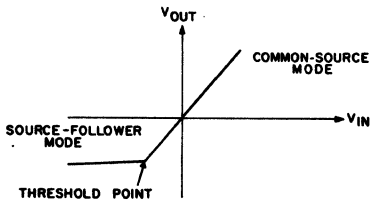


Figure 13.6. Transfer characteristic of p-channel switch.

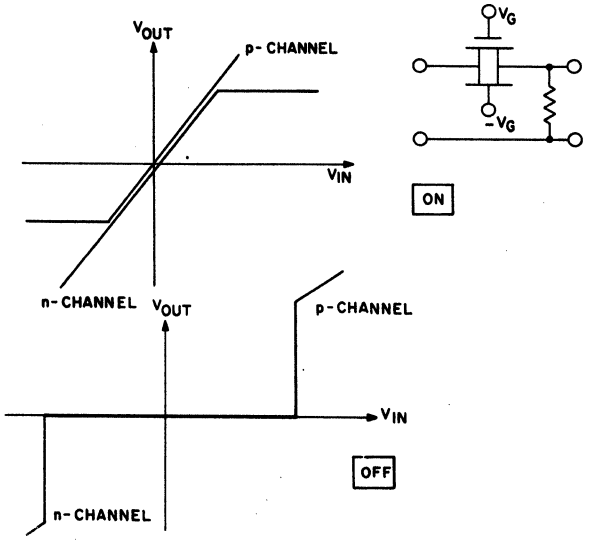


Figure 3.7. Transfer characteristic of COS/MOS switch.

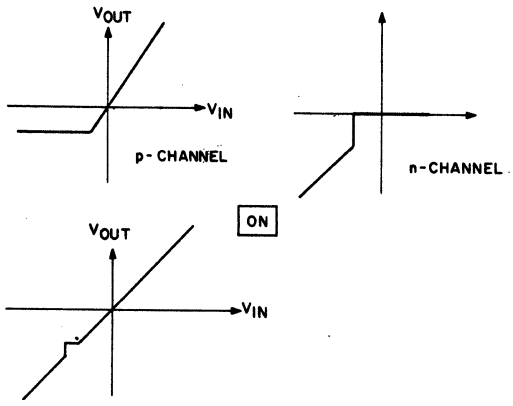
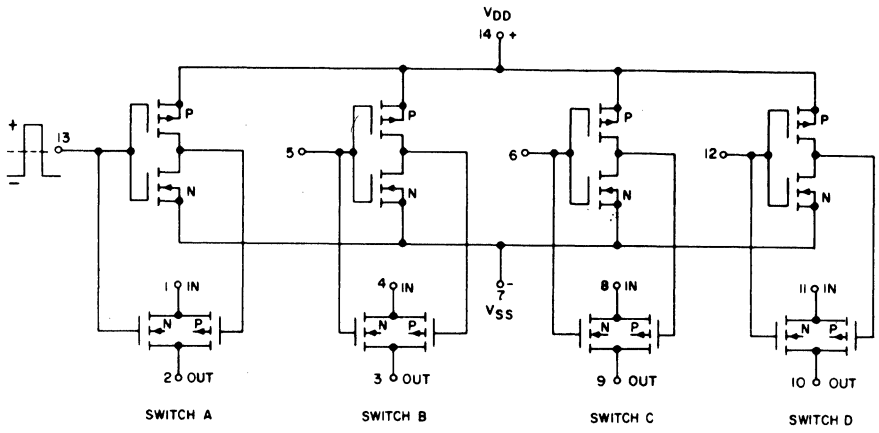
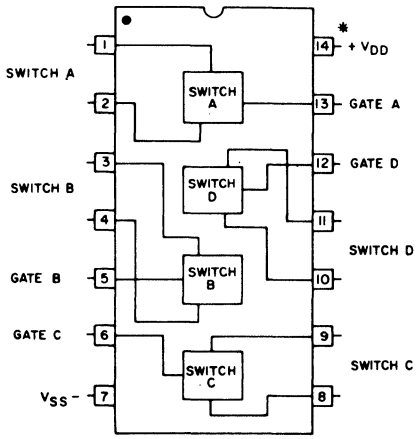


Figure 13.8. Effect of substrate potential on threshold level of COS/MOS switch.





NOTE: All switch P-channel substrates are internally connected to terminal No. 14.
All switch N-channel substrates are internally connected to terminal No. 7.

Figure 13.9. TA5460 four-channel COS/MOS multiplexer.

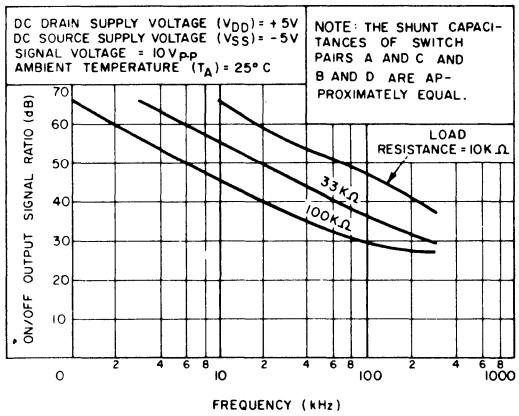
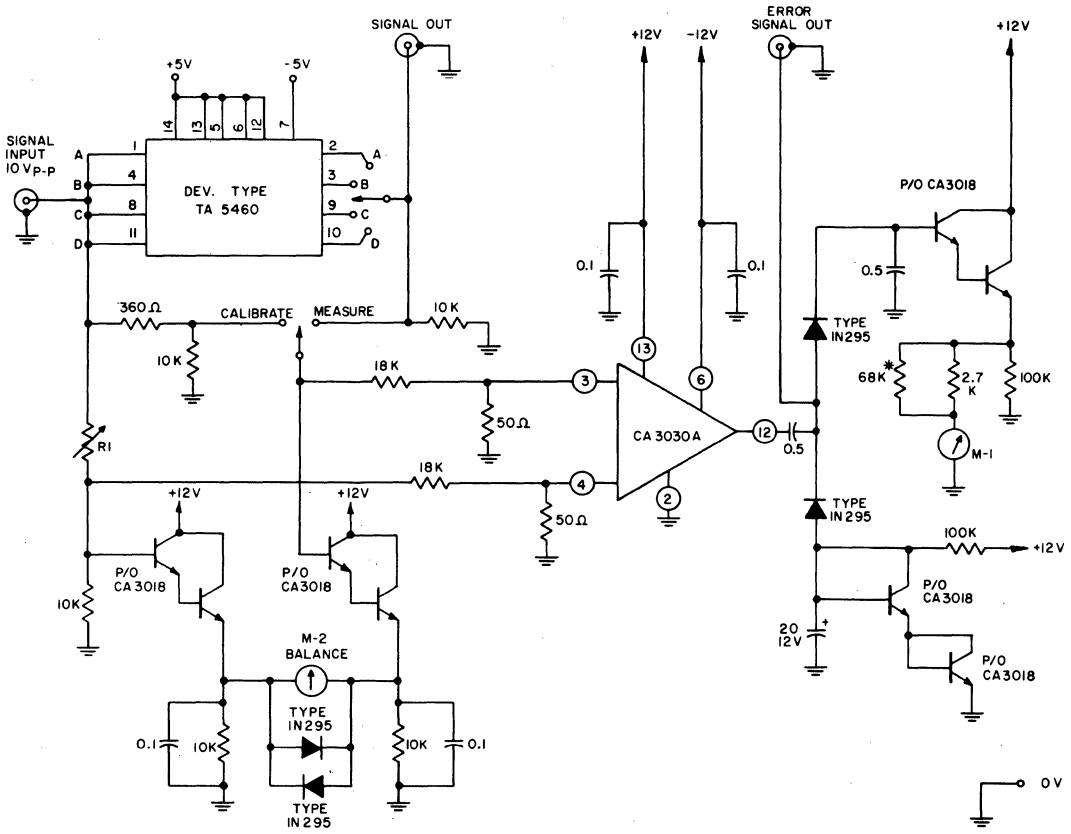


Figure 13.10. Typical ON-OFF output signal ratios of TA5460 as a function of signal frequency.



* = These meter resistors may have to be adjusted to suit individual units.

M-1 = Weston Model 301, 200 Ω/volt or equivalent. Indication: Percent of full signal deviation from best straight line.

M-2 = Weston Model 301, 100 μA-0-100 μA.

R1 = 0-10 K calibrated Helipot

Figure 13.11. Multiplexer linearity test circuit.

14

Voltage Regulator ICs With Foldback Current Limiting

by Douglas R. Sullivan and
Hans W. Mamie
Transitron Electronic Corp.

Damage by short-circuit power dissipation in a voltage regulator can be avoided if the IC contains an overload protection circuit with externally programmable foldback characteristics. Foldback current limiting maximizes the output current capability in the regulated state for a given package power dissipation rating, while minimizing the available current to a temporarily shorted load.

14.1 DESIGN APPROACHES

There are a number of ways to design a regulator with high-current capability. A popular approach is shown in Figure 14.1. Here a voltage proportional to the output voltage is fed back to the error amplifier through the resistor divider composed of R_1 and R_2. The error amplifier output fedback to the series regulating transistors is at a magnitude that keeps the difference between the fedback voltage and the reference at a minimum and regulation is achieved.

The principal advantage in the approach shown in Figure 14.1 is simplicity. However, there are a number of performance compromises that are associated with this circuit. These compromises are caused by the use of the resistor divider made up of R_1 and R_2, which is employed to set the value of the regulator output voltage. The loop gain of the regulator is proportional to the resistor divider ratio, decreasing as the divider ratio is decreased. Therefore, as the desired output voltage is increased, the divider ratio, and therefore the regulator loop gain, is decreased. As the loop gain is decreased the regulator output impedance increases, degrading the no-load to full-load regulation characteristics. Along with this effect, one finds the regulator's bandwidth is also degraded.

Current limiting is usually achieved by adding a resistor in series with the emitter of the output power transistor. The voltage across this resistor is fed to a control transistor as shown in Figure 14.2. If the output current exceeds a predetermined value, which is programmable by selecting the size of the resistor, R_{SC}, the control transistor is turned on, and, as a result, the base current available to the output power transistor is limited or reduced. Thus, output current limiting is achieved, simply, but not without a compromise in performance.

The chief compromise in using the type of current limiting shown in Figure 14.2 is increased power dissipation. Since the current sensing resistor, R_{SC}, is in series with the regulator output, the minimum input-output voltage differential is increased by the current limiting sense voltage. This is at least 600 mV, and can result in total circuit power dissipation, under regulation conditions, that is up to 25% higher than in cases when no current limiting is employed. Another disadvantage of this design approach is that the current sensing resistor increases the output impedance of the regulator; especially at higher output voltages where the loop gain is low due to the resistor ratio, $R_2/(R_1 + R_2)$.

An alternate approach to the regulator circuit design is shown in Figure 14.3. Here the output error amplifier and power transistor are connected as a noninverting amplifier with a gain of one. Variation of the output voltage setting is achieved with the addition of a reference level shifting amplifier whose gain, and hence the regulator output voltage, is determined by the resistor divider composed of R_1 and R_2. Since the load on the level shifting amplifier is constant, there is no degradation in the regulation characteristics for different output-voltage settings. The output power amplifier, on the other hand, offers maximum loop gain, minimum output impedance and wide bandwidth, all of which are constant over the full voltage range of the amplifier.

The resistor R_{SC} in series with the collector of the output transistor is used to sense the output current of the regulator. The voltage across this resistor is fed to additional circuitry such that the base current available to the power transistor is limited and current limiting can be achieved. The addition of this resistor to the circuit does not increase the minimum input-output voltage differential. Current sources and other circuitry common to the output error amplifier account for a voltage drop from the positive supply to the base of the power transistor that far exceeds the 600 mV necessary to drive the current limit circuitry. All that is needed to take advantage of this voltage drop is a power transistor with a low saturation resistance. Thus, no increase in circuit power dissipation is required, and none of the output parameters of the regulator are degraded by the addition of current limiting.

14.2 CURRENT LIMITING VOLTAGE REGULATOR

A complete circuit diagram of the TVR 2000, a monolithic voltage regulator with foldback current limiting, is shown in Figure 14.4, and the complete functional block diagram is depicted in Figure 14.5. As can be seen in Figure 14.5, the regulator contains a temperature-compensated reference. The reference is level shifted by a noninverting amplifier whose gain is determined by an external resistor divider. The output amplifier is connected as a noninverting amplifier with a gain of one, and output current sensing for short-circuit current limiting is done on the collector side of the output power transistor. Thus, the output characteristics are constant, and are independent of the addition of current limiting.

The start circuit is comprised of D_1, R_5, and Q_5. Diode D_2 serves as the main reference and is temperature compensated by Q_{14}, Q_{15}, Q_{17}, Q_{18}, R_8, and R_9. The voltage at the emitter of Q_{15} has a positive temperature coefficient due to the positive temperature coefficient of D_2 and the negative temperature coefficient of the base-emitter diodes of Q_{14} and Q_{15}. The voltage at the base of Q_{17} has a negative temperature coefficient due to the negative temperature coefficient of the base-emitter diodes of Q_{17} and Q_{18}. Resistors R_8 and R_9 are selected so that the voltage at their common point has a temperature coefficient nearly equal to zero. This voltage is the temperature compensated reference for the regulator.

The reference diode D_2 and resistor R_8 and R_9 set the current in the matched Darlington npn current sources $Q_{17}Q_{18}$, $Q_{19}Q_{20}$, and $Q_{21}Q_{22}$. A current divider is formed by Q_{15} and Q_{16} which sets the current in each of the matched pnp current sources Q_1, Q_2, Q_3, and Q_4 at one half of that in the matched npn current sources. This factor of one

half is required because two of the pnp current sources, Q_3 and Q_4, are used as collector loads in two differential amplifiers whose emitter current sources are $Q_{19}Q_{20}$, and $Q_{21}Q_{22}$ respectively.

Transistor Q_5 is back biased and turned off as soon as the pnp current source Q_1 begins furnishing current to the reference D_2. Since Q_1 is matched to Q_2, their collector currents are equal. Neglecting base currents, the collector current of Q_2 is equal to the emitter current of Q_{14}. As discussed previously the collector current of Q_2 is one half that of the Darlington current source $Q_{17}Q_{18}$ which in turn is proportional to the reference voltage and the resistor R_8 and R_9. Thus, the reference diode regulates its own excitation current.

Transistors Q_{24} and Q_{25} form the differential inputs for the reference level shifting amplifier. The current source for this differential amplifier is $Q_{19}Q_{20}$. To obtain maximum gain, Q_3, a pnp current source is used as the collector load for Q_{25}. Differential drive for the output transistor Q_{26} is provided by connecting its emitter as the collector load for Q_{24}. The closed loop gain of the reference level shifting amplifier is determined by the external resistors R_{LS1} and R_{LS2}. Since this amplifier is connected as a noninverting amplifier, its gain is always greater than or equal to one.

Transistors Q_{28} and Q_{29} provide a balanced input for the output differential amplifier. The design of this amplifier is very similar to that of the level shifting amplifier, the circuit consisting of a current source $Q_{21}Q_{22}$, a collector load Q_4 and a differentially driven output transistor Q_{31}. The amplifier output transistor Q_{31} and the regulator series-pass, power transistor Q_{32} are connected as a Darlington pair, providing maximum output current capacity with minimum standby current drain. Transistor Q_{27} is used to shut down the reference level shifting amplifier under regulator output short circuit conditions, protecting the base emitter diodes of Q_{28} and Q_{29}. Stabilization of the output amplifier is achieved by use of the external capacitor, C_1.

Current limiting is obtained by turning on the control transistor Q_{34}, diverting some of the base current intended for the Darlington pair $Q_{31}Q_{32}$. Availability of base current for the control transistor Q_{34} depends on the relative magnitude of the collector current in Q_{37}, Q_{38} and Q_{41}. Summation of currents at the base of Q_{34} yields the equation:

$$I_{C38} - I_{C37} - I_{C41} = I_{B34} \approx 0 \qquad (14.1)$$

where I_{C38} is proportional to I_{OUT}, I_{C37} is proportional to V_{OUT} and I_{C41} is a constant equal to 0.2 mA. The final relationship describing the foldback characteristic is:

$$\frac{I_{OUT}R_{SC} + (0.2 \times 10^{-3})\ (R_{12} + R_{SC})}{R_{13}} - \frac{V_{OUT}}{R_{FB} + R_{14}} - 0.2 \times 10^{-3} = I_{B34} \approx 0 \qquad (14.2)$$

Thus for $V_{OUT} = 0$ (short circuit), I_{OUT} is a function of R_{SC} and the V_{OUT} vs I_{OUT} foldback slope is a linear function of both R_{SC} and R_{FB}. For $R_{FB} = \infty$, the foldback slope is vertical, resulting in straight current limiting without foldback. The equation for straight current limiting is the same as that for the short-circuit current. Substituting values of R_{12} and R_{13} into the foldback relationship above reduces this equation to:

$$R_{SC}I_{OUT} \approx 0.1 \text{ V (short circuit)} \qquad (14.3)$$

Stabilization of the foldback circuitry is accomplished with the external capacitor C_2.

Typical foldback characteristics with a value of R_{SC} of 5 Ω are shown in Figure 14.6. Here, P_{max}, the maximum circuit power dissipation occurs at the intersection of the foldback curve and $I_{P/2}$ where I_p is the intersection of the V_{in} line with the desired foldback slope.

A plot of the intersection of V_{in} and the various foldback slopes, for constant maximum power dissipation, result in the familiar hyperbolic lines. The hyperbolic lines are plotted as a function of the intersection of V_{in} and the various foldback slopes only for the convenience of peak power prediction. It must be remembered that this peak power actually occurs at $I_{P/2}$. For short-circuit conditions, it is clear that the foldback short-circuit power is less than: (1) the peak power at $I_{P/2}$; (2) the power at $I_{OUT\ max}$ (regulated state); or (3) the short circuit power if straight current limiting was employed at $I_{OUT\ max}$.

The circuit design is slanted towards a relatively large active-to-passive component ratio, as evidenced by the component count of 43 transistors, two diodes, and 18 resistors. Considerable advantage was derived throughout the circuit from transistor matching, which is inherent in monolithic technology. The monolithic version of the circuit resulted in a chip size of 70 by 85 mils. Important features of the IC are its power transistor with low saturation voltage at a collector current up to 200 mA, a unique lateral pnp transistor design, and the use of epitaxial pinch resistor technology. Typical electrical characteristics for the TVR 2000 are included in Table 14.1.

14.3 BASIC VOLTAGE REGULATOR

The interconnection for the basic voltage regulator is shown in Figure 14.5. Here, the regulator output voltage is a function of R_{LS1} and R_{LS2} and is given by the equation:

$$V_{OUT} = (V_{LSS}) \frac{R_{LS1} + R_{LS2}}{R_{LS2}} \tag{14.4}$$

where V_{LSS} is the level shift sense voltage, and is approximately equal to 2.8 V. To obtain a minimum output-voltage temperature coefficient, the impedance level of the level-shift resistive divider must be equal to 2.25kΩ. Therefore, the following equation can be formulated:

$$\frac{R_{LS1}R_{LS2}}{R_{LS1} + R_{LS2}} = 2.25k\Omega \tag{14.5}$$

14.4 FREQUENCY COMPENSATION

External capacitor C_1 stabilizes the regulator section while C_2 is used to stabilize the current limiting circuitry. When the current limiting option is not used, so that $R_{SC} = 0$ and the R_{FB} terminal is grounded or left open, C_2 can be eliminated. C_2 can also be eliminated for certain high capacitance loads. However, if the regulator is to be operated over long leads or from an inductive source, an 0.1 μF decoupling capacitor may be required from the input terminal to ground. Table 14.2 summarizes the recommended values of C_1 and C_2 for various capacitive loading of the regulator output.

14.5 CURRENT LIMITING

The short-circuit current is a function of R_{SC}. The equation for the short-circuit current, including transistor β effects, is:

$$I_{OSC} = \frac{120 \text{ mV}}{R_{SC}} \tag{14.6}$$

The slope of the current limiting characteristic is a function of R_{SC} and R_{FB}. The slope is vertical when R_{FB} is infinite (open circuit or R_{FB} terminal grounded); when smaller values of R_{FB} are used foldback current limiting results. The equation for the foldback slope is:

$$\text{Slope} = \frac{R_{SC}(R_{FB} + 5\ \text{k}\Omega)}{1.35\ \text{k}\Omega} \tag{14.7}$$

It should be noted that when the output voltage is less than 0.7 V the slope control transistor Q_{37} becomes inoperative, causing the slope to be vertical just above I_{SC}. This slight nonlinearity in the foldback slope need be considered only when the ratio of the maximum output current to the short circuit current is very large. If multi-valued operation or hysteresis is to be avoided, then:

$$\frac{I_{SC}}{0.7V} \geq \frac{I_{OUT\ MAX}}{V_{OUT}} \ . \tag{14.8}$$

Of course, for operation over wide temperature ranges, the negative 2mV/°C temperature coefficient of the base emitter diode of Q_{37} must also be remembered.

The minimum input-output voltage differential specification of 2.2 V applies with or without current limiting as long as the maximum voltage across R_{SC} is limited to 500 mV. This is necessary to prevent saturation of the output transistor. Therefore, for a maximum current of 100 mA, the maximum value of R_{SC} is 5 Ω, which results in a minimum short circuit current of 24 mA; for a maximum output current of 50 mA, the maximum value of R_{SC} is 10 Ω, resulting in a minimum short circuit current of 12 mA. If larger ratios of maximum output current to minimum short circuit current are required, the user need only provide additional input-output voltage differential. For example, if a short-circuit current of 10 mA and a maximum input current of 100 mA were required, R_{SC} would be 12 Ω and the minimum input-output voltage differential would necessarily be increased by 700 mV to 2.9 V. Thus for ratios of maximum output current to minimum short-circuit current greater than four to one, the additional input-output voltage differential required is given by the following equation:

$$R_{SC}I_{OUT(MAX)} - 0.5 = V_{DIFF}\text{(additional)}. \tag{14.9}$$

This equation only applies if the R_{SC}, $I_{OUT(MAX)}$ product is greater than 500 mV.

14.6 CURRENT EXPANDED POSITIVE REGULATOR

A current expanded positive voltage regulator is shown in Figure 14.7. In this application, foldback current limiting can be employed so that both the regulator and power transistor T_1 are protected under short-circuit conditions. All of the comments made in discussing current limiting as well as the specifications in Table 14.1 apply with the additional requirement that the minimum input-output voltage differential must be increased by the V_{BE} voltage of the power transistor. The maximum output current is limited only by the beta of the power transistor while the output impedance is reduced

by this same beta.

14.7 CURRENT EXPANDED NEGATIVE REGULATOR

A negative voltage regulator is shown in Figure 14.8. Here the maximum output current is limited only by the beta and the power rating of the transistor T_1. The regulated output voltage appearing across resistor R_1 and R_2 is determined by the following equation:

$$\left|V_{OUT}\right| = \frac{V_{LSS}\ (R_1 + R_2)}{R_2} \tag{14.10}$$

In equation 14.10, V_{LSS} is the level-shift sense voltage and is approximately equal to 2.8 V. Resistor RLS should be set equal or larger than 2 kΩ to avoid overloading of the level shift output, and the impedance level of the parallel combination of R_1 and R_2 should be kept low enough to supply 0.1 mA to the #2 output terminal. Absolute value signs are used in Equation 14.9 and succeeding equations to avoid confusion.

The voltage at the #1 output terminal must follow the relationship:

$$\left|V_{OUT\ \#2}\right| \geq \left|V_{OUT\ \#1}\right| \geq \left|V_{DIFF}\right| \tag{14.11}$$

where V_{DIFF} is 2.2 V minimum and V_{OUT} #2 is given by the equation:

$$\left|V_{OUT\ \#2}\right| = \left|V_{OUT}\right| - \left|V_{LSS}\right| \tag{14.12}$$

In order to meet the requirements set forth in equations 14.10 and 14.11, the following relationship can be used in selecting the zener diode:

$$\left|V_{IN}\right| + \left|V_{LSS}\right| - \left|V_{OUT}\right| - \left|V_{BE1}\right| \leq V_Z \leq \left|V_{IN}\right| - \left|V_{BE1}\right| - \left|V_{DIFF}\right| \tag{14.13}$$

where V_{LSS} = 2.8 V, V_{DIFF} = 2.2 V minimum, and V_{BE1} is the base-emitter voltage for T_1. If V_Z is centered between the limits established by equation 14.13, the allowable ripple on V_{IN} will be symmetrical, [equal (+) and (-) swings], and the allowable peak-to-peak ripple will be:

$$\Delta V_{IN\ MAX} = \left|V_{OUT}\right| - \left|V_{LSS}\right| - \left|V_{DIFF}\right| \tag{14.14}$$

The output voltage range is -8 V to -40 V since the full regulated output appears across the regulator input to common terminals.

The minimum difference between $-V_{IN}$ and V_{OUT} is dependent on the saturation voltage of T_1 while the output impedance is given by:

$$Z_{OUT} = \frac{Z_{OR}\ (R_1 + R_2)}{\beta_1 R_2} \tag{14.15}$$

where Z_{OR} is the output impedance of the basic regulator and β_1 is the current gain of T_1.

14.8 CURRENT EXPANDED NEGATIVE FLOATING REGULATOR

The negative voltage regulator shown in Figure 14.8 can be easily converted to a negative floating voltage regulator as shown in Figure 14.9. The only extra components needed are R_4 and D_2. The voltage rating of the zener diode D_2 must be between 8 V and 40 V and R_4 must be small enough to supply: (1) the regulator standby current of 4mA; (2) the zener diode D_2 excitation current; and (3) the base current for T_1. The output current is limited only by the beta and power rating of T1. All of the other considerations mentioned in the negative voltage regulator discussion apply here.

14.9 POSITIVE FLOATING REGULATOR

A positive floating voltage regulator is shown in Figure 14.10. In this circuit, T_1 compensates for the base-emitter diode of T_2 so that the voltage across R_1 is equal to the voltage across the level shifting resistors R_{LS1} and R_{LS2}. This voltage is simply the level shifted reference voltage as measured with respect to the regulator common terminal and is given by the equation:

$$V_{R1} = \frac{V_{LSS}\ (R_{LS1} + R_{LS2})}{R_{LS2}} \tag{14.16}$$

where V_{LSS} is the 2.8 V level-shift sense voltage.

The current through R_2 is essentially equal to that through R_1 if the base current of T_2 is neglected, and the voltage across R_2 plus the V_{BE} of T_1 equals the voltage at which the common terminal of the regulator will float. Therefore, the output voltage is determined by:

$$V_{OUT} = \frac{V_{LSS}\ (R_{LS1} + R_{LS2})\ (R_1 + R_2)}{R_{LS2}\ R_1} \tag{14.17}$$

The output voltage range is unlimited except that the output voltage must be at least 2.2 V below the input voltage and 3 V above the voltage at the regulator common terminal. As in the basic voltage regulator, the voltage from the V_{IN} terminal to the common terminal must be between 8 V and 40 V.

14.10 CURRENT EXPANDED POSITIVE FLOATING REGULATOR

A current expanded, positive floating voltage regulator is shown in Figure 14.11. Voltage regulator #1 regulates the difference between $V_{OUT\ 2}$ and V_{OUT}. This voltage difference is given by:

$$V_{OUT\ 2} - V_{OUT} = \frac{V_{LSS}(R_{LS1} + R_{LS2})}{R_{LS2}} \tag{14.18}$$

Voltage regulator #2 regulates $V_{OUT\ 2}$ (to ground) which is given by the equation:

$$V_{OUT\ 2} = \frac{(V_{OUT} + V_{LSS})\ (R_{LS3} + R_{LS4})}{R_{LS4}} \tag{14.19}$$

Combining equations 14.18 and 14.19 produces the final equation for the output voltage:

$$V_{OUT} = \frac{V_{LSS}R_{LS4}}{R_{LS3}} \left(\frac{R_{LS1} + R_{LS2}}{R_{LS2}} - \frac{R_{LS3} + R_{LS4}}{R_{LS4}} \right) \tag{14.20}$$

The limits of $V_{OUT\ 1}$ for regulator #1 are given in the relationship:

$$V_{OUT} + \frac{V_{LSS}\ (R_{LS1} + R_{LS2})}{R_{LS2}} \leq V_{OUT\ 1\ (\#1)} \leq V_{IN} - V_{DIFF} \tag{14.21}$$

Therefore, the size of the zener diode D_1 can be selected from the relationship:

$$\frac{V_{LSS}(R_{LS1} + R_{LS2})}{R_{LS2}} - V_{BE1} \leq V_Z \leq V_{IN} - V_{OUT} - V_{BE1} - V_{DIFF} \tag{14.22}$$

The allowable range of the input voltage is determined from:

$$V_{OUT} + 8\ V \leq V_{IN} \leq V_{OUT} + 40V \tag{14.23}$$

The impedance level of R_{LS3} and R_{LS4} should be such that the current drawn from the #2 level shift amplifier is no more than 2 mA. The minimum load must at least be able to handle the standby current of both regulators, and the excitation current for D_1. This can be accomplished with a small bleed resistor.

14.11 REMOTE SHUTDOWN REGULATOR

Figure 14.12 shows a voltage regulator with foldback current limiting in an application where the output voltage can be shut down by an external command. The output of the regulator will remain essentially at zero so long as there is a positive voltage at the logic input. Resistor R_1 is included in the circuit to limit the spike current due to the discharging of the capacitor C_1, and can have a value up to 1 kΩ. Resistors R_2 and R_3 should be selected such that transistor T_1 is saturated and can support a collector current greater than 0.5 mA when the logic input is high.

14.12 EXTERNAL REFERENCE REGULATOR

In some applications, it is desirable to run the voltage regulator with an external reference voltage as shown in Figure 14.13. Connecting a number of regulators to the same external reference will produce a system in which all of the regulator output voltages are very nearly equal (approximately 5 mV maximum difference). Since the internal reference and level shifting amplifier temperature coefficients are eliminated, the various regulator outputs will have very low temperature coefficients and will track well. Also, thermal feedback effects due to changes in load currents are minimized.

The zener diode D_1 is included to protect the base-emitter diodes of the level shift amplifier when the external reference voltage is greater than 7 V while R_2 limits the current to D_1. For values of external reference voltage less than 7 V, the zener diode can be eliminated and R_2 can be shorted. The required current drain from the external reference voltage is approximately 0.5 mA.

14.13 SWITCHING REGULATOR

The requirement for high output current in the presence of a large input-output voltage differential results in excess power dissipation and low efficiency. Power dissipation can be reduced and the efficiency can be increased by using a switching regulator similar to that shown in Figure 14.14. Here, the output transistor T_1 is switched on and off, under the control of the TVR2000 regulator. During the period that T_1 is saturated, energy is stored in the inductor L_1 and the capacitor C_3, as well as being supplied to the load. During the period that T_1 is off, the energy stored in L_1 and C_3 is used to energize the load, with D_1 being used as a return path for the current. Since energy is transfered to the inductor L_1 only when T_1 is saturated, the circuit is very efficient.

In the circuit of Figure 14.14, the drive for the output transistor comes from the R_{SC} terminal of the regulator which is the collector of the internal power transistor. The current at this terminal is switched on and off by causing a small square wave to appear at the output of the level-shift amplifier. This is accomplished by connecting the level-shift amplifier in the usual manner with R_{LS1} and R_{LS2} selected to set the desired output voltage, and using T_1 to sink a square wave of current from the

R_{LS1}, R_{LS2} common point. Since this point is the feedback point for the level-shift amplifier, it's voltage is held constant at 2.8 V. Therefore, the square wave of current due to T_2 must flow through R_{LS1}, causing a square wave of voltage to appear at level-shift output terminal. The level-shift output terminal is also an input to the output amplifier, and the square-wave voltage that appears there will control the current in R_7 and therefore, the transistor T_1.

Transistor T_2, in conjunction with R_3, R_4 and R_5, is used to determine the magnitude of the current through R_{LS1}, which should be set to produce at least a 10 mV square wave at the output of the level-shift amplifier. Connecting R_3 to the collector of T_1 results in the proper feedback polarity for oscillation will take place. Excess storage time in the switching transistor T_1 can be limited by carefully selecting the base current so that the overdrive is not too large. Constant overdrive for T_1 is achieved with the internal foldback circuitry. The magnitude of the base current of T_1, and therefore, its overdrive is determined by the selection of R_2 and R_7. The relationship for I_{B1} for various values of R_2 and R_7 is:

$$I_{B1} = \frac{V_{IN}\left(\frac{1k\Omega}{R_2 + 5k\Omega}\right) + 0.2\ V - V_{BE1}}{R_7} \tag{14.24}$$

where the 1kΩ, 5kΩ and 0.2 V parameters are internal to the regulator.

Resistor R_6 is used to isolate the regulator from the heavy capacitive loading so that minimum compensation can be used. Minimizing the compensation maximizes the switching frequencies that can be obtained with good efficiency. The switching frequency is a function of L_1, C_3, V_{IN}, V_{OUT} and ΔV_{OUT}, the output ripple. The relationships for switching frequency are given in the following equations:

$$f = \frac{1}{t_{on} + t_{off}} \ ; \tag{14.25}$$

$$t_{on} = \sqrt{\frac{2L_1C_3\,\Delta V_{OUT}}{V_{IN} - V_{OUT}}} \ , \tag{14.26}$$

$$t_{off} = \sqrt{\frac{2L_1C_3\,\Delta V_{OUT}}{V_{OUT}}} \ . \tag{14.27}$$

The measured characteristics for the switching regulator shown in Figure 14.14 are given in Table 14.3.

14.14 CONCLUSIONS

Important characteristics for a monolithic voltage regulator to have are:

1. Efficiency. The 2.2 V minimum input-output voltage differential of the TVR2000 is one of the lowest available. The fact that this specification applies even with current limiting further enhances its importance. The 8-V minimum input voltage range is also one of the lowest available, providing for high efficiency in low voltage applications.
2. Constant output characteristics. The addition to a voltage-regulator IC of a reference level-shift amplifier and the connection of the output amplifier as a gain of one result in output characteristics which are constant over the full

voltage range of the regulator. Output parameters should not be degraded by current limiting.

3. Foldback Current Limiting. Full advantage can be taken of the package power dissipation rating if the IC allows selecting the type of current limiting best suited for the application. The current limiting option can also be used when the regulator is expanded with an external power transistor.
4. Versatility. The TVR2000, for example, can be used in a number of different applications including plus or minus regulator; plus or minus floating regulator; switching regulator or remote shutdown regulator.

In selecting a voltage-regulator IC, the user should closely examine the electrical characteristics to make sure that electrical performance is not being sacrificed for efficiency or versatility.

Max. Power Dissipation (TO-100 case)	800 mW
Max. Output Current	200 mA
Input Voltage Range	8 to 40 V
Output Voltage Range ($0 \leq I_L \leq 100$ mA)	3 to 37.8 V
Min. Input-Output Voltage Differential ($0 \leq I_L \leq 100$ mA)	2.2 V
Output Impedance ($0 \leq I_L \leq 100$ mA)	40MΩ
Line Regulation (ΔV_{IN} = 1 V)	0.02% V_{OUT}
Level-Shift Sense Voltage	2.8 V
Output Voltage Temperature Stability	0.003 %/°C
Standby Current Drain (V_{in} = 30 V)	2.8 mA
Output Noise Voltage ($0 \leq f \leq 10$ kHz)	40 μ Vrms

Table 14.1 Characteristics

Load Capacitance	Current Limiting	C_1 (pF)	C_2 (pF)
0	no	1000	0
100 pF $\leq C_L \leq$ 100 μF	no	2000	0
$0 \leq C_L \leq 1$ μF	yes	5000	1000
1 μF $\leq C_L \leq$ 20 μF	yes	$\frac{C_L}{100}$	1000
20 μF $\leq C_L \leq$ 100 μF	yes	0.2 μF + $\frac{2C_L}{1000}$	1000
1 μF $\leq C_L \leq$ 100 μF	yes	0.05 μF	0

Table 14.2 Frequency Compensation

V_{IN}	15 V
V_{OUT}	5 V
I_{LOAD}	1 A
Efficiency	75%
$V_{LS\ OUT}$ (ripple)	30 mV peak to peak
V_{OUT} (ripple)	40 mV peak to peak
Frequency	4.5 kHz
Load Regulation (no load to full load)	50 mV
Line Regulation (V_{IN} = IV)	7.5 mV

Table 14.3 Switching Regulator Performance

FIGURES

Figure 14.1. Simple voltage regulator.

Figure 14.2. Simple voltage regulator with current limiting.

Figure 14.3. Complex voltage regulator with current limiting.

Figure 14.4. The TVR2000 is a monolithic voltage regulator with foldback current limiting.

Figure 14.5. Temperature-compensated reference is level shifted by a noninverting amplifier. Gain of amplifier is determined by external resistor divider.

Figure 14.6. Typical foldback characteristics. Maximum circuit power dissipation occurs at the intersection of the foldback cure and $I_{p/2}$.

Figure 14.7. Current-expanded positive voltage regulator with foldback current limiting

Figure 14.8. Current-expandable negative voltage regulator.

Figure 14.9. Current-expandable negative floating voltage regulator.

Figure 14.10. Positive floating voltage regulator.

Figure 14.11. Current-expandable positive floating voltage regulator.

Figure 14.12. Remote shutdown voltage regulator with foldback current limiting.

Figure 14.13. External reference regulator.

Figure 14.14. High-efficiency switching regulator.

Figure 14.15. Photograph of TRV2000 voltage-regulator.

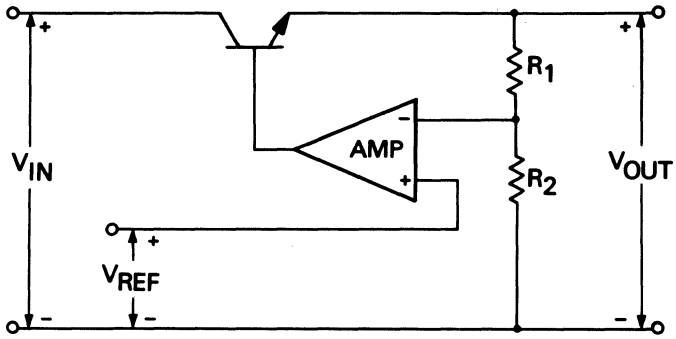


Figure 14.1. Simple voltage regulator.

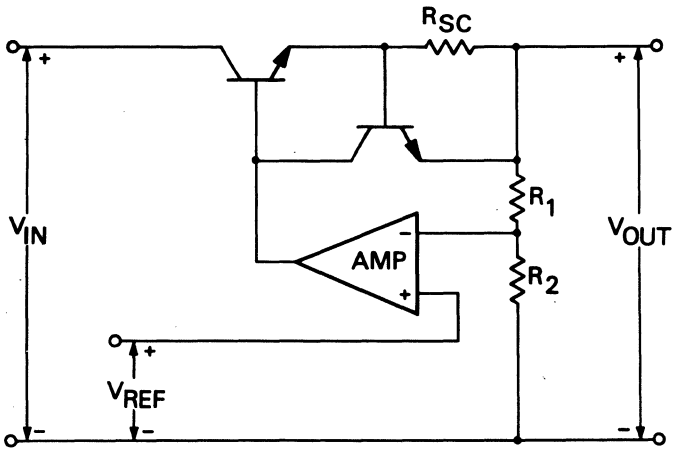


Figure 14.2. Simple voltage regulator with current limiting.

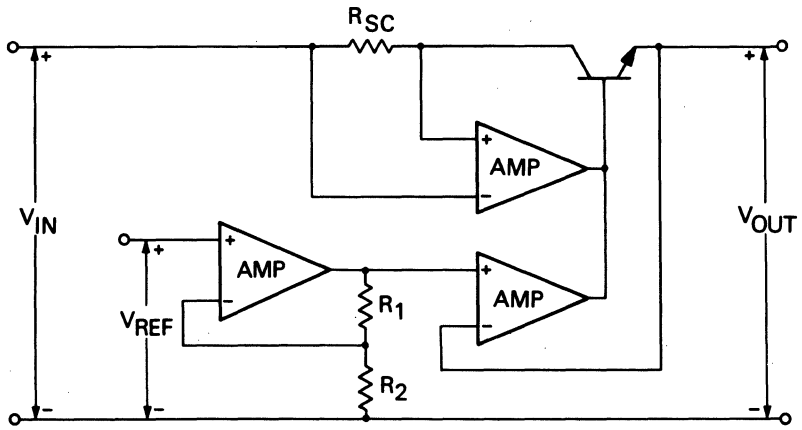


Figure 14.3. Complex voltage regulator with current limiting.

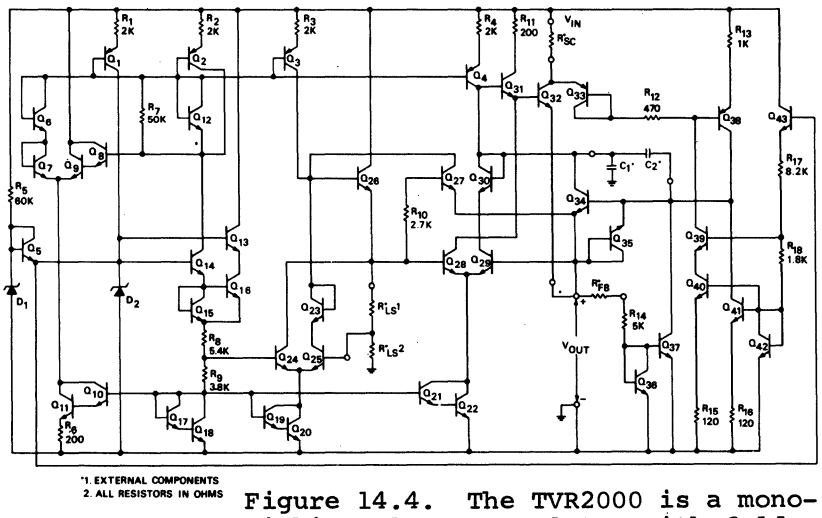


Figure 14.4. The TVR2000 is a monolithic voltage regulator with foldback current limiting.

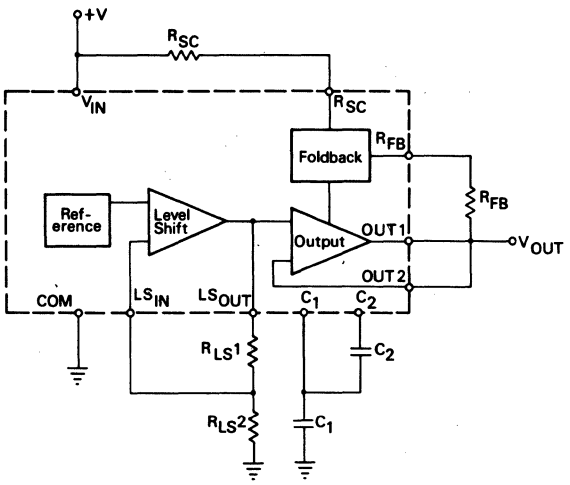


Figure 14.5. Temperature-compensated reference is level shifted by a noninverting amplifier. Gain of amplifier is determined by external resistor divider.

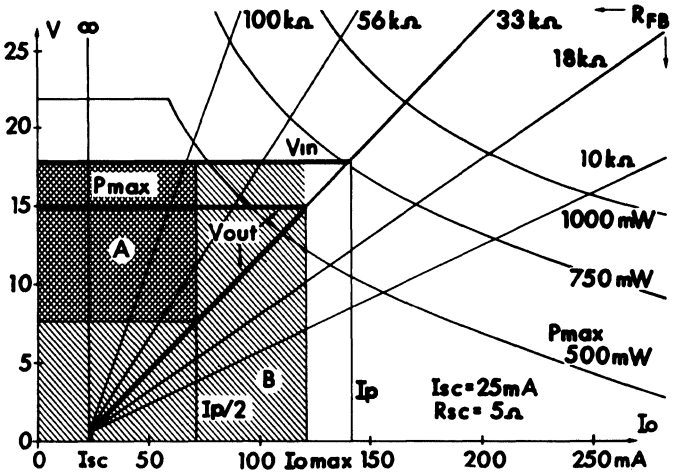


Figure 14.6. Typical foldback characteristics. Maximum circuit power dissipation occurs at the intersection of the foldback cure and $I_{p/2}$.

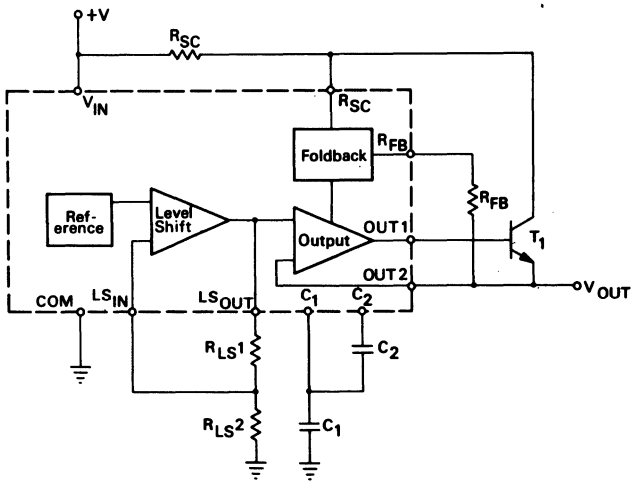


Figure 14.7. Current-expanded positive voltage regulator with foldback current limiting.

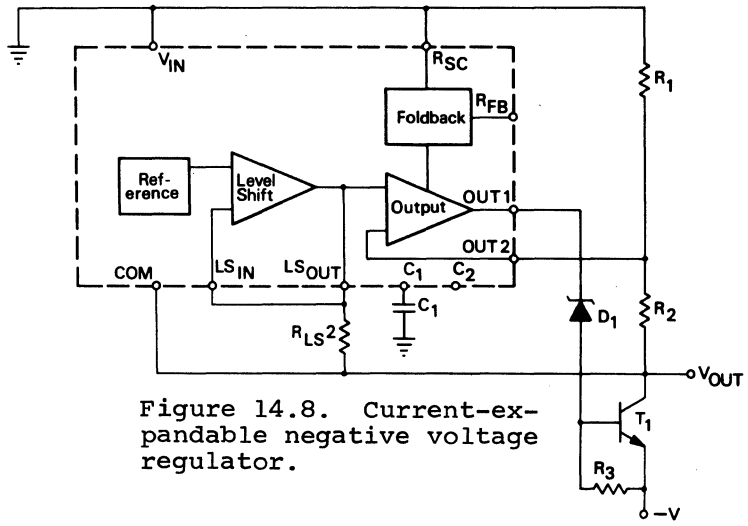


Figure 14.8. Current-expandable negative voltage regulator.

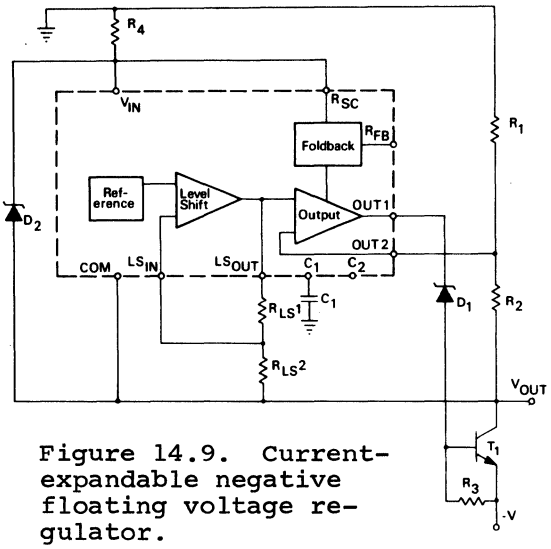


Figure 14.9. Current-expandable negative floating voltage regulator.

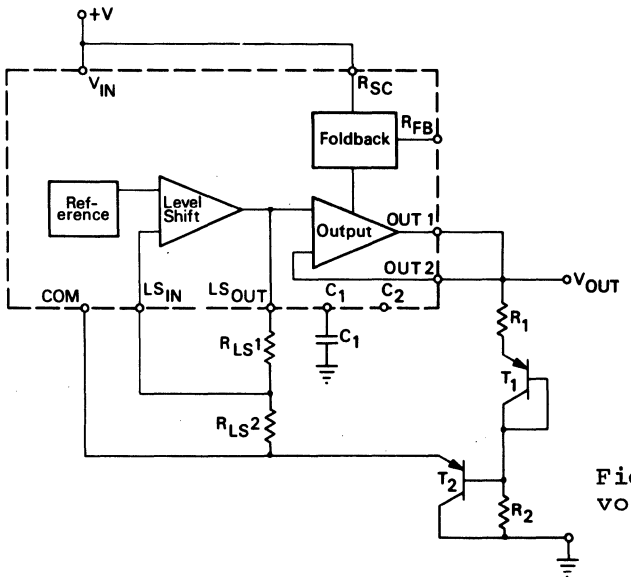


Figure 14.10. Positive floating voltage regulator.

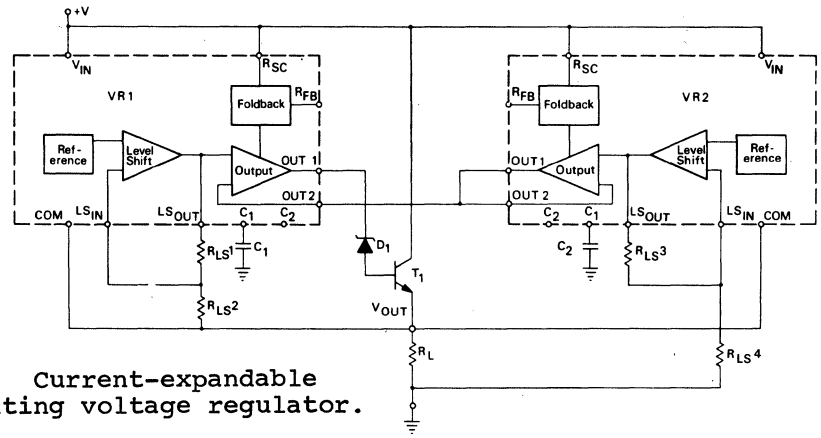


Figure 14.11. Current-expandable positive floating voltage regulator.

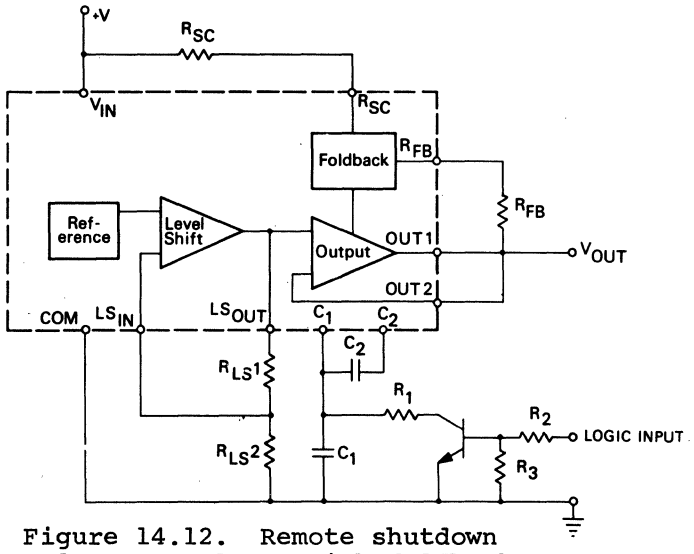


Figure 14.12. Remote shutdown voltage regulator with foldback current limiting.

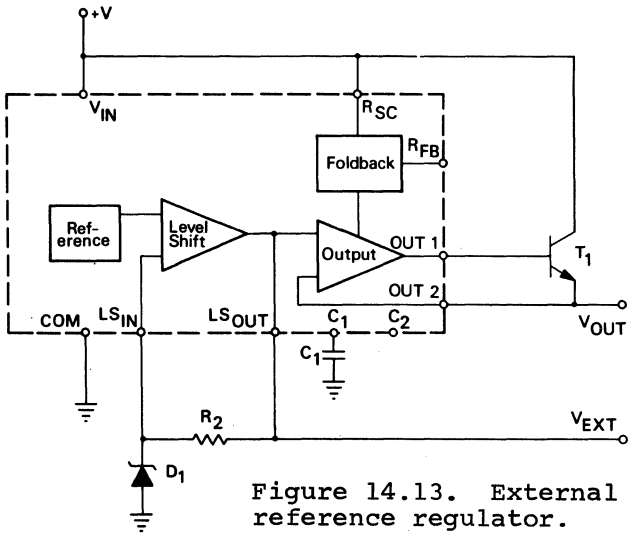


Figure 14.13. External reference regulator.

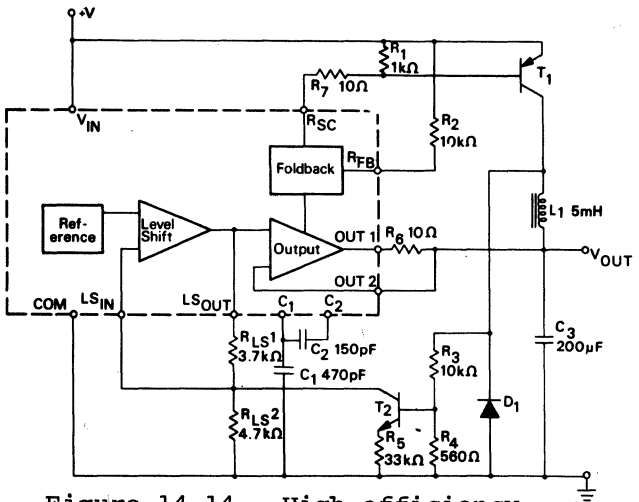


Figure 14.14. High-efficiency switching regulator.

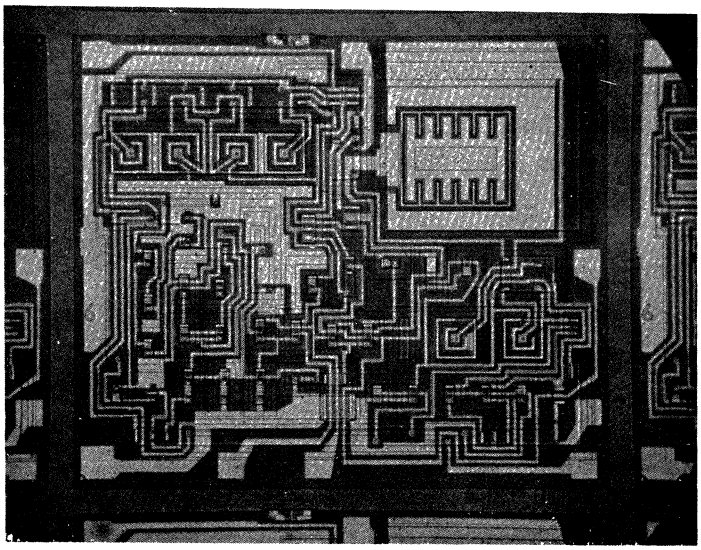


Figure 14.15. Photograph of TRV2000 voltage-regulator.

15

Integrated Voltage Regulators

by Edward L. Renschler
Motorola Semiconductor Products

A two-stage feedback regulator, in essence, consists of a regulator within a regulator. Examples of this type of voltage regulator are the MC1560 and the MC1561 (a higher voltage version of the MC1560).

In the MC1560 (or MC1561) circuit, shown in Figure 13.1, the difference between a temperature stable low-voltage reference E_R and a portion (E_A) of the desired output voltage E_A is amplified and used to control the first stage regulator. The regulator acts to maintain $\beta E_A = E_R$. From Figure 15.1:

$$\beta E_A = E_R = E_A \left(\frac{R_1}{R + R_1}\right) . \tag{15.1}$$

Rewriting equation 15.1:

$$E_A = \left(1 + \frac{R}{R_1}\right)E_R. \tag{15.2}$$

The regulated output voltage (E_A) of the first regulator stage is used as the reference voltage for the second regulator stage. The second regulator compares the output voltage E_o with E_A to maintain the output voltage equal to E_A. Therefore:

$$E_o = E_A = \left(1 + \frac{R}{R_1}\right)E_R \tag{15.3}$$

An advantage of this design approach is that the output is a function only of the external resistor ratio and of the internally generated OTC reference (E_R). The two external resistors can easily be chosen for matched temperature coefficients. Hence, the output is fixed and is not a function of the unregulated input, the regulated output voltage, or the ambient temperature.

The series pass transistor of the second regulator has a very large emitter geometry which enables it to handle large quantities of current, and at the same time exhibit a very low emitter resistance.

15.1 CIRCUIT OPERATION

The complete circuit diagram for the regulator is shown in Figure 15.2. The circuit operates as follows: when the unregulated input voltage V_{in} is applied to pin 3, a current I_A flows through the 60-kΩ resistor to bias the zener diode Z_1 at 6.8 V. Since the voltage across Z_1 is initially greater than the voltage across Z_2, diode D_1 is forward biased and conducts to supply current to Z_2, the main reference zener. As the voltage across Z_2 rises, Q_1 is biased on; this sets the bias for the rest of the regulator. When biased on, transistor Q_3 supplies a constant current to zener Z_2, maintaining the zener voltage constant. This voltage is used to set the reference voltage E_R in the first regulator at the base of Q_5.

Neglecting base currents, the current I_1 through the main bias line is:

$$I_1 \approx \frac{V_{Z_2} - 3V_{BE}}{4.63\ k\Omega + 2.67\ k\Omega + 700\ \Omega} \approx 0.6\ mA \qquad (15.4)$$

The reference voltage is:

$$E_R = V_{Z_2} - V_{BE} - (4.63k)\ I_1 \qquad (15.5)$$

$$E_R = 6.8\ V - 0.7\ V - (4.63\ k\Omega)\ (0.6\ mA)$$

$$E_R \quad 3.4\ V.$$

Diodes D_2 and D_3 serve as temperature compensating elements to give the reference voltage a zero temperature coefficient (OTC). Constant current sources Q_6, Q_7, and Q_8 also derive their bias voltage from the OTC bias chain, thus making these constant current sources independent of temperature variations. The pnp-npn composite transistors Q_3, Q_{12}, and Q_{13} are also used as constant-current sources to provide preregulation. The voltage reference for these sources is set up at the collector of Q_1 by the constant current I_1 drawn through the 834-Ω resistor.

The Darlington transistor pair Q_5 and Q_9 function as a differential comparator. The reference voltage at the base of Q_5 is compared with the voltage at pin 8 (dc shift sense), the base of Q_9. Under normal operation, pin 6 (output reference) is directly tied to pin 9 (dc shift output), thus the voltage at the emitter of Q_{10}, which is also the voltage at the collector of Q_9, is applied to the base of Q_{14}, and is used as the reference voltage for the second differential comparator consisting of transistors Q_{14} and Q_{15}. Diode D_4 serves to temperature compensate the base-emitter junction of transistor Q_{10}, and at the same time protects the regulator against the discharge of the noise capacitor (connected from pin 7 to ground) in the event that the regulator is shut off. Normally, pin 5 (output sense), the base of Q_{15} is tied directly to the output, so that the output voltage, or voltage at the load, is compared directly with the voltage at the base of Q_{14}.

Transistor Q_{11} provides protection to the differential amplifier composed of Q_{14} and Q_{15} when the output of the regulator is short circuited. Normally Q_{11} is off; however, when pin 5 is grounded, transistor Q_{11} conducts and prevents a reverse bias breakdown of the base-emitter junction of transistor Q_{15}.

Transistors Q_{16} and Q_{17} essentially forms a Darlington series pass output device; their large geometries allow for high current handling capabilities. Diodes D_5, D_6, and D_7 are used for short circuit or overcurrent protection. This is accomplished as shown in the circuit of Figure 15.3.

From Figure 15.3:

$$I_{SC}R_{SC} = -2V_{BE} + 3V_{BE} \tag{15.6}$$

$$= V_{BE} \text{ (if diodes } D_5, D_6, \text{ and } D_7 \text{ are conducting).}$$

Rearranging:

$$I_{SC} = \frac{V_{BE}}{R_{SC}} \approx \frac{0.7\ V}{R_{SC}} \quad (\dot{2}5^{o}C) \tag{15.7}$$

Thus when I_{SC} equals the value found above, the diode path conducts, reducing the base drive to the Darlington output device by shunting current through the diode line. By decreasing the current out of the output device, the power dissipation of the device is reduced to a safe level under a short circuit condition. The desired R_{SC} for a specified maximum load current can be determined from the curve shown in Figure 15.3.

Diode D_8 and transistor Q_2 form the MC1560's "shutdown control". When the voltage at pin 2 exceeds $2V_{BE}$, D_8 is forward biased and Q_2 conducts. The current previously flowing through zener Z_2 is shunted through Q_2; thus the bias is removed from the rest of the circuit causing the regulator to shut down. During this shutdown mode, the regulator draws a maximum of 300 μA standby current. When driving pin 2, the designer must ensure that the drive current into pin 2 never exceeds 10 mA. The reason for this is obvious from Figure 15.2.

15.2 BASIC OPERATION

The basic MC1560 voltage regulator circuit is shown in Figure 15.4. As previously stated, resistors R and R_1 form the feedback network which sets the voltage at pin 6, and consequently the output voltage. Hence, the output voltage can be easily adjusted by varying the resistor R. Since pin 8 is the base of a Darlington input comparator, the input current to pin 8 is extremely small and R and R_1 may be selected with little regard for their parallel resistance. For operation where temperature variations are critical, resistors R and R_1 should have the same temperature coefficient. Recalling that the voltage at pin 8 will be equal to the reference voltage, 3.4 V, then from Figure 15.1:

$$E_R = 3.4\ V = IR_1. \tag{15.8}$$

If R_1 is selected as 6.8 kΩ, then $I \approx 0.5$ mA.

The output voltage is:

$$E_o = E_A = E_R + IR. \tag{15.9}$$

If R is in kΩ and the current, I, is 0.5 mA, the output voltage is given by:

$$E_o = 3.4\ V + R/2 \tag{15.10}$$

and hence the output voltage is a linear function of resistor R. This alone points out a number of possible uses for this regulator such as a programmed supply for testing purposes.

An actual plot of this linear function of R is shown in Figure 15.5. The plot will remain linear to E_o = 32 V for the MC1561 (not shown). Because the MC1560 design makes use of high quality VHF transistors in its design, normal high-frequency precautions should be taken when using MC1560 circuits. The series capacitor-resistor combination of 0.1 μF and R_2 on the input and output may be necessary to "de-Q" any unintentional VHF tank circuits caused by large lead inductance. This technique also permits the use of an aluminum electrolytic for C_0. If a tantalum capacitor is used for C_0, the output "de-Qing" network may not be required because of the tantalum capacitor's small inductive reactance.

C_n causes a reduction in output noise by filtering the noise at the output of the first regulator stage. A 0.1 μF capacitor reduces the output noise to typical values of less than 150 μV rms. C_0 should be greater than 10 μF for the basic connection, and larger values such as $C_0 \geq 50$ μF should be used in such applications as current boosting and voltage boosting. The output resistor R_3 is chosen to draw a minimum current of 1 mA with no external load. R_{SC} provides current limiting for short-circuit protection and can be chosen from Figure 15.3. The addition of R_{SC} does not affect the output impedance appreciably and as a consequence, the load regulation also is relatively uneffected by the addition of R_{SC}. This is not the case with many voltage regulators.

The unregulated input voltage, E_{in}, must be greater than 8.5 V to properly bias the MC1560. Also, E_{in} should exceed E_0 by at least the minimum "input-output voltage differential" which is typically 2.1 Vdc.

15.3 SHUTDOWN

A circuit which makes use of the MC1560's "shutdown" control to protect the device from output short circuiting is shown in Figure 15.6. This circuit, as shown, does not give overcurrent protection but, with R_{SC} added, both types of protection are provided. In this circuit, Q_1 is normally saturated because of the base drive supplied through the resistor divider R_1 and R_2.

With Q_1 in saturation, the voltage on pin 2, the shutdown control, is the collector-to-emitter saturation voltage of Q_1 which is considerably smaller than the input necessary to overcome the threshold of pin 2. But if the output is short circuited, Q_1 turns off, the voltage at pin 2 rises and thus shutdown of the regulator occurs. Under a short circuited output condition, the standby current to the regulator is in the order of a few microamperes. Resistors R_1 and R_2 can be chosen to saturate Q_1 as well as sink the minimum regulator load current of 2mA. Resistor R_3 limits the current to pin 2 when Q_1 turns off. Capacitor C_1 is necessary as it permits an R_3C_1 time constant which prevents shutdown when E_{in} is initially applied. When the short circuit is removed, the regulator automatically comes back-up to full regulation.

Another possible use of the shutdown feature is shown in Figure 15.7. Since shutdown of the regulator is initiated when the voltage at pin 2 exceeds $2V_{BE}$ i.e., when diode D_8 and transistor Q_2 (See Figure 15.2) are forward biased, the MC1560's monolithic

processing can provide a novel protection scheme. Diode D_8 and transistor Q_2's junctions are at approximately the same temperature as the output device, hence a fixed dc voltage at pin 2 can provide automatic shutdown when a predetermined junction temperature is reached.

The zener diode provides the fixed dc voltage which can be varied by varying R_b. A zero TC zener is necessary if the complete circuit will be subjected to temperature change. The voltage required at threshold pin 2 will decrease by approximately 4 mV/°C as the junction temperature increases.

For example, assume it is desired to shut the regulator down when the junction temperature (T_j) reaches +125°C (assume V_{BE} = 0.7 V at +25°C). The voltage on pin 2, V_A, needed to threshold the shutdown mechanism at the elevated temperature is:

$$V_A = 2V_{BE}(25^\circ C) + 2\left(\frac{\Delta V_{BE}}{\Delta T}\right)(\Delta T) \tag{15.11}$$

$$V_A = 1.4\ V + 2\left(\frac{-2\ mV}{^\circ C}\right)(100^\circ C)$$

$$V_A = 1.4\ V + \left(\frac{-4\ mV}{^\circ C}\right)(100^\circ C)$$

$$V_A = 1.4\ V - 0.4\ V$$

$$V_A = 1.0\ V$$

Therefore, with V_A = 1.0 V, shutdown will occur at approximately T_j = 125°C. Since the junction temperature is not easily measured, one needs to relate T_j to a more easily measured quantity such as the ambient temperature, T_A. This is done by use of the following relation:

$$T_j = T_a + \theta_T P_D \tag{15.12}$$

$$\theta_T = \theta_{jc} + \theta_{cs} + \theta_{sa} \tag{15.13}$$

where P_D = power dissipated in the device, θ_{jc} = devices thermal resistance, junction to case, θ_{cs} = insulator thermal resistance, case to heat sink, and θ_{sa} = heat sink thermal resistance, heat sink to ambient.

Using the power dissipation derating specifications for the MC1560, θ_{jc} is approximately calculated as 8.35°C/W for the R package (load current rating: 200 mA dc) and 69.5°C/watt for the G package (load current rating: 500 mA dc). G designates a TO-5 case; R denotes a TO-66 power package.

As an example, assume an MC1560R regulator is dissipating 2 W. Also assume θ_{cs} = .65°C/W and θ_{sa} = 10°C/W. Then

$$\theta_T = (8.35 + 0.65 + 10.0)\ ^\circ C/W \tag{15.14}$$

$$\theta_T = 19^\circ C/W$$

and

$$T_j = T_a + \theta_T P_D \tag{15.15}$$

$$T_j = T_a + (19^\circ C/W)\ (2\ W)$$

$$T_j = T_a + 38^\circ C.$$

Thus the junction temperature in this example will be 38°C hotter than the ambient temperature. Consequently, the circuit can be adjusted to automatically shutdown at a prespecified ambient temperature.

15.4 NPN CURRENT BOOST

By using the MC1560 with an external power transistor, much higher output power and improved load regulation can be realized. The improved regulation results because of the increased loop gain added by the external transistor and the corresponding decrease in output impedance. An npn current boosting circuit with "over-current protection" (R_{SC}) is shown in Figure 15.8. A curve of the typical load characteristic is given in Figure 15.9. Input regulation characteristics are the same as those given on the MC1560 data sheet.

A high-efficiency low-voltage npn current-boosting configuration is given in Figure 15.10. The low-voltage supply applied to the external series pass transistor minimizes the input-output differential for less power dissipation in the series pass device, hence improving efficiency. The shutdown control, Q_a, is used here to turn the MC1560 off when $V_2 = 0$, so that, under this condition, the MC1560 will not try to supply the full load current.

The R_{SC}, Q_C combination provides output short-circuit protection. Q_C is normally off but will conduct when $I_{SC}\ R_{SC}$ exceeds V_{BE}. The collector current, I_C ($\approx I_E$), of Q_C has a maximum of approximately 0.6 ma when the output is short circuited, so Q_C can be any low gain, low-power npn transistor. Load regulation is typically better than or equal to the values shown in Figure 15.9, and efficiencies of 75% are easily realized.

15.5 VOLTAGE BOOST

A circuit that offers a voltage boost plus output short-circuit protection is shown in Figure 15.11. The reference voltage for the input of the regulator (pin 3) is obtained by using the zener diode, Z_1. In Figure 15.11, a Vin of 20 Vdc is supplied to the MC1560. The regulator is biased so as to produce an output of +15 V. Zener diode Z_2 is a 47-V device, which will raise the potential at the base of the high pass transistor to about 62 V. The 5.1-kΩ resistor, the IN4001 diode, and the 2kΩ resistor from the +75 V input to ground insures that Z_2 is always operating with the proper zener voltage across it. The 6.2-Ω resistor, the 620-Ω resistor, and the 2N4123 transistor provide output short-circuit protection. When the output is shorted, the 2N4123 transistor conducts, turning off the 2N3738 high-pass transistor.

The IN4001 diode and the 2-kΩ resistor insure that the regulator output is always loaded (1 mA), and that a short circuit on the 60 V output terminal will not pull excessive current out of the MC1560. In addition, it should be noted that zener Z_2 is "inside" the closed loop and consequently the output voltage is uneffected by fluctuations in zener Z_2.

15.6 AUTOMATIC ON-OFF SEQUENCING

The circuit of Figure 15.12 is offered as an example of a circuit that will automatically turn the regulator off when the output becomes short circuited, and will periodically "look" at the output to determine when the output is safe to return the regulator to operation.

In normal operation, Q_2 is saturated, holding Q_1 and Q_3 in an off condition. When the output of the regulator is shorted to ground, Q_2 is turned off, allowing the 20 μF capacitor to charge. As the capacitor is charged, the threshold of pin 2 is reached, turning off the regulator. As the charging continues, the threshold of the unijunction is reached and it fires. This causes the capacitor to discharge, reducing the potential at the base of Q_1. As long as the short remains, the system will continue to cycle (at a low duty cycle and low power dissipation) until the short is removed. When the short is removed, the regulator will return to full regulation. This concept is very attractive for systems that operate unattended.

15.7 DUAL SUPPLY

Figure 15.13 shows a configuration for obtaining two regulated voltages from a single regulator package. The circuit operates as follows. The output from the reference amplifier normally appears at pin 9, the top of resistor R for the single output voltage configuration. If a current-boost transistor (Q_1 in Figure 15.13) is added between pin 9 and R, the reference voltage at R_1 will remain essentially constant while a usable amount of current may now be drawn out of the reference. The value of the reference is still established by R_1 and R, in the normal fashion.

The output amplifier may now be used with all or part of the reference existing as V_{O1}. In the circuit shown in Figure 15.13, a resistive divider applies half of V_{O1} as the reference for the output amplifier. The sense lead, pin 5, is connected to the output to compare V_{O2} with $V_{O1/2}$. Short circuit protection is provided internally for V_{O2}, and the diode string shunts bias current for Q_1 at overloads. Figure 15.14 illustrates the output voltage, V_{O1} and V_{O2}, vs load current for the configuration shown in Figure 15.13.

15.8 DUAL SUPPLY TRACKING REGULATOR

The MC1560 can be used very effectively as a highly stable, zero-temperature-coefficient reference for a dual-supply regulator. Figure 15.15 illustrates this idea. In Figure 15.15, the MC1560G supplies a +15 V reference voltage (V_{REF}) to the system. MC1539G Operational Amplifiers are used as error sensing elements.

With $\pm$20 V unregulated inputs, $\pm$15 V regulated outputs voltages (with regulation better than 0.01%) and a 300mA capability are provided. This type of supply is very useful in generating the well regulated voltages required to supply power to a system containing operational amplifiers, video amplifiers, and other monolithic integrated circuits.

15.9 REGULATOR CAPABILITIES

The performance capabilities of the monolithic voltage regulators described in this article can be summarized as:

	MC1560	MC1561
Output voltage range (Vdc)	+2.5 to +17	+2.5 to +32.0
Input voltage range (Vdc)	+8.5 to +20	+8.5 to +35.0
Typical required input-output voltage differential, $V_{in} - V_{out}$, (Vdc)	2.1	2.1
T. C. of output voltage (%/^{o}C)	$\pm$0.002	$\pm$0.002
Load current (without external transistor):		
Typical input regulation (%/V_{in})	0.002	0.002
Typical output impedance (dc to 100 kHz), Ω:	0.015	0.020

FIGURES

Figure 15.1. Regulator block diagram.

Figure 15.2. Complete circuit diagram for the voltage regulator.

Figure 15.3. Short-circuit function vs short-circuit resistance.

Figure 15.4. Basic voltage regulator circuit. Resistors R and R_1 form the feedback network which determined the value of the output voltage.

Figure 15.5. Output voltage as a function of resistor R.

Figure 15.6. The shutdown circuit.

Figure 15.7. Protection circuitry for limiting junction temperature.

Figure 15.8. The npn current-boast circuit.

Figure 15.9. Load regulation vs load current, for the npn boost circuit (See Figure 15.11).

Figure 15.10. High-efficiency npn current-boost circuit.

Figure 15.11. An npn voltage-boost circuit.

Figure 15.12. ON-OFF sequencing circuit.

Figure 15.13. Dual supply circuit.

Figure 15.14. Dual-supply output voltage vs load current.

Figure 15.15. Tracking dual supply regulator.

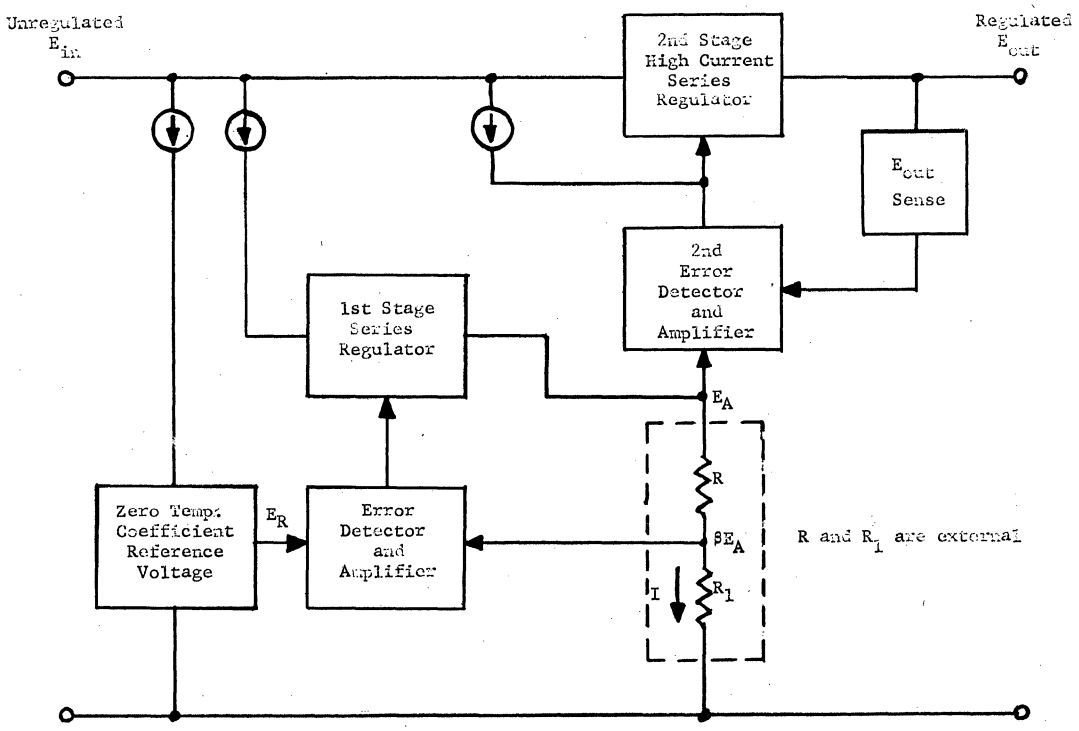


Figure 15.1. Regulator block diagram.

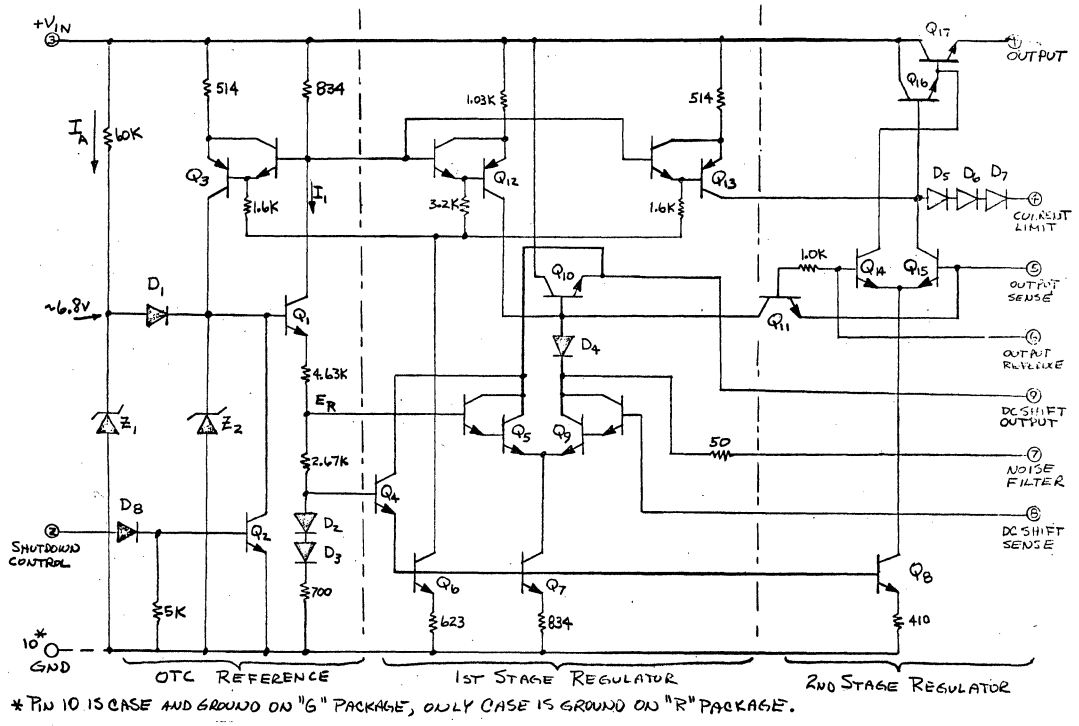


Figure 15.2. Complete circuit diagram for the voltage regulator.

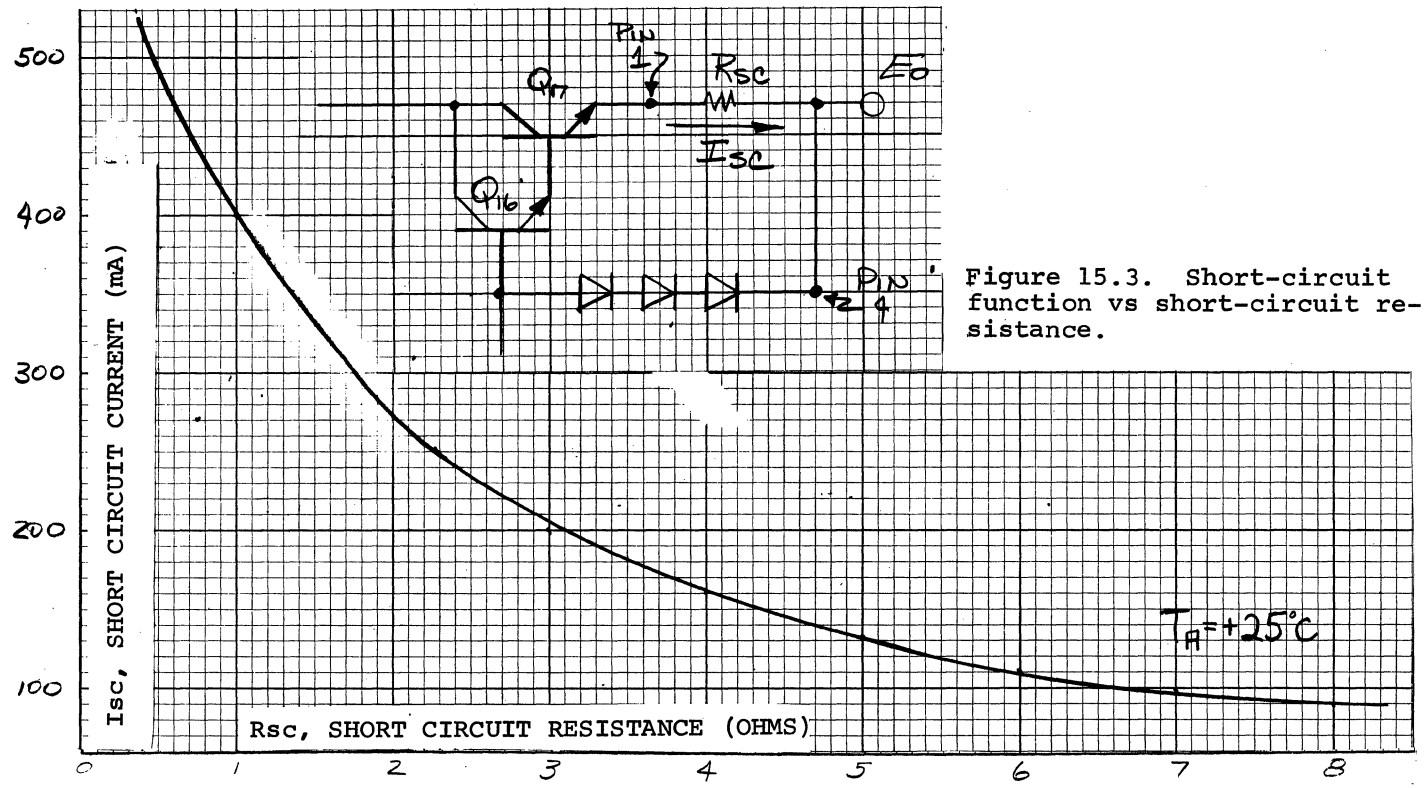


Figure 15.3. Short-circuit function vs short-circuit resistance.

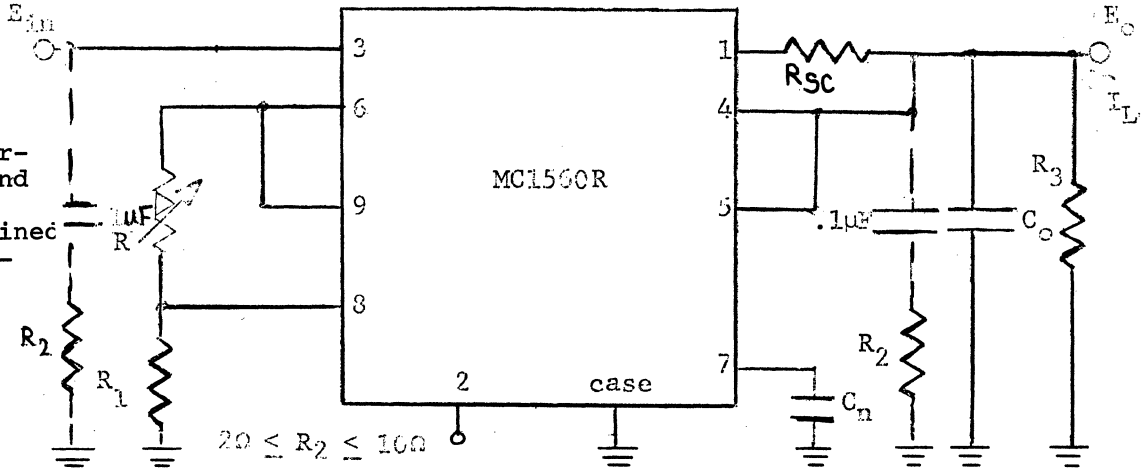


Figure 15.4. Basic voltage regulator circuit. Resistors R and R_1 form the feedback network which determines the value of the output voltage.

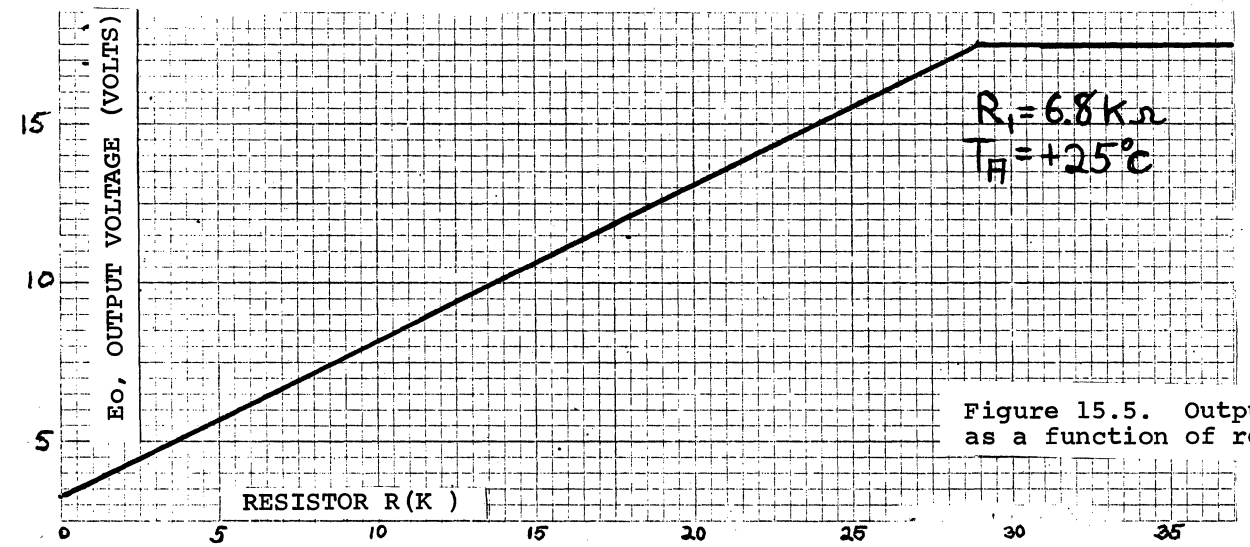


Figure 15.5. Output voltage as a function of resistor R.

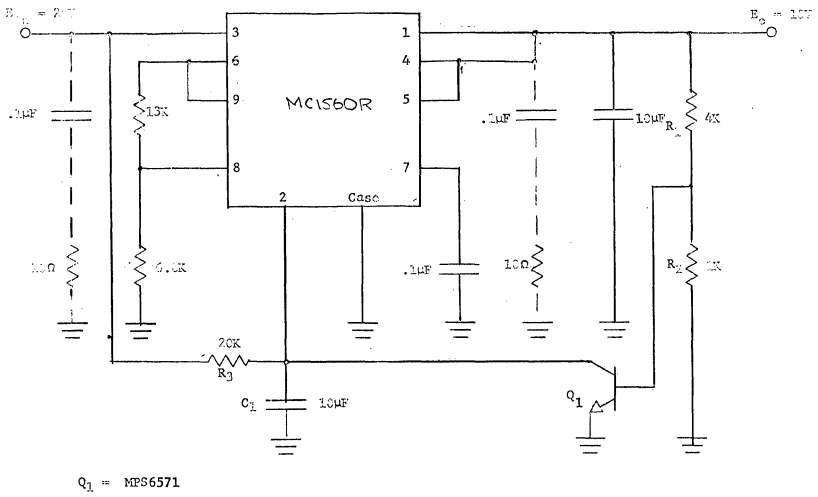
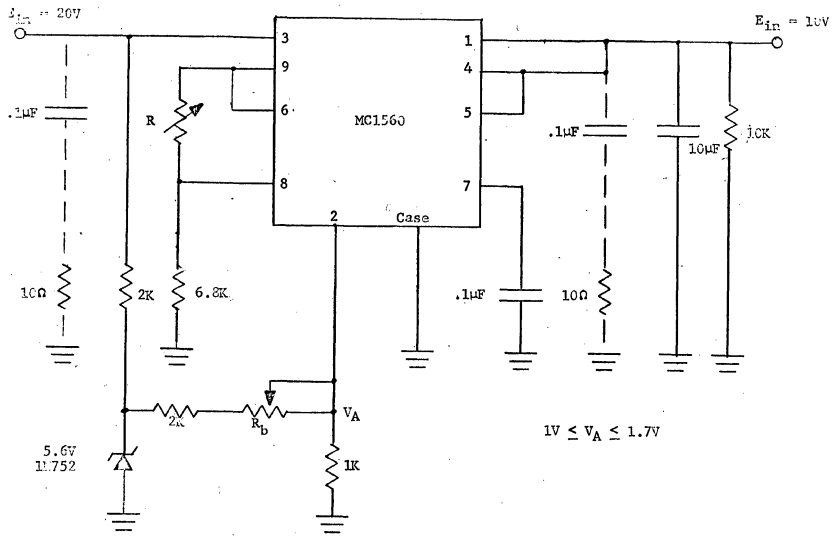


Figure 15.6. The shutdown circuit.

Figure 15.7. Protection circuitry for limiting junction temperature.



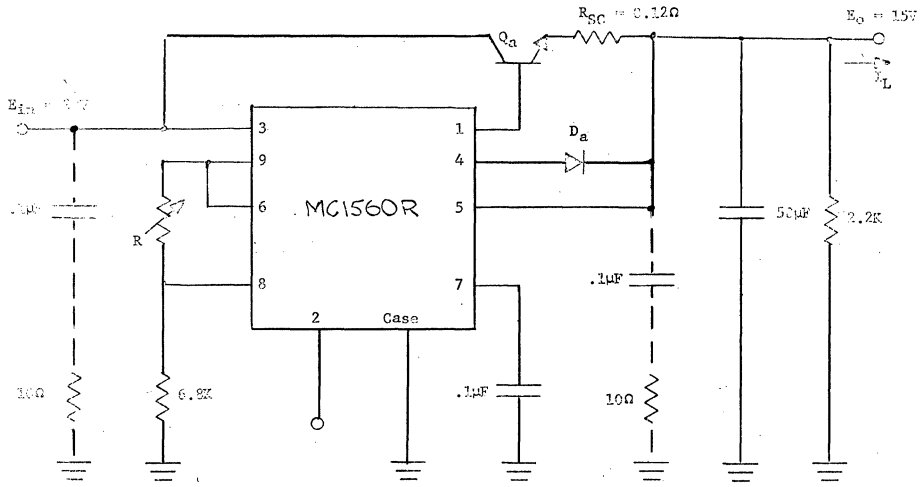


Figure 15.8. The npn current-boast circuit.

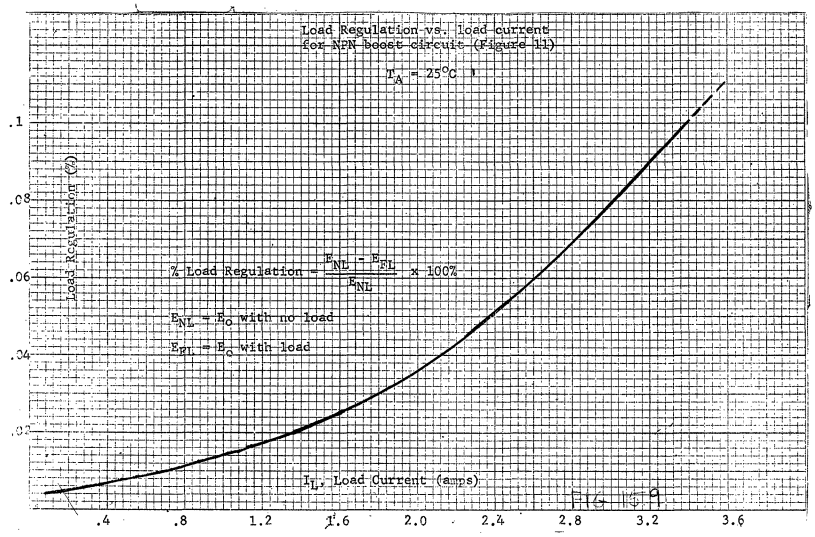
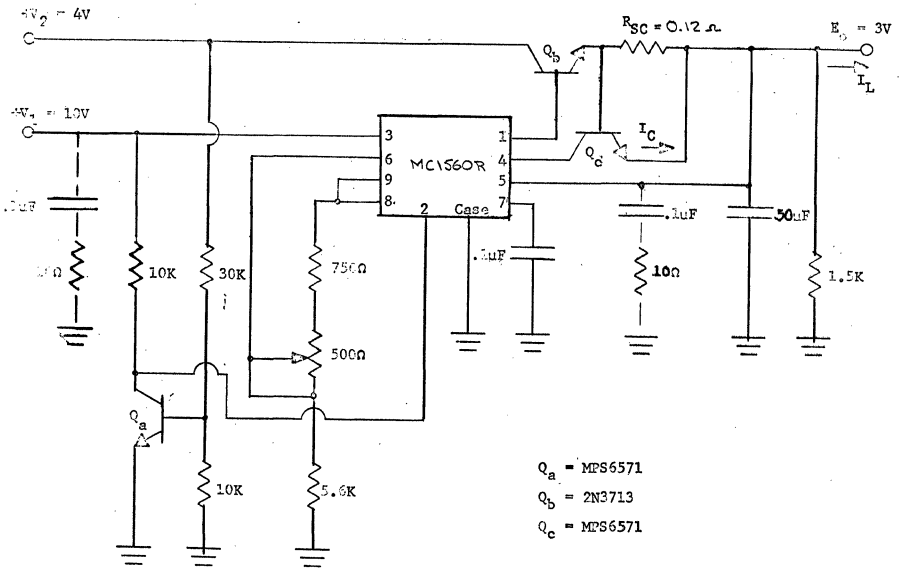


Figure 15.9. Load regulation vs load current, for the npn boost circuit (See Figure 15.11)

Figure 15.10. High-efficiency npn current-boost circuit.



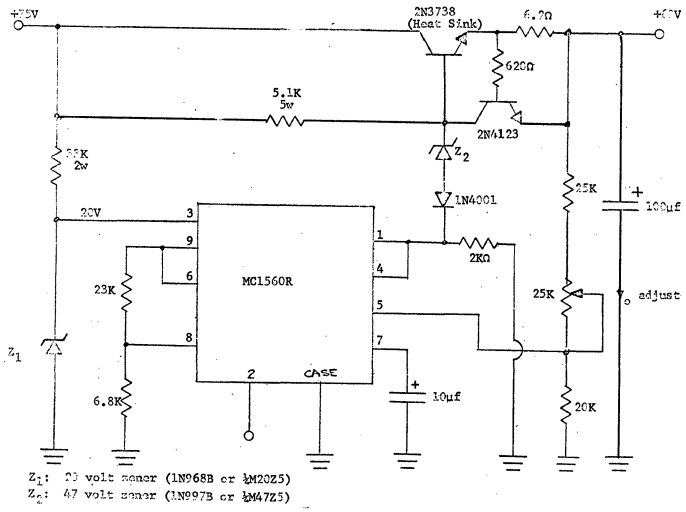


Figure 15.11. An npn voltage-boost circuit.

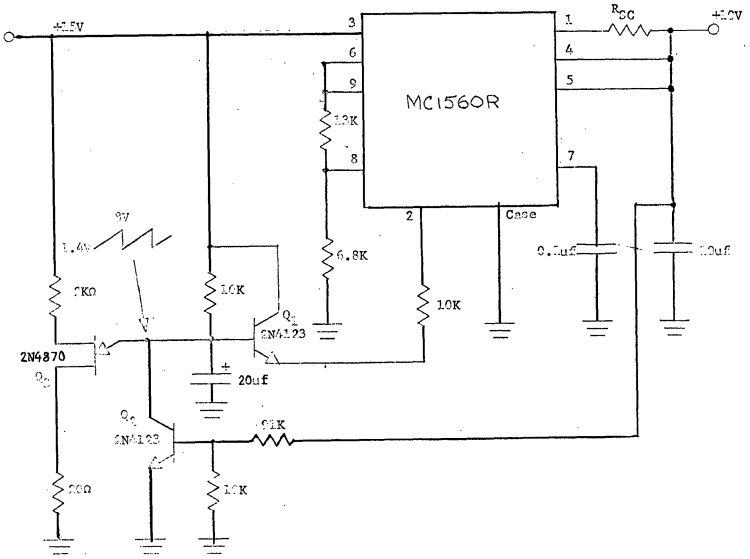


Figure 15.12. ON-OFF sequencing circuit.

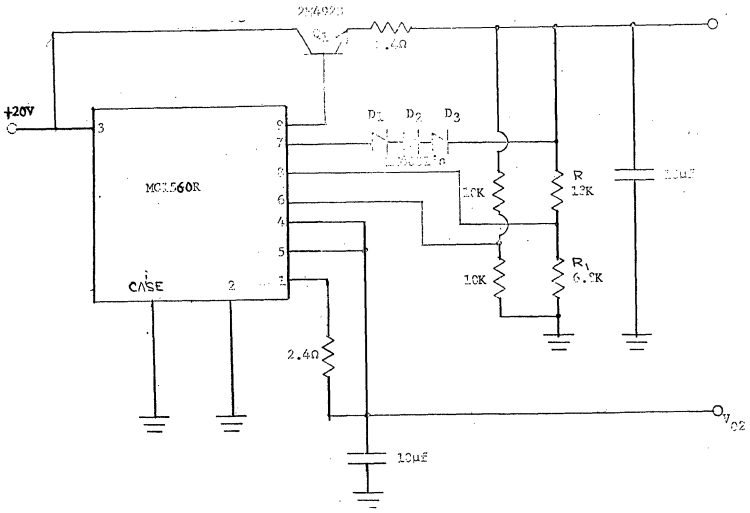


Figure 15.13. Dual supply circuit.

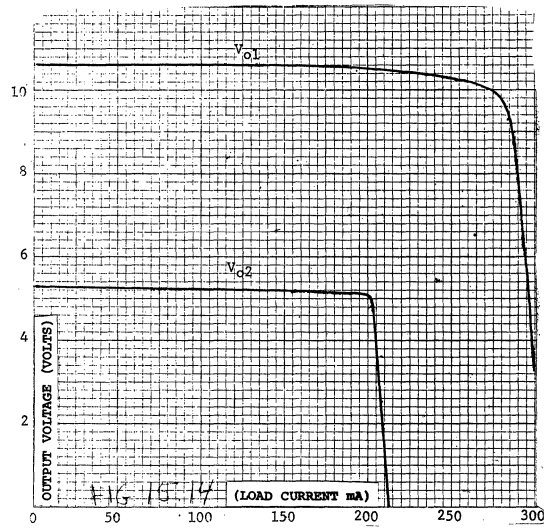


Figure 15.14. Dual-supply output voltage vs load current.

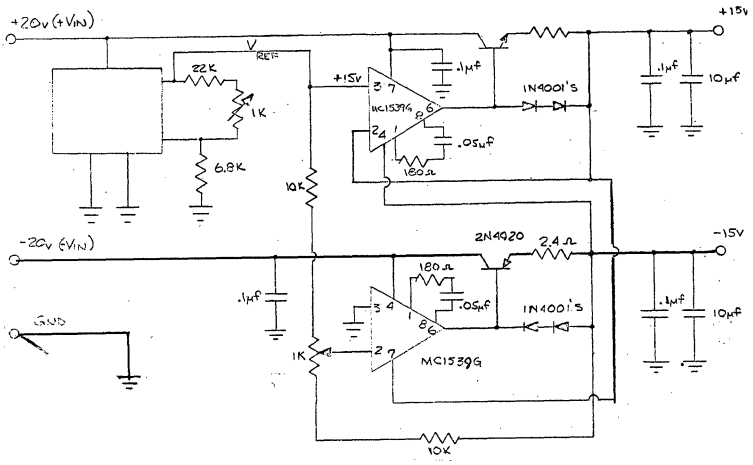


Figure 15.15. Tracking dual supply regulator.

16

Positive Voltage Regulators

by Robert J. Widlar
National Semiconductor

IC voltage regulators are seeing rapidly increasing usage. The LM100, one of the first, has already been widely accepted. Designed for versatility, this circuit can be used as a linear regulator, a switching regulator, a shunt regulator, or even a current regulator. The output voltage can be set between 2 V and 30 V with a pair of external resistors, and the IC works with unregulated input voltages down to 7 V. Dissipation limitations of the IC package restrict the output current to less than 20 mA, but external transistors can be added to obtain output currents in excess of 5 A. The use of the LM100 in many applications has been described (1-3).

One complaint that has been raised about the LM100 is that it does not have good enough regulation for certain applications. In addition, it becomes difficult to prove that the load regulation is satisfactory under worst-case design conditions. These problems prompted development of the LM105, which is nearly identical to the LM100 except that a gain stage has been added for improved regulation. In the great majority of applications, the LM105 is a plug-in replacement for the LM100.

16.1 AN IMPROVED REGULATOR

The load regulation of the LM100 is about 0.1%, no load to full load, without current limiting. When short-circuit protection is added, the regulation begins to degrade as the output current becomes greater than about one half the limiting current. This is illustrated in Figure 16.1. The LM105, on the other hand, gives 0.1% regulation up to currents closely approaching the short-circuit current. As shown in Figure 16.1b, this is particularly significant at high temperatures.

The current limiting characteristics of a regulator are important for two reasons: first, it is almost mandatory that a regulator be short-circuit protected because the output is distributed to enough places that the probability of it becoming shorted is quite high. Secondly, the sharpness of the limiting characteristics is not improved by the addition of external booster transistors. External transistors can increase the maximum output current, but they do not improve the load regulation at currents approaching the short-circuit current. Thus, it can be seen that the LM105 provides more than ten times better load regulation in practical power supply designs.

Figure 16.2 shows that the LM105 also provides better line regulation than the LM100. These curves give the percentage change in output voltage for an incremental change in the unregulated input voltage. They show that the line regulation is worst for small differences between the input and output voltages. The LM105 provides about three times better regulation under worst-case conditions. Bypassing the internal reference of the regulator makes the ripple rejection of the LM105 almost a factor of ten better than the LM100 over the entire operating range, as shown in the figure. This bypass capacitor also eliminates noise generated in the internal reference zener of the IC.

The LM105 has also benefited from the use of new IC components developed after the

LM100 was designed. These have reduced the internal power consumption so that the LM105 can be specified for input voltages up to 50 V and output voltages to 40 V. The minimum preload current required by the LM100 is not needed on the LM105.

16.2 CIRCUIT DESCRIPTION

The differences between the LM100 and the LM105 can be seen by comparing the schematic diagrams in Figures 16.3 and 16.4. Q_4 and Q_5 have been added to the LM105 to form a common-collector, common-base, common-emitter amplifier; a single common-emitter differential amplifier was used in the LM100.

In the LM100, generation of the reference voltage starts with zener diode, D_1, which is supplied with a fixed current from one of the collectors of Q_2. This regulated voltage, which has a positive temperature coefficient, is buffered by Q_4, divided down by R_1 and R_2 and connected in series with a diode-connected transistor, Q_7. The negative temperature coefficient of Q_7 cancels out the positive coefficient of the voltage across R_2, producing a temperature-compensated 1.8 V on the base of Q_8. This point is also brought outside the circuit so that an external capacitor can be added to bypass any noise from the zener diode.

Transistors Q_8 and Q_9 make up the error amplifier of the circuit. A gain of 2000 is obtained from this single stage by using a current source, another collector on Q_2, as a collector load. The output of the amplifier is buffered by Q_{11} and used to drive the series-pass transistor, Q_{12}. The collector of Q_{12} is brought out so that an external pnp transistor, or pnp-npn combination, can be added for increased output current.

Current limiting is provided by Q_{10}. When the voltage across an external resistor connected between pins 1 and 8 becomes high enough to turn on Q_{10}, it removes the base drive from Q_{11} so the regulator exhibits a constant-current characteristic. Prebiasing the current-limit transistor with a portion of the emitter-base voltage of Q_{12} from R_6 and R_7 reduces the current-limit sense voltage. This increases the efficiency of the regulator, especially when fold-back current limiting is used. With foldback limiting, the voltage dropped across the current sense resistor is about four times larger than the sense voltage.

As for the remaining details, the collector of the amplifier, Q_9, is brought out so that external collector-base capacitance can be added to frequency-stabilize the circuit when it is used as a linear regulator. R_9 and R_4 are used to start up the regulator, while the rest of the circuitry establishes the proper operating levels for the current source transistor, Q_2.

The reference circuitry of the LM105 is the same, except that the current through the reference divider, R_2, R_3, and R_4, has been reduced by a factor of two on the LM105 for reduced power consumption. In the LM105, Q_2 and Q_3 form an emitter-coupled amplifier, with Q_3 being the emitter-follower input and Q_2 the common-base output amplifier. R_6 is the collector load for this stage, which has a voltage gain of about 20. The second stage is a differential amplifier, using Q_4 and Q_5. Q_5 actually provides the gain. Since it has a current source as a collector load, one of the collectors of Q_{12}, the gain is quite high: about 1500. This gives a total gain in the error amplifier of about 30,000 which is ten times higher than the LM100.

It is not obvious from the schematic, but the first stage (Q_2 and Q_3) and second stage (Q_4 and Q_5) of the error amplifier are closely balanced when the circuit is operating. This will be true regardless of the absolute value of components and over the operating temperature range. The only thing affecting balance is component matching, which is good in a monolithic integrated circuit, so the error amplifier has good drift characteristics over a wide temperature range.

Frequency compensation is accomplished with an external integrating capacitor around the error amplifier, as with the LM100. This scheme makes the stability insensitive to loading conditions -- resistive or reactive -- while giving good transient response. However, an internal capacitor, C_1, is added to prevent minor-loop oscillations due to the increased gain.

Additional differences between the LM100 and LM105 are that a field-effect transistor, Q_{18}, connected as a current source starts the regulator when power is first applied. Since this current source is connected to ground, rather than the output, the minimum load current before the regulator drops out of operation with large input-output voltage differentials is greatly reduced. This also minimizes power dissipation in the integrated circuit when the difference between the input and output voltage is at the worst-case value. With the LM105 circuit configuration, it was necessary to add Q_{17} to eliminate a latch-up mechanism which could exist with lower output-voltage settings. Without Q_{17}, this could occur when Q_3 saturated and cut off the second-stage amplifiers, Q_4 and Q_5, causing the output to latch at a voltage nearly equal to the unregulated input.

16.3 POWER LIMITATIONS

Although it is desirous to put as much of the regulator as possible on the IC chip, there are certain basic limitations. For one, it is not a good idea to put the series pass transistor on the chip. The power that must be dissipated in the pass transistor is too much for practical IC packages. Further, IC's must be rated at a lower maximum operating temperature than power transistors. This means that even with a power package, a more-massive heat sink would be required if the pass transistor was included in the IC.

Assuming that these problems could be solved, it is still not advisable to put the pass transistor on the same chip with the reference and control circuitry: changes in the unregulated input voltage or load current produce gross variations in chip temperature. These variations worsen load and line regulation due to temperature interaction with the control and reference circuitry.

To elaborate, it is reasonable to neglect the package problem since it is potentially solvable. The lower, maximum operating temperatures of IC's, however, present a more basic problem. The control circuitry in an IC regulator runs at fairly low currents. As a result, it is more sensitive to leakage currents and other phenomena which degrades the performance of semiconductors at high temperatures. Hence, the maximum operating temperature is limited to 150°C in military temperature range applications. On the other hand, a power transistor operating at high currents may be run at temperatures up to 200°C, because even a 1 mA leakage current would not affect its operation in a

properly designed circuit. Even if the pass transistor developed a permanent 1 mA leakage from channeling, operating under these conditions of high stress, it would not affect circuit operation. These conditions would not trouble the pass transistor, but they would most certainly cause complete failure of the control circuitry.

These problems are not eliminated in applications with a lower maximum operating temperature. Integrated circuits are sold for limited temperature range applications at considerably lower cost. This is based mainly on a lower maximum junction temperature. They may be rated so that they do not blow up at higher temperatures, but they are not guaranteed to operate within specifications at these temperatures. Therefore, in applications with a lower maximum ambient temperature, it is necessary to purchase an expensive full-temperature-range part in order to take advantage of the theoretical maximum operating temperatures of the IC.

Figure 16.5 makes the point about dissipation limitations more strongly. It gives the maximum short-circuit output current for an IC regulator in a TO-5 package, assuming a 25°C temperature rise between the chip and ambient and a quiescent current of 2 mA. Dual, in-line or flat packages give results which are, at best, slightly better, but are usually worse. If the short circuit current is not of prime concern, Figure 16.5 can also be used to give the maximum output current as a function of input-output voltage differential. However, the increased dissipation due to the quiescent current flowing at the maximum input voltage must be taken into account. In addition, the input-output differential must be measured with the maximum expected input voltages.

The 25°C temperature rise assumed in arriving at Figure 16.5 is not at all unreasonable. With military-temperature-range parts, this is valid for a maximum junction temperature of 150°C with a 125°C ambient. For low-cost parts, marketed for limited-temperature-range applications, this maximum differential appropriately derates the maximum junction temperature.

In practical designs, the maximum permissible dissipation will always be to the left of the curve shown for an infinite heat sink in Figure 16.5. This curve is realized with the package immersed in circulating acetone, freon or mineral oil. Most heat sinks are not quite as good.

To summarize, power transistors can be run with a temperature differential, junction to ambient, three to five times as great as an integrated circuit. This means that they can dissipate much more power, even with a smaller heat sink. This, coupled with the fact that low-cost, multilead power packages are not available and that there can be thermal interactions between the control circuitry and the pass transistor, strongly suggests that the pass transistors be kept separate from the integrated circuit.

16.4 USING BOOSTER TRANSISTORS

Figure 16.6 shows how an external pass transistor is added to the LM105. The addition of an external pnp transistor does not increase the minimum input output voltage differential. This would happen if an npn transistor was used in a compound emitter-follower connection with the npn output transistor of the IC. A single-diffused, wide-base transistor like the 2N3740 is recommended because it causes fewer

oscillation problems than double-diffused, planar devices. In addition, it seems to be less prone to failure under overload conditions; and low-cost devices are available in power packages like the TO-66 or even TO-3.

When the maximum dissipation in the pass transistor is less than about 0.5 W, a 2N2905 may be used as a pass transistor. However, it is generally necessary to carefully observe thermal deratings and provide some sort of heat sink.

In the circuit of Figure 16.6, the output voltage is determined by R_1 and R_2. The resistor values are selected based on a feedback voltage of 1.8 V to pin 6 of the LM105. To keep thermal drift of the output voltage within specifications, the parallel combination of R_1 and R_2 should be approximately 2 kΩ. However, this resistance is not critical. Variations of ±30% will not cause appreciable effects.

The 1-μ F output capacitor C_2 is required to suppress oscillations in the feedback loop involving the external booster transistor Q_1 and the output transistor of the LM105. C_1 compensates the internal regulator circuitry to make the stability independent for all loading conditions. C_3 is not normally required if the lead length between the regulator and the output filter of the regulator is short.

Current limiting is provided by R_3. The current-limit resistor should be selected so that the maximum voltage drop across it, at full load current, is equal to the voltage given in Figure 16.7 at the maximum junction temperature of the IC. This assures a no-load to full-load regulation of better than 0.1% under worst-case conditions.

The short-circuit output current is also determined by R_3. Figure 16.8 shows the voltage drop across this resistor, when the output is shorted, as a function of junction temperature in the IC. With the type of current limiting used in Figure 16.6, the dissipation under short circuit conditions can be more than three times the worst-case full-load dissipation. Hence, the heat sink for the pass transistor must be designed to accommodate the increase dissipation if the regulator is to survive more than momentarily with a shorted output. It is encouraging to note that the output current will decrease at higher ambient temperatures. This assists in protecting the pass transistor from excessive heating.

16.5 FOLDBACK CURRENT LIMITING

With high-current regulators, the heat sink for the pass transistor must be made quite large in order to handle the power dissipated under worst-case conditions. Making it more than three times larger to withstand short circuits is sometimes inconvenient in the extreme. This problem can be solved with foldback current limiting, which makes the output current under overload conditions decrease below the full-load current as the output voltage is pulled down. The short-circuit current can be made but a fraction of the full load current.

A high current regulator using foldback limiting is shown in Figure 16.9. A second booster transistor, Q_1 has been added to provide a 2-A output current without causing excessive dissipation in the LM105. The resistor across its emitter-base junction bleeds off any collector-base leakage and establishes a minimum collector current for Q_2 to make sure that the circuit will not oscillate. The foldback characteristic is

produced with R_4 and R_5. The voltage across R_4 bucks out the voltage dropped across the current-sense resistor, R_3. Therefore, more voltage must be developed across R_3 before current limiting is initiated. After the output voltage begins to fall, the bucking voltage is reduced, as it is proportional to the output voltage. With the output shorted, the current is reduced to a value determined by the current-limit resistor and the current-limit sense voltage of the LM105.

Figure 16.10 illustrates the limiting characteristics. The circuit regulates for load currents up to 2 A. Heavier loads will cause the output voltage to drop, reducing the available current. With a short on the output, the current is only 0.5 A.

In design, the value of R_3 is determined from

$$R_3 = \frac{V_{lim}}{I_{SC}} \tag{16.1}$$

where V_{lim} is the current-limit sense voltage of the LM105, given in Figure 16.8, and I_{SC} is the design value of short circuit current. R_5 is then obtained from:

$$R_5 = \frac{V_{OUT} + V_{sense}}{I_{bleed} + I_{bias}} \tag{16.2}$$

where V_{OUT} is the regulated output voltage, V_{sense} is maximum voltage across the current-limit resistor for 0.1% regulation as indicated in Figure 16.7, I_{bleed} is the preload current on the regulator output and I_{bias} is the maximum current coming out of pin 1 of the LM105 under full load conditions. I_{bias} will be equal to 2 mA plus the worst-case base drive for the pnp booster transistor Q_2. I_{bleed} should be made at least ten times greater than I_{bias}.

Finally, R_4 is given by:

$$R_4 = \frac{I_{FL}R_3 - V_{sense}}{I_{bleed} + I_{bias}} \tag{16.3}$$

where I_{FL} is the output current of the regulator at full load.

It is recommended that a ferrite bead be strung on the emitter of the pass transistor, as shown in Figure 16.9, to suppress oscillations that may show up with certain physical configurations. It is advisable to also include C_4 across the current-limit resistor.

In some applications, the power dissipated in Q_2 becomes too great for a 2N2905 under worst-case conditions. This can be true even if a heat sink is used, as it should be in almost all applications. When dissipation is a problem, the 2N2905 can be replaced with a 2N3740. With a 2N3740, the ferrite bead and C_4 are not needed because this transistor has a lower cutoff frequency.

One of the advantages of foldback limiting is that it sharpens the limiting characteristics of the IC. In addition, the maximum output current is less sensitive to variations in the current-limit sense voltage of the IC: in this circuit, a 20% change in sense voltage will only affect the trip current by 5%. The temperature sensitivity of the full-load current is likewise reduced by a factor of four, while the short-circuit current is not.

Even though the voltage dropped across the sense resistor is larger with foldback limiting, the minimum input-output voltage differential of the complete regulator is

not increased above the 3 V specified for the LM105 as long as this drop is less than 2 V. This can be attributed to the low sense voltage of the IC by itself.

Figure 16.10 shows that foldback limiting can only be used with certain kinds of loads. When the load looks predominately like a current source, the load line can intersect the foldback characteristic at a point where it will prevent the regulator from coming up to voltage, even without an overload. Fortunately, most solid-state circuitry presents a load line which does not intersect. However, the possibility cannot be ignored, and the regulator must be designed with some knowledge of the load.

With foldback limiting, power dissipation in the pass transistor reaches a maximum at some point between full load and short circuited output. This is illustrated in Figure 16.11. However, if the maximum dissipation is calculated with the worst-case input voltage, as it should be, the power peak is not too high.

16.6 HIGH-CURRENT REGULATOR

The output current of a regulator using the LM105 as a control element can be increased to any desired level by adding more booster transistors, increasing the effective current gain of the pass transistors. A circuit for a 10-A regulator is shown in Figure 16.12. A third npn transistor has been included to get higher current. A low-frequency device is used for Q_3 because it seems to better withstand abuse. However, high-frequency transistors must be used to drive it. Q_2 and Q_3 are both double-diffused transistors with good frequency response. This ensures that Q_3 will present the dominant lag in the feedback loop through the booster transistors, and back around the output transistor of the LM105. This is further guaranteed by the addition of C_3.

The circuit, as shown, has a full-load capability of 10 A. Foldback limiting is used to give a short-circuit output current of 2.5 A. The addition of Q_3 increases the minimum input-output voltage differential by 1 V to 4 V.

16.7 DOMINANT FAILURE MECHANISMS

By far, the biggest reason for regulator failures is overdissipation in the series pass transistors. This has been borne out by experience with the LM100. Excessive heating in the pass transistors causes them to short out, destroying the IC. This has happened most frequently when pnp booster transistors in a TO-5 can, like the 2N2905, are used. Even with a good heat sink, these transistors cannot dissipate much more than 1 W. The maximum dissipation is less in many applications. When a single, pnp booster is used and power can be a problem, it is best to go to a transistor like the 2N3740, in a TO-66 power package, using a good heat sink.

Using a compound pnp / npn booster does not solve all problems. Even when breadboarding with transistors in TO-3 power packages, heat sinks must be used. The TO-3 package is not very good, thermally, without a heat sink. Dissipation in the pnp transistor driving the npn series pass transistor cannot be ignored either. Dissipation in the driver with worst-case current gain in the pass transistor must be taken into account. In certain cases, this could require that a pnp transistor in a power package be used to drive the npn pass transistor. In almost all cases, a heat sink is required if a pnp driver transistor in a TO-5 package is selected.

With output currents above 2 to 4 A, it is good practice to replace a 2N3055 pass transistor with a 2N3772. The 2N3055 is rated for higher currents, but its current gain falls off rapidly. This is especially true at either high temperatures or low input-output voltage differentials. A 2N3772 will give substantially better performance at high currents, and it makes like much easier for the pnp driver.

The second biggest cause of failure has been the output filter capacitors on power inverters providing unregulated power to the regulator. If these capacitors are operated near their maximum dc voltage rating with excessive ripple across them, they will sputter. That is, they short momentarily and clear themselves. When they short, the output capacitor of the regulator is discharged back through the reverse biased pass transistors or the control circuitry, frequently causing destruction. This phenomenon is especially prevalent when solid tantalam capacitors are used with high-frequency power inverters. The maximum ripple allowed on these capacitors decreases linearly with frequency.

The solution to this problem is to use capacitors with conservative voltage ratings. In addition, the maximum ripple allowed by the manufacturer at the operating frequency should also be observed. The problem can be eliminated completely by installing a diode between the input and output of the regulator such that the capacitor on the output is discharged through this diode when the input is shorted. A fast switching diode should be used as ordinary rectifier diodes are not always effective.

Another cause of problems with regulators is severe voltage transients on the unregulated input. Even if these transients do not cause immediate failure in the regulator, they can feed through and destroy the load. If the load shorts out, as is frequently the case, the regulator can be destroyed by subsequent transients.

This problem can be solved by specifying all parts of the regulator to withstand the transient conditions. However, when ultimate reliability is needed, this is not a good solution. Especially since the regulator can withstand the transient, yet severely overstress the circuitry on its output by feeding the transients through. Hence, a more logical recourse is to include circuitry which suppresses the transients. A method of doing this is shown in Figure 16.13. A zener diode, which can handle large peak currents, clamps the input voltage to the regulator while an inductor limits the current through the zener during the transient. The size of the inductor is determined from:

$$L = \frac{\Delta V \Delta t}{I} \tag{16.4}$$

where ΔV is the voltage by which the input transient exceeds the breakdown voltage of the diode, Δt is the duration of the transient and I is the peak current the zener can handle while still clamping the input voltage to the regulator. As shown, the suppression circuit will clamp 70 V, 4-ms transients on the unregulated supply.

16.8 CONCLUSIONS

The LM105 is an exact replacement for the LM100 in the majority of applications, providing about ten times better regulation. There are, however, a few differences:

In switching regulator applications (2), the size of the resistor used to provide positive feedback should be doubled as the impedance seen looking back into the

reference bypass terminal is twice that of the LM100 (2 kΩ versus 1 kΩ). In addition, the minimum output voltage of the LM105 is 4.5 V, compared with 2 V for the LM100. In low-voltage regulator applications, the effect of this is obvious. However, it also imposes some limitations on current regulator and shunt regulator designs (3). Lastly, clamping the compensation terminal (pin 7) within a diode drop of ground or the output terminal will not guarantee that the regulator is shut off, as it will with the LM100. This restricts the LM105 in the overload shutoff schemes (3) which can be used with the LM100.

Dissipation limitations of practical packages dictate that the output current of an IC regulator be less than 20 mA. However, external booster transistors can be added to get any output current desired. Even with satisfactory packages, considerably larger heat sinks would be needed if the pass transistors were put on the same chip as the reference and control circuitry, because an IC must be run at a lower maximum temperature than a power transistor. In addition, heat dissipated in the pass transistor couples into the low level circuitry and degrades performance. All this suggests that the pass transistor be kept separate from the IC.

Overstressing series pass transistors has been the biggest cause of failures with IC regulators. This not only applies to the transistors within the IC, but also to the external booster transistors. Hence, in designing a regulator, it is of utmost importance to determine the worst-case power dissipation in all the driver and pass transistors. Devices must then be selected which can handle the power. Further, adequate heat sinks must be provided as even power transistors cannot dissipate much power by themselves.

Normally, the highest power dissipation occurs when the output of the regulator is shorted. If this condition requires heat sinks which are so large as to be impractical, foldback current limiting can be used. With foldback limiting, the power dissipated under short-circuit conditions can actually be made less than the dissipation at full load.

The LM105 is designed primarily as a positive voltage regulator. A negative regulator, the LM104, which is a functional complement to the LM105 (4), has also been designed.

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3. Widlar, R. J., "New Uses for the LM100 Regulator," National Semiconductor AN-8, June, 1968.
4. Widlar, R. J., "Designs for Negative Voltage Regulators," National Semiconductor AN-21, October, 1968.

FIGURES

Figure 16.1. Comparison of load regulation of ICs without (LM100) and with added-gain stage (LM105) for equal short-circuit currents at (A) $T_j = 25^{\circ}C$ and (B) $T_j = 125^{\circ}C$.

Figure 16.2. Line regulation characteristics of the LM100 and LM105.

Figure 16.3. Circuit diagram of the LM100 voltage regulator.

Figure 16.4. Circuit diagram of the LM105 voltage regulator.

Figure 16.5. Dissipation-limited short-circuit output current for an IC regulator in a TO-5 package.

Figure 16.6. Voltage regulator with 0.2-A load current. Output voltage is determined by R_1 and R_2.

Figure 16.7. Maximum voltage drop across current-limit resistor at full load for worst-case load regulation of 0.1%.

Figure 16.8. Voltage drop across current-limit resistor required to initiate current limiting.

Figure 16.9. Foldback-current limiting included in 2-A voltage regulator.

Figure 16.10. Limiting characteristics of regulator with foldback current limiting.

Figure 16.11. Power dissipation in series pass transistors under overload conditions in regulator using foldback current limiting.

Figure 16.12. Ten-ampere regulator with foldback current limiting.

Figure 16.13. Suppression circuitry for removal of large voltage spikes from unregulated supplies.

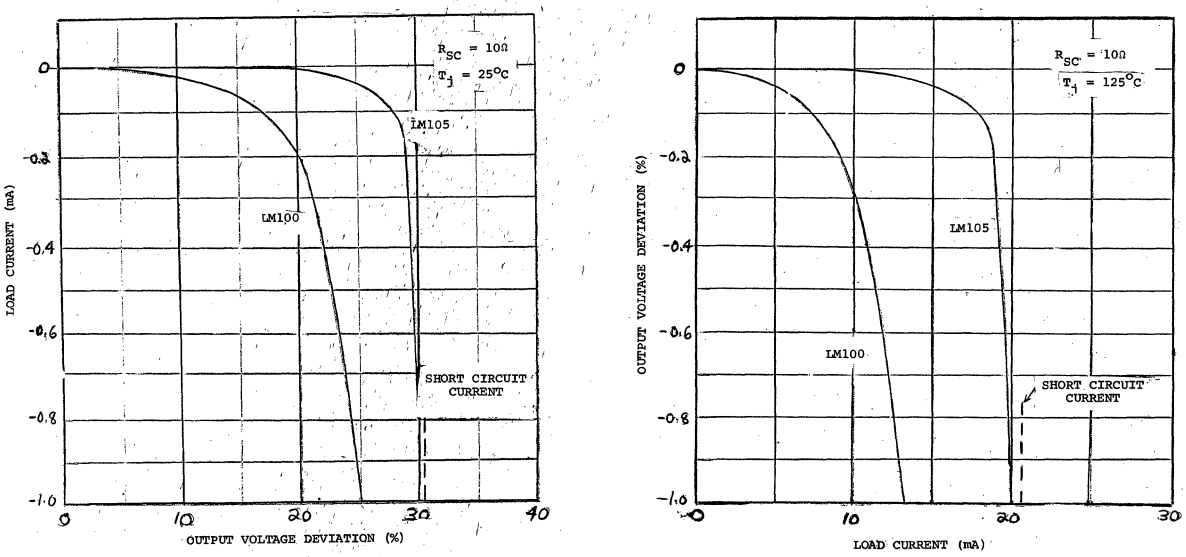


Figure 16.1. Comparison of load regulation of ICs without (LM100) and with added-gain stage (LM105) for equal short-circuit currents at (A) T_j = 25°C and (B) T_j = 125°C.

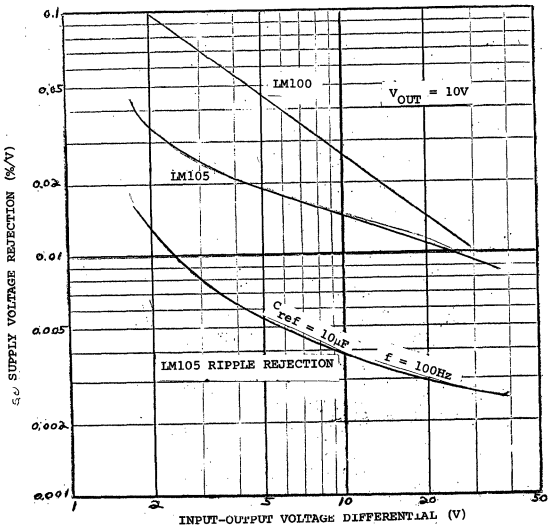


Figure 16.2. Line regulation characteristics of the LM100 and LM105.

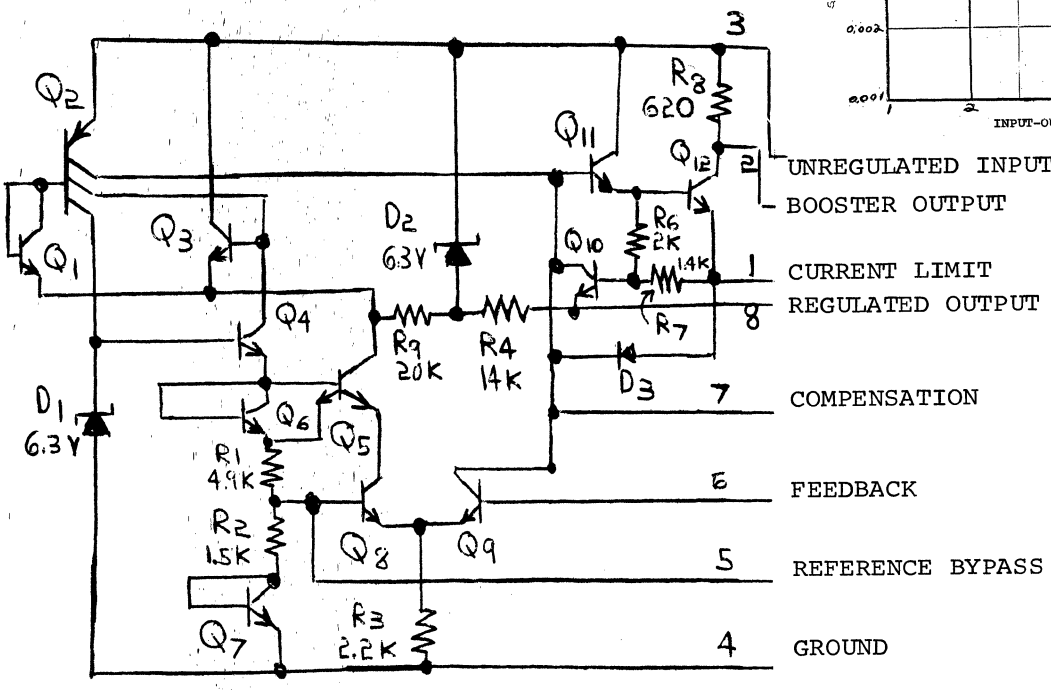


Figure 16.3. Circuit diagram of the LM100 voltage regulator.

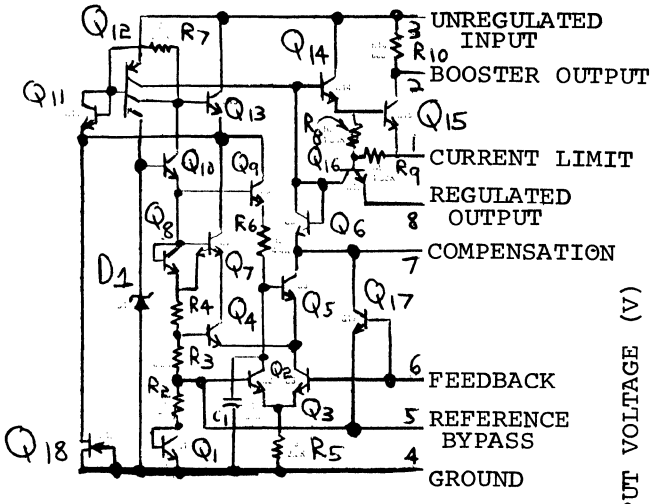


Figure 16.4. Circuit diagram of the LM105 voltage regulator.

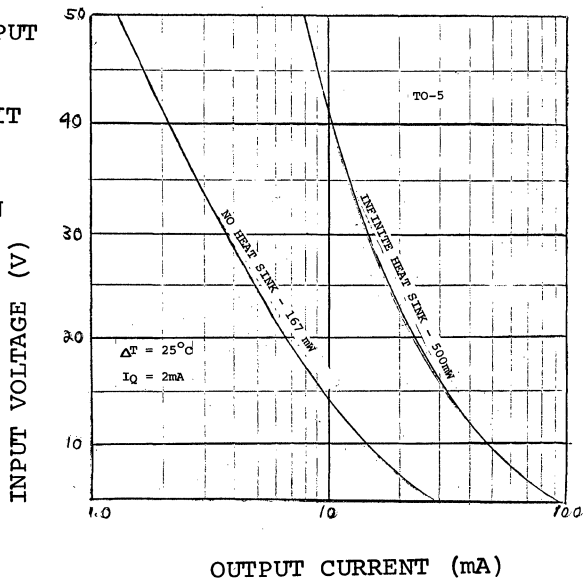


Figure 16.5. Dissipation-limited short-circuit output current for an IC regulator in a TO-5 package.

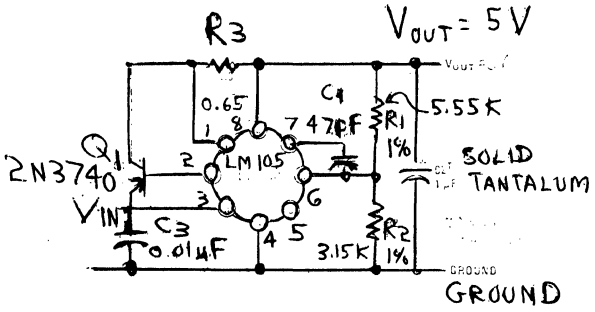


Figure 16.6 Voltage regulator with 0.2-A load current. Output voltage is determined by R_1 and R_2.

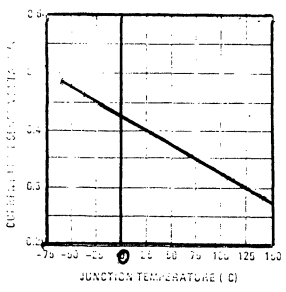


Figure 16.8. Voltage drop across current-limit resistor required to initiate current limiting.

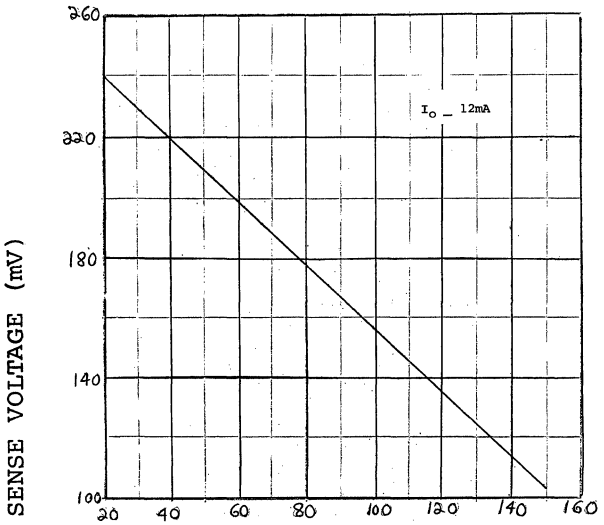


Figure 16.7. Maximum voltage drop across current-limit resistor at full load for worst-case load regulation of 0.1%.

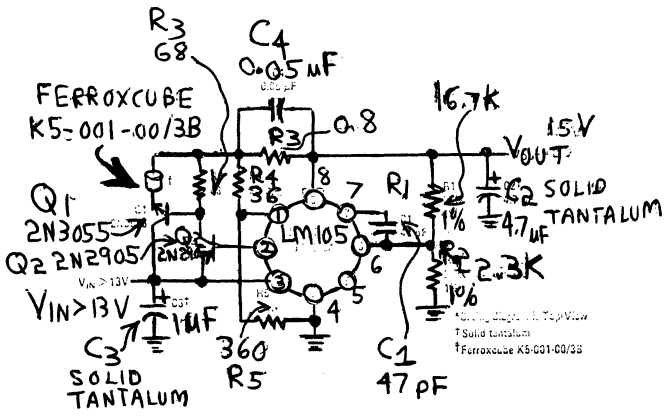


Figure 16.9. Foldback-current limiting included in 2-A voltage regulator.

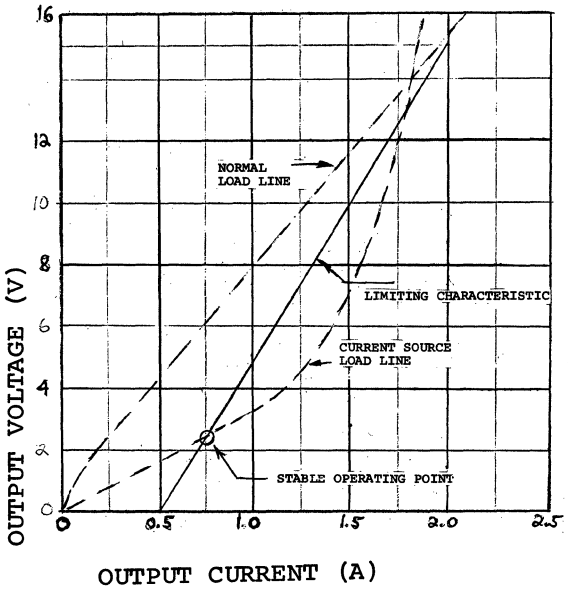


Figure 16.10. Limiting characteristics of regulator with foldback current limiting.

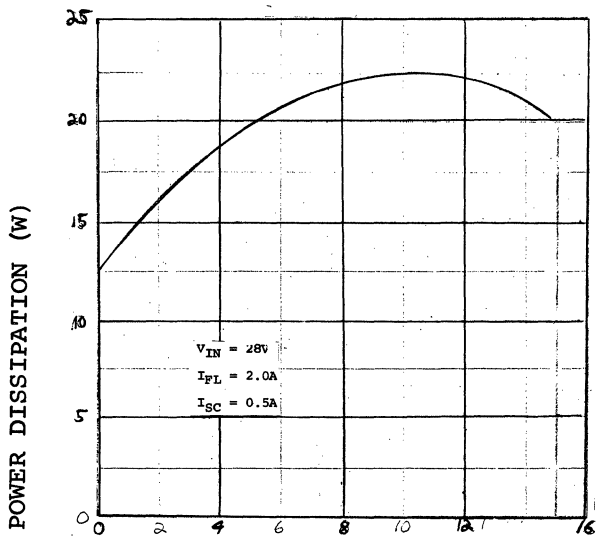


Figure 16.11. Power dissipation in series pass transistors under overload conditions in regulator using foldback current limiting.

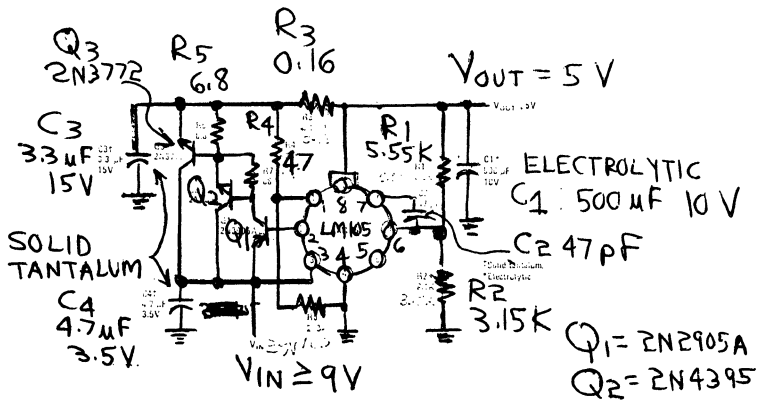


Figure 16.12. Ten-ampere regulator with foldback current limiting.

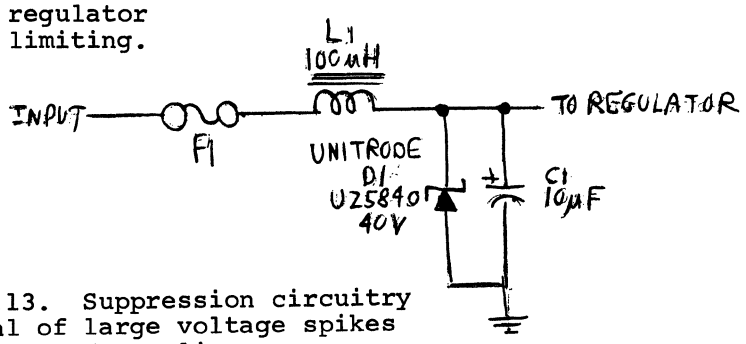


Figure 16.13. Suppression circuitry for removal of large voltage spikes from unregulated supplies.

17

Negative Voltage Regulators

by Robert J. Widlar
National Semiconductor

Although positive voltage regulators can be adapted for use in applications requiring negative voltage regulation, some sacrifice in complexity, performance and flexibility results. This can be avoided by using negative regulators as will be shown in this chapter.

17.1 THE NEGATIVE REGULATOR

The negative regulator used in the circuits described in this chapter is the LM104. This IC can supply any output voltage from 0 to 40 V while operating from a single unregulated supply. The output voltage is set by a single programming resistor and remote sensing at the load is possible. The IC regulates within 0.01% in circuits using a separate, floating bias supply, where the maximum output voltage is limited only by the breakdown of external pass transistors.

17.2 CIRCUIT OPERATION

The circuit diagram for the LM104 is shown in Figure 17.1.

The basic reference for the regulator is zener diode D_1. The reference diode is supplied from a pnp current source, Q_8, which has a fixed current gain of 2. This arrangement permits the circuit to operate with unregulated input voltages as low as 7 V, substantially increasing the efficiency of low-voltage regulators.

The reference supply is temperature compensated by using the negative temperature coefficient of the transistor emitter-base voltages to cancel the positive coefficient of the zener diode. The design produces a nominal 2.4 V between the reference and reference supply terminals of the integrated circuit. Connecting an external 2.4 kΩ resistor between those terminals gives a 1 mA reference current from the collectors of Q_1 and Q_2, which is independent of temperature. The reference voltage supplied to the error amplifier is developed across a second external resistor connected between the adjustment terminal and ground.

The reference supply terminal is normally connected to the unregulated supply. However, improved line regulation can be obtained by pre-regulating the voltage on this terminal. This improvement occurs because Q_1, Q_2, and Q_7 do not see changes in input voltage. Normally, it is the change in the emitter-base voltage of these transistors with changes in collector-base voltage which determines the line regulation.

When the reference supply and unregulated input terminals are operated from separate voltage sources, it is important to make sure that the un-regulated input terminal of the integrated circuit does not get more than 2 V more positive than the reference supply terminal. If this happens, the collector-isolation junction of Q_6 becomes forward biased and disrupts the reference.

The error amplifier of the regulator is quite similar to the LM101 operational amplifier. Emitter follower input transistors, Q_{18} and Q_{19}, drive a dual pnp which is operated in the common-base configuration. The current gain of these pnp transistors is fixed at 4 so that the base can be driven by a current source (Q_{13}). Active collector loads are used for the input stage so that a voltage gain of 2000 is obtained. Q21 and

Q_{22} provide enough current gain to keep the internal, series-pass transistor from loading the input stage. R_{14} limits the base drive on Q_{23} when it saturates with low, un-regulated input voltages. The collector of Q_{23} is brought out separately so that an external booster transistor can be added for increased output current capability. R_{13} establishs the minimum operating current in Q_{23} when booster transistors are used.

The error amplifier operates properly with common mode voltages all the way up to ground. Because of this, the circuit will regulate with output voltages to zero volts.

Current limiting is provided by Q_{24}. When the voltage between the current limit and unregulated input terminals becomes large enough to turn on Q_{24}, it will pull Q_{10} out of saturation and remove base drive from Q_{21} through Q_{20}. This causes the series pass transistor to exhibit a constant current characteristic. The pre-load current, provided for Q_{24} by Q_{10} before current limiting is initiated, gives a much sharper current-limit characteristic. C_1 and R_{11} are included in the limiting circuitry to suppress oscillations.

The error amplifier is connected to a divider on the output (R_{15} and R_{16}) to keep the reference current generator from saturating with low input-output voltage differentials. A compensating resistor, R_{17}, which is equal to the equivalent resistance of the divider is included to minimize offset error in the error amplifier.

The major feedback loop is frequency compensated by the brute-force method of rolling off the response with a relatively large capacitor on the output. C_2 is included on the integrated circuit to compensate for the effects of series resistance in the output capacitor. A compensation point is also brought out so that more capacitance can be added across C_2 for certain regulator configurations. R_8 improves the load-transient response, especially when compensation is added on pin 4.

The purpose of Q_9, which is a collector FET, is to bias the current-source transistors, Q_{12} and Q_{13}. It also supplies the preload current for the current-limit transistor, Q_{24}, through Q_{10}.

17.2 LOW-POWER REGULATOR

The circuit shown in Figure 17.2 can provide output voltages between OV and -40 V at currents up to 25 mA. The output voltage is linearly dependent on the value of R_2, giving approximately 2 V for each 1 kΩ of resistance. The exact scale factor can be set up by trimming R_1. This should be done at the maximum output voltage setting in order to compensate for any mismatch in the internal divider resistors of the integrated circuit.

Short-circuit protection is provided by R_3. The value of this resistor should be chosen so that the voltage drop across it is 300 mV at the maximum load current. This insures worst-case operation up to full load over a -55°C to 125°C temperature range. With a lower maximum operating temperature, the design value for this voltage can be increased linearly to 525 mV at 25°C.

For an output voltage setting of 15 V, the regulation, no load to full load, is better than 0.05%; and the line regulation is better than 0.2% for a ±20% input voltage variation. Noise and ripple can be greatly reduced by bypassing R_2 with a 10 μF capacitor. This will keep the ripple on the output less than 0.5 mV for a 1 V, 120 Hz ripple on the unregulated input. The capacitor also improves the line-transient response by a factor of five.

An output capacitor of at least 1 μF is required to keep the regulator from oscillating. This should be a low-inductance capacitor, preferably solid tantalum, installed with short leads. It is not usually necessary to bypass the input, but at least a 0.01 μF bypass is advisable when there are long leads connecting the circuit to the unregulated power source.

It is important to watch power dissipation in the integrated circuit even with load currents of 25 mA or less. The dissipation can be in excess of 1W with large input-output voltage differentials, and this is above ratings for the device.

17.3 INCREASED OUTPUT CURRENT

When output currents above 25 mA are required or when the dissipation in the series pass transistor can be higher than about 0.2 V, under worst-case conditions, it is advisable to add an external transistor to the LM104 to handle the power. The connection of an external booster transistor is shown here. The output current capability of the regulator is increased by the current gain of the added pnp transistor, but it is still necessary to watch dissipation in the external pass transistor. Excessive dissipation can burn out both the series pass transistor and the integrated circuit.

For example, with the circuit shown in Figure 17.3, the worst-case input voltage can be 25 V. With a shorted output at 125°C, the current through the pass transistor will be 300 mA; and the dissipation in it will be 7.5 W. This clearly establishes the need for an efficient heat sink.

For lower-power operation, a 2N2905 with a clip on heat sink can be used for the external pass transistor. However, when the worst-case dissipation is above 0.5 W, it is advisable to employ a power device such as the 2N3740 with a good heat sink.

The current limit resistor is chosen so that the voltage drop across it is 300 mV, with maximum load current, for operation to 125°C. With lower maximum ambients this voltage drop could be increased by 2.2 mV/°C. If possible, a fast-acting fuse rated about 25% higher than the maximum load current should be included in series with the unregulated input.

When a booster transistor is used, the minimum input-output voltage differential of the regulator will be increased by the emitter-base voltage of the added transistor. This establishes the minimum differential at 2 to 3V, depending on the base drive required by the external transistor.

When output currents in the ampere range are needed, it is necessary to add a second booster transistor to the LM104 circuitry. This connection is shown in Figure 17.4. The output current capability of the LM104 is increased by the product of the current gains of Q_1 and Q_2. However, it is still necessary to watch the dissipation in both the series pass transistor, Q_2, and its driver, Q_1. A clip-on heat sink is definitely required for Q_1, and it is advisable to replace the 2N2905 with a 2N3740 which has a good heat sink when output currents greater than 1 A are needed. A 1000-pF capacitor would also be added between pins 4 and 5 to compensate for the poorer frequency response of the 2N3740. The need for an efficient heat sink on Q_2 should be obvious.

Experience shows that a single-diffused transistor such as a 2N3055 (or a 2N3772 for higher currents) is preferred over a double diffused, high-frequency transistor for

the series pass element. The slower, single-diffused devices are less prone to secondary breakdown and oscillations in linear regulator applications.

As with the lower-current regulators, C_1 is required to frequency compensate the regulator and prevent oscillations. It is also advisable to bypass the input with C_2 if the regulator is located any distance from the output filter of the unregulated supply. The resistor across the emitter base junction of Q_2 fixes the minimum collector current of Q_1 to minimize oscillation problems with light loads. It is still possible to experience oscillations with certain physical layouts, but these can almost always be eliminated by stringing a ferrite bead, such as a Ferroxcube K5-001-00/3B, on the emitter lead of Q_2.

The use of two booster transistors does not appreciably increase the minimum input-output voltage differential over that for a single transistor. The minimum differential will be 2 to 3 V, depending on the drive current required from the integrated circuit.

With high current regulators, remote sensing is sometimes required to eliminate the effect of line resistance between the regulator and the load. This can be accomplished by returning R_2 and pin 9 of the LM104 to the ground end of the load and connecting pin 8 directly to the high end of the load.

The low resistance values required for the current limit resistor, R_3, are sometimes not readily available. A suitable resistor can be made using a piece of resistance wire or even a short length of kovar lead wire from a standard TO-5 transistor.

The current limit sense voltage can be reduced to about 400 mV by inserting a germanium diode (or a diode-connected germanium transistor) in series with pin 6 of the LM104. This diode will also compensate the sense voltage and make the short circuit current essentially independent of temperature.

With high current regulators it is especially important to use a low-inductance capacitor on the output. The lead length on this capacitor must also be made short. Otherwise, the capacitor leads can resonate with smaller bypass capacitors (like 0.1 μF ceramic) which may be connected to the output. These resonances can lead to oscillations. With short leads on the output capacitor, the Q of the tuned circuit can be made low enough so that it cannot cause trouble.

17.5 FOLDBACK CURRENT LIMITING

High current regulators dissipate a considerable amount of power in the series pass transistor under full-load conditions. When the output is shorted, this dissipation can easily increase by a factor of four. Hence, with normal current limiting, the heat sink must be designed to handle much more power than the worst case full load dissipation if the circuit is to survive short-circuit conditions. This can increase the bulk of the regulator substantially.

This situation can be eased considerably by using foldback current limiting, with this method of current limiting, the available output current actually decreases as the maximum load on the regulator is exceeded and the output voltage falls off. The short-circuit current can be adjusted to be a fraction of the full load current, minimizing dissipation in the pass transistor.

The circuit shown in Figure 17.5 accomplishes just this. Normally Q_3 is held in a

non-conducting state by the voltage developed across R_4. However, when the voltage across the current limit resistor, R_7 increases to where it equals the voltage across R_4 (about 1 V), Q_3 turns on and begins to rob base drive from the driver transistor, Q_1. This causes an increase in the output current of the LM104, and it will go into current limiting at a current determined by R_5. Since the base drive to Q_1 is clamped, the output voltage will drop with heavier loads. This reduces the voltage drop across R_4 and, therefore, the available output current. With the output completely shorted, the current will be about one-fifth the full-load current.

When designing, R_7 is chosen so that the voltage drop across it will be 1 to 2 V under full load conditions. The resistance of R_3 should be one-thousand times the output voltage. R_4 is then determined from

$$R_4 \cong \frac{R_7 R_3 I_{FL}}{V_{OUT} + 0.5} \tag{17.1}$$

where I_{FL} is the load current at which limiting will occur.

If it is desired to reduce the ratio of full-load to short-circuit current, this can be done by connecting a resistance of 2 to kΩ across the emitter-base of Q_3.

17.6 SYMMETRICAL POWER SUPPLIES

In many applications, such as powering operational amplifiers, there is a need for symmetrical positive and negative supply voltages. A circuit which is a particularly-economical solution to this design problem is shown in Figure 17.6. It uses a minimum number of components, and the voltage at both outputs can be set up with ±1.5% by a single adjustment. Further, the output voltages will tend to track with temperature and variations on the unregulated supply.

The positive voltage is regulated by an LM105, while an LM104 regulates the negative supply. The unusual feature is that the two regulators are interconnected by R_3. This not only eliminates one precision resistor, but the reference current of the LM104 stabilizes the LM105 so that a ±10% variation in its reference voltage is only seen as a ±3% change in output voltage. This means that in many cases the output voltage of both regulators can be set up with sufficient accuracy by trimming a single resistor, R_1.

The line regulation and temperature drift of the circuit is determined primarily by the LM104, so both output voltages will tend to track. Output ripple can be reduced by about a factor of five to less than 2 mV/V by bypassing pin 1 of the LM104 to ground with a 10 μF capacitor. A center-tapped transformer with a bridge rectifier can be used for the unregulated power source.

17.7 ADJUSTABLE CURRENT LIMITING

In laboratory power supplies, it is often necessary to adjust the limiting current of a regulator. This, of course, can be done by using a variable resistance for the current limit resistor. However, the current-limit resistor can easily have a value below that of commercially-available potentiometers. Discrete resistance values can be switched to vary the limiting current, but this does not provide continuously variable adjustment.

The circuit shown in Figure 17.7 solves this problem, giving a linear adjustment of limiting current over a five-to-one range. A silicon diode, D_1, is included to reduce

the current limit sense voltage to approximately 50 mV. Approximately 1.3 mA from the reference supply is passed through a potentiometer, R_4, to buck out the diode voltage. Therefore, the effective current limit sense voltage is nearly proportional to the resistance of R_4. The current through R4 is fairly insensitive to changes in ambient temperature, and D_1 compensates for temperature variations in the current limit sense voltage of the LM104. Therefore, the limiting current will not be greatly affected by temperature. It is important that a potentiometer be used for R_4 and connected as shown. If a rheostat connection were used, it could open while it was being adjusted and momentarily increase the current limit sense voltage to many times its normal value. This could destroy the series pass transistors under short-circuit conditions.

The inclusion of R_4 will soften the current limiting characteristics of the LM104 somewhat because it acts as an emitter-degeneration resistor for the current-limit transistor. This can be avoided by reducing the value of R_4 and developing the voltage across R_4 with additional bleed current to ground.

17.8 IMPROVING LINE REGULATION

The line regulation for voltage variations on the reference supply terminal of the LM104 is about five times worse than it is for changes on the unregulated input. Therefore, a zener-diode pre-regulator can be used on the reference supply to improve line regulation. This is shown in Figure 17.8.

The design of this circuit is fairly simple. It is only necessary that the minimum current through R_4 be greater than 2 mA with low input voltage. Further, the zener voltage of D_1 must be five volts greater than one-half the maximum output voltage to keep the transistors in the reference current source from saturating.

17.9 USING PROTECTIVE DIODES

It is a little known fact that most voltage regulators can be damaged by shorting out the unregulated input voltage while the circuit is operating even though the output may have short-circuit protection. When the input voltage to the regulator falls instantaneously to zero, the output capacitor is still charged to the nominal output voltage. This applies voltage of the wrong polarity across the series pass transistor and other parts of the regulator, and they try to discharge the output capacitor into the short. The resulting current surge can damage or destry these parts.

When the LM104 is used as the control element of the regulator, the discharge path is through internal junctions forward biased by the voltage reversal. If the charge on the output capacitor is in the order of 40 volt μF, the circuit can be damaged during the discharge interval. However, the problem is not only seen with integrated circuit regulators. It also happens with discrete regulators where the series-pass transistor usually gets blown out.

The problem can be eliminated by connecting a diode between the output and the input such that it discharges the output capacitor when the input is shorted. The diode should be capable of handling large current surges without excessive voltage drop, but it does not have to be a power diode since it does not carry current continuously. It should also be relatively fast. Ordinary rectifier diodes will not do because they look like an open circuit in the forward direction until minority carriers are injected into the intrinsic base region of the PIN structure.

This problem is not just caused by accidental physical shorts on the input. It has shown up more than once when regulators are driven from high-frequency dc-dc converters. Tantalum capacitors are frequently used as output filters for the rectifiers. When these capacitors are operated near their maximum voltage ratings with excessive high frequency ripple across them, they have a tendency to sputter-that is, short momentarily and clear themselves. When they short, they can blow out the regulator; but they look innocent after the smoke has cleared.

The solution to this problem is to use capacitors with conservative voltage ratings, to observe the maximum ripple ratings for the capacitor and to include a protective diode between the input and output of the regulator to protect it in case sputtering does occur.

Heavy loads operating from the unregulated supply can also destroy a voltage regulator. When the input power is switched off, the input voltage can drop faster than the output voltage, causing a voltage reversal across the regulator, especially when the output of the regulator is lightly loaded. Inductive loads such as a solenoid are particularly troublesome in this respect. In addition to causing a voltage reversal between the input and the output, they can reverse the input voltage causing additional damage.

In cases like this, it is advisable to use a multiple-pole switch or relay to disconnect the regulator from the unregulated supply separate from the other loads. If this cannot be done, it is necessary to put a diode across the input of the regulator to clamp any reverse voltages, in addition to the protective diode between the input and the output.

Yet another failure mode can occur if the regulated supply drives inductive loads. When power is shut off, the inductive current can reverse the output voltage polarity, damaging the regulator and the output capacitor. This can be cured with a clamp diode on the output. Even without inductive loads it is usually good practice to include this clamp diode to protect the regulator if its output is accidentally shorted to a negative supply.

A regulator with all these protective diodes is shown in Figure 17.9. D_1 protects against output voltage reversal. D_2 prevents a voltage reversal between the input and the output of the regulator. And D_3 prevents a reversal of the input-voltage polarity. In many cases, D_3 is not needed if D_1 and D_2 are used, since these diodes will clamp the input voltage within two diode drops of ground. This is adequate if the input voltage reversals are of short duration.

17.10 HIGH VOLTAGE REGULATOR

In the design of commercial power supplies, it is common practice to use a floating bias supply to power the control circuitry of the regulator. As shown in Figure 17.10, this connection can be used with the LM104 to regulate output voltages that are higher than the ratings of the integrated circuit. Better regulation can also be obtained because it is a simple matter to preregulate the low current bias supply so that the integrated circuit does not see ripple or line voltage variations and because the reduced operating voltage minimizes power dissipation and associated thermal effects from the current delivered to the booster transistor.

The bias for the LM104, which is normally obtained from a separate winding on the main power transformer, is preregulated by D_1. R_4 is selected so that it can provide the 3 mA operating current for the integrated circuit as well as the base drive of the booster transistor, Q_1, with full load and minimum line voltage. The booster transistor regulated the voltage from the main supply, and its breakdown voltage will determine the maximum operating voltage of the complete regulator.

The connection of the LM104 is somewhat different than usual: the internal divider for the error amplifier is shorted out by connecting pins 8 and 9 together. This makes the output voltage equal to the voltage drop across the adjustment resistor, R_2, instead of twice this voltage as is normally the case. C_2 and C_3 must also be added to prevent oscillation. The value of C_3 can be increased to 4.7 μF to reduce noise on the output.

It is necessary to add Q_2 and R_5 to provide current limiting. When the output current becomes high enough to turn on Q_2, there will be an abrupt rise in the output current of the LM104 as Q_2 tries to remove base drive from the booster transistor. Any further increases in load current will cause the LM104 to limit at a current determined by R_3, and the output voltage will collapse. The value of R_3 must be selected so that the integrated circuit can deliver the base current of Q_1, at full load, without limiting.

A second, npn booster transistor can be used in a compound connection with Q_1 to increase the output current of the regulator. However, with very-high-voltage regulators, the most economical solution may be to use a high voltage pnp driving a vacuum tube for the series pass element.

Remote sensing, which eliminates the effects of voltage dropped in the leads connecting the regulator to the load, can be provided by connecting R_2 to the ground end of the load and pins 8 and 9 to the high end of the load.

17.11 SWITCHING REGULATOR

Linear regulators have the advantages of fast response to load transients as well as low noise and ripple. However, since they must dissipate the difference between the unregulated-supply power and the output power, they sometimes have a low efficiency. This is not always a problem with ac line-operated equipment because the power loss is easily afforded, because the input voltage is already fairly-well regulated and because losses can be minimized by adjustment of transformer ratios in the power supply. In systems operating from a fixed dc input voltage, the situation is often much different. It might be necessary to regulate a 28 V input voltage down to 5 V. In this case, the power loss can quickly become excessive. This is true even if efficiency is not one of the more important criteria, since high power dissipation calls for expensive power transistors and elaborate heat sinking methods.

Switching regulators can be used to greatly reduce dissipation. Efficiencies approaching 90% can be realized even though the regulated output voltage is only a fraction of the input voltage. With proper design, transient response and ripple can also be made quite acceptable.

The circuit shown in Figure 17.11 uses the LM104 as a self-oscillating switching regulator and operates in much the same way as a linear regulator. The reference current is set up at 1 mA with R_1, and R_2 determines the output voltage in the normal fashion. The circuit is made to oscillate by applying positive feedback through R_5 to the non-inverting input on the error amplifier of the LM104. When the output voltage is low, the internal pass transistor of the integrated circuit turns on and drives Q_1 into saturation. The current feedback through R_5 then increases the magnitude of the reference voltage developed across R_2. Q_1 will remain on until the output voltage comes up to twice this reference voltage. At this point, the error amplifier goes into linear operation, and the positive feedback makes the circuit switch off. When this happens, the reference voltage is lowered by feedback through R_5, and the circuit will stay off until the output voltage drops to where the error amplifier again goes into linear operation. Hence, the circuit regulates with the output voltage oscillating about the nominal value with a peak-to-peak ripple of around 40 mV.

The power conversion from the input voltage to a lower output voltage is obtained by the action of the switch transistor, Q_1, the catch diode, D_1, and the LC filter. The inductor is made large enough so that the current through it is essentially constant throughout the switching cycle. When Q_1 turns on, the voltage on its collector will be nearly equal to the unregulated input voltage. When it turns off, the magnetic field in L_1 begins to collapse, driving the collector voltage of Q_1 to ground where it is clamped by D_1.

If, for example, the input voltage is 10 V and the switch transistor is driven at a 50% duty cycle, the average voltage on the collector of Q_1 will be 5 V. This waveform will be filtered by L_1 and C_1 and appear as a 5 V dc voltage on the output. Since the inductor current comes from the input while Q_1 is on but from ground through D_1 while Q_1 is off, the average value of the input current will be half the output current. The power output will therefore equal the input power if switching losses are neglected.

In design, the value of R_3 is chosen to provide sufficient base drive to Q_1 at the maximum load current. R_4 must be low enough so that the bias current coming out of pin 5 of the LM104 (approximately 300 μA) does not turn on the switch transistor. The purpose of C_2 is to remove transients that can appear across R_2 and cause erratic switching. It should not be made so large that it severely integrates the waveform fed back to this point.

17.12 HIGH CURRENT SWITCHING REGULATOR

Output currents up to 3 A can be obtained using the switching regulator circuit shown in Figure 17.12. The circuit is identical to the one described previously, except that Q_2 has been added to increase the output current capability by about an order of magnitude. It should be noted that the reference supply terminal is returned to the base of Q_2, rather than the unregulated input. This is done because the LM104 will not function properly if pin 5 gets more than 2V more positive than pin 3. The reference current, as well as the biase currents for pins 3 and 5, is supplied from the unregulated input through R_5, so its resistance must be low enough so that Q_2 is not turned on with about 2 mA flowing through it.

The line regulation of this circuit is worsened somewhat by the unregulated input voltage being fed back into the reference for the regulator through R_6. This effect can be eliminated by connecting a 0.01 μF capacitor in series with R_6 to remove the dc component of the feedback.

There are a number of precautions that should be observed with all switching regulators, although they are more inclined to cause problems in high-current applications:

For one, fast switching diodes and transistors must be used. if D_1 is an ordinary junction rectifier, voltages in the order of 10 V can be developed across it in the forward direction when the switch transistor turns off. This happens because low-frequency rectifiers are usually manufactured with a pin strucuture which presents a high forward impedance until enough minority carriers are injected into the diode base region to increase its conductance. This not only causes excessive dissipation in the diode, but the diode also presents a short circuit to the switch transistor, when it first turns on, until all the charge stored in the base region of the diode is removed. Similarly, a high-frequency switch transistor must be used as excessive switching losses in low-frequency transistors, like the 2N3055, make them overheat.

It is important that the core material used for the inductor have a soft saturation characteristic. Cores that saturate abruptly produce excessive peak currents in the switch transistor if the output current becomes high enough to run the core close to saturation. Powdered molybdenum-permalloy cores, on the other hand, exhibit a gradual reduction in permeability with excessive current, so the only effect of output currents above the design value is a gradual increase in switching frequency.

One thing that is frequently overlooked in the design of switching circuits is the ripple rating of the filter capacitors. Excessive high-frequency ripple can cuase these capacitors to fail. This is an especially-important consideration for capacitors used on the unregulated input as the ripple current through them can be higher than the dc load current. The situation is eased somewhat for the filter capacitor on the output of the regulator since the ripple current is only a fraction of the load current. Nonetheless, proper design usually requires that the voltage rating of this capacitor be higher than that dictated by the dc voltage across it for reliable operation.

One unusual problem that has been noted in working with switching regulators is excessive dissipation in the switch transistors caused by high emitter-base saturation voltage. This can also show up as erratic operation if Q_1 is the defective device. This saturation voltage can be as high as 5 V and is the result of poor alloying on the base contact of the transistor. A defective transistor will not usually show up on a curve tracer because the low base current needed for linear operation does not produce a large voltage drop across the poorly-alloyed contact. However, a bad device can be spotted by probing on the bases of the switch transistors while the circuit is operating.

It is necessary that the catch diode, D_1, and any bypass capacitance on the unregulated input be returned to ground separately from the other parts of the circuit. These components carry large current transients and can develop appreciable voltage transients across even a short length of wire. If C_1, C_2, or R_2 have any common ground impedance with the catch diode or the input bypass capacitor, the transients can appear directly on the output.

17.13 SWITCHING REGULATOR WITH CURRENT LIMITING

The switching regulator circuits described previously are not protected from overloads or a short-circuited output. The current limiting of the LM104 is used to limit the base drive of the switch transistor, but this does not effectively protect the switch transistor from excessive current. Providing short-circuit protection is no simple problem, since it is necessary to keep the regulator operating in the switching mode when the output is shorted. Otherwise, the dissipation in the switch transistor will become excessive even though the current is limited.

A circuit which provides current limiting and protects the regulator from short circuits is shown in Figure 17.13. The current through the switch transistor produces a voltage drop across R_9. When this voltage becomes large enough to turn on Q_3, current limiting is initiated. This occurs because Q_3 takes over as the control transistor and regulates the voltage on pin 8 of the LM104. This point, which is the feedback terminal of the error amplifier, is separated from the actual output of the regulator by not shorting the regulated output and booster output terminals of the integrated circuit. Hence, with excessive output current, the circuit still operaates as a switching regulator with Q_3 regulating the voltage fed back to the error amplifier as the output voltage falls off.

A resistor, R_7, is included so that excessive base current will not be driven into the base of Q_3. C_4 insures that Q_3 does not turn on from the current spikes through the switch transistor caused by pulling the stored charge out of the catch diode (these are about twice the load current). This capacitor also operates in conjunction with C_2 to produce sufficient phase delay in the feedback loop so that the circuit will oscillate in current limiting. However, C_4 should not be made so large that it appreciably integrates the rectangular wave-form of the current through the switch transistor.

As the output voltage falls below half the design value, D_1 pulls down the reference voltage across R_2. This permits the current limiting circuitry to keep operating when the unregulated input voltage drops below the design value of output voltage, with a short on the output of the regulator.

A transistor with good high-current capability was chosen for Q_3 so that it does not suffer from secondary breakdown effects from the large peak currents (about 200 mA) through it. With a shorted output, these peak currents occur with the full input voltage across Q_3. The average dissipation in Q_3 is, however, low.

17.14 SWITCHING REGULATOR WITH OVERLOAD SHUTOFF

An alternate method for protecting a switching regulator from excessive output currents is shown in Figure 17.14. When the output current becomes too high, the voltage drop across the current-sense resistor, R_8, fires an SCR which shuts off the regulator. The regulator remains off, dissipating practically no power, until it is reset by removing the input voltage.

In the actual circuit, complementary transistors, Q_3 and Q_4, replace the SCR since it is difficult to find devices with a low enough holding current (about 25 μA). When the voltage drop across R_8 becomes large enough to turn on Q_4, this removes the base drive

for the output transistors of the LM104 through pin 4. When this happens Q_3 latches Q_4, holding the regulator off until the input voltage is removed. It will then start when power is applied if the overload has been removed.

With this circuit, it is necessary that the shutoff current be 1.5 times the full-load current. Otherwise, the circuit will shut off when it is switched on with a full load because of the excess current required to charge the output capacitor. The shut-off current can be made closer to the full-load current by connecting a 10-μF capacitor across R_2 which will limit the charging current for C_1 by slowing the rise time of the output voltage when the circuit is turned on. However, this capacitor will also bypass the positive feedback from R_6 which makes the regulator oscillate. Therefore, it is necessary to put a 270-Ω resistor in the ground end of the added capacitor and provide feedback to this resistor from the collector of Q_1 through a 1-MΩ resistor.

17.15 DRIVEN SWITCHING REGULATOR

When a number of switching regulators are operated from a common power source, it is desirable to synchronize their operation to more uniformly distribute the switched current waveforms in the input line. Synchronous operation can also be beneficial when a switching regulator is operated in conjunction with a power converter.

A circuit which synchronizes the switching regulator with a square-wave drive signal is shown in Figure 17.15. It differs from the switching regulators described previously in that positive feedback is not used. Instead, a triangular wave with a peak-to-peak amplitude of 25 mV is applied to the noninverting input of the error amplifier. The waveform is obtained by integrating the square-wave synchronizing signal. This triangular wave causes the error amplifier to switch because its gain is high enough that the waveform easily overdrives it. The switching duty cycle is controlled by the output voltage fed back to the error amplifier. If the output voltage goes up, the duty cycle will decrease since the error amplifier will pick off a smaller portion of the triangular wave. Similarly, the duty cycle will decrease if the output voltage drops. Hence, the duty cycle is controlled to produce the desired output voltage.

Without a synchronous drive signal, the circuit will self oscillate at a frequency determined by L_1 and C_1. This self-oscillation frequency must be lower than the synchronous drive frequency. Therefore, more filtering is required for a driven regulator than for a self-oscillating regulator operating at the same frequency. This also means that a driven regulator will have less output ripple.

The value of C_2 is chosen so that its capacitive reactance at the drive frequency is less than one-tenth the resistance of R_2. The amplitude of the triangular wave is set at 25 mV with R_5. It is advisable to ac couple the drive signal by putting a capacitor in series with R_5 so that it does not disturb the dc reference voltage developed for the error amplifier.

FIGURES

Figure 17.1. Circuit diagram for negative voltage regulator LM104.

Figure 17.2. Low-power voltage regulator can supply outputs of 0 to 40 V at current levels up to 25 mA.

Figure 17.3. Negative voltage regulator with external booster transistor.

Figure 17.4. Use of voltage regulator with two booster transistors.

Figure 17.5. Circuit with foldback limiting.

Figure 17.6. Symmetrial power supply. Positive voltage is regulated by LM105; negative voltage regulation is handled by LM104.

Figure 17.7. Circuit with adjustable current limiting.

Figure 17.8. Use of a zener diode to improve line regulation.

Figure 17.9. Regulator with protective diodes.

Figure 17.10. High-voltage regulator has floating bias supply.

Figure 17.11. Switching regulator circuit.

Figure 17.12. Switching regulator capable of handling output currents to 3 A.

Figure 17.13. Switching regulator with current limiting.

Figure 17.14. Switching regulator with overload shutoff.

Figure 17.15. Switching regulator with square-wave drive signal.

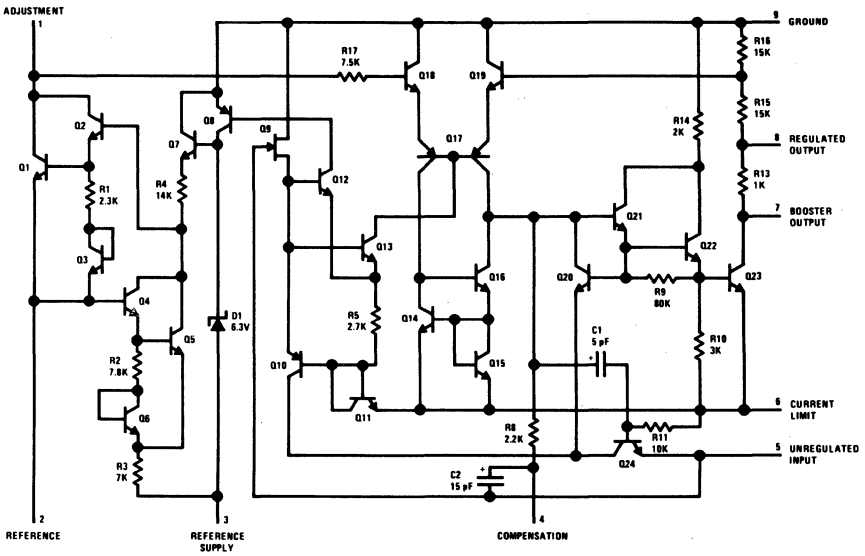


Figure 17.1. Circuit diagram for negative voltage regulator LM104.

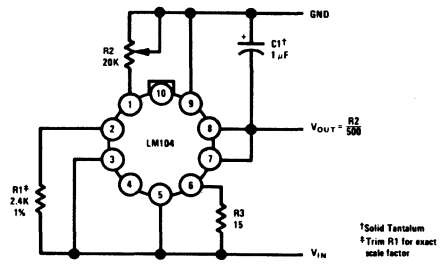


Figure 17.2. Low-power voltage regulator can supply outputs of 0 to 40 V at current levels up to 25 mA.

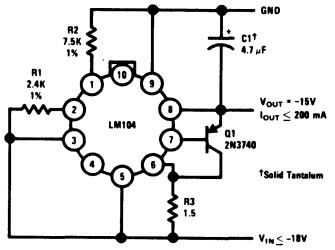


Figure 17.3. Negative voltage regulator with external booster transister.

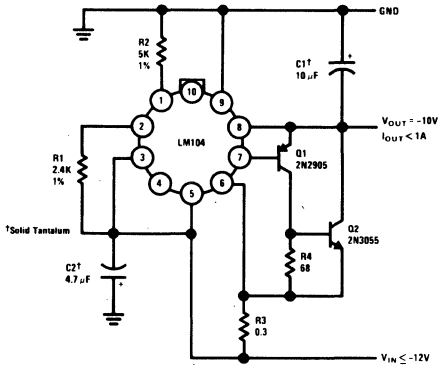


Figure 17.4. Use of voltage regulator with two booster transistors.

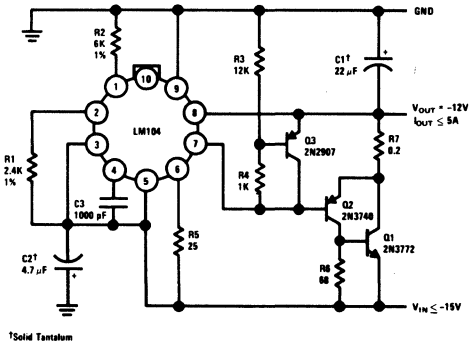


Figure 17.5. Circuit with foldback limiting.

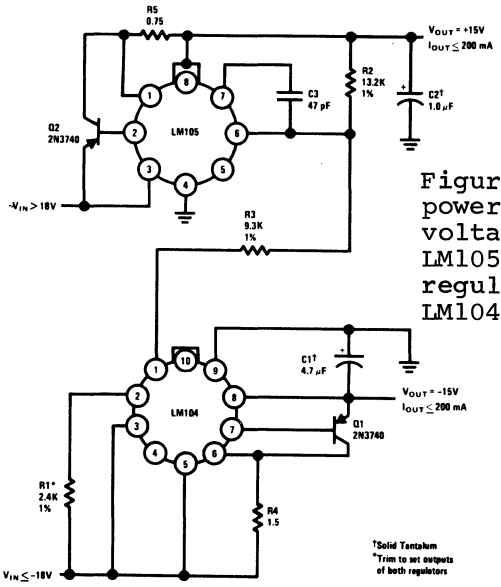


Figure 17.6. Symmetrial power supply. Positive voltage is regulated by LM105; negative voltage regulation is handled by LM104.

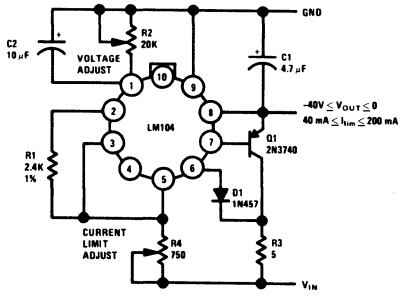


Figure 17.7. Circuit with adjustable current limiting.

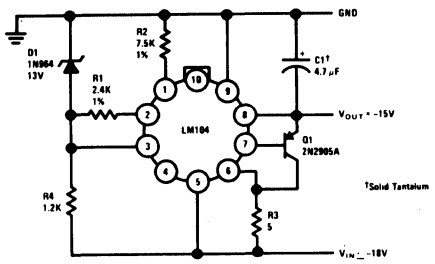


Figure 17.8. Use of a zener diode to improve line regulation.

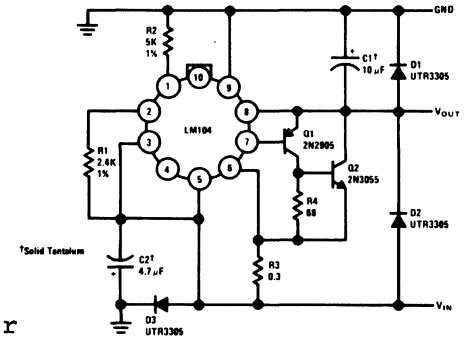


Figure 17.9. Regulator with protective diodes.

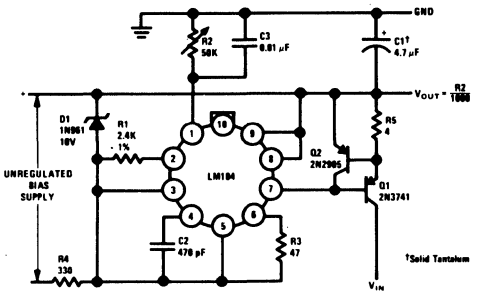


Figure 17.10. High-voltage regulator has floating bias supply.

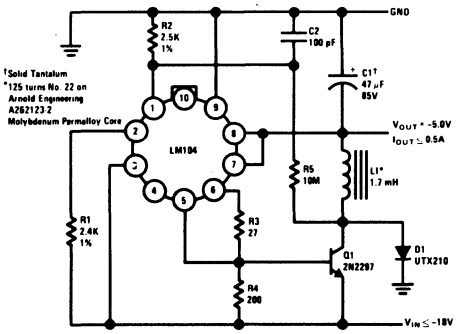


Figure 17.11. Switching regulator circuit.

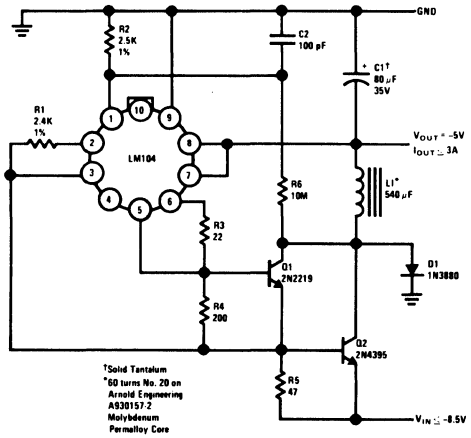


Figure 17.12. Switching regulator capable of handling output currents to 3 A.

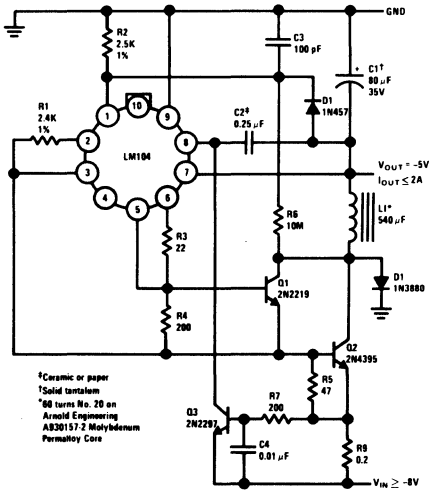


Figure 17.13. Switching regulator with current limiting.

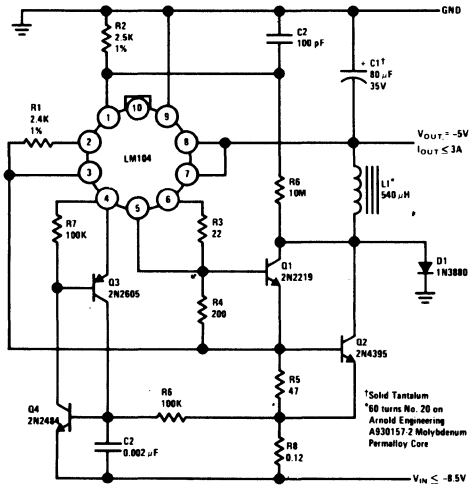


Figure 17.14. Switching regulator with overload shutoff.

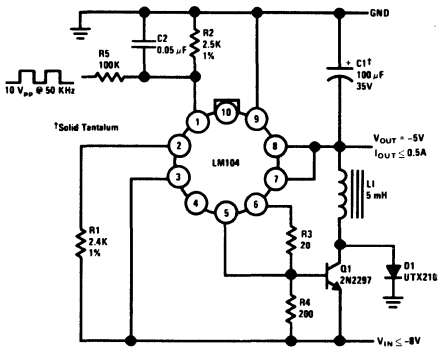


Figure 17.15. Switching regulator with square-wave drive signal.

18

A High-Speed Data-Transmission System

by Jerry Avery
Texas Instruments

Digital systems often require the use of long lines for the transmission of digital information between various equipment locations within the system. These long lines are frequently located in noisy environments which can cause propagation of false information if steps are not taken to overcome the noise and its effects on data transmission. In the past this problem has been overcome by using special line drivers and/or line receivers to interface between the transmission line and the logic circuitry (See Figure 18.1).

Line-driver circuits translate the small logic level swings of the processing and peripheral portions of the computer to either higher voltage levels or matched impedance (current mode) levels for transmission to other areas of the computer. Balanced lines may be used to help overcome noise problems; line receivers must reject the common mode and induced noise on the transmission lines and convert the signals back to forms which are compatible with the standard logic circuits of the computer.

The following paragraphs will cover the use of a compatible line driver and line receiver to overcome noise problems in a high-speed data-transmission system.

18.1 LINE DRIVER CHARACTERISTICS

Input characteristics. The input of the driver is TTL compatible with two inputs per driver. The inputs are designated A_1-A_2 and B_1-B_2. The switching point is between 0.4 V and 2.4 V and typically at 1.4 V.

Input requirements. V_{in} (1) is the logical "1"-input voltage required at an input terminal to insure a logical "1" at the in phase output terminal is typically 1.4 V.

Typical input dc noise immunity. The input gates of the driver will change states at 1.4 V. The output from a TTL gate is typically 3.3 V in the logical "1" state and 0.2 V in the logical "0" state. Therefore the driver can typically tolerate 1.9 V of negative-going noise in the "1" state and 1.2 V of positive going noise in the "0" state before causing the input gate to false trigger.

Guaranteed input dc noise immunity. Simply stating that a circuit will not false trigger is no adequate guarantee for a design engineer. The IC manufacturer must also guarantee voltage levels which allow a specific noise margin. The logic "0" input test voltage to the driver is 0.8 V; with a guaranteed maximum logical "0" output of 0.4 V for the TTL circuits, the guaranteed noise margin of 400 mV.

Output characteristics. The output is a differential amplifier capable of driving single ended or balanced. It has a high common-mode output voltage range of +10 V, -3 V. The large drive range not only allows the gate to drive long lines, but also gives it better noise margins at the receiver.

The differential output also allows the signal to be transmitted on a balanced line, so that common-noise signals induced on the two conductors of the transmission line are ignored at the receiver.

18.2 DRIVER CIRCUIT DESCRIPTION

The SN75109 is a high-speed data transmitter designed to be used in applications such as line drivers in balanced or unbalanced applications, party line systems, and level converters.

This monolithic dual line driver has two independent channels and common supply voltage and ground. Each line driver consists of a TTL-compatible input stage followed by a level shifter and a differential pair providing a current-mode output signal.

An inhibitor input gate (TTL compatible) provided to each output stage may be used to turn off either output stage, regardless of the input signal applied. A common strobe (inhibitor input) is also available for inhibiting both channels (See Figure 18.2).

Input stage. The multiple-emitter transistor Q_1 is used to provide inherent switching-time advantages over other saturated logic schemes.

A low voltage at the inputs A or B will allow current to flow through the base-emitter diode of Q_1 which is in saturation (See Figure 18.8). No drive current will pass through the base collector junction until the voltage at the base of Q_2 exceeds the forward voltages across diodes D_2 and D_3 ($V_{FD2} + V_{FD3}$), for the differential stage Q_2-Q_3 operates basically as a switch. The voltage (V_C) at the base of Q_2 (point C) equals:

$$V_{IN} + V_{OFFSET\ Q_1} \tag{18.1}$$

where $V_{OFFSET} = V_{CE}$

The input D at the base of Q_3 is referenced at 2 Vbe above ground by using the forward drop across the two diodes D_2 and D_3. Therefore, when V_D is greater than V_C, Q_3 is ON and Q_2 is OFF, leading to:

$$V_E = V_{CC1} - (R_2 + R_4)\ (I_S + I_B) \tag{18.2}$$

$$V_F = V_{CC1} - R_2 I_S - (R_2 + R_3)\ I_B \tag{18.3}$$

where I_S is the current provided by the current source (Q_4, D_1, and R_6) and I_B is the current flowing into the next stage. The value of I_s can be obtained from:

$$I_S = \frac{V_{CC1} - V_{FD1}}{R_6} = 1.4\ \text{mA (typical)} \tag{18.4}$$

The reverse situation occurs when V_C is greater than V_D. A clamp voltage at point C is provided through diodes D_2, D_3, D_4 and the offset voltage V_{CE} of Q. This voltage is given by:

$$VC_{clamp} = V_{FD2} + V_{FD3} + V_{FD4} + V_{OFFSET\ Q_1} \tag{18.5}$$

If inputs A and B are raised to a voltage above the clamp level the current flowing through the base-emitter junction of Q_1 (or Q_2) will decrease until these emitters are finally reverse biased. However, transistor Q_1 will not be turned off as in a standard gate, but will remain in the saturation region since the clamping emitter tied between R_5 and D_4 is now forward biased.

Threshold-noise margin. As expected from the preceding analysis, the driver input has an input logic threshold voltage level of approximately 2 V_{BE}.

Besides the logic threshold, the same noise margins guaranteed for Series 54 are assured at each of the driver inputs. This is accomplished by testing each logic input under standard Series 54 conditions, at 2 V in the logical "1"-input condition and 0.8 V in the logical "0"-input condition. An absolute minimum of 0.4 V of noise margin is therefore guaranteed at each input, since the specified driving logic is 2.4 V minimum with a logical "1" input and 0.4 V maximum with a logical "0" input under worst-case conditions.

Input current requirements. Input current requirements reflect worst-case conditions for $T_A = -55^oC$ to 125^oC and a ΔV_{CC} of ± 10 percent. The Q_1 base-emitter saturation during a logical "0"-input level will require no more than 3.0 mA flowing out of the emitter. Each input requires some current into it at a logical "1" level. This current is 40 μA maximum for each emitter input.

Level shifting stage (See Figure 18.4). The voltage levels computed at the points E and F in the preceding section are shifted down through Q_9 and Z_1 and Q_{10} and Z_2 to points G and H.

Q9 and Q_{10}, Z_1 and Z_2, and R_7 and R_8 are carefully matched to provide points G and H with a nominally 1-V differential.

Output stage (See Figure 18.5). The differential voltage at inputs G and H is large enough to switch completely the differential pair Q_{13} and Q_{14}. Therefore, when V_G is greater than V_H, Q_{13} is on and Q_{14} is off. Q_{13} will then sink the amount of current I_S supplied by the current source constituted by Q_{15} - Q_{16} - Q_{17} - Q_{18} - Q_{19} and R_9. It operates as explained in the following paragraphs.

The point I is 2 V_{be} above V_{CC2}, forcing a current Io through R_9 which is equal to:

$$Io = \frac{V_{CC2} - 2\,V_{be}}{R_9} \qquad (18.6)$$

This current will supply the base drive for Q_{15} - Q_{16} - Q_{17} - Q_{19} as well as the collector current for Q_{19} ($Io-4I_B$). Close matching of these four transistors will lead to a total I_S (sink current) of approximately 3 I_o.

This strucuture saves about one-third of the power required by a standard current source using only one diode and one transistor. Furthermore, 2 V_{be} drops are required at point I for proper operation. This advantage will be demonstrated.

Inhibitor stage. As previously stated, this stage has been designed to enable or inhibit the driver function.

Enabling. Here also the multiple-emitter input transistor has been chosen for the reasons stated in the description of the input operation. When the strobe inputs are raised to a high voltage the transistor Q_{25} is turned off and the Q_{23} base drive current is supplied through the base-collector diode of Q_{25}. Q_{23} will saturate, and the current flowing through R_{12} and R_{13} will lower the voltage at point L.

This voltage will then be shifted through the zener diode Z_3, and finally the voltage V_o at the base of Q_{21} will be:

$$V_o = \frac{\frac{R_{13}}{R_{12}} V_{CC1} + \left(1 + \frac{R_{13}}{R_{12}}\right) V_{CC2} - \left(1 + \frac{R_{13}}{R_{12}}\right) V_{23} + V_{CE(SAT)} + V_{BE}}{1 + \frac{R_{13}}{R_{12}} + \frac{R_{13}}{R_{11}}} \quad (18.7)$$

where V_{CE} (SAT) and V_{BE} are measured at Q_{23} and Q_{24} respectively. This voltage V_o will be low enough to turn off transistors Q_{21} and Q_{20} and therefore the driver output current will not be affected. Obviously worst-case conditions are reached, as far as voltage supply values are concerned, when V_o is maximum, i.e., when V_{CC1} and V_{CC2} are at their maximum values.

It should be noted that V_o is a function of resistance ratios and does not depend on resistor absolute values. Therefore resistance fluctuations caused by process or temperature variations will not affect V_o.

Inhibiting. A low voltage at the strobe inputs (See Figure 18.6) will allow current to flow through the base-emitter junction of Q_{25}. Q_{25} will then saturate, and drive current will pass through its base collector diode. Q_{23} and Q_{24} will be turned off, and the voltage at point L will be high. This voltage when shifted down through the zener diode$_{23}$ will supply drive to the transistors Q_{21} and Q_{20}. Therefore the voltage at point I with respect to V_{CC2} will be:

$$V_1 = V_{CESAT_{Q_{21}}} + V_{BE_{Q_{20}}} \quad (18.8)$$

This voltage is low enough to turn off Q_{18} and Q_{19}, thereby inhibiting the driver outputs. The current supplied through R_9 will flow mainly through Q_{21} and Q_{20}.

Worst-case conditions are reached, as far as the voltage supply values are concerned, when V_o is minimum, i.e., when V_{CC1} = min. and V_{CC2} = min.

Inhibitor threshold-noise margins. The inhibitor input presents a transistor-transistor logic (TTL) gate configuration with an input logic threshold voltage level of approximately 2 V_{be}. This circuit features the same noise margins as the driver inputs, and operation is guaranteed in the same manner as explained in the paragraphs on input operation.

Inhibit input-current requirements. Input-current requirements reflect worst-case conditions for T_A = -55°C to 125°C and ΔV_{CC} of ± 10 percent. The input of the inhibitor requires no more than 3.0 mA out of the input at a logical "0" level; therefore one load (N = 1) has a 3.0 mA maximum.

The input also requires current at a logical "1" level. This current is 40 μA maximum. It should be noted that the common strobe used to inhibit both channels will require twice the logical "0" or logical "1" current required by a single strobe.

Unused common strobe. For optimum enabling and inhibiting delays, the unused common strobe should be tied to a positive voltage source of 2.4 to 5.5 V. It is also advisable to use a limiting resistor as described in the input-output section.

18.3 LINE RECEIVER CIRCUIT DESCRIPTION

High-speed voltage-discriminator circuits such as Texas Instruments SN75107 are designed to be used in many applications such as line receivers (balanced, unbalanced, party line, and general-use receivers) or comparators on data-processing equipment, process-control computers, radar interface systems, telephone switching systems, etc.

The monolithic dual line receiver shown in Figure 18.7 has two independent channels (except for the common current source, supply voltages, and ground). Each line receiver consists of a differential input stage which provides a high-input impedance, followed by a level shifting stage and a second differential amplifier which enhances the common-mode rejection ratio and driver a TTL gate output.

A strobe or gating input may be used on the output stage of either channel to hold the output at a logical "1" regardless of the input signal applied to the corresponding channel.

A common strobe is also available for both channels.

Input Differential Stage (Figure 18.8). Basically this differential stage operates as a switch. If V_{IN1} is greater than V_{IN2}, Q_1 is on and Q_2 is off; therefore

$$V_{OUT(A)} = V_{CC1} - RI_S = 3.9 \text{ V}$$

$$V_{OUT(B)} = V_{CC1} = 5.0 \text{ V} \tag{18.9}$$

This reverse situation occurs when V_{IN1} is less than V_{IN2}.

It appears that either of the inputs could withstand about +3.9 V common-mode voltage (in nominal conditions) before Q_1 or Q_2 starts saturating and affecting the speed of the overall system.

In the same manner point C is 1 V_{be} above V_{CC2} (i.e., nominally -4.2 V). V_{IN1} or V_{IN2} could go almost as low as -4.2 V before the current source Q_3 starts saturating.

To cover worst-case conditions, recommended operating common-mode voltage range is ± 3 V. The input bias current is nominally 30 nA when $I_b = I_s/(Q_1 \text{ or } Q_2)$. The logic input impedance is then high. This receiver will therefore provide very little loading to the transmission line, making it very useful in party-line data-transmission systems where cable and installation costs are minimized.

Level shifting stage (Figure 18.9) If we refer back to the preceding section, $V_{OUT(A)}$ and $-V_{OUT(B)}$ can be more exactly expressed as:

$$-V_{OUT_A} = V_{CC1} - R\ (I_S + I_b) \tag{18.10}$$

$$-V_{OUT(B)} = V_{CC1} - R_{1b} \text{ when } V_{IN1} \text{ is greater than } V_{IN2} \tag{18.11}$$

These levels are shifted down through Q_3 and Z_1 or Q_4 and Z_2 to:

$$-V_{OUT(C)} = V_{CC1} - R\ (I_S + I_b) - V_{BE} - V_z \tag{18.12}$$

$$-V_{OUT_D} = V_{CC1} - R\ (0 + I_b) - V_{BE} - V_z. \tag{18.13}$$

Q_3 and Q_4 and Z_1 and Z_2 are carefully matched to provide nominally 1 V differential at outputs C and D. The differential level between C and D will alternate polarity but will always be adequate to trigger the second differential stage.

Second differential stage (Figure 18.10). This stage also operates as a switch. When Q_5 is ON, Q_6 is OFF, and the base voltage of Q_7 is high enough to turn on Q_7.

$$V_{CE\ Q_7} = R_2 I_b + V_{BE\ Q_7},\ V_{CE} = 1\ \text{V nominally}. \tag{18.14}$$

$$V_{OUT(E)} = I_E R_3 \text{ where } I_E = \frac{V_{CC1} - V_{CE\ Q7}}{R_1 + R_3}\ . \tag{18.15}$$

This results in:

$$V_{OUT(E)}\ (\text{logical 1}) = V_{CC1} - (R_2 I_b + V_{BE\ Q7}) \frac{R_3}{R_1 + R_3} \tag{18.16}$$

and is approximately 2.5 V. With 2.5 V at point E no current will pass through the base-emitter diode of Q_8. This constitutes a logical "1" level for the output gate.

When Q5 is off and Q_6 sinks I_S (1 mA), the base of Q_7 is at a voltage level of $V_{CC1} - (R_1 + R_2)\ I_S$ 0 V nom). This is low enough to turn off Q_7.

The resulting low voltage at point E will allow current to flow through the base-emitter junction and R_3 and R_5 to act as a divider, resulting in

$$V_{OUT(E)}\ \text{logical "0"} = (V_{CC1} - V_{BEQ8}) \frac{R_3}{R_3 + R_5} = 0.6\ \text{V (nom.)} \tag{18.17}$$

$$V_{CC1} - V_{BEQ8} = 4.2\ \text{V (nom.)}. \tag{18.18}$$

This constitutes the logical "0" level for the output gate. Values and layout of R_1, R_2, R_3, R_4, and R_5 have been carefully arrived at to achieve convenient logical "0" and logical "1" levels for temperatures between -55°C and 125°C under supply voltage variations of ± 10 percent.

Output gate. The output gate uses a standard series 54 TTL gate with a nominal $-V_{OUT(0)}$ = 240 mV at 20 mA and $V_{OUT(1)}$ = 3.35 V at -0.5 mA. Two strobes have been provided at the input of each gate. The reciever function will be enabled or inhibited respecitvely when a logical "1" level is applied to both strobes, or a logical "0" level to either strobe.

18.4 RECEIVER INPUT CONSIDERATIONS. The input sensitivity is defined as the differential dc voltage required at the inputs of the receiver to force the output to the logic gate threshold voltage level. The input sensitivity of the SN75107 is nominally $\leq$ 3 mV. This feature is particularly important when data are transmitted down a long line and the pulse is deteriorated because of cable losses.

Common-mode voltage range. The CMVR is defined as that voltage which is applied simultaneously to both input terminals and which, if exceeded, will not allow normal operation of the receiver.

Recommended operating CMVR is ± 3 V. However, in some particularly noisey environments common-mode voltage could easily reach ± 10 V to ± 15 V if precautions are not taken to reduce ground noise, power-supply noise, and crosstalk problems. When the receiver is to operate under such conditions input attenuators should be used to decrease the voltage seen by the differential inputs. Differential noise will also be reduced by the same ratio.

These attenuators have been intentionally omitted from the receiver input terminals so that the designer may select resistors which will be compatible with his particular application or environment. Furthermore, the use of attenuators will adversely affect input sensitivity, propagation time, power dissipation, and in some cases input impedance (depending on the selected resistor values) and versatility of the receiver.

Input termination resistors. To prevent reflections the transmission line should be terminated in its characteristic impedance.

Matched termination resistances normally in the range of 25 ohms to 200 ohms are required not only to terminate the transmission line in a desired impedance, but also to provide a necessary dc path for the receiver input bias.

If careful matching of the resistor pairs is not observed the effective common-mode rejection ratio will be reduced.

Reference voltage. The receiver can be used as a single-ended line receiver or comparator by referencing one input.

The operating threshold voltage level is established by and is approximately equal to the applied reference input voltage V_{REF} (selected within the operating range).

A simple method of generating the reference voltage is the use of a resistor voltage divider from either the positive V_{CC1} or negative V_{CC2} voltage supplies.

The reference could also be obtained by a diode or a reference supply or just ground. Bias current required at the reference input is low (nominally 30 μA). Therefore voltage dividers of this type may normally be operated with very low current requirements and may be used also to supply a number of paralleled reference inputs.

In noisy environments the use of a filter capacitor may be helpful.

18.5 DUAL DIFFERENTIAL COMPARATOR

Connected as a differential comparator the SN75107 may be used to compare the non-inverting input terminal with the inverting input, so that a digital "1" or "0" is experienced at the output resulting from one input being greater than the other (See Figure 18.11).

There are many applications for differential comparators, such as voltage comparison, threshold detection, controlled Schmitt trigger, and pulse width control.

The strobe inputs allow for additional control over the circuit, permitting either output or both to be inhibited.

18.6 FURNACE CONTROL

The SN75108 is identical to the SN75107 except that it features an open-collector

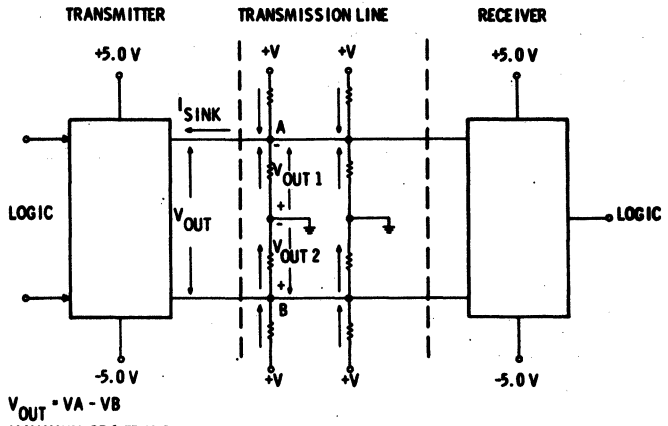
output. The circuit in Figure 18.12 is given as an example of the IC's possible use in areas other than what would normally be considered electronic systems.

Basically, where the room temperature is below the desired level, Channel A input will be above (more positive than) the reference level set on the input differential amplifier. This will in turn cause a high output to operate, the heat-on relay turning on the heat. The output is tied to one of the strobes of Channel B.

When Channel A is on, Channel B can be turned on. The Channel B input will be turned on when the bonnet temperature of the furnace reaches the desired level. Normally the furnace will be shut down when the room temperature reaches the desired level and Channel A is turned off. There is also a safety switch in the bonnet which will shut down the furnace if the temperature at this point exceeds desired limitations. The types will be determined by the particular operating conditions encountered.

FIGURES

Figure 18.1. Typical data transmission system.
Figure 18.2. SN75109 circuit schematic.
Figure 18.3. Driver input stage.
Figure 18.4. Driver level shifting stage.
Figure 18.5. Driver output stage.
Figure 18.6. Driver inhibit stage.
Figure 18.7. SN75107 circuit schematic.
Figure 18.8. Receiver input differential stage.
Figure 18.9. Receiver level shifting stage.
Figure 18.10. Receiver second differential stage.
Figure 18.11. Line receiver as a differential comparator.
Figure 18.12. Line receiver as a furnace control.



$V_{OUT} = VA - VB$

MAXIMUM OF 1 TRANSMITTER "ON" AT ONE TIME

ARROWS INDICATE ACTUAL DIRECTION OF CURRENT FLOW

Figure 18.1. Typical data transmission system.

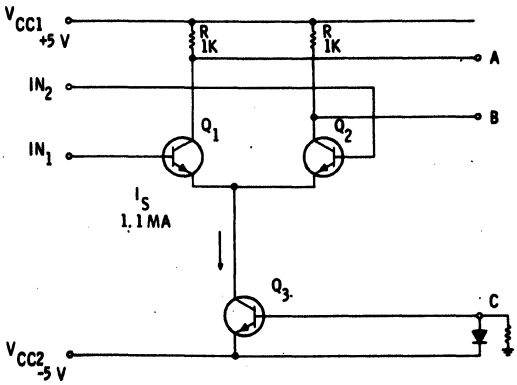


Figure 18.3. Driver input stage.

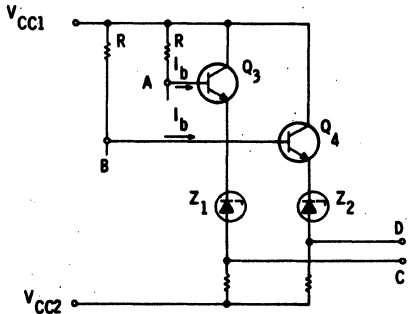


Figure 18.4. Driver level shifting stage.

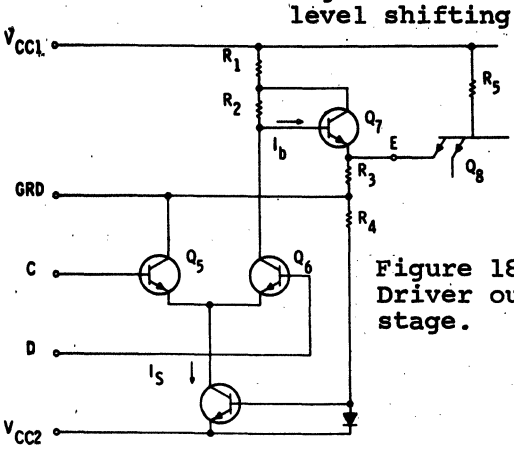


Figure 18.5. Driver output stage.

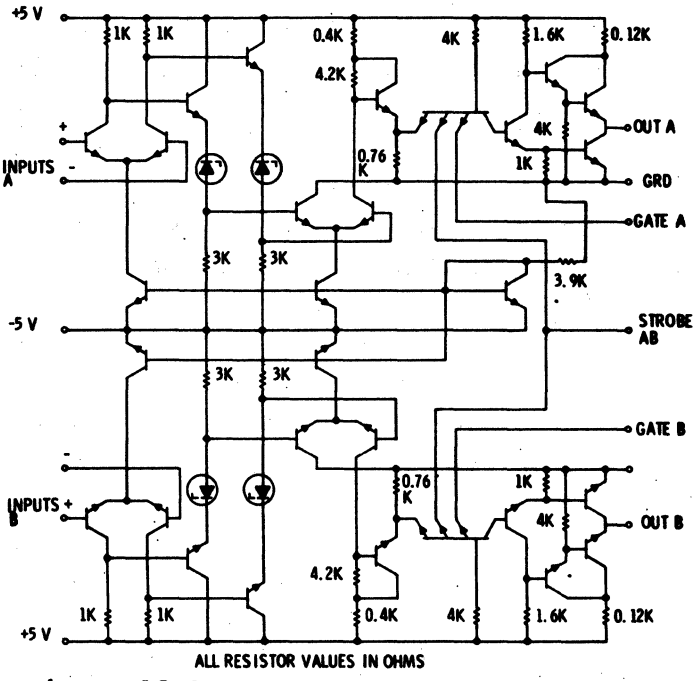


Figure 18.2. SN75109 circuit schematic.

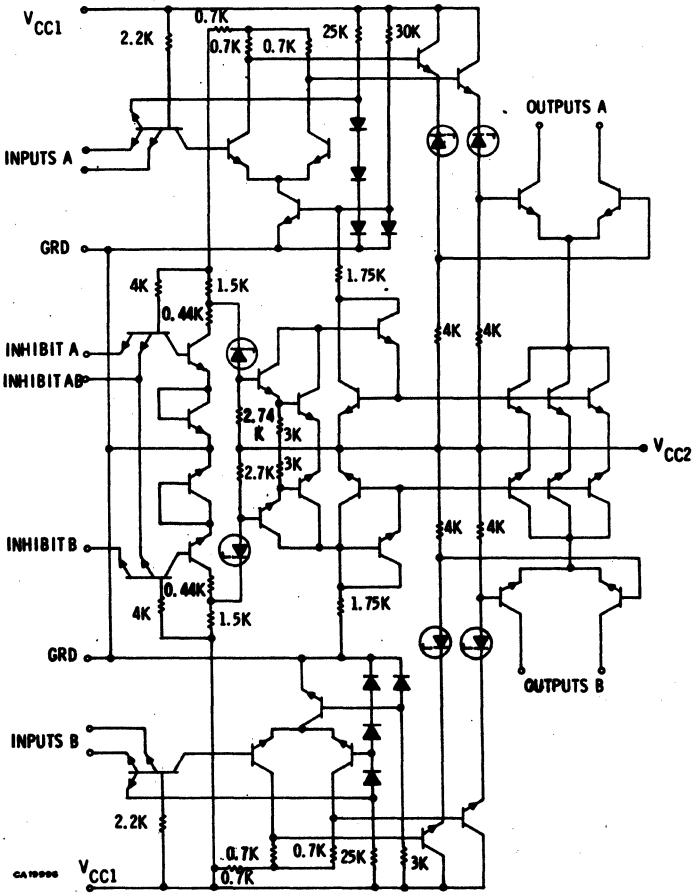


Figure 18.6. Driver inhibit stage.

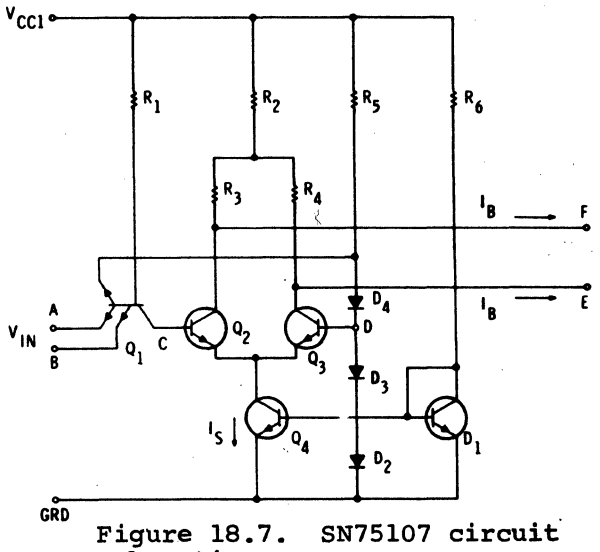


Figure 18.7. SN75107 circuit schematic.

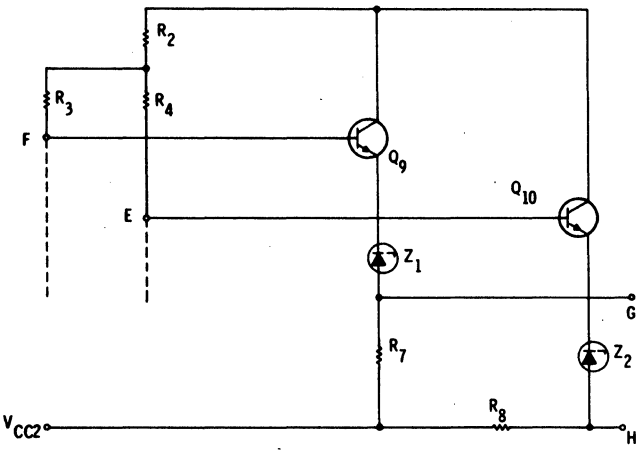


Figure 18.8. Receiver input differential stage.

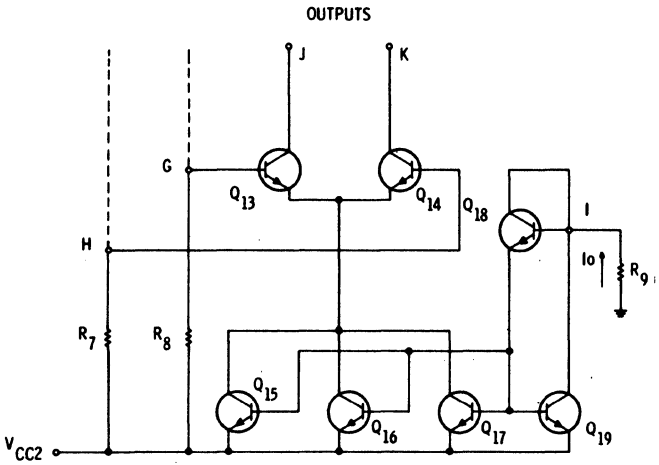


Figure 18.9. Receiver level shifting stage.

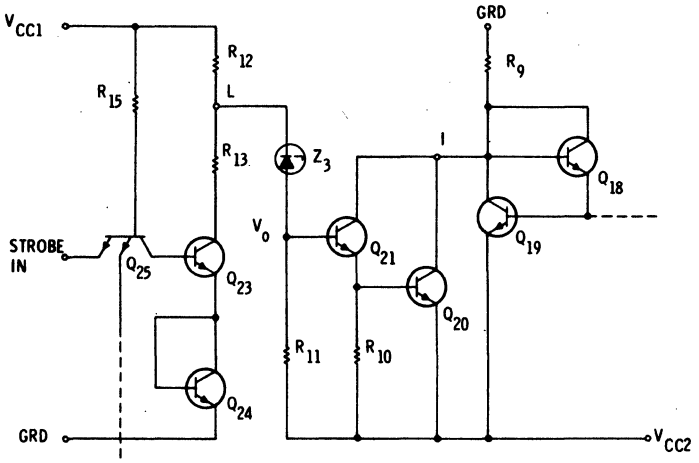


Figure 18.10. Receiver second differential stage.

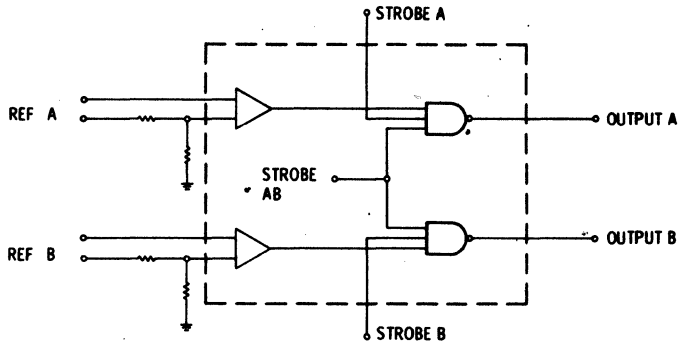


Figure 18.11. Line receiver as a differential comparator.

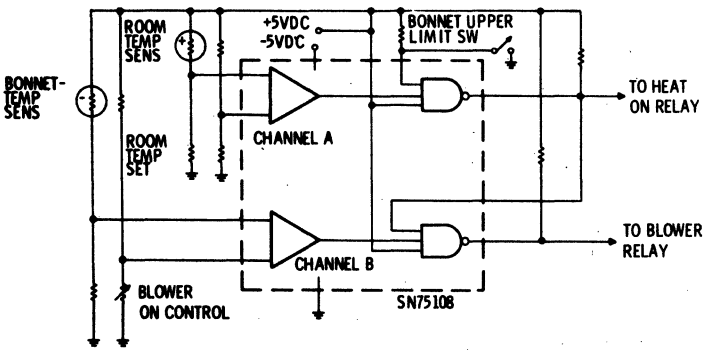


Figure 18.12. Line receiver as a furnace control.