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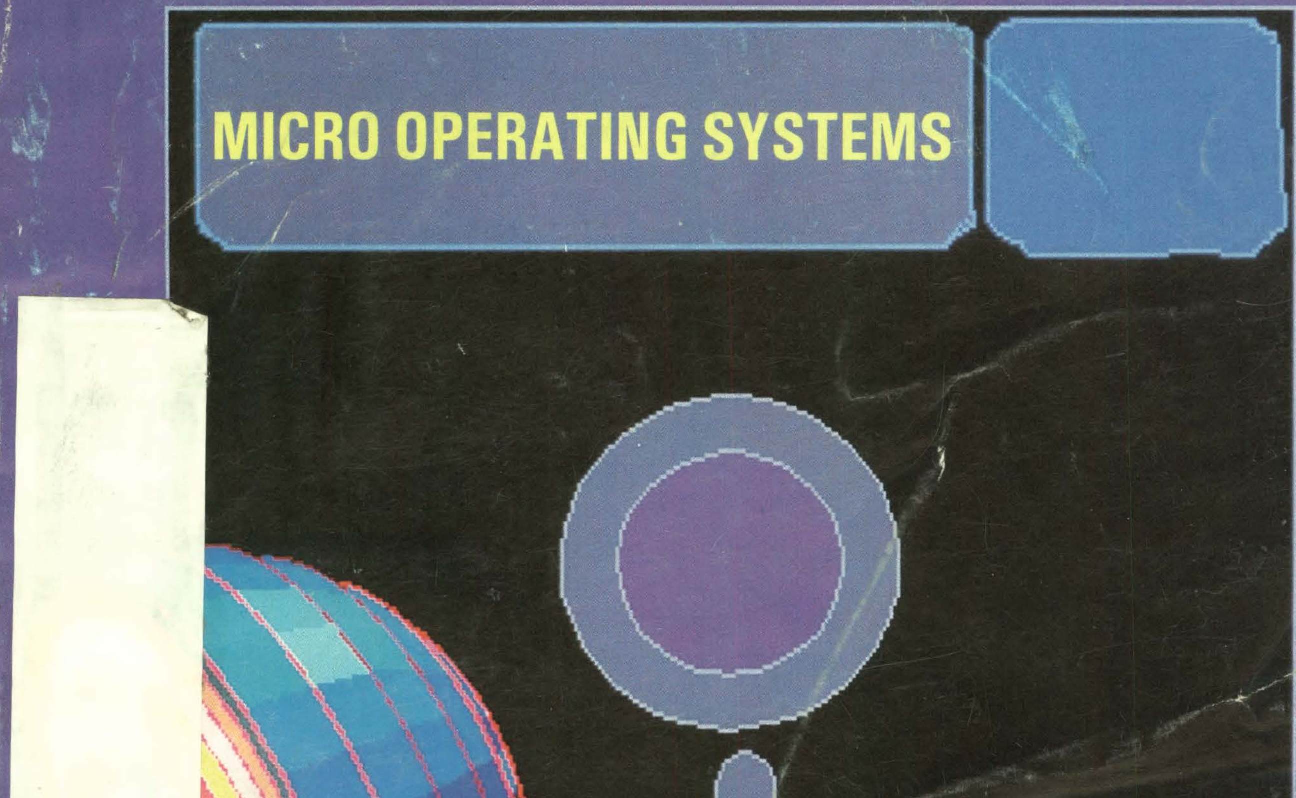
OMPUTER DESIGN

TH E OF COMPUTER BASED SYSTEMS

JULY 1984



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STANDARDS CAN EASE PRODUCT DEVELOPMENT

NETWORKING TECHNIQUES STREAMLINE MULTIPROCESSING

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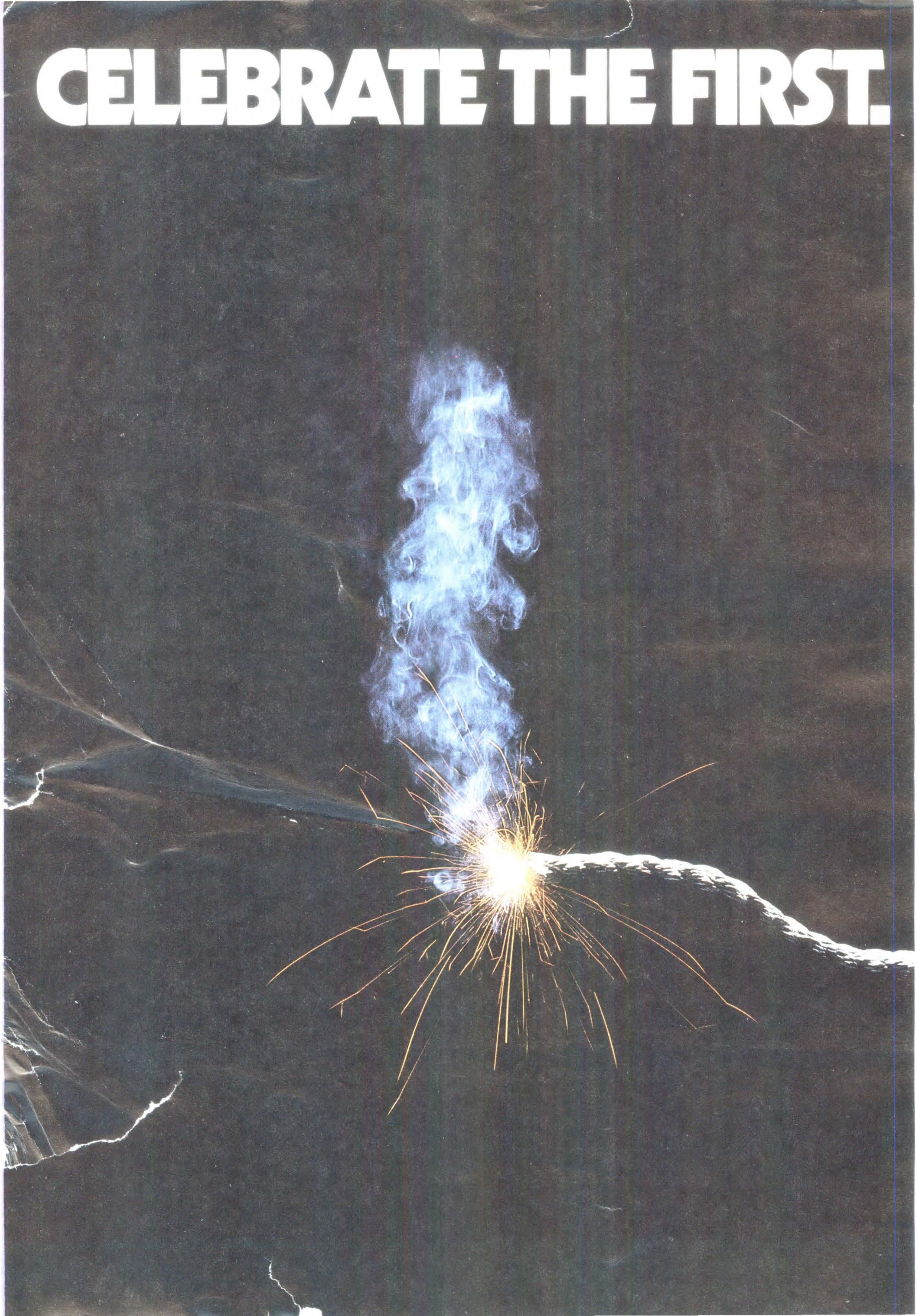
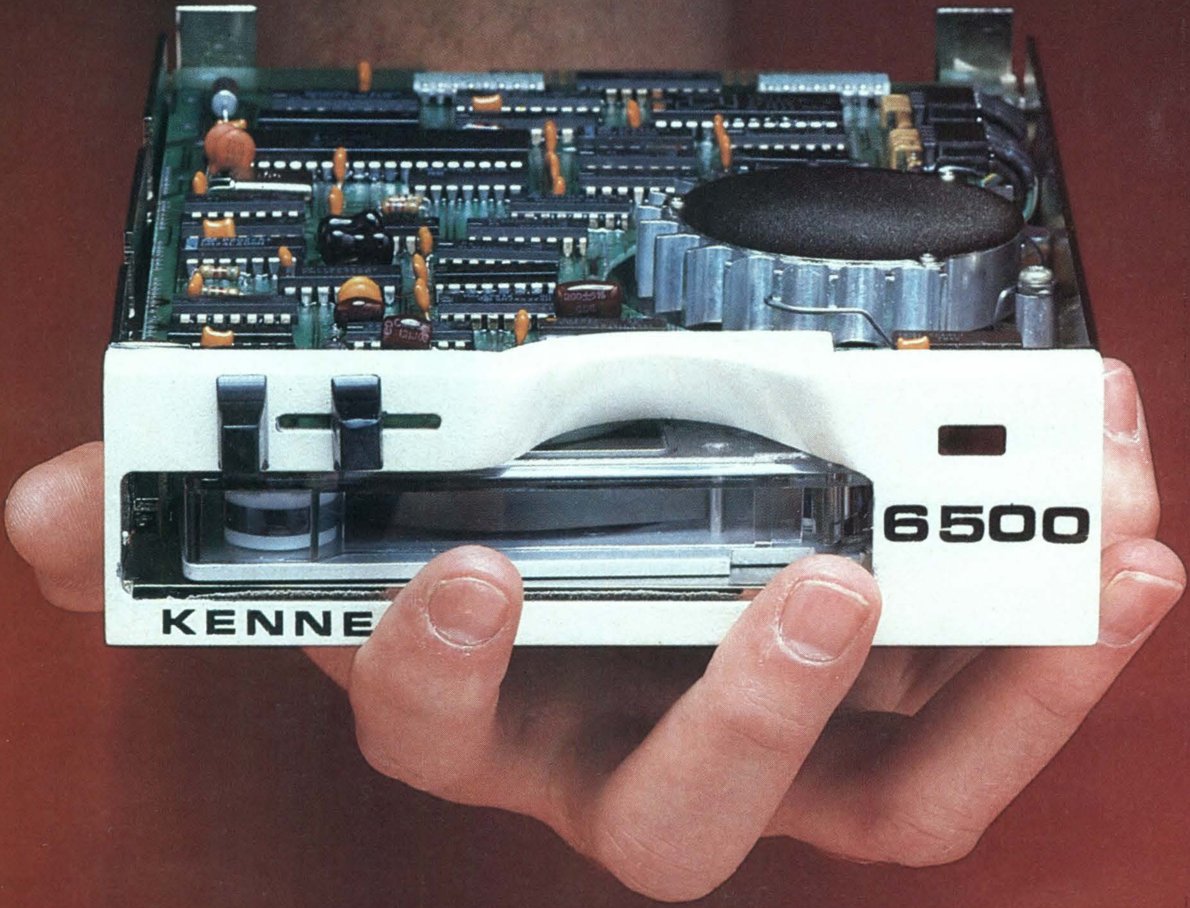
CIRCLE 1

THE FIRST


CELEBRATE THE FIRST.

Introducing Model 6500 —

'the handful'



Kennedy's Model 6500 5¼" Cartridge Recorder — it fits in your hand, but it's more than a handful of new and unique features, such as:

- 16 KBYTE Buffer — Model 6500 can transfer data at a burst rate of up to 3 MBYTE/sec., and maintain streaming longer in systems with little buffering.
- 150 MS Ramp Time — Data access time and reposition time is cut in half; and it can better operate in a Pseudo s/s mode.
- Direct Drive Motor — Assures much higher reliability and lower I.S.V.

Finally, and best of all, Model 6500 features a simple mechanical design — loading is simple, moving the tape to the head instead of the head to the tape.

Model 6500 is one big handful of what you've been looking for in a 5¼" cartridge recorder. Write or call us.

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CIRCLE 2

COMPUTER DESIGN®

System technology

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System design

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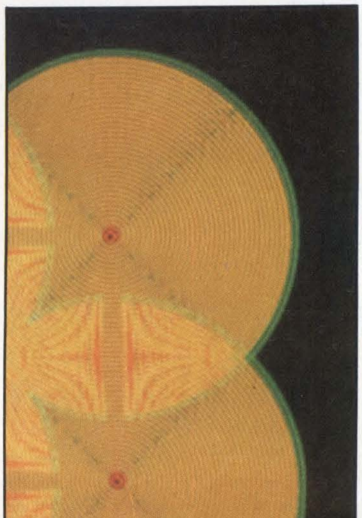

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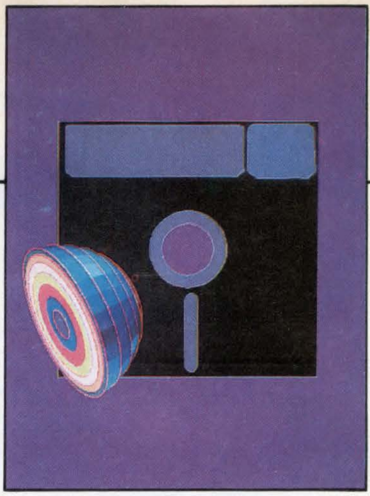

This month's cover was created and designed by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system.

Special report on microcomputer operating systems

System components

Departments

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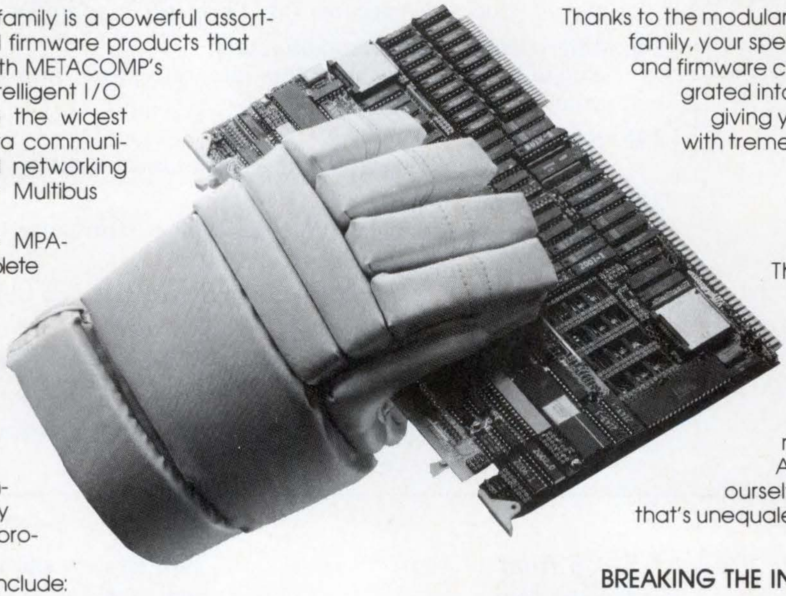

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The COMM-2000 family is a powerful assortment of software and firmware products that perfectly integrate with METACOMP's MPA-2000™ CPU/Intelligent I/O Controller to provide the widest possible range of data communications protocol and networking support available to Multibus system integrators.

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CIRCLE 3

UP FRONT

Technology innovator diversifies OEM offerings

While the large innovative consumer electronics company has been selling 3½-in. drives and disks to a few key OEM customers for close to two years, Sony has now officially launched its Component Products Division to diversify its OEM offerings. Four product targets have been identified: data, displays, semiconductors, and image sensing products. Except for the display product line, which will be part of the consumer product line out of San Diego, Calif, the products will be manufactured in Japan. The division's biggest push, according to Kevin Finn, vice president and general manager, will be in the semiconductor area. Among the first semiconductor chips to be offered will be a CMOS multiplier-adder for digital video signal processing applications that uses a pipelined architecture to achieve an arithmetic operation cycle time of 69 ns. The CX 7997 IC can perform the following operations: 10 x 10 + 16 bits; 10 x 10 bits; 16 + 16 bits; and a delay operation. The unit will be available for $300 this fall. Among products from the other three groups will be high resolution Trinitron monitors for the CAD/CAM industry, CCD color image sensor modules and chips and, of course, the 3½-in. double-sided, double-density disks and accompanying drives that are already part of Hewlett-Packard's HP 150 touch-screen computer and Apple's Lisa and MacIntosh machines.—*N.M.*

Full 32-bit microcomputer to debut as plug-in board

Texas Instruments designers at the firm's Irvine, Calif NuBus and Nu Machine operation are preparing a Motorola 68020 microprocessor-based microcomputer board to run AT&T System V Unix on TI's Nu Machine workstation/computer. The board allows computer system designers performing development work with the multiprocessing-geared Nu Machine to enjoy microcomputer functionality such as full 32-bit internal and external data paths and memory management. Insiders expect that the Irvine designers might get a TI headquarters notice to drop the 68020 and design the same add-on board using National Semiconductor's (Santa Clara, Calif) full 32-bit 32032 microprocessor, now that TI and National have a joint microprocessor development agreement. The NuBus heart of the Nu Machine is designed as a read/write bus only (for processor independence) so a redesign will not generate bus interface problems.—*H.H.*

Unix rides the S-100 bus

For some new system designs the IEEE 696 (S-100) bus is not yet dead. A 68000-based system running Unisoft Unix System V and built around a 14-slot S-100 motherboard will be introduced by Morrow Designs (Hayward, Calif). Called Trinity, the system will have a 512-Kbyte minimum main memory, expandable to 2 Mbytes, and will incorporate the Motorola 68451 MMU. Storage options will include one to four Winchester drives in either 16- or 34-Mbyte capacities, and 5¼-in removable cartridge hard disk. One 400-kbyte floppy drive will be standard and three more can be added. Trinity incorporates a "three-point" DMA architecture, with DMA channels between main memory and I/O, hard disk, and floppy disk channels. In September, Morrow will introduce 80188-based slave processor boards with 128 to 512 Kbytes of onboard, dual-port RAM. These will be able to run MS-DOS applications on the Unix machine transparently to the user. Cost for a minimal configuration may be under $5500.—*T.W.*

Three processor workstation/computer offers Lisp, Prolog, and Unix

Not content with its Lambda 2X2 workstation/computer for two-user Lisp and Unix development, LISP Machine Inc (Los Angeles, Calif) has gone a step further. The firm will now offer the 2X2/Plus, which sports two proprietary, microprogrammable, 32-bit tagged architecture Lisp processors, and a Motorola 68010 processor. The three independent, concurrently-executing processors can handle the Zetalisp-Plus environment, a Prolog software package that runs in the Zetalisp environment, and Unix System V, respectively. All processors communicate during concurrent operation through the firm's extended-streams interface. This software works with the processor-independent NuBus from Texas Instruments (Irvine, Calif) that is the basis of the Lambda machine's bus-centered architecture.—*H.H.*

Hard disk drive has built-in controller

Drive electronics and hard disk controller electronics will be offered on a single circuit board by Xebec Corp (Sunnyvale, Calif), which plans to market the "Owl," a half-height, 10-Mbyte Winchester drive. The Owl will incorporate the integrated board and offer a SASI interface. Xebec will also license its technology to adapt head/disk assemblies from different drive manufacturers. This type of integrated drive is expected to be especially appealing to such systems as personal computers that incorporate only one hard disk and need maximum space and board efficiency at minimum cost.—*T. W*

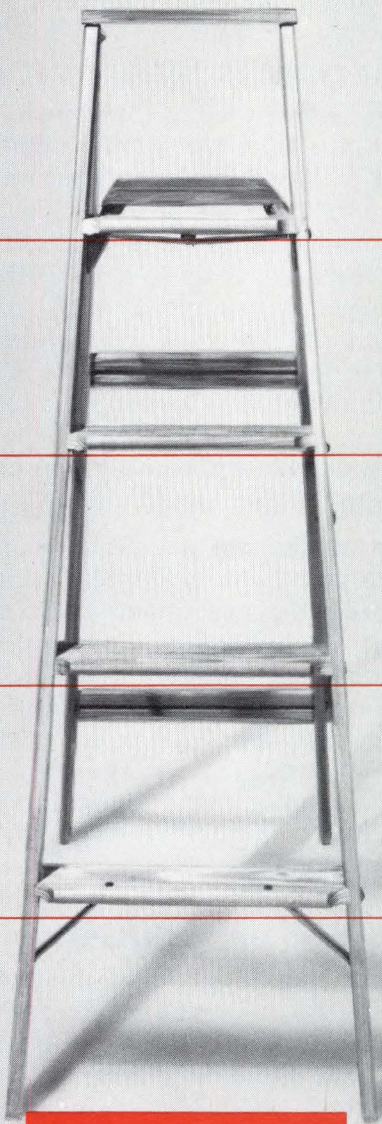
Computer-aided software environment set to make its mark

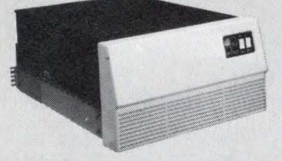
Apollo Computer (Chelmsford, Mass) has developed a computer-aided software engineering environment for distributed workstations. In field test, the Domain Software Engineering Environment (DSEE) runs on the firm's workstations and the Domain network that links them. DSEE provides the computer system designer with source code control, configuration management, release control, advice and task management and user-defined dependency tracking with automatic notification. DSEE is an extension of software environments developed for AT&T's Unix, SofTech Microsystem's Ada, and Xerox's Cedar. It is implemented as one program running at network nodes and is based on five "managers"—software that takes care of history, configuration, tasks, monitoring, and advice. Geared to major system efforts, Apollo uses DSEE to develop microcode, graphics software, languages, and documentation. Future extensions will include structure editors and interpretive debuggers.—*H.H.*

Lisp gets a lift from DEC

Designed to run on the Digital Equipment Corp (Marlboro, Mass) VAX computer line and VAXclusters, Digital's VAX Lisp package is said to be the first fully-supported artificial intelligence product available from and developed by a major computer manufacturer. The package is aimed at programmers and researchers in industry, university, and government activities, and is an implementation of Common Lisp, a version of the language that is becoming a *de facto* standard for Lisp programmers. The Lisp language was originally developed to manipulate symbolic data as well as to compute with numeric values. It is particularly useful in the development of programs representing real-world objects, properties, or relationships between objects. Its capabilities are especially important to artificial intelligence programmers, since the programs they develop can simulate human behavior and thought.—*J.H.*

Step up the performance of your DEC system with Dataram's full range of peripheral subsystems





DATARAM S35/FUJITSU EAGLE

Fujitsu's Eagle, combined with Dataram's S35 controller, adds up to more than a high performance alternative to DEC's UDA50 subsystem. This package of peripheral performance conforms to DEC's MSC protocol and gives you 474 MB of storage at a data rate of 1.8 MB/sec. The S35/Eagle subsystem interfaces to the PDP or VAX UNIBUS and functions under all of DEC's current operating systems, including VMS.

DATARAM D30

"Versatile" is the only word that can describe our 7" D30 subsystem. It combines a ¼" start-stop/streaming cartridge tape unit and an 8" Winchester. The D30 uses the 70 MB CDC Sentinel cartridge drive and emulates the TS11 or TSV05. The Winchester emulates RM02, RK06/07, or the new UDA50, and provides 80 or 160 MB. The D30 operates with all of DEC's minicomputers: LSI-11, PDP-11, VAX, and microVAX.

DATARAM D23

This RL02-emulating subsystem for the Q-Bus provides a 10.4 MB fixed/10.4 MB removable Winchester along with an additional 20 MB Winchester. Both 5¼" Winchesters are directed by a single dual-board controller which treats the total 40 MB capacity as four logical RL02s.

DATARAM FD-311

RX01/RX02/RX03 dual floppy subsystem packaged in a compact 5¼" chassis. Our FD-311 and larger-capacity FD-511 come with a dual-board controller for the LSI-11 Q-Bus or a quad-board controller for your PDP-11 and VAX UNIBUS.

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Joining forces to conquer the CAE market

When the leader in the installed user base of CAD/CAM systems decides to form a joint venture with a hi-tech computer-aided electrical engineering company the result could be a formidable force in the CAE industry. Computervision Corp (Bedford, Mass) has joined with Metheus Corp (Hillsboro, Ore) to form Metheus-CV Inc, and to design, develop, and market electrical CAE workstation products. While Computervision has an installed base of CAD/CAM equipment of over $1.25 billion worldwide, the company lacked good graphics products for such applications as IC and PC board design. This joint venture will be able to bring such products as gate array and PC board design workstations to the market much faster. Metheus-CV, to be headquartered in Hillsboro, Ore, will bring out turnkey workstations for design engineers in the CAE/CAD/CAT/CAM application areas. The joint venture agreement is predicated on Metheus shareholders' approval and will be initially financed with $10 million from Computervision at a rate of $1 million/month.—*N.M.*

Single-chip VMEbus controller replaces fistful of ICs

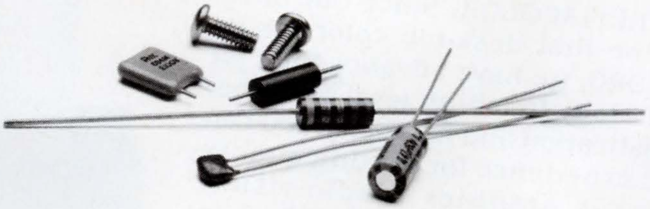
This month, Signetics Corp (Sunnyvale, Calif) will debut the computer industry's first single-chip VMEbus controller. The 23-pin DIP SCB68172 replaces up to 20 ICs (often on a separate board) that would otherwise have to be used by a computer designer to implement a controller. The chip's main function is to arbitrate and switch bus-to-board and board-to-bus signals at up to a 25-MHz rate. It achieves this speed by means of Signetics' proprietary high speed bipolar process and is designed as a gate array using integrated Schottky logic. Two different chip versions handle general-purpose or DMA-based controllers. Propagation time for a clock input to become a clocked output is only 75 ns. This is achieved by operating the chip in a pipelined mode so that there is overlap with the VMEbus address decoding cycle.—*H.H.*

Standards for future ADP systems are under development

Two American national standards for intelligent peripheral interface under development concern logical device specific command sets and logical device generic command sets. The work is under the auspices of X3T9, the ANSI X3 technical committee on I/O interface. One goal of the committee is to simplify the design, development, and utilization of future automated data processing (ADP) systems. The project is on specific command sets for disk drives and supports the proposed intelligent peripheral interface standard currently underway within X3T9. A major thrust in the generic command set effort is the interconnection of masters to slaves within intelligent subsystems in the areas of disk, tape, and communications requiring high speed data transfer.—*J.H.*

P-System operating system to take on multitasking

Although p-System (SofTech Microsystems, San Diego, Calif) operating systems sales pale by comparison with MS-DOS, the p-System continues to gain in utility for computer designers and application developers. The p-System licensee Network Consulting, Inc (NCI) of Burnaby, British Columbia, will soon introduce a p-System Unix emulator geared to vertical markets. IBM has purchased the NCI p-machine emulator (through SofTech) and plans to incorporate it later this year in a p-System version. The new version may have XT support. NCI's claim to fame has been its p-System speed—said to be up to five times faster than IBM's p-System speed. And, in September, NCI will introduce a new MS-DOS compatible p-System.—*H.H.*



WHO CREATES THE JOBS?

Most engineers fervently believe that advanced technology in general, and the computer industry in particular, benefit everybody by creating new jobs, by improving the quality of life, and by ensuring economic growth. We should not, however, assume that the general public shares our optimistic outlook. A recent poll conducted by Louis Harris and Associates for *IEEE Spectrum* magazine points out the discrepancy between the engineers' view of science and technology and that of the American public. Of the IEEE members who responded, only four percent disagreed with the statement that science and technology have done more good than harm. Yet, in a Harris poll of a national cross section of the public, 14 percent held this negative view of the technology benefits.

Of course, engineers and the general public share some concerns about negative aspects of technology, such as the threat of powerful military weapons in the wrong hands, or the massive invasions of privacy made possible by computer and communication systems. (After all, this is 1984). The real split between engineers and the general public centers on the employment issue. The computer industry and organized labor seem to have diametrically opposing views.

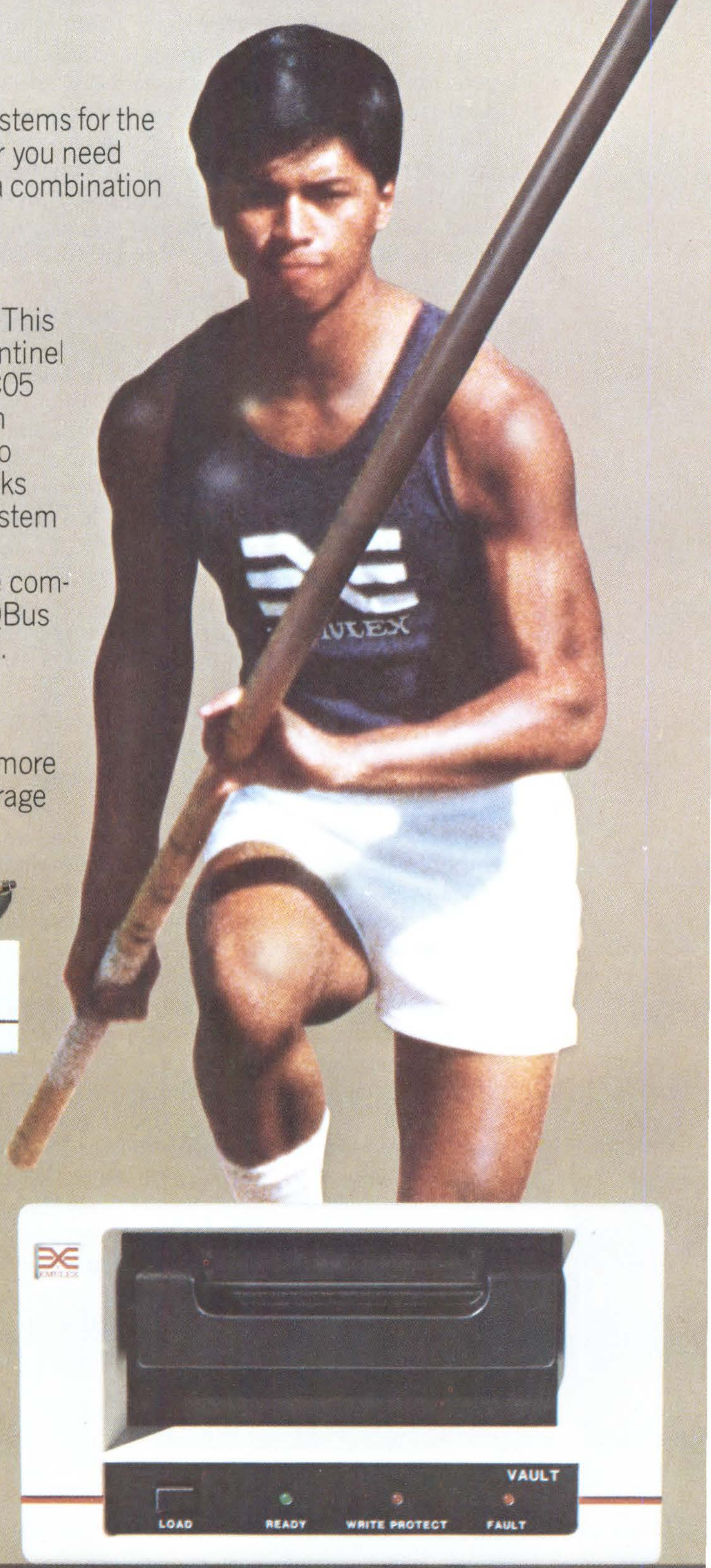
Engineers tend to blame labor unions for lagging U.S. productivity, while organized labor points to the manufacturing jobs lost to automated and offshore manufacturing. For example, in the Harris/IEEE poll, 72 percent of the engineers felt that U.S. productivity was "only fair" or "poor." Of the respondents holding this negative view, 80 percent blamed trade unions for the failure. Labor unions, and research organizations favoring their viewpoint, claim that less than six percent of all new jobs in this decade will be in high technology. Labor also points out the limited unionization and low wages of clerical and production workers in high tech companies. For example, production workers for the electronic components industry had an average annual income of less than $14,000 in 1981.

A lot of pro-union propaganda is based on projections by the Bureau of Labor Statistics, which show that the 10 occupations with the largest expected new job growth are clerical or service jobs. None is directly related to high tech. In descending order of employment growth projection for this decade, the occupations are as follows: secretaries, nurses aids, janitors, sales clerks, cashiers, professional nurses, truck drivers, fast-food workers, general office clerks, and waiters/waitresses. In reply, of course, computer-industry advocates counter that one can prove almost anything with statistics. The simplistic analysis by labor representatives overlooks the fact that every 100 high tech jobs tend to generate about 70 jobs in regular industry and services. In other words, secretaries may be working for engineers, or fast-food workers may be preparing lunch for engineers.

A balanced view of the employment situation was presented by Leonard N. Mackenzie, chairman and CEO of General Automation Inc, in a recent article for the *Los Angeles Times*. He said, "There is no question that computers and automation eliminate jobs. But there is also no question that computers and automation create new jobs. They create a crying need for skilled specialized workers. They create pages of want ads for various types of information handlers, from analysts and programmers to word processor operators. The dilemma is easy to state and difficult to solve: How do we move the workers displaced from 'old' industry to the jobs that 'new' industry will offer?" Mackenzie's proposed long-range solution is to achieve a goal of *adult* computer literacy via retraining programs subsidized by the federal government, and administered by industry and organized labor.

Michael Elphick
Editor in Chief

EMULEX IMPROVES AND TAPE BACKUP BY



Emulex sets the pace with three great storage subsystems for the full range of DEC QBus and Unibus systems. Whether you need Winchester disk, cartridge disk, ¼" streaming tape, or a combination unit, you'll be a step ahead with Emulex.

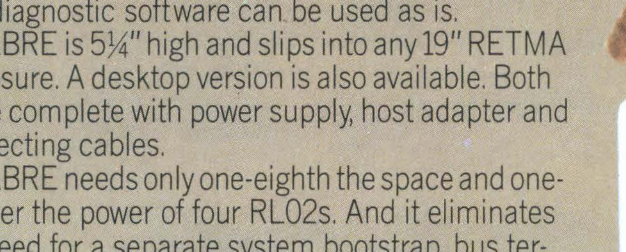
INTRODUCING VAULT.™

Emulex rises above the competition with the Vault.™ This 70-MByte tape subsystem is built around the CDC Sentinel ¼" cartridge tape streamer and uses Emulex's own TC05 (QBus) or TC15 (Unibus) tape coupler to interface with your system. The Vault is totally software transparent to standard TS11 software. So this compact tape unit looks just like a big ½" TS11 subsystem to your operating system and diagnostics.

Vault comes complete with power supply in a single compact cabinet. It's the perfect backup unit for smaller QBus systems such as the MICRO/PDP-11 and MICRO/VAX.

PRESENTING SABRE.™

SABRE™ is a sharp solution for LSI users who need more storage and backup. It packs 31.2 MBytes of main storage onto a 5¼" Winchester and 10.4 MBytes of backup onto a removable 8" cartridge disk.



And since SABRE is an exact RL02 emulation, all existing operating and diagnostic software can be used as is.

SABRE is 5¼" high and slips into any 19" RETMA enclosure. A desktop version is also available. Both come complete with power supply, host adapter and connecting cables.

SABRE needs only one-eighth the space and one-quarter the power of four RL02s. And it eliminates the need for a separate system bootstrap, bus terminator and clock control board.

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ANNOUNCING MEDLEY.™

Emulex has another winning combination with the Medley™ Winchester cartridge tape subsystem. It gives you either 35 or 110 MBytes of formatted storage and up to 70 MBytes of streaming tape backup. The Medley is fully software transparent to the operating system and diagnostic software of QBus and Unibus CPUs. And it uses the powerful and versatile Small Computer System Interface (SCSI) which keeps your options open for peripheral expansion.

Medley is interfaced to the system with a TC05/TC15 tape coupler and a UC02 (QBus) or UC12 (Unibus) host adapter. By using the Mass Storage Control Protocol (MSCP), the UC02 and UC12 allow the operating system to utilize the precise characteristics of the Winchester disk drive without patches or modifications to the operating system.

For convenience, Medley's disk drive, tape drive and power supply all fit into an attractive cabinet that easily mounts in a standard 19" rack. The Medley is also available in an attractive desktop version.

Find out how Emulex subsystems can keep you ahead of the game. Call toll-free (800) 854-7112. In California (714) 662-5600. Or write Emulex Corporation, 3545 Harbor Blvd., P.O. Box 6725, Costa Mesa, CA 92626.

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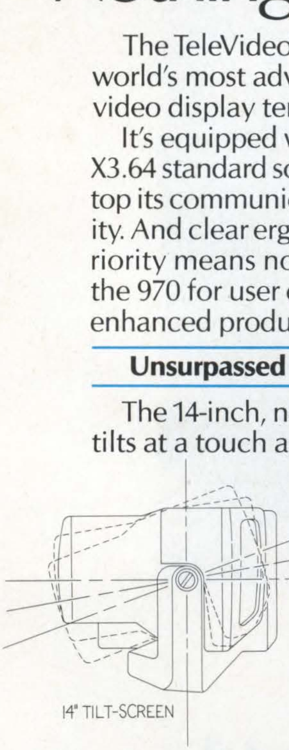

double wide characters and an excellent selection of visual and graphic attributes. For an almost endless array of displays and forms.

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The 970 is compatible with the DEC VT-100/52,® but offers more of the kind of power you'd expect to find at the top. Power that emanates from ANSI — the universal language of data management equipment.

Power that is more effectively directed by 16/32 programmable, non-volatile function keys, logical attributes, a 256 character downloadable soft font, and an optional Tektronix 4010/4014 graphics board.

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The 970 promises state-of-the-art technology you can use with confidence, with peace of mind.

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CIRCLE 13

Computers can not only add and subtract. They can divide.

RACAL

To shorten your electronic design times, you can provide your project teams with Computer-aided Engineering, Design and Manufacturing systems. And those systems will do their individual jobs very well.

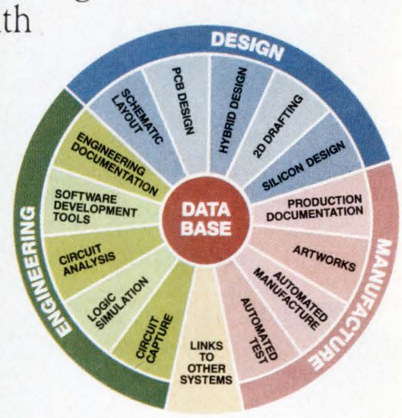
However.

As soon as you try to transfer the data generated by your engineers to the design stage (not to mention manufacturing) you'll find you have a problem. Because none of the systems are fully compatible with each other. Engineering can't get along with Design. Design can't get along with Manufacturing. And vice versa. Worse still, when the systems can't get along, neither can the people using them. So instead of state-of-the-art, you end up with something akin to a state of war.

The solution, of course, is to work with one company that can handle the entire project from beginning to end. A company with a full range of modular systems for every stage of every electronic design project. All fully integrated around a common data base.

That company is Racal-Redac.

With Racal-Redac, you can solve today's problems without creating new problems for yourself tomorrow. Because all the system modules were designed to work together, and grow with you as your needs grow.



Finally, a totally integrated capability for electronics.

Read that last paragraph again. We at Racal-Redac are talking about a range of complete, totally integrated systems which work for you through every stage of the design cycle.

Only unlike other companies, what we're talking about isn't a vague promise for the future. Racal-Redac systems are already hard at work right now in over 1,000 electronics companies around the world. Any one of which we will be happy to discuss in considerable detail.

Just clip your business card to this ad. Or write. Or call. But don't wait for someone else to work it out. Because the alternative to integration is disintegration.

RACAL-REDAC

Linking Concept to Product

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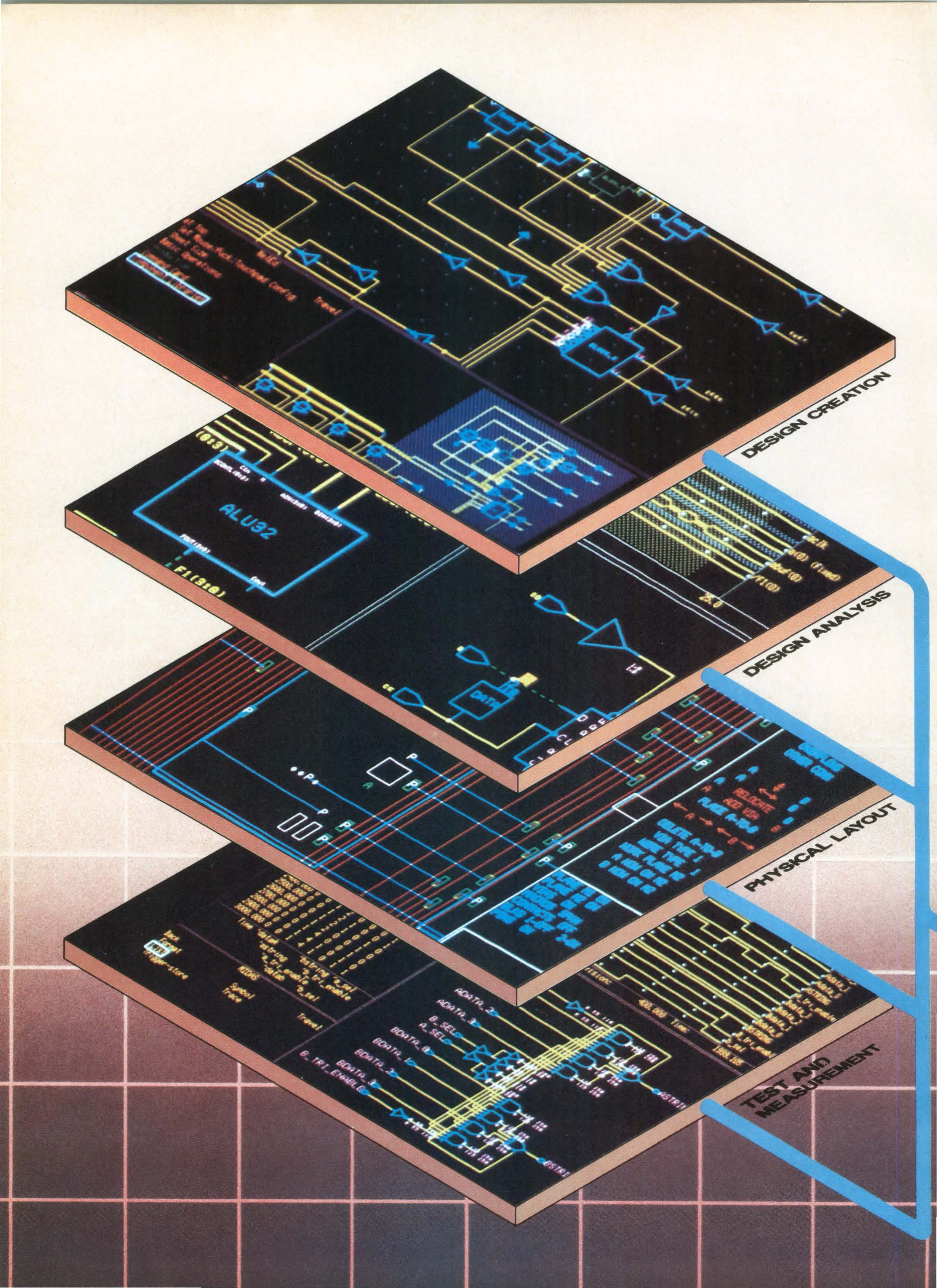
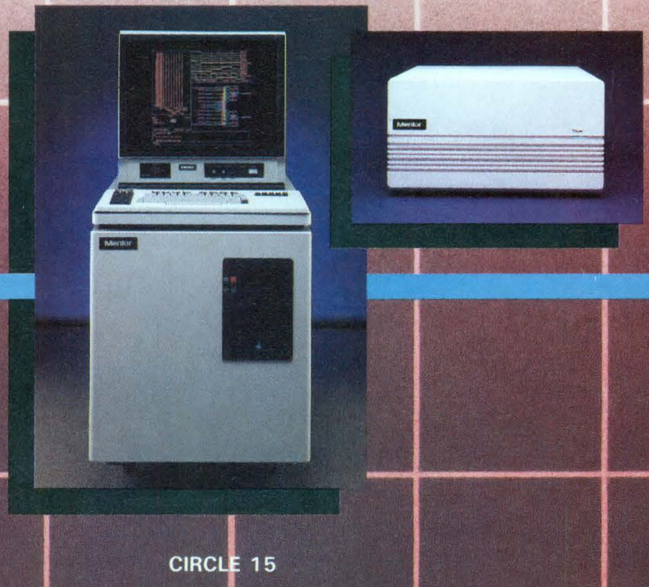

DESIGN CREATION
DESIGN ANALYSIS
PHYSICAL LAYOUT
TEST AND MEASUREMENT
ALU32



When you're designing a first-rate computer system, it doesn't make sense to compromise with a second-rate monitor.

Consider PGS instead. We make three no-compromise monitors, all fully compatible with the IBM-PC, to match your requirements and your budget.

High resolution PGS set the price/performance standard for high resolution RGB color monitors with the HX-12: .31mm dot pitch, 690 dots horizontal resolution, and precise color convergence for a crisp, sharp image.

Super resolution And, when your specifications call for super resolution, there's our no-compromise SR-12: an RGB monitor with a horizontal scan rate of 27.5 KHz which supports 690x480 resolution in non-interlaced mode.

Monochrome For price/performance in a monochrome monitor, we've set the standard with the MAX-12: our amber monitor with dynamic focusing circuitry which ensures sharpness not only in the center but also in the edges and corners.

The monitor to meet your needs

All three PGS monitors are engineered for no-compromise performance to offer you a cleaner, sharper image than any other monitor in the same price class. The HX-12 and the SR-12 both feature uncompromising color convergence for crisp whites without color bleed. The MAX-12 offers impressive clarity in an amber phosphor monitor that runs off a standard monochrome card—no special card is required.

At PGS, our no-compromise approach includes all the details, too, from non-glare screen to a shielded cable—standard features on all PGS monitors, color or monochrome.

Call us at 800-221-1490

Compare your specifications to ours, listed below. Then call us at 800-221-1490 and we'll send you a fully detailed spec sheet plus everything else you need to know about all three no-compromise PGS monitors.

Don't compromise. Look to PGS for the image your eyes deserve.

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(609) 683-1660
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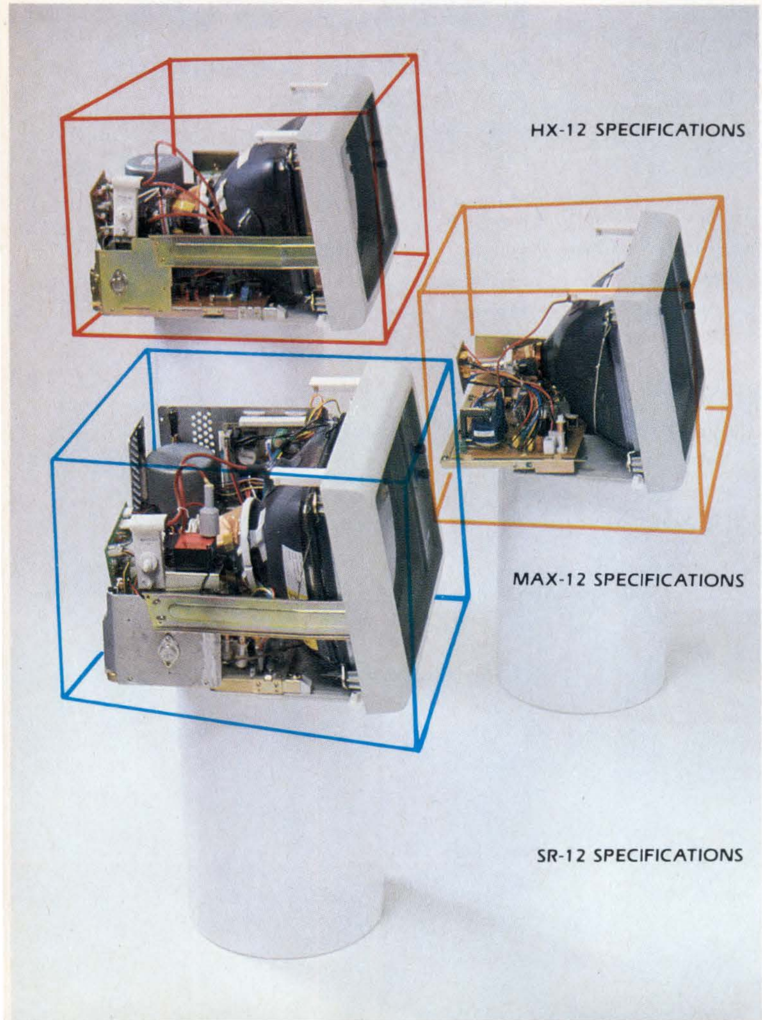
PGS delivers 3 no-compromise ways to improve your image



HX-12 SPECIFICATIONS

CRT	12" Diagonal, 76 degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface (NEC 320CGB22)
Input Signals	R, G, B, channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels
Video Bandwidth	15 MHz
Scan Frequencies	Horizontal: 15.75 KHz Vertical: 60 Hz
Display Size	215mm x 160mm
Resolution	Horizontal: 690 dots Vertical: 240 lines (non-interlaced) 480 lines (interlaced)
Misconvergence	Center: .6mm max Corner: 1.1mm max
Display Colors	16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels)
Characters	2000 characters (80 characters x 25 rows—8x8 dots)
Input Connector	9 Pin (DB9)—cable supplied to plug directly to IBM PC

MAX-12 SPECIFICATIONS

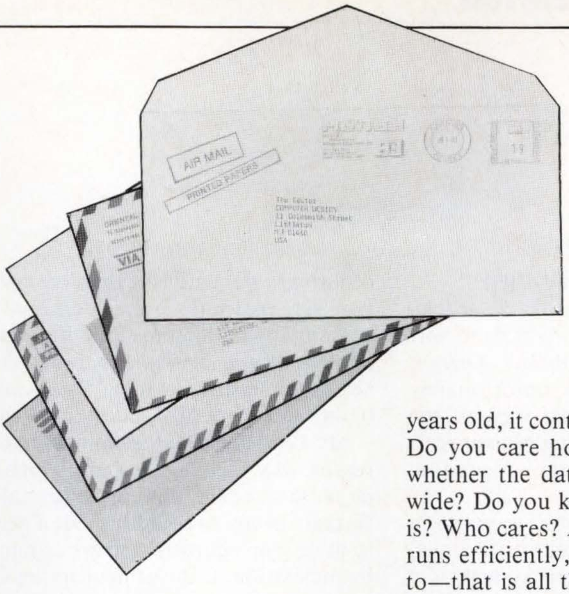
CRT	12" Diagonal, 90 Degree, non-glare surface (P 34 Phosphor)
Input Signals	Video signal, Horz Sync, Intensity—positive TTL levels, Vertical Sync—negative TTL levels
Video bandwidth	18 MHz
Scan frequencies	Horizontal: 18.432 KHz Vertical: 50 Hz
Display size	204mm x 135mm
Resolution	Horizontal: 900 dots Vertical: 350 lines
Input Connector	9 Pin (DB9)—cable supplied to plug directly to IBM PC

SR-12 SPECIFICATIONS

CRT	12" Diagonal, 90 Degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface
Input Signals	R, G, B channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels
Video bandwidth	25 MHz
Scan frequencies	Horizontal: 31.5 KHz Vertical: 60 Hz
Display size	215mm x 160mm
Resolution	Horizontal: 690 dots Vertical: 480 lines (non-interlaced)
Misconvergence	Center: .5mm max Corner: 1.0mm max
Display colors	16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels)
Characters	2000 characters (80 characters x 25 rows)
Input Connector	9 Pin (DB9)—cable supplied

CIRCLE 16

LETTERS TO THE EDITOR



Illiteracy as a ploy

I have enclosed a clipping from a show issue of the *Houston Business Journal*. It relates directly to the form of propaganda your recent editorial trounced. [The published item concerns a discussion of the Houston Computer Showcase Expo, part of which consists of "The New Literacy: An Introduction to Computers," developed as an accredited telecourse for the Public Broadcast System. This series of 25 half-hour segments was "produced by the Southern California Consortium and is an Annenberg/CPB project."]

I thoroughly agree with your premise [see the editorial, *Computer Design*, February 1984, p 11] that the "threat of computer illiteracy" is hogwash, and I think it actually ends up being a subversion of educational material, educators, and students for commercial purposes. PBS has been duped, colleges are being coerced (by those of alma mater colors blue or red), and we must give pity to a foundation such as Annenberg that has been so completely dumbfound that it spends over $1 million and two years to foist such propaganda on an even larger audience. Free college credit! Who wouldn't sign up? And, look who's "pushing" the product—an educator's journal? No. A "showcase expo" or traveling sideshow of computers and accessories. Something smells fishy. Who is the Southern California Consortium? They are not listed in the *Encyclopedia of Associations*. Maybe they are innocent, too—and short-sighted.

Even the Showcase Expo added an element of legitimacy to the proceedings by scheduling a presentation by a small computer college—one whose entire catalog consists of two one-hour presentations for buying a computer and for buying programs.

I'll stop right here and give credit where credit is due. The instructors from Decision Makers are good, very energetic, and know the product. If copious notes were taken the general audience of first-time system buyers would come away with some absolute gems of wisdom and advice well worth remembering. That's heavy stuff, and seems to contradict my point. In fact, however, it strengthens it. The first-time buyer needs Decision Makers and other professionals. The need is real and their service is valuable. But these decision makers should not exist.

Even today—with the adolescent pains and confusion—users should not accept a product that is misdirected, incomplete, and useless 85 percent of the time. (I will stake the gold on the moon that 99.44 percent of all "personal computers" are not used for personal or professionally productive activities during more than 6 hours of every week in a year.) The parents of this growing child have spent so much time traveling to the bank, they have forgotten that any growing thing needs careful monitoring and outside assistance and direction. If the "computer industry" is not being deliberately misdirected, it is lacking direction.

I read (or try to read) several publications that represent a fairly good vertical slice of the computer industry. This does not make me an expert. I own and use (maybe 4 hours a week) a personal business computer with dozens of programs. This does not make me an expert. I spend 20 to 30 hours a week working with computer systems (halls stacked with old printouts). This does not make me an expert. No one is.

I am an educated user, an angry buyer, and a frustrated keypuncher. I've had to learn how to type. I've spent hours learning what control codes are, had to dabble with assembly language to make a simple printer work, and taken time and money to find the perfect patches to my existing software—in order to use it. Why have I, and hundreds and thousands of others like me, done this? We are not masochists, though some may wonder. We've had no choice.

Does anyone who has a need for a programmable calculator spend hours and hundreds of dollars learning how calculators work, what language is used, what memory form is available, or how to "interface" it to other devices? No. It is a simple tool. It is bought as a tool, looked at and evaluated as a tool—nothing more, nothing less. Why is the "personal computer" different? Because someone says so? No. If your car is less than a few years old, it contains a computer of sorts. Do you care how it is programmed or whether the data bus is 4, 8, or 7 bits wide? Do you know what the clock rate is? Who cares? As long as the car starts, runs efficiently, and stops when I tell it to—that is all that matters.

Computer illiteracy is a threat, but to the computer industry, not society. Why? Because the buying public does not know enough to make an intelligent purchasing decision about today's systems. And if people are confused, they get frustrated and refuse to spend money. Therefore, "we must educate them." Is it a conspiracy? You be the judge, then yell and scream till someone starts listening. My screaming is at an end.

I leave you with a thought of what the personal computer should be. There is a device sitting on my desk that is, for all intents and purposes, a pretty black box. When queried, it comes back with a list of activity choices. I respond to a request for needed input in a manner that is convenient to me, not the machine—self-explanatory, courteous, and forgiving of errors. Output is quick and readable. Whether it is printed or displayed, my mind's eye finds the presentation clear and restful. At home, my wife (remember the computer illiterate?) needs a menu. She walks into the study, flips on the terminal/console/TTY/gadget, and the system asks "Who are you?" She responds with her name. It replies with a personalized set of activity choices from which she chooses No. 3 and tells it "peanut butter fudge," etc. Notice the personalized activities? I did not sit down with volume four, start at page 273 and create them several hours later. The salesman did it for me out of a master list at the store. Printer hookup? The salesman did that—and it works without any patches, even with my three-year-old Daisy from Holland. Do I care how many lines in the cable are used? Ask me. I dare you.

A. A. Iverson
ARCO Chemical Co
PO Box 777
Channelview, TX 77530

(continued on page 24)

(continued from page 23)

ACM considers standardization

Harvey J. Hindin's excellent article, "Graphics Standards Finally Start to Sort Themselves Out," (*Computer Design*, May 1984, pp 167-180) unfortunately promulgates an inaccurate view of the Association for Computing Machinery's (ACM's) current status regarding standards.

ACM has not voted to become a standards-making body such as the IEEE, much less adopt the Core system as a graphics standard. What ACM has done is recognize that there would be advantages to the industry if it were to adopt such a role, and has voted to look into becoming a standards-making body similar to the IEEE and a number of other professional societies. A firm decision has not yet been made and is dependent upon further debate and deliberation.

Even if ACM does decide to take on such a standards responsibility, there is no guarantee that it will take on the task of formally standardizing the Core system. I am sure that will require additional discussion, including some exacting consideration of the benefits to be achieved versus the costs (social and financial) to be borne before any action is taken.

My personal belief is that there is no reason why the Core system, which is a *de facto* standard, cannot be formalized further. Doing so could provide a benefit to those graphics users who are committed by inclination or investment to the Core system but does not mean that efforts on the Graphical Kernel System will be hindered. For the most part, I cannot understand the either/or aspects of this debate any more than I can understand other concepts that do not admit alternatives.

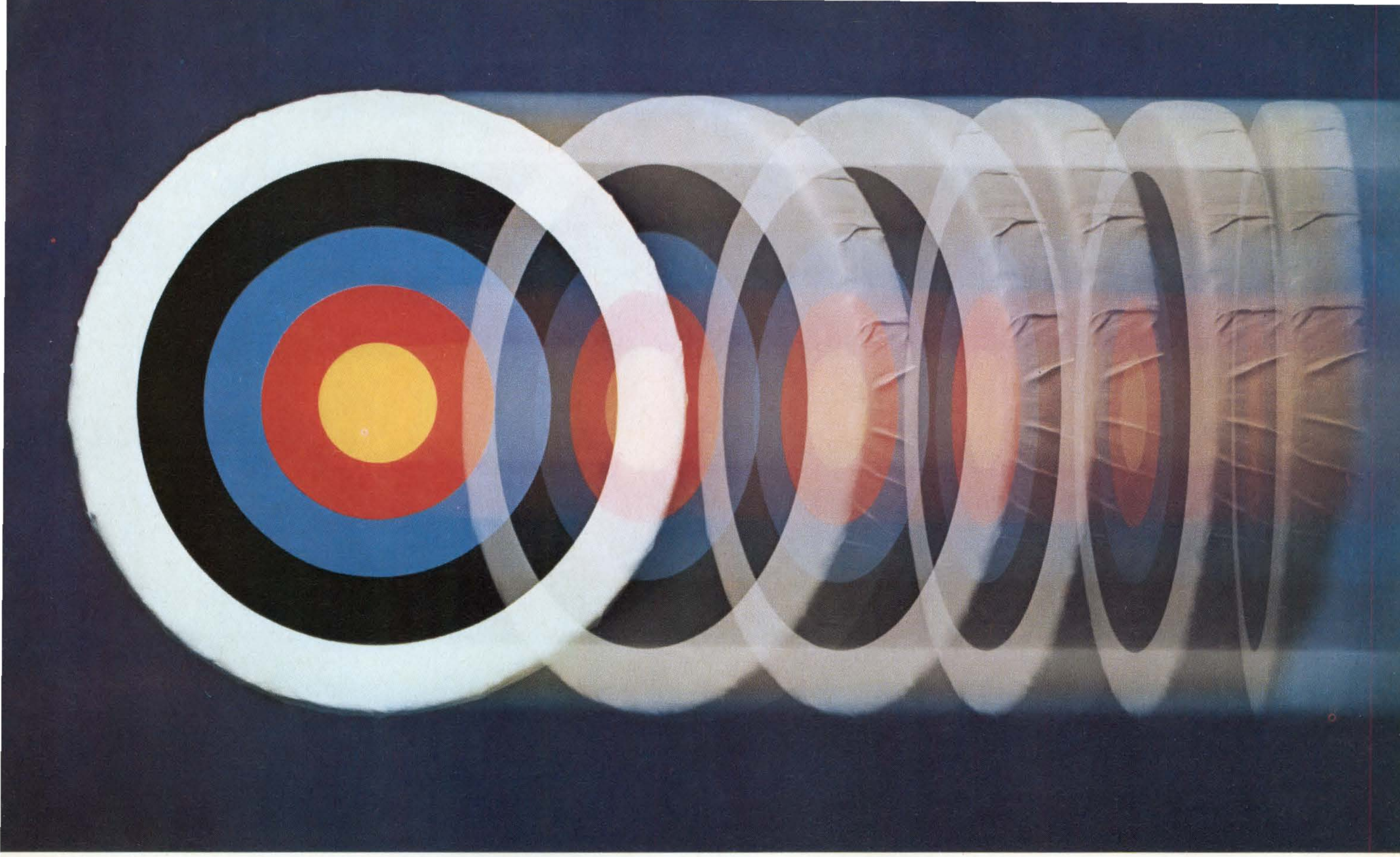
Jon A. Meads
Jon Meads and Associates
2516 NE 19
Portland, OR 97212

Multiple translations

The May 1984 article on "Disk Translation Software Solves Format Mismatches" (pp 123-128) failed to include our translation product, CROSSDATA. This product has been accepted by several OEMs for their IBM-compatible personal computers. These companies include Columbia, Corona, Compaq, Durango, Eagle, Monroe, Northstar, OSM, Panasonic, SEEQA, Sperry, Televideo, and Zenith.

With CROSSDATA, you can convert data/text file formats from CP/M to MS/PC-DOS and back again on any IBM or comparable computer. CROSSDATA is a self-contained program and does not require any additional hardware or software to run. CROSSDATA runs under MS/PC-DOS 2.0 or 2.1.

Rene Vishney
Award Software, Inc
236 N Santa Cruz Ave
Los Gatos, CA 95030



The Strategic Supplier Is Armed With More Than Past Experience To Respond To Future Needs.

Evolving product requirements are a moving target in a changing marketplace. Material innovations for creative designs must be based on the commitment of time and effort to get to know an industry inside out. Because, in the final analysis, thorough research and innovative thinking are the bottom-line chemistry of advanced technology.

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CIRCLE 18

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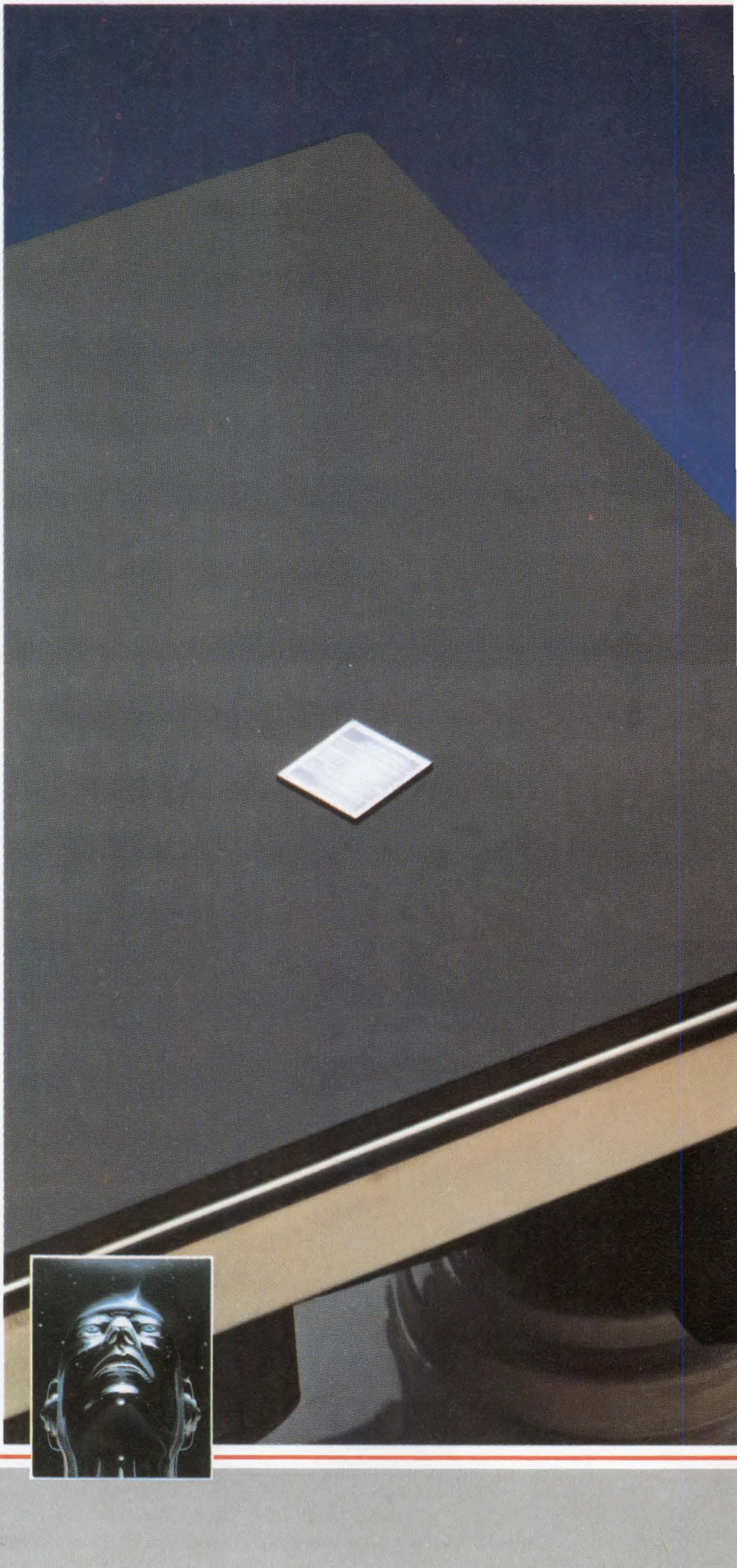
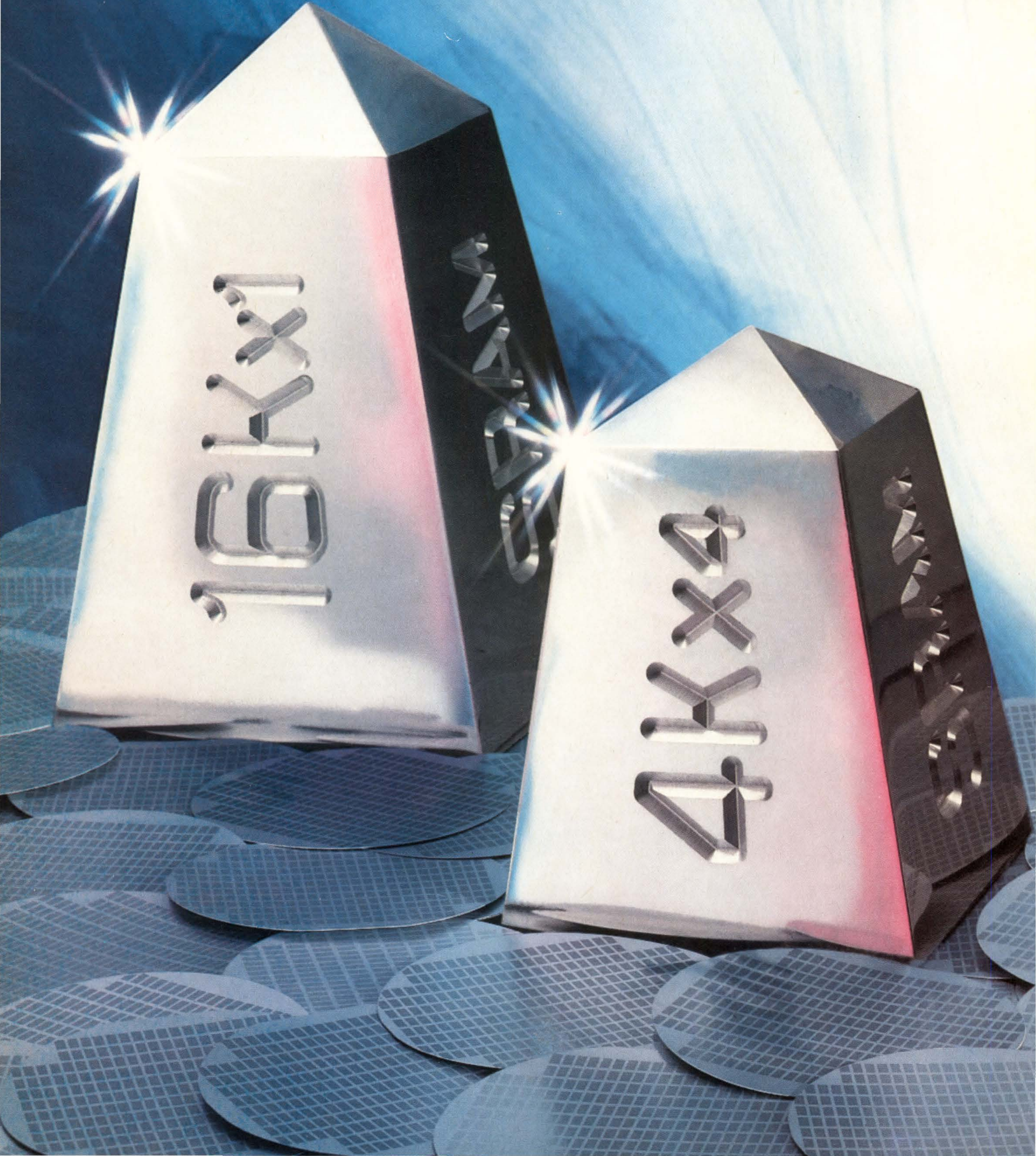
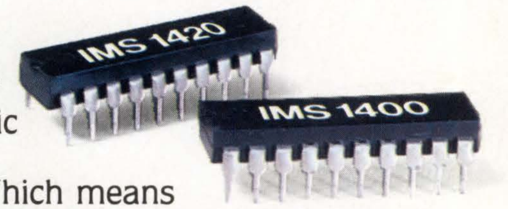


In 16K static RAMs, INMOS choices...starting



means high-performance with 35ns access times



When you're looking for top memory performance in your system, look to today's leading supplier of high-speed static RAMs...INMOS. Because INMOS gives you a choice of speeds, organizations, power dissipation and packaging. Which means you can optimize your designs, without compromising on cost or performance.

High speed. The INMOS family of fast static RAMs deliver access times of 35, 45, and 55ns. Perfect for high-performance tasks such as buffer memories, graphics, and main-store memory. And they give you a low-cost alternative to expensive 35ns ECL parts. Choose our by-1 organization for deep memory. Or the by-4, which also offers versions with 30 and 40ns chip-select access times, for writeable control store and cache memory. Most versions are available in plastic DIPs, ceramic DIPs, and chip carriers.

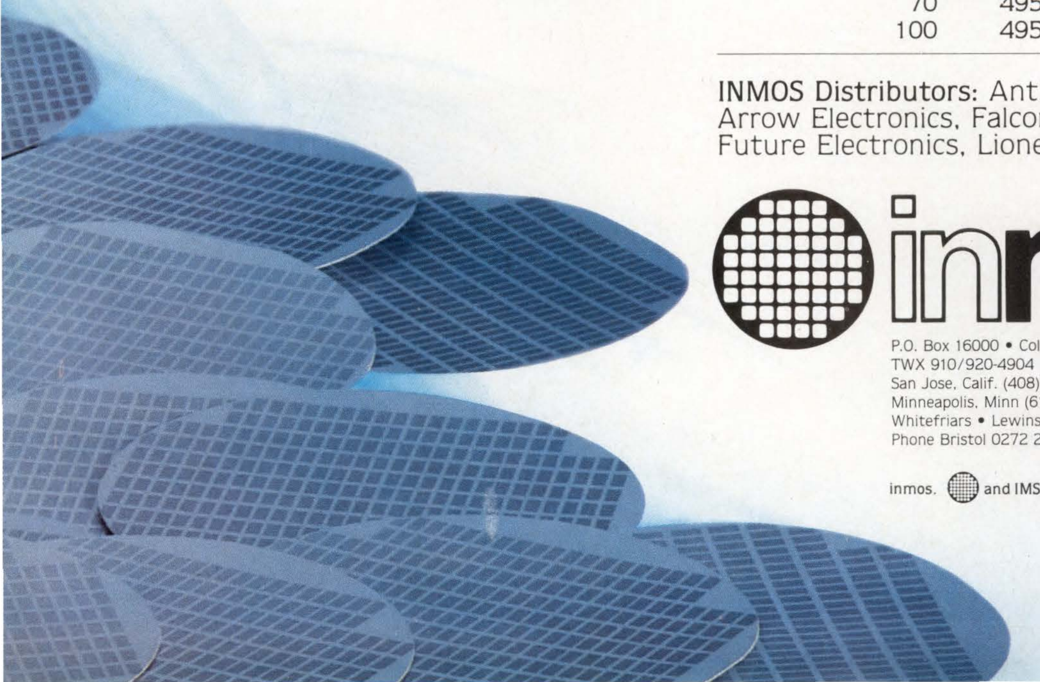
Low power. For high performance combined with low power, INMOS offers plastic packaged SRAMs with 70 and 100ns chip-enable access times in by-1 and by-4 organizations. Both have maximum power dissipation of 495 mW active, 83 mW standby. The by-4 organization is also a better alternative to 2Kx8 SRAMs in many high-speed applications. Best of all, they're both low cost. Here's your answer for fast systems that are power critical and price conscious.

Military versions. When you need fast RAMs you can trust in hostile environments, INMOS can supply 55 and 70ns parts with specs guaranteed over the full military temperature range of -55°C to 125°C. These parts, available in side-brazed ceramic DIPs, chip carriers, and flat-paks, conform to MIL-STD 883B processing, including screening to class B Method 5004 and quality conformance to Method 5005.

Check the chart. With all these choices, its easy to see why INMOS is the leading high-speed RAM supplier. Look for the part you need, then call an INMOS distributor for complete details.

Organization	Speed (ns)	Power (mW) Active	Power (mW) Standby	Part No.
16Kx1	35	660	110	IMS1400-35
	45	660	110	IMS1400-45
	55	660	110	IMS1400-55
	70	495	83	IMS1400-70L
	100	495	83	IMS1400-10L
4Kx4	45	605	165	IMS1420-45
	55	605	165	IMS1420-55
	70	495	83	IMS1420-70L
	100	495	83	IMS1420-10L

INMOS Distributors: Anthem Electronics, Arrow Electronics, Falcon Electronics, Future Electronics, Lionex Corp.



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CIRCLE 20

WE'VE BEEN OVER THIS A MILLION TIMES.

And all that repetition led to another breakthrough — the first E²ROM with million cycle endurance.

Thanks to our proprietary Q-Cell™ technology, every byte of every 5516A can be written at least a million times. In current designs, that makes write failures about as common as carbon paper at Xerox headquarters.

And if you check the features — 8-bit by 2K organization, 200ns read time, on-board latches and timers, 5V power, and inherent non-volatility — you'll realize the 5516A even competes with bulky CMOS-battery back-up combinations in selected applications. The first E² ever to be a contender for static RAM designs.

But we knew all along the 5516A would make history. It's happened before.

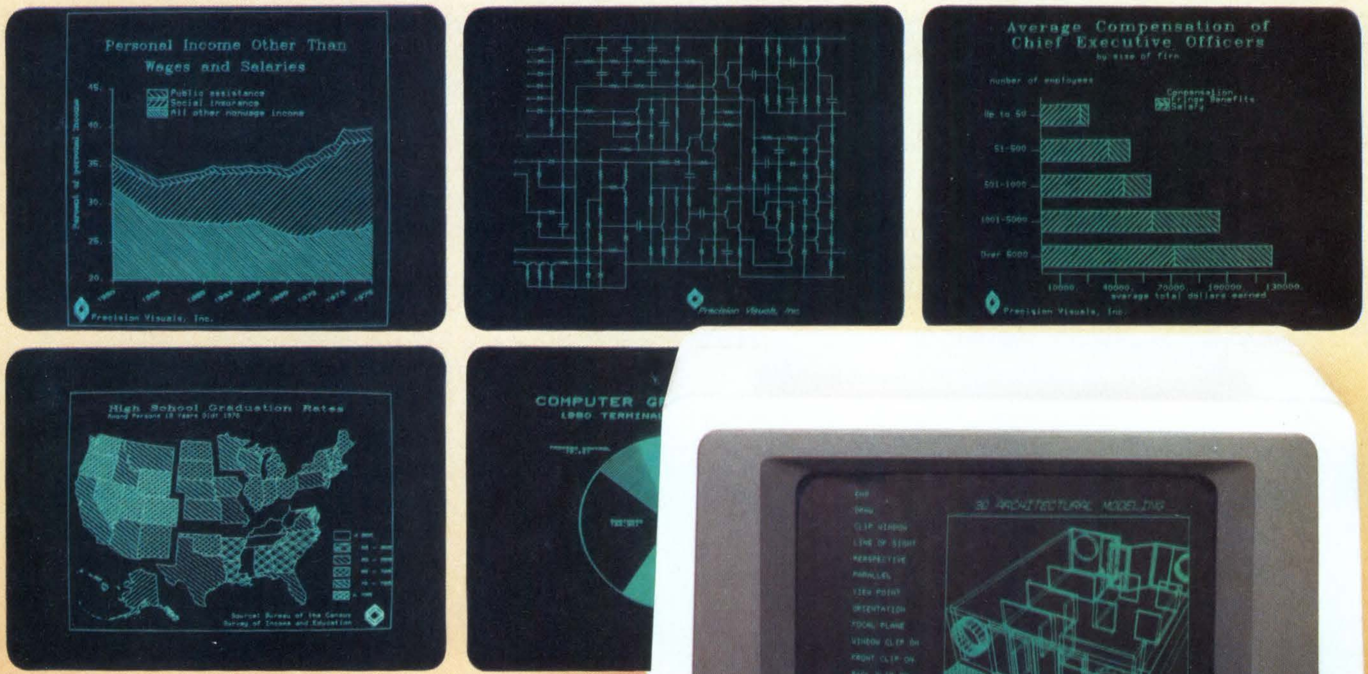
When we introduced the world's first 5V E². The first 64K. The fastest-ever byte-write time, 1msec. The original Silicon Signature.™ Our exclusive DiTrace.™

And now, unique Q-Cell technology in an E² you can write over and over again.

This time, we're making history by repeating ourselves.

For more information on the world's most enduring, full-featured E²ROM call us at (408) 942-1990, or write Seeq Technology, 1849 Fortune Drive, San Jose, California 95131. Or circle number 11 on reader service card.

High resolution, low cost graphics should be more than a retrothought.



Why settle for a low resolution retrofit graphics terminal when you can have a VISUAL high resolution terminal with quality and reliability built in. And at a cost that makes retrofits overpriced.

The VISUAL 500 and VISUAL 550 emulate the Tektronix® 4010/4014 but cost only about half as much. And they provide 585(V) x 768(H) resolution for sharp text and graphic display on a large 14″ screen without the need to add boards or change the CRT. This superior resolution offers the ideal vertical to horizontal dot density ratio of 1:1 for balanced images and reduces the "stairstep" effect you get with most retrothoughts.

The VISUAL 500 provides selectable emulations of the DEC VT52®, Data General D200, Lear Siegler ADM3A,™ and Hazeltine 1500 terminals. The VISUAL 550 is DEC VT100® protocol-compatible as well as a character or block mode terminal which complies to the ANSI X3.64 standard.

Call or write for a free comprehensive reference booklet on graphics terminals including a glossary of graphics buzzwords.

VISUAL See for yourself

Visual Technology Incorporated
540 Main Street, Tewksbury, MA 01876
Telephone (617) 851-5000. Telex 951-539

VISUAL 500/550

	VISUAL		RETROTHOUGHTS						
			DIGITAL ENGINEERING				SELANAR		
	500	**550**	VT640S	VT640	DQ650S	DQ650M	SG100 PLUS	SG200	SG480
Vertical Resolution	**585**	**585**	240	480	240	480	240	240	480
Horizontal Resolution	**768**	**768**	640	640	800	800	1225	1225	780
Dot Density Ratio	**1:1**	**1:1**	1:2	1:1	1:3	1:1	1:4	1:4	1:1
Screen Size	**14″**	**14″**	12″	12″	12″	12″	12″	12″	12″
Tektronix 4014 Compatible	**STD**	**STD**	NO	NO	NO	STD	NO	STD	STD
Data Tablet Support	**STD**	**STD**	NO	NO	OPT	OPT	NO	NO	NO
Multi-Vendor Printer Support	**STD**	**STD**	OPT	OPT	OPT	OPT	OPT	OPT	OPT
8 Dir. Cross Hair Cursor	**STD**	**STD**	NO	NO	NO	NO	OPT	OPT	OPT
Programmable Function Keys	**STD**	**STD**	NO	NO	NO	NO	NO	NO	NO
Tilt/Swivel Enclosure	**STD**	**STD**	NO	NO	NO	NO	NO	NO	NO
Compatibility	**VT52** **ADM3A** **H1500** **D200**	**VT100** **VT52** **ANSI** **X3.64**	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52
PRICE (suggested list*)	**$2,495**	**2,695**	3,025	3,355	3,025	3,510	2,890	3,390	3,190

*Retrothoughts price includes DEC VT100® terminal based on published information as of 4/1/83.

CIRCLE 21

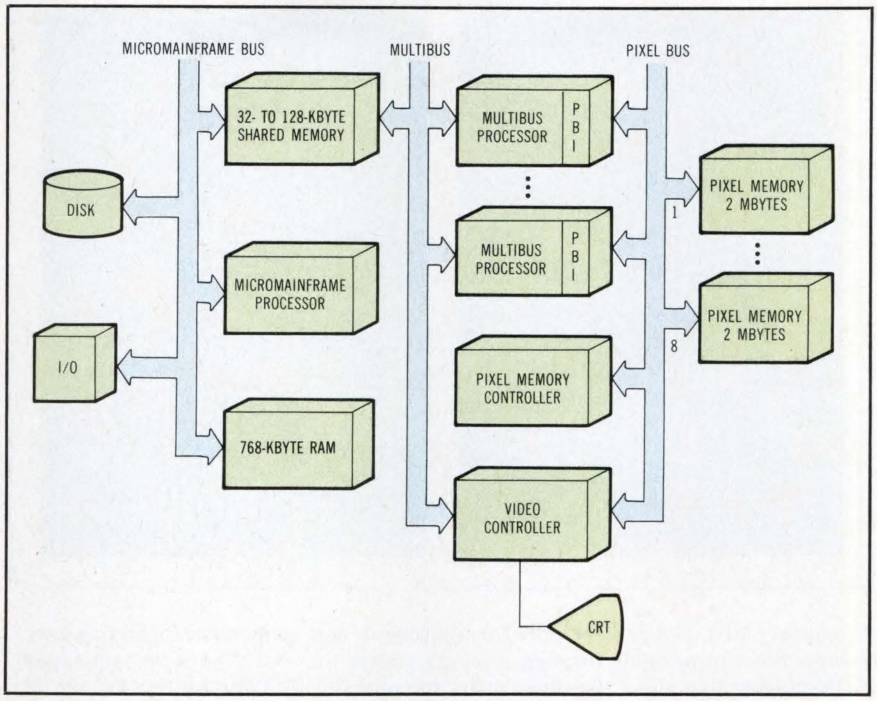
Interactive three-dimensional graphics: more than a pipe dream

Imagine two three-dimensional views of a piping system displayed in color on a video screen. Imagine locating a specific valve that should fit into an opening in one branch of the system. Now, imagine being able to rotate that valve and observe the rotation in both views.

Until recently, this feat was possible only in the mind's eye. Now, however, Cadtrak (823 Kifer Rd, Sunnyvale, CA 94086) has developed a workstation that brings the imaginary to reality. The DS-1's architectural design is organized around a bit-addressable pixel memory. This memory holds images with different numbers of colors and presents them to the video monitor via a microcoded frame instruction set resident in the memory itself. This unique design allows smooth virtual panning and zooming at the 60-Hz video refresh rate.

Unlike the conventional double-frame buffering technique used on current raster graphics systems, DS-1 uses a closely coupled multiprocessor architecture that implements parallel data transfers to achieve a design that is totally independent of vector density. The multiple bus structure allows a high degree of asynchronous operation, and a hardware implemented state-machine decodes instruction on how to compose a video frame.

Closely linked to this tightly coupled hardware configuration is the company's GOS software graphics standard. (For a discussion of graphics standards, see *Computer Design,* May 1984, p 167). The result is that the user can manipulate a three-dimensional object in a complex model at interactive speeds.



The DS-1 workstation performs pipelining operations beginning in the micromainframe processor and continuing in the Multibus processors. Any of the Multibus processors can read/write pixel data or control information into pixel memory. The video controller converts pixel memory information into RGB intensities.

Piping system uses multiple images

Development of this workstation began in 1981 when company founder Joseph Sukonick sought an application for his technique. "We wanted to find an application that would use smooth panning for easy viewing, and where multiple 3-D images could be simultaneously manipulated in 1/60th of a second," says Dr Charles H. Wells, vice president of business development. "Piping system design was the perfect choice."

The architectural design born of this patented technology is the DS-1, whose 64-bit wide pixel bus transfers information between the parallel processors and the pixel memory at 8 MHz. The video board pulls data from the pixel memory, computes the value of the RGB addresses in the color map, then outputs RGB signal levels during the video scan.

The Multibus provides a means to support parallel processors and possible future enhancements such as array processors. Since the pixel address field is 32 bits wide, a total of 4 Gbits of pixel memory can be addressed. A hardware auto-incrementing address feature eliminates loading the higher word during sequential memory accesses. This allows each processor to move data to pixel memory at 400 Kbytes/s, and to clear memory at 1.6 Mbytes/s.

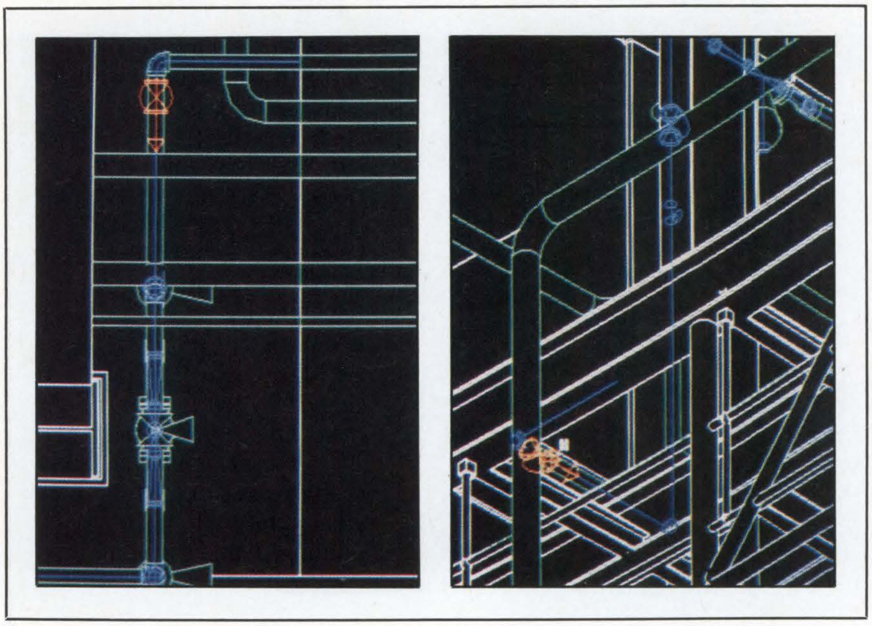
Each pixel board stores 2 Mbytes of RAM, and up to eight boards can be installed in the station's backplane. This provides 16 Mbytes of pixel storage using 64-Kbit DRAMs. This is equivalent to 13 raster images per board, each holding 660 x 480 x 4 pixels. The pixel memory controller contains a PROM, whose microcoded state-machine performs basic logic operations on pixel memory such as read, write, XOR, OR, and AND.

The pivotal hardware that allows accurate video frame composition is the video board, which converts pixel memory data into RGB signal levels for the color monitor. Composed of random logic devices, the video board implements hardware features that allow multiple viewport displays, over/underlayed grids, alternate grid colors when coincident with data, variable bit/pixel images, variable factor pixel replication, zooming replication blanking, smooth panning, and up to 256 colors.

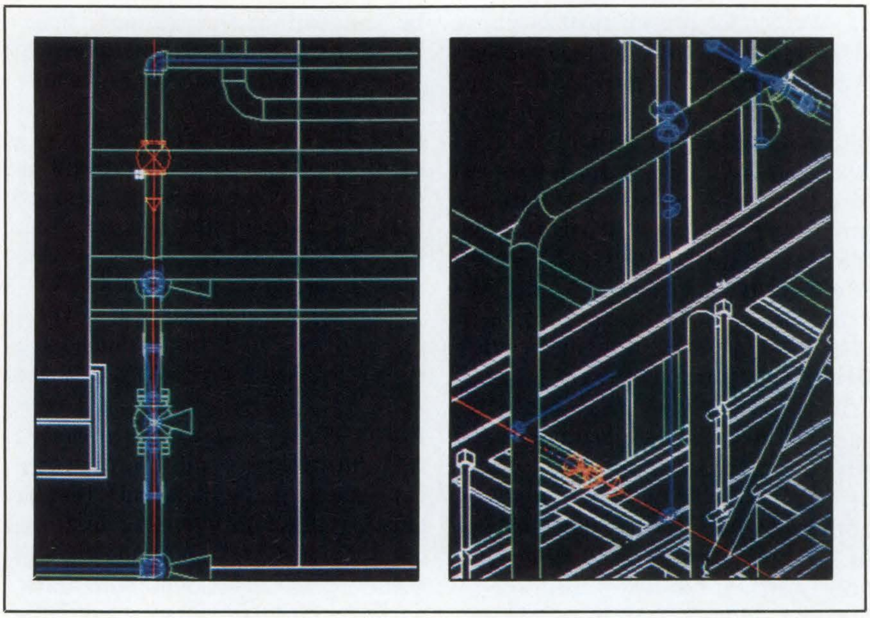
This flexibility is built into the architecture via the microcoded instructions that describe the construction of

(continued on page 34)

Three-dimensional graphics
(continued from page 33)



A sequence of GOS primitive calls for a piping design application illustrates how an operator can navigate through a piping system to "reach" a valve and rotate it. Displaying two views simultaneously, the operator visually locates the area of interest, then scales, windows, and displays the revealed views (top). The operator then points to the object of interest by displaying the attributes of a branch (bottom). The valve handle can then be rotated around the major axis of the pipe centerline. The data base is automatically updated with the valve's new position for all views.



each video frame. Because each frame (1/60th of a second) is described by a separate table of instructions written by any of the Multibus processors, smooth panning can be accomplished by merely rewriting the instructions for the next frame.

Blocks of pixel information representing instructions or pixel data are contiguously transferred to the video board on a first in, first out basis. This enables each viewport to contain differently structured images. Thus, one viewport can have a 1-bit/pixel image, while an adjacent viewport can have a 4-bit/pixel image.

The DS-1 was introduced in early 1983, and Prime Computer Inc (Natick, Mass) was quick to incorporate the hardware and piping application software into its own three-dimensional plant computer aided design (CAD) system. Before DS-1, Prime's system lacked an efficient graphics front end. So far, Prime is Cadtrak's only licensee, although Wells says other manufacturers in various fields are negotiating.

The DS-1 software was designed to make the workstation a self-contained, intelligent graphics computer. It provides the user with an arbitrary number of precomputed backdrop images of the data base. These images are generated on a host computer and downloaded to the workstation. With their hidden lines removed, these images are used as orientation aids, and to provide status of the host resident data base. The Pascal software is enhanced to support realtime multitasking.

Applications that require user interaction with a small number of objects in a data base at any one time are mapping, VLSI layout, and space management. Hitachi (Tokyo, Japan) is interested in DS-1 to help it investigate three-dimensional layout of VLSI chips. In such an application, at least two views are required to provide the user with sufficient visual cues to identify any point in three-dimensional space.

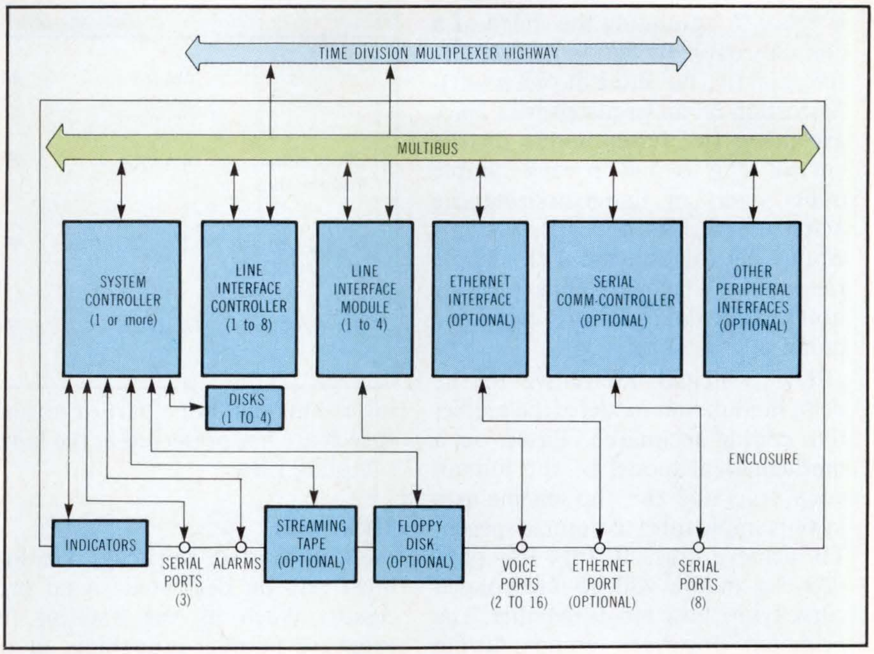
A key aspect in displaying multiple views is a 4 x 4 view definition matrix of floating point real numbers. This matrix describes the transformation for the three-dimensional space to a planar coordinate system, and is sufficient to project the image onto a backdrop view that is generated at any scale factor, position, or window. Typically, a three-dimensional application designer uses multiple views to position objects in space. For interactive piping applications, a four-view plan with the top representing North, elevation views looking South and West, and an isometric view is sufficient to visualize the problem in real time.

—Nicolas Mokhoff, Senior Editor

Speech compression brings voice messaging down to earth

By cutting speech sampling rates to one-half to one-fourth of the conventional 32 kbits/s, speech compression techniques move voice store and forward applications within reach of 16-bit microprocessors. The reduced sampling rate disk not only cuts storage requirements significantly and allows the original message to be reconstructed from less voice information, but also allows voice to be treated by the host processor as just another data type.

However, there is a catch. Compression to sample rates of 24 kbits/s can be readily accomplished by the use of well-known techniques that suppress pauses between spoken words. Beyond this point, however, compression techniques become more black magic and less scientific method, since popular mathematical models break down. As a result, significant degradation occurs in the quality of reconstructed speech. More of the original speech sample is thrown away.



The DSC-2000 Voiceserver implements a conventional Multibus system backplane for conventional data transfers and easy expansion, as well as a 32-channel time division multiplexing highway for voice processing.

A new generation

Exciting possibilities lie on the horizon if these barriers can be broken. For example, Digital Sound Corp (2030 Alameda Padre Serra, Santa Barbara, CA 93103) moves closer to integrated voice/text messaging with its DSC-2000 Voiceserver I store and forward system. Presently, it is configured to handle voice only, although its 68000-based general purpose processor and dual Texas Instruments TMS320 digital signal coprocessors can be programmed to handle text to speech conversion or text alone. Future plans call for incorporating limited speech recognition capabilities for commands and user access, as well as Unix support for private branch exchange (PBX) based networks.

Such high level integration is beyond the capabilities of current message store and forward systems. Typically, separate systems are needed for voice store and forward and for electronic mail. Common user interfaces tie the two together at the application level. For example, take Digital Equipment Corp's (Maynard, Mass) DECtalk II text to speech system and combine it with a voice messaging system from Voice Mail International.

Less ambitious efforts from Centigram Corp (1362 Borregos Ave, Sunnyvale, CA 94089) and Octel Communications Corp (1841 Zanker Ave, San Jose, CA 95112) have more in common with their mainframe counterparts than does the Digital Sound system. Their designs focus solely on voice store and forward, and make no provision for text to speech, speech recognition, or general purpose processing.

Yet, by employing such 16-bit microprocessors and single 5¼-in. rigid disk drives as Digital Sound, Voicememo (from Centigram), and Aspen (Octel) systems keep costs down to about half those of mainframe implementations offering the same functions. Dedicated voice processing logic and telephone interfaces free the microprocessor to handle system management. In contrast, mainframe implementations rely on the 32-bit processing power of the CPU to handle both system tasks and voice processing. Further complications arise from the need to treat voice information differently from conventional data types.

The other side of the coin

Still, microprocessor-based voice messaging systems tax the limits of speech technology. A problem develops because of contradictory goals. Low overall costs can be achieved only if microprocessors handle the same functions as mainframes. On the other hand, there must be significant digital signal processing to bring sample rates down to 16 kbits/s or less. This will allow microprocessors to process voice information as just another data type.

Unfortunately, there are no easy solutions. Mathematical models, which serve as the voice digitization/reconstruction foundation, fall apart when sample rates go outside their set thresholds. Due to the more general approximation of sampled speech, voice quality deteriorates as noise components are introduced.

Delta modulation, the model most favored by voice messaging systems, relies on high sample rates. It focuses on the changes in amplitude (voltage) and frequency between speech

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Speech compression
(continued from page 35)

samples (1 bit/s roughly represents one sample). In concept, this method is equal to estimating the shape of a complex curve by taking its first differential (ie, the slope at one point). Distortion increases as fewer samples are taken (ie, fewer points on the curve). This is due to each sample either over- or undershooting the actual curve. As a result, systems employing this scheme with sample rates that fall below 24 kbits/s, suffer noticeable degradation in voice quality.

The principal alternative to the delta modulation model is the predictive coding technique. Based on a mathematical model of the human vocal tract and ear, the scheme uses lower sample rates to digitize speech. To achieve this, it fills the gaps between samples with an interpolated curve tying those points together. The principal drawback comes during playback when the reconstructed voice comes out sounding "mechanical." This effect occurs because the inflections that are a part of normal speech are not preserved at the lower sampling rate.

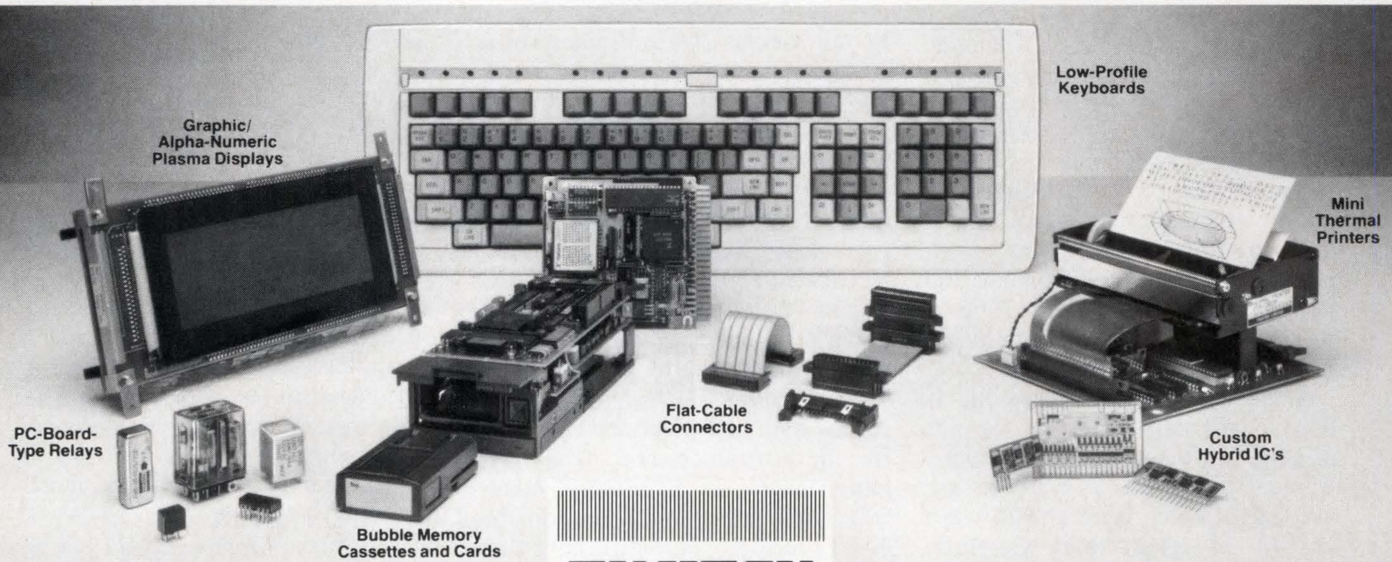
Comparison of Voice Messaging Systems

	No. of ports	Message storage hours	Sample rate	Sample method
Centigram Voicememo	4 to 14	6.2 to 34	15 kbits/s	Adaptive delta modulation
Digital Sound DSC-2000	2 to 16	8 to 32	9.6 kbits/s	Adaptive delta modulation
Octel Aspen	4 to 16	7 to 50	24 kbits/s	Delta modulation

Black magic

In uncharted territory, vendors must rely on dedicated signal processors (such as the TMS320) for extensive number crunching, or on proprietary algorithms that compensate for deficiencies in the mathematical models. At the heart of both approaches is the fact that the human ear can extrapolate the reconstructed speech and smooth over any gaps. Two examples are the ability to interpret the speech of someone with a heavy accent, and the ability to decipher conversation coming over a bad telephone line.

Based on heuristic (trial and error) algorithms gleaned from research involving thousands of hours of speech samples encompassing gender,



age, and accents, both Centigram and Digital Sound have developed proprietary speech algorithms that help the ear smooth over glitches generated by delta modulation techniques. Ron Cornell, vice president of engineering at Digital Sound, notes that even the human ear cannot resolve differences between frames of equal pitch (frequency). This is similar to the inability of the human eye to resolve differences between individual frames in a motion picture. In other words, sine wave signals that are out of phase with each other are indistinguishable from one another.

Reducing the rates

Using these techniques, Centigram reduces voice digitization to 15 kbits/s using only discrete logic components. Meanwhile, by using dual TMS320 digital signal processors, the DSC-2000 Voiceserver reduces sample rates even further to 9.6 kbits/s. This reduced rate allows voice to be transmitted over conventional data links. Octel's Aspen relies solely on pause suppression to achieve a digitization rate of only 24 kbits/s.

Low sample rates make it easier to use off-the-shelf microprocessors and system backplanes. Centigram dedicates an 8088 to handling system processing, while separate line interface cards handle voice processing and interfacing to an external PBX system. All reside on an IBM PC-compatible backplane.

Digital Sound follows a similar scheme with dual microprocessors: a 68000 to run application programs, and an 80186 to handle supervision of the dual TMS320 signal processors. Both processors, as well as line interface cards, reside on a Multibus backplane. In addition, a separate time division multiplex highway carries 32 separate channels of voice at 64 kbits/s. It runs between the line interface module, which physically connects to loop trunks or T1 digital carrier lines, and the line interface cards, which actually process the voice. This limits traffic across this Multibus to conventional data transfers. It also bypasses a potential bottleneck, since voice processing and application processing can occur concurrently.

All three systems use a single disk controller to store voice and data on a single rigid disk drive. Large sample sizes and redundancy characteristics of stored voice make error detection/correction much less important than data storage. Therefore, the error correction mechanisms can be disabled if disk controller software can identify stored voice and data with appropriate header information. Such flexibility extends further to allow data and voice to reside on separate tracks, or to be mixed so that voice samples are stored with any associated system data.

—Joseph Aseo, Field Editor

SYSTEM TECHNOLOGY
(continued on page 42)

High performance is Motorola's M68000

MASSCOMP chose the Motorola 68000 Family "because of its high performance and 'big machine' capabilities."

The very high performance of the MASSCOMP Work-Station-500 is achieved by distributing the system workload to subsystems supporting graphics, data communications and other complex operations. The CPU features a 10 MHz 68010 plus a 10 MHz 68000.

The MASSCOMP system also uses other 68000 processors for memory management, in its Array Processor, and in its Independent Graphics Processors.

"We chose Motorola because of its commitment to leadership in VLSI technology, and we're pleased Motorola has introduced the next generation of 68000 series devices."

Lorrin Gale, Vice President of Engineering, MASSCOMP

Alcyon chose Motorola because "It was obvious that the MC68000 would make a great UNIX* micro engine."

"The 68000's orthogonal instruction set, large virtual address space and rich addressing modes are particularly well suited to high level language and operating system development . . . The architectural benefits of the 68000, combined with considerable interest shown by third-party software houses in the 68000, made it a natural choice for Alcyon's family of high performance UNIX Operating System workstations. Alcyon's super micro computers achieve their high performance in part through use of MC68000 as both host and I/O processors."

William E. Kehret, Executive Vice President, Alcyon Corporation

Auragen Systems uses the MC68010 to provide its "customers with leading-edge technology."

"We believe power and price/performance come from utilizing as many processors as possible to solve a customer's problem. In our fault tolerant System 4000, separate 68010s provide executive, user, and communication functions. Our intelligent terminal uses its own 68008.

"Motorola's commitment to the 68000 product line has enabled us to concentrate our development effort on providing our customers with leading edge technology. We have already made the design changes needed to incorporate the 32-bit 68020 chip into the System 4000. No other family of compatible processors and support chips allows us to provide such power and ease of use to our customers."

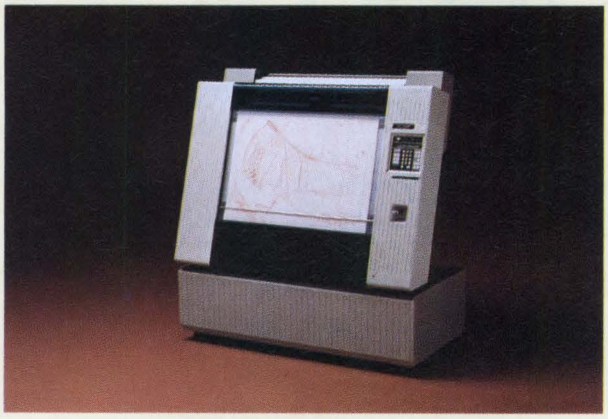
Samuel D. Glazer, System 4000 Architect, Auragen Systems Corp.

Cadmus chose the Motorola 68000 because it's today's performance leader.

"The MC68000 is the heart of our distributed main frame architecture. It's also used to control our bit-map, high resolution graphics display. Cadmus chose the 68000 family of products because the 68000 is today's performance leader in microprocessors and the UNIX* Operating System standard; because the 16MByte address range allows us to run extremely large processes; because the 68000 has become the standard for third-party 32-bit software and the standard microprocessor for running minicomputer applications; and, finally, because 68000 family plans convinced us of leadership through the '80s, and Motorola meets its commitments."

Bill Kiesewetter, Vice President of Marketing
Cadmus Computer Systems

what they all needed. Family is what they all chose.



CalComp chose the Motorola M68000 Family because its comprehensive built-in diagnostics reduce board count.

"In CalComp's newest line of vector plotters, Models 945, 965, 1073, 1075, and 1077, the M68000 was chosen because it makes the following features economically possible:

"Data Manipulation ... allowing incoming data to be tailored to the user's needs ...

"Interactive Control Panel ... the user is led through setups with English language-like statements and prompts ...

"Plotter Parameter Control ... so the user can optimize operation for the given media, pen, and ink.

"Maintainability ... the comprehensive built-in diagnostics continuously monitor plotter performance and quickly identify the source of any malfunction, reducing the mean time to repair to minutes in almost every instance."

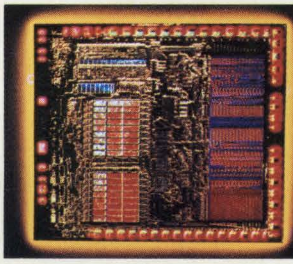
Dave Schlotterbeck, Vice President, Product Development, CalComp

Cadnetix chose the Motorola 68000 for its large linear address space and 32-bit performance.

"Our choice of the Motorola 68000 family for our CDX-5000 system was guided primarily by two requirements. First, the large data structures required for graphics data manipulation necessitated a large linear address space. The 68000 was the only commercially available microprocessor which offered this feature. Second, the ability to handle 32-bit calculations was also necessary."

"High performance cannot be stressed enough in describing our microprocessor needs. The CDX-5000 outperforms all comparably priced products and even compares favorably to superminicomputer products at less than half the cost."

Bruce Holland, President, CADNETIX Corporation



When high performance is what you need, the logical choice is the same one these fast-track companies made — the Motorola M68000 Family. The technology is here today for all the products you'll build for tomorrow.

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After all, ADSI is the major manufacturer of **SCSI**-compatible peripheral controllers. These high-performance controllers are designed to link the powerful industry standard Small Computer Systems Interface **(SCSI)** to the industry standards in disk and tape drives.

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1. 2. 3.

STREAMING TAPE CONTROLLERS

The **SCSI/QIC-36 STC** is the first controller designed specifically for use in a streaming environment. It links **SCSI** to the industry standard **QIC-36** basic streaming tape interface. ADSI has more controller experience with the **QIC-36** interface than anyone else in the world. Maybe that's why we've shipped more than anyone in the world. Data integrity is ensured by bus and buffer parity, 16-bit CRC and read-after-write data check. There is also complete **QIC-11** and **QIC-24** format support. And arbitration is standard. This advanced device was designed for use with basic ¼" streaming tape drives such as those from Archive, Wangtek and Cipher.

FIXED DISK CONTROLLERS

The **SCSI 55 FDC** product family links **SCSI** to the industry standard **"ST506"** 5¼" Winchester disk drive interface. Defective media management provides transparent in-line sparing and post-format block re-assignment with no performance degradation. Non-interleaved operation and arbitration are standard features of the **SCSI 55 FDC** line, producing maximum data throughput. Data integrity is ensured by a 32-bit ECC (transparent to the user) along with bus and buffer parity. The multi-threaded operation of the **SCSI 55 FDC** offers concurrent access to two physically separate disks, increasing I/O capability per second.

IBM PC DISK CONTROLLER

The **PC 5 FDC** links **IBM PC** to the industry standard **"ST506"** Winchester disk drive. This advanced device has exclusive LSI technology and a high performance, on-board microprocessor to provide emulation of the **IBM** controller, establishing full compatibility with **PC-DOS.** It has an **IBM PC** expansion form factor and supports two **ST506** Winchester disk drives. The **PC 5 FDC** has **IBM PC** I/O channel plug compatibility and an 8-bit ECC.

Also available from ADSI is the **IBM PC** Host Adapter which makes the **IBM PC** I/O channel compatible with **SCSI.** This host adapter is designed to provide OEM's with a non-intelligent host interface to yield the highest possible implementation flexibility.

Another standard—available at no extra cost from ADSI—is the unparalleled level of technical support and customer service. As the leading manufacturer of **SCSI**-compatible controllers, ADSI enters into full partnership with each customer. This means you receive support through your design and integration stages, right through your administrative support requirements and finally through your post-sale technical support needs.

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Setting the Standards in Peripheral Controllers

CIRCLE 25

Integrity reinstated in personal computer portability issue

With all the hoopla surrounding the issue of portability in personal computers, and with vendors claiming to have either a portable, transportable, knee-top, or lap computer, design engineers should find professional satisfaction in the fact that an experienced company has introduced the first notebook-sized computer containing more than empty pages. The Hewlett-Packard Personal Computer Group has designed an all-CMOS computer. It features 272 Kbytes of CMOS RAM; the MS-DOS operating system and two popular software programs (Lotus 1-2-3 and the HP MemoMaker) embedded in CMOS RAMs; a 300-baud modem; and a 16-line x 80-char LCD screen—all in a package weighing less than 9 lb (4.08 kg) and costing $2995.

Weighing only 9 lb (48.0 kg) and measuring 13 x 10 x 3 in. (33 x 25 x 8 cm), the portable HP 110 is an ideal battery-powered personal computer for travelers. All-CMOS technology has made this possible.

In addition, an 80C86 16-bit processor lets the HP 110 portable run at twice the processing speed of that in the IBM PC. With the Lotus 1-2-3 business software package, which includes a financial spreadsheet, graphics, and file management embedded in ROM, business users can obtain an instantaneous response to financial program operations. To top it off, battery life is good for up to two weeks of normal use before needing a recharge. Data preservation is guaranteed by the battery backup circuitry and monitoring system. This system alerts users when the charge is down to 20 percent, and locks out the keyboard when the battery reaches the 5 percent charge level.

System accoutrements

Too good to be true? Better than good, when IBM PC users find out that their machines can act like a dumb terminal by the Hewlett-Packard portable. This occurs when it dumps programs into any IBM PC peripheral such as a disk drive or printer via the HP-IL cable and a 5¼-in. disk-based program called HP LINK input into the IBM PC drive. Although the HP 110 lacks a disk drive, a peripheral 3½-in. disk drive can be purchased for $795. This drive provides an additional 710 Kbytes of data space on double-sided, double-density disks. The HP 9114 disk drive also operates off rechargeable batteries for an average of eight hours. Again, its size is no bigger than a three-ring binder (8 x 11½ x 3 in. or 20 x 29 x 8 cm).

Rounding out the peripheral units for the portable is the company's ThinkJet printer, a quiet ink-jet unit introduced last March, which is the same size as the disk drive, weighs 5½ lb and costs $495. In effect, users can purchase a full system for $4285. This compares favorably with the HP portable's nearest competitors (see Table 1).

Hewlett-Packard's Personal Computer Group (19447 Pruneridge Ave, Cupertino, CA 95014) meets this challenge by adhering very closely to the company's definition of PC portability—a fully functional, battery-operated computer weighing under 10 lb. To achieve this standard, program manager Steve Sakoman chose the Harris 80C86 processor and HP's own RAMs and ROMs, all in CMOS, to make up the bulk of the circuitry. Coupling these with an LCD that can yield 128 x 480 pixels, bit-mapped graphics, and using long-lived lead-acid D-cell batteries, brought the overall weight to 9 lb (4.08 kg), kept the size at 13 x 10 x 3 in. (33 x 25 x 8 cm), and the power below 1 W. This, then, is truly portable. (See *Computer Design*, Fall 1983, p 51.)

Truly portable computers are the fastest growing segment of the personal computer market, according to Dataquest, Inc, a San Jose, Calif market firm. Ken Lim, the firm's research analyst of small computers, forecasts that truly portable computer shipments will grow at a compound rate of 116.3 percent from 1983 to 1988 (see Table 2). On the other hand, transportable shipments are expected to grow more slowly during the same period (ie, at a compound rate of 39.7 percent). Lim defines true portables as meeting five basic criteria—ie, they have full-function, self-contained units; an independent power supply; a minimum display of 4 lines x 64 chars; mass storage; and full-sized keyboards.

(continued on page 44)

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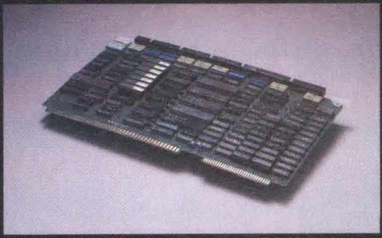

Wespergroup's new Multibest™ tape and disk controllers have the right stuff to successfully perform on Multibus systems. The Multibus MB-SMD disk controller is software compatible with the Intel iSBC 220 disk controller while supporting up to 2 megabyte/sec. disk transfer rate, 4 SMD type disk drives and improving throughput.

The Multibest MB-506/1000 disk controls up to three (3) ST506 or SA1000 disk drives and four (4) SA400 type floppy disk drives. The MB-506/1000 also supports mixed capacity drives and overlapped seeks.

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CIRCLE 26

Personal computer portability
(continued from page 42)

TABLE 1
Features and Prices of Leading Portable Personal Computers

Model	HP 110	Sharp PC-5000	The Gavilan	Compaq Portable*
Price	$2995	$1995	$3995	$2495
80x16 LCD	Standard	N/A	Standard	N/A (CRT)
16-hour Battery	Standard	No (6-hour)	No (8-hour)	N/A
Battery Gauge	Standard	N/A	N/A	N/A
256-Kbit RAM	Standard	$338	$1050	$320
384-Kbit ROM	Standard	N/A (192 Kbits)	N/A (48 Kbits)	N/A
Fast Mass Storage	Standard	$269	N/A (Disk)	N/A (Disk)
Modem	Standard	$349	Standard	$195
RS-232	Standard	Standard	Standard	$145
Built-in Software				
MS-DOS	Standard	Standard	Standard (Floppy)	Standard (Floppy)
Spreadsheet	Standard	$369	Capsule	$495
Word Processor	Standard	Included	Capsule	$175
Data Comm	Standard	Included	Capsule	$149
Personal Application Manager	Standard	N/A	Icon Driven	No
Total	$2995	$3320	$5045	$3974
Printer	$ 495	$ 395	$ 995	$ 495
Second Drive	$ 795	$ 999	$ 695	$ 525
System Price	$4285	$4714	$6735	$4994

*Compaq provides two extra function keys.
Prices are listed as of April 24, 1984.

According to Lim, the HP 110 has met, and exceeded, these criteria. The extra features include connectivity and data file compatibility to the HP 150, IBM PC and Compaq computers. Thus, files can be transferred between the portable and these machines via the HP LINK package. The LINK package costs $150 for connection to the HP 150, and $125 for use with the IBM PC or Compaq. Lim expects that companies such as Compaq and Kaypro will introduce truly portable computers compatible with the HP 110 within the next 18 months. He bases his optimistic forecast on a U.S. Bureau of Labor statistics report, that of the 19.2 million U.S. white collar professionals, 70 percent are highly or moderately mobile, with 5.1 million people spending less than 60 percent of their working day at a desk. These mobile professionals need truly portable computers. According its own study, Hewlett-Packard found that 44 percent of the business professionals surveyed said they plan to use their computers at multiple locations in the office, and 36 percent expect to carry their computers home at night or on weekends.

TABLE 2
Personal Computers $1000 to $5000 Category
Unit Worldwide Shipments
(in thousands)

	1981	1983	1988 (estimated)
Desktop Computers	837	3384	11,940
Transportable Computers	8	324	1725
Truly Portable Computers	0	118	5585
Total	845	3826	19,250

Source: Dataquest Inc, San Jose, Calif

Combining the advantages of desktop computing with those of portability has not escaped HP's marketing gurus. As such, the company promoted the HP 150 desktop computer introduced last year, by reducing the list price by $500, and offering Lotus 1-2-3 and the MemoMaker packages free with the purchase of an HP 150 by the first of this month. In addition, the company is offering a free HP 110 portable to their dealers if a combination of 15 portables and HP 150s are sold by Sept 1, 1984. These clever marketing overtures give credence to the opinion of some analysts who claim that Hewlett-Packard, while playing catch-up in the personal computer market, is becoming a very astute marketeer in its own right.

—Nicolas Mokhoff, Senior Editor

SYSTEM TECHNOLOGY
(continued on page 49)

At AMCC, metamorphosis means a lot more than just reducing board real estate, material cost and assembly time. AMCC metamorphosis transforms your designs from net lists to prototypes in as little as four weeks. It means a dramatic semicustom evolution using AMCC's system oriented logic arrays.

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	Q3500S	QH1500A	Q1500A	Q700	Q710	Q720
Equivalent Gates	3500	1700	1500	1000	500	250
Typ. Gate Delay (ns)	.3 – .7*	.9	.9	.9	.9	.9
Typ. Power (W)	3.5	2.8	2.5	2.0	1.2	.6
I/Os	120	120	84	76	56	36
Gate Utilization	95%	95%	95%	85%	85%	85%

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CIRCLE 27

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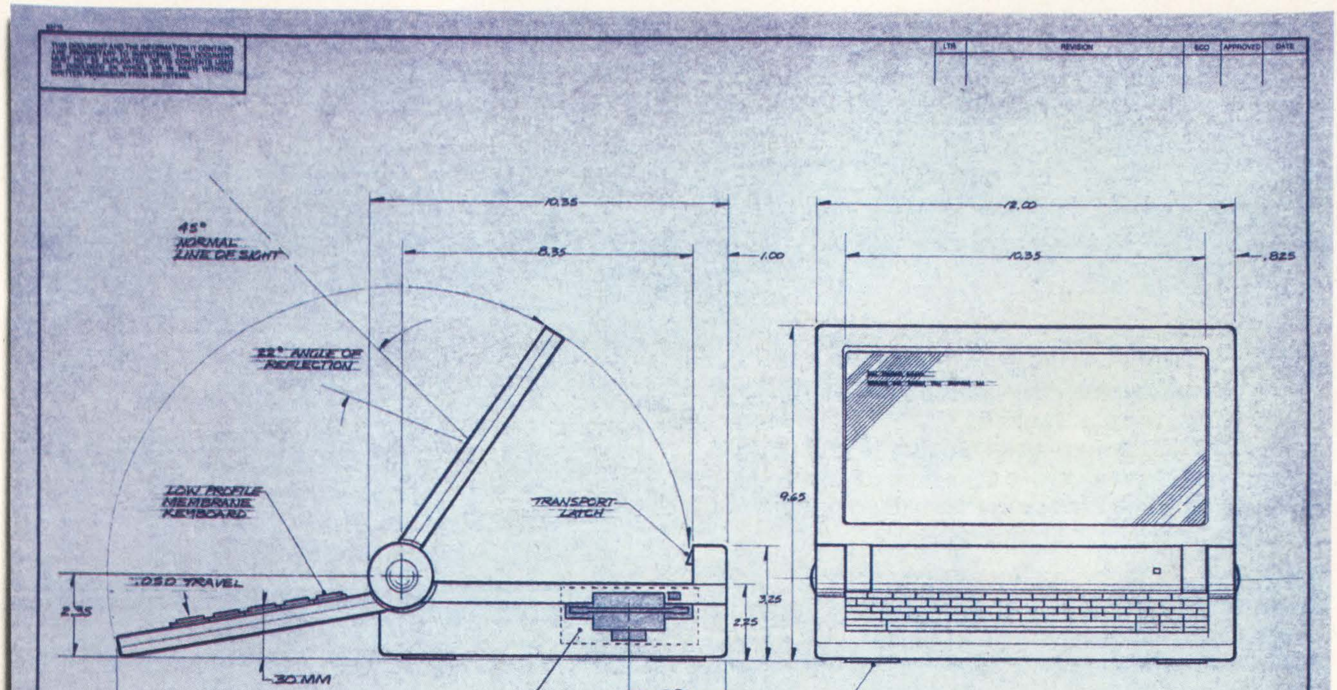

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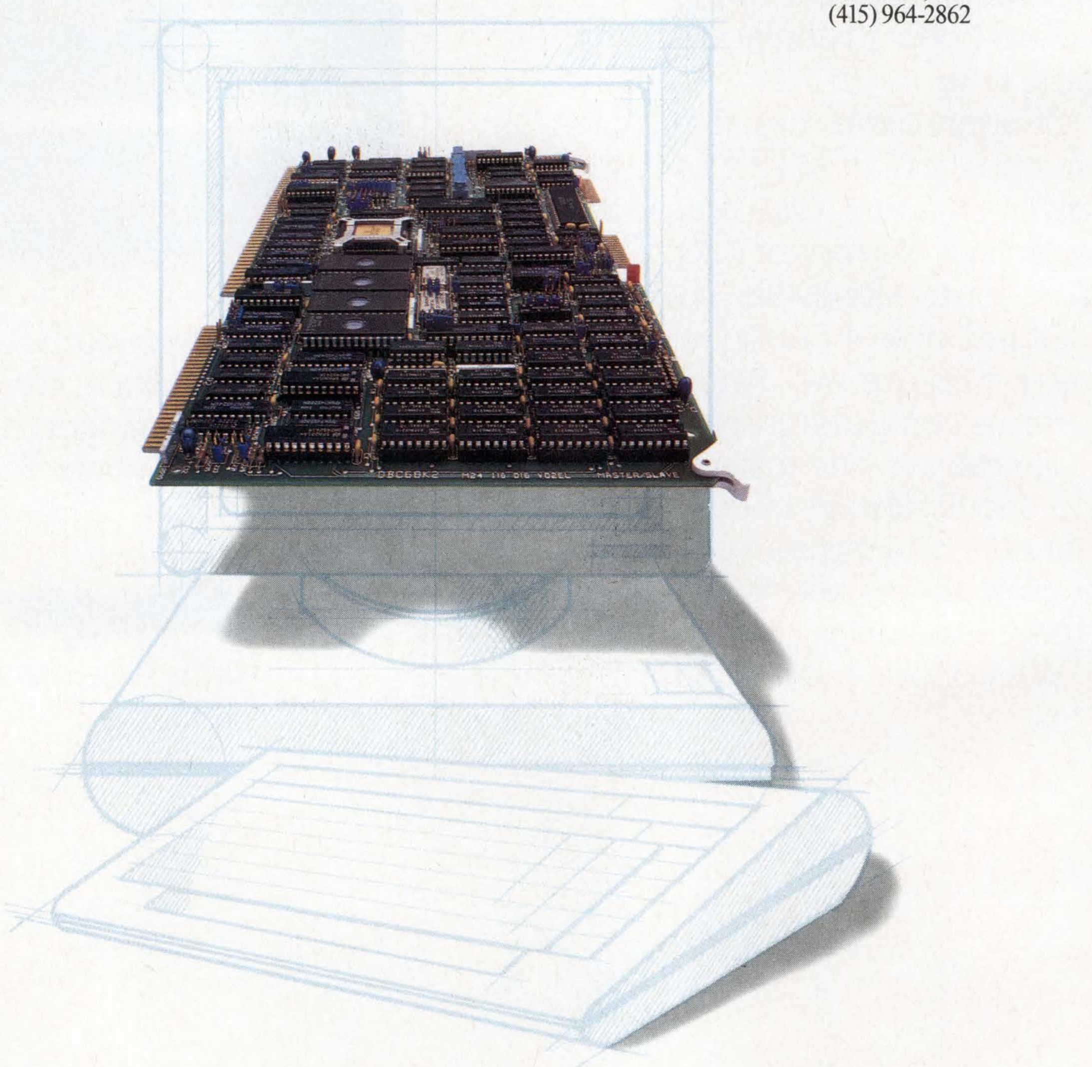

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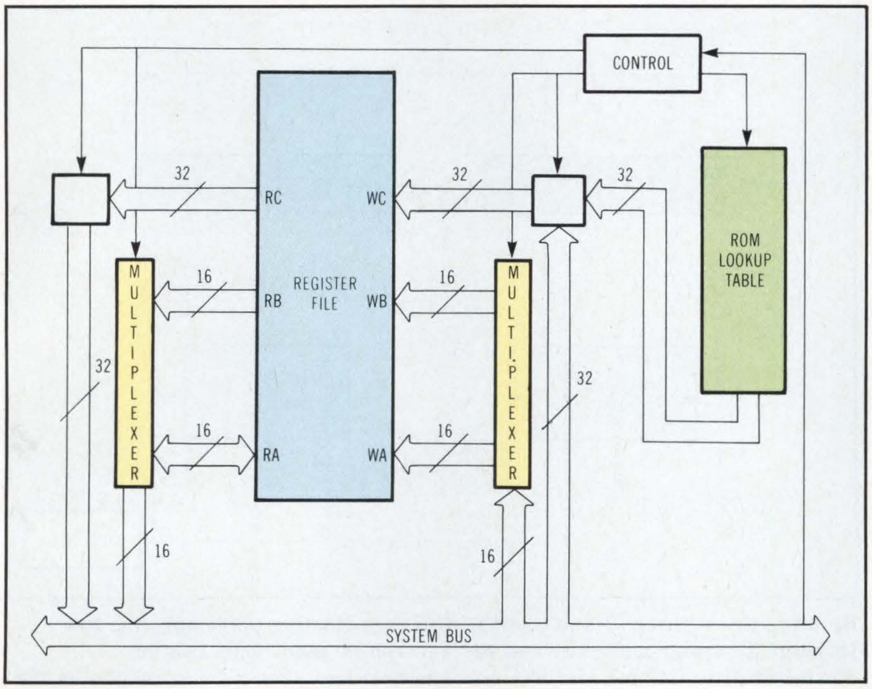
CIRCLE 29

Chips do 64-bit computations at 8 MFLOPS



The register file has three read and three write ports. In each case, two of the three ports are 16-bit, and the third is 32-bit. Using these ports, the package can accommodate 16-, 32-, and 64-bit data from a number of host computer buses.

Computer arithmetic has always been slow, expensive, or inaccurate. Recently, however, chip sets that provide maximum functionality in easily integrated packages have become available. These chips perform like expensive attached array processors and are capable of working with almost any computer bus, yet cost less than $1000.

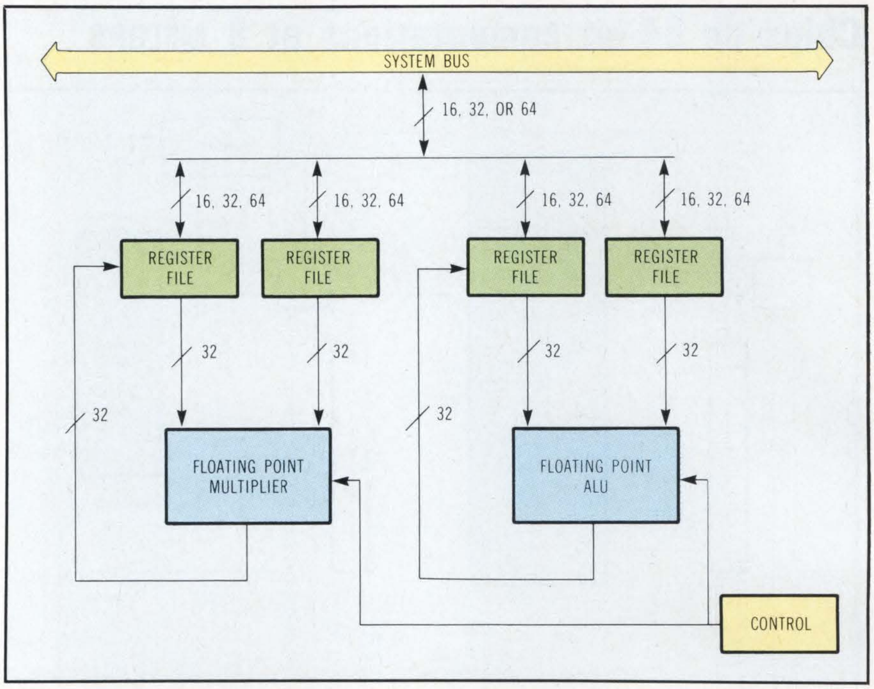
Taken together, the chip set portends the advanced VLSI subsystems that will appear over the next several years. Eventually, entire computer systems with RAM, ROM, and peripherals will be squeezed onto single chips. Standard functions, such as math, local area network (LAN) communications, and virtual memory, will appear as components, and the job of the system integrator will be simplified. Perhaps someday building a computer will be like making a cake, integrators will be able to choose designs and components as if they were ingredients.

One company that has addressed these arithmetic problems is Weitek (501 Mercury Dr, Sunnyvale, CA 94086) with three NMOS devices. WTL 1064, 1065, and 1066 chips, which together will cost between $600 and $1000, speed processing and increase accuracy. In addition, they will cost less than traditional attached array processors.

The 1066 high speed register file is basically a 32-bit by 32-register cache memory. It has onboard multiplexing to deal with 16-, 32-, or 64-bit data buses, and can perform a read/write operation every 60 ns. A ROM lookup table facilitates division and square root functions. Used in parallel, two of these units speed math operations by accepting 16- or 32-bit values from the host bus via DMA, and providing the floating point multiplier and ALU with 64-bit operands on demand, in effect acting like a pipeline to speed processing.

(continued on page 50)

Chips do 64-bit computations
(continued from page 49)



By using two register files in parallel with each floating point unit, the full speed of the 64-bit multiplier and the ALU can be used. Data can be down-loaded to the unit via DMA over the host bus, then used as needed by the math coprocessors.

By itself, the 1066 is useful in a number of applications. It is a natural extension of the Reduced Instruction Set Computer (RISC) machines built at the University of California at Berkeley, providing an external cache to supplement the large internal register set these machines use to speed subroutine calls. In concert with specialized processors or as an adjunct to a 16- or 32-bit CPU, it can act as an extremely fast first in/first out (FIFO) buffer, smoothing out data rate differences between fast CPUs and more leisurely main memory.

Together, the 1064, 64-bit IEEE floating point multiplier, and the 1065, 64-bit IEEE floating point ALU, provide full 32- and 64-bit floating point formats and operations, per the proposed IEEE 745 standard, version 10.0. They also provide full 32- and 64-bit Digital Equipment Corp F and D floating point formats and operations, as well as conversions between 32-bit, 2's complement integers and any specified floating point format.

Speeds vary according to the operation being performed. When they can be pipelined internally, addition, subtraction, conversions, and comparisons are performed once every 120 ns [8 million floating point operations/s (MFLOPS)]. Pipelined 32-bit multiplication occurs within 230 ns (4 MFLOPS), while 64-bit multiplication takes 480 ns (2 MFLOPS). In low latency flowthrough mode (single calculations input during the course of a program), the units operate at 1.3 to 1.9 MFLOPS. This is due to the time needed to load and store operands.

The floating point chips are provided in standard 144-pin grid array packages, and dissipate 2 W of power. In addition, both have single-phase, edge-triggered clocked interfaces, and fully registered, TTL-compatible I/O.

—*Sam Bassett, Field Editor*

August Preview
Special Report on Semiconductor Memories

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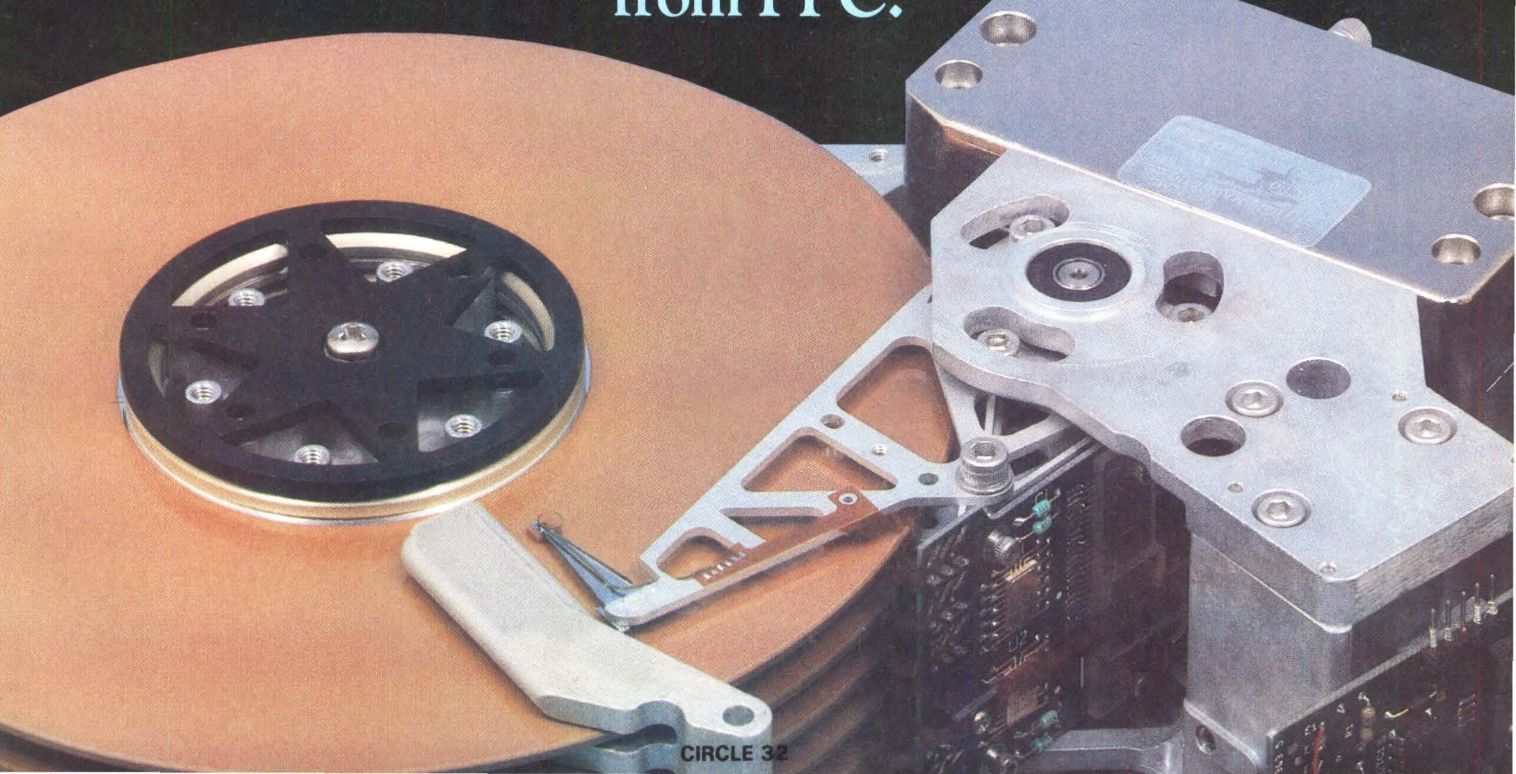
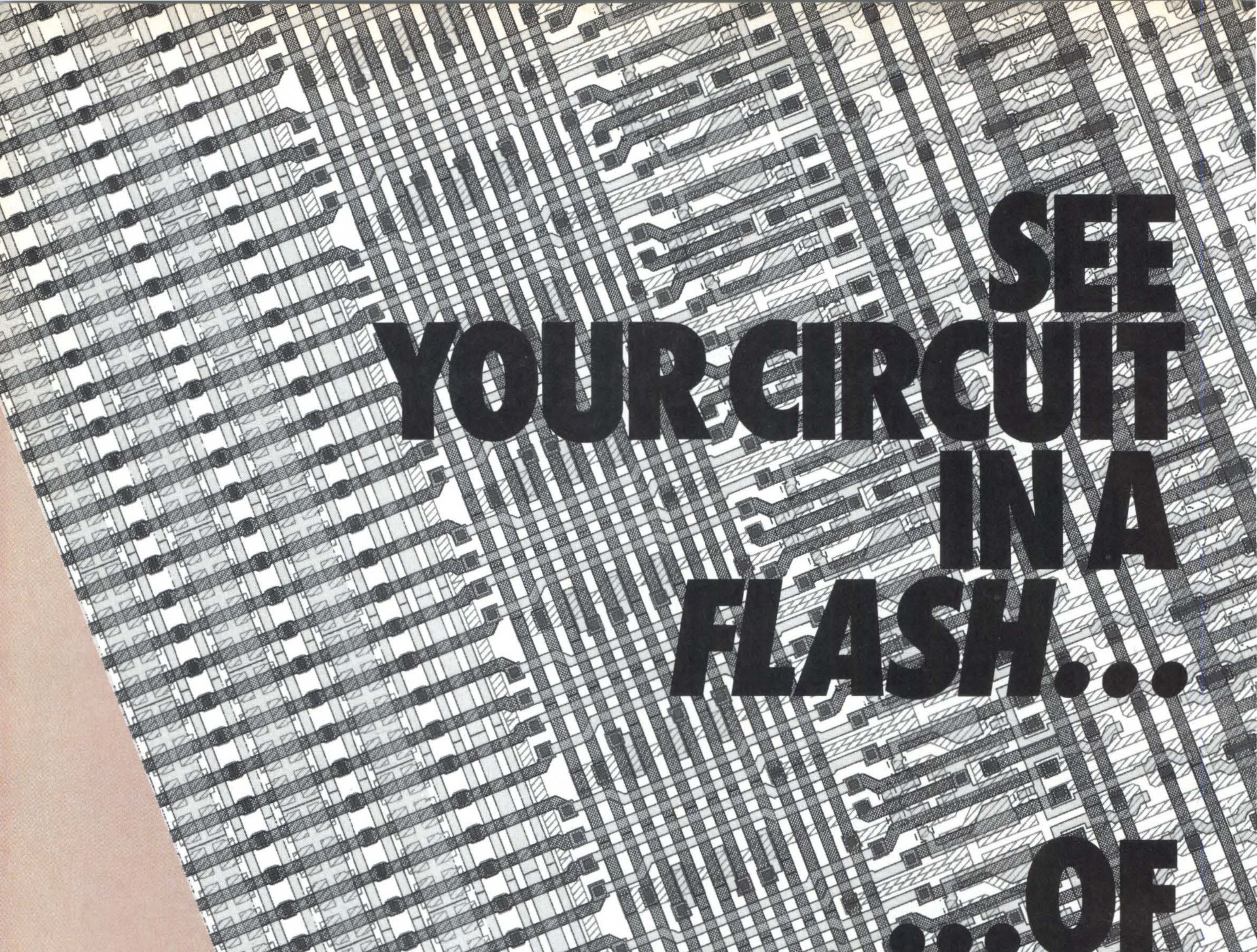


CIRCLE 32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FLASH...
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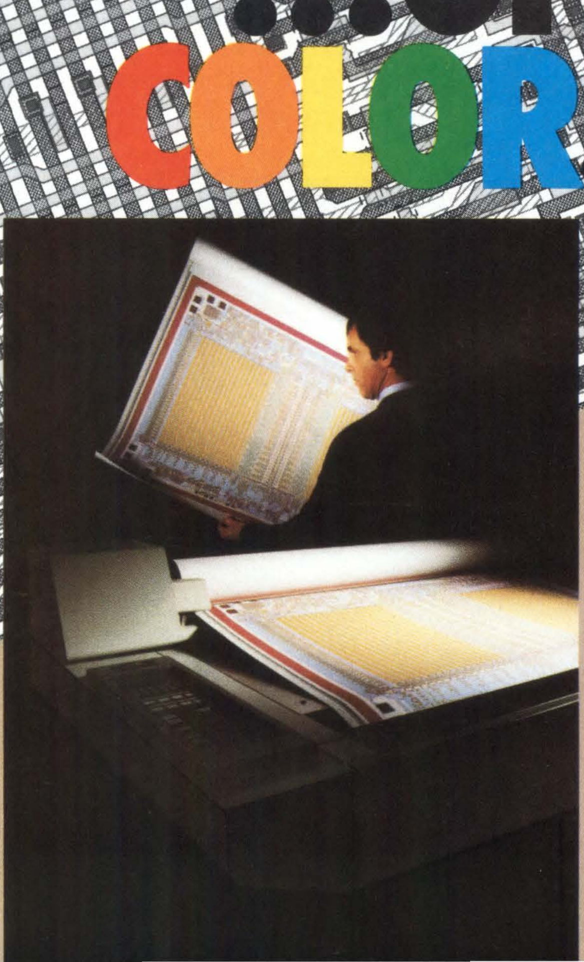
COLOR.



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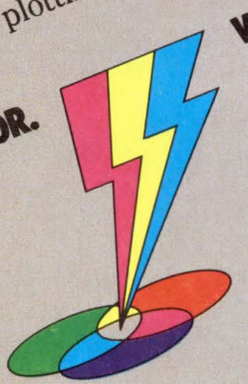

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See the Versatec color plotter at SIGGRAPH.

CIRCLE 33

Introducing the newest member of

The HP 1630G...65 channels and maximize 16-bit system

First came the HP 1630A and the HP 1630D. One, a low-cost general purpose logic analyzer suited to the needs of the full development cycle. The other, with 16 channels of timing analysis and 27 of state, an invaluable tool for the hardware design engineer. Now Hewlett-Packard introduces the HP 1630G. With up to 65 channels of state analysis, it is the new standard for software design engineers working on complex new 16-bit microprocessor-based products. Plus, the ability to configure 8 of those lines for 100 MHz timing analysis gives you a logic analyzer system with investigative power and versatility for virtually all your needs.

Three new software overview modes let you nonintrusively monitor software performance and hardware/software interactions in real time.

The HP 1630G significantly expands on the software performance capabilities already introduced in the HP 1630A/D family members. In addition to time histograms that show execution-time distribution, and label histograms that show address activity, the HP 1630G gives you three new modes: program flow, time positional, and linkage measurements. *Program flow measurement* lets you monitor program activity based strictly on opcode accesses. This can help resolve confusions which may occur when histogramming by address, especially if the program generates inline code or if memory blocks are interspersed between sections of the program. *Time positional measurement* lets you measure the number of occurrences of an event per unit time. Use this to better understand the behavior of your system under a time-varying load. *Linkage measurement* measures the relative frequency of the activity between specific software modules. You'll find this mode invaluable when you want to monitor the transfer activity between a main program and a series of subroutines, for example. Take advantage of all these software performance analysis modes to rapidly

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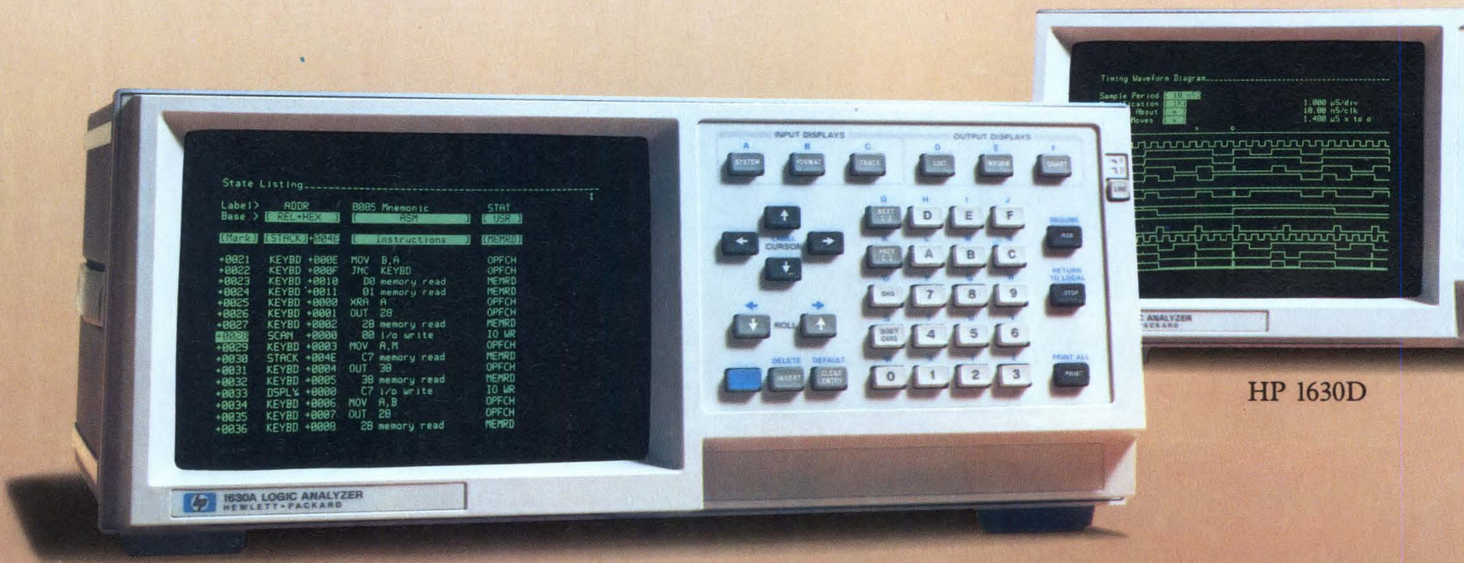

HP 1630D

HP 1630A

HP's logic analyzer family.

advanced software analysis help you performance.

discover if your system is resource-limited or if, for example, poorly chosen program segmentation is causing too much time-consuming disc-to-memory swapping.

Time tagging gives you added insights into system functions.

In the state analysis mode, time tagging measures the time elapsed between each stored state. Make detailed absolute time measurements between states and known physical events. Or, use the mode to measure the total time from the trigger point to a particular state. Because time tagging is a single-pass activity, it is well suited to helping you identify inline sections of code that take longer to execute than anticipated.

Floppy disc interface and popular 16-bit microprocessor support.

On-board non-volatile memory keeps one instrument setup and your current disassembler instantly available at power-up. For even greater storage, the HP 1630G features direct compatibility with a number of HP disc drives such as the HP 9121S/D (the HP 9121D is illustrated). In one convenient 3 1/2'' floppy you can now store data, state listings, timing diagrams, alternate disassemblers, and instrument setup configurations. For added flexibility, the HP 1630G supports all popular 8-bit, as well as the following 16-bit microprocessors: 68000, 8086, 8088, 80186, 80286, Z8001 and Z8002.

Our HP 1630G upgrade kit protects your previous HP investment.

If you've already invested in an HP 1630A or HP 1630D, but you feel you need the added capabilities of the HP 1630G, you'll be glad to know that an upgrade kit is available.

Compare the HP 1630G. At \$12,100* it's even HP-IB programmable for fully automated measurements. To find out more about the HP 1630G or its companions the HP 1630A/D, call your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

* U.S.A. list price only.

HP 1630G

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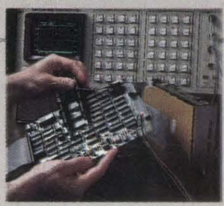
CIRCLE 34

There Are Only Two Thin
New Tested Pairs

The Testing.

OEMs face major problems trying to decide which hard disk drives to build into their microcomputer systems. What with the wide range of drives, and so many hidden costs associated with evaluation, testing and integration, the process becomes a time-consuming and costly hassle.

But there's a way out—from the company that's helped solve OEM disk controller integration problems more often and over a longer period of time than anybody in the business. That company is Xebec.



From standard-setting to vertical integration, from heavy investment in computer-aided design to the total commitment to the most automated manufacturing technologies, Xebec has demonstrated its leadership position in supplying microcomputer storage solutions.

Tested Pairs. The Guaranteed Match.

With its new tested pairs program, Xebec solves a major industry problem: post-delivery drive failure when interfaced to the controller. Having to do "after the fact" drive testing for many of our OEM customers, we have decided to offer a "before the fact" program. We'll guarantee quality and reliability by assuring a match between our zero defect controllers and a choice of drives in different capacities and form factors.

It's simple. Tell us which drives you're considering and we'll test them on Xebec-designed equipment against the most rigorous standards in the industry. Standards we at Xebec have set. Then we'll tell you which of our controllers is the best match for that drive—or we'll customize a controller for you—and accelerate your time to market.

The Edge In Controller Technology.

Xebec controllers are well known as the best in the industry. Their single-board designs incorporate MOS microprocessors and the latest standard cell and surface mount IC technology. Compatible with standard interfaces, our controllers have set the pace with sophisticated data separation, advanced error detection and correction, hard-fault isolation, a high-level

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s That Distinguish Xebec's
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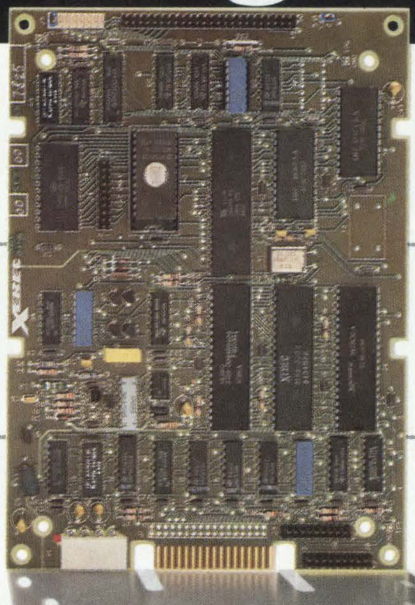
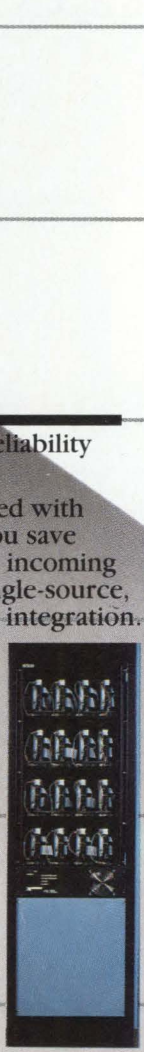


And The Pairing.

command set and other performance and reliability features.

Now these superior controllers can be paired with high-quality, Xebec-qualified drives. And you save time and money on evaluation engineering, incoming inspection, and service—while gaining a single-source, single purchase order solution to disk drive integration.

The Front Line Of Drive Testing.



We were recently asked to design and build a disk drive tester for one of the world's largest OEMs. We'll be using that tester to analyze disk drive performance for you. Full environmental testing, including shock and vibration. Full functional testing at elevated temperatures, with read/write tests at marginalized voltages. Careful calculation of hard and soft bit error rates. Complete checking of FCC and other agency emission standards. We'll make sure any drive meets its stated specifications and performance and quality claims.

How Xebec Does It. And Why.

Xebec can offer its tested pairs service to OEMs because of our commitment to quality. Zero defect quality symbolized by our "Xero D" signature and demonstrated by our superior computer-aided design, manufacturing and testing. Our talented people. Our experience. That's *how* we can provide high-quality products for prices no more than products that deliver a lot less.

Why offer our tested pairs? Why originate a new concept in quality? Enlightened self-interest. Because if we don't, someone else will. Frankly, we want to continue to enjoy the benefits of our leadership position as much as our customers do.

Call Xebec today. Pair up with one of our representatives to find out more about how Xebec tested pairs can benefit you.

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CIRCLE 35

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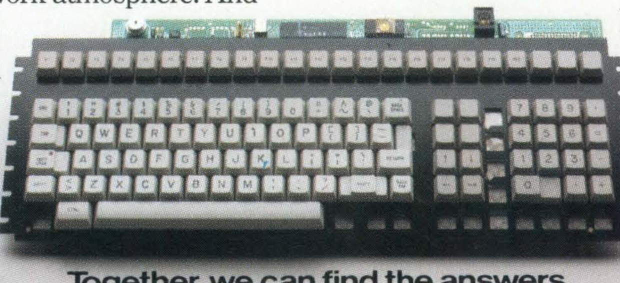
The response you need—and then some.

Over twenty years of keyboard experience has gone into the new Silent-Tactile keyboard design. This experience is combined with the expertise of our field and application engineers and expanded production facilities. So we can work with you to make sure you get the best keyboard for your application...in a standard or custom-tailored design.

Trying is believing.

Don't take our word for it. Sit down with a MICRO SWITCH Silent-Tactile keyboard and test it yourself. You'll see that it's as quiet, responsive and good-looking as we say. Maybe more so. A phone call is all it takes to arrange a demonstration. Simply call 815-235-6600. Or, write MICRO SWITCH, Freeport, IL 61032. Let us show you how good silence can feel.



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MICRO SWITCH
a Honeywell Division

To try this keyboard yourself visit our booth #C-3598 at NCC.

CIRCLE 36

GRAPHICS TECHNOLOGY SPURS ARCHITECTURAL DEVELOPMENT

System architectures change as computer graphics systems become more complex. Integrated graphics controllers, custom VLSI, and multiple microprocessors contribute to the design approaches required for different performance demands.

by John G. Torborg, Jr

Designers and other users of graphics systems are constantly forcing shifts in graphics architecture. From single-processor systems with little graphics memory, designs are now moving toward more complex multiple-processor architectures. These current systems include such features as bit-mapped displays and higher performance. In fact, today's best systems are already faster, have higher display resolutions, and perform more graphics functions locally than their predecessors of only a year ago. They also provide more colors and cost less.

For the past several years, one of the dominant graphics technologies has been raster scan. Because it is similar to that used in television, raster-scan technology has been comparatively well understood, and compatible monitors have been both available and affordable. Yet, as more and more designers switched to raster graphics because of the inherent advantages, they did not want to give up the advantages of their old systems. Raster scan offered color, low cost, and imaging capability. But, designers still wanted both high speed and interactivity.

A number of innovations, notably frame buffers and MOS microprocessors, helped decrease the dissatisfaction. Frame buffers, which consist of a large memory array and a video controller, provided some relief. Yet, they imposed serious system limitations on system performance. Even drawing a line required a significant amount of computer resources.

Incorporating MOS microprocessors into graphics controllers did enable execution of the same algorithms that were previously executed by the host

John G. Torborg, Jr is vice president of engineering at Raster Technologies, Inc, 9 Executive Park Dr, North Billerica, MA 01862. Mr Torborg is responsible for new product development and continuing engineering. He is a co-founder of Raster Technologies.

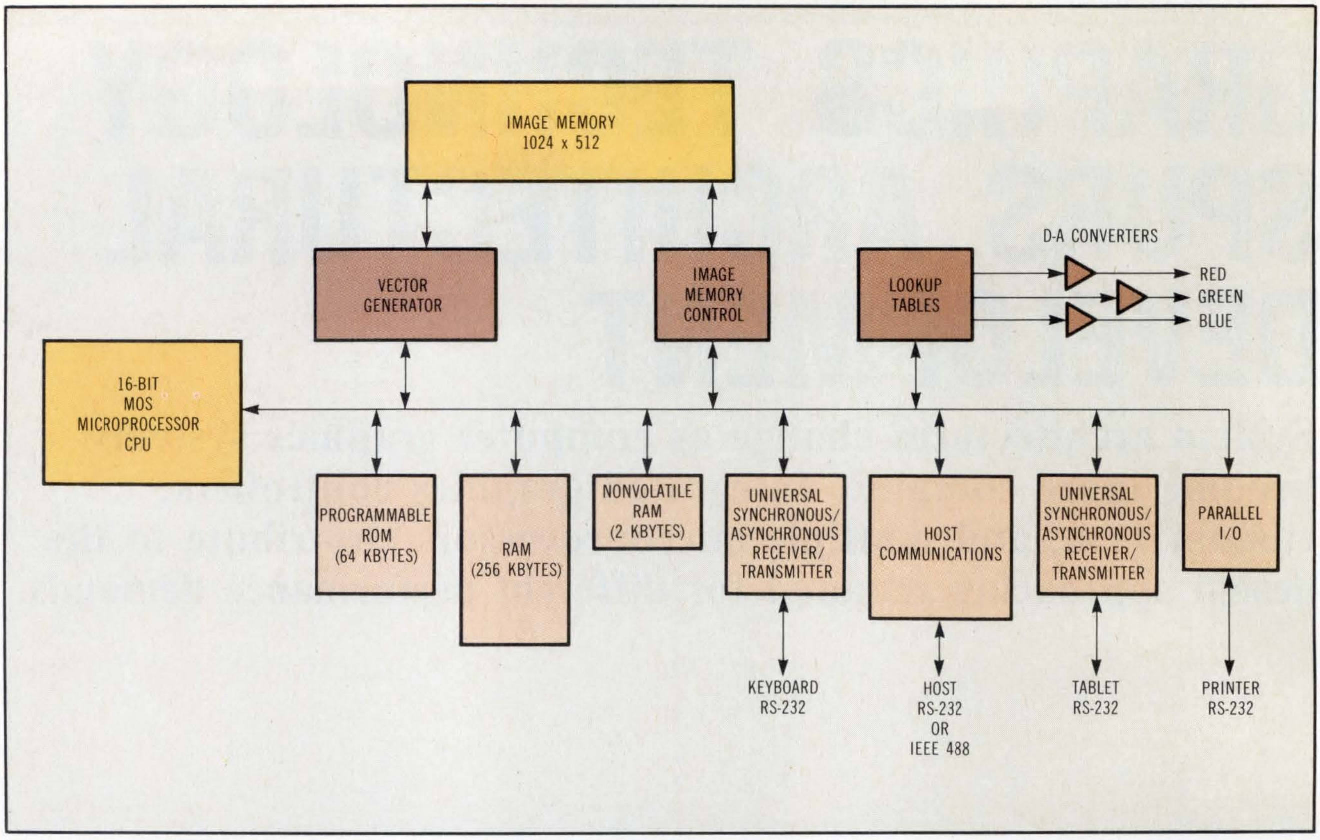

Fig 1 The medium resolution terminal uses three custom ICs for maximum performance—the vector generator, the video controller, and the frame buffer controller.

computer. This freed that computer to perform more complicated operations. System designers could now develop low cost, low to medium performance systems with a minimum of hardware complexity. Later systems improved user friendliness by allowing such interactive operations as rubberbanding of lines, dragging objects, and local menuing—all without host computer intervention. Unfortunately, because the microprocessor had to perform many steps, there were still many applications where these graphics systems were unacceptable.

The solution to at least some of the problems seemed to be the use of bit-slice processors in order to generate graphics primitives. However, the use of only a bit-slice processor still did not provide the necessary interactivity and flexibility.

Today, state-of-the-art graphics systems include both MOS microprocessors, for interactivity and flexible user interface; and special hardware, for graphics primitive generation. These systems can now off-load the host computer, but still provide the necessary user friendliness, high performance, and full interactivity.

Terminals versus workstations

Graphics systems now have two distinct uses: as remote graphics terminals, and as integral parts of engineering workstations. To be cost effective and to meet the user's performance needs, the graphics system has a different set of requirements for both situations.

Usually, a terminal has a considerable distance between the host computer and the user. In this environment, the graphics system is typically connected to the host over a relatively low speed communication link, such as an RS-232 serial interface or a long-distance modem. To achieve high performance levels, the link's low speed requires that the graphics terminal communicate with the host computer as little as possible. Local display list processing and a very powerful command set allow the system to perform interactive operations without host communication. The terminal need only communicate with the host to notify it of changes to the data base and to download the data base at the beginning of processing.

In the workstation application, a high speed communication link between the graphics controller and the host computer is used. Commonly located in the same cabinet or in the same room, the host computer and the controller are connected by a high speed DMA link. In this environment, it is usually too expensive to have redundant display list memory in both the display controller and in the host. However, it is still important (for the same reasons as in the terminal environment) to off-load the host from the heavy demands that interactive processing places on the system. Thus, even in workstation environments, a dedicated graphics controller is important.

Most existing graphics applications use a graphics controller in the terminal evnironment. Generally, the host computer is a minicomputer with many users contending for the system's resources. To achieve the desired system performance level, the graphics controller/terminal must solve as much of the graphics problem as possible. This includes graphics input as well as output.

One recent low cost display terminal optimized for terminal applications is the Raster Technologies Model One/10 (Fig 1). This terminal provides the user with medium resolution (640 x 480) and high performance (1 million pixels/s). It is also designed to handle the majority of graphics terminal applications. Custom VLSI technology makes it possible to obtain the highest possible performance in the unit's price range. In addition, three different ICs are developed to perform primitive generation and video control.

The first of these specialized ICs, the vector generator, is an intelligent device that handles setup and pixel generation for vectors. To generate a line, the IC is loaded with the two endpoints that define the vector. The vector generator handles all other operations. Special hardware inside the IC also supports picking, through the use of an aperture comparator. The aperture comparator greatly speeds display list processing.

Image memory uses nibble-mode 64-Kbit dynamic RAMs, allowing higher bandwidth for reading and writing if four consecutive addresses are accessed. The vector generator contains two 4- x 4-pixel caches that are written to by the vector generation hardware. When the vector generator crosses a 4-pixel boundary, the cache is written into the memory using the nibble-mode access. This allows the system to achieve 1-million pixel/s writing rates without double buffering or blanking. This speed is significantly faster than what designs using graphics controller chips can achieve.

Graphics systems now have two uses: as remote graphics terminals, and as integral engineering workstation parts.

The second IC provides the video frame control. The video controller provides the video refresh addresses and arbitration control. It works in conjunction with the vector generator to generate text when the system is used as an alphanumeric terminal as well as a graphics terminal. The video controller generates two separate addresses for video refresh: one set of addresses is used to drive the first eight bit planes of image memory; the other set of addresses is used to drive an additional two bit planes, which are typically used as overlay planes. The overlay planes can be used for alphanumerics, if desired, and can be scrolled independently of the graphics memory.

In addition, the video controller contains hardware comparators to compare the refresh address

Fig 2 A high resolution graphics system can be used for more demanding tasks, such as solids modeling and three-dimensional list processing.

counter outputs with the cursor position registers. When the two are the same, a cursor signal is generated. This signal is used by the frame buffer controller, the third specialized IC, to generate the cursor on the screen. This off-loads the microprocessor from drawing (and undrawing) the cursor in image memory.

The frame buffer controller takes the data out of image memory and generates the video output signal used by the D-A converters to drive the raster-scan beams. Each IC handles two bit planes; a fully configured system—with 10 bit planes—uses five frame buffer controller ICs. The frame buffer controller IC handles all data paths to and from the image memory DRAMs. It has a simple microprocessor interface that allows it to generate the appropriate data when writing vectors or generating an image. It also contains a 4 x 4 RAM for color lookup operations. When the terminal is configured with only four bit planes (16 displayed colors out of 4096), no additional external lookup table RAMs are required.

When the system is configured with 10 bit planes of image memory, all 10 planes can be used to generate the lookup table addresses. This gives the terminal a palette of 1024 colors. The lookup table output comprises three 8-bit banks of red, green, and blue, which gives the user a choice of 16.7 million possible colors. While the unit has a relatively limited number of colors, the fully programmable lookup table means that it can be used for applications requiring high quality imaging.

The system's high performance 16-bit general purpose MOS microprocessor is used for a flexible user interface and 256 Kbytes of RAM. It provides extensive display list firmware and is thus suitable for the vast majority of terminal applications.

The limitations and benefits of custom VLSI

For functions such as vector generation, custom VLSI processors provide the best way to optimize performance in the low to medium price range. Unfortunately, the VLSI processors have limited hardware flexibility. More complex algorithms must be performed entirely by the MOS microprocessor. For applications requiring two-dimensional line drawing and rectangular files, the terminal is an appropriate choice. However, there are graphics applications with performance demands beyond its capabilities, such as solids modeling and three-dimensional list processing. Model One/80, which incorporates the same high performance 16-bit MOS microprocessor as the Model One/10, meets the higher performance demands (Fig 2).

Instead of using the finely tuned—and relatively inflexible—custom VLSI ICs for performing vector drawing, the Model One/80 contains a very powerful microprogrammed processor that can perform many different graphics tasks in addition to vector generation. This processor incorporates custom VLSI technology, thus maximizing flexibility and performance. Fig 3 shows a block diagram of the display controller.

The display controller uses a uniquely flexible architecture designed to perform equally well in the two environments—as a workstation and as a terminal. It works as well in a tightly coupled workstation, with the host computer handling the display list management and storing the display list information in its own memory, as it does in a remote terminal environment with its own display list memory and handling the display list management itself. Up to 32 Mbytes of display list memory are available. This is more than enough for even the most demanding simulation applications. Whether it is used as a workstation or as a terminal, it handles all redraw and picking functions, as well as transformations and nesting.

Special custom VLSI features let vector generation and shading operations be performed at extremely high speeds.

When used as a terminal, the MOS microprocessor performs the display list management. The display list is stored in local memory. The microprogrammed processor handles all of the transformations, nesting, picking, and redraw functions to achieve maximum performance.

Custom VLSI is used for the complex counting and control functions necessary for high speed graphics primitive generation. This hardware is very

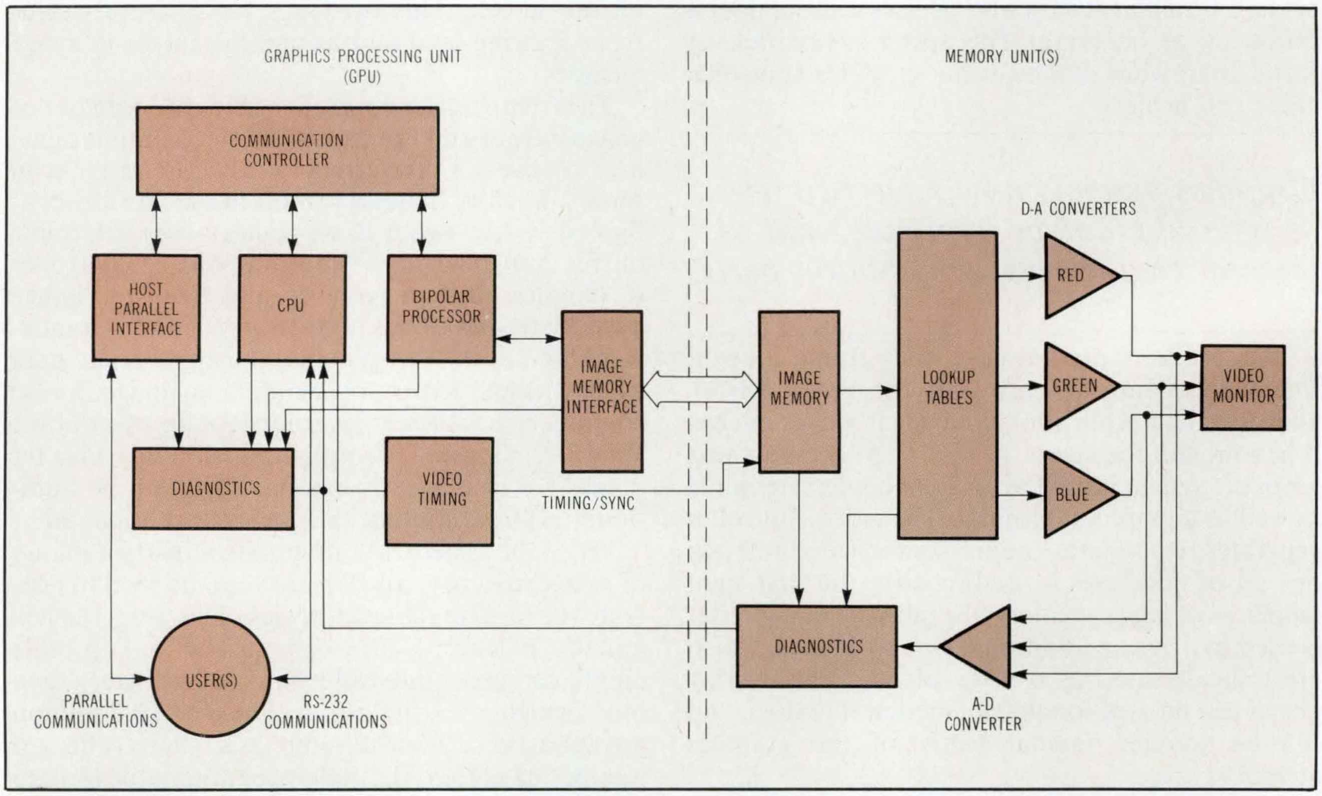

Fig 3 This block diagram shows how the display controller uses custom VLSI for the complex counting and control functions that are required for high speed graphics primitive generation.

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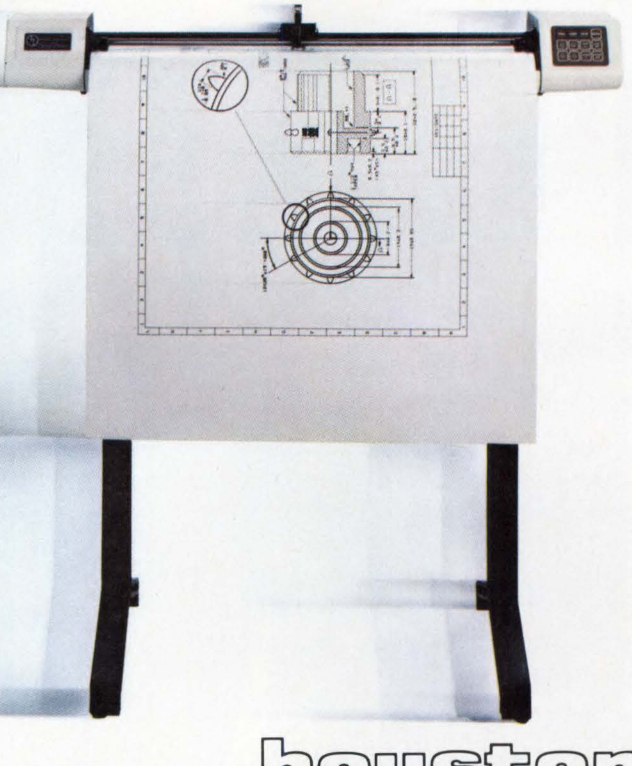

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CIRCLE 37

flexible, allowing a variety of different graphics algorithms to take advantage of the maximum performance available. The ICs are also designed to simplify the microcoding process needed to develop complex algorithms.

Special features in the custom VLSI allow vector generation and shading operations to be performed at extremely high speeds. For example, the system can draw up to 70,000 vectors/s, and it can draw pixels at up to 110 million pixels/s. Other custom hardware supports shading and hidden surface removal at close to 1 million pixels/s. Using custom VLSI achieves this performance level at a significantly lower cost than that of earlier, more primitive designs.

The display controller is designed to support a wide variety of video formats. This allows the system designer to choose the optimal configuration for individual price-performance requirements. It can support video configurations from 1280 x 1024 with 4 memory planes all the way to 1280 x 1024 with 24 or more planes, all running at 30-Hz interlaced or 60-Hz noninterlaced refresh.

A programmable controller handles the video format control. This flexibility is important in applications that switch between different display formats. For example, a high performance computer aided design application may require 1280 x 1024, 60-Hz noninterlaced refresh to reduce user fatigue, but it may also require video hard copy. Currently, video cameras do not support this high refresh rate. To generate hard copy using these cameras, the user can switch (under software control) to a 30-Hz interlaced refresh format.

As memory densities increase and VLSI technology improves, the decreasing cost of the same performance will mean that more users and new applications for graphics will be found. Already, some personal computers have bit-mapped graphics and wide color palettes.

The next generation of display controllers will perform additional functions: local solids modeling and ray tracing of images; faster three-dimensional rotation and transformation of display lists; and transformation and rotation of shaded three-dimensional images. No doubt, graphics controllers will become more powerful, performing more functions that presently require host intervention.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

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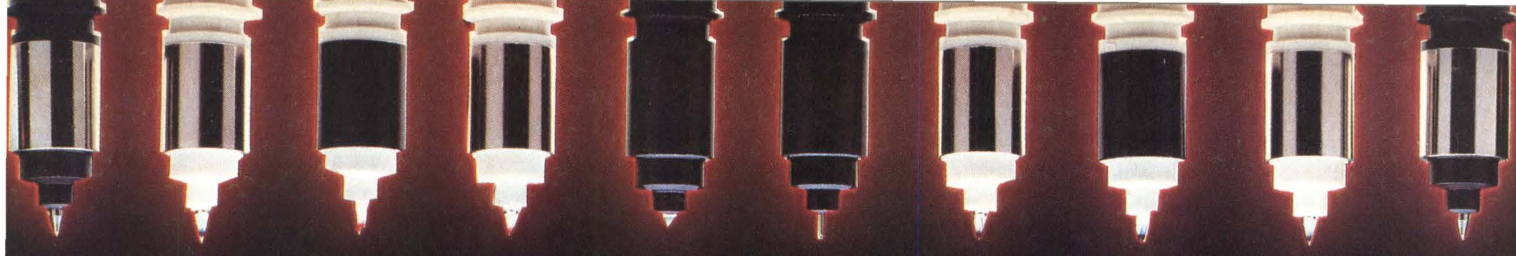


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The TEAM

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i8088	8 MHz
i8087	5 MHz
68000	10 MHz
68008	10 MHz
68010	10 MHz
Z80H	8 MHz
Z80B	6 MHz
i8085	6 MHz
i8048	11 MHz
i8049	11 MHz
i8050	11 MHz
i8035	11 MHz
i8039	11 MHz
i8040	11 MHz
i8748	11 MHz
i8749	11 MHz

The "BOX" Microprocessor Development Systems with the following Operating Systems:

CP/M 80
MP/M 80
CP/M 86
CCP/M 86
MP/M 86
MSDOS
iRMX (Intel Compatible)
CP/M 68K
OS-9
UNIX

Mainframe Simulators:

8086, 8088, 80186, 80188
68000, 68008, 68010
Z80, 8085, 6800, 6801, 6802
6809, 6301, Z8002
6500, 1802, 1804, 1805, 1806

Manufacturer Compatible Mainframe Cross Software for:

8086, 8088, 8087, 80186, 80188
68000, 68008, 68010, 9900, 99000
Z80, 8085, 6800, 6801, 6802
6809, 6805, 6301, 6305, Z8, Z8002
6500, 1802, 1804, 1805, 1806, 8096
8048, 8051, F8/3870, 9940, 8096

Mainframe PASCAL Compilers for:

8086, 8088, 8087, 68000, Z80, 8085

Mainframe "C" Compilers for:

8086, 8088, 8087, Z80, 8085

IBM PC Cross Software for:

8086, 8088, 8087, 80186, 80188
68000, 68008, 68010, Z80, 8085, 8048

IBM PC PASCAL Compilers for:

8086, 8088, 8087, 68000, Z80, 8085

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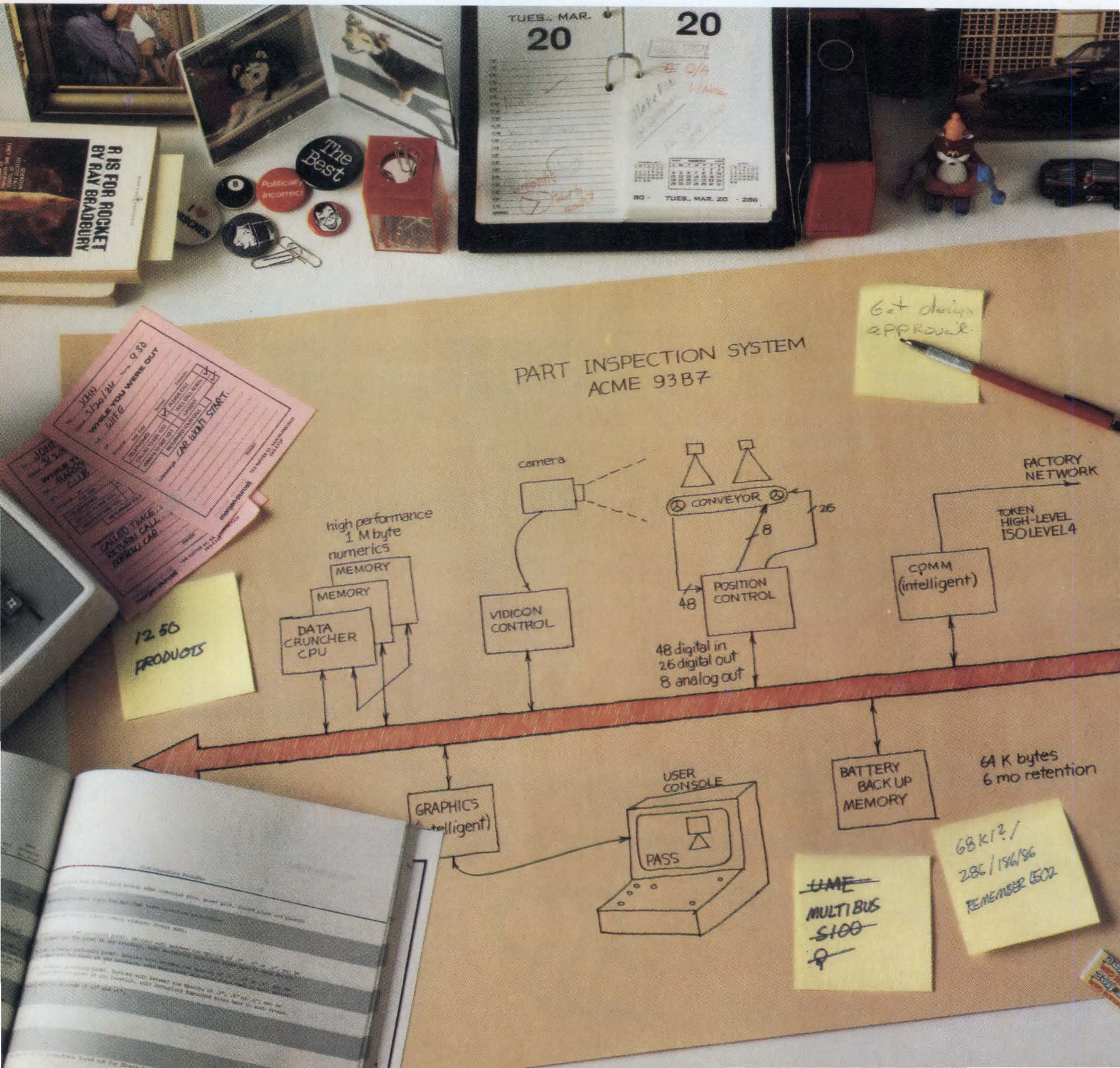

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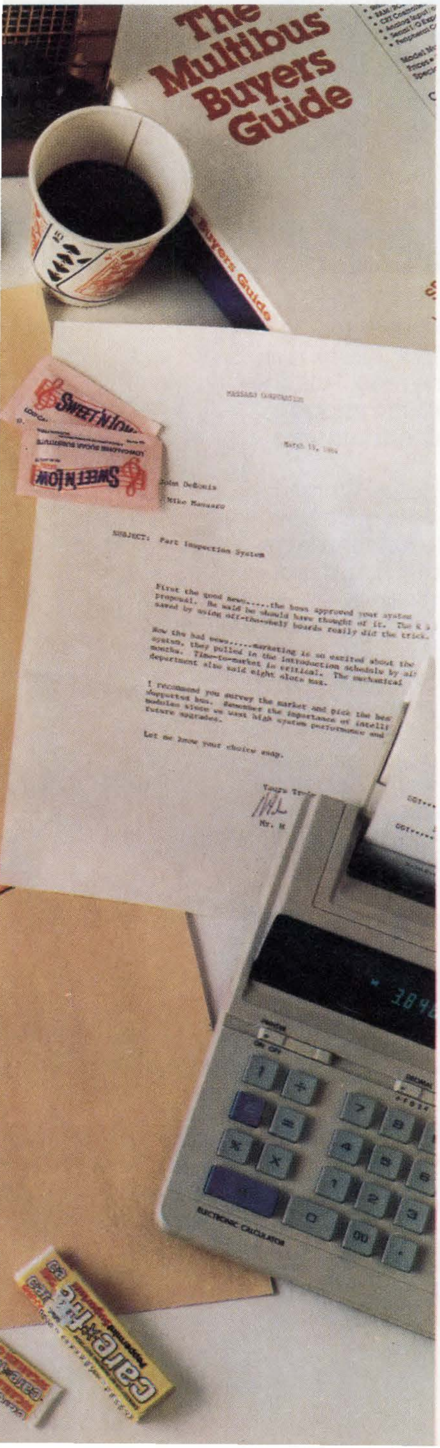

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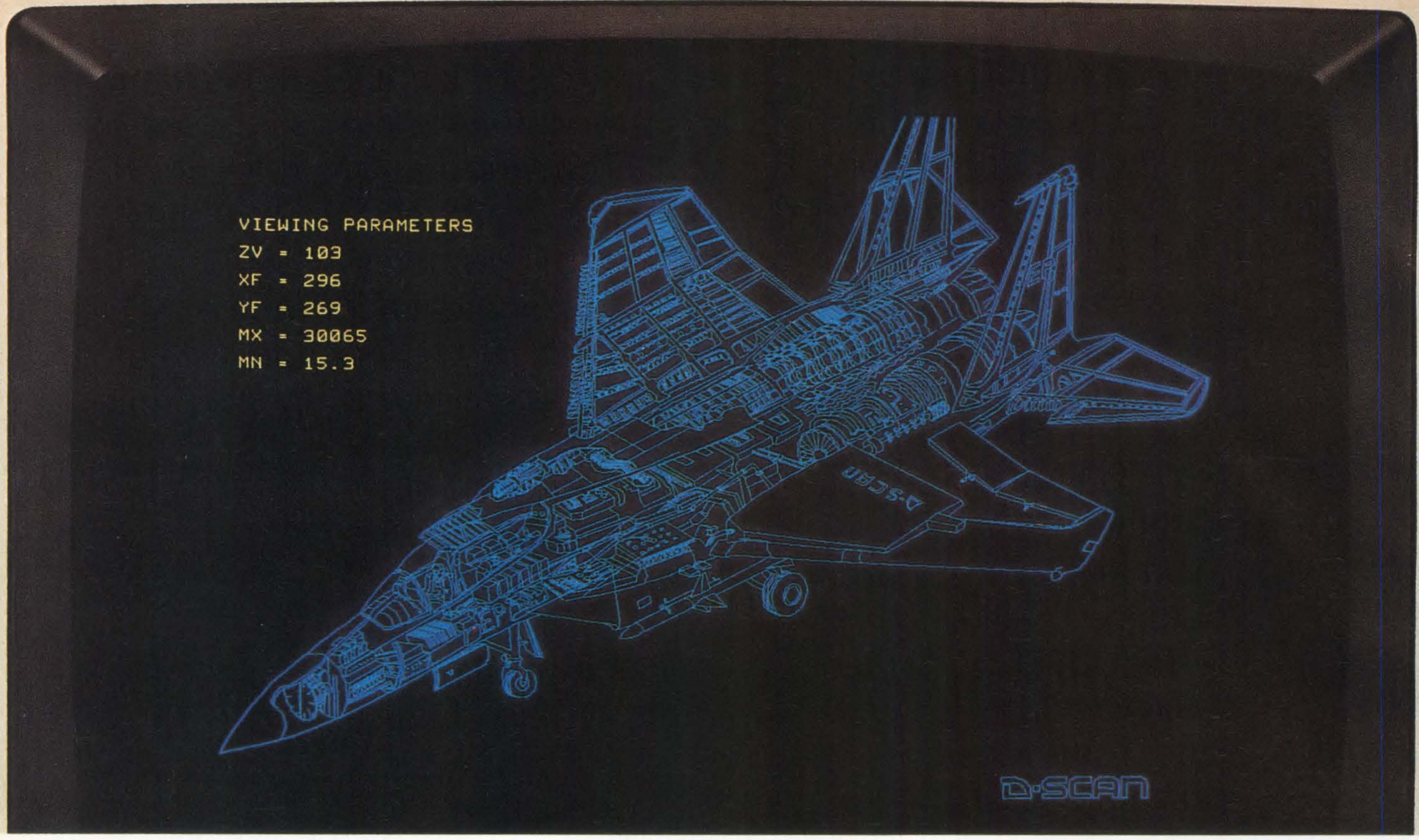

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STANDARDS GUIDE PRODUCT DESIGNS

Although they are potential sources of frustration among designers, standards can ease product development and enhance marketability.

by Bill Schweber

Standards—whether related to safety factors, design considerations, or performance specifications—can make or break a product's marketability. Thus, they deserve consideration early in the planning stages of a product's development cycle.

The effects of standards on design cycles and product cost are as varied as the types of standards themselves. They can either shorten or lengthen development cycles, decrease or increase product cost, and frustrate or aid designers.

Standards usually affect a product's marketability. They can help to better meet customer expectations, and provide companies with the opportunity to become market leaders and standards setters in certain market areas. As a standards setter, a company would be constantly referred to by the competition in such statements as "XYZ compatible." Even such claims as "better than XYZ" remind potential customers of that company's position in the industry as a market leader.

However, to effectively use standards to make a product successful—regarding scheduling and cost constraints as well as meeting market needs—a firm must sort through the multitude of standards available and decide which ones, if any, to use.

Standards exist to cover virtually every aspect of a product's design and performance, yet most products need only comply with a few of these. A successful project involves choosing the right standards for a specific market without burdening users with irrelevant or counterproductive ones. Office-equipment users, for example, are not interested in operation at −20 °C, and equipment designed for such operation would be too awkward and costly for such applications.

Bill Schweber is senior marketing engineer at Analog Devices' Measurement and Control Division, Rt 1 Industrial Park, PO Box 280, Norwood, MA 02062, where he is responsible for front ends and analog and digital I/O. He holds a BSEE from Columbia University and an MSEE from the University of Massachusetts at Amherst.

Covering all the bases

Although all standards must fall into one of the four major groups discussed in the Panel, "Categories of standards," they can also fall into various subcategories, depending on what product features they cover. Safety standards, for example, such as those from Underwriters Laboratories, specify requirements to ensure that a product will be safe in its intended application. However, such standards do not generally make statements relative to performance. In many locations, compliance with such standards is mandatory, and steps to ensure compliance must be considered early in the design cycle.

In another category, design standards specify overall electrical and physical factors. For example, the IEEE 488-1978 standard, entitled "Standard Digital Interface for Programmable Instrumentation," discusses signal types as well as interface connections for the IEEE 488 bus. It does not, however, cover such factors as syntax.

Design standards also include the Federal Communications Commission (FCC) and Verband Deutscher Electrotechniker (VDE) specifications for allowable conducted and radiated noise, as well as the IEEE 472 specification for surge-withstand capability. In another area, design standards for software are becoming increasingly important. In addition to

Categories of standards

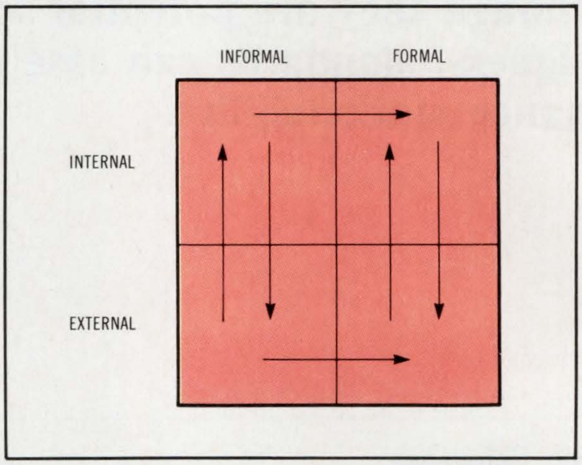
Standards exist in many forms, each of which can affect companies and their customers differently. Some are irrelevant to the user and affect only the product's design; others, in contrast, are vital to the end user. Standards can be promulgated by industry-wide groups or by government bodies, or they may be defined by the market leader. The market leader, of course, would be a company that is one of the first successful entrants in a new product area.

Standards fall into one or more of four groups: external, internal, formal, and informal. Note that these groups overlap to some extent. Indeed, a standard may begin in one group and migrate to another, depending on its success (see Figure).

External standards, for example, are seen by the end user. Although customers might not care what is inside a box, they might very well care whether an RS-232 interface, for example, is available and whether standard line voltages are used. In today's market, external standards also include such functional aspects as operating system software.

Internal standards are those seen only by the project design team and others within a company. They relate to design rules, parts, and assemblies. Examples include such factors as the use of standard board-level voltages such as 5 V and ± 15 V rather than oddball values. Note that, although customers will not care about the internal standards during normal product use, they may well care about how such standards can influence the availability of spare parts and long-term support. Custom assemblies and components are generally expensive and difficult to replace.

Formal standards are defined, recognized, and maintained by a major technical or trade group that does not represent any single manufacturer. These organizations, like Underwriters Laboratories (UL) or the Institute of Electrical and Electronics Engineers (IEEE), often develop industry-wide standards based on proposals from groups of manufacturers and users as well as technical experts. The development of a formal standard takes approximately five years. Compliance with formal standards may be mandatory, especially with those relating to safety and electromagnetic/radio frequency interference (emi/rfi).



Informal standards exist when a manufacturer has a leading market share and, thus, effectively defines the standard for a specific application. The IBM PC, for example, has no formal endorsement, yet it has effectively set a standard for many aspects of personal computer design. Because markets move so fast, informal standards develop relatively quickly compared to formal standards—often within two to three years. Many informal standards develop sufficient support and influence to become formal standards. Intel's Multibus, for example, has become the formal IEEE 796 standard.

operating systems, software standards now influence application packages and are spurring on the emergence of standard library functions as well as standard kernels and software drivers. The emergence of software standards is evident in such packages as the Tektronix PLOT 10 graphics language.

Among other types of standards, recommended practice and procedure standards define methods of setting up repeatable tests that measure the performance of a system or product under well-defined conditions. They can include military standards for shock and vibration and American Society for Testing of Materials (ASTM) standards for measuring wire strength. Such standards are important because they provide a common method for defining product specifications.

One area where these standards apply is in benchmarks for measuring software performance. Without such benchmarks, it would be difficult to evaluate a product's suitability for a specific application. Nevertheless, relatively few such standards exist, largely because of the wide-ranging nature of software products. Moreover, many of the available benchmarks either deliberately or inadvertently highlight only a few areas of computer performance while treating other areas unfairly.

Finally, ergonomic (human factors) standards are increasing in importance. They cover dimensions, operation, and visual aspects of a product's design from the user's viewpoint. Currently, much of the impetus for these standards comes from European organizations such as Deutsches Institute für Normung (DIN), which defines guidelines for computer keyboards and display terminals.

Pros and cons of standards

The case for following a standard is not always clear cut. Judgments must be made with respect to a company's engineering and production resources, allowable product development time, and end-user expectations and requirements. Thus, there are several key points to consider in favor of standards.

Following standards might free designers to buy rather than design and build many assemblies, thereby cutting design time and cost. For example, except in some high volume, low cost applications, buying off-the-shelf power supplies and cabinets can offer large savings without impeding performance. Industry

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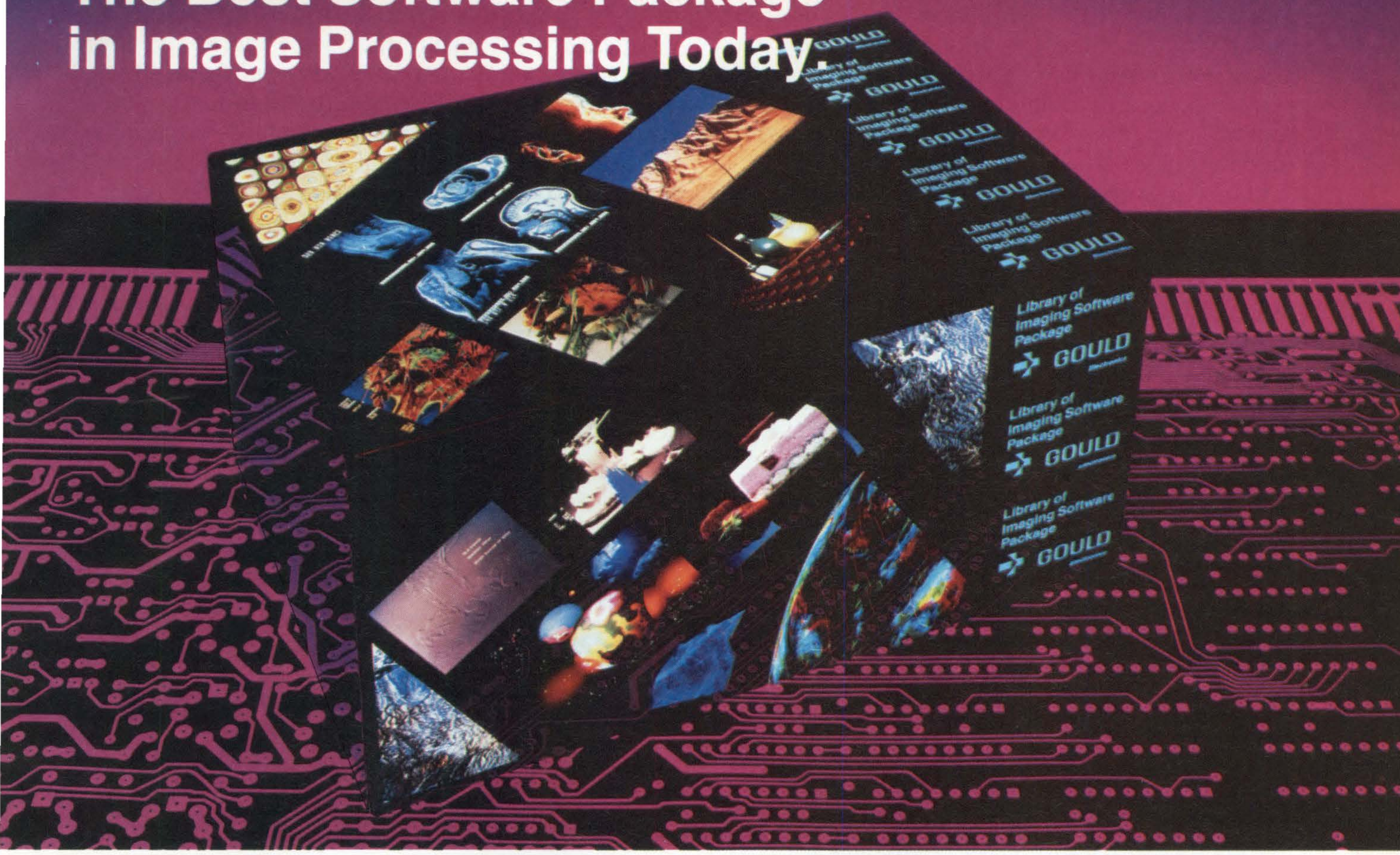

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IMAGE CAPTIONS

Top:

- *Left back corner: 2-D FFT processed in 2 minutes with LIPS Plus.*
- *Four 1024^2 medical images: multimodality, split screen display.*
- *Face: CT scans in 3-D modeling, plastic surgery at Mallinckrodt.*
- *Mountains: LIPS assists fast graphics hardware and large memory matrices with GKS-based Auxiliary Graphics Processor. Courtesy S.A.I.*
- *Pseudo-colored flowers: shows LUT manipulations. Note graphic load display plus intensity reference scale.*
- *Same 1024^2 flowers: shows color cut and paste in 1 frame time.*
- *Jars and pens: Synthetic image like #4, courtesy Pacific Data Images. Photo by Jim Weil.*

Bottom:

- *Two corners: LIPS driver supports 1024^2 LANDSAT imagery, courtesy NASA-Ames Research.*
- *Top bas relief: Matrix filter, the basis of classification and recognition. LIPS allows kernels of any shape and size and executes at video rates.*
- *Histogram: line or pixel analysis under LIPS.*
- *Spheres: fast Z-buffer merge, courtesy Rensselear.*
- *Cake and strawberries: 1024^2 looks good enough to eat.*
- *Bottom: mesh algorithm, courtesy Lunar & Planetary.*
- *Weather satellite: shows graphics overlay, courtesy MacDonald Dettwiler.*

GOULD
Electronics

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standards can ease peripheral interconnection, encourage development of second sources, and make it possible to offer peripherals with a wide range of performance. For example, such a standard could support one-, two- and eight-pen plotters with a single graphics language.

Marketing and sales groups can more readily promote and sell products that meet standards. Consider, for example, that even if salespeople are not experts in the IEEE 488 standard, prospective customers will understand the interface standard's implications. If, on the other hand, a particular product uses a custom interface, customers will require more detailed explanations from a more knowledgeable sales force. Moreover, a nonstandard product that is no better than the standard will fuel customer confusion and skepticism.

Many standard software packages provide tools that speed product development. Chip vendors as well as third parties offer development tools for some 16-bit microprocessors, and many such tools would take a company months to duplicate and debug. If firms use standard software, users can buy standard software packages elsewhere to fit their specific applications, thus opening up new markets. A good office accounting machine, for example, might run materials management software.

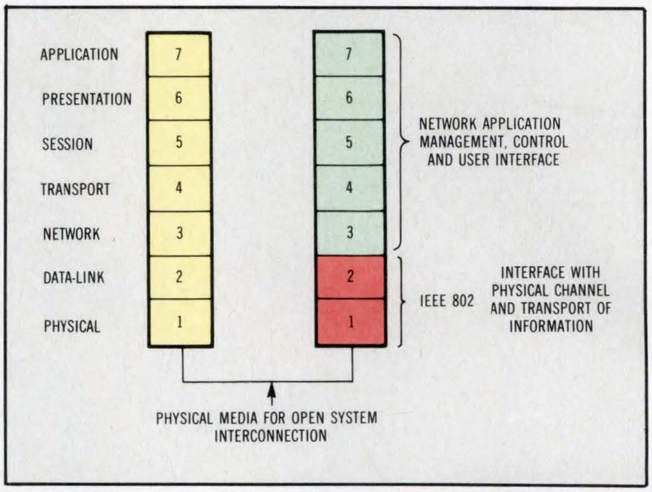
Standards make it easier for firms to develop joint marketing efforts with other companies who offer complementary or supplementary products. With such efforts, a company can offer more to its current customers and expand into new markets. Certain standards (eg, those related to safety) may be required before a firm can sell a product or specify its performance.

Despite these factors, the argument for standards is not one-sided. Many successful designs do not adhere to standards, yet handle the jobs they were intended to do with superior price and performance. It is important, therefore, to also examine the drawbacks of standards.

Many standard software packages provide tools that speed product development.

Following a standard, for example, might cost more than a minimum design that adequately performs the intended task. Similarly, it might prevent reaching performance goals. For example, there may be a need to achieve fast disk I/O performance that cannot tolerate the time-consuming routines and calls of standard software. Standards could also stifle engineering innovation, giving engineers insufficient opportunity to be creative, particularly in the development of a dramatic new product.

Adhering to standards makes it harder for customers to distinguish one firm's product from that of the competition. Thus, in following standards, companies must ensure that some factor (eg, low price, better implementation, or a subtle improvement) makes their offering more than just a "me-too" product. Testing to a standard—especially when it involves an external organization performing the tests (eg, UL or a lab with special equipment)—can be time consuming and costly. This drawback is applicable particularly to safety, and practice and procedure standards.

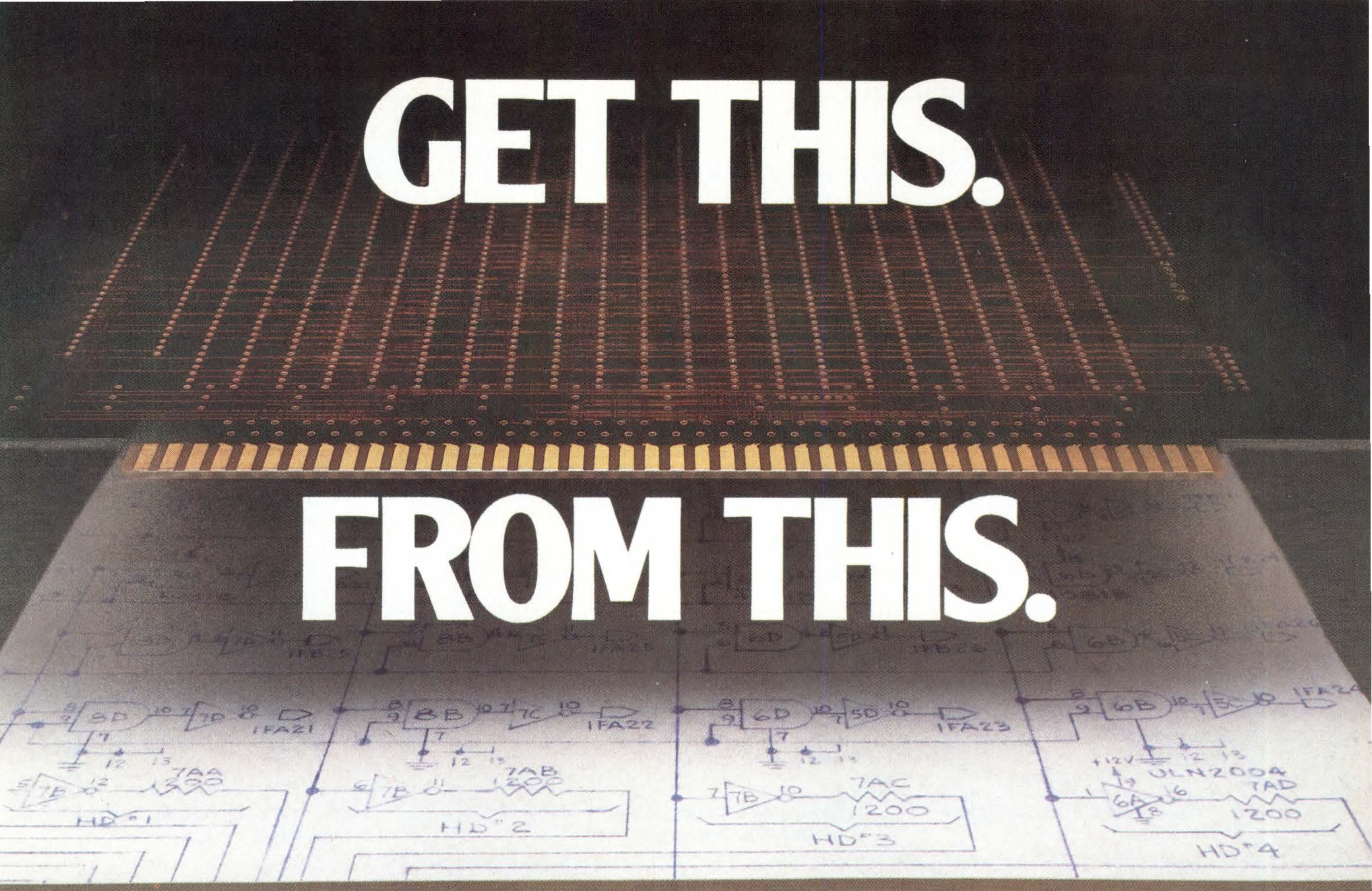


Formalizing standards can reduce confusion among vendors and customers alike. Helping to clarify local area network specification, the IEEE 802 standard is compatible with the lowest two layers of the seven-layer International Standards Organization Open System Interconnection model.

De facto standards could place competing firms at the mercy of the industry leader. For instance, if a company chooses to offer a low cost "XYZ-compatible" terminal, consider how it could respond (eg, it would have to move quickly, refocus its market, or cut prices) when XYZ comes out with a new model, or improved firmware that "turns on" previously hidden features.

Formal standards are slow in developing, and after following a proposed or preliminary standard, a company might find that the standard has changed by the time their product reaches the market. Alternatively, a company might have to wait until the standard is formalized before introducing the product. Neither choice is pleasant, and misjudgment could ruin the product's chances.

Two examples—local area networks and sub-5¼-in. floppy disks—illustrate this last point. Many good networks are now available. But they are harder to explain, and thus more difficult to sell to less-knowledgeable users because the industry standards have not been completely formalized. The approval of some sections of the IEEE 802 standard, which covers the first two layers of the seven-layer International Standards Organization (ISO) Open System Interconnection (OSI) reference model, is correcting this difficulty (see Figure). Until recently, however, the standards situation surrounding networks has confused manufacturers and users alike.



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Formal Standards Organizations

Organization	Types of standards	Examples
American National Standards Institute (ANSI)	A wide variety—data formats, coding, safety, software, test procedures, definitions. Some are jointly published with other organizations.	National Electrical Code, ASCII, Fortran, flowchart symbols
American Society for Testing of Materials (ASTM)	Standard tests for strength and performance of materials and substances; procedures for calibration of testing equipment	Temperature, heat, strength of metals in certain applications, strength of bonds and connections
International Telegraph and Telephone Consultative Committee (CCITT)	Standards related to telecommunications	Modems and interfaces, protocols, formats
Canadian Standards Association (CSA)	Primarily safety-related standards	CSA566B for electrical and electronic test and measuring equipment
Deutsches Institut für Normung (DIN)	Standards covering form factors and ergonometrics, among other things	Panel meter cutouts, keyboard and CRT dimensioning, printed circuit card size and connectors
Electronics Industries Association (EIA)	Interface and signaling standards	RS-232, RS-422 for communications; RS-170 for baseband video
Federal Communications Commission (FCC)	emi/rfi standards	Docket 20780, Class A and Class B
Federal Information Processing Standards (FIPS)	Cover data codes, signaling, data encryption, parity	PUB 46: Data Encryption Standard
International Electrotechnical Committee (IEC)	Standards covering safety, procedures, definitions	IEC 225: octave, half octave, and third octave band filters
Institute of Electrical and Electronics Engineering (IEEE)	Extremely wide variety covering test procedures, definitions, interface standards, safety, networks	IEEE 488 interface bus, -472 surge withstand, -770 Pascal language, -802 networks
Instrument Society of America (ISA)	Standards for installation, calibration, dimensions, and definitions of process-control transducers and instrumentation	S50.1 Compatibility of Analog Signals for Electronic Industrial Process Instruments
International Standards Organization (ISO)	Standards for measurement, data encoding, signal transmission	ISO 646.7 Bit Character Set for Information Processing Interchange
MIL standards (U.S.)	Performance, form factors and connectors, reliability, shock and vibration, emi/rfi	MIL-STD 810C Environmental Test Methods, 561 and 562 emi/rfi
National Bureau of Standards (NBS)	Fundamental physical measurements and calibration	NBS 125 Thermocouples; Data Encryption Standard 1977
Underwriters Laboratories (UL)	Safety and related performance of equipment and components	UL 1244 Electrical and Electronic Measuring and Testing Equipment; UL 94 Flammability of Plastic Materials
Verband Deutscher Electrotechniker (VDE)	Standards for safety, form factors, performance, emi/rfi	VDE-0871A for emi/rfi

Note: Some standards were originally supported by one organization but are subsequently supported by others (eg, ANSI/IEEE C62-41-1980 "Guide on Surge Voltages in Low Voltage ac Power Circuits" was IEEE 587-1980). In other cases, similar though not identical standards exist in several organizations (eg, RS-232-C and CCITT V.24 and V.28).

Similar confusion surrounds the sub-5¼-in. floppy disk market. No single vendor has established a dominant position, so several incompatible 3- to 3½-in. formats have emerged. This may limit market acceptance of any one format.

When deciding which standards to follow, consider these pros and cons as they relate to a particular product and market. Observe whether a company has the resources to handle the entire design of a nonstandard product feature. Determine first if following a standard is a cost-effective approach. If the answer seems to be no, evaluate carefully whether the apparent higher costs of following the standard might be more than offset by the possible availability of multiple sources for assemblies and parts. Also, consider the marketing aspects. Is there a set of standards that the intended user expects a given product to follow? A user may,

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mounting brackets and a face plate, fits into the same space as a half-height 5¼" Winchester offering even further shock and vibration isolation. Now, system designers have a new level of flexibility. One area that has received attention is use with portable computers. Several major portable computer manufacturers have already incorporated Rodime 3½" Winchester disk drives into their products. There are other equally exciting areas such as desk top computer systems, intelligent terminals, point-of-sale terminals, industrial controllers, telecommunications systems, navigation and guidance systems, and portable instrumentation. In fact, the list of potential uses is only limited by the imagination of the system designer.

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In a few short years, Rodime has established itself as a major force within the Winchester disk drive industry. Rodime is one of the few manufacturers that are delivering 5¼" Winchester drives with a broad range of capabilities up to 54 megabytes. And is the only manufacturer delivering high-performance 3½" Winchester drives in production quantities.

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for example, expect a 0- to 10-V output to a recorder rather than the 0- to 10.24-V level that may be easier for a company's 10-bit D-A converter to furnish.

There are many other questions to answer. It is important to find out if standards can be used to leverage the product's capabilities and increase its market. It is equally important to discover whether the sales force will be able to explain the product, and if customers will be able to understand it in areas where it does not conform to a standard. Other questions focus on whether some standards are mandatory, either from a legal or practical standpoint. Finally, finding out which standards the competition follows is a must.

Making the right choice

A firm must also grapple with the problem of making its product stand out while still following the standards that its market demands. In many ways, the best products from the user's viewpoint are those that follow standards and, at the same time, add proprietary features. For example, a computer/controller system that fully follows the IEEE 488 standard but also offers outstanding environmental specifications (eg, a wide temperature range, and the ability to withstand high levels of vibration) would be attractive to potential users in some applications.

To illustrate further, Mostek recently introduced a RAM whose function and configuration is fully compatible with a *de facto* standard IC. The company's RAM, however, also includes a lithium battery built into the package. In addition, it is equipped with the circuitry necessary for automatic switchover from the system power supply to the internal battery. This provides a nonvolatility feature that is transparent to the IC user.

Adding proprietary features to a product that otherwise follows specific standards is only one way of improving its chances for success. A product can also be successful if it performs a relatively straightforward function and complies with specific standards that customers require for their applications.

Consider, for example, a computer that provides an analog output from a built-in D-A converter to a process control system. Although such a function might seem simple, its implementation could involve electrically isolating the computer circuitry from the process control loop and converting a D-A converter's 0- to 10-V signal to a 4- to 20-mA signal. Moreover, the process control interface might have to conform to the Instrument Society of America's (ISA) S50.1 standard, entitled "Compatibility of Analog Signals for Electronic Industrial Process Instruments." Using a component such as the Analog Devices 2B22 voltage-to-current converter can help meet such requirements. It provides isolation to 1500 Vdc, converts a 0- to 10-V level to a 4- to 20-mA current level, and conforms to certain ISA S50.1 and IEEE 472-1974 (surge-withstand) specifications. These features justify the unit's higher cost.

A list of standards-setting organizations can be bewildering. When deciding which standards to consider, first determine what potential customers want and what standards the competition currently meets. Note that many standards specify several levels of performance. Designers should know which levels they want to meet.

It is important to get a copy of the standard being considered rather than just relying on a summary, since there is much folklore surrounding some standards. For example, the RS-232 standard does not discuss the encoding of characters sent over the interface, yet many people assume that the standard specifies ASCII characters because they are almost always used in practice. RS-232 is the formal standard; the use of ASCII characters is an informal one.

The Table shows some key standards organizations, the areas they cover, and some important standards that they publish and maintain. Whatever standards a company elects to follow, it must know exactly what "follow" means. Methods of compliance range from self-certification (eg, stating that a product is RS-232 compatible) through evaluating engineering drawings or sample units by external testing bodies. These are procedures that, when sucessfully completed, allow a firm to state that its product is "approved," "listed," "recognized," "certified," and so on, by the appropriate body. Bear in mind that some national standards are adopted (with modifications) as international standards. Meeting both national and international standards usually provides a marketing advantage.

Remember that a company need not be totally at the mercy of standards. As previously mentioned, it can become an industry leader and set *de facto* standards, as well as participate in the development of formal standards through involvement in professional organizations such as the IEEE, ISA, or ASTM. Through such involvement, a firm can help demonstrate its expertise in product design or in understanding the market.

Areas particularly ripe for involvement now include computer graphics. Currently, the Association for Computing Machinery's Special Interest Group on Computer Graphics (ACM/SIGGRAPH) is developing some standards for computer graphics and languages in cooperation with the IEEE. These standards are aimed at allowing different languages and machines to use, to some extent, the same basic computer graphics software modules.

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DIGITAL'S MICROVAX I. THE BEST ENGINEERED 32-BIT MICROCOMPUTER IN THE WORLD.

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They succeeded with VAX™ architecture. A design strategy so successful, it completely revised what the world expected from 32-bit computers.

Those same engineers have been at it again. This time, compacting VAX architecture into the MicroVAX I™ system.

A micro by every measure, the MicroVAX I system nevertheless delivers all the versatility and speed you've come to expect from its larger namesakes. It guarantees both hardware and software compatibility with other VAX computer family members. It lays claim to the same treasure chest of development tools, utilities and languages. It provides access to the same impressive library of proven applications.

With the MicroVAX I system, the industry's premier 32-bit architecture has been miniaturized by VLSI technology. Along the way, Digital's engineers dramatically reduced something else: the cost.

Entry into the celebrated VAX computing family is now possible for as little as $10,000.

THE UNCOMMON BENEFITS OF VAX ENGINEERING HERITAGE.

A genuine VAX computer, the MicroVAX I system has been, in a sense, already proven at tens of thousands of VAX installations.

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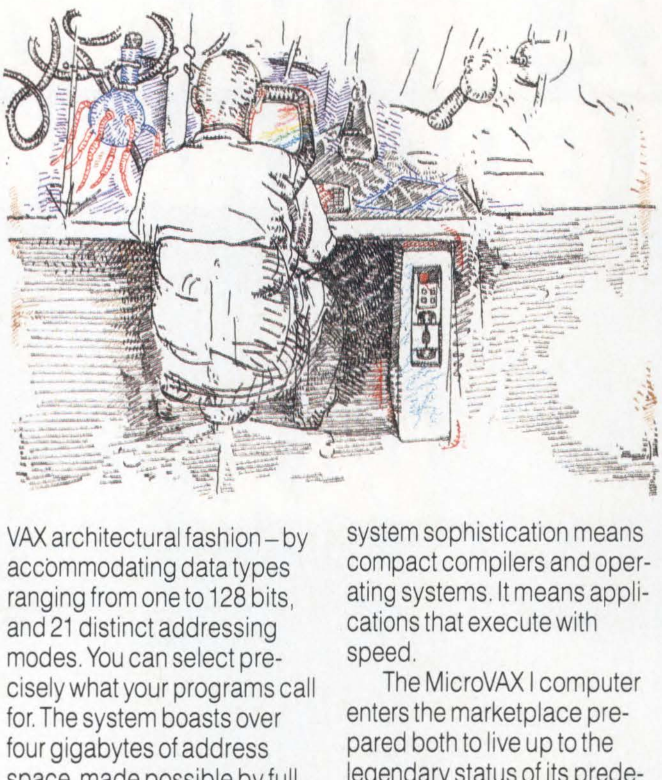

VAX architectural fashion – by accommodating data types ranging from one to 128 bits, and 21 distinct addressing modes. You can select precisely what your programs call for. The system boasts over four gigabytes of address space, made possible by full virtual memory management.

The MicroVAX I system also inherits the elegant VAX instruction set. Some three hundred separate instructions. This gives developers exquisite control over the micro, and in turn, gives the system extraordinary applications flexibility.

Bit efficiency for speed, elegant instructions for flexibility, and consequent growth potential are the heart of VAX architectural excellence. They free MicroVAX I system users from memory overlays, program segmentation and other encumbrances of competitive 16- and 32-bit micros. VAX system sophistication means compact compilers and operating systems. It means applications that execute with speed.

The MicroVAX I computer enters the marketplace prepared both to live up to the legendary status of its predecessors, and to make a name for itself.

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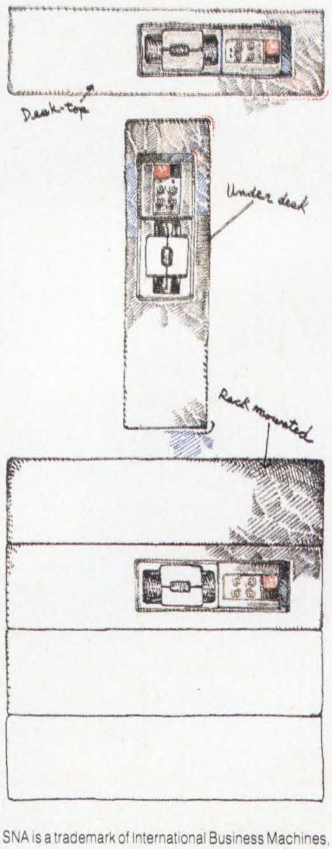
To be sure, the MicroVAX I computer is a true micro. It fits under the desk, on the desk, or most compactly of all, taking up just 5¼" of height in a 19" rack.

The MicroVAX I system delivers over 35% of the raw power of Digital's VAX-11/780 computer. Enough to satisfy your most demanding supermicro applications. Enough to comfortably support up to five users.

There is big system capacity: one-half million bytes of physical memory is standard, and expandable to four megabytes. For highly technical applications, MicroVAX I systems also come standard with support for both single and double precision floating point arithmetic.

To enhance the already impressive execution speed, Digital's engineers even put in



an eight-thousand byte direct-mapped cache memory.

SYSTEM SOFTWARE ENGINEERED TO GIVE YOU UNMATCHED VERSATILITY.

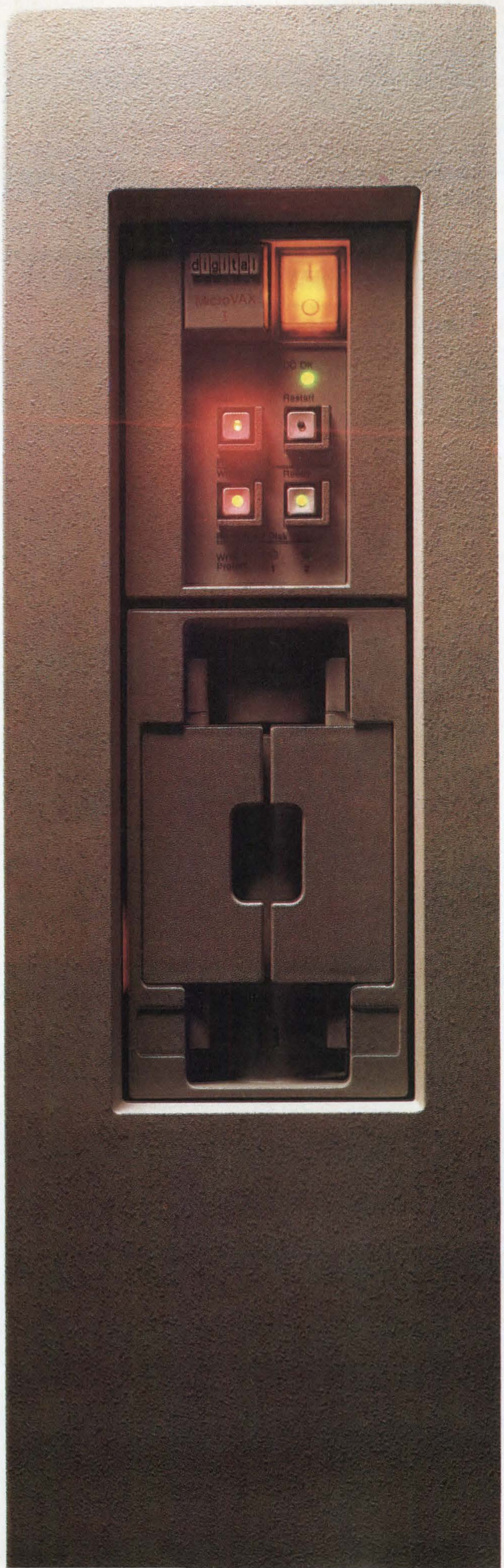
While ordinary micros give you just one, often thinly supported operating environment, the MicroVAX I system gives you a choice.

There is the MicroVMS™ operating system, Digital's famous VMS™ general-purpose system repackaged for the MicroVAX I computer. Within the storage capacity of your configuration, it will execute any user-mode VMS application. Unaltered. This opens up the complete range of unique and highly specialized Digital and third party applications and tools.

For incomparable economy, the MicroVMS operating system has been packaged by function into modules. You buy just the modules you need for your environment, then tailor the system to your application. The basic system module contains all the capabilities necessary to run applications. You can then add a program development module, a choice of networking modules, programming languages, and other optional products simply and easily. Because you never buy what you don't need, up-front investment is minimized and system overhead is reduced.

For realtime control, distributed computing and network-based multiprocessing, there is the VAXELN™ realtime programming toolkit. It gives you access to all the productivity tools of VMS. Applications developed on VMS with VAXELN software can be transported to other VAX or MicroVAX I target systems for execution. The applications do not need an underlying operating system.

The MicroVAX I system will excel in a variety of applications settings. It is a team computer in business. A network node in process control. A technical workstation. It is a compact, high-powered computer that can be taken on location for seismic, marine and field engineering applications.



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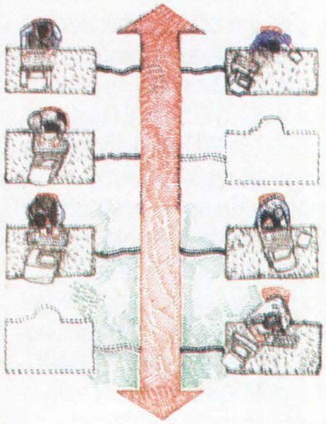
Inexpensive and high performing, the Q-bus™ data path has become a leader in the micro world and the choice of Digital's engineers for the MicroVAX I microcomputer.

The Q-bus data path now performs block mode data transfer, substantially improving its efficiency. The bus delivers transfer rates of over three



million bytes per second.

There are hundreds of devices and interfaces available for it. You may already have an investment in Digital's Q-bus structure. If so, a MicroVAX I system affords an easy and economical upgrade path to 32-bit power. For design start-ups, it gives you ready access to a complete range of supplementary products.

NETWORKING: YOUR WIDE-RANGING PRESENT, YOUR FAR-REACHING FUTURE.

The MicroVAX I system is a full-fledged member of one of the broadest ranges of compatible hardware ever sold. With it, you may employ a single, consistent computing strategy from micros to huge clustered systems.

(Continued overleaf)

You can progress along this computing path with ease, transporting programs and data among systems as your needs dictate.

As your micro applications grow, for example, it is easy and cost-effective to transport programs and files from the MicroVAX I computer to larger systems. Conversely, a MicroVAX I system becomes an ideal target for programs developed on a bigger CPU. The MicroVAX I computer can communicate with all of Digital's other computing systems via DECnet™ software. As part of a DECnet network, MicroVAX I systems can also be linked with highly efficient gateways leading to IBM's SNA™ networks and X.25 public packet switching networks.

Within smaller geographic areas, the MicroVAX I system connects to Ethernet (supported by DECnet software) by simply clamping onto the cable. In doing so, it becomes the first ready-to-implement microcomputer for building high-speed data communications and powerful processing into local area networks. Both MicroVMS and VAXELN software support the Ethernet connection.

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Like all of Digital's products, the MicroVAX I microcomputer is engineered for quality and produced to Digital's enviably high manufacturing standards.

The MicroVAX I computer incorporates many built-in system diagnostics. The most powerful of these is a microcode verify that performs a CPU self-test each time the computer is powered up. Many diagnostics run concurrently with normal processing, so if a failure does occur, it can be corrected quickly.

Every detail that helps assure reliability has been attended to. The system's 230-watt power supply, for instance, features thermal shutdown, overvoltage and overcurrent protection, a/c input transient suppression, and a minimum four millisecond powerdown time.

Overall, modular construction makes system service both rapid and inexpensive.

The MicroVAX I system is backed by one of the industry's most experienced small system support organizations. Digital pioneered on-site service with guaranteed up-time contracts and a selection of field services, software support programs, and user training agreements so comprehensive they suit virtually every need.

No other 32-bit microcomputer in history has ever offered its users greater potential for success.

While others promise performance, you'll be working with the industry standard 32-bit engine.

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And while others promise support, you'll be dealing with a company that has over 475 support offices in 44 countries.

BEST ENGINEERED MEANS ENGINEERED TO A PLAN.

The MicroVAX I computer, like every Digital hardware and software product, is engineered to conform to an overall computing strategy. This means our systems are engineered to work together easily and expand economically. Digital provides you with a single, integrated computing strategy direct from desktop to data center, from chips to huge multiprocessing clusters.

As its name suggests, the MicroVAX I microcomputer is the beginning of a complete system and component program based on Digital-developed VLSI technology.

The MicroVAX I system is shipping now.

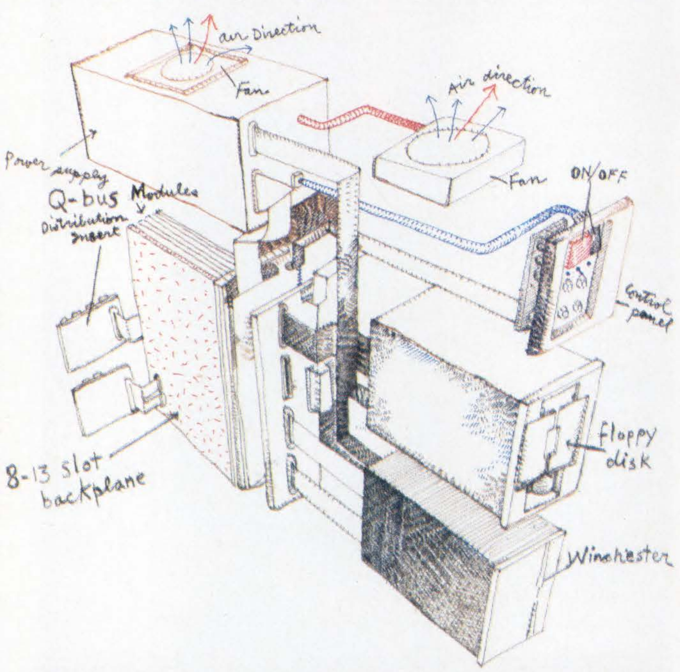
For additional product information or the name of your nearest Digital sales office or Authorized Industrial Distributor, call 1-800-DIGITAL, extension 225. Or write: Digital Equipment Corporation, Dept. MV1, 200 Baker Avenue, West Concord, Massachusetts 01742.

THE BEST ENGINEERED COMPUTERS IN THE WORLD.

DIGITAL'S MICROVAX I TECHNICAL SUMMARY

SYSTEM CONFIGURATION

Basic system for $9,995 (U.S. price, one only) includes: Two-board CPU, one-half Mbyte main memory (expandable), modular power supply, I/O port, and eight-slot Q-bus backplane. A disk-based system at $13,880 (U.S. price, one only) includes a 10 Mbyte fixed Winchester (expandable) and an 800-Kbyte floppy drive. Volume OEM discounts apply.



HARDWARE OPTIONS*		Optional	System Maximum
	Memory:	256 KB, 512 KB with parity	4 MB
	Floppy Disks:	2 x 400 KB	4 x 400 KB
	Fixed Disks:	11 MB, 31 MB	62 MB
	Communications:	1, 4, 8 lines Asynchronous Ethernet Synchronous	

*All configurations not supported by all operating systems.

SOFTWARE

Operating Environments: MicroVMS™; VAXELN.™
Supports Applications Written In: BASIC; COBOL; FORTRAN; PASCAL; PL/I; C; DSM; MACRO; LISP; OPS/5; DIBOL; RPG II.

MECHANICAL SPECIFICATIONS		Width		Height		Depth
	Rack Mount:	48.3 cm	x	13.3 cm	x	64.8 cm
		19″	x	5.25″	x	25.5″
	Floor Stand:	25.4 cm	x	62.3 cm	x	72.4 cm
		10″	x	24.5″	x	28.5″
	Table Top:	54.6 cm	x	15.2 cm	x	68.5 cm
		21.5″	x	6″	x	27″

WEIGHT (chassis only): 22.68kg (under 55 lbs.)
OPERATING TEMPERATURE: 15-32°C (59-90°F) at sea level.
OPERATING HUMIDITY: 20-80% relative humidity, noncondensing.

*Prices apply U.S. only.

SERIAL BACKPLANE SUITS MULTIPROCESSOR ARCHITECTURES

Serial communications based on modified local area network techniques can provide cost savings and flexibility in systems using distributed processors and controllers.

by Mike Webb

The growth of VLSI technology has caused a dramatic drop in the cost of active elements in computing systems. This, in turn, has led to increased use of distributed multiple processors in systems. The greater use of multiprocessor architectures, increased concern for system reliability and integrity, and the rising cost of traditional parallel bus backplanes have all kicked off a search for alternatives to traditional interconnect schemes in computing system architectures. One promising approach is the "serial backplane," which connects subsystem elements by using modified techniques found in local area networks.

Serial backplane interconnects offer significant hardware and software advantages over traditional parallel approaches. The cost of serial interconnect hardware is significantly lower than for edge connectors or pin-and-socket systems. Moreover, serial interconnection is more flexible and gives the system designer more freedom with the final product.

The key to cost-effective serial backplanes, however, is the availability of inexpensive serial controllers that run at data rates sufficient to support system needs. Given the decreasing cost of silicon and the increasing speed of MOS VLSI components, hardware cost advantages are within reach for many applications. The main reason why a serial backplane

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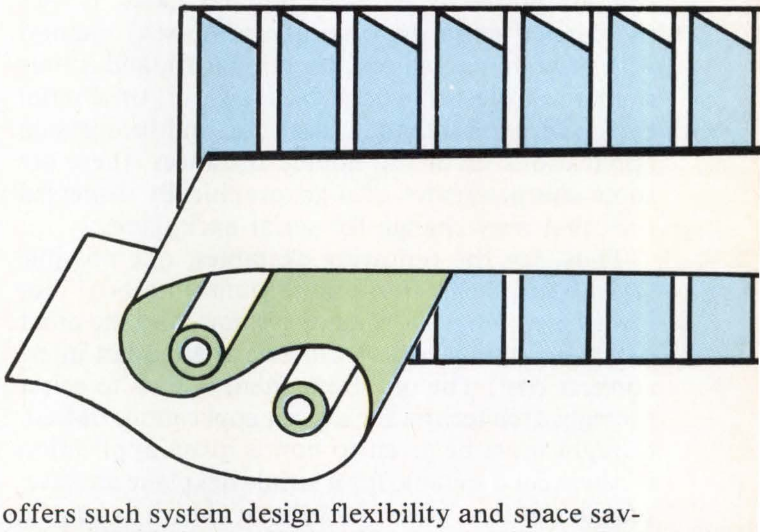

offers such system design flexibility and space savings is that it is usually implemented using as few as one or two signal paths.

A serial backplane architecture also carries considerable software advantages. The serial link allows each subsystem to enforce a standard protocol for communications between system functions. Thus, better software modularity is provided because the hardware architecture tightly controls interaction between modules. Each subsystem gains the same level of autonomy as the nodes in a distributed network architecture. The structured subsystem interface thus allows capabilities to expand with a minimum amount of system modification.

The potential benefits of the serial backplane architecture in a real system are achieved through careful architectural design. Once a serial backplane architecture is adopted, the system becomes a miniature local area network (LAN), with all its potential benefits and problems. It is careful consideration of LAN trade-offs that helps to maximize the efficiency of a serial backplane architecture and to avoid unnecessary limitations.

Considering the two possibilities

Two different data communication philosophies provide a comparison of two possible serial backplane architectures. Although other basic serial backplane architectures are possible, the two examined here illustrate contrasting system goals. These two examples are also attractive because VLSI support is already available.

The first approach defines a network with a master station that controls all data flow. This master generally imposes a sequence in which each station gets a chance to use the data channel. Many multipoint protocols use such a control structure since VLSI advances have made this architecture simple and inexpensive to implement. This architecture usually works well in applications with low to moderate traffic, and where there is a need for centralized control.

The second approach to serial backplane architecture more directly parallels popular LANs. It uses the carrier sense multiple access (CSMA) method with or without collision detection (CD), and is thus similar to Ethernet in concept. However, since serial backplanes are intended more for multiprocessing applications involving limited distances, there are some characteristics of a geographically dispersed LAN that may change for serial backplanes.

Thus, for the following examples, one possible serial backplane offers "multipoint-in-a-box" for low to medium performance systems, and the other offers much higher performance at a modest interconnect cost. The question, then, is how to select the right architecture for a given application. Indeed, thought must be given to how a given application is determined suitable for a serial backplane architecture in the first place. In light of this, it is helpful to consider two specific examples and decide on a design approach for each.

Many laser printer systems use a central controller that is often a multiboard-embedded computer designed on a parallel backplane with a maze of wiring harnesses to interconnect sensors, switches, and servo loops. This application demands a serial backplane. Control intelligence is needed at several spots (eg, the control panel, paper feeder, laser control, and sorter). However, computational needs at these locations are small. By contrast, most of the system's computing power is used to process the images it receives (either electronically or optically) into a form suitable for driving the printing engine [Fig 1(a)].

In this application, cost is a key consideration, while the performance of the serial backplane itself is less important. The first architecture discussed seems most suitable, with the main processor controlling slave microcontrollers at each key point in the system. The Intel 8044 is a good choice for the slave controllers since it contains a complete 8051 microcontroller plus a high level data-link control/synchronous data-link control (HDLC/SDLC) compatible serial port all on one chip. An 82530 (in HDLC/SDLC mode) on the main processor board will control the network of 8044s [Fig 1(b)].

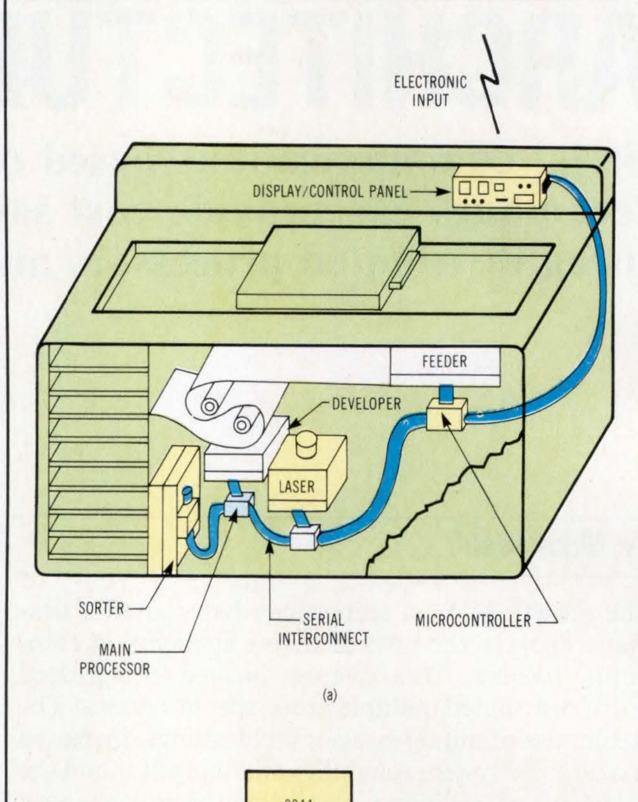

Fig 1 Pictured is a copier architecture using the master/slave approach (a). The 82530 serial communication controller (SCC) controls use of the data channel (b). Traffic is generally low in volume, consisting mainly of commands and status exchanges.

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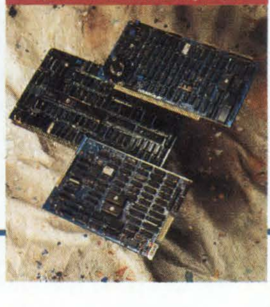

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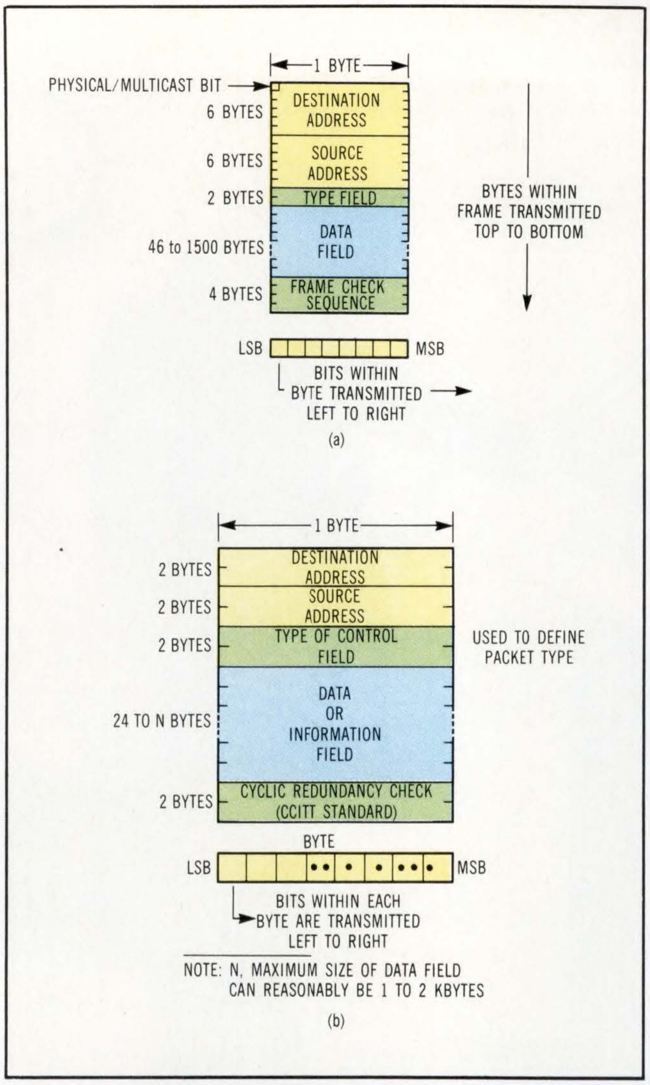

Fig 2 In the realm of the serial backplane, certain changes in the Ethernet frame format (a) can be modified to improve performance. The backplane frame format (b) has been reduced by at least 10 bytes.

The automatic mode of the 8044's serial channel allows each of the microcontrollers in the system to simply update its status message periodically in onchip memory. When a poll from the main processor is serviced, the status packet is sent automatically by the onchip DMA channels of the 8044. The communication protocol for this application is a standard SDLC loop mode supported by both the 82530 and the 8044.

The serial backplane in this architecture requires medium speed data exchanges on the order of 1 Mbit/s. Most messages transversing the link will be relatively short (ie, generally status exchanges and commands). Large blocks of data, such as files, do not usually need to be sent from the central processor to the attached subsystems. The 1-Mbit/s speed is convenient because it is well below the 8044's top speed of 2.4 Mbits/s. It still gives enough bandwidth to support many subsystems, however, and allows use of a standard Manchester encoder/decoder chip that runs up to 1 Mbit/s. As an interconnect structure between the boards, a shielded twisted pair should perform well to 1 Mbit/s over these distances.

This implementation achieves several goals previously mentioned. It provides cost savings in both design and system assembly. A single 8044 component can control the subsystem as well as directly support the serial backplane. The modular design lets new or different subsystems be added with minimum changes in the main processor software, and little or no changes in the other subsystems. This is because they run independently and asynchronously.

In addition, the system is more reliable since a single point failure has less chance of bringing down the entire system. Duplication of the serial backplane itself prevents a single point failure from halting system operation. In fact, if fault tolerance is a key design goal, redundancy is easier to design into a serial backplane architecture. The very nature of the architecture automatically isolates hardware subsystems.

The advanced workstation

Today's advanced personal workstations place a tremendous load on any single microprocessor. Local data rates within a system tax the bus bandwidth of even bit-slice machines. For a design that uses a high resolution bit-mapped display, a hard disk for local mass storage, a high speed LAN interface, and the usual assortment of lower speed I/O, available system bandwidth is often not wide enough to provide a reasonable response. In this case, the serial backplane could help. First, it would improve system performance at low cost by adding multiprocessing capability. Second, it would allow improvements and changes to be made as technology advances, without discarding the overall system design. This is because the final architecture would be more modular.

Key to a successful design is the functional partitioning of system tasks. If subsystems are incorrectly grouped, the serial backplane becomes just another bottleneck. For example, little is gained if one processor is devoted to editing, but then has to send complete bit-mapped screens to the display processor. Transactions between subsystem processors must be at a higher level than this in order to realize the system's full value.

Ethernet is the starting point for the serial backplane model. Fig 2(a) shows the Ethernet frame format and parameters. A quick look at Ethernet parameters reveals some possible changes that can help a peer protocol serial backplane improve performance and simplify implementation.

Xerox Corp studies show that in an Ethernet with 100 active stations, collisions occur far less than 1 percent of the time. In addition, a short-topology network has an even smaller collision window. The collision window is the time interval from the time that a transmitting station begins to insert data on the link until all other stations on the link detect the

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transmission and wait (or defer) to the busy channel before they attempt to transmit. This window is controlled in large part by the round-trip propagation delay of the network medium. For Ethernet, the round-trip, worst-case propagation delay of the network is about 45 μs. For the serial backplane, the time is less than 50 ns, including driver propagation delays (assuming that the total distance the backplane covers is 10 m or less).

This delay factor can prove advantageous in a serial backplane architecture when using the CSMA method without CD to simplify the hardware. In addition, for such short distances, cheap coaxial cable can be used to couple the boards to the coaxial within the same chassis. In this way, the 10-Mbit/s throughput of Ethernet can still be realized while cost and complexity are significantly reduced.

Other Ethernet parameters can also be optimized for the serial backplane. Ethernet defines two 6-byte address fields in order to uniquely identify any host that will ever be connected to the network. In a single system where a serial backplane is used, it is unlikely that more than 64,000 boards will reside in one system, no matter how large. Thus, the address fields can be reduced to 2 bytes each for source and destination. Likewise, the cyclic redundancy check (CRC) can shorten the polynomial to the International Consultative Committee for Telephone and Telegraph (CCITT) 2-byte standard used by HDLC. The serial backplane should have a low inherent error rate, and the CCITT polynomial is sufficient, even on noisy dial-up lines. In order to use standard Manchester encoder/decoder chips, a frame preamble shortened to 16-bit times will be retained. This is sufficient to achieve receive synchronization, since losing preamble bits through repeaters is not a problem. The final frame format for this example is shown in Fig 2 (b). This format should serve many serial backplane applications well. However, the design tradeoffs made to arrive at this frame format are by no means all inclusive.

The CSMA serial backplane can be implemented with the 82586 LAN controller chip. To use the access method and frame format described above, the 82586 is reconfigured from software (on power-up the chip defaults to standard Ethernet parameters). The backplane can run at the full 82586 serial rate of 10 Mbits/s, and still use the 82501 Manchester encoder/decoder chip to drive each board's backplane interface. Low cost coaxial cable will be used for the backplane itself, with a simple dc-coupled transceiver joining the 82501 to the coaxial, and providing full-duplex passage of data (Fig 3).

If fault tolerance is a key design goal, redundancy is easier to design into a serial backplane architecture.

To realize the performance goals for this workstation, dedicated processors are provided for each main task (Fig 4). The display control board is dedicated to building and controlling screen images, and provides high level display services to other system processors. Another processor is dedicated to handling the keyboard, mouse, light pen, digitizing tablet, and whatever other user input devices are provided. Since the boards can have entirely different form factors, this board can easily be embedded within the keyboard enclosure and attached by the serial backplane coaxial itself.

A third processor controls the disk subsystem. In addition to handling normal data flow to and from the disk, this board can offer such features as full track buffering, lookahead cache capability, automatic write/error reallocation, and translation of logical filing conventions to a variety of mass-storage formats. An edit processor coordinates document editing as well as tasks not otherwise mentioned. As system needs grow, or special high performance tasks

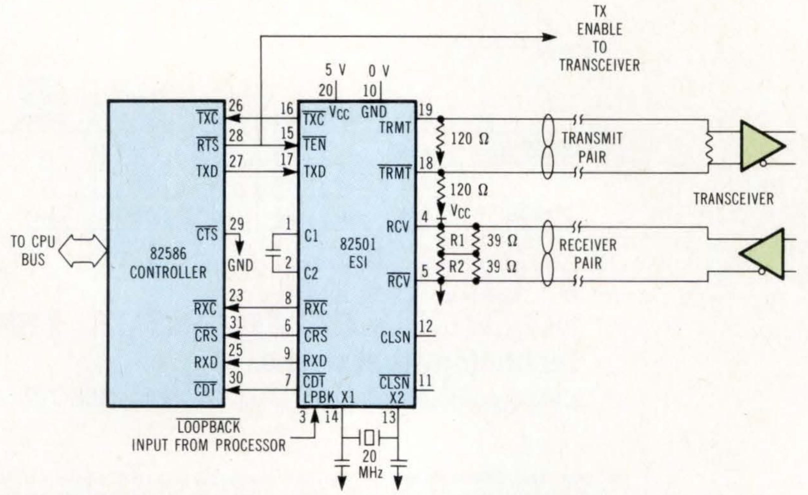

Fig 3 In a serial interface for a carrier sense multiple access (CSMA) serial backplane using the 82501 Manchester encoder, the interface can run at a serial rate of a full 10 Mbits/s.

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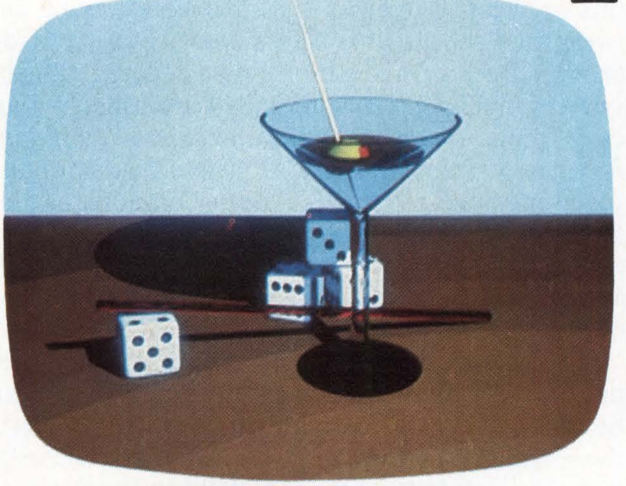

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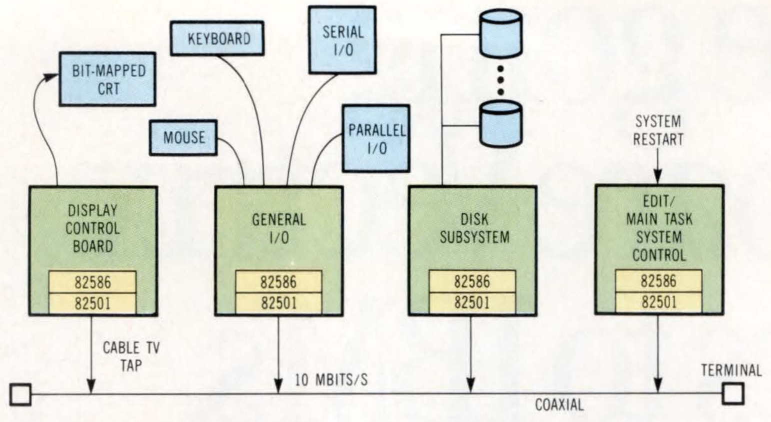


Fig 4 In this workstation block diagram, the modularity of the approach allows different functions (on boards of different form factors) to be added and modified without affecting the overall design.

are needed, other processors can be added to fulfill particular applications. The communication protocols, however, must be carefully designed to ease distribution of additional system tasks.

Identifying software needs

Once the hardware is defined, the serial backplane will have some special software requirements. Most systems would use fairly diverse application software, so the software examined here is only that common to serial backplane communications. The communication protocols should be simple to design and use, ensure reliable transport of data throughout the system, and be easy to extend and enhance.

Serial communication systems have a set of standard protocol models defined to accomplish these goals—the Open System Interconnection (OSI) reference model, which is the International Standards Organization (ISO) architectural model for open systems. The physical and data-link protocols already discussed roughly adhere to this model. The network layer will be simply a place-holder, in case multiple backplane need to be connected into one network in the future.

Focusing on the transport and presentation protocol layers helps to round out the protocol discussion. The intervening session layer defined in the ISO model may not be needed in all systems. This model is based mostly on time-shared communication needs where the concept of a session is important. Fig 5 shows how these protocols fit within each subsystem. They are primary tools needed to ensure a reliable structure for data exchange among the system elements. The frame format shown in Fig 2 serves as a foundation for the additional control fields necessary for the transport layer, and finally for a general-purpose presentation level protocol.

The simple transport protocol (STP) selected for this application creates transient connections between two subsystems. These connections provide an error-free, ordered path for data between the subsystems involved. Certain fields are defined within each frame to control the connection [see Fig 6(a) for the full frame definition]. These fields provide functions similar to the European Computer Manufacturers Association (ECMA) 72 transport protocol proposal or the Intel iNA-960 transport protocol. Where possible, the size of these control fields has been shortened to minimize packet overhead.

The type field in each frame uniquely identifies packet type, one of which is STP. Other types can be added as needed to define other protocols. Next, the length field defines the total length of the packet from the first byte of the type field to the last byte of the data field. This field is included for convenience because it allows the process that fills or transfers

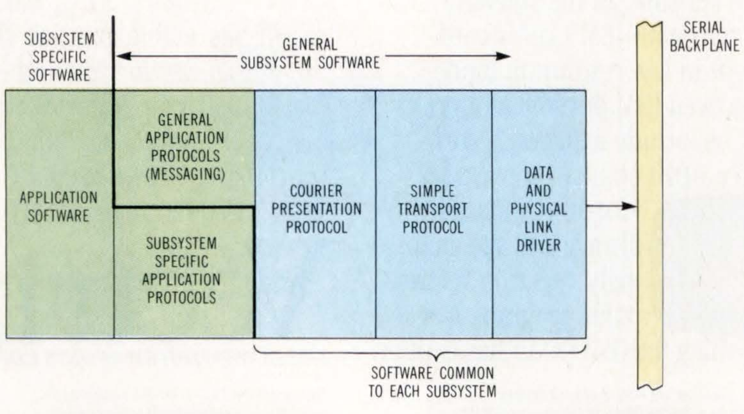


Fig 5 Shown is a system software architecture. Matching a specific application to the protocols common to each subsystem need not always involve the International Standards Organization (ISO) session layer. Application-specific protocols can often be matched with general-application protocols to do the job.

data field information to avoid lengthy calculations. Control of this field in the communication protocols makes it easier to predict the length of transmissions.

The source and destination ID fields uniquely identify a connection. They are generated during the first packet exchange across a new connection. The source ID number is entered by the subsystem making the connection, and the destination ID number is returned by the other subsystem in response to the connection request. These two IDs are then used by the two subsystems for the duration of the connection to distinguish this connection from any other that might arise between them. Connection IDs prevent destructive regeneration of the connection in certain error situations.

For example, if one subsystem processor crashes and then restarts during a connection, the failed processor could mistake an incoming packet as the start of a new connection and return a new connection ID in response to that packet. The other subsystem would receive a response with a new and incorrect destination ID number, react as if the previous connection had terminated abnormally, and take recovery steps such as restarting the previous data exchange. Without connection IDs, this error situation would not have been detected.

The sequence number field counts and orders frames transferred during the connection. The count is set to 0 at the start of the connection and incremented for each packet sent. Overflow of this field is ignored; it simply rolls to 0 and begins incrementing again. The receiving subsystem uses this field to determine the proper order in which packet data should be reassembled. In addition, it can delete any duplicate packets that are received due to retransmit time-outs.

The acknowledge number field acknowledges receipt of packets. The number placed on return packets indicates that the receiving subsystem has successfully received packets with all sequence numbers up to and including the number in the acknowledge number field.

The final STP byte defines special control fields. The receiving station uses the buffer allocation portion to tell the transmitting station the number of free receive buffers it has available at any time. This information can help optimize the throughput of the connection. The transmitting station can send this number of packets prior to receiving any acknowledgment of outstanding packets.

The expedite bit of the control field can be used for emergency or special message packets that the sending station wants the receiver to process, prior to any other

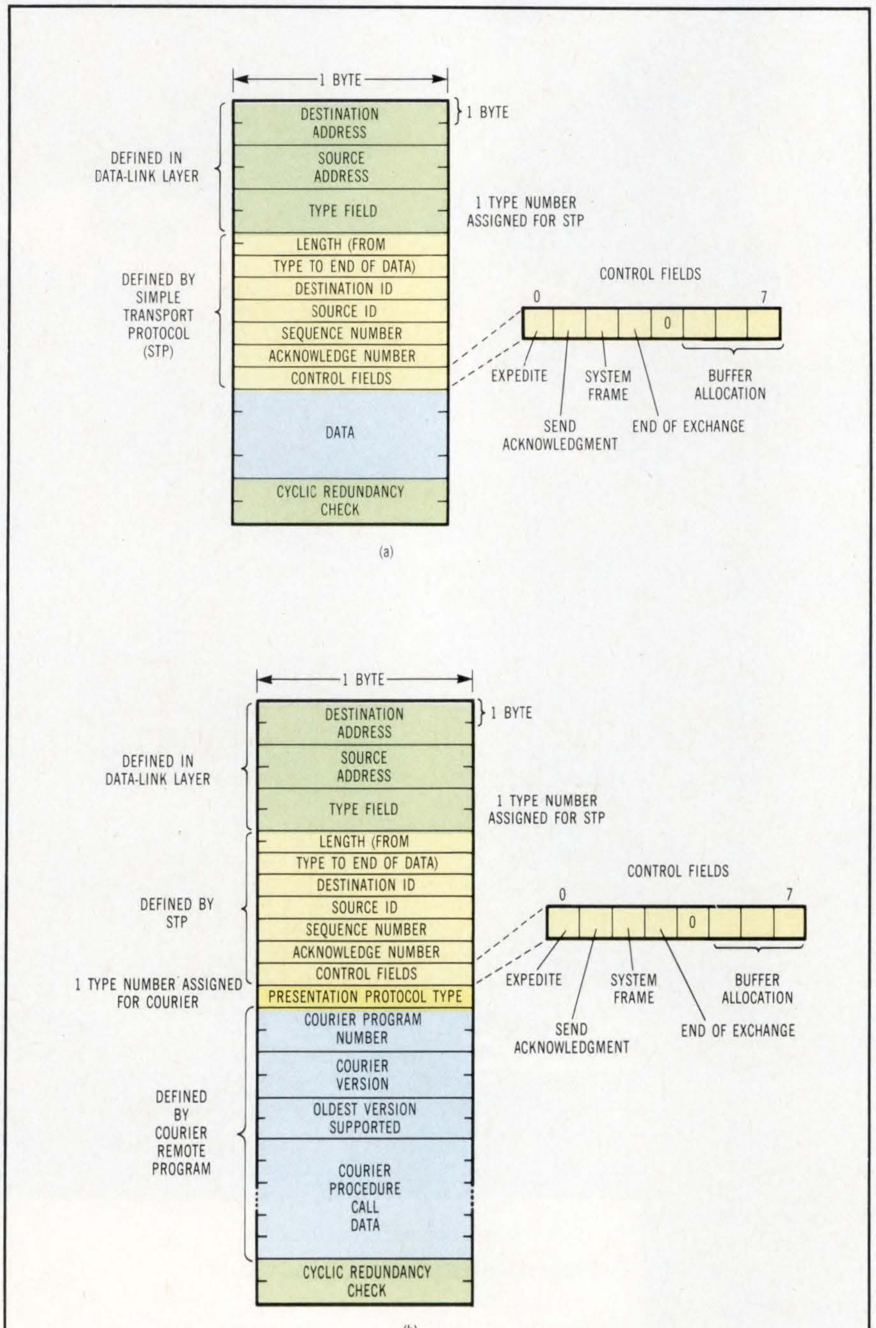
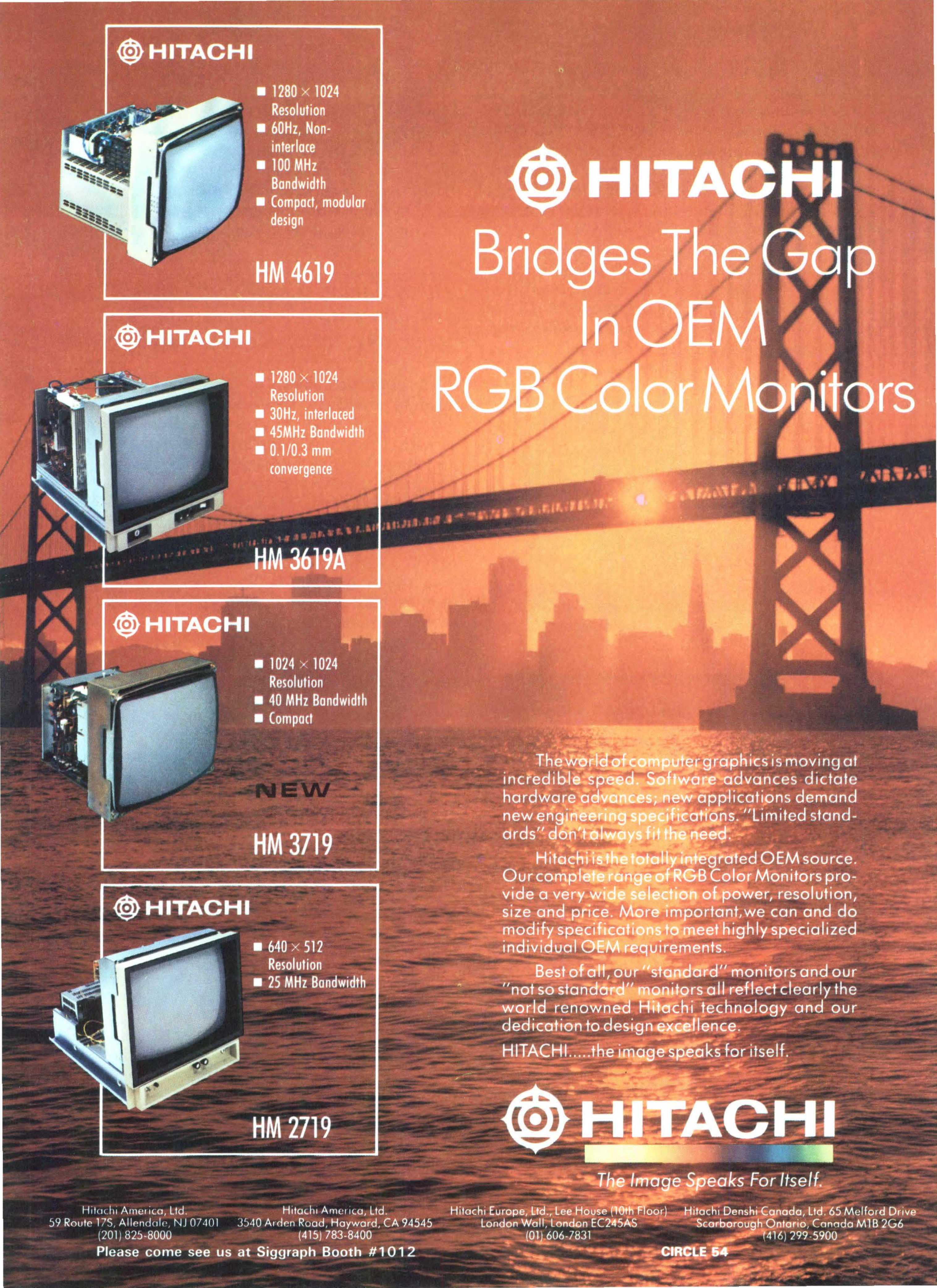


Fig 6 The complete serial backplane frame structure (a) includes the data-link and transport protocol layers adapted from Ethernet. The Courier call (b) also includes a protocol defined by the Courier remote program.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packets in the receive queue. The send acknowledgment bit can be used by the sending subsystem in cases where it requires immediate acknowledgment of a particular packet's reception. The system frame bit can be used to mark frames that may flow between subsystems, to request frame acknowledgment, or to do other housekeeping chores. This bit indicates that the frame is for system use only, and contains no data traffic. The end-of-exchange bit is provided to support higher level presentation protocols and allows such protocols to mark logical breaks in their messages. This transport protocol provides the necessary support to ensure reliable, ordered delivery of frames between two subsystems.

The final protocol provides order to the data structures transversing the connections. The goal in designing such a presentation level protocol (PLP) is consistency and speed. Having a defined order and type for data structures, such as numbers or strings, means that all subsystems will understand and use the same bit patterns for the same data objects. Also, this type definition speeds the creation of application-level protocols in much the same ways as high level languages speed the development of code by providing more functions per source line.

Courier, the Xerox PLP, provides the framework for this serial backplane PLP. The key difference between Courier and PLP is the interface between the transport protocol and PLP. In Courier, this interface assumes the Xerox sequenced packet protocol is the transport protocol. Since the transport protocol is STP, the interface is modified accordingly. No socket field is defined in STP, so a connection is established by the sending of the first Courier packet. In addition to the Courier version number information exchanged in this packet, the first data word of the new connection data field contains an arbitrary number identifying the packet as a Courier packet.

The resultant system architecture provides a high level, flexible framework for application development.

This ID number allows other communication protocols to be added to the system at this level without disturbing or modifying existing Courier applications. The example application uses the Courier definitions of data types, some of which may be modified for particular applications. For instance, the string definition includes a greatly extended character set that may not be necessary in many applications. The end-of-message bit used by Courier to delimit messages is not present in STP. The end-of-exchange bit is in STP and can serve the same function. When this bit is set, it signals the end of the current Courier message.

An example of a data exchange between subsystem elements is taken from Appendix D of the Courier specification. The edit processor needs a page from a file called "Data" to merge into a letter. Appendix E of the Courier specification shows the actual Courier messages involved in opening the file and reading the page. Fig 6(b) shows how the Courier exchange is integrated into the packet structure previously defined.

The resulting system architecture provides a high level, flexible framework for application development. The communication protocols that reside on each system processor allow rapid distributed system development. The 82586 LAN controller provides sufficient configurability and throughput to support such an architecture.

These two examples illustrate some of the potential recently made practical by VLSI component developments. The serial backplane provides excellent support for advanced system design: multiprocessor, functionally partitioned systems are easy to build and modify. The serial backplane provides many of the same benefits offered by LAN distributed architectures.

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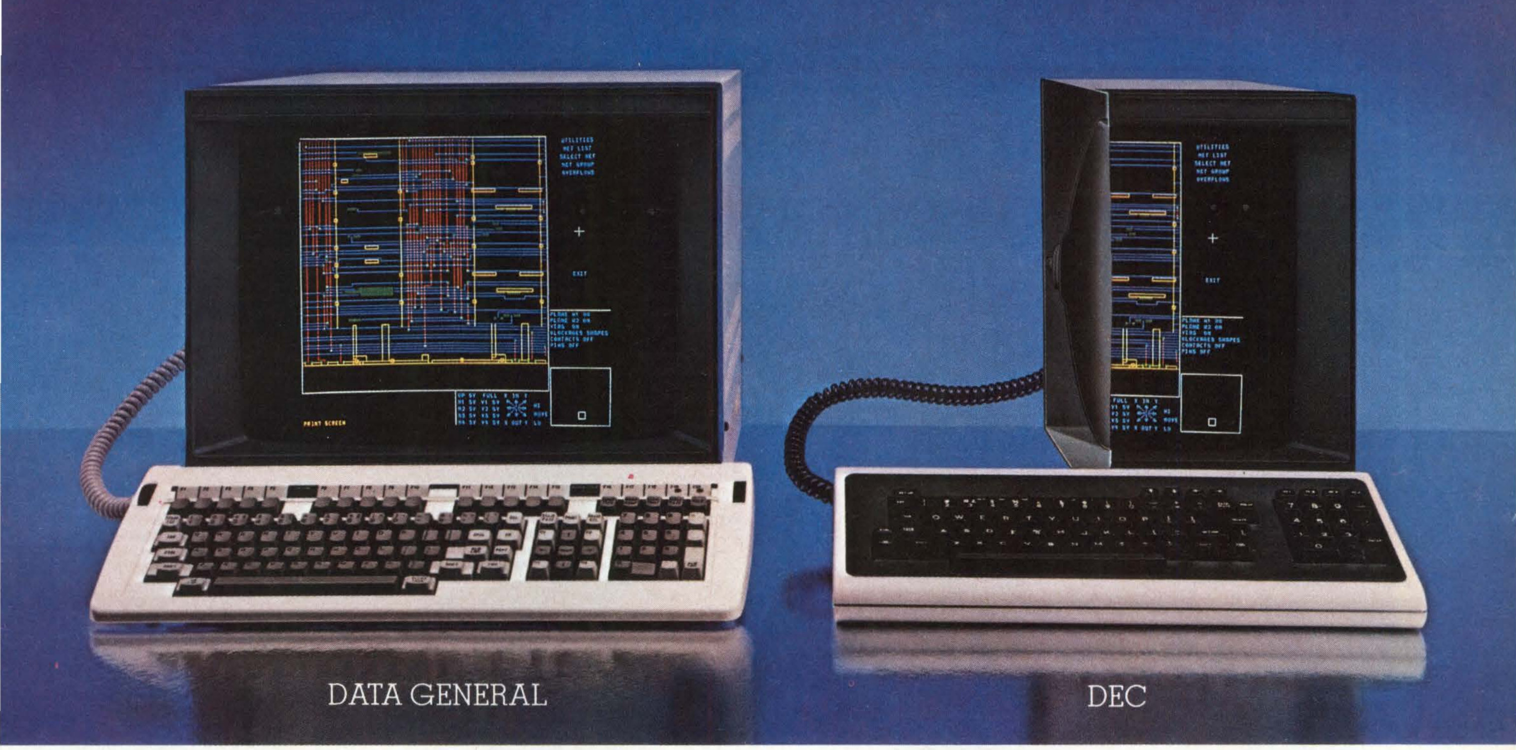

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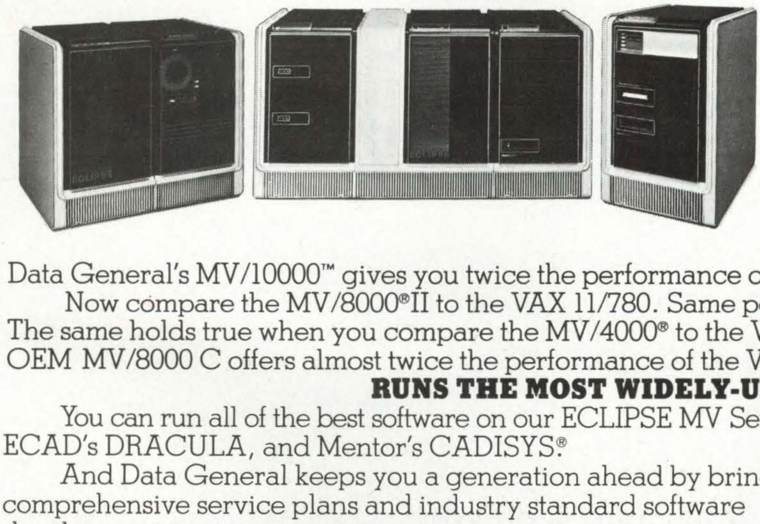

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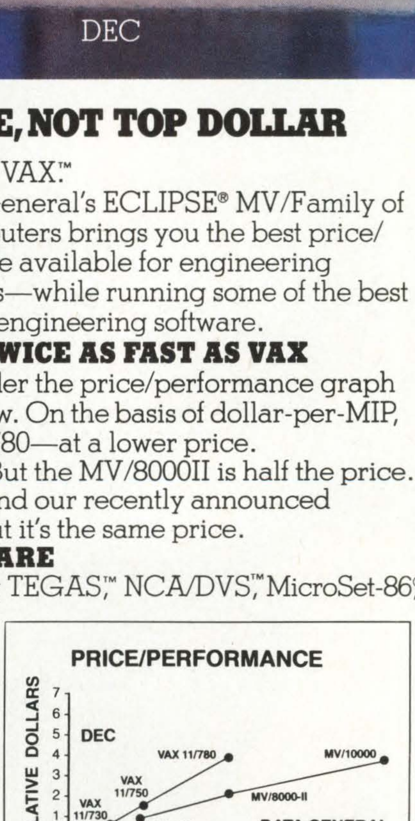

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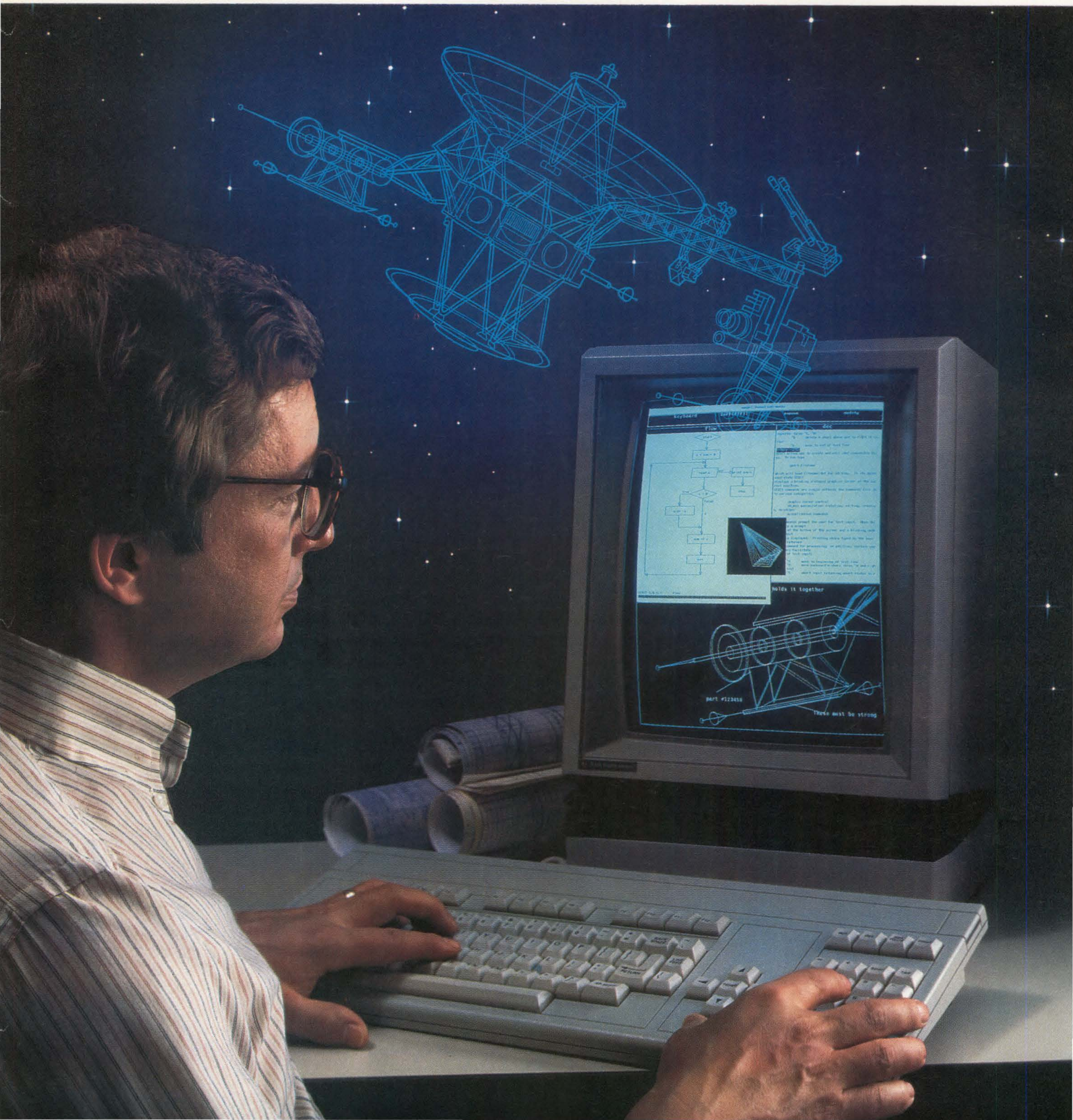

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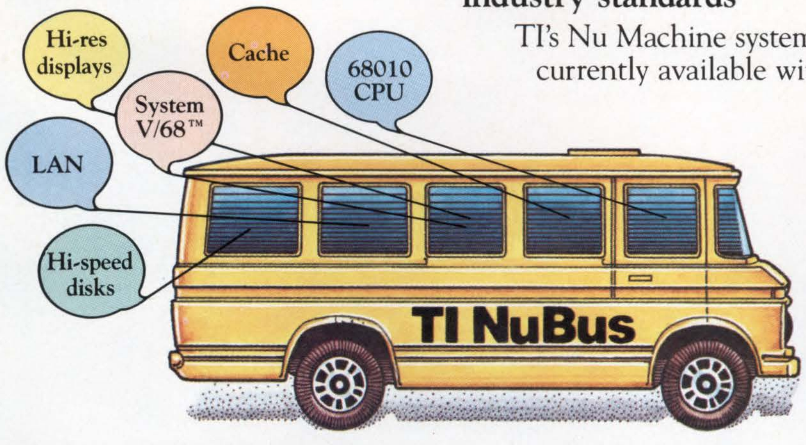

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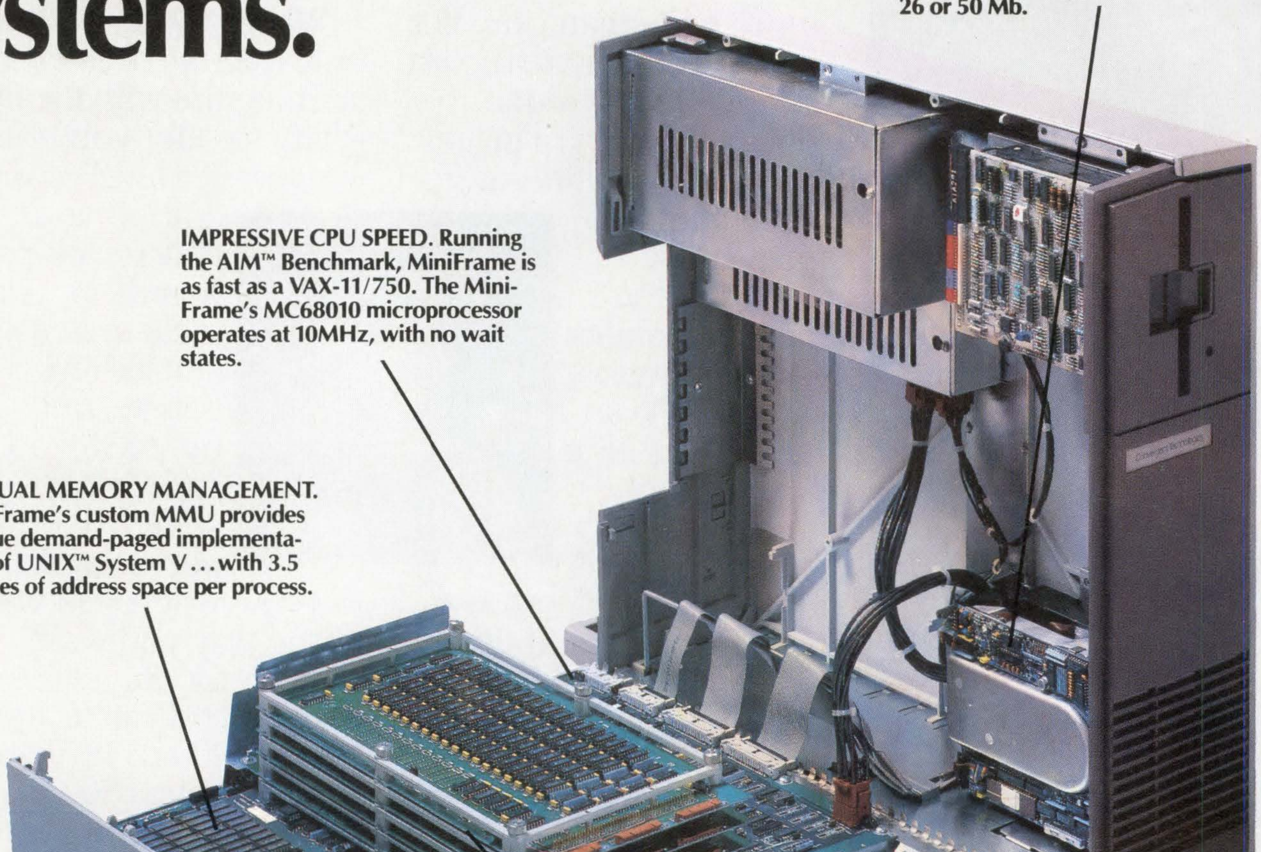

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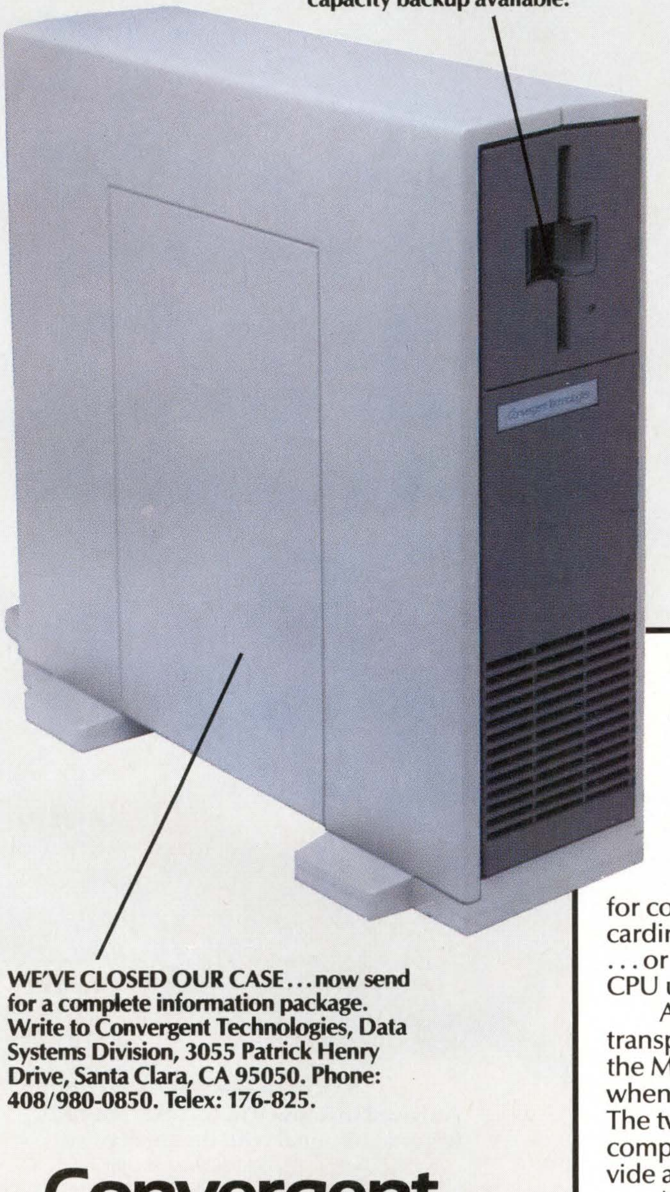

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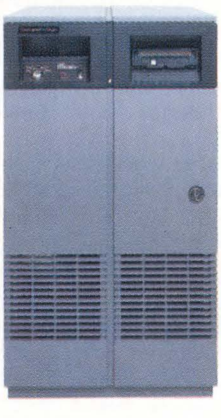

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CIRCLE 60

INSTRUCTIONS ADD FLEXIBILITY TO BIT-SLICE DESIGN

Elegant microcontroller frees designers to emulate architectures with variable word lengths.

by Kaare Karstad

Microcomputers fall into two general classes: single-chip microprocessors and microprogrammable bit-slice machines. Single-chip processors have a predefined and unchangeable word-length architecture, and a fixed instruction set. Microprogrammable bit-slice microprocessors, on the other hand, can be configured to provide a wide variety of digital system architectures with various word lengths and instruction-set capabilities. For some applications, the bit-sliced microprogrammable approach provides the only practical means of achieving special features and high throughput rates.

Perhaps the most exciting feature of user microprogramming is the ability to emulate other machines. Changing the microroutines or substituting another microprogram memory alters the functional complexity of the machine. This enables execution of a completely different set of macroinstructions and the ability to tailor this set to specific applications because of its new architecture.

The microcontroller (or sequencer of the control section) is what determines whether emulation will be easy or practical. The control section of a microcomputer has two parts: the microprogram memory, which holds the microinstructions; and the microprogram sequencer, which presents an address to the microprogram memory so that a microinstruction can be fetched and executed.

Kaare Karstad is a member of technical staff with RCA's Solid State Division, Route 202, Somerville, NJ 08876. He holds an MSEE from Norway's Institute of Technology.

One controller that incorporates many of the subsystems and capabilities required to affect the control section of a bit-slice CPU is the emulating microcontroller (EMC) chip—GP501. Features of the EMC facilitate interfacing to the GP001—an 8-bit register and arithmetic logic unit (RALU) in the same emulation programmable IC (EPIC) family. Although both parts are fabricated in CMOS/silicon on sapphire (SOS) technology, the EMC can be used with bit slices of other processing technologies.

Under EMC control

A large number of registers, latches, and counters are implemented on the chip. Most of these are under explicit EMC program control. Of the registers, five are operation registers (R0 to R4) dedicated to specific functions such as masking, mapping or saving common reentry points (Fig 1). Of these, R0 and R1 are pointers to reentry points that can be given control directly or conditionally. R2 has a pair of 4-bit mapping registers that can be used to transfer execution to one of 16 micromemory locations. R4 is an address masking register and R3 is a maskable address register that can be loaded from microcode or from the external bus.

The microprogram counter is one of four registers pointed to by the stack pointer and is usually adjusted during the current microcycle so that it points to the next address at all times. The four stack registers permit three levels of microcode subroutines and are able to wrap around in either direction. User control of the 2-bit stack pointer is established via reset input and through pushing or popping the stack.

The EMC provides explicit unconditional branch and unconditional branch-and-link instructions for direct sequence control. In addition, the EMC offers a variety of other sequence control options, which

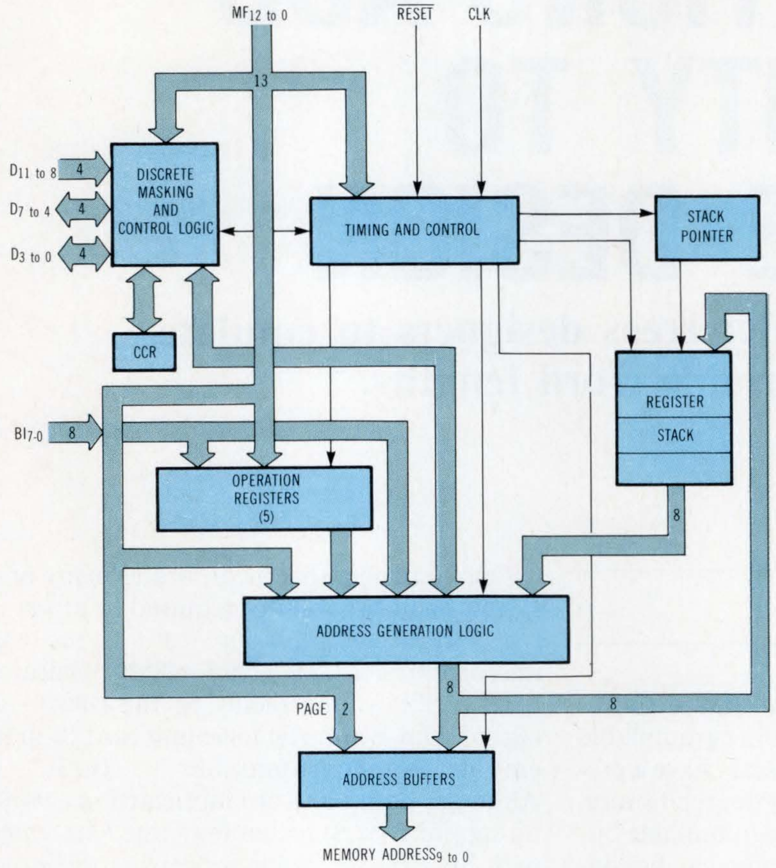

Fig 1 The internal logic structure of the emulating microcontroller (EMC) incorporates most of the subsystems and capabilities required to affect the control section of a bit-slice CPU into one part. A 13-bit control word generates the next 10-bit micromemory address. The address is formulated from inputs at the interface and internal registers as instructed by the control word.

can be used in conjunction with counters and conditional discrete features.

The EMC's two 8-bit counters can be used either to count clock cycles while following normal program flow (sequential counting), or to dwell on a particular instruction while counting clock cycles (iteration counting). The two counters can be nested. The conditional discrete feature provides a means by which bits may be tested and the result used in combination with branching options to provide a conditional two-way branching capability.

The EMC's mapping feature provides a 256-way branch. Values can be sampled at the bus interface, masked, and merged with other values stored internally, then used to generate the new memory address output (Fig 2). This eliminates the need for external mapping and/or interrupt vector ROMs/programmable logic arrays (PLAs), as with a 2910 implementation. In addition to the regular mapping feature, translation allows values at an internal data latch or at one of the 4-bit-wide discrete interface groups, which typically reflect machine or ALU status, to be masked and merged with the current microprogram counter. This feature provides a 16-way relative branch that is based on the current machine state.

The two main goals of the EMC device design are to minimize and/or eliminate control circuitry, and to emphasize efficient use of micromemory. Generally, the controller contains all the required functions, together with the microprogram memory, necessary to implement the control section of a computer. However, there is a trade-off in systems between execution speed and size of micromemory. The faster the machine, the larger the micromemory and the less time wasted in linking common microcode. A fast machine also implies horizontal encoding of the microword (eg, many bits in each word). In an LSI system, the number of micromemory chips has a dominating effect on cost. This, in turn, provides additional incentive to find a controller that uses micromemory efficiently. The GP501 is designed for low subroutine linkage overhead.

Meeting design goals

These GP501 design objectives are met at some sacrifice in understanding and use of the controller. In fact, some of the GP501 instructions may seem complex at first and require a longer learning cycle, but emulating design programmers will find the time and effort worthwhile (see Panel, "It's all in the instructions"). However, where micromemory

requirements are large, the simpler GP502 sequencer is the appropriate choice (see *Computer Design,* Mar 1984, p 213).

At first, some of the GP501 instructions may seem unfamiliar to many programmers. However, it is important to remember that the purpose of any controller is to generate a next microprogram address. The GP501, for instance, has in its first two instructions, an 8-bit field that is an immediate address field. This is directly reflected on the output. In the remaining instructions, the output is an address, which is formulated or computed based on the content of the 8 LSBs in the control word. The output result is generally a combination of bits derived from the interface B0 to 17, the D0 to 11 and/or bits stored in internal operational registers. Sometimes the result is modified by an immediate mask in the control word, and in some cases, internal logic operations are manipulated internally.

Thus, all inputs to affect the microcode sequencing are presented directly to the EMC. Meanwhile, the next microprogram address is internally computed and presented at the memory address (MA) output pins. However, when the reset is active, control word commands are inhibited, with the exception of the load command. This makes it possible to load all addressable internal registers with the reset input active (eg, complete initialization of the EMC while a device reset condition exists).

Assigning commands

The load command sets the EMC's operational registers. Among the addressable registers, only R3, the condition code register (CCR), and the counter-holding registers are altered by other commands. Registers are generally set during initialization. After that, the load command is used to load the counter-holding registers and the CCR, as well as to manage the contents of the branching registers R0 and R1.

The branch (BR) and branch-and-link (BAL) commands provide direct control over microcode address generation. They are the only instructions that pass control word data directly to the address output. The BAL command is the simplest means of invoking subroutine calls. It is used to execute frequently used sections of common code that are only stored once (eg, the normalization routine used by all floating point macroinstructions).

The map command generates branch addresses according to values present at or recorded earlier from the bus input port. This initiates microcode entry points for macrocode instruction execution and interrupt service. Thus, latching bus data in register R3 allows multiple referencing of the same piece of data. The map command can be used for vectoring, but not for relative branching.

The translate command is similar to the map command in that it modifies program flow according to values generated outside the EMC. However, unlike the map command, translate uses stack register values in address formulation. Thus, relative branches are possible, based on values present at the discrete interface. Processor flags and other status indicators are normally interfaced to the I/O pins.

Translate commands are divided into two groups. The first group updates the currently active stack register and affects a one-time, n-way relative branch. The second group does not update the stack

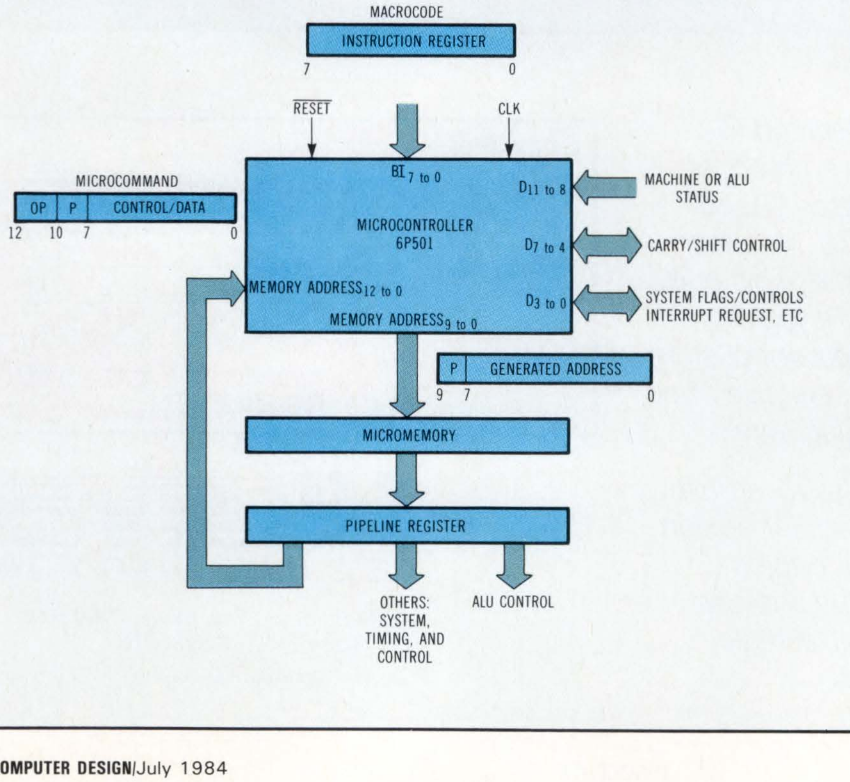

Fig 2 With a GP501-based control section, mapping is typically established by extracting the machine instructions opcode directly at the interface. The opcode is masked and merged with other internally stored values to generate the new micromemory address output. A 256-way branch is possible. A great number of inputs can provide external direct control of microcode sequencing and subroutine linkage.

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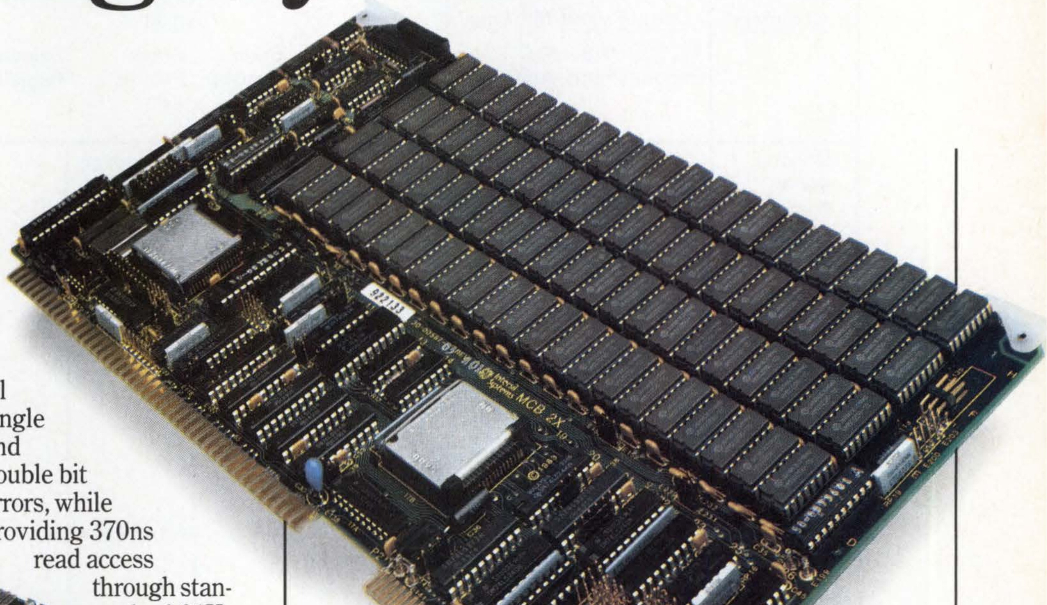

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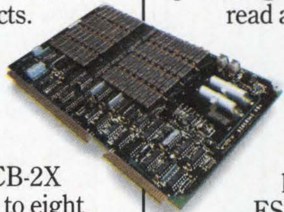

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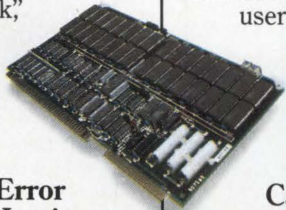

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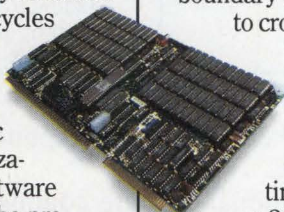

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CIRCLE 62

It's all in the instructions

The EMC uses eight operation codes to perform various functions (see Table). The first two codes implement the branch (opcode 0) and branch-and-link (opcode 1) options. Both of these functions are unconditional and, in both cases, the lower 10 bits are the address of the next microinstruction.

However, while the lower 8 bits are solely incremented and loaded into the currently active stack register in opcode 0, in opcode 1, the stack pointer is incremented prior to loading the incremented microcommand into the stack register. The net effect is that the previously active stack register is left pointing to the micromemory location just past the branch-and-link command. Execution continues until a return causes the controller to pick the next address from the previously active stack register.

The control and mask fields in the map command (opcode 2) formulate a new 8-bit address, using some combination of the value present at the bus interface, the value in register R3, or the mapping register R2. This is done according to a table of 16 choices. Immediate mask data is used as a mask for the high nibble of the new address or as a bit-selection map when pplied to the low nibble via a right justify function.

The translate command (opcode 3) determines if the currently active stack register is updated or not, using

The Eight Operation Codes in the 13-bit Control Word

Command	Control word MF $_{12-0}$ 12-10 Opcode	9-8 Page	7-0 Address, Control, Mask, etc	Result: Memory Out MA $_{9-0}$	Stack Register (SR)	Stack Pointer (SP)	Selected Register	Flag	Comments
Unconditional branch	000	P	Address	P: Address	MA $_{7-0}$ +1	No change	—	—	—
Unconditional branch and link	001	P	Address	P: Address	MA $_{7-0}$ +1	SP+1	—	—	Currently active SR is not changed
Map	010	P	Control / Mask	P: Formulated address	MA $_{7-0}$ +1	No change	—	—	Formulated address from some combination selected by control value of bus in register R2, register R3 and immediate mask
Translate	011	P	Control / Mask	P: Formulated address	MA $_{7-0}$ +1	No change	—	—	Formulated address from some combination, selected by control value of current SR value at discrete interface, register R4, immediate mask and CCR. No SR update if C=4-7 and C-F
Load	100	P	Register / Data	P: SR	SR+1	No change	Data	—	Active also during Reset
Conditional discrete setup	101	P	E / S / Mask	P: SR	SR+1	No change	—	CD Set	Equation select (E), data source select (S), and mask are recorded. Data source is discrete interface or CCR. Testing via opcode 7.
Immediate count	110	P	T / Branch / Count	Branch option selected by branch field	Depends on branch	Depends on branch	—	—	T=0 Sequence T=1 Iterate
Sub-op and branch	111	P	Branch / Sub-op	Branch option selected by branch field	Depends on branch	Depends on branch	—	CD Reset	Sub-op specifies one of several discrete interface operations, counter operations or testing of conditional discrete set-ups.

register and is useful in tight iterative routines where one of n functions is executed until some event occurs. An example would be an asynchronous bus with I/O devices and handshake signals. A number of translate instructions could reference each other until the polled I/O device responds or a timeout should occur.

The conditional discrete command is the most flexible of the conditional test operations. The command allows four logical operations—AND, OR, one of 16 control settings. Thus, the new address is combined from the current program counter values at the discrete interface (DI) and/or the content of the CCR. Other control settings apply the masking register R4 or immediate mask values as a bit map using a right justify function.

The load command (opcode 4) allows the value in the immediate data field to be loaded into one of 16 half registers. The next micromemory address comes from the current stack register and is then incremented.

Two bits, MF5 and MF4, of the conditional discrete setup command (opcode 5) select and examine one of four sets of four signals (the CCR, D8 to 11, D4 to 7 or D0 to 3) from the discrete interface. Bits MF3 to MF0 are a mask that determines which of the selected inputs will be subject to a logical operation (bits MF7 and MF6). If the mask is zero, the current CCR is used as a mask. Bits MF0 to MF7 are all latched for later use. Once the command has set up a discrete operation, the result of the selected logical function is sampled during subsequent operations.

The immediate count instruction (opcode 6) causes the count value to be placed in the holding and masking registers for one of the two counters, and a count of the type specified is initiated. If MF7 is zero, a sequential count begins. Execution continues in normal sequence until the count runs out. At count equals zero, a flag is set and the next instruction is determined by the branch instruction that was set up in the sequential count command.

In an iterative-type subcommand (MF7 = 1), the count is also loaded into an available counter. However,the branch condition determined by MF4 to MF7 is taken immediately. The microcode instruction that results from the branch is repeated until the word count runs out, and execution continues sequentially from the repeated microword.

The sub-op and branch command (opcode 7) combines two semi-independent operations. One suboperation specifies a utility function, such as a discrete interface operation or a counter operation. The other is a branch operation that samples a conditional discrete equation, like AND or OR.

Other suboperations include various methods of loading the CCR, while another method features a no-op command. Another sub-op loads register R3 from the bus interface. Meanwhile a different one samples the discrete operation that is set up by opcode 5.

The branch option specifies one of 16 possibilities when no discrete is pending, or one of 32 when coupled with the conditional discrete evaluation feature. Opcode 7 stops sampling the result of opcode 5 execution (the latest discrete operation) and branches according to the branch field in the command. Command 7 allows all microcode sequences emulating a macroinstruction to branch the fetch routine and load status into the CCR in one single instruction.

XOR, and XNOR—to be performed on any combination of input lines within a set (D11 to 8, D7 to 4, D3 to 0) or within the CCR. The conditional discrete command establishes the conditions determining whether or not a branch will be created later, but it does not initiate a branch. Moreover, the EMC provides two counters—the outer and the inner. The outer counter is used in the non-nested mode. However, if another counter is invoked during the range of a sequential count, the outer counter stops and the inner one takes over. When the inner counter stops, the outer one resumes counting.

The immediate count command is the simplest way to use the counters. In a sequential count, the branch is taken when the count expires. The action is similar to "do" loops, and hence, nesting is possible. This command is useful in limiting sequences of microcode to a preset number of cycles without wasting time testing in-line limits. Typical uses include multiply and divide macroinstructions, where a known number of translate instructions are executed before exiting. The branch-before-count nature of the iterative count makes it useful for repeating in-line instructions (eg, automatic repetition of a shift-1-bit instruction).

The sub-op and branch command specifies two independent operations within the EMC—a branch and a data/utility function. The data operation is used to input logic levels into the CCR, to transfer data between various lines, and to manipulate the count registers. The branch directive field in the command specifies one of 16 branch possibilities. If there is a conditional discrete operation pending, each of these branch possibilities has a true/false option, thus making 32 branches possible.

Designing for real systems

A real-system application illustrates some of the strong features and advantages of the GP501. Many industry programs use the controller and other EPIC chips in both preproduction stages and current applications. These applications include the NAVSTAR global-positioning system and other military programs. An implementation of the military standard (MIL-STD) 1750A instruction set is the architecture shown in a simplified block diagram (Fig 3). The system provides the full processing capability of a large minicomputer, including floating point arithmetic with double and extended precision up to 48-bit wide data manipulation.

The main elements of the MIL-STD 1750A are two GP501 controllers, and concatenated 8-bit GPU slices (GP001), which form the general processing section. The rest of the necessary interconnect logic and the micromemory is integrated on a few LSI parts.

The advantage of the dual-controller approach is more efficient packing of microcode. With dual-controllers, most macroinstructions can be emulated with only two sequences of microcode. One sequence derives the operand, a register pair, an address, a memory word, etc. The other sequence executes an arithmetic or logical function such as add, AND, or complement. These sequences can then be independently shared with other macroinstructions.

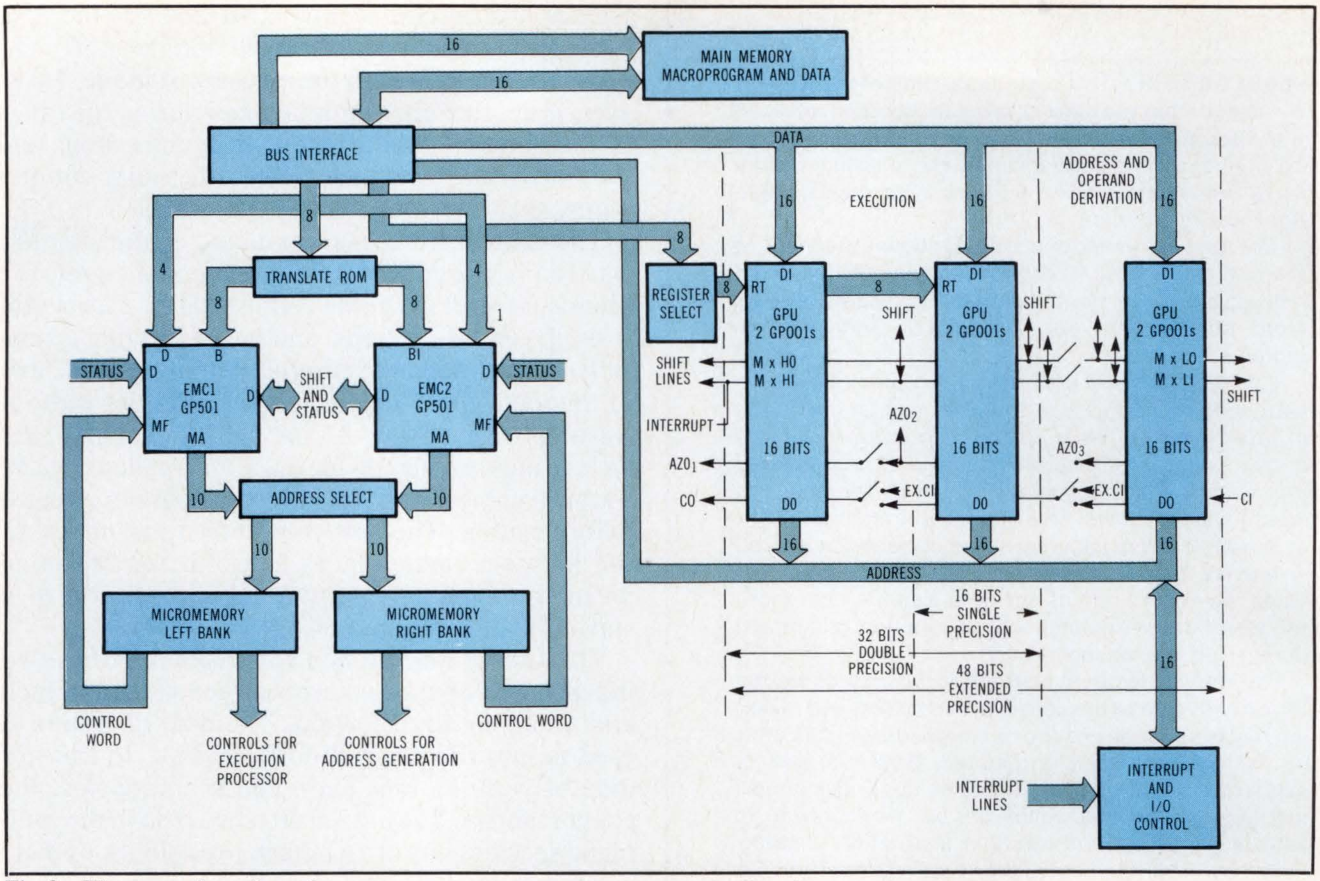

Fig 3 The control section of a 1750A computer uses two GP501 controllers in a synchronized fashion to address micromemory. Concatenated 8-bit ALU slices form the general processing section which comprises an execution part, and an address and operation generation part. Operations can be performed on 16-, 32-, and 48-bit wide data. A few LSI parts tie the whole system together.

Thus, the general processor is divided into two sections; a computational section consisting of two 16-bit subsections, which do 16-bit or 32-bit arithmetic when linked under microcontrol. A third 16-bit group primarily computes addresses and operands. For extended 48-bit precision, the three sections are concatenated. The micromemory is split in half. One bank primarily controls the execution processor, while the other controls address generation, bus, and interrupt control.

When the process after a fetch cycle is initiated, a new macroinstruction enters the CPU via the bus interface unit. The lower 8 bits, which are either operand specifiers or data, load the register select unit. The upper 8 bits are the macro-opcode and address the translate ROM. This is required in order to generate the entry points into the two microcontrollers. The control section uses the 8-bit addresses from the opcode translate memory and microword bit fields to generate right and left address selection data to the address select unit. As discussed earlier, the controllers provide an extensive set of masking and data manipulation functions that allows various combinations of external inputs to be mapped to new micromemory addresses. The address select unit provides the means by which the two controllers synchronize the two micromemory halves.

The processor's arithmetic status—including carry out (CO), accumulator zero (AZO), carry sign, and overflow on lines MXH0 and MXH1—is input directly to the execution controller and updates the internal CCR. The CCR can also output status and thereby build a machine status word. EMC1 is further used to complete a ring shift path for the MX shift lines of the execution processor. The output on the shift lines is tested in the same controller for use in multiple algorithms, which decide when to add, subtract or do nothing.

Acknowledgment

The parts in the EPIC CMOS/SOS family were developed under sponsorship of the USAF Avionics Laboratory. The parts were designed by Tracor Aerospace, Inc and RCA Advanced Technology Laboratories.

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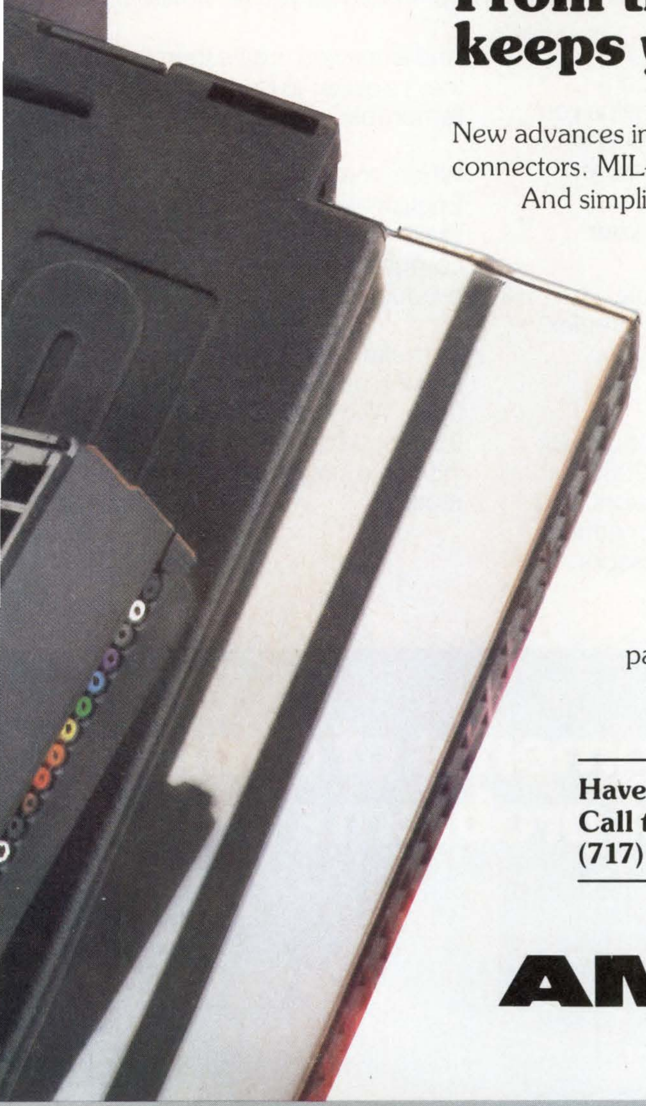

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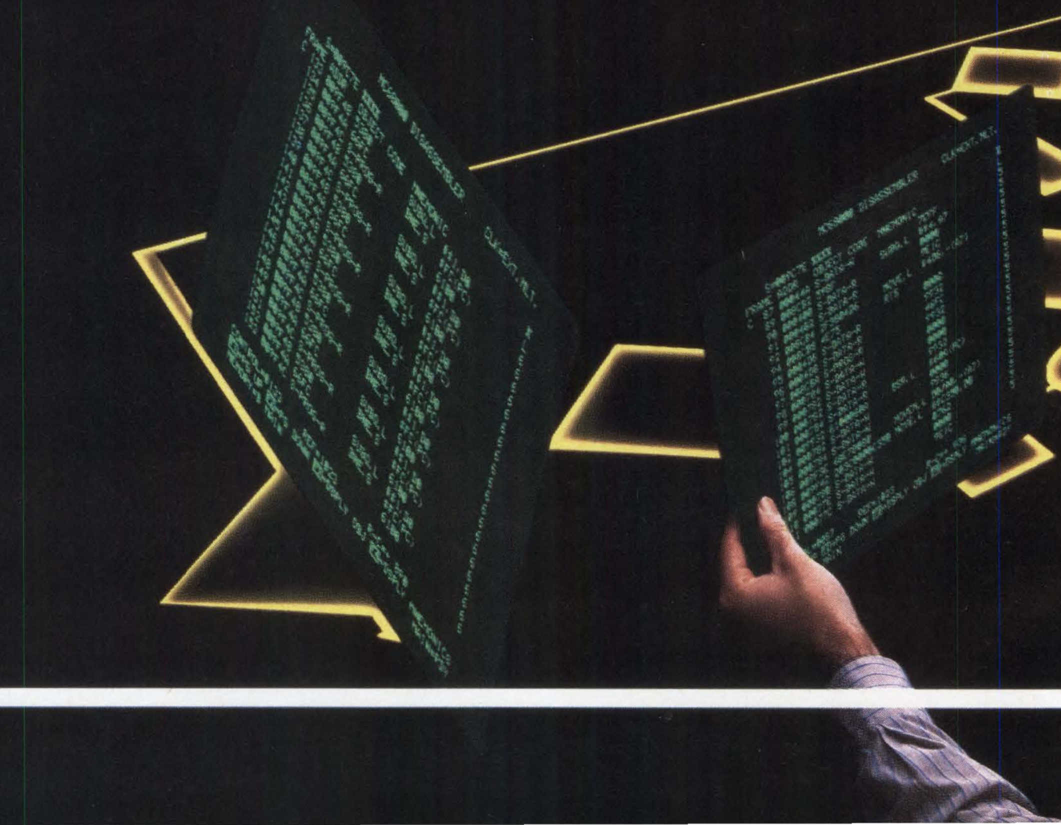

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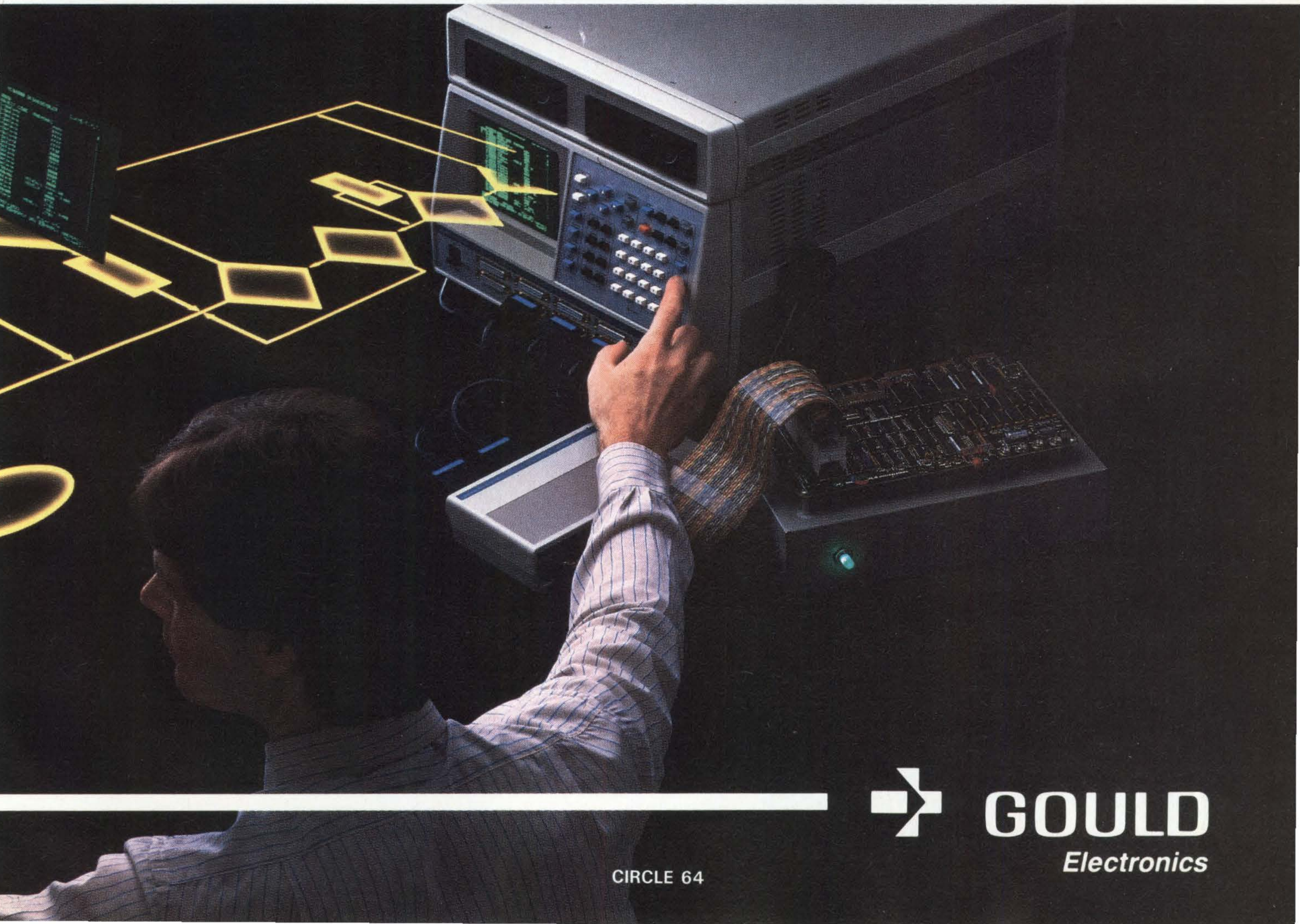

CIRCLE 64

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CIRCLE 65

SHORT-TOPOLOGY LAN DESIGN REQUIRES FLEXIBLE PARAMETERS

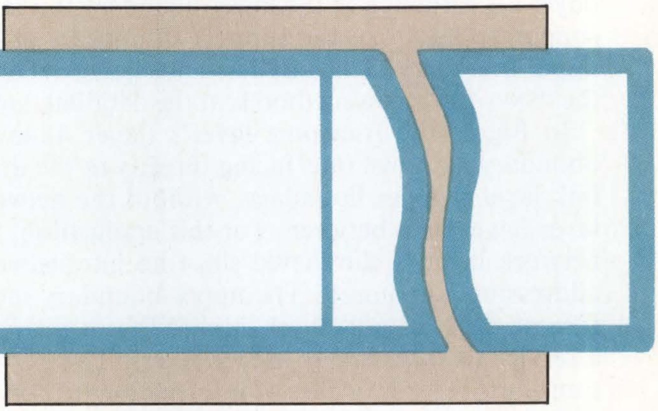
The near realtime operation of a short-topology local area network requires flexible configuration parameters that can be optimized by software.

by Eugene A. Floersch

While most local area network applications focus on medium-to-long topologies, the short-topology system is of particular importance because of its time-critical operation. Design parameters for short-topology networks differ from their medium and long topology counterparts, however, and must be adjusted to optimize frame structures and access mechanisms.

This network uses off-the-shelf components whose target market is for Ethernet applications. All configuration parameters are flexible and default to an Ethernet-compatible configuration at reset time. Key features of the link control component are software-selectable linear priority, interframe spacing, and slot time. Carefully selecting these parameters from a network management perspective and using self-policing access management at each node, can avoid collisions—using the carrier sense multiple access with collision detection (CSMA/CD) method. This preserves the benefits of deterministic methods while leaving the collision detection mechanisms in place for fault-tolerant recovery.

In the present VLSI era, the increasing functional density of devices gives system designers a greater variety of features for application-specific configurations. For standardization groups, this presents a real challenge to ensure that the standards defined do not focus on a narrow set of requirements. In



the context of the seven-layer Open System Interconnection (OSI) model of the International Standards Organization (ISO), standardization efforts may be forced to treat each layer as a "library" of standard types or classes. This should leave to system designers the final selection of functions from each layer to best fit a particular application.

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The OSI starting point

The OSI model of the ISO is a convenient baseline from which to examine networks and other communication systems. For the short-topology system to be described, only the four lower layers of the model need to be discussed. These are the physical layer (layer 1), the data-link layer (layer 2), the network layer (layer 3), and the transport layer (layer 4). In addition, the transceiver and medium are both below the physical layer. Although valid arguments can be made for treating the transceiver as a sublayer of the physical layer, it is convenient in this case to define layer boundary interfaces to match those of off-the-shelf components.

Fig 1 defines the interface between the physical medium and physical layer (layer 1), configured to accommodate the CSMA/CD access method. Moreover, Fig 2 defines the interface at both the

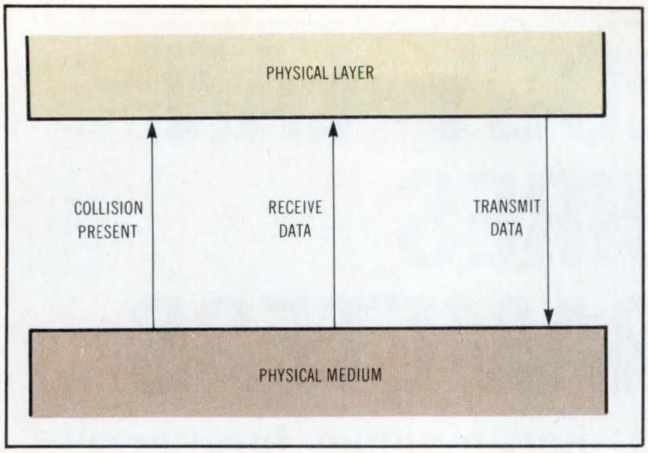


Fig 1 At the lowest level of the Open System Interconnection (OSI) model—layer 1—the physical medium, usually a bus, interfaces to the physical layer. This interface is configured to accommodate the access method.

upper and lower boundaries of the data-link layer (layer 2). Although at the lower boundary this layer supports CSMA/CD, the support disappears at the upper boundary. This implies that management of the CSMA/CD access method is at the data-link layer.

In Fig 3, the transport layer's (layer 4) lower boundary is shown interfacing directly to the data-link layer's upper boundary, without the network layer (layer 3) in between. For this application, the network layer is eliminated since no internetwork addressing is required. The upper boundary interface of the transport layer implies that it provides a service to successively higher layers. This service transports records or files of information (ie, service data units) to peer layers at other nodes.

Service classes are limited to connectionless (with and without error control) broadcast and multicast. Such service assumes full responsibility for end-to-end delivery of the service data unit at the requested quality level. This completely removes from the requesting entity any burden or overhead associated with the transport process. An analogy is the process by which the U.S. Postal Service provides various classes of mail service.

A unique feature of the design is the mechanism, added at the transport layer, that polices the arrival of service requests. This mechanism relies on judicious selection of parameters that regulate the bus access attempts by link control. In so doing, it avoids the collisions that the link control is designed to handle. The collision-resolving function lies dormant until a fault occurs within the network causing a collision. Then, it becomes active in support of fault recovery.

Considering a short-topology system

An example of a short-topology network has many distributed network stations (ie, nodes) that exchange data in a near realtime environment on a 10-MHz bus. The number of nodes can vary, but in this case it is 62, connected by a bus not longer than 60 m.

In this 62-node network traffic is characterized as variable length, falling into two distinct groups. In the first, 50 percent of the stations transmit messages averaging twenty 16-bit words; in the second, 50 percent of the stations transmit messages averaging 100 words. The traffic is distributed randomly in time. Peak demand requires one transmit

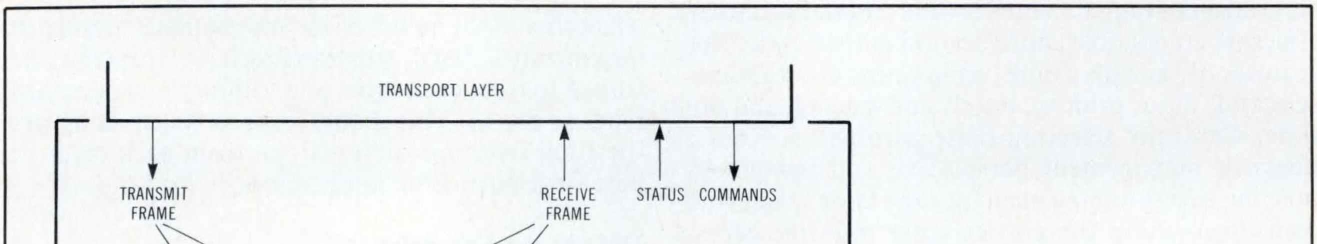
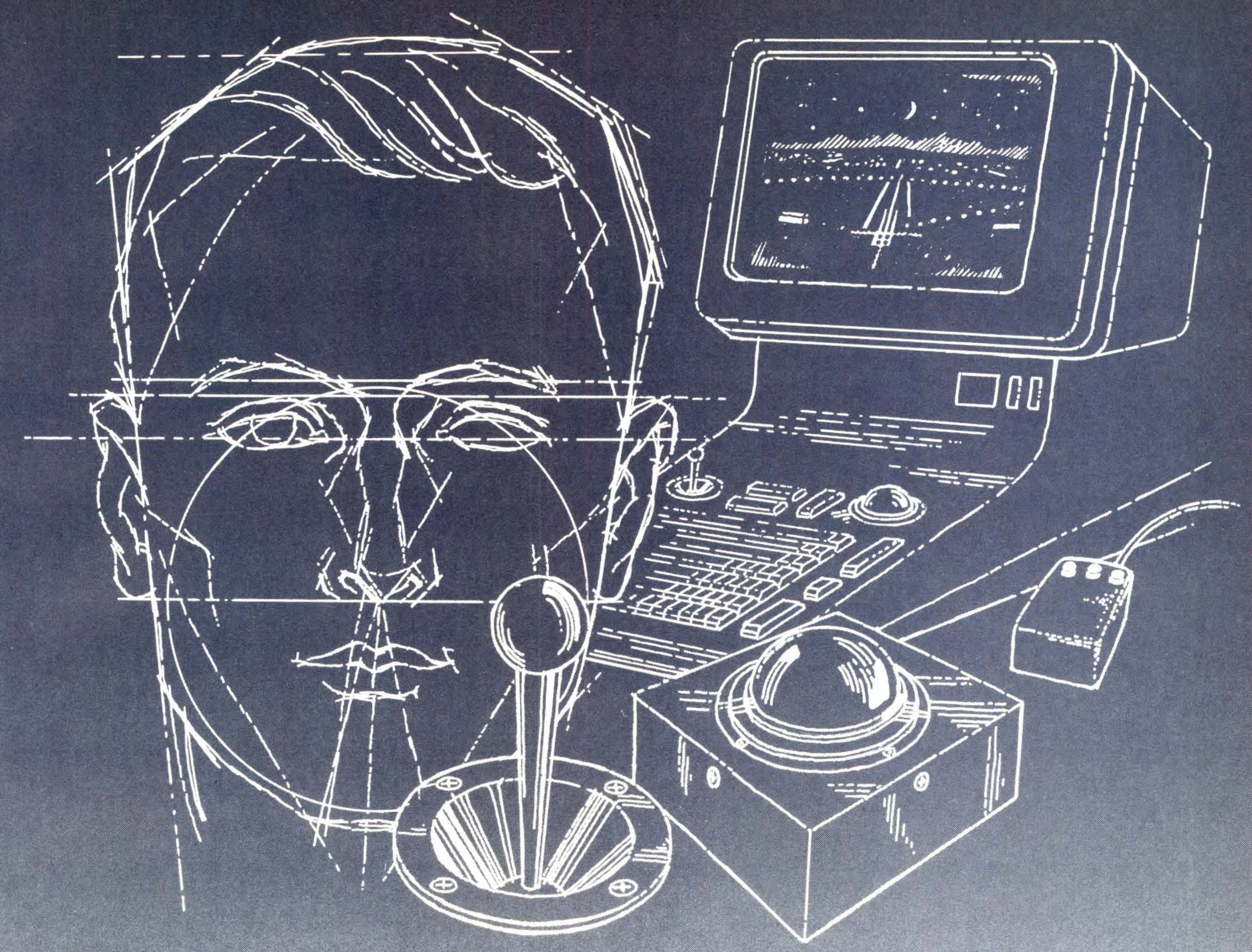


Fig 2 Layer 2 of the OSI model, the data-link layer, is shown interfacing to the physical layer below it and to the transport layer above it. The data-link layer supports the CSMA/CD access method, as does the physical layer.



opportunity for each station during a 10-ms interval, with all opportunities during this interval allowing for messages 20 percent longer than average.

All stations synchronize their transmissions to a 10-ms interval. Data queued for transmission during an interval and not transmitted at least by the next interval is considered stale, and therefore, unusable in subsequent intervals. Data received with errors is noted and discarded.

Fig 4 illustrates a block diagram of a typical station configuration. At initialization time, the transport layer at each station is provided with local-station configuration details and the global network configuration data necessary to map network (logical and physical) addresses. A network management function residing in a station host supplies this data.

At station power-up time, the transport layer controller configures the link controller for the frame structure shown in Fig 5 and the CSMA/CD access method of Ethernet. It then waits for network-related configuration data to be broadcast on the bus. In the case of a station in which the network management function resides, configuration data is passed from the local host.

Network configuration data includes a unique linear-priority parameter for each station, and designates a primary and backup timekeeper station for maintaining the major network access cycle. While the network has a 10-ms major cycle and a single opportunity for each station in a major cycle, network initialization data can establish a different cycle period. Data can also assign multiple opportunities to one or more stations should the traffic requirements dictate.

When network initialization is complete, the transport layer controller at the designated network timekeeper station opens the network for normal traffic exchange by transmitting a timekeeping frame. The frame is uniquely identified by a specific multicast address that all stations are configured to accept. From this point, the transport layer controller at each station will be actively engaged in managing that station's access to the bus.

Fig 6 illustrates the general case in which n stations are uniquely configured—at the link-control level—with a linear priority number. Twice the maximum propagation time on the medium (in this case, 2 x 60 x 5 ns/m = 600 ns) multiplied by a number one less than the station number equals the linear priority number. The timekeeper station is given first-access priority, or linear priority equals 0. This linear priority number represents the time that the link controller must wait, beyond the interframe spacing (IFS) interval g (see Fig 6), before attempting to acquire the bus. For Ethernet compatibility, the IFS is set to 9.6 μs; for the example at hand, the IFS is 3.2 μs. This is the shortest interval allowed in the link controller design.

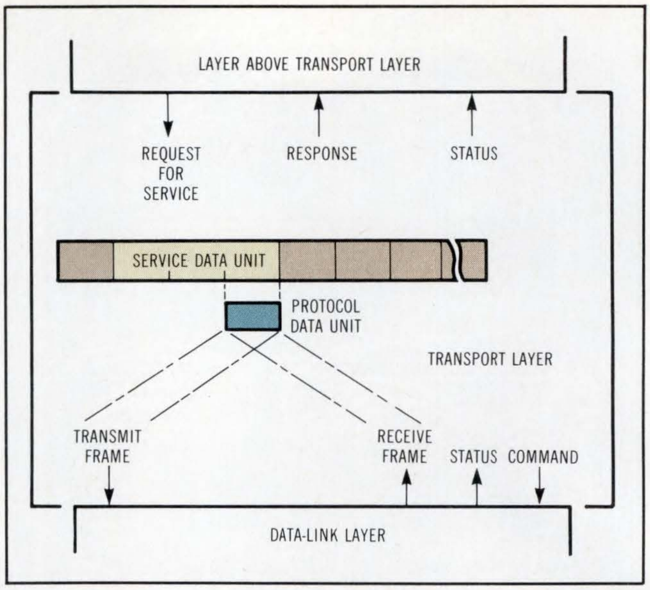


Fig 3 Since the short-topology LAN does not use internetwork addressing, the data-link layer interfaces to the transport layer, with no network (layer 3) layer in between. The transport layer exchanges records or files with transport layers at other stations in the network.

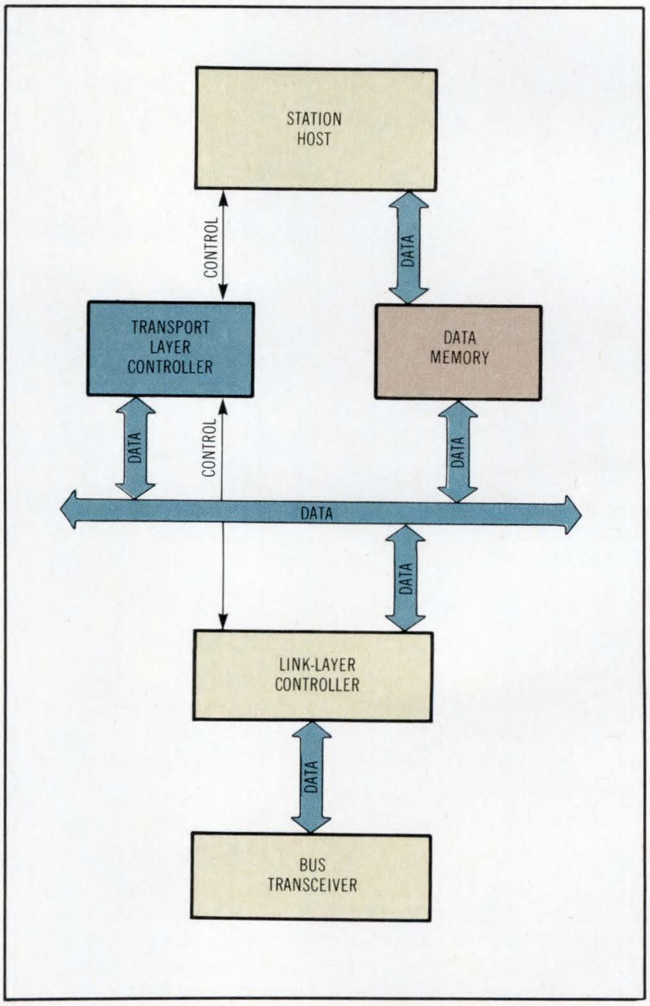


Fig 4 A typical station or node on the short-topology LAN contains a host, transport, and link layer controllers and a data memory. The transport layer controller is responsible for configuring the link controller for the frame structure shown in Fig 5 and for the CSMA/CD method.

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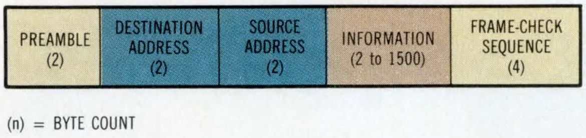


Fig 5 The frame structure shown here represents the protocol by which data is passed between stations on the short-topology LAN. This structure is set by the transport layer when a station is first powered up.

Each major station is allowed one opportunity to transmit in each major cycle metered by the timekeeper station. Each transport layer controller ensures that not more than one request for bus access is levied on the link-layer controller during that interval. Moreover, requests that arrive during a current interval, but after the opportunity quota for that station has been exhausted, are queued for delivery during the next interval.

Overhead considerations

Assume a definition for overhead that includes all time intervals outside the information field interval shown in Fig 5. This means that every frame transmitted contains 10 bytes of frame overhead—at 10 MHz, this is equal to 8 μs. In Fig 6, assume that every opportunity for transmission during a major cycle is used, and that each station is given one opportunity.

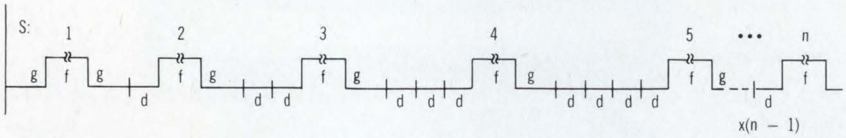
Overhead for each opportunity consists of a fixed part made up of the IFS ($g = 3.2\ \mu s$) plus the frame overhead ($f = 8\ \mu s$) and a part that varies with the station number (an integral multiple of $d = 0.6\ \mu s$). This latter part is the linear priority of the station.

In the final equation for computing total overhead time in a major cycle, the first-order term represents the fixed part, which is linearly proportional to the number of transmit opportunities used in the interval. The second-order term is contributed by the linear-priority delay, which increases with the station number. The difference between the major cycle time (10 ms in this case) and the total overhead time/cycle, is the total useful bandwidth in bit times, to be shared by all stations in any proportion. Fig 7 illustrates each term's contribution toward the total overhead. It also shows that as the number of stations approaches 40, the second-order term starts to predominate. Further increases in the number of stations raise the overhead due to linear-priority delays at an expanding rate, with a corresponding loss in total bandwidth.

Each major station is allowed one opportunity to transmit in each major cycle metered by the timekeeper station.

A modified approach is possible in which the 10-ms major cycle is divided into two 5-ms minor cycles. For convenience, assume that the 31 stations with the highest priorities have the opportunity to transmit during the first minor cycle, and the 31 stations with the lowest priorities have opportunities to transmit during the second minor cycle. This scheme allows the same linear-priority number to be assigned to two different stations without conflict for access.

Each transport layer controller regulates its link-layer controller's attempts at bus access according to assignment to a minor cycle and allowed opportunities within that cycle. It is conceivable that a particular station's traffic requirements would dictate that one or more opportunities be offered in each of the minor cycles. In this case, a station's linear-priority assignment would be unique to that station.



WHERE:

S = STATION NUMBER

$g = IFS = 3.2\ \mu s$

f = FRAME OVERHEAD TIME = 8 μs

$d = 2 \times t_p = 0.6\ \mu s$

TOTAL OVERHEAD TIME FOR A MAJOR CYCLE

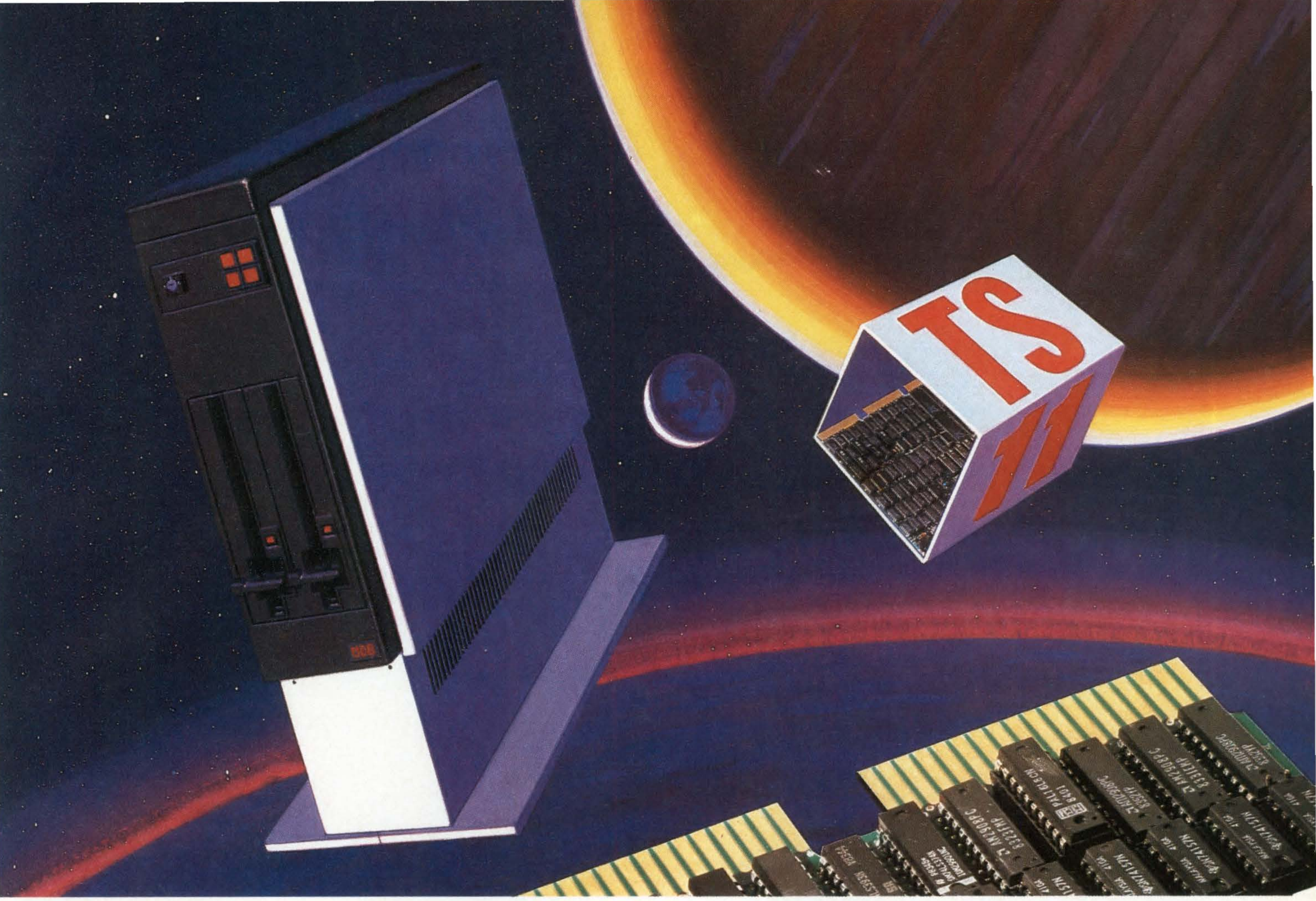
$$T_{total} = \sum_{s=1}^{s=n} [g + f + d(s - 1)] = n(g + f) + (d) \sum_{s=1}^{s=n} (s - 1)$$

$$= n(11.2) + (0.6)\frac{n(n - 1)}{2}$$

$$= 11.2n - 0.3n + 0.3\,n^2$$

$$= 10.9n + 0.3\,n^2 \text{ (in microseconds)}$$

Fig 6 The overhead time of a major cycle is composed of a number of variables: interframe spacing (IFS) time, frame overhead time (f), and a linear delay which varies with the station number. The overhead defined here includes all time intervals outside the information field shown in Fig 5.



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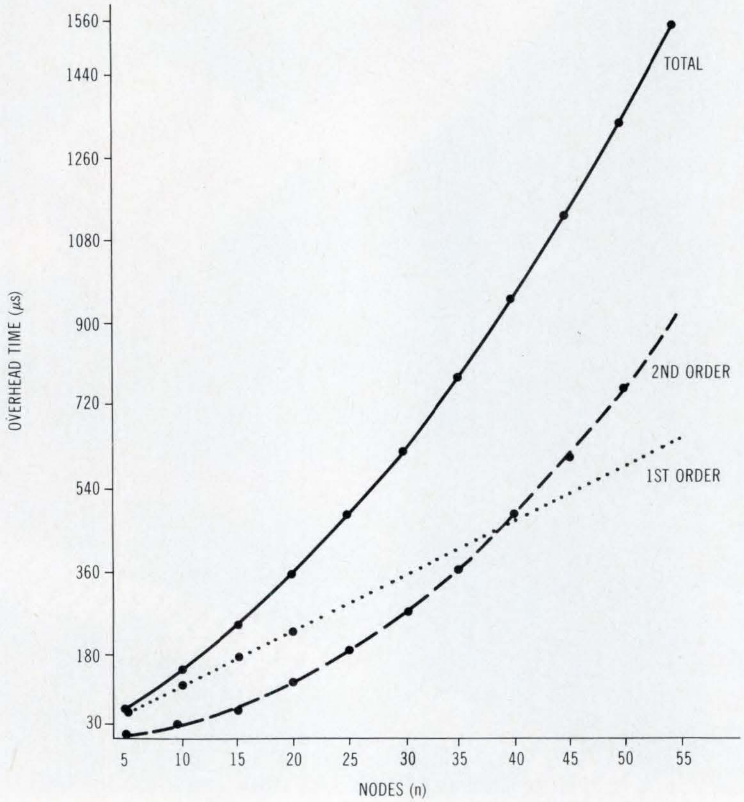

Fig 7 Total overhead (T_{total}) consists of a first- and second-order term. In a LAN with up to 40 nodes or stations, the first-order term is the larger contributor to overhead, but as more stations are added, the second-order term makes a greater contribution to the total overhead.

To illustrate bandwidth gain in the approach just described, the Table shows step-by-step calculations for two 5-ms intervals and one 10-ms interval. Note that the linear portion of the total overhead time (T_{total}) is exactly one-half the value for the case n = 31 and for the case n = 62, as is expected. However, the contribution of the second-order term is only one-quarter of that for the case n = 62.

After subtracting the total for each 10-ms interval in both cases from the total time available, the technique of two minor cycles offers a gain of over 500 kbits/s. Under the traffic conditions assumed:

31 stations x 20 words/10-ms cycle
= 620 words/10-ms cycle
31 stations x 100 words/10-ms cycle
= 3100 words/10-ms cycle

	3720
At peak demand:	x 1.2 (120 percent)
Total required/10 ms	4464 word bandwidth

Even with a single 10-ms major cycle there is a 14 percent reserve bandwidth (5106 words/10 ms). With two minor cycles, this is increased to 22 percent or 5467 words/10 ms.

Contrasted with this approach is the Ethernet protocol which uses an IFS of g = 9.6 μs, and a frame overhead of 26 bytes (f = 20.8 μs). Ignoring for the moment the occurrence of collisions, the total overhead for 62 transmission opportunities is

g + f =	30.4	μs/opportunity
	x 62	opportunities
	1884.8	μs or 18,848 bit times.

Assuming that the 62 opportunities occur every 10 ms,

100,000	bit times/10 ms
− 18,848	bit times overhead/10 ms
81,152	bit times/10 ms or 8.1152 Mbits/s.

This figure is just slightly less than that shown in the Table for 62 opportunities. However, since collisions are ignored, 8.1152 Mbits/s represents an ideal case that never occurs.

Much research has gone into the practical limits of the CSMA/CD method as the offered load increases. Shock and Hupp[1] report a 94 percent utilization by 10 stations, each offering a 10 percent load. Meisner[2] suggests 85 percent as a reasonable figure. Using the more optimistic figure reduces the 8.1152 Mbits/s to 7.6283 Mbits/s. Assuming a minimum backoff delay of one slot time—512 bit times—and a 32-bit jam interval, a minimum of 512 + 32 + 96 = 640 bit times are lost for each collision. The difference between the ideal (no collision) case and the practical limit can be attributed to time lost in collision.

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Two Approaches to Bandwidth Calculations

	For a single 10-ms interval, 62 opportunities/interval	For two 5-ms intervals, 31 opportunities/interval
n=:	62	31
T_{total} $10.9n + 0.3n^2$=:	675.8 μs + 1153.2 μs = 1829 μs	337.9 μs + 288.3 μs = 626.2 μs
Total overhead/interval:	= 18,290 bit times/interval x 1 interval/10 ms	= 6262 bit times/interval x 2 intervals/10 ms
	18,290 bit times/10 ms	12,524 bit times/10 ms
Total bit times/10 ms:	100,000	100,000
Minus overhead:	− 18,290	− 12,524
Usable bandwidth:	81,710 bit times/10 ms x 100 intervals/s	87,476 bit times/10 ms x 100 intervals/s
	8.171 Mbits/s	8.7476 Mbits/s
Bandwidth gain:	8,747,600 − 8,171,000 = 576,600 bits/s	

Using the approach presented earlier, the time lost due to collisions can be avoided. In addition, the nondeterministic character of a pure CSMA/CD method is removed, and with it, one of the major objections to its use. By leaving the collision-detection mechanism in place as a fall-back to support recovery from abnormal operation, a less complex implementation for fault-tolerant systems appears more feasible than with token-ring designs.

Fault-handling procedures

A short-topology network of the type described can experience three types of faults. The first is the jabbering transmitter, in which the transmitter fails to terminate a frame and surrender the bus in a normal manner. The protection against this type of fault resides in the self interrupt capability of transceivers specified for CSMA/CD designs.

A second major fault results from stations failing to police their own access attempts in accordance with the opportunities allotted at initialization time. This can occur because of loss of synchronism with the timekeeper that meters network cycles, resulting in collisions. The transport-layer controller is notified when a collision is detected, and it initiates three actions: it temporarily removes the station from normal transport service even though it may not be the offending station; it notifies the local process that requested transport service that it is suspended temporarily; and it notifies the local network management function of a network fault causing collisions.

The network management function can now initiate a series of diagnostics to isolate the fault. If local diagnostics identify local faults, the station is held out of service until corrective action is complete. If none are identified, the station is returned to normal transport service. This begins with the first subsequent timekeeping multicast from the timekeeper station following completion of local checks and process notification. Persistent and continued collisions detected at a station after it returns to service, force the station to withdraw from service permanently and await maintenance action.

A third major fault is the failure of a timekeeper station to transmit the multicast time marker. When the transport layer controller at the backup timekeeper station recognizes that two successive time markers have been missed, it resets the primary station and removes it from operation. The backup station then assumes the role of primary time keeper.

Because component designers include configuration flexibility in products without compromising their target market, careful selection of design parameters is permitted to minimize overhead. This, coupled with self-regulating access management to overcome the disadvantages of a standard access method, results in attractive performance in a short-topology network.

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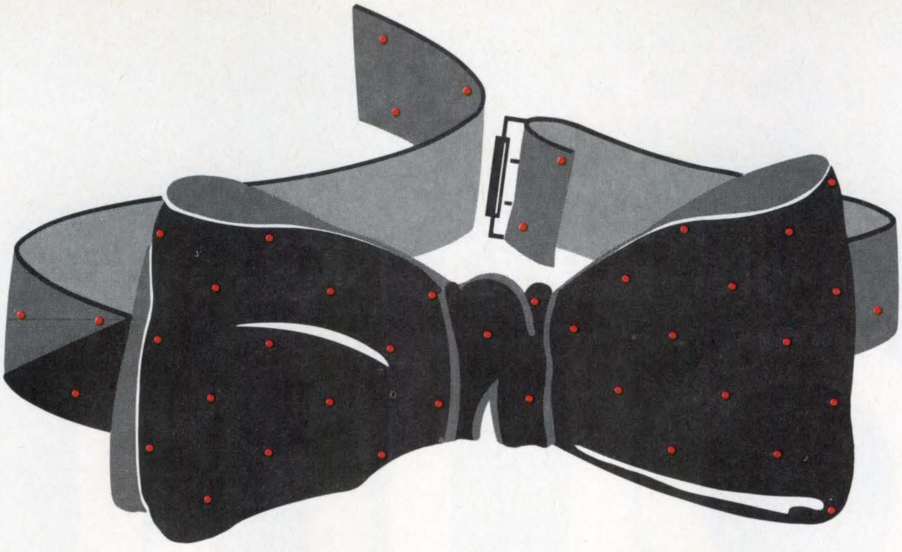
1. Shock, John F. and Hupp, Jon A., "Performance of an Ethernet Local Network—A Preliminary Report," *Digest of Papers—Compcon Spring '80,* IEEE Computer Society, Los Alamitos, CA, pp 318-322.

2. Meisner, Norman B., "Estimating the Throughput of Broadband LANs," *Systems and Software*, Nov 1982, pp 75-77.

Announcing the WY-75.



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CIRCLE 69

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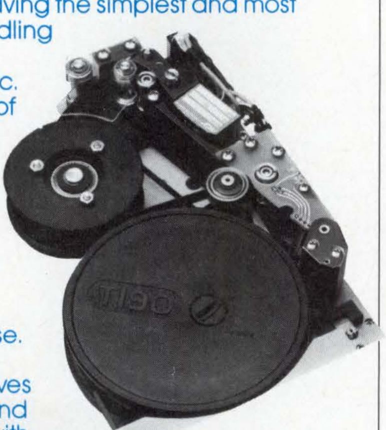

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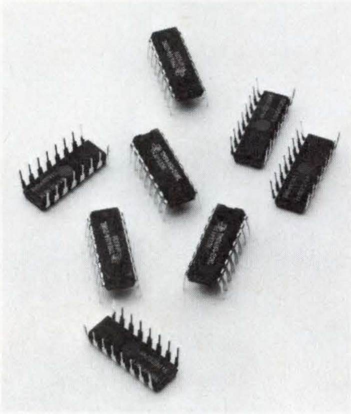

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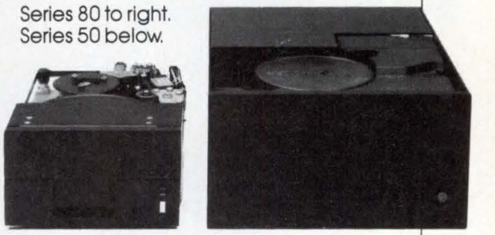

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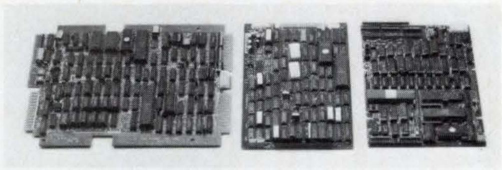

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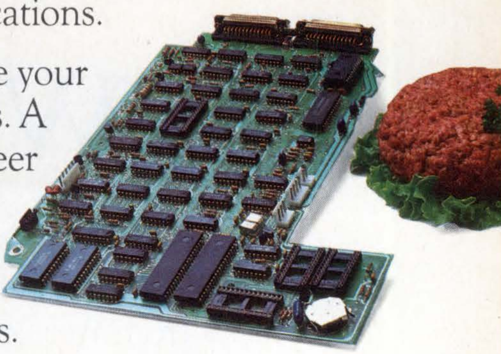

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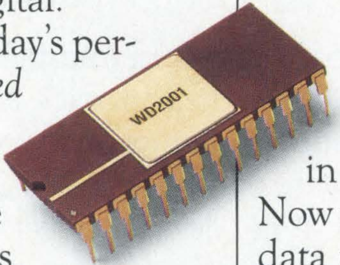

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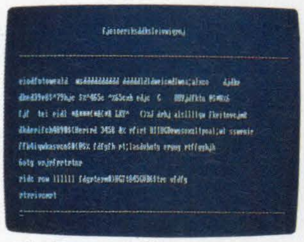

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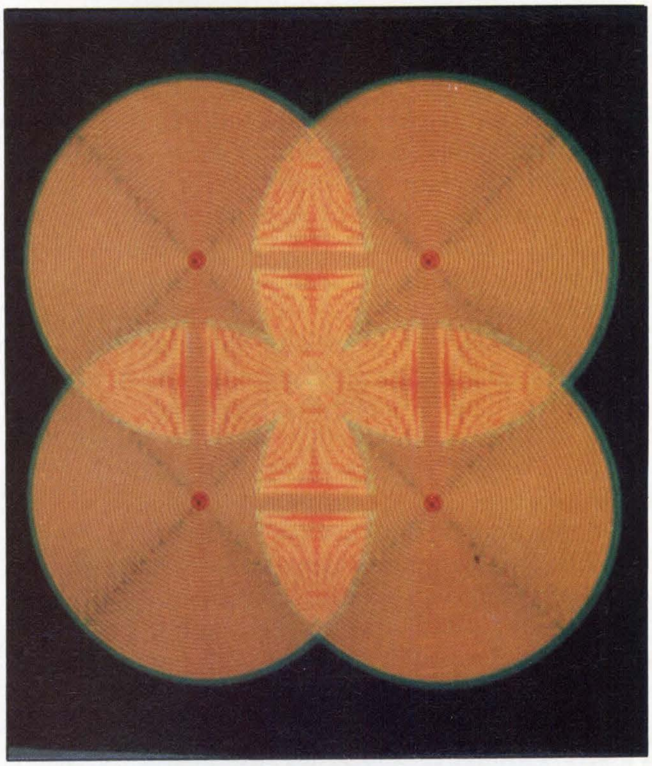
MULTIPLE CONTROLLERS CREATE HIGH SPEED COLOR GRAPHICS

Four graphics controller chips can be used to build high resolution color graphics terminals. But first, designers must resolve the problem of synchronizing controller chip operation.

by Steve Slade

Until recently, design engineers found it difficult to create high resolution color graphics terminals that were cost effective. The state of the art graphics terminal was not advanced enough to permit high resolution at a relatively low cost. In 1982, however, the introduction of the NEC 7220-1 graphics display controller chip opened many design possibilities. Engineered by NEC to replace a substantial amount of dedicated graphics hardware and software, the 7220-1 represents a remarkable improvement in time and cost over traditional graphics systems. Its subsequent cross-licensing to Intel establishes it as an emerging standard in graphics processor chips.

When Intecolor Corp began the design work on its newest generation of color graphics terminals last year, there was little doubt about what technology would be used. The company received some of the first preproduction NEC 7220-1 graphics chips and immediately began incorporating them into a new product. This is now the very high resolution VHR-19 (Fig 1). The company has traditionally been a supplier of cost-effective color graphics terminals with very low prices for low to medium resolution. But, low cost, high resolution (which is vital for the human interface needed for control and measurement applications), had previously been considered an unattainable goal. To meet this goal, the design objectives for the VHR-19 are high speed, 1024 x 1024 dot-addressable resolution, smooth pan, zoom, and other high level features at a price consistent with the company's cost-conscious marketing strategy. With several 7220-1 chips included in the design, a great deal of power and speed could be made available at a low price. Such a new design does, however,



Steve Slade is digital design manager at Intecolor Corp, 225 Technology Park, Norcross, GA 30092, where he is responsible for high resolution graphics design. He holds a BS in electronic engineering from the University of Illinois.

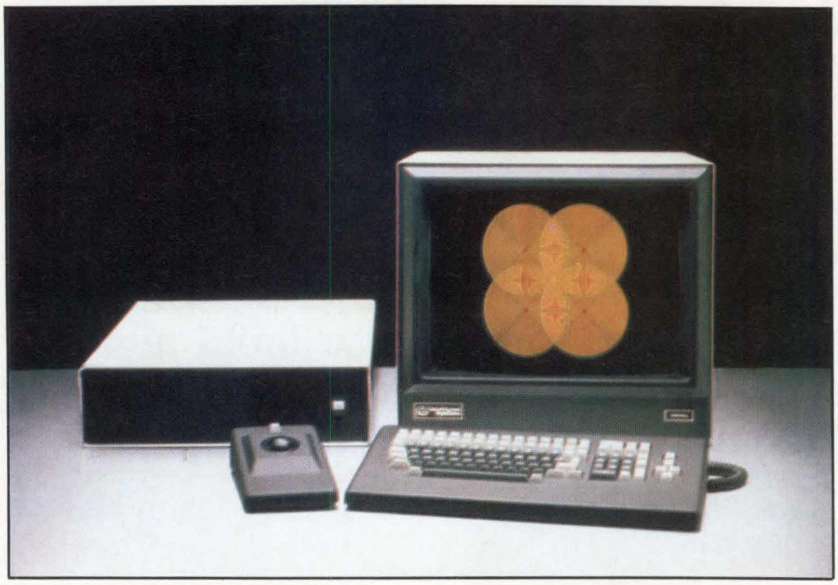


Fig 1 The color graphics terminal incorporates four 7220-1 graphics chips for high speed processing. Design objectives include 1024 x 1024 dot-addressable resolution, smooth pan, and zoom.

require solving a number of new problems and redefining the way color itself is generated.

Processing in three planes

Like most color terminals, the VHR-19 has to create colors with three color guns. Analog control is used to create screen color, permitting more color variation than is possible with systems that merely turn each color gun on or off. Prior to the 7220-1 chip, color was created by individually controlling each pixel in each of three colors. This required writing graphics vectors up to three times, resulting in a need for more memory and more execution time than is necessary in black and white displays.

By using three separate 7220-1 chips, however, the VHR-19 could address all three bit planes simultaneously. With a one-chip design, the 7220-1 would need to be time-shared for each plane. This greatly reduces the speed at which the displays are generated. The multichip design combines the power of the 7220-1's rapid internal graphics calculations with the advantages of parallel processing. Ample room for the three 7220-1s is available on the graphics generator board (Fig 2), which also holds 48 dynamic RAM chips, with sixteen 64-K x 1-bit chips used for each plane. The 7220-1 chips can then transfer 16 bits of data in parallel to and from the memory chips.

In addition to using the three 7220-1s to control color graphics displays, the VHR-19 was designed to employ a fourth 7220-1 to handle the generation of alphanumeric characters. This fourth 7220-1 would always remain in alphanumeric mode to allow the user the convenience of a terminal with ANSI X3.64, which is rapidly becoming the industry's standard communication protocol. This standard is compatible with DEC hosts and VT100s, and works well with DEC-supported text editors. The terminal mode enables users to switch from sophisticated graphics to efficient data entry easily. Characters generated in alphanumeric mode can be viewed as an overlay on the graphics and will not interfere with the graphics display. The terminal also includes a menu-driven setup mode that is saved on command with electrically erasable PROMs.

The graphics terminal's CPU is a Z80, which controls the four 7220-1s over the 8-bit data bus from the terminal board. Any command can be designated for all 7220-1s, thus reducing programming time. Each 7220-1 performs the necessary internal calculations and sends instructions to the graphics memory planes.

The video output board has a high speed (25-ns) color lookup memory arranged in a table of two 8-color maps, each 12 bits wide. The 12-bit output is arranged in three 4-bit groups that give 16 intensity steps for each of three color CRT guns. The two maps enable a blink scheme where any color can be "blinked" to any other color at a 2-Hz rate. This

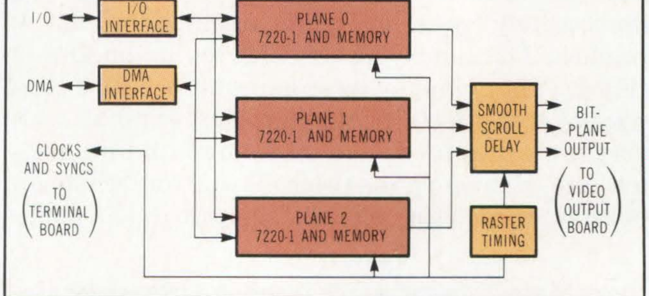


Fig 2 The graphics generator board has three 7220-1 chips, each controlling a separate bit plane. Parallel outputs feed into the smooth scroll taped delay line and then to the video output board.

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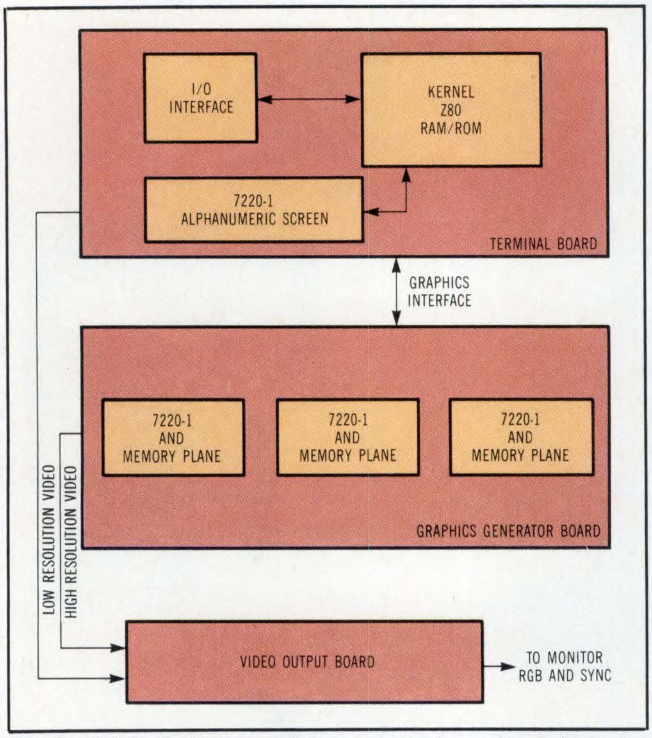

Fig 3 A block diagram of the system shows the principal components—terminal board, graphics generator board, and video output board. The terminal board controls the system sending display commands to the graphics generator, and color map commands to the video output board.

system is, therefore, more flexible than a simpler "blink to black."

The low resolution video is transmitted over a separate cable from the Z80 terminal board. A priority circuit is included so that low resolution video preempts the graphics video. With this scheme, low resolution characters with a black background appear to be in the graphics plane. But when a character has a colored background, it will appear to be in a separate screen in front of the graphics.

The biggest design problem

The main design challenge for the graphics terminal (Fig 3) is synchronizing the operation of the four 7220-1 chips. This system uses interlaced video, which requires synchronizing not only the video, but also the odd/even fields so that the frames are in sync and not a half line off. The 7220-1s are arranged so that plane 0 of the graphics board is the sync master and the remaining two graphics and one alphanumeric 7220-1s are sync slaves to the master chip. (See Fig 4.)

There is a problem in making these four chips work together in harmony because the 7220-1 devoted to alphanumerics has a different raster format than the graphics 7220-1s. The graphics pixel clock is divided by two to form the low resolution pixel clock. In addition, the horizontal line of the graphics raster must be a multiple of 16 and the low resolution line must be a multiple of six low resolution pixels (12 high resolution pixels).

By necessity, the 7220-1 chips are synchronized at power up for two vertical sync periods. Thereafter, the 7220-1s are free to run. Thus, the low resolution and high resolution rasters must have the exact same number of high resolution pixel clocks or the low resolution screen would "roll" out of sync with the graphics. This means that the horizontal dot count must be a multiple of 16 and 12. Also, the high resolution must have an active region of sixty-four 16-bit words and the low resolution an active region of eighty 6-bit words. To satisfy all of these constraints, the horizontal blanking period was padded to achieve the multiple of 16 and 12.

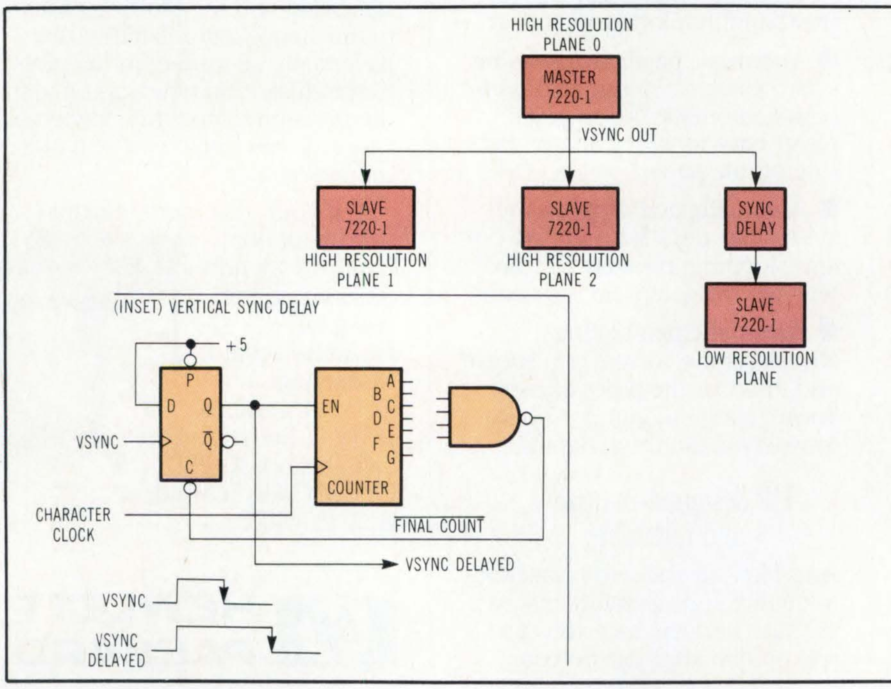

Fig 4 This block diagram shows the master generating vertical sync, and driving the sync inputs of the two slave graphics modes and the slave resolution alphanumeric through the sync delay circuit. The inset shows the details of the sync delay circuit. Vsync is supplied by the master, which sets the D flipflop. This enables the delay counter, which counts low resolution character clocks. The NAND gate is wired to detect the final count. When it is active, it clears the delay flop, which starts the slave.

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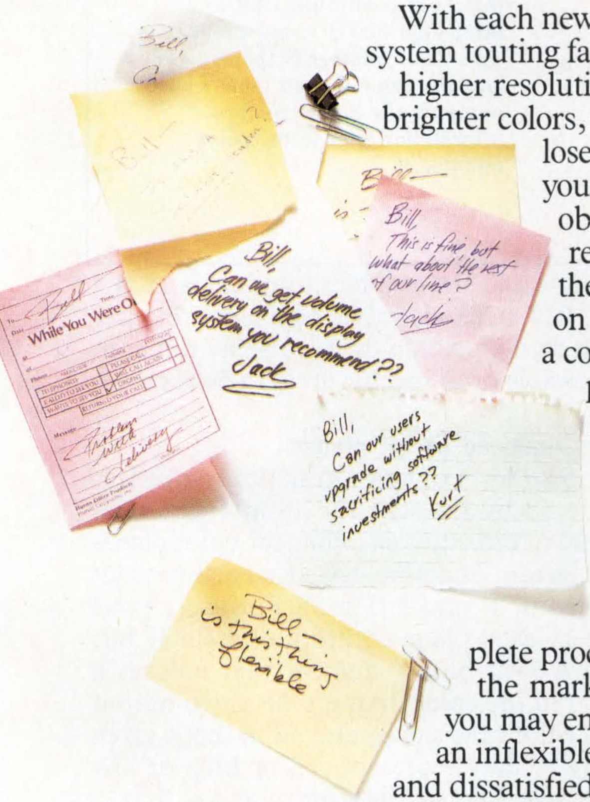

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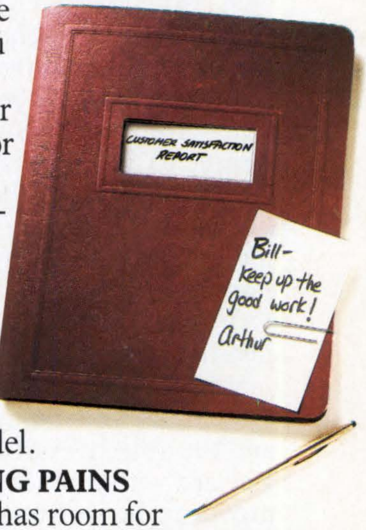

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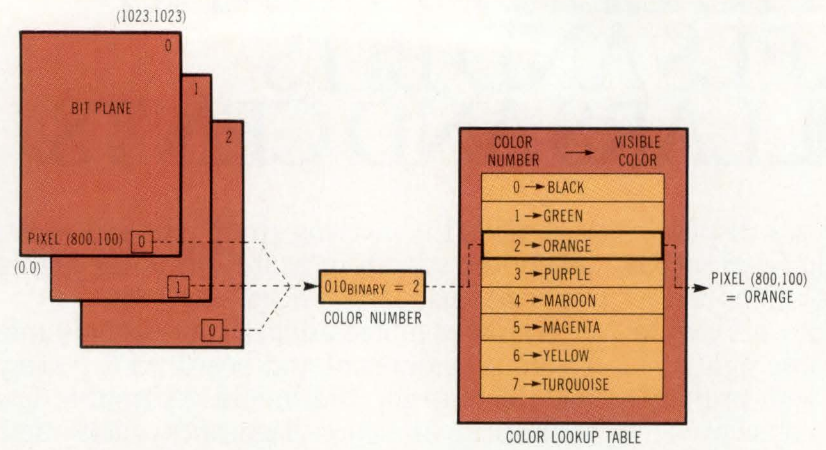

Fig 5 Bit-plane color mapping enables the user to change colors without redrawing vectors. Three 7220-1 chips control the bit planes that each contribute 1 bit to a three-digit binary color number. This color number is the address into the color lookup table whose output is the actual color information sent to the color monitor.

After the exact horizontal timing was determined, the position of the low resolution screen over the high resolution screen had to be set. The active raster size of the high resolution screen is 1024 x 768, and the active raster for the low resolution screen (in high resolution pixels) is 960 x 768. Since the low resolution screen is narrower than the high resolution screen, its position relative to the high resolution screen must be set. The low resolution screen position is set by delaying the master vertical sync from the graphics board by an integral number of low resolution character clocks. The circuit used in the VHR-19 allows the raster to be either left or right justified; left justification was chosen.

With the synchronization problem solved, the capabilities of a multiple 7220-1 design become clear and the objectives of Intecolor's new terminal project are within reach. The improvement in speed proves to be worthwhile, even though the cost of adding the extra chips is not small. A full-screen vector on the VHR-19 is 1024 pixels long, yet requires only 1/180th of a second to draw, a significant improvement over single-chip designs.

The benefits are obvious for virtually every kind of graphics application. The 7220-1s improve speed and allow special features to be added while costs are kept low. For example, zoom and pan, necessary for imaging applications, are handled largely by the 7220-1s. The 16 levels of zoom are created by pixel replication calculated in the 7220-1s.

External circuitry is required to obtain horizontal smooth pan because the 7220-1s operate on a 16-bit character basis, which causes the 7220-1 zoom display to jump by 16 pixels when a new character boundary is reached. To correct this, the VHR-19 sends data through the 7220-1 into a 16-bit tapped delay line, enabling the display to start on a pixel boundary and giving a smooth and continuous pan regardless of the zoom factor.

The vertical pan capability is resident within the 7220-1s, which calculate new start addresses to give a scanning effect. Because pan requires only the loading of a start address, it is very fast and smooth.

The resolution of the graphics terminal is 1024 x 1024, with 1024 x 768 viewable. Pan gives the user quick access to the portion of the display not concurrently viewable or to specific areas to be zoomed.

Color planes replaced by bit planes

An additional level of color graphics sophistication is achieved by the way the VHR-19 generates color. Instead of directly controlling the color planes labeled red, green, and blue, the 7220-1s control bit planes labeled 0, 1, and 2 (Fig 5). For every pixel on the screen, each plane contributes a single bit, resulting in a 3-bit binary number that indexes a unique color in the color map on the video output board. This color map can be altered so that a given number, say 5, may represent red or blue or any other shade specified by the user.

The VHR-19 lets the user concurrently display any 8 of 4096 shades. The shades are created by four bits of intensity data, and 16 levels of intensity are created for each of three color guns. These 16 levels produce the possible 4096 different colors using all three guns. Information that defines intensity for each pixel is generated by the CPU and sent to the video RAM. The 7220-1s send 16 bits of information from their bit planes into three shift registers. Bits from each register are sent serially to the video RAM containing the color map. The corresponding 12-bit color value found in the map defines the color displayed.

The user may redefine the color map at any time. By assigning the same color to two different color numbers, shapes can be hidden within other shapes. Since it already exists, the hidden shape can be quickly displayed just by changing the color assignment of the appropriate number in the map. This color map approach to color generation is less confining and makes creating displays less demanding for the programmer.

The VHR-19's ability to send and retrieve the graphics generated by the 7220-1s is essential to many applications. It has a read/write direct screen memory access channel that effectively transforms

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the screen into a high speed frame buffer. With a transfer speed of 1 Mbyte/s, a screen display can be sent in 1.2 s—250 times as fast as a screen display can be sent at 9600 baud. With a simple interface, a digital camera can be attached. The VHR-19 uses the standard RS-343-A video output so the system can be interfaced easily to large screen projection systems at 24-kHz horizontal sweep speeds.

VHR-19 has a communication output port that can be either serial or parallel. As a serial RS-232-C port, four pins are used to transfer data. A parallel port is provided on the pins not used for serial transfers. The port is switchable so that a serial text printer or a parallel, color ink-jet printer can be used alternately without complex changes or additional ports. Other options, such as a track ball or digitizer, can be interfaced as high speed positioning devices.

Reliability by design

Given the complexity of the VHR-19 and the high processing speeds involved, it is essential that reliability be designed into the product from the board level up. The Intecolor reliability effort focuses on two objectives: the synchronous operation of parallel functions and the reduction in the number of separate components.

The first objective is attained with a design of fully synchronous circuitry ensuring that timings are precise. Intecolor designs the VHR-19's bit planes on a CAD system, replicating the first plane to create the two remaining planes. The result is precise timing, since the planes are exactly the same. The second objective is achieved with the 7220-1s. The three bit planes fit on a single 10- x 16-in. card. Without the 7220-1s, the logic would have to be squeezed to fit on two cards.

In addition, new power supply assemblies are designed for the VHR-19. The new assemblies reduce heat, give better voltage regulation, and are made modular and expandable through the use of a 100-kHz switcher design. The new power supply allows the graphics terminal to be operated over a wider range of input voltages and is in excess of 85 percent efficient.

The critical timings of the graphics terminal require a more accurate design process and a more intricate PC board layout. The solution is a pipeline design that performs well in both alpha and beta tests.

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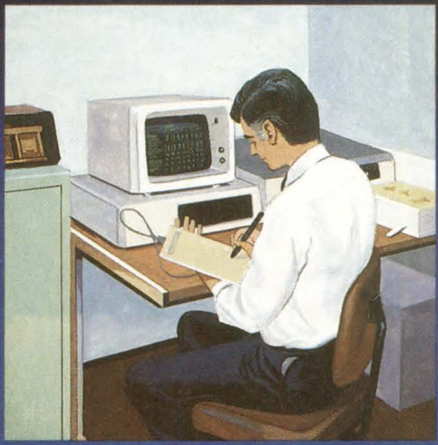

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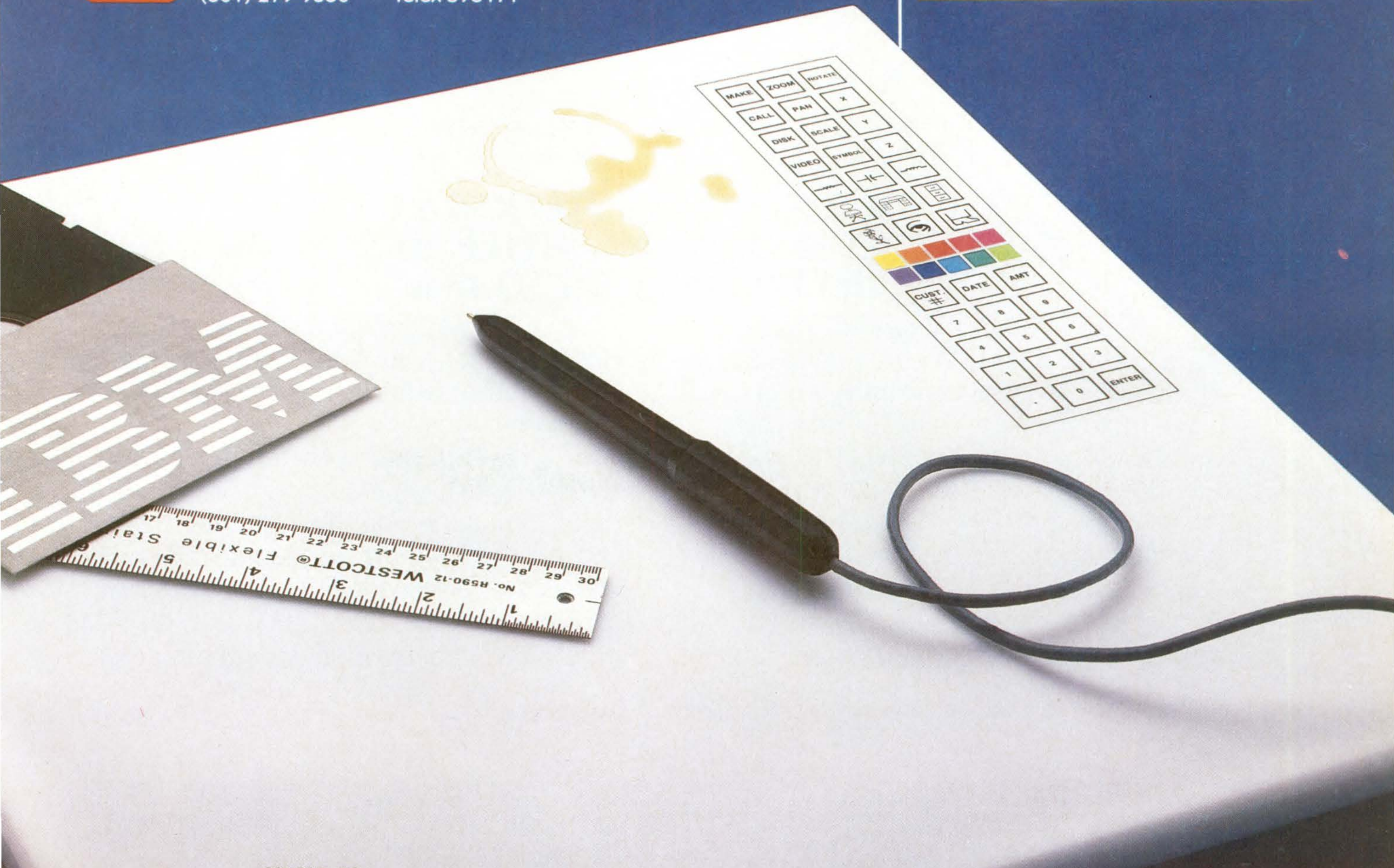

CIRCLE 80

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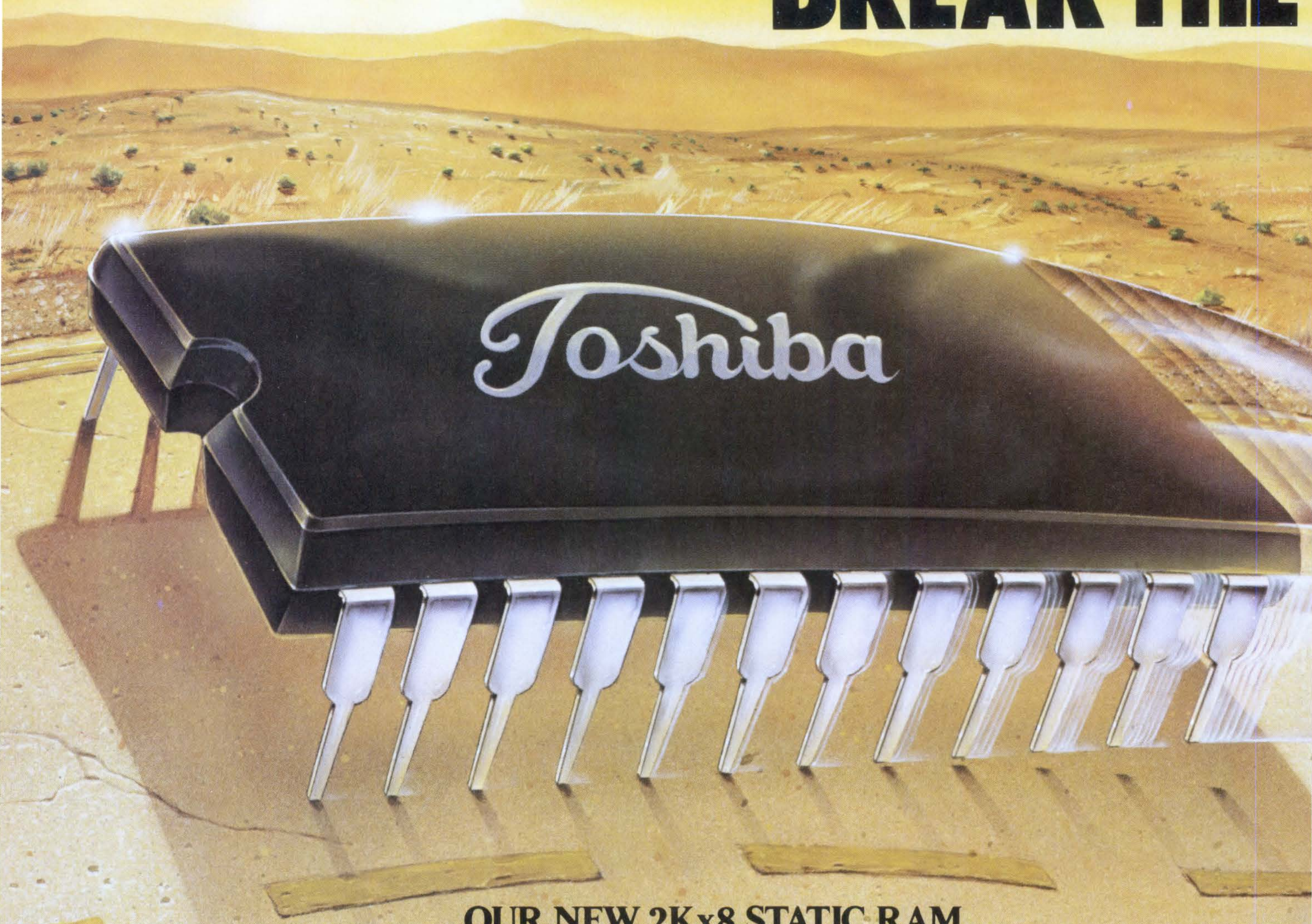

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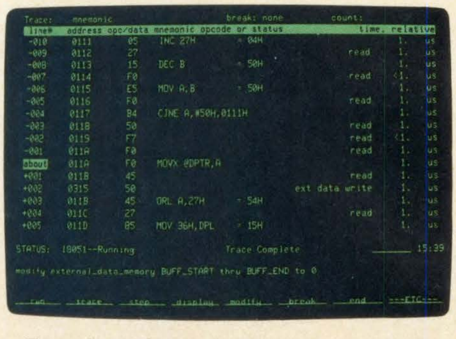

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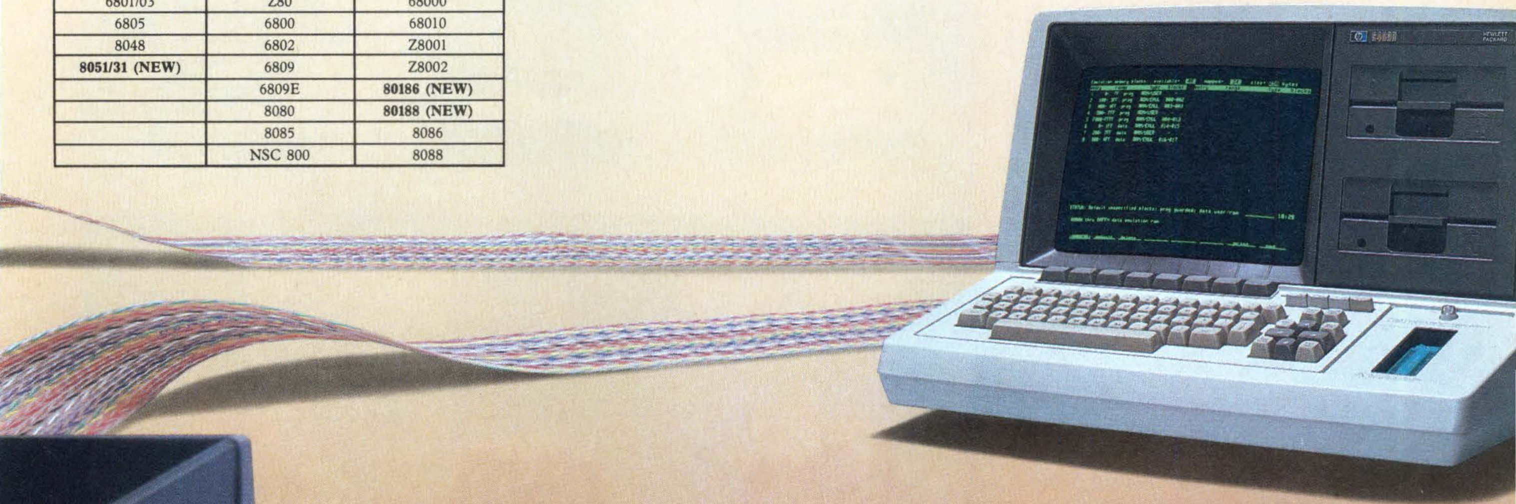

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CIRCLE 82

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	14"		10½"	8"			5¼"		
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AVERAGE POSITIONING TIME (ms)	27	27	18	70	20	20	95	83	35
TRANSFER RATE (K Bytes/s)	1012	1860	1860	1200	1229	1229	625	625	625
INTERFACE	SMD	SMD (MOD)	SMD (MOD)	SA4000	SMD	SMD	ST506/ SA4000	ST506/ SA4000	ST506/ SA4000
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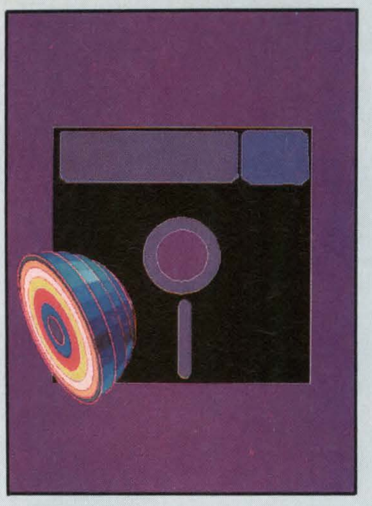

Special report on microcomputer operating systems

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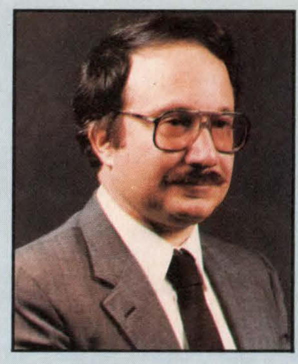

SPECIAL REPORT ON

MICROCOMPUTER OPERATING SYSTEMS

History notes that the first mainframe computer operating systems were humans. One of their chores involved watching vacuum tubes burn out on room-sized machines. While this task did not call on high technology, it was significant because the computer had so many tubes that a burn out occurred often.

Today, events of similar importance are taking place for millions of microcomputers, although this does not include watching VLSI chips burn out. What the tube watcher was to the early mainframe, the software-based operating system is to today's wide array of microcomputers. Modern microcomputer operating systems take care of the basic functions that computer systems need (eg, turning on and off, fault detection, I/O control, multitasking, and multiprogramming).

Rather than just perform some of these classic functions, today's microcomputer operating systems provide an operating system environment. Thus, they let application programs interact with graphics, graphics standards, light pens, touch screens, multiple file system formats, multi-users, multitasking, multiple operating systems, and multiple application programs. They also accommodate mice, drawing tablets, and other I/O devices, and various communication protocols.

"Sophisticated" is the watchword that best describes the microcomputer operating systems currently available. As operating environments, they are a far cry from the CP/M operating system that kicked off the microcomputer boom. Because they have so many functions and features, it is difficult to use them efficiently. And, there is a price for all these features. While the industry tries to resolve the problem, by and large, the available operating systems remain so different from each other that applications written for one do not work with another.

Many operating systems—or extensions to existing ones that allow the aforementioned capabilities—have been introduced in the last six months. More will be introduced in the second half of this year. Still others will debut in 1985. In short, activity in the microcomputer operating system business is at a high, and is fueled by machine usage in the home, office, and factory by tyros, hobbyists, engineers, and managers alike.

The contributed articles in this special report section concentrate on recent and soon-to-come product introductions. Computer system designers or integrators will learn what they can expect in order to help produce even more functional microcomputer-based products for the 1985 and 1986 markets.

Harvey J. Hindin
Special Features Editor

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CIRCLE 85

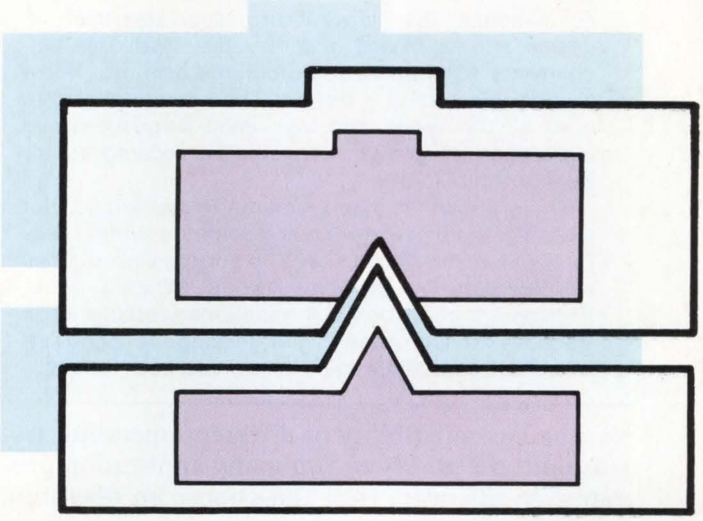
MICRO OPERATING SYSTEMS YIELD MIXED BLESSINGS

Keeping pace with the ever-increasing need for more microcomputer power, operating systems are becoming operating environments. But, it is hard to choose between them and there are compatibility problems.

by Harvey J. Hindin,
Special Features Editor

To accommodate the wide variety of application software demanded by microcomputer system users, the microcomputer operating system is slowly evolving into an operating system environment. This environment handles a multiplicity of coordinated software services to the user, the application program, and the microcomputer itself. It is no longer acceptable for a microcomputer operating system to be just a software program that turns a machine on and operates a floppy disk or two. Many of today's and (certainly most of tomorrow's) microcomputer operating systems will have to serve other operating systems, multiple application programs, multitasking and multi-users, windows, local networks, data bases, graphics, I/O (eg, touch screens and voice), natural language interfaces, and more.

Unfortunately, although microcomputer operating systems are evolving into operating environments, they are having problems. The chief problem is compatibility. It is very difficult to get operating systems to look alike, let alone "communicate" with each other. An application program, microcomputer, or computer network that works with one operating system will very often not work with another. For example, most operating systems cannot read the files created by other operating systems. The industry is making major efforts to overcome such limitations and progress has been made with standards and clever designs.



The evolution toward operating systems with built-in features providing specific environments cannot take place overnight. There is too much invested in existing operating systems and application software for that. Thus, computer designers must decide which operating system or operating system extension fits their needs. An operating system extension is software that is added to an existing operating system. Unlike application programs, extensions work with, and add services to, existing operating systems and can be called on for services by other applications.

To produce a computer system best suited for the application at hand, designers need to know which operating systems and extensions are available and how they are unique. They must also understand

MS-DOS: the inside story

Perhaps the most critical part of the PC-DOS operating system, as far as application programs are concerned, is its ROM-Basic I/O System (ROM-BIOS). It defines the basic I/O software primitives that operate I/O devices. There are also several files that govern MS-DOS operation. One file, the IBMBIO.COM, defines the hardware operating system interface to the physical devices and independent device drivers. Another, the IBMDOS.COM file, contains reference disk operating routines that are separate from any immediately executed I/O. Finally, there is the COMMAND.COM file. It processes typed-in user commands.

With IBM's PC-DOS 1.0, adding new PC-peripheral devices involves modifying the operating system and the IBMBIO.COM file. With PC-DOS 2.0, it is more practical to install new I/O devices because there is a Microsoft-provided mechanism to add device drivers. Thus, when PC/DOS 2.0-based IBMBIO.COM executes, it checks for the CONFIG.SYS system configuration file. It is read for instructions, which, in turn, dynamically set various operating system parameters. These instructions include the names of the device drivers to be included in the IBMBIO.COM.

Microsoft is not content to let MS-DOS remain at this level, and it is further modifying it. Version 2.0 already has a Unix-like multilevel hierarchical file structure and device-independent I/O with I/O redirection. Both are steps toward making MS-DOS more Unix compatible. For example, the file structure associates each I/O device with a device directory file. With this file, compilers and application programs need not make assumptions about a device. The operating system does all the work, and high level language-based application programs need only be recompiled for Xenix portability.

There are other improvements in the wings. For example, the firm is developing common system calls for Xenix and MS-DOS as well as porting Unix utilities and features like pipes to MS-DOS. What is more, Version 3.0 of MS-DOS will handle networking while Version 4.0 will handle multitasking. In contrast, Microsoft says there will be no multi-user MS-DOS.

how the incompatibility of different operating systems limit the ability to run many application programs. In this way, they can choose an operating system that, besides providing the desired environmental features, minimizes the compatibility problem. With an optimum operating system choice, computer designers will be able to execute the largest variety of application software for a long time, and meet the end users' ever changing needs.

From monitor programs to operating systems

Some operating environment features are available as part of the operating system itself. Others may be used as application programs that run on a particular operating system or systems. In any case, operating systems are not recognizable by those old-timers who used to call them monitor programs.

Early operating systems, programmed in mainframe machine language, got a machine ready for a job, and they were soon taking care of display and disk operations (eg, device driver routines or software). They replaced the human operator who loaded cards, turned I/O devices on and off, and manually sequenced programs. In addition, the early systems provided multiprogramming of multi-user programs, which naturally led to time-sharing. IBM's (White Plains, NY) System 360 provided what was probably the first operating system environment—albeit for a mainframe. It took care of batch and multiprocessing, time-sharing, some realtime applications, and more.

Today's microcomputer operating system environment is a descendant of early mainframe systems. It usually makes its services available independent of the application program to be run. Some observers say that building the services into the operating system is the best design approach. This reduces software overhead burdens. In addition, if these services are built into the application software, this design will prevent complex application software from executing on many of the operating systems already in place. On the other hand, some software experts feel that, for true application software portability from one operating system to another, the operating system should contain only minimal, standard software. All software providing specialized services should be in the application programs, which would then run on any standard operating system.

For harried designers who need an operating system for their latest computer designs, the Table offers some help in sorting out the facts. Compiled by Multi Solutions, Inc (Lawrenceville, NJ), it does not compare and contrast the features of all available operating systems. It says nothing about the environment-oriented operating systems that were introduced this year from vendors such as Digital Research (Pacific Grove, Calif). Moreover, some of its classifications can be debated. For example, Microsoft (Bellevue, Wash) has a Windows extension to MS-DOS. According to several independent software gurus, the Table represents the best possible list when honest differences in specification interpretation are taken into account.

The Table is particularly valuable in pointing out the environmental features available today, such as windowing, I/O facilities, and those necessary for networking. A section of the chart not shown indicates that only Multi Solution's S1 operating system supports other operating system file structures. However, two operating systems being introduced this year—Concurrent DOS from Digital Research and the latest version of the realtime VRTX operating system from Hunter & Ready (Rolling Hills Estates, Calif) provide support for CP/M and MS-DOS, and MS-DOS and Unix file structures respectively.

Before an operating system choice is made, computer designers must get the latest information from vendors and update the Table to suit their needs. In doing so, they must consider areas such as product support, price and delivery, market acceptability, microprocessor connections, and application software availability.

The main question is whether or not tomorrow's 16- and 32-bit micros will be based on Unix or a Unix look-alike.

Of course, computer designers can hitch their wagons to an already existent or rising operating system "star" that is sure to be technically adequate, at least for the purpose at hand, well supported by its supplier, and well accepted in the marketplace. In this category are Digital Research's CP/M for 8-bit systems, Microsoft's MS-DOS for 16-bit designs, and AT&T Technologies' (Murray Hill, NJ) Unix and its look-alikes for 16- and 32-bit machines.

As far as market share is concerned, these operating systems are, or are expected to be, *de facto* standards. Other operating system choices might be based on the need for special features, such as the realtime capability of Hunter & Ready's VRTX. Or, the designer can take a chance on future success and opt for the environment-oriented Concurrent DOS from Digital Research, which was announced in the middle of May 1984.

For 8-bit systems, it is a CP/M operating system world. This *de facto* standard was the first to allow application portability to different microcomputers. The secret is in its modular design concepts. Many of these are incorporated into Microsoft's MS-DOS, which in turn, in its latest released and unreleased versions, is becoming more like Unix (see Panel, "MS-DOS: the inside story"). Note, however, that the spectacular success of MS-DOS in the 16-bit world is due less to its attributes than to the success of IBM's rather mundane—at least as far as technology goes—personal computer product.

The main question is whether or not tomorrow's 16- and 32-bit microprocessor-based microcomputers will be based on Unix or a Unix look-alike. Certainly AT&T Technologies is carefully orchestrating the porting of the Unix System V operating system to the latest microprocessor offerings of National Semiconductor (Santa Clara, Calif,) Motorola, (Phoenix, Ariz), and Intel (Hillsboro, Ore). This would neatly take care of the major contenders for microprocessors for tomorrow's 16- and 32-bit workstations, other high end machines, and maybe even microcomputers. As higher power processors get into microcomputers, these machines will have the ability to handle minicomputer-oriented Unix.

Whether or not Unix should run on a microcomputer is an open question. By design, Unix is a multiuser system. This fact would seem to contradict the single-user concept with which the microcomputer is often associated. Nevertheless, IBM has come up with a multitasking, but single-user Unix for its PC. Developed by Interactive Systems (Santa Clara, Calif) for IBM, the multi-user capability is just not called upon (see Panel, "Unix on the IBM PC: a software kluge?").

Of course, AT&T's Unix has lots of look-alike competitors that are not ready to be counted out of the fray. And, Unix itself has its own problems because it is relatively old as operating systems go, and not designed for many of today's requirements. For example, the University of California at Berkeley has its Berkeley 4.1 and 4.2 BSD versions of Unix. Many of the features that AT&T's Unix lacks (eg, networking, memory management, and sophisticated file systems) are provided by Berkeley.

Berkeley 4.2 is available on the IBM PC by means of an add-on board from Sritek, Inc (Cleveland, Ohio). Sritek uses a National Semiconductor NS16032 microprocessor (running as a coprocessor) as the basis for its board. The NS16032 uses the Intel 8088 only as an I/O processor. This design allows the computer designer with a PC to call on an operating system with advanced capabilities.

Now that Unix is being marketed at reasonable prices, AT&T is concerned with providing the best possible system. According to AT&T, the new Unix versions will provide Berkeley-like features. It remains to be seen if these features will migrate to microcomputers as a long-range result of System V being ported to the latest 16- and 32-bit microprocessors.

With the advent of Unix, rivals AT&T and IBM have got one foot in the same door. If IBM licenses and develops a Unix for its mainframes, Unix can provide the much heralded micro-to-mainframe connection. An entire generation of managers is waiting for this connection to help tap mainframe data bases at individual desks. On the other hand, IBM has a proprietary mainframe operating system—VMS—that it is porting to its microcomputers. IBM's wealth of software is tied up with the VMS and its other mainframe operating systems. For this reason, IBM would have no desire to stop making these products.

Operating system communications

While all of this microcomputer operating system activity is going on, the computer designers who come up with networks to access remote resources (eg, laser printers, mainframe data bases, disk and file servers, and other designers' microcomputers), have a special problem. They must communicate with a variety of operating systems or the network is useless. One way around this problem is to implement software (as extensions to all the network's operating systems) that creates a network operating system environment. This software can take the place of, for example, translator software for each different computer. It can also serve until the International

Standards Organization's (ISO) seven-layer model for computer communications is a reality and an agreed-upon standard protocol software is available.

One of these operating system extensions, which is roughly equivalent to ISO transport layer software, is the PC-NOS operating system extension from Applied Intelligence (Mountain View, Calif). PC-NOS allows certain disparate, networked microcomputers to communicate regardless of network or operating system form.

There are many other network operating systems. For example, Orchid Technology (Fremont, Calif)

Feature Comparisons of Representative Operating Systems—Part 1

	Concurrent (CP/M	CP/M	MP/M II	MS-DOS	Oasis	Pick	p-System	S1	Unix	Xenix
System Structure										
Portability										
Written: high level language	yes	yes	yes	no	yes	no	yes	yes	yes	yes
Device independent	no	no	no	no	yes	yes	yes	yes	yes	yes
Machine language implementation	yes	yes	yes	yes	yes	yes	no	yes	yes	yes
Modularity										
Replaceable components	no	no	yes	some	no	no	no	yes	some	some
Removable components	no	no	yes	no	no	no	no	yes	few	few
Extendable	no	no	yes	no	no	no	no	yes	no	no
Movable										
Variable storage requirements	yes	no	yes	no	no	yes	yes	yes	yes	yes
Adjustable storage location	yes	no	yes	no	no	yes	yes	yes	yes	yes
Application Portability										
Standard source level system calls	no	no	no	no	no	yes	yes	yes	yes	yes
Machine language implementation	yes	yes	yes	yes	yes	no	no	yes	yes	yes
File byte order standard	yes	yes	yes	yes	yes	no	no	yes	no	no
File System										
File name length	11(8,3)	11(8,3)	11(8,3)	11(8,3)	16(8,8)	32K	15	64	14	14
Minimum file size	0	0	0	0	256	0	0	0	0	0
Maximum file size	32 Mbytes	256 Kbytes	32 Mbytes	4 Gbytes	350 Mbytes	unlimited	16 Mbytes	unlimited	4 Gbytes	4 Gbytes
Allocation										
Single contiguous	no	no	no	no	no	no	no	yes	no	no
Extents	yes	yes	yes	no	no	no	yes	yes	no	no
Linked	no	no	no	no	no	no	no	yes	no	no
Mapped	no	no	no	yes	no	no	no	yes	yes	yes
Record size variable	yes	no	yes	yes	yes	yes	yes	yes	yes	yes
Record lock	yes	no	yes	no	yes	yes	no	yes	no	no
System/user manage I/O buffer	no	no	no	no	no	no	no	yes	no	no
File system security passwords	no	no	yes	no	yes	yes	no	yes	no	no
Shared access control	no	no	no	no	yes	yes	no	yes	yes	yes
Hierarchical directories available	no	no	no	no	no	yes	no	yes	yes	yes
Removable	no	no	no	no	no	no	no	yes	no	no
Maximum no. files on disk	8192	64	8192	64	unlimited	unlimited	77	unlimited	unlimited	unlimited
Record files available	yes	yes	yes	yes	yes	yes	yes	yes	no	no
Removable	no	no	no	no	no	no	no	yes	no	no
Minimum record size	128	128	128	1	0	0	2	0	no	no
Maximum record size	2048	128	2048	64 Kbyte	350 Mbytes	32 Kbytes	32 Kbytes	4 Gbytes	no	no
Random access files	yes	yes	yes	yes	yes	yes	yes	yes	no	no
Stream files available	no	no	no	no	yes	no	yes	yes	yes	yes
Random access	no	no	no	no	yes	no	no	yes	yes	yes
Keyed files available	no	no	no	no	yes	yes	no	yes	no	no
Removable	no	no	no	no	no	no	no	yes	no	no
ISAM	no	no	no	no	yes	no	no	yes	no	no
VSAM	no	no	no	no	no	no	no	yes	no	no
B-tree	no	no	no	no	no	no	no	yes	no	no
Command Processor										
Replaceable	no	no	no	yes	no	no	no	yes	yes	yes
Menu driven	no	no	no	no	no	no	yes	yes	no	no
Command driven	yes	yes	yes	yes	yes	yes	no	yes	yes	yes
Command procedures available	yes	yes	yes	yes	yes	yes	no	yes	yes	yes
Removable	no	yes	no	yes	no	yes	no	yes	no	yes
Variables	no	no	no	no	yes	yes	no	yes	yes	yes
Conditional execution	no	no	no	no	yes	yes	no	yes	yes	yes
Error handling	no	no	no	no	yes	yes	no	yes	yes	yes
File I/O	no	no	no	no	no	yes	no	yes	no	no

has its environment to hook up IBM PCs. And, operating system extension software from Rair Computer Corp (Santa Clara, Calif) allows microcomputers with CP/M or CP/M-like operating systems to communicate. Computer system designers and integrators can apply these operating system extension ideas to their own projects.

Local networks have been slow in coming. So, another approach to computer communications is to recognize that computer data-handling networks need not be based on collision detection or token passing. They can, for example, combine voice and data transmission on a proprietary time-division multiplexing network. Telenova, Inc (Los Gatos, Calif) has come up with an object model decomposition-based operating system to run such a network. Computer system designers can use object modeling wherein functional software blocks are developed from specifying common operating system tasks, for their own microcomputer networks. They can also use the Telenova network design as the basis for integrating a variety of computers into a network.

Feature Comparisons—Part 2

	Concurrent (CP/M	CP/M	MP/M II	MS-DOS	Oasis	Pick	p-System	S1	Unix	Xenix
Commands										
Backup and restore	some	no	some	yes	yes	yes	no	yes	yes	yes
Compare	no	no	no	yes	yes	no	no	yes	yes	yes
Cryptographic functions	no	no	no	no	yes	no	no	yes	yes	yes
Disk formatting	no	no	no	yes	yes	yes	no	yes	yes	yes
Electronic mail	no	no	no	no	yes	no	no	yes	yes	yes
File system validation	no	no	no	yes	yes	yes	no	yes	yes	yes
Sort	no	no	no	no	yes	yes	no	yes	yes	yes
Supervisor Facilities										
Multi-user available	no	no	yes	no	yes	yes	no	yes	yes	yes
Removable	no	no	no	no	no	no	no	yes	no	no
Multitasking available	yes	yes	yes	no	yes	yes	no	yes	yes	yes
Removable	yes	no	no	no	no	no	no	yes	no	no
Multitasking per user	yes	no	yes	no	no	no	no	yes	yes	yes
Multiprocessing (task can run on any CPU)	no	no	no	no	no	no	no	yes	no	no
Removable	no	no	no	no	no	no	no	yes	no	no
No. of simultaneous processors supportable	1	1	1	1	1	1	1	256	1	1
Synchronization										
Semaphores	yes	no	yes	no	no	no	no	yes	no	no
Locks	yes	no	yes	no	no	no	no	yes	no	no
Networking										
Available	no	yes	no	no	yes	no	no	yes	no	no
Removable	no	no	no	no	no	no	no	yes	no	no
Usable from any program	no	no	no	no	no	no	no	yes	no	no
Recognized by file system	no	no	no	no	no	no	no	yes	no	no
Windowing										
Available	no	no	no	no	no	no	no	yes	no	no
Removable	no	no	no	no	no	no	no	yes	no	no
Separate task per window allowed	no	no	no	no	no	no	no	yes	no	no
Non-tasking windowing	no	no	no	no	no	no	no	yes	no	no
Terminal Support										
Full-screen available	no	no	no	no	yes	no	yes	yes	no	no
Removable	no	no	no	no	yes	no	yes	yes	no	no
Usable by any program	no	no	no	no	yes	no	yes	yes	no	no
Bit-mapped display support available	no	no	no	no	no	no	no	yes	no	no
Removable	no	no	no	no	no	no	no	yes	no	no
Printer Support										
Available	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes
Removable	no	no	no	no	no	no	no	yes	yes	yes
Spooling available	yes	yes	yes	no	yes	yes	no	yes	yes	yes
Removable	yes	yes	yes	no	yes	no	no	yes	yes	yes
Bit-mapped printer support available	yes	no	no	no	no	no	no	yes	no	no
Removable	yes	no	no	no	no	no	no	yes	no	no
Plotting Support										
Standard graphics control	yes	no	no	no	no	no	yes	yes	no	yes
Spooling available	yes	no	no	no	no	no	no	yes	no	yes
Removable	no	no	no	no	no	no	no	yes	no	yes

There is no end of operating system vendors; most have a product with some unique element. However, there is a price for this uniqueness. Application program portability between these operating systems remains an elusive goal.

While CP/M, MS-DOS and Unix versions make their mark, there are the offerings from the various semiconductor manufacturers. These are typical of the lesser known, but nevertheless useful, operating systems for computer designers. For example, Intel, Motorola, National Semiconductor and Mostek (Carrollton, Tex), have Unix look-alikes, realtime operating systems, and proprietary operating systems geared to specific microprocessors and their development systems.

For computer designers whose companies tap the business-user market, a wide choice of operating systems is available. The multi-user Oasis operating

Unix on the IBM PC: a software kluge?

There have been Unix-like operating systems available for the IBM PC for some time, as evidenced by names such as Coherent, Idris, Xenix, and Venix. But IBM has ignored all of them and contracted with Interactive Systems to come up with an IBM-blessed and AT&T Technologies-licensed Unix.

Perhaps IBM hopes to tap the vast pool of university trained software people who are familiar with Unix and wean them to its PC. Or, perhaps, it just wants to make money on both the Unix and PC bandwagons that show no signs of abating. Certainly Unix is no major operating system with IBM's mainframe customers who are used to IBM's operating system offerings. In fact, IBM is porting subsets of these operating systems to PCs so they can directly hook to mainframes. And, IBM certainly does not care to put its stamp of approval on AT&T's offering.

What is probable is that because of Unix's marketing, IBM realizes that the computer community perceives Unix as a future standard, wants it, and wants to be compatible with it. After all, IBM is not about to stop giving its customers what they want and covering all its operating system bases.

What is the use of Unix on a PC? Certainly it is an environment with comprehensive utilities. And, it is only unfriendly to the uninitiated. Experienced software people swear by it because of its power. Finally, there is no doubt that if PC users have their machines hooked to minicomputers or mainframes running Unix, they enjoy the benefits of Unix's portability and need learn only a single operating system interface.

Network server processes are also well served by multitasking Unix which can run them as background tasks while an application program runs in the foreground. MS-DOS can be modified to accomplish this feat but it is not often done nor is it necessary.

Running Unix on the PC presents several practical problems. First, there is the PC's Intel 8088. It is not as versatile as the Motorola 680X0 family or the National XX032 in handling Unix. For example, the 8088 is less able to deal with address space requirements, memory protection, interrupt handling, memory allocation, and certain kinds of error handling.

IBM does not make a microcomputer based on either the National or Motorola microprocessors except for one scientific workstation whose price is greater than that of a PC by a factor of 10. The PC and other IBM-developed PC-like microcomputers so far appear to be the whole ballgame for microcomputer-based Unix as far as market-conscious IBM is concerned.

The biggest drawback of the PC is lack of memory management capability—critical when running multitasking operations such as a networked PC executing an application program. With Unix, multiple tasks are run, even though memory is finite, by swapping blocks of code and data between disk and memory as they are needed and under Unix control. In contrast, with MS-DOS, and with the 8088, swapping is controlled by the application program.

Memory management not only takes care of swap management, it allocates main memory locations, and isolates executing processes so they cannot get in each other's way. One way around these problems—at least in part—is to off-load the 8088 with peripheral controller chips that free it from some of its I/O chores. Then PC-IX can execute more efficiently. And, memory management can be added by clever circuitry. These approaches have been taken, for example, by Altos Computer Systems (San Jose, Calif). Sritek also helps computer system integrators get memory management into the IBM PC by providing add-on coprocessor boards.

There is yet another problem. With single-tasking MS-DOS, it is possible to swap (or overlay as it is known) large numbers of bytes (perhaps kilobytes) since the one application program can keep track of the swaps without difficulty or major software overhead. It is a different story, however, with Unix and multiple, concurrent applications. Now, it is difficult to track large data blocks so Unix works with small (2- to 4-Kbyte) chunks of memory known as pages. These can be readily found in a short time.

Page swapping is best handled by dedicated memory management hardware—this minimizes the overhead burden and the time taken. None is to be had in the PC environment. The IBM/Interactive Systems solution is to control swapping in software. This design slows down the operating system but what this slowing down translates to in a multitasking PC-IX environment is slower program execution compared to the time they would take if they were running alone on MS-DOS. Slower execution is most noticeable in an I/O intensive as opposed to a compute-intensive environment. Whether or not slowing down is a problem, of course, depends on the application. With another, more suitable processor, Unix has no such problem and the benefits of multitasking are preserved.

The size of the PC's 10-Mbyte hard disk is also a problem. About 8 Mbytes can be taken by Unix but a 5-Mbyte subset is said to be enough for many PC-IX applications. Even so, some observers feel that 5 or so Mbytes is not enough to split between multiple users who will, for example, if they are engineers/designers, run a lot more software than relatively small word processing programs.

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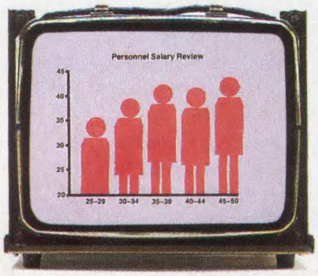

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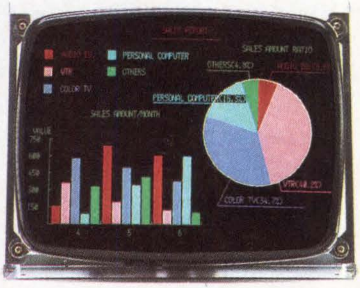

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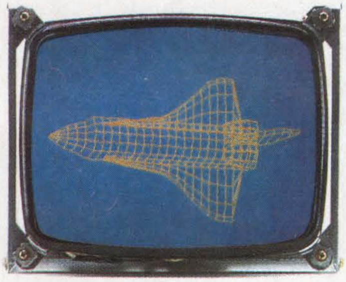

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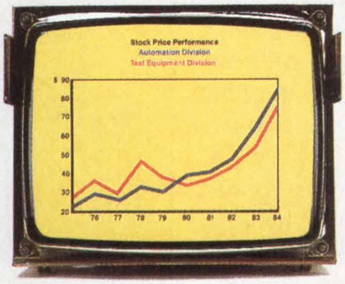

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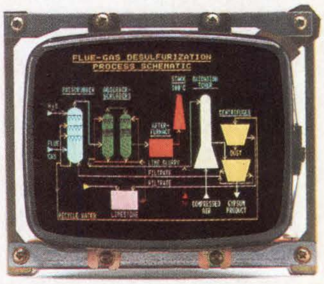

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ADVANCED AND EVER ADVANCING

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system from Phase One Systems (Oakland, Calif) sports Unix-like features made practical for the realities of a multi-user business environment. For example, unlike original Unix, which is multi-user but set up for a research environment, Oasis has file- and record-locking, and a user friendly job control language.

Oasis, of course, is not the only choice for business applications. Microsoft's Xenix is the most widely sold Unix look-alike. Microsoft sells it, as does Intel, National, and even IBM on one of its scientific workstations. Then there is the database management oriented Pick operating system from Pick Systems (Irvine, Calif). It has been around almost as long as Unix, and is being ported to a wide variety of microprocessors. Along with its virtual memory management capabilities, it will soon sport a C compiler that supports Unix applications.

Other Unix-type systems include Coherent from Mark Williams (Chicago, Ill), which already runs on the IBM PC, Idris from Whitesmiths, Inc (Concord, Mass), and Venix from VenturCom (Cambridge, Mass). Venix comes already ported on a 10-Mbyte hard disk that fits in the IBM XT. The VenturCom product is a perfect example of how computer system designer/integrator needs may be satisfied by other integrators combining operating systems with ready-to-use hardware.

The RM-COS operating system from Ryan-McFarland (Rolling Hills Estates, Calif) is the best example of business computer applications that do not need Unix or its look-alikes. This operating system is geared to the business application-oriented Cobol language. Also available on the IBM PC through a Sritek coprocessor board, this operating system features a very small size for its power—even with a built-in compiler. Its secret is its portable Cobol which, similar to the p-System compiles to produce C-code for a hypothetical C-machine (see Panel, "Where the p-System fits in"). Like the p-System, its application program execution speed suffers because of the intermediate code, but this is of little concern in business applications that tend to be I/O bound anyway. The C-coded object programs produced by the Ryan-McFarland compiler are portable across CP/M, Unix, and other operating systems. This is because system calls are not issued by the C object code, but by an emulator specific to each operating system.

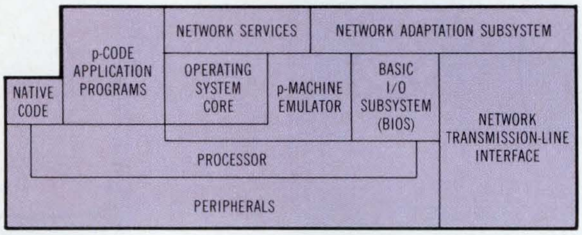
Searching for a standard

Although there appear to be as many (or more) operating systems as programming languages, and full communication between operating systems seems to be a lost cause, there is hope. Clearly, if there were a set of rules for writing operating systems, there might be more compatibility among them. Such rules or standards are being worked out by the IEEE's Microprocessor Operating System Interface (MOSI) Task Group 855. These are known as the MOSI interface.

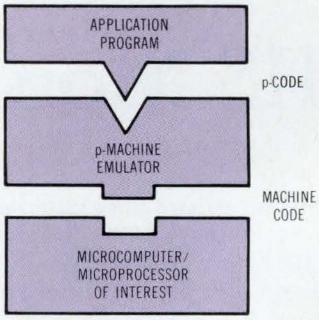
With an interface, application developers write their software for the MOSI interface software which, in turn, communicates with specific operating system software (see the Figure). The interface software translates system calls and functions from the application program to the operating system in question. The approach is like the virtual terminal

Where the p-System fits in

SofTech's (San Diego, Calif) p-System operating system is designed to allow maximum application program portability. It is presently less than marketplace-successful because of marketing and application program execution speed problems. However, the p-System operating system is an elegant example of what can be done when portability is a design criterion in the first place. Inexpensive to implement, it has been ported to most popular microprocessors and microcomputers. Not giving up on it, SofTech, Inc has introduced p-System extensions in the form of an ISO-like networking environment [see Figure (a)].



(a)



(b)

Originally developed by the University of California at San Diego, the p-System achieves object-code portability across a variety of microcomputers with a simple design principle. The p-System based applications and compilers are written only once for a hypothetical p-machine. They port from one machine to another because they need only communicate with an easy-to-write emulator that is machine-specific on one side and p-machine-specific on the other [see Figure (b)]. All that need be done for a new machine is write the emulator. The technique is spreading. For example, as mentioned, the Ryan-McFarland Cobol RM-COS operating system makes use of it and BOS National (Dallas, Tex) has a similar intermediate code-based operating system.

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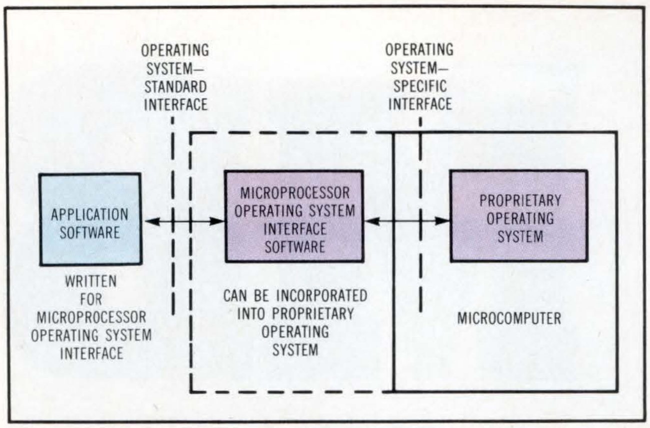

The IEEE's Microprocessor Operating System Interface (MOSI) Task Group 855 is charged with devising a standard interface so that application programs can communicate with diverse operating systems. The interface will translate system calls and functions as shown.

protocol under ISO development (see Panel, "What MOSI is up to").

MOSI is not the only operating system standardization effort. With the multiple Unix flavors that are around, it was only a matter of time before some standards-making efforts got under way. For example, Unix interfaces are being defined by various Unix user groups.

These standards-making efforts are notable. Like all such voluntary endeavors, however, they take time because a wide variety of people and proprietary interests must be accommodated. Several firms have announced their intentions to conform to standards if they are developed, but much work remains before there is marketplace impact. However, the members of the various operating systems standards committees believe in what they are doing and point to ISO's computer communication protocols success (see *Computer Design*, June 15, 1984, p 57). They claim that the operating system standards are no less important.

Other solutions abound

There are other methods besides intermediate code and interface standards to get around the operating system incompatibility problem. In fact, work is proceeding apace throughout the software community. Other methods include operating system runtime libraries, emulators, and portability guidelines for compilers. Which of these is suitable for a given compatibility problem depends, among other factors, on whether or not the execution environments provided by the microcomputers are the same. For example, computer graphics and memory management may or may not be operating system independent.

Operating system compatibility is a matter of defining what an application program may expect from an operating system when it attempts to communicate with it. Individual operating environments handle networks, windows, memory management, and other computer environment features differently (eg, system calls for these services are usually unique to the operating system in question). Naming conventions for files are different, as are file formats, etc. These parameters are often different even in updated versions of what is nominally the same operating system from one manufacturer.

This unfortunate state of affairs is being reversed by some suppliers. Most notably, AT&T Technologies

What MOSI is up to

The IEEE's Microprocessor Operating System Interface (MOSI) Task Force 855 has several hundred members dedicated to coming up with a standard operating system interface. This interface will allow application software to be written for its standard interface "side." This in turn, will be converted by interface software so it can interface or communicate with a particular operating system connected to the other side of the interface software.

Representing most software, computer, and semiconductor firms with a smattering of other interests, the task force members are trying to agree on how such operating system chores as memory management (for example, how memory is allocated), time management (how a software process is delayed), synchronization and communication (how processes are created and destroyed), and exception handling (what happens when there is a parity error) should be handled by the MOSI interface. MOSI must define inputs and outputs for each of these categories or, equivalently, what functions can (or should) be expected.

Some MOSI tasks are more difficult than others. For example, much debate has gone into how the standard should deal with file systems. Each operating system handles files in its own way. Like all standards efforts when there are well-established contenders for honors, only a minimal set of file specifications will show up in early MOSI documents.

MOSI offers a choice of two paths to success. Either software designers can be convinced to write software for a specific MOSI interface that would interpret such software for a particular operating system; or, designers of new operating systems can conform to the MOSI interface and thereby run properly designed application software directly.

Whether there will be such standard interfaces remains to be determined. Operating systems, like programming languages, are matters of personal preference as well as matters of technology. In an industry that depends on software designers who are usually quite individualistic, personal preference is a big issue. This is one of the reasons why MOSI has opted for classes of standardization. These four, known as A, B, C, and D, also accommodate operating systems with fundamental differences in capability. For example, if an operating system does not support windows, no interface can make it do so.

Voting for MOSI has started. Ultimately, all of MOSI's classes will be voted on by the committee members, approved, submitted to the IEEE for consideration as a standard, made available for public comment, and finally made a standard. Then, time will tell if the computer industry adopts them.

is taking great pains to control the porting of Unix System V. AT&T and, for example, the semiconductor firms doing the porting job, are working together to ensure that, while value-added features will appear as computer designers do their job, a minimal standard of portability from one microprocessor's Unix to another processor's Unix will be possible. AT&T calls this a generic port.

One of these porting efforts involves Digital Research working with Intel to port System V to the Intel virtual memory-based iAPX 286 microprocessor. Actually, the Digital Research/Intel effort is but one step in Digital Research's counterattack to regain a dominant position in the operating system marketplace. Smarting from Microsoft's *de facto* dominance of the 16-bit market because of its MS-DOS-IBM connection, and well remembering how it enjoyed CP/M's 8-bit market mastery, Digital Research is also working with AT&T to publish, test, and market third-party System V application software. It is also helping to define System VI which, it is said, will run CP/M files and Digital's Graphical Kernel System (GKS). (See *Computer Design*, May 1984, p 167.) Digital Research will also supply Motorola with languages and applications for the 68000 microprocessor family's already announced System V port.

Making look-alike operating systems

It is possible to make operating systems behave in similar ways simply by making them look alike. Thus, Microsoft is designing advanced versions of its MS-DOS with Xenix/Unix features. And, Oasis has Unix's system calls. This approach is limited because it cannot account for fundamental operating system differences.

A more flexible technique is that of using high level compilers and languages. Compilers, specific by design to an operating system and a microprocessor, generate the instructions that a microprocessor needs to execute a particular application. They also generate the operating system's system calls. So, assuming that an application is written in a high level language for which a compiler exists, recompilation ports the program from one computer system to another.

Unfortunately, the computer designer's life is not so simple. The necessary compilers are not available and are not easy to write. Worse, if the application software directly communicates with a machine's specific hardware without the operating system as an intermediary, nothing can be done. For example, as is well known, MS-DOS application programs run on the IBM PC. In contrast, PC-DOS applications—software written for the PC that uses its unique hardware—do not always run on MS-DOS.

Compilers, regardless of their complexity, still have a portability role to play. For example, there are compiler standards that have been established. Many of these are related to the C language, the intermediate to high level language, in which Unix is written.

The runtime library technique helps make the differences between operating systems disappear. A runtime library allows application software written for one operating system to run on another by compiling the application and linking it with software (the runtime library) whose function is to provide the software routines and functions of the target operating system. In other words, a runtime library allows source programs written in one operating system to link to another's system calls and commands.

Clearly, runtime libraries must be specifically written for the source and target operating systems. Most importantly, in the runtime library concept, the source operating system still performs its designed-in chores. Digital Research has been active in this area and Hunter & Ready's VRTX clearly takes advantage of it.

While source-code compatibility is a major problem for computer system designers and integrators, they cannot ignore the object-code compatibility problem when they come up with their computer systems. Networked computer systems provide a particularly good example of this problem. The diverse computers in a network most likely run different operating systems. Normally, they cannot run the same applications unless disks are purchased separately (if they are available) for each operating system—an expensive proposition. What is more, much application software is distributed as object code—originators guard their design secrets well—so it is particularly important that this software be accessible to many operating systems.

As can be seen, there are some methods for achieving object-code compatibility. For example, the SofTech Microsystems p-System provides object-code compatibility, as does Ryan-McFarland's RM-COS. And, Microsoft's Xenix and Unix have a Microsoft-derived common object-code module format for computers with the same microprocessor.

There are still other techniques. Some depend on application program/operating system software interfaces that isolate the two; others depend on the time honored operating system emulation technique. Still, much work remains to be done before a floppy disk can be put into any microcomputer and run an application—even when the microcomputer's microprocessors are identical.

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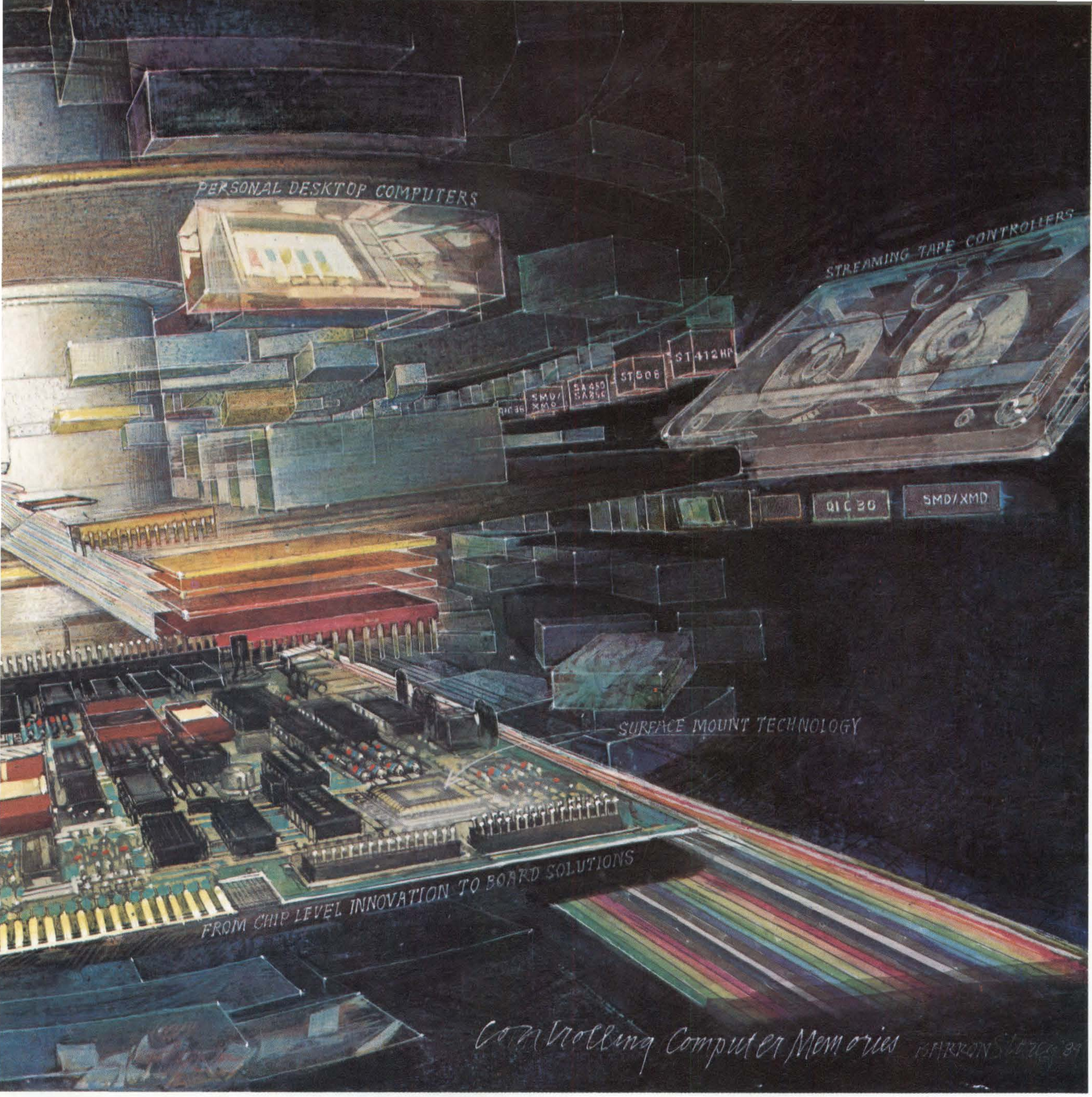

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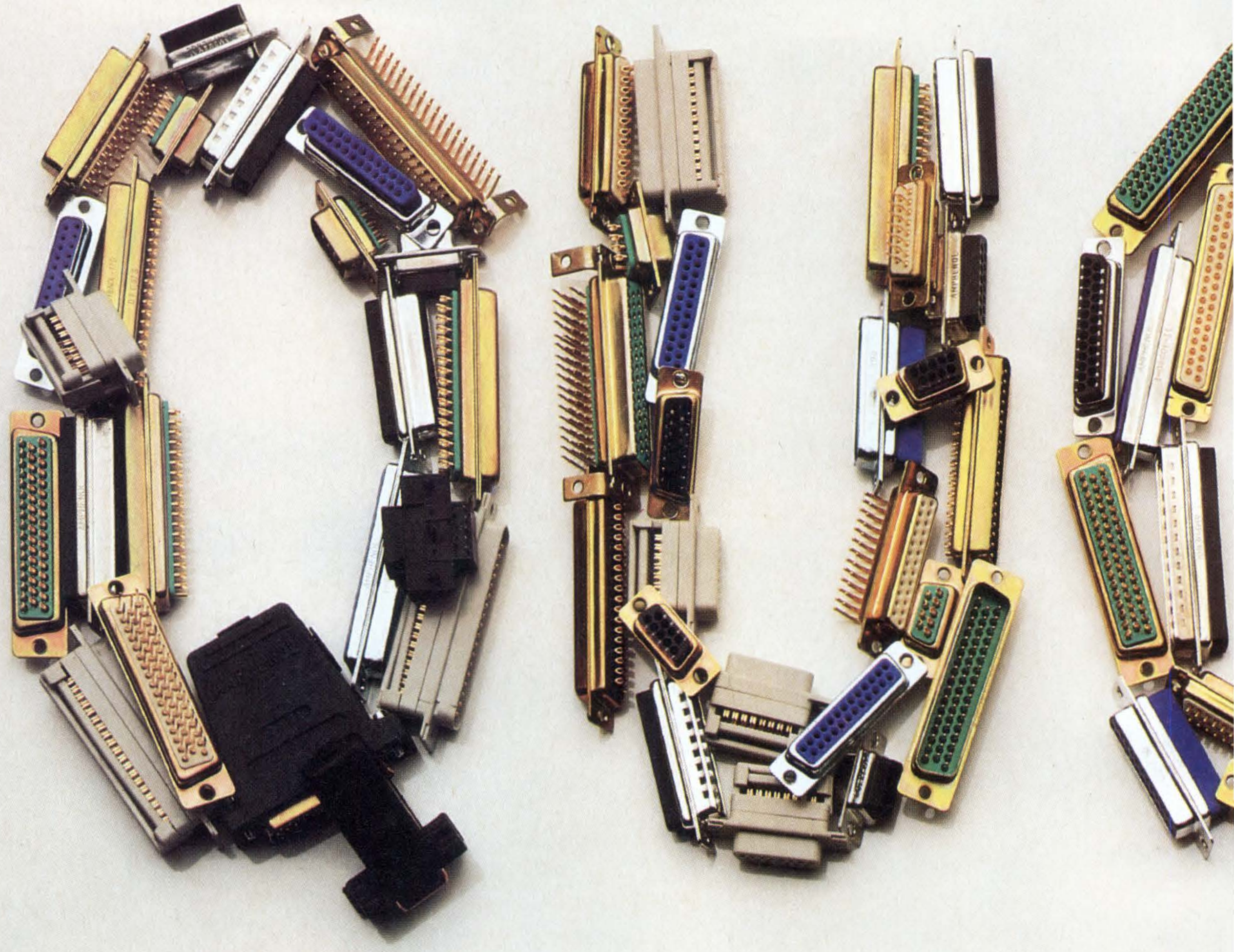

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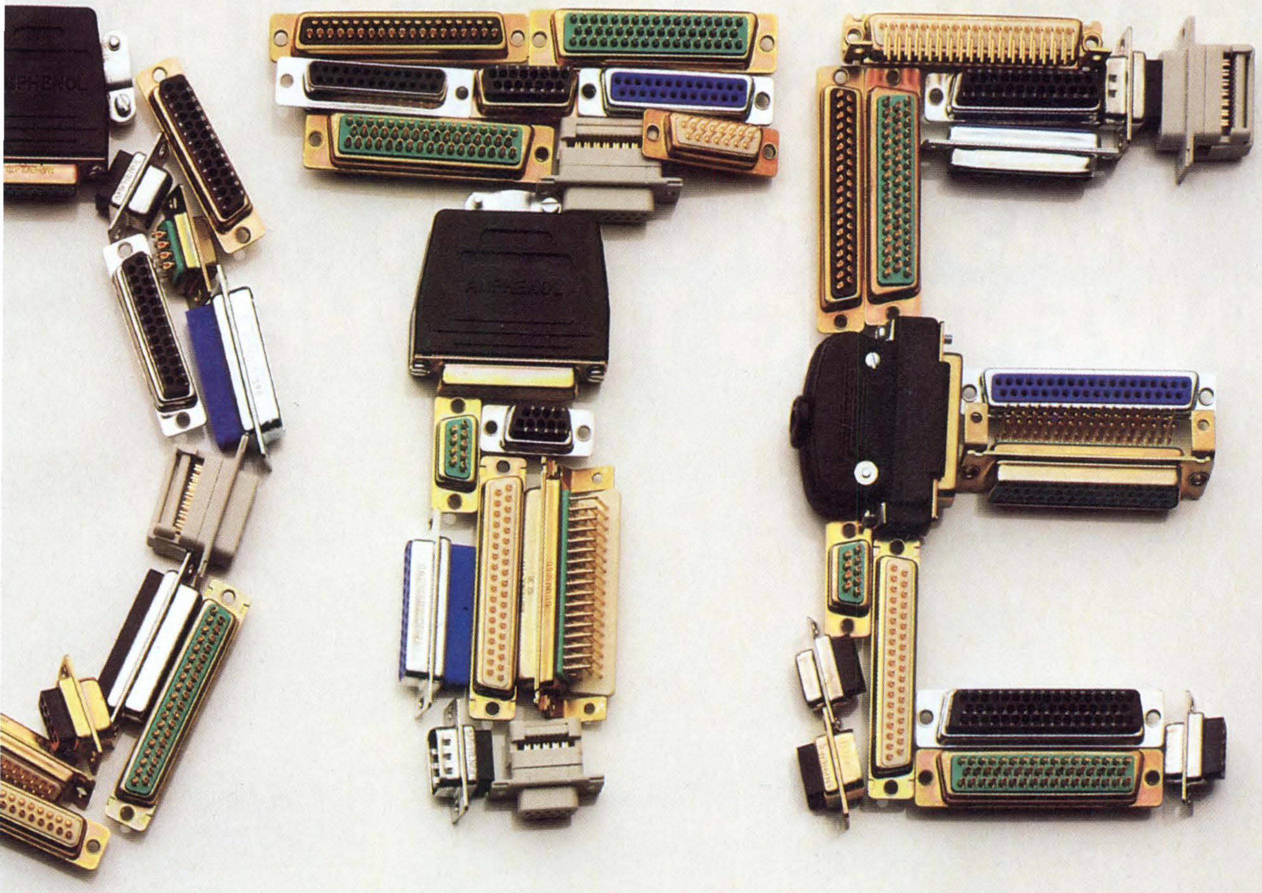

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CIRCLE 89

OPERATING SYSTEM EXTENSIONS LINK DISPARATE SYSTEMS

When a network connects microcomputers from different manufacturers, it is likely they cannot communicate without help. Software routines and modules help save the day.

by John Row and David Daugherty

Computer system integrators, program developers, and end users alike can easily be confused by today's array of new, complex computer operating systems. The problem is at its worst in a networked, distributed processing environment because of the diverse computers and operating systems that need to communicate. Network users simply do not want to deal with either the intricacies of each computer's particular operating systems, or the communication (or lack thereof) between a resident operating system and another, different operating system in the network.

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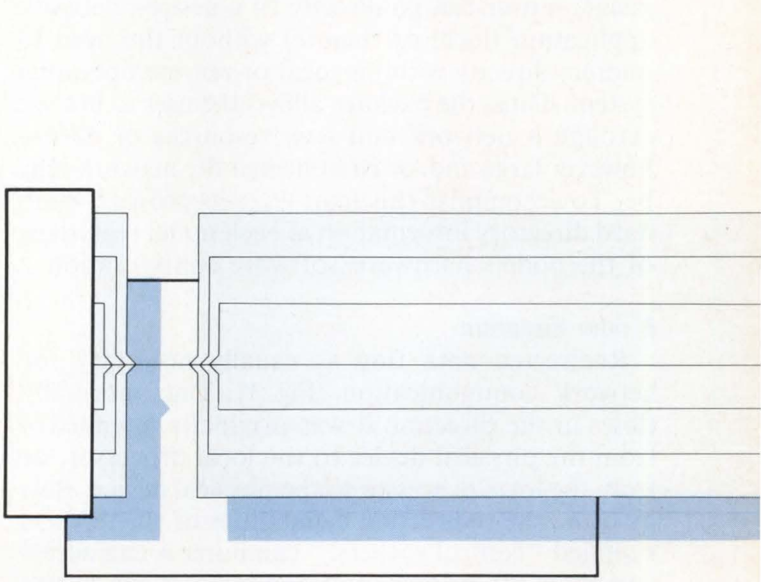
David Daugherty is a senior engineer at Applied Intelligence, Inc. He holds a BA in computer science from the University of California at Berkeley.



One possible solution to this operating system babble problem is the Personal Computer/Network Operating System (PC/NOS), a package of software routines and modules. Its standard form accomplishes what used to be possible only after the arduous writing and testing of software specifically designed for given networks, computers, and operating systems. In other words, PC/NOS is a network product composed entirely of software that is not tied to a particular operating system, network, or hardware configuration.

The intention of this software package is not to define a new operating system, but to define, in simplest terms, a set of software primitives that can be used to describe any existing operating system or computer system. It is strictly a message-passing

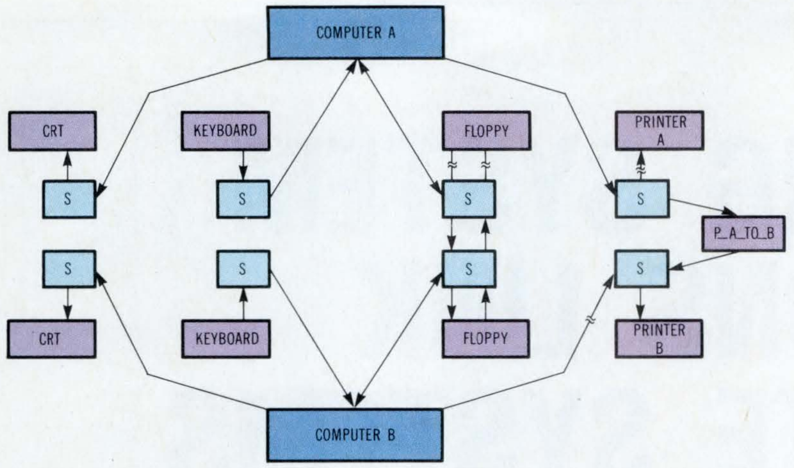


Fig 1 The operating system performs data flow redirection. Control sockets (the boxes marked "S") have been inserted between the peripheral devices and the processor. The CRTs and KEYBOARDS are operating normally. Computer A is using computer B's printer. There is a translator program P_A_TO_B that handles mapping control command sequences from printer A to printer B. Computer B is using computer A's floppy drive. In this case, computer A is also using its own floppy drive.

operating system extension that makes no assumptions about the organization of the resident or networked operating systems with which it works.

Briefly, the operating system is a standardized, user-transparent communication link between disparate network elements. With the its command language, a user can go directly to a desired network application (local or remote) without the need to interact directly with his local or remote operating system. Thus, the package allows the user to browse through a network and seek resources or data—however large and/or complicated the network may be. To accomplish this feat, PC/NOS provides standard directory information at each node, regardless of the node's hardware/software configuration.

A new direction

Redirected data flow is usually necessary for network communication (Fig 1). Data normally flows in the direction it was originally intended—from the physical device to the local processor, or from the local processor to the physical device. But, by using the redirection capabilities of the PC/NOS supplied "control sockets," computer A can access computer B's printer, and computer B can access computer A's floppy disks. This is just the kind of activity desirable in a networked distributed processing environment.

The sockets know how to use the communication channel between computer A and B through a limited and well-defined interface. In fact, the drivers that are streaming data through the sockets do not know anything about the actual workings of the communication channel, or even that the channel exists. Having the communication channel transparent to the drivers is very important since it means that programs using the drivers can make use of redirected data streams without being modified.

Redirected data flow—the heart of the PC/NOS system—may be further understood by considering how a telephone conversation takes place. If person A wants to talk to person B, A does so by dialing B's number, and the telephone system internally sets up a series of connections from person A's phone to person B's phone. When A hangs up, the telephone system must tear down these connections, transparently to A. Person A is not interested in these internal details. All person A cares about is picking up a phone, dialing a number, talking to person B, and hanging up. Later, person A goes through the same process to talk to someone else, this time dialing a different number.

The software package operates very much like the telephone system just described. A common connection language sets up connections between various network devices so that data can flow between them without user interference.

PC/NOS is analogous to an operating system's operating system. As it coordinates and facilitates communications, it relates to a standard operating system in the same way that an operating system relates to user or application programs. As mentioned earlier, it is a purely software product consisting of a number of modules that run on different host operating systems and hardware configurations, which are connected together by a network. When thus connected, the standalone computer becomes a node in a distributed computing environment. In practice, the network need only implement any form of message-oriented communication, even a non-instruction-fetch backplane connecting independent processors. Or, it could be a message-oriented bus such as the Small Computer System Interface (SCSI) bus.

Having divided the host system into any number of standard computing entities defined in a standardized connection or socket table at each node, PC/NOS allows interconnection between these entities with a message-passing protocol. The interconnections may be actual physical network connections between machines or logical connections within an existing standalone system.

The ISO connection

The PC/NOS package is based on levels 4 through 7 of the International Standards Organization (ISO) reference model for computer communications. Level 4, the transport layer, provides end-to-end data integrity protocols. To accomplish its task at level 4, PC/NOS requires what is known as "reliable datagram service." If this service is not provided by the host network, there are software modules for the PC/NOS that do.

For their part, the search and connect facilities of the session layer (layer 5) provide the user with the ability to search for, and connect to, any available network resource. This feature is PC/NOS-implemented with interactive windows that show available resources and existing connections. The windows also implement the execution of connection requests.

Application-level (layer 7) software has full access to the PC/NOS features using the software package's programmable interface. In addition, some PC/NOS modules (for example, the Back-end Servers), can themselves function as applications.

Details of the actual modules incorporated into a given network installation depend on the services provided by a host network. On Omninet, for example, which provides a reliable data-link service, PC/NOS provides some level 4 functions, such as end-to-end flow control. It also supplies some level 5 and level 7 functions. Using the Xerox Corp XNS network protocols, however, PC/NOS is configured above the XNS-provided transport layer and uses the most primitive datagram service provided at that level.

Its manner of describing system components in standard ways allows PC/NOS to define a connection or common International Standards Organization (ISO) based session layer language throughout the distributed network system (see Panel, "The ISO connection"). The purpose of the ISO seven-layer model for computer communications is to make communications operating system-, network-, device-, and processor-independent. PC/NOS software satisfies this requirement.

Yet to come

Currently, PC/NOS provides interfaces to CP/M 2.2, CP/M-86, and MS-DOS 1.1/2.0. Plans are underway to support other common operating systems such as Unix, CP/M 3.0, and Concurrent DOS (see Panel, "Relating Unix and PC/NOS"). Four networks are currently accommodated: Corvus Omninet; PC-BUS, from TriComp Polytechnical Inc; Televideo's Network; and Morrow's Network. In addition, configurable modules are provided for the creation of network file and print servers.

Network access via PC/NOS is completely point to point, thus providing a true distributed processing environment. It does not require centralized control from such devices as back ends, but allows them to be integrated into the distributed environment. As might be expected, PC/NOS can interface with networks that provide datagram or virtual circuit service. To do this, it offers transport-level functions (eg, end-to-end sequenced protocols) if the services provided by the host network are not adequate.

Although PC/NOS does not allow all applications to talk to all nodes, it does provide the structure for conversion or virtual terminal modules. These can be loaded and connected by the PC/NOS command processor in a manner transparent to the user.

The telephone analogy also helps in understanding PC/NOS features. Suppose person A wants to talk to person B in a foreign country. First, A dials the

Relating Unix and PC/NOS

There are a number of different approaches to network a multi-user operating system like Unix. Unfortunately, no single solution provides all the answers to the problems that arise. The PC/NOS approach to the problem is to provide a number of different ways to connect Unix systems and microcomputer operating system-based machines. The PC/NOS command language is used to present alternatives to the user in a consistent manner.

In following this philosophy, there are two basic rules. For one, the PC/NOS command language must exist logically "above" the host command language. For another, host transparency is maximized while the system is in the host command or application mode.

There are six basic services to be provided in the Unix environment under the PC/NOS umbrella. The first is the virtual terminal. One of the main reasons for linking a Unix system and a CP/M- or MS-DOS-based microcomputer is to use the microcomputer as a Unix terminal. The second service implements the microcomputer operating system volumes as Unix files to give the microcomputer user access to Unix system hardware resources such as large hard disks. Interconnection on a file-by-file basis, the third service, allows the transparent mapping of a MS-DOS or CP/M file (or device) and vice versa. It also provides an easy-to-use file transfer capability between the different file systems. The fourth service allows for shared microcomputer operating system volumes to be implemented as Unix files. This design implements standard PC/NOS Back-end modules as Unix processes. The fifth service allows direct access to the Unix file system from microcomputer processes. Sixth, as might be expected, direct access to microcomputer file organization from Unix processes is available.

The implementation of these goals may involve the integration of other vendor's software as PC/NOS modules. The key to the approach is implementing the operating system-independent PC/NOS command language on all the host operating systems, including Unix.

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correct number and person C answers it. Unfortunately, A speaks only English and C speaks a different language. Even though the underlying phone system has set up the proper connection, A is still unable to communicate. Person A can solve this problem by using an interpreter.

Similar communication problems occur in the computer world. For example, consider printer A and printer B, each of which can underline and print in bold type when sent a command code sequence. A word processing system must be customized to handle command codes so that it properly controls the accompanying printer. When the command code sequence for printer A is different from that for printer B, it follows that if the word processing system is customized for printer A, it will not work correctly for printer B.

PC/NOS allows the insertion of translator programs in its connection command list to adjust for such incompatibility problems. Assume that all of the software running on computer A has been customized for printer A (Fig 1). A programmer has written a printer A to printer B translator program, called P_A_TO_B. This program looks at a data stream destined for printer A, finds the command codes, and replaces them with analogous printer B command codes before sending them on. In this case the connection command would be stated as CONNECT LISTDEV = P_A_TO_B = COMPUTER_B/PRINTER.

The software package uses customized translator programs to handle other common system snags and incompatibilities, such as cursor controls for smart terminals, terminals with different character widths, and integer and real-number representations. Another typical network problem involves running programs written for one machine on an entirely different machine. If the program is written in a high level language without any machine dependencies and does not make any operating system calls, it may be possible to easily transport it to the new machine.

In most cases, however, a programmer must customize or even completely rewrite the programs. PC/NOS does not provide complete solutions to all of these incompatibility problems. Through the use of its customized translator programs, though, programmers have a structured way of dealing with most of them.

Consolidate the network

The first release of PC/NOS, which is written primarily in the C programming language, has four modules (Fig 2). These modules have two basic functions. First, they supply each host computer or network workstation with a common, host-independent, ISO session layer. Second, they allow customization that creates network file and printer servers.

The four Version 1.0 PC/NOS modules comprise the Exploration, Connection, and Security Command language, Front End, Single-user Back End, and Multi-user Back End. The Exploration, Connection, and Security Command language is supported by standardized directories and connection tables maintained at each network node. This easy-to-use language exists "above" the operating system command language in the same way that the operating system command language exists "above" an application command language. An example can make this clear.

When CP/M or MS-DOS is run in the command mode, a prompt appears. A command can be entered to run an application that responds with its

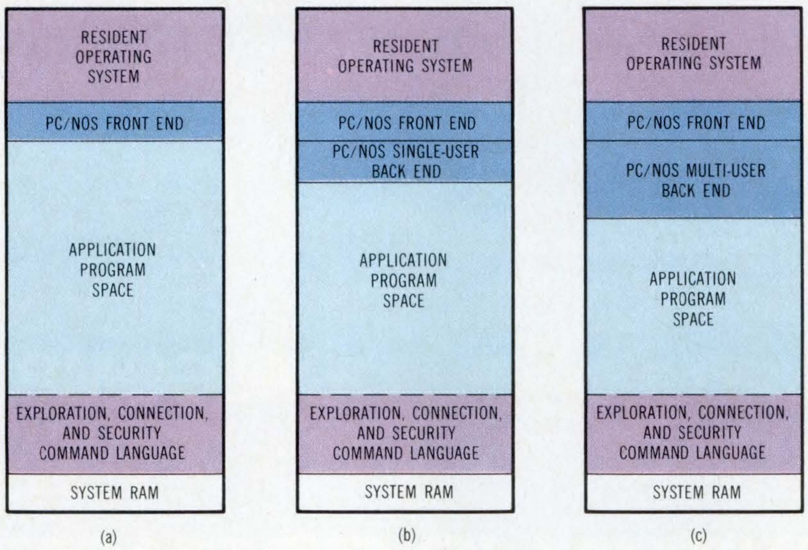

Fig 2 There are various PC/NOS configurations. The minimal configuration (a) uses the least amount of application program space (less than 4 Kbytes). The addition of the Single-user Back End (b) allows other nodes to access this node's resources. The Multi-user Back End configuration (c) allows file serving, print spooling, and electronic mail services. The Exploration, Connection, and Security Command Language exists as a file on disk, and is only resident while it is being used.

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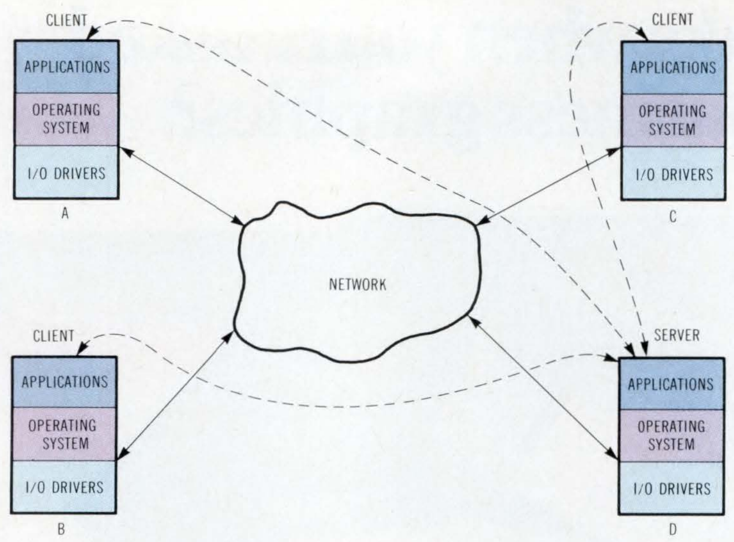

Fig 3 In a typical network there are three clients using one server. Clients cannot communicate directly with other clients, nor can they directly share their resources. Typically, network patches are "inserted" at the junction of the operating system and the I/O drivers. This means that whatever data is coming over the net at this level will be strongly flavored by the resident operating system.

own prompt. A user can return to the host operating system command mode by entering a CTRL-C in application mode. Similarly, entering a CTRLN in CP/M or MS-DOS command mode puts the console into PC/NOS command mode. In menu-driven systems, PC/NOS command mode can be considered as another menu "above" the level of the basic system menu.

The Exploration mode is analogous to an operating system's directory command; it allows users to explore the network to which they are connected. The Exploration mode provides information about computing entities in the network and at which node/socket they are located, as well as about how the entities are interconnected in the distributed environment.

The Connection mode is analogous to the command execution function of a typical operating system; it forges connections between peripherals, servers, data, applications, and workstations in the computing network. A user-level request can result in an indefinite chain of connection requests at a low level. This is one of the most powerful features of PC/NOS. A user might request, for example, connection to a specific file server. Once that connection is established, the user might then request connection of a specific local logical unit to a specific server logical number or directory. More generally, a user can request connection to any entity defined on the net.

The Security feature ensures network security by controlling access to network entities. In a typical distributed processing system, each user is assured security through a centralized password file. But, since decentralization is integral to the PC/NOS design, validation of network users is carried out by the PC/NOS processor resident at a particular network node. That is, passwords are verified against a user file stored locally at the workstation. In addition, each network node has a node administrator responsible for establishing access privileges for lower level node users.

The PC/NOS Front End consists of the software that exists at each workstation in the network. This software, in effect, changes the workstation into a network "client," and allows the user to talk to servers. A typical workstation contains connection and security language and a front end.

For its chores, the Single-user Back End of PC/NOS is the software element that allows several users to access one user's computer resources. To minimize memory space requirements, this back end does not contain general server modules. Thus, only one user can use resources such as printers or individual files at a given time.

The Multi-user Back End allows several users to access resources on a workstation simultaneously. This Back End includes such elements as a file server, print spooler, or centralized mail service, and includes both record and file locking (Fig 3). Multiple reads are allowed, but only one write can occur at a time. The Multi-user Back End includes the Single-user Front End, so that it can be used as a workstation with reduced memory space. The Multi-user Back End can also be configured to run server packages in an "under the desk" box without a console.

Common thread

Operating systems can be regarded, in essence, as combinations of processors and address space managers. A CP/M or MS-DOS directory, for example, can be considered as an address space. Each file can also be considered as an address space with an address space manager that translates from a virtual address to a physical disk address.

Although different operating systems have different schemes for address translation, ranging from

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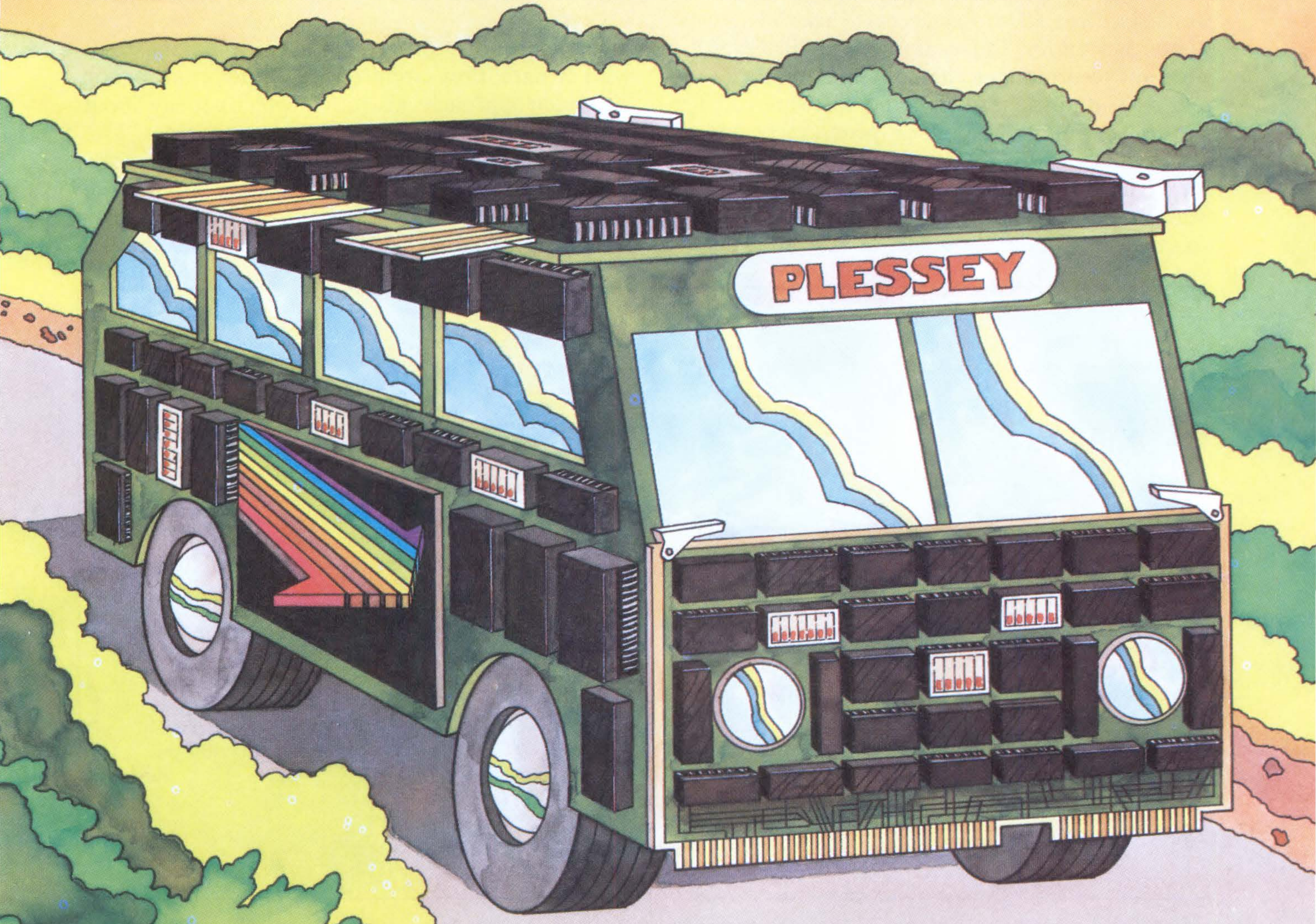

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logical or virtual to physical and different allocation schemes, they can all be described in PC/NOS terms (Fig 4). In CP/M or MS-DOS terms, a logical unit or "directory address space" is an entry in the PC/NOS socket table. This entry can be connected by the software package's transport routines to a local floppy or it may be connected via the network, transparent to the user, to a remote floppy or shared Back-end directory.

A user-level request can result in an indefinite chain of connection requests at a low level.

Other node resources, such as consoles, CRTs, and printers are also brought out to the PC/NOS socket table. When running locally for example, the console of a CP/M- or MS-DOS based workstation is connected locally via the socket table to the CP/M operating system CONIN or command processor, and the CRT is similarly connected to the CP/M CONOUT function.

The internal PC/NOS connection is transparent to the user. Its connection language, however, allows the keyboard to be connected to some other entity on the network, even a different operating system. Similarly, the CRT can be accessed via the network by another entity. For example, a mail server can interrupt to announce the arrival of mail.

PC/NOS defines hardware and software configurations as a combination of processors, address spaces, data sources, and data sinks. Processors are defined in the most general sense and can be either hardware or software. A micro's RAM is an example of an address space, as is a hard disk.

Traffic on the network is classed as either transactions destined for processors or data transfer requests between data storage elements. These data transfer requests can be generated by processors or can result from keeping copies or "equivalences" of the same data at more than one location on the network. This concept encompasses caching, blocking, virtual addressing, and conventional channel-oriented I/O.

There are other benefits to defining all host systems in common terms. By reducing an operating system to common primitives, modules can be easily defined for common access to files from different operating systems. It is also easy to create network servers to service different operating systems, an immediate aim of a distributed computing system.

Parallel and asynchronous communication

The computing entities and data transfer primitives defined by PC/NOS have some other important properties. Parallelism is emphasized in the defined message-passing protocols (Fig 5). For example, a large data transfer, such as a bootstrap load of 64 Kbytes of memory from a remote disk, can proceed in parallel as 64 independent 1-Kbyte packets that can arrive in any order. PC/NOS transport layer routines can handle any number of outstanding packets.

Asynchronous processing is also emphasized, with a data flow architecture rather than a von Neumann approach. There is much talk today about so-called "Non von," or data flow machines. This talk usually conjures up the image of a huge number-crunching machine. In fact, today's commercial transaction networks, such as those used for making airline reservations, also have many of the qualities

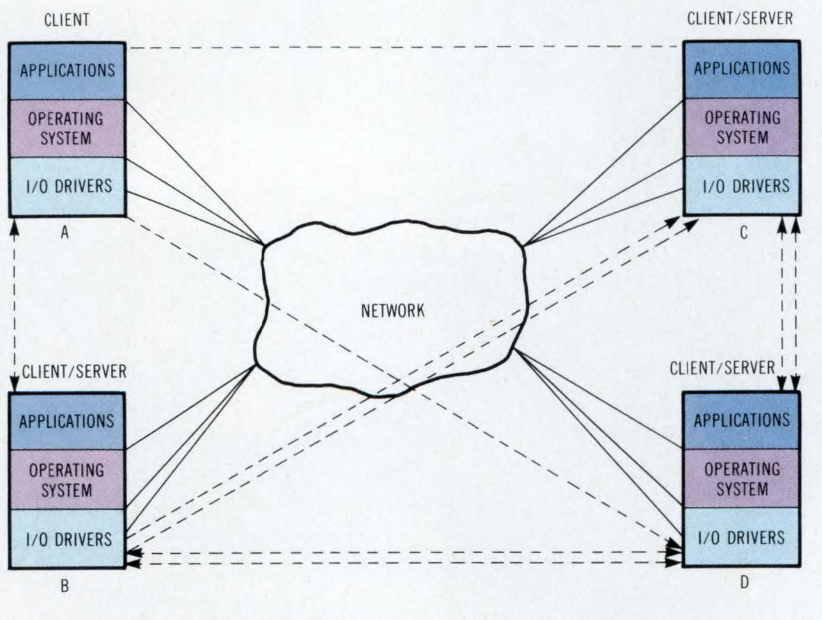

Fig 4 When the software package is patched into existing operating systems, not only does it tap in at the junction of the operating system and the I/O drivers, it also connects between the application program and the operating system. In addition, the individual I/O drivers are brought out to the network. Through the use of Single-user Back Ends, clients are directly connected and can share each other's resources. Note that in system A, the client is not also a server. This client has access to other client/server resources, but no one can access its resources.

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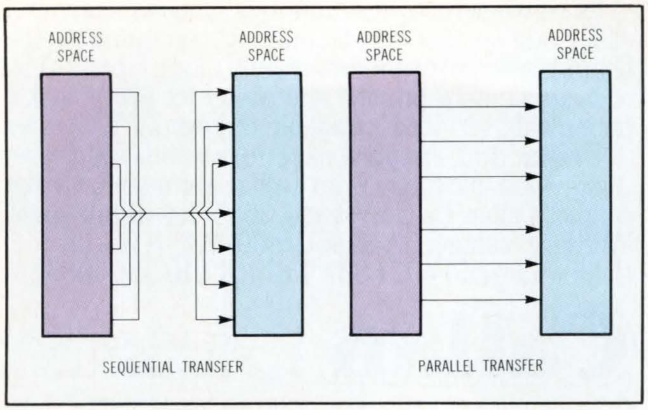

Fig 5 There are differences between serial and parallel data transfer. In the serial case, all data must go through a common "knot" hole. Usually it must be sent and arrive in order. In the parallel case, data may be sent in any order and does not necessarily have to go through one knot hole. This approach tends to be faster and less restrictive than the serial case. In practice, the parallel transfer may go through a serial channel in the lower levels of the transfer; however, there is nothing in PC/NOS that prevents complete parallelism.

of data flow machines. In many ways, the von Neumann approach is inadequate when it comes to distributed computing. Sequential computing concepts simply do not work effectively in a network environment.

PC/NOS Back-end modules are optimized for a network environment rather than for conventional time-shared I/O. For example, if physical disk block sizes are greater than a logical record size, typical time-shared multi-user systems do a "read before write." This is a very inefficient approach for a communication channel or network.

In contrast, PC/NOS Back-end modules support the notion of "logical write through," with variable data transfer sizes. Data transfers are handled in a general way by an "address space manager." This manager is actually a combination of cache manager and blocking and deblocking features, optimized for fast machines connected together by relatively slow serial channels. Address space managers can be chained together in a "distributed caching" scheme.

The Back End is organized around the data flow concept so that network transactions can generate further chained transactions as data flows around the net. The Back End is designed around a target operating system file organization. Thus, the Back-end software can coexist with the host operating system as well as function as a standalone server. This is not a conventional "scheduler" design in which users are "executing" or are in some kind of "I/O wait" queue. Scheduling is handled in a manner more appropriate to a distributed message-passing system. For example, packets can be held in queues and released by other packets.

In connecting the Back-end modules to a work station, PC/NOS takes a multilevel approach. Each workstation runs a copy of the particular host operating system so that address translation from logical to physical is not centralized. File access is handled at a control level. Once access is granted by the control level, actual I/O occurs at the disk-server level, allowing efficient blocking on the net and the use of caching techniques. In addition, host operating system compatibility is assured because the workstation is still running the host operating system.

Allocation is handled in a distributed fashion, with a locking protocol. The standardization of the control I/O and allocation levels permits different operating systems to share Back-end space.

Other features of the PC/NOS Exploration, Connection, and Security language may be illustrated by specific examples of their use. Consider the running of a remote program, one of the more useful tasks PC/NOS allows on a network. With this feature, a remote computer can be set up to print a list of files while a word processor is run locally to generate a report. Or, assume that computer designers have an 8-bit computer and wish to run a 16-bit application. Using the PC/NOS connection language, they can connect their CRT and keyboard to the remote 16-bit computer. Suppose an idle 16-bit machine called M16 has a spreadsheet program called SS16 that the designers want to use to perform some calculations for a project report prediction. Setting up the connection is as simple as selecting the "make connection" option on the PC/NOS main menu and typing M16/SS16.

When examining a connection list, PC/NOS looks first at the left-most entity to see if it is one that expects to receive input; if so, it automatically adds the local KEYBOARD command to the beginning of the connection list. Likewise, it examines the right-most entity to see if it expects to produce output; if so, the local CRT is added to the connection. This connection list looks like this to PC/NOS: KEYBOARD=M16/SS16=CRT.

Filling in the connection gaps

The example just described is one case in which PC/NOS adds a keyboard and a CRT to a connection list. In addition, it attempts to fill in gaps in the middle of a connection list by searching all of its directories for the missing pieces. For example, suppose that a designer wishes to run a database program called DB to check the inventory for a report. DB needs to talk to a database server called DBS. When the designer sets up the connection, it is only necessary to specify the DB as DB. After the searching is done, PC/NOS, by default, makes the following internal connection to a DBS on the SERV_1 node: KEYBOARD=DB=SERV_1/DBS=CRT.

Default connections can easily be overridden by more fully defining the connection. Assume, for example, that the designer really wants to use the DBS on SERV_2 and that the input is to come from a file call INF in batch mode. Further assume that the output is to be written to a file called OUTF instead of the CRT. In this case, the following connection command list is typed: INF = DB = SERV2/DBS = OUTF.

Standard modules interface with the common microcomputer operating systems and create servers optimized for a network environment.

PC/NOS is not just another operating system. In fact, it is not an operating system and does not "compete" with CP/M, MS-DOS or Unix. Its job is to provide a structure on which to build an integrated, distributed computer environment with diverse hardware and software configurations at network nodes. To do this job, PC/NOS shields the user from having to cope with overall system diversity. Standard modules are provided to interface with the common microcomputer operating systems and to create servers optimized for a network environment.

Most important, the Back-end modules go far in satisfying the requirements for multi-user applications within a distributed computing environment, without using conventional multi-user, time-shared systems such as MP/M or Unix. The PC/NOS structure is tied together with a common network command language and a distributed directory of network entities. The network structure also allows the creation of custom servers, such as database servers, for specific applications that can coexist on hosts with standard PC/NOS server modules. Apart from the standard transactions to support the common language, PC/NOS imposes no restrictions on network modules and transaction formats. All this is accomplished with an emphasis on asynchronous communication. Decentralized processing is the key to a network environment.

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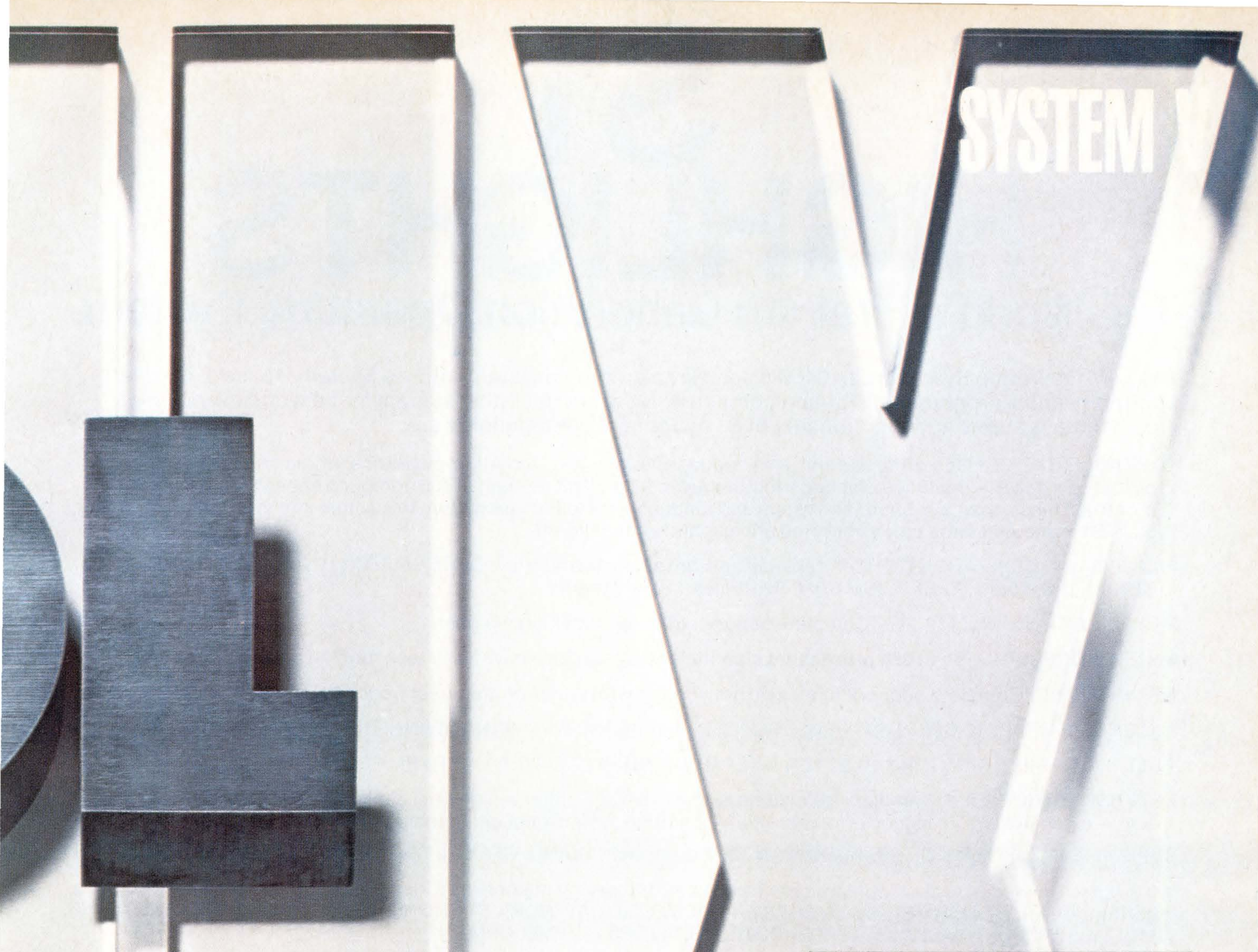

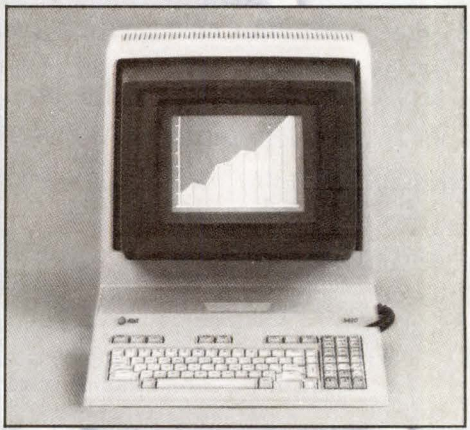

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CIRCLE 97

EVOLUTION OF FUTURE MICROCOMPUTER OPERATING SYSTEMS

Removing the restrictions on what microcomputer operating systems can do sets up a new world of applications. Here is a peek at what this world will look like in the next year.

by Vincent Alia and Gary Gysin

An operating system is a combination of software functions that gives programmers the basic tools to design and implement their particular application program. It gives users the control program they need to manage hardware. It also gives microcomputer users the ability to read and write data to disks, print letters, make graphs with plotters, and in general, handle the communication between application program and hardware.

Not only should an operating system handle and coordinate this communication, but it should do so in a standard way. Having a standard interface makes computers easier to use, both from a programmer's and an end-user's viewpoint, because it

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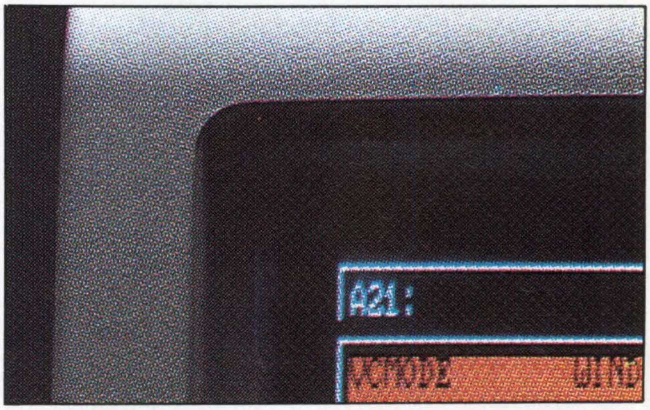
Gary Gysin is product line manager at Digital Research, Inc, where he is responsible for next-generation operating systems. He holds a BA in economics from the University of California at Santa Cruz.



allows people to concentrate on the task at hand rather than having to worry about the details of how to run the hardware. In addition to handling hardware, an operating system must be able to schedule the running of programs, to load them into memory, to provide a logical file structure for storing data on different media, and to provide an easy-to-use interface to the hardware and operating system functions.

In the next generation of microcomputer operating systems, the necessary functions will be numerous and varied. The main requirements, which will come up over and over again, are device independence, software portability, and the need for operating system primitives to support advanced application programming needs. Moreover, the next generation of operating systems must increase productivity. Portable software will aid software vendors. End-user productivity will increase by means of a user interface that allows people to concentrate on the task rather than on running the computer. Finally, easy hardware installation will enhance hardware manufacturer productivity.

The marketplace is also demanding an operating system that supports graphics, database management, communications, local networks, and advanced user interfaces. The days of the CP/M and PC-DOS kernels, which do not support these extensions to the operating system, are limited. These kernels have become inadequate for the incipient 16- and 32-bit marketplace.

The first step in the development of a standard microcomputer operating system, although limited in scope, was making programs run on different machines and also carrying data between these different machines (see Panel, "Benefits from CP/M"). This first step was somewhat limited by available hardware. With only 64 Kbytes of memory, the operating system could not be very large and therefore could not contain sophisticated functions while still leaving room for application programs.

The 16-bit microprocessor gave programmers the horsepower needed to run more complicated programs, both at the operating system and the application level. Today's 16-bit operating system of choice is PC-DOS. In fact, due to its endorsement by IBM, PC-DOS has become the CP/M of the 16-bit world.

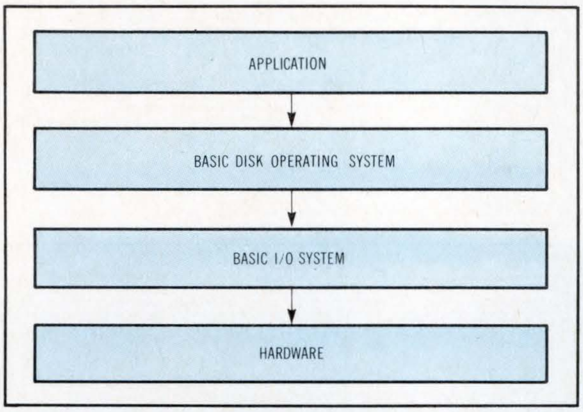
The earliest versions of PC-DOS were not much more than a translation of the CP/M ideas; the system looked much like CP/M and it even programmed like CP/M. Improvements were made in the file handling capabilities and some of the utilities, but no new, significant features were added to the first versions of PC-DOS.

With the 8088-based microcomputers on the market, programmers had a 16-bit machine to work with, but, in essence an 8-bit operating system (PC-DOS). It soon became evident that programmers were going around this operating system in order to take full advantage of a particular hardware environment. Applications were soon talking directly to hardware to get better performance and more functional ability.

Unfortunately, this design eliminated the portability that the operating system was supposed to provide. With it, each application had its own version of a user interface, graphics capabilities were limited and not very useful, and programs were tied to a specific machine. In short, sophisticated applications were developed only by application programmers who took on the tasks that were not embedded in the early 16-bit operating systems.

Benefits from CP/M

As the first operating system available, CP/M became the accepted standard for 8-bit microcomputers over a period of several years. CP/M's success was due primarily to a standard architecture that allowed application portability across any machine that ran CP/M. In fact, CP/M's major benefit was portability. With it, users could run the same program on several different machines, and data diskettes could be moved from one machine to another. However, the portability benefit had a drawback.



In order for all CP/M applications to work on many different machines, the programs had to be written to a lowest common denominator. In other words, a generic program had to be written. The result was plain-vanilla software that would work on many different machines, but unable to take full advantage of special hardware features for a particular machine. CP/M also needed improvement in several areas such as user interface, advanced services for programmers, improved usage of machine-specific functions, and better facilities for intermachine communications.

The most important thing to remember about CP/M is the principle of machine independence. This independence is due to its logical separation of machine-dependent functions (mainly hardware drivers for peripherals), from the logically independent functions of the operating system (see Figure).

The machine-dependent portion of CP/M is called the Basic I/O System (BIOS) and the logically invariant portion is called the Basic Disk Operating System (BDOS). Hardware manufacturers have only to write the BIOS, or hardware drivers, in order to bring up the operating system. This means that application programmers do not have to worry about specific hardware. They can simply write to a standard interface, the BDOS, that does not change from machine to machine.

Making progress with microcomputers

As might be expected, operating system design does not stand still; continuous advances are taking place for both 16- and 32-bit microcomputers. These advances include operating systems with more sophisticated services for programmers, additions allowing the generic use of windows, and file handling with tree-structured directories.

There is more. New microcomputer operating systems are being introduced and developed for the next generation of hardware and microprocessors. These new systems attempt to give application programmers all the necessary tools for developing programs for users who have advanced beyond the initial 8-bit marketplace. In its attempt to define and implement operating system software that will benefit application programmers, Digital Research has developed its Concurrent CP/M and Concurrent DOS operating systems.

With the introduction of advanced architecture microprocessors like the Intel (Hillsboro, Ore) 80286 and the Motorola (Phoenix, Ariz) 68000, operating systems must become more advanced to make efficient use of the architecture's features. Yet, at the same time, they must be easier to use since a wide variety of people will work with them. For example, the company's operating systems are used in Fortune 1000 companies and various commercial installations where multi-user and networking workstations are common.

Customers of this gear include data processing managers, general managers, office productivity workers, and administrative assistants. The next wave of operating systems will be integrated into the office environment and will be used by people who know nothing about computers and, often, do not care to know. The operating system transparency to these workers is the key issue.

The success of an operating system will depend on fulfilling the needs of end users, software vendors, and machine manufacturers. The end users will need an environment that allows them to run the existing application base and also to take advantage of more powerful environments and any associated applications. The new operating system will have to be much easier to use than previous operating systems, will have to provide concurrent and multi-user capabilities, and will have to allow end users to organize and manage information needs better.

Maintaining portability in operating systems

For their part, software vendors are looking for an operating system that enables them to write programs that can be executed on various machines and microprocessors without modification. At the same time, they want to take advantage of machine-specific features. As if this is not enough, these software vendors are looking for more help from the operating system in file handling and database management. Indeed, the operating system that allows only reading of fixed-size records is no longer acceptable; now there must be some type of support allowing software vendors to use different access methods.

Software vendors are also anticipating that services with the new desktop style of user interface will be built into the operating system. Thus, facilities for support of such features as icons, menus, mice, and windows need to be operating system extensions and must be accessible by software vendors. These user interface services must be portable so that software vendors do not have to rewrite an application for each machine or new set of hardware.

Hardware manufacturers must be able to install a new operating system as quickly and easily as possible. At the same time, the operating system must be expandable and easily configured for different hardware environments. The use of loadable device drivers for different hardware pieces will enable hardware manufacturers to bring the system up quickly. This will let manufacturers add new peripherals and machines easily and with much less development effort. The operating system that requires building drivers into the system is no longer acceptable to hardware manufacturers and will soon become an obsolete method for attaching devices to an operating system.

A look inside the kernel

The operating system model chosen by Digital Research is shown in Fig 1. This model expands the services that have been provided by microcomputer operating systems for today's marketplace. These extensions include support for graphics, database management, local networks, communications, and an application environment. Low level operating system primitives must be built into the system kernel so that the additional extensions can be easily included in the total package.

The operating system kernel provides the basic services for the surrounding software layers. These services include, but are not limited to, concurrency (the

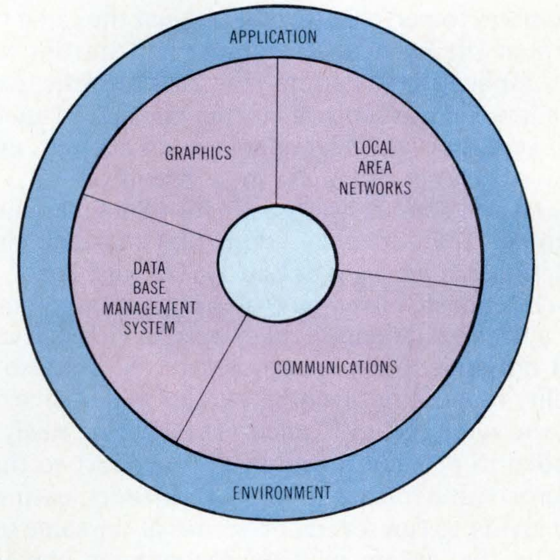


Fig 1 Digital Research's model of an operating system provides the services for state-of-the-art 16- and 32-bit microcomputer systems. It includes support for graphics, local networks, communications, and database management systems—all within an application environment.

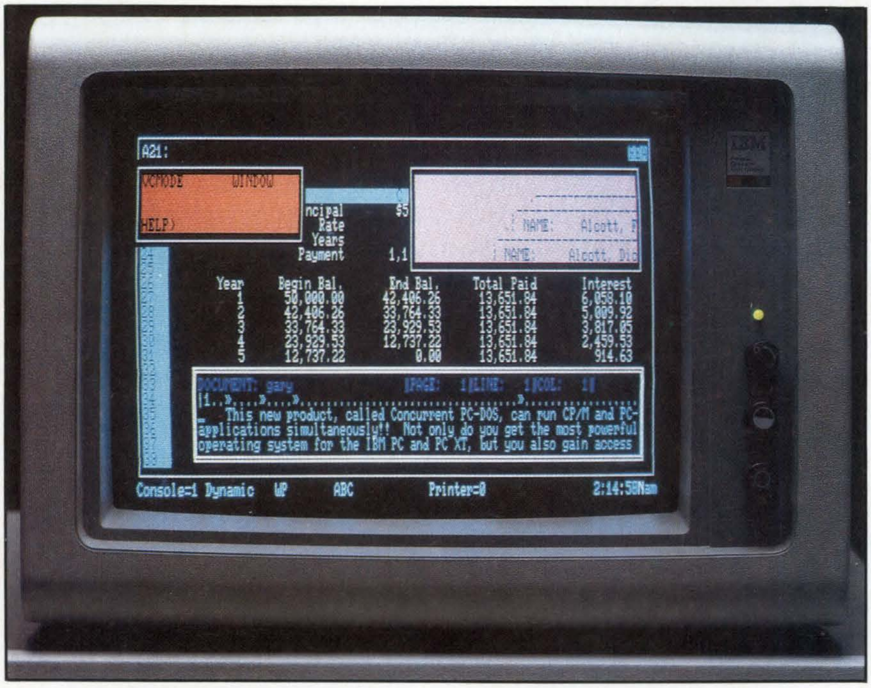


Fig 2 Microcomputer system users (eg, a design engineer preparing a project progress report) can use windows to see parts lists, spreadsheets, calculations, and other items simultaneously. Such windowing is an invaluable aid when writing reports on word processing programs.

ability to run multiple applications at the same time through a windowing system), a robust file system that can be shared and protected, support for real-time data acquisition, communications, and process control. There is also the need for device or peripheral independence by use of virtual device interfaces, and support for advanced user interfaces.

Concurrency is a must in the professional workplace. Today's microcomputer systems must allow end users to perform several tasks at the same time without the burden of stopping and starting various application programs (Fig 2). The basic idea is to allow end users to switch from one task to another in a very simple and straightforward manner, much like switching channels on a television set. The operating system supports this channel change through a windowing system that makes a single workstation act as if it had several displays.

The console or screen switching can be enhanced by a window management system, giving end users not only the ability to switch screens, but also the ability to monitor several programs at the same time on the same screen. Concurrency can be easily extended to provide for multi-user support so that a microcomputer can support several users, each with the ability to run several programs at the same time.

The file system in a microcomputer operating system must not only allow for the sharing and protection of files in a multitasking environment; it must also take into consideration the workplace and the naive user. File sharing is essential in an environment that allows multiple single-user programs to run at the same time. In this situation, an end user has to run applications that were designed for earlier microcomputer environments; these assumed they owned the entire machine. File protection here becomes critical to running existing programs. Of particular importance are file sharing capabilities for simultaneous access of multi-user environments as well as update functions for database applications.

Preventing potential system failures

In designing a file system, the current workplace where microcomputers are found must be taken into account. Often this workplace includes such potentials for disaster as power strips near users' feet, reset buttons that can be leaned on, and floppy disks that can be removed during program execution. By allowing the recognition of such open-door interrupts from the hardware, the operating system can make sure that removable media are protected from accidental changes during the running of a program.

The effects of catastrophic failures, such as turning off the power, can be somewhat lessened by having the file system update the directory and media on a periodic basis. This procedure helps users who reset a machine while in the middle of an application program, not to lose all the work entered in a particular session. In addition, application programmers must be able to force information out to the media in those cases where a loss of data is unacceptable—for example, a database application.

An operating system that supports various types of logical media, or media from another operating system, can provide a major benefit to its users. The company's Concurrent DOS 3.1, for example, has the ability to support both CP/M and PC-DOS

media at the same time (Fig 3). This feature gives users a greater choice in the types of applications that can be run. Most likely, the next generation of operating systems will support various disk media by allowing users to choose a file system.

Key kernel feature

A realtime kernel is crucial for the support of realtime control applications, interprocess communications (a process is a program and the associated system overhead), synchronization, and support of both local networks and communications. The basic attribute of a realtime operating system is its ability to respond to external interrupts in as fast a manner as possible. This response is measured in terms of both interrupt latency and context switching time; it must be short enough to ensure that data will not be lost and that the synchronization or communication request is speedily serviced.

In addition to its performance characteristics, a realtime system should aid the programmer in controlling the hardware, and the program's response to the hardware. This feat can be accomplished by allowing the programmer to control I/O devices, set dispatching priorities, and control exception processing. By allowing data to be passed back and forth between processes, a realtime application can be developed so that one high priority process monitors the hardware and passes off any data to a lower priority process that manipulates the data.

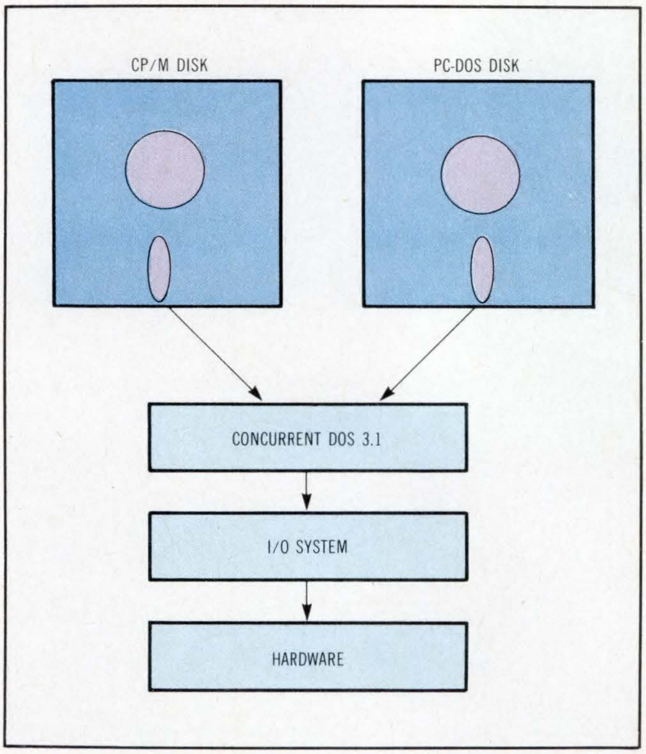


Fig 3 While the Concurrent DOS 3.1 operating system is advanced enough to allow either CP/M- or DOS-based magnetic media, future operating systems will go a step further and support multiple media by permitting system operators to choose a file system at will.

There are still other attributes that a modern operating system must have. To help application programmers get the most benefits from their programs, an operating system should allow the application to talk to the hardware in a generic manner. This is equivalent to device independence and allows the programmer to concentrate on the program logic and not worry about the particular piece of hardware that an end user might have.

Device-independence should carry over to such areas as support for foreign languages and character sets. Whether the end user is in Japan, using a Kanji keyboard, or in California, using an English character set, it should not have an effect on the application logic. Using a concept of a standard terminal, the application program can be sheltered from the actual hardware. This standard terminal allows the program to make calls to the operating system, which do not change with different character sets, and moves the support for the translation of the differing character sets to the device driver level. It also allows new hardware to be added to a system without change to the application program. With this design, a new terminal can be added, and the changes necessary for all programs can be localized in the hardware driver. All applications can then take advantage of this hardware without changing each program to support the new device.

Adding graphics to the picture

The support of a standard graphics interface is becoming increasingly significant as microcomputers become more powerful, and as peripherals become more sophisticated. Graphics capabilities are fast becoming requirements for business management tools. It turns out that a standard operating system interface to graphics functions is becoming a marketplace requirement. Moreover, the graphics interface should also provide a standard programmer interface as well as a standard device interface (Fig 4).

For its part, the programmer interface takes care of the conceptual model and syntax that is used when incorporating graphics functions into an application program. The device interface relates to the protocol used for communication between the device-dependent and device-independent functions of a graphics extension.

The programmer interface should follow an established standard to port graphics programs from machine to machine. The primitives for this interface should provide for control of multiple output devices at the same time, the use of both normalized device coordinates as well as raster coordinates, the ability to fill areas with either solid patterns or patterns defined by cell structures, the use of drawing primitives for lines and curves, and the ability to position and rotate text (see "VDI Promises Graphics Software Portability," *Computer Design*, May 1984, p 197). A comprehensive set of input primitives is

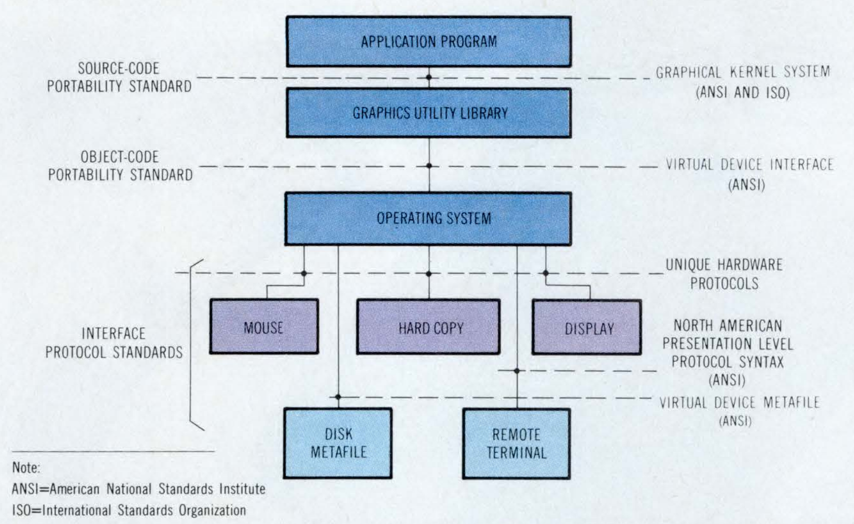


Fig 4 There are many different graphics interface standards coming on the market, including the Concurrent DOS 3.1 operating system software. Most of the standards are designed to ensure portability of one kind or another.

needed to manipulate pointing devices. It includes such primitives as getting the position of a structure in the applicable coordinate space, getting the current value of a valuator device such as a joystick, getting keyboard input, and representing choices that have been made by the user, either as an absolute choice, or as a pointer to a graphics symbol.

The device interface can also be based on established standards and should provide a portable I/O protocol for all graphics devices. As more graphics functions are being implemented in hardware, a standard device interface will prove to be extremely beneficial. The same application program will be able to talk to several kinds of devices without a change in program logic or code. This approach has already been taken with disk systems in the Shugart Associates Standard Interface (SASI) protocol for disk drive subsystems. As is the case with any attempt a standardization, the long-term benefits of such a policy will be welcomed by both hardware manufacturers, software vendors, and end users.

One more standard for graphics primitives, a standard method of talking to a nonstandard or specific device, should be discussed. In many cases, the use of standard device interfaces results in a performance degradation that may not be acceptable for applications such as advanced user interfaces. In such cases, the application program must be able to address the hardware more directly, and make calls that do not apply to other standard devices. The Bitblt (bit-block transfer) method of device-dependent communication has gained wide usage and would be appropriate for such device-dependent support.

Support of the data base

Database facilities will be used more and more as the application program complexity increases, and as the expectations in the microcomputer marketplace rise. The main job of database primitives is to provide software vendors with the ability to examine and manipulate data from different viewpoints by specifying different data relationships. The current file access methodologies (sequential and random reading of records) is inadequate for such applications. Even the indexed sequential access method (ISAM) may not be sufficient for advanced database applications. Fast and reliable access methods must be provided in order to support database functions.

The functions offered by database primitives should address database modification without reconstruction of the entire database, security through various access levels, definition of database through a data dictionary, report generation through a query system, nonredundancy of data items, and access to the database through high level languages. Database access through the operating system must allow the software vendor to create, read, and modify data relationships, as well as provide the traditional file system functions available for data records.

Typical database primitives allow the creation, retrieval, modification, and deletion of data records. In addition, the operating system primitives must allow access to the data dictionary. Then, software vendors can develop generalized programs that are independent of any specific database management system.

A query system for report generation and for those nontechnical users who wish to use the data base has to be provided as part of the database support. The system should be flexible enough to work with different data bases and data structures, yet simple enough that clerical people will not have a problem in extracting needed information. Thus, for example, the clerical staff should be able to generate reports that are assembled from data produced by the inventory application and the accounts payable application.

Without database management support, one report would list the current inventory and a separate report would list the current status of the accounts payable files. Then it would be up to end

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users to construct, for example, a list of all the suppliers who are owed more than $10,000 and a list of the stock on hand from those suppliers. The query system should allow the specification of the report that would tie together the inventory files and the accounts payable files.

A major advantage of data bases is the nonredundancy of data, or the single occurrence of a data item. This simply means that rather than having a data item appear in several different files, the database management system will coordinate the usage of one item by different files. The main advantage of this feature is the ability to easily and securely update the data base by making one change. If data items were duplicated, the update procedure would become very complex, and error possibilities would increase.

In order to make full use of a database software, vendors must be able to write programs that can access database primitives from a high level language. The combination of a data dictionary and support for database primitives will allow programs to be written for specific markets not addressed by the query system.

Making the connection

Operating system support for communication functions serves to demonstrate the use of the operating system as a total environment for the system integrator, designer, or end user. In single-tasking systems, communication programs either use the entire machine with no possibility of doing other work, or in some cases, they run as a background task with no user interaction. Now, however, with the ability to take advantage of concurrency, communication programs can now become more useful and easier to use.

The basic difference in a concurrent environment is that the communication program can monitor the communication link and report events as they occur. In case nothing happens, the program will not interfere with the other system processes. The combination of an operating system's windowing support and concurrency allows the software vendor to be very creative in communication program design. For example, end users can be notified if there is something that needs attention. Then, they can switch to the communication program and handle the transaction.

Local network issues

With the advent of low priced microcomputers, the use of networked multi-user systems became more economically feasible and therefore, more popular. Until now, the primary concern of networking has been hardware. In contrast, networking software has not been properly addressed.

There are several issues that networking software must consider. Two of the most important are compatibility with existing single-user programs and the basic question of where in the computer software system networking support should reside. The company approach is to build the networking support into the operating system. This allows existing single-user programs to be supported in a multitasking environment by having the operating system make the decisions that involve contention of resources and file sharing and/or protection.

Networking support in the operating system consists of multitasking, file sharing, loadable device drivers, and identification of remote resources. Multitasking and file sharing are necessary to arbitrate the contention that results when various nodes try to access the same device or file. This level of protection should reside in the operating system in order to provide the necessary support to run existing single-user applications and to provide the standardization that is needed at all levels of system software. Loadable device drivers are important to the networking architecture because they allow application programs to be independent of the physical network.

The identification of a remote resource allows the operating system to deal with networking requests in a clean fashion (Fig 5). Rather than looking at all operating system calls and trying to determine if a local resource or remote resource is required, the use of a network specifier in the device name allows the operating system to streamline determining the resource location. This network identification is achieved either through logical mapping of remote resources or through a network ID in the device naming convention. Once a particular operation is identified as a networking request, the operating

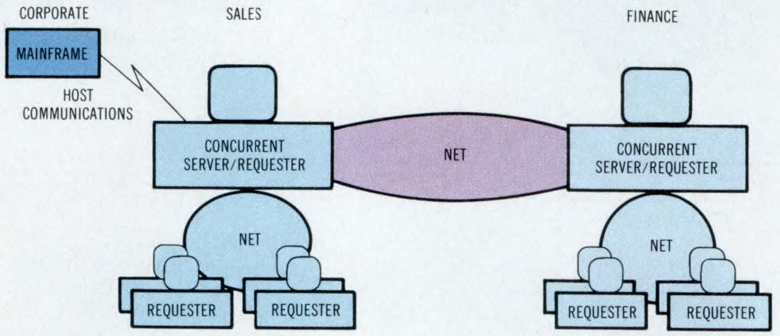

Fig 5 Remote resource identification by the operating system allows it to deal efficiently with networking requests. ID is accomplished by the use of a network specifier in the device name; either a logical mapping or network-ID will do the job for the operating system's service routine.

system can easily route the request to the appropriate service routine.

Networking support for the software vendor includes sharing of remote files and resources, file and record locking, password protection, assigning private drives, support for requester access to multiple servers, compatibility across CPU types, and compatibility across different operating systems. The combination of these services will result in the transparency of the network to the application program and to end users.

The desktop style of microcomputer interface is becoming an increasingly important area that people working with user interfaces and application programs must address. Advanced user interfaces need the same type of support as do most other applications. These include concurrency, windowing, control and synchronization of asynchronous events, interprocess communication, loadable device drivers, and device independent graphics support. With these operating system primitives in place, the application environment can provide such services as a consistent user interface at all levels of applications, data interchange between concurrent processes, window management functions, and user interface primitives.

The application environment must provide certain primitives for software vendors. For their part, these included icon manipulation, window services such as pull-down windows, an overlapping approach to windows, online help facilities, dialog and alert windows, and data interchange among nonintegrated applications.

With all these basic operating system services, application programs will tend to look alike. For this reason, software vendors need the additional capability to make their product different. Otherwise, there is no reason to pick one product over another. Having the support for the user interface in the operating system allows programmers to pick and choose the particular method of writing applications. This capability gives software vendors the flexibility needed to differentiate the product.

Fulfilling present and future needs

To meet some of the operating-system-as-environment needs, Digital Research has developed the Concurrent DOS 3.1 operating system and extensions. Parts of it are available today, and, in the near term the company will complete the fully functional operating system model that has been described.

Simply put, Concurrent DOS 3.1 is on a natural evolutionary path towards the higher level operating system environments and extensions that new marketplaces are demanding. It is a multitasking single- or multi-user operating system for Intel 8086/8088 microprocessor-based systems. It supports realtime operations, windows, communications, and an improved user interface. In addition, extensions are available that support graphics, local networks, and advanced file handling capabilities.

From the viewpoint of computer designer and end user, the most striking feature of Concurrent DOS is its ability to run several programs at the same time on one computer. These can be either CP/M or PC-DOS applications. Thus, a PC-DOS application, like Lotus 1-2-3, may be had at the same time that a CP/M application like Wordstar is run, without having to reload the programs.

Such concurrency has advantages for hardware manufacturers. For example, they can configure a system so that several terminals can be attached to a main processor. These terminals can provide support for multiple programs running simultaneously on each processor.

Supporting concurrency

The Concurrent DOS 3.1 kernel supports concurrency through its multitasking and single- or multi-user capabilities, offers realtime response for process control applications, supports file- and record-locking for the protection of all applications, and supports hardware-independent character devices. This can be done efficiently because Concurrent DOS is truly concurrent. It does not suspend operations of background tasks when primary tasks are executed.

The tasks placed in the background by means of switching consoles, still get their share of the CPU and continue to work. This true concurrency is most easily demonstrated by the Concurrent with Windows operating system software. With it, software developers, for example, can have four separate processes working in overlapping windows.

Concurrent DOS 3.1 is supported in its kernel by interprocess communications, a flag system for waiting on asynchronous events, and sharing code areas between multiple copies of the same application. For its part, interprocess communication is handled by a pipe system that allows messages to be passed back and forth between processes (programs). These reside only in memory so there is no performance degradation because of disk accesses. The pipes are handled like disk files with the ability to create, read, write, and delete named-pipes, or queues, as they are sometimes called.

For processes that need to use a synchronization mechanism, the kernel supports a semaphore called a flag. When a process needs to wait for an event, it "does" a flag-wait and another process or interrupt routine does a corresponding flag-set to signal the completion of an asynchronous event.

Finally, shared code support allows an end user to run several application copies while having one copy of the code resident in memory. This design saves memory space—a very valuable system resource. Programs that have pure code areas (code that is not modified by the program), can have one code area shared by each of the several programs. Naturally, each program will have its own separate data area.

Concurrent DOS supports existing programs that were developed for a single-user environment. In this situation, file integrity becomes a critical issue. Since multiple programs must have the ability to access the same files at the same time, a file protection scheme was devised; this allows the sharing of files in a controlled manner. Files are opened in three modes: locked, read only, and unlocked.

A file opened in locked mode cannot be accessed by another process, a file opened in read only mode cannot be written to by any other process, and a file opened in unlocked mode can share a file with another process. In those cases where file sharing is required, the application program has the option of locking a record so that an update can be safely made. The default open-mode for existing single-tasking programs is the locked mode.

To improve file handling capabilities for software vendors, the company provides Access Manager, a library that provides support for index files. Access Manager makes use of B+ tree index structures to maximize file operation efficiency. The functions in Access Manager are categorized as system initialization and maintenance, data file setup and maintenance, data file update, data file locking, index file setup and maintenance, index file update, and index file search.

With Access Manager, duplicate keys can be maintained if the application program requires them. Error handling is specified at run time, and software developers have the choice of stopping the program on an error condition, or handling the error within the program.

As mentioned, Concurrent DOS 3.1 also has communication support. Communications is supported through operating system primitives that allow an application program to talk to serial devices and through software functions that allow the setting of a process's priority.

The usual calls that allow access to a communication device are not sufficient in a multitasking system to ensure the correct functioning of communication programs. In fact, there must be a way to ensure that the CPU is available when characters are being received at a high rate. The communication application can control this problem by raising its priority when it cannot be interrupted by other processes. Raising a task's priority ensures that it will continue to run when the next dispatch occurs. Of course the program cannot run at a higher priority at all times. Clearly, this would interfere with other system processes.

An improved user interface is integral to Concurrent DOS. This is a menu-driven interface that can be tailored by the end user and hardware manufacturer. The interface consists of a menu editor that allows end users or hardware manufacturers to build a menu, a program to make menu copies, and a default menu that is shipped with the distribution disk.

The default menu can be changed to suit individual needs by using the interactive editor. The editor allows users to specify screen attributes such as blinking, highlighting, underlining, and colors. For those brave folks who prefer the traditional "A>" interface, that command line is still available.

Opting for pretty pictures

In addition to the kernel, Concurrent DOS 3.1 also supports extensions that give the user graphics functions and local network support. Graphics is supported through the Digital Research Graphic System Extension, known as GSX. GSX allows both CP/M and PC-DOS programs to execute in a device-independent manner.

The GSX is based on the American National Standards Institute (ANSI) Virtual Device Interface (VDI) and provides portability across systems and devices. It provides the application programmer with a set of graphics primitives and a library of device drivers. The graphics primitives can be accessed directly through the operating system, or from high level languages.

To provide device independence, GSX comprises two components. These are the Graphics Device Operating System (GDOS) and the device-dependent Graphics I/O System (GIOS). This architecture follows the CP/M model of both the Basic Disk Operating System (BDOS) and the Basic I/O System (BIOS).

Local networks are supported through the DR NET operating system extension. With DR NET, workstations can share expensive peripherals such as hard disks and printers, while maintaining full local processing power. This network support is designed to work with any physical network such as Ethernet, Arcnet, or Omninet.

With DR NET, both network requesters and servers are supported. Requesters act as workstations and initiate all network activity. In contrast, servers manage the networking requests including remote file handling and printer and console activities. A Concurrent DOS 3.1 workstation can be both a requester and a server simultaneously. Note that DR NET will allow PC-DOS programs to work over the network. Therefore, it is now possible to have PC-DOS programs, written for a single-user environment, work in a networked concurrent environment.

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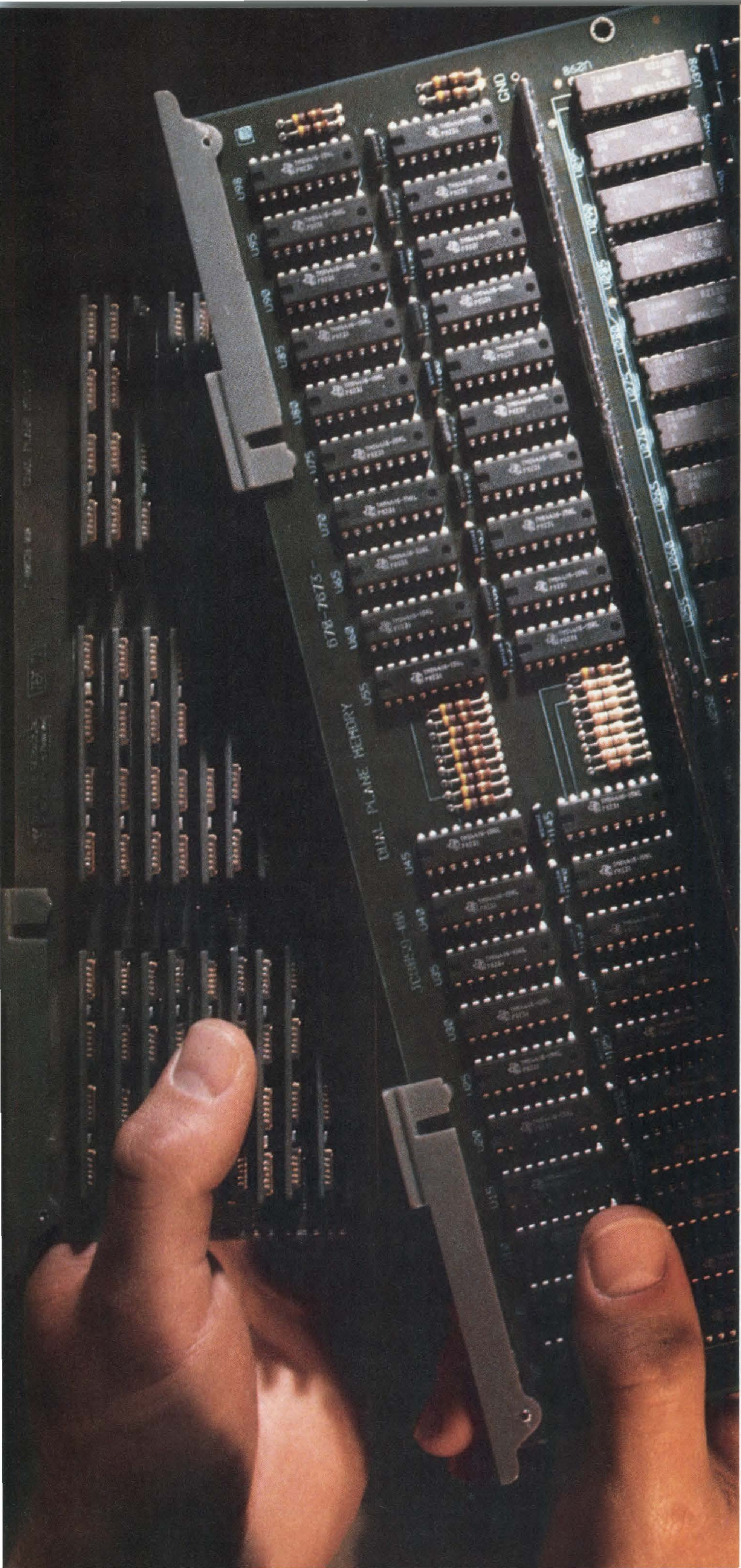

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125 MHz pixel-rate performance. With memory parts count cut by 75%. And cost savings more than 50%. The unique TMS4416 16K × 4 DRAM from Texas Instruments is the first 64K dynamic random-access memory (DRAM) in the world that could provide this performance at that price. And that's why it was chosen for the new, advanced Tektronix 4115B Computer Display Terminal.

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System-wide cost savings

By upgrading from four 16K devices per single in-line package to one TMS4416 ByFour™ DRAM (see photo), Tektronix cut costs by more than 50% and memory parts count by four times.

System costs also were lowered, due to fewer interconnects and support circuits. This reduced inventory, cut power requirements, and enhanced reliability.

Lower power, higher reliability

With one 5-V power supply at 130 mW per 64K, the TMS4416 significantly cut power consumption. This increased power supply margins and reduced noise. Plus, lower heat dissipation and fewer interconnects improved system reliability.

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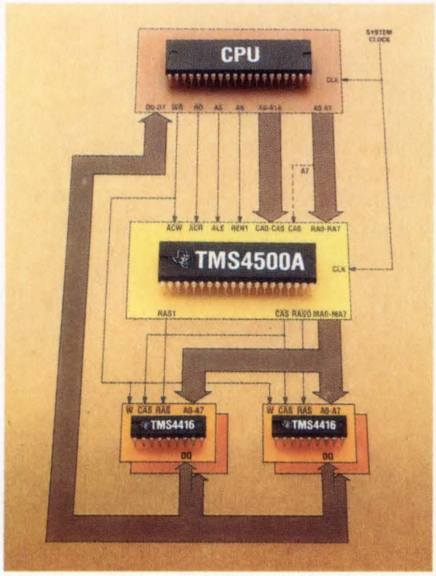
16K x 4 DRAM cuts costs by 50% for Tektronix.



For a cost-effective, low-power memory system that uses minimum board space, combine the TMS4416 or the TMS4164 64K DRAM with the TMS4500A.

One TI chip links DRAMs with CPUs.

TI's TMS4500A DRAM controller saves design time and IC costs.

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Highly versatile, the TMS4500A interfaces with all popular microprocessors. And is compatible with DRAMs from 4K up—*from any manufacturer.*

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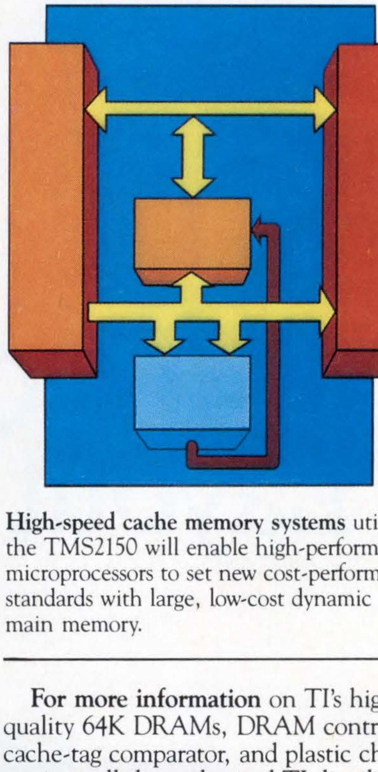

High-speed cache memory systems utilizing the TMS2150 will enable high-performance microprocessors to set new cost-performance standards with large, low-cost dynamic main memory.

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COMPONENT-BASED OPERATING SYSTEM WORKS IN REAL TIME

Realtime operating systems often have to communicate with the real world of IBM PC-based MS-DOS operating system files and Unix operating system files. Modules do the trick.

by Gary Funck

Operating systems have existed as separate, identifiable programs for approximately 25 years. They have developed either from libraries of commonly used routines for controlling I/O devices (device drivers) or special programs designed to replace computer operators who loaded cards, turned on I/O devices, and sequenced programs manually. Even now, mainframe and batch oriented operating systems do not provide much more. And operating systems, whether for mainframes, minicomputers, or microcomputers, provide at least these two services.

But three key developments, each beginning in the 1960s and intensifying dramatically from the 1970s until now, have caused changes in operating system technology. On the one hand, there is the development of practical time-sharing systems, and the development of inexpensive, single-user computers. It began with the minicomputer and continues with the personal microcomputer. Finally, there is the development of embedded computer systems in which computers control machines or processes in real time.

Gary Funck is director of engineering at Hunter & Ready, Inc, 445 Sherman Ave, Palo Alto, CA 94306, where he is responsible for IOX and FMX/DOS product development. Mr Funck holds a BS in computer science from North Carolina State University and an MS in computer science from Indiana University.

Each development has led to a new type of operating system quite different from "bare-bones" programs. Thus, the industry now enjoys time-sharing, single-user, and realtime operating systems. Today in fact, almost all mini- and microcomputers use one of these three types. In contrast, classic batch-oriented operating systems are still limited to mainframe installations.

While time-sharing and single-user operating systems are relatively well known, little has been said about realtime systems. Unfortunately, standards have been slow to emerge in this area and most systems are proprietary. However, Hunter & Ready's Versatile Realtime Executive (VRTX) software kernel is an exception. In fact, this *de facto* industry standard now fits in with existing Unix and PC-DOS file standards. The connection is made through the company's VRTX extension software known as the I/O Executive (IOX), the File Management Extension compatible with PC-DOS (FMX/DOS), and the Standard C/Unix I/O Library (STDIO).

Before examining the software components that complement VRTX, it is necessary to understand the nature of operating system software standards. What is meant by saying that Unix has emerged as the *de facto* standard time-sharing operating system, PC-DOS as the standard single-user operating system, and VRTX as the standard realtime kernel? In essence, the same program has been implemented on a number of different hardware configurations from different manufacturers.

Remember, the software interface provided by the operating system has taken on a life of its own, independent of any one manufacturer's hardware. For example, Unix has been implemented on the VAX-11 and PDP-11 computers from Digital Equipment Corp, large IBM mainframes, the IBM PC, and many microcomputers based on the Motorola 68000. For its part, PC-DOS has been implemented (in its MS-DOS version from Microsoft) on a large number of Intel 8086- and 8088-based personal computers. And, VRTX has been implemented, in 1983 alone, on more than 300 different embedded, custom microcomputer systems based on the 8086 and 68000, and Zilog's Z8000 and Z80.

This situation can be contrasted with operating systems that are proprietary to particular manufacturers, and work solely with that manufacturer's hardware. The VMS time-sharing operating system for the VAX computer, the AppleDOS single-user operating system for the Apple II, and the RMX-86 realtime executive for Intel iSBC-86 single-board computers are all examples of popular, but proprietary, operating systems.

TABLE 1

STDIO Functions

fclose, fflush	- close or flush a stream
feof, ferror, clearerr, fileno	- stream status inquiries
fopen, freopen, fdopen	- open a stream
fputc, putw	- put character or word on
fread, fwrite	a stream
fseek, ftell, rewind	- buffered binary I/O
getc, getchar, fgetc, getw	- reposition a stream
gets, fgets	- get character or word
popen, pclose	from stream
printf, fprintf, sprintf	- get a string from a stream
puts, fputs	- initiate I/O to/from a process
scanf, fscanf, sscanf	- formatted output conversion
setbuf	- put a string on a stream
ungetc	- formatted input conversion
	- assign buffering to a stream
	- push character back into
	input stream

Standard interfaces

Four interfaces define the external behavior of an operating system. In fact, with a standard operating system, these four interfaces actually define the standard. The first interface, the application interface, is defined by the operating system's set of system calls. The second interface, the user interface, is defined by a command interpreter program and by a command set from a user console that it can interpret.

The third interface, the media interface, is defined by the format of any media transported between systems for exchanging data or programs. Finally, there must be a device interface. This software is defined by a command set that the operating system issues to devices or to device specific routines to make them carry out I/O operations.

Since these four interfaces make up the standard, every standard operating system consists of four standards. But, some standard operating system interfaces are not as important or even as "standard" as others. Consider Unix, for example. The application interface is not the set of assembly language system calls. These depend on the instruction set of the host processor and differ in format for each system implementation. Instead, the real application interface is the C language version of Unix's system calls (most Unix application programs are written in C). Seen from a C program, Unix contains two principal sets of resources: process control resources such as fork and pipe, and file I/O resources such as open and read.

Note, however, that the C language definition includes a standard I/O library known as STDIO that includes a set of higher level I/O functions, such as printf, than are provided by the Unix I/O functions. As a result, most C programs use this library instead of making explicit Unix calls for I/O. Of course, if the program runs on a Unix system, the library functions are ultimately implemented by Unix calls.

There is another practical matter to consider. Most C language programs running under Unix do not make use of its process control resources; they execute as a single process. Thus, for all practical purposes, the Unix application interface boils down to the functions in STDIO (Table 1), which are not actually part of Unix at all, but part of the C language. This is only one example of the many oddities one encounters when examining "standard" operating systems.

The C language includes an I/O library known as STDIO which has higher level I/O instructions than the Unix.

Other Unix interfaces can be treated more quickly. Thus, the user interface is the well-known Unix "shell." It comes in two versions, the standard or "Bell shell," and the "Berkeley" or "C shell." Because few Unix installations include any type of floppy disk, the only Unix media interface is magnetic tape in the "tar" format. Finally, the device interface is defined by the interface between the Unix kernel and device drivers. This is a fairly high level interface since Unix drivers are responsible for their own buffering of data transfers.

Of the four Unix interfaces, the most important "standard" is the STDIO interface and shell. Magnetic tape has been replaced by floppy disks as the preferred transfer medium in most microcomputer applications. Moreover, there is no extensive market for Unix-compatible device drivers. But neither tar tape nor Unix drivers can be ignored, since both may become more significant in the future.

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In a PC-DOS operating system interface, the application interface consists of a set of 8086 assembly language system calls, a command interface called the Command Interpreter (CI) program, a 5 ¼-in. IBM standard floppy disk, and a device interface defined by the format of user-installed device drivers.

The two most important characteristics of realtime software are responsiveness and multitasking.

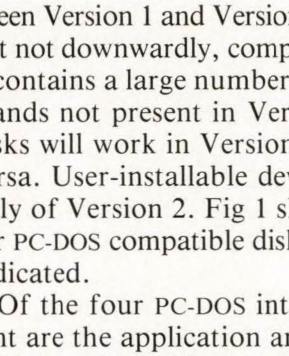
All four PC-DOS interfaces differ significantly between Version 1 and Version 2. Version 2 is upwardly, but not downwardly, compatible with Version 1; and it contains a large number of system calls and commands not present in Version 1. Version 1 floppy disks will work in Version 2 systems, but not vice-versa. User-installable device drivers are a feature only of Version 2. Fig 1 shows the media interface for PC-DOS compatible diskettes with the differences indicated.

Of the four PC-DOS interfaces, the most important are the application and the media. This is due to the many application programs available for the IBM PC. They make use of PC-DOS system calls and are distributed on PC-DOS compatible diskettes. Currently, the user interface is in a state of flux. The increasing popularity of "integrated" systems and "windowing" programs are replacing the CI. Take Microsoft's Windows for example. It is designed to replace the CI as a standard user interface. As of yet, no significant market in third-party PC-DOS compatible device drivers has emerged.

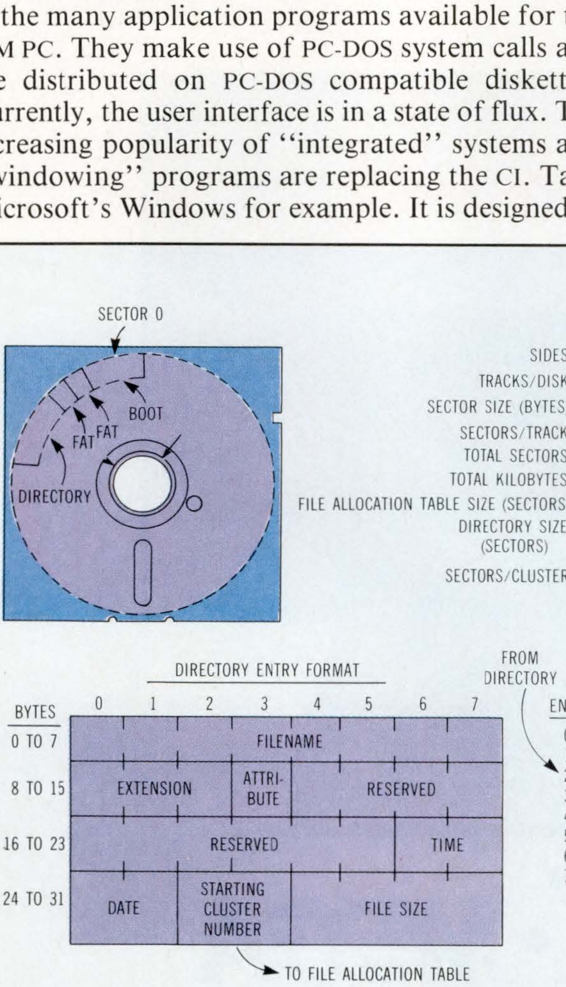
Considering realtime standards

As mentioned in the operating system interfaces background, it is easy to understand how the emergence of standard time-sharing and single-user operating systems affects the world of realtime applications, and subsequently, how realtime operating system standards emerge. First, it is important to realize the differences between realtime microprocessor applications, and time-sharing or single-user microcomputer or minicomputer applications. Most realtime microcomputer applications use "embedded" microprocessors. The processor is buried inside some larger instrument (robot, terminal, communication device, guidance system, or copier, among others); the end user is unaware that a microprocessor is present. The software that directs these systems is primarily concerned with monitoring and controlling devices that are, for the most part, not standard computer peripherals.

Perhaps the most important characteristics of realtime software are responsiveness and multitasking. The system must respond to device-generated interrupts rapidly enough to control some ongoing process—the system is even said to be interrupt-driven. The software must also handle many tasks concurrently, since in the real world, events generally overlap each other. A realtime operating system is designed to provide application programs with realtime, interrupt-driven, multitasking services, as



	VERSION 1		VERSION 2	
SIDES	1	2	1	2
TRACKS/DISK	40	40	40	40
SECTOR SIZE (BYTES)	512	512	512	512
SECTORS/TRACK	8	8	9	9
TOTAL SECTORS	320	640	360	720
TOTAL KILOBYTES	160	320	180	360
FILE ALLOCATION TABLE SIZE (SECTORS)	1	1	2	2
DIRECTORY SIZE (SECTORS)	4	7	4	7
SECTORS/CLUSTER	2	2	2	2



FILE ALLOCATION TABLE ORGANIZATION (EXAMPLE)

ENTRY	VALUE	USE
0	FFE	SINGLE-SIDED
1	FFF	FILLER
2	003	NEXT CLUSTER: 3
3	004	NEXT CLUSTER: 4
4	FFF	LAST CLUSTER IN FILE
5	000	UNUSED CLUSTER
6	000	UNUSED CLUSTER
7	FF7	BAD CLUSTER

Fig 1 The PC-DOS 5¼-in. floppy disk media standard is well specified. Version 1 floppy disks work in Version 2 systems, but not vice versa. The differences in some key parameters are shown in the illustration, which also shows a typical file allocation table.

well as more traditional I/O services (which must also be compatible with multitasking).

To explore the standards that have emerged in the world of realtime operating systems, consider each of the four operating system interfaces. Just as the Unix application interface was separated into process control services and I/O services, the application interface of a realtime operating system is separated into a group of task-control services and a group of I/O services. The clearest example of a realtime operating system interface standard has emerged for task control services. Here, VRTX system calls (Table 2) constitute an industry standard by virtue of their widespread acceptance and implementation across multiple architectures.

An I/O services standard has not yet emerged, although the introduction of IOX and FMX may change this situation. Meanwhile, either the Unix STDIO interface or the PC-DOS application interface (both are largely I/O services) may develop into realtime standards. This results from the increased popularity of the C language and the widespread availability of PC-DOS application programs. Also a factor is the desire of manufacturers to embed entire PCs inside their instruments.

No user interface has yet emerged in the realtime world, nor is this likely to happen any time soon. Realtime programs are characterized by a minimum of user interaction. Where user interaction occurs, it is usually by means of special purpose devices. There is also no media interface that has developed into a standard. But, the IBM PC's floppy disk format probably has the best chance. At present, floppy disk drives are cheap enough, small enough, and reliable enough to be installed in a great many instruments. And, although many embedded applications have no need for any magnetic media device at all, a significant fraction can use floppy disks for data logging.

Since embedded, realtime applications are characterized by specialized, nonstandard devices, it is unlikely that any one device interface standard will ultimately prevail. However, there seems to be a certain amount of momentum behind the Small Computer System Interface (SCSI, originally called SASI). It can be used for disks, tapes, and some character I/O devices.

Realtime components

Two companion components to VRTX, namely the IOX and the FMX, provide a package of device and file I/O services to complement VRTX's task management services for realtime applications. In fact, they support overlapped, high performance I/O operations by handling multiple tasks in multiple files and devices. The first FMX product, called FMX/DOS, is media compatible with PC-DOS; diskettes may be transferred directly between FMX/DOS systems and PC-DOS systems. Tables 3 and 4 show

TABLE 2

VRTX System Calls

Task management:	
SC_TCREATE	Task create
SC_TDELETE	Task delete
SC_TSUSPEND	Task suspend
SC_TRESUME	Task resume
SC_TPRIORITY	Task priority change
SC_TINQUIRY	Task inquiry
SC_LOCK	Disable task rescheduling
SC_UNLOCK	Enable task rescheduling
Memory allocation:	
SC_GBLOCK	Get memory block
SC_RBLOCK	Release memory block
SC_PCREATE	Create memory partition
SC_PEXTEND	Extend memory partition
Communication and synchronization:	
SC_POST	Post message
SC_PEND	Pend for message
SC_ACCEPT	Accept message
SC_QPOST	Post message to queue
SC_QPEND	Pend for message from queue
SC_QACCEPT	Accept message from queue
SC_QCREATE	Create message queue
Realtime clock:	
SC_GTIME	Get time
SC_STIME	Set time
SC_TDELAY	Task delay
SC_TSLICE	Enable round-robin scheduling

TABLE 3

IOX System Calls

Type	Call	Description
Channel control	io_opend	Connect a channel to a device
	io_close	Disconnect from a device
Buffered I/O	io_get	Read bytes from a device
	io_put	Write bytes to a device
Direct I/O	io_read	Read a block from a device
	io_write	Write a block to a device
	io_cntrix	Device control operation X
	io_wait	Wait for oustanding I/O requests
	io_rest	Reset the I/O error indicator
Device definition	io_dfchr	Define a character device
	io_dfblk	Define a block device
	io_dfdsk	Define a disk device
	io_rmdef	Remove a device definition
Device servicing	io_post	Post an I/O request completion
	io_rxchr	Put a character into the input buffer
	io_txrdy	Transmit-ready interrupt received
	io_echo	Put a character into the echo buffer
	io_stmr	Start the device timer
	io_ctmr	Cancel the device timer
	io_timer	Announce an I/O timer interrupt
	io_excpt	Raise an I/O exception
System interface	io_init	Initialize IOX
	io_atchc	Connect an I/O handler

TABLE 4

FMX/DOS System Calls

Type	Call	Description
Volume control	fd_mount	Mount a file system volume
	fd_dmount	Dismount a file system volume
	fd_format	Format a file system volume
File operations	fm_create	Create a file
	fm_delete	Delete a file
	fm_rename	Rename a file
	fm_gattr	Get the file attributes
	fm_sattr	Set the file attributes
	fm_cntrix	File control operation X
Directory operations	fm_crdir	Create a directory
	fm_deldir	Delete a directory
	fm_gdinfo	Get directory information
File connection operations	io_openf	Open a file (relative to a directory)
	io_close	Close a file
File I/O operations	io_get	Read bytes from a file
	io_put	Write bytes to a file
	io_read	Read a block from a file
	io_write	Write a block to a file
	io_wait	Wait for outstanding I/O requests
	io_reset	Reset the I/O error indicator

the C language interfaces that are defined by these two components.

IOX and FMX modules are separated. I/O operations are logically distinct from the details of particular disk file formats. Future FMX products will support such popular file formats as Unix and CP/M. Because systems may be designed with several FMXs sharing a common IOX, the same operating system will be able to read both CP/M and PC-DOS diskettes. The PC-DOS media is, in fact, quite compatible with FMX.

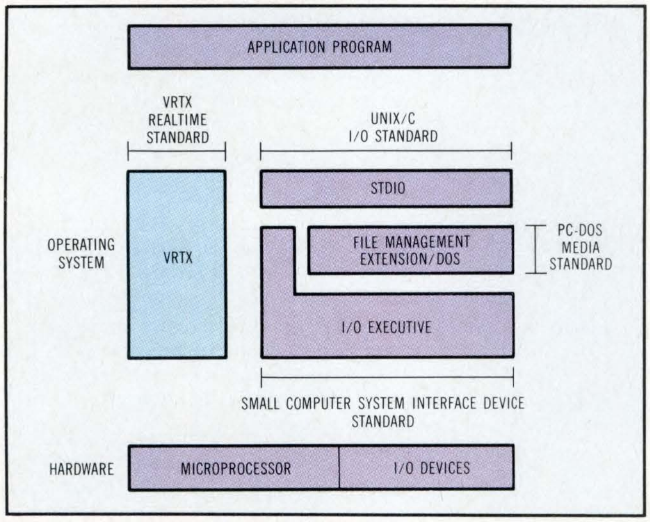


Fig 2 A typical VRTX-based realtime operating system can have four modules that take care of a realtime tasking services interface, the STDIO I/O services interface, the PC-DOS media interface, and the Small Computer System Interface (SCSI) device interface. Other modules are under development.

The device interface for the two new components is between IOX and the devices; FMX interfaces to IOX and has no direct device connection. The IOX device interface is very similar to SCSI, so SCSI-style devices require no "device drivers." They simply connect directly to IOX. Non-SCSI devices require simple device service routines and interrupt handlers to make the IOX connection.

Additional software components to translate Unix/C STDIO calls into IOX/FMX calls and to translate PC-DOS system calls into IOX/FMX calls are on the way. These interfaces will allow the PC-DOS and STDIO standard interfaces to exist in a realtime context. Details on STDIO compatibility are given later in this article.

Fig 2 illustrates a diagram of a realtime operating system made up of four available Hunter & Ready components. This system supports four different standard interfaces that include the VRTX realtime tasking services interface, the STDIO I/O services interface, the PC-DOS media interface, and the SCSI device interface.

Media compatibility

The PC-DOS format was chosen because it is compatible with so much off-the-shelf software. For example, data logged by a realtime data acquisition system can be read directly and analyzed by available personal computer software. Media compatibility has been achieved, however, without limiting the capabilities of FMX/DOS. Indeed, the built-in FMX/DOS facilities broaden its range of applications and make it a particularly appropriate choice for use in realtime embedded microprocessor designs.

FMX/DOS provides several methods for guaranteeing timely access to file data and for ensuring proper operation in a multitasking environment. For example, shared file access is permitted, and multiple I/O requests are processed asynchronously, while tasks execute concurrently. In addition, multiple buffers eliminate task waiting for most sequential I/O operations, and updates are cached in memory to eliminate unnecessary disk accesses.

There are still other features. First, files can be allocated contiguously to minimize disk head movement. The use of contiguous pre-allocated files provides the consistent response time required in many realtime environments. Second, directory entries and file allocation tables are cached in memory to speed the process of locating files and allocating disk space. Third, unnecessary directory searches can be avoided by specifying file names that are relative to a particular directory (a generalization of the "working directory" concept found in many operating systems). Finally, relative file names avoid the need to begin all searches at the file system's top directory level ("root"). None of these facilities are available

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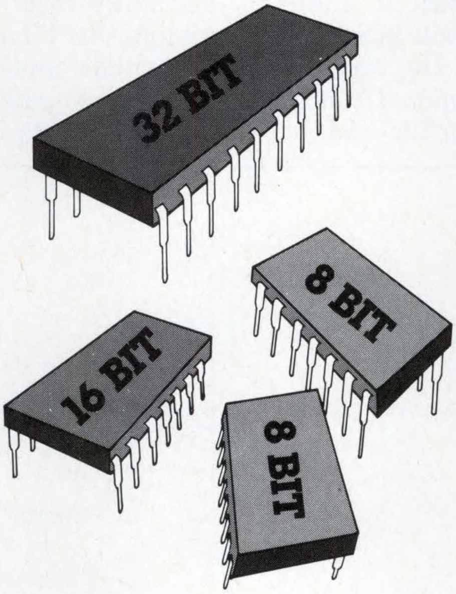

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CIRCLE 105

in PC-DOS (or MS/DOS), which was designed for more specialized and less demanding applications than FMX/DOS.

Embedded systems demand a high degree of system integrity in that file system consistency must be maintained at all times. FMX/DOS ensures that the file system is always consistent and intact by writing directory and file allocation table (FAT) entries out to disk whenever they are modified. Also, calling programs can force modified file buffers to be written to disk on demand.

For applications in which media compatibility is not an issue, the granularity of disk space allocation can be changed. Whenever FMX/DOS needs to extend a file, it allocates disk space in clusters. Generally, a smaller cluster size will increase the amount of usuable disk space at the expense of time lost in performing allocations more frequently. Access times can also be longer for files that have many clusters, because the contents of the file tend to become scattered over the entire disk. FMX/DOS reduces this tendency by grouping clusters allocated for the same file.

A look at I/O library compatibility

Many high level programming languages such as Fortran and Pascal build I/O capabilities directly into the language definition. The interface between the compiler and the operating system is then generally left up to compiler implementation. Fortunately, I/O functions in the C language are available through the language's normal function call mechanism as a STDIO. Thus, the implementation of I/O is decoupled from the language. This is one of the reasons that C has become a popular choice for use in realtime applications.

STDIO compatibility can be achieved several ways. One simple way is to rely on a compiler vendor to

```
main( )
   {
   int    i , j;
   char  *lit

      lit = "string literal";
      i = 0;
      j = 1;
      printf ( "two numbers %d , %d  \n and a %s\n", i, j, lit );
   }
```

(a)

```
 push  bp
  sub  sp, +06
  mov  bp,sp
  mov  ax,000c
  mov  word ptr  [bp+00] ,0000
  mov  word ptr  [bp+02] ,0001
 push  ax
 push  [bp+02]
 push  [bp+00]
  mov  bx,001b
  mov  [bp+04] ,ax
 push  bx
  call  printf
  mov  sp, bp
  add  sp, +06
  pop  bp
   ret
```

(b)

```
ss:sp→   00       return address
         02       offset of format string
         04              i
         06              j
         08       offset of literal string
```

(c)

```
PUSH   BP                      ; save registers used
MOV    BP, SP                      ; set up stack frame pointer
ADD    SP, 06H                     ; add space for local variables
PUSH   AX                      ; save some more registers
PUSH   BX
PUSH   CX
PUSH   DX
PUSH   SI
PUSH   DS
PUSH   ES
MOV    AX, 0005H               ; function code for SC_TINQUIRY
MOV    CX, 0000H               ; ask about self
INT    20H                     ; component call to VRTX
MOV    AX, ES:WORD PTR[BX+06]    ; get TCB extension address
                                 ; segment
MOV    DS, AX                     ; use as current data segment
MOV    SI, ES:WORD PTR [BP+04]    ; get TCB extension address
                                  ; offset
MOV    AX, DS:[SI]                ; get tasks i/o channel id
MOV    WORD PTR [BP-06] , AX        ; put channel id in local
                                    ; data block
MOV    AX, SS                     ; get current value of stack
                                  ; segment
MOV    WORD PTR [BP-02] , AX        ; put printf argument segment
                                    ; in block
MOV    AX, BP                     ; get current value of frame pointer
ADD    AX, 04                     ; offset for printf argument list
MOV    WORD PTR [BP-04] , AX        ; put in data block
MOV    AX, BP                     ; get current value of frame pointer
SUB    AX, 06H                    ; stack offset for local data block
MOV    BX, AX                     ; put in component argument
                                  ; register
MOV    AX, SS                     ; get current value for stack
                                  ; segment
MOV    ES, AX                     ; put in component argument
                                  ; register
MOV    AX, 0401H               ; function code for PRINTF
INT    20H                     ; component call to STDIO
POP    ES                      ; restore registers
POP    DS
POP    SI
POP    DX
POP    CX
POP    BX
POP    AX
POP    BP
RET                            ; return back to caller
```

(d)

Fig 3 An example of what the modules can accomplish starts with the code section in (a). On the IBM PC, the code produces assembly language (b); the language interface library implementation of printf is based on the stack format in (c) and is shown in (d).

produce a C compiler, which includes an STDIO library that is targeted for a specific operating system such as the IBM PC.

The limitations of this approach are fairly obvious. Since the STDIO interface is provided by the compiler vendor, it is limited to programs on that vendor's compiler. Moreover, since most PC-DOS programs are not reentrant, it is unlikely that the vendor will have written the library to be reentrant. If it is not reentrant, the library cannot serve in realtime multitasking applications since reentrancy is a prerequisite for multitasking performance.

The same problems of reentrancy and the limitation to one compiler's output occur with almost any vendor's STDIO no matter what operating system the library executes on. So, it made little sense for Hunter & Ready to interface IOX and FMX to any existing STDIO implementation. Instead, the decision was made to develop a multitasking, reentrant, software component implementation of STDIO.

This STDIO is provided as a software component. Each compiler is targeted to the component in much the same fashion as compilers are targeted to VRTX. In other words, a "language interface library" is supplied that maps the compiler's calling conventions onto those required by the component.

The code fragment shown in Fig 3(a) is a good example of what is possible with the STDIO design. This code is an example of a C program that uses the STDIO function printf to perform formatted I/O. When this program is compiled with a generally available compiler running on an IBM PC, the assembly language code in Fig 3(b) is produced. Notice that the fifth command from the end is a call to an external procedure called "printf." The language interface library contains a routine called "printf" that is responsible for translating this call to the STDIO component.

The language interface library implementation of printf for this compiler is illustrated in Fig 3(c). The stack is referenced frequently in the code; upon entry to printf, the stack has the format shown in Figure 3(d). Note that the INT 20H call is a software interrupt instruction that is used to call the component STDIO. In short, the result of the implementation of STDIO as the component STDIO is that the standard Unix/C I/O interface can be used in a multitasking environment.

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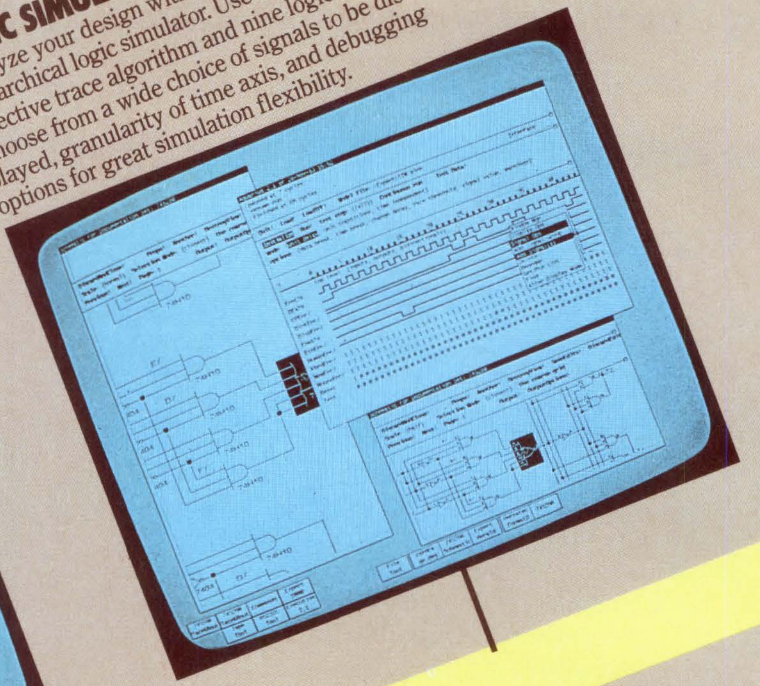

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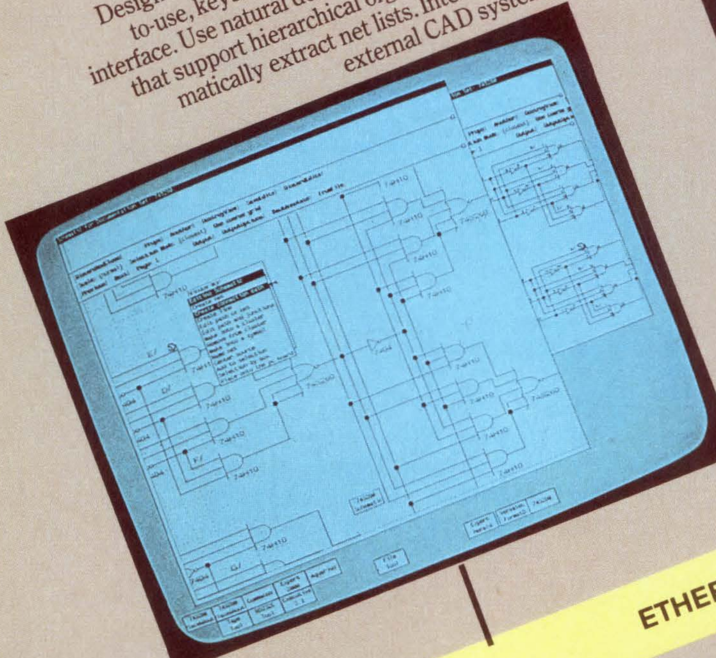

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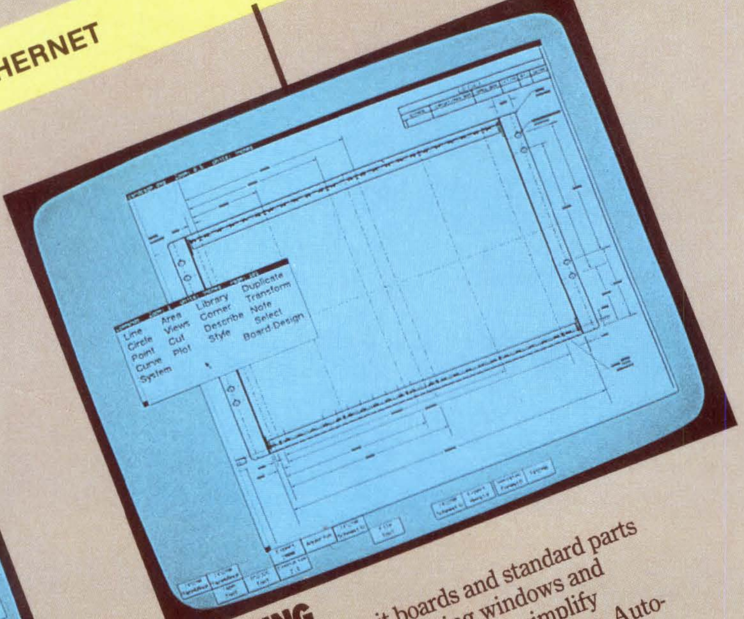

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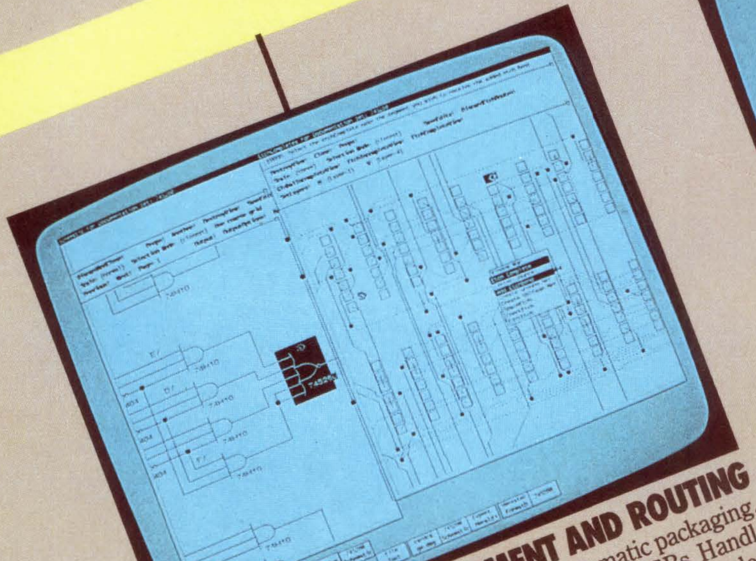

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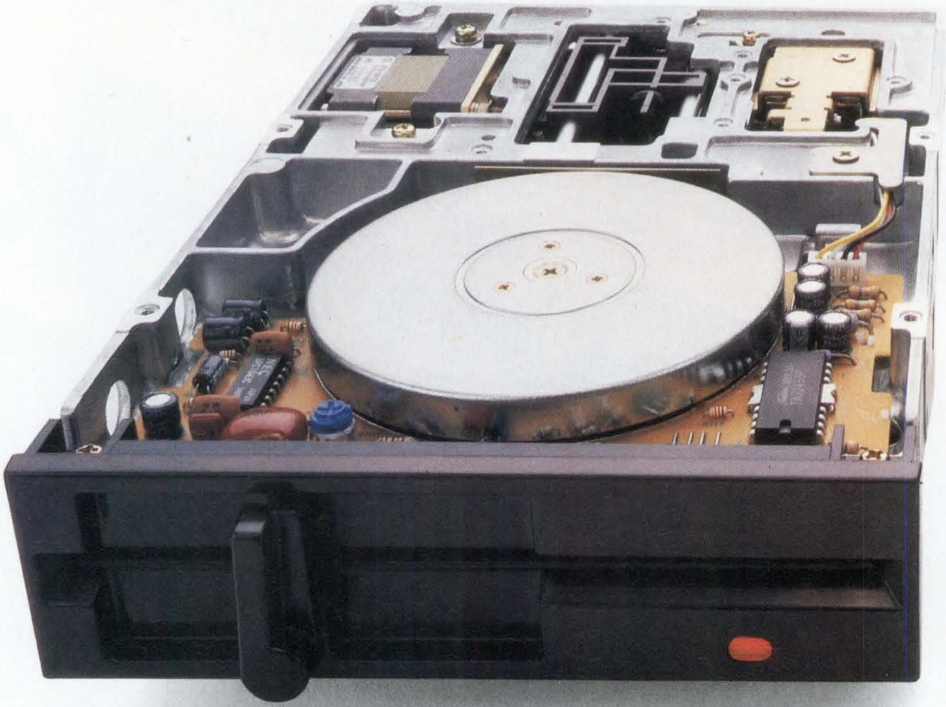

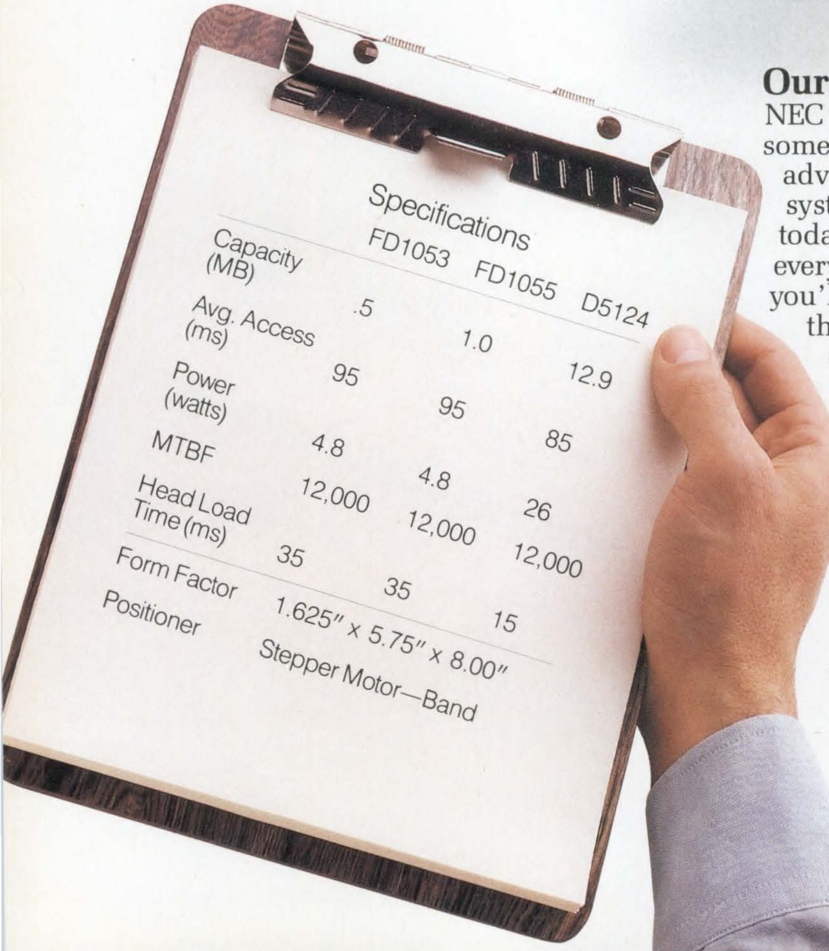

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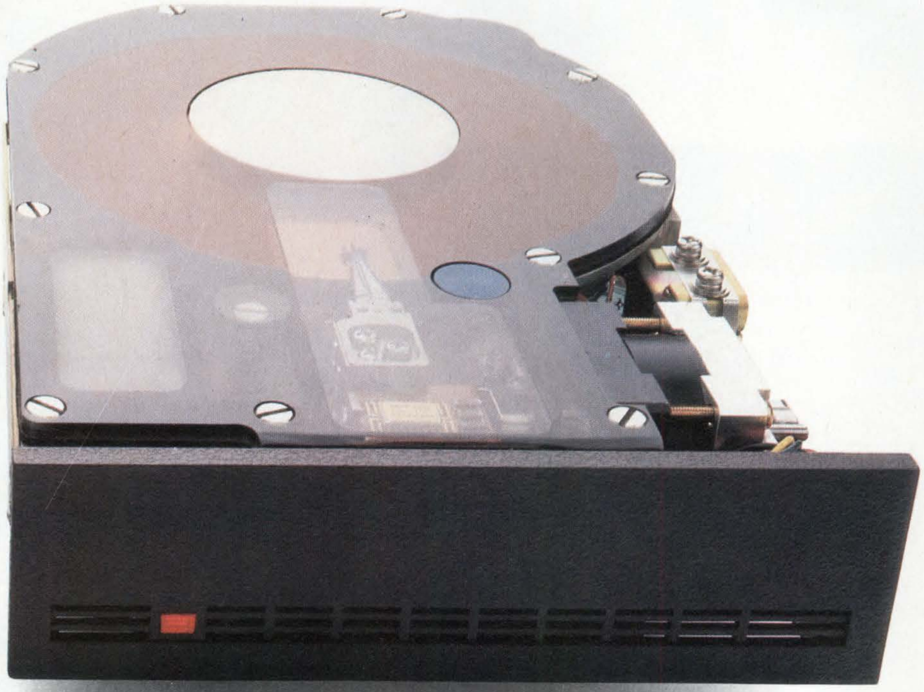

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A MODULE APPROACH TO MICROCOMPUTER OPERATING SYSTEMS

One way to create an operating environment is to offer every capability in one operating system. It is just a matter of picking the right modules and hooking them up.

by John Little

As microcomputers and their environments become more advanced, system developers and end users begin to realize the limitations of current operating systems. There are increased demands for networking, sophisticated database applications, improved user interfaces such as windows, and powerful tools to build applications. All of these demands emphasize the weaknesses of today's popular operating systems.

There are three ways to make an operating system more functional (Table 1). First, application packages can implement needed features. Third-party software vendors have often taken this approach. Second, existing operating systems can be patched to provide the necessary features. This is the approach taken by Microsoft's Windows, Visi Corp's VisiOn, and the numerous enhanced versions of Unix. Third, the necessary features can be designed directly into the operating system. This is, in essence, the concept used in the S1 operating system from Multi Solutions. This system promises a solution to the advanced capabilities problem of current systems.

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There are many disadvantages to adding more features at the application level. For example, each new application must "reinvent the wheel" and create, from scratch, those particular features that it needs. Each of the modifications will probably be incompatible with those made by other software modifiers. Frequently, there is also a substantial penalty in execution efficiency. This is because the application itself cannot perform many of the necessary functions simply with the add-on approach. For example, given the existence of stream files, record and keyed files can be simulated (with reduced speed) by application programs. However, file locking (prohibiting several users from simultaneously accessing the same file) must be performed by the operating system itself and cannot be added to the application.

Modifying the operating system to provide the needed features (the second alternative) can be done either by making changes to the basic operating system or through add-on patches. However, each of these methods has severe limitations. Because most operating systems were not designed to support the add-on features of interest, modifications are usually haphazard add-ons that are not well integrated with the rest of the system. In addition, the efficiency of this approach is usually low, and each manufacturer's operating system patches are usually incompatible with all others. The current proliferation of "enhanced," incompatible Unix versions illustrates this problem. The operating system is being forced to do something that it was not designed to do, thereby causing frequent conflicts with its basic design principles.

TABLE 1 Three Approaches to Operating System Limitations		
Add Features to Applications	Modify or Patch Operating System	Design Better Operating System
maybe too slow	maybe too slow	greater efficiency
no standard version of code feature	may conflict with basic design	standard implementation
much work for the programmer	poorly integrated, inconsistent	consistent, well-integrated features
some features cannot be added to applications		

The third approach, which avoids all these difficulties, is to design the operating system so that all interesting and useful features can be easily included. To avoid premature obsolescence, the operating system should be extendable, allowing future enhancements to be made without affecting the system. The S1 operating system is designed in this way.

Make it modular

The S1 approach produces a module, highly functional operating system that is suitable for a wide range of applications on a wide range of computers. As such, S1 is a highly modular system. For example, in S1, each basic operating system function (eg, multitasking, scheduling, device management, windowing) is implemented as a separate module (Table 2). Each module communicates with the system via procedure calls. S1 versions are currently available for the 68000, 68010, 8080, 8085, and Z80 microprocessors. Ports for the 8086, 80186, 80286, and several others are under development.

TABLE 2

The Set of S1 Modules

multi-user	terminal support
tasking	line
multitasking	full screen
gates	windowing
events	bit-mapped
file directories	vector graphic
hierarchical	time management
flat	device management
scheduler	image management
voluntary dispatch	absolute
round robin	relocating
priority	linking
dynamic	overlay
file processing	messages
stream	intertask
record	general
indexed	queues
file allocation	arithmetic
linked allocation	character conversion
mapped allocation	command processor
contiguous allocation	menu
multi-user	conventional
groups	prompting
privilege classes	command lists
network	resident commands
networking	

Modularity provides several advantages. First, since each module is distinct, functions can be included or omitted as needed. For example, if windowing is not desired, the windowing module can be omitted, producing a smaller S1 version. Virtually any of the modules in Table 2 can be included or omitted as needed. Versions of the system can be specifically tailored to the individual application using the S1 "generate" command. If an application program attempts to use a function that is not included, then a "condition" is raised in the calling program. Conditions are software interrupts that are similar to "signals" in Unix and PL/I. They are used to inform programs of certain events, such as "divide by zero" or "invalid system call arguments." The user can choose to perform various actions when conditions are raised, or the system will perform a default action. In the case of a system call that is not present, the "notcapable" condition is raised. Applications can use this condition to adapt themselves to the specific hardware and software configuration of the microcomputer system.

Given the modular nature of the S1 system, the boundary between the operating system and applications is made less distinct (Fig 1). Most operating system modules can be linked into user code, allowing these functions to be performed by the applications themselves. Also, any utility (both standard and user-provided) can be linked into the operating system and made resident. This procedure not only improves the response time to the user, it also gives both the system and application developer flexibility in tailoring the system to their particular requirements.

The implementation of S1 modules is straightforward. Each one is a collection of procedures called to perform certain tasks. The entry points to these procedures are known as "system calls." Application programs and other operating system modules access the code in conceptually the same way by simply calling a procedure. The procedure arguments are saved, the procedure code is executed, and a value may be returned. Although each module may have local data structures, S1 has no global data structures. Each module is responsible for maintaining the information that it needs within its local storage.

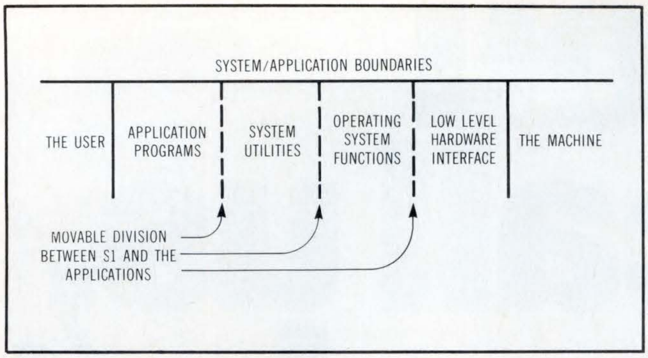

Fig 1 With the S1 operating system, the division between the operating system and application programs is arbitrary. Modules implementing system functions can be linked into applications, and both utilities and applications can be included in the developer-tailored system.

The actual mechanism of system calls is different for application and system modules. The description of this mechanism for the Motorola 68000 is typical (Fig 2). Application programs that issue system calls must be linked with a library of system call access routines. These library routines store a value in the 68000's D0 register that specifies the system call. Then they execute a TRAP instruction. In the next step of the procedure, the operating system catches the trap and examines the value in D0. This value may meet one of three conditions.

If it is outside the valid range of values, then the "invalidsystemcall" condition is raised. If it is within the valid range, but the related function is not present in this version of S1, then the "notcapable" condition is raised. If it is a valid system call, and the user has the appropriate permissions, the code is executed, and control returned to the calling program.

System routines that use system calls do not use the TRAP mechanism. Instead, the procedure calls are resolved by the linker. Then, the desired code is executed directly.

Many functions

The S1 operating system includes modules that implement a wide range of capabilities, thus providing a rich environment for program development and execution. S1 draws its inspiration from a variety of systems, ranging from experimental operating system developments, to features on existing minicomputers and mainframes. Consider, for example, the S1 file system.

The file system is perhaps the most heavily used function of the operating system. The S1 operating system has a fully featured file system designed for producing sophisticated applications. One type of file is the stream file. Stream files are unstructured, and can be written or read at any position. They can contain up to four billion bytes and are similar to those used in Unix.

In many applications, the data stored in files has some type of structure associated with it. This data may be inventory records, lines of text, or database entries. S1 record files allow these groups of related data to be stored and manipulated as a single entity called a record. Records range in size from 1 to 4 billion bytes each, can be of fixed or variable length, and can be inserted or deleted at any point in the file. Since a large record file may contain thousands, even millions, of records, searching such a file for a particular record may be prohibitive. To get around this problem, S1 features keyed files.

Each keyed file possesses one or more indices that specify the locations of records with particular values. Inventory files can be indexed by part number, by manufacturer, by cost, or by any other value contained in the record. A particular record can be accessed via its index, rather than by searching the entire file. Indexing is done automatically by the system, and as records are added or removed, the indexes are updated automatically.

S1's keyed files are implemented with either indexed sequential access method (ISAM), virtual storage access method (VSAM), or B-trees. Each method has its particular advantages, and users can pick the one best-suited to their applications. Specialized access methods can easily be added by the user to optimize certain types of accesses. For example, a hashed access method could easily be added to support some types of database organization.

S1 allows the user to specify the method used to allocate space on the disk for the file. In contrast to most systems that provide a standard method, S1 provides three different methods (Fig 3), each offering different tradeoffs between speed and reliability. System developers or users can specify the allocation method best suited to their applications.

All S1 allocation methods share several characteristics. In each method, space on the disk is allocated in units called groups—one or more adjacent disk sectors. The basic description of each file is found in a directory which specifies the name of the file, the allocation method, and the file location.

The simplest allocation method is "contiguous allocation," especially useful for large, high speed data transfers. The user specifies how large the file will be when it is created, and one large group is allocated to hold the specified amount of data. Contiguous files can be accessed rapidly since the disk spends very little time "seeking" to different blocks in the file. Contiguous files are the least reliable since a lost directory entry will cause the file to disappear. There is also a problem with contiguous files when the initially allocated space is too small to hold the entire contents of the file. When this occurs, S1 allocates additional groups called "extents." The penalty for using extents is slower access, since the extents are usually not contiguous with the rest of the file.

The second allocation method is called "mapped." As disk groups are allocated, their addresses are placed on the disk in a "map." This map allows a particular block on the disk to be found fairly rapidly, since only the map must be searched to find the disk location of any part of the file. Mapped allocation is also useful for inserting and deleting records from the middle of the file since the map blocks can be reorganized without rewriting large parts of the file. With mapped files, however, if a map disk block is lost, then all of the data blocks pointed to by that block are lost.

The final form of disk allocation is known as "linked." With this form, each disk group contains pointers to the previous group, to the next group, and to the associated directory entry. This is the most reliable form since the destruction of any particular block results in the loss of that block only, and if the directory entry for the file is lost, the file itself can be completely recovered. This is also the slowest form because access to a particular location in the file requires that all of the preceding disk blocks be read in order to traverse the links. However, the system will optionally build an in-memory map of the disk blocks so that seeks to random locations will proceed quickly.

The S1 "recover" command helps users to recover data that was lost during disk failures. In general, it utilizes the redundant information stored on the disk to regenerate as much of the lost disk files as possible. The amount of data recovered depends on which allocation method was used and what type of failure occurred.

Intertask communications

S1 has extensive facilities for intertask communications that can be used to synchronize cooperating processes or to transmit information over a network. The first intertask communication primitive is the "event," which is used to signal the occurrence of a particular event to any task waiting for it. Tasks that are waiting for a particular event issue the "eventwait" system call and go to sleep. When the event is detected (by another task), the event is signaled with the "eventset" system call, and all tasks waiting for this event begin to execute again. The system allows an arbitrary number of events to be created and used.

Another primitive is the gate. Gates are used to control access to a resource and to provide either shared or exclusive access. Tasks that request a gate sleep until the gate can be granted. When they no longer need access to the resource, they free the gate. Tasks request access to the gate with the "gatelock" call, which offers either a shared access or exclusive access operating mode. If the gate can be granted, then the task continues executing; otherwise, it sleeps until the gate is available. When the process is finished with the gate, it issues the "gateunlock" call.

If the gate is currently shared access, then all subsequent shared access requests will be granted, until an exclusive access request is made. When this happens, all shared access requests will be blocked. After all the shared accesses have been unlocked, the exclusive access will be granted. By alternating between shared and exclusive access as needed, S1 ensures that both types of requests are processed. This same mechanism (with slightly different details) is used to provide file locking.

Another mechanism is the intertask message, a very fast mechanism for sending messages between tasks. Messages are sent with the "msgsend" system call and are received, as might be expected, with "msgreceive."

Shared memory, a very high speed intertask communications method, is still another capability. This mechanism slows cooperating tasks to access the same memory, but, it is limited to tasks on the same machine. Shared memory is created with the "sharedalloc" call and freed with "sharedfree."

A final communications primitive is the general message. It is similar to spool files in some operating systems. General messages are arbitrary-size data blocks that can be sent anywhere on the network. Facilities exist that allow messages to be placed in queues, to be forwarded to other queues of tasks, and to be returned to the sender. Typically, general messages are used for file transfer, electronic mail, and similar applications.

The S1 networking philsophy is that the distributed network of machines should mimic one large machine to both programmers and users. In short, the user should not be aware that network facilities are being used. Consequently, there are only two basic commands, "connect" and "disconnect," that are used to attach and remove a machine from the network. Both commands are independent of network topology, interconnection hardware, and communication protocols. The intertask communication primitives previously described are usually all that are needed to produce network applications.

Drivers are used to implement the protocols and hardware interfaces for S1 networking. Changing

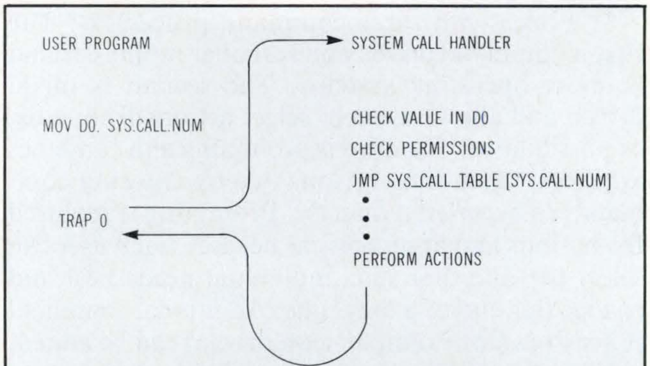

Fig 2 The actual mechanism of system calls is different for its application and system modules. The illustration applies to a Motorola 68000 microprocessor-based S1, but the same principles are used regardless of the microprocessor chosen by the computer designer.

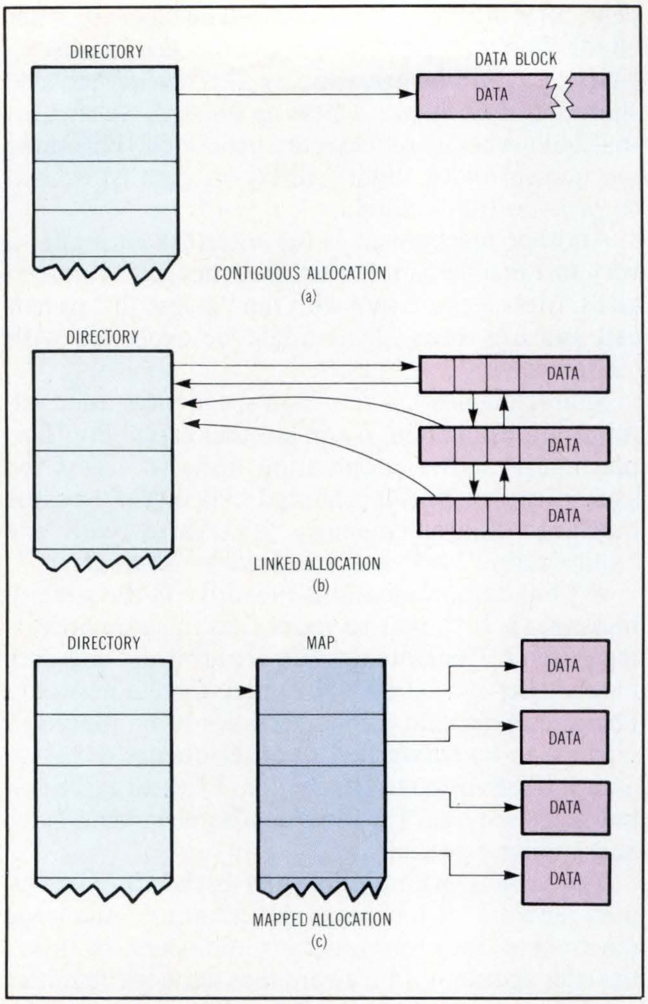

Fig 3 The computer system designer may choose from three disk allocation methods with the operating system. Contiguous allocation (a), linked allocation (b), and mapped allocation (c) all have advantages and disadvantages that must be taken into account.

the interconnection hardware or protocols is a matter of loading a new driver routine. Thus, the networking software, includes X.25, SNA, TCP/IP, Ethernet, and broadband coaxial cable, among others.

Command processors

S1 comes with three command processors. The first is command driven and is similar to those found in most operating systems. The second is menu driven and allows users to select actions from a list of possibilities. The third is prompting and combines attributes from the previous two by allowing commands to be entered directly. Prompting is required for options and arguments as needed. Each user can select the one that suits individual needs best and change this choice at any time. Additional command processors (for example, icon driven) can be added.

The operating system was explicitly designed to be portable across a wide range of hardware. Portability is achieved through several methods. First, SL, the system implementation language, is exactly the same on all machines (from small 8-bit micros to large 32-bit systems). Integers are always 16-bits, long integers are always 32-bits, and so forth. Unsigned arithmetic is used for all operations, so that there is no question about operations such as sign extension. Most common system implementation languages, including C and Pascal, are not truly machine independent, so their system code must usually be modified when switching to a different architecture.

Second, all of the machine-dependent parts of the operating system (mainly device interfaces) have been isolated into modules called "drivers." A port to a new machine or architecture is well defined, since all of the machine-dependent parts are known in advance.

Third, system data structures were designed to be machine-independent. A common problem on many computers is that the byte order of data differs. Some machines store the MSB of a 2-byte integer in the lower address, others in the higher. This storage method difference means that tapes and disks generated on some machines are unreadable by others. To solve this problem, all S1 data structures are stored in a common byte order. Consequently, any S1 machine can read a disk written on any other machine, and many different types of machines can be networked together.

The real-world power of S1 and its modules is illustrated by examples of several different applications. For example, it can easily be configured for workstation applications. Actually, most workstation networks have several types of machines with greatly different requirements. Besides the conventional single-user workstation with local disk storage, most systems also feature a typical workstation with a fast processor (68000, 80286, 16032), a small (10- to 20-Mbyte) disk, a high resolution display, and a high speed communication facility (Ethernet). The operating system for this hardware would include the S1 modules for windowing, bit-mapped displays, networking, and multitasking. Since workstations are intrinsically single-user, the multi-user support can be omitted.

A low cost workstation has less memory, a lower resolution display, and no disk. But, it still retains high speed communications. It uses disks on other machines for its long-term storage. This version of S1 resembles the previous version, but omits the local file system support and the disk drivers. Instead, a remote file system module is substituted, which gives this machine full access to the other network disk. Other features could be omitted to produce a smaller S1 version. In addition, the "connect" and "remotelogin" utilities can be configured into S1, and the entire operating system burned into PROM. When the machine is turned on, it will automatically attach to the network and begin normal operation.

A high end workstation can be built around multiple CPUs, either general or special purpose. For

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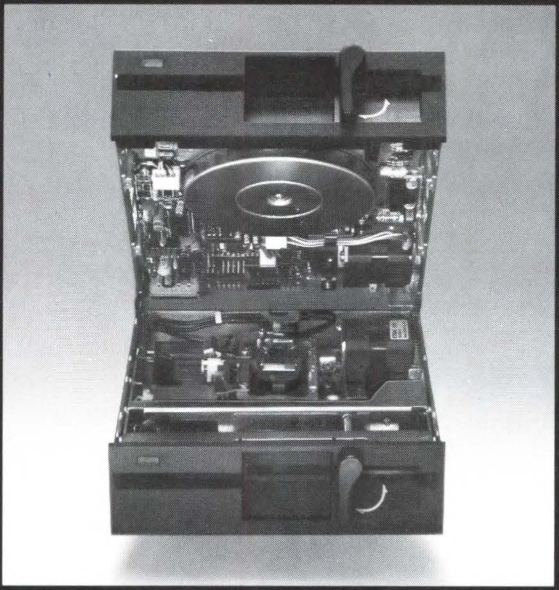

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example, a computer aided design (CAD) station may include several 68020s, a floating point accelerator, and a graphics processor. S1 is designed for multiprocessor operation, and can support up to 255 processors on the same bus. Additional processors can be added to increase the machine's speed without affecting applications programs.

Servers can also be accommodated by S1 and its modules. Servers are dedicated machines that provide specific services to other networked machines. For example, disk servers give the other machines access to large amounts of disk storage, print servers allow multiple users to share the same printers, and communications servers are gateways to other computers and networks.

Requirements for a server operating system are very different from those of a workstation. Since a single server is shared among a number of users, it must be able to fairly allocate its resources to the demands of the network. S1 allows the system to be tuned to vary its response characteristics. With the system, it is difficult for a misbehaving task to use more than its share of resources.

Disk servers will usually handle a large number of disk transactions. The actual throughput to the disk can be varied over a wide range by varying the number of I/O buffers. Buffering allows frequently accessed data to be stored in main memory, so that every I/O request does not access the relatively slow disk. S1 allows the user explicit control over disk buffering so that a large number of buffers can be allocated. Also, each user has a buffer pool so that one misbehaving user cannot overly affect the response of others. The number of buffers is limited only by the amount of main memory.

Servers frequently provide more than one service. For example, one machine may work as a disk server, a communications server, and a print server. These three applications each have different speed requirements. Disk requests should be completed as soon as possible; communications transactions often have time constraints, while print jobs can usually be delayed if necessary. The S1 priority scheduler in the server will consider these characteristics and allocate machine resources accordingly. The priorities can be adjusted to provide the best service.

Realtime data acquisition

The S1 is well suited for realtime systems. A version that includes contiguous files, the priority scheduler, and the intertask communication primitives will serve as the base for this system. Contiguous files provide high disk throughput; the priority scheduler provides the explicit priority control that realtime systems need; and the intertask communication mechanisms allow tasks to synchronize themselves with external events. In addition, the system calls are designed to permit rapid interrupt response and are all reentrant.

The S1 system can be the basis of a multi-user, time-sharing system. The basic time-sharing version would include the modules for multi-user, multitasking, and dynamic scheduling. Additional modules, including networking (for compatibility with S1 workstations), advanced file system (for mainframe-type application software), windowing and bit-mapped displays (for improved user interfaces) can all be added as needed.

The operating system's multiprocessor support allows additional processors to be added as the user population grows. This allows incremental growth in computing power. Alternatively, multiple time-sharing systems can be tied together to provide an integrated, high capacity system.

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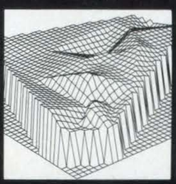
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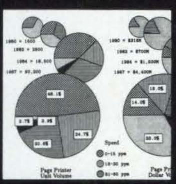
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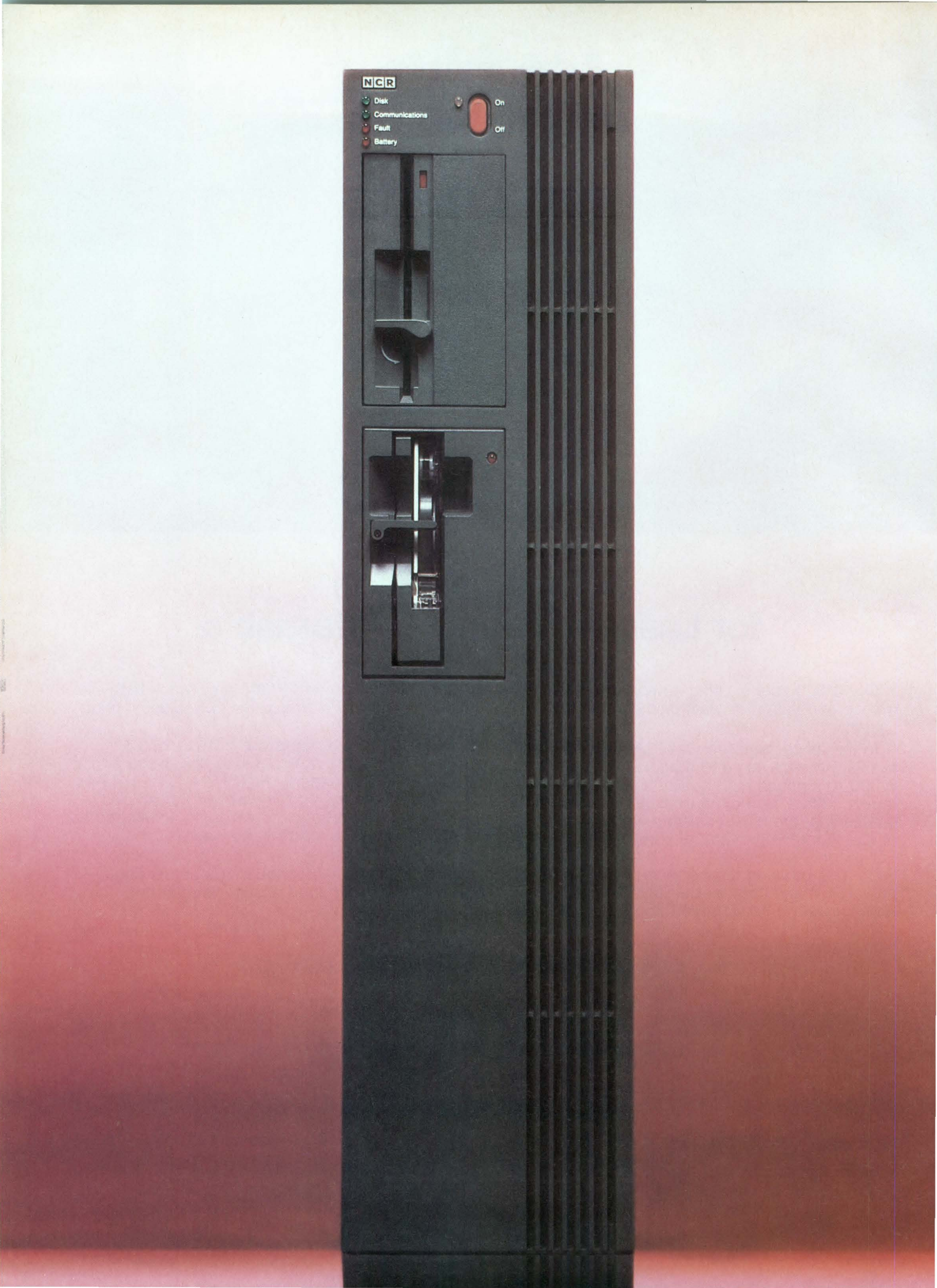
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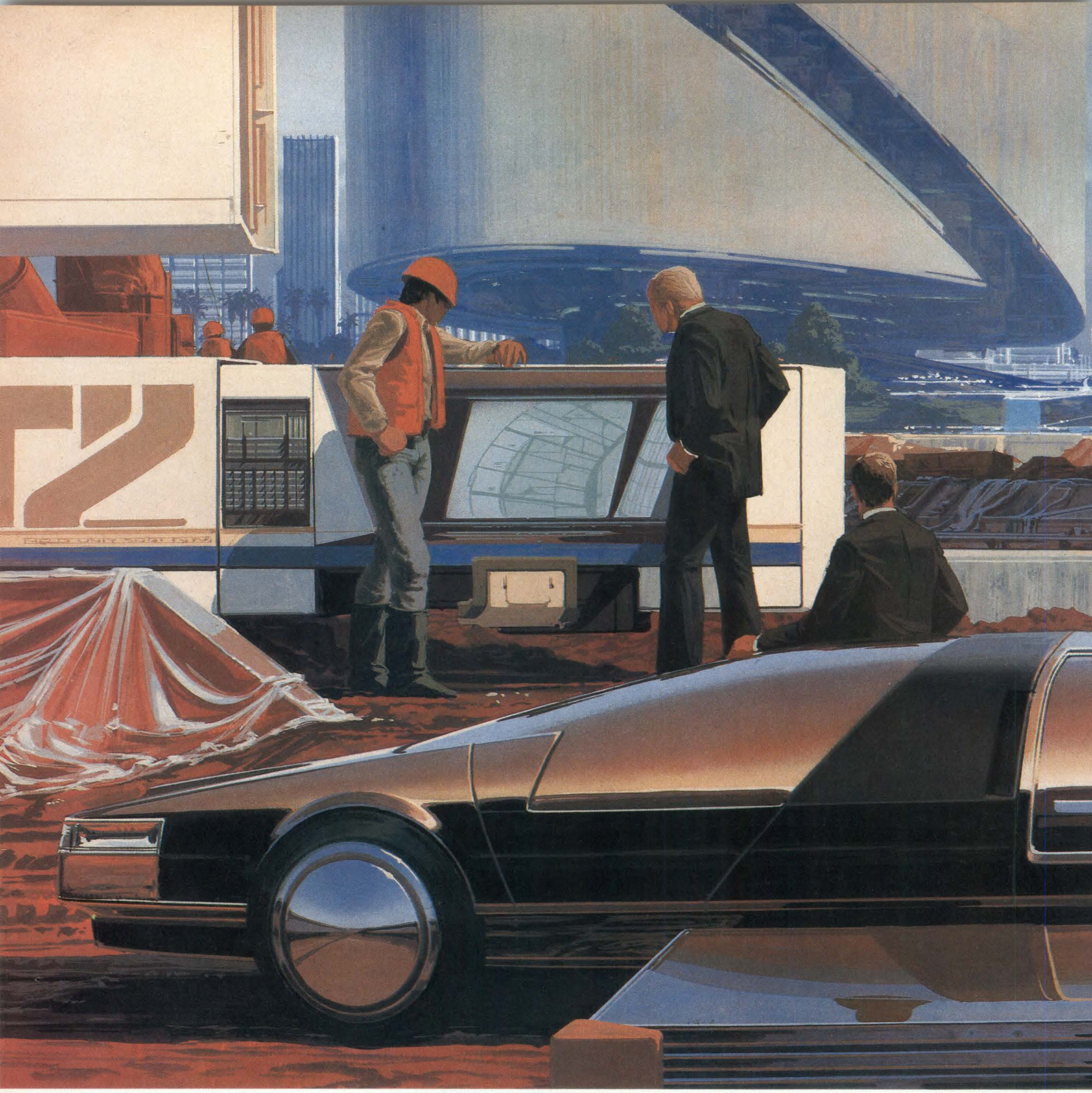

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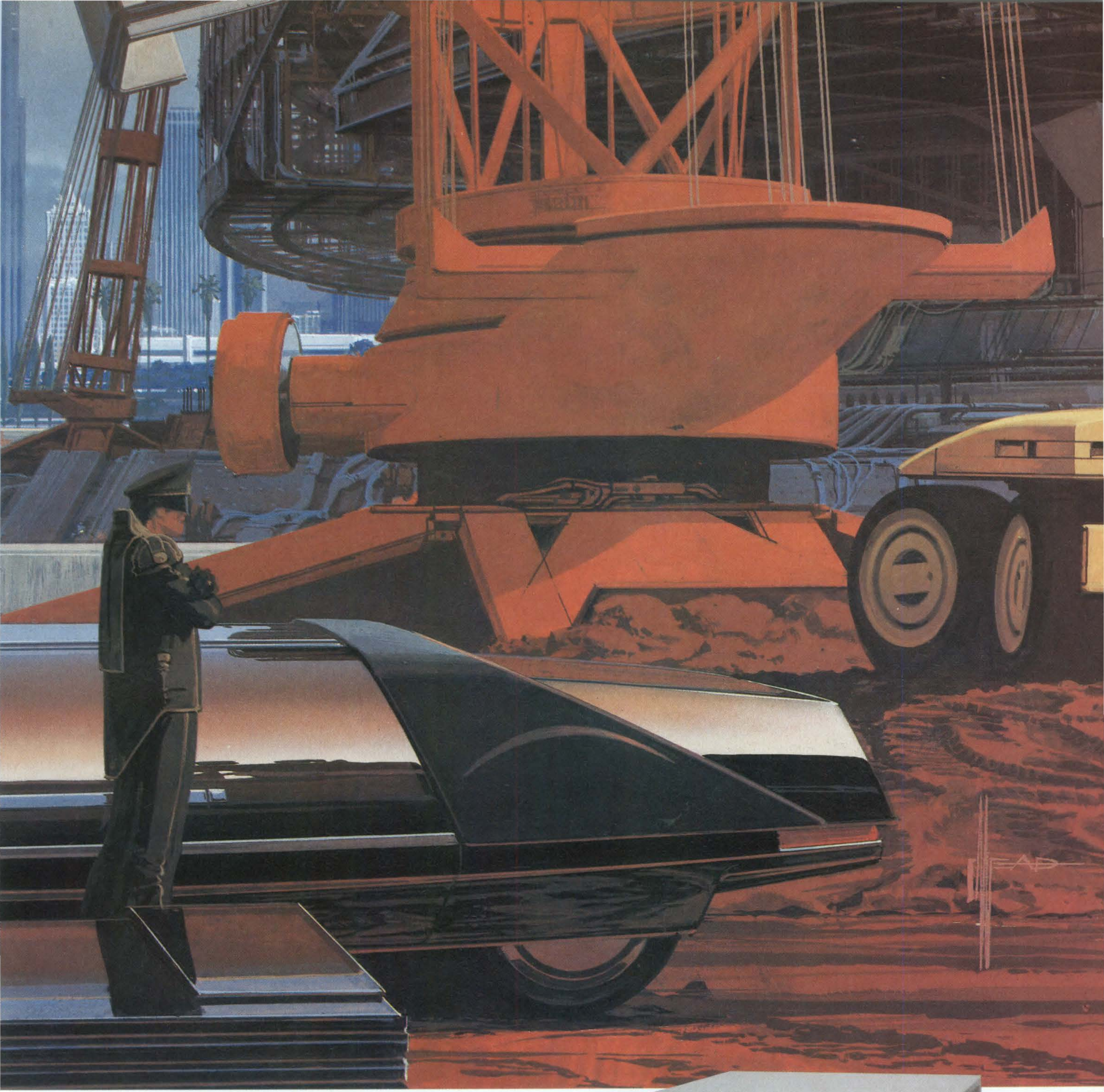

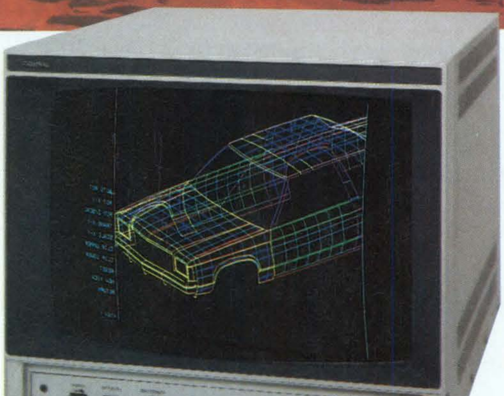

OBJECT MODELS SIMPLIFY AND SPEED SYSTEM DESIGN

A computer network that handles voice and data needs a specially designed operating system. The design technique is useful for other computer networks linking different microcomputers.

by Gary L. Passon

A computer system designer or integrator with the task of developing a telephone-based, integrated voice, data, and application communication system for businesses with just 10 to 100 telephones cannot use the tools and technology appropriate for a high end communication system. Techniques to solve this dilemma vary, but one solution is the object model decomposition technique. This technique calls for the system to be divided into "objects," each of which is responsible for a specific system capability. Examples of the highest level objects include the system's switching matrix, control subsystems, and signaling subsystem.

This process formally defines an object as a unique entity that receives a specifiable input, performs an operation, and generates an output to another object. Objects defined at the beginning of the process are then successively decomposed into the next level, or "moved to another level of abstraction." At each level, services and requirements common to the objects are pursued. These shared services and needs are gathered together to form the operating system software requirements.

In conjunction with explicit voice and data communication system requirements, this technique is instrumental in realizing an appropriate decomposition level to implement different communication system capabilities. For example, the decomposition process reveals that the basic path services required in a communication system (ie, making, monitoring, and breaking down paths) have the software form of an application, just as an electronic directory is an application.

This process can be implemented by the computer system designer for a variety of operating systems, including communication or process control computers. It also enables the operating system, rather than the hardware, to control expansion and upgrading. All this facilitates the speedy and efficient design of a variety of computer systems.

A new system that uses this technique to solve the voice and data handling communication problem is the Telenova 1 system, and its network operating system (TNOS). TNOS supports private branch exchange (PBX) features for easy telephony. In addition, it is compatible with the data generated by many computer types regardless of vendor, operating system, or size.

Gary L. Passon is software engineering manager at Telenova, Inc, 102-B Cooper Ct, Los Gatos, CA 95030, where he is responsible for software and architecture of the Telenova 1. Mr Passon previously worked for Digital Equipment Corp on the Ethernet program and for Telemed Corp on large system communication servers.

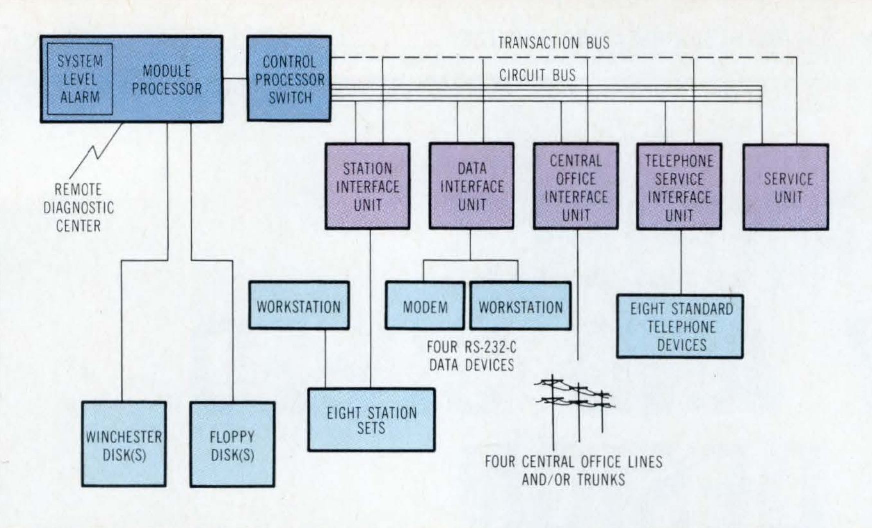

Fig 1 A Telenova I module includes a central processor, mass storage devices, and a control processor switch. It has 18 slots for a mix of interface units to connect to central office trunks, station instruments, and a variety of data generating and receiving devices.

Telenova I's development closely models the techniques used in operating system research, rather than classical communication system design methods. In the classic approach, switching hardware and software are the system's heart, and the operating system is designed to support these switching requirements. In contrast, the object model decomposition approach presupposes that all system requirements can be analyzed in the beginning of the design and that all common design elements can be isolated at each design step.

The benefits of the message-passing software in TNOS are typical of object model decomposition-based design. It also helps determine common communication system needs that the operating system could solve. These needs make this operating system process interface different from previous operating systems. For example, formal support of both channel addressing (do function x on channel y) and transaction addressing (do function x, number z, and signal when finished) are capabilities available at the process interface.

Critical to the system's development is an architectural design that accommodates all of the system's anticipated functions and degrees of freedom. The technique used to generate this design involves four steps. These include agreeing on the model of the connecting devices, selecting the future growth paths or degrees of freedom, establishing maintainability, availability and reliability goals (eg, wait no more than 150 ms for a dial tone), and recursively decomposing the problem into finer and finer objects.

Also fundamental to the design process is a set of "what technology is available" decisions. These set a time frame and cost goals for system design. For example, one major decision stemming from this time frame consideration is the splitting of realtime control and responsiveness into intelligent interface units, separate from the communication system's resource control and database manipulation processor. Another decision reflects that the software "mechanisms" for system operation should be in the interface units (eg, looping back a data stream), and the software "policy" should be in the module processor (eg, go loop back).

The Telenova I system consists of a module that contains a digital backbone, interface units, a module processor subsystem, a storage subsystem, and a power supply subsystem (Fig 1). A wide range of specialized interface units can be attached to the digital time division multiplexed backbone. Each of these interface units is an intelligent, distributed partner in system operation. Note that voice is converted from analog to digital form in a station set with a display and keyboard using industry standard mulaw codecs to permit the entire switching unit to operate digitally.

Software problems

For both the voice and the data handling capabilities of the classic PBX-like communication system, the communication software developers' freedom is limited. Typically, developers selected a realtime operating system model. In this design, only a limited priority system can be set up, and it is usually run from a master interrupt. Moreover, system processes are created and given a priority level when the system is initially designed. When an interrupt occurs, the interrupt handler calls the appropriate process and it begins to run. Each process is designed to be complete in a very short time, or to "call" a process at a much lower priority level for additional processing.

In general, all processes in these systems share memory and communicate via globally known memory locations. This design is efficient in terms of needed computer power and memory space. But, it is difficult to maintain or enhance. Most voice and data handling PBXs are a variation of this theme.

Once the requirements for a network operating system are generated by the object model decomposition technique, it is important to examine how the operating system meets classical (necessary) operating system criteria. The most important question is the processor/memory/communication schedule trade-off. However, these trade-offs are not well-known at the early design stage. Therefore, at least one of them (eg, memory) must be thought of as fairly flexible.

There are also considerations of system throughput, response time, and availability. Throughput can be considered a measure of transactions per unit time, and is a function of both the hardware and the software system design. In TNOS, constraints are defined for the number of messages per second that can be delivered to applications, and for the scheduling overhead. This is a typical design approach for computer-controlled communications.

Once the demands of classical operating systems are met, a model process studies process communication.

To meet these and other design goals, critical system constraints must be defined. These include the number of processes to be managed, the priority distribution, and the runtime requirements. These decisions affect the operating system's database size and scheduling algorithm. They also allow rough computation of the overall system response time for a set of operations.

Along with its system services, an operating system must address itself to resource management issues like fairness and protection. The primary resources managed by the operating system are buffers (quantity, size, by what process, and number per process) and messages (number outstanding on a specific port of a process).

Often, processes need to communicate with each other. This is possible by passing values on a shared stack, sharing data bases, or message passing. Selection of the process communication mechanism affects the "cost" of communications between cooperating processes and the ease of moving the processes to different machines. In this system, message passing is used for flexibility. There is also an optional buffer that is "given" away to the message receiver.

The message-passing structure does not require the process developer to know the internal structure of other processes. In addition, it also allows the hardware design to implement a memory protection mechanism, and facilitates network communication by hiding the real location of other processes that may later be housed in other modules. Thus, the message-passing structure facilitates process development.

Execution order

As described earlier, object model decomposition generates a set of objects, each object a separate abstraction with its own input operations and outputs. Consequently, the order of operation execution is determinate between any two objects. However, since many object sets are managed concurrently, a mechanism is required to give priority to different processes servicing sets of objects. Normally, a priority structure contains the processes and is evaluated after every message transmission. A timeslicing schedule driven by a hardware clock interrupt is also used.

As might be expected, some form of protection from inadvertent destruction of code, state, or data is necessary since multiple processes share resources. Many voice and data communication systems do not feature hardware protection; this makes resolution of some system faults difficult or impossible to accomplish. In a highly reliable communication system, nothing short of a hardware protection scheme is appropriate. Therefore, processes are protected by a set of hardware registers associated with each process's mapping registers. This system causes an immediate trap whenever a process attempts to access beyond its allowable address range.

Finally, in any operating system, some method of synchronization between processes must be supported. In shared memory systems these are sometimes called monitors/locks. TNOS supports synchronization by allowing a process to perform a blocking read on a specific port when it requires a message. This means posting a read for a specific message to arrive on a specific input port, and dismissing until it arrives (or a timer goes off).

Model processes

Once the demands of classical operating systems are met, a model process is selected to study how processes communicate among themselves. The operating system supplies an environment for the rapid development and efficient execution of processes that closely follow the model. In fact, its interface allows the solution of many problem classes. These include single object per process, multiple object per process, hierarchical object addressing to two levels, hierarchical function addressing to two levels, and channel orientation addressing. Processes communicate via a protocol that is given a unique number and revision level to allow elements of the system to evolve in a controlled manner, and to supply a first level dispatching method. The model process and environment has six major components: the static build region, runtime support, context region, execution region, data region, and message structure (Fig 2).

The static build parameters form a set of information given to the communication system and a generation process to define the initialization specifics. These include the process name, resource requirements, and runtime limits. For its part, the runtime support package supplies a set of system services, group libraries, and system libraries, as well as resource requirements and limits that can be dynamically set. The system services include a timer that

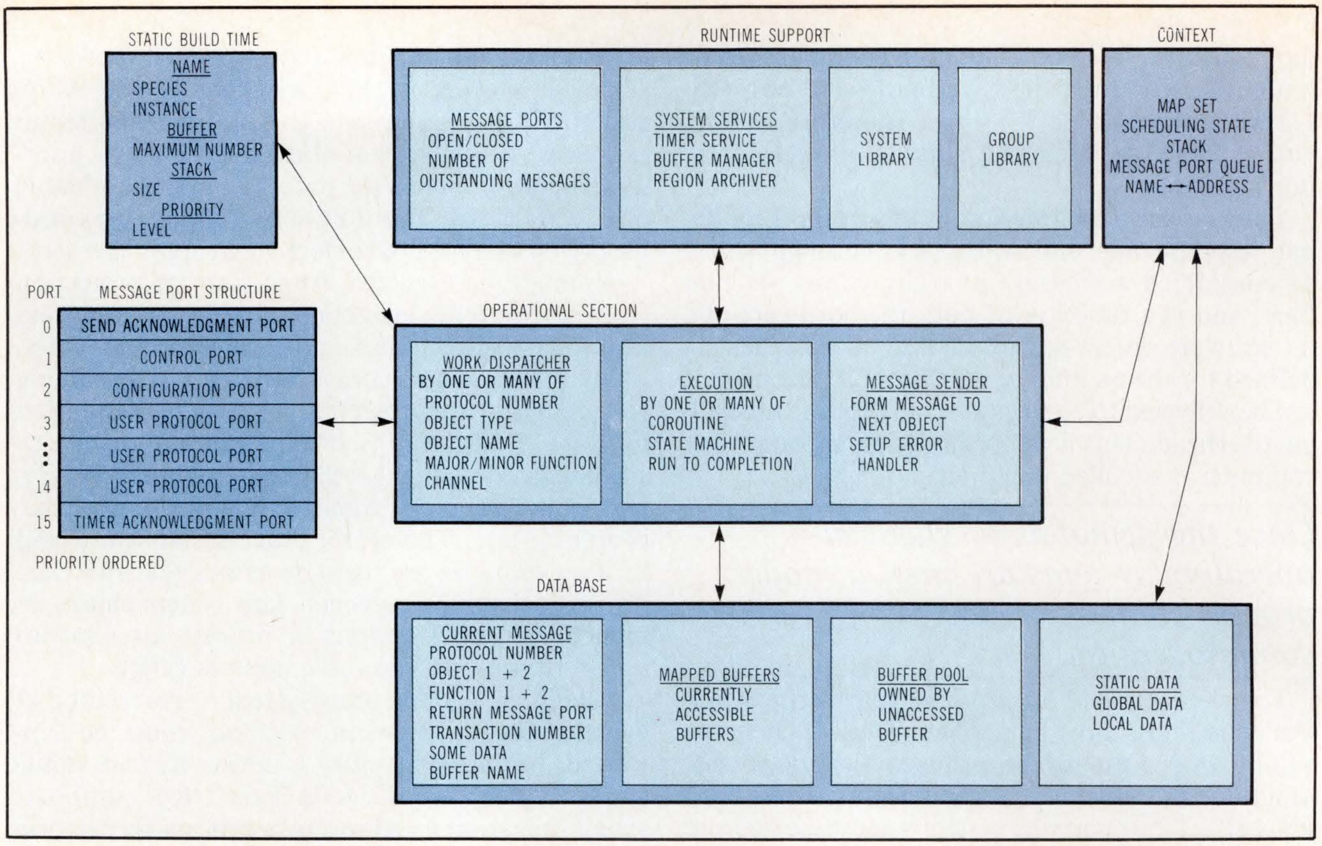

Fig 2 The network operating system's (TNOS) model process environment has the six parts shown. These help the computer system designer determine the best method of communication between the operating system software process and the operating system kernel.

can send a process-defined message to the process at an appointed or relative time, and a region archiving service that can store and retrieve regions by name on a rotating storage device.

The context region contains the per process information TNOS requires to properly manage the process and to protect it from inadvertent damage. Each context block is evaluated on a scheduling cycle to determine the appropriateness of allowing a process to execute.

The operational section contains a message dispatcher, execution, and message sender. The message dispatcher is coded to fit the developer's model of how the work is to be managed or scheduled inside the process. This allows for development of an internal per process operating system that fits a specific need or processing model.

The execution section performs the object database manipulations, and determines if additional processing is required from outside this process. From here, the message sender section, which packages a response to the caller and/or a message to another object (process) in the correct form and sends it out, is called. Then the process loops to the message dispatcher and sets up to get the next message.

The database section contains all the data base required to operate the process. Because code and data are separated, code segments can be shared between multiple installations of a specific process. The model process manipulates four kinds of data bases plus local variables stored on the stack. The process has the message protocol header available as it processes the incoming message. This data base is special because of its general usefulness throughout the execution of the process, and is globally available inside the process.

The mapped buffers are dynamically allocated buffers gotten by the process to keep a "per something" data base at startup or may have been passed to the process during a message receipt. Each process may "look" at up to two of these buffers at once. The rest of a process's dynamic buffers are kept in an unmapped state. This makes them owned, but not accessible, without an explicit "accessbuf" system operation. Finally, each process has a static data area in which global and static variables can be located and accessed.

The last component of the model is the message structure. This is a set of 16 message queues per process that have implicit and explicit definition. The system manages the message ports as queues in a priority manner. Thus, if one message is waiting on message port 3 and another on message port 5, the system will give the process the message on port 3 first. If another message arrives for port 3 before the next read of the message ports by the process, then the next read will return the newer message on port 3. The system uses message ports 0 and 15 for supplying acknowledgments as well as negative

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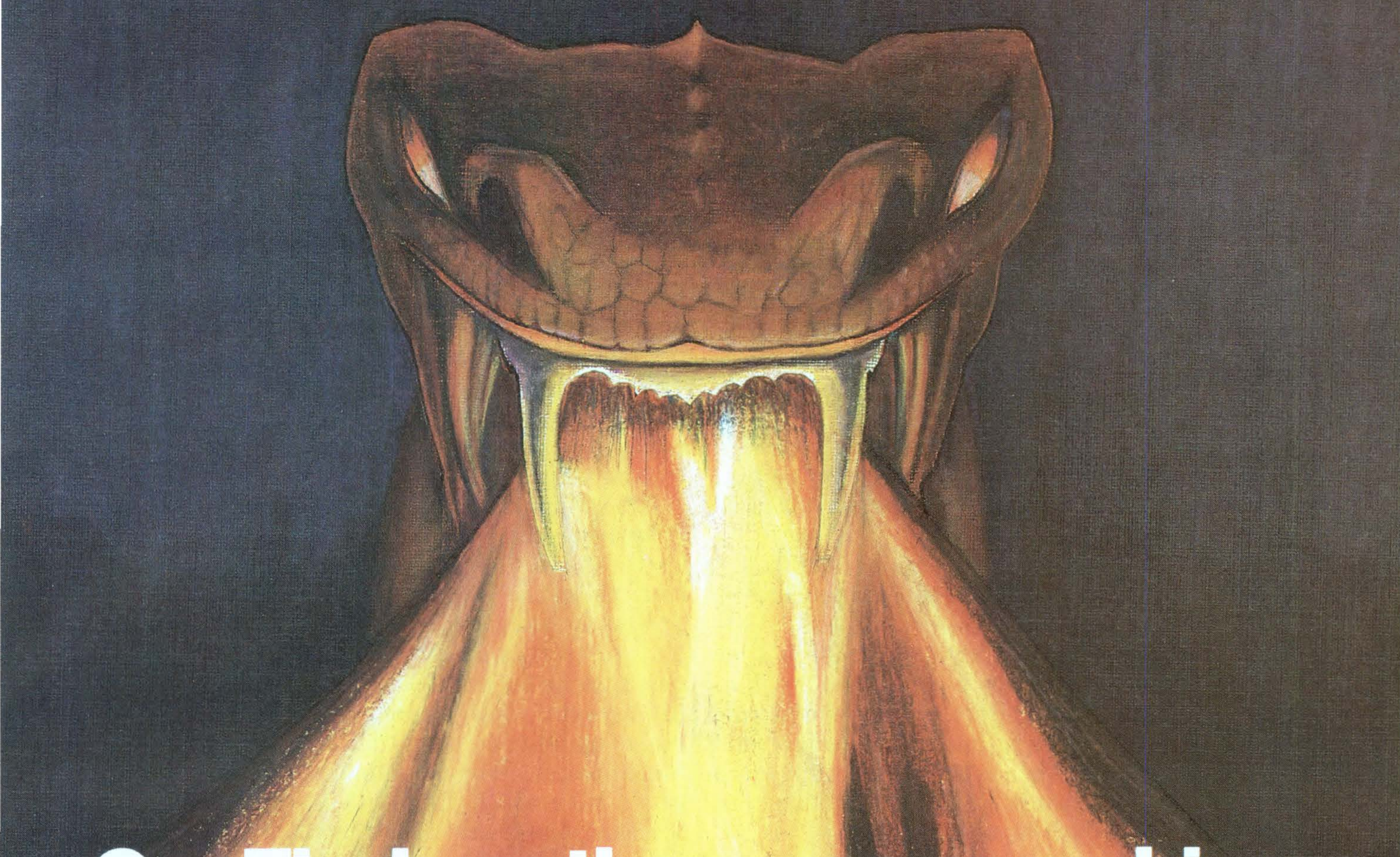

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acknowledgments for system services, and these are neither accessible nor controllable by the process. Ports 2 and 3 are used by the control and configuration subsystem to communicate to all processes in a like manner and to assure that its commands receive the highest priority.

An example is useful in explaining how the TNOS environment supports operation, control and error-handling. The example process is called the user interface process and is responsible for the syntactic and limited semantic parsing of commands for the application set. It also masks the applications from device idiosyncracies. It is a multichannel process, handles multiple protocols, and uses an interpreter with loadable scripts to isolate the application-specific command sequences from the user interface environment. At system initialization time, the process is created and awaits configuration.

The configuration system determines both hardware and software availability and then proceeds to inform the applications and user interface of the system resources they are to know about. This is done by means of a configuration protocol and is sent to a "configuration" message port. At any time during the operation of the system, additional configuration messages may arrive that can perform functions such as install, activate, pause, continue, deactivate, or deinstall on an object or object set.

Once the user interface has some resources, it begins to communicate with the applications via application-specific protocols and with the appropriate drivers via driver-specific protocols. These messages are sent to the message port as specified by the protocol, but responses are returned to the message port of choice as specified by the user interface. A voice or data connection, or some kind of asynchronous event soon occurs and a work sequence is started. This will cause a message or a set of messages to start traveling through the system. Each of the messages updates data bases, causes more messages, or has the user's display updated until the transaction requested has been supplied. The user interface is only one of many processes but it is typical in that it uses many of the available TNOS interfaces.

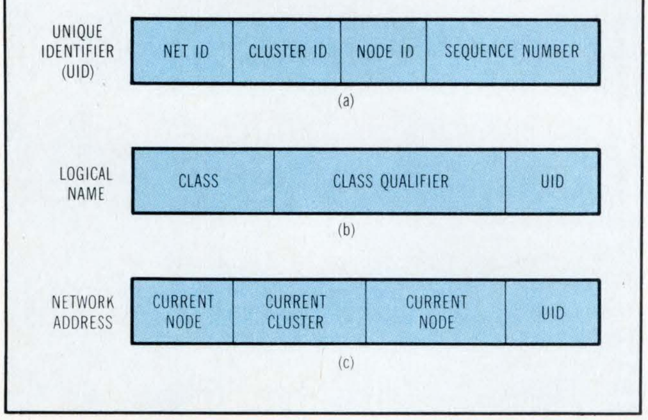

Fig 3 Network operating system processes have specific name and address formats. The unique identifier (UID) in (a) is included in both the logical name (b), and the network address (c). It is 48-bits long, guaranteed to be unique, and is assigned at process creation time.

Everyone needs a name...

One fundamental attribute of a network operating system is the need to resolve both the process-naming and the name-to-address translation issues. TNOS's naming convention makes processing location-independent and provides two levels of names—file servers, local and remote. The flexible naming system provides enhanced fault tolerance by letting processes request what they need instead of to whom they wish to communicate.

In TNOS, processes have a logical name, or system-unique indentifier (UID), and a network address. The TNOS UID is a 48-bit ID whose uniqueness is guaranteed across the entire network and is assigned at process creation time (Fig 3). Processes are not allowed to take advantage of the contents of the name, except the remote interprocess communication (IPC) system, which uses the name information as a hint to optimize the access time to locate the process. Since processes may not know the UID of other processes with which they wish to communicate, a mechanism of logical names and logical name translation is created.

The logical part of the name is assembled by the sending process by selecting a class, is typically a service of some type (eg, file or directory server), and a class qualifier (eg, local, offnode, all, named). A special class qualifier (named) allows a process to communicate with a specific process and uses the supplied UID as a communication handle. This approach allows very efficient addressing once two processes locate each other because no evaluation is necessary.

Network addresses are formed by concatenating the local UID to the current location of the process. This new, larger form is also guaranteed to be unique and absolute. Network addresses are moved through the network on a need-to-know basis by a group of processes called Name-to-Address Mappers.

...and a common language

With TNOS, processes can find each other by logical or real name. But, it is also helpful to specify a standard message format. Such specification allows a process to represent a number of objects or channels and receive different protocols for each, all the while knowing that, at least at the most basic level, the message format is similar.

Fig 4 illustrates the standard message format including the User Protocol Block (UPB). Processes are required to abide by all the fields of the standard message format, by the protocol number field, and the response port field of the UPB. Remaining

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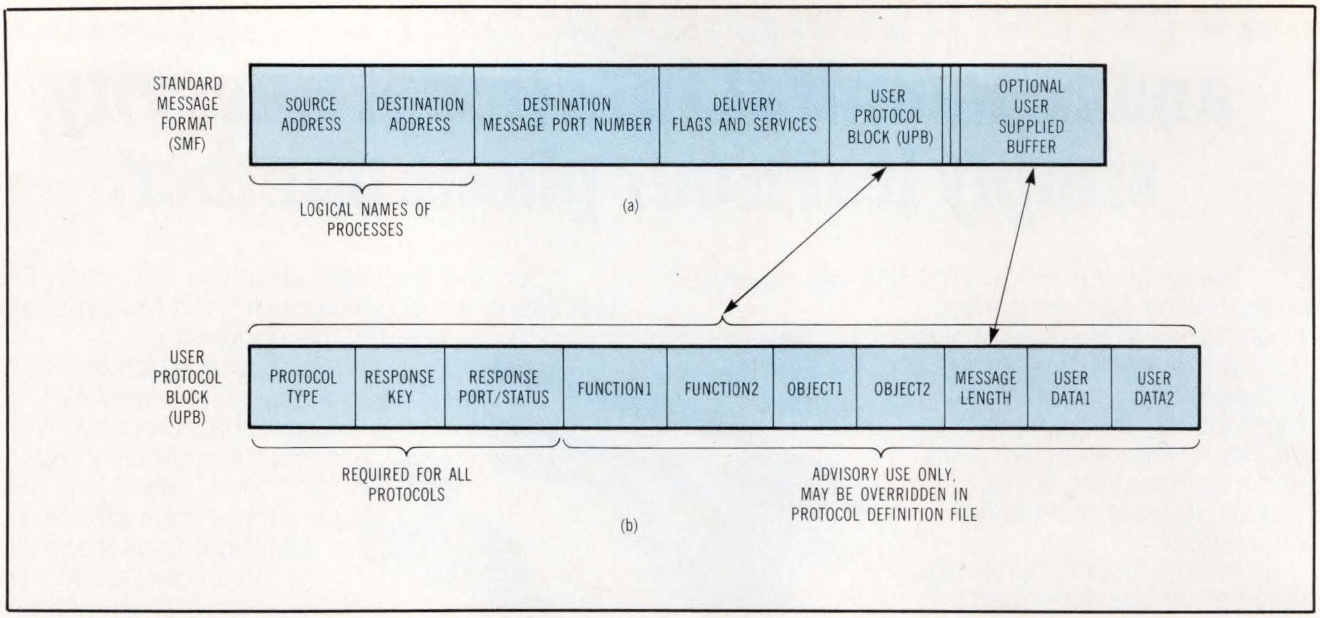

Fig 4 The TNOS standard message format (SMF) in (a) includes the user protocol block (UPB) in (b). Part of the UPB is optional and may be suppressed by the particular protocol in use. Similarly, there is an optional user-supplied buffer in the standard message format.

UPB fields are advisory and may be overridden by explicit definition in the appropriate protocol definition file. Each protocol has a protocol file called DOTPCL.

The Standard Message Format (SMF) has six fields: source address, destination address, destination message port, delivery flags and services, user protocol block, and optional user buffer. The user protocol block consists of 20 bytes, and contains fields for protocol type, response key, response port or response status, function1, function2, object1, object2, message length, userdata1, and userdata2.

The protocol type field indicates whether the data at hand is a command or a response, and the protocol number. The response key is a transaction code that returns with the response to assist the caller in locating the original request. Response port is also used by the process in returning the response; in this case it is the destination message port. The function and object words are used for dispatching and are generally protocol-dependent. Message length tells the receiver the length of the message in the buffer. Note that the buffer is optional and most protocols do not send one. Finally, the user data words are a mini-buffer for sending data between processes.

Real environment

The Telenova 1 is built of a large collection of processes which follow the guidelines discussed earlier. Fig 5 shows its software architecture decomposition. The most fundamental element is the kernel. It is very small and contains the message passing software, a basic resource control and hardware-dependent code. It is written in assembler for fastest performance. Kernel processes cover the classical ele-elements of operating system services. These include buffer management, process management, and swap management. Each of these processes has a special status because it can share memory with the kernel itself. System processes supply the higher level services, which are sent messages just like any standard application process, and receive no special treatment.

Drivers have a special place in the system because of their ability to interrupt handlers placed in their address space and to connect and disconnect from the interrupts. Drivers do not handle real interrupts. They are code segments that are executed after the system interrupt handler processes the "real" interrupt.

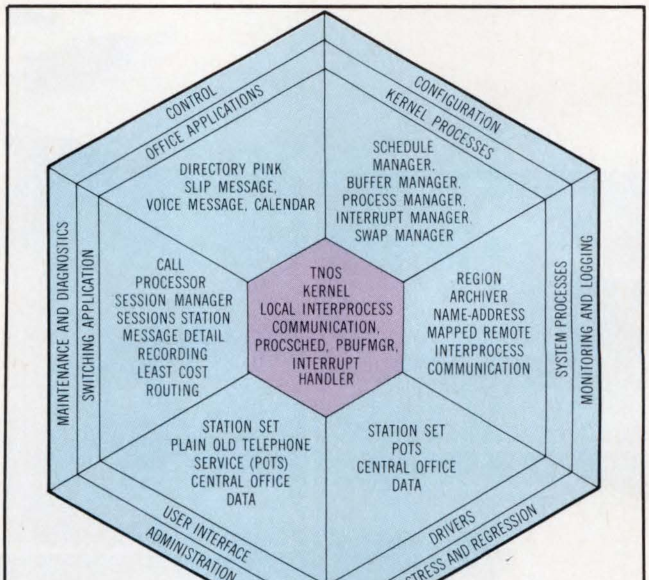

Fig 5 The operating system architecture is centered around its kernel, which is written in assembler, and performs classic kernel functions. Higher level processes communicate by message passing; no special software treatment is needed.

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User interface modules are the device-independent portion of the system. They are interpreter-based, multichannel processes that perform the syntactic and some semantic processing of the user requests for service. Finally, the system contains a significant set of applications. These are grouped into two sets: those that pertain to switching and those that pertain to office productivity.

It is important to understand that TNOS supports the development, test and integration of software and hardware in a unique manner. It is designed to allow the developer to take the object decomposition output and implement processes without changing its basic form. The advantage is less development time.

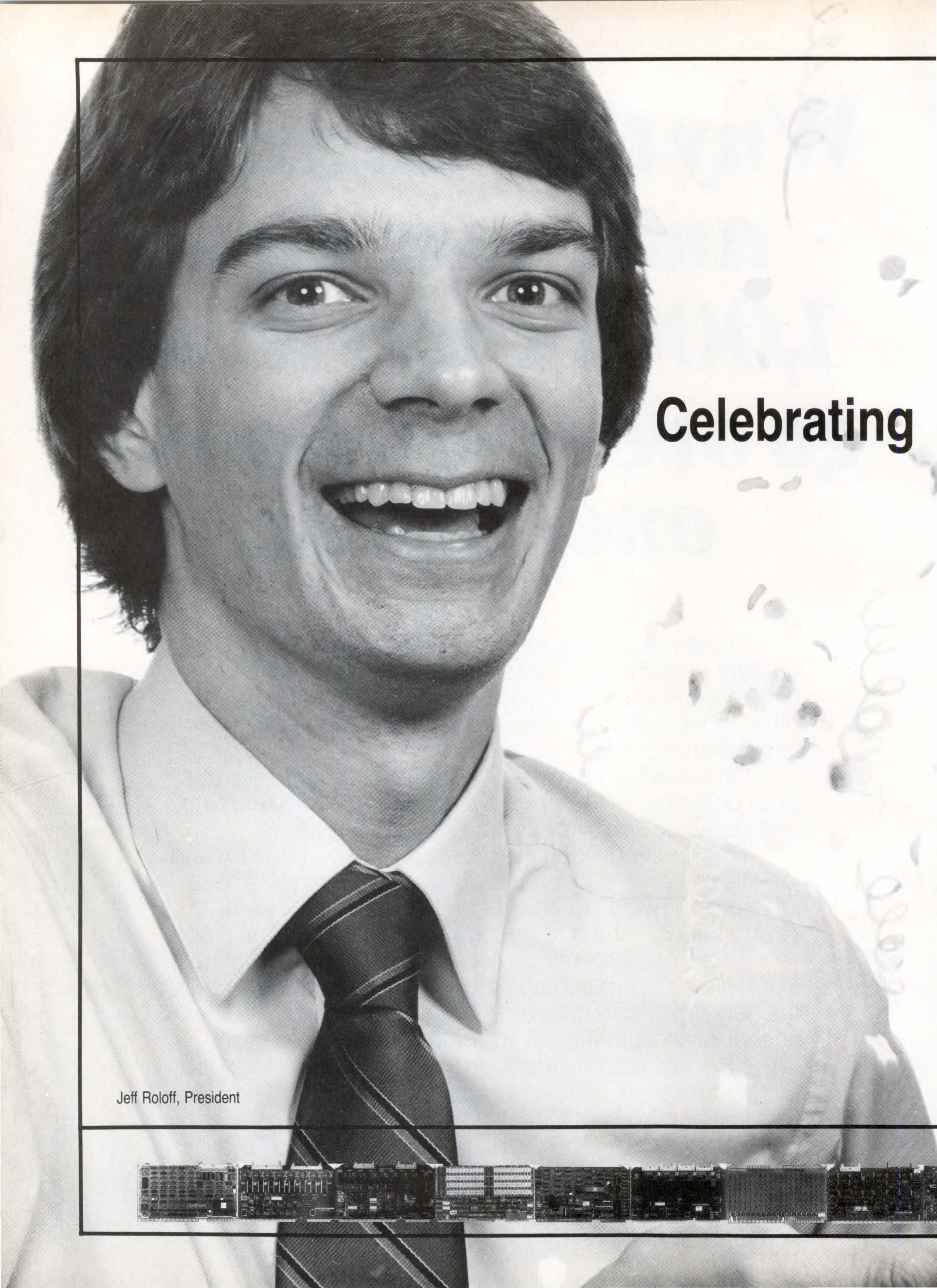
The development process is broken into five segments and consists of the conception stage as described above, specification state, development and unit test, integration, and monitoring logging. In the specification stage, the process or subsystem is specified by an internal specification, which is the developer's guide book, and a protocol document with external interface and operation descriptions. The protocol document or DOTPCL file, is a controlled document. Its standard form documents the specific use of the standard message form as implemented by TNOS and the executing process.

During development and unit test, TNOS also plays an important role. First as a host environment, processes can be brought into a subset runable system and use the runtime resources as if they were in a complete system. Processes that do not yet exist are simulated by "message generators" which impersonate the other pieces that are still under development. Taking the notion of machine-independent operating systems literally, TNOS not only runs on the Telenova 1 module processor, but also on the IBM PC. This feature allows each developer to test design independently and conveniently.

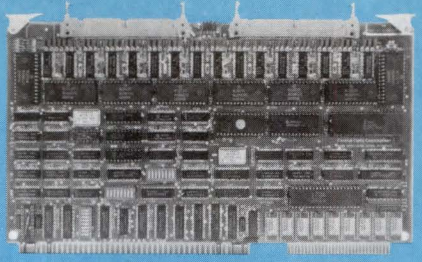
The design integration phase is always one of the trickiest phases in any project; TNOS can assist here as well. At integration time, processes run with protection turned on, and developers have access to a debugger. Finally, this system has a common logger and monitoring subsystem that allows ongoing event tracking.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 734 *Average 735* *Low 736*



Jeff Roloff, President



Multibus High Performance Terminal Controller
- Greater than 9600 baud-full duplex on all 8 channels
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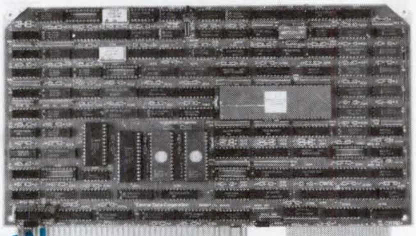
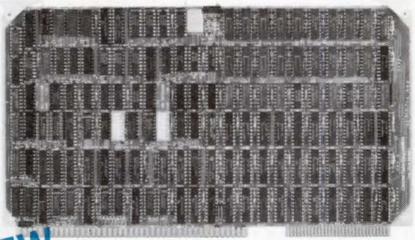
- Byte and word transfers to 64K on-board RAM with parity
- Bus vectored and non-vectored interrupts
- Intel 8088 processor running at 8 MHz
- RS-232C with all modem control signals

NEW **15-Slot iLBX Backplane**
- Parallel priority resolution capability
- Full Faraday shielding on all P1 data lines
- iLBX capability using 64 conductor ribbon cable & 96 pin din connector
- All 24 address lines bussed the full 15-slot length
- 4 layer PCB, internal +5V and ground layers

NEW High Performance Multibus* Boards



NEW **Multibus 12.5 MHz 68000 CPU**
- Primary master iLBX* interface
- 68010 virtual memory CPU with SUN memory management
- 64K bootstrap/monitor PROM sockets
- 8 Mbyte Multibus address space



NEW **Multibus iLBX Cache Memory**
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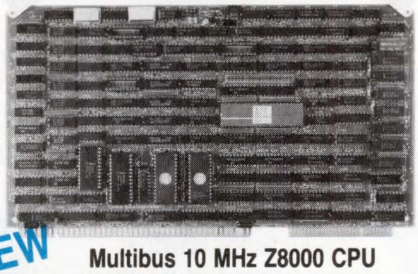
- Extensive error checking and testing



NEW **Multibus 10 MHz Z8000 CPU**
- Primary master iLBX interface
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- 32K bookstrap/monitor PROM sockets
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- Controls 4 Standard 5¼″ Winchester disks, 4 5¼″ Floppys, 4 QIC-02 Cartridge tapes
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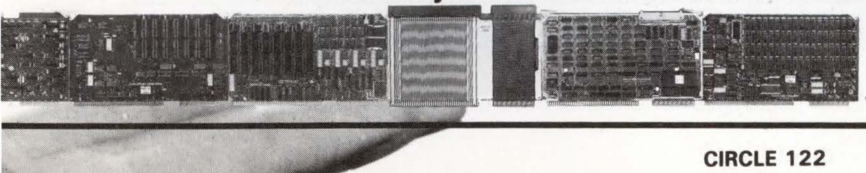

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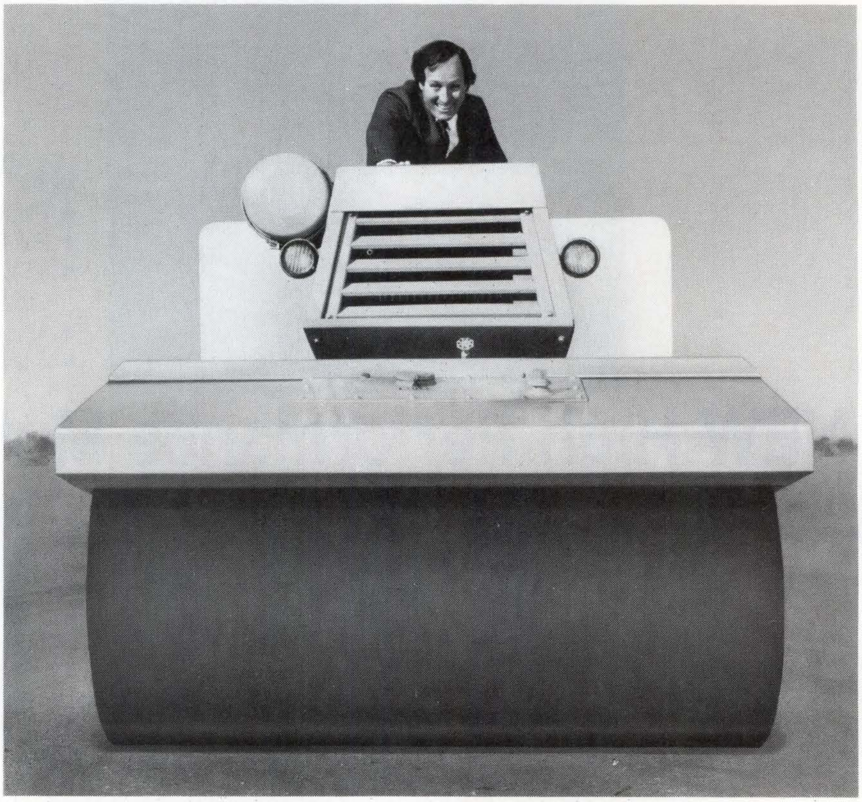
CIRCLE 122

Data Translation flattens the competition! STD Bus analog input boards – just $195.*

Fred Molinari, President



We're on a roll.

Introducing a low-cost data acquisition board specifically designed for the industrial control marketplace. The DT2712, with 32 analog inputs, 10-bit A/D resolution and signal conditioning options. The capabilities you really need, on the bus you've always asked for, at a price you can hardly believe.

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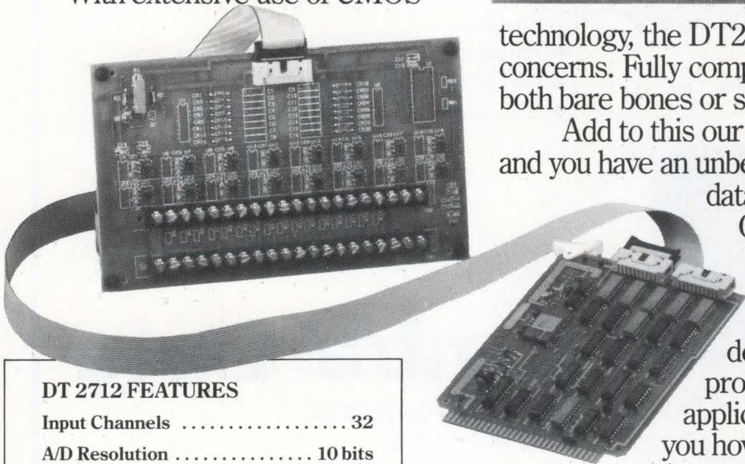
The DT2712 gives you all the resolution, speed and input ranges you need for industrial applications like data logging, process control and plant automation.

With extensive use of CMOS technology, the DT2712 design reduces power, heat and packaging concerns. Fully compatible with *all* STD Bus processors, it's ideal for both bare bones or sophisticated systems.



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DT 2712 FEATURES

Input Channels	32
A/D Resolution	10 bits
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World Headquarters: Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951 646.
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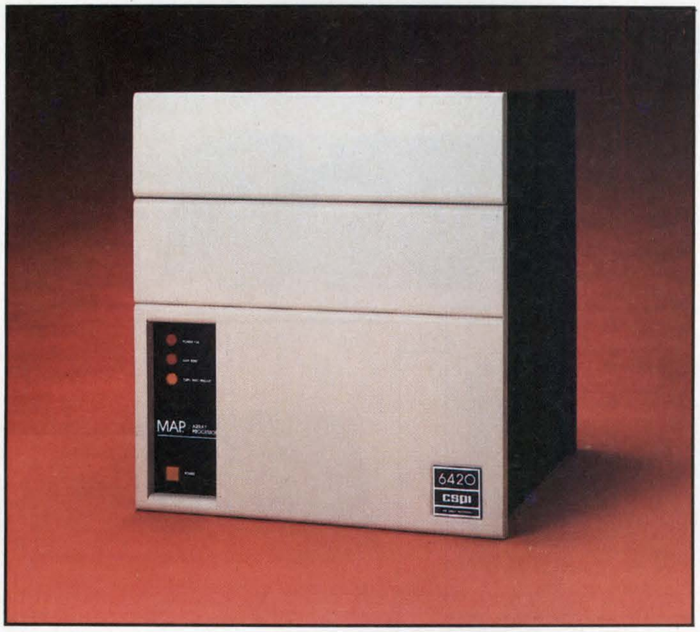
*OEM Quantities



Array processor executes fast Fortran via compiler

When interfaced to a host, the MAP-6420, provides a programmable peripheral that can off-load, from the host, numerical algorithms—executing them several times faster than the host. Software development is Fortran based with highly efficient compiler-generated code and full integration into the host Fortran environment.

An independent control processor and separate system and data memory buses provide internal control capabilities that cause no interference with the processor's numerical computations. Data memory is expandable to 64 Mbytes, and for additional storage, disk subsystems can be used. Address space reaches 1 Gbyte for future memory configurations.

Central to the development software on the processor is the MAP Fortran compiler that supports the user's development application libraries. Working together, the machine's architecture and the compiler provide fast, efficient execution of Fortran programs. Parallel units perform integer operations, memory references, and floating point operations in the program while both components optimize their concurrent operation. This approach is in contrast to other array processors whose pipelined architecture handles vector operations and exhibits poor performance unless the program is specifically optimized for the compiler.

All I/O, control, or communication between the host Fortran program and the 6420 is carried out with commands, declarations, statements, and calls—all familiar to the Fortran programmer. This software system, integrated into the host environment, allows the development or conversion of scientific programs and packages to fully exploit both processor and host power.

Parallel execution of arithmetic, I/O, and system control through the use of multiple processors and memory systems allows efficient concurrent operation and high performance. The memory system consists of two independent memory buses, a 32-bit system bus, and a 64-bit data bus. Therefore, system control activities on the system bus do not degrade concurrent numerical computations on the data bus. In addition, the memories are not interleaved, so memory access time is consistently fast and not dependent on address patterns.

The system bus has anywhere from 256 Kbytes to 2 Mbytes of system memory, which stores the SNAP-III operating system, control information, and large user programs. This bus is also used for all interprocessor communication. The data bus contains 4 to 64 Mbytes of data memory for storing arrays, variables, and constants associated with an application program.

As the computational engine of the 6420, the arithmetic processor (AP) performs algorithms at speeds of up to 5 MFLOPS. The AP is made up of a 32-bit integer/addressing processor unit (IPU) and a 64-bit floating point processor (APU) operating in parallel. To generate addresses fast enough to keep the APU near peak capacity, the IPU was designed as the fastest unit with both an integer adder and multiplier. The IPU also has powerful indirect addressing for efficient handling of sparse matrices and other complex data structures.

Programs for the AP reside in the internal program memories of the IPU and APU. Memory capacity is approximately 2000 lines of Fortran. Larger programs can be split into smaller overlays stored in system memory. These overlays are then loaded into the AP program memories from the array processor as needed.

There are three categories of software for the processor: development software, system software, and maintenance utilities. The development software consists of compilers, utilities, and the Scientific Subroutine Library, which helps the user develop application programs primarily for the AP.

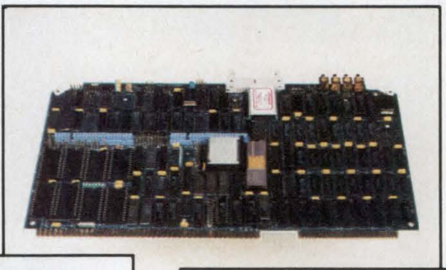
System software includes the MAP-resident SNAP-III operating system and a host-resident driver and library for software interfacing to the host Fortran run-time system. An installation and SYSGEN procedure as well as diagnostics constitute the maintenance utilities.

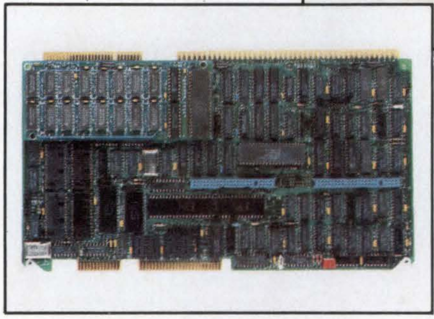
The basic configuration includes 4 Mbytes of data memory in a 21-in. rack-mountable chassis and is priced at $100,000. The first host interface available is for VAX computers running VMS. Shipments with up to 18 Mbytes of memory are scheduled for August. **CSP, Inc**, 40 Linnell Cir, Billerica, MA 01821.

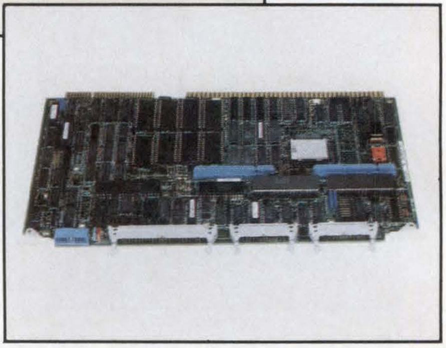
—M.B.

Circle 260

Single-board microcomputers integrate power and versatility of full computer systems







Three board-level computers, based on iAPX 186 and 86 microprocessors, provide such full-system capabilities as CPU, operating system functions, peripheral device interfaces, memory, and industry standard software. The iSBC 186/03, 186/78, and 86/35 combine these functions on single 6.75- x 12-in. Multibus PC boards. All run under the latest version of iRMX 86 operating system software.

Based on a 6-MHz, 16-bit CPU (the 80186), the iSBC 186/03 has eight (expandable to 12) 28-pin JEDEC universal memory sites, two I/O expansion connectors, interface for high speed memory expansion, and two programmable serial interfaces (one RS-232-C, the other RS-232-C or RS-422 compatible). It also has 24 programmable I/O lines, configurable as an ANSI small computer interface intelligent peripheral interconnect, as a Centronix parallel printer interface, or for general purpose I/O. This board contains six programmable timers and 27 levels of vectored interrupt control.

The second computer, the 86/35, is based on an 8086-2 CPU (16-bit with 5- or 8-MHz clock rate). It contains 512 Kbytes of dual-ported read/write memory (expandable to 1 Mbyte with the iSBC 314 512-Kbyte memory expansion Multimodule board), sockets for up to 128 Kbytes of JEDEC 24/28-pin standard memory devices, and two iSBX system expansion connectors. An optional iAPX numeric data processor is available. This computer also has 24 programmable I/O lines and three programmable 16-bit BCD or binary timers/event counters. Its nine levels of vectored interrupt control are expandable off-board to 65. A programmable synchronous/asychronous RS-232-C compatible serial interface offers software-selectable baud rates.

Video graphics subsystem 186/78, the third computer board, is also based on an 80186 CPU with 6-MHz clock. It includes an 82720 bit-mapped graphics display controller, and has a programmable 50- or 60-Hz frame rate. Display resolution is 1024 x 800 x 1 interlaced or 512 x 512 x 4 noninterlaced; drawing rate is 150 k pixels/s. Up to 16 colors can be displayed at one time, out of a 4096-color palette. One available graphics software interpreter, the iPLP 720, implements the NAPLPS standard; a second, the iVDI 720, is based on the ANSI proposal for virtual device interface. PROM capabilities of both interpreters provide standard graphics support for the iSBC 186/78, or for an iSBX 275 Multimodule board. The system interfaces to either monochrome or color raster-scan display monitors, has eight universal memory sites for local RAM or ROM store, and provides full RS-343 or RS-170 support.

Production units of both the iSBC 186/03 and 86/35 are now available at $1650 and $3495, respectively; engineering samples of the 186/78 sell for $3000. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051. —*S.F.S.*

Circle 261

Artificial intelligence language programs expert systems under VAX

Expert system design requires the use of an artificial intelligence language. OPS5, based on Carnegie-Mellon University's original AI language, takes advantage of the VAX/VMS system architecture by offering added capabilities.

To let the language be fully involved in the expert system design process, it is separated into individual parts. A changing model represents expert knowledge using rules in an if. . .then format. This dynamic "knowledge base" is also used to build and maintain the model. The third part of the AI language, the interference engine, has the responsibility of deciding which rules to execute for any given situation. Unlike AI languages that are Lisp based, OPS5 requires no garbage collection and will execute in real time. It is reimplemented in native mode on the VAX, yielding a program running 5 to 20 times faster than Lisp machines.

OPS5 applications can call and be called by software written in any language supporting the VAX calling standard. For example, a data collection routine written in another language can be called from OPS5, and the information incorporated into the AI model.

Targeted for companies with in-house AI departments and programmers with AI experience, the forward-chaining, rule-based language handles large production systems. Forward-chaining combines inputs from previous rule-based decisions and forms another version of the present model. Two different conflict resolution strategies are provided, so users can choose one that best meets their application.

Available through DEC's External Application Software Library, OPS5 is priced at $5000, with right to copy licenses at $3000. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754. —*M.B.*

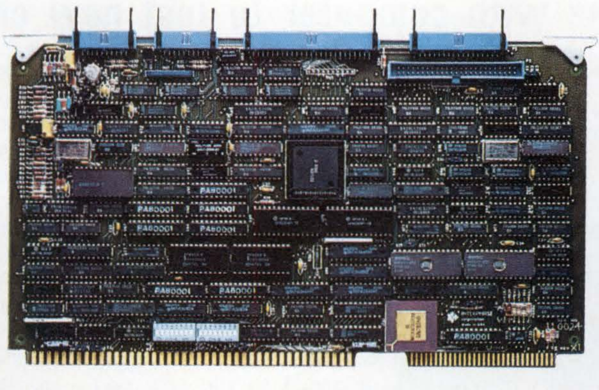
Circle 262

"With the Interphase Storager,™ I can make a 5¼" hard disk perform like an 8" disk."

Frank Emser
Manager Hardware Development
Paradyne Corporation

The Interphase Storager Multibus™ controller can give a 5¼" Winchester disk capabilities never before possible. Storager not only gets more performance from existing ST506 drives, but also supports the new ESDI and ST412HP interfaces for more power and capacity than ever before. And since Storager can control two Winchester disks, four ¼" tapes (QIC-02), and two 3½", 5¼" or 8" floppies, the same controller can be used for every storage need.

Storager features 1:1 interleave, with concurrent disk and tape transfers and simultaneous disk and bus transfers for speed and high performance. And Storager's unique "virtual buffer" architecture with UNIX™-optimized intelligent caching can reduce or eliminate disk rotational latency and overcome data overrun/underrun problems of FIFO-based controllers. Plus,



for the very first time on a controller, Storager has an *on-board* 68000 CPU.

The Storager controller is the latest product in Interphase's line of high-performance Multibus controllers. Interphase also offers Multibus controllers for SMD disks, local area networks and video monitors. Plus powerful disk controllers for the IBM® PC. They're all backed by a great customer support team that works full time with Interphase customers to assure that our products work the way they should — in the system.

Find out how Storager can make a 5¼" disk perform like an 8" disk. Call Interphase today at (214) 350-9000.

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CIRCLE 124

Node processor brings Ethernet high performance to VMEbus

As a frontend processor for Ethernet, ENP 10 provides VMEbus compatibility with Ethernet host to host transfer rates of 1.6 Mbits/s. Because the processor takes on communication responsibilities, the host is off-loaded for increased performance.

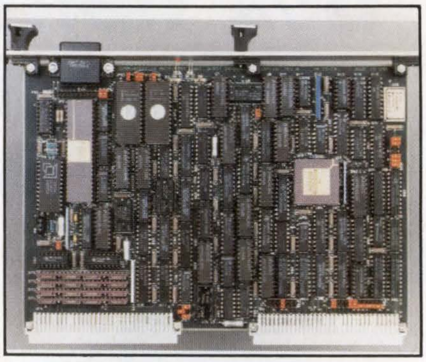
The node processor's main function is to free any VMEbus host from protocol burden by using a 10-MHz, MC68000 16-bit MPU. As part of the MPU, a communication executive performs supervisory functions over an Ethernet controller with closely coupled RAM and ROM, VMEbus interface to host, and a timer. This executive kernel provides initialization, transmit, receive, statistics, and timer functions. Layered around the kernel is a bus interface protocol, power-up diagnostics, and debugger.

The bus interface protocol provides control primitives for communication with the host operating system. The debugger aids upper level protocol development, displays and modifies memory and registers, and also permits multiple breakpoints.

In addition to the realtime kernel written for Ethernet, each unit in the series contains all levels of protocol software, including host I/O drivers for operating system networking. XNS and TCP/IP protocols are supported, together with development tools that allow custom networking capabilities and protocols.

As a single board, the ENP 10 appears as an I/O driver/handler to the operating system. This makes it easy to use and maintain. In addition, the board conforms to IEEE P802.3 (ISO) or Ethernet 2.0 specs for local area networks. Board resident elements of high level protocol can be ROM-based or down-loaded from host or network to RAM, permitting degrees of flexibility.

Features include 128-Kbyte dual-access RAM with parity and no wait states, 16 to 64 Kbytes of ROM, and VMEbus master and slave interface for host to ENP communications. In addition, a 2-ms timer



interrupts the MPU for protocol software timing. Physical specs include a double Eurocard form factor, operating temperatures of 5 to 50 °C, and power requirements of 4.4 A at 5 V, and 0.6 A at 12 V.

Board prices range from $1125 to $2500 in quantity. **Communication Machinery Corp**, 1421 State St, Santa Barbara, CA 93101. *—M.B.*

Circle 263

Logic analyzer teams with computer to test new chips

Engineers presently using VLSI design automation tools available on VAX computers can now test chip designs on the Tektronix DAS 9100 logic analysis system. The 91DVV VLSI verification software package from Tektronix creates a close relationship between the VAX host and logic analyzer. This combination implements chip testing more easily and at much lower cost than production testers.

Instrument cards in the DAS perform the tests, while the system interfaces to VAX running Unix. Within the DAS, a pattern generator card supplies the input stimuli. A data acquisition card captures the response outputs, which are then uploaded to the VAX and compared to reference data. Reference data can come from a simulation program, a good device, or the user. Comparison results can be formatted to graphically highlight discrepancies.

Test pattern vectors used by logic simulation programs (eg, Berkeley RNL or Sandia SALOGS) can be down-loaded to the DAS 9100 for use as a stimulation program. A program reformats the simulator test program to take advantage of the system's algorithmic pattern generation, and allows long sequential test patterns to fit into pattern generator memory. Interactive operation permits stimulus control and acquisition setups, tri-state control, and pattern to pin mapping.

The system runs under Unix 4.1 BSD, with the software composed of several modules that act as Unix shell commands. Test vectors and setup information are pipelined through the modules to conduct the test. The 91DVV software modules convert the test vectors into the DAS format and down-load them to the DAS pattern generators. The software exercises the device, collects responses, uploads to the VAX, compares responses to response predictions, and outputs the results. The package is $1000 and is available immediately. A typical DAS 9100 configuration for this application is about $40,000. **Tektronix, Inc**, PO Box 1700, Beaverton, OR 97077. *—J.B.*

Circle 264

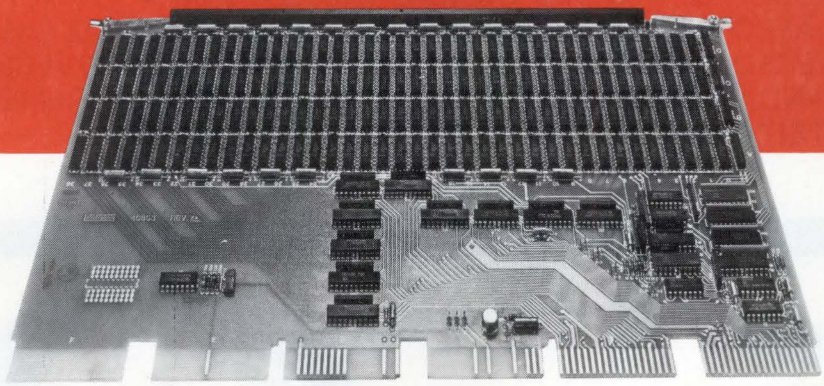
DEC®-COMPATIBLE SEMI ADD-INS

NEW!

1.0 MB VAX 730

1.0 MB VAX 750

2.0 MB VAX 780



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PDP-11	DR-114SP	hex	256 KB
PDP-11	DR-214	hex	1.0 MB
PDP-11	DR-144	hex	256 KB
PDP-11	DR-244	hex	1.0 MB
VAX®-11/750 PDP-11/70	DR-175	hex	256 KB
VAX-11/750 VAX-11/730	DR-275	hex	1.0 MB
VAX-11/780	DR-178	extended hex	512 KB
VAX-11/780	DR-278	extended hex	2.0 MB
DECSYSTEM 2020®	DR-120	extended hex	256 KB

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Dataram also provides core ADD-INs, core and semiconductor ADD-ONs, memory system units, memory management, and a wide range of memory-related accessories for DEC users.

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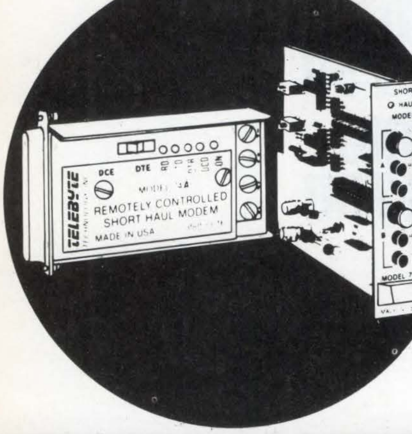
CIRCLE 125

LOCAL-AREA NETWORK PRODUCTS



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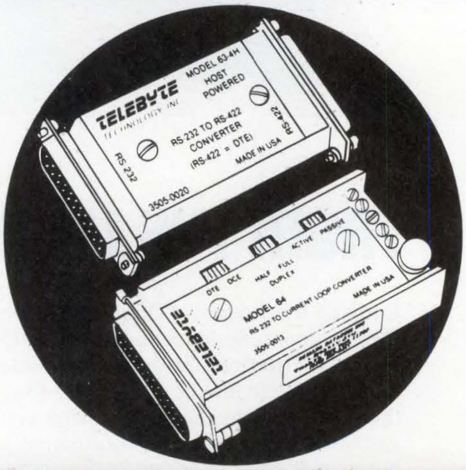

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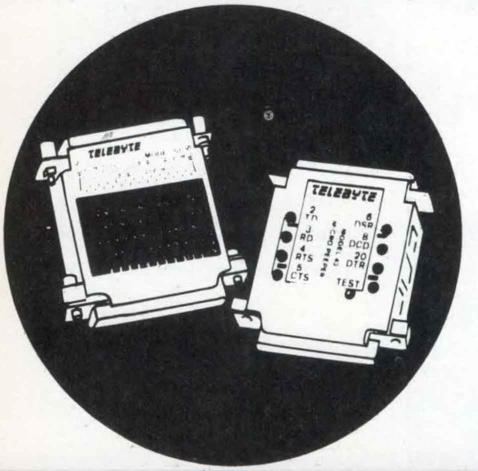

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CIRCLE 126

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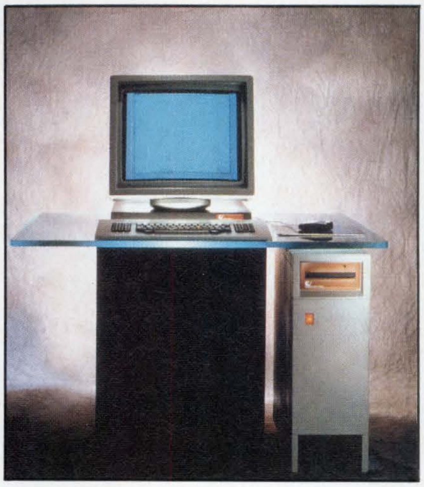
Workstations act as single-user solution to CAE/CAD/CAM applications

The CDS 3000 series of intelligent 32-bit workstations handles schematic capture, two-dimensional drafting and dimensioning, and technical publications—all in a single-user, desktop package. Nongraphics applications include spreadsheet generation, word processing, and electronic mail.

Based on the 68010, the 3000 employs virtual memory Unix enhanced for CAE/CAM/CAD applications. Supported programming languages include Fortran 77, C, and Pascal, as well as standard utilities.

All series workstations incorporate CADDS Access, enabling a user to log on to an existing CDS 4000 or 5000 series system. Connections are point to point, or via a modem. This connection permits access, display, and manipulation of CADDS 4X commands, files, and data bases. CADDS 4X, the latest version of the company's multi-user, multitasking software, provides the basis for an integrated graphics data base. Processing, retrieval, and storage take place on the host system, ensuring file and database integrity.



The systems communicate with each other, with other CDS systems, and with mainframes through industry standard protocols. With a shared resource manager and Ethernet software, the workstations can be clustered in multi-user networks and linked to central peripherals.

Though available in several configurations, all include as standard the 68010 with 2 Mbytes of main memory, Unix, a Multibus chassis, and graphics unit. The graphics unit provides a high resolution (900 x 1152 pixels), 19-in. monochrome display and controller, low profile keyboard, and mouse. Optional features include additional memory, an FPU, peripheral units, and communication links.

Several application packages are available to complement current CAE/CAD/CAM capabilities now on the system. Schematic Capture/3000 produces logical block diagrams and electrical schematics, as well as permitting online design rule checking. An optional logic design simulation package is available.

The Drafting/3000 software gives high productivity in layout design, detailing, and dimensioning. It uses dual English and metric dimensioning, standard parts libraries, and a graphics programming language.

Prices for the workstations range from $35,000 to $52,000. **Computervision Corp**, 100 Crosby Dr, Bedford, MA 01730. —*M.B.*

Circle 265

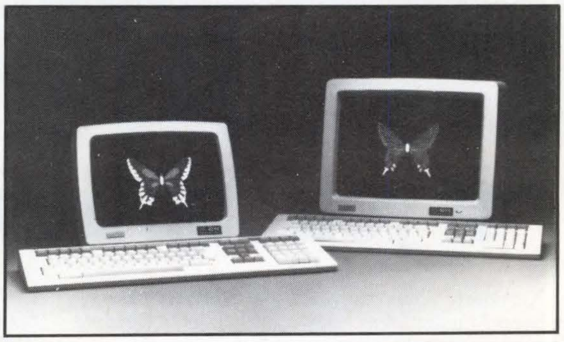
Color and monochrome terminals race with megapixel graphing speed

HiScan Graphics terminals apply high speed CMOS to low cost graphics displays. Based on dual-processor architecture, the terminals include a proprietary graphics coprocessor, and HiScan Graphics technology. This technology provides a faster graphing speed and more industry standard terminal emulations than comparably priced terminals. The 4210 is based on DEC's VR201 monitor and a VT200 keyboard; the VR241 color monitor and the same keyboard make up the 4205 terminal. All are compatible with DEC and other peripherals.

Image quality considerations are fundamental to terminals. In both terminals, image quality is increased with a high line rate noninterlaced display that is nonsmearing and flicker free. To further enhance image quality, the monochrome display offers an 800- x 600-pixel resolution—the color monitor provides 800 x 300 pixels. The terminals support 80- and 132-col formats with characters formed on a 10 x 20 cell.

By incorporating multiple bit-mapped memory planes, the monochrome terminals offer a four-level gray scale (using two memory planes). With four memory planes, the color terminals can simultaneously display 16 colors out of a 64-color palette.

Integrated architecture uses the bit map to display both text and graphics. Text features include a plain language setup menu displayed in English, French, or German. Also included are downloadable character fonts, and 15 programmable function keys.



Support is provided for TEK 4027 or 4105, DEC ReGIS protocols, as well as standard DEC VT220 text, and TEK 4010/4014 graphics functionalities.

To achieve graphing speeds of 1 million pixels/s, the terminals use a specially designed graphics coprocessor that works with a Z8002 16-bit microprocessor. The coprocessor handles all graphics processing tasks while general purpose calculations are delegated to the Z8002.

The graphics processor consists of three main elements—one for graphics processing, one for read-modify-write, and a CRT controller. These elements, together with the Z8002 in a pipeline architecture, are responsible for the megapixel rate.

The monochrome terminals are priced at $2195 each, while the color terminals will be $2995 each. **Digital Engineering, Inc**, 630 Bercut Dr, Sacramento, CA 95814. —*M.B.*

Circle 266

If you still believe in me, save me.

For nearly a hundred years, the Statue of Liberty has been America's most powerful symbol of freedom and hope. Today the corrosive action of almost a century of weather and salt air has eaten away at the iron framework; etched holes in the copper exterior.

On Ellis Island, where the ancestors of nearly half of all Americans first stepped onto American soil, the Immigration Center is now a hollow ruin.

Inspiring plans have been developed to restore the Statue and to create on Ellis Island a permanent museum celebrating the ethnic diversity of this country of immigrants. But unless restoration is begun now, these two landmarks in our nation's heritage could be closed at the very time America is celebrating their hundredth anniversaries. The 230 million dollars needed to carry out the work is needed now.

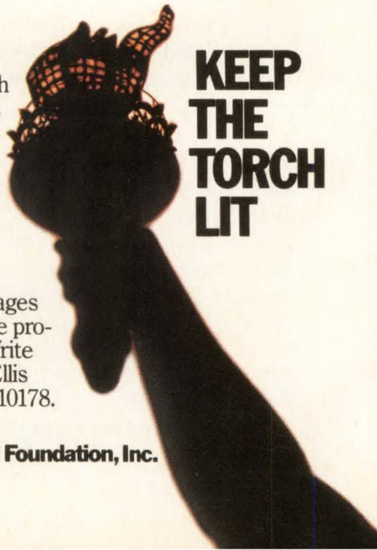
All of the money must come from private donations; the federal government is not raising the funds. This is consistent with the Statue's origins. The French people paid for its creation themselves. And America's businesses spearheaded the public contributions that were needed for its construction and for the pedestal.

The torch of liberty is everyone's to cherish. Could we hold up our heads as Americans if we allowed the time to come when she can no longer hold up hers?

Opportunities for Your Company.

OFFICIAL SPONSOR LIBERTY

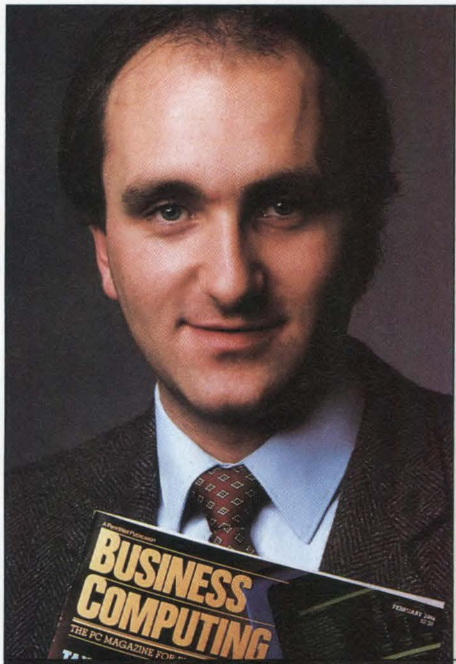
You are invited to learn more about the advantages of corporate sponsorship during the nationwide promotions surrounding the restoration project. Write on your letterhead to: The Statue of Liberty-Ellis Island Foundation, Inc., 101 Park Ave, N.Y., N.Y. 10178.



KEEP THE TORCH LIT

Save these monuments. Send your personal tax deductible donation to: P.O. Box 1986, New York, N.Y. 10018. **The Statue of Liberty-Ellis Island Foundation, Inc.**

"We couldn't manage without Business Computing."



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Rolf Grueniger
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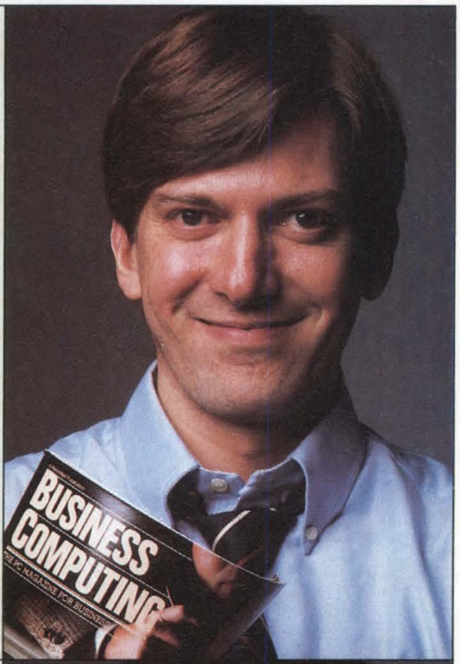

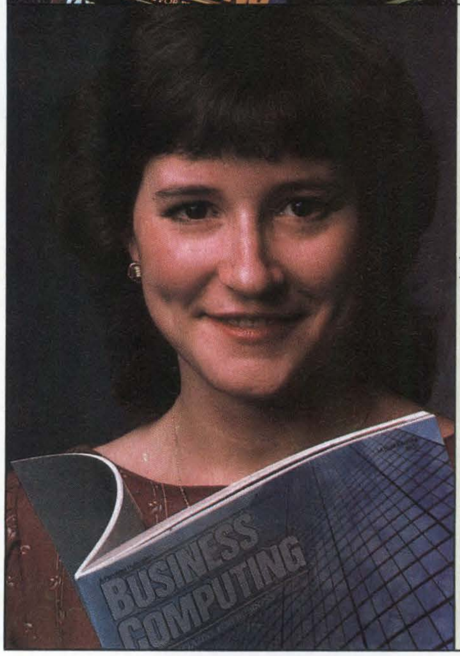

"Saved me hours of research on spread-sheet software."

Karen Leahy
PRODUCTION MANAGEMENT ASSOCIATE
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"Thanks for the sound advice on word processing."

Jim Hill
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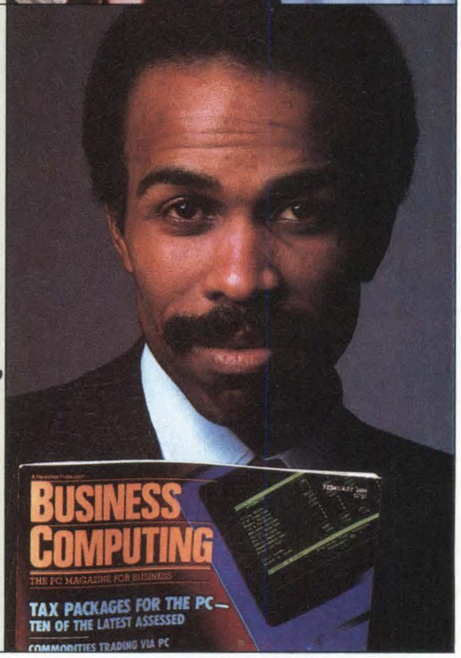

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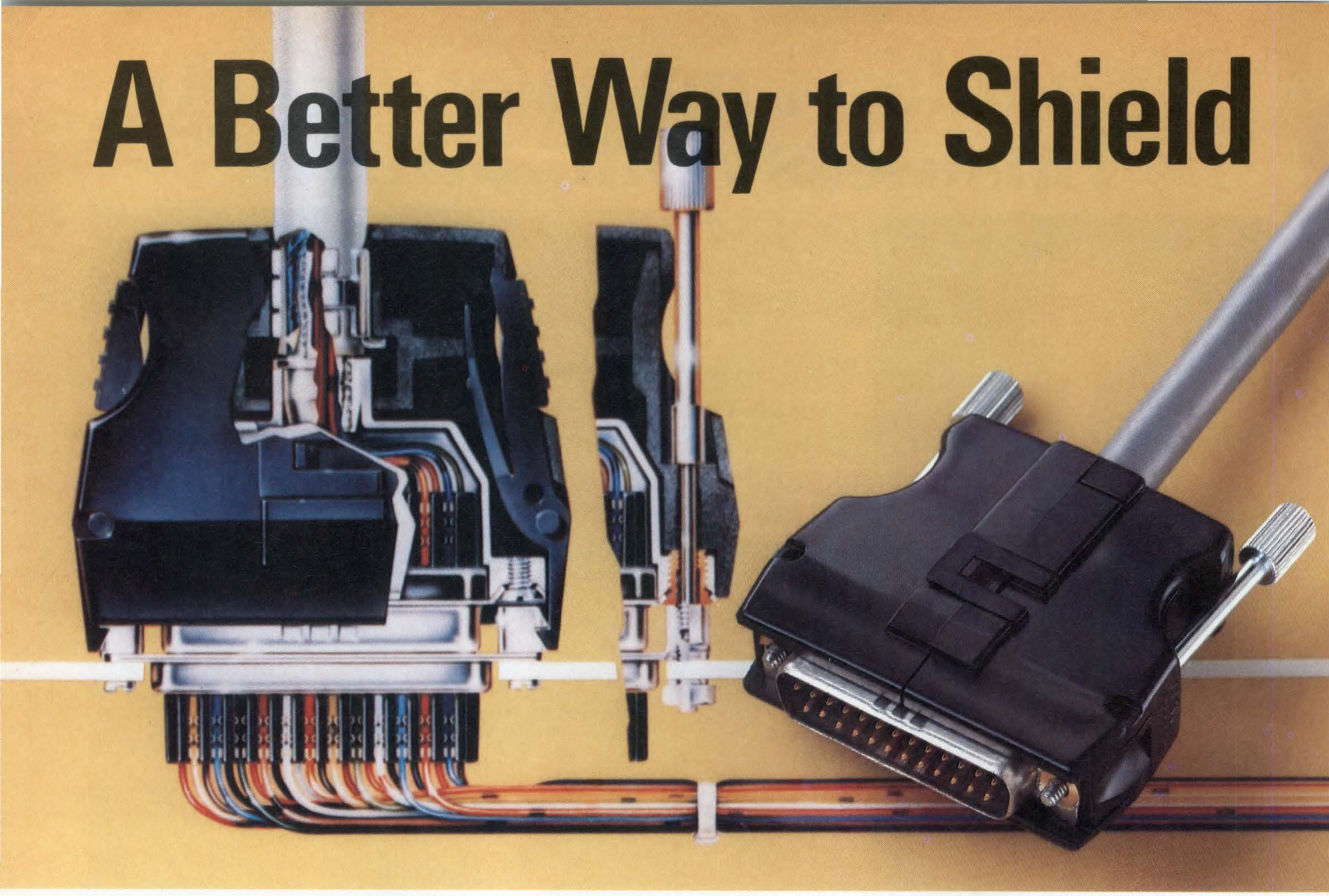
CIRCLE 161

A Better Way to Shield



TRW Shielded SUPER D* connectors... the D-subminiatures that meet new EMI/RFI shielding requirements.

FACT: FCC Docket 20780 now requires effective EMI/RFI shielding in electronic equipment.

FACT: EMI/RFI signals can escape through even the tightest seams.

FACT: TRW closes EMI/RFI escape hatches with a one-piece, seamless, die cast shield.

*Trademark TRW Inc.

FACT: Most shielded connectors are difficult—or impossible—to field terminate. TRW Shielded SUPER D connectors are designed *specifically* for ease of field termination.

FACT: Solderless termination and rapid assembly provides the most reliable means to attach the connector to a foil shield.

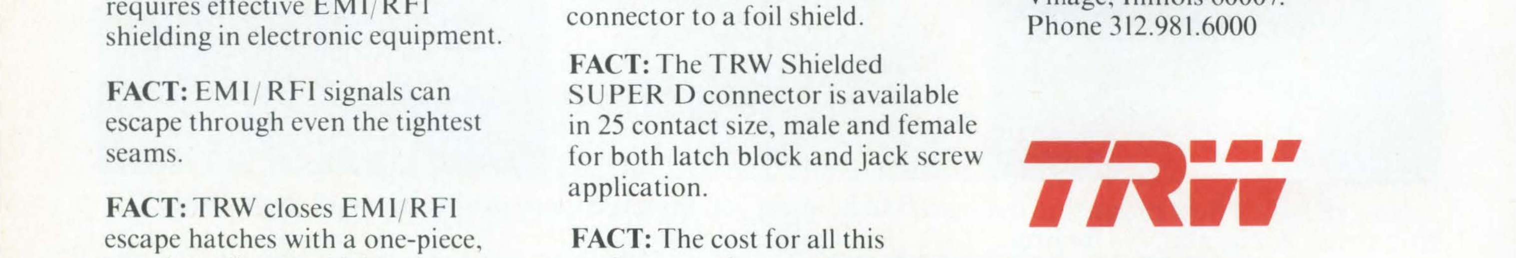
FACT: The TRW Shielded SUPER D connector is available in 25 contact size, male and female for both latch block and jack screw application.

FACT: The cost for all this performance is remarkably low.

FACT: A free sample of the TRW Shielded SUPER D connector is yours for the asking. Call your TRW Electronic Components Group Sales Representative and judge all the facts for yourself. Or contact: Connector Division, TRW Electronic Components Group, 1501 Morse Avenue, Elk Grove Village, Illinois 60007. Phone 312.981.6000

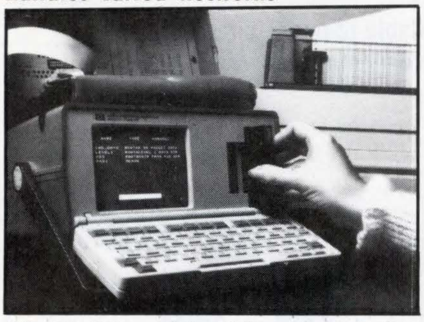
TRW

Connector Division
TRW Electronic Components Group



CIRCLE 128

Compact protocol analyzer handles varied networks



The HP 4951A weighs 14 lb and meets data comm network installation and maintenance needs. This protocol analyzer simulates a CPU, terminal, or group of terminals so a network can be tested without shutdown. Unit supports X.25, BSC, HDLC, SDLC, and user-definable character asynchronous and synchronous protocols. Data codes include ASCII and EBCD, among others. Error checking is performed on CRC-CCITT, LRC and parity, as well as CRC-6, -12 and -16. Basic HP 4951A costs $3595. **Hewlett-Packard,** 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 267**

Interconnection of terminal to host occurs via transparent gateway

The XP-GTY Gateway uses remote communication facilities to link local area cable installations and provides fully transparent routing. It has complete terminal frontend processing for VAX/VMS computers and terminal switching to any computer using local and remote communication links. VAX/VMS terminal functions are implemented in a small distributed cluster controller. The interface at the VAX is via a single intelligent board. The system sells for $5800. **Xyplex, Inc,** 100 Domino Dr, Concord, MA 01742.
Circle 268

Processor gains 3270 communication capabilities

The MME/RHO (Multiple Access Facility with Remote Host Option) extends SNA and BSC 3270 communication capabilities to non-IBM hosts. Intended for use with Comten 3600 communication processor systems, the MAF/RHO supports link-attached BSC 3271 or 3274 cluster controllers, providing internetwork communications without host modification. Initial license fee is $3218, with a continuing monthly fee of $585. **NCR Comten, Inc,** 2700 Snelling Ave N, St Paul, MN 55113.
Circle 269

Double wide card gives plug-in modem full-duplex operation

Taking advantage of the IEEE P959 (Intel SBX) port, the 8400 modem provides a programmable Bell 103/CCITT V.21 operation at 300 baud. Bell 202/CCITT V.23 half-duplex operation is at 1200 baud. The SBX port allows communication additions to new or existing Multibus equipment or VMEbus designs. The card contains a USART and a programmable baud rate generator as well as interface circuitry to support auto-dial/auto-answer operation when used with 8183-type approved data access arrangement. Price is $430. **ETI Micro,** 6918 Sierra Ct, Dublin, CA 94568.
Circle 270

Communication system matches voice, data, and management features

System 75 incorporates simultaneous voice/data communication over a single line via the digital communication protocol. Transmissions occur at up to 64 kbits/s. The 16-bit micro in the system's control complex runs under a realtime Unix-derived operating system. Advanced 256-Kbit RAMs make up the 2-Mbyte system memory. Remote and local diagnostics and maintenance can be performed even at switch failure. **AT&T Information Systems,** 100 Southgate Pkwy, Morristown, NJ 07960.
Circle 271

Concentrator passes data with different media and protocols

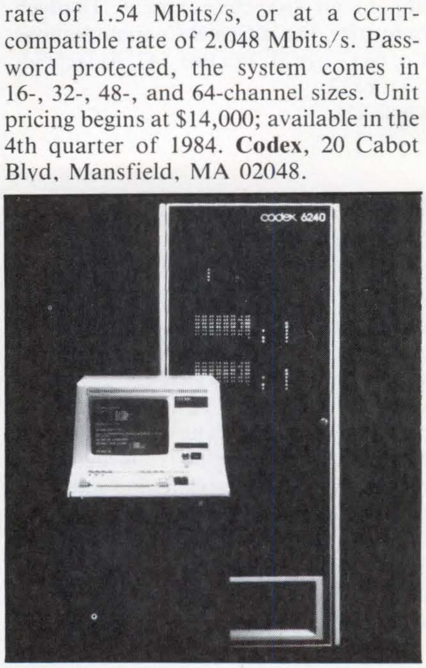
The multipoint Elite One switches between multiple dissimilar processors and terminals. It supports all traditional networking transmission media, including both analog and digital lines to 72 kbits. Data is transmitted and managed over continuous bidirectional transmission paths that are independent of transmission media, attached devices, and their protocols. A single switching node accommodates up to 32 user ports with either asynchronous or synchronous transmission rates. Prices start at $4500 for an eight-port unit. **Doelz Networks, Inc,** 18581 Teller Ave, Irvine, CA 92715.
Circle 272

Single-chip digital bell-ringer chimes in

This tone-ringer circuit replaces the conventional telephone bell with a single chip. The MC 34017, with three base frequency options, generates a warbling square wave output drive to a piezo sound element. Tone ringer provides an onchip diode bridge. Output voltage is 37 V_{pp}. Unit price in 100 to 999 quantities is $1.24. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.
Circle 273

Multiplexer combines high volume voice, data, and image traffic

A time-division multiplexer, the 6240 can integrate voice, data, and compressed images for transmission on one link. It can handle up to 64 data or voice channels and permits reconfiguration from a central site. The 6240 operates at the T1/DS1 (domestic telephony standard) rate of 1.54 Mbits/s, or at a CCITT-compatible rate of 2.048 Mbits/s. Password protected, the system comes in 16-, 32-, 48-, and 64-channel sizes. Unit pricing begins at $14,000; available in the 4th quarter of 1984. **Codex,** 20 Cabot Blvd, Mansfield, MA 02048.



Circle 274

Fiber optic/coax interconnect aims at ARCnet machines

A 3100 plug-in fiber optic/coax interconnect device delivers fiber optic capabilities to ARCnet local area networks (LANs) of Datapoint Corp and others. Requiring no change in the LAN operating software, the 3100 offers transmission benefits of fiber optic media at a data rate of 2.5 Mbits/s. Transmissions can travel 4000 ft without repeaters. This 3-port active hub supports two active coaxial ports and one fiber optic port. Six devices can attach to a 3100 by means of passive hubs. Units are less than $200 in quantity. **Raycom Systems, Inc**, 6395 Gunpark Dr, Boulder, CO 80301.
Circle 275

Portable network analyzer runs data comm software

A package for SDLC/HDLC analysis gives the user a window to network activities. With this program, the analyzer checks line use, frame types, link stats, and error stats. User specified triggers measure times and quantities, while reports can be displayed on a CRT, or printer, or saved on disk. The program works in the same way for binary synchronous control networks. An SNA monitor allows one disk to monitor, capture, and display information in an SNA environment. **Digitech Industries, Inc, a Centel Communications Co,** 66 Grove St, PO Box 547, Ridgefield, CT 06877.
Circle 276

Modem filter features onchip equalizers

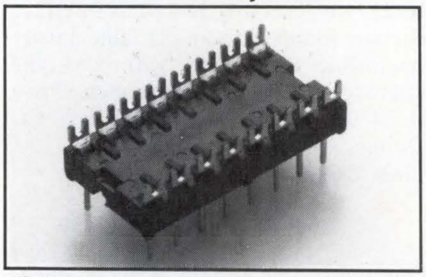
Monolithic S35212 includes onchip originate/answer mode selection logic thereby eliminating the need for external circuitry. Two uncommitted op amps provide antialiasing, smoothing, and gain-control functions. The continuous low pass filter for smoothing can be switched between a call progress tone detection mode and a data transmission mode. It can be operated at multiple clock frequencies of 153.6 kHz, 1.228 MHz, and 2.304 MHz. The 24-pin device is available at $16 per 100 pieces. **American Microsystems, Inc,** 3800 Homestead Rd, Santa Clara, CA 95051.
Circle 277

SYSTEM ELEMENTS

Op amp features low current noise and low voltage drift

Dielectric isolation (DI) with onchip guarding obtains low bias current for OPA111 DIFET operational amplifiers. On the OPA111 version, maximum input bias current is ± 1 pA, average offset voltage drift is $\pm 1\ \mu V/°C$, and rms noise is $1\ \mu V$. Designed for precision input specifications and reduced susceptibility to flicker noise, the amp is priced from $6.35 in 100s. **Burr-Brown, Analog Div**, PO Box 11400, Tucson, AZ 85734. **Circle 278**

Component carrier mounts end-to-end and side-by-side

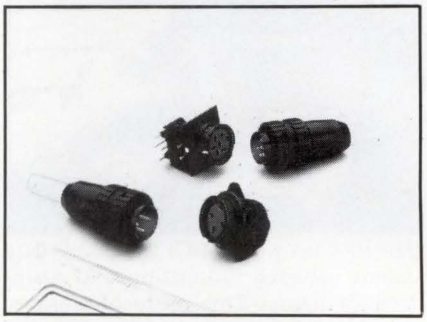


High temperature component carriers in the 1100 series feature end-to-end and side-by-side insulator mounting. A thermoplastic insulator, rated at 260 °C for 10 s, is molded into a mechanical configuration to allow this variable mounting. Precision stamped and formed terminals are plated with a choice of platings. Available in stock sizes or 14, 16, 18, 22, 24, 28, 36, and 40 terminal devices. The cost for the component carrier is $0.029 per terminal in a 5000-piece quantity. **Augat Inc**, 33 Perry Ave, PO Box 779, Attleboro, MA 02703. **Circle 279**

Damaged cables gain snap-on protection

Cracked, corroded, cut-through cables can be restored with Snaptube protective wrapping. Made from Teflon®, the wrapping permits snaplock around damaged insulation. Snaptube features resistance to heat of up to 260 °C, and can withstand highly corrosive chemicals. This flexible insulator offers resistance to shock, abrasion, and moisture, while exhibiting marked dielectric properties. **Zeus Industrial Products, Inc**, PO Box 298, Raritan, NJ 08869. **Circle 280**

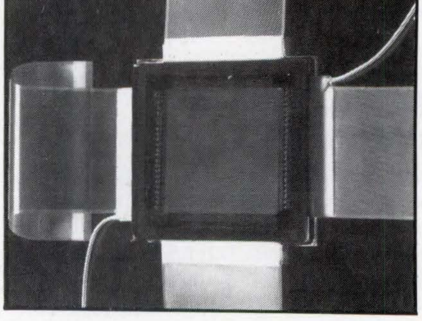
Cable-to-panel circular connectors are offered



Miniature circular connectors in the 703-91T series are available with three to seven contacts. A right angle PC mount receptacle for direct soldering to a circuit board is available with 3, 5, or 6 contacts. For shielded applications, basic models are metal with 1 to 14 contacts. Screw, friction, and bayonet locking styles, and either solder or crimp termination are offered. Current ratings for the 703-91T series are 3 A per contact; voltage is rated at 120 V. **Amphenol Products**, 2122 York Rd, Oak Brook, IL 60521.
Circle 281

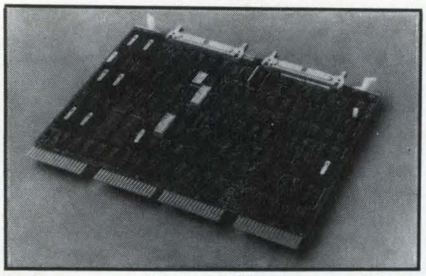
Vacuum fluorescent display achieves flat-panel dot matrix

Graphic and alphanumeric capabilities are possible in this vacuum fluorescent flat-panel display. The standard, dot-matrix GH-256X256 comes with flat ribbon cables for PC board interconnection. Dot pitch measures 0.3175 mm (center-to-center). Sample quantities are available from stock at $315 each, with volume discounts available. **MH & W International Corp**, 14 Leighton Place, Mahwah, NJ 07430.



Circle 282

Tape coupler connects GCRs to PDP-11s and VAX-11s



Industry-standard half-inch tape drives link to PDP-11 and VAX-11 systems via the TC13 tape coupler. This quad size PC board emulates DEC's TS11 tape system and embeds on any Unibus backplane. It has a 3.5-Kbyte buffer that permits operation at any density and tape speed, with density selections made at the tape drive. TC13 data rates reach 781 kbytes/s. Coupler handles conventional start/stop and streaming drives, along with 6250 bits/in. GCR (group code recording tape drives). The TC13 lists for $2000. **Emulex Corp,** PO Box 6725, 3545 Harbor Blvd, Costa Mesa, CA 92626.
Circle 283

Universal floppy controller is compatible with the EXORbus

The 9671 is a peripheral controller specifically designed for compatibility with the MC68/B09E microprocessor bus. As an intelligent subsystem, it uses a local MC68B09E to perform controller tasks normally done by the host processor. The subsystem controls up to four diskette drives of intermixed sizes with one- or two-sided head configurations, and FM or MFM encoding. Price is $595. **Creative Micro Systems,** 3822 Cerritos Ave, Los Alamitos, CA 90720.
Circle 284

Ethernet network controller connects to PDP-11 and VAX systems

Compatible with the IEEE 802.3 and TCP/IP protocols, the Easyway/ET consists of two modules—a host protocol processor and a communication adapter board. The host module has the Unibus interface, data line interface, and TCP/IP protocols. The adapter board provides the data-link and physical layer protocol to the Ethernet network. Software device drivers are provided for the VMS and RSX operating systems. The price, including driver, is $7200. **Able Computer,** 1732 Reynolds Ave, Irvine, CA 92714. **Circle 285**

Intelligent controllers interface with Companion tape drives

Controllers in the M1200 Companion Controller series offer SCSI interface compatibility. The controller line handles up to four Companion tape drives, reading or writing data at speeds of 192 kbits/s to 900 kbits/s. A 20-Mbyte tape can be backed up in 4 min. Two 1200 series models are presently offered; the M1200, which is housed on a 8- x 11-in. (20.3- x 27.9-cm) board; and the M1201, which receives a 5- x 8-in. (12.7- x 20.3-cm) housing. Unit prices start at $225. **Memtec,** Keewaydin Dr, Salem, NH 03079.
Circle 286

At last! Powerful solutions for identifying and eliminating datacomm and network problems.

With HP's family of protocol analyzers, you can minimize network downtime and handle even the thorniest of datacomm problems. Choose from the standard HP 4955A, or our newest member, the powerful HP 4951A, weighing in at only 14 pounds. They set new standards of performance for R&D and field service personnel involved in solving datacommunications problems, and end-users responsible for network maintenance and planning.

The HP 4951A/4955A team—your key for high-powered datacomm testing.

Here's high analytic power and productivity. The HP 4955A and HP 4951A are fully program-compatible. You can develop test programs on an HP 4955A and then transfer them to your field service personnel via a modem or tape cartridge. With the HP 4951A/4955A protocol analyzer team, you can now go wherever your datacommunications problems take you and have the confidence of on-site versatility, with back-up power just a phone call away.

HP 4955A—increase your capability with top performance features.

With the HP 4955A you can bring your products to market faster, and with a greater level of reliability than ever before. Our datacomm-enhanced BASIC lets you program sophisticated test routines and perform high-level protocol analysis. Exercise your hardware and software as it's being developed, not after it's installed. Monitor, simulate, and trigger from 50 bps to 72 kbps. You can easily identify protocol problems at the physical interface, frame, and packet levels using the HP 4955A's multiple display formats. Plus, our intelligent 256K byte buffer memory increases real data storage by eliminating line idles without sacrificing timing information.

HP 4951A—"instant" productivity.

The HP 4951A features advanced one-button autoconfiguration which easily does the setup work for you and gets you monitoring data quickly on-line. Like the HP 4955A, it gives you 63 simultaneously active triggers for extensive testing. In post-processing mode, you can do detailed repetitive analysis for hard-to-track errors. You can trap on characters, error conditions and lead transitions. To isolate problems down to the network component level, BERT mode lets you measure bit errors, block errors, errored seconds, and percent error-free seconds. You can simulate a CPU, modem, terminal, or group of terminals for complete interactive testing. The HP 4951A accommodates most popular protocols, data codes, and speeds (to 19.2 kbps).

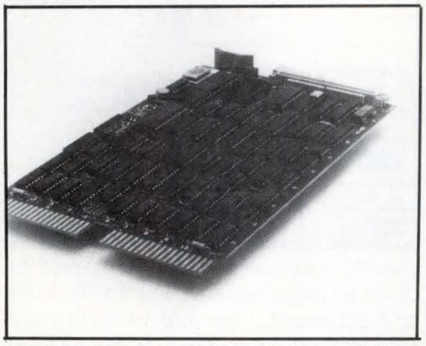
For more information on the HP 4951A and HP 4955A protocol analyzers, call your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

HEWLETT PACKARD

CIRCLE 132

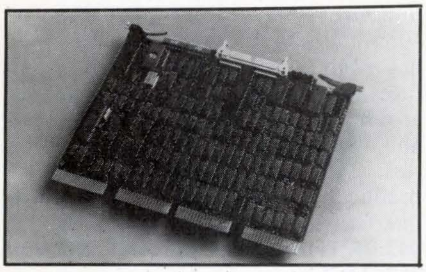
3801401

Board integrates double density floppy disk drives to Q-bus



Model DQ419 8-in. floppy disk controllers interface industry standard SA801/850 double-density floppy disk drives to LSI-11 through 11/23 Plus and Micro PDP-11 computers. Featuring full emulation and operating system compatibility for up to two SA801/850 drives, DQ419 units feature dc motor control, switch-selectable 18/22 bit addressing for up to 4 Mbytes of memory, onboard diagnostics, full sector data buffer, and onboard bootstrap loader. **DILOG,** 12800 Garden Grove Blvd, Garden Grove, CA 92643.
Circle 287

Emulating host adapter joins SCSI devices to Q-bus



The UC02 quad size, single-board host adapter, connects SCSI peripherals with DEC's LSI-11 Q-bus. Another SCSI connecting unit, the UC12, is a hex size board that plugs into a single Unibus backplane slot in PDP/VAX-11 Unibus computers. Both boards emulate DEC's Mass Storage Communications Protocol (MSCP) and allow up to four drives of any standard type or capacity to connect to each host. The UC02 host adapter is priced at $1500, while the UC12 is $1700. **Emulex Corp,** PO Box 6725, 3545 Harbor Blvd, Costa Mesa, CA 92626.
Circle 288

Interface card links Apples to IBM mainframes

Providing a wide range of mainframe communications, the Apple communication protocol card allows Apple II computers to act as remote terminals or workstations in IBM networks. The card emulates the IBM 2780/3780 remote job entry batch and 3270 interactive display system protocols. When configured to use the 3270 protocol, the Apple II system becomes functionally equivalent to an IBM 3271 or 3274 controller with a single attached 3278 display unit. It connects directly to mainframes via a modem. An Apple software package is required. Connecting to Apple II, II Plus, or IIe expansion slots, the card costs $700. Emulator software packages sell for $300. **Apple Computer,** 20525 Mariani Ave, Cupertino, CA 95014.
Circle 289

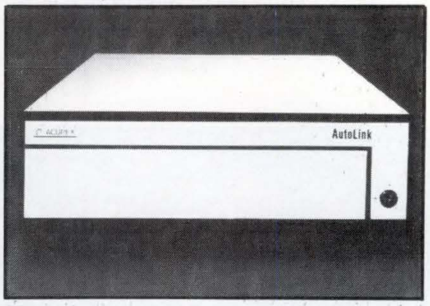
Disk and tape controller interfaces Nova/Eclipse minis

Dual-function controller compatibility with Data General's Nova/Eclipse series minicomputers is offered in the ZDF-1 disk and tape controller. Designed to link drives including CacheTape II and GCR equipment, the unit performs data transfers at up to 2 Mbytes on disk drives, and up to 1 Mbyte on tape drives. Price is $4195. **Zetaco Div, Custom Systems Inc,** 6850 Shady Oak Rd, Eden Prairie, MN 55344.
Circle 290

Low power controller automatically refreshes DRAMs

Low power dissipation is featured in the 82C03 peripheral chip. Using 0.14 W, this high performance CMOS device takes up the space of one 40-pin DIP on a PC board. It controls and automatically refreshes arrays of NMOS or CMOS 64-Kbit DRAMs and is functionally compatible with the bipolar 8202A and 8203. Features include multiplexing of row and column memory addresses; generation of strobes used by RAMs to latch addresses internally; and acknowledgment to system CPU when memory access cycles actually begin. The price is $35 each in 100-piece purchases. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.
Circle 291

Front end processor handles data acquisition



Host data acquisition can be off-loaded via the Autolink intelligent I/O processor. This allows parallel processing power for I/O. Continuous or interval monitoring of up to 90 local or 256 remote I/O channels is possible. Auto-link accomplishes remote user programming via standard RS-232 ports. Optional front-panel display and keyboard are available. The processor maintains optional history files with up to 100,000 channel readings (512 Kbytes). **Acurex Corp,** 555 Clyde Ave, PO Box 7555, Mountain View, CA 94039.
Circle 292

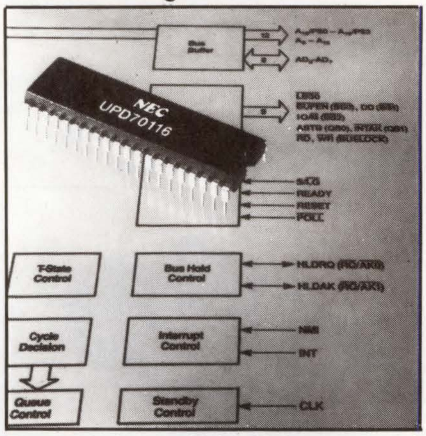
Control interface communicates through many ports

The DMS561 data acquisition and control interface system supports various analog and digital I/O configurations and will operate with RS-232-C, RS-422 or RS-423 serial ports, or with the 20-mA current loop. It can be used either as a local front end or remotely at distances up to 4000 ft (using the RS-422/RS-433 option), or up to 10,000 ft with the 20-mA current loop. The DMS561 accommodates up to eight I/O modules plus an A-D converter. **DI-AN Micro System Ltd,** Mersey House, Battersea Rd, Heaton Mersey, Stockport, Cheshire SK4 3EA England.
Circle 293

Single-board computer offers STD bus compatibility

Based on the Z80A, the MP6102 provides a byte-wide memory in EPROM with an 8-Kbyte capacity. Three channels of user definable counter/timer functions are provided by a Z80A-CTC. One channel is software programmable as the time base for an RS-232-C port. Interrupt control provides management and priority resolution for up to 8 maskable interrupt inputs. Designed to operate in a single processor mode or in the master/slave mode for multiprocessor environments, the board requires no additional serial or parallel I/O cards, counter/timer card, or separate interrupt controller. Cost is $570. **Burr-Brown, Data Acquisition and Control Systems Div**, Box 11400, Tucson, AZ 85734. **Circle 294**

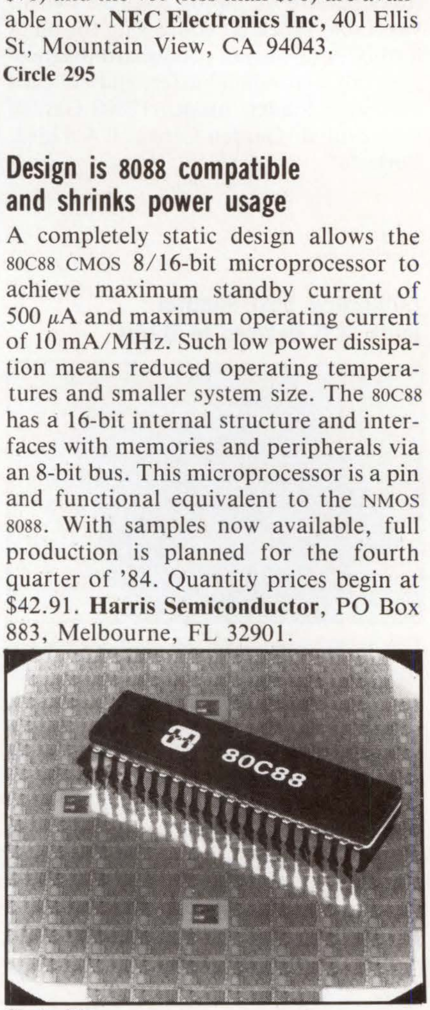
Microprocessors use dual-bus configuration



Two 8-bit devices kick off the V-series of CMOS microprocessors. The V20 features an 8-bit external bus and 16-bit internal bus, while the V30 uses a 16-bit external and internal bus. Employing 2-μm fine pattern CMOS technology and dual-bus configuration, the devices achieve processing speeds 1.5 times that of previous NMOS products at the same clock rate. Sample shipments of the V20 (less than $70) and the V30 (less than $90) are available now. **NEC Electronics Inc**, 401 Ellis St, Mountain View, CA 94043.
Circle 295

Design is 8088 compatible and shrinks power usage

A completely static design allows the 80C88 CMOS 8/16-bit microprocessor to achieve maximum standby current of 500 μA and maximum operating current of 10 mA/MHz. Such low power dissipation means reduced operating temperatures and smaller system size. The 80C88 has a 16-bit internal structure and interfaces with memories and peripherals via an 8-bit bus. This microprocessor is a pin and functional equivalent to the NMOS 8088. With samples now available, full production is planned for the fourth quarter of '84. Quantity prices begin at $42.91. **Harris Semiconductor**, PO Box 883, Melbourne, FL 32901.



Circle 296

The Convergence Factor.

Convergence: the single most critical factor in color CRT performance.

Until now, Delta-gun tubes were the best way to achieve near perfect convergence, but only with costly adjustment electronics. Meanwhile, many in-line tubes are plagued by perceptible misconvergence. Which can lead to poor picture quality. A poor quality image for your product. And poor, bleary-eyed operators.

The Panasonic achievement: low cost in-line color CRTs with better-than-Delta convergence performance.

Without complex adjustment electronics . . . and none of the convergence drift inherent in active correction systems. At last, high resolution in-line tubes with stable performance that stands up to the ravages of time and tough office/industrial environments.

How did we do it? With a preconverged in-line tube/yoke combination unlike any other. Our precision S/ST (saddle/saddle toroidal) deflection yoke is ideally matched to each tube, for near perfect convergence, high repeatability and stability over a wide range of operating conditions.

We combine it with a specially-designed OLF (overlapping field lens) gun and unitized grid construction, providing spot uniformity across the entire screen and near-Delta resolution.

The result: a triumph over the convergence factor. Find out what it can do for your next color terminal or monitor, and ask about our full line of quality color and monochrome CRTs. Write or call: Panasonic Industrial Company, Electronic Components Division, One Panasonic Way, Secaucus, N.J. 07094; (201) 348-5278.

The achievement of Panasonic high resolution in-line color CRTs.

Panasonic
Industrial Company

CIRCLE 134

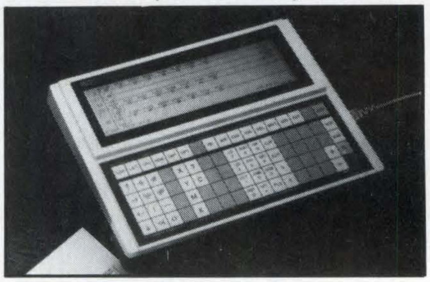
Closed-loop servo interfaces to Multibus systems

Providing the interface between the IEEE 796 environment and two-positioning servo systems, the EI-8941 plugs into the Multibus and handles the system's realtime position tracking. Continuous velocity control over a 4000 to 1 range is possible. Each 8-bit up/down counter is periodically sampled into a holding register by a software controlled timer that also generates an interrupt request and status flag. The system uses a 50-kHz tracking rate. Two or more modules can be slaved to a common timer for simultaneous position data in multi-axis contouring control. **Symbicon Associates, Inc,** 89 Rte 101A, Amherst, NH 03031. **Circle 297**

Single-board computers plug into industrial computer

The IND 68011 analog board and the 68021 digital board fit into the IMP 68000 computer. Each board is divided into two sections. The analog board has a 68000 micro system and an analog I/O section. The I/O section has 4 outputs and 16 inputs, all analog. The digital board is designed along the same lines, yet differs in the I/O section. It has 32 proprietary bidirectional thick-film modules that operate at up to 200 kHz. **Indocomp, Inc,** 5409 Perry Dr, PO Box 157, Drayton Plains, MI 48020. **Circle 298**

Controller's programming panel lets users see sequences in symbol form



The GP-80 programs F series controllers off- or online. Offline programming uses relay ladder circuit diagrams or word instructions. Online, the controller monitors sequences and transfers code through the controller's interface attachment. The screen displays up to 7 lines of a diagram, each containing as many as 11 contacts plus one coil. Two lines at the bottom are for comments. The programming unit can accept as many as 221 contacts in a serial connection. The device costs $3325. **Mitsubishi Electric Sales America, Inc, Industrial Products Div,** 3030 E Victoria St, 1 Rancho Dominguez, CA 90221. **Circle 299**

Programmable controller system merges with computer and software

Disit S5 monitors processes and operator/process communications. It connects Simatic S5-150 programmable controllers to the interactive Disit system. CRT dialog and process visualization functions are implemented in the Disit S5 system with the 3974 M alphanumeric display unit and the S5-150 programmable controller with a 512C interface module. Plant monitoring with mimic diagrams, lists, reports, bar charts, and graphs are possible via interactive screen formats. **Siemens AG, Zentralstelle für Information,** Postfach 103, D-8000 Munich 1, Fed Rep of Germany. **Circle 300**

WHO ELSE COULD FIT 520MB, 20 YEARS OF EXPERIENCE AND A $6 BILLION COMPANY INTO A 9" DISK DRIVE?

9" DRIVE: 520 MB, SIZED FOR TODAY'S SMALLER SUPERMINIS.

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Our latest drive achievement, the NEC D2300, features 520 megabytes (unformatted) of storage capacity, a 15 millisecond average access time and data transfer rate of 1.859 megabytes per second.

Behind our new 520 MB drive is a field-tested technology.

The technology of the D2300 is evolutionary. It is based on our successful 402 MB plated media 8" drive that NEC customers have been using for the past three years.

We know what systems builders need. We build systems too.

That gives us an edge over other drive companies. Because it gives us a special insight into the needs of a systems builder.

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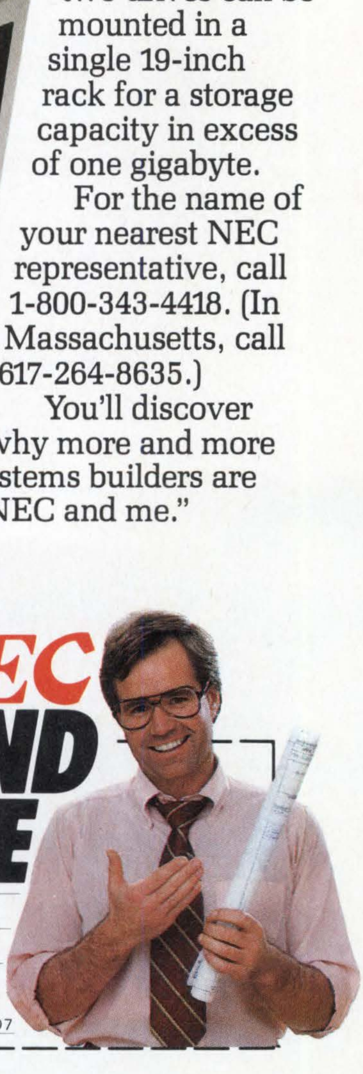
For the name of your nearest NEC representative, call 1-800-343-4418. (In Massachusetts, call 617-264-8635.)

You'll discover why more and more systems builders are saying "NEC and me."

NEC AND ME



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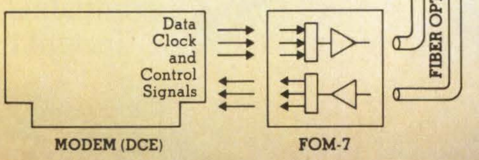
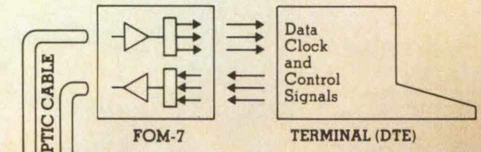
This New Fiber Optic Modem will Extend a DCE Interface to Any Point in Your Local Area Network.

Plus a whole lot more.

- **Can also be used for standard modem applications**
- **Automatically accepts or supplies DCE/DTE clocks**
- **Fully supports all EIA handshaking signals**
- **Provides secondary data channel**

In short, you can use our new fiber optic modem between *any* two plug compatible units in your local area network. And it won't require any jury-rigging or looping clock and interface signals. That's because, from an operating standpoint, our fiber optic modem looks just like an EIA cable; whether you're going from a long-haul modem to a remote terminal or from a CPU port to a printer. And it's just about as easy to install as a cable — we even provide two separate connectors (DTE and DCE) on each modem. YOU determine how our modem will function simply by selecting which connector you use!





Once our fiber optic modem is installed and operating it'll really begin to shine. You'll benefit not only from the advantages inherent with fiber optics (traffic security plus noise immunity) but also from the exceptional operating performance. Our very low error rate and continual signal quality monitoring means that you'll operate with a higher throughput and less downtime than ever before.

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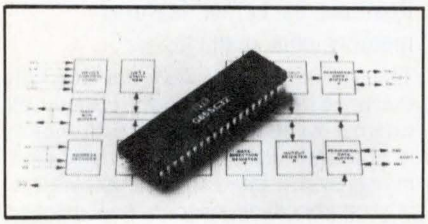
CIRCLE 137

Programmable CMOS RAM links with 6500/6800 series



Bus-compatible with 6500/6800 series microprocessors, the G65SC32 carries functions for programmed control of two peripherals. This CMOS I/O timer device combines a 128- x 8-bit static RAM, two 8-bit directional data ports, an interval timer, and an interrupt control in a single 40-pin DIP. Other features include edge-detect interrupt circuitry, a high impedance three-state data bus, and low power consumption (2 mA at 1 MHz). Part is available in plastic, ceramic, or cerDIP packages. In quantities of 100 or more (plastic package), unit price is $7.65. **GTE Microcircuits,** 2000 W 14th St, Tempe, AZ 85281. **Circle 301**

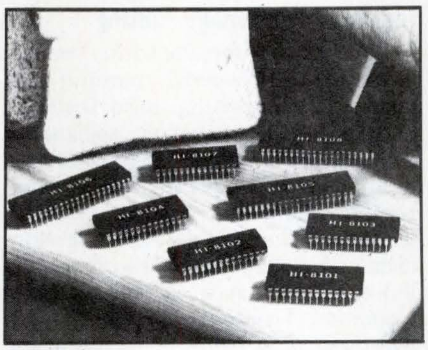
High speed ECL device boasts excellent power/speed ratio

Three ECL10KH devices—dubbed the MC10H101, MC10H210, and MC10H211—form an alternative source of Motorola MECL10KH family products. The devices feature propagation delays of 1 ns, and typical dissipation of 160 mW for the MC10H210/211 and 130 mW for the MC10H101. Complementary outputs cause a function and its complement to appear simultaneously at the device outputs, eliminating the need for external inverters. Skew-timing differential problems and system power requirements are also reduced via these chips. Available in quantity in the fourth quarter '84, the MC10H101 costs $3.34, and the MC10H210/211 ICs are $3.37. **Monolithic Memories,** 2175 Mission College Blvd, Santa Clara, CA 95050. **Circle 302**

Ready for sampling, this 256-Kbit DRAM comes in HMOS

Fabricated in HMOS, the MCM6257 is a 256-Kbit dynamic RAM chip. It requires only nine address lines and can be packaged in standard 16-pin, 300-mil wide, dual-inline formats. Input and outputs are TTL-compatible. Maximum access times are: 100 ns for the 6257-10, 120 ns for the 6257-12, and 150 ns for the 6257-15. Power dissipation on the 6257-10 equals 70 mA maximum active, and 4.5 mA maximum standby. The chip uses laser fuse redundancy and is manufactured with direct step-on wafer photolithographic equipment. Sampling will begin in the second half of 1984. **Motorola Inc, Memory Products Div,** 3501 Ed Bluestein Blvd, Austin, TX 78721.
Circle 303

Breadboard ICs match custom characteristics



A family of breadboard chips offers a wide variety of analog components that match the operating traits of custom ICs. The HI-8000 series consists of eight CMOS chips that constitute a full array of commonly-used analog components and standard circuits. They simplify the integration of analog circuitry, decreasing semicustom circuit development time. The system supports single- or dual-supply voltages from 1.6 to 18 Vdc. **Holt Inc, Integrated Circuits,** 8 Chrysler Ave, Irvine, CA 92714.
Circle 304

Gate arrays combine with high speed onchip memory

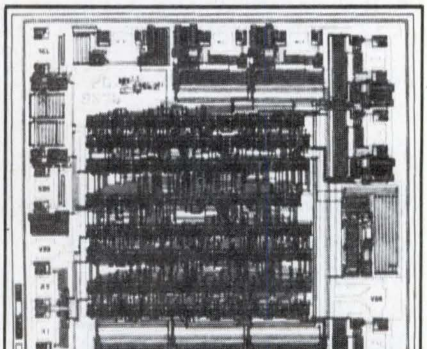
The MCA1500M packs in 1464 equivalent gates of logic and 1280 bits of user-configurable RAM. Onchip memory access time is 5 ns. The chip offers 110 total logic cells of which 64 are major cells and 46 are output cells (ECL inputs are direct). Dedicated memory test capability allows access to each memory block and is independent of the user selected memory configuration and logic portions of the array. There are 110 basic memory macros available, ranging from 32 x 5 to 256 x 5. Memory is also configurable in dual-port mode with macros ranging from 32 x 5 to 128 x 5. Packaged in a 149-pin grid array, the device, in 1000-piece or more quantities, is priced at $150 each. Nonrecurring engineering cost is approximately $25,000 plus CPU time. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.
Circle 305

Variable-length shift register joins digital filter

The TDC1011 8-bit register is planned as a companion to the TDC1028 finite impulse response (FIR) filter. Operating at a 50-ns cycle time (20-MHz shift rate), the TDC1011 is fully synchronous and controlled by a master clock. It can be programmed to any word length between 3 and 18 stages. This variable-length shift register is available in a 24 lead DIP or cerDIP, and priced at $23 per 1000 pieces cerDIP. **TRW, LSI Products Div,** PO Box 2472, La Jolla, CA 92038.
Circle 306

Remote I/O expander features low current consumption

The PCF8574 CMOS remote I/O expander comes with 8-bit parallel channels and onchip I²C bus. This IC uses the two-wire serial I²C bus to connect to an MAB8400 microcomputer or to any standard 8-bit microcomputer (in which case the I²C bus receives a software implementation). Supply voltage range is 2.5 to 6 V. Low current consumption is typically 3 μA with no external load. Onchip power-on reset circuits set all ports to high at power-up. **Philips, Electronic Components and Materials Div,** PO Box 523, 5600 AM Eindhoven, the Netherlands.



Circle 307

Controller processor available from second source

A semicustom, 4-bit microcontroller—the ETC-9420—claims fully-compatible equivalency to National Semiconductor's COP-420C. This CMOS device contains system timing, internal logic, ROM, RAM, and I/O for many dedicated control functions. Ten sample devices can be delivered within eight weeks, with the first 5000 pieces typically shipped within eight additional weeks. **Thomson Semiconductor**, 6660 Variel Ave, Canoga Park, CA 91303.
Circle 308

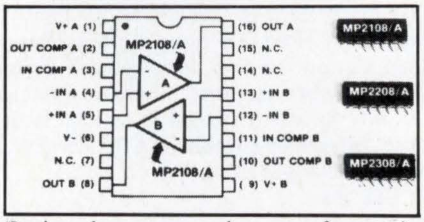
Family of CMOS MACs offers selectable accumulation

A family of high speed CMOS multiplier-accumulators provides selectable accumulation, subtraction, rounding, and preloading. These MACs—aimed at portable and handheld applications—dissipate 1/10th the power of TRW bipolar equivalents. The TMC2010 operates at 160 ns and provides 35-bit accumulation, while the TMC2009 performs 27-bit accumulation in 135 ns, and the TMC2008 does 19-bit accumulation in 100 ns. Available in 64 lead DIP (except for the 48 lead DIP TMC2008), 68 contact chip carrier, or 68 leaded chip carrier, the TMC2010, TMC2009, and TMC2008 are $166, $98, and $48, per 1000 pieces, respectively. **TRW, LSI Products Div**, PO Box 2472, La Jolla, CA 92038.
Circle 309

Semicustom array in CMOS reduces high voltage routing

The TMG5002 uncommitted array features 16 push-pull 200-V output transistor pairs controlled by low voltage logic. Dielectric isolation enhances operation. Applications include panel display driving, electrostatic or ink jet printing, piezo crystal driving, high voltage leakage testing, ATE, and telecommunications. TMG5002 development costs start at $20,000 with production costs based on circuit complexity and quantities. **Telmos Inc**, 740 Kifer Rd, Sunnyvale, CA 94086. **Circle 310**

Op amps cover low power applications



Designed as a second source for PMI's PM2108/A series, the MP2108/A amplifier line features low input current operation. Offset current measures 200 pA maximum, bias current rates 2.0 nA maximum, power consumption is 18 mW maximum at ±15 V, and low offset voltage drift hits 5.0 μV/°C maximum. Parts are apt for battery operated and low power applications, as well as for integrators, log generators, low drift peak detectors, and current sources. Typical 100-piece prices are MPOP2108Q, 16-pin cerDIP, military temperature range, $19.30; MPOP2108A/883B, 16-pin cerDIP, military temperature range, $76.70. **Micro Power Systems, Inc**, 3100 Alfred St, Santa Clara, CA 95050.
Circle 311

SOFTWARE

Realtime OS kernel features memory pool manager

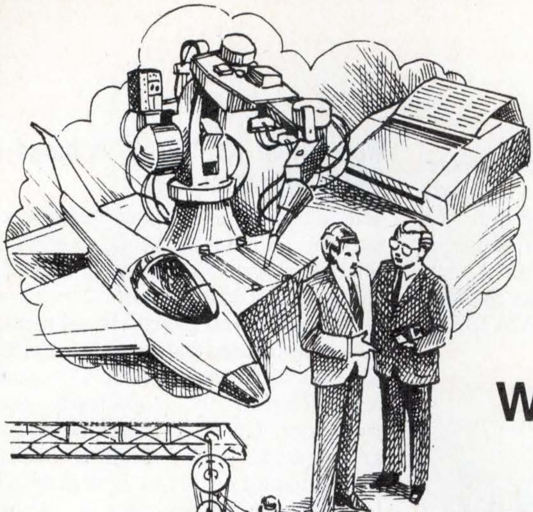
The ROMable NS-EXEC multitasking executive monitors and controls multiple external events occurring asynchronously in real time. Performing task and event management, intertask communication, interrupt handling, memory pool management, and timer management, this operating system kernel for the NS16000 microprocessor family requires only 2 Kbytes of RAM and 4 Kbytes of ROM. It executes at a 50 μs rate, measured as the time from interrupt to first user defined instruction. Available for one-time license fee of $1000. **National Semiconductor Corp, Software Products Group**, 2900 Semiconductor Dr, Santa Clara, CA 95051. **Circle 312**

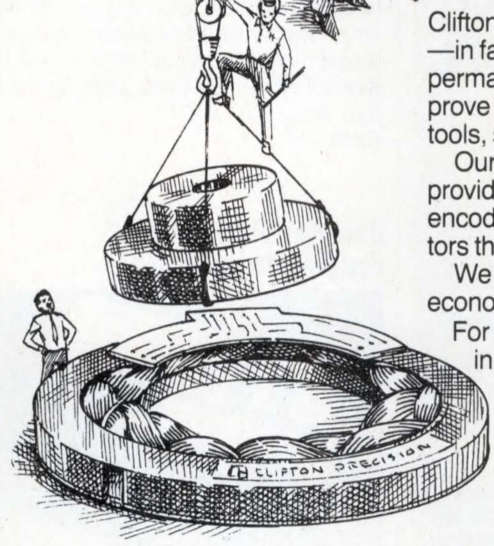
Domain gains Lisp language fluency

The Domain programming language base receives an artificial intelligence extension with the addition of Lisp capabilities. Domain Lisp includes an interpreter and optimizing compiler, as well as tools for building expert systems, special purpose graphics, and robot vision software. Communications support includes IBM 3270 emulation, X.25, and Ethernet. Domain Lisp is priced at $1850 per node, and $15,500 per site. **Apollo Computer Inc**, 15 Elizabeth Dr, Chelmsford, MA 01824.
Circle 313

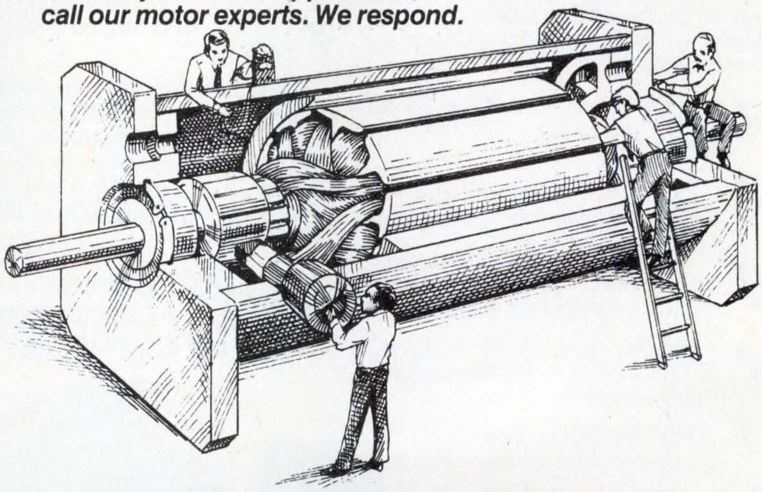
Graphics software packages combine GKS and Unix

Written in C for the Unix environment, Visual:GKS and Visual:C-Chart packages are based on the Graphical Kernel System (GKS). Visual:GKS lets system programmers create multiple graphics windows on multi-user systems for applications such as CAD/CAM, process control, mapping, and simulation analysis. Visual:C-Chart contains features such as automatic axis and legend scaling, shadowing, filled fonts and user defined markers. Visual:GKS costs $1200 for a single-user license and up to $8000 for a 32 user license; Visual:C-Chart costs $2000 for a single user license, and up to $12,000 for a 32 user license. **Visual Engineering**, 502 Mace Blvd, Davis, CA 95616.
Circle 314





CLIFTON PRECISION



High capacity file server adds to distributed system

The 9760 unison server is a rackmounted design providing full data storage and backup capabilities for installations with a large number of diskless nodes. It functions transparently to other nodes for a virtually unlimited amount of shared data storage as well as backup and storage. The server is built around the basic 9000 system including a 68010 based CPU with 1 Mbyte of dual ported RAM, Ethernet hardware, Unix, and a distributed operating system. **Cadmus Computer Systems, Inc**, 600 Suffolk St, Lowell, MA 01854.
Circle 315

Workstation for CAD/CAE is based on 32-bit microprocessor

The SaberStation's application processor uses the National Semiconductor NS32032 microprocessor. Operating at a 10-MHz clock rate, it executes at 1.2 MIPS, and provides demand paged virtual memory plus a hardware floating point coprocessor. Pascal, Fortran-77, and C languages are offered for this Unix-based system. SIGGRAPH, Core 2-D and 3-D, and GKS are included in the graphics package. Image memory is 1664 x 1248 pixels. The image processor provides a 180-MHz video display with 24-bit color resolution. Single quantity price is less than $40,000. **Saber Technology Corp**, 2381 Bering Dr, San Jose, CA 95131.
Circle 316

Universal programmer designed for upgrades

The PP39 dedicated programmer accommodates future extensions. Its single-level, plug-in modules contain integral firmware adaptable to multiple devices. It handles EPROMs and EEPROMs as well as NMOS, HMOS and CMOS microprocessors. For high programming integrity, all 8-bit integral RAM data is continuously checked by a parity bit. Dynamic access time tests can be performed for any device. The PP39 is priced at $1749. **Stag Microsystems, Inc**, 528-5 Weddell Dr, Sunnyvale, CA 94086.
Circle 317

Instrument stores and compares video images

Video Subtractor 492 uses solid state dual memory to compare video images and display any differences. Aimed at applications including inspection and quality control, model 492 offers a choice of 512- x 256-pixel memory or 512- x 512-pixel memory with a 6- or 8-bit gray scale. **Colorado Video**, PO Box 928, Boulder, CO 80306.
Circle 318

Introducing the VP-10 Graphic Element Processor

Graphics Magic from KMW Systems

KMW Systems Corporation has combined years of experience in graphics processing with the latest in single-board micro-processing technology to produce the new VP-10 Graphic Element Processor. The speed, reliability and *cost-effectiveness* of the VP-10 make it the ideal graphic controller for a wide variety of color and monochromatic raster hardcopy devices.

Performance Features

High speed hardware interpolation allows the VP-10 to drive most popular hardcopy raster output devices, including smaller electrostatic plotters, at full rated speed. The Tektronix 4691, the Versatec V-80, the Seiko CH-5201, and Benson plotters are but a few of the raster devices currently supported by the VP-10. The VP-10 features color support for both intensity modulated and dithered or halftone devices. Input requirements and host processing are minimized by the VP-10's ability to handle high-level graphic structures such as polygons, circles and text. Automatic dual modes of operation allow page-size plots with unlimited element capacity and large format plots with 200,000 element capacity.

Integrated Communications

For the remote use of the raster output device, the VP-10 features a full range of input communications options. Among the available options are integrated communications for the IBM 2780/3780 and HASP Bisync protocols, the IBM 3770 SNA/SDLC protocol and the Honeywell GRTS 115 protocol. Direct-attach interfaces available with the VP-10 include Data Products parallel and serial EIA RS-232-C.

Operational Features

The VP-10 incorporates many of the features of KMW's other Vector Processor products as well as some new innovations. Among the VP-10's operational features are:

- Transparent mode of operation
- Print spooler capabilities
- Input and output overlapping
- Multiple copy capabilities
- Real-time optimization of memory for list processing or full-page buffering
- Color or monochromatic device control
- High-level graphic element input such as polygons, circle/arc, vectors and text

The VP-10 also features internal diagnostic capabilities including test plot and error handling.

If you think Graphic Element Processing is a trick, let the VP-10 work a little graphics magic on you.

KMW SYSTEMS CORPORATION

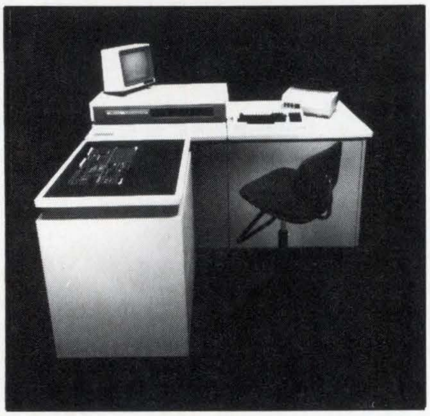
8307 Highway 71 West • Austin, Texas 78735 • Call toll free 800/531-5167
TWX: 910-874-2005/CABLE: KMWSYS AUS

NCC Booth #C3630 Siggraph Booth #906

CIRCLE 142

Performance testing system handles high volume

Acting as an in-circuit tester or diagnostic repair station for boards, the 2720 diagnoses PC boards of processor families (eg, the 68000 and 8086) at their operating speeds in their native system environments. The 2720 applies stimulus through a microprocessor on a bus structured unit-under-test (UUT) and can simultaneously control up to four processors. A bed-of-nails fixture provides maximum throughput for high volume operations. The tester's 1024 high speed sensors collect qualified data at rates up to 32 MHz. Prices begin at $105,000 with deliveries starting in the third quarter of this year. **GenRad Inc**, 300 Baker Ave, Concord, MA 01742.



Circle 319

Compiler and emulator assist 8096 microprocessor development

The PL/M-96 compiler generates code for execution on the upcoming family 8096 microcontrollers. This package includes a floating point subroutine library, plus programs for linking software modules and creating libraries of commonly used routines. A single-board emulator—the iSBE-96—aids the 8096 software and hardware debugging process. It costs $3500. The PL/M-96 license fee is $4000. **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.
Circle 320

August Preview
Watch for a special article on power supplies/packaging

PACKAGING & POWER

Uninterruptible power system improves efficiency

The slim-line, compact 1.0-kVA UPS is available in 60- and 50-kHz models to protect electronics from all common ac power problems, including blackouts. It uses two separate dc power supplies to power the inverter and charge the battery. A full wave diode bridge powers the inverter and a linear current-limited power series-pass regulator charges the battery. The system features a relay bypass transfer that switches the load directly to the utility power line if load demands exceed the overload capacity of 200 percent for 167 ms. The UPS sells for $2955. **Sola Electric,** 1717 Busse Rd, Elk Grove Village, IL 60007. **Circle 321**

Switching power supply provides 80-W operation

The XL80 is a 70- to 100-W switching power supply in a 60-W form factor. This four-output device will supply a full 80 W of power at 50 °C in free air and up to 100 W of continuous power with 20 ft^2/min of forced air. It is especially aimed at small computer applications requiring highly filtered 12-V output, isolated from other 12-V loads, to drive a CRT display for jitter-free operation. Available in August, the 100-piece price is $107. **Boschert Inc**, 384 Santa Trinita Ave, Sunnyvale, CA 94086.
Circle 322

Switching-power supplies comply with international noise/safety standards

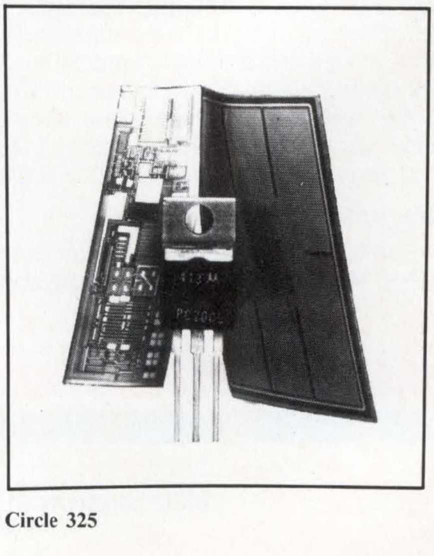
Modular ac to dc 930 series meets VDE-0871/875 and European IEE regulations for emi/rfi, as well as CSA, FCC and UL requirements. The compact 25-W supplies guarantee 80-percent minimum efficiency and have output ratings of 5 V at 5 A, 12 V at 2 A, and 24 V at 1 A. Minimum input-to-output isolation is guaranteed at 3750 Vac, while maximum leakage current is guaranteed at 5 μA. The series accepts 110-Vac line voltage at frequencies ranging from 47 to 440 Hz; 220-Vac versions are also available. Unit prices start at $156 with quantity discounts available. **Analog Devices, Inc,** Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062. **Circle 323**

Plastic window package eases EPROM erasure

A plastic package with an integral window for erasing the EPROM it houses has been developed. Preproduction model EPROMs mounted in this package have sustained 2000 h of continuous operation with no significant change in electrical parameters. They do so while enduring thermal cycles of -55 to 150 °C and temperature/humidity bias tests of 85 percent relative humidity at 85 °C. **Oki Semiconductor,** 1333 Lawrence Expwy, Suite 401, Santa Clara, CA 95051.
Circle 324

Overvoltage protection derives from single chip

High speed CMOS logic and high current TMOS vertical power structuring combine in SMARTpower II devices. The MPC2005, first in this line, represents an overvoltage and temperature protection circuit capable of discharging capacitors with peak currents of 150 A and operating at up to 15 A of continuous anode current. When voltage exceeds 6.2 V or the junction temperature rises over 125 °C, the device will trip and remove the voltage from the system. This single chip can replace three resistors, an SCR, and an IC, while protecting memories on 5-V buses from overvoltage transients and extreme temperatures. Pricing in quantities of 100 and up is $4.50. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.



Circle 325

First "Graphics Ready" monolithic raster scan DAC.

125 MHz, 8-bit, 800 mW Glitch-free DAC for only $39*

The TDC1018 from TRW is the first monolithic 8-bit, 125 MHz D/A converter that's "graphics ready." This means you can skip the analog buffer amplifiers, video sync and blank inserters or deglitching circuitry—they're on the chip. And because the TDC1018 uses the TRW 1 Micron OMICRON-B™ process, it features higher reliability, improved speed-power product and pixel-perfect signal conversion.

The TRW TDC1018 is your complete solution to raster scan applications, color graphics, digital synthesizers, automated test equipment and high speed, high resolution video system designs.

Our compact design fits into a small 24 pin DIP, and is suitable for your large volume applications. Consider these outstanding features:

- 1.7 ns rise time; <5 ns settling time
- Unique design virtually glitch-free
- On-chip latching for easy interface of blank, sync, bright and reference white
- Differential logic for maximum speed, minimum noise

- Protection circuitry prevents power supply spikes at output
- Directly drives standard 75Ω load
- Multiplying capability allows gain adjustment
- Differential clock reduces power supply ripple effect
- Differential outputs produce true and inverse video
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- 1/2 LSB linearity

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CIRCLE 143

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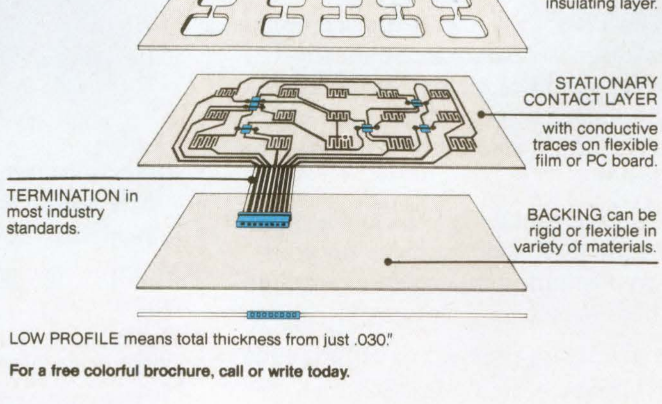
All this versatility... and long service life, too. In home, office or hostile industrial environments. Because each TOUCH PANEL is custom designed and produced by the people who know more about keyboards than just about anybody. The people at Cherry.



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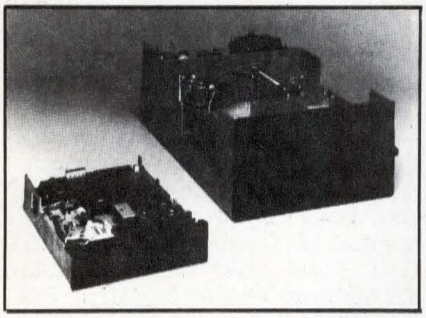
CIRCLE 144

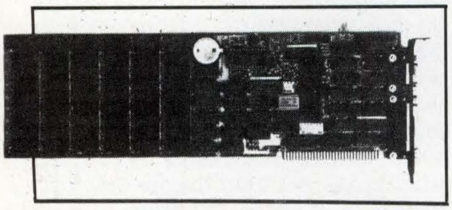
High performance, compact unit increases bit density



The Shugart 475 double-sided drive features 1.6-Mbyte capacity, 500- kbit/s data transfer rate, and track-to-track access time of 3 ms. This half-height 5¼-in. minifloppy disk drive can read data written on 49-track/in., 5¼-in. diskettes. Bit density in the 475 reaches 9646. A low profile, brushless direct drive dc spindle motor revolves the spindle at 360 rpm, compared to 300 rpm for current minifloppies. In quantity, the 475 costs under $200. **Shugart Corp,** 475 Oakmead Pky, Sunnyvale, CA 94086.
Circle 326

Plug-in multifunction card increases PC memory

A combination card providing from 64 to 384 Kbytes of parity checked DRAM, the IDEAmax 384 requires only one slot in the IBM PC or XT and comes with RAMFloppy disk emulation, print spooler, diagnostic, and realtime clock software. The IDEAmax 384 is available with such options as serial interface, parallel interface, and clock/calendar. This card allows cabling of both serial and parallel interfaces from the back of the board. Prices range from $320 for 64-Kbyte memory with one option, to $795 for 384 Kbytes and four options. **IDE Associates Inc,** 7 Oak Park Dr, Bedford, MA 01730.



Circle 327

Subsystem backs up units using SCSI controller designs

High speed rewind, track select, and file orientation mean rapid access times for the IDS-412. This ¼-in. tape backup unit handles computers with SCSI controllers (including machines from DEC, Fujitsu, Sanyo, and others) while storing 17.6 Mbytes and writing at 1 Mbyte/min. The IDS-412 subsystem MTBF lists at 5000 h and power requirements are 120 Vac at 60 Hz, 240 Vac at 50 Hz. Unit price: $2295. **Alloy Computer Products,** 100 Pennsylvania Ave, Framingham, MA 01701. **Circle 328**

Chocolate media double conventional capacity

Named "Chocolate media" for its resemblance to confectioner's chocolate, these high coercivity rigid oxide media deliver twice the capacity of conventional oxide rigid Winchester disks. These 8-in. and 5¼-in., 96- and 95-mm disks represent an alternative to thin-film media. The media's oxide is a particulate gamma ferric oxide that has been enhanced through cobalt treatment, which increases media coating coercivity from approximately 350 to 600 Oe, increasing storage to 20 Mbytes per 5¼-in. and 40-Mbyte per 8-in. rigid disk. **Dysan,** 5201 Patrick Henry Dr, Santa Clara, CA 95050.
Circle 329

Miniaturized disk drives offer substantial storage

A 3½-in. Winchester disk drive handles 6- or 12-Mbyte and ST506 or 412 interfaces, measures 1.625 x 4.000 x 5.750 in. (4.13 x 10.16 x 14.61 cm) and weighs only 2.2 lb (5.58 kg). The reduced size affords a smaller footprint, lower power requirements, less heat generation, and greater shock resistance. A family of drives has been created around this 3½-in. model, with common parts and identical performance specifications. Three different bracket sizes with bezels and mounting dimensions conforming to industry standard form factors are available. Smaller drive advantages are immediately available to systems using 5¼-in. drives without design changes. Replacing larger drives with the 3½-in. size leaves space for additional shock protection. Prices are under $500 for 10,000 quantity. **Microcomputer Memories, Inc,** 7444 Valjean Ave, Van Nuys, CA 91406.
Circle 330

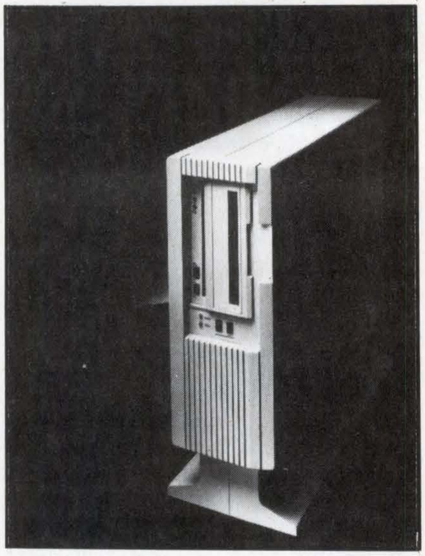
Option enables improved 308X execution

An enhancement for 308X base model processors increases internal execution speed by about 6 percent. The option reduces cycle time—for the 3081 G and K; the 3083 E, B and J; and the 3084 Q—to 24.5 ns. The 3084 processor requires two performance options, one for each processing side. Available in September, the features required for the option can be purchased for $16,000; option is available under lease and rental plans as well. **IBM Corp, Information Systems Group**, 900 King St, Rye Brook, NY 10573.
Circle 331

Lightweight PC-compatible, portable unit uses LCD screen

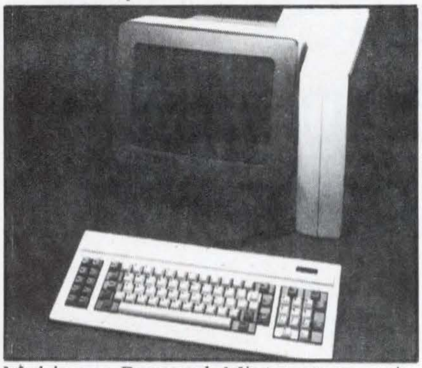
Featuring 256 Kbytes of onboard RAM, a 25-line x 80-col LCD and a clock rate doubling that of the IBM PC, this 17-lb (7.7 kg) system is compatible with IBM PC software, though some diskette formats must be converted. Built-in modem, two double-density 96-track/in. disk drives (each providing 1 Mbyte of unformatted additional storage), and a built-in, 40-col thermal printer are other significant features of the 80186-based system. It can also combine with a special graphics terminal for low cost CAD applications. Cost: $3449. **STM Electronics Corp**, 535 Middlefield Rd, Ste 250, Menlo Park, CA 94025.
Circle 332

Variable architecture system based on DEC processor



Based on a PDP-11/23 Plus processor, the Powerframe 2340 is a midrange, variable architecture system. Operating systems available for the 2340 model include RSTS/E, RSX-11M+, and RT-11. The unit supports up to 12 concurrent users. An 8-in. fixed/removable rigid disk drive provides 40 Mbytes of user storage. Dual ports, 256 Kbytes of DRAM, and an expandable system pedestal cabinet round out the standard system. The free-standing cabinet contains a slide-out wire cage for easy exchange of logic, memory boards, and storage subsystems. The chassis holds empty slots for expanding memory to 4 Mbytes or adding logic cards. Systems are priced at $13,990. **Ford Higgins Ltd**, 4755 Walnut St, Boulder, CO 80301.
Circle 333

System makes connections for PC-compatibles



Multi-user Personal Mini systems gain minicomputer capabilities for IBM PCs and PC-compatibles. A PM/16 desktop computer, using an 80186 and Z80A, serves as host for up to 16 microcomputers. Mass storage is provided by a 46-Mbyte (formatted) internal Winchester disk drive. The system can support one serial and one parallel printer. An InfoShare operating system lets users share data files, programs and peripherals, run multi-user software as well as single-user PC-DOS, and protect confidential data. The Personal Mini PM/16 computer with OS sells for \$8995. PM Workstations sell for \$1995. A plug-in card to add work stations sells for \$99. **Televideo Systems Inc,** 1170 Morse Ave, Sunnyvale, CA 94086.
Circle 334

Low cost Apple-compatible runs on CP/M

Romar II(X) runs under both Apple DOS and CP/M operating systems. Featuring a detached fully encoded keyboard with 87 keys, the unit is centered around a 6502 microprocessor. It has 64 Kbytes of ROM, expandable to 192 Kbytes, plus a Z80 circuit card for running CP/M programs. The chassis contains eight expansion slots. Price is \$695. **Romar Computer Systems, Inc,** 22110 Clarendon St, Suite 103, Woodland Hills, CA 91367.
Circle 335

Micro with mainframe power handles AI applications

Designed for artificial intelligence applications and exploratory software development, the Xerox 1108 dedicated workstation is now offered with larger memory and extended processor board options. The memory option increases the unit's maximum main memory from 1.5 to 3.5 Mbytes, while the extended processor option provides a larger control store, a floating point processor, and a parallel I/O port. Pricing for the 1108 starts at \$26,000, with the main memory option set at \$9100 and the extended processor option listed at \$4500. **Xerox Special Information Systems,** 250 Halstead St, PO Box 7018, Pasadena, CA 91109.
Circle 336

Two-user machine furnishes lower cost AI power

Lambda 2X2 systems (composed of two independent, concurrently executing Lisp processors) have artificial intelligence capabilities. These 32-bit virtual microcode processors operate through a 37.5-Mbyte/s multiprocessor NuBus architecture, with 128 Mbytes of virtual address space per user. Each user has a keyboard, mouse, high resolution display, and display controller. The machine's 2-Mbyte physical memory is segmented between the processors, while a 470-Mbyte Winchester and integral Multibus are shared. In quantity, per user price is as low as \$44,000. Field upgrades for LMI Lambdas are \$40,000. **LISP Machine Inc,** 6033 W Century Blvd, Suite 900, Los Angeles, CA 90045.
Circle 337

Supermicro implements RISC architecture

The 32S is a single-user 32-bit workstation capable of executing up to 8 MIPS. Measuring 28.4 x 17.5 x 30 in. (72.1 x 44.5 x 76.2 cm) and weighing 225 lb (102.1 kg), the 32S can be placed under a desk or configured as a standalone. It uses a reduced instruction set computer architecture and is fully software compatible with the Ridge 32C. Featuring a virtual memory system with 4 Gbytes of addressable code and data, the 32S uses the ROS Release 3.1 operating system, (derived from Unix System V, under license from AT&T) and BSD 4.2. Unit price of the basic configuration: \$36,400. **Ridge Computers,** 2451 Mission College Blvd, Santa Clara, CA 95054.
Circle 338

PERIPHERALS

Versatile printers deliver high resolution and multispeeds

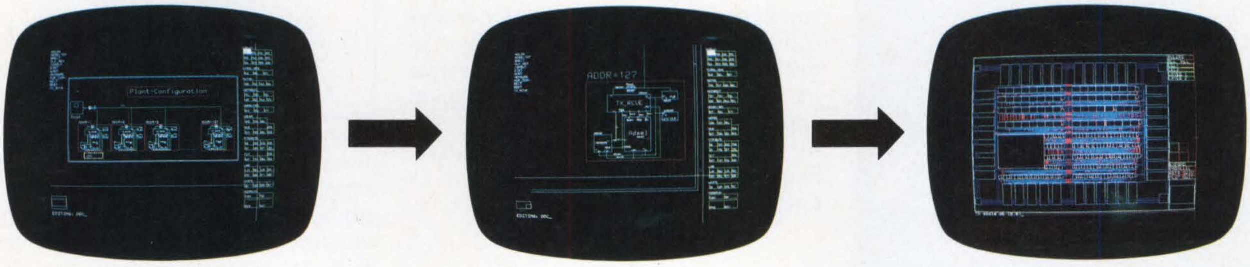
Model 8010 dot-matrix printers can print words, numbers, and graphics with high resolution, multispeed capability. The 8010 is the first member of the 8000 series. It links to popular microcomputers including the IBM PC, Apple II, TRS-80, and DEC Rainbow. It can print drafts at 180 chars/s, text at 110 chars/s, and letter quality at 30 chars/s. A dual-pass technique and staggered wire print-head combine to form letter quality characters. Unit measures under 5 in. (12.7 cm) high, less than 16 in. (40.6 cm) wide, less than 12 in. (30.5 cm) deep, and weighs under 19 lb (8.62 kg). It costs \$650, with quantity discounts available. **Dataproducts Corp,** 6200 Canoga Ave, Woodland Hills, CA 91365. **Circle 339**

Large area screen printer can cover diverse applications

Various electronic print applications are handled by the 4114A model screen printer. These include PC board resist and legend printing, thick film work, solder paste deposition, membrane touch switches, and LCDs. The 4114A has a 10- x 8-in. (2.54- x 20.3-cm) print area and an automatic motorized print cycle, as well as adjustable print speed ranging from 0 to 4.7 in./s. On-contact printing allows extra thick deposition of paste when metal stencils are used. Print registration (held to ±0.001 in.) results from close print cycle control and high repeatability. **Universal Instruments Corp,** PO Box 825, Binghamton, NY 13902.

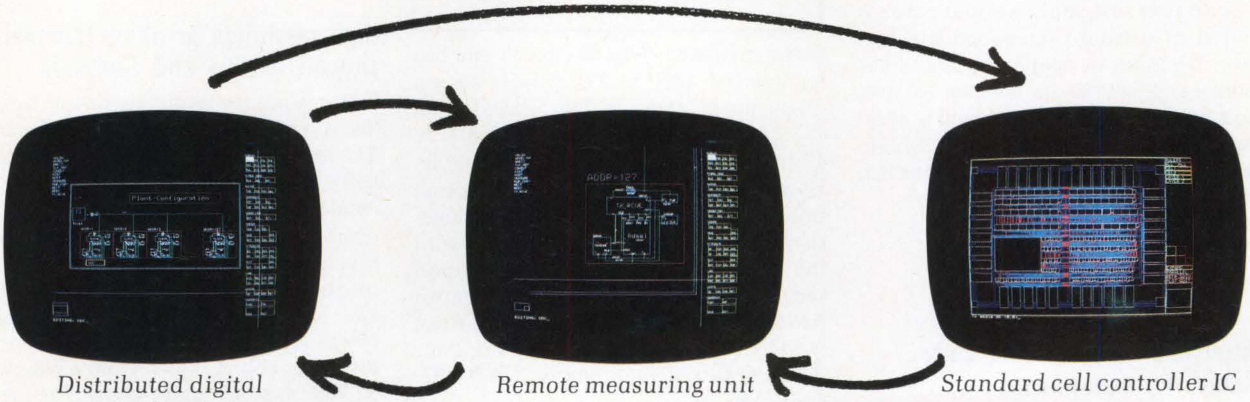
Circle 340

Silvar-Lisco presents hierarchical design–your way.



Distributed digital control system *Remote measuring unit* *Standard cell controller IC*

Or your way.



Distributed digital control system *Remote measuring unit* *Standard cell controller IC*

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SILVAR LISCO™

CIRCLE 147

Tilt-and-swivel display terminal is compact

The HP 2392A display terminals offer all the functions of predecessor HP 2622A block-mode data entry terminals while reducing price and adding a green screen and ergonomically improved design. Even with 12-in. diagonal display, the unit takes up only 1 ft^3. An integrated tilt-and-swivel mechanism adjusts according to the user's preference. Smooth scrolling of up to four text pages without pause is offered as standard. Designed for data entry, program development, and data-inquiry applications on HP 3000, HP 1000, and HP 9000 systems, the terminal is ANSI-standard compatible. It costs $1295. **Hewlett-Packard**, 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 341

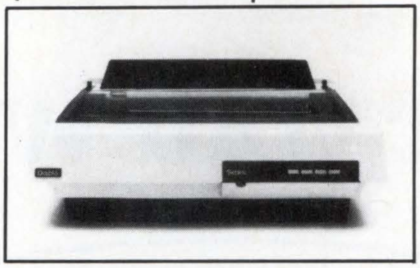
Plotter and copier deliver color graphics for supermicros

Color graphics plotter and copier options, designated the PL660 and the GC810 respectively, are available for MC-500 and Workstation-500 Unix-based, 32-bit systems. Offering 0.001-in. resolution, the PL660 has easily selectable 8.5- x 11-in. (21.6- x 27.9-cm) or 11- x 17-in. (27.9- x 43.2-cm) paper sizes. It can create color transparencies. The peripheral is controlled by the host via an RS-232 serial interface. The GC810 color graphics copier sports drop-on-demand, ink jet technology with 120 addressable dots/in. resolution (enabling 960 x 1280 points on an 8.5- x 11-in. image). This device links via a parallel line printer interface board inserted in a host Multibus slot. **Masscomp**, One Technology Park, Westford, MA 01886.
Circle 342

Electrostatic monochrome plotters improve in expanded series

The 7000 series is available in 36- and 44-in. widths and offers up to 4 times more resolution and 25 percent greater accuracy than the previous 8000 series. The devices plot at 400 points/in. and use an integral raster data translator to accept data at half resolution. Adjustable plot speed control permits the operator or host computer to set speed from ⅛ in./s to rated speed. Maximum accumulated error of a plot is ± 0.15 percent, horizontal and vertical. Prices range from $47,200 to $58,100. **Versatec**, 2710 Walsh Ave, Santa Clara, CA 95051.
Circle 343

Low cost daisy wheel printer operates at medium speed

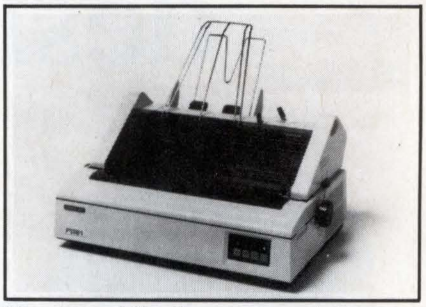


Series 36 runs at 30 to 40 chars/s and has an MTBF of 4000 h. The printer has an all-purpose interface that includes an RS-232-C, IEEE 488, and Centronics port. A 12-bit parallel interface is also available. User friendly features include drop-in printwheels and snap-in ribbon cartridges that can be inserted and removed with the feeder on. Automatic printwheel recognition and a fully featured control panel allow unattended operation. Price is $1595. **Diablo Systems Inc**, 901 Page Ave, PO Box 5030, Fremont, CA 94537.
Circle 344

Pen for digitizer tablets increases reliability

Designed for use with electronic digitizers, this electronic pen sports high reliability. It has only one moving part. An easily replaceable dome switch is located in the pen's housing. Life expectancy of the switch is 7.5 million operations. A high degree of tactile feedback is achieved when the pen is pressed against the digitizer tablet because the user feels a "click," confirming that data is being recorded. **California Computer Products, Inc**, 2411 W La Palma Ave, Anaheim, CA 92801.
Circle 350

Printhead design eliminates scalloping for higher quality text



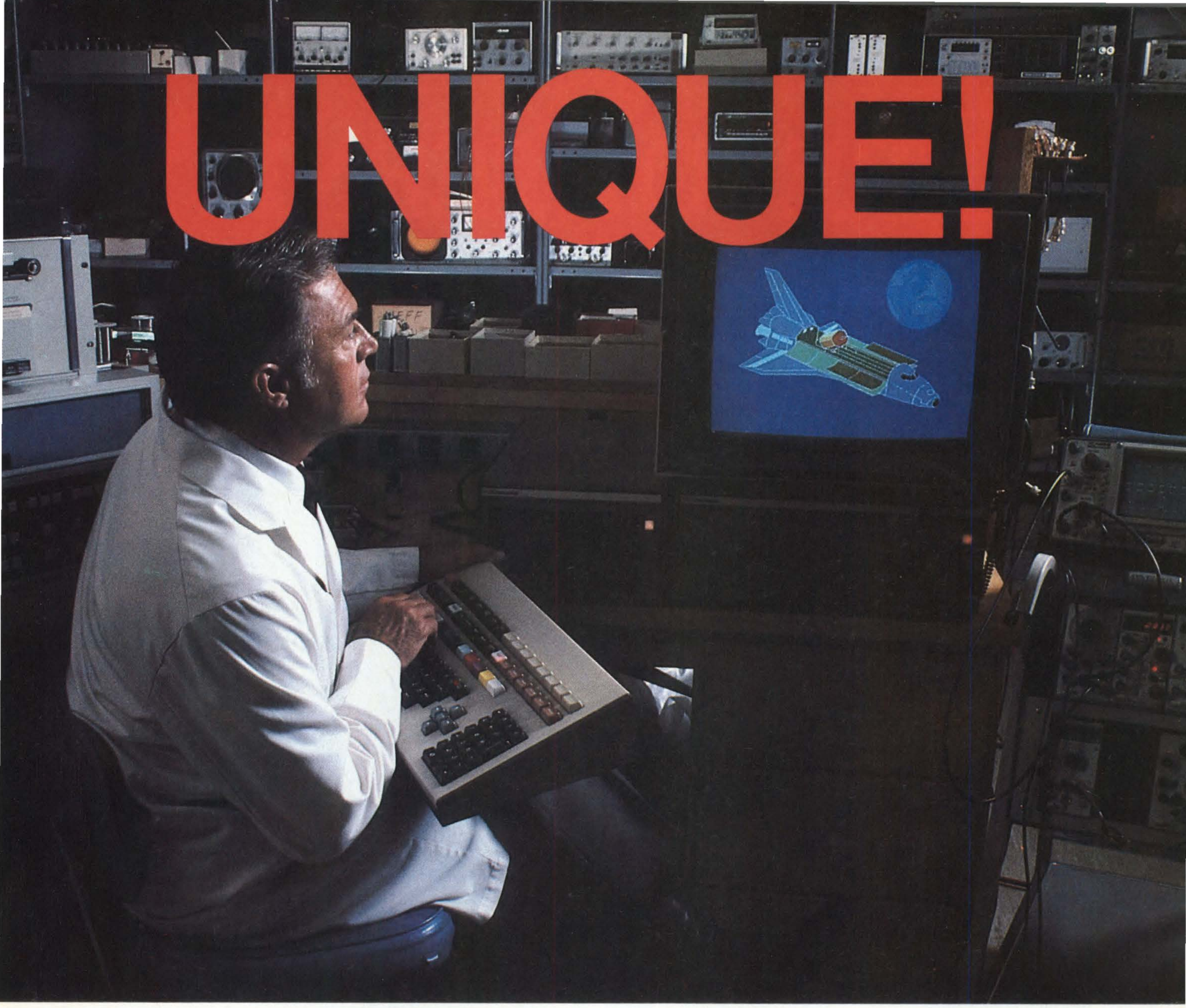
The top-of-the-line P1351 printer can download fonts and produce high speed letter-quality text and high resolution graphics. Using a 24-pin printhead composed of fine wire pins that create precisely overlapped dots, the design eliminates common printer "scalloping" and "stair-stepping" effects. The 132-col P1351 produces letter-quality work at 100 chars/s, and draft copy at 192 chars/s. A 226-col format for spreadsheets and paper saving is also featured. **Toshiba America, Inc, Information Systems Div**, 2441 Michelle Dr, Tustin, CA 92680.
Circle 351

High resolution graphics terminals support DISSPLA and Template

Color graphics terminals in the D-SCAN line come in 14- and 19-in. raster displays. The line supports DISSPLA and Template software as well as providing Tektronix emulation. The GR-1104 offers 1024 x 780 pixel resolution and onscreen display of 8 colors from a 512-color palette. The GR-2414 offers speed of 25,000 vectors/s and 1280 x 1024 pixel resolution on a 19-in. screen with 1024 simultaneously displayed colors drawn from a palette of 32,768. D-SCAN units are priced from $5000 to $19,000. **Seiko Instruments**, 1623 Buckeye Dr, Milpitas, CA 95035.
Circle 352

Raster-scan display is marked by 1000-line video resolution

A high performance raster-scan monochrome CRT display, the 15DD977, offers high resolution for critical applications. This 15-in. display is available with both composite video and TTL input. It features 1000-line horizontal resolution, 30-MHz video bandwidth, and horizontal scanning frequency of 15.75 kHz standard with options of up to 31.5 kHz. **Audiotronics**, 7428 Bellaire Ave, North Hollywood, CA 91605. **Circle 353**



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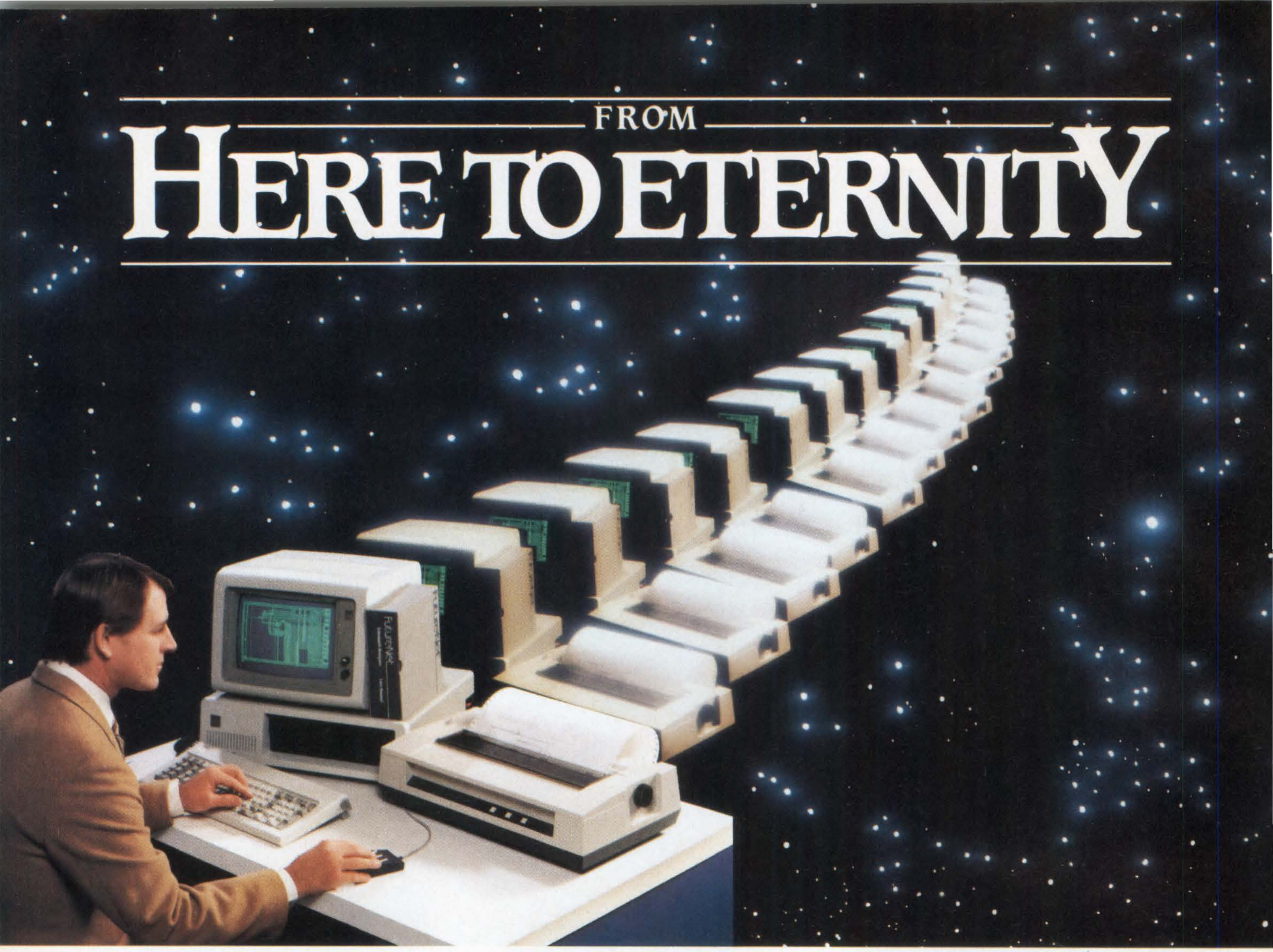
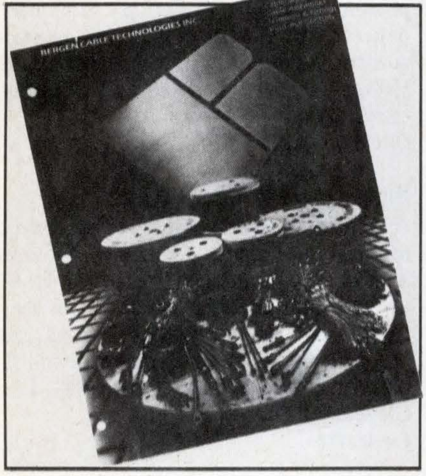

FROM
HERE TO ETERNITY

Cabling data



Full-line catalog deals with cable and related assemblies in 20-page format. General data includes part numbers, construction, diameter, material, and breaking strength. **Bergen Cable Technologies, Inc,** Lodi, NJ. **Circle 410**

Family of STD bus units

Combination design manual and product listing provides specs and data sheets on series 7000 STD bus line that includes memory and I/O cards, motherboards, card racks, and power supplies. **Pro-Log Corp,** Monterey, Calif.
Circle 411

Monolithic A-D/display driver

Application note outlines how to expand a system's measurement range by combining a 13-bit, microprocessor-compatible CMOS LSI A-D converter with software and a CMOS display driver; the design forms a 3¾-digit DVM. **Teledyne Semiconductor,** Mountain View, Calif.
Circle 412

Interconnect cabling

Guidelines for selecting and installing coax, twinax, triax, and quadrax cabling in computer networks and data distribution systems are highlighted in 50-page catalog. **Trompeter Electronics Inc,** Chatsworth, Calif. **Circle 413**

Stepping motors

Bulletin details hybrid permanent-magnet stepping motors with 2.2-, 3.4-, and 4.2-in. outer diameters; design considerations, performance parameters, and application examples are included. **Sigma Motion Control,** Braintree, Mass.
Circle 414

Optical memory

Brochure explains the laser-based, optical memory process and spotlights firm's own Gigadisc memory systems. Specs depict SCSI-compatible devices that guarantee over 10 years of storage life with very high levels of data compression. **Thomson-CSF Communications, Inc,** El Segundo, Calif.
Circle 415

Benchmark of LANs

Study consists of test results from benchmarks conducted on several local area networks (LANs); provides speed comparisons using NetWare and native network operating systems; limited supply of complimentary copies available upon request on company letterhead. **Novell Inc,** 1170 N Industrial Park, Orem, Utah 84057

Vision system applications

The KR-95 line of image recognition and inspection systems is profiled in a four-page, four-color brochure; sorting, reading, measuring, and counting operations are outlined. **Key Image Systems, Inc,** Chatsworth, Calif.
Circle 417

Programmable controllers

An eight-page brochure profiles mid- and large-size programmable controllers in the 584 line. Flexible I/O, ASCII-compatibility, and enhanced communications are highlighted. **Gould Inc, Programmable Controller Div,** Andover, Mass.
Circle 418

Field maintenance

A 13-page guide lists 118 independents, manufacturers, and corporate divisions providing third party maintenance for most electronic and computer products, plus the companies' geographic scope, number of locations, and types of service offered. **Assn of Field Service Managers,** Fort Myers, Fla.
Circle 419

Data acquisition/control system

Brochure details system, software, and applications for CompuDAS 3, programmable data acquisition and control system that functions like a high speed data logger when hooked up with powerful desktop computer and programmable controllers. **Ithaco, Inc,** Ithaca, NY.
Circle 420

Electronic components

Illustrated, 102-page electronic components catalog provides tab-indexed sections on metal film resistors, ceramic and glass capacitors, and solid tantalum capacitors; each section has introductory product line overview. **Corning Glass-works,** Corning, NY. **Circle 421**

Brushless motors

Technical bulletin describes 1.5-in. brushless motors ideally suited for computers, robotics, machine tools, plus military and aerospace applications; bulletin contains electrical, mechanical, and thermal performance data. **Harowe Servo Controls, Inc,** West Chester, Pa. **Circle 422**

Supplies for CAD/CAM

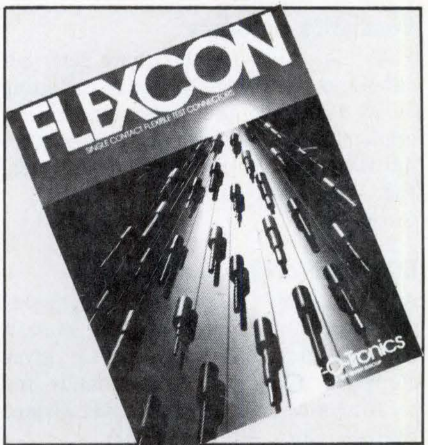
Computer graphics support supplies (eg, wet ink and disposable ink pens, plotter papers, and related products) are listed in a 24-page pricing catalog. **Matrix Resources,** Dayton, Ohio.
Circle 423

Data comm gear

Data communication products, systems, and services are described in this comprehensive 32-page catalog, which includes data encryption products, modems, multiplexers, net management systems, protocol translators, and communication controllers. **Racal-Milgo,** Miami, Fla.
Circle 424

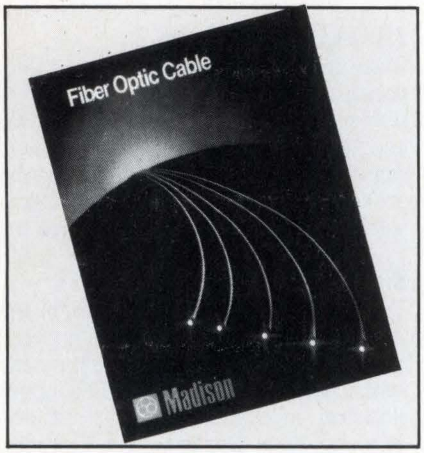
Flexible connectors for testing

Four-page brochure highlights flexible test connectors for continuity, signal, and voltage testing of telecommunication and computer equipment. Diagrams show both pin and socket flexible models. **Air-O-Tronics,** Cazenovia, NY.



Circle 425

Optic cables include hybrids



Illustrated 8-page fiber optic catalog features standard and customized single-, dual-, and multiple-channel fiber optic bulk cables, including hybrids that combine copper and fiber. **Madison Wire & Cable Corp,** Danielson, Conn.
Circle 426

Performance measurement

Two data sheets explain performance monitors: the Multipoint Network Design (MND), which is a tool for use on SMART performance measurement systems; and the MS-SMART Bridge software and hardware enhancement to the MS system. **Tesdata Systems Corp,** McLean, VA.
Circle 427

Optical fiber standard

Copies are available of the Recommended Standard RS-458-A for development of optical waveguide communication systems and associated components. This is a revision of RS-458 and includes RS-459. It costs $7. **Electronic Industries Assn, Standard Sales Dept,** 2001 Eye St, NW, Washington, DC 20006.

Simulation software

Full-color, nine-page brochure describes simulation software systems including SLAM II, MAP/1, and TESS; capabilities, applications, and necessary computer hardware are outlined. **Pritsker & Assoc, Inc,** West Lafayette, Ind.
Circle 429

Reference card for MPL

A programmer's reference card highlights commands and capabilities of the Motion Programming Language (MPL); gives complete overview of commands for creating motion control routines. **Ormec Systems Corp,** Rochester, NY.
Circle 430

Converters for dc-dc

Product handbook includes comprehensive data on dc-dc converter line; power supply characteristics are presented in 32-page format that includes selection tables followed by engineering data on models, a glossary, and tutorial section. **Power General,** Canton, Mass.
Circle 431

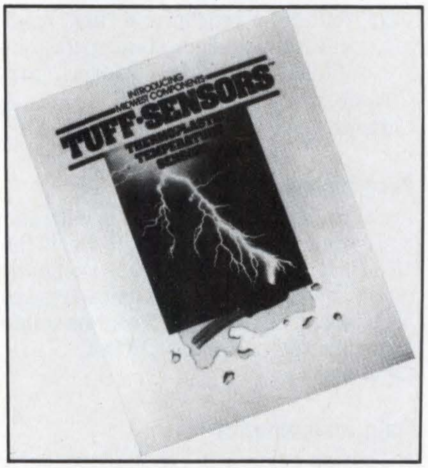
Frequency band translator

Literature describes System 1776, a multichannel programmable frequency band translator; this technical sheet details product features, operations, options, and accessories. **Precision Filters, Inc,** Ithaca, NY.
Circle 432

Educational kits

Heathkit educational catalog includes listings of new products for learning CAD, passive circuit design, and robotics. **Heath Co,** Benton Harbor, Mich.
Circle 433

Hermetically sealed temp sensors



Sensing elements are the focus of the TUFF SENSOR catalog. Technical issues for probe design in harsh environments are discussed. **Midwest Components, Inc,** Muskegon, Mich.
Circle 434

Contacts and connectors

Catalog is 40 pages long and details test data and specs for line of IC sockets, connectors, contactors, and carriers; includes 20 families of production and burn-in/test sockets, card edge and D-subminiature connectors, as well as contactors and carriers for flatpack, quad pack, DIP, and TO-5 devices. **Wells Electronics, Inc,** South Bend, Ind.
Circle 435

Fiber optic cable

Hard-clad silica fiber optic cable products are introduced in an eight-page pamphlet; products have use in various short-haul data communication applications, process control, and local area networking. **Ensign-Bickford Industries, Inc,** Simsbury, Conn.
Circle 436

High accuracy measurement

Available application notes on electronic test and measurement issues are listed in a two-page bulletin. The notes cover topics that include static charges in electronic manufacturing, capacitor leakage measurements, and switching in multipoint testing. **Keithley Instruments, Inc,** Cleveland, Ohio.
Circle 437

Signal processing

Twelve-page document describes operation and architecture of SPS-1000 digital processor; diagrams, text, and specs outline these devices, which are useful for time delay measurement, communication, image processing, and simulation, among other applications. **Signal Processing Systems, Inc,** Waltham, Mass.
Circle 438

Power conditioning

Beginning with a consideration of irregular voltage causes, this illustrated power-conditioning brochure covers 24 pages; products detailed include micro/minicomputer regulators, constant voltage transformers, and Solatron/Acuvolt regulators for static-magnetic high power applications. **Sola Electric,** Elk Grove Village, Ill.
Circle 439

Dual-inline switches

Four-page technical bulletin describes 8-pin, 14-pin, and 16-pin DIPSWITCHES®. Specs on these subminiature rotary shaft-operated dual-inline switches are augmented with sample programs, shaft options, and panel mounting information. **Armtec Industries, Inc, Daven Components Group,** Manchester, NH.
Circle 440

Electrostatic discharge

An 18-page, illustrated catalog studies approaches to electrostatic discharge problems; products listed include surfaces for assembly and testing, as well as packaging materials. **Charleswater Products, Inc,** West Newton, Mass.
Circle 441

CONFERENCES

AUG 19-24—Technical Symposium on Optics and Electro-Optics and Instrument Display, Town & Country Hotel, San Diego, Calif. INFORMATION: Rich Donnelly, Information Services, SPIE, PO Box 10, Bellingham, WA 98225. Tel: 206/676-3290

AUG 21-24—Conf on Parallel Processing, Hilton Shanty Creek, Bellaire, Mich. INFORMATION: Tse-yun Feng, 1604 Stormy Ct, Xenia, OH 45385. Tel: 614/422-1408

AUG 30-SEPT 1—Conf on Solid State Devices and Materials, Kobe, Hyogo, Japan. INFORMATION: Susumu Namba, Osaka Univ, Faculty of Engineering Science, Toyonaka, Osaka, Japan 560.

SEPT 5-8—Conf on Digital Signal Processing, Florence, Italy. INFORMATION: A. G. Constantinides, Dept of Electrical Engineering, Imperial College of Science & Technology, Exhibition Rd, London SW7 2BT, England. Tel: 01/5895111

SEPT 10-13—Advanced Control Conf, Purdue Univ, W Lafayette, Indiana. INFORMATION: Theodore J. Williams, Director, Purdue Laboratory for Applied Industrial Control, W Lafayette, IN 47907. Tel: 317/494-7434

SEPT 11-13—Midcon Electronics Exhibition and Convention, Dallas Convention Ctr, Dallas, Tex. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 11-13—Mini/Micro-Southwest Computer Conf and Exhibition, Dallas Convention Ctr, Dallas, Tex. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 11-13—Voice Input/Output System Applications Conf, Marriott Crystal Gateway Hotel, Arlington, Va. INFORMATION: Robert Burgess, Public Information Office, Lockheed Missiles & Space Co, Inc, Sunnyvale, CA 94086. Tel: 408/742-6688

SEPT 16-19—World Congress on Human Aspects of Automation, Hotel du Parc, Montreal, Quebec, Canada. INFORMATION: Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. Tel: 313/271-1500

SEPT 16-20—Compcon Fall, Hyatt Regency Crystal City, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SEPT 17-21—FOC/LAN (Fiber Optic Communications and Local Area Networks) Exposition, MGM Grand Hotel, Las Vegas, Nev. INFORMATION: Michael O'Bryant, Information Gatekeepers, Inc, 138 Brighton Ave, Suite 212, Boston, MA 02134. Tel: 617/787-1776

SEPT 19-21—Connector and Interconnection Technology Symposium, Disneyland Hotel, Anaheim, Calif. INFORMATION: Electronic Connector Study Group, Inc, PO Box 167, Fort Washington, PA 19034. Tel: 215/279-7084

SEPT 26-28—Eurocon: Computers in Communications & Control, Brighton, England. INFORMATION: Brian Atkinson, IEE, Savoy Place, London, WC2R OBL England.

OCT 1-4—AUTOFACT 6 Conf & Exhibit, Anaheim Convention Center, Anaheim, Calif. INFORMATION: Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0777

OCT 2-4—Northcon Electronics Conf & Exhibit, Seattle Center Flag Coliseum, Seattle, Wash. INFORMATION: Nancy Hogan, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

OCT 2-4—Mini/Micro Northwest Conf & Exhibit, Seattle Center Flag Pavilion, Seattle, Wash. INFORMATION: Nancy Hogan, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

OCT 8-10—9th Conf on Local Area Networks, Minneapolis, Minn. INFORMATION: Harvey A. Freeman, Architectural Technology Corp, PO Box 24344, Minneapolis, MN 55424.

OCT 8-10—ACM Annual Conf: The Fifth-Generation Challenge, San Francisco Hilton Hotel, San Francisco, Calif. INFORMATION: Karen Duncan, Chairman, ACM '84, 15 Parsons Way, Los Altos, CA 94022.

OCT 10-12—Design Automation Workshop, East Lansing, Mich. INFORMATION: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

OCT 10-12—LOCALNET '84, Sheraton Harbor Island Hotel, San Diego, Calif. INFORMATION: Online Conferences, Inc, Suite 1190, 2 Penn Plaza, New York, NY 10121. Tel: 212/279-8890

OCT 15-17—The Future of Optical Memories, Loew's Summit Hotel, New York, NY. INFORMATION: Joanna Spilman, Technology Opportunity Conference, PO Box 14817, San Francisco, CA 94114. Tel: 415/626-1133

OCT 15-18—Conf on Ada Applications & Environments, Sheraton Midway Hotel, St. Paul, Minn. INFORMATION: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

OCT 16-19—Int'l Test Conf (Cherry Hill '84), Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

OCT 22-26—Annual Industrial Electronics Conf (IECON '84), on Industrial Applications of Microelectronics, Keio Plaza Intercontinental Hotel, Tokyo, Japan. INFORMATION: Frank A. Jur, Bechtel Corp, 45 Fremont St, MS 45/17A26, San Francisco, CA 94109. Tel: 415/768-3023

OCT 30-NOV 2—Wescon Electronics Exh and Conf, Anaheim Convention Center, Anaheim, Calif. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SHORT COURSES

AUG 1-3, Hartford, Conn; AUG 8-10, Boulder, Colo; AUG 15-17, Honolulu, Hawaii—Network Communication Protocols. INFORMATION: Center for Advanced Professional Education, 1820 E Garry St, Suite 110, Santa Ana, CA 92705. Tel: 714/261-0240

AUG 14-17—VLSI Design Technology, Los Angeles, Calif. ARC Educators, 2847 Deep Canyon Dr, Beverly Hills, CA 90210. INFORMATION: Earl Swaartzlander, TRW, 1 Space Pk, Redondo Beach, CA 90278. Tel: 213/535-4177.

AUG 20-24—Hands-on Programming in Ada, George Washington Univ campus. INFORMATION: George Harrison, The George Washington Univ School of Engineering and Applied Science, Washington, DC 20052. Tel: 800/424-9773

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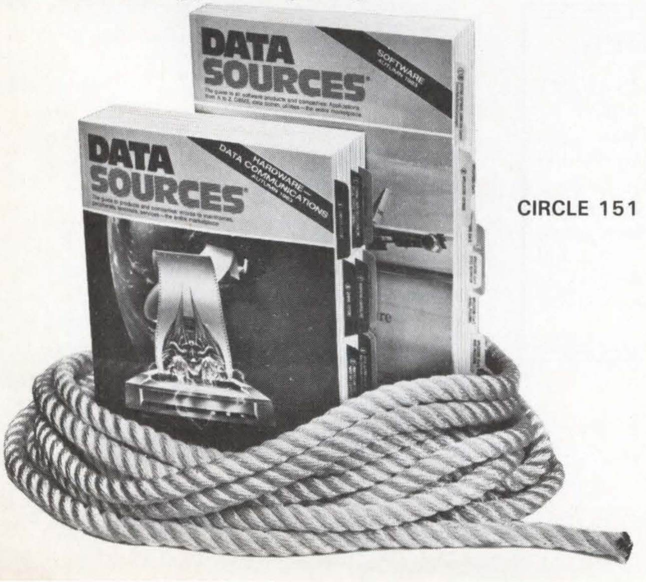

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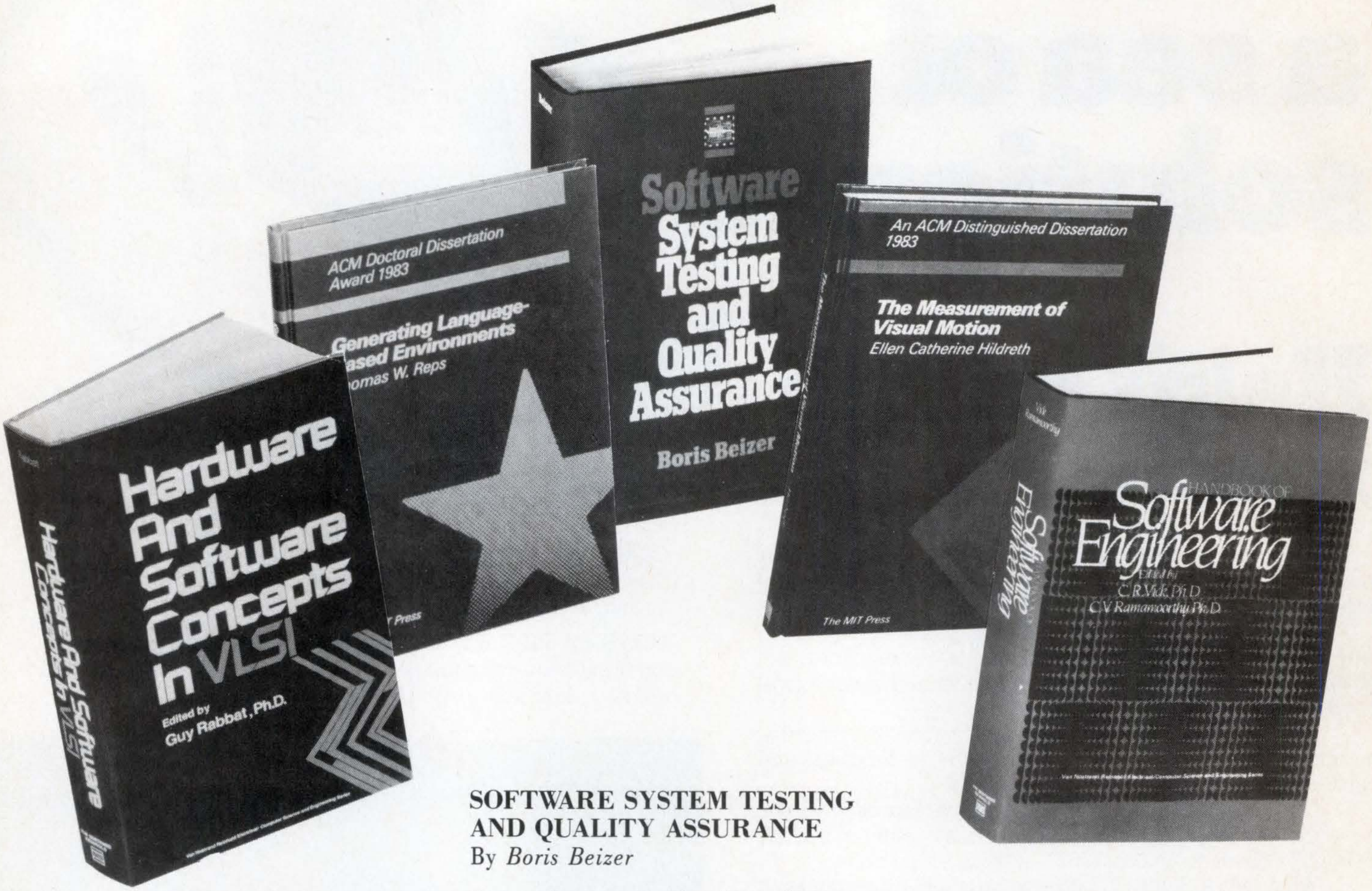

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For years, the quality of computer graphics has been limited by the resolution of display monitors. But at Ikegami, we're making it easy for your system to live up to its images with our new DM-2050 60-Hz noninterlaced superhigh resolution RGB monitor. Sporting a 1280 x 1024 pixel display and 100-MHz-plus video bandwidth, it gives you reliability and stable operation, eliminating the need for a long-persistence phosphor.

Simpler is better
How did we do it? By keeping it simple. And that we did. The chassis of our new DM-2050 is a marvel of compact, modular and functional design. In fact, Ikegami's unique design configures all the circuit boards by function within the chassis.

Keeping cool
We also took some steps to make sure our monitors wouldn't blow your designs. For example, we made the DM-2050 run so cool it doesn't require a blower. That means your monitor will never overheat because of blower failure. It also means the DM-2050 is lighter and more efficient.

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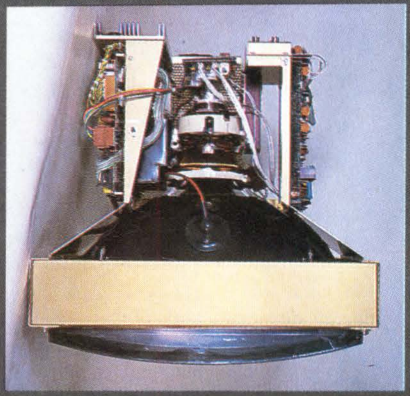
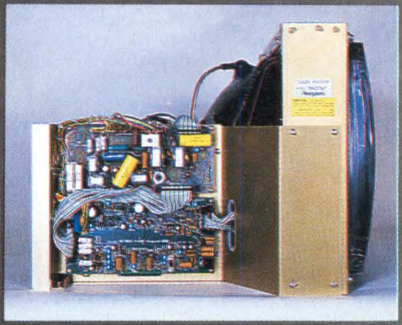
Along with meeting these time-honored Ikegami standards of simplicity and reliability, we also made our new 64-KHz monitor meet a few others along the way. Like UL, DHHS, CSA, IEC, FCC and VDE standards for safety and emissions. Now you can put the same monitor in every system you sell no matter where in the world it is used.



Keeping a low profile
But no matter what system you put the DM-2050 into, you know it will always fit in. The unique packaging of the DM-2050 fits right into CDA 19V enclosures. So in many cases, you won't have to change your existing design. And its extremely compact size gives you a free hand in new designs.

The price is right
You might think that a superhigh resolution monitor as advanced as your designs would come at a state-of-the-art premium. But the DM-2050 won't put a drain on your system's resources. In fact, Ikegami will make your profit picture look even better, because it's a finished product with on-time delivery.



In addition to the DM-2050, Ikegami makes a full line of color and monochrome monitors for virtually all OEM applications. For information, contact Ikegami Electronics (U.S.A.), Inc., 37 Brook Avenue, Maywood, NJ 07607; (201) 368-9171. In the West, 3445 Kashiwa Street, Torrance, CA 90505; (213) 534-0050.

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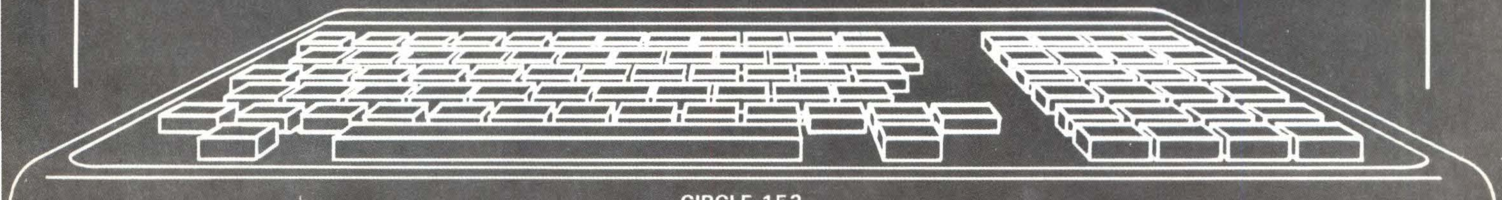

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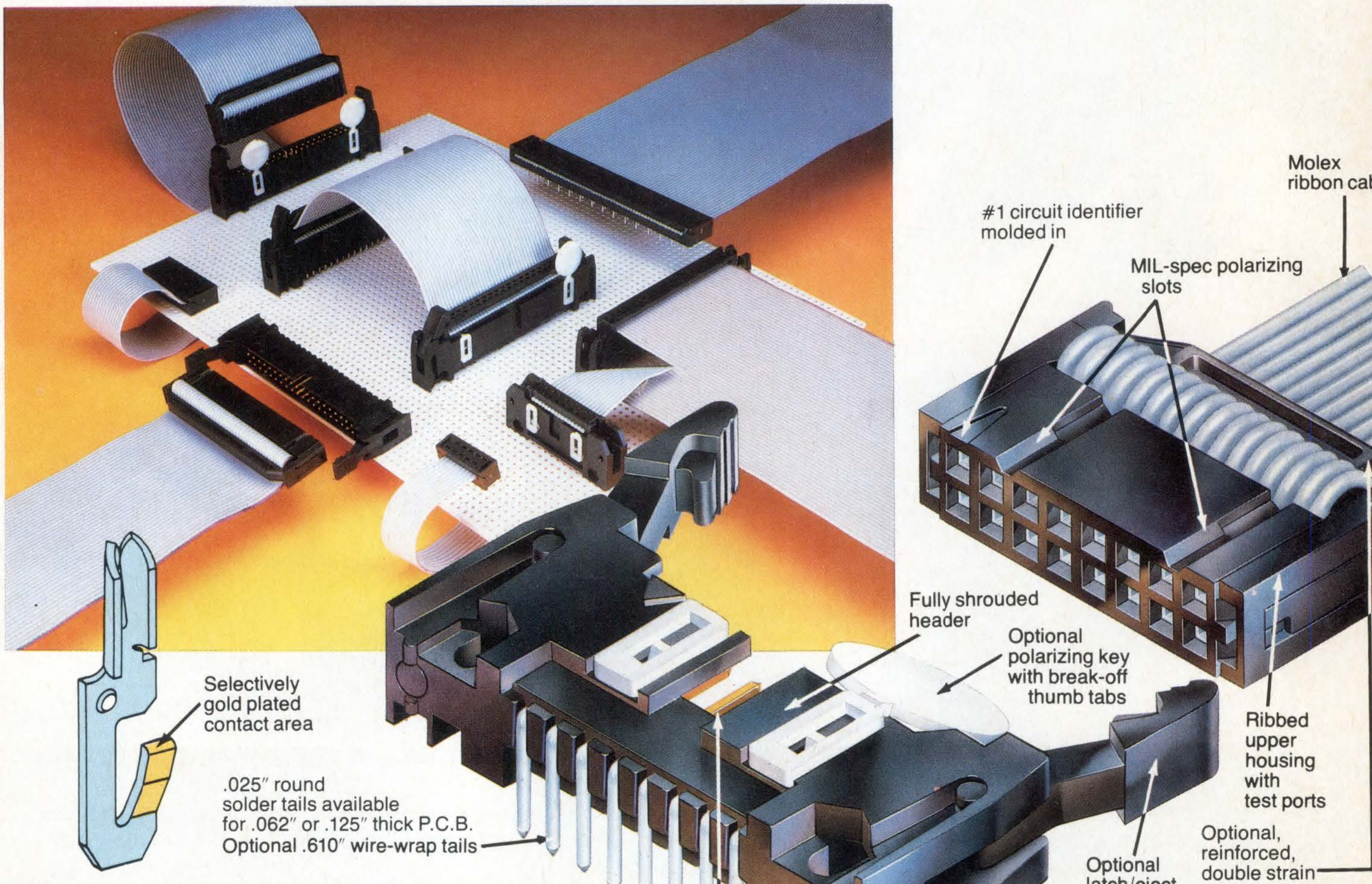
The Molex MX50™ flat cable system meets or exceeds MIL-C-83503.



The electronics industry has focused on military specification MIL C-83503 as its standard for .050″ (1,27mm) centerline ribbon cable connectors and headers.

The primary feature of this specification is the method of polarization. The new Molex MX50™ system has polarizing ribs on the header and corresponding mating slots on the connector.

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Molex also provides easy-handling, semi-automatic production tools for cost-saving application.

For more information on our MX50 ribbon cable system and the many ways Molex can help you lower your total applied costs, contact the Molex office nearest you.

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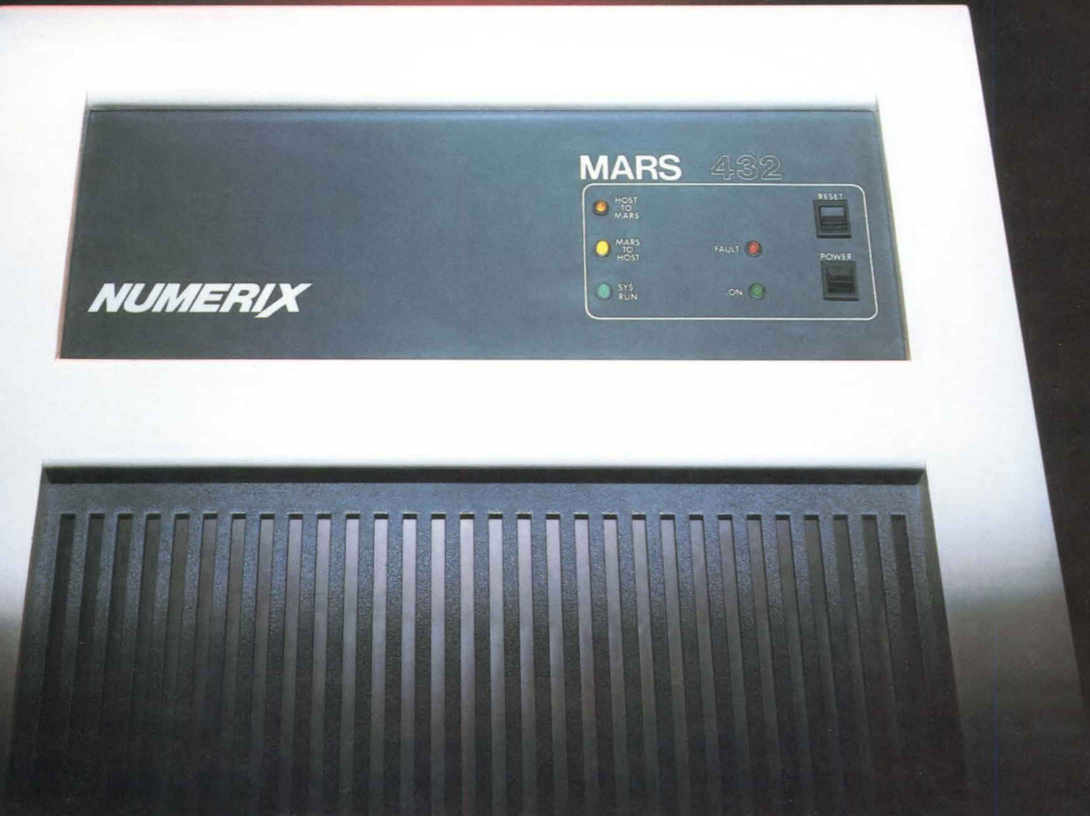

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Program and data memories compatible with programs written for today's array processor applications.

MARS-432 Array Processor Software
An architecture specifically designed to support a FORTRAN compiler and other software development tools.

The state of the art in 32-bit floating point array processors. Direct addressability of up to 16 million words (64 megabytes) of data memory and direct access to the high-speed internal data bus assure the user of highest throughput rates.

MARS-432 Array Processor Features Include:

- Add and multiply times of 100ns
- Computational power of 30 megaflops
- Computes a 1024-point complex FFT in 1.7ms
- DMA transfers at I/O bus rates of 20 megabytes/sec
- Data memory read or write in 100 ns
- Memory paging for uninterrupted processing during I/O transactions.

Program Memory
Virtual and physical address space of 4K words – standard. Expanded configuration uses a 4K cache memory to extend total memory to 64K words.

Data Memory
Data I/O is supported by DMA transfers into data memory with a physical address space of 16 million words. A data memory page-loading feature provides the option of zero overhead background loading of data during time critical program execution. No DMA cycle stealing overhead is incurred. Uninterrupted processing can occur simultaneously with high-speed I/O transfers.

FORTRAN Development System (FDS)
FORTRAN compiler, linker, and trace/monitor provide high-level language access to the MARS-432.

Microcode Development System
Off-line development package includes macro-assembler, microcode diagnostics, and a unique utility for automatic microcode optimization.

AP Run Time Executive Support Package (AREX)
As the interface to the MARS-432 at run time, AREX provides processor initialization, I/O operations, and array function execution.

Applications Libraries
Extensive applications libraries include math, signal processing, and image processing.

NUMERIX

For additional information on the MARS family of high-speed Array Processors, write or call:
Numerix Corp., 320 Needham Street, Newton, MA 02161 Tel. 617-964-2500 TELEX 948032

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