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COMPUTER DESIGN

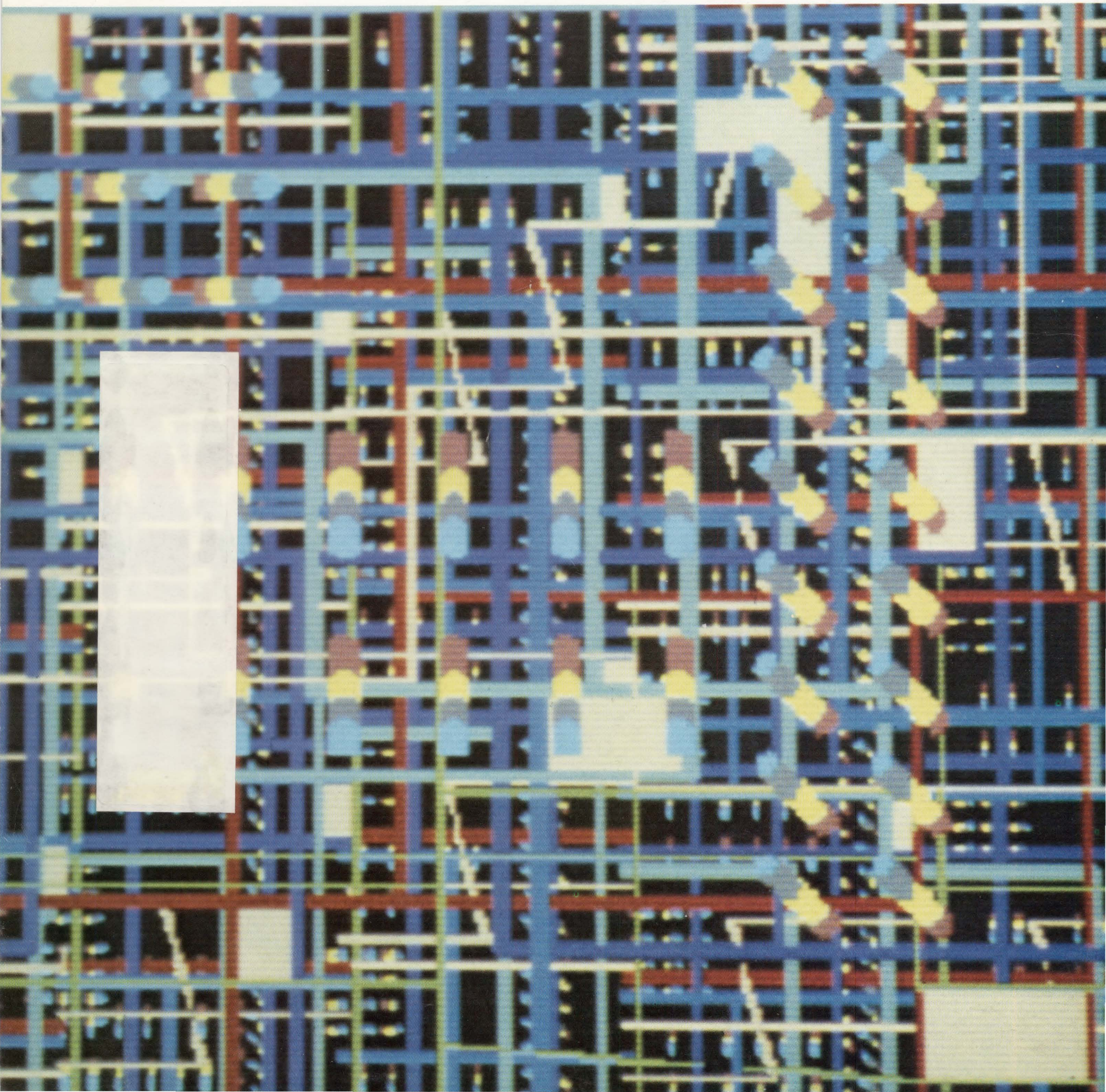
THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

AUGUST 1981

IN-CIRCUIT TESTING COMES OF AGE

PARALLEL CHANNEL PROCESSING OVERLAPS DATA ACQUISITION AND REDUCTION

TOUCH-SENSITIVE SCREENS ENSURE A USER FRIENDLY INTERFACE



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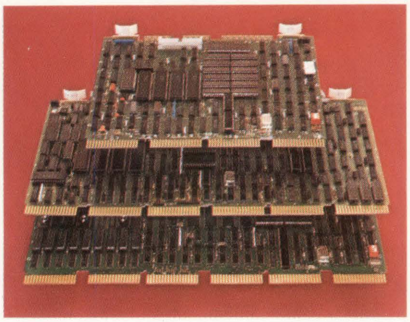
Now there's an advanced technology family of single board controllers for DEC* computers from Western Peripherals—the number one name in controllers.

The TC-131 (for PDP-11s*) is the first TM-11 emulating controller to combine PE and NRZ on one standard hex board. It lets you mix 9-track, PE, NRZ or dual density tape units in any combination up to 125 ips. A 64 byte data buffer allows installation at any point on the unibus without consideration of NPR priority.

The TC-151 single board NRZI tape controller interfaces any industry-standard drive to the LSI-11.* Add a dual width Phase Encode Board for the same performance as the TC-131.

The DC-231 accommodates up to four SMD disc drives of 40 to 600 mb each with RMO2 emulation. Its four sector (2048 bytes) data buffer makes "data-late" errors a thing of the past. The advanced technology "micro-engine" allows a complete track to be written on a single drive revolution. A measurable performance advantage for your PDP-11.



All three controllers are software compatible. All have self test. All are backed by one of the best factory service organizations in the business. And all can be delivered in 30 days.

For more information, call or write today: Western Peripherals Division, Wespercorp, 14321 Myford Road, Tustin, CA 92680, U.S.A. (714) 730-6250. TWX: 910 595-1775. CABLE: WESPER

Number 1 in controllers for DEC and Data General computers.

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CIRCLE 1 ON INQUIRY CARD

*Trade name of Digital Equipment Corporation.

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That's right. Ask any other supplier of peripheral products for system backup, and you'll find that some can supply a disk, some can supply a cartridge recorder, others a streaming transport. But none can supply the choice which Kennedy can offer.

Kennedy is the only company that can offer an SMD compatible, 8″ 40 MByte disk drive (Model 7300) and an 80 MByte 14″ Winchester disk drive (Model 5380). To back them up, Kennedy has a ¼″ cartridge recorder (Model 6450), and Model 6809, ½″ Data Streamer Tape Transport.

Kennedy was the first to utilize the ¼″ 3M cartridge for disk backup; Kennedy was the pioneer in Winchester disk technology, and was a leader in developing a low cost streaming tape drive.

All of these products were conceived and designed to meet the need for reliable, low cost backup — for our systems or for any other system.

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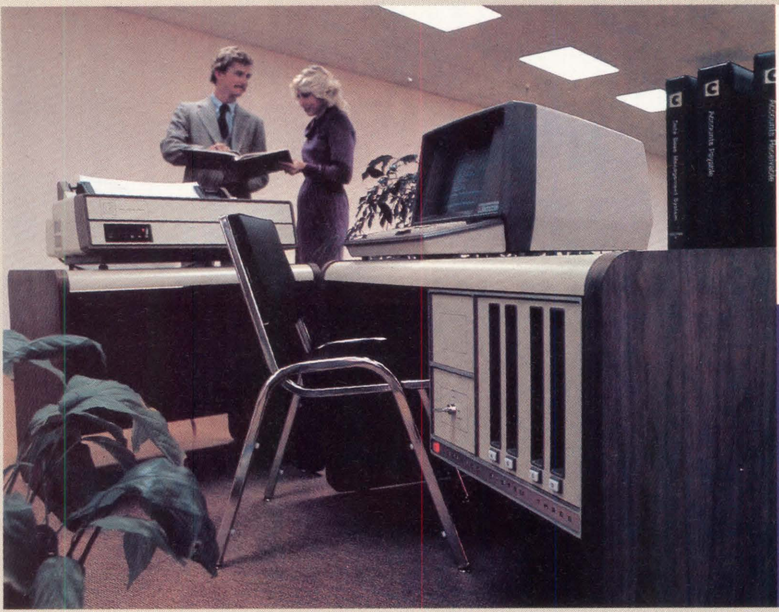
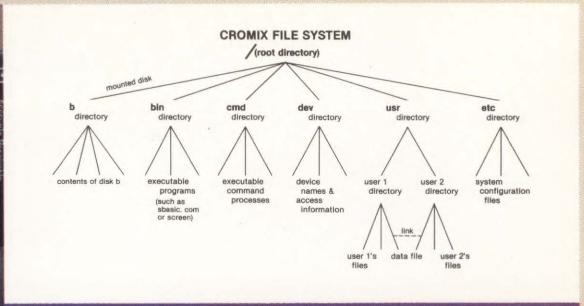
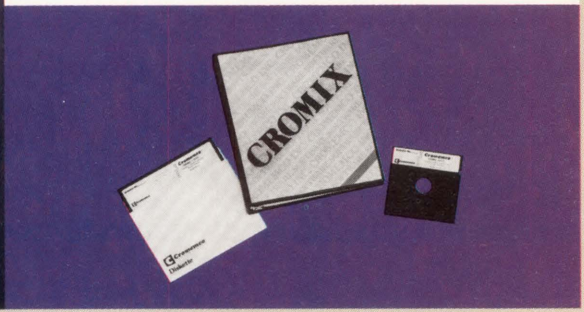
CIRCLE 2 ON INQUIRY CARD







CROMIX*— Cromemco's outstanding UNIX†–like operating system

CROMIX is just the kind of major development you've come to expect from Cromemco. After all, we're already well-known for the most respected software in the microcomputer field.

And now we've come up with the industry's first UNIX-lookalike for microcomputers. It's a tried and proven operating system. It's available on both 5″ and 8″ diskettes · for Cromemco systems with 128K or more of memory.

Here are just some of the features you get in this powerful Cromemco system:

- Multi-user and multi-tasking capability
- Hierarchical directories
- Completely compatible file, device, and interprocess I/O
- Extensive subsystem support

FILE SYSTEM

One of the important features of our CROMIX is its file system comprised of hierarchical directories. It's a tree structure of three types of files: data files, directories, and device files. File, device, and interprocess I/O are compatible among these file types (input and output may be redirected interchangeably from and to any source or destination).

The tree structure allows different directories to be maintained for different users or functions with no chance of conflict.

PROTECTED FILES

Because of the hierarchical structure of the file system, CROMIX maintains separate ownership of every file and directory. All files can thus be protected from access by other users of the system. In fact, each file is protected by **four separate access privileges** in each of the three user categories.

TREMENDOUS ADDRESS SPACE, FAST ACCESS

The flexible file system and generalized disk structure of CROMIX give a disk address space in excess of one gigabyte per volume — file size is limited only by available disk capacity.

Speed of access to disk files has also been optimized. Average access speeds far surpass any yet implemented on microcomputers.

'C' COMPILER AVAILABLE, TOO

Cromemco offers a wide range of languages that operate under CROMIX. These include a high-level command process language and extensive subsystem support such as COBOL, FORTRAN IV, RATFOR, LISP, and 32K and 16K BASICs.

There is even our highly-acclaimed 'C' compiler which allows a programmer fingertip access to CROMIX system calls.

THE STANDARD O-S FOR THE FUTURE

The power and breadth of its features make CROMIX the standard for the next generation of microcomputer operating systems.

And yet it is available for a surprisingly low $595.

The thing to do is to get all this capability working for you now. Get in touch with your Cromemco rep today.

*CROMIX is a trademark of Cromemco, Inc.
†UNIX is a trademark of Bell Telephone Laboratories

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CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN®

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

AUGUST 1981

VOLUME 20, NUMBER 8

DEPARTMENTS

Cover Artist: Darcy Gerbarg
Digital Video Graphics and Animation System by Aurora Imaging Systems, San Francisco, Calif

FEATURES

BPA

ABP

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CD* STAFF

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Peg Killmon **James W. Hughes**

Western Field Editor N. Calif & NW
(408) 371-8901
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Editorial & Executive Offices
11 Goldsmith St, Littleton, MA 01460
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ALSO FROM DATARAM
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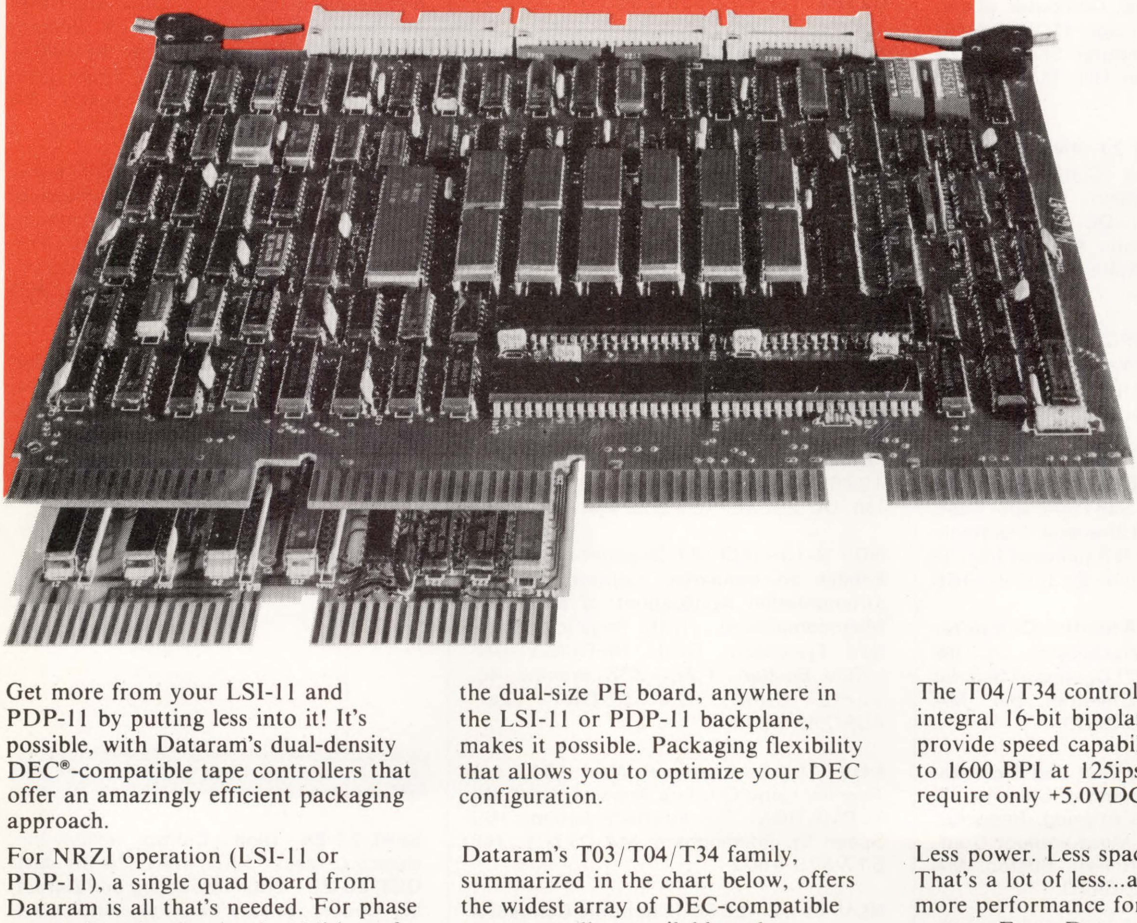

Get more from your LSI-11 and PDP-11 by putting less into it! It's possible, with Dataram's dual-density DEC®-compatible tape controllers that offer an amazingly efficient packaging approach.

For NRZI operation (LSI-11 or PDP-11), a single quad board from Dataram is all that's needed. For phase encoded mode, the simple addition of the dual-size PE board, anywhere in the LSI-11 or PDP-11 backplane, makes it possible. Packaging flexibility that allows you to optimize your DEC configuration.

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	NRZI	PE
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	T04 1 QUAD	
PDP-11	T34 1 QUAD	T34 1 QUAD and 1 DUAL

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CIRCLE 5 ON INQUIRY CARD

CALENDAR

CONFERENCES

AUG 31-SEPT 1—Software Mgmt, The 57 Park Plaza, Boston, Mass. INFORMATION: EFDPMA Confs, Dept SMC, PO Box 91295, Los Angeles, CA 90009. Tel: 213/670-2973

SEPT 9—NECOM '81, Marriott Hotel, Newton, Mass. INFORMATION: Margo Landrum, Norm De Nardi Enterprises, Suite 204, 289 S San Antonio Rd, Los Altos, CA 94022. Tel: 415/941-8440

SEPT 10-13—Midwest Computer Show, McCormick Place, Chicago, Ill. INFORMATION: The Nat'l Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

SEPT 14, OCT 1, OCT 27, AND OCT 29—Invitational Computer Confs: Newton, Mass; Minneapolis, Minn; Valley Forge, Pa; AND Washington, DC, area. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

SEPT 14-18—COMPCON FALL '81, Capital Hilton Hotel, Washington, DC. INFORMATION: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

SEPT 15-17—WESCON '81, Brooks Hall and Civic Auditorium, San Francisco, Calif. INFORMATION: Dale Litherland, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

SEPT 24-27—Mid-Atlantic Computer Show, DC Armory, Washington, DC. INFORMATION: The Nat'l Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

OCT 5-8—Electronics Test and Measurement Conf, Hyatt Regency, Chicago, Ill. INFORMATION: Dona Atwood, Registrar, Electronics Test and Measurement Conf, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

OCT 12-14—Conf on Local Computer Networks, Hilton Inn, Minneapolis, Minn. INFORMATION: Dr Abe Franck, Gen'l Chm, UCC, U of Minnesota, 227 Experimental Engineering, 208 Union St SE, Minneapolis, MN 55455

OCT 12-16—India Industrial Exhibition, Atlanta, Ga. INFORMATION: Alan Isacson, A. B. Isacson Assocs, Inc, 331 Park Ave S, New York, NY 10010. Tel: 212/475-1771

OCT 15-18—Northeast Computer Show, Hynes Auditorium, Boston, Mass. INFORMATION: The Nat'l Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

OCT 19-20—ACM Sym on the Impact of Small Computer Systems (Sigsmall), Orlando, Fla. INFORMATION: S. Ron Oliver, The MITRE Corp, 433 N Circle Dr, Colorado Springs, CO 80908. Tel: 303/471-0102

OCT 28-29—Western Computer Show, Calgary, Alberta. INFORMATION: Laurie Whitsed, Computing Equipment Assoc, 55 Bloor St W, Suite 1201, Toronto, Ontario M4W 3K2, Canada

OCT 29-NOV 1—Southeast Computer Show, Atlanta Civic Ctr, Atlanta, Ga. INFORMATION: The Nat'l Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

NOV 5, 12, AND 17—Invitational Computer Confs, Amsterdam, The Netherlands; Paris, France; AND Milan, Italy. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

NOV 9-11—ACM '81 (Assoc for Computing Machinery Conf and Expo), Bonaventure Hotel, Los Angeles, Calif. INFORMATION: ACM '81 Conf Info, PO Box 24059, Village Station, Los Angeles, CA 90024

NOV 9-12—Isratech '81, Binyanei Ha'ooma Conv Ctr, Jerusalem, Israel. INFORMATION: Joan Leavitt, Ruder & Finn, 1225 19th St NW, Suite 270, Washington, DC 20036. Tel: 202/466-7800

NOV 9-13—IECI '81 (Internat'l Conf and Exhibit on Industrial, Control, and Instrumentation Applications of Mini- and Microcomputers), Hyatt Regency Hotel, San Francisco, Calif. INFORMATION: LeRoy Bushart, FMC, 328 Brokaw Rd, Santa Clara, CA 95051. Tel: 408/289-3871

NOV 10-12—Interface West '81, Los Angeles Conv Ctr, Los Angeles, Calif. INFORMATION: The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

NOV 11-12—ECSG (Electronic Connector Study Group) Sym, Franklin Plaza, Philadelphia, Pa. INFORMATION: Jim Pletcher, Amp, Inc, Harrisburg, PA 17105. Tel: 717/780-8857

NOV 19-22—COMDEX '81, Las Vegas Conv Ctr, Las Vegas, Nev. INFORMATION: The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

DEC 15-19—Gulf Computer Exhibition, Dubai Internat'l Trade Ctr, Dubai, U.A.E. INFORMATION: Seymour House, 17 Waterloo Pl, London SEIY 4AR, England. Tel: 01/930-3881; OR Trade Ctr Mgmt Co, PO Box 9292, Dubai, U.A.E., Tel: 472200

SEMINARS

SEPT 14-16—Standard Architecture, Interface, and Protocols, New York Hilton Hotel, New York, NY. INFORMATION: McGraw-Hill Conf Ctr, 1221 Ave of the Americas, Suite 3677, New York, NY 10020. Tel: 212/997-3928

SEPT 17-18 AND 21-22 (dates tentative) AND SEPT 22-25—Design/Testing of Computer Devices per FCC Docket 20780; Product Safety Stds for Electronic Equipment; AND How to Meet VDE and emi Requirements for Computer and Other Electronic Devices, Chicago, Ill; Boston, Mass; AND Philadelphia, Pa. INFORMATION: Leonard Levin, R and B Enterprises, 1050 Colwell Ln, Conshohocken, PA 19428. Tel: 215/828-6236

OCT 6-7, NOV 2-3, AND NOV 5-6—Computing Applications in Engineering, Boston, Mass; Dallas, Tex; and Houston, Tex. INFORMATION: Educational Programs Mgr, Engineering Systems Group, MR1-1/M75, Digital Equipment Corp, 200 Forest St, Marlboro, MA 01752

OCT 13-15 AND NOV 17-19—Understanding and Using Computer Graphics, New York, NY, AND Atlanta, Ga. INFORMATION: Bob Sanzo, Dir of Marketing, Frost & Sullivan, Inc, 106 Fulton St, New York, NY 10038. Tel: 212/233-1080

SHORT COURSES

SEPT 23-25—Digital Control, Holiday Inn, Newton, Mass; AND **SEPT 28-30 AND OCT 26-28—Error Correcting and Detecting Codes,** Holiday Inn, Palo Alto, Calif, AND Arlington, Va. INFORMATION: Hellman Assocs, 299 S California Ave, Palo Alto, CA 94306. Tel: 415/328-4091

SEPT-NOV—Courses concerning emc, emi, and rfi, various cities and dates. INFORMATION: Don White Consultants, Inc, PO Box D, Gainesville, VA 22065. Tel: 703/347-0030

SEPT-DEC—Microprocessor Software, Hardware, and Interfacing; Computer Graphics; Hands-on Pascal Workshop; AND Distributed Processing, various cities and dates. INFORMATION: Cassie Mason, Integrated Computer Systems, Inc, 3304 Pico Blvd, PO Box 5339, Santa Monica, CA 90405. Tel: 213/450-2060

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DEC® designs great CPUs. But if you want 7.8 megabytes of disk storage, they give it to you in two ungainly boxes 21 inches high. Data Systems Design gives you one compact package 5¼ inches high, with an ultra-reliable 7.8 megabyte winchester drive *and* a 0.5 megabyte single-sided (or 1 megabyte double-sided) floppy for I/O and integral backup, plus on-board diagnostics and lots of extras.

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Fully compatible three ways.

DSD 880 is hardware compatible. And it integrates with any DEC LSI-11 or PDP-11 computer-based system.

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CIRCLE 6 ON INQUIRY CARD

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The most powerful general purpose logic analyzer you can buy for the years ahead.

It's here. Biomation K101-D. The first logic analyzer to combine high-speed 50 MHz data and 100 MHz time domain capabilities with advanced 48-channel recording. With enough powerful extras to demolish your toughest hardware/software integration problems—even on the most complex multiplexed microprocessor.

Fast, accurate software debugging.

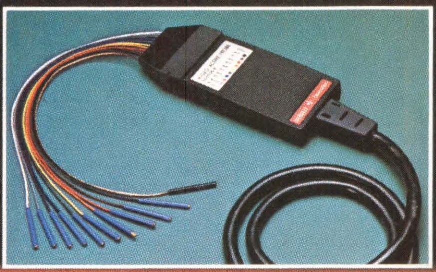
With its 50 MHz clock rate, 48-channel recording and 16 triggering levels, the K101-D isolates software bugs faster and more precisely than ever before. Sophisticated disassembly firmware generates precise mnemonics that cut analyzing time. And 12 external clocks (AND or OR) let you demultiplex 16-bit microprocessors, 16- and 32-bit minicomputers and bit-slice processors.

100 MHz high-speed hardware analysis.

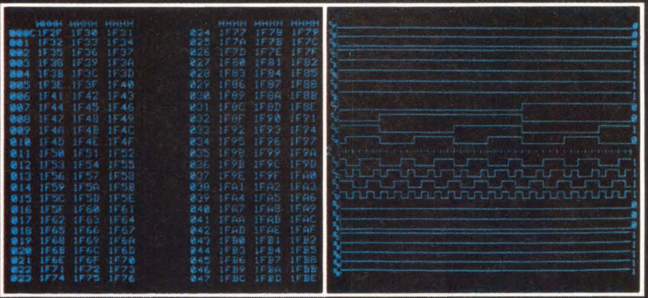
The K101-D's advanced high-performance hybrid probes let you capture glitches as narrow as 5 ns. And, with 48-channel recording, 515-word memory and 16-level triggering, you'll trap the data you need. The convenient display formatting and expansion simplify analysis.

Call now for a free demo.

See for yourself why the K101-D is a breakthrough in logic analyzers for the years ahead. For a demonstration or a copy of our detailed product brochure, write Gould Inc., Biomation Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For fastest response, call 408-988-6800.



For powerful software debugging, K101-D data domain capabilities include disassembly, 50 MHz clocking, 48-channel recording, 12 external clocks, 515-word memory, demultiplexing, 16-level trace control for triggering, 6 display code formats, and reference memory.

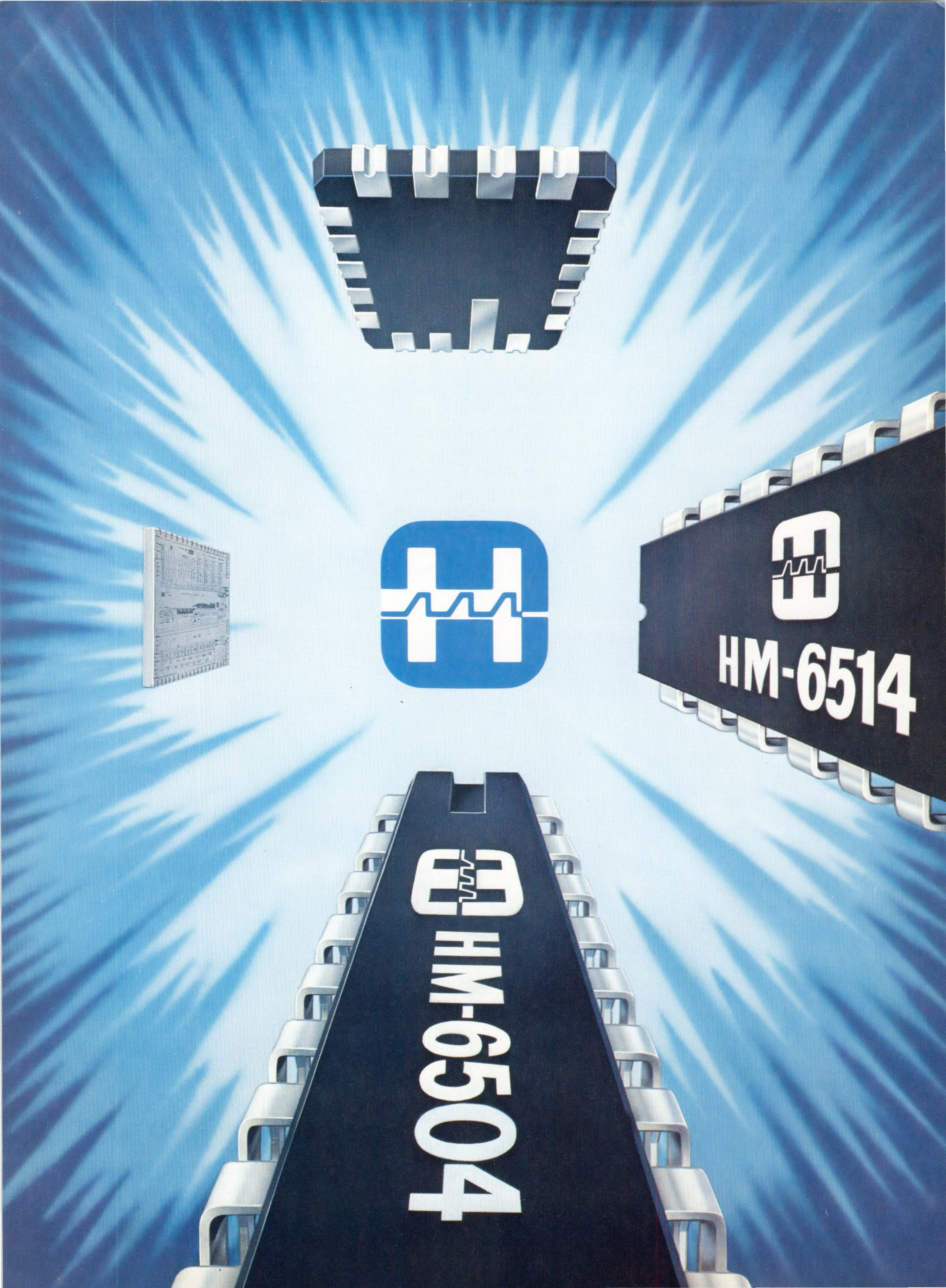


For powerful hardware debugging, K101-D time domain capabilities include 100 MHz clocking, 48-channel recording, 515-word memory, 5-ns glitch capture, 16-level triggering, channel labeling, new high-performance probe design, as well as horizontal and vertical display expansion for easy reading.

GOULD

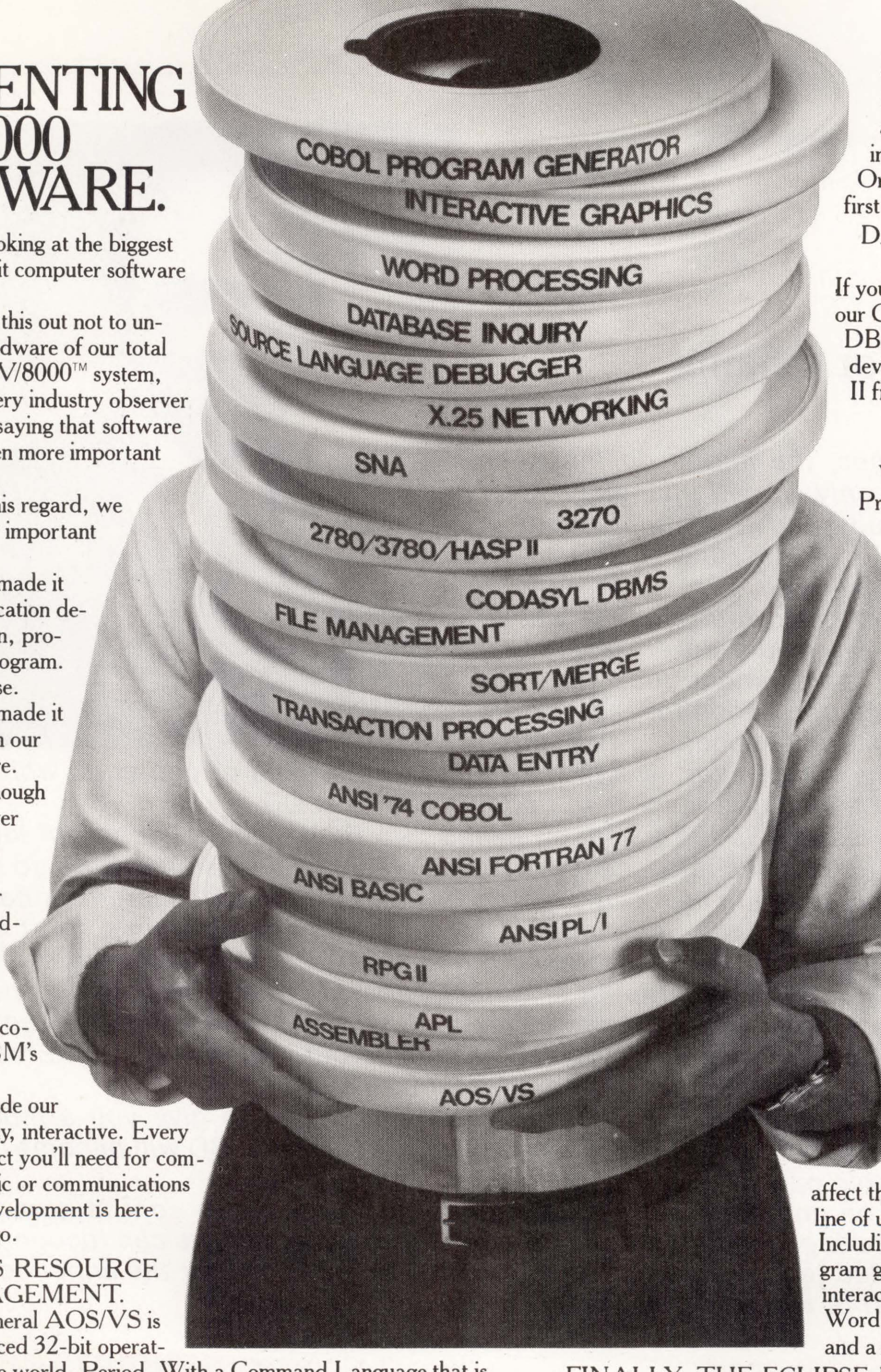
An Electrical/Electronics Company

CIRCLE 7 ON INQUIRY CARD


HM-6514
HM-6504

DO YOU REALIZE WHY THE OTHER 32-BIT COMPUTER COMPANIES ARE SHOWING OFF THEIR HARDWARE?

PRESENTING MV/8000 SOFTWARE.



You're looking at the biggest library of 32-bit computer software in the business.

We point this out not to underplay the hardware of our total ECLIPSE MV/8000™ system, but because every industry observer we've heard is saying that software has become even more important than hardware.

And in this regard, we have some very important software.

We have made it easier for application designers to design, programmers to program. And users to use.

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Wherever worldwide standards exist, we've followed them. (We're even peacefully coexisting with IBM's standards.)

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Here again you have a choice. If you're after productivity, you have our CODASYL-compliant, DG/DBMS software with design and development aids. Or our INFOS® II file management software.

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This is where you can affect the bottom line most. With our full line of user-friendly, interactive aids. Including an automatic COBOL program generator. TRENDVIEW™ interactive business graphics software. Word processing. Database inquiry and a source level language debugger.

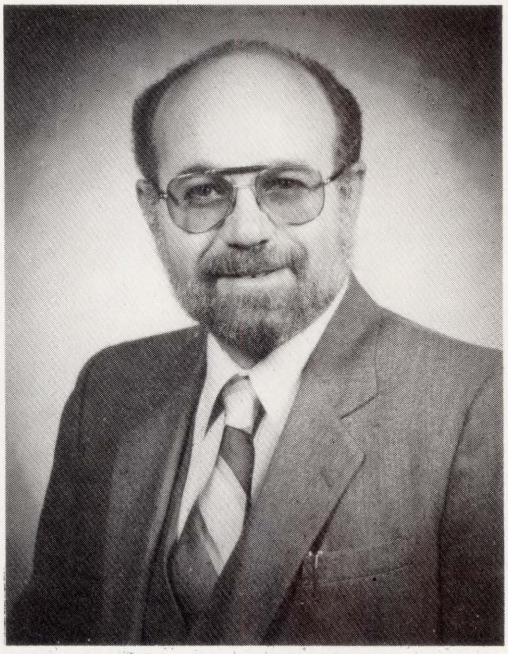
FINALLY. THE ECLIPSE MV/8000 HARDWARE.

If, after reading all this information about MV/8000 software you are disturbed to find nothing about the ECLIPSE MV/8000 systems hardware, write us at ISD Marketing Communications, Data General, 4400 Computer Drive, Westboro, MA 01580.

We will even include some very impressive four color photography of our 32-bit hardware. Just like you see on all the other pages of this publication.

Data General

CIRCLE 8 ON INQUIRY CARD



A Season for Change

As fall approaches, the leaves on the trees will not be the only things changing. After considerable study and a summer spent in redesign, CD will be sporting a brand new face starting next month.

The first, and most obvious, change will be the cover. Changes in the cover design will give us an even more unique look than our adoption of computer generated covers did about a year ago. The second, and next most apparent, change will be user oriented revisions to the table of contents, which will make it a lot easier and quicker to find everything in CD.

Next month's issue will add a section called "Up Front"—a collection of late breaking product and news releases, received as close as 3 days before we go to press. Since we are going to be moving quite a few things around to match our new table of contents design, the September "Up Front" will also contain a short introduction on how to find your way around the new CD. The interior layout of the editorial material is also undergoing a metamorphosis. This, however, will not become apparent until the October issue and will not be completed until November. This interior redesign is aimed at making our material easier to read and helping you to locate articles and product information.

In short, we are redesigning CD cover to cover in order to give you a more readable and useful product. We hope you will enjoy it and that CD will become an even more valuable part of your monthly technical reading.

Following up on my request in July's editorial for prospective contributors to CD, we are instituting, beginning now, a program through which we can recognize the best submitted technical article each month. See page 114 for the announcement and the list of winners for January, February, and March.

Saul B. Dinman
Editor

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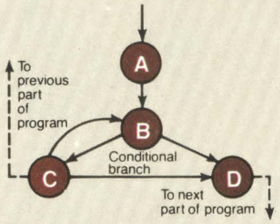
7D02 Solution: State and timing sections are included in a single logic analyzer, with each section able to trigger or qualify data acquisition by the other.

Design Problem: Monitoring I/O activity on the system bus.

7D02 Solution: Acquire both synchronous and asynchronous data through interactive triggering to examine both slides of an I/O transaction.

Design Problem: Tracking program flow through non-sequential algorithms with conditional branches to pinpoint an error.



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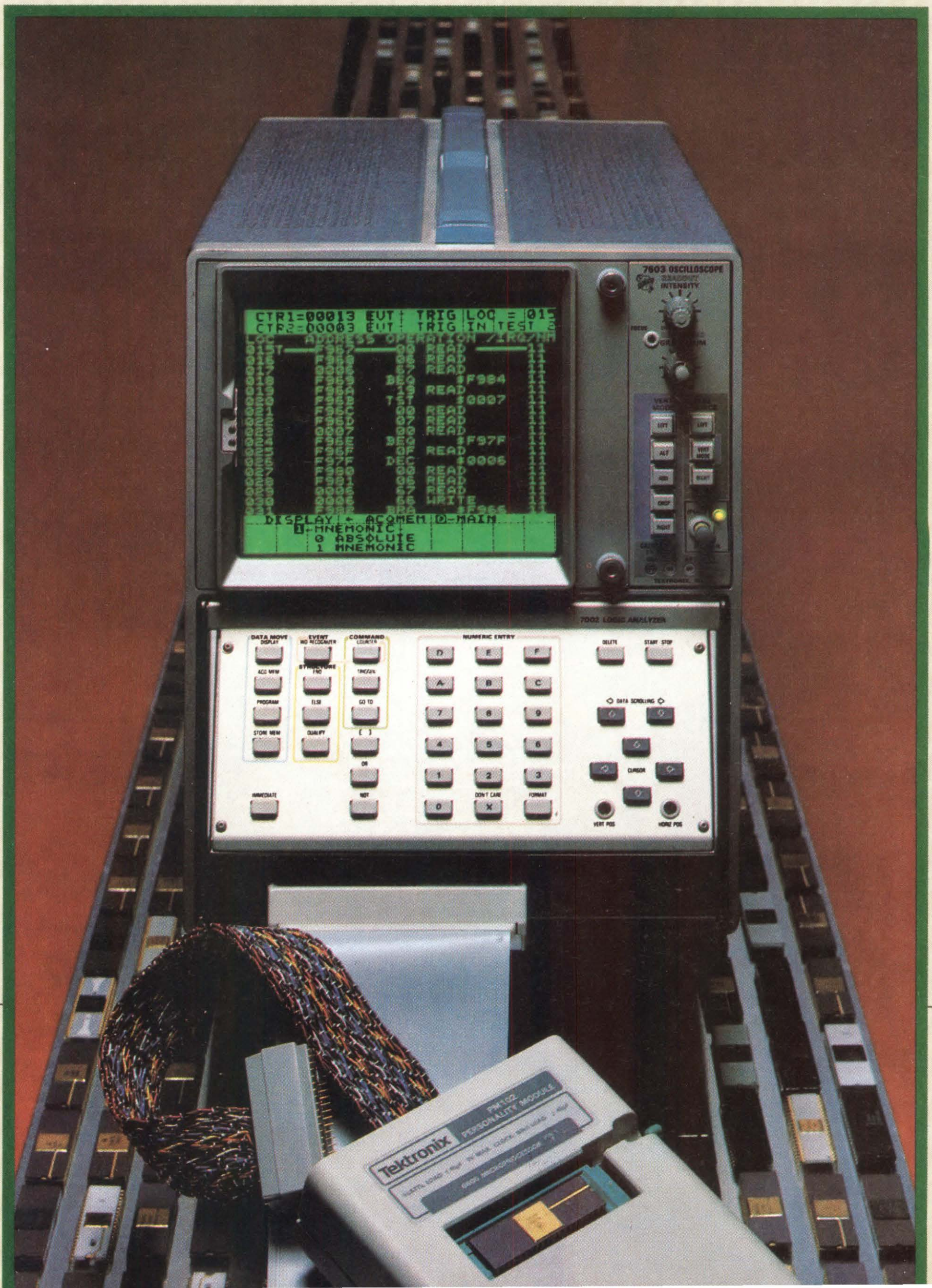

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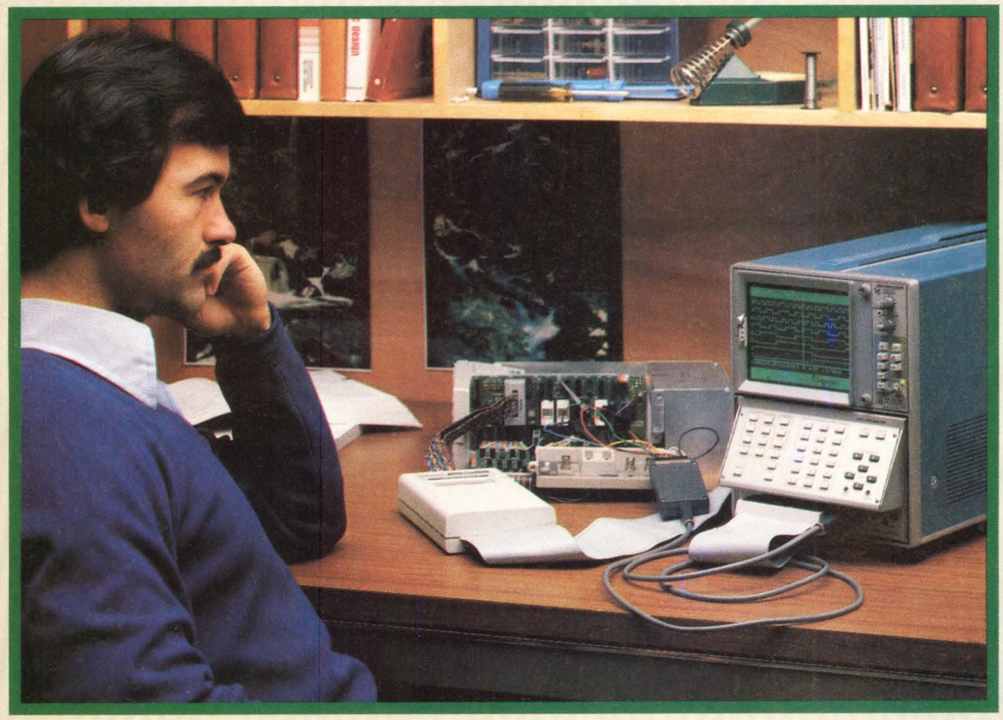

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Reliability/Availability of Wideband Local Communication Networks

D. G. Willard

The MITRE Corporation
Bedford, MA 01730

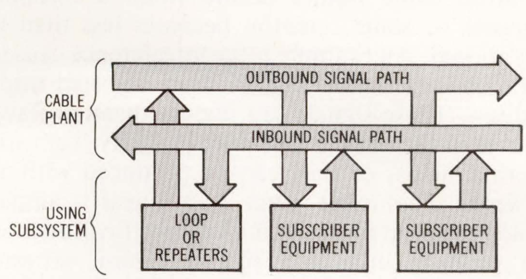

Fig 1 Network segments. Wideband distributed communication network consists of cable plant segment (either single- or dual-cable) and using subsystems (distributed subscriber equipment and centrally located signal processing devices)

The adolescent multimode broadband bus network technology provides operational benefits in local networks that are not possible with conventional communication methods. The very architecture of these systems, however, increases the risk of major consequences when single components fail. Happily, the architecture also provides an opportunity to implement comprehensive monitoring and control procedures at moderate cost. Recognizing potential failure modes, redesigning components to increase reliability, and incorporating certain monitor and control functions will result in a network that provides improved services with higher reliability than can be achieved with conventional communications alternatives.

Local area multimode bus networks can be thought of as consisting of two major system segments: the wideband medium ("cable plant") on which subscriber signals are exchanged, and the devices ("using subsystems") that interface subscriber equipment to the medium (Fig 1). Reliability of the bus network depends on the reliability of the individual components of these segments. Network availability, in turn, depends on the identification and repair procedures used to rectify failures.

Cable Plant Equipment: Failure Analysis

The community antenna television (CATV) cable plant that supports communication signals is usually implemented as tree, star, or a combination of these two basic architectures. Subscribers are effectively connected in parallel for the purpose of retrieving signals from and introducing signals to the network. Consequently, if a portion of the cable plant degrades, a large number of subscribers can be cut off from the network.

Among the major failure modes is a conductive short between center conductor and shield of the coaxial system. This is usually caused by direct shorts on the cable itself, but can be caused by failures in cable components such as taps, amplifiers, and splitters. Not only are the radio frequency (rf) signals prohibited from passing such a short circuit, but because 60-Hz ac is multiplexed onto the cable to power amplifiers, an increased load is drawn from the power supplies. Because commercial practice provides each power supply with overload protection, the ac is either reduced or totally removed.

Fault isolation is difficult under these conditions, since signal tracing techniques are ineffective on coaxial systems; reflectometer processes cannot be employed because the amplifiers are one-way devices for a single frequency. Amplifiers are also made inoperative by the lack of power. The isolation process is made more difficult; large segments of the cable plant are inoperative because many amplifiers are serviced by one power supply. Cable open circuits are similarly difficult to identify and to locate. They do not tend to pull down other segments of the otherwise properly operating cable plant, however, since power supplies are not overloaded.

Cable amplifiers are generally the only active components in the cable signal path and, as such, are primary contributors to the failure rate of local area CATV networks. Measured mean time between failure (MTBF) figures of 50 years have permitted one manufacturer recently to guarantee 20-year MTBFs. Experience has indicated, however, that amplifier failures are not evenly distributed. Failures tend to be bunched into the early (infant mortality) and late (old age) portions of the useful (guaranteed) lifetime. Although architectural design can minimize the effect of single-amplifier failures, many applications would suffer serious consequences if even a portion of the network became inoperative.

(continued on page 20)

Partial cable failure occurs when a component degrades or some function becomes less than fully operational. An example is the interference caused by extraneous rf signals and/or noise injected into the medium. These signals can ingress through flaws or failures in the coaxial shielding integrity from strong external fields, or they can be produced within the network. The cable plant is a linearly amplified analog medium in which out-of-specification stresses can produce undesired signals. These extraneous signals can interfere directly with acceptable signal detection and themselves contribute to additional system stress. Loose connections, poor solder joints and other intermittents, as well as unstable amplifiers—all can generate noise that will be propagated throughout the network.

Cable Plant Reliability Improvements

Fuses of appropriate value should be inserted throughout the cable plant so that those nearest a short will open. This action removes overload from the power supply and severs the segment of plant that includes the failure. Cable splitters that include provisions for power fusing and satisfy the fusing needs of most cable plant designs are available. This process permits the rest of the plant to continue in service but provides no direct indication of the occurrence or location of the shorting fault. Cable components can also fail "open," but in that case only the affected cable segment becomes inoperative.

Both short and open component failure cases can be automatically identified and isolated with a pilot monitoring subsystem. The basic function of the pilot monitoring process is to loop signals sequentially through selected portions of the cable plant while measuring each returned signal level. If a returned signal is not within tolerance, the integrity of the associated branch is suspect.

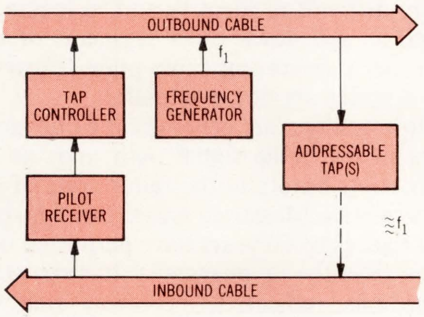

Fig 2 Basic pilot monitoring subsystem. Tap controller located at cable head end causes each remote addressable tap to close, looping only pilot frequency back to head end. Pilot receiver provides measurement of looped signal amplitude to controller for determination of abnormal operation in each branch of cable plant

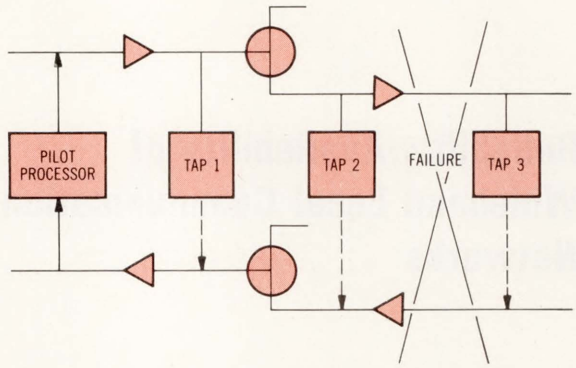

Fig 3 Cable fault isolation. Pilot processor can determine that cable fault has occurred and that it is located between tap 2 and tap 3 locations, since taps 1 and 2 produce normal looped-back pilot amplitudes

In its simplest form, pilot monitoring uses a set of commercially available addressable taps with pilot passing filters. The tap controller and pilot receiver are located at the head end of a 2-cable network, as shown in Fig 2. The controller issues a "close" command to a specific tap and then accepts an amplitude reading from the receiver; this reading is compared with a stored value of expected amplitude. An alert is generated if that value is not within tolerance. The controller then issues an "open" command to that tap, and a new measurement is made to ensure successful opening. The cycle then repeats for each of the other taps in the system.

Different forms of pilot monitoring are possible for other cable configurations. If the pilot monitoring process is applied to a single-cable network, for instance, frequency conversion is required at each tap location. Conversion can be accomplished by frequency translation, a receiver/transmitter combination, or more exotic circuitry.

Automatic processing of data from strategically placed taps can isolate a cable fault to any resolution desired. As an example, Fig 3 illustrates a failure on a 2-cable network between taps 2 and 3 that would be indicated by a successful loop through taps 1 and 2, but an unsuccessful loop through tap 3.

Redundancy is a technique that can be used to minimize the effect of amplifier failures. Inline amplifiers can be effectively paralleled in such a way that the failure of one will reduce the net gain by only 6 dB. Properly implemented, the pilot monitoring subsystem just described can identify which amplifier location has suffered the failure. Replacement of the failed unit can then be effected without disrupting the network. Since the pilot subsystem also identifies

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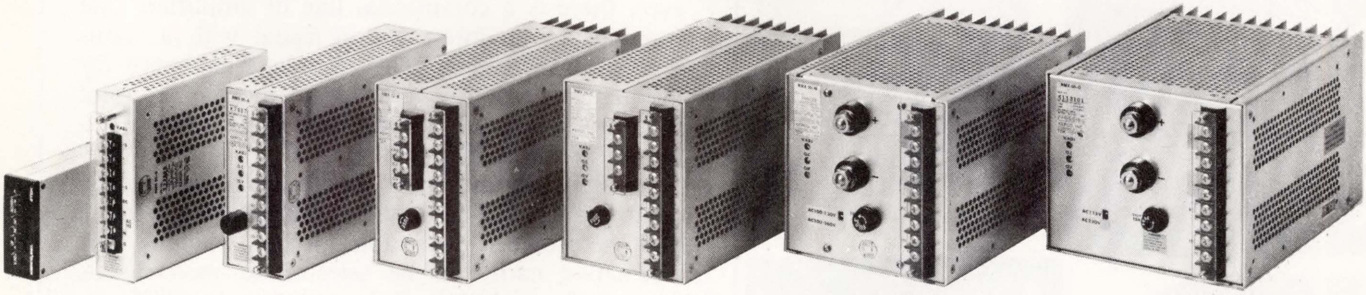

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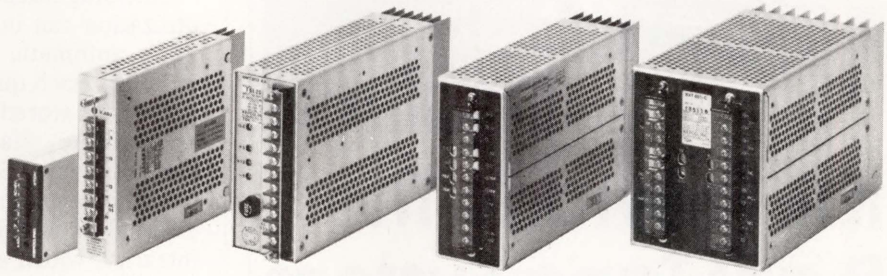

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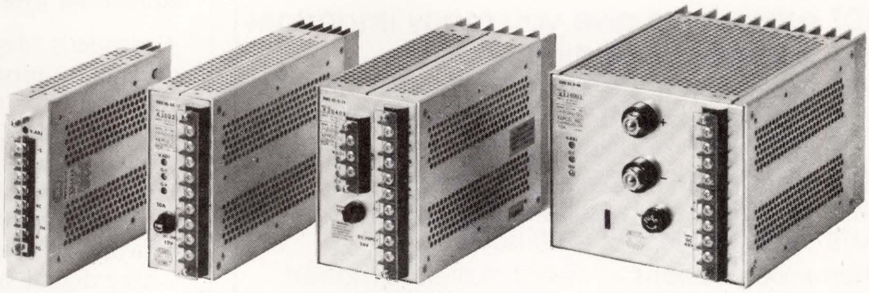

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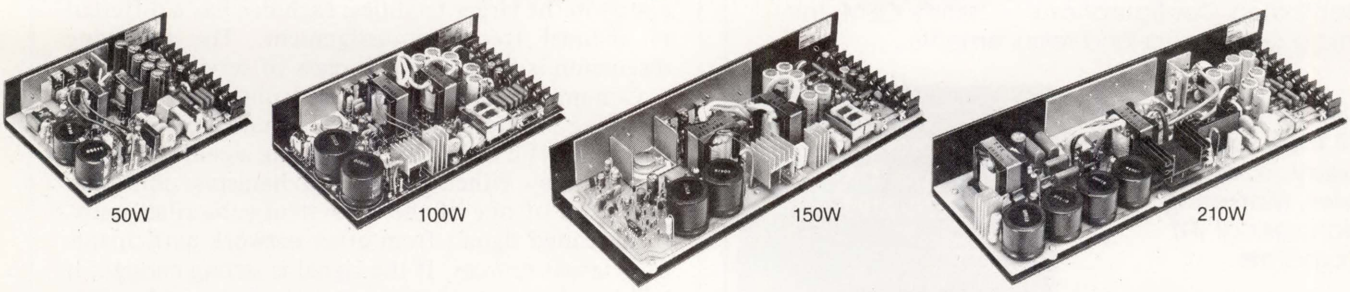

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and isolates other forms of degradation, it is recommended that the pilot monitoring function be implemented in parallel amplifier installations. However, there is a commercial line of amplifiers that responds to an interrogation signal with a status message transmission. This technique has merit for installations that do not plan to include the pilot monitoring function, but do require rapid identification of amplifier degradation.

An alternate routing technique can be used to circumvent a single-component failure. If a parallel path is provided with appropriate switching, the alternative path can be selected to pass signals around the primary path when it becomes inoperative.

Shielding integrity of the cable plant and spectrum utilization can both be determined by a low resolution, automatic frequency stepped rf amplitude monitor. Each quantum of the spectrum can be compared with stored values of expected signal levels and appropriate alarms generated for unexpected measurements. Such measurements indicate either unauthorized use of bandwidth or the ingression of external signals. Ingression suggests a break in cable integrity, which also permits signal egression.

Subscriber Interface Equipment: Failure Analysis

A properly designed and maintained CATV based cable plant provides a highly reliable and benign environment for the distribution of signals in a local area network. The high signal to noise ratio (S/N) permits high quality analog and low error rate digital signal propagation. Consequently, classic noise associated errors are not a problem in cable based networks. Other problems exist, however.

One digital subsystem that may use the cable network forms a common-channel time division bus on which all intersubscriber communications are exchanged. Several of these buses may exist simultaneously in the larger facilities; each bus has a different rf channel frequency assignment. The following discussion is limited to this class of service.

Common-channel buses are subject to channel jamming. Extraneous inband signals can seriously disrupt traffic flow. The interfering signal can be introduced by either of two mechanisms: improper operation of one of the subsystem subscriber units, or unrelated signals from other network participants or external sources. If the signal is strong enough, it will mask transmissions desired at the subscriber receivers. Interfering signals at normal levels will confuse the receivers and may be misinterpreted as legitimate transmissions.

Little if any effect is felt by the other bus participants if a subscriber is unable to insert a transmit signal onto the channel. Such a condition can occur if the transmit cable connection, the rf modulator, or

(continued on page 27)

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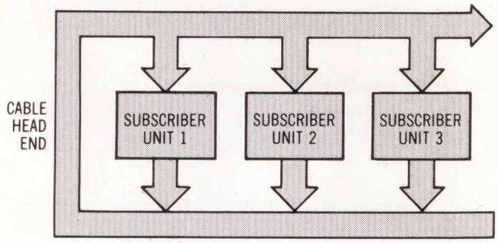

Fig 4 Listen-before/listen-while-talk digital communication bus network. Units intercommunicate by transmitting onto inbound (lower) channel and listening on outbound (upper) channel. These channels are connected (looped) at cable head end. Channel is timeshared among units by unslotted contention protocol in which each unit determines as best it can that channel is unoccupied before starting its transmission (listen-before-talk) and monitors its own transmission for errors and/or contention collisions (listen-while-talk). When collision is detected, each unit involved will invoke retransmission and schedule it after pseudorandom time. In adaptive systems arithmetic mean of this time is chosen as function of collision rate, either by individual unit or by central authority

the control logic fails. However, serious malfunctions can occur if the receive process fails at a subscriber. System timing and the general information necessary for the channel sharing protocol will become unavailable. A subscribing device operating without full receiving capability can issue signals "in the blind," which will cause severe interference to other traffic on the timeshared channel.

In adaptive bus subsystems, signals received in error can produce effects that last longer than the signals themselves. An example of an adaptive subsystem is the listen-before/listen-while-talk bus, in which the mean random backoff parameter is determined as a function of signal collision rate. (See Fig 4.) An error producing interference signal burst can create a large queue of users attempting random delay retransmissions through the collision avoidance process. If it is not carefully implemented, the adaptive backoff parameter protocol can prolong the effects of such a burst.

Bus subscriber units can also develop problems in which distorted operation occurs without full failure. Distorted transmissions can affect all receivers. Such transmissions sometimes result in messages that are not accepted and require retransmission; or they may result in messages that are accepted but are misinterpreted, depending on the strength of the error detection process. Degraded receptions, on the other hand, will also cause missed or misinterpreted messages, but generally at the malfunctioning unit only. These degraded subscriber units have the potential to indirectly cause an unnecessary increase

(continued on page 28)

in channel loading because of retransmission attempts that can, in turn, seriously impair subsystem throughput and end to end delay.

Another condition that can completely block communications is a failure at the cable head end location. Since all inbound signals are looped by one or more devices to the outbound path at the head end, most head end failures impede traffic from all subscriber locations equally. Some head end configurations provide a simple wideband loop, others use band limited filters, while others employ repeaters of various complexities. In most installations, either the wideband loop or several active repeaters are employed. Seldom is a single repeater used, since the wideband nature of the medium is usually exploited to propagate various signals simultaneously. Although a wideband loop failure interrupts all services, it is unlikely to occur; thus, in the long run, the wideband loop is less likely to cause problems. On the other hand, a failure of one in a complex of repeaters will affect only its associated channel or subset of channels, but is more likely to fail unless special design precautions are implemented.

Subscriber Interface Reliability Improvements

Buses that contain an inherent monitoring and control capability, such as polling and dynamically assigned slots, can obtain information about the connectivity and technical welfare of each subscribing unit as part of the network control function. (See Fig 5.) Additional technical information can be obtained by interrogating and measuring individual elements.

In contrast, a central network control that can serve as technical control is not available in a distributed control bus system. (See Fig 6.) Some information on the status of the subscriber units can be obtained by passive traffic monitoring. However, full technical monitoring and control requires additional communications and measurement to ascertain whether minimal functions are being performed. In this class of distributed control bus, it is recommended that a periodic status message be issued by each subscriber unit—either automatically or in response to a poll—independent of but containing information about other types of transmission. This report should provide information pertinent to the unit's operation since the last such report. A special facility must then monitor these messages and perform the technical control function.

Analysis of status messages from individual subscriber units permits the technical monitoring and control facility to judge an appropriate random backoff parameter that is based on the current operation of the complete bus. Continuous modification of the parameter can be broadcast to each subscriber unit as required. This global view is preferred, since an individual unit can modify its parameter based only on a limited view of the bus; consequently, the unit must modify its parameter conservatively.

In both centralized and distributed network control buses, measurements should be made on the quality of the rf signal. It is important to anticipate the degradation in both a subscribing unit's modulator and demodulator. Specialized rf measurement devices provide this data to the technical control facility. Measurement of the transmitted signal from each subscriber unit can be made at any location in the network. Such measurements are nearly useless, of course, unless they can be associated with specific transmitters. One method is to have the measurement device perform this association (ie, digital address decoding). Alternatively, the rf measurement information can be provided to status message interception circuits, where the association will be based on arrival time.

Indirect measurement of each receiver's performance at the subscriber units can also be implemented in the above configuration. The technical control processor can issue cyclic interrogations of each subscriber unit to which a specific response will

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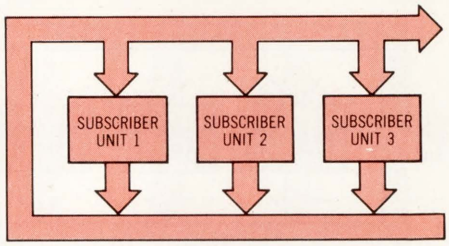

Fig 6 Distributed control network. Subscriber units coordinate exchange of information among themselves without central control authority. Each unit has only parochial view of network health and welfare

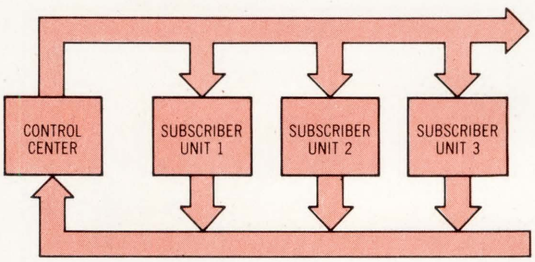

Fig 5 Centralized control network. Here subscriber units exchange information with or through control center. Polling or slotted buses are two such protocols. As byproduct, control center is aware of much of health and welfare of each subscriber unit and hence of that of network

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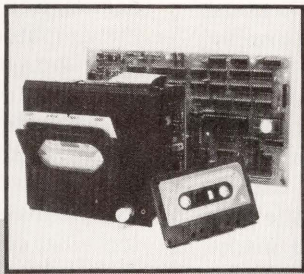

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be issued. If a known rf signal from technical control is progressively perturbated, an operation range can be determined over which the subject receiver performs properly.

To prevent a subscriber unit from transmitting inadvertently because its receiving circuitry is not functioning, the design could include a transmit inhibit function. One method would be to make each unit ascertain that it can hear its status message clearly; otherwise, all other types of transmission will be prohibited. To prevent abnormally long transmissions when the subscriber control logic fails in that mode, each modulator can include a "dead-man" switch to provide an inhibiting function.

Technical Control Considerations

The dichotomy of too little or too much information applies to technical control systems as well as to other forms of monitoring. When the system is performing properly, simple indication of that fact is required. An alert condition calls for a straightforward indicator. However, how the specific cause for alert is presented is critical to successful maintenance. A system that presents only the fact of alert can be designed, but a better system would present the process or logic by which the alert decision was made. The best system design would process all alerts for correlation and present a probable cause.

As an example of these three levels, assume that a cable pilot monitoring function identifies a major cable severance. The simplest system would indicate only that there was a problem on the cable plant. A more complicated design would list all addressable tap locations that report the amplitude of the looped pilot to be low. The best design would determine that, since all out-of-tolerance levels were at the noise level and the locations were all in one building, probable cause for the failure was a break in the cable plant at the building interface.

In a similar manner, the well-designed technical control process would analyze the fact that the amplitude of all status messages on the digital bus had been reduced by 4 dB, and indicate the probable cause as a degradation either of a head end cable amplifier or of the amplitude measurement device itself. Analysis algorithms must be formulated to provide detailed backup information for maintenance personnel.

The technical control facility should not be designed as an integral part of normal systems operations. That is, the complete system of cable plant and using subsystems must continue to function even if technical control is not active. As an example, in a digital bus design that incorporates a centralized adaptive retransmission backoff parameter, each subscriber interface unit must incorporate a fail-safe fallback parameter to be invoked if no such value is received from the central technical control facility. Such design permits the introduction of technical control during any phase of the system's lifetime, and permits modifications to tailor the functions to specific needs.

A single computer based technical control facility is more economical to implement than separate computers for each subsystem. A single-processor configuration is possible if the technical control functions are not built into the subsystem or designed to be time critical. Design should allocate the processing power among the subsystems as necessary. The single-processor configuration can also coordinate and exchange information among individual technical control processes for different subsystems, readily permitting probable cause analysis. For example, probable cause analysis can associate loss of pilot looping with absence of subscriber unit status messages to report the status of a specific section of the network.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 719 **Average 720** **Low 721**

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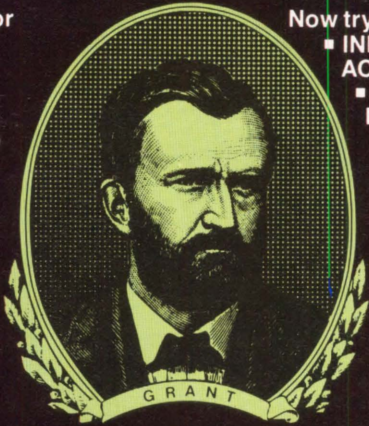

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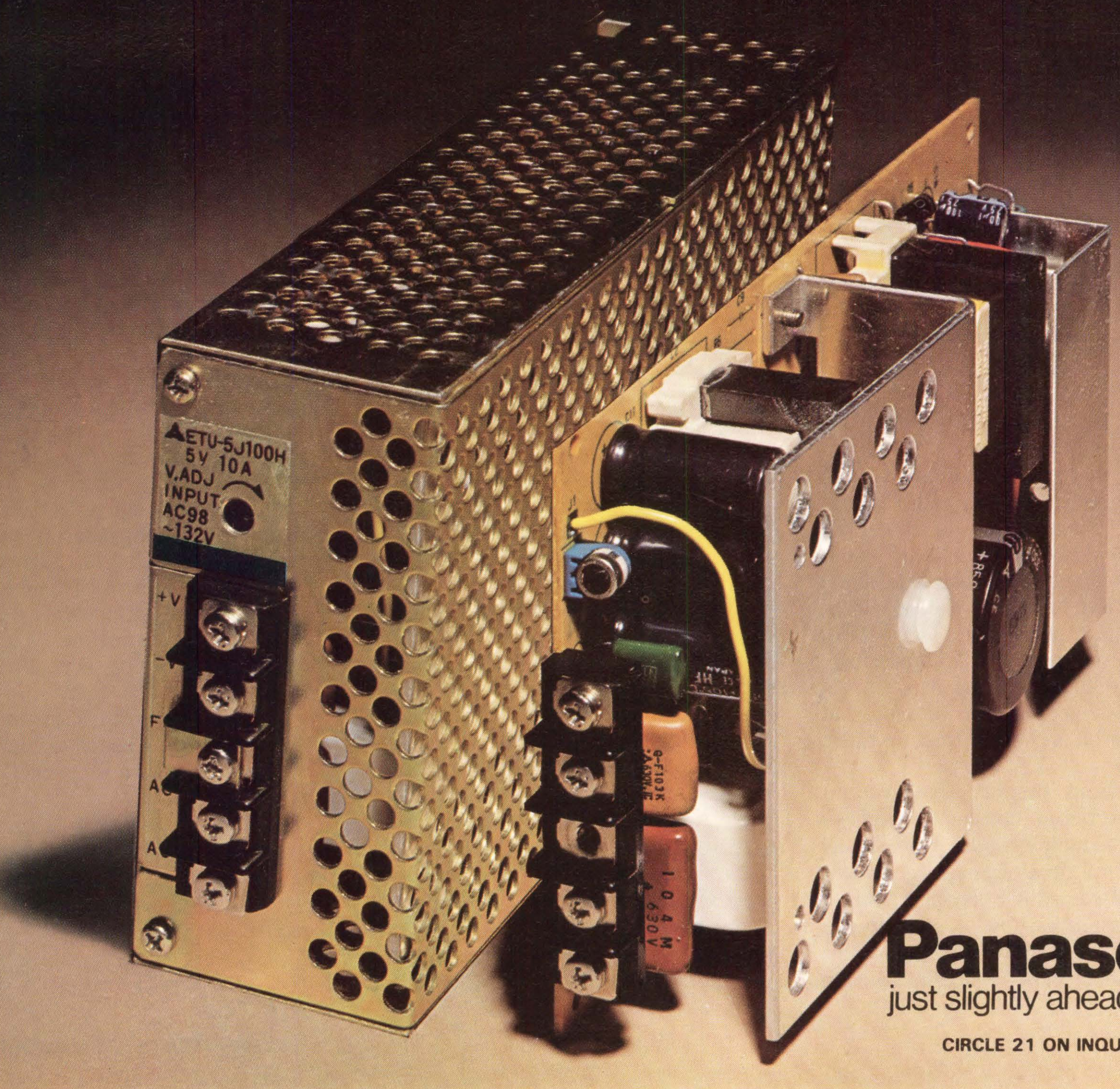

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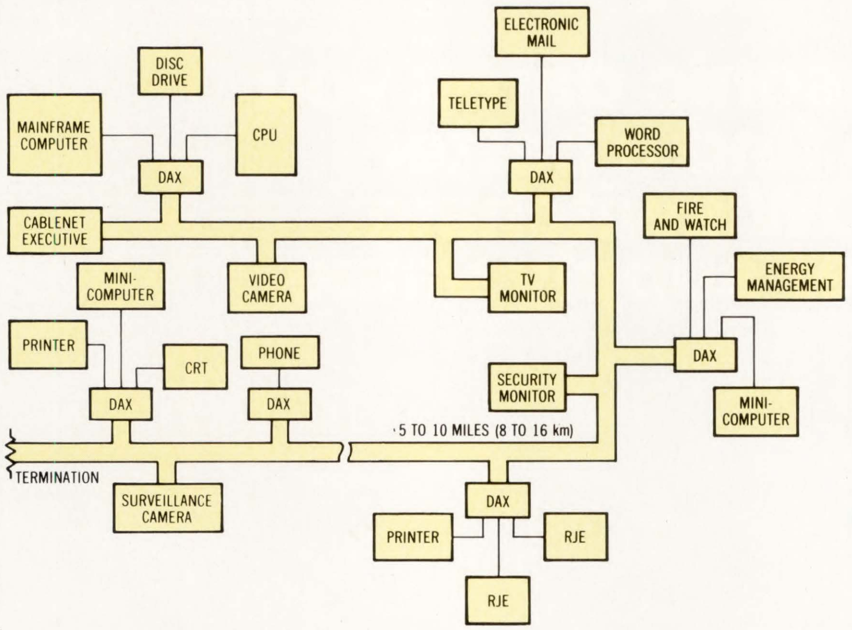
CIRCLE 21 ON INQUIRY CARD

Broadband coaxial local area network supports multimode communications over 50-mile range



Idealized CableNet configuration. Universal general purpose communications medium broadband coaxial cable supports such applications as computers, word processors, data terminals, TV monitors, and energy management systems. Broadband cable offers capacity 50 times that of conventional baseband systems

Using a single broadband coaxial cable as the transmission medium, CableNet™ supports over 16,000 devices operating at data rates to 64k bits/s while using only 8% of the cable's total bandwidth. The remaining bandwidth is available for such additional concurrent applications as voice, video, or other data transmission. The system, recently introduced by Amdax Corp, 160 Wilbur Pl, Bohemia, NY 11716, comes in two versions for operation at 7M- or 14M-bit/s channel transfer rates, respectively.

Both versions support asynchronous and bisynchronous communications at full- or half-duplex modes between all computers and data terminal equipment using standard serial interfaces. SDLC/HDLC is also supported to provide IBM compatibility. Access to the cable medium is determined via time division multiple access (TDMA) reservation. Devices on the system may be 50 mi (80 km) apart. The system automatically provides speed and protocol conversion to accommodate communications between dissimilar computers and peripheral devices.

The network is composed of four basic hardware components: CableNet Executive, Data Exchange (DAX) interface units, broadband coaxial cable, and standard CATV taps and connectors.

Placed at the head end of the system, the Executive controls communications between the devices connected to the cable, and all communications on the system pass through it. Data are sent in packet format from connected devices to the Executive in the "reverse" direction at low frequency (5.75 to 106 MHz), and the Executive retransmits the packet in the high frequency (160 to 300 MHz) "forward" direction for distribution throughout the entire network. The Executive automatically adjusts the level of every network device's transmitter as well as the levels of any newly added devices.

The system uses the properties of propagation speed and distance from the Executive to place all devices equidistant from the controller if viewed in the time domain. A process called "ranging" automatically performs all calculations required for the logical topology during initialization or when a device is added to the network. This enables an almost unlimited number of network topologies. In the initialization procedure, the Executive also establishes transmission delay times for every active device in the network. The controller can be supplied in a redundant configuration with another Executive and a switchover unit as a hot standby.

DAX interface unit is placed between user terminal equipment and the cable network. Each DAX has four digital interface ports; three connect to user devices at data rates up to 19.2k bits/s, and the fourth is configured for diagnostic functions. An rf interface connects to the system trunk via a coaxial drop cable. Because of the variety of available data terminal equipment and the number of associated variable parameters, each DAX port is configured for the specific user devices it will service. The parameters, called default parameters, are stored in nonvolatile memory within the interface unit and can be changed by entering a command sequence through the diagnostic port. No operator control of DAX units is required since all parameters are set during network configuration. Logical addresses and a physical address are assigned to each DAX by software. The DAX receives all transmissions from the Executive and decodes all packets, but responds only to those packets that bear its addresses.

The system uses standard CATV connectors, taps, amplifiers, and broadband coaxial cable that have been used by the cable television industry for many years.

Circle 321 on Inquiry Card

Build your own DEC system with CRDS...

MF-211

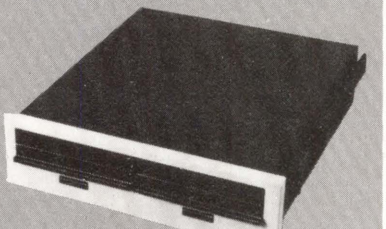
10½" Enclosure for LSI 11/23 System with built-in RX02 equivalent floppy disk system. Available with or without processor and memory.

HD-11/T

20.8 Megabyte Winchester disk software equivalent to 4 RL01 units. Optional cartridge tape backup.

FD-311

RX02 equivalent dual floppy system, single or double sided. Includes bootstrap loader, self-tester, formatter and diagnostic diskette.



MB-211

5¼" enclosure with 8 quad slot backplane. Front panel console with switches for Enable/Halt, Boot/Init and Line Time Clock.

Complete software compatibility at a savings!

With CRDS, you can configure your own DEC system and be assured of complete software compatibility. Each of the above systems is provided with slides for rack mounting or can be used in desk top applications. All DEC LSI 11 based modules and associated software packages are available through CRDS, if desired.

Attractive Packaging
Careful attention is given the CRDS repertoire of enclosures in assuring you an attractive yet comfortable blending of product in the DEC environment.

Significant Savings
Flexibility of procurement plus attractive OEM schedules allows you to optimize dollar savings in configuring your CRDS system. Use the time tested technique. Compare.

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A 90 day warranty is offered with your CRDS system. In the event of malfunction, by use of provided diagnostic routines, the defective submodule is normally found within minutes. After verification with the CRDS Maintenance Department, a replacement for your defective module will be promptly forwarded.

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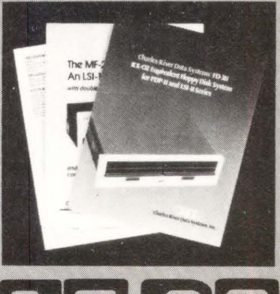

CRDS

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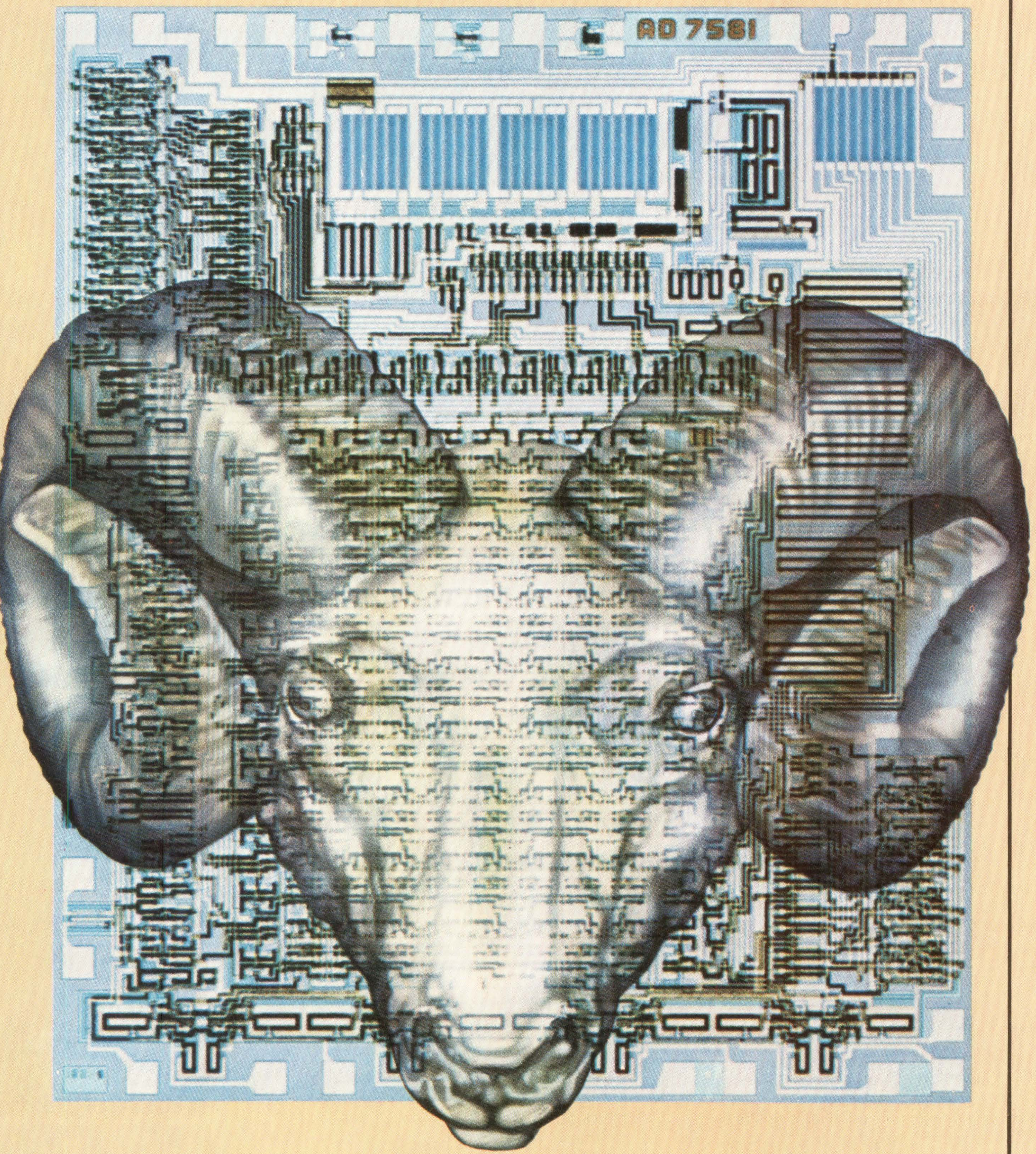
HERE'S THE FIRST ADC



TMS4164

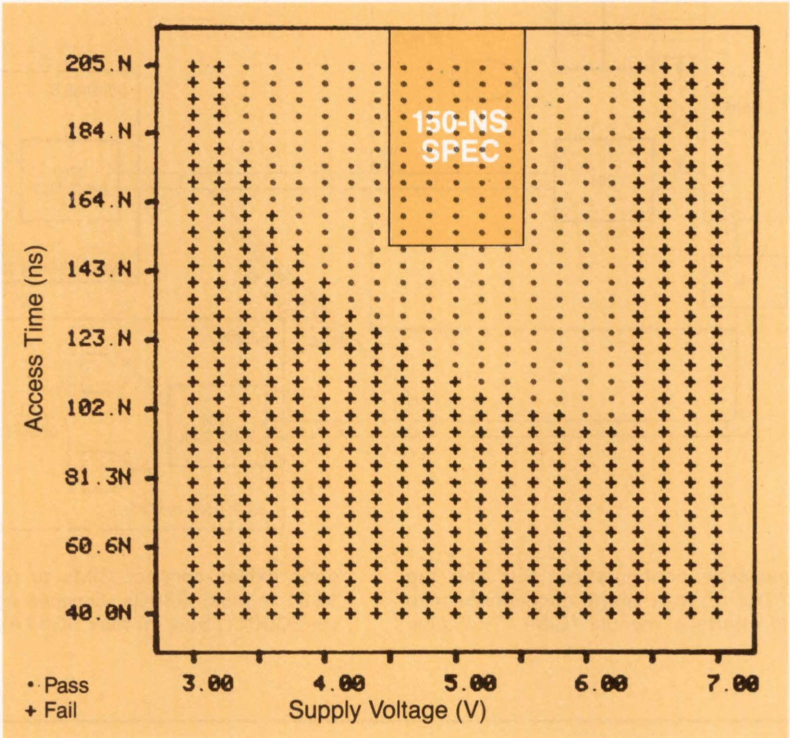
The performance leader. From Texas Instruments.

When we began designing the 64K RAM, we decided to make it better than the 16K. Not just four times bigger.

What's better? In a word, performance. Add up high speed, reliability, low power and improved system operating margins, and you'll see why our superior performance puts the TMS4164 in a class all by itself.

Faster access times

The wide range of TMS4164 functionality and speed potential is demonstrated in the graph to the right. This illustrates the wide operating margins designed into the high-performance 150-ns TMS4164. And, even faster devices are on the way.



Power dissipation

At 125-mW typical, the TMS4164 is unequalled in the industry for low power dissipation. Power design features like interlocked clocks mean you use only as much power as you need. Only when you need it. Our optimum architecture, requiring only 256 sense amplifiers, assures you of minimum power dissipation and enhanced reliability.

Ease of use

Two separate 8-bit internal buffers simplify use — one is for row address, one is for column address. TTL-compatible, one-clock operation greatly expands input timing flexibility and assures fast throughput.

TMS4164 64K Dynamic RAM

	4164-15	4164-20	4164-25
Access Time Row Address (Max)	150 ns	200 ns	250 ns
Cycle Time Read or Write (Min)	280 ns	350 ns	410 ns
Cycle Time Read/Write (Min)	280 ns	350 ns	410 ns
Power Dissipation Operating (Typ)	140 mW	125 mW	105 mW

Lowest power surge

Our 256 cycle refresh architecture has significantly reduced the current surge problem of designing with other dynamic RAMs. The resultant lower current spikes (≅60mA), less than on *one* 16K dynamic RAM, facilitate system power distribution, increase noise immunity and improve board layout.

And there's more

The TMS4164 is the smallest 64K chip (35K mil²) in production. Perfectly suited for use in main-frame computers and large minicomputers, the TMS4164 also finds ideal application in microprocessor-based systems which demand small size, low cost, and improved performance.

Available now

The high-performance TMS4164 is now stocked for immediate delivery. Order today from your nearest authorized TI distributor. Or, for more information, write Texas Instruments Incorporated, P.O. Box 202129, Dallas, Texas 75220.

Texas Instruments invented the integrated circuit, microprocessor and microcomputer. Being first is our tradition.

TEXAS INSTRUMENTS
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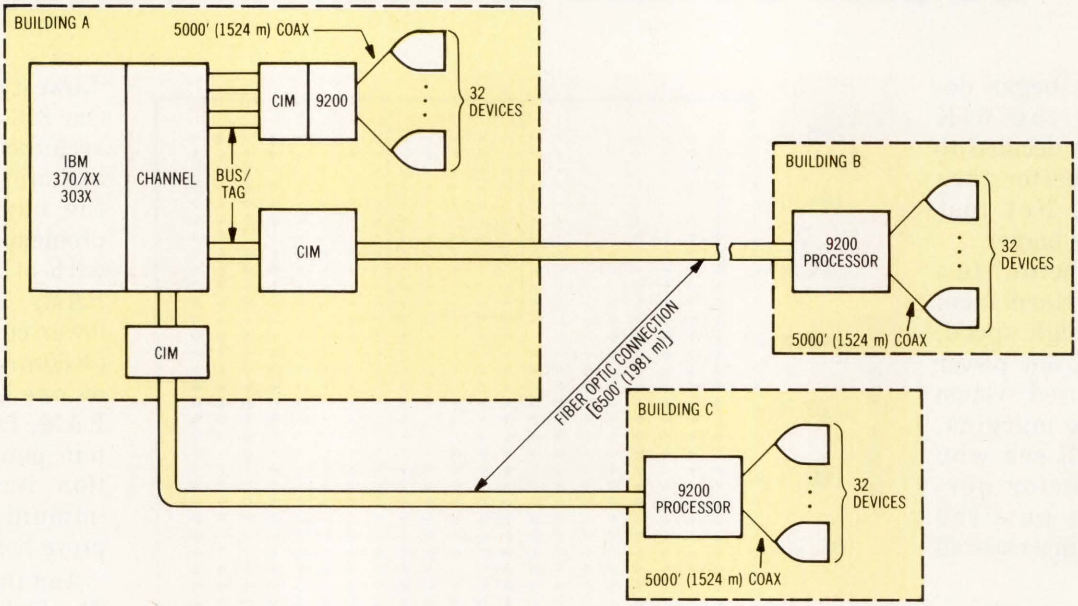
CIRCLE 24 ON INQUIRY CARD

85011A

Fiber optic link extends host channel attachment, reduces response time



Typical campus-style configuration. Bus and tag cable of 200′ (61 m) max length connects host to 9200 channel interface module (CIM). Two fiber optic cables connect CIMs to remote (6500′ or 1981 m max) 9200s. Devices connect to 9200s via 5000′ (1524 m) max RG62AU coaxial cable

A fiber optic link option allows displays and printers that normally communicate with a host over transmission facilities to have direct channel access. This significantly reduces response time for inquiries and may decrease costs by eliminating the need for communications facilities, according to Harris Corp, Data Communications Div, 16001 Dallas Pkwy, PO Box 400010, Dallas, TX 75240.

The link option for the company's 9200 information processing systems extends maximum direct channel attachment between an IBM host and 3270-type displays and printers from 5000 ft (1524 m), the standard for this type local attachment, to 11,500 ft (3505 m). Data rates over the fiber optic link are up to 2M bits/s.

The 9200 processor is functionally compatible with the IBM 3274 controller and 3278 displays in remote and local configurations. In standard local arrangement, the processor is attached to an IBM host channel operating in 3272 or SNA modes. Up to 32 displays and printers may be located as much as 5000 ft (1524 m) from the 9200 via coaxial cables.

With the fiber optic channel option, the processor adds a channel interface module (CIM). The processor and CIM each contain LED light source and PIN photodiode detect elements that launch and decode the light impulses. CIM and processor are linked by fiber optic cable and data are transmitted at up to 2M-bit/s rates.

Maximum length of the link between CIM and 9200 processor is 6500 ft (1981 m). In addition, devices connected to the processor may be placed 5000 ft (1524 m) from the processor. Combining the fiber optic and coaxial links allows location of devices up to 11,500 ft (3505 m) from the host and continued operation at channel speeds.

Circle 322 on Inquiry Card

Communications interface board improves distributed network performance

Bit Character Asynchronous Interface Module (BCAIM) microprocessor based communications interface board from Texas Instruments Inc, Digital System Group, PO Box 202146, Dallas, TX 75220, enhances the distributed network performance of the company's DS990 computer systems. It provides an economical communication interface and handles many protocols, speeds, and configurations.

An onboard TMS9900 microprocessor and semiconductor memory combine to reduce CPU overhead. Memory includes 8k bytes of ROM and 2k bytes of RAM. The module buffers multiple data bytes in onboard memory before interrupting the system CPU, and the microprocessor

(continued on page 43)

Wouldn't it be great if every kind of keyboard had our kind of performance?

SC Series Capacitance Membrane Keyboard

KD Series Touch Panel Keyboard

SD Series Hall Effect Keyboard

CT Series Contact Membrane Keyboard

Now they do.

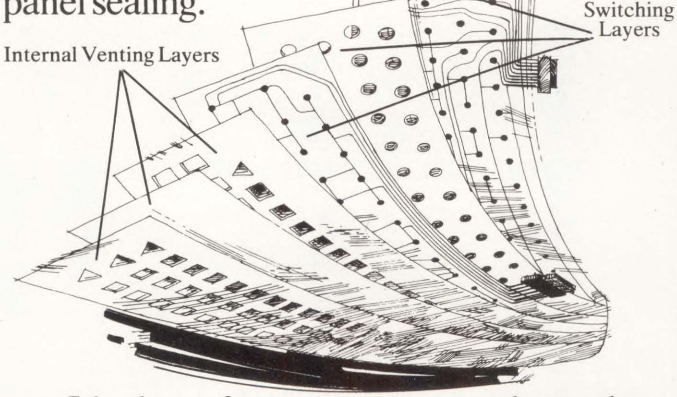
Until now, getting a keyboard at the price you needed could have meant giving up the kind of performance you wanted.

But not anymore.

Because, with the introduction of three new membrane keyboards, MICRO SWITCH has become the world's only full-line supplier of reliable keyboards. We offer a high-performance and cost-effective solution for virtually any application.

Now, in addition to our time-proven Hall effect offerings, you can specify MICRO SWITCH SC Series full-travel capacitance membrane or CT Series contact membrane keyboards, and KD Series touch panel membrane keyboards.

Whatever type of seal you need, all you have to do is ask. The capacitance membrane units are the world's only capacitance keyboards with all the benefits of membrane sealing. And we're the first to solve the venting problems associated with previous membrane designs. Both our capacitance membranes and contact membranes are internally vented to maintain their seal while preventing switch collapse due to air pressure or temperature changes. And for especially severe environments, the touch panel keyboards give the added feature of panel sealing.



It's those features, among others, that make these new keyboards more reliable than other capacitance and hard-contact designs.

And because all three new keyboards have been designed with traditional MICRO SWITCH quality and reliability, each carries a 1% Acceptable Quality Level and 2-year warranty.

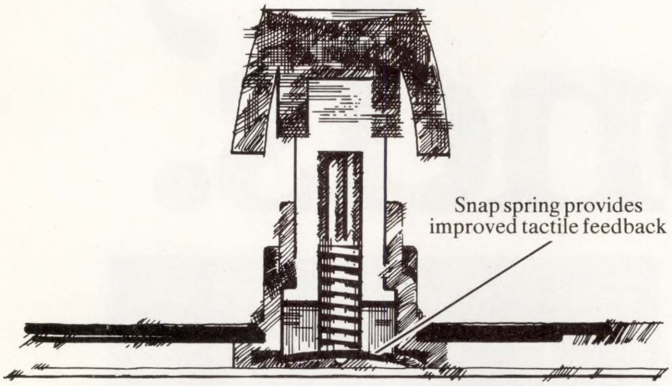
Now any combination of keyboard features you can name can have the MICRO SWITCH name on it.

Now your keyboard specifications are only limited by what you want. Not by what you can get.

Our full-travel series, for example, are available in a wide variety of keyboard configurations, with a choice of over 40,000 legends.

Because legends are screened on our touch panel designs, the graphic possibilities are endless. And, we can combine full-travel and touch panel actuation in a single assembly, featuring either capacitive or hard contact technology.

We make it easier to comply with European standards, because our full-travel membrane designs are available in low-profile versions to meet world requirements.



And, the actuator module for the full-travel membrane keyboards helps achieve new levels of tactile feedback and operator satisfaction.

So you can come to MICRO SWITCH for the keyboard technology, travel, actuation, sealing, appearance, profile, electronics, and special features you need.

And get them all – backed with the experience and full application support that's been a MICRO SWITCH tradition.

Being able to design a keyboard to fit any application is important. But doing it to fit any operator is imperative.

It's important to understand that half of any keyboard application is a human being. There's probably no keyboard manufacturer who understands that better than MICRO SWITCH.

Our unique human factors research – an intensive, on-going program for over 20 years – has given us the tools to develop industry standards for key speeds and multi-key rollover; tactile, visual, and audible feedback; and various keytop shapes, spacing, configurations and travel. We're continually improving the man/machine interface.

This human factors research is part of

what makes our keyboards unique. And it's part of every keyboard we make.

Instead of resting on our laurels, we're relying on our research.

Being able to add state-of-the-art capacitance membrane, contact membrane, and touch panel keyboard types to our Hall effect offerings is the result of extensive planning, research and testing.

But it's only the beginning.

Each of these keyboard types will be continually subjected to the refinements growing from our human factors research, customer feedback, and our unmatched R&D facilities which include backup by our Honeywell corporate facilities.

Also, every keyboard customer benefits from a manufacturing capability that stands unmatched: it's large enough to handle the most extensive order; responsive enough to give the modest order the same kind of intensive, individualized and quality-conscious attention.

All of these efforts are to make sure that, as your keyboard needs change and grow, you'll always have the choice of a progressive alternative with one unchanging feature: the MICRO SWITCH name. With all the performance that name implies.

For more information on our keyboard technologies, call 815-235-6600. Or write, MICRO SWITCH, the Keyboard Consultants, Freeport, IL 61032.

MICRO SWITCH
a Honeywell Division

CIRCLE 25 ON INQUIRY CARD

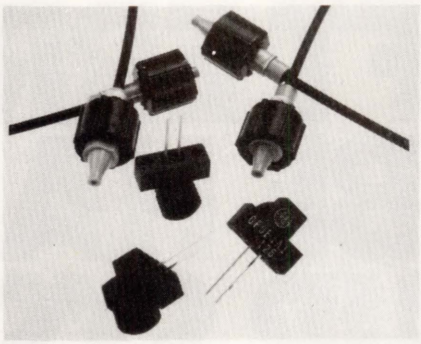
performs the character processing associated with a number of protocols. The board supports bit-oriented SDLC and HDLC, and also character-oriented Bisync and TTY.

Speeds to 9600 bits/s are accommodated at full-duplex over RS-232-C or local line connection with full modem control and conformity with FCC emission standards. System software for the interface board includes 3780/2780 protocols under distributed network operating system DNOS, batch communications under DX10 3780/2780, and interactive communications under DX10 3270.

The new module is an intermediate step between the company's communication interface module and its Four-Channel Communications Controller (FCCC). While the former provides a less costly means of connecting remote terminals, the BCAIM adds speed and support for bit-oriented protocols and is best suited to system configurations supporting one or two independent communication channels. FCCC, on the other hand, is a frontend processor for controlling up to four independent channels. The FCCC has the additional capability of accepting downloaded user-coded software that further reduces the host computer workload. The new board requires a half slot in the DS990 chassis and interfaces to the communications register unit bus.

Circle 323 on Inquiry Card

Low cost emitters and detectors are available for fiber optic applications



Fiber optic emitters and detectors. Semiconductor components are designed to mate with AMP plastic ferrule connectors that can be coupled to over 40 different types of optical fibers

Cost-effective light sources and detectors for fiber optic industrial control and data communication systems have been introduced by General Electric Co, Semiconductor Products Div, MD44, W Genesee St, Auburn, NY 13021. The medium-performance devices are OEM priced in the \$1.50 to \$2.00 range. The initial product offering, which will be extended to a full line, is composed of a 100-μW min, 940-nm emitter in two output ratings, and two photodetectors, each with two response levels.

Infrared emitting diodes (IREDs) GFOE1A1 and GFOE1A2 are GaAs diodes that emit noncoherent IR energy at a peak wavelength of 940 nm. Power output for the GFOE1A1 is 100 μW min and for the GFOE1A2 60 μW min measured at the end of 1-m long Galite™ 1000 cable. Measured using Crofon® 1040 cable GFOE1A1 produces 45 μW and GFOE1A2 25 μW min, respectively.

Detectors GFOD1A1 and GFOD1A2 are silicon photodetectors that detect and convert light signals from optical fibers into electrical signals. GFOD1A1 has a responsivity of 70 μA/μW, and GFOD1A2 of 30 μA/μW when coupled via 1-m length Crofon 1040 cable to the GFOE1A1 emitter.

Detectors GFOD1B1 and GFOD1B2 are silicon photo-Darlington devices. Under the same conditions noted above GFOD1B1 exhibits 1000 μA/μW, and GFOD1B2 500 μA/μW responsivity, respectively.

The components are mounted and terminated with self-tapping screws, screw and nut combinations, or rivets. They are PCB mounting compatible with both metric and English systems.

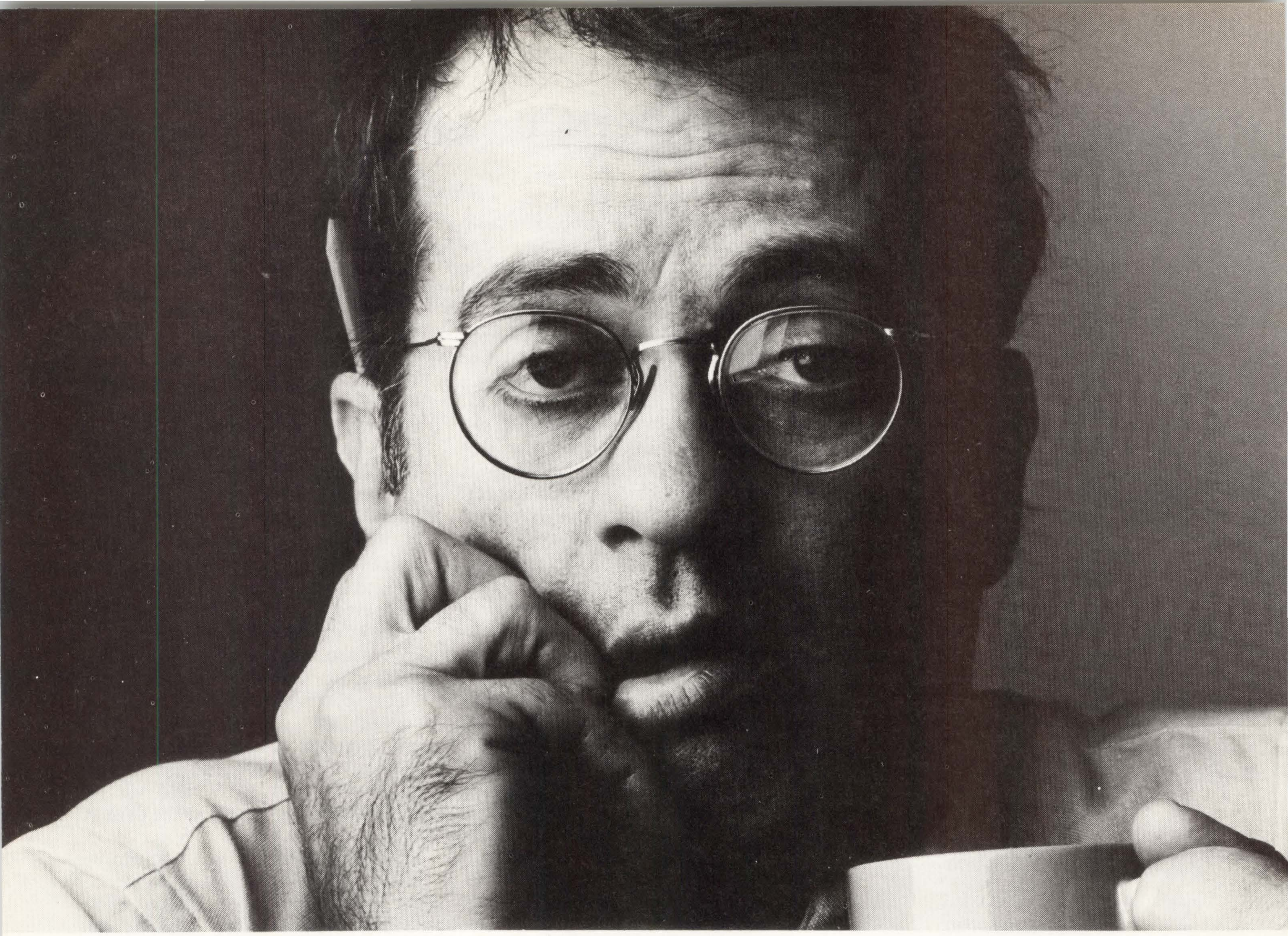
Circle 324 on Inquiry Card

Communications frontend processor for System/34 supports X.25 protocol

GATEWAY/34 communications frontend system for use with IBM System/34 allows users to connect to System/34 with any combination of local terminals, dial-up or leased lines, and public packet networks. The system supports X.25 communications protocol for access to GTE-Telenet and Tymnet in the U.S. The processor was developed by Systar Corp, 1762 Technology Dr, Suite 208, San Jose, CA 95110, for small to medium sized businesses, typically with 8 to 16 terminal sites nationwide.

The system uses the IBM Series/1 minicomputer and supports access to

(continued on page 46)



SOFT ERRORS CAN BE HARD ON YOUR SYSTEM.

System/34 using IBM 3101 display terminals and printers. The minicomputer connects to System/34 via a single 9600-bit/s link using SDLC protocol, and appears as a set of multidropped workstation clusters. Sixteen terminal/printer workstations can be connected to a single System/34 communications port. Software performs protocol conversion between the SNA and X.25 network protocols, and between the 5251 and 3101 display formatting commands.

As many as four System/34s may be connected to a single GATEWAY/34 front end. The destination System/34 can be selected by user command when a remote terminal connects to the front end. The computers may be connected to the processor via direct local cable, or by dial-up or leased lines.

The company's X.25 communications software has been certified for operation on both GTE-Telenet or Tymnet at speeds to 9600 bits/s. The processor can be simultaneously connected to multiple public packet networks.

Circle 325 on Inquiry Card

300-baud modem features integral autodial and autoanswer

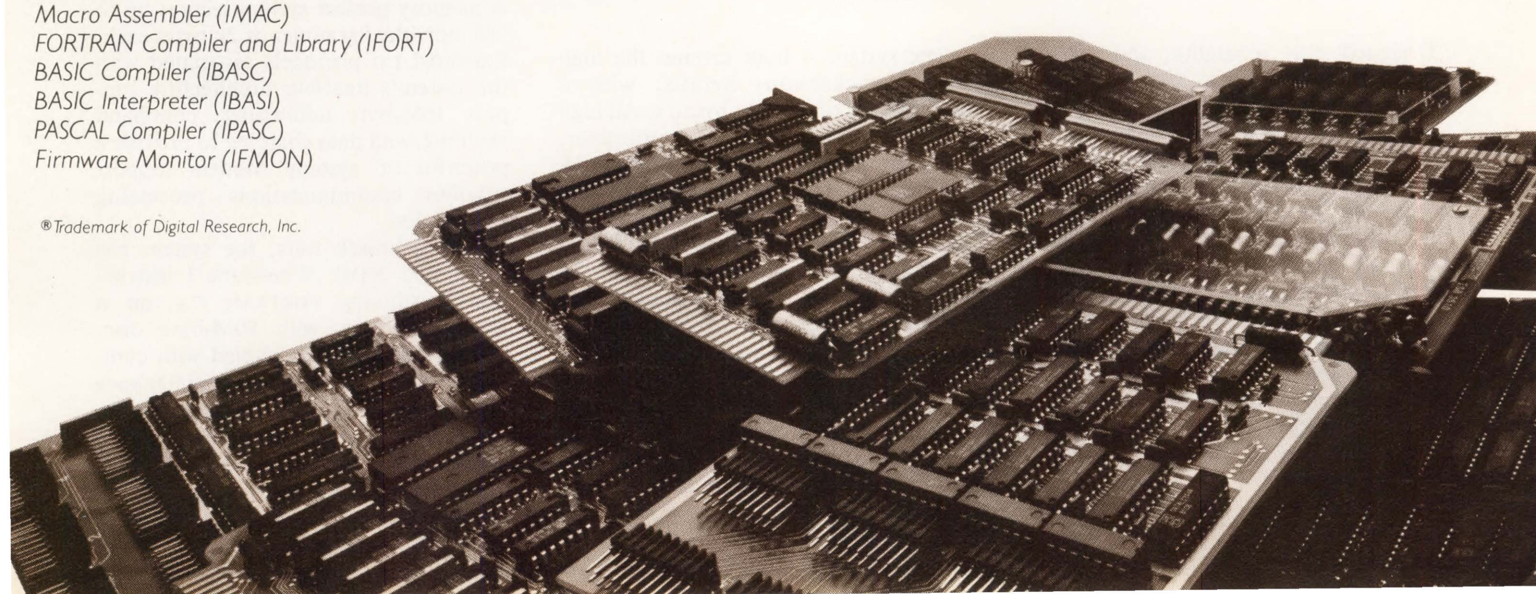
Smartmodem is an FCC-approved direct connect device that enables RS-232-C compatible computers or terminals to communicate with other computers or timesharing systems via the public switched telephone network. The modem, a product of Hayes Microcomputer Products Inc, 5835 Peachtree Corners E, Norcross, GA 30092, can be program controlled in any language by ASCII character strings. Intelligence is provided by a Z8 microprocessor with a 2k-byte control program.

All circuits required for autodial and autoanswer functions are built into the unit, eliminating the need for auxiliary equipment. Dialing can be either Touch-Tone^R or pulse; both modes can be combined within a command. A pulse can be used to access a PBX with Touch-Tone picking up access to the outside number when the second dial tone is received. An audio monitor follows the progress of a call and alerts to wrong numbers and busy signals. A repeat command automatically redials the number at any time when a busy signal is encountered.

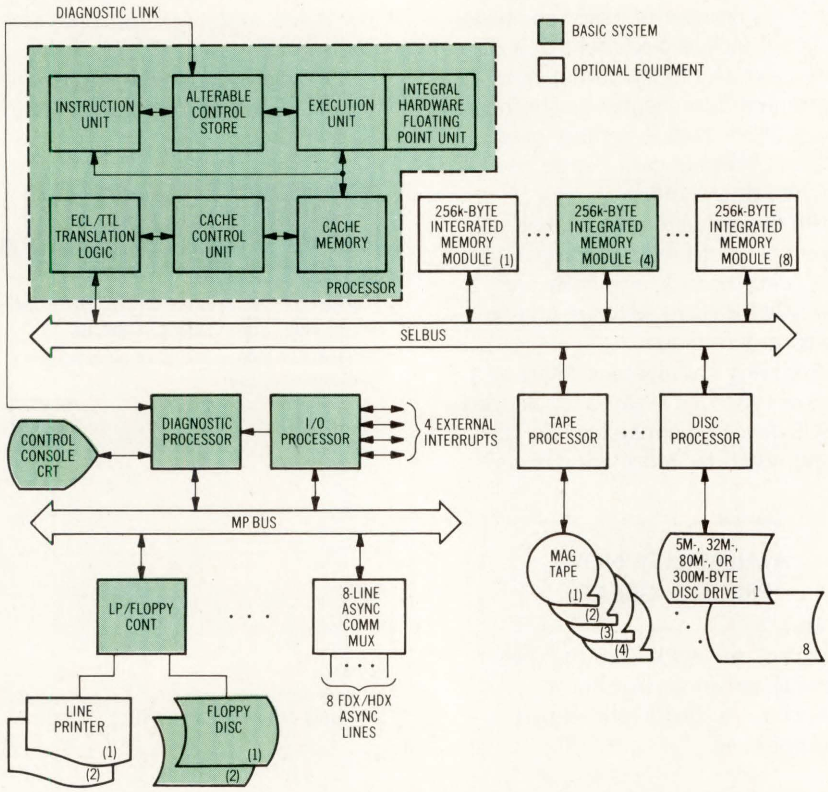
Operation is full- or half-duplex at 0- to 300-baud data rates. The unit is Bell 103 compatible. Data format is serial, binary, asynchronous, 7 or 8 data bits, 1 or 2 stop bits, and odd, even, or no parity. Unique "Set" commands allow selection and change of such operational parameters as dialing speed, escape code character, and number of rings to respond to. Receive sensitivity is −50 dBm and transmit level −10 dBm.

Seven option switches control power-on default options, four of which can be overridden by software command. Operational status of the unit is indicated by front panel LEDs. The modem measures 1.5 x 5.5 x 9.6" (3.8 x 14 x 24.4 cm). It connects to the telephone network via modulator jacks RJ11W, RJ11C, RJ12W, RJ12C, RJ13W, or RJ13C.

Circle 326 on Inquiry Card



32-bit minicomputer gains power from separate instruction/execution units



Designed with pipelined instruction execution, alterable control store, cache memory, and separate I/O and diagnostic processors, CONCEPT 32/87 provides transfer rate of 26M bytes/s over synchronous bus connecting high speed I/O devices, I/O processor, and main memory

Designed for reliability and performance, the CONCEPT 32/87 challenges other processors in its category by performing more than 3.6M instructions/s (MIPS). Architecturally, the system, designed by Systems Engineering Laboratories, Inc, a subsidiary of Gould Inc, 6901 W Sunrise Blvd, Fort Lauderdale, FL 33313, offers separate instruction and execution units and associative cache memory. Mainframe performance is made possible by incorporating an ECL 10k CPU with a 75-ns cycle time, 4-way set associative cache memory, hierarchical memory system, alterable control store, and 4-way instruction pipeline.

The system is built around the high speed synchronous SelBUS, with a transfer rate of 26.67M bytes/s. All high performance I/O devices, I/O processor, and main memory reside on this bus. A medium-speed asynchronous I/O bus, the multipurpose (MP) bus transfers data at a rate of up to 1.5M bytes/s under control of the I/O processor (IOP). Up to 16 device controllers with a total of up to 124 I/O devices can exist on the bus at any time.

Implemented in 10,000 series ECL that supplies fast gate switching times, the CPU outperforms units built using traditional technologies. Functional units within the CPU are connected by internal buses that boast 75-ns bus cycle times. During each 75-ns cycle, four macroinstructions are in various phases of execution, increasing the effective throughput of the CPU and the system.

Of particular significance in the unit's instruction set are eight bit-manipulation instructions that provide capability to selectively set, zero, add, or test any bit in memory or a register. They also provide interprocessor semaphore capability in multiprocessor configurations. The floating point processor, an integral part of the CPU, is a high speed, ECL based computational processor with 64-bit wide buses to achieve high speed, single- and double-precision floating point operations.

A hierarchical memory system increases system performance. Each level is successively faster than the one below, with the CPU exchanging data with the 16k- or 32k-byte cache. The 90% hit ratio of the cache combined with main memory, which is capable of providing double-word fetches to the CPU and cache in 1050 ns, deliver words from main memory to the CPU in 94.5 to 153 ns.

Main memory, consisting of a single board with 256k-byte MOS RAM, memory controller, error correction logic, and refresh circuitry, interfaces directly with the SelBUS. By overlapping two read cycles, it permits read to be initiated every 300 ns. The computer supports up to 16M bytes of physical memory.

The IOP operates independently of and in parallel to the CPU to increase CPU availability and system performance. A single IOP handles 16 device controllers supporting a total of 124 devices on a single MP bus.

The system runs under the MPX-32 operating system, a mapped executive that addresses memory in mapped non-extended, or mapped extended modes. A memory protect system secures up to 256 individual granules of 2k bytes each. Extended I/O protocols associated with the system's dual-bus architecture support 16M-byte addressing, command chaining, and data chaining to provide a powerful I/O system. Modem support supplies communications processing capabilities.

In benchmark tests, the system has performed 3604k Whetstone I instructions/s running FORTRAN 77+ on a 1M-byte system with 80M-byte disc. This performance is coupled with comprehensive diagnostic and maintenance support to meet demands of scientific, engineering, and mainframe offload applications.

Circle 351 on Inquiry Card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8-inch Winchester Multi-User Systems. Now In Volume-$8,500.

Altos is delivering the cream of the crop with their new 8-inch multi-user Winchester disk systems. They're freshly packed with the quality features you expect from Altos, and at a price you expect from Altos, too—just $8,500.

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Here's the most bountiful selection of systems and capacities in the field from the company that knows how to deliver quality systems in the volumes that OEMs need to stay competitive.

And Altos supports these systems with a broad software selection including the three industry standard operating systems—CP/M, multi-user MP/M** and OASIS†. These operating systems support seven high level programming languages: BASIC, FORTRAN, COBOL, PASCAL, APL, PL/1 and C. Also available are comprehensive communications packages: ASYNC—Altos-to-Altos, BISYNC—Altos-to-mainframe and full networking with CP/NET. All are designed to run on a high speed 800 Kilobaud networking channel—standard with every system.

The ACS8000-10 Winchester systems join our growing family of field-proven products. In just three years, more than 8,000 systems have been shipped to an OEM customer-base.

Get to market fast. Harvest your 8-inch Winchester system direct from the heart of Silicon Valley. Call or write today for specific product information and OEM pricing. Altos Computer Systems. 2360 Bering Drive, San Jose, CA 95131, (408) 946-6700, Telex 171562 ALTOS SNJ.

SYSTEMS PICTURED:

ACS8000-10 (10Mb HD + 1 floppy)	$ 8,500
ACS8000-10/MTU (10Mb HD + DEI Mag Tape)	$10,990

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ALTOS
COMPUTER SYSTEMS

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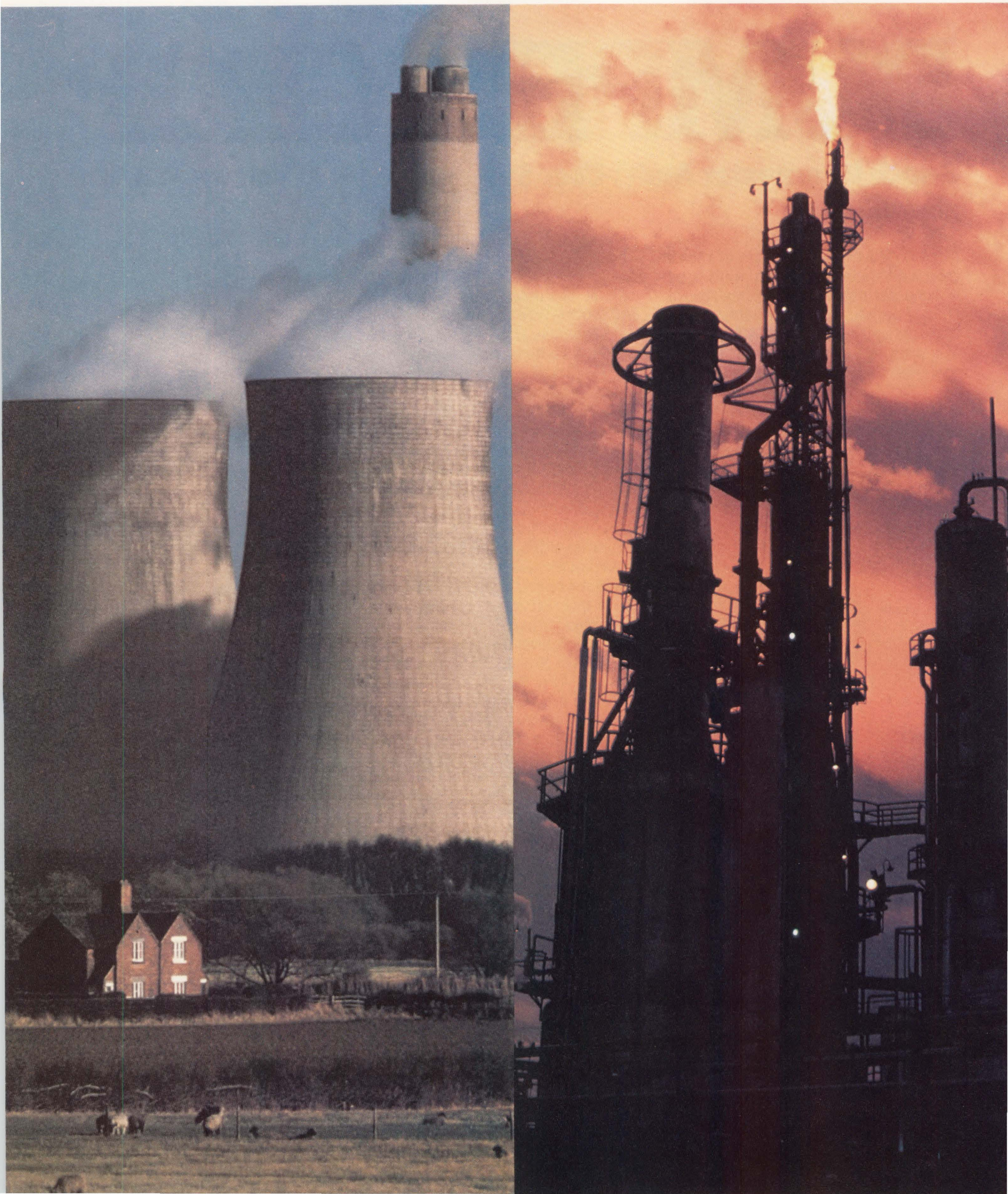
**CP/M and MP/M are registered trademarks of Digital Research, Inc.
†OASIS is a registered trademark of Phase One Systems, Inc.
‡datapro is a registered trademark of Datapro Research Corp.

VRC: Memory Products for



Removable cartridge adds 4M-bytes capacity to 5.25" Winchester drive

Fixed portion of MIKRO-DISC V Winchester disc drive (left) stores 2M or 4M bytes. Cartridge portion of unit (right) uses Winchester technology to provide additional 2M- or 4M-bytes capacity. Together units match dimensions of standard 5.25" (13.34-cm) floppy drive

Using a removable cartridge to store an additional 2M or 4M bytes, MIKRO-DISC V offers the convenience of a removable disc cartridge in the space of a standard mini-floppy. The 5.25" (13.34-cm) Winchester disc drive from New World Computer Co, 3176 Pullman St, #120, Costa Mesa, CA 92626, supplies bubble memory performance using a proprietary low mass multiple-head assembly.

The removable cartridge is a hermetically sealed package complete with multiple-head assembly, media, and actuator positioner. This package measures 5.75 x 7.8 x 1" (14.6 x 19.8 x 2.5 cm) and weighs 1.5 lb (0.7 kg).

Head assembly used in the drives provides 8 or 16 read/write heads. Because of the positioning of the assembly, the capacity of a standard 5.25" (13.34-cm) floppy drive is under the heads at any given time. Access time from one cylinder to another is 5 ms; average access time is 8.3 ms. Data transfers occur at a 6.25M-bit/s rate.

Reliability figures cited for the units claim soft error rates of 1 in 10^{10} bits/head, 1 in 10^{12} bits/head hard errors, and 1 in 10^6 accesses for seek errors for both disc and cartridge. Fixed and removable drives both give 100% copy up/down capability and ensure reliability and portability through the head lifting feature that automatically lifts the heads from the disc surface during power down.

Drives are available in five versions. Model 2/0 offers 2M bytes of fixed storage; the 4/0 offers 4M bytes fixed. Model 2/2 provides 2M bytes of fixed and 2M bytes of removable storage; 4/2, 4M bytes fixed, 2M removable; and 4/4, 4M fixed with 4M removable.

Two interfaces are available. One takes advantage of the drive's performance, directly addressing up to 32 heads at once and providing 450k bytes of data and an average rotational latency of 8 ns. The other maintains compatibility with Seagate or Shugart drives.

Circle 352 on Inquiry Card

Low cost, portable dual-trace scopes achieve 60 MHz

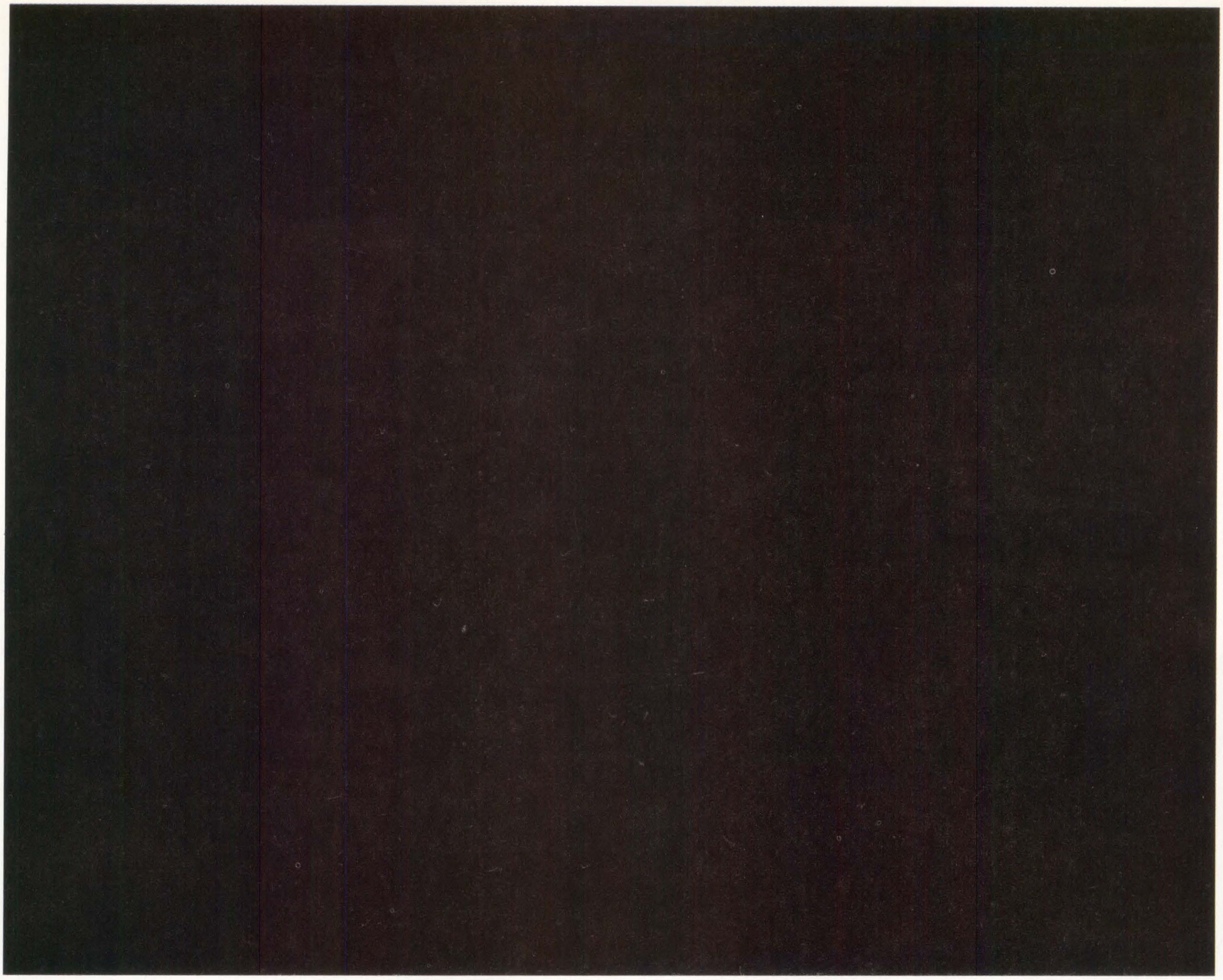
Dual-trace, delayed sweep oscilloscopes that achieve 60 MHz at 20 mV to 10 V and 50 MHz at 2-, 5-, and 10-mV settings, models 2213 and 2215 have a maximum sweep speed of 5 ns/div. Designed to meet growing needs for units in the low to mid performance range, the instruments were developed by Tektronix Inc, PO Box 500, Beaverton, OR 97077, to offer increased performance at lower cost.

The scopes incorporate advanced systems for easy triggering. A vertical mode system triggers on asynchronous signals in dual-channel alternate operation and uses enhanced auto-triggering to minimize the time consuming adjustments. TV line and field triggering offer a wide range of video measurements, and variable hold-off gives stable triggering on long or complex analog and digital signals. Position insensitive triggering provides easy waveform positioning without affecting the triggers.

The 2213, with a single time base, has a screen calibrated delayed sweep with 3% accuracy and an intensified sweep. The 2215 has a dual time base with 1.5% delay time accuracy and includes alternate sweep switching, A/B sweep separation control, and B triggering after delay for jitter free delayed time measurements. Both instruments also provide Z-axis input, front panel trace rotation, and beam finder controls. Fewer operator CRT adjustments are required because the scopes have auto intensity and auto focus. A and B sweeps are maintained at nearly the same intensity regardless of changes in sweep speeds.

Designed for high performance, ease of use, serviceability, and reliability, the scopes have 65% fewer mechanical

(continued on page 57)



In case of memory loss, it's nice to have a number you can call.

Any independent supplier can save you a bundle on add-in/on memories for your DEC minicomputer.

But now, there's one that offers you more than a bargain, a handshake and a piece of paper good for a year.

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They offer you the sensible luxury of a qualified technician who can isolate the problem in a hurry. Whether you're in mid Manhattan or outer Osawatomie (we have over 50 service centers in the United States, Canada and Europe).

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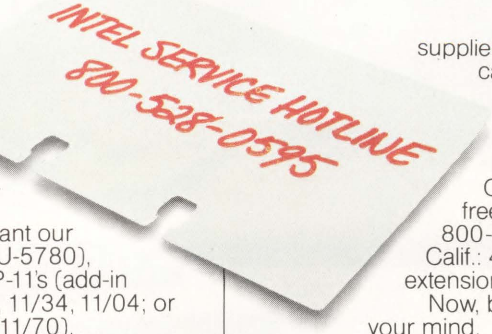
With off-the-shelf replacement boards (90% are on their way to you within 24 hours). Flat rates that won't catch your budget by surprise.

And whatever else we can do to keep your DEC system producing—be it a VAX 750 (in which case, you'll want our MU-5750), 780 (MU-5780), or a number of PDP-11's (add-in CM-5044 for 11/44, 11/34, 11/04; or add-on IN-1671 for 11/70).



And when you need our attention at the snap of a finger, just pick up our toll-free service hot line.

That's a lot of support. Exactly what you'd expect from a company with ten years of reliable leadership in the business. Providing Data General as well as DEC memories. Plus standard and custom memory systems.

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CIRCLE 32 ON INQUIRY CARD

The Lexidata System 3400 Display Processor and full line of interactive peripheral devices are designed specifically for OEMs and sophisticated end-users. The System 3400, rapidly becoming the leader, with over 1,000 units shipped to date, possesses the product characteristics required by this demanding customer group.

• System 3400 *performance* is truly outstanding. Only the System 3400 offers 1280x1024 resolution at 60Hz non-interlaced black-and-white and grayscale capability, or 880x704 resolution at 60Hz non-interlaced color. Our programmable lookup tables are the industry standard of performance. Double buffered memories or multiple lookup tables with bank switchable memories and processor features, such as pan/zoom and 4K WCS, are available.

• System 3400 *quality* satisfies the requirements of Fortune 500 companies, the leading CAD/CAM systems vendors and military and government contractors. We continue to focus on quality because we believe that quality and cost effectiveness are closely related.

• System 3400 *flexibility* ensures a configuration to meet the exact requirements of each customer. The System 3400 offers a complete range of OEM configurations, starting from $7,540, including monitor.

• System 3400 *software* provides a high-level language user-interface to execute graphics and imaging functions. The powerful subroutine library streamlines application software development and facilitates user interaction.

• System 3400 *cost effectiveness* enables even price-sensitive OEMs to configure a highly competitive product. You will be able to maximize your value-added contribution and optimize your overall system performance.

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LEXIDATA CORPORATION

CIRCLE 33 ON INQUIRY CARD

parts, and 90% less cabling than the instruments they replace. A high efficiency power supply design reduces power consumption and eliminates the need for line voltage selection switches (units operate from 90 to 250 Vac, 48 to 62 Hz).

User convenience is improved using two probes designed for the series. These probes provide full bandwidth measurements at the probe tip and are lightweight with flexible cable for convenience. An IC grabber tip provides precise, accurate, in-circuit IC connections.

The series is designed to replace the T900 line (except for T912 and T932A), and the Telequipment line, 442 and 445. The units weigh 13.5 lb (6.1 kg). With optional pouch, probes, and protective front panel cover they weigh 15 lb (6.8 kg) each. The 2213 is priced at $1100 and the 2215 at $1400.

Board level voice units supply high accuracy, low cost recognition

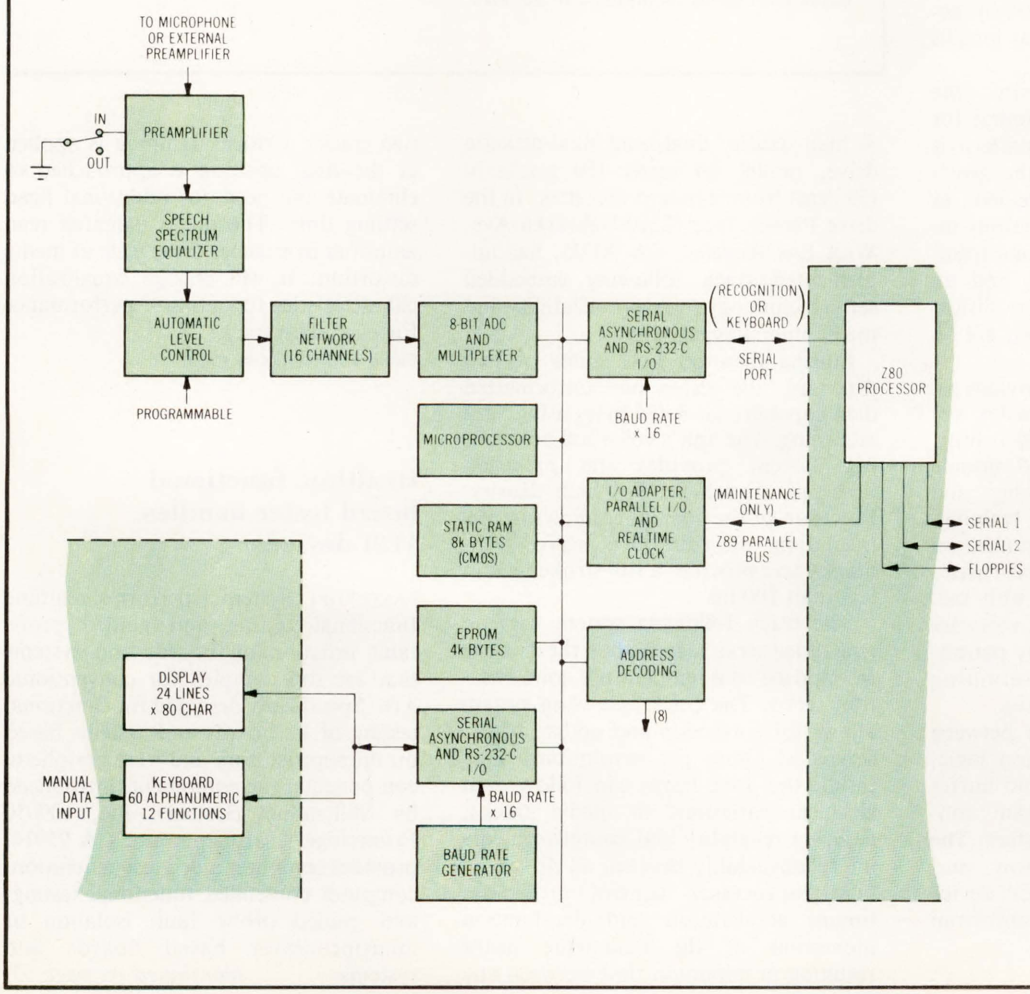
Voice recognition units supply high accuracy voice input capability for integration into various systems. The devices, available from Interstate Electronics Corp, Voice Products Operation, 1001 E Ball Rd, Anaheim, CA 92803, lower data entry costs and enable higher accuracy, while allowing the operator a wide range of movement.

Included in the line are the VRT101, a fully integrated intelligent voice recognition terminal, and the VRT200, an add-on voice recognition capability for Lear Siegler ADM3A and ADM5 video displays. Board level products include a VRQ400 Q-bus board and a VTM 150 Multibus board that offer 1500 words of voice response.

Combining dual Z80 processors and 48k-byte memory with an 80-char by 25-line display, keyboard, floppy drive, and 100-word voice recognition module (VRM), the VRT101 accepts and processes input data from either the keyboard or the voice unit. One microprocessor services display and keyboard while the second serves as a programmable host computer. The host CPU is supplied with 48k bytes of RAM and two serial RS-232-C ports for communication to central host, printer, or telecommunications channel.

Speech input is analyzed by a 16-channel spectrum analyzer and converted to a digital representation of the characteristics of the spoken input. This digital data is then converted to a fixed size pattern that preserves the information content of the spoken inputs while discarding redundant features. During word training, these patterns are used to

(continued on page 58)



Integrating voice recognition in a diskette based terminal, VRT101 combines dual Z80 microprocessors and intelligent CRT display with 100-word voice recognition module. Unit accepts and processes data independently from either keyboard or voice source derive templates for each vocabulary item. The templates are then used for comparison with incoming spoken words. Recognition capability is accomplished without use of the Z80 host processor or its RAM, therefore the VRM has no impact on the host's capabilities. This dual PC board automatic speech recognizer consists of a microprocessor, 8k bytes of ROM, 8k bytes of RAM for reference pattern storage, analog circuitry for speech spectrum analysis, and interface electronics.

The terminal supports the CP/M operating system and standard utility programs. Voice functions are provided via the VOICE utility program. Utility software enhances system design and through adaptive training, minimizes the need for end user knowledge of training and system optimization.

Designed for use in Lear Siegler ADM 3A and 5 video displays, the VRT 200 is a total hardware/software system designed to install without modification to existing software. All logic necessary to recognize 100 words with 99%+ accuracy is on a single board that installs without special tools.

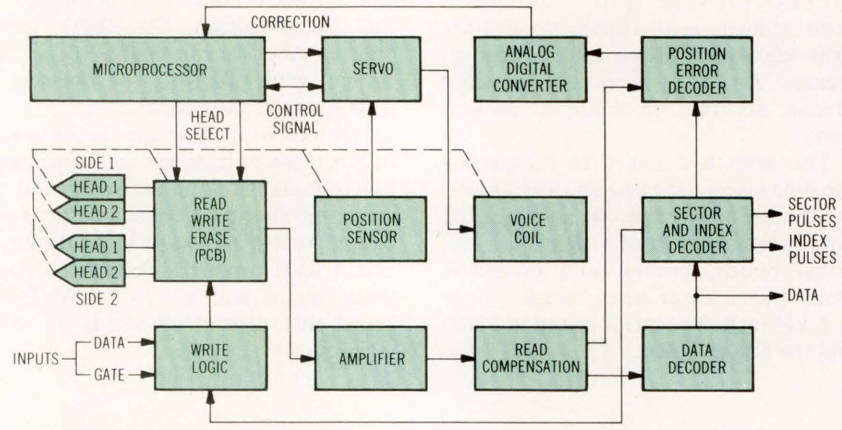
A speaker dependent device, the board requires vocabulary training for each user. Once a reference pattern is built, it can be uploaded to the host's mass storage, then downloaded as needed. All voice specific functions including vocabulary definition and training, reject threshold control, and an editor to support creation and modification of application vocabularies, are on the board.

The Q-bus VRQ400 module provides accurate recognition of a 100-word vocabulary on command of an LSI-11 host. The module, housed in a quad module board slot, contains all logic and memory necessary to perform training, word recognition, and communication protocol independent of the user's operation mode. Compatible with DEC software using RT-11, support software augments the VT103 terminal by permitting voice input while retaining keyboard and display capabilities.

In addition to an interface between the Q-bus and voice recognition logic, the board provides the logic and buffer registers necessary for program controlled parallel 8-bit data transfers. The interface provides selection and decoding of user selected 16-bit device address and transfers data to and from the Q-bus.

Circle 354 on Inquiry Card

Drive uses hard disc techniques to store 8M bytes on floppy media



Storing 8M bytes on two standard diskettes, model 899 uses track following embedded servo technology to achieve 150 track/in density in drive that matches standard floppy form factor

A high density dual-head/dual-diskette drive, model 899 reads 150 tracks/in (59 /cm) from standard diskettes. In the drive PerSci, Inc, 12210 Nebraska Ave, West Los Angeles, CA 90025, has implemented track following embedded servo technology to assure reliability and media interchangeability.

Storing data on both sides of two diskettes, the drive has unformatted data capability of 8.4M bytes using MFM recording. The unit's voice coil positioning system provides the precision necessary to achieve this high density. Precision of the positioner allows implementation of embedded servo technology and provides a full stroke seek in less than 100 ms.

The track following system uses an embedded servo recorded on the diskette as opposed to a temperature compensation servo. The track following system allows for correction and update of the servos 32 times per revolution. As a result, the drive heads can follow even elliptical variations in media tracks, assuring reliability and complete media interchangeability between all drives.

Microprocessor control gives optimum acceleration and deceleration movement of the read/write heads resulting in minimum time between any two tracks. Critical damping is applied as the final position is approached to eliminate the need for additional head settling time. The unit's patented read amplifier overcomes the effects of media distortion. It will change equalization characteristics to optimize performance for each data track.

Circle 355 on Inquiry Card

Realtime functional board tester handles VLSI devices

FASTPROBE System I performs realtime functional testing and guided probe fault isolation on boards and systems that are too complex for conventional ATE. Specifically designed for functional testing of PC boards and systems based on microprocessors and VLSI peripheral components, the equipment, introduced by Millennium Systems, Inc, 109050 Pruneridge Ave, Cupertino, CA 95014, provides computer aided test generation, computer controlled functional testing, and guided probe fault isolation of microprocessor based boards and systems. *(continued on page 63)*

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Long the recognized leader in quality open-frame linears, Power-One is now setting the pace in switching power supplies.

Our fast growing line of efficient high-performance switchers offer a combination of features not found in others at these low prices. Features such as fully regulated outputs, 115/230 VAC input capabilities, superior hold-up time, and totally enclosed packaging for enhanced safety. Additionally, these models incorporate many other innovative ideas that set our switchers apart... while reflecting the same simplicity of design that has kept our open-frame linears the most cost-effective in the industry.

Best of all, Power-One switchers are 100% American built by Power-One personnel, at Power-One facilities, and under tough Power-One quality control standards. Adding up to total dependability at typical Power-One low prices.

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VOLTS	AMPS	MODEL
5V	40A	SK5-40
12V	16.8A	SK12-16.8
15V	13.4A	SK15-13.4
24V	8.4A	SK24-8.4
28V	7.2A	SK28-7.2
SIZE: 2"H X 4.88" W X 13"L		

$250
200 WATTS

OUTPUT	VOLTS	AMPS
#1	5V	20A
#2	12V	5A
#3	−12V	3A
#4	5V, 12V, 15V, or 24V. USER SELECTABLE	3.5A
SIZE: 2"H X 4.88"W X 14"L		
MAX OUTPUT POWER: 150 WATTS CONTINUOUS, SUM OF ALL OUTPUTS		
150 WATTS - 4 OUTPUTS THE UNIVERSAL SHQ-150W		

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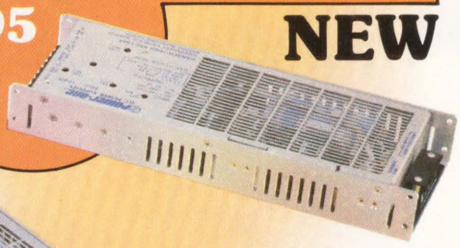

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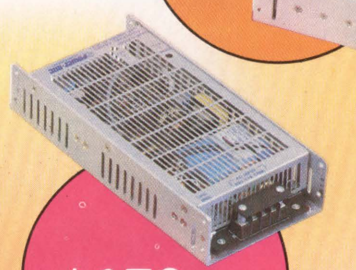
50 WATTS

VOLTS	AMPS	MODEL
5V	10A	SD5-10
12V	4.2A	SD12-4.2
15V	3.4A	SD15-3.4
24V	2.1A	SD24-2.1
28V	1.8A	SD28-1.8
SIZE: 2"H X 4.88"W X 6.25"L		



$170
100 WATTS

VOLTS	AMPS	MODEL
5V	20A	SF5-20
12V	8.4A	SF12-8.4
15V	6.7A	SF15-6.7
24V	4.2A	SF24-4.2
28V	3.6A	SF28-3.6
SIZE: 2"H X 4.88"W X 10"L		

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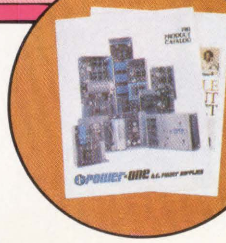

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CIRCLE 34 ON INQUIRY CARD


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For connectors and cable systems... Molex has the answer.

IDT . . . Insulation Displacement Technology.

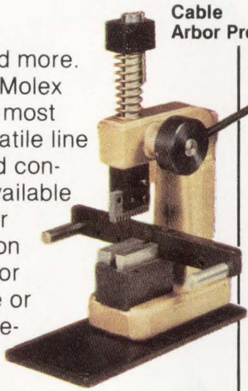
Planar cable technology was first developed to meet the aerospace industry's need for lighter and more compact electronic systems packaging while enhancing electrical characteristics. Since then, it has evolved rapidly to its present level of development mainly because industry was quick to recognize the tremendous advantages it had to offer in an extremely wide variety of product applications.

Now, Molex has taken the state-of-the-art one step further by joining connector technology and planar cable with fully automated termination equipment. This gives the designer, components engineer or production manager a totally integrated system capable of meeting the most exacting standards or adapting to the most demanding configurations.

Today's electrical or electronics manufacturer bases his selection of terminal connections on a number of key considerations:

- *Compact size* to save space in high density situations.
- *Flexibility* for greater durability and longer flex life.
- *Reliability* for precision center-to-center spacing critical to proper termination.
- *Performance* in terms of mechanical properties and current carrying capabilities.
- *Versatility* for adaption over a number of application uses.
- *Lower installation cost* to yield greater profitability.

The Molex IDT cable and connector system lets you meet all these goals . . . and more.


Cable Arbor Press

Over the years, Molex has developed the most complete and versatile line of mass terminated connector products available anywhere. Whether your interconnection requirements are for signal-level voltage or your application presents a packaging density problem, Molex's IDT system offers you a solution. And your options include discrete or planar cable terminations...or *both*, in the same connector.

Cost savings up to 40%

The Molex IDT system can lower your applied costs from 30% to 40% by replacing the strip-crimp-and-insert steps with one simultaneous mass termination operation.

But the connectors and cable are only half of the system. The greatest advantage the Molex IDT system offers is the full range of application tooling; from single-wire hand tools to fully automatic assembly machines for both discrete wire and cable assembly.

For discrete wire termination, we have an arbor-type press, a semi-automatic single wire terminating machine, a harness board assembly tool (completely compatible with your present harness board) or an automatic, multi-wire assembly machine.

Mini Cam III Semi-Automatic Terminator

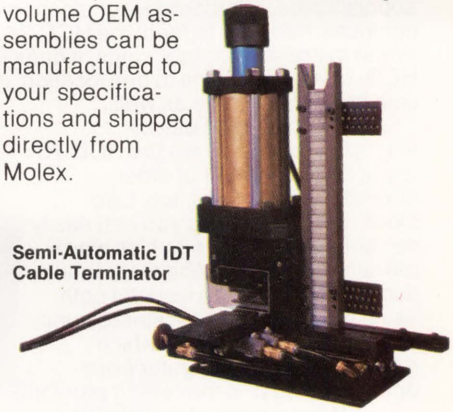
For cable termination, we can offer an arbor-type press, a semi-automatic terminator or a fully automatic cable assembly machine that will put connectors on one or both ends of cable or discrete wire of various lengths at the rate of up to 18,000 terminations per hour.

Many of these unique application tools are available for demonstration right in your own plant. Or, if you prefer, one of the Molex Equipment Demonstration Vans can pay you a visit and show you the complete array of tooling available to help you lower your costs.


Harness Board Assembly Tool

Molex and distributors offer you cable system assemblies.

Molex offices and distributors worldwide have the equipment to manufacture your assemblies quickly and economically with in-stock products and materials. High volume OEM assemblies can be manufactured to your specifications and shipped directly from Molex.


Semi-Automatic IDT Cable Terminator

◀ **This automatic cable assembly machine puts connectors on one or both ends of various lengths of cable, discrete wire, or a combination of the two, at a rate of up to 18,000 terminations per hour.**

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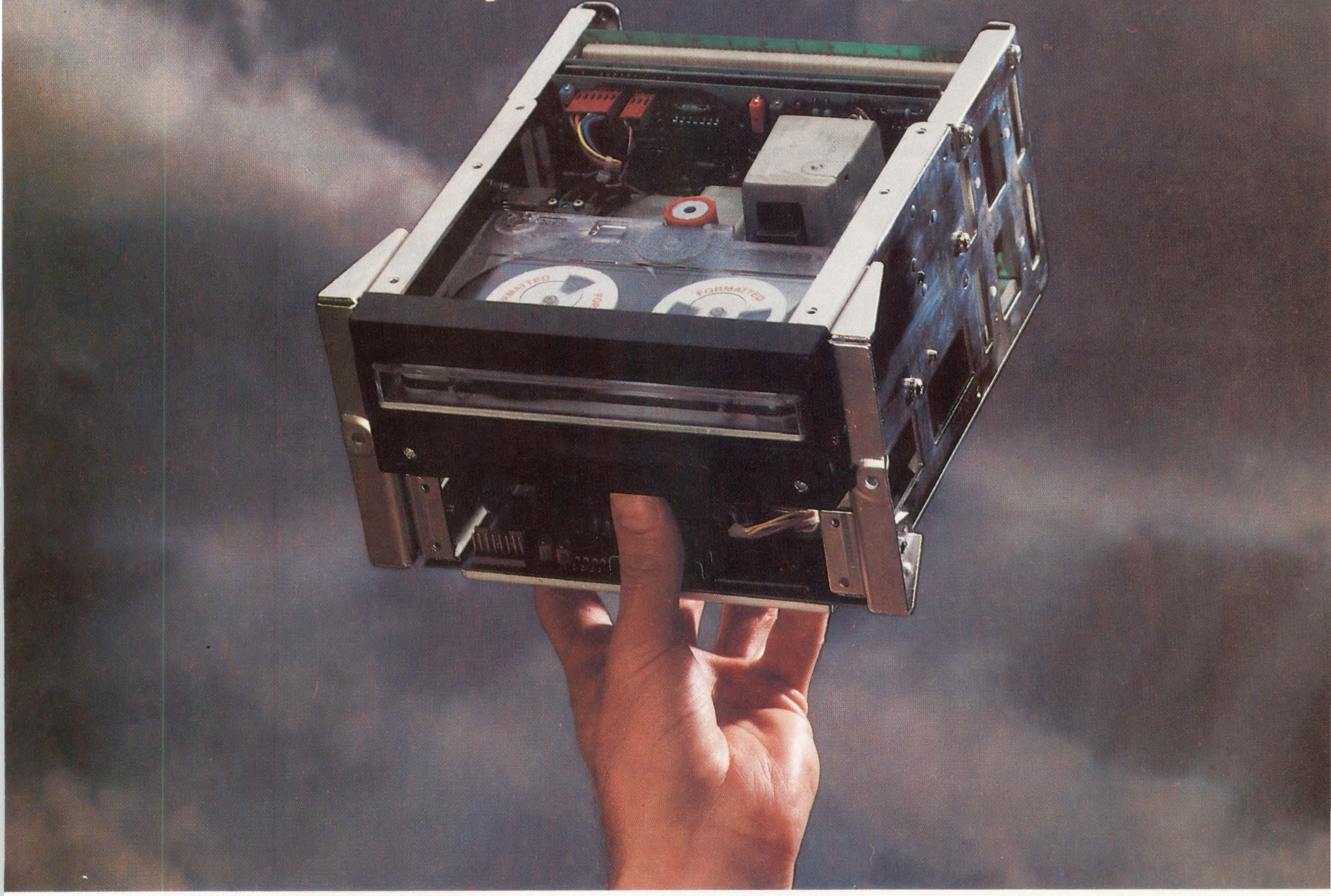
CIRCLE 35 ON INQUIRY CARD

Never Before Has A Back-up System Been As Intelligent As The System It's Backing Up.



This is the 3M Brand HCD-75 High Capacity Data Cartridge Drive. And the reason it's as intelligent as a computer is because it thinks like one.

You see, unlike other back-up systems, the HCD-75 is interfaced directly with the primary system by means of sophisticated, microprocessor electronics. When the host computer has data to feed, the HCD-75 starts automatically. When the host computer stops, it does too. And since the HCD-75 also positions to any location, it not only saves tape cost but retrieval time as well.

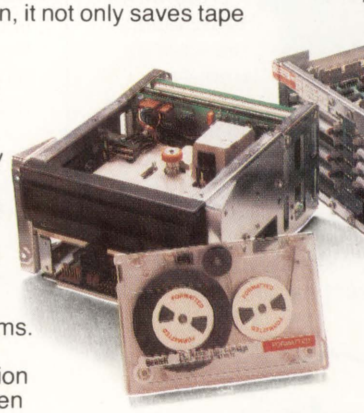
Of course the use of microprocessors allows the HCD-75 to perform a number of other time-saving functions, too. Like block replacement, so you can easily correct errors or change files which pertain to updating. And fast random access which makes it useful both as an I-O device or as a storage unit for low-usage files. All of which relieves the host computer from difficult timing and formatting problems.

What's more, the HCD-75 features state-of-the-art error detection and correction capabilities. Even when the system is off-line, self-test diagnostic routines monitor its performance. And, combined with each of its high-capacity cartridges, the HCD-75 provides a full 67 megabytes of formatted user information (144 mbytes unformatted). So costly operator interventions are sharply reduced.

If you're looking for a reliable, cost-effective solution to the problem of disk back-up, the 3M Brand HCD-75 High Capacity Data Cartridge Drive is the system you should be thinking about.

Not only has a lot of thinking gone into it. But a lot of thinking comes out of it, too.

For more information, check the listing on the next page for the representative nearest you. Or write: Data Recording Products Division/3M, Bldg. 223-5N 3M Center, St. Paul, MN 55144.



The Back-up System That's Suddenly Way Out Front.

CIRCLE 36 ON INQUIRY CARD

It uses incircuit emulation for functional testing and signature analysis for fault isolation. These techniques are applicable to any board or system using a microprocessor. Functional testing is performed in realtime as is fault isolation. Marginal components within a system are detected and isolated.

Consisting of an LSI-11/23 host, video terminal, 1M-byte disc storage, and model 4500 MicroSystem Analyzer test station, the system is modularly upgradable to a multistation test network. Shared resources in the multistation version include hard disc and test development station.

Production testing can occur in two modes. The first uses all facilities of the system. The test station connects to the system under test via the microprocessor socket. Test routines transmitted from the host are executed out of the station's emulation memory; test results are transmitted from the station to the host, and the computer determines whether a board is good or bad. Bad boards are diagnosed using signature analysis. The computer displays a node to be probed on the station's display, the operator probes the node, and the signature is sent back to the computer for comparison. The computer continues to read signatures and direct probing until the bad node is found.

The second mode involves use of a standalone test station. Either the 4500 supplied with the system or the 4000 portable tester may be used. The system is used to burn test routines into 2708 or 2716 P/ROMs, which can be inserted into sockets on the front panel of either tester. Tests are executed from the P/ROMs, and results are displayed on the tester display. The system also outputs fault trees that list the signatures for each possible data path and provide a semiautomatic means for isolating faults to the node level.

Circle 356 on Inquiry Card

Desktop computers increase processing speed, offer distributed capability

Users gain 2 to 5 times more computational power by using the multilanguage HP 9826A desktop computer and additions to the HP 9845 system line. In addition, Hewlett-Packard Co, Desktop Computer Div, Fort Collins, CO 80521, announced distributed systems capability that enables the computers to become integral parts of the company's distributed systems network. The units offer increased processor power to enhance the personal productivity of users in computer aided test and engineering applications.

Characteristics of the 9826A adapt it to use in computer aided test, while its computational speed makes it effective in computer aided engineering and manufacturing. Contributing to its speed and versatility are an internal MC68000 CPU with 8-MHz clock rate, and integral flexible disc drive. Built-in IEEE-488 capability simplifies configuration of computer controlled systems using the interface.

The unit has a 7" (18-cm) CRT with 10 programmable soft keys whose labels can be displayed. It also provides 15 levels of priority program interrupt and makes 512k bytes of memory available to the user. A data communications interface supplies both asynchronous protocol and DSN data link protocol; IEEE-488 interface is built in. Graphics capability offered by the unit allows computation results to be displayed graphically on the CRT using a 400 x 300-dot raster or to be converted to hard copy via an external printer or plotter.

Designed for use with the computer, thermal printers offer 120-char/s bidirectional printing using flat fanfold paper. HP 2671A provides the 128-char ASCII set, line drawing character set, and Roman extension set for special national characters. In addition, the 2671G offers raster graphics with 90 dots/in (35/cm) resolution to produce dot for dot hard copies from the screen. The 2673A adds raster graphics functions and print and character set enhancement to features of the other printers.

Additions to the 9845 computer line provide monochrome and color graphics displays. The monochromatic display can produce 17 shades of brightness for area fill; the color unit, 4913 distinguishable colors of fill. The processors run computation intensive programs three times faster than previous versions. To achieve this, a microprogrammed bit slice processor replaces the language processing unit.

Firmware/software for the units offers a data communications package that provides distributed system networking, allowing desktop systems to link with HP 1000 or 3000 systems. Other packages include an assembly programmer's translator utility and a plug-in ROM that supplies structured programming commands to increase programmer productivity and facilitate software maintenance.

Circle 357 on Inquiry Card

Desktop computer supplies both Winchester drive and cartridge tape backup

Desktop computer SYST-23VTJ features a 28M-byte 8″ (20-cm) Winchester drive with 0.25″ (0.64-cm) cartridge tape drive as backup. A companion to the LSI-11/23 based system, SYST-23VZJ is configured with 28M-byte 8″ (20-cm) Winchester and 1M-byte double-sided floppy.

In the SYST-23VTJ, Plessey Peripheral Systems, 17466 Daimler, Irvine, CA 92714, provides the power and storage capacity of a multiple-user system and the necessary backup for most data and word processing applications in a desktop cabinet. The system uses the PDP-11 instruction set, 128k-byte memory, 8″ (20-cm) Winchester drive, and cartridge tape backup. The Winchester subsystem uses the PM-FCV06 single-quad wide controller board and one 28M-byte PM-FDV06J Winchester fixed disc drive. The controller will interface up to four drives if additional capacity is needed. The 15M-byte cartridge tape subsystem, PM-CSV11 satisfies backup requirements using removable DC300-type cartridge tape. Operating in streaming mode under software control the controller supports up to four tape drives.

Circle 358 on Inquiry Card

High throughput system provides data analysis for discrete device testing

T357 tests a broad range of device types, simplifies program generation, and supplies online data reduction. The discrete semiconductor test system's 64k memory permits job development without impacting throughput. The system also provides dual 3M tape drives and a comprehensive software package for use by inexperienced personnel. An improvement of the T347C from Teradyne, Inc, 35 Morrissey Blvd, Boston, MA 02125, the system can perform wafer probe, final test, quality assurance, incoming inspection, or evaluation on devices including bipolar transistors, diodes, SCRs, triacs, FETs, optocouplers, and transistor and diode arrays.

The system has basic mainframe capabilities of 16 A for conducting tests and 400 V (600 V pulsed) for leakage and breakdown tests. Options extend these to 160 A and 2000 V for power device testing. A low current measurement option performs FET leakage measurements down to 100 fA with 10-fA resolution. A thyristor testing option meets requirements for accurate thyristor testing including accurate, predictable, and clean test pulses preventing false triggering due to dv/dt and variable test time for holding current testing.

Device libraries permit users to prepare job plans from memory, shortening job preparation time. An online help list aids programmers by providing the name and function of all keyboard commands, names of all tests that may be used with each module, or names of all modules loaded in memory.

Online data reduction performed by the system can be used to generate histograms, cumulative curves, or probability curves graphically displaying lot variations as an aid to process control. Correlation analyses performed logarithmically over up to four decades between two datalogged parameters permit accurate display of large dimensions of data that can cover decades of values.

Circle 359 on Inquiry Card

16-bit desktop computer offers alternative to timesharing mainframe

Processing full ANSI FORTRAN 77 and Pascal software under its UNIX-like MERLIN operating system, the CTS-300 offers the capabilities of a large minicomputer in a desktop package. Developed by Codata Systems Corp, 285 N Wolfe Rd, Sunnyvale, CA 94086, the unit combines an M68000 CPU, 256k bytes of high speed cache memory, and intelligent high speed control devices on one Multibus card. CRT and independent keyboard and floppy and Winchester disc drives are also incorporated.

Significantly, the system directly addresses up to 1.5M bytes of memory without segmentation. Programs can be up to 1.5M bytes long. Because differentiation between code and data is dynamic and optional, there is no limit on FORTRAN array or Pascal procedure size.

Software for the system includes ANSI-standard FORTRAN 77 and Pascal compilers so that software written for mainframes can run without change. A 68000 assembler and linker allow Pascal and FORTRAN to be linked to assembly language programs. The FORTRAN compiler has been benchmarked at 7000 lines/min.

Circle 360 on Inquiry Card

THE WINCHESTER ALTERNATIVE

HIGH CAPACITY, I/O, BACKUP

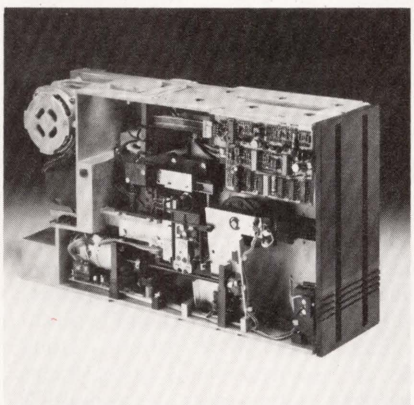
Until now, you thought only a fixed disk could give you the high capacity, speed and reliability your system needs. Until now, you were right.

Before today, you were considering buying a Winchester for mass storage, a floppy for I/O and a cartridge for backup. Before today, you didn't have much choice.

But now, you can get what you need in high capacity *flexible* disk drives—3.2, 6.4 and 8.4 Mbytes (with more on the way) from the world leader in high technology floppys—PerSci. Diskette drives that are their own I/O and their own backup so you buy just one drive, not three!

And PerSci high density drives do *not* use exotic media or expensive cartridges like some you've been reading about. PerSci drives store more bytes than a floppy could ever store before on standard, off-the-shelf diskettes.

How did PerSci do it? We started with voice coil positioning—the "big disk" positioning technology which makes PerSci drives 3 to 6 times faster than other floppys (1 ms track to track), far more precise in positioning and gives the drives reliability approaching hard disks. The unique accuracy of the voice coil has made it possible for PerSci to design a truly effective dual diskette drive—that is, two diskettes housed in one drive the size of a standard



8 inch floppy. Add dual head techniques to that high reliability and you have two heads reading double density data on both sides of two diskettes in one compact package. In other words you have a PerSci Model 299B with data storage of 3.2 Mbytes—the perfect storage capacity for a wide variety of applications.

And if you need twice as much data, PerSci has it in the Model 699 diskette drive. The extreme precision of the PerSci positioner has allowed PerSci to make the move to 96 tpi (the first 8 inch drive to reach this density) with no major redesign. This means you get *proven* technology in a PerSci 6.4 Mbyte drive.

To take the next capacity step PerSci has added to this proven high technology design the first true track following servo system ever to be implemented on a floppy disk drive. This unique system, so precise it can follow even elliptical variations in media tracks, allows PerSci drives to store 8.4 Mbytes of data on 150 tracks per inch with complete reliability on absolutely standard removable media. And this is just a sample of what this system can do.

So before you spend money and time on Winchesters and low performance floppys and cartridge drives with multiple controllers (and before you start betting on tape for backup)—consider the alternatives. PerSci drives are microprocessor based, have a patented hub and cone assembly for ultra-reliability and a unique low noise read amplifier. They have all the benefits you can expect from hard disks—with the removable, low cost, mailable, stackable floppy media that is the standard of the industry. So now that you've got a choice, choose a PerSci high density floppy—the Winchester alternative.

Call or write today for information to PerSci, Inc., 12210 Nebraska Avenue, West Los Angeles, CA 90025. (213) 820-7613. Telex 687-444.

PERSCI

Peripherals a Generation Ahead.

CIRCLE 38 ON INQUIRY CARD

Printer offers choice of operating speed and dot density

Variable speed TASKMASTER MVP2 adapts to virtually any printing application, including multitask operations, distributed data networks, and heavy duty industrial uses. In the unit, Printronix, Inc, 17421 Derian Ave, Irvine, CA 92713, has incorporated a number of technological innovations, including variable print speed operation with corresponding dot densities, and a self-driven hammer shuttle assembly.

Print speeds are operator or computer selectable for 80 lines/min with 100 x 100 dots/in^2 (39 x 39/cm^2) for correspondence/word processing applications; 150 lines/min with 60 x 72 dots/in^2 (24 x 28/cm^2) for data processing output; and 200 lines/min with 66.7 x 66.7 dots/in^2 (26.3 x 26.3/cm^2) for compressed character printing on smaller forms.

The simple hammer spring in the mechanism provides higher impact energy than competitive units. This higher energy allows use of a larger dot size, even when printing on 6-part paper, so dots can be made to overlap at data processing print speeds.

The characters of correspondence quality print are close together. A 13 x 9 matrix produces solid, well-defined characters. Because of the hammer's high energy, word processing quality can be printed without reducing speed.

The printer's self-driven shuttle mechanism features a linear motor integrated into the assembly. This allows the unit to operate at noise levels of less than 60 dBa in a compact 12 x 20 x 24" (30 x 51 x 61-cm) desktop size. Design of the integral shuttle moves the hammer bank from side to side across the paper a distance of less than 1" (2.5 cm). In this way, it creates a line of dots. The integral linear motor and the energy-conserving reversal springs permit construction of a compact lightweight mechanism.

Microprocessor control permits the host computer to change from data processing speed to word processing quality, or to plot at any one of three different speeds, by electronic command. High dot density allows system flexibility by providing compatibility with many existing graphic systems.

The printer offers a repertoire of capabilities that include 6-part forms, business graphics, plotting, forms generation, labeling, OCR, and bar codes. Other standard features are double-height printing, character printing, underlining, and electronic vertical formatting. Options provide users with foreign, special, and expanded character sets, a manual forms length selector, a static eliminator, and an RS-232-C interface.

Circle 361 on Inquiry Card

Digital image processor eases operation by accepting voice input

A speech recognition system that operates with a digital image processing system fits applications where hands-off use is necessary. The system, resulting from basic research and development performed by 3M Co's central research group, has been refined to meet specific requirements of image processing by Comtal Corp, 505 W Woodbury Rd, Altadena, CA 91001.

The system can process more than 100 command words or short phrases, can string two separate commands together, and is programmed to respond to an individual user's voice pattern. Using voice to issue commands to the image processing system eases the operator's task in dimly lit photo-interpretation areas, in harsh remote environments, and in medical research.

The system is first trained to a voice pattern by having the user record the vocabulary of commands. Then, as the user issues commands, the system compares the pattern to the voice signature stored in a series of lookup tables. Once a match is made, a string of ASCII characters is sent to the image processing system and becomes the command signal to the system.

In operation, two separate command words or phrases may be strung together and used to form another command. A preprogrammed set of windows limits the commands that may be combined with each command word or phrase.

Responding to voice commands, the Vision One/10 is an interactive standalone image processing system that operates in realtime. Its memory has capacity for up to four 512 x 512 x 8-bit images and up to four 512 x 512 x 1-bit graphic planes. Using an LSI-11/2 computer/controller with a P/ROM operating system, the unit has a 8-bit in to 24-bit out pseudocolor processor with 8 red, 8 green, and 8 blue. A zoom feature based on pixel representation provides image enlargement by factors in 1X, 2X, and 4X.

Circle 362 on Inquiry Card

Benchtop system handles parametric/functional testing of LSI and memory devices

Performing dc parametric and functional testing of digital devices ranging from SSI to LSI and memories, the 1732K handles incoming inspection. The benchtop microprocessor controlled unit from GenRad Inc's Component Test Div, 300 Baker Ave, Concord, MA 01742, delivers capability and performance comparable to those of larger, more expensive systems. An added Kelvin measurement feature ensures the integrity of critical test signals and maintains accuracy of test results.

High throughput is supplied by the multiprocessor architecture. A Z80 with 64k bytes of RAM controls the system and operates the CRT display. A second processor operates the system's magnetic tape mass storage unit. A third high speed pattern processor applies test vectors to the device under test at rates up to 2 MHz. Test vectors are stored in a large pattern memory with 4k x 4 bits of storage for each driver/sensor pin. Test pattern entry is aided by a unique learn mode whereby the response portion of the truth table is derived from a known-good device.

The system permits Kelvin connections to a device remote from the test system, an important consideration when interfacing to automatic handlers and probers. Operating system software performs a Kelvin self-test for verification of contact closure on automatic handlers.

System interfaces include IEEE 488 bus and 20-mA current loop. These data ports allow test programs to be loaded from another computer, or test results to be transferred to printers, calculators, or computers.

Simplified operation and programming are supported by making control decisions selectable from a menu of options displayed on the system's built-in CRT. Program generation and modification are facilitated by special programming keys and displays. No special program language is required.

Circle 363 on Inquiry Card

Develop more programs without developing more programmers with STARPLEX II.™

Introducing STARPLEX II, the fast and easy development system that makes more efficient use of your development time.

The fastest development cycles yet are taking place on STARPLEX II with ISE™ (In-System-Emulator), the maximum support development system.

With its increased memory space and high level language support, STARPLEX II is the logical choice for programmable devices, such as the NSC800, Z-80,® 8080 and 8085. Like STARPLEX,™ it supports our INS8048, INS8049, INS8050, INS8070, COPS™ Family of microcontrollers, PROMs, PALs and our entire BLC SuperChip™ board level computers.

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ISE puts programmers out front with fast development cycles. The ISE module allows you to see exactly what's happening in the target system during emulation, either step-by-step or in real time.

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STARPLEX II was designed for maximum ease of use. Its highly interactive software provides on-screen menus for function selection and makes each task as easy as possible to learn and use. User definable function keys allow most frequently used programs to be loaded with a single key stroke.

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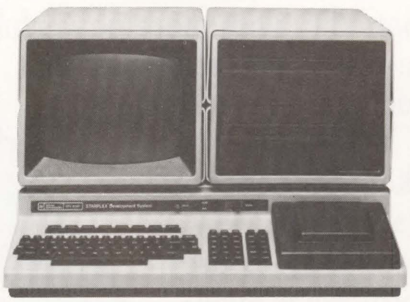

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CIRCLE 39 ON INQUIRY CARD

IF YOU WANT TO START YOUR OWN COMPUTER COMPANY, YOU NOW HAVE THE COMPUTER TO START WITH.

The entrepreneurial spirit runs rampant in the computer industry. In fact, it's come to our attention that a significant number of the technical/engineering types have some thoughts of starting their own company.

So we have come out with a computer for them. And for those entrepreneurs within companies who are in a hurry to get their hot new project to market in a hurry.

It's called the MPT/100.

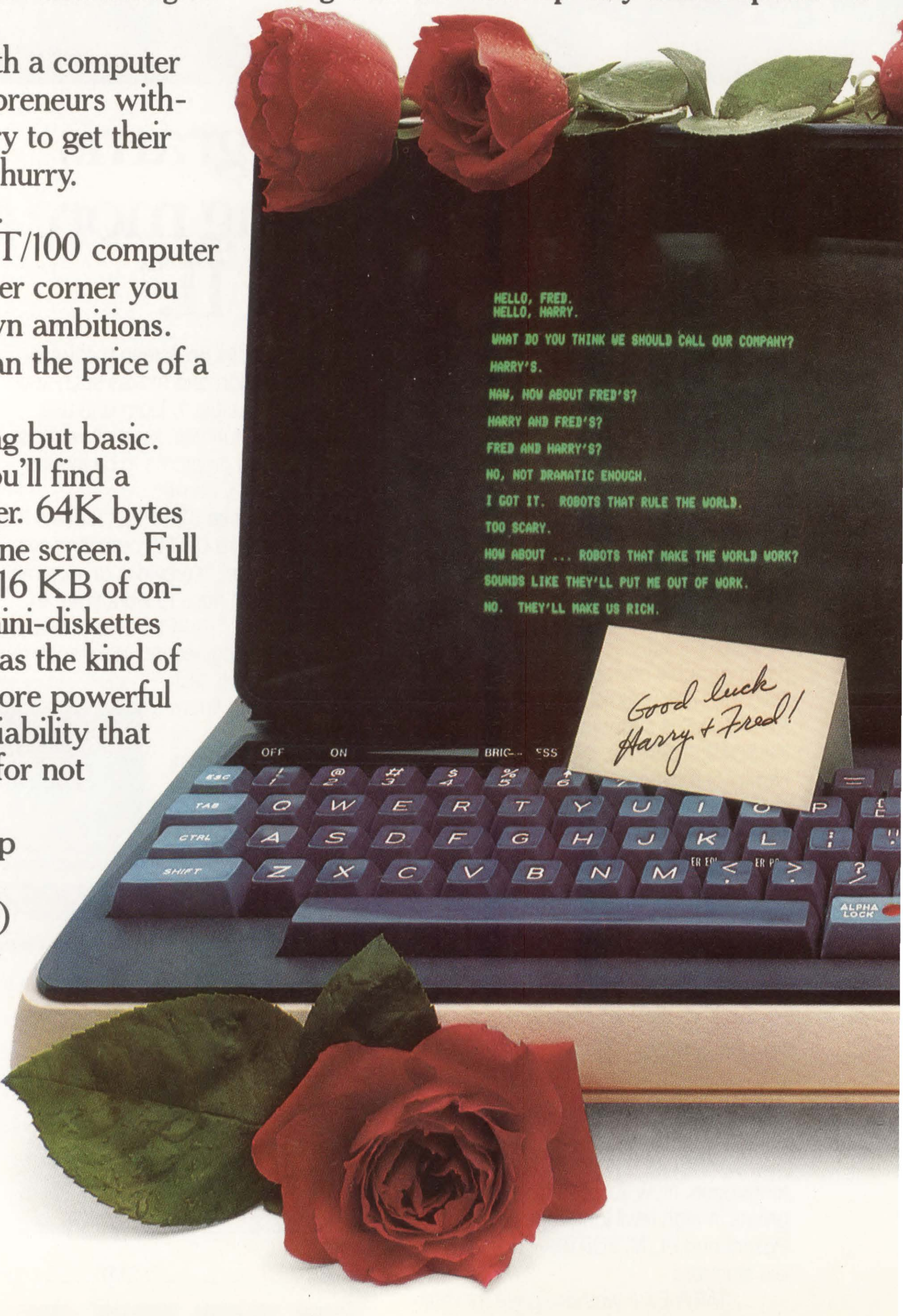
As you can see, the MPT/100 computer is small enough to fit in whatever corner you set aside for furthering your own ambitions.

And it'll cost you less than the price of a basic new car.

This computer is anything but basic.

Inside the MPT/100, you'll find a 16-bit microNOVA™ computer. 64K bytes of memory. 80 column by 24 line screen. Full keyboard with numeric pad. 716 KB of on-line storage on two 358 KB mini-diskettes all packaged in a system that has the kind of software, compatibility with more powerful computers, ease-of-use and reliability that desk-top computers are noted for not having.

Also unlike most desk-top computer software, some very sophisticated (read easy-to-use) big computer software is available for the MPT/100 computer: A multi-tasking FORTRAN that meets all the ANSI standards. A PASCAL that executes at assembly language speeds. An ANSI compatible BASIC that lets you write enormously complex programs that take up only a little space. A



full range of user-friendly interactive programming aids. And MP/OS, an operating system anyone who's into operating systems will tell you is one of the most advanced in the world.

(Anyone who considers any of the above to be of trivial importance should consider the fact that a single line of application code costs a good deal more than many microcomputers. And that cost is only going one way.)

Saving money on programming is only part of the attraction of the MPT/100. It also saves you time. So you can get your company up and running before anyone can do the same thing.

As you grow, all the software you've written, all the peripherals you've interfaced, all the blood, sweat and tears you've put into your company will grow with you. Because we've invested no small amount of energy working to make our computers compatible.

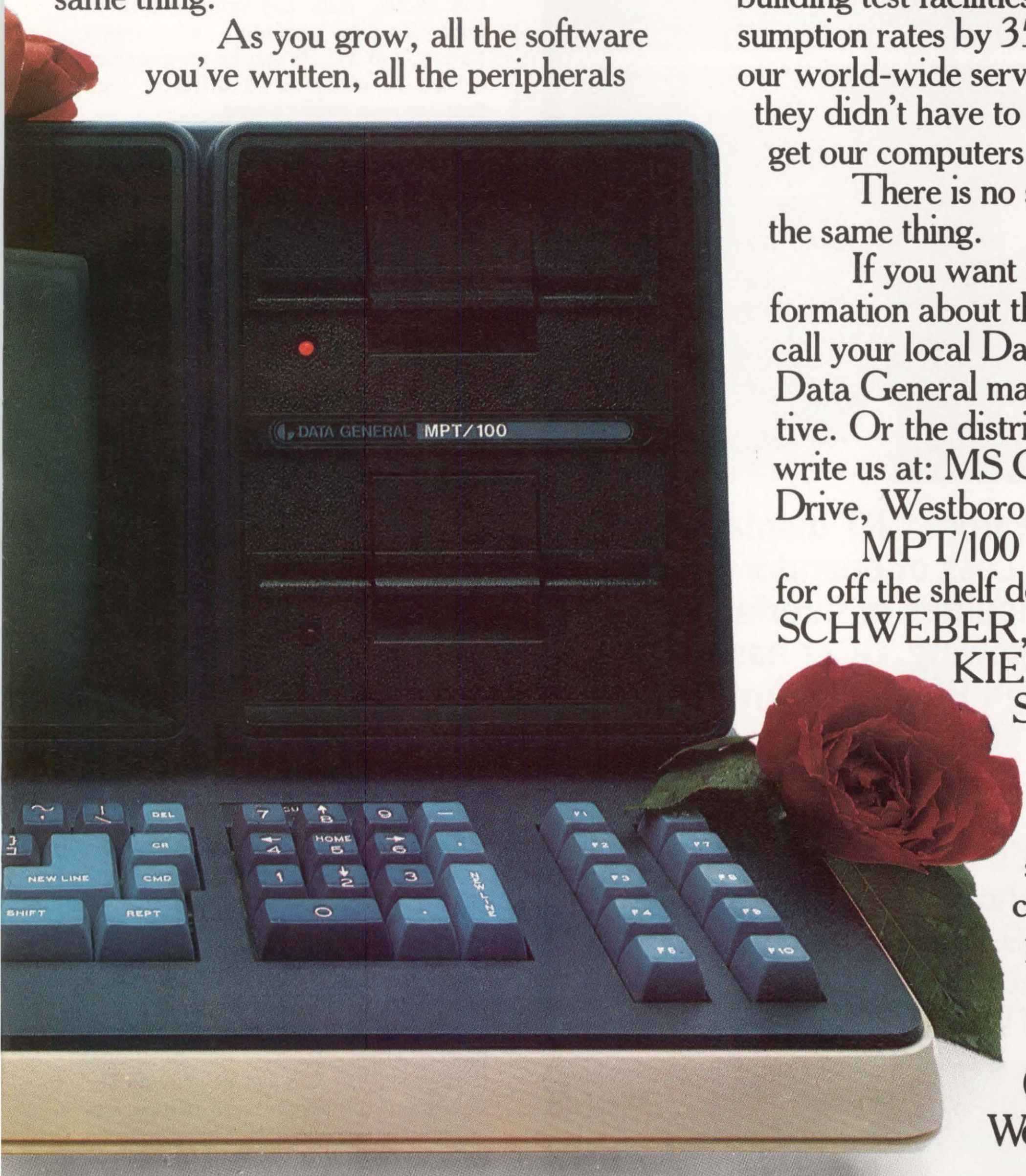
The point here is that the MPT/100 can make you what a lot of companies have become with Data General.

Like Aero Systems Engineering, of St. Paul, Minnesota, for example. They're far and above the leading manufacturer of computerized aircraft jet engine testing systems. A position they came to occupy partly by building test facilities that could cut fuel consumption rates by 35%. Partly because of our world-wide service. And partly because they didn't have to wait eighteen months to get our computers.

There is no stopping you from doing the same thing.

If you want to get more detailed information about the MPT/100 computer, call your local Data General office or your Data General manufacturer's representative. Or the distributors listed below. Or write us at: MS C-228, 4400 Computer Drive, Westboro, MA 01580.

MPT/100 computers are available for off the shelf delivery from:
SCHWEBER, HALL-MARK, KIERULFF, ALMAC/STROUM and R.A.E. in Canada.



Look at it this way. All of you who want to start your own computer company, are very lucky people. We didn't have anybody to write to when we got started.

Data General
We take care of our own.

TECH REVIEW

Digital in-circuit test system handles mixed families on board

The Troubleshooter 900, with up to 3024 universal test points, performs production testing of digital PCBs—such as the large boards used in computer systems. The unit, from Plantronics/Zehntel, Inc, 2625 Shadelands Dr, Walnut Creek, CA 94598, tests any combination of logic families, including ECL, CMOS, LS/TTL, and TTL. It can be programmed to test as many as 63 different logic families on a single board.

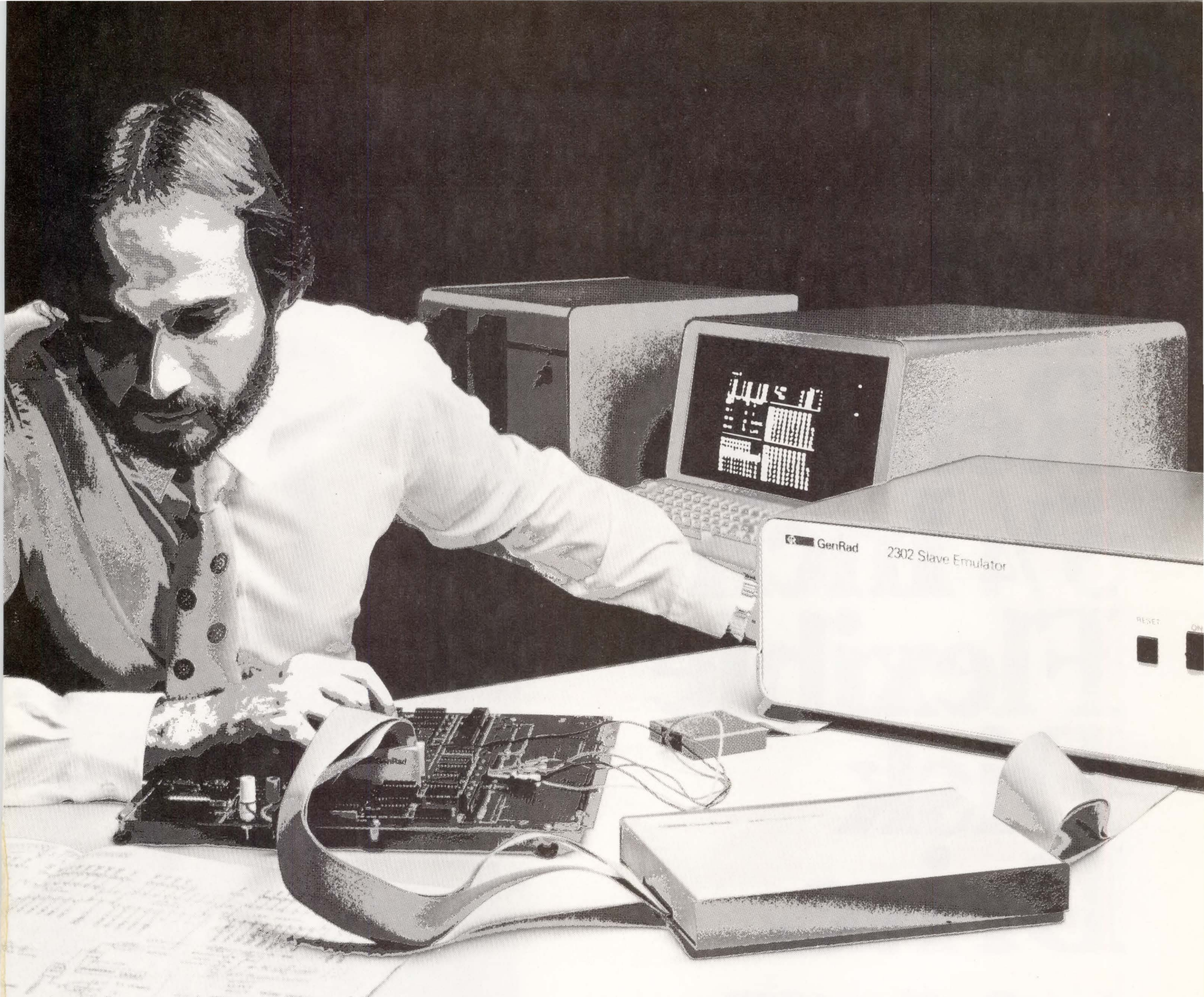
The system derives its ability to test mixed logic families from bipolar drive and distributed programmable power. Each driver/receiver card (48 hybrid nodes each, 63 cards maximum) is individually programmable for either positive or negative logic levels and power supply voltages. In addition to 38 drivers for stimulus, each card has 0- to 3-A, −6- to 12-V power supply for device under test power, all under program control.

In the system, each driver/receiver connection is treated as a transmission line. Short coaxial cables, with selectable terminations to reduce ringing, overshoot, and crosstalk, are used for each of the lines. Bandwidth enables high speed operation. Combination of high speed and less distortion makes possible testing of boards containing ECL.

Stimulating at a 1-MHz pattern rate and receiving signals at up to 4 MHz, the system can test microprocessors running at their own speed. Those that include clock circuitry in their architecture can be tested by synchronizing the tester to the freerunning clock of the processor. The unit can select any of three external clocks on the board for specific tests under program control. Analog and digital capabilities at every node permit shorts and continuities testing on every test point.

Software features include the company's Data Director for functional testing of VLSI and LSI devices on the board and the Producer to reduce programming time and cost. The system can be used with the optional model 110 remote programming station, which serves to generate and edit test programs and run the Failure Analysis Data program offline to free the test system for production testing.

Circle 364 on Inquiry Card



Our 16-Bit Support is Complete

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68000	•	•
Z8001/ 8002	•	•

Complete support also available for the 6809 and other 8-bit chips

If you're into microprocessor-based design with 16-bit chips, call us. We've got the hardware and software support you need. We've got it NOW! We can support you with full-speed, real-time, transparent emulation; simultaneous emulation of multiple processors; and full logic analysis capability. We're also shipping PASCAL Compilers for 8086, 68000 and the Z8000 series. Give us a call and we'll prove we've got the only way to emulate . . . the only way to write programs for 16-bit chips. Call today. We won't ask you to wait for 16-bit support.

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CIRCLE 41 ON INQUIRY CARD

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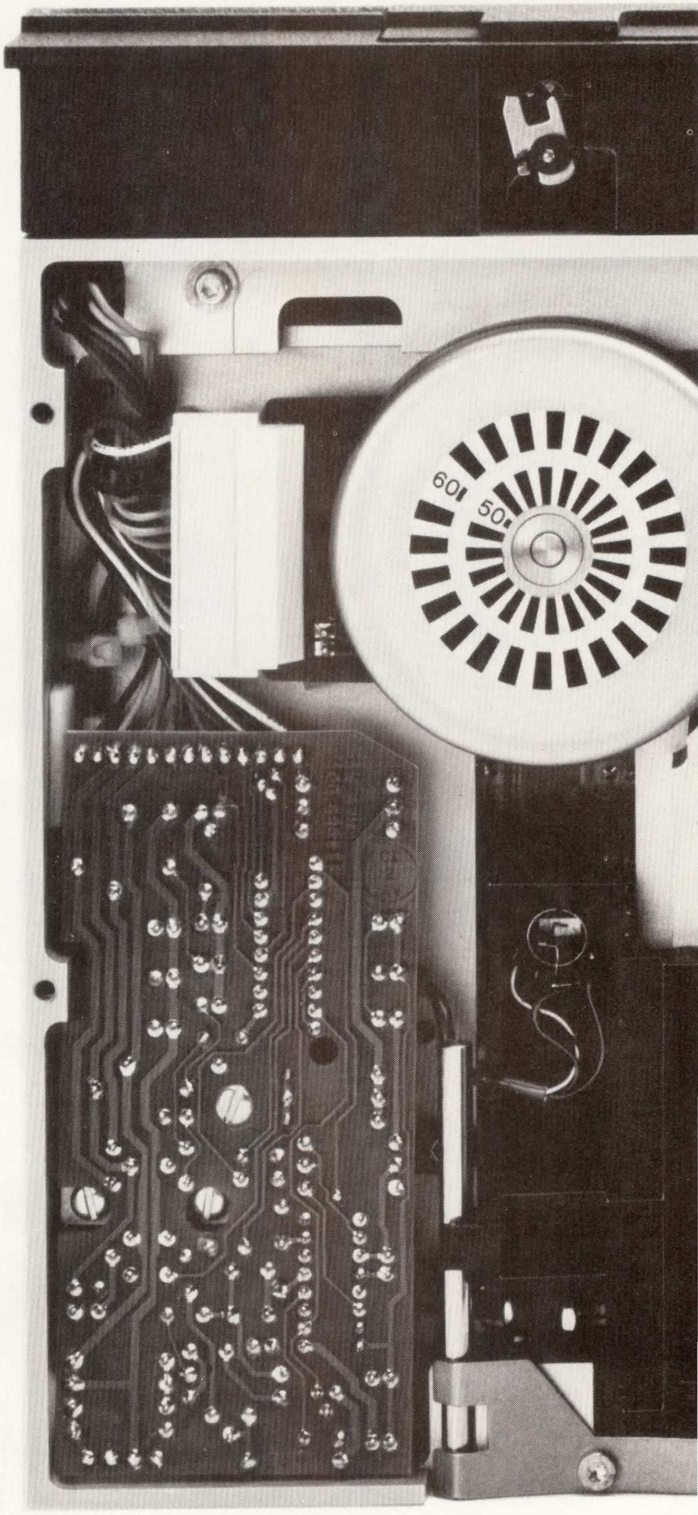
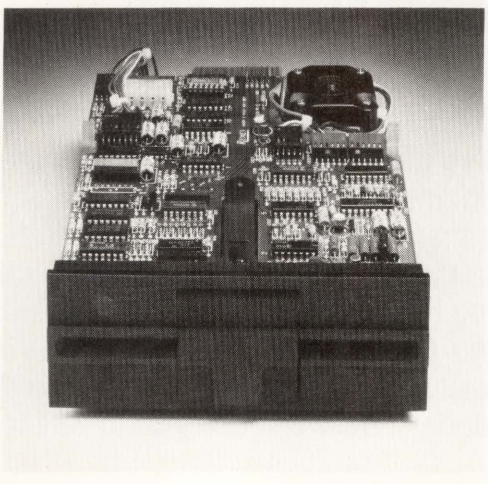
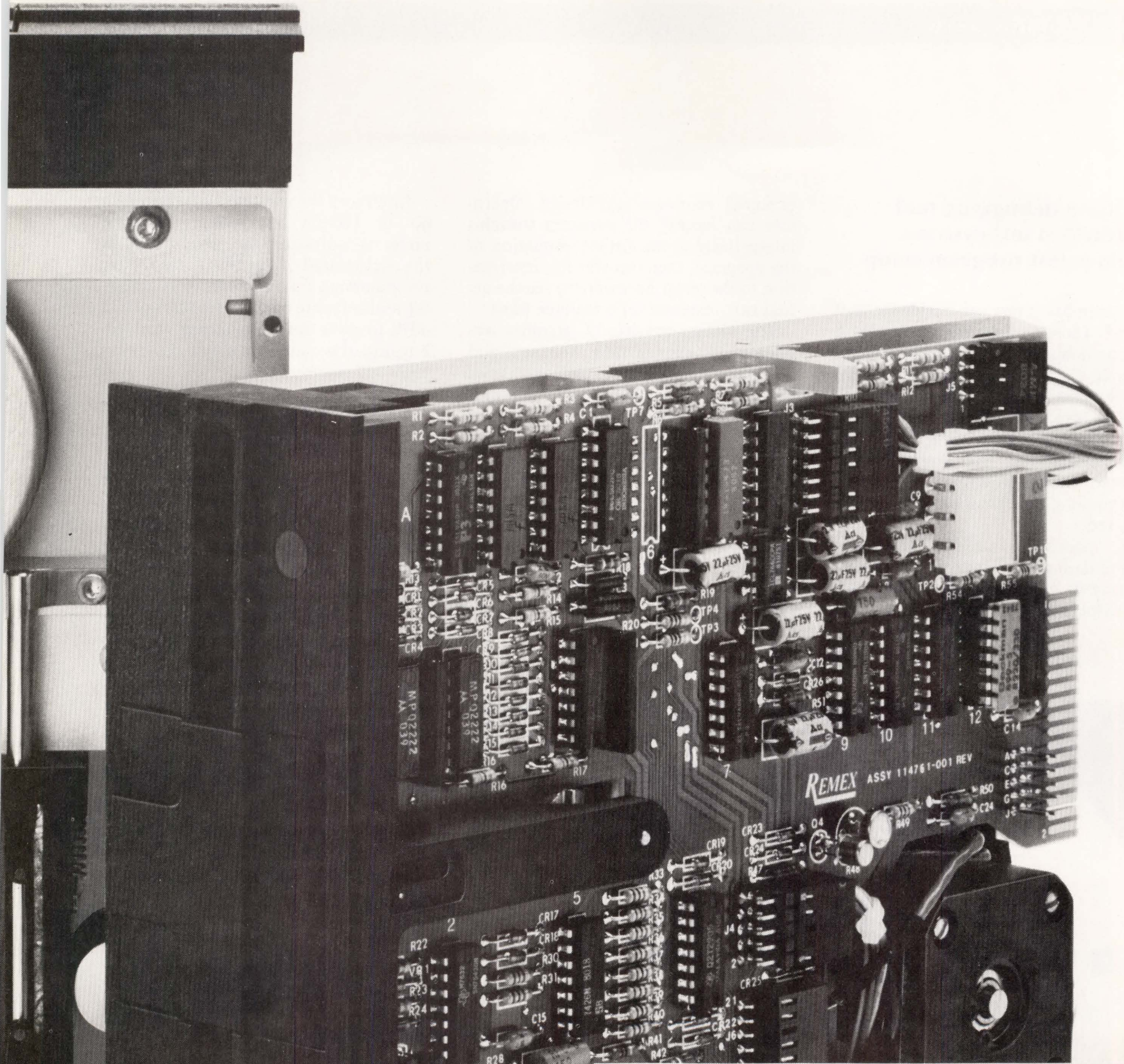
Low Profile, 96 TPI.
Direct Drive Performance.






REMEX ASSY 11476 1-001 REV

Realtime debugging tool for LSI/VLSI test systems displays test program setup

SAGE supplies users of Series 20 and Sentry[R] LSI/VLSI test systems with a realtime debugging tool. In the system, Fairchild Camera and Instrument Corp, Test Systems Group, 1725 Technology Dr, San Jose, CA 95110, has combined interactive software with a color graphics terminal to provide visual display of the test program setup so that programming errors can be detected and corrected.

The package simplifies debugging by simulating the system hardware's interaction with the device under test and displaying both the stimulus and expected response graphically. Operators can modify the program stimulus interactively in the virtual simulation of the program, then transfer this information to the tester hardware to see the actual DUT response on a realtime basis.

The system consists of graphics terminal with color display, lightpen, and keyboard. The software package allows the terminal to display the waveform of all programmed inputs, waveforms of actual device outputs, placement of measurement strokes, and results of pass/fail decisions. A virtual tester simulates in software what tester hardware does, displaying the waveform as it appeared on the device under test. Using the state library, the virtual to real translator then records all changes accomplished and lists them on a printer.

Interfaced through the RS-232 port of a 60- or 120-pin test system operating under M^3 software, the system runs in the background of the CPU. It can reduce programming time and use of engineering and software resources by as much as 40% to 50% for development and debugging of a complex LSI test program.

Circle 365 on Inquiry Card

Realtime 32-bit machine offers hardware support for multiprogramming

Supporting multiprogrammed operation through hardware, the model 4090 also provides 16k bytes of high speed cache memory and 4M bytes of main memory. GEC Computers Ltd, Elstree Way, Borehamwood, Hertfordshire WD6 1RX, England, has designed the CPU to execute 1.5M instructions/s and has provided the system with built-in diagnostics. Hardware segment registers support memory protection; other functions are supported through Nucleus, a hardware realtime executive.

As on other 4000 series systems, Nucleus supplies a number of functions that are normally performed by a software operating system. Among these functions are maintaining protection between programs, providing communication facilities between programs, short term scheduling of programs, providing fully protected I/O facilities, and routing interrupts to appropriate programs. A microprocessor based control unit enables the operator to control the CPU and monitor contents of memory and registers.

Performance improvements are demonstrated. The system runs programs 2.5 to 5 times faster than the model 4085; its extended facilities enable it to run typical FORTRAN benchmarks 10 times faster than the model 4065.

Babbage, CORAL 66, FORTRAN 77, Algol 60, Pascal, COBOL, APL, RPG II, and BASIC languages are supported. The FORTRAN compiler includes a feature called FOCUS which serves as an interactive source level debugging tool. □

Circle 366 on Inquiry Card

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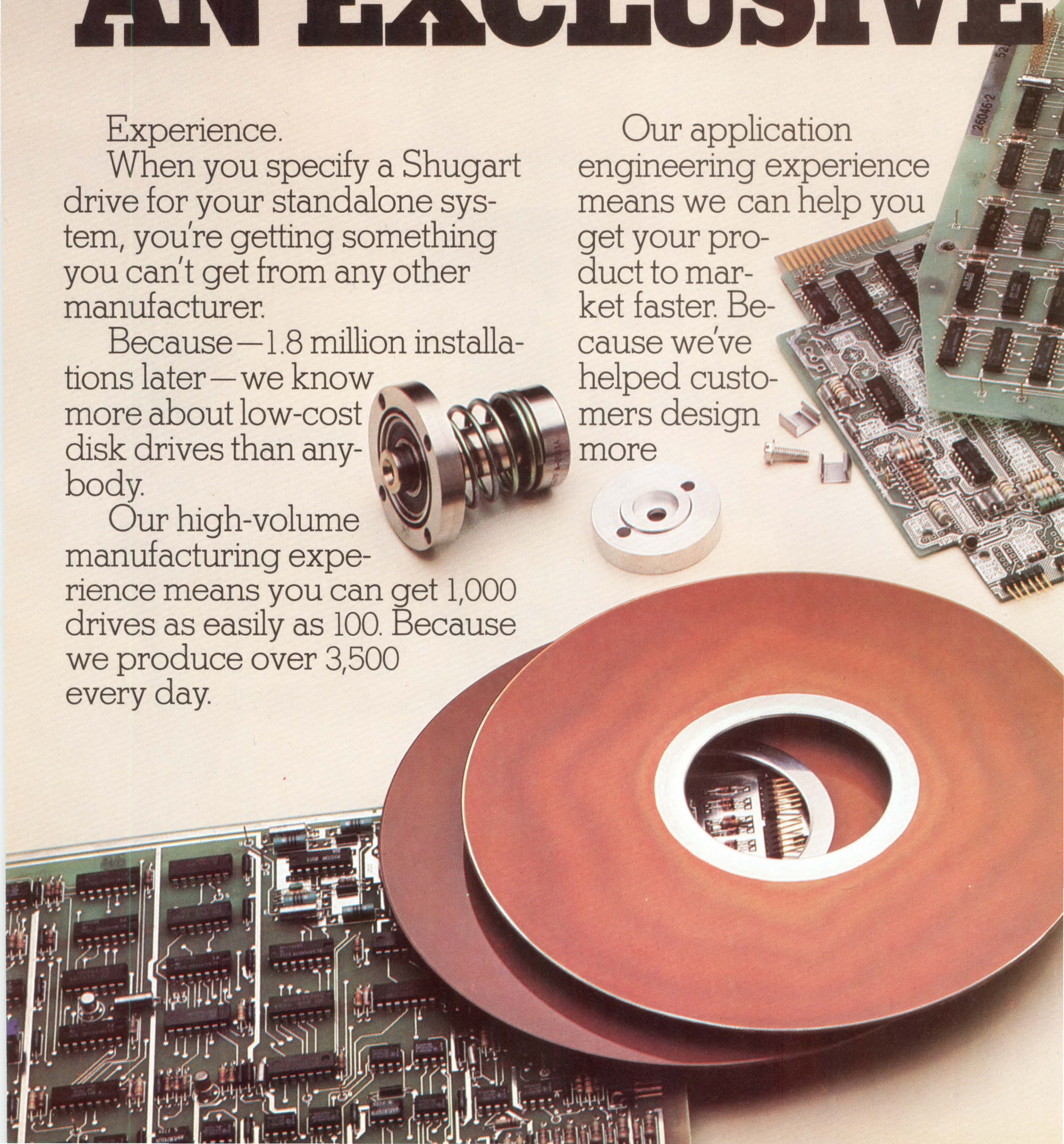
Experience.

When you specify a Shugart drive for your standalone system, you're getting something you can't get from any other manufacturer.

Because—1.8 million installations later—we know more about low-cost disk drives than anybody.

Our high-volume manufacturing experience means you can get 1,000 drives as easily as 100. Because we produce over 3,500 every day.

Our application engineering experience means we can help you get your product to market faster. Because we've helped customers design more



INTRODUCES INGREDIENT.

controllers than anyone else.

Our world-wide field engineering experience means longer running drives and faster repairs. Because we've got the largest field service force dedicated to our industry.

And our new product development experience means the biggest choice in low-cost disk drives.

From the industry-standard SA800 floppy—the recognized leader for low cost and high reliability.

To the SA850 double-sided floppy with up to 1.6 megabytes of storage. All reliable thanks to its Bi-Compliant™ head design.

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Monitoring and Control of a Research Lumber Kiln with a Personal Computer

Ronald G. Fluet*

General Dynamics Corporation
Eastern Point Rd, Groton, CT 06340

John L. Pokoski
John L. Hill

University of New Hampshire
Durham, NH 03824

Freshly cut timber retains most of its internal moisture content and usually cannot be processed until much of this moisture has dissipated. During the drying process, the lumber undergoes scheduled atmospheric variations in an environmentally controlled building called a dry kiln. Such kilns generally contain large circulation fans, a heat source (eg, steam in a finned pipe), a humidity source (eg, steam), and ventilation to exhaust humidity to the outside. Lumber is stacked in the kiln to provide air circulation over the wide boards.

As energy, labor, and raw material costs continue to rise, efficient lumber drying becomes extremely important. For instance, 150 m^3 of high grade lumber, contained in a single kiln charge, can be worth over $50,000 after drying. Improved drying schemes minimize lumber loss (degradation) and shorten processing schedules to bring about significant dollar savings. A microcomputer based kiln controller with a control program written in BASIC is now being developed as a research unit at the University of New Hampshire. By accurately sensing and controlling wood-drying kiln environments, the instrument regulates an efficient and cost-effective wood processing system.

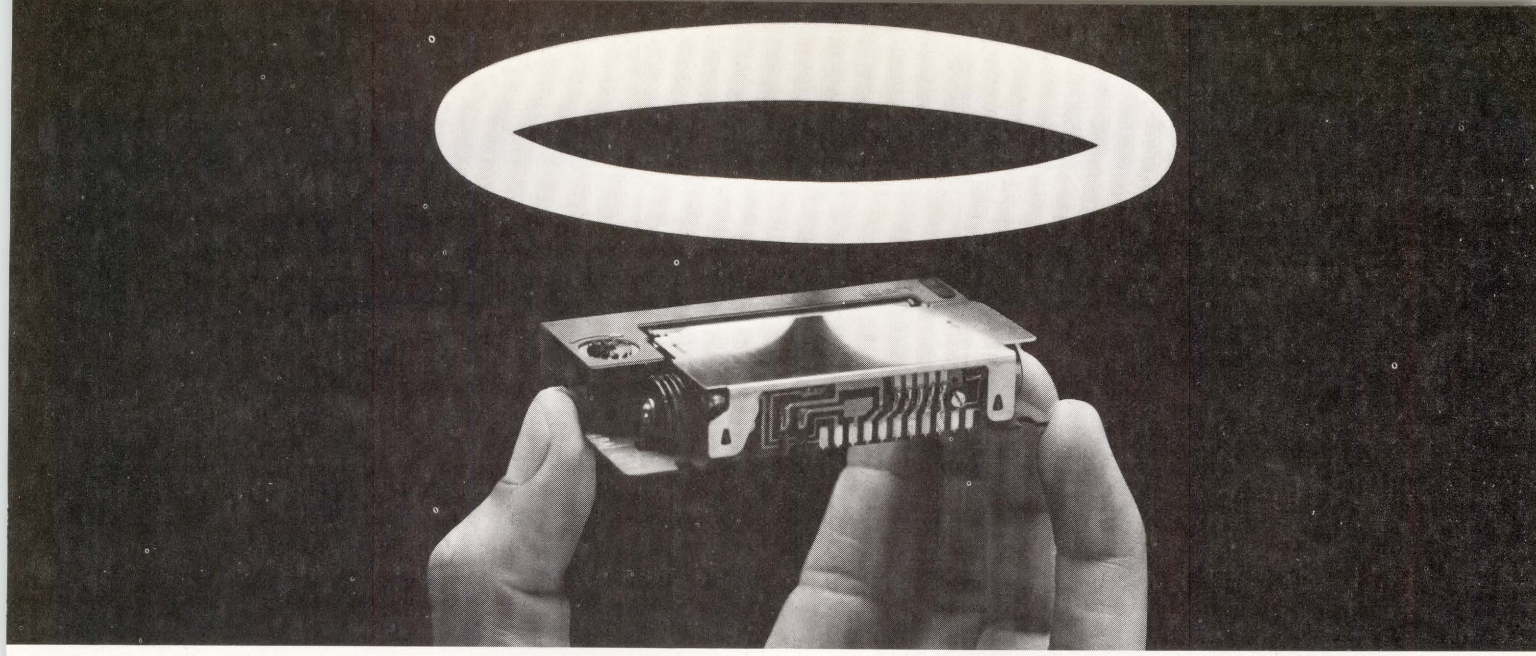
Most controllers fit an open-loop, manual setpoint description. Some use a slowly rotating cam, while others require manual input at specific time intervals determined by changing wood moisture. A wet and dry bulb scheme is the standard means of sensing kiln conditions. Bulb sensors drive pneumatic valves that are calibrated mechanically to actuate heat, steam, and ventilation in the kiln. The bulbs also drive two pens that record the conditions on a rotating circular chart. Other controllers vary from this scheme somewhat, but their degree of sophistication is similar.

System performance and product quality governed by such controllers are not as efficient as today's theory and technology can provide through automatic control. For example, continuous monitoring and storage of changing kiln and wood conditions, and corresponding automatic adjustment of the control outputs, should result in tighter control over dried lumber quality, as well as time and energy savings. Kiln capacity in lumber volume per unit time should increase through use of an improved adaptive reference input scheme and elimination of sample board moisture-measurement delays. An automatic controller shortens drying time and avoids overdrying (continuing a run after the wood has reached the desired target moisture content).

Previous reports on automatic kiln control[1,2] describe the system performance of a weight actuated controller; a German kiln manufacturer has published information about its automatic controller.[3] However, neither of these systems uses a computer controller such as that in the small [500 to 800 board feet (152 to 244 m)] research unit kiln in the Wood Products Laboratory at the University of New Hampshire. Automatic kiln control research there involves: (1) improved sensors for both shrinkage and moisture gradients; (2) a procedure for producing a drying schedule according to a predetermined performance index, which may be a function of time, energy, drying stress, and related failure—a key element in the generation of this schedule is a mathematical drying model for the wood; and (3) the

(continued on page 82)

*Ronald G. Fluet is a former Graduate Research Assistant at the University of New Hampshire. Scientific contribution number for this study is 1073, from the New Hampshire Agricultural Experiment Station.



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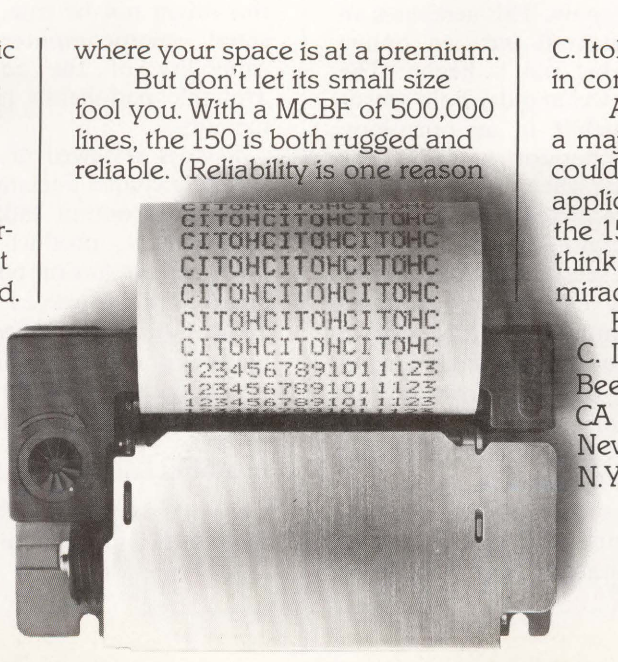

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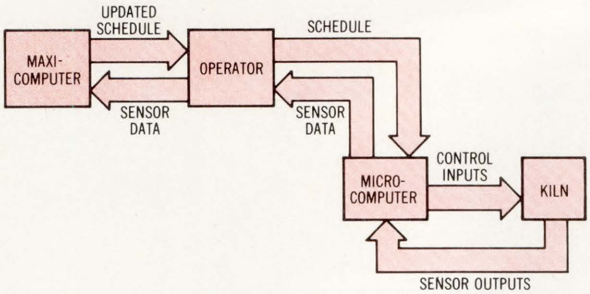

Fig 1 Simplified block diagram of complete kiln control system. Kiln operator periodically closes loop to generate new schedule based on up to date sensor information

development of a computer based system for sensing and controlling the wood drying process as described here.

General Considerations

An online computer controlled system must sense the critical parameters continuously and adjust the drying schedule according to a control algorithm based on the performance index. In this case, the control algorithm is lengthy and complex, requiring the use of a large, expensive computer. Since the time constants of the plant (kiln and lumber) are extremely slow, and typical kiln schedules also change slowly, a more economical solution is suggested in Fig 1. Initially, the operator makes a test run of the schedule program in an offline maxicomputer, using typical wet lumber values as sensor inputs. This generates an optimal schedule that is entered into an online microcomputer and the drying run is begun. The microcomputer monitors the wet and dry bulb sensor outputs and tracks the schedule in an open-loop fashion. Periodically, the operator monitors the wood moisture sensor outputs; when they deviate too far from values originally predicted by the optimal schedule program, the operator generates a new schedule based on the actual sensor values. Then the operator closes the loop by entering the updated schedule into the microcomputer. In this way, a relatively small amount of time in a timeshared maxicomputer is used, and money is saved. However, this system requires more operator attention than would a completely automated one. In a research environment, operator monitoring is no handicap, since sensor data and schedule outputs are analyzed as a matter of course. Even in a commercial kiln, it may be desirable to keep the operator actively involved in the process. However, the links between the micro- and maxicomputers can be automated easily. A longer range goal is to simplify the schedule generating program and eliminate the maxicomputer entirely.

Selection of the Computer

Use of a computer as the heart of a kiln controller has many potential commercial advantages, including low cost, flexibility, and reliability. These factors—particularly flexibility—are even more important for a research controller. Variables and constants in the program can be changed easily, and the system program edited to modify the actual characteristics of the control system. Research kiln operation also requires collection and storage of large amounts of data for future analysis. This is facilitated by standard computer interfaces to printers, magnetic tapes, and magnetic discs.

A personal microcomputer system was chosen for the kiln tracking controller at the University mainly because of its low cost. A minicomputer would have performed the required functions faster and could have been expanded with greater flexibility than a microcomputer. However, operating speed was not critical, expansion requirements were moderate, and the cost differential between computer types was impressive. Processing power, memory capacity, and expansion capability of the microcomputer systems were more than adequate for implementation of a kiln controller.

Choice of a personal microcomputer system over a single printed circuit board microcomputer was influenced by the determination that the hardware cost and development from board level would exceed the cost of an equivalent personal microcomputer system significantly. On the other hand, if the controller were being developed for commercial production, this might not be true. As a research tool, the personal microcomputer enhances the expansion capability of the controller through its many available peripherals and the potential for add-on memory.

Factors reviewed in choosing the microcomputer system included documentation support, special purpose input/output capability, reliability in the kiln environment, product stability, maintenance support, and expansion potential. Market conditions in June 1978 influenced the specific microcomputer choice. Although several personal microcomputers met minimum requirements, the Radio Shack TRS-80 was chosen—primarily because of convenient local service and readily available documentation.[4,5]

Systems Engineering Considerations

Certain system input factors must be considered in the synthesis of a computer controller. Estimates

(continued on page 86)

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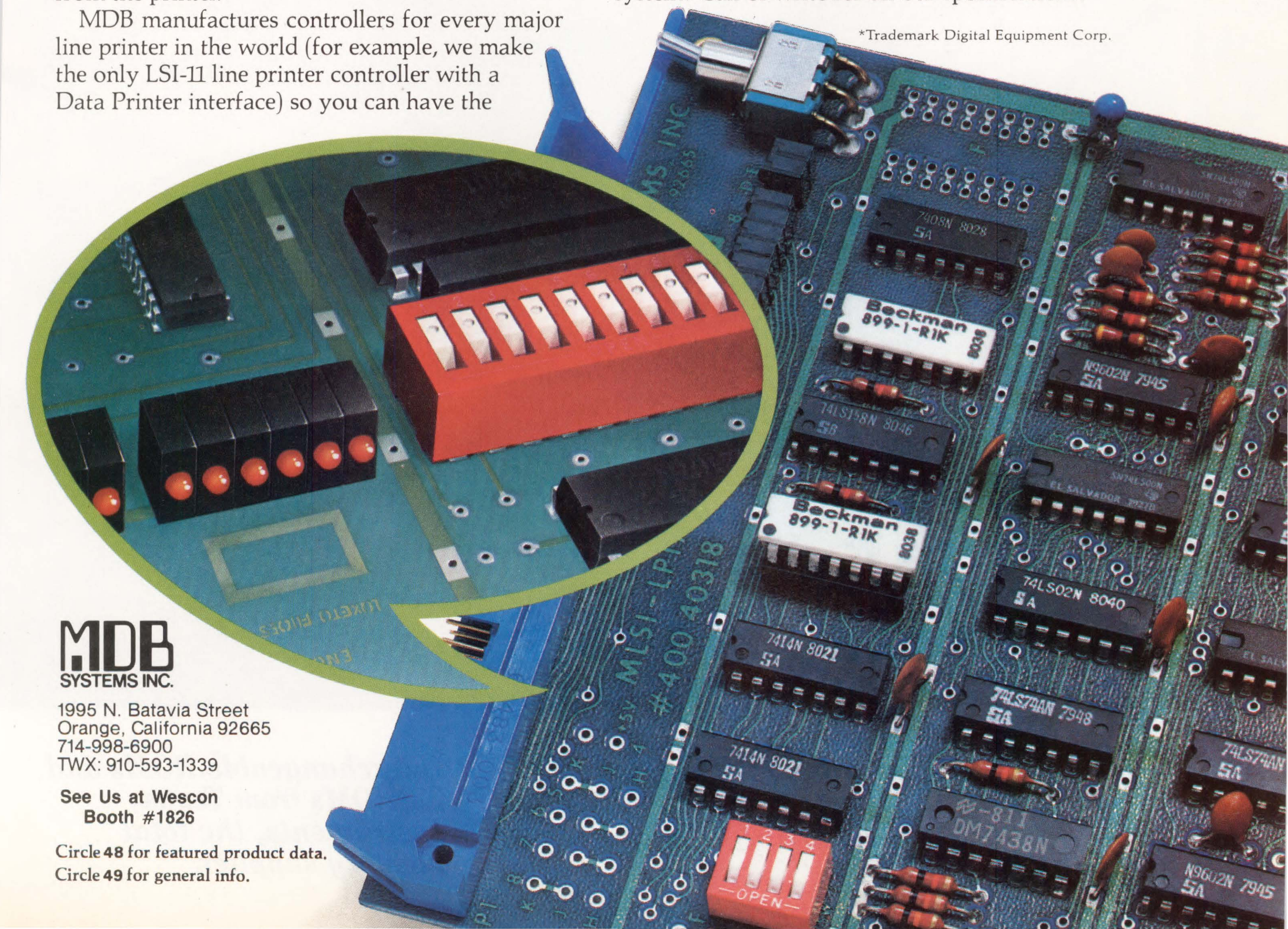

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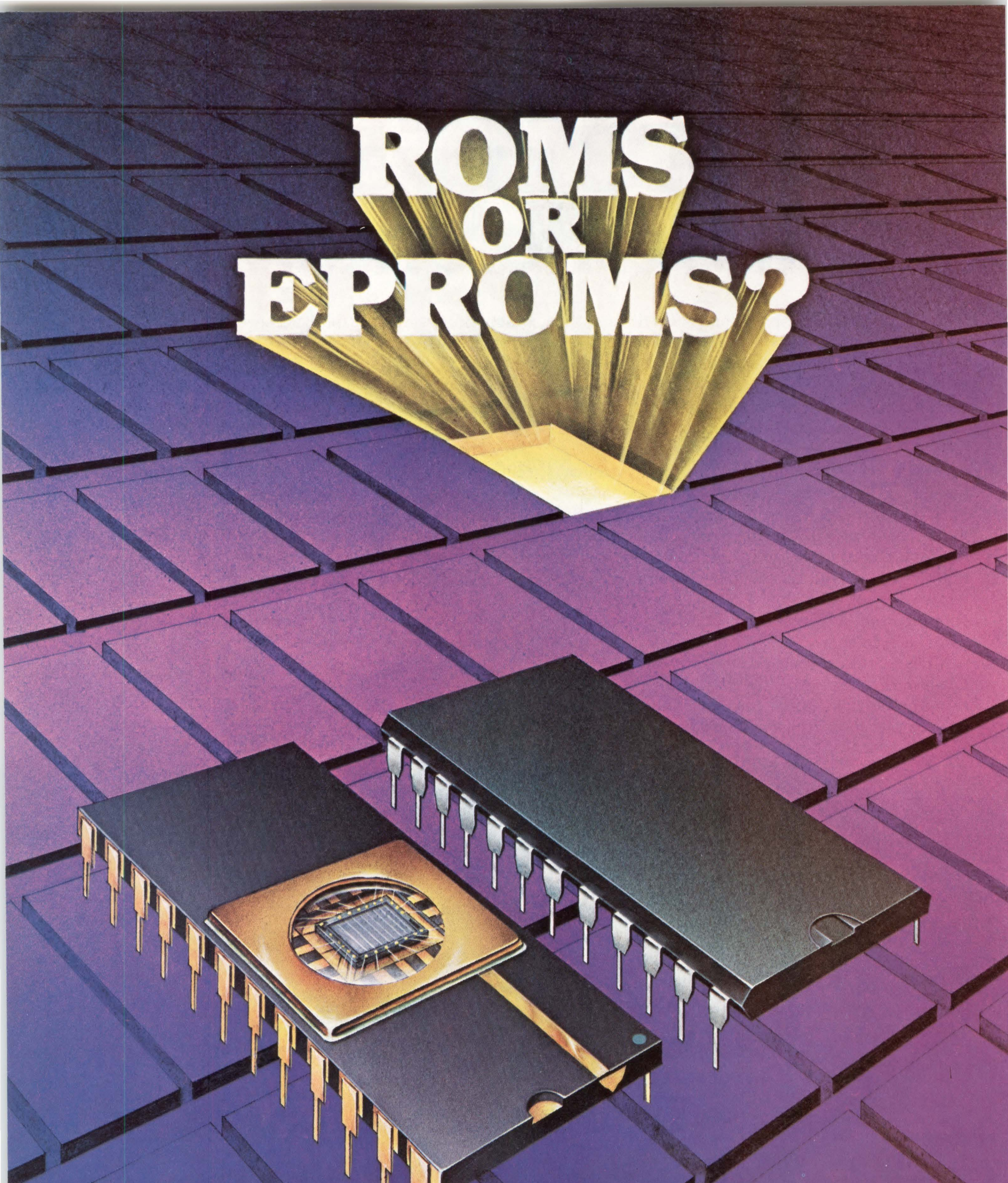

Interchangeable ROMs and EPROMs from Texas Instruments, the total memory supplier.

Here are tips from Texas Instruments on which to use when. Your decision may hinge on economics.

There are times when your system design will clearly dictate either ROMs or EPROMs. At other times, the dividing line between the two is hazy. That's when a careful analysis of the economics involved — particularly the recent substantial pricing changes in the marketplace — may tip you to one or the other with considerable long-term savings as a result.

Texas Instruments, a leader in non-volatile memories and a broad-based supplier, can deliver the byte-wide ROMs or EPROMs you need. And from its years of experience with these memory devices, TI offers suggestions that may help you decide on the least expensive solution for your system.

The case for ROMs

In general, ROMs provide more memory for less cost than any other semiconductor memory. The key to their use is high volume and high memory capacity — on the order of 32K and 64K. Coupled with programming — performed by the supplier — that will not change or need to be updated.

In these circumstances, ROMs are especially cost effective. Total costs are spread so widely that per-bit cost is relatively inexpensive.

Consumer and computer peripheral applications where the volume of end products is large can make very economical use of ROMs.

The case for EPROMs

Prices for 16K and 32K EPROMs have declined significantly, and those for 64K devices will follow suit. Making EPROMs economically attractive, especially for applications where the program is likely to change.

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Device	Density	Power Dissipation*	Access Time*
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TMS2564-45	64K	840mW	450ns
TMS2564-50	64K	840mW	500ns
TMS2532-25	32K	840mW	250ns
TMS2532-35	32K	840mW	350ns
TMS2532-45	32K	840mW	450ns
TMS25L32-45	32K	500mW	450ns
TMS2516-35	16K	525mW	350ns
TMS2516-45	16K	525mW	450ns
TMS2508-25	8K	446mW	250ns
TMS2508-30	8K	446mW	300ns

*Worst case over operating temperature range

If you are in a hurry to get to market, EPROMs can be your best bet. They are available from multiple sources on short lead times.

One additional advantage: Because of their programming flexibility, EPROMs are an excellent prototyping tool prior to conversion to ROMs. And, at the end of a product's life when both volume and the number of ROMs being used decline, converting back to EPROMs can cut costs.

The case for Texas Instruments

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In EPROMs, you have the broadest choice in the industry — 8K through 64K. All have the same basic pin configuration to ease memory capacity expansion.

Weigh the pros and cons of ROMs vs. EPROMs. Evaluate your system requirements and carefully check out the economics. Then call your nearest TI field sales office for prices and delivery on your choice. Of course, if you still have doubts about which is best for you, we are ready to consult with you at any time.

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must be made for the number of input channels adequate to maintain control and to perform other desired functions. A substantial number of channels should be available if future use in a research and development application is desired. In the application discussed here, 42 independent input channels are used. Six channels are designated for dry bulb temperature sensors, 6 for wet bulb temperature sensors, 12 to 24 for core moisture content sensors, and at least 6 for future use. Multiplexing data through a single channel would make more channels available for future expansion.

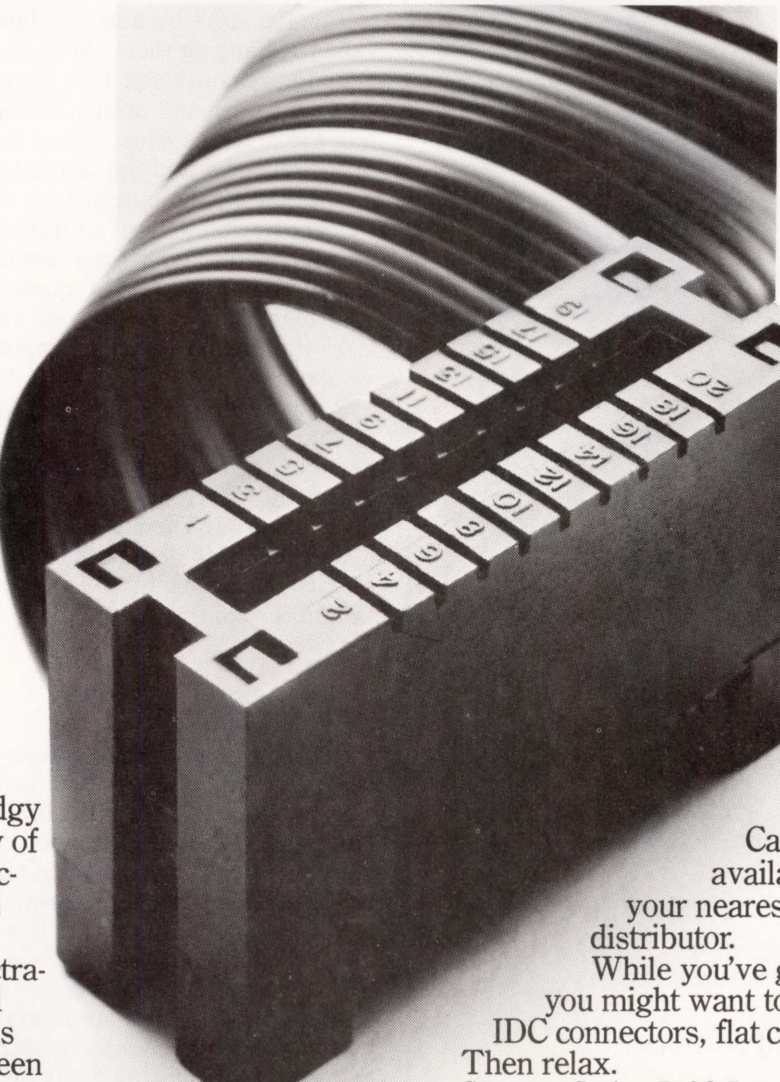
In most data control systems, the type of sampling used is critical for obtaining an accurate representation of the sensed parameters. Sampling of independent channels may be sequential or in parallel, and the time intervals between samples may be synchronous or asynchronous. In terms of hardware implementation, sequential sampling is much less expensive than sampling all the inputs in parallel. Time between samples is crucial in representing the original signal without harmful distortion. Sampling requirements are dictated by the characteristics of the parameters under investigation and the overall system response. Lumber drying is accomplished by regulating the kiln temperature and relative humidity. Temperature and humidity in a kiln respond slowly to step changes in heat and steam—estimated time constants of these responses are in the order of seconds. Using a computer, the time between samples would be several orders of magnitude faster than the time constants of the temperature and humidity responses. Thus, sequential sampling may be used without serious distortion of the actual values.

System output characteristics must also be considered in the initial design stages of the controller. For example, the number of outputs necessary to control the kiln adequately must be estimated. In this case, the computer control outputs had to link to the actuator system without disabling the existing control system. Three control outputs are used in conventional lumber kiln drying equipment. Specifically, these outputs control the kiln's heat, steam, and ventilation.

At the University of New Hampshire, the experimental dry kiln has a pneumatic system, commonly used in commercial installations, that is actuated by three float valves controlling heat, steam spray, and intake/exhaust vents. It was possible to link the computer outputs to the pneumatic system through an electromechanical device that drives the float valves. For greater flexibility in this research, the electropneumatic linkage had to operate easily with either the present control system or the online computer controller. This was accomplished through a solenoid linkage to the float valve of the present control system.

(continued on page 88)

Advantedge



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Output is a major factor in controller design; for example, output can be on/off or proportional. To decide on which type of output to choose, the designer must consider the dynamics of the kiln, feasibility of the present system actuators, and flexibility for future experimentation in control. Proportional output would have caused problems in linkage to the actuators because the float valves are on/off valves. Changing these valves to proportional valves would have conflicted with the operation of the present controller and destroyed the objective to maintain the present system. Since the float valve was an on/off element and the computer also operated with on/off logic, this output type was selected. An extremely flexible on/off output scheme adequate for precise control with these actuators is pulse width modulation (PWM). For control purposes, this is equivalent to a step input of variable duration and gives the on/off valves a proportional effect on the system.

With the controller in operation before the present research unit, several instances occurred when alerting the operator to critical conditions would have meant the difference between success and failure in the drying run. Therefore, a warning system has been included in this design. Basically, the alarm will be set off for power loss, operator negligence, sensor failure, or control error.

Hardware Overview

The hardware interface between computer and kiln can be considered as the heart of the controller, whereas the computer is the brain. The interface contains several distinct networks: analog to digital converters (ADCs), signal conditioning, PWM, actuator linkage, and a warning system. The entire controller interface is housed in a 12 x 10 x 8" (30 x 25 x 20-cm) metal box, and includes the two power supplies, two wirewrapped circuit boards, a 6-V battery and charger, three solid state relays, and a buzzer. The box has four switches for power and alarm control, and four light emitting diode (LED) status indicators.

The main objective of the hardware network design is to allow the microcomputer to interact with the kiln, not to experiment with sensing networks. Therefore, the computer must issue commands to the kiln and then interpret information from the kiln in order to make decisions for controlling the wood-drying process. Communication between the computer and the outside world is through ports.[4] Using external hardware, these ports must decode eight computer address lines and the IN or OUT signals. The computer has control of the ports through software by simply using the INP (port address) or OUT (port address, data) BASIC commands.[5]

(continued on page 92)

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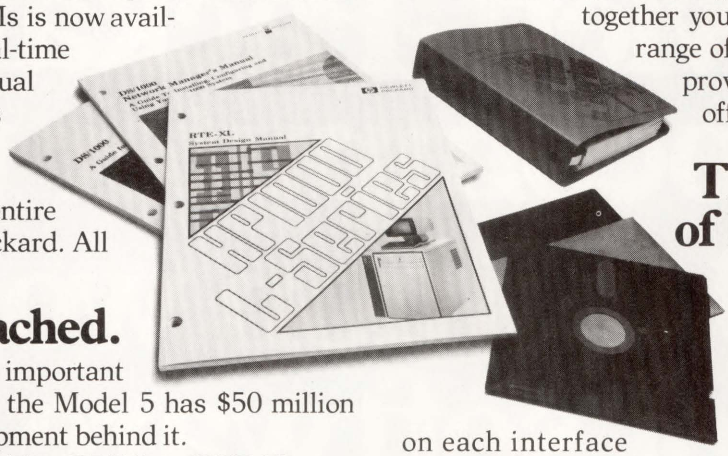

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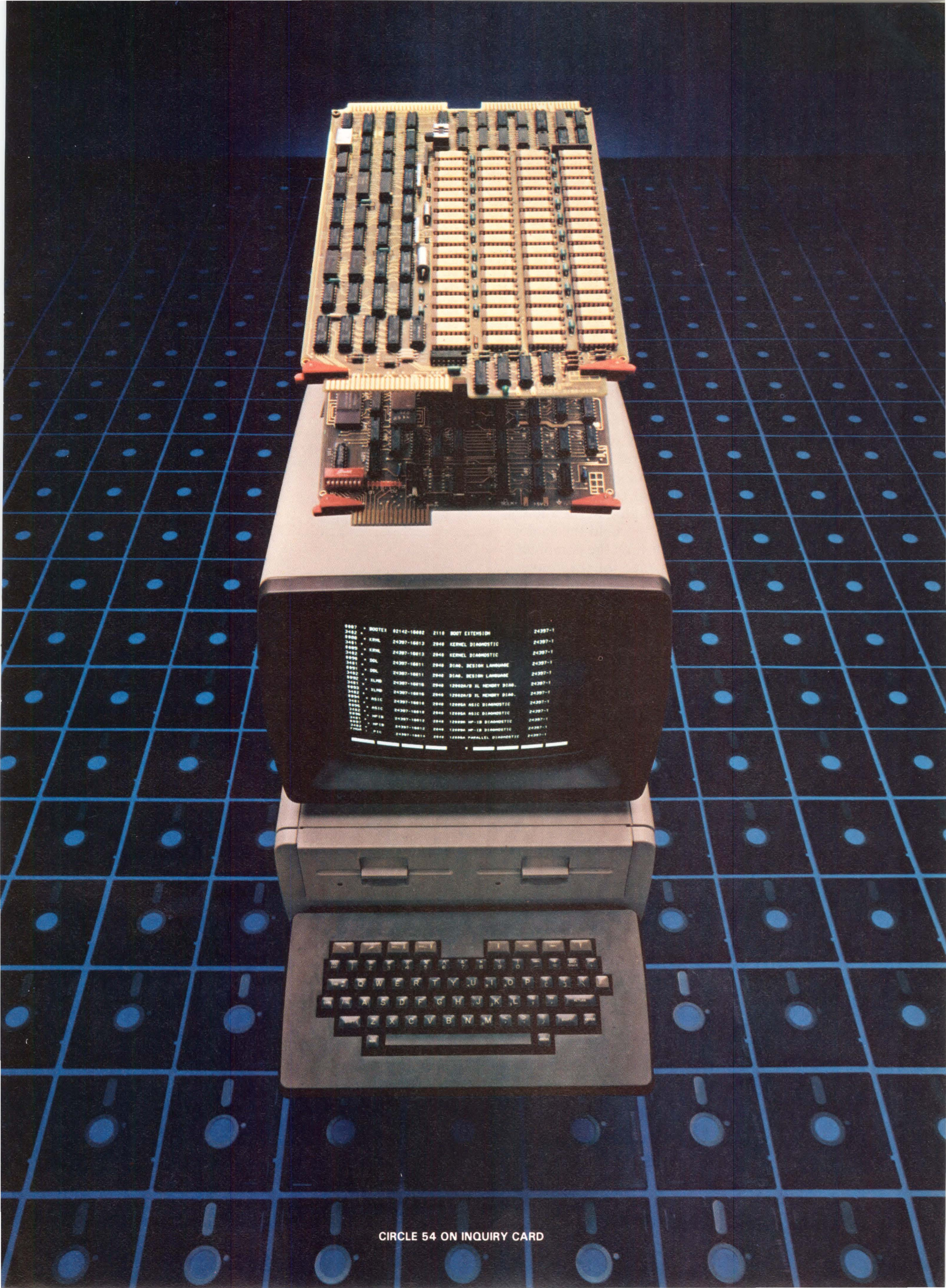

The input hardware interface conditions analog signals from sensors and converts them to digital information that is read into the computer and processed as meaningful data. Presently the inputs are set up to sense wet and dry bulb temperature and core moisture content. The design requirement of 42 input channels significantly influenced the type of ADC used in the design. Resolution required in the conversion, speed of conversion, and cost also influenced ADC selection. The Fairchild 9708 is a low cost, 6-channel, 8-bit processor controlled ADC and was found to be suitable for this application, along with seven 9708 chips, to meet the 42-input channel requirement. The 9708 ADC and the specific channel on that chip to be converted is selected by the computer through port decoding. Conversion from analog to digital is accomplished by timing the controlled discharge rate of the stored analog input voltage. Counting during the discharge of the analog input is performed by an external counter, and its 8-bit output is the digital representation of the analog signal. The command to sample and hold the analog voltage and start the count is given by the computer. The computer then checks the status of the conversion, and, when completed, it reads in the digital word. (See Fig 2.)

Sensor instrumentation was included in this project for demonstration only. Instrumentation hardware was placed on a board separate from the interface hardware to allow for future changes in the number and types of sensors. Temperature was sensed by a thermocouple, cold junction compensation device and an instrumentation amplifier.[6] Moisture content of the wood core was also sensed electronically. Impedance between pairs of special metal pins embedded in a board is related to wood moisture content; the higher the moisture content, the lower the impedance between the probes.

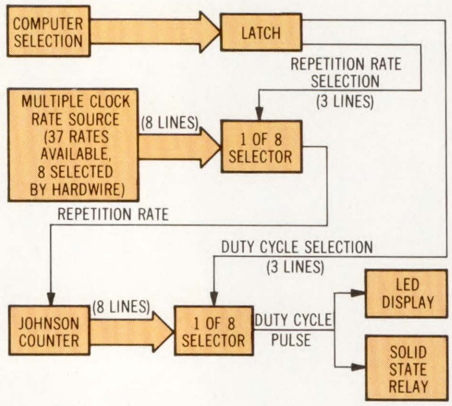

Fig 3 Pulse width modulation network. Output is sent to appropriate solid state relay for control, and to LED for diagnostic purposes

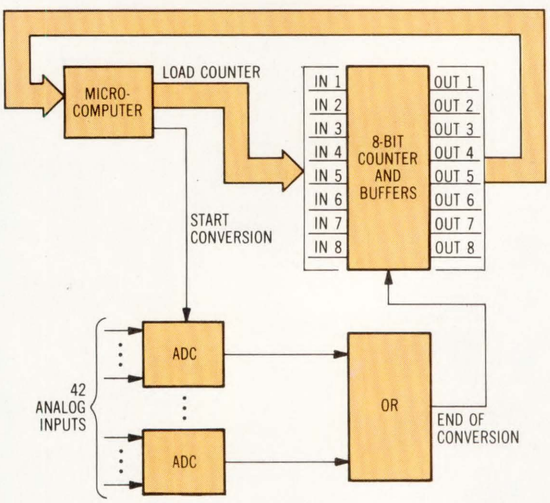

Fig 2 Block diagram of ADC network. Computer selects 1 of 42 inputs and starts count. 9708 completes its conversion, count is stopped, and computer reads counter's output into memory

Much of the sensor circuitry involves low voltage levels and associated distortion due to electrical noise and ground loops, for instance. In particular, radio frequency (rf) interference problems occurred between the microcomputer and the sensor circuits. Most of these problems have been eliminated by improved termination and shielding, but effort will be required to cut down the interference further.[7]

Output hardware allows the computer to issue commands to the kiln actuator system through a solenoid linkage to the actuators of the present control system and a PWM network interfaced to the computer. Functionally independent of the computer, the PWM network will accept computer commands to direct its operation at any time. Thus, if the computer fails, the controller outputs will continue to function at their last setting so that the operator can reconfigure the computer without losing substantial time from the drying run. This is the principal reason for implementing PWM in hardware rather than in software. Other supportive reasons for hardware PWM are inexpensive design and the need for three independent PWM outputs, which would be tedious in software. Easy software modification is not an advantage because PWM is a standard function.

The PWM circuit is centered around the Johnson Counter (4022) chip. (See Fig 3.) This system has three

(continued on page 95)

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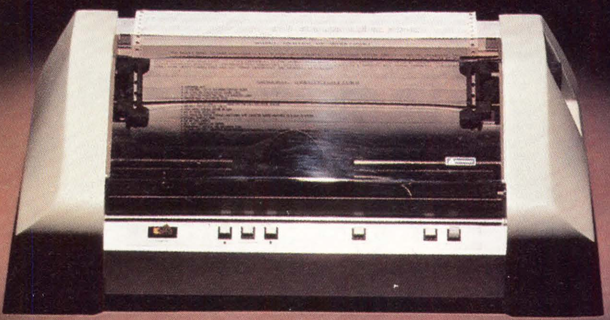

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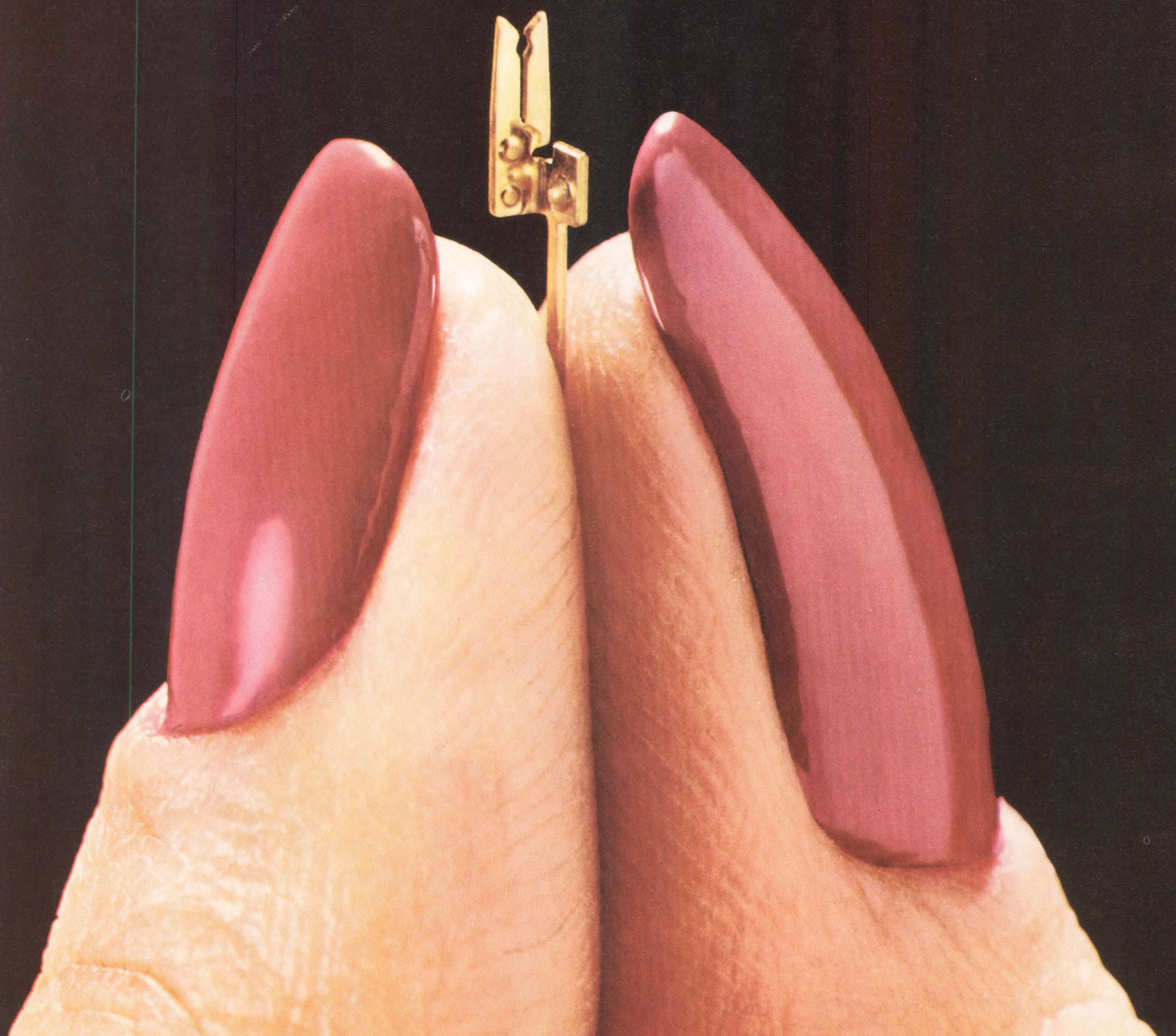

CIRCLE 56 ON INQUIRY CARD

identical PWM networks that operate independently of each other to provide separate control of heat, steam, and ventilation in the kiln. Fig 4 shows signals available to drive the outputs. Synchronization is the only physical interdependence these outputs require.

Linkage between the kiln's pneumatic actuator system and the electrical computer interface is accomplished through three electromechanical solenoids mounted in the kiln's present control box next to the three float valves. Metal strips extending from the solenoid plungers to the valve needle can be slipped out of position easily to allow the present pneumatic controller mechanism to operate. Solid state relays (SSRs) are used to allow 5-V logic to control the 120-V ac signal that drives the solenoids. These SSRs have optical isolation between the input and output to prevent any noise generated by the solenoids from reentering the system.

Although not very extensive, the warning system hardware, combined with software, monitors the four determined causes for alarm. The audible alarm is a hi-lo siren, 90-dB buzzer mounted on the side of the interface box. The buzzer can be disabled by a switch; an alarm LED is connected to the same signal as the buzzer. Once the audible alarm has been recognized, the operator can disable the buzzer while correcting the problem, and still monitor the alarm conditions with the LED.

Two alarm conditions are detected through hardware: power loss and operator negligence. A battery powered circuit monitors the 5-V power supply and drives the buzzer for the power loss condition; this monitor charges continuously during power-up. Operator negligence is defined as taking longer than five minutes to continue execution after striking the BREAK key on the microcomputer keyboard to stop the controller program. The BREAK key is decoded and triggers a programmable timer that counts five minutes before setting off the alarm. Software in the controller program resets the timer.

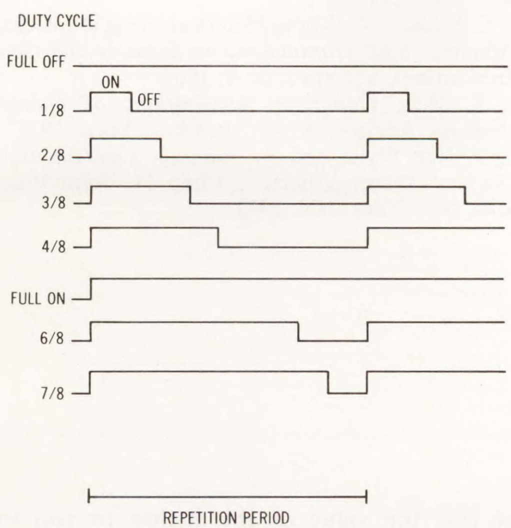

Fig 4 PWM signals drive heat, steam, and vent valves. Repetition rate varies from 33.5 s to 71.6 min, depending on hardwired configuration

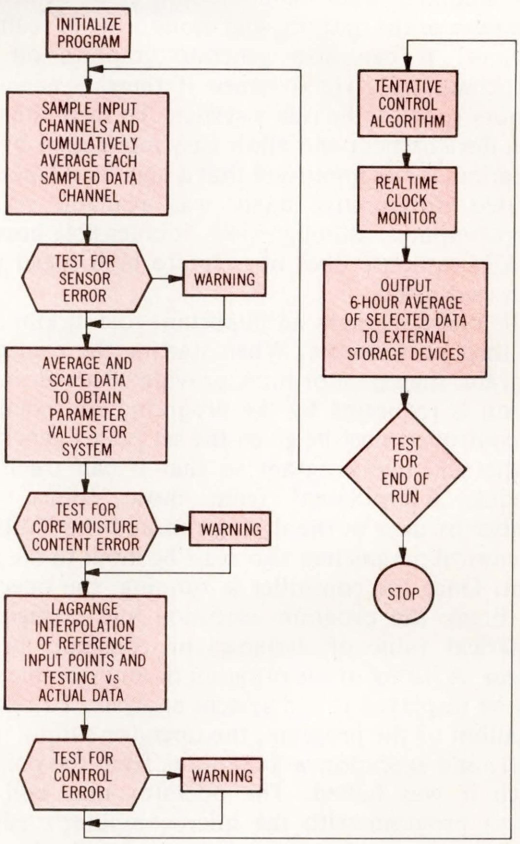

Fig 5 General flowchart of system program. Basic functions—sampling, data manipulation, error detection, PWM output rates, and realtime monitoring—are directed by software

Software Overview

Software is the key to flexibility in a computer control system, and, properly combined with hardware, it can result in an instrument well suited for research. The general overview of the controller computer program in Fig 5 illustrates the basic functions directed

(continued on page 96)

by system software. Essentially, the software controls sampling, data manipulation, error detection, PWM rates of the outputs, and monitoring of realtime activities. It can also generate graphics on the microcomputer's video screen if there is adequate memory space in the user's system. To facilitate program development and allow easy interaction by the operation, it was important that a high level language be used. Interpretive BASIC was available on the microcomputer; although slow, it is feasible because the kiln response does not require high speed program execution.

The operator plays an important role in kiln control through software. When starting the controller program, the operator must provide whatever information is requested by the program. For example, the controller must be given the set points generated by the schedule program so that it can track the schedule interpolated[8] from those points. The number of days in the drying run and the limits on the control parameters also must be input to the program. Once the controller is running, the operator can break the program execution and change the numerical value of variables or constants in the system. A listing of the program or any variable may also be displayed to aid system analysis. To resume execution of the program, the operator simply types CONT, and execution will continue from the point at which it was halted. The operator may edit the system program with the microcomputer's editor. However, the program must be restarted after any editing of its code.

Two alarm conditions are detected in software: control error and sensor failure. Control failure is indicated when a kiln parameter exceeds its limits. Two tests are performed to determine sensor failure. One test compares the most recent data of an individual channel with the cumulative average of that channel's data over 6-hour intervals. The second test compares the most recent data of an individual channel with the parameter average corresponding to that channel. If both tests fail, the sensor is probably not operating properly. The system reacts by eliminating that channel from consideration and alerting the operator. If only one test fails, the operator is alerted, but the data in that channel are considered valid.

Summary and Recommendations

This project completed a major step in developing fully automatic instrumentation for process control in wood-drying kilns: to design a computer based unit capable of inputting information from external signals, outputting commands to external devices, and displaying current and past kiln conditions—all under operator control. Results of this effort demonstrate that a personal microcomputer can be suitable for industrial control purposes. Provisions for expanding the system, including a TRS-80 line printer, an RS-232 link, TRS-80 mini discs, and memory expansion, can be implemented in the system easily.

Thus far the personal microcomputer has functioned well in the surrounding kiln environment. Although the controller has not yet been exercised for a complete drying run of approximately 60 days, it has been reliable over several 3- to 4-day runs. The controller outputs (PWM solenoid actuation) have performed extremely well and with high reliability. Although this research represents a major step in establishing fully automatic process control for lumber drying, sensing techniques can be improved further and a control model based on a mathematical model[9] of the kiln environment developed.

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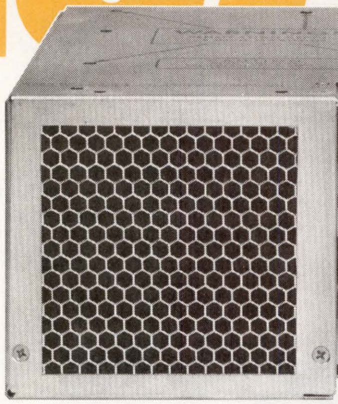

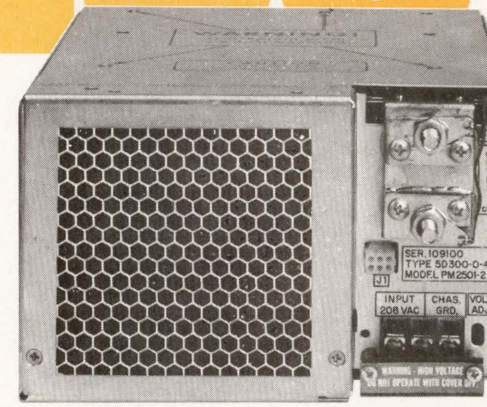

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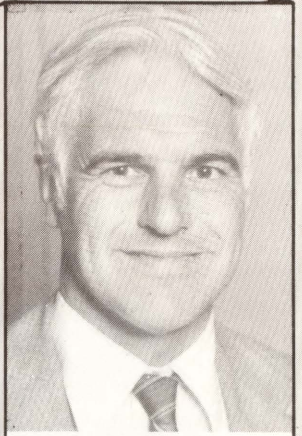

Derek Bray
Chairman of the Professional Program Committee

Dixy Lee Ray
Keynote Speaker

Wescon/81's theme—"30 Years of Electronics Leadership"—significantly denotes the anniversary of what is claimed to be America's largest high technology electronics exhibition and convention. Returning to Brooks Hall & Civic Auditorium for the last time as part of its annual alternating with the Los Angeles area (in 1983 the much larger Moscone Convention Center will be host), this year's conference is expected to be the largest held in San Francisco in the past dozen years. In fact, it is going to be necessary to locate many overflow exhibits in ballrooms and corridors of the San Francisco Hilton Hotel. As usual, the conference is co-sponsored by northern and southern units of the Institute of Electrical and Electronics Engineers and the Electronics Representatives Association.

Professional program

Approximately 160 papers will be presented in three blocks of sessions on each of the three days of the conference. Each session will last two hours, with session blocks beginning at 9 am, 12:30 pm, and 3:30 pm. Major subject emphasis will be on microprocessor/computer hardware and software, but other subjects such as memories, signal and array processing, analog to digital interface systems, voice processing, industrial control, and integrated circuit sensors will also be covered. As an assist to *Computer Design* readers, sessions of particular interest are outlined below, separated into categories.

Microprocessors/computers

Progressions from familiar 8-bit microcomputers to the more sophisticated and capable 16-bit families offer advantages for both hardware and software system designers. In a group of sessions spread over three days, representatives of several microcomputer, peripheral, and memory manufacturers and of the companies that design those products into their systems will discuss both the advantages of the products and the implications inherent in their use. Emphasis will be on information of value to the working engineer.

(continued on page 100)

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Wescon/81

Session 1 **16-Bit Microcomputer Architecture—Advanced Features**

Tues, Sept 15 **9-11 am** **Continental Ballroom 4**

Organizer and Chairperson: K. S. Padda, Texas Instruments, Inc, Houston, Tex

"Practicality and Advance Architecture of NS16000"
S. Bal, National Semiconductor Corp, Santa Clara, Calif

"Advanced Processor or Advanced System"
D. Lafitte, Texas Instruments, Inc, Houston, Tex

"iAPX 286"
P. Heller, Intel Corp, Santa Clara, Calif

"MC 68000—Breakaway from the Past"
J. Browne, Motorola, Inc, Austin, Tex

"Design Decisions in the Z8000 Architecture"
S. R. Mateosian, Zilog, Inc, Cupertino, Calif

Session 5 **Advanced 16-Bit Peripherals: The Family Concept**

Tues, Sept 15 **12:30-2:30 pm** **Continental Ballroom 4**

Organizer: H. Bryce, Motorola, Inc, Austin, Tex
Chairperson: D. Collins, Motorola, Inc, Austin, Tex

"Coherent Family of Peripherals for the Z8000 16-Bit Microprocessor"
M. Pitcher, Zilog, Inc, Cupertino, Calif

"Advanced Peripherals Complement NS16000 Family"
G. Martin, National Semiconductor Corp, Santa Clara, Calif

"Motorola Support Chips Complement the MC68000 Architecture"
D. Collins, Motorola, Inc, Austin, Tex

"Task Driven Peripheral Interfaces"
D. Tjoa and T. Rossi, Intel Corp, Santa Clara, Calif

"Intelligent Peripherals of the VLSI Era"
J. Samsen, Texas Instruments, Inc, Houston, Tex

Session 9 **Virtual Memory Concepts for 16-Bit Microprocessors and Computers**

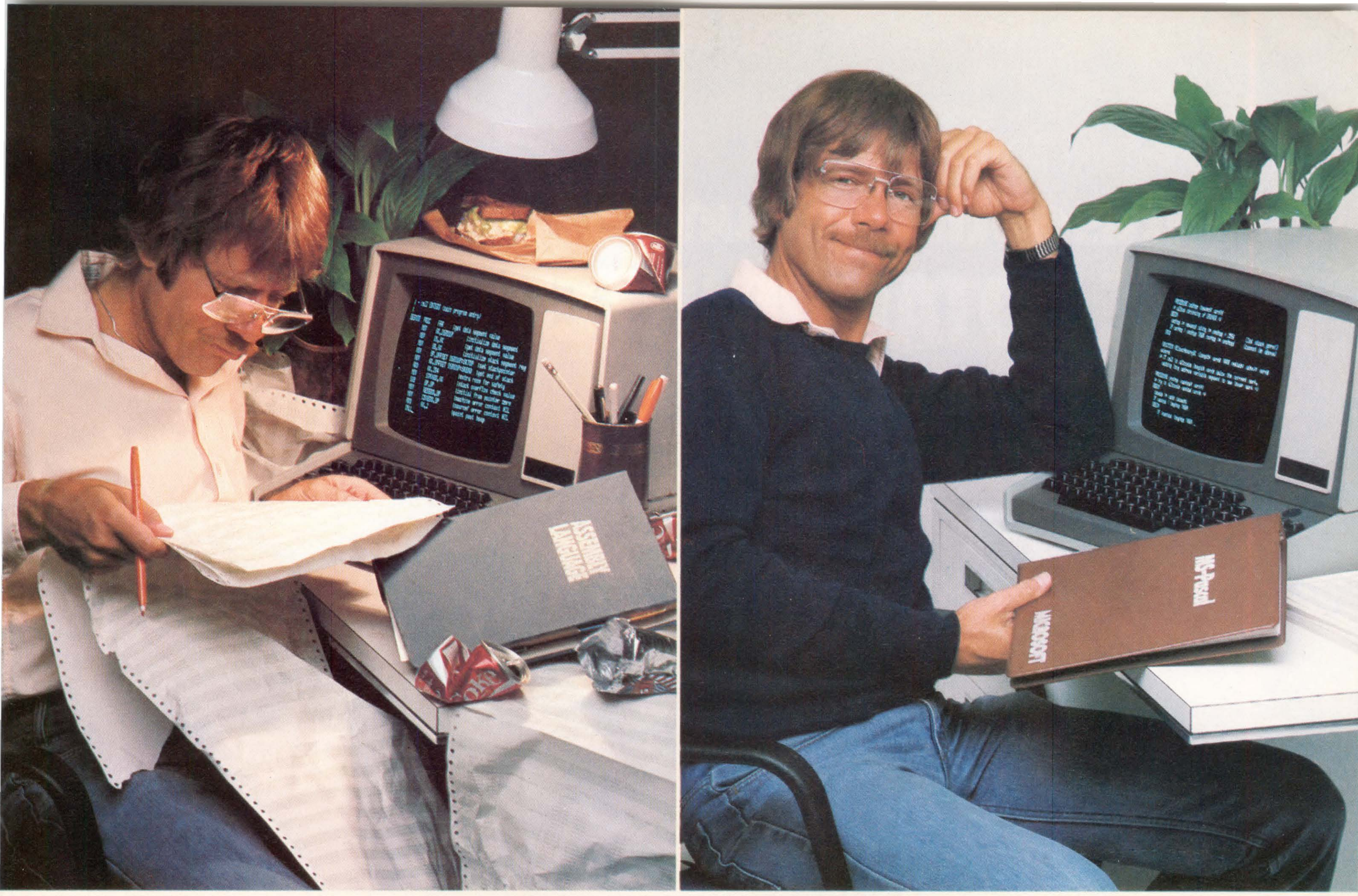
Tues, Sept 15 **3:30-5:30 pm** **Continental Ballroom 4**

Organizer and Chairperson: J. J. Farrell III, Motorola, Inc, Austin, Tex *(continued on page 103)*

WESCON PROFESSIONAL PROGRAM SUMMARY*

Day	Time	CONTINENTAL BALLROOM 4	CONTINENTAL BALLROOM 5	CONTINENTAL BALLROOM 6	CONTINENTAL BALLROOM 7
Tues, Sept 15	9 to 11 am	**1** 16-Bit Microcomputer Architectures—Advanced Features	**2** Speech Technology in the 80s	**3** Future Trends in Digital Signal/Array Processing	**4** Strategies for High Technology Product Marketing
Tues, Sept 15	12:30 to 2:30 pm	**5** Advanced 16-Bit Peripherals: The Family Concept	**6** Voice Processing—A Technology and Market Assessment for the 80s	**7** Modern Trends In Digitizing Signal Analyzers	**8** Technical Publishing Opportunities for Engineers
Tues, Sept 15	3:30 to 5:30 pm	**9** Virtual Memory Concepts for 16-Bit Microprocessors and Computers	**10** Computer Controlled Voice Message Systems and the Office of the Future	**11** User Friendliness in Advanced Instrumentation	**12** California's Favorable Small Business Climate
Wed, Sept 16	9 to 11 am	**13** Trends in CMOS Microprocessors	**14** Very High Speed Digital LSI	**15** Integrated Circuit Sensors Markets, Applications, and Technologies	**16** Fiber Optics Today
Wed, Sept 16	12:30 to 2:30 pm	**17** Single-Chip Microcomputers I—Cost Effective System Solutions	**18** Transporting High Speed Digital Signals Point to Point on Circuit Board Assemblies	**19** The Outlook for Linear ICs in the 80s	**20** Flux Residue Removal and Its Impact on Quality Control and Reliability
Wed, Sept 16	3:30 to 5:30 pm	**21** Single-Chip Microcomputers II—Software Considerations	**22** Advances in Leadless Chip Carrier Packaging and Attachment Techniques	**23** Analog-Digital Interface Systems	**24** Mixers for High Performance Radio
Thurs, Sept 17	9 to 11 pm	**25** Electrically Erasable Memories Provide New System Flexibility	**26** Multitasking Operating Systems for Microprocessors	**27** Microcomputer Bus Structures—What the Future Holds	**28** Technology to Help the Handicapped
Thurs, Sept 17	12:30 to 2:30 pm	**29** Battery Backup Techniques for Memory Preservation	**30** Computers for Engineering Applications	**31** The Expanding Spectrum of Microprocessor Peripherals	**32** Competition in the Electronics Industry—Legal Pitfalls and Remedies
Thurs, Sept 17	3:30 to 5:30 pm	**33** User Programmable Circuits	**34** Standard Software for Standard Microcomputer Modules	**35** Microprocessors in Industrial Control—A Look at Distributed Control Networks	**36** Manufacturing Offshore in the 80s

*All sessions are being held at the San Francisco Hilton Hotel. The session schedule is subject to change.



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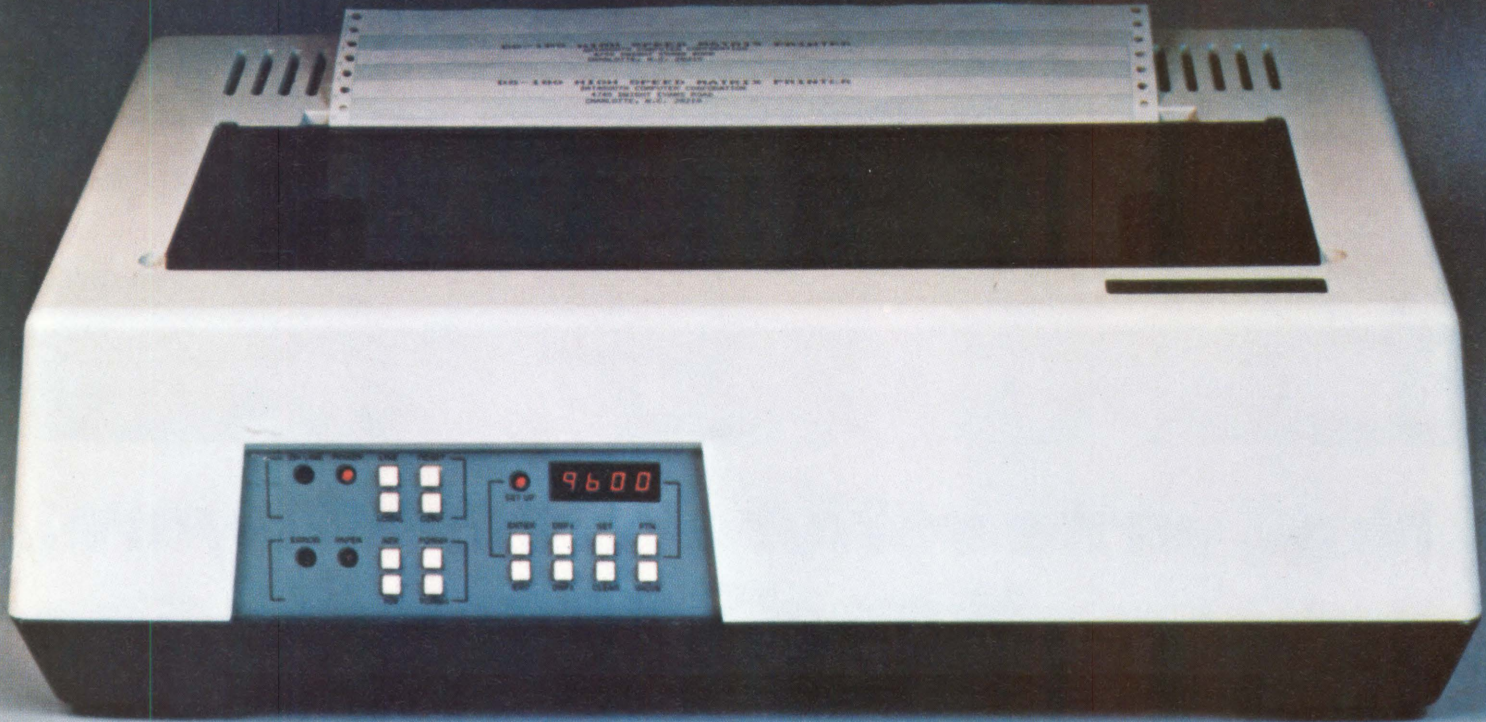

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"The Management of Extended Memory for Concurrent Processes in TI Microprocessor Pascal"
L. Spry, Texas Instruments, Inc, Lewisville, Tex
"iAPX 286—Virtual Memory and Distributed Processing"
R. Markowitz, Intel Corp, Santa Clara, Calif
"Memory Management Made Easy with the Z8000 Microprocessor Family"
S. Walters, Zilog, Inc, Cupertino, Calif
"Implementation of a Virtual Memory System Using the MC68451 Memory Management Unit"
H. Scales, Motorola, Inc, Austin, Tex
"Benefits of NS16082 Memory Management Unit"
Y. Lavi, National Semiconductor (Israel), Ltd, Herzliya, Israel

Session 13 — Trends in CMOS Microprocessors
Wed, Sept 16 — 9-11 am — Continental Ballroom 4

Organizer and Chairperson: B. Huston, Motorola, Inc, Austin, Tex
"Low Power Peripheral Components, Hardware/Software Support Solve System Design Problems"
G. Mullinix and D. Zrepski, National Semiconductor Corp, Santa Clara, Calif
"A High Performance CMOS ROM-Based Processor"
B. Hilton, Motorola, Inc, Austin, Tex
"High Performance CMOS Microprocessor Family Is Designed to Ease the Software Development Burden"
F. Toth, American Microsystems, Inc, Santa Clara, Calif
"1800 Series Peripherals—Building Blocks of a Complete Processor Family"
J. Paradise, RCA Solid State Div, Somerville, NJ

Session 17 — Single-Chip Microcomputers I—Cost Effective System Solutions
Wed, Sept 16 — 12:30-2:30 pm — Continental Ballroom 4

Organizer and Chairperson: J. Fattal, Motorola, Inc, Austin, Tex
"6500/1-11 High Performance Microcomputer"
D. Smith, Rockwell International, Anaheim, Calif
"The Hardware Features of the M6805 Family of Single-Chip Microcomputers"
J. Farrell, Motorola, Inc, Austin, Tex
"Cost Effective Microcontroller"
J. Irwin, National Semiconductor Corp, Santa Clara, Calif
"16-bit CMOS Microcomputer"
J. Bauer, American Microsystems, Inc, Santa Clara, Calif
"A Compact Z8 Microcomputer Board with On-Chip BASIC"
P. Brown, Zilog, Inc, Cupertino, Calif

Session 21 — Single-Chip Microcomputers II—Software Considerations
Wed, Sept 16 — 3:30-5:30 pm — Continental Ballroom 4

Organizer and Chairperson: J. Boney, Motorola, Inc, Austin, Tex
"Single-Chip Microcomputer Programming—A User's View"
A. Choperena, E. I. duPont de Nemours & Co, Wilmington, Del
"Large Computer Programming Traits in a Single-Chip Microcomputer Family"
B. Huston, Motorola, Inc, Austin, Tex
"Programming Trade-offs—Code Density Versus Speed"
R. Dumse and P. T. Whalen, Rockwell International, Anaheim, Calif
"Software Design Practices for Single-chip Microcontrollers"
M. Stevens, American Microsystems, Inc, Santa Clara, Calif
"Programming the TMS 7000"
J. Millar and M. Patrick, Texas Instruments, Inc, Houston, Tex

Session 26 — Multitasking Operating Systems for Microprocessors
Thurs, Sept 17 — 9-11 am — Continental Ballroom 5

Organizer and Chairperson: T. Cramer, Zilog, Inc, Cupertino Calif
"iRMX Family of Operating Systems"
B. Schaefer, Intel Corp, Hillsboro, Ore
"BLMX 80"
N. Rodes, National Semiconductor Corp, Sunnyvale, Calif
"ZRTS, Zilog Realtime Software"
S. Savitzky, Zilog Corp, Cupertino, Calif
"Versa DOS"
J. Glaser, Motorola, Inc, Phoenix, Ariz
"An Anthropomorphic Approach to Operating Systems"
J. Lowry, Advanced Micro Computers, Santa Clara, Calif

Session 27 — Microcomputer Bus Structures—What the Future Holds
Thurs, Sept 17 — 9-11 am — Continental Ballroom 6

Co-organizers: S. Edelman, Marken Communications, Palo Alto, Calif, and J. Spackman, Texas Instruments, Inc, Houston, Tex
"STD Bus: A Standard for the 80s"
W. C. Cummings, Mostek Corp, Carrollton, Tex
"The Multibus/IEEE P796 Bus Standard-The Multiprocessing Bus of the 80s"
J. Barthmaier and R. Dilbeck, Intel—OMS, Hillsboro, Ore
"IEEE P696.1: The Bus Whose Time Has Come"
M. Wright, SSM Microcomputer Products, San Jose, Calif
"Functional Architecture: Optimizing a Powerful System Bus Solution"
L. Ames, Texas Instruments, Inc, Houston, Tex
"The Advanced Microcomputer System Bus—IEEE P896"
A. Allison, Consultant, Los Altos, Calif

Session 31 — The Expanding Spectrum of Microprocessor Peripherals
Thurs, Sept 17 — 12:30-2:30 pm — Continental Ballroom 6

Organizer and Chairperson: B. Huston, Motorola, Inc, Austin, Tex
"A New LSI CRT Controller for Avanced Video Display Systems"
M. Herman and J. Tweedy, Standard Microsystems Corp, Hauppauge, NY
"Battery Backed-up Realtime Clock Techniques"
R. Davis, Motorola, Inc, Austin, Tex
"Local Networks—LSI's Next Challenge"
M. Stieglitz, Western Digital Corp, Newport Beach Calif
"Microprogrammable Peripheral Controllers for 8-bit Systems"
M. Patrick and J. Millar, Texas Instruments, Inc, Houston, Tex
"Color Graphics with an Advanced LSI Controller"
J. Wise and H. Szejnwald, NEC Microcomputers, Wellesley, Mass

Session 34 — Standard Software for Standard Microcomputer Modules
Thurs, Sept 17 — 3:30-5:30 pm — Continental Ballroom 5

Organizer and Chairperson: D. E. Starbuck, Rockwell International, Anaheim, Calif

"The Marriage of Forth and the RM 65 Modular Microcomputer"
G. Malolepsy, Rockwell International, Anaheim, Calif
"Architectural Building Blocks"
A. Doerr and R. Markowitz, Intel Corp, Santa Clara, Calif
"M/OS-80 A CP/M Compatible Operating System"
W. R. Vaughn, Mostek Corp, Carrollton, Tex
"Texas Instrument's Component Software"
R. Jackson, Texas Instruments, Inc, Houston, Tex

Memories

Session 25 Electrically Erasable Memories Provide New System Flexibility
Thurs, Sept 17 9-11 am Continental Ballroom 4
Organizer and Chairperson: J. F. Rizzo, Intel Corp, Santa Clara, Calif
"2816 Floating Gates Bring a Revolution to Nonvolatile Memory"
J. F. Rizzo, Intel Corp, Santa Clara, Calif
"A Family of In-the-Circuit 5-V-Programmable Nonvolatile Static RAMs"
J. Drori and G. Landers, Xicor, Inc, Sunnyvale, Calif
"New Developments in MNOS EAROMS"
E. Edwards, General Instrument Corp, Hicksville, NY
"CMOS Brings New Capabilities to Electrically Erasable Memory"
G. DesRochers, Hughes Semiconductor, Newport Beach Calif
"Bubble Memory Developments in the 1980s"
R. McDonald, Texas Instruments, Inc, Houston, Tex

Session 29 Battery Backup Techniques for Memory Preservation
Thurs, Sept 17 12:30-2:30 pm Continental Ballroom 4
Organizer and Chairperson: D. Linden, Consultant, Little Silver, NJ
"Miniature Batteries for Memory Preservation"
D. Linden, Consultant, Little Silver, NJ
"New Lithium Batteries for Memory Preservation"
R. E. Ralston, Duracell International, Inc, Elmsford, NY
Characteristics of the Lithium Solid State Battery in Memory Circuits"
S. J. Garlock, Lear-Siegler Instrument Div, Grand Rapids, Mich
"The Use of Lithium Batteries in Memory Circuits"
L. H. Fentnor and L. A. Schaum, Hughes Aircraft Co, Tucson, Ariz
"Lithium Batteries for Industrial Control Equipment"
W. Phillips, Texas Instruments, Inc, Johnson City, Tenn
"Lithium/Thionyl Chloride Batteries for Memory Preservation"
B. Ravid, Tadiran, Ltd, and G. Giveony, Israel Electronics Industries, Ltd, Rehovot, Israel

Speech Technology

Session 2 Speech Technology in the 80s
Tues, Sept 15 9-11 am Continental Ballroom 5
Organizer and Chairperson: S. B. Crook, Texas Instruments, Inc, Midland, Tex
"Overview of Speech Technology of the 80s"
S. K. Brown, Texas Instruments, Inc, Midland, Tex
"Linear Predictive Coding"
J. Gaur, General Instruments, Hicksville, NY
"High Quality and Less Memory Using Waveform Digitization"
F. Wickersham, National Semiconductor Corp, Santa Clara, Calif
"Proposal for a High Quality Complex LPC (Linear Predictive Coding) Speech Coder/Decoder"
W. Hartwell, Bell Telephone Laboratories, Naperville, Ill
"Industrial Applications of Speech Technology"
A. F. Mandel and K. M. Eichler, Westinghouse R&D Center, Pittsburgh, Pa

Session 6 Voice Processing—A Technology and Market Assessment for the 80s
Tues, Sept 15 12:30-2:30 pm Continental Ballroom 5
Organizer and Chairperson: H. K. Lake, Jr, The Diebold Group, Newport Beach, Calif
"Voice Processing—An Outlook for the Coming Decade"
N. R. Miller, The Diebold Group, New York, NY
"Automatic Speech Recognition Systems—Evaluation and Application"
D. F. Fink, Intel Corp, Santa Clara, Calif
"Voice Data Entry—An Industrial User's Perspective"
A. R. Strass and A. J. Nanow, General Electric Co, Bridgeport, Conn
"Implemented Voice Recognition, A Practical Application"
E. R. Wendorff, AT&T Long Lines, Beaminster, NJ

Integrated Circuits

Session 14 Very High Speed Digital LSI
Wed, Sept 16 9-11 am Continental Ballroom 5
Organizer and Chairperson: R. Walker, LSI Logic Corp, Santa Clara, Calif
"A Systems Approach to VLSI Logic"
C. Davis, IBM Corp, Hopewell Junction, NY
"ECL Provides Highest Available System Speeds"
H. Mueller, Motorola, Inc, Mesa, Ariz
"CML Masterslice Family Provides Sub-Nanosecond VLSI"
D. L. Presholdt, Honeywell Solid State Electronics Div, Plymouth, Minn
"Future Trends in Very High Speed LSI Technology"
C. Dell'Oca, LSI Logic Corp, Santa Clara, Calif

Session 19 The Outlook for Linear ICs in the 80s
Wed, Sept 16 12:30-2:30 pm Continental Ballroom 6
Organizer and Chairperson: D. Grant, Analog Devices Semiconductor, Wilmington, Mass
"Applications of CMOS Technology to Linear ICs and Data Converters"
J. Zis, Intersil, Inc, Cupertino, Calif
"Technological Advances in Monolithic Instrumentation Amplifiers and Voltage Regulators"
C. Nelson, National Semiconductor Corp, Santa Clara, Calif
"Bipolar Amplifiers with High Accuracy and Bandwidth"
T. Schwartz, Precision Monolithics, Inc, Santa Clara, Calif
"Achieving the Impossible: Systems-Level Precision ICs"
L. Counts, Analog Devices Semiconductor, Wilmington, Mass

(continued on page 106)

Miscellaneous

Session 3 — Future Trends in Digital Signal/Array Processing
Tues, Sept 15 — 9-11 am — Continental Ballroom 6

Organizer and Chairperson: L. F. Pittroff, Advanced Micro Devices, Sunnyvale, Calif

"Minimum-Chip-Count Number Cruncher Uses Bipolar Co-Processor"
C. Hastings, R. Blasco, Consultant, and U. Gordon, Monolithic Memories Inc, Sunnyvale, Calif

"Advances in Array Processor Programming Techniques"
D. Birkner, Computer Design & Applications, Newton, Mass

The Application of FFT in Fast Convolution and Digital Filtering"
A. M. Peterson, Stanford University, Stanford, Calif

"FFT Address Sequencer Gives Easy Access to the Frequency Domain"
B. J. New, Advanced Micro Devices, Sunnyvale, Calif

"Digital Correlators Bring DSP Techniques to New Areas"
J. A. Eldon, TRW LSI Products, Inc, La Jolla, Calif

Session 7 — Modern Trends in Digitizing Signal Analyzers
Tues, Sept 16 — 12:30-2:30 pm — Continental Ballroom 6

Organizer and Chairperson: A. W. Crooke, Data Precision Corp, Danvers, Mass

"The Modern Digital Oscilloscope and Its Applications"
A. Tegen, Nicolet Instrument Co, Madison, Wis

"Sampling Network Analyzer for Periodic Functions"
B. Talambiras, Dranetz Engineering Labs, Inc, Edison, NJ

"The Computing Oscilloscope, Why? How?"
G. Williams and G. Kueneman, Norland Corp, Fort Atkinson, Wis

"User Interface: Complexity vs Flexibility in a Sampled Data Instrument"
A. W. Crooke, E. E. Stebbins, and C. Gyles, Data Precision Corp, Danvers, Mass

Session 8 — Technical Publishing Opportunities for Engineers
Tues, Sept 15 — 12:30-2:30 pm — Continental Ballroom 7

Organizer and Chairperson: J. A. Titus, The Blacksburg Group, Blacksburg, Va

"Why Engineers Can't Write—Or Can They?"
G. Rotsky, *Electronic Engineering Times,* Mannasset, NY

"How a Technical Publisher Can Enable You to Share Your Knowledge"
J. B. Pascoe, Howard W. Sams and Co, Inc, Indianapolis, Ind

"Special Writing and Publishing Opportunities"
J. A. Titus, The Blacksburg Group, Blacksburg, Va

"The Engineer and His Audience—Non-Technical Writing"
A. Osborne, Osborne & Associates, Berkeley, Calif

Session 16 — Fiber Optics Today
Wed, Sept 16 — 9-11 am — Continental Ballroom 7

Organizer and Chairperson: R. L. Ohihaber, Belden Corp, Geneva, Ill

"Application Considerations for Fiber Optic Cables"
R. L. Ohihaber, Belden Corp, Geneva, Ill

"Advances in Fiber Optic Connectors"
J. Leidy, AMP, Inc, Harrisburg, Pa

"Low Cost Fiber Optic Components for Industrial Applications"
J. Bliss and D. Stevenson, Motorola HFO Div, Phoenix, Ariz

"Fiber Optic Transmission Links"
H. A. Carnes and E. E. Basch, GTE Laboratories, Waltham, Mass

Session 18 — Transporting High Speed Digital Signals Point to Point on Circuit Board Assemblies
Wed, Sept 15 — 12:30-2:30 pm — Continental Ballroom 5

Organizer: S. E. Grossman, Stephen E. Grossman, Inc, Los Altos, Calif

Chairperson: S. Smockler, Kollmorgen Corp, Glen Cove, NY

"Implementing High Speed Logic on Printed Circuit Boards"
T. Balph, Motorola, Inc, Phoenix, Ariz

"High Speed Signal Pathways from Board to Board"
R. K. Southard, AMP, Inc, Harrisburg, Pa

"Implementing Controlled Impedance Techniques in Discrete Wiring"
J. P. Plonski, Kollmorgen Corp, Glen Cove, NY

"Design Considerations of Printed Circuit Transmission Lines for High Performance Circuits"
N. Arvanitakas and J. J. Zara, IBM Corp, Endicott, NY

Session 23 — Analog-Digital Interface Systems
Wed, Sept 16 — 3:30-5:30 pm — Continental Ballroom 6

Organizer and Chairperson: J. Sullivan, Harris Semiconductor Group, Melbourne, Fla

"Session Overview"
J. Sullivan, Harris Semiconductor Group, Melbourne, Fla

"DAS Front End Design Considerations"
T. Fleming, Harris Semiconductor Group, Melbourne, Fla

"New Low Cost 8-bit A-Ds with Unique Input MUX in 'Mini' to 'Skinny' DIP Packages"
T. Reagan, National Semiconductor Corp, Santa Clara, Calif

"Current New Device Technology, Including Fabrication Aspects"
G. McGlinchey and E. Macachor, Advanced Micro Devices, Sunnyvale, Calif

"Ins and Outs of Interfacing A-D Converters"
D. Grant, Analog Devices Semiconductor, Wilmington, Mass

Session 30 — Computers for Engineering Applications
Thurs, Sept 17 — 12:30-2:30 pm — Continental Ballroom 5

Co-organizers and Co-chairpersons: T. H. Bruggere, Mentor Corp, West Linn, Ore, and B. Hamilton, Tektronix, Beaverton, Ore

"Desktop Computer: Versatile Tools for Computer Aided Engineering"
J. Stedman, Tektronix, Beaverton, Ore

"CAE—Productivity Improvements Using Desktop Computers"
B. Cummings, Hewlett-Packard Co, Fort Collins, Colo

"Trends in Desktop CAD"
T. H. Bruggere, Mentor Corp, West Linn, Ore

"System Needs for Engineering Workstations"
J. D. Howard, Intel Corp, Aloha, Ore

Session 33 — User Programmable Circuits
Thurs, Sept 17 — 3:30-5:30 pm — Continental Ballroom 4

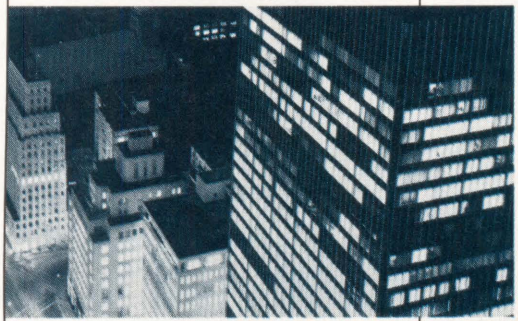
Organizer and Chairperson: F. H. Cherrick, Intel Corp, Santa Clara, Calif

"Registered P/ROMs"
R. C. Lutz, Advanced Micro Devices, Sunnyvale, Calif

(continued on page 108)

When the Canadian Government needed a totally secure local data distribution network, they ordered our Fiber Optic System.

The data distribution Problem: The Canadian Government made their problem completely clear. One of their agencies was expanding its headquarters into several floors of an adjacent office building and they insisted upon installing a secure local data distribution network to carry "sensitive" traffic. Minimal start-up costs and future expandability were further considerations.



The Fiber Optic Solution: Versitron's System Design Group studied the problem and recommended a fiber optic network utilizing advanced fiber optic modems. This recommendation assured total traffic security throughout the network. Not only because of fiber optic's inherent physical protection; but also through a unique intrusion alarm feature that immediately shuts down any data link where the integrity is suspect. The start-up cost for this system proved to be highly competitive with an equivalent coaxial system. Plus, the fiber optic system's capacity could be expanded by a factor of fifteen by merely replacing the single channel modem with Versitron's 15 channel multiplexer system.

The Final Outcome: The Canadian Government was impressed. They ordered the fiber optic system and, in one stroke, met all of their requirements for security, cost, and expandability.

The lesson learned here is applicable to a large range of data distribution situations. Let Versitron's System Design Group assist you on your next project. Call us at (202) 882-8464. Or write to: 6310 Chillum Place N.W., Washington, D.C. 20011.

VERSITRON, INC.

CIRCLE 62 ON INQUIRY CARD

"Designing a 16k CMOS P/ROM"
C. Rantz and R. Goslin, Harris Semiconductor, Melbourne, Fla

"New P/ROM Technology Provides High System Throughput"
W. Plummer and H. Fung, Intel Corp, Santa Clara, Calif

"High Level Language for Program Array Logic"
J. M. Birkner, Monolithic Memories, Sunnyvale, Calif

"Innovative Architecture in Programmed Logic Increases Design Flexibility"
N. Cavian, Signetics, Sunnyvale, Calif

Session 35 Microprocessors in Industrial Control—A Look at Distributed Control Networks
Thurs, Sept 17 3:30-5:30 pm Continental Ballroom 6

Organizer and Chairperson: G. O. Roop, Mostek Corp, Carrollton, Tex

"RIOS—Crydom's Remote I/O System"
V. Gregory, Crydom Division of International Rectifier, El Segundo, Calif

"Distributed Process Control to Multiple Remote Job Sites Via a Serial Link"
B. Tracey, OPTO-22, Huntington Beach, Calif

"Serial Communication Protocol Improves Data Acquisition and Control System Cost and Performance"
S. Osgood, Analog Devices/Intersil, Cupertino, Calif

"Implementation of Distributed Processing on the STD Bus"
G. Davidson, Mostek Corp, Carrollton, Tex

Exhibits

To help attendees and minimize time spent searching for comparison of like products, exhibits at the Civic Auditorium and Brooks hall will be separated into four main categories:

- components, microelectronics, and fiber optics
- instrumentation, test equipment, and control systems
- computers, EDP peripherals, and data communication
- production and packaging equipment.

Those at the Hilton Hotel will be in the Tower Lobby, Franciscan Room, and Plaza Room. Exhibit hours at all locations will be 9 am to 6 pm on Tuesday, 9 am to 7 pm on Wednesday, and 9 am to 5 pm on Thursday.

A Wescon Special Exhibit at the Garden Lane in the Hilton Hotel will highlight small business and engineering computers. Stress will be on existing functions and capabilities.

Registration

Attendance at Wescon/81 is open to all electronics industry members over 18 years of age. To register:

- contact a Wescon exhibitor, obtain a complimentary registration card, and complete and mail the form August 28; or
- contact a member of Wescon's Inner Circle or Attendance Committee at major facilities to obtain a registration card and complete and mail the card before August 28 to receive free admission credentials (cards will require a $10 admission fee if presented at the door); or
- stand in line and register at the door for $10.

For further information, contact Wescon/'81, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965.

Marketing conference and keynote luncheon

New business possibilities developing because of shortages will be the basis of this year's Marketing Conference theme: "Future Marketing Opportunities." Both the Marketing Conference and the accompanying Keynote Luncheon will take place at the Hilton Hotel on the Monday preceeding the Professional Program and Exhibition. Included will be a "bread and butter" forecast of the electronics marketplace; a review of electronics in the "futuristic world," moderated by industry analyst Ben Rosen; and discussions of marketing techniques. Keynote speaker will be Dixy Lee Ray, former Governor of the State of Washington and ex-chairperson of the Atomic Energy Commission. □

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CIRCLE 64 ON INQUIRY CARD

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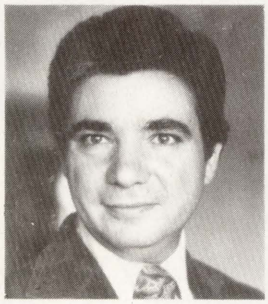

V. R. Basili

R. Yeh

Program Chairmen

Productivity: An Urgent Priority

Tues, Sept. 15

11:30 am - 12:30 pm

Invited speakers (concurrent sessions):

Session 1 B. Boehm, TRW/DSSG
Chairperson: Y. Ohno, Univ of Kyoto

Session 2 J. Albus, National Bureau of Standards
Chairperson: V. Basili, Univ of Maryland

Session 3 C. V. Ramamoorthy, Univ of California
Chairperson: R. Yeh, Univ of Maryland

2 - 3:30 pm

Session 4 Human Factors
Chairperson: Y. Chu, Univ of Maryland
"Human Productivity in Software Development"
R. C. Linger, International Business Machines Corp
"Matching Software Tools to Organizations Using Maturity Factors"
J. Matejeck, U. S. Dept of Commerce, and M. Weiser, Univ of Maryland
Discussant: J. Gannon, Univ of Maryland

Session 5 Quality Assurance I
Chairperson: F. Kamijo, IIPA
"Allocation of Resources for Software Reliability"
H. Hecht, SoHaR, Inc
"Steps: Integrated Software Standards and Its Productivity Impact"
M. Azuma and Y. Mizuno, Nippon Electric Co
Discussant: J. Musa, Bell Laboratories

Session 6 Experience with Tools
Chairperson: to be determined
"Experiences with a Code Generation Tool"
R. Roonan, College of William and Mary
"Productivity Experiences with a Scenario Tool"
R. E. A. Mason and T. T. Carey, Univ of Guelph
Discussant: M. Zelkowitz, Univ of Maryland

4 - 5:30 pm

Session 7 Software Productivity Measurement Panel
Chairperson: B. Curtis, ITT
Discussant: S. Fuller, Digital Equipment Corp

Session 8 Human Factors Panel
Chairperson: B. Schneiderman, Univ of Maryland
Discussant: E. Sibley, Alpha Omega Group, Inc.

Session 9 Education Panel
Chairperson: C. Coates, Purdue Univ
Discussant: H. D. Mills, International Business Machines Corp

Wed, Sept 16

10:30 am - 12:30 pm

Session 10 Software Models
Chairperson: I. Miyamoto, Univ of Maryland
"Applicability of the Rayleigh Model to Three Different Types of Software Projects"
W. K. Wiener-Erlich, J. Hamrick, and V. Rupolo, Bankers Trust Co
"The Implications of Program Composition and Size on Development Productivity"
L. Paulsen, International Business Machines Corp
"An Approximate Queueing Network Model of a Shared Device among Independent Computing Systems"
A. Mink, National Bureau of Standards and S. C. Silio, Univ of Maryland
Discussant: M. Lehman, Imperial College

Session 11 Hardware Design
Chairperson: H. Cragon, Texas Instruments, Inc
"Design Methodology for Testable VLSI"
C. Chen, Sperry Univac

Holmberg DIP IC Sockets set two new pricing standards:

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CIRCLE 65 ON INQUIRY CARD

"A Mask Artwork Analysis System for Bipolar Integrated Circuits"
T. Chiba, T. Mitsuhashi, M. Takashima, and K. Yoshida, Toshiba Corp
"Measuring CAD Productivity"
D. Borda, Arthur D. Little Inc.
Discussant: D. Kuck, Univ of Illinois—Urbana-Champaign

Session 12 Database Standards Panel
Chairperson: E. H. Sibley, Alpha Omega Group, Inc

2 - 3:30 pm

Session 13 Quality Assurance II
Chairperson: Y. Mizuno, Nippon Electric Co
"A Structured Functional Testing Approach Generic Data Structure + Test Algorithm = Test Program"
C. Lin, NCR
"The Role of Strategic Planning for Productivity Improvement Through Computer Aided Engineering"
L. Lipchin, Nolan, Norton & Co
Discussant: A. Goel, Syracuse Univ

Session 14 Tool Evaluation
Chairperson: C. Vick, Systems Control, Inc
"Early Experience with MONSTR: A Software Maintenance"
K. Knobe, Massachusetts Computer Assoc, Inc
"COBOL Machine Evaluation"
R. Nakazaki, M. Yamamoto, M. Yokota, and M. Umemura, Nippon Electric Co
Discussant: W. Riddle, Cray Laboratories

Session 15 Evaluation Development
Chairperson: L. Belady, International Business Machines Corp/T. J. Watson Research Center
"Evolutionary Cyclic Model for Development of Complex Software Systems"
R. Friehmelt, Karlsruhe Inst
"Productivity across the Software Life Cycle"
M. Lehman, Imperial College

4 - 5:30 pm

Session 16 Software Management Productivity Panel
Chairperson: E. Goldberg, TRW, Inc
Discussant: J. Manley, ITT

Session 17 Office Automation Panel
Chairperson: R. Kopka, U. S. Air Force Office of Scientific Research
Discussant: V. Lum, International Business Machines Corp

Session 18 ICAM Panel
Chairperson: R. Mayer, AFWAI/MLTC Wright-Patterson Air Force Base
Discussant: L. Stucki, Boeing Computer Services

Thurs, Sept 17

10:30 am - 12:30 pm

Session 19 Software Development Process
Chairperson: To be determined
"Applying Industrial Engineering to the Software Development Process"
W. W. Agresti, Univ of Michigan
"Unifying Data Flow and Control Flow Based Modularization Techniques"
K. Iwamoto and O. Shigo, Nippon Electric Co
"Specification vs Implementation"
D. Ridjanovic and M. L. Brodie, Univ of Maryland
Discussant: D. Parnas, International Business Machines Corp

Session 20 Software Design
Chairperson: C. V. Ramamoorthy, Univ of California
"Documentation Technology for Packing Hierarchical Function, Data, and Control Structures"
S. Hanata, T. Satoh, and M. Inada, Yokosuka Electrical Commun Laboratory
"An Interactive Tool for Narrative, Operational, and Structural Documentation"
P. N. Robillard, Ecole Polytechnique, Montreal
"A Successful Approach to Managing, Developing, and Maintaining Software"
R. G. Lanergan and D. K. Dugan, Raytheon Co
Discussant: G. Parikh, Shetal Enterprises

Session 21 DOD's Software Technology Initiative
Chairperson: J. Batz, U.S. Dept of Defense
Discussant: J. Munson, System Development Corp

2 - 3:30 pm

Session 22 Software Productivity Tools and Techniques Panel
Chairpersons: C. Davis, U.S. Army; P. Mauro, TRW, Inc
Discussant: D. Gries, Cornell Univ

Session 23 Software Product Quality Panel
Chairperson: Y. Mizuno, Nippon Electric Co
Discussant: S. Gerhart, Univ of Southern California, Information Sciences Inst

Session 24 Software Productivity via Hardware Architecture
Chairperson: Y. Patt, Univ of California
Discussant: Y. Chu, Univ of Maryland

Tutorials

Four all-day tutorials—**Database Management in the 80s, Office Automation Systems, Productivity Improvement Plans for White Collar/Knowledge Worker Organizations, and Software Design Techniques**—will be presented on Sept 14, preceding the beginning of COMPCON Fall '81. Registration for these tutorials requires payment of an extra fee.

Registration

Reduced fees will be charged for all registrations prior to Sept 4. After that date, payment of full fees will be required, both for mail and at conference registrations.

Fees for advance (and regular) registration are: any tutorial *or* the conference *only*, $85 ($95) for members, $95 ($110) for non-members; any tutorial *and* the conference, $170 (180) for members, $185 ($195) for non-members. A discount registration of $30 for the Conference *only* is available for IEEE student members who are not employed full time. Tutorial registration fees include luncheon and notes; conference registration fees include one copy of the *Proceedings* and two drink tickets each for parties hosted by COMPCON on Tuesday and Wednesday evenings.

Exclusive new Zenith CRT Display with L-Power for logic circuits means lower system cost.

This is no ordinary CRT Display. It also provides the power for your terminal logic circuits. This unique, scan-derived system replaces conventional power supplies, and results in CRT Display systems that are compact, uncomplicated, and have fewer parts. You get optimum reliability, a cooler-running terminal and lower system cost.

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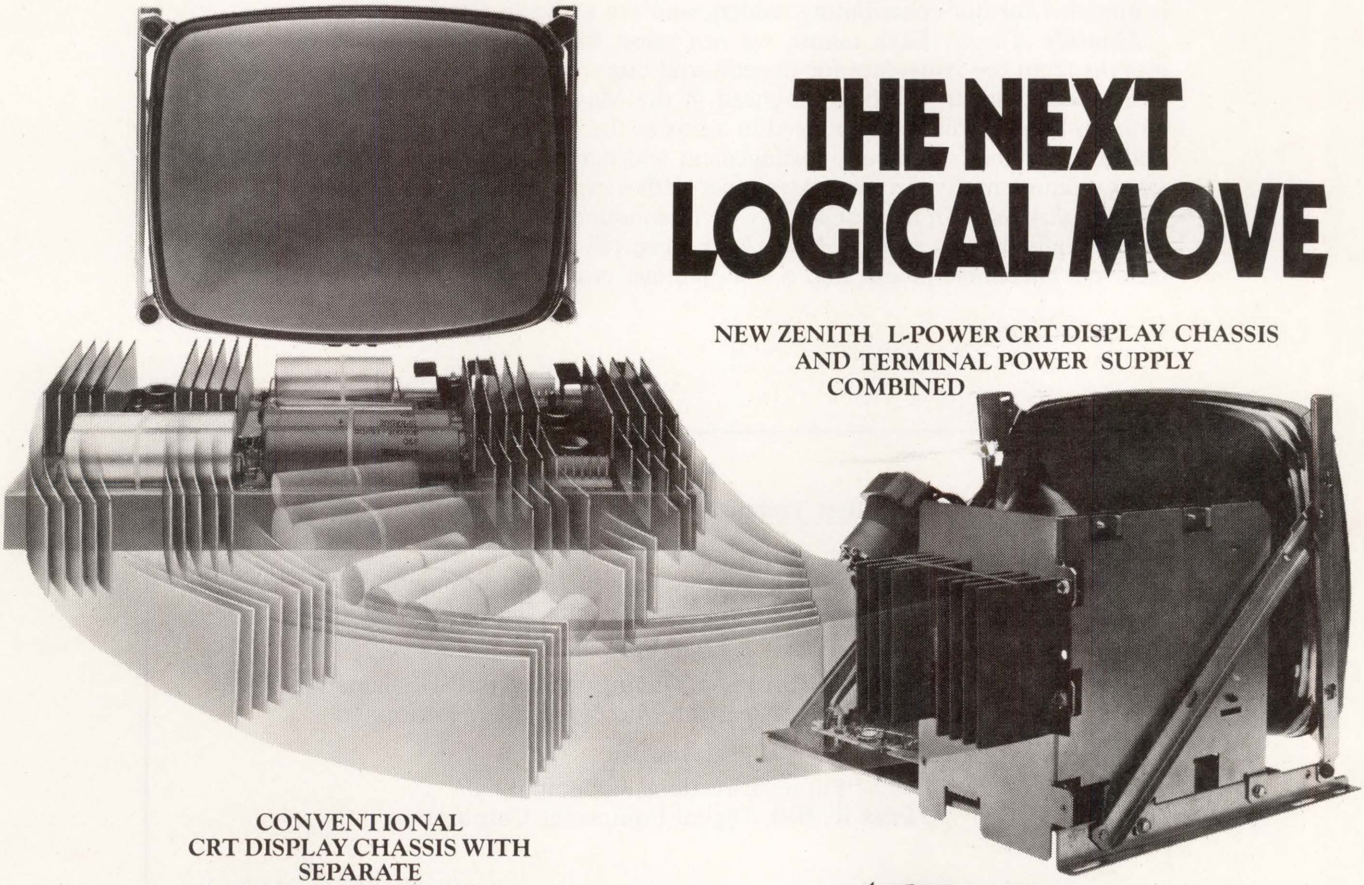

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CIRCLE 66 ON INQUIRY CARD

ANNOUNCING: *COMPUTER DESIGN'S* TECHNICAL WRITING AWARD PROGRAM

Because you, our readers, are the principal source of our best technical articles, we feel that it's about time you got some public recognition for your contributions to your colleagues and the state of digital systems art. Therefore, we are proud to announce the *Computer Design* Technical Writing Award Program. A winning article will be selected each month, starting with January 1981. The choice will be based on a weighted score tabulated from the editorial box scores in each issue.

Eligibility: You must be employed in a technical department of your company. Although this includes technical writers because they generally work in a technical department, we must exclude professional writers from advertising agencies or in-house public relations or communications departments and professional free-lance writers. The award is intended for our contributing readers who are active in a technical capacity.

Monthly Award: Each month we will select the best article. It will take about six months from the issue date for the editorial box scores to reach a steady state value, ie, December's winner will be announced in the May 1982 issue. Starting in October the monthly winner will be announced in a box at the bottom of our editorial page. We will notify the winner's company management and make arrangements to have a *Computer Design* representative present the winner with a certificate citing the award.

Annual Award: In May of 1982, we will announce the best article for 1981. Watch for more details on this early in 1982. All we can tell you now is that the 1981 winner will receive a handsome plaque and a Windjammer cruise for two in the Caribbean.

Best Technical Article of the Month

January

"32-Bit Minicomputer Achieves Full 16-Bit Compatibility"
Steve Wallach and Chuck Holland, Data General Corporation

February

"Reducing Roundoff Errors in Microprocessor Based Calculations"
Henry A. Davis, American Microsystems, Incorporated

March

"Future Directions in Computing"
James R. Bell, Digital Equipment Corporation

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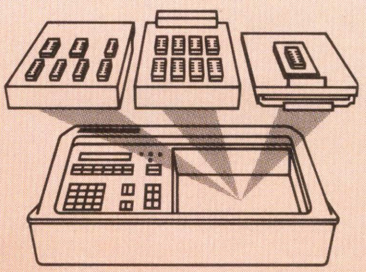

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23 communication formats including six for development systems. Development systems, computers, teletypes and CRT terminals interface easily with the System 19. The System 19 accepts micro-processor instruction codes from Motorola, Intel, Tektronix, Fairchild, FutureData and other development systems without intermediary equipment.

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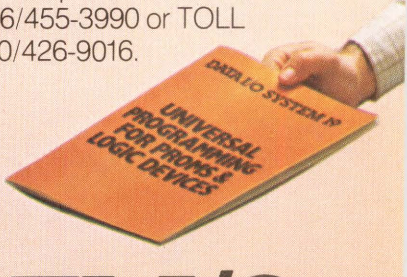

DATA I/O

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EXHIBIT B:
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Monolithic Systems MSC 3610 is a direct replacement for the DEC M8210 VAX memory. The 256KB system is designed to provide maximum heat dissipation and thus extend memory life.

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IN CONCLUSION:
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MSC MODEL NUMBER	LSI-11	LSI-11/2	LSI-11/23	VAX 11/780	VAX 11/750	PDP-11/70	PDP-11/04	PDP-11/05	PDP-11/10	PDP-11/30	PDP-11/34	PDP-11/35	PDP-11/40	PDP-11/44	PDP-11/45	PDP-11/50	PDP-11/55	PDP-11/60	DATA SYSTEM 330	DATA SYSTEM 350	DATA SYSTEM 570	NEAREST * DEC MEMORY EQUIVALENT
3602						X															X	MK11-
3605							X	X	X	X	X	X	X		X	X	X	X		X		NONE
3606							X				X							X				MS11-L
3607						X	X	X	X	X	X	X	X		X	X	X	X		X	X	NONE
3608						X	X	X	X	X	X	X	X		X	X	X	X		X	X	NONE
3610				X																		MS780
3611						X															X	MK11-
3612					X																	MS750
3901						X															X	NONE
4604	X	X	X																X			MSVII
4804		X	X																X			MSVII
To Be Announced														X								MSII-M

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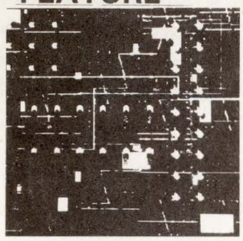
FEATURE



Digital signature analysis techniques isolate most circuit board defects by extending an analog philosophy

In-circuit testing comes of age

Card-edge functional testing of digital circuit boards is no longer cost-effective. Component-by-component, in-circuit test equipment can now isolate as many as 98% of all circuit board defects. Therefore, it simply does not pay to purchase a card-edge test system to catch the remaining 2%; it is, instead, less costly to omit functional testing altogether and troubleshoot, or even discard, any boards that fail system-level tests later on.

A card-edge test verifies the functioning of a circuit board as a whole; an in-circuit test verifies individual components on a board, one at a time, without regard for how the components interact in the overall circuit. From these bare definitions, it would seem that card-edge testing is the better method. After all, even if an in-circuit test showed that all the components on a board worked, there would be no guarantee that the board as a whole worked. However, a closer look at card-edge and in-circuit test technologies reveals that card-edge testing does have inherent limitations, and that today's in-circuit test systems are sufficiently sophisticated to eliminate almost all of these limitations.

At first, in-circuit for analog, card-edge for digital

One basic limitation of card-edge testing is that it cannot test analog circuit boards. The task of diagnosing an out of tolerance reading that shows up at a card-edge connector is mathematically intractable. There are two reasons for this. One is the problem of observability: Card-edge testers cannot measure the analog signals at a board's internal nodes, nor can they deduce continuous internal signals from what can be measured at the edge. The other is controllability: To create a desired condition at a particular internal node requires exercising intervening devices. A defect in an intervening device prevents the tester from establishing the desired state at the node of interest.

With an in-circuit test system, these problems do not exist. In-circuit tests are administered via a multiple-pin bed-of-nails fixture, and a different fixture is built for each different circuit board configuration. When a board is being tested, the vacuum-actuated fixture pins come into contact with every node on the board, isolating each part and testing it for its own characteristics. Every component is directly accessible, and therefore fully observable and controllable.

In-circuit testing is particularly straightforward when applied to analog components. In fact, when in-circuit testing made its debut in the early 1960s, it was used strictly as a method for testing analog boards. Card-edge testing was still the accepted procedure for digital boards, where the discreteness of the input/output states reduced the edge-testing problem to manageable proportions—at least in the beginning days of digital electronics.

Card-edge testing shows limitations

By the early 1970s, the in-circuit test approach had found its way onto many production floors—not only

Douglas W. Raymond
Plantronics/Zehntel, Incorporated
2625 Shadelands Dr, Walnut Creek, CA 94598

as an effective means of testing analog boards but also as a preliminary screening procedure for hybrid boards. In other words, in-circuit testing of hybrid boards was usually followed up by card-edge testing. At that time, card-edge testing was still the only viable approach for all-digital boards.

However, as digital devices became more complex, card-edge testing proved less satisfactory. The twin problems of observability and controllability caused difficulties even on digital boards. The setting and reading of internal logic states from the edge of a board under test meant working through numerous layers of suspect logic. This can be an enormously difficult task if the board contains even a small number of integrated circuits. Three different approaches have been developed over the years in an attempt to reduce this difficulty.

One of these approaches involves an elaborate set of engineering rules for designing testable circuits, rules such as partitioning the circuit into functional blocks; providing for component initialization; breaking feedback loops; and avoiding time-dependent events such as pulse outputs, certain race conditions, and the outputs from 1-shots and oscillators. In theory, boards designed according to these rules are easier to test on a card-edge tester. In practice, however, these rules are rarely followed.

Even if all the design-for-testability rules are followed, card-edge testing of complex digital boards is impossible without the other two support approaches that have been developed: manual probing and software simulation. Today, almost all card-edge test systems use manual probing routines to pinpoint defects. Manual probing lets the test system gain direct access to the board's internal nodes. In theory, this gets around the observability and controllability limitations of card-edge testing. The trouble is that manual probing is a slow and costly procedure that usually requires a skilled operator. In addition, when a defect is located, the board must be removed from the test system and the defect repaired before other aspects of board function can be tested. Several time-consuming, one-defect-at-a-time iterations may be needed before a board is fully repaired. By contrast, an in-circuit tester locates all defective components in one pass, thereby significantly shortening the test and repair operation.

Software simulations, used by test engineers to generate card-edge test programs, also have their problems. Complex boards require complex simulations, which in turn require fast computers with large memories. Even with the most sophisticated simulators, program generation for card-edge testing is a laborious and intricate procedure that only a skilled programmer can perform.

Because of the difficulty of following the design-for-testability rules and because of the time and expense involved in manual probing and software simulation, card-edge testing began to outlive its usefulness. Electronic systems were built around increasingly complex digital circuit boards, and it was vital to test these boards thoroughly, at reasonable cost. As a result, test equipment companies developed techniques for extending the in-circuit test approach to digital devices. As in-circuit techniques evolved, yields at the next level of test began to rise. By the late 1970s, yields of 95% were common. This meant that 95% of the boards that passed an in-circuit test would have also passed a subsequent functional test. Today, yields as high as 98% can be achieved by using the latest technological advances combined with careful debugging and test program maintenance. With high yield, it is now difficult to justify the use of a card-edge tester at all.

In-circuit testing goes digital

What is it that makes in-circuit testing successful enough to replace traditional card-edge testing on the production line? Part of the answer lies in the in-circuit test techniques themselves, especially signature analysis and programmable input specification. The other part of the answer lies in automated test program development.

Signature analysis and Gray codes

Digital signature analysis, as applied to in-circuit testing, means driving a device's inputs with a set of harmonically related square waves alternating between logic states 0 and 1, then feeding each output into a signal generating register that produces a 4-digit hexadecimal number, or signature. A master clock maintains the proper relationships between the inputs and ensures that the output is sampled over a specified time period.* (See Fig 1.)

The value of digital signature analysis is that test engineers need not program the tester to analyze the expected outputs in detail. Instead of having to check out perhaps thousands of logic states in order to test an output response, the tester need only look at a 4-digit signature. A device passes inspection if all its output signatures agree with those of a similar device known to be free of defects; the correct signatures, determined empirically, are stored in test system memory.

The value of using harmonically related square waves for inputs is that there is no need to program all possible truth table values bit-by-bit—a prohibitively time-consuming procedure. Instead, the square wave inputs automatically interact to produce all possible combinational states at the device inputs over a time period equal to the period of the lowest-frequency input. This is the time period over which the outputs must be sampled.

On today's equipment, F1 is typically set at 500 kHz. Programming the test of a digital device simply means stating which nodes get which input frequencies and which nodes should produce what output signatures. (See Fig 2.) If any of the signatures fail to match, a diagnostic message is printed indicating which device failed.

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*For a more detailed discussion of the basics of signature analysis, see D. W. Raymond, "Component-by-Component Testing of Digital Circuit Boards," *Computer Design,* April 1980, pp 129-137.

Programmable sequence generator

Digital devices in the large scale integration (LSI) range generally require a more sophisticated approach than simply exercising all possible input combinational states. In the case of a microprocessor, for example, particular waveforms defined by the device manufacturer must be applied to the control lines in order for the device to accept or produce data. Generating the required waveforms by properly combining the different Gray code frequencies is a prohibitively tedious task, especially since many such waveforms may be needed for testing different operations of the device. What is needed is a simple method of specifying arbitrary input waveforms. In other words, what is needed is not just a Gray code sequence generator, but a programmable sequence generator.

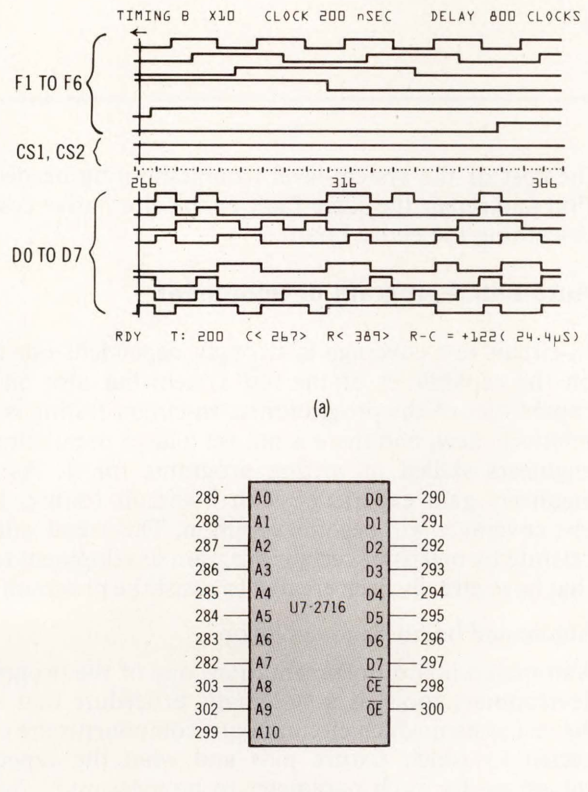

Fig 1 Digital signature analysis. Oscilloscope trace in (a) shows inputs and outputs for testing 2716 type 16k ROM in (b). Top six traces display six highest frequency inputs. Next two traces are ROM chip select inputs forced low during test. Bottom eight traces are ROM outputs D0 to D7. Harmonic frequency inputs form all possible input combinations in Gray code sequence. Output signature is 16-bit cyclic redundancy check character generated from output signal at particular node

```
"U7-2716"

300,LL      CS1
298,LL      CS2

289,F1 288,F2 287,F3 286,F4
 285,F5 'A0-A4
284,F6 283,F7 282,F8 303,F9 302,F10
 'A5-A9
299,F11 'A10

CRC C9F1 M290 CRC 99A3 M291 CRC 588A
 M292    'D0-D2
CRC 71C3 M293 CRC 3449 M294 CRC F357
 M295    'D3-D5
CRC BF31 M296 CRC 8A1A M297     'D6-D7
```

Fig 2 In-circuit test segment. Program to test 2716 ROM from Fig 1 first assigns logic low to chip enable and output enable lines at nodes 300 and 298, respectively. It next assigns an input frequency to each input node, with low-order address line A0 receiving highest frequency, F1, and high-order line A10 receiving lowest frequency, F11. Program then designates expected signature for each node, eg, signature C9F1 at node 290, signature 9983 at node 291. Tester prints message "U7-2716" when it detects incorrect signature

One recently developed programmable sequence generator provides four different levels of programming capability. On the lowest level, programmers can specify the actual bit pattern that is to appear on a particular pin. Bit patterns that make up basic suboperations for the device, eg READ, WRITE, FETCH, are called protocols; these protocols are available for use at the second level of programming capability. At this second level, the protocols can be combined into subroutines corresponding exactly to device instructions. The subroutines are available on the third level of the hierarchy, where they can be combined to produce the actual segment of code that tests all the desired functions of the device. The test segment for the device is then incorporated into the test program for the entire circuit board of which the device is a part. Invoking the test segments for the various LSI devices on the board constitutes the fourth and highest level of programming capability.

A complete device test for the 8085 microprocessor, for example, executes a number of the device's instructions, such as LHLD (Load H and L Direct) and SHLD (Store H and L Direct). The LHLD instruction uses two different suboperations: one FETCH and four READs. Each of these suboperations is tested by applying the proper bit stream to the proper pins in accordance with the device manufacturer's specifications. The bit-by-bit, level 1 programming for the FETCH protocol is shown in

```
CONTROL PROTOCOL FETCH (16)
NODE 72,1H          'RESET IN*
NODE 111,1L,1H      'X1
NODE 110,1H,1L      'X2
NODE 73,1H          'READY
LISTEN,1L,1H,6L
DRIVE,5L,6H,5L
ADVANCE,1L
DONE
```

Fig 3(a) Control protocol. In test of 8085 microprocessor FETCH, nodes 111 and 110 are clock pins X1 and X2, respectively. Bit patterns (eg 1L,1H) repeat to fill out 16-cycle FETCH sequence. Nodes 72 and 73 are reset and ready pins, respectively, both forced high during test. LISTEN and DRIVE sample and apply test data, where H enables operation and L suppresses it. ADVANCE directs tester to next instruction word; here, ADVANCE is disabled during all 16 clock pulses

```
SUBR LHLD
    INVOKE FETCH
    INVOKE READ
    INVOKE READ
    INVOKE READ
    INVOKE ENDREAD
RET
```

Fig 3(b) Test subroutine. For 8085 Load H and L Direct (LHLD) instruction, which accesses five bytes of data, five invoke statements branch to various control protocols that handle appropriate data bytes

```
INVOKE RESET
INVOKE START
CALL LHLD
CALL SHLD
INVOKE STOPIT
INVOKE EXHALT
HALT
DONE
```

Fig 3(c) Multifunction test of 8085. Program tests microprocessor reset and clocking capabilities, its ability to fetch instruction that reads additional data after execution (LHLD), and its ability to fetch instruction that writes data obtained prior to execution (SHLD)

Fig 3(a). The FETCH protocol and a protocol for the READ suboperation can be combined into the subroutine LHLD as shown in Fig 3(b), representing level 2 programming. On level 3 [Fig 3(c)], LHLD combines with other subroutines and protocols to produce a complete device test for the microprocessor. The example shown follows LHLD with SHLD, thereby testing the 8085's ability to reproduce data in one cycle that it had read in the previous cycle. Note that level 3 programming uses subroutines whose names are the same as the device mnemonics; therefore it is quite similar to using 8085 assembly language. The complete device test can then be incorporated into a circuit board test using level 4 programming, which simply means inserting the statement "8085" at the appropriate place in the overall test program.

The programmable sequence generator programmers need not go through this entire 4-level procedure for every LSI device under test because a magnetic disc library is supplied containing test templates for most of the popular LSI devices. The templates include complete device tests, instruction subroutines, and suboperation protocols. Stored subroutine and protocol templates can be used to construct test segments without having to perform level 1 bit-pattern programming. Level 1 bit-pattern programming is available to create customized protocols.

A programmable sequence generator is especially valuable for cost-effective testing of boards with numerous LSI components. For most such boards, a programmable sequence generator noticeably increases the yield. Even a small increase in yield—regardless of the source—can be economically significant. Because repairing a fault called out by an in-circuit test system takes only a few minutes, the labor cost is far less than the cost of the system-level troubleshooting needed to find and repair the same fault or the alternative cost of discarding the entire board.

Automated program development

In-circuit test coverage is strongly dependent not only on the capabilities of the test system but also on the capabilities of the programmer. In-circuit testing is still relatively new, and there is not yet a large population of engineers skilled in writing programs for it. As test engineers gain experience with in-circuit testing, high test coverages will become common. This trend will accelerate by means of certain program development tools that have already been created to assist the programmer.

Automated board documentation

Automated board documentation, one of the program-development tools, is a systematic procedure that tells the test system which circuit board components are connected to which fixture pins and what the expected values are for each parameter to be measured. This is typically performed in three steps. In step 1, the operator places a conductive plate over the fixture pins. On keyboard command, the pin numbers of the pins that have been wired are automatically displayed on the terminal, along with an exception list of all unused pins. This display helps the operator quickly locate any errors in the fixture assembly.

In step 2, the operator replaces the conductive plate with a circuit board known to be free of defects and issues a command causing the system to automatically map out and store all electrical continuities. Step 3 is an interactive procedure initiated by the PROBE command.

(continued on page 122)

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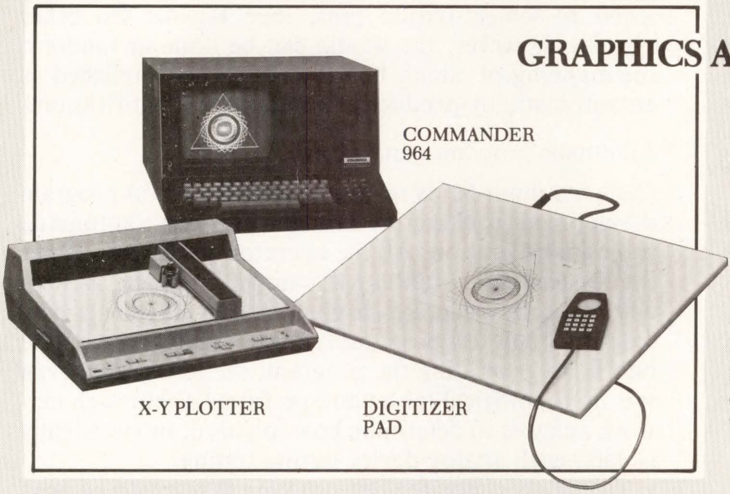

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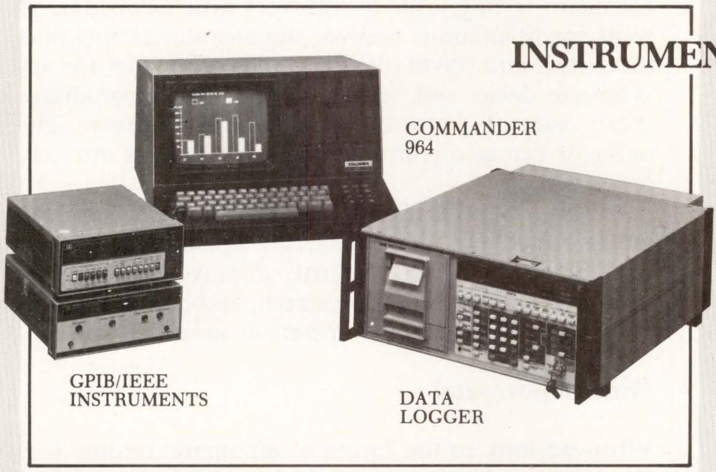

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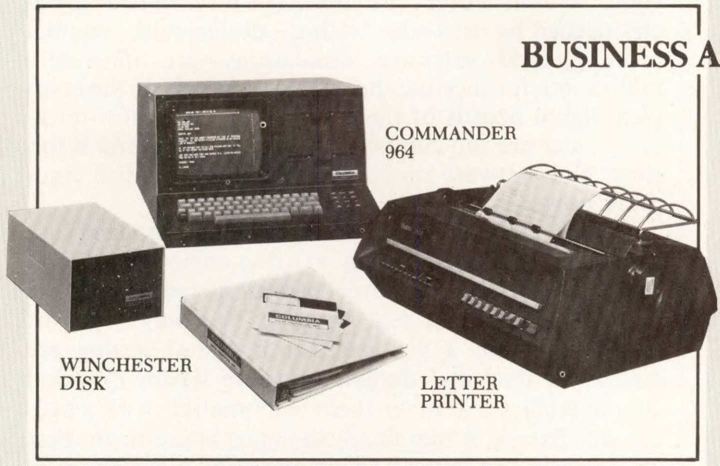

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The operator enters a component's name, and then is asked, via prompts on the terminal, to probe the component's leads and enter the expected values, including tolerances, of all parameters to be measured. (For probing integrated circuits, a special connector contacts 16 leads at a time. The expected values that the operator enters are the 4-digit hexadecimal signatures.) For popular LSI components, however, only the device name needs to be entered; the device test segment stored in the template library already contains the expected signatures. This is also true of any LSI devices for which complete test segments exist.

The result of these three steps of automated board documentation is a complete input list for the circuit board. On command, the system can now print a node-by-node list of components and/or a component-by-component list of nodes. This procedure streamlines two of the most time-consuming aspects of developing in-circuit test programs: determining continuities and wiring the fixture. Continuities, which are determined automatically in step 1, represent a laborious manual procedure with many other systems. Fixture wiring is generally an even more laborious task because on some systems the technician who assembles the fixture must keep track of which internal test system nodes are being wired to which fixture pins. (See Fig 4.) On other systems, however, the wiring can be done at random; the mapping of circuit board nodes is accomplished as an automatic by-product of component identification.

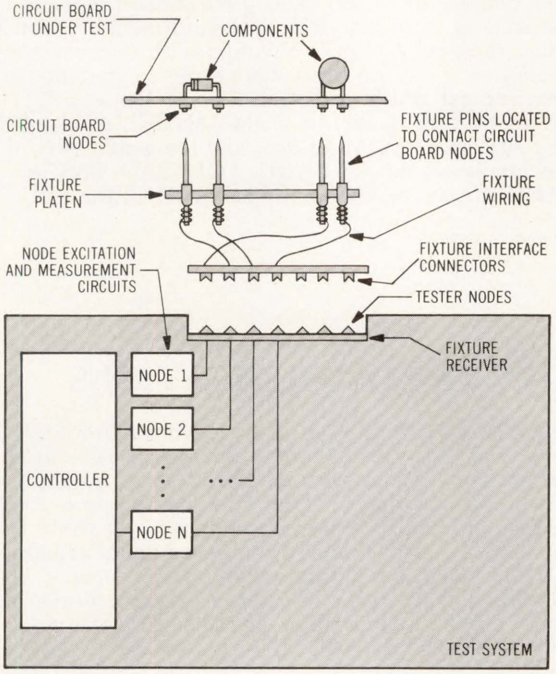

Fig 4 In-circuit test system diagram. Using in-circuit test system architecture and test fixture design shown here, fixture wiring can be done at random. Then, interactive phase of circuit board documentation automatically maps tester nodes to circuit board nodes

Automatic program generation

Once the input list is ready, another powerful program development tool can be brought into play: automatic program generation. All the operator needs to do is put the system into GENERATE mode, and the system automatically generates a complete, syntactically correct, in-circuit test program for every component on the board. In generating the program, the test system even sets up topological tables and performs a thorough network analysis to determine how to guard, or electrically isolate, each analog device during testing.

The newly generated test program is ready to be used for board testing, usually with very little debugging. If some modification is needed, the operator simply puts the system into DEVELOP mode, adds or rewrites the appropriate device test segments, and then incorporates these segments into the test template library. The operator can also rearrange the test segments into any order desired.

Program modification is performed interactively via the terminal. For debugging, the operator can insert breakpoints in a test segment, display the values of measured parameters on the screen, and change the program to modify these parameters as needed.

Growth potential

When we look to the future of automatic testing, it is clear that in-circuit testing will become the method of choice in almost every situation. The three outside agencies needed by card-edge testing—design rules, manual probing, and software simulations—are inherently inadequate for meeting the testing demands of the complex digital boards of the future. The design-for-testability rules are too cumbersome, manual probing is too slow, and software simulations require too much computer power.

In fact, there already are boards being produced that cannot be simulated on any existing computer system. These same boards, however, present no major problem to today's in-circuit test systems. The only kinds of boards that are a problem for in-circuit testing are boards of marginal design, or those having physical characteristics that make them incompatible with a bed-of-nails fixture. A marginally designed board might pass an in-circuit test but still fail in operation. This might be because the device inputs, for example, are less constrained than the precisely controlled inputs provided by the test system. Boards manufactured with painted-on resistors, or with components attached on both sides, or with conformal coatings (as in some military applica-

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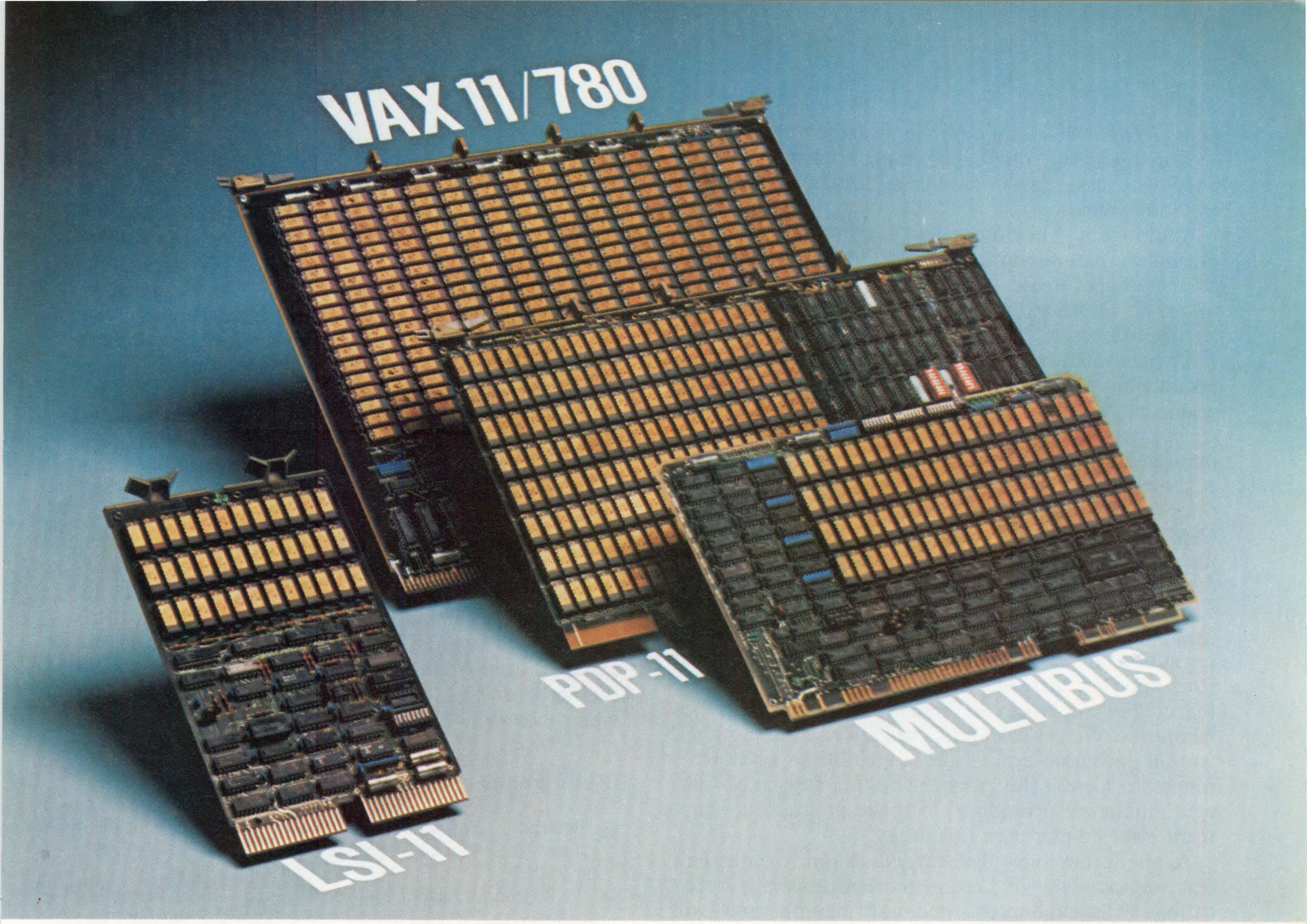

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tions) cannot be tested on an in-circuit test system because the fixture pins cannot make contact with every node. In these cases, card-edge testing is the only method available.

Additionally, in-circuit test technology currently precludes manufacturing smaller, less expensive in-circuit testers for use at field service depots. Card-edge testers do not have this limitation. As a result, card-edge testing dominates the realm of field service, motivating some manufacturers to opt for card-edge testing on the production line as well. Because production test programs can be made compatible with the smaller field-service test systems, overall programming costs are reduced. Although in some cases this may be a means of economizing today, it will not be sufficient justifications for a card-edge production test system tomorrow. Card-edge production testing has reached the limits of its capabilities; in-circuit production testing is still capable of rapid growth. Future in-circuit testers will incorporate faster and more complex device stimulation capabilities and will provide higher precision (increased resolution) in the timing relationships for stimuli and for responses; increased timing resolution will increase the ability of in-circuit testers to test high speed memories. We can also look forward to even more advanced program-generation capabilities—new techniques to handle the increased testing capacities, plus new interactive procedures to make program development even simpler than it is today.

As the technology advances, education for in-circuit test programmers will become more widespread. Applications skills will improve, and more manufacturers will enjoy the high yields that today's in-circuit testing systems already offer to those who know how to use them to full advantage.

Summary

Component-by-component, in-circuit testing of digital circuit boards has come of age. No longer requiring card-edge testing as a backup, in-circuit testing can isolate as many as 98% of all circuit board faults, including defects in complex LSI devices. The test techniques that make this possible are digital signature analysis and programmable input specification, while the programming tools that make the job tractable are automated board documentation and automatic generation of test programs.

Card-edge testing seems to have reached the limit of its capabilities. Card-edge testing aids—manual probing, software simulations, and a collection of design-for-testability rules—are cumbersome and time-consuming. Using these aids becomes prohibitively costly, and/or technically unfeasible, as boards become more complex. In-circuit testing procedures, however, are just as effective on complex boards as on simple ones, and the technology is capable of rapid growth. This growth, coupled with an increase in the number of people having expertise in in-circuit test programming, will help meet the need for high testing yields on tomorrow's digital circuit boards.

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About the Author:

Douglas W. Raymond is a project manager at Plantronics/Zehntel, Incorporated, where he is involved in hardware and software development of in-circuit test equipment. He was manager of the group that developed the Troubleshooter 800, an in-circuit test system incorporating digital signature analysis for testing complex digital components. Mr Raymond holds BSME and MSME degrees from the University of California at Berkeley.

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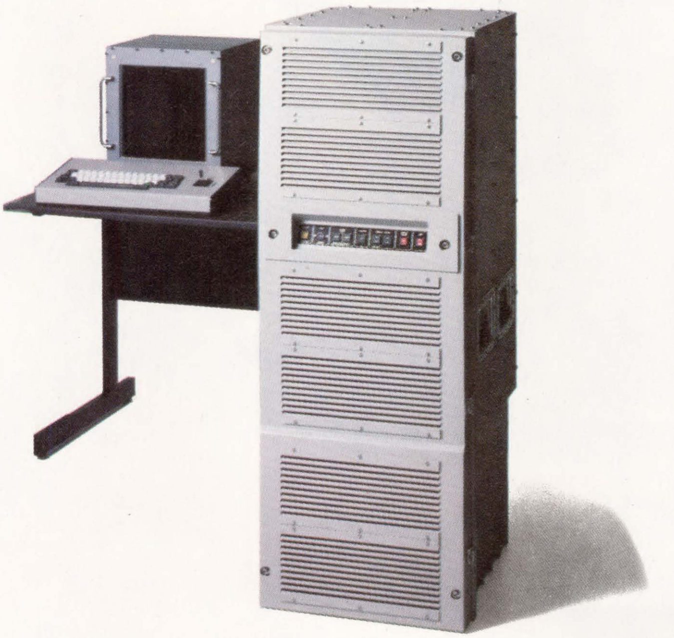

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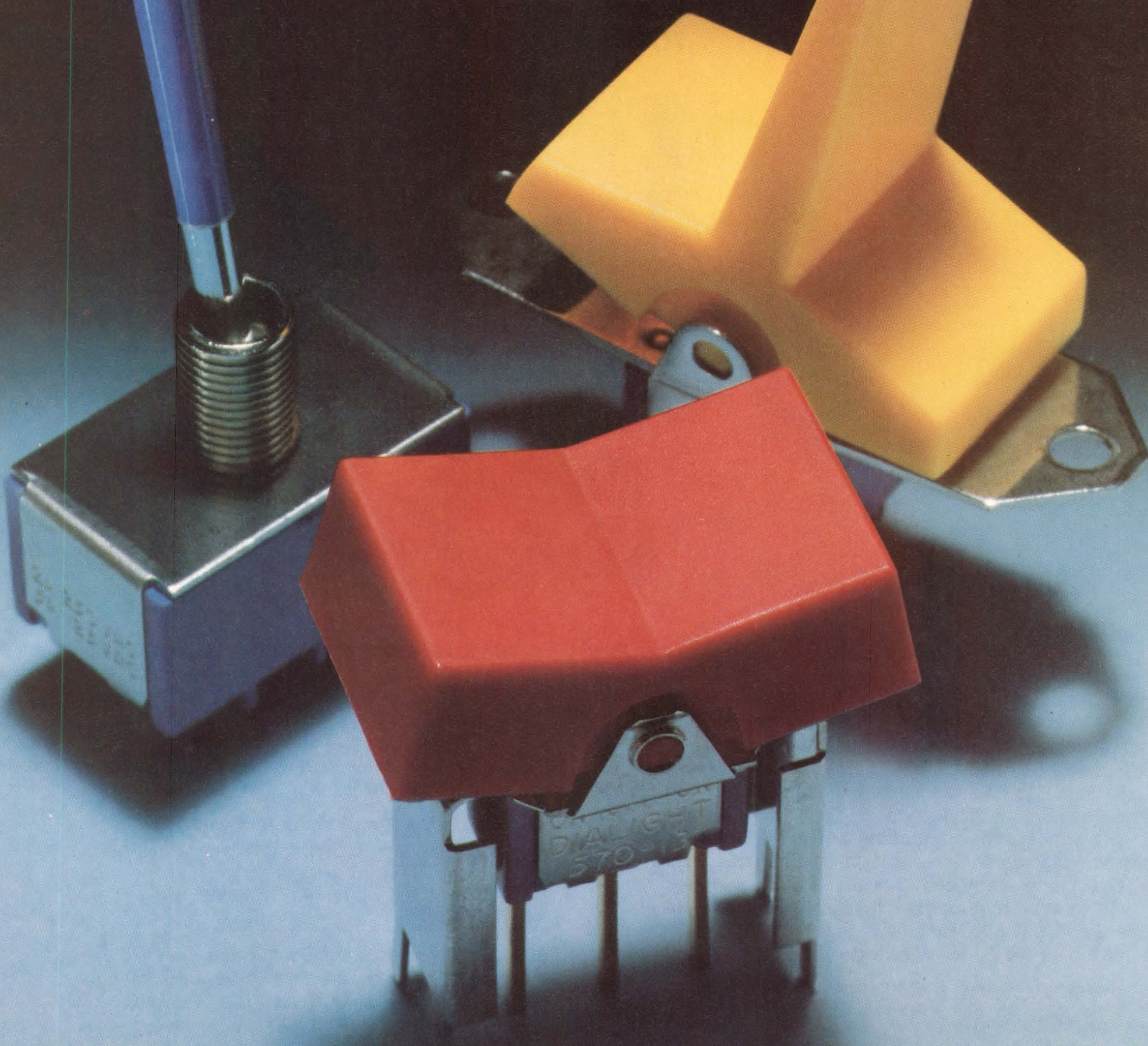

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FEATURE

Mailbox concept helps one program to direct several dedicated microprocessors, speeding up data acquisition and reducing the need for separate program or data memories

Parallel channel processing overlaps data acquisition and reduction

One of the primary advantages of digital data recording is that the data can be processed at a later time to remove glitches and nonlinearities, thus making the data suitable for display. The major problem with digital recording of analog data is the amount of storage required. Analog data digitized with 8-bit accuracy at a 10-kHz rate fills a 2400-ft, 1600-bits/in tape in less than an hour. Microprocessors present the opportunity to build intelligence into a recording system so that data correction can be done on the fly, permitting recording of the data in their final form, eg, some sort of paper record. The problem here is that most microprocessors (and minicomputers, for that matter) are not all that fast. At a 10-kHz data rate, only 100 μs are available to acquire, process, and output a data sample. Using tight assembly language programming and time-saving tricks, such as table lookup instead of computation, a microprocessor can be coaxed into performing useful tasks during those 100 μs. However, if the recording system has more than one data channel, one microprocessor cannot handle the load. A bipolar, bit slice microprocessor can do much more than a metal oxide semiconductor (MOS) processor, but to obtain any real advantage, custom microcode has to be written. This is out of the question for limited-production systems.

Thomas L. Clarke
National Oceanic and Atmospheric Administration
Atlantic Oceanographic and Meteorological Laboratories
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If the recording system has to handle n channels of data, the obvious approach is to provide n microprocessors. But this necessitates n random access memories (RAMs), n read only memories (ROMs), etc, and results in a complicated system. The approach outlined here uses a combination of hardware and software to implement a system using n microprocessors that share one ROM and one RAM. When all channels can be handled similarly, this approach saves considerable hardware.

Mailboxes

Some microprocessors facilitate connection of multiple processors to the same data, control, and address buses. The National Semiconductor SC/MP (INS8060) and the Fairchild F8 make shared bus systems particularly easy to implement. Other microprocessor families (eg, 8080 and 6800) can also be used but require random logic to implement a bus protocol that resolves access conflicts without excluding any processor for an excessive length of time.[1] A single microprocessor actively accesses the system buses less than half of the time; thus, several microprocessors can be tied to the same buses with little loss in speed but with extensive savings in hardware.

The most elegant hardware does nothing, of course, without software, and if a separate program has to be provided for each microprocessor, the advantages of shared buses are lost because separate programs generally require separate ROMs for each processor. If a software technique known as the mailbox is used, a common program can be shared by all the processors. Mailboxes are commonly used in large multiprocessing systems to effect communications between various tasks within the system. A mailbox is an area of memory, known to all programs or processors within a system, that contains parameters set by one program or processor and needed by another program or processor. When using the mailbox technique, the processor's access to the mailbox must be exclusive. If one processor is changing the mailbox's content while another is reading it, the second processor might receive erroneous information. Although there are techniques that guarantee exclusive access by using flags to signal that the mailbox is being accessed, it is simpler in a dedicated system to ensure exclusive access by means of established protocols.

In a data acquisition system, differences between the programs executed by the various processors in a system consist primarily of buffer addresses, input/output (I/O) port addresses, and, possibly, correction factors applied to the data. A system optimized for speed contains addresses in internal processor pointer registers that are initialized at system start-up. A mailbox can be used to guarantee that each processor has the appropriate addresses for its task and, initially, has a pointer to the first entry in a table of addresses. The first processor uses the pointer to load its registers from the table and then updates the pointer contained in the mailbox. The second processor loads its registers from the next entries in the table (appropriate to its task) and updates the pointer. This continues until all processors have been initialized.

Initializing the mailbox pointer presents a problem. An external signal must be available to inform a processor that it is the first to initialize and that the mailbox is empty. This is fairly easy with processors that have separate inputs on each chip. An appropriate pin is tied to logic 1 on the first processor and to 0 on the others. Alternatively, a master processor, can initialize the mailbox pointer, tables, etc, before relinquishing the bus and starting the slave processor initialization sequence.

The second processor has to be prevented from accessing the table until the pointer has been updated by the first processor. Because most processors have a pause or halt input, this is most easily done in hardware. A flipflop or other element (possibly an output of another processor) can be used to hold each processor in the halt state until it is reset. When a processor has incremented the pointer, it enables the next processor, and so on. The enabling signal from the last processor starts the system, since at this time all processors have been initialized.

Differences in corrections applied to the data by the processors can be handled by the mailbox pointer and address array technique. Corrections are programmed as subroutines. The address table contains the address of the subroutine appropriate to the data channel handled by the processor, and the program common to all processors has a jump to the subroutine address in the table entry for the processor. These subroutines should be of the same length, however, to minimize execution time differences between microprocessors, and they can be filled out with no-ops or waiting loops if necessary.

An example

The shared bus, mailbox pointer-address table concept can be illustrated by a system, designed around four SC/MP processors, that acquires data from a sidescan sonar (SSS) system, removes distortion, and outputs the data to a hardcopy device. SSS is a system for obtaining acoustic images of the seafloor in oceanography. The surveying ship tows a fish containing a transducer that emits acoustic pulses in two fan-shaped beams on both sides of the fish. These beams are narrow in the direction parallel to the ship, and wide in the vertical direction. The acoustic echo at a given time after the pulse transmission consists only of reflection from a patch of the bottom determined by the width of the beam and the time interval. If the echo voltage is displayed on a raster scan device, an image of the seafloor is built up. These images are useful for distinguishing different types of seafloor sediment as well as locating undersea objects such as pipelines or wellheads.

SSS suffers from two types of distortion that limit its usefulness as a mapping technique. If the vertical rate of the raster scan does not correspond to the actual ship speed, anamorphic distortion is produced due to inequality of the horizontal and vertical scales of the image. The nonlinear relation of sound travel time to transverse distance from the fish (due to the fish's height off the bottom) produces a nonlinear horizontal scale if a raster scan device with a linear sweep is used. The first of these distortions can be eliminated by coupling a ship speed transducer to the paper drive of a raster scan display device, such as the Honeywell 1856A fiber optic recorder. The second distortion is more difficult to remove. The nonlinear sweep approach requires some fancy analog circuitry since the exact correction is a function of fish height above the bottom. Removal of this type of distortion can also be accomplished by sampling and storing the echo from a

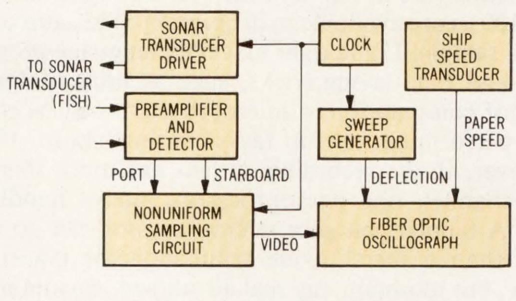


Fig 1 Sidescan sonar block diagram. Timing, sweep, and sampling functions are closely related. Four processors separately handle port and starboard acquisition or display subfunctions

pulse and then reconstructing the echo from the samples using nonuniform time intervals. If the reconstruction intervals are correctly chosen, the resulting display with a linear sweep will be undistorted. This technique is implemented by using multiple SC/MP microprocessors in a particularly elegant fashion.

Fig 1 shows the overall SSS recording system. The ship speed transducer controls the paper speed of the 1856A, and the timing circuit generates pulses that trigger the sonar transducer driver and synchronize the horizontal sweep generator and nonuniform sampling circuit. Echo returns are amplified by the preamplifier and pass through the nonuniform sampling circuit before controlling the intensity of the 1856A cathode ray tube (CRT) beam. The system described here is concerned with the timing, sweep, and nonuniform sampling circuits, which are intimately related.

A typical SSS operates with a pulse repetition rate of 5 Hz and a video bandwidth of 5 kHz. The Nyquist theorem requires a sampling rate of 10 kHz for this bandwidth; thus, 2000 samples must be stored to reproduce a pulse echo. Four buffers will be required: two (port and starboard) for storing the current echo, and two for the previous echo. Thus, if sampling is done by an 8-bit analog to digital converter (ADC), an 8k-byte buffer memory is required. An interrupt-terminated sampling loop for the SC/MP might be programmed:

```
Loop:  LD   ATOD       Get sample
       ST   @BUFF(P2)  Store it, auto-indexed
       LD   WCNT       Load wait count
       DLY  0          Delay
       J    LOOP       Repeat
```

This loop requires 78 microcycles, or 78 μs at a 1-MHz cycle rate. Thus, one SC/MP processor handles data acquisition or display for either port or starboard, and four handle the entire playback system. The architecture of the SC/MP makes it easy to interface four of them to both a common buffer memory and a common ROM containing the data acquisition and display code.

The chief problems occur during system start-up. The various SC/MPs must begin executing the proper program at the proper time and continue to do so. Also, it is desirable that the program for all the processors be identical so that only one program ROM is needed.

Fig 2 shows a system that solves these problems in a particularly simple fashion. When the run/stop switch is put in the run position, all NRST pins go high, but only

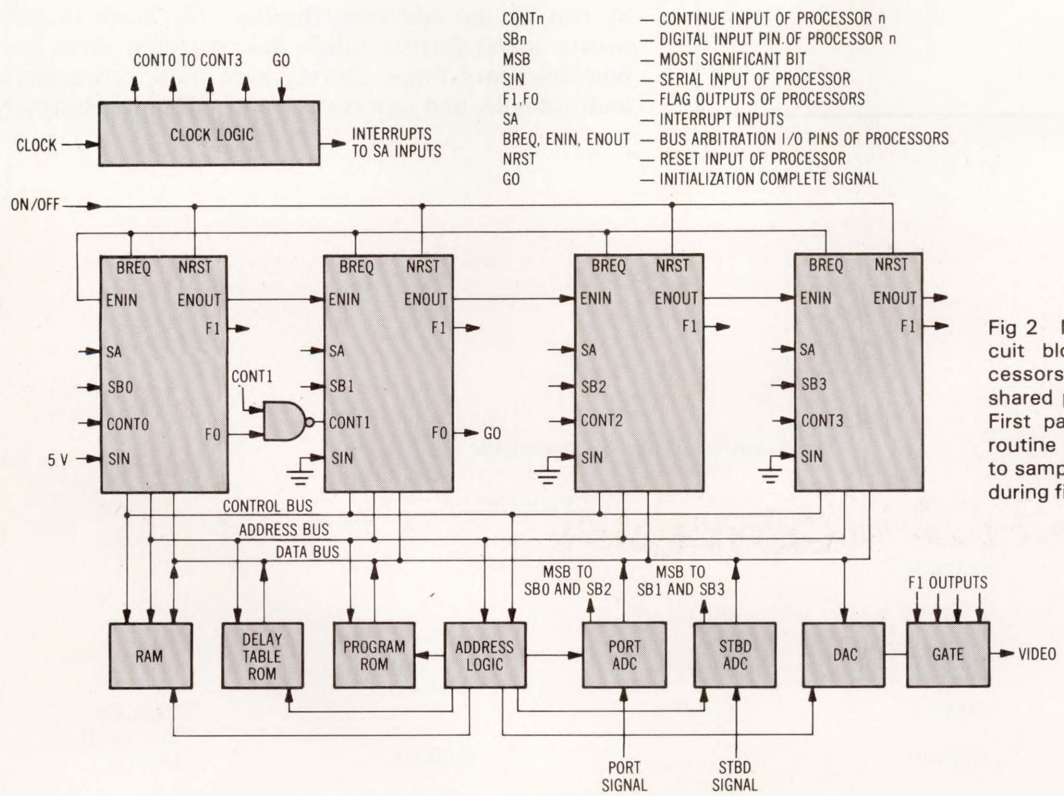


Fig 2 Nonuniform sampling circuit block diagram. Microprocessors must begin running shared program at correct time. First pair executes initialization routine in sequence and begins to sample. Second pair initializes during first data acquisition cycle

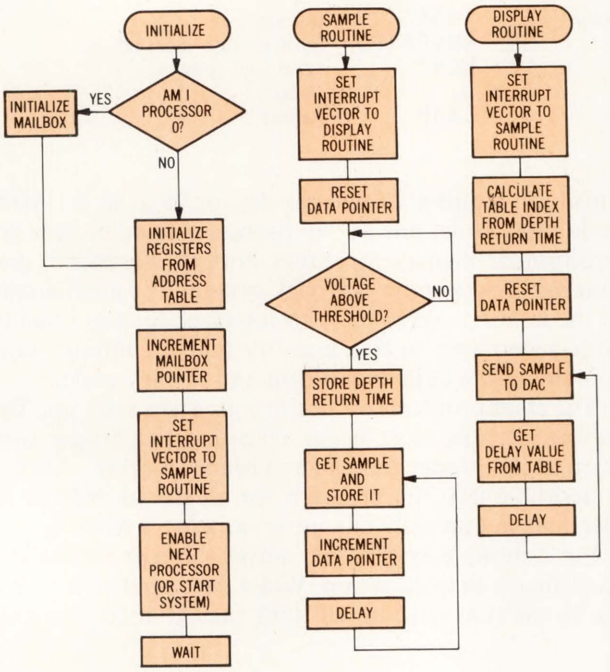


Fig 3 Flowchart of shared program. Initialize routine uses mailbox to initialize pointer registers and ends with waiting loop. External interrupts cause processors to alternately enter sample routine or display routine

processor 0 begins execution at 0001 because the CONT pins of all other processors are held high. Processor 0 executes an initialization routine. The SIN input is tested and, since it is high, processor 0 sets the mailbox pointer to its initial value. The mailbox pointer then loads internal register PC2 from the address table with the address of the first data buffer. The address of the input ADC is also obtained from the table. A trick is used here to save processor registers. The address in the table determines the highest address bit of the program counter (A_{15}); this bit is ignored by all hardware except the ADCs, allowing program counter relative addressing to be used to access the ADCs. One ROM address must be decoded, of course, and used to gate the ADCs onto the bus.

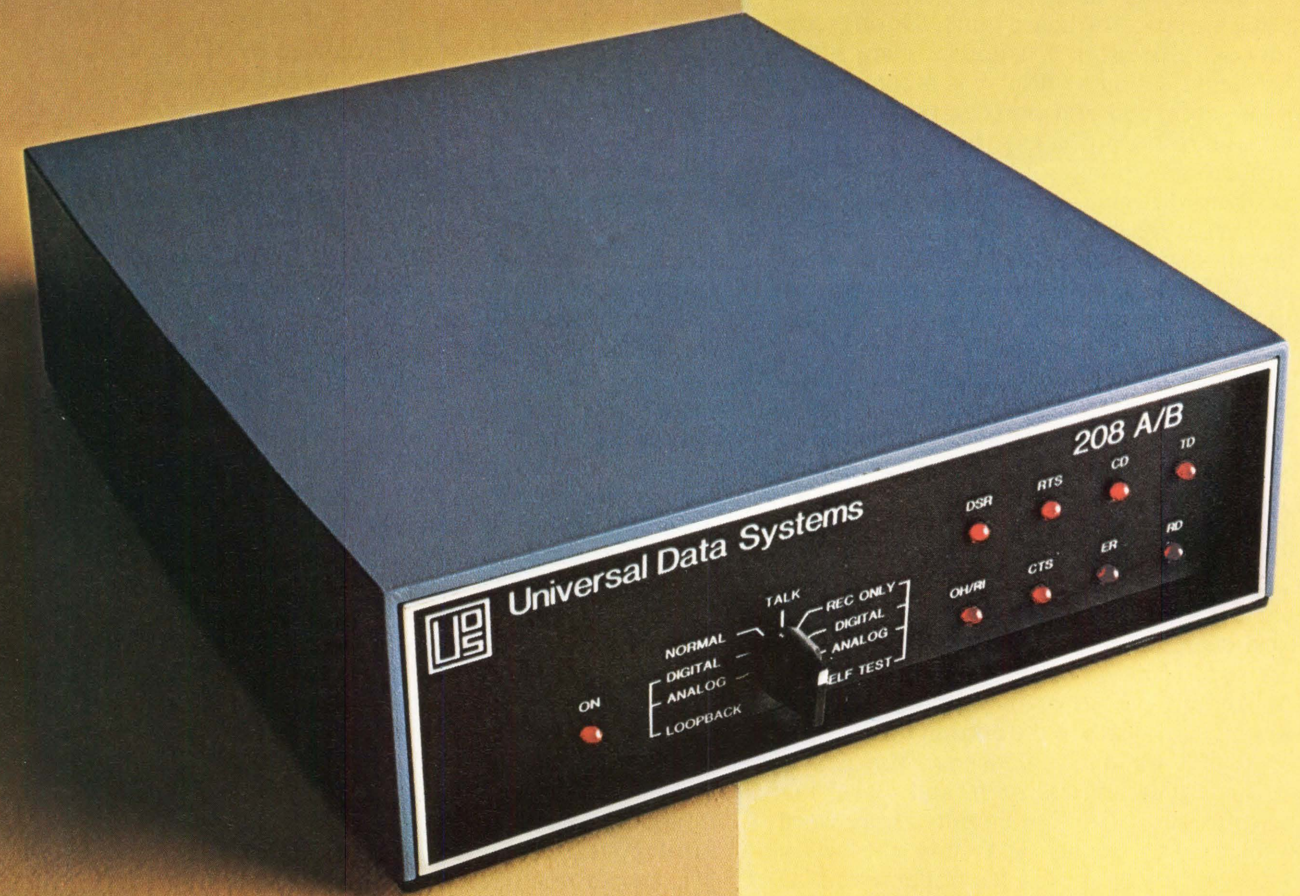
The next processor (SC/MP 1) is held off by the F2 output of the first processor until the mailbox pointer has been updated. The first processor then executes a waiting loop, and the second processor executes the same initialization program. Its SIN input is low, so it directs the mailbox pointer to initialize its registers. After its F2 output goes high, the system begins to sample. Processors 2 and 3 are held off by external hardware until sampling begins, at which time they initialize in sequence. The waiting loops that end the initialization program are exited in response to external interrupts. During initialization, PC3, the interrupt vector, is set to the address of the sampling routine. Fig 3 illustrates the initialization, sampling, and display routines.

At this point it is best to discuss the normal sequence of operations presented in the Table. Positive transitions of the clock drive the sonar transducer and the SA (interrupt) pins of the processors. The clock is divided by two by the odd/even flipflop. The clock (a 50% square wave) further subdivides odd/even times into port/starboard times. During even time, processors 0 and 1 sample, and processors 2 and 3 display. However,

Time Sequence of System Operations

Clock/Time	Processor 0	Processor 1	Processor 2	Processor 3
---RUN	INITIALIZE	-	-	-
	WAIT	INITIALIZE	-	-
↑ ODD PORT	SAMPLE	SAMPLE	DISPLAY (INITIALIZE*)	-
↓ ODD STBD	SAMPLE	SAMPLE	-	DISPLAY (INITIALIZE*)
↑ EVEN PORT	DISPLAY	-	SAMPLE	SAMPLE
↓ EVEN STBD	-	DISPLAY	SAMPLE	SAMPLE

*Processor initializes upon first turn on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processor 2 displays only during even/port time and processor 3 during even/starboard time. During odd time, the roles of processors 0, 1 and 2, 3 are interchanged. This time division of display is accomplished by gating of the even/odd and port/starboard signals onto the CONT pins of the processors. In response to the interrupt strobe, the processors execute response routines that, before beginning the appropriate task, change the interrupt vector to point to the response routine of the alternate task. Thus, the interrupt ping-pongs the processors in pairs between acquisition and display. During display mode, the processors in a pair alternate via gating of the CONT pin.

Following initialization, F2 of processor 1 goes high, and the next interrupt pulse starts processors 0 and 1 sampling. Instead of display, processors 2 and 3 execute the initialization routine in port and starboard times, continuing the mailbox pointer increment, pointer table access cycle. At the next interrupt, 0 and 1 begin display and 2 and 3 take up sampling.

The ADCs are tracking units based on the MC 1507 and MC 1508. They are assigned address 00FF and 80FF with port/starboard determined by A_{15}. Tracking ADCs permit the most significant bit (MSB) of the ADC to be monitored by output pin SB of the appropriate processor to determine the depth to the bottom (first strong return). The digital to analog converter (DAC) is a MC 1508 and is assigned address $80FF_{16}$ and $00FF_{16}$, but responds to writes only. The flag outputs F1 are ORed together to blank the display and reset the sweep generator. F1 is set early by the display response routine and reset just before beginning the actual display. The sign of the linear sweep is determined by the port/starboard signal.

Distortion is allowed for by monitoring SB for bottom return in the sampling response routine. A counter reflecting the time to bottom is maintained and stored in the internal processor E register before beginning actual sampling after SB goes high. The display response routine uses the E register to calculate the address to be used in the table ROM. The table ROM ignores bits A_0 to A_5, producing, conceptually, a display table that approximates the exact delays with a piece-wise linear function where each linear segment is 64 sample times long. Each echo is thus approximated by 32 segments. In playback, internal register P2 is used to point to the table ROM and is auto-indexed by 1 for each sample: the value read determines the delay in the loop and thus the time interval between samples.

The architecture of the processors combines with the mailbox pointer and address table technique to permit a simple implementation of the nonuniform sampling circuit basic to the SSS playback system. Common programs are used by all four processors in the circuit, and the shared bus system saves considerable hardware.

Conclusion

Using a mailbox to permit processors to share a bus in order to execute a common program has wide applicability, since it results in hardware saving while retaining the speed of a multiple-processor system. The SSS playback system, described here, performs functions similar to the other types of systems—such as tape recording and playback speed compression systems and audio signal delay systems—in which a time series of data is sampled, processed, and reconstructed at a later time.

A general layout that should prove useful in a variety of applications, this system is part of a dedicated instrument system and thus incorporates few options. A general purpose system can be implemented by using a master processor to receive control inputs and to dynamically generate programs containing the appropriate system sampling parameters. The generated program is stored in RAM and is executed by the slave processors. Once the code has been generated, the master processor relinquishes the bus and starts the first slave processor. The master processor then idles, waiting for an interrupt or manual input. In a system using a master processor to generate code for slave processors, the entire RAM is a mailbox, and the content of the mailbox is the program for the slave processors.

About the Author:

As a mathematician at the Marine Geology Laboratory of AOML/NOAA U.S. Department of Commerce, Thomas L. Clarke is responsible for the design and specification of oceanograhpic data acquisition and processing systems and is involved in the development of concepts leading to the capability to model transport of sediment in the ocean. He holds a BS in mathematics from Florida International University and an MS in applied mathematics from the University of Virginia.

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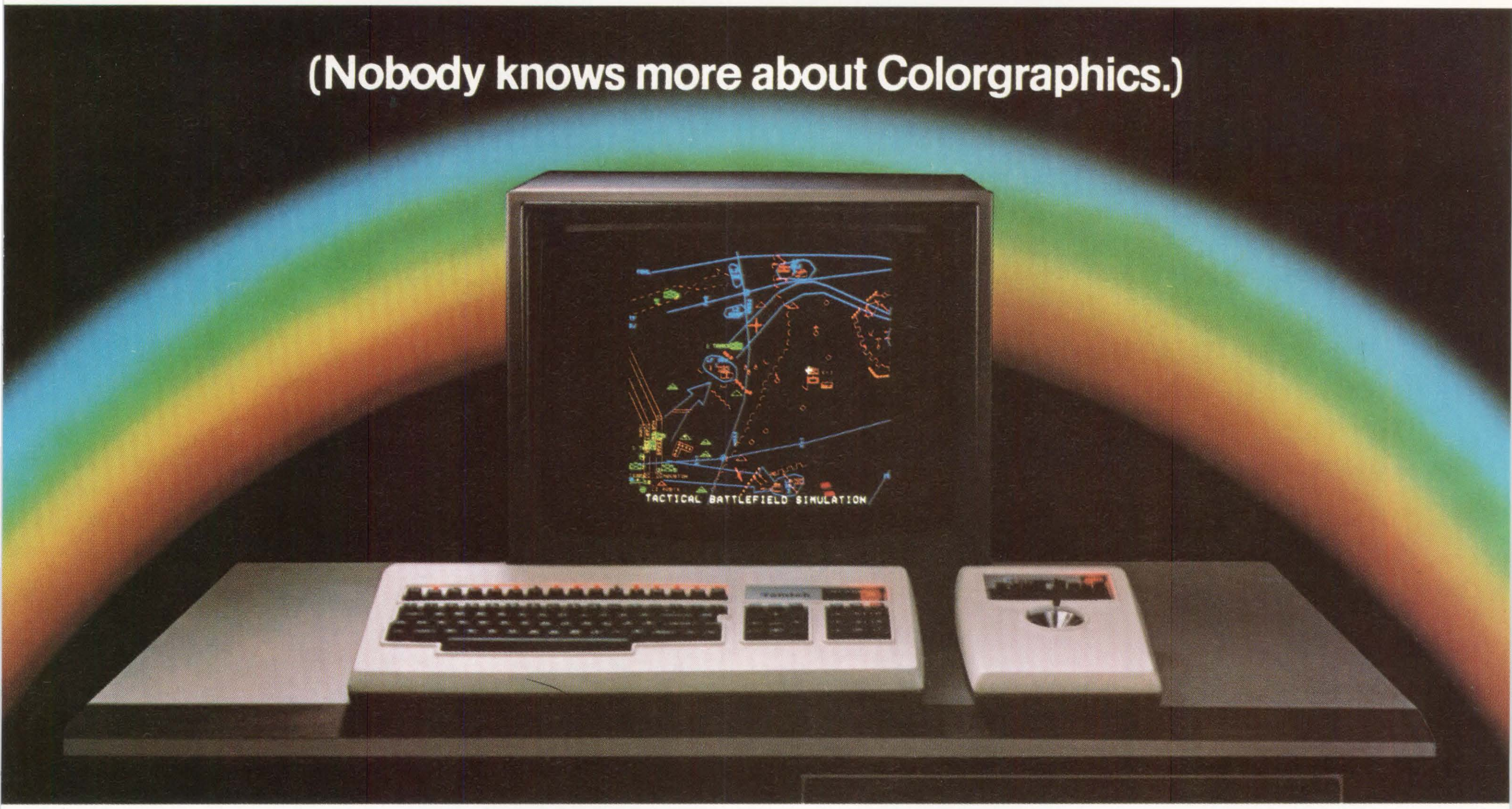

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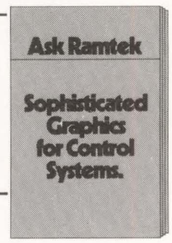

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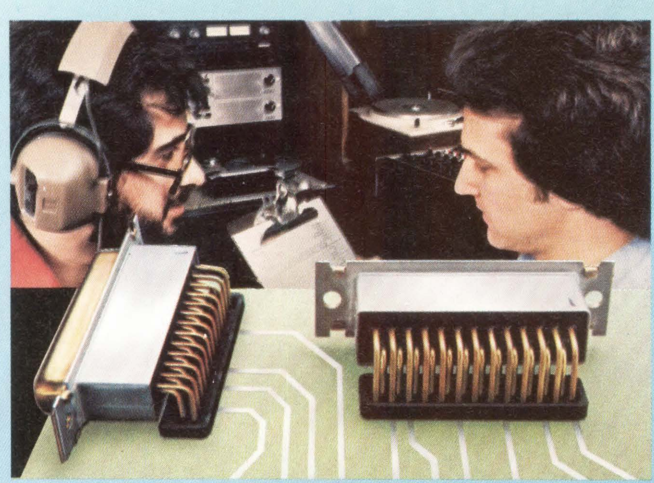

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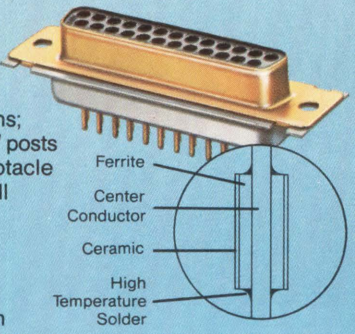

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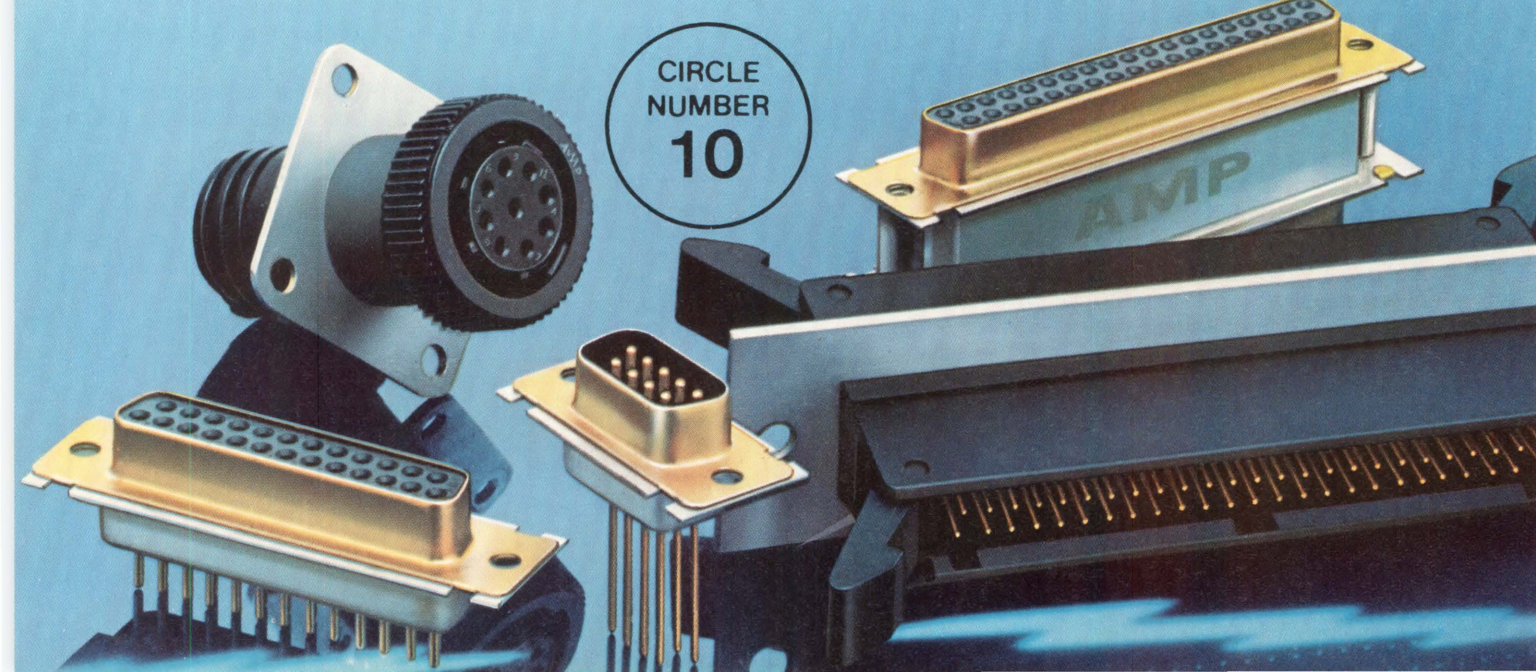

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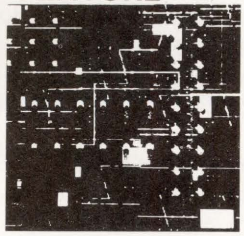


Capacitance-sensing faceplate replaces keyboard, making cathode ray tube a versatile input device

Touch-sensitive screens ensure a user friendly interface

Many designers today are using terminals with touch-sensitive screens to simplify the operation of data processing systems. Intended mostly for data retrieval, these terminals abandon the traditional keyboard in favor of touch-sensitive screens on which operators designate data to be retrieved and displayed on the system by touching an associated location on the terminal display.

The first touch-screen implementations were mechanical, such as a plastic overlay embedded with wire mesh. Later, to overcome the inaccuracy and unreliability of mechanical switches, solid state techniques that used banks of emitters and receptors were implemented. Solid state touch-screens flood the faceplate with beams of infrared light or high frequency sound; the breaking of a beam is interpreted as a "touch." In such schemes, relatively high resolution is possible [eg, 0.25" (0.64-cm) separation between beams], but the numerous active components result in higher cost and decreased reliability. The numerous active components produce a lower mean time between failure (MTBF), which results in associated maintenance and replacement costs.

Henry H. Ng
Steven J. Puchkoff
Interaction Systems, Inc
24 Munroe St, Newtonville, MA 02160

Capacitance-sensing technology has made possible a touch-sensitive display terminal with neither moving parts nor active components on the faceplate. A microprocessor recalibrates the faceplate continuously to eliminate susceptibility to capacitance changes caused by shifts in ambient conditions such as temperature, humidity, or dirt on the screen. The only limitation of capacitance-detecting touch screens is diminished resolution, because each capacitive touchpad must intersect a border of the screen.

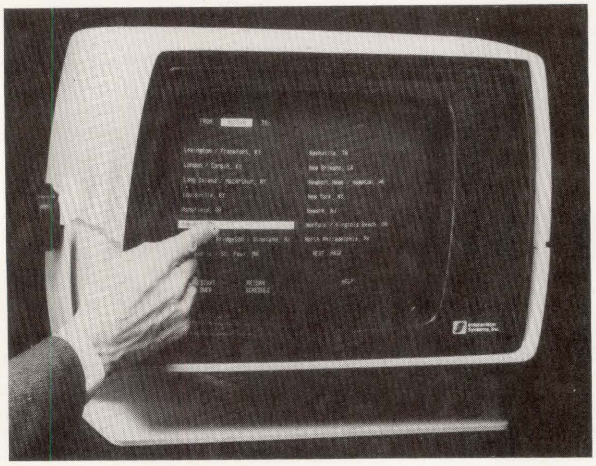
Keyboard entry display systems use special function keys and single-letter/number response keys—such as Y and N for "yes" and "no"—to reduce human error. Similarly, designers incorporate "menus" that list items and associate them with numbers or letters; operators select an appropriate key to respond to the displayed menu. Other special function systems incorporate push-button arrays directing operators to depress the push button associated with an item on the screen. Finite, hard coded function keys or push-button arrays do not provide the flexibility of touch-sensitive terminals. Further, touch-sensitive terminals do not require the transfer of eye and hand, as do keyboard systems. Both input and output occur on the screen. (See the photo.)

Finger-aiming accuracy varys widely among individuals and depends on many variables—eg, whether the person is sitting or standing, or close to or far from the screen. In view of such human operating factors, items presented on a touch-sensitive screen should occupy alternate lines, separated by about 0.5″ (1.3 cm) vertically and 1.0″ (2.54 cm) horizontally. Limiting the number of selection items exhibited on the screen at any one time is also helpful.

In very large search functions that are alphabetized or listed in numerical order, the designer must consider the number of items on the screen and the number of times a choice must be touched. It is more efficient to ask for two choices among ten items than it is to ask for one choice among twenty items. If the access program is structured into a hierarchy or pyramid sequence, then each screen menu or display should be one step on the pyramid. Experience indicates that it is better to use more screen display steps than to group multiple "branches" into one step.

When the operator touches a portion of the screen that does not contain a logical choice item, the system can respond to the touch or ignore it. Feedback indicating to the operator that the man/machine interface is functioning at each step of the interaction is effective reinforcement, although it is generally worthwhile to program the system to respond to an illogical selection only if the operator is not using the system continuously. Programmed responses to an illogical touch in a "public" system, where each use is isolated and transactions are relatively short, should convey only that the system is functioning. In such cases, the user might enter an illogical choice inadvertently by resting a hand on the screen or tapping fingers while thinking; or he may aim inaccurately and miss the desired item.

Acknowledgment of a touch can be registered visually by showing the item selected in reverse video,



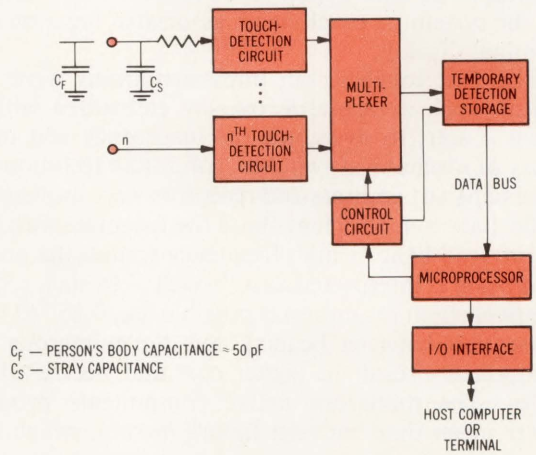
Touch-sensitive display terminal. Both input and output occur on screen; here, acknowledged touch is registered visually by highlighting item selected in reverse video. At bottom of display screen, HELP and RETURN commands provide assistance when needed, then call display back to point in transaction prior to request for help

Touch-Sensitive Display Terminal

The touch-screen has a transparent contact, or touchpad element, at each designated location. When the data processing system displays information, the operator directs the system by placing a finger on the screen at the location associated with the desired information. The touch-terminal then identifies which pad element at the screen location the operator selected and responds with the appropriate display of retrieved data. A totally passive medium, the touch-sensitive surface of the display does not employ mechanical contact techniques or acoustic emitters and receptors. Elimination of active elements makes the display highly reliable and maintenance-free. Software performs control, interpretation, decoding, and calibration.

A microprocessor controlled touch-detection circuit, located on the controller board, connects to conductive transparent pads on the display screen and continuously recalibrates the capacitive loading on the faceplate. Once it detects the signal that a person's touch conveys to any pad, it raises a READY status flag for the microprocessor. After all pads are scanned by the microprocessor, the error detection algorithm is applied. Finally, the touched pad is located and the signal transmitted to the terminal control electronics or directly to the host through a parallel or serial communication link.

Under software direction, the computer controlled touch-detection technique achieves an optimum balance between capacitive sensitivity and elimination of false touch signals. Intervals during which the human fingertip must be in continuous contact with the touch-sensitive position can vary in 15-ms increments. A continuous interval of 0.25 s in the software generally meets human expectations of response to the touch. Thus, false touch senses are eliminated and the frequency of touch-position inaccuracy becomes minimal.



Block diagram of capacitance-sensing faceplate. Microprocessor controlled touch-detection circuit recalibrates capacitive loading on faceplate once every 1000 μs (on moving average basis). In this way, unit compensates for fluctuating ambient conditions without registering false touches underlining, or changing intensity. Alternatively, a PLEASE REPEAT message can be issued without a change in the display screen. Audible feedback, such as a bell, can animate the interchange and indicate that the operation is proceeding normally. Touch-sensitive terminals are ideal for implementing a large number of simple commands. With each screen display, new commands that are appropriate for particular stages of the process can be invoked. Designers need to consider whether a command is a one-time event or a repeated event to determine whether an operator may still be touching the screen after the system has obeyed the command.

Many commands are likely to be repetitive. For instance, the operator may be searching data, browsing rapidly through a large file. In this case, it may be desirable to keep a finger on the screen to achieve continuous scrolling. A speedier technique for larger directories is to skip a certain number of entries, forwards or backwards, upon each command. Other commands, however, are likely to require only one response. In these cases, it is advantageous to shift the command location on the screen to an adjacent touch area after each command. Forcing the operator to move a finger slightly to repeat the command, this design feature is appropriate for such procedures as PRINT, NEXT PAGE, and PREVIOUS PAGE.

Conflicts in the "scrolling" function of touch-sensitive terminals can arise when the screen is also used for commands or function keys. In such cases, the programmer usually wishes to move (scroll) only the text portion of the screen, not the commands. Firmware can resolve this problem easily by creating a partial screen scroll mode that saves and rewrites the nonscrolling sections of the screen so that they appear not to move.

HELP and RETURN commands

Detailed HELP commands on the touch-sensitive terminal make computerized data retrieval possible for people who are unfamiliar with computer systems or equipment. Contents of the HELP messages depend on the stage in the transaction at which the operator requests assistance. At the start of the procedure, for example, HELP may explain the general goal and techniques of the transaction. At other points, HELP may clarify the meaning of the commands available at that point in the process.

When two or more pages reside in the terminal, the HELP command should be entered on a new, blank page. Since operators generally wish to resume their procedure on the display page at the point at which HELP was touched, a RETURN command should be displayed on the HELP page. This will call the display back to the page prior to the display of the HELP message.

A terminal recognizes a person's touch in approximately 100 ms. However, the computer system, of which the terminal is only one part, may have a much longer response time. Public transaction users unfamiliar with computer system response may not recognize the time lag factor, and think that their touch was not recognized. Continuing to touch the screen, they will inadvertently generate additional commands to the system. Designing the system to accept only one command at a time is one solution to this potential stacking problem. Thus, while responding to the first command, the system would not save or stack additional commands. Even though the computer, telecommunications system, and terminal all may be capable of full-duplex operation, experience shows that operating the touch system in this half-duplex mode is preferable for the man/machine interface.

Conclusion

Technology of touch-sensitive display terminals has evolved beyond the early mechanical overlays consisting of soft, wire-embedded material and solid state arrays of light emitting diodes and receptors. Today's terminals, designed with capacitance-sensing technology, are reliable, low cost devices—basically passive and maintenance-free. They make possible the economical implementation of "public access" systems, which will broaden the uses of computerized data significantly. Eventually touch-sensitive displays could evolve to voice-sensitive displays that can understand and respond to a limited vocabulary in normal human speech. Until that time, however, the touch-sensitive terminal will simplify access to a wide range of online computerized systems for a variety of operators—skilled and unskilled in computer technology.

About the Authors:

Henry H. Ng is vice president of engineering at Interaction Systems, Inc, where he directs the research, development, and engineering of touch-sensitive devices and other electronic components for terminal applications. He has been involved in R&D for the past eleven years. He has a BSEE from Lowell Technological Institute and an MSEE from Northeastern University.

Steven J. Puchkoff is vice president of marketing at Interaction Systems, Inc, where he is involved in the integration of public access terminals into a wide variety of applications. He has a BSEE from City College of New York and an MBA from Boston University.

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Efficient use of low power WAIT mode requires a careful choice of CMOS microprocessor clock rate

Choosing optimal microprocessor clock frequency minimizes power consumption

Naveen J. Tangri **Department of Electrical Engineering**
University of Florida, Gainesville, FL 32611

Complementary metal oxide semiconductor microcomputer systems are being used increasingly in applications where power consumption must be reduced to an absolute minimum. Such applications include realtime digital control, data acquisition, and signal processing. Although the processing speeds of the microprocessors for these microcomputer systems are lower than those of P- or N-channel metal oxide semiconductor or bipolar microprocessors, a complementary metal oxide semiconductor microcomputer is selected for a specific application mainly because it consumes little power. This factor can be critical in portable battery-powered systems or in remote solar-powered stations.

To increase the energy efficiency of complementary metal oxide semiconductor (CMOS) microprocessors, many designs provide for a software- or hardware-controlled WAIT or HALT mode in addition to the full-power operating mode. In the WAIT state, a microprocessor's power consumption is usually an order of magnitude smaller than when it is fully operational. However, because average power consumption is proportional to clock frequency in both the WAIT and full-power modes, the choice of clock frequency is crucial in determining a microprocessor's average power consumption.

It is possible to analyze the power consumption behavior of a CMOS microprocessor in a typical realtime signal processing application. This analysis, in turn, can be used to determine how to minimize power consumption.

Typical application

Fig 1 shows a typical application in which a CMOS microprocessor is used for realtime signal processing or control. Most such low power systems are fabricated of CMOS components throughout. A number of analog signal channels are sampled from the target system at a certain frequency. This sampling frequency is entirely dependent on the frequency content of the signals sampled and the signal processing to be performed by the microprocessor. It is assumed here that the sampling frequency is fixed by considerations other than minimum power consumption.

After an analog signal channel has been sampled, analog to digital conversion is performed, and the

(continued on page 140)

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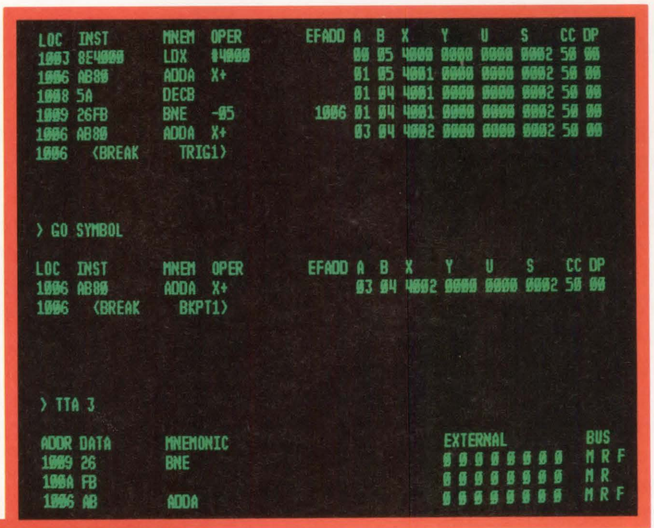

(top) Trace All display gives disassembled prototype code plus the status of all key processor registers on a step-by-step basis.

(middle) Symbolic debugging allows all major address locations to be defined as easily read mnemonics. Breakpoint information includes full display of processor status.

(bottom) Trigger Trace display shows real-time bus activity on a cycle-by-cycle basis plus eight channels of hardware logic defined by the user.

6809 Prototype Control Probe tip fits easily in hard to reach locations. Probe status lights monitor key processor signals.

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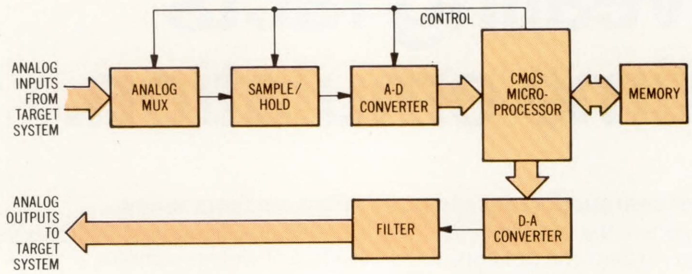

Fig 1 Typical CMOS microprocessor application. Realtime signal processing is performed on one or more analog channels. Although sampling frequency is governed by system application constraints, microprocessor's clock frequency can usually be chosen with considerable degree of freedom

digital representation of signal amplitude is presented to the microprocessor. For each signal sample, a certain amount of realtime signal processing is performed, depending on the specific application. This processing has to be completed before the next sampling instant. Usually, all the necessary processing for a sample is completed well before the next sample arrives, and the microprocessor enters a WAIT state in the meantime to conserve power.

Most manufacturers supply power consumption characteristics for their microprocessors as a function of clock frequency. Fig 2 shows the power dissipation curves for the RCA CDP1802. As can be seen, power consumption increases logarithmically with clock frequency. This occurs because most power consumed by a CMOS microprocessor is dissipated indirectly in charging and discharging gate capacitances through CMOS transistors, instead of directly as joule heat in circuit resistances.

How, then, should the clock frequency of a microprocessor be chosen? At one extreme, the microprocessor could be run at the minimum permissible clock frequency. In this case, it would be fully operational during the time between sampling instants in order to complete the necessary processing before the arrival of the next sample. Ideally, it would never have time to go into a WAIT state, and so would consume full operating power at all times. At the other extreme, the microprocessor could be run at the maximum permissible clock frequency. In this case, the signal processing would be completed in the minimum possible time. Once the necessary processing is completed, the microprocessor could go into a power-conserving WAIT state until the arrival of the next sample. However, since the power consumption of a microprocessor increases logarithmically with clock frequency, this extreme case is not necessarily the most energy-efficient.

Thus, there is a choice (or maybe, choices) of clock frequency low enough for the microprocessor to consume moderate amounts of power while processing, and yet high enough for it to complete all the necessary processing quickly and go into a power-conserving WAIT state for the remainder of the sampling interval.

Analysis of power consumption

A hypothetical graph of a CMOS microprocessor's power consumption vs time for a typical case. is shown in Fig 3. After each sampling instant, the microprocessor *(continued on page 142)*

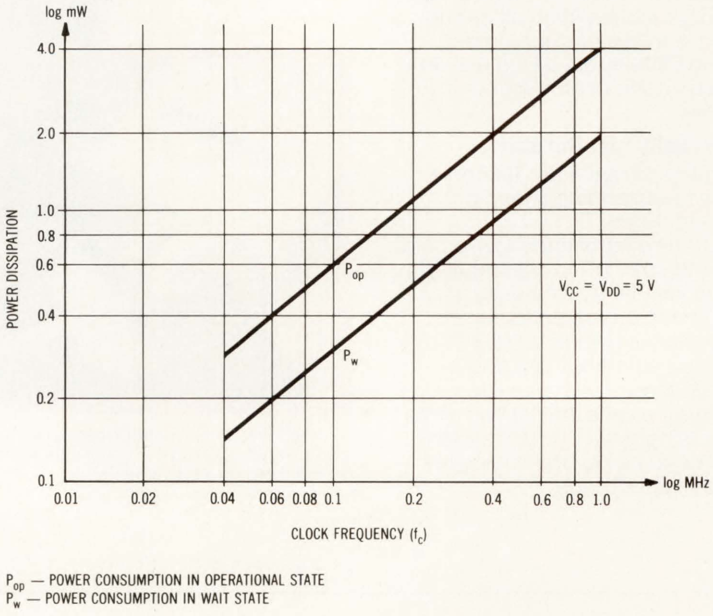

Fig 2 Power dissipation curves for microprocessor. Curves plotted as function of clock frequency for RCA CDP1802 show how power consumption increases logarithmically with clock frequency

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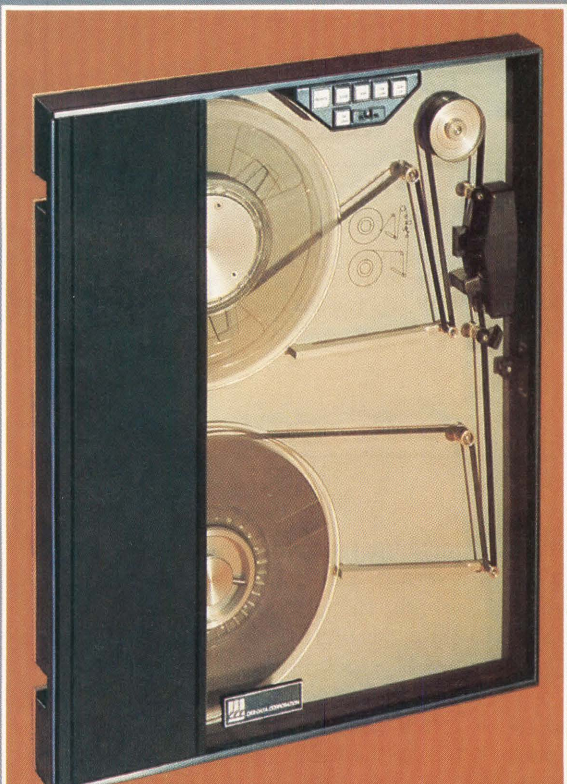

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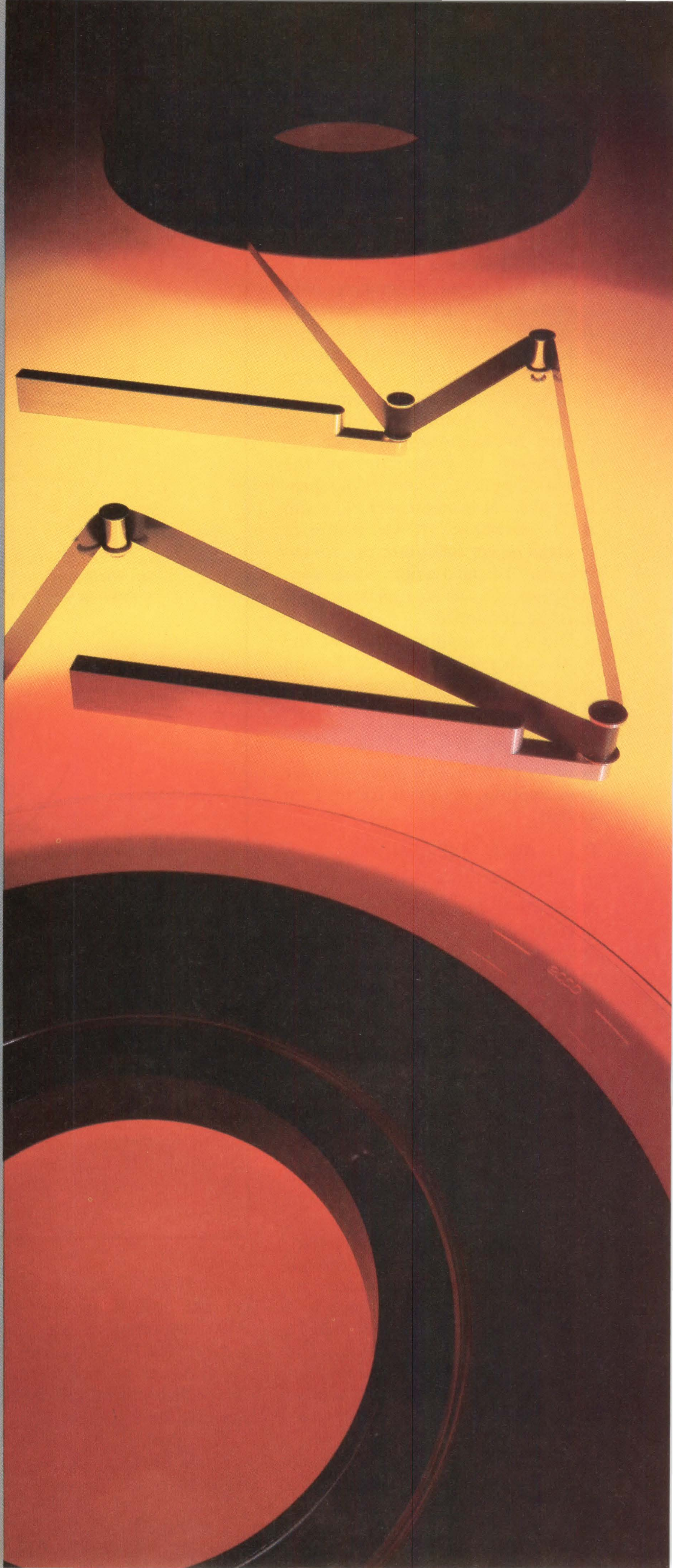

performs a certain amount of processing with power consumption P_{op} for a time Δt. When this processing is completed, it goes into a WAIT state, with power consumption P_w, for the remainder of the sampling interval T_s. As mentioned earlier, T_s is assumed to be a constant, determined by signal processing constraints and not by power consumption considerations.

Let f_c be the microprocessor's clock frequency, and let N be the number of clock cycles required to perform the necessary signal processing for each sample. Since this processing is dependent on the specific application and is independent of f_c, N is a constant. The aim is to determine f_c to minimize average power consumption. An expression for the average power consumption P_{av} as a function of f_c must be developed.

During a sampling interval, the total energy ΔE consumed by the microprocessor is the shaded area in Fig 3. Thus,

$$\Delta E = P_{op}\Delta t + (T_S - \Delta t)P_W$$

In order to determine average power consumption, we divide ΔE by T_s to obtain

$$P_{av} = \Delta E/T_S = [P_{op}\,\Delta t + (T_S - \Delta t)P_W]/T_S$$

Now, Δt is the time spent by the microprocessor, operating at a clock frequency f_c, to execute N clock cycles. Thus $\Delta t = N/f_c$. Substituting this in the expression for P_{av} yields

$$P_{av}(f_C) = [P_{op}N/f_C + (T_S - N/f_C)P_W]/T_S$$

in which N and T_s are constants, depending on the application. P_{op} and P_w are functions of f_c. $P_{op}(f_c)$ and $P_w(f_c)$ can be gleaned from manufacturer's data sheets, or can be determined by simple experiment.

In order to determine optimal f_c, $P_{av}(f_c)$ must be minimized. Although $P_{av}(f_c)$ can be minimized by numerical techniques, perhaps it is easiest to plot P_{av} as a function of f_c, for a feasible range of f_c. The minimum P_{av} and the optimal f_c can then be determined graphically. Using the power consumption characteristics of the MC146805E2 microprocessor, and assuming N = 200 clock cycles and T_s = 2000 μs for a typical application, a short FORTRAN program was written to generate the P_{av} vs f_c curve shown in Fig 4. As can be seen, the optimal f_c can be determined quite easily by inspecting the $P_{av}(f_c)$ plot.

This analysis can also be used to evaluate different signal processing techniques to determine which technique would consume the least average power. Suppose, for example, that a choice exists between using zero-crossing analysis requiring N_z clock cycles and peak detection requiring N_p clock cycles. Different curves for $P_{av}(f_c)$ can be plotted on the same axes for $N = N_z$ and

(continued on page 144)

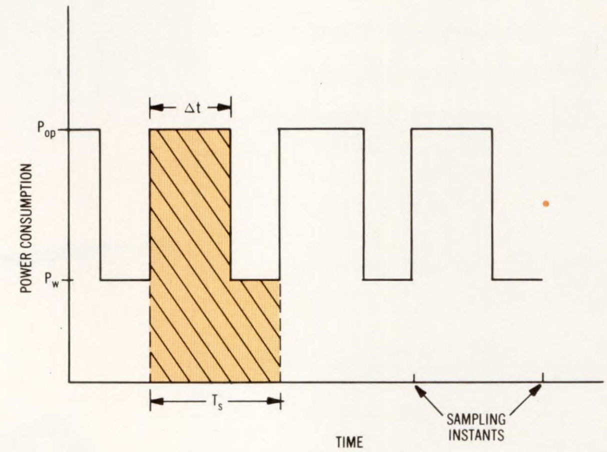

Fig 3 Plot of power consumption vs time. Typical signal processing application is for microprocessor incorporating power-conserving WAIT state in addition to full-power processing mode

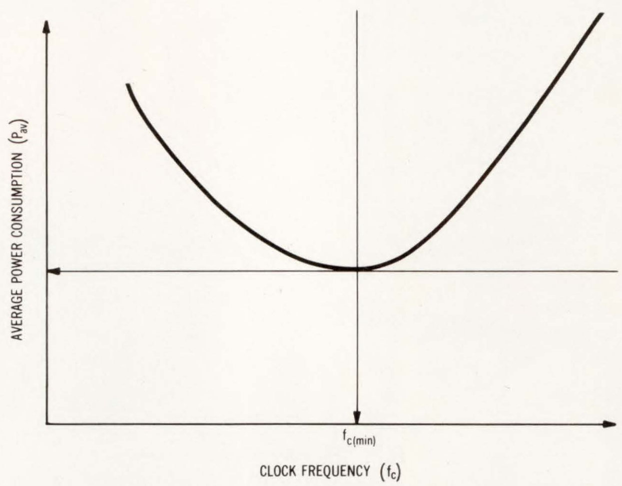

Fig 4 Average power consumption vs clock frequency. Computer generated plot for microprocessor shows typical realtime signal processing application in which $f_{c(min)}$ is clock frequency that requires minimum average power

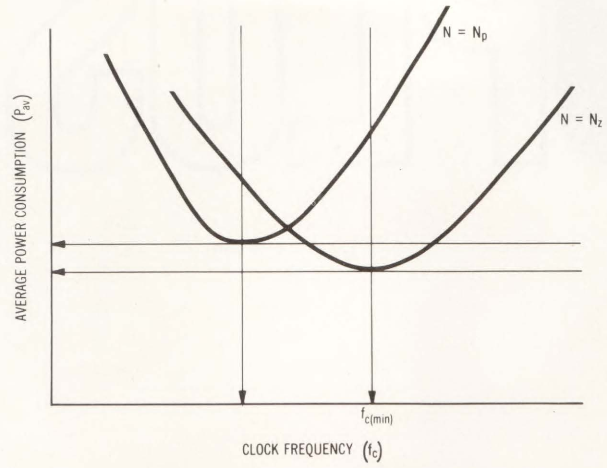

Fig 5 Power consumption for different techniques. By plotting average power consumption curves as functions of clock frequency on same axes, signal processing technique that requires minimum average power can be identified

$N = N_p$, as shown in Fig 5. A simple inspection of the curves will determine not only the most energy-efficient signal processing technique but the optimal clock frequency as well.

Summary

CMOS microcomputer systems are widely used in applications where power consumption must be reduced to a minimum. Most CMOS microprocessors therefore incorporate a power-conserving WAIT or HALT mode. However, because the average power consumption of a microprocessor is proportional to its clock frequency, the choice of clock frequency is crucial. The mathematical analysis presented here offers a simple technique for determining a microprocessor's optimal clock frequency that minimizes average power consumption. Although this technique was applied to a CMOS microprocessor, it holds good for any microprocessor that has a power-conserving WAIT state in addition to its full-power operating mode.

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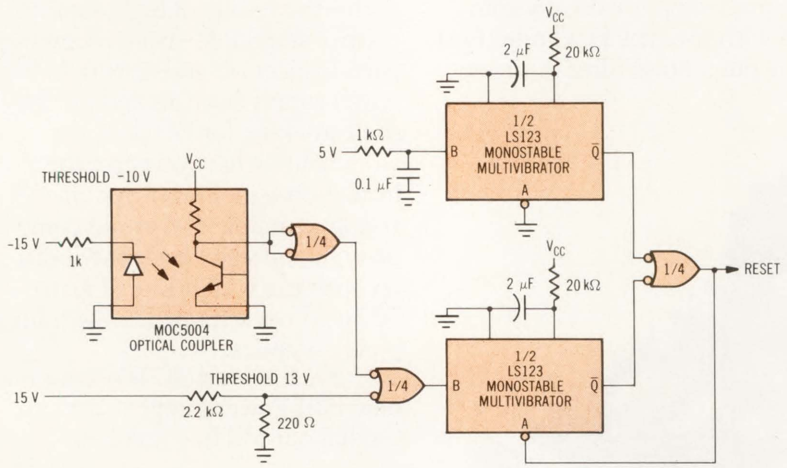

The digital power supply monitor/reset generator circuit checks one negative voltage and two positive voltage power supplies, generating a reset signal for low voltage inputs. Only three integrated circuits and a few discrete components are required for the configuration.

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When the delayed 5-V supply becomes valid, a monostable multivibrator (1-shot) is triggered and the reset signal is generated. (See the Figure.) If at the end of the 1-shot pulse both the 15-V and −15-V supplies are not above their thresholds, the second 1-shot is triggered and the reset signal is held active. Until the 15-V and −15-V supplies are above threshold, the second 1-shot continuously re-triggers at the trailing edge of its own output pulse. Once all power supplies are at valid levels, a drop below threshold either in the 15-V or in the −15-V supply causes the 1-shot to be triggered. It continues to re-trigger until both supplies are at valid levels.

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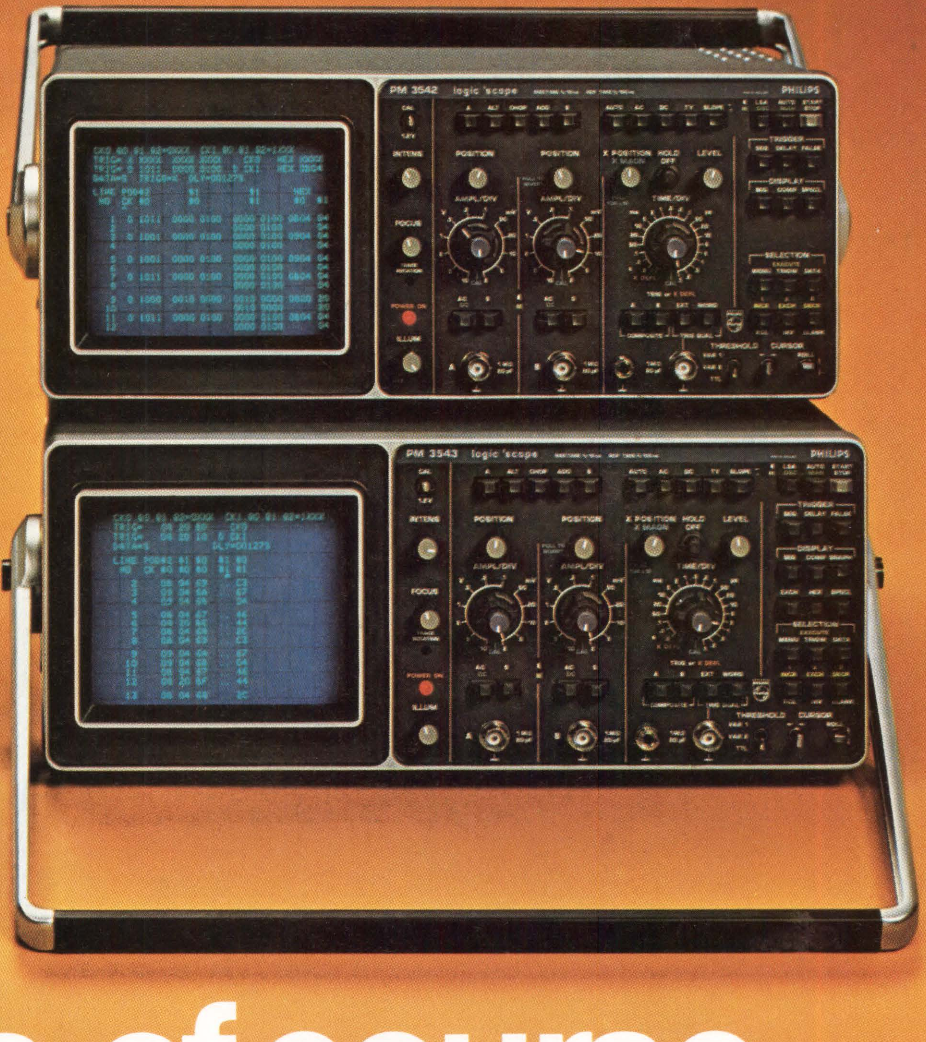

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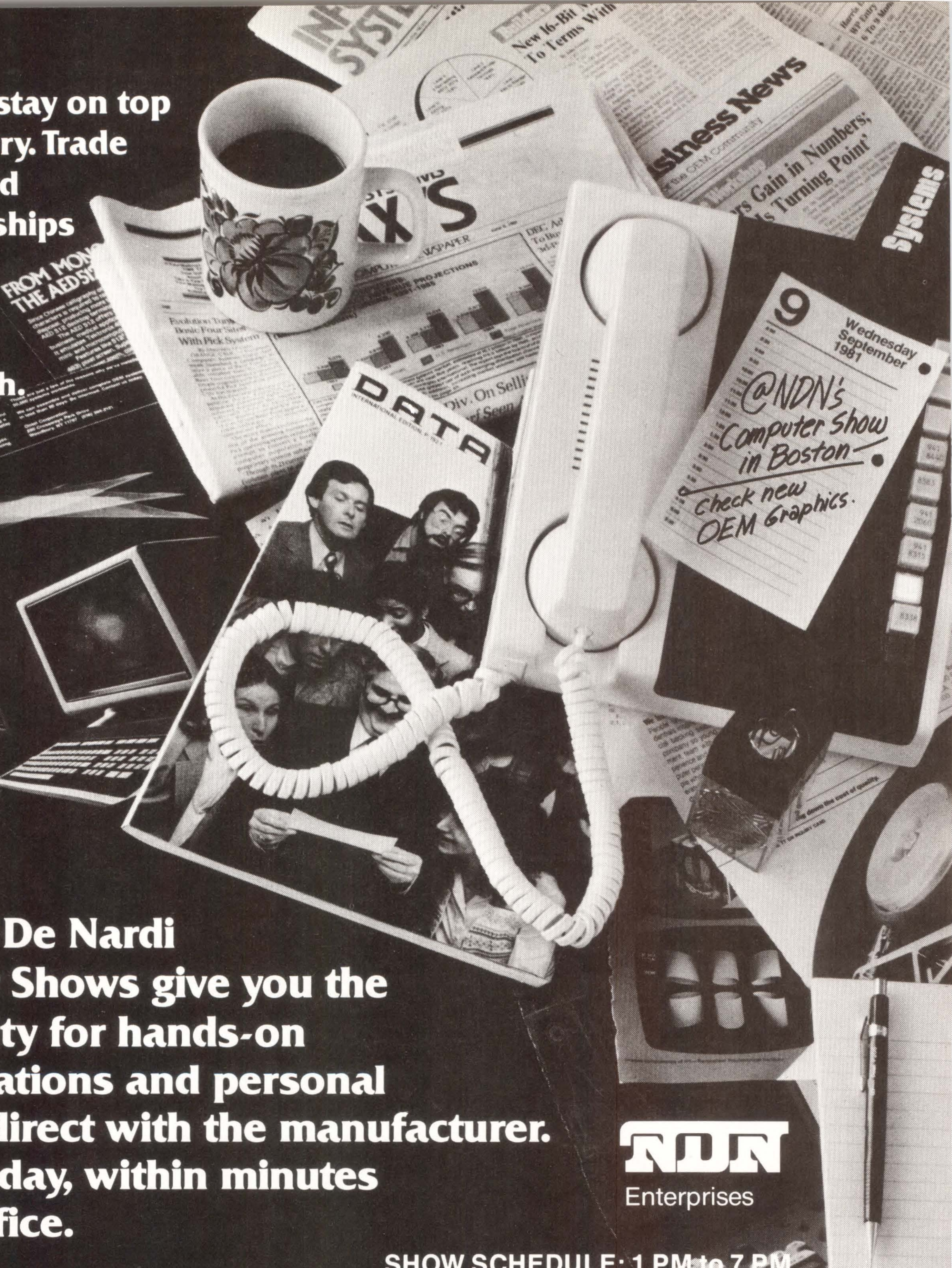

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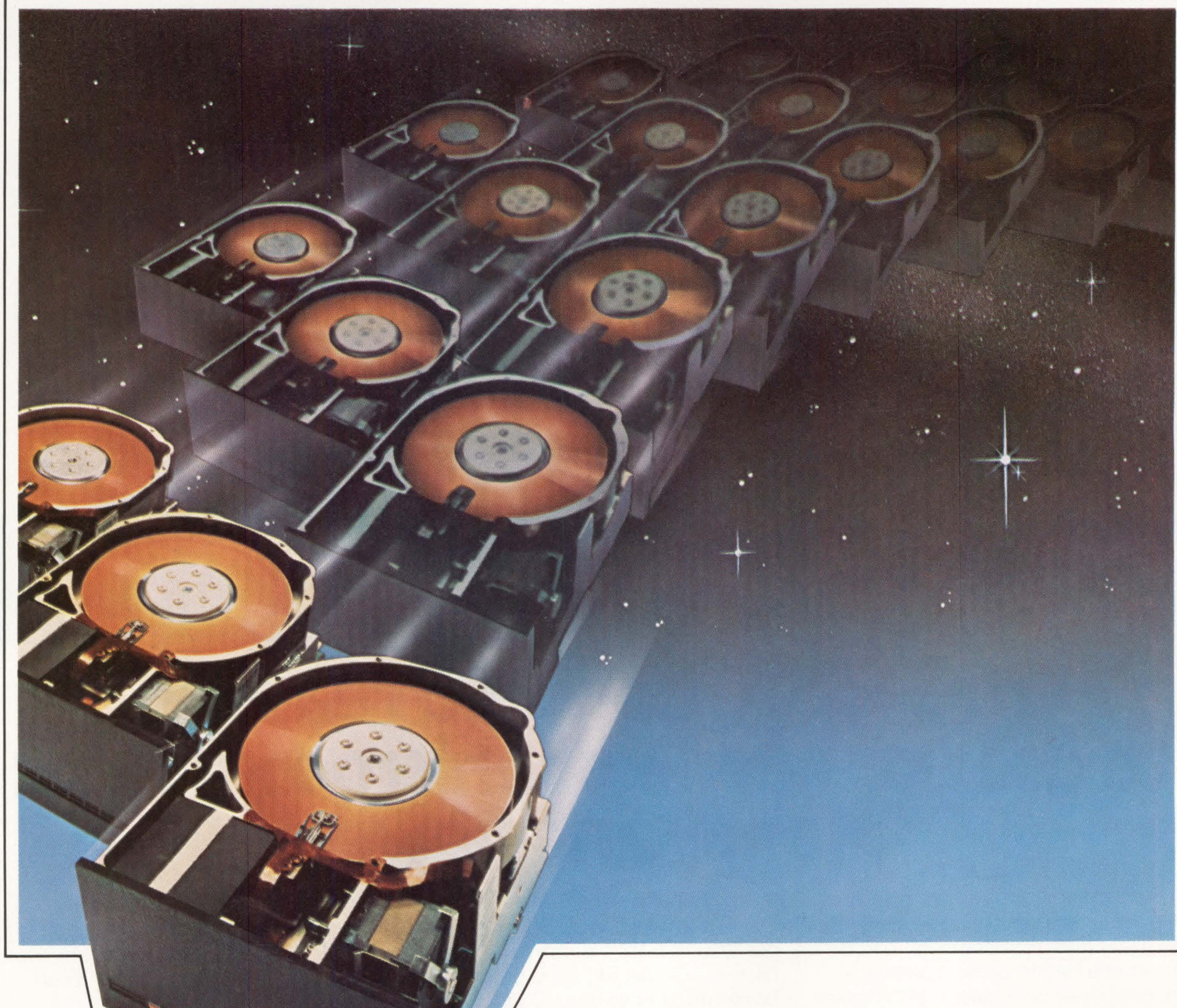

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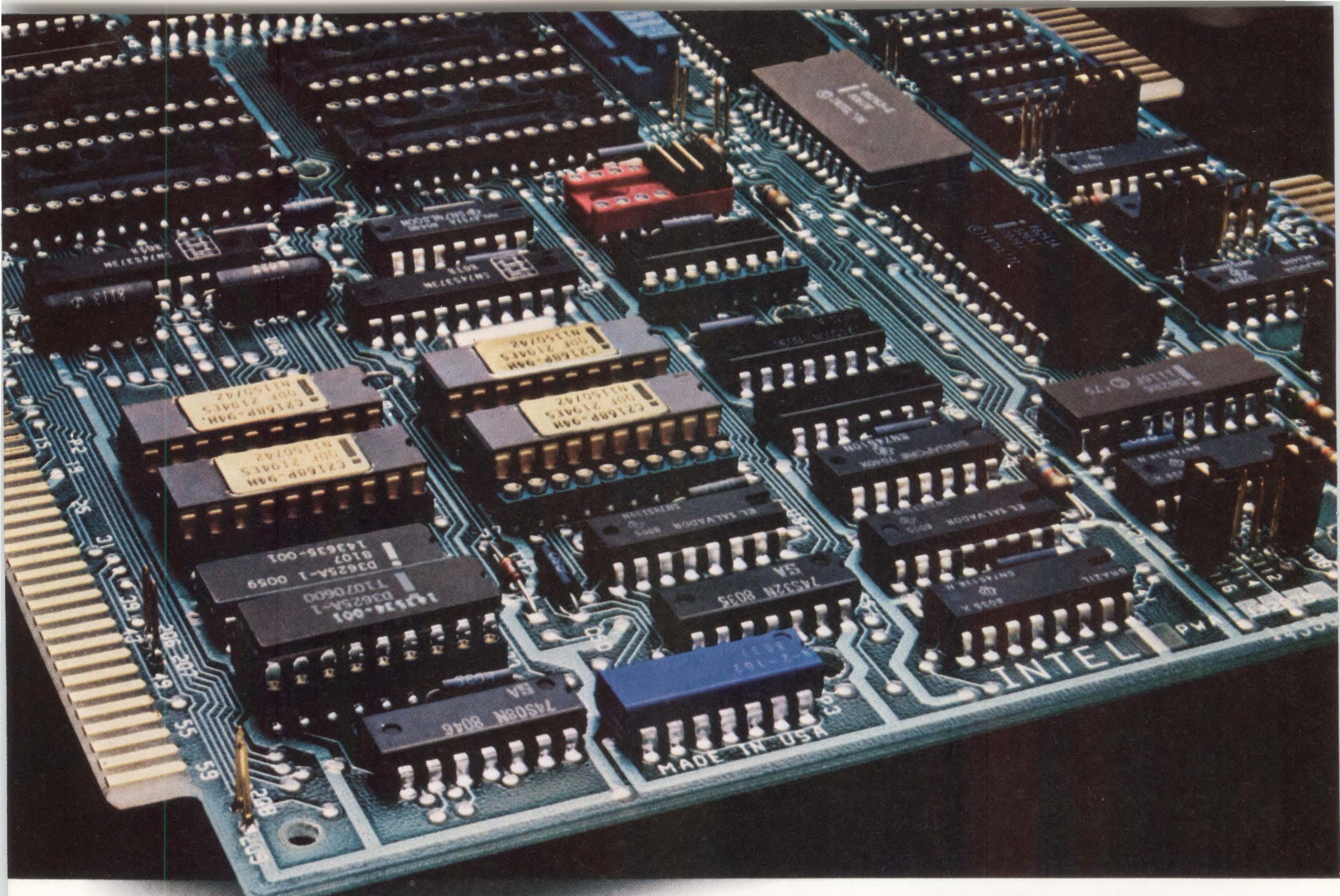

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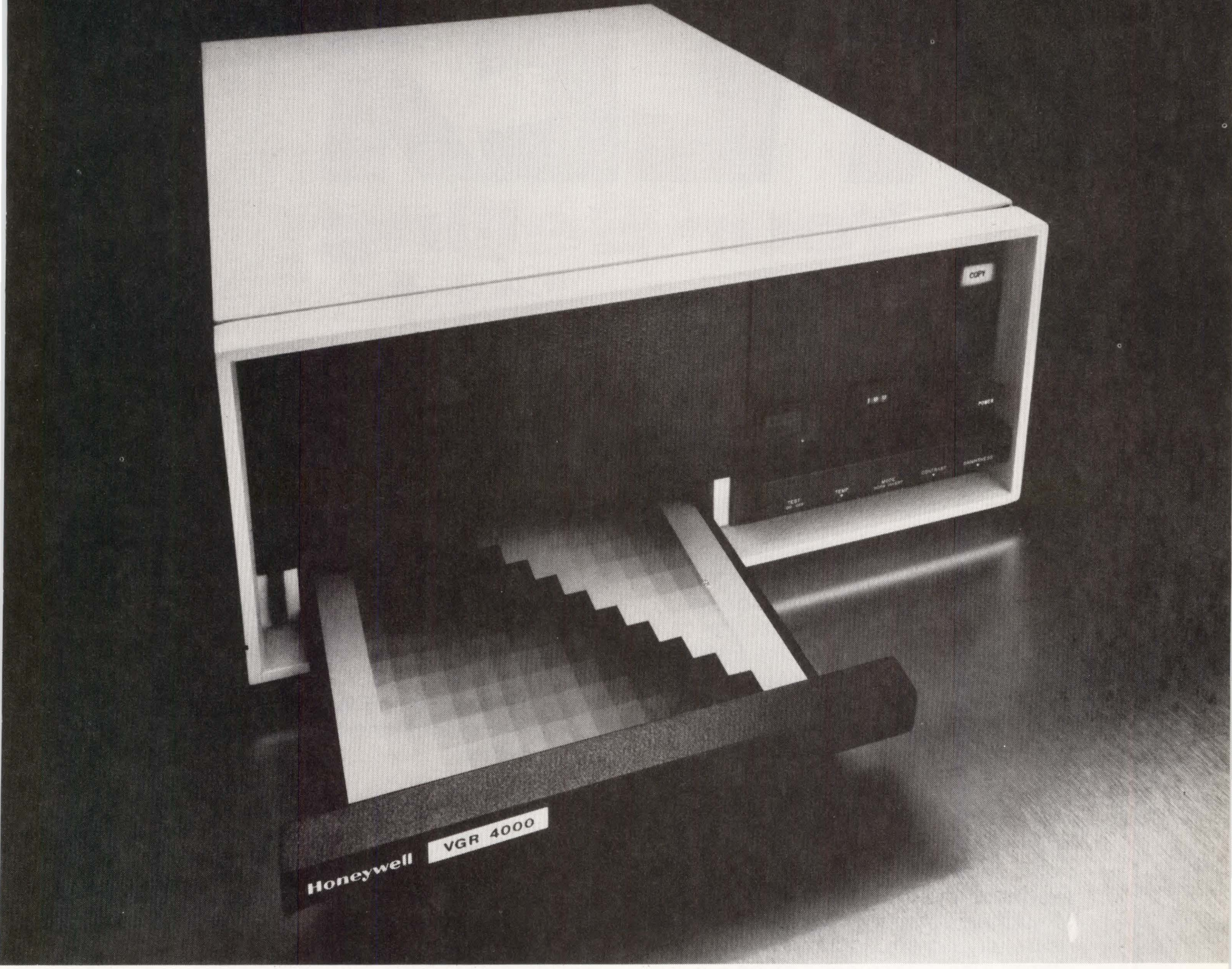

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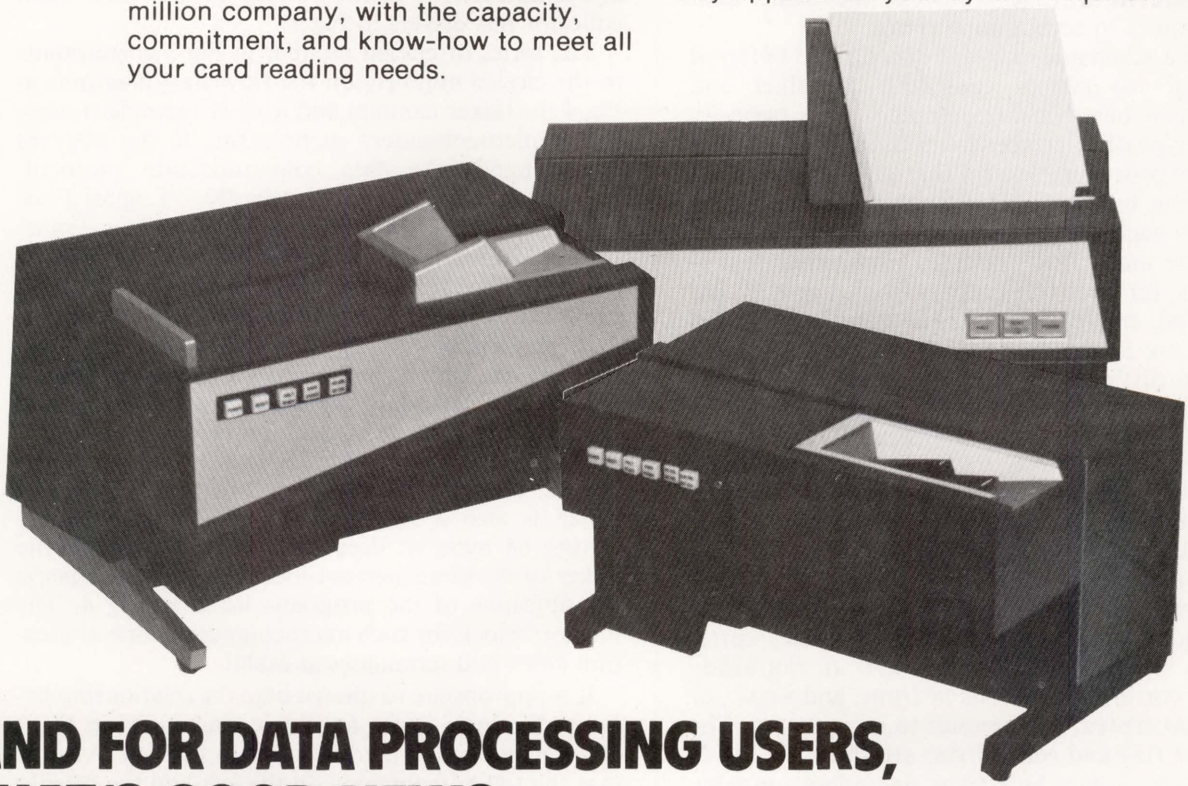

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Interfacing Fundamentals: 3-Wire Handshake Using Two Microcomputers

Peter R. Rony

Department of Chemical Engineering
Virginia Polytechnic Institute and State University
Blacksburg, VA 24061

The relationship between the flowcharts[1-3] and timing diagrams[1,2] for the IEEE 488 *3-wire handshake protocol* can be experimentally demonstrated using two or more microcomputers that are interfaced to each other via the use of 8255 programmable peripheral chips and IEEE 488 bus transceivers or their equivalents. The 3-wire handshake is used for byte-serial data communication applications in which one output port at a time transfers the same data simultaneously to several input ports.

Fig 1 is a schematic diagram of a double-buffered conditional I/O system consisting of talker and listener 8080A based microcomputers. It is basically the same type of interface circuit used for the 2-wire handshake procedure[4] except that (a) there are three handshaking bus lines between the two microcomputers, (b) each bus line permits additional connections to be made, for example, from other microcomputers, (c) three flag outputs from each 8255 chip are required, and (d) three bus line status inputs from each 8255 are also required. As a substitute for the somewhat difficult to obtain IEEE 488 bus transceivers, 74LS05 open-collector bus drivers are employed. Each bus line is pulled up to 5 V with a 3-kΩ resistor and down to ground with a 6.2-kΩ resistor; these are the values recommended by the IEEE Standard 488-1978.[1] A 74LS04 chip inverts the bus signal back to positive logic before it enters an input port bit on each 8255 chip.

The three IEEE 488 handshake lines are called DAV, NRFD, and NDAC. DAV, or Data AVailable, corresponds to bits PC0/PB0 in Fig 1; NRFD, or Not Ready For Data, corresponds to bits PC1/PB1; and NDAC, or Not Data ACcepted, corresponds to bits PC2/PB2. The handshake flag and status bytes are shown in Fig 2.

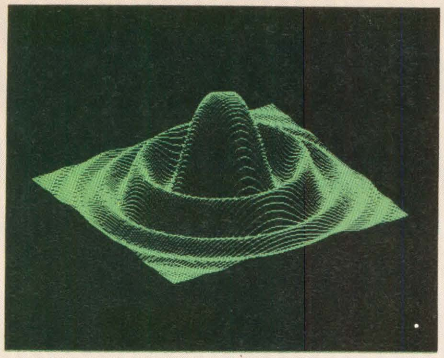
To transfer a data byte from one microcomputer to the other, not all of the flag bits (PC0, PC1, and PC2) or bus line status input bits (PB0, PB1, and PB2) are used on a given 8255 chip. For example, assume that the microcomputer on the left in Fig 1 is the talker, and the one on the right the listener. The talker outputs the DAV flag and inputs the status of the NRFD and NDAC bus lines. Thus, the microcomputer on the left outputs bit PC0 (DAV) and inputs/tests bits PB1 (NRFD) and PB2 (NDAC). The listener outputs NRFD to bit PC1, NDAC to bit PC2, and inputs/tests bit PB0 (DAV). Now assume that the direction of data transfer is reversed, with the microcomputer on the right talking to the listener on the left. This time, the microcomputer on the right outputs bit PC0 and tests bits PB1 and PB2, whereas the microcomputer on the left outputs bits PC1 and PC2 and tests bit PB0. Data transfer can be in only one direction at a time. The use of such bused flags[5] permits bidirectional data transfer between any number of devices that are tied to data lines PA0 to PA7 and to the DAV, NRFD, and NDAC bus lines shown in Fig 1.

Fig 3 is the same as Fig 4 in reference 5, only now a series of circled numbers is assigned to important points on the timing diagrams for the seven signals given. Shown are the data bus DIO1 to DIO8, which corresponds to data lines PA0 to PA7 in Fig 1; the DAV flag (bits PB0 and PC0 in Fig 1); the NRFD flag (bits PB1 and PC1); the NDAC flag (bits PB2 and PC2); and the DAV, NRFD, and NDAC bus lines, which are located at the intersection of the outputs of the 74LS05 open collector bus drivers in Fig 1.

The series of circled number in Fig 3 corresponds to the circled numbers on the flowchart diagrams in Fig 4 for talker (source) and listener (acceptor) 8080A based microcomputers participating in the IEEE 488 3-wire handshake data communication protocol. Fig 4 corresponds directly to Fig B2, "Logical Flow of Events for Source and Acceptor When Transferring Data Using Handshake Process," on p 70 of the IEEE Standard 488-1978. Except for the consolidation of series process blocks, every process block or decision symbol in Fig 4 has a one-to-one correspondence with a similar block or decision symbol in Fig B2. The only difference between the two figures is the series of circled numbers used: in Fig 4, the numbers correspond to those in Fig 3, whereas in Fig B2, the numbers correspond to those in Fig B1, which is also a series of timing diagrams. Transferring 64 bytes of data from the memory of the talker to the same memory locations in the listener is the objective of the programs listed in Fig 4. The memory block for each microcomputer starts at location 0380H and terminates at 03BFH.

It is appropriate to discuss here the relationship between the logic states and logic transitions in Fig 3 and the microcomputer instructions in Fig 4. Assume that the talker (source) is on the left and the listener (acceptor) is on the right in Fig 1. In Fig 4, the flowchart for the talker is on the left, and that for the listener is on the right. By location 1 both the talker and listener microcomputers have been initialized.

(continued on page 156)



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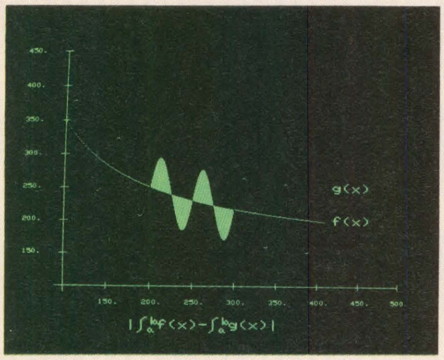

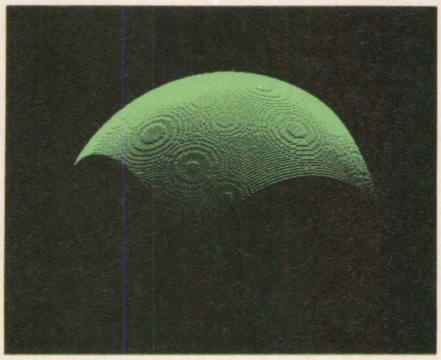

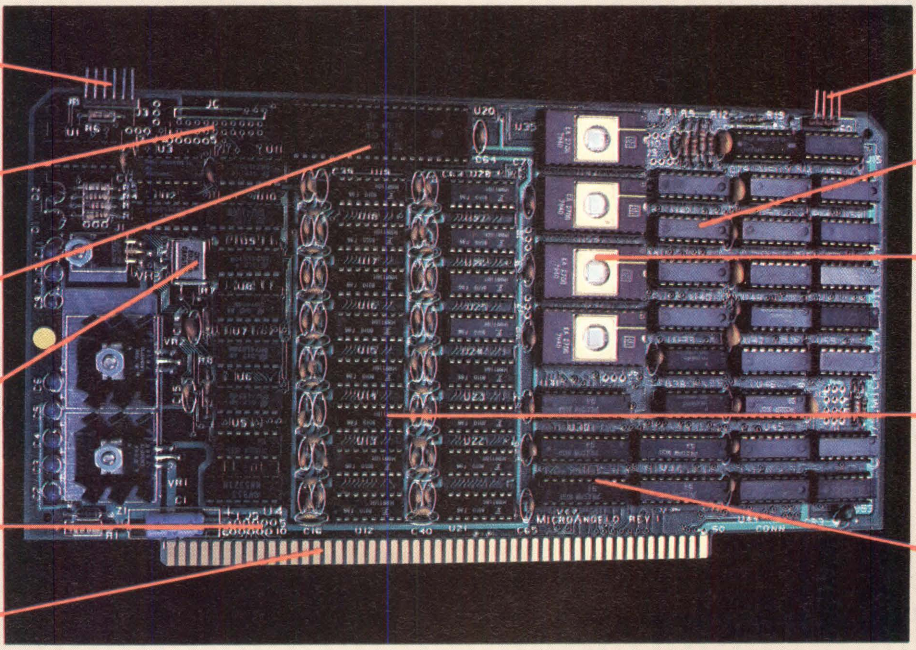

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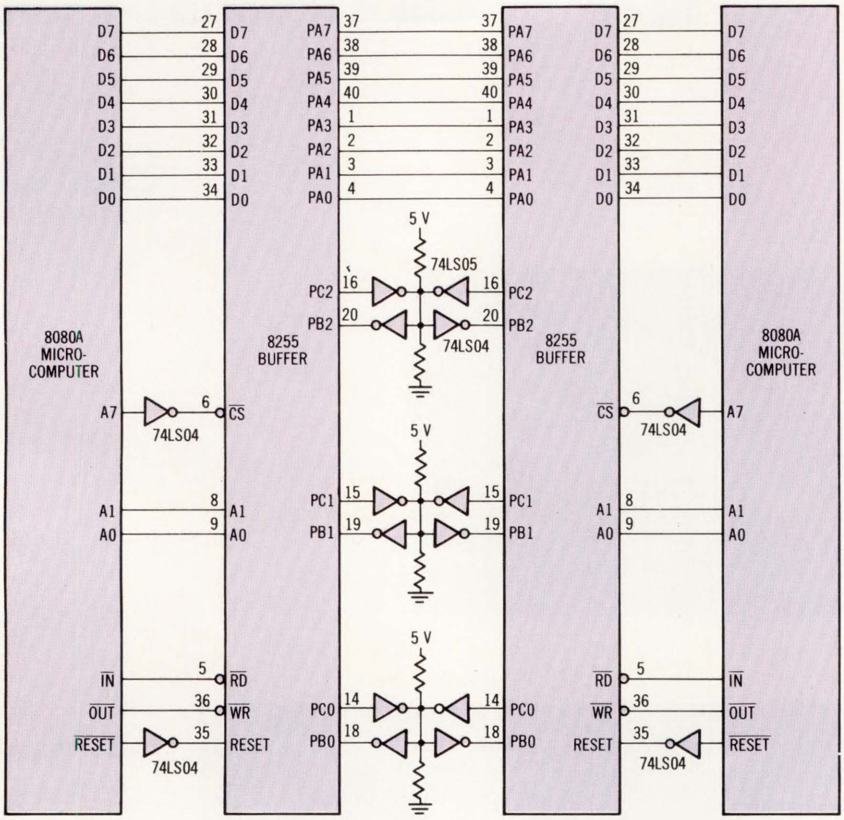

Fig 1 2-microcomputer doubled-buffered conditional I/O circuit. 3-wire handshake protocol is used, with bits PC0/PB0 corresponding to DAV, bits PC1/PB1 to NRFD, and bits PC2/PB2 to NDAC. Depending upon control words chosen for two 8255 chips, data flow can be either from left to right, or right to left. Each bus line is pulled up to 5 V with a 3-kΩ resistor, and down to ground with a 6.3-kΩ resistor

This means that port A for the talker 8255 chip is initialized to be an output port, and port A for the listener 8255 chip is initialized to be an input port. [Note that at a later time, the talker and listener roles in Fig 1 could be reversed. This presents no problem since the 8255 chip is programmable. Such a change in roles would not be possible if non-programmable chips, such as the 74LS244 3-state octal buffer and the 74LS373 octal D-type latch chips, were used.] Also, PC0 (DAV) is initialized so that the DAV bus line is at logic 0*; PC1 (NRFD) is initialized so that the NRFD bus line is at logic 1*; and PC2 (NDAC) is initialized so that the NDAC bus line is also at logic 1*. Since both the talker and listener 8255 chips contribute to the logic states of the DAV, NRFD, and NDAC bus signals, the correct output bytes to ports C must be picked. In this case, the talker outputs F8H to port C, whereas the listener outputs FEH to its port C. Asterisks (*) are used to distinguish between a positive-logic flag output or status input, and a negative-logic IEEE 488 bus signal.

An attractive feature of the 3-wire handshake protocol is that either talker or listener can be started first. If the talker is started before the listener is ready, NRFD = 0* and NDAC = 0*, and the talker halts. The three NOP instructions in the talker

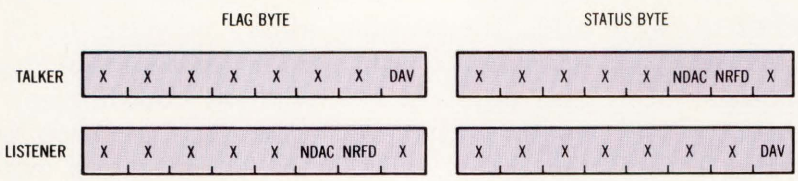

Fig 2 Flag and status bytes. Status of talker flag, DAV, is tested by listener. Status of each listener flag, NRFD and NDAC, is tested by talker. X indicates that logic state of bit is irrelevant

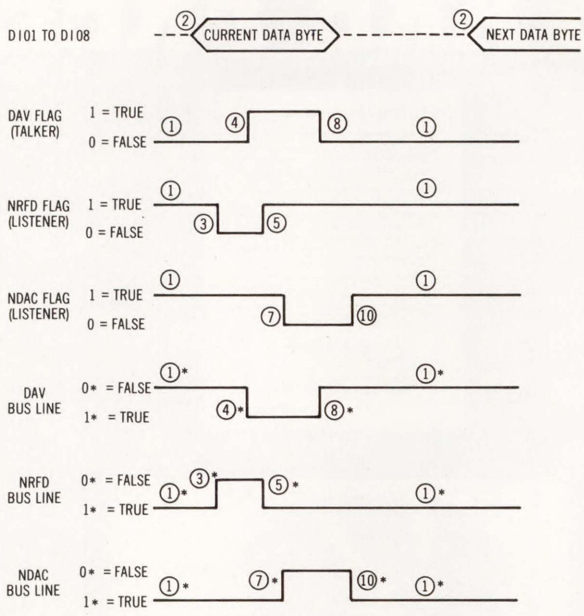

Fig 3 3-wire handshake timing diagram. Timing diagrams for three flags as well as three bus lines are shown. Circled numbers are correlated with Fig 4, and indicate important events that occur during single handshake cycle. Asterisk (*) indicates bus transition or condition

flowchart are provided so that a JMP 0319H instruction can be placed to bypass the HLT instruction. If the listener is started before the talker is ready, DAV = 1*, and the listener is trapped in a loop. For the purposes of the experiment described here, we have ignored the situation when either of the 8255 chips has just been reset and port C is no longer an output port; the programs work well, but no attempt has been made to detect the 8255 reset condition.

At location ② the talker outputs a data byte to data lines PA0 to PA7. Prior to location ③, the listener checks whether or not its memory block is full (YES if all 64 bytes have been transferred from talker to listener). If the answer is NO, the listener at point ③ resets NRFD = 0, indicating that it is ready for data, and then waits for DAV = 1*. At point ③*, the talker detects NRFD = 0* and thus passes to point ④, where it sets DAV = 1 and thus informs the listener that data are available. Finally, the talker proceeds to a loop where it waits for the NDAC = 0* condition. The listener detects the DAV = 1* condition at point ④*, sets NRFD = 1 at point ⑤ to indicate that it is not ready for the next data byte, inputs the data from data lines PA0 to PA7, stores the data byte in memory, and increments the memory pointer. At point ⑦, the listener resets NDAC = 0, indicating that it has accepted the data. Finally, the listener proceeds to a loop and waits for the DAV = 0* condition. The talker at point ⑦* detects the NDAC = 0* condition, calls a subroutine (placed in the program to permit experimentation with a time delay in the talker program), resets DAV = 0 at point ⑧ to indicate to the listener that data are no longer available, tests the memory pointer to determine if more data must be transmitted, and finally, if the answer is YES, jumps to the loop that tests for an error condition. At point ⑧*, the listener detects the DAV = 0* condition, and at point ⑩ sets NDAC = 1 to indicate to the talker that it has not accepted the next data byte. The listener then calls a subroutine (also placed in the program to permit experimentation with a time delay in the listener program), and jumps to the loop that tests for the memory full condition. *(continued on page 159)*

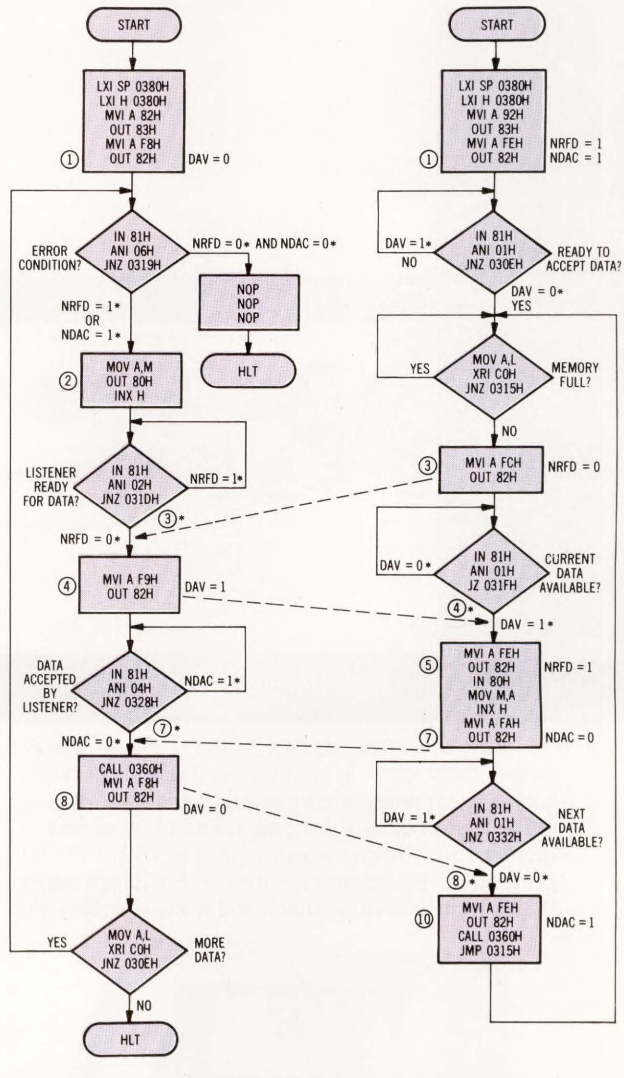

Fig 4 Flowcharts for 3-wire handshake protocol. Talker is on left, and listener on right. Asterisk (*) indicates testing of bus line signal status. Circled numbers are correlated with timing diagrams in Fig 3

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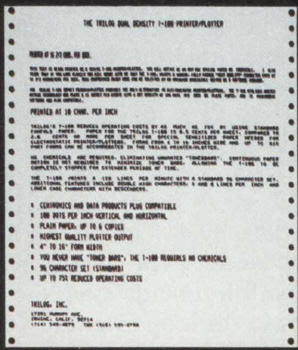
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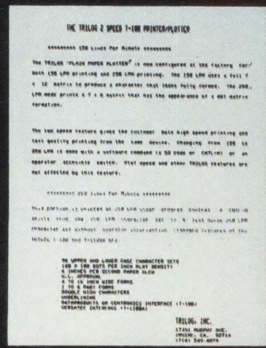
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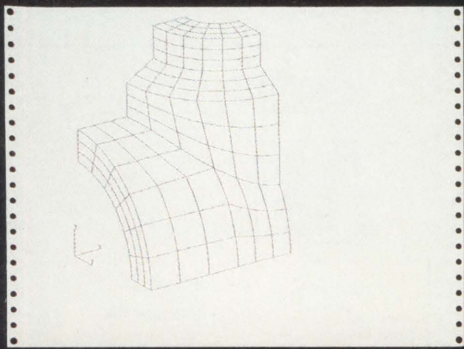
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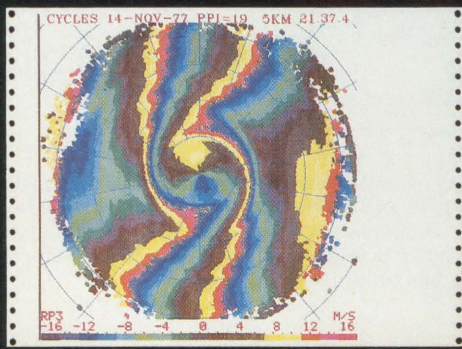

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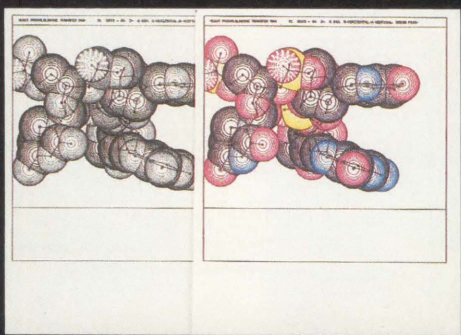
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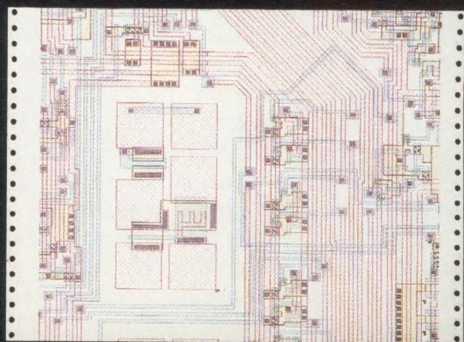
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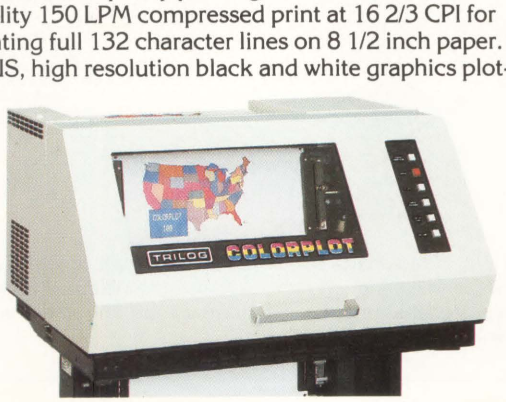

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Finally, the time required by the listener to input a single byte of data, that is, the time needed to execute one full pass through its program, was measured for a pair of 8080A based microcomputers that were both operating at 750 kHz. With no delay in either program, (a RET instruction at location 0360H), either 379 or 451 μs were required to make a single pass through the listener program. With a 9.53-ms time delay in the talker program, either 9.881 or 9.954 ms were required. With a 9.53-ms time delay in the listener program, 9.891, 9.927, or 9.964 ms were required. Lastly, with 9.53-ms delays in both programs, 19.394 ms, 19.430 ms, or 19.466 ms were required for the transfer of a single data byte from talker to listener. The variations in the preceding figures for a given choice of timing conditions are multiples of 36 μs, which corresponds, for microcomputers operating at 750 kHz, to 27 machine cycles. Since any of the bit-testing loops consists of IN, ANI, and JNZ or JZ instructions that add up to exactly 27 machine cycles, the 36-μs variation is easily understood.

Another example of a software IEEE 488 handshaking protocol is provided by Young.[6] The article helps to develop an understanding of other aspects of the IEEE 488 bus standard by giving bus protocol software listings, reduced state diagrams for the bus controller, and application subroutines.

References

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2. J. Pieper and R. J. Grossi, "LSI Streamlines Instrument Interface with Standard IEEE-488 Bus," *Electronics,* Apr 26, 1979, pp 145-150
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6. R. Young, "Implementing an IEEE-488 Bus Controller with Microprocessor Software," *IEEE Trans on IECI,* IECI-27, Feb 1980, pp 10-15

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High 722 **Average 723** **Low 724**

Dual-CPU microcontrollers execute in parallel to increase throughput

Offered for use in demanding control environments, especially those with human interfaces, COP2440 series microcontrollers contain two totally independent CPUs that share ROM, RAM, and I/O, and provide the user with custom capabilities. COP440 microcontrollers are single-CPU versions designed for high speed numerical operations, bit test/manipulation, and I/O intensive applications. They are also Microbus compatible, for use as smart peripherals in large computer systems. Both series, housed in 40-pin DIPs, are available from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051.

The availability of two CPUs allows the microcontrollers to handle two simultaneous, independent, realtime events on one chip. The two CPUs can work together, sharing data, or one CPU can offload tasks to the other. This 2-CPU approach increases throughput, allowing tasks to be executed in parallel instead of serially. Multiprocessing also reduces the required memory space by decreasing the amount of executive software required to schedule tasks.

In addition to two identical CPUs, these microcontrollers contain all the system timing, internal logic, RAM, ROM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include single-supply operation, numerous output configuration options, instruction set, internal architecture, and an I/O scheme designed to facilitate keyboard input, display output, and data manipulation.

Fabricated with N-channel silicon gate technology, single-CPU microcontrollers provide a 4-μs instruction execution time. Features include multivectored interrupt from four selectable sources (plus restart), 4-level subroutine stack, a programmable time-base counter for realtime processing, an internal counter-register, and MICROWIRE compatible serial I/O.

Desktop computer supports multiple operating systems, various peripherals

PC-8000 desktop computer houses processor, memory, and flexible disc subsystem in a compact keyboard display unit. A product of NEC Information Systems, Inc, 5 Militia Dr, Lexington, MA 02173, the computer supports multiple operating systems, programming languages, application packages, and peripheral devices.

System hardware consists of a Z80 compatible microprocessor with up to 64k bytes of dynamic RAM, plus up to 32k bytes of optional ROM. Available in either green-phosphor monochromatic or optional 8-color versions, the 80-column × 25-line video CRT allows users to select variable screen widths; variable size upper- and lowercase characters; static paging, scrolling, or split screen viewing; graphics; an alternate character set; blinking; inverse video; and an operator prompt line. The keyboard's 82-key array includes a standard typewriter layout, as well as a numeric pad and five dual-level programmable function keys.

Online data are stored on a minifloppy disc drive with a capacity of 320k bytes; a second 320k-byte dual-disc unit can be added when greater online storage is required. Magnetic tape cassette storage is also available. Standard I/O port adapters include a serial interface, monochromatic and color CRT interfaces, parallel printer interface, tape cassette interface, and expansion bus port. Data communications, at rates up to 4800 bits/s, is also available. Printers attach through either a serial or standard parallel interface.

Several operating systems, including CP/M, support various user languages: N-BASIC, FORTRAN, and assembler, among others. Application software includes a business analysis and planning system, as well as packages for payroll, general ledger, accounts payable and receivable, and inventory control.

Circle 401 on Inquiry Card

Z80 based boards offer local and remote I/O for control applications

Single function microcomputer boards based on the Z80 8-bit microprocessor are available from Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006, for industrial control applications. The boards complement the company's STD-Z80-Bus compatible microcomputer cards (see *Computer Design,* Aug 1980, p 140) with new features in local and remote I/O, process control software, built-in test and diagnostics, and hardware designed to function in industrial environments.

Cards offered include a clock with battery backup, dynamic RAM with battery backup, and a power fail detect board with battery backup that allows orderly power-down, memory retention, and power-up. Other cards available include the DIOB1 interface, high speed math, EPROM/UART, dynamic memory, serial and parallel I/O, and A-D conversion.

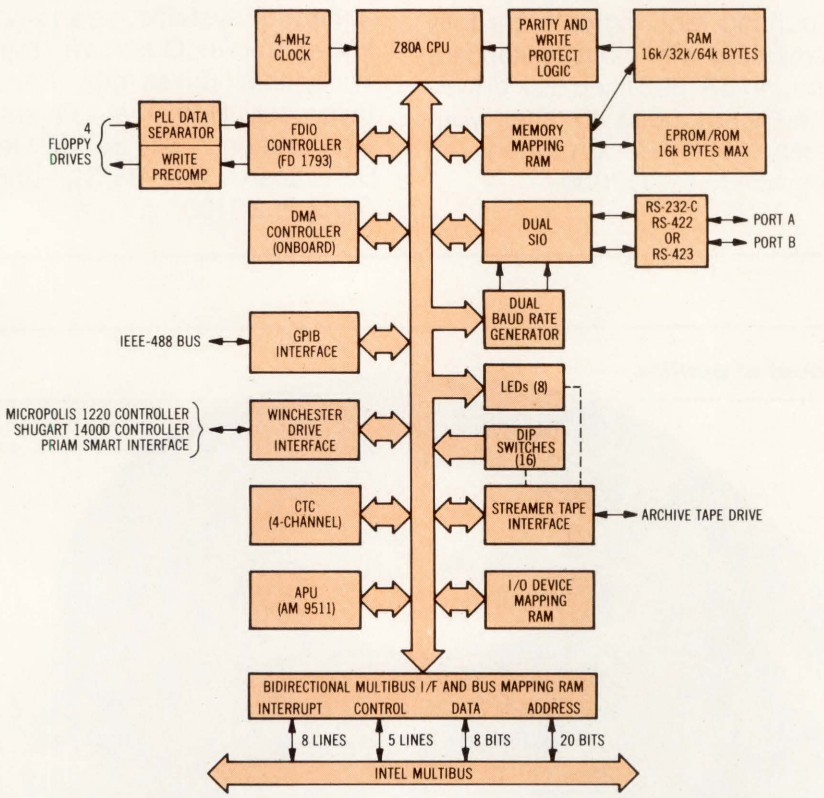
An optional interface, the RS-422 permits I/O to be located up to 4000′ (1219 m) from the main system. Two cards are available that permit either isolated or nonisolated transmission of data, allowing these units to function in a distributed process control configuration.

A system can provide control functions through the digital I/O panel (DIOP) that has up to 16 optically isolated connection points. Each point has a socket for a standard isolated solid state relay, fuse holder, LED indicator, and manual test mechanism. These are mounted in sockets for ease of replacement. Up to 16 DIOP units can be connected to the control box via a digital I/O bus that interfaces with a DIOB1 card in the card cage. Each DIOB1 card accepts 256 points of digital and/or analog I/O. As many as 16 single-ended or 8 differential input channels can be connected.

Measuring 4.5 x 6.5″ (11.4 x 16.5 cm), the cards fit into a standard 16-slot card cage in a special enclosure, designated ENCL-1, that also has a 150-W power supply and front panel controls and mounts in a NEMA container for use in an industrial environment. The 16-slot card cage allows for system expansion with additional cards, and use of single-function boards allows the system to be configured to meet specific requirements.

Circle 402 on Inquiry Card

Single-board μcomputer incorporates dynamic memory controller chip



Single-board microcomputer. Heurikon Corp's Z80A based MLZ-91A uses 40-pin TMS-4500 dynamic memory controller chip from Texas Instruments to handle dynamic RAM timing, refresh, and address multiplexing functions

A Z80A based, single-board microcomputer, MLZ-91A uses the TMS-4500 dynamic memory controller chip from Texas Instruments Inc to handle timing, refresh, and address multiplexing for 64k bytes of onboard DRAM. The microcomputer, offered by Heurikon Corp, 3001 Latham Dr, Madison, WI 53713, also contains DMA controller, memory mapping RAM, and I/O mapping RAM onboard.

The 40-pin TMS-4500 chip connects directly to the CPU address bus and is supplied with an 8-MHz clock signal. When a RAM access is desired, an enable signal triggers the chip to perform a memory cycle. Memory refresh cycles are automatically generated to prevent memory loss even in the absence of CPU requests. The system's dynamic RAM runs at full processor speeds without wait states.

Vectored interrupt capability and Z80 instruction set are provided by the Z80A CPU. An onboard jumper allows system clock frequency to be reduced to 2 MHz for system debug operations. Onboard programmable DMA offers Z80 compatible I/O and memory data transfers; multimode operation; and memory to memory, port to memory, memory to port, and port to port transfers.

The microcomputer has two ROM sockets that accommodate Intel 2716, 2732, or 2764 type EPROMs and 64k bytes of oncard dynamic RAM with a parity bit to detect errors. Compatible with the expanded Intel MULTIBUS, the microcomputer features 20-bit address space, fully addressable by CPU or DMA, that provides 1M bytes of addressable memory offcard. A programmable address mapping RAM puts the memory map completely under software control, allowing full use of the 20-bit bus address space.

Two serial ports are provided with dual baud rate generator and crystal. These ports support synchronous or asynchronous communications, including SDLC. Both ports can be configured for RS-232, RS-422, or RS-423, and baud rates are software selectable from 50 to 19.2k baud. Four independent counter/timer channels can be used as event counters, realtime clocks, or timed interrupt generators.

Circle 403 on Inquiry Card

Magnetic bubble memory system conforms to IEEE S-100 standard

A self-contained magnetic bubble memory system that includes driver software to interface to any 8080/Z80 CP/M (version 2.0) system, S100B MBMS uses Intel's 7710 1M-bit bubble device and is fully IEEE compatible. The board, available from Teleram Communications Corp, 2 Corporate Park Dr, White Plains, NY 10604, has a capacity of 128k to 256k bytes of nonvolatile storage and occupies one slot in any S-100 system. Up to four boards can be daisy chained to provide 1M bytes of storage. The compact board offers low power consumption and high reliability and is suited for portable process control and point of sale applications.

To detect and correct burst errors of up to 5-bits, a 14-bit Fire code is appended to each 256 bits of data. Data rates range from 100k bits/s in a 1-bubble system to 800k bits/s in an 8-bubble system; average access time is 40 ms. Polling, interrupt, and DMA transfer methods are provided, as well as a power fail detect capability. Operating temperature is 0 to 50 °C at 95% humidity; temperature range for nonvolatile storage is −40 to 100 °C.

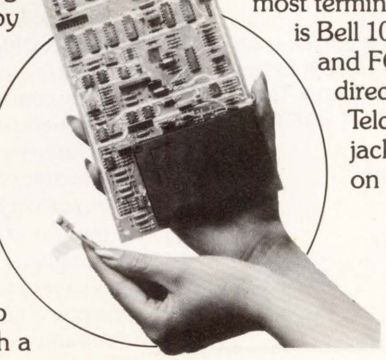
Circle 404 on Inquiry Card

Now, OEMs can take the High Road or the Low Road with our Direct-Connect Modem Cards, small enough to mount inside Data Terminals.

As the auld Scottish tune suggests, Racal-Vadic now makes it easy for OEMs to take the high road (1200 bps) or the low road (300 bps), with low cost direct-connect "Modems-on-a-Card," small enough to mount inside CRT displays, teleprinters, POS devices, and other terminals and systems.

The High Road: 1200 bps

Meet the compact VS1200P, a complete modem on a single PC board measuring 5″ by 8.35.″ That's a thrifty 42 square inches of space. It's fully compatible with Bell 202C and S modems. Only better, offering much more in performance, flexibility and test capability. It's registered for direct-connect, too. Connects to the switched network with a cable that plugs right into a Telco voice or data jack. Built-in 20 pin ribbon connector easily interfaces the VA1200P to your terminal. Price is right, too. Just $200 in quantities of 100.



The Low Road: 300 bps

The VS300P is a 300 bps full duplex, automatic originate/answer "Modem-on-a-Card." Like the VS1200P, it measures only 5″ by 8.35,″ making it small enough to mount inside most terminals. The VS300P is Bell 103/113 compatible, and FCC Registered for direct connect via a Telco voice or data jack. Mounting holes on each corner make it a cinch to install. And the price would put a smile on the face of the thriftiest Scotsman. Just $200 in lots of 100.

Both Roads: The TI Story

Two of Texas Instruments new Silent 700* data terminals include Triple Modems custom made by Racal-Vadic. Although small enough to fit into TI's portable 17 pound terminal, this remarkable modem combines a Racal-Vadic VA3400, a Bell 212A, and a Bell 103. Imagine, a full originate/answer direct-connect modem with both 1200 bps full duplex and 300 bps full duplex in such a tiny package. And it can even be acoustically coupled.

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CIRCLE 90 ON INQUIRY CARD

Z80A processor and byte wide memory cards offered for STD BUS

Two complementary STD BUS cards, a processor card with 3-channel counter/timer, and a byte wide memory card are supplied by Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940.

Model 7804 is a Z80A processor card with an onboard 3-channel counter/timer function and four JEDEC 28-pin memory sockets. Each independent 16-bit counter/timer channel can be configured under program control for event/frequency counting from dc to 2.5 MHz or for waveforms generation. The four sockets have jumper selectable option for seven current RAM/ROM device types, and JEDEC standard ensures future device compatiblity.

The 7704 byte-wide memory card has eight JEDEC 28-pin sockets onboard. Each card offers 15 user-selectable ROM, P/ROM, and RAM options for maximum population flexibility using the STD BUS MEMEX line. With two cards, total memory capacity is 128k bytes.

Circle 405 on Inquiry Card

Multibus compatible development/control system for rugged applications

A Multibus compatible development/control system based on the 8086 microprocessor, DCS/86 is available from Distributed Computer Systems, 223 Crescent St, Waltham, MA 02154. A logical upgrade to the company's DCS/80 (see *Computer Design,* Jan 1980, p 158), the system provides 24 bits of parallel I/O and three serial ports.

A 5- or 10-MHz 8086 16-bit microcomputer, vectored interrupt, and timer/counter are contained in the system's DCS 86/16 CPU. One of the three serial ports is a standard 8251A; the others are standard RS-232 and RS-422 protocol ports. The RS-422 port is intended for distributed network systems when up to 32 systems can be connected using DCS/86 or ICM/80 industrial control modules. Point to point systems and communication with IBM mainframes can be accomplished in bisynchronous modes using RS-232 ports. With the addition of floating point processor (8087), the system's performance rivals a PDP-11/45 midrange minicomputer.

Full multimaster control is provided, and multiple CPUs can be placed in the backplane for true tightly coupled multiprocessor operation. The system can contain up to 1M bytes of memory, and includes 8" (20-cm) floppy discs and an all aluminum, vertically mounted, 9-slot Multibus card cage with an integral fan.

Included in the system is the CPM/86 disc operating system that is functionally compatible with CP/M. The operating system contains random and sequential file structures, editor, macro assembler, and utilities to enhance programmer productivity; there is complete file interchangeability between diskettes. MPM/86, a multi-user, multitasking system, will be available in the future. High level languages include BASIC, Pascal, COBOL, FORTRAN, and PL/1 (Subset G).

Circle 406 on Inquiry Card

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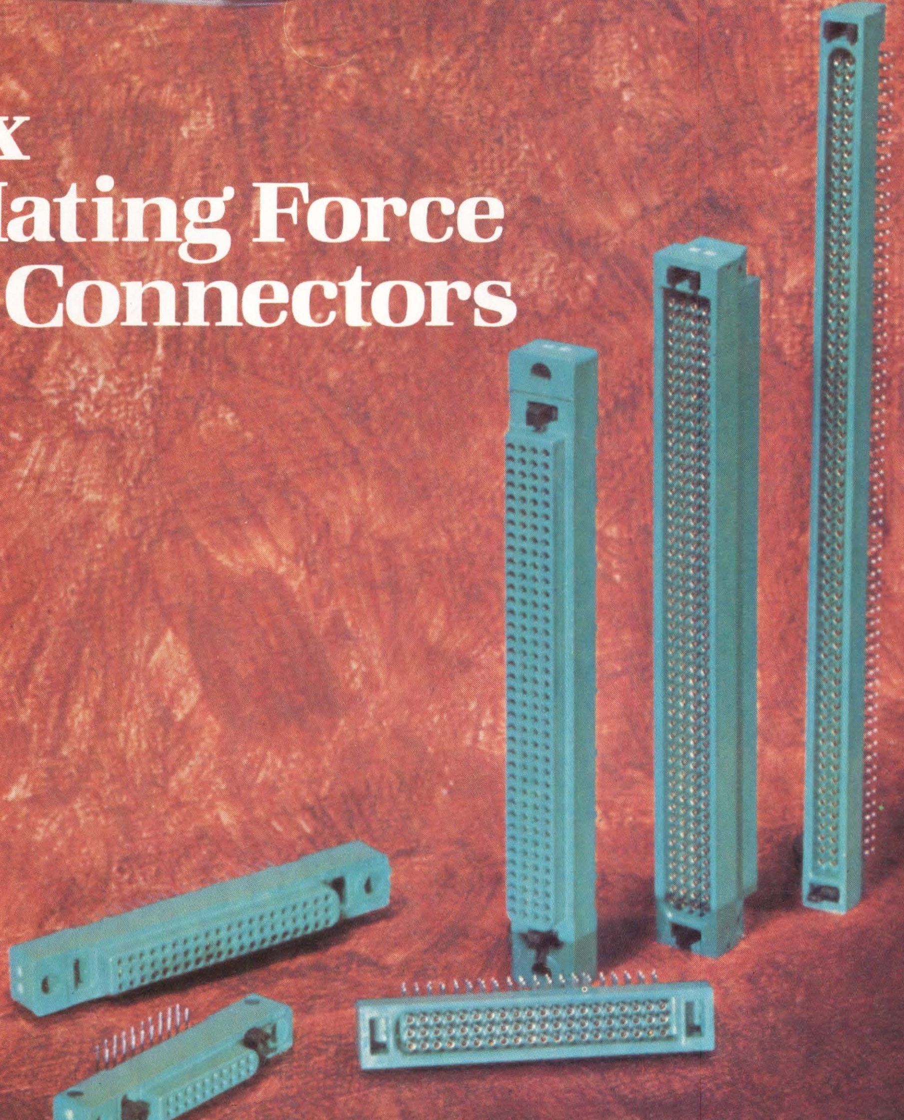

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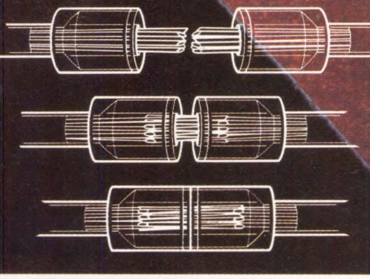

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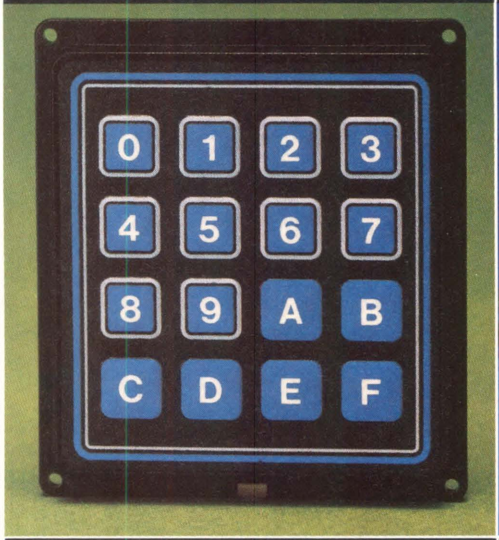
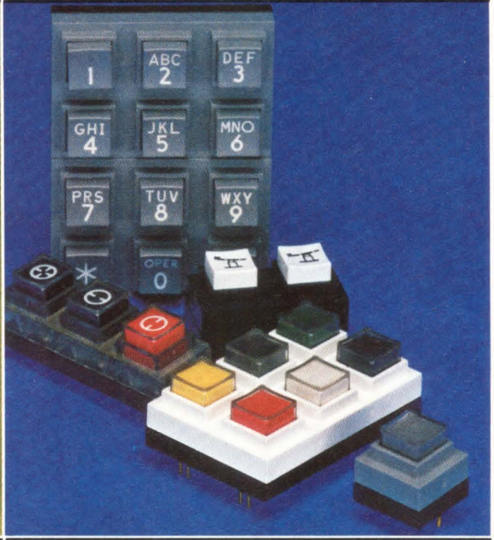
CIRCLE 92 ON INQUIRY CARD

GRAYHILL KEYBOARDS: DIFFERENT STROKES FOR DIFFERENT FOLKS

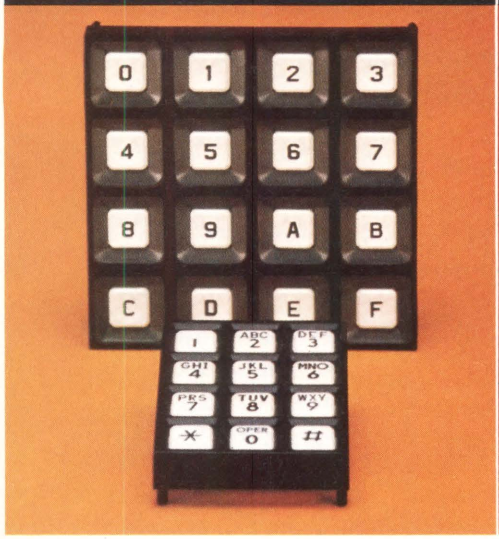
SERIES 88 A short stroke *sealed* keyboard with excellent audible and tactile feedback. Colorful standard or custom-made graphics integrates this keyboard into your front panel. Coded outputs and low bounce characteristics easily mate with logic circuitry. Circle No. 191



SERIES 82 Long stroke high profile, wiping contacts. 1, 2, 3 and 6 button modules can be arranged for your specific needs. SPST to 4PST circuitry under each button; also available with coded outputs. Circle No. 192



SERIES 83-84-86 Short stroke standard 3x4 and 4x4 keyboard configurations. Choice of ½ inch or ¾ inch button centers and post or flange mounting. Standard coded outputs—easily interfaces with logic circuitry. Excellent audible and tactile feedback. Circle No. 193



SYSTEM 87 Short stroke low profile, snap dome contact system provides tactile and audible feedback. Modular units—1 thru 6 buttons and 3x4 and 4x4 pads can provide any conceivable button arrangement. Circle No. 194

Your product is distinctive, and thus your keyboard needs are also likely to be unique. That's why Grayhill offers you four different keyboard families, with a host of options in each. We'll help you arrive at the keyboard solution that's most practical, attractive, and cost effective. Two of our four families—Series 83-84-86 and Series 88—are built around the popular 3 x 4 and 4 x 4 keyboard configuration; the other two—Series 82 and System 87—are modular, allowing you to create any unique keyboard arrangements.

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- high or low profile
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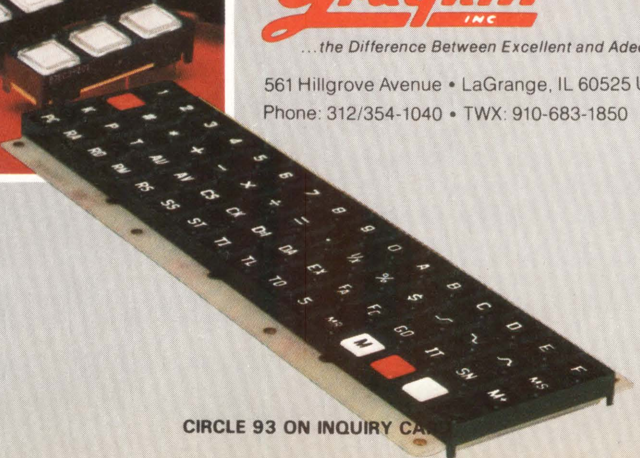


CIRCLE 93 ON INQUIRY CA

8-bit CMOS μcomputers supported by peripheral chips, development system

A family of single-chip 8-bit CMOS microcomputers, Series 80 consists of four microcomputer unit circuits, peripheral chips, and a complete development support system. Offered by OKI Semiconductor, Inc, 1333 Lawrence Expressway, Suite 401, Santa Clara, CA 95051, the family corresponds to 8048/8049-type NMOS devices. The microcomputer unit circuits are fully pin compatible with Intel Corp's 8048/8049 circuits, but provide lower power dissipation.

The MSM80C48 microcomputer unit (MCU) offers 1k bytes of mask-programmable onchip ROM, 64 bytes of RAM, and a standby supply current of 50 μA maximum and 10 mA maximum at 11 MHz in operation. The MSM80C49 MCU offers 2k bytes of mask-programmable onchip ROM, 128 bytes of RAM, and standby power of 70 μA maximum and 12 mA maximum at 11 MHz in operation. Both units feature an interval timer/event counter, single-level interrupts, 110 instructions (70% single byte), and 2.5-μs instruction cycle time, and operate from a 5-V ± 10% supply voltage with full TTL compatibility. MSM80C35 is identical to MSM80C48 except that instructions are fetched from external memory, either ROM or EPROM, while MSM80C39 is the development circuit for the MSM80C49.

In addition to 8048/8049 instructions, the series includes two types of HALT and three types of FLOAT (3-state I/O) instructions. Eight instructions implement efficient port moves and indirect decrement functions.

Providing realtime emulation, the MPB800 evaluation board is the major development tool for the series. The board operates with any computer or development system using Intel's ISIS or Digital Research Corp's CP/M operating system. Debugging features include unlimited breakpoints, trace capability, and single-step mode. CMOS I/O peripheral circuits designed for the Series 40 family (see *Computer Design,* Dec 80, p 140) are fully compatible with Series 80 parts. Circuits designed specifically for this family include the 82C43 I/O expander, with additional peripherals under development.

Circle 407 on Inquiry Card

Single-board 16-bit computer series supports large memory requirements

Gateway series 16-bit single-board computers, designed around Intel's 8086 and 8087 and Motorola's MC68000, conform to Multibus standards, including multi-master capability, and are compatible with both 8- and 16-bit peripheral boards. The series was designed by Forward Technology Inc, 1440 Koll Circle, Suite 105, San Jose, CA 95112, specifically to meet the needs for memory management and protection encountered with multi-user operating systems.

Models FT-86C and FT-86M feature Intel's 16-bit 8086 processor, and can directly address 1M bytes of memory and support mapping addresses of 8M bytes. Using Motorola's MC68000, the -68M directly addresses 15M bytes. FT-86C/FP and FT-86M/FP add Intel's 8087 numeric data processor that multiplies 32-bit and 64-bit real numbers in 19 μs and 27 μs, respectively. All four models have two RS-232-C user programmable communication ports, each of which handles asynchronous formats, synchronous byte-oriented protocols, and bit-oriented protocols such as HDLC and SDLC. CRC codes are generated in synchronous mode to ensure data integrity. Each communication channel supports speeds up to 19.2k baud. Digital Research's CP/M-86 and the company's firmware-resident Forth operating system are supported.

Computers in the series are provided with 4k bytes of user programmable RAM and four sockets for up to 32k bytes of ROM. The firmware-resident Forth operating system uses two sockets, leaving 16k bytes for custom firmware. Eight priority levels of vectored interrupts are also provided.

Models FT-86C and FT-86C/FP offer a customization area of unused board space that enables users to add custom logic and circuitry. The customization area accommodates approximately 30 16-pin ICs, or fewer 20-pin ICs. Users can also include 32k bytes of additional RAM in this area.

Memory management and protection features of both FT-86M and FT-86M/FP support up to seven users. Additional low duty cycle users can be added for a small increase in system overhead. The memory management system extends the 8086's addressing range to 8M bytes that can be allocated in 2k-byte pages. Intertask protection and common write protect areas are supported as standard.

Circle 408 on Inquiry Card

8-bit slice CMOS chip set comprises emulation and programmable ICs

An expandable, 8-bit slice CMOS microprocessor chip set, the GP Series from RCA/Solid State Div, Route 202, Somerville, NJ 08876, can be used to emulate computers with established software as well as for entirely original computer architecture. To increase flexibility and computing power, a number of microprocessors can be linked together in a series to permit word lengths in multiples of 8 bits. The chip set offers power and performance advantages over existing bipolar chip sets, as well as parts count reductions, and provides opportunities for standardization in military applications.

Initially, the set will include an 8-bit slice general processor unit (GP001A), an emulating controller (GP501A), a microprogram sequencer (GP502A) similar to the industry standard 2910 bipolar unit, and an 8 x 8 multiplier (GP503A). RAM, ROM, and gate universal array (GUA) ICs support these circuits. Included are two 4k-byte RAMs (1k x 4 and 4k x 1 GP201A/202A), two ROMs (512 x 8 and 256 x 16 GP301A/302A), and GUA functions such as address select (GP504A), register select (GP505A), bus interrupt (GP506A), and interrupt control (GP507A).

The devices are specified to the full military temperature range, −55 to 125 °C. They are man-rated radiation hardened and screened to MIL-STD-883 Class B. All of the devices are offered in leadless hermetic ceramic chip carrier packaging. General processor unit cycle time is 10 MHz at 10 V.

The chip set is expandable and reconfigurable via concatenation and CMOS gate arrays. Mask programmable arrays having 182 to 848 gates can be customized to provide I/O and support circuits using the company's computer aided design automation system.

Circle 409 on Inquiry Card

Variable speed control system plugs into microprocessor backplane

A variable speed motor control system for industrial applications has been developed by Datatran Labs, Inc, PO Box 384, Sussex, NJ 07461, for use with its PC-774 microprocessor based controllers. The system plugs directly into the same enclosure and backplane used by the microprocessor and provides full wave phase controlled armature voltage to both shunt wound and permanent magnet dc motors rated up to 1 hp.

Standard speed range is 100 to 1, with 12-bit resolution. Speed regulation is better than 1% under load change. Linear acceleration and deceleration are adjustable from 0.050 to 200 s, in nine overlapping ranges. Controls limit maximum armature current as well as compensate for the drop in speed that occurs with increasing shaft load when armature voltage is used for the speed feedback signal. The speed control system appears as four memory locations on the address bus. All interface lines are TTL compatible as well as buffered and optically isolated from the power section of the system. The system meets interface requirements of any 6800 based system. Circle 410 on Inquiry Card

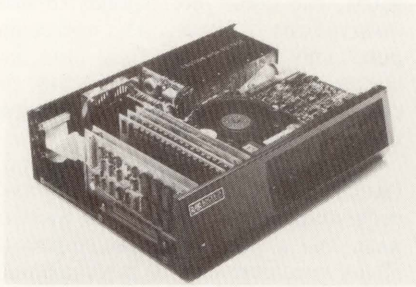
Interface card links personal computer with IEEE-488 instruments

Designed to link Apple II computers with over 1400 instruments used in scientific and technical applications, the IEEE-488 interface card is available from Apple Computer Inc, 10260 Bandley Dr, Cupertino, CA 95014. The card allows Apple II and II Plus computers to monitor production lines, record and evaluate scientific data, run test equipment, and interface with any device compatible with the IEEE-488 bus.

The card can function as both a controller and a device. Using resident firmware, it needs only simple commands to control the bus. The card implements a fully compatible subset of the IEEE-488 standard. When functioning as a device, the interface card can be used to attach non-IEEE-488 compatible devices to the bus.

The card can also be driven from any Apple II supported language. Up to three cards can be installed in the Apple II's interface slots, enabling a single system to control as many as 42 IEEE-488 compatible instruments.
Circle 411 on Inquiry Card

Desktop μcomputer contains 5.25" Winchester and floppy disc drives



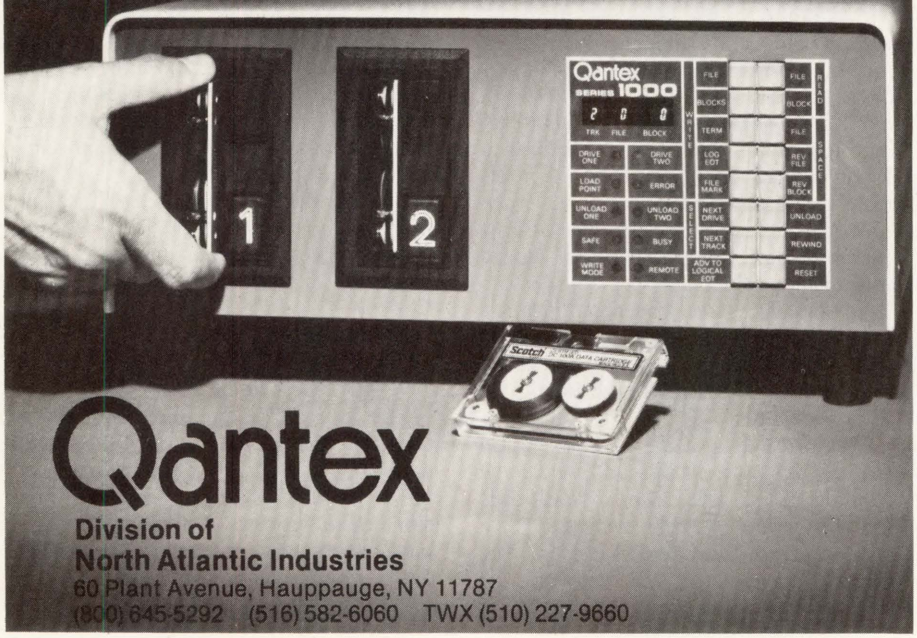
Microcomputer system. Black Box III, offered by Rair Microcomputer Corp, contains 5.25" (13.34-cm) Winchester drive plus 500k bytes of floppy disc backup storage in desktop enclosure

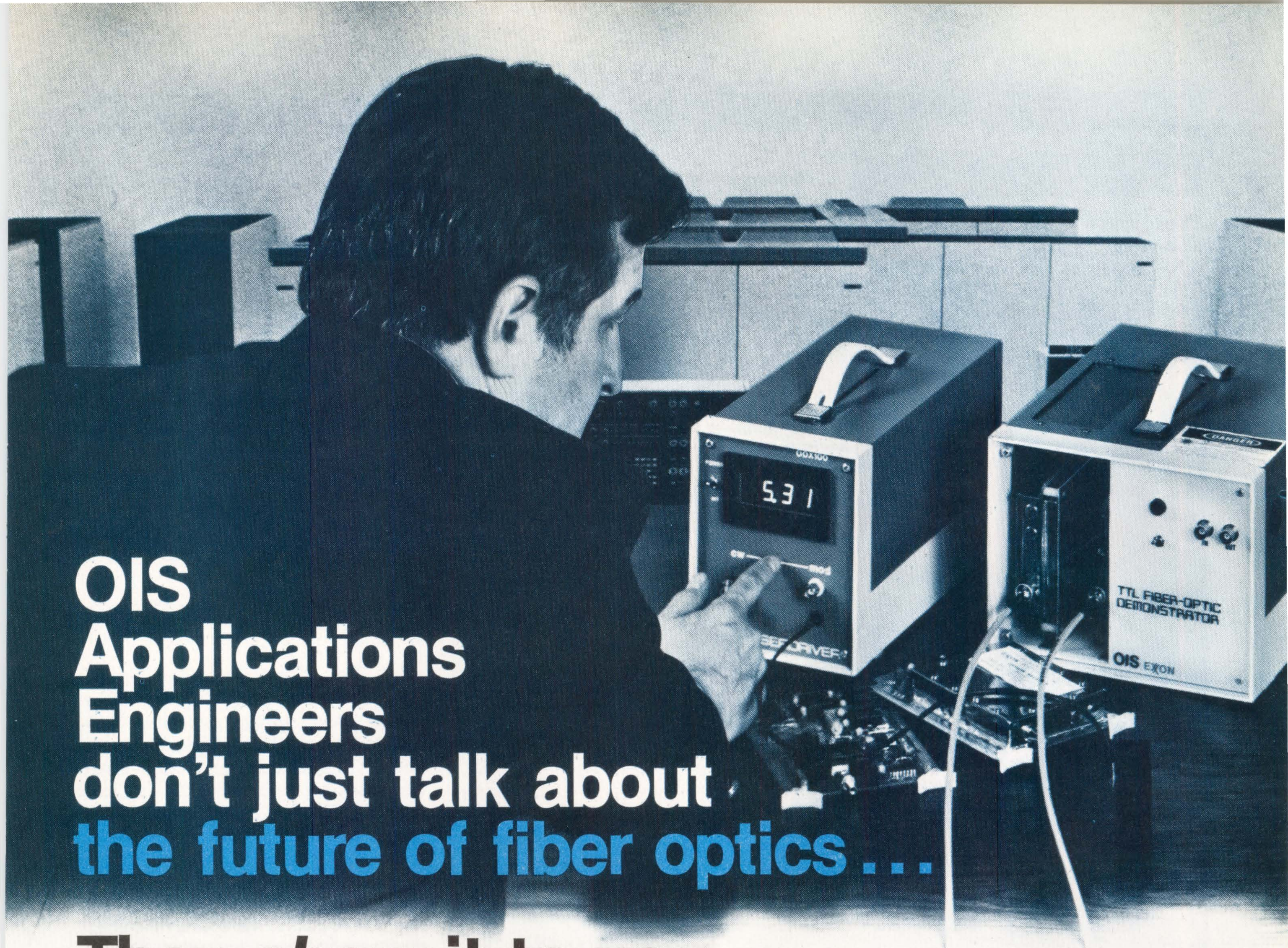
A general purpose microcomputer system aimed at OEMs and system integrators, Black Box III model 3/30 includes a built-in 5.25" (13.34-cm) Winchester disc drive with 6.9M bytes of storage, as well as 500k bytes of double-sided, double-density floppy disc backup storage, in a low profile desktop enclosure. Developed by Rair Microcomputer Corp, 4101 Burton Dr, Santa Clara, CA 95050, the computer expands from a basic single-user system to support a multiterminal system with networking capabilities.

Up to 16 peripheral devices can be connected to a single system using standard RS-232-C serial ports; the IEEE-488 parallel bus can connect an unlimited number of peripherals and provide a high speed computer-to-computer link.

The unit features 64k bytes of RAM, standard; additional RAM may be included in 64k- or 256k-byte increments, up to the system's total 512k-byte capacity.

The computer is supported by a range of operating system software, including single-user and multi-user/multiprogramming systems and shared resource networking. Compatible languages include BASIC, FORTRAN, COBOL, Pascal, and PL/1.
Circle 412 on Inquiry Card





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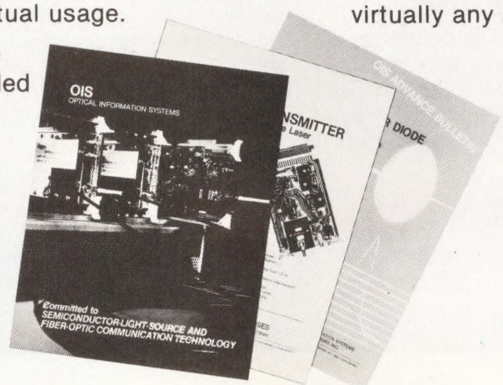

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CIRCLE 95 ON INQUIRY CARD

BRIEFS

Power supply system serves floppy disc μcomputer systems—An open frame power supply with four regulated dc outputs, CP125, from Microcomputer Power, Inc, 2272 Calle de Luna, Santa Clara, CA 95050, provides both floppy disc and microcomputer voltages and currents in a single package. Outputs are 5 V at 6 A, 24 V at 1.3/1.7 A peak, 12 V at 1 A, and −12/−5 V at 0.5/0.25 A. Features include 0.05% line and load regulations, 3-mV peak to peak ripple, built-in OVP on 5 V of output, and current limit/foldback for continuous overload protection.
Circle 413 on Inquiry Card

High resolution light pen provides 60-Hz coordinate generation—A high resolution light pen system with full 280 x 192 Apple Hi-Res resolution, LPS-II is available from Gibson Laboratories, Bldg 10, 406 Orange Blossom, Irvine, CA 92714, for Apple II computers. The pen is compatible with Applesoft and Integer BASIC, FORTRAN, Pascal, PILOT, Forth and CP/M, and can be used in every Apple screen mode. It installs on the computer's motherboard and provides the user's program with instantaneous horizontal and vertical location of the pen point at a full 60-Hz rate.
Circle 414 on Inquiry Card

Controller board doubles Shugart compatible disc storage capacity—Compatible with the Heath 88/89 microcomputer, floppy disc controller board FDC-880H converts 5.25″ (13.34-cm) hard sectored discs to standard soft sector double-density, allowing users to double their storage capacity without adding drives or discs. Offered by CDR Systems, Inc, 7667 Vickers St, Suite C, San Diego, CA 92111, the board runs under the CP/M 2.2 operating system and accommodates up to four Shugart compatible drives simultaneously. It handles single- or double-sided operation and single- or double-density data, and occupies any I/O slot in the computer without modification.
Circle 415 on Inquiry Card

μcomputer combines processor, keyboard, and disc drives in desktop console—Standalone Microlite II microcomputer combines keyboard with 100 key stations, numeric pad, and 32 function keys; 24-line x 80-character plasma display; and two 5.25″ (13.34-cm) floppy disc drives in a single typewriter sized console. Options for the system, from Q1 Corp, 125 Ricefield Lane, Hauppauge, NY 11787, include 8″ (20-cm) floppy disc drives with 500k-byte capacity; rigid disc drives with 27/54/205M-byte removable or 24/40M-byte Winchester fixed media; magnetic tape drives; and daisywheel, dot matrix, or 300-line/min printers.
Circle 416 on Inquiry Card

BRIEFS

Video monitor supplies 40- or 80-character display for microcomputers—ZVM-121, 12″ (30-cm) monitor, offered by Zenith Data Systems, 1000 Milwaukee Ave, Glenview, IL 60025, displays an 8 x 10-character matrix and up to 24 lines of information on a green screen. Exterior controls include power, black level, contrast, horizontal and vertical adjustment, vertical size adjustment, and a switch that permits selection of 40- or 80-character display. Bandwidth greater than 12.5 MHz and 60-ns rise time provide increased character definition.

Circle 417 on Inquiry Card

Asynchronous multiplexer offered for DEC LSI-11 hardware—DHK11 asynchronous multiplexer is offered for use in communications applications with Digital Equipment Corp's LSI-11 hardware by K. O. Mair Assoc, Ltd, 145 Spruce St, Ottawa, Ontario K1R 6P1, Canada. The unit is RT-11 and RSX11/M software compatible, and is modular in groups of eight lines per set of dual boards. Features include eight separate DMA channels for each serial output line, 16 software selectable baud rates of up to 19.2k baud, software control of all line parameters, and a 64-character hardware buffer for received characters.

Circle 418 on Inquiry Card

Floppy disc controller board is compatible with Apple μcomputer—LCA-22 disc controller board for the Apple microcomputer is software compatible with APPLE DOS, and contains 256 bytes of onboard boot ROM. A product of Lobo Drives International, 354 S Fairview Ave, Goleta, CA 93117, it controls up to four 8″ (20-cm), single- or double-sided, single- or double-density floppy disc drives with a total storage capacity of 4.4M bytes. Features include an average access time of 200 ms and a DMA designed for full 6.25k-byte/s transfer rate.

Circle 419 on Inquiry Card

Microcomputer operates standalone or as development tool—K-8073 microcomputer uses National's INS8073 single-chip Tiny BASIC microinterpreter MPU and functions as a development tool or standalone dedicated computer. Developed by Transwave Corp, Cedar Valley Bldg, Vanderbilt, PA 15486, the single-board computer features RS-232 serial communication, casette tape I/O, plug-in EPROM, onboard EPROM programmer, 1k-byte local RAM, STD (MOD) BUS structure, asynchronous receiver transmitter remote controller, PPI with 24 bidirectional I/O lines, realtime/date clock, two sense interrupts, multitasking, and 2k-byte ROM firmware that provides all development utilities.

Circle 420 on Inquiry Card

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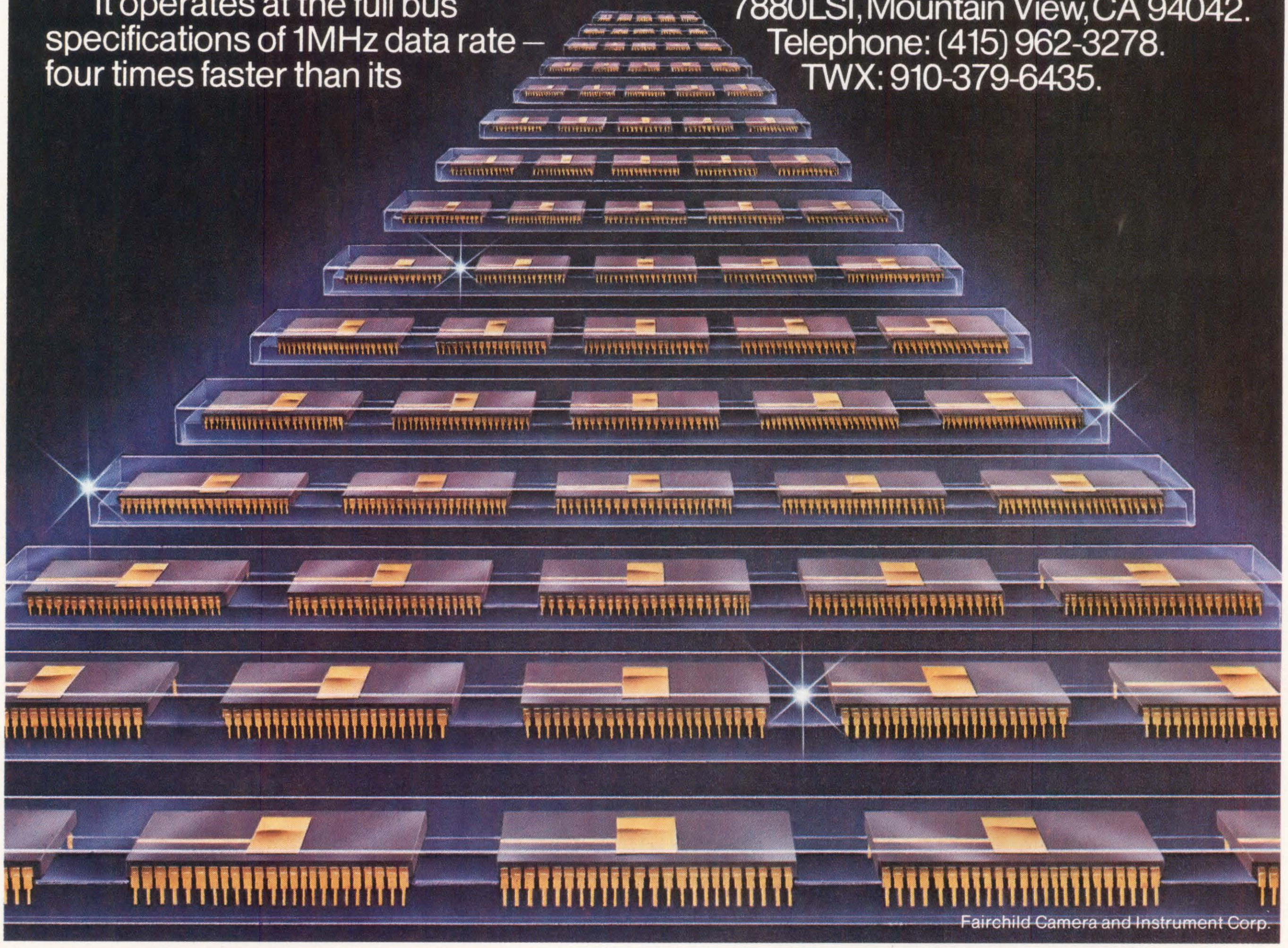

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CIRCLE 99 ON INQUIRY CARD

DATA STACK

BRIEFS

Microcomputer analyzer features internal trace capability—Handheld microcomputer analyzer from Patuck Inc, 5073 Russell Ave, Pennsauken, NJ 08109, clips directly to the microcomputer under test; when connected, it can single-step the processor or let it run to a selected error vector or trap address. Internal trace capability allows examination of the 63 machine cycles that precede breakpoint. Information is displayed and the problem analyzed on 8.5-digit display. Interchangeable interfaces are available for various 8-bit chips, including Z80, 8080, 2650, 6501, 6502, 6605, 6800, 6802, 8060, and 8085.

Circle 421 on Inquiry Card

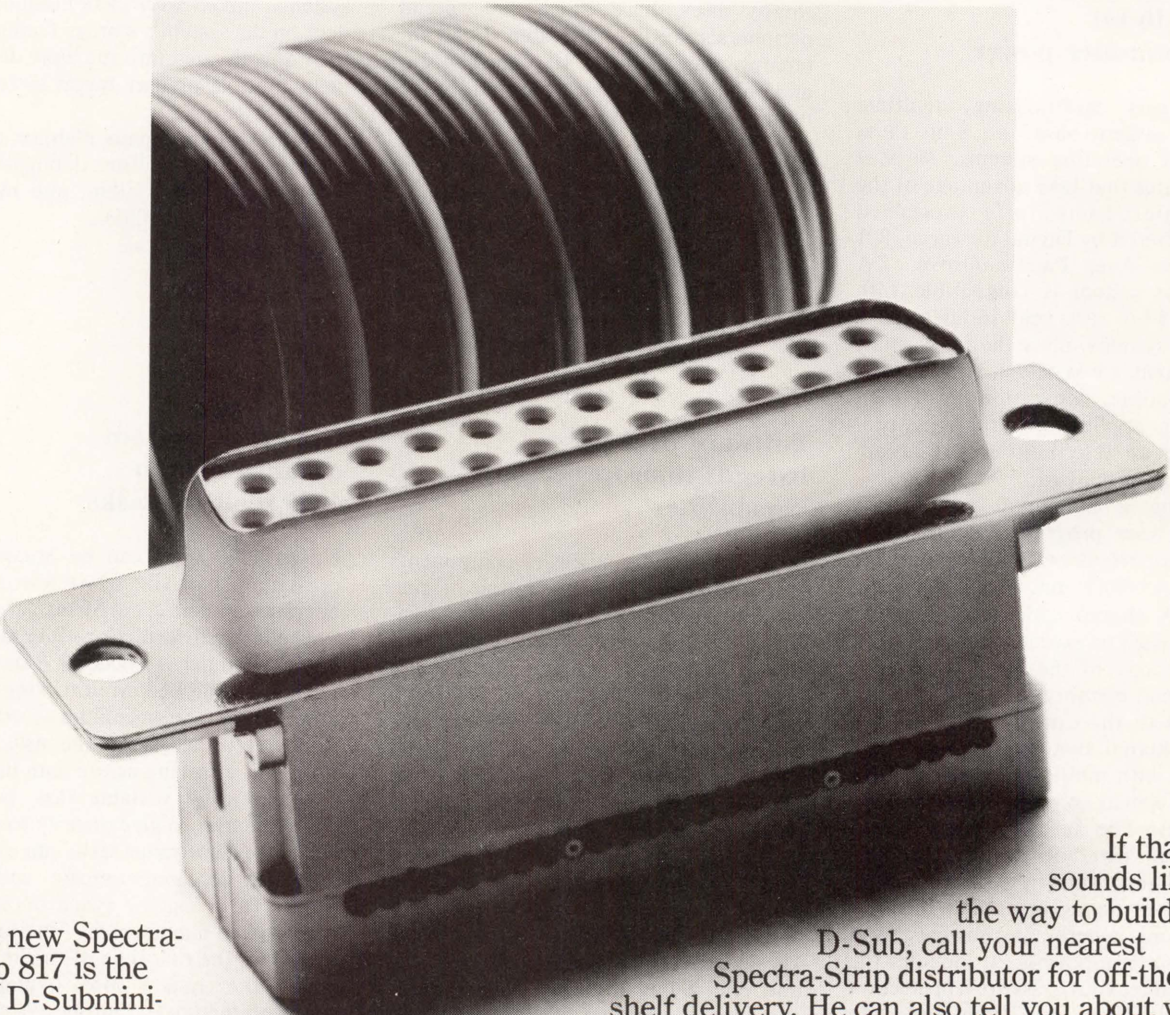
Z80 based video display terminal offers 10 programmable functions—IQ 130, from Soroc Technology, Inc, 165 Freedom Ave, Anaheim, CA 92801, incorporates screen editing, protected fields, multiple video attributes, and 10 programmable functions. Other features include a 25th status line with user message facility, adjustable righthand margin, and programmable blink and repeat rate. User selectable buffered print output is standard, utilizing printer port or auxiliary port at rates ranging from 110 to 19,200 baud.

Circle 422 on Inquiry Card

Priority interrupt controller offered for Z80 STD BUS systems—A priority interrupt controller for Z80 based STD BUS systems, model SB8303 accepts 16 discrete interrupt inputs from other STD BUS modules or external sources, prioritizes and masks the inputs, and implements a vectored interrupt sequence applicable to the target processor. The unit, offered by Micro/sys, Inc, 1353 Foothill Blvd, La Canada, CA 91011, implements the Z80 Mode 2 interrupt protocol, providing a unique vector for each of its 16 inputs; users can add STD BUS cards that do not support Z80 Mode 2 operation to their system and have them participate in Mode 2 protocol through the controller.

Circle 423 on Inquiry Card

D-Suberior



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SOFTWARE

Operating system utilizes 16-bit microcomputer power

A multi-user multitasking, realtime operating system based on 8-bit CP/M and MP/M operating systems, MP/M-86 adds features that take advantage of the 16-bit microcomputer's increased power. Offered by Digital Research, 801 Lighthouse Ave, Pacific Grove, CA 93950, the system is compatible with both the 8-bit CP/M and 16-bit CP/M-86 operating systems. Since the file formats of the system, CP/M, MP/M, and CP/M-86, are compatible, conversion from 8-bit single-user application programs running under CP/M to multi-user 16-bit applications is simplified.

Allowing a maximum amount of space for user programs, the compact system supports networking capabilities through CP/NET network operating system. A shared code facility allows multiple users to execute programs with only one copy of the object code resident in main memory.

Central to the operating system is a realtime kernel that supports multiple terminals with multitasking at each terminal, as well as concurrent CPU and I/O operations. The kernel allows realtime control of external devices and instrumentation. The file system is suited to database management and business applications where file security and reliability are important. It includes file and record lockout, password protection at the file level, and time and date stamps that record last access and modification. The file system manages up to 8G bytes of mass storage with both random and sequential file access.

"Standard I/O" supports console I/O and list device output mapping to disc files, queues, other consoles, or other list devices. Virtual consoles support true background tasks. The terminal message processor defines the format and syntax of commands entered by a user at a console, and is easily modified or rewritten for a custom environment.

Internal queue mechanisms support mutual exclusion, pipes, synchronization, and communication between multiple tasks. Monitors or simulators of other operating systems can operate under the system without affecting other tasks. I/O drivers can be changed to match various hardware configurations. Subroutines that interface consoles, floppy discs, hard discs, and special peripherals are field-alterable. Logic interrupt control uses a flag mechanism, and polling mechanisms are provided for noninterrupting devices.

A typical system occupies approximately 20k bytes of memory. A minimal version, supporting only the realtime portion of the system, occupies only 7k bytes of memory.

Circle 424 on Inquiry Card

Software package extends microprocessor capabilities

A set of modular software components that allows the implementation of customized operating systems for Z8001 (segmented) and Z8002 (non-segmented) CPUs, ZRTS 8000 realtime software is available from Zilog, Inc, 10340 Bubb Rd, Cupertino, CA 95014. The package extends the capabilities of the 16-bit Z8000 microprocessor, enabling it to manage realtime, multitasking applications via simple commands.

The package consists of the kernel, a small realtime multitasking executive program, and a language processor called the system configurator. The kernel provides a means of monitoring and controlling multiple events occurring in a realtime environment. It manages all major realtime functions, such as task synchronization, priority scheduling, intertask communication, realtime clock control, and interrupt handling. The kernel requires 4k bytes of memory that can reside in either P/ROM or RAM and can execute on the Z8001 and Z8002 development modules, or on any Z8000 based target system with a realtime clock.

Supporting a variety of target configurations, the system configurator allows the various components of the target system to be defined in high level terms via the ZRTS configuration language (ZCL). The language's free format syntax makes configuration commands highly readable and maintainable.

User application programs can be assembled and/or compiled on the company's ZDS, PDS, MCZ, or Z-LAB 8000 systems, linked with ZRTS modules resident on the system's storage facility, and then downloaded into the Z8000 development module or user target system for testing.

Future enhancements planned for the system include a realtime debugger, console handler, file system, and memory management capabilities.

Circle 425 on Inquiry Card

Operating system organizes up to 4096 realtime tasks

Up to 4096 tasks can be organized in realtime by the SMP-RMOS1S-A81 operating system from Siemens AG, Zentralstelle fur Information, Postfach 103, D-8000 Munich 1, Federal Republic of Germany. The Real Multitasking Operating System (RMOS) enables several tasks to be performed simultaneously, with a floppy disc serving as the data medium.

Dynamically variable task priorities allow the user to give priority to specific tasks. Asynchronous tasks can exchange messages to communicate with each other. Tasks can be synchronized with special time management functions.

Besides the CPU time of the individual tasks, the system also manages the resource memory. During system generation, memory systems are arranged into pools from which memory blocks of optional size can be requested and returned. The functional range of the system includes a file management system requiring the use of the floppy disc controller SMP-E341. The driver for the serial interface is a component of the I/O system for the display screen (terminal handler). Up to 256 files can be processed quasi-simultaneously, and an interactive debugger can be linked. In addition, the system offers a time of day clock function with calendar.

The operating system works with two boards: the SMP-E8 CPU board and the SMP-E303 cascadable interrupt and counter control board. Memory and peripheral boards are chosen to meet specific application requirements.

Circle 426 on Inquiry Card

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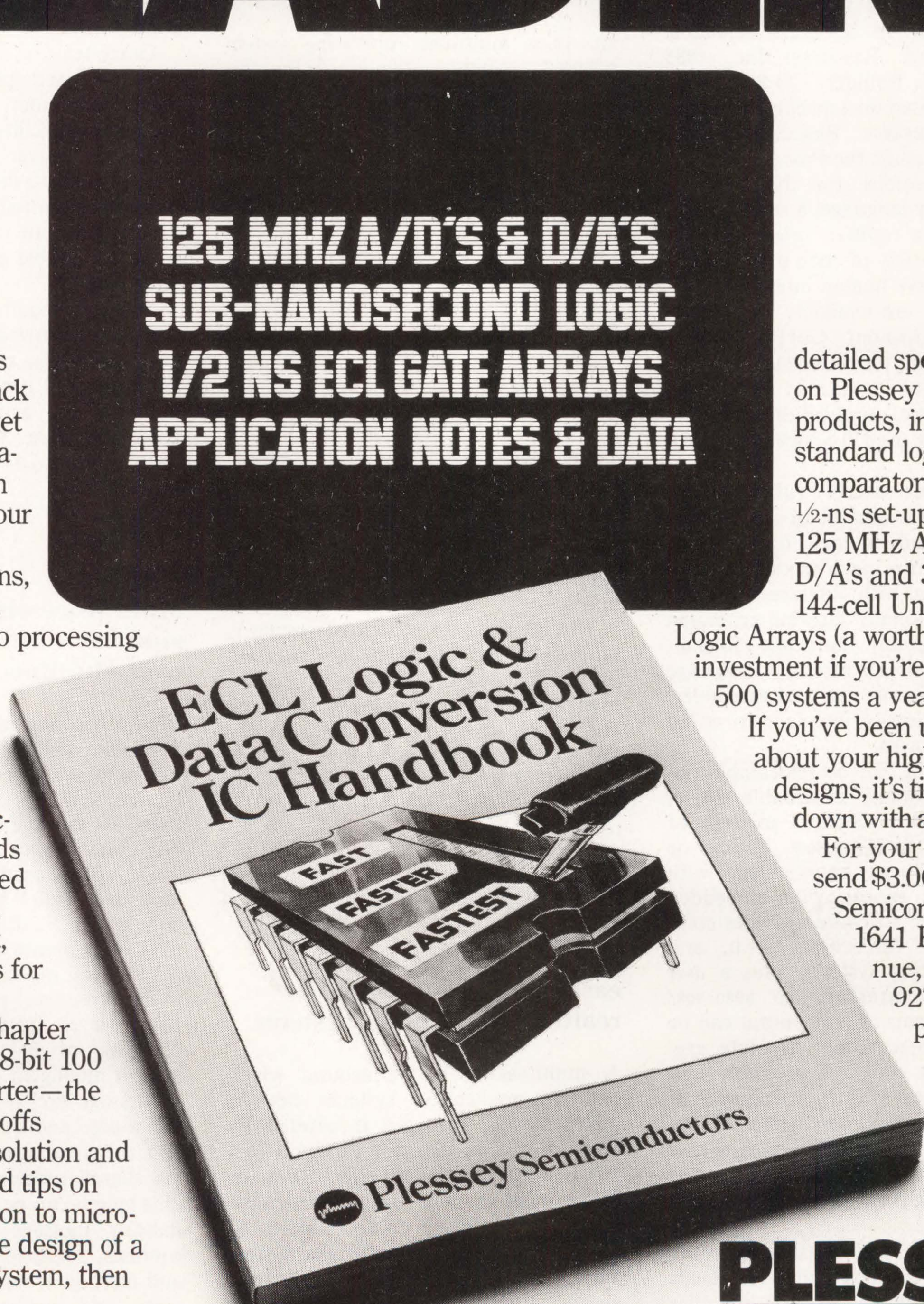

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CIRCLE 101 ON INQUIRY CARD

SOFTWARE

Pascal compiler systems speed development, ensure software portability

Compiler based PAS-80 and -86 series software development systems speed both the development of Pascal programs and their movement from one microprocessor to another. Available from Language Resources Inc, 4885 Riverbend Rd, Boulder, CO 80301, the systems are based on a machine independent, retargetable Pascal compiler system and include the Pascal compiler, a macro assembler for the universal AL/M assembly language, a runtime support library, a resolver subsystem that generates a variety of code outputs, and a comprehensive human interface.

Both series are available for use on Digital Equipment Corp's VAX-11 systems running the VAX-VMS operating system. The PAS-80 facility is used to develop 8080/8085 application software, while PAS-86 is used for 8086/8088 microprocessors.

The systems accept full standard Pascal, separate compilation of Pascal procedures and linkage to assembly language routines, and produce a compilation listing with interspersed error messages, optionally showing generated code in assembly language format. Features include an assembly language macro facility, a conditional assembler, and a user-friendly interface to speed development tasks.

PAS-80 output can be relocatable object code, absolute executable object code, interpretive code, a mixture of native and interpretive code, or assembly language source text with Pascal source appearing as embedded comments. The software provides complete support for CP/M, ISIS-II, and RMX-80 operating systems, plus a user configurable interface to 8080/8085 operating systems. PAS-86 output can be relocatable object code, absolute executable object code, or assembly language source text with Pascal source appearing as embedded comments. The interface to 8086 operating systems is user configurable, and CP/M-86, MTOS-86, and RS-86 operating systems are completely supported.

The runtime library interfaces to the target system. Code modules previously developed in FORTRAN, COBOL, or other specialized languages can be linked to code developed on the system. Utilities for selecting, binding, and locating the final programs are provided as well.

PAS-86 packages run on DEC VAX and PDP computers and on IBM System/370. PAS-80 runs on VAX systems.

Circle 427 on Inquiry Card

Multi-user capability supported without operating system patches

MULTI/os multi-user operating system offers the 8080/Z80 system user full multiuser capability without the need for user patching or configuration. The system, a product of InfoSoft Systems, Inc, 25 Sylvan Rd S, Westport, CT 06880, is compatible with applications software and languages that run under CP/M and CDOS and simultaneously supports various functions including word processing, data entry, inventory control, and order entry.

Based on the company's single-user I/OS, the system handles up to 16 simultaneous users, each with up to 56k bytes of user memory. It supports both floppy and hard discs, with a shared data base of up to 975M bytes of online data. An expanded directory capability allows a virtually unlimited number of files, and multiple disc controllers are supported without custom programming.

The interactively generated system is tailored for each hardware configuration on which it is used. The system can be used with memory banking or extended addressing, and can be set up in a turnkey mode. System provisions allow a network of single- or multi-user systems running MULTI/os and I/os, respectively, to be built.

Circle 428 on Inquiry Card

Multitasking software eases implementation of realtime application systems

A multitasking kernel around which realtime application systems can be built, RMS68K software is offered by Motorola Semiconductor Products Inc, PO Box 20912, Phoenix AZ 85036, for use in systems built around the VERSA module monoboard microcomputer of the MC68000 microprocessor. The system allows designers to implement systems without large expenditures for design and programming efforts on complex realtime and multitasking functions.

A task controller, an intertask communication facility, an initialization facility, and an optional memory management facility make up the system. These facilities receive all hardware and software interrupts and dispatch them to the proper task for processing, dispatch tasks competing for use of the microprocessing unit, provide intertask communication and synchronization, and manage and allocate memory. They also provide system initialization capability and diagnostic feedback during error conditions.

Other features include resource sharing using semaphores, fast interrupt response, timer options, exception monitoring facility, highly modularized functions, server task capability, and user-written I/O device driver capability. System generation capability allows the user to custom configure the system, while trace table capability eases system debugging.

Memory requirements depend upon the system environment, user-supplied code and data, and the functions configured in the system. If delay task and periodic task activation functions are used, a realtime clock is necessary.

Circle 429 on Inquiry Card

Multiprocessing software simplifies message exchange over Multibus

Multiprocessing and message exchange between multiple single-board computers attached to a common Multibus interconnect bus are simplified by the iMMX 800 package from Intel Corp, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123. Composed of a set of library modules that are linked to the company's realtime executives, the package supports the transportation and delivery of messages between applications programs running on different board level systems, simplifying the coupling of 8- and 16-bit masters, and/or intelligent slaves.

Message exchange software identifies the source and destination of messages and then manages the reliable transfer via shared memory. Messages of variable length can be passed. The software handles message to task connection routines, message buffer management, and message transport and delivery services, and implements the company's MULTIBUS interprocessor protocol.

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DATA STACK

SOFTWARE

Software/firmware packages support STD BUS for 8085 and Z80 based systems

A CP/M based operating system, relocatable macro assembler, and extended language package are offered by Intersil, Inc, Systems Div, 10710 N Tantau Ave, Cupertino, CA 95014, for their STD BUS product line for both 8085 and Z80 microprocessor based systems. All software is provided on 8" (20-cm), single-sided, single-density floppy diskettes.

Based on CP/M, the ICP/M operating system has a minimum memory requirement of 8k bytes and supports a file system using a maximum of 16 logical devices. It includes a text editor, assembler, debug, and batch operating mode.

IMAC relocatable macro assembler includes an assembler with comment blocks, a variable input radix, and an inclusion statement; a LINK-80 linking loader for loading relocatable modules; and a CREF-90 cross-reference facility that supplies an alphabetized list of all program variable names.

The package has a 14k-byte minimum memory requirement with the ICP/M operating system.

Extended program language packages include IBASI, an extensive implementation of BASIC for Z80 and 8085 systems, with an 8k-byte minimum memory requirement; IBASC, a single-pass BASIC compiler for optimized 8080 high speed machine code, with a 40k-byte minimum memory requirement; and IPASC, a Pascal system that features a compiler, linker, debugger, and disassembler, with a 52k-byte minimum memory requirement. IFORT provides all of ANSI FORTRAN X3.9-1966, with a 25k-byte minimum memory requirement when used with ICP/M.

Firmware packages include the IFMON monitor and the IFDEV firmware monitor system. IFMON provides for the control of STD systems which contain either an 8085 or a Z80 microprocessor. Minimum memory requirement is less than 2k bytes. The IFDEV firmware development system has a 12k-byte minimum EPROM requirement and consists of a ROM based resident monitor, assembler, and text editor. An assembly source file can be created and edited in memory, and the source can be assembled without destroying it. The assembled code can be debugged with the resident firmware monitor. □

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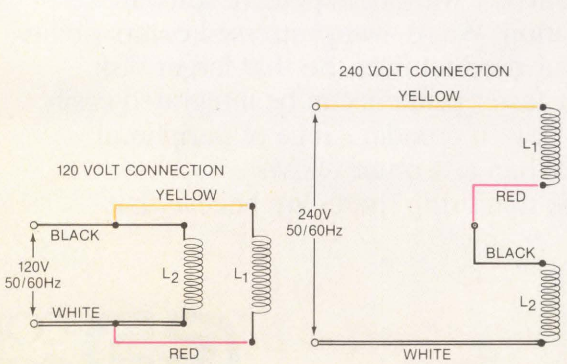

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ISL Gate Arrays Operate at Low Power Schottky TTL Speeds

Gerald R. Davis
Signetics Corporation
811 E Arques Ave, Sunnyvale, CA 94086

Until the late 1970s, implementing a system of many small and medium scale integration ICs with gate arrays was not cost effective because of the limits of IC complexity—limits that were largely imposed by photolithographic production capabilities. Gate arrays could not compete with the low cost per gate of standard logic. Instead, low power Schottky logic, the familiar 74LSXX series, was the technology of choice for the majority of designs. Uncommitted logic arrays, or gate arrays, became feasible as a general logic replacement when semiconductor processing improved to allow cost competitive LSI devices.

In 1978, at the Philips Research Laboratories, Eindhoven, The Netherlands, Jan Lohstroh developed a new circuit form utilizing standard Schottky processing to produce logic with the high packing density and low power consumption of I²L, but with the capacity to attain low power Schottky speeds. His invention was ISL, or integrated Schottky logic. The family of ISL gate arrays was subsequently created to reduce system size, power consumption, and cost. As soon as ISL was ready, Signetics Corp, with a few improvements, developed the 1200-gate, 52-buffer, 36-I/O 8A1200, the first of the ISL gate arrays. In 1980, the 8A1260 (1200 gates, 52 buffers, 60 I/Os) and the 8A1542 (1500 gates, 64 buffers, 42 I/Os) were added to the family. Since ISL has a worst-case maximum gate delay of 6 ns, functions made from these gates achieve low power Schottky TTL (LSTTL) performance.

ISL Gate Array Logic and Structure

The basic logic function of an ISL gate is that of an inverter. A 700 mV high level at the base of the NPN transistor produces a 500 mV low level on the output Schottky diodes. The passive resistor current source, attached to the base of a gate, also acts as a pullup resistor for the output of a previous gate. The PNP transistor associated with each gate is used to control the base charge on the NPN, keeping the NPN out of saturation and providing fast switching speeds. The gate may also be considered a single-input NAND function.

The power of NAND gate logic is amplified in ISL design because of the single-input multiple-output structure of the gate. All functions are constructed by using several gates and then inverting the AND. This AND requires no active devices. A single wire connects the diode outputs. This is more efficient than multiple-input NANDs since there is only one wire attached to the input of a gate. A regular 10-input NAND would require 10 wires to be attached to the input of the gate; in ISL gate arrays there is only one input wire. This characteristic is partly responsible for the high routability (wirability, gate utilization factor) of these arrays.

(continued on page 184)

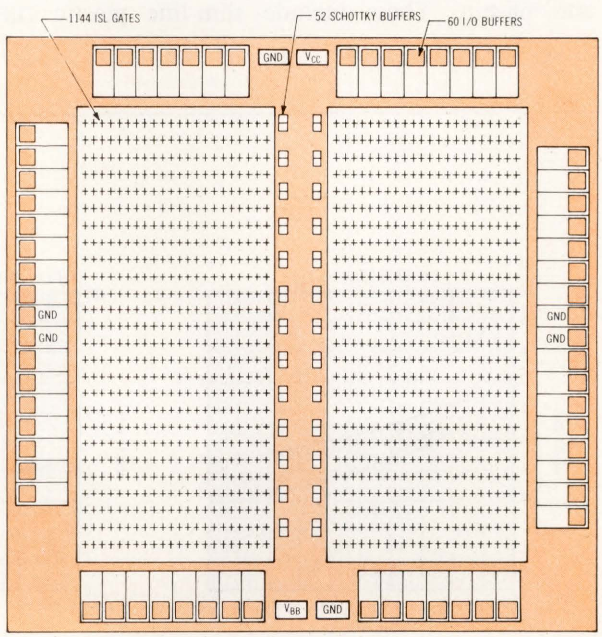

Fig 1 Configuration of 8A1260 ISL gate array. 60 I/O buffers and bonding pads occupy device perimeter. 1144 ISL gates are organized as 26 rows x 22 columns (x2). 52 Schottky buffers are placed in two vertical columns

ISL gates do not have fixed output collector contacts, which also contributes to their high routability. Each gate has five output contact sites available, even though only four can be used. The fifth was added to improve wirability. If one output cannot be easily reached, perhaps another one can be. What is most significant about these programmable output contacts is that they allow for routing metallization runs over unused outputs.

Because of their single-input multiple-output structure and programmable output contacts, ISL arrays, unlike other arrays, are not provided with dedicated routing channels. Since there are no dedicated routing channels (area of the die with no contributing active or passive devices), ISL gate array die areas are quite small, making high yields and low cost possible.

ISL Gate Array Features

Fig 1 shows the configuration of the 8A1260 gate array. Logic functions are defined by the user and are implemented by connecting 1144 ISL NAND gates using two layers of metal routing. Fifty-two Schottky buffers drive multi-load internal clock or enable signals. Sixty LSTTL I/O buffers are available. Each I/O can be configured to implement any of 11 functions, eg, inputs, I/O, totem pole, open collector, and 3-state. All inputs are standard PNP. The ISL family is available in a variety of packages: 22-, 28-, 40-, 44-, and 68-pin. These include slim-line plastic DIP, plastic/ceramic DIP, and leadless ceramic chip carrier. Typical performance characteristics of the ISL family are shown in Fig 2. Gate delays are a function of several variables, any of which influences the performance of the circuit.

Applications

Using a combination of appropriately configured NAND gates, any logic operation can be created: an 11-bit counter, a 17-bit shift register—anything. If desired, Boolean equations and DeMorgan's theorem may be used as design tools for implementing logic in NAND gates. Karnaugh maps or any design technique may be employed. If a favorite function is desired, it can be copied directly out of the *TTL Data Manual*. The efficiency of gate array design quickly manifests itself when functions are being copied. Often, unused operations are available in a standard logic part. For example, a 74LS161 4-bit synchronous binary counter has two enable lines, a load line, four data input lines, and a clear. Many applications do not require all of these functions, however, and in a gate array design, the unnecessary functionality can be eliminated. A 74LS161 has 62 gates, but a simple 4-bit synchronous binary counter can be created using only 47 ISL gates—a 32% improvement.

Higher speeds are obtainable. If the LSTTL speeds are too slow, special design techniques can be

(continued on page 186)

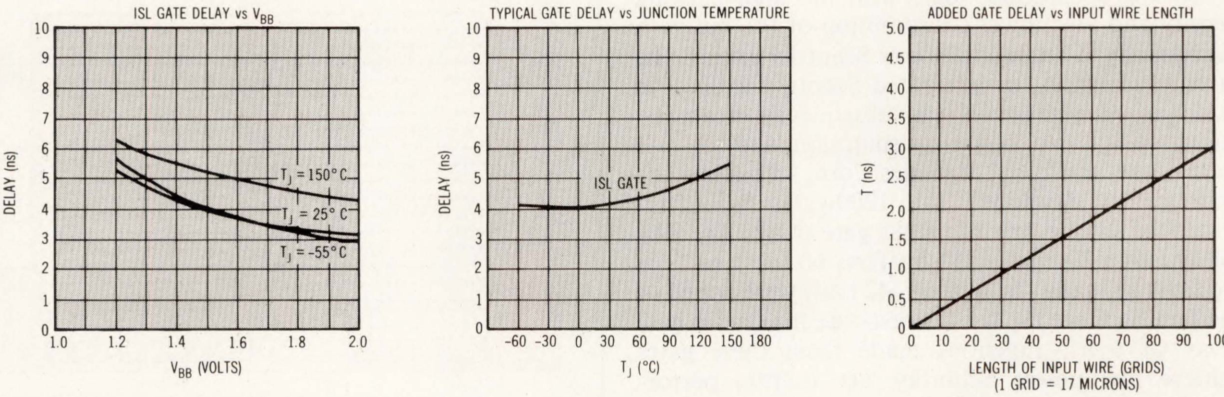

Fig 2 Performance characteristics of ISL gate array family. Overall performance is influenced by voltage and junction temperature. Interconnect wire increases gate delay

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CIPHER	CAELUS	CONTROL DATA	CENTURY DATA	CONTROL DATA	KENNEDY	DECITEK
CONTROL DATA	CENTURY DATA		CONTROL DATA	FUJITSU	PEREX	MICROPOLIS
DIGI-DATA	CONTROL DATA		BALL COMPUTER	KENNEDY	QUANTEX	PERTEC
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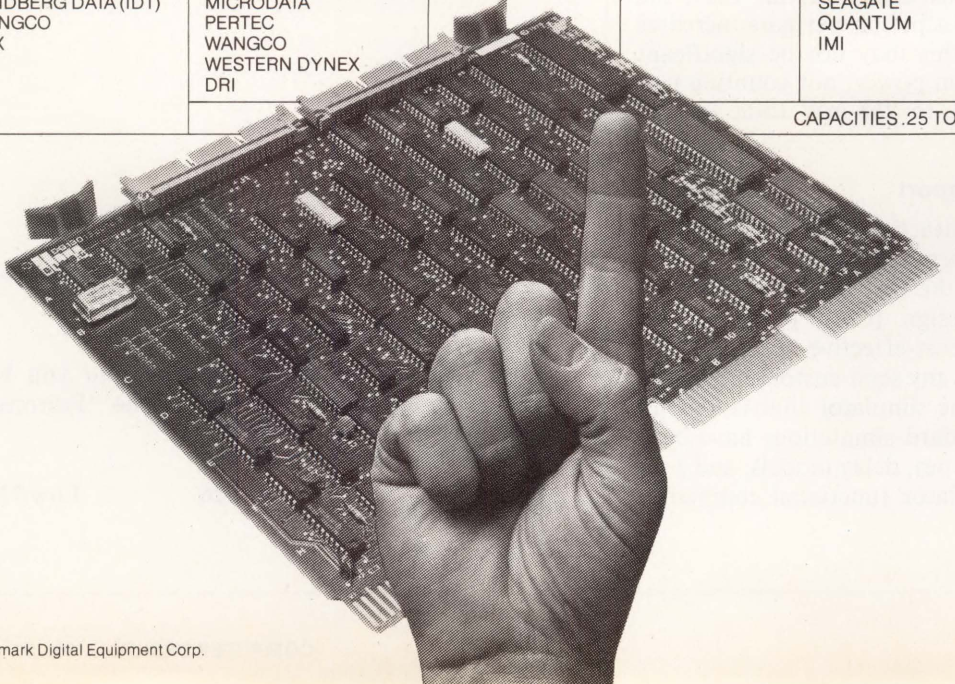

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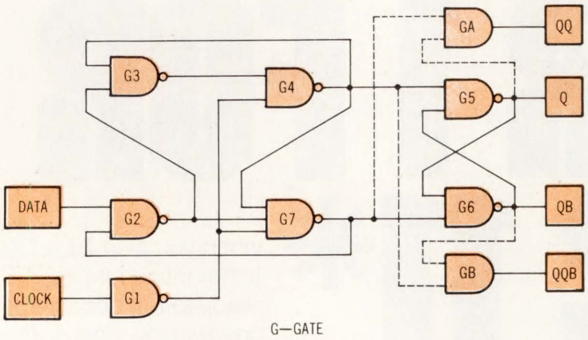

Fig 3 NAND gate diagram of D flipflop with quick Q and QB. Design reduces high to low propagation delay by 12 ns

employed in speed critical paths. Fig 3 shows a regular negative edge-triggered D flipflop with the addition of a feed-forward path for Quick Q (QQ) and QB (QQB) outputs. Gates GA and GB provide paths around the two crosscoupled latch output gates, eliminating two delays, which results in a high to low propagation delay for QQ and QQB that is 12 ns shorter than the standard Q and QB outputs.

A significant gate delay improvement can also be attained by raising the V_{BB} ISL gate power supply from the usual 1.5 V to 2.0 V. This reduces the maximum gate delay to about 4 ns, an improvement of 2 ns over the regular 6-ns delay. In this case, the typical 168-uW power dissipation per gate increases to about 224 uW. But this may not be significant since the typical maximum power, not counting I/O, would change from 200- to 268-mW total for the entire array of gates.

Design and Testing Support

The semiconductor manufacturer's responsibility in gate array design is to provide the user of uncommitted logic arrays with the best tools. A variety of computer automated design (CAD) programs are necessary to achieve a cost-effective solution. The first CAD tool required in any semi-custom integrated circuit project is the logic simulator that is used in design verification. Standard simulations have been created to include logic types, delay models, and a set of macros. All the simulator functional commands have been preprogrammed so that the only requirements for simulation are a redundant logic network description and input stimulus vectors to functionally exercise the design.

A logical design rule check follows the logic simulation. This check includes fan-in/fan-out and I/O violations. Two CAD programs have been developed to ensure that the designer drew the layout according to the design rules and that the layout is accurate. GASPAR, a symbolic placement and routing and design rule check program is then used. Next, a layout accuracy program called LATCH ensures that the layout of the logic network at the metal level is functionally identical to the simulation logic. Autoplacement and Route (available in late 1981) will use the simulation wire-list. Since in any auto-route program it will be necessary to finish the last few wire interconnections by hand, GASPAR and LATCH programs will still be useful CAD tools.

SENGEN, the automatic test generation program, also uses the logic simulation. This is not a vector generation program, but one in which the results of the logic simulation are translated into an LSI test system program that is used at E-sort and the final electrical test. By using a custom control file of ac tests defined by the gate array user, and with standard subroutine setups for usual dc tests, SENGEN reduces the time consumed by a task from weeks to a few minutes on the computer.

Summary

Low power Schottky speeds are easily attained with ISL gate arrays. Delay specifications can be improved by clever logic design or by increasing ISL gate power supply voltage. Moreover, ISL gate arrays provide efficient layouts and small die areas, with utilization as high as 75% to 95%. Layout and testing are supported by interactive CAD tools.

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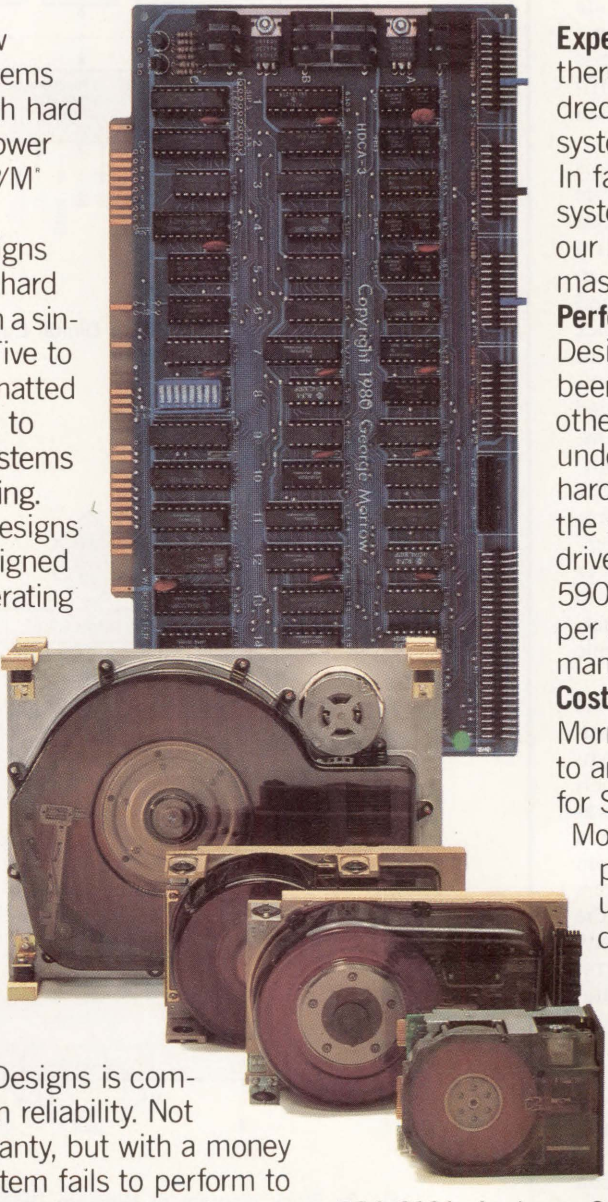

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BOART, DEUCE, and LIFO/FIFO ICs improve CPU-peripheral communications efficiency

Western Digital Corp, 3128 Red Hill Ave, Newport Beach, CA 92663, recently introduced three ICs dedicated to communications applications. Two of the devices are bus oriented asynchronous receiver/transmitters (BOARTS), one of which has dual-baud rate generators and dual-channel receiver/transmitter channels. The third device is a LIFO/FIFO designed to increase the efficiency of computer-peripheral data flow.

The first BOART, designated WD1983, is an N-channel silicon gate MOS/LSI device that interfaces a digital asynchronous channel with a parallel channel. It is a fully programmable microprocessor I/O peripheral with two control registers and a status register. Capable of full duplex operations, the device was designed to operate in an 8-bit microprocessor environment. Internal control is provided by two microcontrollers: one for transmit and one for receive. Control registers, modem control, logic, read/write control logic, and various counters provide input to the microcontrollers, generating the control signals necessary to send and receive serial data according to the programmed asynchronous format. (See Fig 1.) The 28-pin plastic or ceramic LSI is a 5 V only device.

The WD2123 DEUCE is claimed to be the first programmable LSI device to combine two independent full-duplex asynchronous receiver/transmitter channels and two independent baud rate generators in a single 40-pin package. The MOS part replaces two 28-pin and one 18-pin LSI devices. Designed for manufacturers of DP and peripheral equipment, the DEUCE allows simultaneous talk in any combination between CPUs, CRTs, printers, FAX machines, and digital PABXs from a single socket. Programming is identical to the WD1983 in the asynchronous mode, and the device can be interfaced to bus oriented microprocessors such as the Z80, 8080A, 8085, and the 6800.

Fabricated using N-channel silicon gate technology, the device merges two WD1983 BOARTs and one WD1941 baud rate generator. As shown in Fig 2, the channels are referred to as A and B. Channel A is addressed or controlled by the input signal CS1; channel B is similarly controlled by CS2. CS3 controls the baud rate generators.

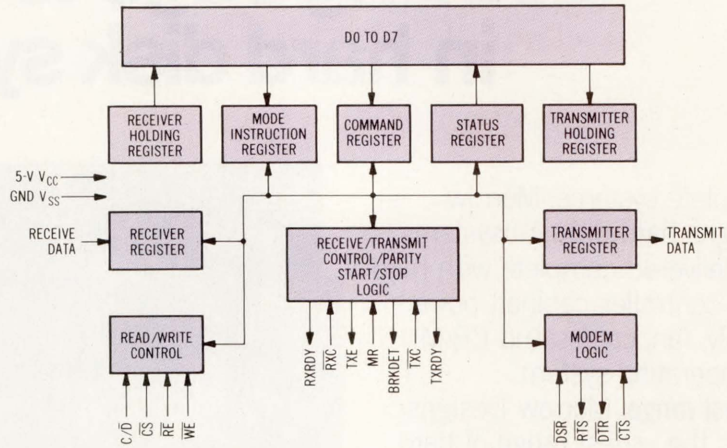

Fig 1 Block diagram of Western Digital Corp's WD1983 bus oriented asynchronous receiver/transmitter

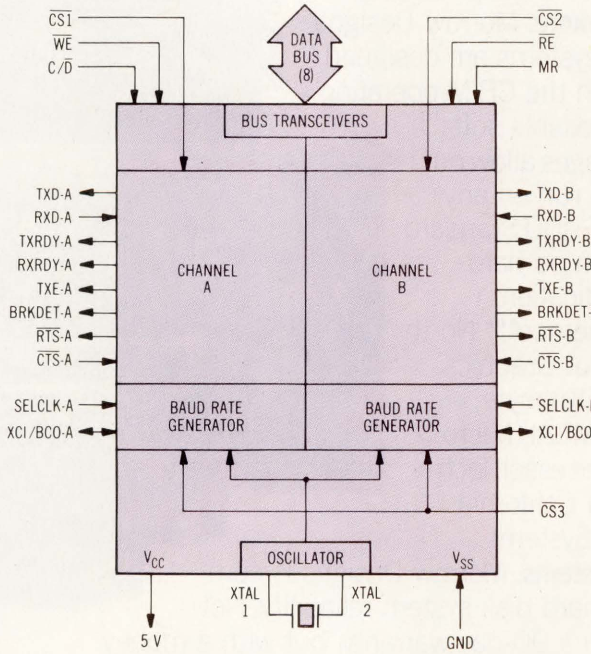

Fig 2 Block diagram of Western Digital Corp's WD2123 dual-enhanced universal communications element. Part contains two independent baud rate generators and two independent receiver/transmitter channels

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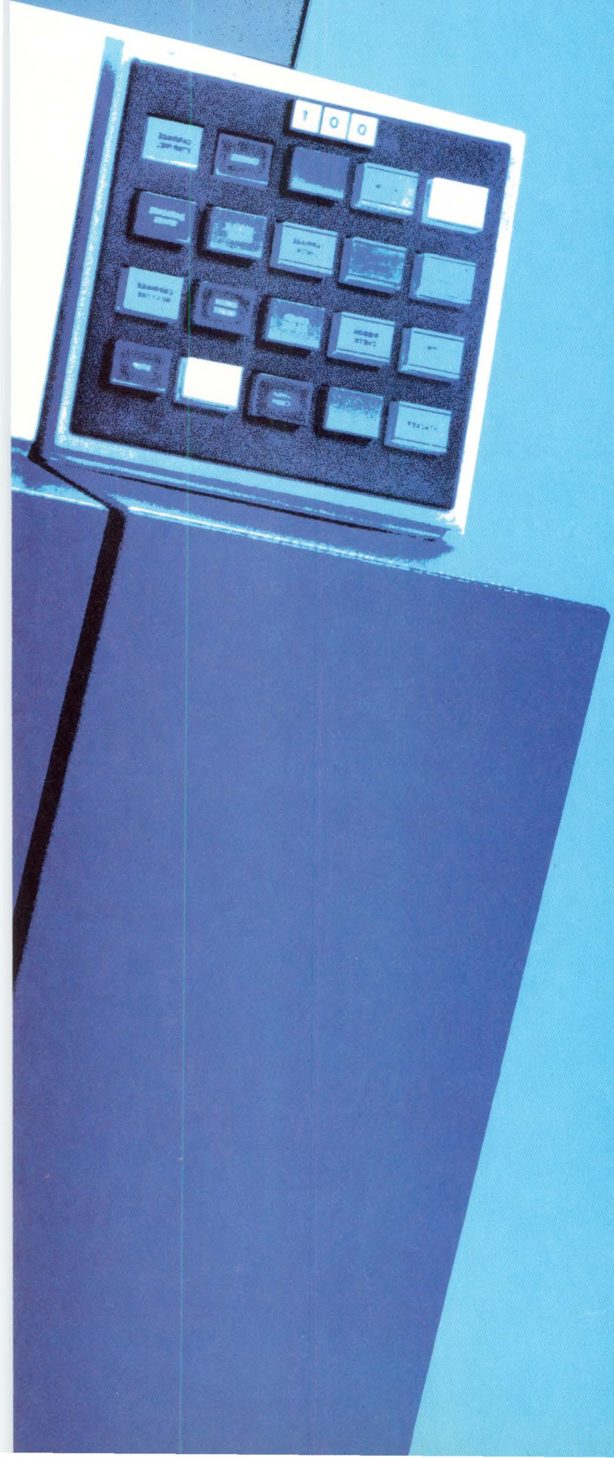

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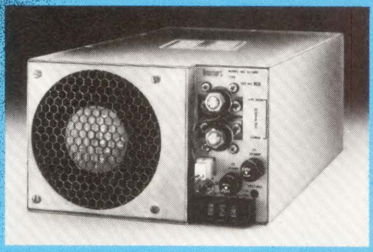

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Each channel can be programmed to receive and transmit asynchronous serial data. The WD2123 performs serial to parallel conversion on data characters received from an I/O device or a modem, and parallel to serial conversion on data characters received from the CPU. The CPU can read the status of either channel at any time. Status information on a per channel basis reported includes the type and condition of the transfer operations being performed as well as any transmission error conditions—parity, overrun, or framing.

The third part, designated WD1510, is an MOS/LSI memory buffer. Organized as a 9-bit by 128- or 132-word stack, the chip has two bidirectional data ports and may be read from or written into through either port. Thus, it can function as a LIFO from either port or as a FIFO with data flow from port A to port B or vice versa. The DIRECTION input pin is used to specify the data flow direction. The LIFO/FIFO is fabricated in 5 V only N-channel technology.

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Complementary N- and P-channel power MOSFETs are second sourced

Two series of complementary 6-A, N- and P-channel power MOSFETS, the ZVN02 and ZVP02, respectively, are suited for a variety of applications, including microprocessor and IC logic interface driving, motor control, sensing and timing circuits, power supplies, and frequency amplification. Manufactured by Ferranti Electric, Inc, Commack, NY 11725, the devices can be used to replace or second source the Supertex VN02 and VP02 series.

Utilizing the company's vertical DMOS process, with its compact interdigitated geometries, the devices have low input capacitance (less than 100 pF) and fast switching speeds (t_{on} less than 200 ns, t_{off} less than 40 ns). Both parts can be paralleled without base current sharing resistors and do not exhibit thermal runaway and thermally induced secondary breakdown.

Both series feature 10 voltage ratings from 20 to 200 V and drain current ratings up to 6 A. Each is available in TO-3, TO-39, and TO220 packages, and as arrays in 14-pin DIL packages (also available in chip form).

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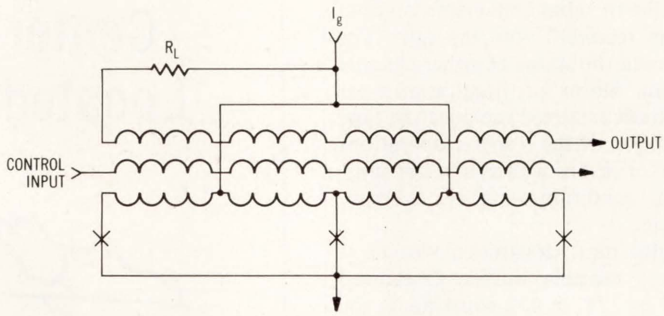
Submicron Josephson junctions fabricated



Feedback circuit implemented with Josephson junctions in procedure developed at Bell Labs. Output current of interferometer is fed back through control line. Selection of coupling of output current fed back to interferometer results in step function

A group of researchers from the Electronics Research Lab of Bell Labs, Holmdel, NJ 07733, have fabricated what are believed to be the smallest superconducting Josephson junctions ever made. Lawrence Jackel, Evelyn Hu, Richard Howard, Linus Fetter, and Donald Tennant have constructed a variety of small superconducting tunnel junctions and simple superconducting interferometer circuits using novel E-beam and optical lithographic techniques.

The Pb-oxide-Pb(In) tunnel junctions are made using self-aligning processes that involve multiple oblique evaporations through suspended liftoff stencils formed in 2-layer resist systems. Oxide barriers are grown in situ immediately after evaporation of base electrode films. Junction areas range from 10^{-9} cm^2 (optically patterned) to about 10^{-10} cm^2 (E-beam patterned). Current densities as high as 2 x 10^6 A/cm^2 have been attained. The high current density junctions show only small hysteresis at 4 °K and are completely non-hysteretic at higher temperatures.

Josephson junctions consist of three parts: two thin metal layers that act as electrodes, separated by an even thinner insulating layer. At very low temperatures, just a few degrees above absolute zero, the metals become superconducting, and electron pairs, as predicted by Josephson, are able to tunnel across the junction from one electrode to the other. By means of a control electrode, however, this no-resistance path can be changed to a high-resistance path, cutting off the electron flow. The junction, then, is really a switch that opens or closes depending on the state of the control electrode.

The Figure shows the configuration of a possible feedback circuit. Output current of the interferometer is fed back through one of its control lines. If an input signal in the other control line causes a reduction in the interferometer critical current to a value less than the bias current, output current will begin to flow in the feedback line. This feedback current again reduces the critical current, further increasing the output current. By proper choice of the coupling of the output current fed back to the interferometer, a step-function response can be obtained.

Four ADC series offer improvements in speed, accuracy, and capability

Four recently announced ADC lines claim significant improvements over previous designs. The first is a highly accurate 35-μs device. The second series includes two ADCs with display hold: one for LCDs, the other for LEDs. A third ADC offers 50-μs conversion in a hybrid package. The fourth is a low power video speed device.

High accuracy and fast conversion make the first ADC suited for applications in automatic test equipment, medical and nuclear instrumentation, pulse code modulation, industrial scales, and robotics. ADC1140 is specified for a max conversion time of 35 μs and a guaranteed max linearity of ±0.003% FSR. The 16-bit successive approximation ADC is manufactured by Analog Devices, Rte 1 Industrial Park, Norwood, MA 02062. Implemented in a 2 x 2 x 0.4" (5 x 5 x 1-cm) 32-pin package, device coefficients include: nonlinearity of ±2 ppm/°C, offset temperature of ±30 μV/°C, and gain temperature of 12 ppm/°C.

The ADC includes a 16-bit DAC, precision 10-V reference, a clock, a comparator, and input scaling resistors for pin selectable input voltage ranges of ±5 V, ±10 V, 0 to 5 V, and 0 to 10 V. The reference is available for external application. No external components are necessary for a ±0.003% accurate conversion.

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Two 3½-digit monolithic CMOS ADCs with display hold were also announced by Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94043. The ADCs hold a reading without change or flicker. 7116 is designed to interface with an LCD and includes a backplane drive. 7117 directly drives an LED display with 8 mA/segment. Both devices include 7-segment decoders, display drivers, reference, and a clock. Applications include digital voltmeters, digital panel meters, digital thermometers, digital bridges (strain gauges and load cells), portable instruments, multimeters, and digital process indicators.

A high performance panel meter can be built by adding a display, 4 resistors, 4 capacitors, and a single power supply. When assembled, the panel meter has a full scale as low as 200 mV with input noise less than 15 μV pk-pk. In addition, the auto-zero is less than 10 μV, zero drift is less than 1 μV/°C, input bias current is 10 pA max, and rollover error is less than one count. True differential input allows the measurement of bridge-type transducers such as load cells, strain gauges, and temperature transducers. 7116/7117 is offered in 40-pin plastic or ceramic packages.

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Complete with internal reference, clock, comparator, and laser-trimmed, thin-

(continued on page 194)

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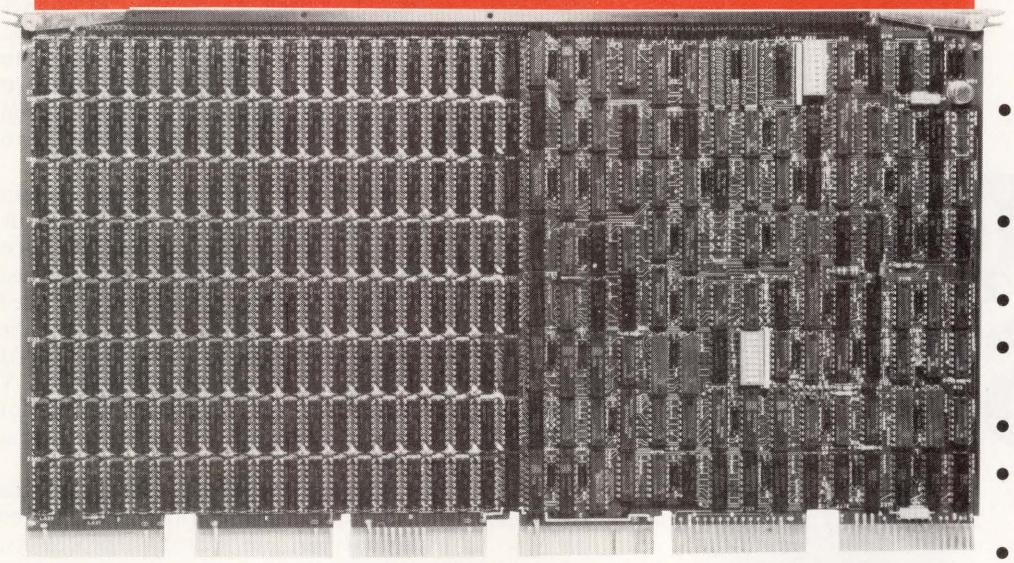

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The DR-144S is another industry first from Dataram. This 1.0MB semiconductor ADD-IN quadruples the size of 16K RAM-based ADD-INs available from either Digital Equipment Corporation (DEC) or ADD-IN memory suppliers.

Unlike other manufacturers, Dataram's ADD-IN memory for the PDP-11/44 uses a double word organization with ECC (32 data + 7 ECC) making it completely software compatible with DEC's memory diagnostics. A Mother Board and two Array Boards are joined together by pluggable pins (as shown below) to provide the 1.0MB DR-144S system.

The Mother Board is the only board of the DR-144S assembly which interfaces to the host PDP-11/44. This means that there is only one unit load and that 1.0MB power requirements are dramatically reduced compared to the approach of using four separate 256KB modules. Also, the DR-144S current drains are much lower in the battery backup mode.

The DR-144S is available with only the Mother Board and in versions including one or two array boards. The DR-144S Mother Board provides a capacity of 256KB. The DR-144S Mother Board with one array board is 512KB; with two array boards, the DR-144S capacity can be either 768KB or 1.0MB.

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Side view of Dataram's 1.0MB DR-144S

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film, scaling resistors, the third type, ADC72, is a hybrid, 16-bit resolution successive approximation ADC packaged in 32-pin metal DIP. Six analog input ranges of ±2.5 V, ±5 V, ±10 V, 0 to 5 V, 0 to 10 V, and 0 to 20 V can be selected. Max conversion speed is 50 μs. The TTL compatible device is manufactured by Burr Brown, PO Box 11400, Tucson, AZ 85734.

Applications are seen in analytical instruments and clinical analyzers where high resolution and accuracy are critical requirements. In automatic test equipment 14-bit accuracy permits testing of 10- and 12-bit parts. Four models are available. ADC72AM has a non-linearity of ±0.006%, while -BM has a non-linearity of ±0.003%. Both operate over a −25 to 85 °C range. Non-linearity of the -JM and -KM devices is ±0.006% and ±0.003% FSR, respectively, and they operate over a temperature range of 0 to 70 °C.

Circle 445 on Inquiry Card

Finally, CA3300 is a video speed ADC manufactured by RCA/Solid State Div, Route 202, Somerville, NJ 08876. CMOS technology allows sampling rates as high as 15 MHz with 66-ns conversion time attained with power consumptions below 200 mW. The ADC is therefore suited for applications where low power consumption is as important as speed. Operating from a single dc supply of 3 to 12 V, the ADC develops a 6-bit latched 3-state output with an overflow bit and two "chip enables" at an accuracy to within ±0.5 LSB.

CA3300 operates over a dynamic input voltage range from 2.5 V up to the dc supply voltage with typical low CMOS power consumptions. When operated from a 5-V supply at a clock generated sampling frequency of 11 MHz, the power dissipation is less than 50 mW. At a sampling frequency of 15 MHz, an 8-V supply is required, and the amount of power consumed increases to about 180 mW.

The high conversion rate makes the ADC suited for digitizing high speed signals that are routed to processors, display drivers, and other instruments, such as radar-pulse or ultrasound-signal analyzers, motion and transient-signal detectors, charge and time digitizers, and CRT displays. The overflow bit allows the connection of two or more of the devices in series to increase the resolution of the conversion system. A series connection of two devices may be used to produce a 7-bit high speed converter. Operation of two ADCs in parallel doubles the conversion speed, ie, increases the sampling rate from 15 to 30 MHz.

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4k and 16k Schottky P/ROMs are fast and reliable

Implemented in advanced Schottky process technology and employing titanium-tungsten fuses, a family of 4k and 16k P/ROMs offers fast access times with high reliability. Both P/ROM families, produced by National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, share a common programming algorithm. (continued on page 196)

Oak puts E^3 up against the world's fastest typists.

In a keyboard market clogged with claims and confusion about "N-key-rollover," look to Oak's FTM® keyboard for the practical answer. It provides E^3-Entry Error Elimination. And that means precisely what it says. We challenge the fastest typists in the world to make it error. They can't.

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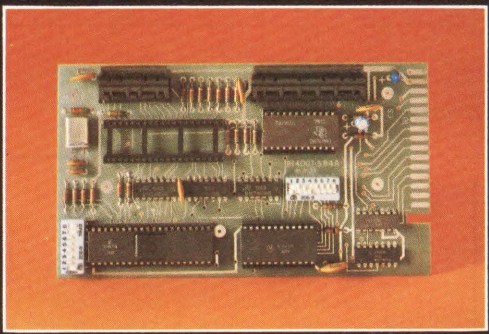

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CIRCLE 114 ON INQUIRY CARD

The 4k P/ROM family is available in both 512 x 8 and 1024 x 4 versions, all having open collector and TRI-STATE[R] outputs. The 16k P/ROM is a 2048 x 8 device with address access times of 65 ns max for the commercial temperature range, and 80 ns for the military temperature range. Power dissipation is typically 600 mW. The 4k P/ROMs are available in military and commercial temperature ranges in 20- and 24-pin plastic or ceramic packages; 16k devices are available in 24-pin plastic commercial or ceramic military packages.

To accommodate testing, the Schottky P/ROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests and in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to verify operation of the row and column select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

20-pin, 512 x 8 devices in plastic are designated DM74S472/473AN and in ceramic, DM54S472/473AJ, while 1024 x 4 devices in plastic are DM74S572/573AN and in ceramic, DM54S573/574A. 24-pin, 1024 x 8 P/ROMs in plastic are numbered DM74S474/475A and in ceramic, DM54S474/475A, and 2048 x 8 P/ROMs in plastic are DM87S190/191N and in ceramic, DM77S190/191J.

16,384-bit bipolar P/ROM has 35-ns access time

Ten recently announced electrically programmable Schottky ROMs are organized in the industry standard 2048 x 8 configuration. Five of the parts are offered in the industry standard 600-mil, 24-pin DIP: the Am27S190/191, the faster Am27S190A/191A, and the power switched Am27PS191. An equivalent series designated Am27S290/291 are available in high density 300-mil, 24-pin DIPs. Standard parts have an access time of 50 ns. "A" versions are guaranteed to have a max access time of 35 ns. The Am27S190 and Am27S290 have open collector outputs, while the Am27S191 and the Am27S291 offer 3-state outputs. The P/ROMs are manufactured by Advanced Micro Devices, 901 Thompson Pl, Sunnyvale, CA 94086.

High reliability is a result of 100% MIL-STD-883C assurance testing. The devices are members of the company's advanced P/ROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

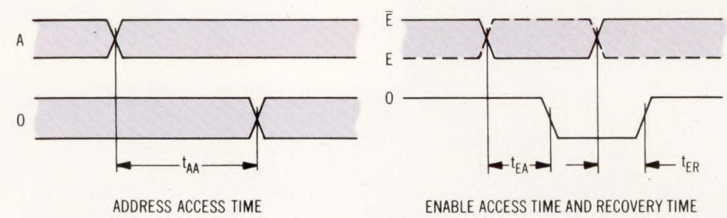
All parts are fabricated with reliable platinum-silicide fuse technology. Utilizing easily implemented programming (and common programming personality card sets), these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to ensure high field programming yields and produce high parametric correlation.

Common design features include active loading of all critical ac paths regulated by a built-in temperature and voltage compensated bias network. Selective feedback techniques have been employed to minimize delays through critical paths.

The devices are manufactured using the company's selective oxidation process, IMOX II[TM]. This advanced process combined with a merged fuse array permits an increase in density and a decrease in internal capacitance, resulting in the fastest possible P/ROMs.

Circle 447 on Inquiry Card

8k P/ROM access time reduced to 55 ns



Waveforms of Monolithic Memories Inc's 6381-2 P/ROM. Logical high is stored and low state is programmed. Address access time (t_{AA}) is on left. Enable access time (t_{EA}) and recovery time (t_{ER}) are on right

A high speed 8k P/ROM with an access time of 55 ns is available from Monolithic Memories Inc, 1165 E Arques Ave, Sunnyvale, CA 94086. Designated 6381-2, the device is 40% faster than its predecessor, the 6381-1. Implemented with 2-μm line resolution, in comparison to 4 μm for the -1, the -2 is also 25% smaller than the earlier part.

The P/ROM features low current PNP inputs, full-Schottky clamping, and 3-state and open collector outputs. Nichrome fuses store a logical high and are programmed to the low state. Special onchip circuitry and extra fuses provide preprogramming tests that ensure high programming yields and high reliability.

The 3-state devices are identified as 6381-2 and 5381-2; those with open collector outputs are known as 6380-2 and 5380-2. All are organized as 1k by 8 and have industry compatible pinouts.

The 6381-2 and 5381-2 have access times of 55 ns and 70 ns, respectively; while the 6380-2 and 5380-2 have access times of 70 ns and 90 ns. The address access, enable access, and recovery time are shown in the Figure. Because of their speed, the devices are ideal for microprogram store, lookup tables, programmable logic elements, and character generators. All the devices are available in either a 0.3" (0.8 cm) wide SKINNYDIP[TM] or a standard 0.6" (1.5 cm) wide 24-pin package.

Circle 448 on Inquiry Card

Retro-Graphics,™ TI Style. Strong Gets Stronger.

It just makes sense. If you can successfully marry *two* strong ideas, the result will almost assuredly be *one* stronger idea. Example—Texas Instrument's recently introduced OPTI 900™ Model 940 Electronic Video Terminal. Clearly, the Model 940 fits the "strong idea" mold, combining the power of an editing terminal and the convenience of video display.

But what makes strong stronger here is an idea of ours. The idea is the Retro-Graphics enhancement, an idea that adds one impressive feature to TI's Model 940—*graphics.* Full-featured graphics. With complete emulation of Tektronix® 4010 Series terminals. With two graphics bit planes for multiple intensity levels or multiple pages of graphics display. With arc drawing, vector drawing, and point plotting capabilities. With area fill, selective erase, and an enhanced text mode. With an interactive cross hair cursor and an optional light pen. And, of course, complete compatibility with industry-standard graphics software, including ISSCO's® DISSPLA® and TELLAGRAF® and Tektronix PLOT 10.™

Strong get stronger. It's a fact that Retro-Graphics has proven time and again. With Lear Siegler's Dumb Terminal® displays. With DEC's™ VT100™ terminal. And now, with the Model 940, TI's self-proclaimed "screen star," Retro-Graphics is making it shine just that much brighter.

DIGITAL ENGINEERING
630 Bercut Drive, Sacramento, CA 95814
(916) 447-7600 TWX: 910-367-2009

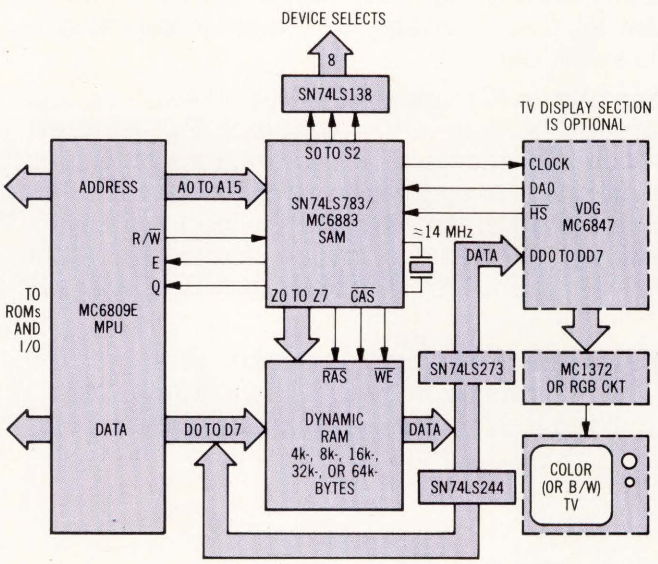
Synchronous address multiplexer simplifies memory to microprocessor interface

A recently announced synchronous multiplexer, SAM, combines the MC6809E microprocessing unit (MPU), the MCM6849 color video display generator (VDG), and a dynamic RAM to form a compact computer and display system. (See the Figure.) Designed to end contention problems in systems in which several microprocessors or peripherals share a single memory, the SAM replaces 40 gates, 35 MSI packages, and an oscillator package. Designated SN747LS783/MC6833, the part is offered by Motorola Semiconductors, PO Box 20912, Phoenix, AZ 85036.

The SAM is capable of handling 4k to 64k dynamic or static RAMs and has an addressing range of 96k. Although the device may be used as a dynamic RAM controller without a video display, most applications are likely to include a MC6847 video display generator. To minimize the number of RAM and interface chips, both the MPU and VDG share common dynamic RAM. Yet, the use of common RAM creates an apparent difficulty: the MPU and VDG must both access the RAM without contention. This difficulty is overcome by taking advantage of the timing and architecture of the company's MPUs.

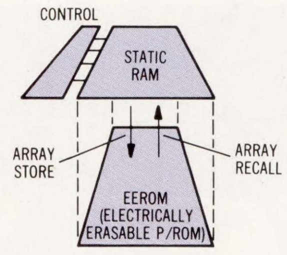
For most applications, the SAM can supply complete system timing from its onchip precision 14.31818-MHz oscillator. This includes buffered MPU clocks (E and Q), VDG clock, color subcarrier (3.58 MHz), row address select ($\overline{RAS}$), column address select ($\overline{CAS}$), and write enable ($\overline{WE}$). Encapsulated in a 40-pin ceramic or plastic package, the device operates from a 5-V supply. Typically, the SAM draws 180 mA (to 230 mA max).

Circle 449 on Inquiry Card



System block diagram of Motorola Semiconductors' asynchronous address multiplexer. Device includes MPU, color video display generator, and dynamic RAM

64 x 4 and 256 x 4 nonvolatile static RAMs allow in-system programming



Memory organization of Xicor, Inc's nonvolatile static RAM. Transfer of RAM data to EEROM is controlled by low logic STORE signal. Low level ARRAY RECALL signal copies data back to RAM

The industry's first 5-V programmable nonvolatile static RAM (NOVRAM), the X2201 1024 x 1 device, has been joined by two recently announced companion NOVRAMs—the 256-bit (64 x 4) X2210 and the 1024-bit (256 x 4) X2212. The devices are manufactured by Xicor, Inc, 851 Buckeye Court, Milpitas, CA 95035.

NOVRAMs provide in-system programmability with 5-V operation and N-channel, floating gate MOS technology. In the normal operating mode, the NOVRAM functions as a conventional static RAM with a 300-ns max cycle time. In case of power failure, the user's data are saved by transfer to an onchip nonvolatile memory EEROM. The data can be stored indefinitely, without power, and can be brought quickly back into RAM whenever necessary. The entire data array can be stored in 10 ms. Moreover, since it requires no more than 5 V to perform all functions, the NOVRAM allows onsite reprogramming without the need for previously required unsocketing, high voltage, or ultraviolet light sources.

The 4-bit wide I/O data configuration makes the two devices well suited for use in smart terminals, metering systems, instrumentation, process control, and data processing systems. NOVRAMs also are suitable in applications where it is desirable to allow user configuration of a product. For example, NOVRAMs can replace DIP switches to set mode and status parameters in terminals and are also suitable for applications where parameters change over time but require permanent storage.

Circle 450 on Inquiry Card

NMOS 128k ROM in 28-pin package

Organized 16,386 words by 8 bits, a recently announced ROM has a typical access time of 250 ns and a maximum access time of 450 ns over 0 to 70 °C. The device requires a single 5-V supply. Active power consumption is 120 mA. In the standby mode, power consumption is 20 mA. Compatible with the Intel 2364, MSM 38128 features a power-down state and is non-clocked so that it can be used in asynchronous applications. All inputs and outputs are TTL compatible.

Designed for large ROM applications such as intelligent typewriters, word processors, communications systems, voice synthesizers, and language translators, the ROM is available from OKI Semiconductor, Inc, 1333 Lawrence Expy, Suite 401, Santa Clara, CA 95051. A CMOS version, well suited for low power applications, is due shortly. Packaging is a 28-pin plastic DIP. It is pin compatible with JEDEC Version B.

Circle 451 on Inquiry Card

Op amp series introduced by three companies

Three recently introduced operational amplifier series include: a low noise, high speed device; two high voltage high current types; and a bipolar part. OP-27 from Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara 95050, offers a peak to peak noise of only 80 nV in the 0.1- to 10-Hz bandwidth combined with an offset voltage of 10 μV, a slew rate of 2.8 V/μs, a gain bandwidth of 8 MHz and a long term drive of 0.2 μV/month. The low noise, high speed, and precision characteristics of the device make it useful in audio preamp circuits, instrumentation, ultraprecise voltage threshold detectors, comparators, stable integrators, and precision summing amplifiers. Modeled after the OP-07, the first high precision, low noise op amp IC available, the OP-27 has about one-third to one-fourth the noise voltage of the OP-07.

Other key specifications for the OP-27 include a max input offset voltage of 25 μV for A/E suffix devices, 0.2-μV/°C offset drift with temperature, voltage gain of 1.8 M, and common-mode and power supply rejections in excess of 120 dB. OP-27 is available in 8-pin dual-inline packages and in 8-pin TO-99 cans. It is offered with a −55 to 125 °C or a −25 to 85 °C temperature range and three grades of electrical specifications.

Circle 452 on Inquiry Card

Two high voltage, high current op amps designed to drive up to ±150 mA into resistive, capacitive, and inductive loads were introduced by Apex Microtechnology Corp, 1130 E Pennsylvania St, Tucson, AZ 85714. In typical applications, they power high voltage motors, actuators, coils, or transducers, and may also be used as precision programmable power sources or for accurate analog simulation circuits. The max available output power is a function of the load but can be as high as 42 W into a resistive load when using a single power supply. Internal thermal resistance is 6.5 °C/W from junction to case allowing for a max internal dissipation of 26 W at Tj = 200 °C. To meet safe operating area criteria with any load, the current limit is externally programmable using two resistors.

Designated PA08 and PA08A, the op amps can operate with dual supplies between ±15 and ±150 V and with single supplies from 30 to 300 V. Specifications include a slew rate of 30 V/μs and gain bandwidth of 5 MHz. Input offset is ±1 mV for the PA08 and ±0.5 mV for the PA08A. Input bias current is 5 pA for PA08 and 3 pA for PA08A.

The hybrid integrated circuits utilize beryllia (BeO) substrates, thick film resistors, ceramic capacitors, and silicon semiconductors to maximize reliability. Ultrasonically bonded aluminum wires help ensure reliable interconnections at all temperatures. The 8-pin TO-3 package is isolated from internal circuits.

Circle 453 on Inquiry Card

Model 9918 from Optical Electronics Inc, PO Box 11140, Tucson, AZ 85734, is a bipolar, differential input, single-ended hybrid output op amp. It features a fast settling time with high slew rates. The wide bandwidth, low propagation delay of 5 ns and straight forward compensation make this device easy to stabilize. Features of the Model 9918 are: ±1% settling time of 20 ns, 200-MHz minimum unity gain frequency, ±300-V/μs minimum slewing rate, and ±5-V minimum voltage swing into a 100-Ω load.

The operating temperature range is −55 to 85 °C. Packaged in a standard 24-pin DIP, the device is functionally equivalent to the Teledyne Philbrick 1435.

Circle 454 on Inquiry Card

Video timer and controller generates CRT timing signals

An N-channel silicon gate COPLAMOS[R] MOS/LSI video timer and controller contains the logic to generate all of the timing signals for the presentation and formatting of interlaced and non-interlaced data on a CRT monitor. The latest member of Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge, NY 11787, VTAC[R] CRT controller family, CRT 5057 synchronizes its vertical refresh rate to a 50- or 60-Hz line frequency, thereby eliminating the "swim" phenomenon caused by line frequency variations.

The device is well suited for European system requirements. Combining CRT 5057 with the company's CRT 8002 video display attributes controller provides all of the video electronics for a CRT terminal.

Circle 455 on Inquiry Card

High speed 5 V only 16k static RAM

MB8167 is a high speed, 5 V only, 16k x 1 static RAM. Pin compatible with Intel's 2167, the RAM features an access time of 70 ns, fully static operation, max power consumption of 180 mA, separate data I/O, TTL compatibility, 3-state output with OR-tie capability, chip select for simplified memory expansion, and automatic power down. Manufactured by Fujitsu Microelectronics, 2945 Oakmead Village Court, Santa Clara, CA 95051, it is suited for applications requiring high speed, low power dissipation, and low cost. The RAM is implemented in a 20-pin DIP.

Circle 456 on Inquiry Card

8k RAM is compatible with 2716 EPROM—Designated the 8112, a recently announced static RAM is pin-for-pin compatible with the 2716 EPROM. This allows the RAM to be used in software development with the elimination of erasing and reprogramming. Organized 1024 x 8 bits, the 8112 from GTE Microcircuits, 2000 W 14th St, Tempe, AZ 85281, provides common input/output pins for connection to a data bus. It is available in 200-, 300-, and 400-ns standard and low power versions and requires a single 5-V supply. The 8k unit is available in plastic and cerDIP packaging. Circle 457 on Inquiry Card

20- and 40-V semicustom arrays offered—Ten semicustom arrays rated at 20 V maximum and three at 40 V maximum, without metal pattern delineation and requiring packaging, are in inventory at Micro-Circuit Engineering, Inc, 1111 Fairfield Dr, West Palm Beach, FL 33407. Upon receipt of a metallization diagram, the company will provide the final metal masking step, package and test the circuits, and ship evaluation quantities, all within five to seven weeks.

The 20- and 40-V circuits offer 20-, 100-, and 200-mA NPN transistors, lateral and vertical PNP transistors, Schottky diodes, and a selection of diffused resistors.

Named UNIRAYs™, the devices can be adapted for applications such as interface circuits, oscillators, biasing circuits, voltage regulators, amplifiers, comparators, and active filters, as well as a number of other IC functions.

Circle 458 on Inquiry Card

Asynchronous communications interface adapter second-sourced—S6551 asynchronous communications interface adapter is offered by American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, with an onchip baud rate generator for the 6500 and 6800 microprocessor families. A second source to Synertek's SY6551, the device requires a 1.8432-MHz crystal as an external component to provide serial communications and modem capability for the 6500 and 6800 families. Rates of 50 to 19,200 baud can be derived.

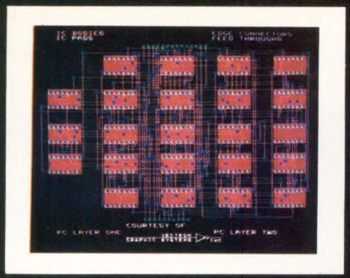
Available in 28-pin plastic or cerDIP packages, the S6551 includes a programmable interrupt and status register, and an 8-bit bidirectional data bus. Full- or half-duplex operation is provided.

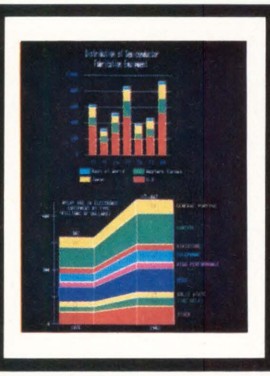
Circle 459 on Inquiry Card

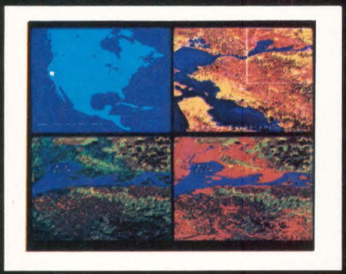
16k static RAM faster—A 45-ns version of the IMS1400 static 16k x 1 RAM was recently announced by Inmos Corp, PO Box 16000, Colorado Springs, CO 80935. Housed in a standard 20-pin, 300-mil (7.6-mm) wide package, and requiring a single 5-V supply, the device consumes 660 mW maximum and is 10 ns faster than its previously announced companion RAM.

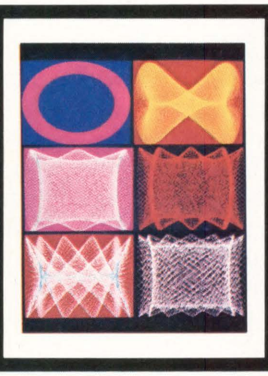
All inputs and the output are TTL compatible. The memory has equal access and cycle times. A chip enable pin is provided which, when taken high, automatically puts the chip in a low-power standby mode.

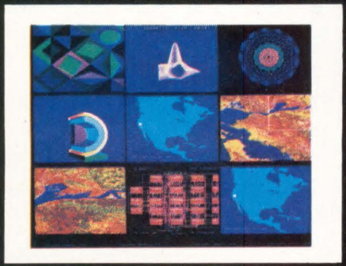
Circle 460 on Inquiry Card











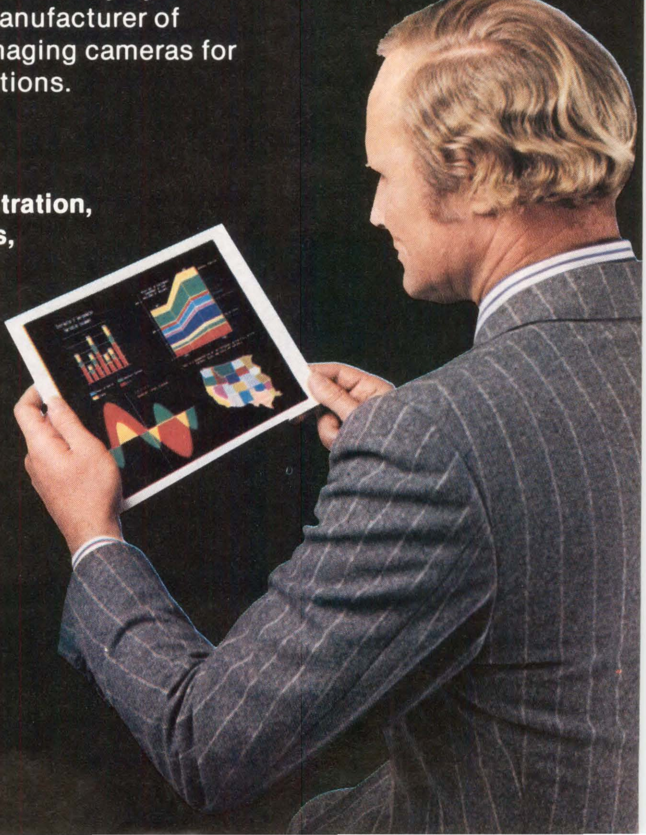
Color Graphics Hard Copy... Made Easy

The Matrix Color Graphic Camera System converts the output of any raster scan computer color terminal into brilliant, high resolution photographic hard copy. Both line and continuous tone images can be made with accurate, bright, saturated colors.

Our system does what no other instrument can do — it produces instant, on-the-spot results with Polaroid® 8 x 10 film, 8 x 10 color transparencies for backlit displays and overhead projection, 35mm color slides, 60 image color microfiche, and 16mm/35mm color animation films. All with one camera system. It also allows recording of multiple image formats. Related and sequential images can be recorded in orderly arrays, on a single sheet of 8 x 10 instant print film. The resultant ease of comparison and analysis is unmatched. The system is also fully modular and field upgradable. . . you purchase only the capability that you need now.

Microprocessor based electronics provide many automation, self-calibration, self-diagnosis and remote control functions. Color graphics hard copy made easy by Matrix Instruments, the leading manufacturer of precision electro-optical imaging cameras for diagnostic medical applications.

For more information, film samples, or a demonstration, contact Matrix Instruments, 230 Pegasus Avenue, Northvale, New Jersey 07647.
Telephone (201) 767-1750
Or call toll-free: (800) 526-0274.



MATRIX INSTRUMENTS

CIRCLE 119 ON INQUIRY CARD

Hard copy shown reduced from original 8" x 10", slide, and microfiche films.
Multiple images recorded on a single sheet of film.
"Polaroid" is a registered trademark of the Polaroid Corporation.

Hardware/software integration unit handles software developed on host computer

Major needs of those using host computers to generate software for microcomputer systems are satisfied by the 8540 integration unit. Taking executable object code generated on the host, this member of Tektronix's 8500 family of microcomputer development labs provides facilities for integrating hardware/software, executing and debugging the code, and obtaining performance analysis from the prototype in real time.

System operation

From prototype software developed on the host, object code is downloaded to the unit's program memory that accommodates up to 128k bytes. This code can then be substituted for prototype memory. The emulator can support large address capabilities of 16-bit chips, since program memory can be mapped to reside at different logical addresses.

Downloaded program code is executed on the unit's emulator processor, identical to the processor that will be used in the target system. A prototype control probe links this processor to the prototype hardware so that the program is tested in its actual hardware environment. Since emulators run in real time with no wait states, time critical areas of program code can be tested and verified.

The debugging system allows software to be integrated with hardware on a step by step basis using three distinct emulation modes. Each step of the program execution is traced by the debugging system and displayed on the terminal screen or on a line printer. Trace display contains all pertinent processor information, including instruction mnemonics and labels from the symbol table. Breakpoints halt program execution at key locations; a built-in disassembler permits object code to be displayed in mnemonic form; and symbolic references are allowed in commands and trace displays.

Choice of emulation modes allows software testing to progress before prototype hardware is completed or even available. Mode 0 uses the unit as a prototype substitute; the system supplies the clock, and there is no connection between emulator processor and prototype hardware. I/O transactions are simulated through temporary code insertions that transfer I/O to the console terminal, or by breakpoints that halt the program so that certain parameters can be examined or modified.

Other modes tie the emulator to the prototype using the control probe so that the system can control the prototype directly. In mode 1, all prototype clock I/O and interrupt signals are used, but code is executed in prototype hardware and mapped over to prototype memory in sections. The entire program is transferred to prototype memory in mode 2. Because the control probe is still inserted in the prototype, debugging software can monitor program execution and debugging until testing is complete.

Options

A design tool that provides high resolution debugging capabilities for 8- and 16-bit design, the trigger trace analyzer (TTA) has four independent channels each with a 16-bit counter that reckons triggers or time, or provides delays. All four channels are composed of identical word recognizers that trigger on address, data, and control signal information, or various combinations. Trace memory 225 events deep by 62 bits wide acquires address, data, external probe, and control line information from the emulator. It accepts up to 24 address signals, 16 data signals, 14 processor dependent signals, and 8 external probe signals. For word recognizers and acquisition trace memory, the TTA has 8-MHz (125-ns) bus cycle resolution. Maximum clock rate for counting or timing on each channel is 5 MHz.

A P/ROM programmer allows code under development to be transferred into a P/ROM for later use as a program memory source in the prototype. Individual card modules adapt the programmer to any P/ROM family.

Specifications

The system interfaces to a host computer via an RS-232-C ASCII terminal port. Connection can be through data sets (modems) or hardwired. Communications variables are programmed from the keyboard, while data rates are selectable up to 9600 baud.

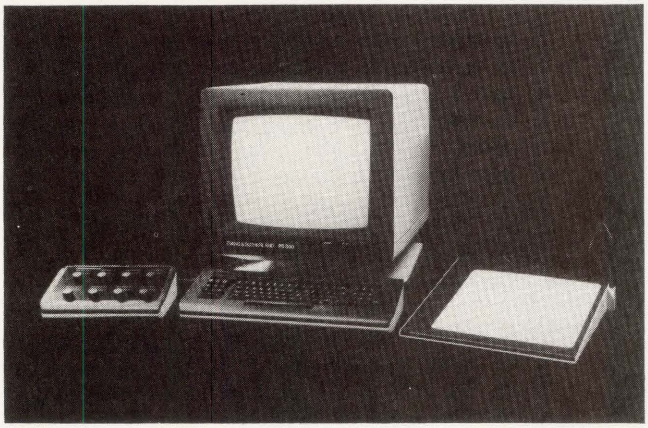
In addition to Z8001A and Z8002A chips, the unit supports the Z80A. Support for 8085, 8048, 6801, 8080A, 6800, and 6802 will be available within 6 to 9 mo; and 16-bit 8086 and 68000 chips will be supported later this year.

Price and delivery

With customer deliveries scheduled to begin in November, the 8540 will sell for $10,900. Options are priced as follows: trace analyzers, $4150; host interface package, $400; and P/ROM programmer, $1650. Emulator prices range from $4000 for 8-bit units to $6500 for 16-bit versions. Tektronix, Inc, PO Box 500, Beaverton, OR 97075. Tel: 800/547-6711.

For additional information circle 199 on Inquiry Card.

Distributed graphics system operates interactively using standard RS-232 connections



A self-contained dynamic interactive graphics system designed for CAD/CAM and other high performance applications, PS300 operates wherever conventional communications lines are available, reducing system operating cost by eliminating the host computer as part of the system. The unit is capable of high performance dynamic interactive operation at any distance from the host computer using standard RS-232 or RS-449 communications connections and operates with a variety of host computers for application programs. Incremental building and changing of complex graphic data structures are performed with all object references by name. Interactive manipulation of objects is handled by commands that allow devices and objects to be linked through a large library of functions. In addition to convenience and utility, the architecture provides a high performance calligraphic display system that can compute and display images of up to 95,000 vectors/frame. Operations include traditional rotation, translation, scaling, clipping, and depth cuing to produce dynamic isometric or perspective drawings.

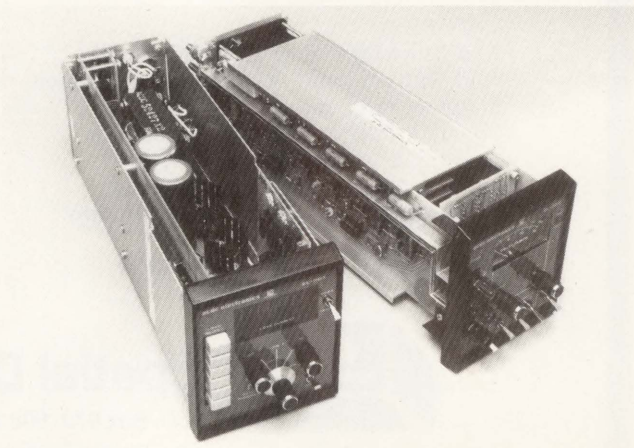
The minimum configuration includes 256k bytes of memory which expands to 4M bytes. It may be equipped with up to 4 monitors. Available interactive devices include an 11" (28-cm) tablet, 8 control dials, and a freestanding alphanumeric keyboard including 12 function keys. A keyboard option provides alphanumeric LEDs that can be programmed to provide an 8-char label for each function key. A similar LED option is available for the control dials. Built-in maintenance facilities allow the system to be serviced and comprehensive diagnostic programs to be executed without using the host computer. When power is applied, the system automatically executes confidence tests. **Evans & Sutherland,** 580 Arapeen Dr, Salt Lake City, UT 84108.

Circle 200 on Inquiry Card

Electronic instrument handles static or dynamic load testing of dc power sources

EL300 series, consisting of 2 basic modules and various accessories, handles static or dynamic load testing of dc power sources. As a basic load, the unit is a low cost instrument for loading power supplies under test or for burn-in. When used with the EL301 instrument module it becomes a precision, programmable test system for use in laboratories, quality control and receiving, or production test. Lightweight and portable, it also serves in onsite troubleshooting and field service. The load module with internal fan can dissipate 300 W continuously when operated from an ac line. Power sources from 4.5 to 60 Vdc can be tested for proper operation. As a portable test instrument, the module, with optional carrying case, operates with no line power and dissipates up to 250 W at 50% duty cycle (150 W continuously). Other features include front panel metering to 3% accuracy, selectable for voltage or current in either of 2 ranges, and a current signal output. All controls are located on the front panel for power on, load current adjustment, and mode selection. Facility for load connection up to 20 A, short circuit testing, or external monitoring of voltage is also on the panel. Higher load currents interface on the rear panel.

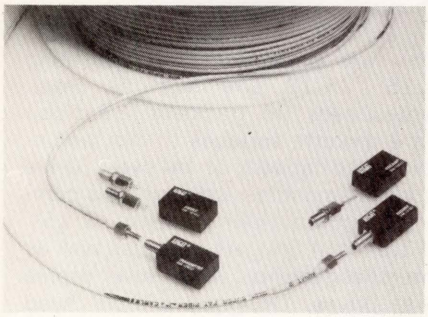
The EL301 instrument control module complements the dynamic load by expanding operation capabilities. It can monitor and program up to 6 loads, test dc levels as low as 1.8 Vdc (1.5 Vdc derated), and allows dynamic loading in two modes—a square wave at approx 120 Hz or 1 kHz. It also facilitates programming from various external voltage waveforms. Other features are digital current meter (0.5% accuracy), and provision for constant current operation. Accessories include portable benchtop case or 4-position RETMA rack. Load modules can be operated in parallel to achieve higher power ratings. **ACDC Electronics,** 401 Jones Rd, Oceanside, CA 92054.



Circle 201 on Inquiry Card

CIRCUIT COMPONENTS AND SUBASSEMBLIES

FIBER OPTIC DATA LINKS



CL10 offers a choice between integral transmitters and receivers or separate component parts. Systems will transmit data over 150 m at rates from dc to min of 10M bits/s with bit error rate of less than 10^{-9}. 689-CL10-1 provides separate driver/emitter and preamp/detector components with distance capability of 50 m. 689-CL10-2 is composed of similar components with emitter having distance capability of 150 m. 698-CL10-3 consists of transmitter and receiver pair also capable of 150 m. **Augat Inc,** 40 Perry Ave, Attleboro, MA 02703.
Circle 202 on Inquiry Card

DUAL-ROW 18-WIRE IMPACT MATRIX PRINTHEAD

Model 4000 Version A prints typewritten quality text at speeds greater than 100 chars/s and std EDP chars at up to 400 chars/s. 50% overlap of dots yields 144 dots/in (57/cm) vertical density. Version B, for use in matrix printers with speeds of 350 to 450 chars/s, has print wire frequency of 2000 Hz for theoretical top speed of 800 chars/s. Both versions are designed for continuous duty, bidirectional printing. **DH Associates,** 754 N Pastoria Ave, Sunnyvale, CA 94086.
Circle 203 on Inquiry Card

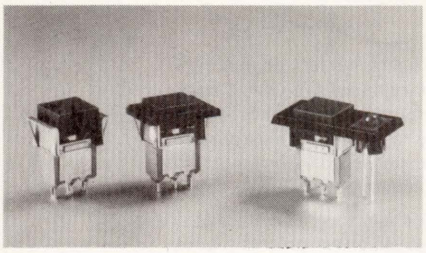
PRINTER CONTROLLERS

DPC 40-DS uses an 8-bit parallel data transfer bus that handles full ASCII 96-char set along with vertical format paper movement instructions. DPC 50-DS has 16-bit parallel input from the computer with 8-bit parallel output bus to the computer for handshake signals, and 256-bit RAM that permits the computer to set and clear horizontal tabs in 132 positions. Both units are bus and software compatible with DG NOVA and ECLIPSE minicomputers and accommodate BDS band printers with speeds of 300, 600, 900, and 1500 lines/min. **BDS Computer Corp,** 1120 Crane St, Menlo Park, CA 94025.
Circle 204 on Inquiry Card

16-BIT ADC WITH 0.003% LINEARITY ERROR

ADC1140 includes 16-bit ADC with max conversion time of 35 μs, successive approximation register, precision 10-V reference, clock, comparator, and input scaling resistors for pin-selectable input voltage ranges of ±5, ±10, 0 to 5, and 0 to 10 V. Power requirements are ±15 V at ±25 mA, max, and 5 V at 150 mA, max, for power consumption of 1.5 W max. Op temp is 0 to 70 °C, low gain temp coefficient is 12 ppm/°C, max. **Analog Devices, Inc,** Rte 1 Industrial Pk, Norwood, MA 02062.
Circle 205 on Inquiry Card

MINIATURE PUSHBUTTON SWITCHES



PS series switches have a snap-in superstructure that permits 1-step mounting from the front of the panel. Designated PS14, PS15, PS16, and PS17, all models fit into a 0.500 x 0.600" (1.27 x 1.52-cm) rectangular panel hole. Available in 1- or 2-pole, double-throw circuit configurations, devices have either solder lug or PC mount terminals in 1 A at 120 Vac or 0.4 A at 20 Vac or dc. Various caps, bezels, and colors are available. Std colors are red, white, and black. **Eaton Corp, Commercial Controls Div,** 4201 N 27th St, Milwaukee, WI 53216.
Circle 206 on Inquiry Card

MAGNETIC TAPE HEADS

Series A heads measure 0.2" x 0.48" x 0.5" (0.5 x 1.22 x 1.3 cm) and incorporate two 0.057" (0.145-cm) channels in fully drawn case for max shielding, balanced core/coil structure to ensure write symmetry, and center tapped windings. They are offered with terminal pins or flexible leads; variations in gap, inductance, and lamination thickness tailored to specs for applications up to 6400 flux changes/in (2520/cm). Heads work on cassette or cartridge using 0.15" (0.38-cm) tape. **Data Recording Heads Inc,** 690 Mendelssohn Ave, Minneapolis, MN 55427.
Circle 207 on Inquiry Card

LOW PROFILE KEYBOARD

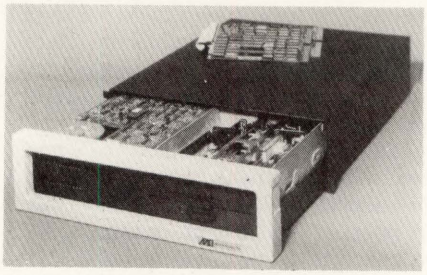
FC-2550, a low profile, ferrite core, solid state keyboard, allows designers to meet the 30-mm or less European ergonomic requirements for detached keyboard enclosures. The keyswitch is contactless and features few parts, true linear feel, and excellent resistance to environmental factors. It is 17.1 mm high without keytop and 21.9 mm with keytop. Life cycle test rating is in excess of 100M cycles. Keytops have full matte finish and are available in LED lighted versions. **Cortron, Div of Illinois Tool Works Inc,** 400 W Grand Ave, Elmhurst, IL 60126.
Circle 208 on Inquiry Card

WINCHESTER DISC CONTROLLER BOARDS

WD1000 provides complete disc controller for Winchester systems, featuring all necessary buffers, a 5M-bit/s transfer rate, and control for up to 4 drives and 8 read/write heads. WD1100 controller set, with 5 MSI chips (address mark detector, CRC generator/checker, MFM generator, serial/parallel converter, and parallel/serial converter), replaces 75 chips to provide an ST500/SA1000 interface. Set is offered in 20-pin plastic or ceramic DIP. **Western Digital Corp,** 3128 Red Hill Ave, Newport Beach, CA 92663.
Circle 209 on Inquiry Card

MEMORIES

RL01/02 EMULATING WINCHESTER/FLOPPY SUBSYSTEM



MD 3500 fully emulates the DEC RL01/02 removable cartridge subsystem with an 8" (20-cm) Shugart SA1000 or Quantum Q2000 series Winchester disc drive and provides 10M to 40M bytes of formatted data storage. A double-sided/double-density Qume DT/8 floppy drive provides RX02 compatibility with 0.5M bytes of formatted data storage. The system has the capability of copying only current working files to the floppy. Emulation is achieved using a proprietary recording technique that produces a higher data storage capacity but does not exceed the max specified disc flux density. Disc management is provided by the MLXVII controller configured on two dual-wide LSI-11 sized cards. **Micro Technology, Inc,** 2192 Martin, Suite 210, Irvine, CA 92715.

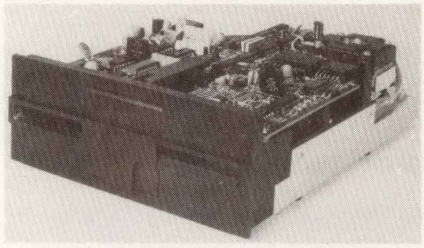
Circle 210 on Inquiry Card

2M-BYTE 5.25" FLOPPY DRIVE

Double-sided Megafloppy 1117 models offer 2.175M and 2.025M bytes of formatted storage at 100 and 96 tracks/in (39.4 and 37.8/cm), respectively; single-sided versions offer 1.2M and 1.1125M bytes of storage at 100 and 96 tracks/in (39.4 and 37.8/cm), respectively. For all models, recording density is 12 bits/in (4.724/cm), track to track positioning speed is 6 ms, and data transfer rate is 600k bits/s. Units are fully compatible with industry std interfaces, mounting dimensions, and bezels. **Micropolis Corp,** 21329 Nordhoff St, Chatsworth, CA 91311.

Circle 211 on Inquiry Card

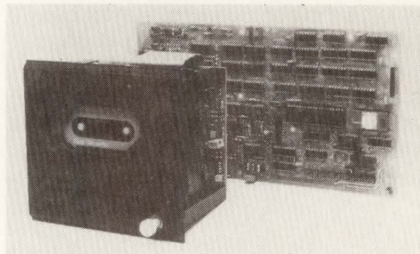
5.25" FLOPPY DRIVE



The low profile RFD960, measuring 2.25" (5.72 cm) high at bezel, writes/reads 96 tracks/in (37.8/cm) on 2 diskette surfaces to provide unformatted capacity of 1M bytes. Drive is ANSI compatible and maintains complete compatibility with 5.25" (13.34-cm) Shugart drives as well as interchangeability with low profile BASF drives. Designed without head solenoid, the unit features clutch and spindle design that positions media accurately without damage or distortion. **Remex, Div of Ex-Cell-O Corp,** 1733 Alton St, Irvine, CA 92713.

Circle 212 on Inquiry Card

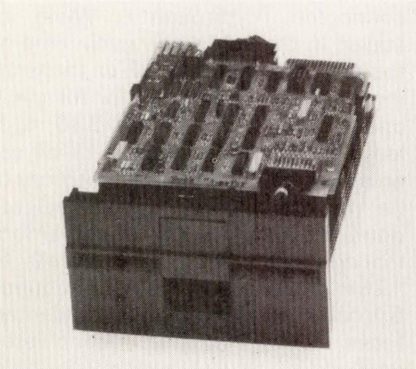
DIGITAL CASSETTE RECORDER



Model 6440 Raycorder II uses a microprocessor based control system to continuously monitor and regulate tape speed and tension, and to ensure uniform start/stop profiles. The reel drive transport is designed with all major structural components molded of thermoset plastic materials. A cassette inserted into the unit is constrained within a precision head guide assembly mounted in the door. When the door is closed, the cassette engages reel motor hubs and cassette positioning guides. Sensing is provided for tape leader, load point, early warning, cassette in place, side A/B, and write protect. Tape speed and tension are controlled by a system that incorporates optical sensors located on each motor shaft to provide velocity information. A microprocessor monitors velocities and controls voltage applied to provide uniform tape speed. **Raymond Engineering, Inc, Raycorder Products Div,** 217 Smith St, Middletown, CT 06457.

Circle 213 on Inquiry Card

96-TRACK/IN 5.25" FLOPPY DISC DRIVE



Single-sided SA410 and double-sided SA460 drives offer 500k- and 1M-byte (unformatted) storage capacity, respectively. Drives incorporate helical cam lead screw design for accurate head positioning and fast starting dc motor, and are downward compatible with 48-track/in (19/cm) drives through software. For both models, avg access time is 160 ms, avg latency is 100 ms, and transfer rate is 250k bits/s. **Shugart Associates**, 475 Oakmead Pkwy, Sunnyvale, CA 94086.

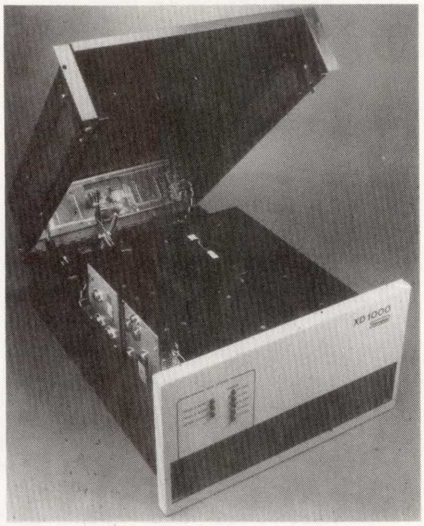
Circle 214 on Inquiry Card

5-CHIP BUBBLE MEMORY SUPPORT CIRCUIT SYSTEM

When combined with the NBM2256 256k-bit bubble memory and a few discrete components, 5-chip support circuit set forms a dense, compact bubble memory system. Density and size result from use of bubble domain, bipolar, and XMOS technologies. The 256k-bit NBC82851 LSI bubble memory controller provides data transfer, all signal timing necessary to drive 1, 2, 4, or 8 bubble memory modules, and control of remaining interface circuits. Digital TTL level pulses generated by a timing circuit are converted into current pulses required by the NBM2256 by the DS3615 function driver. The DS3616 coil driver provides high current drive capability for the triangular current waveforms used for the drive coils. Two drivers are required for each memory module. The DS3617 sense amplifier converts low level signals from magnetoresistive detectors of the bubble memory into TTL compatible output levels. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

MEMORIES

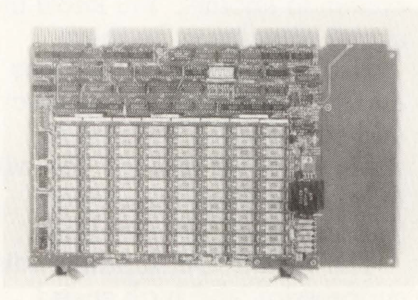
WINCHESTER DISC MODULE



XD1000 provides up to 48M bytes of online storage capacity for computer systems including DEC Unibus and Q-bus systems, DG I/O type bus systems, and Multibus type systems. The module consists of up to two 24M-byte, high reliability Winchester type disc drives and associated power supplies. It is self-contained in a rack mountable steel enclosure [25.25" deep x 16.75" wide x 10.5" high (64 x 42.5 x 26.7 cm)]. Power requirements are accommodated by power supplies in the module, which requires only 115- or 230-Vac input power. The only operator actuated control is the power on/off switch. The front panel contains 8 status indicators that provide operational information. An electronic head lock option protects the drives under adverse conditions. **Xylogics, Inc,** 42 Third Ave, Burlington, MA 01803.

Circle 215 on Inquiry Card

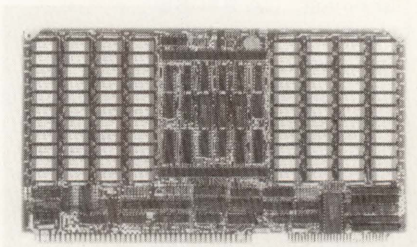
128k x 12 SEMICONDUCTOR ADD-IN FOR PDP-8/A



DR-118S, a single-board 128k x 12 add-in for DEC PDP-8/A, is offered on a quint board (5 card edge connectors) and is completely plug compatible with DEC's 16k x 12 MS8-CA and 32k x 12 MS8-CB memory modules. The board plugs into one card slot using connectors A through E. While installed in the computer, cycle time of the memory is 1.5 or 1.2 μs (depending on CPU module used) for full-cycle operations. Access time is 330 ns or less. The module accepts a 15-bit address, which allows 32k of memory to be accessed. Four bank selects generated by the KT8-A memory management option allow access to 128k words. The memory requires 5 Vdc for normal operation, and interfaces via the OMNIBUS. Depopulated versions are available with 96k, 64k, 32k, and 16k. **Dataram Corp,** Princeton Rd, Cranbury, NJ 08512.

Circle 216 on Inquiry Card

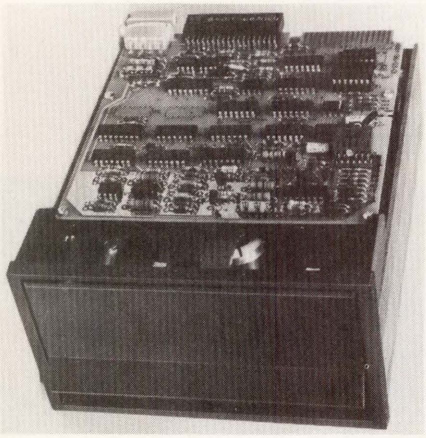
LARGE SCALE MULTIBUS MEMORY WITH ECC



Onboard error correction and detection circuitry enables MBC-XXX/16 MULTIBUS RAM boards to correct single-bit errors and detect double-bit errors. Units from 32k to 512k bytes in capacity include battery backup, onboard refresh circuitry, and LED status indicators. /16 series versions provide up to 512k bytes of straight memory; /16C versions provide error detection and correction. Both accommodate 8-bit byte and 16-bit word transfers. Error correction information is stored in an onboard register that is available to CPU via program control. Onboard refresh circuitry performs all necessary functions for maintaining the dynamic RAM contents; all refresh functions can be powered from the battery backup bus. **Advanced Digital Technology,** 696 E Trimble Rd, San Jose, CA 95131.

Circle 217 on Inquiry Card

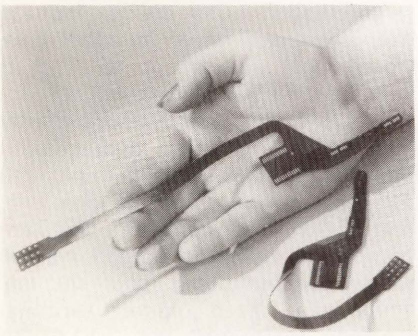
DOUBLE-SIDED DISC DRIVE



Double-head high speed random access FDD 296-5 stores and retrieves data on both sides of a 5.25" (13.34-cm) diskette. It uses a ceramic ferrite recording head design that is said to allow precise alignment, reduce head wear, and afford improved data interchangeability. Precise control of head loading dynamics reduces velocity and allows softer head landing. The unit provides 1M bytes of online unformatted data storage in double-density, and 500k bytes in single-density applications. Up to 4 drives can be combined on a single bus. Track to track access time is 20 ms for a random access time of 542 ms avg for 80 tracks. Head load time is 50 ms. Data transfer times are 125k bits/s (single) and 250k bits/s (double). **Siemens Corp, OEM Data Products Div,** 240 E Palais Rd, Anaheim, CA 92805.

Circle 218 on Inquiry Card

ROTATING MEMORY SYSTEM STANDARD FLEXIBLE CIRCUITS



Functioning as dynamic interconnect for read/write signals, circuits transmit data between wound-coil magnetic head and stationary PCB on large Winchester drives. Circuits are bonded to arms supporting flying magnetic heads; folded over to place dynamic loop in proper stress plane; and then attached by connector plugged into stationary PCB within system. **Rogers Corp, Flexible Circuits Div,** PO Box 700, Chandler, AZ 85224.

Circle 219 on Inquiry Card

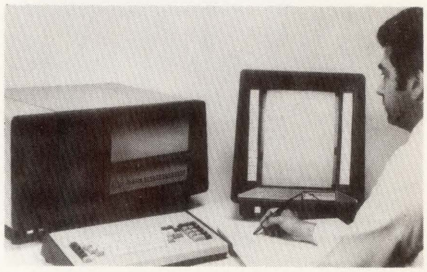
DATA TERMINALS AND DISPLAYS

SCALE OPTION FOR COLOR GRAPHICS TERMINAL

MACROFONT™ option for IDT-2000 automatically scales ASCII characters from 1 to 20 times their original size. Characters can be displayed in any combination of 8 colors with variable horizontal boldface, vertical boldface, depth of shadow, and character spacing. Free-formed dot addressable and vector formed pictures can be programmed and stored in RAM or P/ROM for rapid display with minimum communication from host computer. **Industrial Data Terminals Corp,** 173 Heatherdown Dr, Westerville, OH 43081.

Circle 220 on Inquiry Card

GRAPHICS WORKSTATIONS AND SOFTWARE



Built around a dual-processor architecture and Pascal operating system, the GS1100 includes 2 diskette drives, parity memory, dual processors, 2 RS-232 ports, keyboard and control electronics, black and white display and control electronics, data tablet and control, 64k-byte bit map, power supplies, and enclosures; the GS1120 adds a diskette drive and a 10M-byte Winchester fixed disc drive. The GS1200 has a 13" (33-cm) color display, instead of the black and white monitor, plus all 1100 features; the GS1220 adds a diskette drive and 10M-byte Winchester drive. IC designer software provides both general purpose and circuit design software, in addition to applications commands, data structure, and user interface including symbol recognition, communications, and data structure formatter. **Avera Corp,** 340 El Pueblo Dr, Scotts Valley, CA 95066.

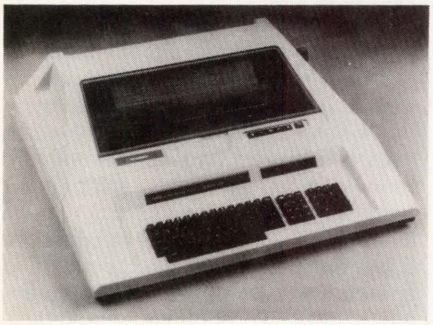
Circle 221 on Inquiry Card

VIDEO TERMINAL SUBSYSTEMS

VTS7710 small-cluster and VTS7740 large-cluster subsystems include microprocessor driven terminal controllers that support up to 4 or 8 keyboard display terminals, respectively, as well as 4 or 8 independently addressable printers, respectively. Both offer keyboard/display unit with 12" (30-cm), 24-line x 80-char CRT, and 76-key ANSI II keyboard. Units are compatible with the company's full range of computers, plus VIP7700, 7700R, and 7760 cluster terminal systems. **Honeywell, Inc,** 200 Smith St, Waltham, MA 02154.

Circle 222 on Inquiry Card

DOT MATRIX PRINTING TERMINALS



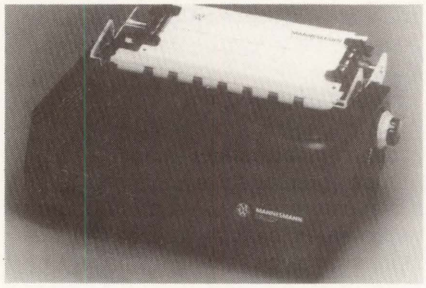
A keyboard and 40-char display provide interactive capabilities in the DP-9620 KSR. The 40-char single-line vacuum fluorescent display allows message editing and composition prior to transmission. An entire message can be displayed by a bidirectional scrolling feature. After a message is composed, it may be transmitted in echo mode; the printer receiving the message sends the data back to the originating unit, which then prints it. In another mode, data are transmitted and printed directly by the originating printer. In local mode, the message is composed locally and transmitted on command. Like its companion, model -9610 RO, the unit writes at 200 chars/s using a 10-char/in (3.9/cm) font. An 80-key alphabetic keyboard is included in the -9610 KSR; a 16-key numeric key pad is available on both -9610 and -9620 KSR. A 600-char FIFO buffer memory is std; additional 2k- and 4k-char buffers are optional. **Anadex Inc,** 9825 De Soto Ave, Chatsworth, CA 91311.
Circle 223 on Inquiry Card

GRAPHICS WORKSTATIONS

WHIZZARD 6240 uses a 19" (48-cm) black and white monitor with 512 x 512 resolution, 6245 a 19" (48-cm) black and white monitor with 1024 x 1024 resolution, and 6255 a 19" (48-cm) 1024 x 1024 resolution color monitor. All offer performance features of the 6250. 6240 and 6245 models offer flicker free display operating noninterlaced at a 60-Hz refresh rate. Packaged with keyboard and joystick control in a desk style cabinet, terminals include graphics processor, display list memory, and RS-232 serial asynchronous interface and room for optional modules. The 6255 is packaged with a keyboard and joystick control in a desk style cabinet, and may have data tablet and either additional display list memory or hardcopy output device. All units incorporate the high speed digital vector generators used in models 6250 and 7250, updating and manipulating complex pictures at rates from 30 to 60 times/s. WAND 6200 software provides intelligence in remote terminals to reduce communications traffic with the host. **Megatek Corp,** 3931 Sorrento Valley Blvd, San Diego, CA 92121.
Circle 224 on Inquiry Card

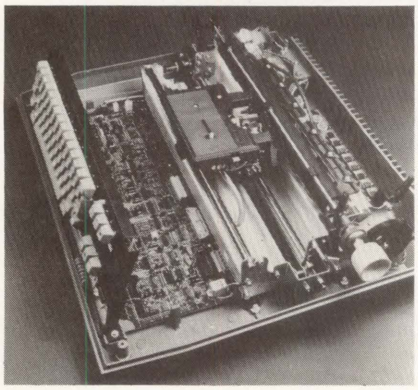
PRINTERS/PLOTTERS

80-COL SERIAL PRINTER



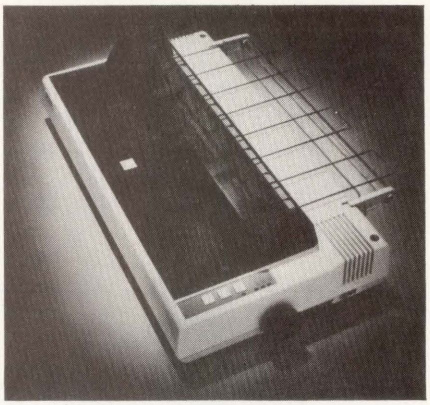
MT-100 series printers feature programmable print fonts and formats, speeds from 100 to 160 chars/s with optimized bidirectional printing, and character matrices of 7 x 7, 7 x 9, 9 x 9, or 40 x 18. Features include special plotting modes, flexible forms handling capability, quiet (55-dBa) operation, easy to change ribbon cartridge, operator replaceable printhead, multipart forms printing, and 2k-byte buffer with asynchronous serial interface. Interchangeable plug-in interface modules connect to a variety of computers. **Mannesmann Tally,** 8301 S 180th, Kent, WA 98031.
Circle 225 on Inquiry Card

KSR PRINTER TERMINAL



SPRINT 9/35™ operates at 35 chars/s and features MicroDrive print mechanism with KEVLAR direct drive belt, universal linear power supply, improved ribbon handling, 65-dBa max acoustic noise level, and switch-selectable automatic proportional spacing. All electronics are on a single board located under the removable keyboard. MTBF is 3000 h. Receive only (RO) model is also available. **Qume Corp,** 2350 Qume Dr, San Jose, CA 95131.
Circle 226 on Inquiry Card

136-COL DOT MATRIX PRINTER



MX-100 uses dot matrices ranging from 9 x 9 to 18 x 18 to generate correspondence quality printing in 12 different character weights and sizes. Unit prints bidirectionally at 80 chars/s, with a logical seeking function to minimize printhead travel time and maximize throughput. Features include the company's Micro-Nine disposable printhead, GRAFTRAX high resolution bit image graphics capability, friction paper feed platen, and adjustable tractors on removable tractor mechanism. **Epson America, Inc,** 23844 Hawthorne Blvd, Torrance, CA 90505.
Circle 227 on Inquiry Card

180-CHAR/s MATRIX IMPACT PRINTER

Model 1000 produces data processing quality characters at 10, 12, or 16.5 chars/in (4, 4.7, or 6.5/cm) and correspondence quality characters at 10 chars/in (4/cm), at 6.0 or 8.0 lines/in (2.4 or 3.1/cm). Max print speed is 180 chars/s, with up to 136-col output and no duty cycle limitations. Printer measures 7.25 x 25.5 x 15.0" (18.42 x 6.48 x 38.1 cm) and weighs 32 lb (14.4 kg). Input power is 110, 120, 220, or 240 Vac, optionally; 47 to 63 Hz; 75 W max. Unit operates in graphics mode as well. **Infoscribe, Inc,** 2720 S Croddy Way, Santa Ana, CA 92704.
Circle 228 on Inquiry Card

COMPUTERS AND COMPUTER SYSTEMS

REALTIME DIGITAL VIDEO PROCESSOR

Q/VP-122 processes video images in real time with full spatial resolution of 768 x 512 and amplitude resolution of 256 levels; entire frame of video data is digitized and stored onboard for video or CPU processing. Unit features pipeline processing, image averaging, image noise reduction, edge enhancement, and correlation and convolution of realtime video imagery data. Throughput is 14 MIPS. Processor interfaces to DEC LSI Q-bus and Intel MULTIBUS (8086/Z800). **Datacube, Inc,** 670 Main St, Reading, MA 01867. Circle 229 on Inquiry Card

DESKTOP COMPUTER SYSTEM

Entry level member of the company's series 21 line, the basic 21/10 system is comprised of controller/console CRT with 96k memory and communications controller integrating as std one diskette drive, in addition to a display screen with moveable keyboard. A second diskette and a choice of either 45-char/s letter quality or 120-char/s matrix printer are available. The system supports asynchronous and Bisync communications including 3270 dialogue at speeds to 4800 bits/s. The system can process two separate jobs concurrently. **Mohawk Data Sciences,** 7 Century Dr, Parsippany, NJ 07054. Circle 230 on Inquiry Card

MINICOMPUTERS

Models 34 and 44 MAGNUM minicomputers are offered as alternatives to DEC's PDP-11/34 and /44, and are supported by RSTS/E, RSX-11M, and RT11 operating systems. Std configuration includes CPU with floating point and memory management, serial console interface, programmable line time clock, bootstrap loader, 8k-byte cache memory, microcoded ODT, maintenance console, and 256k (34 MAGNUM) or 512k (44 MAGNUM) bytes of memory. **Able Computer,** 1751 Langley Ave, Irvine, CA 92714. Circle 231 on Inquiry Card

OEM VERSION DATA PROCESSOR

An OEM version of the 1550 dispersed data processor, the 2150 is a low cost desktop processor that can support multiple workstations. Built around a high speed Z80A microprocessor chip, the unit has approx 67% more processing speed than its predecessor, and can be used with commercially available operating systems designed for Z80A processors, as well as a range of applications software packages. It supports the company's DATABUS[R] business programming language, FORTRAN, BASICPLUS, word processing, and electronic message services. EM3270 software allows it to perform interactive IBM mainframe communications. Software for IBM batch communications, 2780/3780 is also available. The processor is equipped with 32k, 64k, or 96k memory. Dual-diskette modules are available in either single-sided/single-density or double-sided/double-density versions, offering 0.5M- or 2M-bytes systems. With 64k of memory the unit can support a 9310/9320 10M-byte cartridge disc drive. **Datapoint Corp,** 9725 Datapoint Dr, San Antonio, TX 78284.

Circle 232 on Inquiry Card

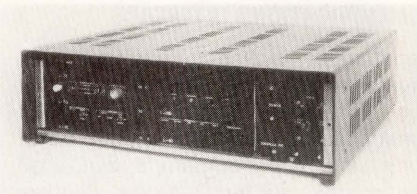
ARRAY PROCESSOR

Designed for Data General NOVA/ECLIPSE minicomputers, MSP-2X block floating point array processor is contained on one 15 x 15" (38 x 38-cm) board and plugs directly into an I/O slot of the host. The processor uses a 24-bit mantissa and 8-bit exponent in its format and includes a 2k x 24-bit high speed data memory and onboard memory table of trigonometric values. It includes a library of FORTRAN-callable routines that includes real and complex Fourier analysis, data transfer, filtering, real and complex vector, and other signal analysis functions. **Computer Design & Applications Inc,** 377 Elliot St, Newton, MA 02164.

Circle 233 on Inquiry Card

DATA COMMUNICATIONS

INVERSE MUX



Lineplexer II eliminates need for wideband facilities, providing full-duplex data communications at rates up to 19.2k bits/s over 2 independent analog or digital channels, each operating at 9600 bits/s. Features include extensive diagnostics, automatic/manual rate adjustment for line degradation, automatic compensation for path delay difference, day/night reconfiguration, and automatic or manual training sequence. **Timeplex, Inc,** One Communications Plaza, Rochelle Park, NJ 07662.

Circle 234 on Inquiry Card

DATA COMMUNICATIONS

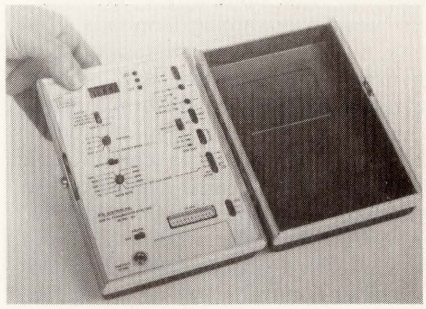
SYNC/ASYNC SERIAL COMMUNICATIONS INTERFACE

Capable of either synchronous or asynchronous printer-computer operations, the microprocessor controlled serial communications interface functions with the company's 200-line/min matrix printer, B-series printers with speeds from 300 to 900 lines/min, and with QT band printers. Programmed for synchronous operation, the SI-9076 enables printers to function with IBM 2780/3780, Burroughs poll and select, Univac 1004, Honeywell VIP 7700, and other industry standard protocols. The interface allows users to implement a smart printer on a serial communications network, and can replace communications processors. It operates full- or half-duplex or as a null modem hookup; synchronous serial data rate may be from dc to 64k baud; asynchronous rate is from 50 to 19.2k baud. Std or special code conversions (ASCII, EBCDIC, Baudot, IBM selectric, and others) can be performed. Programming area allows complete lookup table implementation. **Southern Systems, Inc,** 2841 Cypress Creek Rd, Ft Lauderdale, FL 33309.

Circle 235 on Inquiry Card

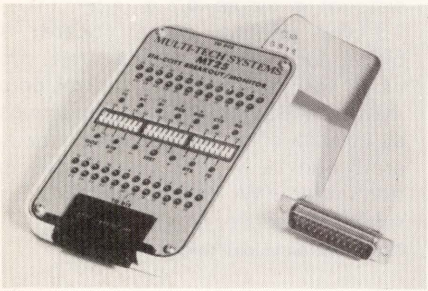
HANDHELD DATA TRANSMISSION ANALYZER

Weighing but 25 oz (709 g), digital transmission analyzer DTA-181 has 3 operational modes that (1) measure bit errors simultaneously, total test seconds and errored seconds; (2) measure elapsed time between transitions on any signal and/or control lead; and (3) trap and count 1 to 0 or 0 to 1 transitions. It handles any of 5 data patterns, full-duplex, with choice of 10 asynchronous speeds from 50 to 9600 bits/s and 5 synchronous speeds from 1200 to 19.2k bits/s. Five-digit accuracy is provided by a 4-digit LCD plus a unique overflow display technique. **AQ Systems, Inc,** 1736 Front St, Yorktown Heights, NY 10598.



Circle 236 on Inquiry Card

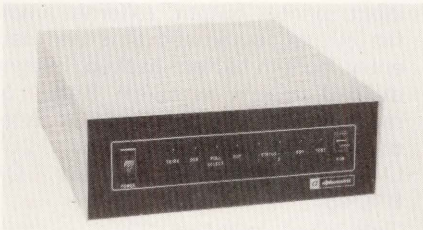
PORTABLE COMMUNICATIONS DIAGNOSTIC DEVICE



Permitting users to individually access leads of EIA RS-232 interface and to patch and monitor these leads, MT25 EIA/CCITT breakout/monitor uses 11 LEDs to indicate status of primary RS-232 signals; 2 additional LEDs are provided for other chosen signals. Twenty-four miniature rocker switches allow each signal to be interrupted; test access points at both DTE and DCE side of the interface allow for patching and monitoring each signal. Jumper wires facilititate patching and cable reconfiguration. **Multi-Tech Systems, Inc,** 82 Second Ave SE, New Brighton, MN 55112.

Circle 237 on Inquiry Card

PROTOCOL CONVERTER



Bisync printer controller BAE-806 enables communications between any ASCII RS-232-C line printer and any DP system supporting IBM 2780/3780 devices. The converter automatically performs all buffering, code conversion, and realtime requirements. Both printer and converter may direct connect to a CPU Bisync port or be located remotely via a pair of synchronous modems. Std features include data compression, forms control and programmable tab stops, 8 LED status indicators, internal/external synchronous clock, auto-answer, and loopback self-test/diagnostics. **Alphamatrix Inc,** 1021 Millcreek Dr, Feasterville, PA 19047.

Circle 238 on Inquiry Card

MULTILINE CALLING UNIT

VA811 connects directly to switched network, allowing a single RS-366 computer port to address up to 60 single-board or 28 double-board modems. It replaces Bell 801 single-line automatic calling unit, and handles a mix of modems including the company's VA3400, and Bell 103, 201, 202, and 212. Features include automatic selection of pulse or tone dialing, positive dial tone, answer tone and busy signal detection, and 15- to 56-s abandon call and re-try times. **Racal-Vadic,** 222 Caspian Dr, Sunnyvale, CA 94086.

Circle 239 on Inquiry Card

VOICE RECOGNITION/ SYNTHESIS

SPEAKER-INDEPENDENT VOICE RECOGNITION SYSTEM

Self-contained analyzer and voice controller extracts cues from human speech and accurately identifies voice, fundamental pitch, and duration. Common noises and clicks are suppressed even when more intense than message signal. Unit recognizes 16 distinct commands and has unlimited capacity when used with a microcomputer. Conventional radio and telephone channels suffice for this system, allowing a variety of remote control applications. **Covox Co,** PO Box 2342, Santa Maria, CA 93455.

Circle 240 on Inquiry Card

INTELLIGENT COMMUNICATIONS CONTROLLER

SLC-II is a microprocessor with a synthesized voice and vocabulary of over 300 words. Connecting to an RS-232 line between computer and terminal, it monitors message flow, automatically responding to any of 15 preprogrammed events on each of 4 channels. It can initiate voice or data messages at intervals or on recognition of an event, or respond to phone messages originating at a remote terminal or a telephone keypad. Features include ASCII input/output, touch-tone input, printer output, external amplifier output, automatic time and data entry, built-in battery backup, integral auto-dial/auto-answer Bell 103 modem, and 16k, 32k, or 80k bytes of RAM. **Digital Pathways, Inc,** 1260 L'Avenida, Mountain View, CA 94043.

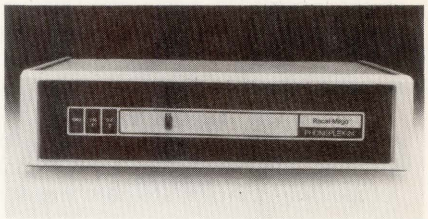
Circle 241 on Inquiry Card

TEXT TO SPEECH SYSTEM

SPEECH MACHINE converts unconstrained English text into audible natural speech. Natural English word stress patterns and overall phrase pitch and stress contours add to the system's intelligibility. Vocalization and pauses are paced automatically to reflect format, content, and punctuation of text. Canned utterances and symbolic phonetic strings may be mixed with unconstrained text on input, and will be joined in output. Onboard utility facilitates incorporation of applications and operator specific text and sound rules to accommodate exceptions. The unit handles a variety of special forms including acronyms, money amounts, special punctuation, numbers, and other conventional codes. Physically the machine consists of a single 4" x 7.5" (10 x 19-cm) printed circuit board. A bidirectional 8-bit parallel port provides for passing text, control commands, and symbolic phonetic strings, all in ASCII code. Power requirements are 5 and 12 V, with peak consumption under 3 W. **Yahara Corp,** PO Box 479, Centerville, MA 02632.

Circle 242 on Inquiry Card

VOICE DIGITIZER



Phoneplex-24 transmits voice communications in digital form at 2400 bits/s; used in conjunction with multiport modems, the device allows up to 4 simultaneous voice conversations or any combination of voice and data communications to share a common facility link. Unit addresses point to point and PBX tandem switching applications, and allows digital transmission facilities to be used for voice transmission. It also works with Datacryptor II and CMS 1000 and 2000 communications management series. **Racal-Milgo, Inc,** 8600 NW 41st St, Miami, FL 33166.

Circle 243 on Inquiry Card

LITERATURE

Data Acquisition Components

Monolithic and hybrid data conversion products and computer interface systems are covered in 566-p handbook that includes data sheets and selection tables. **Datel-Intersil,** Mansfield, Mass.
Circle 281 on Inquiry Card

Data Communications Equipment

35-p catalog contains descriptions, system configurations, photos, and circuit diagrams for data traps, test sets, modems, and multiplexers. **International Data Sciences, Inc,** Lincoln, RI.
Circle 282 on Inquiry Card

Capabilities Guide

Four-color, 4-p folder describes 6-vol reference guide to company's products and services. Send written request for document EC-19851-18/81 to Consultant Programs, MS PK 3-1/K 21, **Digital Equipment Corp,** 129 Parker St, Maynard, MA 01754.

Operating System Reference

Reference guide for single- and multiuser OASIS BASIC operating system for Z80 microcomputers. Request on company letterhead from **Phase One Systems, Inc,** 7700 Edgewater Dr, Suite 830, Oakland, CA 94621.
Circle 283 on Inquiry Card

Synchro/Resolver to Digital Converter

Std features, applications, and specs are summarized in booklet on 3-state, microprocessor compatible 16-bit hybrid device; performance graphs and circuit configurations are also included. **Natel Engineering Co, Inc,** Canoga Park, Calif.
Circle 284 on Inquiry Card

RFI/EMI Filters

Illustrated 16-p catalog uses photos, flowcharts, and spec charts to describe range of devices that meet new FCC requirements. **Raytheon Co,** Burlington, Mass.
Circle 285 on Inquiry Card

Interconnection Components

Features, specs, photos, drawings, and cross-references are found in 288-p catalog that presents full line of high current components, interconnection systems, connectors and wafers, tooling, single- and double-sided edge connectors, switches, and sockets. **Molex Inc,** Lisle, Ill.
Circle 286 on Inquiry Card

Disc Capacitors

Eight ceramic disc capacitor types are illustrated in 18-p, 2-color catalog featuring specs, graphs, and charts. **TRW Universal Capacitors,** Ogallala, Neb. Circle 287 on Inquiry Card

Industrial Process Control Systems

Over 90 DEC LSI-11 compatible devices, as well as Intel, Data General, Unibus, and Omnibus related devices, are detailed in complete ordering guide/price list. **ADAC Corp,** Woburn, Mass. Circle 288 on Inquiry Card

Design Guide

Multicolor, 4-p configurator chart aids in selection of specific, DEC compatible LAB-DATAX microcomputer peripheral system to meet I/O needs. **Data Translation, Inc,** Marlboro, Mass.
Circle 289 on Inquiry Card

Diode Laser

Data sheet on AlGaAs semiconductor device describes model OLX3400Z TAB-PAC providing operating specs, performance curves, and dimensional drawings. **Optical Information Systems,** Elmsford, NY.
Circle 290 on Inquiry Card

FCC Regulations

Booklet uses question and answer format to examine FCC emi emission rules as applied to digital equipment. **Sierracin/Power Systems,** Chatsworth, Calif. Circle 291 on Inquiry Card

Computer Graphics

Matching color graphics to MIS is explored in 12-p pamphlet directed to managers involved in statistical analysis. **Ramtek Corp,** Santa Clara, Calif. Circle 292 on Inquiry Card

Indicator Lights

Full-size photos, dimensional drawings, mounting information, and technical specs and ratings describe off-the-shelf devices. **Industrial Devices, Inc,** Edgewater, NJ.
Circle 293 on Inquiry Card

Image Array Processor

Full-color 6-p brochure uses photos and flowchart to illustrate capabilities of IP8500. **DeAnza Systems Inc,** San Jose, Calif. Circle 294 on Inquiry Card

CMOS Microboards

Color photos and spec charts in booklet present detailed information on 5 computers, 9 memories, 7 digital I/O expansion modules, 2 video audio-keyboard interface modules, and 8 ADCs and DACs. **RCA/Solid State Div,** Somerville, NJ.
Circle 295 on Inquiry Card

CMOS 3.9-V Battery Backup

Catalog contains discharge curves at various drain rates and dimensions of standard cell sizes, as well as information on stainless steel cases, terminations, hermetic seals, and temperature ranges for models BCX72, CSC93, and CSC150. **Electrochem Industries, Inc,** Clarence, NY.
Circle 296 on Inquiry Card

Power Supplies

Fully illustrated, 28-p catalog features specs, diagrams, and graphs covering full line of switching and uninterruptible power supplies that operate on any voltage worldwide. **Converter Concepts, Inc,** Pardeeville, Wis.
Circle 297 on Inquiry Card

Precision Measurement and Control Devices

Feature selection charts and specs are used in short form guide to provide information on complete line of products from IC op amps to computer based measurement and control systems. **Analog Devices,** Norwood, Mass. Circle 298 on Inquiry Card

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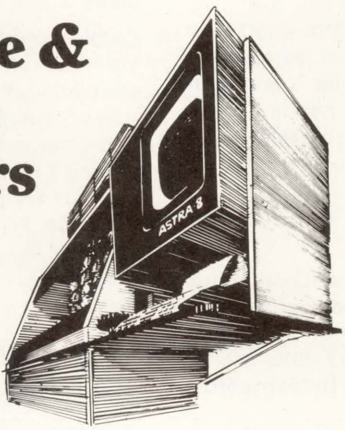

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FOR FURTHER CAREER OPPORTUNITIES SEE PAGE 26

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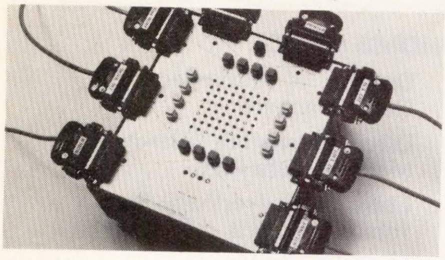

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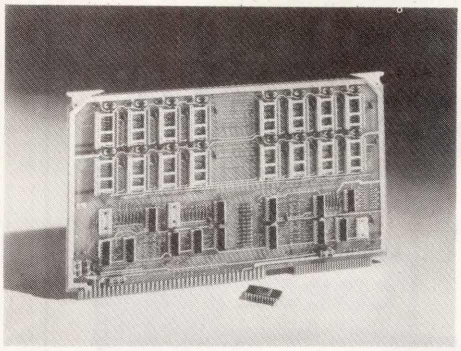
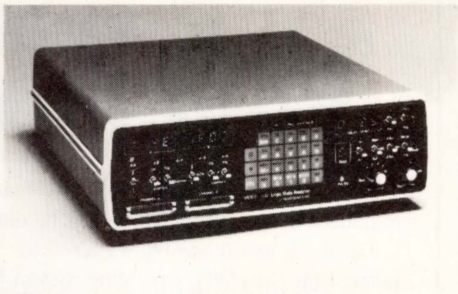


SBC 80 COMPATIBLE 32K PROM BOARD

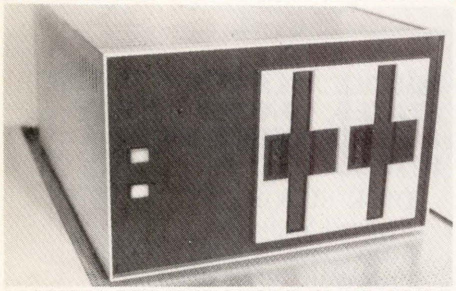
The PROM-32 accepts sixteen 2716 E-PROMS. The base addresses of the memory fall on 16K boundaries and are settable to 0000, 4000, 8000 and C000 Hex. Any 2K memory block may be deselected. 3 Year Warranty. $295 (Qty 1-9) Stock. **ELECTRONIC SOLUTIONS**, 5780 Chesapeake Ct, San Diego, CA 92123 Tel: (800)854-7086. In California call 292-0242 **CIRCLE 526**



LOGIC ANALYZER-32 CHANNELS ON A BUDGET

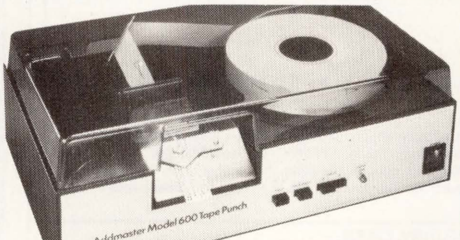
Only $3600, the PI-532C 32-channel logic analyzer includes all probes and a self-study course. Standard features are a 32-bit-wide by 250-word-deep memory, a separate reference memory, 21 triggering modes, demultiplexing and choice of displays: standalone or using a scope or video terminal. **PARATRONICS INC.**, 2140 Bering Drive, San Jose, CA 95131, 800-538-9713 (Toll-Free Outside California), 408/263-2252.

CIRCLE 527



MOSTEK STD BUS MICRO RUNS CP/M

The XM800 includes dual 8" drives, 16 slot card cage, and Mostek STD BUS cards in a single all metal attractive enclosure, 11" x 17" x 22". Complete system with 64k RAM and CP/M 2.2 from $4000; less user supplied cards, drives and software $995 Multibus and Eurocard versions also available. Available Mostek MD cards 30% off. STD proto systems also available. For full STD product catalog, contact **QC MicroSystems,** 9861 Chartwell Dr., Dallas, TX 75243. Phone (214) 343-1282. **CIRCLE 528**



Computer compatible Paper Tape Punch

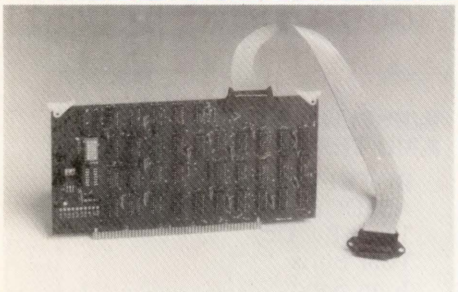
From Addmaster Corporation — a self-contained paper tape punch which makes 5, 6, 7 or 8-level tapes at speeds up to 50 cps. Parallel data keyboard inputs, manual back space, tape low lamp, TTL level compatible, 5-8 level (ANSI), optional RS232C I/O serial port are features. Maximum 8" reel, standard hub. (1000 feet). Optional attachment for standard fanfold tape.

Contact Addmaster Corporation, 416 Junipero Serra Drive, San Gabriel, CA 91776. Telephone: (213) 681-3098 **CIRCLE 529**

HEWLETT PACKARD 9845B/C & 9835A BINARY UTILITY PROGRAMS

Binary programs to enhance program editing capabilities and provide new keyboard commands are now available. ● **SEARCH & REPLACE** Provides a program-global facility to change names of labels, functions, variables and subprograms on BASIC programs in memory. ● **SYMBOL FINDER** Searches BASIC program for identifiers and reports defining line number and all occurrences. ● **MEMORY MAPPER** Prints memory map to help programmers write BASIC programs which execute faster and use less memory. ● **CROSS REFERENCE** An invaluable aid in preparing documentation. Produces a cross reference table to show all identifiers and line numbers where they occur. ● **DUMP ALPHA** Copies the CRT display to the internal printer or an external hardcopy device. ● **COMMENT STRIPPER** Removes comments from BASIC programs to reduce memory requirements and improve execution speed. ● **OEMSEC** Enciphers BASIC programs to prevent listing, tracing or interrogation of program variables. Insures that algorithms and trade secrets embodied in programs remain secure. ● **NODUP** Prevents duplication of the program media. Works with tape, floppy, or hard disc based systems.

STRUCTURED SOFTWARE SYSTEMS, INC., Box 1072, Irick Road, Mt. Holly, NJ 08060. (609)267-1616 **CIRCLE 530**



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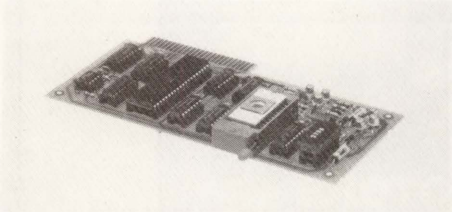
THE P&T-488 INTERFACE BOARD lets your S-100 computer be a talker, listener, or controller on the IEEE-488 instrumentation bus. Software packages allowing high level language access to the 488 bus are available for CP/M, CDOS, North Star DOS/BASIC, as well as for direct assembly language programming. Price of the P&T-488, assembled and tested with one of the software packages, is $450.

PICKLES & TROUT, Box 1206, Goleta, CA 93116 (805) 967-9563. **CIRCLE 531**



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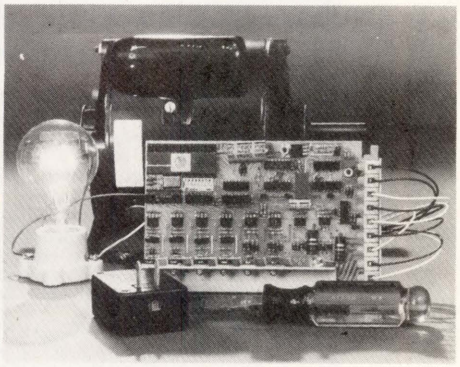
Apparat's Prom Blasting system (A.P.B.) will program model 2704, 2708, 2716, 2732, 2508, 2516 and 2532 EPROMs. The package comes complete with interface card, a complete set of personality modules, software on disk and a detailed instruction manual. The cost of the A.P.B. system is $149.00. TRS-80 versions require the Apparat Bus-Extender at $79.00 to $169.00, or a user supplied power supply and cable.

For details on the A.P.B. system, contact **APPARAT, INC**, located at 4401 S. Tamarac Parkway, Denver, Colo, 80237 or call Apparat's technical/service department at 303-741-1778. **CIRCLE 532**



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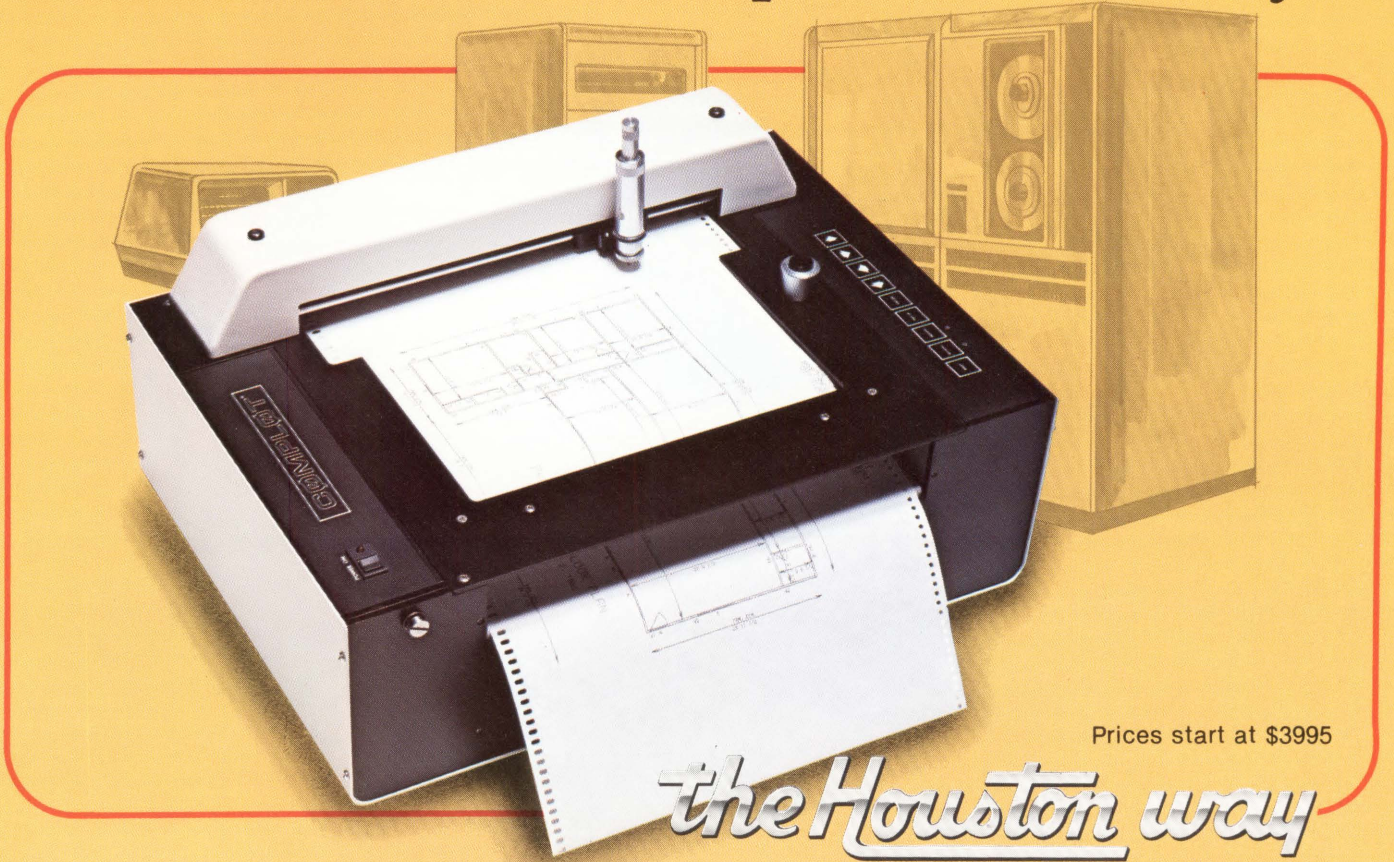

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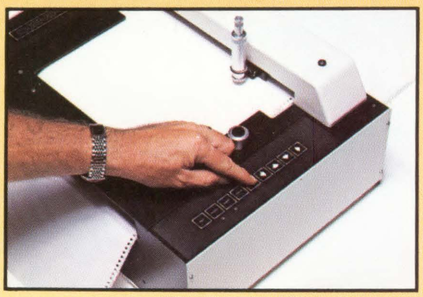

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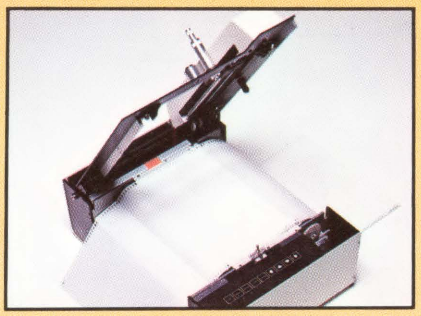

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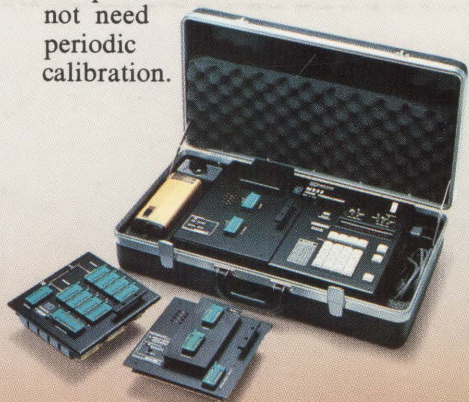

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