TOSHIBA

DRAM Components and Modules

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DATA BOOK

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

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DRAM Components and Modules
1994

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

Introduction

We are proud to introduce Toshiba's 1994 DRAM Components and Modules data book. The layout and contents of this data book were designed to address and resolve various concerns expressed by the design engineering and purchasing communities.

The first section consists of our DRAM component data sheets and corresponding package mechanical dimensions. It was our intention only to provide data sheets which correspond to part numbers of DRAM products which are in volume production and are recommended for new designs. We hope that this approach will help eliminate the experience of designing-in a particular device, only to find out later that it is difficult or impossible to source.

The next section consists of DRAM module data sheets and their corresponding AC conditions. Again, only module configurations and part numbers in volume production are listed in this section.

We have included a section labeled "Next Generation Products". The devices in this section will soon be in production and are suitable for new designs in the 1994 time-frame.

Finally, we have included reference documents and application notes to make your use of our products easier.

For additional information, please contact your local Toshiba sales office listed on the back cover.

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DRAM COMPONENTS

* See NOTE 1 on last contents page

DRAM PACKAGE MECHANICAL DIMENSIONS

DRAM MODULES

+ See NOTE 2 on last contents page.

DRAM MODULE AC CONDITIONS

NEXT GENERATION PRODUCTS

APPLICATION NOTES

NOTE 1:

Sym-512 = Symmetrical Address(9 Row/9 Column)
512 Refresh Cycles/8ms

Sym-1K = Symmetrical Address (10 Row/10 Column)
1024 Refresh Cycles/16ms

Sym-2K = Symmetrical Address (11 Row/11 Column)
2048 Refresh Cycles/32ms

Asym-1K = Asymmetrical Address (10 Row/8 Column)
1024 Refresh Cycles/16ms

Asym-2K = Asymmetrical Address (11 Row/10 Column)
2048 Refresh Cycles/32ms

Asym-4K = Asymmetrical Address (12 Row/10 Column for 4M or 12 Row/8 Column for 1Mx16)
4096 Refresh Cycles/64ms

Refer to Application Note for further details

NOTE 2:

x36 modules designated with "ECC" are optimized for ECC applications and x36 modules without the "ECC" designation are optimized for parity applications.
Refer to Application Note for further details.

4,194,304 WORD X 1 BIT DYNAMIC RAM

DESCRIPTION

THE TC514100A is the new generation dynamic RAM organized 4,194,304 word by 1 bit. The TC514410ASJ/AZ/AFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514100A to be packaged in a standard 26/20 pin plastic SOJ (300mil), 20 pin plastic ZIP, 26/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 1 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  660mW MAX. Operating
  (TC514100ASJ/AZ/AFT-60)
  550mW MAX. Operating
  (TC514100ASJ/AZ/AFT-70)
  468mW MAX. Operating
  (TC514100ASJ/AZ/AFT-80)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC514400ASJ : SOJ26-P-300A
  TC514400AZ : ZIP20-P-400A
  TC514400AFT : TSOP26-P-300

KEY PARAMETERS

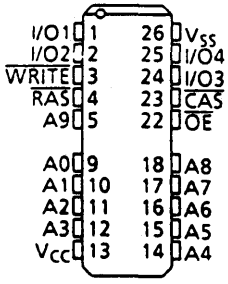
ITEM		TC514400ASJ/AZ/AFT		
		-60	-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC}	Cycle Time	110ns	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAME

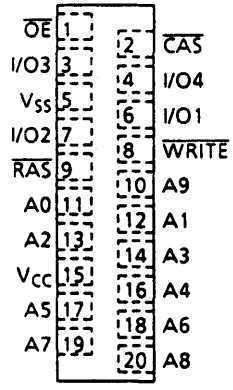
A0~A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

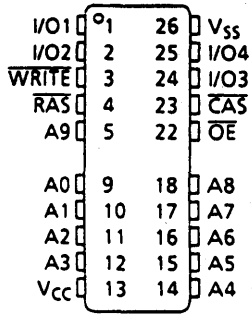
Plastic SOJ



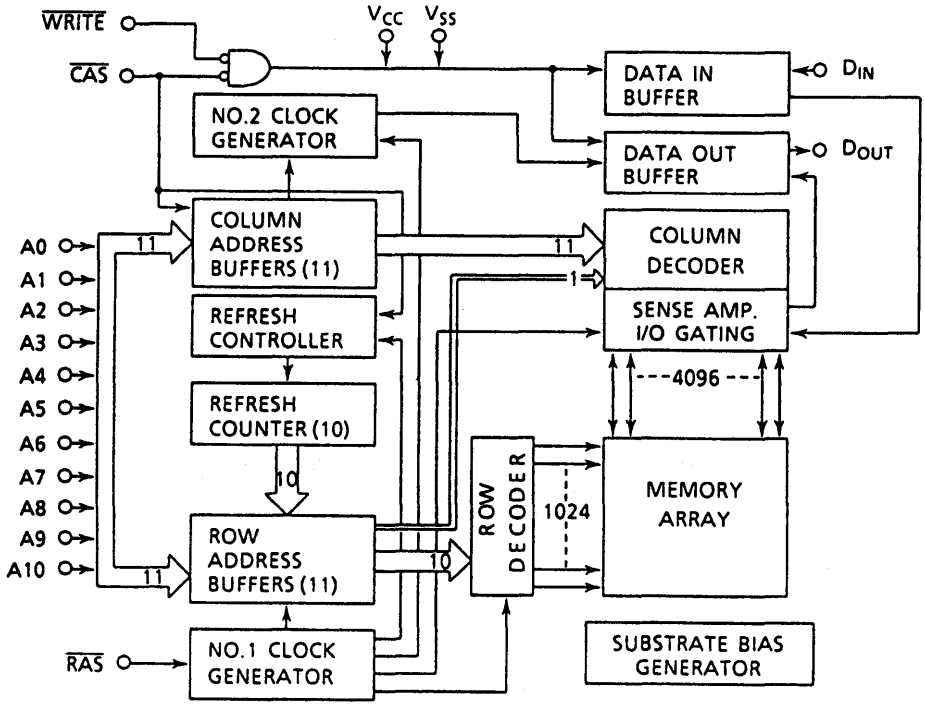
Plastic ZIP



Plastic TSOP (Normal Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

*This parameter is periodically sampled and is not 100% tested,

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input LowVoltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN)	TC514100ASJ/AZ/AFT-60	-	120	mA	3,4 5
		TC514100ASJ/AZ/AFT-70	-	100		
		TC514100ASJ/AZ/AFT-80	-	85		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514100ASJ/AZ/AFT-60	-	120	mA	3, 5
		TC514100ASJ/AZ/AFT-70	-	100		
		TC514100ASJ/AZ/AFT-80	-	85		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC514100ASJ/AZ/AFT-60	-	60	mA	3,4 5
		TC514100ASJ/AZ/AFT-70	-	60		
		TC514100ASJ/AZ/AFT-80	-	50		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC514100ASJ/AZ/AFT-60	-	120	mA	3, 5
		TC514100ASJ/AZ/AFT-70	-	100		
		TC514100ASJ/AZ/AFT-80	-	85		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV<V_{IN}<6.5V, All Other Pins Not Under Test=OV)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (OV<V_{OUT}<5.5V),		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC514100ASJ/AZ/AFT						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	135	-	155	-	175	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	70	-	70	-	75	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Uup Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ACH}	Column Address Set-Up Time	0	-	0	-	0	0	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514100ASJ/AZ/AFT						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	16	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	20	-	30	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	60	-	70	-	80	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	-	35	-	40	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	40	-	40	-	45	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	30	-	40	-	40	-	ns	
t_{WTS}	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	10		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC514100ASJ/AZ/AFT						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	155	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	50	-	55	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	-	85	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	25	ns	9, 14
t_{AA}	Access Time from Column Address	-	35	-	40	-	45	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	45	-	50	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	85	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	85	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	85	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	45	-	45	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	45	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	
C_O	Input Capacitance (D_{OUT})	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

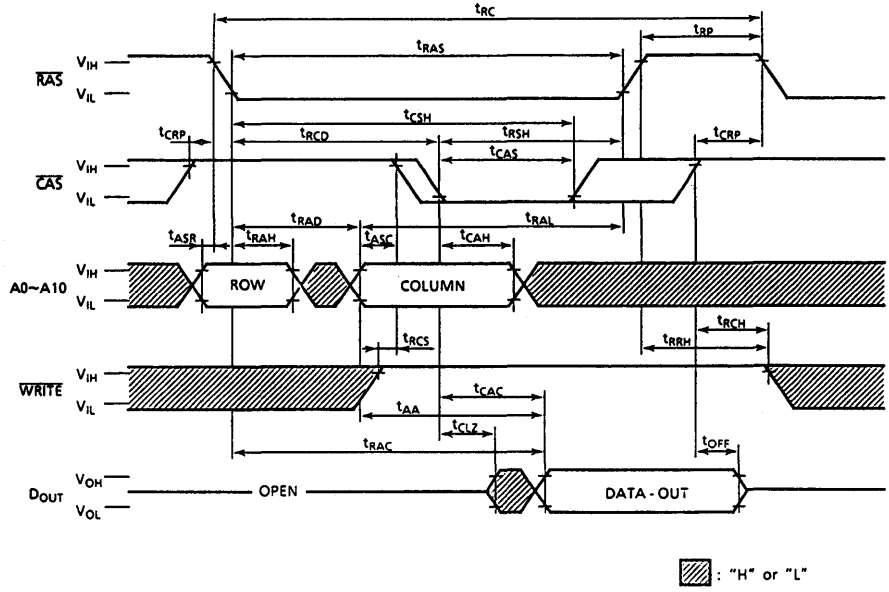
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

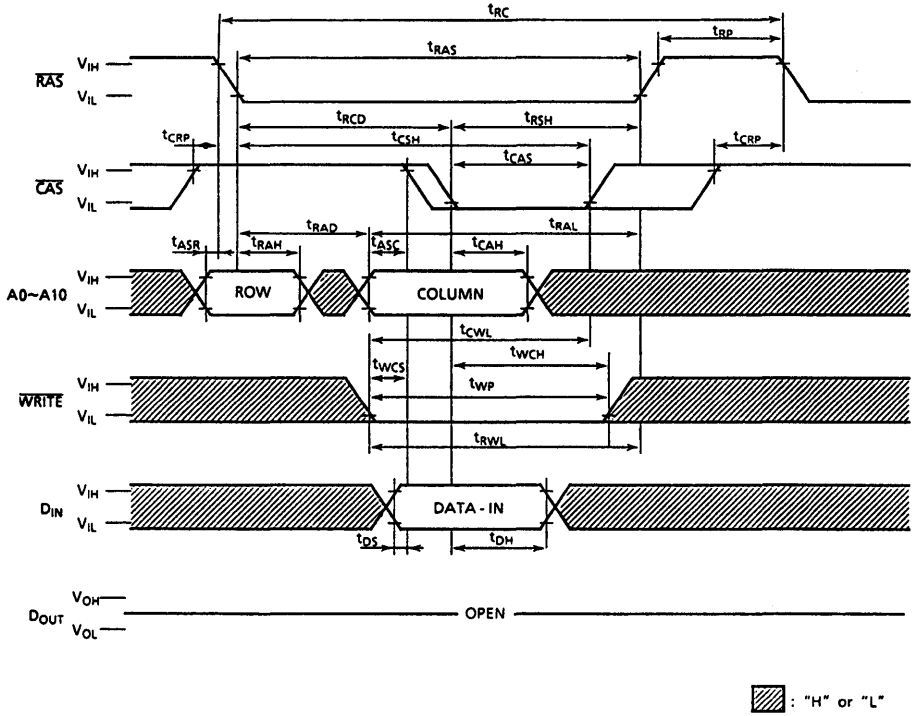
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

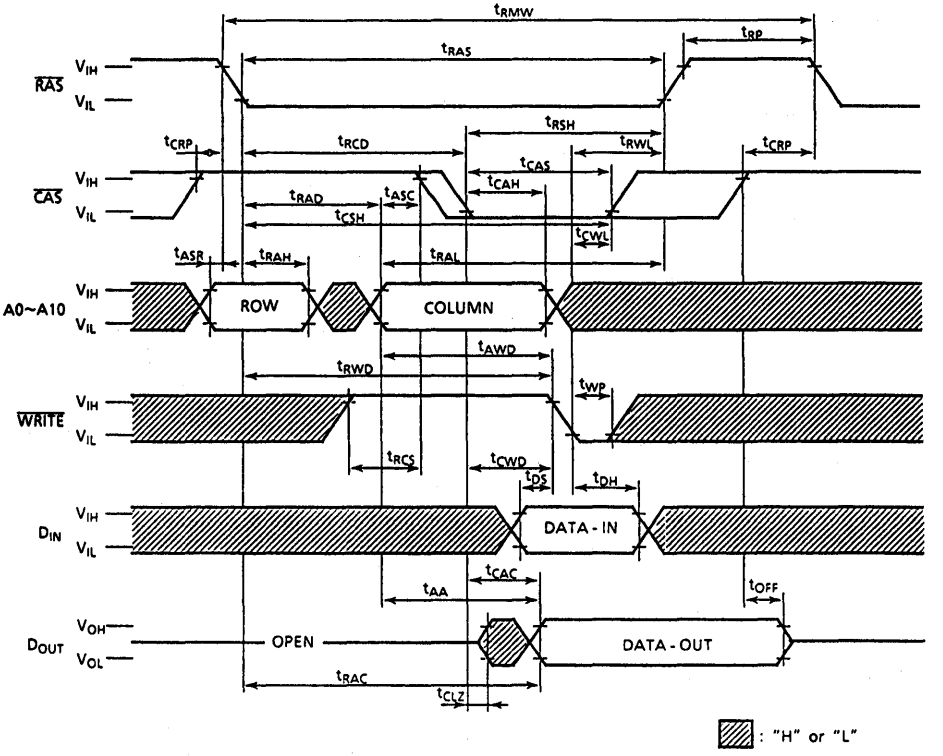
READ CYCLE



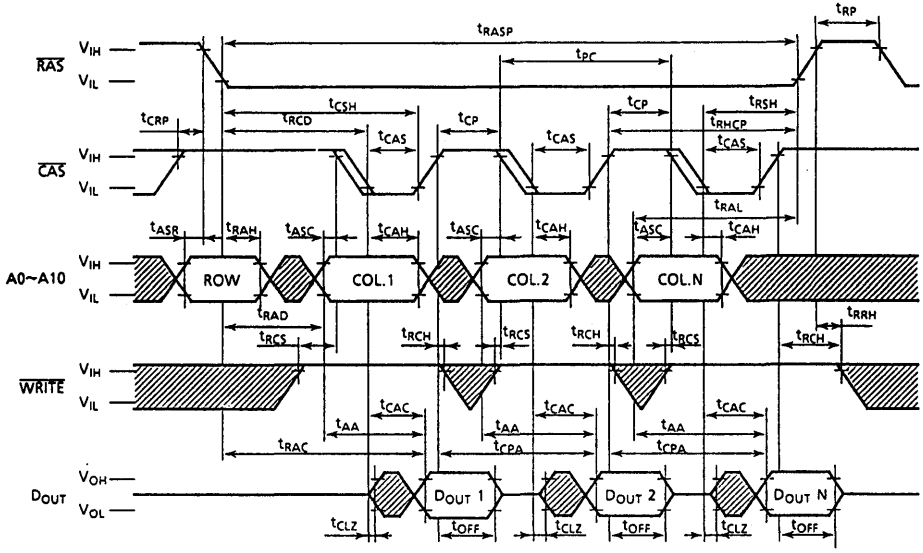
WRITE CYCLE (EARLY WRITE)



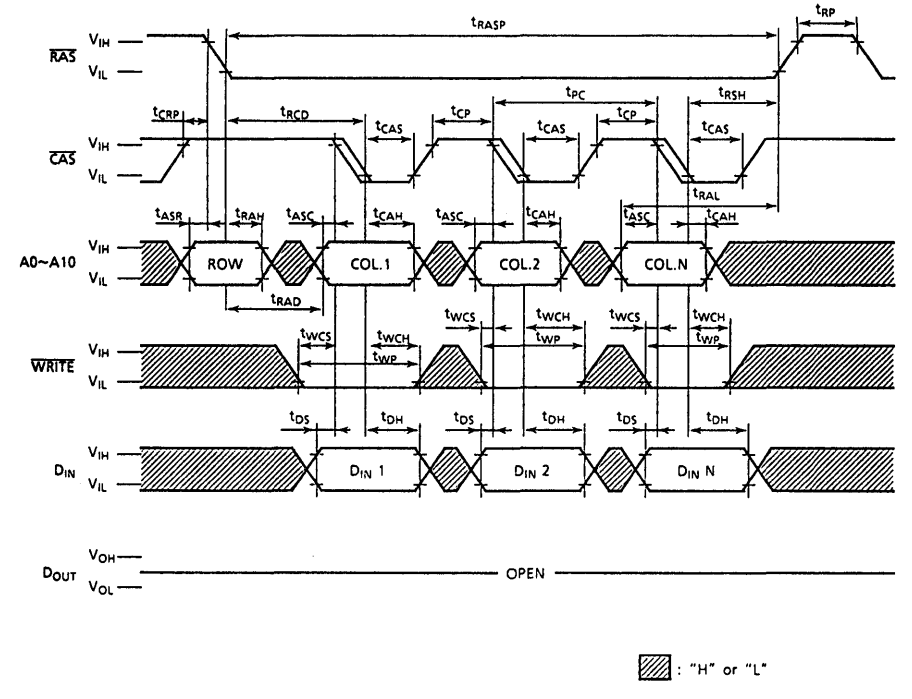
READ-MODIFY-WRITE CYCLE



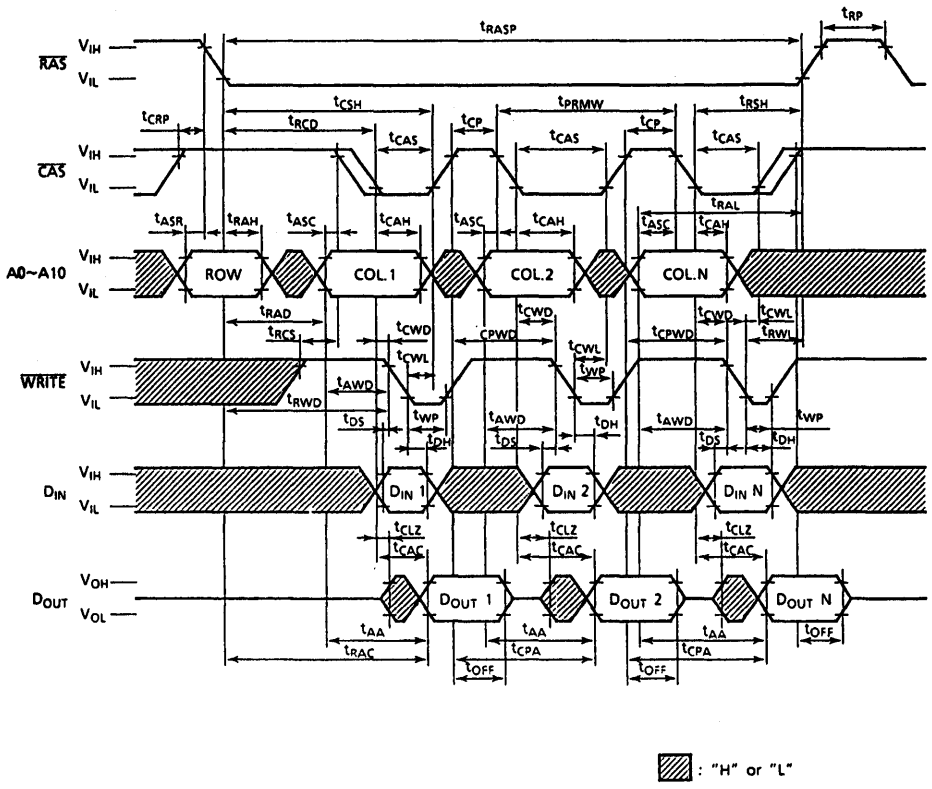
FAST PAGE MODE READ CYCLE



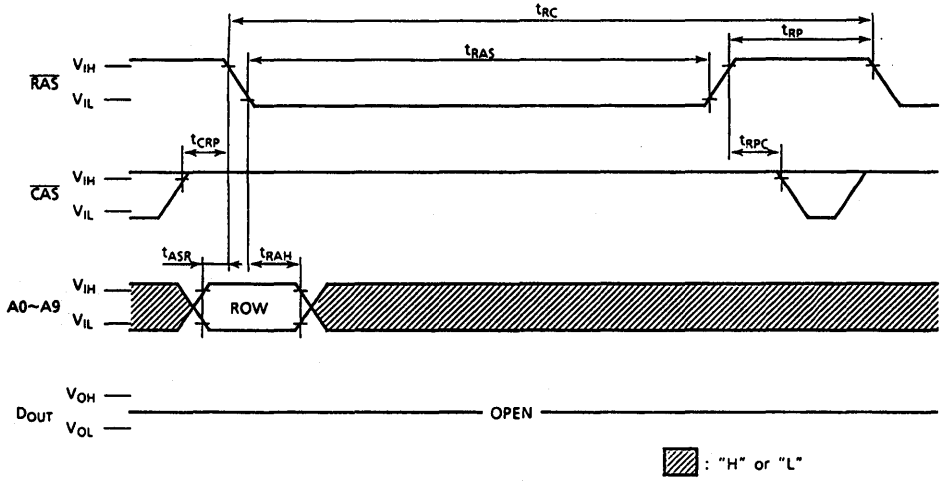
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

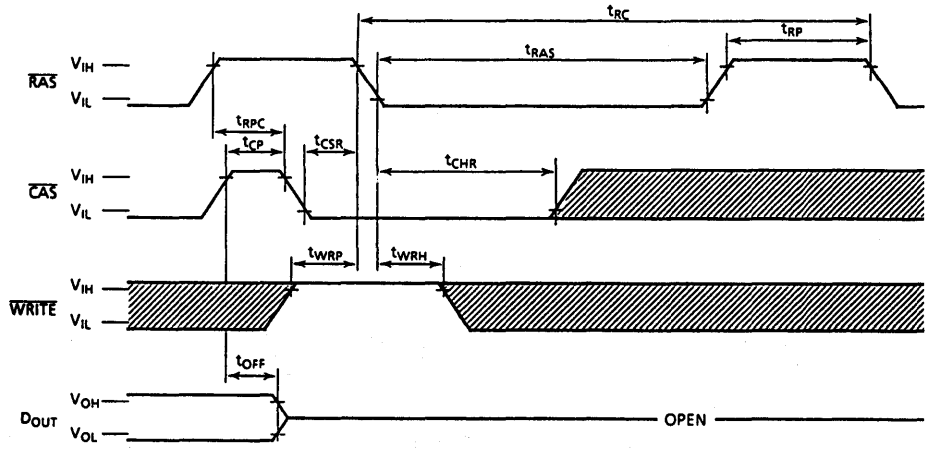


$\overline{RAS}$ ONLY REFRESH CYCLE



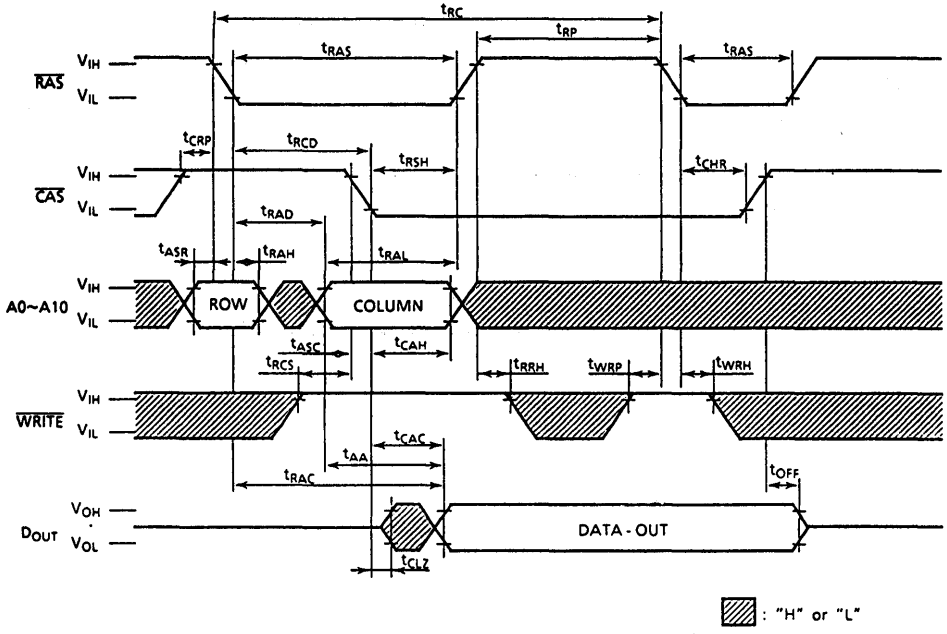
Note : $\overline{WRITE}$, A10 = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

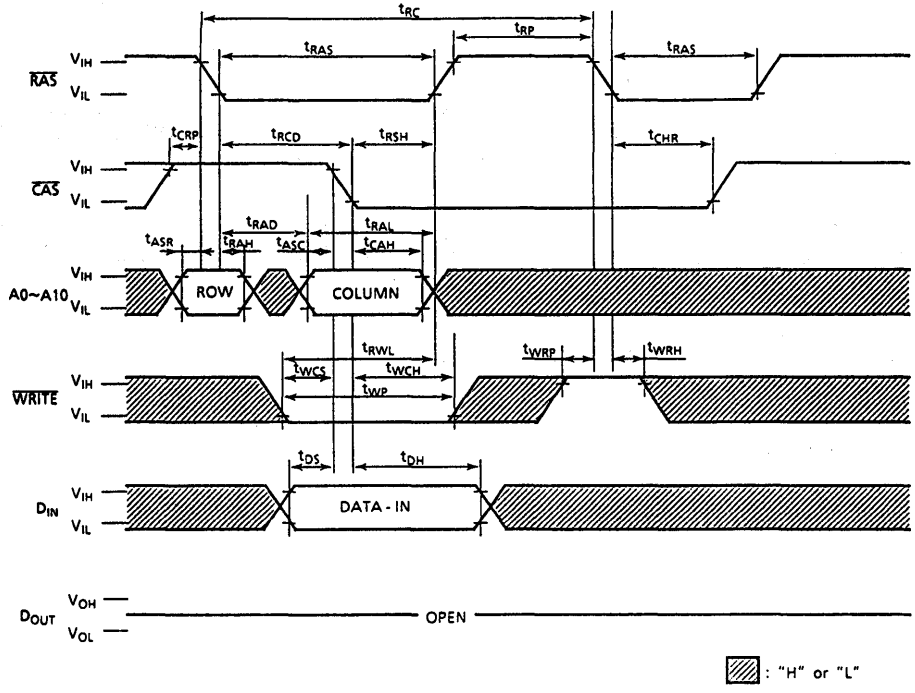


Note : A0~A10 = "H" or "L"

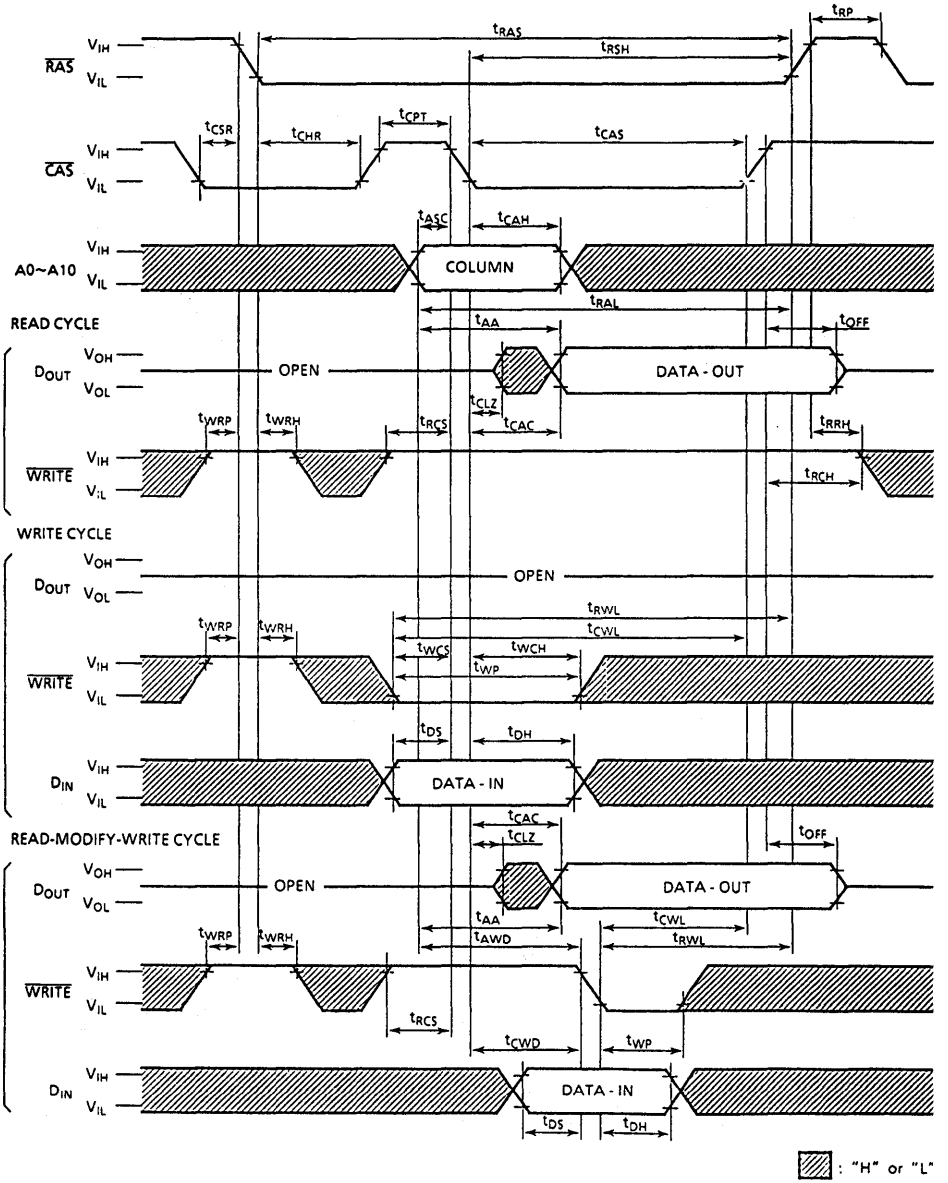
HIDDEN REFRESH CYCLE (READ)



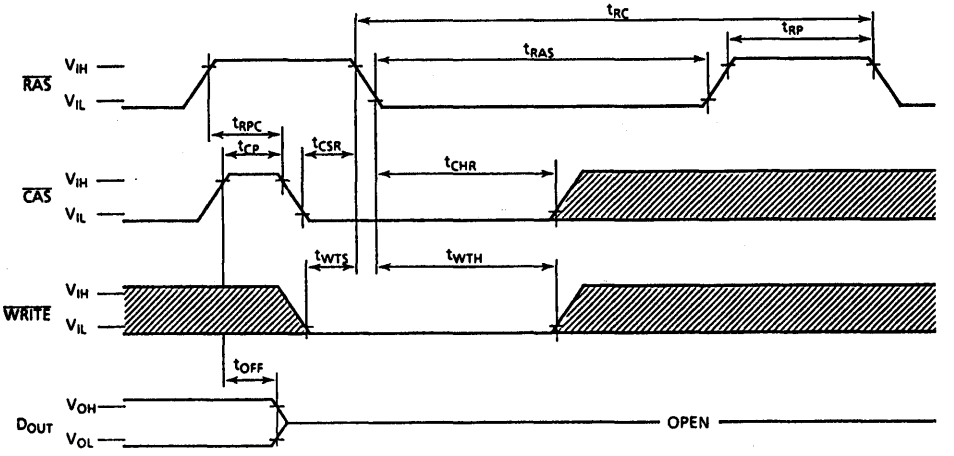
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



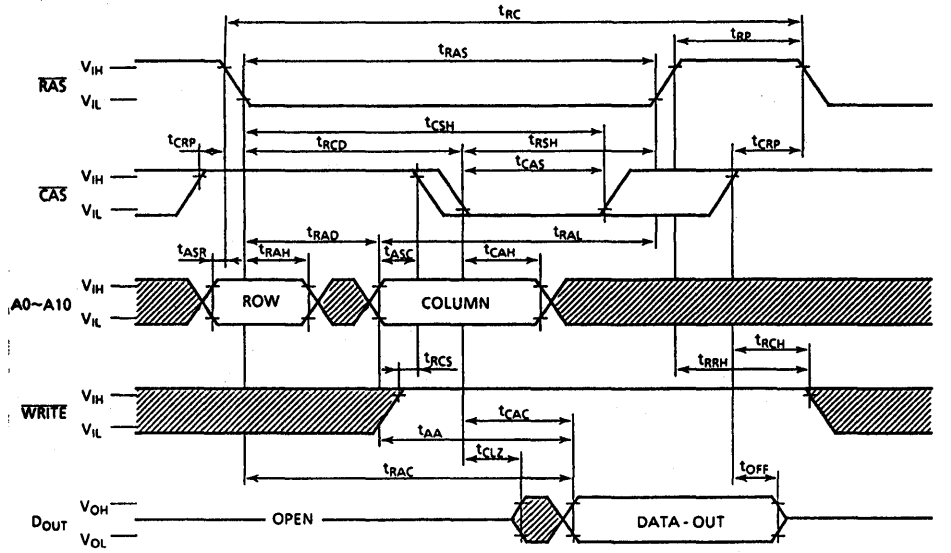
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, A0~A10 = "H" or "L"

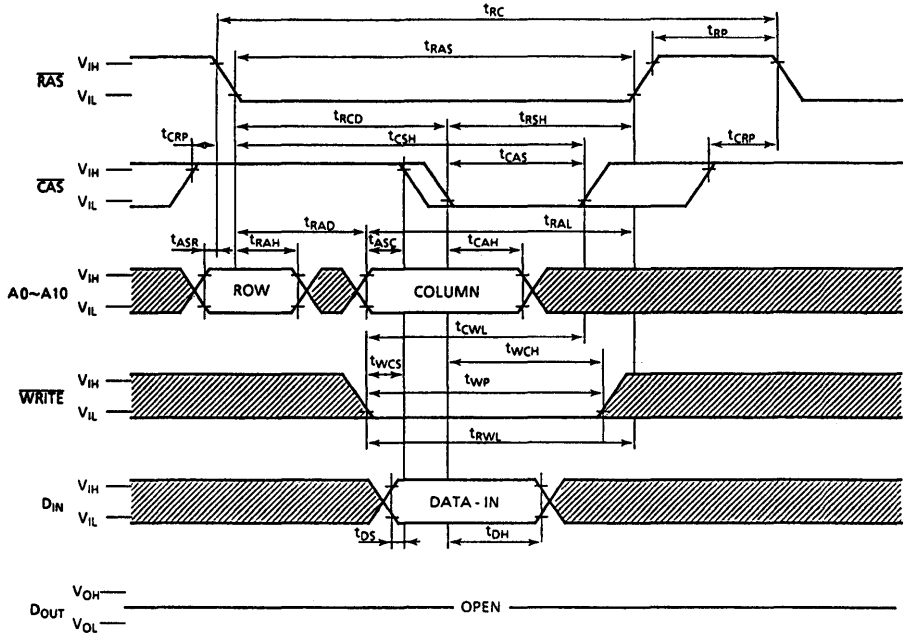
▨ : "H" or "L"

READ CYCLE IN THE TEST MODE

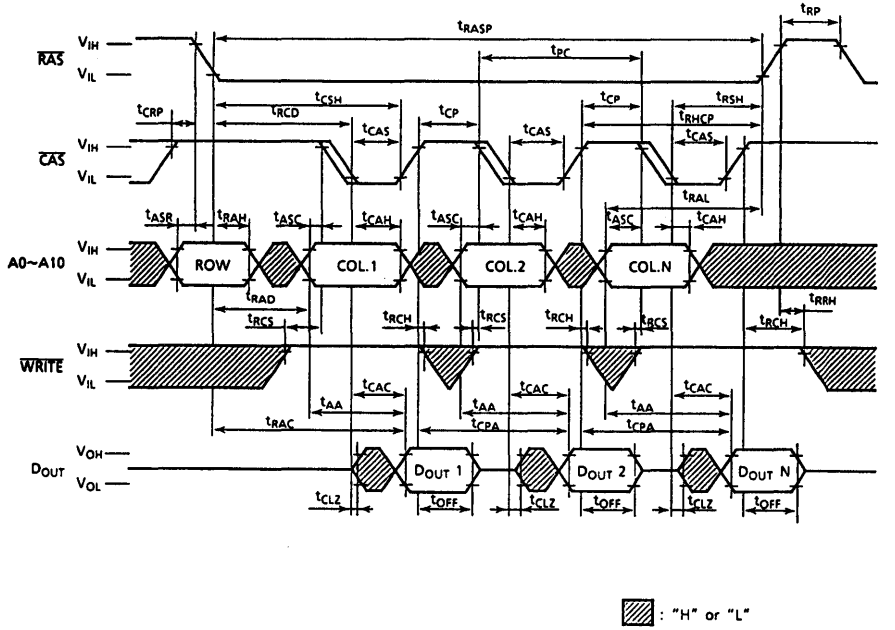


▨ : "H" or "L"

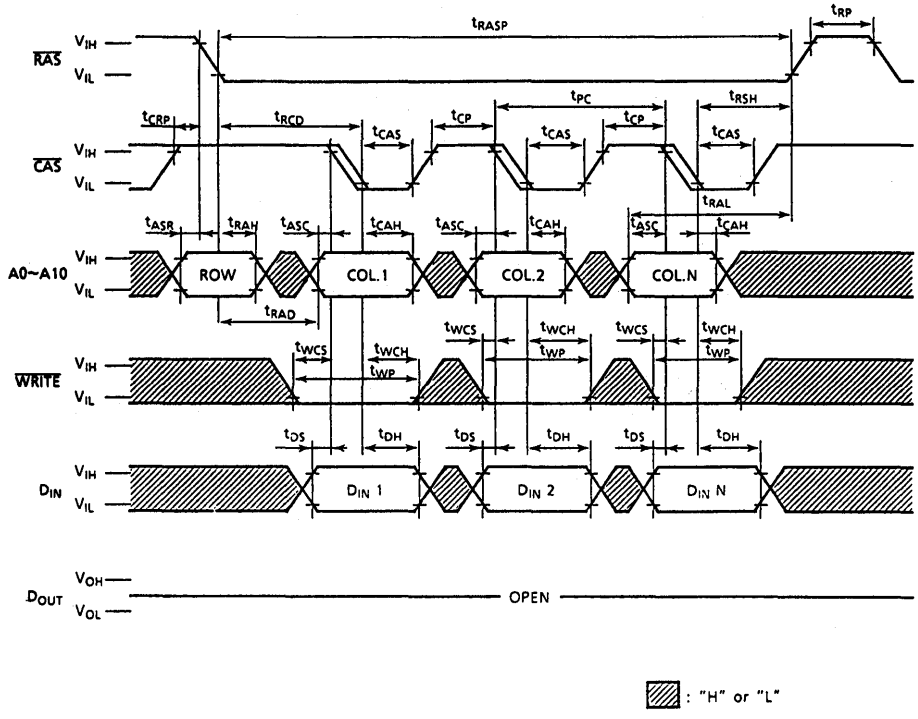
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



FAST PAGE MODE READ CYCLE IN THE TEST MODE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



TEST MODE

The TC514100/ASJ/AZ/AFT is the RAM organized 4,194,304 words by 1 bits, internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} is not used. If, upon reading, all bits equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0". Fig. 1 shows the block diagram of TC51400/ASJ/AZ/AFT. In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

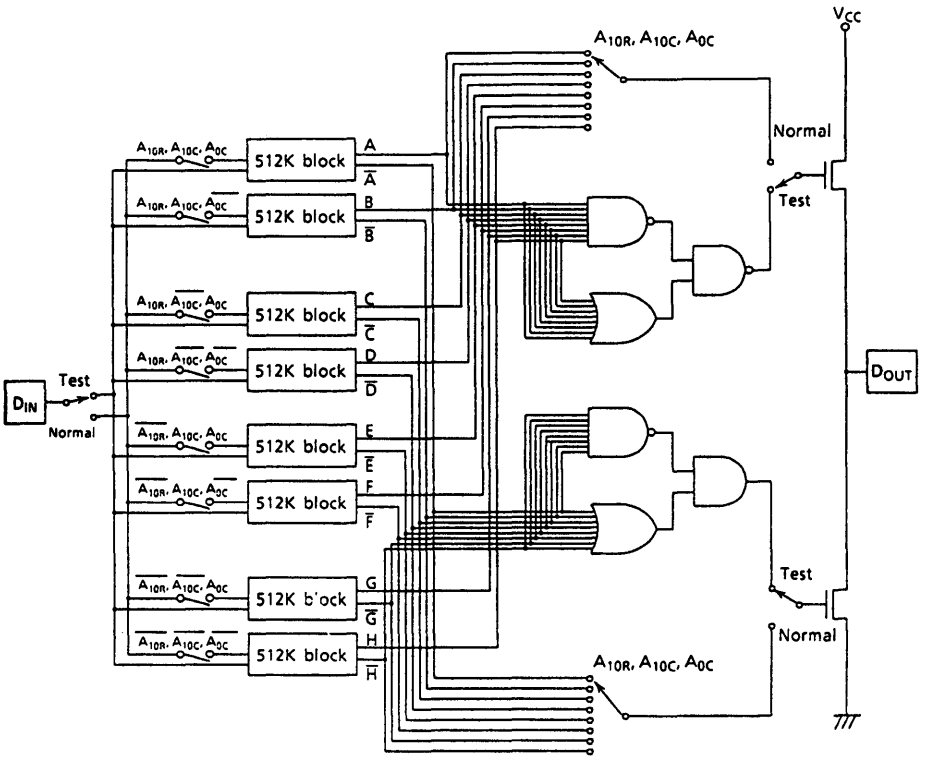


Figure 1

4,194,304 WORD X 1 BIT DYNAMIC RAM

DESCRIPTION

The TC514100ASJL/AFTL is the new generation dynamic RAM organized 4,194,304 word by 1 bit. The TC514100ASJL/AFTL utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514100ASJL/AFTL to be packaged in a standard 26/20 pin plastic SOJ (300), 26/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  660mW MAX .Operating
  (TC514100ASJL/AFTL-60)
  550mW MAX. Operating
  (TC514100ASJL/AFTL-70)
  468mW MAX. Operating
  (TC514100ASJL/AFTL-80)
  1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514400ASJL : SOJ26-P-300A
  TC514400AFTL : TSOP26-P-300

KEY PARAMETERS

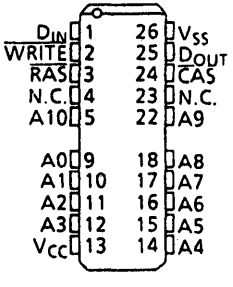
ITEM		TC514100ASJL/AFTL		
		-60	-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC}	Cycle Time	110ns	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAME

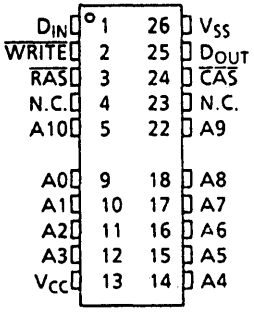
A0~A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

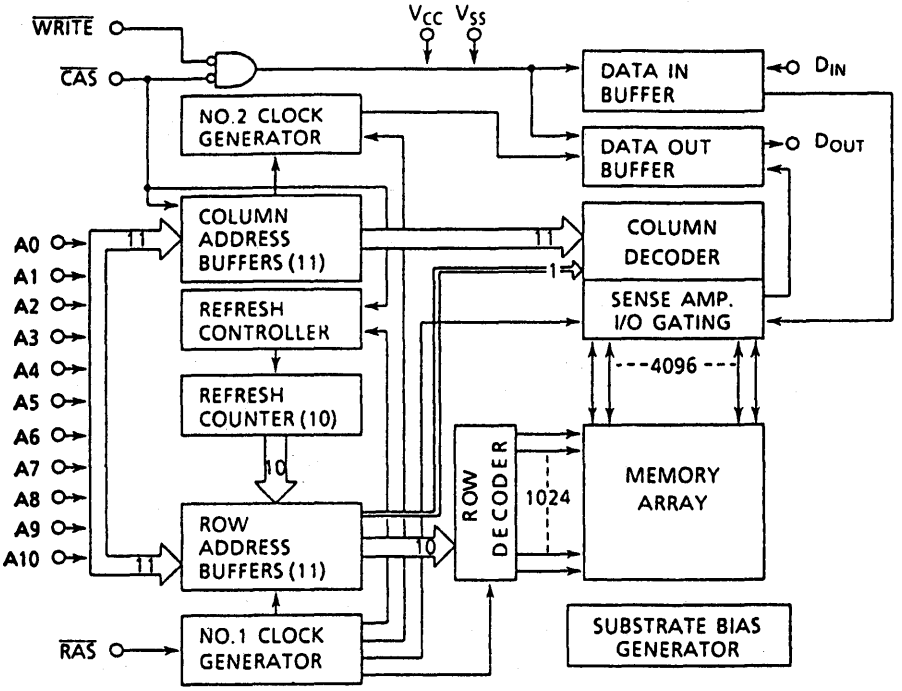
Plastic SOJ



Plastic TSOP (Normal Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514100ASJL/AFTL-60	-	120	mA	3,4 5
		TC514100ASJL/AFTL-70	-	100		
		TC514100ASJL/AFTL-80	-	85		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514100ASJL/AFTL-60	-	120	mA	3, 5
		TC514100ASJL/AFTL-70	-	100		
		TC514100ASJL/AFTL-80	-	85		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	TC514100ASJL/AFTL-60	-	60	mA	3,4 5
		TC514100ASJL/AFTL-70	-	60		
		TC514100ASJL/AFTL-80	-	50		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			200	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC514100ASJL/AFTL-60	-	120	mA	3, 5
		TC514100ASJL/AFTL-70	-	100		
		TC514100ASJL/AFTL-80	-	85		
I_{CC7}	Battery Back Up Current Average Power Suuply Current, Battery Back Up Mode ($\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{WRITE}$=V_{CC}-0.2V A0~10=V_{CC}-0.2V or 0.2V, D_{IN}==Vcc-0.2V, 0.2V or OPEN: t_{RC}=125µs, t_{RAS}=t_{RES} MIN. ~1µs)		-	300	µA	3.6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	µA	
V_{OH}	OUTPUT LEAKAGE CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEAKAGE CURRENT Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 7,8,9)

SYMBOL	PARAMETER	TC514100ASJL/AFTL						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	135	-	155	-	175	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	70	-	70	-	75	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	10,15, 16
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	20	ns	10,15
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	40	-	45	-	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	0	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	12
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514100ASJL/AFTL						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	13
t_{DH}	Data Hold Time	15	-	15	-	15	-	ns	13
t_{REF}	Refresh Period	-	128	-	128	-	128	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	20	-	20	-	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	60	-	70	-	80	-	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	-	35	-	40	-	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	40	-	40	-	45	-	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	30	-	40	-	40	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	10		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE (V_{CC} = 5V ± 10%,Ta = 0~70°C(Notes 7,8,9)

SYMBOL	PARAMETER	TC514100ASJL/AFTL						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	155	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	50	-	55	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	-	85	ns	10,15, 16
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	25	ns	10,15
t_{AA}	Access Time from Column Address	-	35	-	40	-	45	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	45	-	50	ns	10
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	85	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	85	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	85	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	-	45	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	45	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$,)	-	7	pF
C_O	Input Capacitance (D_{OUT})	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. t_{RAS} (max.)=1μs is only applied to refresh of battery-back up. t_{RAS} (max.)=10μs is applied to functional operating.

7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

8. AC measurements assume t_T=5ns.

9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

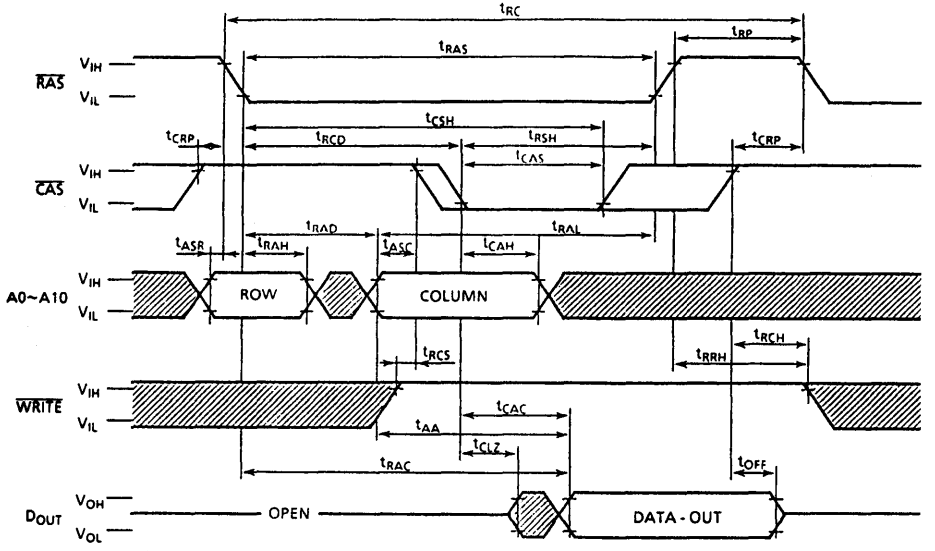
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWP} > t_{CPWDD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

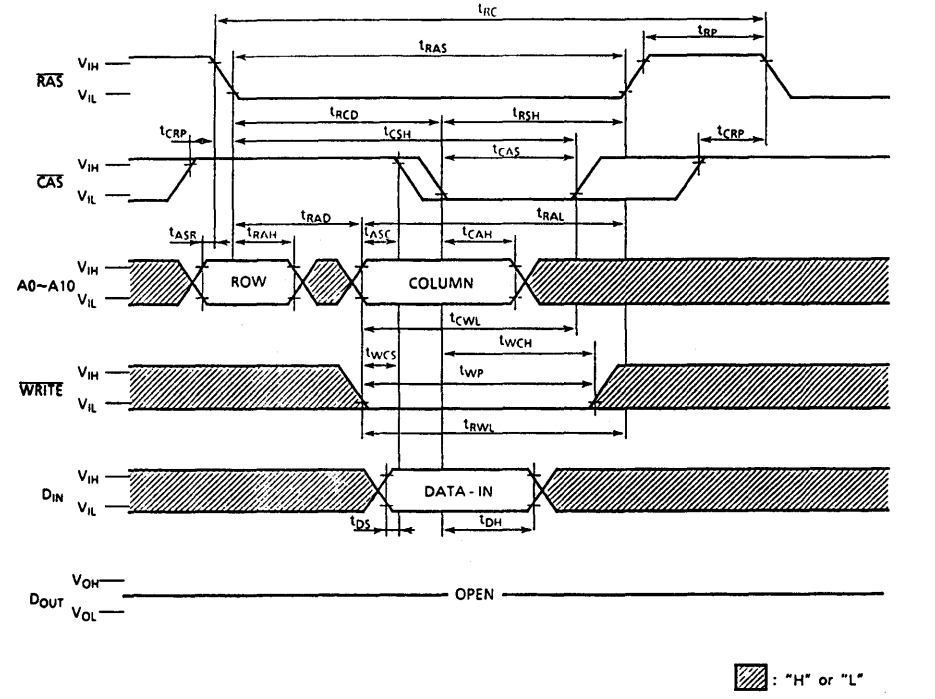
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

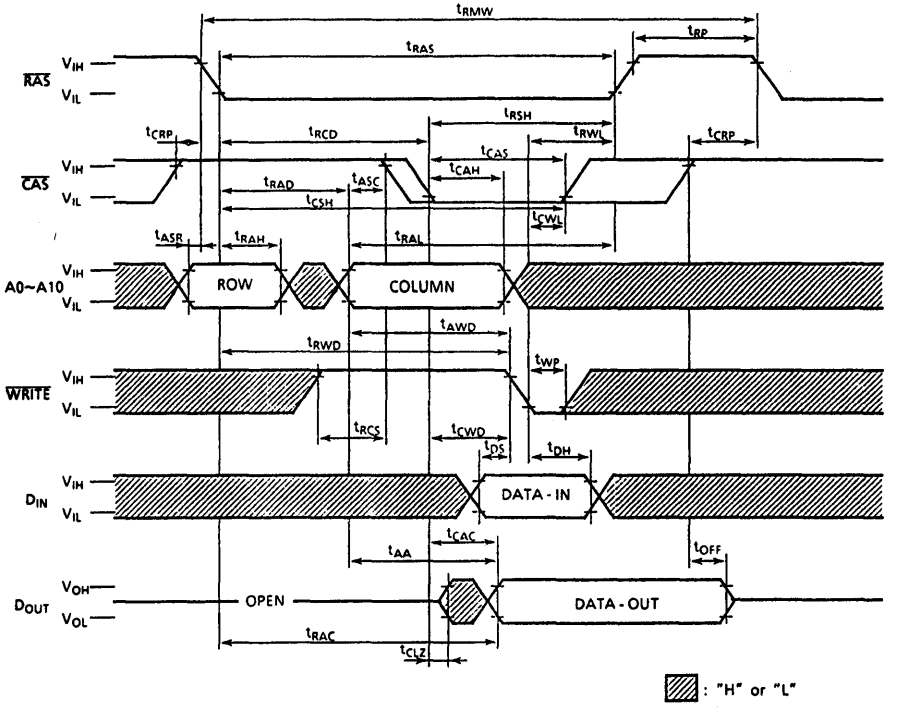
READ CYCLE



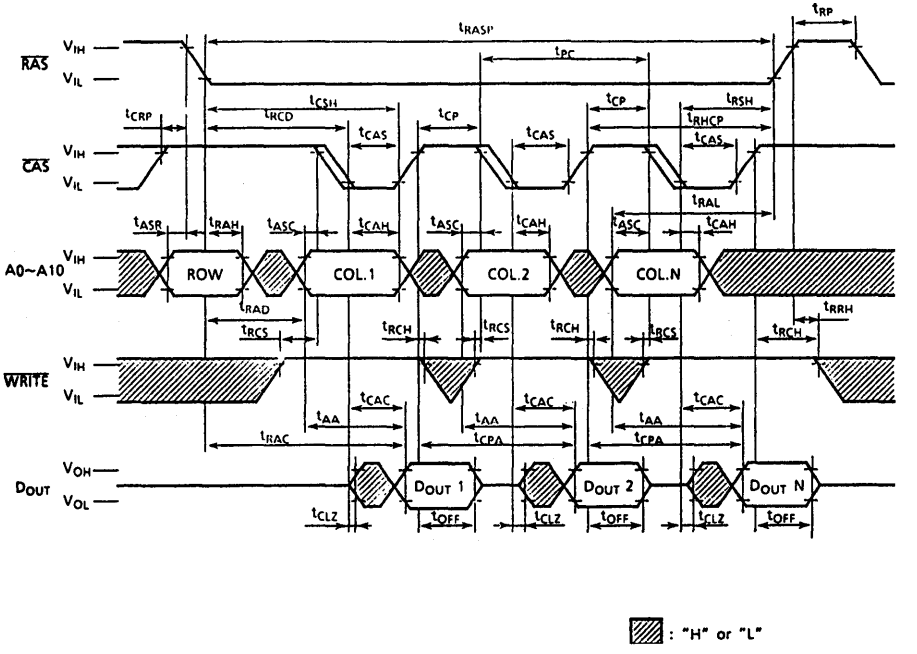
WRITE CYCLE (EARLY WRITE)



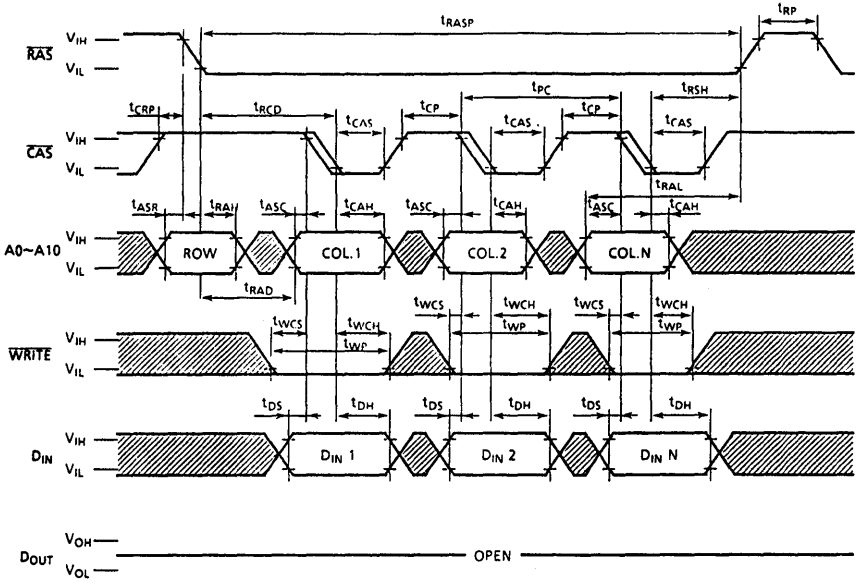
READ-MODIFY-WRITE CYCLE



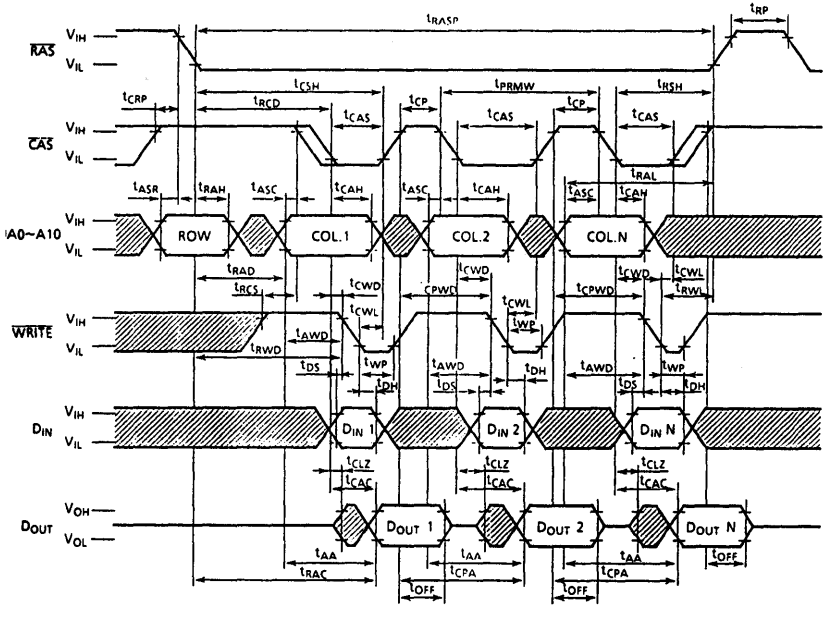
FAST PAGE MODE READ CYCLE



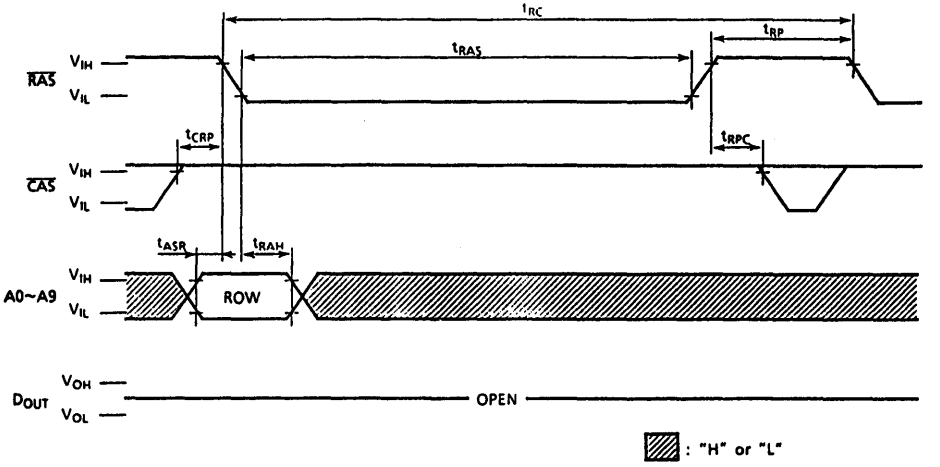
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

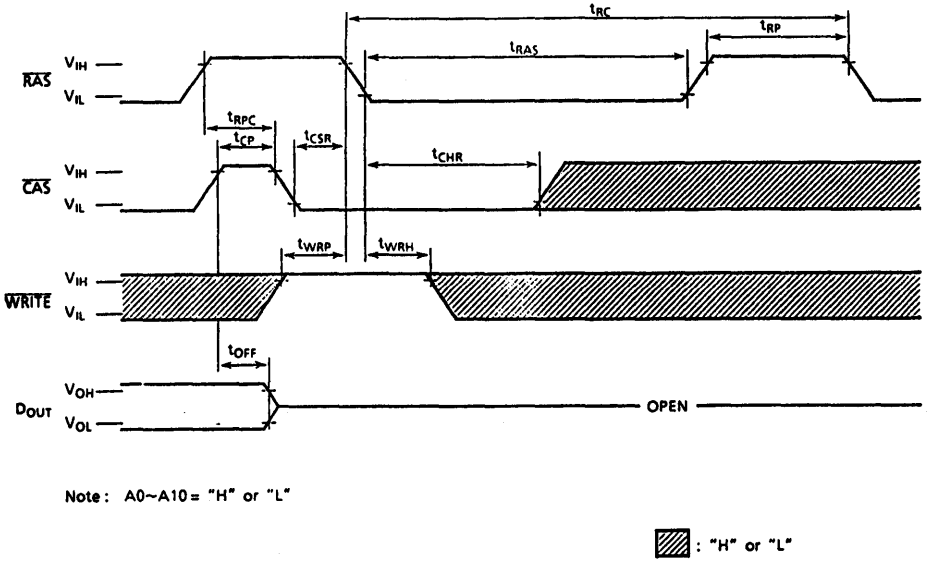


$\overline{RAS}$ ONLY REFRESH CYCLE



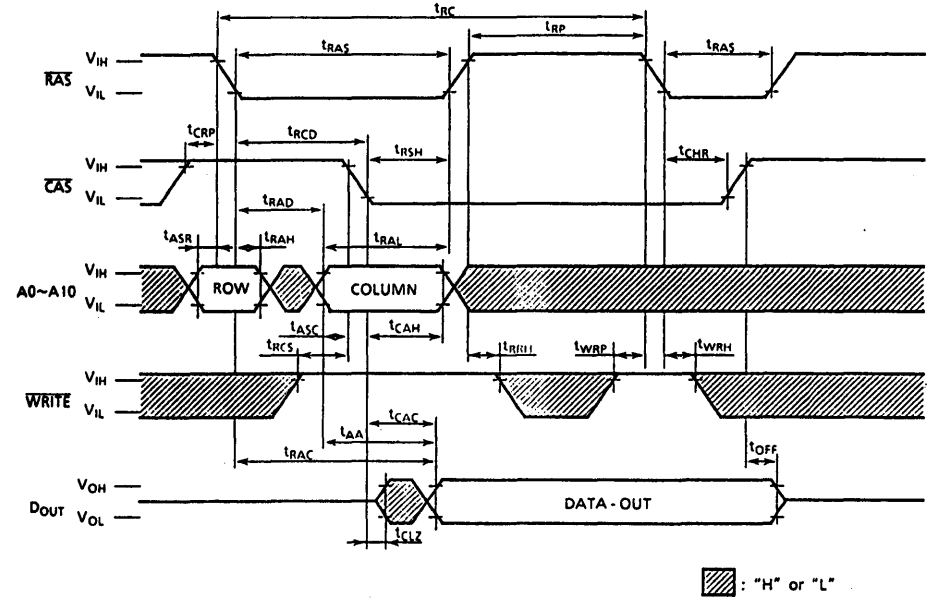
Note: $\overline{WRITE}$, A10 = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

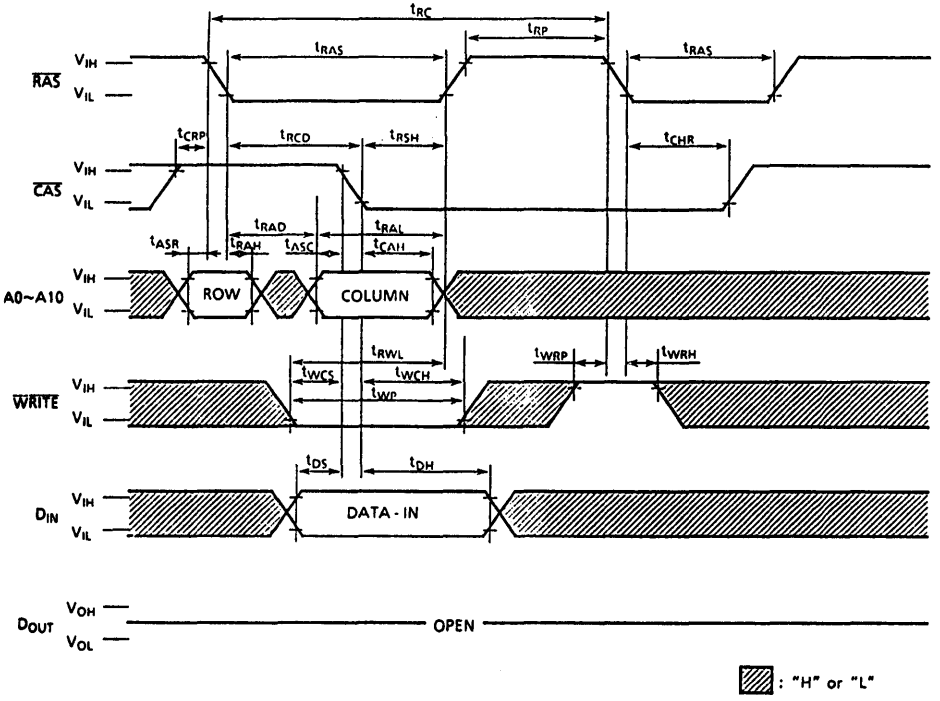


Note: A0~A10 = "H" or "L"

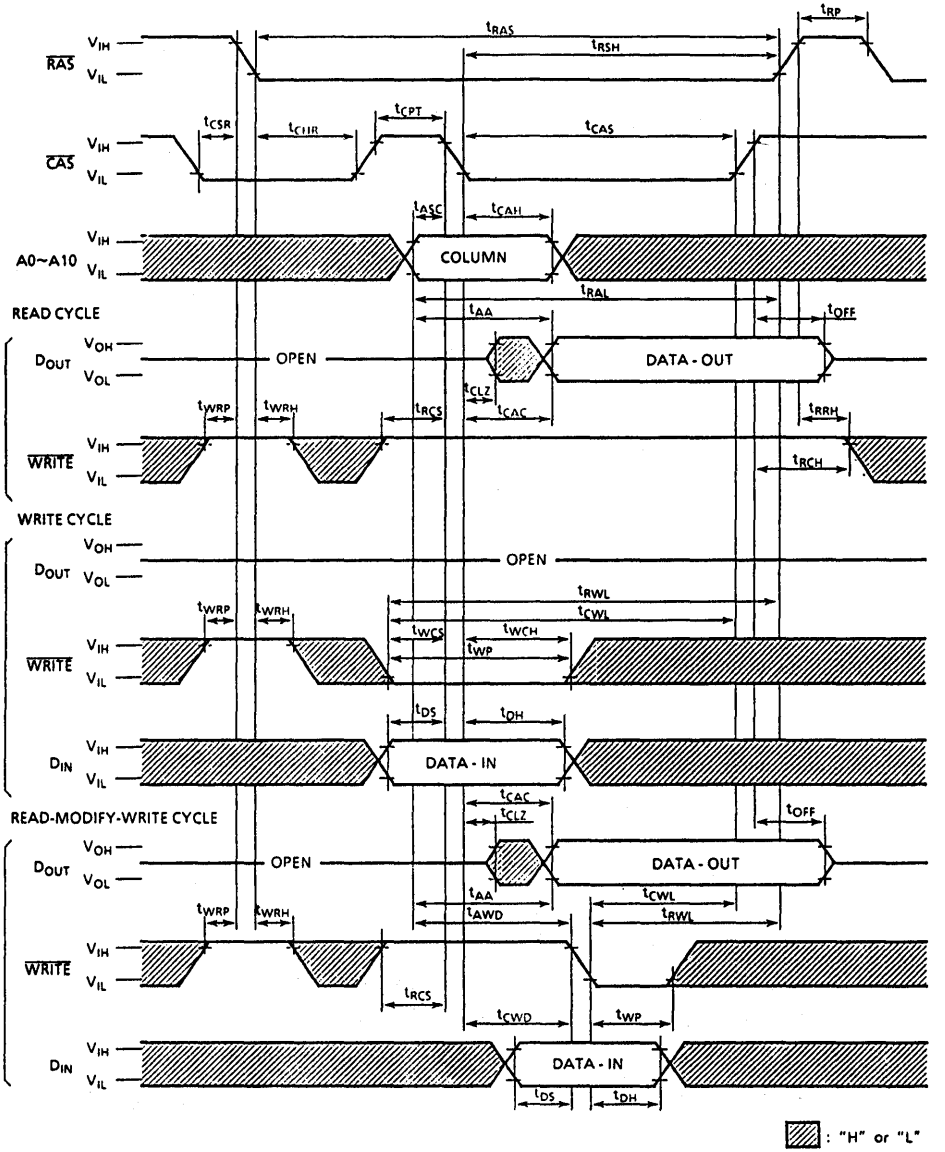
HIDDEN REFRESH CYCLE (READ)



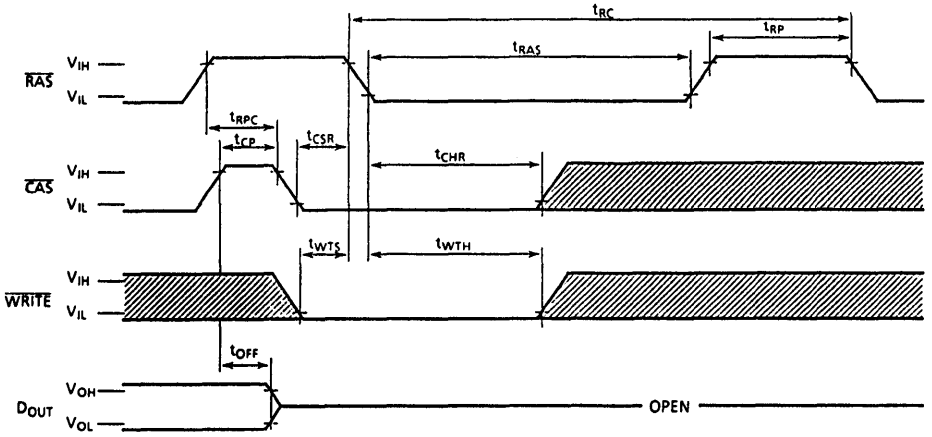
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



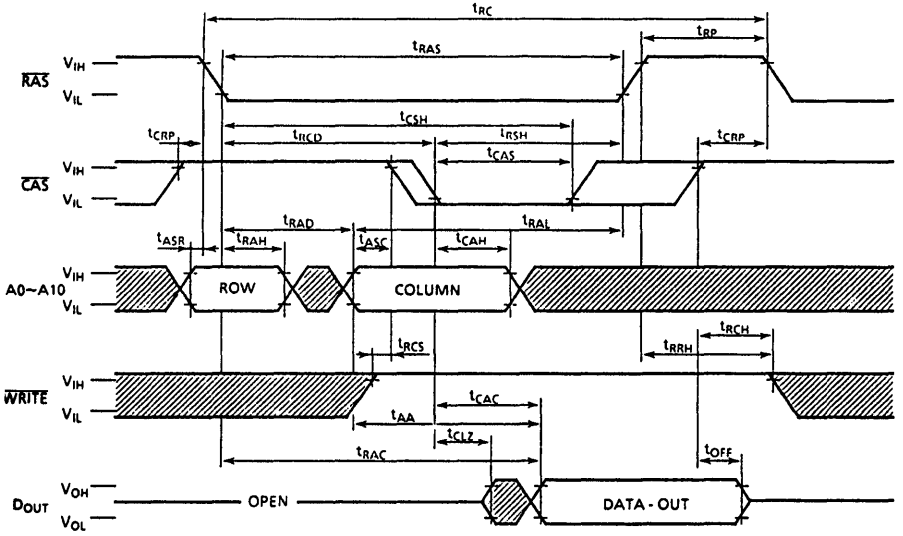
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note : D_{IN}, A0~A10 = "H" or "L"

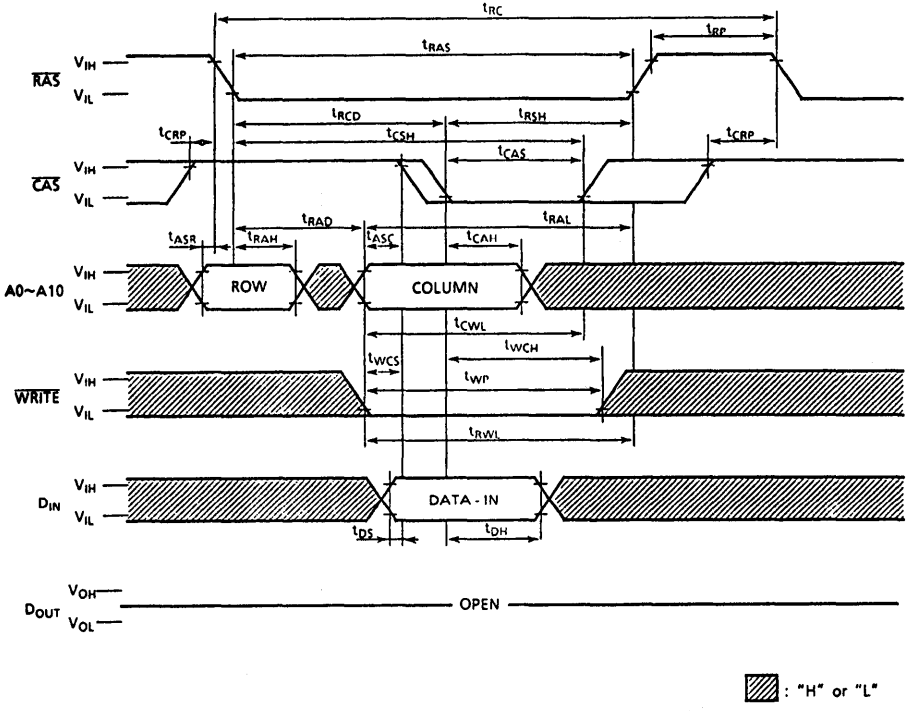
▨ : "H" or "L"

READ CYCLE IN THE TEST MODE

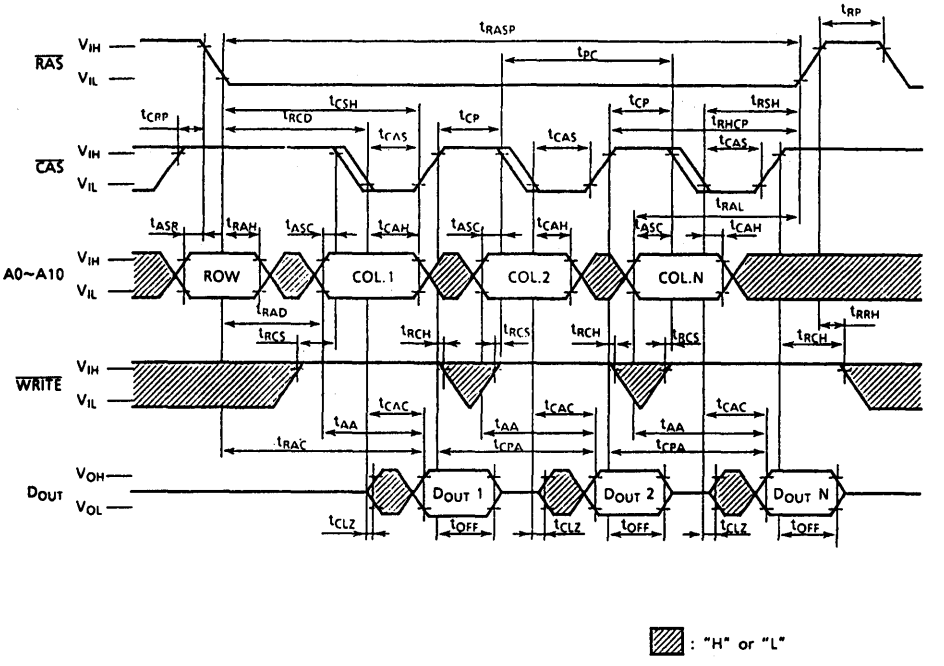


▨ : "H" or "L"

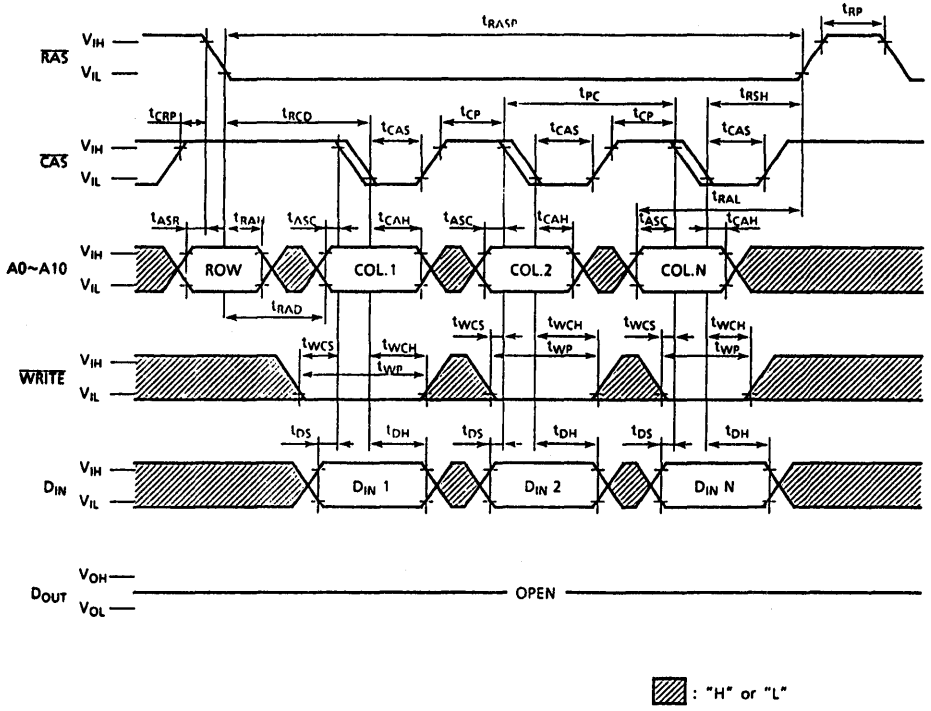
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



FAST PAGE MODE READ CYCLE IN THE TEST MODE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



TEST MODE

The TC514100ASJL/AFTL is the RAM organized 4,194,304 words by 1 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits equal (all "1"s or "0"s), the data output pin indicates a"1". If any of the bits differed, the data output pin would indicate a "0". Fig. 1 shows the block diagram of TC514100ASJL/AFTL. In "Test Mode", the DRAM can be tested as if it were a 512K DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/8 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

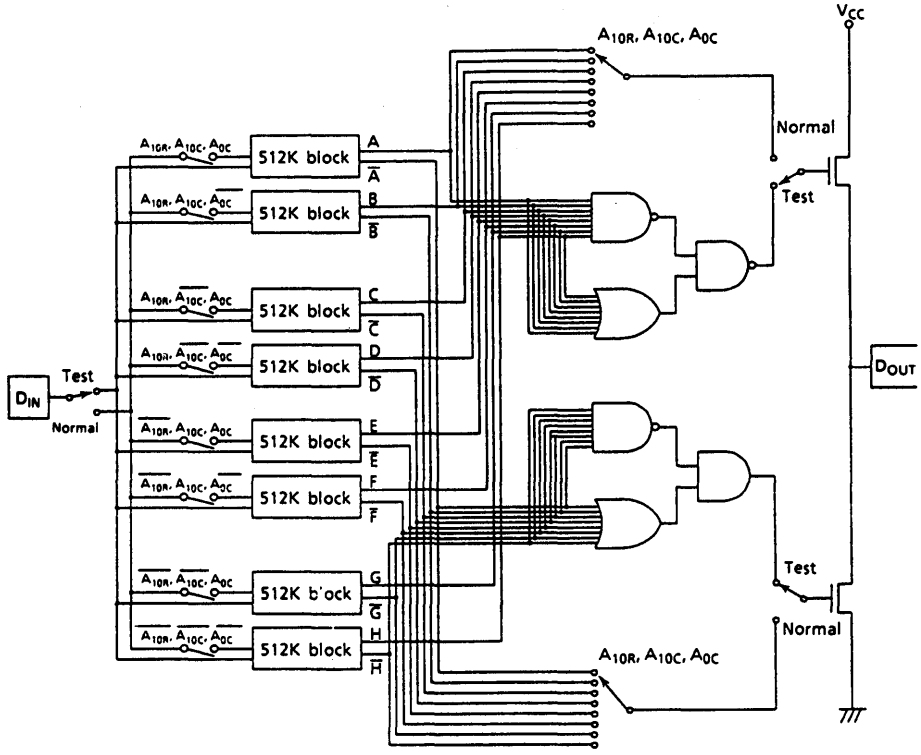


Figure 1

16,777,216 WORD X 1 BIT DYNAMIC RAM

DESCRIPTION

The TC5116100J/Z/FT is the new generation dynamic RAM organized 16,777,216 word by 1 bit. The TC5116100J/Z/FT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5116100J/Z/FT to be packaged in a standard 28/24 pin plastic SOJ, 24 pin plastic ZIP and 28/24 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 16,777,216 word by 1 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  495mW MAX .Operating
  (TC5116100J/Z/FT/TR-60)
  440mW MAX. Operating
  (TC5116100J/Z/FT/TR-70)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 4096 refresh cycles/64ms
- Package TC5116100J : SOJ28-P-400A
  TC5116100Z : ZIP24-P-475
  TC5116100FT : TSOP28-P-400B

KEY PARAMETERS

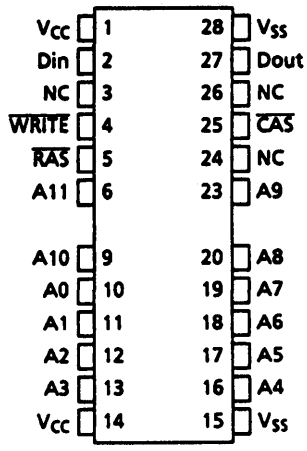
ITEM		TC5116100J/Z/FT	
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

PIN NAME

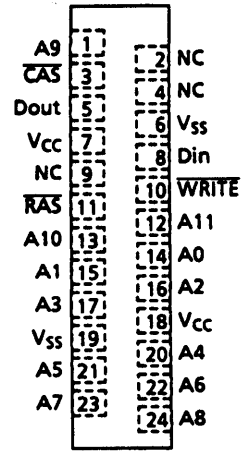
A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C	No Connection

PIN CONNECTION (TOP VIEW)

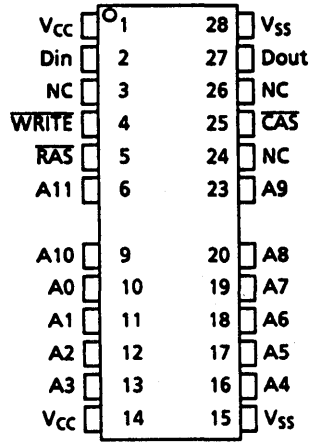
Plastic SOJ



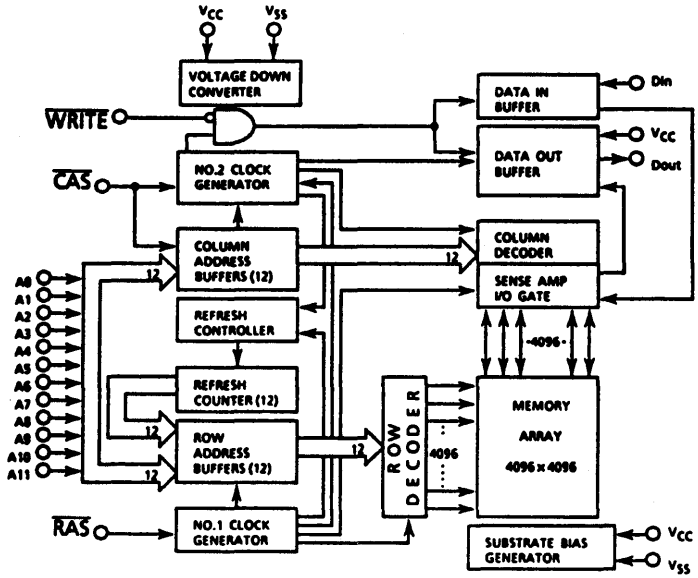
Plastic ZIP



Plastic TSOP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

*This parameter is periodically sampled and is not 100% tested.

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	V_{CC}+0.5	V	2
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V	2

*-2.0V at pulse width ≤ 20ns.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN)	TC5116100J/Z/FT-60	-	90	mA	3,4 5
		TC5116100J/Z/FT-70	-	80		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC5116100J/Z/FT-60	-	90	mA	3, 5
		TC5116100J/Z/FT-70	-	80		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC5116100J/Z/FT-60	-	70	mA	3,4 5
		TC5116100J/Z/FT-70	-	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC5116100J/Z/FT-60	-	90	mA	3, 5
		TC5116100J/Z/FT-70	-	80		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≤V_{IN}≤V_{CC}, All Other Pins Not Under Test=OV)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (OV≤V_{OUT}≤V_{CC}),		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)			0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC5116100J/Z/FT				UNIT	NOTES
		-60		-70			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	ns	
t_{RMW}	Read-Modify-Write Cycle	130	-	155	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	60	-	70	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	400,000	70	400,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC5116100J/Z/FT				UNIT	NOTES
		-60		-70			
		MIN	MAX.	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	10	-	15	-	ns	12
t_{REF}	Refresh Period	-	64	-	64	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	15	-	20	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	60	-	70	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	-	35	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	35	-	40	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	20	-	30	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC5116100J/Z/FT				UNIT	NOTES
		-60		-70			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	9, 14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	400,000	75	400,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold	40	-	45	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead	35	-	40	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A10, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of Icc4, it can be changed once or less during a fast page mode cycle (tPC).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) defines the time at which the output achievsd the open circuit condition and is not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

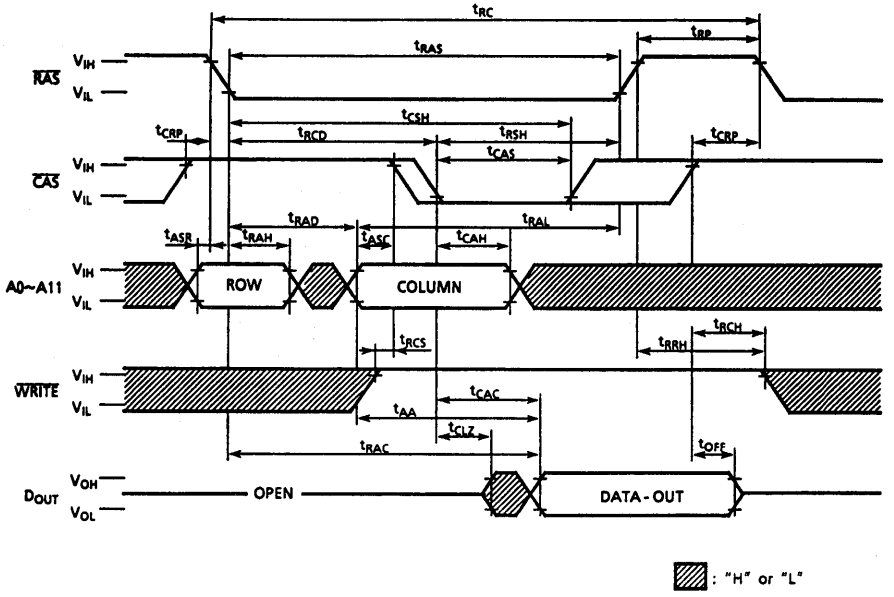
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWP} > t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

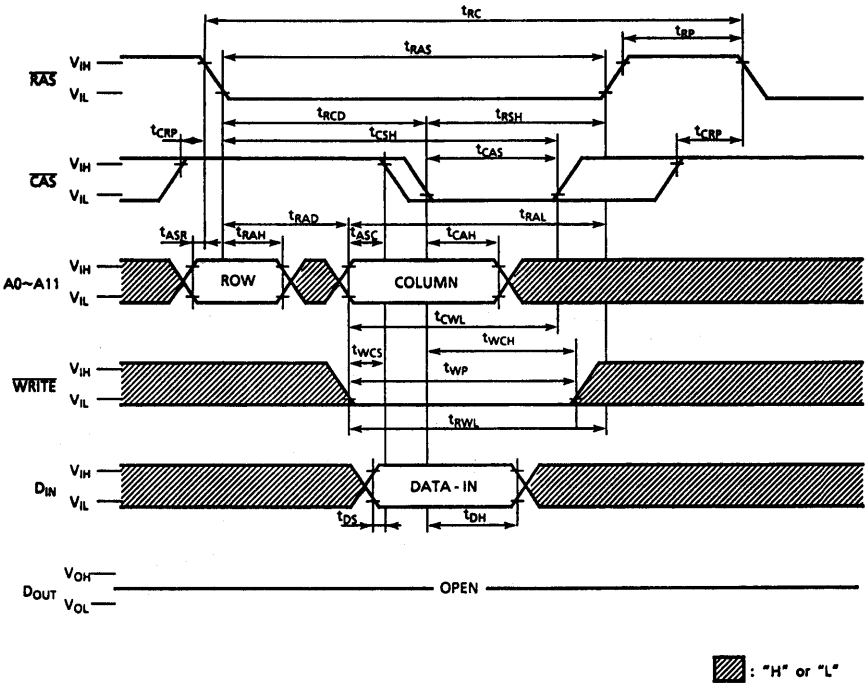
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

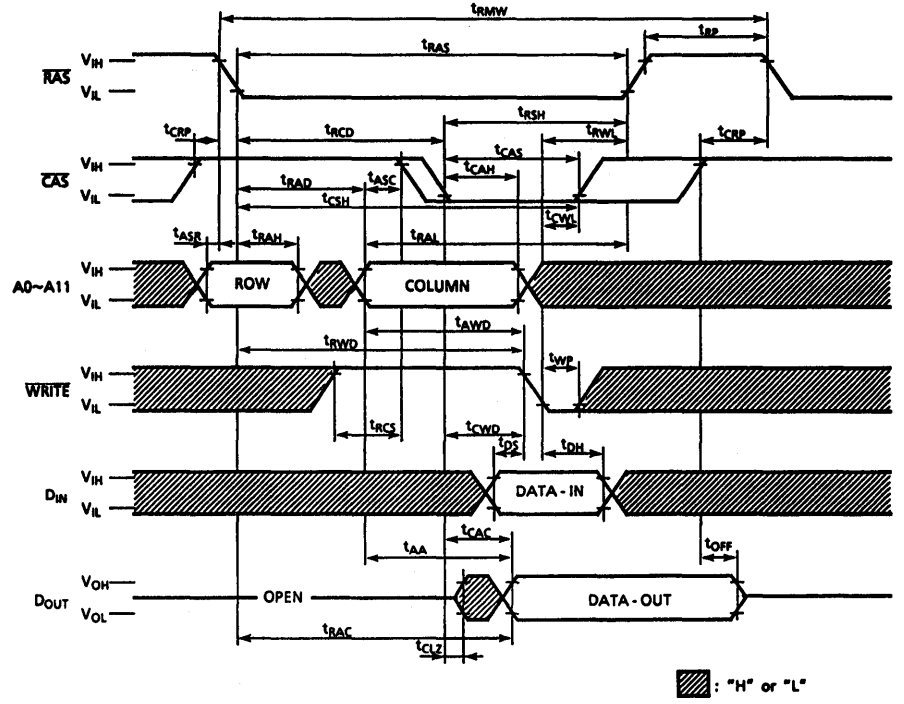
READ CYCLE



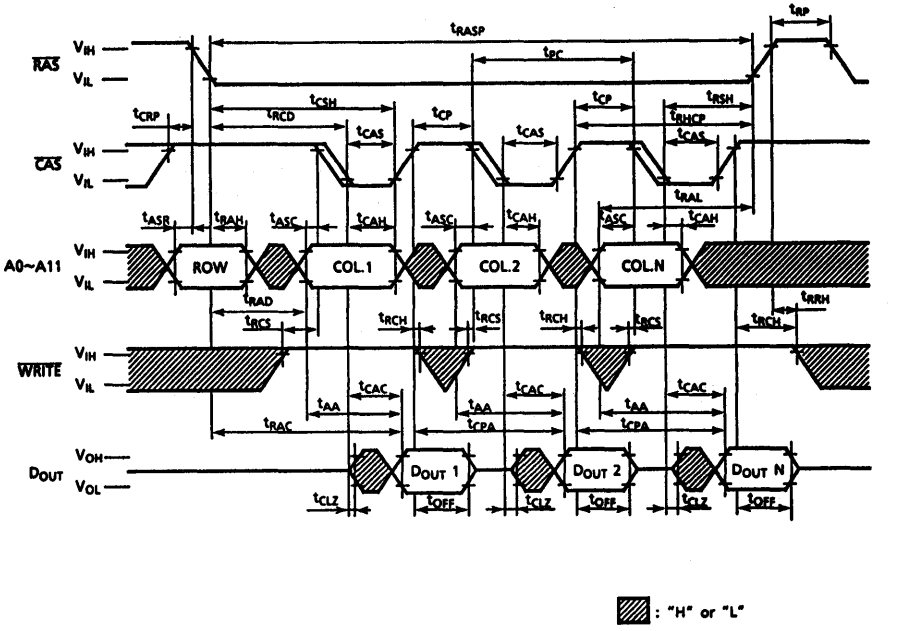
WRITE CYCLE (EARLY WRITE)



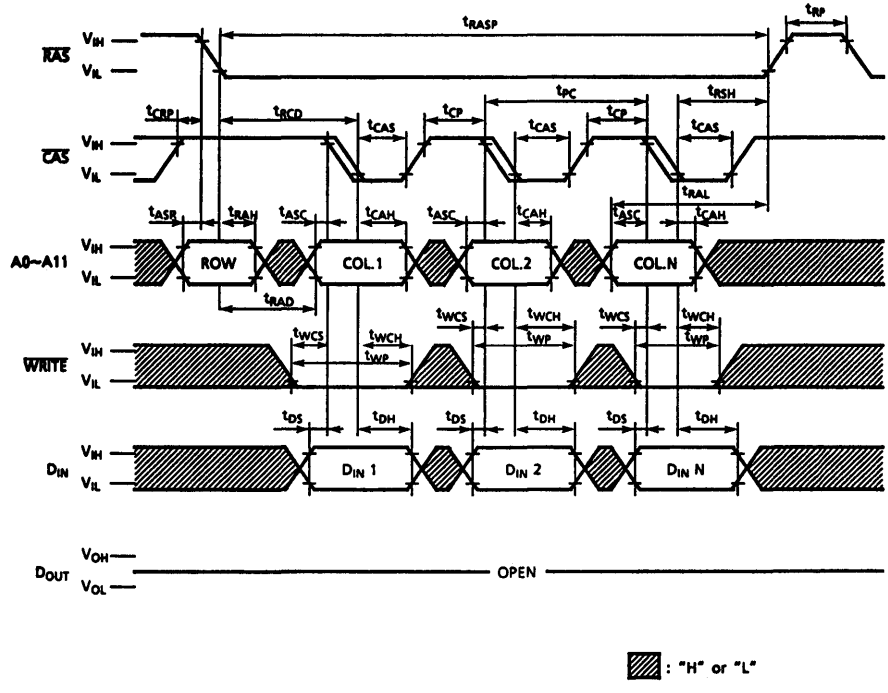
READ-MODIFY-WRITE CYCLE



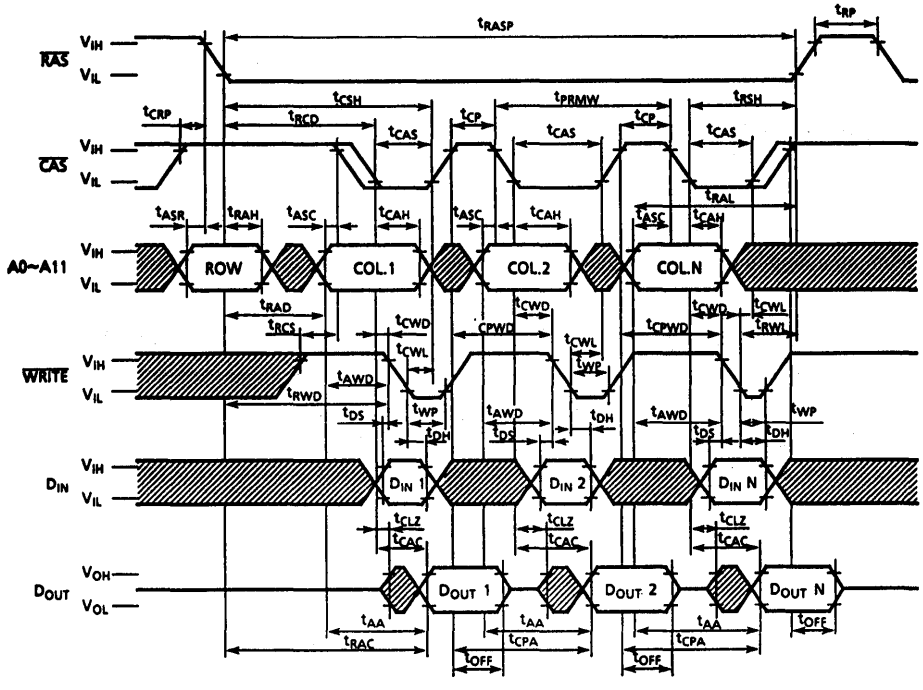
FAST PAGE MODE READ CYCLE



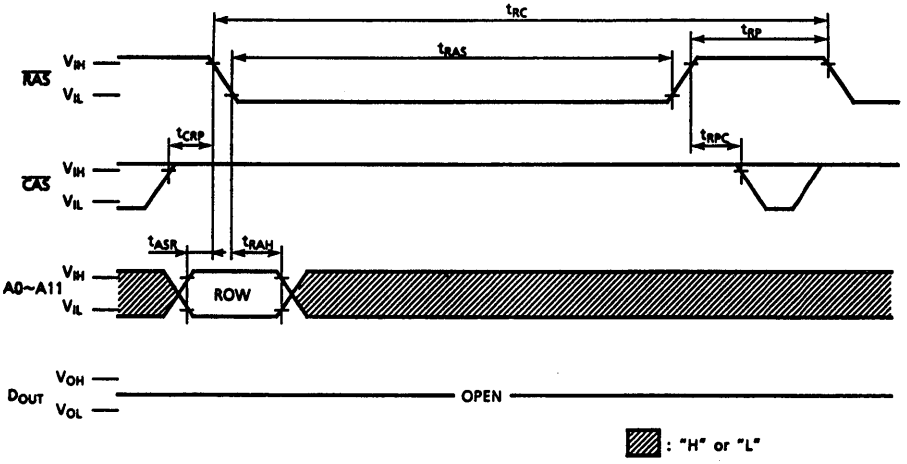
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

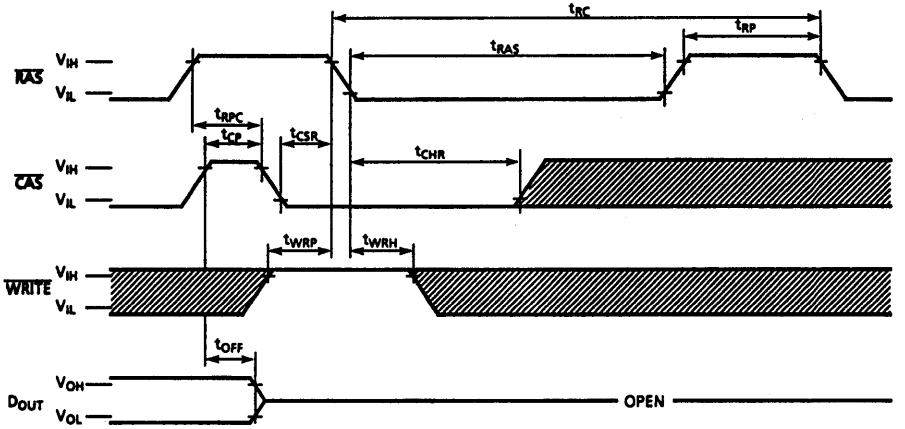


$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$ = "H" or "L"

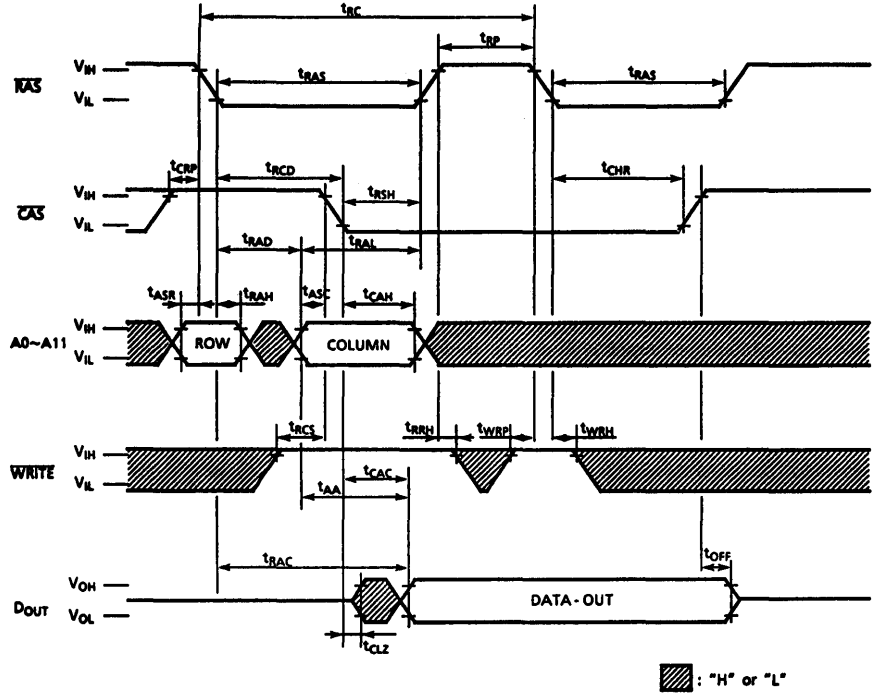
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



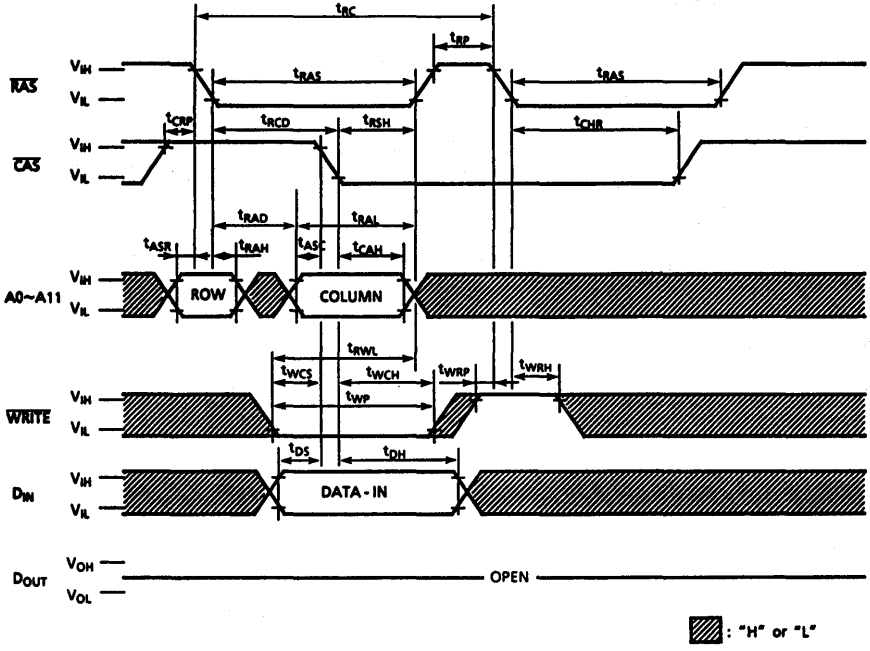
Note: A0~A11 = "H" or "L"

: "H" or "L"

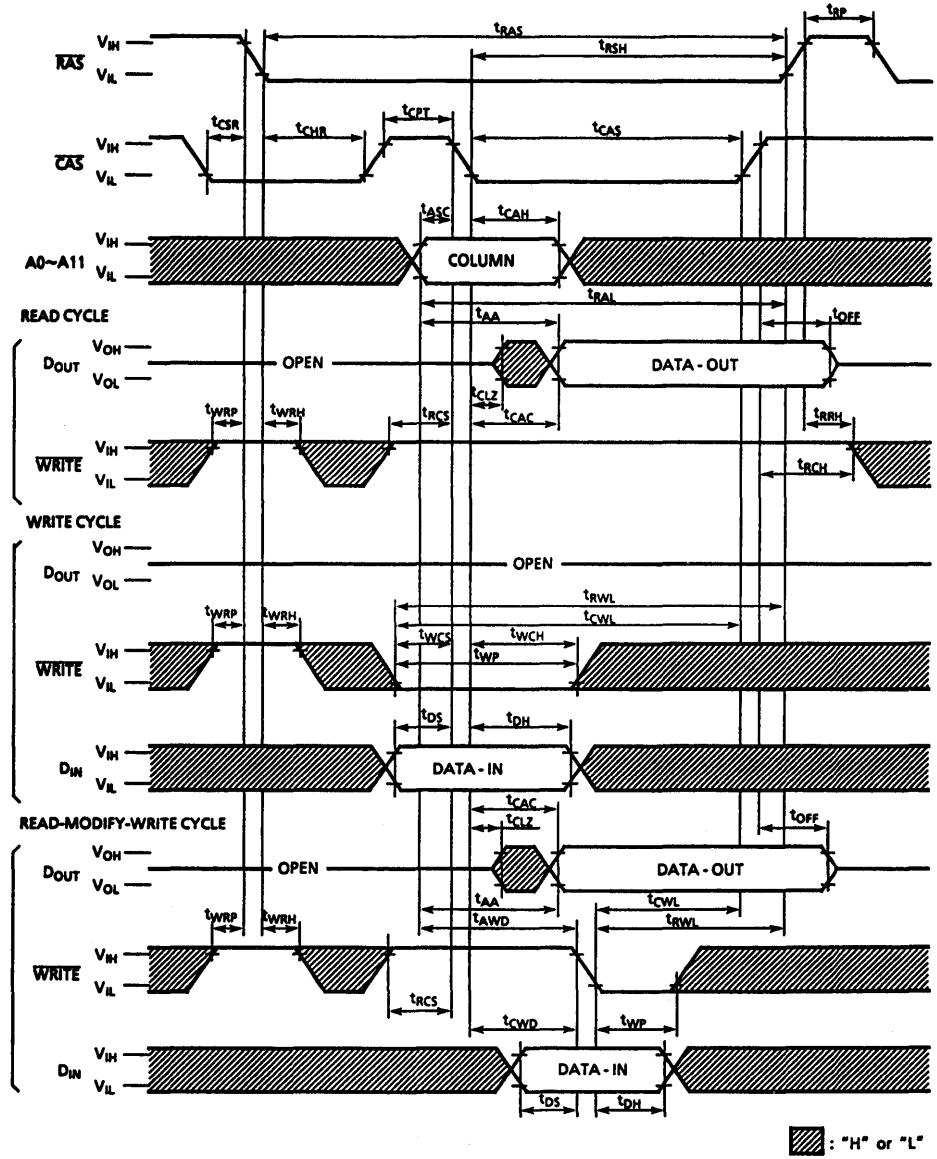
HIDDEN REFRESH CYCLE (READ)



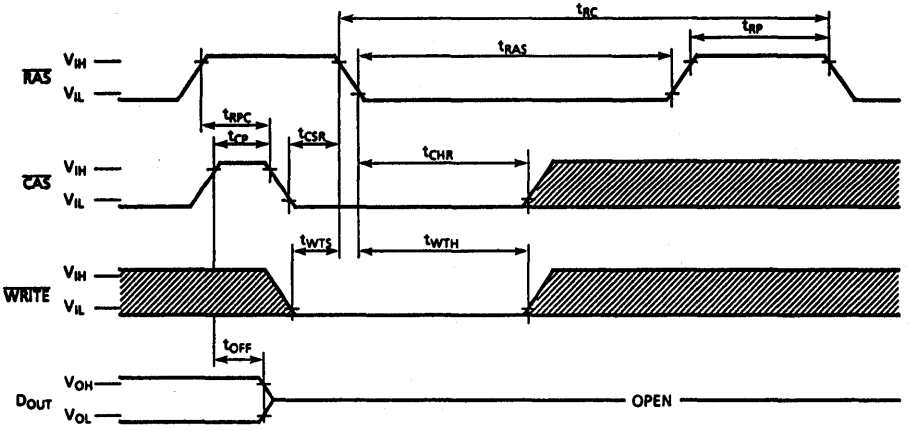
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



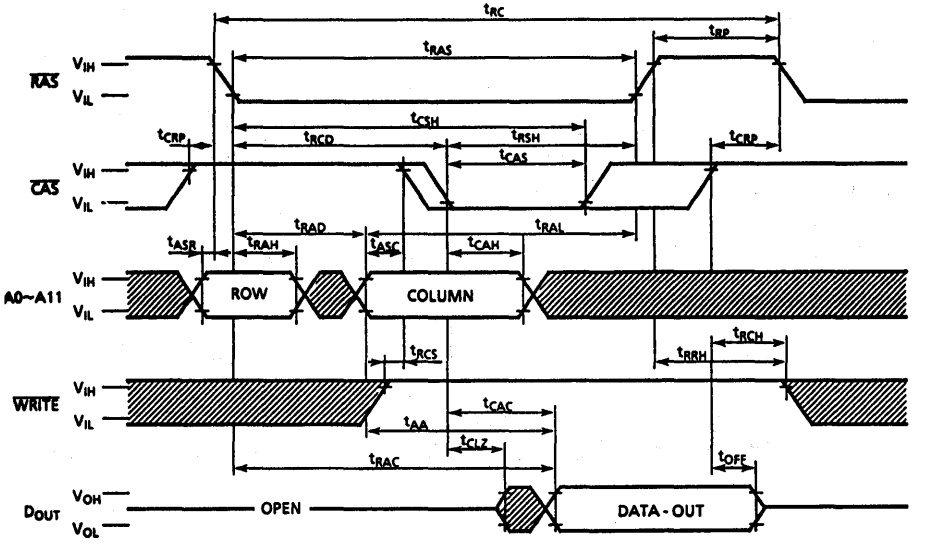
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, A0~A11 = "H" or "L"

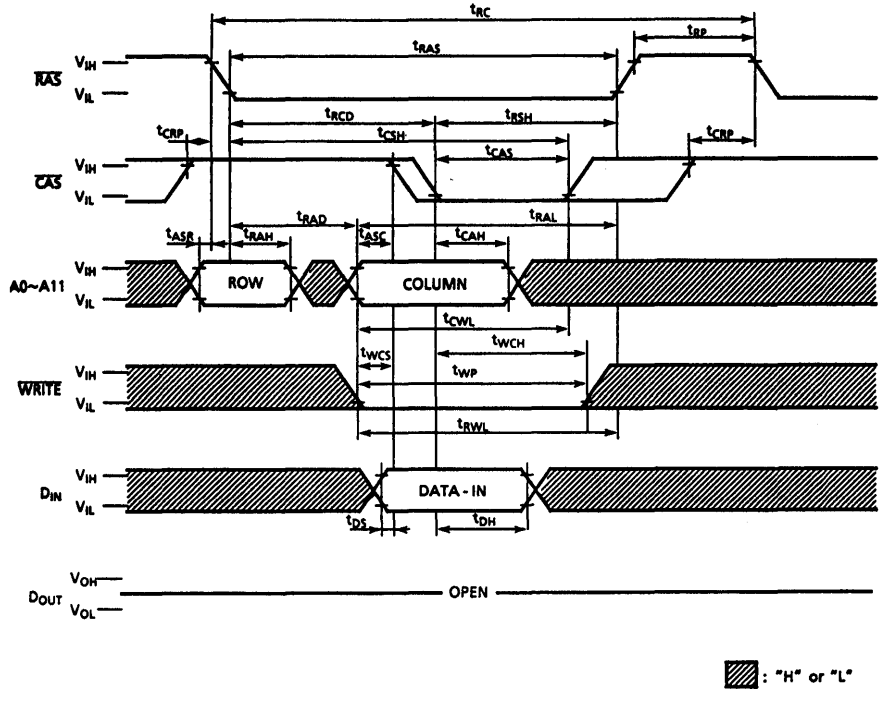
▨: "H" or "L"

READ CYCLE IN THE TEST MODE

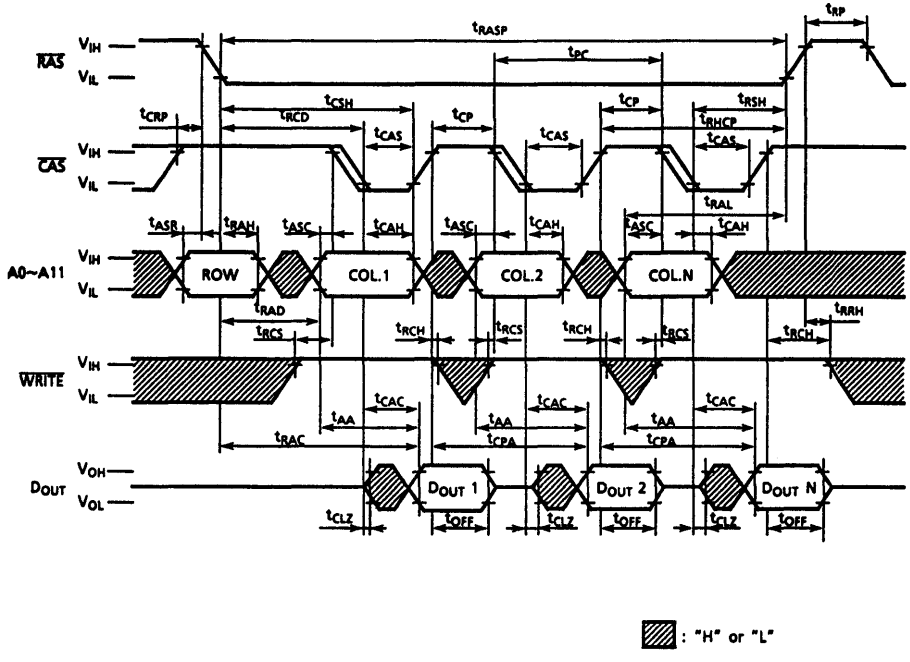


▨: "H" or "L"

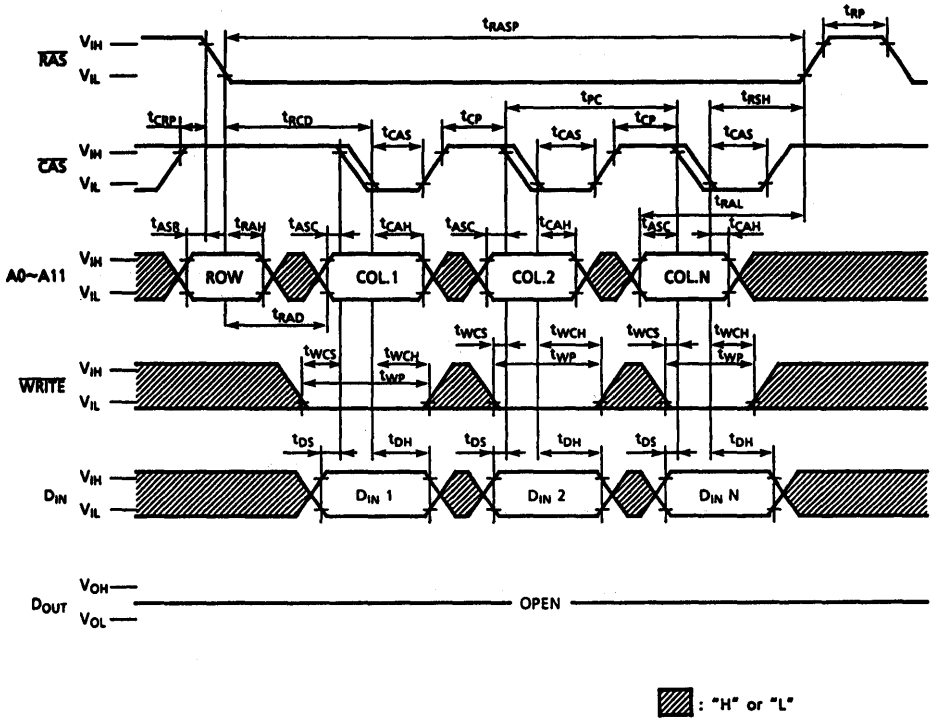
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



FAST PAGE MODE READ CYCLE IN THE TEST MODE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



TEST MODE

The TC5116100J/Z/FT is the RAM organized 16,777,216 words by 1 bits, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. A_{11C}, A_{10C}, A_{1C} and A_{0C} are not used. If any of the bits differed, the data output pin would indicate a "0". Fig. 1 shows the block diagram of TC5116100J/Z/FT. In "Test Mode", the 16M DRAM can be tested as if it were a 1M DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/16 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

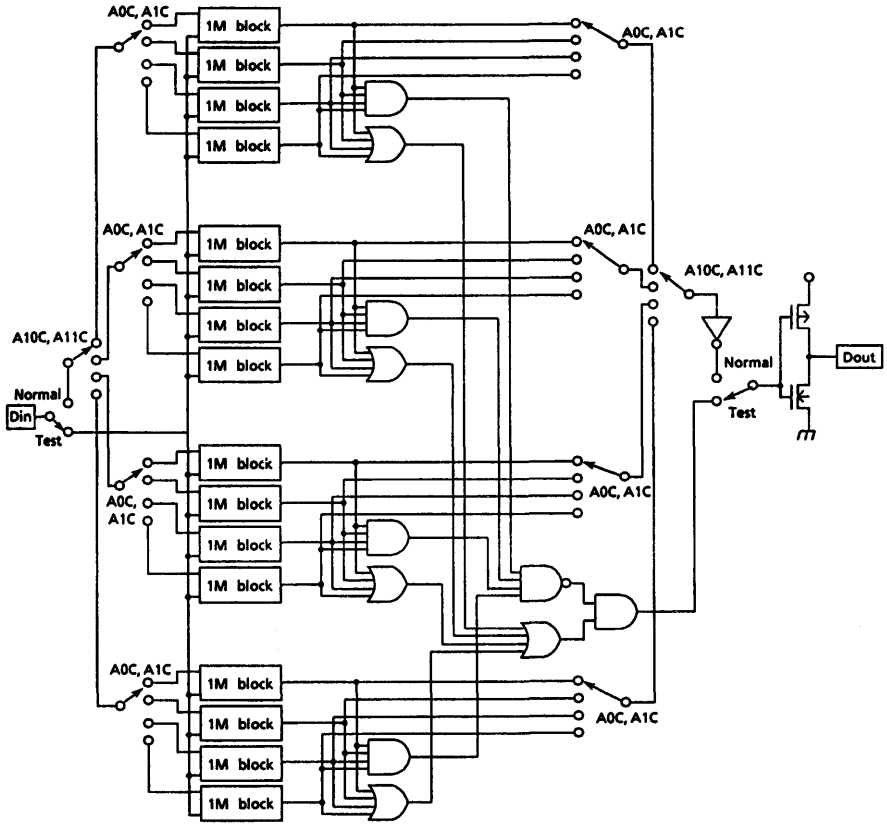


Figure 1

1,048,576 WORD X 4 BIT DYNAMIC RAM

DESCRIPTION

THE TC514400ASJ/AZ/AFT is the new generation dynamic RAM organized 1,048,576 word by 4 bit. The TC514400ASJ/AZ/AFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514400ASJ/AZ/AFT to be packaged in a standard, 26/20 pin plastic SOJ (300), 20 pin plastic ZIP, 26/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  660mW MAX .Operating
  (TC514400ASJ/AZ/AFT-60)
  550mW MAX. Operating
  (TC514400ASJ/AZ/AFT-70)
  468mW MAX. Operating
  (TC514400ASJ/AZ/AFT-80)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC514400ASJ : SOJ26-P-300A
  TC514400AZ : ZIP20-P-400A
  TC514400AFT : TSOP26-P-300

KEY PARAMETERS

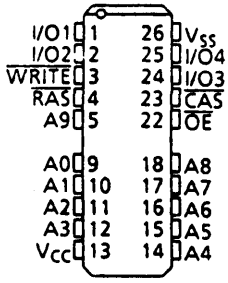
ITEM		TC514400ASJ/AZ/AFT		
		-60	-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC}	Cycle Time	110ns	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAME

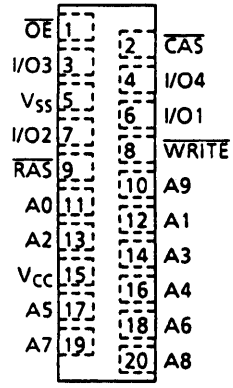
A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

PIN CONNECTION (TOP VIEW)

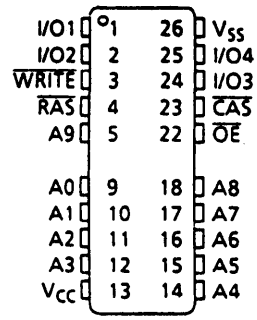
Plastic SOJ



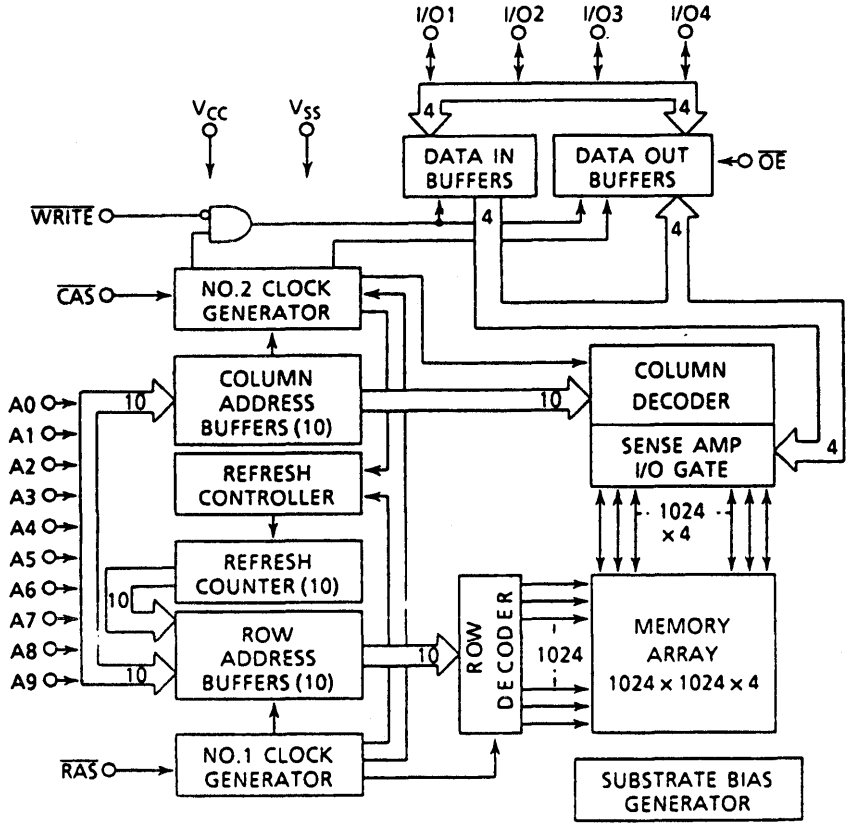
Plastic ZIP



Plastic TSOP (Normal Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514400ASJ/AZ/AFT-60	-	120	mA	3,4 5
		TC514400ASJ/AZ/AFT-70	-	100		
		TC514400ASJ/AZ/AFT-80	-	85		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514400ASJ/AZ/AFT-60	-	120	mA	3,5
		TC514400ASJ/AZ/AFT-70	-	100		
		TC514400ASJ/AZ/AFT-80	-	85		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC514400ASJ/AZ/AFT-60	-	70	mA	3,4 5
		TC514400ASJ/AZ/AFT-70	-	70		
		TC514400ASJ/AZ/AFT-80	-	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC514400ASJ/AZ/AFT-60	-	120	mA	
		TC514400ASJ/AZ/AFT-70	-	100		
		TC514400ASJ/AZ/AFT-80	-	85		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≤V_{IN}≤6.5V, All Other Pins Not Under Test=OV)		-10	10	μA	3,5
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (OV≤V_{OUT}≤5.5V),		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)			0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC514400ASJ/AZ/AFT						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	165	-	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	0	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514400ASJ/AZ/AFT						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	16	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	50	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	90	-	100	-	110	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	-	65	-	70	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	70	-	75	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	-	40	-	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	20	-	20	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	0	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC514400ASJ/AZ/AFT						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	155	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	50	-	55	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	-	85	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	25	ns	9, 14
t_{AA}	Access Time from Column Address	-	35	-	40	-	45	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	45	-	50	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	85	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	85	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	85	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold	45	-	45	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead	35	-	40	-	45	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input Capacitance (I/O1~I/O4)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

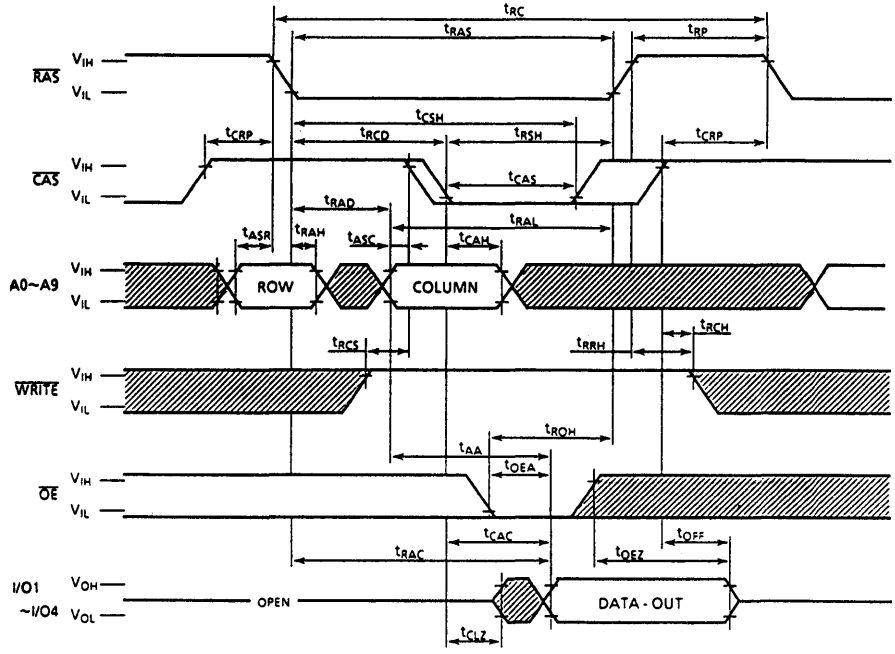
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the date sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

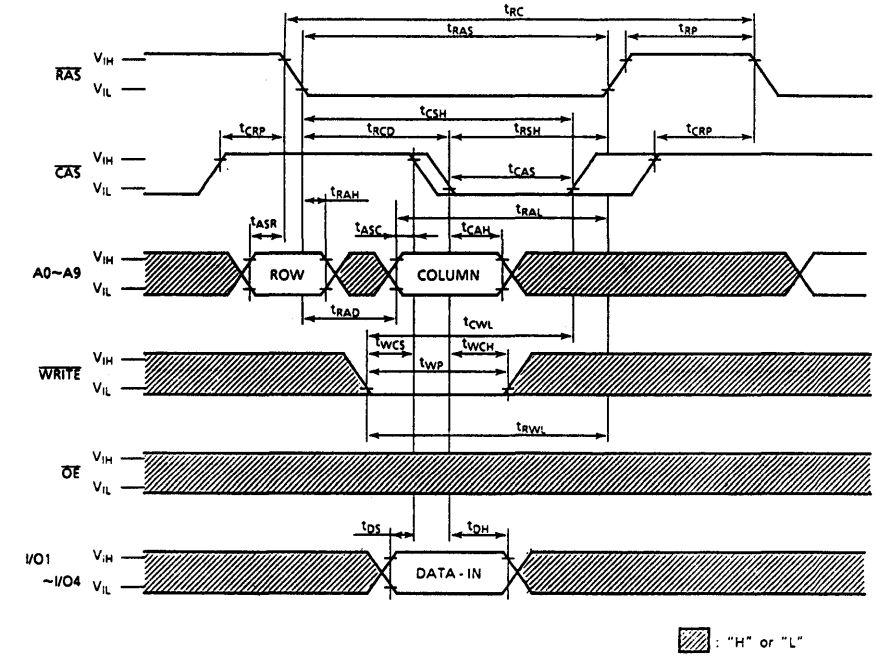
READ CYCLE



Note: D_{IN} = OPEN

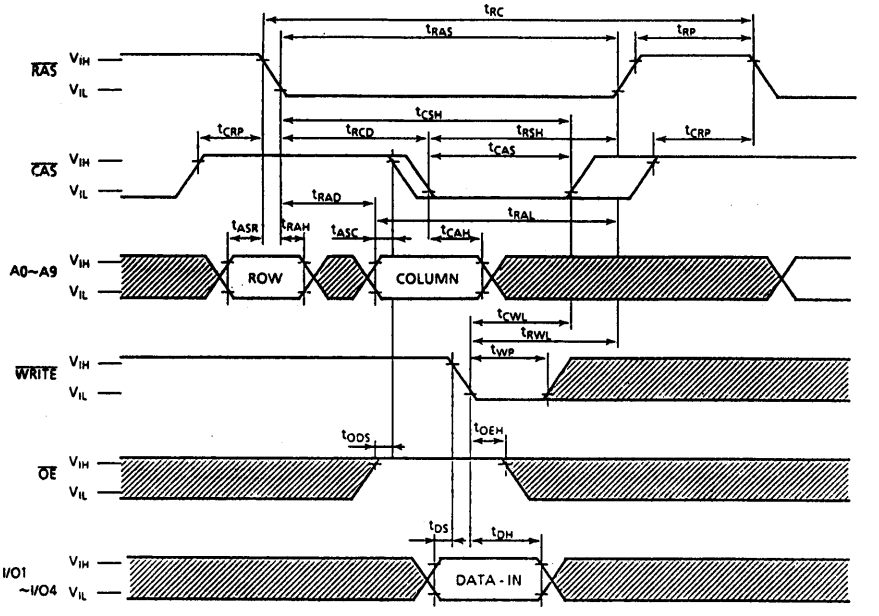
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE)



▨ : "H" or "L"

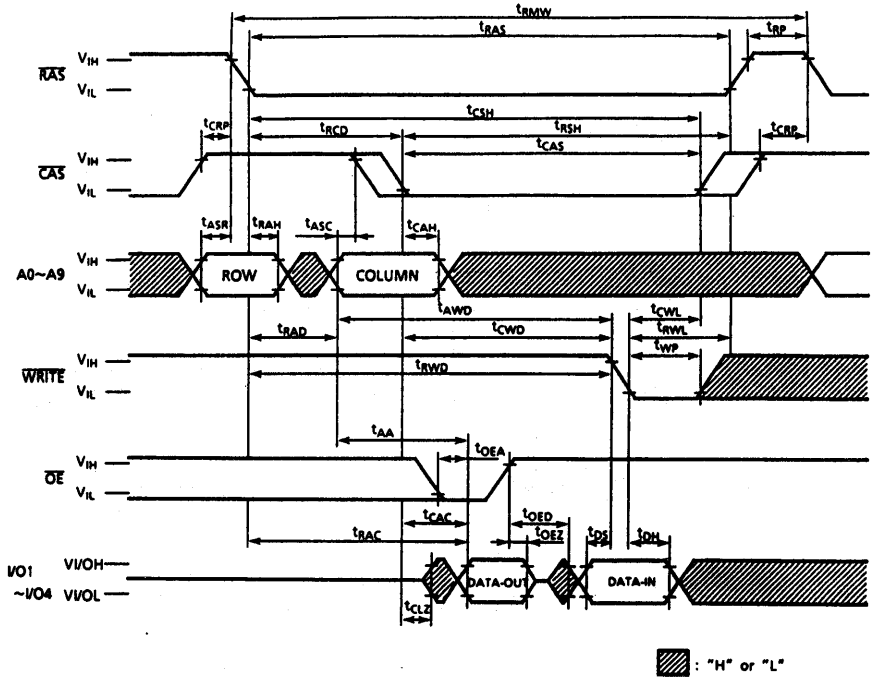
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

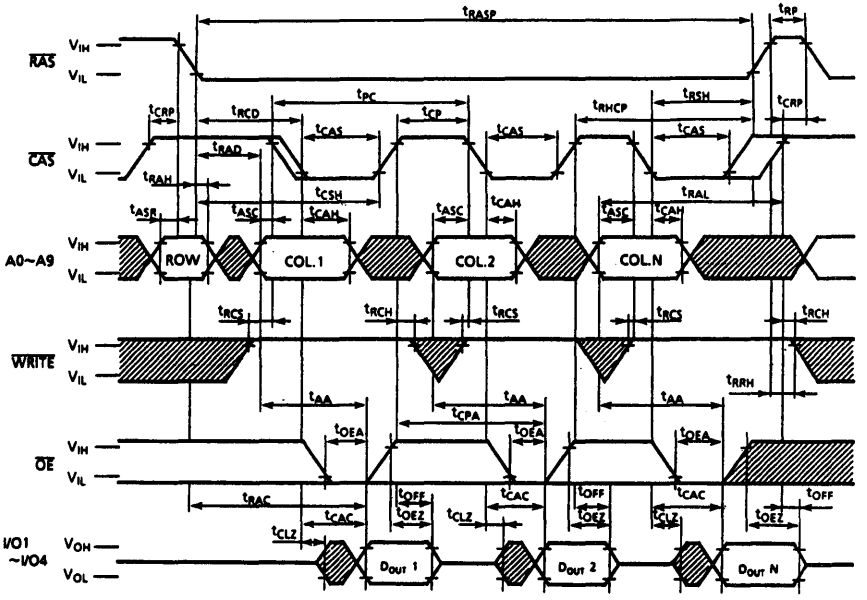
▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



▨ : "H" or "L"

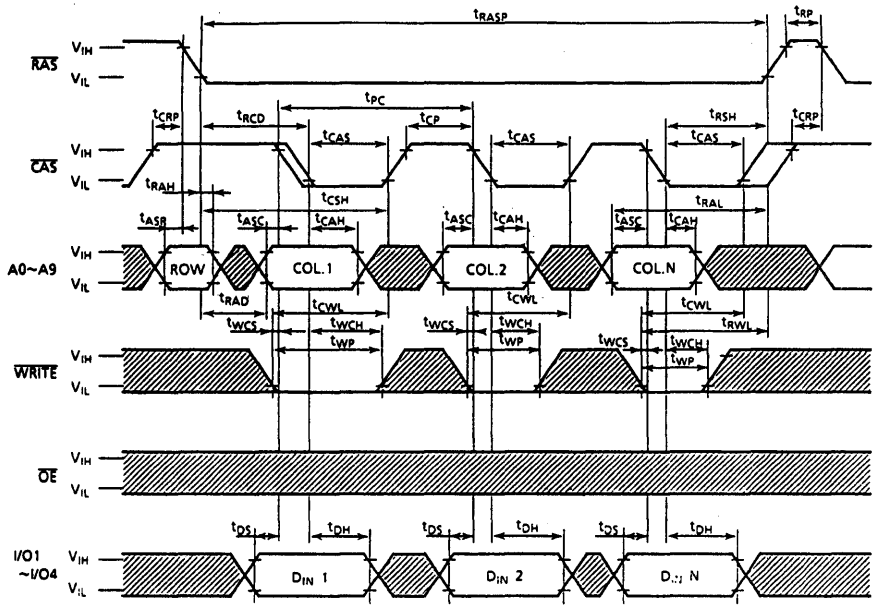
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

: "H" or "L"

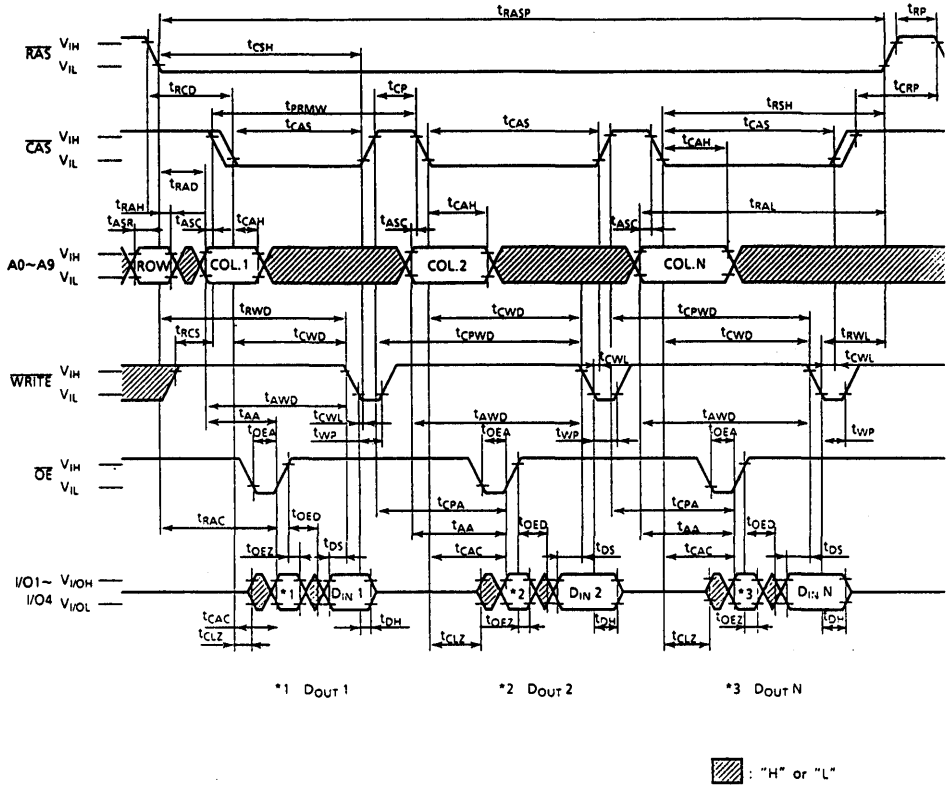
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



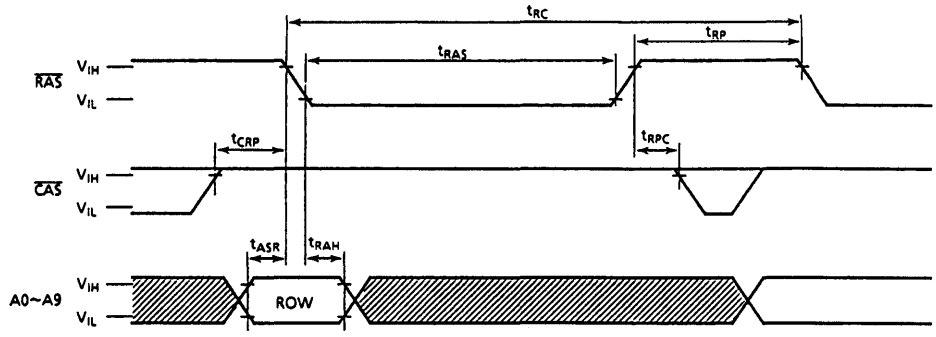
Note: D_{OUT} = OPEN

: "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



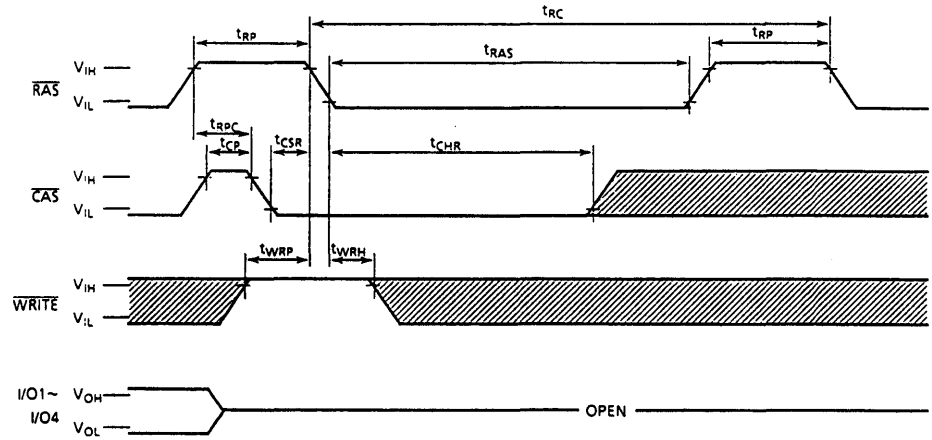
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

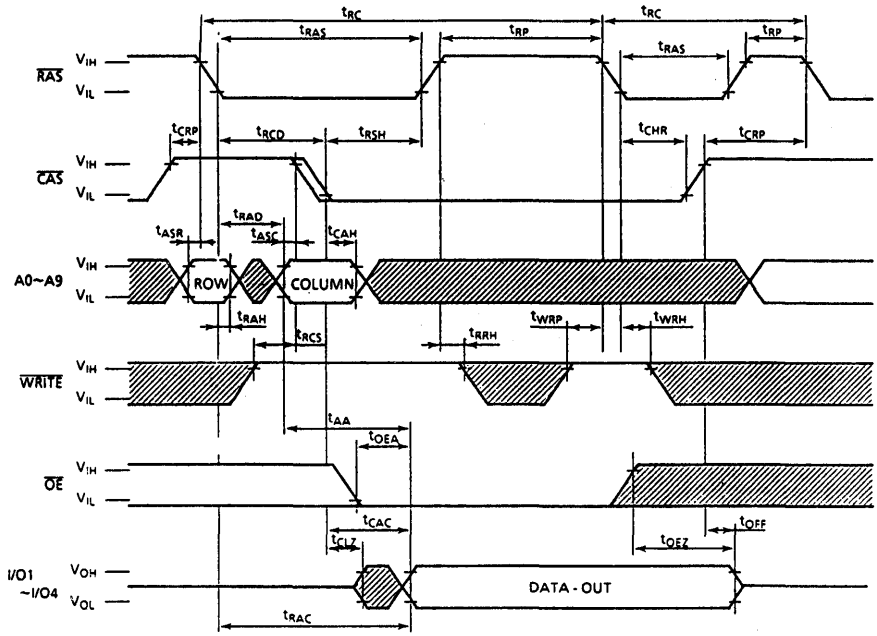
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

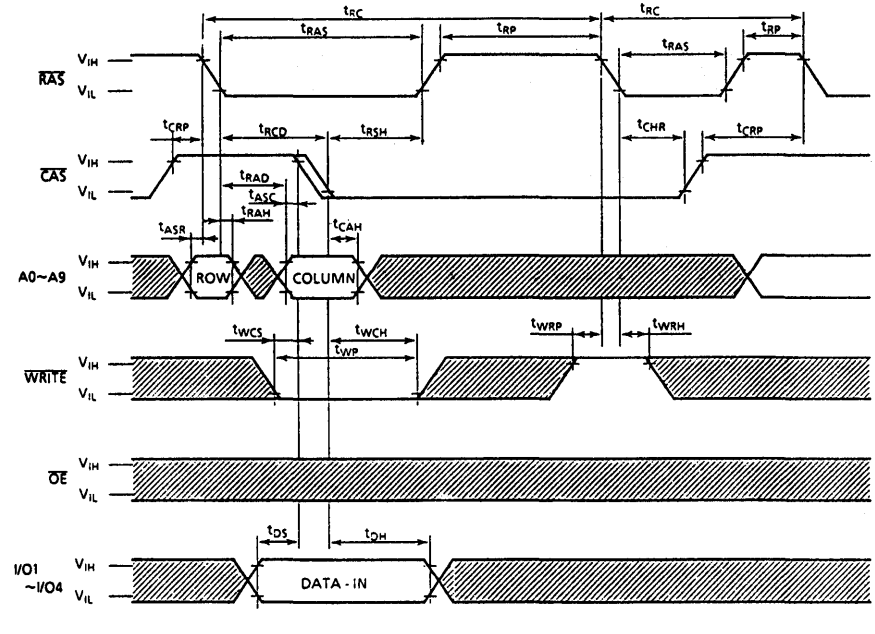
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨ : "H" or "L"

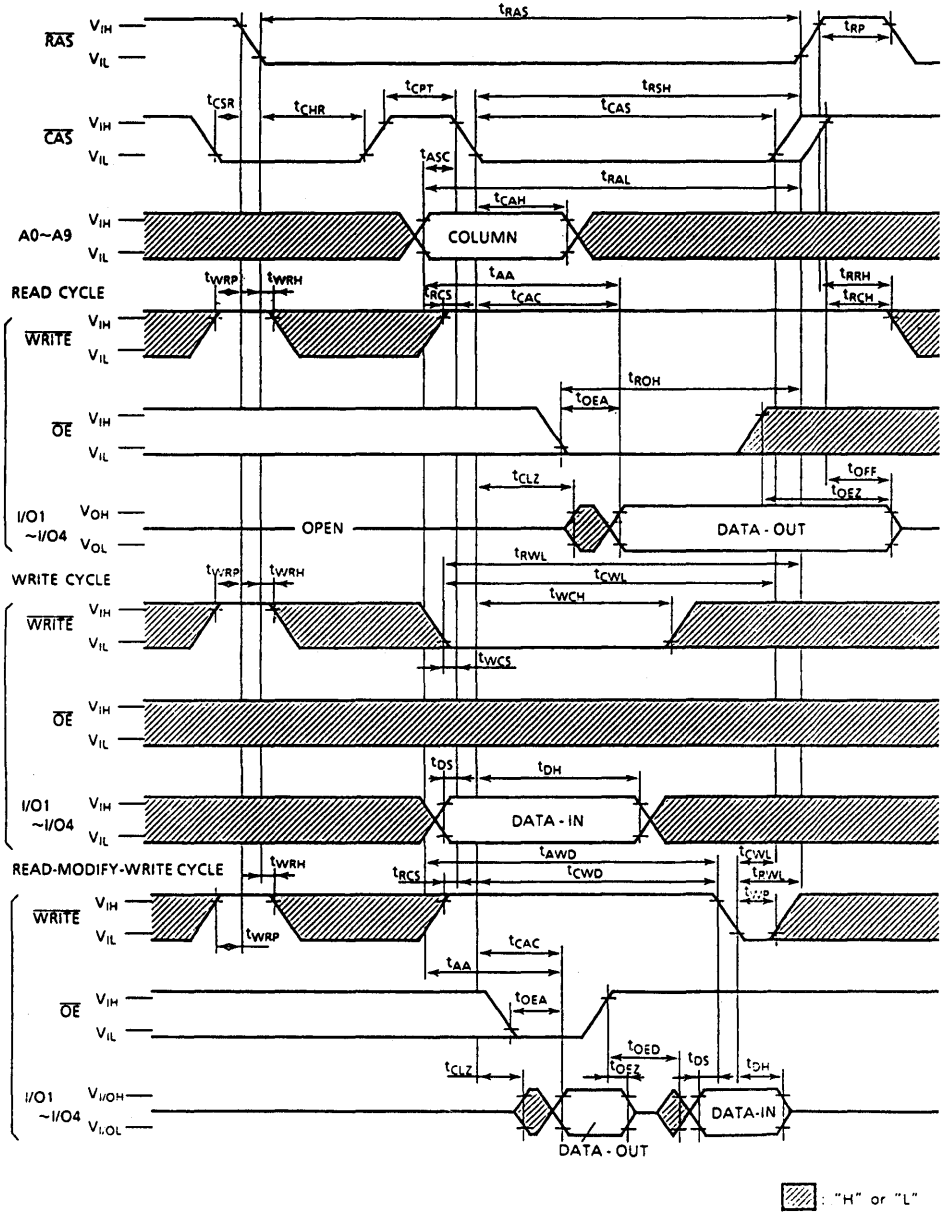
HIDDEN REFRESH CYCLE (WRITE)



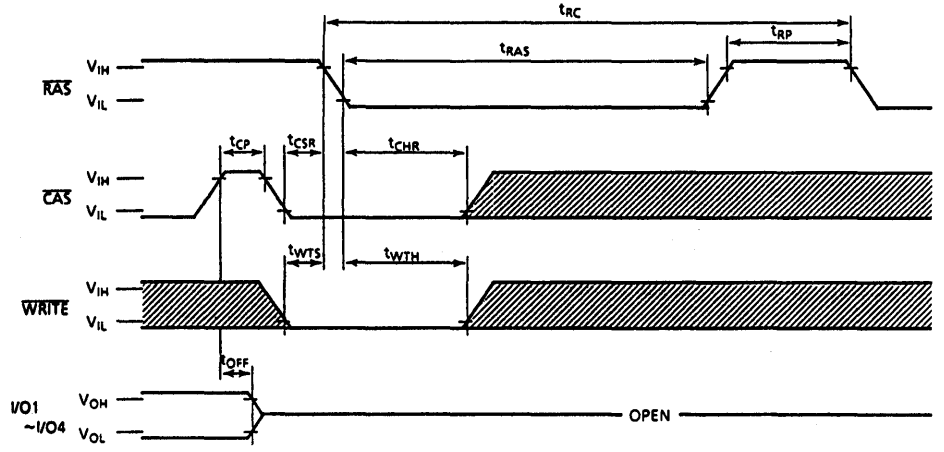
Note: D_{OUT} = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



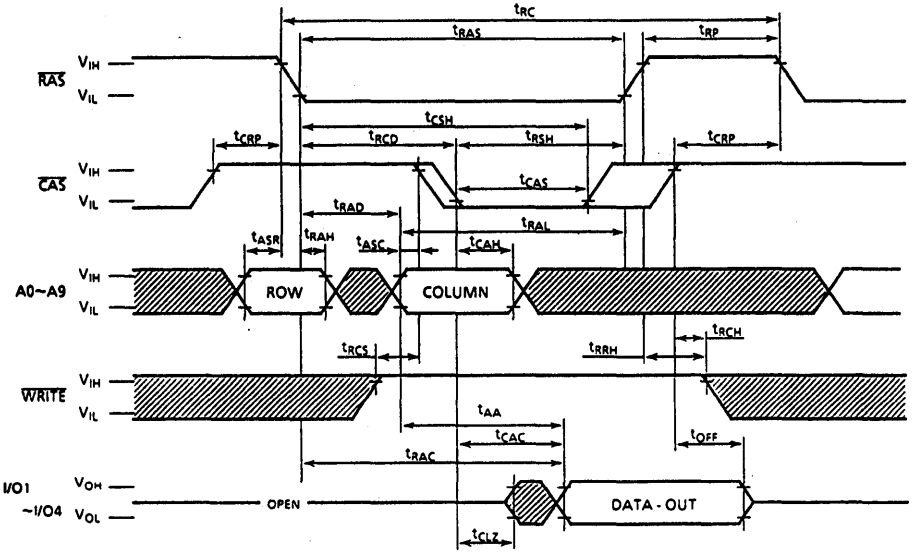
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨: "H" or "L"

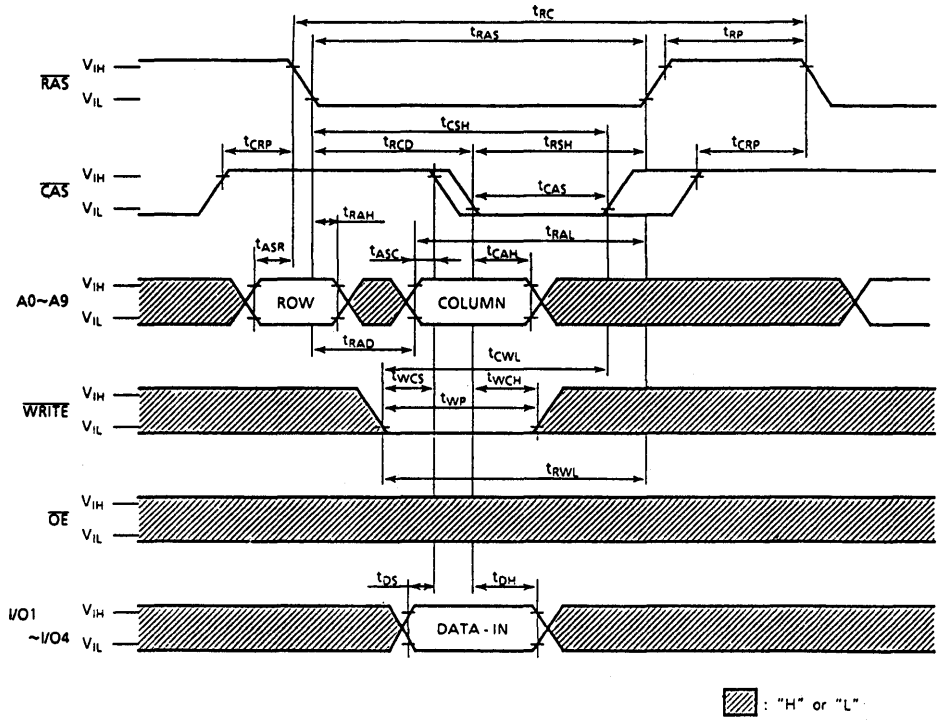
READ CYCLE IN THE TEST MODE



Note: $\overline{OE}$ = "L" D_{IN} = OPEN

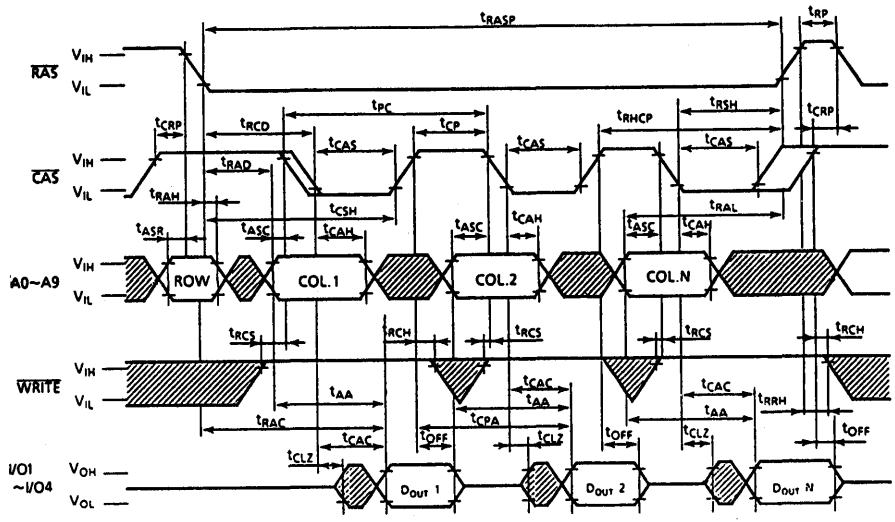
▨: "H" or "L"

WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note: D_{OUT} = OPEN

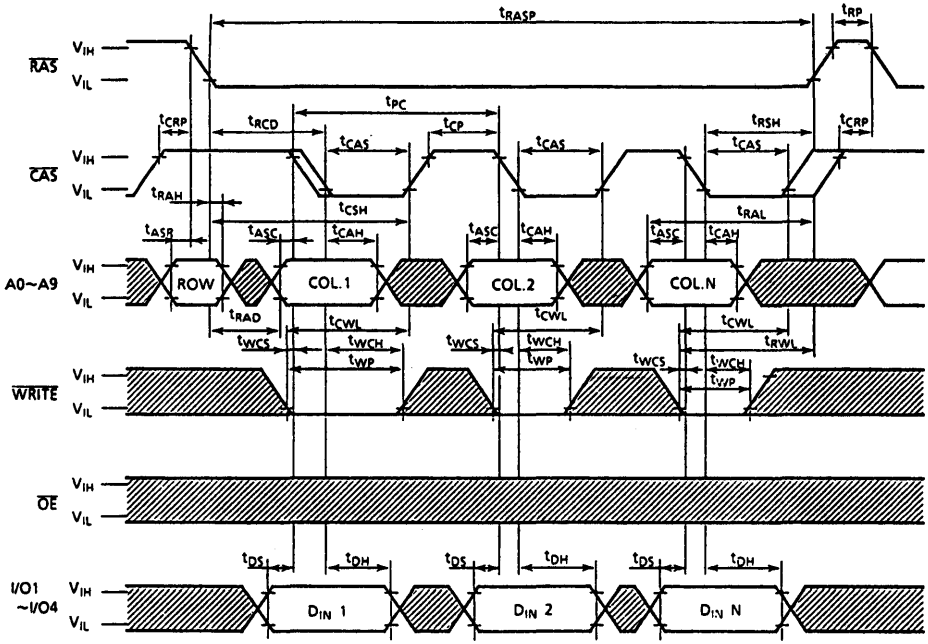
FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note: $\overline{OE}$ = "L" D_{IN} = OPEN

▨ : "H" or "L"

FAST PAGE MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note: D_{OUT} = OPEN

▨ : "H" or "L"

TEST MODE

The TC514400/ASJ/AZ/AFT is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A0c is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1".

If they were not equal the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514400/ASJ/AZ/AFT. In "Test Mode", the 1MX4 DRAM can be tested as if it were a 512KX4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

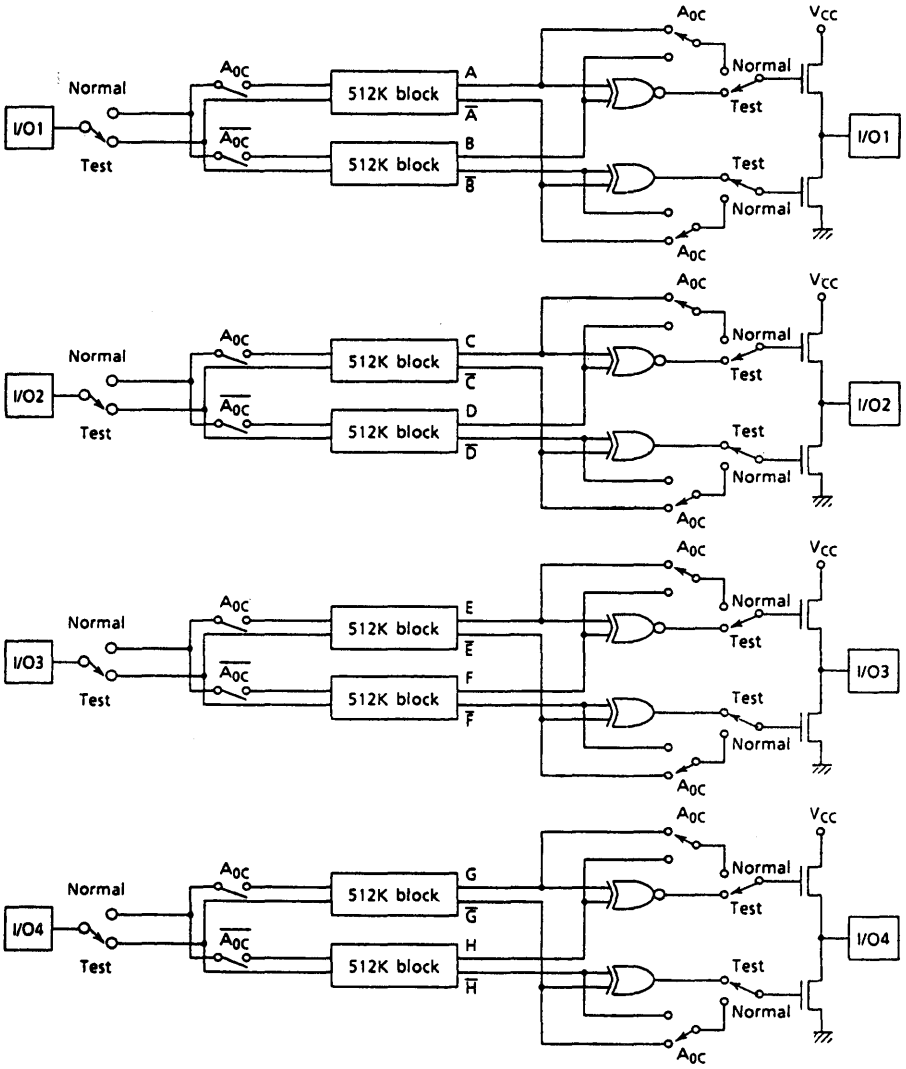


Figure 1

1,048,576 WORD X 4 BIT DYNAMIC RAM

DESCRIPTION

The TC514400ASJL/AFTL/ATRL is the new generation dynamic RAM organized 1,048,576 word by 4 bit. The TC514400ASJL/AFTL/ATRL utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514400ASJL/AFTL/ATRL to be packaged in a standard 26/20 pin plastic SOJ (300), 26/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  660mW MAX .Operating
  (TC514400ASJL/AFTL/ATRL-60)
  550mW MAX. Operating
  (TC514400ASJL/AFTL/ATRL-70)
  468mW MAX. Operating
  (TC514400ASJL/AFTL/ATRL-80)
  1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514400ASJL : SOJ26-P-300A
  TC514400AFTL : TSOP26-P-300
  TC514400ATRL : TSOP26-P-300A

KEY PARAMETERS

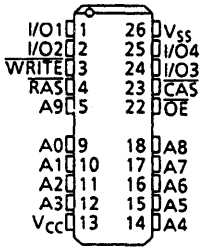
ITEM		TC514400ASJ/AZ/AFT		
		-60	-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC}	Cycle Time	110ns	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAME

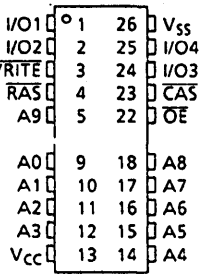
A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

PIN CONNECTION (TOP VIEW)

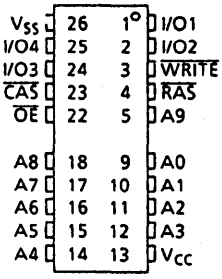
Plastic SOJ



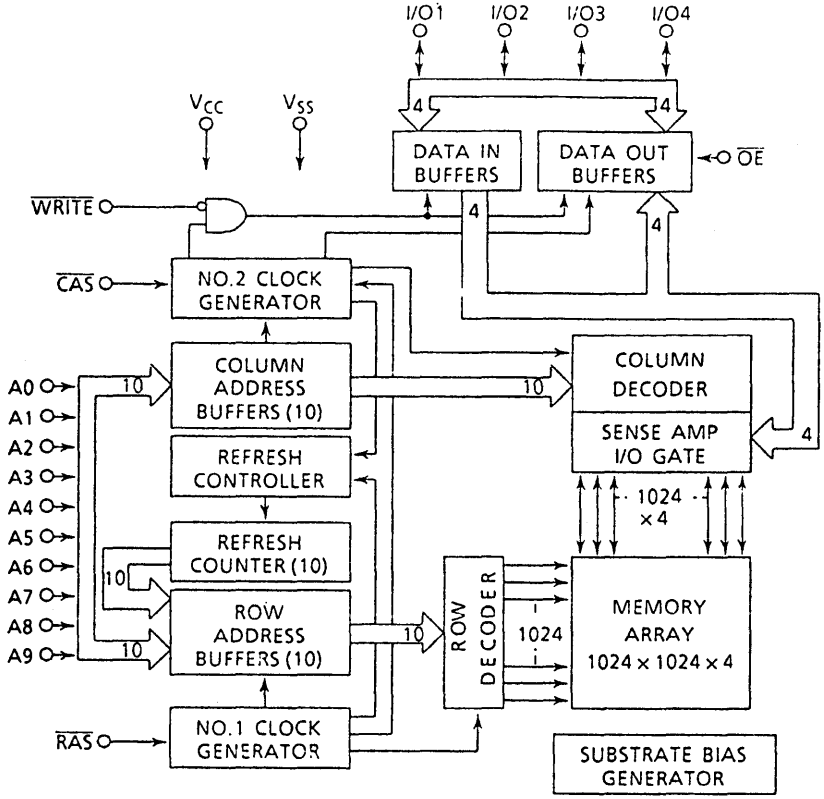
Plastic TSOP (Normal Bend Type)



Plastic TSOP (Reverse Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514400ASJL/AFTL/ATRL-60	-	120	mA	3,4 5
		TC514400ASJL/AFTL/ATRL-70	-	100		
		TC514400ASJL/AFTL/ATRL-80	-	85		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514400ASJL/AFTL/ATRL-60	-	120	mA	3, 5
		TC514400ASJL/AFTL/ATRL-70	-	100		
		TC514400ASJL/AFTL/ATRL-80	-	85		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL},$\overline{CAS}$, Address Cycling:t_{PC}=t_{PC} MIN.)	TC514400ASJL/AFTL/ATRL-60	-	70	mA	3,4 5
		TC514400ASJL/AFTL/ATRL-70	-	70		
		TC514400ASJL/AFTL/ATRL-80	-	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	200	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC514400ASJL/AFTL/ATRL-60	-	120	mA	3, 5
		TC514400ASJL/AFTL/ATRL-70	-	100		
		TC514400ASJL/AFTL/ATRL-80	-	85		
I_{CC7}	Battery Back Up Current Average Power Suuply Current, Battery Back Up Mode ($\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$=V_{CC}-0.02V, $\overline{WRITE}$= V_{CC}-0.2V,A0~9=V_{CC}-0.2V or 0.2V, I/O1~4=Vcc-0.2V, 0.2V or OPEN:t_{RC}=125μs, t_{RAS}=t_{RAS} MIN. ~1μs)		-	300	μA	3.6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled,0 ≤V_{OUT}≤5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEAKAGE CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEAKAGE CURRENT Output "L" Level Voltage (IOUT=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 7,8,9)

SYMBOL	PARAMETER	TC514400ASJL/AFTL/ATRL						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	165	-	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	10,15, 16
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	20	ns	10,15
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	40	-	45	-	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	0	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	12
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514400ASJL/AFTL/ATRL						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	13
t_{DH}	Data Hold Time	15	-	15	-	15	-	ns	13
t_{REF}	Refresh Period	-	128	-	128	-	128	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	50	-	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	90	-	100	-	110	-	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	-	65	-	70	-	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	70	-	75	-	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	30	-	40	-	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	20	-	20	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	11
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	0	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	10		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC514400ASJL/AFTL/ATRL						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	155	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	50	-	55	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	-	85	ns	10,15, 16
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	25	ns	10,15
t_{AA}	Access Time from Column Address	-	35	-	40	-	45	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	45	-	50	ns	10
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	85	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	85	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	85	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold	45	-	45	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead	35	-	40	-	45	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input Capacitance (I/O1~I/O4)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. t_{RAS} (max.)=1μs is only applied to refresh of battery-back up. t_{RAS} (max.)=10μs is applied to functional operating.

7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

8. AC measurements assume t_T=5ns.

9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

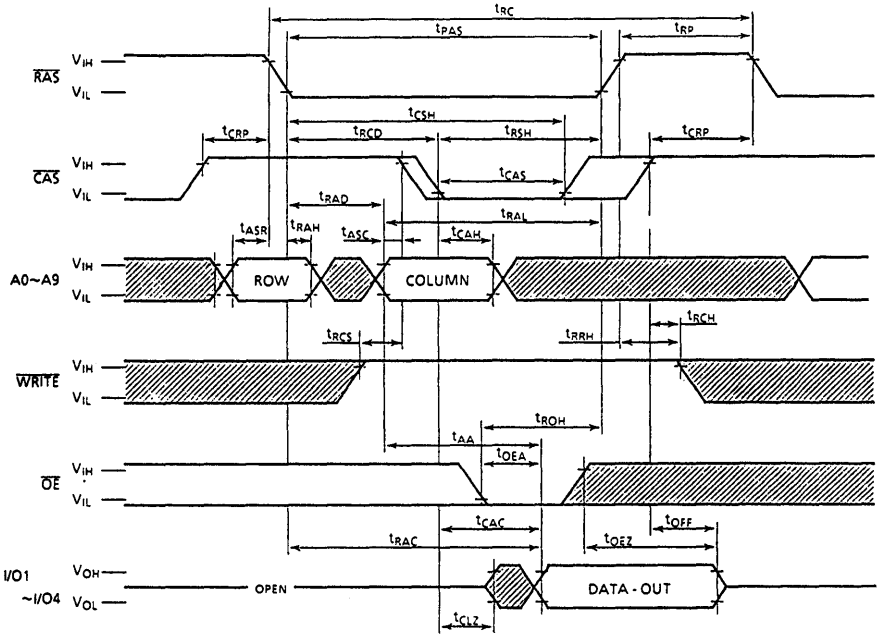
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWD} > t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCS} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

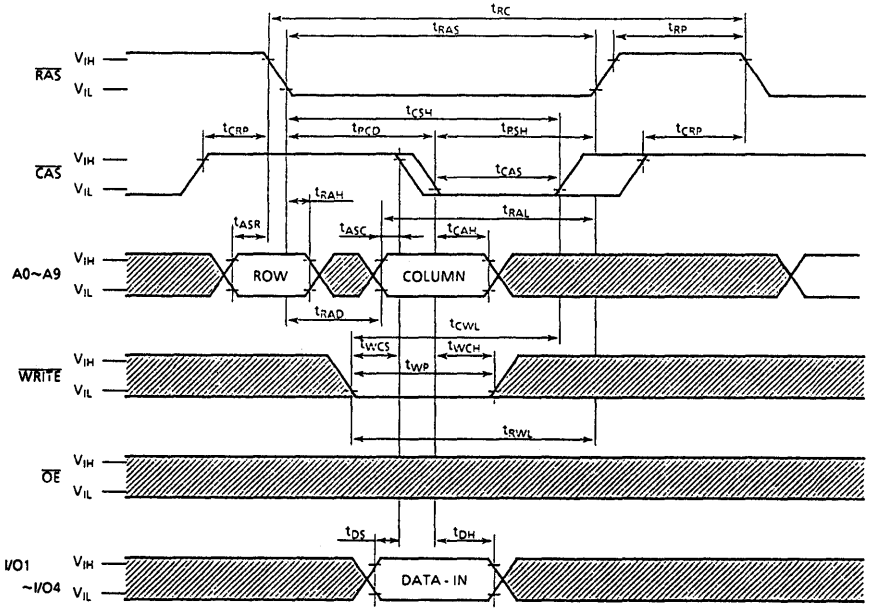
READ CYCLE



Note: D_{IN} = OPEN

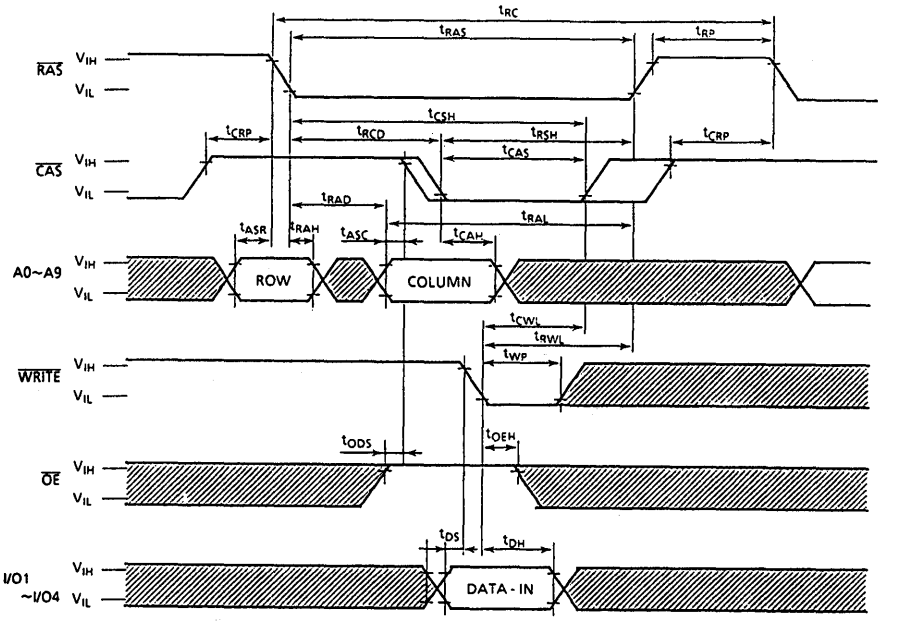
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE)



▨ : "H" or "L"

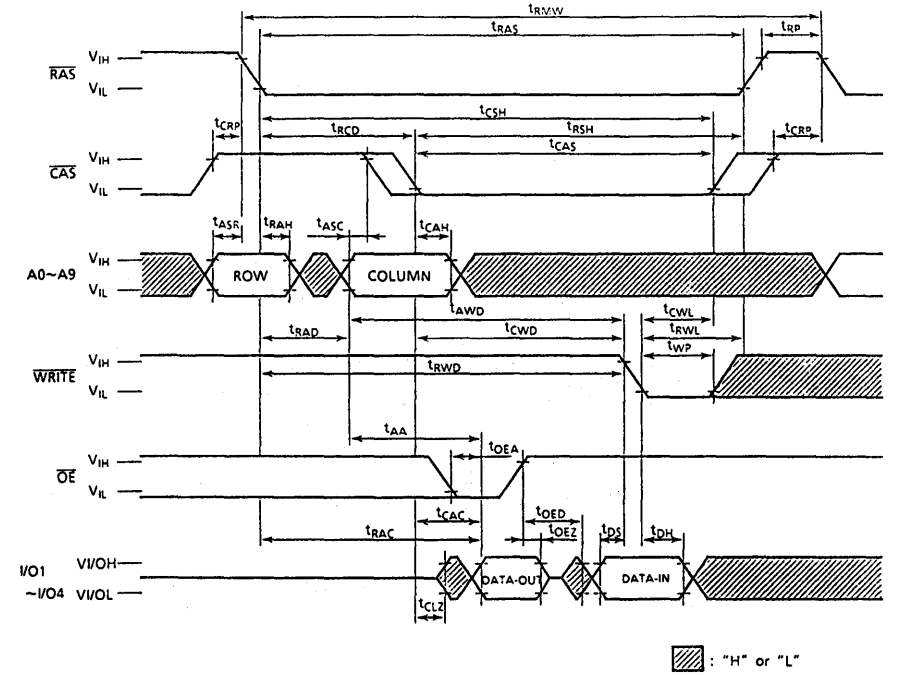
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

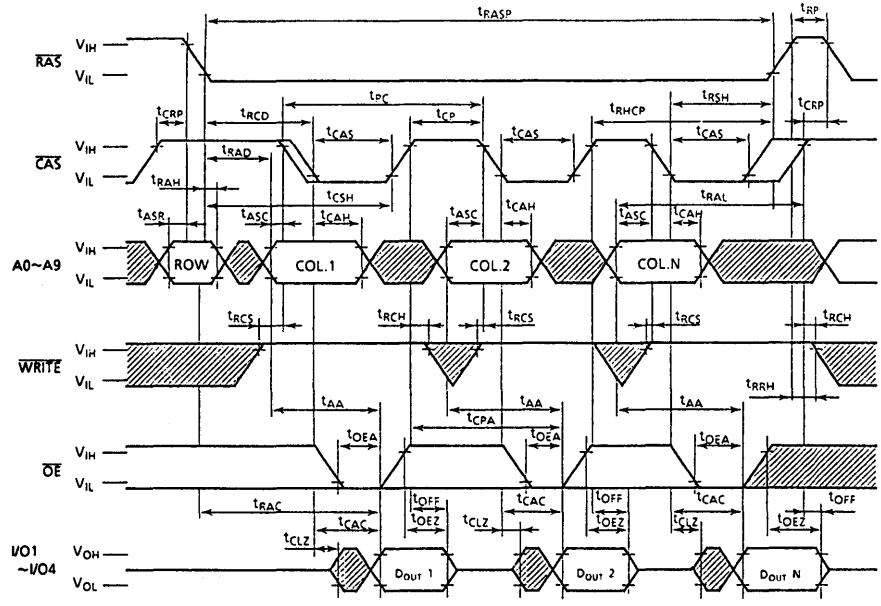
▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



▨ : "H" or "L"

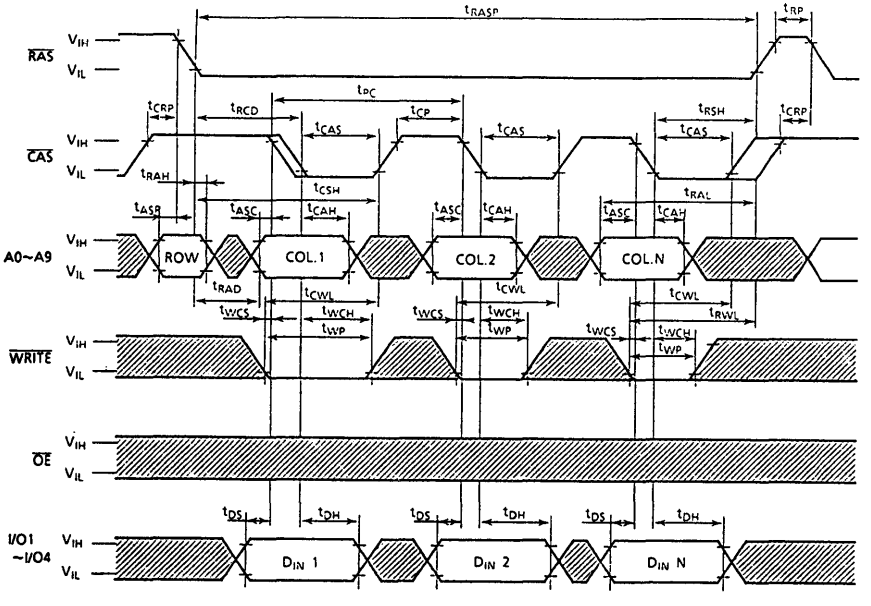
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨: "H" or "L"

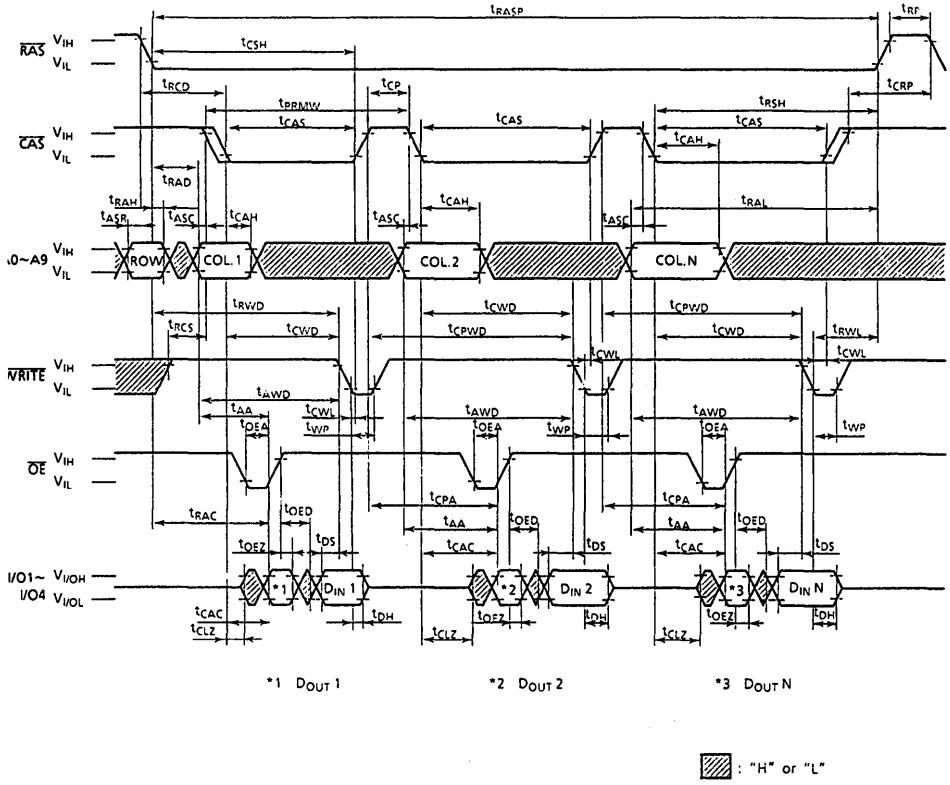
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



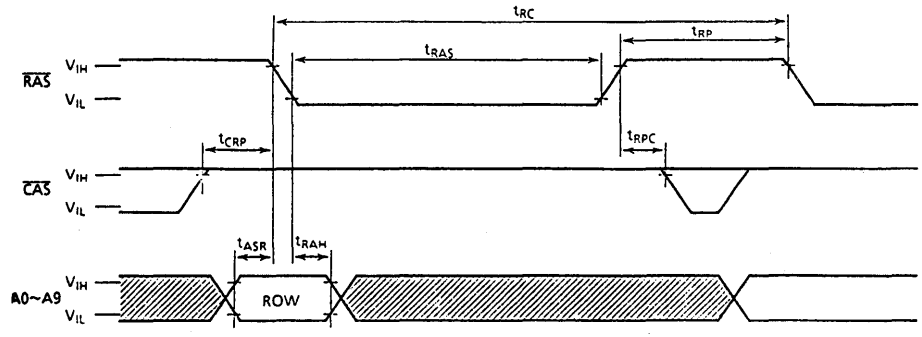
Note: D_{OUT} = OPEN

▨: "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



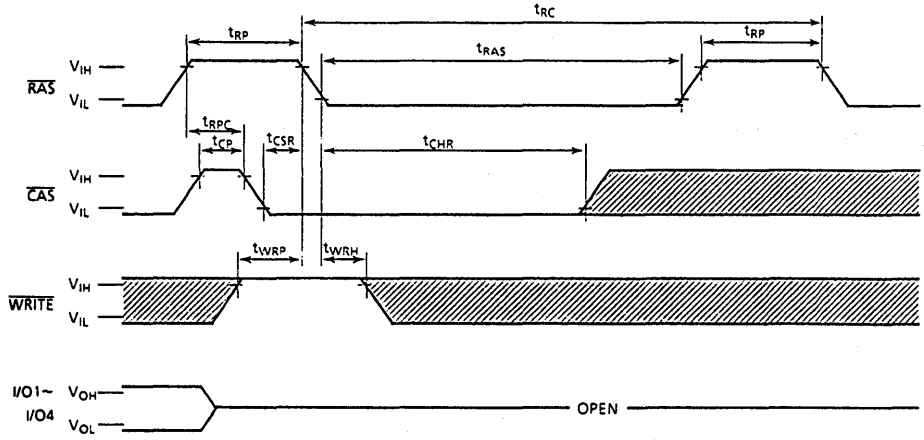
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

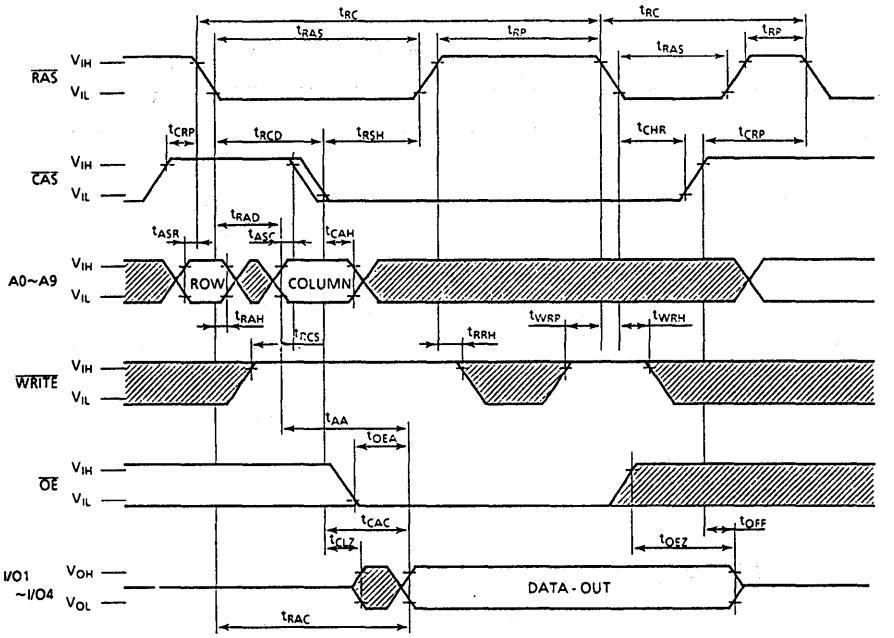
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

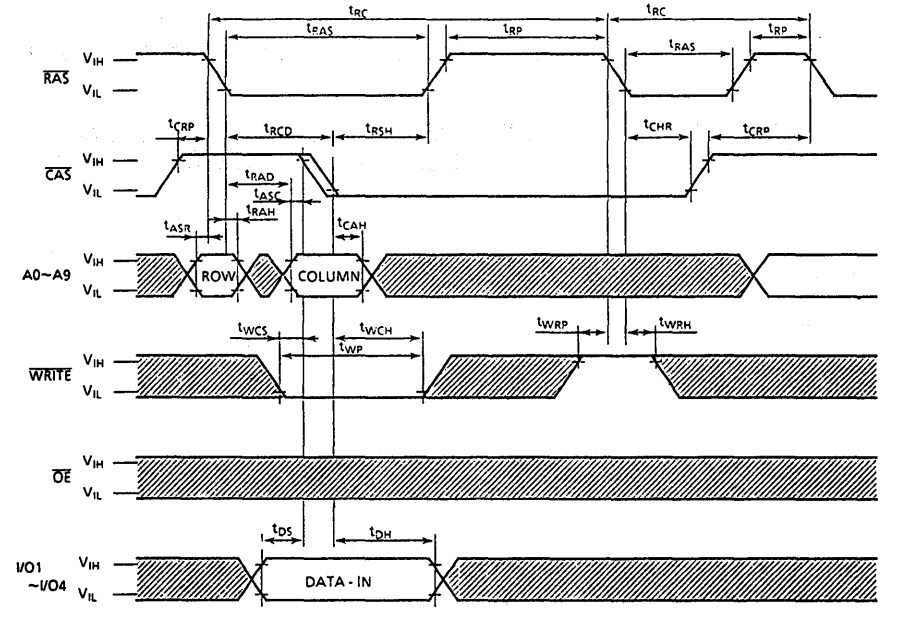
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨: "H" or "L"

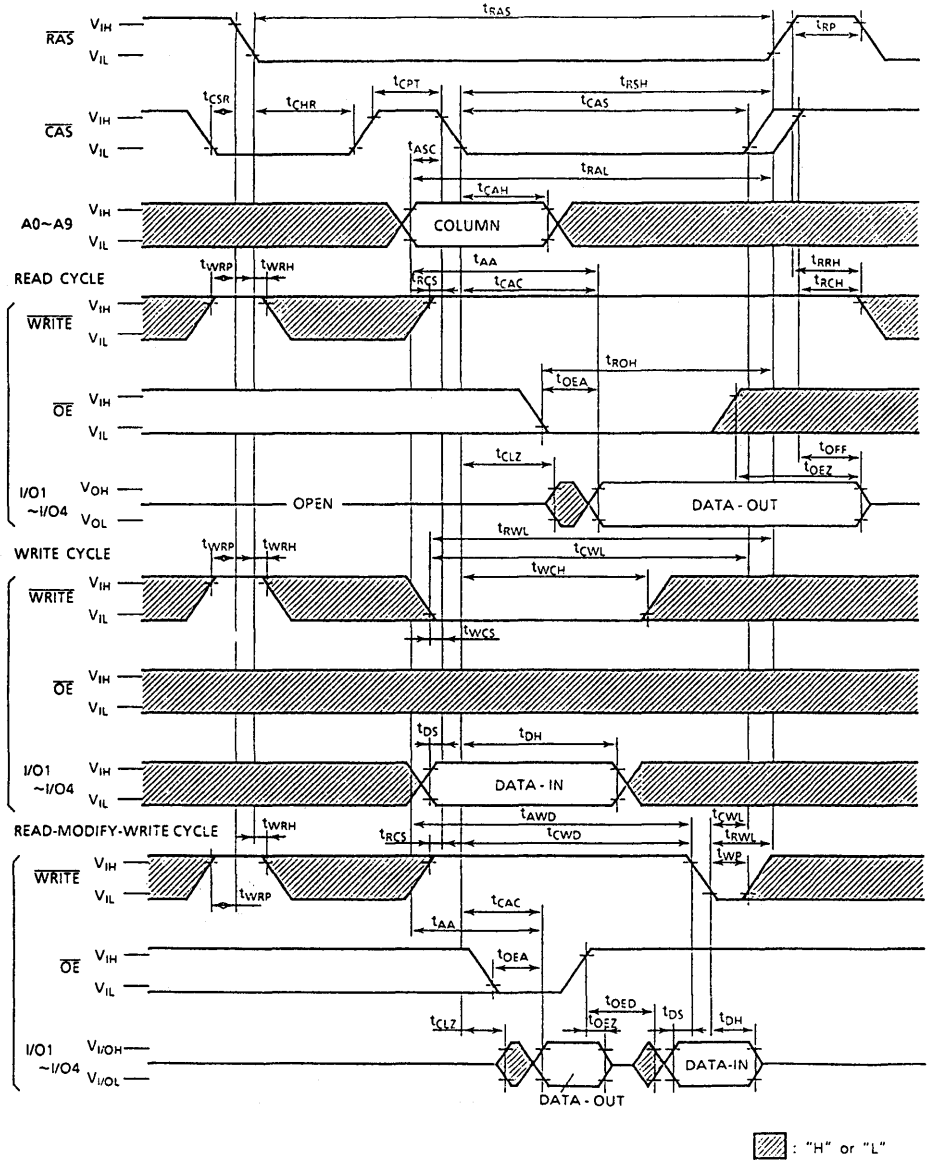
HIDDEN REFRESH CYCLE (WRITE)



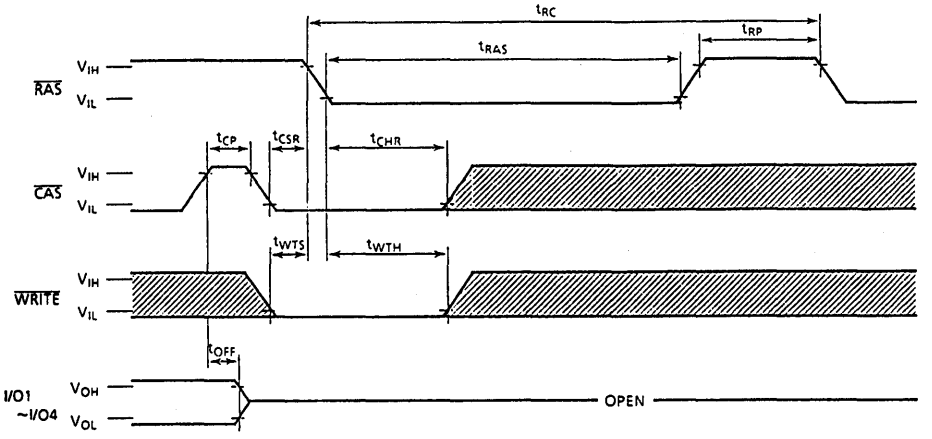
Note: D_{OUT} = OPEN

▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



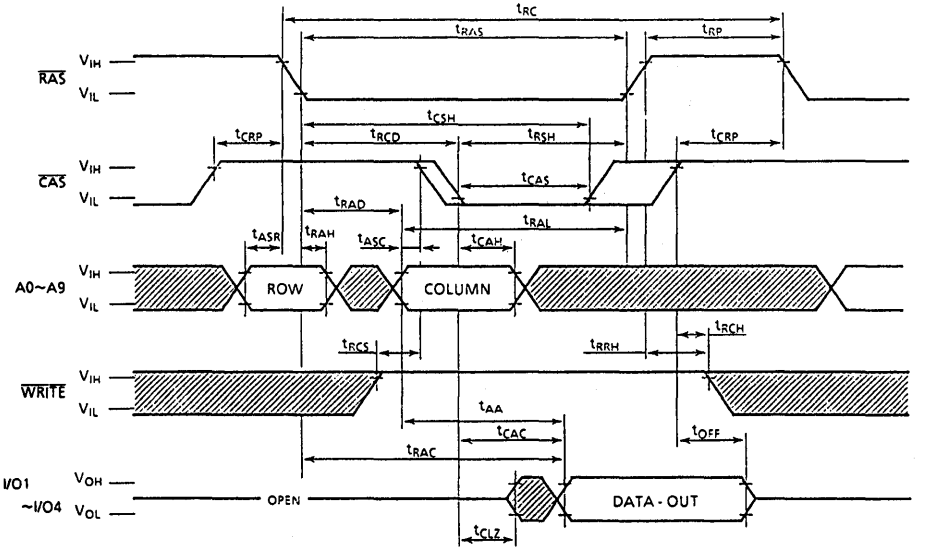
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

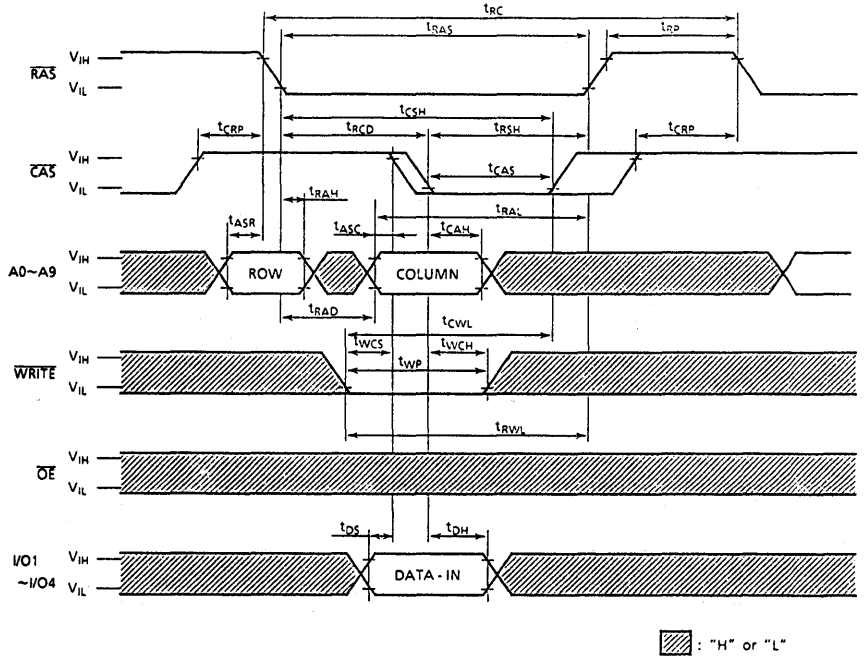
READ CYCLE IN THE TEST MODE



Note: $\overline{OE}$ = "L" D_{IN} = OPEN

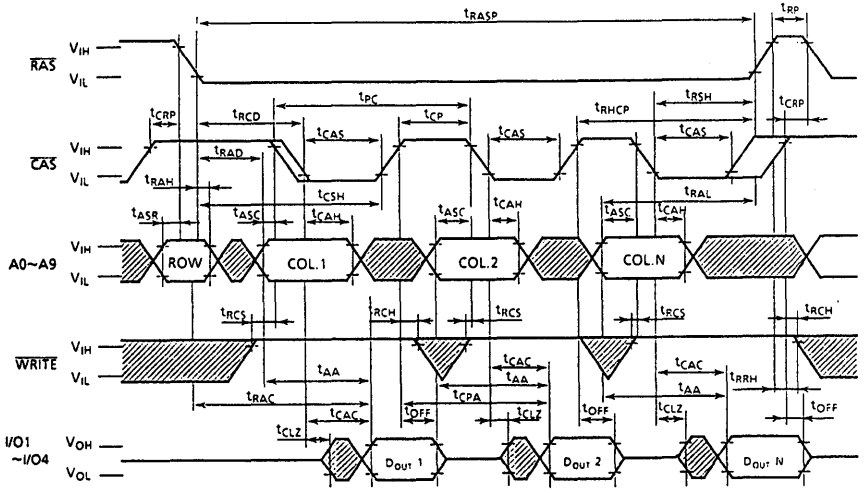
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



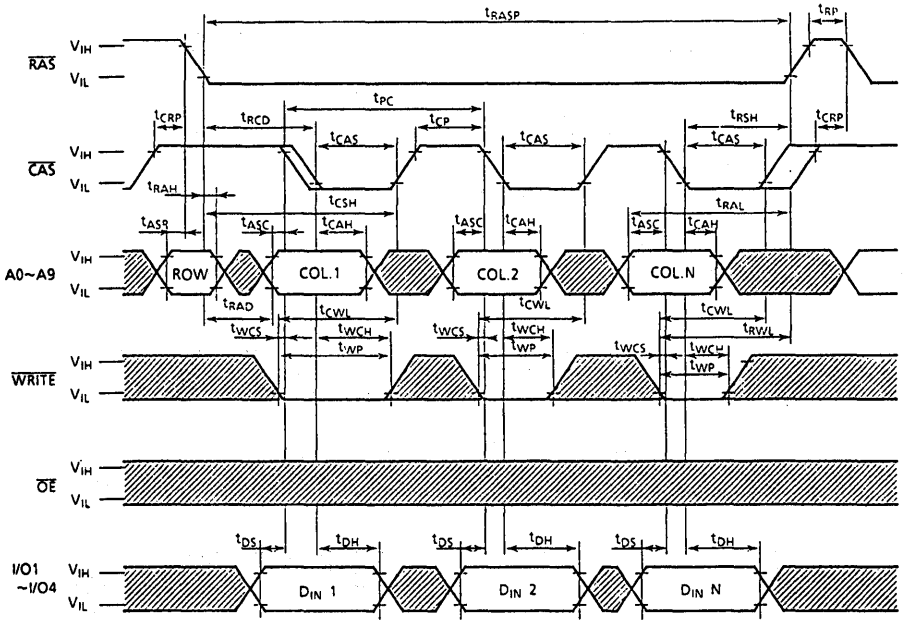
Note: D_{OUT} = OPEN

FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note: $\overline{OE}$ = "L" D_{IN} = OPEN

FAST PAGE MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note: D_{OUT} = OPEN

▨: "H" or "L"

TEST MODE

The TC514400ASJL/AFTL/ATRL is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A0c is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1".

If they were not equal the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514400ASJL/AFTL/ATRL. In "Test Mode", the 1M54 DRAM can be tested as if it were a 512K54 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

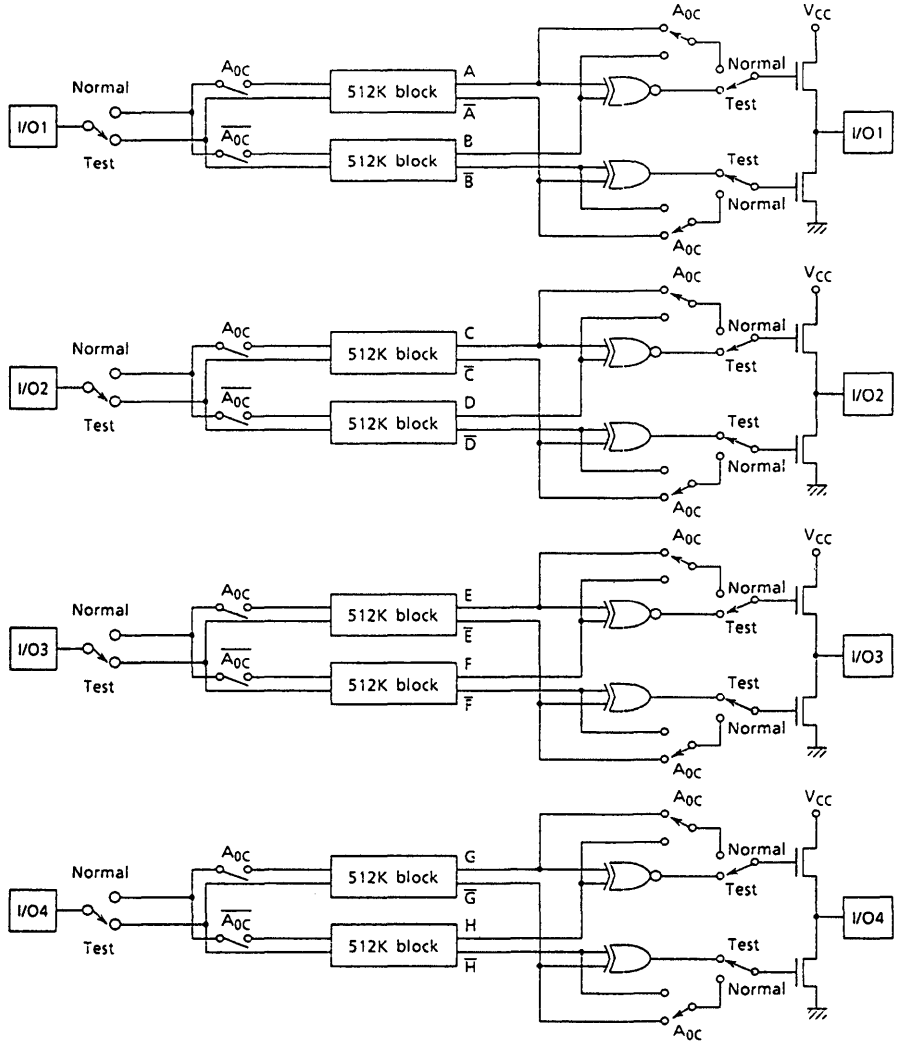


Figure 1

1,048,576 WORD X 4 BIT DYNAMIC RAM

DESCRIPTION

The TC51V4400ASJL/AFTL is the new generation dynamic RAM organized 1,048,576 word by 4 bit. The TC51V4400ASJL/AFTL utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC51V4400ASJL/AFTL to be packaged in a standard 26/20 pin plastic SOJ (300), 26/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 3.3V±0.3V tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of 3.3V±0.3V with a built-in V_{BB} generator
- Low Power
  216mW MAX .Operating
  0.54mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC51V4400ASJL : SOJ26-P-300A
  TC51V4400AFTL : TSOP26-P-300

KEY PARAMETERS

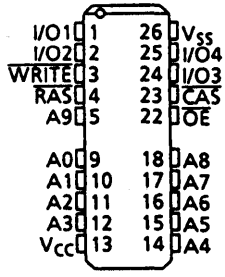
ITEM		TC51V4400ASJL/AFTL
t_{RAC}	$\overline{RAS}$ Access Time	80ns
t_{AA}	Column Address Access Time	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	150ns
t_{PC}	Fast Page Mode Cycle Time	50ns

PIN NAME

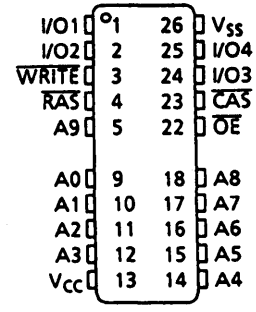
A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground

PIN CONNECTION (TOP VIEW)

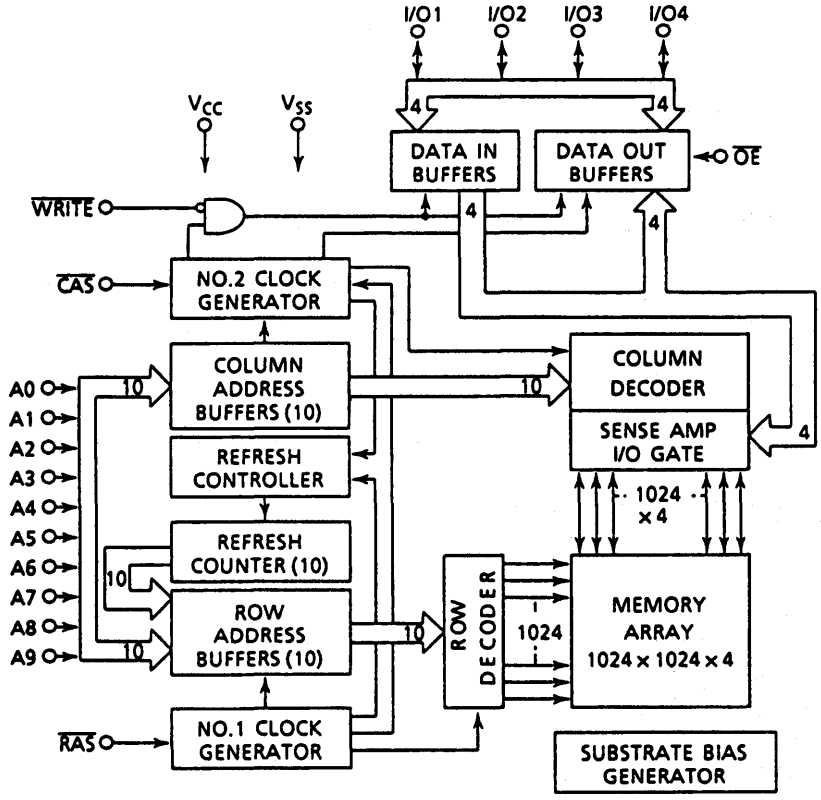
Plastic SOJ



Plastic TSOP (Normal Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	—0.5~V_{CC}+0.5	V	1
Output Voltage	V_{OUT}	—0.5~V_{CC}+0.5	V	1
Power Supply Voltage	V_{CC}	— 0.5~4.6	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	Input HighVoltage	2.2	-	V_{CC}+0.3	V	2
V_{IL}	Input LowVoltage	-0.3	-	0.6	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN)	TC51V4400ASJL/AFTL-80	-	60	mA	3,4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			1	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC51V4400ASJL/AFTL-80	-	60	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC51V4400ASJL/AFTL-80	-	40	mA	3,4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			250	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC51V4400ASJL/AFTL-80	-	60	mA	3, 5
I_{CC7}	BATTERY BACK UP CURRENT Average Power Suuply Current, Battery Back Up Mode ($\overline{CAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$=V_{CC}-0.2V, $\overline{WRITE}$ =V_{CC}-0.2V, A0~9=V_{CC}-0.2V or 0.2V, I/O~4=Vcc-0.2V, 0.2V or OPEN: t_{RC}=125µs, t_{RAS}=t_{RAS} MIN. ~1µs)		-	300	µA	6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≤V_{IN}≤0.5V, All Other Pins Not Under Test=OV)		-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (OV≤V_{OUT}≤5.5V),		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 3.3V ± 0.3V, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC51V4400ASJL /AFTL -80		UNIT	NOTES
		MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	80	ns	10,15,16
t_{CAC}	Access Time from $\overline{CAS}$	-	20	ns	10,15
t_{AA}	Access Time from Column Address	-	40	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	ns	
t_{RP}	$\overline{RAS}$ Presharge Time	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	0	ns	
t_{CAH}	Column Address Hold Time	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	ns	12
t_{WCH}	Write Command Hold Time	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514400ASJL/AFTL -80		UNIT	NOTES
		MIN	MAX		
t_{WP}	Write Command Pulse Width	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	ns	13
t_{DH}	Data Hold Time	15	-	ns	13
t_{REF}	Refresh Period	-	128	ms	
t_{WCS}	Write Command Set-Up Time	0	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	110	-	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	70	-	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	75	-	ns	14
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	ns	10
t_{OED}	$\overline{OE}$ to Data Delay	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	ns	11
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC514400ASJL/AZ/AFT -80		UNIT	NOTES
		MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	155	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	ns	10,15,16
t_{CAC}	Access Time from $\overline{CAS}$	-	25	ns	10,15
t_{AA}	Access Time from Column Address	-	45	ns	10,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	ns	10
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead	45	-	ns	

CAPACITANCE (V_{CC} = 3.3V ±0.3V, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. t_{RAS} (max.)=1μs is only applied to refersh of battery-back up. t_{RAS}(max)=10μs is applied to functional operating.

7. An initial pause of 2ms is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

8. AC measurements assume t_T=5ns.

9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

10. Measured with a load equivalent to 100pF and at V_{OH}=2.0V(I_{OUT}=-2mA), V_{OL}=0.8V (I_{OUT}=2mA).

11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

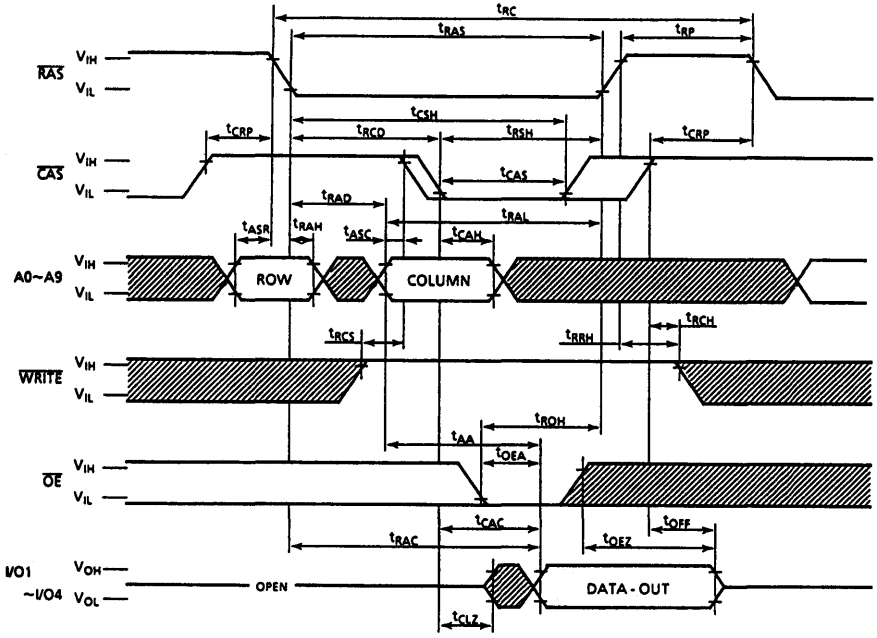
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWP} > t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

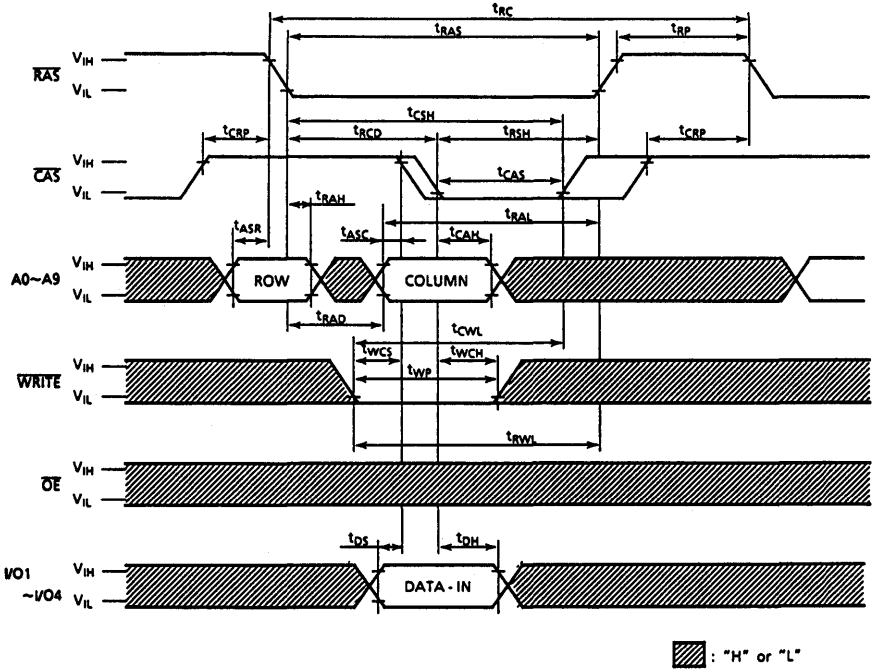
READ CYCLE



Note: D_{IN} = OPEN

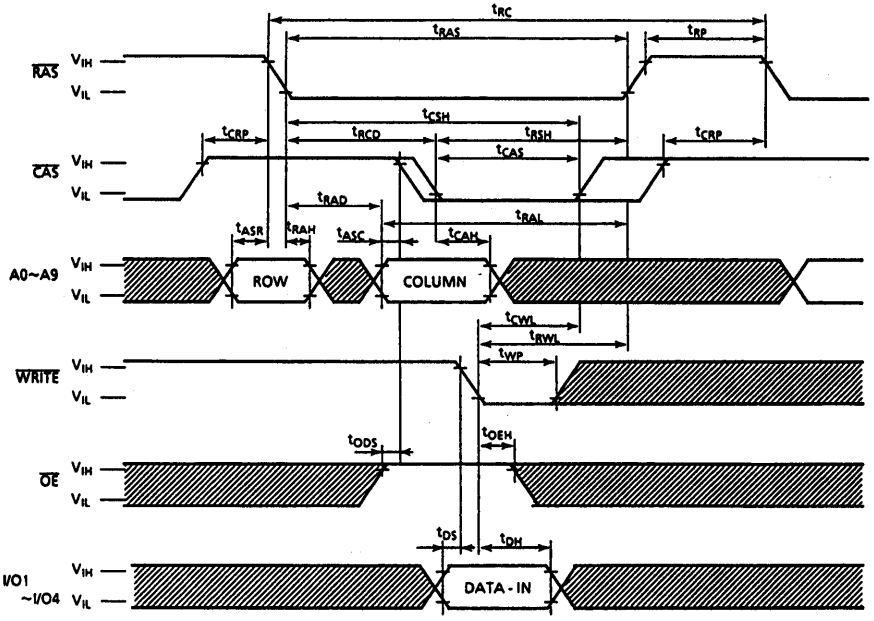
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE)



▨ : "H" or "L"

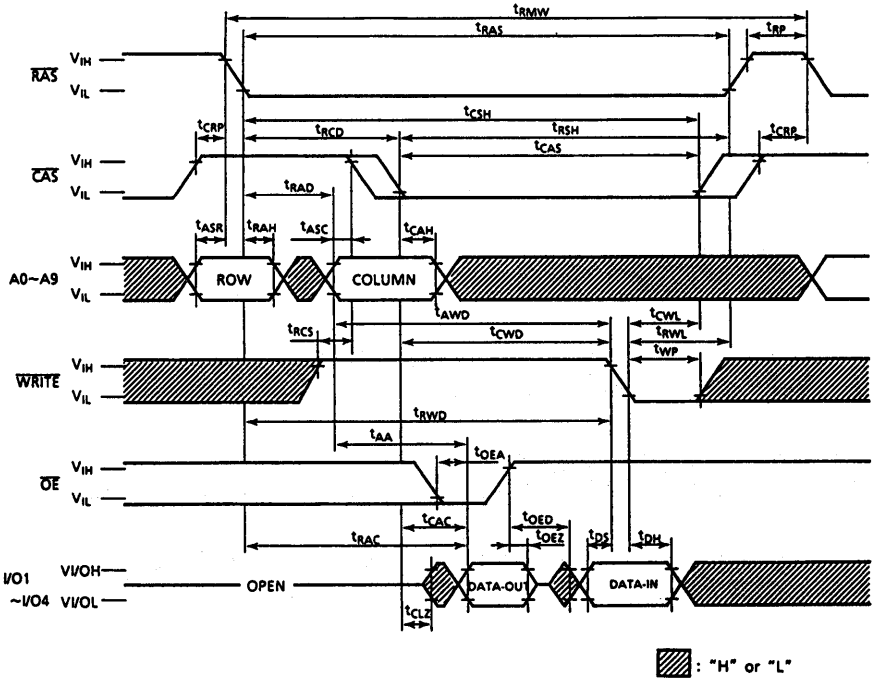
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

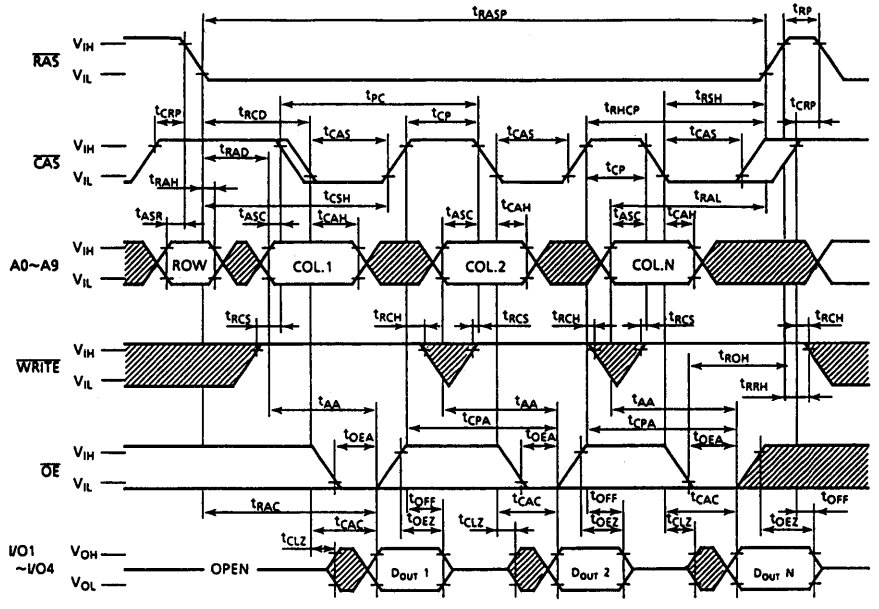
▨: "H" or "L"

READ-MODIFY-WRITE CYCLE



▨: "H" or "L"

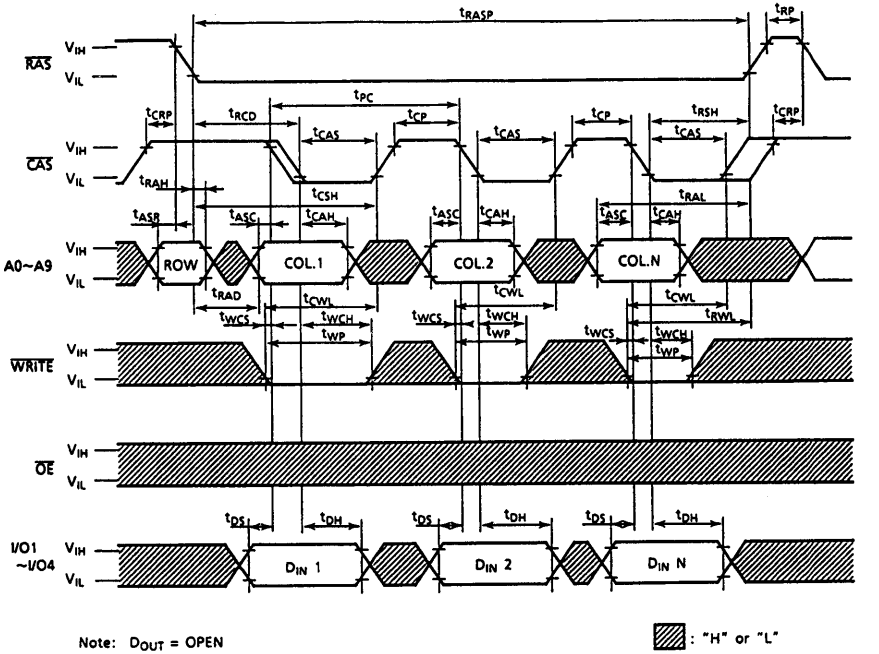
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

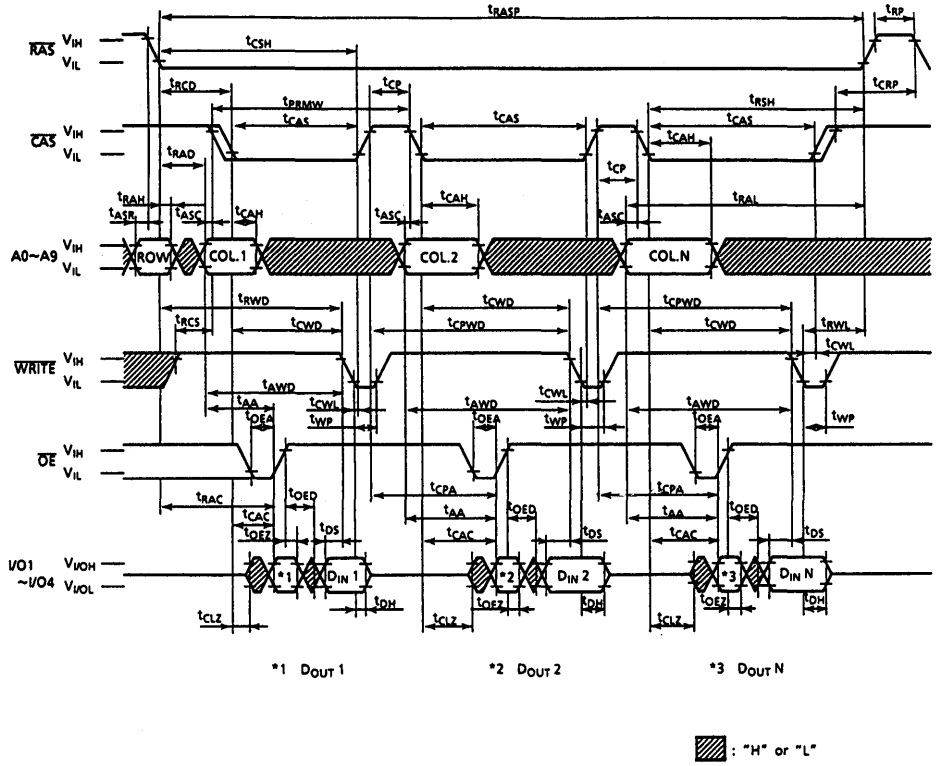
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



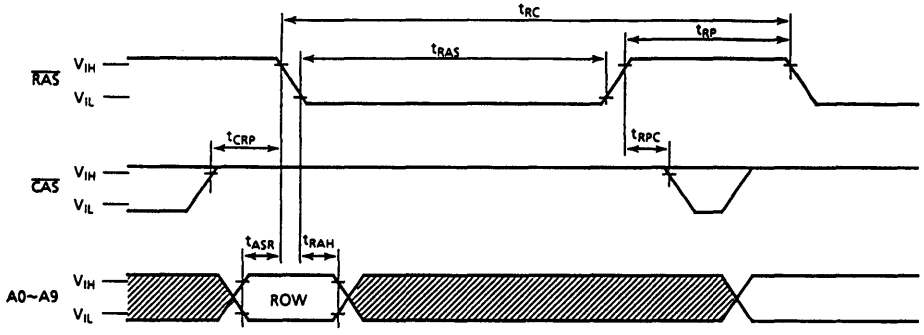
Note: D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



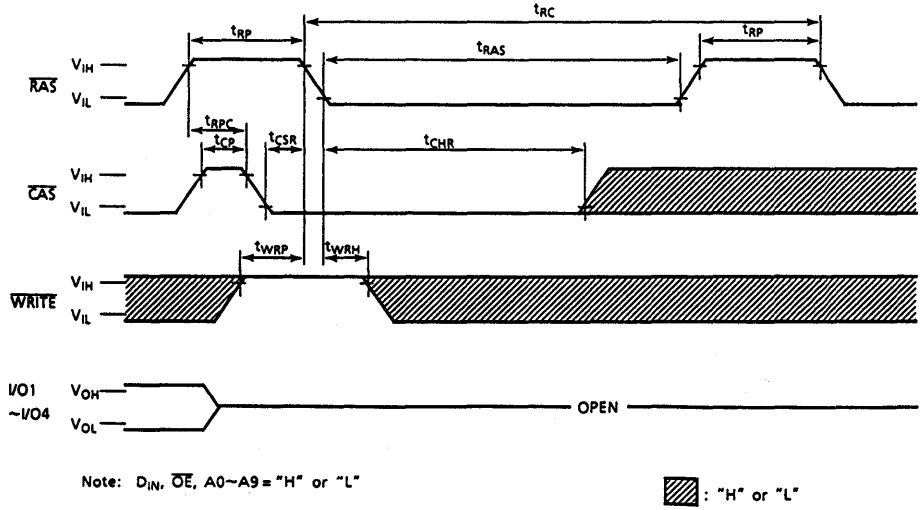
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"
D_{OUT} = OPEN

▨ : "H" or "L"

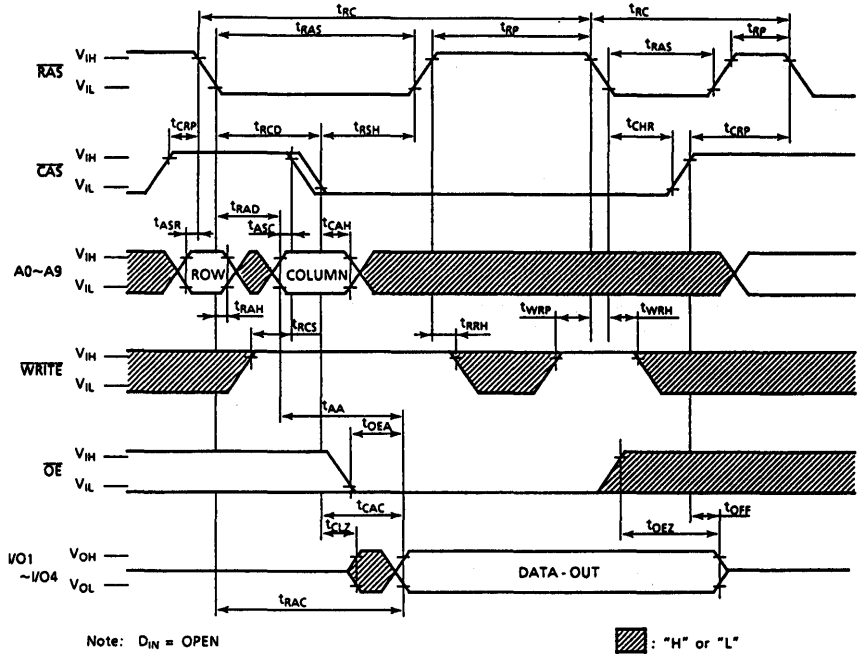
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

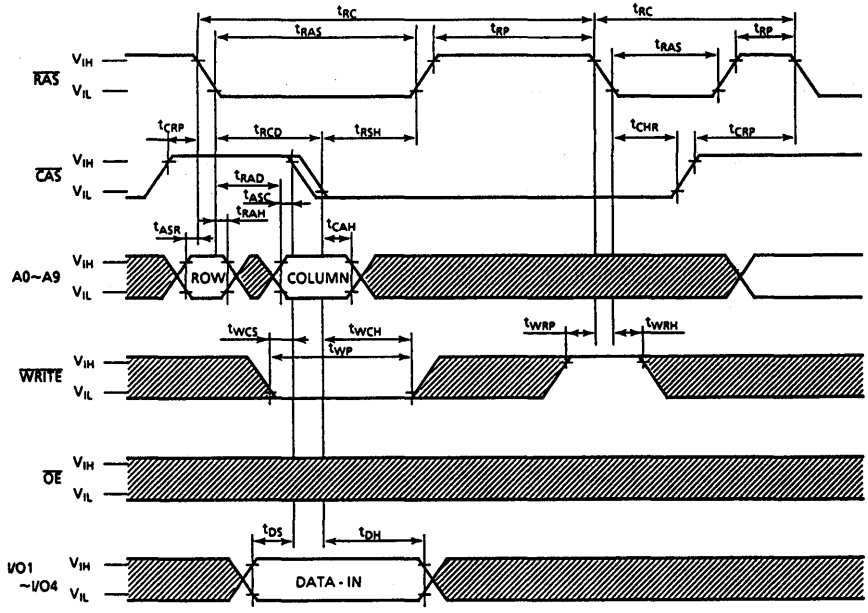
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨: "H" or "L"

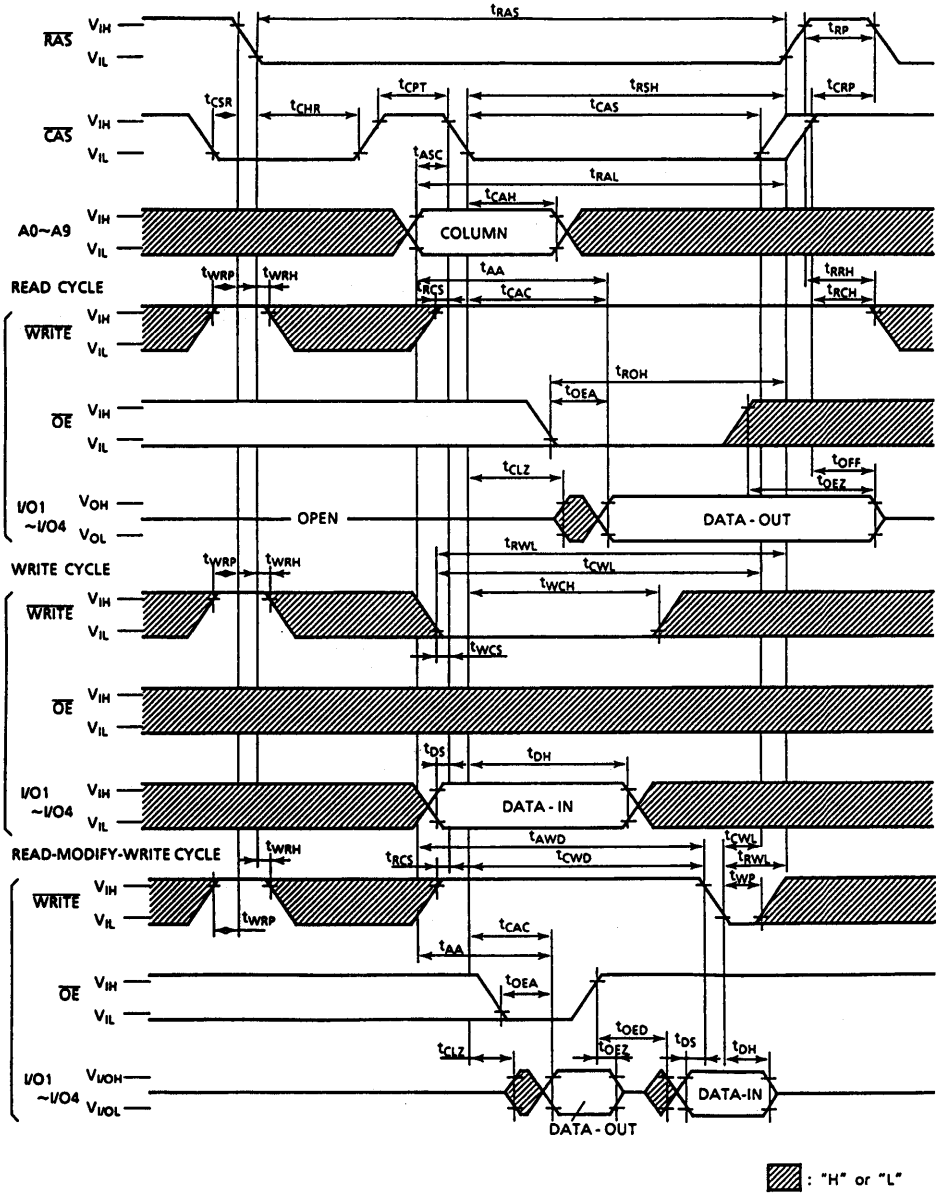
HIDDEN REFRESH CYCLE (WRITE)



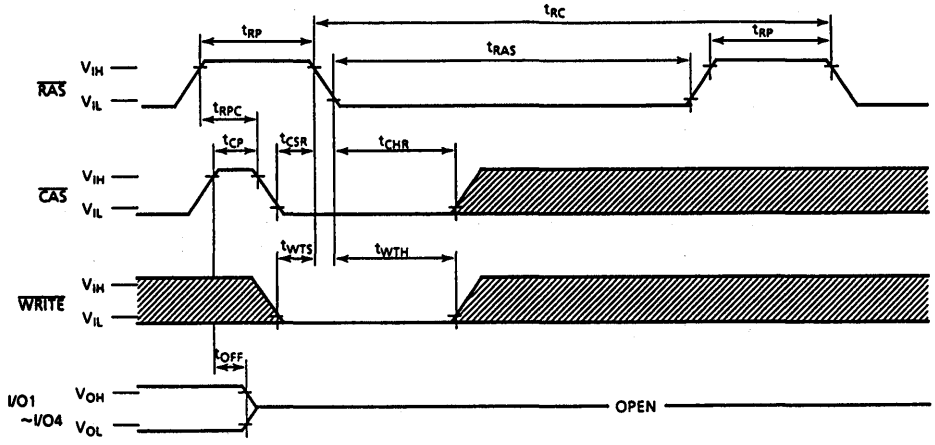
Note: D_{OUT} = OPEN

▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



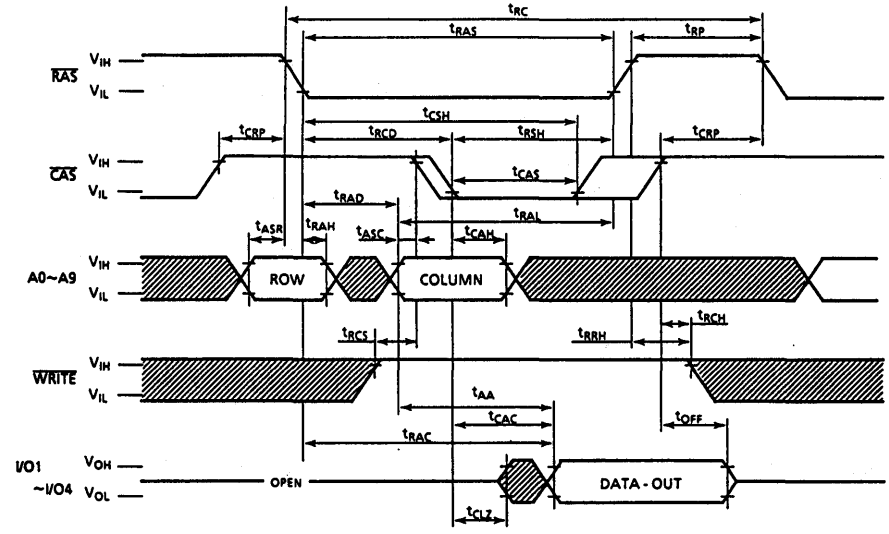
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

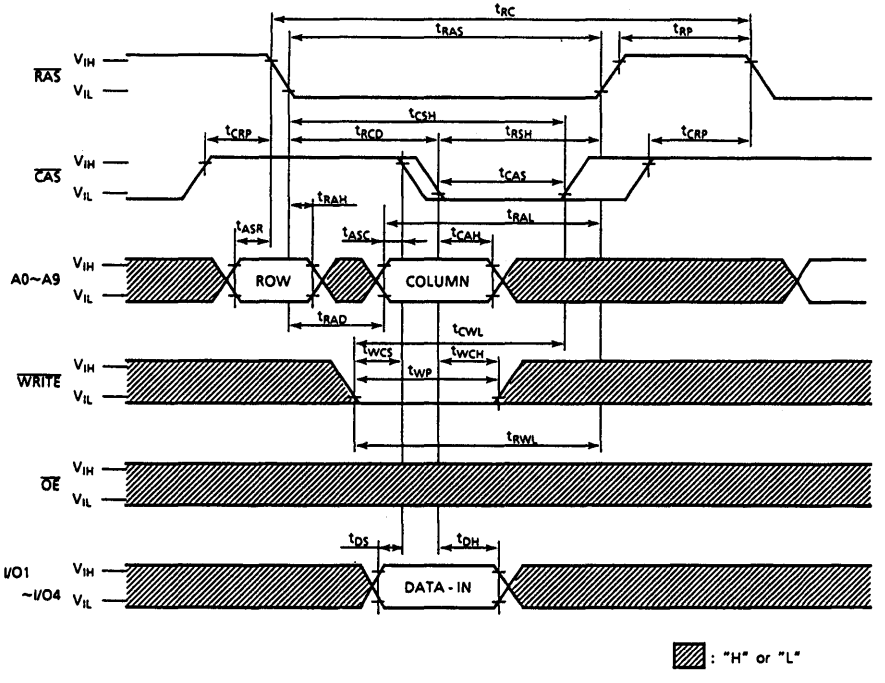
READ CYCLE IN THE TEST MODE



Note: $\overline{OE}$ = "L" D_{IN} = OPEN

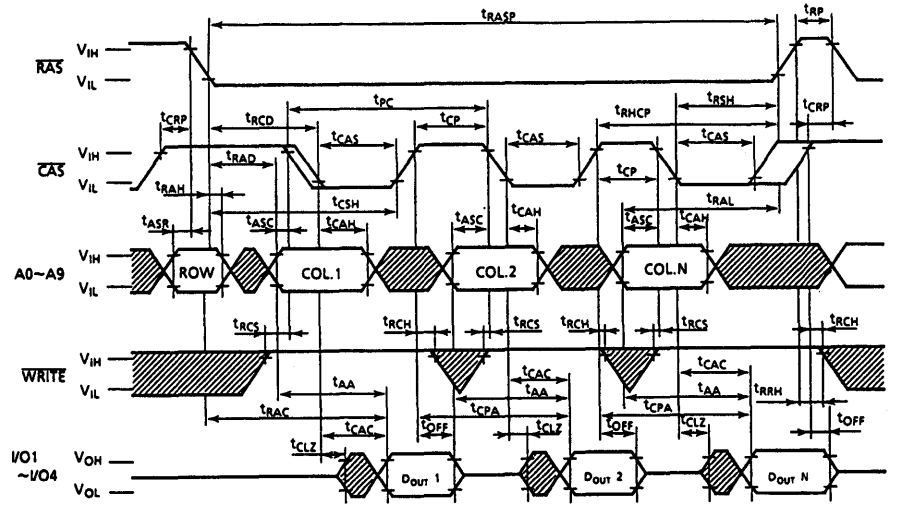
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE) IN THE TEST MODEFAST PAGE MODE



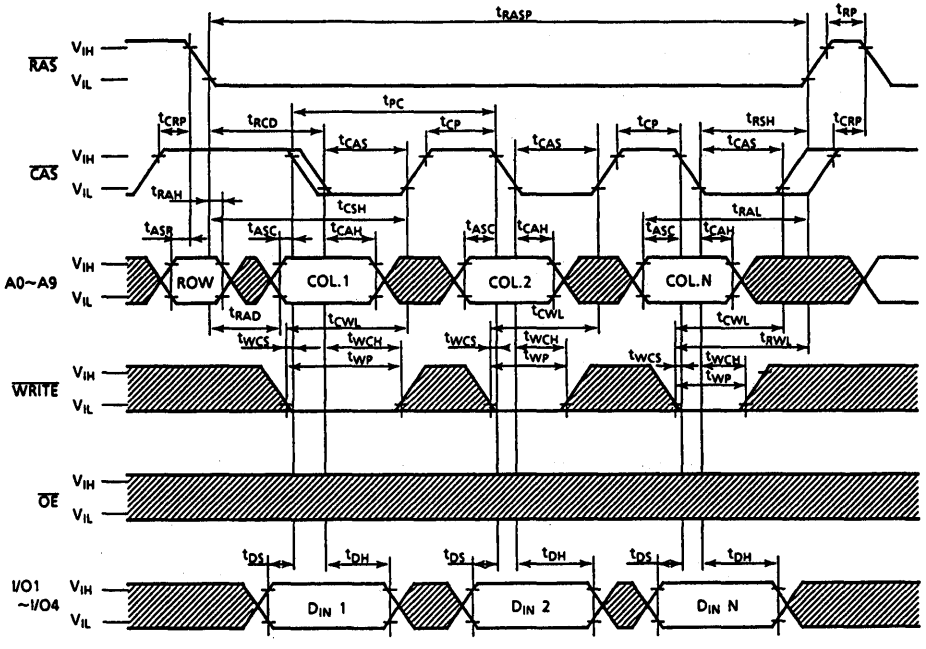
Note: D_{OUT} = OPEN

READ CYCLE IN THE TEST MODE



Note: $\overline{OE}$ = "L" D_{IN} = OPEN

FAST PAGE MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note: D_{OUT} = OPEN

▨ : "H" or "L"

TEST MODE

The TC51V4400/ASJL/AFTL is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A0c is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1".

If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC51V4400/ASJL/AFTL. In "Test Mode", the 1MX4 DRAM can be tested as if it were a 512KX4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

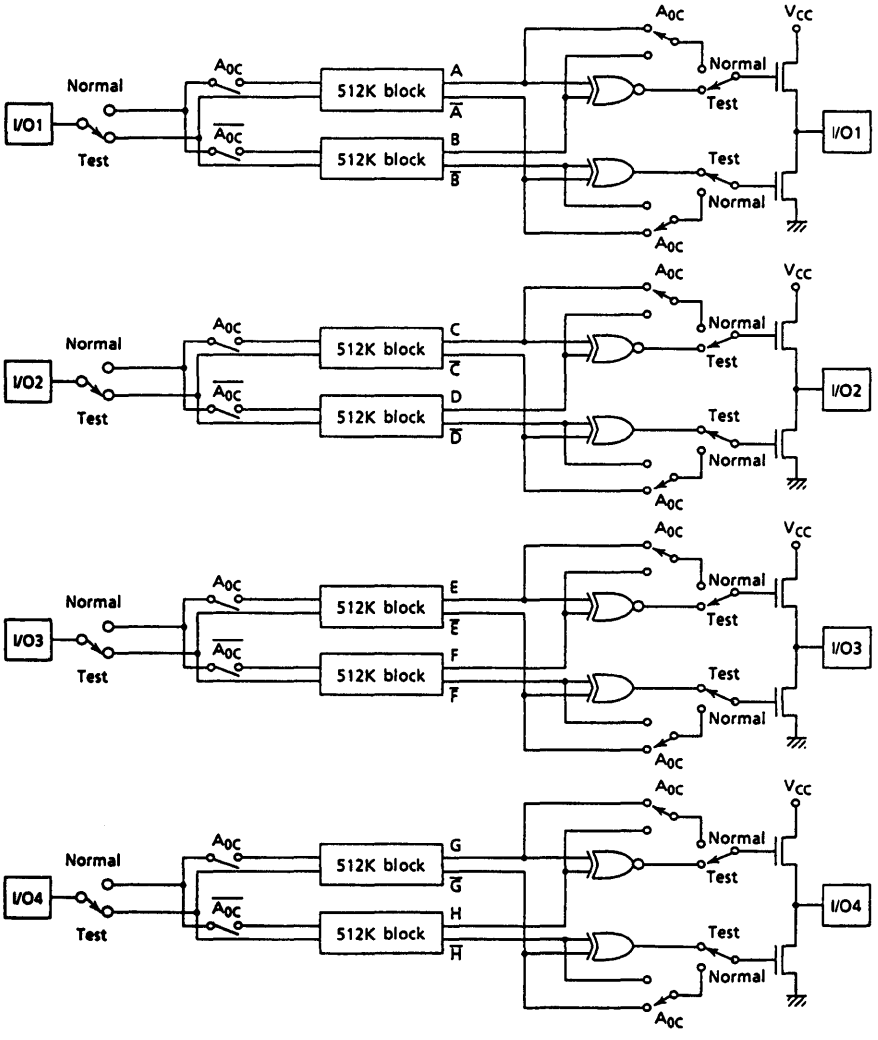


Figure 1

1,048,576 WORD X 4 BIT DYNAMIC RAM

DESCRIPTION

The TC514410ASJ is the new generation dynamic RAM organized 1,048,576 word by 4 bit. The TC514410ASJ utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514410ASJ to be packaged in a standard, 26/20 pin plastic SOJ (300mil). The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  660mW MAX .Operating
  (TC51440ASJ-60)
  550mW MAX. Operating
  (TC51440ASJ-70)
  468mW MAX. Operating
  (TC51440ASJ-80)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC514410ASJ : SOJ26-P-300A

KEY PARAMETERS

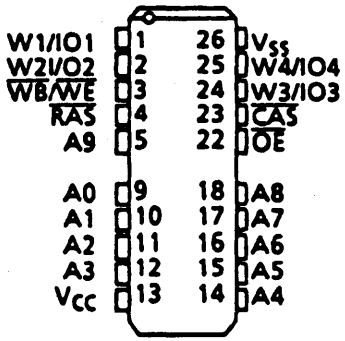
ITEM		TC514410ASJ		
		-60	-70	-80
t_{RAC}	$\overline{RAC}$ Access Time	60ns	70ns	80ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC}	Cycle Time	110ns	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAME

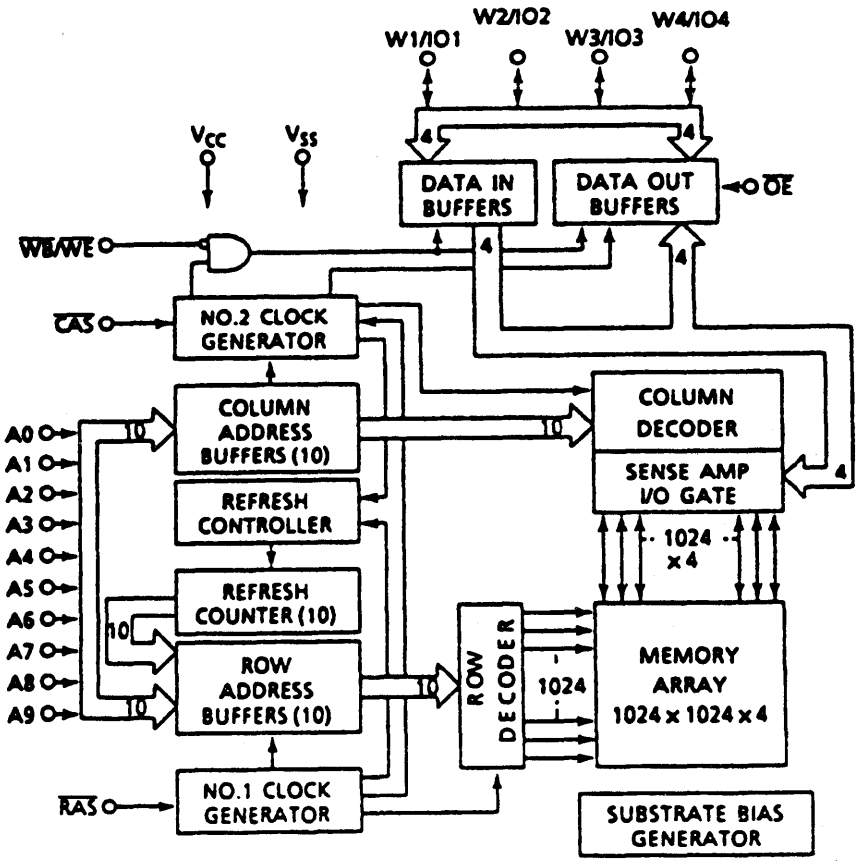
A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
WB/$\overline{WE}$	Write Per Bit/Read/Write Input
$\overline{OE}$	Output Enable
W1/IO1~ W4/I04	Write Select/Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

PIN CONNECTION (TOP VIEW)

Plastic SOJ



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC5144100ASJ-60	-	120	mA	3,4 5
		TC5144100ASJ-70	-	100		
		TC5144100ASJ-80	-	85		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC5144100ASJ-60	-	120	mA	3, 5
		TC5144100ASJ-70	-	100		
		TC5144100ASJ-80	-	85		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC5144100ASJ-60	-	70	mA	3,4 5
		TC5144100ASJ-70	-	70		
		TC5144100ASJ-80	-	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC5144100ASJ-60	-	120	mA	3, 5
		TC5144100ASJ-70	-	100		
		TC5144100ASJ-80	-	85		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≤V_{IN}≤6.5V, All Other Pins Not Under Test=OV)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (OV≤V_{OUT}≤5.5V),		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	CHARACTERISTIC	TC5144100ASJ						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	165	-	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	0	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	CHARACTERISTIC	TC5144100ASJ						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	16	-	16	-	16	ns	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	-	50	-	50	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90	-	100	-	110	-	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60	-	65	-	70	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	70	-	70	-	75	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	-	40	-	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	20	-	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	20	-	ns	
t_{ODS}	Output Disable Set-up Time	0	-	0	-	0	-	ns	
t_{WTS}	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC5144100ASJ						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WBS}	Write Per Bit Set-Up Time	0	-	0	-	0	-	ns	
t_{WBH}	Write Per Bit Hold Time	10	-	10	-	10	-	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	-	0	-	0	-	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	-	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC5144100ASJ						UNIT	NOTES
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	155	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	50	-	55	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	-	85	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	25	ns	9, 14
t_{AA}	Access Time from Column Address	-	35	-	40	-	45	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	45	-	50	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	085	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	85	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	85	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	-	45	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	45	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (W1/IO1~W4/IO4)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Column address can be changed one or less while $\overline{RAS}=V_{IL}$ and CAS = V_{IH}

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

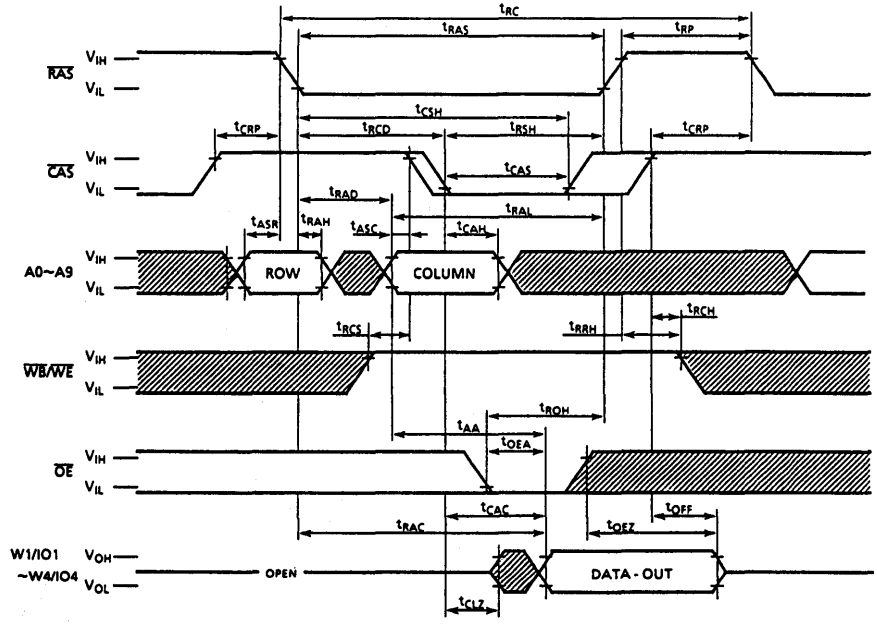
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WB/WE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

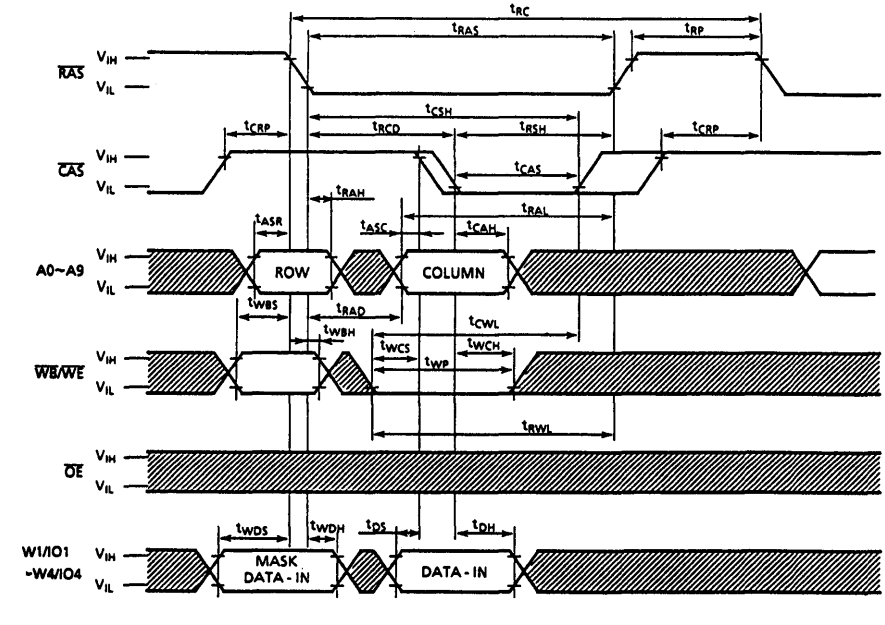
READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

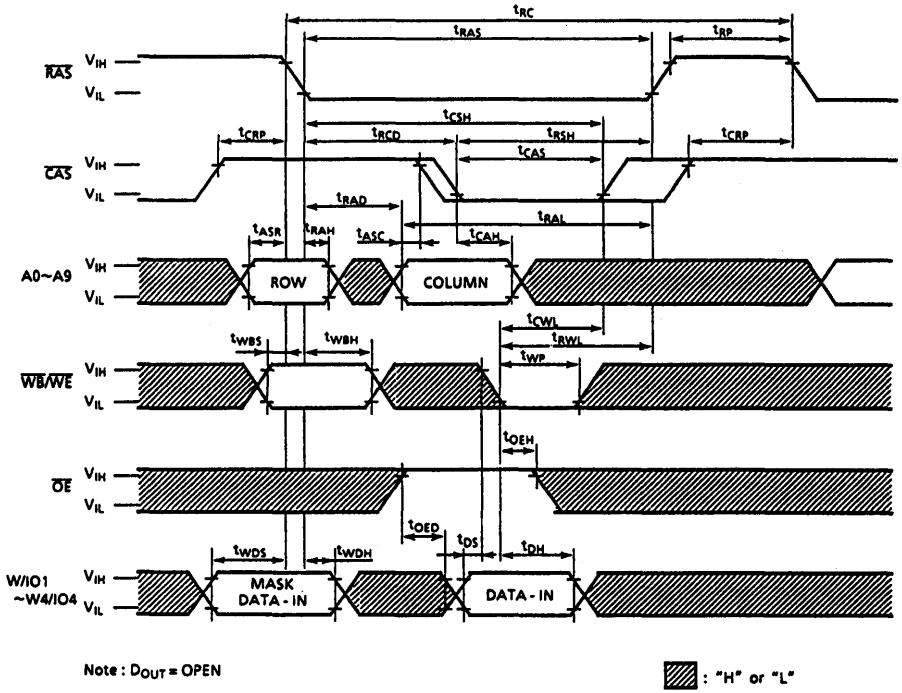
WRITE CYCLE (EARLY WRITE)



Note : D_{OUT} = OPEN

▨ : "H" or "L"

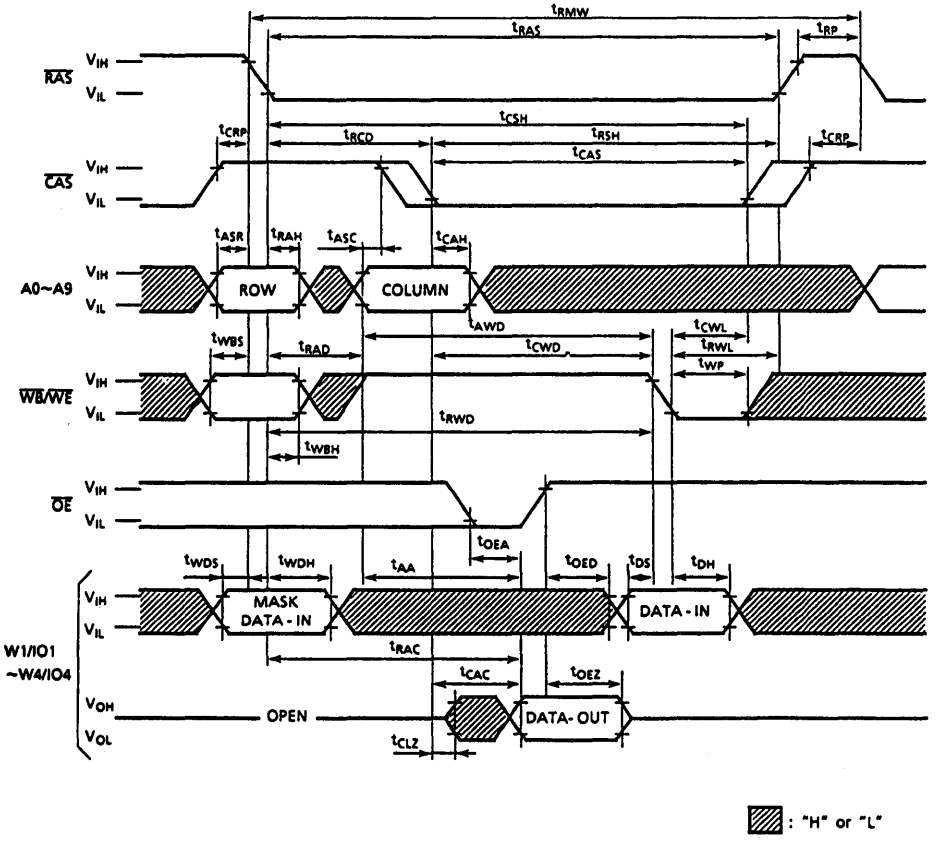
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



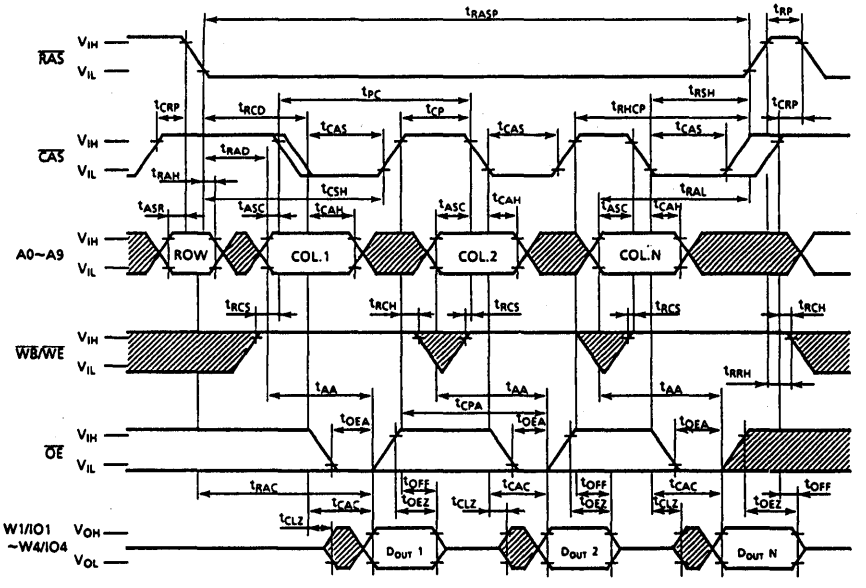
Note : D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



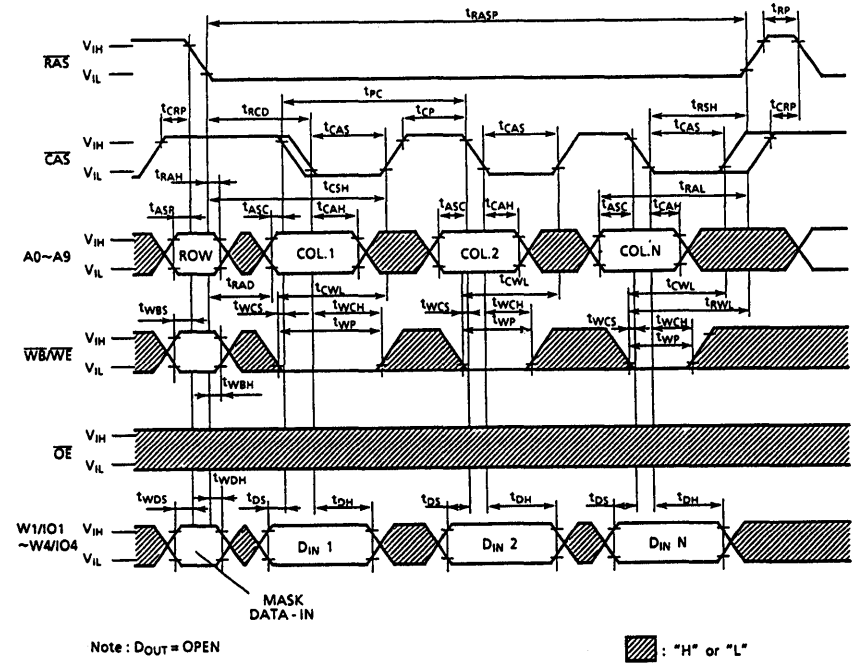
FAST PAGE MODE READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

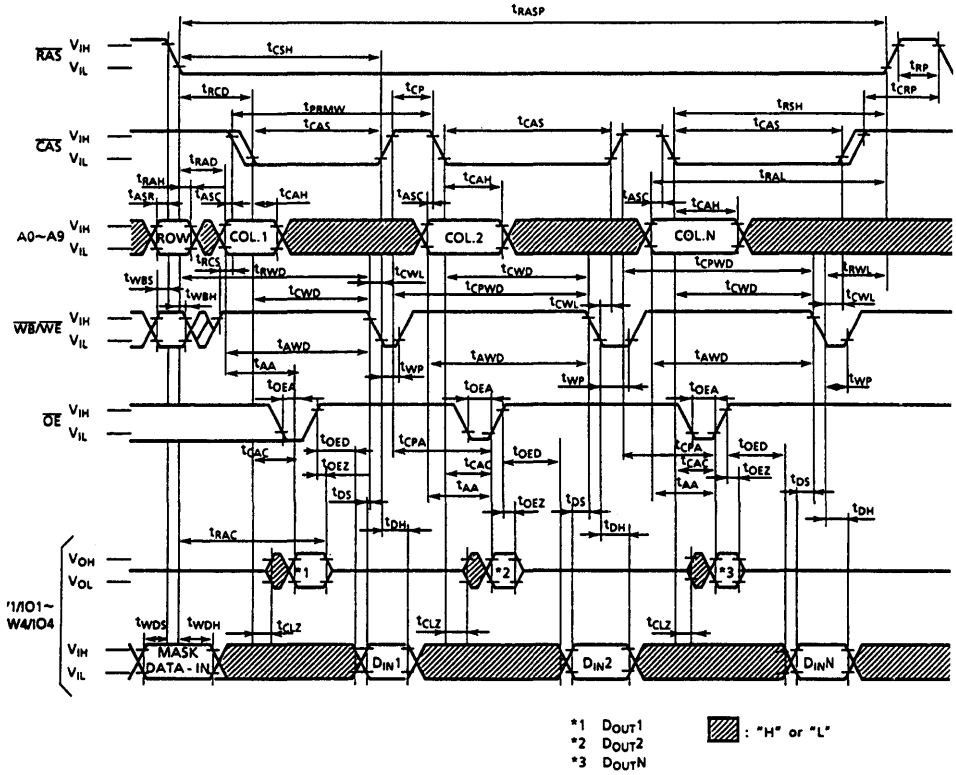
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



Note : D_{OUT} = OPEN

▨ : "H" or "L"

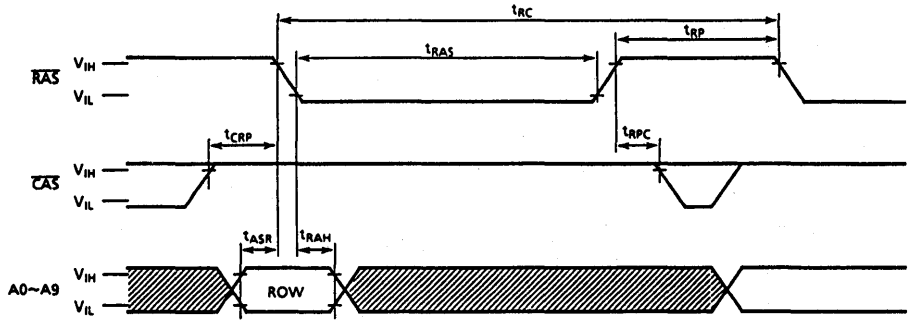
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



*1 $D_{OUT}1$
*2 $D_{OUT}2$
*3 $D_{OUT}N$

▨ : "H" or "L"

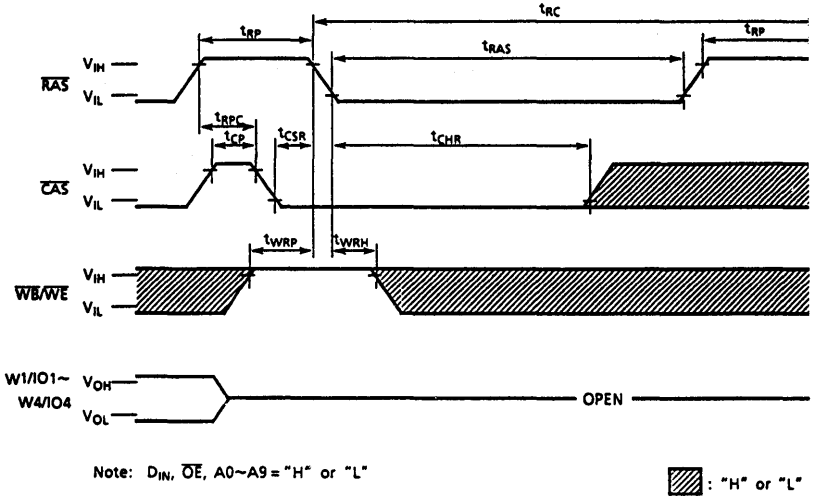
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WB/WE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

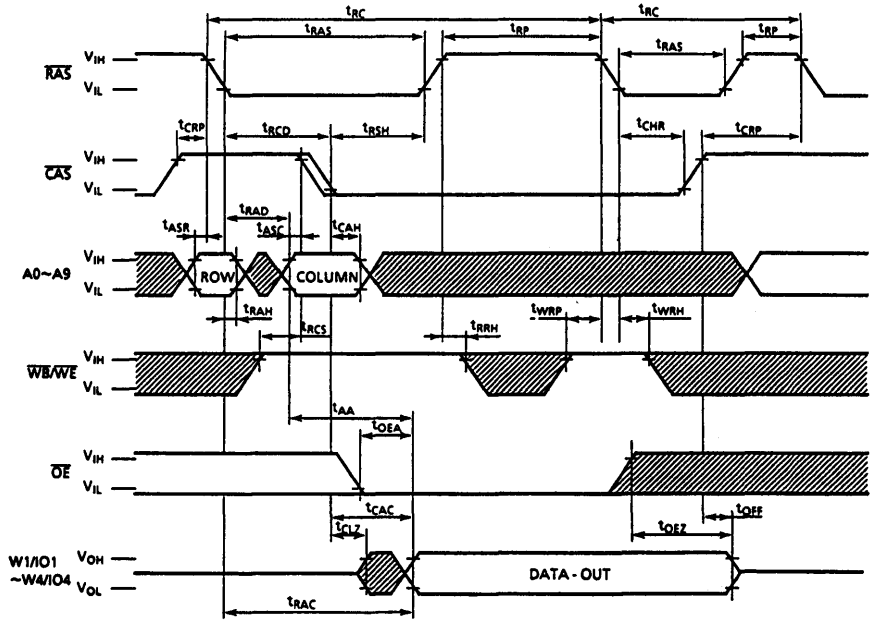
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

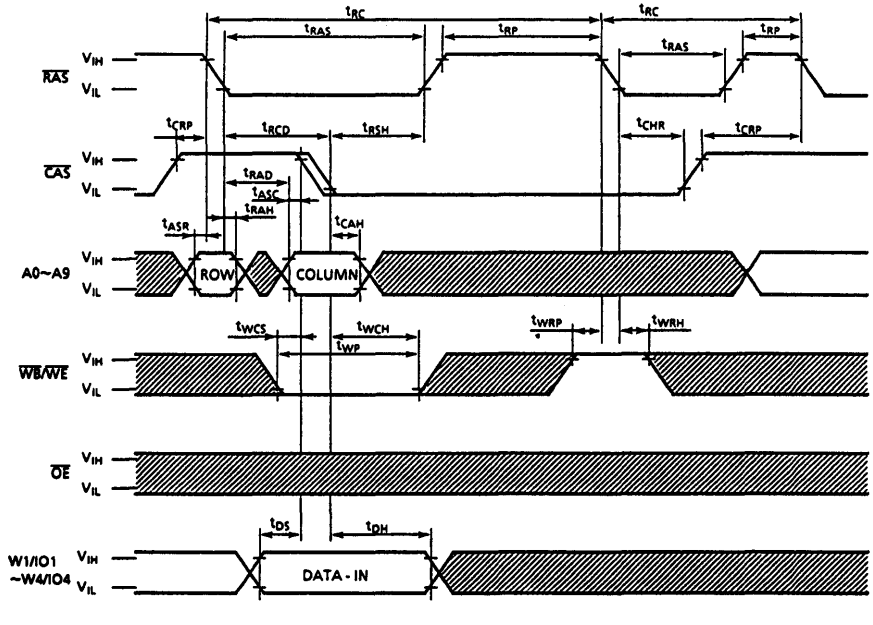
HIDDEN REFRESH CYCLE (READ)



Note : D_{IN} = OPEN

▨ : "H" or "L"

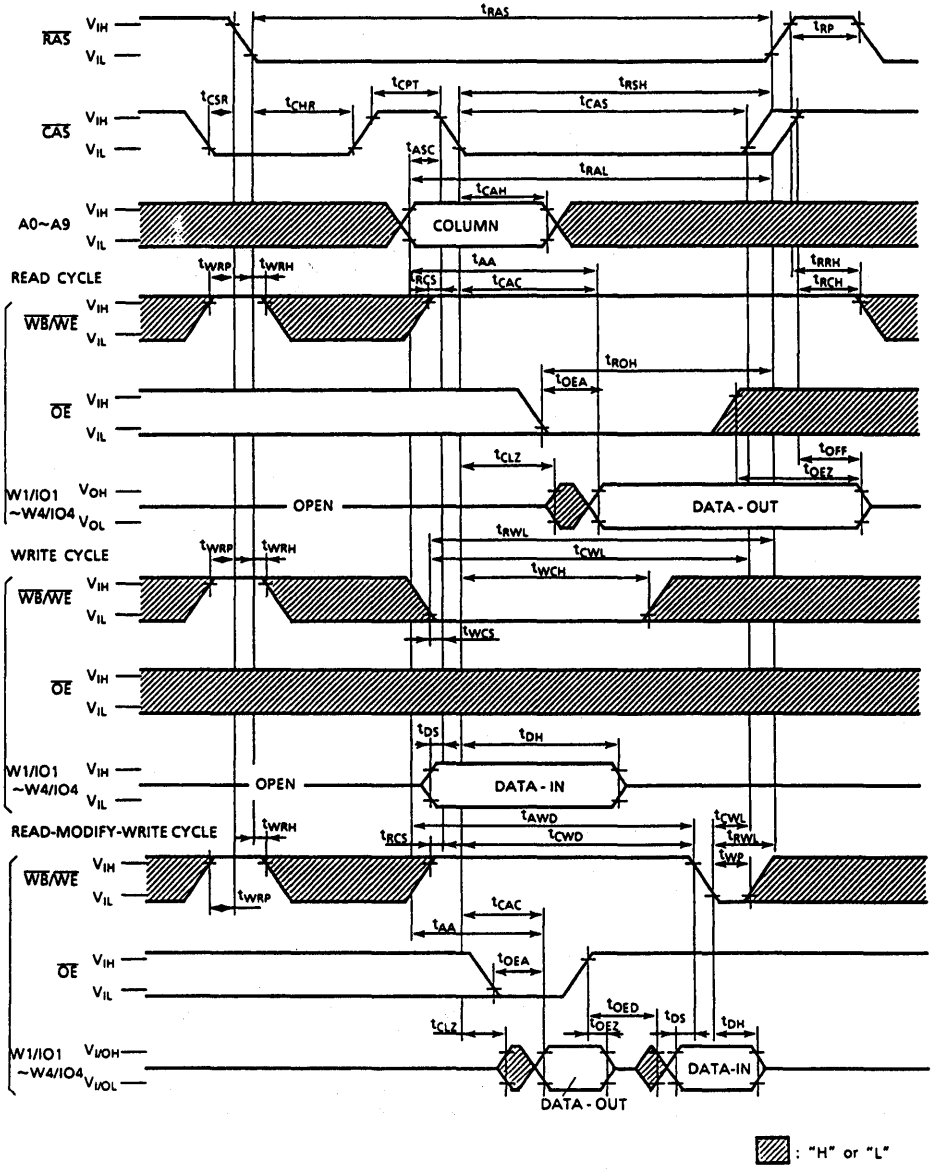
HIDDEN REFRESH CYCLE (WRITE)



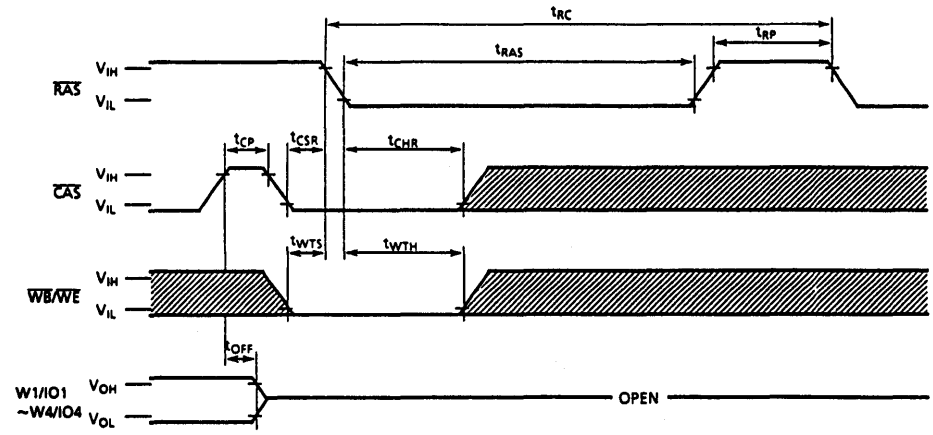
Note : D_{OUT} = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



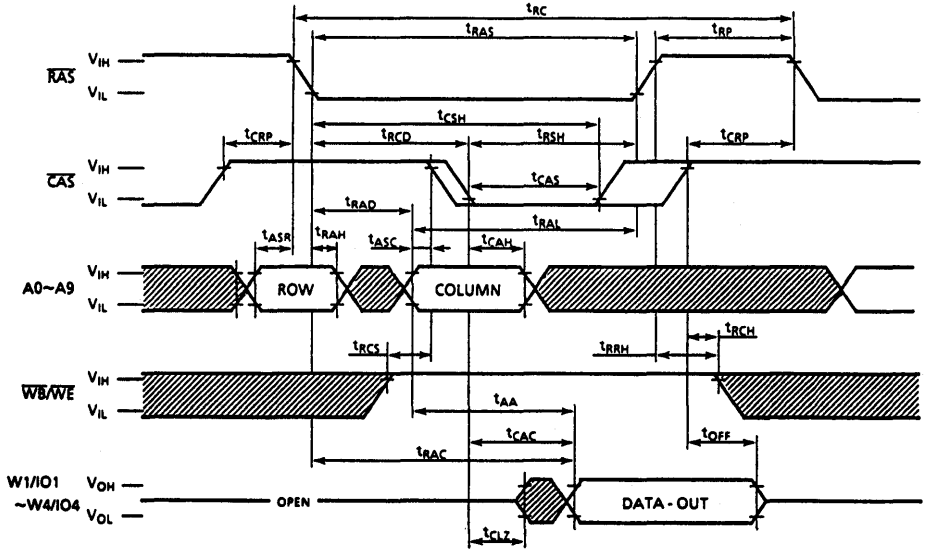
WE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

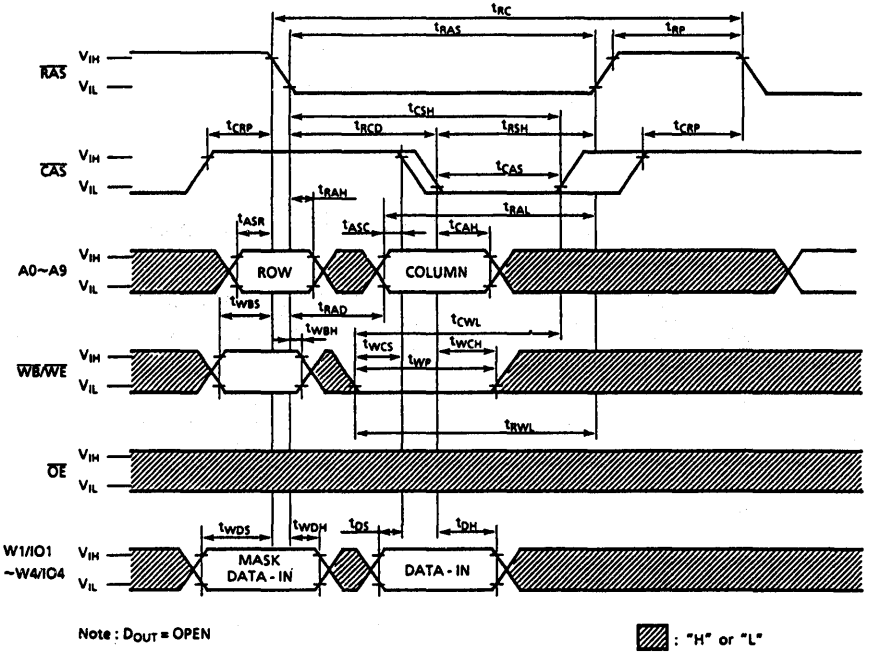
READ CYCLE IN THE TEST MODE



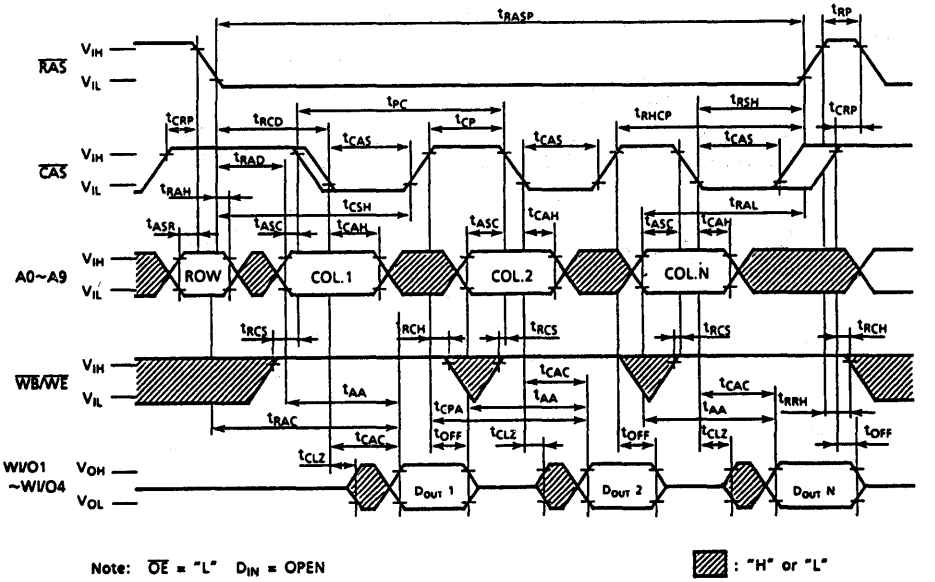
Note: $\overline{OE}$ = "L" D_{IN} = OPEN

▨ : "H" or "L"

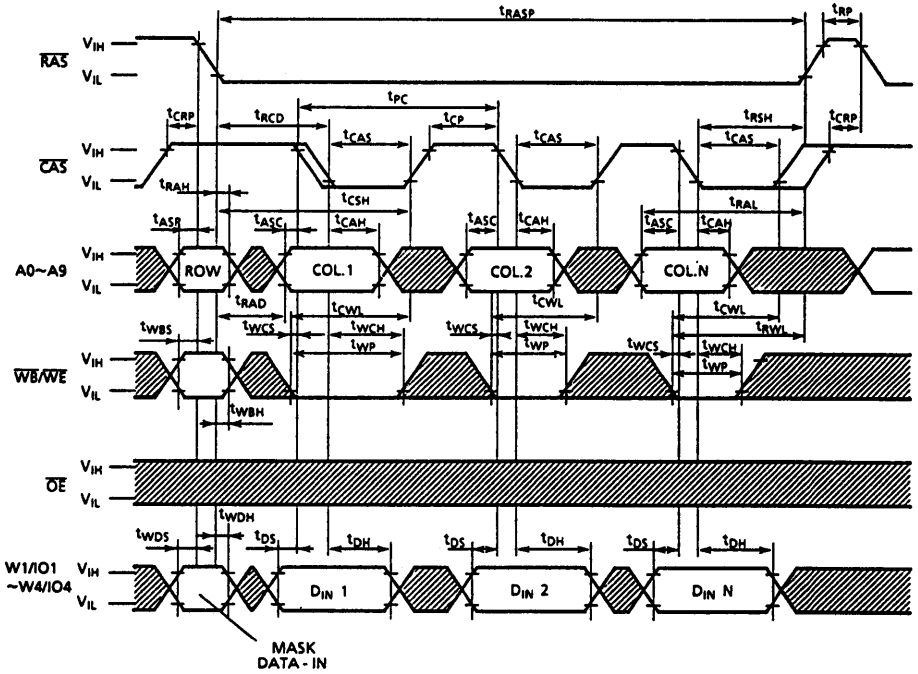
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



FAST PAGE MODE READ CYCLE IN THE TEST MODE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note : D_{OUT} = OPEN

▨ : "H" or "L"

TEST MODE

The TC5144100/ASJ is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A0c is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1".

If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC5144100/ASJ. In "Test Mode", the 1MX4 DRAM can be tested as if it were a 512KX4 DRAM.

"$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" or $\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

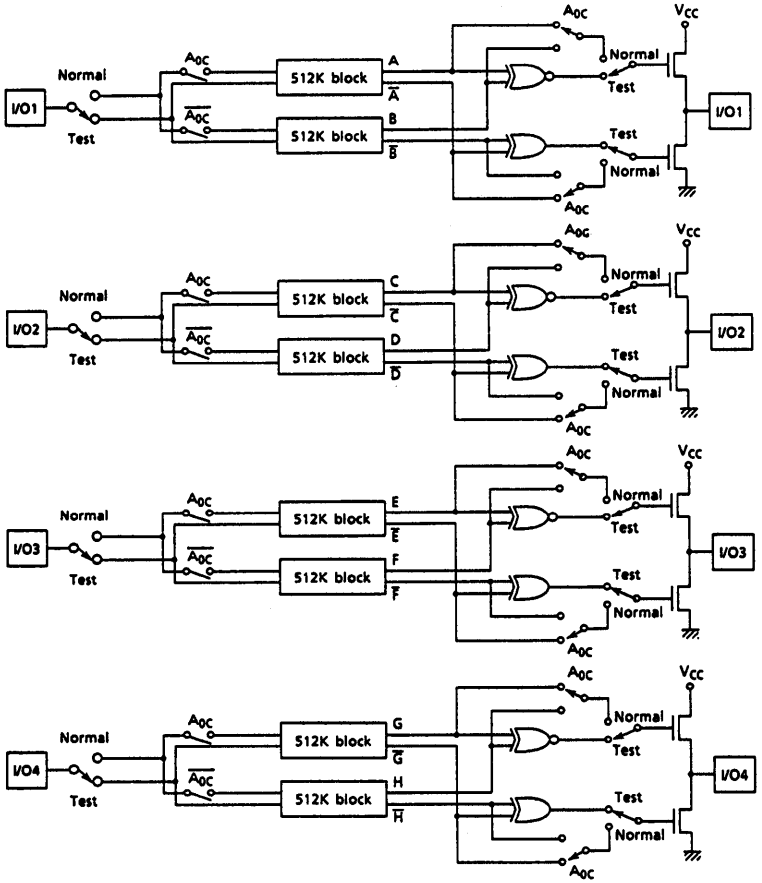


Figure 1

4,194,304 WORD X 4 BIT DYNAMIC RAM

DESCRIPTION

The TC5117400J/Z/FT-60/70 is the new generation dynamic RAM organized 4,194,304 word by 4 bit. The TC5117400J/Z/FT-60/70 utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC5117400J/Z/FT-60/70 to be packaged in 28/24 pin plastic SOJ, 24 pin plastic ZIP and 28/24 pin plastic TSOP. The package provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  660mW MAX. Operating
  (TC5117400J/Z/FT-60)
  550mW MAX. Operating
  (TC5117400J/Z/FT-70)
  5.5mW MAX. Standby
  Outputs unlatched at cycle end allows two dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 2048 refresh cycles/32ms
- Package
  TC5117400J : SOJ28-P-400A
  TC5117400Z : ZIP24-P-475
  TC5117400FT : TSOP28-P-400B

KEY PARAMETERS

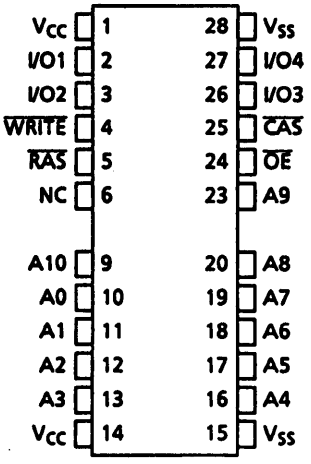
ITEM	TC5117400J/Z/FT	
	-60	-70
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns
t_{AA} Column Address Access Time	30ns	35ns
t_{CAC} $\overline{CAS}$ Access Time	15ns	20ns
t_{RC} Cycle Time	110ns	130ns
t_{PC} Fast Page Mode Cycle Time	40ns	45ns

PIN NAME

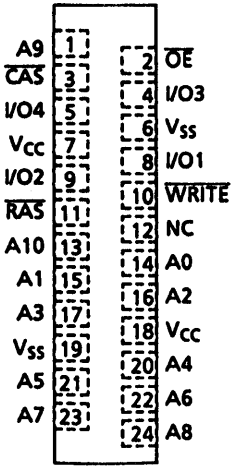
A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/01~I/04	Data Input/Output
V_{CC}	Power (+ 5V)
V_{SS}	Ground

PIN CONNECTION (TOP VIEW)

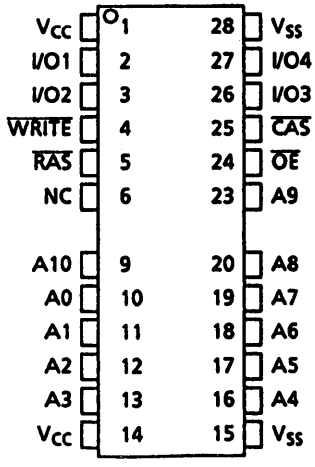
Plastic SOJ



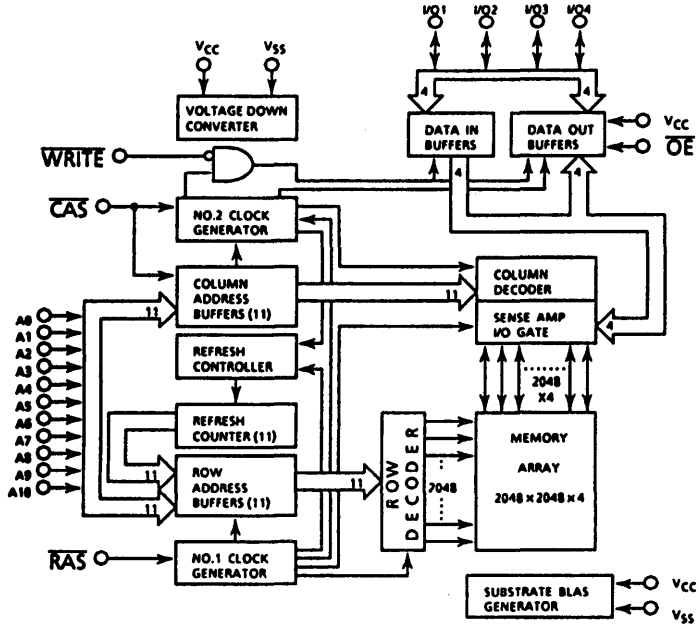
Plastic ZIP



Plastic TSOP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RANGES	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	^0C	1
StorageTemperature	T_{STG}	—55~150	^0C	1
Soldering Temperature •Time	T_{SOLDER}	260 • 10	^0C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Ouput Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITION (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	V_{CC}+0.5	V	2
V_{IL}	Input Low Voltage	—0.5*	—	0.8	V	2

*—2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Address Cycling: t_{RC} = t_{RC} MIN.)	TC5117400J/Z/FT-60	—	120	mA	3, 4, 5
		TC5117400J/Z/FT-70	—	100		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH}		—	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC5117400J/Z/FT-60	—	120	mA	3, 5
		TC5117400J/Z/FT-70	—	100		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC5117400J/Z/FT-60	—	70	mA	3, 4, 5
		TC5117400J/Z/FT-70	—	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}—0.2V)		—	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC5117400J/Z/FT-60	—	120	mA	3, 5
		TC5117400J/Z/FT-70	—	100		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≤V_{IN}≤V_{CC}, All Other Pins Not Under Test=OV)		—10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV≤V_{OUT}≤V_{CC})		—10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= —5mA)		2.4	—	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		—	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC5117410J/Z/FT				UNIT	NOTES
		—60		—70			
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RMW}	Read-Modify-Write Cycle Time	155	—	180	—	ns	
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	85	—	95	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	0	15	0	20	ns	9, 14
t_{AA}	Access Time from Column Address	—	30	—	35	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	9
t_{CLZ}	$\overline{CAS}$ to ouput in Low-Z	0	—	0	—	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	—	40	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	15	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	ns	
t_{RCHS}	Read Command Hold Time	0	—	0	—	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	—	0	—	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC5117400J/Z/FT				UNIT	NOTES
		—60		—70			
		MIN..	MAX.	MIN.	MAX.		
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{DS}	Data Set-Up Time	0	—	0	—	ns	12
t_{DH}	Data Hold Time	10	—	15	—	ns	12
t_{REF}	Refresh Period	—	32	—	32	ms	
t_{WCS}	Write Command Set-Up Time	0	—	0	—	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	40	—	45	—	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	—	95	—	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	55	—	60	—	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	60	—	65	—	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	—	5	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	—	15	—	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	—	5	—	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	20	—	30	—	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	—	10	—	ns	
t_{OEA}	$\overline{OE}$ Access Time	—	15	—	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	15	—	15	—	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	15	0	15	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	15	—	ns	
t_{ODS}	Output Disable Set-Up Time	0	—	0	—	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	—	10	—	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	—	10	—	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	—	10	—	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC5117400J/Z/FT				UNIT	NOTES
		—60		—70			
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	115	—	135	—	ns	
t_{PC}	Fast Page Mode Cycle Time	45	—	50	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	65	—	75	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	9, 14
t_{AA}	Access Time from Column Address	—	35	—	40	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	—	75	—	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	40	—	45	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	40	—	ns	
t_{OEA}	$\overline{OE}$ Access Time	—	20	—	25	ns	
t_{OEH}	$\overline{OE}$ Hold Time	20	—	20	—	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance(A0~A10)	—	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	—	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	—	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. SPEcified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieveS the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

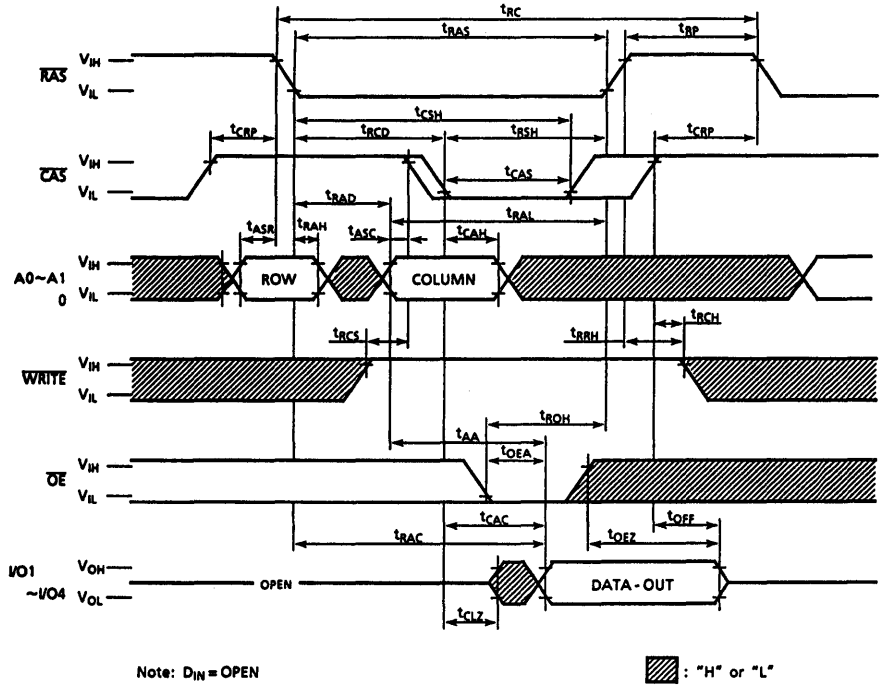
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCS} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

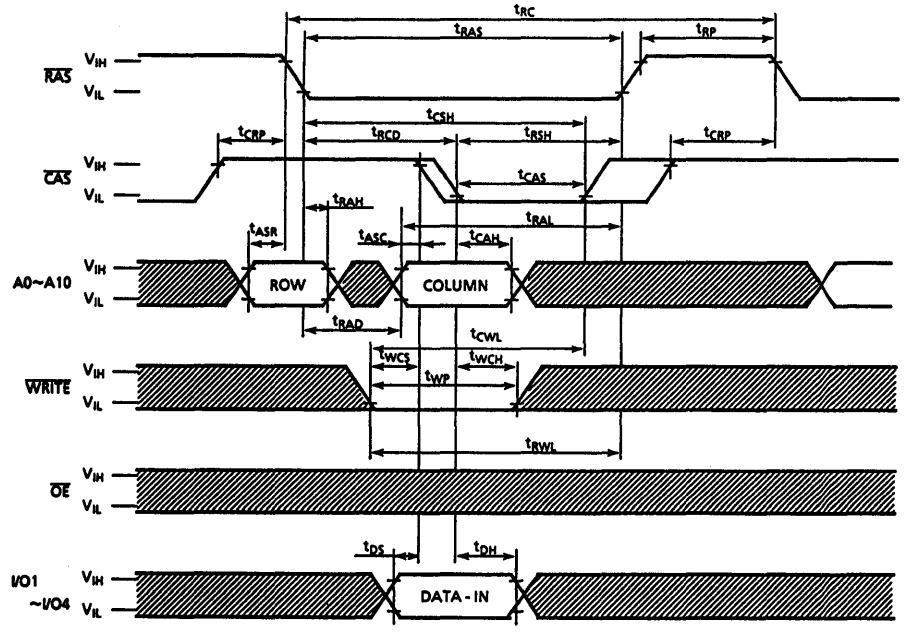
READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

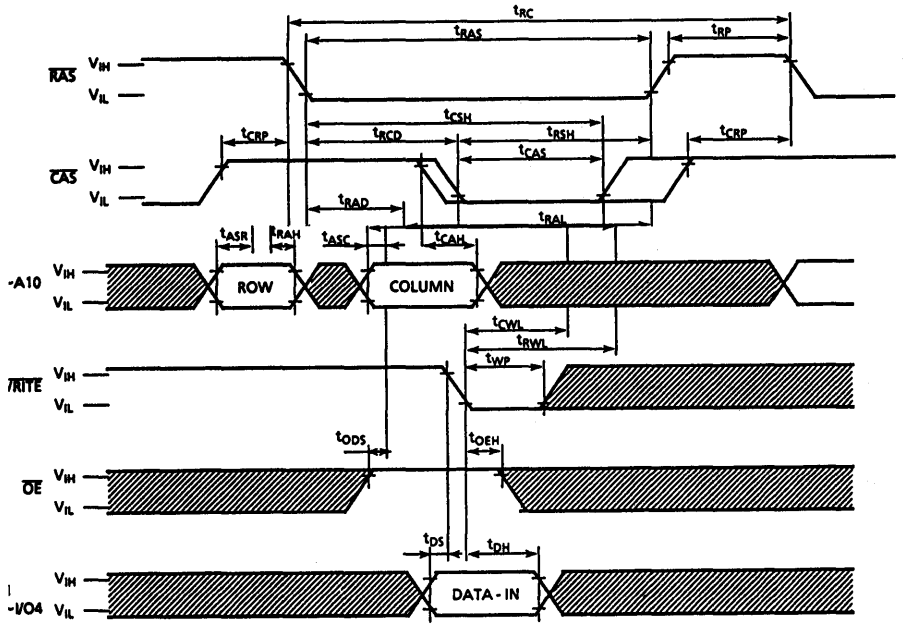
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

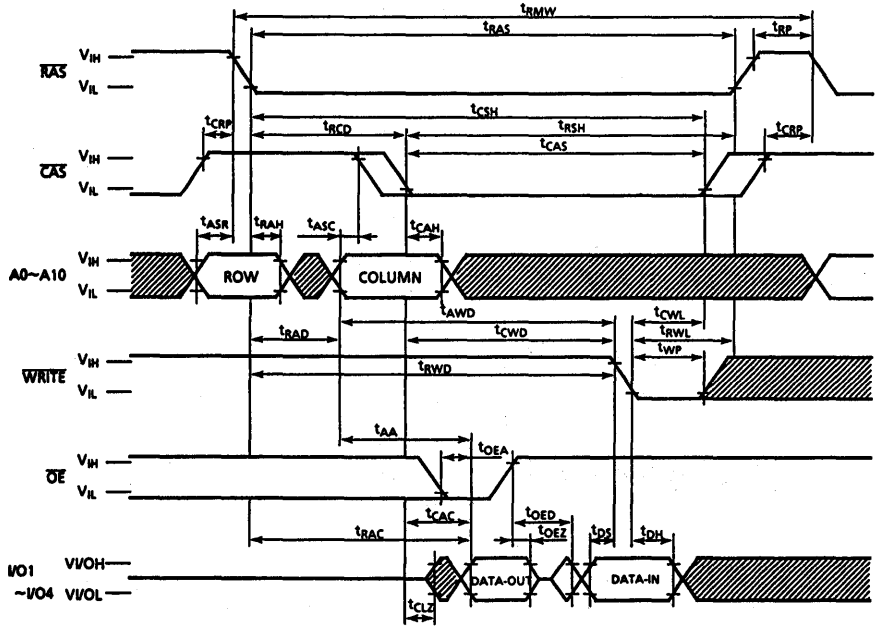
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

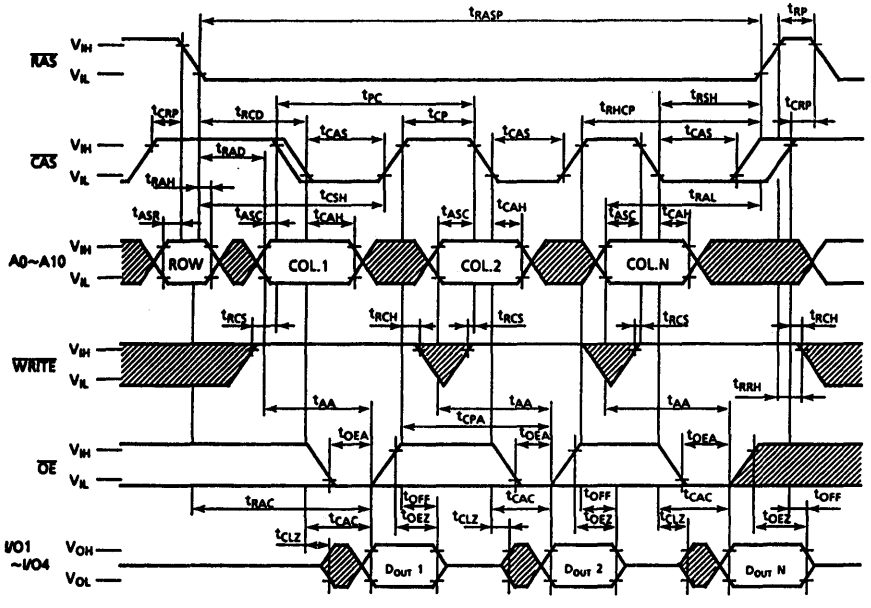
▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



▨ : "H" or "L"

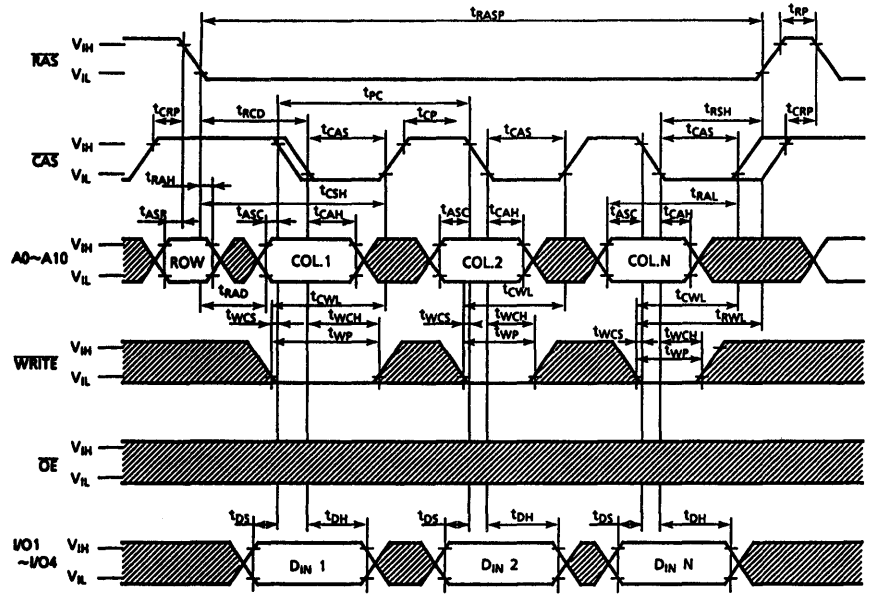
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

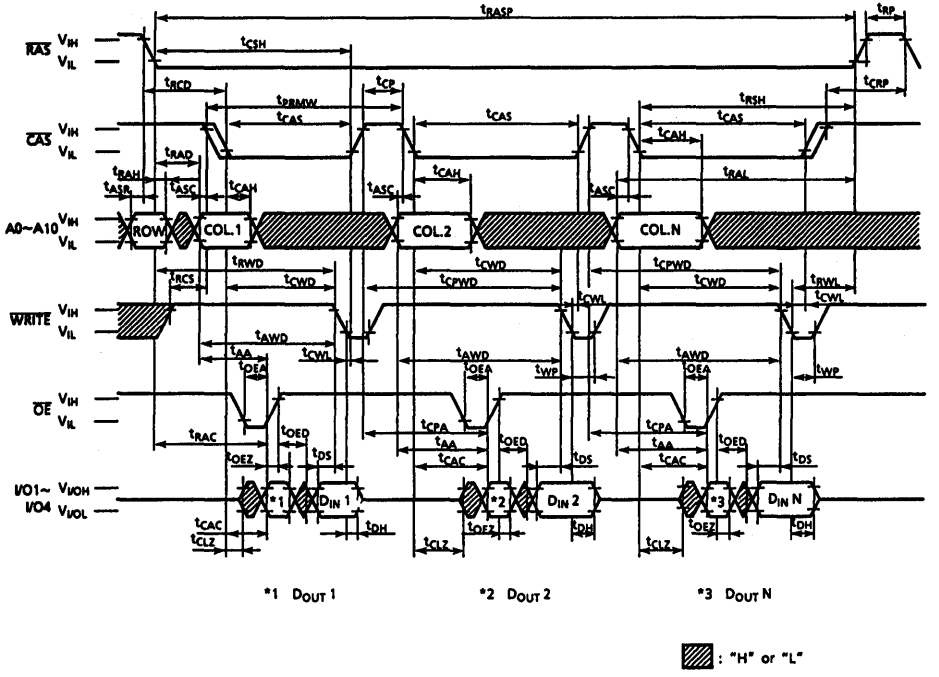
FAST PAGE MODE WRITE CYCLE



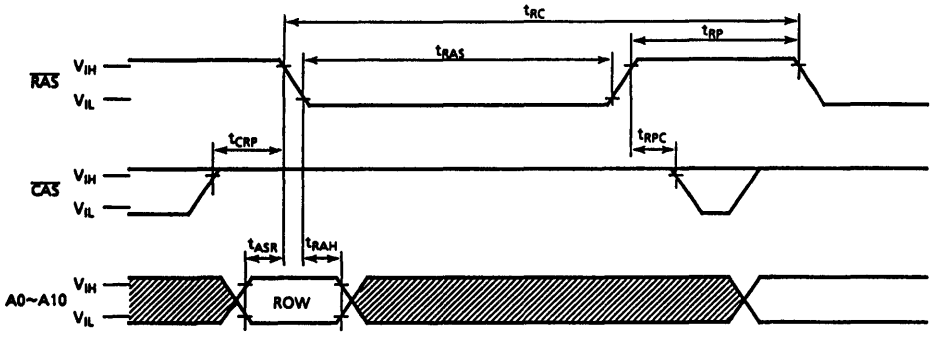
Note: D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



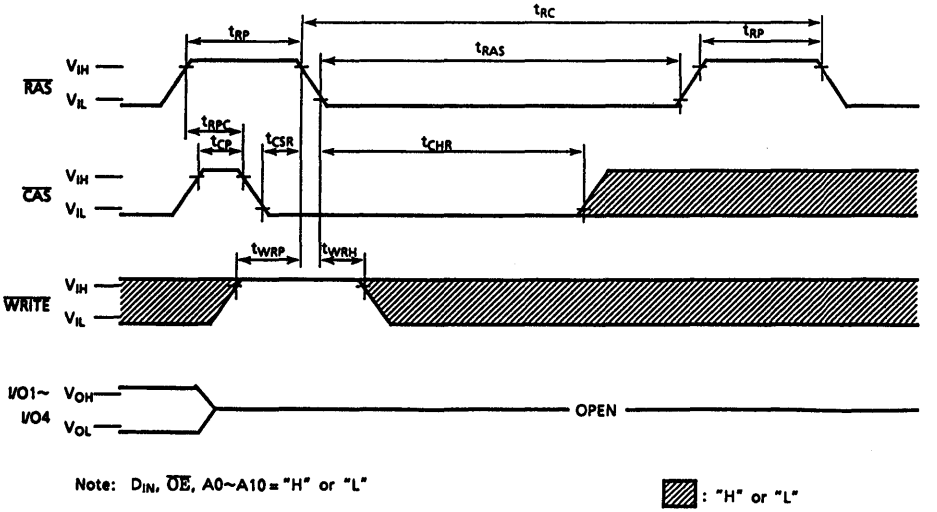
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

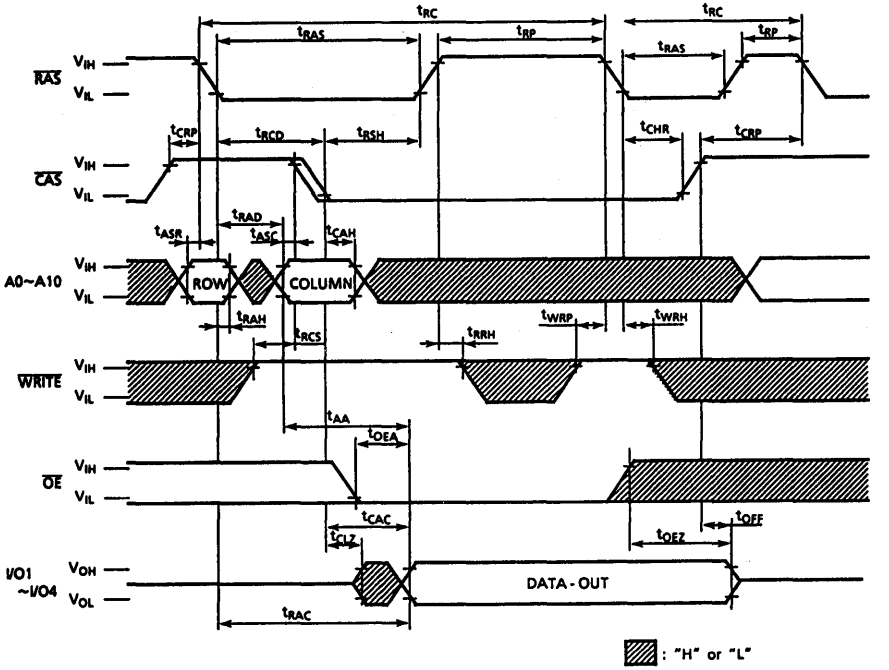
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A10 = "H" or "L"

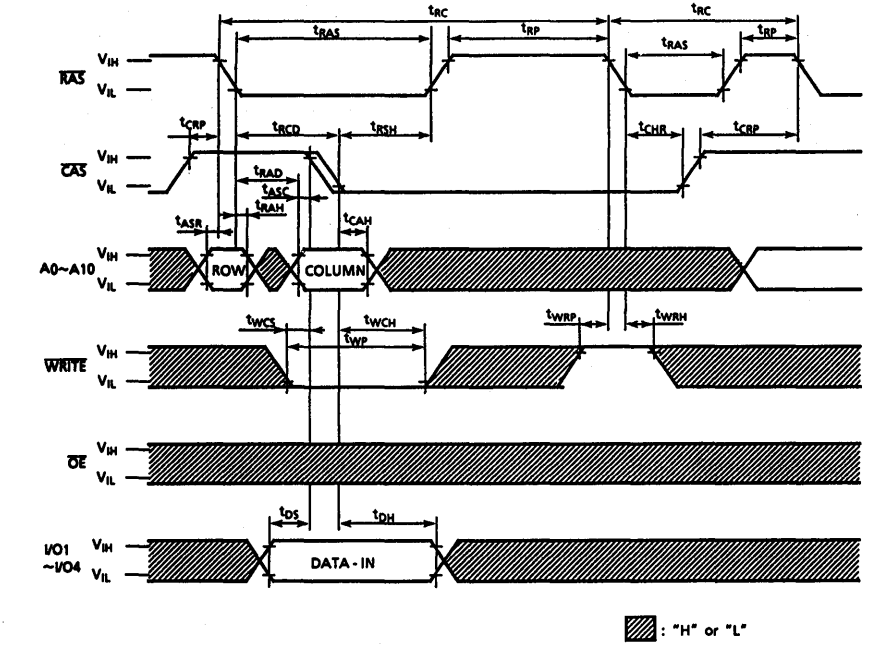
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)

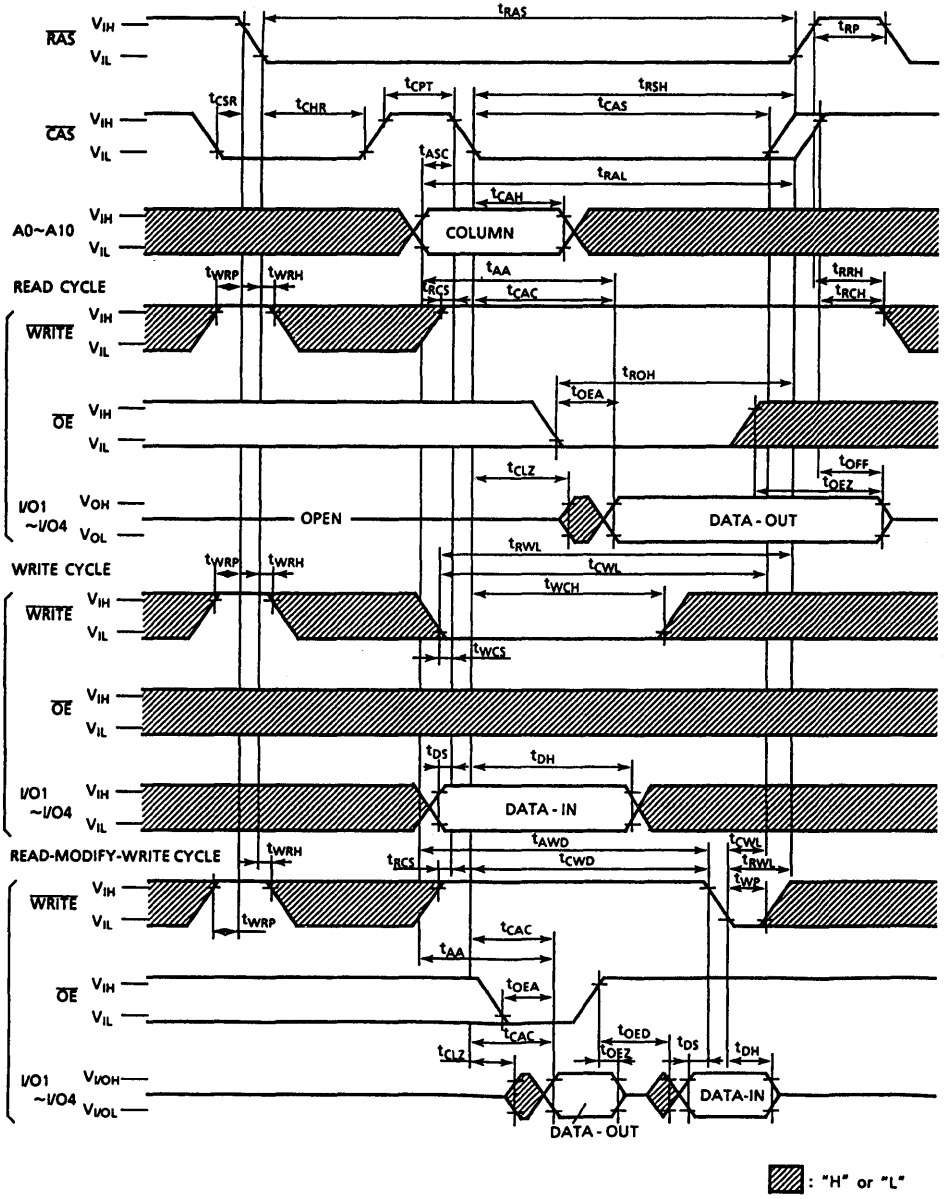


Note: D_{IN} = OPEN

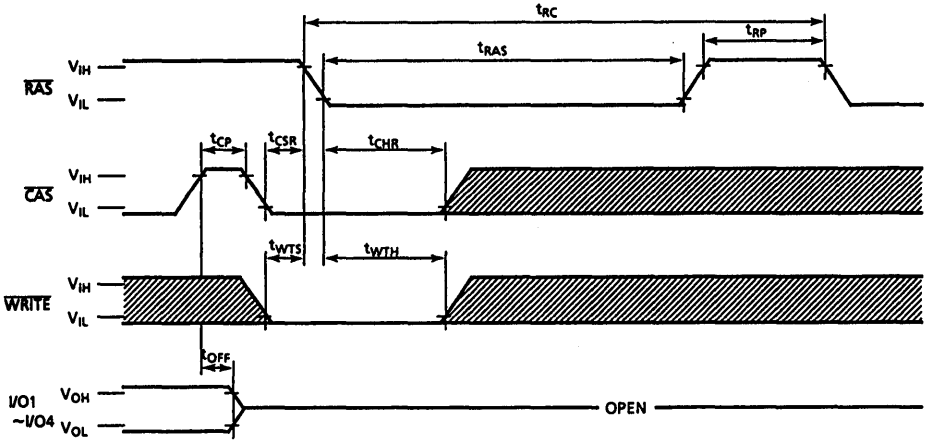
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



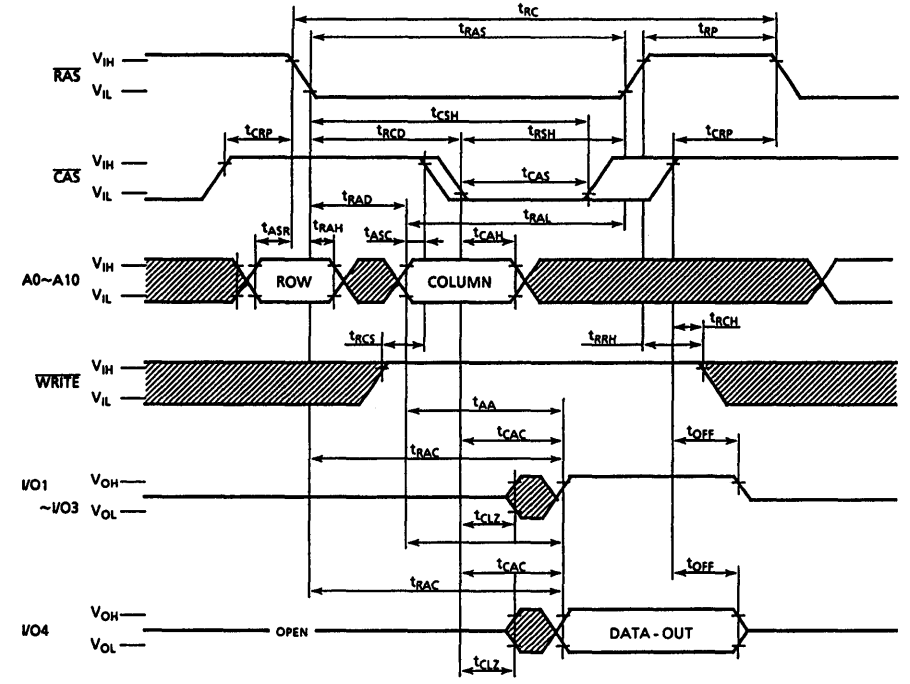
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A10 = "H" or "L"

▨: "H" or "L"

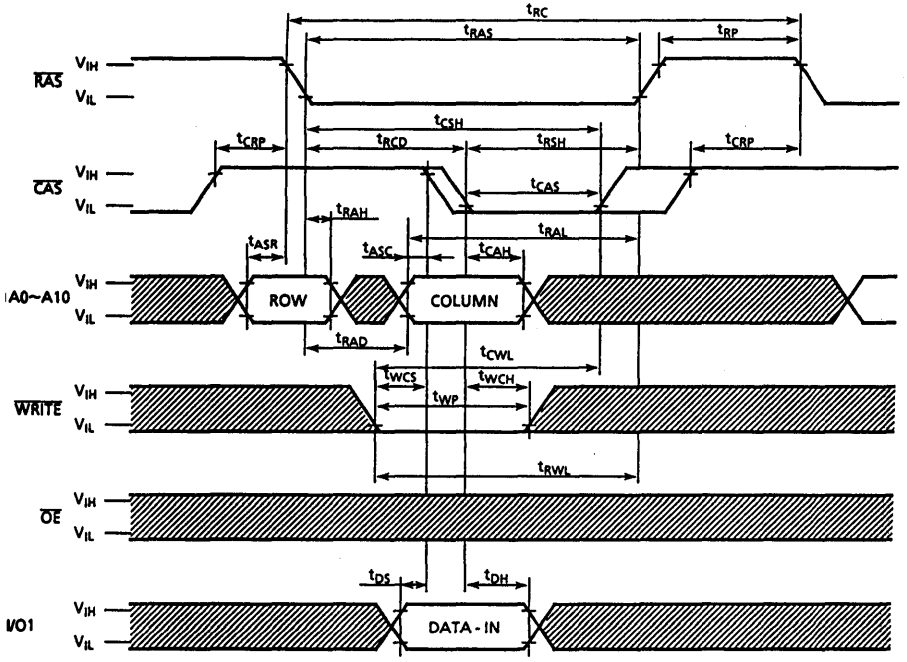
READ CYCLE IN THE TEST MODE



Note : $\overline{OE}$ = "L", D_{IN} = OPEN

▨: "H" or "L"

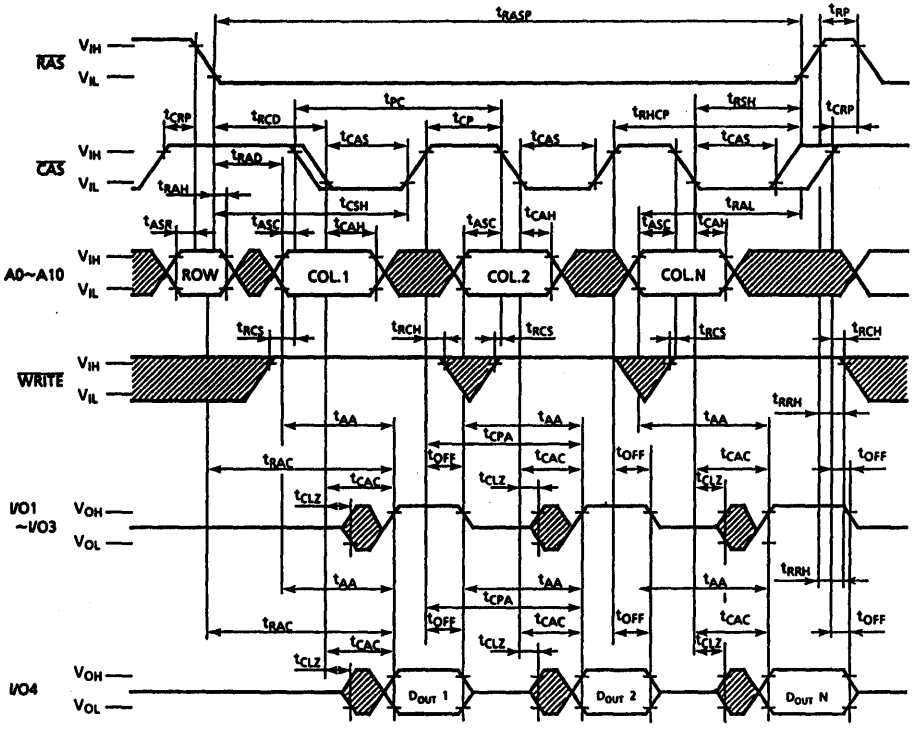
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L", D_{OUT} = OPEN

▨ : "H" or "I

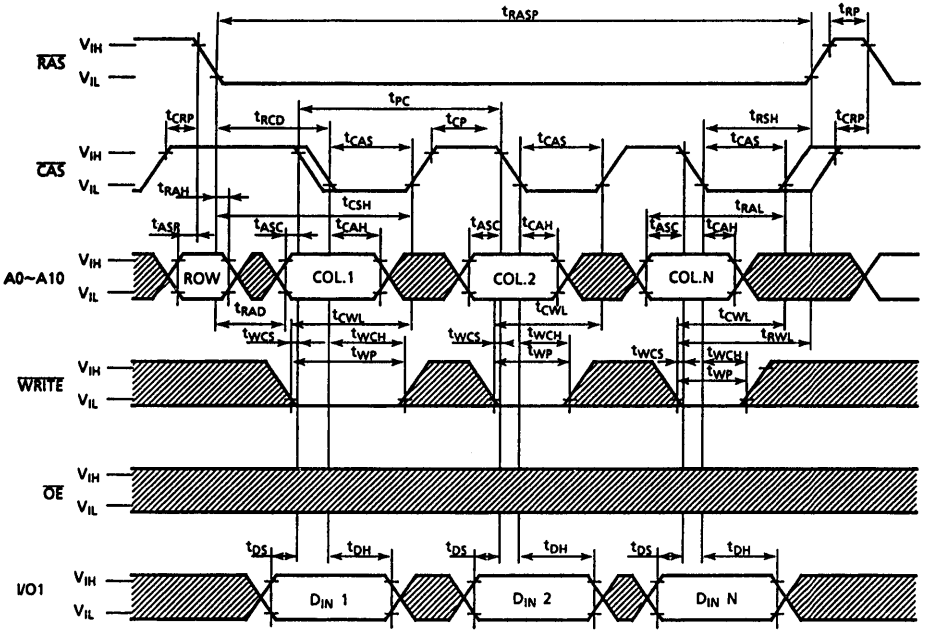
FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note : $\overline{OE}$="L", D_{IN}=OPEN

▨ : "H" or "L"

FAST PAGE MODE WRITE CYCLE IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L", D_{OUT} = OPEN

▨ : "H" or "L"

TEST MODE

The TC5117400J/Z/FT is the RAM organized 4,194,304 words by 4 bits; it is internally organized 1,048,576 words by 16 bits. In "Test Mode," data are written into 16 sectors in parallel by using only I/01. A1c, A0c are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s), the I/04 pin indicates a "1." If they were not equal, the I/04 pin would indicate a "0." I/01, I/02 and I/03 always indicate a "1" during test mode read cycle. Fig. 1 shows the block diagram of TC5117400J/Z/FT. In "Test Mode," the 4Mx4 DRAM can be tested as if it were a 1MX16 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode." And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "RAS Only Refresh Cycle" puts it back into "Normal Mode." In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/4 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

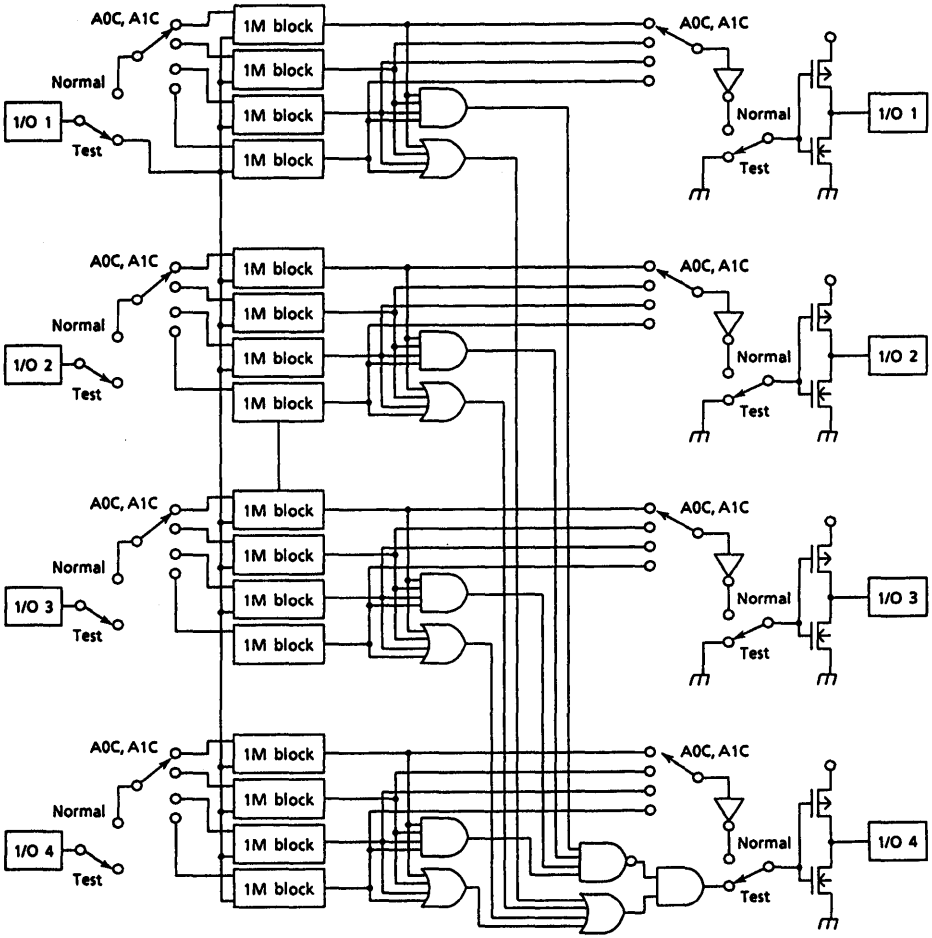


Figure 1

4,194,304 WORD X 4 BIT DYNAMIC RAM

DESCRIPTION

The TC5116400J/FT is the new generation dynamic RAM organized 4,194,304 word by 4 bit. The TC5116400J/FT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5116400J/FT to be packaged in a 28/24 pin plastic SOJ, and 28/24 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 4,194,304 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  495mW MAX .Operating
  (TC5116400J/FT-60)
  440mW MAX. Operating
  (TC5116400J/FT-70)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 4096 refresh cycles/64ms
- Package TC5116400J : SOJ28-P-400A
  TC5116400FT : TSOP28-P-400B

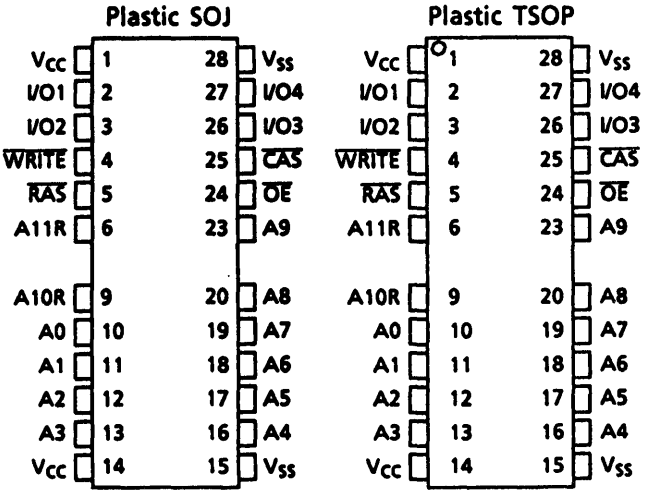
KEY PARAMETERS

ITEM		TC5116400J/FT	
		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

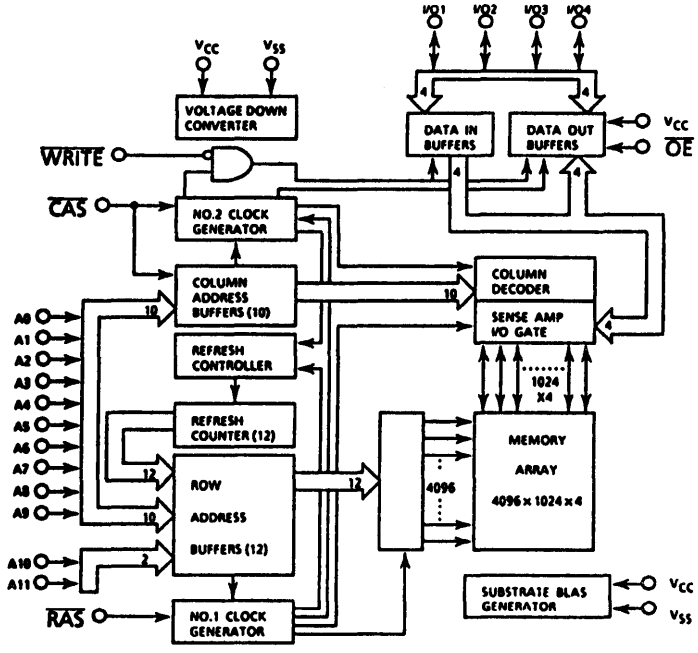
PIN NAME

A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	V_{CC}+0.5	V	2
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V	2

*-2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511640J/FT-60 TC511640J/FT-70	- -	90 80	mA	3,4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511640J/FT-60 TC511640J/FT-70	- - -	90 80	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling:t_{PC}=t_{PC} MIN.)	TC511640J/FT-60 TC511640J/FT-70	- - -	70 60	mA	3,4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC511640J/FT-60 TC511640J/FT-70	- - -	90 80	mA	3, 5
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤V_{CC}, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤V_{CC})		-10	10	μA	
V_{OH}	OUTPUT CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT CURRENT Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC5116400J/FT				UNIT	NOTES
		-60		-70			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	ns	
t_{RMW}	Read-Modify-Write Cycle	155	-	180	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	85	-	95	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC5116400J/FTL				UNIT	NOTES
		-60		-70			
		MIN	MAX	MIN	MAX		
t_{WCH}	Write CommandHold Time	10	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	10	-	15	-	ns	12
t_{REF}	Refresh Period	-	64	-	64	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	40	-	45	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	-	95	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	55	-	60	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	60	-	65	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	20	-	30	-	ns	
t_{ROH}	RAS Hold Time referenced to OE	10	-	10		ns	
t_{OEA}	OE Access TIme	-	15		20	ns	
t_{OED}	OE to Data Delay	15	-	15	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from OE	0	15	0	15	ns	10
t_{OEH}	OE Command Hold Time	15	-	15	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC5116400J/FTL				UNIT	NOTES
		-60		-70			
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold	40	-	45	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead	35	-	40	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20		25	ns	
t_{RAL}	$\overline{OE}$ Command Hold Time	30	-	20	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A11)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input Capacitance (I/O1~I/O4)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

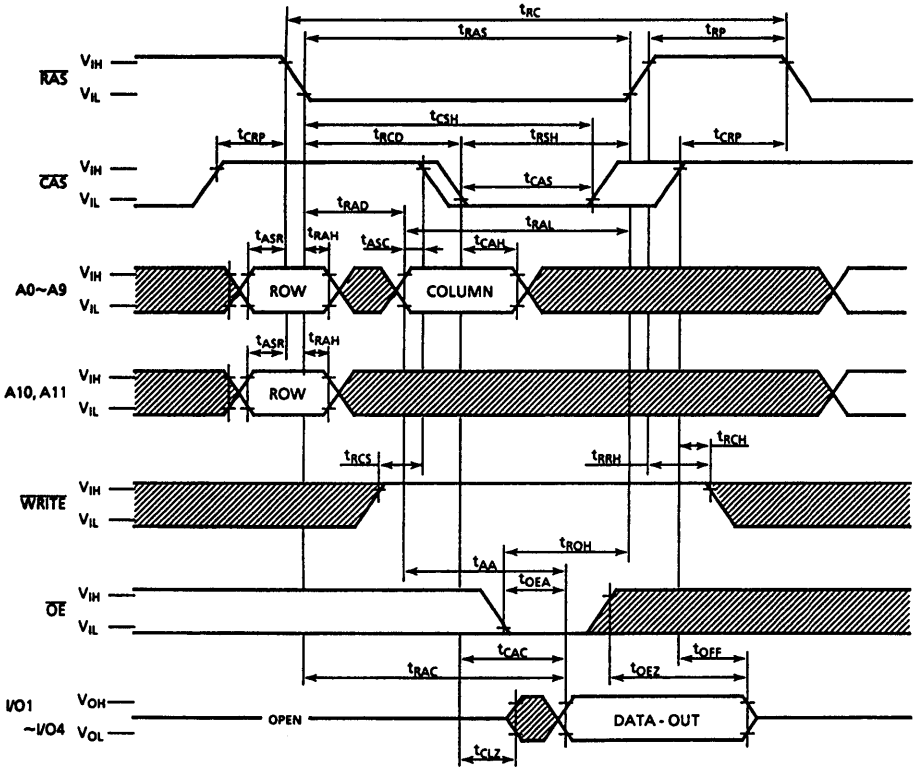
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the date sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWP} > t_{CPWDD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

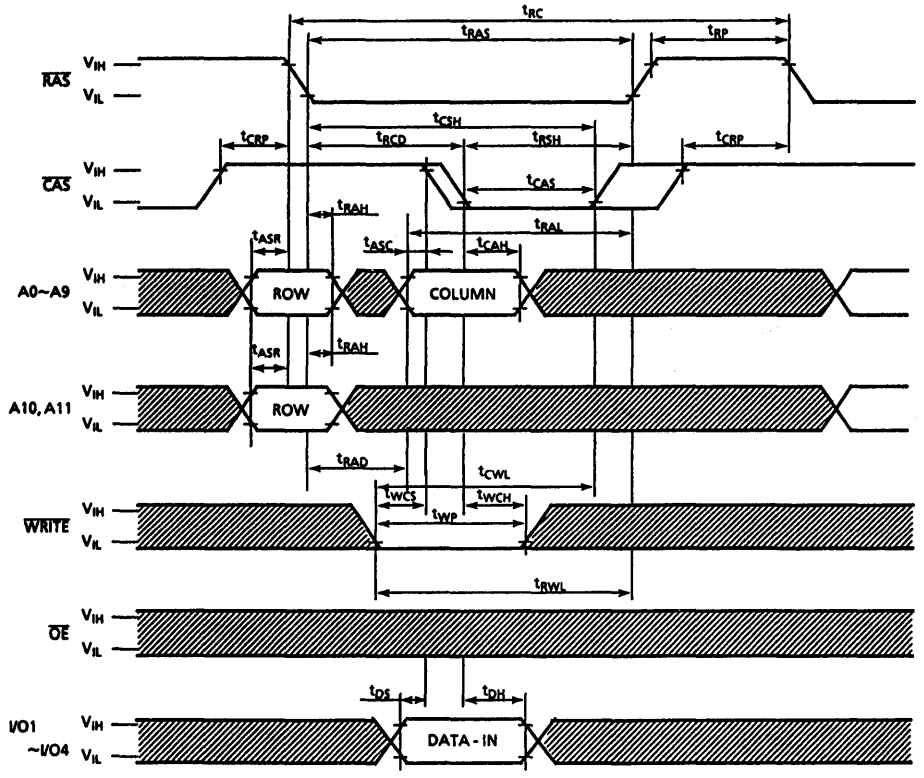
READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

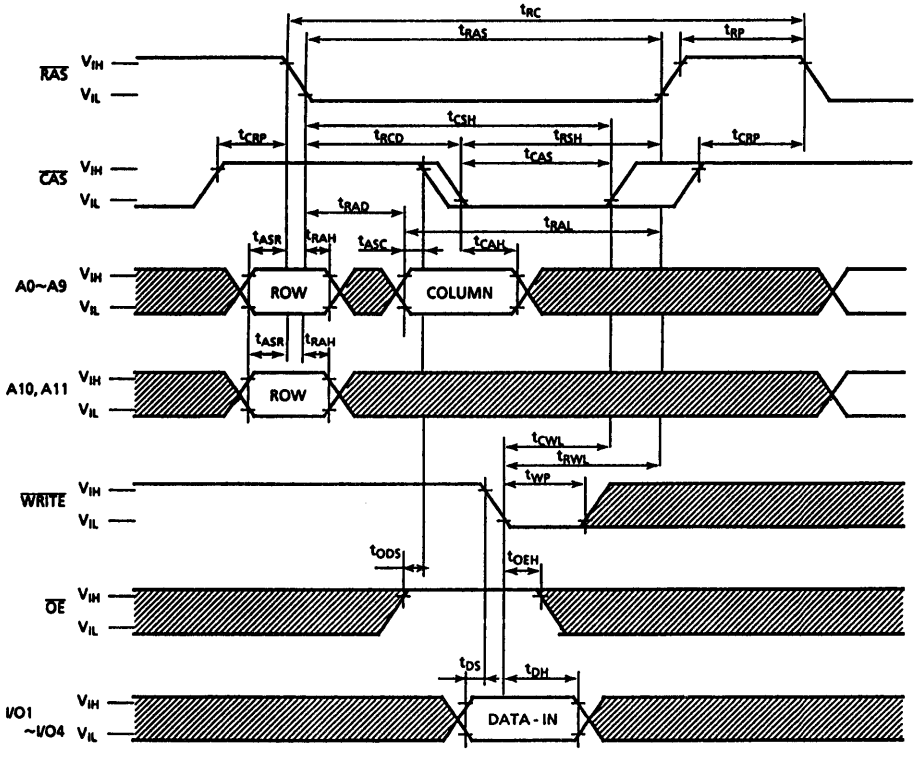
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

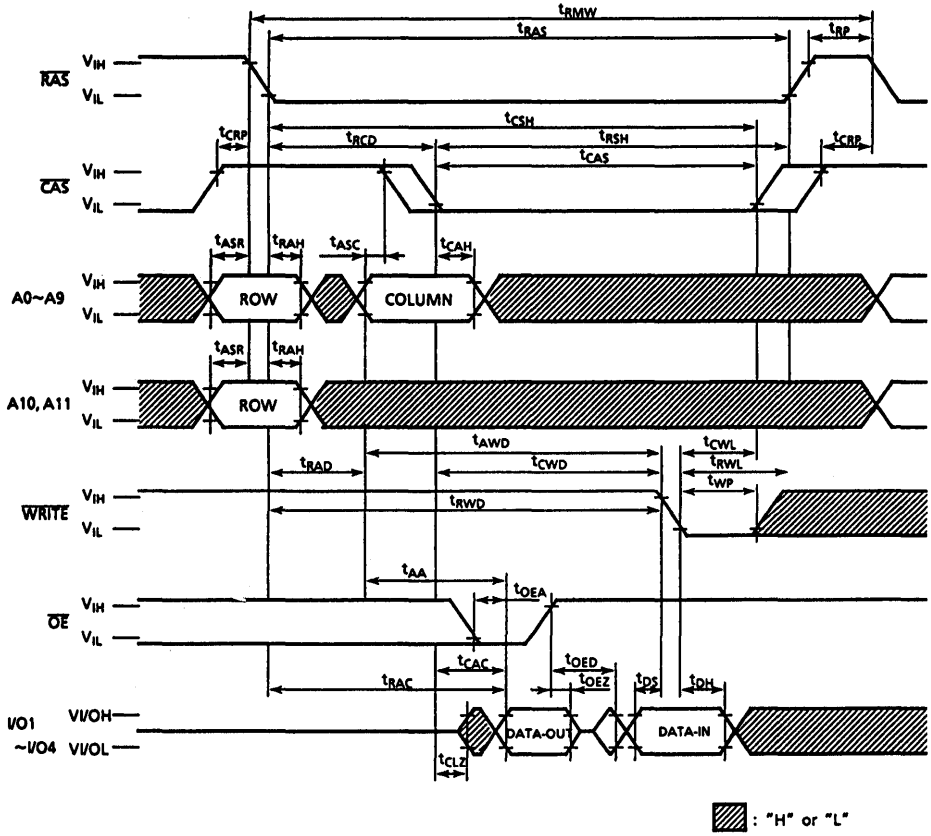
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



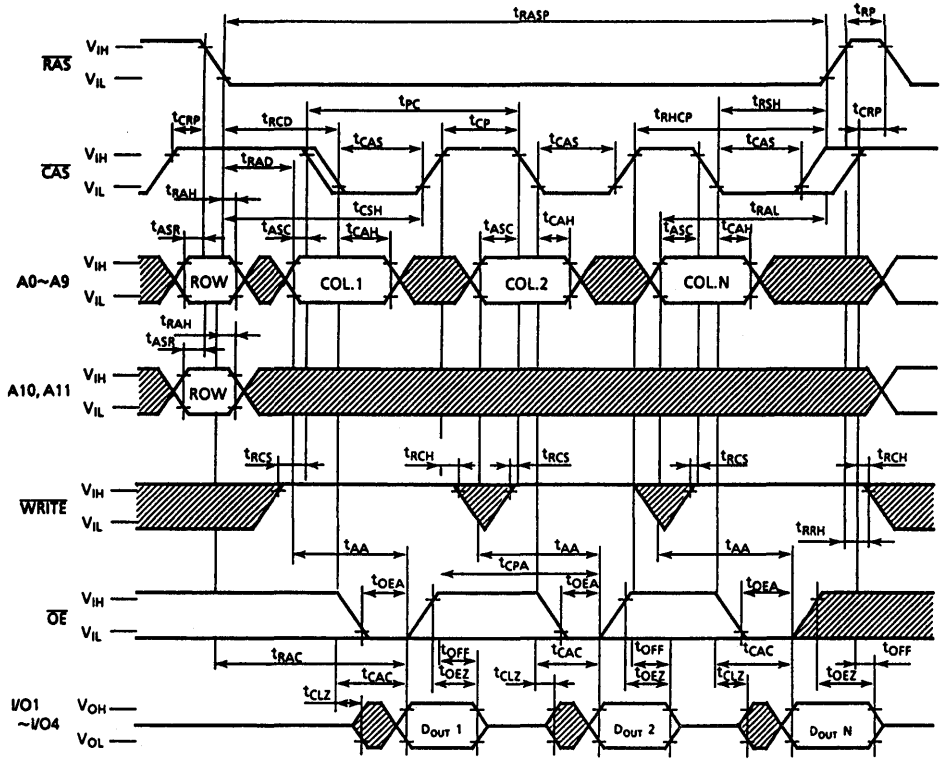
Note: D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



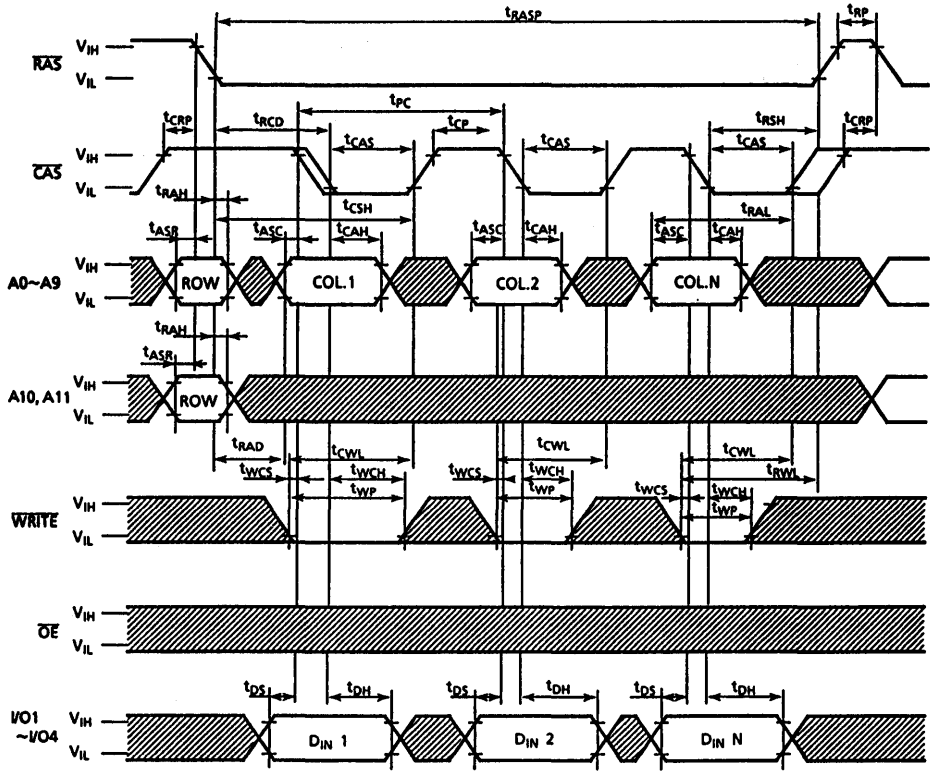
FAST PAGE MODE READ CYCLE



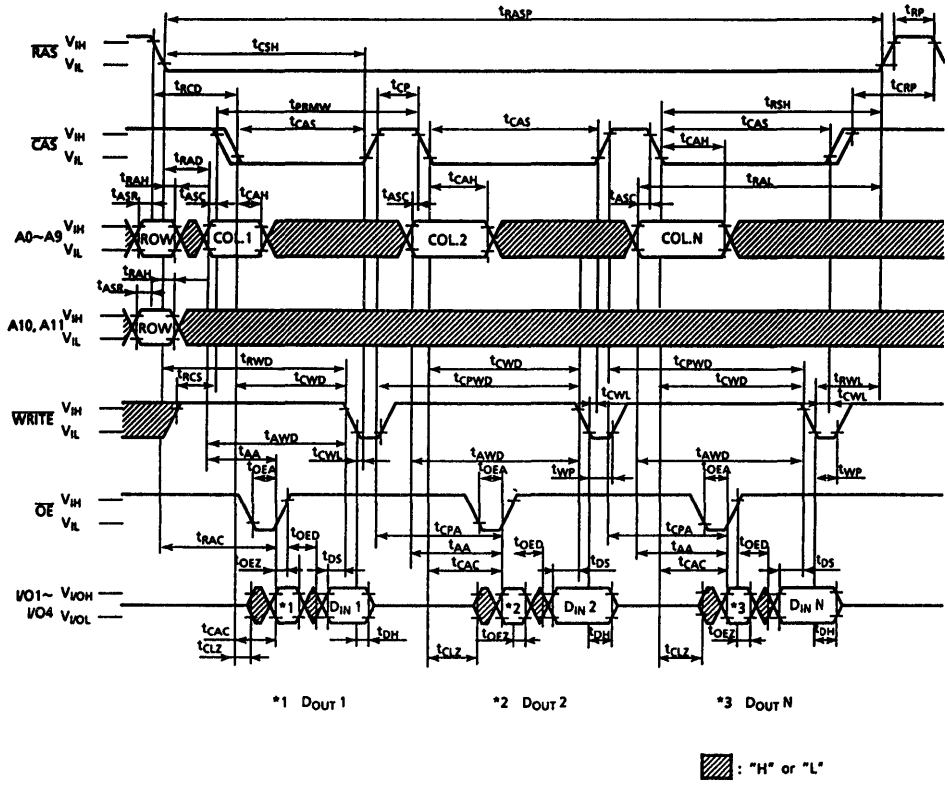
Note: D_{IN} = OPEN

▨ : "H" or "L"

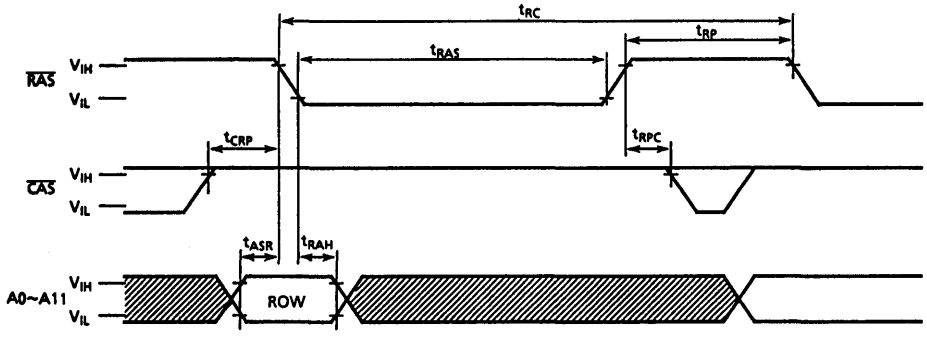
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



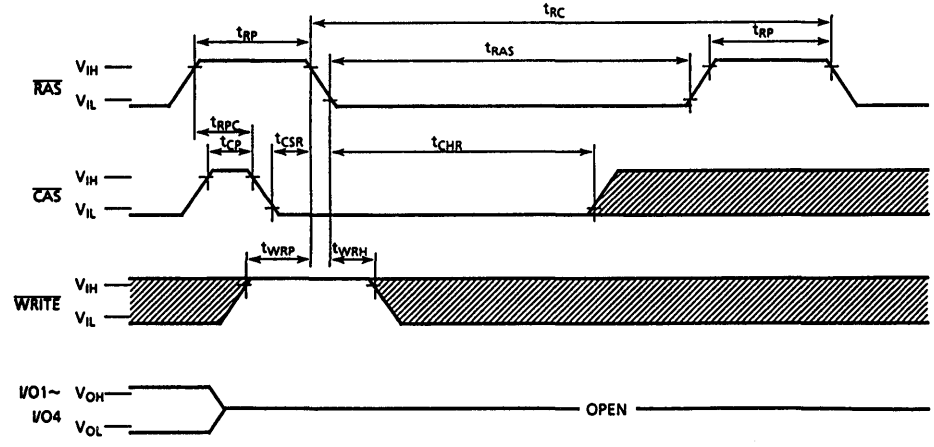
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

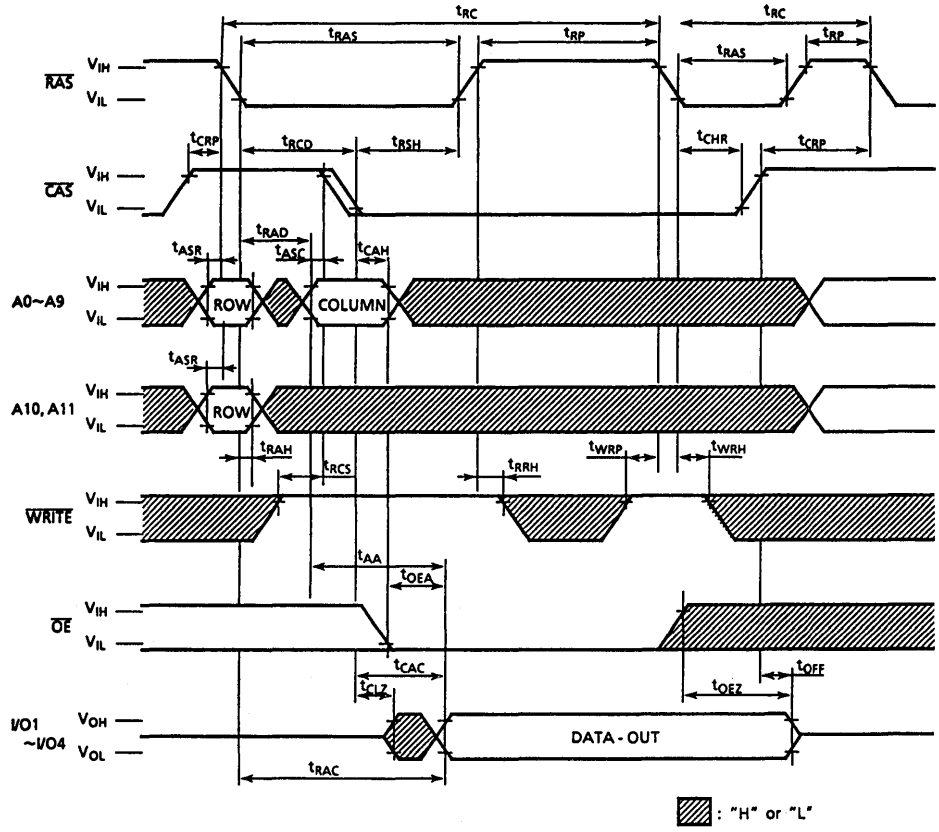
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A11 = "H" or "L"

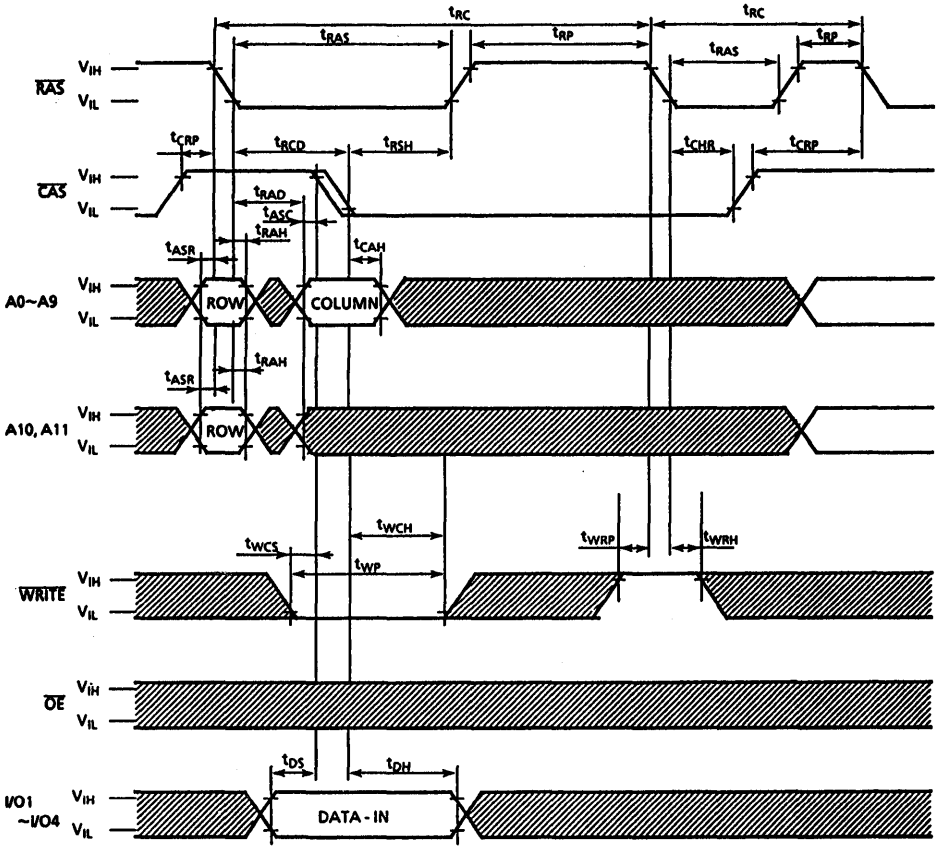
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

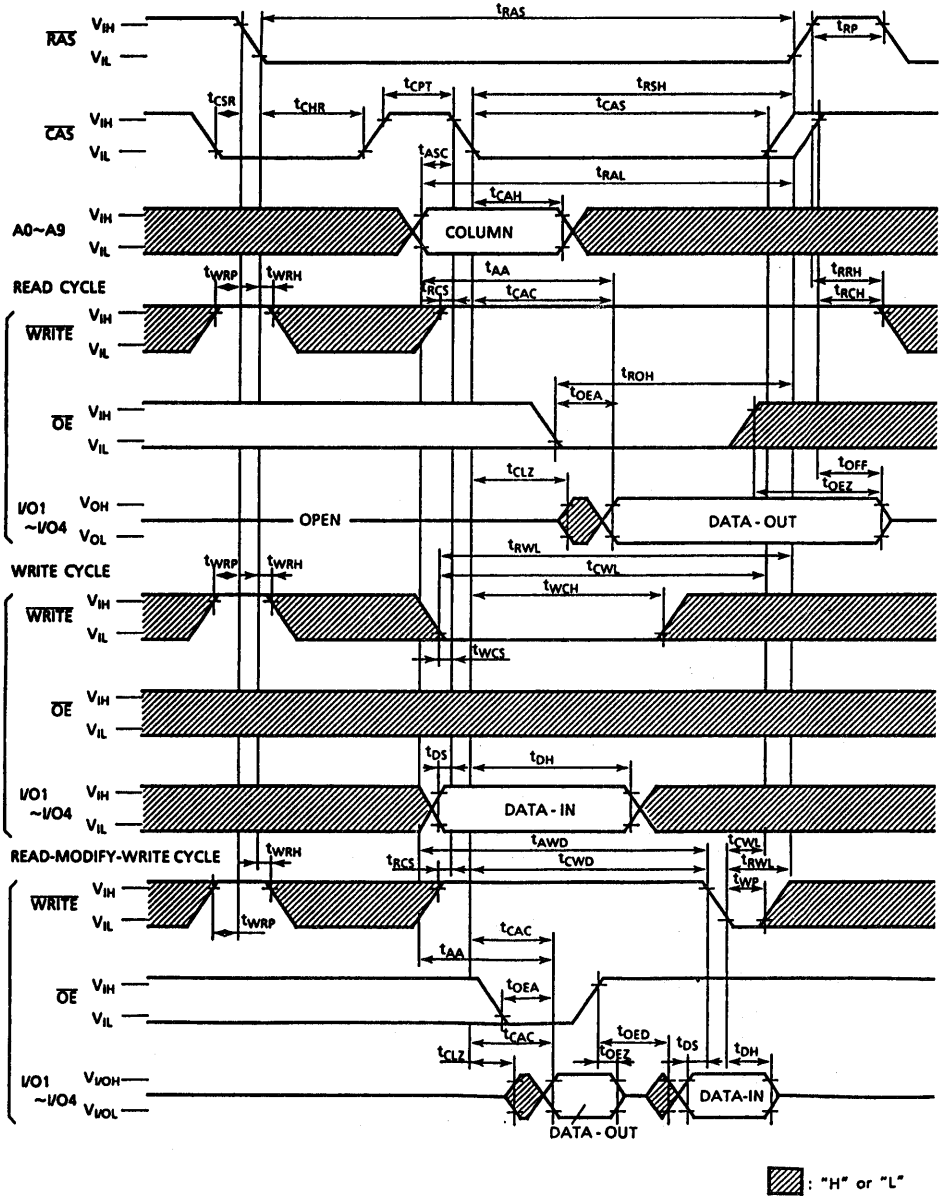
HIDDEN REFRESH CYCLE (WRITE)



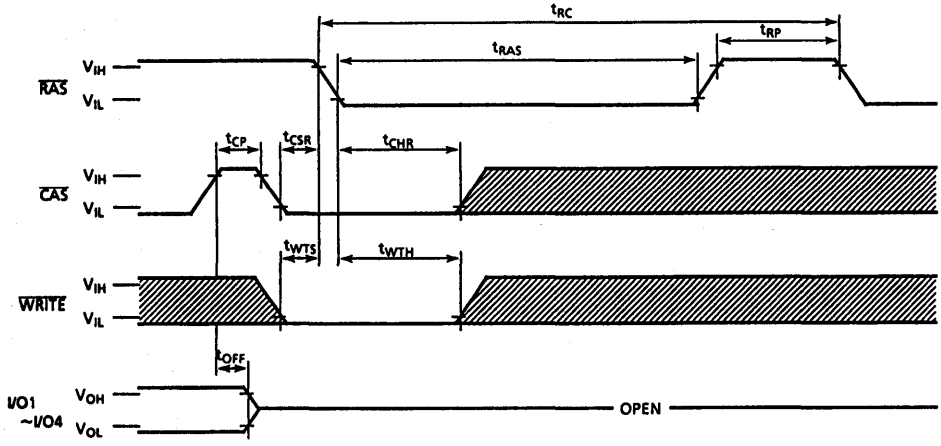
Note: D_{OUT} = OPEN

▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



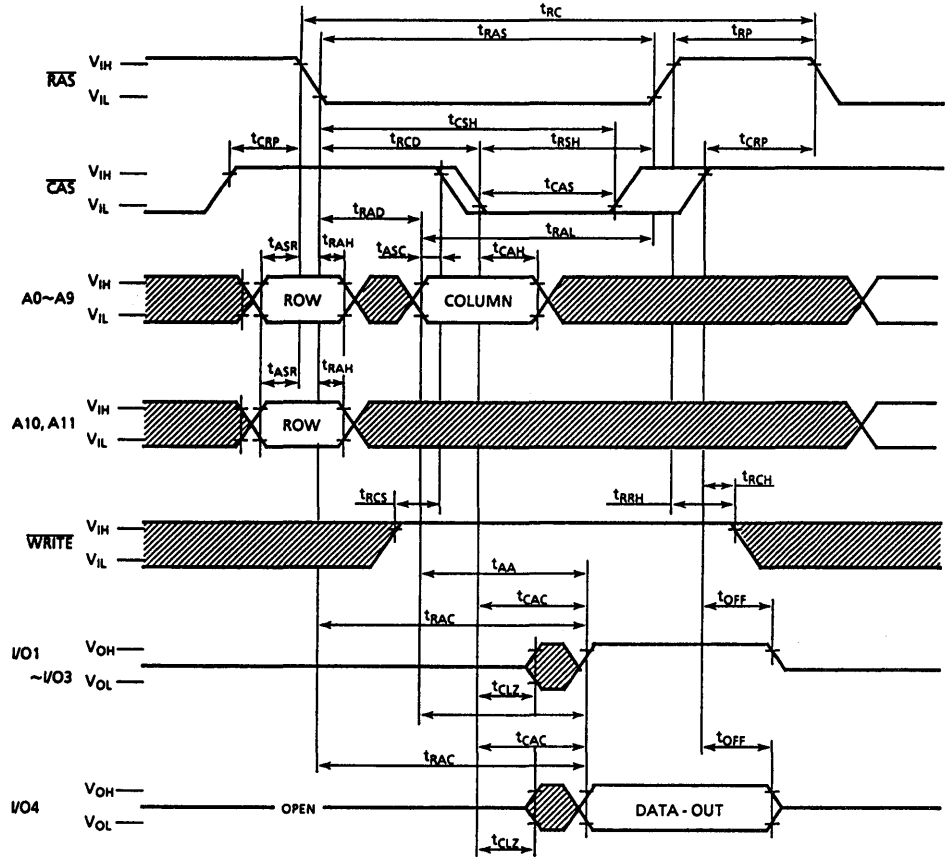
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



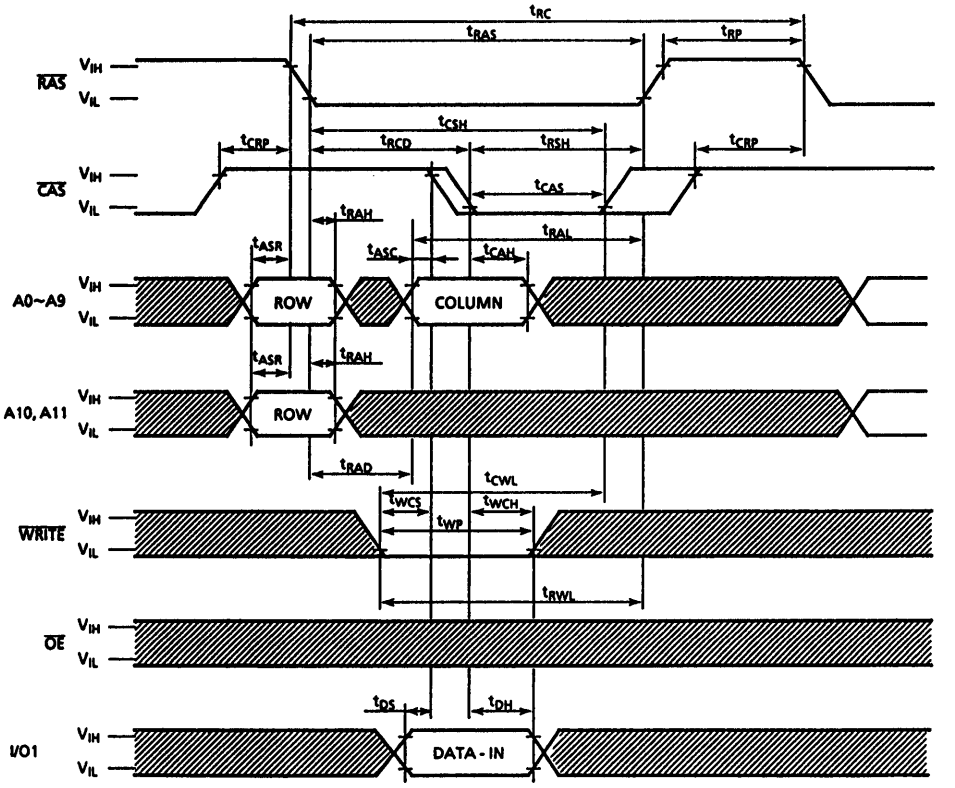
Note: D_{IN}, $\overline{OE}$, A0~A11 = "H" or "L"

▨ : "H" or "L"

READ CYCLE IN THE TEST MODE



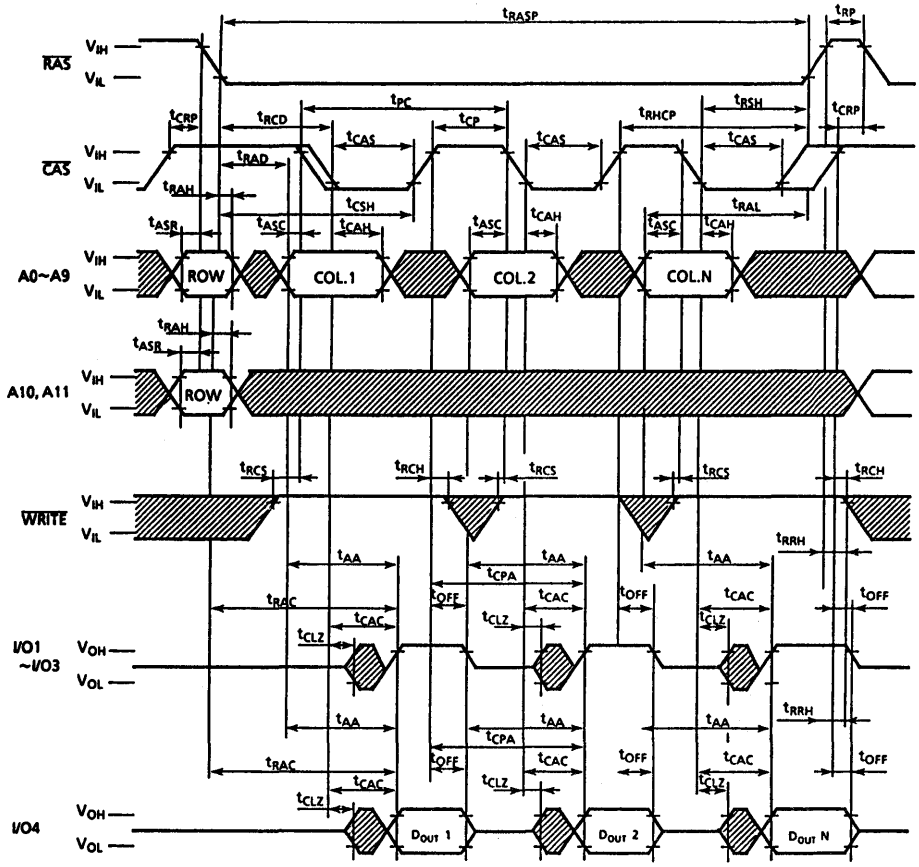
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L" , D_{OUT} = OPEN

▨ : "H" or "L"

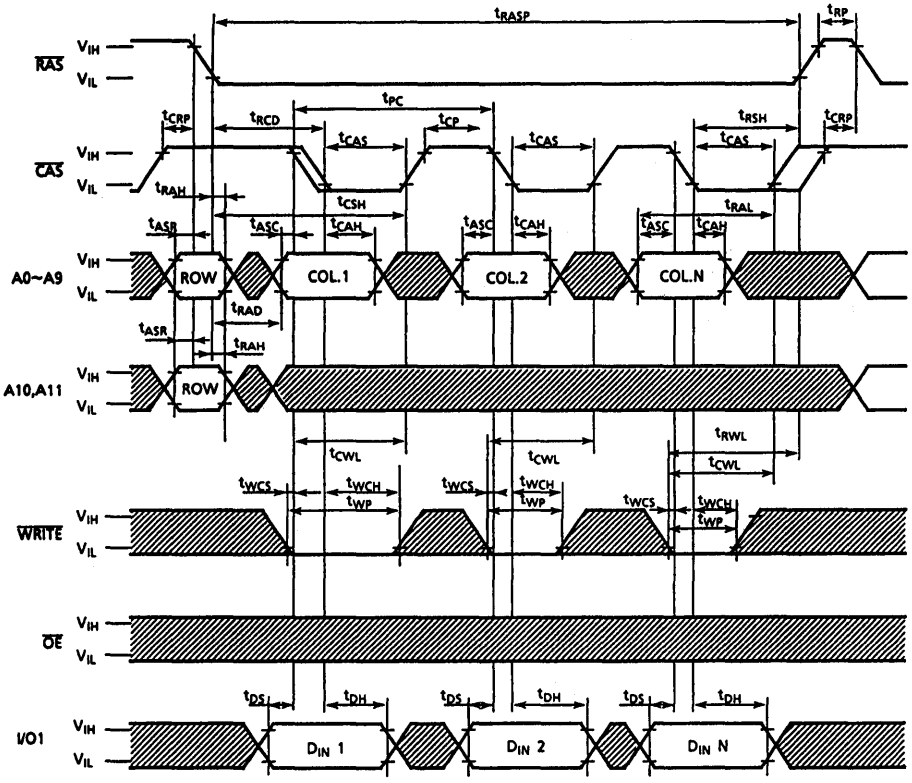
FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note : $\overline{OE}$="L" , D_{IN}=OPEN

▨ : "H" or "L"

FAST PAGE MODE WRITE CYCLE IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L" , D_{OUT} = OPEN

TEST MODE

The TC5116400J/FT is the RAM organized 4,194,304 words by 4 bits, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel by using only I/IO. A1c, A0c are not used. If, upon reading, 16 bits equal (all "1"s or "0"s), the IIO4 pin indicates a"1". If they were not equal, the I/O4 pin would indicate a "0". I/O1, I/O2 and I/O3 always indicate "1" during test mode read cycle. Fig. 1 shows the block diagram of TC5116400J/FT. In "Test Mode", the 4M5DRAM can be tested as if it were a 1M516DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/4 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

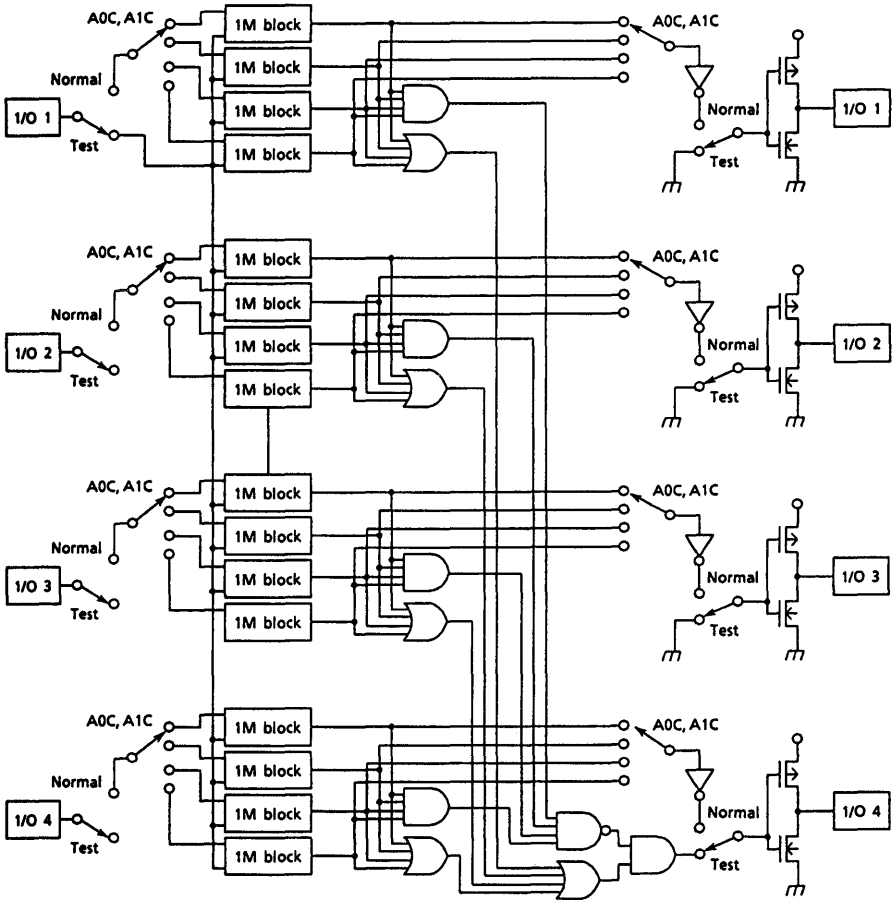


Figure 1

524,288 WORD X 8 BIT DYNAMIC RAM

DESCRIPTION

The TC514800AJ/AZ/AFT is the new generation dynamic RAM organized 524,288 word by 8 bit. The TC514800AJ/AZ/AFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514800AJ/AZ/AFT to be packaged in a standard 28 pin plastic SOJ, 28 pin plastic ZIP and 28 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL,

FEATURES

- 524,288 word by 8 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-ion V_{BB} generator
- Low Power
  578mW MAX .Operating
  (TC514800AJ/AZ/AFT-70)
  495mW Max. Operating
  TC514800AJ/AZ/AFT-80
  5.5mW Max. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package
  TC514800AJ :SOJ28-P-400
  TC514800AZ :ZIP28-P-400
  TC514800AFT :TSOP28-P-400

KEY PARAMETERS

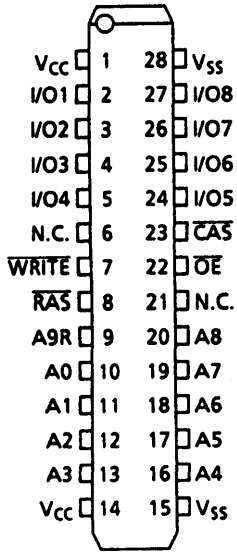
ITEM		TC514800AJ/AZ/AFT	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

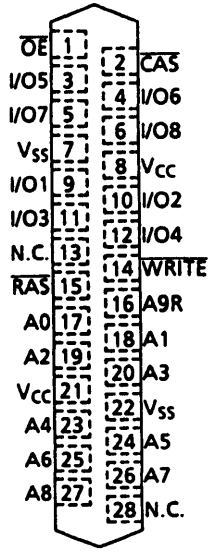
A0~A8 A9R	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Input/Output
V_{CC}	Power (+ 5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

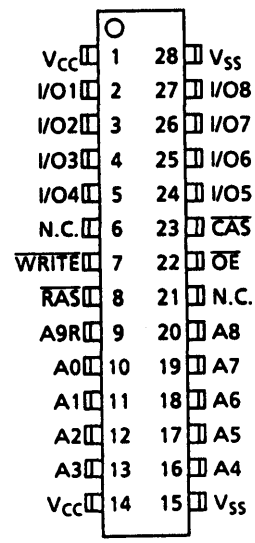
Plastic SOJ



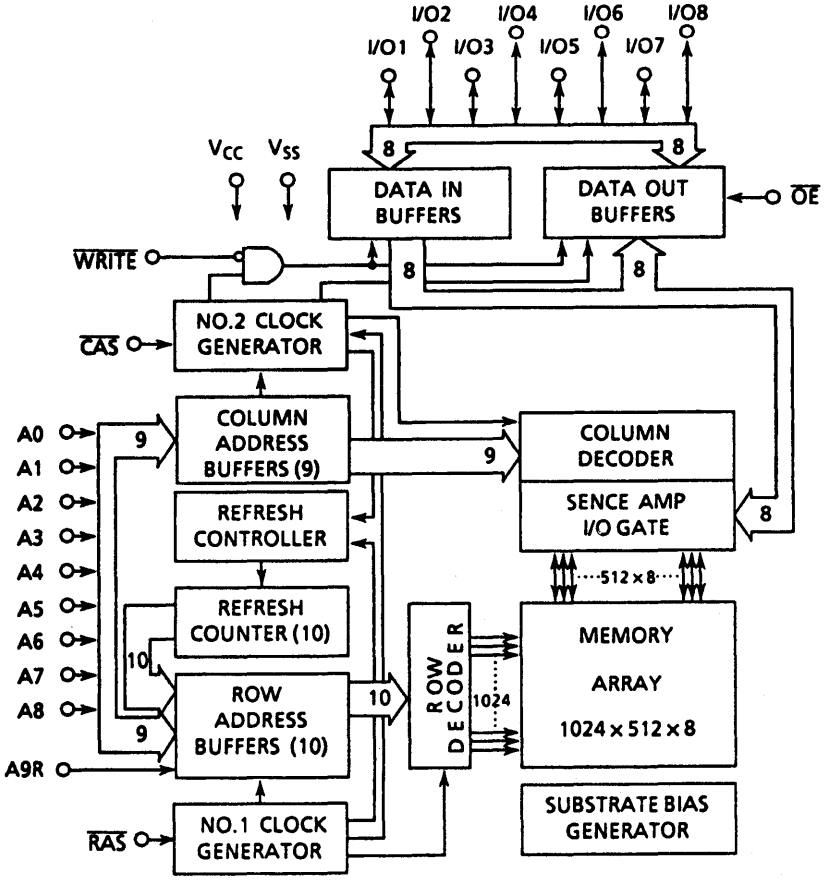
Plastic ZIP



Plastic TSOP
(Normal Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6..5	V	2
V_{IL}	Input Low Voltage (A0~A8,A9, $\overline{RAS}$, $\overline{CAS}$, WRITE, $\overline{OE}$)	-1.0*1	-	0.8	V	2
V_{IL}	Input Low Voltage ($\overline{I/O}$~$\overline{I/O9}$)	-0.5*2	-	0.8	V	2

*1 -2.5V at pulse width ≤ 20ns
*2 -2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514800AJ/AZ/AFT-70 TC514800AJ/AZ/AFT-80	- -	105 90	mA	3,4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514800AJ/AZ/AFT-70 TC514800AJ/AZ/AFT-80	- -	105 90	mA	3,5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC}MIN.)	TC514800AJ/AZ/AFT-70 TC514800AJ/AZ/AFT-80	- -	75 65	mA	3,4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$,Cycling: t_{RC}=t_{PC} MIN.)	TC514800AJ/AZ/AFT-70 TC514800AJ/AZ/AFT-80	- -	105 90	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	μA	
V_{OH}	OUTPUT CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT CURRENT Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC514800AJ/AZ/AFT				UNIT	NOTES
		-70		-80			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	ns	
t_{AR}	Column Address Hold Time	55	-	60	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold TIme	15	-	15	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514800AJ/AZ/AFT				UNIT	NOTES
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DHR}	Data Hold Time	15	-	15	-	ns	12
t_{DH}	Data Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	-	110	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	-	70	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	75	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to OE	10	-	10		ns	
t_{OEA}	$\overline{OE}$ Access TIme	-	20	0	20	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A8, A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$))	-	7	pF
C_O	Input Capacitance (I/O1~I/O8)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieveS the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

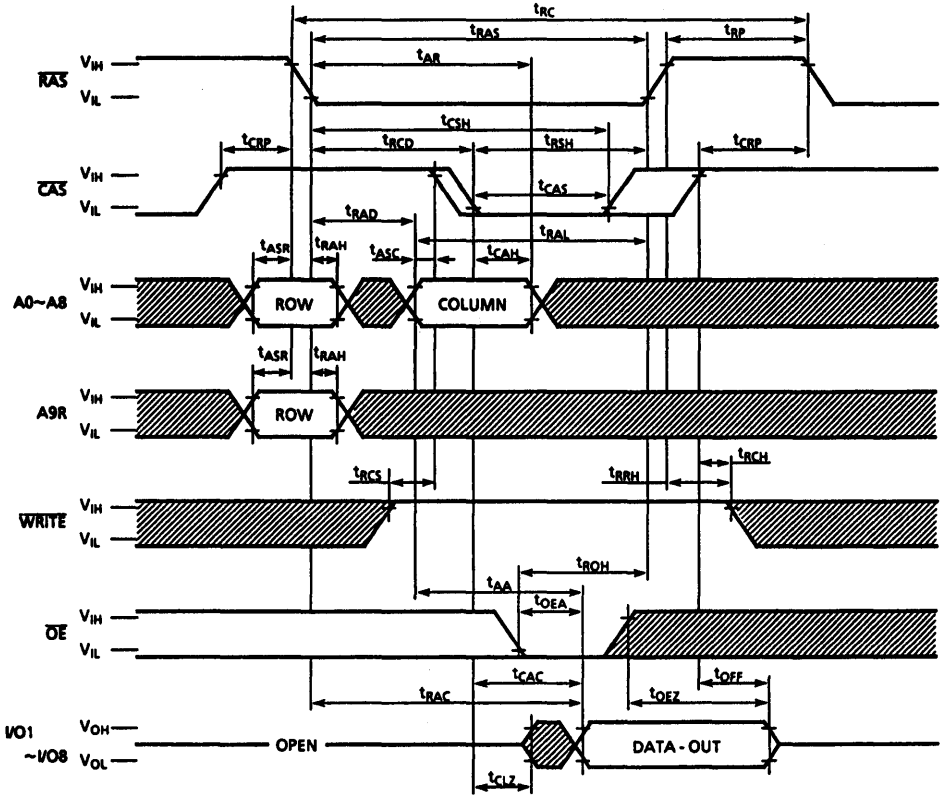
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the date sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

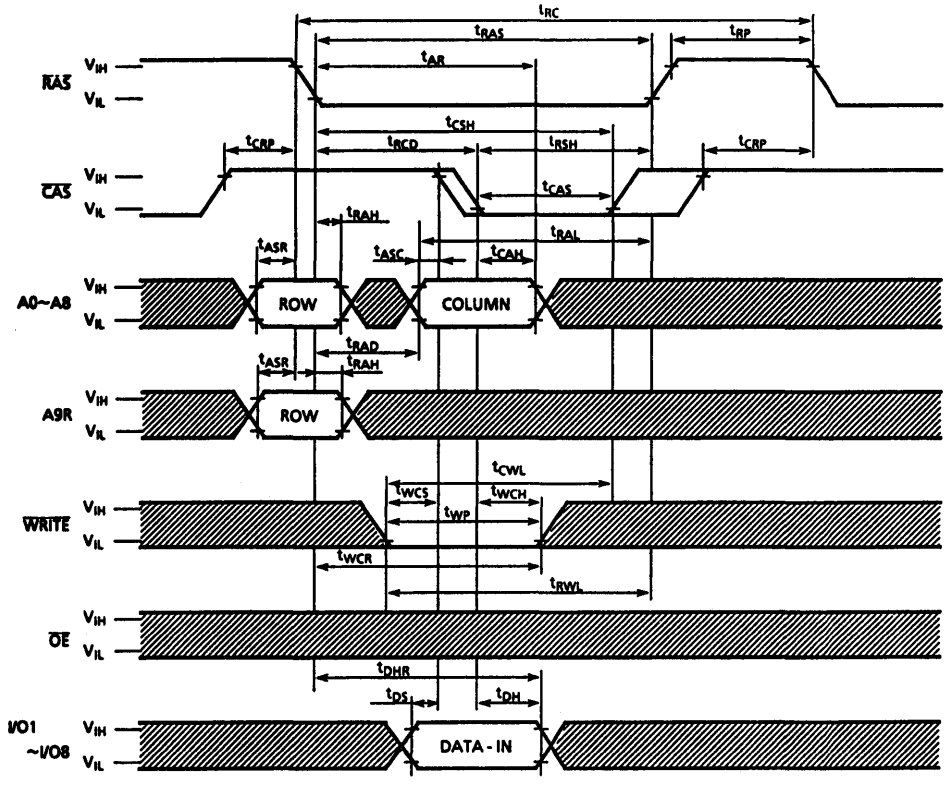
READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

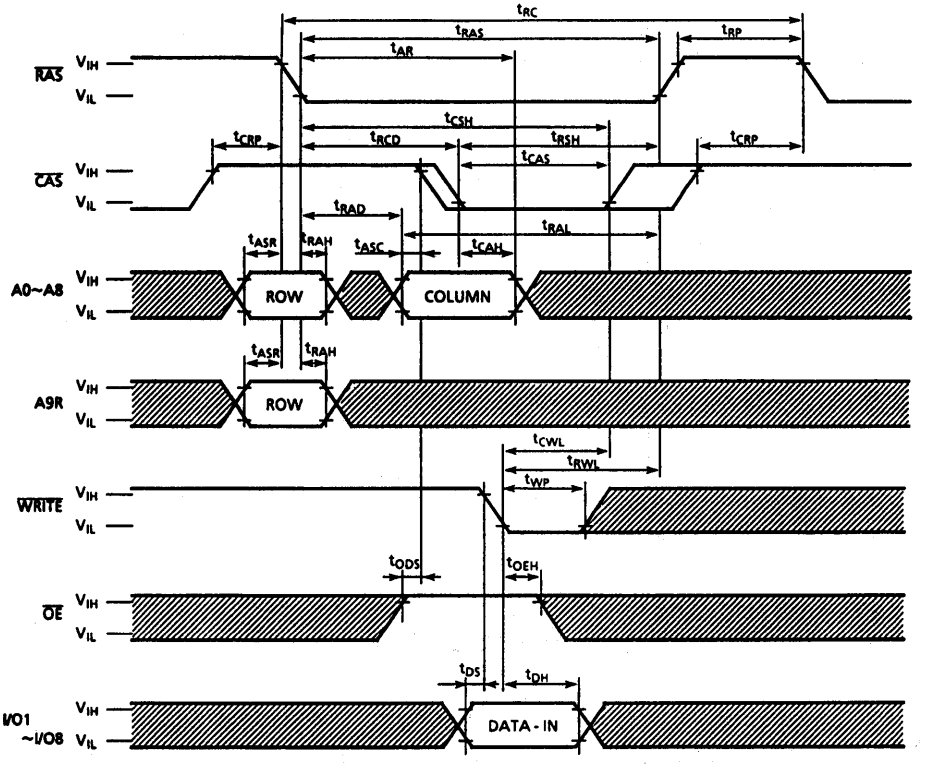
WRITE CYCLE (EARLY WRITE)



Note : D_{OUT} = OPEN

▨ : "H" or "L"

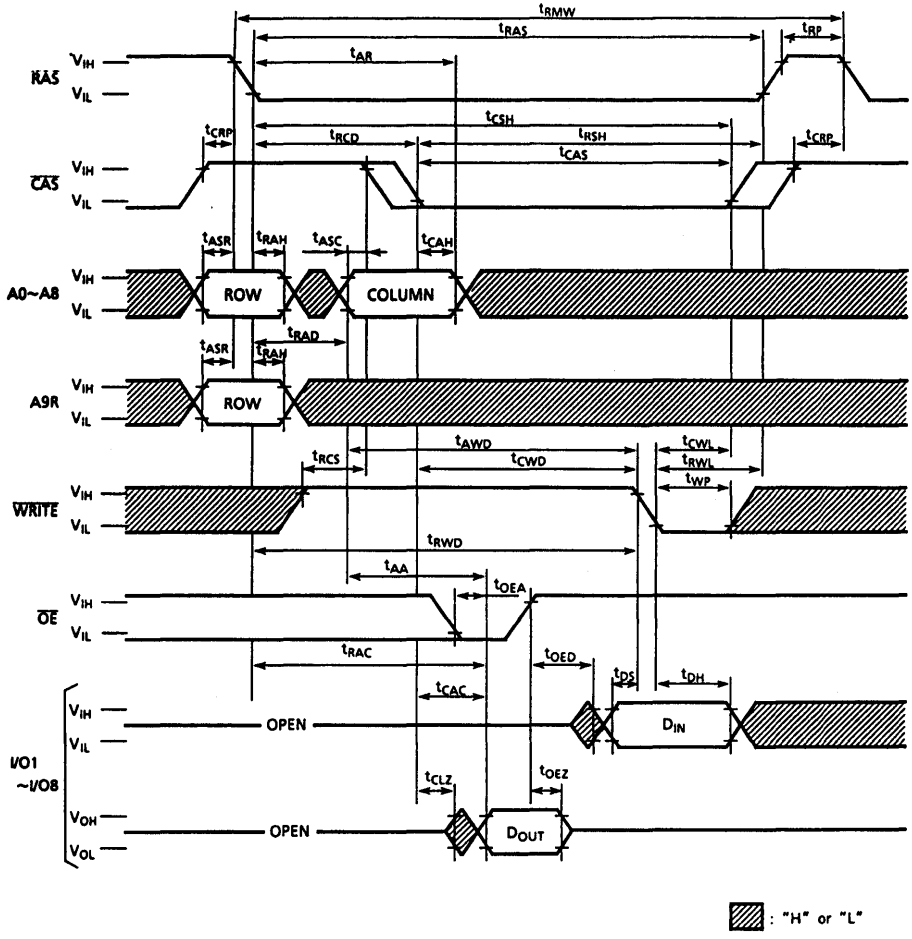
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



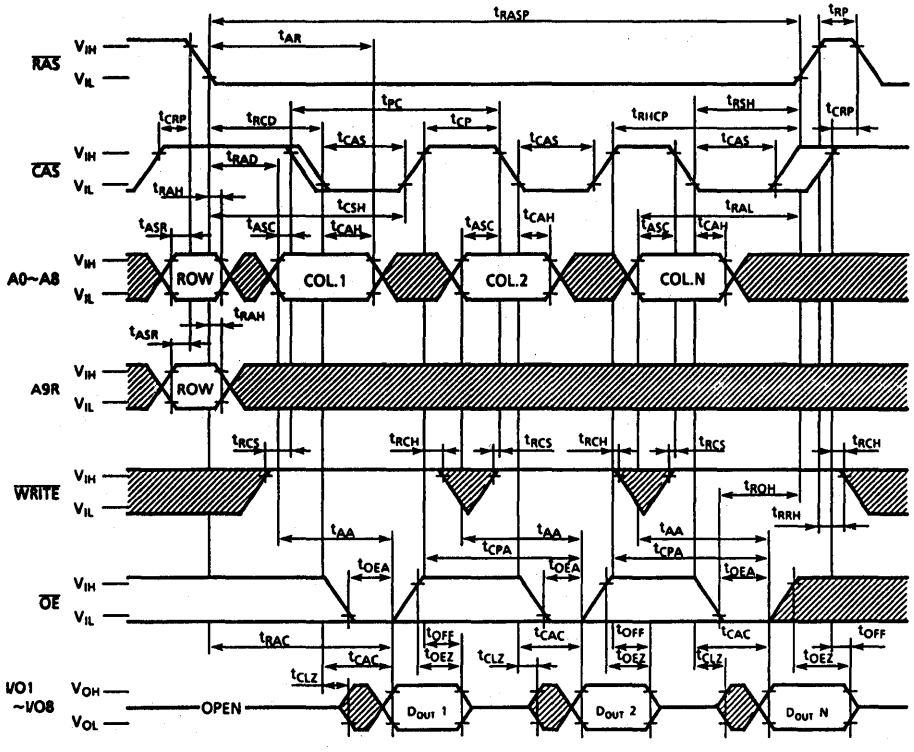
Note : D_{OUT} = OPEN

▨ : "H" or "L"

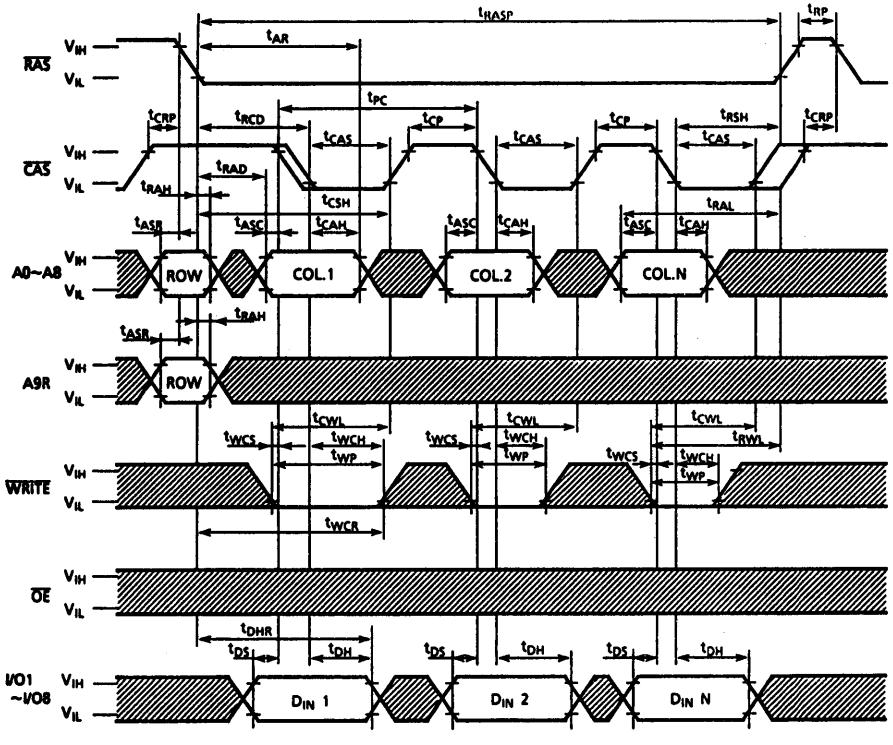
READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE



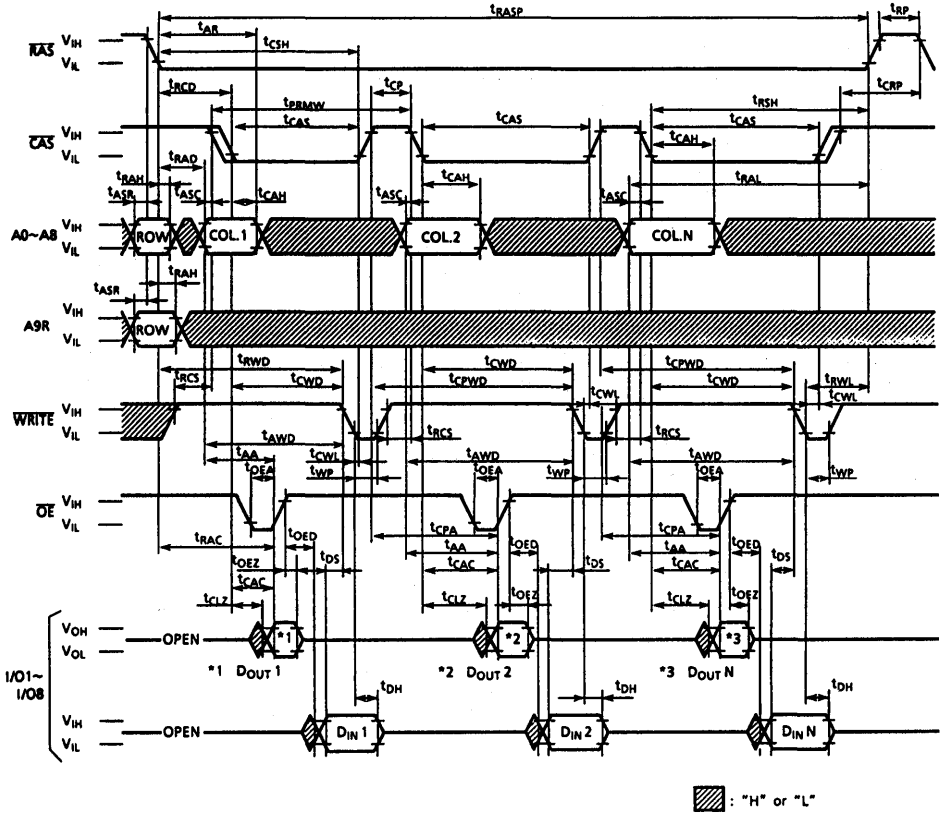
FAST PAGE MODE WRITE CYCLE



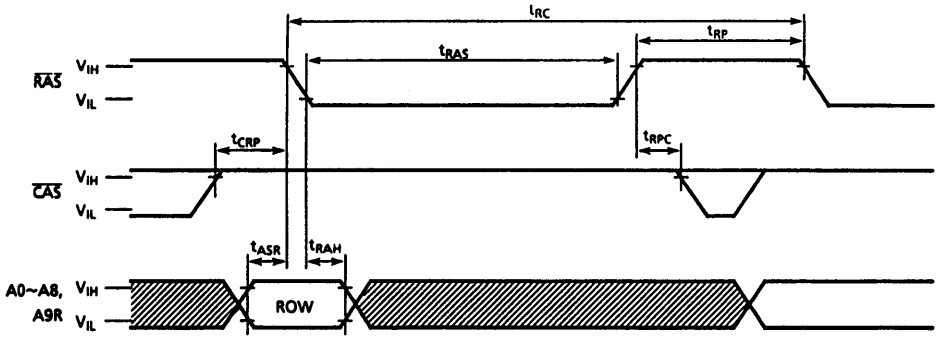
Note : D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



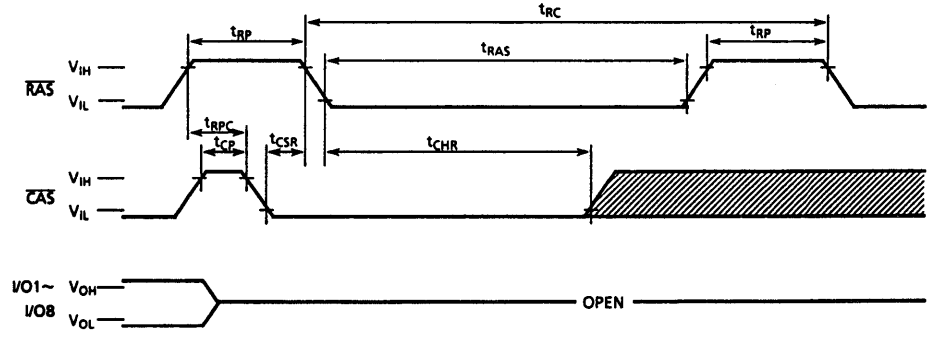
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$, D_{IN} = "H" or "L"
D_{OUT} = OPEN

▨ : "H" or "L"

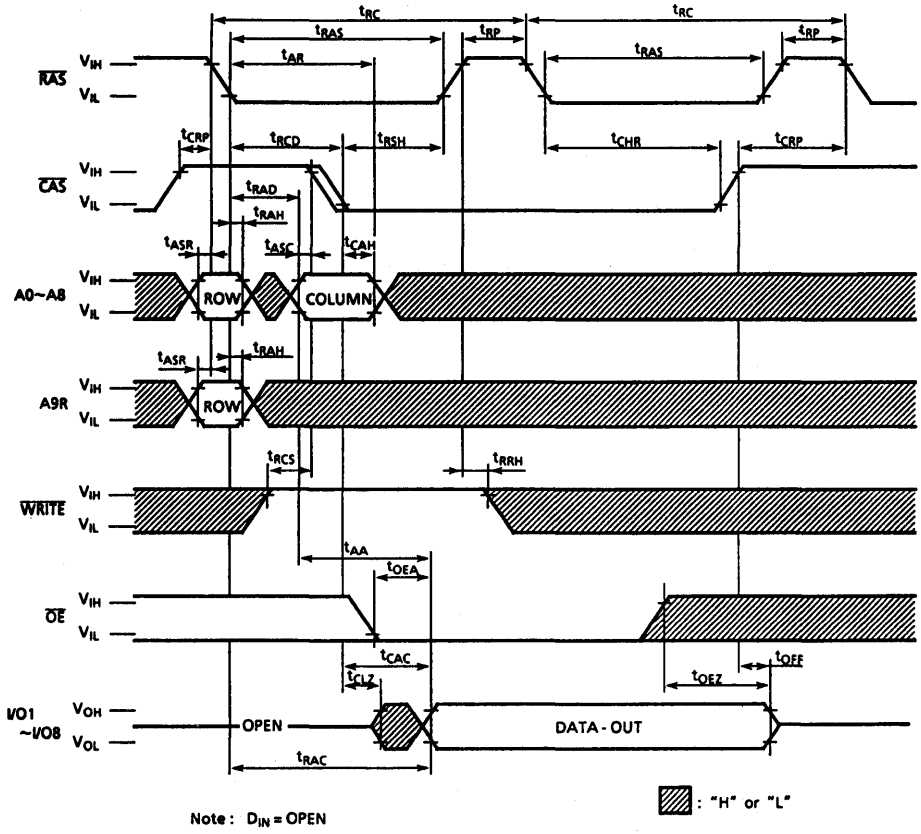
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$, A0~A8, A9R = "H" or "L"

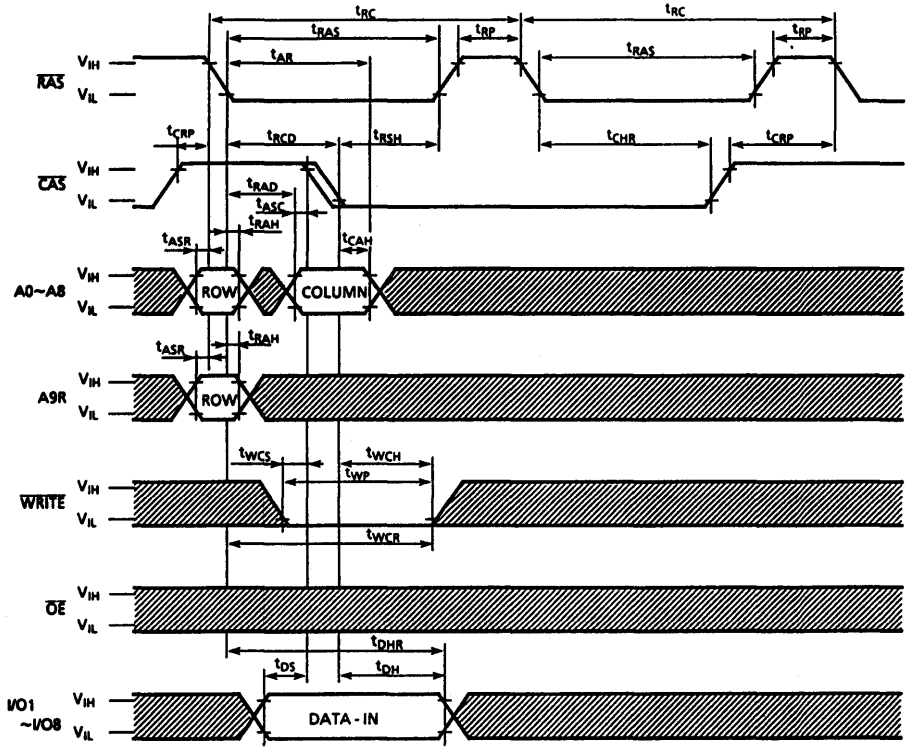
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)



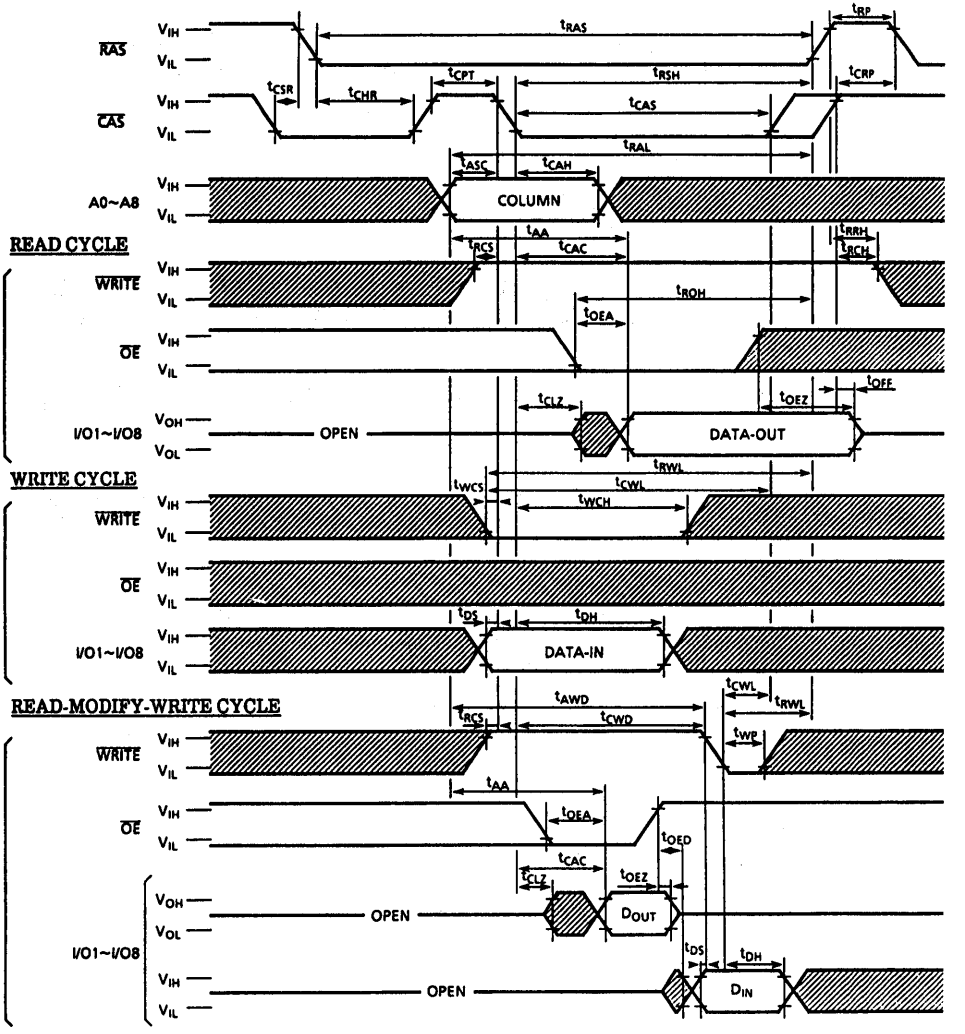
Note : D_{IN} = OPEN

HIDDEN REFRESH CYCLE (WRITE)



Note : D_{OUT} = OPEN

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



Note : A9R = "H" or "L"

APPLICATION INFORMATION

ADDRESSING

The 19 address bits required to decode 1 of the 524,288 cell locations within the TC514800AJ/AZ/AFT are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing $\overline{WRITE}$ low during the $\overline{RAS}/\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or $\overline{WRITE}$ stobes data on I/O1~I/O8 into the on-chip data latch. In an early write cycle, $\overline{WRITE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In delayed write or read modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WRITE}$ with setup and hold times referenced to these signals.

In delayed or read modify write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data Ouputs

The three state output buffers provide direct TTL compatibility with a fan-out of standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ imput is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 1024 row addresses (A0~A8, A9R) within each 16 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

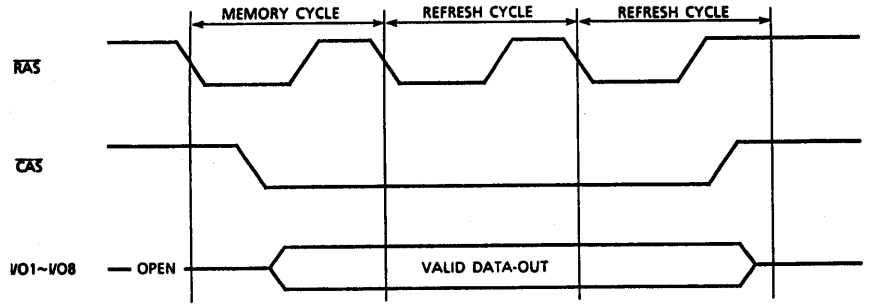
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514800AJ/AZ/AFT offers an alternate refresh method. If $\overline{CAS}$ is hold on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh opeation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC514800AJ/AZ/AFT allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514800AJ/AZ/AFT is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is perfomed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC514800AJ/AZ/AFT can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle as initialization cycles. The test procedure is as follows.

1. Write "0" into all the memory cells normal write mode.
2. Select one certain column address and read "0" out and write "1' in each cell be performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 1024 times.
3. Check "1" out of 1024 bits at normal read mode , which was written at 2.
4. Using the same column as 2., read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat This operation 1024 times.
5. Check "0" out of 1024 bits as normal read mode, which was written at 4.
6. Perform the above 1. to 5. to the complement data.

524,288 WORD X 8 BIT DYNAMIC RAM

DESCRIPTION

The TC514800AJL/AFTL is the new generation dynamic RAM organized 524,288 word by 8 bit. The TC514800AJL/AFTL utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514800AJL/AFTL to be packaged in a standard 28 pin plastic SOJ, and 28 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL,

FEATURES

- 524,288 word by 8 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-ion V_{BB} generator
- Low Power
  578mW MAX .Operating
  (TC514800AJ/AZ/AFT-70)
  495mW Max. Operating
  TC514800AJ/AZ/AFT-80
  1.1mW Max. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package
  TC514800AJL :SOJ28-P-400
  TC514800AFTL :TSOP28-P-400

KEY PARAMETERS

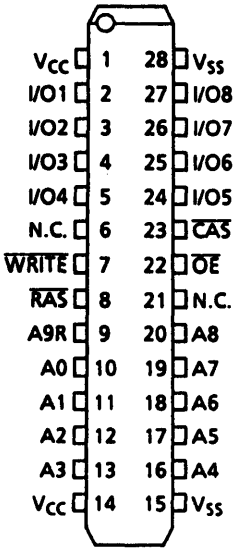
ITEM		TC514800AJL/AFTL	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

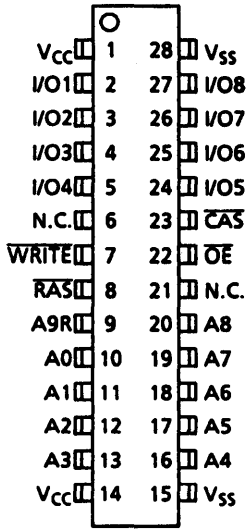
A0~A8 A9R	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Input/Output
V_{CC}	Power (+ 5V)
V_{SS}	Ground

PIN CONNECTION (TOP VIEW)

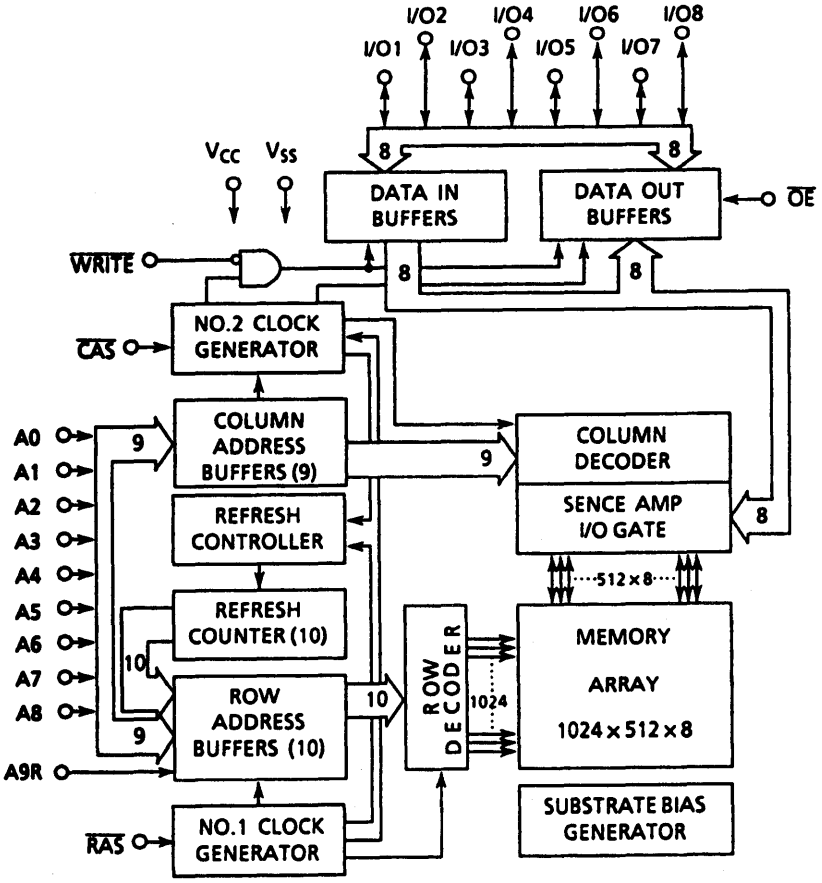
Plastic SOJ



Plastic TSOP
(Normal Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	—1~7	V	1
Output Voltage	V_{OUT}	—1~7	V	1
Power Supply Voltage	V_{CC}	—1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	—55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6..5	V	2
V_{IL}	Input Low Voltage (A0~A8,A9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-1.0*1	-	0.8	V	2
V_{IL}	Input Low Voltage ($\overline{I/O}$~$\overline{I/O9}$)	-0.5*2	-	0.8	V	2

*1 -2.5V at pulse width ≤ 20ns
*2 -2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	UNIT
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514800AJL/AFTL-70	-	105	mA	3,4 5
		TC514800AJL/AFTL-80	-	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514800AJL/AFTL-70	-	105	mA	3,5
		TC514800AJL/AFTL-80	-	90		
			-			
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC}MIN.)	TC514800AJL/AFTL-70	-	75	mA	3,4 5
		TC514800AJL/AFTL-80	-	65		
			-			
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			200	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$,Cycling: t_{RC}=t_{PC} MIN.)	TC514800AJL/AFTL-70	-	105	mA	3
		TC514800AJL/AFTL-80	-	90		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, Battery back up Mode ($\overline{CAS}$= $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ =V_{CC}-0.2V or 0.2V,			300	mA	3.6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	μA	
V_{OH}	OUTPUT CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT CURRENT Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC514800AJL/AFTL				UNIT	NOTE
		-70		-80			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	10,15, 16
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	10,15
t_{AA}	Access Time from Column Address	-	35	-	40	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Presharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	ns	
t_{AR}	Column Address Hold Time	55	-	60	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	12
t_{WCH}	Write Command Hold TIme	15	-	15	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514800AJL/AFTL				UNIT	NOTES
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	13
t_{DHR}	Data Hold Time	15	-	15	-	ns	13
t_{DH}	Data Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	
t_{REF}	Refresh Period	-	128	-	128	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	-	110	-	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	-	70	-	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	75	-	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to OE	10	-	10		ns	
t_{OEA}	$\overline{OE}$ Access TIme	-	20	0	20	ns	10
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	11
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A8, A9R)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$))	-	7	pF
C_O	Input Capacitance (I/O1~I/O8)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. t_{RAS} (max.) = 1 µms is only applied to to refresh of battery-back up. t_{RAS} (max.) = 10µs is applied to functional opration.

7. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

8. AC measurements assume t_T=5ns.

9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieveS the open circuit condition and are not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

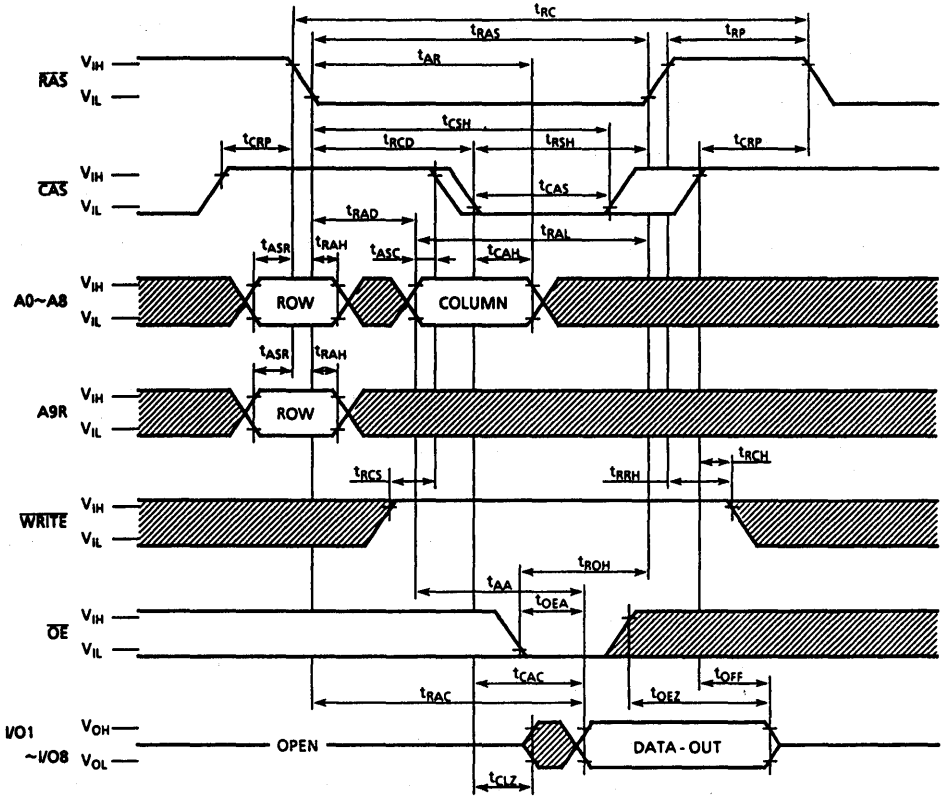
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the date sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RC}D (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

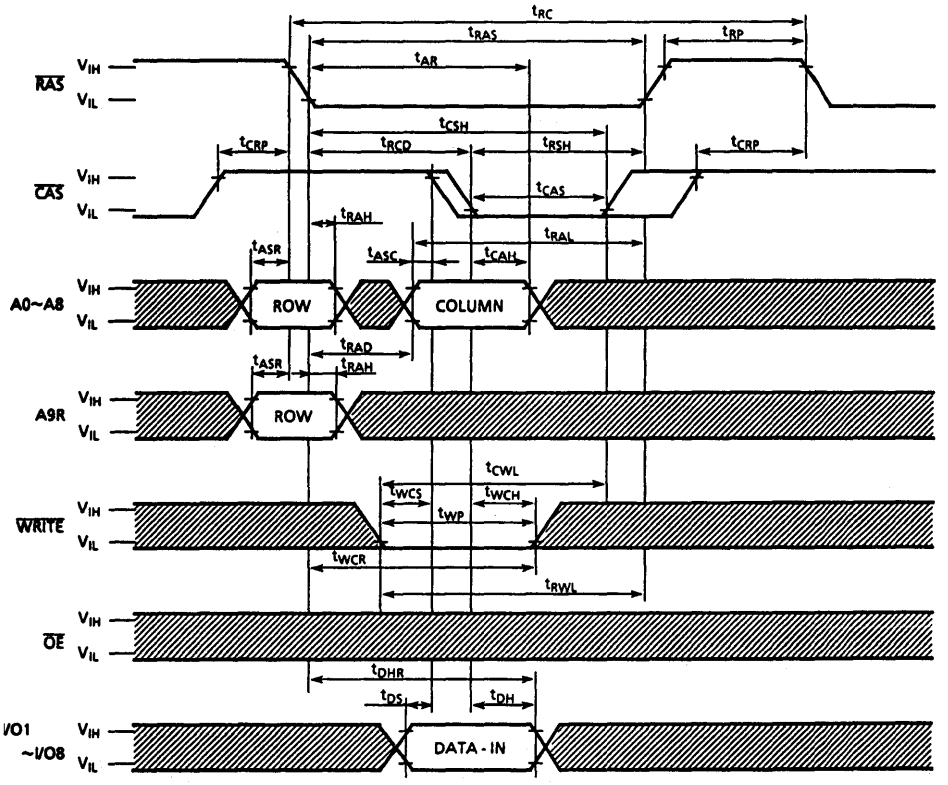
READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

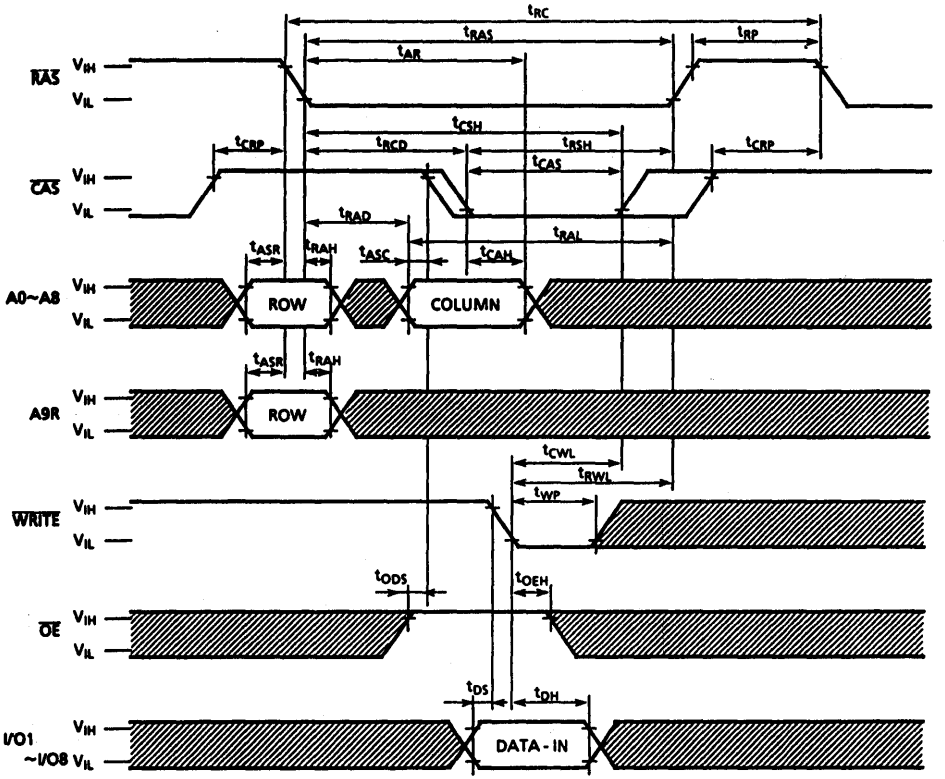
WRITE CYCLE (EARLY WRITE)



Note : D_{OUT} = OPEN

▨ : "H" or "L"

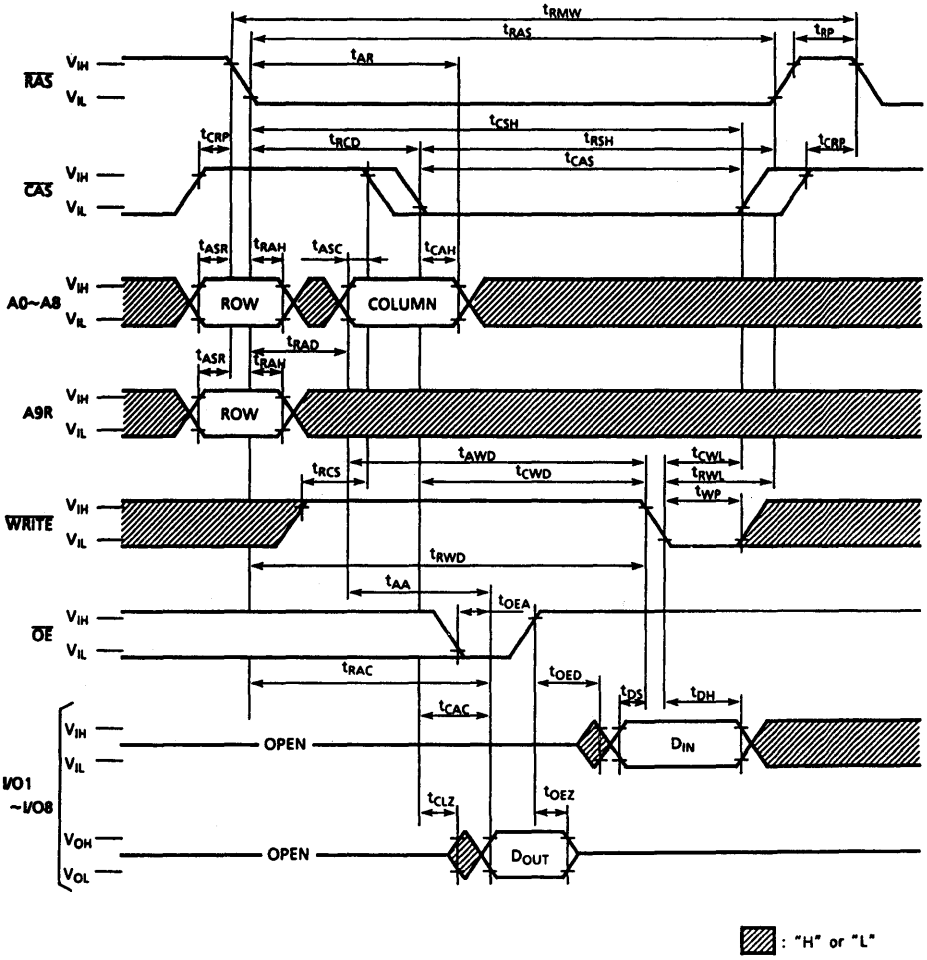
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



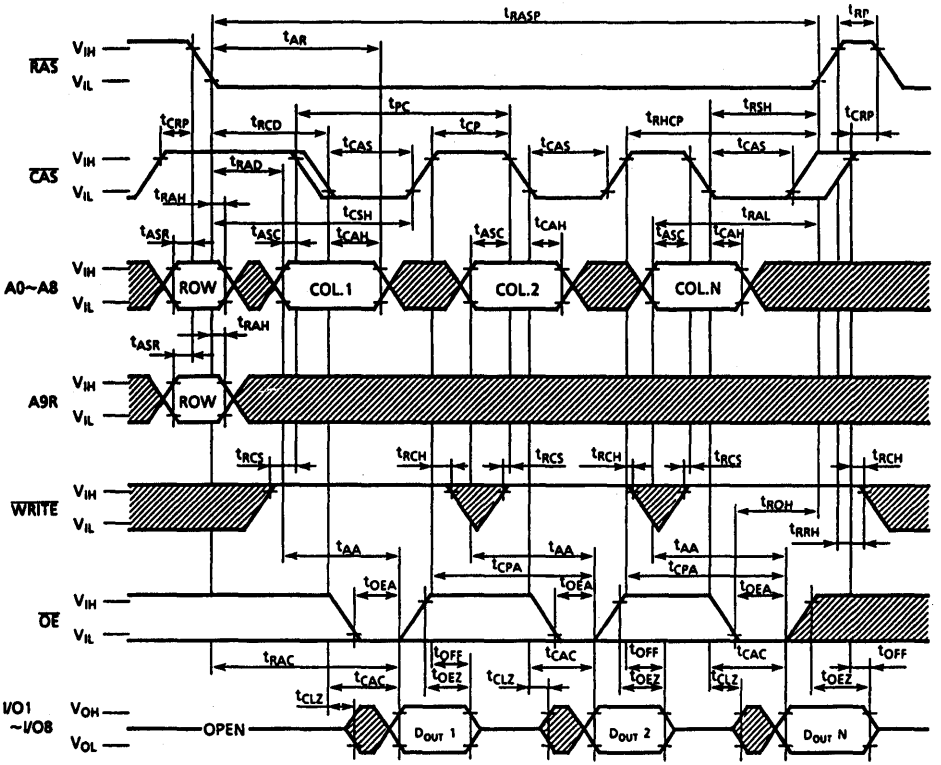
Note : D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



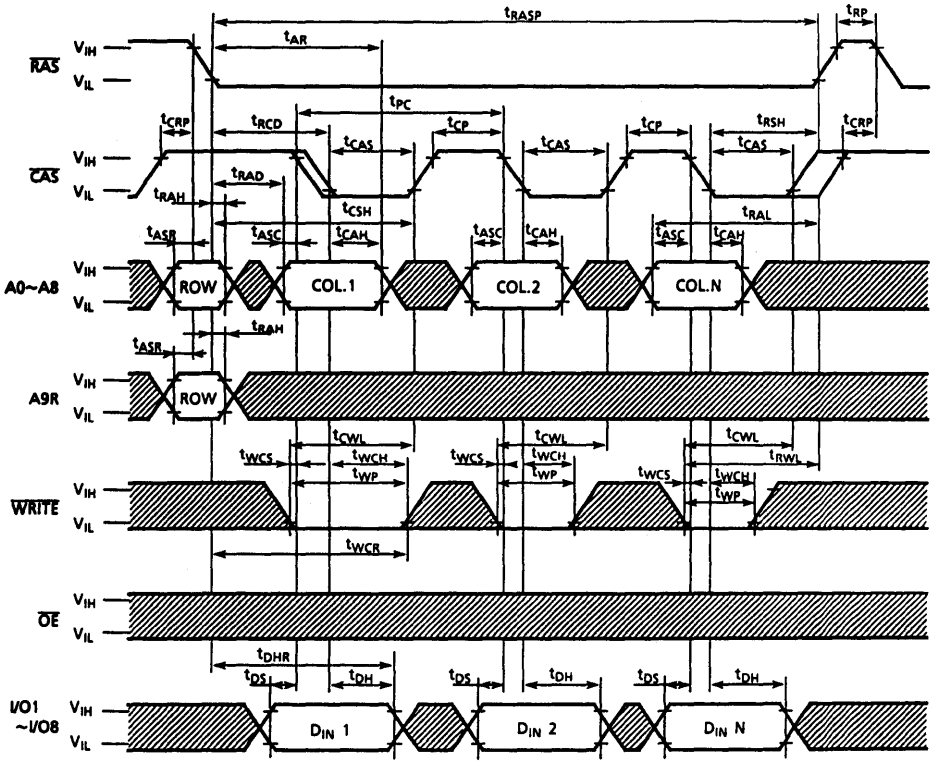
FAST PAGE MODE READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

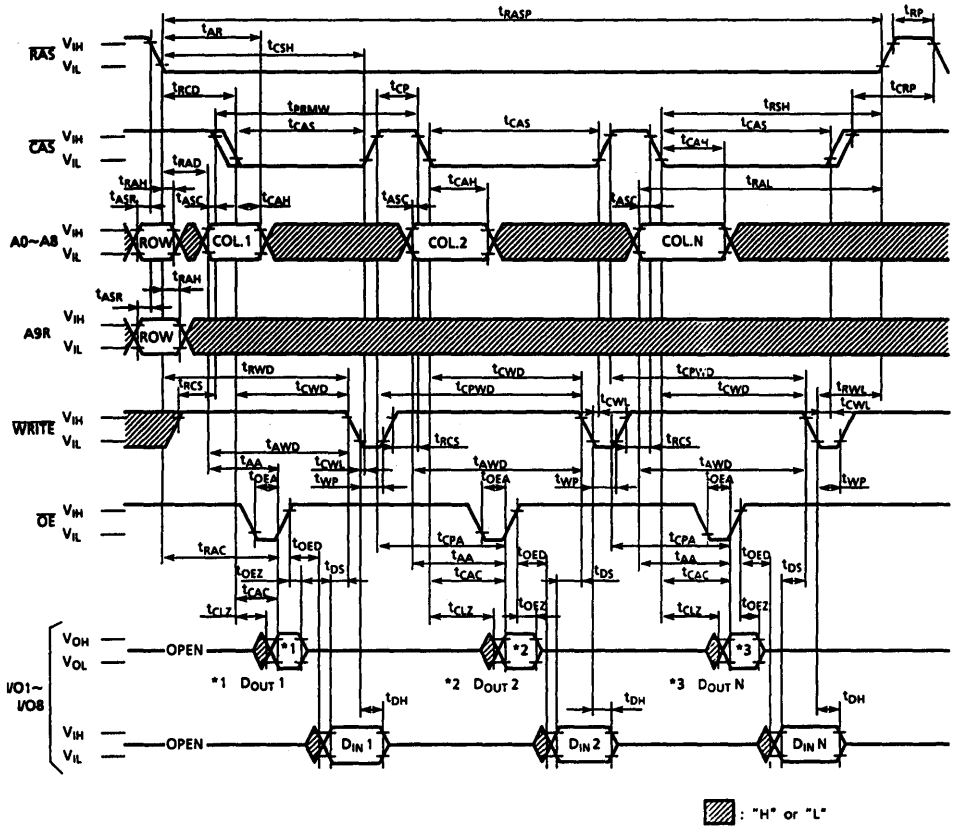
FAST PAGE MODE WRITE CYCLE



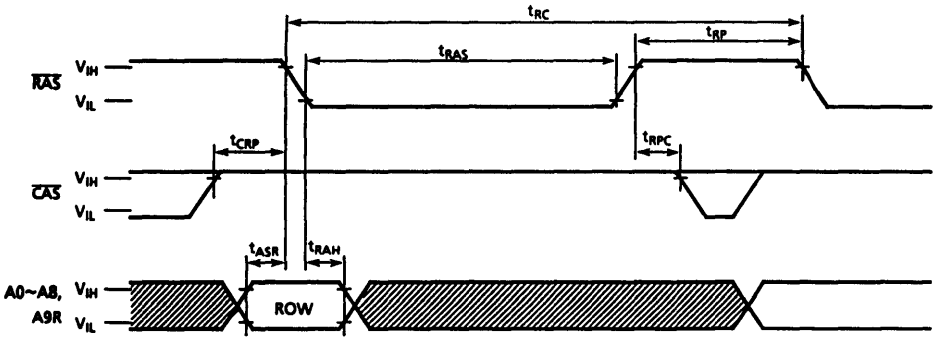
Note : D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



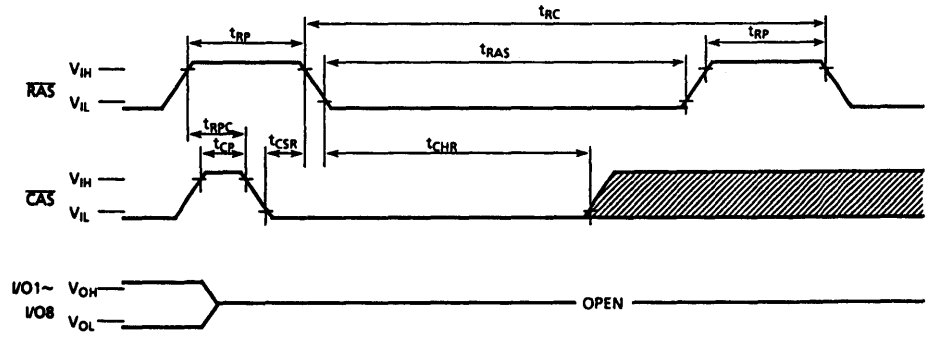
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$, D_{IN} = "H" or "L"
D_{OUT} = OPEN

▨ : "H" or "L"

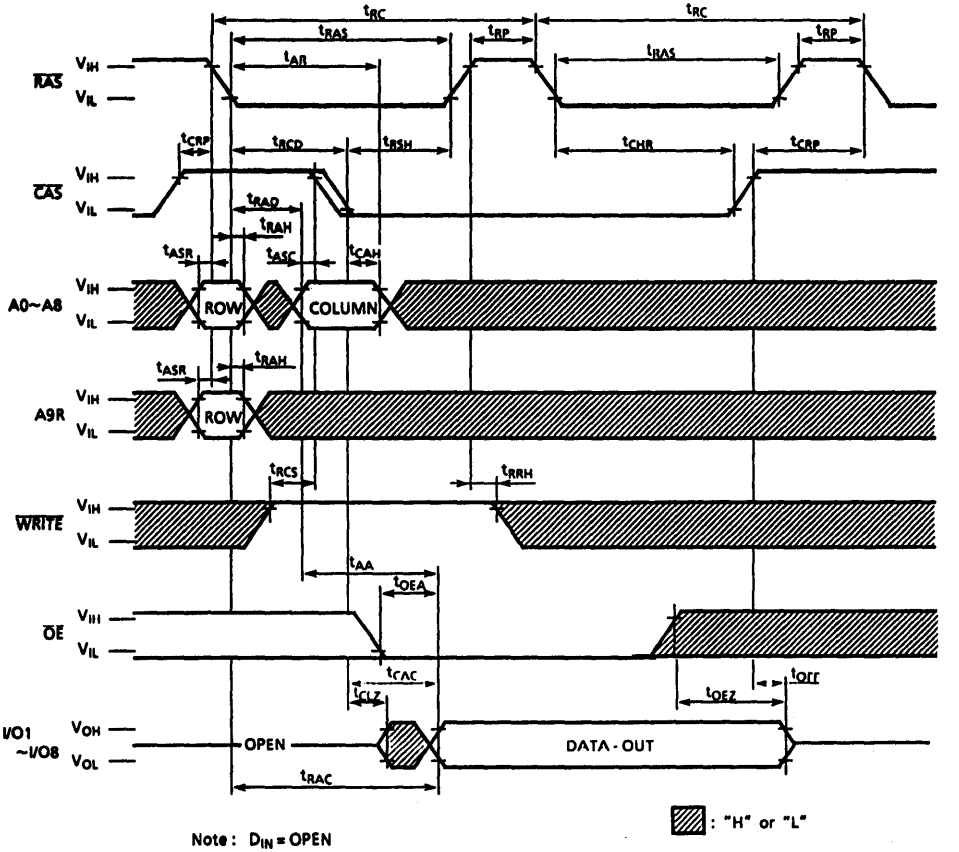
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$, A0~A8, A9R = "H" or "L"

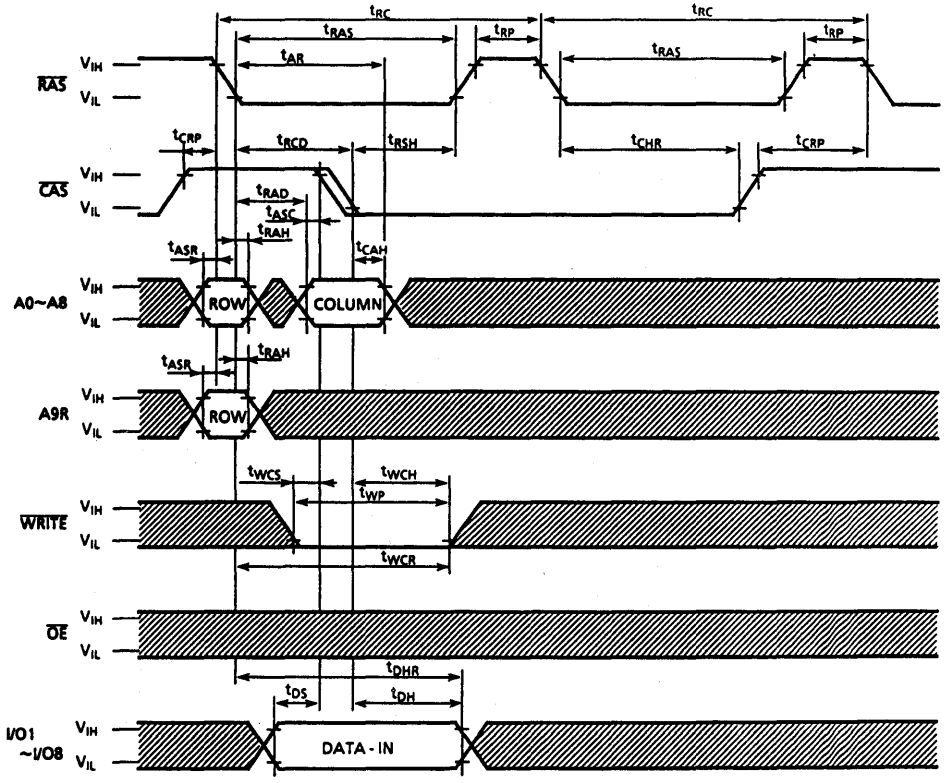
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)



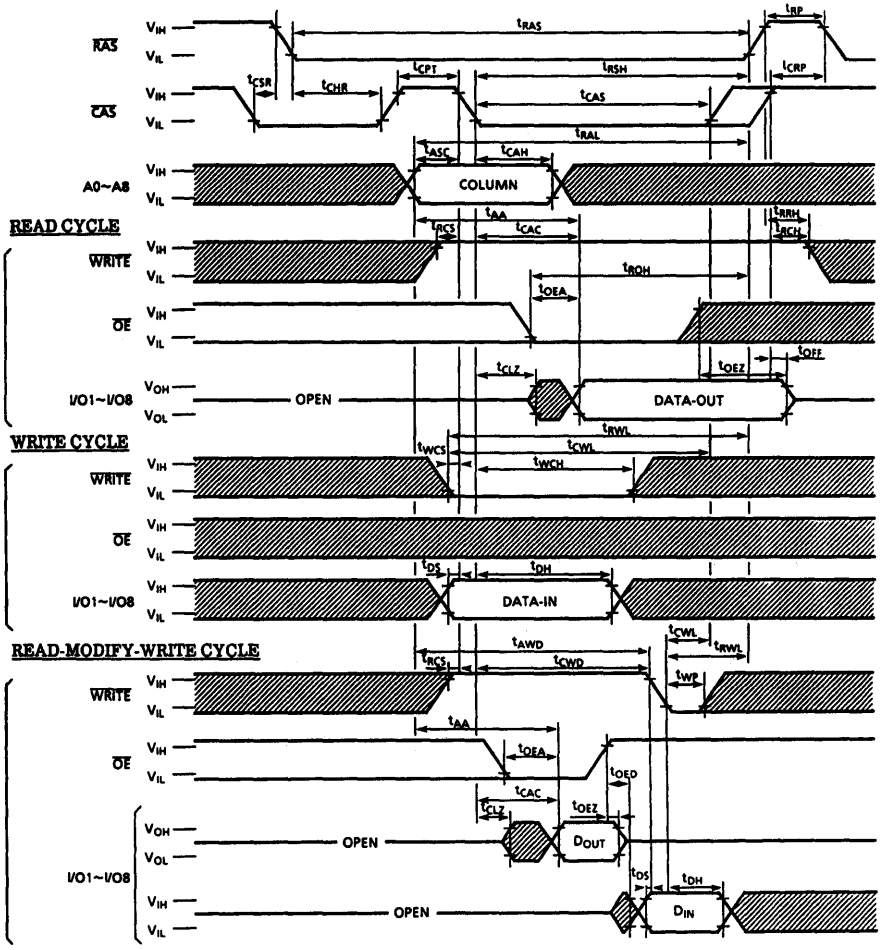
Note : D_{IN} = OPEN

HIDDEN REFRESH CYCLE (WRITE)



Note : D_{OUT} = OPEN

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



Note : A9R = "H" or "L"

APPLICATION INFORMATION

ADDRESSING

The 19 address bits required to decode 1 of the 524,288 cell locations within the TC514800AJL/AFTL are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing $\overline{WRITE}$ low during the $\overline{RAS}/\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or $\overline{WRITE}$ stobes data on I/O1~I/O8 into the on-chip data latch. In an early write cycle, $\overline{WRITE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In delayed write or read modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WRITE}$ with setup and hold times referenced to these signals.

In delayed or read modify write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data Ouputs

The three state output buffers provide direct TTL compatibility with a fan-out of standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ imput is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{\text{RAS}}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 1024 row addresses (A0~A8, A9R) within each 128 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished "$\overline{\text{RAS}}$-only" cycles, $\overline{\text{RAS}}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

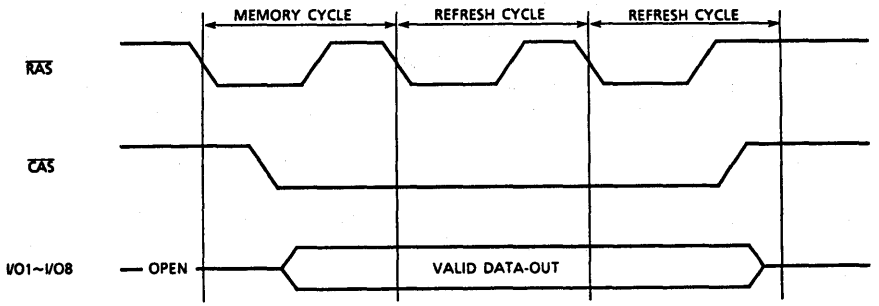
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing available on the TC514800AJL/AFTL offers an alternate refresh method. If $\overline{\text{CAS}}$ is hold on low for the specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh opeation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC514800AJL/AFTL allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{\text{RAS}}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514800AJL/AFTL is the refresh cycles may be performed while maintaining valid data at the output pins. This referred to as Hidden Refresh. Hidden Refresh is perfomed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. (see figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC514800AJL/AFTL can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle as initialization cycles. The test procedure is as follows.

1. Write "0" into all the memory cells normal write mode.
2. Select one certain column address and read "0" out and write "1' in each cell be performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 1024 times.
3. Check "1" out of 1024 bits at normal read mode , which was written at 2.
4. Using the same column as 2., read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat This operation 1024 times.
5. Check "0" out of 1024 bits as normal read mode, which was written at 4.
6. Perform the above 1. to 5. to the complement data.

524,288 WORD X 8 BIT DYNAMIC RAM

DESCRIPTION

The TC514800AJLL/AFTLL is the new generation dynamic RAM organized 524,288 word by 8 bit. The TC514800AJLL/AFTLL utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514800AJLL/AFTLL to be packaged in a standard 28 pin plastic SOJ, and 28 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 524,288 word by 8 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  578mW MAX .Operating
  (TC514800AJLL/AFTLL-70)
  495mW MAX. Operating
  (TC514800AJLL/AFTLL-80)
  1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Self Refresh Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514800AJLL : SOJ28-P-400
  TC514800AFTLL : TSOP28-P-400

KEY PARAMETERS

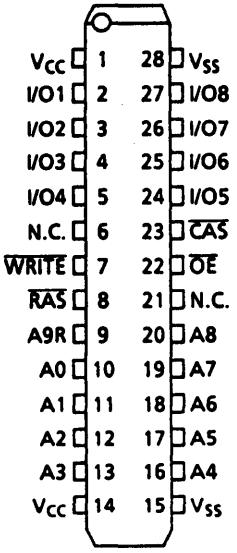
ITEM		TC514800AJLL/AFTLL	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

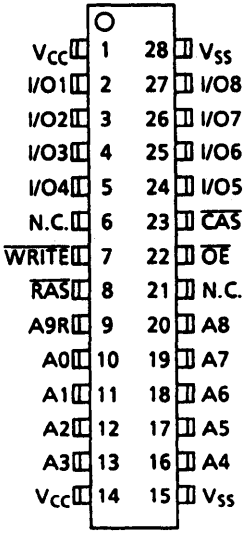
A0~A8, A9R	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

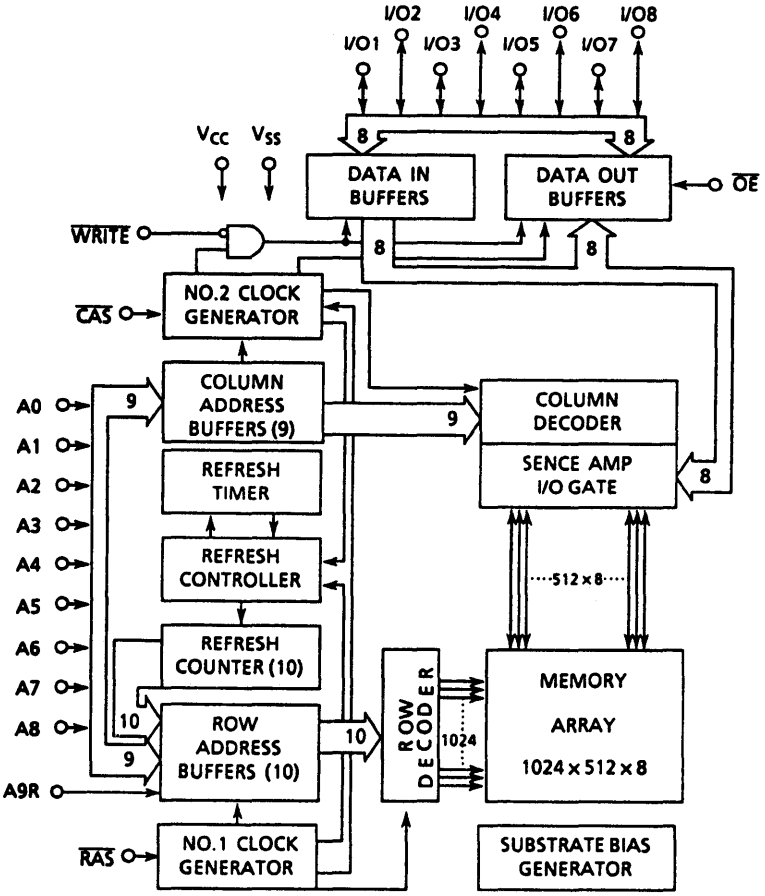
Plastic SOJ



Plastic TSOP
(Normal Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage (A0~A8, A9R, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-1.0*1	-	0.8	V	2
V_{IL}	Input Low Voltage (I/01~I/08)	-0.5*2	-	0.8	V	2

*1 -2.5V at pulse width ≤ 20ns
*2 -2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN)	TC514800AJLL/AFTL-70	-	105	mA	3,4 5
		TC514800AJLL/AFTL-80	-	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514800AJLL/AFTL-70	-	105	mA	3, 5
		TC514800AJLL/AFTL-80	-	90		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC514800AJLL/AFTL-70	-	75	mA	3,4 5
		TC514800AJLL/AFTL-80	-	65		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			200	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC514800AJLL/AFTL-70	-	105	mA	3
		TC514800AJLL/AFTL-80	-	90		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Suuply Current, Battery Back Up Mode ($\overline{RAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$=V_{CC}-0.2V or 0.2V $\overline{WRITE}$ =V_{CC}-0.2V or 0.2V, A0~A8, A9R=V_{CC}-0.2V or 0.2V, I/O~I/O8=Vcc-0.2V, 0.2V or OPEN:t_{RC}=125µs, t_{RAS}=t_{RAS} MIN. ~1µs)		-	300	µA	3,6
I_{CCS}	SELF REFRESH CURRENT Average Power Supply Current, Self Refresh Mode ($\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{WRITE}$=V_{CC}-0.2V or 0.2V, $\overline{OE}$=V_{CC}-0.2V or 0.2V A0~8=V_{CC}-0.2V or 0.2V, I/O1~8=V_{CC}-0.2V, 0.2V or OPEN		-	200	µA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≤V_{IN}≤0.5V, All Other Pins Not Under Test=OV)		-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (OV≤V_{OUT}≤5.5V),		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 7,8,9)

SYMBOL	PARAMETER	TC514800AJLL/AFTLL				UNIT	NOTES
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	10,15,16
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	10,15
t_{AA}	Access Time from Column Address	-	35	-	40	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Presharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	0	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	-	60		ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	35	-	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	12
t_{WCH}	Write Command Hold Time	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514400AJLL/AFTLL				UNIT	NOTES
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{WCR}	Write Command Hold Time referenced $\overline{RAS}$	55	-	60	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	13
t_{DH}	Data Hold Time	15	-	15	-	ns	13
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	
t_{REF}	Refresh Period	-	128	-	128	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	-	110	-	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	-	70	-	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	75	-	ns	14
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	40	-	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	20	ns	10
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	11
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	
t_{RASS}	$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	100	-	100	-		
t_{RPS}	$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	130	-	150	-	ns	
t_{CHS}	$\overline{CAS}$ Hold time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	-50	-	-60	-	ns	

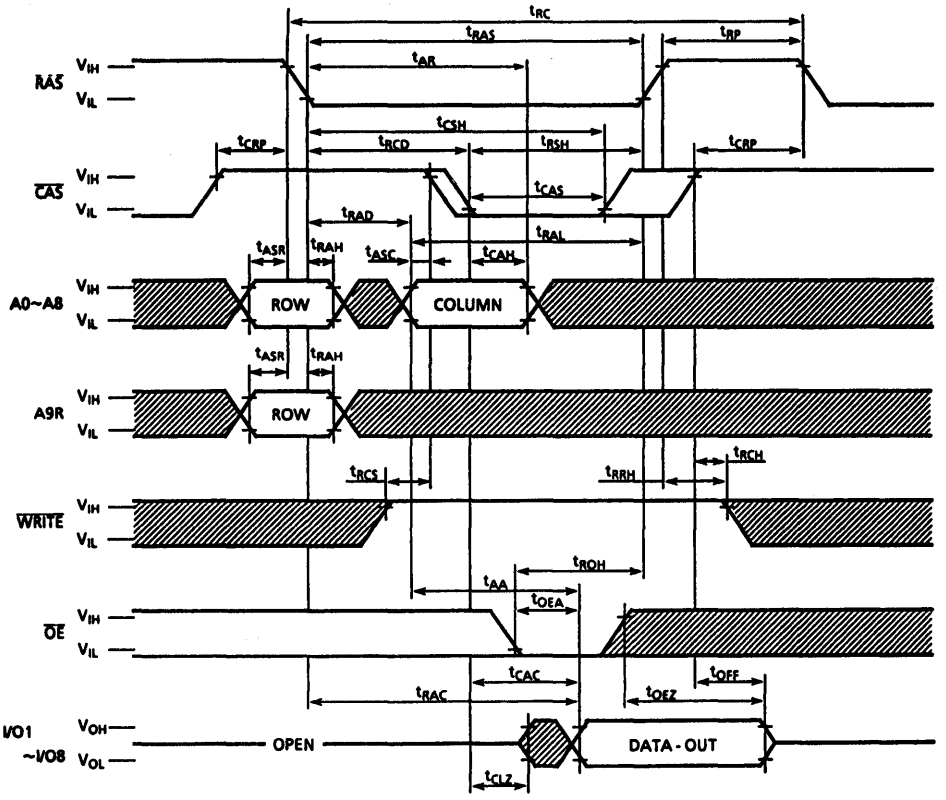
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A8, A9R)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (I/O1~I/O8)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}$=V_{IL}. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
6. t_{RAS}(max.)=1μs is only applied to refresh of battery-back up. t_{RAS}(max.)=10μs is applied to functional operating.
7. An initial pause of 200μs is required after pwoer-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume t_T=5ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the date sheet as electrical characteristics only. If t_{WCS} >t_{WCS} (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If t_{RWD}>t_{RWD} (min.), t_{CWD}>t_{CWD} (min.), t_{AWD}>t_{AWD} (min.) and t_{CPWP}>t_{CPWD} (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

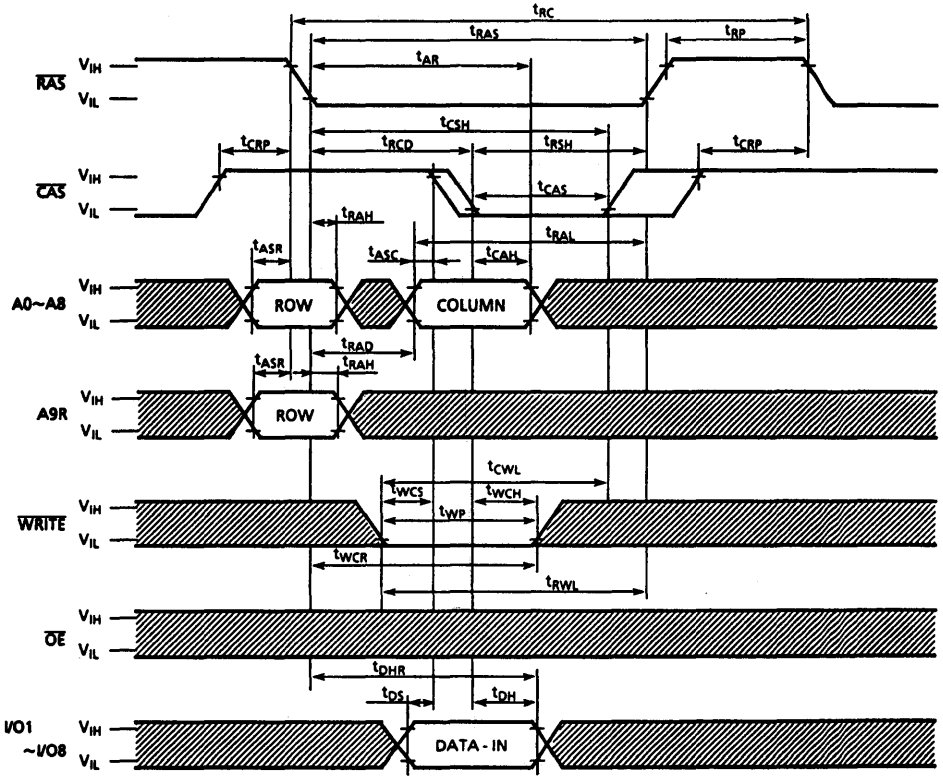
READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

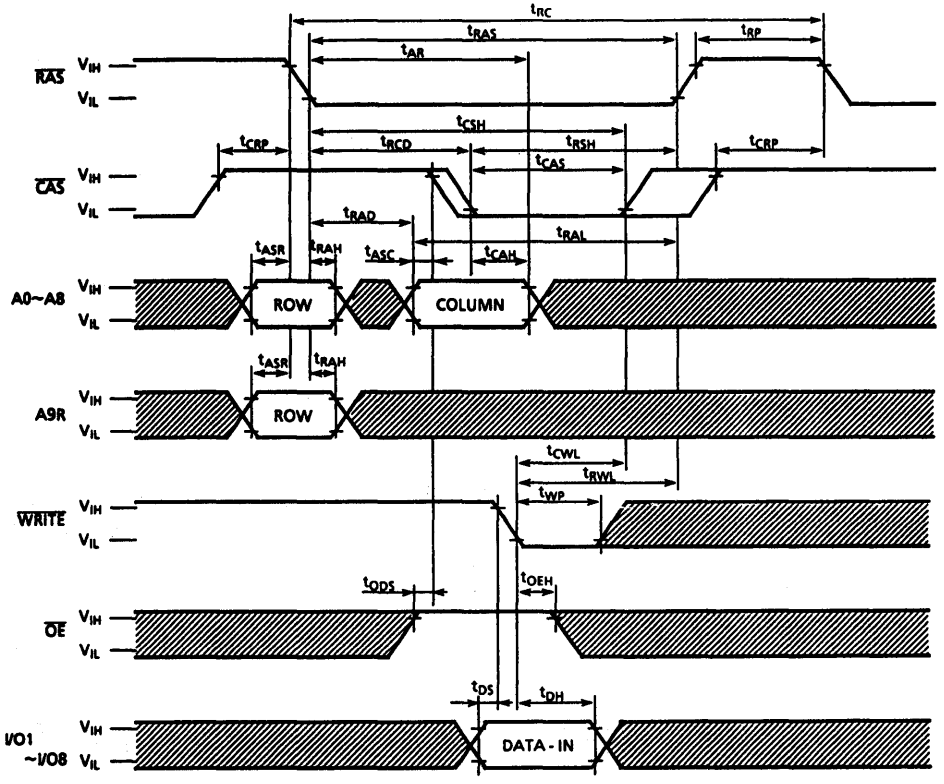
WRITE CYCLE (EARLY WRITE)



Note : D_{OUT} = OPEN

▨ : "H" or "L"

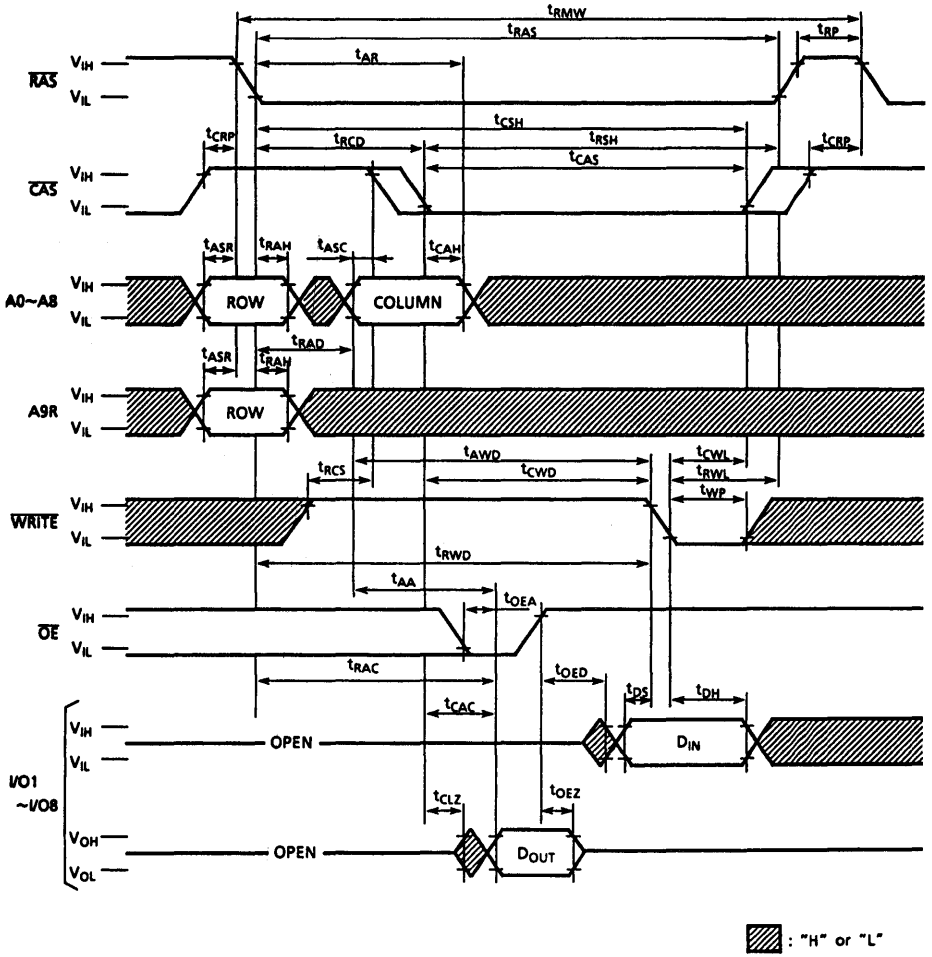
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



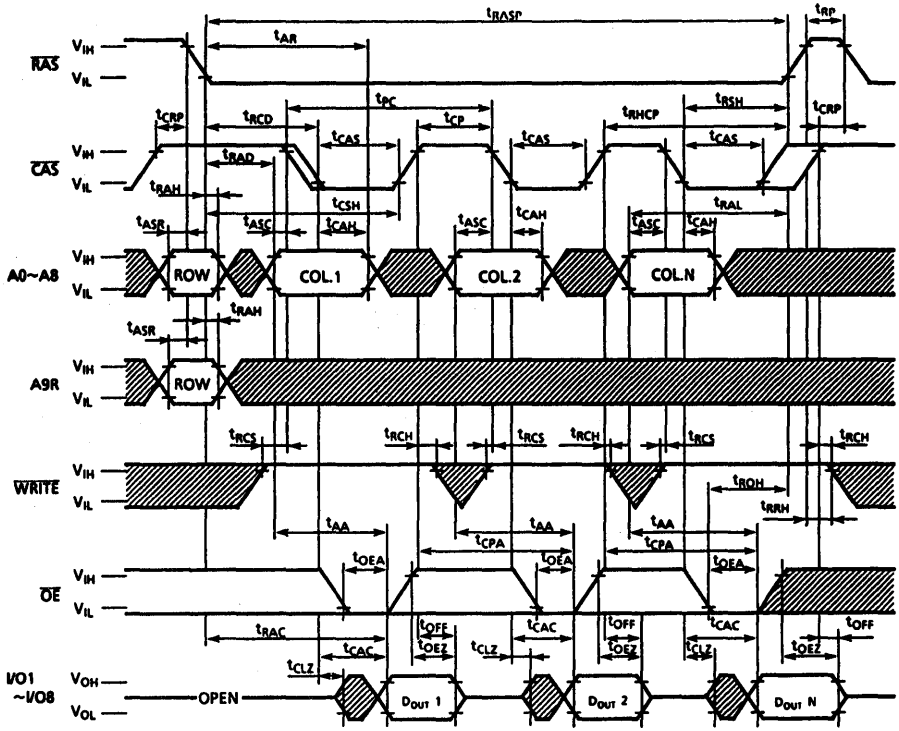
Note : D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



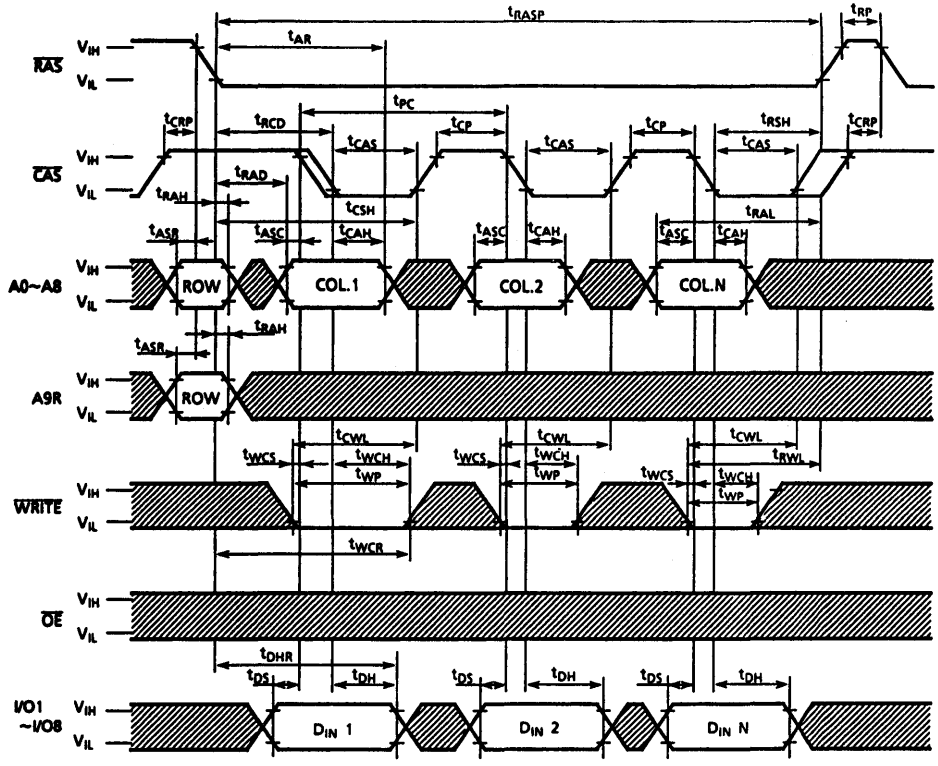
FAST PAGE MODE READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

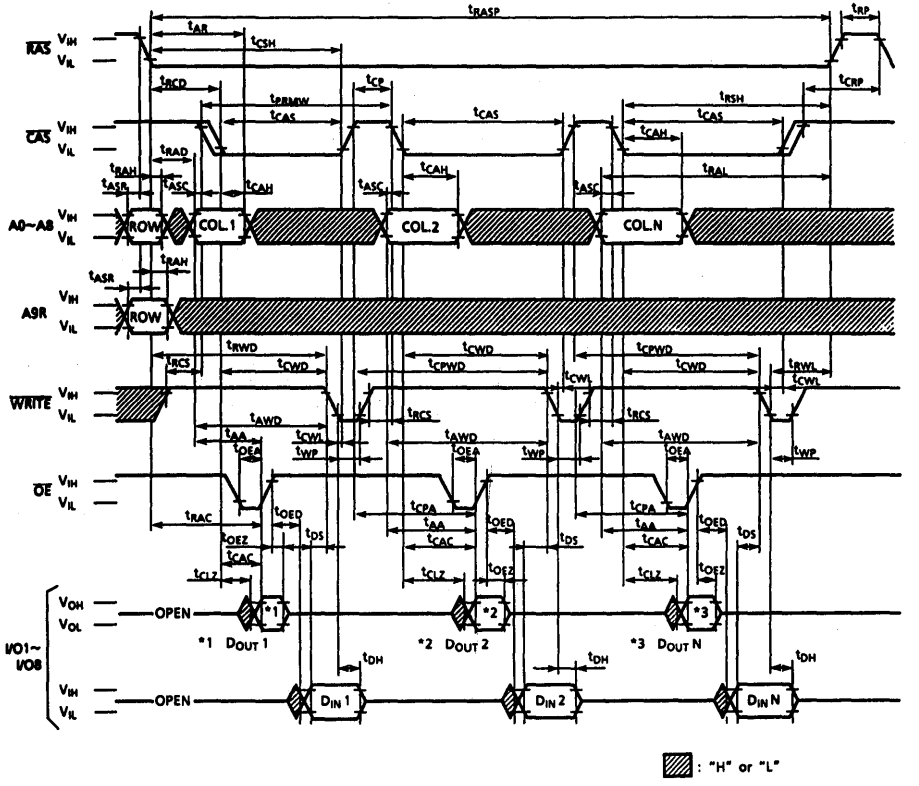
FAST PAGE MODE WRITE CYCLE



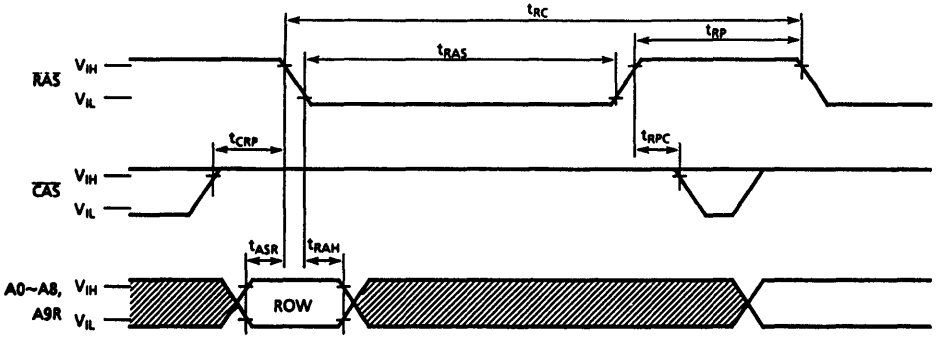
Note : D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



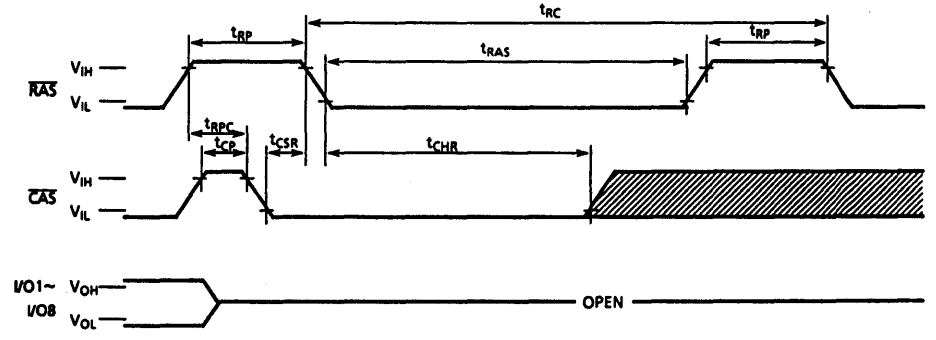
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$, D_{IN} = "H" or "L"
D_{OUT} = OPEN

▨ : "H" or "L"

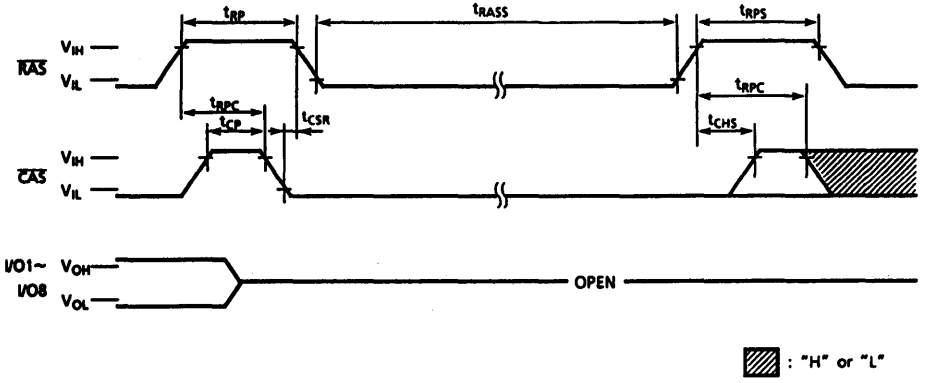
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$, A0~A8, A9R = "H" or "L"

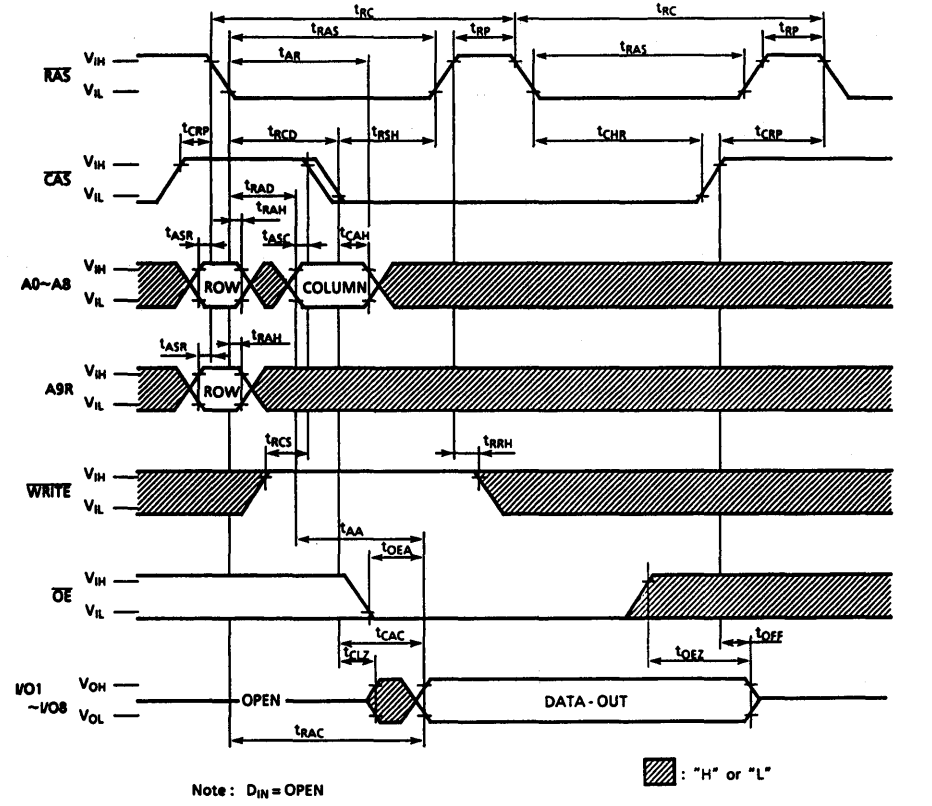
▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ SELF REFRESH CYCLE



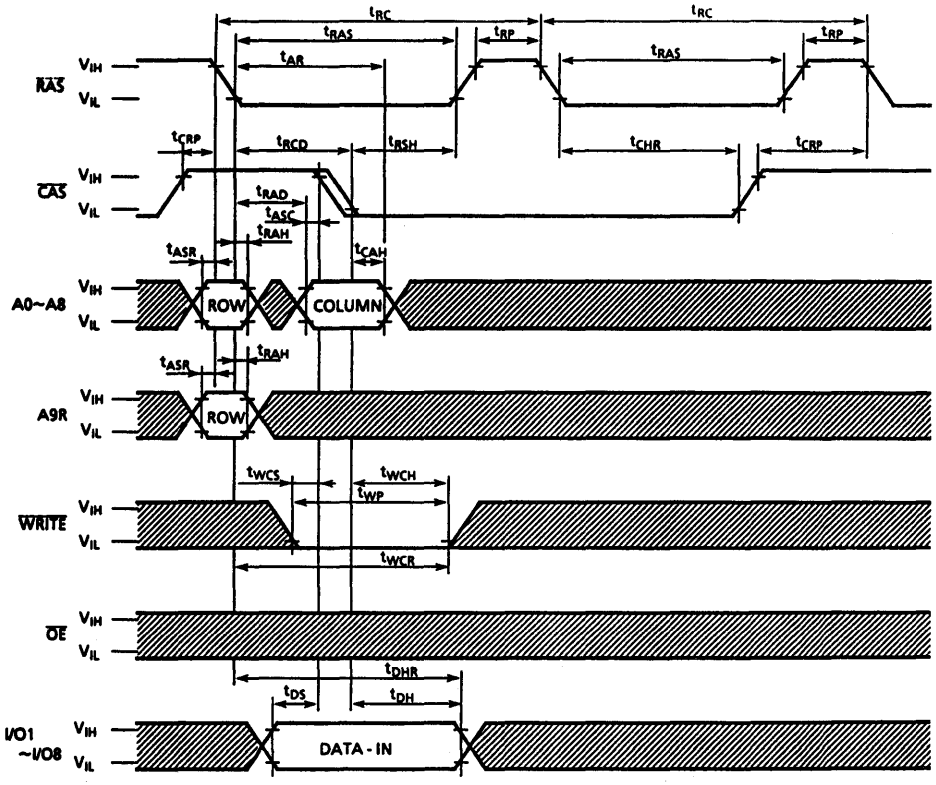
Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$, A0~A8, A9R = "H" or "L"

HIDDEN REFRESH CYCLE (READ)



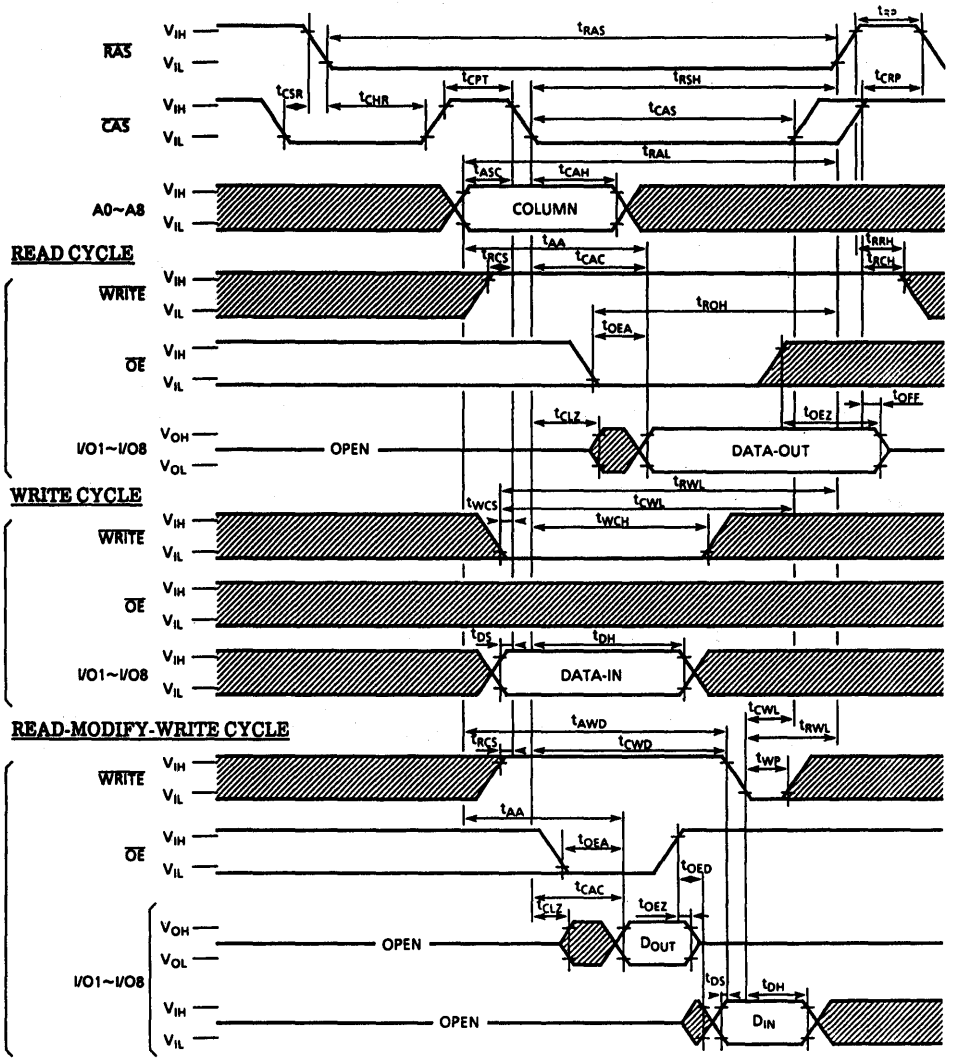
Note: D_{IN} = OPEN

HIDDEN REFRESH CYCLE (WRITE)



Note : D_{OUT} = OPEN

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



: "H" or "L"

Note : A9R = "H" or "L"

2,097,152 WORD X 8 BIT DYNAMIC RAM

DESCRIPTION

The TC5117800A series is the new generation dynamic RAM organized 2,097,152 word by 8 bit. The TC5117800A series utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC5117800A to be packaged in 28 pin plastic SOJ, and 28 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 2,097,152 word by 8 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  633mW MAX .Operating
  (60ns Version)
  523mW MAX. Operating
  (70ns Version)
  440mW MAX. Operating
  (80ns Version)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 2048 refresh cycles/32ms
- Package
  TC5117800ANJ : SOJ28-P-400C
  TC5117800ANT : TSOP28-P-400

KEY PARAMETERS

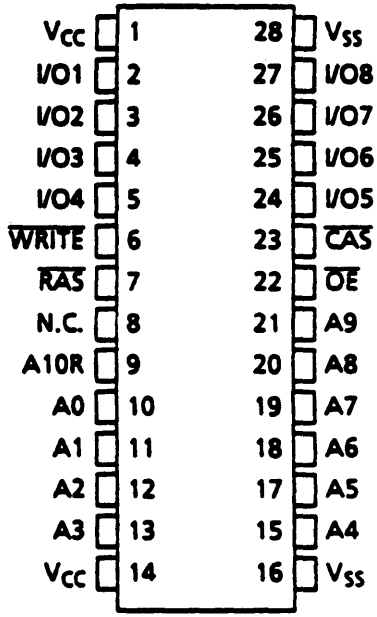
ITEM		TC5117800ANJ/ANT		
		-60	-70	-80
t_{RAC}	$\overline{RAC}$ Access Time	60ns	70ns	80ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns	20ns
t_{RC}	Cycle Time	110ns	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	50ns

PIN NAME

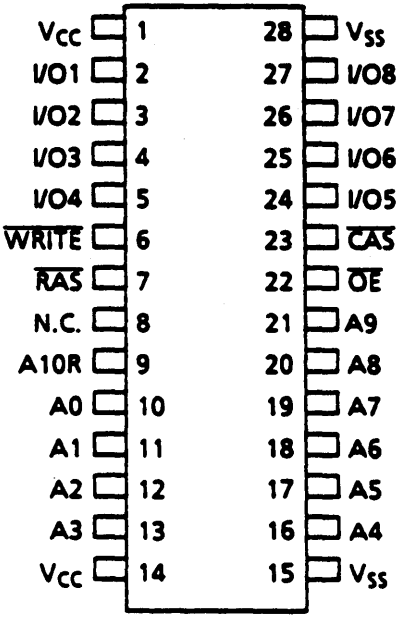
A0~A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/01~/I08	Data Input/Output
V_{CC}	Power (+ 5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

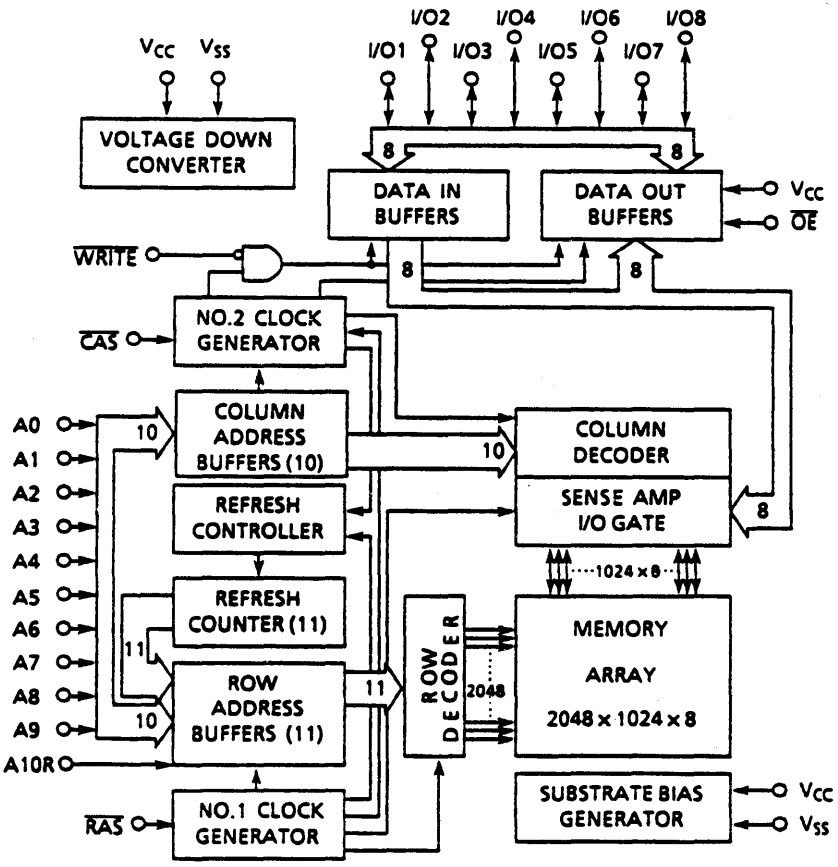
TC5117800ANJ



TC5117800ANT



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7.0$	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	900	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C))

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	V_{CC}+0.5*	V	2
V_{IL}	Input Low Voltage	—0.5**	—	0.8	V	2

* V_{CC} + 2.0V at pulse width ≤20ns. (pulse width is measured at V_{CC})
**-2.0V at pulse width ≤20ns. (pulse width is measured at OV)

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	-60	-	115	mA	3,4 5
		-70	-	95		
		-80	-	80		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	-60	-	115	mA	3, 5
		-70	-	95		
		-80	-	80		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	-60	-	75	mA	3,4 5
		-70	-	65		
		-80	-	55		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	-60	-	115	mA	3, 5
		-70	-	95		
		-80	-	80		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≤V_{IN}≤0.5V, All Other Pins Not Under Test=OV)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (OV≤V_{OUT}≤5.5V),		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	CHARACTERISTIC	TC5117800AJ/ANJ/AZ/ANZ/AFT/ANT/ATR/ANR						UNIT	NOTE
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	12
t_{DH}	Data Hold Time	10	-	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	32	-	32	-	32	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	40	-	45	-	45	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	-	95	-	105	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	55	-	60	-	65	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	60	-	65	-	70	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	20	-	30	-	30	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	15	-	20	-	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	15	-	15	-	15	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	15	0	15	0	15	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	15	-	15	-	15	-	ns	
t_{ODS}	Output Disable Set-up Time	0	-	0	-	0	-	ns	
t_{WTS}	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC5117800AJ/ANJ/AZ/ANZ/AFT/ANT/ATR/ANR						UNIT	NOTE
		-60		-70		-80			
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	155	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	55	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	-	85	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	-	25	ns	9, 14
t_{AA}	Access Time from Column Address	-	35	-	40	-	45	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	50	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	85	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	85	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	85	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	40	-	45	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	45	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A10)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (I/O1~I/O8)	-	7	pF

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC5117800AJ/ANJ/AZ/ANZ/AFT/ANT/ATR/ANR						UNIT	NOTE
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	155	-	180	-	200	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	85	-	95	-	100	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	15	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed once or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (tPC).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

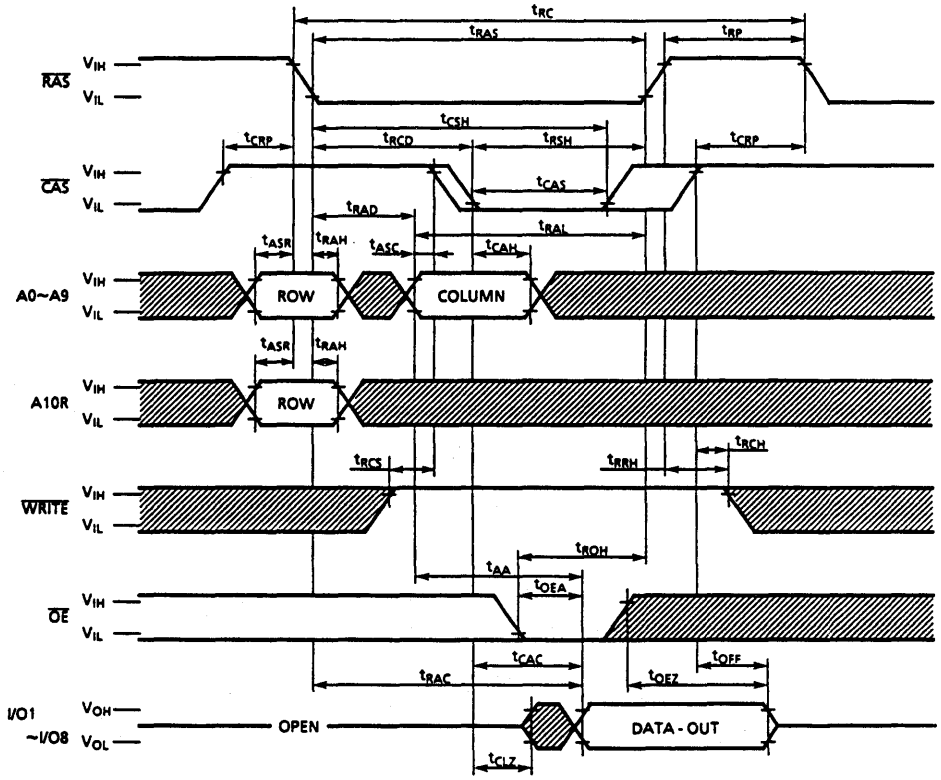
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

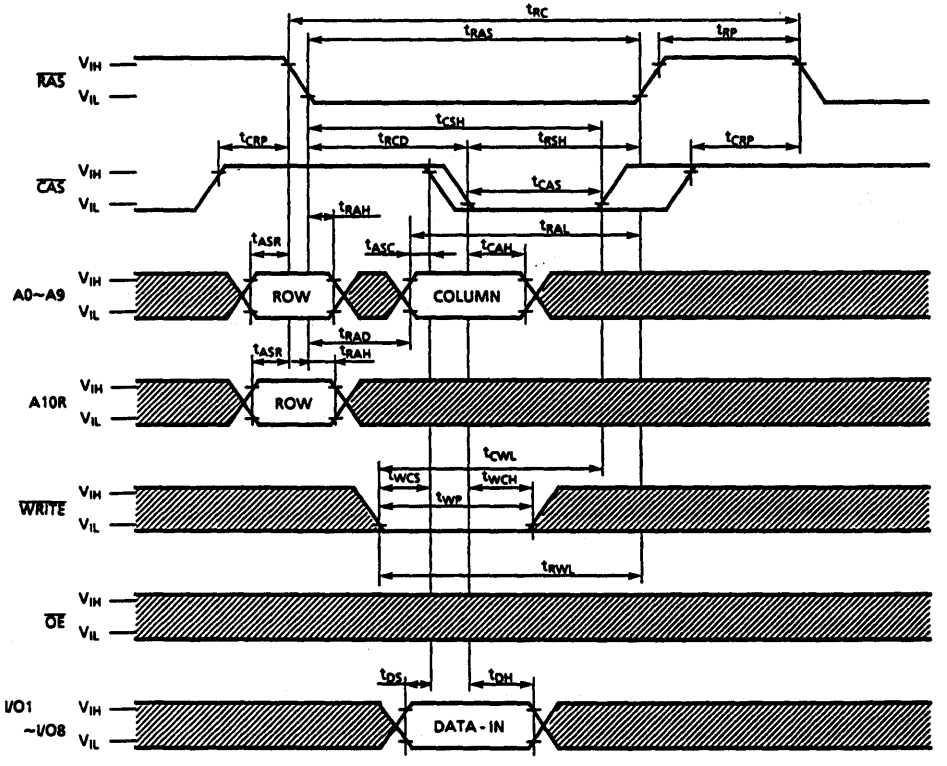
READ CYCLE



Note : D_{IN} = OPEN

: "H" or "L"

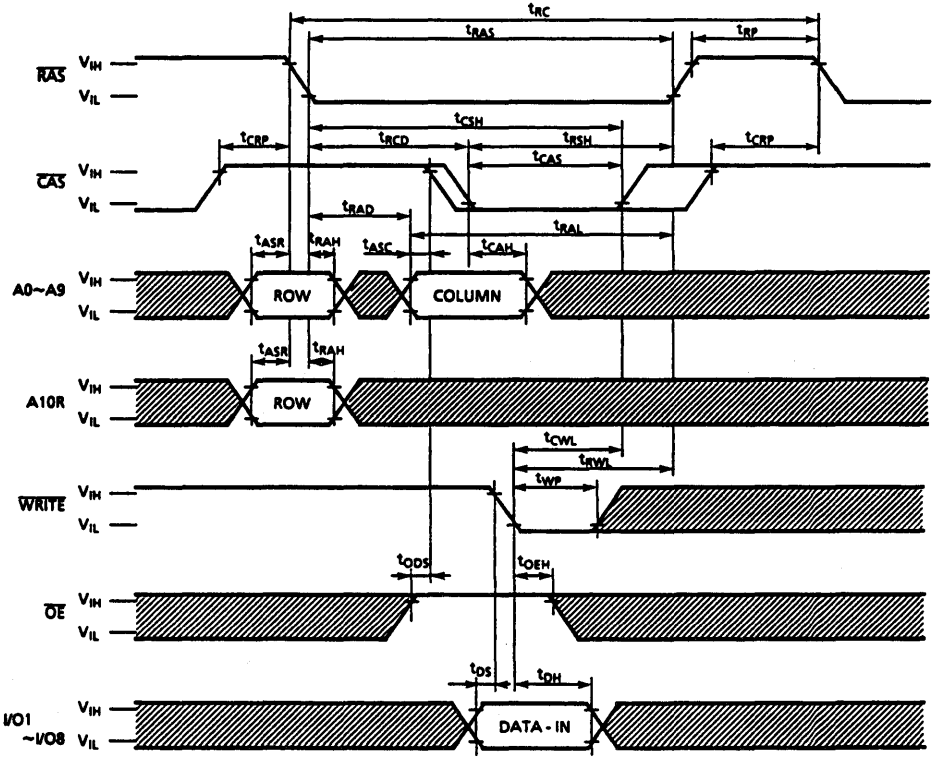
WRITE CYCLE (EARLY WRITE)



Note : D_{OUT} = OPEN

▨ : "H" or "L"

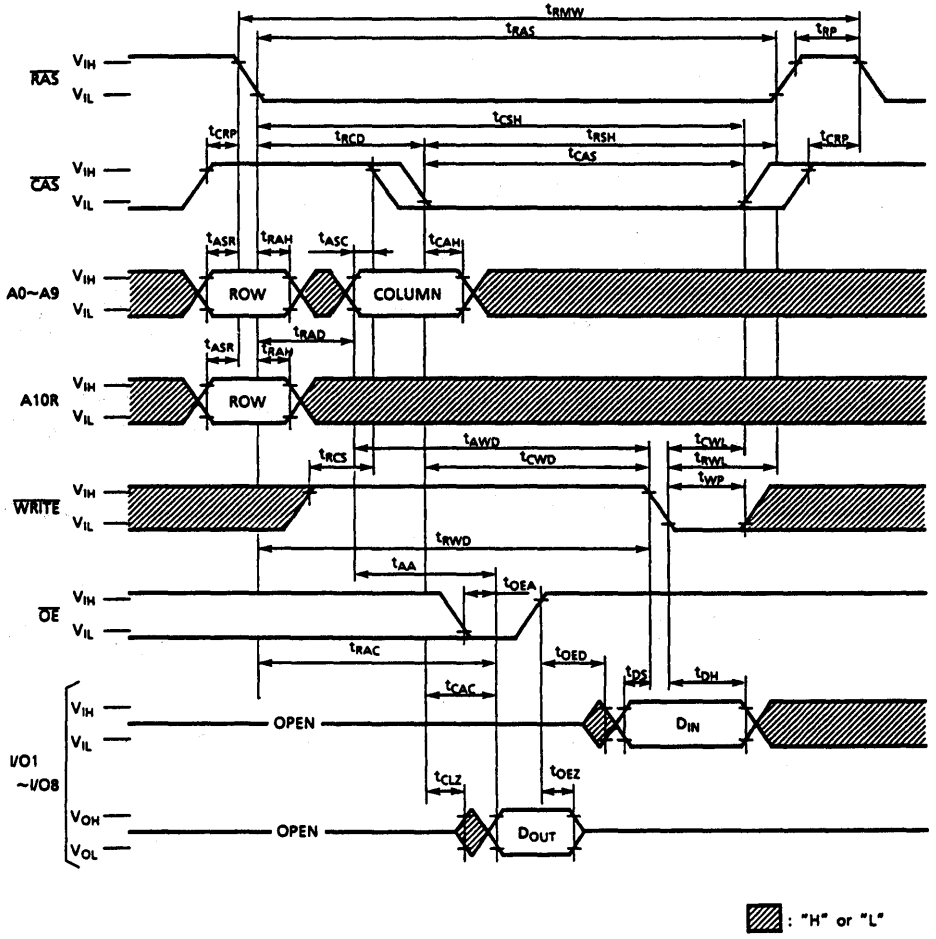
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



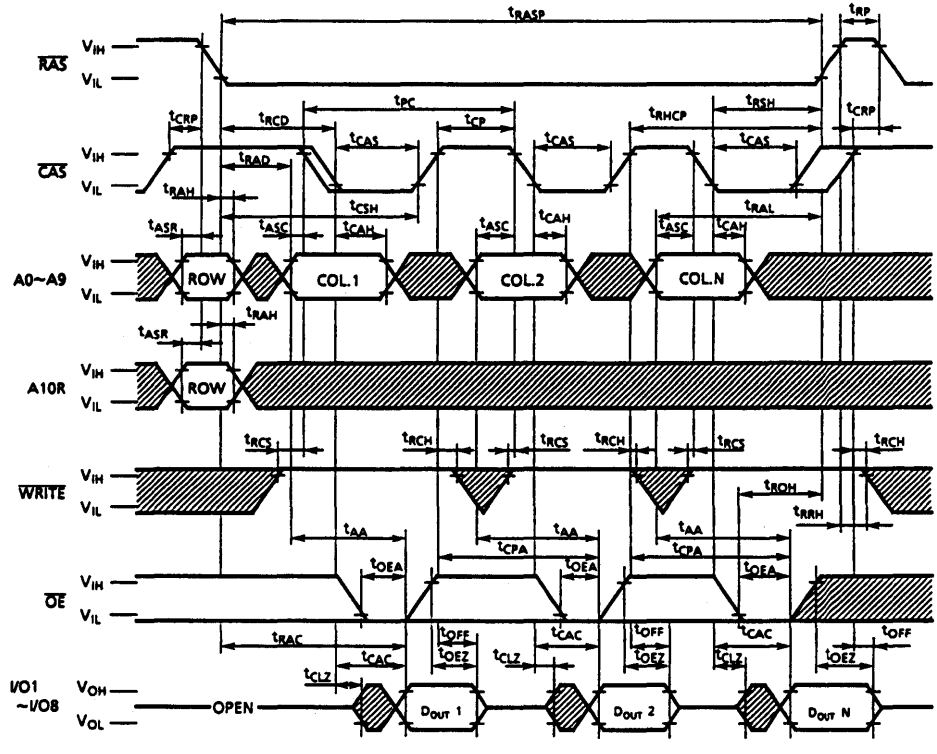
Note : D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



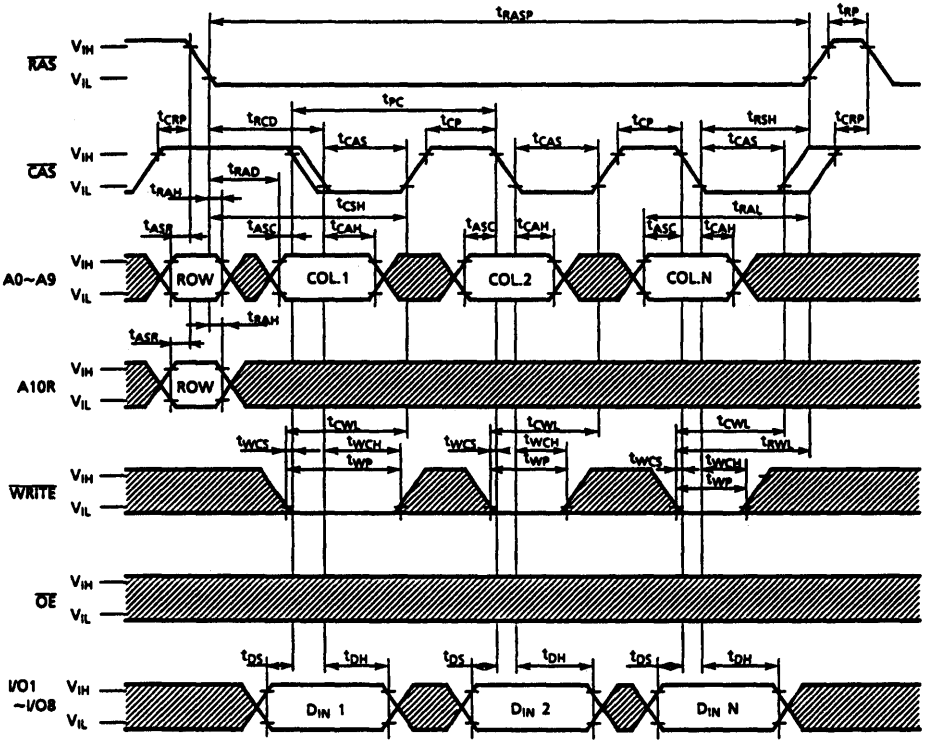
FAST PAGE MODE READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

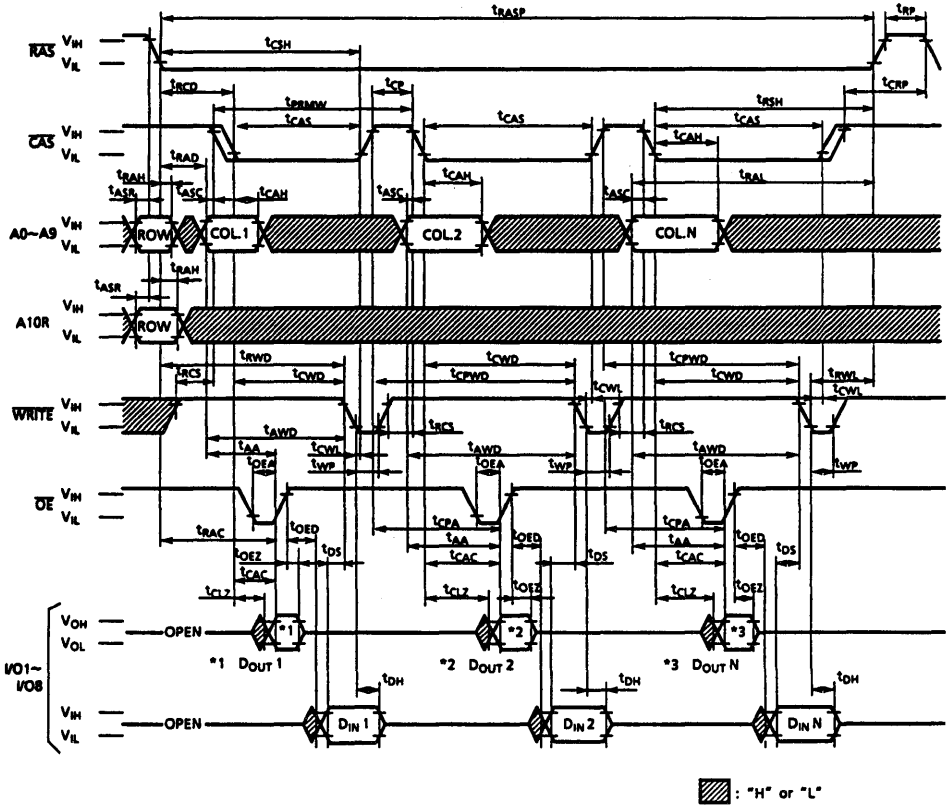
FAST PAGE MODE WRITE CYCLE



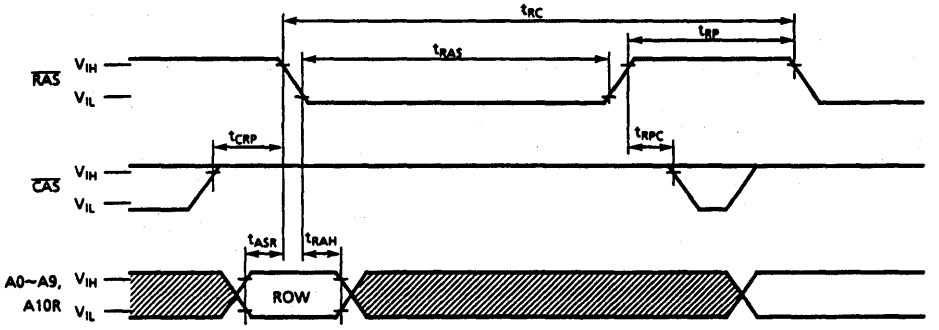
Note : D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



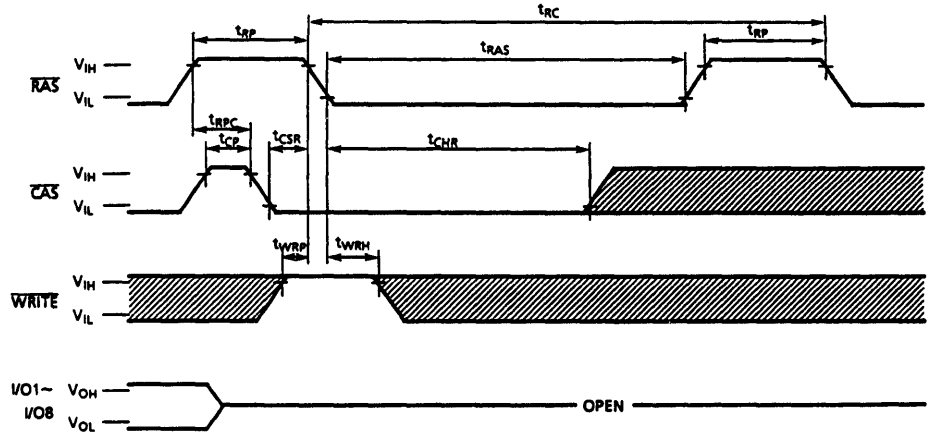
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$, D_{IN} = "H" or "L"
D_{OUT} = OPEN

▨ : "H" or "L"

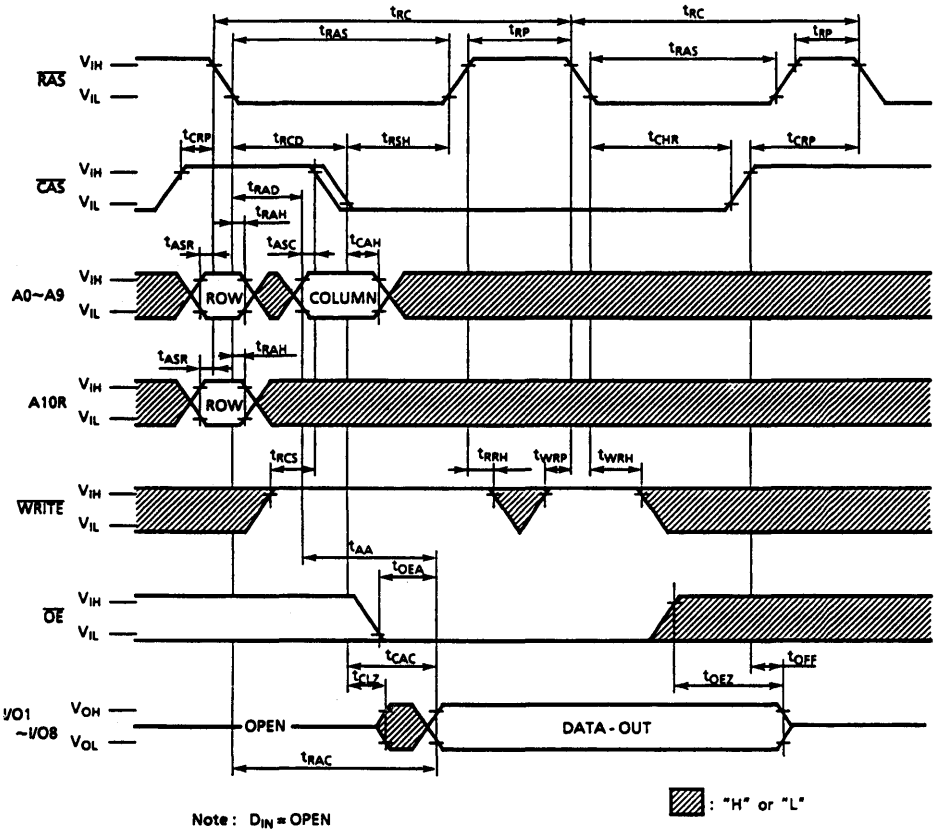
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9, A10R = "H" or "L"

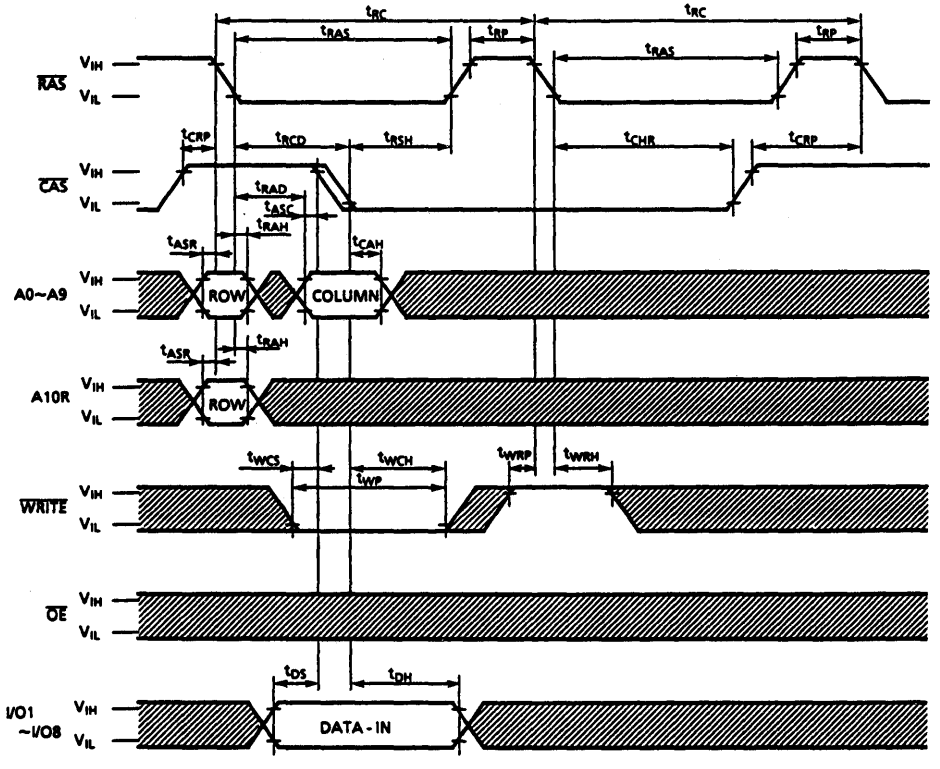
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)



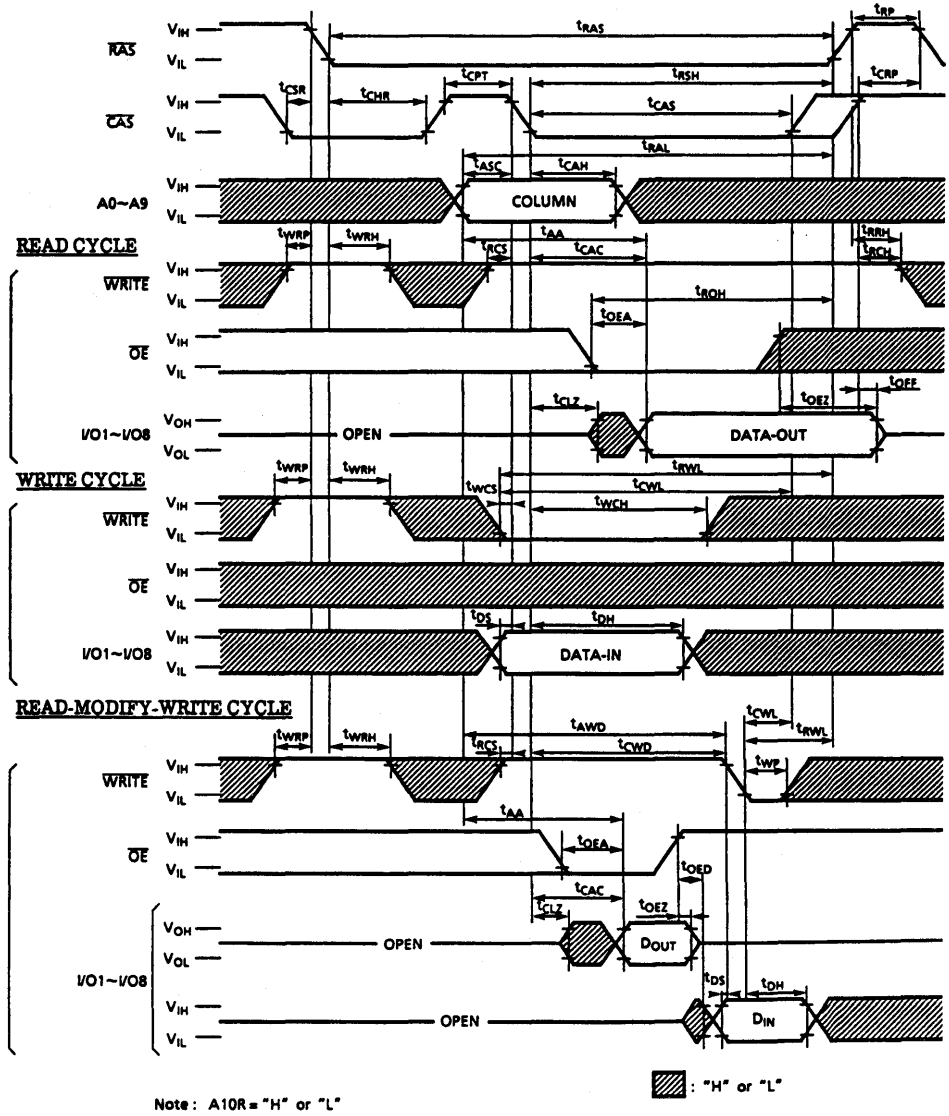
Note : D_{IN} = OPEN

HIDDEN REFRESH CYCLE (WRITE)



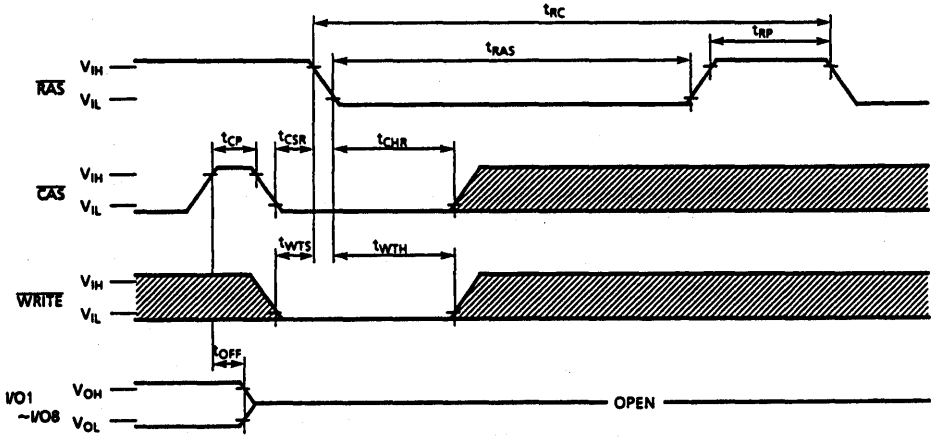
Note : D_{OUT} = OPEN

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



Note: A10R = "H" or "L"

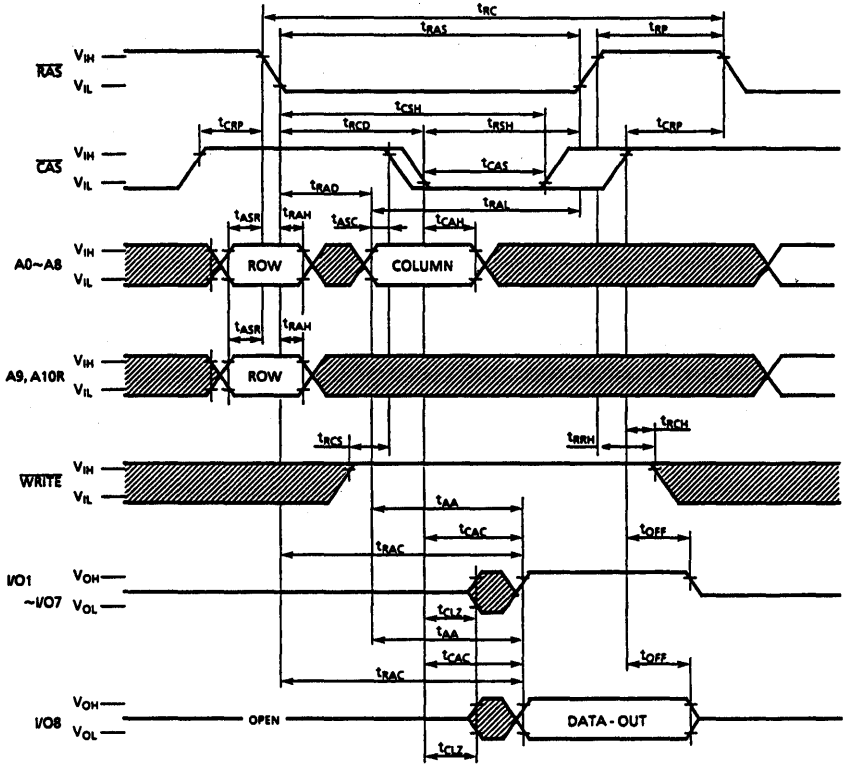
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9, A10R = "H" or "L"

▨: "H" or "L"

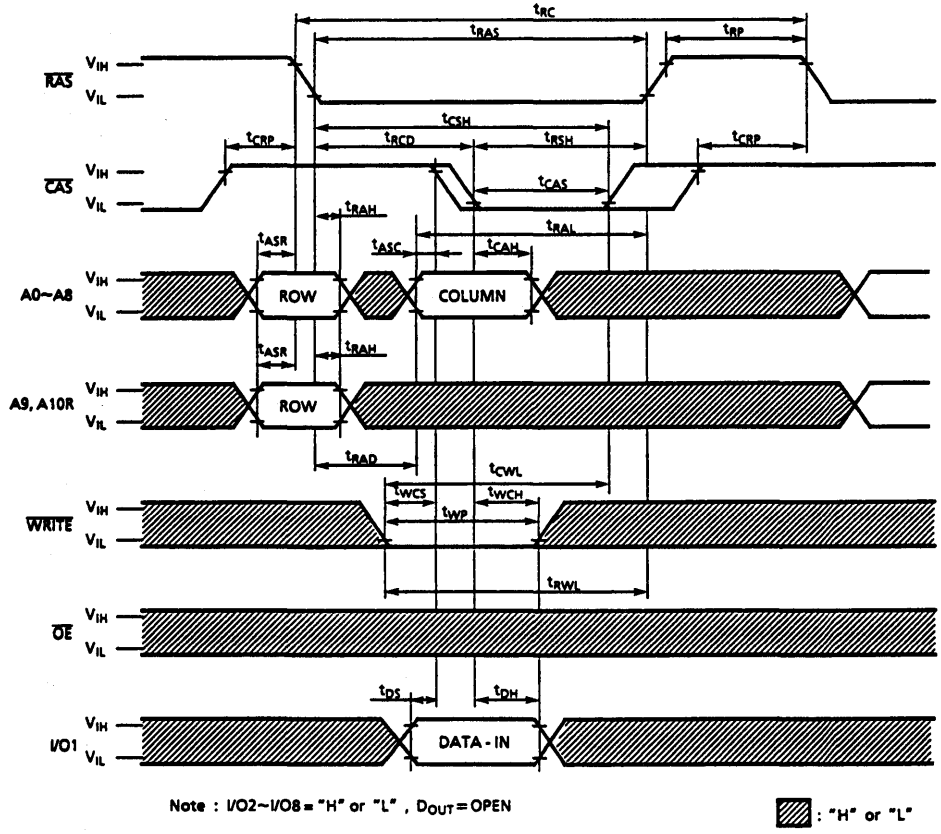
READ CYCLE IN THE TEST MODE



Note : $\overline{OE}$ = "L", D_{IN} = OPEN

▨: "H" or "L"

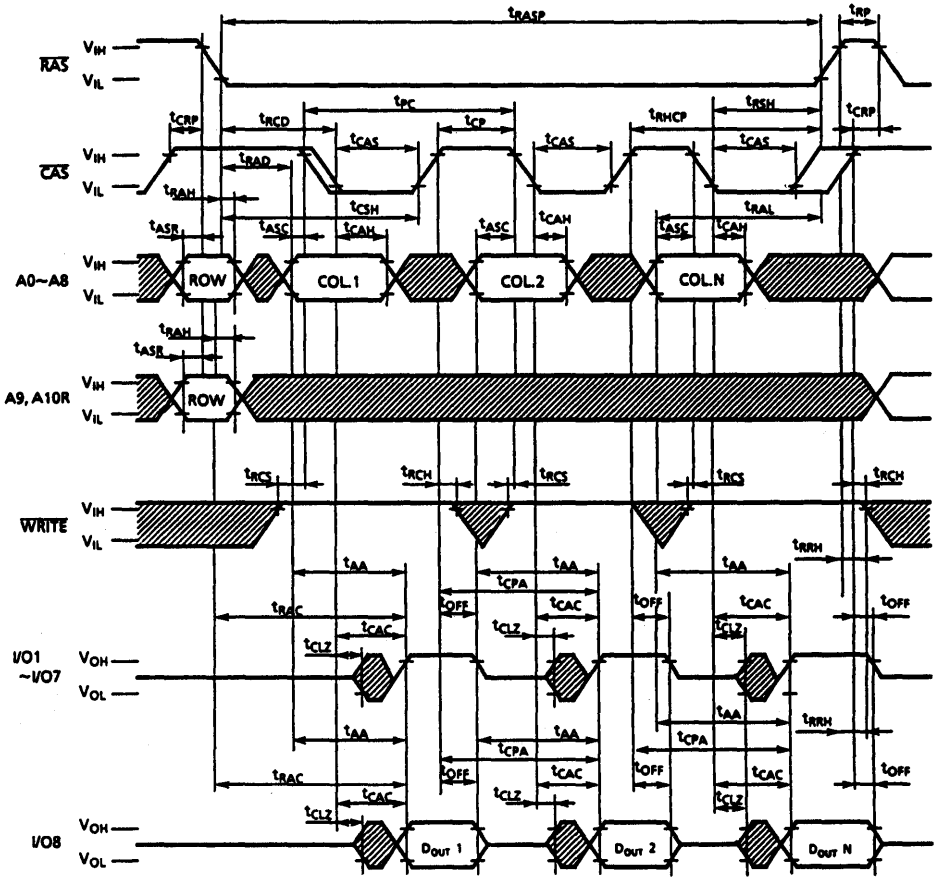
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note : I/O2~I/O8 = "H" or "L" , D_{OUT} = OPEN

▨ : "H" or "L"

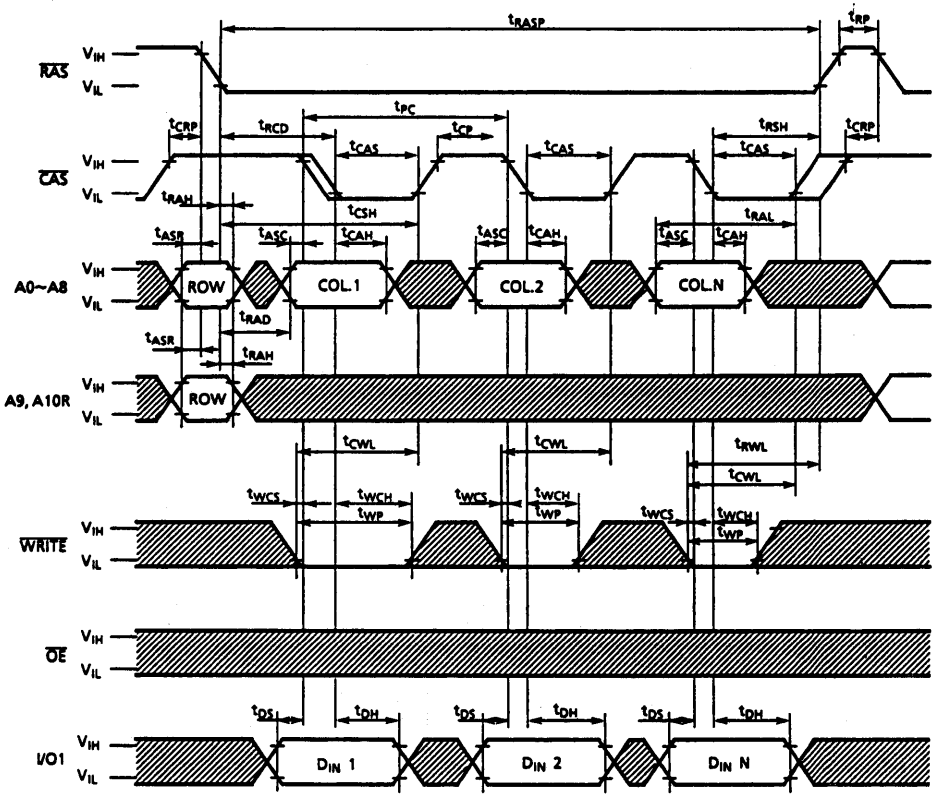
FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note : $\overline{OE}$ = "L", D_{IN} = OPEN

▨ : "H" or "L"

FAST PAGE MODE WRITE CYCLE IN THE TEST MODE



Note : I/O2~I/O8 = "H" or "L" , D_{OUT} = OPEN

TEST MODE

The TC5117800AJ/ANJ/AZ/ANZ/AFT/ANT/ATR/ANR is the RAM organized 2,097,152 words by8 bits; it is internally organized 1,048,576 words by16 bits. In "Test Mode", data are written into 16 sectors in parallel by using only I/01. A9C is not used. If, upon reading, 16 bits are equal (all "1"s or "0"s), the I/O8 pin indicates a "1".

If they were not equal, the I/O8 pin would indicate a "0". Other I/O pins (I/01~I/07) always indicate a "1" during test mode read cycle. Fig. 1 shows the block diagram of TC5117800AJ/ANJ/AZ/ANZ/AFT/ANT/ATR/ANR. In "Test Mode", the 2MX8 DRAM can be tested as if it were a 1MX16 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

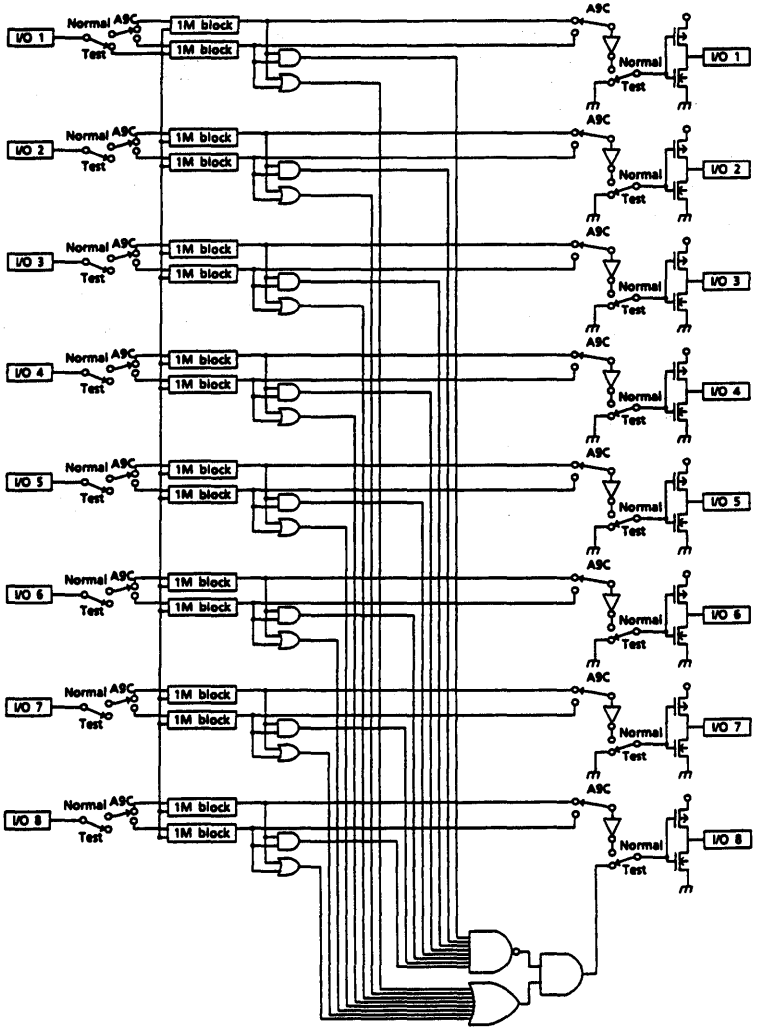


Figure 1

524,288 WORD X 9 BIT DYNAMIC RAM

DESCRIPTION

The TC514900AJ/AFT is the new generation dynamic RAM organized 524,288 word by 9 bit. The TC514900AJ/AFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514900AJ/AFT to be packaged in a standard 28 pin plastic SOJ, and 28 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 524,288 word by 9 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  633mW MAX .Operating
  (TC514900AJ/AFT-70)
  550mW MAX. Operating
  (TC514900AJ/AFT-80)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC514900AJ : SOJ28-P-400
  TC514900AFT : TSOP28-P-400

KEY PARAMETERS

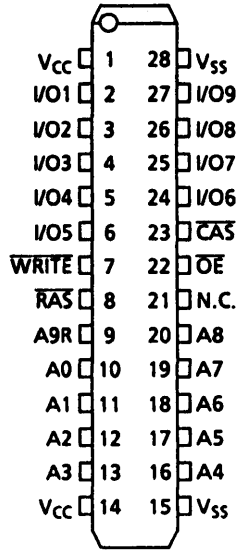
ITEM		TC514900AJ/AFT	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

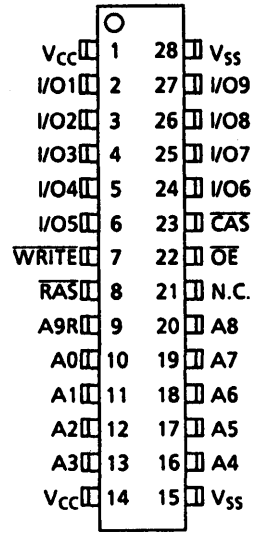
A0~A8, A9R	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O9	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

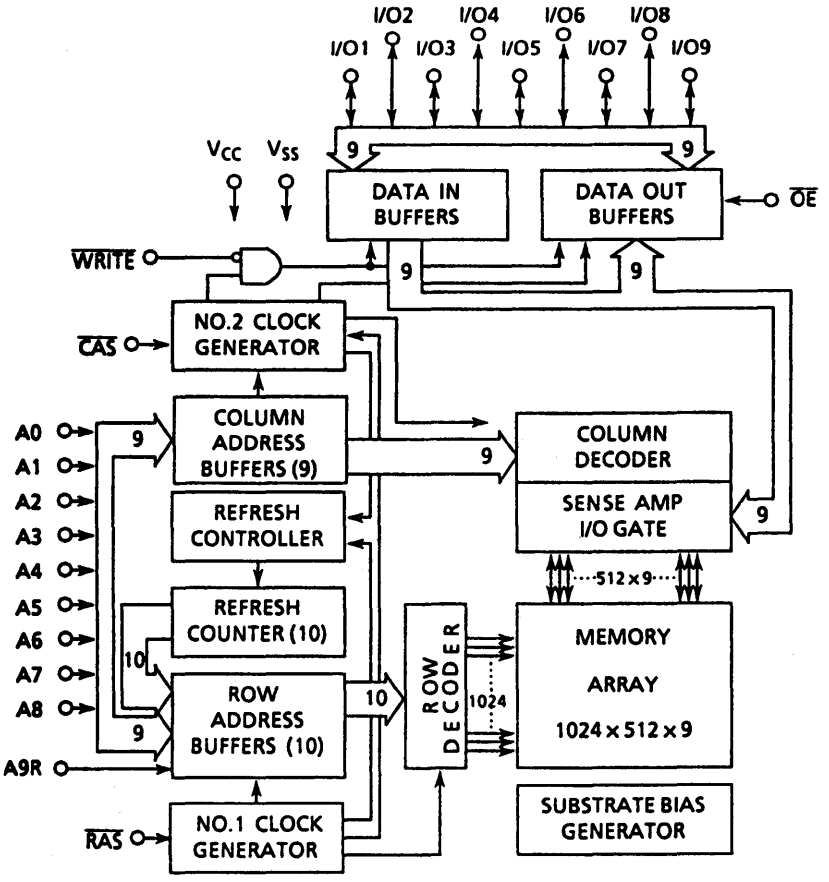
Plastic SOJ



Plastic TSOP
(Normal Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6..5	V	2
V_{IL}	Input Low Voltage (A0~A8,A9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-1.0*1	-	0.8	V	2
V_{IL}	Input Low Voltage ($\overline{I/O}$~$\overline{I/O9}$)	-0.5*2	-	0.8	V	2

*1 -2.5V at pulse width ≤ 20ns
*2 -2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514900AJ/AFT-70 TC514900AJ/AFT-80	- -	115 100	mA	3,4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514900AJ/AFT-70 TC514900AJ/AFT-80	- -	115 100	mA	3,5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC}MIN.)	TC514900AJ/AFT-70 TC514900AJ/AFT-80	- -	80 70	mA	3,4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$,Cycling: t_{RC}=t_{PC} MIN.)	TC514900AJ/AFT-70 TC514900AJ/AFT-80	- -	115 100	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	µA	
V_{OH}	OUTPUT CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT CURRENT Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC514400ASJL/AFTL/ATRL				UNIT	NOTES
		-70		-80			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	ns	
t_{AR}	Column Address Hold Time	55	-	60	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold TIme	15	-	15	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514273BJ				UNIT	NOTES
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	15	-	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	-	110	-	ns	15
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	-	70	-	ns	15
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	75	-	ns	15
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to OE	10	-	10		ns	
t_{OEA}	$\overline{OE}$ Access TIme	-	20	0	20	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A8, A9R)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$))	-	7	pF
C_O	Input Capacitance (I/O1~I/O9)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieveS the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

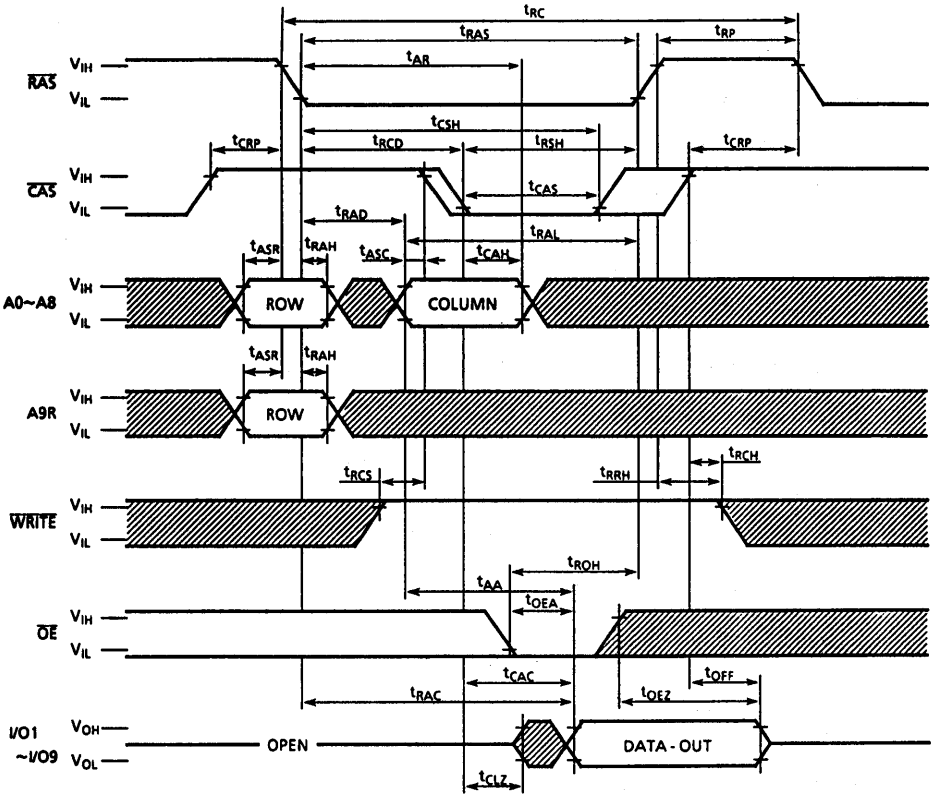
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the date sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

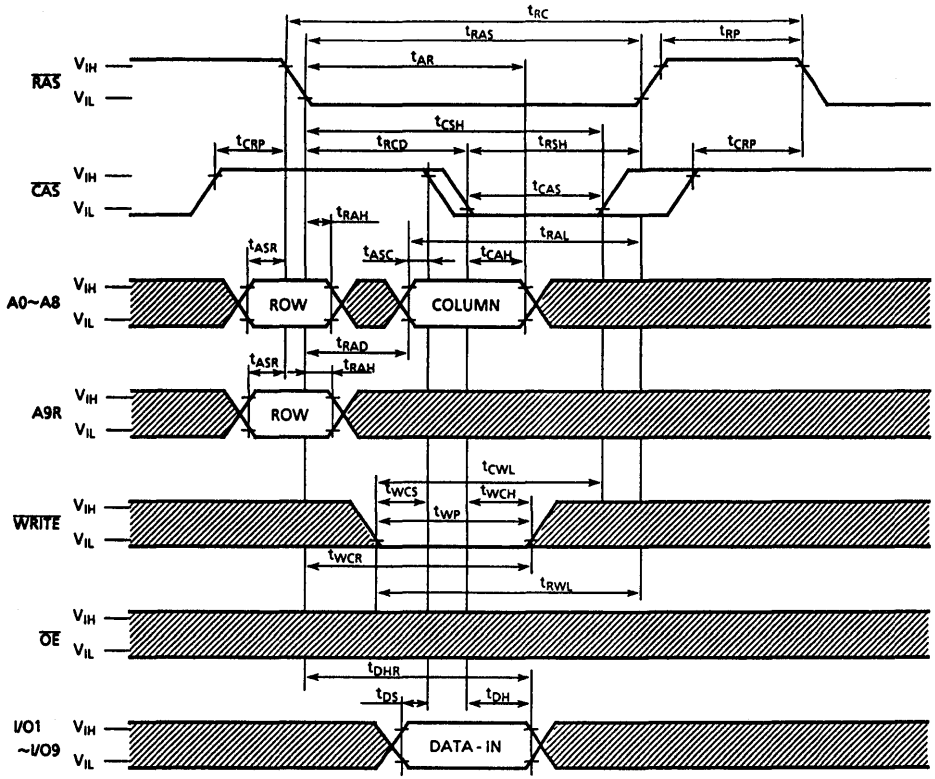
READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

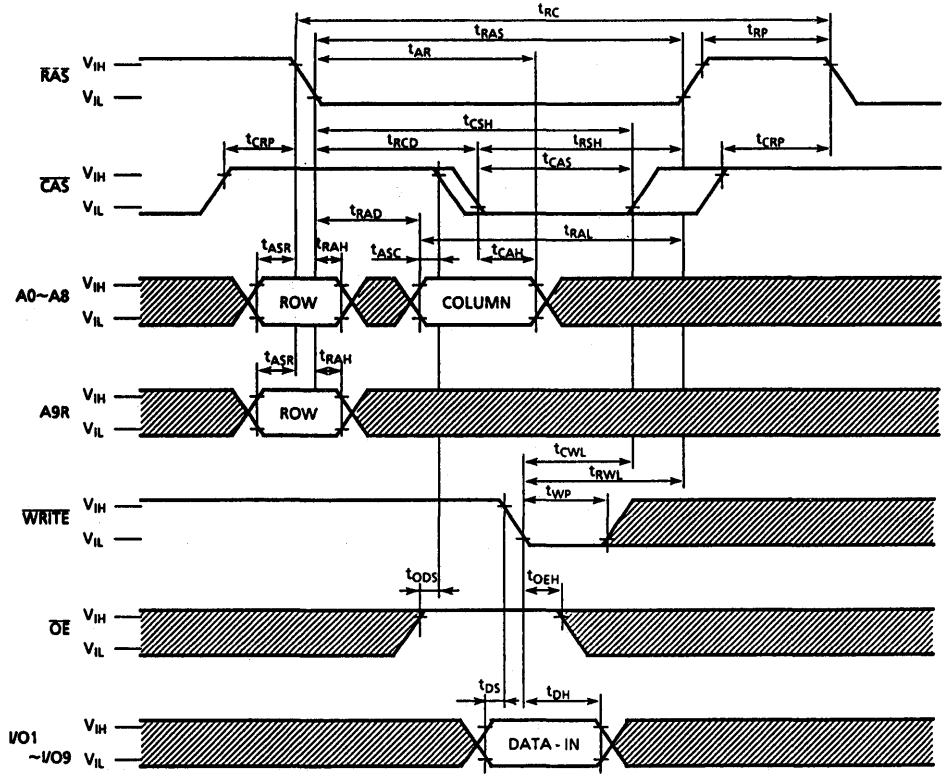
WRITE CYCLE (EARLY WRITE)



Note : D_{OUT} = OPEN

▨ : "H" or "L"

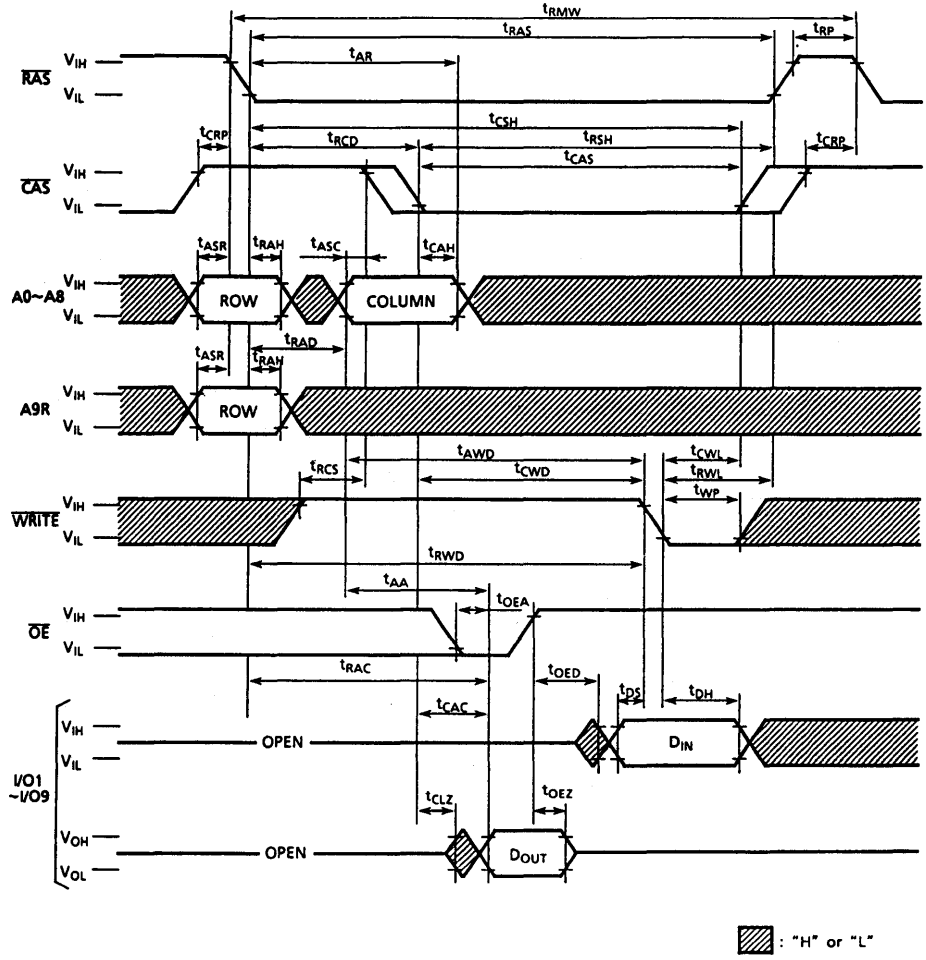
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



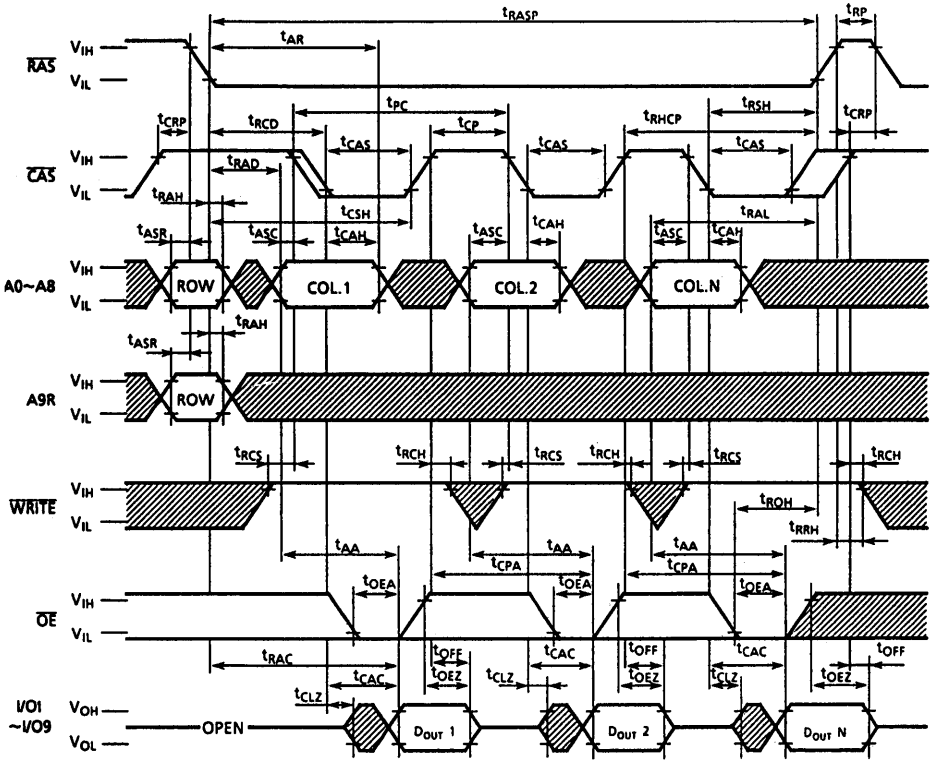
Note : D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



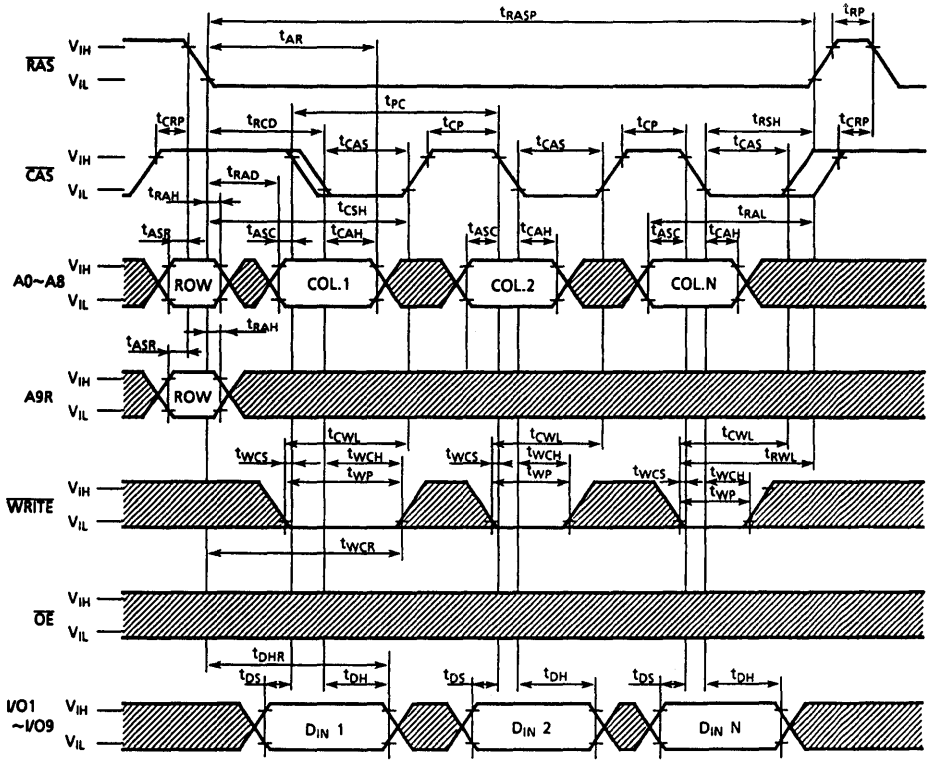
FAST PAGE MODE READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

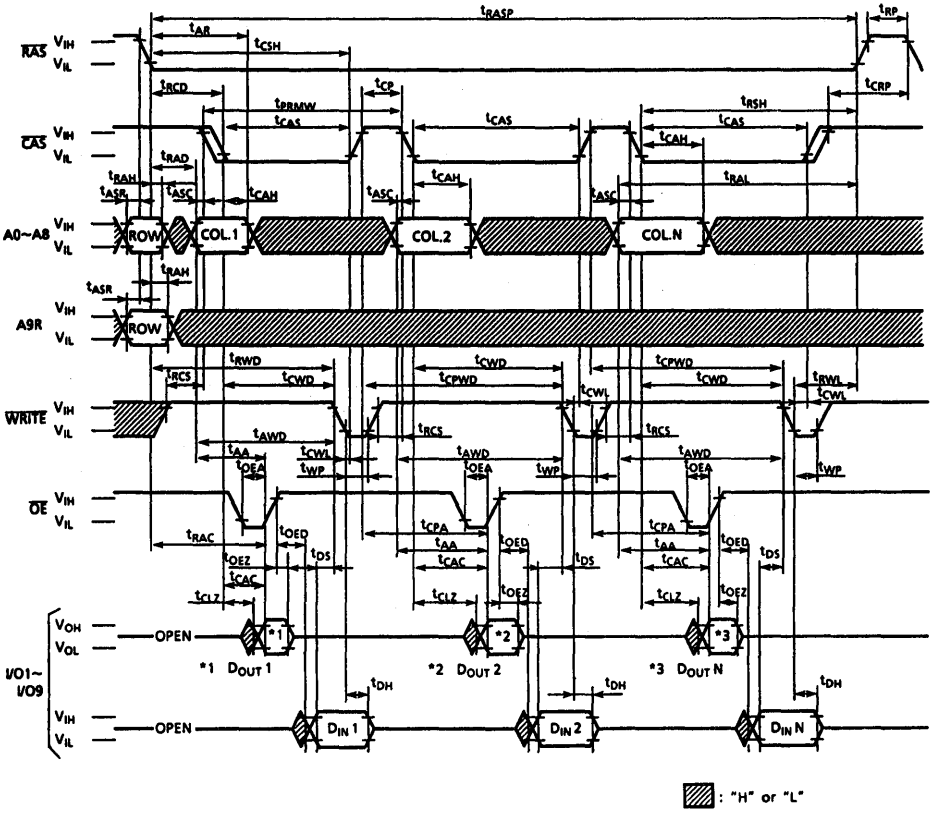
FAST PAGE MODE WRITE CYCLE



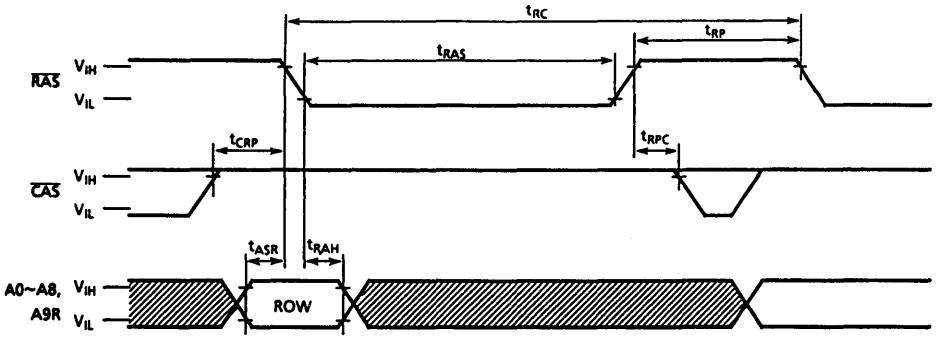
Note : D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



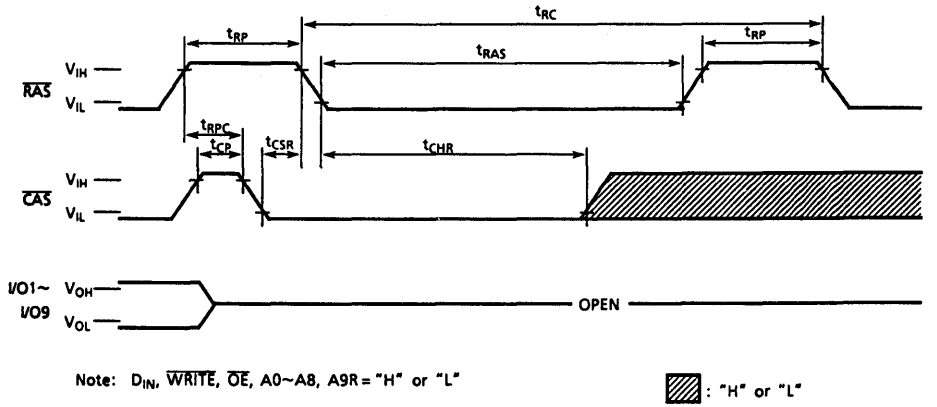
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$, D_{IN} = "H" or "L"
D_{OUT} = OPEN

▨: "H" or "L"

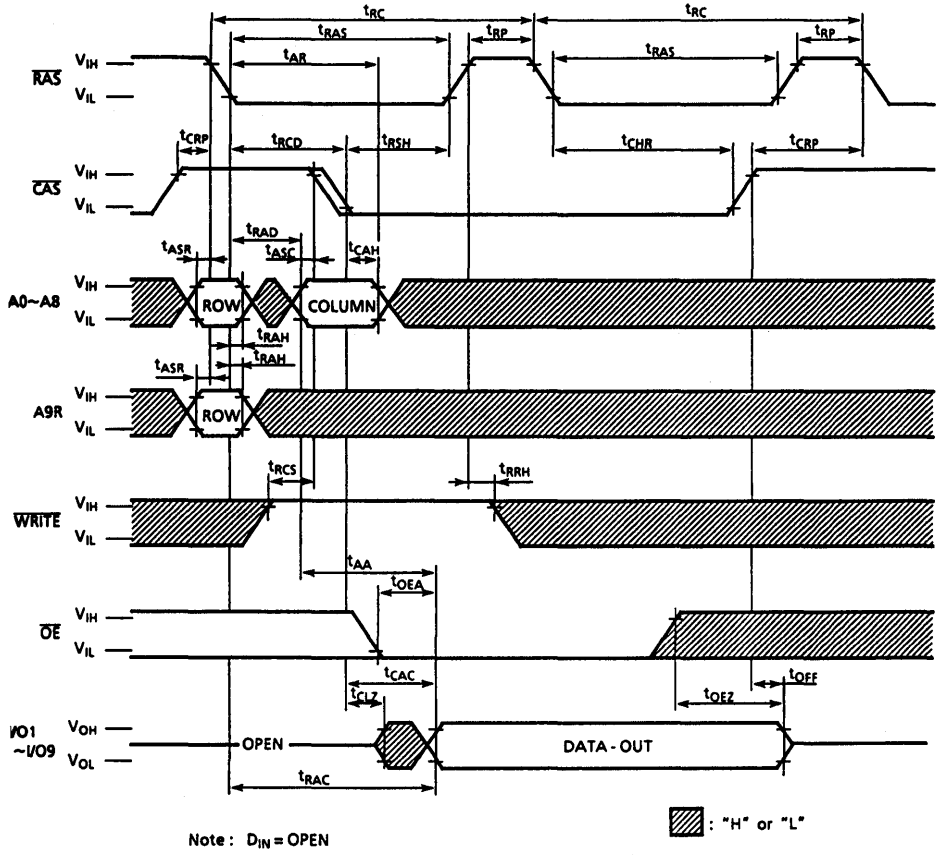
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$, A0~A8, A9R = "H" or "L"

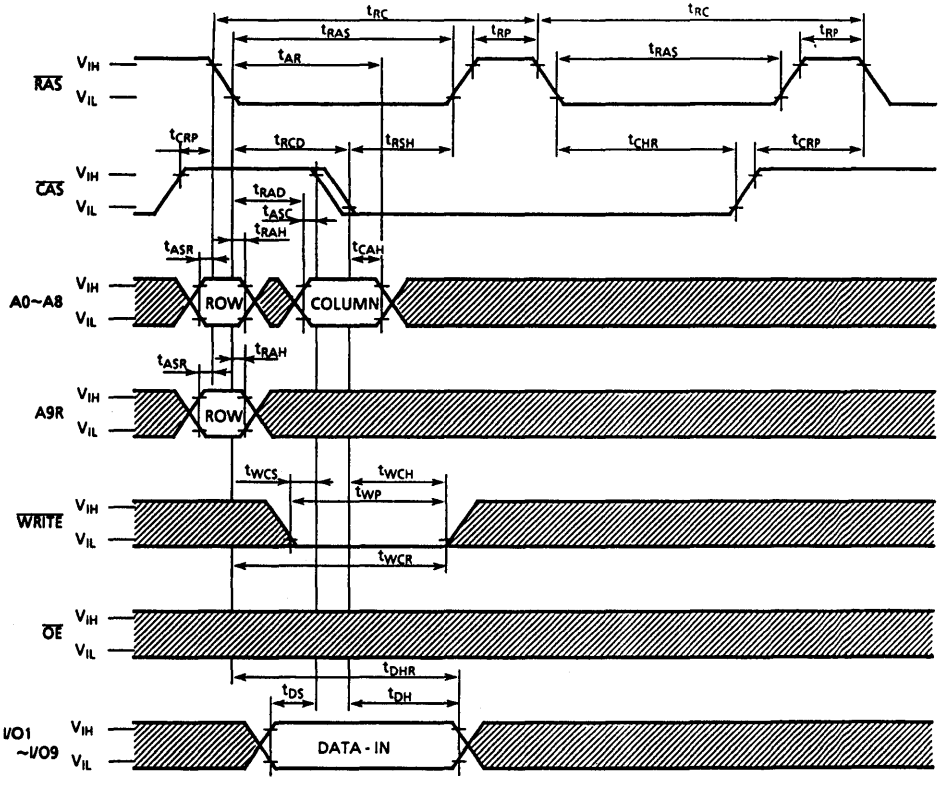
▨: "H" or "L"

HIDDEN REFRESH CYCLE (READ)



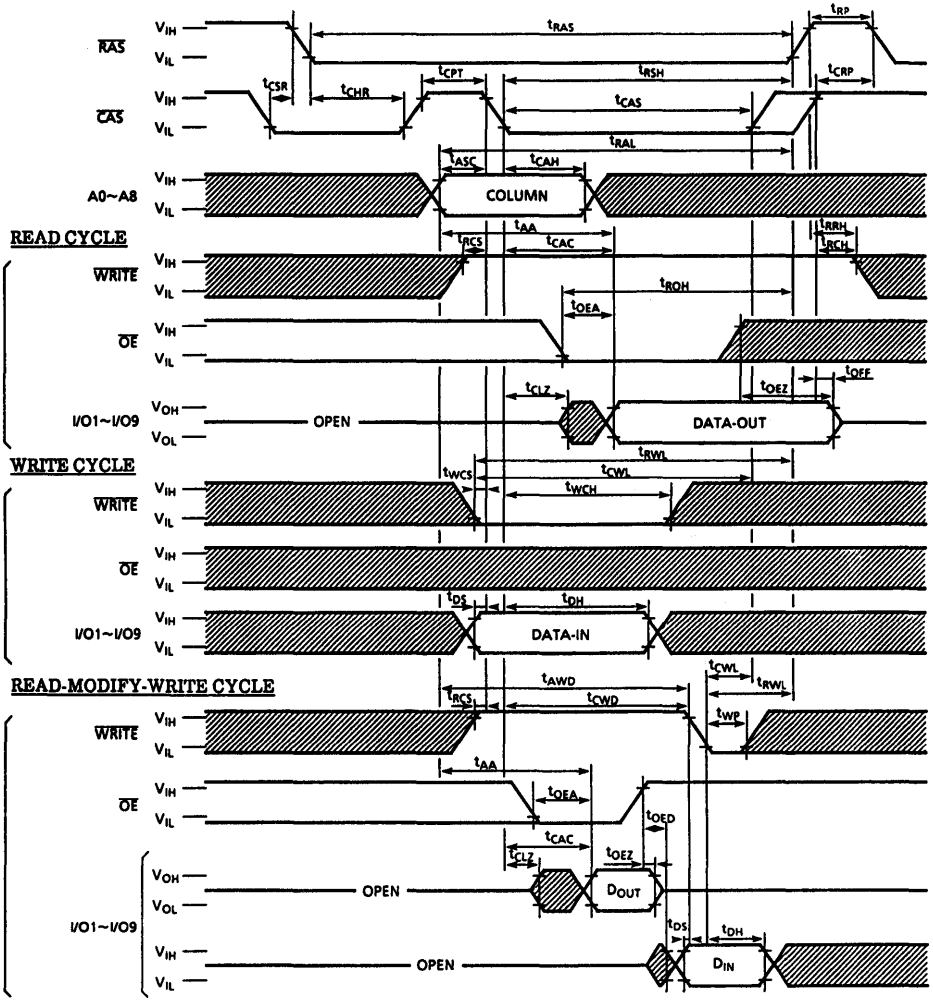
Note : D_{IN} = OPEN

HIDDEN REFRESH CYCLE (WRITE)



Note : D_{OUT} = OPEN

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



Note : A9R = "H" or "L"

APPLICATION INFORMATION

ADDRESSING

The 19 address bits required to decode 1 of the 524,288 cell locations within the TC514900AJ/AFT are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing $\overline{WRITE}$ low during the $\overline{RAS}/\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or $\overline{WRITE}$ stobes data on I/O1~I/O9 into the on-chip data latch. In an early write cycle, $\overline{WRITE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In delayed write or read modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WRITE}$ with setup and hold times referenced to these signals.

In delayed or read modify write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data Ouputs

The three state output buffers provide direct TTL compatibility with a fan-out of standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ imput is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 1024 row addresses (A0~A8, A9R) within each 16 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

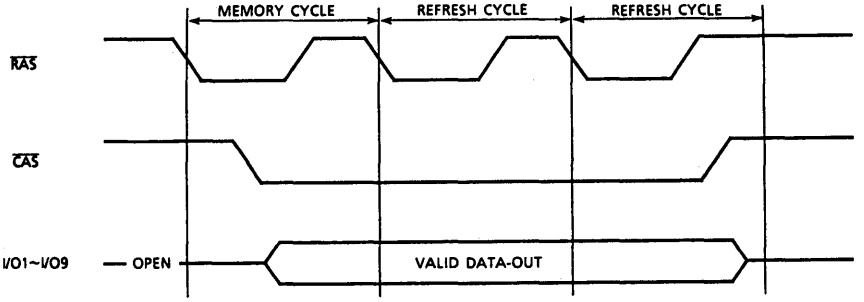
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514900AJ/AFT offers an alternate refresh method. If $\overline{CAS}$ is hold on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh opeation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC514900AJ/AFT allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514900AJ/AFT is the refresh cycles may be performed while maintaining valid data at the output pins. This referred to as Hidden Refresh. Hidden Refresh is perfomed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC514900AJ/AFT can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle as initialization cycles. The test procedure is as follows.

1. Write "0" into all the memory cells normal write mode.
2. Select one certain column address and read "0" out and write "1' in each cell be performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 1024 times.
3. Check "1" out of 1024 bits at normal read mode , which was written at 2.
4. Using the same column as 2., read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat This operation 1024 times.
5. Check "0" out of 1024 bits as normal read mode, which was written at 4.
6. Perform the above 1. to 5. to the complement data.

524,288 WORD X 9 BIT DYNAMIC RAM

DESCRIPTION

The TC514900AJL is the new generation dynamic RAM organized 524,288 word by 9 bit. The TC514900AJL utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514900AJL to be packaged in a standard 28 pin plastic SOJ. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 524,288 word by 9 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  633mW MAX .Operating
  (TC514900AJL-70)
  550mW MAX. Operating
  (TC514900AJL-80)
  1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514900AJL : SOJ28-P-400

KEY PARAMETERS

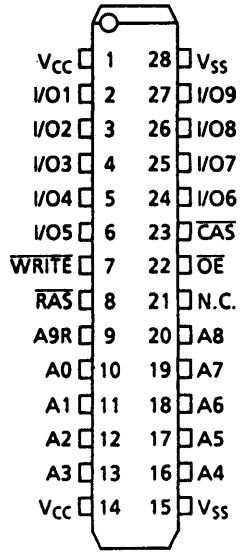
ITEM		TC514900AJL	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

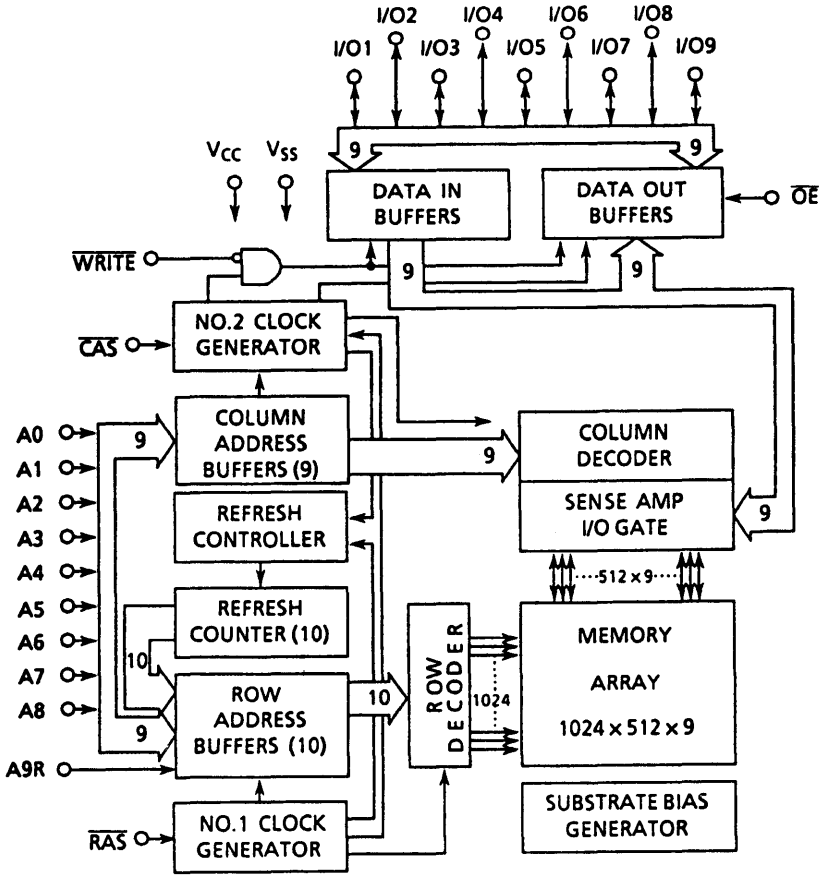
A0~A8 A9R	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O9	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

Plastic SOJ



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage (A0~A8, A9R, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$	-1.0*1	-	0.8	V	2
V_{IL}	Input Low Voltage (1/01~1/09)	-0.5*2	-	0.8	V	2

*1-2.5V at pulse width ≤ 20ns
*2-2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514900AJL-70	-	115	mA	3,4 5
		TC514900AJL-80	-	100		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514900AJL-70	-	115	mA	3, 5
		TC514900AJL-80	- -	100		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling:t_{PC}=t_{PC} MIN.)	TC514900AJL-70	-	80	mA	3,4 5
		TC514900AJL-80	- -	70		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	200	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC514900AJL-70	-	115	mA	3
		TC514900AJL-80	- -	100		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, Battery back up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} -0.2V or 0.2V, $\overline{WRITE}$ = V_{CC}-0.2V or 0.2V, A0~A9 = V_{CC} -0.2V or 0.2V, 1/01~ 9 = V_{CC}-02V, 0.2V or OPEN : t_{RC}=125µ5, t_{RAS} = t_{RAS} MIN~1µ5)	TC514900AJL-70	-	300	µA	3,6
		TC514900AJL-80				
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN} ≤ 6.5V, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT} ≤ 5.5V)		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 7,8,9)

SYMBOL	PARAMETER	TC514900AJL				UNIT	NOTE
		-70		-80			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	10, 15,16
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	10, 15
t_{AA}	Access Time from Column Address	-	35	-	40	ns	10, 16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	10
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514900AJL				UNIT	NOTE
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	15	-	15	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	13
t_{DH}	Data Hold Time	15	-	15	-	ns	13
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	
t_{REF}	Refresh Period	-	128	-	128	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	-	110	-	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	-	70	-	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	75	-	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	40	-	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	20	ns	10
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	11
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A8, A9R)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input Capacitance (I/O1~I/O9)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. t_{RAS} (max.) = 1μs is only applied to refresh of battery-back up. t_{RAS} (max.) = 10μs is applied to functional operating.

7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

8. AC measurements assume t_T=5ns.

9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

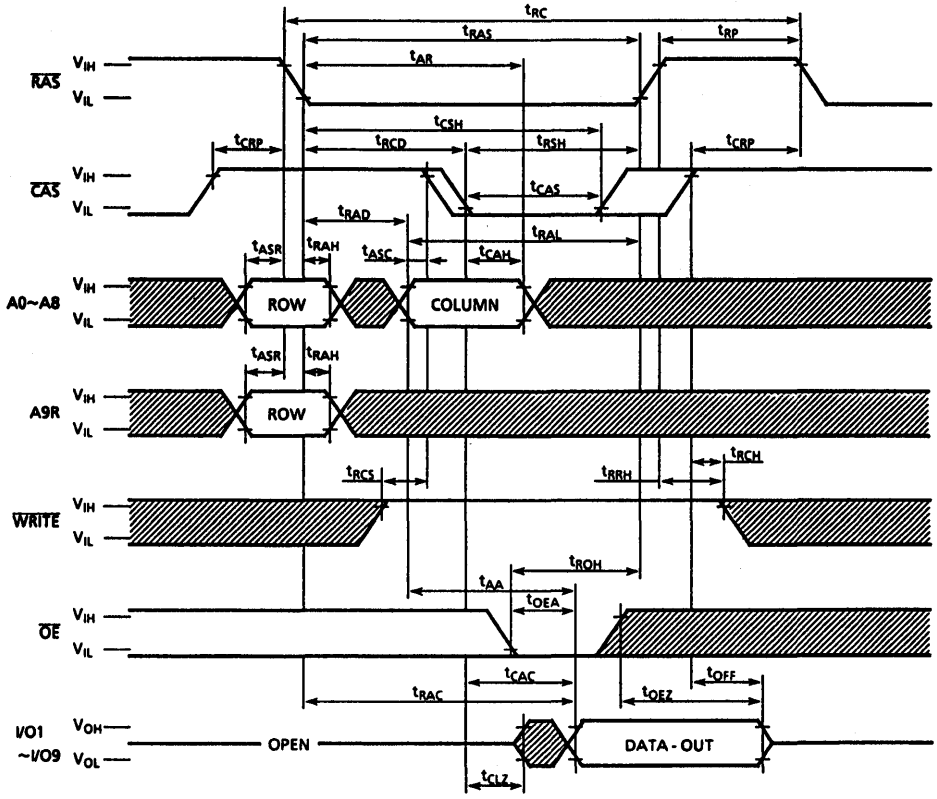
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWD} > t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

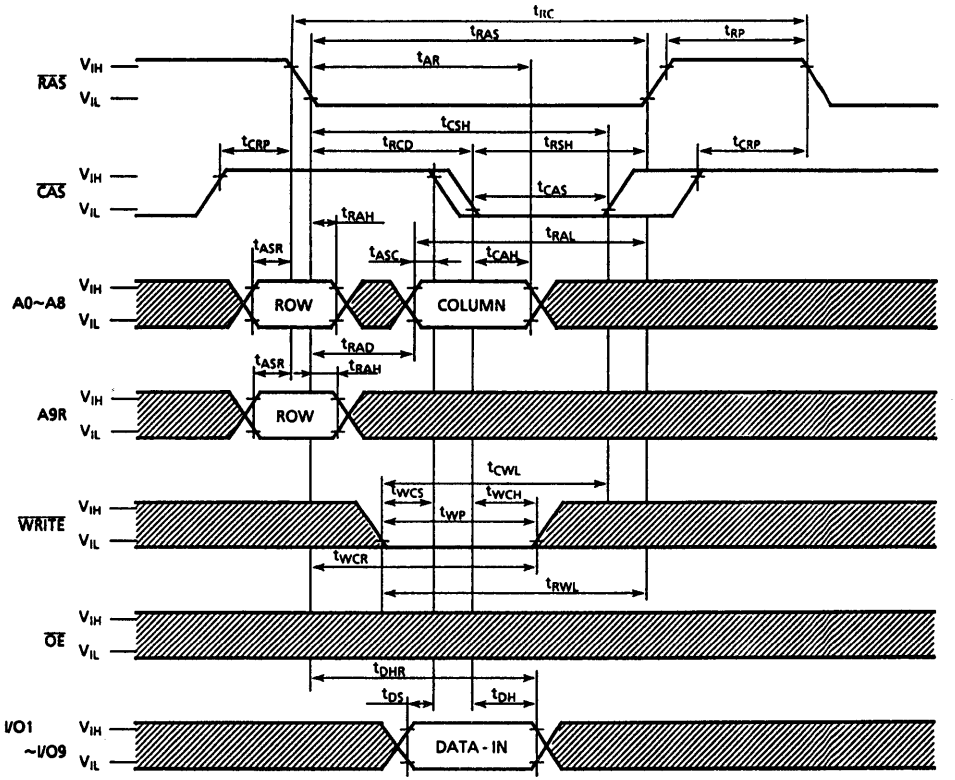
READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

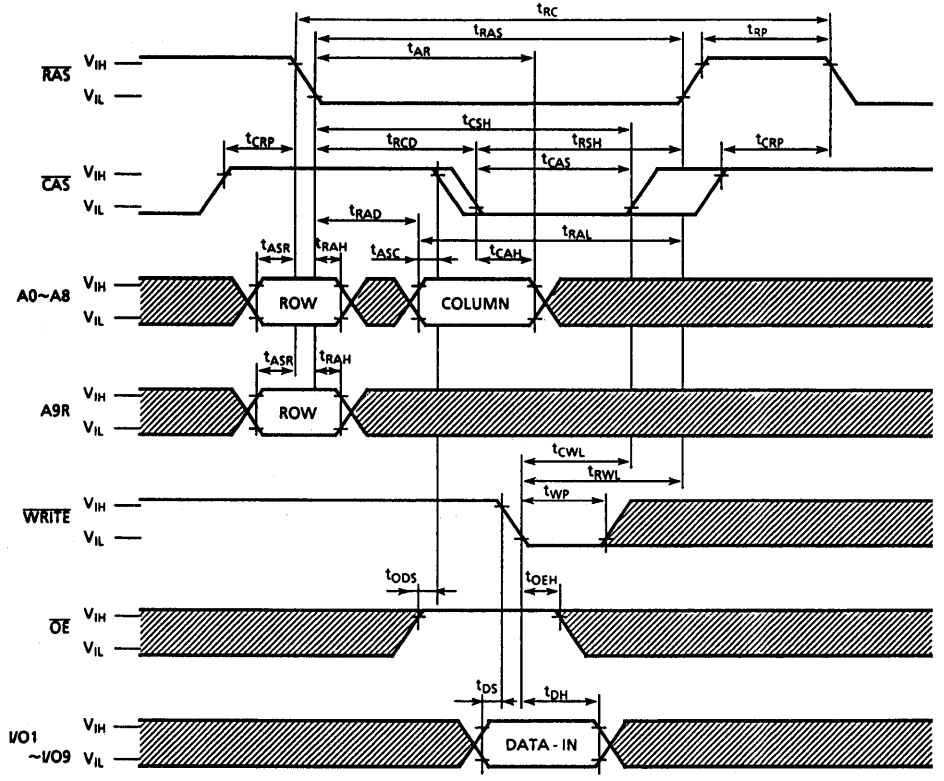
WRITE CYCLE (EARLY WRITE)



Note : D_{OUT} = OPEN

▨ : "H" or "L"

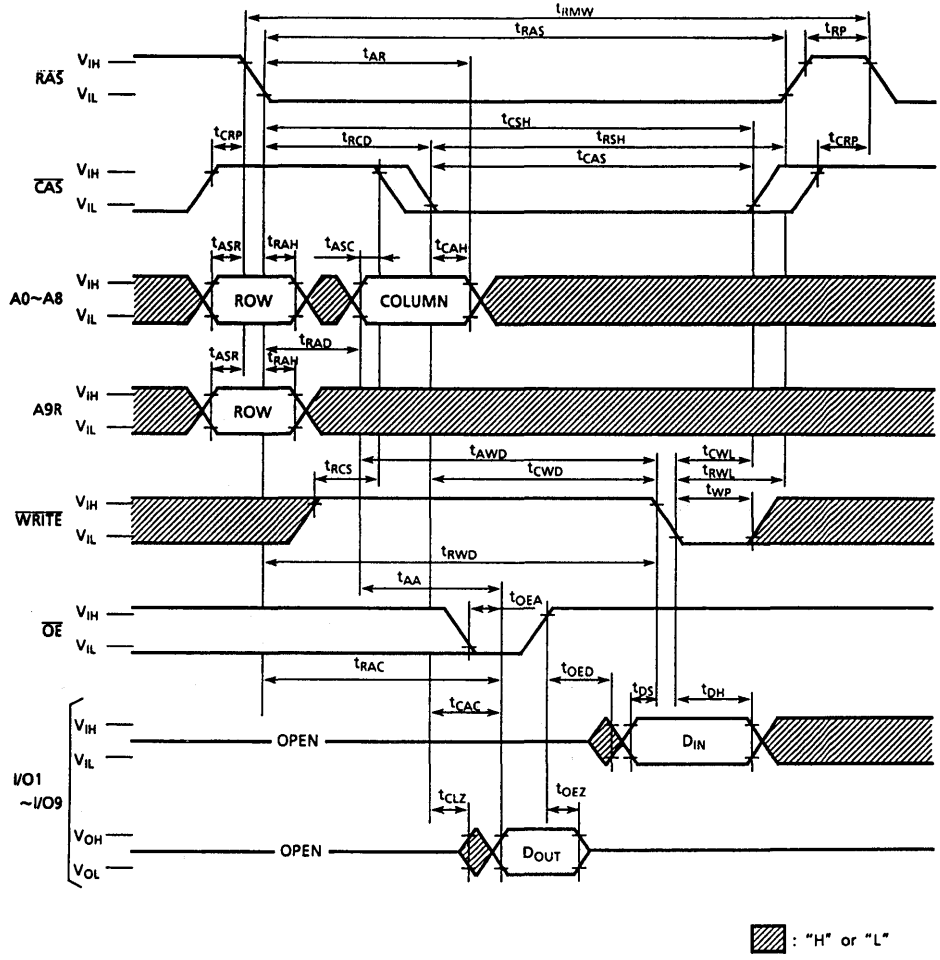
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



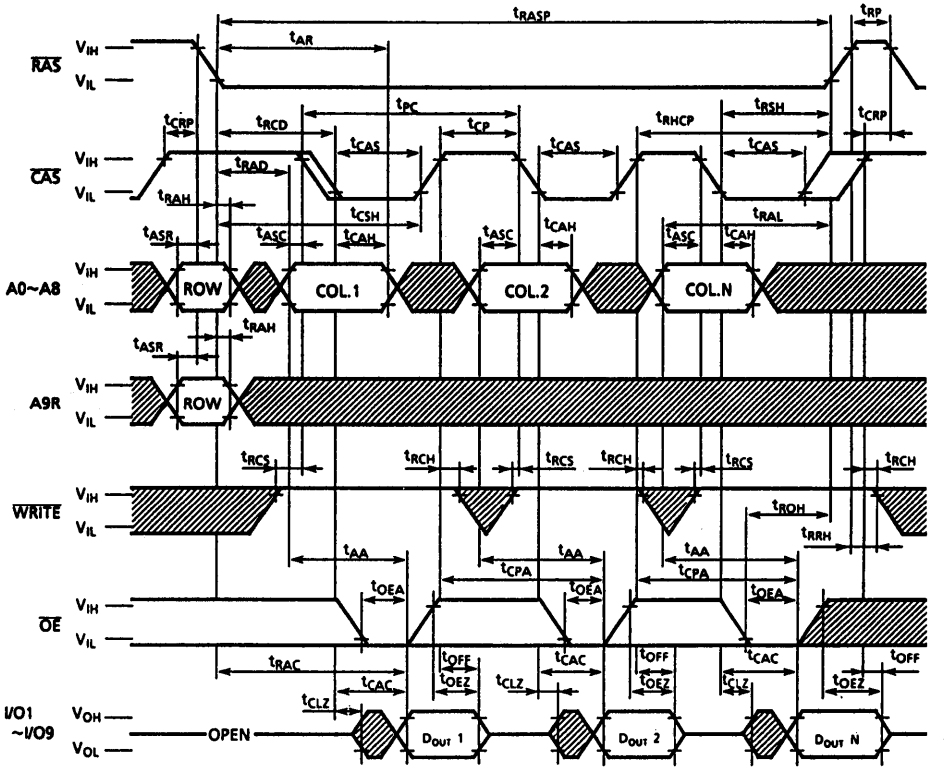
Note : D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



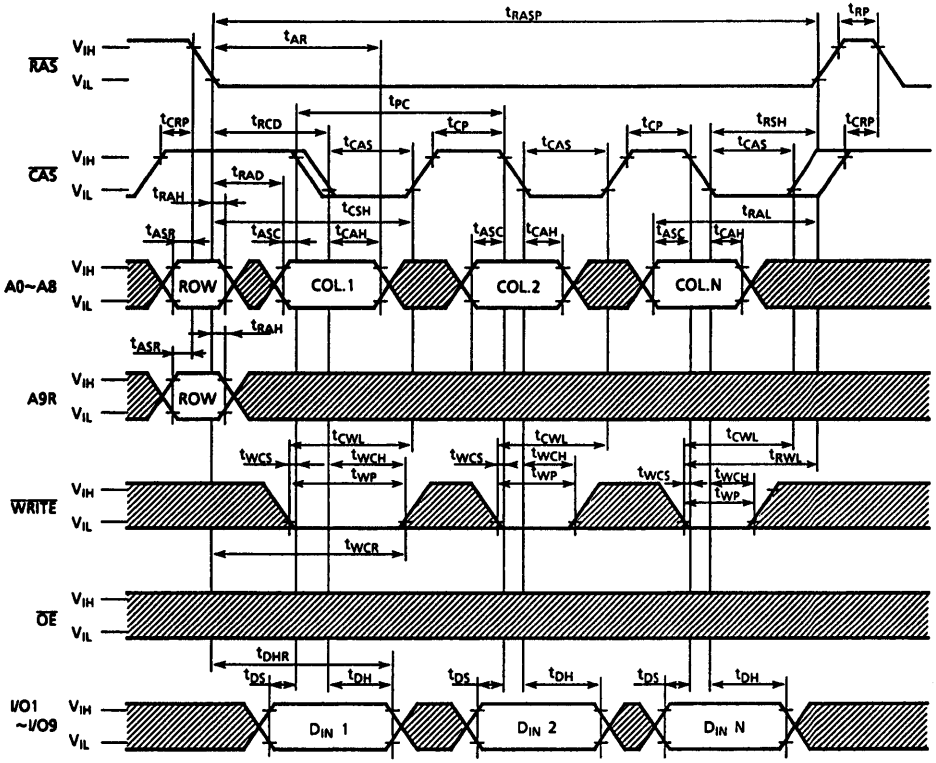
FAST PAGE MODE READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

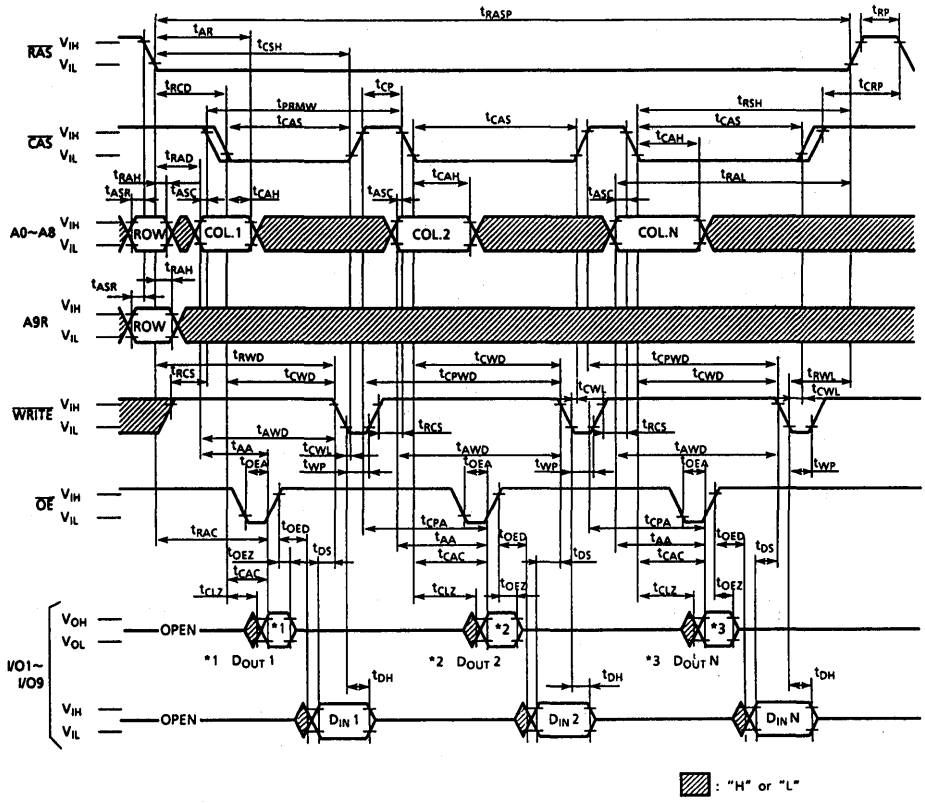
FAST PAGE MODE WRITE CYCLE



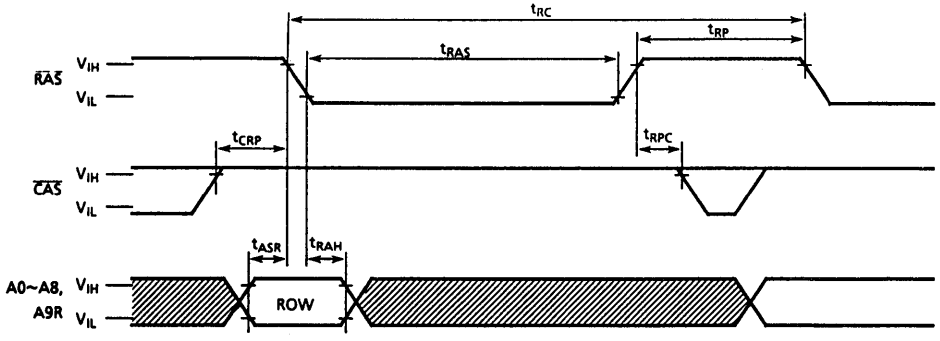
Note : D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



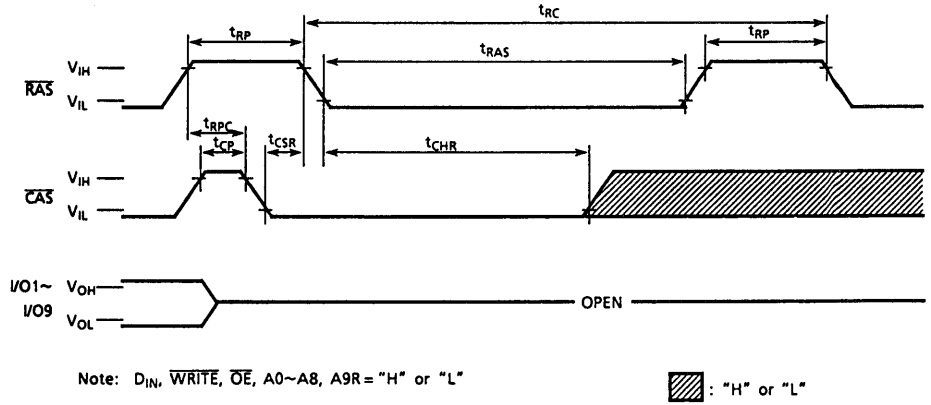
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$, D_{IN} = "H" or "L"
D_{OUT} = OPEN

▨ : "H" or "L"

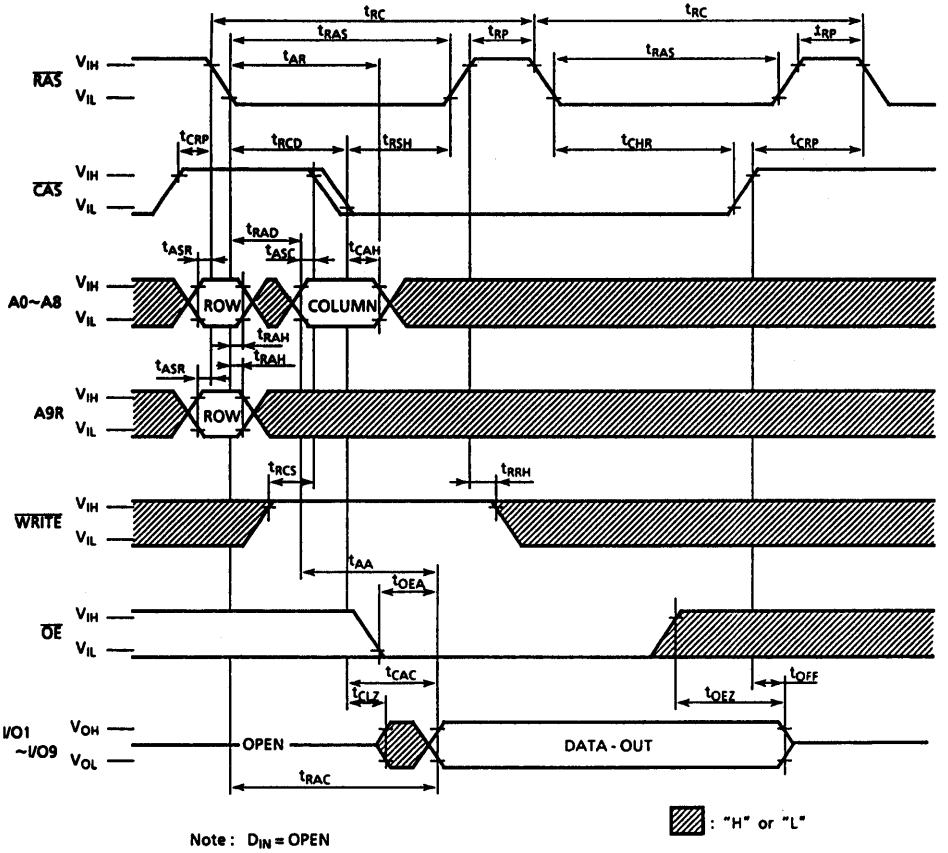
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$, A0~A8, A9R = "H" or "L"

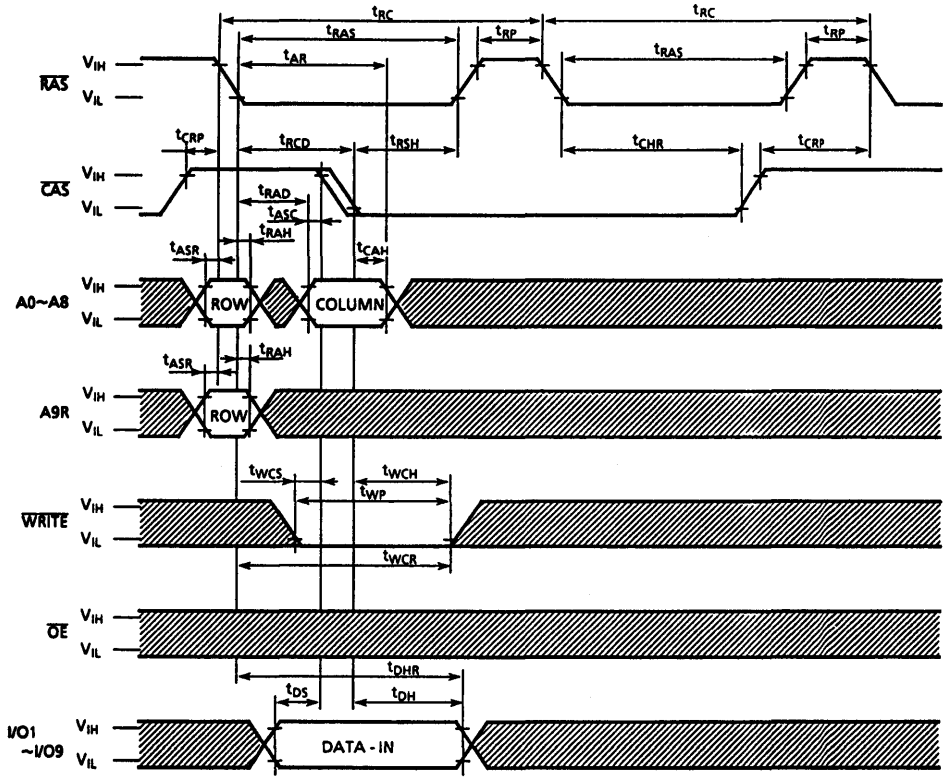
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)



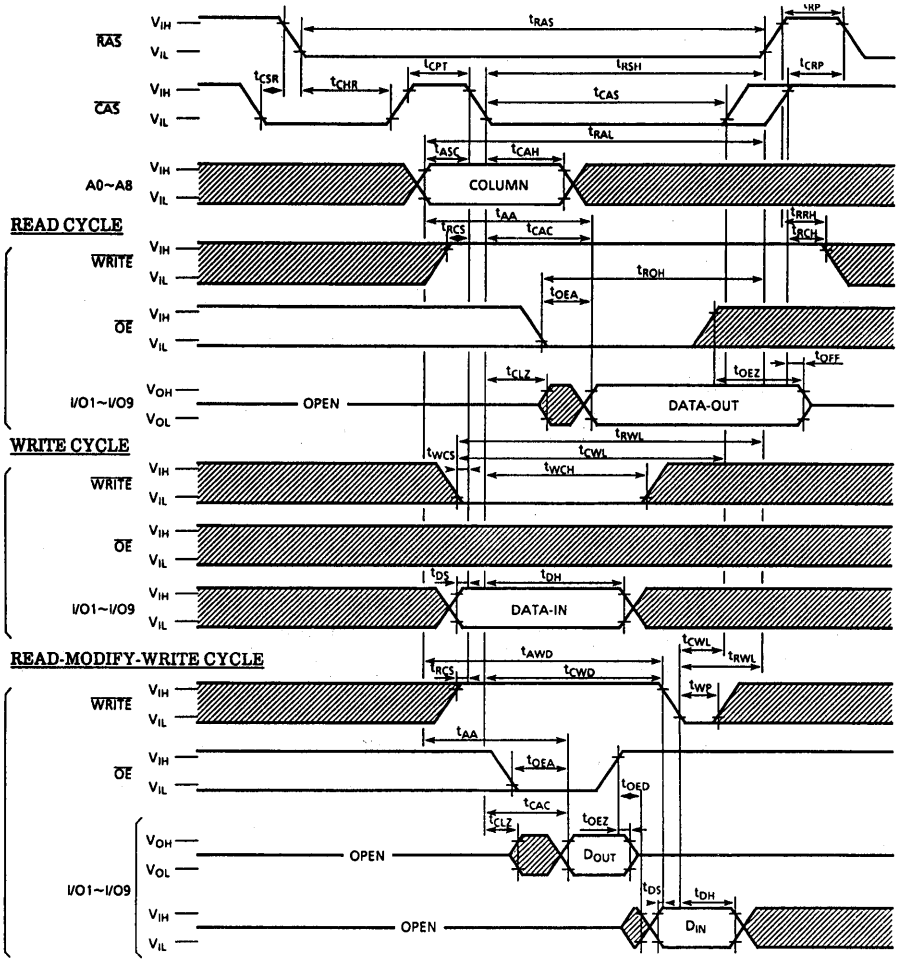
Note : D_{IN} = OPEN

HIDDEN REFRESH CYCLE (WRITE)



Note : D_{OUT} = OPEN

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



Note : A9R = "H" or "L"

APPLICATION INFORMATION

ADDRESSING

The 19 address bits required to decode 1 of the 524,288 cell locations within the TC514900AJL are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUTS

A write cycle is performed by bringing $\overline{WRITE}$ low during the $\overline{RAS}/\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or $\overline{WRITE}$ strobes data on I/O1~I/O9 into the on-chip data latch. In an early write cycle, $\overline{WRITE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In delayed write or read modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WRITE}$ with setup and hold times referenced to these signals.

In delayed or read modify write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

DATA OUTPUTS

The three-state output buffers provide direct TTL compatibility with a fan-out of a standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high impedance state until CAS is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In a delayed write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 1024 row addresses (AO~A8, A9R) within each 16 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

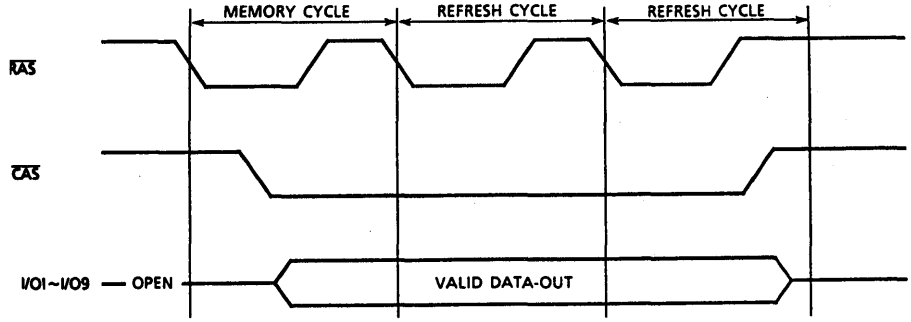
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514900AJL offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC514900AJL allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514900AJL is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC514900AJL can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST." This cycle performs READ/WRITE operation taking internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows:

- 1. Write "0" into all the memory cells normal write mode.
- 2. Select one certain column address and read "0" out and write "1" in each cell by performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)."
- 3. Check "1" out of 1024 bits at normal read mode, which was written at ≠.
- 4. Using the same column as ≠, read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST." Repeat this operation 1024 times.
- 5. Check "0" out of 1024 bits at normal read mode, which was written at √.

6. Perform the above ÷ to f to the complement data.

524,288 WORD X 9 BIT DYNAMIC RAM

DESCRIPTION

The TC514900AJLL is the new generation dynamic RAM organized 524,288 word by 9 bit. The TC514900AJLL utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514900AJLL to be packaged in a standard 28 pin plastic SOJ. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 524,288 word by 9 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  663mW MAX .Operating
  (TC514900AJLL-70)
  550mW MAX. Operating
  (TC514900AJLL-80)
  1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/128ms
- Package TC514400AJLL : SOJ28-P-400

KEY PARAMETERS

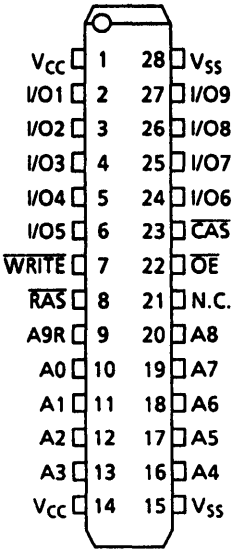
ITEM		TC514400AJLL	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

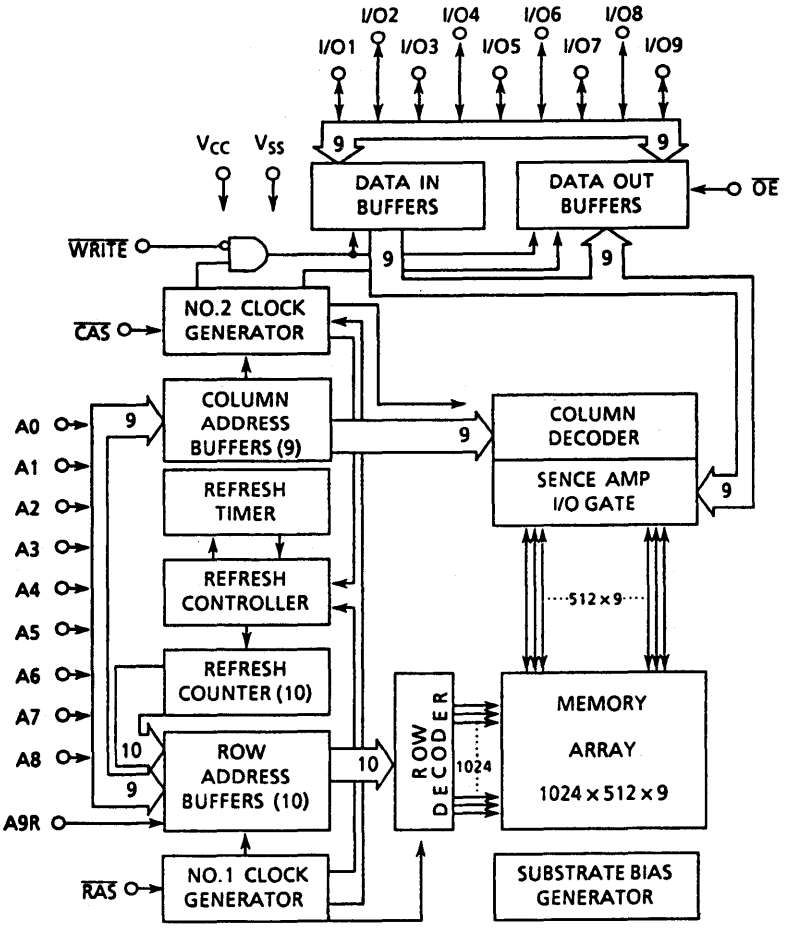
A0~A8, A9R	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O9	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

Plastic SOJ



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage (A0~A8,A9R, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$	-1.0*1	-	0.8	V	2
V_{IL}	Input Low Voltage ($\overline{I/O0~I/O9}$	-0.5*2	-	0.8	V	2

*1 -2.5V at pulse width ≤ 20ns
*2 -2.0V at pulse width ≤ 20ns

D.C. OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514100AJLL-70	-	115	mA	3,4 5
		TC514100AJLL-80	-	100		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514100AJLL-70	-	115	mA	3, 5
		TC514100AJLL-80	-	100		
			-			
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling:t_{PC}=t_{PC} MIN.)	TC514100AJLL-70	-	80	mA	3,4 5
		TC514100AJLL-80	-	70		
			-			
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			200	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC514100AJLL-70	-	115	mA	3
		TC514100AJLL-80	-	100		
			-			
I_{CC7}	BATTERY BACK UP CURRENT Average Power Suuply Current, Battery Back Up Mode ($\overline{RAS}$=$\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$=V_{CC}-0.2V or 0.2V, $\overline{WRITE}$ =V_{CC}-0.2V or 0.2V A0~A8, A9R=V_{CC}-0.2V or 0.2V, I/O~I/O9=Vcc-0.2V, 0.2V or OPEN:t_{RC}=125µs, t_{RAS}=t_{RES} MIN. ~1µs)		-	300	µA	3,6
I_{CCS}	SELF REFRESH CURRENT Average Power Supply Current, Self Refresh Mode ($\overline{RAS}$=$\overline{CAS}$=V_{IL}, $\overline{WRITE}$=V_{CC}-0.2V or 0.2V, $\overline{OE}$=V_{CC}-0.2V or 0.2V A0~A9=V_{CC}-0.2V or 0.2V, I/O1~9=V_{CC}-0.2V, 0.2V or OPEN		-	200	µA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	µA	
V_{OH}	OUTPUT CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT CURRENT Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 7,8,9)

SYMBOL	PARAMETER	TC514400AAJLL				UNIT	NOTE
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	10,15, 16
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	10,15
t_{AA}	Access Time from Column Address	-	35	-	40	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Presharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	0	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	ns	
t_{AR}	Column Address Hold Time referenced $\overline{RAS}$	55	-	60		ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	35	-	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	12
t_{WCH}	Write Command Hold Time	15	-	15	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514400AAJLL				UNIT	NOTE
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	13
t_{DH}	Data Hold Time	15	-	15	-	ns	13
t_{REF}	Refresh Period	-	128	-	128	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	20	-	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	70	-	80	-	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	-	40	-	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	40	-	45	-	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	40	-	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	20	ns	10
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	11
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	
t_{RASS}	$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	100	-	100	-	μs	
t_{RPS}	$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before Self Refresh)	130	-	150	-	ns	
t_{CHS}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh)	-50	-	-60	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A8,A9R)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input Capacitance (I/O1~I/O9)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. t_{RAS} (max.)=1μs is only applied to refresh of battery-back up. t_{RAS} (max.) = 10μs is applied to functional operating.

7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

8. AC measurements assume t_T=5ns.

9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

10. Measured with a load equivalent to 2 TTL loads and 100pF.

11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

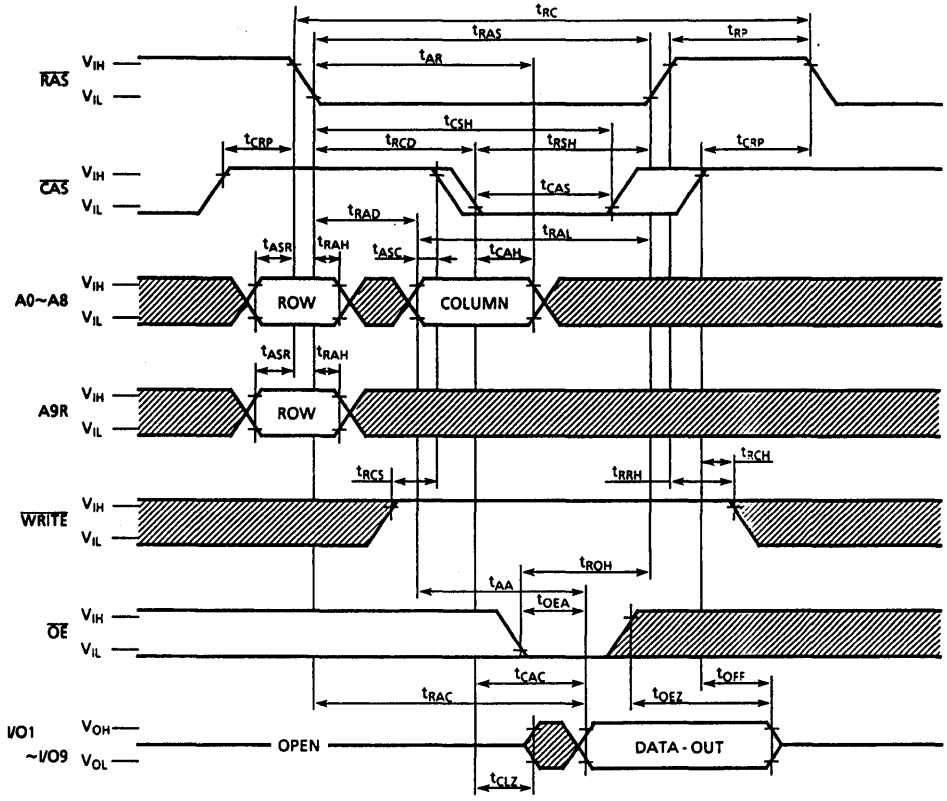
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the date sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWP} > t_{CPWDD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

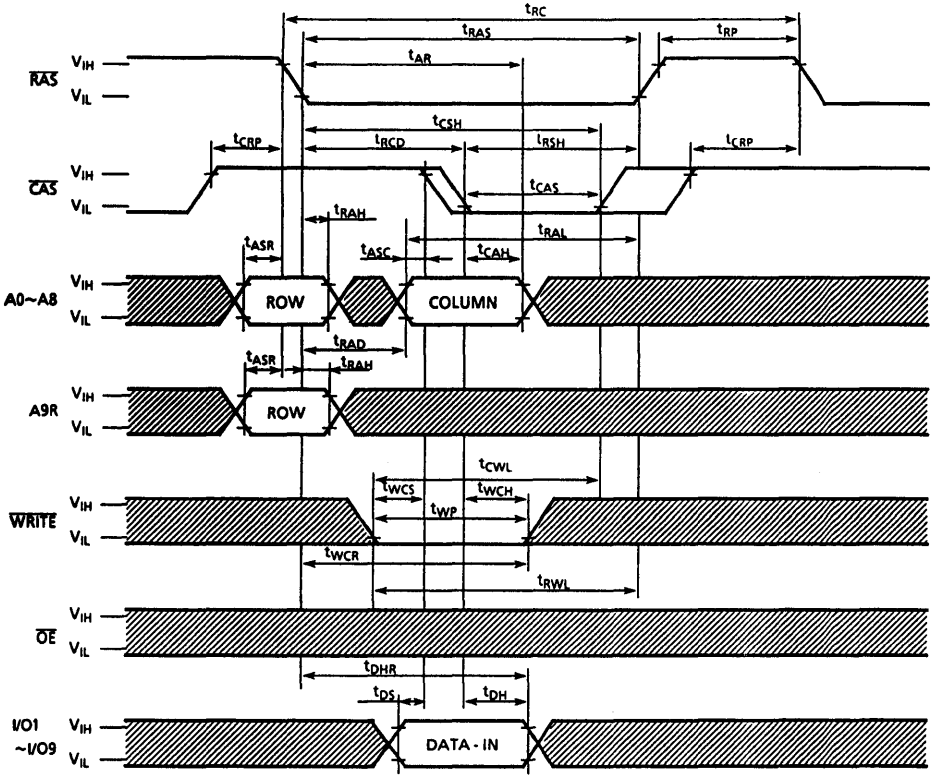
READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

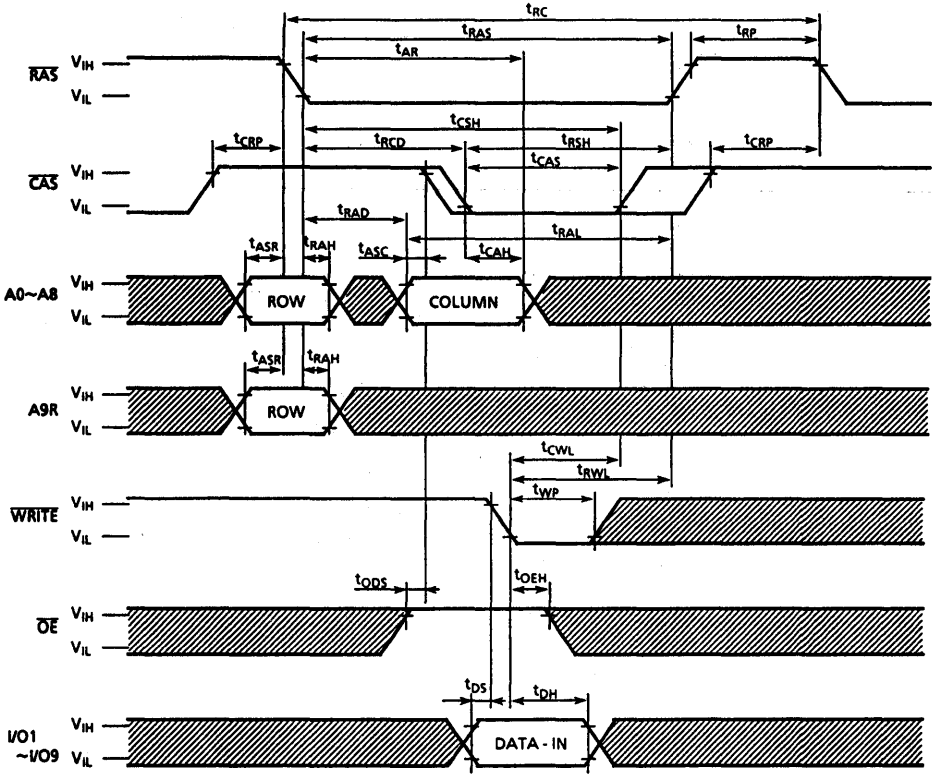
WRITE CYCLE (EARLY WRITE)



Note : D_{OUT} = OPEN

▨ : "H" or "L"

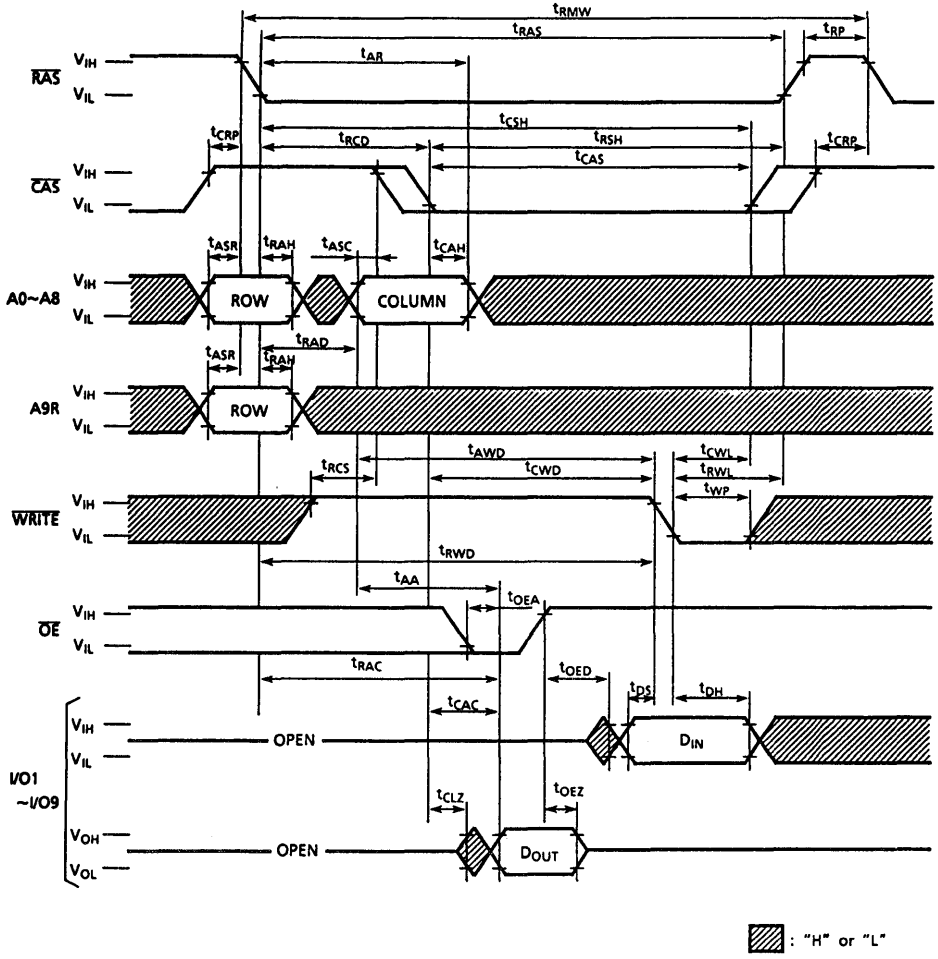
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



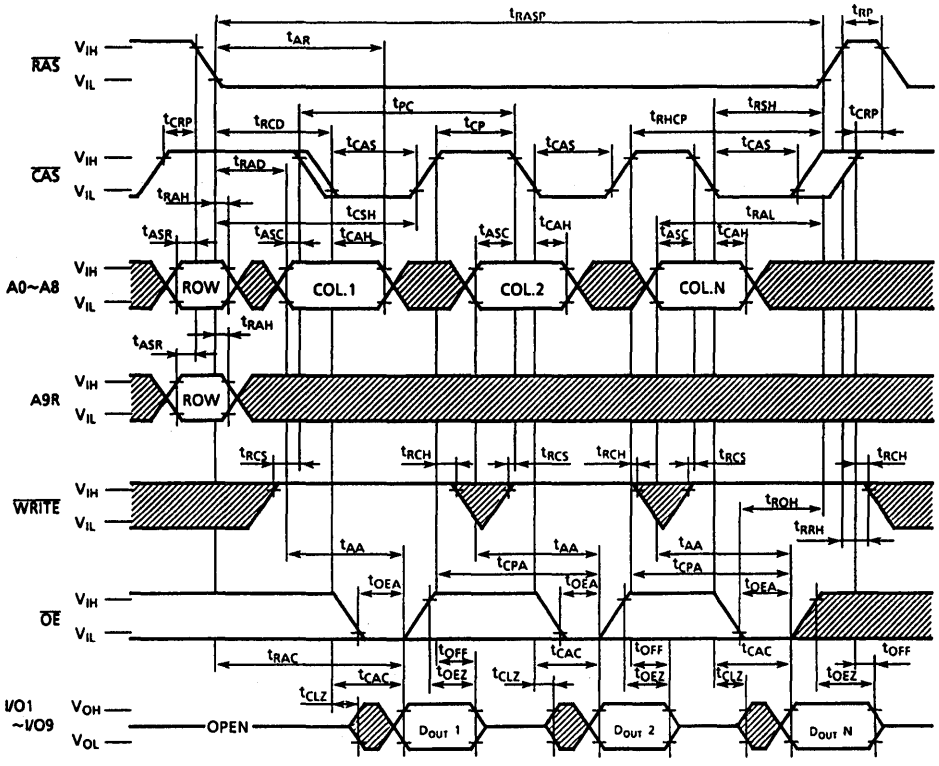
Note : D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



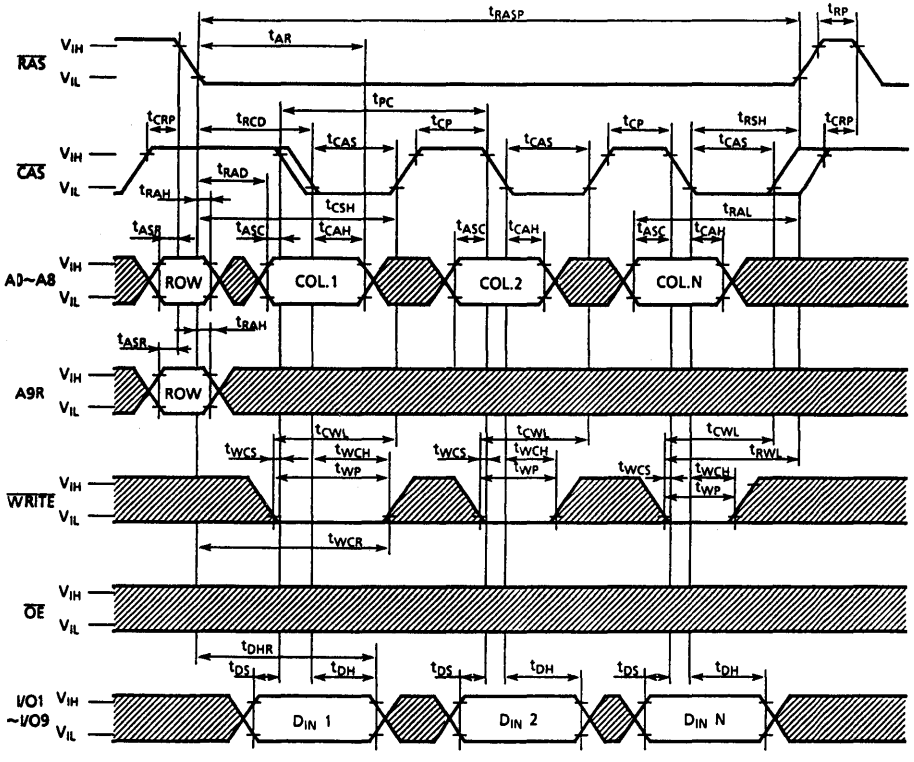
FAST PAGE MODE READ CYCLE



Note : D_{IN} = OPEN

▨ : "H" or "L"

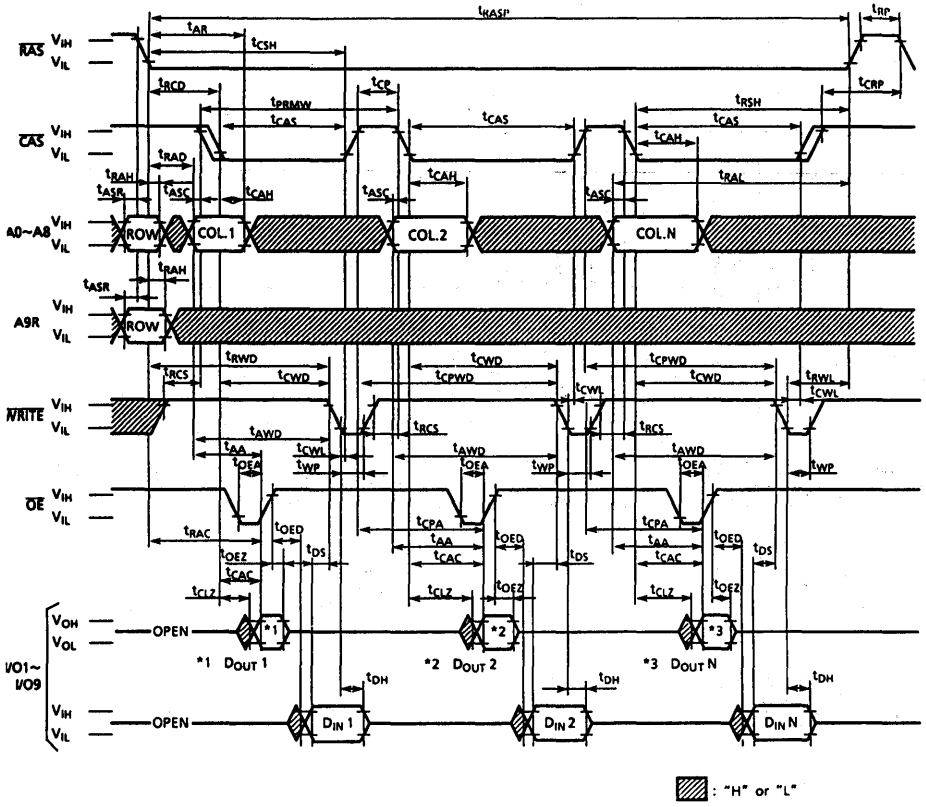
FAST PAGE MODE WRITE CYCLE



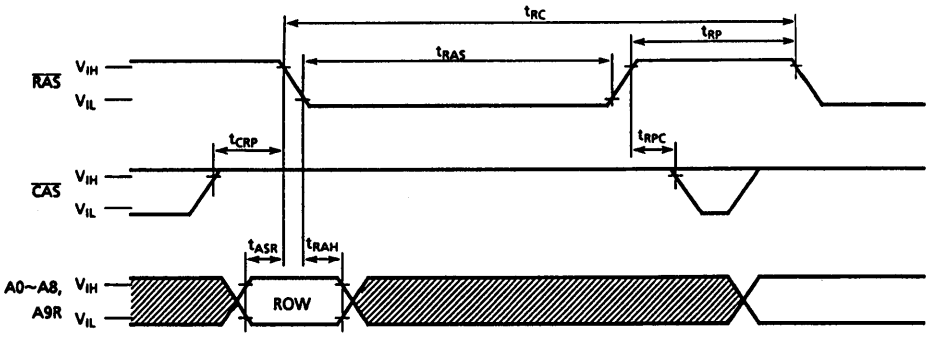
Note : D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



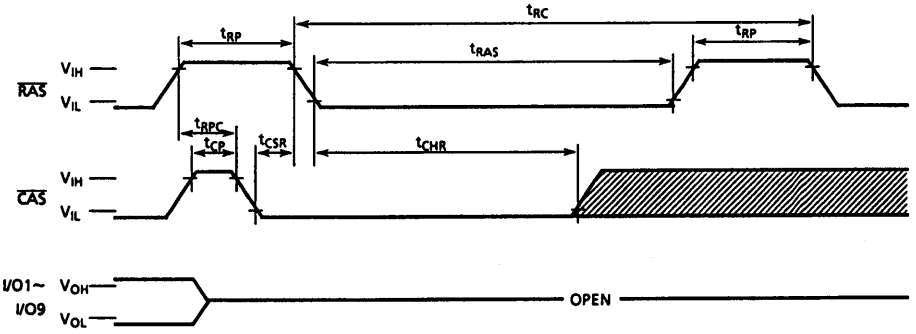
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$, D_{IN} = "H" or "L"
D_{OUT} = OPEN

▨ : "H" or "L"

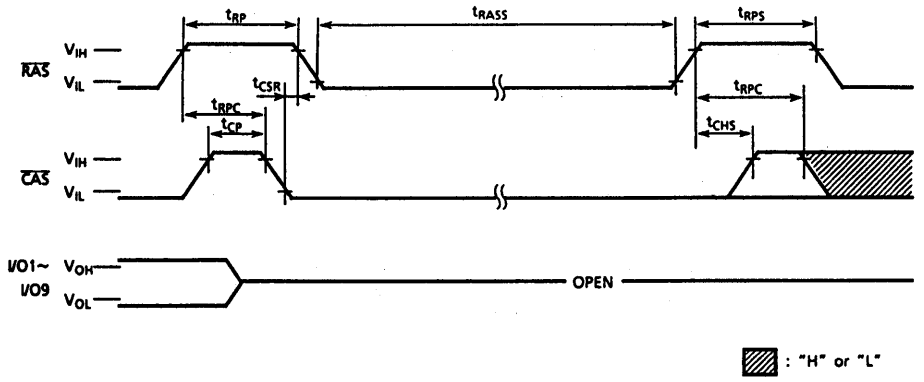
$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$, A0~A8, A9R = "H" or "L"

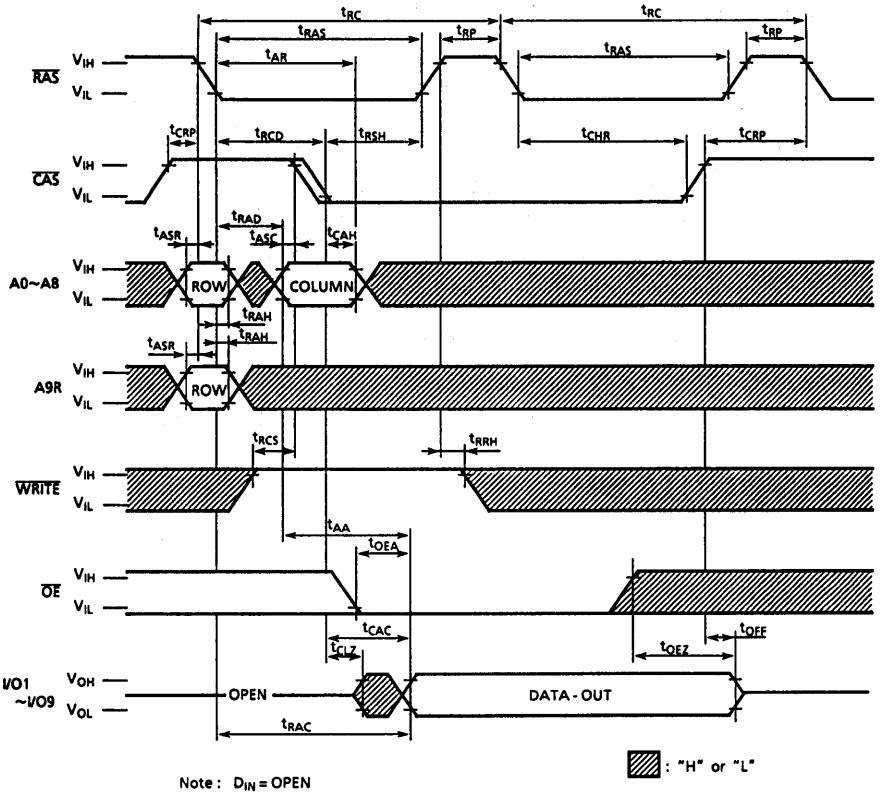
▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ SELF REFRESH CYCLE



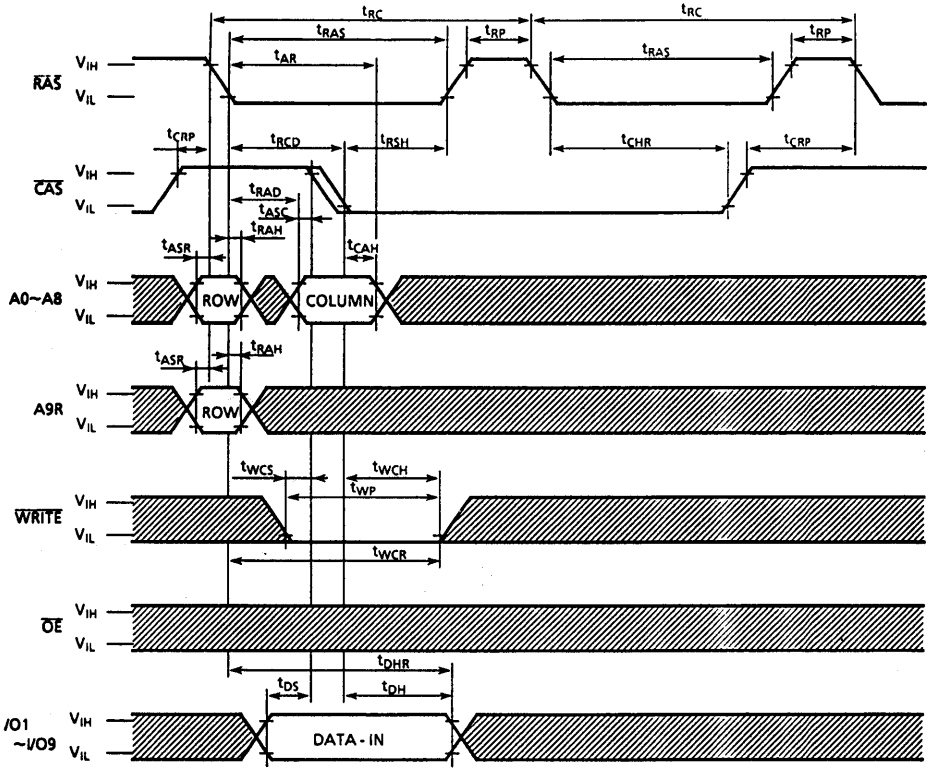
Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$, A0~A8, A9R = "H" or "L"

HIDDEN REFRESH CYCLE (READ)



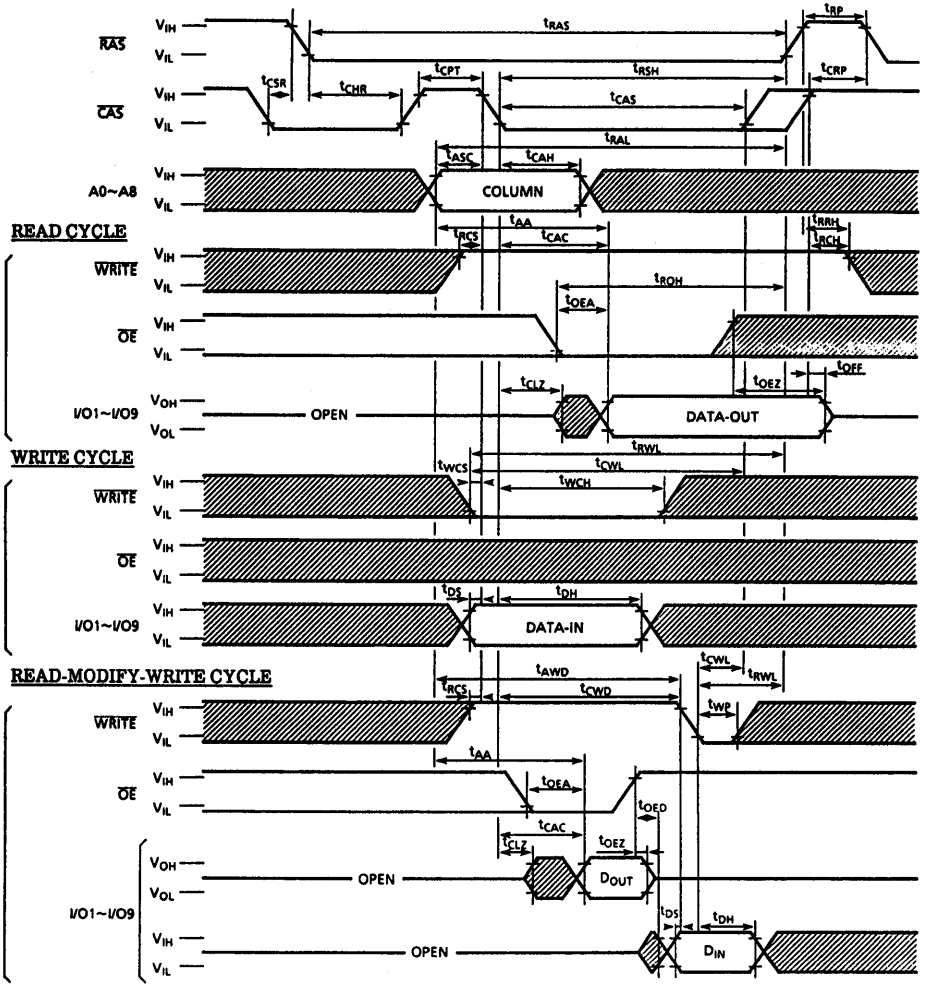
Note: D_{IN} = OPEN

HIDDEN REFRESH CYCLE (WRITE)



Note : D_{OUT} = OPEN

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



Note : A9R = "H" or "L"

262,144 WORD X 16 BIT DYNAMIC RAM

DESCRIPTION

The TC514260BJ/BFT is the new generation dynamic RAM organized 262,144 word by 16 bit. The TC514260BJ/BFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514273BJ to be packaged in a standard 40 pin plastic SOJ, and 44/40 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 262,144 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  550mW MAX .Operating
  (TC514273BJ-70)
  468mW MAX. Operating
  (TC514273BJ-80)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 512refresh cycles/8ms
- Package TC514260BJ : SOJ40-P-400
  TC514260BFT : TSOP44-P-400B

KEY PARAMETERS

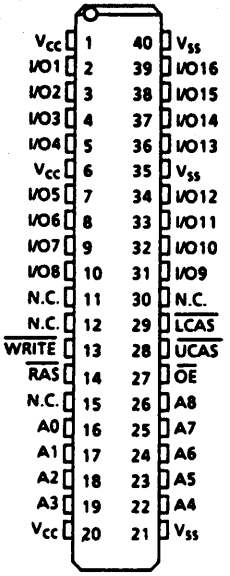
ITEM		TC514260BJ	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

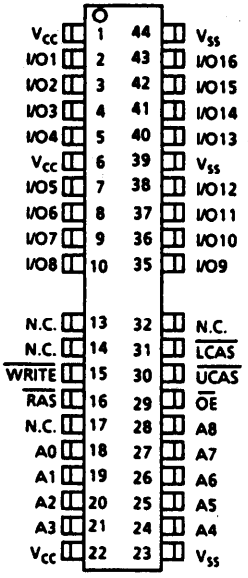
A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O16	Write Section/ Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

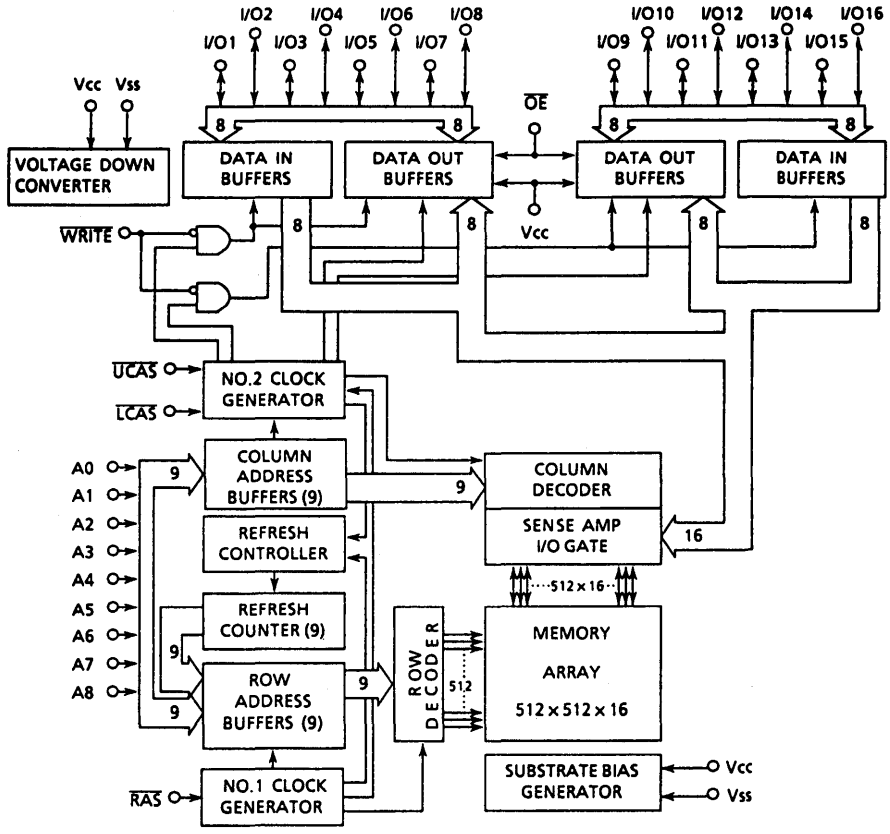
Plastic SOJ



Plastic TSOP
(Normal Bend Type)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITION (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	V_{CC}+0.5	V	2
V_{IL}	Input Low Voltage	-0.5	-	0.8	V	2

*-2.0V at pulse width ≤ 20ns

D.C. OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514260BJ/BFT-70 TC514260BJ/BFT-80	- -	100 85	mA	3,4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode($\overline{RAS}$ Cycling, $\overline{UCAS}$=$\overline{LCAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514260BJ/BFT-70 TC514260BJ/BFT-80	- -	100 85	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode($\overline{RAS}$ =V_{IL},$\overline{UCAS}$,$\overline{LCAS}$,Address Cycling:t_{PC}=t_{PC}MIN.)	TC514260BJ/BFT-70 TC514260BJ/BFT-80	- -	70 60	mA	3,4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ Cycling: t_{RC}=t_{PC} MIN.)	TC514260BJ/BFT-70 TC514260BJ/BFT-80	- - -	100 85	mA	3, 5
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	μA	
V_{OH}	OUTPUT CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT CURRENT Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC514260BJ/BFT				UNIT	NOTES
		-70		-80			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ Presharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514260BJ/BFT				UNIT	NOTES
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	8	-	8	ns	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	-	110	-	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	-	70	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	75	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	30	-	30	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to OE	10	-	10		ns	
t_{OEA}	$\overline{OE}$ Access TIme	-	20	0	20	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{OE}$))	-	7	pF
C_O	Input Capacitance(I/O1~I/O16)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

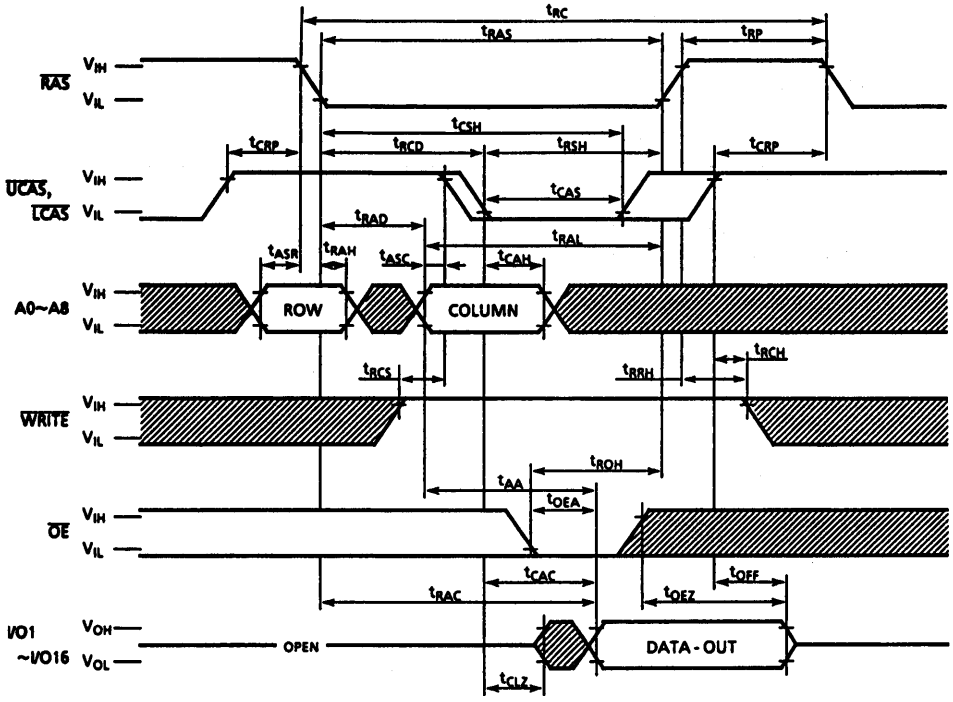
12. These parameters are referenced to $\overline{UCAS}$, $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WRITE}$, leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

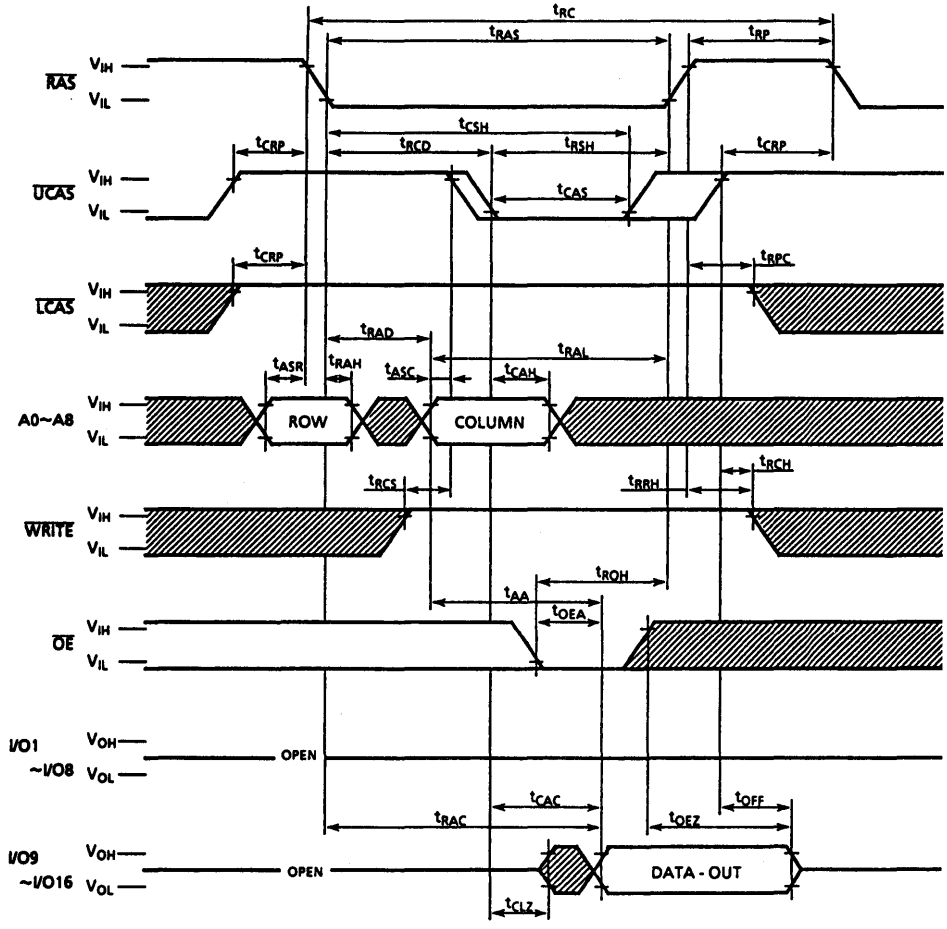
READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

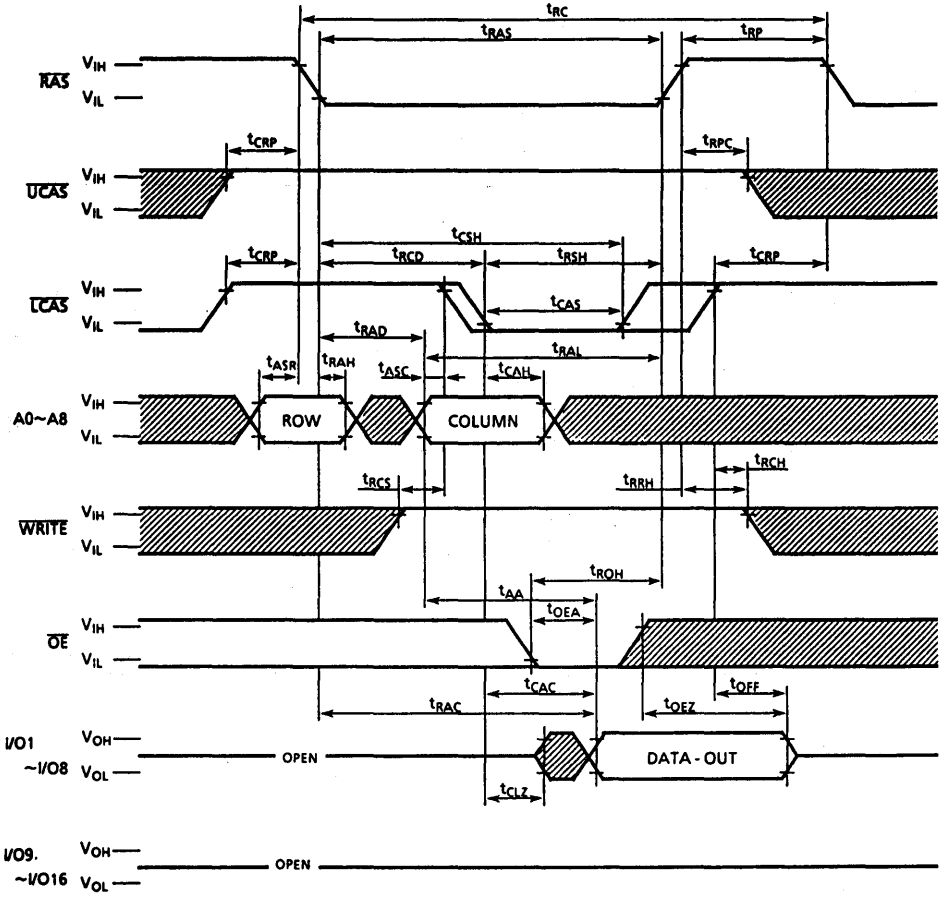
UPPER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{IN} (I/O9~I/O16) = OPEN

▨ : "H" or "L"

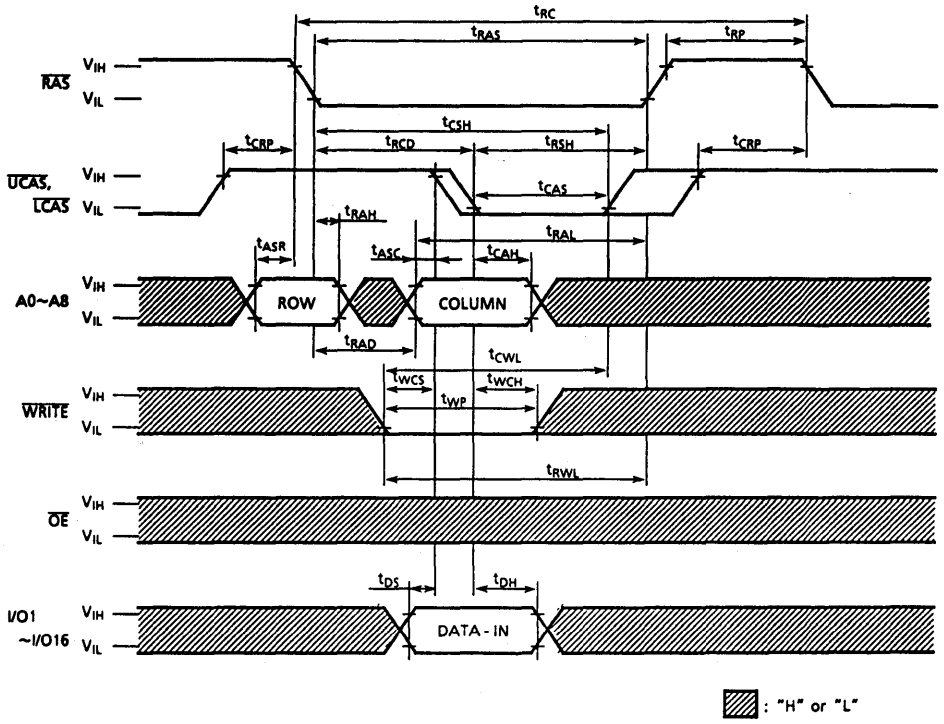
LOWER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O8) = OPEN
D_{IN} (I/O9~I/O16) = Don't Care

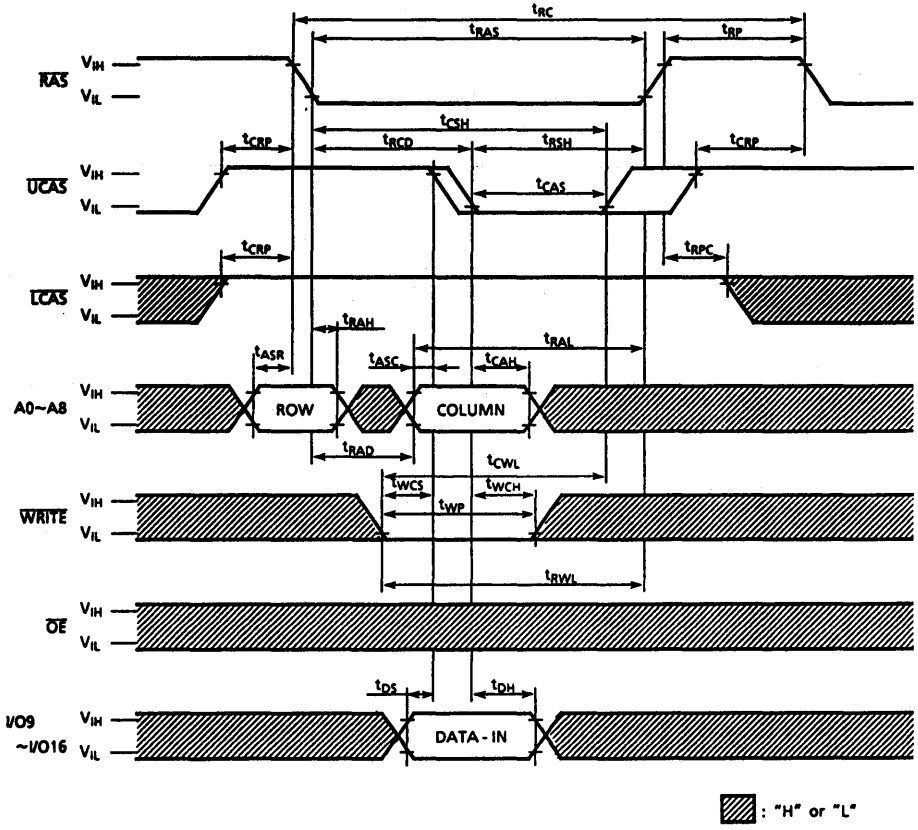
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE)



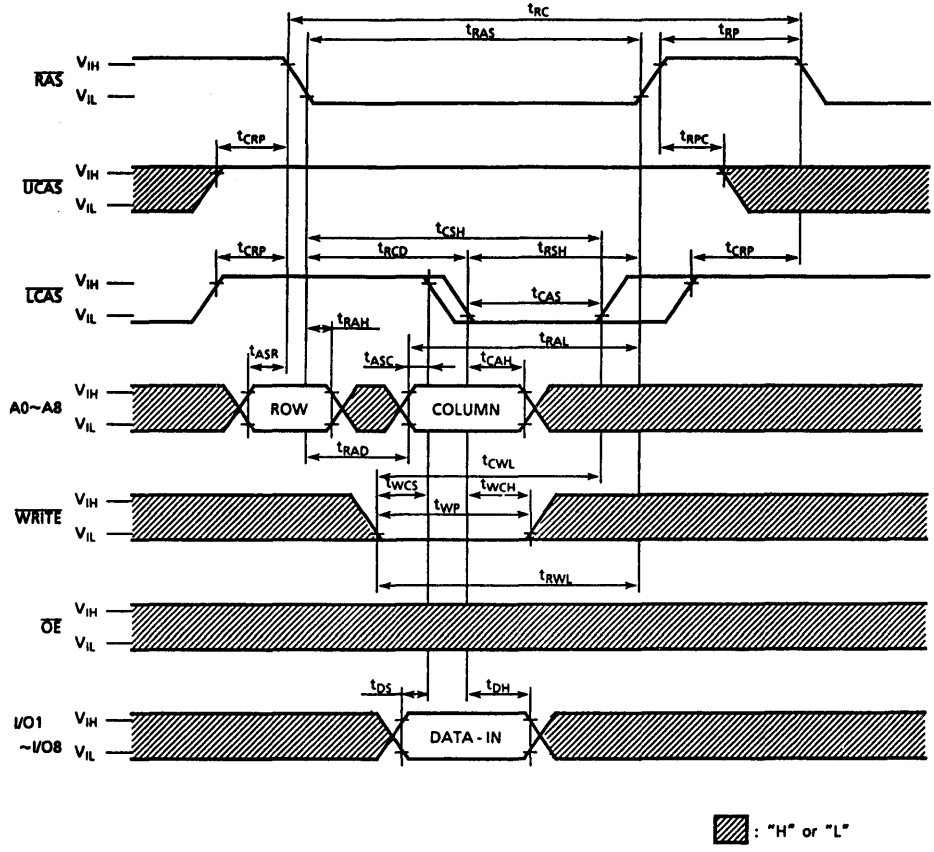
Note: D_{OUT} = OPEN

UPPER BYTE WRITE CYCLE (EARLY WRITE)



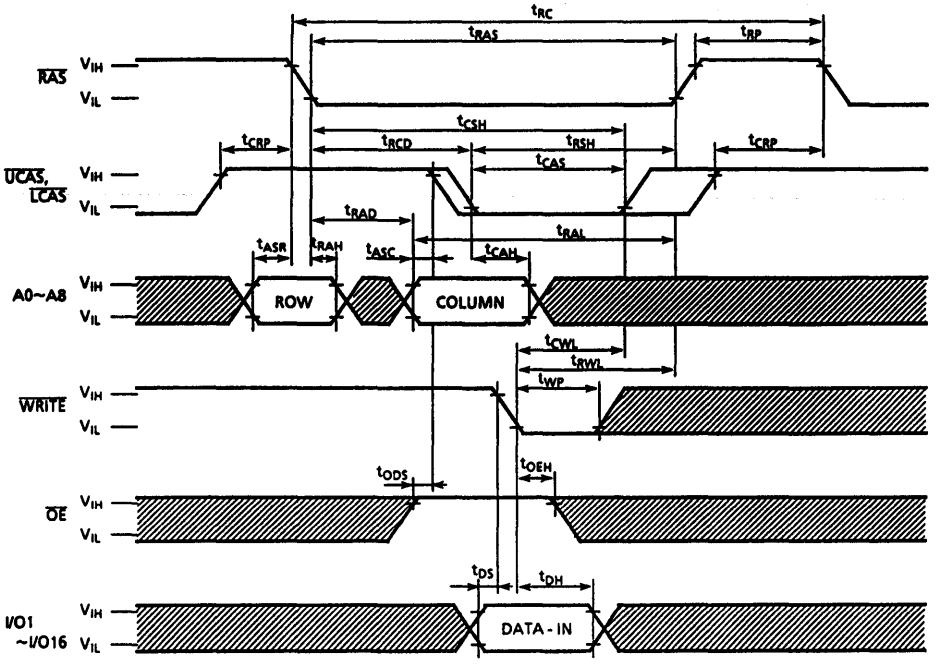
Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} = OPEN

LOWER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} = OPEN

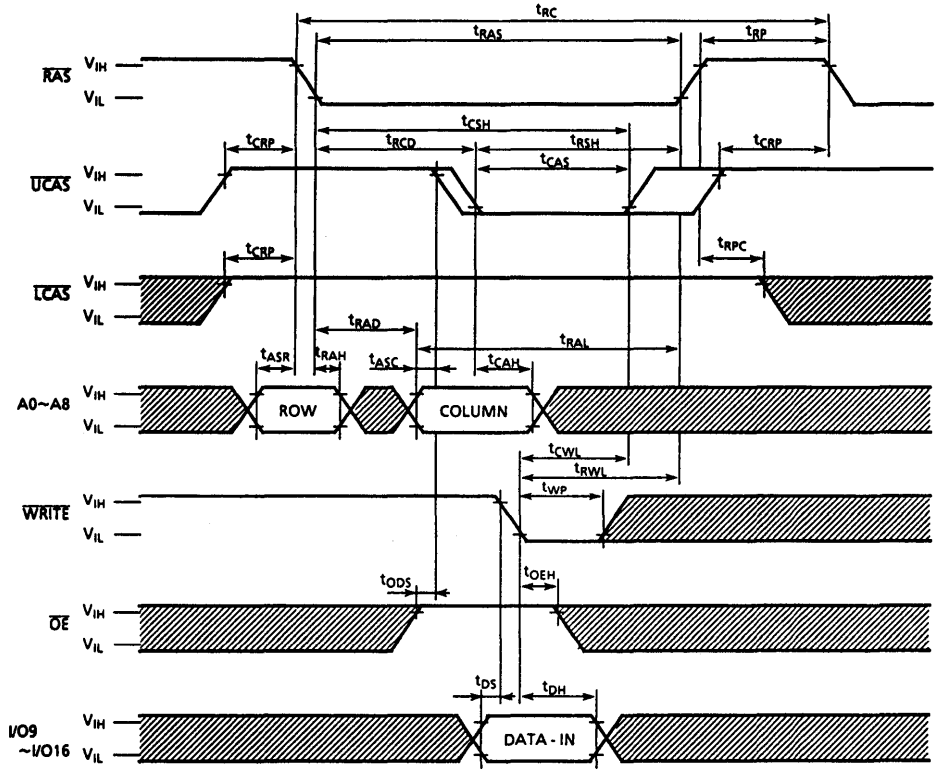
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

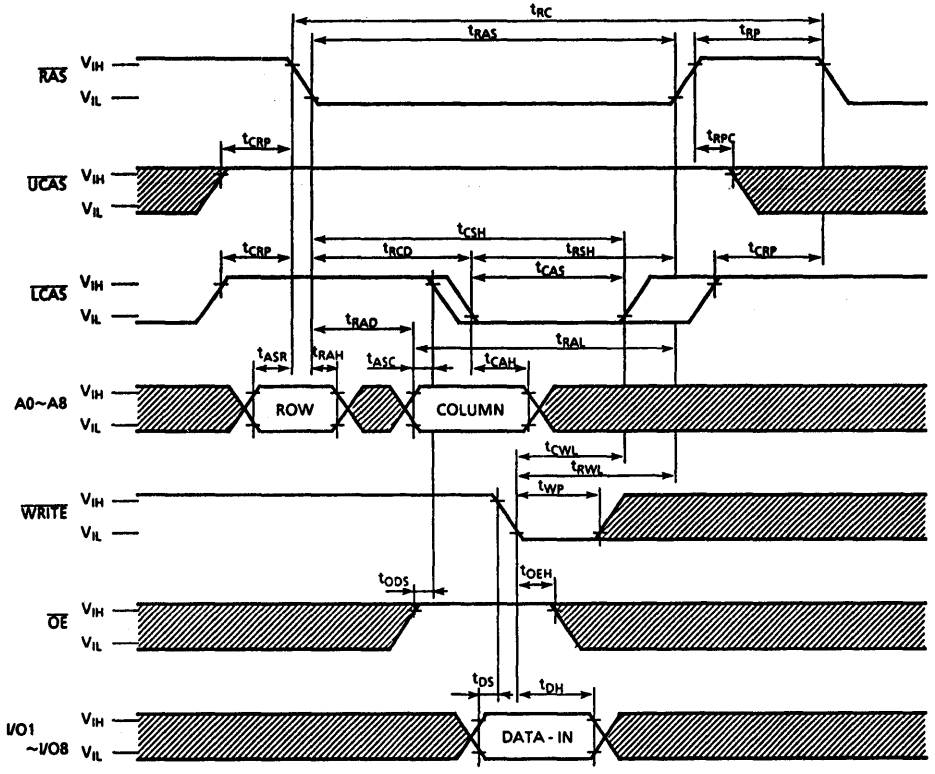
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

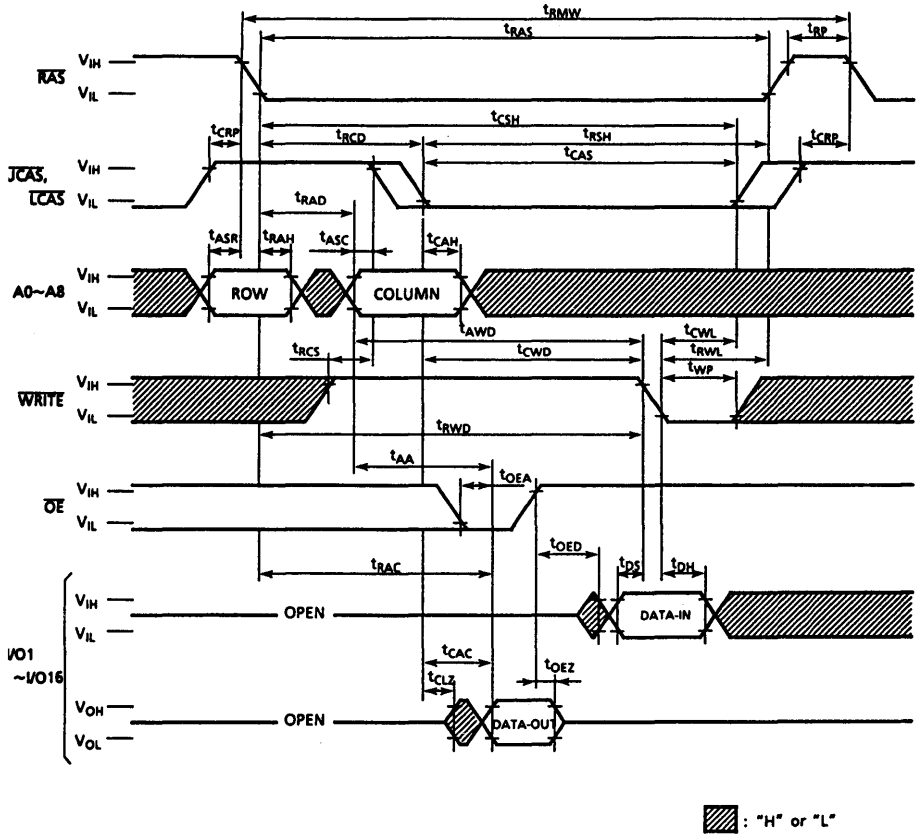
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



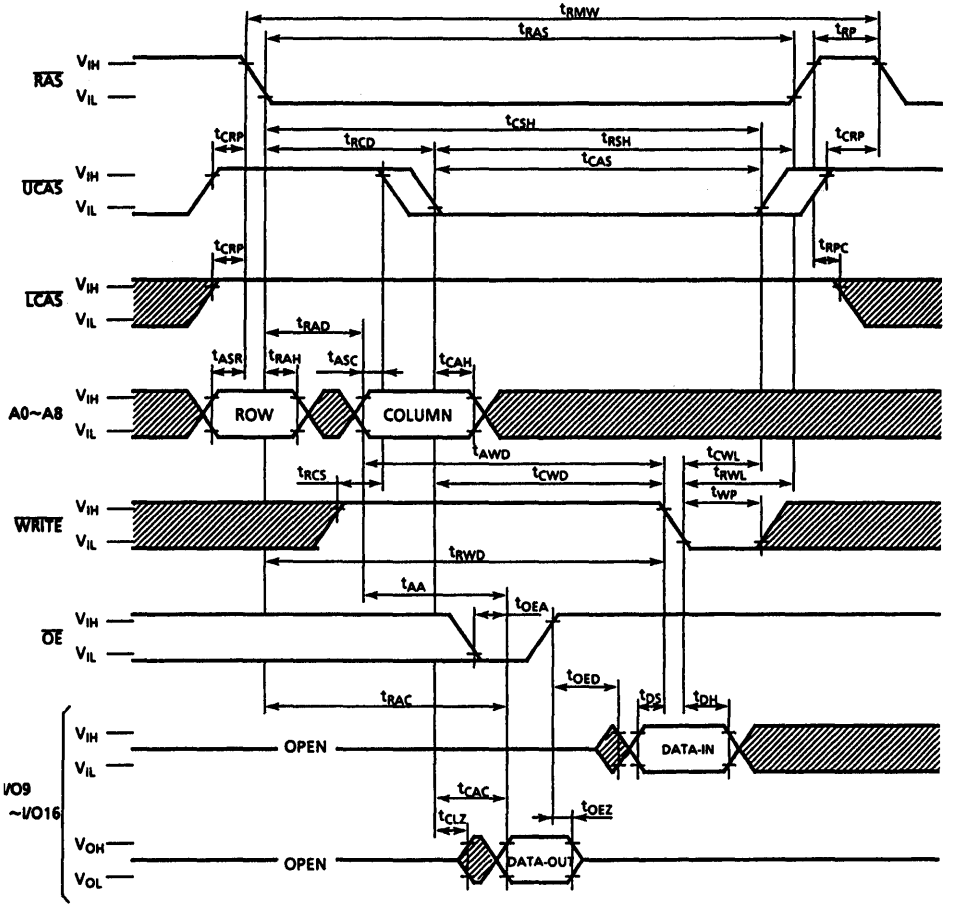
Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE

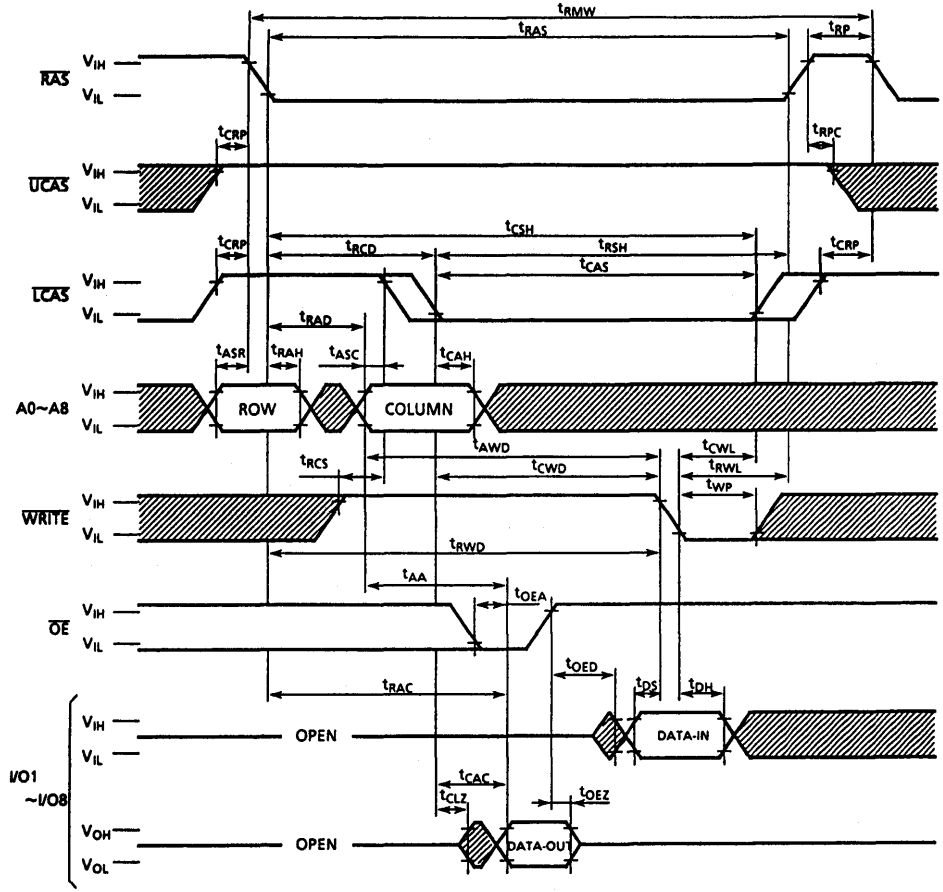


UPPER BYTE READ-MODIFY-WRITE CYCLE



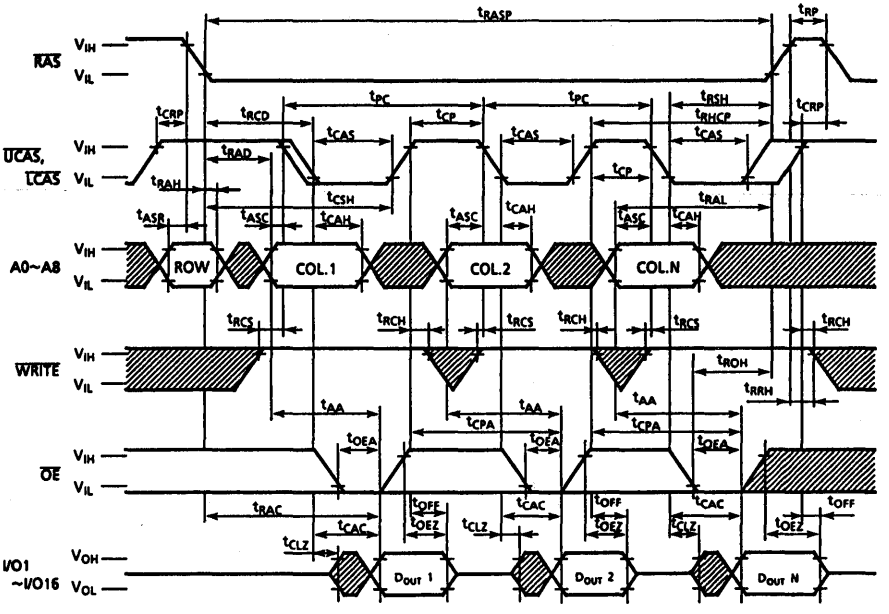
Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} (I/O1~I/O8) = OPEN

LOWER BYTE READ-MODIFY-WRITE CYCLE



Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} (I/O9~I/O16) = OPEN

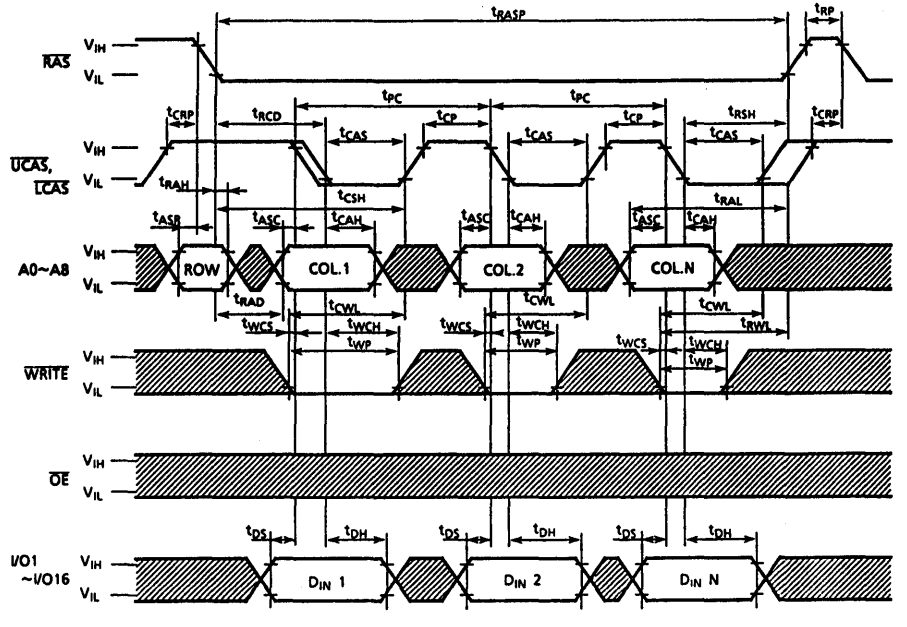
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨: "H" or "L"

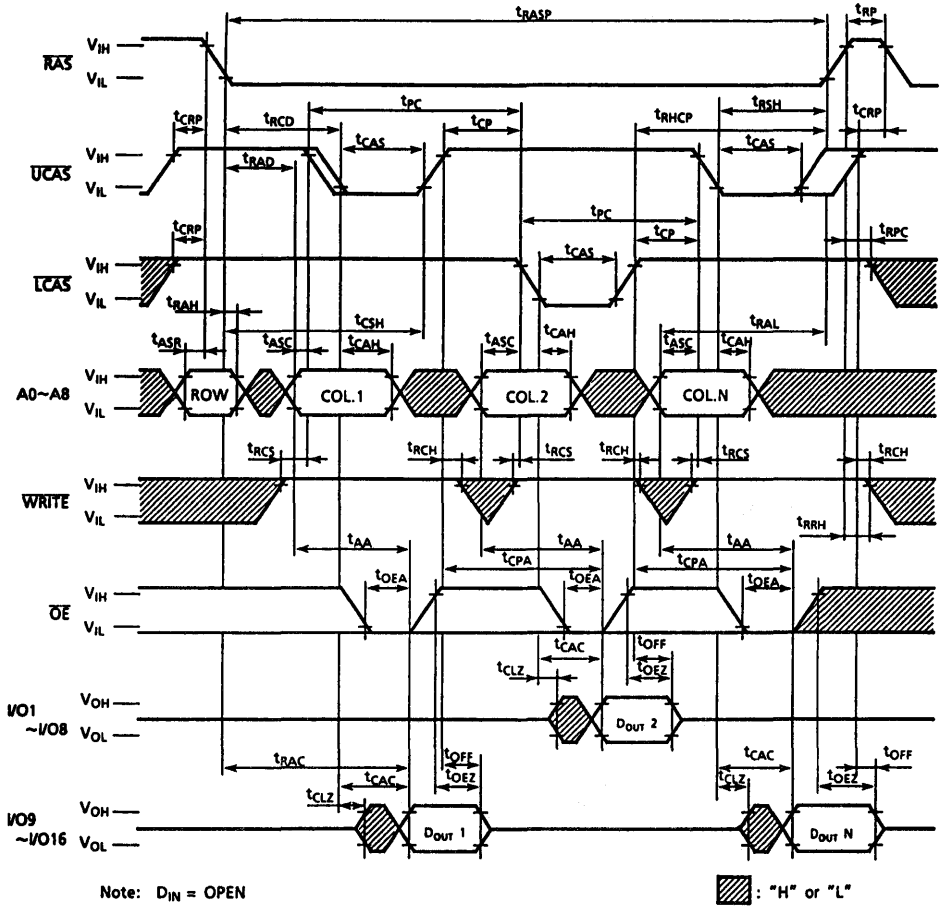
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨: "H" or "L"

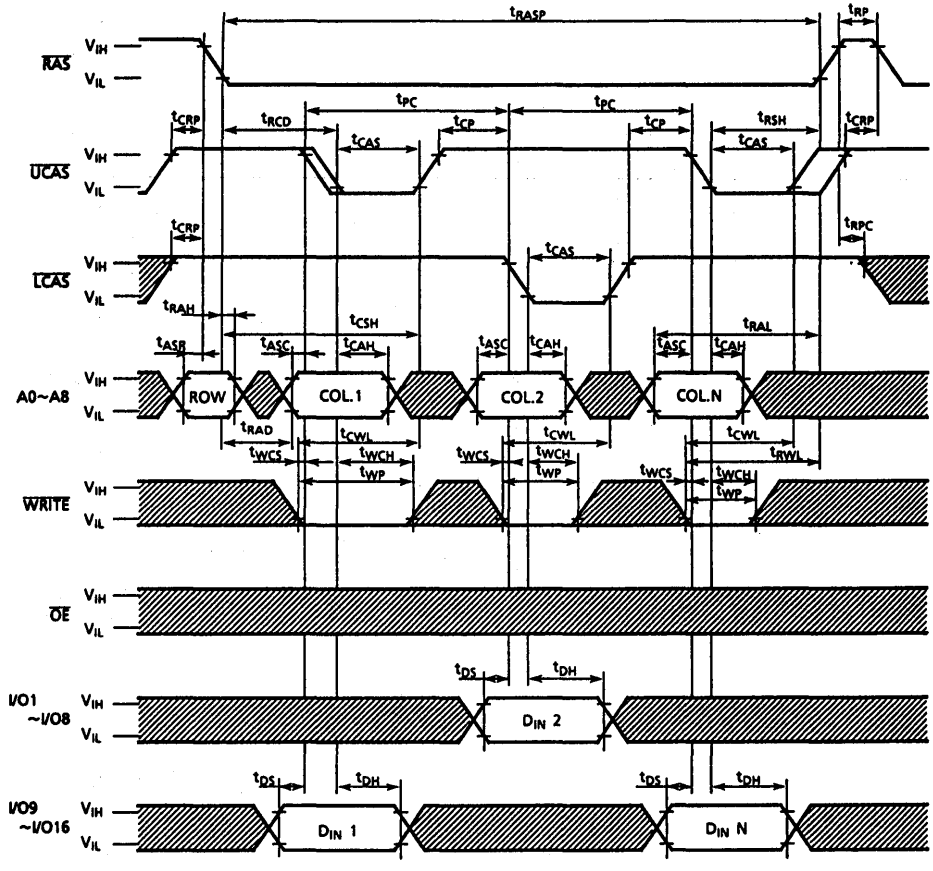
FAST PAGE MODE BYTE READ CYCLE



Note: D_{IN} = OPEN

▨: "H" or "L"

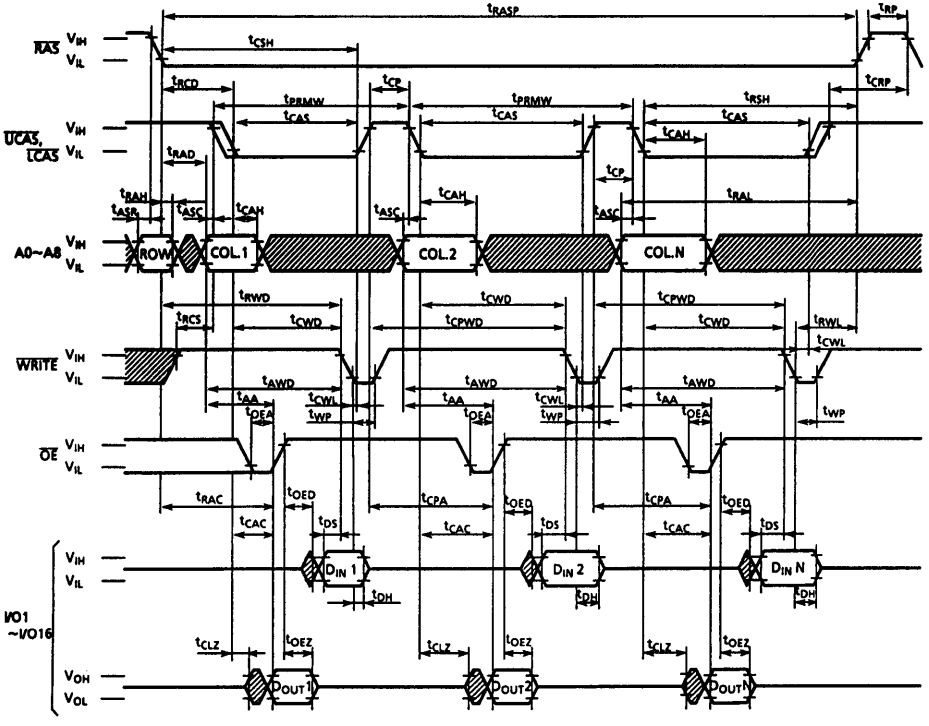
FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



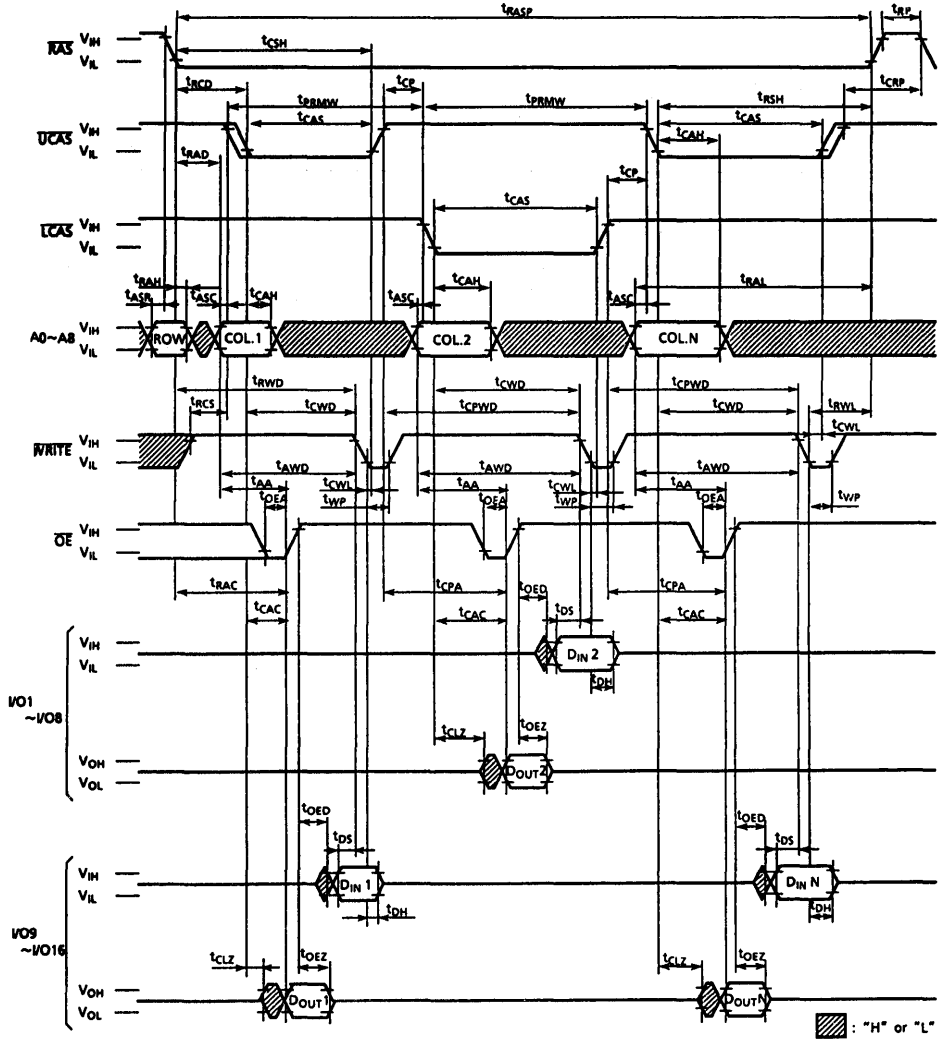
Note: D_{OUT} = OPEN

▨: "H" or "L"

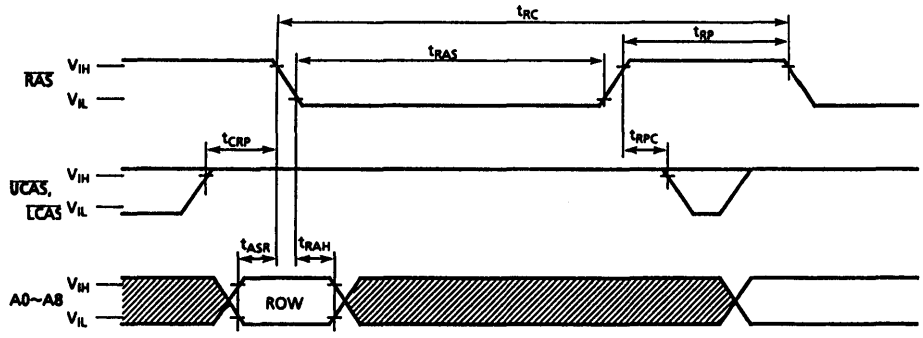
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE



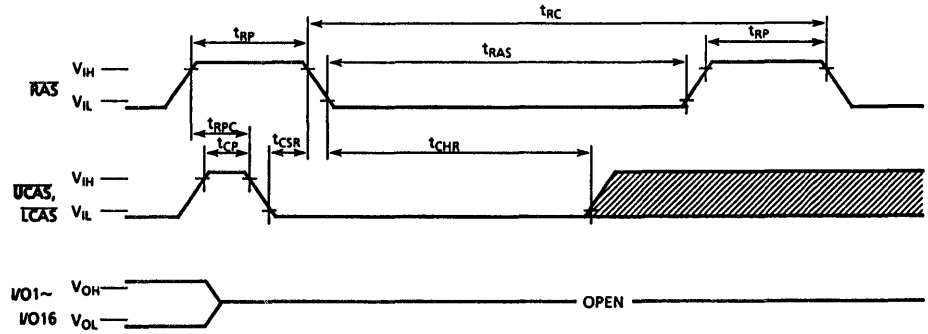
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"
D_{IN} = Don't Care
D_{OUT} = OPEN

▨: "H" or "L"

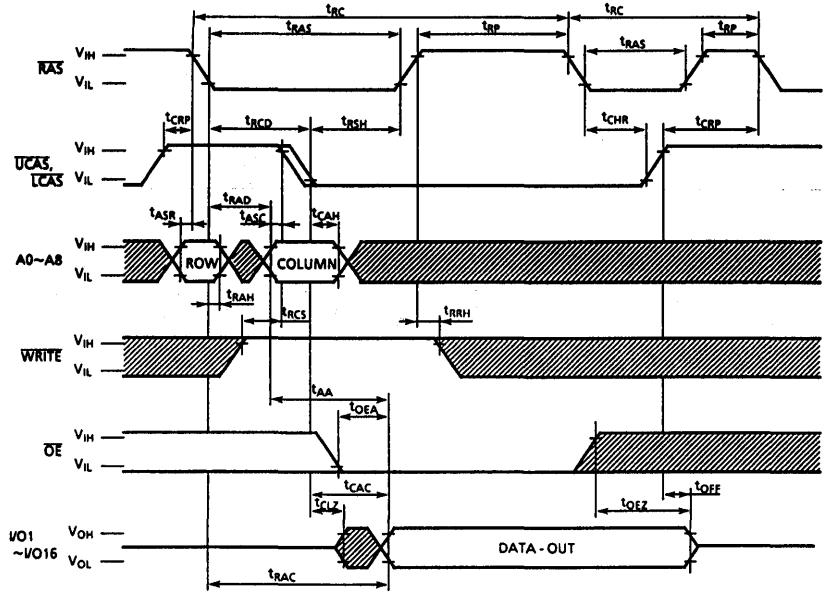
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



▨: "H" or "L"

Note: $\overline{WRITE}$, $\overline{OE}$, A0~A8 = "H" or "L"
D_{IN} = Don't Care
$\overline{CAS}$ before $\overline{RAS}$ refresh is performed when either $\overline{UCAS}$ or $\overline{LCAS}$ meets this timing.

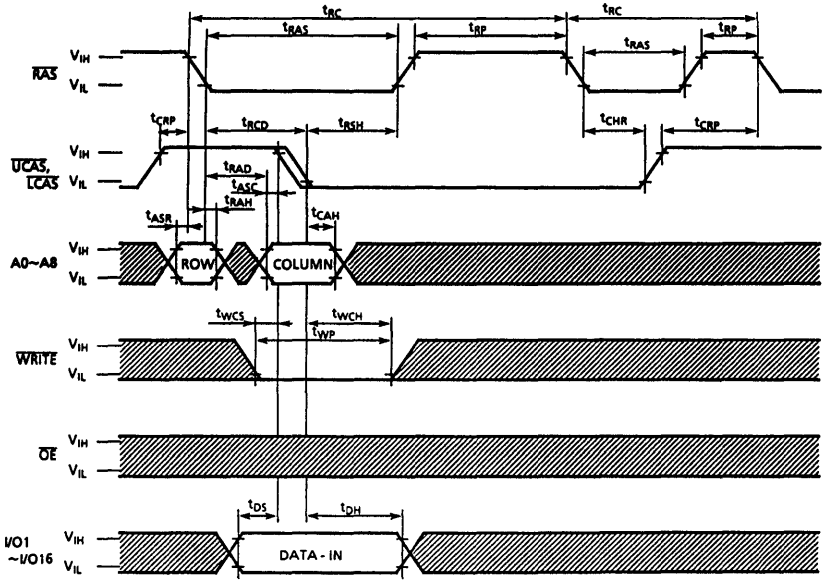
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨: "H" or "L"

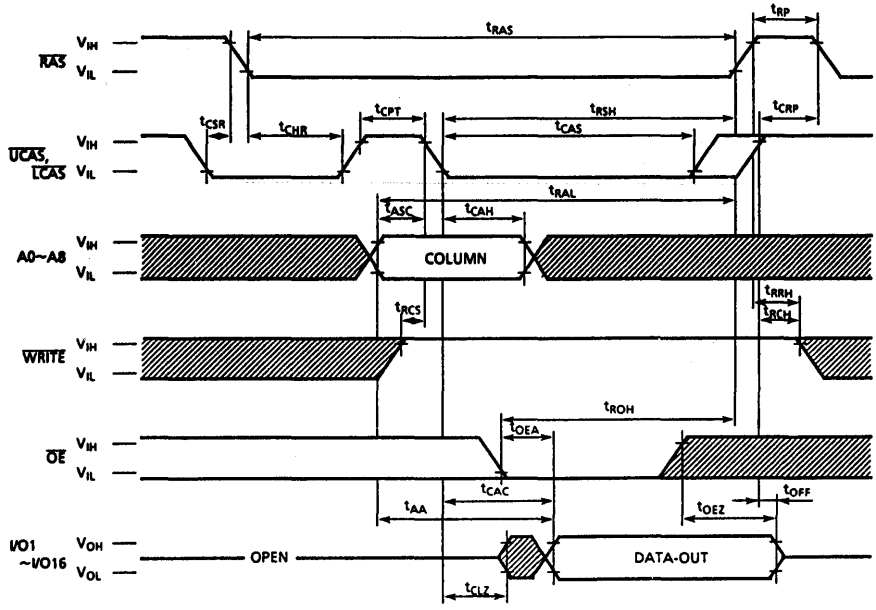
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

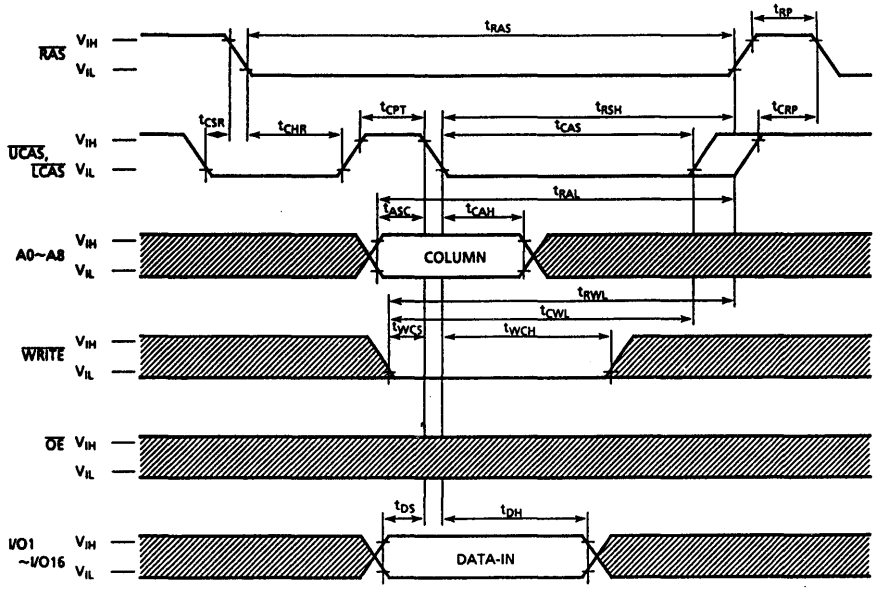
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



Note: D_{IN} = OPEN

▨: "H" or "L"

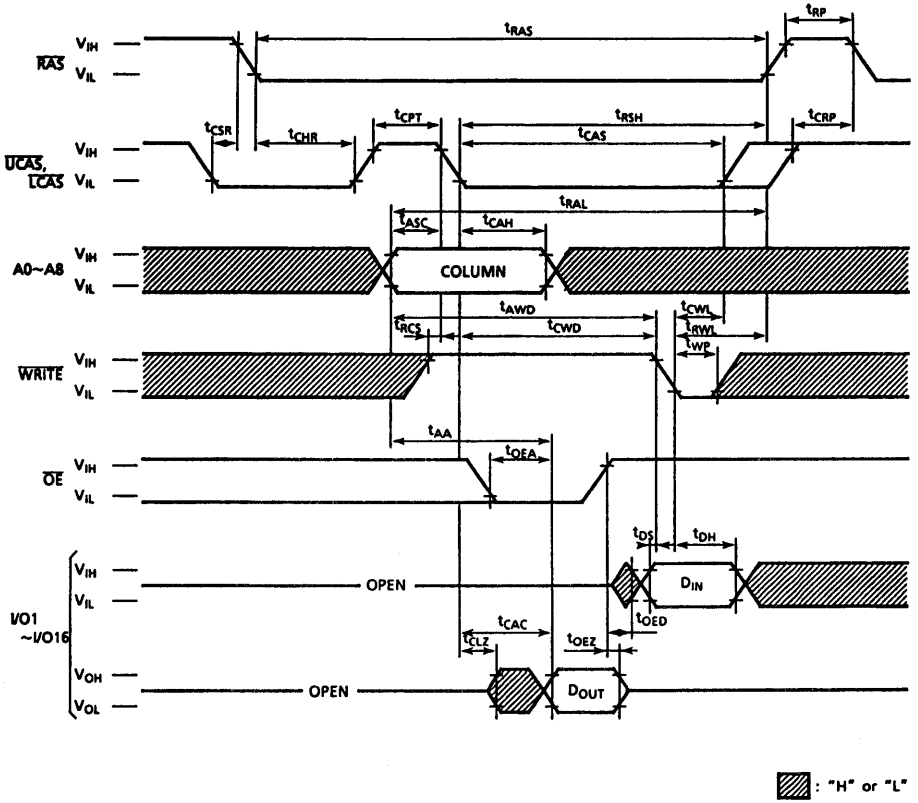
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



Note: D_{OUT} = OPEN

▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



262,144 WORD X 16 BIT DYNAMIC RAM

DESCRIPTION

The TC514170BJ is the new generation dynamic RAM organized 262,144 word by 16 bit. The TC514170BJ utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514170BJ to be packaged in a standard 40 pin plastic SOJ. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL,

FEATURES

- 262,144 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-ion V_{BB} generator
- Low Power
  413mW MAX .Operating
  (TC514170B-70)
  358mW Max. Operating
  TC514170B-80
  5.5mW Max. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, CAS before RAS refresh, RAS-only refresh, Hidden refresh, Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC514170BJ : SOJ40-P-400

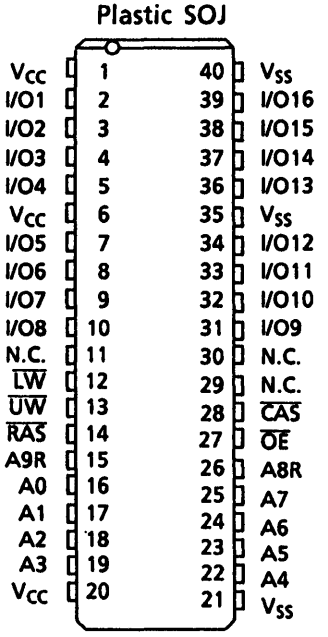
KEY PARAMETERS

ITEM		TC514170BJ	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

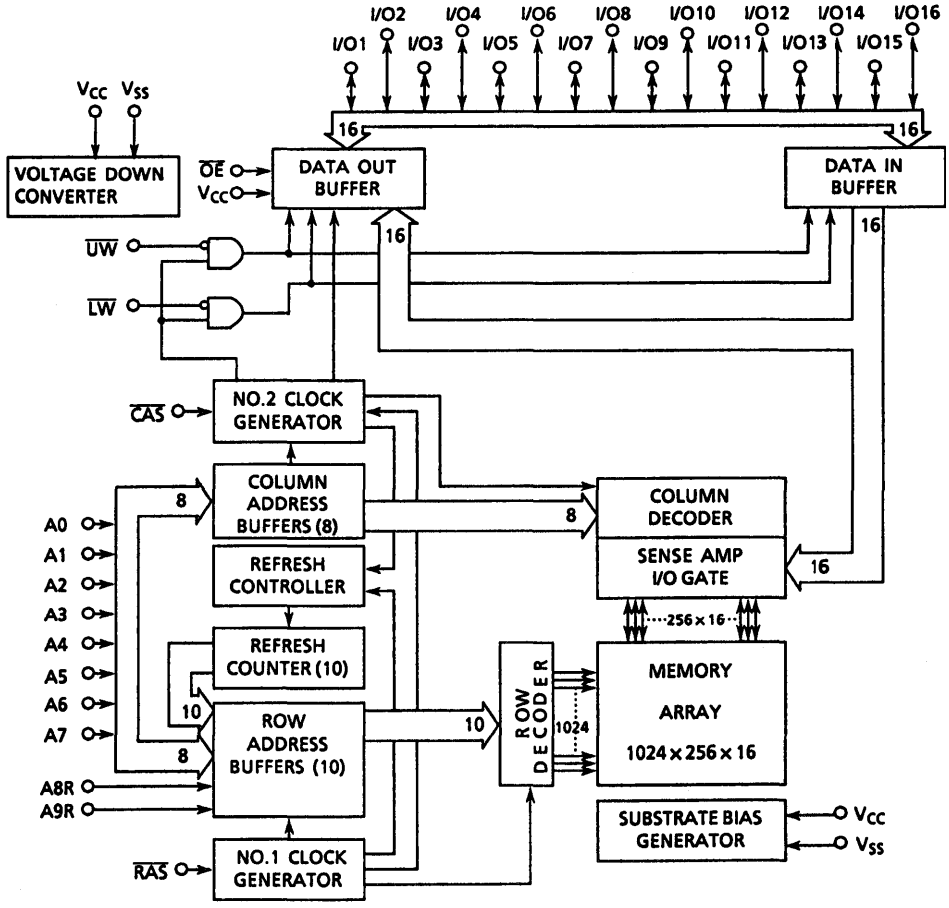
PIN NAME

A0~A7, A8R, A9R	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read/Upper Byte Write Input
$\overline{LW}$	Read/Lower Byte Write Input
$\overline{OE}$	Output Enable
I/01~I/016	Data Input/Outputt
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1~7	V	1
Output Voltage	V_{OUT}	— 1~7	V	1
Power Supply Voltage	V_{CC}	— 1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITION (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	High Level Input Voltage	2.4	-	V_{CC}+0.5	V	2
V_{IL}	Low Level Input Voltage	-0.5*	-	0.8	V	2

* 2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling:t_{RC}=t_{RC} MIN)	TC514170BJ-70	-	75	mA	3,4 5
		TC514170BJ-80	-	65		
I_{CC2}	STANBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$, =V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current ($\overline{RAS}$ Only Mode ($\overline{RAS}$, Cycling, $\overline{CAS}$,= V_{IH}: t_{RC}=t_{RC} MIN)	TC514170BJ-70	-	75	mA	3, 5
		TC514170BJ-80	-	65		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$,Adress Cycling: t_{PC}=t_{PC} MIN)	TC514170BJ-70	-	70	mA	3, 4, 5
		TC514170BJ-80	-	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current, ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$,Adress Cycling: t_{PC}=t_{PC}	TC514170BJ-70	-	75	mA	3, 5
		TC514170BJ-80	-	65		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≤ V_{IN}≤ V_{CC}, All Other Pins Not Under Test=OV		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, ≤ OV≤ V_{OUT} ≤ V_{CC}		-10	10	μA	
V_{OH}	OUTPUT LEVEL (Output "H" Level Voltage (I_{OUT} = 5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL (Output "H" Level Voltage (I_{OUT} = 4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC514170BJ				UNIT	NOTES
		-70		-80			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z Data Hold Time	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ Presharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514170BJ				UNIT	NOTE
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	16	-	16	ns	
t_{WCS}	Write Command Set-up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	-	110	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	-	70	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	75	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	30	-	30	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10		ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	0	20	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-up Time	0	-	0	-	ns	
t_{MCS}	Masked Write Set-Up Time	0	-	10	-	ns	
t_{MRH}	Masked Write Hold Time referenced to $\overline{RAS}$	0	-	10	-	ns	
t_{MCH}	Masked Write Hold Time referenced to $\overline{CAS}$	0	-	10	-	ns	

CAPACITANCE (T_{CC}= 5V± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 ~A7, A8R, A9R)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (I/O1~I/O16)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieveS the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

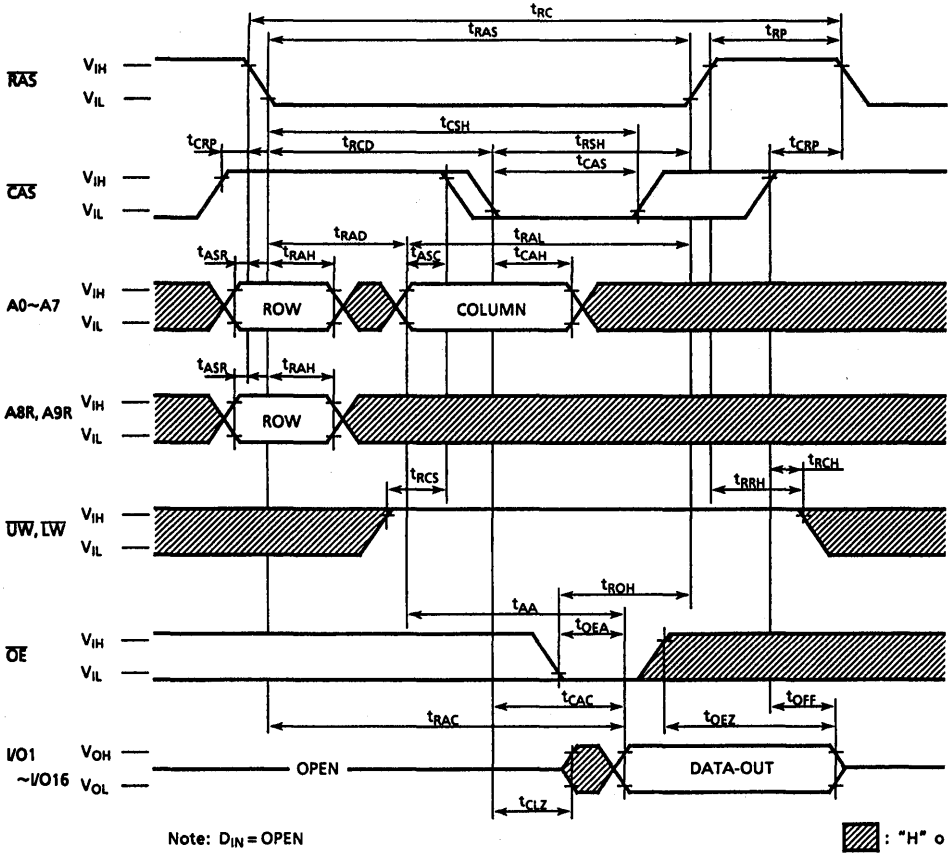
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

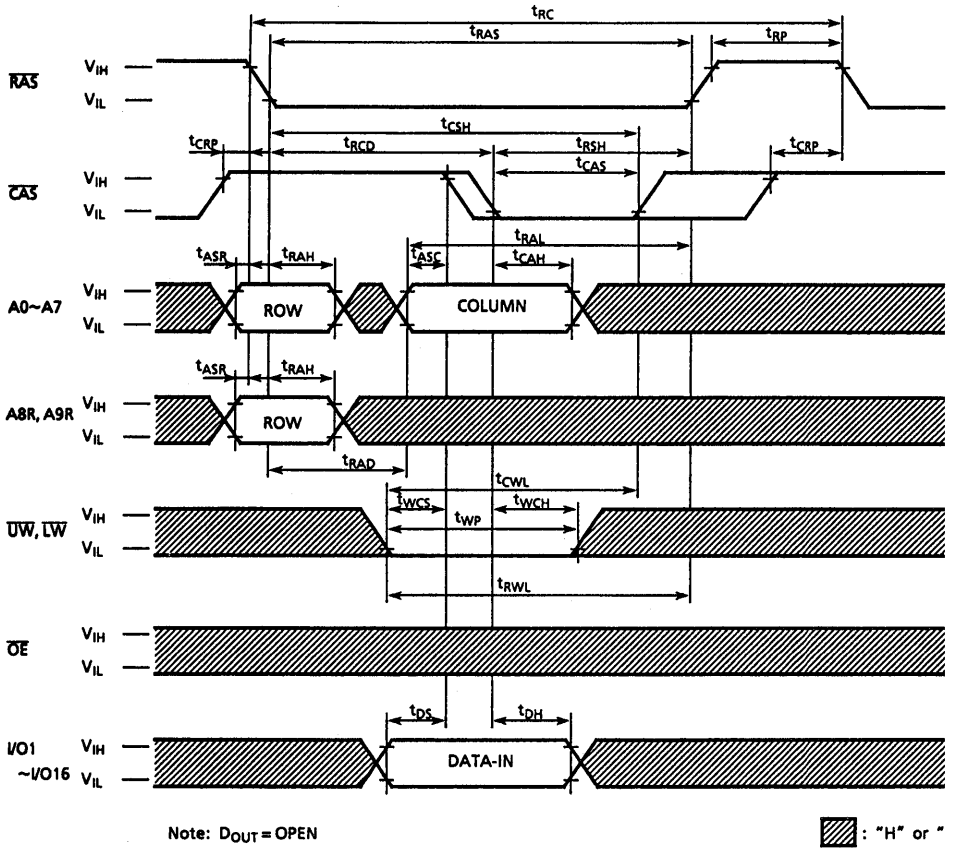
READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" o

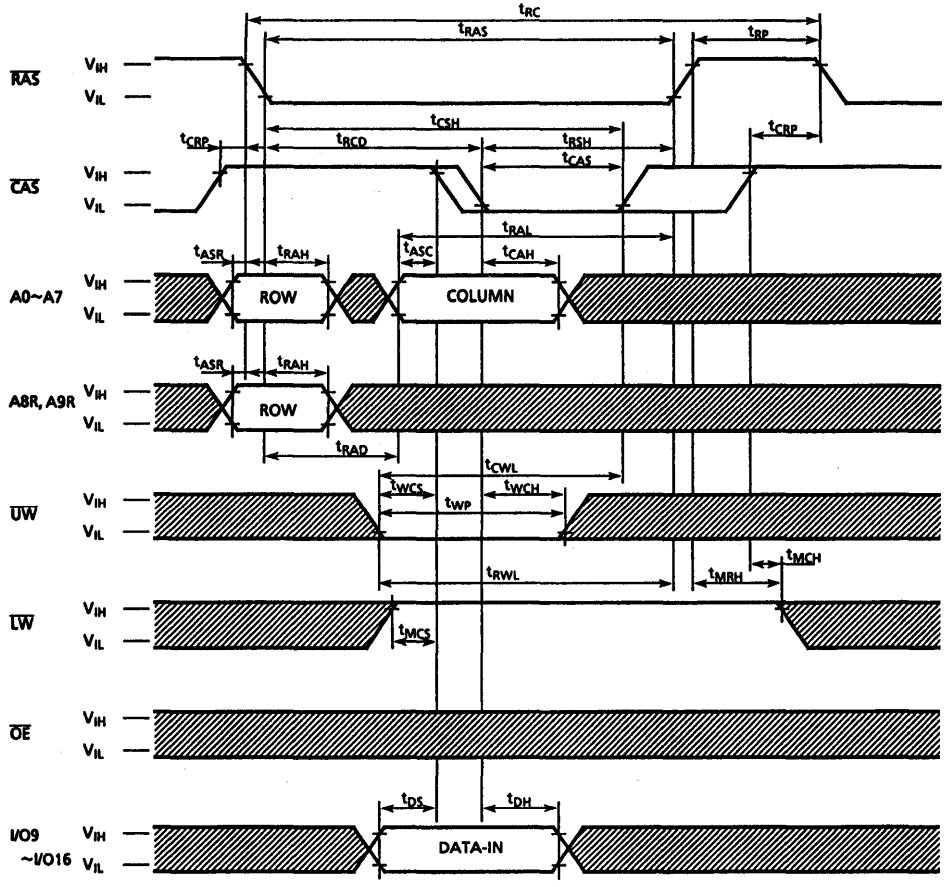
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "

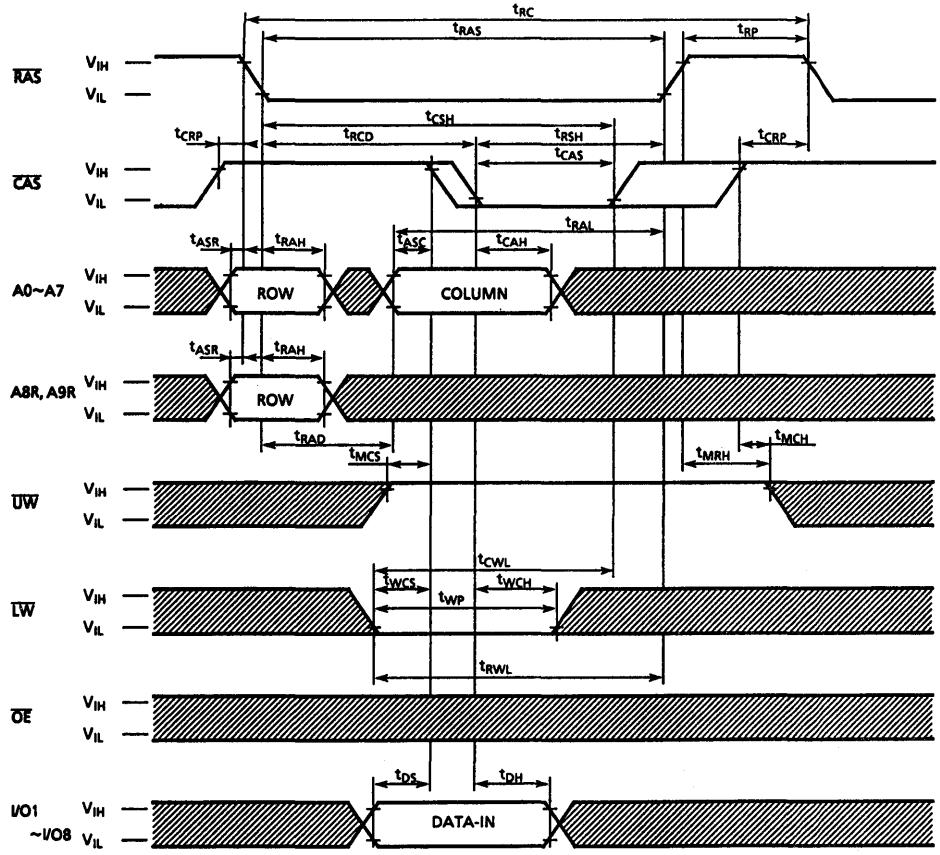
UPPER BYTE READ CYCLE (EARLY WRITE)



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

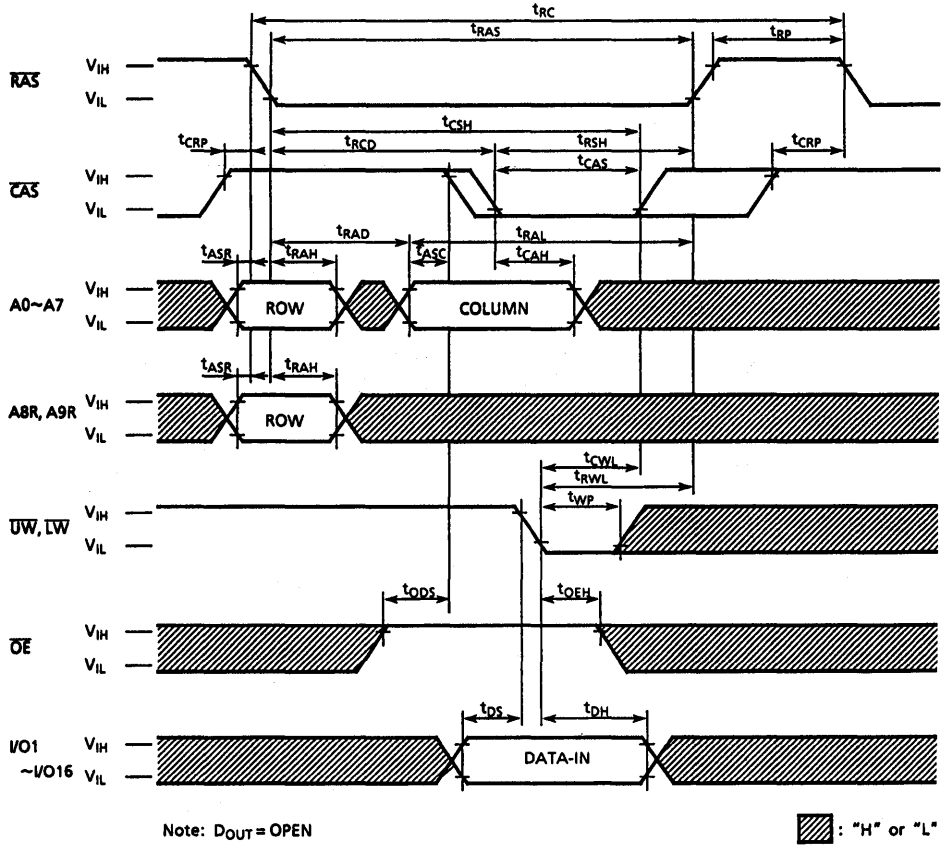
LOWER BYTE READ CYCLE (EARLY WRITE)



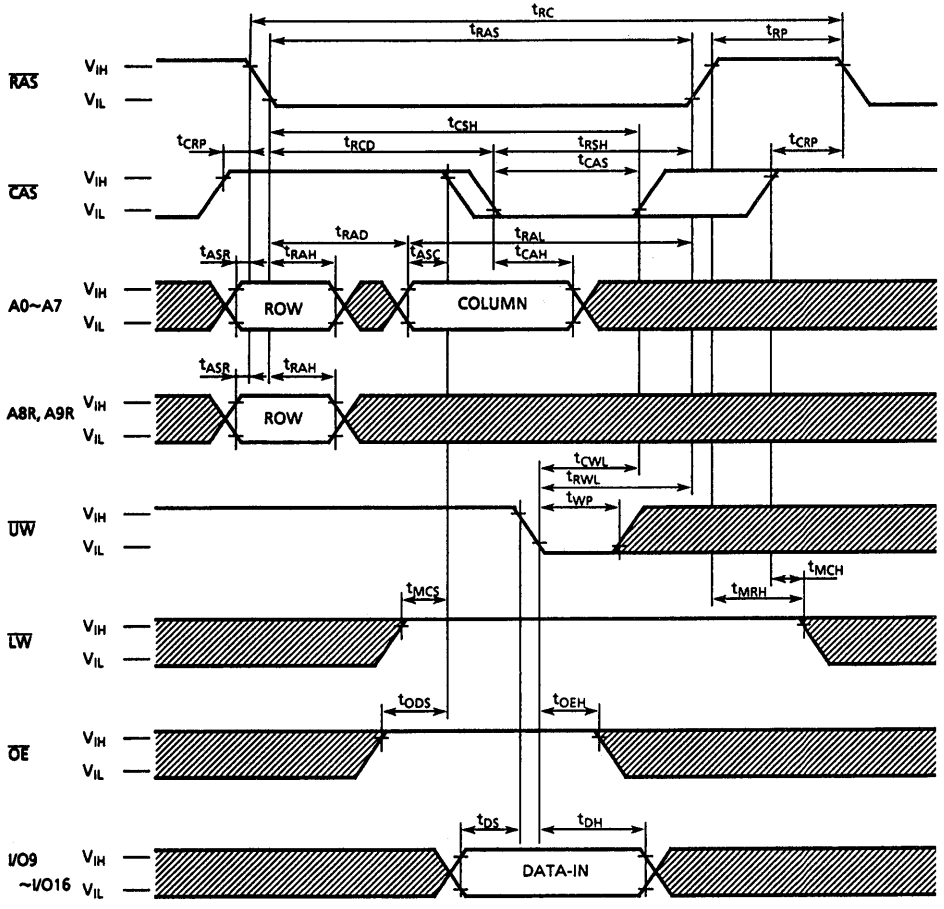
Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

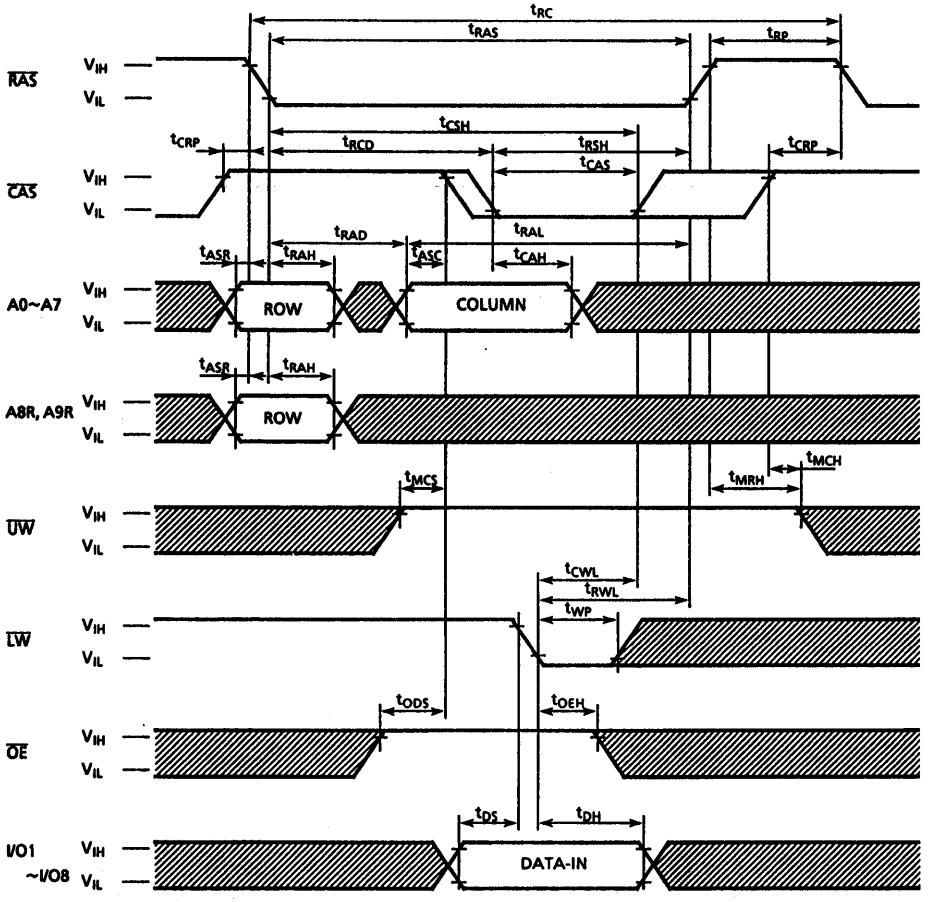


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} = OPEN

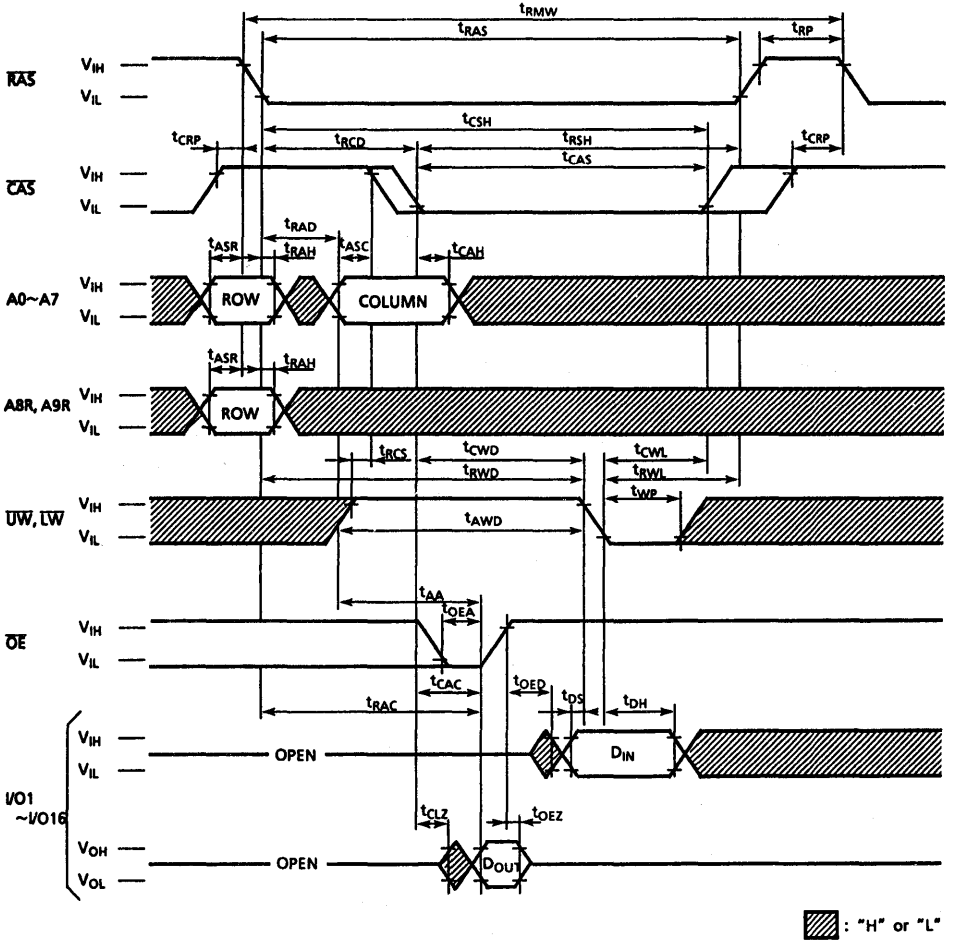
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



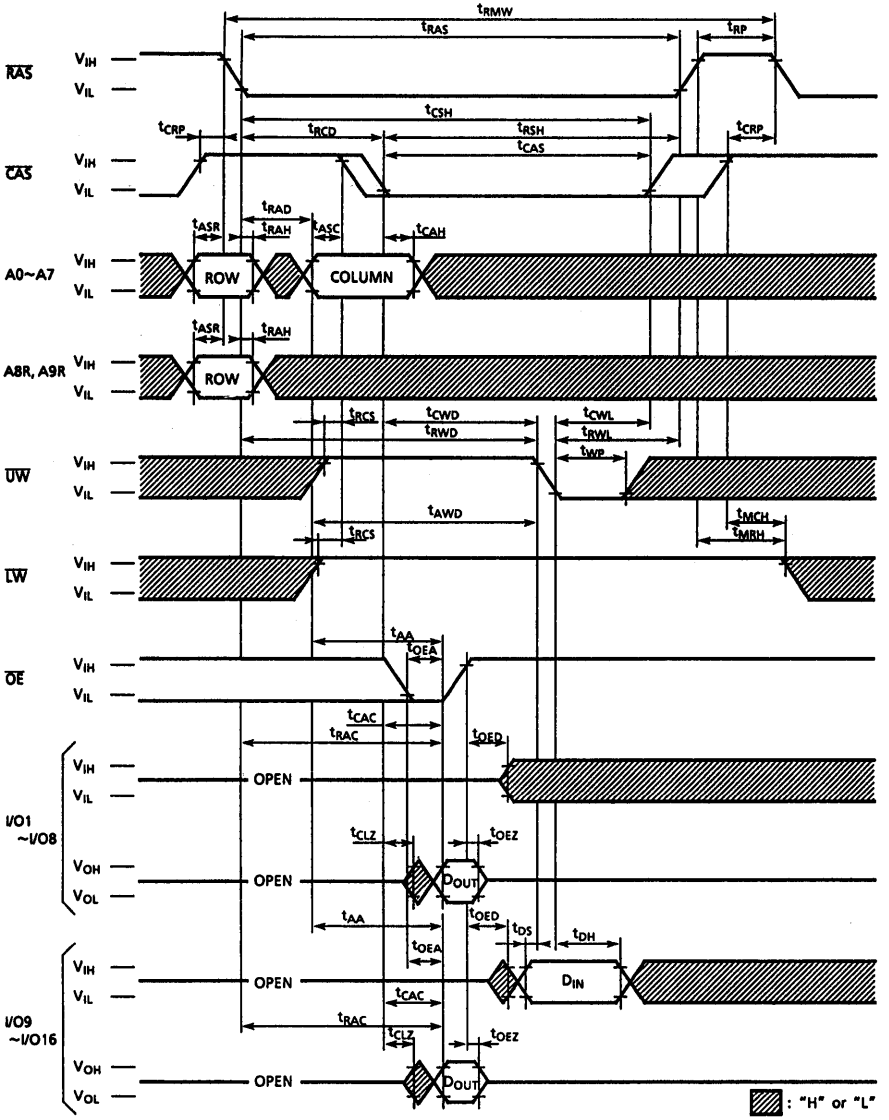
Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} = OPEN

▨ : "H"

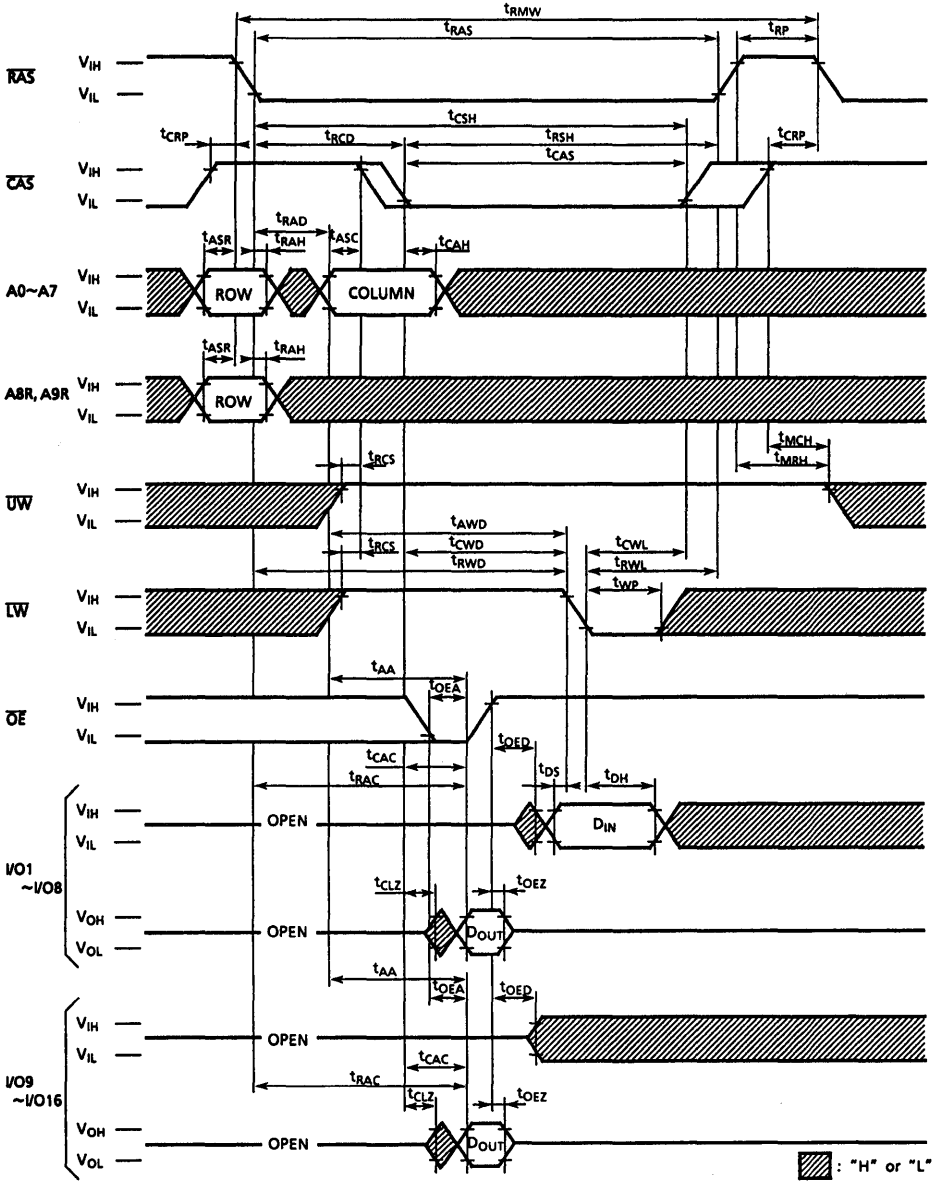
READ-MODIFY-WRITE CYCLE



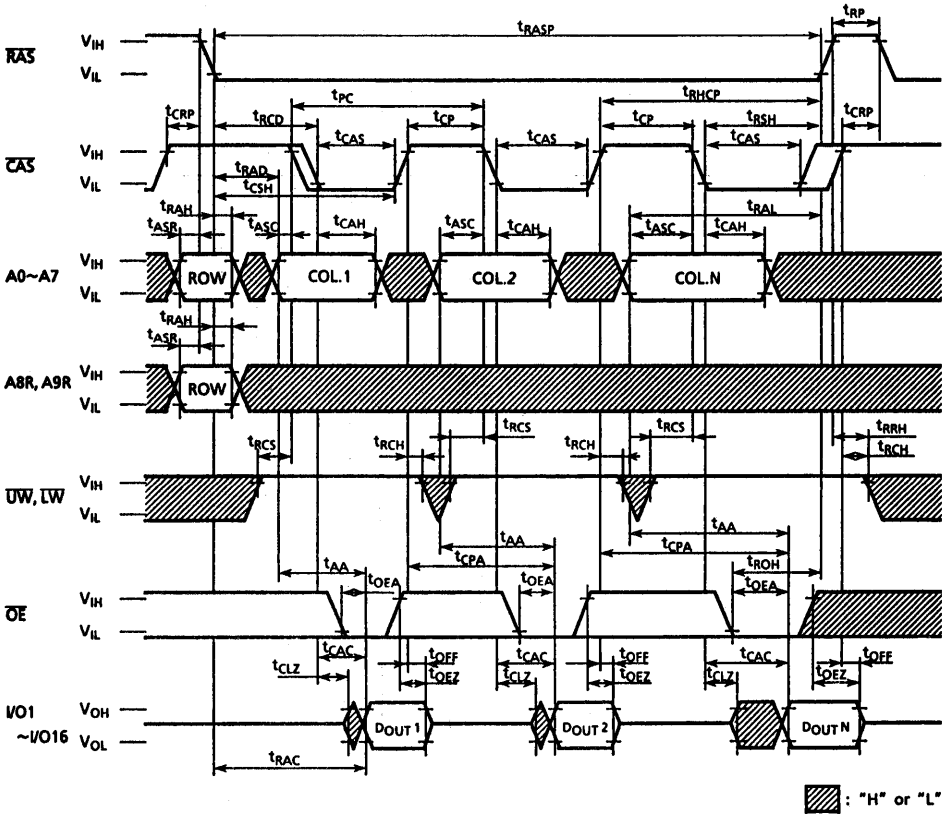
READ-MODIFY-UPPER-BYTE-WRITE CYCLE



READ-MODIFY-LOWER-BYTE-WRITE CYCLE

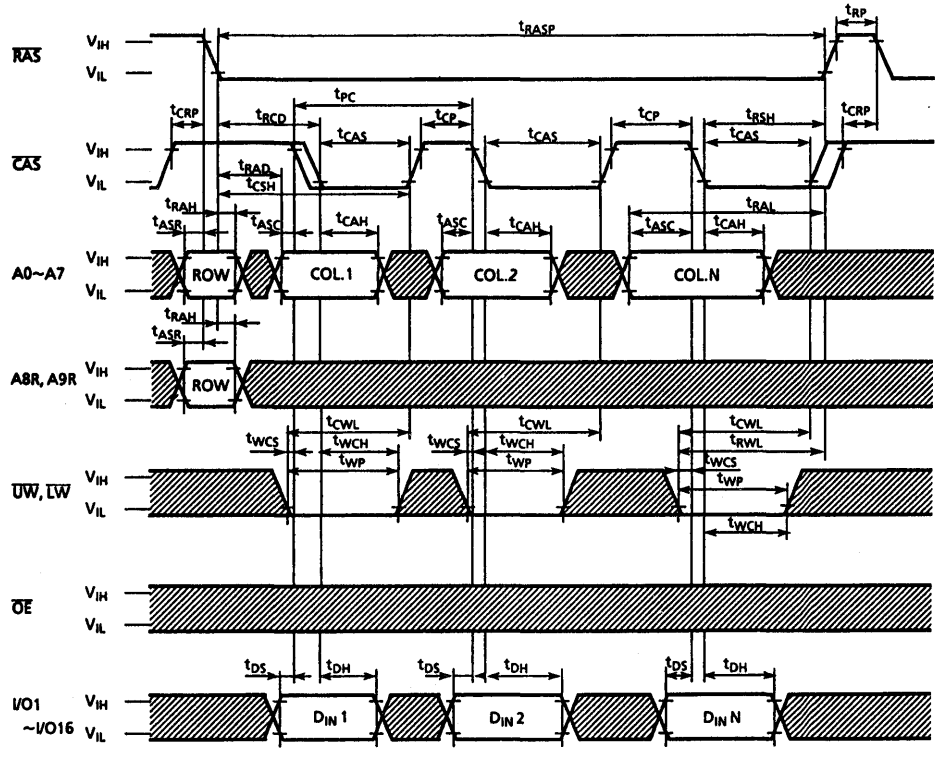


FAST PAGE MODE READ CYCLE

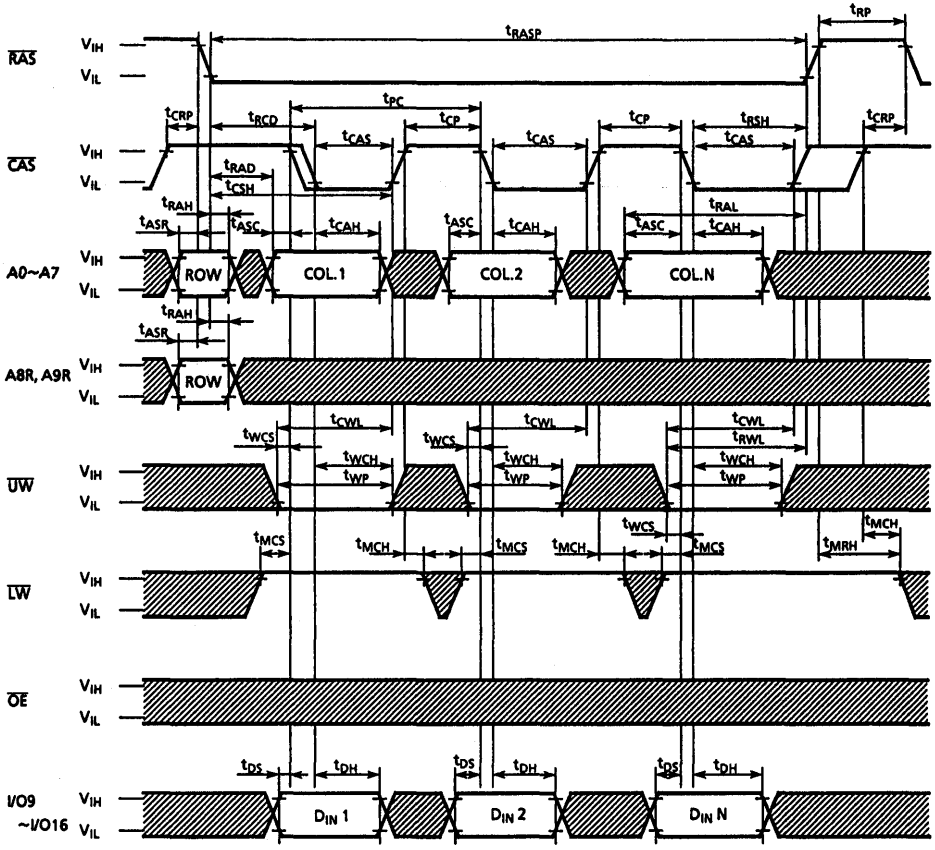


Note: D_{IN} = OPEN

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



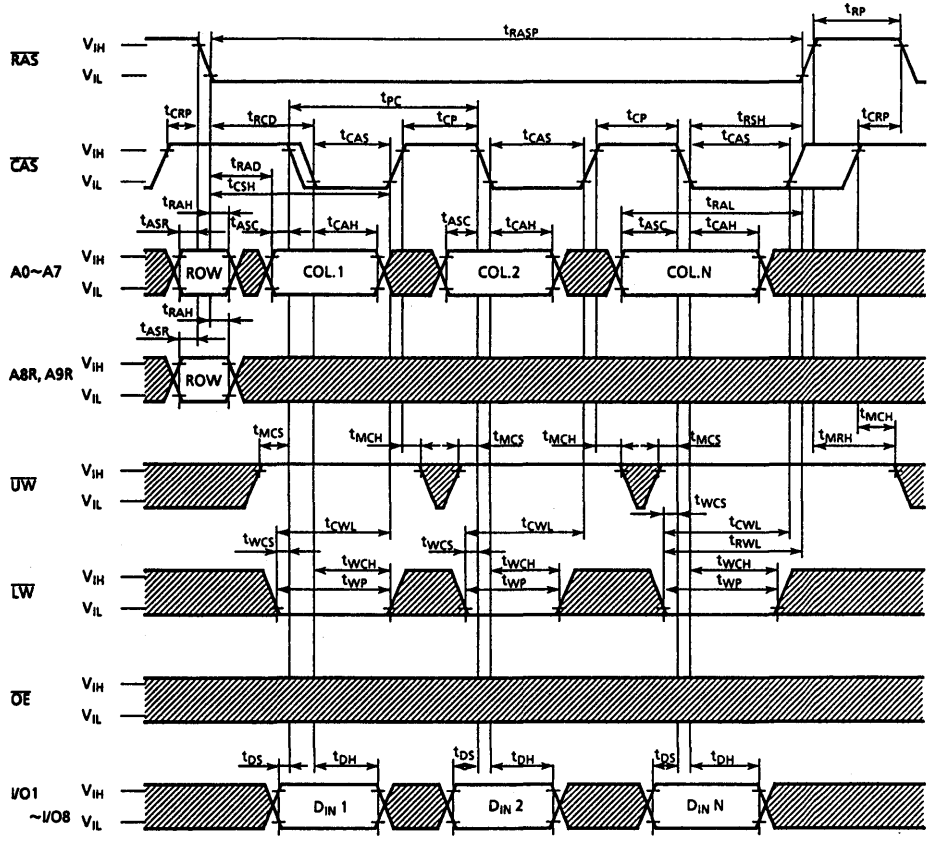
FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

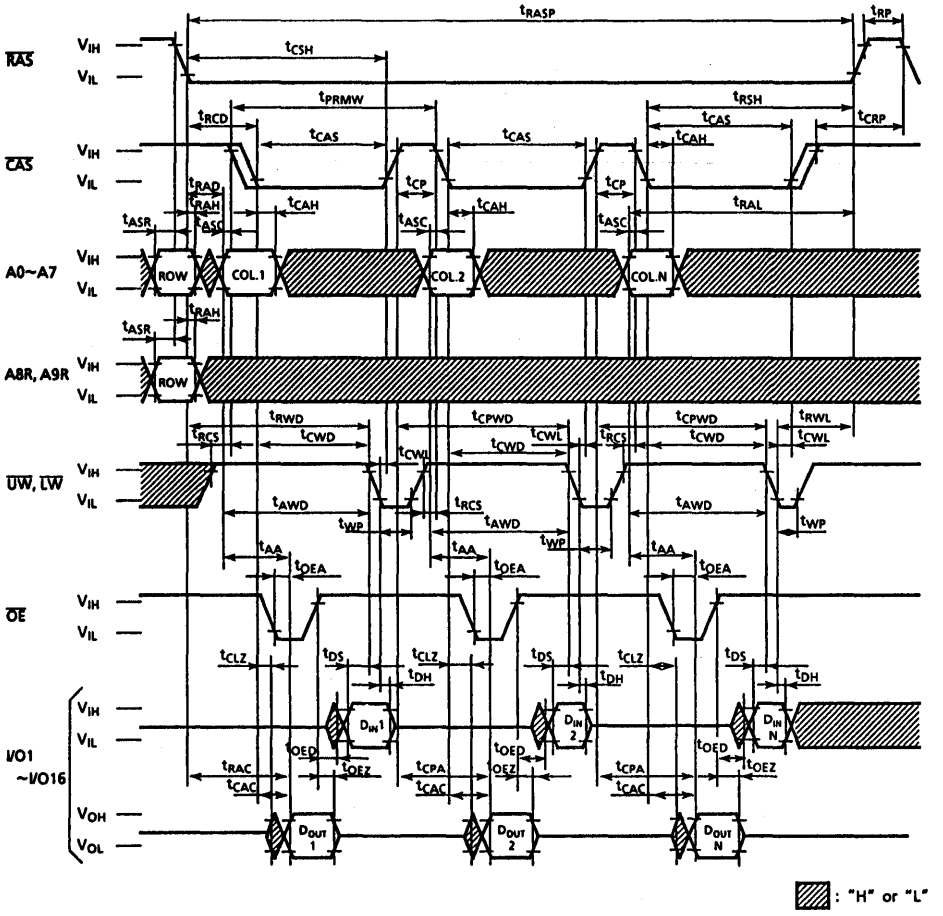
FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)



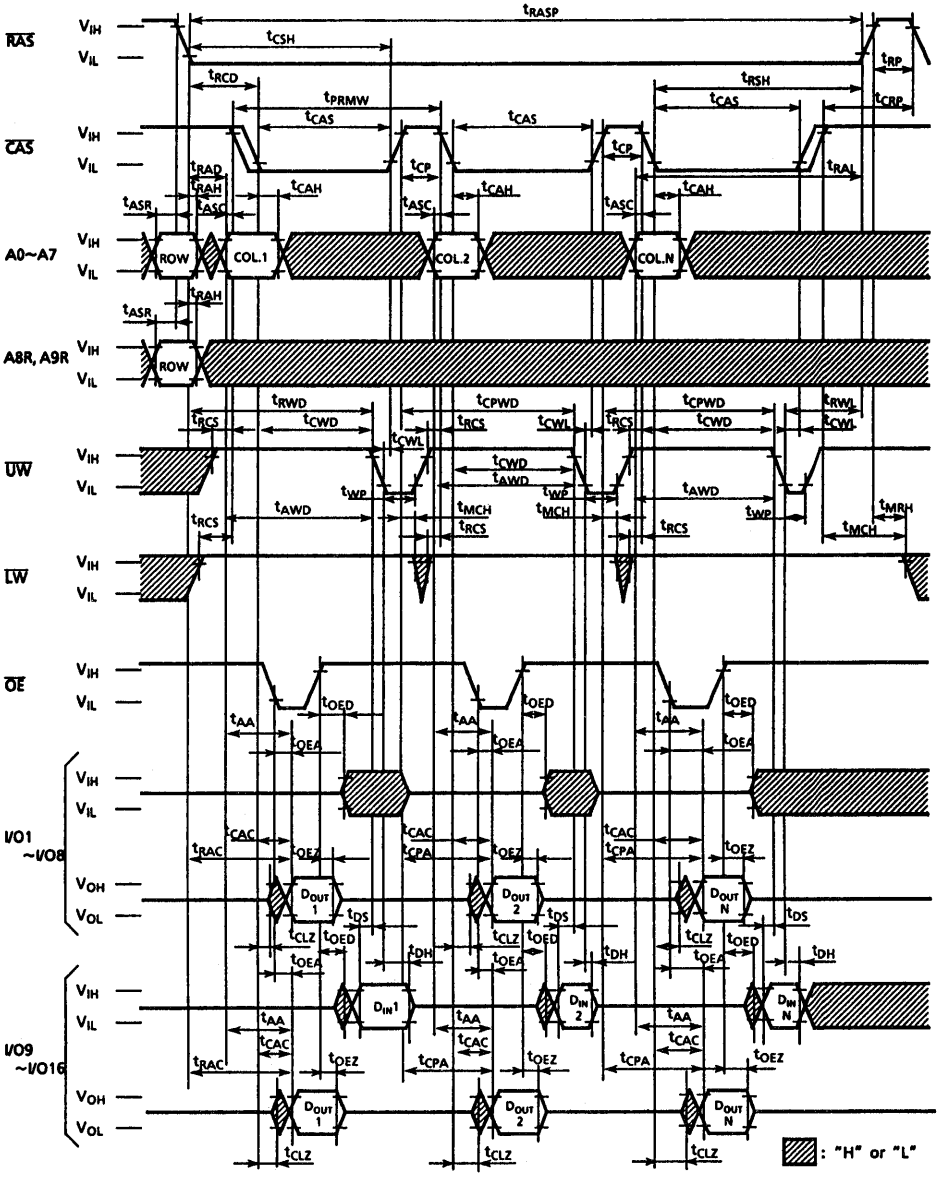
Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

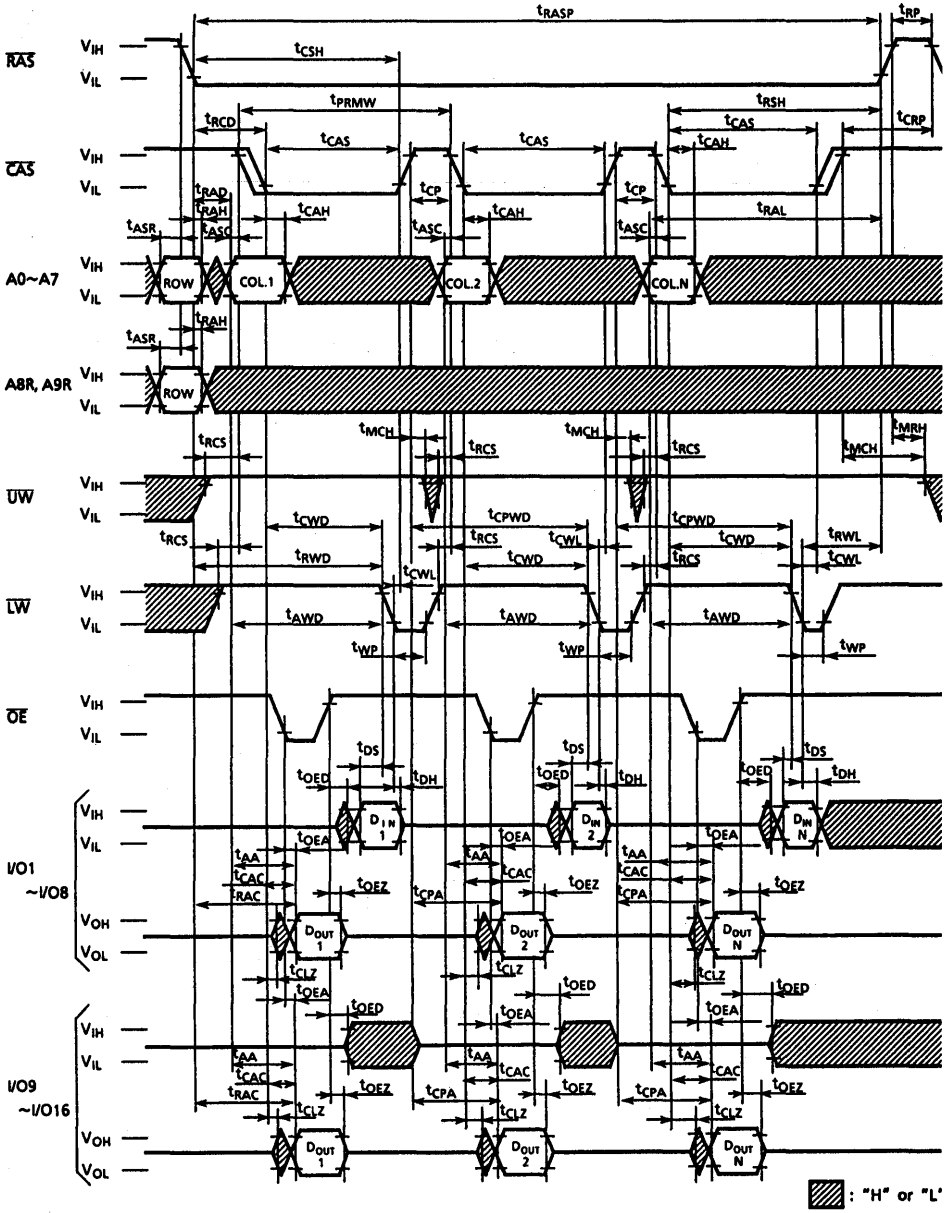
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



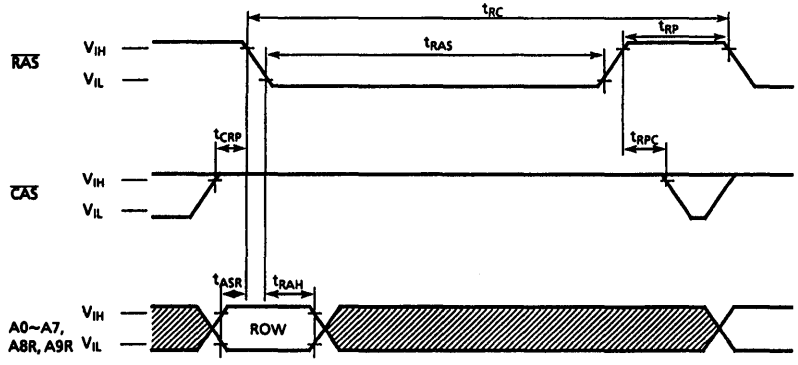
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



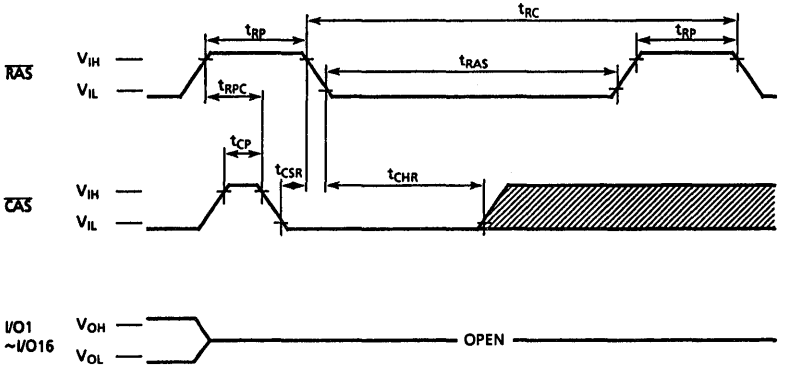
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{UW}$, $\overline{LW}$, $\overline{OE}$ = "H" or "L"
D_{IN} = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

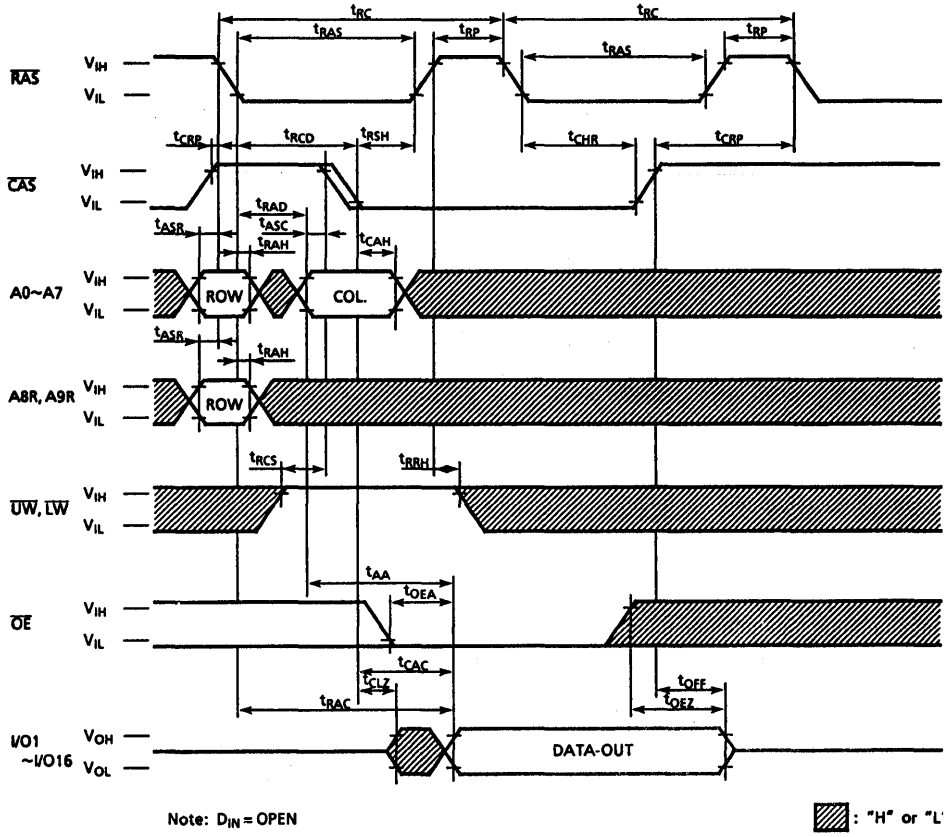
$\overline{CAS}$ BEFORE $\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, A0~A7, A8R, A9R = "H" or "L"
D_{IN} = Don't Care

▨ : "H" or "L"

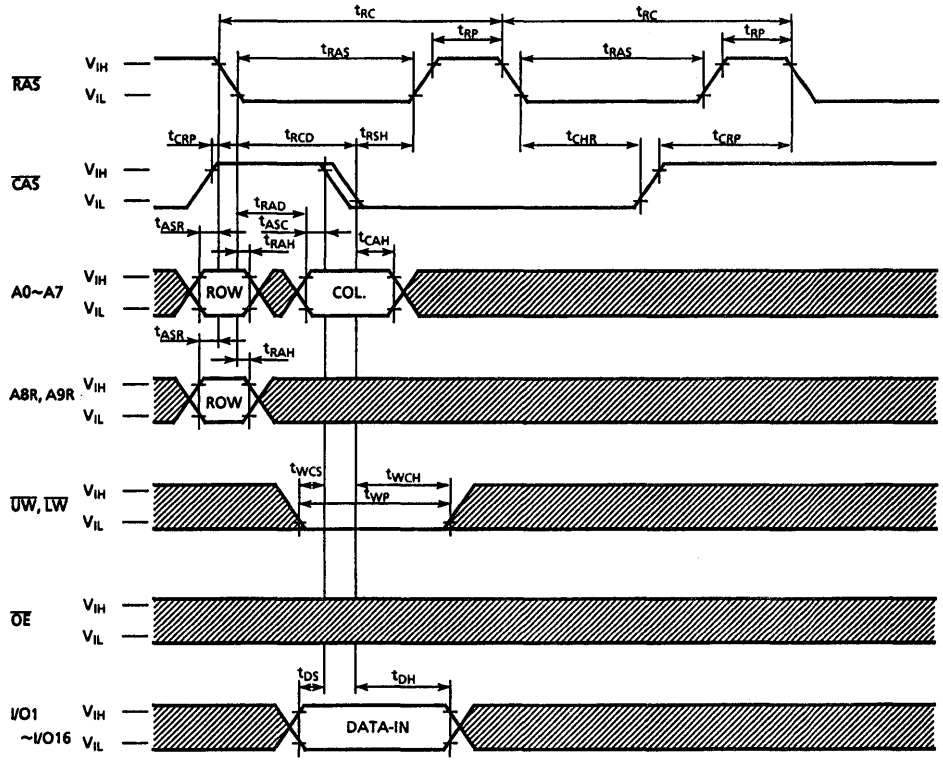
HIDDEN REFRESH CYCLE



Note: D_{IN} = OPEN

▨: "H" or "L"

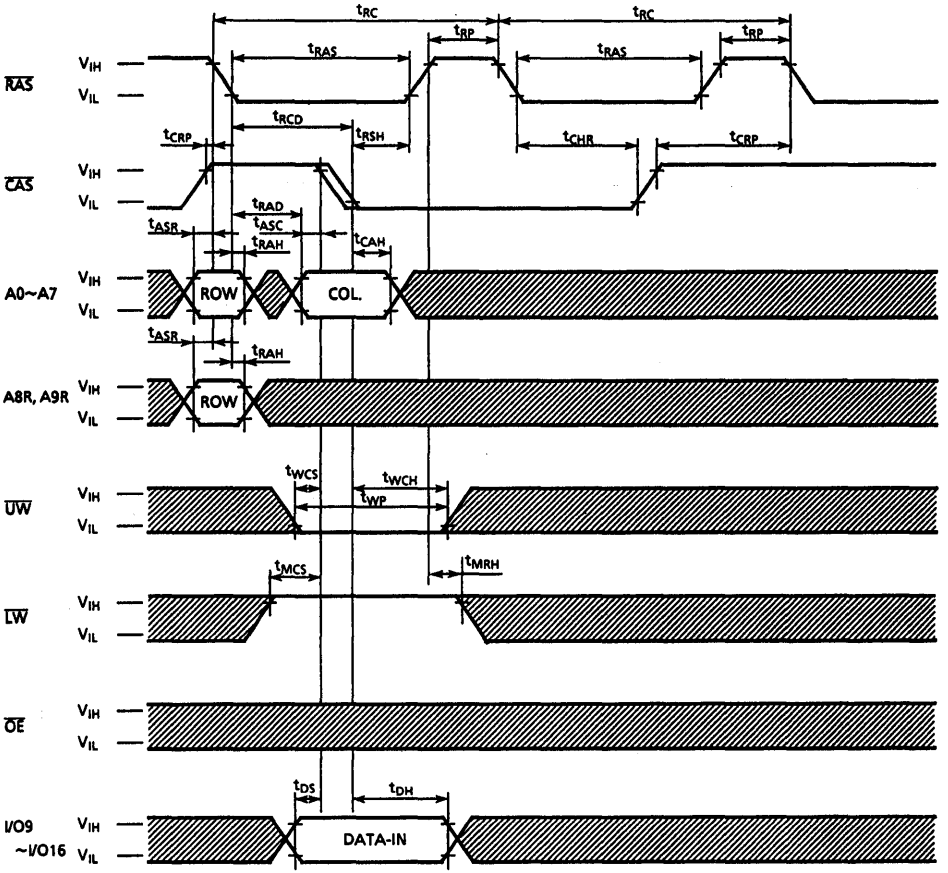
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨: "H" or "L"

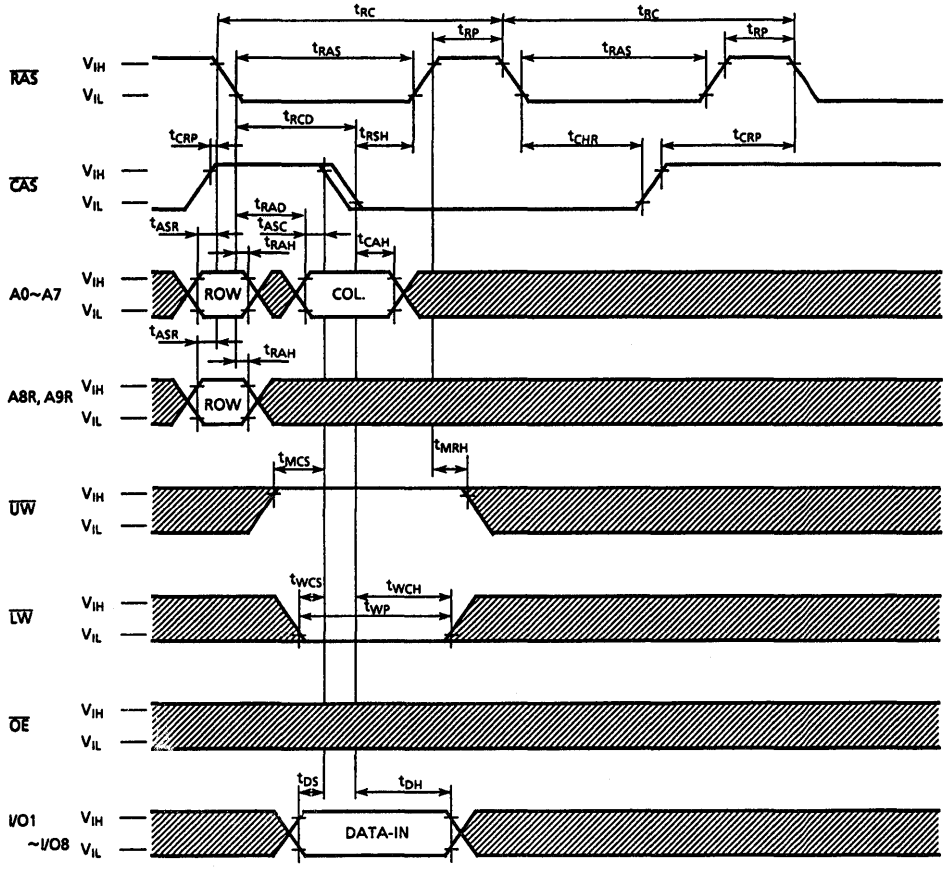
HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

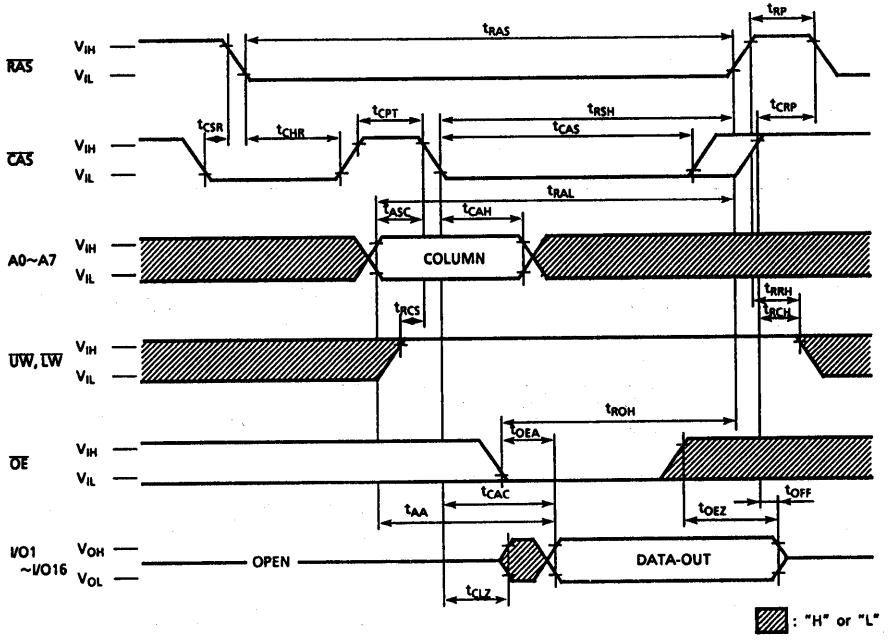
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} = OPEN

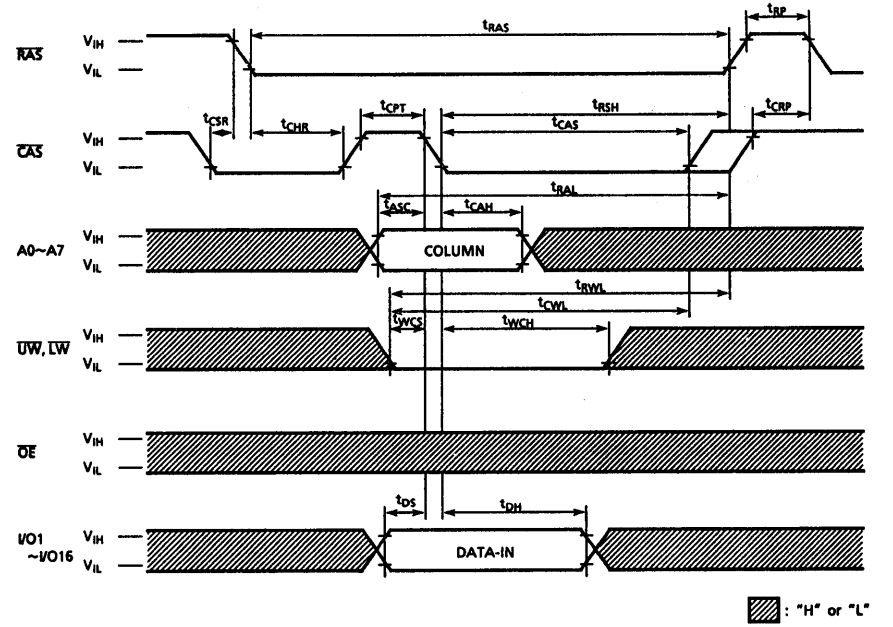
▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



Note: A8R, A9R = "H" or "L"
D_{IN} = OPEN

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



Note: A8R, A9R = "H" or "L"
D_{OUT} = OPEN

262,144 WORD X 16 BIT DYNAMIC RAM

DESCRIPTION

The TC514273BJ is the new generation dynamic RAM organized 262,144 word by 16 bit. The TC514273BJ utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514273BJ to be packaged in a standard 40 pin plastic SOJ. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 262,144 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  550mW MAX .Operating
  (TC514273BJ-70)
  468mW MAX. Operating
  (TC514273BJ-80)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write-Per-Bit and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package TC514273BJ : SOJ40-P-400

KEY PARAMETERS

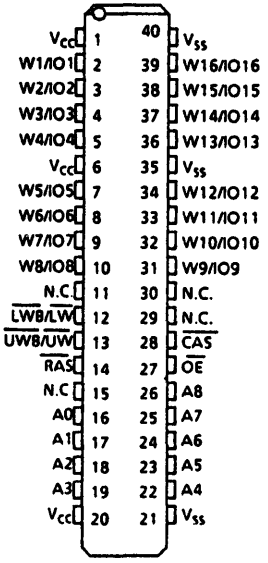
ITEM		TC514273BJ	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

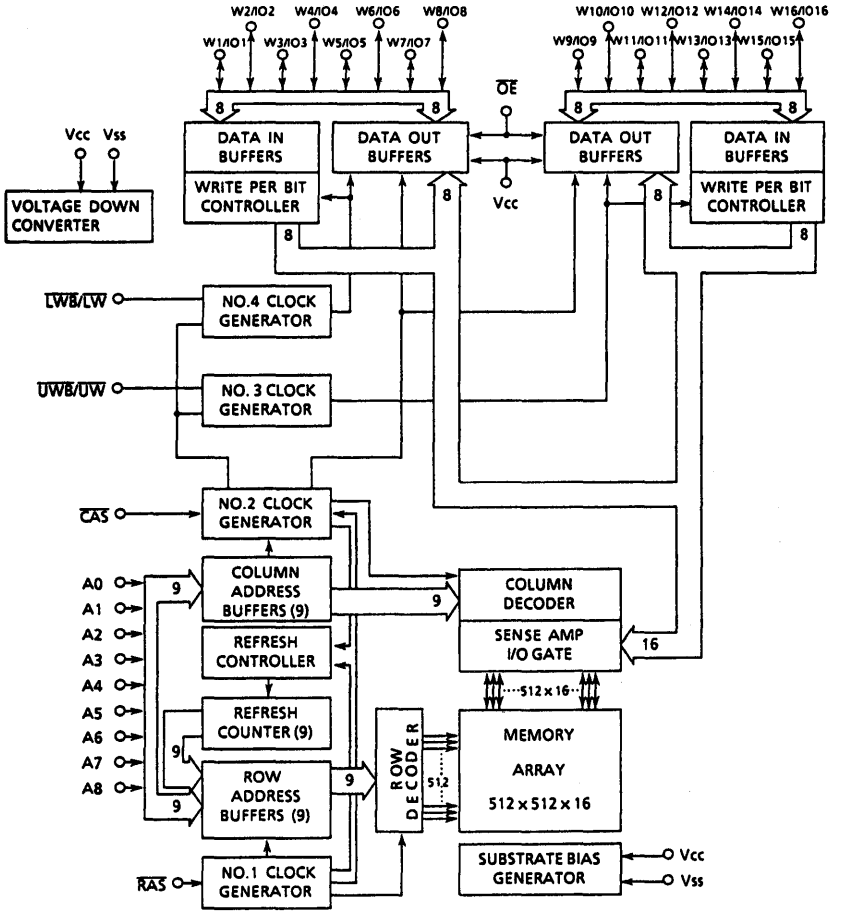
A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UWB}$/UW	Write Per Bit/Read/Upper Byte Write Input
$\overline{LWB}$/$\overline{LW}$	Write Per Bit/Read/Lower Byte Write Input
$\overline{OE}$	Output Enable
W1/IO1~W16/IO16	Write Section/ Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

Plastic SOJ



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7.0$	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	$-55 \sim 150$	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	V_{CC}+0.5	V	2
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V	2

*-2.0V at pulse width ≤ 20ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514273BJ-70	-	100	mA	3,4 5
		TC514273BJ-80	-	85		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514273BJ-70	-	100	mA	3, 5
		TC514273BJ-80	-	85		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC}MIN.)	TC514273BJ-70	-	70	mA	3,4 5
		TC514273BJ-80	- d	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$,Cycling: t_{RC}=t_{PC} MIN.)	TC514273BJ-70	-	100	mA	3, 5
		TC514273BJ-80	-	85		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤V_{CC}, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤V_{CC})		-10	10	μA	
V_{OH}	OUTPUT CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT CURRENT Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC514273BJ				UNIT	NOTES
		-70		-80			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ Presharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold TIme	15	-	15	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC514273BJ				UNIT	NOTES
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	-	50	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	-	110	-	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	-	70	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	70	-	75	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	-	30	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10		ns	
t_{OEA}	$\overline{OE}$ Access TIme	-	20	0	20	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	
t_{MCS}	Masked Write Set-Up Time	0	-	0	-	ns	
t_{MRH}	Masked Write Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	16
t_{MCH}	Masked Write Hold Time referenced to $\overline{CAS}$	0	-	0	-	ns	16
t_{WBS}	Write Per Bit Set-Up Time	0	-	0	-	ns	
t_{WBH}	Write Per Bit Hold Time	10	-	10	-	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	-	0	-	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	-	10	-	ns	

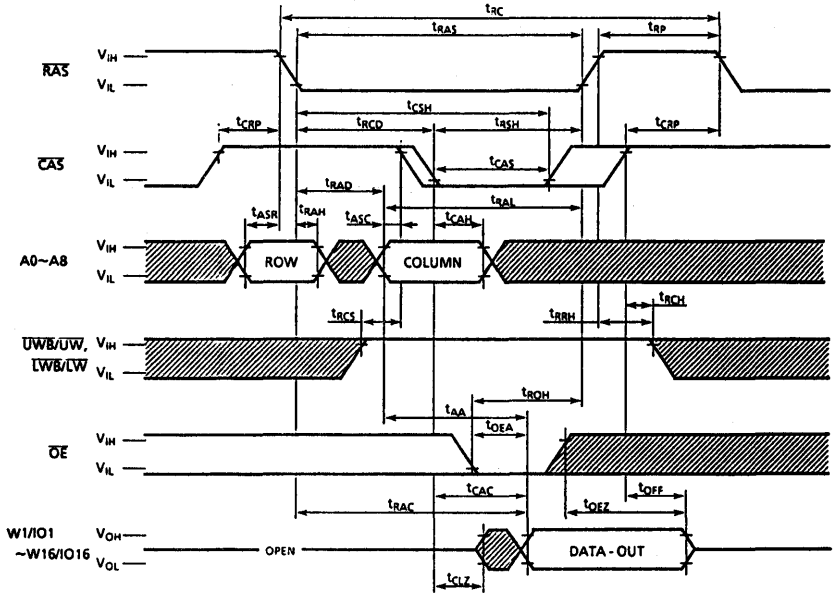
CAPACITANCE (V_{CC} = 5V ± 10%,f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{UWB}$/UW, $\overline{LWB}$/LW,$\overline{OE}$))	-	7	pF
C_O	Input Capacitance (W1/IO1~W16/IO16)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume t_T=5ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieveS the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to ($\overline{UWB}$/) $\overline{UW}$, ($\overline{LWB}$/) $\overline{LW}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWP} > t_{CPWDD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
16. Either t_{MCH} or t_{MRH} must be satisfied for a byte write cycle.

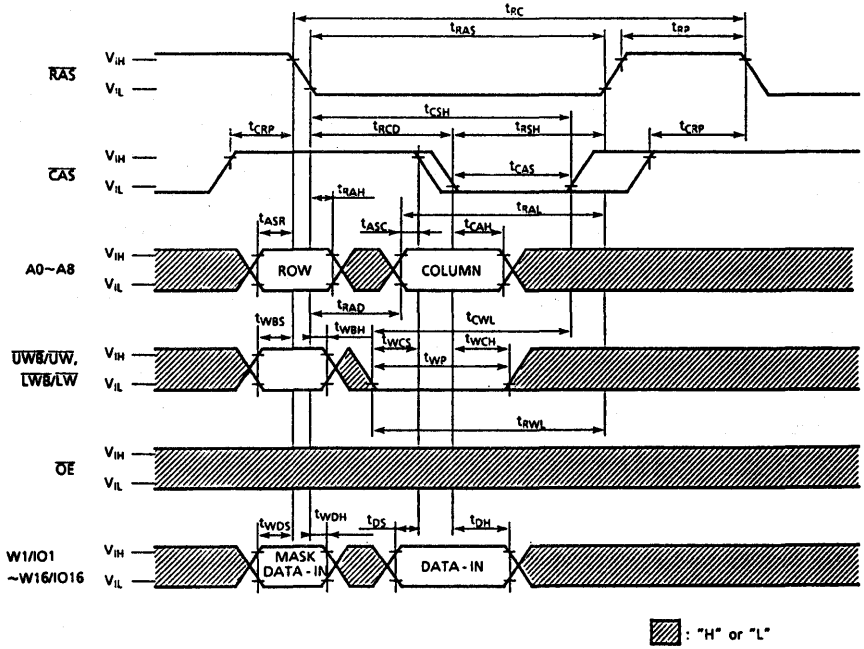
READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

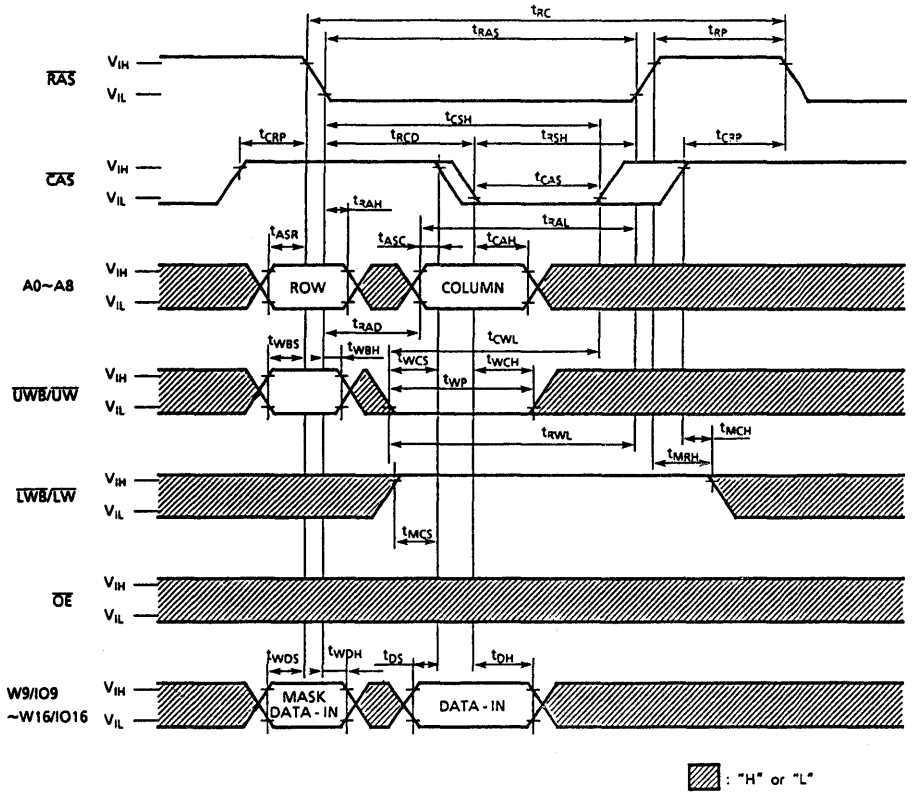
WRITE CYCLE (EARLY WRITE)



▨ : "H" or "L"

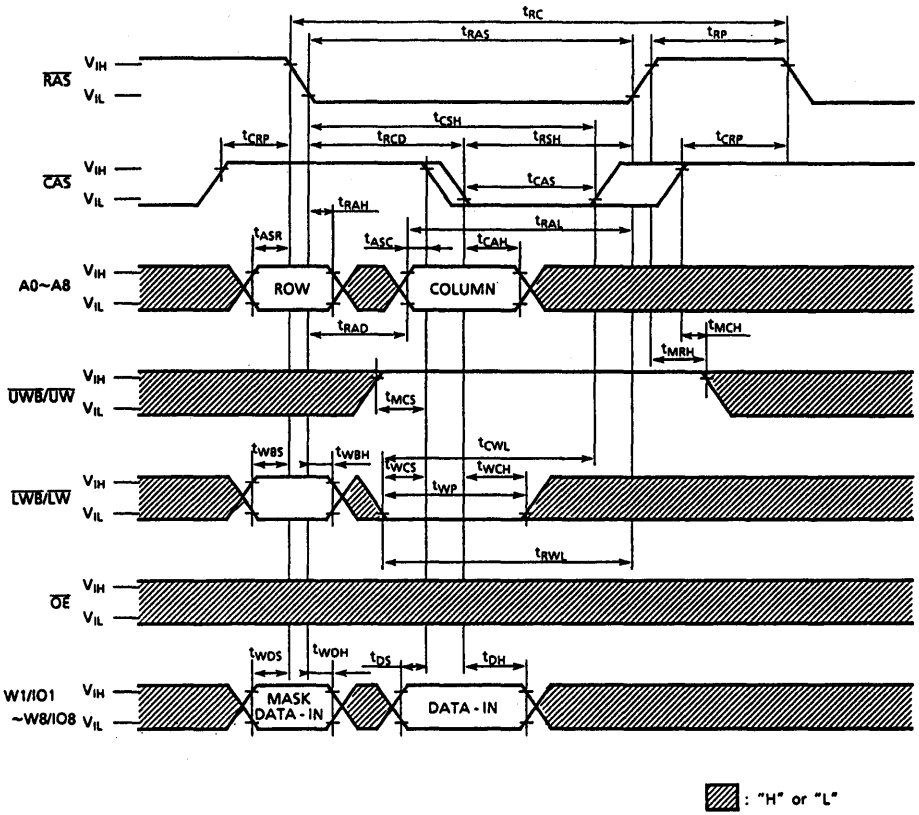
Note: D_{OUT} = OPEN

UPPER BYTE WRITE CYCLE (EARLY WRITE)



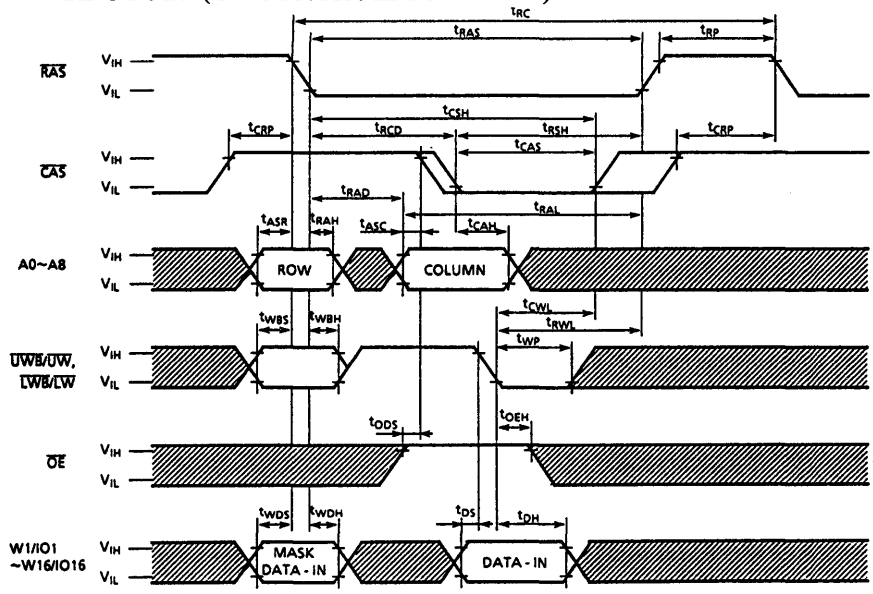
Note: D_{IN} (W1/IO1~W8/IO8) = Don't Care
D_{OUT} = OPEN

LOWER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{IN} (W9/IO9~W16/IO16) = Don't Care
D_{OUT} = OPEN

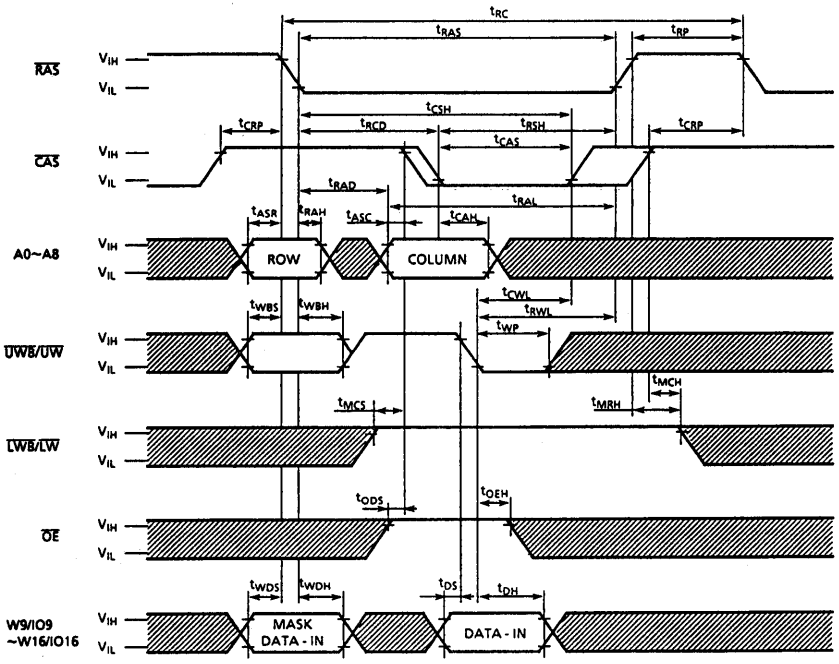
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

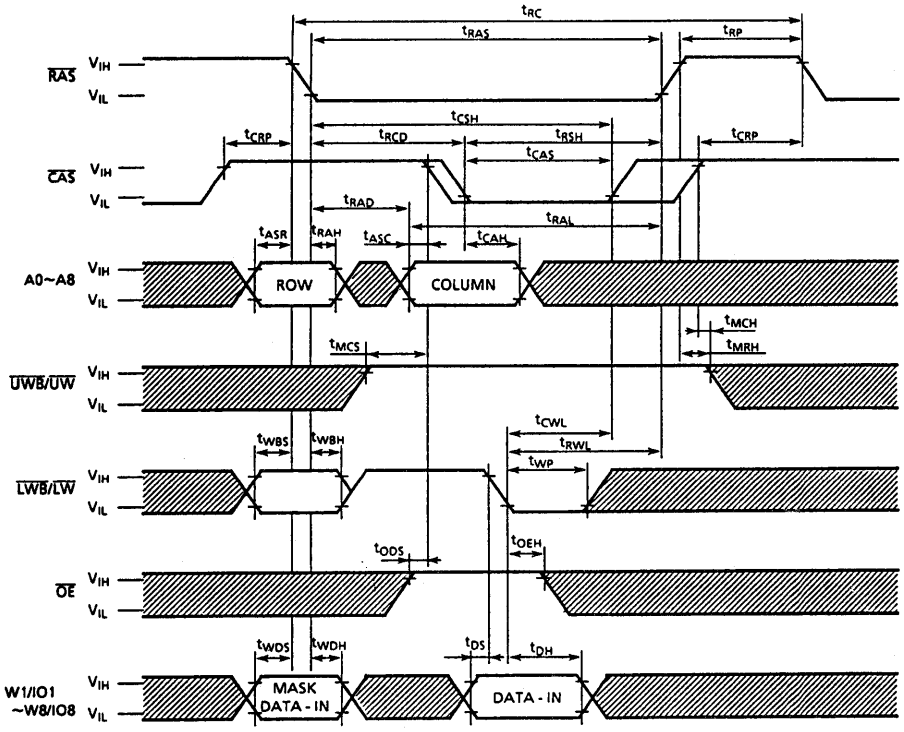
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{IN} (W1/IO1~W8/IO8) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

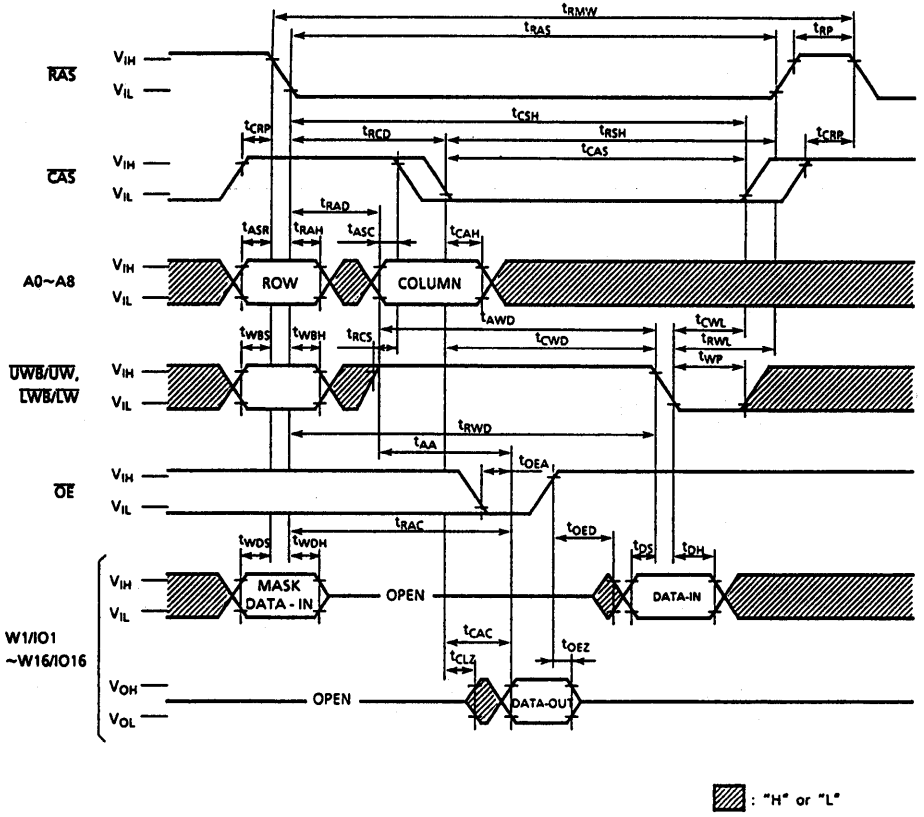
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



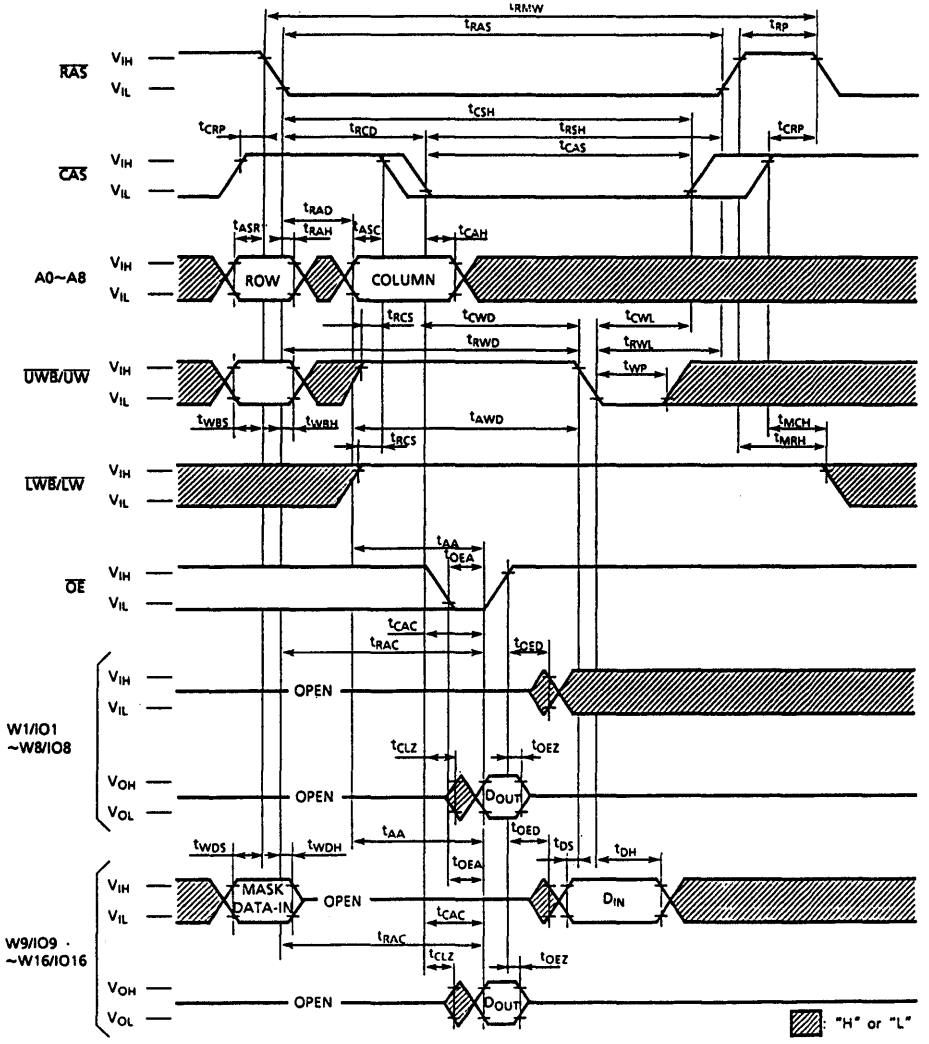
Note: D_{IN} (W9/IO9~W16/IO16) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

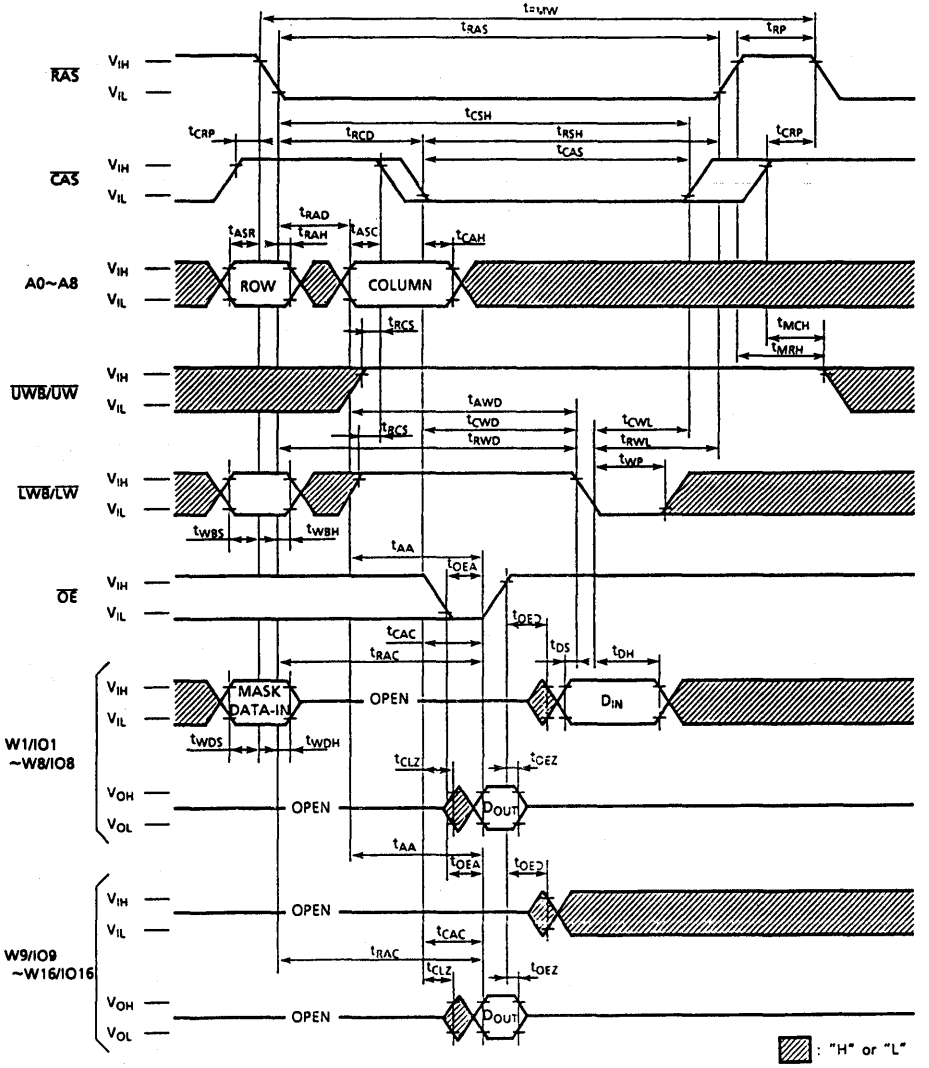
READ-MODIFY-WRITE CYCLE



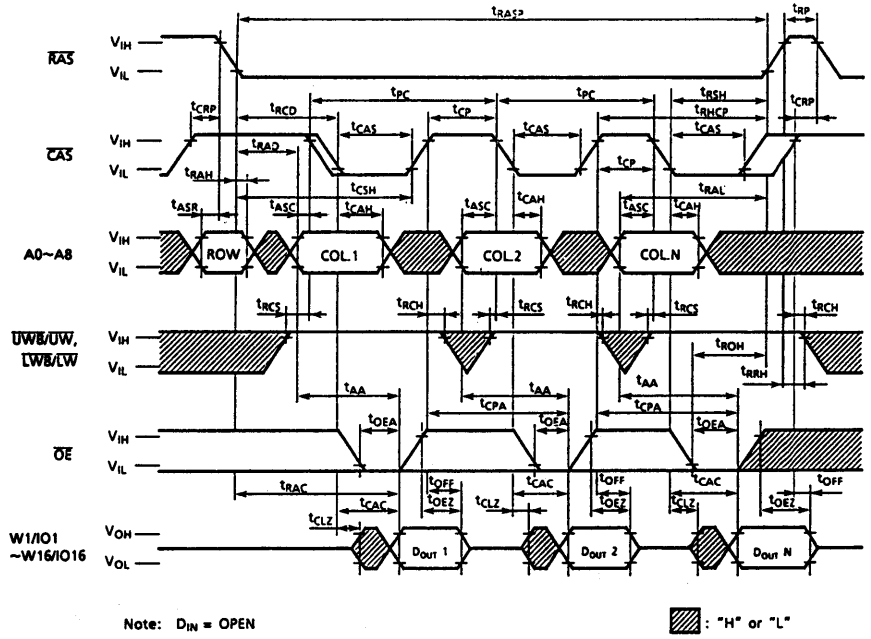
READ-MODIFY-UPPER-BYTE-WRITE CYCLE



READ-MODIFY-LOWER-BYTE-WRITE CYCLE



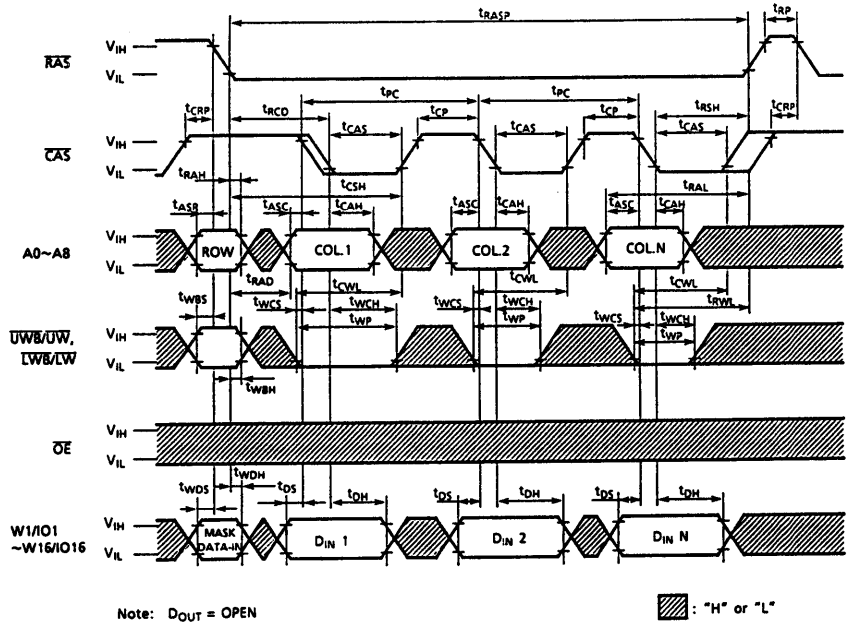
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨: "H" or "L"

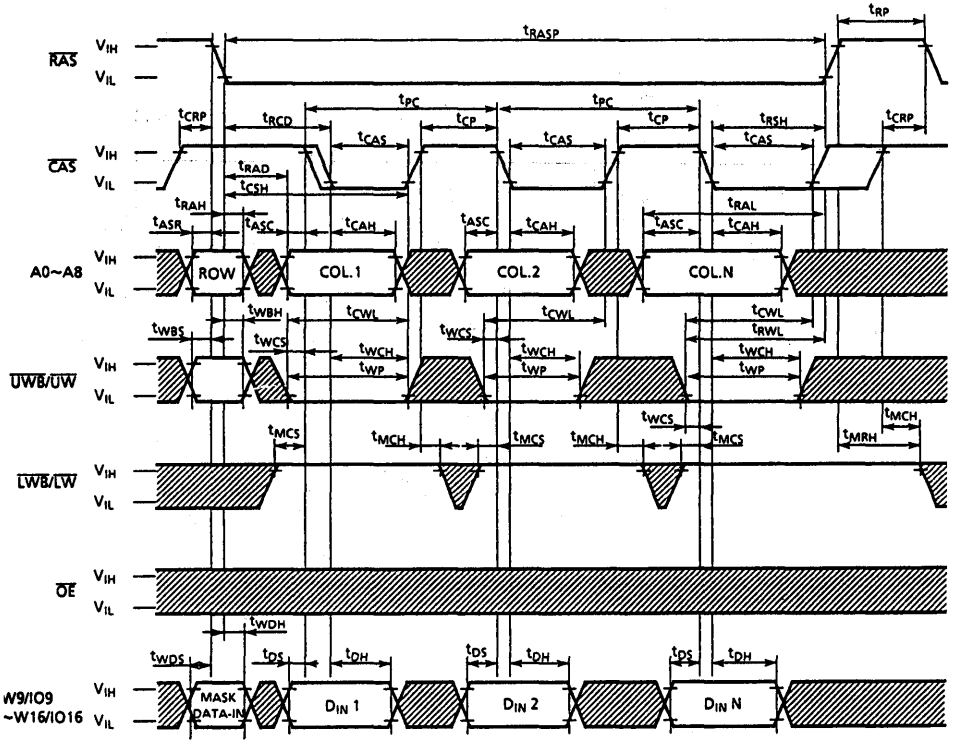
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

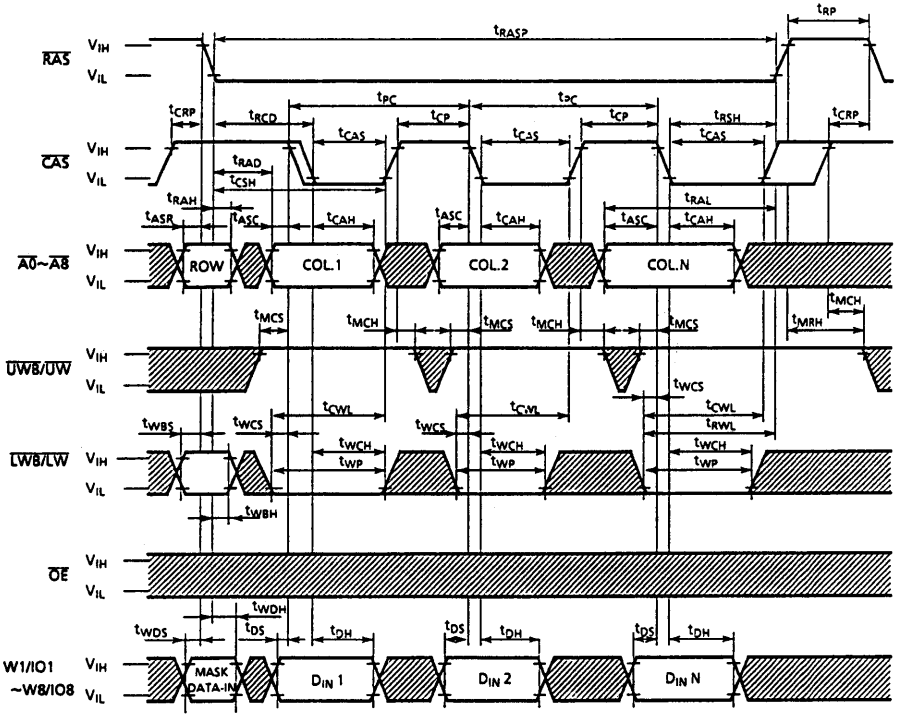
▨: "H" or "L"

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{IN} (W1/IO1~W8/IO8) = Don't Care
D_{OUT} = OPEN

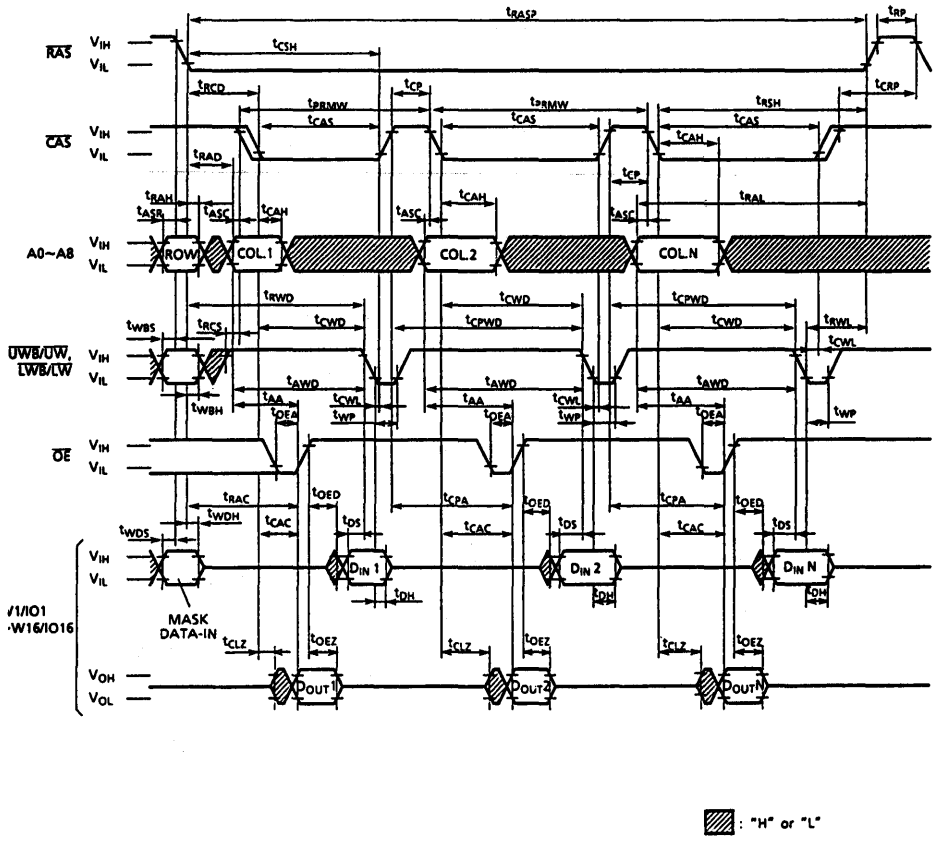
FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)



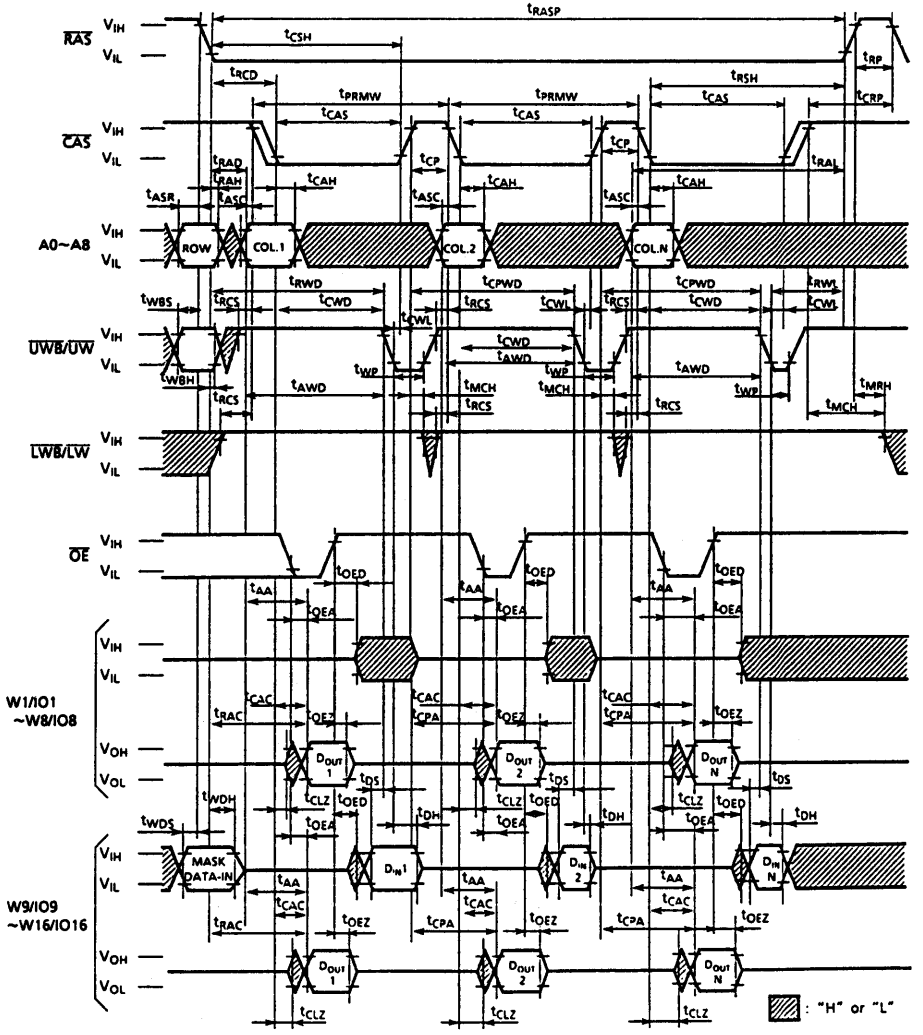
Note: D_{IN} (W9/IO9~W16/IO16) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

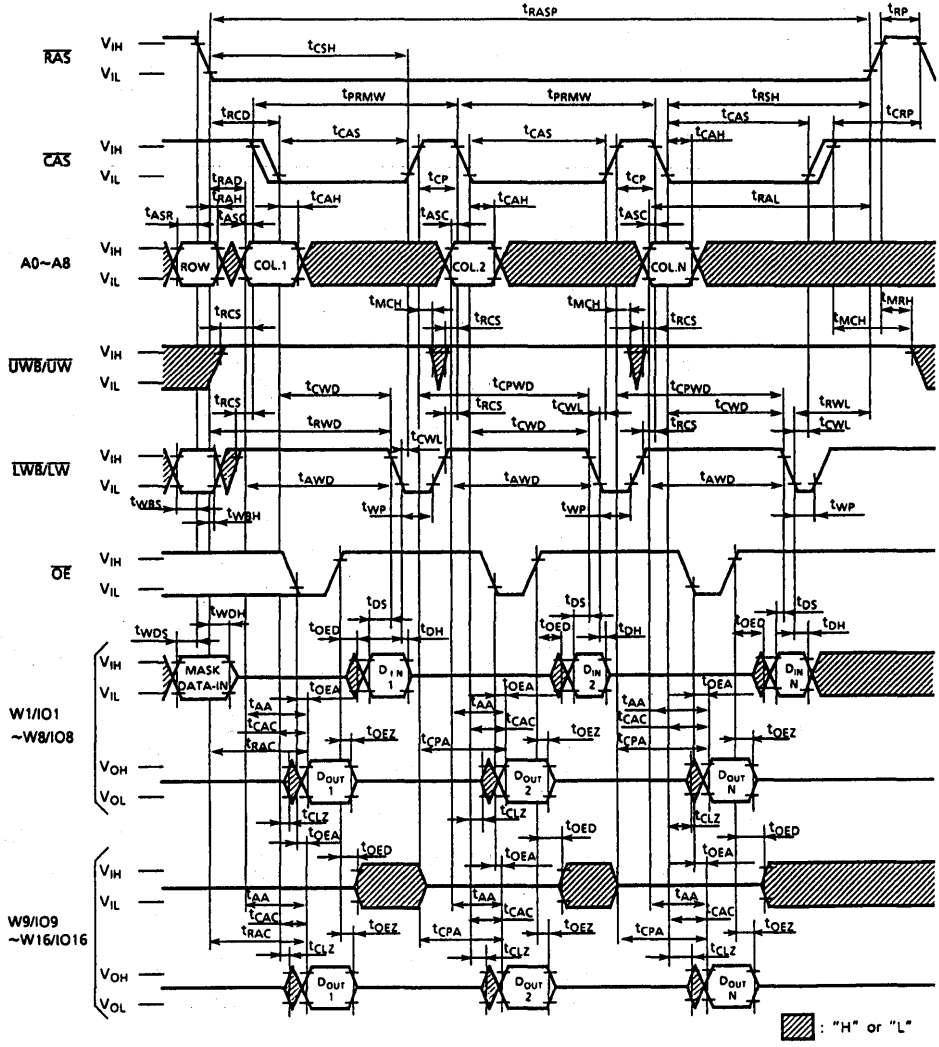
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



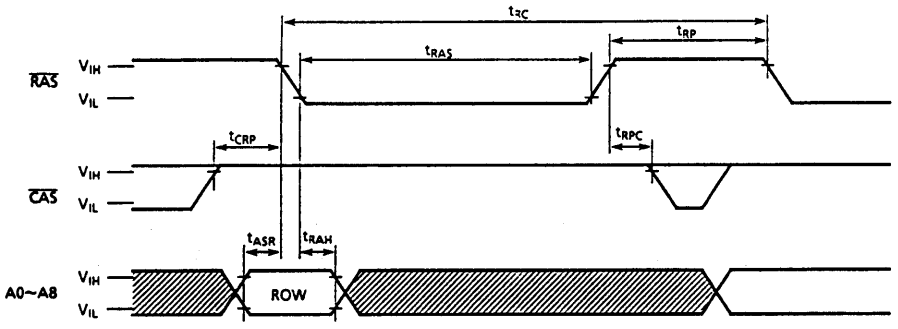
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



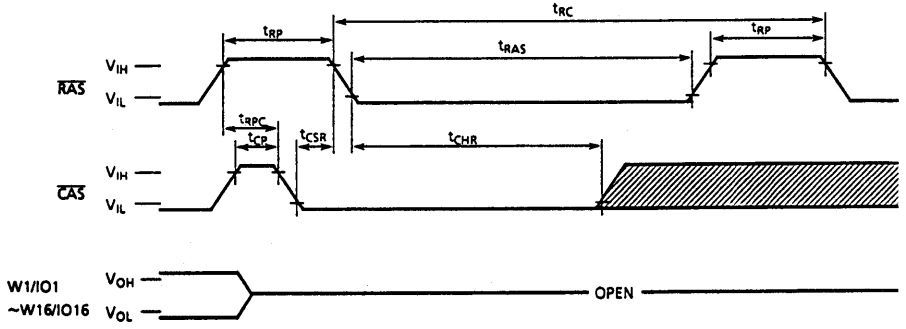
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{UWB}/\overline{UW}$, $\overline{LWB}/\overline{LW}$, $\overline{OE}$ = "H" or "L"
D_{IN} = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

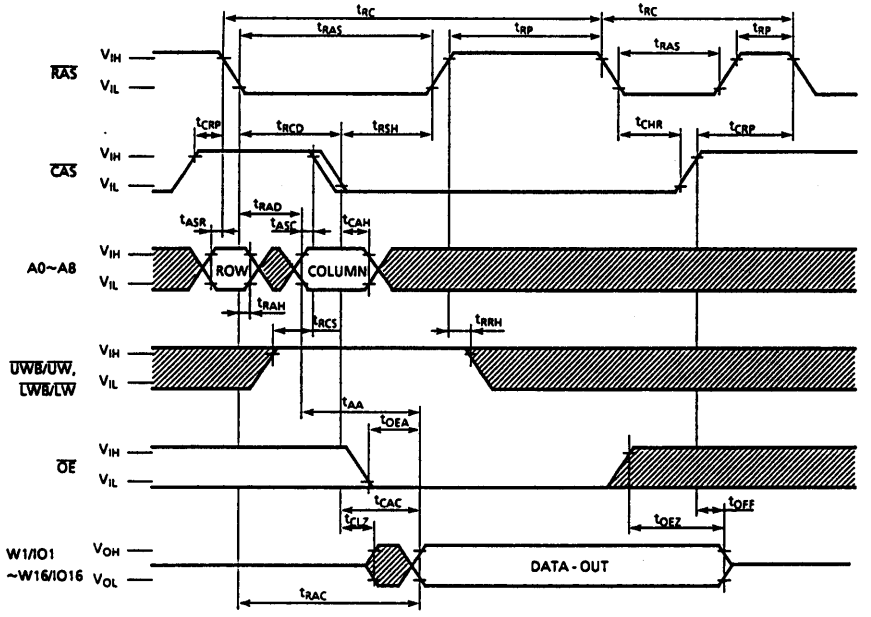
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: $\overline{UWB}/\overline{UW}$, $\overline{LWB}/\overline{LW}$, $\overline{OE}$, A0~A8 = "H" or "L"
D_{IN} = Don't Care

▨ : "H" or "L"

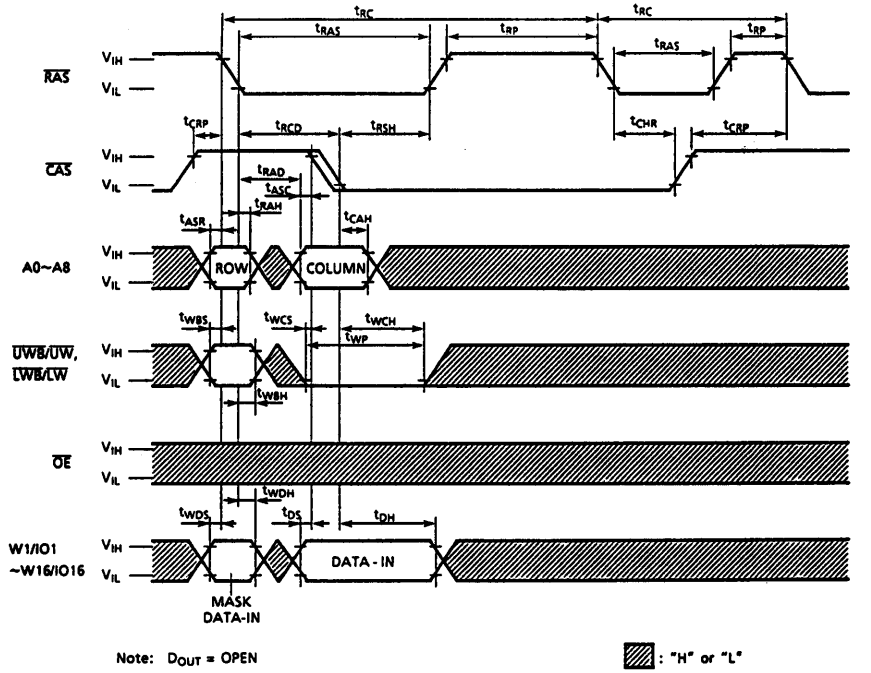
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨ : "H" or "L"

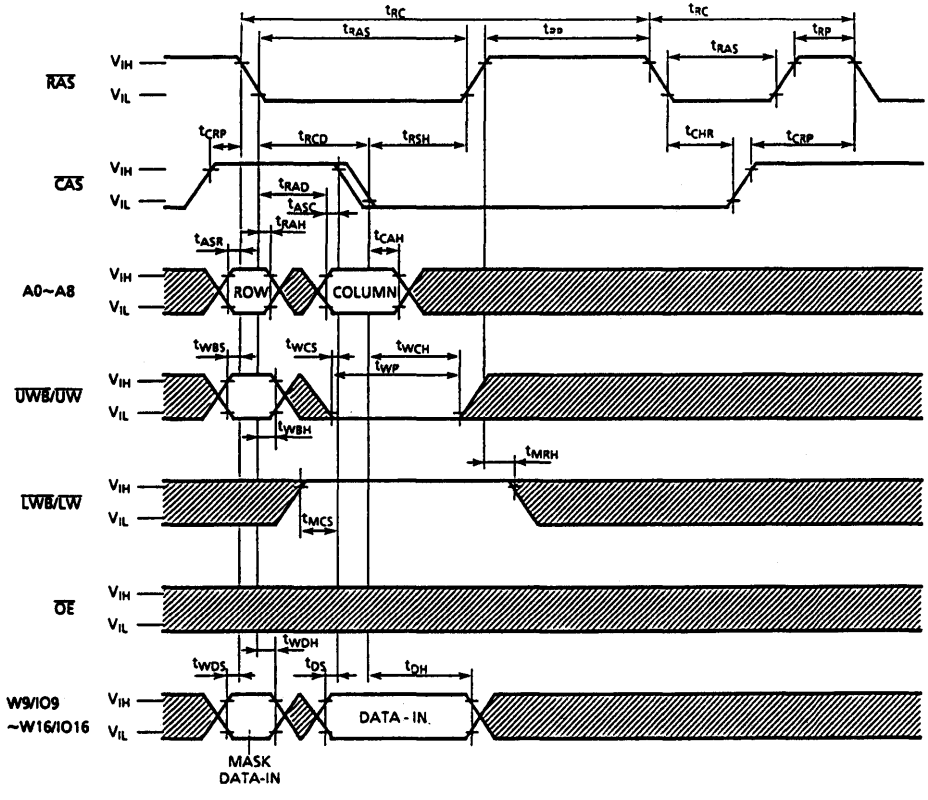
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

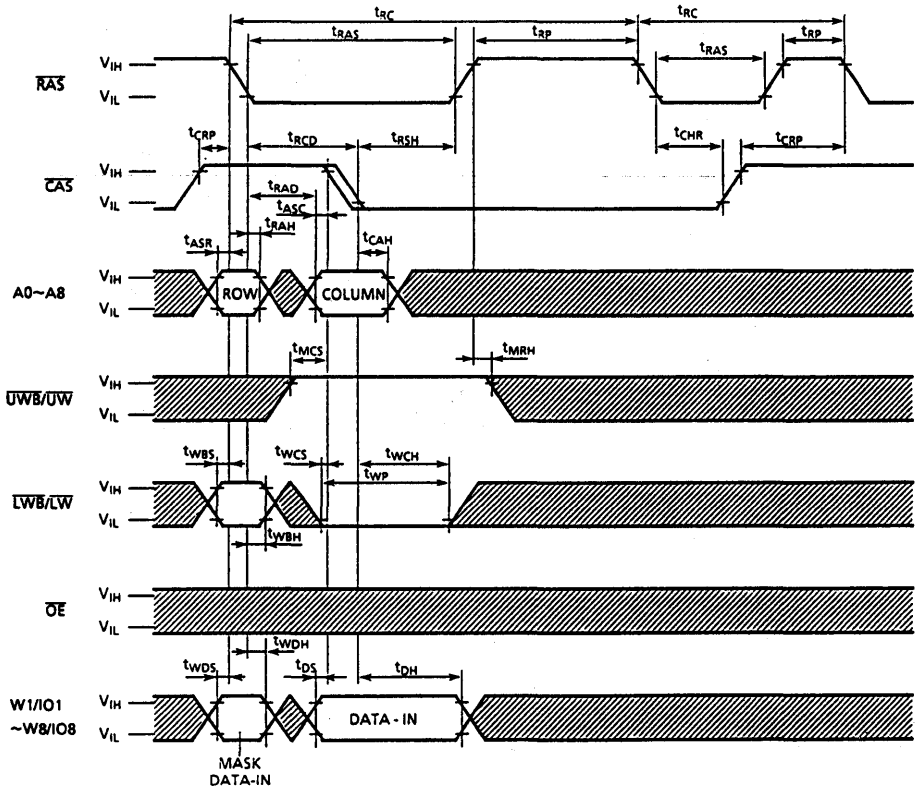
HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Note : D_{IN} (W1/IO1~W8/IO8) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

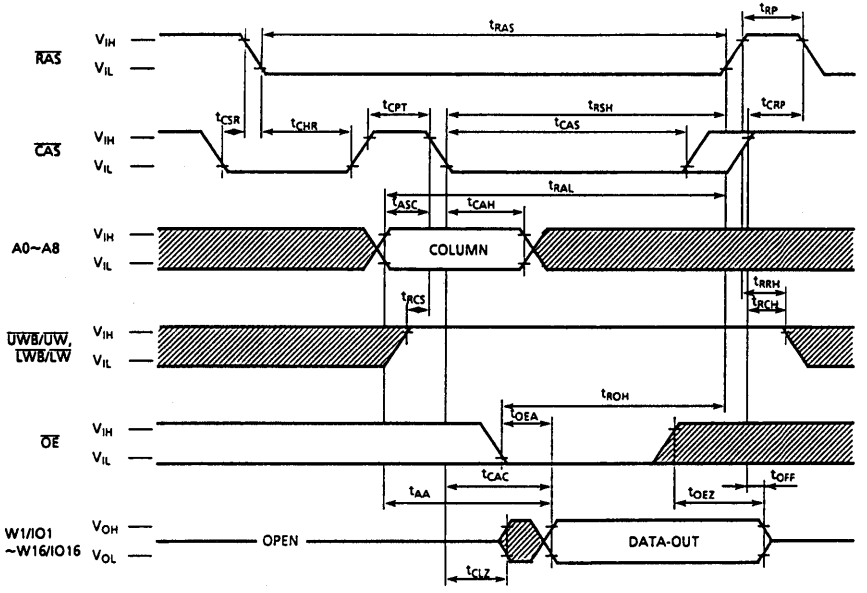
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



Note : D_{IN} (W9/IO9~W16/IO16) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

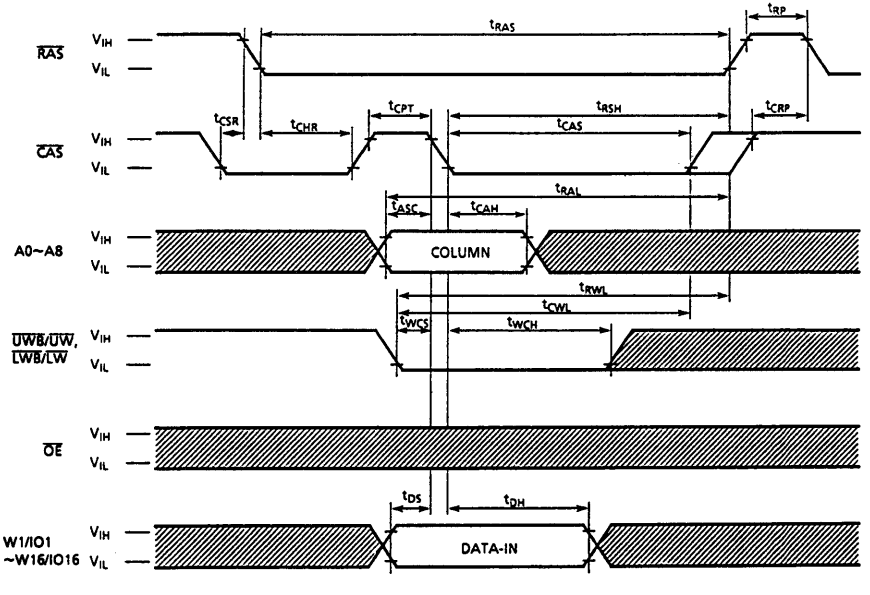
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

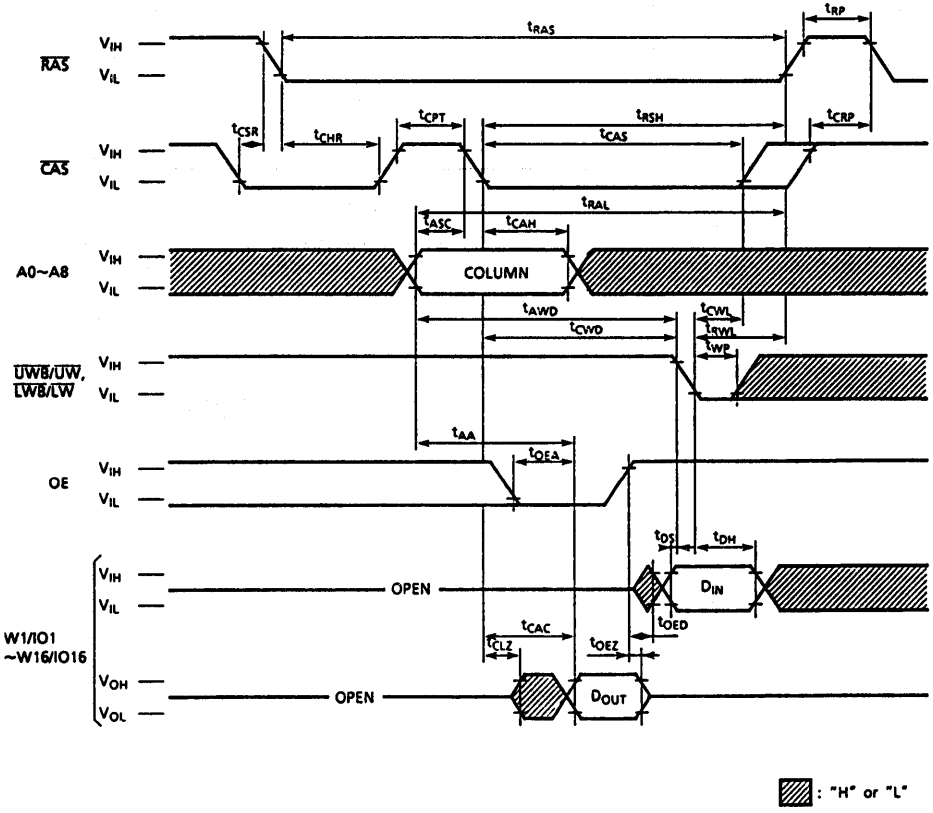
CAS BEFORE RAS REFRESH COUNTER TEST WRITE CYCLE



Note: D_{OUT} = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



1,048,576 WORD X 16 BIT DYNAMIC RAM

DESCRIPTION

The TC5118160AJ/AFT is the new generation dynamic RAM organized 1,048,576 word by 16 bit. The TC5118160AJ/AFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5118160AJ/AFT to be packaged in 42 pin plastic SOJ. The package provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  770mW MAX. Operating
  TC5118160AJ/AZ/AFT/ATR-70
  660mW MAX. Operating
  (TC5118160AJ/AZ/AFT/ATR-80)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package
  TC5118160AJ : SOJ42-P-400
  TC5118160AFT :TSOP50-P-400

KEY PARAMETERS

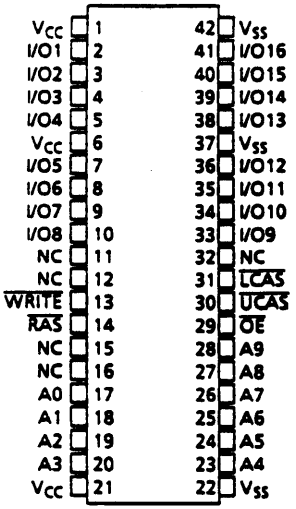
ITEM		TC5118160AJ/AFT	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

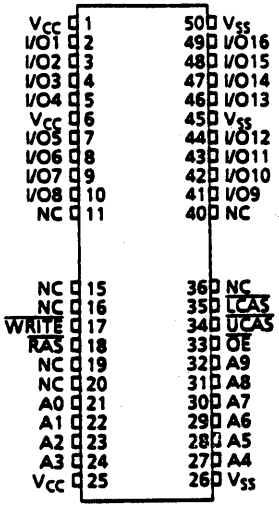
A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe /Upper Byte Control
$\overline{LCAS}$	Column Address Strobe /Lower Byte Control
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/01~I/016	Data Input/Output
V_{CC}	Power (+ 5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

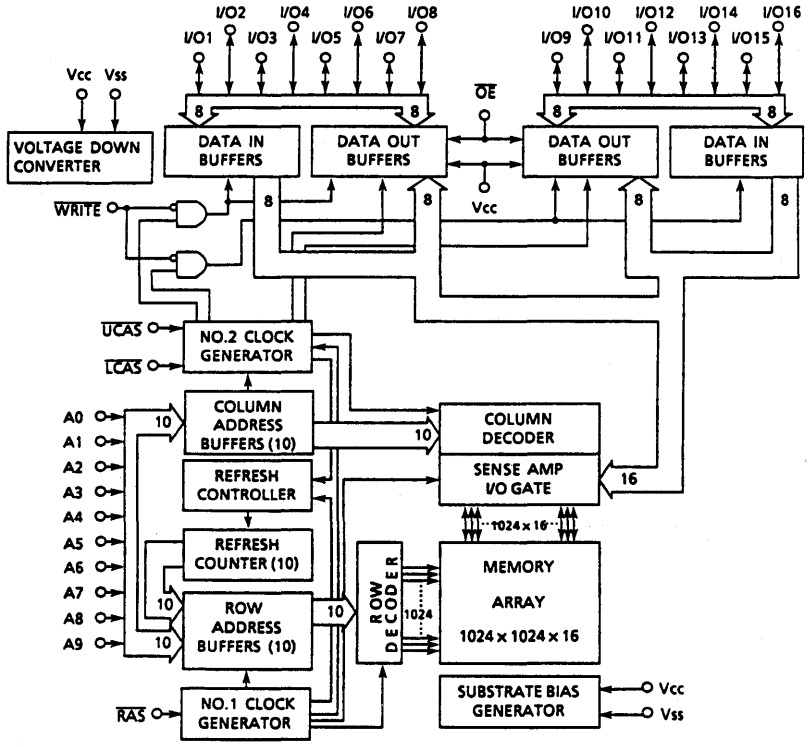
Plastic SOJ



Plastic TSOP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RANGES	UNIT	NOTE
Input Voltage	V_{IN}	— 0.5~Vcc + 0.5	V	1
Output Voltage	V_{OUT}	— 0.5~Vcc + 0.5	V	1
Power Supply Voltage	V_{CC}	— 0.5~7	V	1
Operating Temperature	T_{OPR}	0~70	^{0}C	1
Storage Temperature	T_{STG}	—55~150	^{0}C	1
Soldering Temperature •Time	T_{SOLDER}	260 • 10	^{0}C • sec	1
Power Dissipation	P_D	900	mW	1
Short Circuit Ouput Current	I_{OUT}	50	mA	1

*This parameter is periodically sampled and is not 100% tested,

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	V_{CC}+0.5*	V	2
V_{IL}	Input Low Voltage	—0.5**	—	0.8	V	2

*V_{CC} + 2.0V at pulse width ≤ 20ns. (pulse width is measured at V_{CC}).
**-2.0V at pulse width ≤ 20ns. (pulse width is measured at OV)

D.C. OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC5118160AJ/AFT-70	-	140	mA	3,4 5
		TC5118160AJ/AFT-80	-	120		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC5118160AJ/AFT-70	-	140	mA	3, 5
		TC5118160AJ/AFT-80	-	120		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling:t_{PC}=t_{PC} MIN.)	TC5118160AJ/AFT-70	-	75	mA	3,4 5
		TC5118160AJ/AFT-80	-	65		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC5118160AJ/AFT-70	-	140	mA	3, 5
		TC5118160AJ/AFT-80	-	120		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	μA	
V_{OH}	OUTPUT CURRENT Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT CURRENT Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC5118160AJ/AFT				UNIT	NOTE
		—70		—80			
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	—	150	—	ns	
t_{RMW}	Read-Modify-Write Cycle Time	180	—	200	—	ns	
t_{PC}	Fast Page Mode Cycle Time	45	—	50	—	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90	—	100	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	70	—	80	ns	9, 14, 15
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	ns	9, 14
t_{AA}	Acess Time from Column Address	—	35	—	40	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	9
t_{CLZ}	$\overline{CAS}$ to ouput in Low-Z	0	—	0	—	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	60	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	—	45	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	80	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	40	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time	0	—	0	—	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	—	0	—	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC5118160AJ/AFT				UNIT	NOTE
		—70		—80			
		MIN.	MAX.	MIN.	MAX.		
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	ns	
t_{DS}	Data Set-Up Time	0	—	0	—	ns	12
t_{DHS}	Data Hold Time	15	—	15	—	ns	12
t_{REF}	Refresh Period	—	16	—	16	ms	
t_{WCS}	Write Command Set-Up Time	0	—	0	—	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	45	—	45	—	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	95	—	105	—	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	—	65	—	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	65	—	70	—	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	—	5	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	—	15	—	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	—	5	—	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	30	—	30	—	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	—	10	—	ns	
t_{OEA}	$\overline{OE}$ Access Time	—	20	—	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	15	—	15	—	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	15	0	15	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	15	—	ns	
t_{ODS}	Output Disable Set-Up Time	0	—	0	—	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, TA = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance(A0~A9)	—	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WRITE}$, $\overline{OE}$)	—	7	pF
C_O	Input/Output Capacitance (I/O1~I/O16)	—	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieveS the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

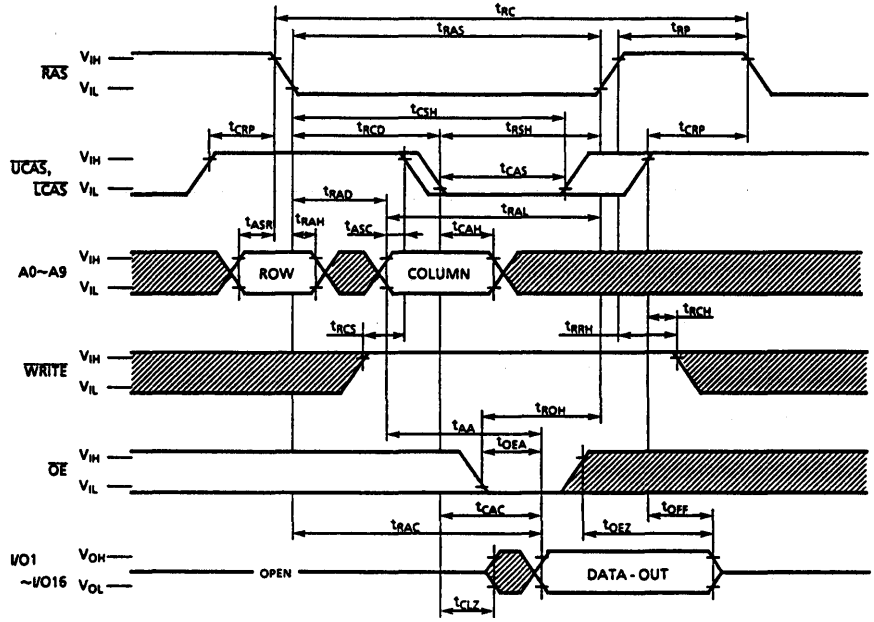
12. These parameters are referenced to $\overline{UCAS}$ or $\overline{LAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWP} > t_{CPWDD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

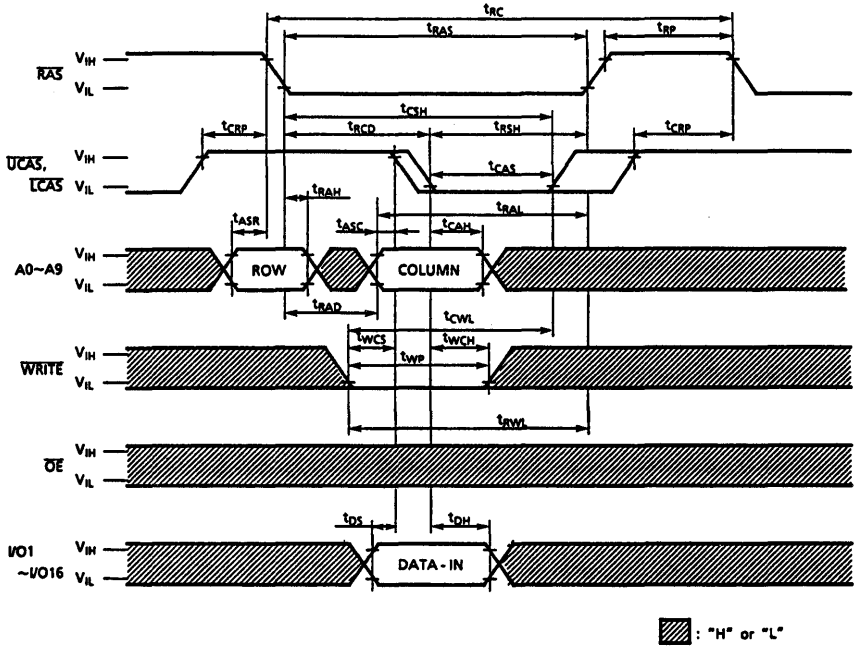
READ CYCLE



Note: D_{IN} = OPEN

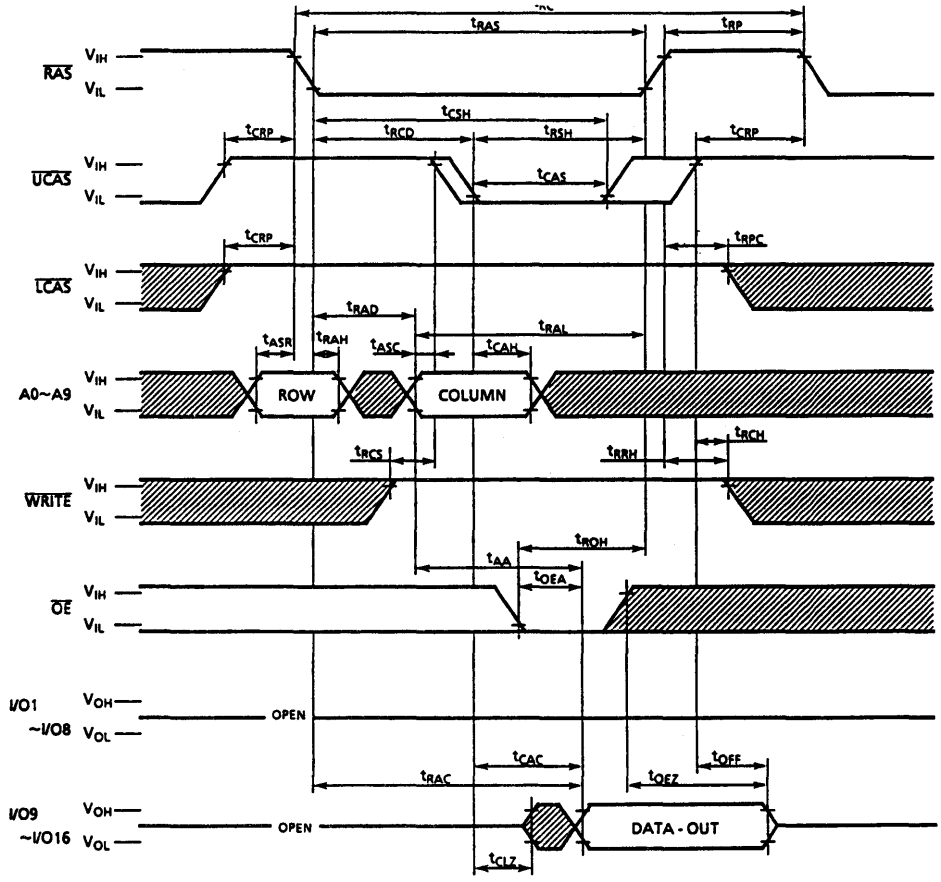
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE)



▨ : "H" or "L"

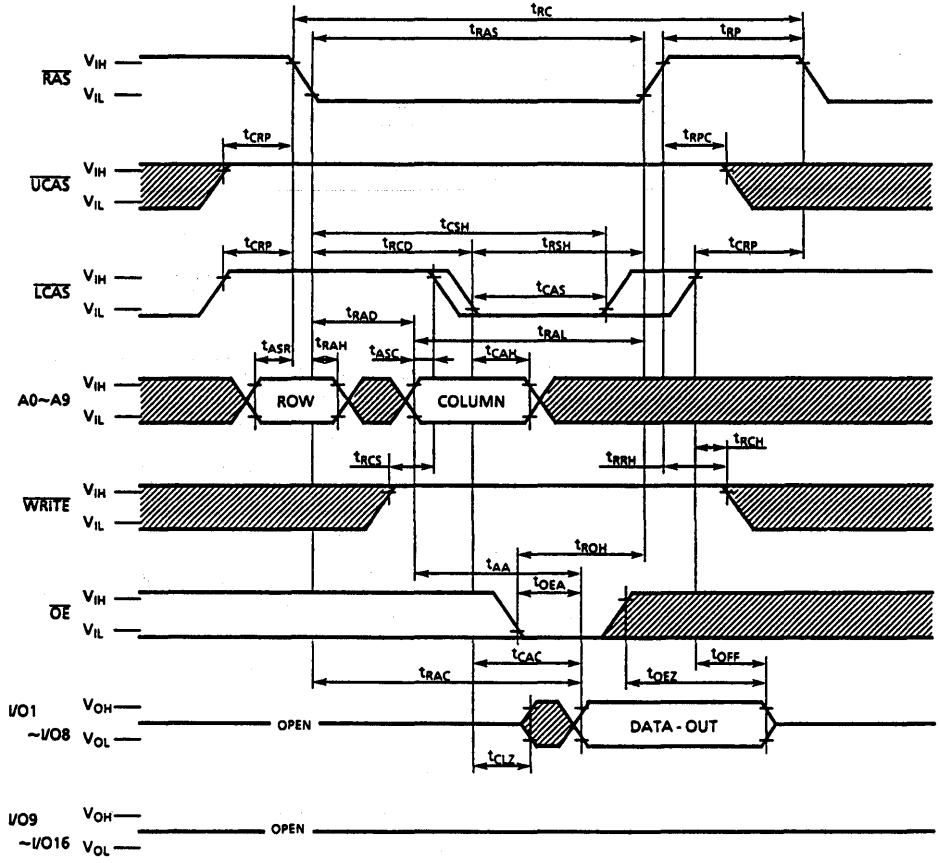
UPPER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{IN} (I/O9~I/O16) = OPEN

▨ : "H" or "L"

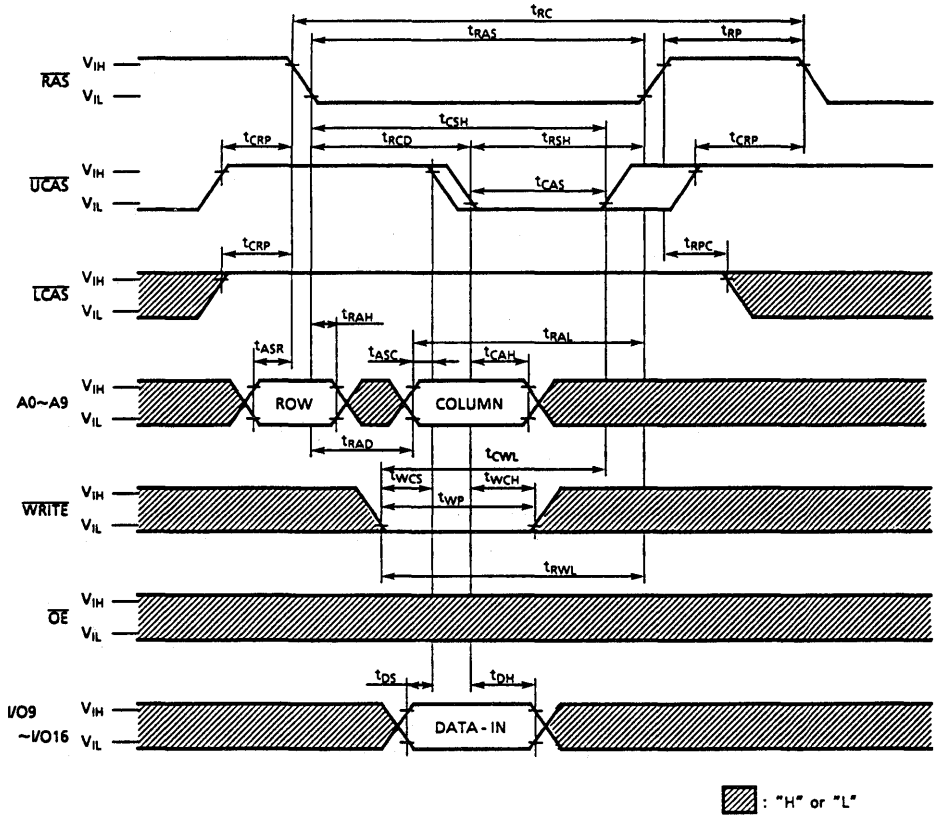
LOWER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O8) = OPEN
D_{IN} (I/O9~I/O16) = Don't Care

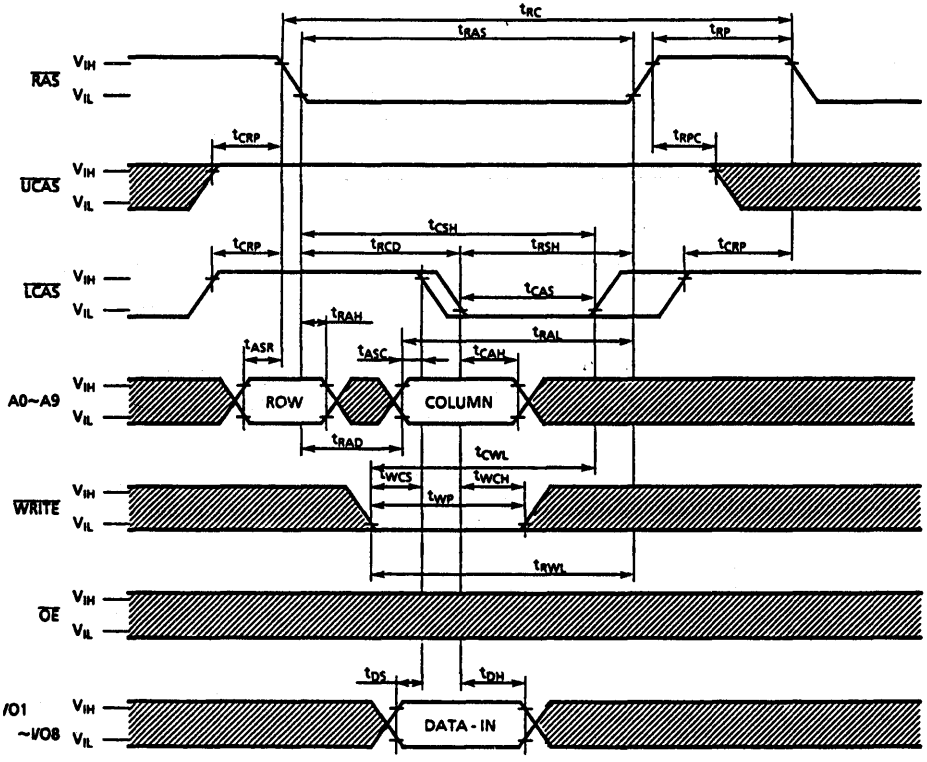
▨ : "H" or "L"

UPPER BYTE WRITE CYCLE (EARLY WRITE)



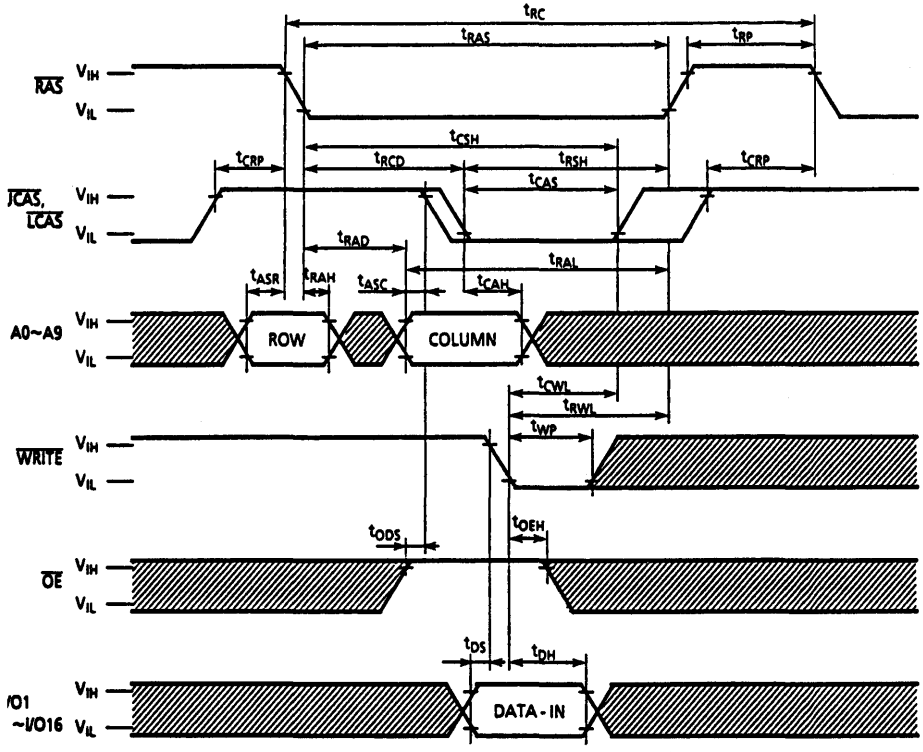
Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} = OPEN

LOWER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} = OPEN

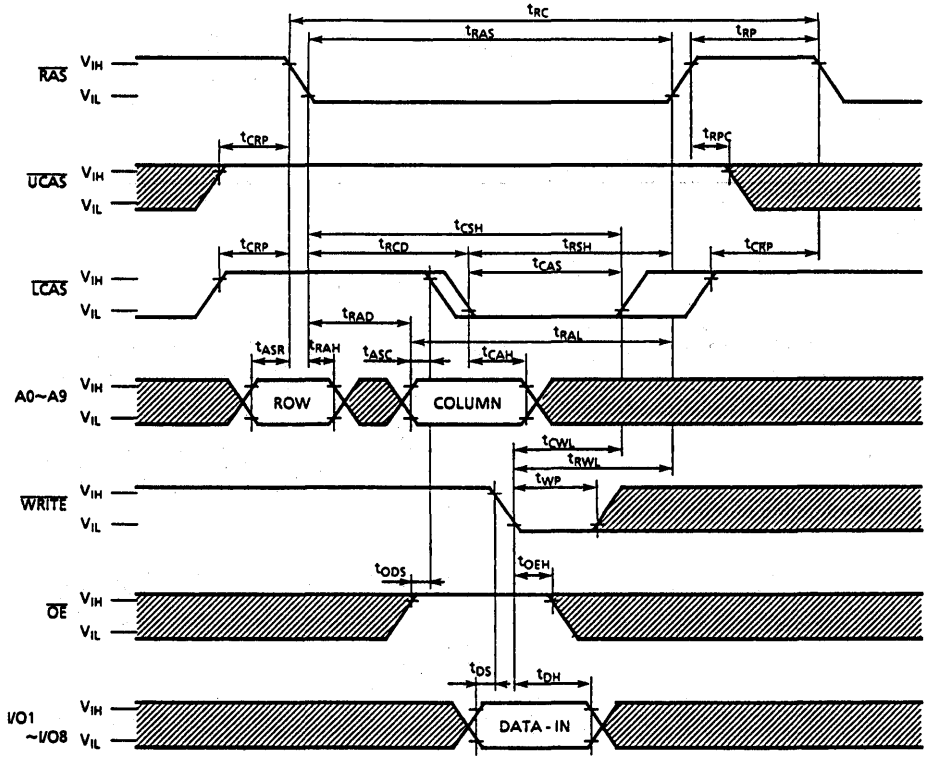
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

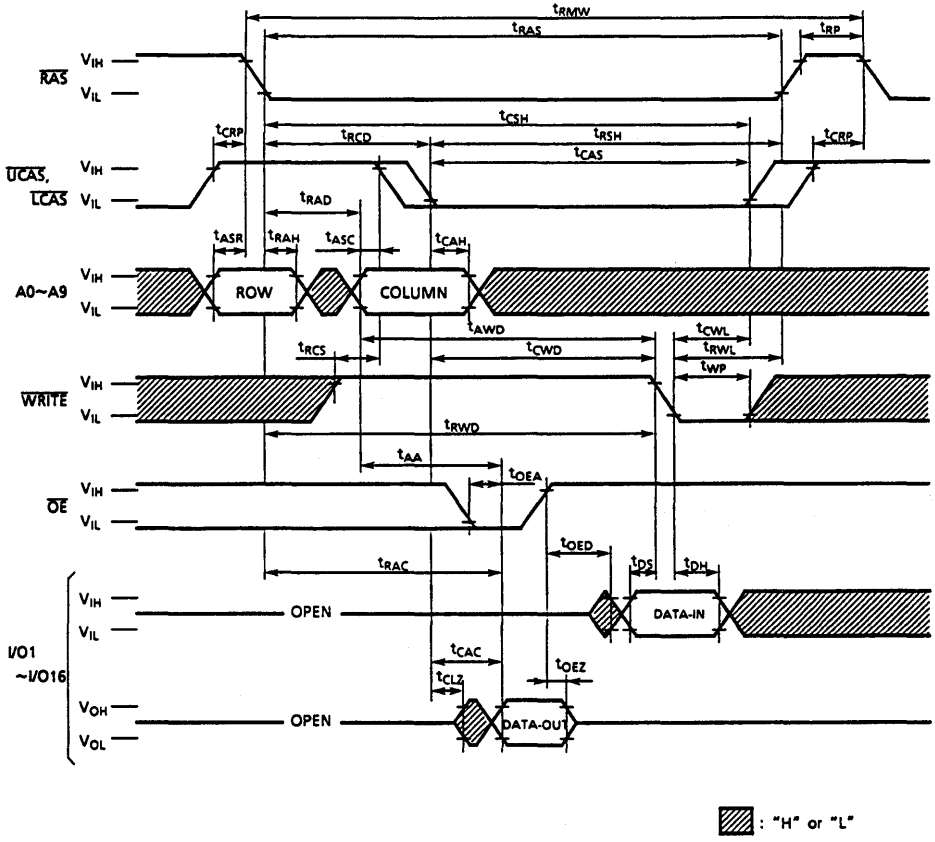
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



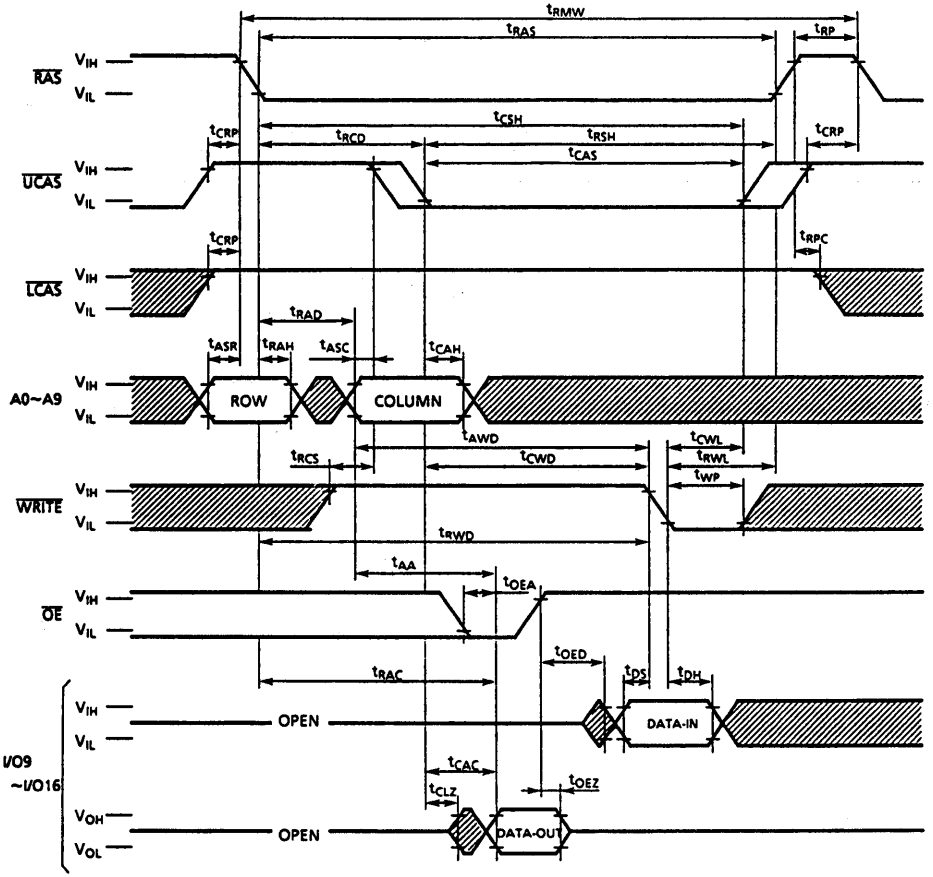
Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

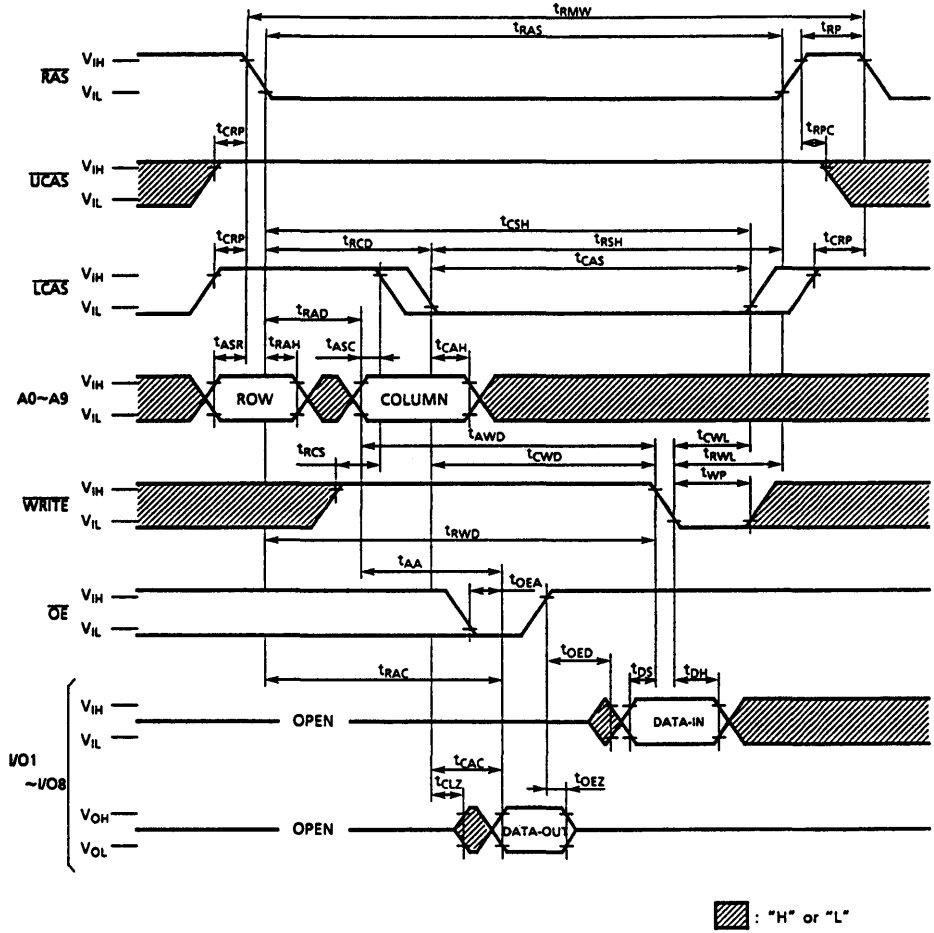


READ-MODIFY-WRITE CYCLE



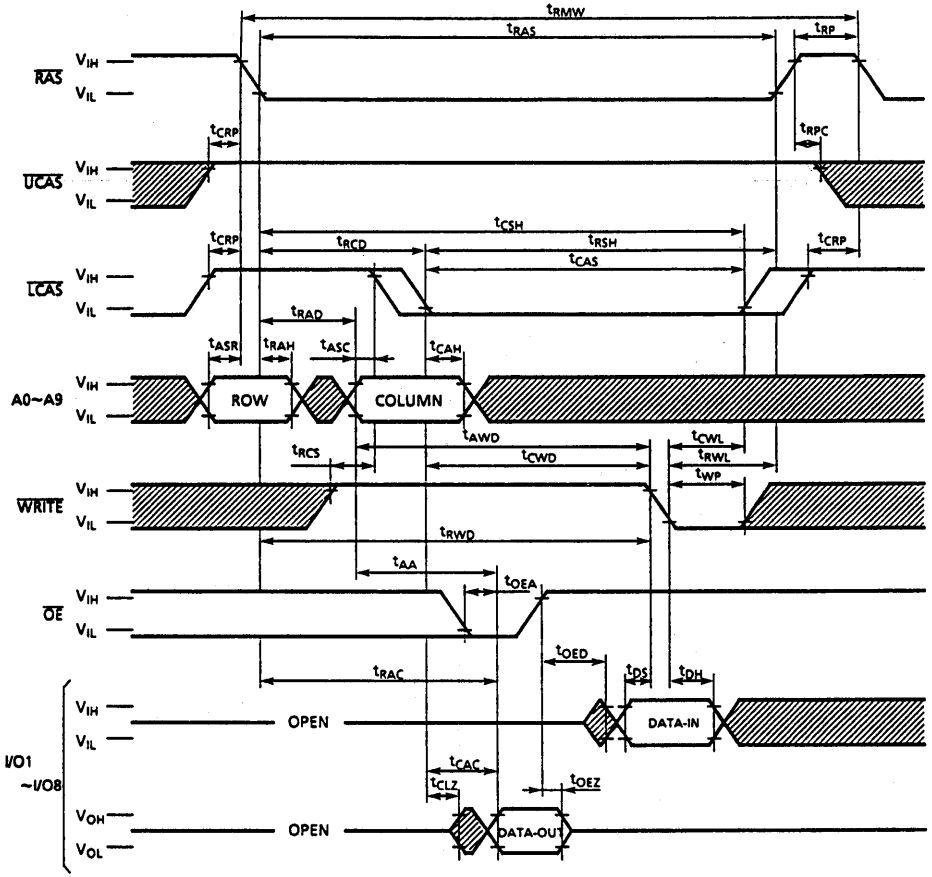
Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} (I/O1~I/O8) = OPEN

UPPER BYTE READ-MODIFY-WRITE CYCLE



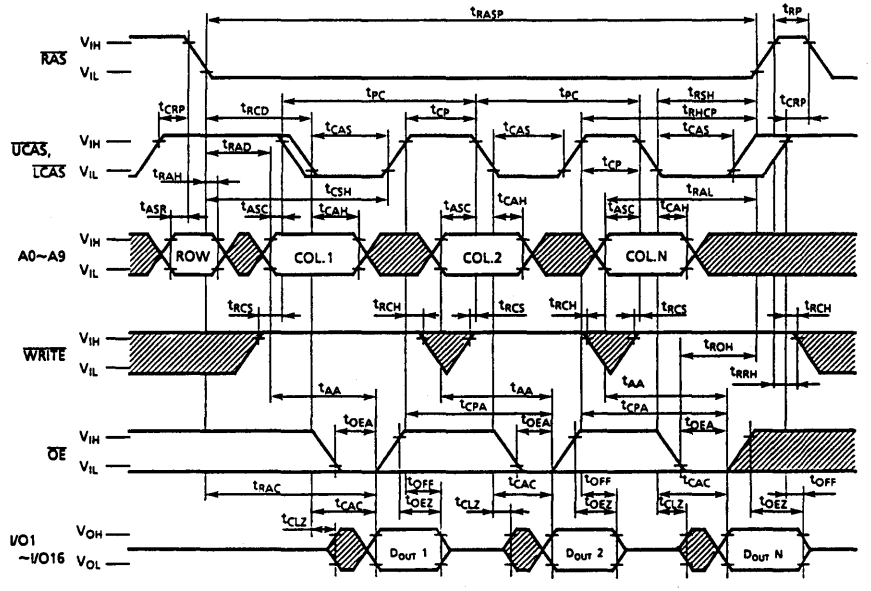
Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} (I/O9~I/O16) = OPEN

LOWER BYTE READ-MODIFY-WRITE CYCLE



Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} (I/O9~I/O16) = OPEN

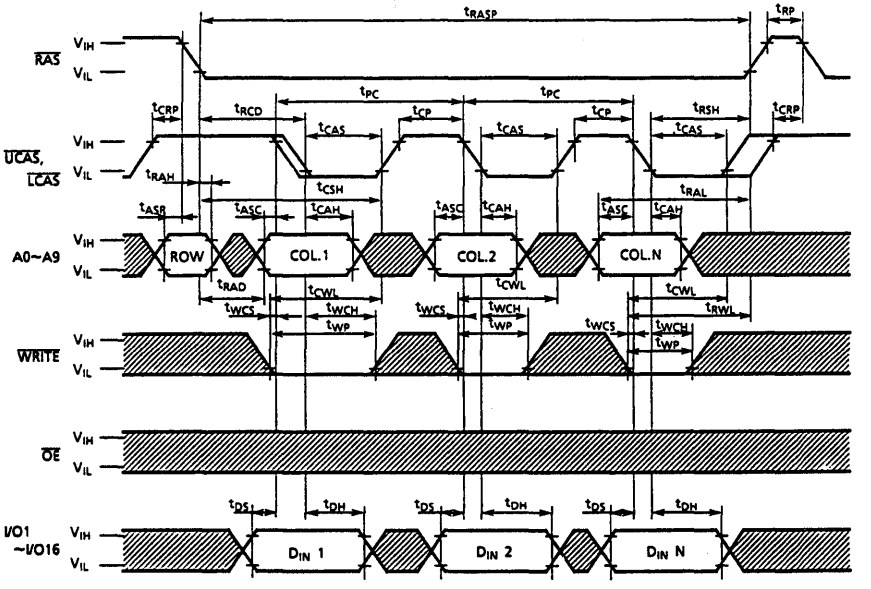
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨: "H" or "L"

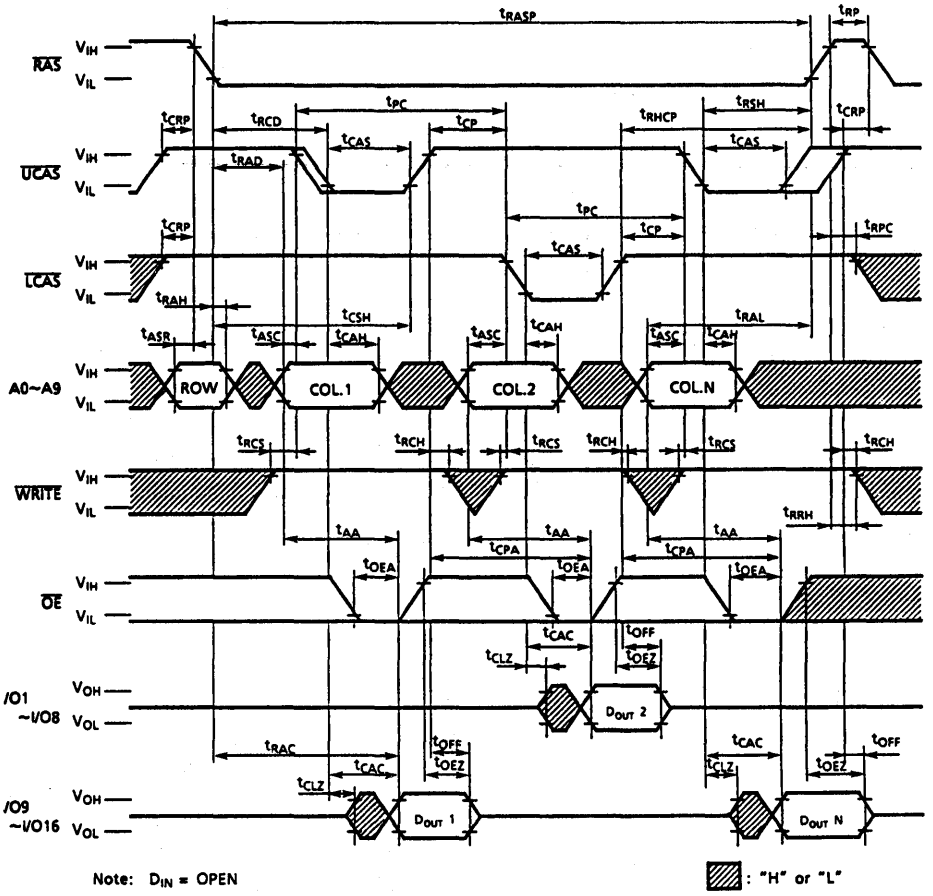
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



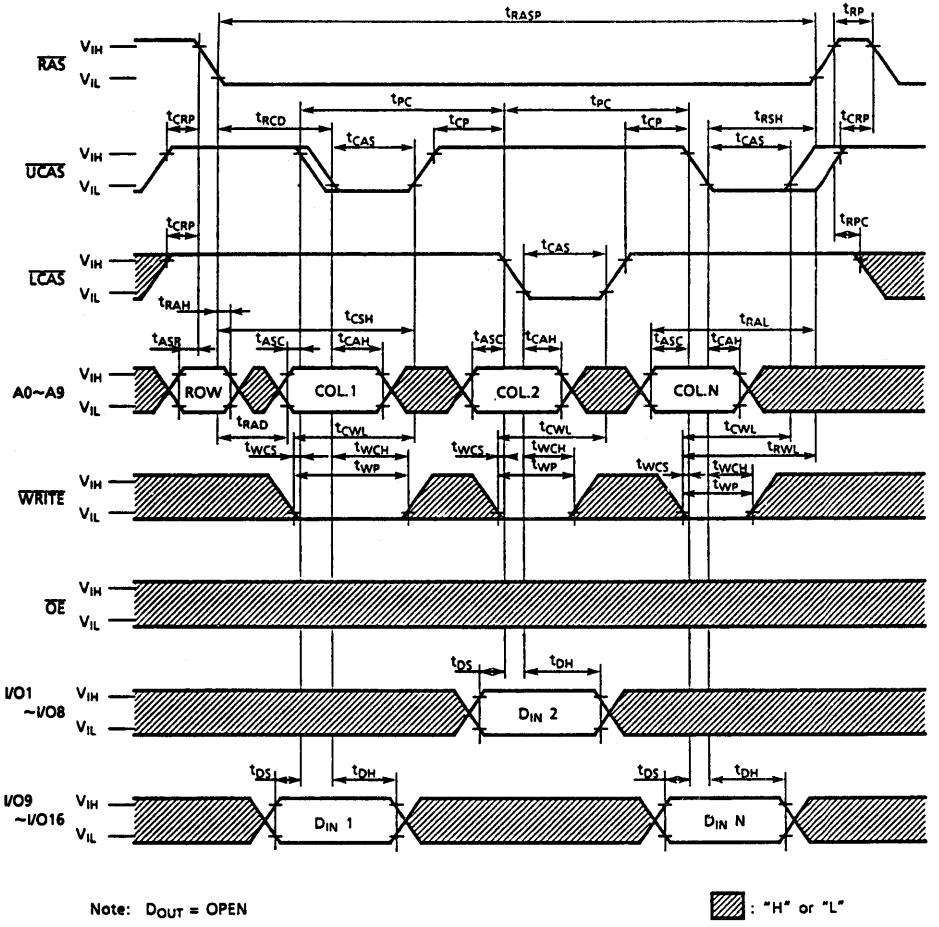
Note: D_{OUT} = OPEN

▨: "H" or "L"

FAST PAGE MODE BYTE READ CYCLE



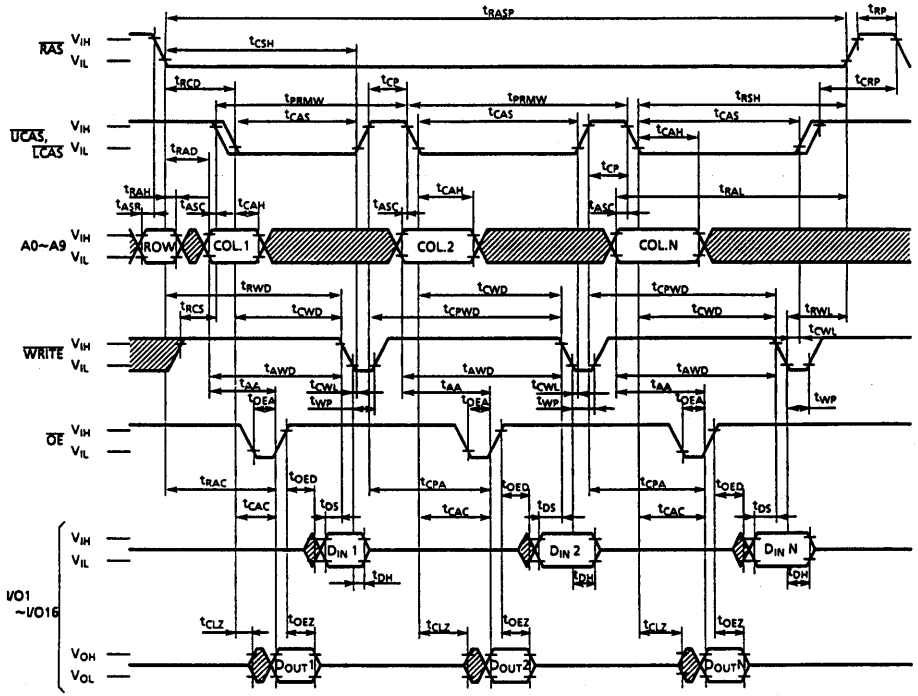
FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



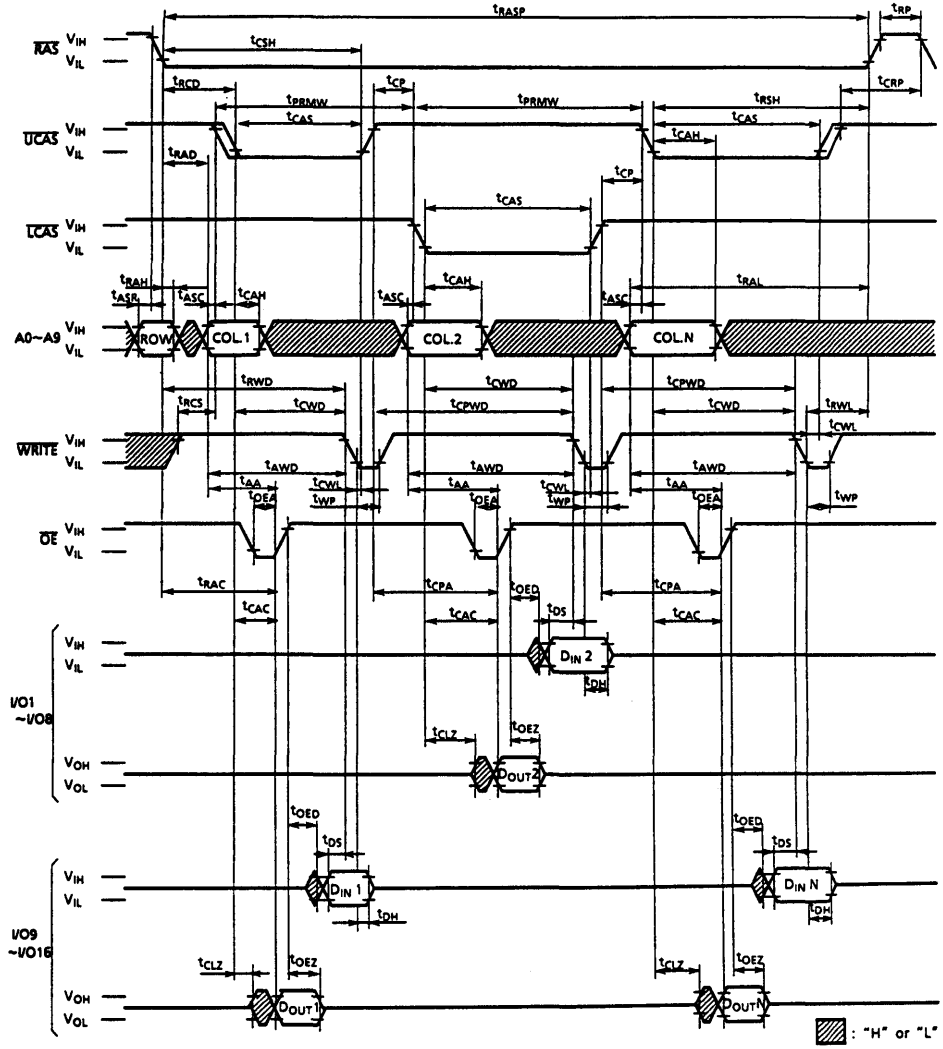
Note: D_{OUT} = OPEN

▨ : "H" or "L"

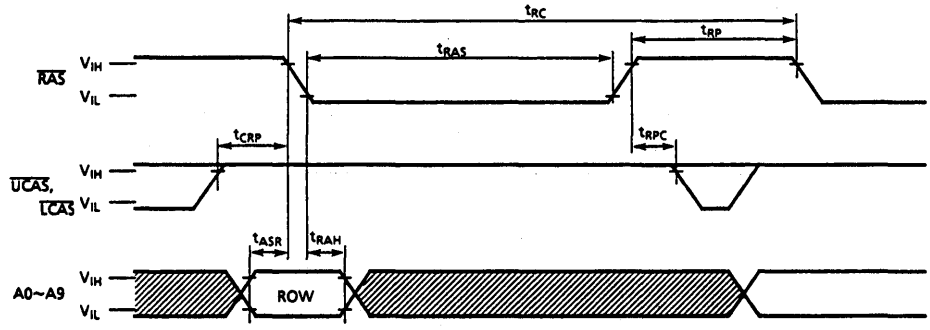
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE



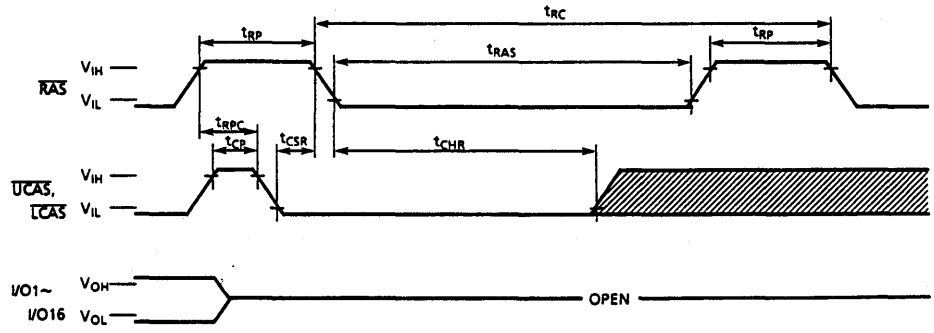
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"
D_{IN} = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

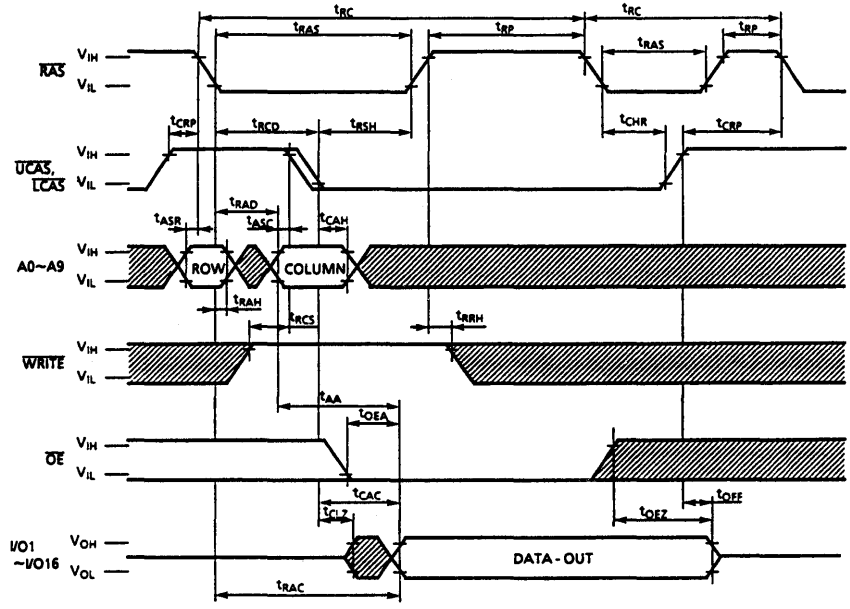
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



▨ : "H" or "L"

Note: $\overline{WRITE}$, $\overline{OE}$, A0~A9 = "H" or "L"
D_{IN} = Don't Care
$\overline{CAS}$ before $\overline{RAS}$ refresh is performed when either $\overline{UCAS}$ or $\overline{LCAS}$ meets this timing.

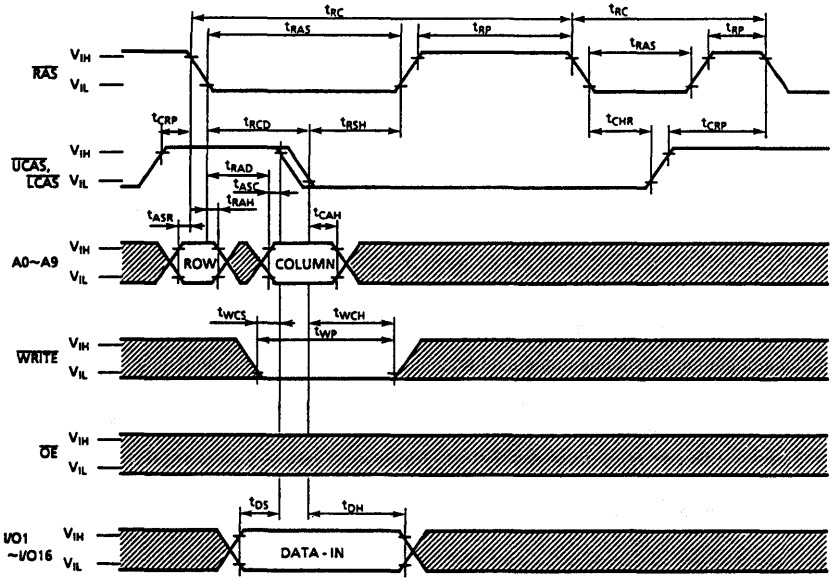
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨: "H" or "L"

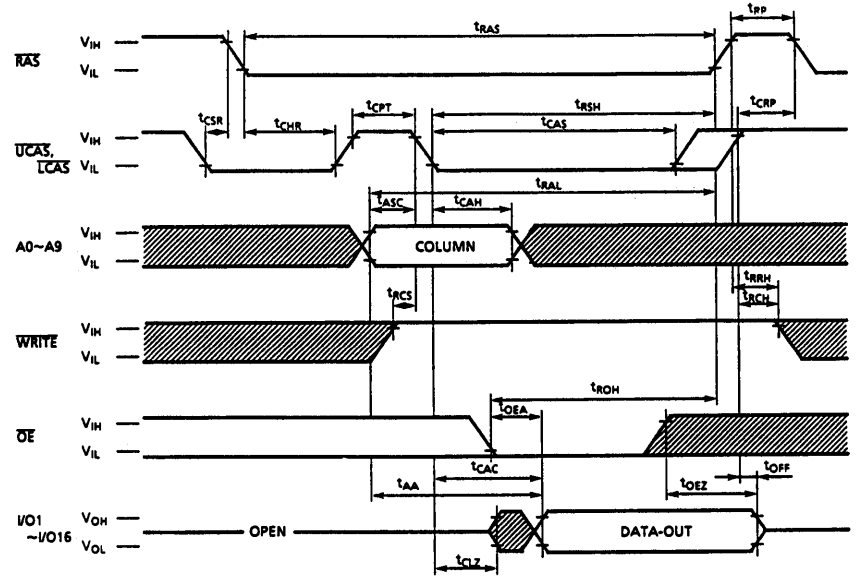
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨: "H" or "L"

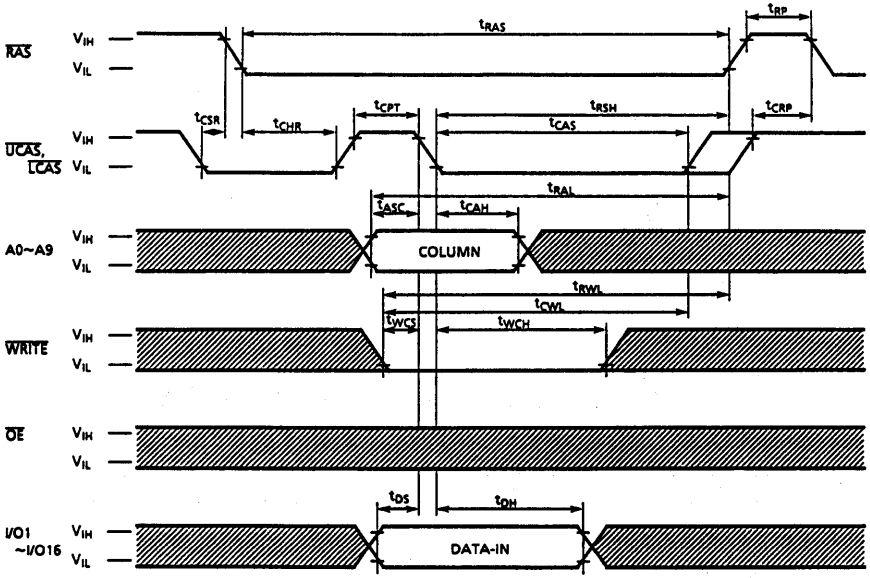
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



Note: D_{IN} = OPEN

▨: "H" or "L"

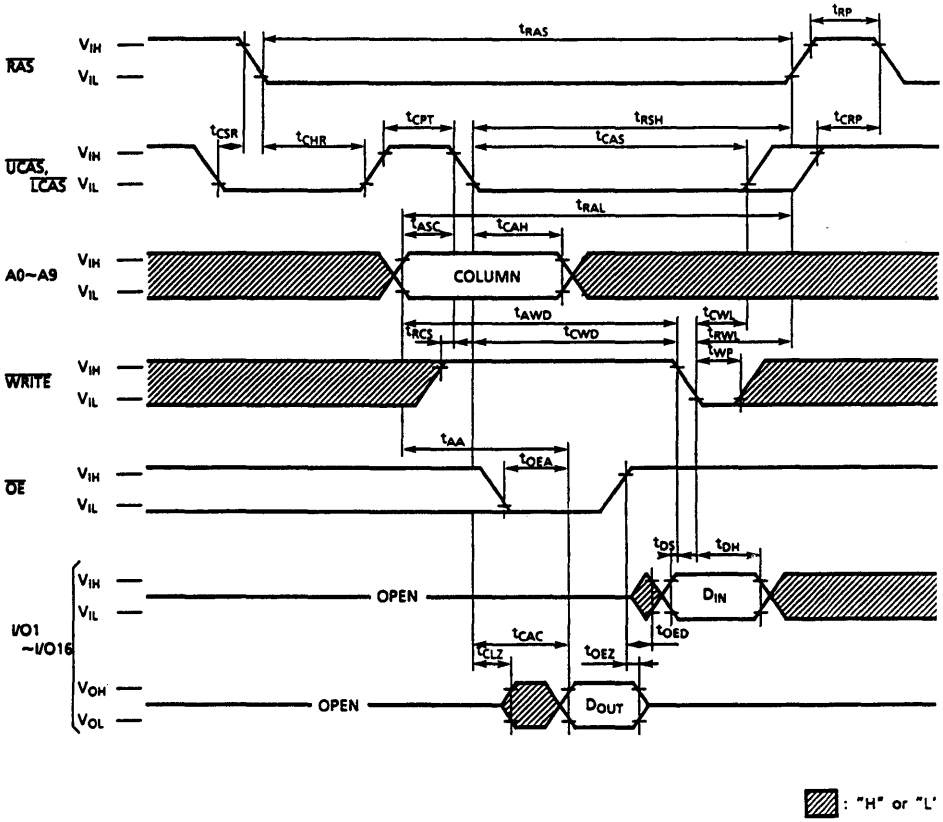
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



Note: D_{OUT} = OPEN

▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



1,048,576 WORD X 16 BIT DYNAMIC RAM

DESCRIPTION

The TC5116160AJ/AFT is the new generation dynamic RAM organized 1,048,576 word by 16 bit. The TC5116160AJ/AFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC5116160AJ/AFT to be packaged in a standard 42 pin plastic SOJ, and 50/44 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  523mW MAX. Operating
  (TC5116160AJ/AFT-60)
  440mW MAX. Operating
  (TC5116160AJ/AFT-70)
  385mW MAX. Operating
  (TC5116160AJ/AFT-80)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 4096 refresh cycles/16ms
- Package TC5116160AJ : SOJ42-P-400
  TC5116160AFT : TSOP20-P-400

KEY PARAMETERS

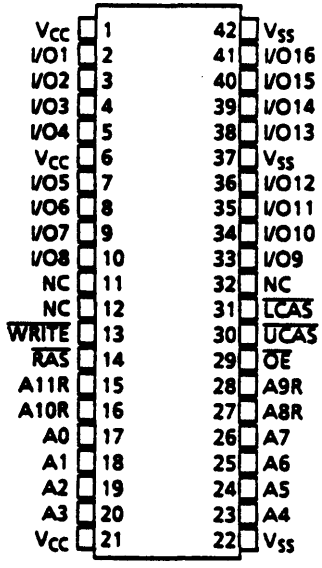
ITEM		TC5116160AJ/AFT		
		-60	-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns	20ns
t_{RC}	Cycle Time	110ns	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	50ns

PIN NAME

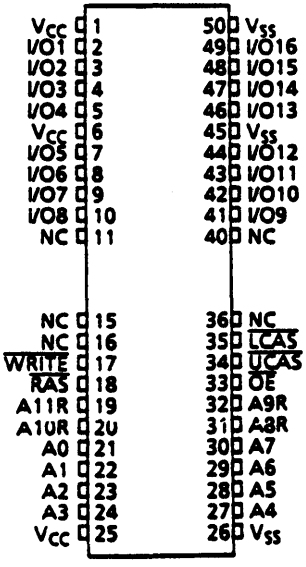
A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe /Upper Byte Control
$\overline{LCAS}$	Column Address Strobe /Lower Byte Control
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/01~I/016	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

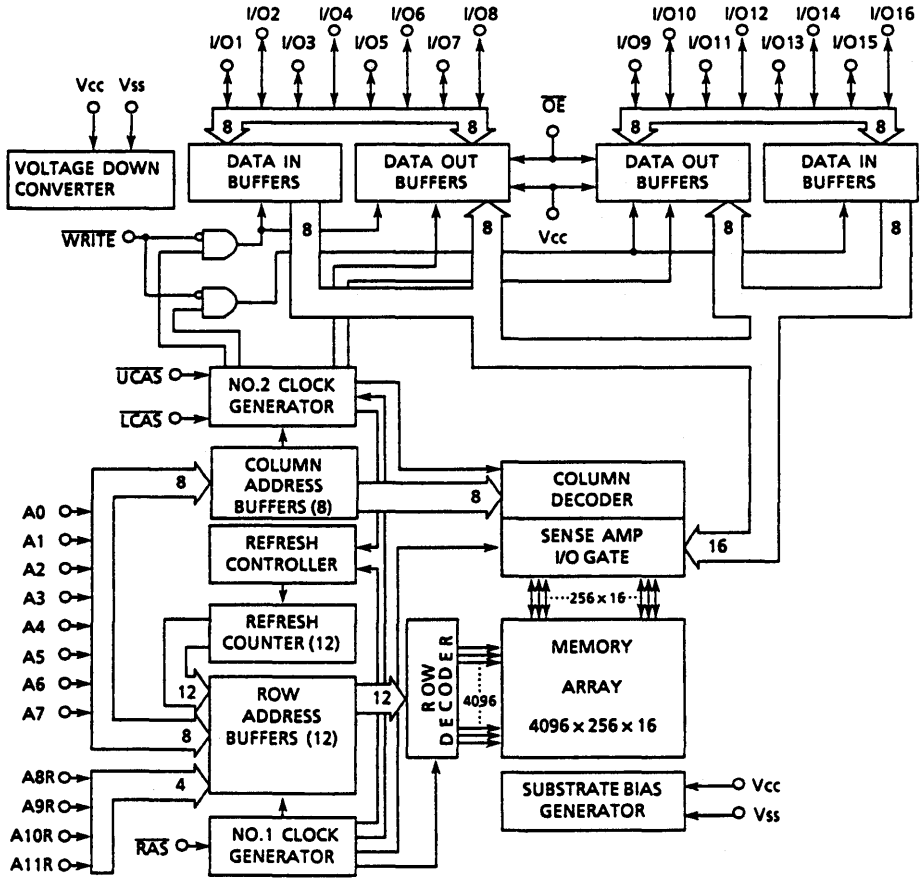
Plastic SOJ



Plastic TSOP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7$	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	$-55 \sim 150$	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	900	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	V_{CC}+0.5*	V	2
V_{IL}	Input LowVoltage	-0.5**	-	0.8	V	2

*V_{CC}+2.0V at pulse width ≤20ns (pulse width measured at V_{CC}).
**-2.0V at pulse width ≤20ns (pulse width measured at V_{CC}).

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN)	TC511610AJ/AZ/AFTAFTR-60	-	95	mA	3,4 5
		TC511610AJ/AZ/AFTAFTR-70	-	80		
		TC511610AJ/AZ/AFTAFTR-80	-	70		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511610AJ/AZ/AFTAFTR-60	-	95	mA	3, 5
		TC511610AJ/AZ/AFTAFTR-70	-	80		
		TC511610AJ/AZ/AFTAFTR-80	-	70		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC511610AJ/AZ/AFTAFTR-60	-	75	mA	3,4 5
		TC511610AJ/AZ/AFTAFTR-70	-	65		
		TC511610AJ/AZ/AFTAFTR-80	-	55		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC511610AJ/AZ/AFTAFTR-60	-	95	mA	3, 5
		TC511610AJ/AZ/AFTAFTR-70	-	80		
		TC511610AJ/AZ/AFTAFTR-80	-	70		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≤V_{IN}≤0.5V, All Other Pins Not Under Test=OV)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (OV≤V_{OUT}≤5.5V),		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC511610AJ/AZ/AFTAFTR						UNIT	NOTE
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	135	-	155	-	175	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	70	-	70	-	75	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Uup Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	0	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC511610AJ/AZ/AFTAFTR						UNIT	NOTE
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	12
t_{DH}	Data Hold Time	10	-	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	64	-	64	-	64	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	40	-	45	-	45	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	-	95	-	105	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	55	-	60		65	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	60	-	65	-	70	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	20	-	30	-	30	-	ns	
t_{ROH}	RAS Hold Time referenced to $\overline{OE}$	10	-	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	15	-	20	-	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	15	-	15	-	15	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	15	0	15	0	15	ns	10
t_{OEH}	Output Hold Time	15	-	15	-	15		ns	
t_{ODS}	Output Disable Set-up Time	0	-	0	-	0		ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A11)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	
C_O	Input Capacitance (I/O1~I/O16)	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

12. These parameters are referenced to $\overline{UCAS}$ or $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

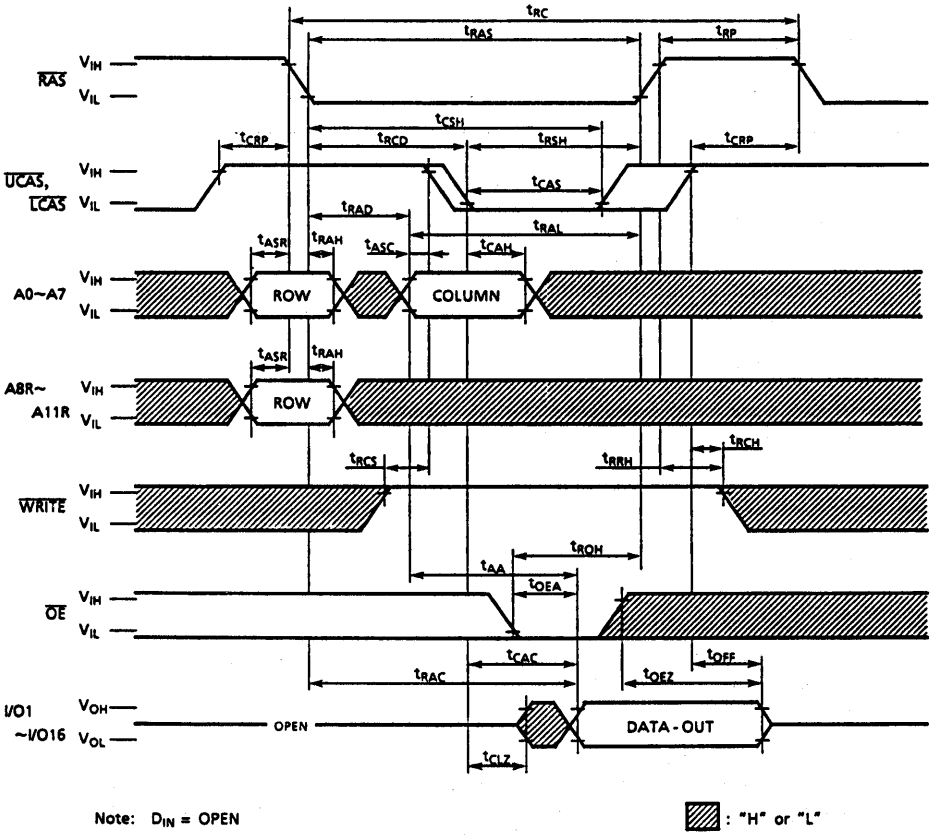
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

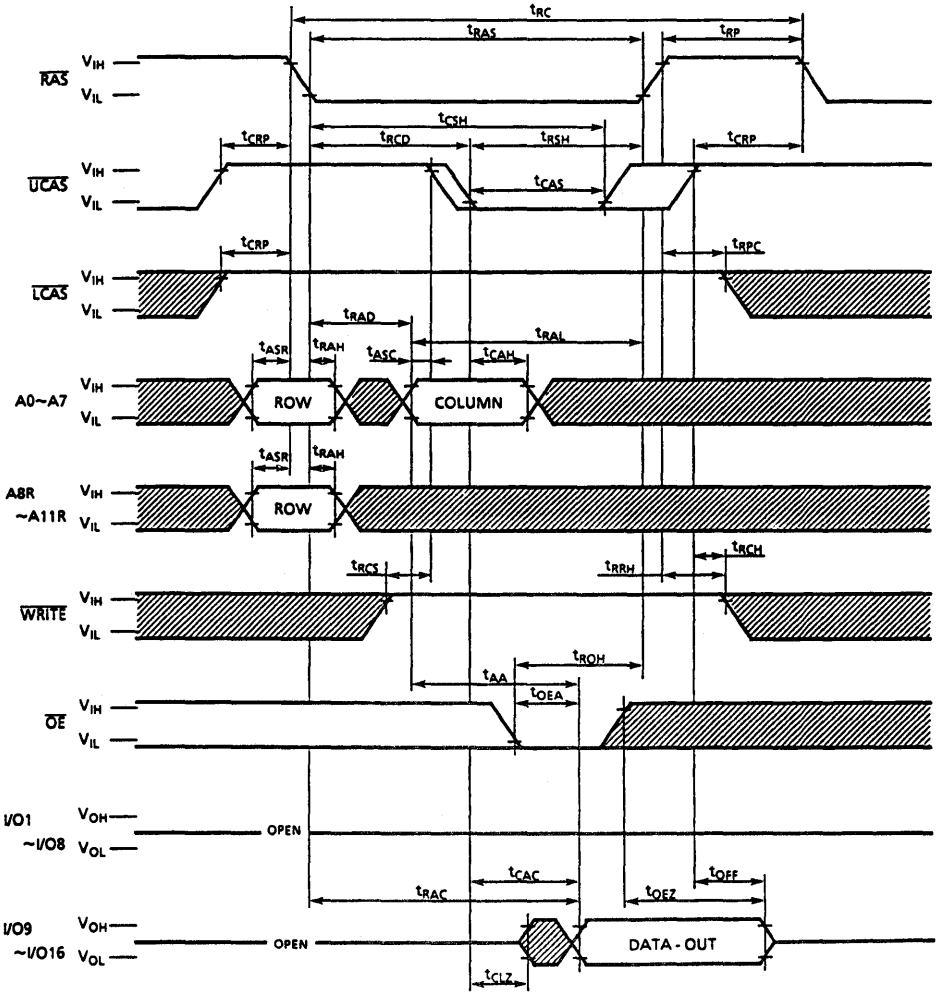
READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

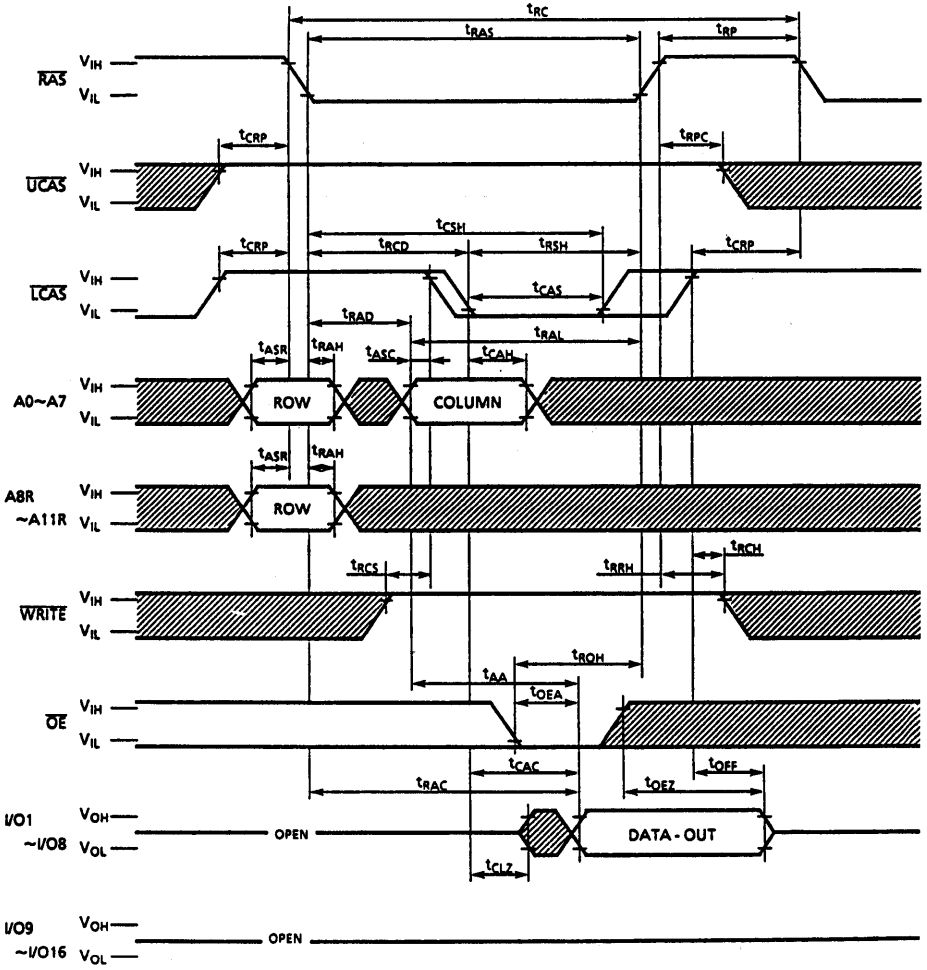
UPPER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{IN} (I/O9~I/O16) = OPEN

▨ : "H" or "L"

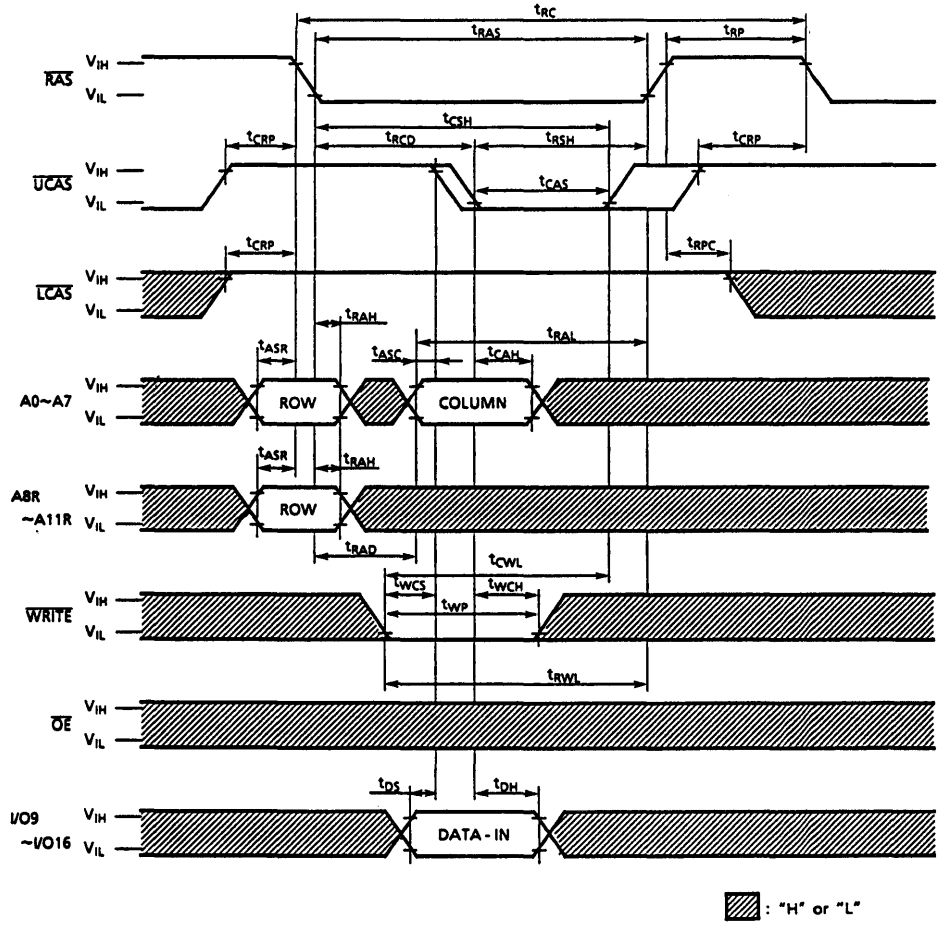
LOWER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O8) = OPEN
D_{IN} (I/O9~I/O16) = Don't Care

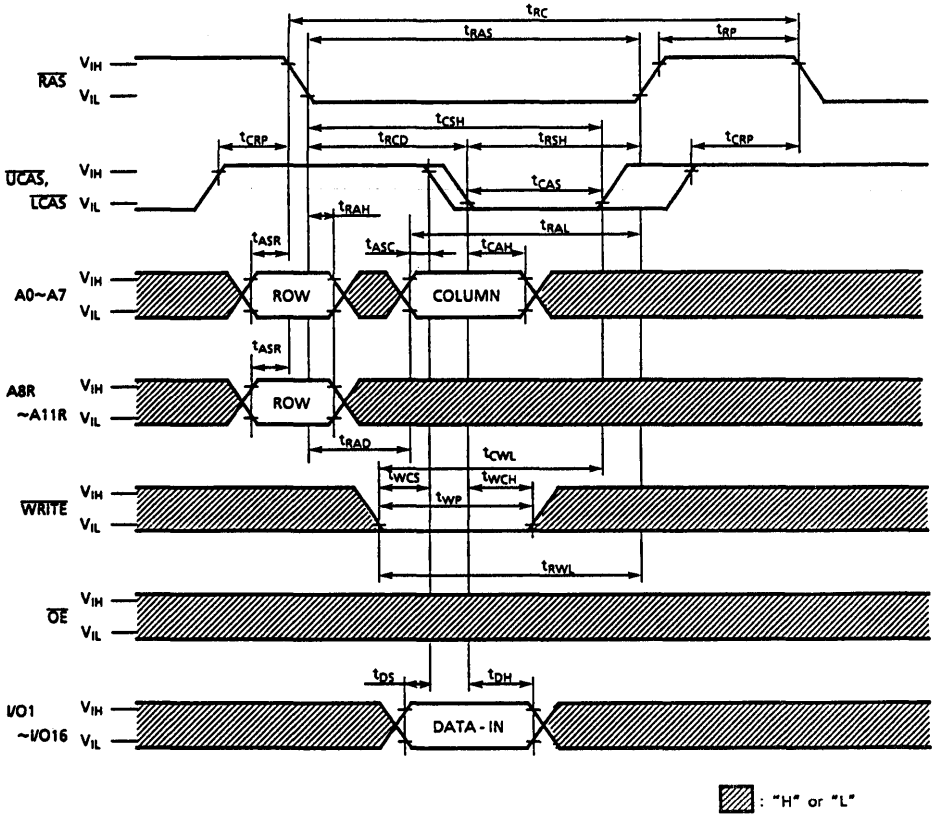
▨ : "H" or "L"

UPPER BYTE WRITE CYCLE (EARLY WRITE)



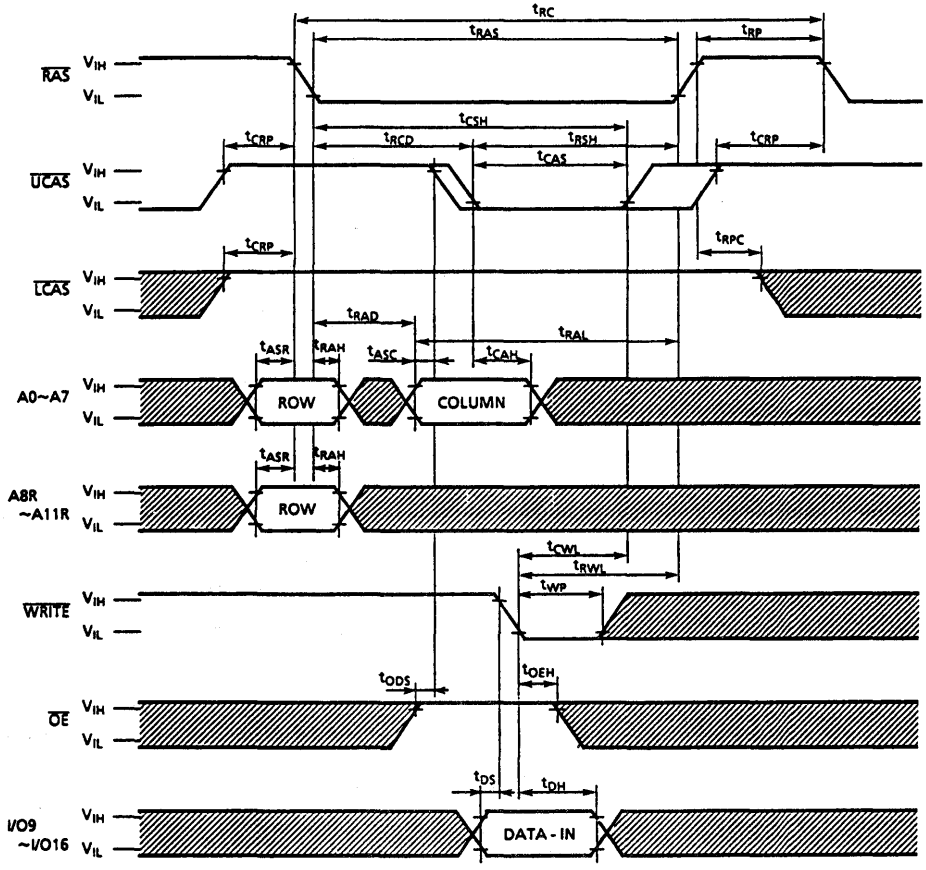
Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} = OPEN

LOWER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

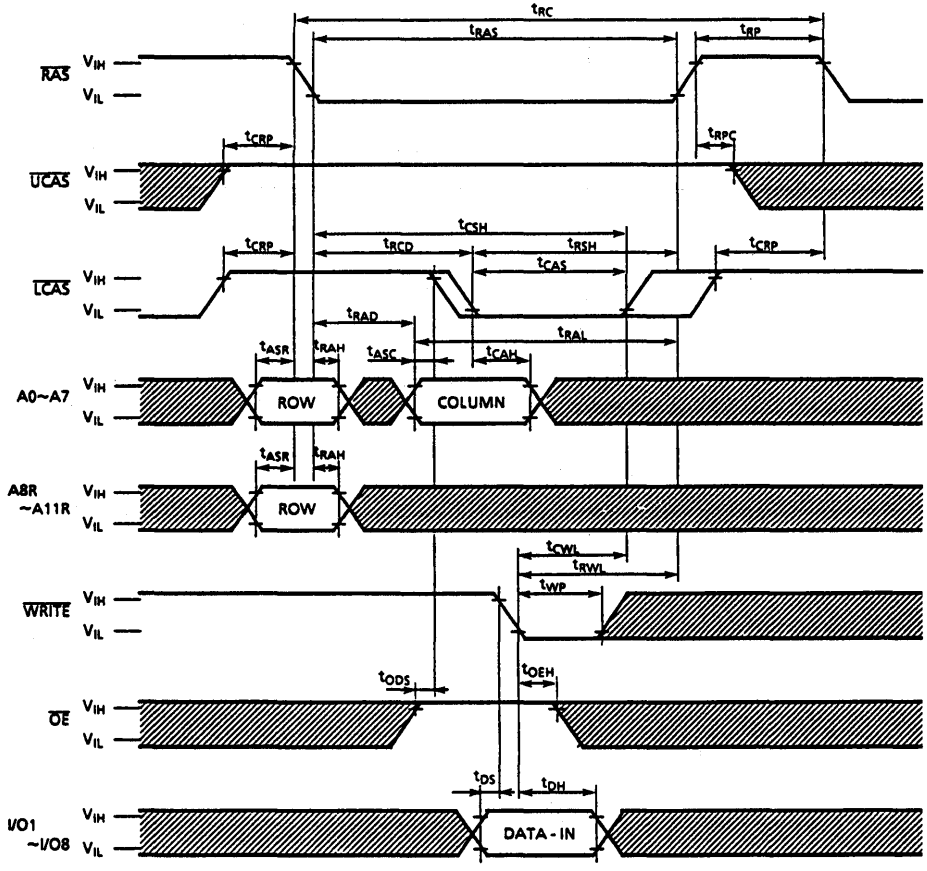
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

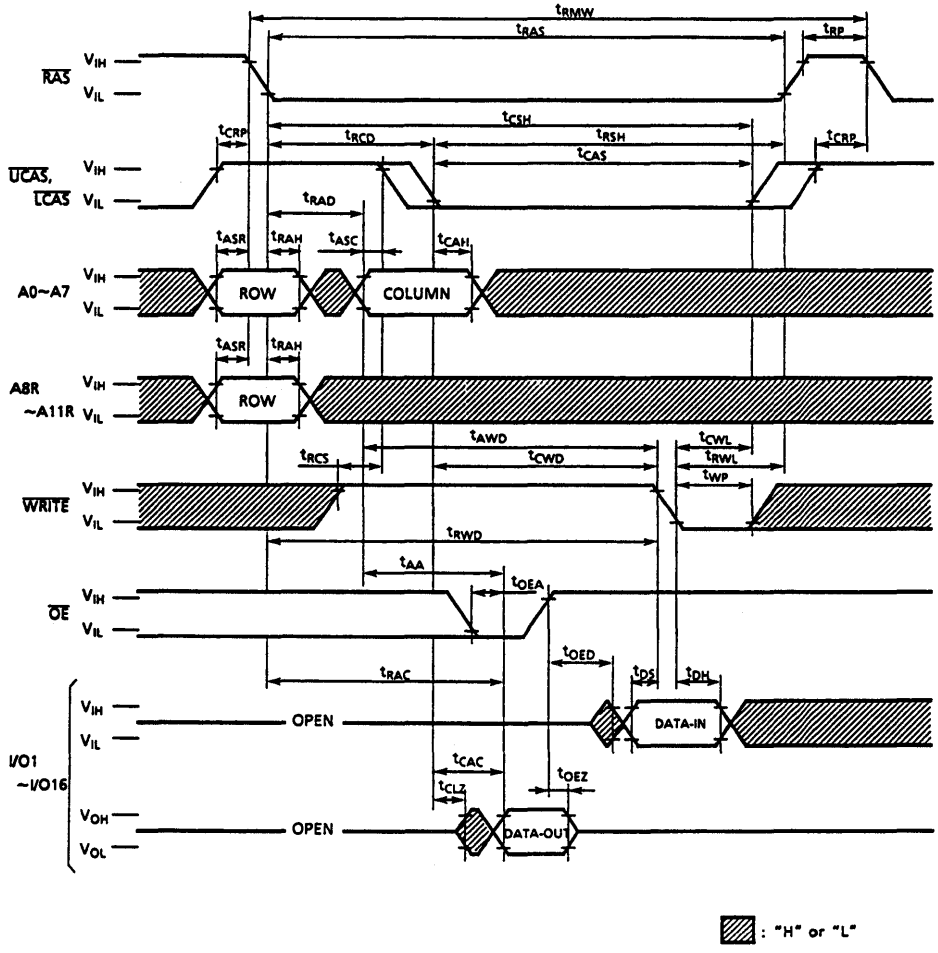
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



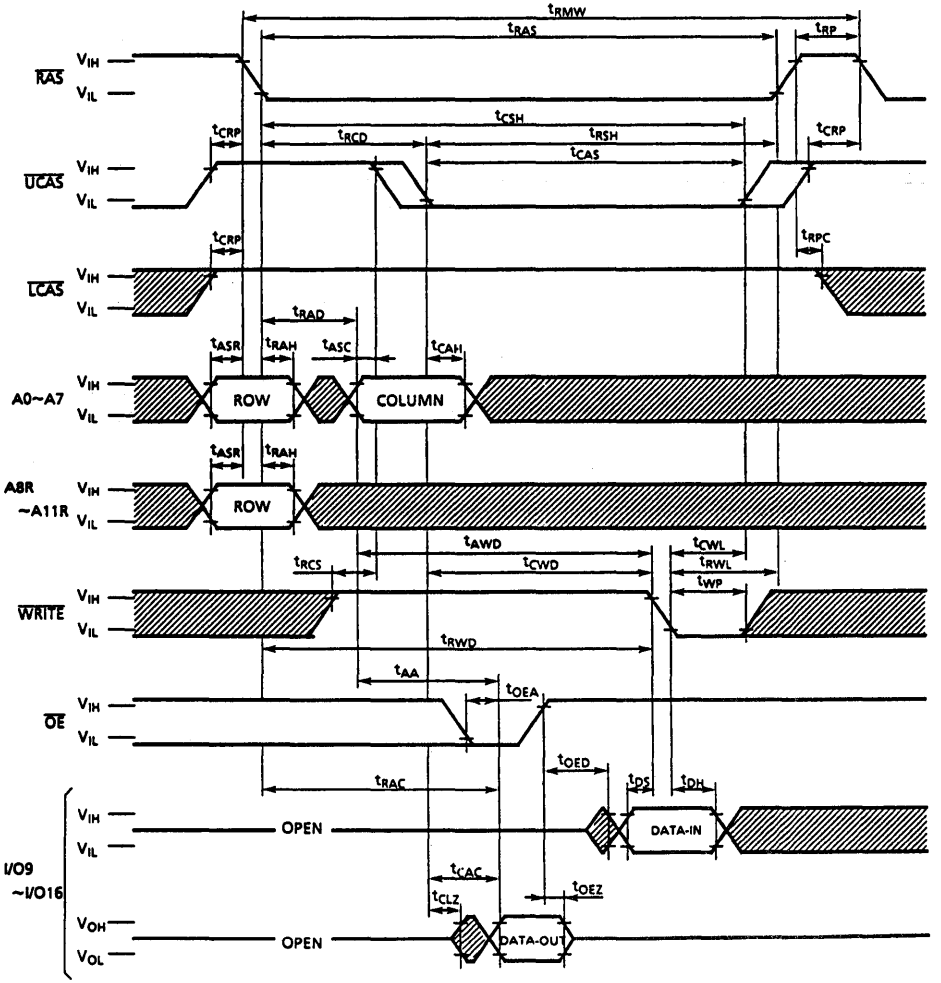
Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE

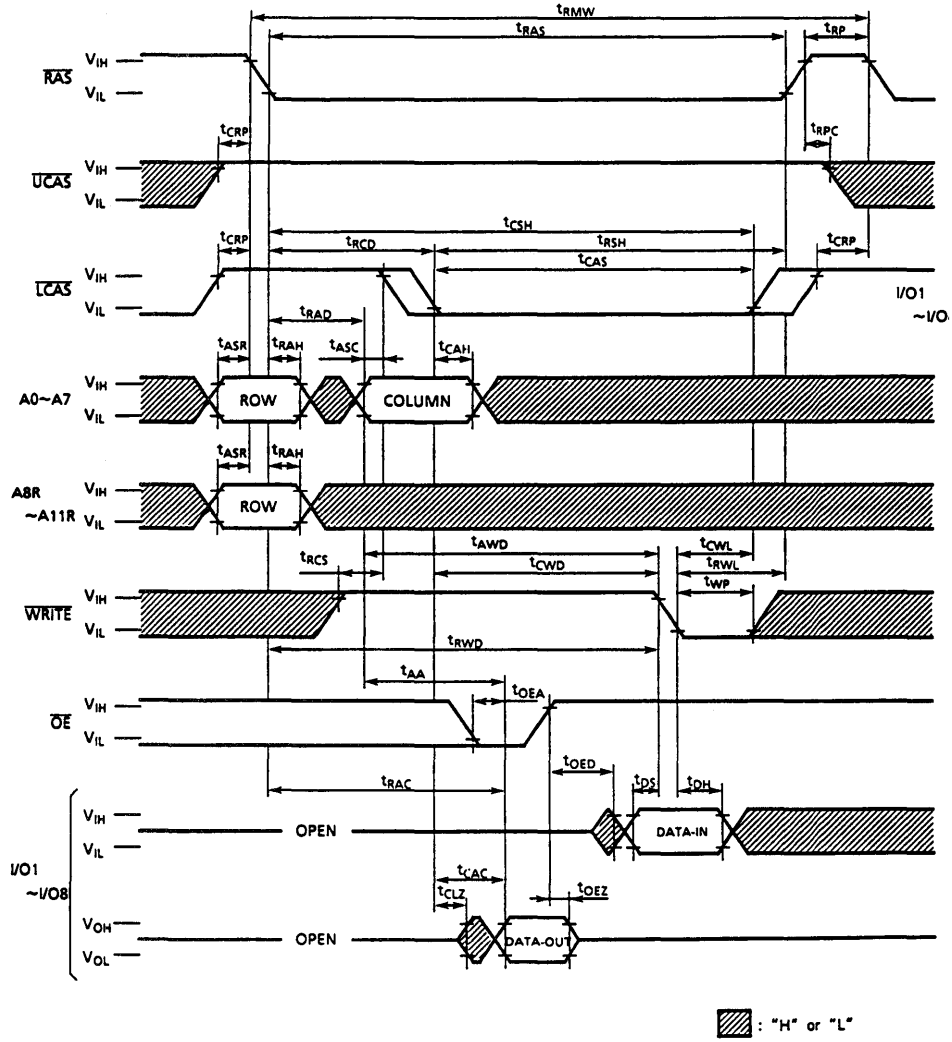


UPPER BYTE READ-MODIFY-WRITE CYCLE



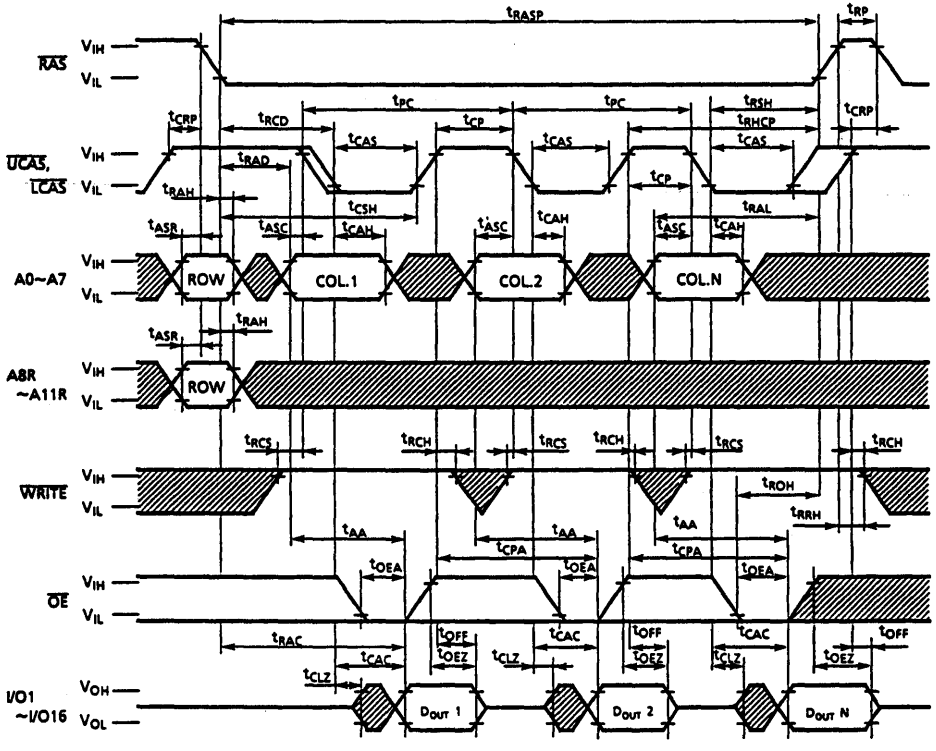
Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} (I/O1~I/O8) = OPEN

LOWER BYTE READ-MODIFY-WRITE CYCLE



Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} (I/O9~I/O16) = OPEN

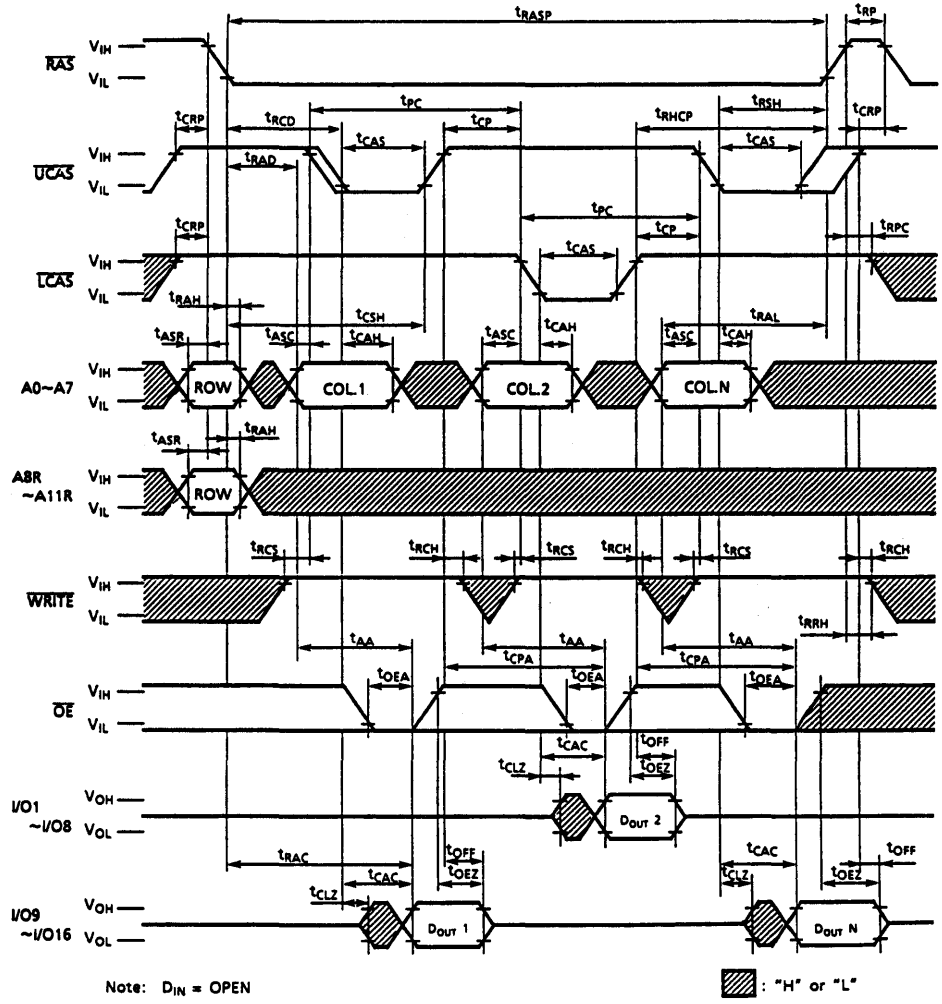
FAST PAGE MODE READ CYCLE



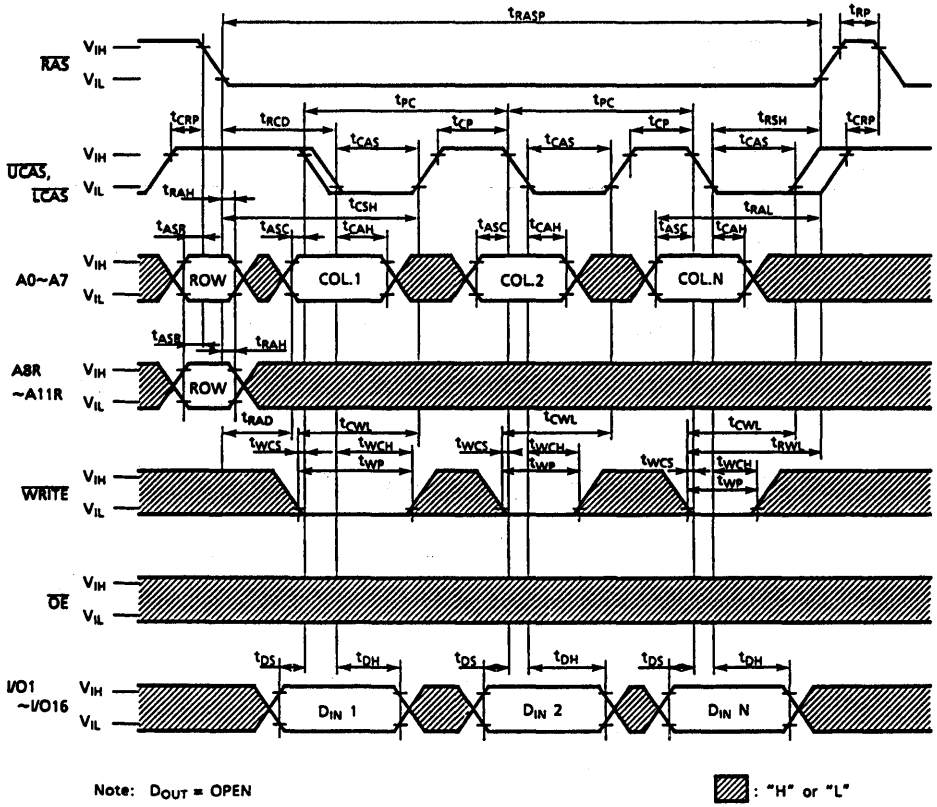
Note: D_{IN} = OPEN

▨ : "H" or "L"

FAST PAGE MODE BYTE READ CYCLE



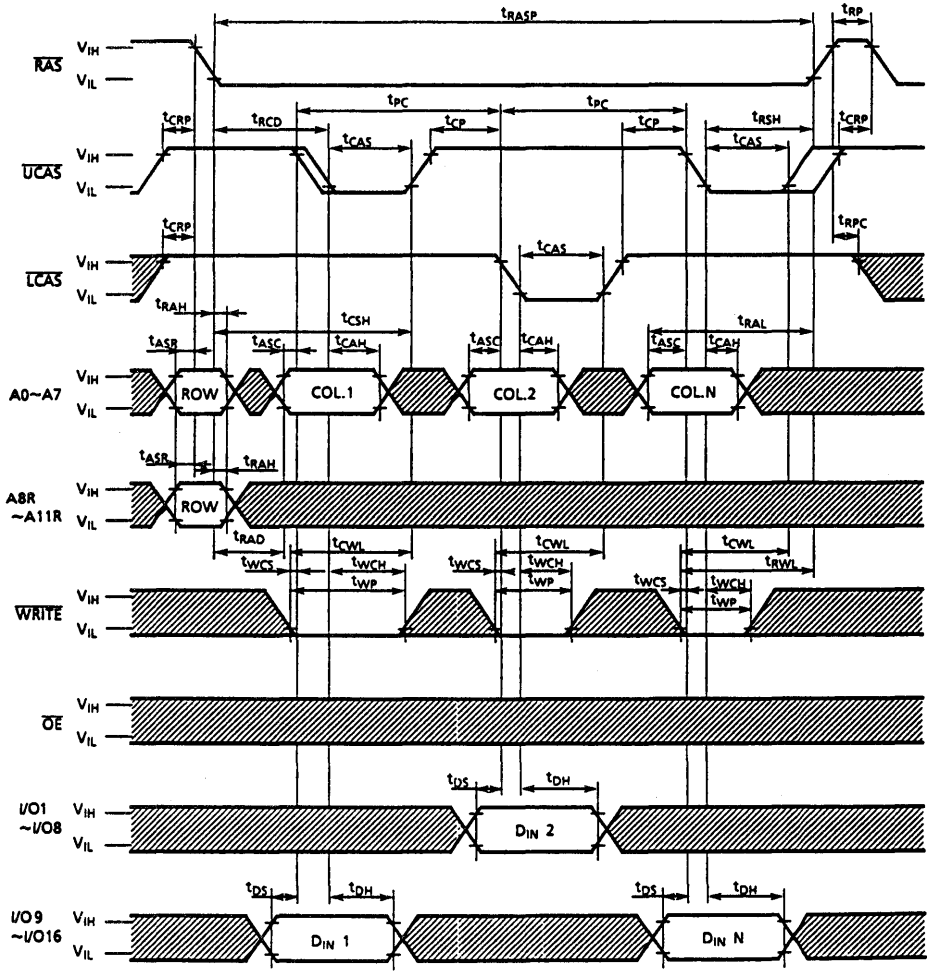
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

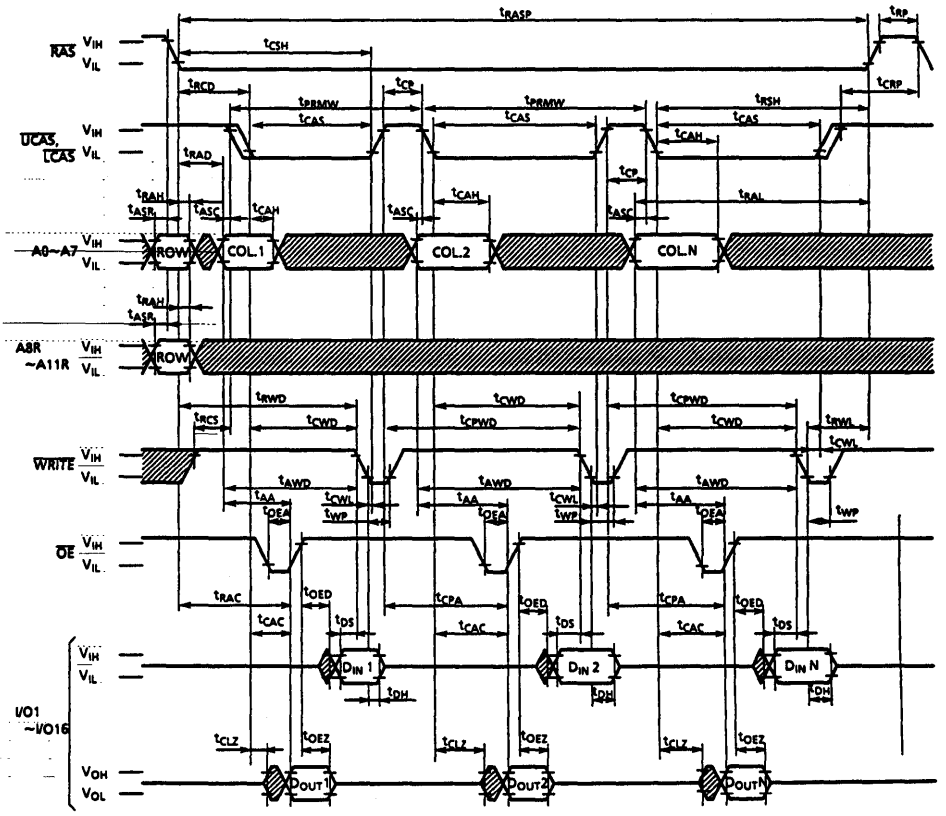
FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



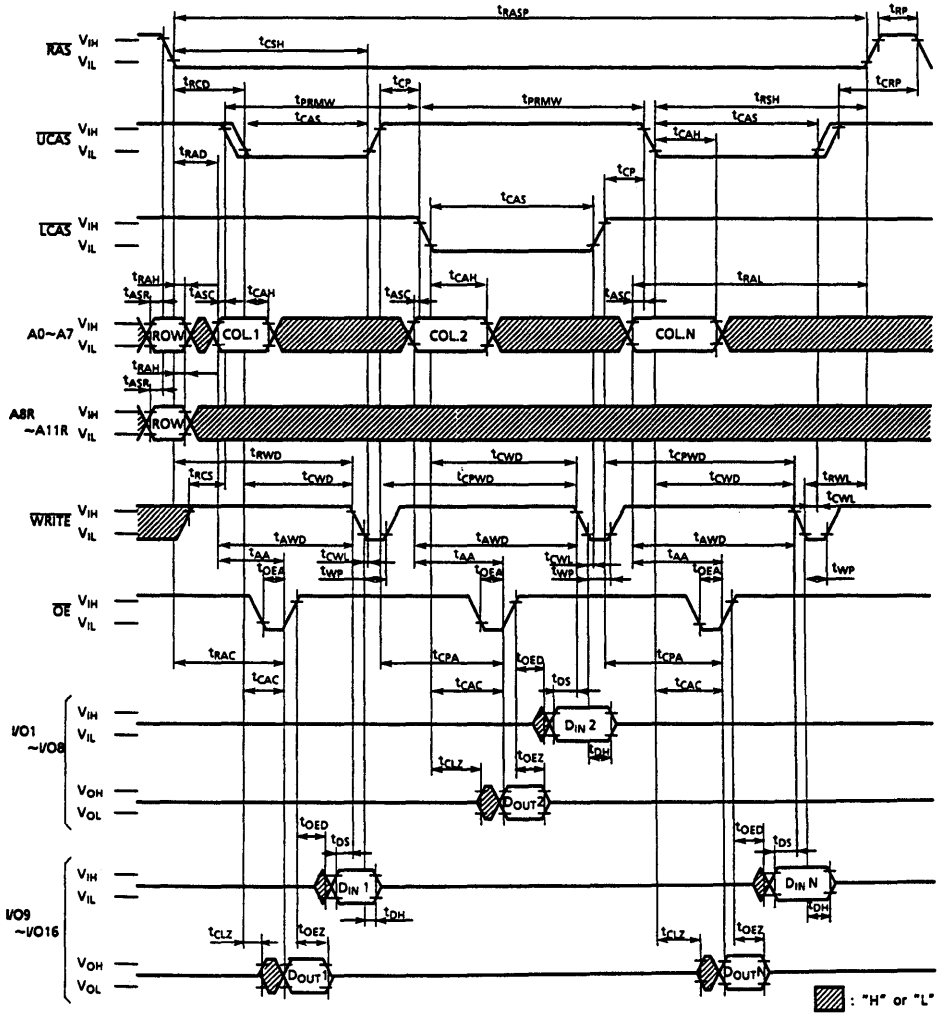
Note: D_{OUT} = OPEN

▨ : "H" or "L"

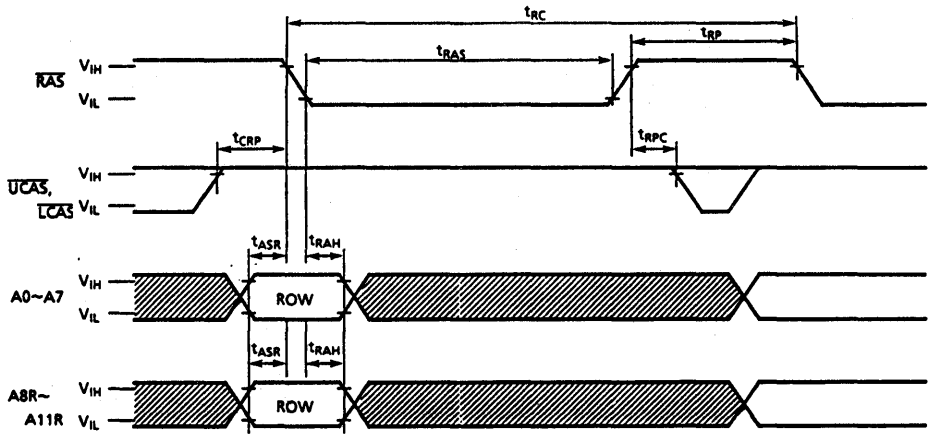
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE

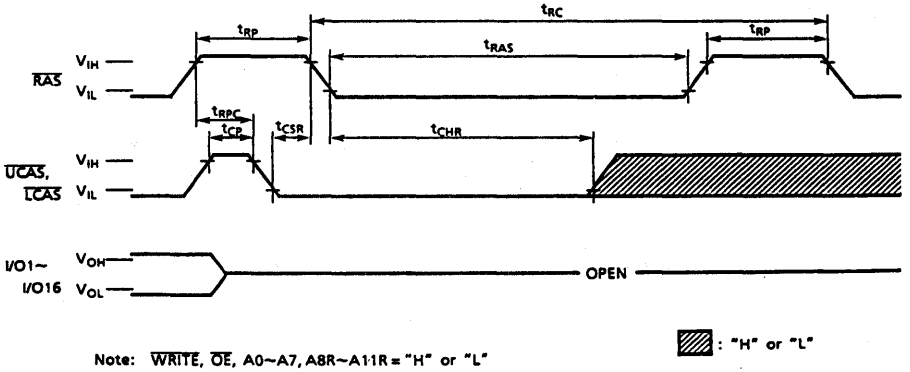


$\overline{RAS}$ ONLY REFRESH CYCLE



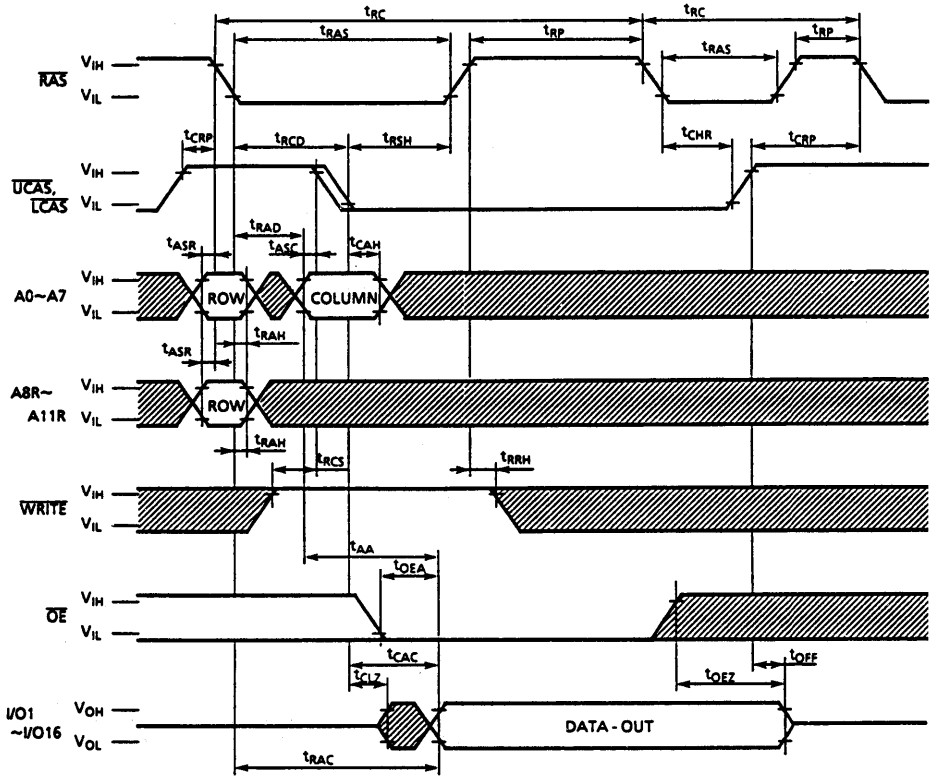
Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"
D_{IN} = Don't Care
D_{OUT} = OPEN

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$, A0~A7, A8R~A11R = "H" or "L"
D_{IN} = Don't Care
$\overline{CAS}$ before $\overline{RAS}$ refresh is performed when either $\overline{UCAS}$ or $\overline{LCAS}$ meets this timing.

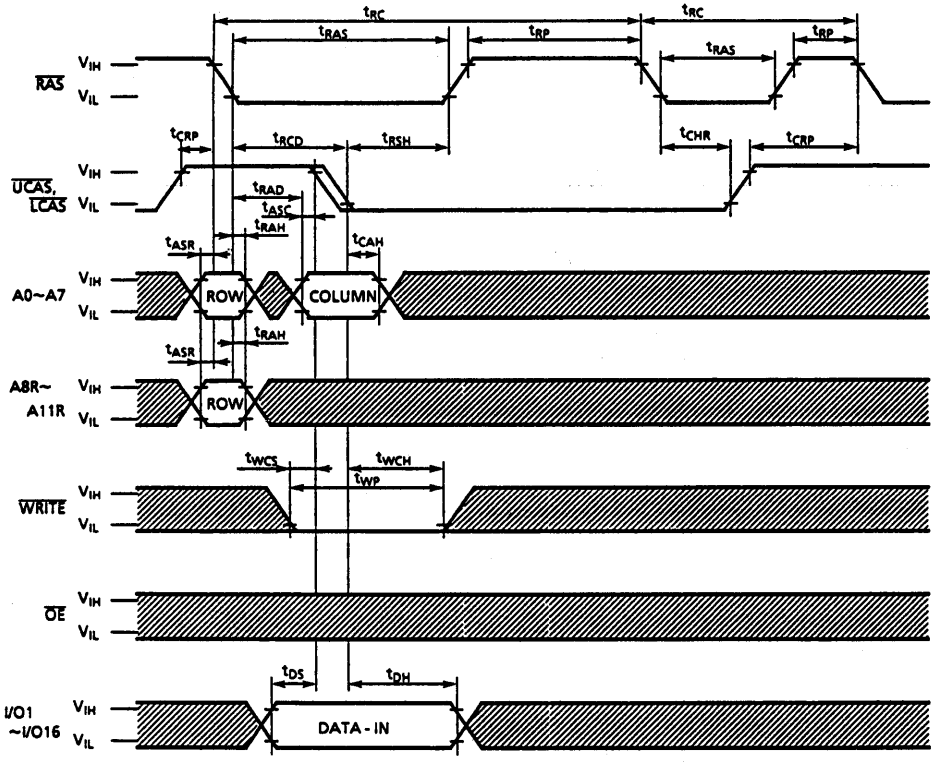
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨ : "H" or "L"

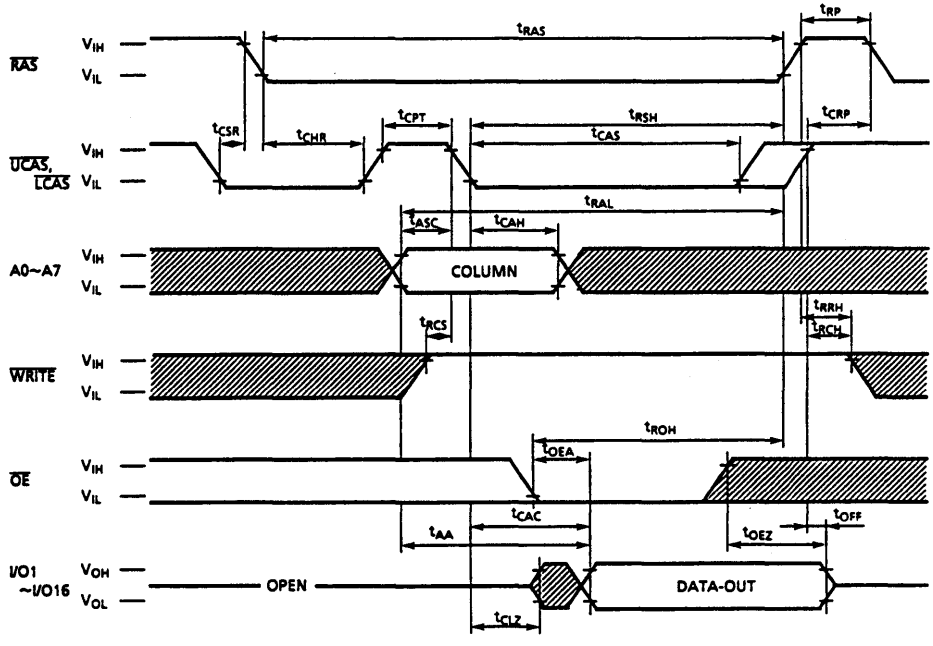
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

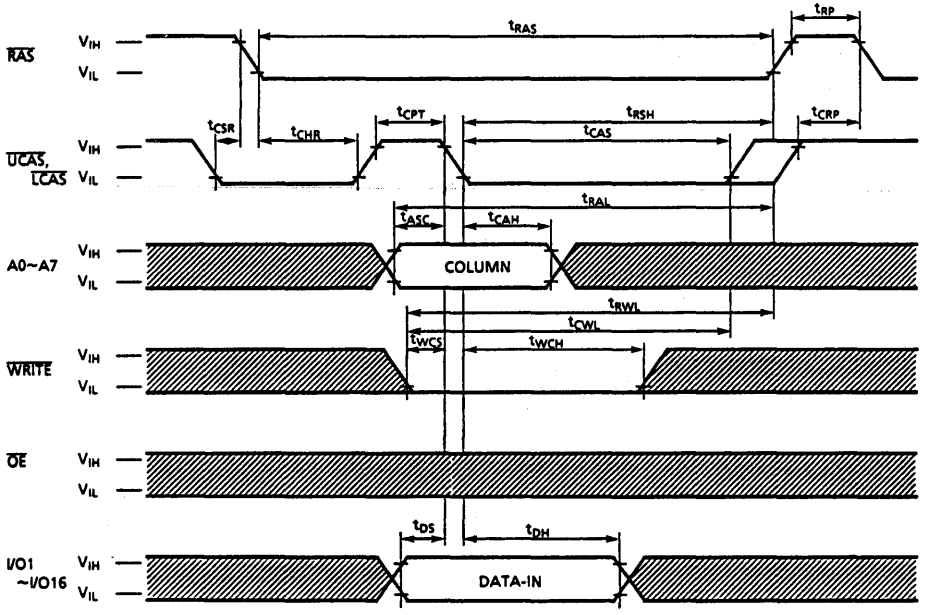
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



Note: A8R~A11R = "H" or "L"
D_{IN} = OPEN

▨ : "H" or "L"

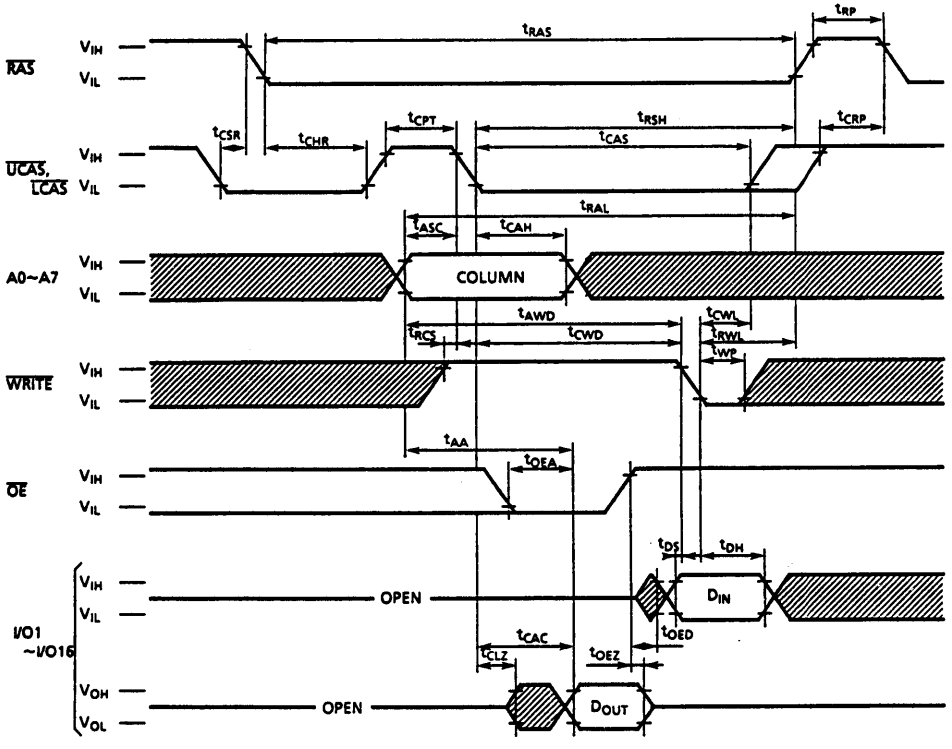
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



Note: A8R~A11R = "H" or "L"
D_{OUT} = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



Note: A8R~A11R = "H" or "L"

▨: "H" or "L"

1,048,576 WORD X 18 BIT DYNAMIC RAM

DESCRIPTION

The TC5118180AJ/FT is the new generation dynamic RAM organized 1,048,576 word by 18 bit. The TC5118180AJ/AFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5118180AJ/AFT to be packaged in a standard 40 pin plastic SOJ, and 50/44 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL,

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  825mW MAX .Operating
  (TC5118180AJ/AFT-70)
  715mW Max. Operating
  TC5118180AJ/AFT-80
  5.5mW Max. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Moode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package TC5118180AJ : SOJ42-P-400
  TC5118180AFT : TSOP50-P-400

KEY PARAMETERS

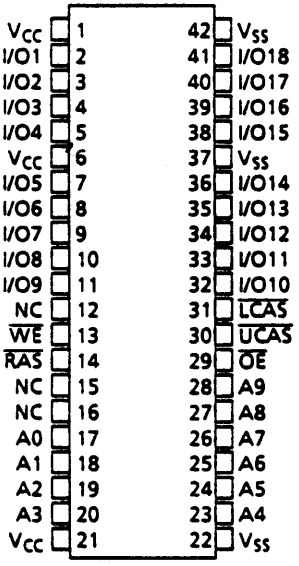
ITEM		TC5118180AJ/AFT	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	45ns	50ns

PIN NAME

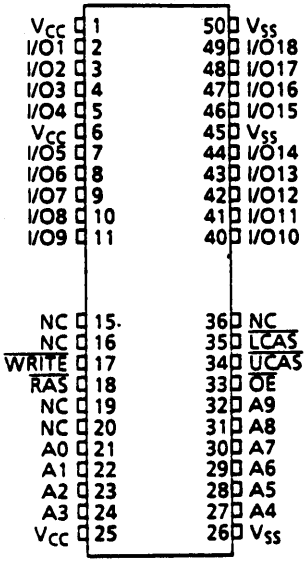
A0~A9	Row Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Byte Control
$\overline{LCAS}$	Lower Byte Control
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O18	Data Input/Output
V_{CC}	Power (+ 5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

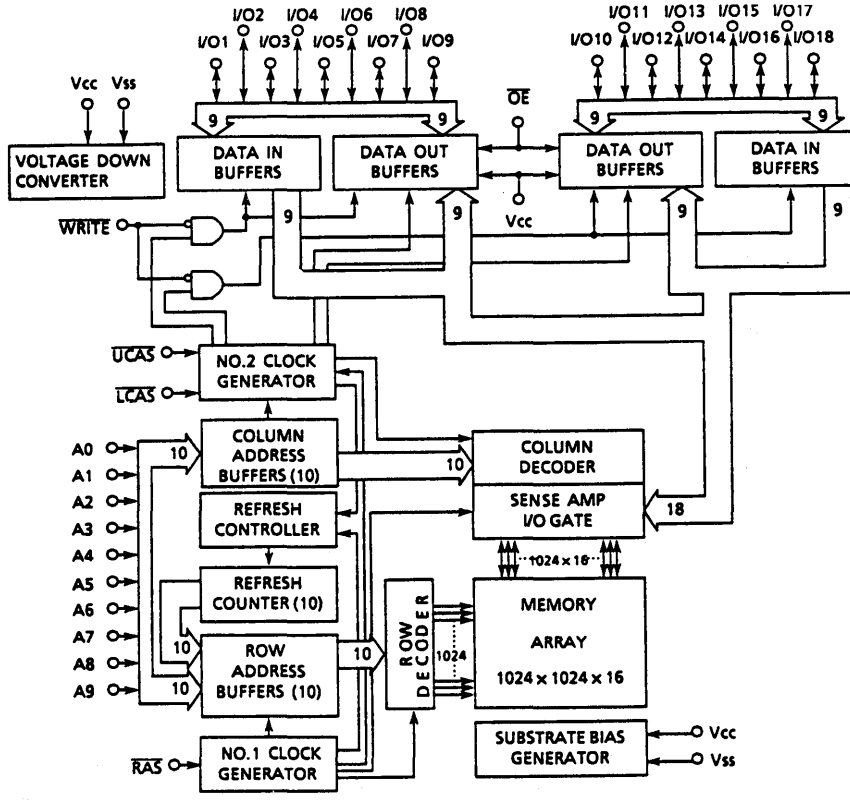
Plastic SOJ



Plastic TSOP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7$	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	900	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITION (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	High Level Input Voltage	2.4	-	V_{CC}+0.5*	V	2
V_{IL}	Low Level Input Voltage	-0.5**	-	0.8	V	2

* V_{CC} + 2.0V at pulse width ≤ 20ns. (pulse width is measured at V_{CC})
** -2.0V at pulse width ≤ 20ns. (pulse width is measured at 0V)

D.C. OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ Addrs. Cycling: t_{RC}=t_{RC} MIN)	TC5118180AJ/AFT-70	-	150	mA	3,4 5
		TC5118180AJ/AFT-80	-	130		
I_{CC2}	STANBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current ($\overline{RAS}$ Only Mode ($\overline{RAS}$, Cycling, $\overline{UCAS}$,= $\overline{LCAS}$ V_{IH}: t_{RC}=t_{RC} MIN)	TC5118180AJ/AFT-70	-	150	mA	3, 5
		TC5118180AJ/AFT-80	-	130		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$ Addrs.Cycling: t_{PC}=t_{PC} MIN)	TC5118180AJ/AFT-70	-	85	mA	3, 4, 5
		TC5118180AJ/AFT-80	-	75		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current, ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$= V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$,Cycling: t_{RC}=t_{RC}	TC5118180AJ/AFT-70	-	150	mA	3, 5
		TC5118180AJ/AFT-80	-	130		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≤ V_{IN}≤ V_{CC}, All Other Pins Not Under Test=OV		-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, ≤ 0V≤ V_{OUT} ≤ V_{CC}		-10	10	µA	
V_{OH}	OUTPUT LEVEL (Output "H" Level Voltage (I_{OUT} = 5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL (Output "H" Level Voltage (I_{OUT} = 4.2mA)		-	0.4	V	

CAPACITANCE *(T_{CC}= 5V± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 ~A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_0	Input/Output Capacitance (I/O1~I/O18)	-	7	pF

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC5118180AJ/AFT				UNIT	NOTES
		-70		-80			
		MIN	MAX.	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC5118180AJ/AFT				UNIT	NOTES
		-70		-80			
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	8	-	8	ns	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	-	110	-	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	-	70	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	75	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	30	-	30	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to OE	10	-	10		ns	
t_{OEA}	$\overline{OE}$ Access TIme	-	20	0	20	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieveS the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

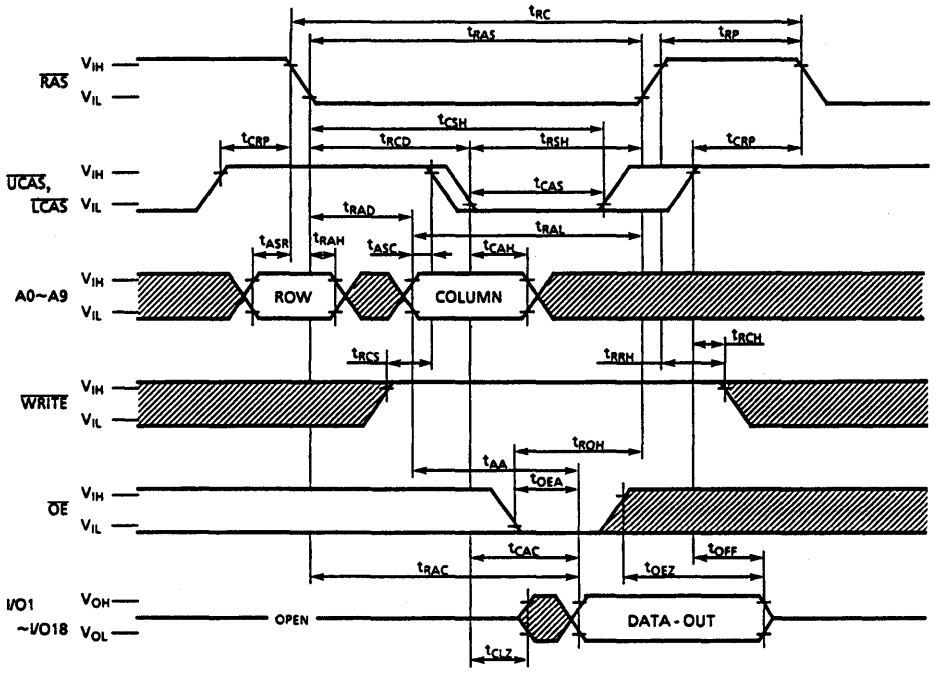
12. These parameters are referenced to $\overline{UCAS}$ or $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

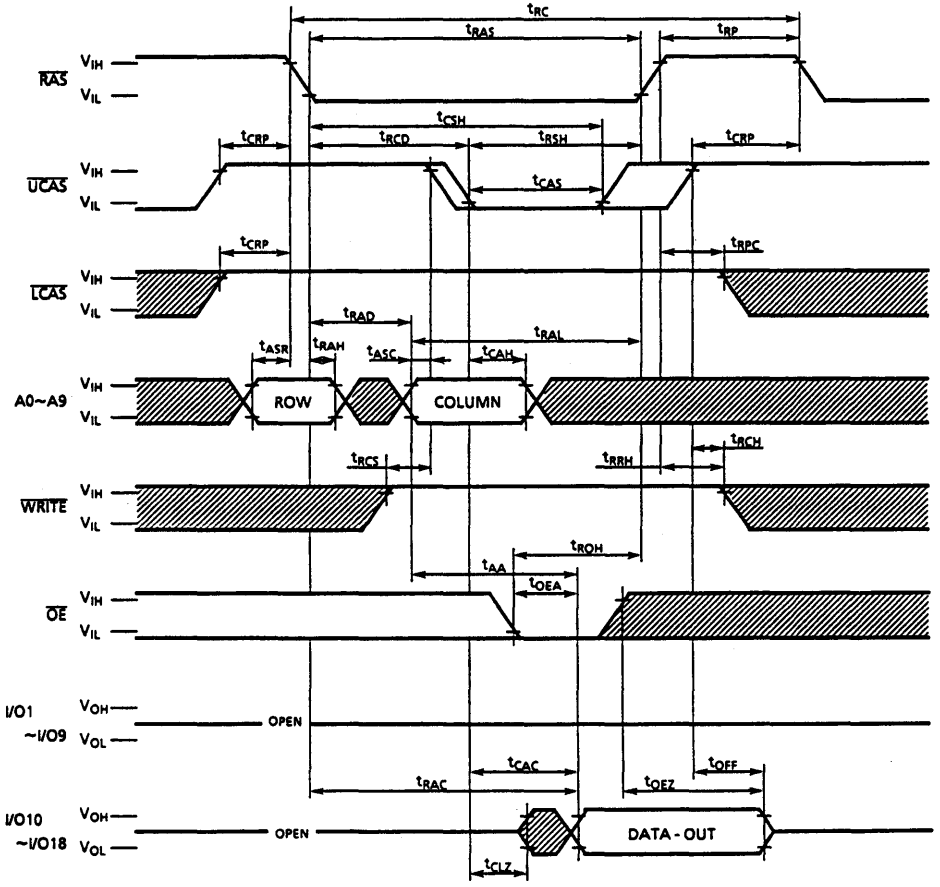
READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

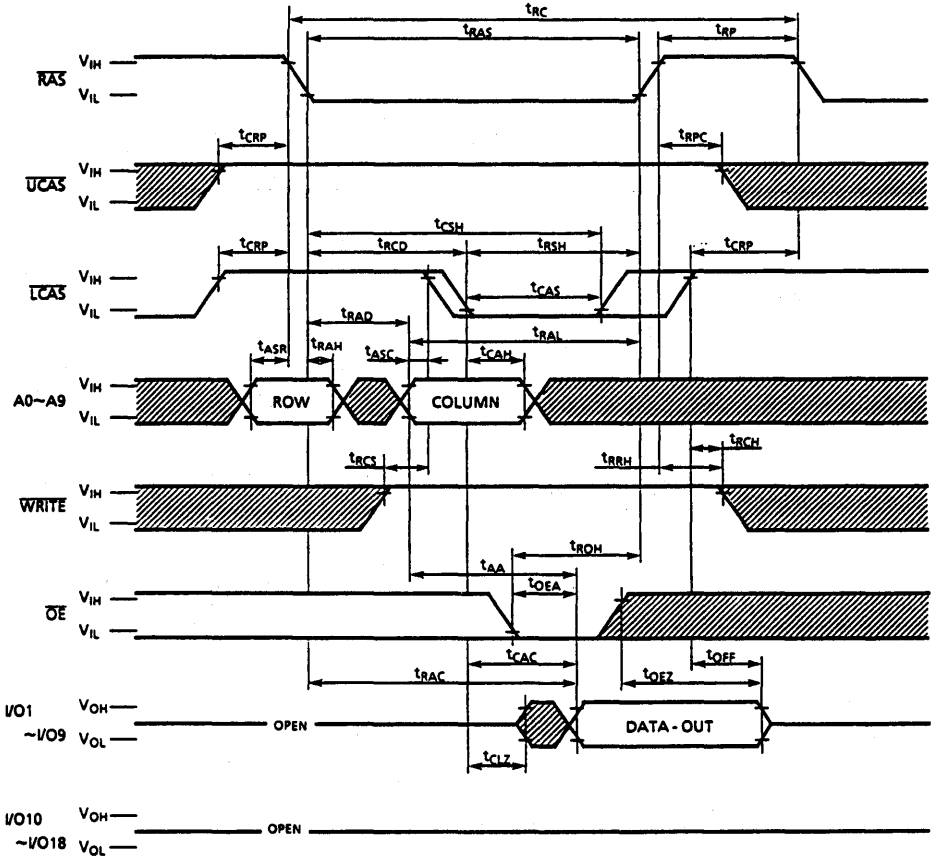
UPPER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O9) = Don't Care
D_{IN} (I/O10~I/O18) = OPEN

▨ : "H" or "L"

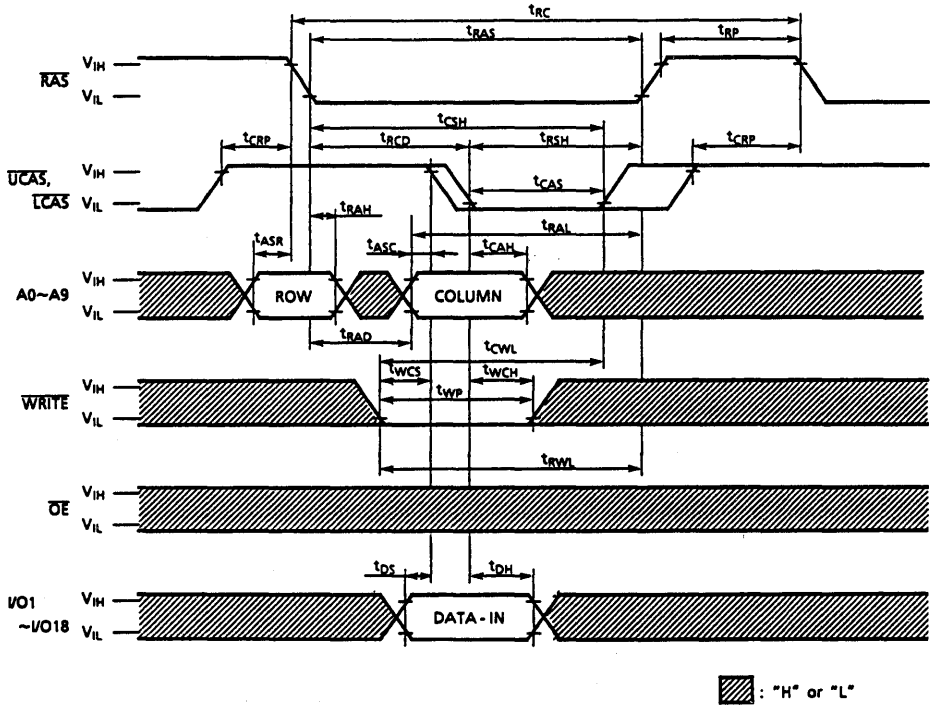
LOWER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O9) = OPEN
D_{IN} (I/O10~I/O18) = Don't Care

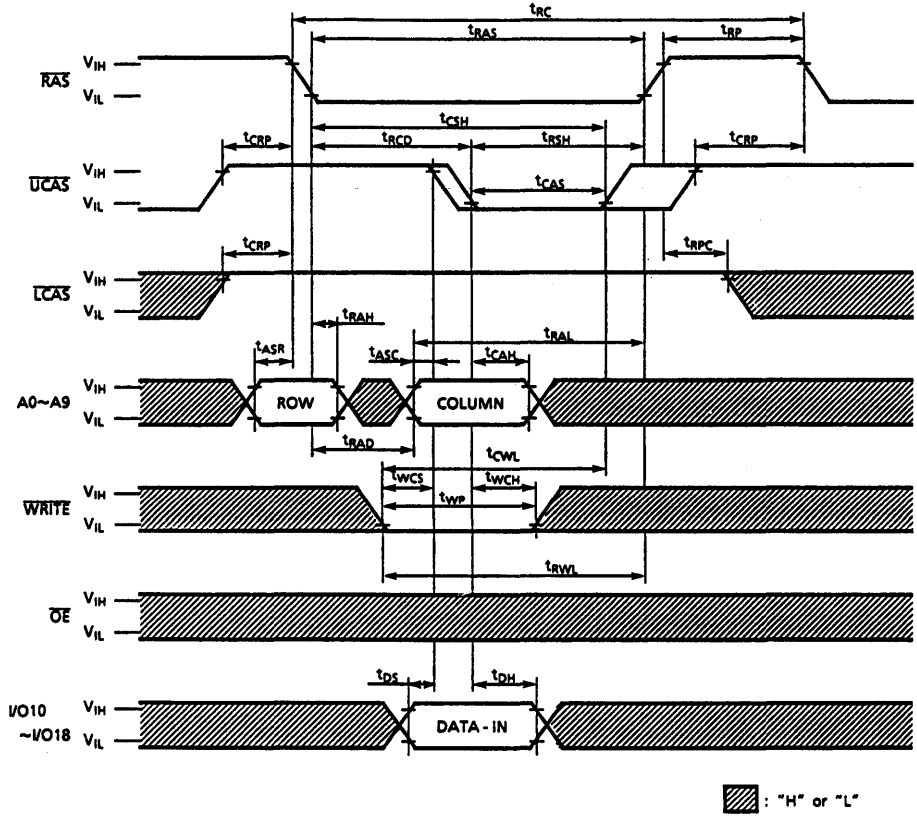
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE)



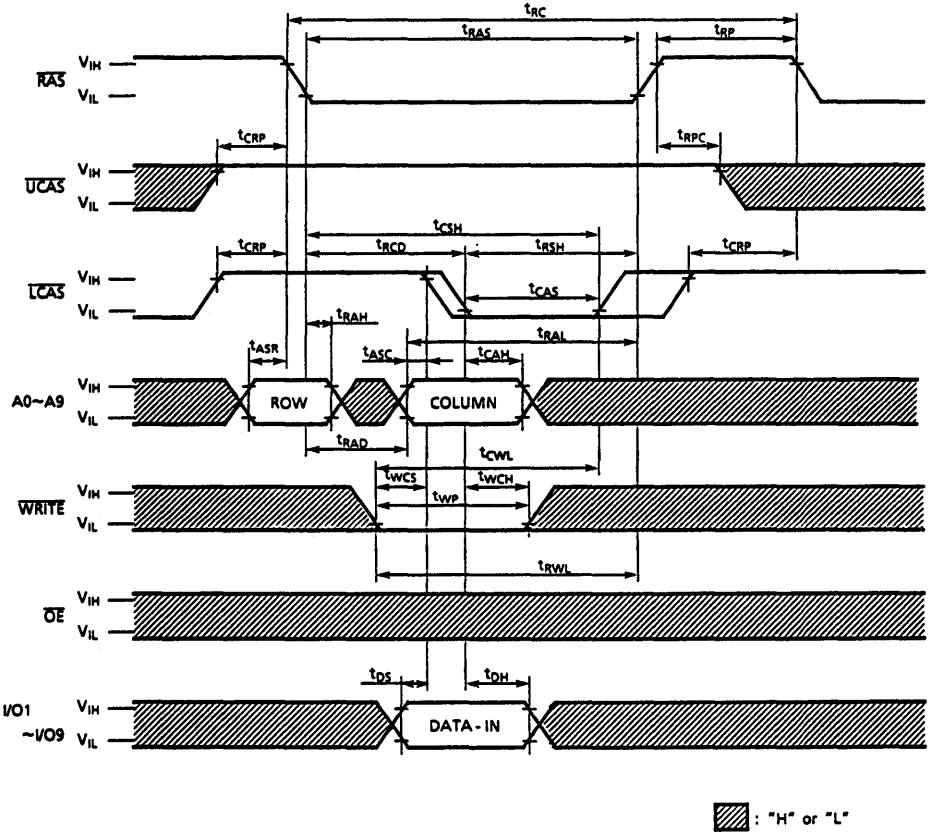
Note: D_{OUT} = OPEN

UPPER BYTE WRITE CYCLE (EARLY WRITE)



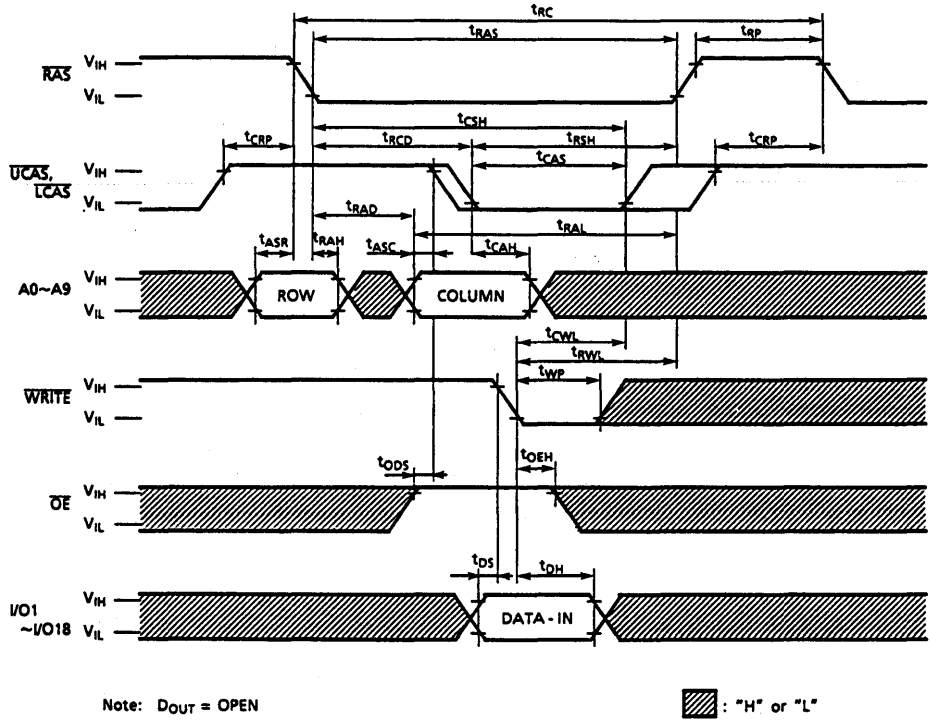
Note: D_{IN} (I/O1~I/O9) = Don't Care
D_{OUT} = OPEN

LOWER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{IN} (I/O10~I/O18) = Don't Care
D_{OUT} = OPEN

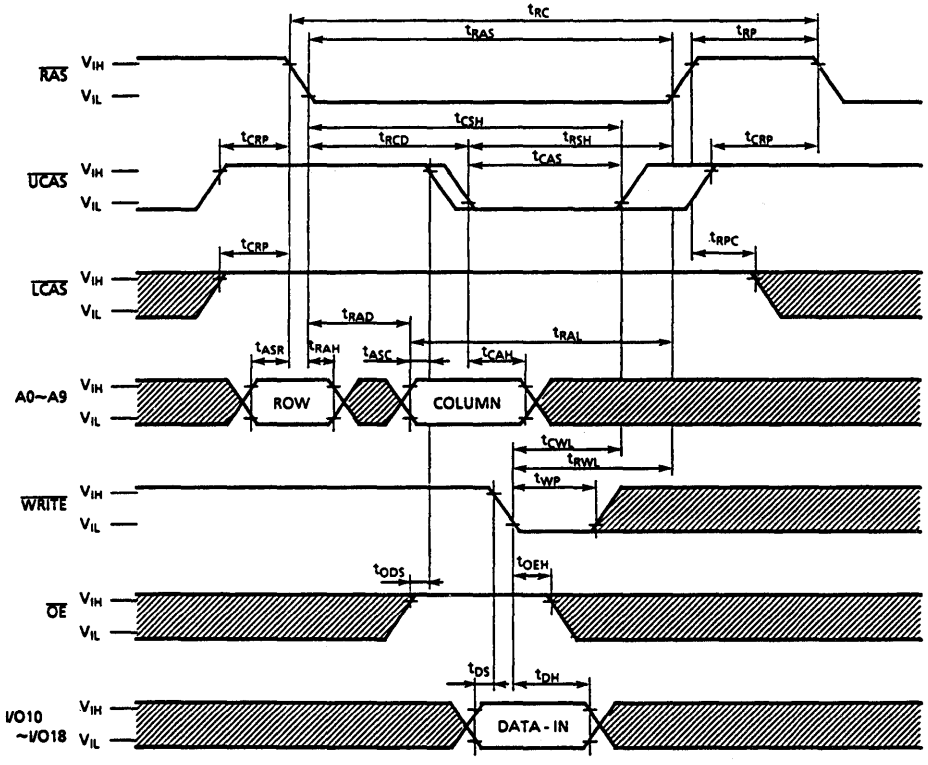
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

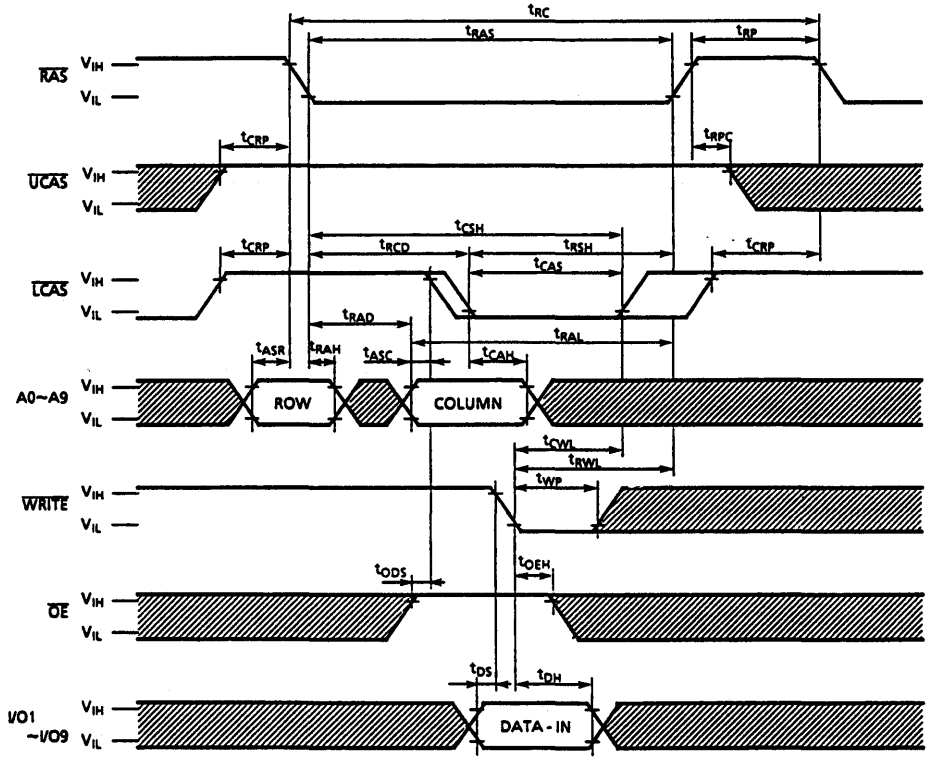
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{IN} (I/O1~I/O9) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

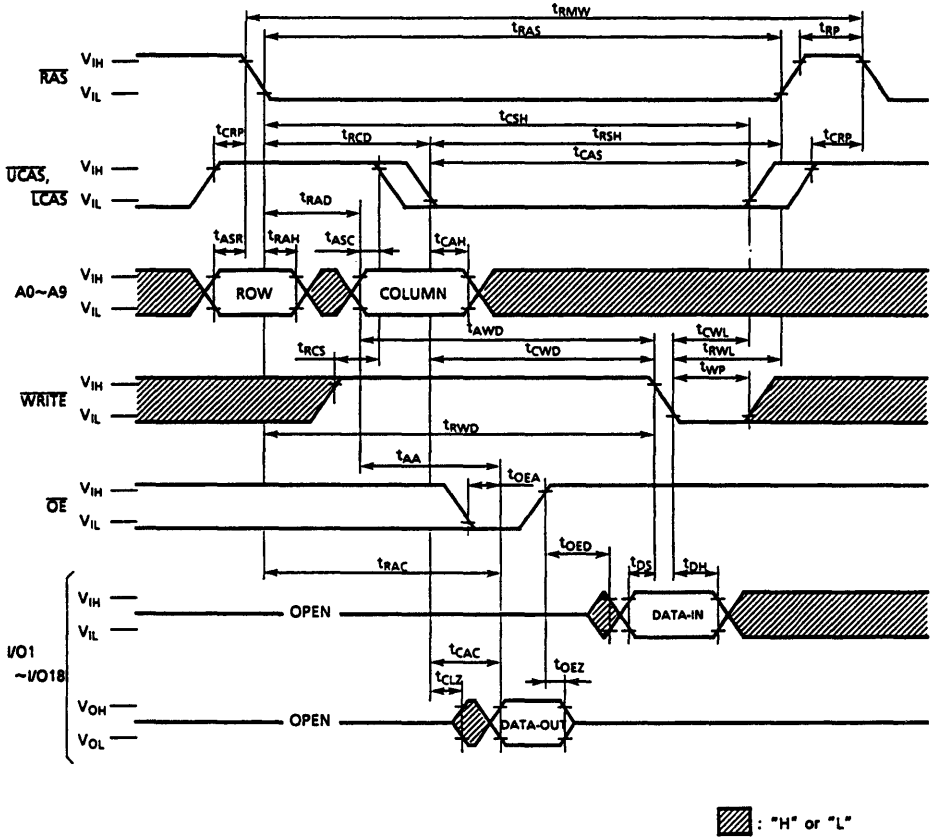
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



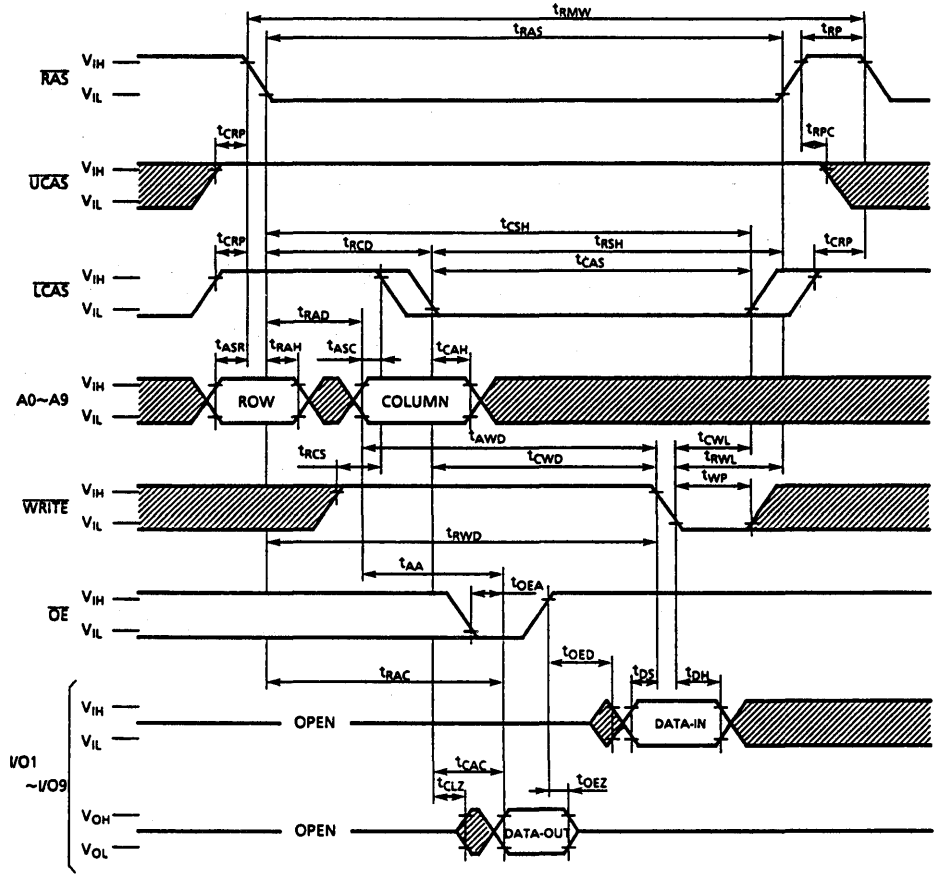
Note: D_{IN} (I/O10~I/O18) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE

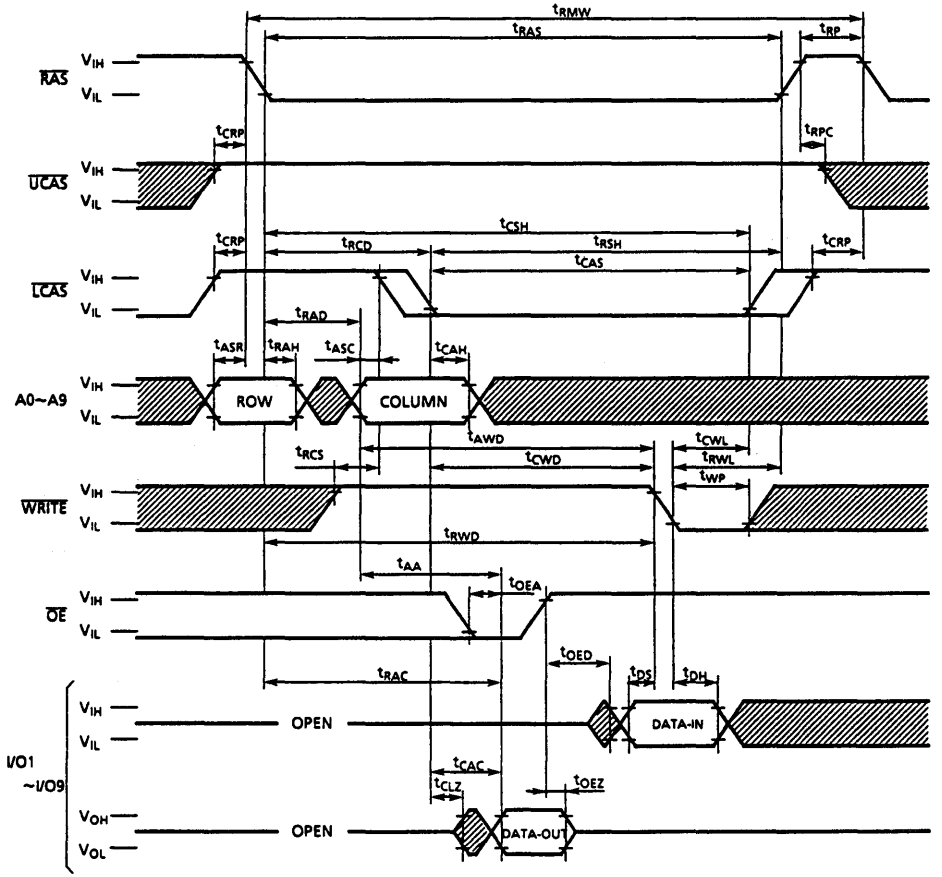


UPPER BYTE READ-MODIFY-WRITE CYCLE



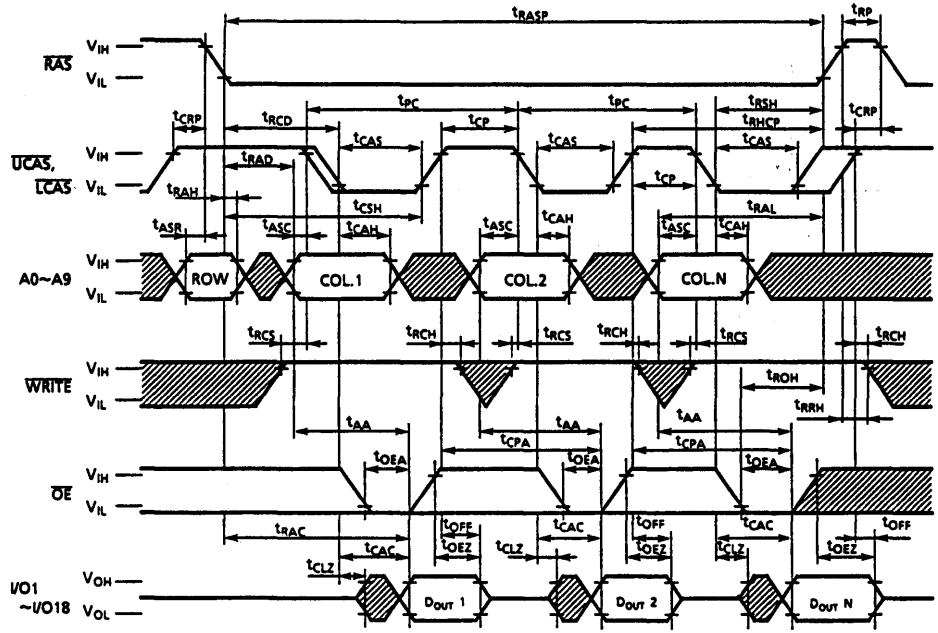
Note: D_{IN} (I/O10~I/O18) = Don't Care
D_{OUT} (I/O10~I/O18) = OPEN

LOWER BYTE READ-MODIFY-WRITE CYCLE



Note: D_{IN} (I/O10~I/O18) = Don't Care
D_{OUT} (I/O10~I/O18) = OPEN

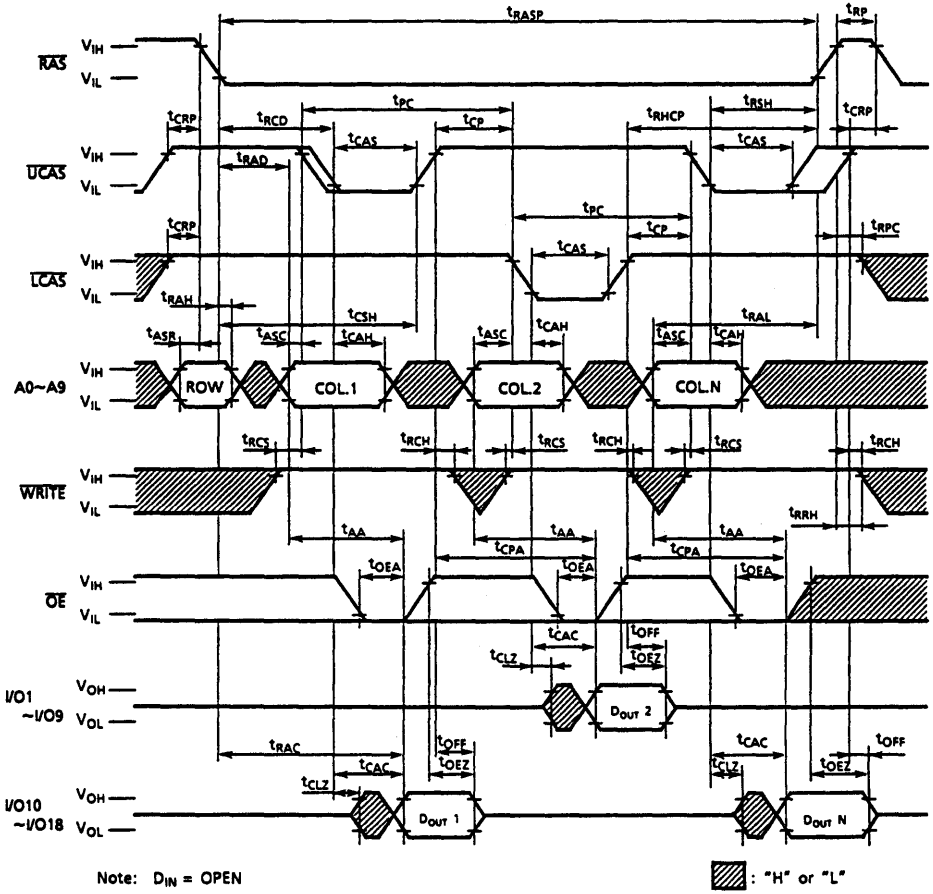
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

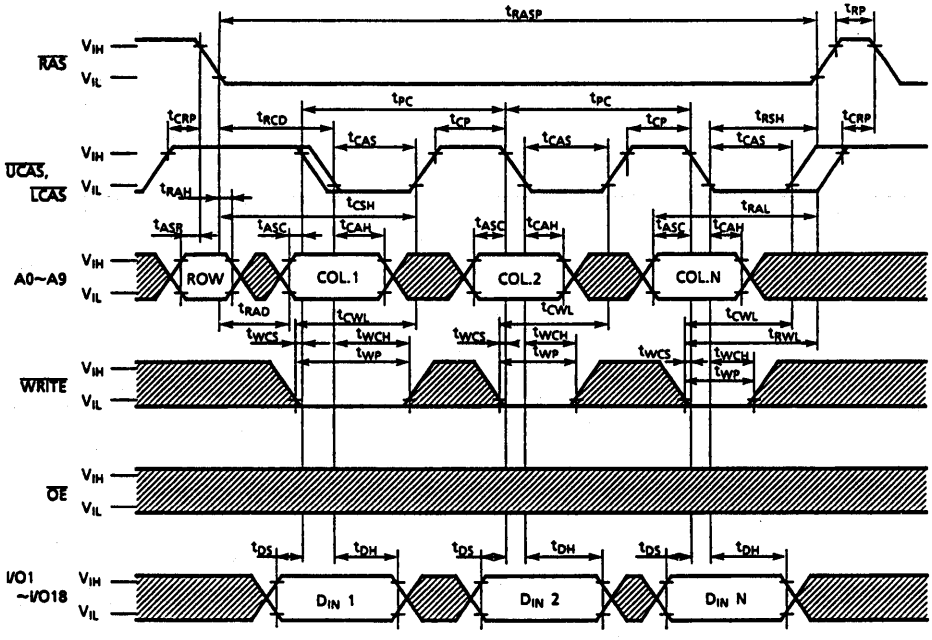
FAST PAGE MODE BYTE READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

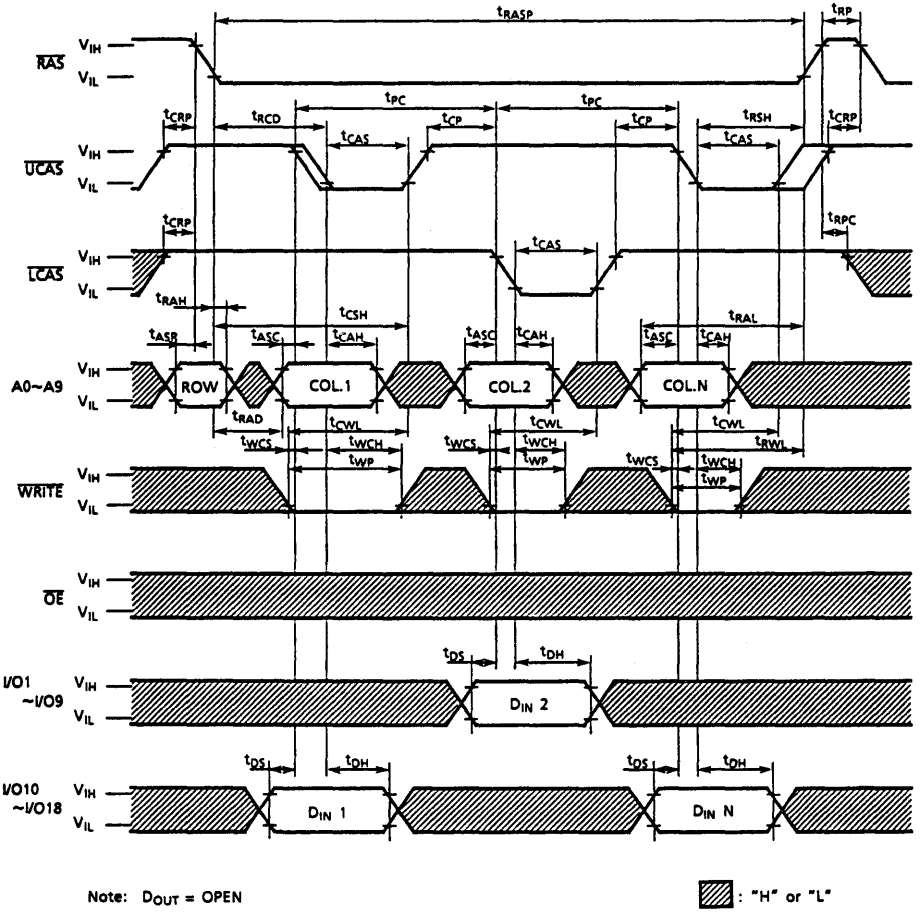
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨: "H" or "L"

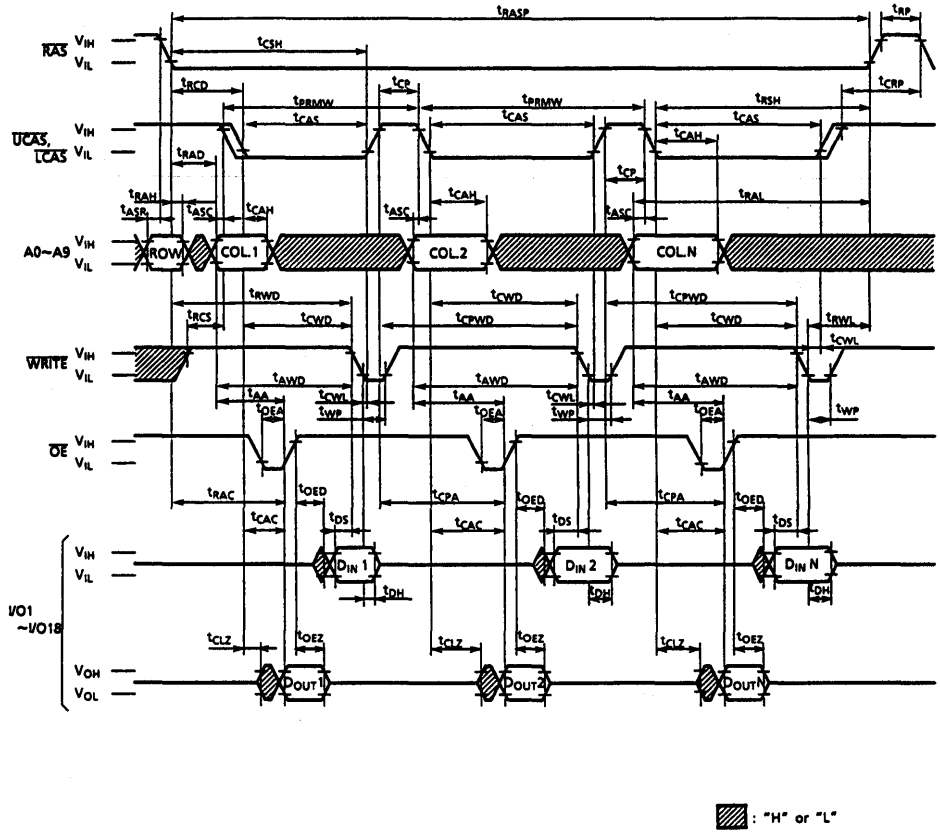
FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



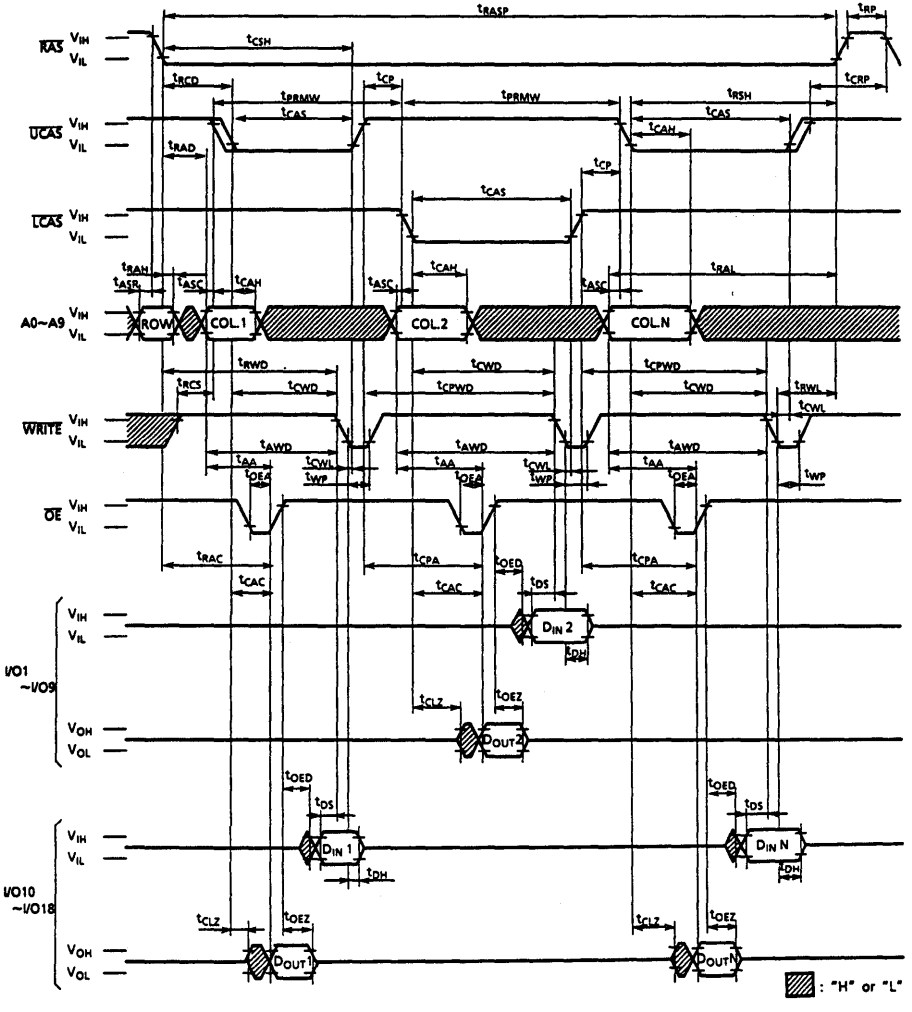
Note: D_{OUT} = OPEN

▨ : "H" or "L"

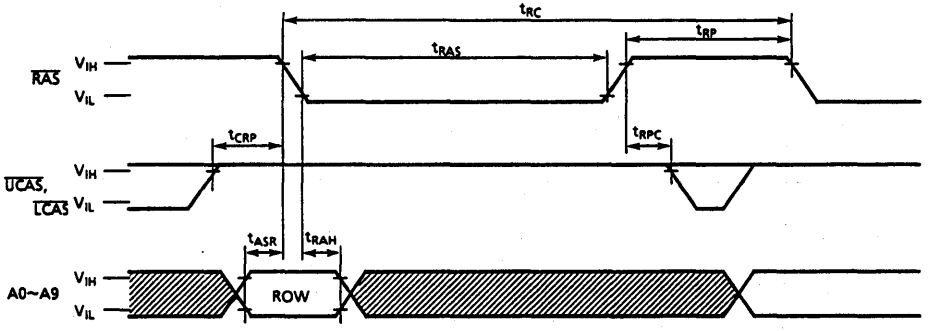
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE



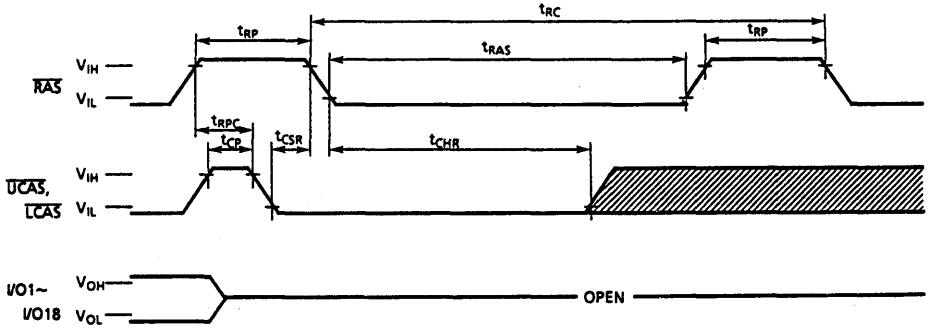
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"
D_{IN} = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

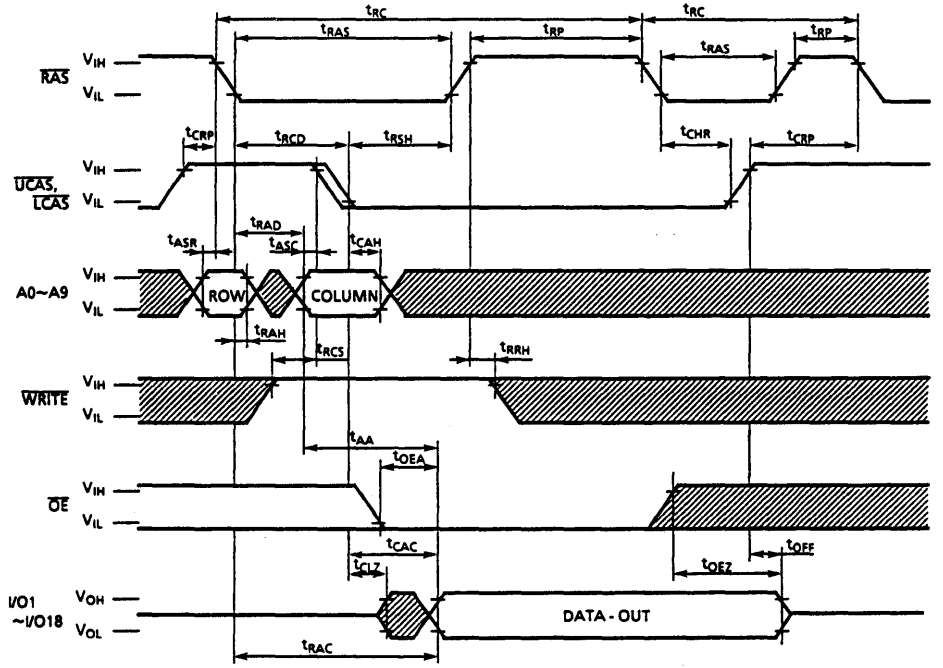
$\overline{CAS}$ BEFORE $\overline{RAS}$ ONLY REFRESH CYCLE



▨ : "H" or "L"

Note: $\overline{WRITE}$, $\overline{OE}$, A0~A9 = "H" or "L"
D_{IN} = Don't Care
$\overline{CAS}$ before $\overline{RAS}$ refresh is performed when either $\overline{UCAS}$ or $\overline{LCAS}$ meets this timing.

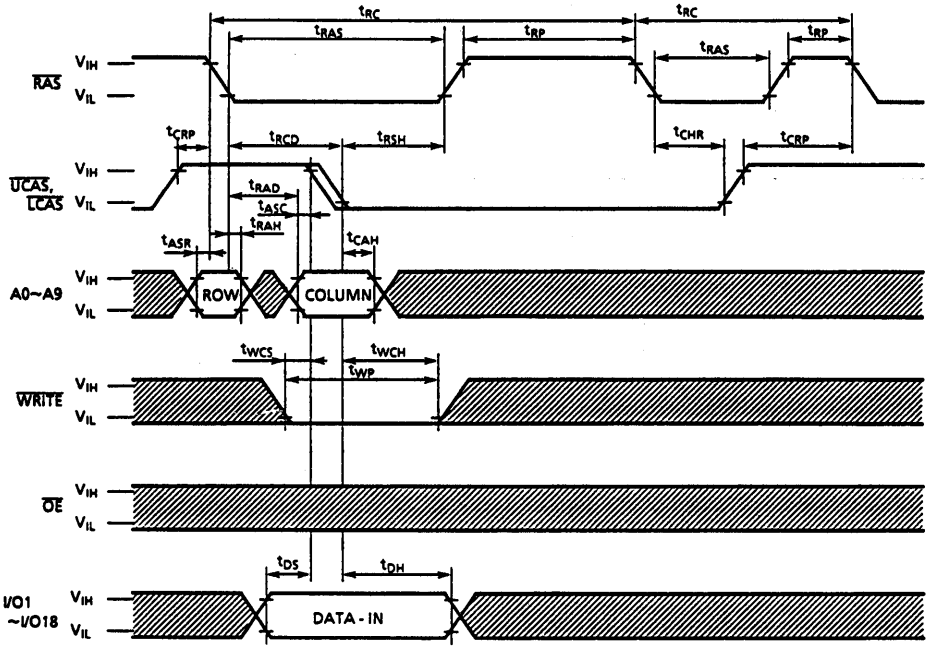
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨ : "H" or "L"

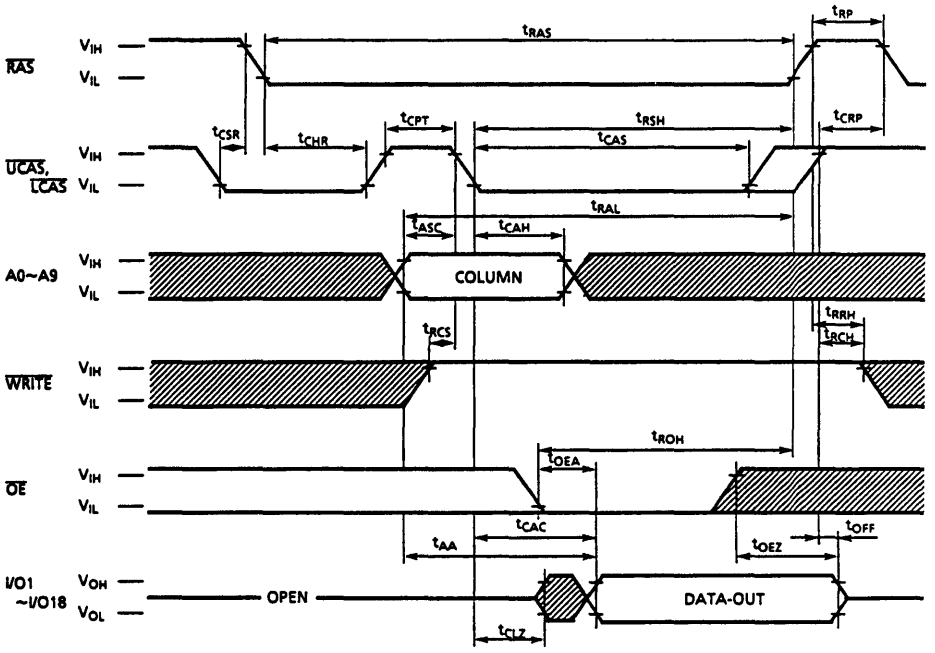
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

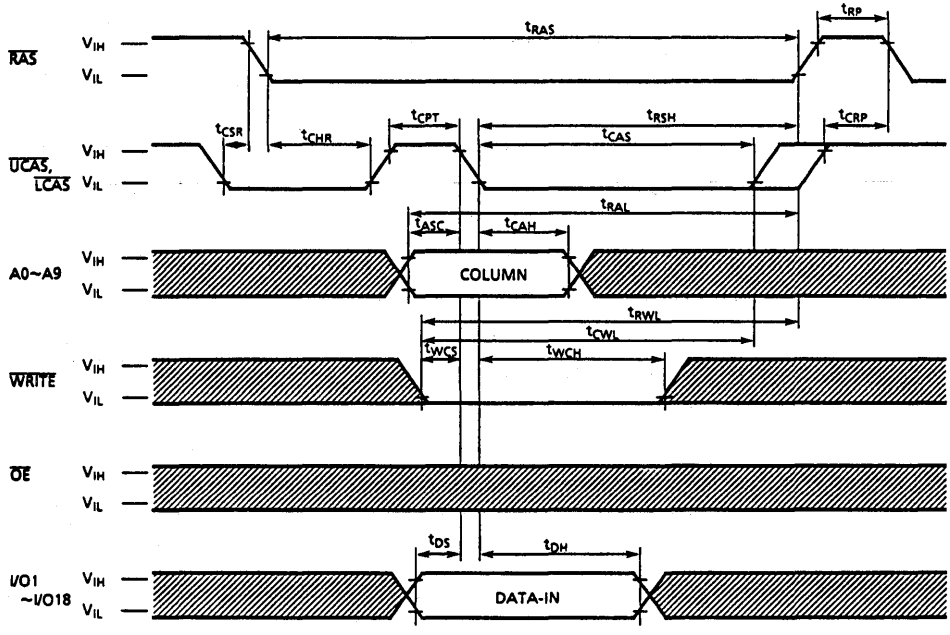
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or

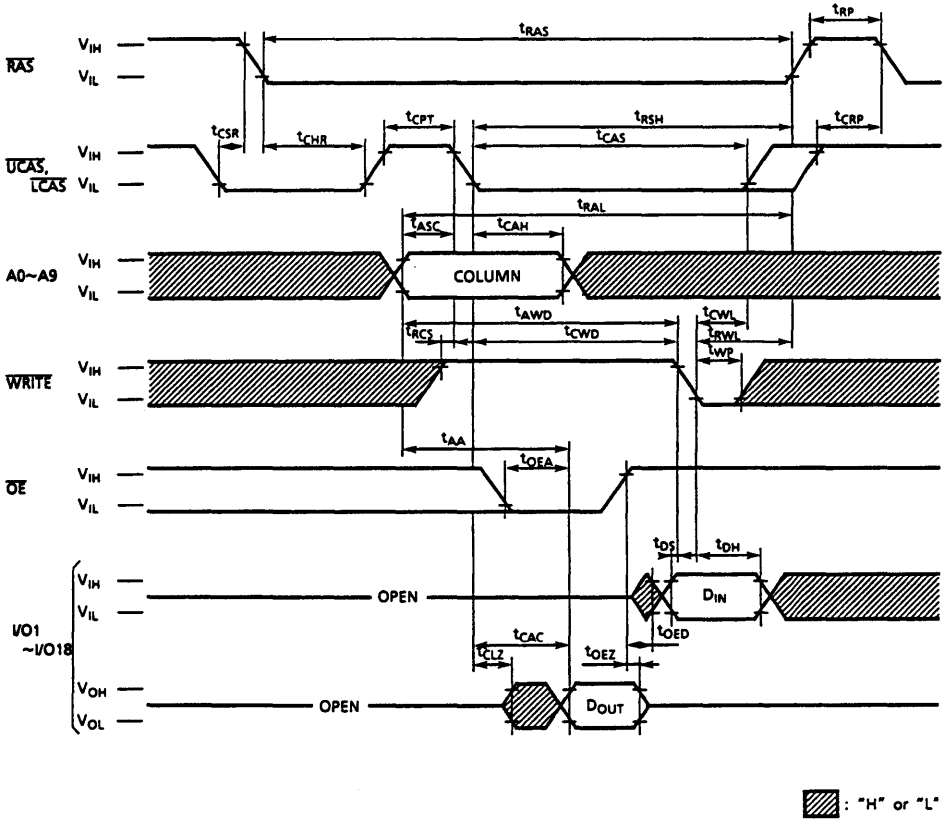
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



Note: D_{OUT} = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



1,048,576 WORD X 18 BIT DYNAMIC RAM

DESCRIPTION

The TC5116180AJ/AFT is the new generation dynamic RAM organized 1,048,576 word by 18 bit. The TC5116180AJ/AFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5116180AJ/AFT to be packaged in a standard 42 pin plastic SOJ, and 50/44 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  578mW MAX .Operating
  (TC5116180AJ/AZ/AFT/ATR-60)
  495mW Max. Operating
  (TC5116180AJ/AZ/AFT/ATR-70
  440mW Max. Operating
  (TC5116180AJ/AZ/AFT/ATR-80
  5.5mW Max. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode capability
- All inputs and outputs TTL compatible
- 4096 refresh cycles/16ms
- Package TC5116180AJ : SOJ42-P-400
  TC5116180AFT :TSOP50-P-400

KEY PARAMETERS

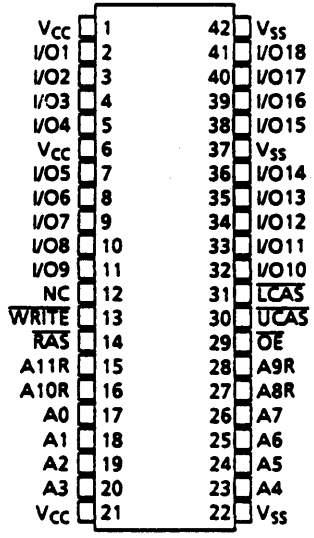
ITEM		TC5116180AJ/AFT		
		-60	-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA}	Column Address Access Time	30ns	40ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns	20ns
t_{RC}	Cycle Time	110ns	150ns	150ns
t_{PC}	Fast Page Mode Cycle Time	40ns	50ns	50ns

PIN NAME

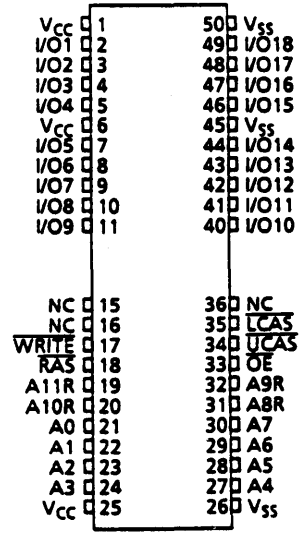
A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Byte Control
$\overline{LCAS}$	Lower Byte Control
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O18	Data Input/Output
V_{CC}	Power (+ 5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

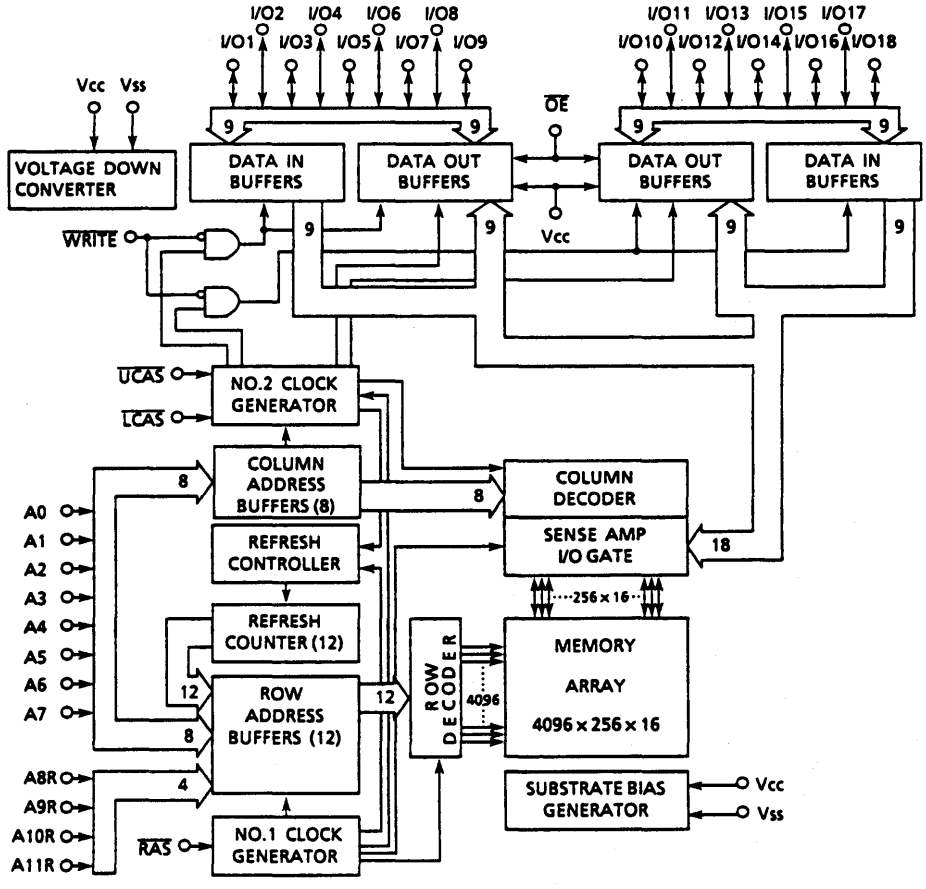
Plastic SOJ



Plastic TSOP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7$	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	$-55 \sim 150$	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	900	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITION (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	High Level Input Voltage	2.4	-	V_{CC}+0.5*	V	2
V_{IL}	Low Level Input Voltage	-0.5**	-	0.8	V	2

*V_{CC}+2.0V at pulse width ≤20ns (measured at V_{CC})
**-2.0V at pulse width ≤20ns (measured at V_{CC})

D.C. OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ Addrs. Cycling: t_{RC}=t_{RC} MIN)	TC5116180AJ/AFT-60	-	105	mA	3,4 5
		TC5116180AJ/AFT-70	-	90		
		TC5116180AJ/AFT-80		80		
I_{CC2}	STANBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IH})			2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current ($\overline{RAS}$ Only Mode ($\overline{RAS}$, Cycling, $\overline{UCAS}$=$\overline{LCAS}$=V_{IH}: t_{RC}=t_{RC} MIN)	TC5116180AJ/AFT-60	-	105	mA	3, 5
		TC5116180AJ/AFT-70	-	90		
		TC5116180AJ/AFT-80		80		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$ Addrs.Cycling: t_{PC}=t_{PC} MIN)	TC5116180AJ/AFT-60	-	80	mA	3, 4, 5
		TC5116180AJ/AFT-70	-	70		
		TC5116180AJ/AFT-80	-	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current, ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$= V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$,Cycling: t_{RC}=t_{RC}	TC5116180AJ/AFT-60	-	105	mA	3, 5
		TC5116180AJ/AFT-70	-	90		
		TC5116180AJ/AFT-80		80		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤ V_{IN}≤ V_{CC}, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, ≤ 0V≤ V_{OUT} ≤ V_{CC}		-10	10	μA	
V_{OH}	OUTPUT LEVEL (Output "H" Level Voltage (I_{OUT} = 5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL (Output "L" Level Voltage (I_{OUT} = 4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC5116180AJ/AFT						UNIT	NOTE
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	155	-	180	-	200	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	85	-	90	-	100	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-ZData Hold Time	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	10
t_T	Transition Time (rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		5		ns	
t_{CP}	$\overline{CAS}$ Presharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASH}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	15	-	ns	
t_{RAL}	Column Address To RAS Lead Time	30	-	35	-	40	-	ns	
t_{RCS}	Read Command Set-up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to RAS	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC5116180AJ/AFT						UNIT	NOTE
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	20	-	ns	
t_{DS}	Data Set-up Time	0	-	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	64	-	64	-	64	ns	
t_{WCS}	Write Command Set-up Time	0	-	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	40	-	45	-	45	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	-	95	-	105	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	55	-	60	-	65	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	60	-	65	-	70	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test	20	-	30	-	30	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	15	-	20	-	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	15	-	15	-	15	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	15	0	15	0	15	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	15	-	15	-	15	-	ns	
t_{ODS}	Output Disable Set-up Time	0	-	0	-	0	-	ns	

CAPACITANCE *(T_{CC}= 5V± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 ~A9)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (I/O1~I/O18)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieveS the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

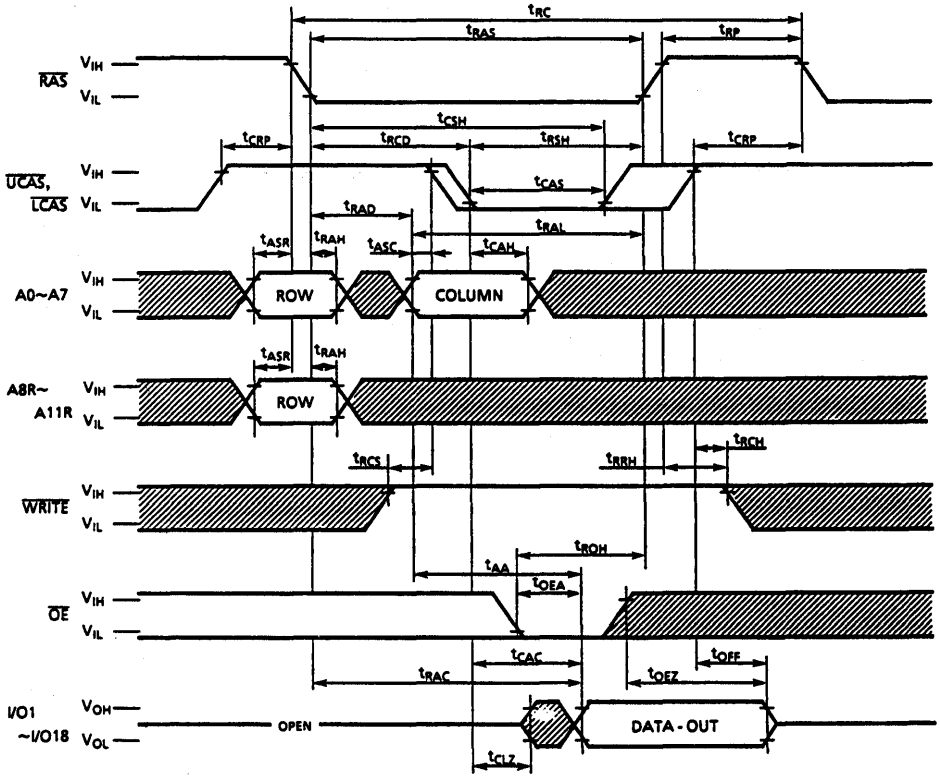
12. These parameters are referenced to $\overline{UCAS}$ or $\overline{LAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWP} > t_{CPWDD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

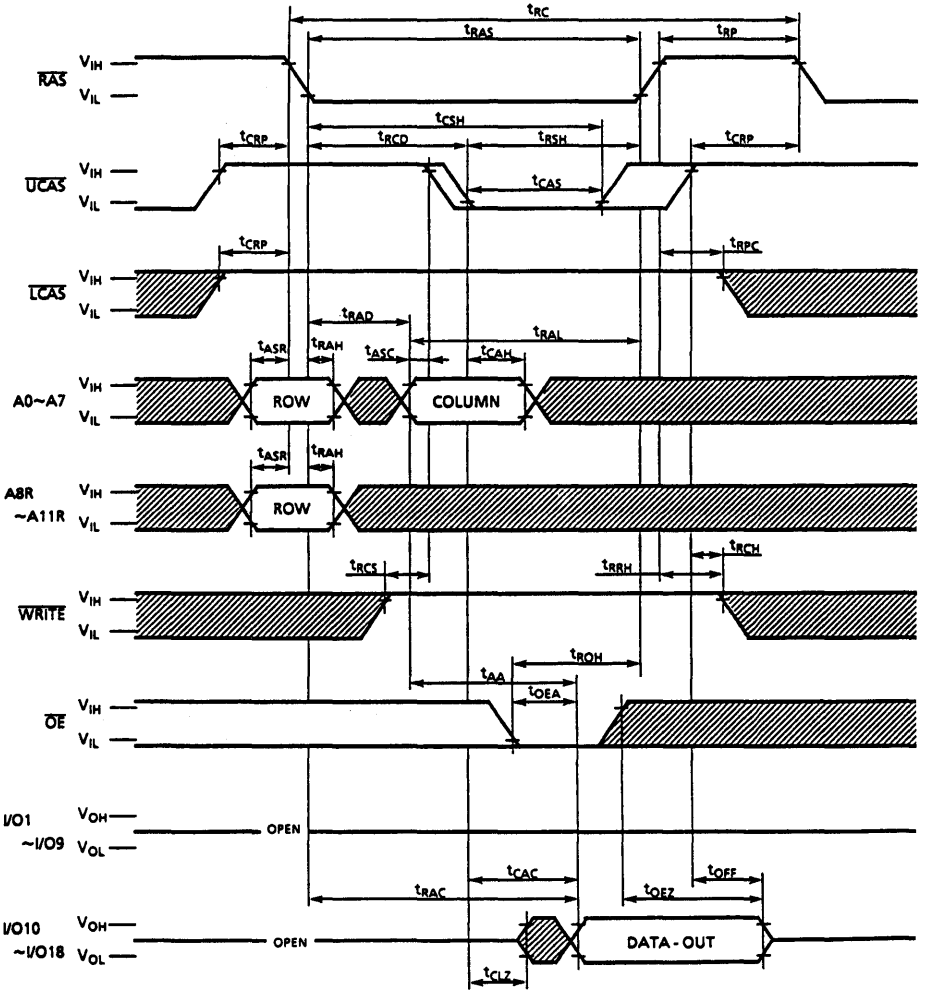
READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

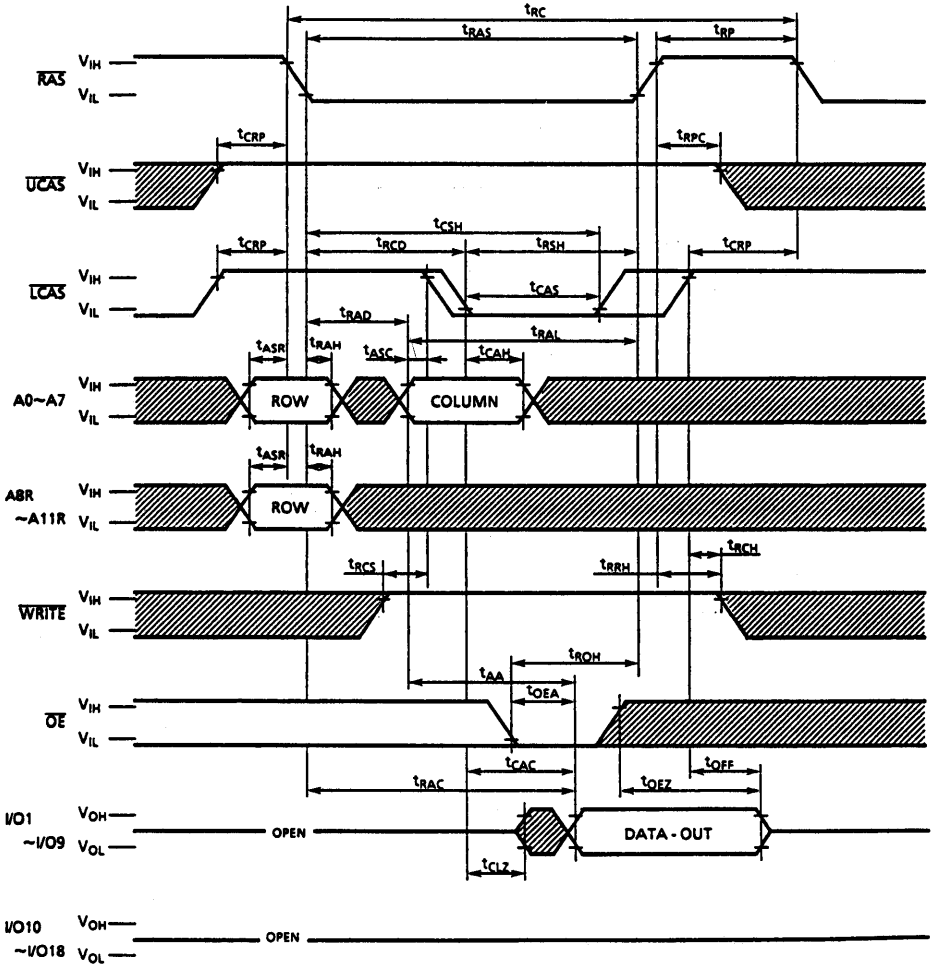
UPPER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O9) = Don't Care
D_{IN} (I/O10~I/O18) = OPEN

▨ : "H" or "L"

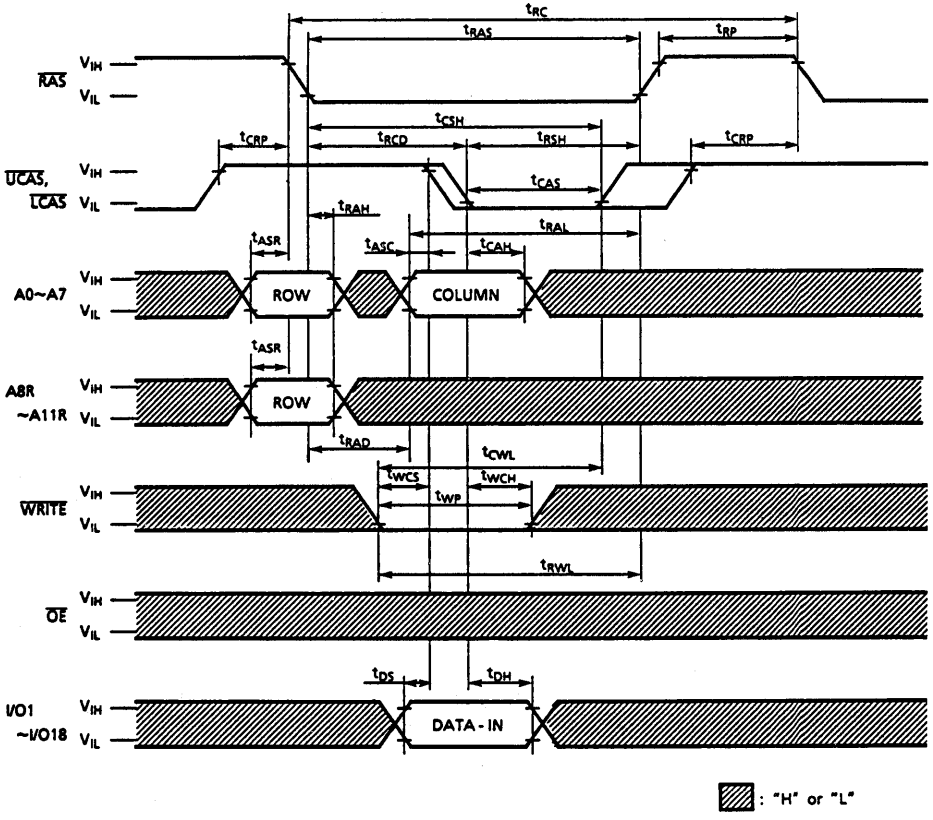
LOWER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O9) = OPEN
D_{IN} (I/O10~I/O18) = Don't Care

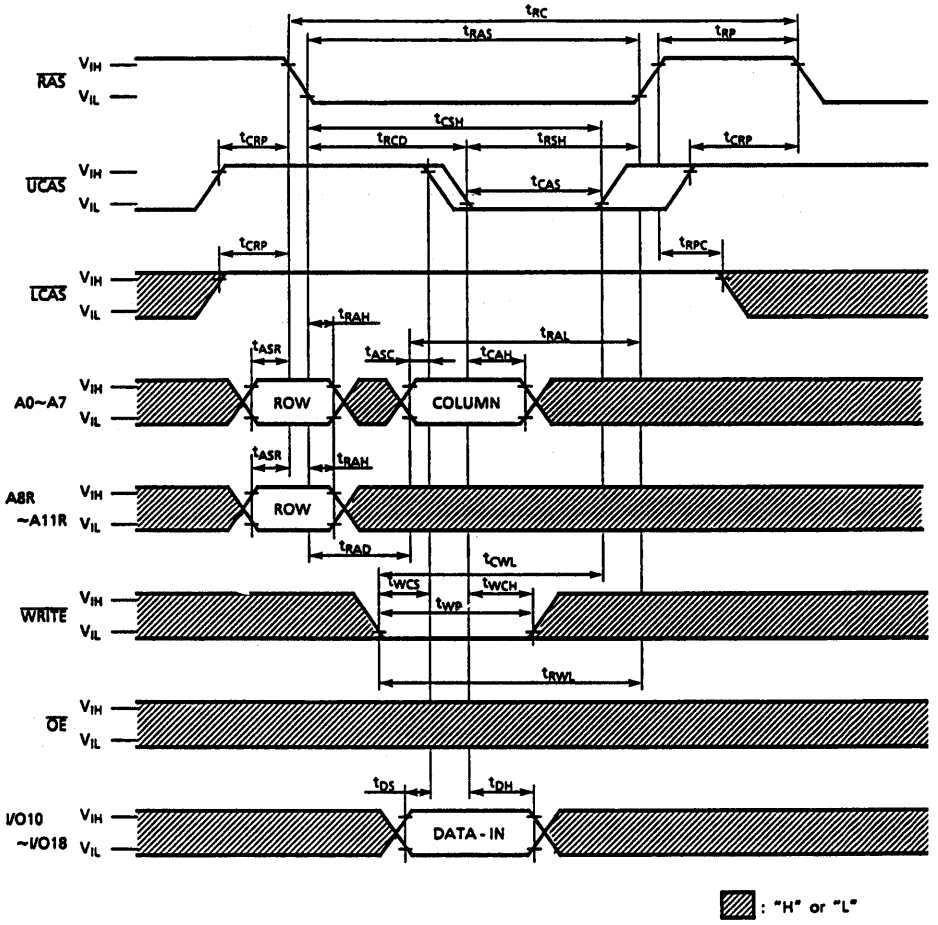
▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE)



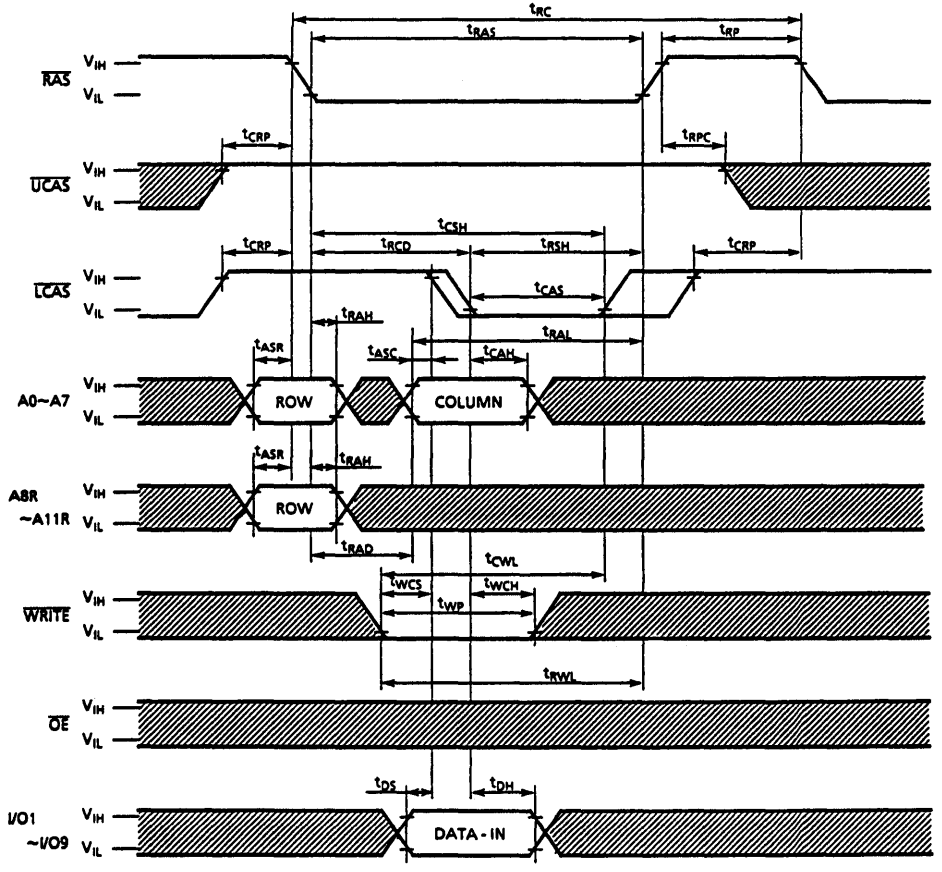
Note: D_{OUT} = OPEN

UPPER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{IN} (I/O1~I/O9) = Don't Care
D_{OUT} = OPEN

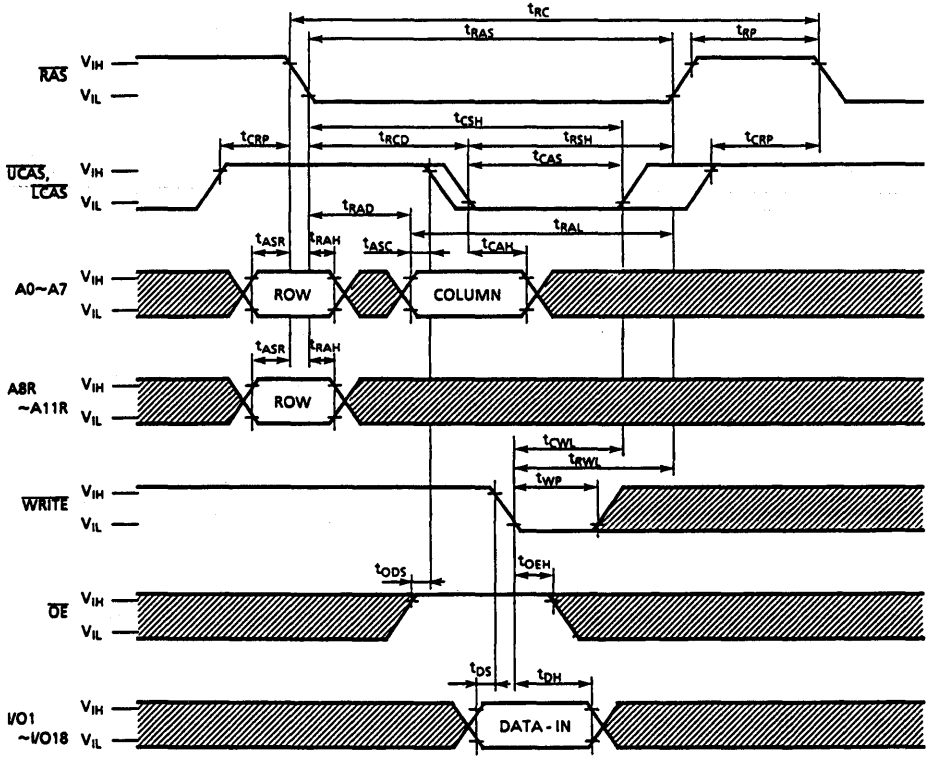
LOWER BYTE WRITE CYCLE (EARLY WRITE)



▨ : "H" or "L"

Note: D_{IN} (I/O10~I/O18) = Don't Care
D_{OUT} = OPEN

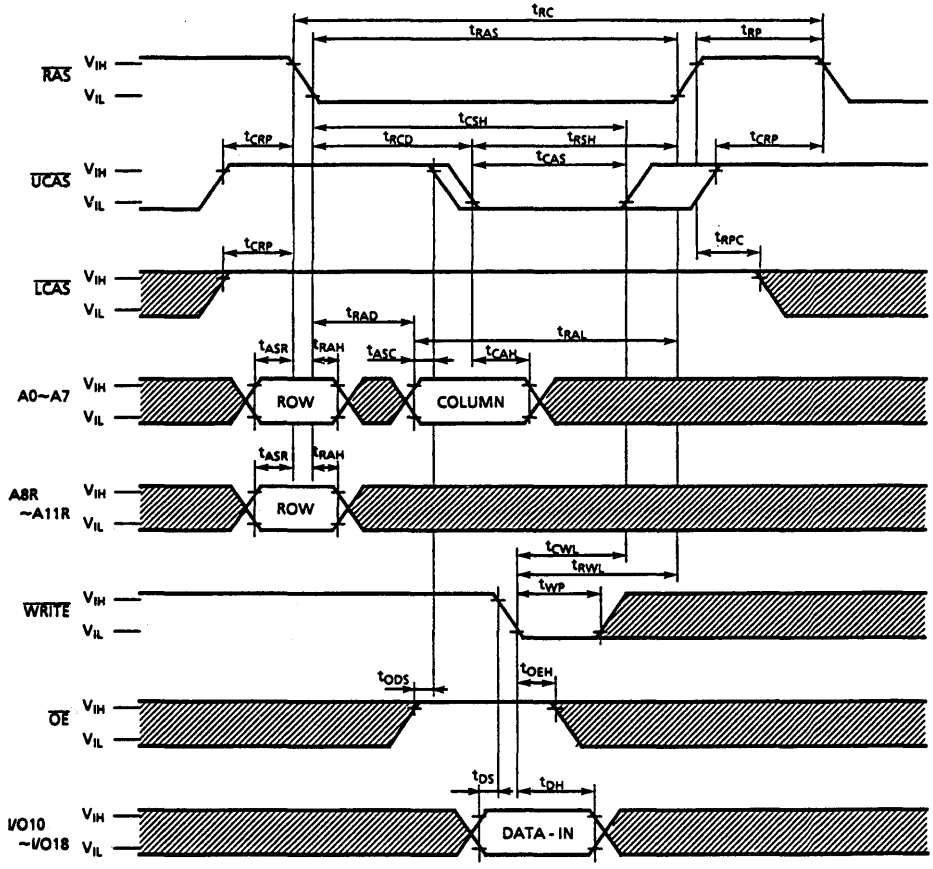
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

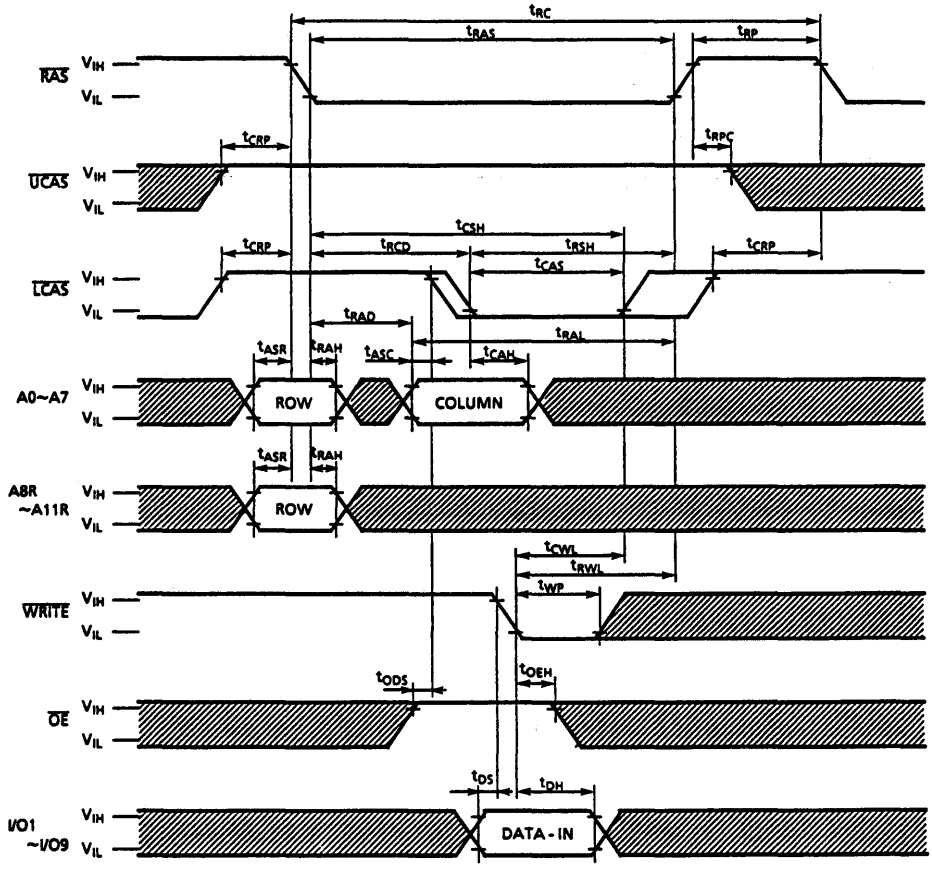
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{IN} (I/O1~I/O9) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

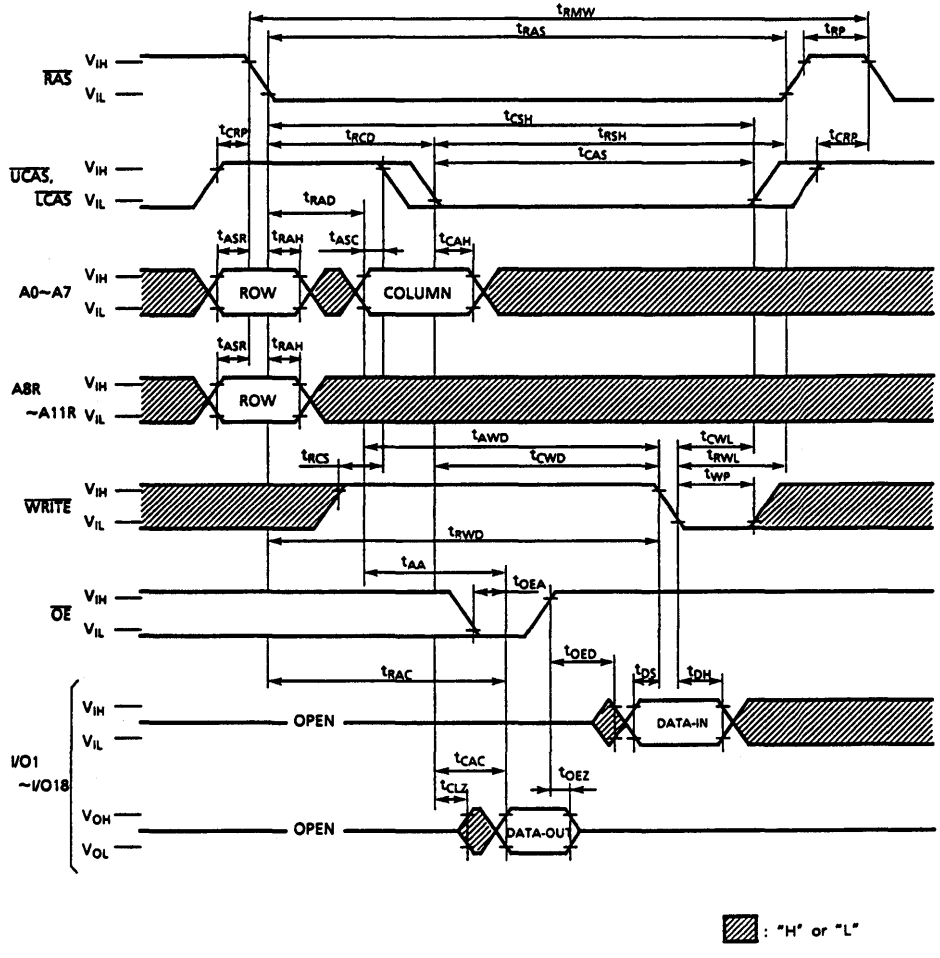
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



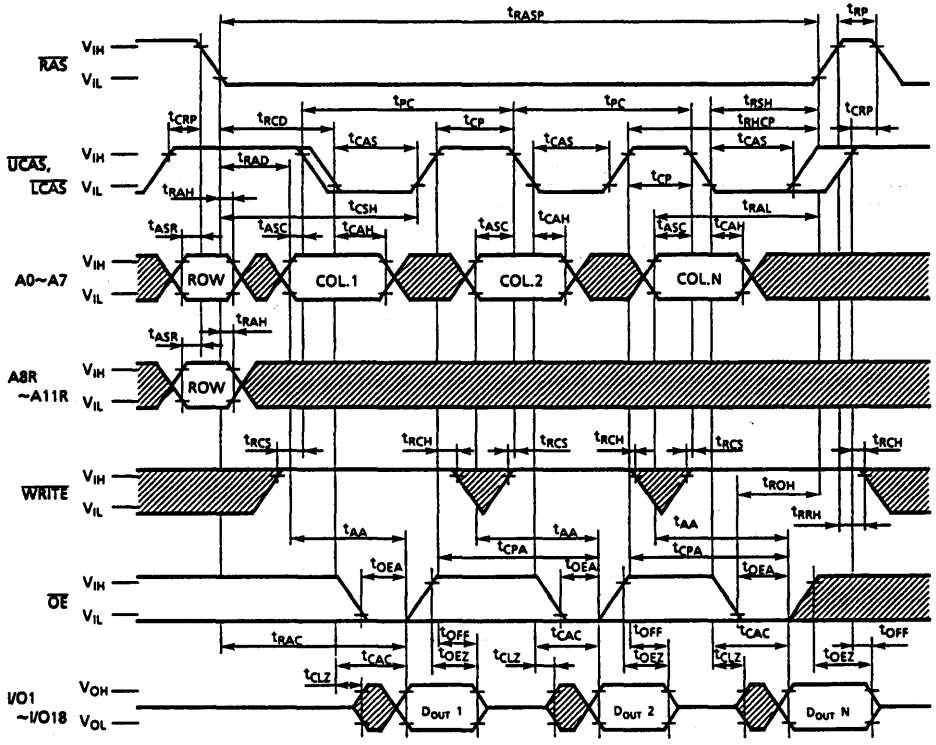
Note: D_{IN} (I/O10~I/O18) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



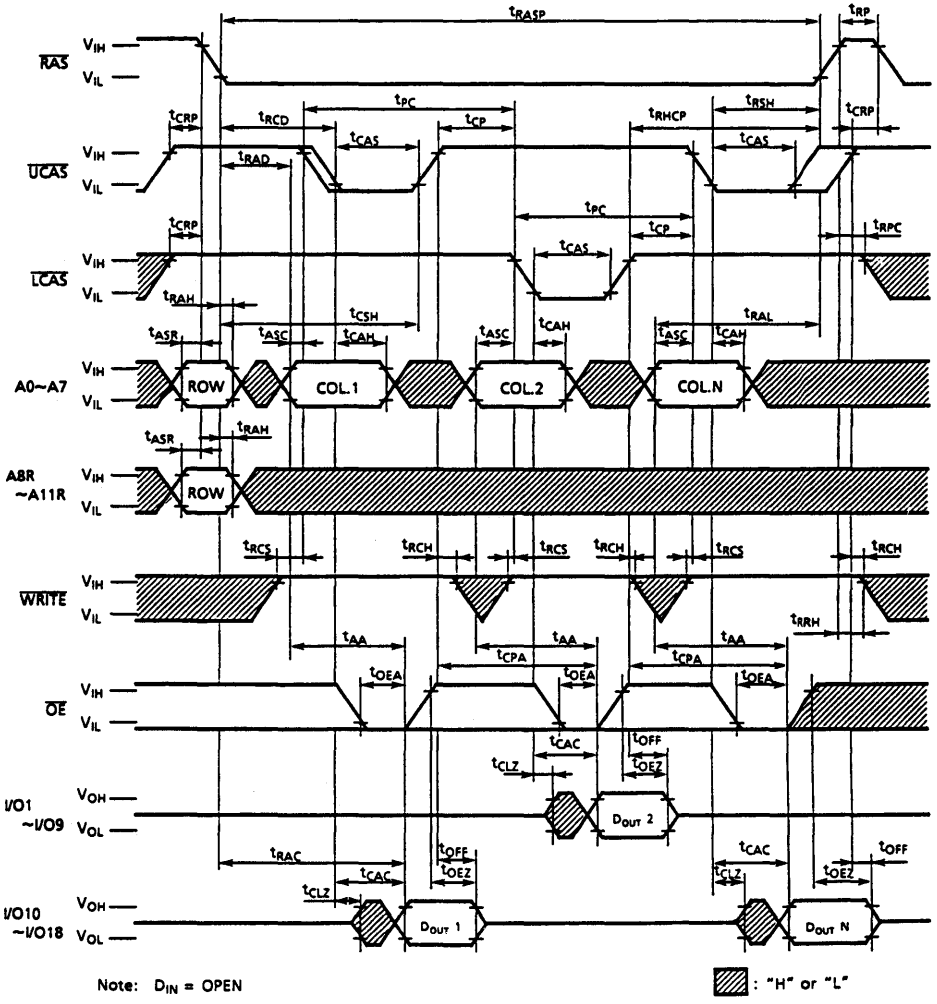
FAST PAGE MODE READ CYCLE



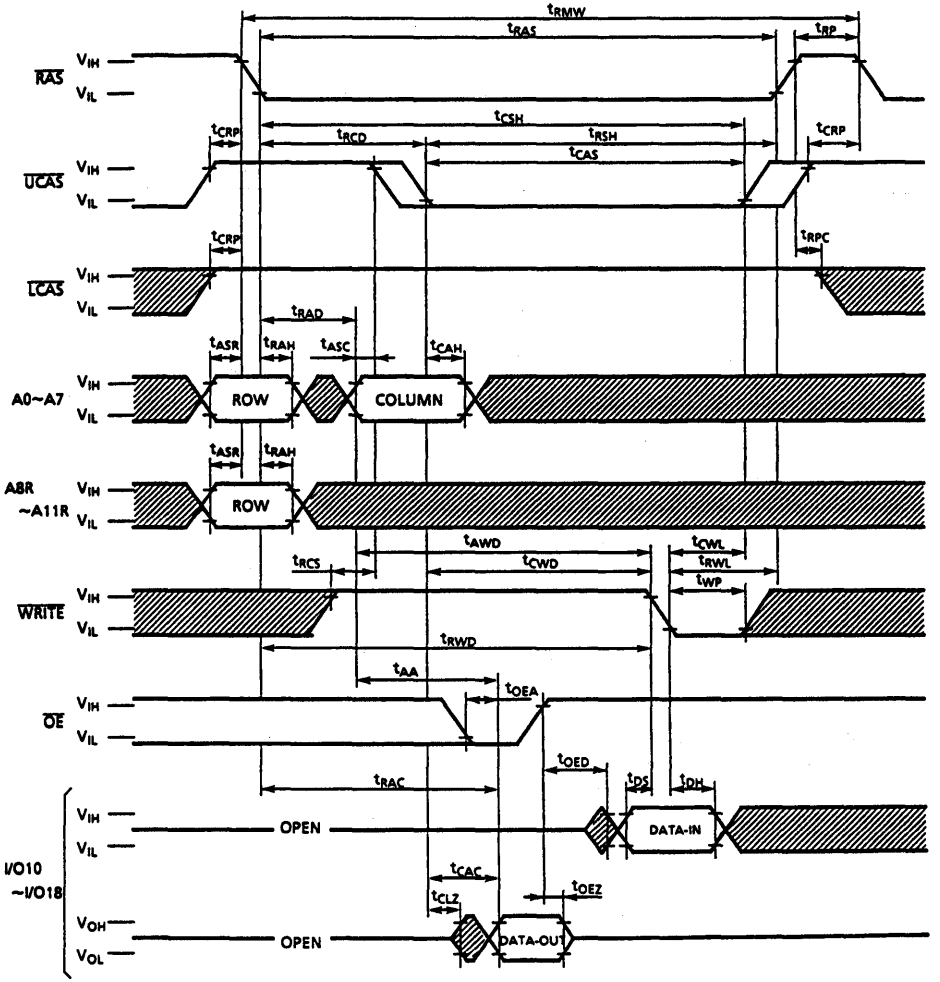
Note: D_{IN} = OPEN

▨ : "H" or "L"

FAST PAGE MODE BYTE READ CYCLE

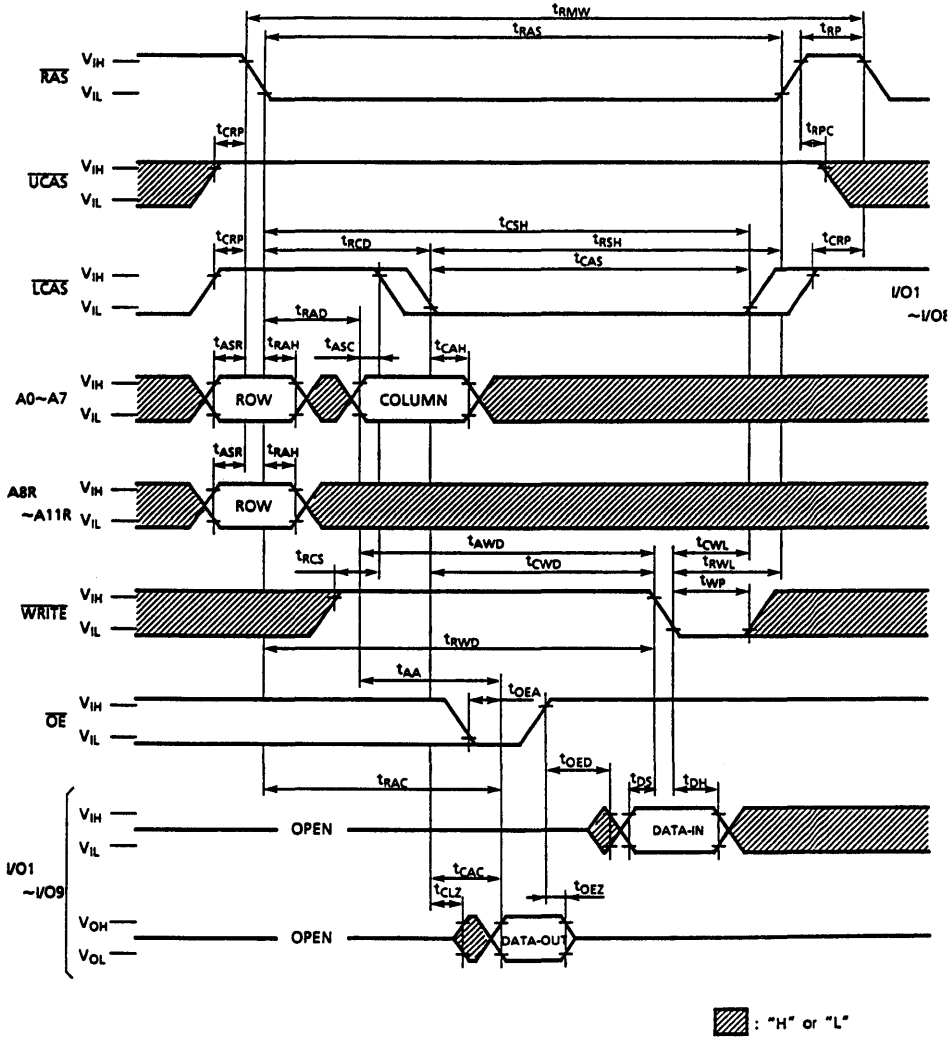


UPPER BYTE READ-MODIFY-WRITE CYCLE



Note: D_{IN} (I/O1~I/O9) = Don't Care
D_{OUT} (I/O1~I/O9) = OPEN

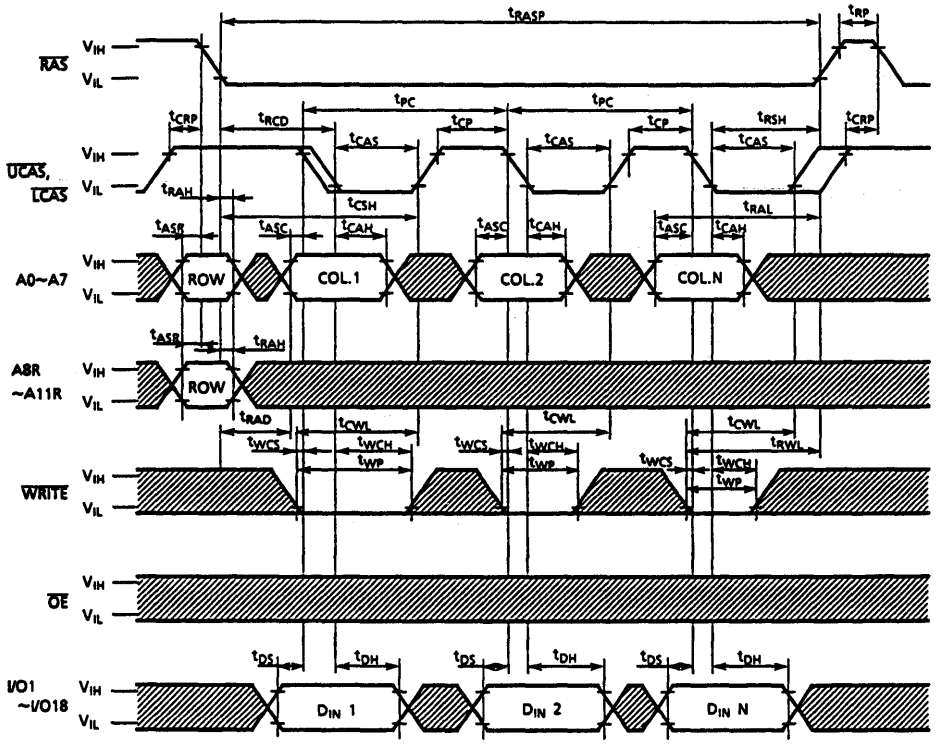
LOWER BYTE READ-MODIFY-WRITE CYCLE



: "H" or "L"

Note: D_{IN} (I/O10~I/O18) = Don't Care
D_{OUT} (I/O10~I/O18) = OPEN

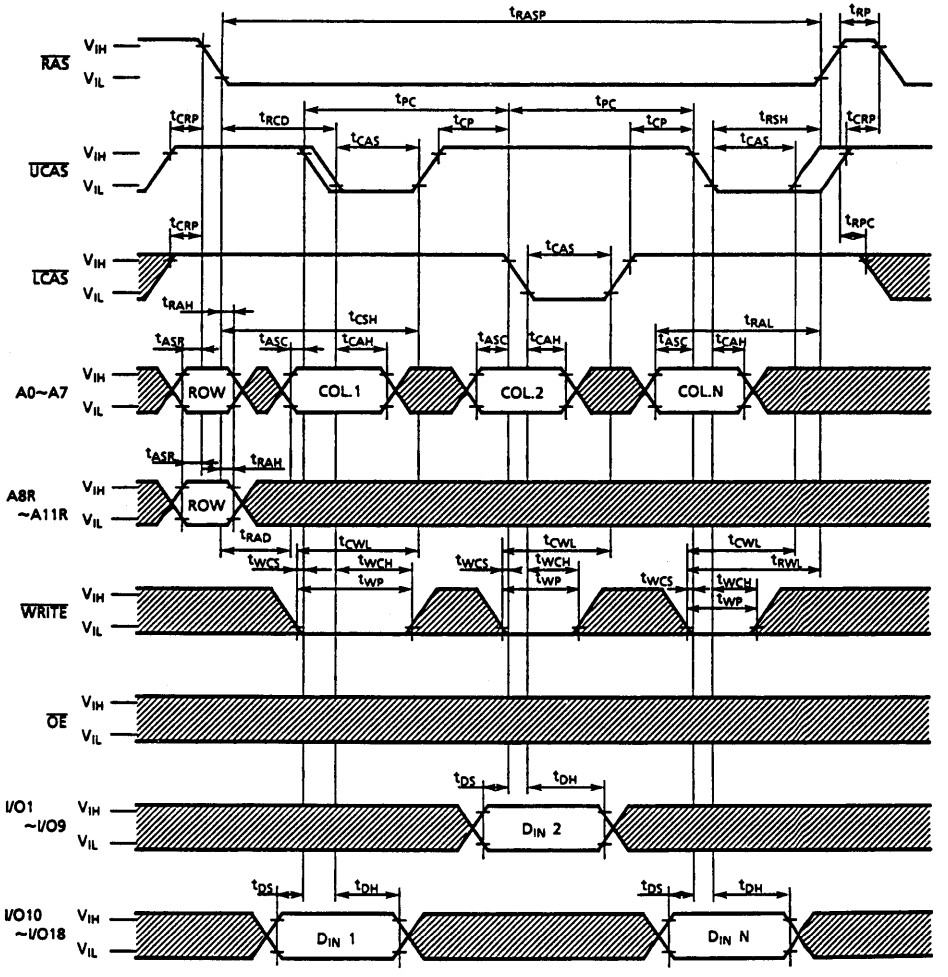
FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨: "H" or "L"

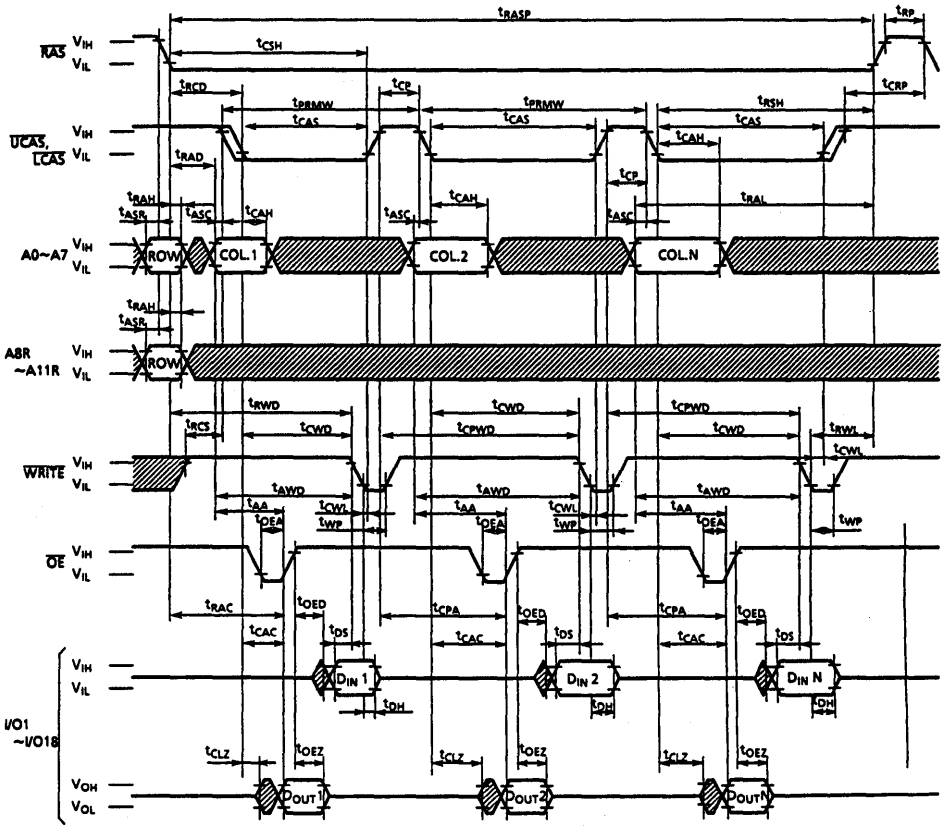
FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



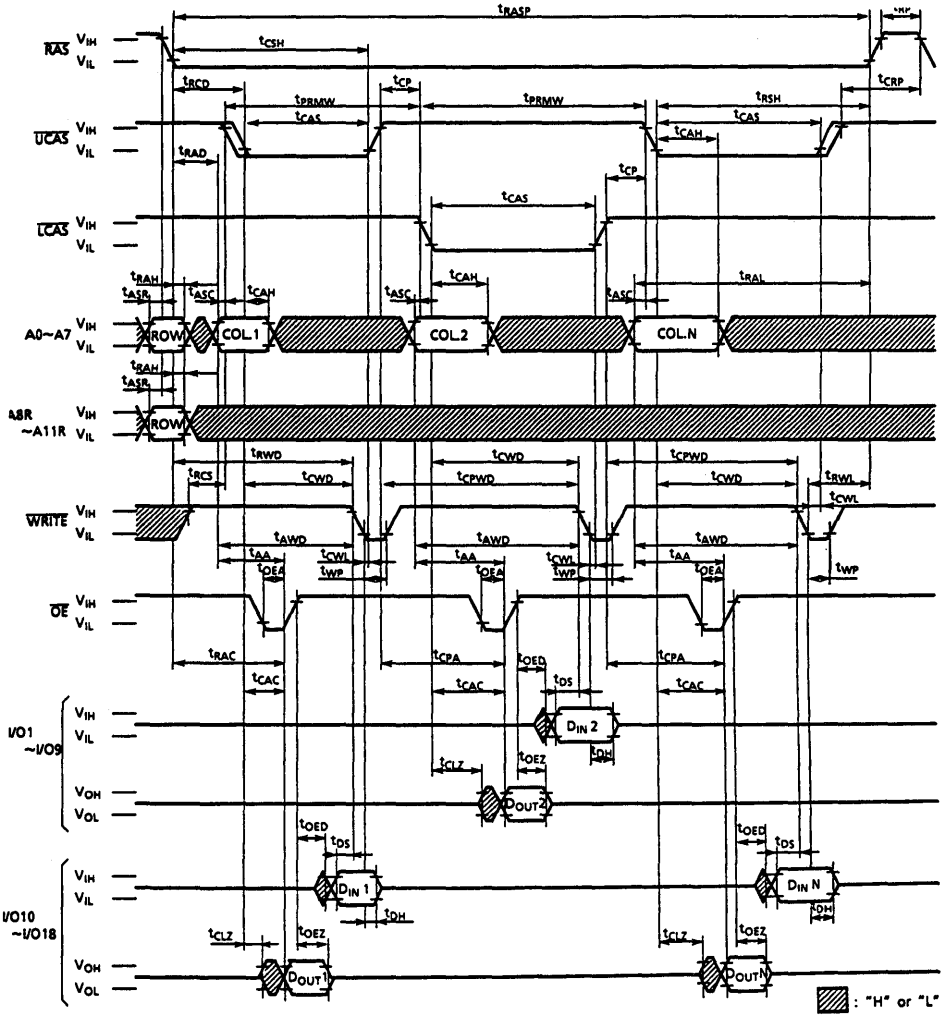
Note: D_{OUT} = OPEN

▨ : "H" or "L"

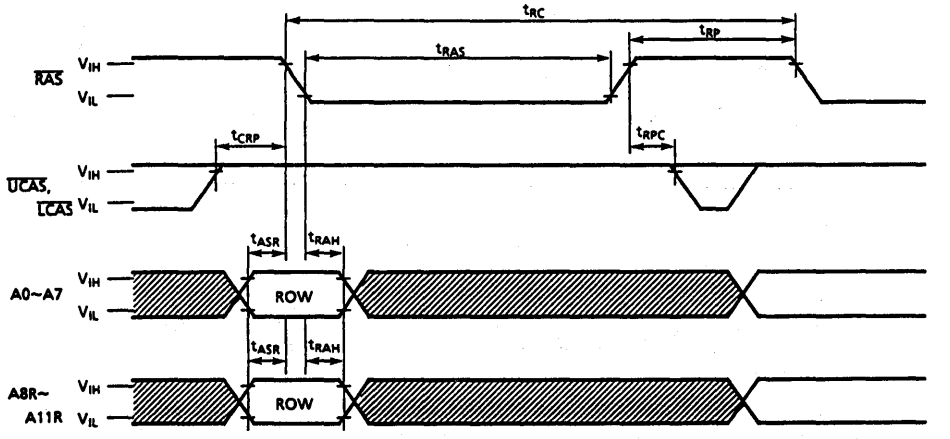
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE



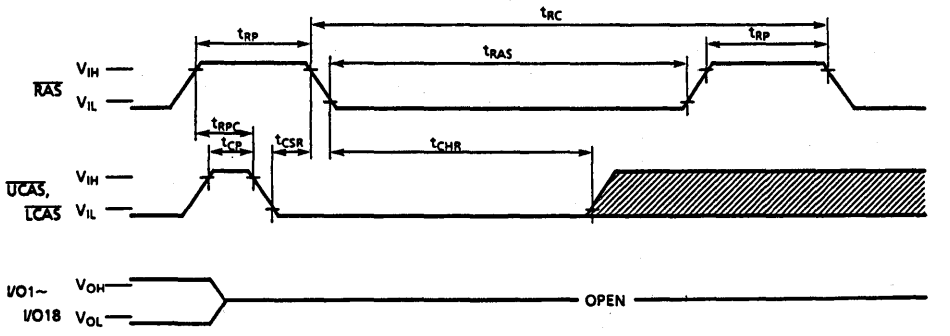
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"
D_{IN} = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

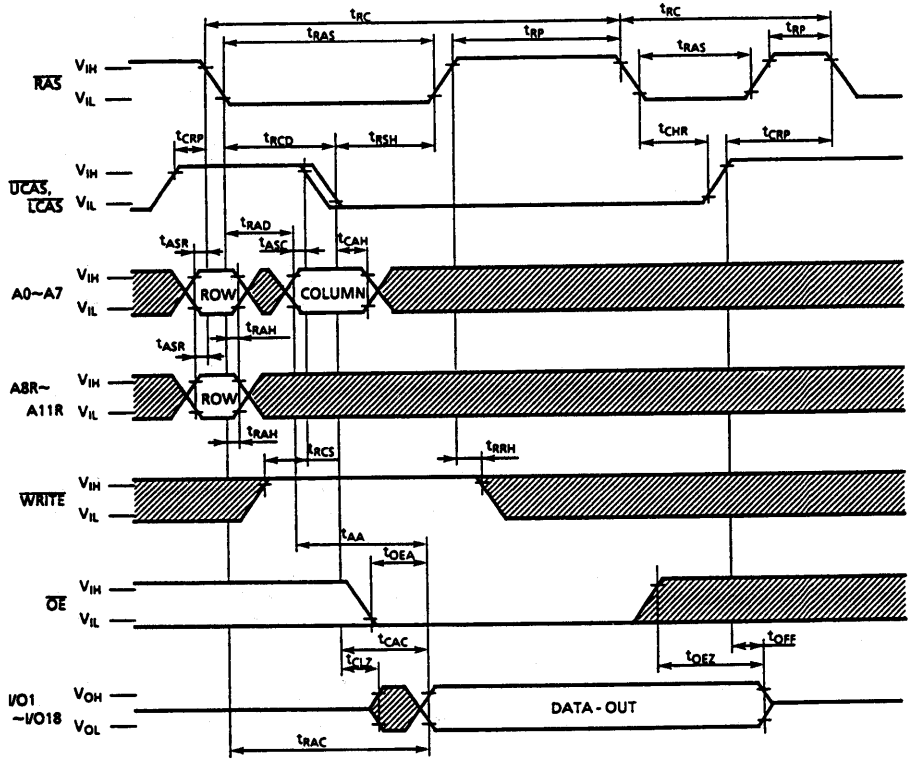
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



▨ : "H" or "L"

Note: $\overline{WRITE}$, $\overline{OE}$, A0~A7, A8R~A11R = "H" or "L"
D_{IN} = Don't Care
$\overline{CAS}$ before $\overline{RAS}$ refresh is performed when either $\overline{UCAS}$ or $\overline{LCAS}$ meets this timing.

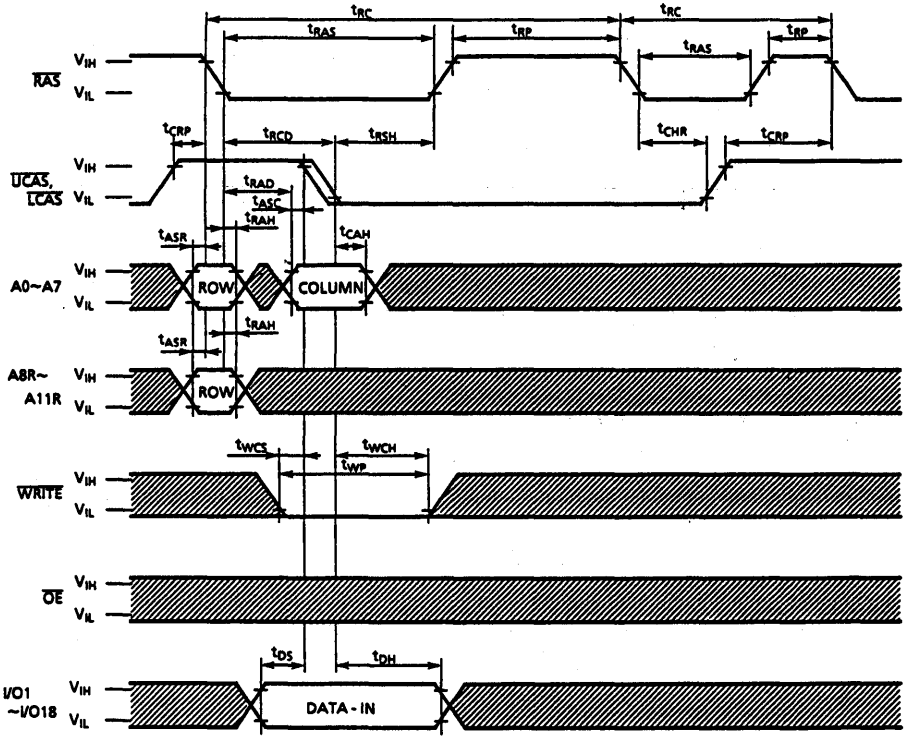
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨ : "H" or "L"

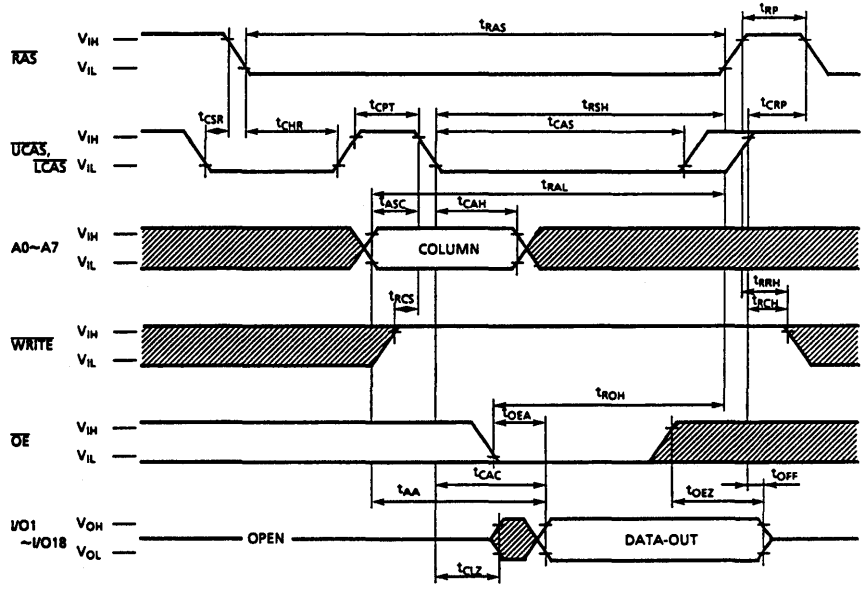
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

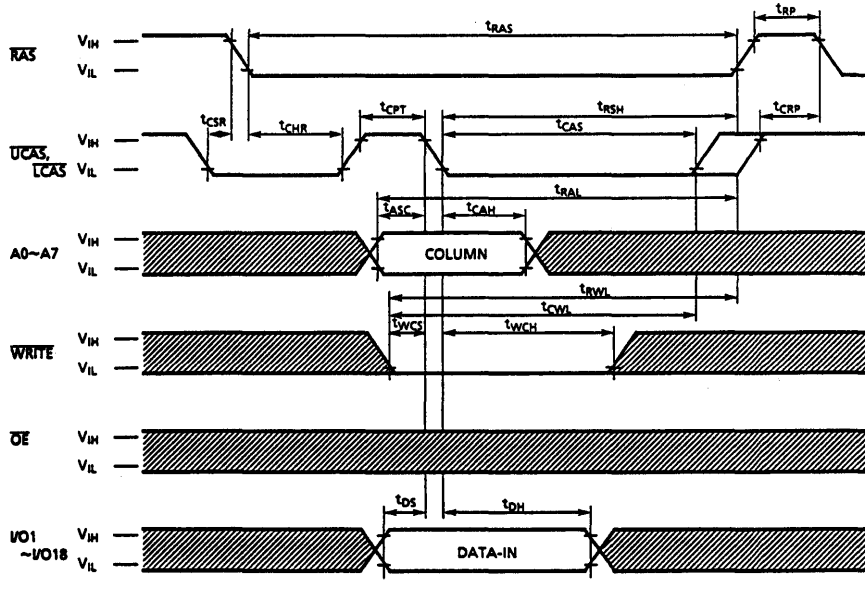
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



Note: A8R~A11R = "H" or "L"
D_{IN} = OPEN

▨ : "H" or "L"

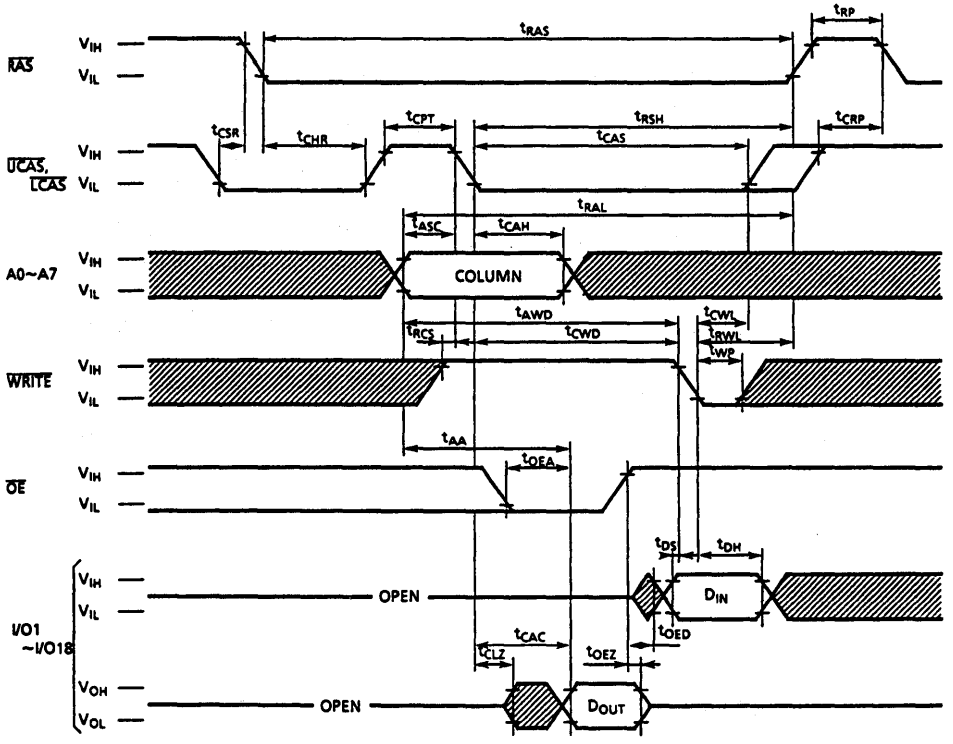
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



Note: A8R~A11R = "H" or "L"
D_{OUT} = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE

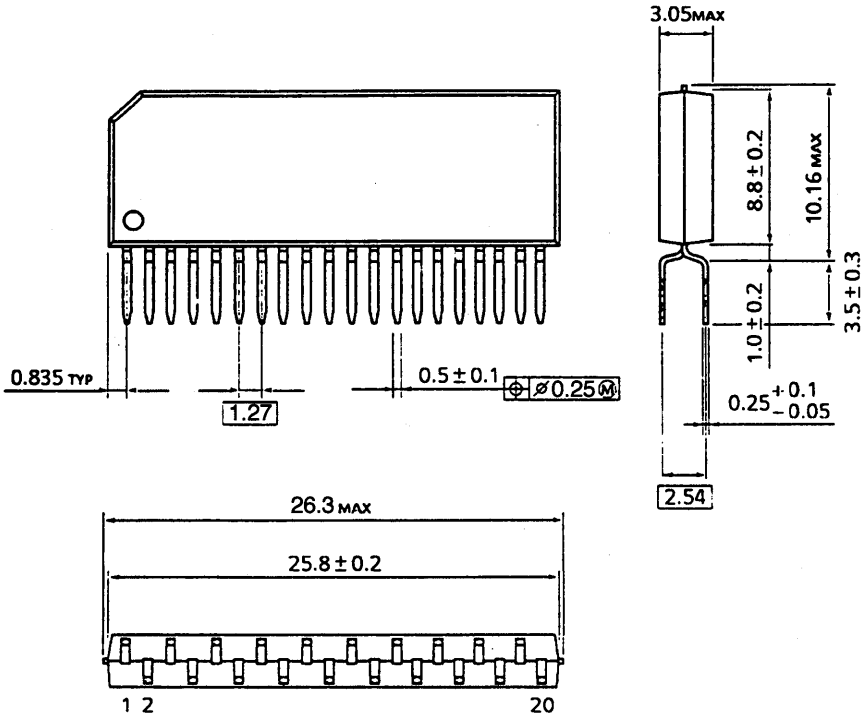


Note: A8R~A11R = "H" or "L"

▨ : "H" or "L"

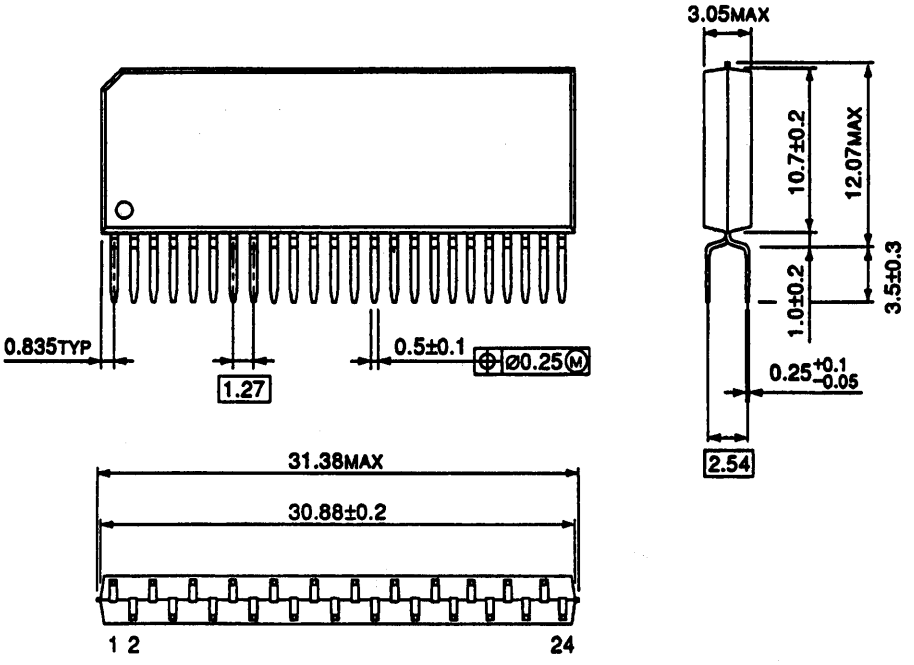
OUTLINE DRAWINGS (ZIP20 - P - 400A)

Unit in mm



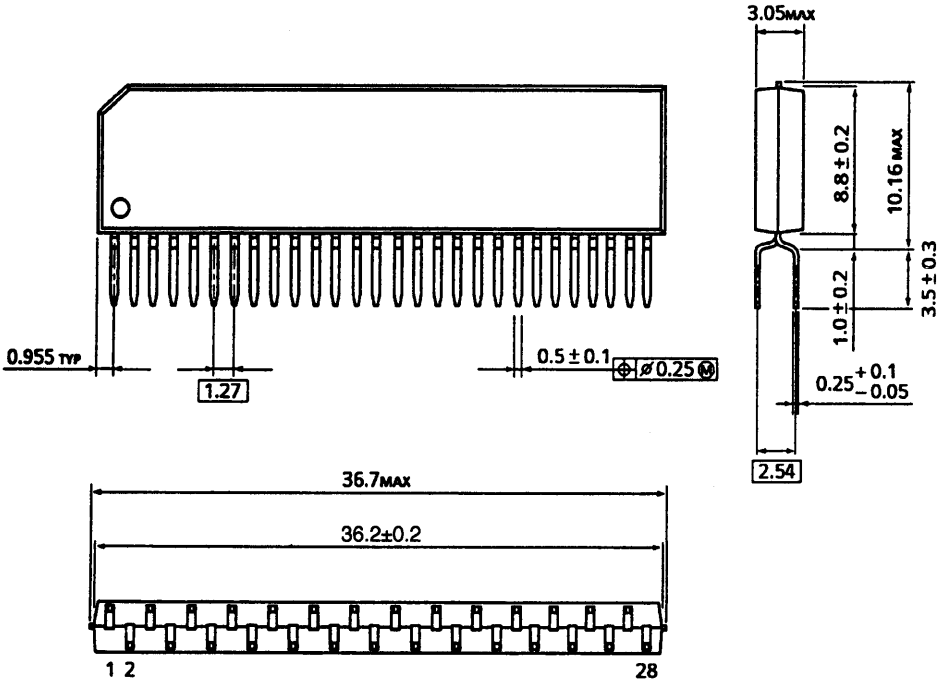
OUTLINE DRAWINGS (ZIP24 - P - 475)

Unit in mm



OUTLINE DRAWINGS (ZIP28 - P - 400)

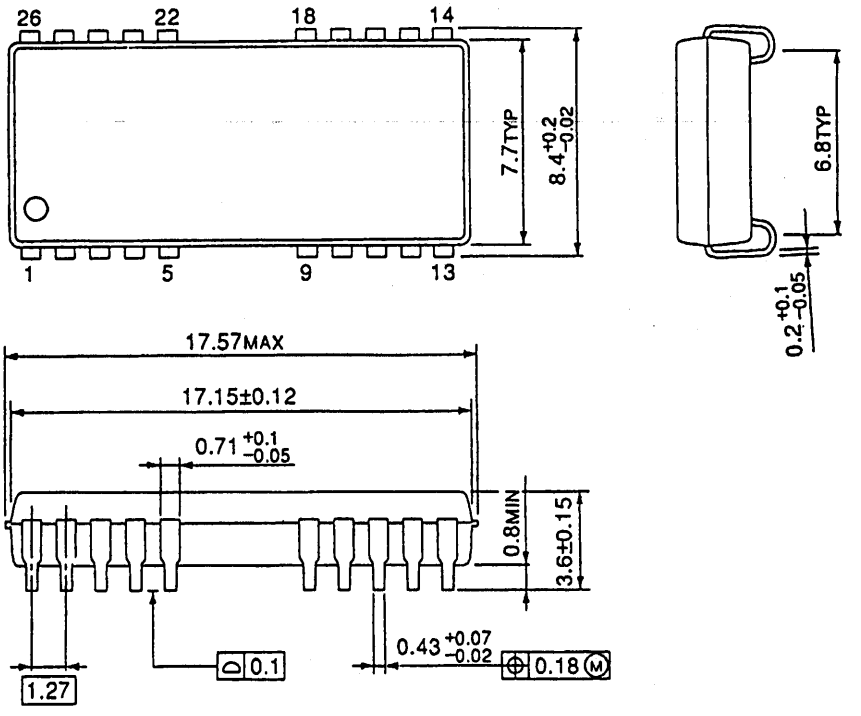
Unit in mm



Weight : 2.04g(TYP.)

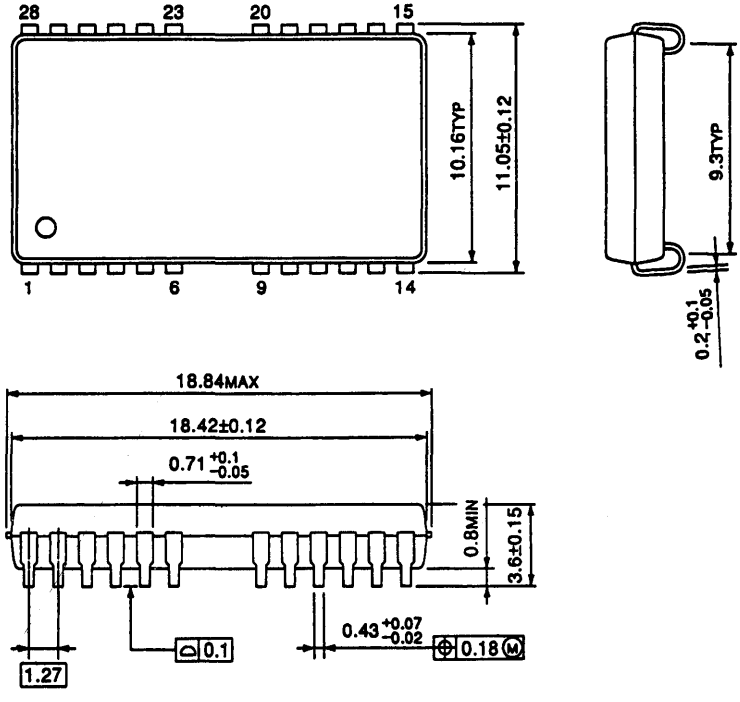
OUTLINE DRAWINGS (SOJ26 - P - 300A)

Unit in mm



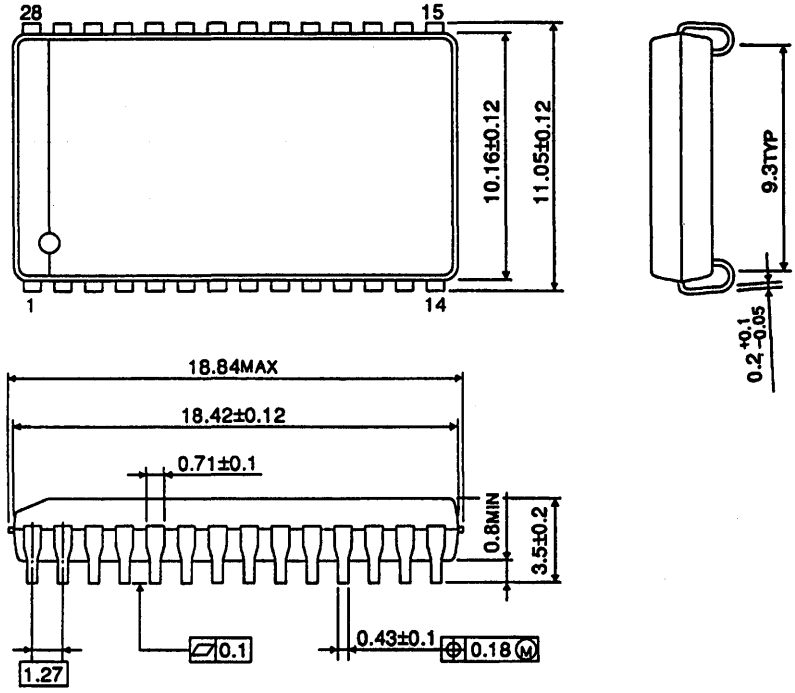
OUTLINE DRAWINGS (SOJ28 - P - 400A)

Unit in mm



OUTLINE DRAWINGS (SOJ28 - P - 400)

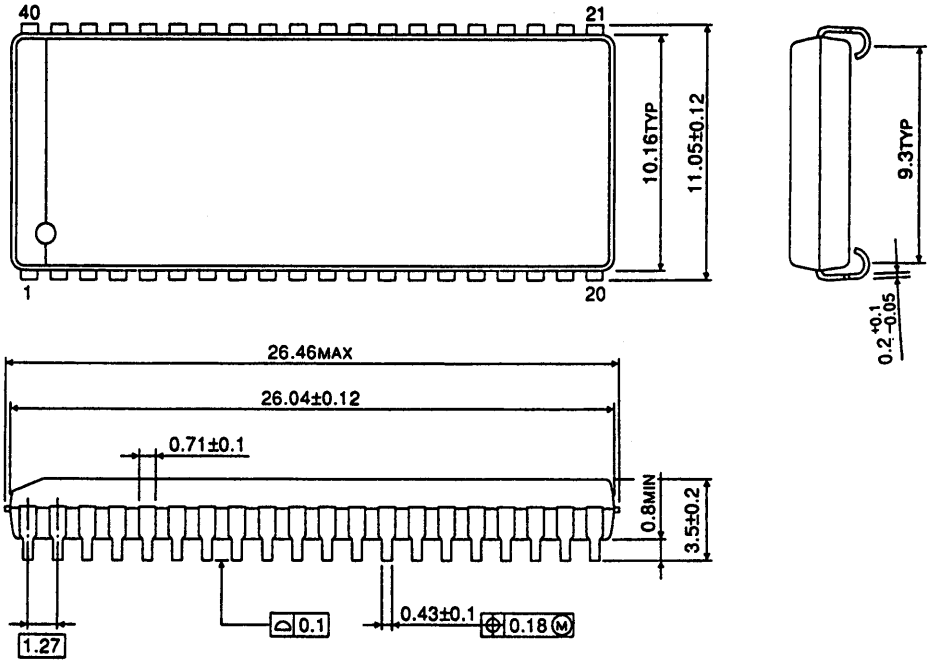
Unit in mm



Weight : 1.12g(TYP.)

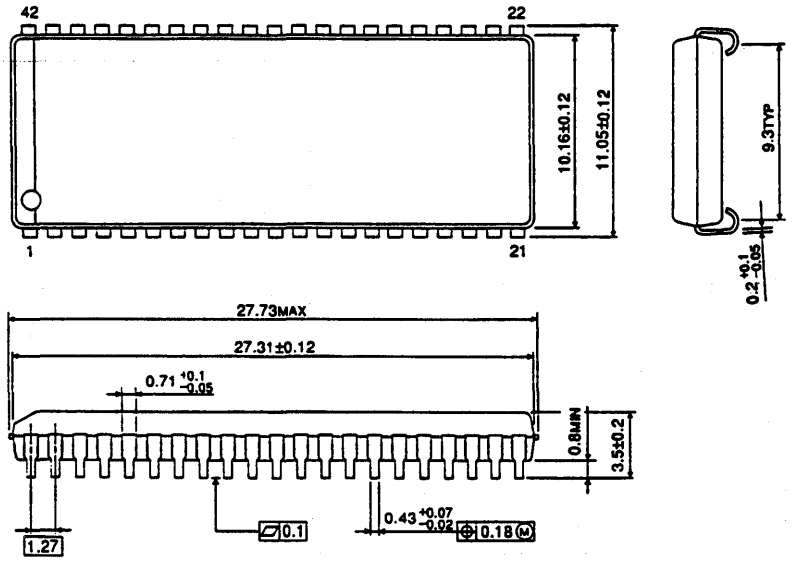
OUTLINE DRAWINGS (SOJ40 - P - 400)

Unit in mm



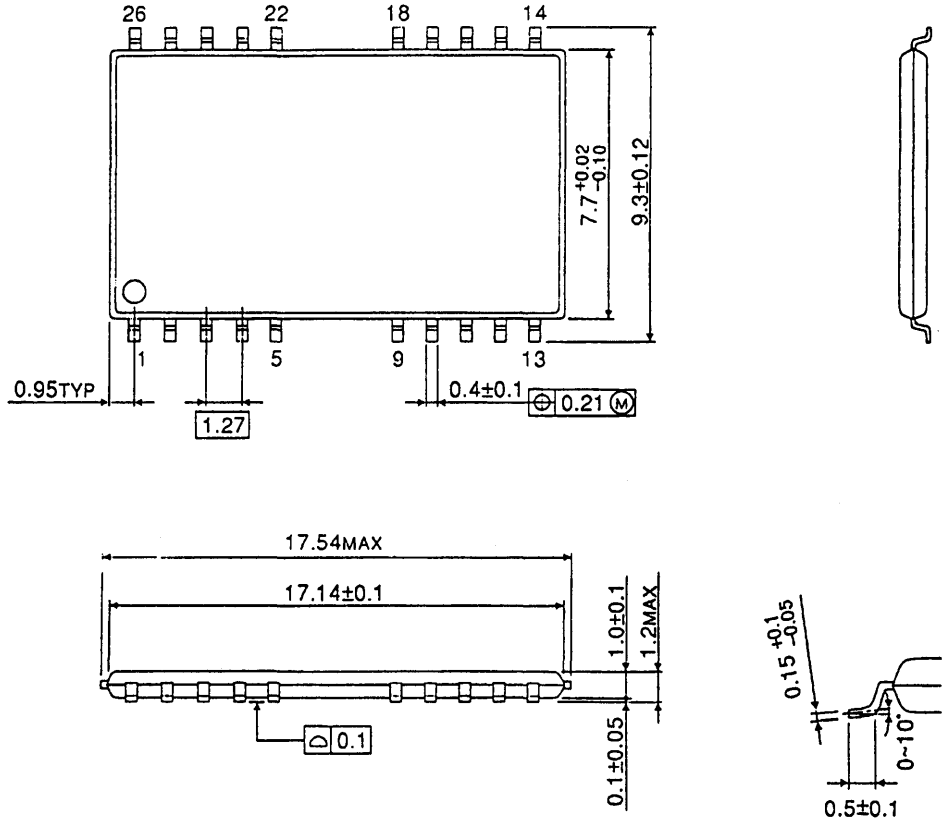
OUTLINE DRAWINGS (SOJ42 - P - 400)

Unit in mm



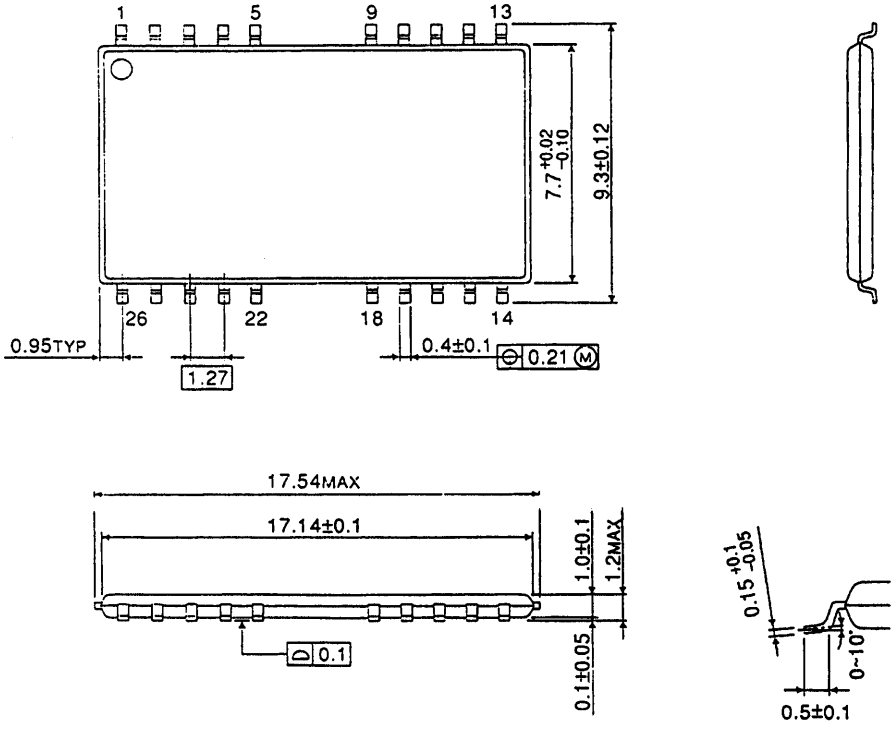
OUTLINE DRAWINGS (TSOP26 - P - 300)

Unit in mm



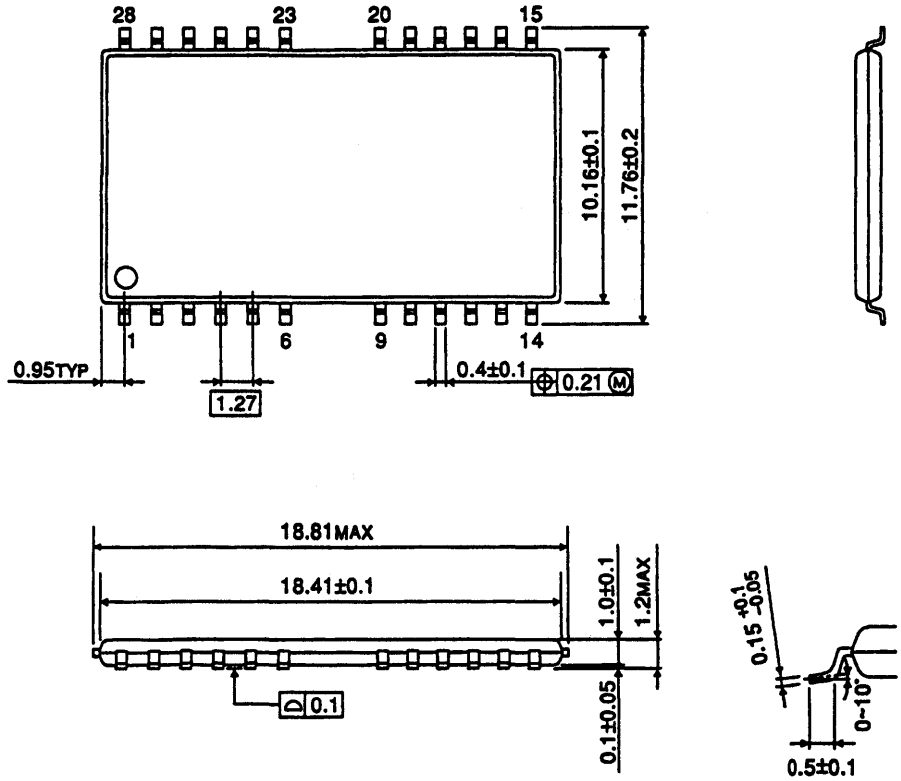
OUTLINE DRAWINGS (TSOP26 - P - 300A)

Unit in mm



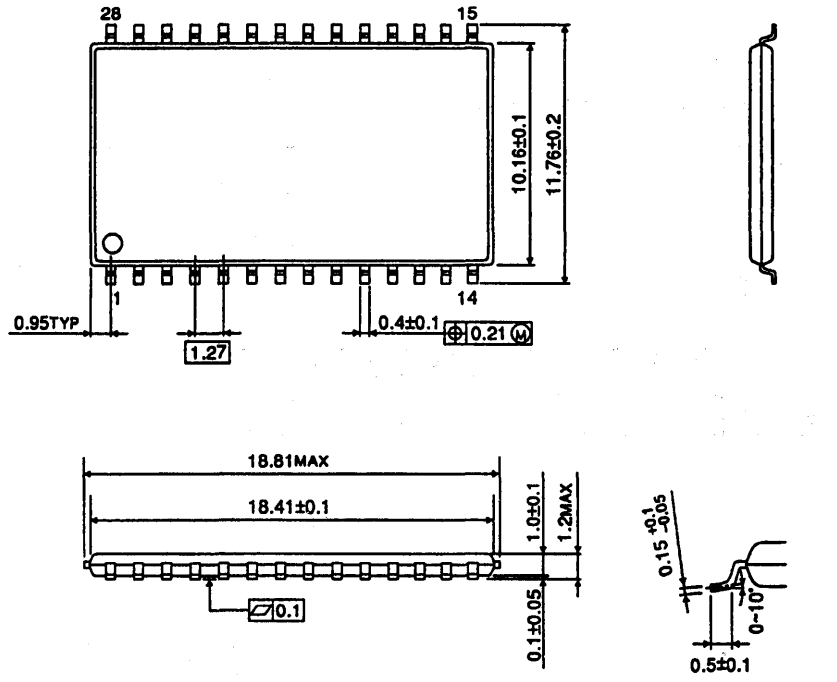
OUTLINE DRAWINGS (TSOP28 - P - 400B)

Unit in mm



OUTLINE DRAWINGS (TSOP28 - P - 400)

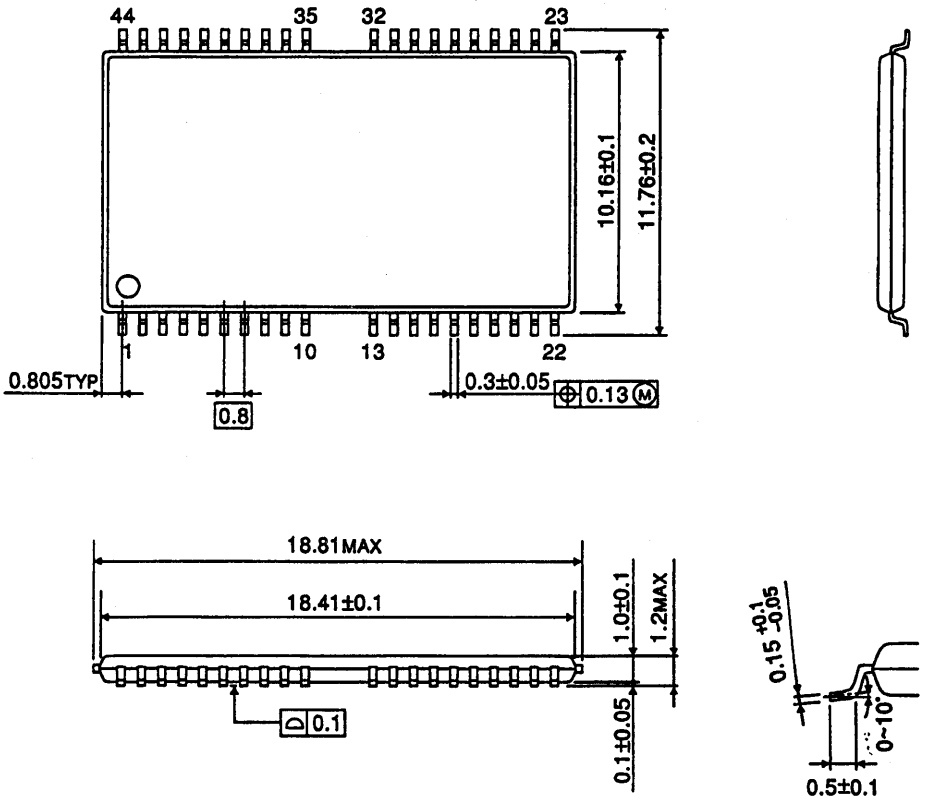
Unit in mm



Weight : 0.49g(TYP.)

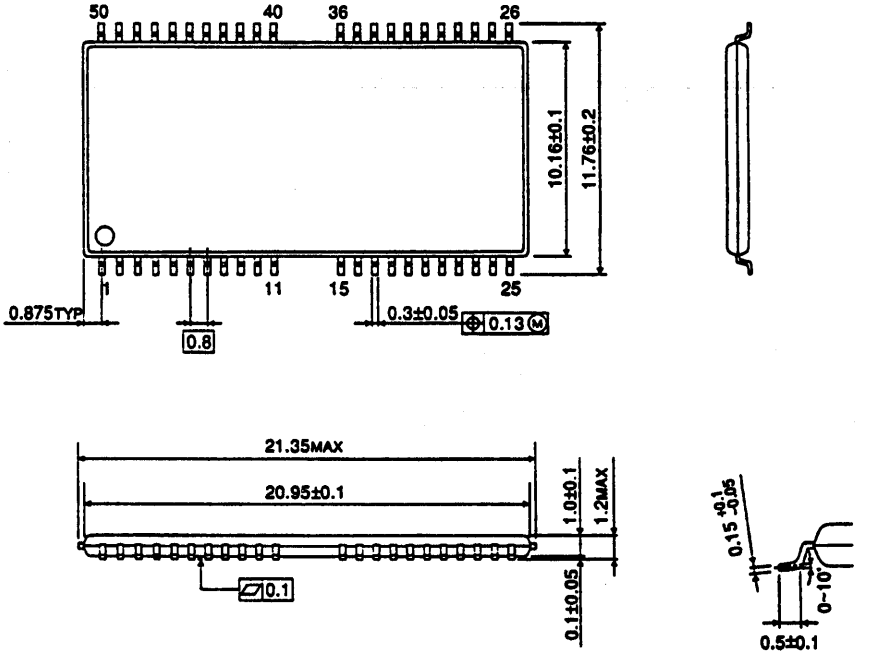
OUTLINE DRAWINGS (TSOP44 - P - 400B)

Unit in mm



OUTLINE DRAWINGS (TSOP50 - P - 400)

Unit in mm



1,048,576 WORD X 32 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM321000A is a 1,048,576 word by 32 bit dynamic RAM module which is assembled with eight TC514400ASJ devices on the printed circuit board. This module can be used as well as 2,097,152 word by 16 bit by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ·····, DQ15 and DQ31, respectively. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 1,048,576 word by 32 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  5,280mW MAX. Operating (THMxxxxxx-60)
  4,4009mW MAX. Operating (THMxxxxxx-70)
  3,744mW MAX. Operating (THMxxxxxx-80)
  44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 Refresh cycles/16ms
- Package
  72pin SIMM Tin-Lead Contact: THM321000AS-60,70,80
  72pin SIMM Gold Contact: THM321000ASG-60,70,80

KEY PARAMETERS

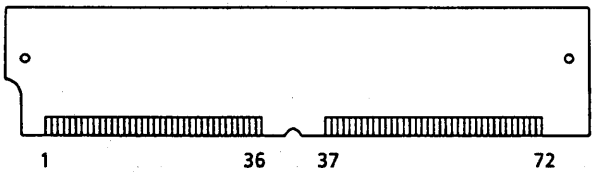
	-60	-70	-80
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA} Column Address Access Time	30ns	35ns	40ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC} Cycle Time	110ns	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ31	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$,$\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

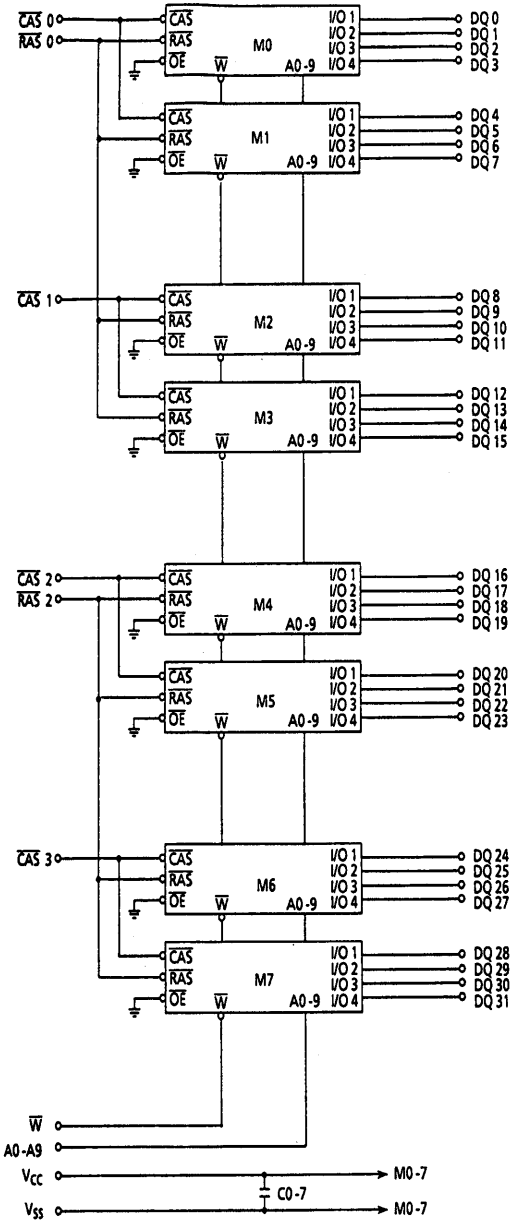
	-60	-70	-80
PD0	V_{SS}	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	NC	V_{SS}	NC
PD3	NC	NC	V_{SS}

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	4_0	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD1
9	DQ19	21	DQ20	33	NC	45	NC	57	DQ12	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD3
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	5.6	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	960	mA	3,4 5
		THMxxxxxx-70	-	800		
		THMxxxxxx-80		680		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	960	mA	3,5
		THMxxxxxx-70	-	800		
		THMxxxxxx-80		680		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	560	mA	3,4 5
		THMxxxxxx-70	-	560		
		THMxxxxxx-80		480		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	960	mA	3,5
		THMxxxxxx-70	-	800		
		THMxxxxxx-80		680		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-80	80	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

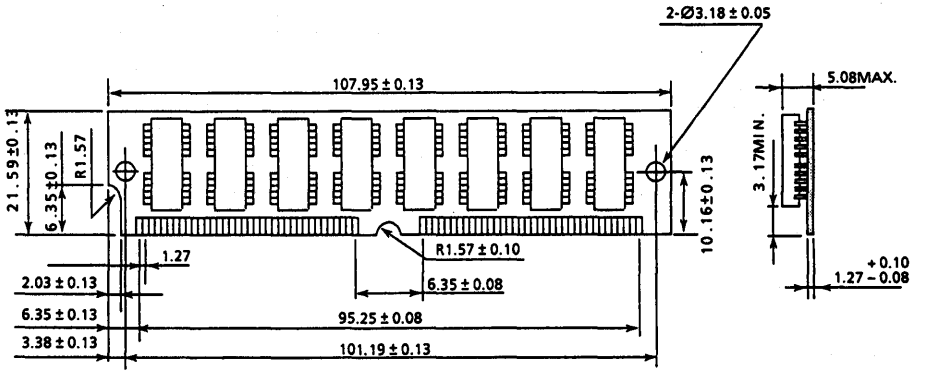
Please refer to the DRAM Module A.C. Conditions No. 8. Notes which are referenced in this section are also located in the A.C. Conditions.

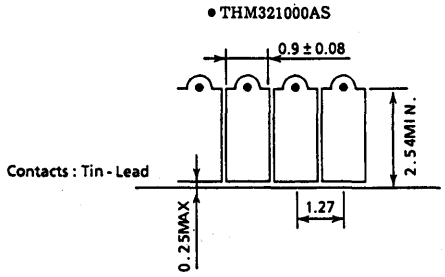
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

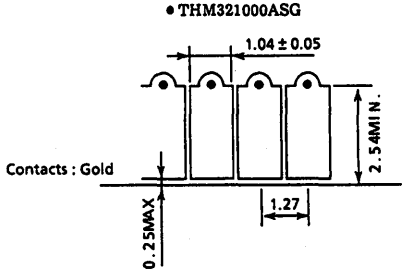
SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9)	-	60	pF
CI2	Input Capacitance ($\overline{W}$)	-	45	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	-	35	pF
CI4	Input Capacitance ($\overline{CAS0}$, $\overline{CAS3}$)	-	30	pF
CDQ1	I/O Capacitance (DQ0~31)	-	17	pF

OUTLINE DRAWINGS

Unit in mm







1,048,576 WORD X 32 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM3210B0A is a 1,048,576 word by 32 bit dynamic RAM module which is assembled with two TC5118160AJ devices on the printed circuit board. This module can be as well used as 2,097,152 word by 16 bit by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ·····, DQ15 and DQ31, respectively. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 1,048,576 word by 32 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  1,540mW MAX. Operating (THMxxxxxx-70)
  1,320mW MAX. Operating (THMxxxxxx-80)
  11mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 Refresh cycles/16ms
- Package
  72pin SIMM Tin-Lead Contact: THM3210B0AS-xx
  72pin SIMM Gold Contact: THM3210B0ASG-xx

KEY PARAMETERS

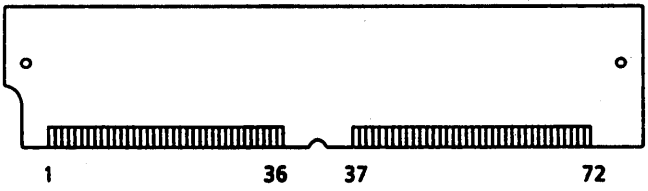
	-70	-80
t_{RAC} $\overline{RAS}$ Access Time	70ns	80ns
t_{AA} Column Address Access Time	35ns	40ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns
t_{RC} Cycle Time	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	50ns

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ31	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

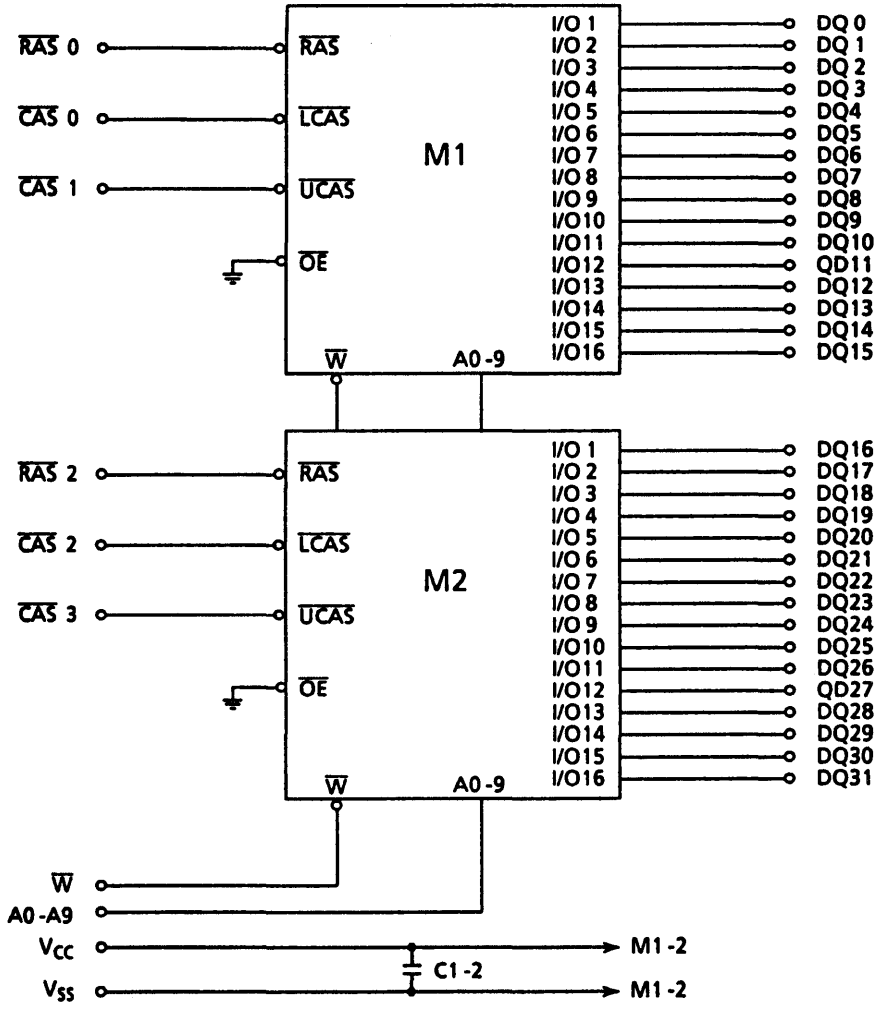
	-70	-80
PD0	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	NC
PD3	NC	V_{SS}

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	4_0	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD1
9	DQ19	21	DQ20	33	NC	45	NC	57	DQ12	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD3
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7.0$	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	1.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	$V_{CC} + 0.5$*	V	2
V_{IL}	Input Low Voltage	-0.5**	-	0.8	V	2

*V_{CC} + 2.0V at pulse width ≤ 20 ns (pulse width measured at V_{CC})
**-2.0V at pulse width ≤ 20 ns (pulse width measured at 0V)

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	280	mA	3,4 5
		THMxxxxxx-80	-	240		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			4	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	280	mA	3,5
		THMxxxxxx-80	-	240		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-70	-	150	mA	3,4 5
		THMxxxxxx-80	-	130		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			2	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	280	mA	3,5
		THMxxxxxx-80	-	240		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-20	20	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 20. Notes which are referenced in this section are also located in the A.C. Conditions.

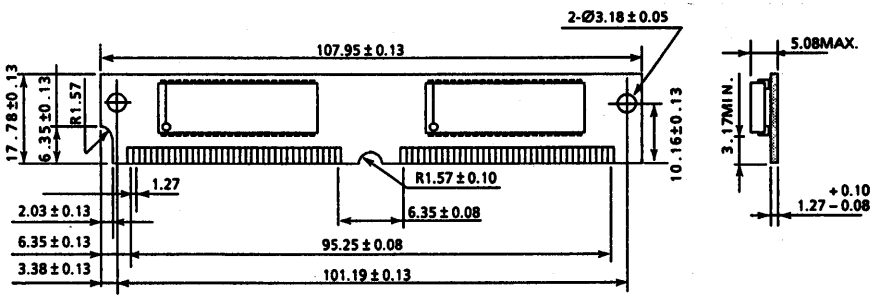
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9)	-	15	pF
CI2	Input Capacitance ($\overline{W}$)	-	19	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	-	12	pF
CI4	Input Capacitance ($\overline{CAS0}$ ~$\overline{CAS3}$)	-	12	pF
CDQ	I/O Capacitance (DQ0~31)	-	12	pF

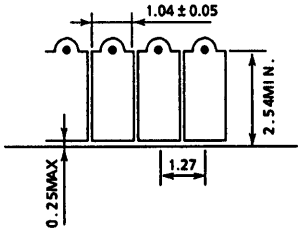
OUTLINE DRAWINGS

THM3210B0AS/ASG

Unit in mm



• THM3210B0AS/ASG



2,097, 152 WORD X 32 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM322020A is a 2,097,152 word by 32 bit dynamic RAM module which is assembled with 16 TC514400ASJ devices on the printed circuit board. This module can be used as well as 4,194,304 word by 16 bit by means of connecting DQ0 and DQ16, DQ1 and DQ17, ·····, DQ15 and DQ31, respectively. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 2,097,152 word by 32 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  5,368mW MAX. Operating (THMxxxxxx-60)
  4,488mW MAX. Operating (THMxxxxxx-70)
  3,832mW MAX. Operating (THMxxxxxx-80)
  88mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 Refresh cycles/16ms
- Package
  72pin SIMM Tin-Lead Contact: THM322020AS-60,70,80
  72pin SIMM Gold Contact: THM322020ASG-60,70,80

KEY PARAMETERS

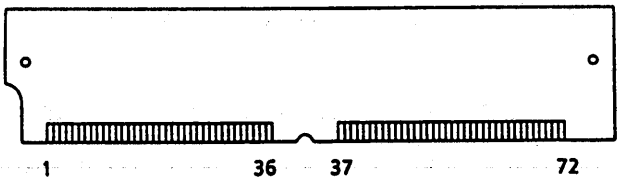
	-60	-70	-80
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA} Column Address Access Time	30ns	35ns	40ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC} Cycle Time	110ns	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ31	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

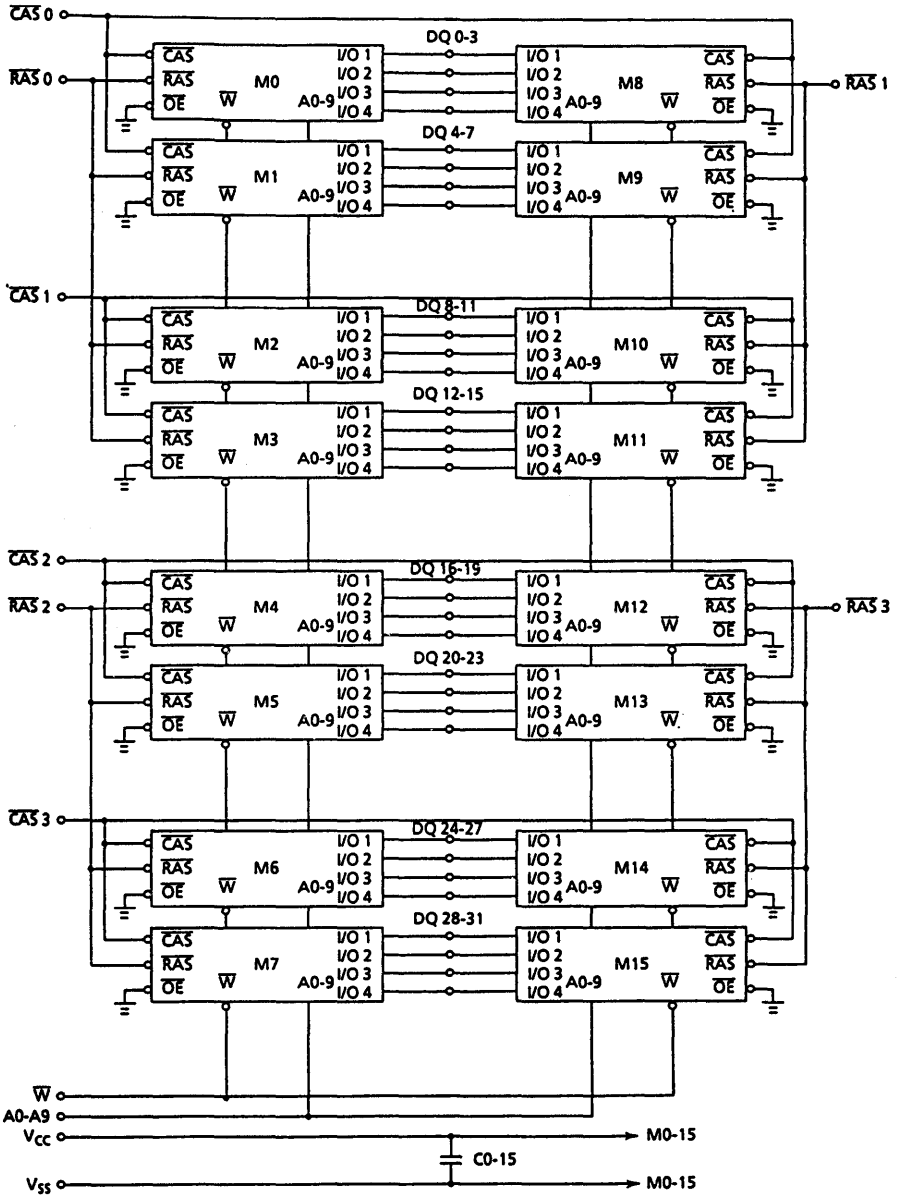
	-60	-70	-80
PD0	NC	NC	NC
PD1	NC	NC	NC
PD2	NC	V_{SS}	NC
PD3	NC	NC	V_{SS}

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	4_0	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD1
9	DQ19	21	DQ20	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ12	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD3
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	11.2	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	976	mA	3,4 5
		THMxxxxxx-70	-	816		
		THMxxxxxx-80	-	696		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			32	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	976	mA	3,5
		THMxxxxxx-70	-	816		
		THMxxxxxx-80	-	696		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	576	mA	3,4 5
		THMxxxxxx-70	-	576		
		THMxxxxxx-80	-	496		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			16	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	976	mA	3,5
		THMxxxxxx-70	-	816		
		THMxxxxxx-80	-	696		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-160	160	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 8. Notes which are referenced in this section are also located in the A.C. Conditions.

CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta=0~70°C)

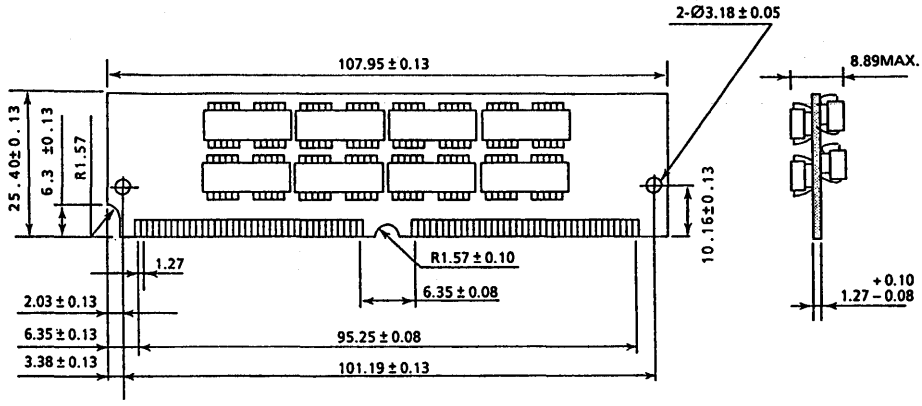
SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9)	-	100	pF
CI2	Input Capacitance ($\overline{W}$)	-	80	pF
CI3	Input Capacitance ($\overline{RAS0}$~$\overline{RAS3}$)	-	40	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	35	pF
CDQ1	I/O Capacitance (DQ0~31)	-	25	pF

OUTLINE DRAWINGS

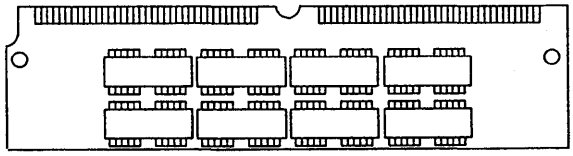
THM322020AS/ASG

FRONT SIDE

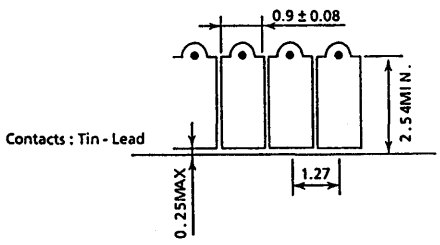
Unit in mm



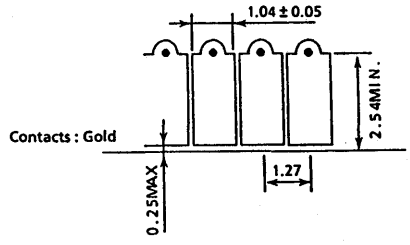
BACK SIDE



• THM322020AS



• THM322020ASG



2,097,152 WORD X 32 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM3220C0A is a 2,097,152 word by 32 bit dynamic RAM module which is assembled with 4 TC5118160AJ device on the printed circuit board. This module can be as well used as 4,194,304 word by 16 bit by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ·····, DQ15 and DQ31, respectively. THM3220C0A is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 2,097,152 word by 32 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  1,562mW MAX. Operating (THMxxxxxx-70)
  1,342mW MAX. Operating (THMxxxxxx-80)
  22mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 Refresh cycles/16ms
- Package
  Tin-Lead Contact: THM3220C0AS-xx
  Gold Contact: THM3220C0ASG-xx

KEY PARAMETERS

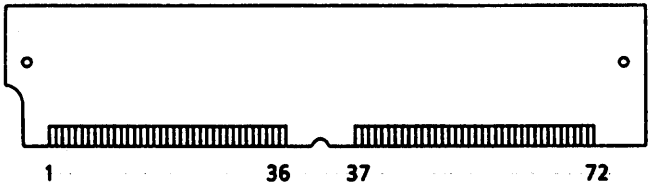
	-70	-80
t_{RAC} $\overline{RAS}$ Access Time	70ns	80ns
t_{AA} Column Address Access Time	35ns	40ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns
t_{RC} Cycle Time	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	50ns

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ31	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

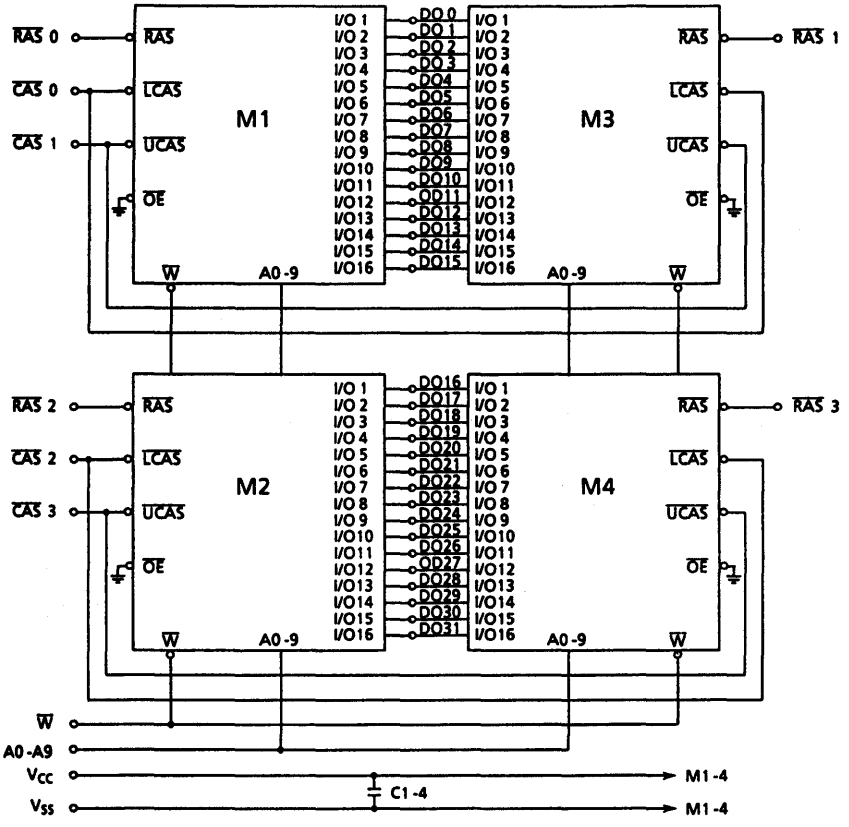
	-70	-80
PD0	NC	NC
PD1	NC	NC
PD2	V_{SS}	NC
PD3	NC	V_{SS}

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	4_0	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD1
9	DQ19	21	DQ20	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ12	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD3
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7.0$	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	$-55 \sim 125$	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	3.6	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	$V_{CC} + 0.5$*	V	2
V_{IL}	Input Low Voltage	-0.5**	-	0.8	V	2

*V_{CC} + 2.0V at pulse width ≤ 20 ns (pulse width measured at V_{CC})
**-2.0V at pulse width ≤ 20 ns (pulse width measured at 0V)

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	284	mA	3,4
		THMxxxxxx-80	-	244		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			8	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	284	mA	3,5
		THMxxxxxx-80	-	244		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-70	-	154	mA	3,4 5
		THMxxxxxx-80	-	134		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			4	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	284	mA	3,5
		THMxxxxxx-80	-	244		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-40	40	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

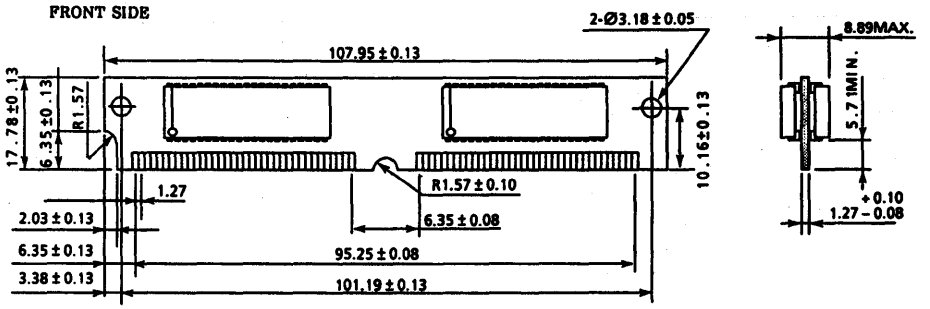
Please refer to the DRAM Module A.C. Conditions No. 20. Notes which are referenced in this section are also located in the A.C. Conditions.

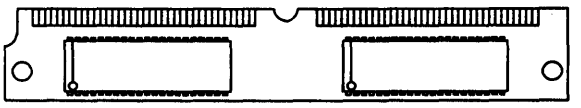
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

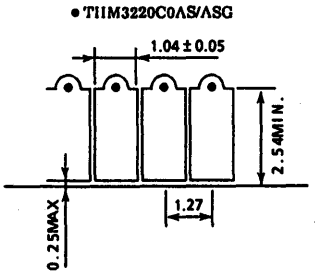
SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9)	-	25	pF
CI2	Input Capacitance ($\overline{W}$)	-	33	pF
CI3	Input Capacitance ($\overline{RAS0}$~$\overline{RAS3}$)	-	12	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	19	pF
CDQ	I/O Capacitance (DQ0~31)	-	19	pF

OUTLINE DRAWINGS

Unit in mm







4,194,304 WORD X 32 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM324000S/SG is a 4,194,304 word by 32 bit dynamic RAM module which is assembled with 8 TC5117400J devices on the printed circuit board. The THM324000 can be used as well as 8,388,608 word by 16 bit by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ·····, DQ15 and DQ31, respectively. THM324000 is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 4,194,304 word by 32 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  5,720mW MAX. Operating (THMxxxxxx-60)
  4,840mW MAX. Operating (THMxxxxxx-70)
  4,180mW MAX. Operating (THMxxxxxx-80)
  44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 2,048 Refresh cycles/16ms
- Package
  Tin-Lead Contact: THM324000S-60,70
  Gold Contact: THM324000SG-60,70

KEY PARAMETERS

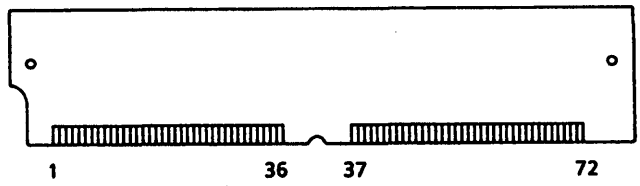
	-60	-70
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns
t_{AA} Column Address Access Time	30ns	35ns
t_{CAC} $\overline{CAS}$ Access Time	15ns	20ns
t_{RC} Cycle Time	110ns	130ns
t_{PC} Fast Page Mode Cycle Time	60ns	70ns

PIN NAMES

A0~A10	Address Inputs
DQ0~DQ31	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

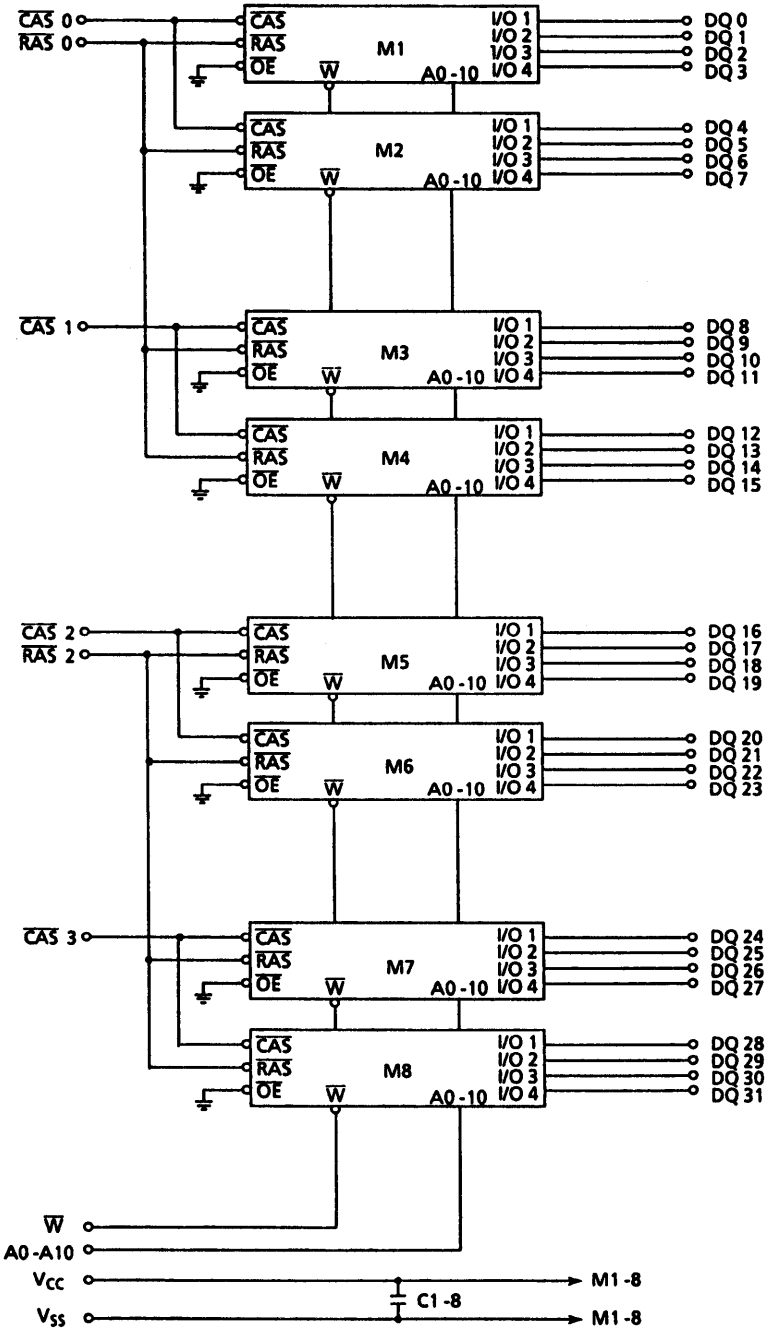
	-60	-70
PD0	V_{SS}	V_{SS}
PD1	NC	NC
PD2	NC	V_{SS}
PD3	NC	NC

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	4_0	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD1
9	DQ19	21	DQ20	33	NC	45	NC	57	DQ12	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD3
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	5.6	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0*	-	0.8	V	2

*-2.0V at pulse width ≤ 20 ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1040	mA	3,4
		THMxxxxxx-70	-	880		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1040	mA	3
		THMxxxxxx-70	-	880		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	560	mA	3,4
		THMxxxxxx-70	-	480		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1040	mA	3
		THMxxxxxx-70	-	880		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-80	80	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

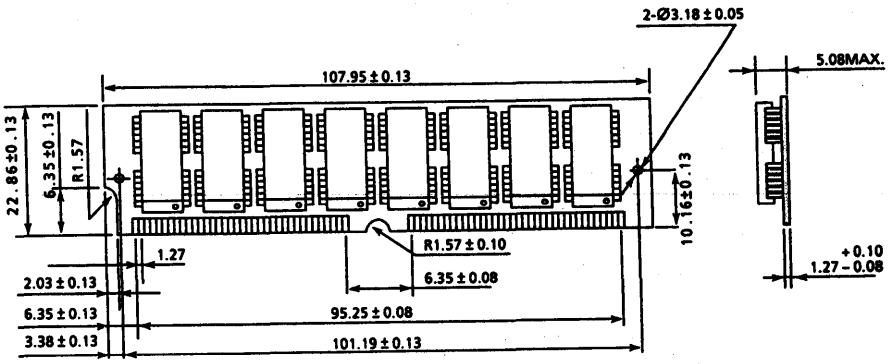
ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

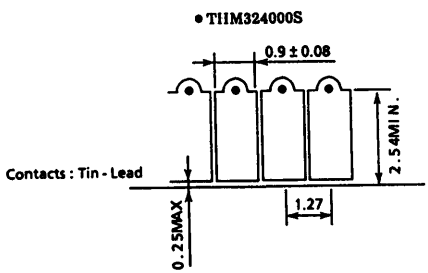
Please refer to the DRAM Module A.C. Conditions No. 16. Notes which are referenced in this section are also located in the A.C. Conditions.

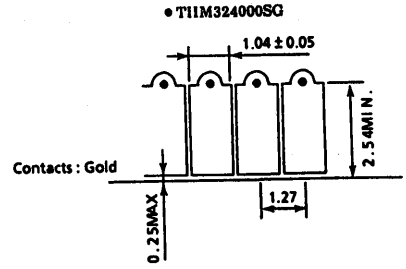
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A10)	-	88	pF
CI2	Input Capacitance ($\overline{W}$)	-	84	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	-	42	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	36	pF
CDQ	I/O Capacitance (DQ0~31)	-	17	pF

OUTLINE DRAWINGS







8,388,608 WORD X 32 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM328020 is a 8,388,608 word by 32 bit dynamic RAM module which is assembled with 16 TC5117400J devices on the printed circuit board. The THM328020 can be used as well as 16,777,216 word by 16 bit by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18,....., DQ15 and DQ31, respectively. THM328020 is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 8,388,608 word by 32 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  5,808mW MAX. Operating (THMxxxxxx-60)
  4,928mW MAX. Operating (THMxxxxxx-70)
  88mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 2,048 Refresh cycles/32ms
- Package
  Tin-Lead Contact: THM328020S-60,70
  Gold Contact: THM328020SG-60,70

KEY PARAMETERS

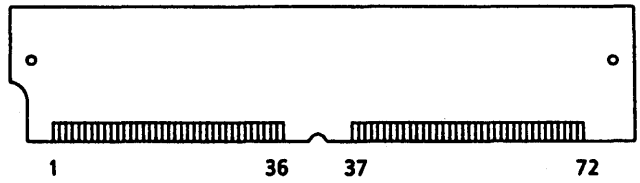
	-60	-70
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns
t_{AA} Column Address Access Time	30ns	35ns
t_{CAC} $\overline{CAS}$ Access Time	15ns	20ns
t_{RC} Cycle Time	110ns	130ns
t_{PC} Fast Page Mode Cycle Time	40ns	45ns

PIN NAMES

A0~A10	Address Inputs
DQ0~DQ31	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

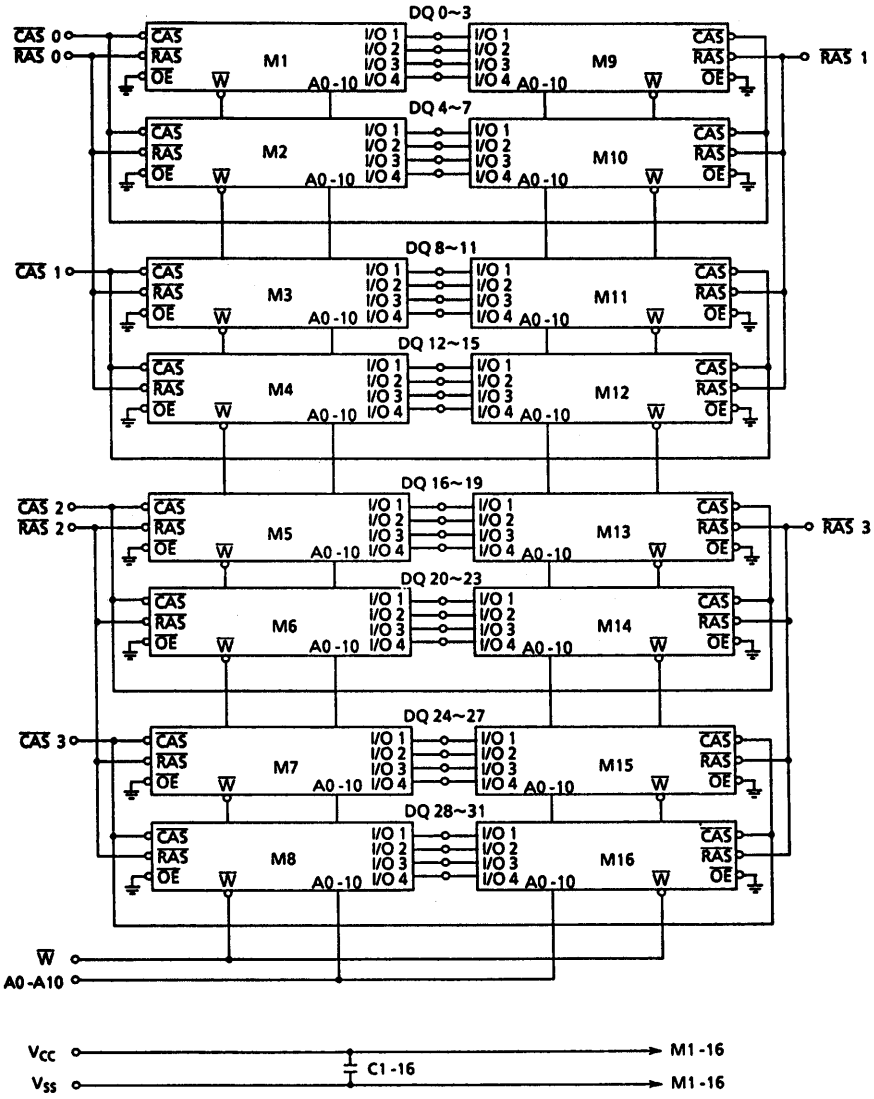
	-60	-70
PD0	NC	NC
PD1	V_{SS}	V_{SS}
PD2	NC	V_{SS}
PD3	NC	NC

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	4_0	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD1
9	DQ19	21	DQ20	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ12	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD3
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	11.2	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0*	-	0.8	V	2

*-2.0V at pulse width ≤ 20 ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1056	mA	3,4
		THMxxxxxx-70	-	896		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			32	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1056	mA	3
		THMxxxxxx-70	-	896		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	576	mA	3,4
		THMxxxxxx-70	-	496		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			16	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1056	mA	3
		THMxxxxxx-70	-	896		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-160	160	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 16. Notes which are referenced in this section are also located in the A.C. Conditions.

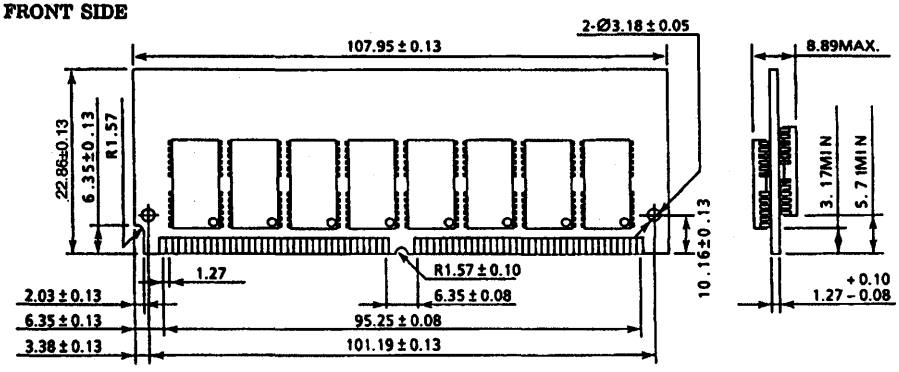
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A10)	-	100	pF
CI2	Input Capacitance ($\overline{W}$)	-	80	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	-	40	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	35	pF
CDQ1	I/O Capacitance (DQ0~31)	-	25	pF

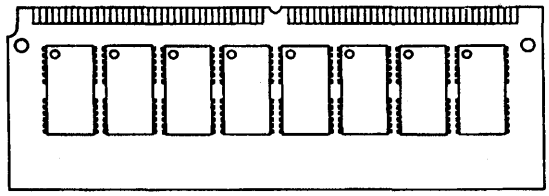
OUTLINE DRAWINGS

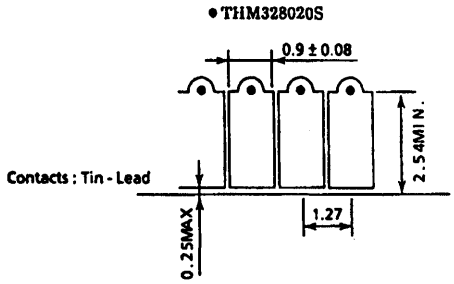
Unit in mm

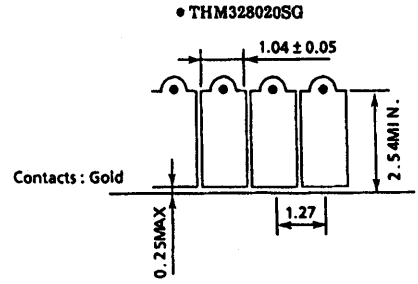
FRONT SIDE



BACK SIDE







1,048,576 WORD X 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM361020A is a 1,048,576 word by 36 bit dynamic RAM module which is assembled with 8 TC514400ASJ devices and 4 TC511000AJ/BJ devices on the printed circuit board. This module can be used as well as 2,097,152 word by 18 bit by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ·····, DQ17 and DQ35, respectively. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 1,048,576 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  7,260mW MAX. Operating (THMxxxxxx-60)
  6,160mW MAX. Operating (THMxxxxxx-70)
  5,2844mW MAX. Operating (THMxxxxxx-80)
  66mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 Refresh cycles/8ms (Burst Refresh)
- 1,024 Refresh cycles/16ms (Distributed Refresh)
- Package
  72pin SIMM Tin-Lead Contact: THM361020AS-60,70,80
  72pin SIMM Gold Contact: THM361020ASG-60,70,80

KEY PARAMETERS

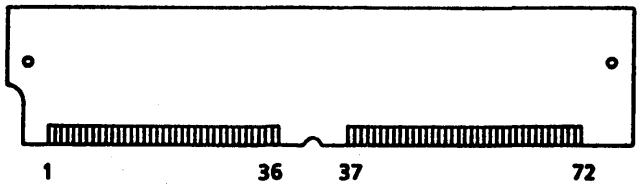
	-60	-70	-80
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA} Column Address Access Time	30ns	35ns	40ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC} Cycle Time	110ns	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$,$\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin
NC	No Connection

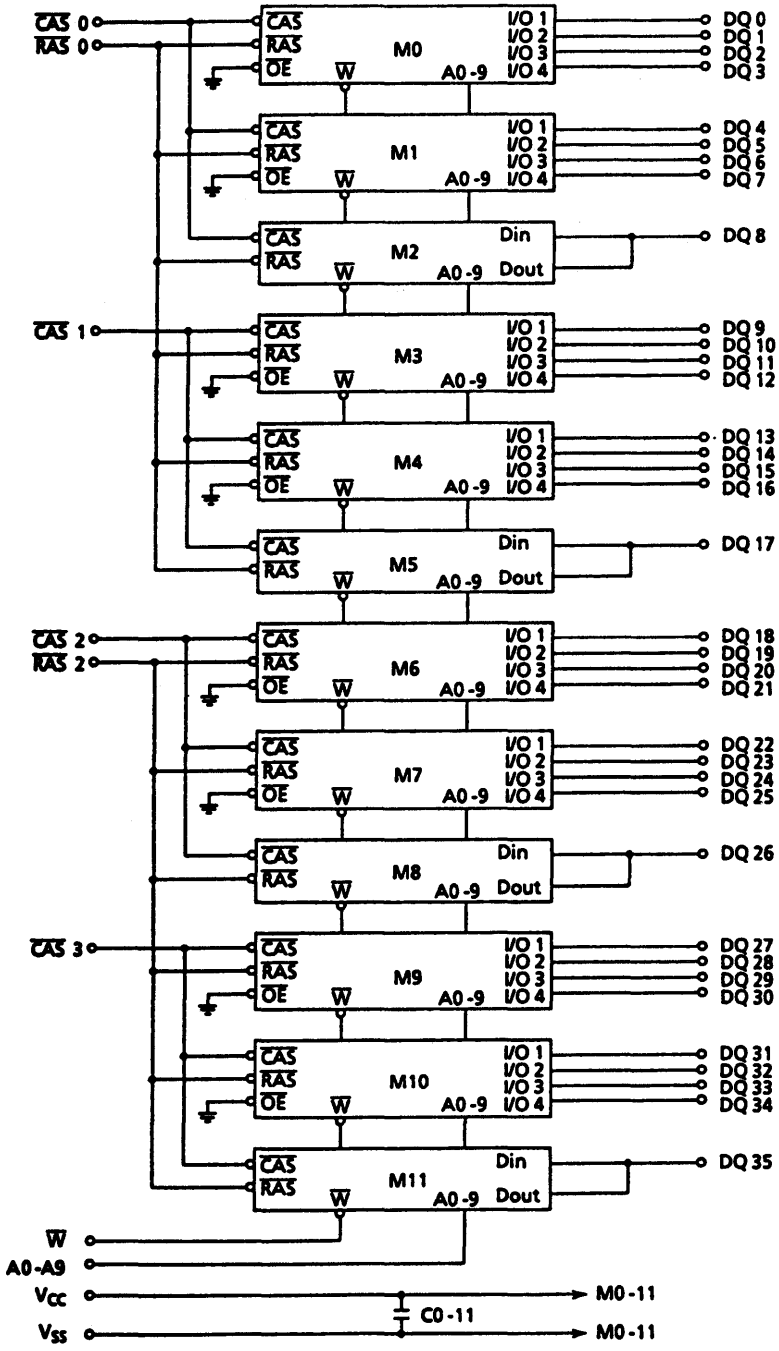
	-60	-70	-80
PD0	V_{SS}	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	NC	V_{SS}	NC
PD3	NC	NC	V_{SS}

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	8.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1320	mA	3,4 5
		THMxxxxxx-70	-	1120		
		THMxxxxxx-80	-	960		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			24	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1320	mA	3,5
		THMxxxxxx-70	-	1120		
		THMxxxxxx-80	-	960		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	800	mA	3,4 5
		THMxxxxxx-70	-	800		
		THMxxxxxx-80	-	680		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			12	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1320	mA	3,5
		THMxxxxxx-70	-	1120		
		THMxxxxxx-80	-	960		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-120	120	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 4. Notes which are referenced in this section are also located in the A.C. Conditions.

CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

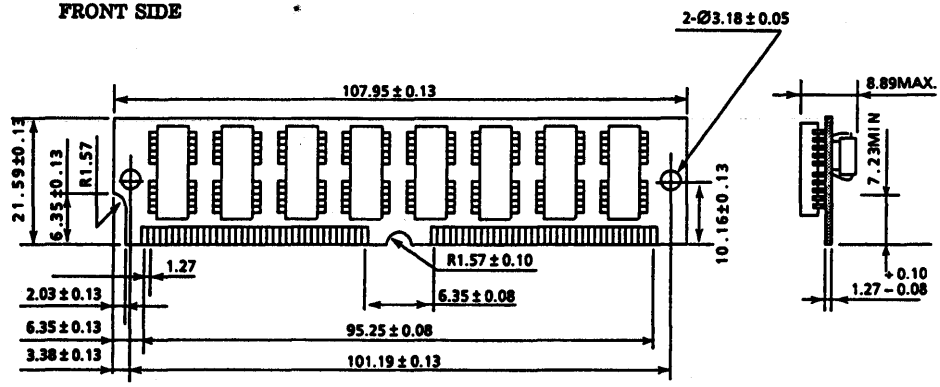
SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9)	-	88	pF
CI2	Input Capacitance ($\overline{W}$)	-	84	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	-	42	pF
CI4	Input Capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	-	36	pF
CDQ1	I/O Capacitance (DQ0~7, 9~16, 18~25, 27~34)	-	17	pF
CDQ2	I/O Capacitance (DQ8, 17, 26, 35)	-	22	pF

OUTLINE DRAWINGS

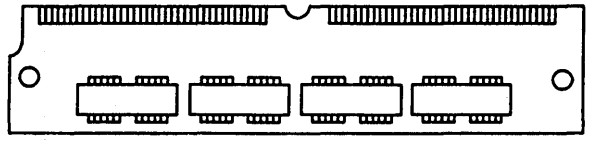
THM361020AS/ASG

Unit in mm

FRONT SIDE

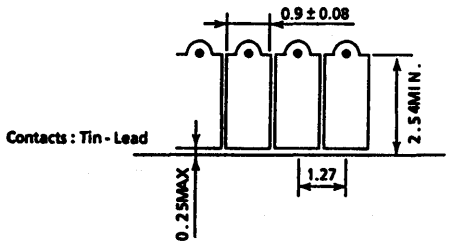


BACK SIDE

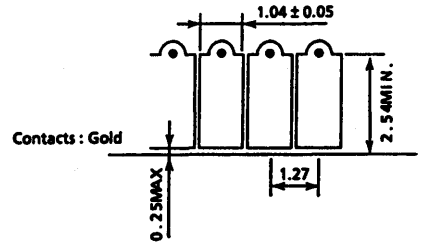


- **THM361020AS/ASG-60** USE TC514400ASJ , TC511000BJ
- **THM361020AS/ASG-70,80,10** USE TC514400ASJ , TC511000AJ

- **THM361020AS**



- **THM361020ASG**



1,048,576 WORD X 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM3610B0AS/ASG is a 1,048,576 word by 36 bit dynamic RAM module which is assembled with 2 TC5118180AJ devices on the printed circuit board. This module can be as well used as 2,097,152 word by 16 bit by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ·····, DQ17 and DQ35, respectively. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 1,048,576 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  1,650mW MAX. Operating (THMxxxxxx-70)
  1,430mW MAX. Operating (THMxxxxxx-80)
  11mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 Refresh cycles/16ms
- Package
  Tin-Lead Contact: THM3610B0AS-xx
  Gold Contact: THM3610B0ASG-xx

KEY PARAMETERS

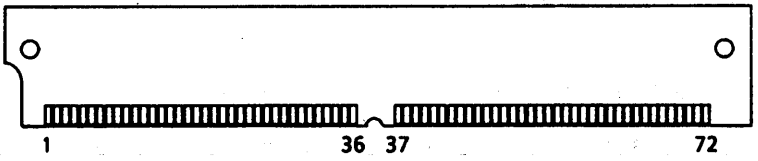
	-70	-80
t_{RAC} $\overline{RAS}$ Access Time	70ns	80ns
t_{AA} Column Address Access Time	35ns	40ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns
t_{RC} Cycle Time	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	50ns

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin
NC	No Connection

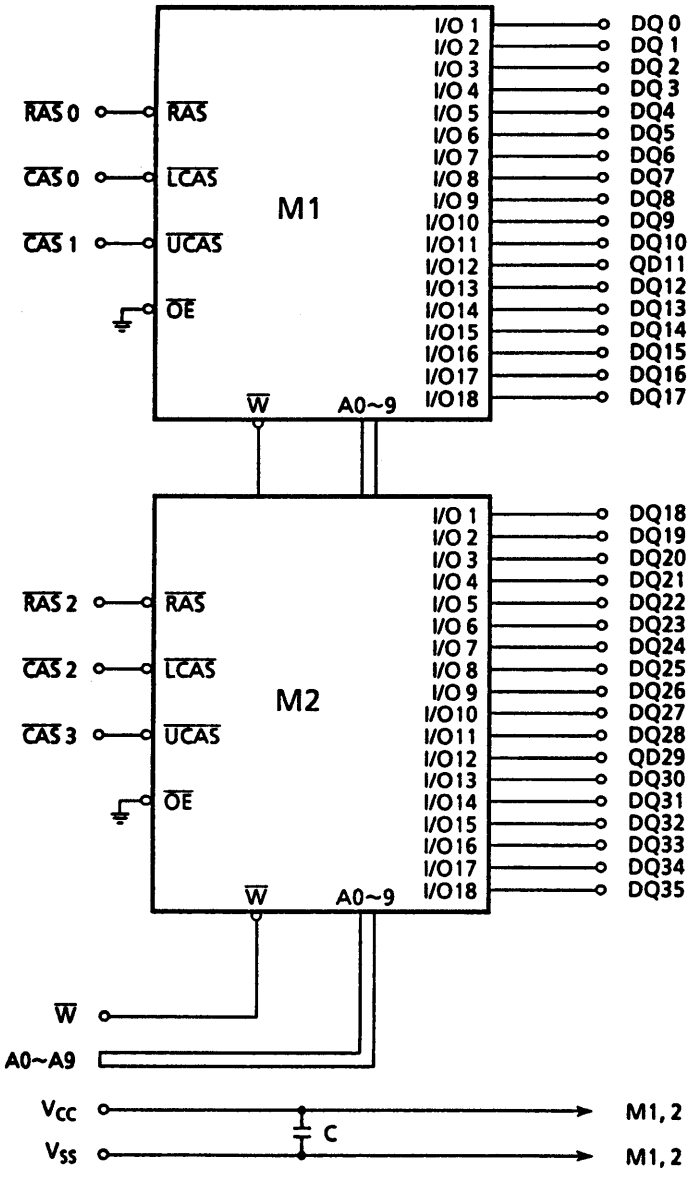
	-70	-80
PD0	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	NC
PD3	NC	V_{SS}

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7.0$	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	1.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	$V_{CC} + 0.5$*	V	2
V_{IL}	Input Low Voltage	-0.5**	-	0.8	V	2

*V_{CC} + 2.0V at pulse width ≤ 20 ns (pulse width measured at V_{CC})
**-2.0V at pulse width ≤ 20 ns (pulse width measured at 0V)

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	300	mA	3,4 5
		THMxxxxxx-80	-	260		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			4	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	300	mA	3,5
		THMxxxxxx-80	-	260		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-70	-	170	mA	3,4 5
		THMxxxxxx-80	-	150		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			2	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	300	mA	3,5
		THMxxxxxx-80	-	260		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-20	20	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 20. Notes which are referenced in this section are also located in the A.C. Conditions.

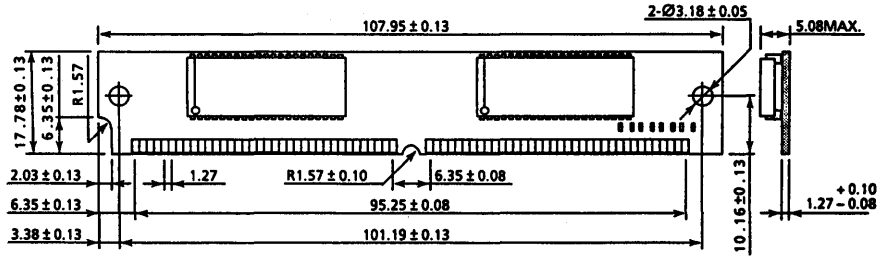
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9)	-	15	pF
CI2	Input Capacitance ($\overline{W}$)	-	19	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	-	12	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	12	pF
CDQ	I/O Capacitance (DQ0~35)	-	12	pF

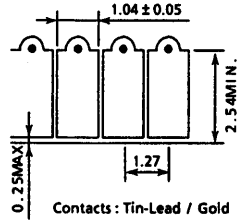
OUTLINE DRAWINGS

THM3610B0AS/ASG

Unit : mm



DETAIL OF CONTACTS • THM3610B0AS/ASG



1,048,576 WORD X 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM361070AS/ASG is a 1,048,576 word by 36 bit dynamic RAM module which is assembled with 8 TC514400SJ devices on the printed circuit board. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 1,048,576 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  5,940mW MAX. Operating (THMxxxxxx-60)
  4,950mW MAX. Operating (THMxxxxxx-70)
  4,208mW MAX. Operating (THMxxxxxx-80)
  49.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 Refresh cycles/16ms
- Package
  72 pin SIMM Tin-Lead Contact: THM361070AS-60,70,80
  72 pin SIMM Gold Contact: THM361070ASG-60,70,80

KEY PARAMETERS

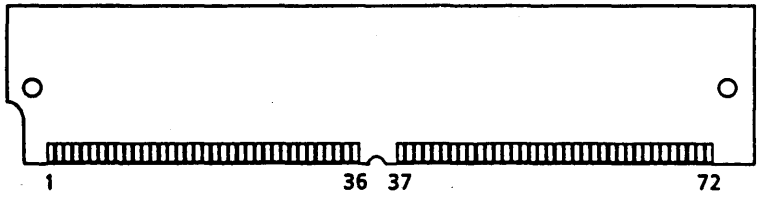
	-60	-70	-80
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA} Column Address Access Time	30ns	35ns	40ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC} Cycle Time	110ns	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin
NC	No Connection

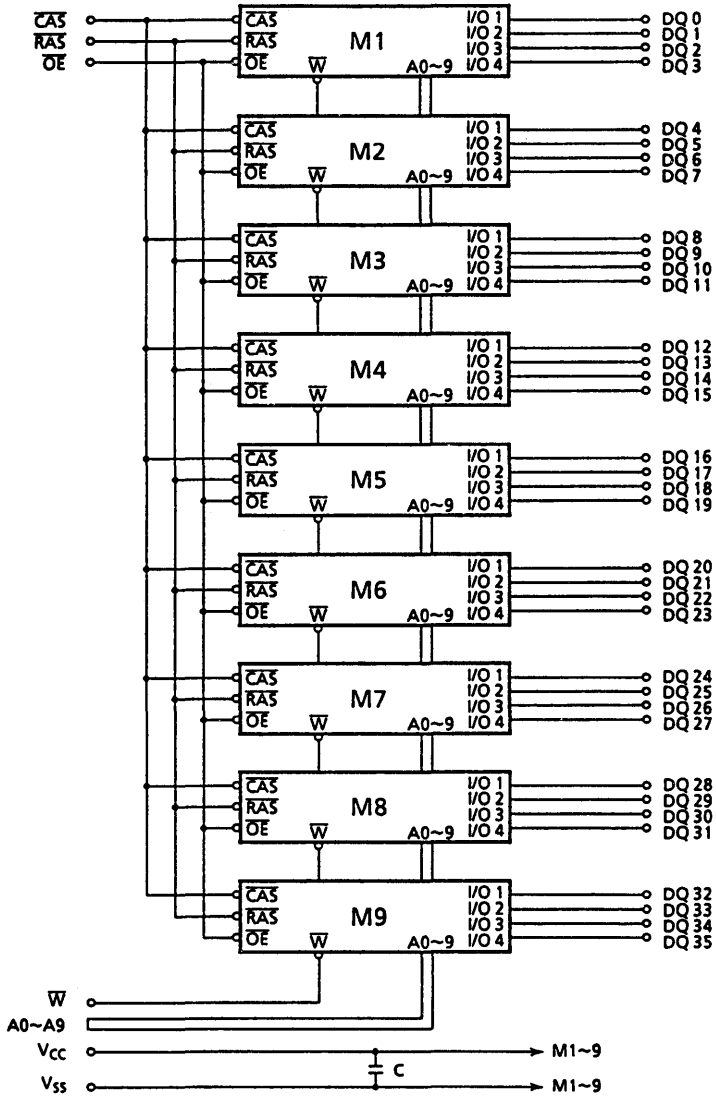
	-60	-70	-80
PD0	V_{SS}	V_{SS}	V_{SS}
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	NC	V_{SS}	NC
PD3	NC	NC	V_{SS}
PD4	NC	NC	NC

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS}$	52	DQ25	64	NC
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	NC
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	NC
7	DQ5	19	$\overline{OE}$	31	A8	43	NC	55	DQ28	67	PD0
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS}$	56	DQ29	68	PD1
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ30	69	PD2
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD3
11	PD4	23	DQ11	35	DQ17	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ12	36	DQ18	48	V_{SS}	60	DQ32	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	6.3	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1080	mA	3,4 5
		THMxxxxxx-70	-	900		
		THMxxxxxx-80	-	765		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1080	mA	3,5
		THMxxxxxx-70	-	900		
		THMxxxxxx-80	-	765		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	630	mA	3,4 5
		THMxxxxxx-70	-	630		
		THMxxxxxx-80	-	540		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1080	mA	3,5
		THMxxxxxx-70	-	900		
		THMxxxxxx-80	-	765		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-90	90	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 11. Notes which are referenced in this section are also located in the A.C. Conditions.

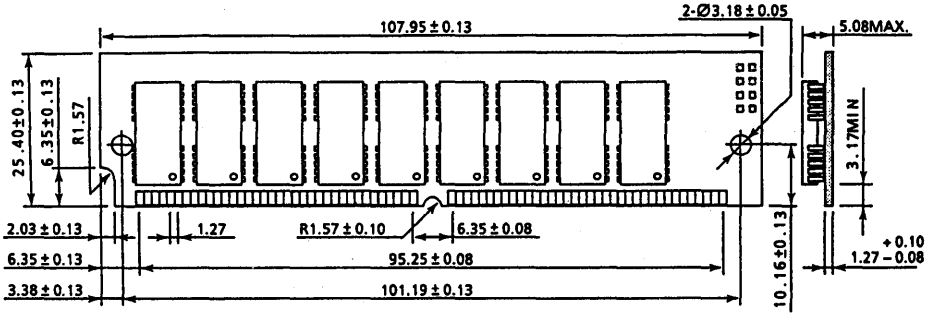
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9)	-	80	pF
CI2	Input Capacitance ($\overline{W}$, $\overline{OE}$)	-	70	pF
CI3	Input Capacitance ($\overline{RAS}$)	-	60	pF
CI4	Input Capacitance ($\overline{CAS}$)	-	50	pF
CDQ	I/O Capacitance (DQ0~35)	-	15	pF

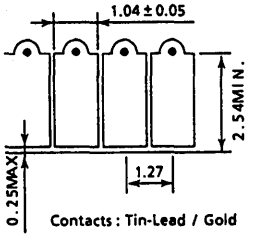
OUTLINE DRAWINGS

THM361070AS/ASG

Unit : mm



DETAIL OF CONTACTS • THM361070AS/ASG



2,097,152 WORD X 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM362020A is a 2,097,152 word by 36 bit dynamic RAM module which is assembled with 16 TC514400ASJ devices and 8 TC511000BJ/AJ devices on the printed circuit board. This module can be used as well as 4,194,304 word by 18 bit by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ·····, DQ17 and DQ35, respectively. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 2,097,152 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  7,392mW MAX. Operating (THMxxxxxx-60)
  6,292mW MAX. Operating (THMxxxxxx-70)
  5,416mW MAX. Operating (THMxxxxxx-80)
  132mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 Refresh cycles/8ms (Burst Refresh)
- 1,024 Refresh cycles/16ms (Distributed Refresh)
- Package
  72 pin SIMM Tin-Lead Contact: THM362020AS-60,70,80
  72 pin SIMM Gold Contact: THM362020ASG-60,70,80

KEY PARAMETERS

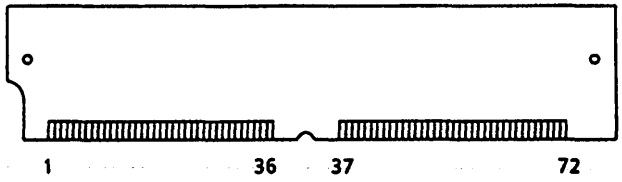
	-60	-70	-80
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA} Column Address Access Time	30ns	35ns	40ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC} Cycle Time	110ns	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

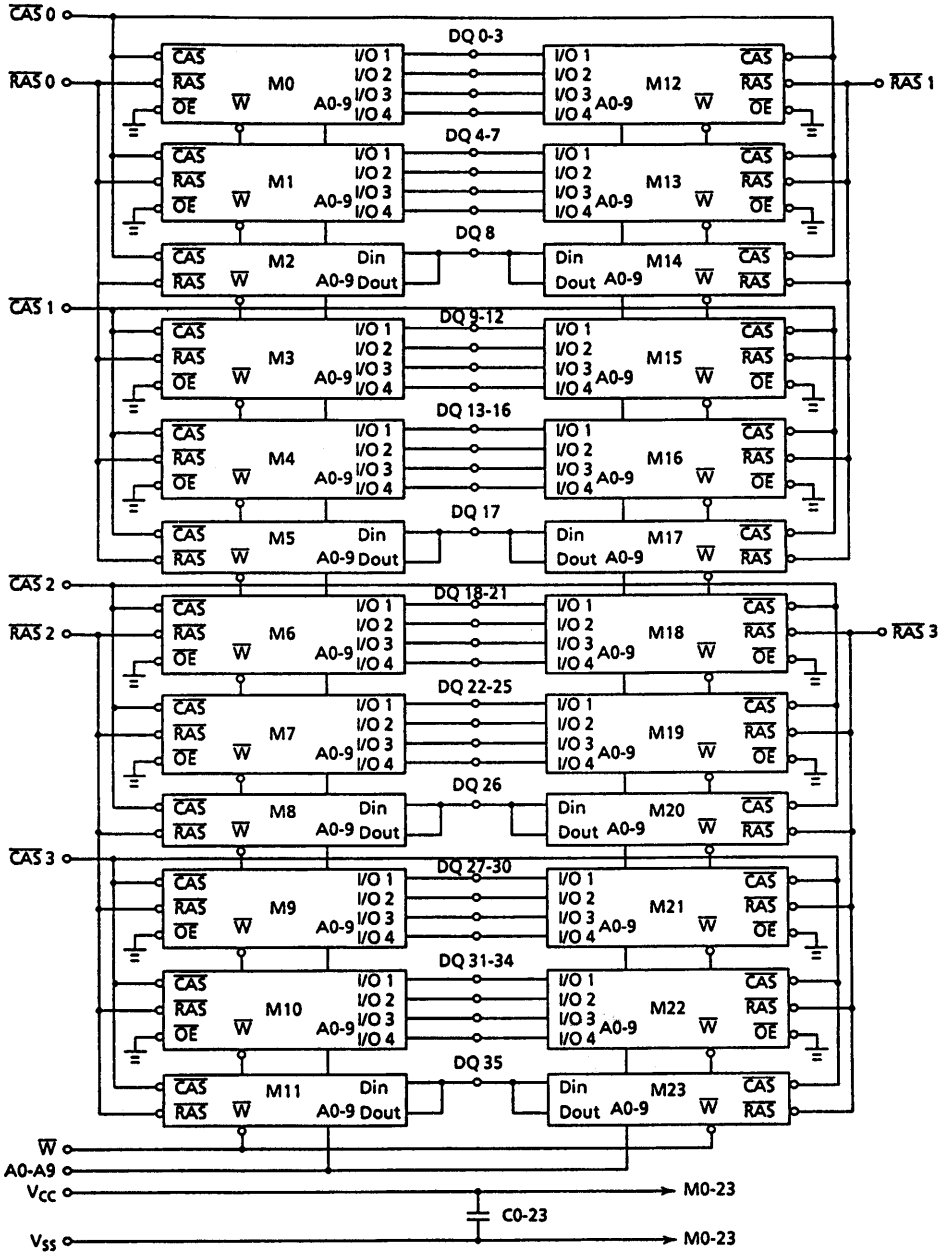
	-60	-70	-80
PD0	NC	NC	NC
PD1	NC	NC	NC
PD2	NC	V_{SS}	NC
PD3	NC	NC	V_{SS}

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	16.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1344	mA	3,4 5
		THMxxxxxx-70	-	1144		
		THMxxxxxx-80	-	984		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			48	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1344	mA	3,5
		THMxxxxxx-70	-	1144		
		THMxxxxxx-80	-	984		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	824	mA	3,4 5
		THMxxxxxx-70	-	824		
		THMxxxxxx-80	-	704		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			24	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1344	mA	3,5
		THMxxxxxx-70	-	1144		
		THMxxxxxx-80	-	984		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-240	240	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 4.Notes which are referenced in this section are also located in the A.C. Conditions.

CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta= 0~70°C)

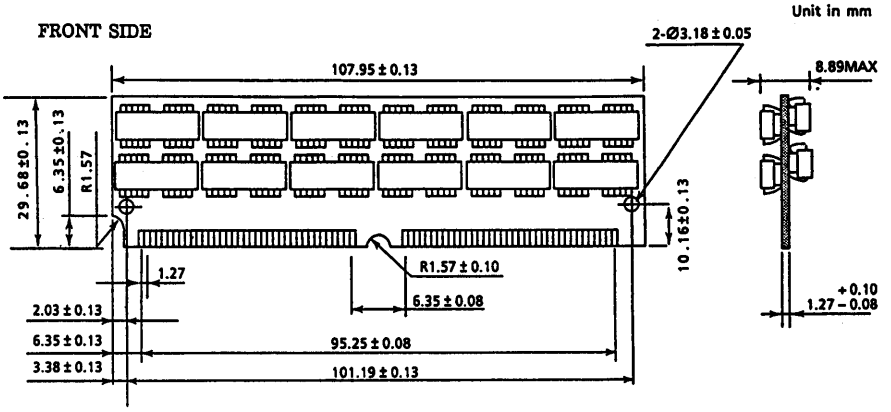
SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9)	-	161	pF
CI2	Input Capacitance ($\overline{W}$)	-	168	pF
CI3	Input Capacitance ($\overline{RAS0}$~$\overline{RAS2}$)	-	42	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	42	pF
CDQ1	I/O Capacitance (DQ0~7, 9~16, 18~25, 27~34)	-	29	pF
CDQ2	I/O Capacitance (DQ8, 17, 26, 35)	-	39	pF

OUTLINE DRAWINGS

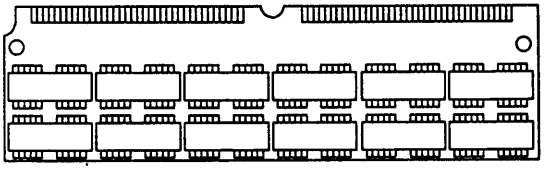
THM362020AS/ASG

Unit in mm

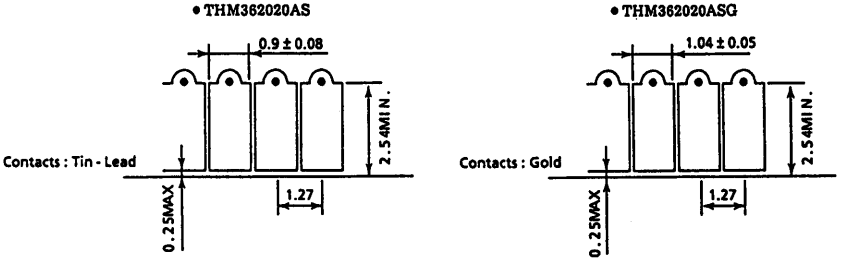
FRONT SIDE



BACK SIDE



•THM362020AS/ASG-60 USE TC514400ASJ, TC511000BJ
•THM362020AS/ASG-70,80,10 USE TC514400ASJ, TC511000AJ



2,097,152 WORD X 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM362040A is a 2,097,152 word by 36 bit dynamic RAM module which is assembled with 18 TC514400ASJ devices and 8 TC511000BFT devices on the printed circuit board. This module can be used as well as 2,097,152 words by 18 bits dynamic RAM module, by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ·····, DQ17 and DQ35, respectively. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 2,097,152 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  7,392mW MAX. Operating (THMxxxxxx-60)
  6,292mW MAX. Operating (THMxxxxxx-70)
  5,416mW MAX. Operating (THMxxxxxx-80)
  132mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 Refresh cycles/8ms (Burst Refresh)
- 1,024 Refresh cycles/16ms (Distributed Refresh)
- Package
  72 pin SIMM Tin-Lead Contact: THM362040AS-60,70,80
  72 pin SIMM Gold Contact: THM362040ASG-60,70,80

KEY PARAMETERS

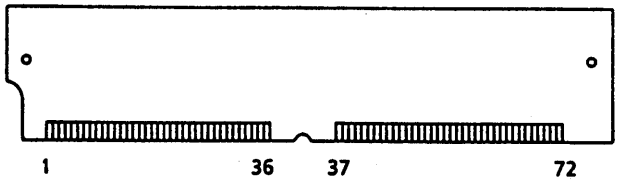
	-60	-70	-80
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA} Column Address Access Time	30ns	35ns	40ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC} Cycle Time	110ns	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

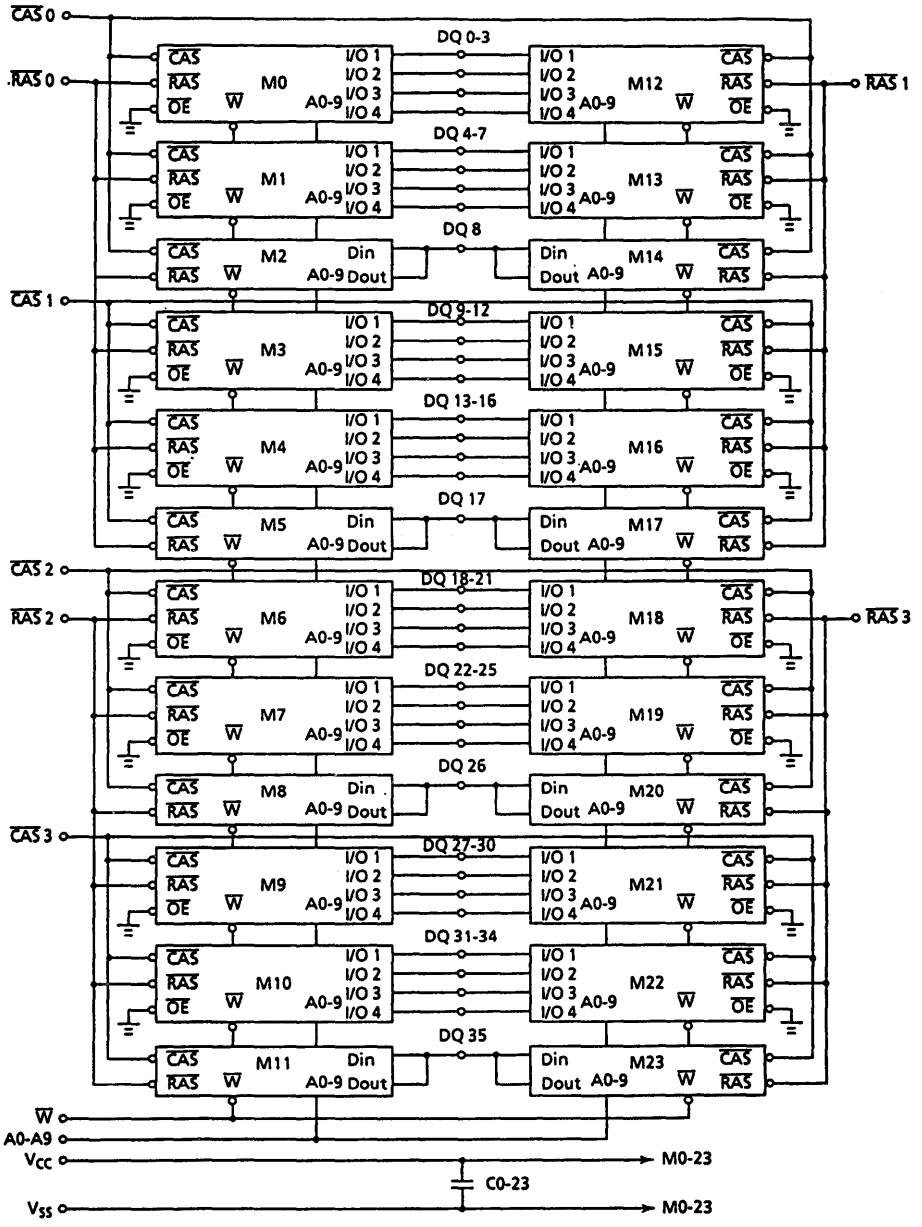
	-60	-70	-80
PD0	NC	NC	NC
PD1	NC	NC	NC
PD2	NC	V_{SS}	NC
PD3	NC	NC	V_{SS}

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS1}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	NC	57	DQ13	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	16.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1344	mA	3,4 5
		THMxxxxxx-70	-	1144		
		THMxxxxxx-80	-	984		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			48	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1344	mA	3,5
		THMxxxxxx-70	-	1144		
		THMxxxxxx-80	-	984		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	824	mA	3,4 5
		THMxxxxxx-70	-	824		
		THMxxxxxx-80	-	704		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			24	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1344	mA	3,5
		THMxxxxxx-70	-	1144		
		THMxxxxxx-80	-	984		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-240	240	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 12. Notes which are referenced in this section are also located in the A.C. Conditions.

CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

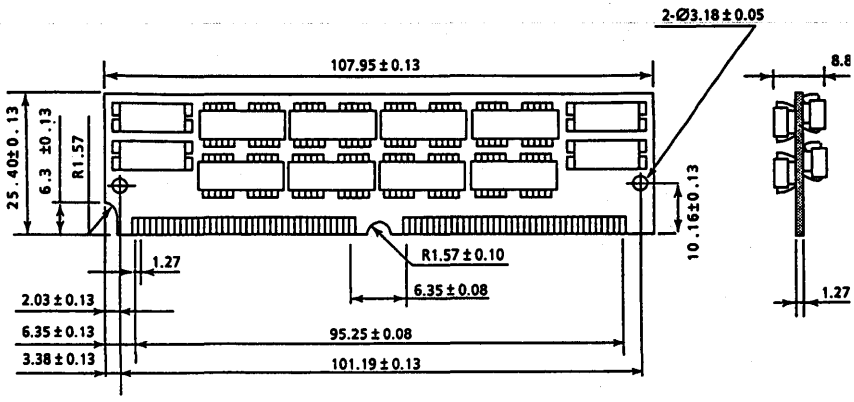
SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9)	-	161	pF
CI2	Input Capacitance ($\overline{W}$)	-	168	pF
CI3	Input Capacitance ($\overline{RAS0}$~$\overline{RAS3}$)	-	42	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	42	pF
CDQ1	I/O Capacitance (DQ0~7, 9~16, 18~25, 27~34)	-	29	pF
CDQ2	I/O Capacitance (DQ8,17, 26, 35)	-	39	pF

OUTLINE DRAWINGS

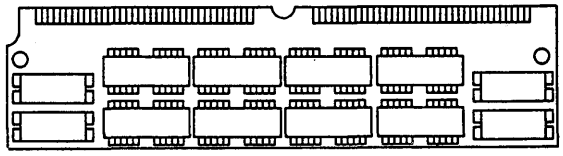
THM362040AS/ASG

Unit i

FRONT SIDE

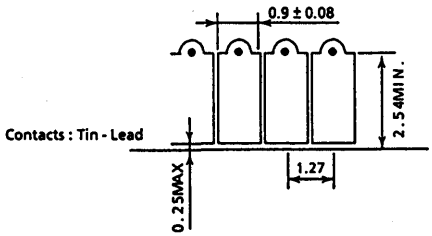


BACK SIDE

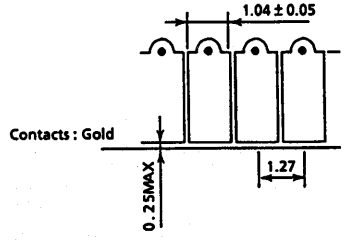


•THM362040AS/ASG-60,70,80,10 USE TC514400ASJ , TC511000BFT

• THM362040AS



• THM362040ASG



2,097,152 WORD X 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM3620C0A is a 2,097,152 words by 36 bit dynamic RAM module which is assembled with 4 TC5118180AJ devices on the printed circuit board. This module can be as well used as 4,193,304 word by 18 bit by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ·····, DQ17 and DQ35, respectively. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 2,097,152 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  1,672mW MAX. Operating (THMxxxxxx-70)
  1,452mW MAX. Operating (THMxxxxxx-80)
  22mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 Refresh cycles/16ms
- Package
  72 pin SIMM Tin-Lead Contact: THM3620C0AS-xx
  72 pin SIMM Gold Contact: THM3620C0ASG-xx

KEY PARAMETERS

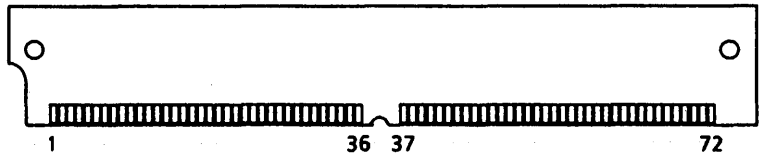
	-70	-80
t_{RAC} $\overline{RAS}$ Access Time	70ns	80ns
t_{AA} Column Address Access Time	35ns	40ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns
t_{RC} Cycle Time	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	50ns

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ31	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin
NC	No Connection

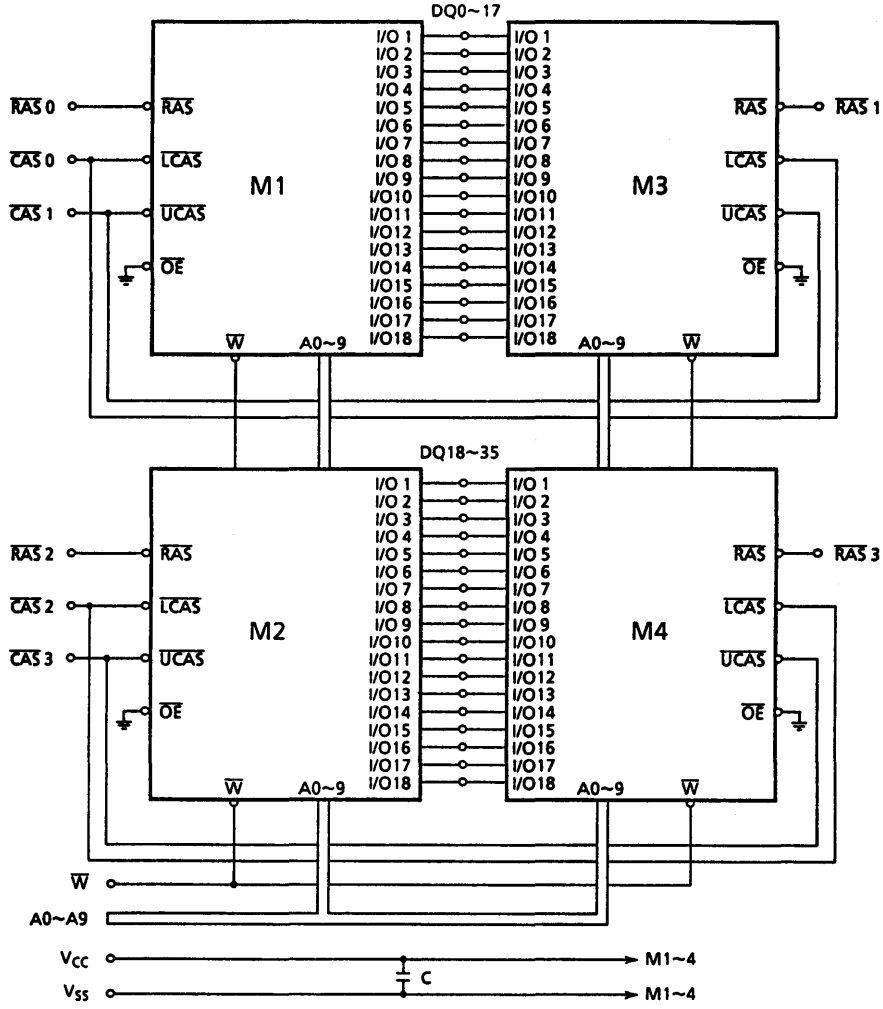
	-70	-80
PD0	NC	NC
PD1	NC	NC
PD2	V_{SS}	NC
PD3	NC	V_{SS}

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7.0$	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	3.6	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	$V_{CC} + 0.5$	V	2
V_{IL}	Input Low Voltage	-0.5	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	304	mA	3,4 5
		THMxxxxxx-80	-	264		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			8	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	304	mA	3,5
		THMxxxxxx-80	-	264		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-70	-	174	mA	3,4 5
		THMxxxxxx-80	-	154		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			4	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-70	-	304	mA	3,5
		THMxxxxxx-80	-	264		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-40	40	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 20. Notes which are referenced in this section are also located in the A.C. Conditions.

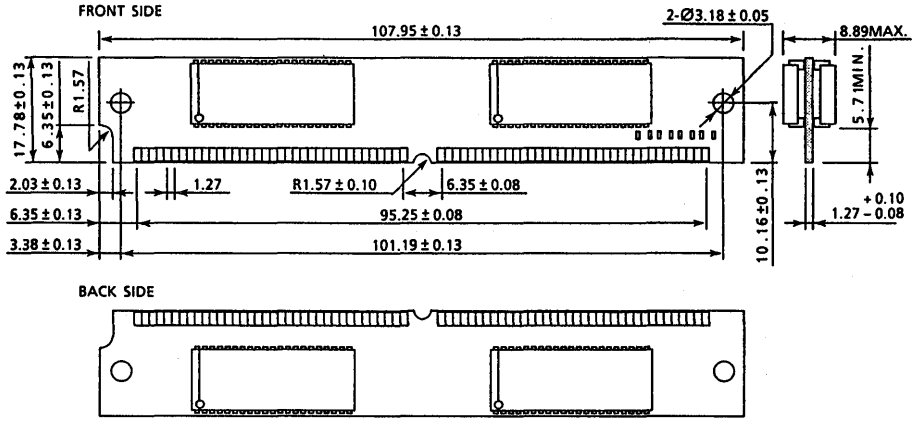
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta= 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9)	-	25	pF
CI2	Input Capacitance ($\overline{W}$)	-	33	pF
CI3	Input Capacitance ($\overline{RAS0}$~$\overline{RAS3}$)	-	12	pF
CI4	Input Capacitance ($\overline{CAS0}$ ~$\overline{CAS3}$)	-	19	pF
CDQ	I/O Capacitance (DQ0~35)	-	19	pF

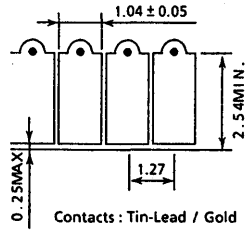
OUTLINE DRAWINGS

THM3620C0AS/ASG

Unit : mm



DETAIL OF CONTACTS • THM3620C0AS/ASG



2,097,152 WORD X 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM362060A is a 2,097,152 word by 36 bit dynamic RAM module which is assembled with 18 TC514400ASJ devices on the printed circuit board. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 2,097,152 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  6,039mW MAX. Operating (THMxxxxxx-60)
  5,049mW MAX. Operating (THMxxxxxx-70)
  4,307mW MAX. Operating (THMxxxxxx-80)
  99mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 1,024 Refresh cycles/16ms
- Package
  72 pin SIMM Tin-Lead Contact: THM362060AS-60,70,80
  72 pin SIMM Gold Contact: THM362060ASG-60,70,80

KEY PARAMETERS

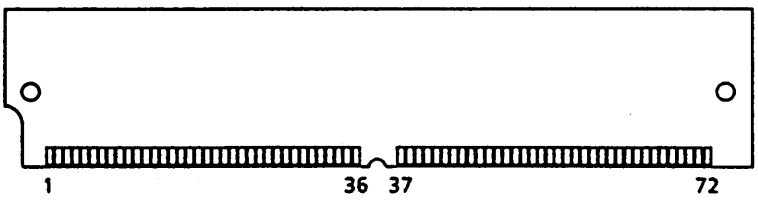
	-60	-70	-80
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA} Column Address Access Time	30ns	35ns	40ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns
t_{RC} Cycle Time	115ns	130ns	150ns
t_{PC} Fast Page Mode Cycle Time	45ns	45ns	50ns

PIN NAMES

A0~A9	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS0}$,$\overline{CAST}$	Column Address Strobe
$\overline{RAS0}$,$\overline{RAST}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin
NC	No Connection

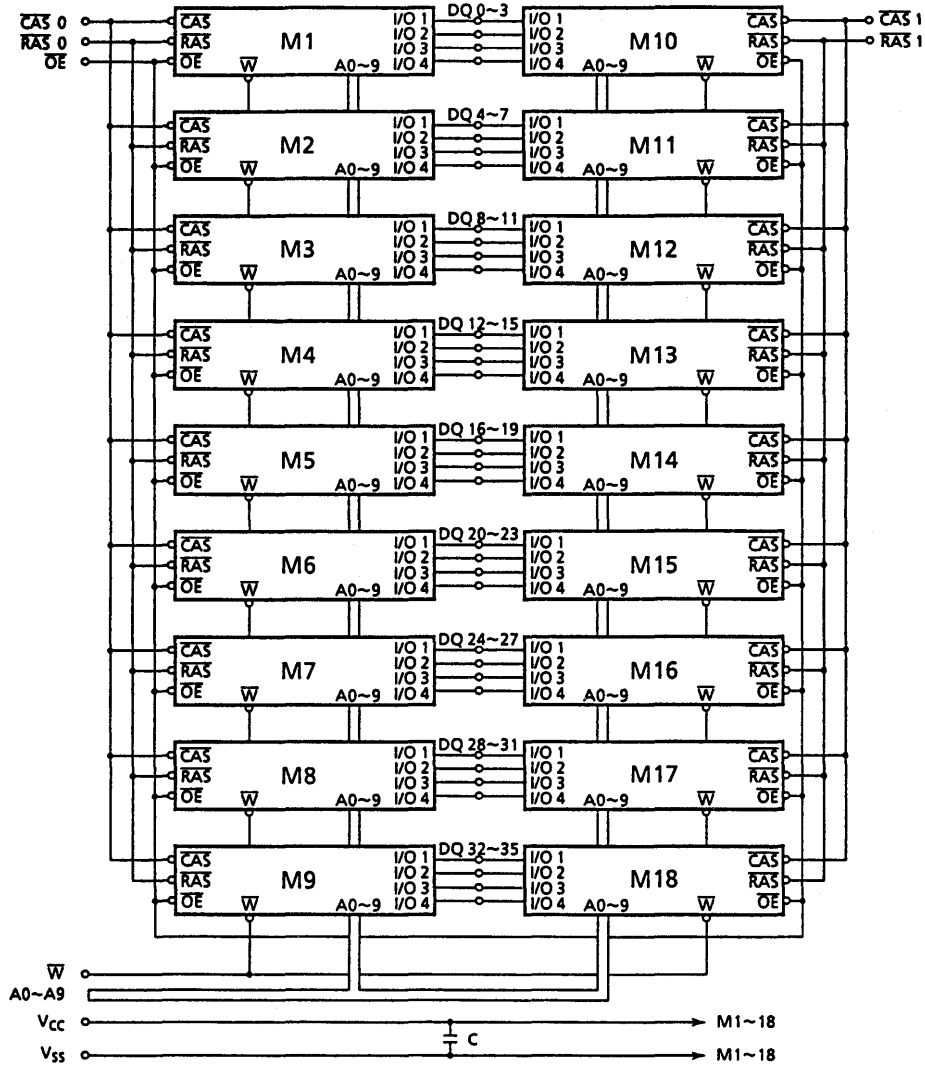
	-60	-70	-80
PD0	NC	NC	NC
PD1	NC	NC	NC
PD2	NC	V_{SS}	NC
PD3	NC	NC	V_{SS}
PD4	NC	NC	NC

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	NC
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	NC
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	NC
7	DQ5	19	$\overline{OE}$	31	A8	43	$\overline{CAS1}$	55	DQ28	67	PD0
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS0}$	56	DQ29	68	PD1
9	DQ7	21	DQ9	33	NC	45	$\overline{RAS1}$	57	DQ30	69	PD2
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD3
11	PD4	23	DQ11	35	DQ17	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ12	36	DQ18	48	V_{SS}	60	DQ32	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	12.6	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1098	mA	3,4 5
		THMxxxxxx-70	-	918		
		THMxxxxxx-80	-	783		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			36	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1098	mA	3,5
		THMxxxxxx-70	-	918		
		THMxxxxxx-80	-	783		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	648	mA	3,4 5
		THMxxxxxx-70	-	648		
		THMxxxxxx-80	-	558		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			18	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1098	mA	3,5
		THMxxxxxx-70	-	918		
		THMxxxxxx-80	-	783		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-180	180	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 11. Notes which are referenced in this section are also located in the A.C. Conditions.

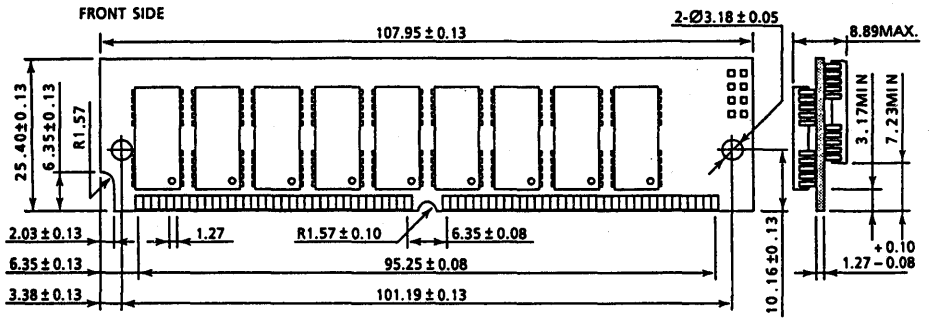
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta= 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9)	-	130	pF
CI2	Input Capacitance ($\overline{W}$, $\overline{OE}$)	-	130	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS1}$)	-	70	pF
CI4	Input Capacitance ($\overline{CAS0}$, $\overline{CAS1}$)	-	70	pF
CDQ	I/O Capacitance (DQ0~35)	-	35	pF

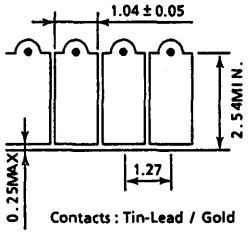
OUTLINE DRAWINGS

THM362060AS/ASG

Unit : mm



DETAIL OF CONTACTS • THM362060AS/ASG



Weight : 24.5g (Typ.)

4,194,304 WORD X 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM364020 is a 4,194,304 word by 36 bit dynamic RAM module which is assembled with 8 TC5117400J devices and 4 TC514100AJ devices on the printed circuit board. The THM364020S can be used as well as 16,777,216 word by 18 bit by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20,·····, DQ17 and DQ35, respectively. THM364020 is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 4,194,304 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  8,360mW MAX. Operating (THMxxxxxx-60)
  7,040mW MAX. Operating (THMxxxxxx-70)
  66mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 2,048 Refresh cycles/16ms (Burst Refresh)
- 2,048 Refresh cycles/32ms (Distributed Refresh)
- Package
  Tin-Lead Contact: THM364020S-60,70
  Gold Contact: THM364020SG-60,70

KEY PARAMETERS

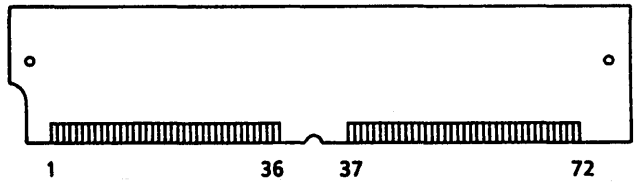
	-60	-70
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns
t_{AA} Column Address Access Time	30ns	35ns
t_{CAC} $\overline{CAS}$ Access Time	15ns	20ns
t_{RC} Cycle Time	110ns	130ns
t_{PC} Fast Page Mode Cycle Time	40ns	45ns

PIN NAMES

A0~A10	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

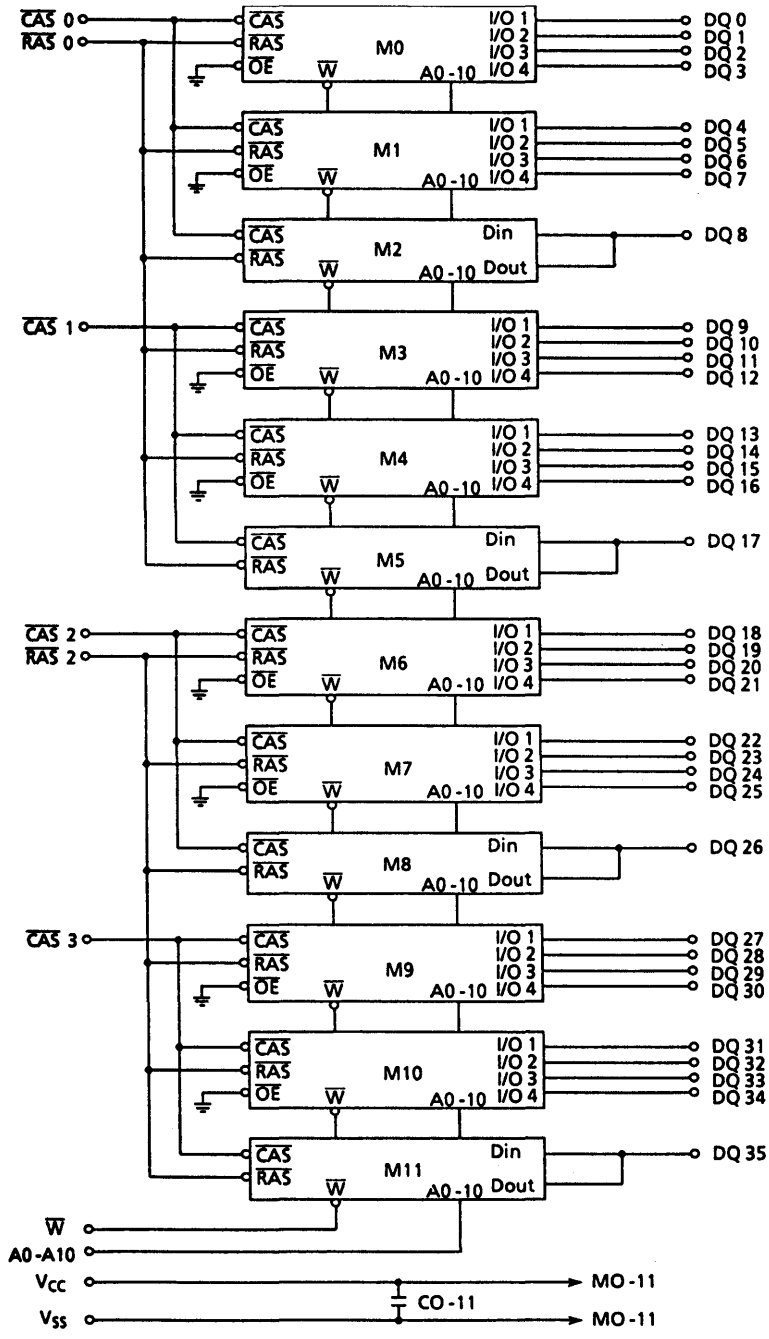
	-60	-70
PD0	V_{SS}	V_{SS}
PD1	NC	NC
PD2	NC	V_{SS}
PD3	NC	NC

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	8.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0*	-	0.8	V	2

*-2.0V at pulse width ≤ 20 ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1520	mA	3,4
		THMxxxxxx-70	-	1280		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			24	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1520	mA	3
		THMxxxxxx-70	-	1280		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	800	mA	3,4
		THMxxxxxx-70	-	720		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			12	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1520	mA	3
		THMxxxxxx-70	-	1280		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-120	120	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 15. Notes which are referenced in this section are also located in the A.C. Conditions.

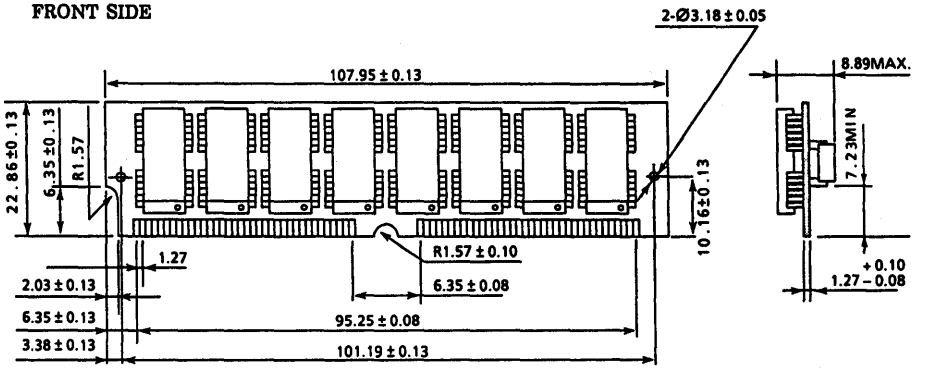
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A10)	-	88	pF
CI2	Input Capacitance ($\overline{W}$)	-	84	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	-	42	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	36	pF
CDQ1	I/O Capacitance (DQ0~7, 9~16, 18~25, 27~34)	-	17	pF
CDQ2	I/O Capacitance (DQ8, 17, 26, 35)	-	22	pF

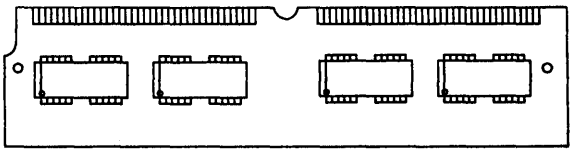
OUTLINE DRAWINGS

Unit in mm

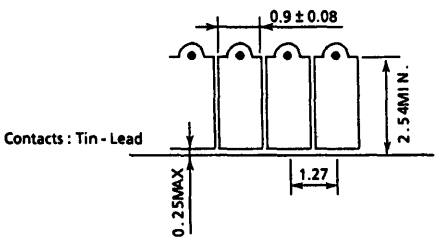
FRONT SIDE



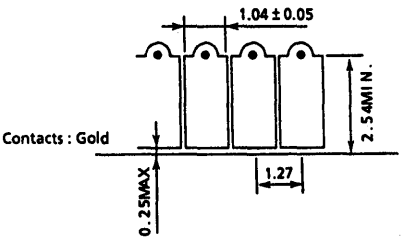
BACK SIDE



• THM364020S



• THM364020SG



4,194,304 WORD X 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM3640A0 is a 4,194,304 word by 36 bit dynamic RAM module which is assembled with 9 TC5116400J devices on the printed circuit board. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 4,194,304 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  4,455mW MAX. Operating (THMxxxxxx-60)
  3,960mW MAX. Operating (THMxxxxxx-70)
  49.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 4,096 Refresh cycles/64ms
- Package
  72pin SIMM Tin-Lead Contact: THM3640A0S-60,70
  72pin SIMM Gold Contact: THM3640A0SG-60,70

KEY PARAMETERS

	-60	-70
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns
t_{AA} Column Address Access Time	30ns	35ns
t_{CAC} $\overline{CAS}$ Access Time	15ns	20ns
t_{RC} Cycle Time	110ns	130ns
t_{PC} Fast Page Mode Cycle Time	40ns	45ns

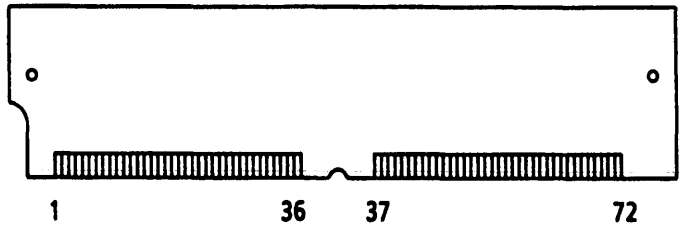
PIN NAMES

A0~A9 A10R, A11R	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
PD	Presence Detect Pin

	-60	-70
PD0	V_{SS}	V_{SS}
PD1	NC	NC
PD2	NC	V_{SS}
PD3	NC	NC
PD4	V_{SS}*	V_{SS}*

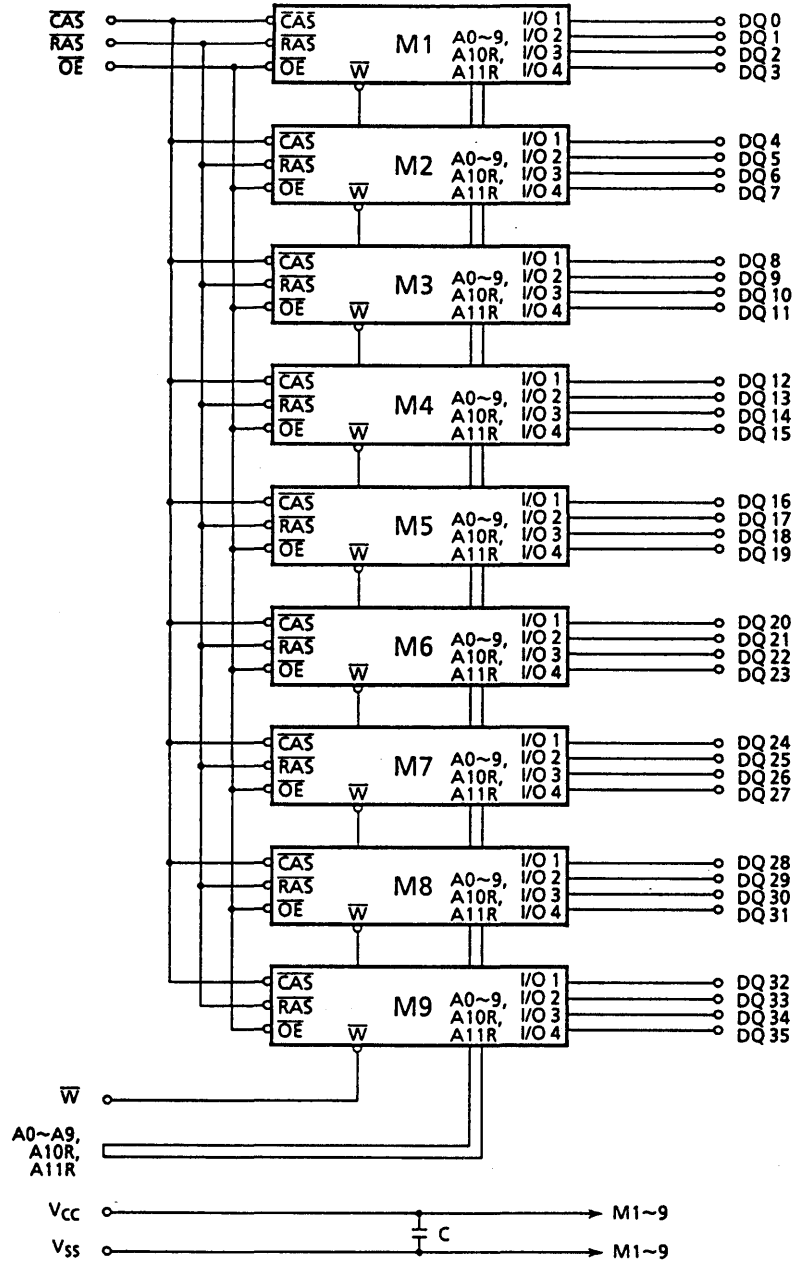
* Through the resistor (2.6KΩ) to GND.

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CASØ}$	52	DQ25	64	NC
5	DQ3	17	A5	29	DQ16	41	A10R	53	DQ26	65	NC
6	DQ4	18	A6	30	V_{CC}	42	A11R	54	DQ27	66	NC
7	DQ5	19	$\overline{OE}$	31	A8	43	NC	55	DQ28	67	PD0
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS}$	56	DQ29	68	PD1
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ30	69	PD2
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD3
11	PD4	23	DQ11	35	DQ17	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ12	36	DQ18	48	V_{SS}	60	DQ32	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	6.3	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0*	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	810	mA	3, 4, 5
		THMxxxxxx-70	-	720		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	810	mA	3, 5
		THMxxxxxx-70	-	720		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	630	mA	3, 4, 5
		THMxxxxxx-70	-	540		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	810	mA	3, 5
		THMxxxxxx-70	-	720		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-90	90	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A. C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C Conditions No. 13. Notes which are referenced in this section are also located in the A.C. Conditions.

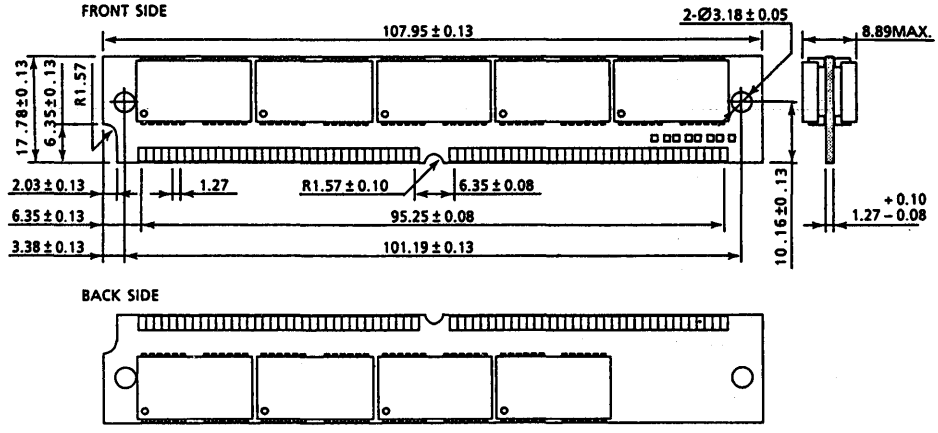
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta= 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9, A10R, A11R)	-	65	pF
CI2	Input Capacitance ($\overline{W}$, $\overline{OE}$)	-	60	pF
CI3	Input Capacitance ($\overline{RAS}$)	-	55	pF
CI4	Input Capacitance ($\overline{CAS}$)	-	55	pF
CDQ	I/O Capacitance (DQ0~35)	-	15	pF

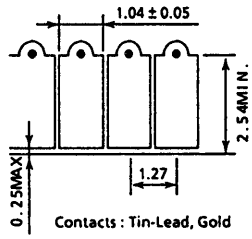
OUTLINE DRAWINGS

THM3640A0S/SG

Unit : mm



DETAIL OF CONTACTS • THM3640A0S/SG



Contacts : Tin-Lead, Gold

Weight : 17.0g (Typ.)

8,388,608 WORD X 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM368020 is a 8,388,608 word by 36 bit dynamic RAM module which is assembled with 16 TC5117400J devices and 8 TC514100ASJ devices on the printed circuit board. The THM368020 can be used as well as 16,777,216 word by 18 bit by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20,·····, DQ17 and DQ35, respectively. THM368020 is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 8,388,608 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  8,492mW MAX. Operating (THMxxxxxx-60)
  7,172mW MAX. Operating (THMxxxxxx-70)
  132mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 2,048 Refresh cycles/16ms (Burst Refresh)
- 2,048 Refresh cycles/32ms (Distributed Refresh)
- Package
  Tin-Lead Contact: THM368020S-60,70
  Gold Contact: THM368020SG-60,70

KEY PARAMETERS

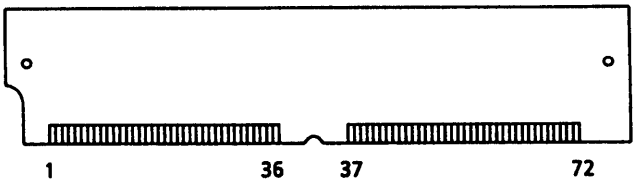
	-60	-70
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns
t_{AA} Column Address Access Time	30ns	35ns
t_{CAC} $\overline{CAS}$ Access Time	15ns	20ns
t_{RC} Cycle Time	110ns	130ns
t_{PC} Fast Page Mode Cycle Time	40ns	45ns

PIN NAMES

A0~A10	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

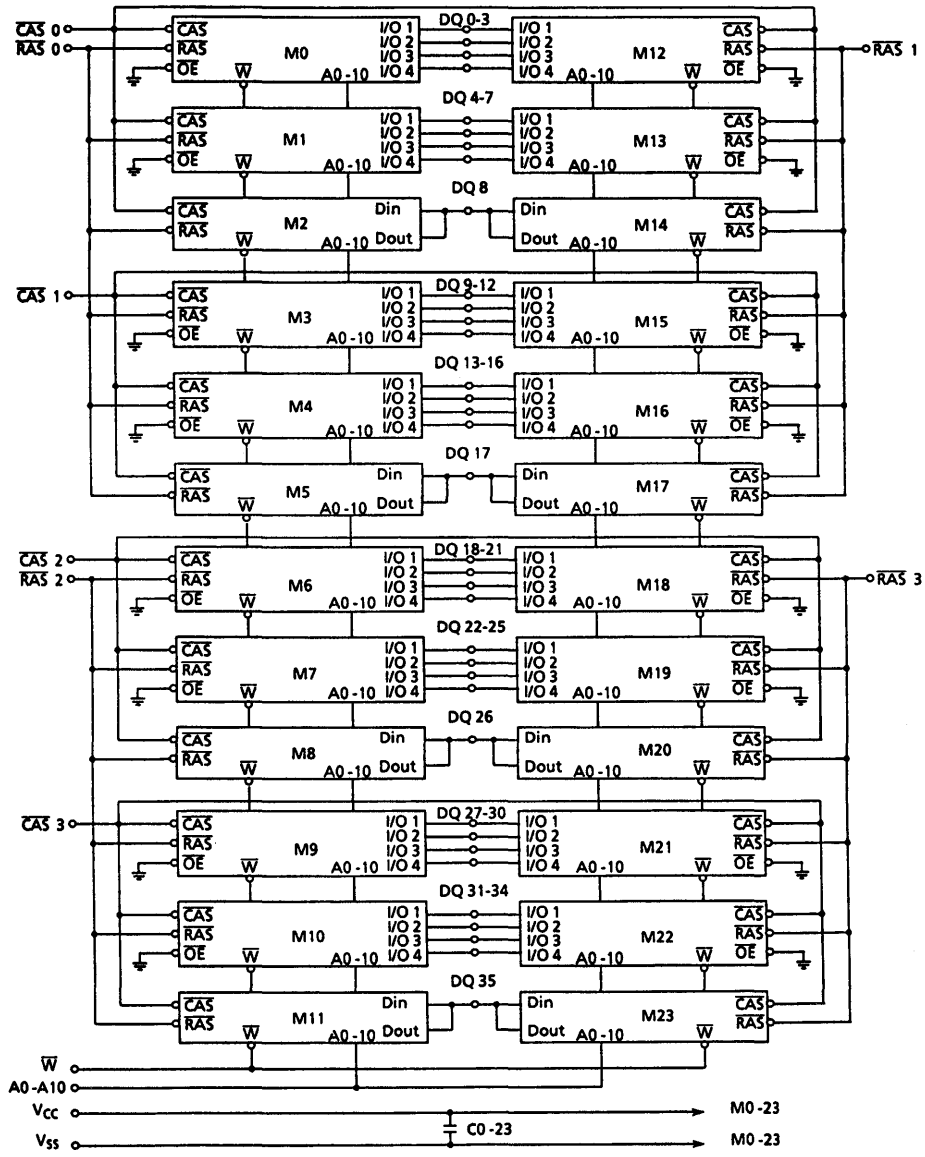
	-60	-70
PD0	NC	NC
PD1	V_{SS}	V_{SS}
PD2	NC	V_{SS}
PD3	NC	NC

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	14.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0*	-	0.8	V	2

*-2.0V at pulse width ≤ 20 ns

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1544	mA	3,4
		THMxxxxxx-70	-	1304		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			48	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1544	mA	3
		THMxxxxxx-70	-	1304		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	824	mA	3,4
		THMxxxxxx-70	-	744		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			24	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	1544	mA	3
		THMxxxxxx-70	-	1304		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-240	240	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 15. Notes which are referenced in this section are also located in the A.C. Conditions

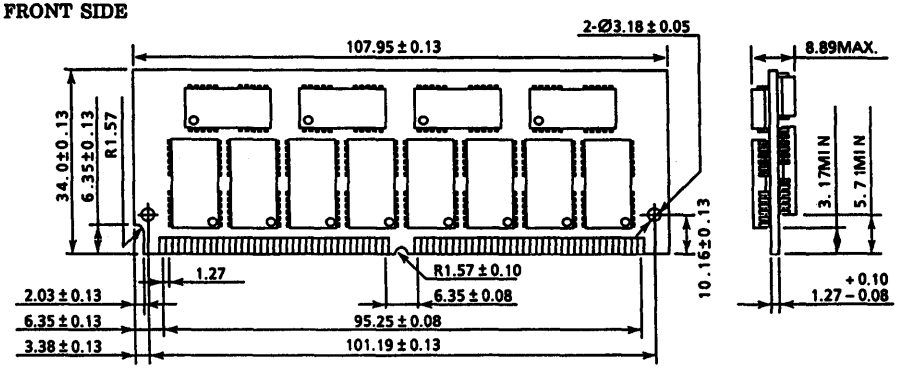
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A10)	-	88	pF
CI2	Input Capacitance ($\overline{W}$)	-	84	pF
CI3	Input Capacitance ($\overline{RAS0}$~$\overline{RAS3}$)	-	42	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	36	pF
CDQ1	I/O Capacitance (DQ0~7, 9~16, 18~25, 27~34)	-	17	pF
CDQ2	I/O Capacitance (DQ8, 17, 26, 35)	-	22	pF

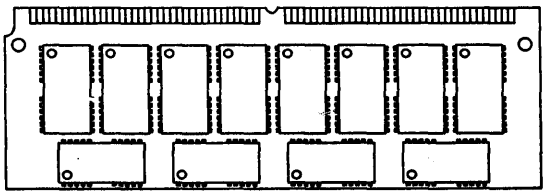
OUTLINE DRAWINGS

Unit in mm

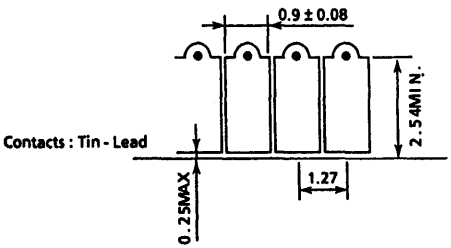
FRONT SIDE



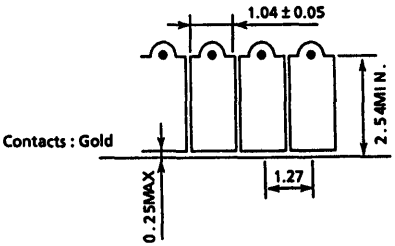
BACK SIDE



• THM368020S



• THM368020SG



8,388,608 WORD X 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM3680A0 is a 8,388,608 word by 36 bit dynamic RAM module which is assembled with 18 TC5116400J devices on the printed circuit board. This module is optimized for applications which require high density and large capacity such as main memory, image memory systems, and others which require compact size.

FEATURES

- 8,388,608 word by 36 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10%
- Low power
  4,555mW MAX. Operating (THMxxxxxx-60)
  4,059mW MAX. Operating (THMxxxxxx-70)
  99mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 4,096 Refresh cycles/64ms
- Package
  72pin SIMM Tin-Lead Contact: THM3680A0S-60,70
  72pin SIMM Gold Contact: THM3680A0SG-60,70

KEY PARAMETERS

	-60	-70
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns
t_{AA} Column Address Access Time	30ns	35ns
t_{CAC} $\overline{CAS}$ Access Time	15ns	20ns
t_{RC} Cycle Time	110ns	130ns
t_{PC} Fast Page Mode Cycle Time	40ns	45ns

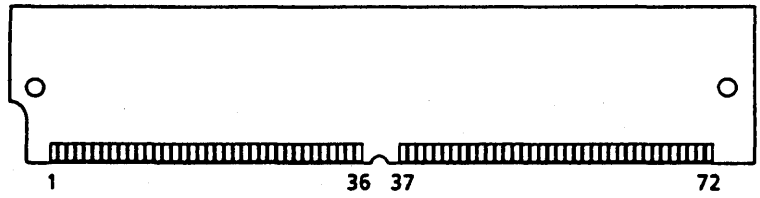
PIN NAMES

A0~A9 A10R, A11R	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CASØ}$, $\overline{CAST}$	Column Address Strobe
$\overline{RASØ}$, $\overline{RAST}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
PD	Presence Detect Pin

	-60	-70
PD0	NC	NC
PD1	V_{SS}	V_{SS}
PD2	NC	V_{SS}
PD3	NC	NC
PD4	V_{SS}*	V_{SS}*

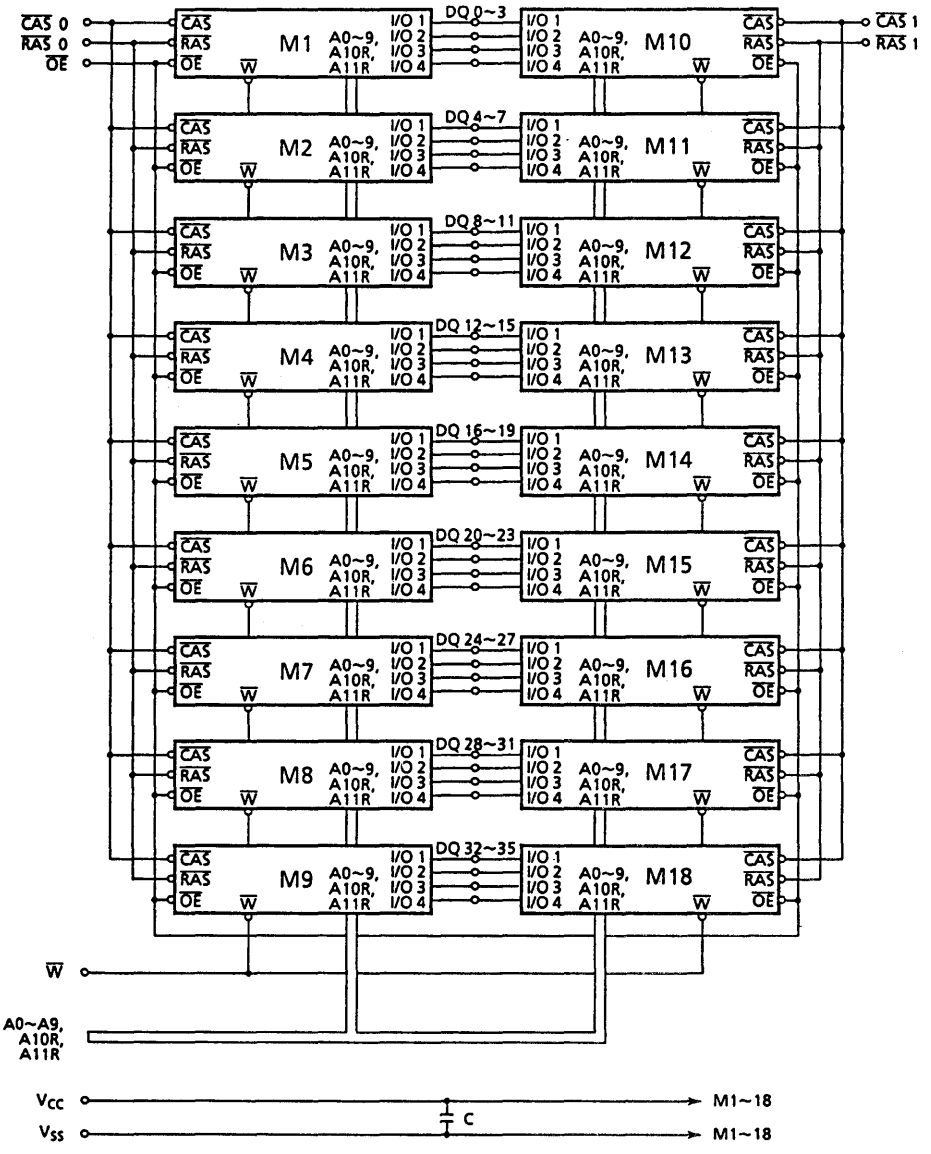
* Through the resistor (2.6KΩ) to GND.

PIN CONNECTION (TOP VIEW)



1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	NC
5	DQ3	17	A5	29	DQ16	41	A10R	53	DQ26	65	NC
6	DQ4	18	A6	30	V_{CC}	42	A11R	54	DQ27	66	NC
7	DQ5	19	$\overline{OE}$	31	A8	43	$\overline{CAS1}$	55	DQ28	67	PD0
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS0}$	56	DQ29	68	PD1
9	DQ7	21	DQ9	33	NC	45	$\overline{RAS1}$	57	DQ30	69	PD2
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD3
11	PD4	23	DQ11	35	DQ17	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ12	36	DQ18	48	V_{SS}	60	DQ32	72	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	— 1.0~7.0	V	1
Output Voltage	V_{OUT}	— 1.0~7.0	V	1
Power Supply Voltage	V_{CC}	— 1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	— 55~125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	12.6	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input HighVoltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0*	-	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	828	mA	3,4 5
		THMxxxxxx-70	-	738		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			36	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	828	mA	3,5
		THMxxxxxx-70	-	738		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$,Address Cycling:t_{PC}=t_{PC} MIN.)	THMxxxxxx-60	-	648	mA	3,4 5
		THMxxxxxx-70	-	558		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			18	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	THMxxxxxx-60	-	828	mA	3,5
		THMxxxxxx-70	-	738		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≤V_{IN}≤6.5V, All Other Pins Not Under Test=0V)		-180	180	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤V_{OUT}≤5.5V)		-20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}= -5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

Please refer to the DRAM Module A.C. Conditions No. 13. Notes which are referenced in this section are also located in the A.C. Conditions.

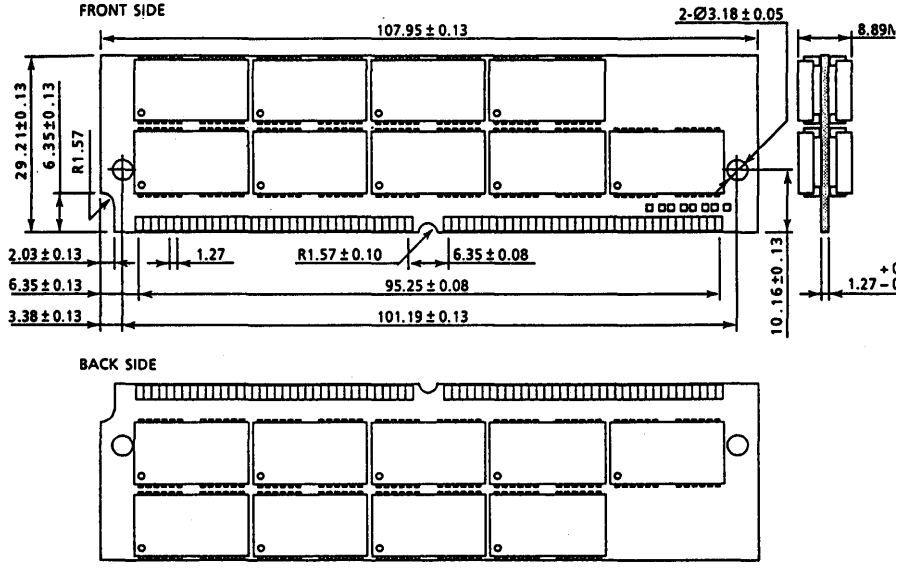
CAPACITANCE (V_{CC} = 5V ± 10%, f= 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
CI1	Input Capacitance (A0~A9, A10R, A11R)	-	161	pF
CI2	Input Capacitance ($\overline{W}$, $\overline{OE}$)	-	168	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS1}$)	-	42	pF
CI4	Input Capacitance ($\overline{CAS0}$, $\overline{CAS1}$)	-	42	pF
CDQ	I/O Capacitance (DQ0~35)	-	29	pF

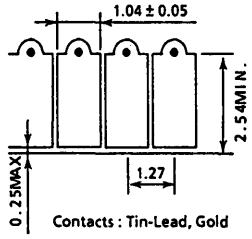
OUTLINE DRAWINGS

THM3680A0S/SG

Unit : mm



DETAIL OF CONTACTS • THM3680A0S/SG



Weight : 31.5g (Typ.)

DRAM Module A.C. Conditions No.4
1Mx4/1Mx1-Based Modules

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	9,13
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	20	ns	9,13
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	-	55	-	60	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	-	55	-	60	-	ns	

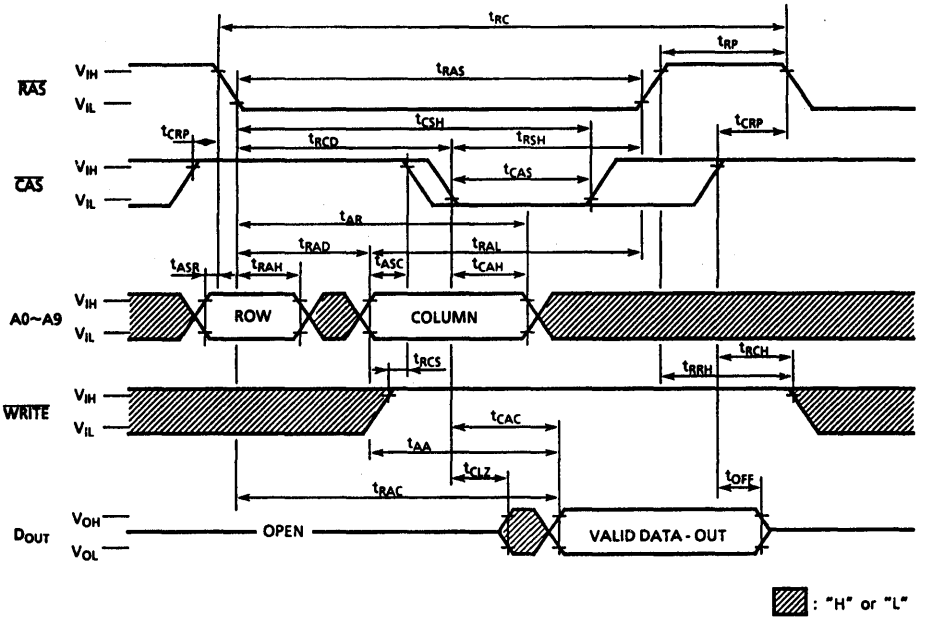
ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	15	-	15	-	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	-	55	-	60	-	ns	-
t_{REF}	Refresh Period	-	16	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	-	40	-	40	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	10		ns	

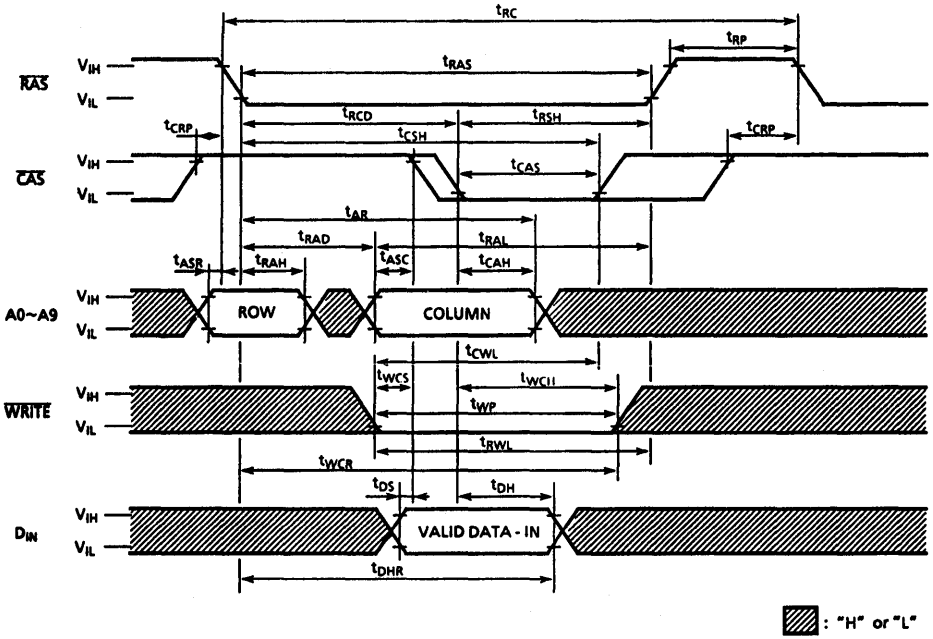
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume t_T=5ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. t_{WCS} is not a restictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

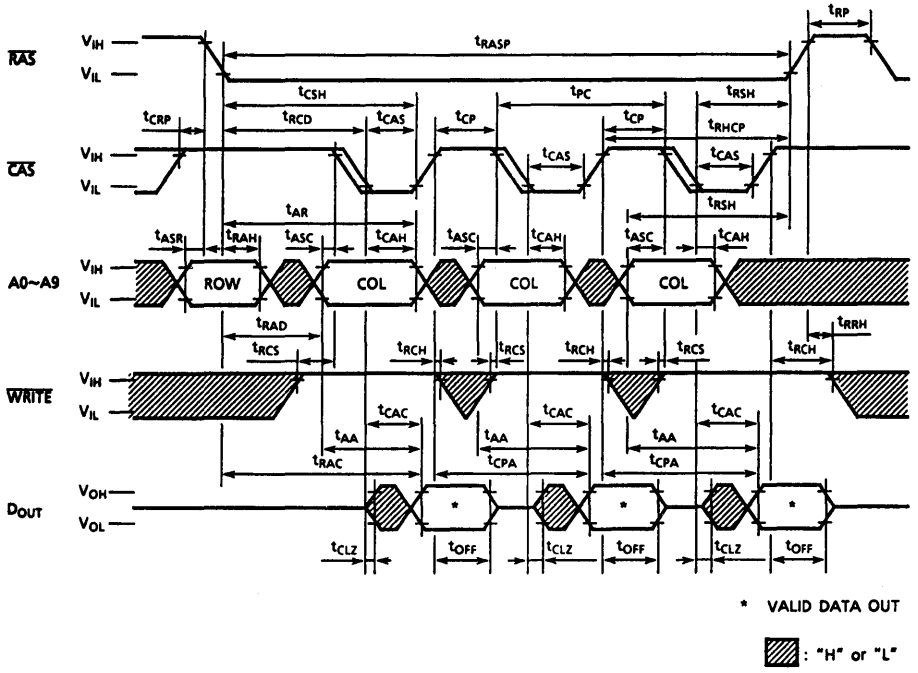
READ CYCLE



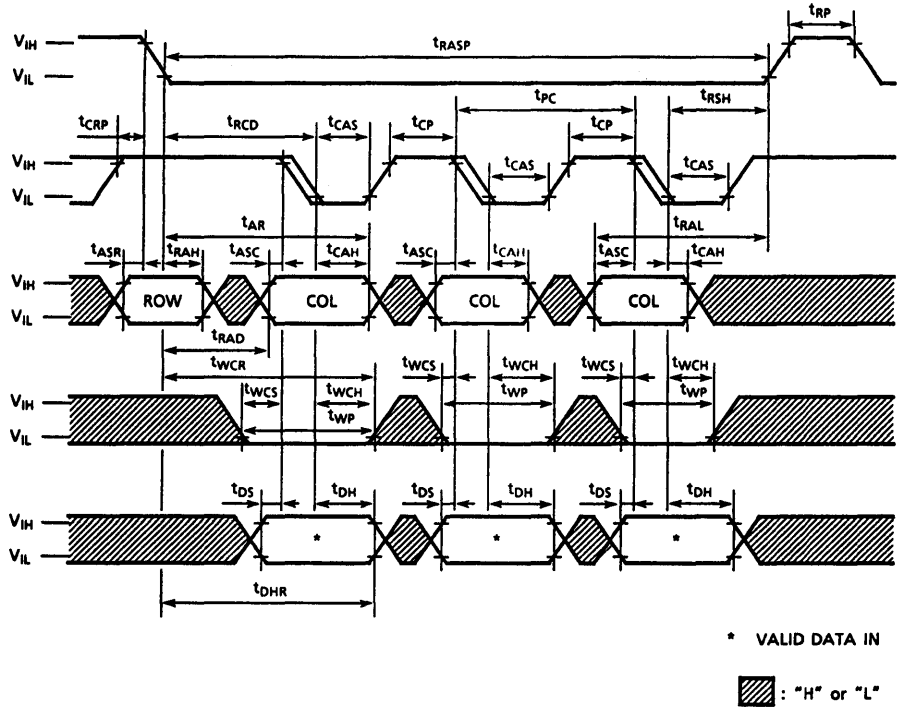
WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ CYCLE

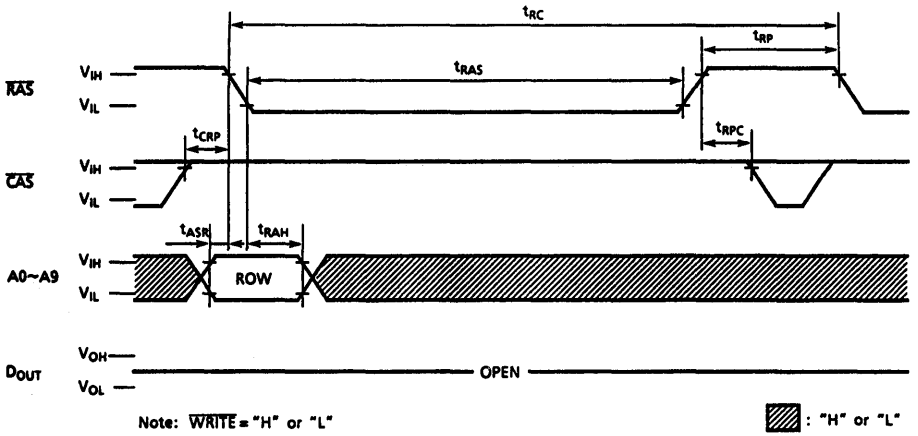


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



DRAM Module A.C. Conditions No.4
1Mx4/1Mx1-Based Modules

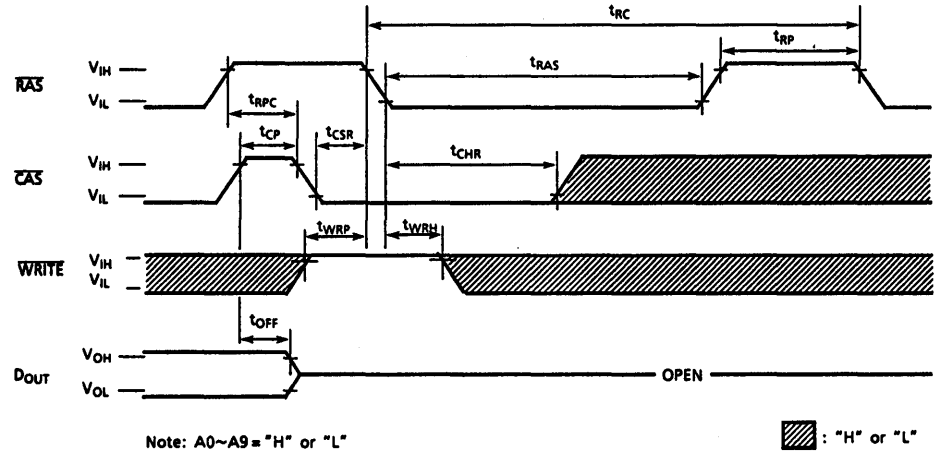
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$ = "H" or "L"

▨ : "H" or "L"

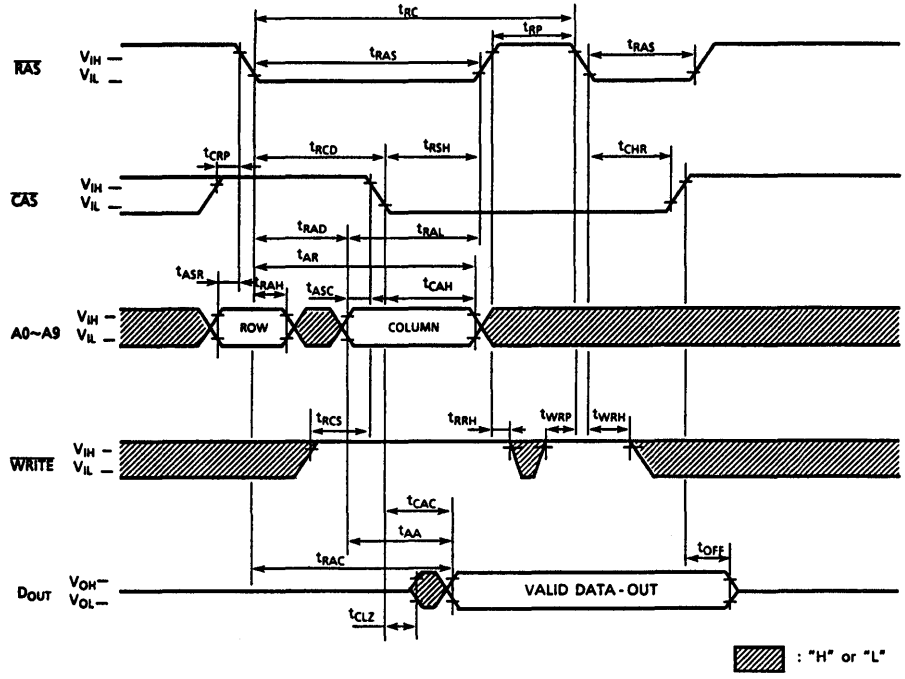
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



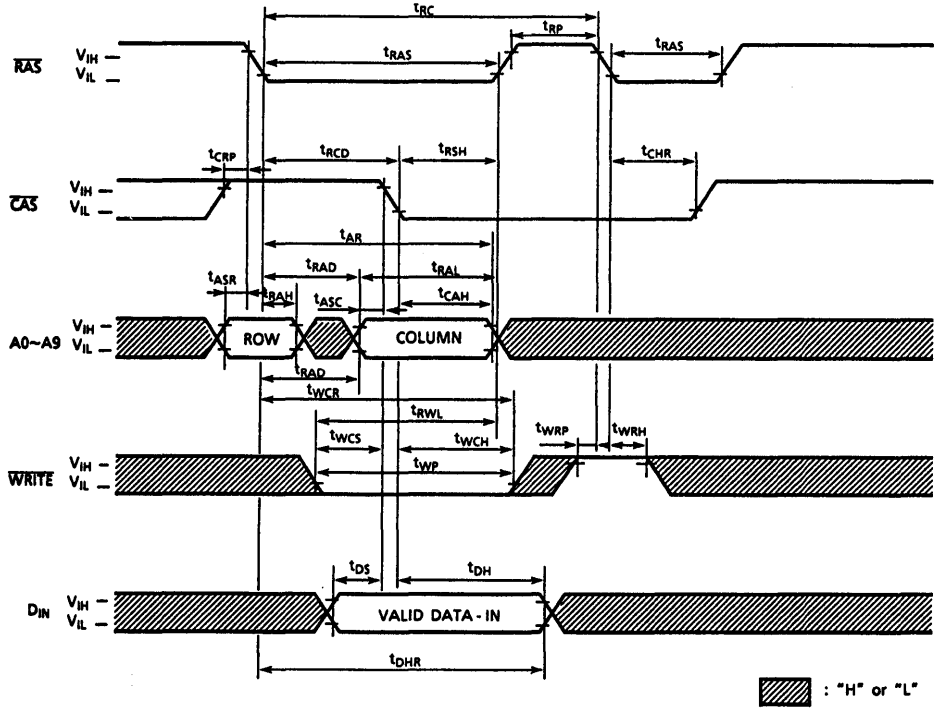
Note: A0~A9 = "H" or "L"

▨ : "H" or "L"

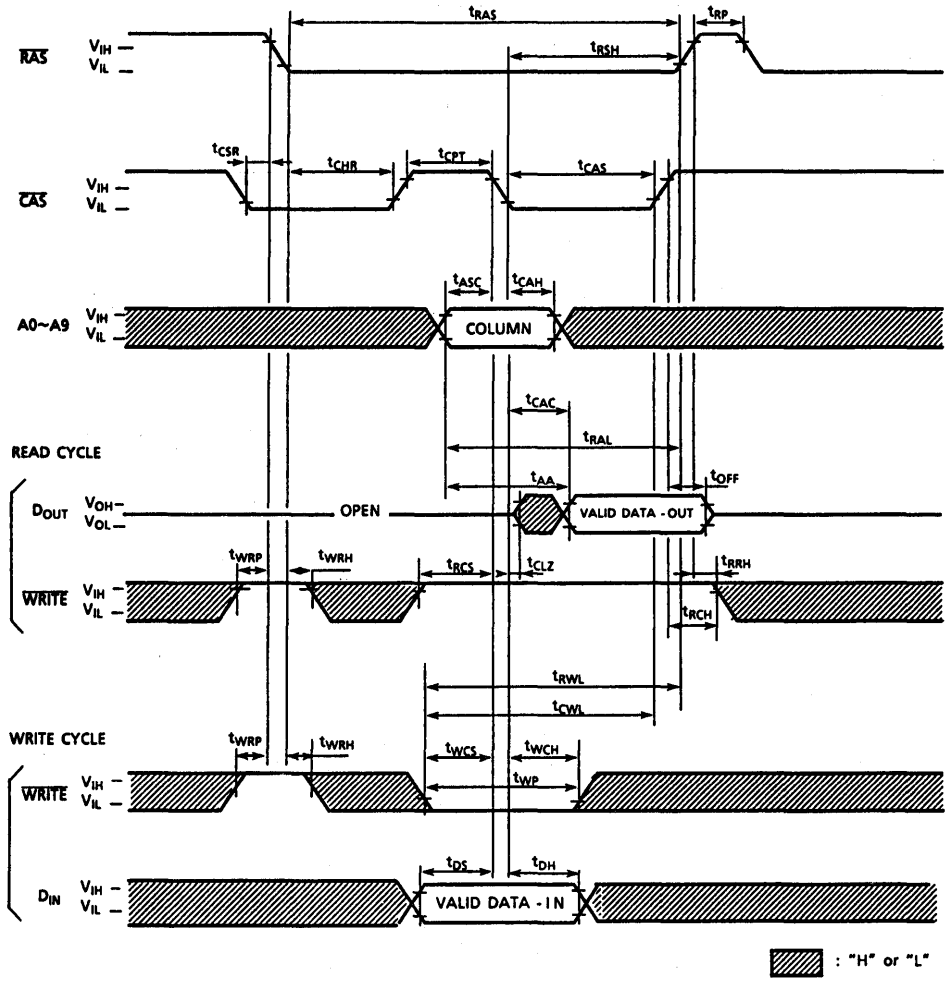
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DRAM Module A.C. Conditions No.8
1Mx4-Based Modules

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	9,13
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	20	ns	9,13
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	
t_{DH}	Data Hold Time	15	-	15	-	15	-	ns	
t_{REF}	Refresh Period	-	16	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	-	40	-	40	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	10		ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	10		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE (V_{CC} = 5V ± 10%,Ta = 0~70°C) (Notes 6,7,8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	155	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	50	-	55	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	-	85	ns	9,13, 14
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	25	ns	9,13
t_{AA}	Access Time from Column Address	-	35	-	40	-	45	ns	9,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	45	-	50	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	85	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	85	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	85	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	-	45	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	45	-	ns	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

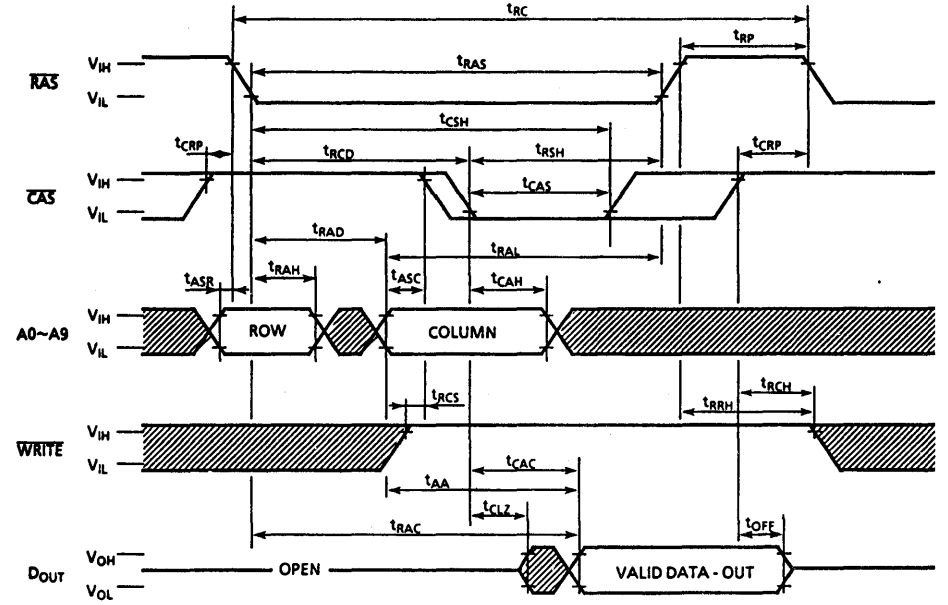
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

12. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWP} > t_{CPWDD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

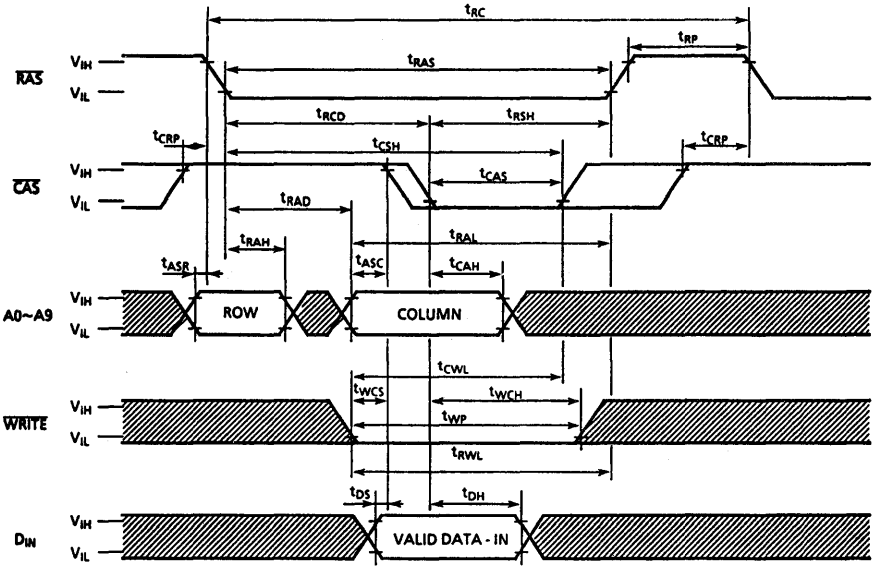
14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

READ CYCLE



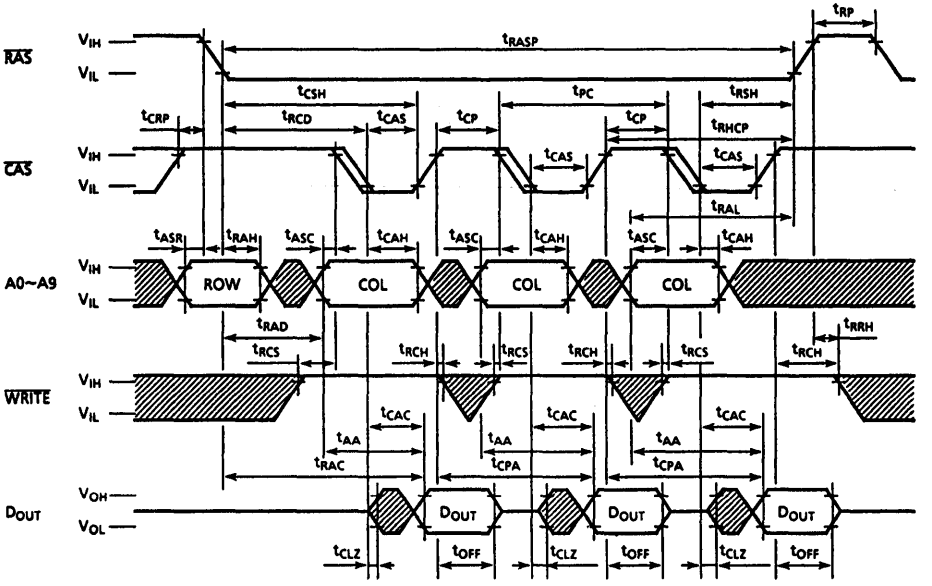
: "H" or "L"

WRITE CYCLE (EARLY WRITE)



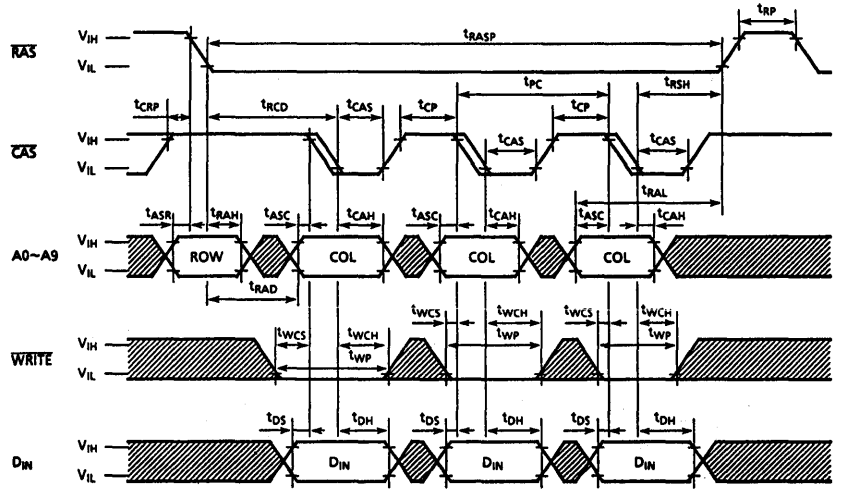
: "H" or "L"

FAST PAGE MODE READ CYCLE



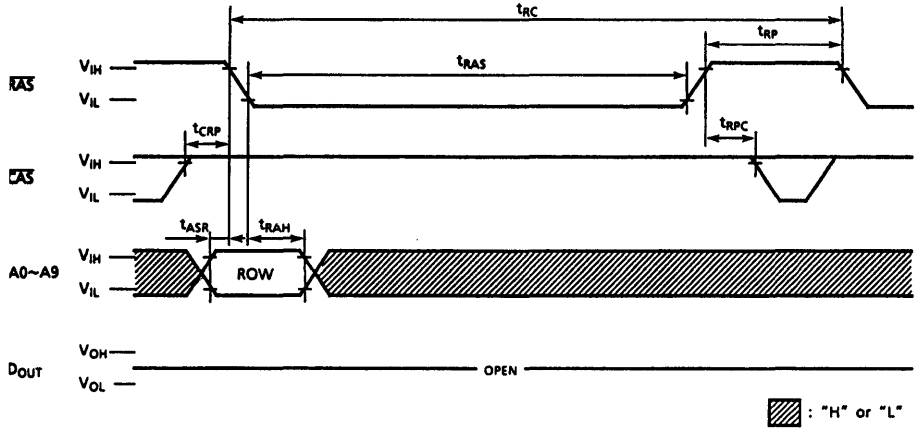
: "H" or "L"

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



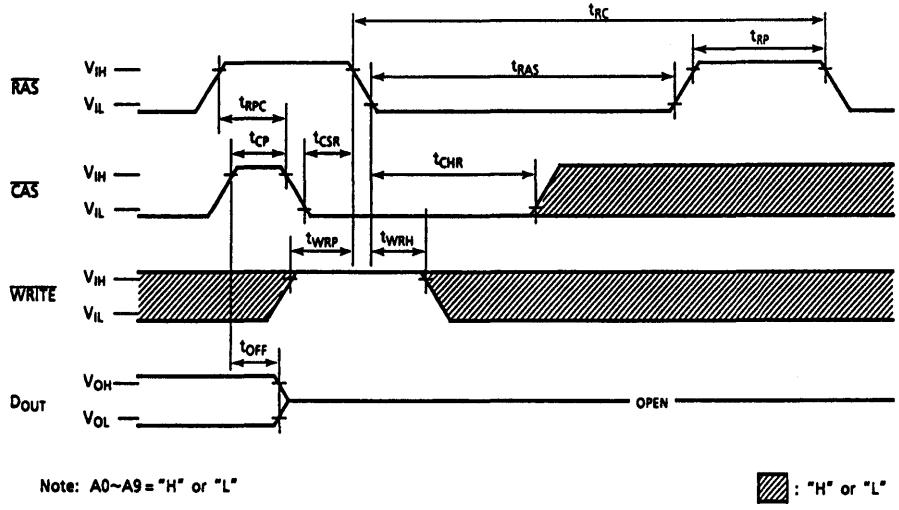
: "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



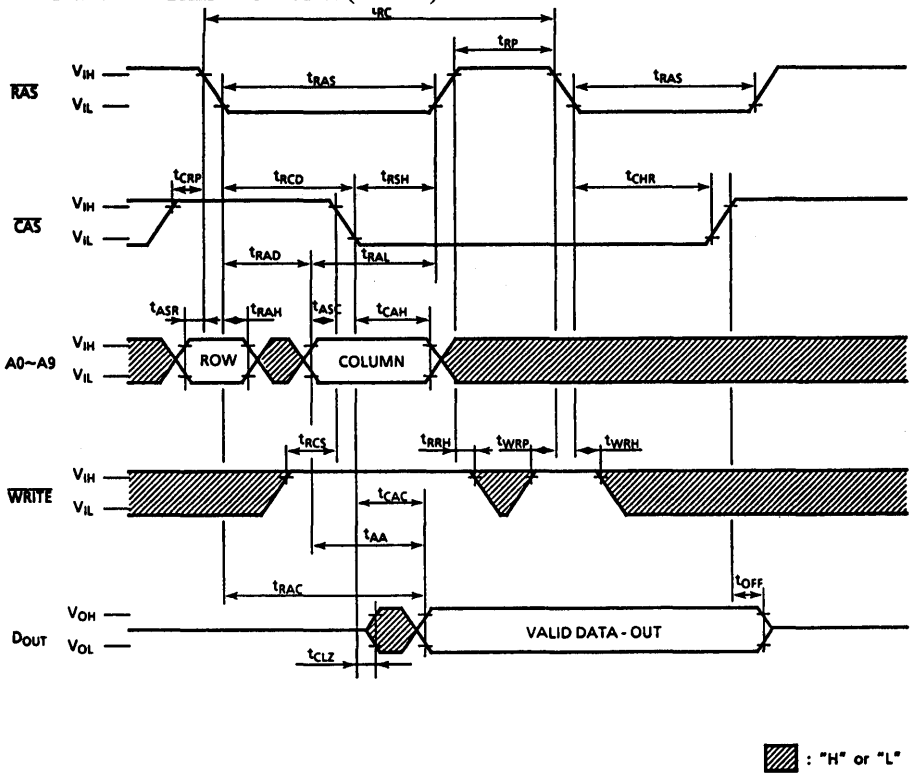
Note: $\overline{WRITE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

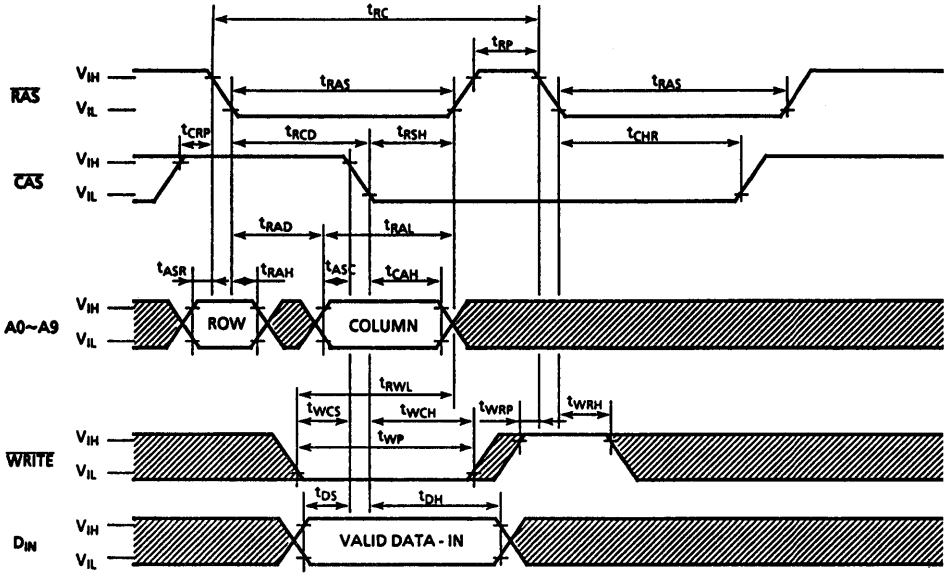


Note: A0~A9 = "H" or "L"

HIDDEN REFRESH CYCLE (READ)

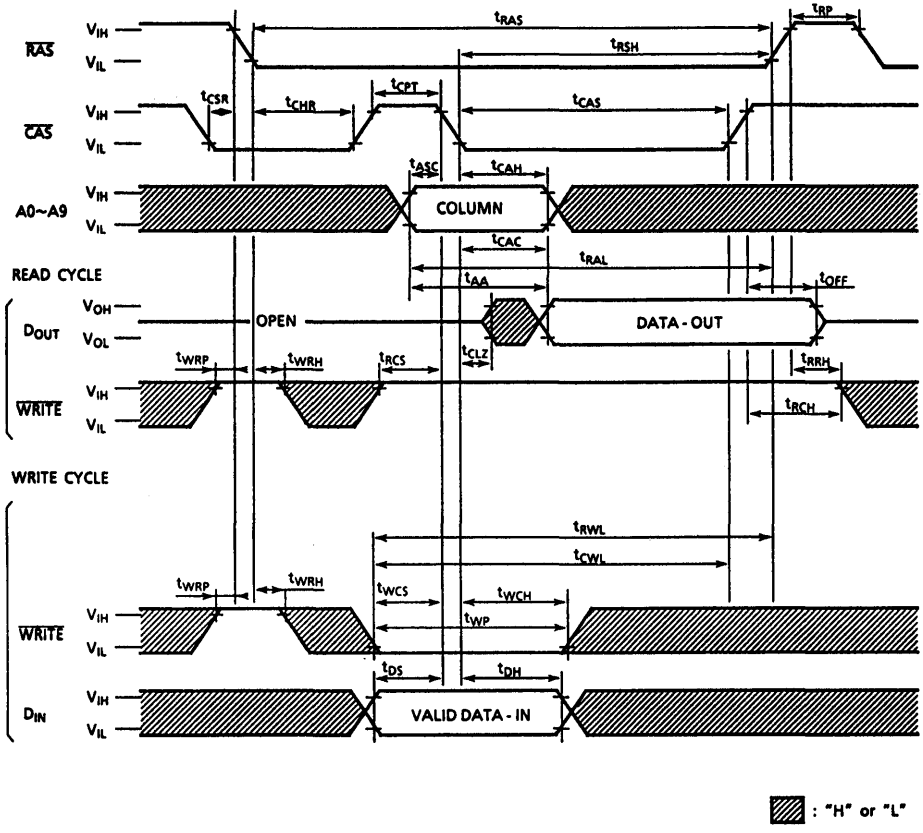


HIDDEN REFRESH CYCLE (WRITE)

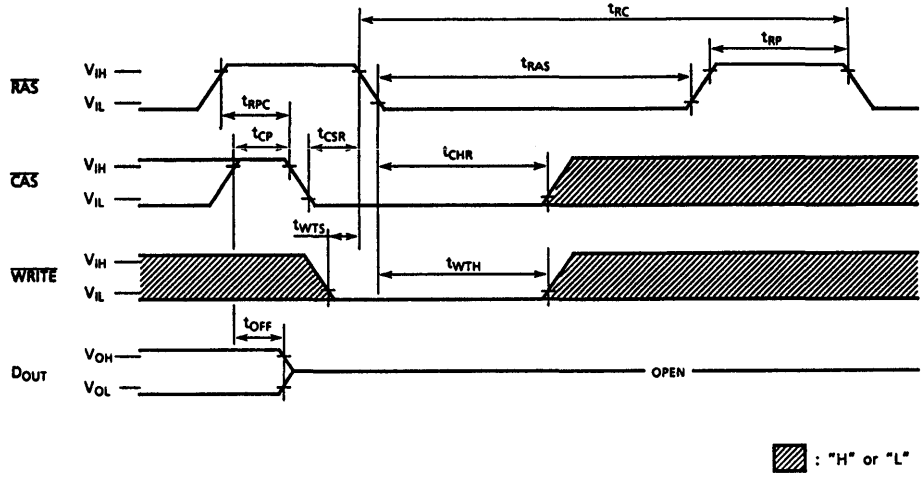


: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

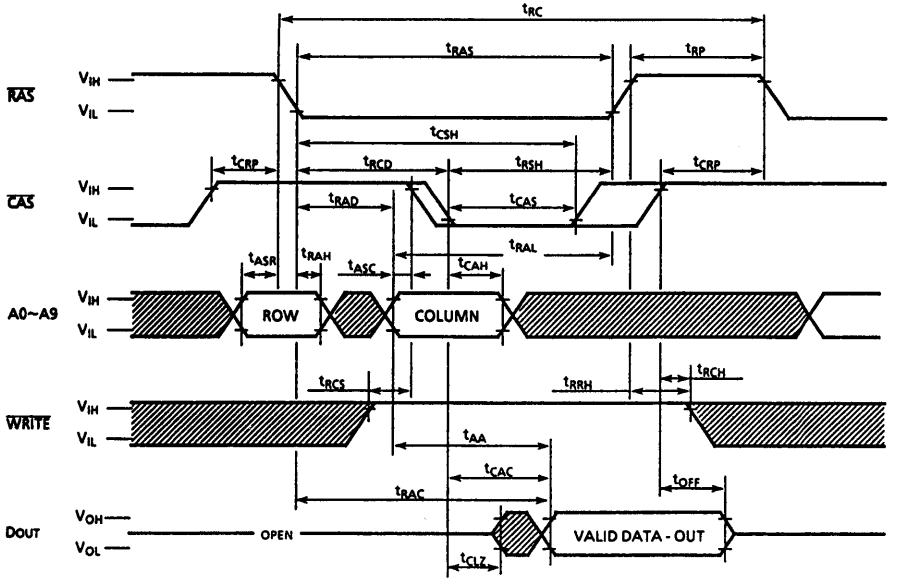


WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, A0~A9 = "H" or "L"

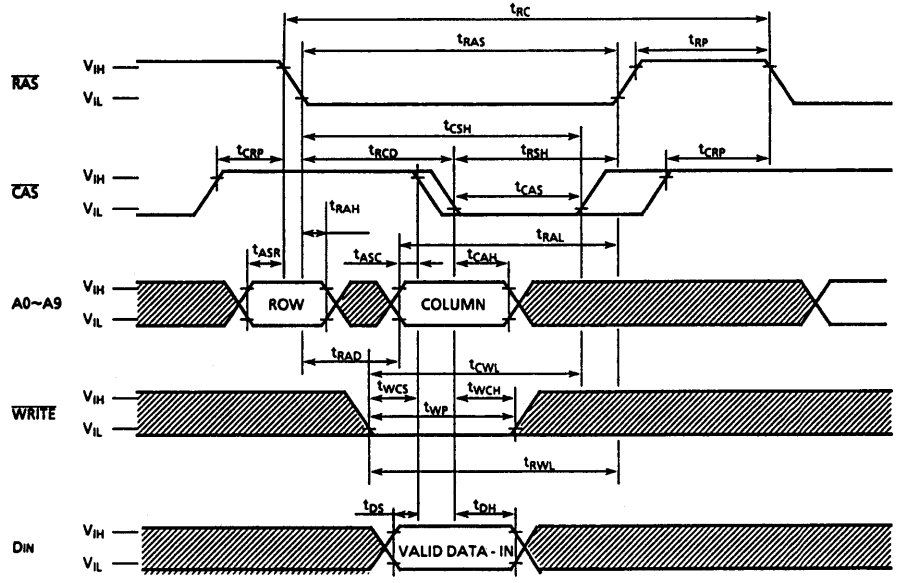
READ CYCLE IN THE TEST MODE



Note: D_{IN} = OPEN

▨ : "H" or "L"

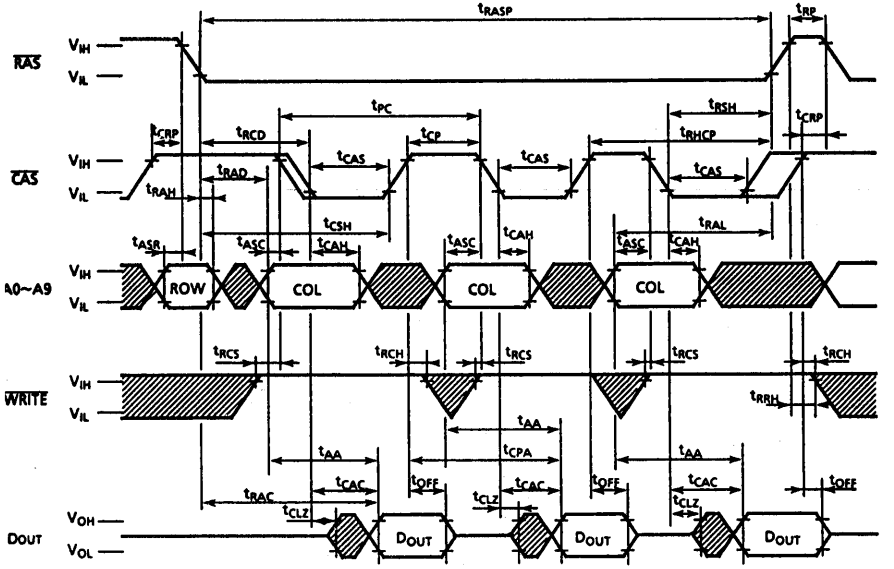
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note: D_{OUT} = OPEN

▨ : "H" or "L"

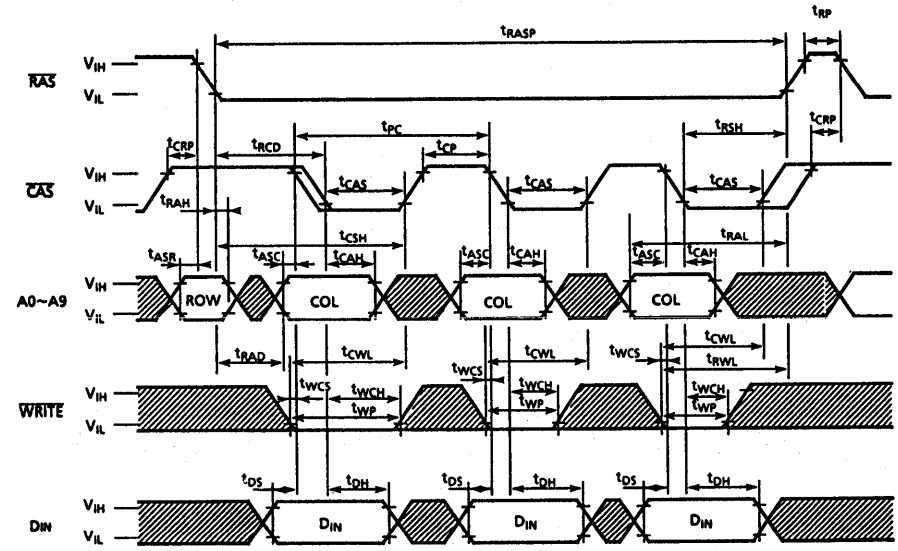
FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note: D_{IN} = OPEN

▨ : "H" or "L"

FAST PAGE MODE WRITE CYCLE IN THE TEST MODE



Note: D_{OUT} = OPEN

▨ : "H" or "L"

TEST MODE

The TC514400AJ is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{0C} is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a"1".

If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514400AJ. In "Test Mode", the 1MX4 DRAM can be tested as if it were a 512K X 4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

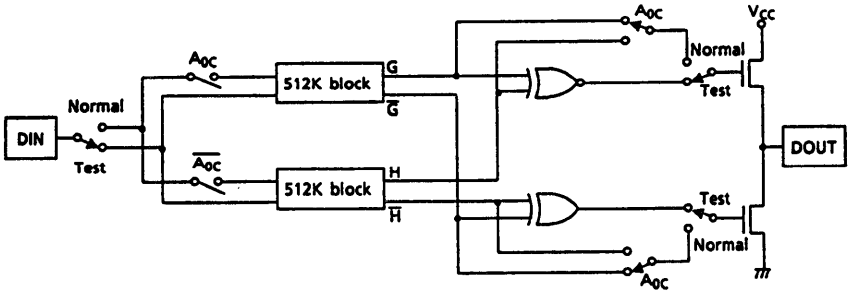


Figure 1

DRAM Module A.C. Conditions No.11
1Mx4-Based Module, with Output Enable

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	165	-	185	-	205	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	-	100	-	105	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	0	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	12
t_{DH}	Data Hold Time	15	-	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	16	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	50	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	90	-	100	-	110	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	-	65	-	70	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	70	-	70	-	75	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	-	40	-	40	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ to Access Time	-	20	-	20	-	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	20	-	ns	
t_{OEZ}	Ouput buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	20	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	0	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	10		ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	10		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE (V_{CC} = 5V ± 10%,Ta = 0~70°C) (Notes 6,7,8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	155	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	50	-	55	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	-	85	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	-	45	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	45	-	50	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	85	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	85	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	85	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	45	-	45	-	50	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	45	-	ns	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.

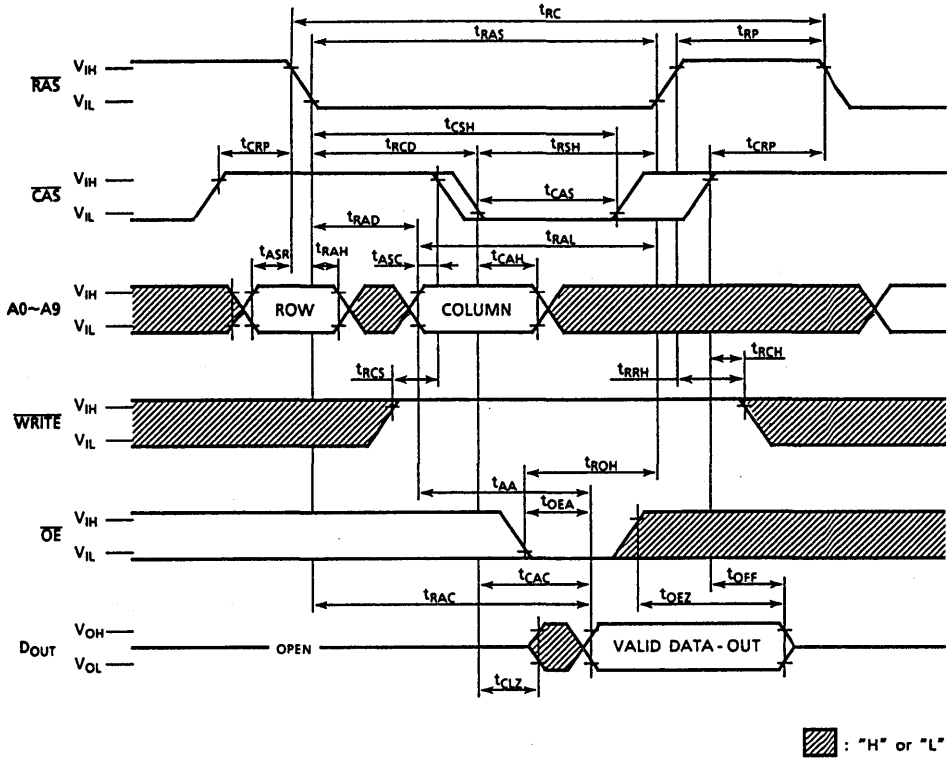
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} > t_{RWD}$ (min.), $t_{CWD} > t_{CWD}$ (min.), $t_{AWD} > t_{AWD}$ (min.) and $t_{CPWP} > t_{CPWDD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

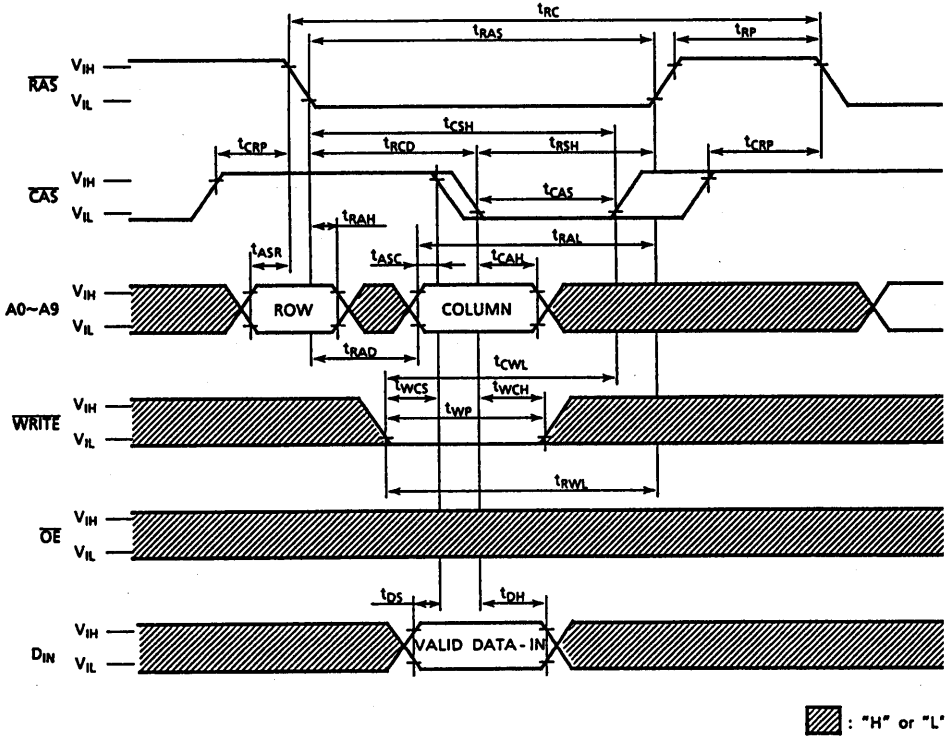
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

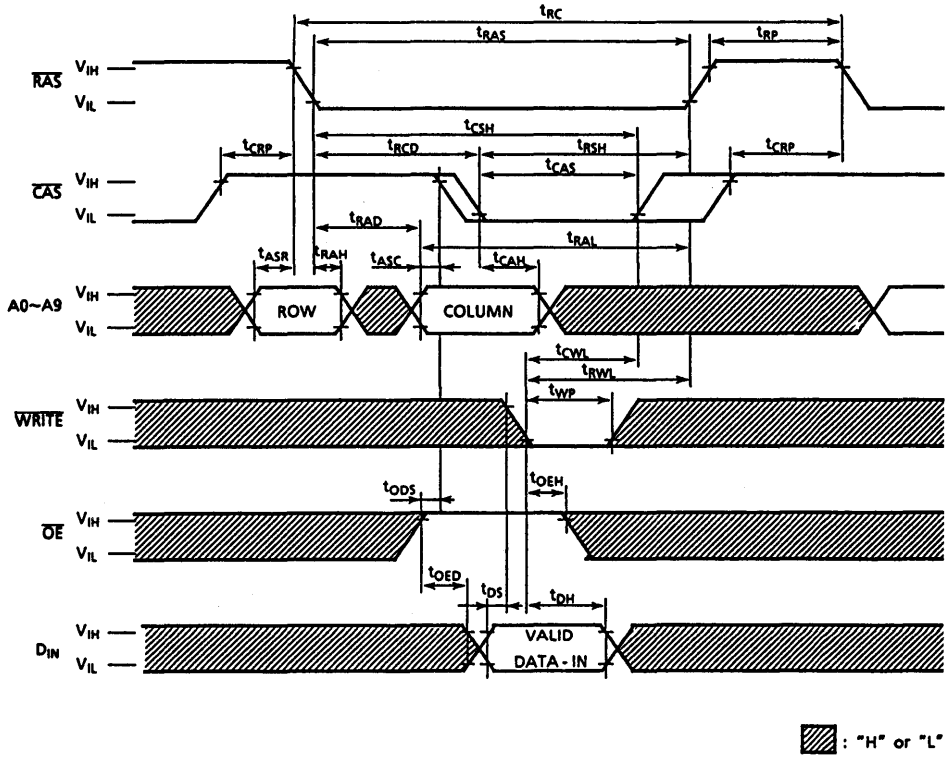
READ CYCLE



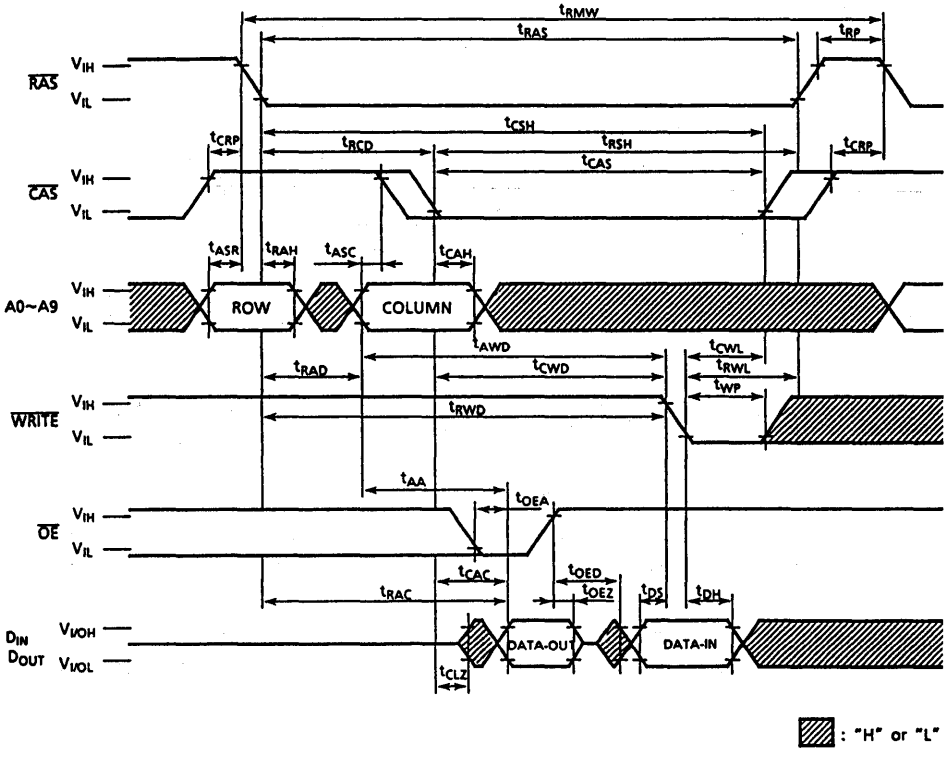
WRITE CYCLE (EARLY WRITE)



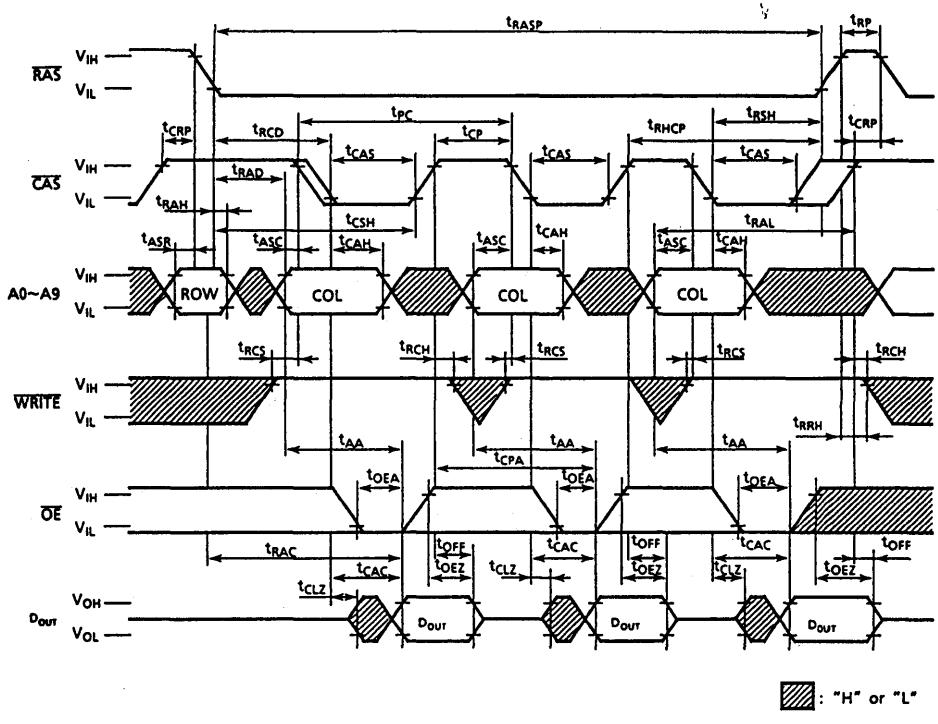
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



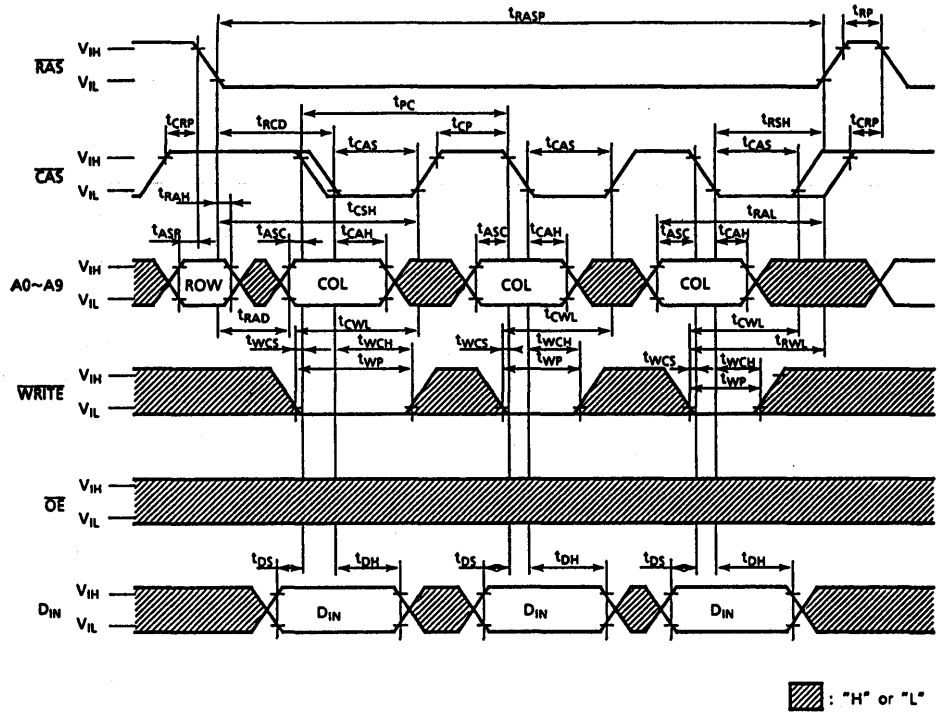
READ-MODIFY-WRITE CYCLE



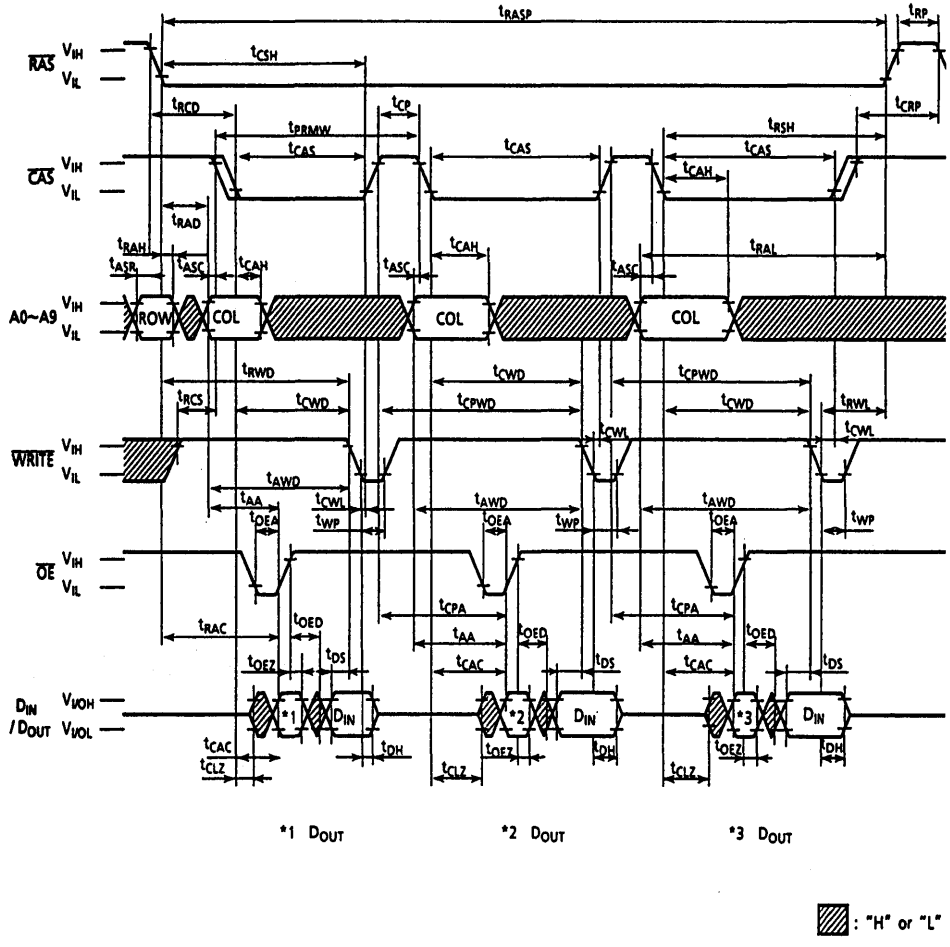
FAST PAGE MODE READ CYCLE



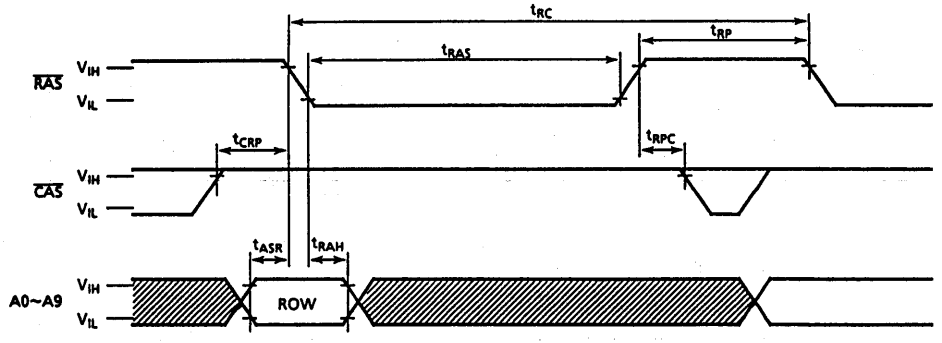
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



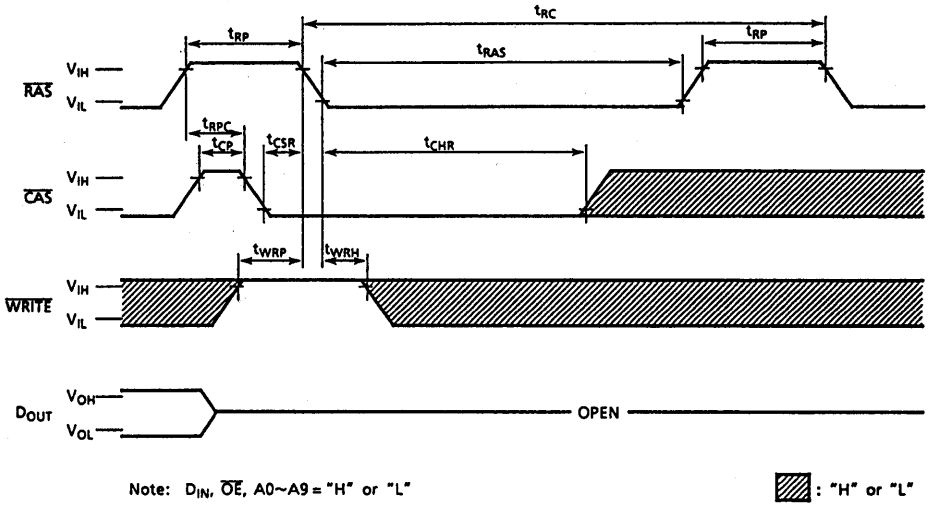
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

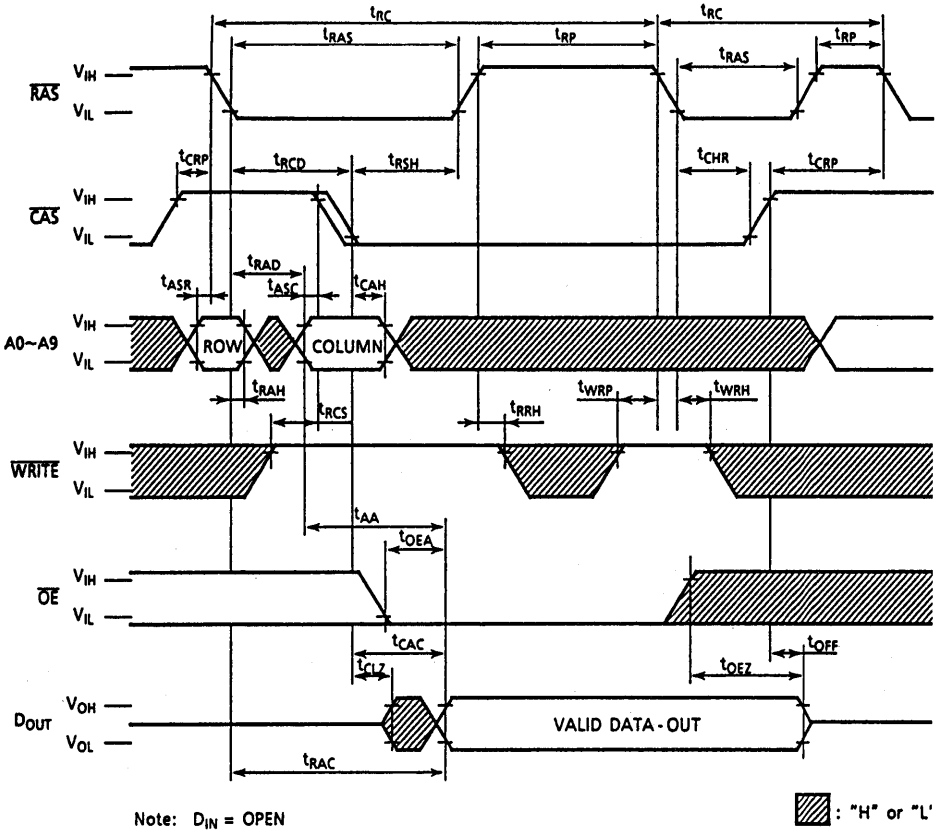
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

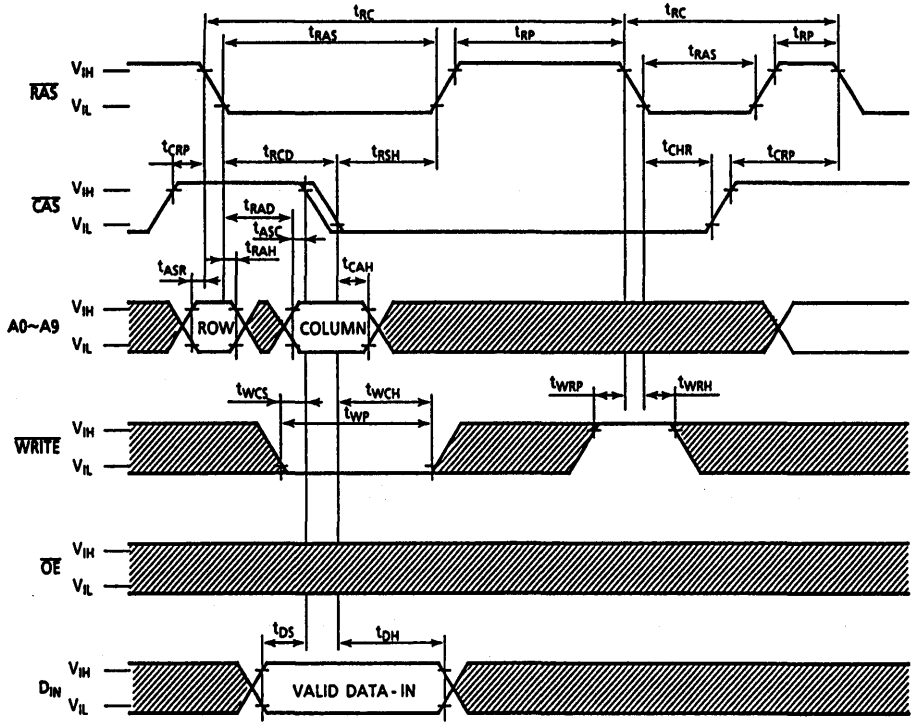
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨: "H" or "L"

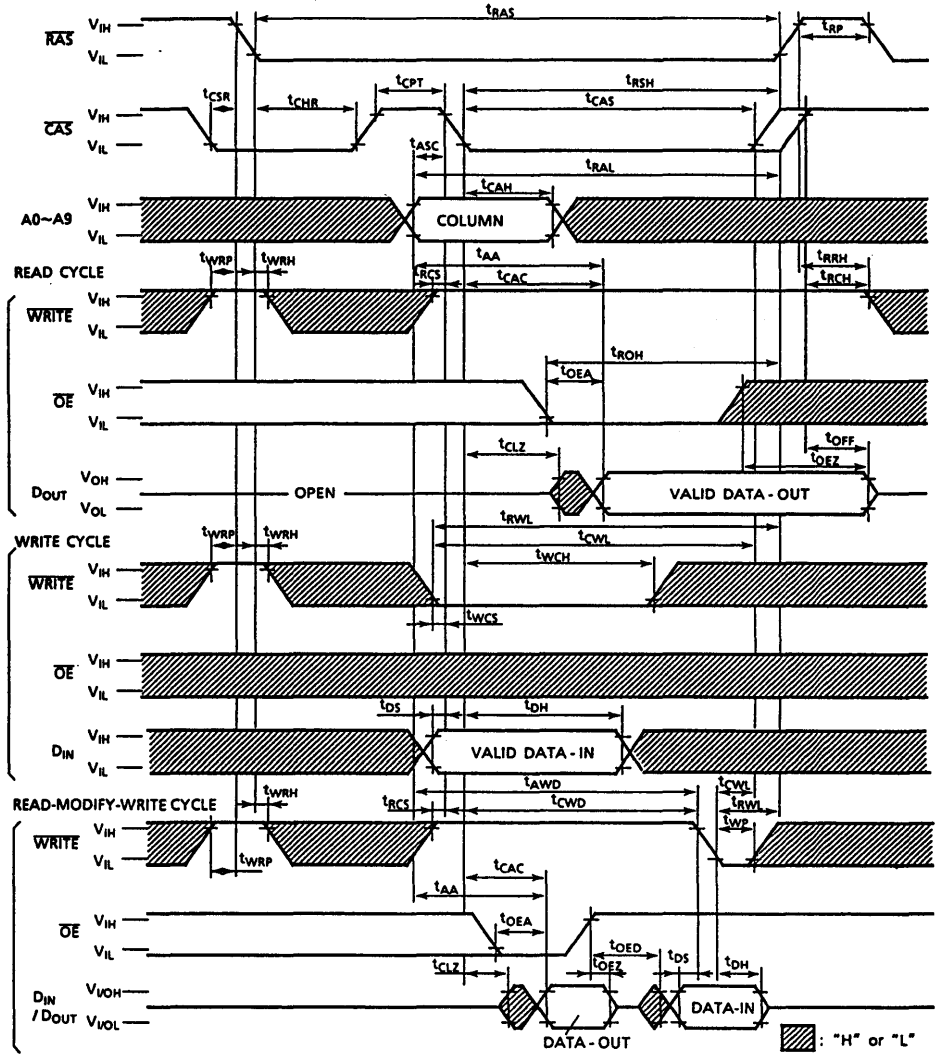
HIDDEN REFRESH CYCLE (WRITE)



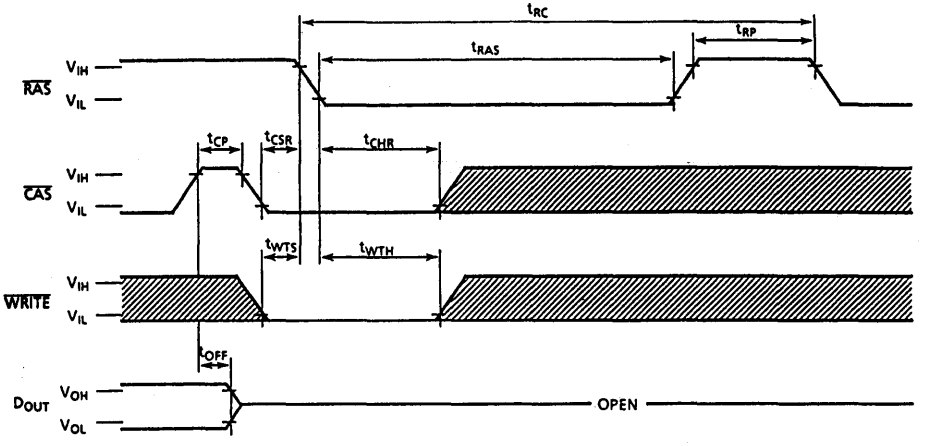
Note: D_{OUT} = OPEN

▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



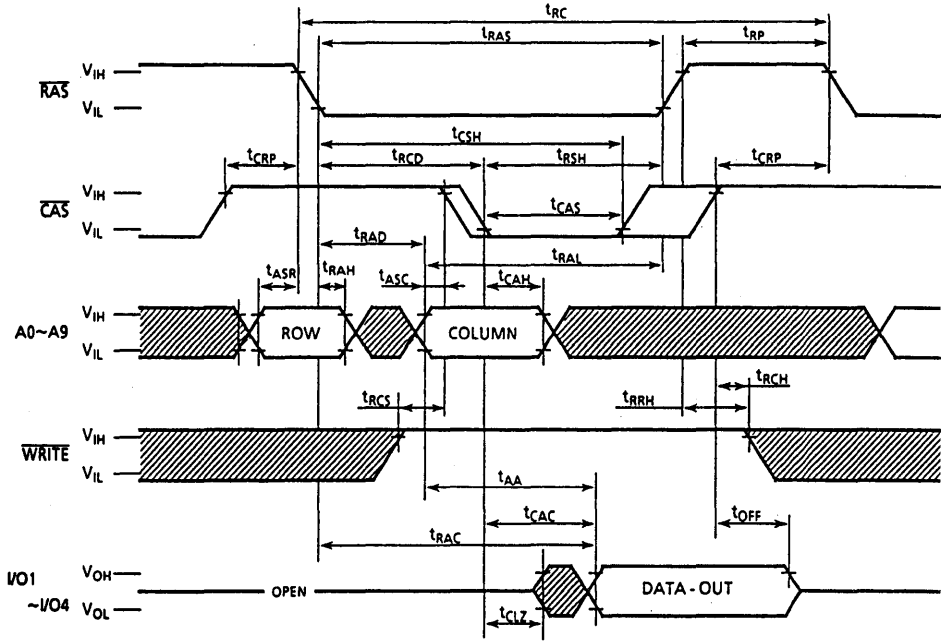
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A9 = "H" or "L"

▨ : "H" or "L"

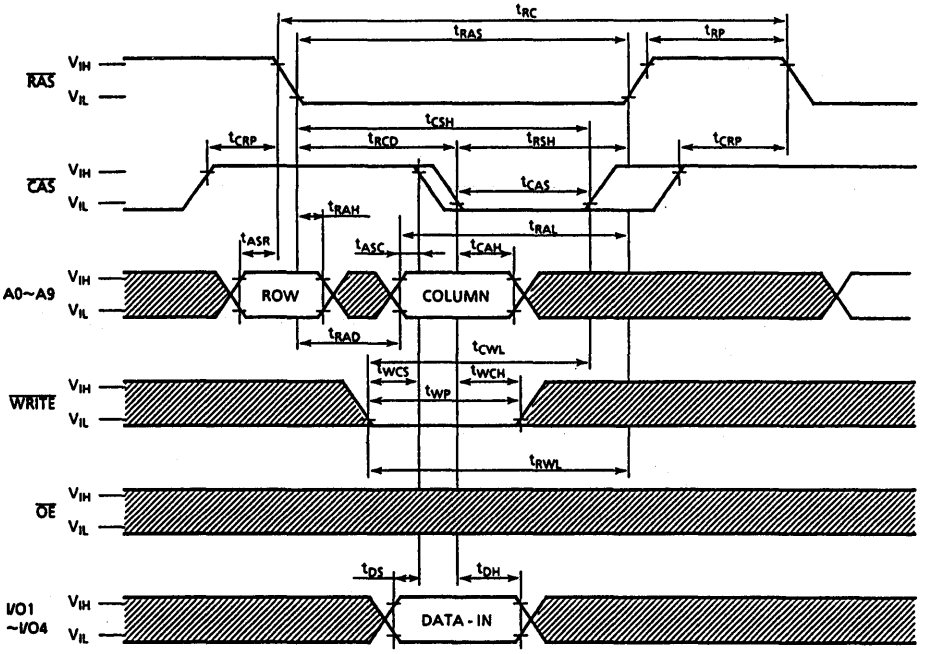
READ CYCLE IN THE TEST MODE



Note : $\overline{OE}$="L", D_{IN}=OPEN

▨ : "H" or "L"

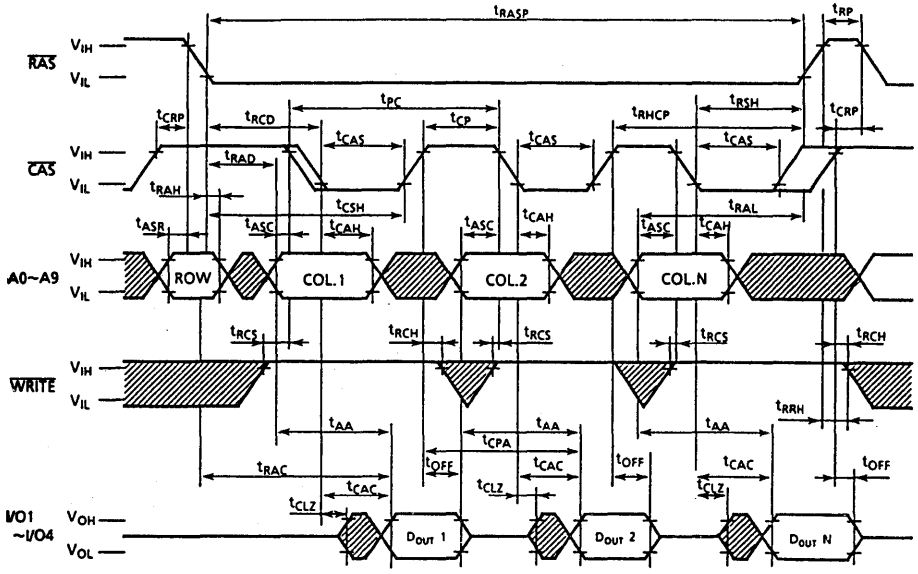
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note : D_{OUT} = OPEN

▨ : "H" or "L"

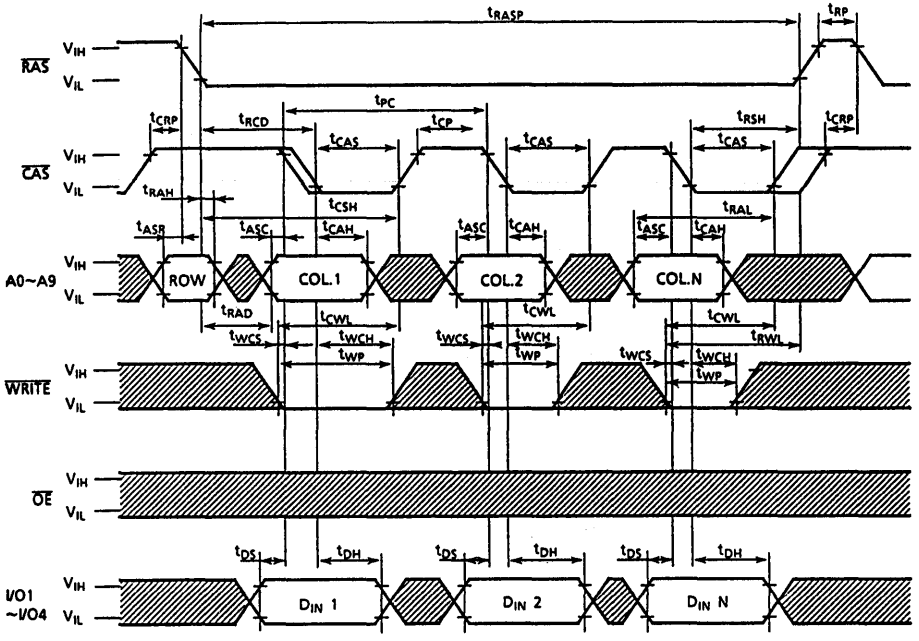
FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note : $\overline{OE}$="L", D_{IN}=OPEN

▨ : "H" or "L"

FAST PAGE MODE WRITE CYCLE IN THE TEST MODE



Note : D_{OUT} = OPEN

▨ : "H" or "L"

TEST MODE

The TC514400AJ/ASJ/AFT/ATR is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{0C} is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a"1".

If they were not equal, the I/O pin would indicate a "0". Fig. 1 shows the block diagram of TC514400AJ/ASJ/AFT/ATR. In "Test Mode", the 1MX4 DRAM can be tested as if it were a 512K X 4 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or "$\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/2 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

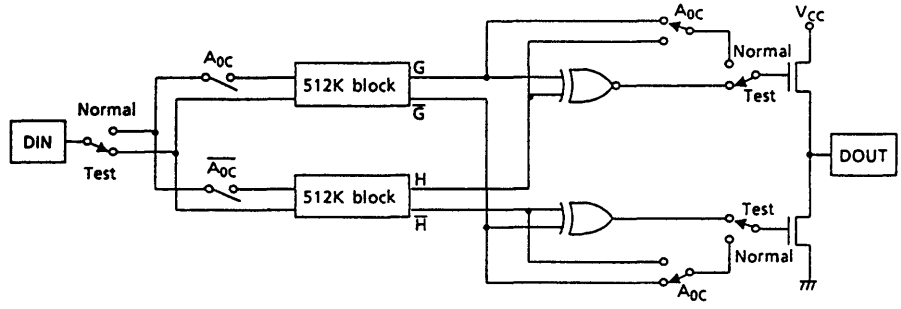


Figure 1

DRAM Module A.C. Conditions No.12
1Mx4/1Mx1 TSOP-Based Modules

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	9,13
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	20	ns	9,13
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	-	55	-	60	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	-	55	-	60	-	ns	

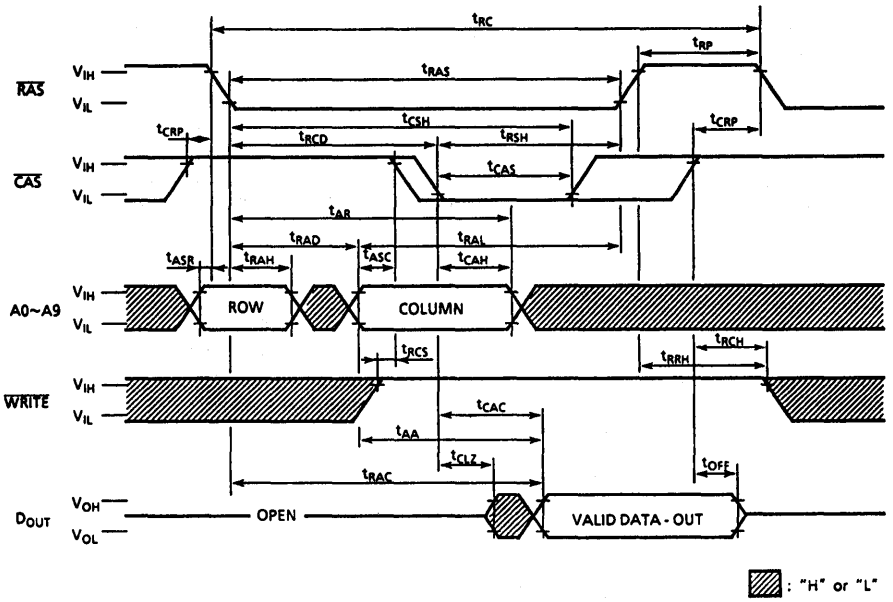
ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	
t_{DH}	Data Hold Time	15	-	15	-	15	-	ns	
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	-	55	-	60	-	ns	
t_{REF}	Refresh Period	-	16	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	-	40	-	40	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	10		ns	

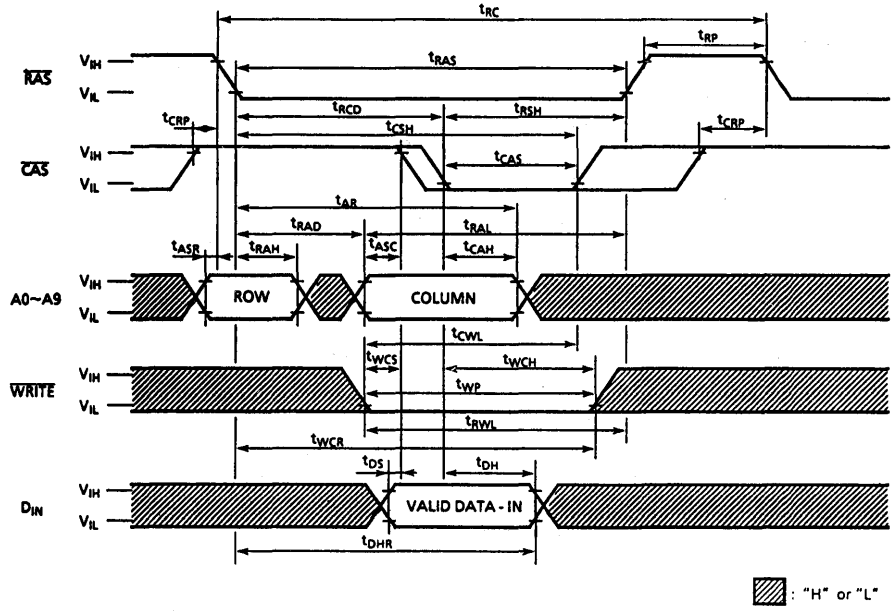
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume t_T=5ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. t_{WCS} is not a restictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

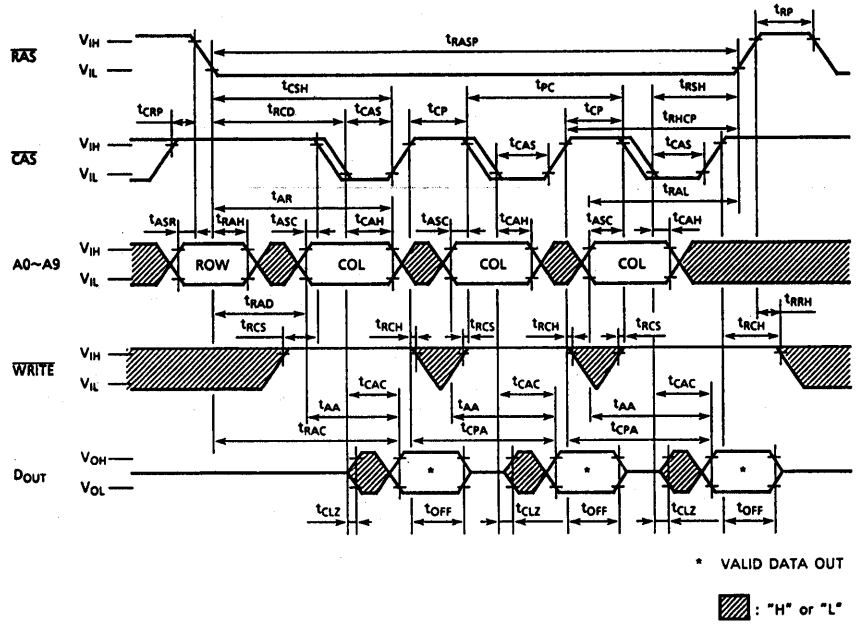
READ CYCLE


tRC
tRP
RAS
VIH
VIL
tRAS
tCSH
tRSH
tCRP
tRCD
tCRP
CAS
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
ROW
COLUMN
tRCS
tRCH
tRRH
WRITE
tCAC
tAA
tCLZ
tOFF
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA - OUT
: "H" or "L"

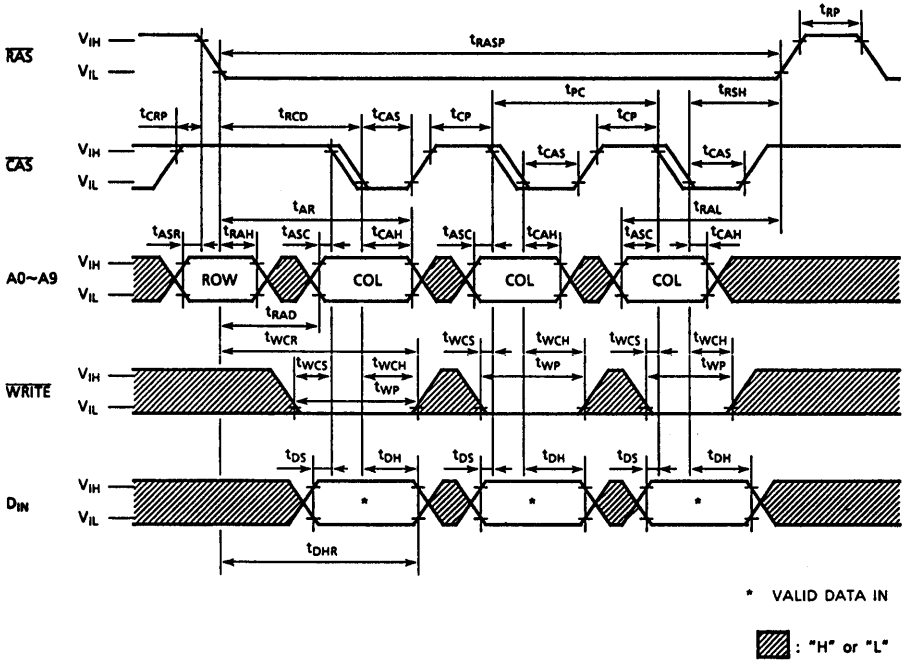
WRITE CYCLE (EARLY WRITE)



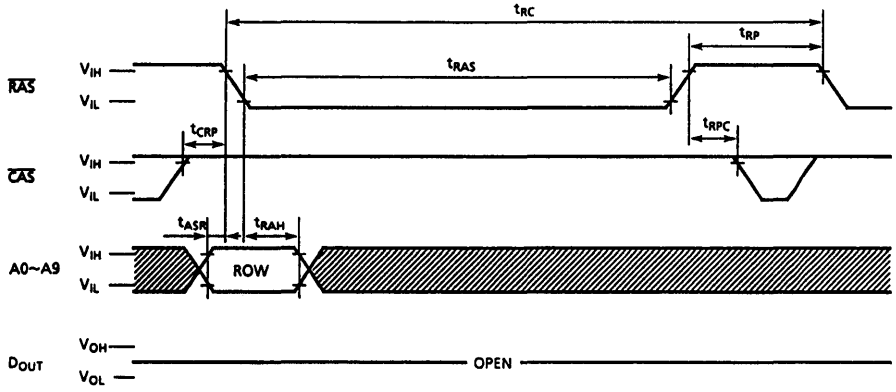
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



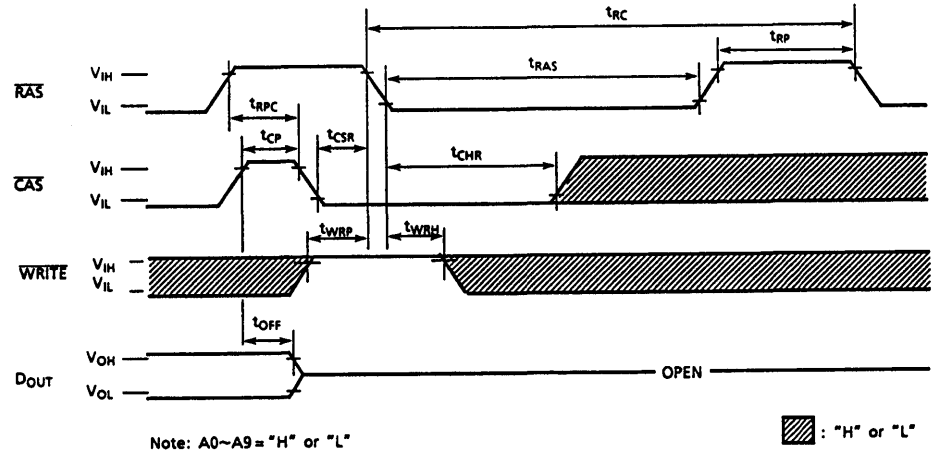
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$ = "H" or "L"

▨ : "H" or "L"

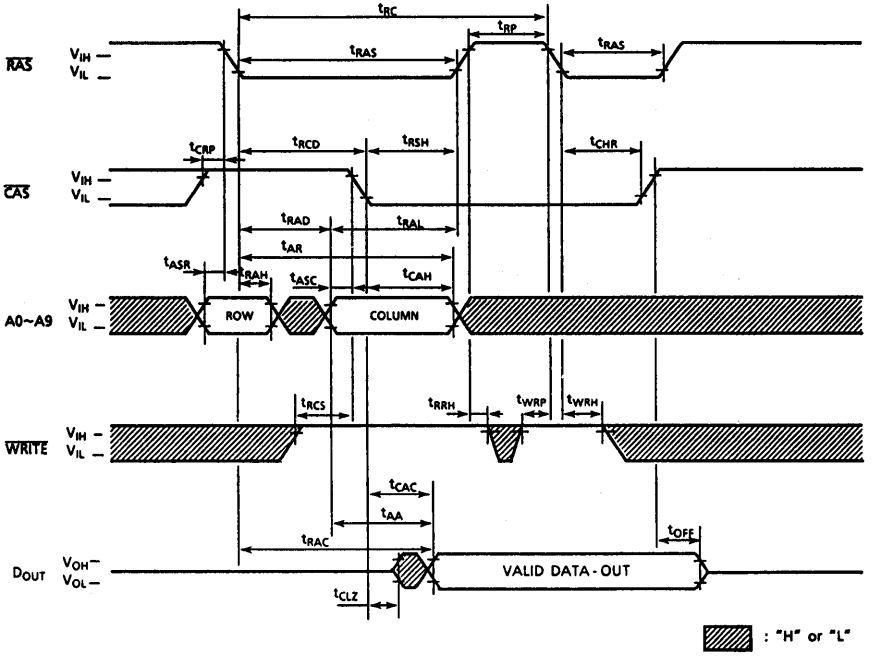
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



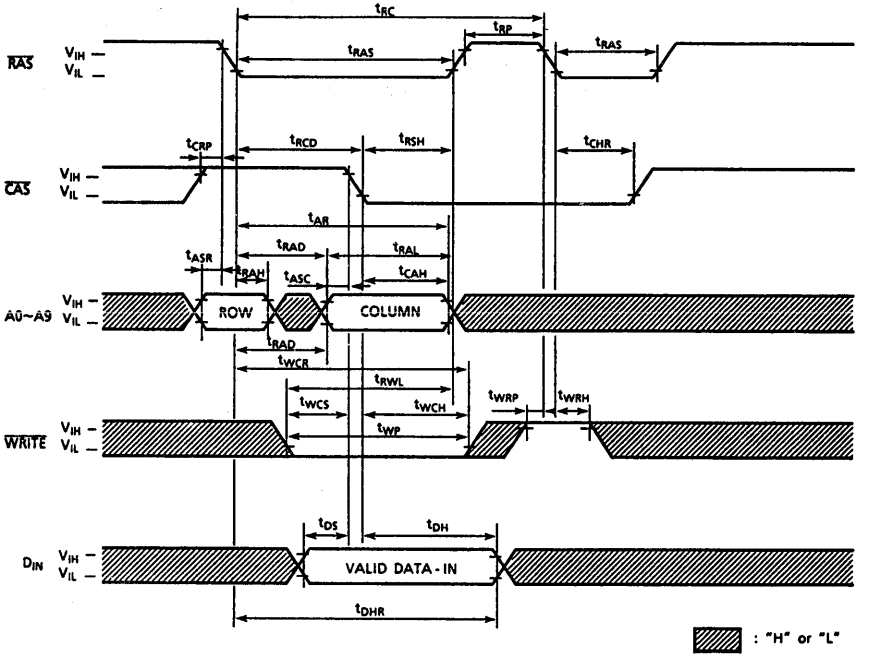
Note: A0~A9 = "H" or "L"

▨ : "H" or "L"

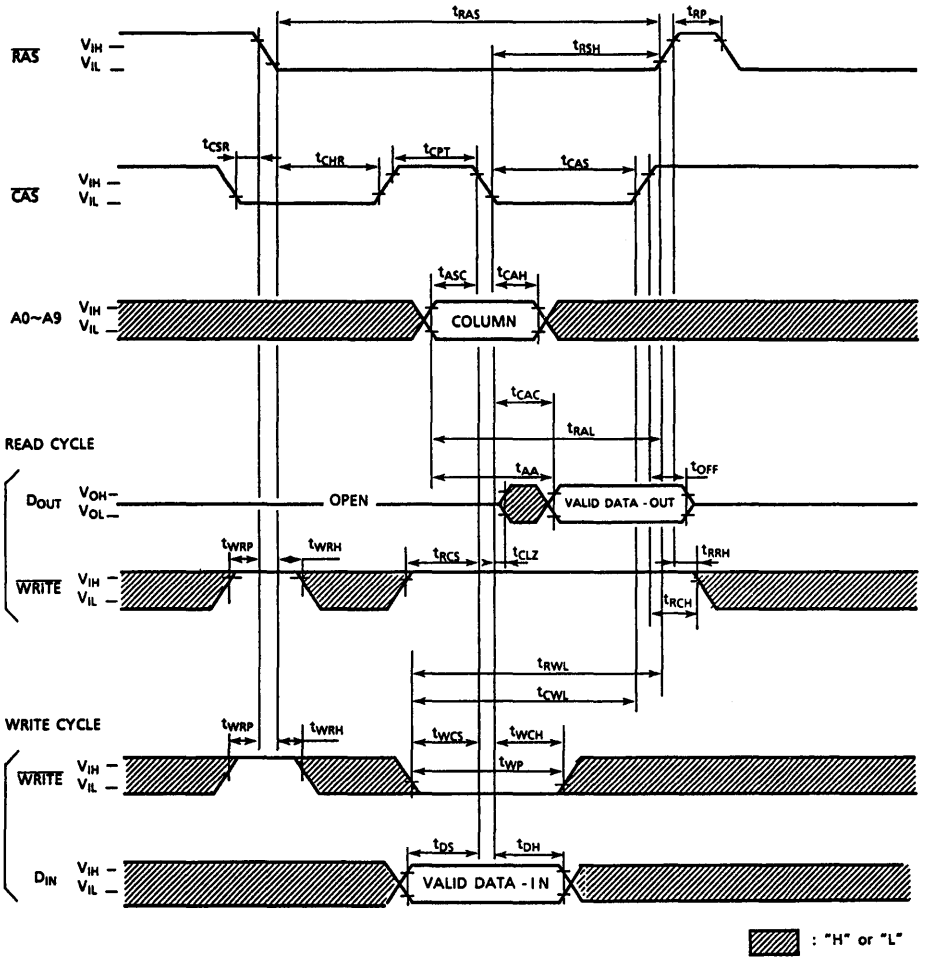
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	ns	
t_{RMW}	Read-Modify-Write Cycle	155	-	180	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	85	-	95	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{WP}	Write Command Pulse Width	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	10	-	15	-	ns	12
t_{REF}	Refresh Period	-	64	-	64	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	40	-	45	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	-	95	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	55	-	60	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	60	-	65	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	20	-	30	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ to Access Time	-	15	-	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	15	-	15	-	ns	
t_{OEZ}	Ouput buffer turn off Delay Time from $\overline{OE}$	0	15	0	15	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	15	-	15	-	ns	
t_{ODS}	Output Disable Set-Up Time	0	-	0	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE (V_{CC} = 5V ± 10%,Ta = 0~70°C)(Notes 6,7,8)

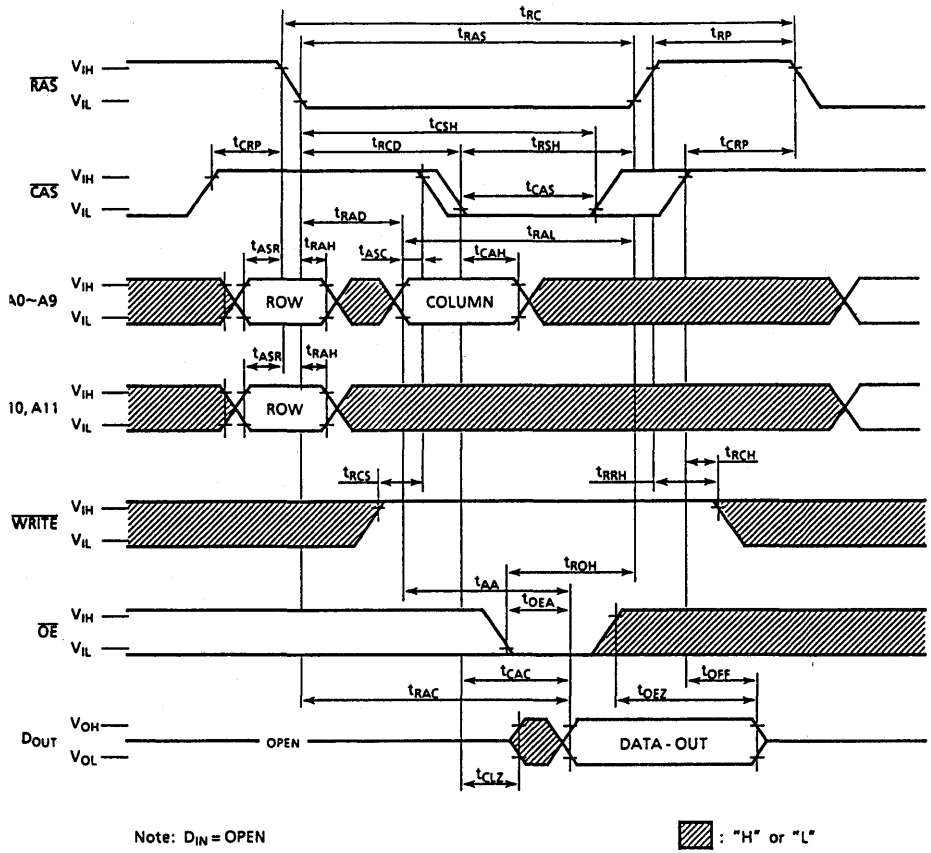
SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	40	-	45	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	ns	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume t_T=5ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and to E2 (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS} is not a restictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

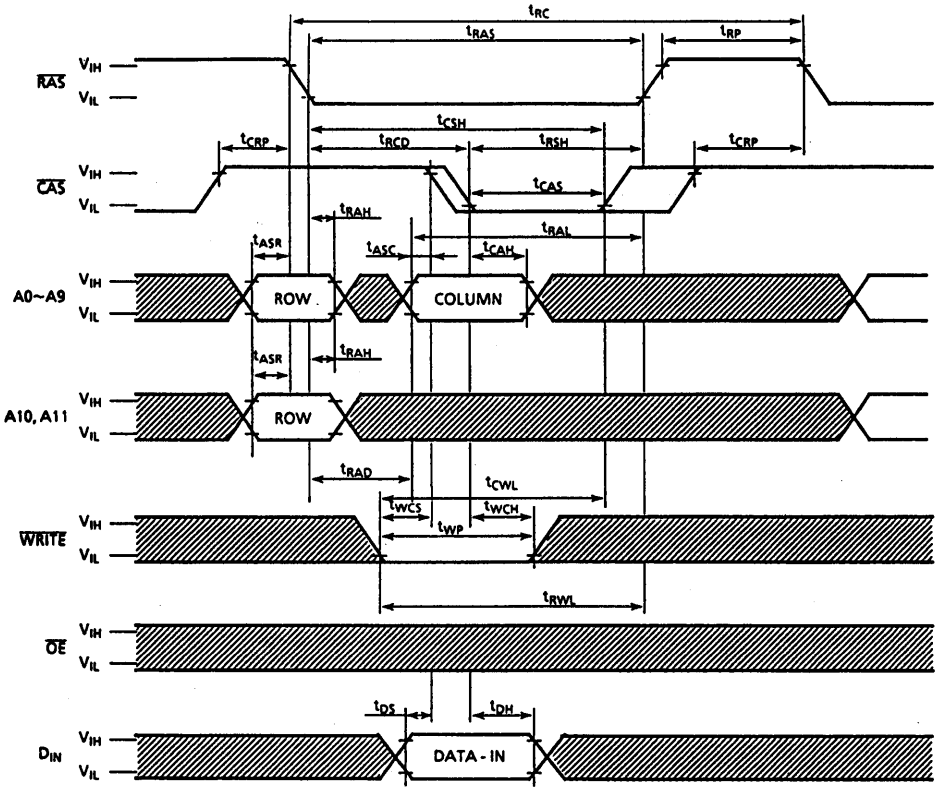
READ CYCLE



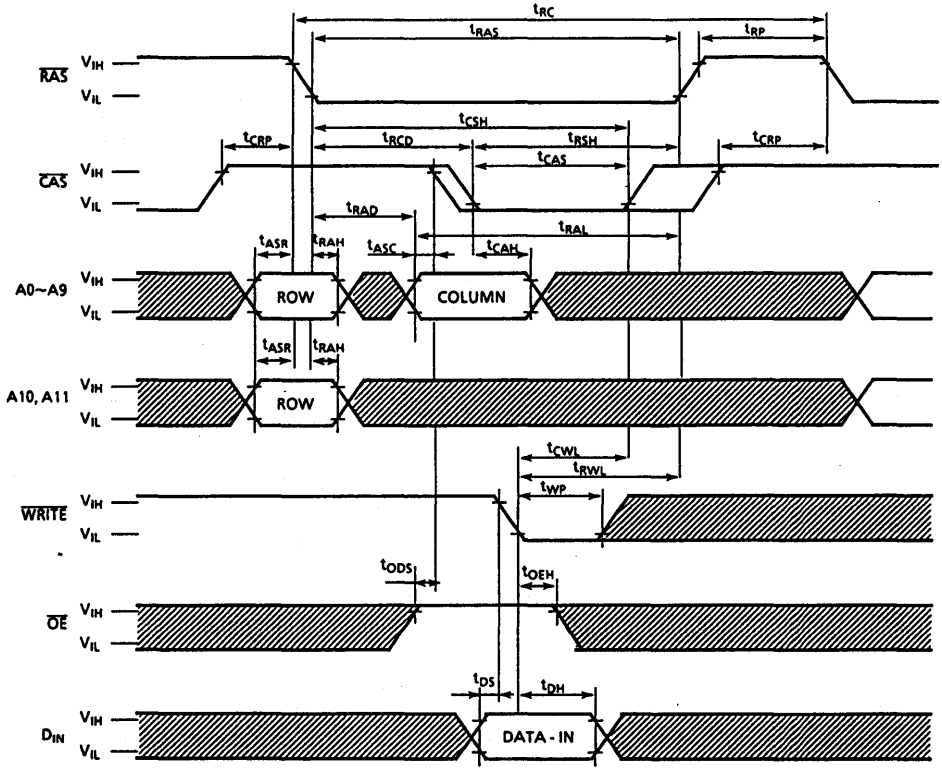
Note: D_{IN} = OPEN

▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE)



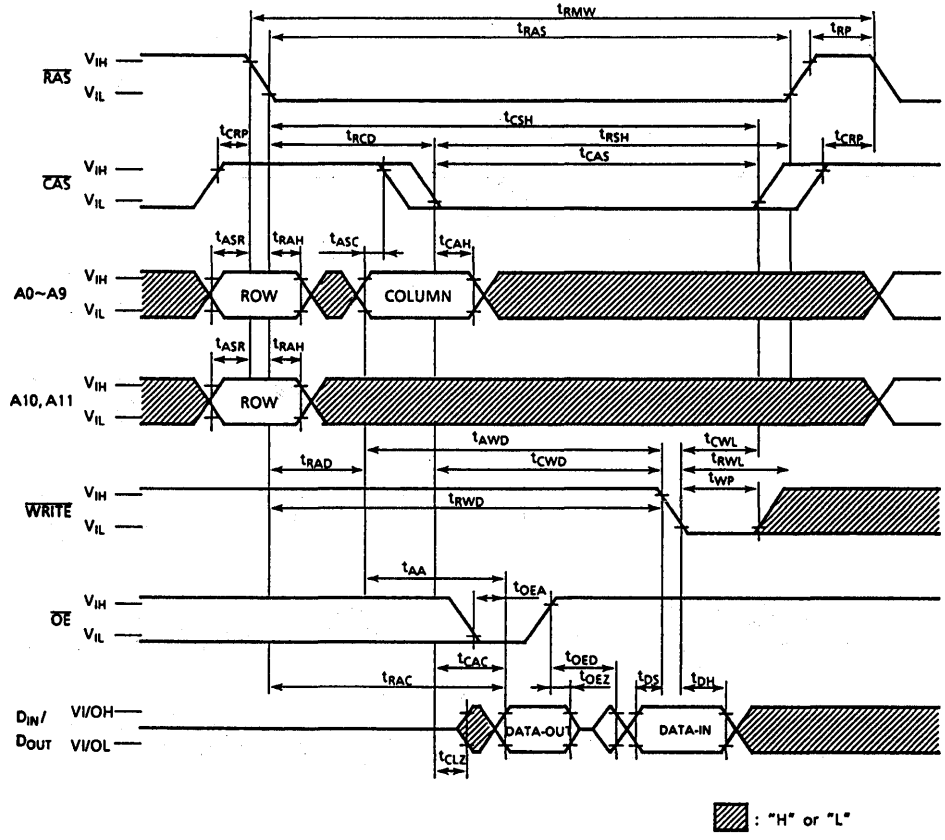
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



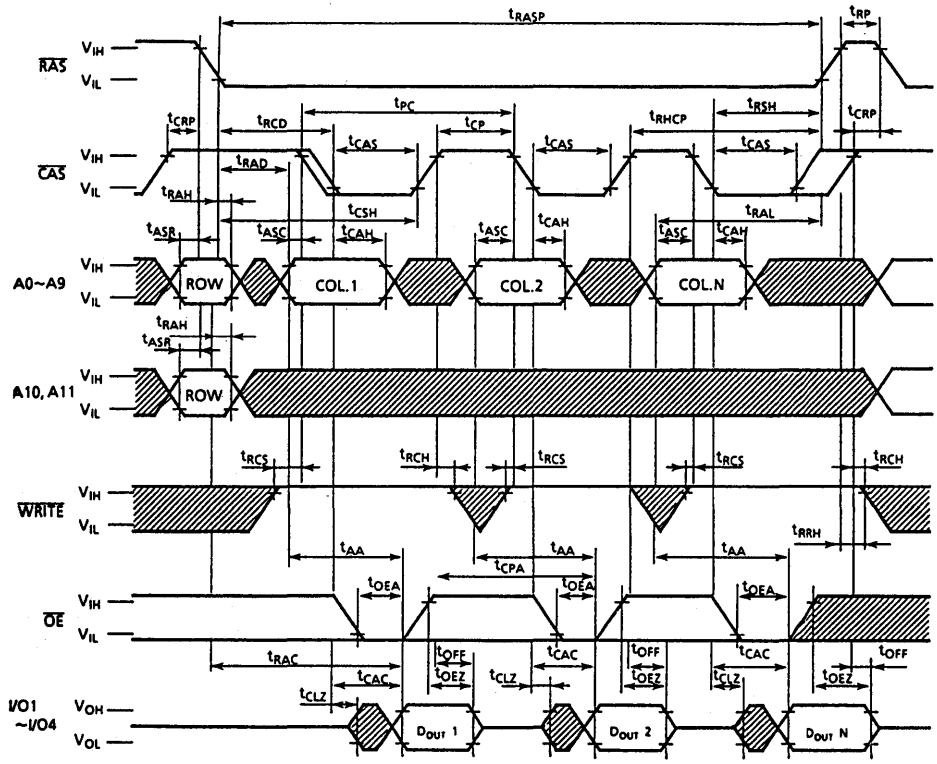
Note: D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE



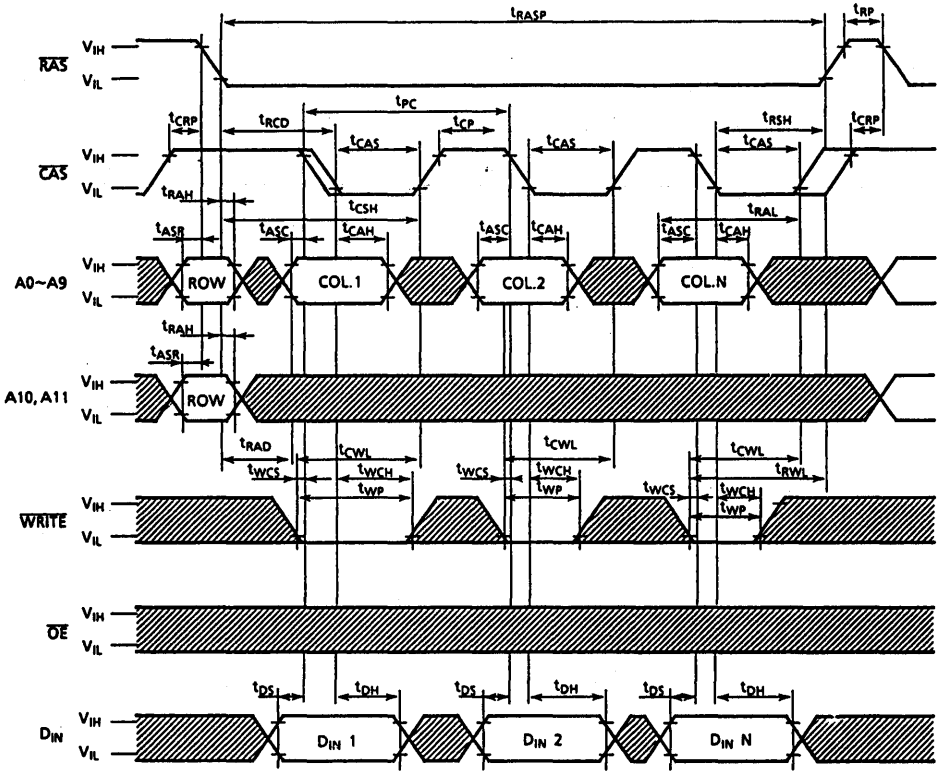
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

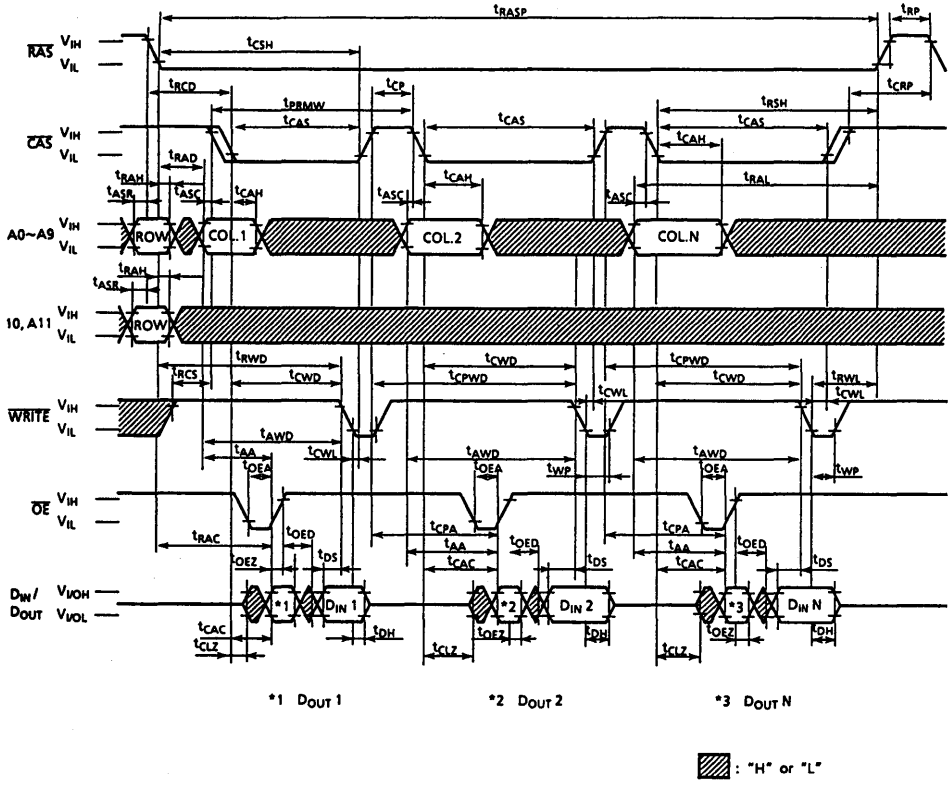
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



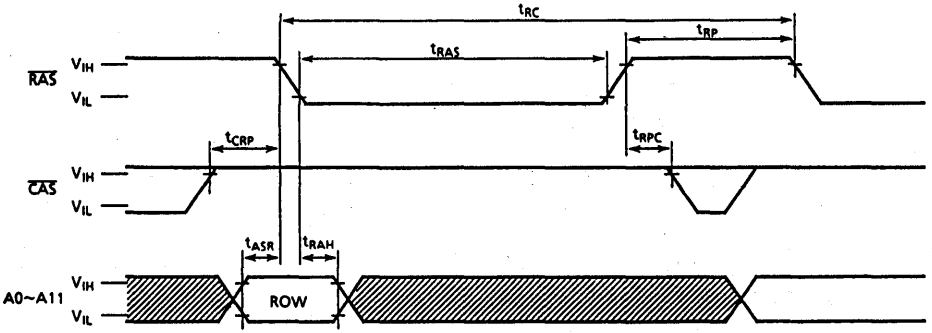
Note: D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



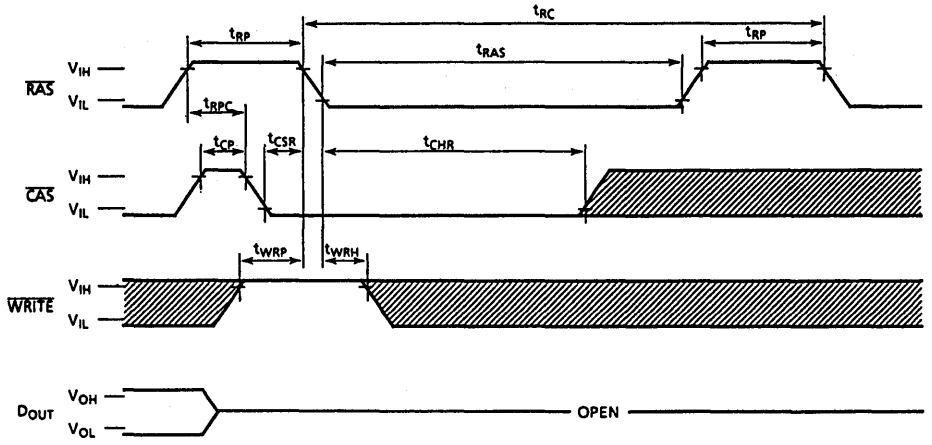
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

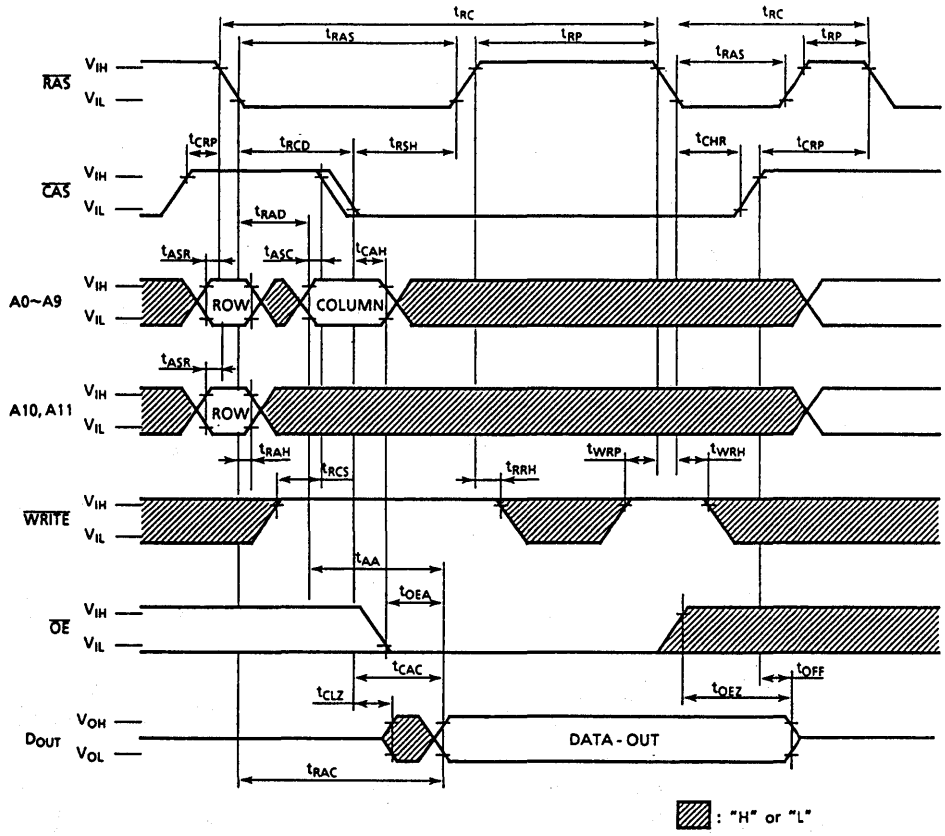
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A11 = "H" or "L"

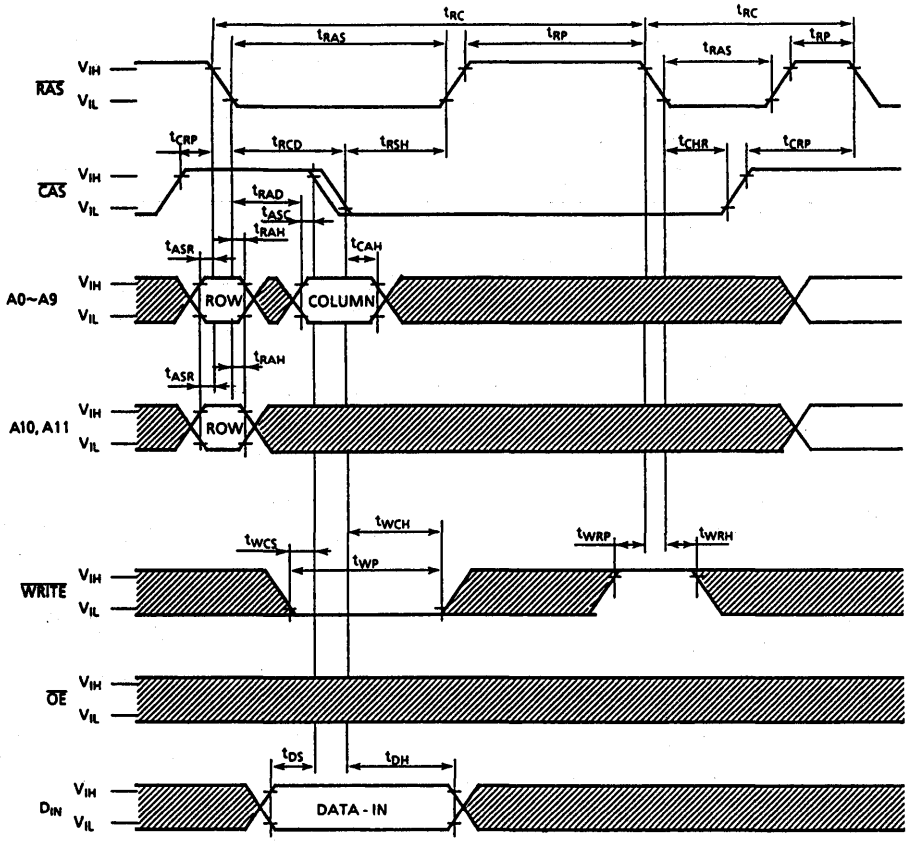
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

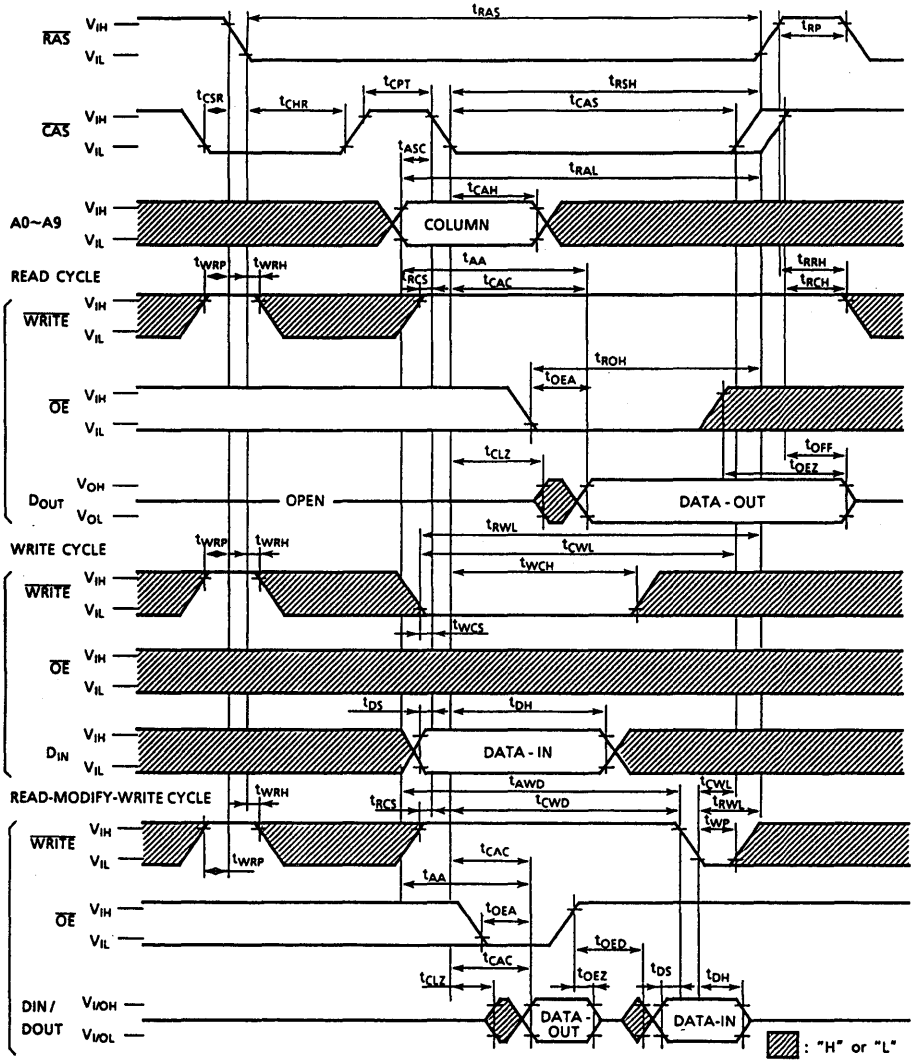
HIDDEN REFRESH CYCLE (WRITE)



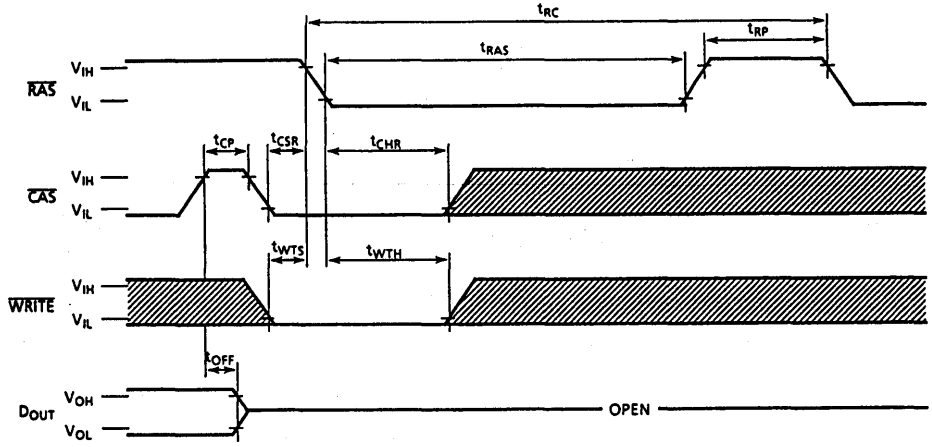
Note: D_{OUT} = OPEN

▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



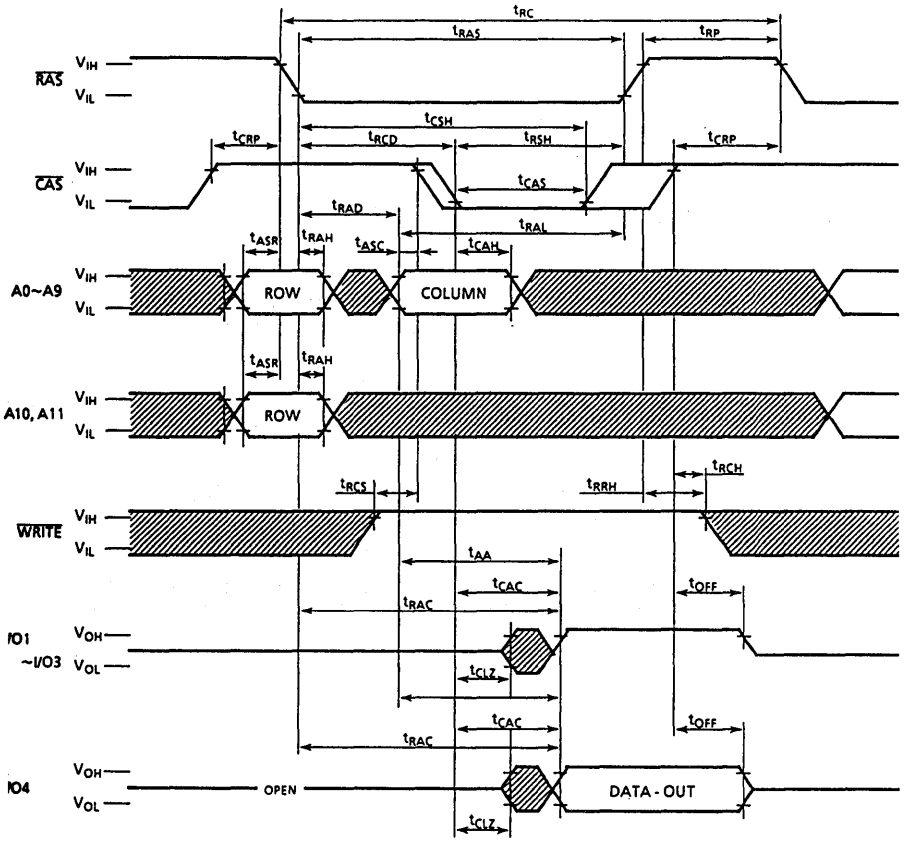
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A11 = "H" or "L"

▨ : "H" or "L"

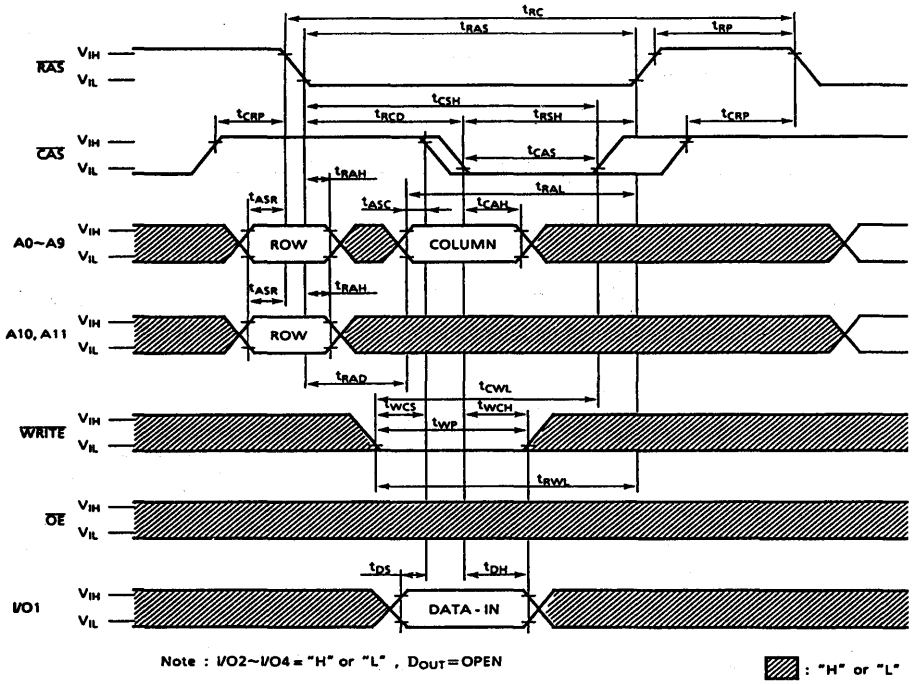
READ CYCLE IN THE TEST MODE



Note : $\overline{OE}$ = "L", D_{IN} = OPEN

▨ : "H" or "L"

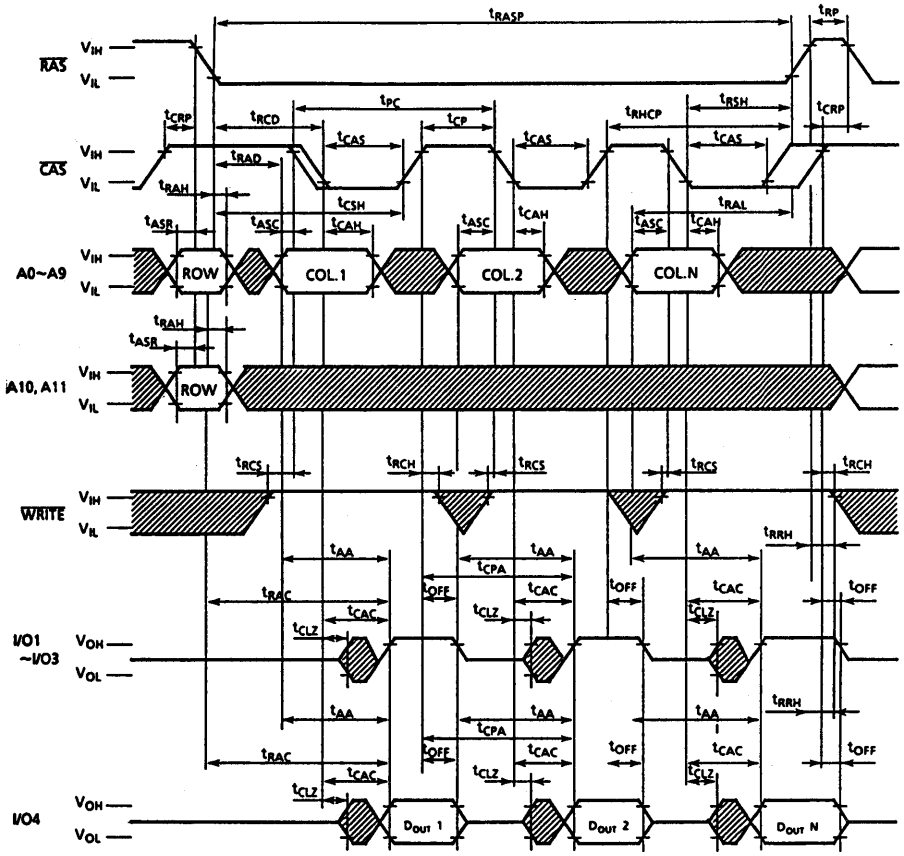
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L" , D_{OUT} = OPEN

▨ : "H" or "L"

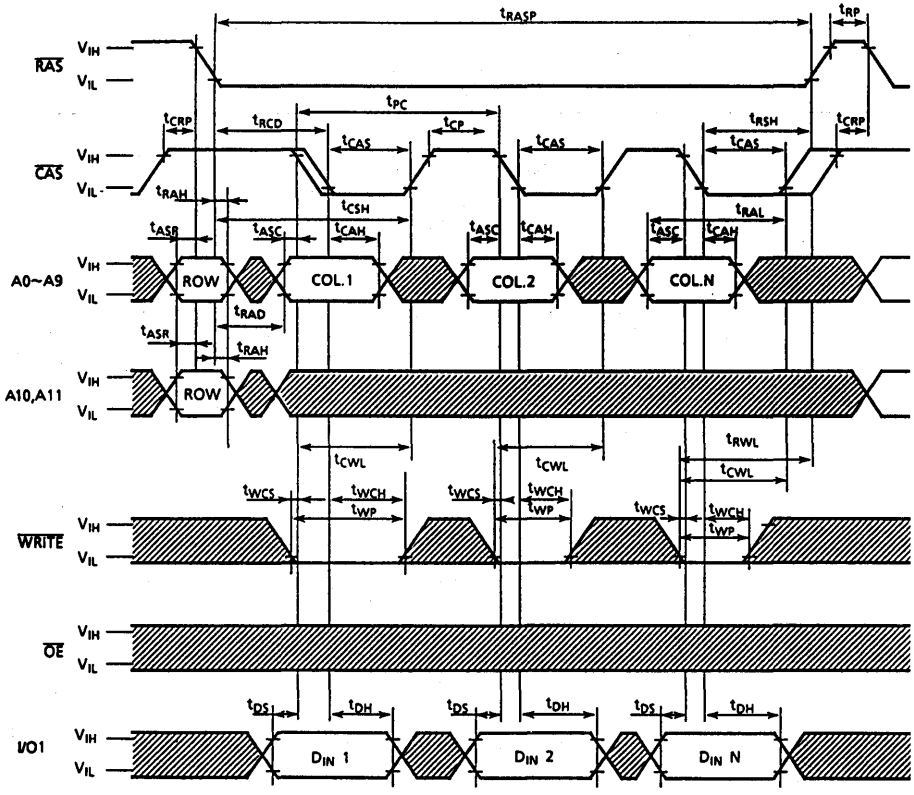
FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note : $\overline{OE}$ = "L" , D_{IN} = OPEN

▨ : "H" or "L"

FAST PAGE MODE WRITE CYCLE IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L" , D_{OUT} = OPEN

TEST MODE

The TC5116400J is the RAM organized 4,194,304 words by 4 bits, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel by using only I/O1. A_{1C}, A_{0C} are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s), the I/O4 pin indicates a"1".

If they were not equal, the I/O4 pin would indicate a "0". I/O1, I/O2 and I/O3 always indicate a "1" during test mode read cycle. Fig. 1 shows the block diagram of TC5116400J. In "Test Mode", the 4MX4 DRAM can be tested as if it were a 1M X 16 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/4 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

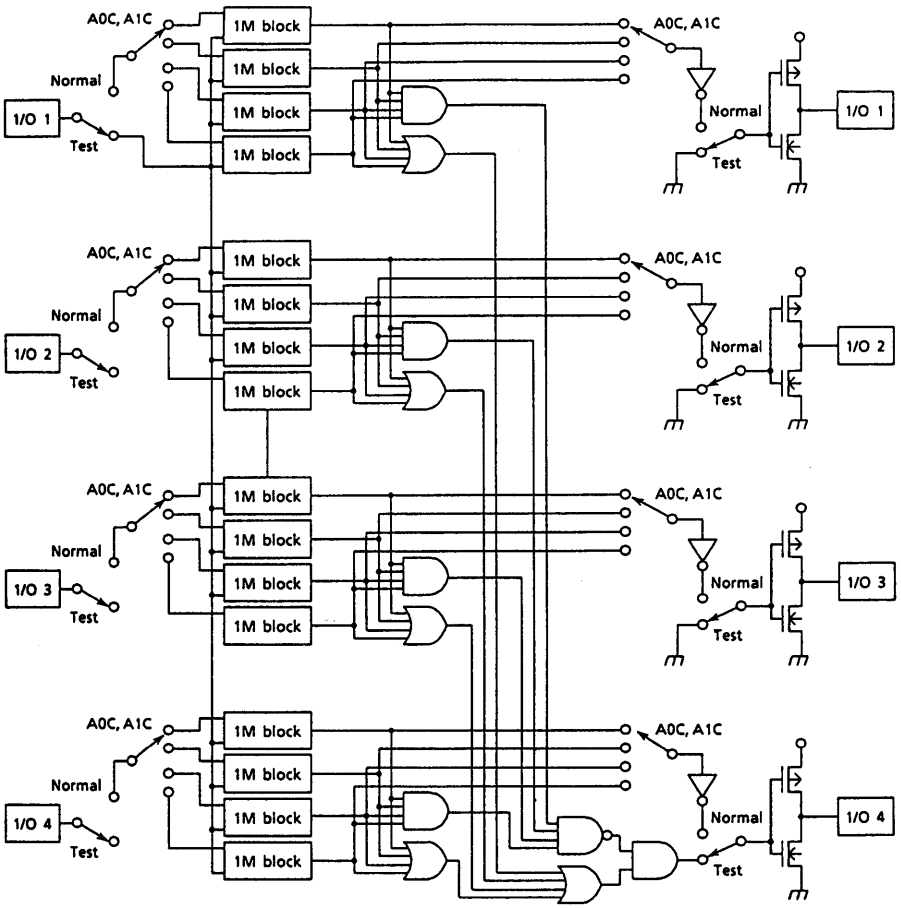


FIGURE 1

DRAM Module A.C. Conditions No.15
4Mx4/4Mx1-Based Modules

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	9,14 15
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11

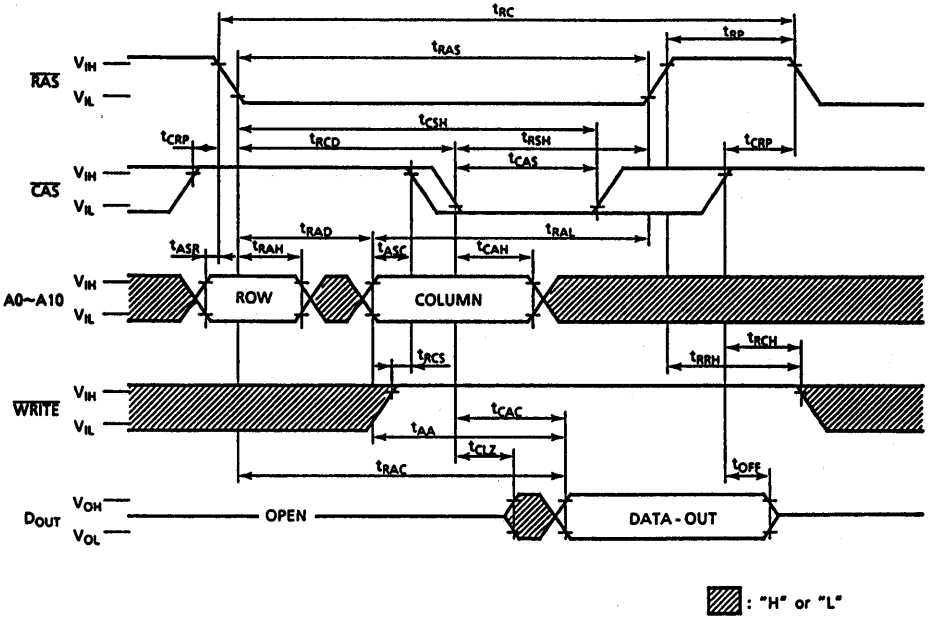
ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	12
t_{DH}	Data Hold Time	10	-	15	-	ns	12
t_{REF}	Refresh Period	-	32	-	32	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	20	-	30	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	ns	

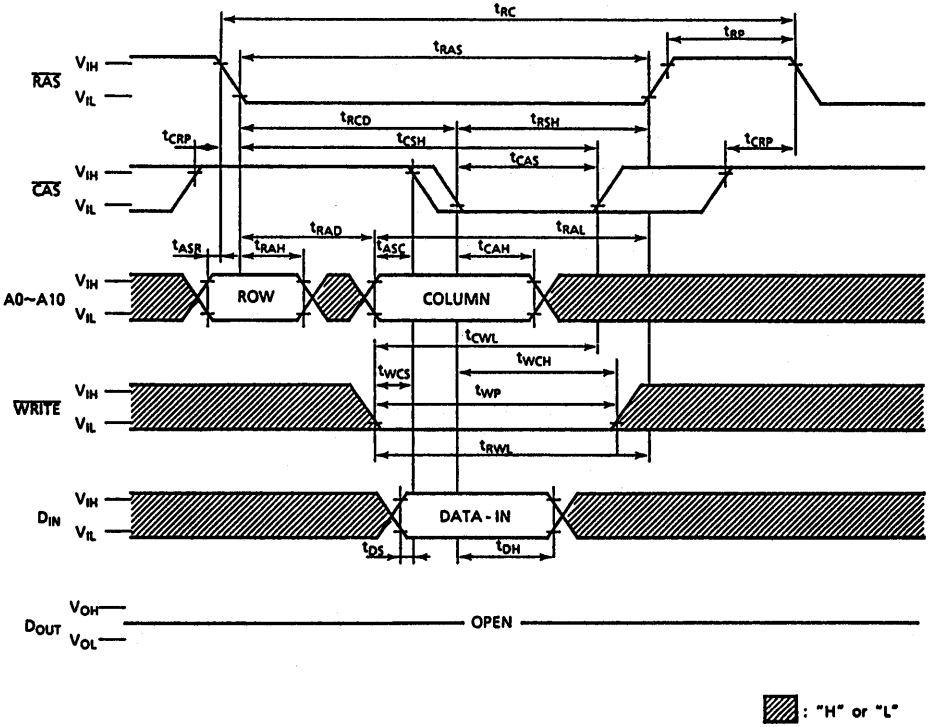
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume t_T=5ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS} is not a restictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

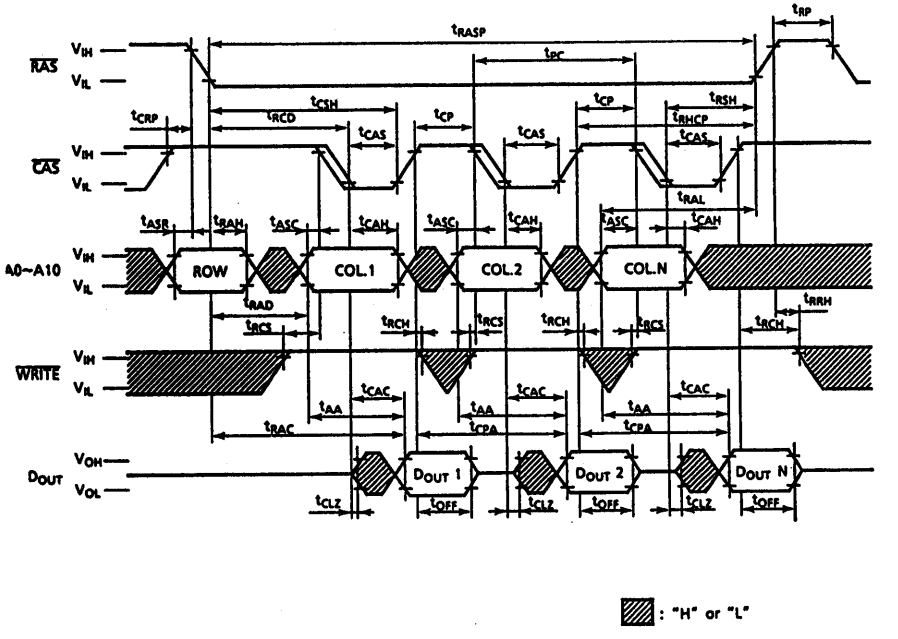
READ CYCLE



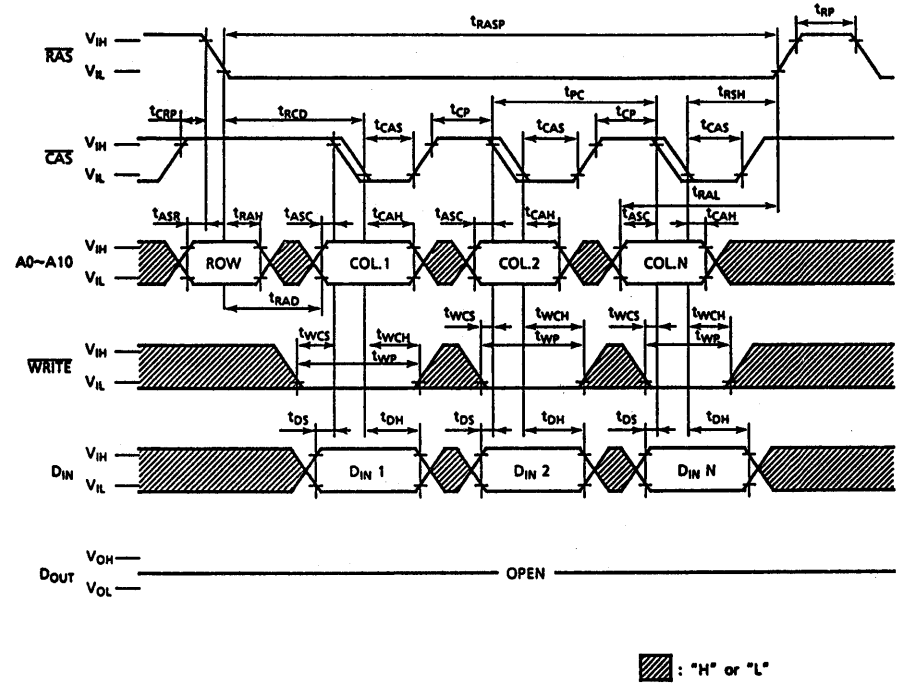
WRITE CYCLE (EARLY WRITE)



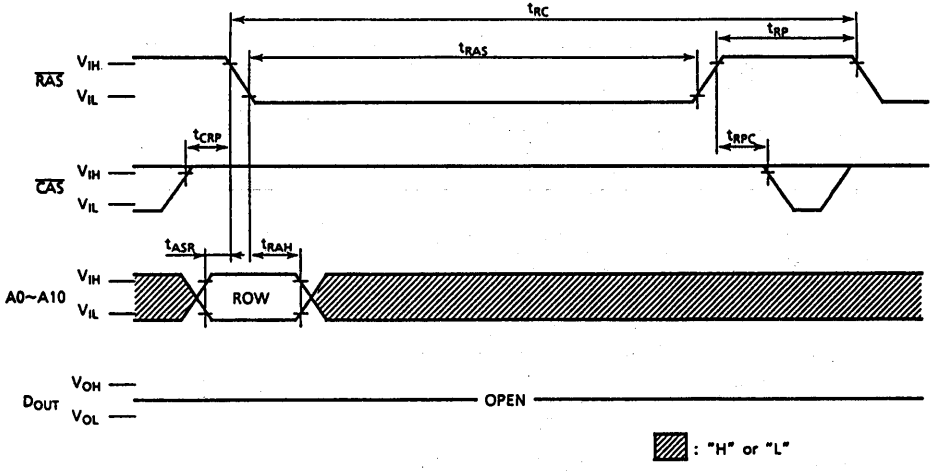
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

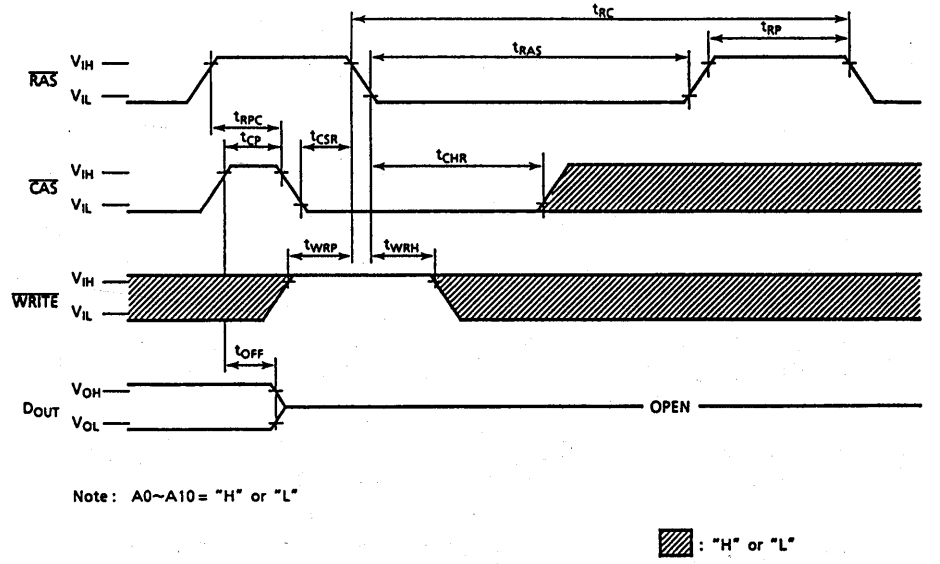


$\overline{RAS}$ ONLY REFRESH CYCLE



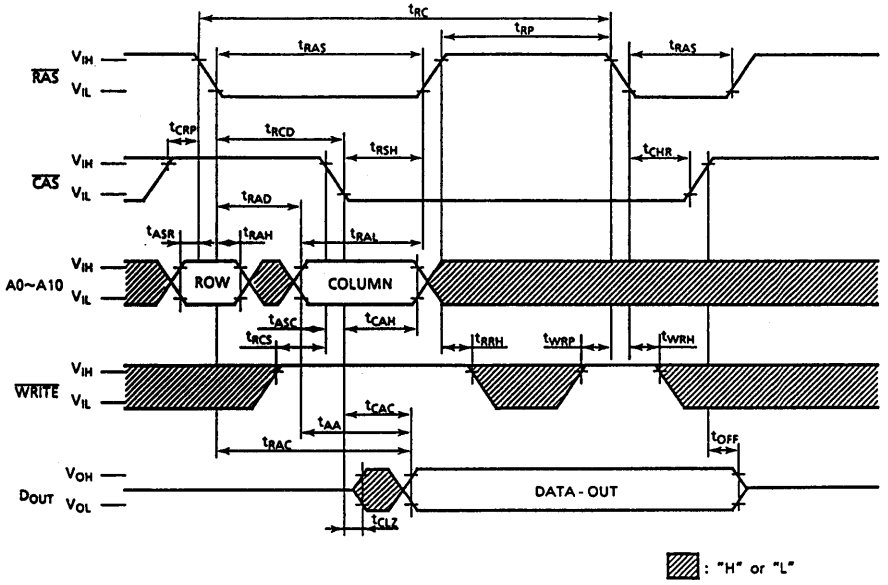
Note: $\overline{WRITE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

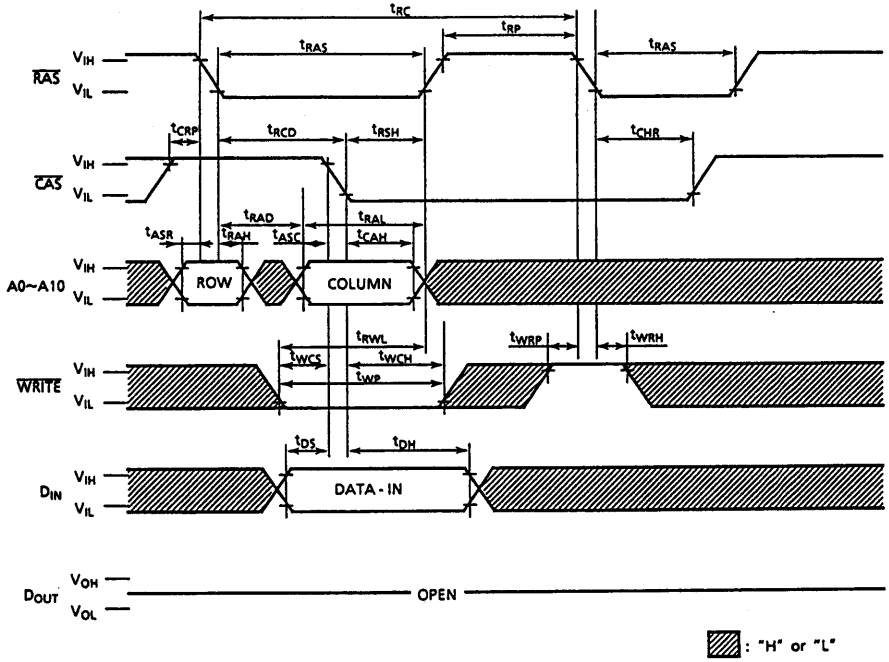


Note: A0~A10 = "H" or "L"

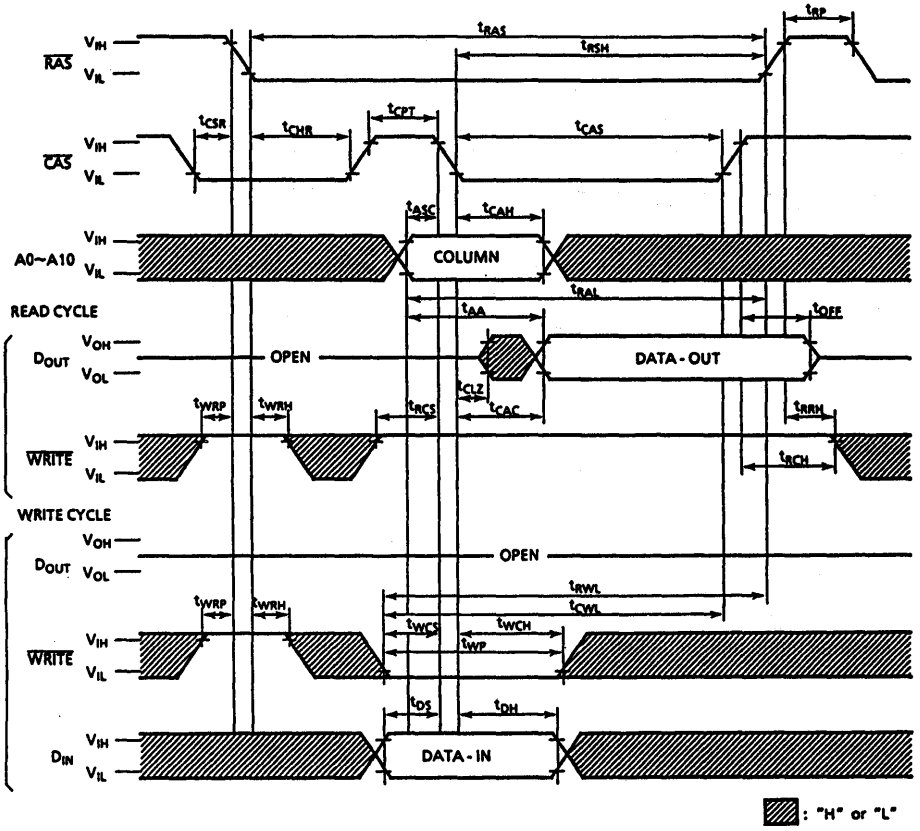
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	9,13, 14
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	ns	9,13
t_{AA}	Access Time from Column Address	-	30	-	35	ns	9,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	
t_{DH}	Data Hold Time	10	-	15	-	ns	
t_{REF}	Refresh Period	-	32	-	32	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	20	-	30	-	ns	
t_{WTS}	Write Command Set-Up Time (Test Mode In)	10	-	10	-	ns	
t_{WTH}	Write Command Hold Time (Test Mode In)	10	-	10	-	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle	10	-	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	115	-	135	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	65	-	75	ns	9,13, 14
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	25	ns	9,13
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	65	10,000	75	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200,000	75	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	65	-	75	-	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	40	-	45	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	ns	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

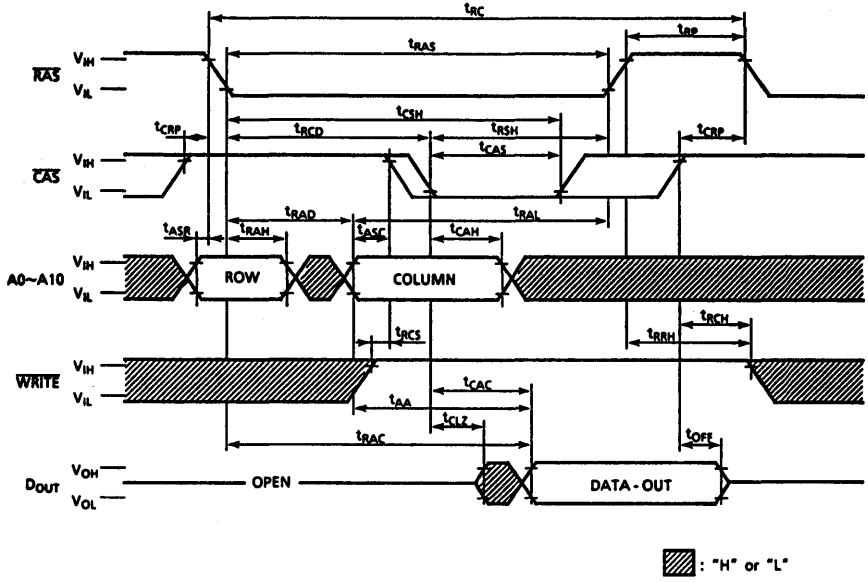
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

12. t_{WCS} is not a restictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle.

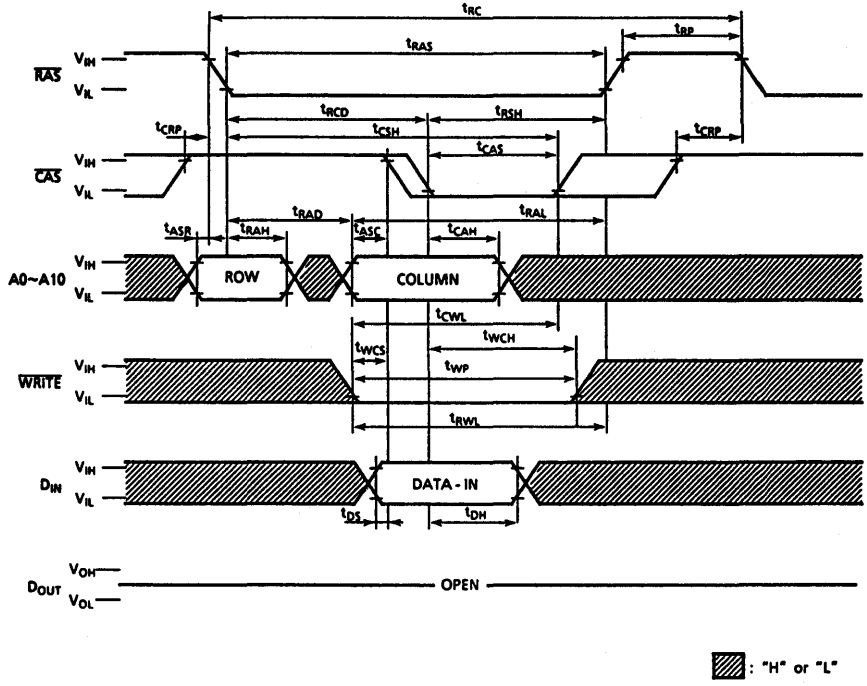
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

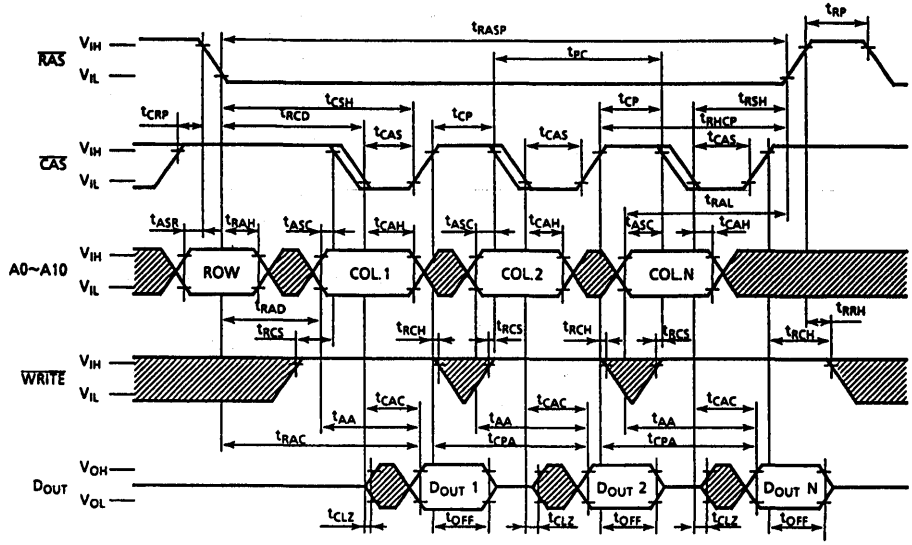
READ CYCLE



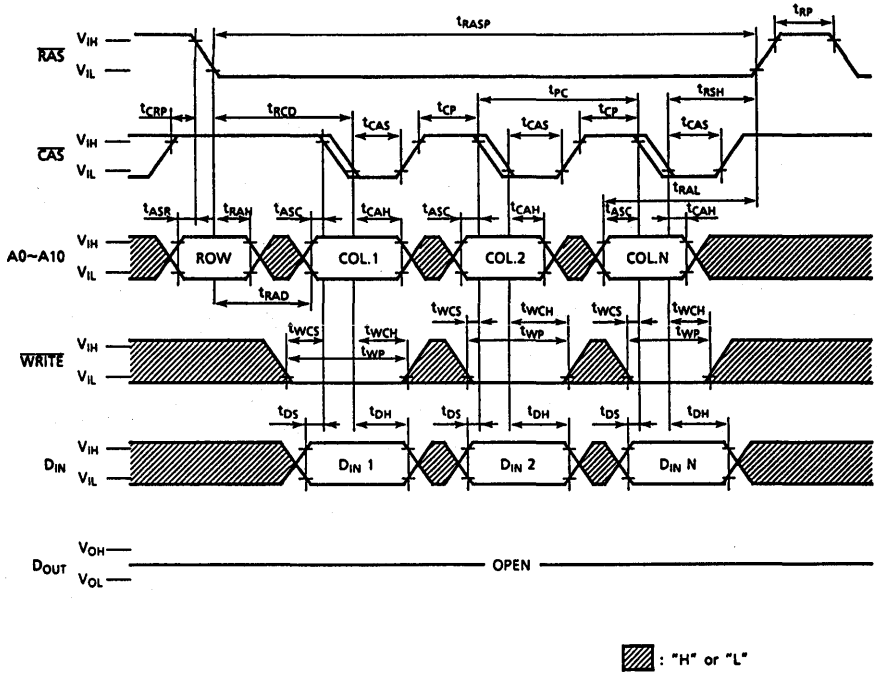
WRITE CYCLE (EARLY WRITE)



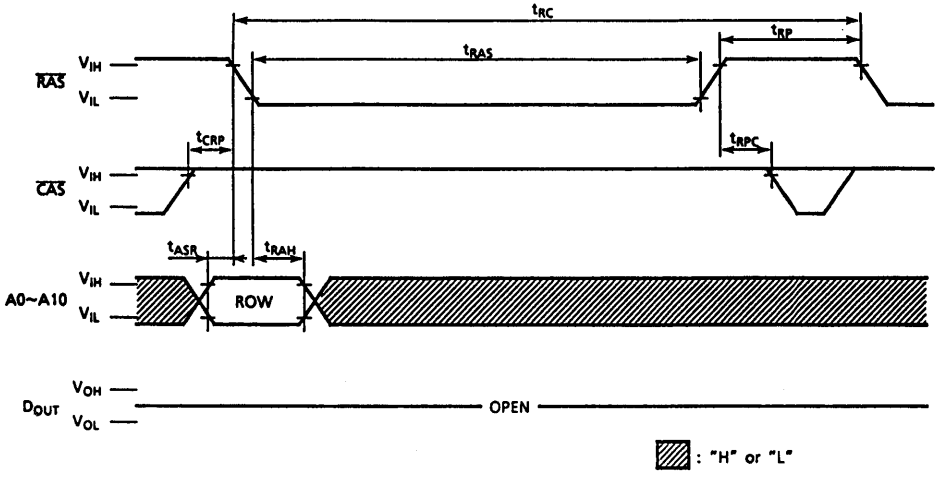
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

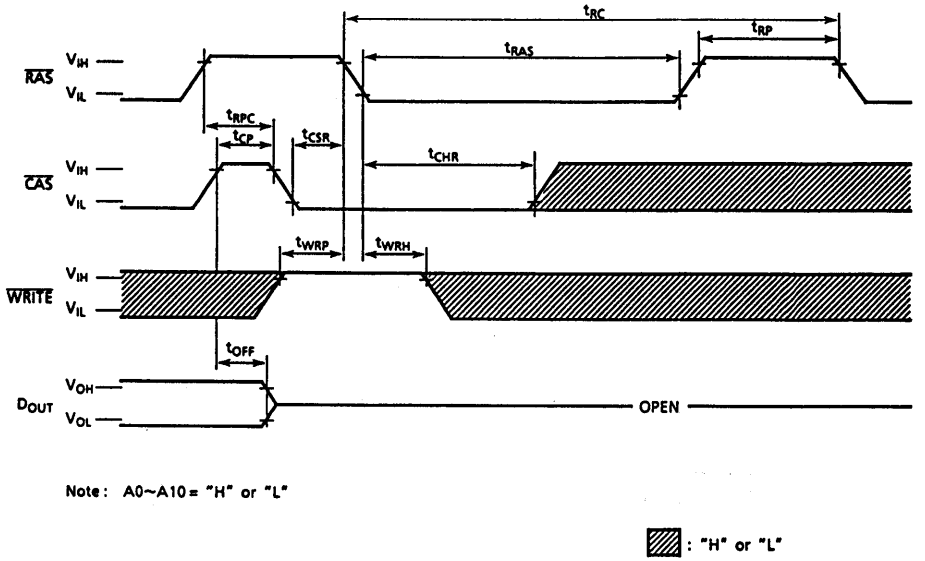


$\overline{RAS}$ ONLY REFRESH CYCLE



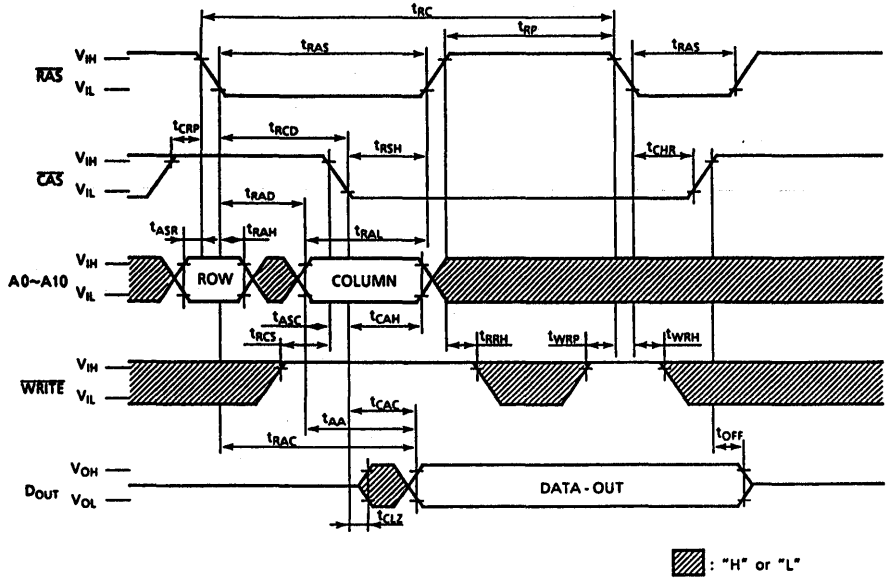
Note : $\overline{WRITE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

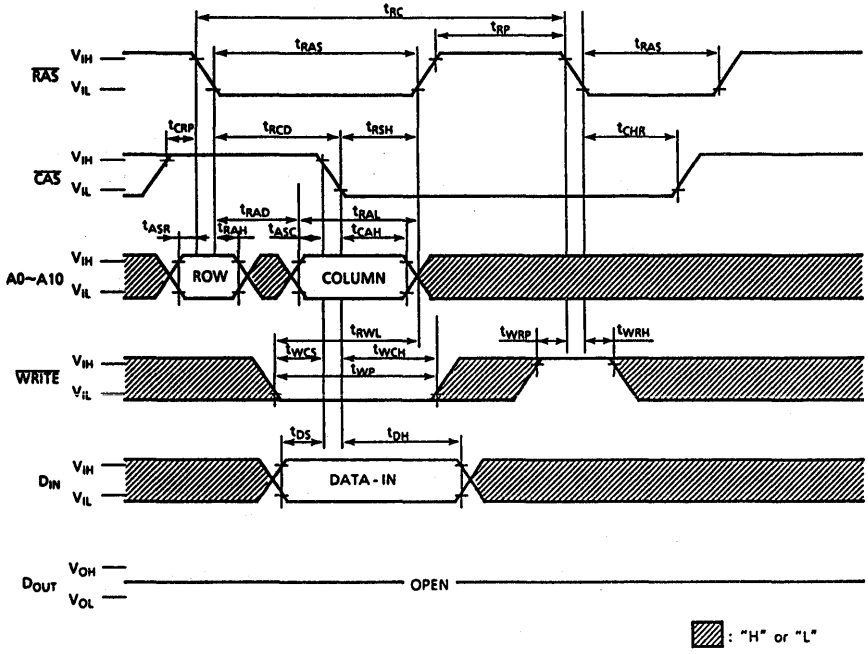


Note : A0~A10 = "H" or "L"

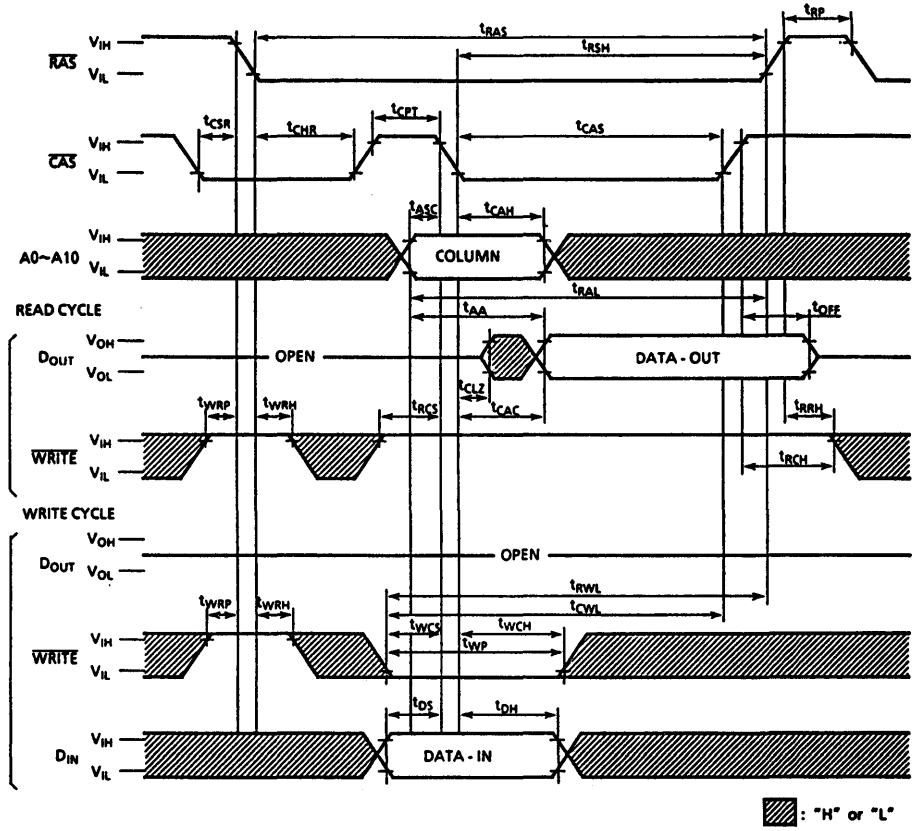
HIDDEN REFRESH CYCLE (READ)



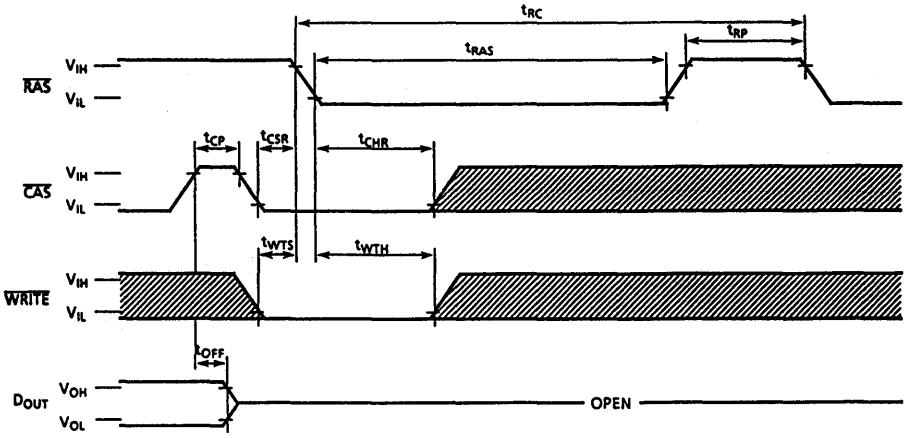
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



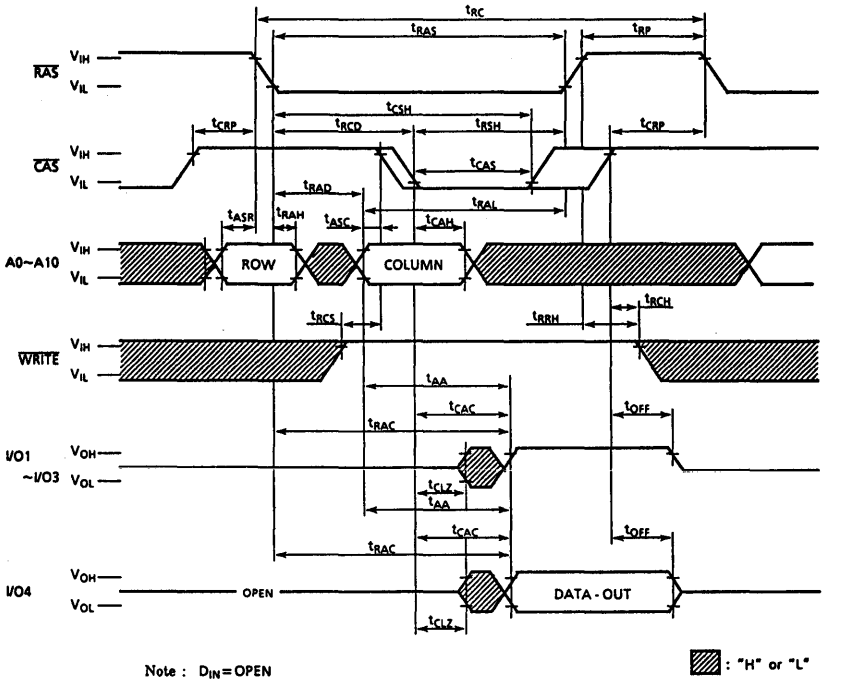
WRITE, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, A0~A10 = "H" or "L"

▨ : "H" or "L"

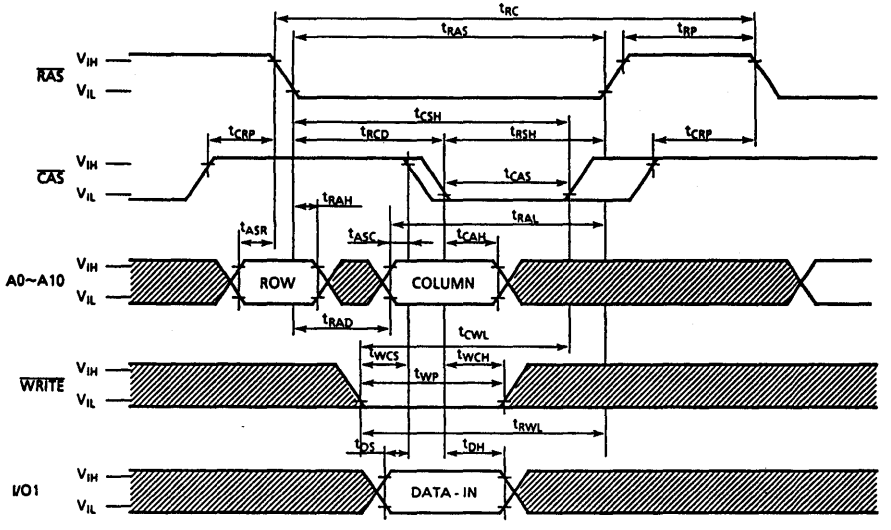
READ CYCLE IN THE TEST MODE



Note : D_{IN} = OPEN

▨ : "H" or "L"

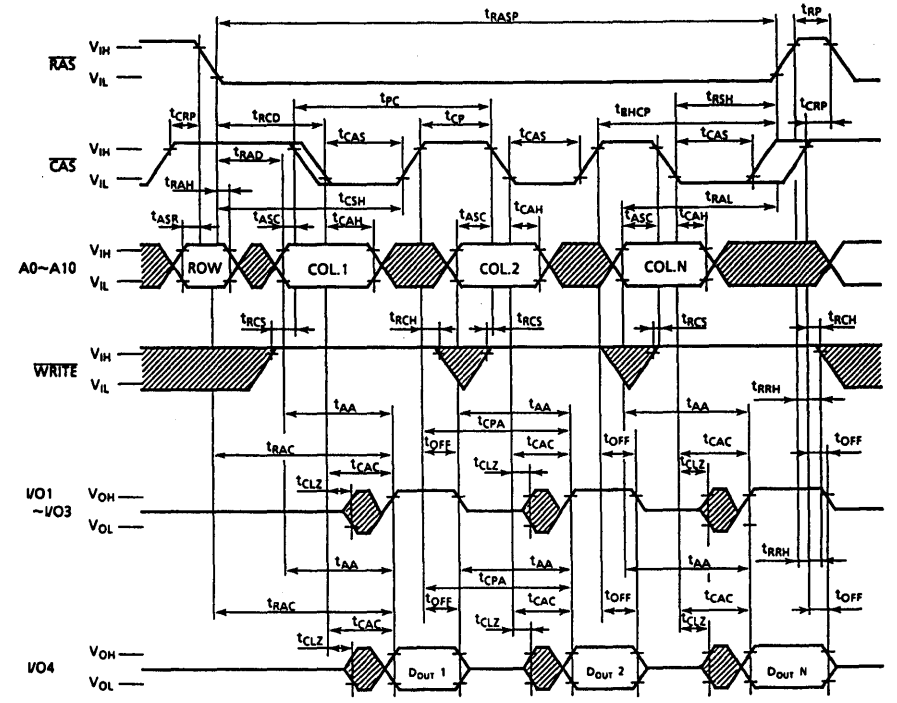
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L", D_{OUT} = OPEN

: "H" or "L"

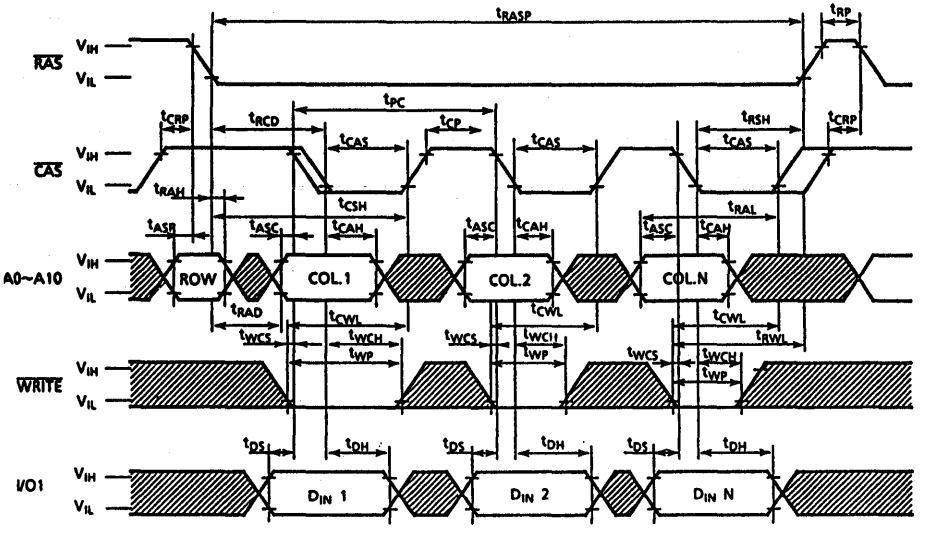
FAST PAGE MODE READ CYCLE IN THE TEST MODE



Note : D_{IN} = OPEN

: "H" or "L"

FAST PAGE MODE WRITE CYCLE IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L", D_{OUT} = OPEN

▨ : "H" or "L"

TEST MODE

The TC51174100J/FT/TR is the RAM organized 4,194,304 words by 4 bits, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel by using only I/O1. A_{1C}, A_{0C} are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s), the I/O4 pin indicates a "1". If they were not equal, the I/O4 pin would indicate a "0". I/O1, I/O2 and I/O3 always indicate a "1" during test mode read cycle. Fig. 1 shows the block diagram of TC5117400J/FT/TR. In "Test Mode", the 4MX4 DRAM can be tested as if it were a 1MX16 DRAM.

"$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" puts the device into "Test Mode". And "$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" or $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{\text{WRITE}}$, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal refresh address counter. The "Test Mode" function reduces test times (1/4 in case of N test pattern).

BLOCK DIAGRAM IN THE TEST MODE

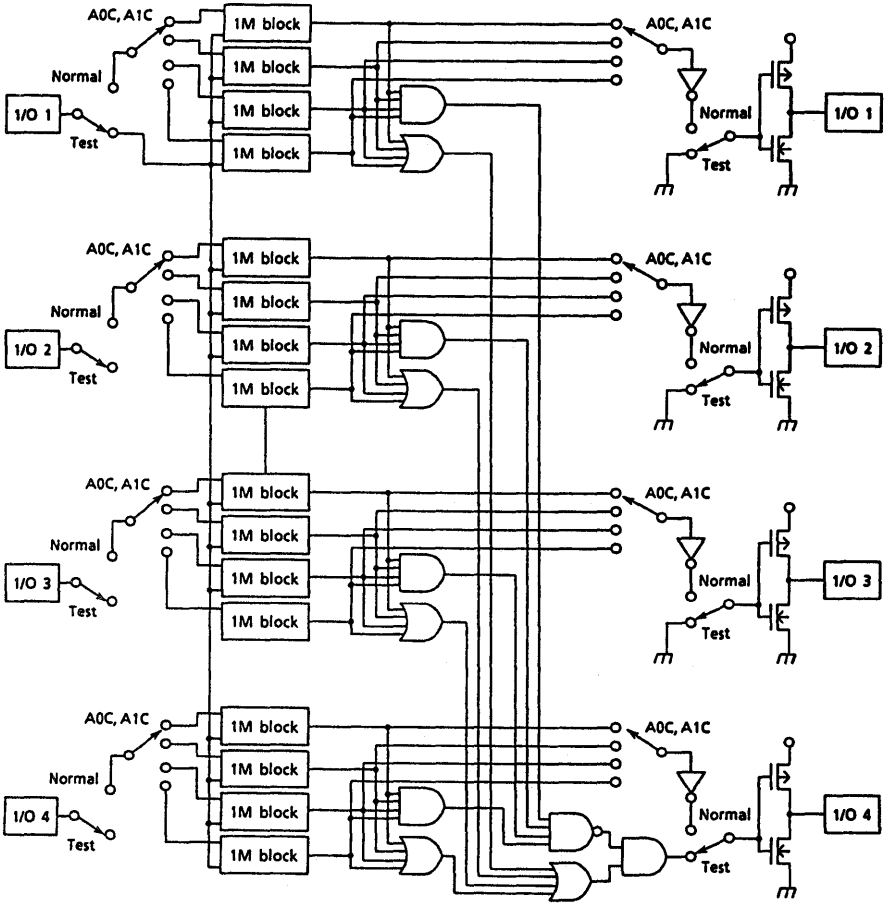


Figure 1

DRAM Module A.C. Conditions No.20
1Mx16 and 1Mx18-Based Modules

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	ns	9,13 14
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	ns	9,13
t_{AA}	Access Time from Column Address	-	35	-	40	ns	9,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	35	-	40	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RHH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	THMxxxxxx-70		THMxxxxxx-80		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	15	-	15	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	
t_{DH}	Data Hold Time	15	-	15	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	30	-	30	-	ns	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.

7. AC measurements assume t_T=5ns.

8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

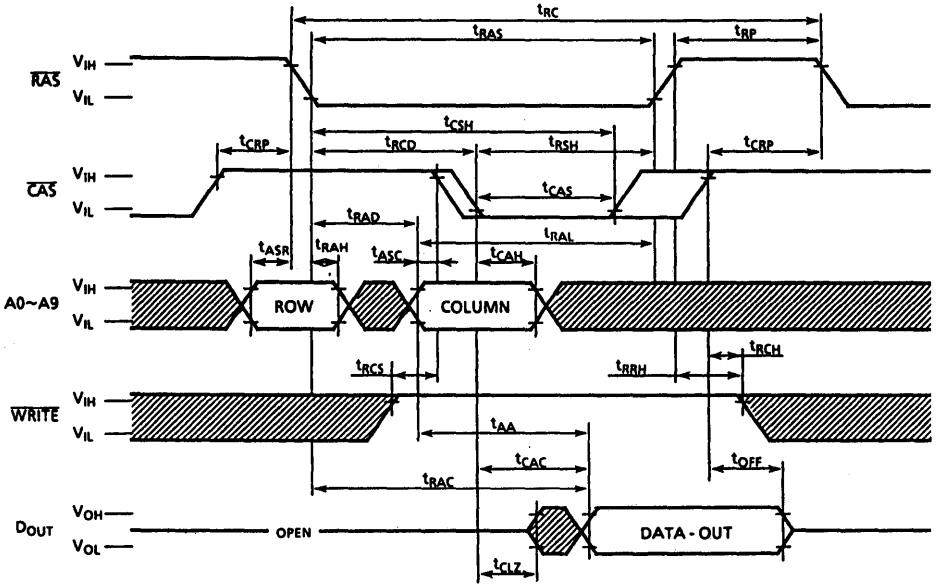
12. t_{WCS} is not a restictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle.

13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

DRAM Module A.C. Conditions No.20
1Mx16 and 1Mx18-Based Modules

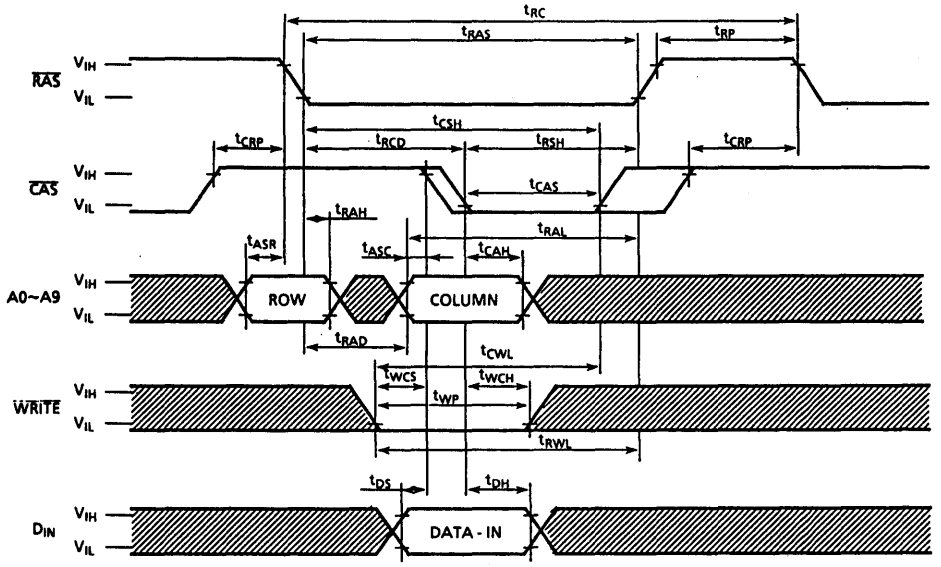
READ CYCLE



Note: D_{IN} = OPEN

: "H" or "L"

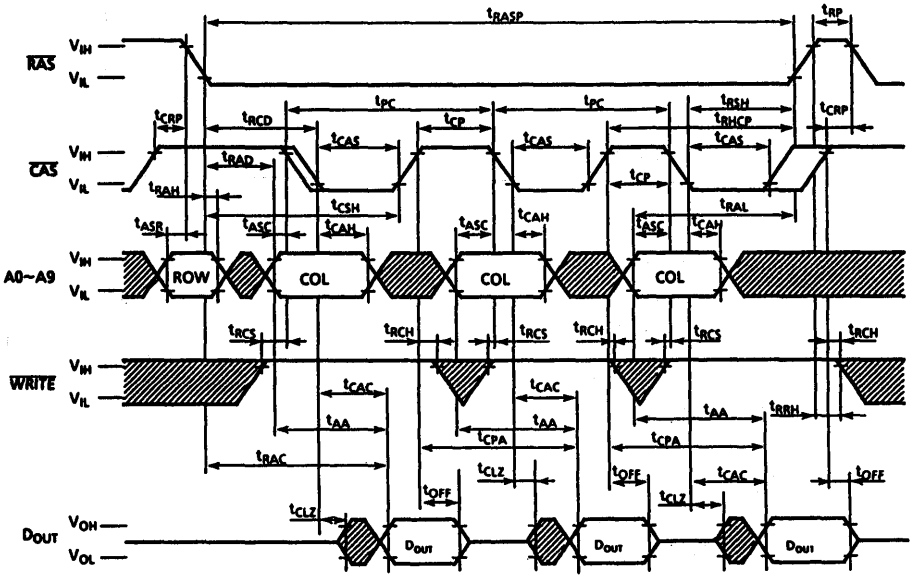
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

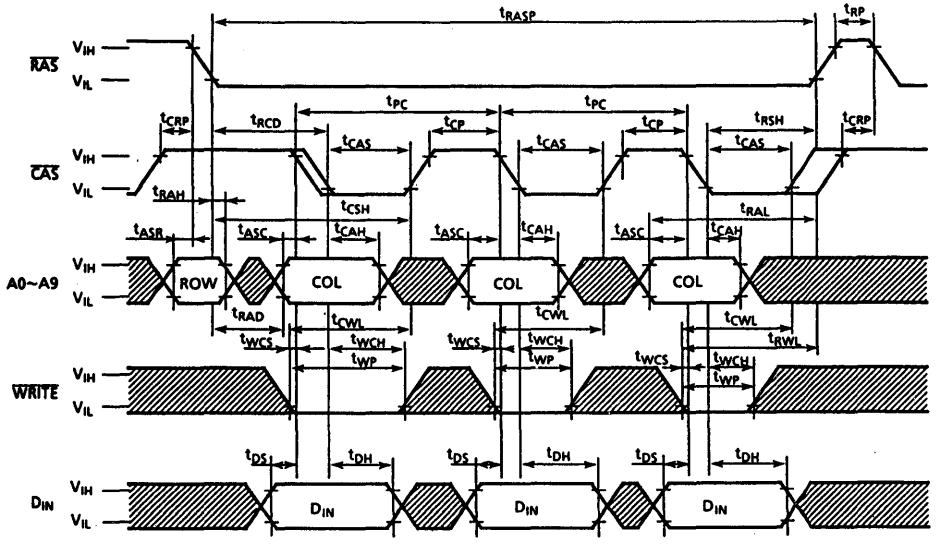
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨: "H" or "L"

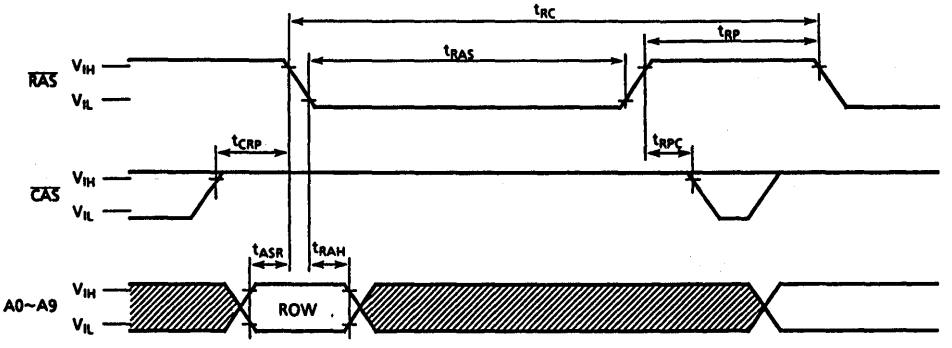
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

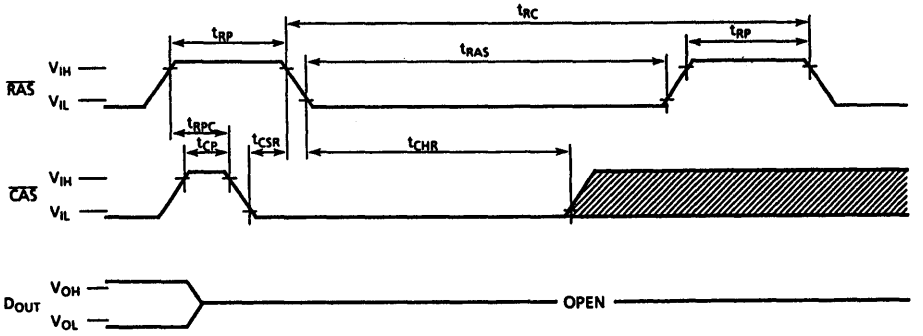
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$ = "H" or "L"
D_{IN} = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

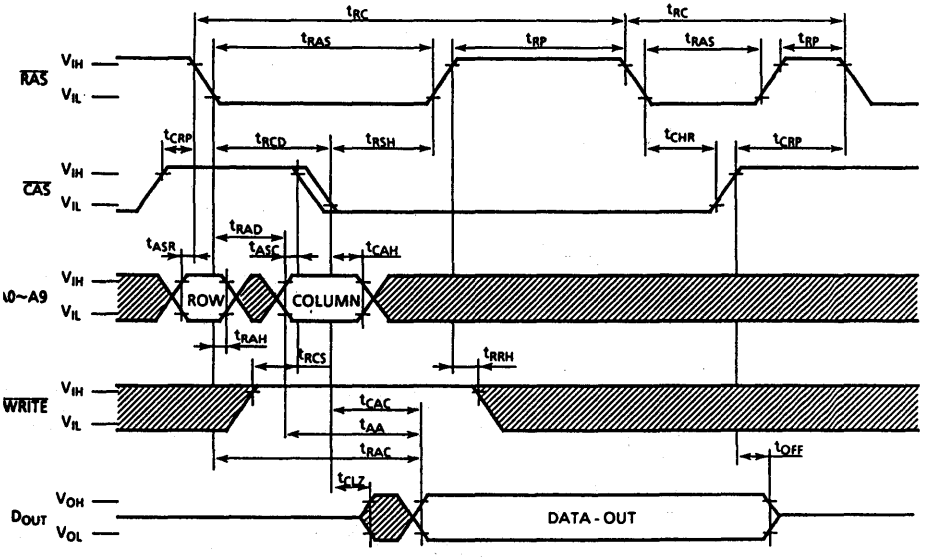
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



▨ : "H" or "L"

Note: $\overline{WRITE}$, A0~A9 = "H" or "L"
D_{IN} = Don't Care.

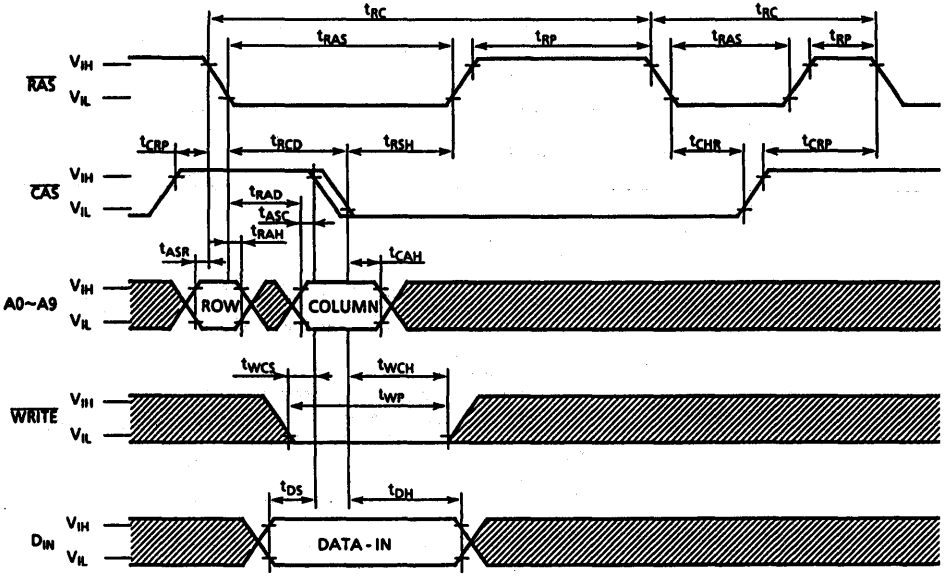
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨: "H" or "L"

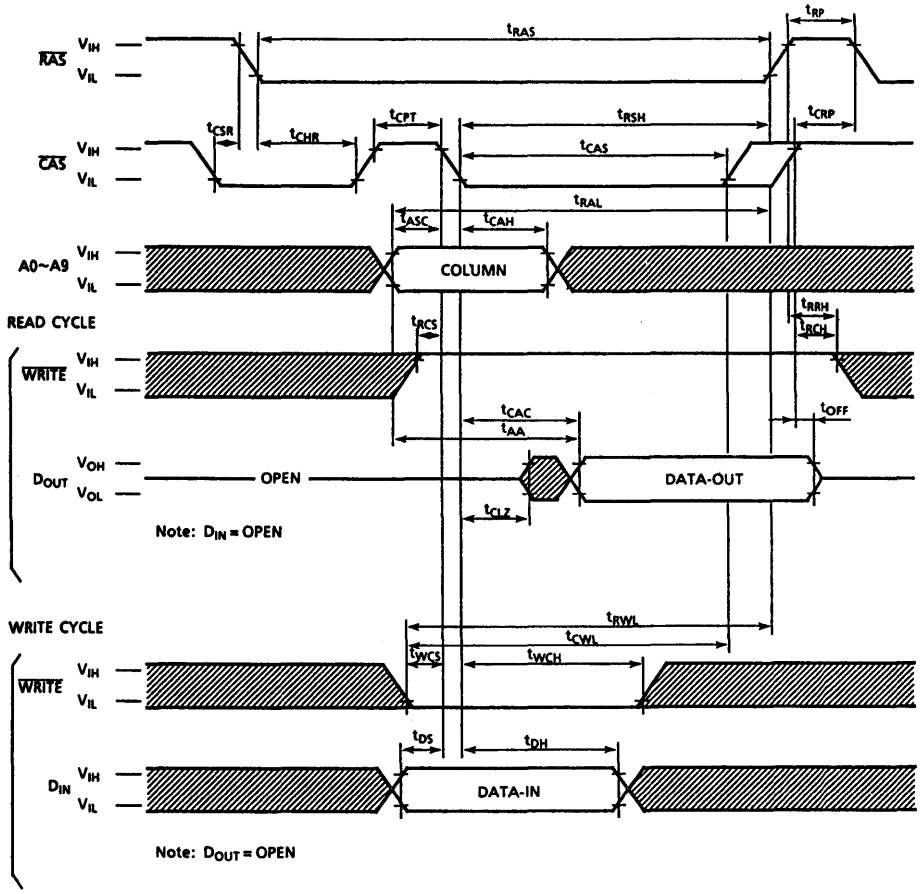
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



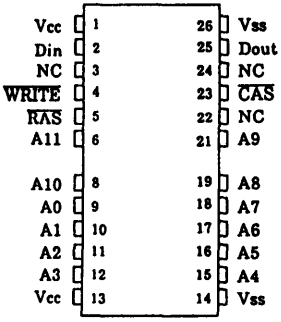
TOSHIBA 3RD GENERATION 16M DRAM

FEATURES

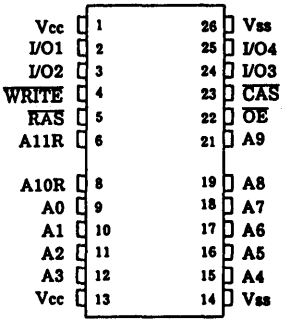
- 0.5μm Device Technology
- Single 5V/3.3V supply
  (Internal Voltage Down Converter)
- 16M Word x1 bit Organization
  4M Word x4 bit Organization
- Access Time / Cycle Time
- 5V···t_{RAC} = 50ns 3.3V···t_{RAC} = 60ns
  t_{CAC} = 12ns t_{CAC} = 15ns
  t_{AA} = 25ns t_{AA} = 30ns
  t_{CPA} = 30ns t_{CPA} = 35ns
  t_{RC} = 90ns t_{RC} = 110ns
  t_{PC} = 35ns t_{PC} = 40ns
  t_{HPC} = 20ns t_{HPC} = 25ns
- Operating/Standby Current
  Operating Current (Icc1) = 130mA (2K refresh)
  Operating Current (Icc1) = 1300mA (4K refresh)
  Standby Current (Icc5) = 1mA
- Operation Mode
  Fast Page Mode
  Hyper Page Mode
  Write Per Bit Mode (5V only)
  4$\overline{CAS}$ Function
- Refresh
  $\overline{RAS}$ only Refresh
  $\overline{CAS}$ before $\overline{RAS}$ Refresh
  Hidden Refresh
- All Inputs and Outputs are TTL Compatible
- 2048 Refresh Cycle/32ms
- 4096 Refresh Cycle/64ms
- Package
  BSJ/BST: 26 pin 300 mil Plastic SOJ/TSOP
  BJ/BFT: 28(24) pin 400 mil Plastic SOJ/TSOP (Compatible with First Generation)
  28 pin 300 mil Plastic SOJ/TSOP (4$\overline{CAS}$)

26 PIN 300MIL SOJ/TSOP PIN CONNECTION

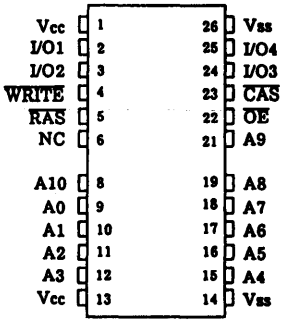
16M×1 DRAM



4M×4 DRAM (4K Refresh)

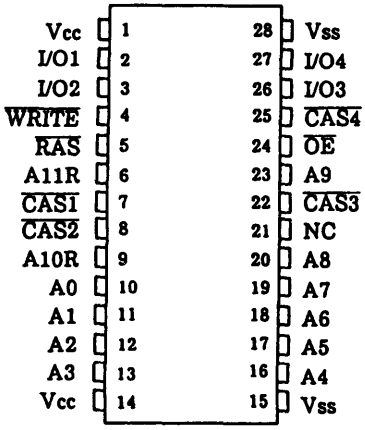


4M×4 DRAM (2K Refresh)

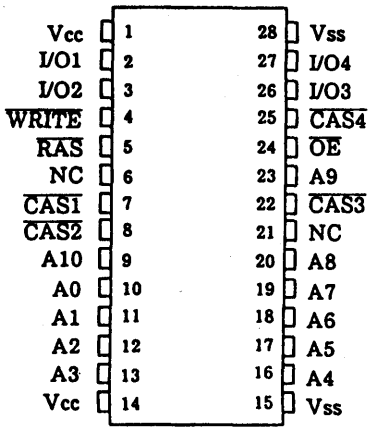


28 PIN 300MIL SOJ/TSOP PIN CONNECTION (4CAS)

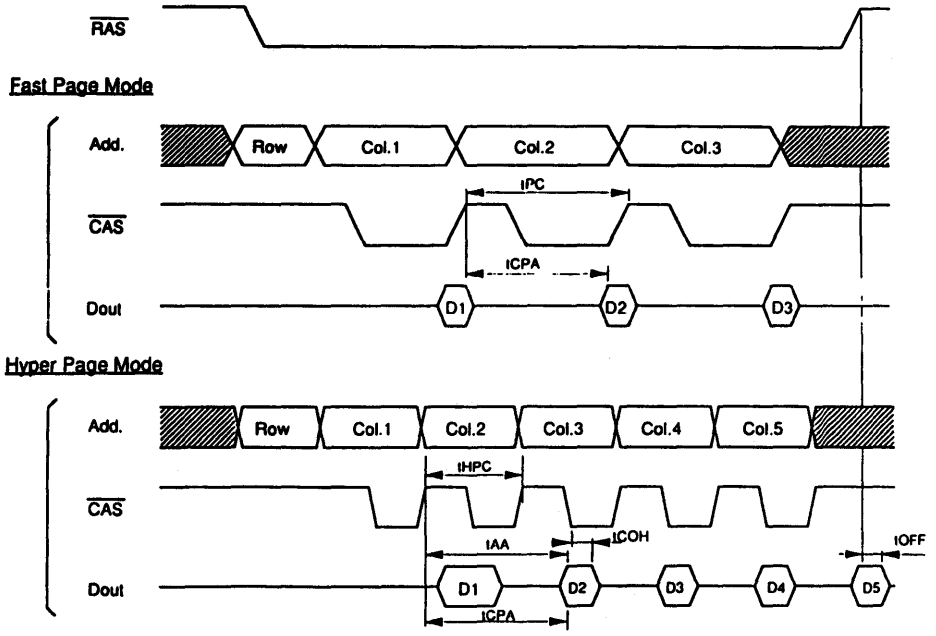
4M×4 DRAM (4K Refresh)



4M×4 DRAM (2K Refresh)



FAST PAGE VS. HYPER PAGE MODE

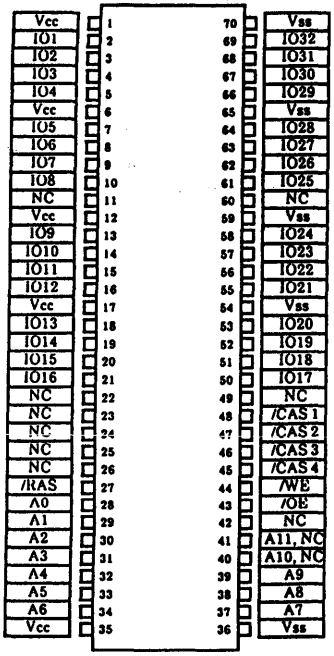


Note:

Hyper page differs from Fast Page Mode in that rising CAS does not disable the outputs. This allows the fastest possible cycle time (tHPC) to be acheived. The above timing diagram does not reflect the case where data is continually valid, as it is posible to disable the I/O's with Hyper Page Mode. Please contact your local Toshiba Sales Office for detailed Hyper Page Mode timing parameters and diagrams.

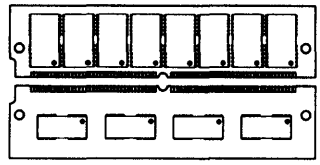
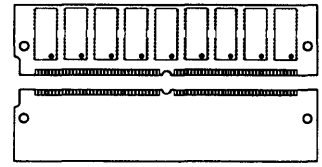
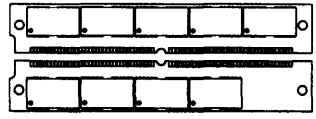
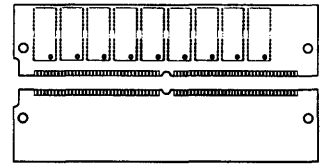
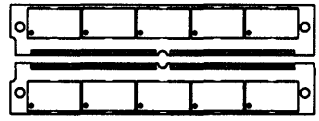
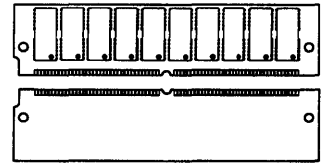
512Kx32 CMOS DYNAMIC RAM

ORGANIZATION	512Kx32
PART NO.	TC116320/18320B
PROCESS	0.5μm
POWER SUPPLY	5.0V/3.3V (VOLTAGE DOWN CONVERTER)
REFRESH	1024 CYCLES/16ms 4096 CYCLES/ms
ROW ADDRESS	A0-A11 (4K REFRESH)/A0-A9 (1K REFRESH)
COLUMN ADDRESS	A0-A6 (4K REFRESH)/A0-A8 (1K REFRESH)
ACCESS TIME (ns)	60/70/80 (5.0V) 70/80 (3.3V)
PACKAGE	400mil 70pin SOJ (0.8mm PITCH) 400mil 70pin TSOP (0.8mm PITCH)
OPERATION MODE	FAST PAGE MODE/HYPER PAGE MODE
BYTE CONTROL	4/$\overline{CAS}$

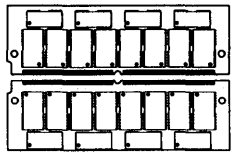
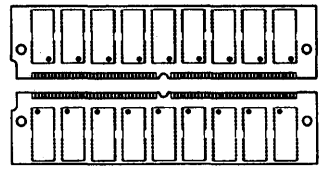
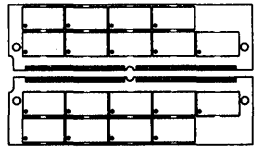
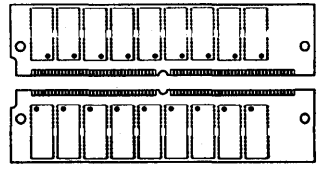
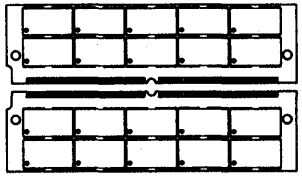
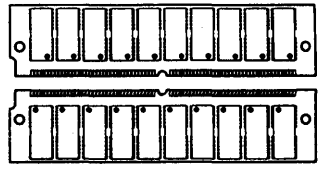


512K×32 DRAM
(70pin 400mil SOJ / TSOP)

THIRD GENERATION 16M DRAM-BASED MODULES

	1st Gen. 16M DRAM used(400mil)	3rd Gen. 16M DRAM used(300mil)
4M x36 (36bit Parity)	THM36402S/SG  • TC5117400J x8 • TC514100ASJ x4 • 22.86mm Height	THM36400BS/BSG  • TC5117400BSJ x8 • Quad CAS(4Mx4)x1 • 25.40mm Height
4M x36 (36bit ECC Module)	THM364060SG  • TC5117400J x9 • 17.78mm Height	THM364070BSG  • TC51174BSJ x9 • 25.40mm Height
4M x40 (40bit ECC Module)	THM404020SG  • TC5117400J x10 • 17.78mm Height	THM404000BSG  • TC5117400BSJ x10 • 25.40mm Height

THIRD GENERATION 16M DRAM-BASED MODULES

	1st Gen. 16M DRAM used(400mil)	3rd Gen. 16M DRAM used(300mil)
8M x36 (36bit Parity)	THM3648020S/SG  • TC5117400J x16 • TC514100ASJ x8 • 34.00mm Height	THM368020BS/BSG  • TC5117400BSJ x16 • Quad CAS(4Mx4)x2 • 25.40mm Height
8M x36 (36bit ECC Module)	THM368060SG  • TC5117400J x18 • 29.21mm Height	THM368060BSG  • TC51174BSJ x18 • 25.40mm Height
8M x40 (40bit ECC Module)	THM408020SG  • TC5117400J x20 • 29.21mm Height	THM408020BSG  • TC5117400BSJ x20 • 25.40mm Height

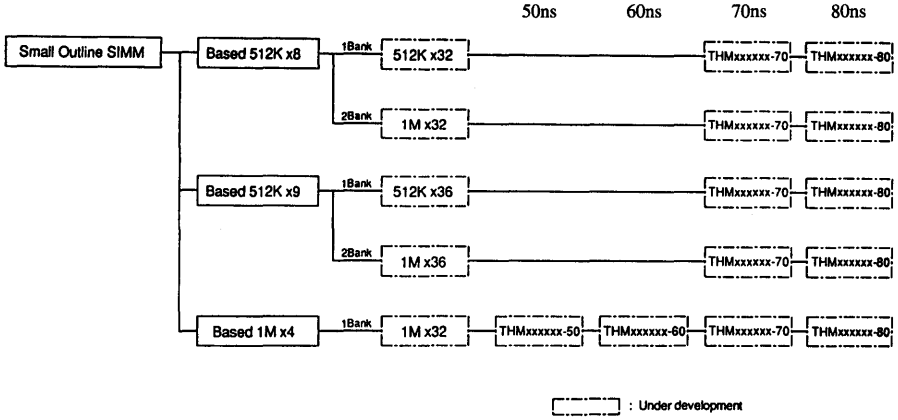
3.3V DRAM

Type		Package		Voltage Supply	Target Access Time
Organization	Gen.	SOJ	TSOP		
4M DRAM (256Kx16)	4th	○		3.3V±0.3V	70ns
16M DRAM (16Mx1, 4Mx4)	3rd	○	○	3.3V±0.3V	60ns
16M DRAM (2Mx8)	2nd	○	○	3.3V±0.3V	70ns
16M DRAM (1Mx16,x18)	2nd	○	○	3.3V±0.3V	70ns

3.3V Vcc, I/O Interface Target Spec.

Abs. Max. Rating	— 0.5~4.6V (V_{CC})
	— 0.5~V_{CC} + 0.5V≤ (Input pin)
V_{CC} Operating	3.3V ± 0.3V
V_{OL} Max. (DC)	0.4V (I_{OUT} = 2mA)
V_{OH} Min. (DC)	2.4V (I_{OUT} = -2mA)
V_{OL} Max. (DC)	0.8V (I_{OUT} = 2mA)
V_{OH} Max. (AC)	2.0V (I_{OUT} = -2mA)
V_{IL} Min.	-0.3V
V_{IL} Max.	0.8V
V_{IH} Min.	2.0V
V_{IH} Max.	V_{CC} + 0.3V

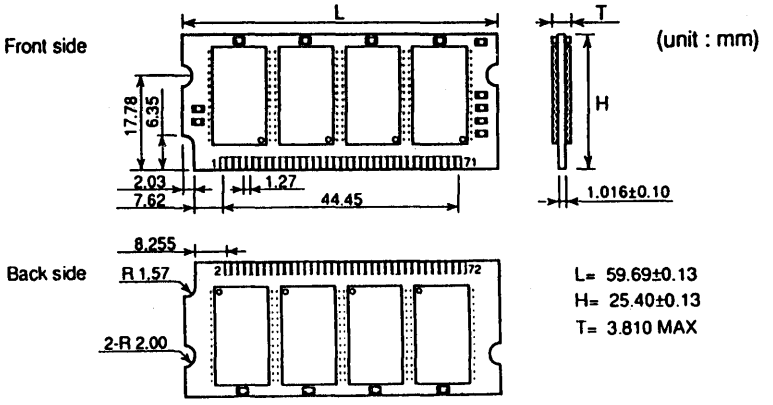
TOSHIBA SMALL OUTLINE SIMM



TOSHIBA SMALL OUTLINE SIMM

1. Outline

Dimension



Pin Count
72pin (50mil pitch 1row / zig-zag read out)

2. Data bus width

x32 / 36 bit

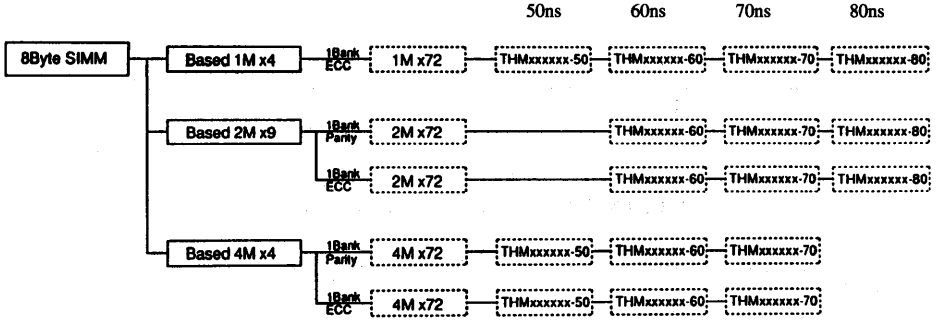
3. Maximum capacity

256M byte maximum using 256M DRAM

4. Pin function assignment

		Pin count	
Signals	**Function**	**x32**	**x36**
A0 to A13	Address input	14	14
DQ	Data-in/Data-out	32	36
/RAS	Row address strobe	4	4
/CAS	Column address strobe	4	4
/WE	Read/Write enable	1	1
Vcc	Power supply	3	3
Vss	Ground	3	3
PD	Presence detect	7	7
NC	No connection	4	0

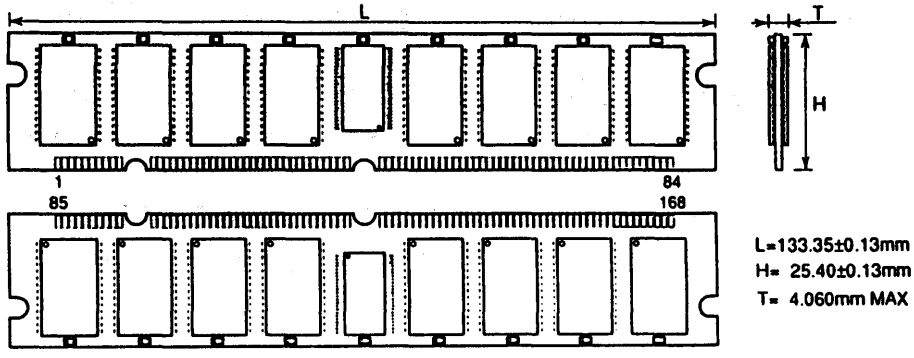
TOSHIBA 8-BYTE SIMM



TOSHIBA 8-BYTE SIMM

1. Outline

Dimension



Pin Count
168pin (50mil pitch 1row / dual read out)

2. Data bus width

x64/72 - bit (Parity mode), x72/80 - bit (ECC mode)

3. Maximum capacity

512M byte maximum using 256M DRAM

4. Pin function assignment

		Pin count		ECC mode	
Signals	**Function**	**x32**	**x36**	**x72**	**x80**
A0 to A13, B0	Address input	15	15	15	15
DQ (, PQ*)	Data-in/Data-out	64	64	72	80
/RAS	Row address strobe	4	4	4	4
/CAS	Column address strobe	8	8	8	8
/WE	Read/Write enable	2	2	2	2
/OE	Output enable	2	2	2	2
Vcc	Power supply	16	16	16	16
Vss	Ground	16	16	16	16
PD	Presence detect	8	8	8	8
ID	ID bit	2	2	2	2
/PDE	PD enable	1	1	1	1
Reserved	Presence detect	16	8	12	4
RFU	Reserved for future use	14	14	14	14

*PQ is used for x72 parity only.

DRAM/MODULE CROSS REFERENCE GUIDE

DRAM (x1/x4)

Organization	4Mxl (Fast Page)	16Mx1 (Fast Page)	1Mx4 (Fast Page)	4Mx4 (2K Refresh	4Mx4 (4K Refresh
TOSHIBA	TC514000A	TC5116100	TC514400A	TC5117400	TC5116400
Fujitsu	MB814100	MB8116100	MB814400		MB8116400
Hitachi	HM514100	HM5116100	HM514400	HM5117400	HM5116400
Micron	MT4C1004	MT4C16M1A1	MT4C4001	MT4C4M4B1	MT4C4M4A1
Mitsubishi	M5M44100		M5M44400		
Motorola	MCM514100		MCM514400		
NEC	uPD424100	uPD4216100	uPD424400	uPD4217400	uPD4216400
Oki	MSM514100		MSM514400		
Samsung	KM41C4000	KM41C16000	KM44C1000	KM44C4100	KM44C4000
Siemens	HYB514100	HYB511610	HYB514400		HYB511640
TI	TMS44100		TMS44400		

DRAM (x8/x9)

Organization	512Kx8	2Mx8 (2K Refresh)	512Kx9
TOSHIBA	TC514800A	TC5117800	TC514900A
Hitachi	HM514800		HM514900
Micron	MT4C8512	MT4C2M8B1	
Mitsubishi	M5M44800		M5M44900
NEC	uPD424800A	uPD4217800	uPD424900A

DRAM (x16/x18)

Organization	256Kx16 (2 CAS)	256Kx16 (2 WE)	1Mx16 (1K, 2 CAS)	1Mx18 (1K, 2 CAS)
TOSHIBA	TC514260B	TC514170B	TC5118160A	TC5118180A
Hitachi	HM514260	HM514170		
Micron	MT4C16257	MT4C16256	MT4C1M16C3	
Mitsubishi	M5M44260	M5M44170		
NEC	uPD424260A	uPD424170A	uPD4218160	uPD4218180

MODULE (x32)

Organization	1Mx32	2Mx32	4Mx32	8Mx32
TOSHIBA	THM321000A	THM362020A	THM364020	THM368020
Hitachi	HB56D132	HB56D232		
Micron	MT8D132	MT16D232	MT8D432	MT16D832
NEC	MC421000A32	MC422000A32	MC424000A32	MC428000A32
Oki		MSC383		

MODULE (x36)

Organization	1Mx36	2Mx36	4Mx36	8Mx36
TOSHIBA	THM361020A	THM362020A	THM364020	THM368020
Hitachi	HB56D136	HB56D236	HB56D436	HB56D836
Micron	MT9D136	MT18D236	MT12D436	MT24D836
Mitsubishi	MH1M36	MH2M36	MH4M36	
NEC	MC421000A36	MC422000A36	MC424000A36	MC428000A36
Oki	MSC2350			
Samsung	KMM5361000	KM5362000		

TOSHIBA

16M DRAM Reliability Report

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TOSHIBA AMERICA ELECTRONIC COMPONENTS. INC.

CONTENTS

I. 16M DRAM Family and Process Parameters

1) 16M DRAM (x1/x4)

Device	Org.	t_{RAC}	t_{CAC}	Special Function
TC5116100J/Z/FT/TR-60 -70	16Mx1	60 ns 70 ns	15 ns 20 ns	Fast Page
TC5116101J/Z/FT/TR-70	16Mx1	70 ns	20 ns	Nibble
TC5116102J/Z/FT/TR-70	16Mx1	70 ns	20 ns	Static Column
TC5116400J/Z/FT/TR-60 -70	4Mx4	60 ns 70 ns	15 ns 20 ns	Fast Page 4K Refresh
TC5116402J/Z/FT/TR-70	4Mx4	70 ns	20 ns	Static Column 4K Refresh
TC5116410J/Z/FT/TR-70	4Mx4	70 ns	20 ns	Fast Page Write-per-bit 4K Refresh
TC5117400J/Z/FT/TR-60 -70	4Mx4	60 ns 70 ns	15 ns 20 ns	Fast Page 2K Refresh
TC5117402J/Z/FT/TR-70	4Mx4	70 ns	20 ns	Static Column 2K Refresh
TC5117410J/Z/FT/TR-70	4Mx4	70 ns	20 ns	Fast Page Write-per-bit 2K Refresh

J:SOJ package
Z:ZIP package
FT:Normal TSOP package
TR:Reverse TSOP package

2) Key Process Parameters

1st Generation 16M DRAM

Process	Triple-well CMOS Double-Poly/WSi2/Double-Metal
Feature Size	0.6 µm
External Voltage	5V
Internal Voltage	4V
Transistor Lpoly tox	0.7 µm (n-ch) 0.9 µm (p-ch) 160Å
Memory Cell Cell Size Structure tox (ONO)	1.57 X 2.95 µm2 (4.63 µm2) Trench 100Å (effective)

Bonding Options:x1/x4
Fast Page / Nibble / Static Column Mode

3) 16M DRAM (x8, x9, x16, x18)

Device	Org.	t_{RAC}	t_{CAC}	Special Function
TC5116800ANJ/ANT/ANR-60 -70	2Mx8	60 ns 70 ns	15 ns 20 ns	Fast Page 4K Refresh
TC5117800ANJ/ANT/ANR-60 -70	2Mx8	60 ns 70 ns	15 ns 20 ns	Fast Page 2K Refresh
TC5116900AJ/AFT/ATR-60 -70	2Mx9	60 ns 70 ns	15 ns 20 ns	Fast Page 4K Refresh
TC5117900AJ/AFT/ATR-60 -70	2Mx9	60 ns 70 ns	20 ns	Fast Page 2K Refresh
TC5116160AJ/AFT/ATR-60 -70	1Mx16	60 ns 70 ns	15 ns 20 ns	Fast Page 4K Refresh 2 CAS, 1 WE
TC5118160AJ/AFT/ATR-70 -80	1Mx16	70 ns 80 ns	20 ns 20 ns	Fast Page 1K Refresh 2 CAS, 1 WE
TC5116180AJ/AFT/ATR-60 -70	1Mx18	60 ns 70 ns	15 ns 20 ns	Fast Page 4K Refresh 2 CAS, 1 WE
TC5118180AJ/AFT/ATR-70 -80	1Mx18	70 ns 80 ns	20 ns 20 ns	Fast Page 1K Refresh 2 CAS, 1 WE

AJ:SOJ package (2Mx9:32 pin, 1Mx16/18:42 pin)
ANJ:SOJ package (2Mx8:28 pin)
AFT:TSOP package (2Mx9:32 pin, 1Mx16/18:50/44 pin)
ANT:TSOP package (2Mx8:28 pin)
ATR:Reverse TSOP package (2Mx9:32 pin, 1Mx16/18:50/44 pin)
ANR:Reverse TSOP package (2Mx8:28 pin)

II. Major reliability study

The first generation 16M DRAM is a CMOS device based on 0.6 mm design rule. This section details the reliability of the Toshiba 16M DRAM technology.

1) Oxide Breakdown

Time Dependent Dielectric Breakdown (TDDB) of the 16M DRAM gate oxide is very critical because of the very thin oxide layer. (,100Å). The TDDB failure rate greatly depends on the process.

Figure II-1 shows the TDDB results for the 16M DRAM process. The reliability of this process exceeds 10 years even with stress induced by a 5 MV/cm electric field. In order to reduce the electric field in the 16M DRAM memory cell capacitor, a 1/2 VINT cell plate is used.

In order to estimate the field failure rate of actual devices, it is necessary to derive the acceleration factor. The relation between the time to failure (tF) and the stress condition is given by the following equation1).

$t_F = A\, e[-bV + (Ea/kT)]$ (1)

where

A=constant
E_a=activation energy (eV)
k=Boltzmann's constant (1.38×10^{-23} J/K)
T=absolute temperature (K)
V=stress voltage (V)
β=voltage acceleration factor

The numerical values for the E_a and β parameters were determined experimentally to be the following.
$E_a = 0.3$ eV
$\beta = 3$

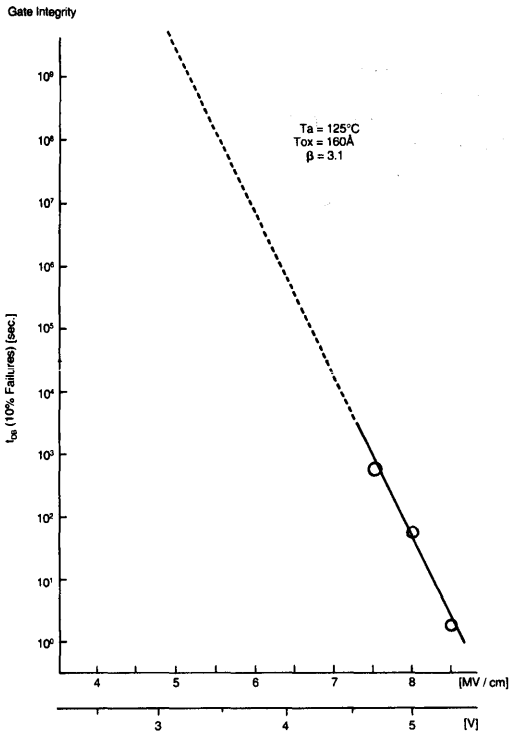


Figure II-1. TDDB Results for the 16M DRAM

2) Electromigration

It has been established that, when a high density current is applied to the Al metal, an open circuit can result in this metal. This phenomenon is known as electromigration and is one of the critical failure mechanisms relative to the narrow Al line width of the large scale devices.

The mechanism of electromigration on a thin film is explained as follows.

While current flows in the thin film, an electron wind force is applied on the metallic atoms. As a result, the Al atoms diffuse in the direction of the electron flow (from cathode to anode), forming a void on the cathode side, and a hillock or a whisker on the anode side.

The open circuit failure on the thin film occurs when the mass movement in the metal becomes uneven. This unevenness is caused by variations in temperature, current density or transfer rate of Al ions. For example, (1) uneven Al grain size2), (2) generation of device3), and (3) metal in contact with other materials4).

The electromigration life of the thin film is generally expressed as the mean life (MTTF : Mean Time To Failure) as shown below5).

$$MTTF = AJ^{-n} e^{(E_a/kT)} \qquad (2)$$

where J is the current density, n is a constant in relation to current density, Ea is the activation energy, T is the absolute temperature, k is Boltzmann's constant, and A is a constant in relation to the material, structure, and size of the metal. From this expression, it is understood that the mean life increases with the decrease of current density or temperature. Also, the life distribution approximates the log normal distribution with small dispersion.

Figure II-2a shows the test condition for the electromigration test. Figures II-2b and II-2c show the results of this test for the lines and vias, respectively. The stress conditions are J = 23106 and Ta = 200°C.

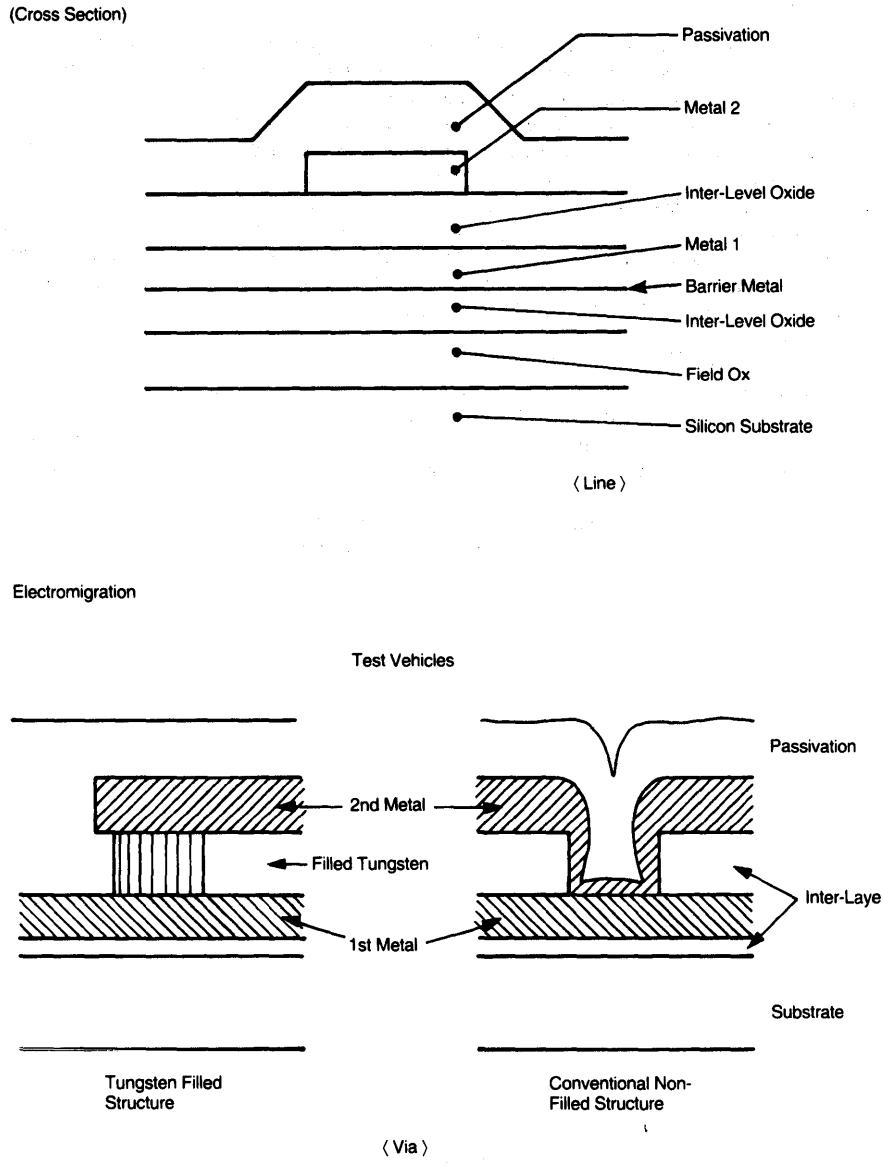


Figure II-2a. Test Conditions for the 16M DRAM Electromigration Test

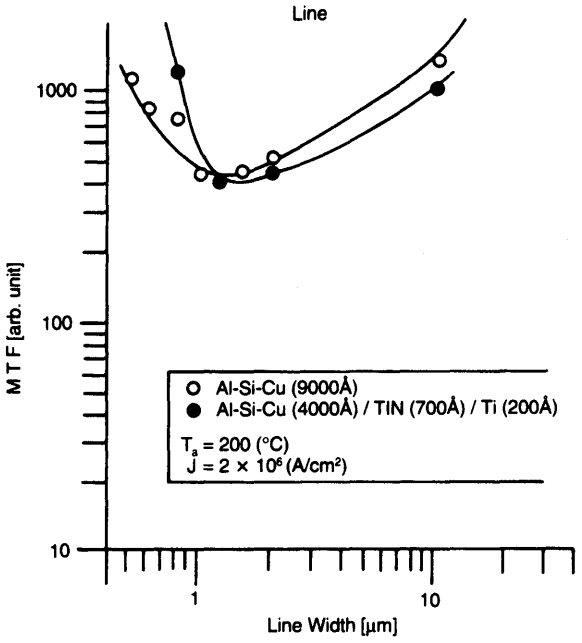


Figure II-2b. 16M DRAM Electromigration Test Results for Lines

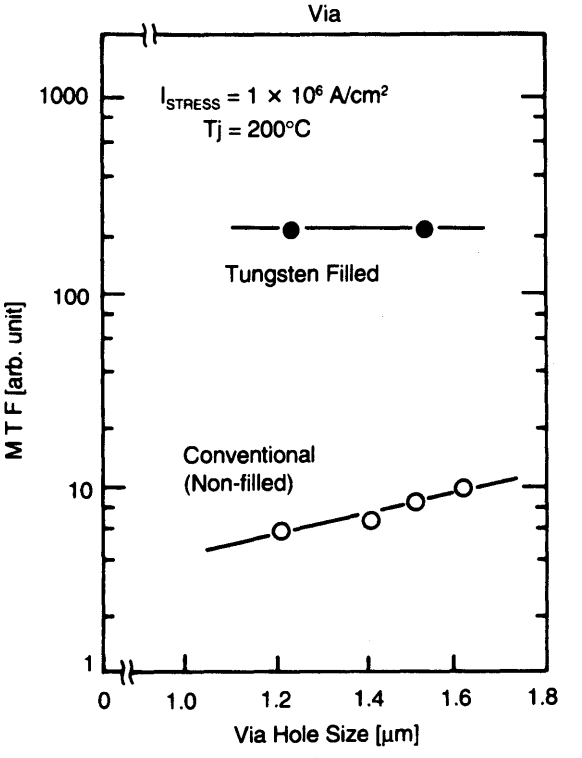


Figure II-2c. 16M DRAM Electromigration Test Results for Vias

3) Hot electron injection[6]

The N channel MOS transistor, while operating in the saturation region, generates a large electric field in the depletion region around the drain. Electrons, the carriers of the channel current, are accelerated and applied with high energy in this region (hot electron) and some of these electrons are scattered as photons and others may lose energy through the impact ionization. Some of the electrons scattered as photons and ionized by the impact are injected through the Si-SiO2 interface to the interior of the gate oxide film. A few of the injected electrons are trapped in the gate oxide film, and the others move in the oxide film to be absorbed in the gate electrode. The electrons are trapped, primarily, at the pinch-off point around the drain and cause a shift in the threshold voltage (Vth) during operation over a long period of time. LDD (Lighted Doped Drain) transistors are used in the 16M DRAM to reduce the Vth shift during operation.

Figures II-3a and II-3b show the hot carrier reliability duty ratio and hot carrier reliability DC stress for the 16M DRAM, respectively.

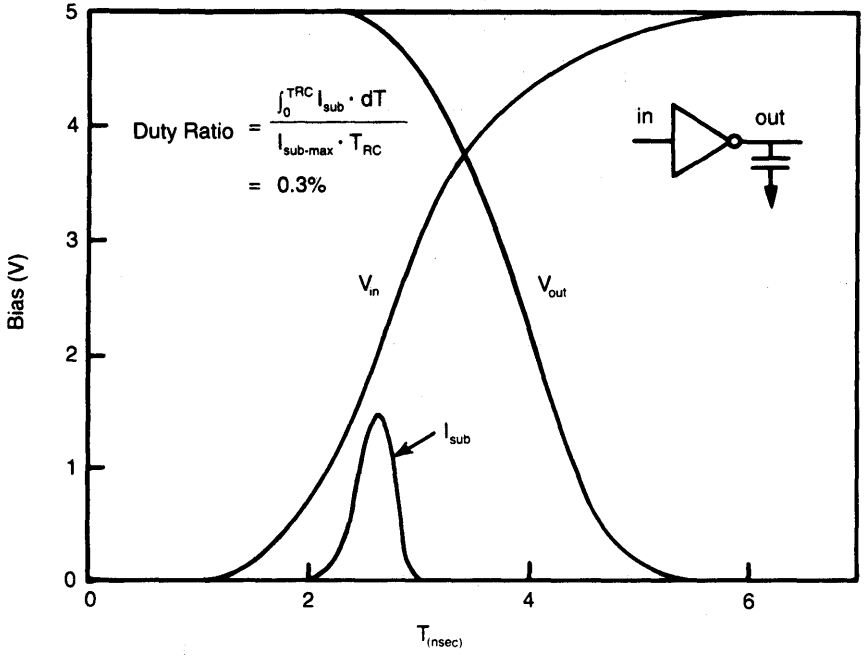


Figure II-3a. Hot Carrier Reliability Duty Ratio

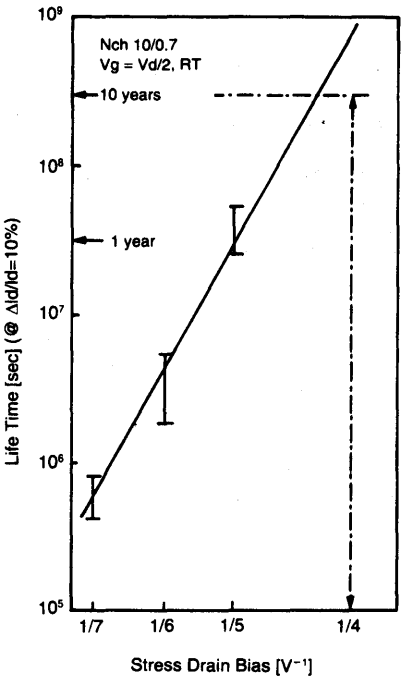


Figure II-3b. Hot Carrier Reliability DC Stress

4) Soft Error

As memory density and circuit complexity increase, concern about the DRAM's susceptibility to soft errors also increases because the higher levels of integration have primarily been achieved through a reduction of the storage cell size.

Soft Errors are random, non-recurring, single-bit errors which may be induced by alpha particles emitted by radioisotopes in the package material during decay. Electron-hole pairs are generated as the alpha particles lose energy after they penetrate the substrate. The electrons are drawn into the storage cells while the holes are drawn into the substrate. If the charges collected in the cell exceed the critical charge, a cell mode soft error will result. A bit-line soft error can also occur if alpha particles hit a floating node while a bit line is open. As a result bit-line soft errors have a higher rate of occurrence with faster cycle times.

Toshiba has implemented the following countermeasures which have been extremely effective in reducing the soft error rates (SER).

i) Thin oxide films to increase the cell capacitance in order to maintain a high critical charge level.

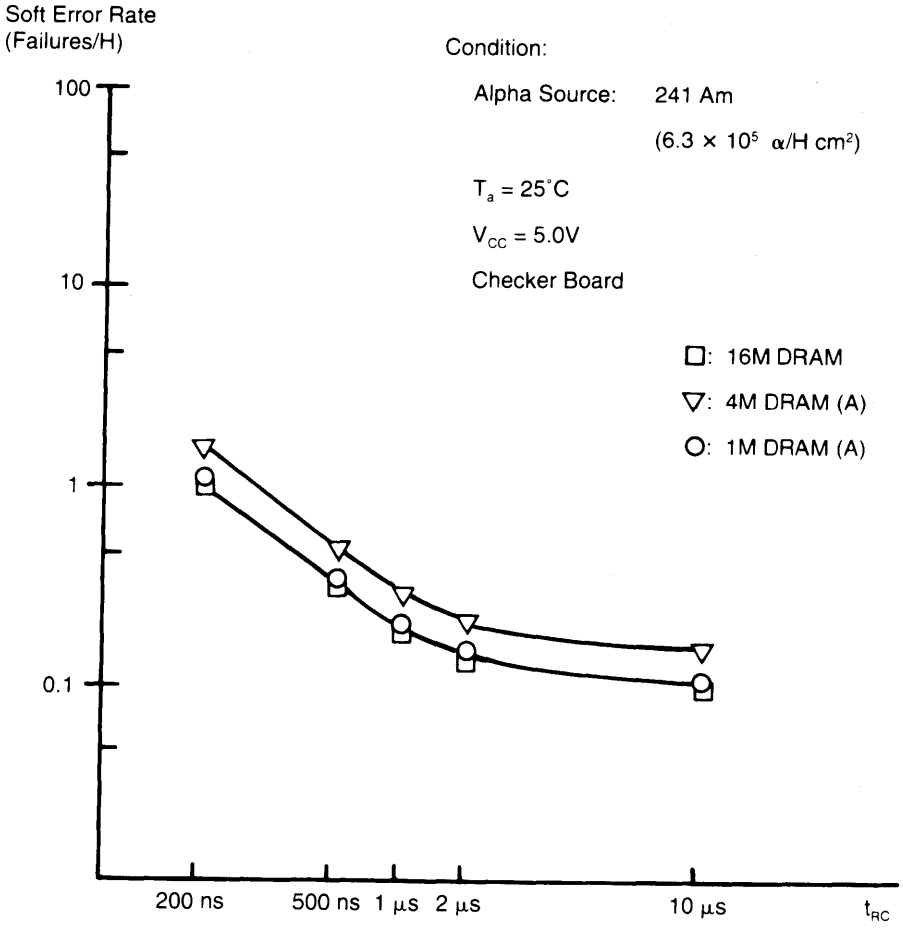
ii) A high grade resin to minimize alpha particle emissions from the packaging material.

Figure II-4 shows the SER test results of our 16M DRAM as compared to the 1M and 4M DRAMS.

Note :

Soft Error Rates can also be caused by excessive system noise levels and other operating conditions such as voltage supply level and timing conditions. A careful system design and an adequate board layout will help prevent the occurrence of this type of soft error.

Accelerated Test Results



System Test Results

Test Device	Device Hour	Number of fail	Estimated Soft Error Rate (C.L. = 60%)
TC514100A	4.14×10^6	2	748 Fit
TC5116100	2.24×10^6	1	902 Fit

Test Conditions: V_{CC} = 5V T_a = 35°C
t_{RC} = 1 μs
Test pattern: Checker board

Figure II-4. 16M DRAM Soft Error Rate Test Results

5) ESD sensitivity

Concerns about Electro-Static Discharge (ESD) increased as thinner oxide gates and fine design rule were used in higher density devices. ESD damage results from stray discharge on the device input pins and can cause gate oxide failure. Static electricity may be encountered during all stages of the manufacturing process, during shipping and during handling by the customer. To protect the devices from damage caused by the high voltages generated from static electricity, all inputs are provided with an input protection circuit.

The input protection circuit of the Toshiba 16M DRAM is shown in Figure II-5a. The resistance (R1) attenuates fast rise time large positive voltage spikes, while the diode (D1) acts to discharge the electricity to V_{SS}.

The input protection circuit is tested with the following models which simulate ESD-induced failure mechanisms:

	Test Method	Test Results
i) The human body model	Figure 5b	Figure 5c
ii) The machine model	Figure 5b	Figure 5d

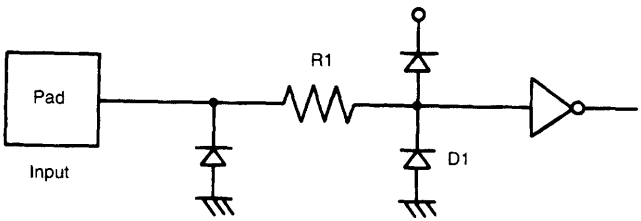


Figure II-5a. 16M DRAM Input Protection Circuit

TC5116400/0210J ESD Protection TEST Circuit

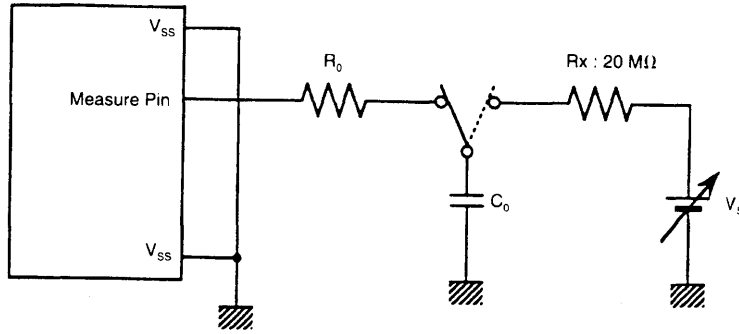
Human Body Model: R_0 = 1.5 KΩ

C_0 = 100 pF

Machine Model: R_0 = 0Ω

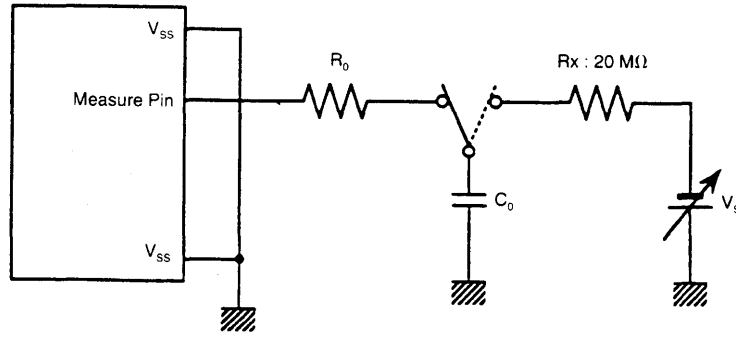
C_0 = 200 pF

Plus



Other Pins OPEN

Minus



Other Pins OPEN

Figure II-5b. Human Body and Machine Model Test Methods

TC5116400/02/10J

Internal Qualification Data for ESD

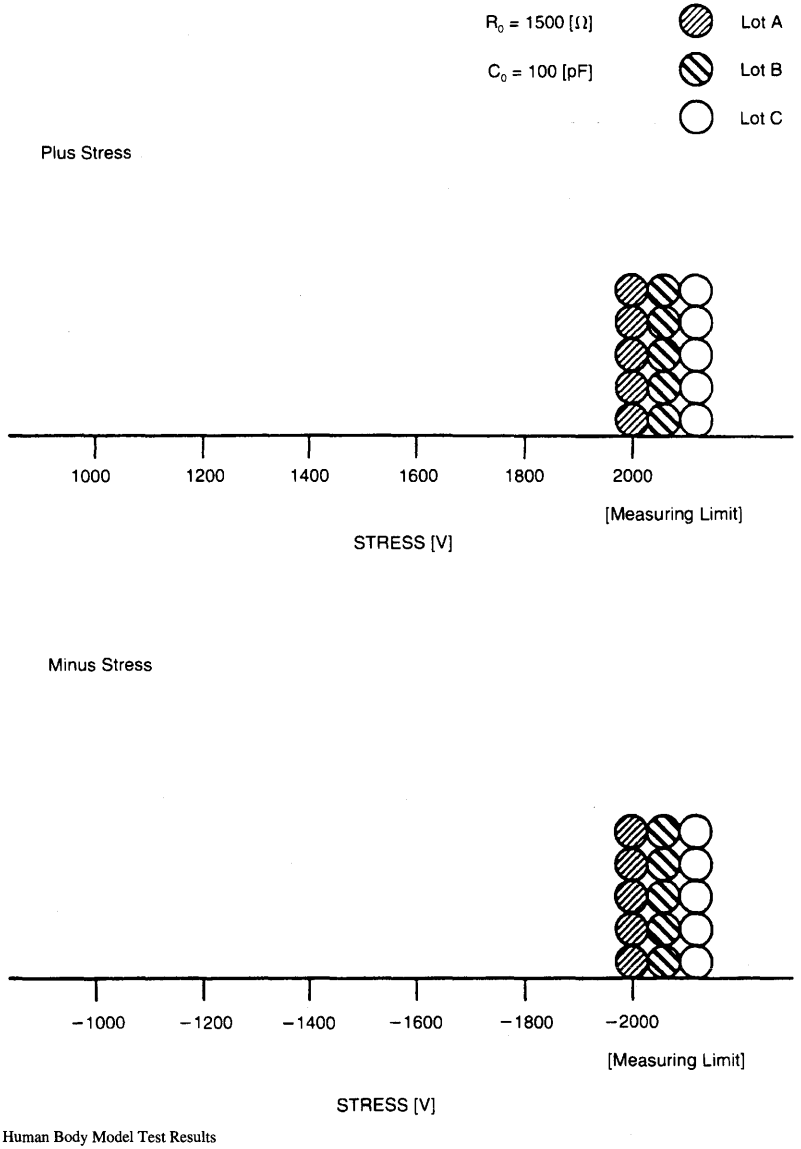


Figure II-5c. Human Body Model Test Results

TCC5116400/02/10J
Internal Qualification Data for ESD

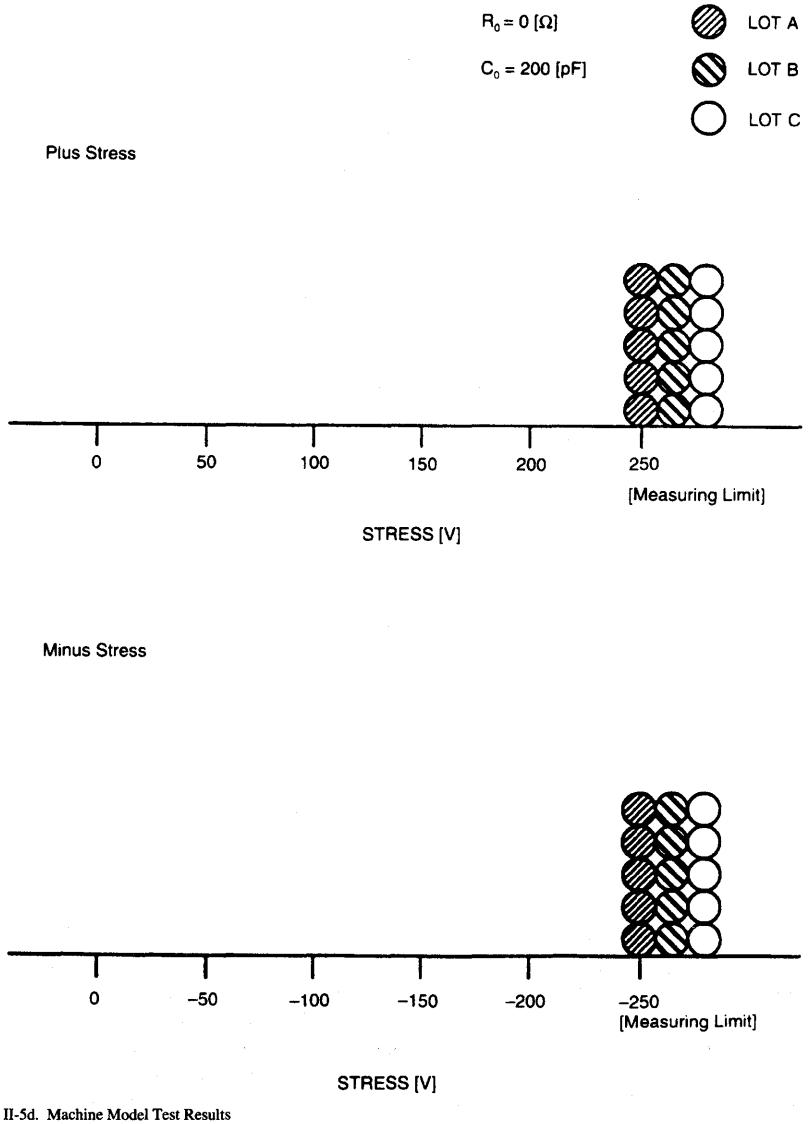


Figure II-5d. Machine Model Test Results

6) Latch-up

CMOS devices have intrinsically parasitic thyristors which are composed of parasitic npn and pnp transistors, as shown in Figures II-6a and II-6b.

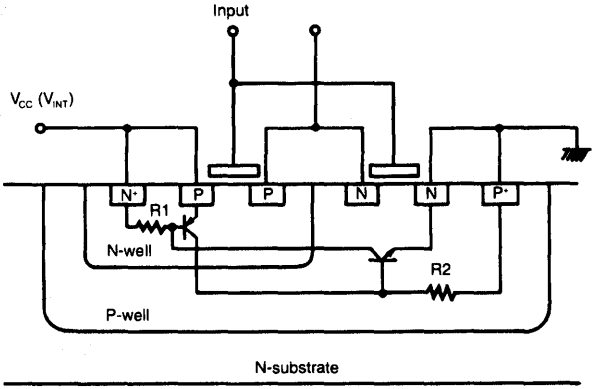


Figure II-6a. Example of parasitic bipolar transistor of a CMOS device

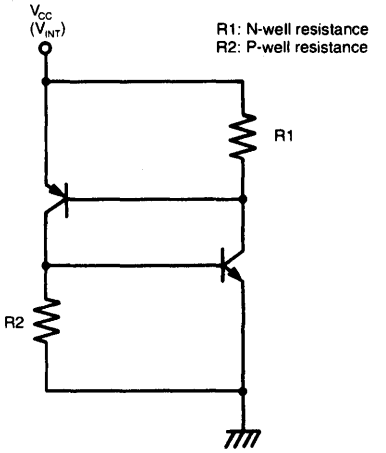


Figure II-6b. Equivalent Circuit

Latch-up is a phenomenon which occurs when these parasitic thyristors are turned on, resulting in a low impedance path from VCC to ground (VSS) which usually exceeds the current handling capability of the on-chip metallization. Latch-up can be triggered when sufficient current is induced by noise on the input, output or VCC pins, resulting in the flow of excessive current from VCC to VSS which continues to flow until VCC is turned off. Latch-up initially causes functional device failure and finally causes thermal destruction. With increased circuit densities and finer design rules, latch-up sensitivity became more critical. Latch-up immunity for devices such as the 16M DRAM has been improved through the use of the following techniques:

i) Input protection resistances are placed in input circuits.

ii) The critical resistance of the N-well, P-well, and the N-substrate is greatly reduced with the use of a guard ring.

Toshiba's latch-up test method is shown in Figure II-6c. The test results, shown in Figure II-6d, indicate that our 16M DRAMs have a high resistance to latch-up.

16M DRAM Latch up TEST Circuit

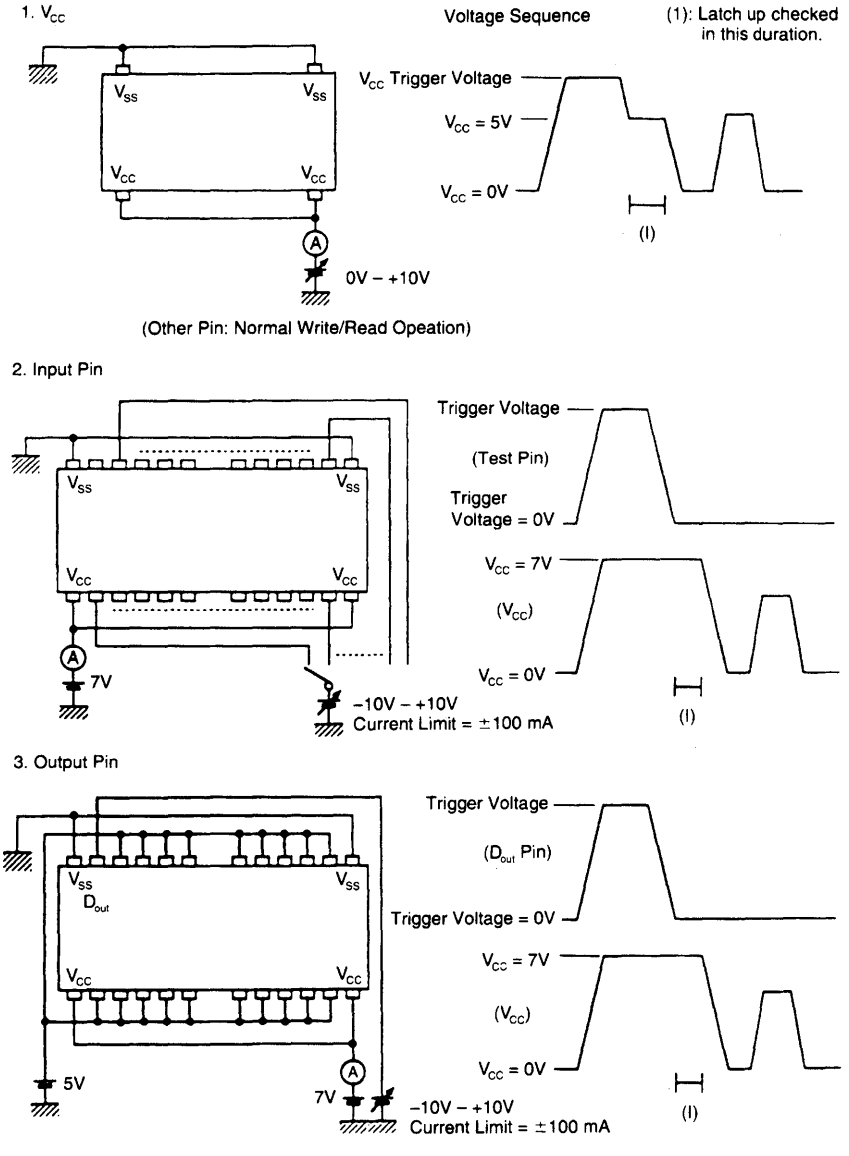


Figure II-6c. Latch-up Test Method

16M DRAM Latch up Test Result

Measured Pin	Spec.	Sample Size	Result
VCC	+10V	5 pcs x 3 Lot	15 / 15 Pass
Input	+10V or ±100mA	5 pcs x 3 Lot	15 / 15 Pass
Output	+10V or ±100mA	5 pcs x 3 Lot	15 / 15 Pass

Figure II-6d. Latch-up Test Results

7) Temperature cycling

One of the most serious problems for a large die size is an increase in the package resin stress. Figure II-7a shows a simulation of the shear stress distribution on the die using the finite element method. The shear stress is concentrated on the corner of the die.

Known failure modes caused by the stress consist of package crack, top passivation crack and metal open due to deformation. A low stress resin and a polyimide coating are used for the 16M DRAM in order to prevent these failures.

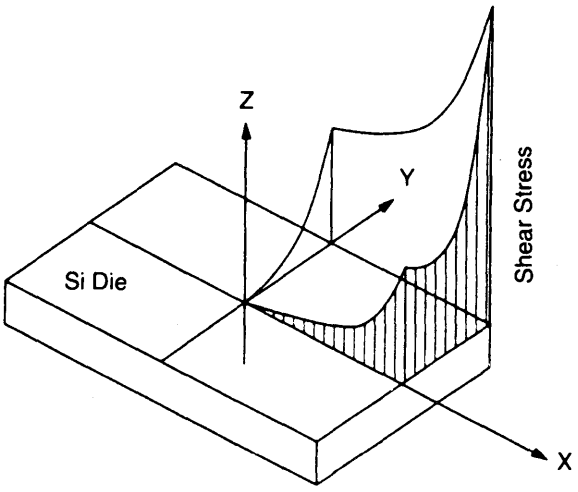


Figure II-7a. Resin Stress Distribution Over a Die
(Three-dimensional finite element method)

Figure II-7b shows the relation between number of cycles to 1% failure rate and temperature differences (DT) of the Temperature Cycling Test (TCT), where devices with conventional resis and without die coating are used.

300 cycles of TCT (265°C/150°C) guarantee more than 10 years of field use (Δ = 75°C, 2 cycles/day).

The low stress resin and polyimide coating further extend the life expectancy of Toshiba's 16M DRAM's.

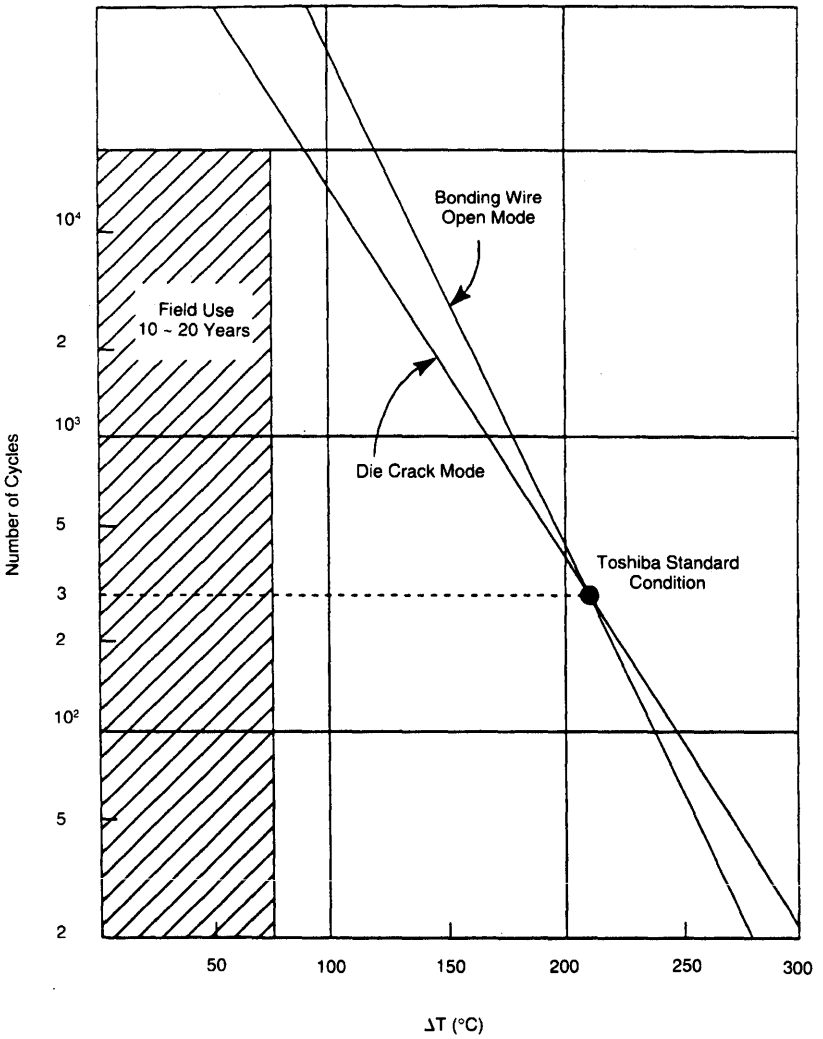


Figure II-7b. Temperature Dependence of TCT Failures

8) Humidity study

Problems associated with humidity become more critical as the die size increases because of the shorter path between the outer lead frame and the die despite improvement of the packaging material. For devices with fine design rule, moisture penetration will also cause electrical parameter shifting due, in particular, to a voltage threshold Vth drift in the P-channel transistors.

Figure II-8a shows the humidity test results using TEG devices and the temperature dependency (with relative humidity fixed at 85%) is given as

E_a = 0.8 eV for Al corrosion and E_a = 1.0 eV for parameter shift ($\propto e^{[-E_a/kT]}$).

E_a = 0.8 eV indicates that 2000 hours of 85°C/85% or 120 hours of 130°C/85% guarantees 10 years of field use at 40°C/85%.

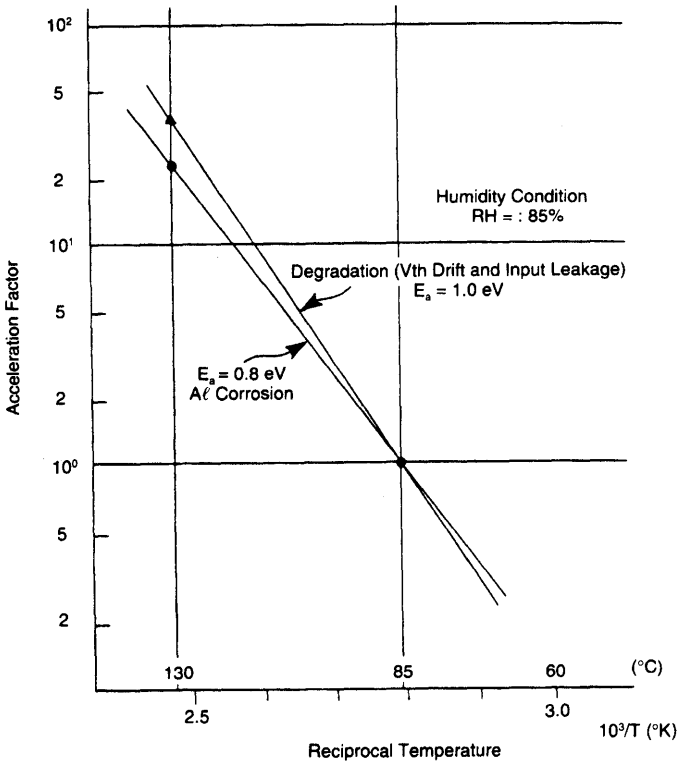


Figure II-8a. Temperature Dependence of Humidity Failure

9) SOJ package reliability during the soldering process

Plastic surface mount packages are susceptible to cracking induced by moisture absorption. Epoxy resin molded packages have a strong tendency to absorb moisture. The absorbed moisture vaporizes when the package is exposed to an abrupt and extreme transition in temperature during reflow soldering. The resulting pressure of the water vapor can cause the package to crack.

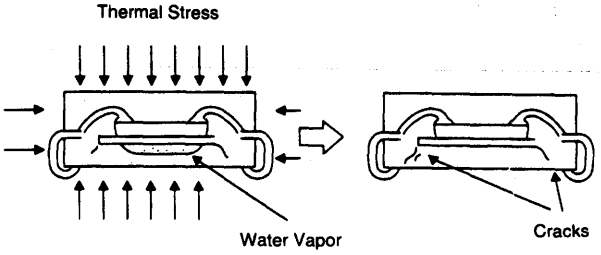


Figure II-9a. Mechanism of Package Crack

Moisture absorption and desorption characteristics of the 16M DRAM SOJ and TSOP packages are shown in Figures II-9b, c, d and e, respectively.

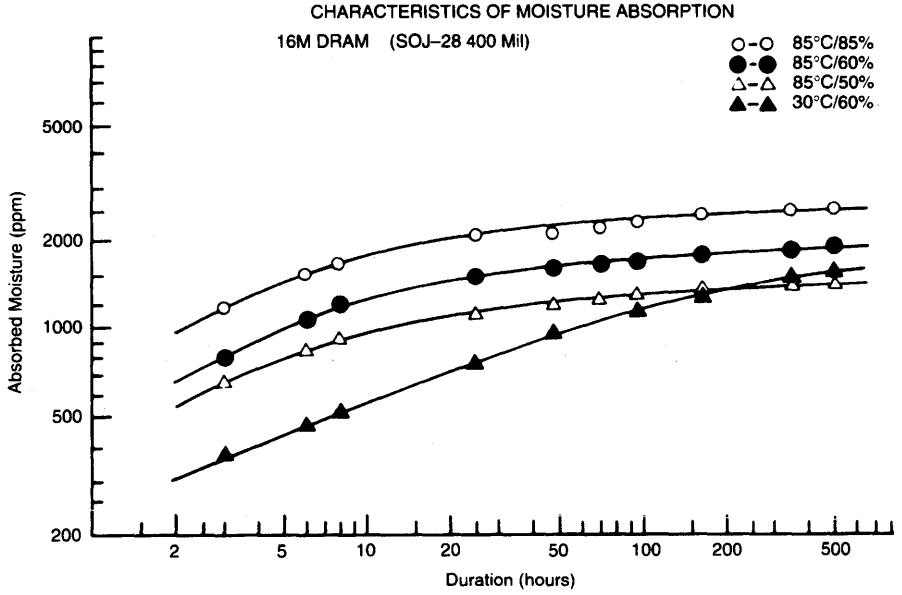


Figure II-9b. Characteristics of Moisture Absorption
16M DRAM (SOJ-28 400 Mil)

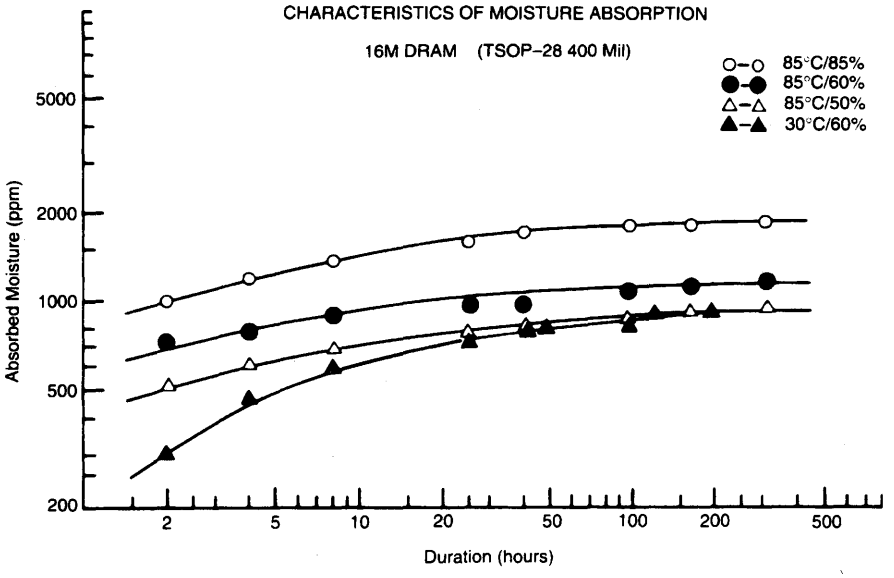


Figure II-9c. Characteristics of Moisture Absorption
16M DRAM (TSOP-28 400 Mil)

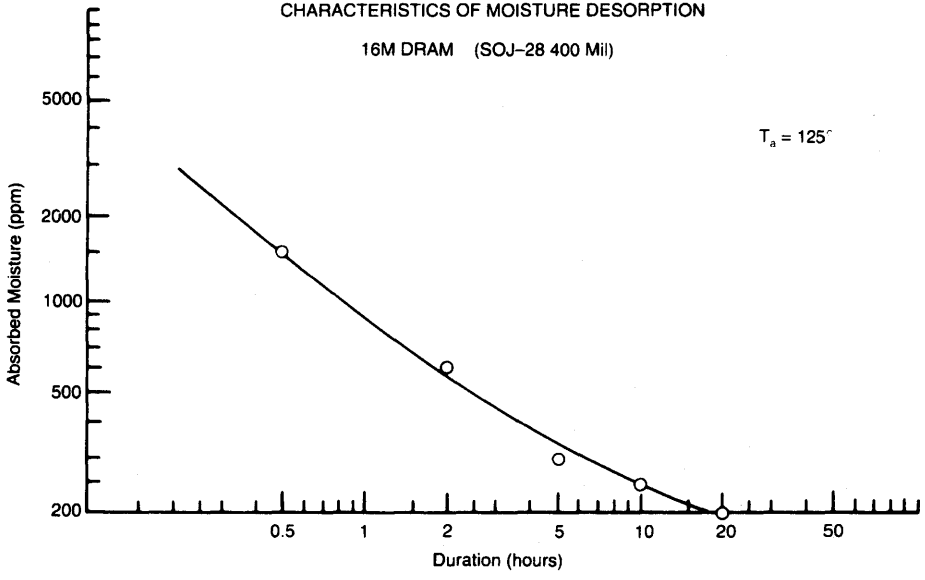


Figure II-9d. Characteristics of Moisture Desorption
16M DRAM (SOJ-28 400 Mil)

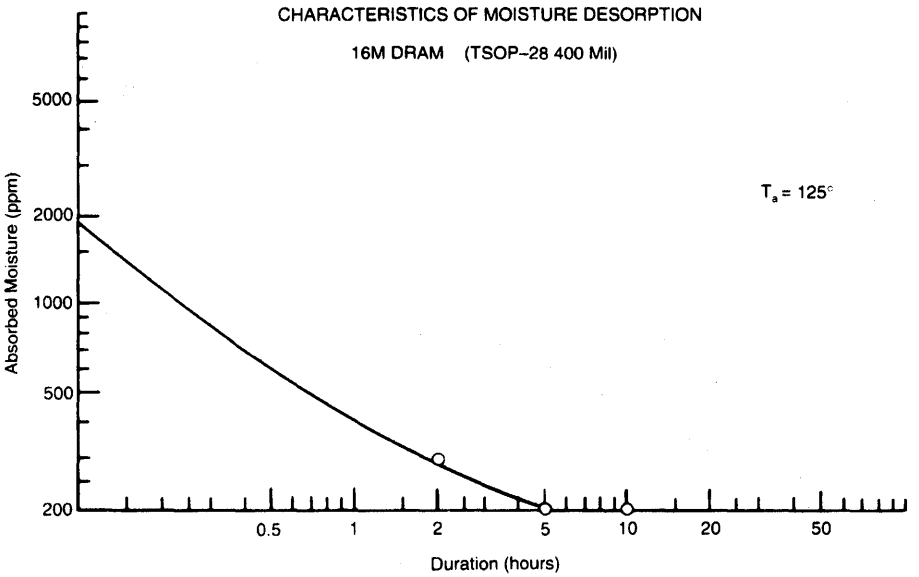


Figure II-9e. Characteristics of Moisture Desorption
16M DRAM (TSOP-28 400 Mil)

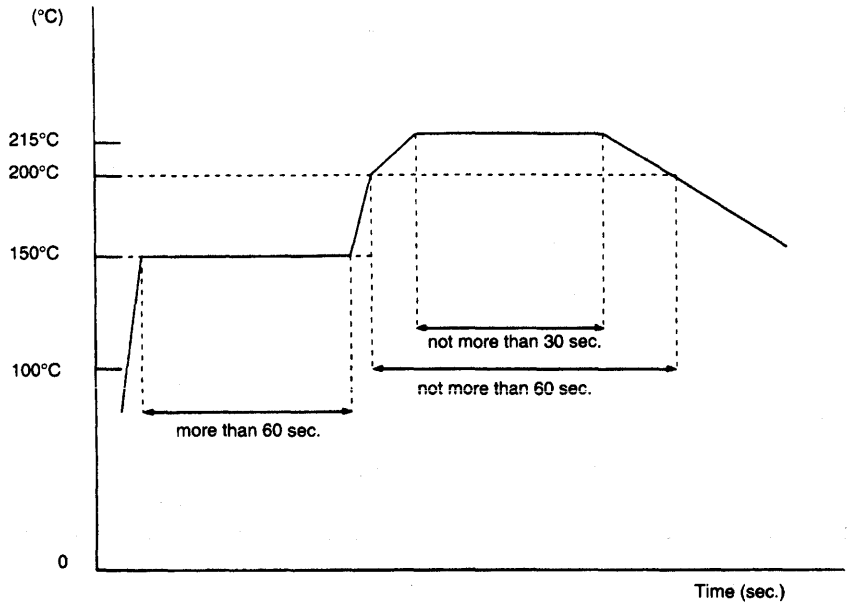
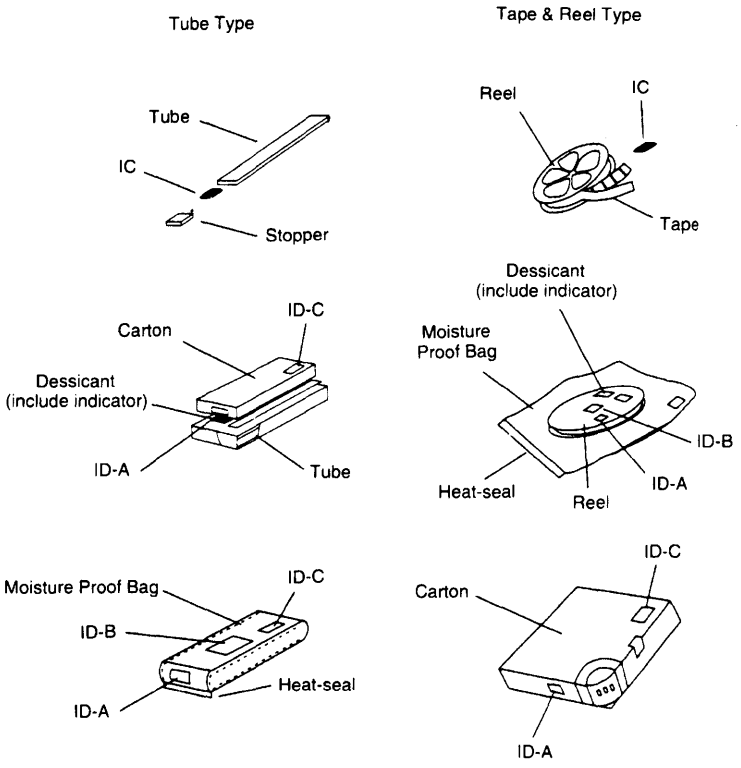


Figure II-9g. V.P.S.Reflow Curve

To prevent surface mount package cracks, pre-baking is necessary in order to exhaust the moisture content of the package prior to soldering. With the new Toshiba dry packing method the customers will be given the benefit of eliminating the pre-baking step in their process.

Dry packing methods for both tube type and tape and reel tape surface mount packages are shown in Figure II-9f.



note *As the material of moisture proof bag, a laminated aluminum is used.
*ID:Identification – A (ID-A)
Part Number, Date Code, Quantity (by labelling or pricing)
*ID:Identification – B (ID-B)
Precaution after opening dry packing (by printing)
*ID:Identification – C (ID-C)
Precaution for strategic product control (by labelling or printing) — COCOM control product only.

Figure II-9f. Dry Packing Methods

Recommended Soldering Methods for Soldering SOJ and TSOP:

A. Vapor phase soldering process:

1)Fluorinert FC-70* or equivalent should be used as heating media.
(*3M's registered trade name)

2)To be performed at ambient temperature of 215°C for not more than 30 sec. and at 200°C for not more than 60 sec.

3)Refer to the figure below as an example of the recommended temperature profile.

B. IR reflow

1)Middle/far IR and both side heaters should be used. (See Figure II-9h.)

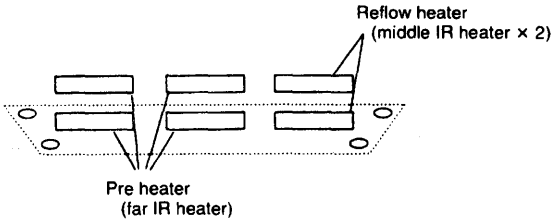


Figure II-9h. IR Reflow Equipment

2)Refer to the figure below as an example of recommended temperature profile.

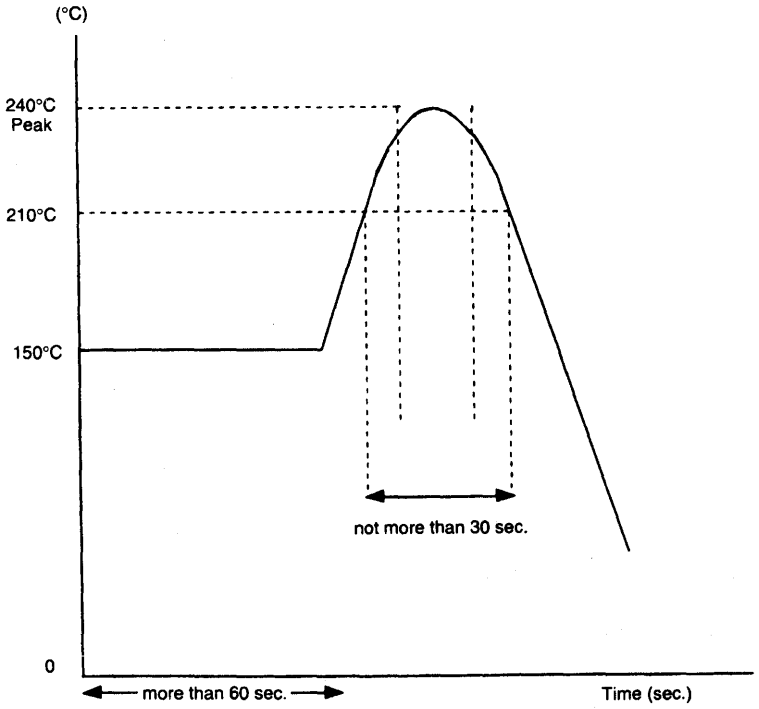
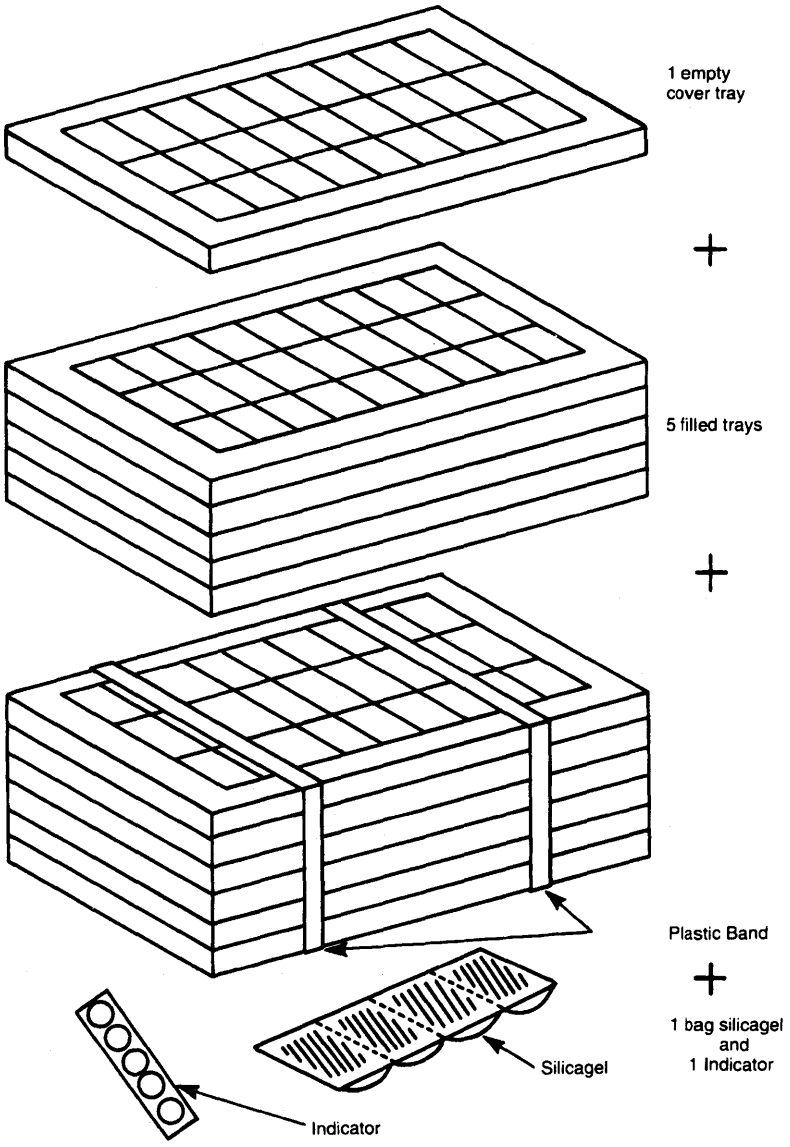
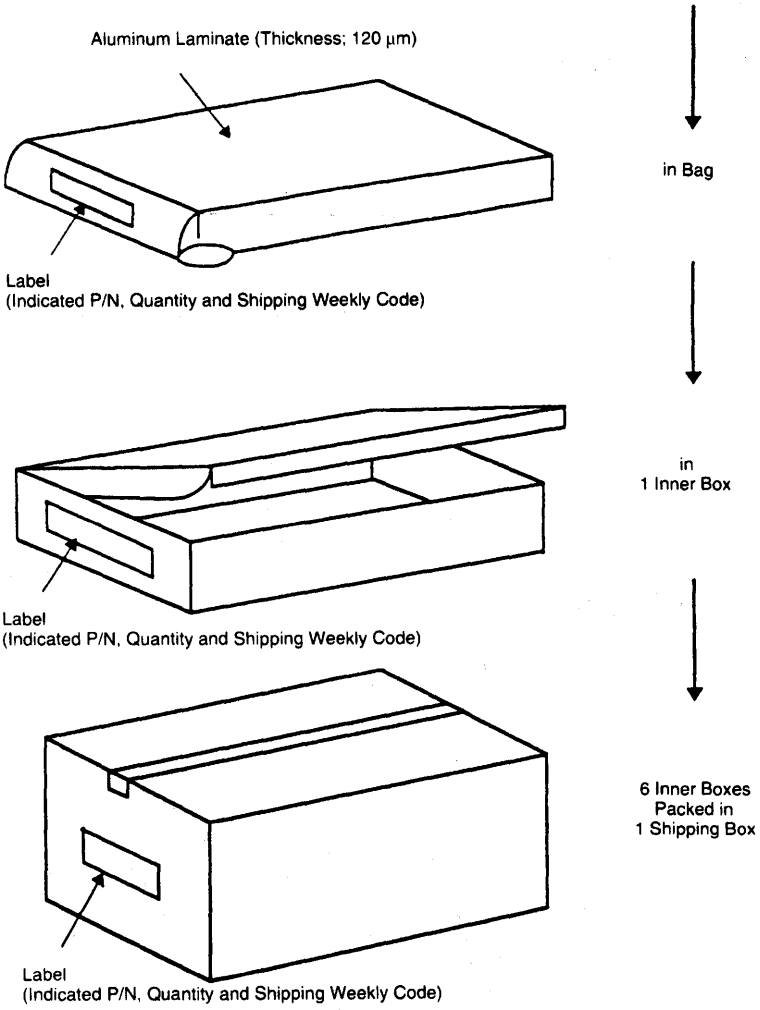


Figure II-9i. IR Reflow Curve

Shipping Form for TSOP

1) Outline of Packaging





2) Number of TSOP per Shipping Box

No. of Pin	No. of TSOP per Tray	No. of Trays per Inner Box	No. of TSOPs per Inner Box	No. of Inner Boxes per Shipping Box	No. of TSOPs per Shipping Box
24 26 28 32 44	60 pcs	5+1 cover	300 pcs	6	1800

III. Quality and Reliability Assurance

1)At the stage of new device development:
Internal qualification tests are performed for the purpose of verifying the desired characteristics and reliability levels. TEG qualification for new technologies, prior to products qualification, are applied as shown in Figure III-a. Internal qualification results for products are shown in section IV.

2)At the stage of mass production:
In order to monitor the quality and reliability, lot quality assurance inspections and a periodical reliability test (long term life test) are performed on the finished products on a sampling basis, as shown in Figure III-b. If the acceptance criteria is not met during the lot assurance test, all the devices in the lot are tested or burned-in again or scraped, depending on the failure category.

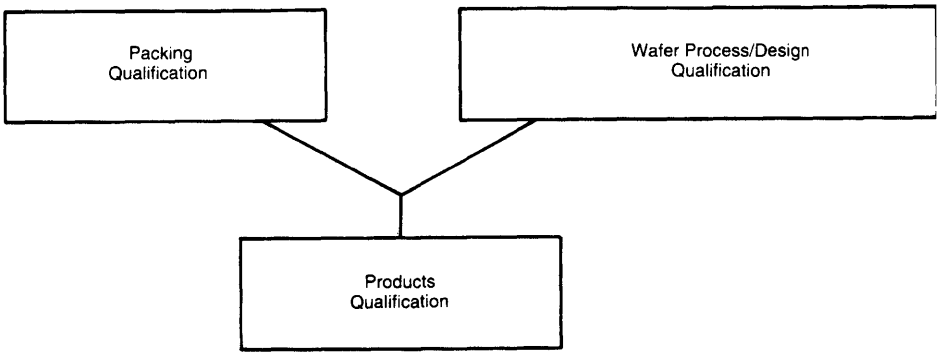


Figure III-1. Qualification Procedure for New Technologies

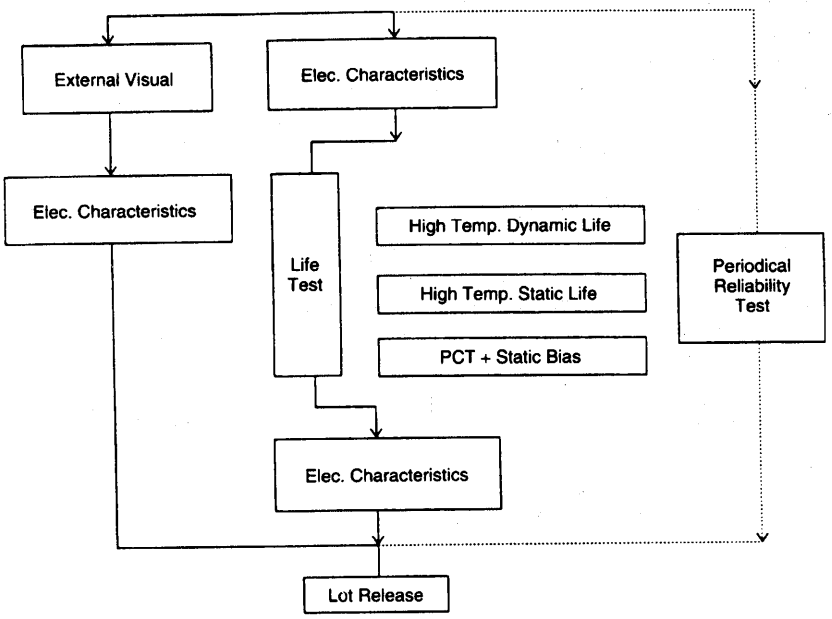


Figure III-2. Quality Assurance System in Mass Production Process

Classification of Inspection		Sampling Plan		
		LTPD (%)	C	
External Visual	Catastrophic Defect	1.2	0	Assembly lot less
	Major Defect	1.2	0	
	Minor Defect	1.2	0	
Electrical Characteristics Inspection		1.2	0	
Life Test	High Temp Dynamic Life	20	0	Wafer lot basis
	High Temp	20	0	
	PCT + Static Bias	20	0	

Table III. MOS IC Product Lot Assurance Inspection Criteria

IV. Reliability test results

RELIABILITY REPORT OF TOSHIBA INTEGRATED CIRCUITS

Type : CMOS Silicon Gate Dynamic RAM

TC5116100J16M DRAM
TC5116100J/Z/FT/TR
TC5116101J/Z/FT/TR
TC5116102J/Z/FT/TR
TC5116400J/Z/FT/TR
TC5116402J/Z/FT/TR
TC5116410J/Z/FT/TR
TC5117400J/Z/FT/TR
TC5117402J/Z/FT/TR
TC5117410J/Z/FT/TR

January 1993

SEMICONDUCTOR QUALITY ASSURANCE DEPARTMENT
RELIABILITY ENGINEERING SECTION II

1. Test Device

Type	Functions	Package	Leads
TC5116100J TC5116101J TC5116102J	16,777,216 Words x 1 bit Dynamic RAM	SOJ 400 mil	28 (24)
TC5116100Z TC5116101Z TC5116102Z		ZIP 475 mil	24
TC5116100FT/TR TC5116101FT/TR TC5116102FT/TR		TSOP 400 mil	28 (24)
TC5116400J TC5116402J TC5116410J	4,194,304 Words x 4 bit Dynamic RAM (4K Refresh)	SOJ 400 mil	28 (24)
TC5116400Z TC5116402Z TC5116410Z		ZIP 475 mil	24
TC5116400FT/TR TC5116402FT/TR TC5116410FT/TR		TSOP 400 mil	28 (24)
TC5117400J TC5117402J TC5117410J	4,194,304 Words x 4 bit Dynamic RAM (2K Refresh)	SOJ 400 mil	28 (24)
TC5117400Z TC5117402Z TC5117410Z		ZIP 475 mil	24
TC5117400FT/TR TC5117402FT/TR TC5117410FT/T		TSOP 400 mil	28 (24)

2. Failure Rate Estimation

Sample Size	Type	Equivalent Component Hours T_a = 60°C, V_{CC} = 5.0V, E_a = 0.3 eV, β = 3	Number of Failures	Failure Rate (Fit)*
700	SOJ	11.6×10^7	3	36

3. Test Results

3.1 Life Tests

Test Item	Condition	Package Type	Sample Size	No. of Failures/Test Time					
High Temperature Operating	T_a=125°C V_{CC}=7.0V	SOJ	500 200	168H	336H	500H	1000H	1500H	2000H
Low Temperature Operating	T_a=30°C V_{CC}=7.0V	SOJ	60	0 0	*1 2 0	0 0	0 0	0 -	*2 1 0
High Temperature Operating	T_a=150°C	SOJ	300	0	0	0	0	-	0
Temperature Humidity Bias	T_a=85°C RH=85° V_{CC}=5.5V	SOJ	300	0	0	0	0	0	0
		ZIP	200	0	-	0	0	-	0
		TSOP (FT)	100	0	-	0	0	-	0
		TSOP (TR)	100	0	-	0	0	-	0

*1: Column failure, Single bit failure
*2: Column failure

3.2 Thermal Environmental Tests

Test Item	Package Type	Sample Size	Test Time	Failures
Soldering Heat	SOJ	22	-	0
	ZIP	22		0
	TSOP	22		0
Temperature * Cycling	SOJ	300	1000 cyc	0
	ZIP	200		0
	TSOP	100		0
Thermal Shock	SOJ	22	30 cyc	0
	ZIP	22		0
	TSOP	22		0
Moisture Resistance	SOJ	22	10 cyc	0
	ZIP	22		0
	TSOP	22		0

* With Pre-Conditioning
SOJ/TSOP (FT):TCT 20 cyc→125°C 20HBake (SOJ)→ 85°C/60% 168H→ I.R.
6HBake (TSOP) (240°C max X 4 times)
TSOP (TR):TCT 20 cyc→ 125°C 6H Bake ' 30°C/60% 30H→ I.R. (240°C max X 4 times)
ZIP:TCT 20 cyc → 85°C/85% 168 H→ Solder dip (260°C 10 sec.)

3.3 Mechanical Tests

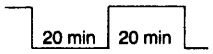
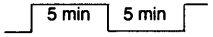
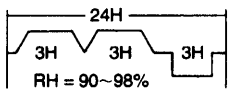
Test Item	Package Type	Sample Size	Failures
Vibration (Variable Frequency)	SOJ	22	0
	ZIP	22	0
	TSOP	22	0
Mechanical Shock	SOJ	22	0
	ZIP	22	0
	TSOP	22	0
Constant Acceleration	SOJ	22	0
	ZIP	22	0
	TSOP	22	0

3.4 The Others

Test Item	Package Type	Sample Size	Test Time	Failures
Solderability	SOJ	22	-	0
	ZIP	22		0
	TSOP	22		0
Salt Atmosphere	SOJ	22	24 hours	0
	ZIP	22		0
	TSOP	100		0
Pressure Cooker*	SOJ	100	300 Hours	0
	ZIP	100		0
	TSOP	100		0

* With Pre-Conditioning
SOJ/TSOP (FT):TCT 20 cyc→125°C 20HBake (SOJ)→ 85°C/60% 168H→ I.R.
6HBake (TSOP) (240°C max X 4 times)
TSOP (TR):TCT 20 cyc→ 125°C 6H Bake ' 30°C/60% 30H→ I.R. (240°C max X 4 times)
ZIP:TCT 20 cyc → 85°C/85% 168 H→ Solder dip (260°C 10 sec.)

4. Test Conditions

Group	Tests	Test Conditions	Referred Standard
Life Tests	High Temperature Operating	T_a = Specified Temperature V_{CC} = Specified Voltage	MIL-STD-883 Method 1005
	High Temperature Storage	T_a = Specified Temperature	MIL-STD-883 Method 1008
	Temperature * Humidity Bias	T_a = 85°C, RH = 85% V_{CC} = 5.5V, VIM = 5.5 V/GND	-
Thermal Environmental Tests	Soldering Heat	260°C, 10 sec. Dipped into meltingsolder to a depth 1.5±0.8 mm from the body	MIL-STD-750 Method 2031
	Temperature * Cycling	150°C -65°C  100 cycles	MIL-STD-883 Method 1010
	Thermal Shock	100°C 0°C  30 cycles	MIL-STD-883 Method 1011
	Moisture Resistance	65°C 25°C -10°C  10 cycles	MIL-STD-883 Method 1004
Mechanical Tests	Vibration (Variable Frequency)	100~2000 Hz, 20 G, 4 min./1 sweep 3 orientations, 4 times each	MIL-STD-883 Method 1008
	Mechanical Shock	1500 G, 0.5 msec, 4 orientations, 3 times each	MIL-STD-883 Method 2007
	Constant Acceleration	20000 G, 6 orientations, 1 min. each	MIL-STD-883 Method 2002
The Others	Solderability	SOJ: 230°C, 5 sec. / 215°C, 10 sec. — at least 95% covered	MIL-STD-883 Method 2001
	Salt Atmoshere	5% salt atmoshere, 35%C, 24 Hours	MIL-STD-883 Method 1009
	Pressure Cooker *	2.5 atm. (T_a = 127°C, RH = 100%)	-

* With Pre-Conditioning
SOJ/TSOP (FT):TCT 20 cyc→125°C 20HBake (SOJ)→ 85°C/60% 168H→ I.R.
6HBake (TSOP) (240°C max X 4 times)
TSOP (TR):TCT 20 cyc→ 125°C 6H Bake ' 30°C/60% 30H→ I.R. (240°C max X 4 times)
ZIP:TCT 20 cyc → 85°C/85% 168 H→ Solder dip (260°C 10 sec.)

References

1) E.S. Anolick and L.Y. Chen "Application of Step Stress to Time Dependent Breakdown" 19th annual Proc. Rel. Phys. p23 (1981).

2) E. Nagasawa: "Electromigration of sputtered Al-Si Alloy Films" Proceedings of annual reliability physics symposium, pp. 64-71, (1978).

3) Francois M. D'Hearle: "Electromigration and Failure Electronics: An Introduction," Proceedings of the IEEE, vol. 59, No. 109 (1971).

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5) M.C. Shine and F.M. d'Heurle: "Activation Energy for Electromigration in Aluminum Films Alloyed Copper," IBM J. Res. Dev., vol. 15, no. 5.

6) Bruce Euzent: "Hot Electron Injection Efficiency in IGFET Structures" 15th annual proc. Rel. Phys., p1 (1977).

7) T.C. May and M.H. Woods: A New Physical Mechanism for Soft Errors in Dynamic Memories 16th annual Proc., Rel., p33 (1978).

Symmetrical vs. Asymmetrical Dynamic RAM Addressing

With the introduction of higher density and wide data path DRAM products, a new method of addressing, called asymmetrical addressing, has also been introduced. For example, Toshiba's 16M- bit DRAM product lineup includes the following:

PRODUCT	ADDRESSING MODE
16Mx1	12 Row/12 Column (Symmetrical)
4Mx4	12 Row/10 Column (Asymmetrical) 11 Row/11 Column (Symmetrical)
2Mx8	11 Row/10 Column (Asymmetrical)
1Mx16 &1Mx18	12 Row/8 Column (Asymmetrical) 10 Row/10 Column (Symmetrical)

As the advantages and disadvantages of symmetrical and asymmetrical addressing are being discovered, the application base and their addressing preference has become segmented. The purpose of this Application Note, is to present the advantages and disadvantages of the different addressing modes and to provide foresight in matching the addressing mode to the application.

COMPATIBILITY

Since DRAM's with symmetrical addressing have the same number of row addresses as column addresses, they are backward compatible with the previous generation. This is critical for applications where the higher density device will be used to replace the lower density device without a re-design of the DRAM controller. For example, the 4Mx4 DRAM with 11 row and 11 column addresses has the same addressing as the 4Mx1 DRAM.

Another important application for symmetrical addressing is in modules. One of the industry's most popular module configurations is the 1Mx36. Current implementations of the 1Mx36 module use eight pieces of 1Mx4 and four pieces of 1Mx1 DRAM. We can now replace this module with a fully compatible version using only 2 pieces of the 1Mx18 DRAM with 10 row and 10 column addresses. Besides the performance advantages, such as a lower module height profile, and less power consumption and loading, the use of the higher density DRAM product also provides lower cost (after price- per-bit crossover) and a solution with a longer life.

DRAM's with asymmetrical addressing cannot be used as "drop-in" replacements for the previous generation products, without a redesign of the DRAM controller, due to the incompatibility of addresses.

REFRESH

The number of row addresses affects the refresh rate since all rows of the DRAM must be refreshed within a specified refresh period. For example, one of the devices previously listed is the 4Mx4 DRAM with 12 row addresses and 10 column addresses. Since this device has 12 row addresses, it has 4096 rows of memory cells. The industry has also adopted the terminology "4K refresh" to describe the asymmetrical address 4Mx4 device.

The table below shows how the addressing method affects the refresh rate, using the 1Mx16 DRAM as an example, and offers some interesting insight for low-power applications .

	STANDARD REFRESH		EXTENDED REFRESH	
DRAM TYPE	BURST	DISTRIBUTED	BURST	DISTRIBUTED
IMx16 Asym 12 Row/8 Col	4K cycles per 64ms	1 cycle per 15.6us	4K cycles per 128ms	1 cycle per 31us
IMx16 Asym 10 Row/10 Col	1K cycles per 16ms	1 cycle per 15.6us	1K cycles per 128ms	1 cycle per 125us

Note: Extended Refresh calculations assume tREF = 128ms max.

As shown above under the columns labeled "Standard Refresh", the addressing method has no effect on the refresh rate when using distributed refresh. The row refresh rate is 15.6 us. However, there are many applications which require low standby power consumption utilizing the extended refresh capability of the DRAM. The longer the refresh period is extended, the lower the standby power.

As shown above, there is an advantage for the symmetrical device in applications which use extended distributed refresh. The symmetrical device's distributed rate can be extended by a factor of eight vs. only two for the asymmetrical device.

One may wonder why the 1Mx16 asymmetrical device's burst refresh rate is not extended to 4K cycles every 512 ms, which would provide a distributed refresh rate of 125 us. The issue is that at 512 ms, some of the DRAM cells may lose their data. Although the exact point at which a DRAM cell can no longer retain data depends on the DRAM manufacturer's design and process technology, most would probably agree that a refresh period (tREF) of 512 ms is very difficult for all of the cells in the DRAM array to achieve. It is possible to screen the DRAM for longer data retention periods, however the yields may be very low and resulting price premiums unattractive.

The data retention problem will become even more of an issue for higher density DRAM products and the advantage of using symmetrical addressing in extended refresh applications will become even more apparent.

POWER CONSUMPTION

The asymmetrical devices were designed to provide a lower power solution. With more rows than columns, there is less internal circuitry (sense amplifiers, etc.) per row, hence less power consumed when a row is accessed.

DRAM specifications for average power supply operating current and refresh current clearly show an advantage for the asymmetrical device. An example, using Toshiba's 4Mx4 DRAM (a 70 ns device operated at minimum cycle time), is shown in the following table.

SPECIFICATION	4Mx4 Asym.	4Mx4 Sym.
Operating Current	80mA max.	110mA max.
RAS-only Refresh Current	80mA max.	110mA max.
CAS-before-RAS Refresh Current	80mA max.	110mA max.

While these specifications demonstrate a clear advantage for the asymmetrical devices, one must consider the application to determine the true power consumption. As mentioned in the previous section, standby current is lower for the symetrical device, therefore the percentage of the time the application's DRAM is active vs. inactive (duty-cycle) must be considered to determine overall power consumption.

During any DRAM access, the peak power consumption occurs when a row is activated (RAS goes active), and the average power consumption is inversely proportional to cycle time. This means that applications which perform mostly random accesses at minimum cycle time will derive the most benefit from using asymmetrical addressing. As the cycle time increases, the power saving benefit of asymmetrical addressing decreases.

This last point is especially important for applications which utilize the DRAM's fast page mode capability. The longer the application stays in page mode, the smaller the difference in power consumption between asymmetrical and symmetrical devices. This is because of the long cycle time associated with fast page mode. Toshiba's 4Mx4 DRAM average power supply current specifications for fast page mode verify this, as this specification is the same regardless of the addressing mode of the device.

Some other DRAM devices may show a power consumption advantage for the asymmetrical device in fast page mode. This is most likely due to the definition of fast page mode and not a reflection of a long cycle time. Most DRAM manufacturers define fast page mode as two or more consecutive column addresses in the same page. Obviously, a page length of two does not require a long cycle.

PAGE LENGTH

Applications which utilize fast page mode such that data is read from the entire page (or attempt to stay in the same page as long as possible) will benefit most from the symmetrical device since it has more column addresses and hence a longer page length.

ACCESS TIME

There appears to be an advantage emerging for wider (x16/x18) asymmetrical devices. Faster access and cycle times imply higher operating current. In addition, the operating current is even higher for devices with symmetrical addressing since more internal circuitry is activated during a random access (when RAS goes low). The reliability effects of this large amount of current are now under study for symmetrical addressing. The high operating current is only an issue for wider (x16/x18) devices because of the larger disparity between asymmetrical and symmetrical addressing (12 row addresses vs. 10 row addresses). At this time, Toshiba is offering 60 ns for our 1Mx16 and 1Mx18 DRAM's with asymmetrical addressing, but only 70 ns for symmetrical addressing, with 60 ns under study.

SUMMARY/CONCLUSION

A summary of the advantages and probable applications for both addressing modes is shown in the table below. New applications which will not realize any major advantage by using either of the two addressing modes would benefit most from a DRAM controller design which supports both addressing modes. This allows maximum product sourcing flexibility and upward compatibility with higher density products.

Symmetrical	Asymmetrical
1. Backward compatible with older generations 2. Replacement of older generation module solutions. 3. Longer extended distributed refresh period in low power/battery operated applications 4. Longer page length, with no difference in power consumption vs. asymmetrical device for long page mode cycles.	1. Lower power consumption for random access or fast cycle time applications. 2. Possibility of faster access times for wide I/O devices.

DRAM Comparison: 5V 1Mx4 vs. 3.3V 1Mx16

Due to the ever-increasing demand for portable computer products with long battery life, DRAM manufacturers have been pushed to supply 3.3V DRAMs. Currently, the supply for 3.3V DRAMs has not been able to keep pace with the demand.

Fortunately, one can replace an existing product designed for 3.3V 4M DRAMs with a new one designed for 5V 16M DRAMs, and realize lower power along with several other advantages. An example is shown below for a system with 4M bytes of DRAM.

COMPARISON	3.3V 1Mx4 80ns	5V 1Mx16 80ns
Number of DRAMs for 4MB	8	2
Board area - SOJ package	1.9 (normalized)	1 (normalized)
Board area - TSOP package	2.6 (normalized)	1 (normalized)
Operating/Refresh Power	1.73W max.	1.32W max.
Fast Page Mode Power	1.15W max.	0.72W max
Standby Power (TTL)	28.8mW max.	22.0mW max.
Standby Power (CMOS)	7.2mW max.	11mW max.
Input Capacitance (Addr)	40pF max.	10pF max.
Input Capacitance (Other)	56pF max.	14pF max.

Note 1: The 1Mx16 DRAM with symmetrical addressing (10 row/10 column) was used for this comparison since it is fully compatible with the 1Mx4 DRAM in terms of addressing and refresh.

Note 2: The above power consumption comparison is based on maximum DC voltage and current specifications.

As this example clearly shows, the 1Mx16 offers not only lower power consumption, but also consumes less board area and load capacitance. Similar comparsons could be made for other 16M DRAM products replacing 4M DRAMs and the results would be the same .

Module Conversion from 4M DRAM Based to 16M DRAM Based

Toshiba offers several module configurations which have compatible 4M DRAM based and 16M DRAM based versions. These are listed below.

CONFIGURATION	4M DRAM BASED	16M DRAM BASED
1Mx32	THM321000A	THM3210B0A
2Mx32	THM322020A	THM3220C0A
1Mx36	THM361020A	THM3610B0A
2Mx36	THM362020A	THM3620C0A
4Mx36	THM364080A	THM364020

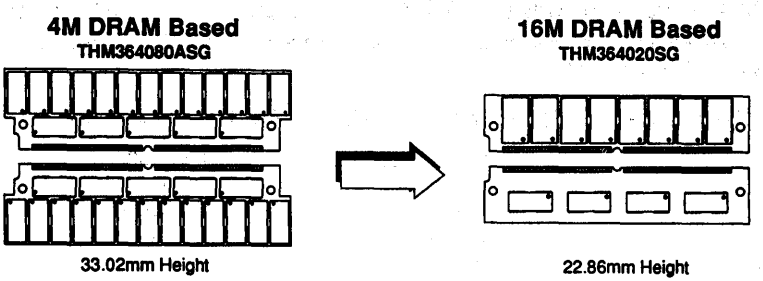
The advantages of using 16M DRAM based modules to replace 4M DRAM based modules include technical advantages such as reduced height profile, power consumption, and input capacitance. An example is shown on the next page. At 4M/16M DRAM price per-bit crossover, 16M DRAM based module also provides a lower cost solution. There are some additional advantages which may not be as obvious.

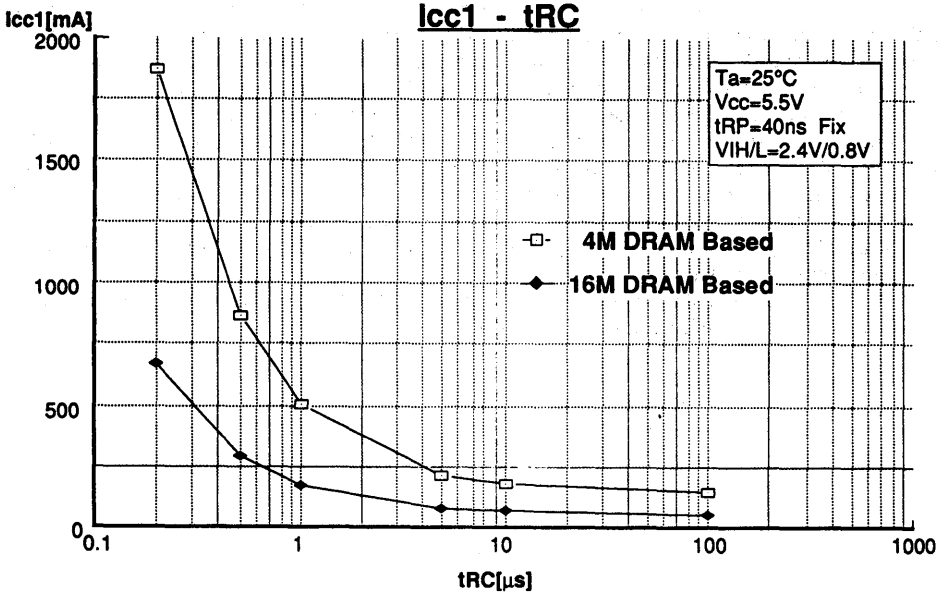
16M DRAM based modules can provide a feasible solution for extending the life of the module. For example, one the most popular module configurations is the 1Mx36. A 4M DRAM based 1Mx36 is assembled with eight 1Mx4 DRAMs and four 1Mx1 DRAMs. In comparison, the 16M DRAM based 1Mx36 uses only two 1Mx18 DRAMs. Long after the 1Mx1 DRAM has been phased out of production (and hence the 4M DRAM based 1Mx36), the 16M DRAM based 1Mx36 module can still be produced.

Reduced component count by converting from 4M to 16M DRAM based modules also means a reduction in soft error rates on a per bit basis.

For specific details on the technical advantages of using 16M DRAM based modules, please refer to the specific data sheet for the module configuration of interest.

x36 MODULE COMPARISON





CAPACITANCE (V_{CC} = 5V ± 10%, f=1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	4M DRAM Based	16M DRAM Based
CI	Input Capacitance (A0 ~ A10)	190	88
CI2	Input Capacitance ($\overline{W}$)	190	84
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	100	42
CI4	Input Capacitance ($\overline{CAS0}$, $\overline{CAS2}$)	60	36
CDQ1	I/O Capacitance (DQ0 ~ 7,9 ~ 16, 18 ~ 25, 27 ~ 34)	35	17
CDQ2	I/O Capacitance (DQ8, 17, 26, 35)	35	22

DRAM Module Applications

The industry's most popular DRAM modules consist of various configurations of the 72-pin family. The different module configurations of the 72-pin family are optimized for specific applications. The information shown below summarizes the various 72-pin module configurations offered by Toshiba, their typical applications, and some characteristics which distinguish the different configurations.

CONFIGURATION	TYPICAL APPLICATIONS
x32	Low to medium range PCs, Printers
x36 (Parity)	Medium to high range PCs, Workstations, Servers
x36 (ECC)	High range PCs, Workstations, Servers
x40	Workstations, Servers

The x32 modules are optimized for non-parity applications with 16 or 32-bit data bus widths. A single bank x32, such as the 1Mx32 or 4Mx32, has single RAS and CAS controls. A double bank x32, such the 2Mx32 or 8Mx32, has double RAS and CAS controls. In either case, a 32-bit word is read or written in each cycle.

The x36 parity modules are optimized for parity applications. In parity applications, a 9-bit word is read or written in each cycle. In the case of single bank x36 parity modules, such as the 1Mx36 or 4Mx36, there are four CAS controls, one for each 9- bit word. Additionally, there are two RAS controls to reduce active power consumption and simplify 16-bit data bus width designs. Double bank x36 parity modules, such the 2Mx36 or 8Mx36, have the same number of CAS controls and twice as many RAS controls to act as bank enables.

The x36 ECC modules are optimized for 8-byte ECC applications with 64 bits of data and eight ECC bits. In this case, a single 36-bit word is read or written in each cycle, and two modules are used to realize the full 72-bit word.

The x40 modules are optimized for 4-byte ECC applications with 32 bits of data and seven ECC bits. These applications actually need a x39 module, but the use of x4 DRAMs makes x40 easier. Additionally, the extra bit has been useful in some custom ECC applications.

Hopefully this information combined with the data sheets will allow the proper module selection. For additional information, please contact your local Toshiba Sales Office.

TAEC Regional Sales Offices

NORTHWEST
Sunnyvale, CA
TEL: (408) 737-9844
FAX: (408) 737-9905

SOUTHWEST
Irvine, CA
TEL: (714) 453-0224
FAX: (714) 453-0125

Denver, CO
TEL: (303) 220-9848
FAX: (303) 220-9856

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TEL: (708) 945-1500
FAX: (708) 945-1044

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FAX: (214) 235-4114

NORTHEAST
Boston, MA
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FAX: (617) 224-1096

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FAX: (908) 248-8030

SOUTHEAST
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TEL: (404) 368-0203
FAX: (404) 368-0075

Orlando, FL
TEL: (407) 332-0966
FAX: (407) 339-3777

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