RCA-3N128 (formerly Dev. No.TA2840) is an N-channel, depletion-type silicon insulated-gate field-effect (MOS*) transistor for VHF amplifiers and oscillators in commercial and industrial applications. The 3N128 is also extremely well suited for use in low-frequency amplifier applications requiring a transistor having high power gain and very high input impedance.

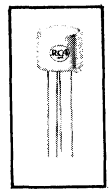
Because of its improved transfer characteristic the 3N128 provides substantially better cross-modulation performance in linear-amplifier applications than do conventional (bipolar) transistors.

The insulated gate of the 3N128 is offset towards the source – a feature which provides extremely low feedback capacitance (0.13 pF typ.). The 3N128 is hermetically sealed in a 4-lead metal package.

Application data for RCA-3N128, including biasing requirements, basic circuit configurations, selection of optimum operating point, and methods of automatic gain control are given in RCA Application Note AN-3193, "Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor".

*Metal-Oxide-Semiconductor.

SILICON MOS TRANSISTOR– N-Channel Depletion Type



For Amplifier and Oscillator Applications in Commercial and Industrial VHF Communications Equipment Operating up to 250 MHz

Maximum Ratings, *Absolute-Maximum Values:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 max.	V
GATE-TO-SOURCE VOLTAGE, V_{GS}:		
CONTINUOUS	0, -8 max.	V
INSTANTANEOUS	±15 max.	V
DRAIN CURRENT, I_D	Limited by power dissipation	
TRANSISTOR DISSIPATION, P_T:		
At Ambient Temperatures up to 100°C	100 max.	mW
AMBIENT-TEMPERATURE RANGE:		
Storage	-65 to +125	°C
Operating	-65 to +100	°C
LEAD TEMPERATURE (During Soldering):		
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265 max.	°C

Features:

- **High input resistance –** $r_{GS} = 10^{14}\ \Omega$ typ.
- **Low gate leakage current –** $I_{GSS} = 0.1$ pA typ.
- **Low feedback capacitance –** $C_{rss} = 0.13$ pF typ.
- **High forward transconductance –** $g_{fs} = 7300\ \mu$mho typ.
- **High vhf power gain –** $G_{PS} = 18$ dB typ. at 200 MHz
- **Low vhf noise figure –** NF = 4 dB typ. at 200 MHz
- **Exceptionally good cross-modulation characteristics**

RADIO CORPORATION OF AMERICA
ELECTRONIC COMPONENTS AND DEVICES, HARRISON, N.J.

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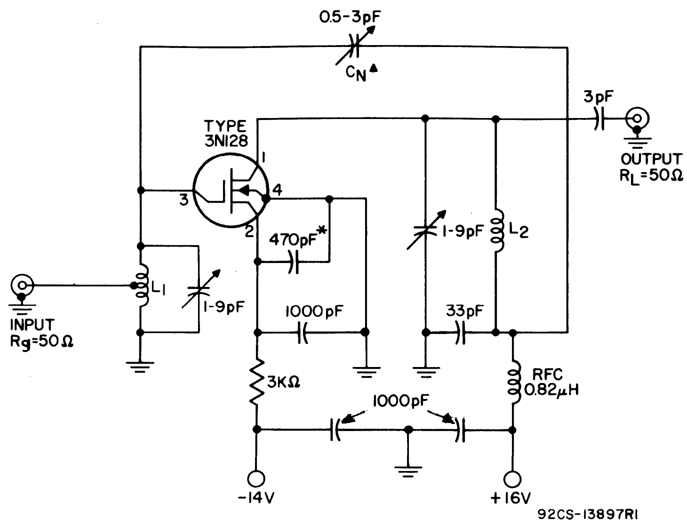
Printed in U.S.A.
3N128 8-66



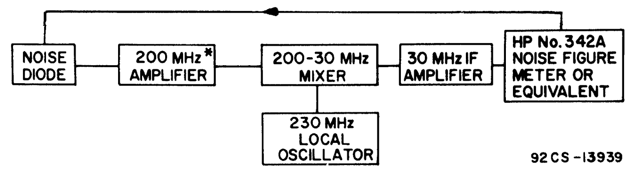
L_1 = 4-1/2 turns #20 AWG wire, 3/16" dia., approx. 1/2" long, tapped 1 turn from ground end.

L_2 = 3-1/2 turns #20 AWG wire, 3/8" dia., approx. 1/2" long.

* Leadless-type disc capacitor.

▲ Neutralization fixed for a Transistor having a Typical value of C_{rss} (0.13 pF)

Fig.1 - Test Circuit used to Measure 200-MHz Power Gain and Noise Figure.



* See Fig.1 for Circuit.

Fig.2 - Noise-Figure Measurement Setup.

ELECTRICAL CHARACTERISTICS: *(At T_A = 25°C)*

Measured with Substrate Connected to Source Unless Otherwise Specified.

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS Min.	Typ.	Max.	UNITS
Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz	-	10,000	-	μmho
		V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7300	12,000	μmho
Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8 V	-	0.1	50	pA
Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	5.8	-	pF
Small-Signal Short-Circuit Reverse Transfer Capacitance*	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	0.13	0.2	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	1.4	-	pF
Gate Leakage Resistance	r_{GS}	V_{DS} = 0, V_{GS} = -8 V	-	10^{14}	-	Ω
Drain-to-Source Channel Resistance	r_{ds}	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	-	200	-	Ω
Pinch-Off Voltage	V_P	I_D = 50 μA, V_{DS} = 15 V	-	-3.5	-8	V
Zero-Bias Drain Current**	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	5	15	30	mA
Power Gain (see Fig.1)	G_{PS}	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	14.5	18	-	dB
Noise Figure (see Figs.1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	4	5	dB

*Three-Terminal Measurement: Source Returned to Guard Terminal.

**Pulse Test: Pulse Duration 20 ms max.; Duty Factor ≤ 0.15.

TYPICAL 200-MHz COMMON-SOURCE ADMITTANCE (Y) COMPONENTS vs DRAIN CURRENT

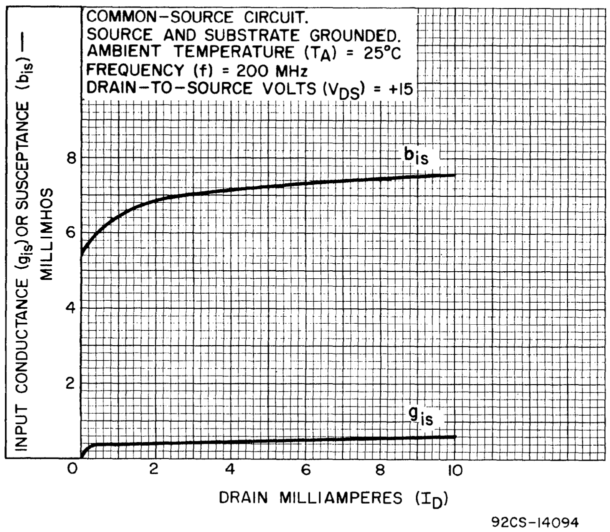


Fig.6 - Input Admittance (Y_{is}) Components.

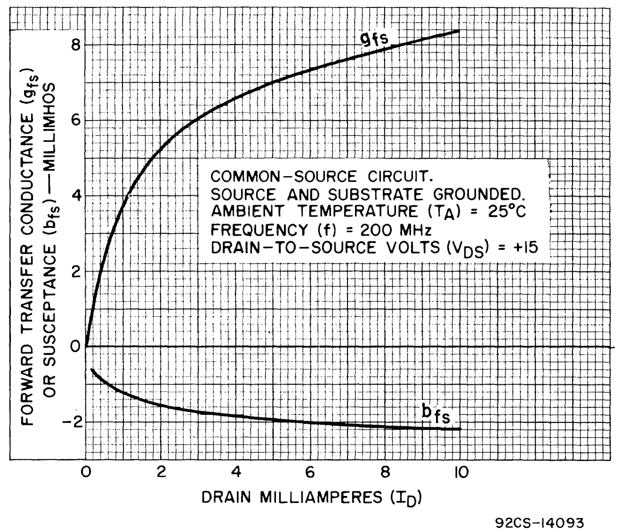


Fig.7 - Forward Transadmittance (Y_{fs}) Components.

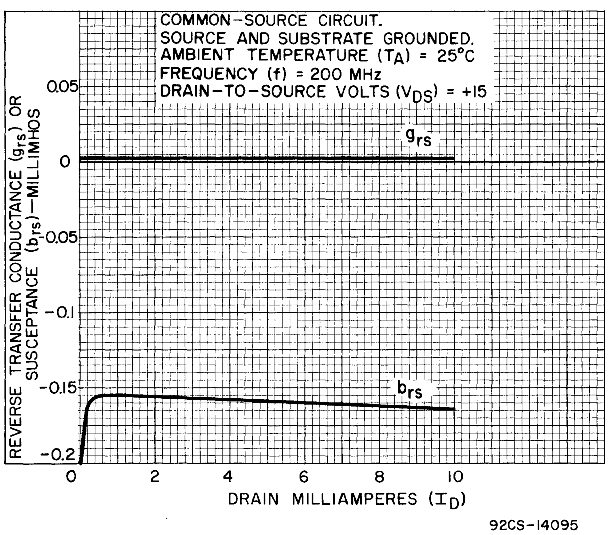


Fig.8 - Reverse Transadmittance (Y_{rs}) Components.

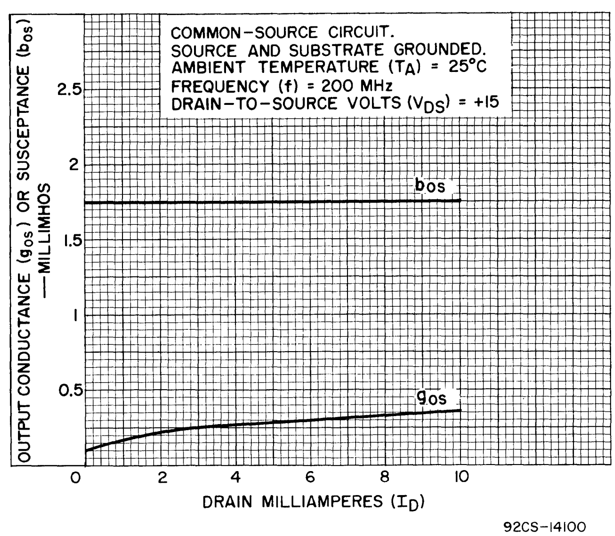


Fig.9 - Output Admittance (Y_{os}) Components.

TYPICAL COMMON-SOURCE ADMITTANCE (Y) COMPONENTS vs FREQUENCY

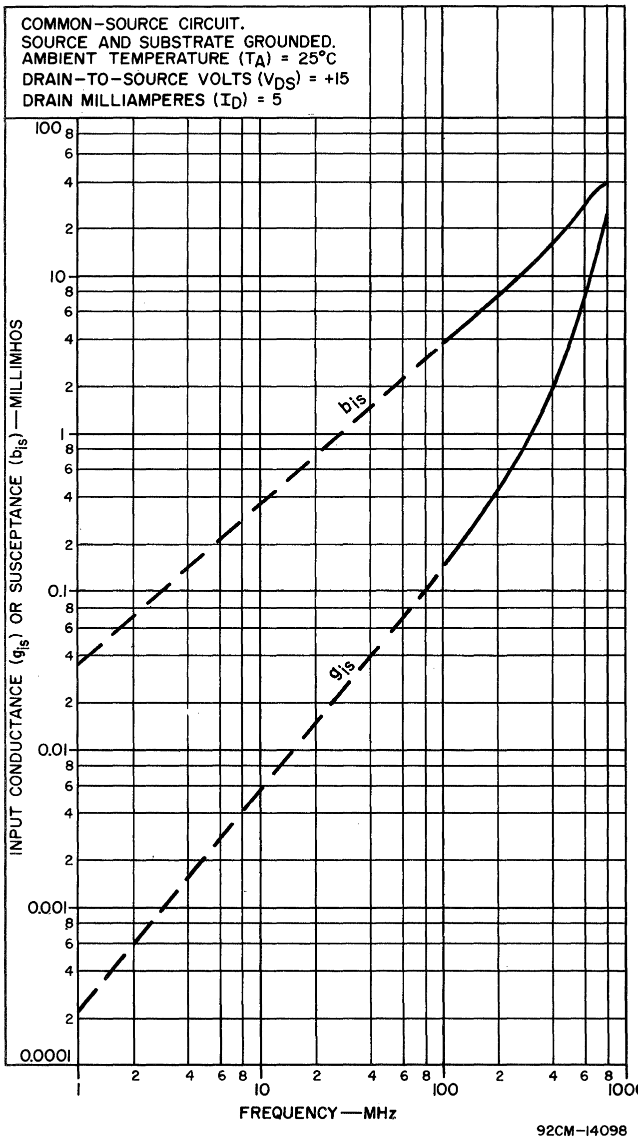


Fig.10 - Input Admittance (Y_{is}) Components.

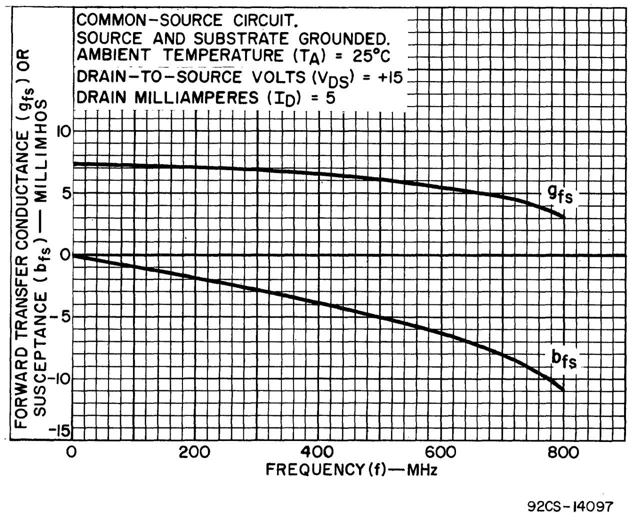


Fig.11 - Forward Transadmittance (Y_{fs}) Components.

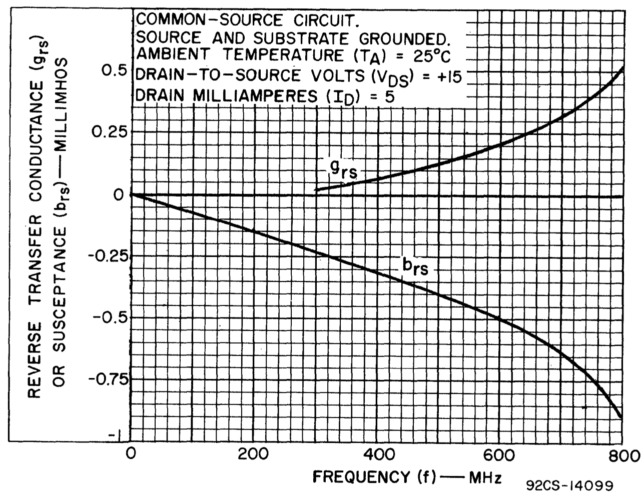


Fig.12 - Reverse Transadmittance (Y_{rs}) Components.

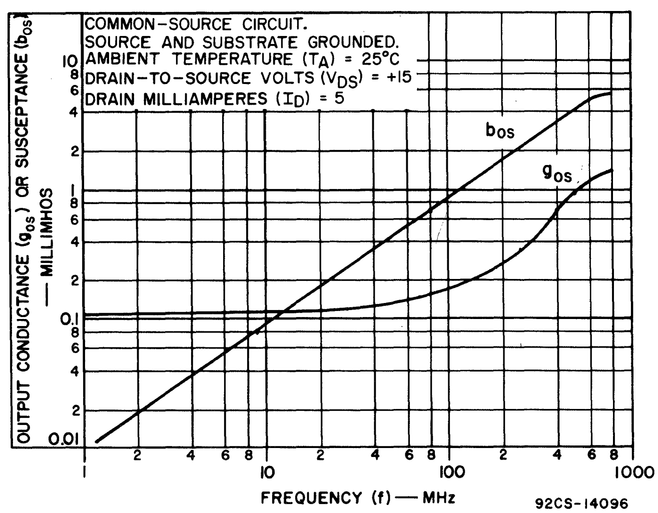


Fig.13 - Output Admittance (Y_{os}) Components.

HANDLING AND OPERATING CONSIDERATIONS

CAUTION

RCA-3N128, like conventional (bipolar) high-frequency silicon transistors, is susceptible to the detrimental effects of high-potential electrostatic discharges applied to its input terminals.

The polystyrene insulating snow, commonly used as a convenient carrying tray for semiconductor devices, can acquire high static charges and should not be used unless it has been specially treated to make it electrically conductive ($R \geq 10\ k\Omega/in^3$).

To avoid the possibility of subjecting these devices to high ac voltages that may be present on the tips of soldering irons, some means for grounding these tips should be provided.

RCA 3N128 should never be inserted in or removed from circuits with the power on because transient voltages may permanently damage the device. AC-operated power supplies for the 3N128 should also have provision for suppression of transients during turn-on and turn-off. If such suppression is not provided, the following procedure should be used in applying power to the 3N128.

1 - Before inserting the 3N128 in the equipment turn ac line switch on and reduce the dc output of the power supply to zero.

2 - Insert the 3N128.

3 - Increase the dc supply voltage to the desired value.

This procedure should be reversed when the 3N128 is taken out of the equipment.

TYPICAL CHARACTERISTICS

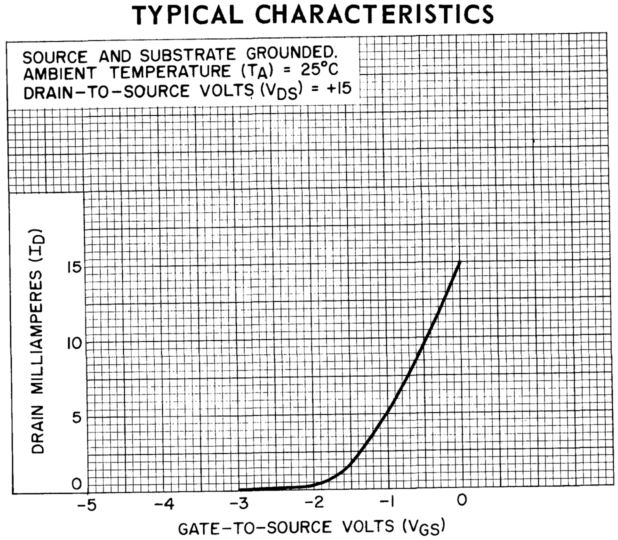


Fig.3 - Drain Current vs Gate-to-Source Voltage.

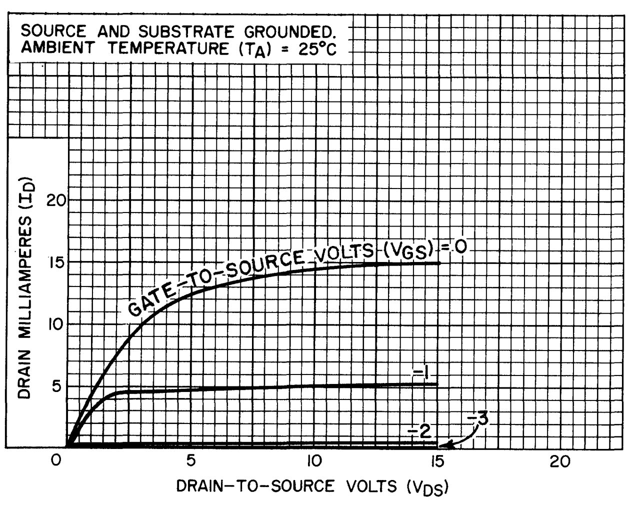


Fig.4 - Drain Current vs Drain-to-Source Voltage.

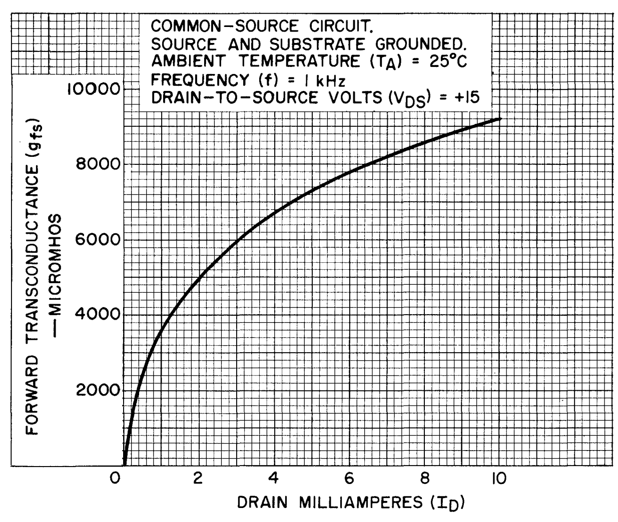
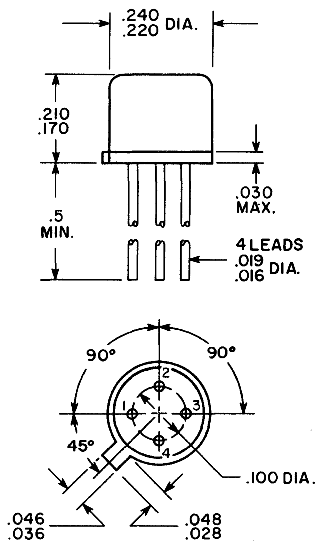


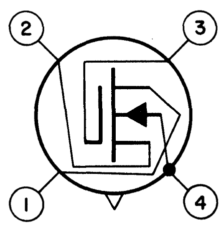
Fig.5 - 1-kHz Forward Transconductance vs Drain Current.

DIMENSIONAL OUTLINE



Dimensions in Inches

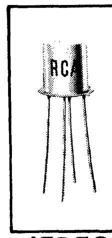
TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

SILICON INSULATED-GATE FIELD-EFFECT TRANSISTOR N-Channel Depletion Type

For Critical Chopper Applications and Multiplex Service up to 60 MHz: in Military Communications, Navigation, and Instrumentation Equipment in Industrial Instrumentation and Control Circuits



JEDEC TO-72

RCA-3N138‡ is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is intended primarily for critical chopper and multiplex applications up to 60MHz.

This transistor features a New Terminal Arrangement in which the gate and source connections are interchanged to provide maximum isolation between the output (drain) and the input (gate) terminals. Although this new basing configuration does not appreciably change the measured device feedback capacitance, it permits the use of external interterminal shields to reduce the feedback due to external capacitances, particularly on printed circuit boards. This feature makes it possible to minimize feedthrough capacitance.

The insulated gate provides a very high value of input resistance (10^{14} ohms typ.) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N138 also features extremely low feedthrough capacitance (0.18pF typ.) and zero inherent offset voltage.

The 3N138 is hermetically sealed in the JEDEC TO-72 package and features a gate metallization that covers the entire source-to-drain channel.

‡ Formerly Dev. No. TA7032.
* Metal-Oxide-Semiconductor.

Maximum Ratings, Absolute-Maximum Values:

(Substrate connected to source unless otherwise specified)

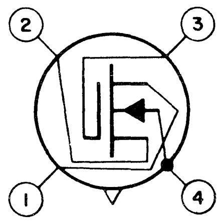
DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+35 max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+35, −0.3 max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+35, −0.3 max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	±10 max.	V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max.	V
PEAK VOLTAGE, GATE-TO-ALL OTHER TERMINALS: V_{GS}, V_{GD}, V_{GB}, non-repetitive	±45 max.	V
DRAIN CURRENT, I_D (Pulse duration 20 ms, duty factor $\leq$ 0.10)	50 max.	mA
TRANSISTOR DISSIPATION, P_T: At ambient temperatures from −65 to +125°C	150 max.	mW
AMBIENT TEMPERATURE RANGE:		
Storage	−65 to +150	°C
Operating	−65 to +125	°C
LEAD TEMPERATURE (During Soldering): At distances ≥ 1/32″ to seating surface for 10 seconds max.	265 max.	°C

Applications

- Servo Amplifiers
- Telemetry Amplifiers
- Computer Operational Amplifiers
- Sampling Circuits
- Electrometer Amplifiers

Features

- new terminal arrangement



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

- excellent thermal stability
- zero inherent offset voltage
- low leakage current: 10 pA max.
- low "on" resistance — $r_{DS}(on) = 240\Omega$ typ. ($V_{GS} = 0V$)
- high "off" resistance — $R_{DS}(off) = 10^{10}\Omega$ typ.
- low feedback capacitance — $C_{rss} = 0.18pF$ typ.
- low input capacitance — $C_{iss} = 3pF$ typ.
- symmetrical configuration — permits interchangeability of drain and source

Printed in U.S.A.
3N138 8-67

ELECTRICAL CHARACTERISTICS, at $T_A = 25°$ C, Unless Otherwise Specified. Substrate Connected to Source.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Type 3N138			UNITS
			Min.	Typ.	Max.	
Gate-Leakage Current	I_{GSS}	$V_{GS} = \pm 10$, $V_{DS} = 0$, $T_A = 25°C$ $V_{GS} = \pm 10$, $V_{DS} = 0$, $T_A = 125°C$	— —	0.1 20	10 200	pA pA
Drain-to-Source "ON" Resistance	$r_{DS}(on)$	$V_{GS} = 0$, $V_{DS} = 0$, f = 1 KHz, $T_A = 25°C$ $V_{GS} = +10$, $V_{DS} = 0$, f = 1 KHz, $T_A = 25°C$ $V_{GS} = 0$, $V_{DS} = 0$, f = 1 KHz, $T_A = 125°C$	— — —	240 135 350	300 — —	Ω Ω Ω
Drain-to-Source "OFF" Resistance	$R_{DS}(off)$	$V_{GS} = -10$, $V_{DS} = +1$	2×10^8	10^{10}	—	Ω
Drain-to-Source Cutoff Current	$I_D(off)$	$V_{GS} = -10$, $V_{DS} = +1$, $T_A = 25°C$ $V_{GS} = -10$, $V_{DS} = +1$, $T_A = 125°C$	— —	0.01 0.01	0.5 0.5	nA μA
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	$V_{GS} = -10$, $V_{DS} = 0$, f = 1 MHz	—	0.18	0.25	pF
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	$V_{GS} = -10$, $V_{DS} = 0$, f = 1 MHz	—	3	5	pF
Zero-Gate-Bias Forward Transconductance	g_{fs}	$V_{GS} = 0$, $V_{DS} = 12$	—	6000	—	μmho
Offset Voltage	V_O	$V_{GS} = \pm 10$, $V_{DS} = 0$	—	0*	—	V

* In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No. 107-1.0.1, or equivalent.

OPERATING CONSIDERATIONS

The flexible leads of the 3N138 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields.

This device should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the device.

TYPICAL CHARACTERISTICS

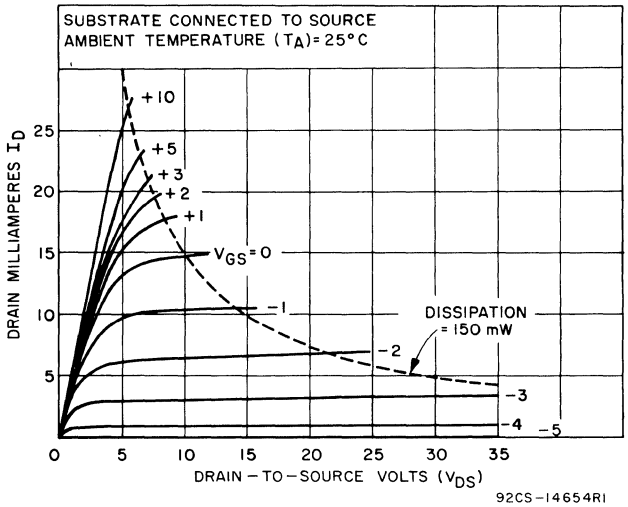


Fig. 1 – Drain Current vs Drain-to-Source Voltage

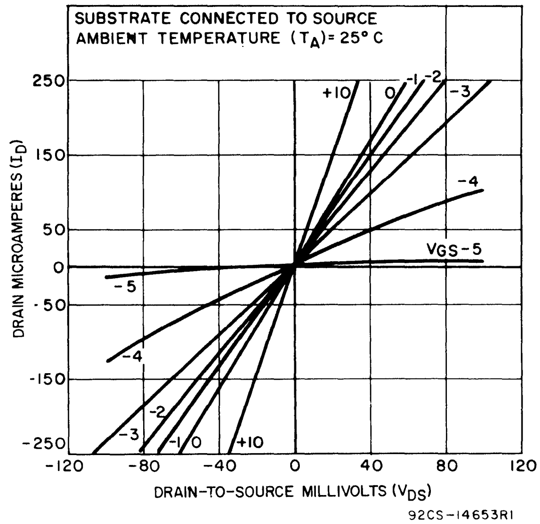


Fig. 2 – Low-Level Drain Current vs Drain-to-Source Voltage

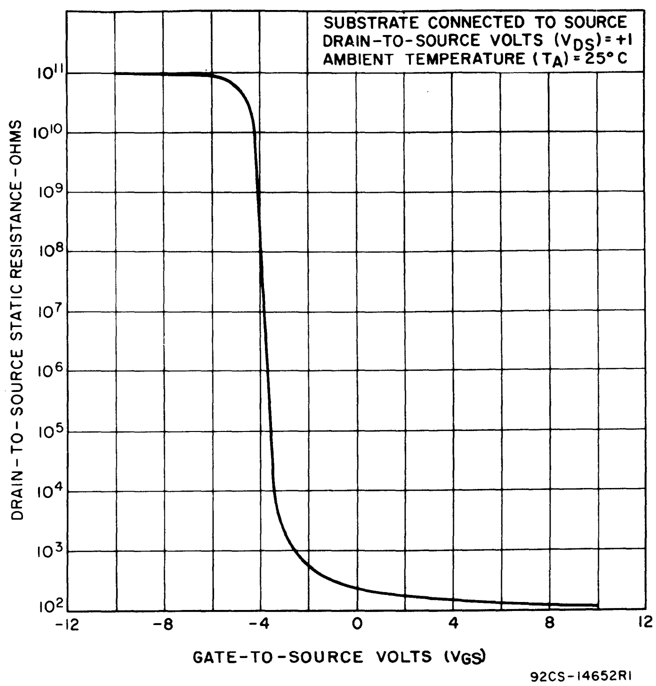
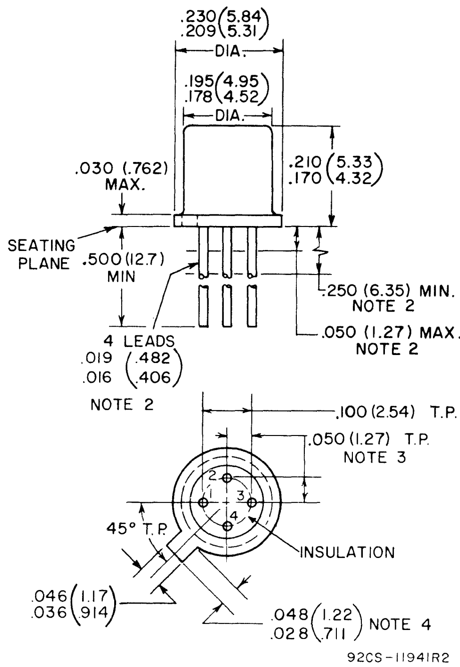


Fig. 3 – Drain-to-Source Static Resistance vs Gate-to-Source Voltage

DIMENSIONAL OUTLINE
JEDEC TO-72



Dimensions in inches and millimeters

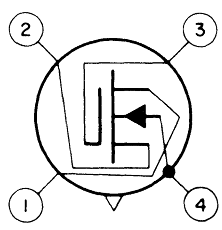
Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Note 2: The specified lead diameter applies in the zone between 0.050" (1.27 mm) and 0.250" (6.35 mm) from the seating plane. From 0 250" (6.35 mm) to the end of the lead a maximum diameter of 0.021" (0.533 mm) is held. Outside of these zones, the lead diameter is not controlled.

Note 3: Leads having a maximum diameter of 0.019" (0.482 mm) at a gauging plane of 0.054" (1.372 mm) + 0.001" (0.025 mm) - 0.000" (0.000 mm) below seating plane shall be within 0.007" (0.177 mm) of their true position (location) relative to a maximum width of tab.

Note 4: Measured from actual maximum diameter.

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

RCA MOS FIELD-EFFECT TRANSISTOR

For Audio, Video, and RF Amplifier Applications

3N139

File No. 284

RCA 3N139+ is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is a general purpose transistor especially suited for audio, video, and rf applications, and for wide-band amplifier designs. The insulated gate provides a very high input resistance (10^{14} Ω typ.) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N139 also has a high transconductance, a low value of input capacitance (3 pF typ.), and a very low feedback capacitance (0.19 pF typ.).

This transistor features a New Terminal Arrangement in which the gate and source connections are interchanged to provide maximum isolation between the output (drain) and the input (gate) terminals. Although this new basing configuration does not appreciably change the measured device feedback capacitance, it permits the use of external inter-terminal shields to reduce the feedback due to external capacitances, particularly on printed circuit boards. This feature makes it possible to achieve greater circuit stability or higher useable gain per stage.

The 3N139 is hermetically sealed in the standard 4-lead JEDEC TO-72 package.

+Formerly Dev. No.TA7244

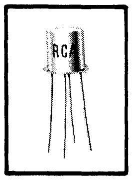
* Metal-Oxide-Semiconductor

Maximum Ratings, *Absolute-Maximum Values:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS} . . .	+35 max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+35, -0.3 max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+35, -0.3 max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS} ·	±10 max.	V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max.	V
PEAK VOLTAGE, GATE-TO-ALL OTHER TERMINALS; V_{GS}, V_{GD}, V_{GB}, non-repetitive	±42 max.	V
DRAIN CURRENT, I_D (Pulse duration 20 ms, duty factor ≤ 0.10).	50 max.	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures from -65 to +125°C.	150 max.	mW
AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +150	°C
Operating	-65 to +125	°C
LEAD TEMPERATURE (During Soldering):		
At distance not closer than 1/32 inch to seating surface for 10 seconds max. . .	265 max.	°C

SILICON MOS TRANSISTOR

For Audio, Video, and RF Amplifier Applications



JEDEC TO-72

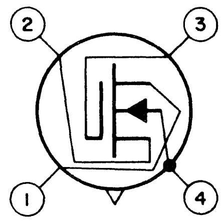
in Military Communications, Instrumentation, & Navigation Equipment

in Mobile and Fixed Communication Equipment

in Industrial Instrumentation and Control Circuits

FEATURES

- new terminal arrangement



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

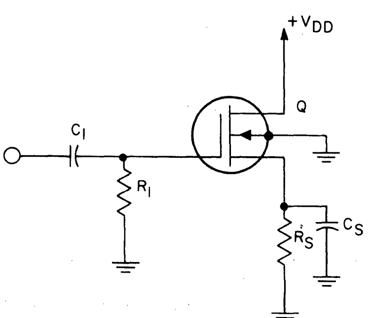
- high input resistance $R_{GS} = 10^{14}$ Ω typ.
- high forward transconductance g_{fs} (V_{DS} = 15 V, R_S = 0, f = 1 kHz) = 6000 μmho typ.
- low input capacitance C_{iss} = 3 pF typ.
- high power gain G_{ps} = 17 dB typ. at 200 MHz
- low noise figure NF = 4 dB typ. at 200 MHz
- low gate leakage current I_{GSS} = 0.1 nA typ.
- high drain-to-source voltage: +35 max. V

ELECTRICAL CHARACTERISTICS: *At T_A = 25°C, Unless Otherwise Indicated. Substrate Connected to Ground.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Gate Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V_{GS} = ±10 V, V_{DS} = 0, T_A = 125°C	- -	0.1 -	1 4	nA nA
Forward Transconductance *(See Fig.1)*	g_{fs}	V_{DS} = 15 V, R_S = 0, f = 1 kHz V_{DD} = 15 V, R_S = 360 Ω, f = 1 kHz V_{DD} = 15 V, R_S = 360 Ω, f = 1 kHz, T_A = 125°C	3000 3000 -	6000 4500 3300	- 7500 -	μmho μmho μmho
Zero-Bias Drain Current*	I_{DSS}	V_{DS} = 15 V, R_S = 0	5	15	25	mA
Drain Current *(See Fig.1)*	I_D	V_{DD} = 15 V, R_S = 360 Ω V_{DD} = 15 V, R_S = 360 Ω, T_A = 125°C	3 -	4.5 3.3	7 -	mA mA
Output Resistance *(See Fig.1)*	r_d	V_{DS} = 15 V, R_S = 0, f = 1 kHz V_{DD} = 15 V, R_S = 360 Ω, f = 1 kHz V_{DD} = 15 V, R_S = 360 Ω, f = 1 kHz, T_A = 125°C	- - -	5 20 23	- - -	KΩ KΩ KΩ
Drain-to-Source Cutoff Current	$I_{DS(off)}$	V_{DS} = 15 V, V_{GS} = -6 V V_{DS} = 15 V, V_{GS} = -6 V, T_A = 125°C V_{DS} = 35 V, V_{GS} = -6 V	- - -	1 2 -	50 - 75	μA μA μA
Equivalent Input Noise Voltage	e_n	V_{DS} = 15 V, R_S = 0, R_g = 0, f = 1 kHz V_{DD} = 15 V, R_S = 360 Ω, R_g = 0, f = 1 kHz	- -	0.06 0.06	- -	μv/√Hz μv/√Hz
Audio Spot Noise Figure**	NF	V_{DD} = 15 V, R_S = 360 Ω, R_g = 1 MΩ, f = 1 kHz	-	0.86	-	dB
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	V_{DS} = 15 V, R_S = 0, f = 1 MHz V_{DD} = 15 V, R_S = 360 Ω, f = 1 MHz	- -	3.3 3	- 7	pF pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	V_{DS} = 15 V, R_S = 0, f = 1 MHz V_{DD} = 15 V, R_S = 360 Ω, f = 1 MHz	- -	0.21 0.19	- 0.30	pF pF
Power Gain (Neutralized) *(See Fig.2)*	G_{ps}	V_{DD} = 15 V, R_S = 360 Ω, f = 200 MHz	15	17	-	dB
Noise Figure *(See Fig.2)*	NF	V_{DD} = 15 V, R_S = 360 Ω, f = 200 MHz	-	4	6	dB

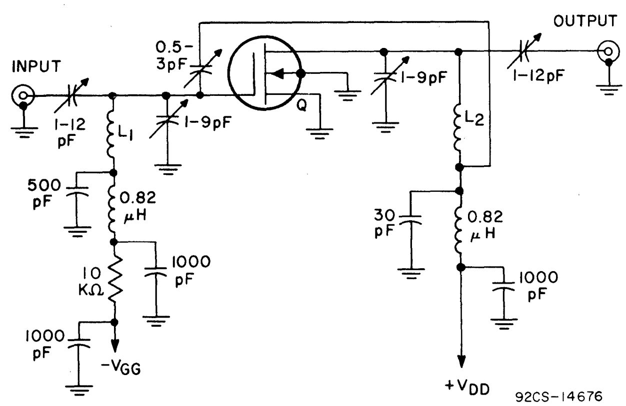
* Pulse Test: Pulse Duration = 300 μS, Duty factor ≤ 0.10.

** Noise Figure = $10 \log_{10}\left[1 + \frac{e_n^2}{4\,KT\,BW\,R_g}\right]$ where K = 1.38 x 10^{-23}; T = Temperature in °Kelvin; BW = Bandwidth in Hz; R_g = Generator resistance



C_S = 200 μF
C_1 = .01 μF
R_1 = 1 MΩ
Q = 3N139

Fig.1 - Basic test circuit.



L_1 = 4 turns #20 AWG wire 3/16"dia.,1/2"long
L_2 = 3-1/2 turns #20 AWG wire 3/8"dia.,approx. 1/2"long
Q = 3N139

Fig.2 - 200-MHz noise figure & power gain test circuit.

TYPICAL CHARACTERISTICS

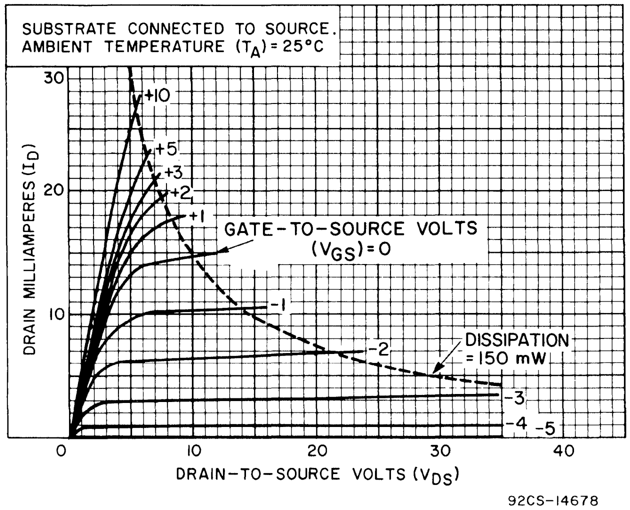


Fig.3 - Drain current vs. drain-to-source voltage.

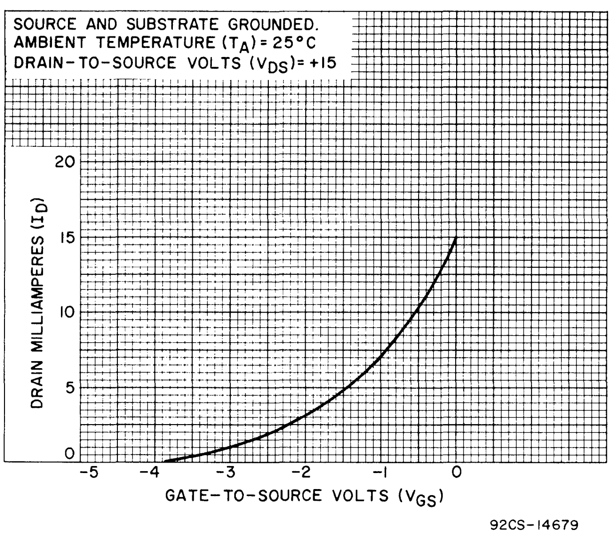


Fig.4 - Drain current vs. gate-to-source voltage.

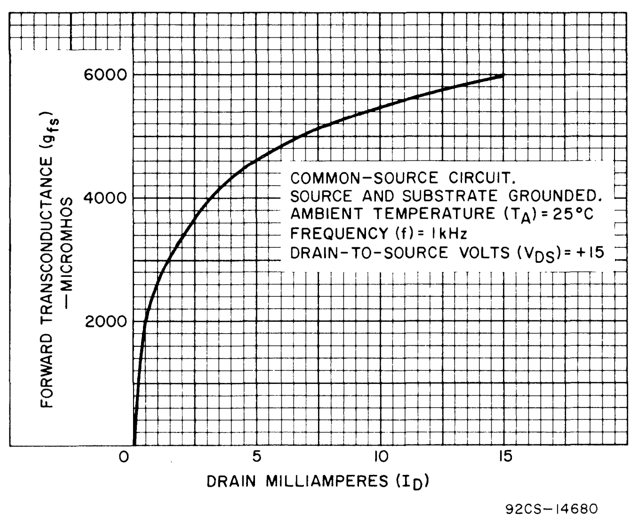
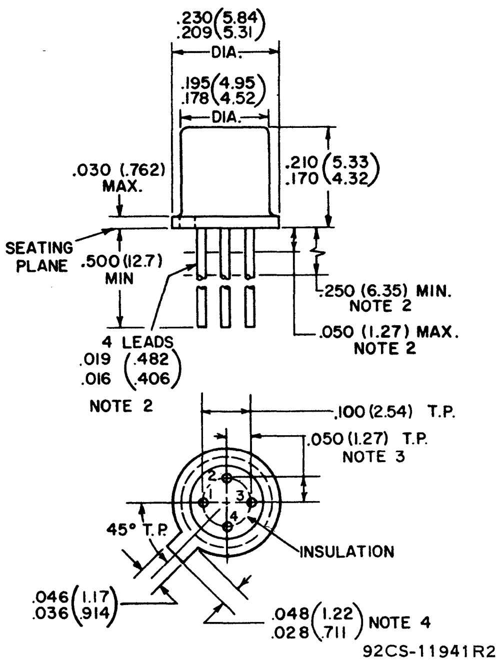


Fig.5 - 1-kHz forward transconductance vs. drain current.

DIMENSIONAL OUTLINE
JEDEC TO-72



Dimensions in inches and millimeters

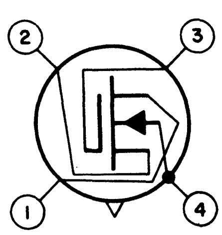
Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Note 2: The specified lead diameter applies in the zone between 0.050" (1.27 mm) and 0.250" (6.35 mm) from the seating plane. From 0 250" (6.35 mm) to the end of the lead a maximum diameter of 0.021" (0.533 mm) is held. Outside of these zones, the lead diameter is not controlled.

Note 3: Leads having a maximum diameter of 0.019" (0.482 mm) at a gauging plane of 0.054" (1.372 mm) + 0.001" (0.025 mm) - 0.000" (0.000 mm) below seating plane shall be within 0.007" (0.177 mm) of their true position (location) relative to a maximum width of tab.

Note 4: Measured from actual maximum diameter.

NEW TERMINAL ARRANGEMENT



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

RCA MOS FIELD-EFFECT TRANSISTORS

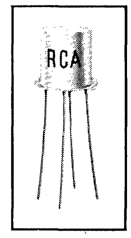
Dual Insulated-Gate Types for RF Amplifier & Mixer Service

3N140
3N141

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTORS

N-Channel Depletion Types

For Commercial and Industrial Amplifier and Mixer Applications Up to 300 MHz:



TO-72

RCA-3N140 and 3N141* are N-channel silicon, depletion type, dual insulated-gate, field-effect transistors utilizing the MOS• construction. They have exceptional characteristics for rf-amplifier and mixer applications at frequencies up to 300 MHz. These transistors feature a series arrangement of two separate channels, each channel having an independent control gate.

In the RCA-3N140 this configuration (common-source with gate No. 2 at ac ground potential) can provide exceptional rf-amplifier performance. In the RCA-3N141 each of the two signal frequencies being mixed has its own control element, thus providing excellent isolation between the oscillator and rf signals.

The mixing function performed by the 3N141 is unique in that the signal applied to gate No. 2 is used to modulate the input-gate (gate No. 1) transfer characteristic. This technique is far superior to conventional "square law" mixing, which can only be accomplished in the non-linear region of the device transfer characteristic.

The use of the 3N141 as described provides high useful conversion gains at all vhf frequencies, and the reduction in spurious responses is substantial and easily obtainable in simple circuits.

The 3N140 and 3N141 are hermetically sealed in metal JEDEC TO-72 packages.

* Formerly Dev. Nos. TA2644 and TA7274 respectively.
• Metal-Oxide-Semiconductor.

Applications

- RF Amplifier, Mixer, in TV, CB, and Communications Receivers
- Aircraft and Marine Receivers
- CATV and MATV Equipment

Performance Features

- large dynamic range
- dual gates allow product mixing with extremely low cross modulation
- greatly reduced spurious responses in FM receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability
- superior cross-modulation performance and greater dynamic range than bipolar and single-gate field-effect transistors

Device Features

- low gate leakage currents — I_{G1SS} & I_{G2SS} = 1nA max.
- high forward transconductance — (gate no. 1-to-drain): g_{fs} = 6000 μmho min.
- high unneutralized RF power gain — g_{ps} = 15dB min. at 200MHz
- low VHF noise figure — NF = 5dB max. at 200MHz
- full gate metalization

Maximum Ratings, Absolute-Maximum Values:

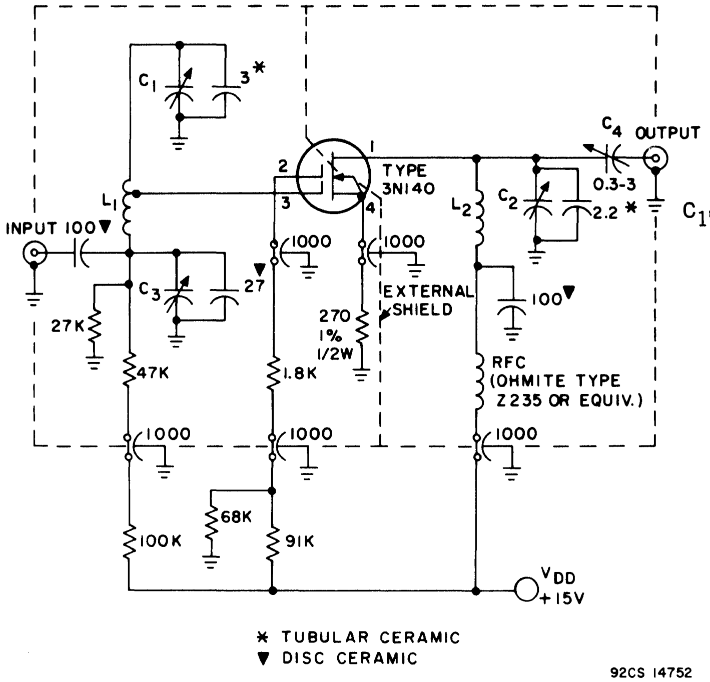
DRAIN-TO-SOURCE VOLTAGE, V_{DS}	0 to +20 max.	V
GATE NO. 1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	+1 to −8 max.	V
Instantaneous	+20 to −8 max.	V
GATE NO. 2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	−8 to 40% of V_{DS} max.	V
Instantaneous	−8 to +20 max.	V
In No Case Should the Voltage Between the Drain and Either Gate Exceed 20 Volts		
DRAIN CURRENT, I_D	Limited by Dissipation	
(Pulsed): Pulse duration ∠ 20 ms, duty factor ∠ 0.1)	50 max.	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures, up to 100°C	150 max.	mW
At ambient temperatures, above 100°C	derate linearly at 3mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	−65 to +150	°C
LEAD TEMPERATURE (During soldering): At distances ≥ 1/32″ from seating surface for 10 seconds max.	265 max.	°C

ELECTRICAL CHARACTERISTICS, at T_A = 25° C Unless Otherwise Specified. Common-Source Circuit

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS Type 3N140 RF AMPLIFIER Min.	Typ.	Max.	Type 3N141 MIXER Min.	Typ.	Max.	UNITS
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S}(off)$	V_{DS} = +20 V, I_D = 200 μA, V_{G2S} = +4 V		—	−2	−4	—	−2	−4	V
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S}(off)$	V_{DS} = +20 V, I_D = 200 μA, V_{G1S} = 0		—	−2	−4	—	−2	−4	V
Gate No. 1 Leakage Current	I_{G1SS}	V_{G1S} = −20 V, V_{G2S} = 0, V_{DS} = 0	T_A = 25°C	—	—	1	—	—	1	nA
			T_A = 125°C	—	—	2	—	—	2	μA
Gate No. 2 Leakage Current	I_{G2SS}	V_{G2S} = −20 V, V_{G1S} = 0, V_{DS} = 0	T_A = 25°C	—	—	1	—	—	1	nA
			T_A = 125°C	—	—	2	—	—	2	μA
Gate Forward Current	$I_{G(f)}$	V_{G1S} = +1 V, V_{DS} = 0		—	—	1	—	—	1	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = +13 V, V_{G1S} = 0, V_{G2S} = +4 V		5	—	30	5	—	30	mA
Drain-to-Source Cutoff Current	$I_D(off)$	V_{DS} = +20 V, V_{G1S} = −4 V, V_{G2S} = +4 V		—	—	200	—	—	—	μA
		V_{DS} = +20 V, V_{G1S} = −3 V, V_{G2S} = +1 V		—	—	—	—	—	200	μA
Small-Signal, Short-Circuit Gate No. 1-to-Source Capacitance*	C_{iss}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 MHz		2	4.5	6	2	4.5	6	pF
Small-Signal, Short-Circuit Reverse Transfer Capacitance (Drain to Gate No. 1)**	C_{rss}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 MHz		0.01	0.02	0.03	0.01	0.02	0.03	pF
Forward Transconductance (Gate No. 1 to Drain)	g_{fs}	V_{DD} = +15 V, R_S = 270 Ω, V_{G2S} = +4 V, f = 1 kHz		6000	8000	18000	6000	8000	18000	μmho
Cutoff Forward Transconductance (Gate No. 1-to-Drain)	$g_{fs}(off)$	V_{DS} = +14 V, V_{G1S} = −0.5 V, V_{G2S} = −2 V, f = 1 kHz		—	—	—	—	—	100	μmho
Power Gain (See Fig. 1 for Measurement Circuit)	G_{ps}	V_{DD} = +15 V, R_S = 270 Ω, f = 200 MHz		15	19	22	—	—	—	dB
Conversion Power Gain (See Fig. 2 for Measurement Circuit)	G_{psc}	V_{DD} = +14 V, R_S = 120 Ω, f_{IN} = 200 MHz, f_{OUT} = 30 MHz		—	—	—	15	18	21	dB
Measured Noise Figure (See Fig. 1 for Measurement Circuit)	NF	V_{DS} = +13 V, I_D = 10 mA, f = 200 MHz		—	3.5	5	—	—	—	dB
Interfering Signal Level for 1% Cross-Modulation Distortion	E_{int}	Cross Modulation = 1%, Desired Signal Frequency = 200 MHz, Undesired Signal Frequency = 150 MHz, Untuned Input, V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V		—	120	—	—	—	—	mV
Bandwidth	BW	V_{DD} = +15 V, R_S = 270 Ω, f = 200 MHz		10	—	15	10	—	15	MHz

* Capacitance between Gate No. 1 and all other terminals

** Three-Terminal Measurement with Gate No. 2 and Source Returned to Guard Terminal.



C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

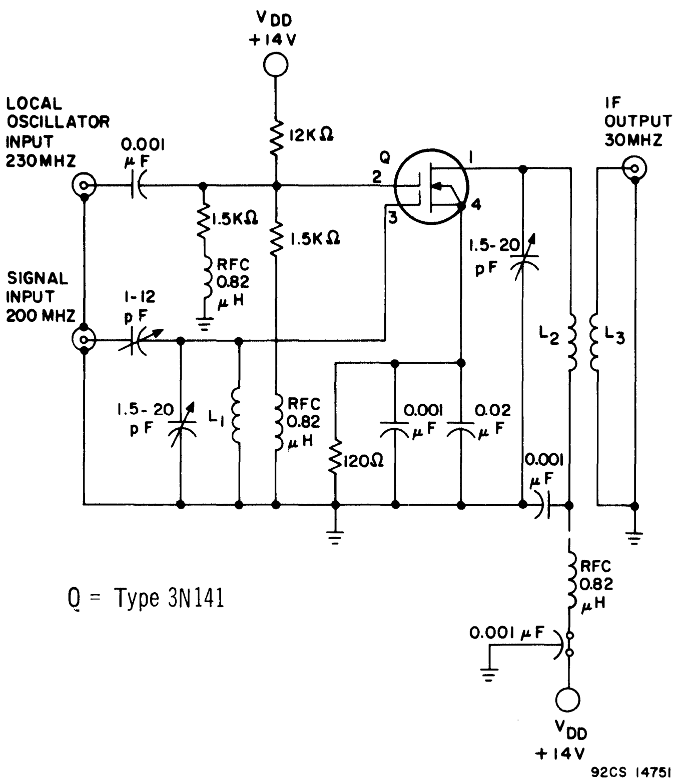
C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig. 1 – 200MHz Power Gain and Noise Figure Test Circuit for Type 3N140



L_1: 2 turns No.16 AWG enameled copper wire, 1/4" I.D.

L_2: 25 turns No.32 AWG enameled copper wire, wound on 1/4" O.D. ceramic form

L_3: 4 turns No.26 AWG enameled copper wire, wound on top of and at DC-supply end of L_2

Fig. 2 – Conversion Gain Test Circuit for Type 3N141

TYPICAL CHARACTERISTICS FOR TYPE 3N140

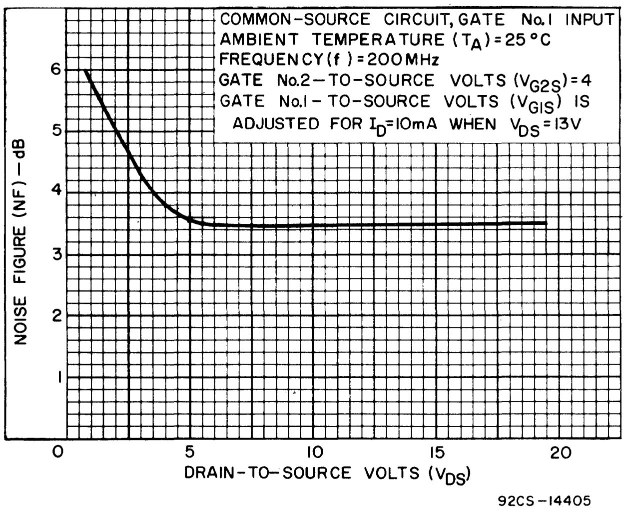


Fig. 3 — Noise Figure vs Drain-to-Source Voltage

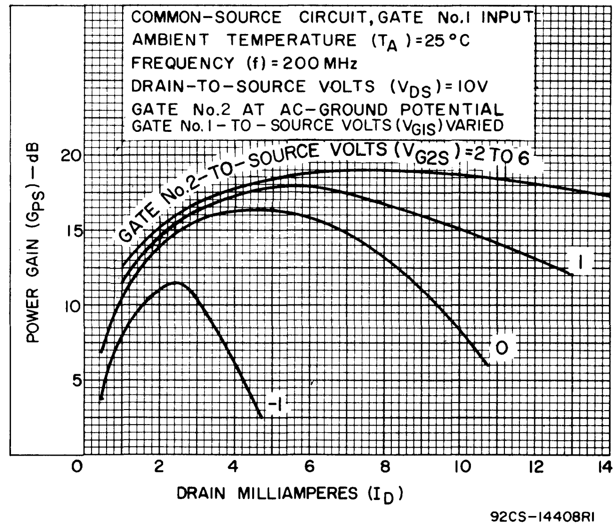


Fig. 6 — Power Gain vs Drain Current . . . V_{DS} = 10V

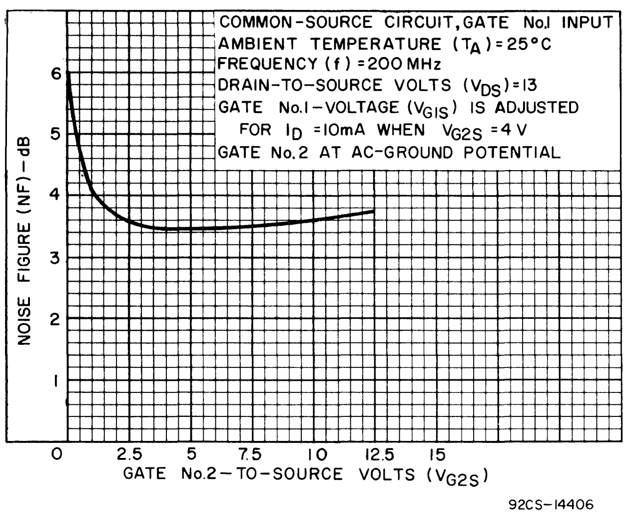


Fig. 4 — Noise Figure vs Gate No. 2-to-Source Voltage

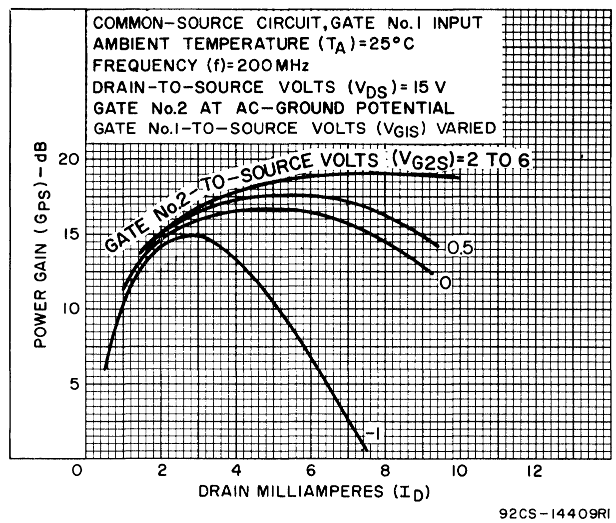


Fig. 7 — Power Gain vs Drain Current . . . V_{DS} = 15V

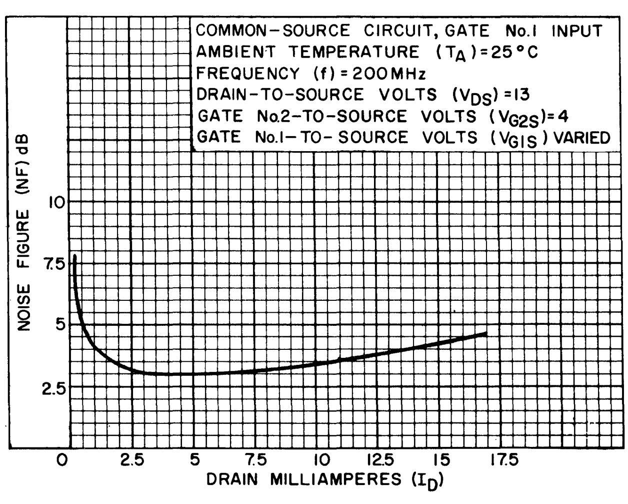


Fig. 5 — Noise Figure vs Drain Current

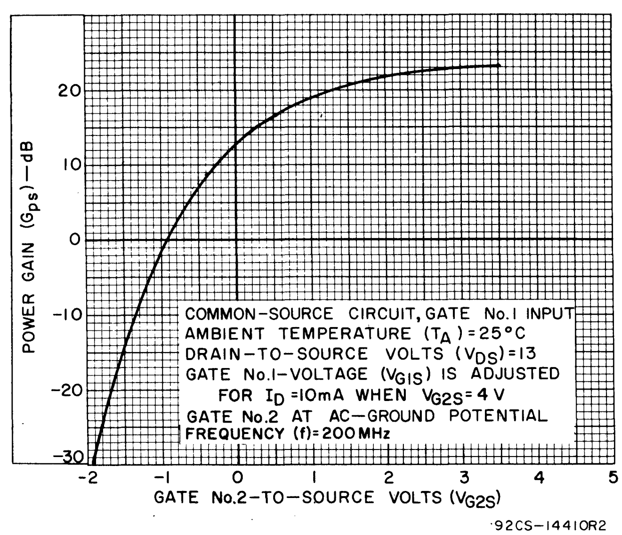


Fig. 8 — Power Gain vs Gate No. 2-to-Source Voltage

TYPICAL CHARACTERISTICS FOR TYPES 3N140, 3N141

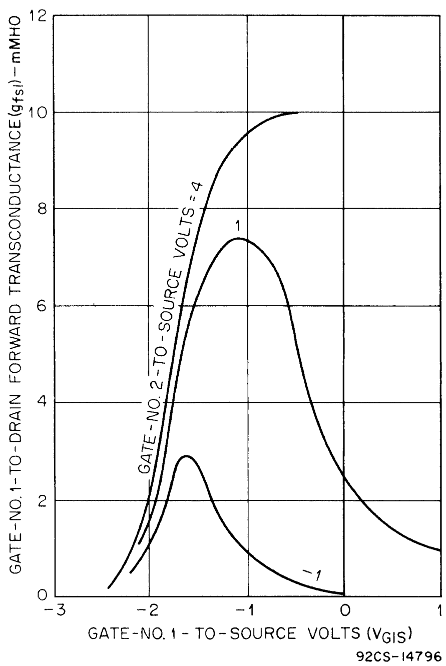


Fig. 16 – Gate-No. 1-to-Drain Forward Transconductance of a Dual-Gate MOS Transistor as a Function of Gate-No. 1-to-Source Voltage for Several Values of Gate-No. 2-to-Source Voltage

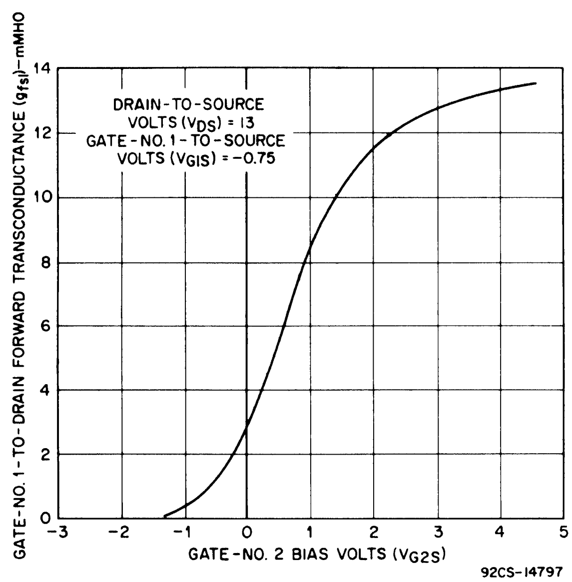


Fig. 17 – Gate-No. 1-to-Drain Forward Transconductance as a Function of Gate-No. 2 Bias Voltage for a Constant Gate-No. 1-to-Source Voltage

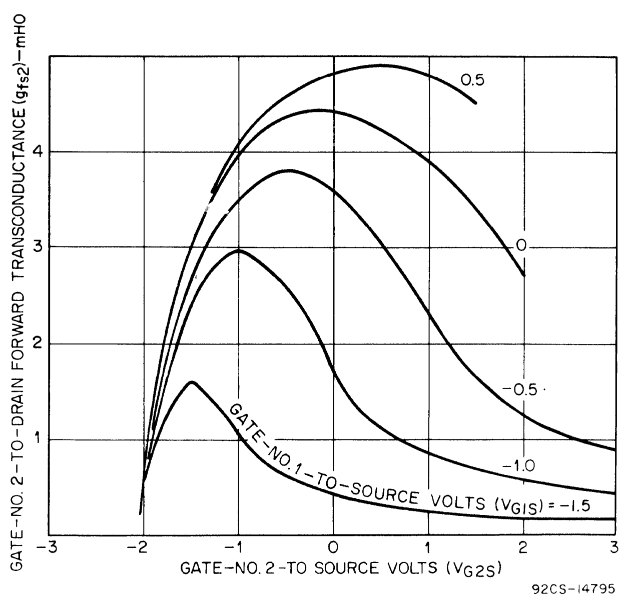


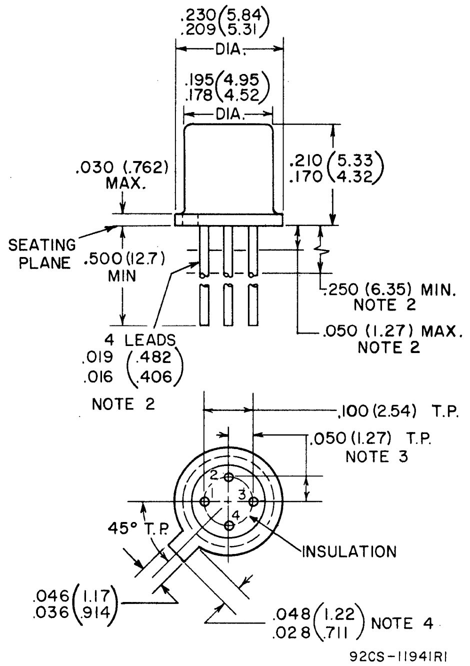
Fig. 18 – Gate-No. 2-to-Drain Forward Transconductance as a Function of Gate-No. 2 Bias Voltage for Several Values of Gate-No. 1-to-Source Voltage

OPERATING CONSIDERATIONS

The flexible leads of the 3N140 and 3N141 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the devices against high electric fields.

These devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

DIMENSIONAL OUTLINE FOR TYPES 3N140 AND 3N141 JEDEC TO-72



Dimensions in Inches and Millimeters

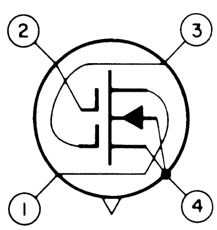
Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Note 2: The specified lead diameter applies in the zone between 0.050" (1.27 mm) and 0.250" (6.35 mm) from the seating plane. From 0.250" (6.35 mm) to the end of the lead a maximum diameter of 0.021" (0.533 mm) is held. Outside of these zones, the lead diameter is not controlled.

Note 3: Leads having a maximum diameter of 0.019" (0.482 mm) at a gauging plane of 0.054" (1.372 mm) + 0.001" (0.025 mm) -0.000" (0.000 mm) below seating plane shall be within 0.007" (0.177 mm) at their true position (location) relative to a maximum width of tab.

Note 4: Measured from actual maximum diameter.

TERMINAL DIAGRAM



Lead 1 — Drain
Lead 2 — Gate No. 2
Lead 3 — Gate No. 1
Lead 4 — Source, Substrate and Case

TYPICAL CHARACTERISTICS FOR TYPE 3N140

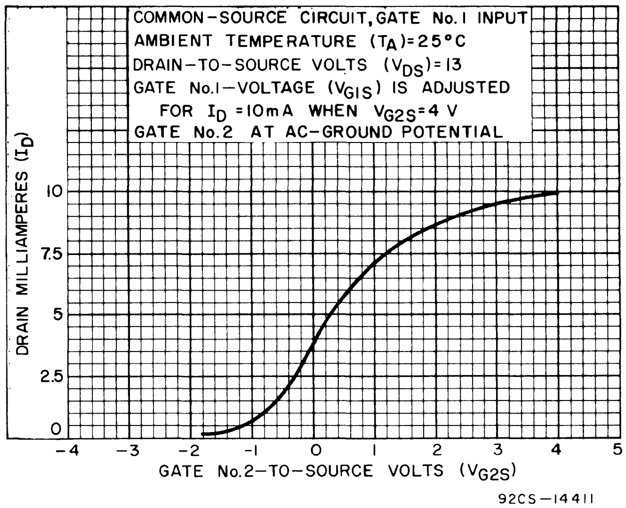


Fig. 9 – Drain Current vs Gate No. 2-to-Source Voltage

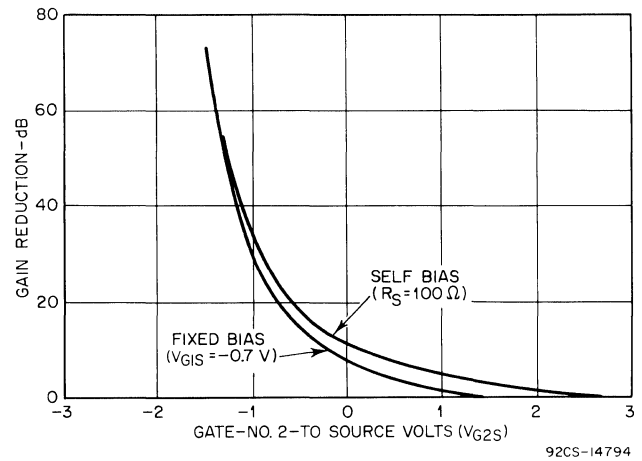


Fig. 10 – Curves Showing Gain Reduction of Dual Gate MOS RF Stage Using Fixed Bias and Self Bias as a Function of Gate-No. 2 Bias Voltage

TYPICAL CHARACTERISTICS FOR TYPE 3N141

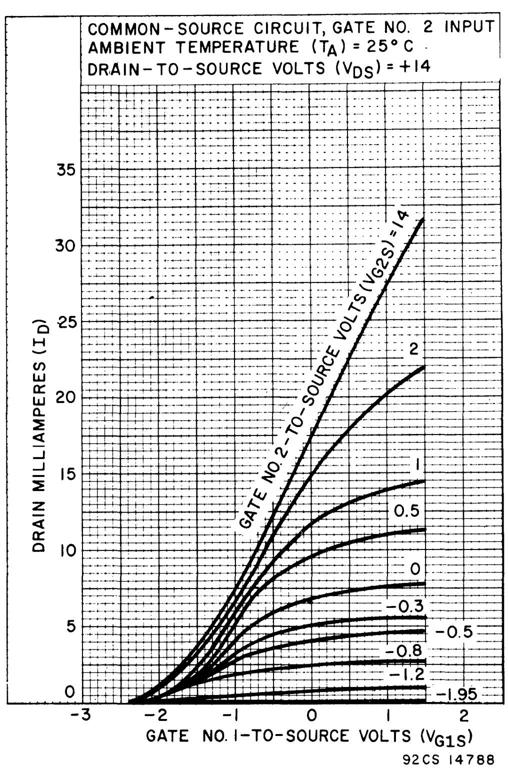


Fig.11 – Drain Current vs Gate-No. 1-to-Source Volts

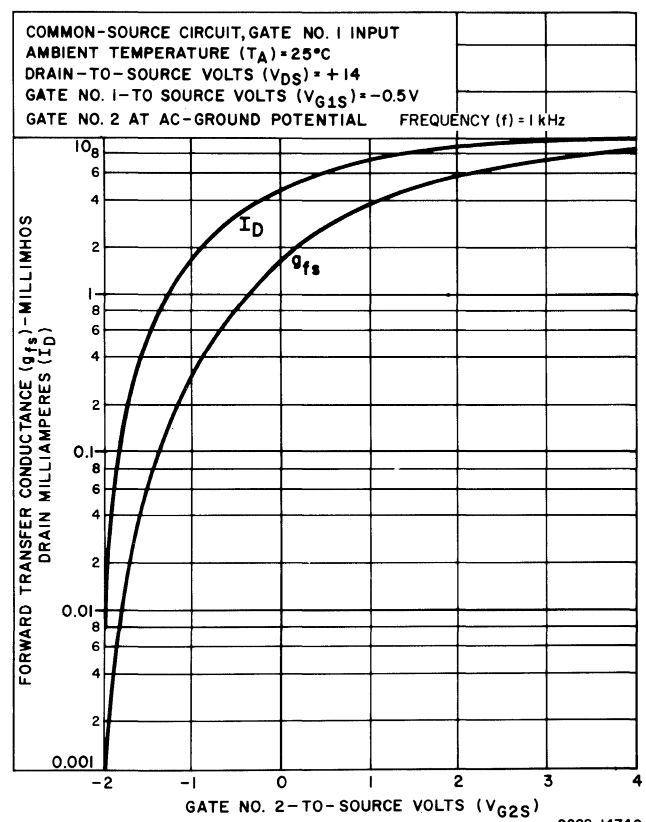


Fig. 12 – Forward Conductance and Drain Current vs Gate-No. 2-to-Source Volts

TYPICAL CHARACTERISTICS FOR TYPES 3N140, 3N141

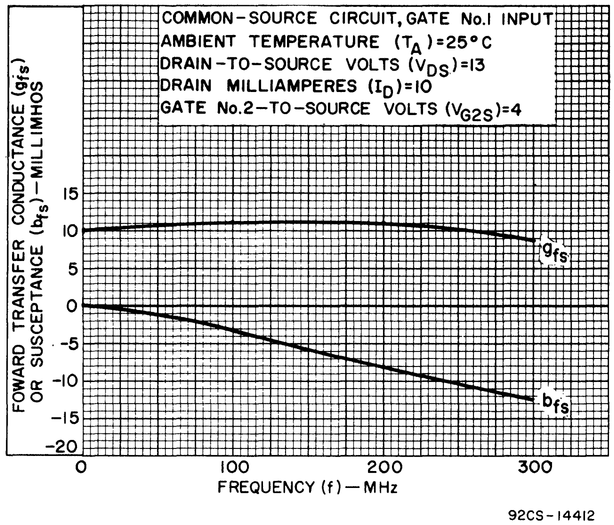


Fig. 13 – Forward Transfer Admittance (Y_{fs}) vs Frequency

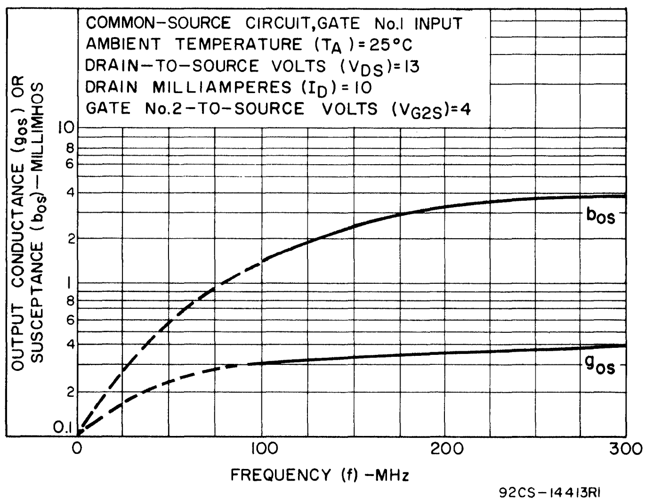


Fig. 14 – Output Admittance (Y_{os}) vs Frequency

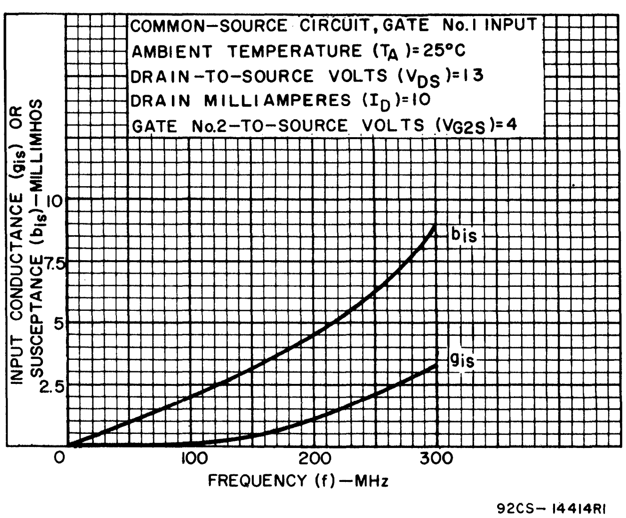


Fig. 15 – Input Admittance (Y_{is}) vs Frequency

RCA MOS FIELD-EFFECT TRANSISTOR

For Industrial and Military Applications to 175 MHz

3N142

File No 286

RCA-3N142† is a silicon, insulated-gate field-effect transistor of the N-channel depletion type utilizing the MOS* construction. It features

- high input resistance — 1000 megohms
- low feedback capacitance — 0.2pF max.
- low noise figure — 4dB typ.
- high useful power gain —
  neutralized — 17dB typ. } at 100MHz
  unneutralized — 14dB typ. }
- hermetically sealed TO-104 metal package

RCA-3N142 is intended primarily for use as the rf amplifier in FM receivers covering the 88 to 108MHz band, but can be used for general amplifier applications at frequencies up to 175 MHz.

The wide dynamic range of the 3N142 reduces cross-modulation effects in AM receivers and minimizes the generation of spurious responses in FM receivers.

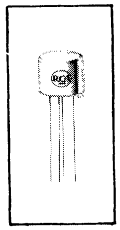
† Formerly Dev. No. TA7306
* Metal-Oxide-Semiconductor

Maximum Ratings, Absolute-Maximum Values:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 max.	V
GATE-TO-SOURCE VOLTAGE, V_{GS}:		
Continuous	0 to −8 max.	V
Instantaneous	±15 max.	V
DRAIN-TO-GATE VOLTAGE, V_{DG}	+20 max.	V
DRAIN CURRENT, I_D**	50 max.	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures { up to 85°C	100 max.	mW
At ambient temperatures { above 85°C	Derate at 6.67mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage	−65 to +100	°C
Operating	−65 to +100	°C
LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32″ from seating surface for 10 seconds max.	265 max.	°C

** Pulse Value. Pulse duration, 20ms max., Duty factor ≤0.1

SILICON INSULATED-GATE FIELD-EFFECT TRANSISTOR N-Channel Depletion Type



JEDEC TO-104

For Frequencies up to 175 MHz

Applications

- RF Amplifier, Mixer, and Oscillator in:
  CB and Mobile Communication Receivers
  Aircraft and Marine Receivers
  CATV and MATV Equipment
- Industrial Control Circuits
- Variable Attenuators
- Current Limiters
- Instrumentation Equipment
- High-Impedance Timing Circuits

Performance Features

- large dynamic range
- enhanced signal-handling capability for low cross-modulation
- dual-polarity gate permits positive and negative swing without degradation of input impedance
- reduced spurious responses in FM receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability for critical oscillator designs

ELECTRICAL CHARACTERISTICS, at T_A = 25° C Unless Otherwise Specified. Bulk (Substrate) Connected to Source

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS			UNITS
		FREQUENCY f	DC DRAIN-TO-SOURCE VOLTAGE V_{DS}	DC GATE-TO-SOURCE VOLTAGE V_{GS}	DC DRAIN CURRENT I_D	TYPE 3N142			
		MHz	V	V	mA	Min.	Typ.	Max.	
Drain-to-Source Cutoff Current	$I_D(off)$		20	−8		—	—	100	μA
Zero-Bias Drain Current*	I_{DSS}		15	0		5	20	50	mA
Gate Reverse Current	I_{GSS}	T_A = 25°C	0	−8		—	—	1	nA
		T_A = 100°C	0	−8		—	—	100	nA
Gate-to-Source Cutoff Voltage	$V_{GS}(off)$		20		0.05	−2	−5	−8	V
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15		5	—	0.12	0.2	pF
Input Resistance	r_{is}	100	15		5	2	4.5	—	KΩ
Input Capacitance	C_{iss}	1	15		5	—	5.5	10	pF
Output Resistance	r_{os}	100	15		5	2.25	4.2	—	KΩ
Output Capacitance	C_{oss}	100	15		5	—	1.4	—	pF
Forward Transconductance	g_{fs}	100	15		5	4	7.5	—	mmho
Maximum Available Power Gain	MAG	100	15		5	—	24	—	dB
Maximum Usable Power Gain (Unneutralized)	MUG	100	15		5	—	14	—	dB
Maximum Usable Power Gain (Neutralized)	MUG	100	15		5	15	17	—	dB
Noise Figure	NF	100	15		5	—	4	5	dB

* Pulse test: Pulse Duration 20 ms max. Duty Factor ≤0.15.

OPERATING CONSIDERATIONS

The flexible leads of the 3N142 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields.

This device should not be connected into, or disconnected from, circuits with the power on because high transient voltages may cause permanent damage to the device.

TYPICAL y PARAMETER CHARACTERISTICS

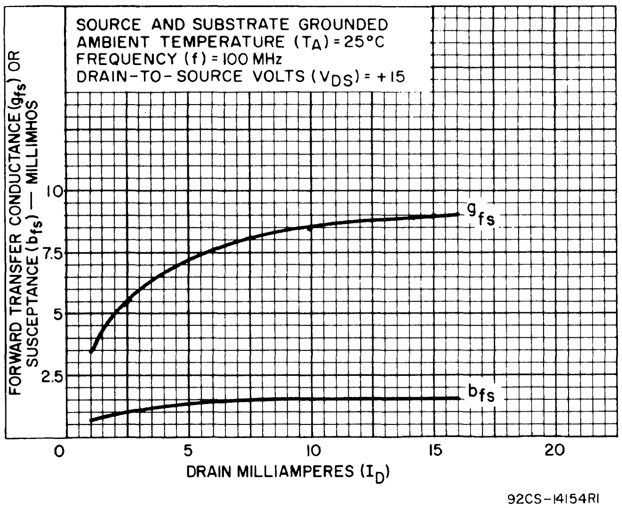


Fig. 7 – Forward Transadmittance (y_{fs}) vs Drain Current (I_D)

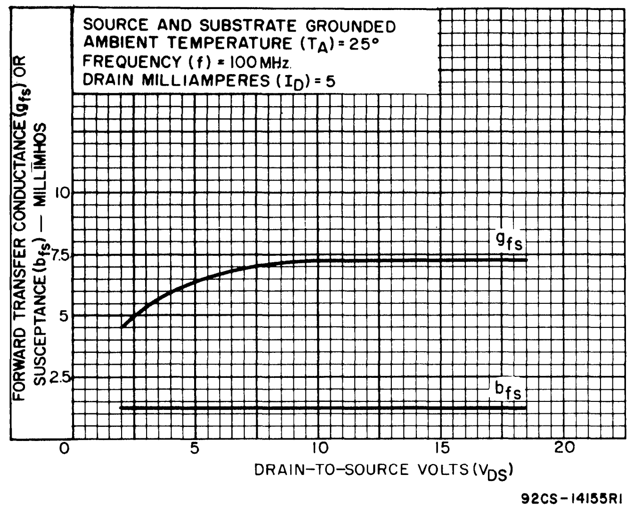


Fig. 8 – Forward Transadmittance (y_{fs}) vs Drain-to-Source Voltage (V_{DS})

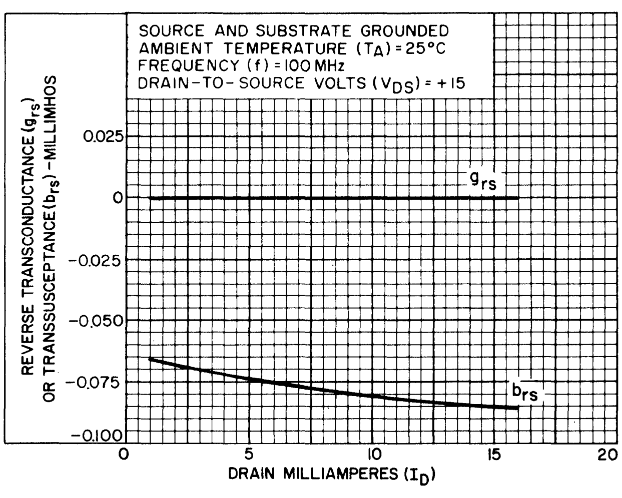


Fig. 9 – Reverse Transadmittance (y_{rs}) vs Drain Current (I_D)

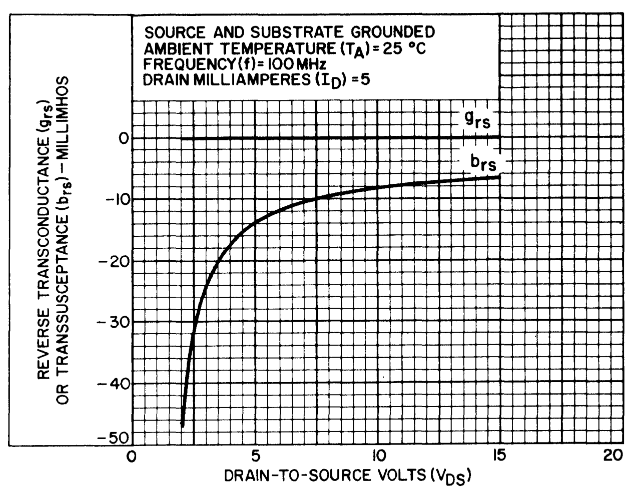


Fig. 10 – Reverse Transadmittance (y_{rs}) vs Drain-to-Source Voltage (V_{DS})

TYPICAL COMMON-SOURCE ADMITTANCE (Y) COMPONENTS vs FREQUENCY

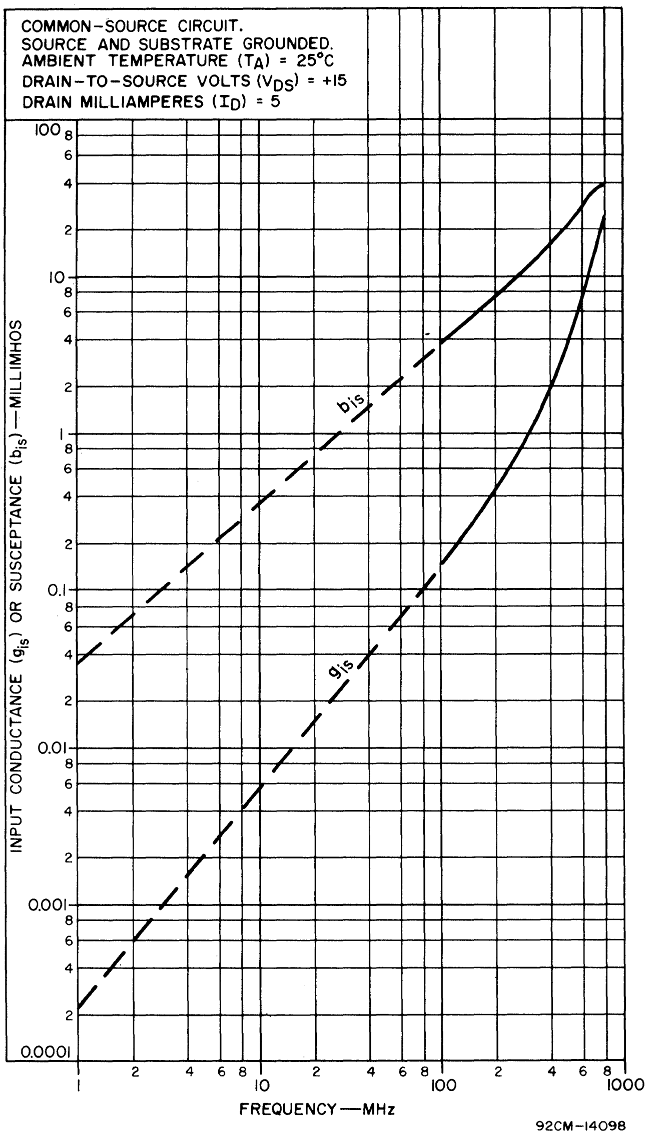


Fig. 11 – Input Admittance (Y_{is}) Components

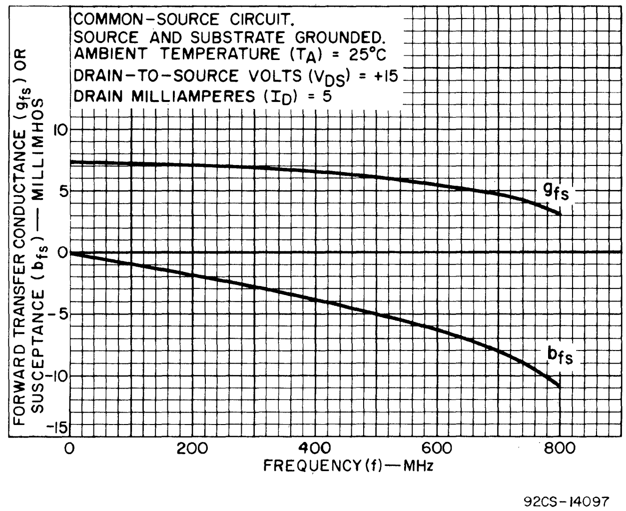


Fig. 12 – Forward Transadmittance (Y_{fs}) Components

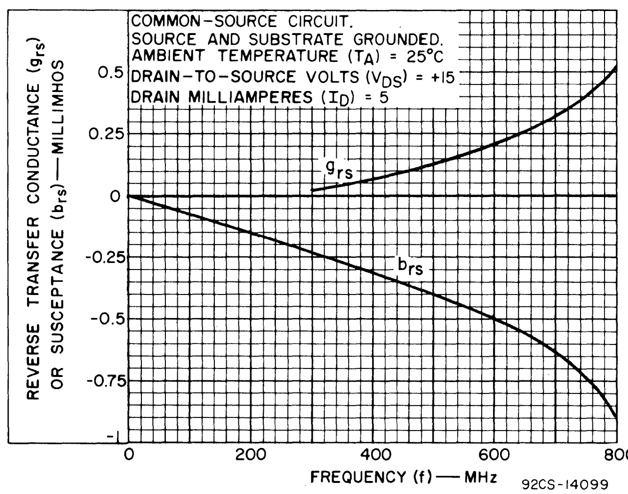


Fig. 13 – Reverse Transadmittance (Y_{rs}) Components

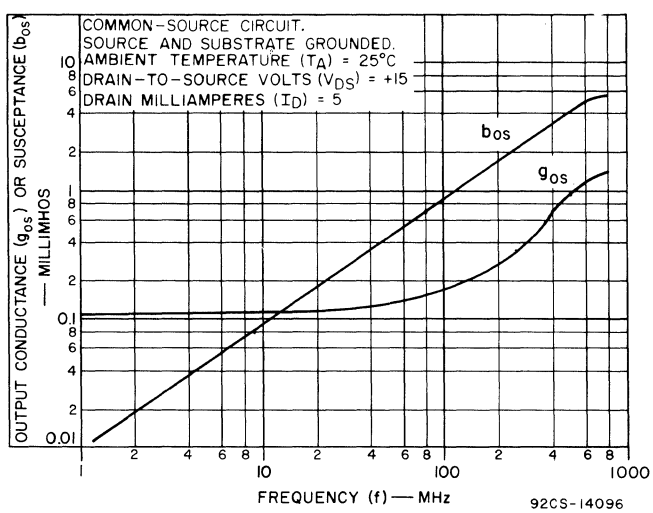
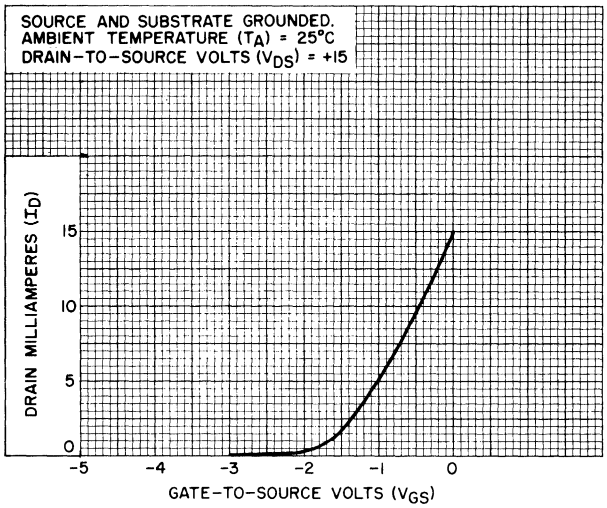


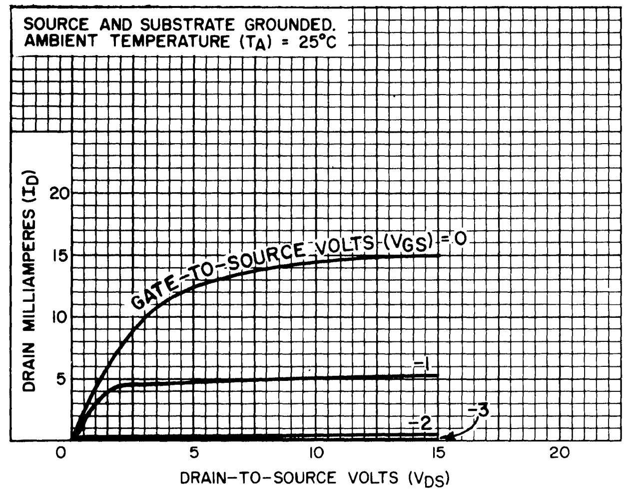
Fig. 14 – Output Admittance (Y_{os}) Components

TYPICAL CHARACTERISTICS



92CS-14090

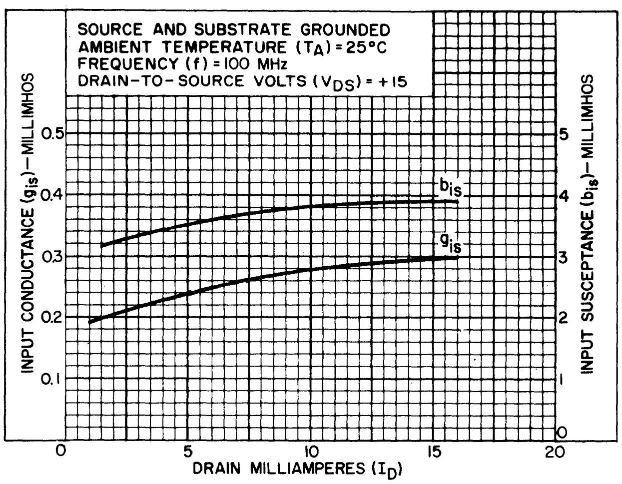
Fig. 1 – Typical Characteristic of Drain Current (I_D) vs Gate-to-Source Voltage (V_{GS})



92CS-14091

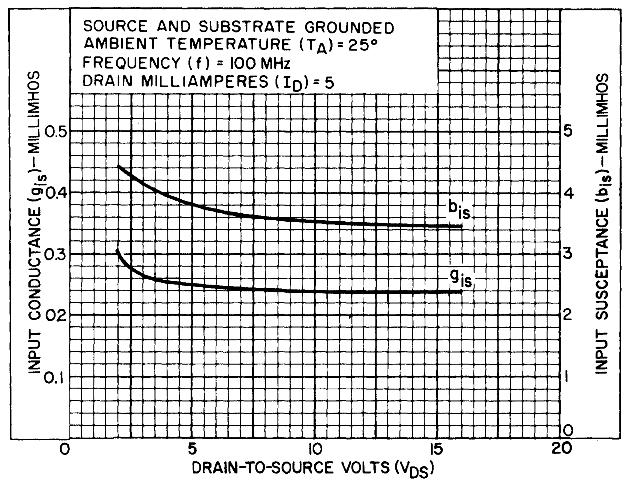
Fig. 2 – Drain Current (I_D) vs Drain-to-Source Voltage (V_{DS})

TYPICAL y PARAMETER CHARACTERISTICS



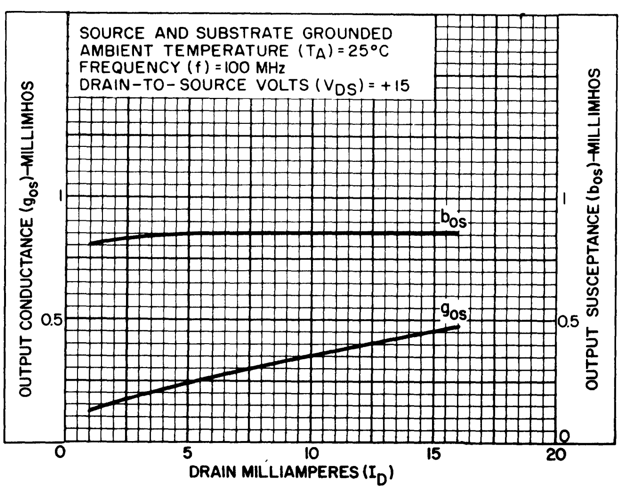
92CS-14149RI

Fig. 3 – Input Admittance (y_{is}) vs Drain Current (I_D)



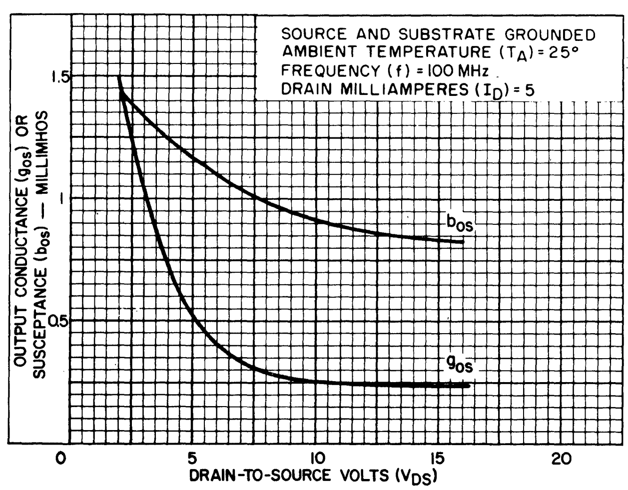
92CS-14148RI

Fig. 4 – Input Admittance (y_{is}) vs Drain-to-Source Voltage (V_{DS})



92CS-14152RI

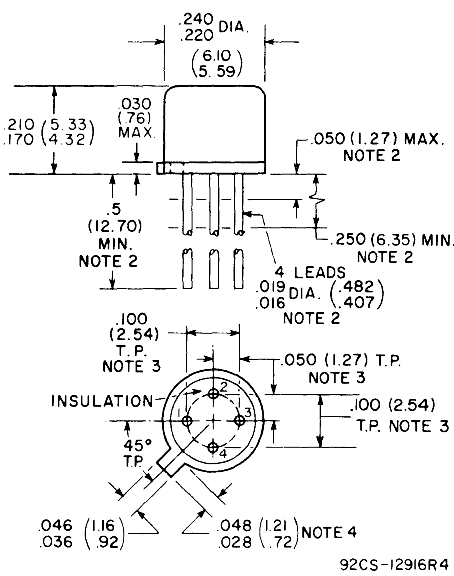
Fig. 5 – Output Admittance (y_{os}) vs Drain Current (I_D)



92CS-14153RI

Fig. 6 – Output Admittance (y_{os}) vs Drain-to-Source Voltage (V_{DS})

DIMENSIONAL OUTLINE
TO-104



DIMENSIONS IN INCHES AND MILLIMETERS

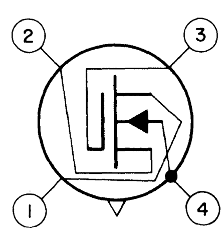
Note 1: *Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.*

Note 2: The specified lead diameter applies in the zone between 0.050" (1.27 mm) and 0.250"(6.35 mm) from the seating plane. From 0.250"(6.35 mm) to the end of the lead a maximum diameter of 0.021"(0.533 mm) is held. Outside of these zones, the lead diameter is not controlled.

Note 3: Leads having a maximum diameter of 0.019" (0.482 mm) at a gauging plane of 0.054"(1.372 mm) + 0.001" (0.025 mm) -0.000"(0.000 mm) below seating plane shall be within 0.007" (0.177 mm) of their true position (location) relative to a maxi- width of tab.

Note 4: Measured from actual maximum diameter.

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - SOURCE
LEAD 3 - INSULATED GATE
LEAD 4 - BULK (SUBSTRATE) AND CASE