NCR Product Design Series

VS1500F Standard Cell Library Data Sheets

Revision 5.0
May 1991

NCR 1.5µ FAST STANDARD CELL LIBRARY DATA SHEETS ALPHABETICAL CONTENTS

NCR 1.5μ FAST STANDARD CELL LIBRARY DATA SHEETS FUNCTIONAL CONTENTS

Simple Logic Cells

Buffers

Latches

Shift Registers

Decoders and Multiplexers

Flip–flops

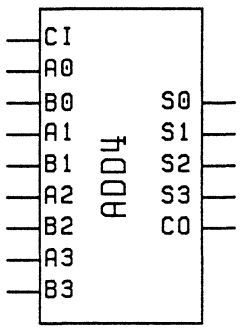
Special Function Cells

Tristate Elements

Input/Output Cells

4–Bit Adder

The ADD4 is a four–bit, asynchronous, ripple adder with carry–in/carry–out function. See the ADD4CS data sheet for application notes.



Inputs: CI, A0, B0, A1, B1, A2, B2, A3, B3
Outputs: S0, S1, S2, S3, CO
Input Cap.: CI, A0: 0.406
B0: 0.407
A1: 0.361
B1: 0.360
A2: 0.218
B2: 0.221
A3: 0.218
B3: 0.221 pF
Cell Size: 112 grids wide, 12 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A0 TO CO	4.60	8.49	8.85	9.93	4.51+0.583*C_L ns
t_{PHL}		4.71	8.70	9.07	10.2	4.57+0.924*C_L ns
t_{PLH}	A1 TO CO	4.04	7.45	7.77	8.72	3.95+0.585*C_L ns
t_{PHL}		4.17	7.69	8.02	9.00	4.02+0.937*C_L ns
t_{PLH}	A2 TO CO	3.23	5.97	6.22	6.98	3.14+0.573*C_L ns
t_{PHL}		3.61	6.66	6.95	7.79	3.47+0.931*C_L ns
t_{PLH}	A3 TO CO	2.10	3.88	4.05	4.54	2.01+0.592*C_L ns
t_{PHL}		2.46	4.54	4.73	5.31	2.32+0.932*C_L ns
t_{PLH}	B0 TO CO	4.63	8.55	8.91	10.0	4.54+0.573*C_L ns
t_{PHL}		4.64	8.56	8.93	10.0	4.49+0.939*C_L ns
t_{PLH}	B1 TO CO	4.15	7.66	7.98	8.96	4.06+0.582*C_L ns
t_{PHL}		4.18	7.72	8.04	9.03	4.04+0.937*C_L ns
t_{PLH}	B2 TO CO	3.34	6.18	6.44	7.22	3.26+0.567*C_L ns
t_{PHL}		3.64	6.73	7.02	7.87	3.50+0.939*C_L ns
t_{PLH}	B3 TO CO	2.20	4.06	4.23	4.75	2.11+0.577*C_L ns
t_{PHL}		2.50	4.62	4.82	5.41	2.36+0.923*C_L ns
t_{PLH}	CI TO CO	4.49	8.30	8.65	9.71	4.41+0.563*C_L ns
t_{PHL}		4.60	8.50	8.86	9.94	4.46+0.929*C_L ns
t_{PLH}	CI TO S0	1.43	2.65	2.76	3.10	1.13+2.05*C_L ns
t_{PHL}		0.939	1.73	1.81	2.03	0.799+0.932*C_L ns
t_{PLH}	CI TO S1	2.27	4.19	4.37	4.90	2.05+1.46*C_L ns
t_{PHL}		1.90	3.51	3.65	4.10	1.75+0.999*C_L ns

Switching characteristics (Sheet 1 of 3)

ADD4

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CI TO S2	3.38	6.24	6.50	7.30	3.16+1.44*C_L ns
t_{PHL}		3.04	5.61	5.85	6.56	2.89+0.995*C_L ns
t_{PLH}	CI TO S3	4.53	8.37	8.73	9.79	4.32+1.42*C_L ns
t_{PHL}		4.19	7.73	8.06	9.04	4.04+0.988*C_L ns
t_{PLH}	A0,B0 TO S0	2.10	3.88	4.05	4.54	1.78+2.14*C_L ns
t_{PHL}		2.01	3.72	3.88	4.35	1.81+1.36*C_L ns
t_{PLH}	A0,B0 TO S1	2.37	4.38	4.57	5.12	2.15+1.47*C_L ns
t_{PHL}		2.01	3.71	3.86	4.34	1.85+1.01*C_L ns
t_{PLH}	A0,B0 TO S2	3.50	6.46	6.73	7.56	3.28+1.44*C_L ns
t_{PHL}		3.14	5.81	6.05	6.79	2.99+0.999*C_L ns
t_{PLH}	A0,B0 TO S3	4.65	8.59	8.96	10.0	4.43+1.44*C_L ns
t_{PHL}		4.29	7.91	8.25	9.26	4.13+0.998*C_L ns
t_{PLH}	A1,B1 TO S1	2.10	3.88	4.05	4.54	1.78+2.14*C_L ns
t_{PHL}		2.01	3.72	3.88	4.35	1.81+1.36*C_L ns
t_{PLH}	A1,B1 TO S2	2.56	4.73	4.93	5.53	2.35+1.43*C_L ns
t_{PHL}		1.81	3.34	3.49	3.91	1.66+0.993*C_L ns
t_{PLH}	A1,B1 TO S3	3.27	6.03	6.29	7.05	2.94+2.14*C_L ns
t_{PHL}		3.81	7.04	7.33	8.23	3.60+1.36*C_L ns
t_{PLH}	A2,B2 TO S2	2.10	3.88	4.05	4.54	1.78+2.14*C_L ns
t_{PHL}		2.01	3.72	3.88	4.35	1.81+1.36*C_L ns
t_{PLH}	A2,B2 TO S3	2.15	3.97	4.14	4.64	1.83+2.14*C_L ns
t_{PHL}		2.66	4.90	5.11	5.74	2.45+1.36*C_L ns
t_{PLH}	A3,B3 TO S3	2.10	3.88	4.05	4.54	1.78+2.14*C_L ns
t_{PHL}		2.01	3.72	3.88	4.35	1.81+1.36*C_L ns
t_r	A0 TO CO	0.735	1.36	1.41	1.59	0.564+1.14*C_L ns
t_f		0.767	1.42	1.48	1.66	0.491+1.84*C_L ns
t_r	A1 TO CO	0.736	1.36	1.42	1.59	0.566+1.14*C_L ns
t_f		0.776	1.43	1.49	1.68	0.498+1.85*C_L ns
t_r	A2 TO CO	0.725	1.34	1.40	1.57	0.554+1.14*C_L ns
t_f		0.780	1.44	1.50	1.68	0.503+1.84*C_L ns
t_r	A3 TO CO	0.739	1.37	1.42	1.60	0.568+1.14*C_L ns
t_f		0.774	1.43	1.49	1.67	0.499+1.83*C_L ns
t_r	B0 TO CO	0.736	1.36	1.42	1.59	0.566+1.13*C_L ns
t_f		0.778	1.44	1.50	1.68	0.501+1.84*C_L ns
t_r	B1 TO CO	0.728	1.34	1.40	1.57	0.556+1.14*C_L ns
t_f		0.778	1.44	1.50	1.68	0.501+1.84*C_L ns
t_r	B2 TO CO	0.735	1.36	1.42	1.59	0.565+1.13*C_L ns
t_f		0.776	1.43	1.49	1.68	0.499+1.85*C_L ns
t_r	B3 TO CO	0.736	1.36	1.42	1.59	0.564+1.14*C_L ns
t_f		0.768	1.42	1.48	1.66	0.493+1.83*C_L ns
t_r	CI TO CO	0.736	1.36	1.42	1.59	0.566+1.13*C_L ns
t_f		0.778	1.44	1.50	1.68	0.500+1.85*C_L ns
t_r	CI TO S0	1.59	2.93	3.06	3.43	0.882+4.70*C_L ns
t_f		1.19	2.20	2.29	2.57	0.835+2.35*C_L ns
t_r	CI TO S1	1.76	3.26	3.40	3.81	1.16+4.06*C_L ns
t_f		1.02	1.89	1.97	2.21	0.659+2.43*C_L ns
t_r	CI TO S2	1.69	3.12	3.26	3.65	1.08+4.09*C_L ns

Switching characteristics (Sheet 2 of 3)

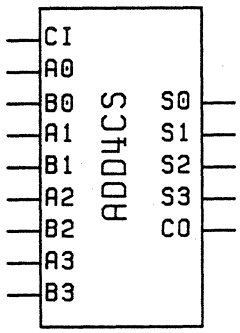
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_f		1.02	1.88	1.96	2.20	0.655+2.43*C_L ns
t_r	CI TO S3	1.71	3.16	3.29	3.70	1.10+4.07*C_L ns
t_f		1.02	1.89	1.97	2.21	0.657+2.43*C_L ns
t_r	A0,B0 TO S0	1.46	2.69	2.80	3.15	0.736+4.80*C_L ns
t_f		0.872	1.61	1.68	1.88	0.453+2.79*C_L ns
t_r	A0,B0 TO S1	1.73	3.20	3.34	3.75	1.12+4.09*C_L ns
t_f		1.05	1.93	2.01	2.26	0.682+2.42*C_L ns
t_r	A0,B0 TO S2	1.67	3.09	3.22	3.61	1.06+4.10*C_L ns
t_f		1.02	1.89	1.97	2.21	0.660+2.43*C_L ns
t_r	A0,B0 TO S3	1.68	3.11	3.24	3.64	1.07+4.09*C_L ns
t_f		1.03	1.89	1.97	2.22	0.661+2.43*C_L ns
t_r	A1,B1 TO S1	1.46	2.69	2.80	3.15	0.736+4.80*C_L ns
t_f		0.872	1.61	1.68	1.88	0.453+2.79*C_L ns
t_r	A1,B1 TO S2	1.71	3.15	3.29	3.69	1.10+4.07*C_L ns
t_f		1.000	1.85	1.93	2.16	0.633+2.45*C_L ns
t_r	A1,B1 TO S3	1.47	2.71	2.82	3.17	0.745+4.80*C_L ns
t_f		0.865	1.60	1.67	1.87	0.445+2.80*C_L ns
t_r	A2,B2 TO S2	1.46	2.69	2.80	3.15	0.736+4.80*C_L ns
t_f		0.872	1.61	1.68	1.88	0.453+2.79*C_L ns
t_r	A2,B2 TO S3	1.47	2.72	2.83	3.18	0.751+4.80*C_L ns
t_f		0.879	1.62	1.69	1.90	0.462+2.78*C_L ns
t_r	A3,B3 TO S3	1.46	2.69	2.80	3.15	0.736+4.80*C_L ns
t_f		0.872	1.61	1.68	1.88	0.453+2.79*C_L ns

Switching characteristics (Sheet 3 of 3)

4–Bit Carry Select Adder

The ADD4CS is a 4-bit adder with carry-in/ carry-out function optimized for fast carry-in to carry-out and sum propagation delay.



Inputs: CI, A0, B0, A1, B1, A2, B2, A3, B3
Outputs: S0, S1, S2, S3, CO
Input Cap.: CI: 0.319
A0: 0.408
B0: 0.405
A1: 0.361
B1: 0.360
A2: 0.218
B2: 0.221
A3: 0.218
B3: 0.221 pF
Cell Size: 186 grids wide, 14 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A0 TO CO	5.05	9.32	9.72	10.9	4.96+0.545*C_L ns
t_{PHL}		4.89	9.04	9.42	10.6	4.75+0.918*C_L ns
t_{PLH}	A1 TO CO	4.69	8.66	9.02	10.1	4.64+0.321*C_L ns
t_{PHL}		5.27	9.74	10.2	11.4	5.13+0.943*C_L ns
t_{PLH}	A2 TO CO	4.18	7.71	8.04	9.02	4.12+0.323*C_L ns
t_{PHL}		4.95	9.15	9.54	10.7	4.81+0.956*C_L ns
t_{PLH}	A3 TO CO	3.11	5.74	5.99	6.72	3.06+0.321*C_L ns
t_{PHL}		3.83	7.08	7.38	8.28	3.69+0.940*C_L ns
t_{PLH}	B0 TO CO	5.05	9.33	9.73	10.9	4.97+0.545*C_L ns
t_{PHL}		4.96	9.16	9.55	10.7	4.82+0.917*C_L ns
t_{PLH}	B1 TO CO	4.84	8.94	9.32	10.5	4.76+0.551*C_L ns
t_{PHL}		5.14	9.49	9.89	11.1	5.00+0.913*C_L ns
t_{PLH}	B2 TO CO	4.33	8.00	8.33	9.35	4.25+0.545*C_L ns
t_{PHL}		4.82	8.90	9.28	10.4	4.68+0.914*C_L ns
t_{PLH}	B3 TO CO	3.24	5.99	6.24	7.00	3.16+0.547*C_L ns
t_{PHL}		3.71	6.85	7.14	8.01	3.57+0.921*C_L ns
t_{PLH}	CI TO CO	0.933	1.72	1.80	2.01	0.844+0.586*C_L ns
t_{PHL}		0.940	1.74	1.81	2.03	0.805+0.901*C_L ns
t_{PLH}	CI TO S0	2.30	4.26	4.44	4.98	2.00+2.05*C_L ns
t_{PHL}		1.84	3.41	3.55	3.98	1.70+0.934*C_L ns
t_{PLH}	CI TO S1	2.07	3.83	3.99	4.47	1.98+0.610*C_L ns

Switching characteristics (Sheet 1 of 3)

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}		2.17	4.01	4.18	4.68	2.07+0.640*C_L ns
t_{PLH}	CI TO S2	2.07	3.83	3.99	4.47	1.98+0.610*C_L ns
t_{PHL}		2.17	4.01	4.18	4.68	2.07+0.640*C_L ns
t_{PLH}	CI TO S3	2.07	3.83	3.99	4.47	1.98+0.610*C_L ns
t_{PHL}		2.17	4.01	4.18	4.68	2.07+0.640*C_L ns
t_{PLH}	A0,B0 TO S0	2.05	3.79	3.95	4.43	1.73+2.13*C_L ns
t_{PHL}		1.94	3.58	3.74	4.19	1.73+1.39*C_L ns
t_{PLH}	A0,B0 TO S1	4.07	7.53	7.84	8.80	3.98+0.625*C_L ns
t_{PHL}		3.07	5.67	5.91	6.63	2.97+0.648*C_L ns
t_{PLH}	A0,B0 TO S2	5.11	9.44	9.84	11.0	5.02+0.618*C_L ns
t_{PHL}		4.16	7.69	8.02	9.00	4.07+0.643*C_L ns
t_{PLH}	A0,B0 TO S3	6.21	11.5	12.0	13.4	6.11+0.644*C_L ns
t_{PHL}		5.25	9.69	10.1	11.3	5.14+0.661*C_L ns
t_{PLH}	A1,B1 TO S1	2.05	3.79	3.95	4.43	1.73+2.13*C_L ns
t_{PHL}		1.94	3.58	3.74	4.19	1.73+1.39*C_L ns
t_{PLH}	A1,B1 TO S2	4.70	8.68	9.05	10.2	4.60+0.630*C_L ns
t_{PHL}		3.49	6.45	6.73	7.55	3.39+0.647*C_L ns
t_{PLH}	A1,B1 TO S3	4.67	8.63	9.00	10.1	4.58+0.632*C_L ns
t_{PHL}		5.61	10.4	10.8	12.1	5.51+0.652*C_L ns
t_{PLH}	A2,B2 TO S2	2.05	3.79	3.95	4.43	1.73+2.13*C_L ns
t_{PHL}		1.94	3.58	3.74	4.19	1.73+1.39*C_L ns
t_{PLH}	A2,B2 TO S3	3.59	6.62	6.90	7.75	3.49+0.631*C_L ns
t_{PHL}		4.47	8.25	8.60	9.65	4.37+0.674*C_L ns
t_{PLH}	A3,B3 TO S3	2.05	3.79	3.95	4.43	1.73+2.13*C_L ns
t_{PHL}		1.94	3.58	3.74	4.19	1.73+1.39*C_L ns
t_r	A0 TO CO	0.618	1.14	1.19	1.33	0.444+1.16*C_L ns
t_f		0.721	1.33	1.39	1.56	0.443+1.85*C_L ns
t_r	A1 TO CO	0.441	0.815	0.850	0.953	0.361+0.534*C_L ns
t_f		0.730	1.35	1.40	1.58	0.452+1.85*C_L ns
t_r	A2 TO CO	0.451	0.832	0.868	0.973	0.371+0.532*C_L ns
t_f		0.725	1.34	1.40	1.57	0.448+1.85*C_L ns
t_r	A3 TO CO	0.446	0.824	0.859	0.964	0.366+0.533*C_L ns
t_f		0.734	1.36	1.41	1.59	0.457+1.84*C_L ns
t_r	B0 TO CO	0.617	1.14	1.19	1.33	0.443+1.16*C_L ns
t_f		0.720	1.33	1.39	1.55	0.442+1.85*C_L ns
t_r	B1 TO CO	0.612	1.13	1.18	1.32	0.437+1.16*C_L ns
t_f		0.719	1.33	1.38	1.55	0.442+1.85*C_L ns
t_r	B2 TO CO	0.619	1.14	1.19	1.34	0.445+1.16*C_L ns
t_f		0.722	1.33	1.39	1.56	0.445+1.84*C_L ns
t_r	B3 TO CO	0.615	1.14	1.18	1.33	0.440+1.16*C_L ns
t_f		0.700	1.29	1.35	1.51	0.420+1.87*C_L ns
t_r	CI TO CO	0.592	1.09	1.14	1.28	0.417+1.16*C_L ns
t_f		0.723	1.34	1.39	1.56	0.446+1.85*C_L ns
t_r	CI TO S0	1.55	2.86	2.99	3.35	0.844+4.71*C_L ns
t_f		1.25	2.31	2.41	2.70	0.904+2.31*C_L ns
t_r	CI TO S1	0.665	1.23	1.28	1.44	0.498+1.11*C_L ns
t_f		0.653	1.21	1.26	1.41	0.506+0.978*C_L ns

Switching characteristics (Sheet 2 of 3)

ADD4CS

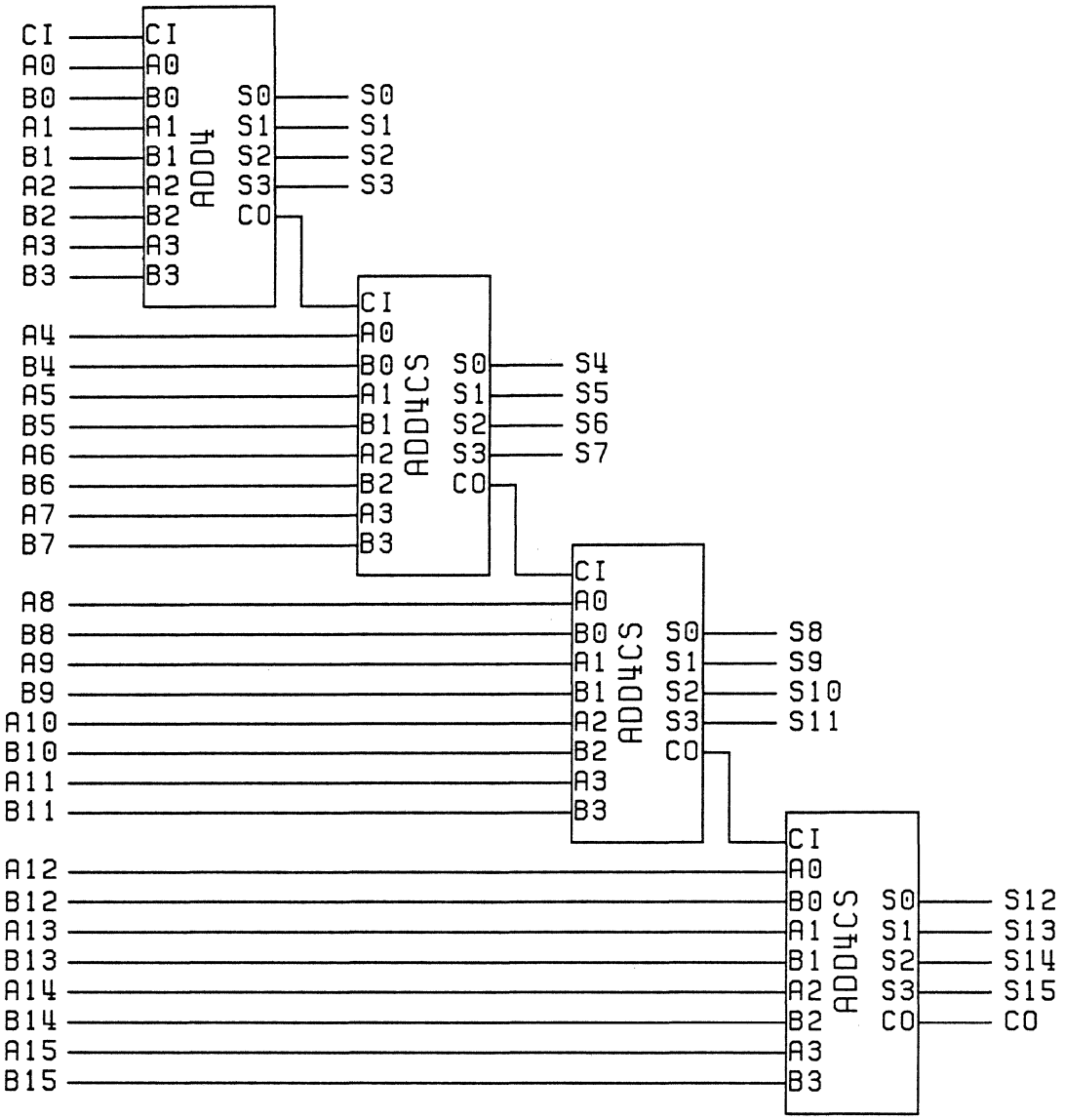
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_r	CI TO S2	0.665	1.23	1.28	1.44	0.498+1.11*C_L ns
t_f		0.653	1.21	1.26	1.41	0.506+0.978*C_L ns
t_r	CI TO S3	0.665	1.23	1.28	1.44	0.498+1.11*C_L ns
t_f		0.653	1.21	1.26	1.41	0.506+0.978*C_L ns
t_r	A0,B0 TO S0	1.45	2.68	2.80	3.14	0.733+4.79*C_L ns
t_f		0.877	1.62	1.69	1.89	0.459+2.79*C_L ns
t_r	A0,B0 TO S1	0.689	1.27	1.33	1.49	0.521+1.12*C_L ns
t_f		0.691	1.28	1.33	1.49	0.547+0.959*C_L ns
t_r	A0,B0 TO S2	0.707	1.31	1.36	1.53	0.543+1.10*C_L ns
t_f		0.690	1.28	1.33	1.49	0.547+0.953*C_L ns
t_r	A0,B0 TO S3	0.666	1.23	1.28	1.44	0.491+1.16*C_L ns
t_f		0.712	1.32	1.37	1.54	0.571+0.938*C_L ns
t_r	A1,B1 TO S1	1.45	2.68	2.80	3.14	0.733+4.79*C_L ns
t_f		0.877	1.62	1.69	1.89	0.459+2.79*C_L ns
t_r	A1,B1 TO S2	0.656	1.21	1.26	1.42	0.486+1.13*C_L ns
t_f		0.689	1.27	1.33	1.49	0.545+0.955*C_L ns
t_r	A1,B1 TO S3	0.666	1.23	1.28	1.44	0.494+1.15*C_L ns
t_f		0.656	1.21	1.26	1.42	0.506+1.000*C_L ns
t_r	A2,B2 TO S2	1.45	2.68	2.80	3.14	0.733+4.79*C_L ns
t_f		0.877	1.62	1.69	1.89	0.459+2.79*C_L ns
t_r	A2,B2 TO S3	0.702	1.30	1.35	1.52	0.533+1.12*C_L ns
t_f		0.671	1.24	1.29	1.45	0.523+0.986*C_L ns
t_r	A3,B3 TO S3	1.45	2.68	2.80	3.14	0.733+4.79*C_L ns
t_f		0.877	1.62	1.69	1.89	0.459+2.79*C_L ns

Switching characteristics (Sheet 3 of 3)

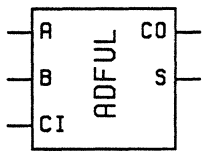
The ADD4 and ADD4CS standard cells offer the designer a performance or cell area choice. The ADD4 is a 4-bit ripple adder with a maximum propagation delay of 6ns under nominal conditions. The ADD4CS cell is optimized to provide carry-in to carry-out and sum times less than 2 and 3ns, respectively, for nominal conditions.

Cascading ADD4CS adders with the ADD4 (as shown in the following figure) allows for 16- and 32-bit nominal add times of less than 13 and 21ns, respectively. Speed may be traded off for cell area by using only ADD4 cells.



Full Adder

The ADFUL is a single-bit asynchronous adder with carry-in/carry-out function.



Inputs: A, B, CI
Outputs: CO, S
Input Cap.: All: 0.210 pF
Cell Size: 22 grids wide, 12 grids high

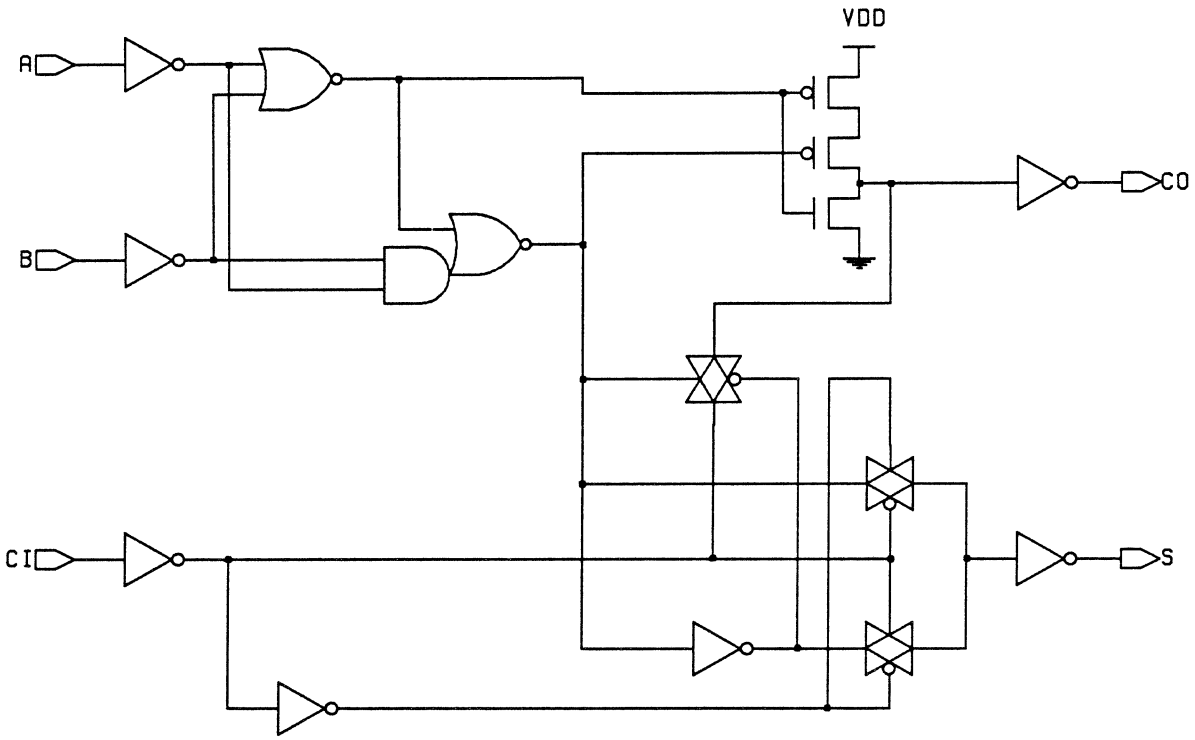
FUNCTION TABLE

A	B	CI	S	CO
L	L	L	L	L
L	H	L	H	L
H	L	L	H	L
H	H	L	L	H
L	L	H	H	L
L	H	H	L	H
H	L	H	L	H
H	H	H	H	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO CO	2.72	5.02	5.23	5.87	2.47+1.66*C_L ns
t_{PHL}		2.67	4.93	5.14	5.77	2.43+1.58*C_L ns
t_{PLH}	CI TO CO	2.40	4.43	4.62	5.19	2.15+1.66*C_L ns
t_{PHL}		2.45	4.53	4.72	5.30	2.21+1.59*C_L ns
t_{PLH}	*IN TO S	4.04	7.46	7.77	8.72	3.78+1.70*C_L ns
t_{PHL}		4.03	7.44	7.76	8.70	3.76+1.82*C_L ns
t_{PLH}	CI TO S	3.75	6.93	7.22	8.11	3.49+1.71*C_L ns
t_{PHL}		3.91	7.22	7.52	8.44	3.65+1.68*C_L ns
t_r	*IN TO CO	0.935	1.73	1.80	2.02	0.391+3.62*C_L ns
t_f		0.831	1.54	1.60	1.80	0.375+3.04*C_L ns
t_r	CI TO CO	0.940	1.74	1.81	2.03	0.396+3.62*C_L ns
t_f		0.805	1.49	1.55	1.74	0.345+3.06*C_L ns
t_r	*IN TO S	1.15	2.13	2.22	2.49	0.624+3.52*C_L ns
t_f		1.24	2.30	2.40	2.69	0.798+2.97*C_L ns
t_r	CI TO S	1.25	2.32	2.42	2.71	0.729+3.50*C_L ns
t_f		1.15	2.13	2.22	2.49	0.714+2.93*C_L ns
* Timing applies to either A or B input						

Switching characteristics



Functional diagram: ADFUL

2–Input AND Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.071 pF
Cell Size: 4 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.955	1.76	1.84	2.06	0.709+1.64*C_L ns
t_{PHL}		1.21	2.23	2.33	2.61	0.973+1.57*C_L ns
t_r	*IN TO X	0.882	1.63	1.70	1.91	0.336+3.64*C_L ns
t_f		0.790	1.46	1.52	1.71	0.332+3.05*C_L ns
* Slowest input						

Switching characteristics

3–Input AND Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.088 pF
Cell Size: 5 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.10	2.04	2.13	2.38	0.855+1.65*C_L ns
t_{PHL}		1.59	2.93	3.05	3.43	1.35+1.60*C_L ns
t_r	*IN TO X	0.919	1.70	1.77	1.98	0.375+3.62*C_L ns
t_f		0.912	1.68	1.76	1.97	0.463+2.99*C_L ns
* Slowest input						

Switching characteristics

4–Input AND Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.089
B, C: 0.088
D: 0.089 pF
Cell Size: 6 grids wide, 10 grids high

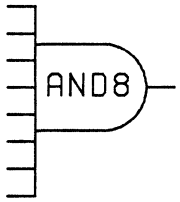
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.37	2.53	2.64	2.96	1.11+1.70*C_L ns
t_{PHL}		1.75	3.23	3.37	3.78	1.51+1.62*C_L ns
t_r	*IN TO X	0.998	1.84	1.92	2.15	0.459+3.59*C_L ns
t_f		0.969	1.79	1.87	2.09	0.521+2.98*C_L ns
* Slowest input						

Switching characteristics

8–Input AND Gate

Inputs: A, B, C, D, E, F, G, H
Outputs: X
Input Cap.: A: 0.072
B, C: 0.071
D, E: 0.072
F, G: 0.071
H: 0.072 pF
Cell Size: 13 grids wide, 10 grids high



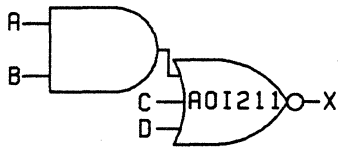
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.74	3.21	3.35	3.75	1.41+2.17*C_L ns
t_{PHL}		1.75	3.23	3.36	3.78	1.51+1.61*C_L ns
t_r	*IN TO X	1.39	2.56	2.67	3.00	0.676+4.74*C_L ns
t_f		1.20	2.22	2.31	2.59	0.753+2.98*C_L ns
* Slowest input						

Switching characteristics

2–1–1 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.089
B: 0.088
C, D: 0.072 pF
Cell Size: 5 grids wide, 10 grids high



$$X = \overline{(A \cdot B) + C + D}$$

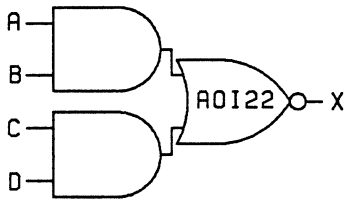
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.62	3.00	3.13	3.51	1.15+3.19*C_L ns
t_{PHL}		0.782	1.45	1.51	1.69	0.569+1.42*C_L ns
t_r	*IN TO X	2.58	4.76	4.97	5.57	1.51+7.14*C_L ns
t_f		1.32	2.43	2.54	2.84	0.899+2.78*C_L ns
* Slowest input						

Switching characteristics

2–2 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.089
B, C: 0.088
D: 0.089 pF
Cell Size: 5 grids wide, 10 grids high



$$X = \overline{(A \bullet B) + (C \bullet D)}$$

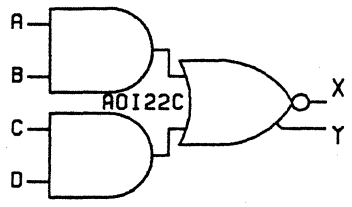
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.919	1.70	1.77	1.99	0.676+1.62*C_L ns
t_{PHL}		0.858	1.58	1.65	1.85	0.650+1.38*C_L ns
t_r	*IN TO X	1.43	2.64	2.75	3.09	0.890+3.60*C_L ns
t_f		1.26	2.33	2.43	2.73	0.847+2.77*C_L ns
* Slowest input						

Switching characteristics

2–2 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: A: 0.089
B, C: 0.088
D: 0.089 pF
Cell Size: 7 grids wide, 10 grids high



$$X = \overline{(A \cdot B) + (C \cdot D)}$$

$$Y = (A \cdot B) + (C \cdot D)$$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

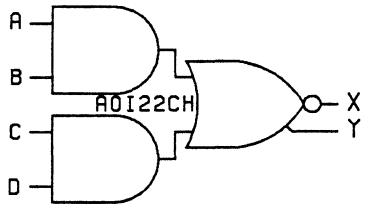
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.02	1.89	1.97	2.21	0.783+1.60*C_L ns
t_{PHL}		0.962	1.78	1.85	2.08	0.757+1.37*C_L ns
t_{PLH}	X TO Y	0.659	1.22	1.27	1.42	0.415+1.62*C_L ns
t_{PHL}		0.681	1.26	1.31	1.47	0.442+1.59*C_L ns
t_{PLH}	*IN TO Y	1.42	2.62	2.73	3.06	1.17+1.62*C_L ns
t_{PHL}		1.46	2.70	2.82	3.16	1.22+1.59*C_L ns
t_r	*IN TO X	1.75	3.24	3.38	3.79	1.22+3.55*C_L ns
t_f		1.56	2.89	3.01	3.38	1.16+2.70*C_L ns
t_r	X TO Y	1.12	2.06	2.15	2.41	0.592+3.49*C_L ns
t_f		1.07	1.97	2.06	2.31	0.635+2.89*C_L ns
t_r	*IN TO Y	1.12	2.06	2.15	2.41	0.592+3.49*C_L ns
t_f		1.07	1.97	2.06	2.31	0.635+2.89*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions see Calculating Standard Cell Timings application note.

2–2 AND–OR–Invert (High Drive) with Complementary Outputs

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: A: 0.158
B: 0.157
C, D: 0.159 pF
Cell Size: 13 grids wide, 10 grids high



$X = \overline{(A \cdot B) + (C \cdot D)}$

$Y = (A \cdot B) + (C \cdot D)$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.849	1.57	1.63	1.83	0.728+0.803*C_L ns
t_{PHL}		1.04	1.91	1.99	2.24	0.897+0.918*C_L ns
t_{PLH}	X TO Y	0.408	0.754	0.786	0.881	0.316+0.616*C_L ns
t_{PHL}		0.389	0.719	0.750	0.841	0.296+0.622*C_L ns
t_{PLH}	*IN TO Y	1.31	2.41	2.51	2.82	1.21+0.616*C_L ns
t_{PHL}		1.12	2.06	2.15	2.41	1.02+0.622*C_L ns
t_r	*IN TO X	1.46	2.70	2.81	3.16	1.20+1.75*C_L ns
t_f		1.58	2.92	3.05	3.42	1.30+1.86*C_L ns
t_r	X TO Y	0.639	1.18	1.23	1.38	0.468+1.14*C_L ns
t_f		0.560	1.03	1.08	1.21	0.414+0.971*C_L ns
t_r	*IN TO Y	0.639	1.18	1.23	1.38	0.468+1.14*C_L ns
t_f		0.560	1.03	1.08	1.21	0.414+0.971*C_L ns
* Slowest input						

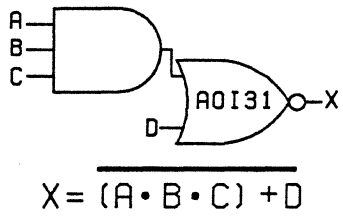
Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions see Calculating Standard Cell Timings application note.

AOI31

3–1 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.089
B, C: 0.088
D: 0.072 pF
Cell Size: 5 grids wide, 10 grids high



$$X = \overline{(A \cdot B \cdot C) + D}$$

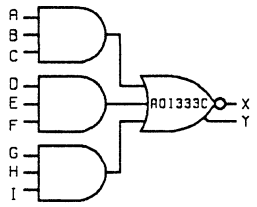
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.13	2.09	2.18	2.44	0.810+2.14*C_L ns
t_{PHL}		0.943	1.74	1.81	2.04	0.649+1.96*C_L ns
t_r	*IN TO X	2.07	3.82	3.98	4.47	1.35+4.77*C_L ns
t_f		1.34	2.48	2.58	2.90	0.726+4.10*C_L ns
* Slowest input						

Switching characteristics

3–3–3 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H, I
Outputs: X, Y
Input Cap.: A: 0.105
B: 0.106
C, D: 0.105
E: 0.106
F, G: 0.105
H: 0.106
I: 0.105 pF
Cell Size: 18 grids wide, 11 grids high



$X = \overline{(A \cdot B \cdot C) + (D \cdot E \cdot F) + (G \cdot H \cdot I)}$

$Y = (A \cdot B \cdot C) + (D \cdot E \cdot F) + (G \cdot H \cdot I)$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	Y TO X	0.406	0.749	0.781	0.876	0.160+1.64*C_L ns
t_{PHL}		0.442	0.817	0.852	0.956	0.208+1.56*C_L ns
t_{PLH}	*IN TO Y	3.60	6.64	6.92	7.77	3.31+1.87*C_L ns
t_{PHL}		3.06	5.66	5.90	6.61	2.78+1.86*C_L ns
t_{PLH}	*IN TO X	3.19	5.89	6.14	6.89	2.94+1.64*C_L ns
t_{PHL}		3.76	6.94	7.24	8.12	3.52+1.56*C_L ns
t_r	Y TO X	0.930	1.72	1.79	2.01	0.388+3.61*C_L ns
t_f		0.849	1.57	1.63	1.83	0.397+3.01*C_L ns
t_r	*IN TO Y	1.99	3.68	3.84	4.31	1.49+3.35*C_L ns
t_f		1.69	3.12	3.25	3.65	1.25+2.92*C_L ns
t_r	*IN TO X	0.930	1.72	1.79	2.01	0.388+3.61*C_L ns
t_f		0.849	1.57	1.63	1.83	0.397+3.01*C_L ns
* Slowest input						

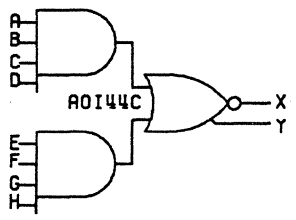
Switching characteristics

NOTE:
The propagation delay for X is dependent upon the Y output delay. The delays listed for "IN TO X" and delay equation for X assume no load on the Y output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

AOI44C

4–4 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H
Outputs: X, Y
Input Cap.: All: 0.054 pF
Cell Size: 22 grids wide, 10 grids high



$$X = \overline{(A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)}$$

$$Y = (A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)$$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

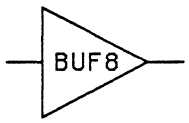
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	2.05	3.78	3.94	4.42	1.57+3.19*C_L ns
t_{PHL}		2.36	4.35	4.54	5.09	2.11+1.64*C_L ns
t_{PLH}	*IN TO Y	2.70	4.98	5.19	5.82	2.45+1.65*C_L ns
t_{PHL}		2.42	4.47	4.66	5.23	2.18+1.61*C_L ns
t_r	*IN TO X	1.73	3.19	3.33	3.73	0.654+7.15*C_L ns
t_f		1.21	2.23	2.33	2.61	0.766+2.94*C_L ns
t_r	*IN TO Y	0.916	1.69	1.76	1.98	0.372+3.62*C_L ns
t_f		0.909	1.68	1.75	1.96	0.457+3.01*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The Y output delay is not dependent upon the X output delay for this cell.

Noninverting Buffer (8X Drive)

BUF8 has 8 times the drive of an SBUF.



Inputs: A
Outputs: X
Input Cap.: A: 0.106 pF
Cell Size: 6 grids wide, 11 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

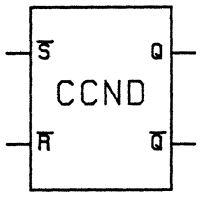
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.955	1.76	1.84	2.06	0.916+0.259*C_L ns
t_{PHL}		1.07	1.98	2.06	2.31	1.03+0.262*C_L ns
t_r	A TO X	0.456	0.842	0.878	0.985	0.394+0.414*C_L ns
t_f		0.501	0.925	0.964	1.08	0.449+0.344*C_L ns

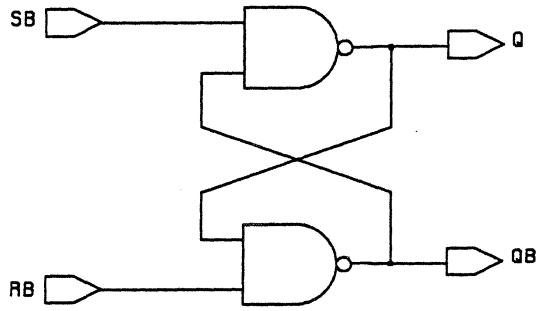
Switching characteristics

Cross–Coupled NAND Latch

CCND is very sensitive to negative spikes on SB or RB.

Inputs: SB, RB
Outputs: Q, QB
Input Cap.: All: 0.072 pF
Cell Size: 5 grids wide, 10 grids high





Functional diagram: CCND

FUNCTION TABLE

SB	RB	Q	QB
L	L	*	*
L	H	H	L
H	L	L	H
H	H	Q_o	QB_o

* Both outputs will remain high as long as SB and RB remain low, but the output states are unpredictable if SB and RB go high simultaneously.

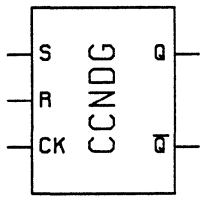
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	SB TO Q	0.805	1.49	1.55	1.74	0.557+1.65*C_L ns
t_{PHL}		0.668	1.23	1.29	1.44	0.464+1.35*C_L ns
t_{PLH}	SB TO QB	0.805	1.49	1.55	1.74	0.557+1.65*C_L ns
t_{PHL}		1.52	2.80	2.92	3.28	1.000+3.43*C_L ns
t_{PLH}	RB TO Q	0.816	1.51	1.57	1.76	0.569+1.65*C_L ns
t_{PHL}		1.53	2.83	2.95	3.31	1.02+3.43*C_L ns
t_{PLH}	RB TO QB	0.816	1.51	1.57	1.76	0.569+1.65*C_L ns
t_{PHL}		0.667	1.23	1.28	1.44	0.463+1.35*C_L ns
t_r	SB TO Q	1.29	2.39	2.49	2.79	0.744+3.64*C_L ns
t_f		1.05	1.95	2.03	2.28	0.639+2.77*C_L ns
t_r	SB TO QB	1.29	2.39	2.49	2.79	0.744+3.64*C_L ns
t_f		1.12	2.08	2.16	2.43	0.639+3.23*C_L ns
t_r	RB TO Q	1.26	2.33	2.43	2.72	0.755+3.37*C_L ns
t_f		1.11	2.05	2.14	2.40	0.626+3.23*C_L ns
t_r	RB TO QB	1.26	2.33	2.43	2.72	0.755+3.37*C_L ns
t_f		1.07	1.97	2.05	2.30	0.651+2.77*C_L ns

Switching characteristics

Gated R/S Flip–Flop

CCNDG is very sensitive to positive spikes on S and R while CK is high.



Inputs: S, CK, R
Outputs: Q, QB
Input Cap.: S: 0.055
CK: 0.108
R: 0.055 pF
Cell Size: 10 grids wide, 10 grids high

FUNCTION TABLE

CK	S	R	Q	QB
L	X	X	Q_o	QB_o
H	L	L	Q_o	QB_o
H	L	H	L	H
H	H	L	H	L
H	H	H	*	*

* Both outputs will remain high as long as S, R, and CK are high, but the output states are unpredictable if S and R go low simultaneously or if CK goes low while S and R are still high.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	S TO Q	1.31	2.42	2.52	2.83	1.06+1.66*C_L ns
t_{PHL}		1.41	2.61	2.72	3.05	0.999+2.76*C_L ns
t_{PHL}	S TO QB	2.39	4.42	4.60	5.16	1.64+4.97*C_L ns
t_{PLH}	CK TO Q	1.30	2.40	2.50	2.81	1.05+1.66*C_L ns
t_{PHL}		2.37	4.38	4.57	5.12	1.63+4.97*C_L ns
t_{PLH}	CK TO QB	1.31	2.43	2.53	2.84	1.07+1.64*C_L ns
t_{PHL}		2.38	4.40	4.58	5.14	1.63+4.97*C_L ns
t_{PHL}	R TO Q	2.39	4.42	4.60	5.16	1.64+4.97*C_L ns
t_{PLH}	R TO QB	1.31	2.42	2.52	2.83	1.06+1.66*C_L ns
t_{PHL}		1.41	2.61	2.72	3.05	0.999+2.76*C_L ns
t_r	S TO Q	1.18	2.19	2.28	2.56	0.640+3.63*C_L ns
t_f		1.67	3.08	3.21	3.61	0.816+5.69*C_L ns
t_f	S TO QB	1.72	3.17	3.31	3.71	0.820+5.98*C_L ns
t_r	CK TO Q	1.21	2.24	2.33	2.62	0.674+3.57*C_L ns
t_f		1.72	3.17	3.30	3.71	0.817+5.99*C_L ns
t_r	CK TO QB	1.22	2.25	2.35	2.64	0.685+3.57*C_L ns
t_f		1.72	3.17	3.30	3.71	0.818+5.98*C_L ns
t_f	R TO Q	1.72	3.17	3.31	3.71	0.820+5.98*C_L ns
t_r	R TO QB	1.18	2.19	2.28	2.56	0.640+3.63*C_L ns
t_f		1.67	3.08	3.21	3.61	0.816+5.69*C_L ns

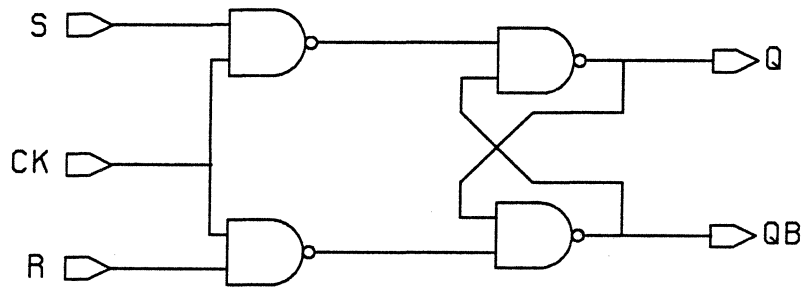
Switching characteristics

CCNDG

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	S to CK	3.00	ns
t_{su}	R to CK	3.00	ns
t_h	CK to S	3.00	ns
t_h	CK to R	3.00	ns
t_{pwh}	High CK Pulse Width	5.00	ns

Timing requirements

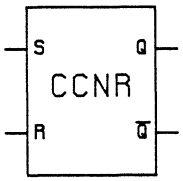


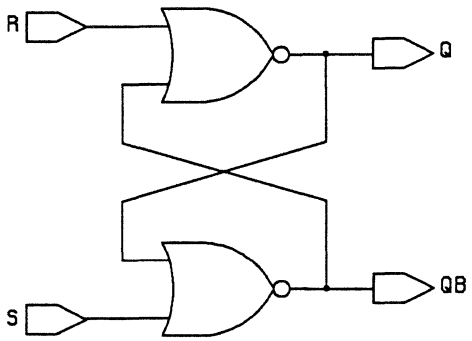
Functional diagram: CCNDG

Cross–Coupled NOR Latch

CCNR is very sensitive to positive spikes on S and R.

Inputs: S, R
Outputs: Q, QB
Input Cap.: All: 0.055 pF
Cell Size: 5 grids wide, 10 grids high





Functional diagram: CCNR

FUNCTION TABLE

S	R	Q	QB
L	L	Q_o	QB_o
L	H	L	H
H	L	H	L
H	H	*	*

* Both outputs will remain low as long as S and R are high, but the output states are unpredictable if S and R go low simultaneously

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

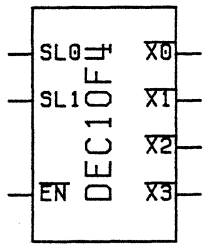
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	S TO Q	1.92	3.54	3.69	4.14	1.14+5.17*C_L ns
t_{PHL}		0.721	1.33	1.39	1.56	0.487+1.56*C_L ns
t_{PLH}	S TO QB	1.19	2.19	2.29	2.57	0.709+3.19*C_L ns
t_{PHL}		0.721	1.33	1.39	1.56	0.487+1.56*C_L ns
t_{PLH}	R TO Q	1.13	2.08	2.17	2.43	0.648+3.19*C_L ns
t_{PHL}		0.704	1.30	1.36	1.52	0.470+1.56*C_L ns
t_{PLH}	R TO QB	1.96	3.62	3.78	4.24	1.19+5.16*C_L ns
t_{PHL}		0.704	1.30	1.36	1.52	0.470+1.56*C_L ns
t_r	S TO Q	2.22	4.10	4.27	4.79	1.11+7.36*C_L ns
t_f		1.01	1.87	1.95	2.19	0.552+3.07*C_L ns
t_r	S TO QB	2.28	4.20	4.38	4.92	1.20+7.19*C_L ns
t_f		1.01	1.87	1.95	2.19	0.552+3.07*C_L ns
t_r	R TO Q	2.18	4.03	4.20	4.72	1.10+7.19*C_L ns
t_f		0.967	1.79	1.86	2.09	0.507+3.07*C_L ns
t_r	R TO QB	2.31	4.26	4.44	4.98	1.20+7.36*C_L ns
t_f		0.967	1.79	1.86	2.09	0.507+3.07*C_L ns

Switching characteristics

DEC1OF4

1–of–4 Decoder

Inputs: SL0, SL1, ENB
Outputs: X0B, X1B, X2B, X3B
Input Cap.: SL0, SL1: 0.200
ENB: 0.055 pF
Cell Size: 25 grids wide, 12 grids high



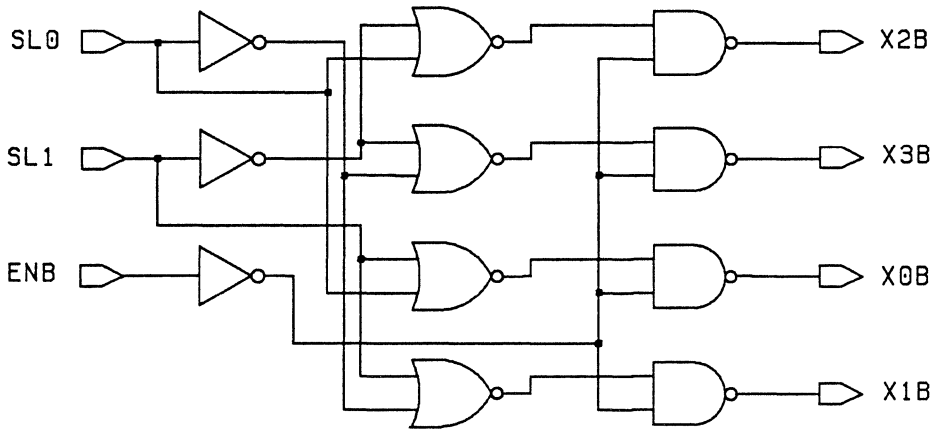
FUNCTION TABLE

SL0	SL1	ENB	X0B	X1B	X2B	X3B
X	X	H	H	H	H	H
L	L	L	L	H	H	H
H	L	L	H	L	H	H
L	H	L	H	H	L	H
H	H	L	H	H	H	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*SL TO XnB	1.80	3.32	3.46	3.88	1.63+1.12*C_L ns
t_{PHL}		2.33	4.31	4.49	5.04	1.92+2.77*C_L ns
t_{PLH}	*ENB TO XnB	1.43	2.64	2.75	3.09	1.26+1.15*C_L ns
t_{PHL}		1.95	3.60	3.76	4.21	1.53+2.78*C_L ns
t_r	*SL TO XnB	0.776	1.43	1.49	1.68	0.420+2.37*C_L ns
t_f		1.51	2.79	2.91	3.26	0.668+5.61*C_L ns
t_r	*ENB TO XnB	0.963	1.78	1.85	2.08	0.615+2.32*C_L ns
t_f		1.53	2.83	2.95	3.30	0.689+5.60*C_L ns
* SL timing applies to both SL0 and SL1. XnB represents any output.						

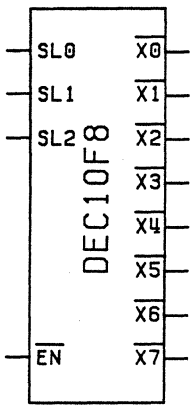
Switching characteristics


SL0
SL1
ENB
X2B
X3B
X0B
X1B

DEC1OF8

1–of–8 Decoder

Inputs: SL0, SL1, SL2, ENB
Outputs: X0B, X1B, X2B, X3B, X4B, X5B, X6B, X7B
Input Cap.: All: 0.055 pF
Cell Size: 48 grids wide, 14 grids high



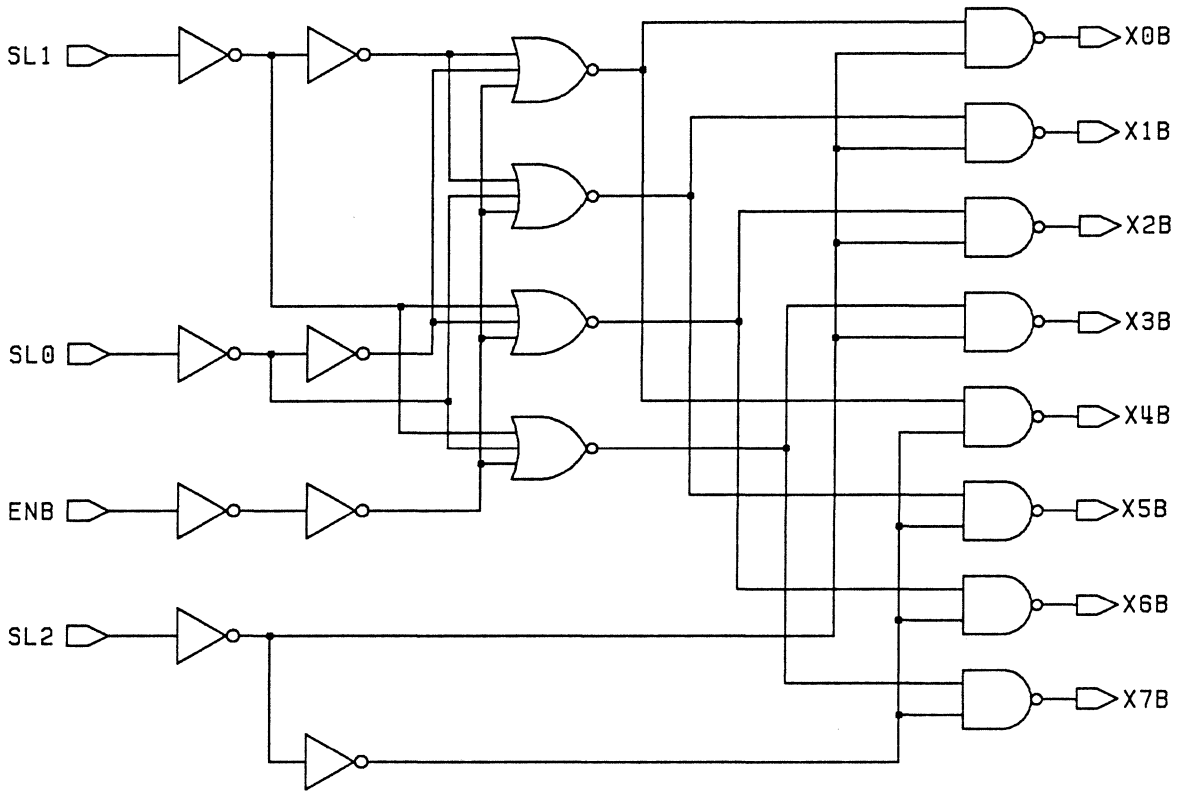
FUNCTION TABLE

SL0	SL1	SL2	ENB	X0B	X1B	X2B	X3B	X4B	X5B	X6B	X7B
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*ENB TO XnB	2.97	5.49	5.72	6.42	2.72+1.67*C_L ns
t_{PHL}		3.44	6.36	6.63	7.44	3.02+2.79*C_L ns
t_{PLH}	*SL2 TO XnB	3.25	6.00	6.25	7.02	2.99+1.69*C_L ns
t_{PHL}		3.39	6.26	6.52	7.32	2.96+2.81*C_L ns
t_r	*ENB TO XnB	1.00	1.85	1.93	2.16	0.462+3.58*C_L ns
t_f		1.55	2.86	2.98	3.34	0.715+5.55*C_L ns
t_r	*SL2 TO XnB	1.09	2.01	2.09	2.35	0.555+3.55*C_L ns
t_f		1.55	2.86	2.98	3.35	0.716+5.55*C_L ns
* ENB timing applies to SL0, SL1 and ENB. XnB represents any output.						

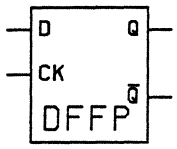
Switching characteristics



Functional diagram: DEC1OF8

D Flip–Flop, Positive Edge Triggered

DFFP is a fully static D-type flip-flop. It is positive edge triggered with respect to the single phase clock input (CK). For a faster version of this cell, see DFFPF.



Inputs: D, CK
Outputs: Q, QB
Input Cap.: D: 0.039
CK: 0.055 pF
Cell Size: 17 grids wide, 11 grids high

FUNCTION TABLE

D	CK	Q	QB
L	↑	L	H
H	↑	H	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

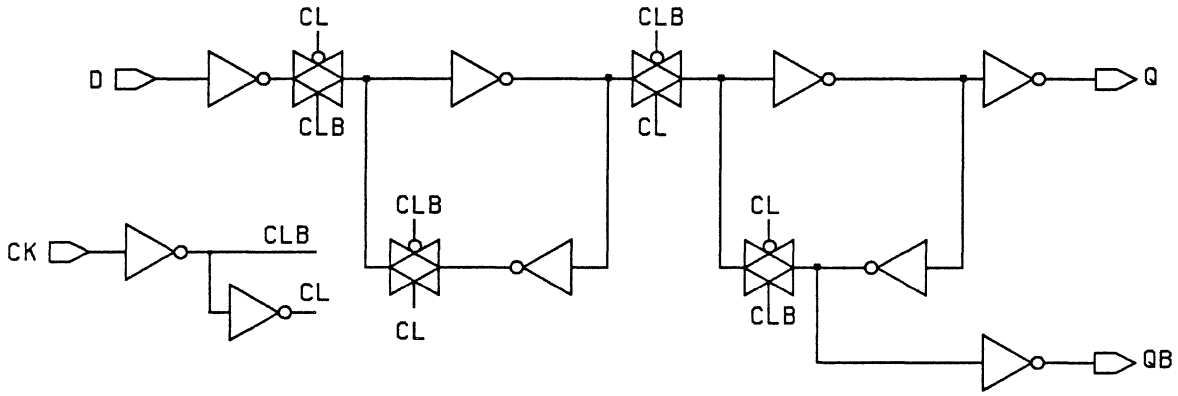
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	2.65	4.90	5.11	5.73	2.52+0.856*C_L ns
t_{PHL}		2.54	4.69	4.89	5.49	2.41+0.839*C_L ns
t_{PLH}	CK TO QB	3.14	5.80	6.04	6.78	3.01+0.812*C_L ns
t_{PHL}		3.30	6.10	6.36	7.14	3.18+0.793*C_L ns
t_r	CK TO Q	0.754	1.39	1.45	1.63	0.493+1.74*C_L ns
t_f		0.678	1.25	1.31	1.46	0.460+1.45*C_L ns
t_r	CK TO QB	0.702	1.30	1.35	1.52	0.441+1.74*C_L ns
t_f		0.638	1.18	1.23	1.38	0.419+1.46*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	2.00	ns
t_h	Hold Time CK to D	−0.75	ns
t_{pwh}	High CK Pulse Width	4.75	ns
t_{pwl}	Low CK Pulse Width	4.75	ns

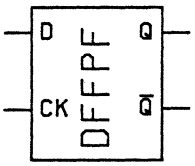
Timing requirements



Functional diagram: DFFP

Fast D Flip–Flop, Positive Edge Triggered

DFFPF is a fully static D–type flip–flop. It is positive edge triggered with respect to the single phase clock input (CK).



Inputs: D, CK
Outputs: Q, QB
Input Cap.: D: 0.083
CK: 0.205 pF
Cell Size: 13 grids wide, 13 grids high

FUNCTION TABLE

D	CK	Q	QB
L	↑	L	H
H	↑	H	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

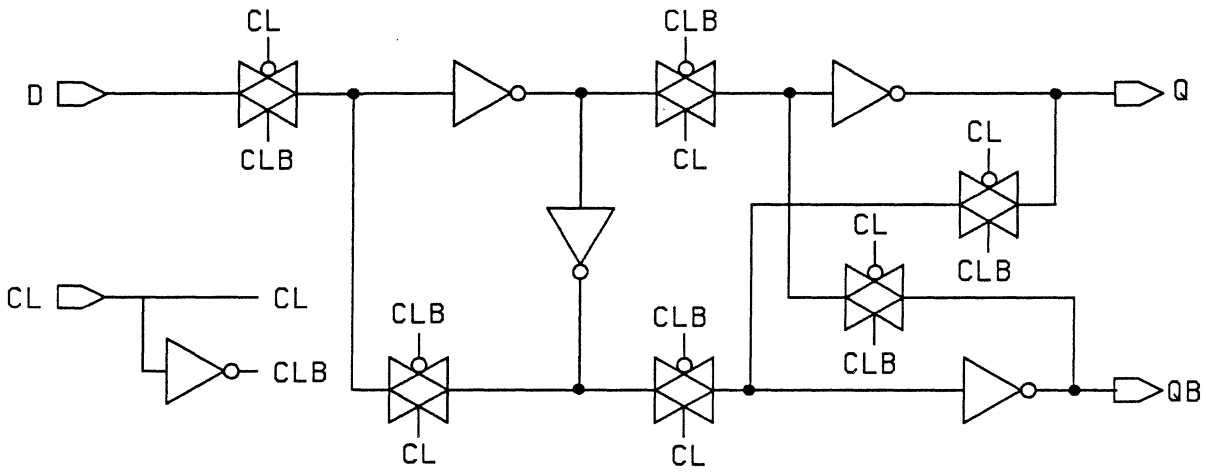
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	0.863	1.59	1.66	1.86	0.650+1.41*C_L ns
t_{PHL}		1.35	2.49	2.60	2.91	1.12+1.53*C_L ns
t_{PLH}	CK TO QB	0.880	1.63	1.69	1.90	0.670+1.40*C_L ns
t_{PHL}		1.35	2.49	2.59	2.91	1.12+1.53*C_L ns
t_r	CK TO Q	0.840	1.55	1.62	1.81	0.376+3.09*C_L ns
t_f		0.924	1.71	1.78	2.00	0.507+2.78*C_L ns
t_r	CK TO QB	0.867	1.60	1.67	1.87	0.407+3.06*C_L ns
t_f		0.951	1.76	1.83	2.05	0.536+2.77*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.25	ns
t_h	Hold Time CK to D	0.00	ns
t_{pwh}	High CK Pulse Width	3.75	ns
t_{pwl}	Low CK Pulse Width	3.75	ns

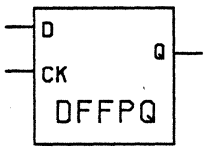
Timing requirements



Functional diagram: DFFPF

D Flip–Flop, Positive Edge Triggered

DFFPQ is a fully static D-type flip-flop with only a Q output. It is positive edge triggered with respect to the single phase clock input (CK).



Inputs: D, CK
Outputs: Q
Input Cap.: D: 0.038
CK: 0.145 pF
Cell Size: 10 grids wide, 10 grids high

FUNCTION TABLE

D	CK	Q
L	↑	L
H	↑	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

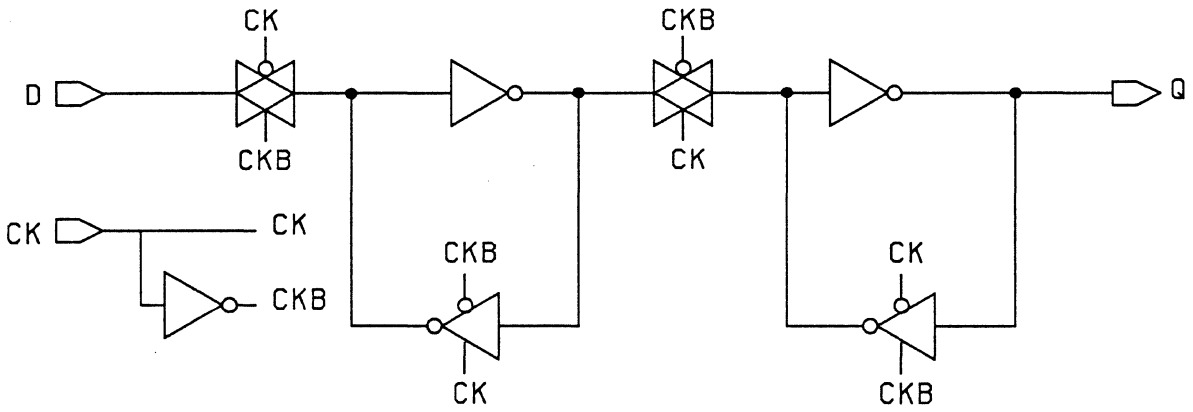
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	0.806	1.49	1.55	1.74	0.663+0.952*C_L ns
t_{PHL}		1.09	2.01	2.10	2.36	0.942+0.987*C_L ns
t_r	CK TO Q	0.679	1.25	1.31	1.47	0.386+1.95*C_L ns
t_f		0.717	1.32	1.38	1.55	0.475+1.61*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.50	ns
t_h	Hold Time CK to D	−0.50	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwl}	Low CK Pulse Width	4.25	ns

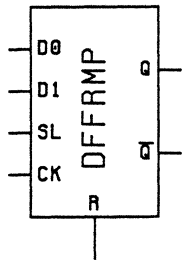
Timing requirements



Functional diagram: DFFPQ

D Flip–Flop with Reset and Multiplexed Inputs, Positive Edge Triggered

DFFRMP is a fully static D-type edge triggered flip-flop with a multiplexed D input. Selection of D0 or D1 is controlled by SL. It is positive edge triggered with respect to the single clock input CK. R is asynchronous and active high.



Inputs: R, D0, D1, SL, CK
Outputs: Q, QB
Input Cap.: R, D0, D1, SL: 0.056
CK: 0.055 pF
Cell Size: 29 grids wide, 12 grids high

FUNCTION TABLE

D0	D1	SL	R	CK	Q	QB
X	X	X	H	X	L	H
H	X	H	L	↑	H	L
L	X	H	L	↑	L	H
X	H	L	L	↑	H	L
X	L	L	L	↑	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

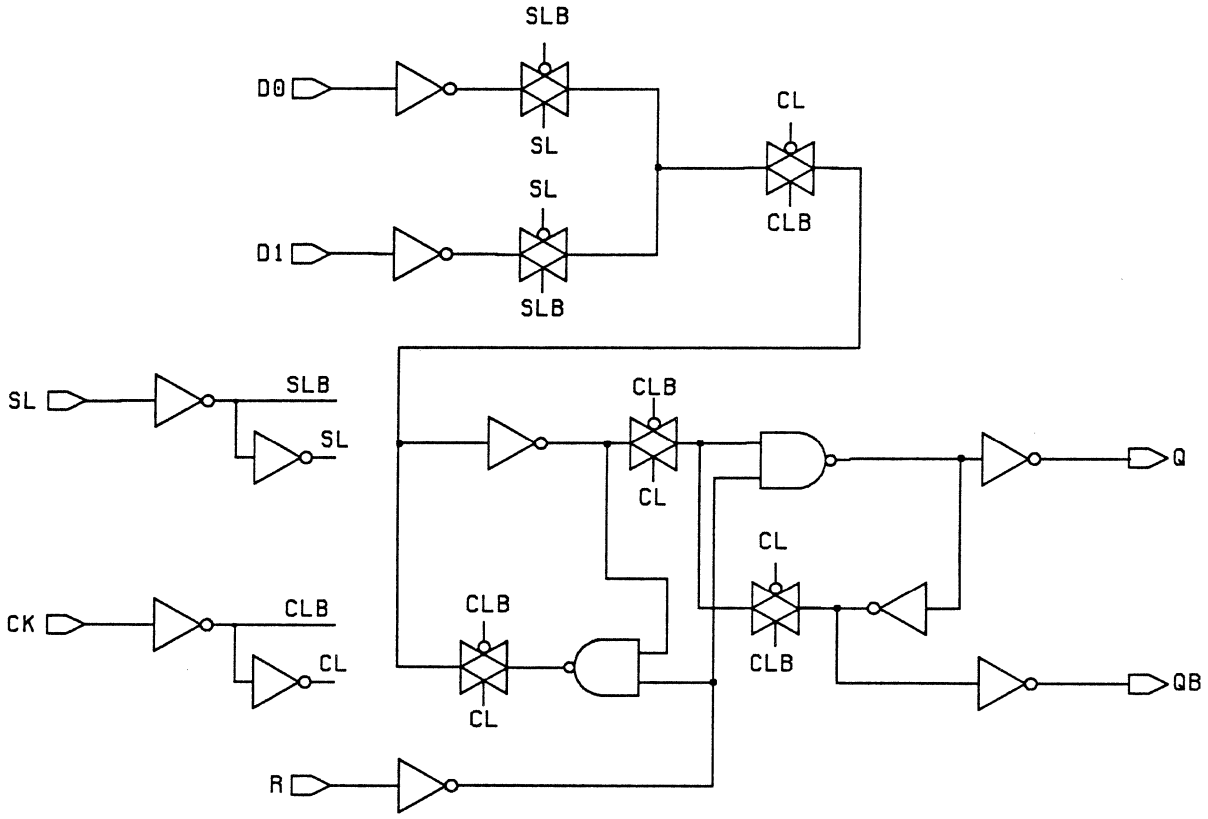
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	R TO Q	1.98	3.66	3.82	4.29	1.74+1.64*C_L ns
t_{PLH}	R TO QB	3.29	6.08	6.34	7.11	3.04+1.66*C_L ns
t_{PLH}	CK TO Q	3.60	6.66	6.94	7.79	3.35+1.69*C_L ns
t_{PHL}		3.31	6.12	6.37	7.15	3.07+1.57*C_L ns
t_{PLH}	CK TO QB	2.58	4.77	4.97	5.58	2.34+1.65*C_L ns
t_{PHL}		2.65	4.89	5.10	5.72	2.41+1.60*C_L ns
t_f	R TO Q	0.952	1.76	1.83	2.06	0.504+2.99*C_L ns
t_r	R TO QB	0.949	1.75	1.83	2.05	0.409+3.60*C_L ns
t_r	CK TO Q	1.06	1.95	2.04	2.28	0.521+3.57*C_L ns
t_f		0.856	1.58	1.65	1.85	0.403+3.01*C_L ns
t_r	CK TO QB	0.967	1.79	1.86	2.09	0.428+3.59*C_L ns
t_f		0.839	1.55	1.62	1.81	0.384+3.03*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D0 to CK	3.00	ns
t_{su}	Setup Time D1 to CK	3.00	ns
t_{su}	Setup Time SL to CK	4.00	ns
t_h	Hold Time CK to D0	−2.00	ns
t_h	Hold Time CK to D1	−2.00	ns
t_h	Hold Time CK to SL	−3.00	ns
t_{pwh}	R Pulse Width (high)	4.75	ns
t_{pwh}	High CK Pulse Width	4.50	ns
t_{pwl}	Low CK Pulse Width	4.75	ns
rt	R Recovery Time	−0.50	ns

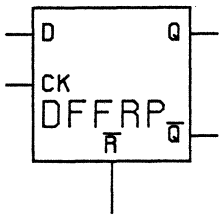
Timing requirements



Functional diagram: DFFRMP

D Flip–Flop with Reset, Positive Edge Triggered

DFFRP is a fully static D-type edge triggered flip-flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low. For a faster version of this cell, see DFFRPF.



Inputs: RB, D, CK
Outputs: Q, QB
Input Cap.: RB: 0.143
D: 0.038
CK: 0.054 pF
Cell Size: 20 grids wide, 12 grids high

FUNCTION TABLE

D	CK	RB	Q	QB
L	↑	H	L	H
H	↑	H	H	L
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

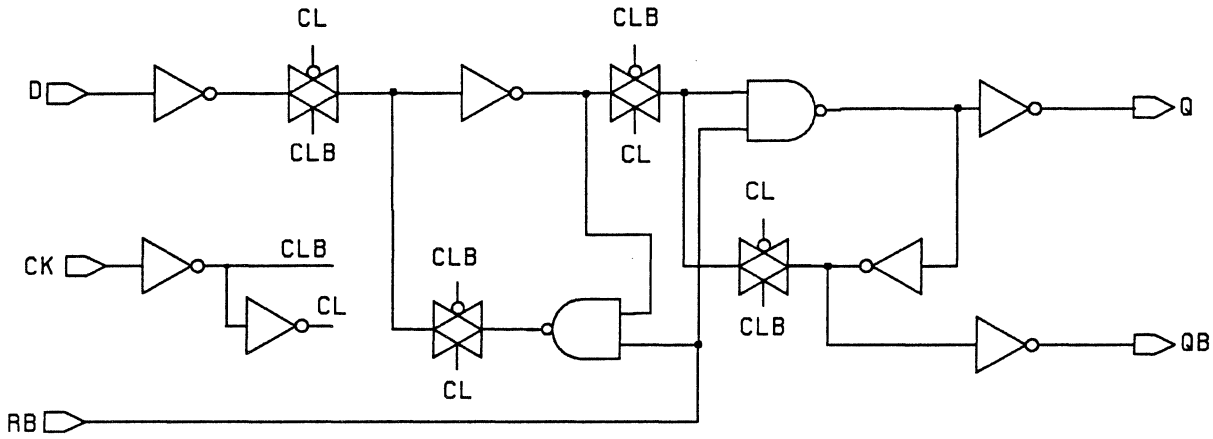
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	2.56	4.73	4.93	5.54	2.43+0.858*C_L ns
t_{PHL}		2.56	4.73	4.93	5.54	2.44+0.830*C_L ns
t_{PLH}	CK TO QB	3.08	5.70	5.94	6.66	2.96+0.815*C_L ns
t_{PHL}		3.71	6.85	7.14	8.01	3.58+0.845*C_L ns
t_{PHL}	RB TO Q	1.27	2.35	2.45	2.75	1.14+0.859*C_L ns
t_{PLH}	RB TO QB	2.17	4.00	4.17	4.68	2.03+0.891*C_L ns
t_r	CK TO Q	0.718	1.33	1.38	1.55	0.455+1.75*C_L ns
t_f		0.656	1.21	1.26	1.42	0.437+1.46*C_L ns
t_r	CK TO QB	0.686	1.27	1.32	1.48	0.424+1.75*C_L ns
t_f		0.817	1.51	1.57	1.77	0.603+1.43*C_L ns
t_f	RB TO Q	0.690	1.27	1.33	1.49	0.472+1.45*C_L ns
t_r	RB TO QB	0.804	1.48	1.55	1.74	0.541+1.75*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.50	ns
t_h	Hold Time CK to D	-0.75	ns
t_{pwh}	High CK Pulse Width	4.25	ns
t_{pwl}	RB Pulse Width (low)	4.50	ns
t_{pwl}	Low CK Pulse Width	4.50	ns
rt	RB Recovery Time	-2.00	ns

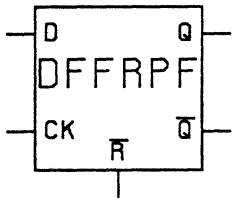
Timing requirements



Functional diagram: DFFRP

Fast D Flip–Flop with Reset, Positive Edge Triggered

DFFRPF is a fully static D-type edge triggered flip-flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low.



Inputs: RB, D, CK
Outputs: Q, QB
Input Cap.: RB: 0.251
D: 0.115
CK: 0.200 pF
Cell Size: 18 grids wide, 14 grids high

FUNCTION TABLE

D	CK	RB	Q	QB
L	↑	H	L	H
H	↑	H	H	L
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

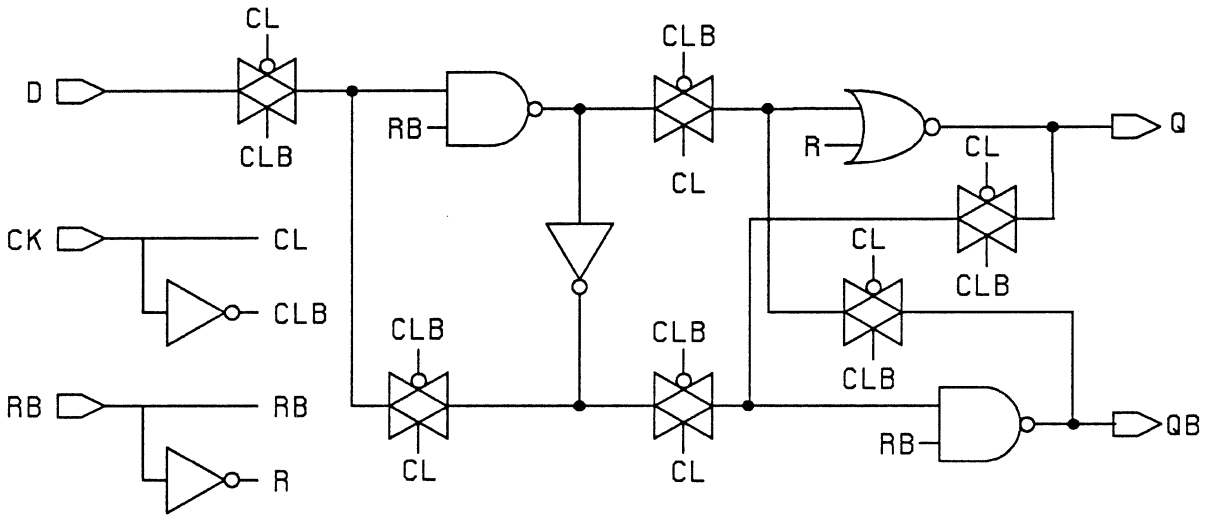
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.04	1.91	1.99	2.24	0.831+1.36*C_L ns
t_{PHL}		1.78	3.29	3.43	3.85	1.55+1.55*C_L ns
t_{PLH}	CK TO QB	1.07	1.98	2.07	2.32	0.859+1.43*C_L ns
t_{PHL}		1.37	2.53	2.64	2.96	1.17+1.36*C_L ns
t_{PHL}	RB TO Q	1.45	2.69	2.80	3.14	1.23+1.52*C_L ns
t_{PLH}	RB TO QB	0.793	1.47	1.53	1.71	0.561+1.55*C_L ns
t_r	CK TO Q	1.16	2.15	2.24	2.51	0.713+3.00*C_L ns
t_f		1.22	2.25	2.35	2.63	0.803+2.77*C_L ns
t_r	CK TO QB	0.996	1.84	1.92	2.15	0.530+3.10*C_L ns
t_f		1.02	1.89	1.97	2.21	0.640+2.55*C_L ns
t_f	RB TO Q	1.45	2.69	2.80	3.14	1.09+2.44*C_L ns
t_r	RB TO QB	1.78	3.28	3.42	3.84	1.40+2.51*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.25	ns
t_h	Hold Time CK to D	-0.25	ns
t_{pwh}	High CK Pulse Width	3.75	ns
t_{pwl}	RB Pulse Width (low)	5.50	ns
t_{pwl}	Low CK Pulse Width	3.75	ns
rt	RB Recovery Time	0.50	ns

Timing requirements

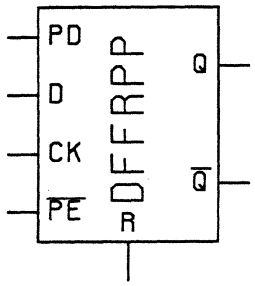


Functional diagram: DFFRPF

DFFRPP

D Flip–Flop with Reset and Parallel Data Input, Positive Edge Triggered

DFFRPP is a D–type, positive edge triggered flip–flop with parallel load, and single clock input. Parallel data from PD is transparent when PEB is low. R is asynchronous and active high.



Inputs: R, D, PD, PEB, CK
Outputs: Q, QB
Input Cap.: R: 0.056
D, PD, PEB, CK: 0.055 pF
Cell Size: 29 grids wide, 12 grids high

FUNCTION TABLE

R	D	PD	PEB	CK	Q	QB
H	X	X	X	X	L	H
L	X	H	L	X	H	L
L	X	L	L	X	L	H
L	H	X	H	↑	H	L
L	L	X	H	↑	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	R TO Q	2.11	3.90	4.07	4.56	1.97+0.944*C_L ns
t_{PHL}		1.74	3.21	3.35	3.76	1.61+0.859*C_L ns
t_{PLH}	R TO QB	2.64	4.88	5.08	5.70	2.51+0.873*C_L ns
t_{PHL}		2.81	5.18	5.40	6.06	2.69+0.797*C_L ns
t_{PLH}	CK TO Q	3.00	5.55	5.78	6.49	2.86+0.952*C_L ns
t_{PHL}		2.53	4.67	4.87	5.46	2.40+0.840*C_L ns
t_{PLH}	CK TO QB	3.14	5.80	6.05	6.79	3.02+0.810*C_L ns
t_{PHL}		3.69	6.82	7.11	7.98	3.57+0.809*C_L ns
t_{PLH}	PD TO Q	3.59	6.64	6.92	7.76	3.45+0.956*C_L ns
t_{PHL}		3.30	6.10	6.36	7.14	3.17+0.853*C_L ns
t_{PLH}	PD TO QB	3.92	7.24	7.55	8.47	3.80+0.822*C_L ns
t_{PHL}		4.29	7.92	8.26	9.26	4.17+0.807*C_L ns
t_{PLH}	PEB TO Q	4.17	7.70	8.02	9.00	4.02+0.956*C_L ns
t_{PHL}		3.34	6.17	6.43	7.21	3.21+0.850*C_L ns
t_{PLH}	PEB TO QB	3.95	7.30	7.61	8.53	3.83+0.824*C_L ns
t_{PHL}		4.86	8.98	9.36	10.5	4.74+0.807*C_L ns
t_r	R TO Q	0.889	1.64	1.71	1.92	0.625+1.75*C_L ns
t_f		0.714	1.32	1.37	1.54	0.497+1.45*C_L ns
t_r	R TO QB	0.800	1.48	1.54	1.73	0.539+1.74*C_L ns

Switching characteristics (Sheet 1 of 2)

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_f		0.666	1.23	1.28	1.44	0.449+1.44*C_L ns
t_r	CK TO Q	0.883	1.63	1.70	1.91	0.618+1.76*C_L ns
t_f		0.690	1.27	1.33	1.49	0.472+1.45*C_L ns
t_r	CK TO QB	0.701	1.30	1.35	1.52	0.441+1.74*C_L ns
t_f		0.646	1.19	1.24	1.39	0.426+1.46*C_L ns
t_r	PD TO Q	0.897	1.66	1.73	1.94	0.632+1.76*C_L ns
t_f		0.704	1.30	1.35	1.52	0.487+1.44*C_L ns
t_r	PD TO QB	0.686	1.27	1.32	1.48	0.423+1.75*C_L ns
t_f		0.652	1.20	1.26	1.41	0.433+1.46*C_L ns
t_r	PEB TO Q	0.893	1.65	1.72	1.93	0.629+1.76*C_L ns
t_f		0.706	1.30	1.36	1.53	0.490+1.44*C_L ns
t_r	PEB TO QB	0.661	1.22	1.27	1.43	0.398+1.75*C_L ns
t_f		0.650	1.20	1.25	1.40	0.431+1.46*C_L ns

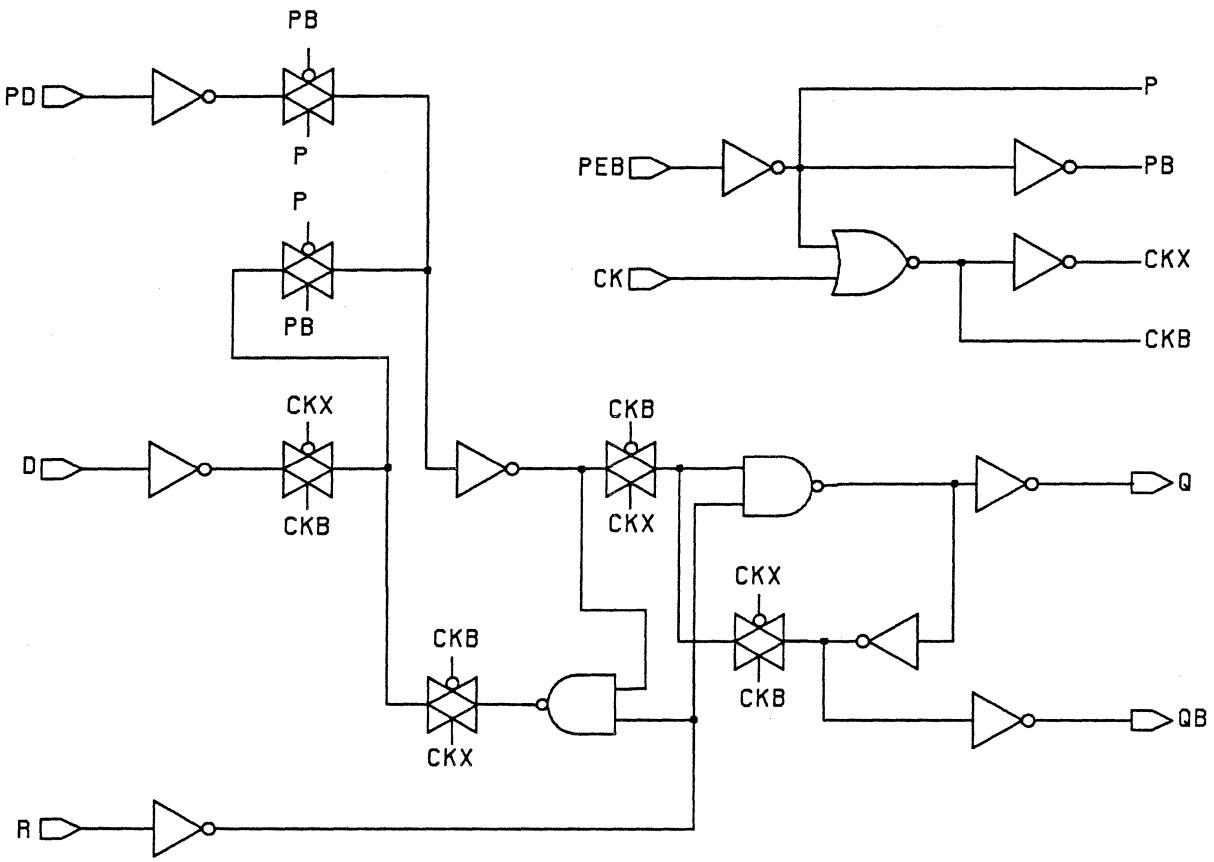
Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	2.50	ns
t_{su}	Setup Time PD to PEB	1.50	ns
t_h	Hold Time CK to D	0.00	ns
t_h	Hold Time PEB to PD	0.00	ns
t_{pwh}	R Pulse Width (high)	5.50	ns
t_{pwh}	High CK Pulse Width	4.75	ns
t_{pwl}	PEB Pulse Width (low)	5.00	ns
t_{pwl}	Low CK Pulse Width	6.50	ns
rt	R Recovery Time	−2.75	ns
rt	PEB Recovery Time	5.75	ns

Timing requirements

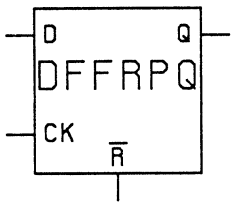
DFFRPP



Functional diagram: DFFRPP

D Flip–Flop with Reset, Positive Edge Triggered

DFFRPQ is a fully static D-type, positive edge triggered flip-flop with only a Q output. RB is asynchronous and active low.



Inputs: D, CK, RB
Outputs: Q
Input Cap.: D: 0.038
CK: 0.167
RB: 0.171 pF
Cell Size: 13 grids wide, 11 grids high

FUNCTION TABLE

D	CK	RB	Q
L	↑	H	L
H	↑	H	H
X	X	L	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.05	1.94	2.02	2.27	0.829+1.46*C_L ns
t_{PHL}		1.24	2.29	2.39	2.68	1.06+1.18*C_L ns
t_{PHL}	RB TO Q	0.956	1.76	1.84	2.06	0.856+0.663*C_L ns
t_r	CK TO Q	1.16	2.14	2.23	2.50	0.706+3.02*C_L ns
t_f		0.861	1.59	1.66	1.86	0.563+1.99*C_L ns
t_f	RB TO Q	0.537	0.992	1.03	1.16	0.387+0.998*C_L ns

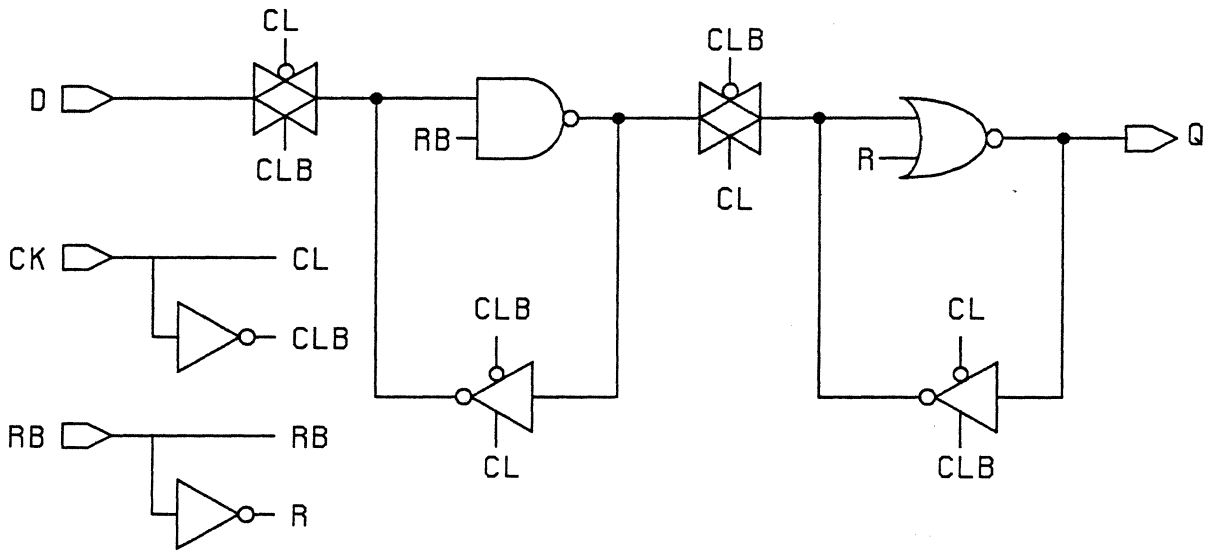
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.50	ns
t_h	Hold Time CK to D	−0.50	ns
t_{pwh}	High CK Pulse Width	3.75	ns
t_{pwl}	RB Pulse Width (low)	4.25	ns
t_{pwl}	Low CK Pulse Width	4.25	ns
rt	RB Recovery Time	0.00	ns

Timing requirements

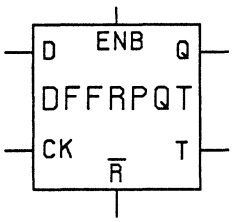
DFFRPQ



Functional diagram: DFFRPQ

D Flip–Flop with Reset and Tristate, Positive Edge Triggered

DFFRPQT is a fully static D-type, positive edge triggered flip-flop with only a Q output. RB is asynchronous and active low. When ENB is high, the T output is in a Hi-Z state and Q functions as a normal flip-flop using any of the given states defined for Q in the Function Table.



Inputs: ENB, D, CK, RB
Outputs: Q, T
Input Cap.: ENB: 0.124
D: 0.038
CK: 0.169
RB: 0.153 pF
Output Cap.: T: 0.152 pF
Cell Size: 17 grids wide, 11 grids high

FUNCTION TABLE

D	CK	RB	ENB	Q	T
L	↑	H	L	L	L
H	↑	H	L	H	H
X	X	L	L	L	L
L	↑	H	H	L	HiZ
H	↑	H	H	H	HiZ
X	X	L	H	L	HiZ

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.25	2.30	2.40	2.69	1.02+1.48*C_L ns
t_{PHL}		1.44	2.66	2.77	3.11	1.28+1.09*C_L ns
t_{PLH}	CK TO T	1.30	2.40	2.50	2.81	1.06+1.57*C_L ns
t_{PHL}		1.50	2.77	2.89	3.24	1.30+1.33*C_L ns
t_{PHL}	RB TO Q	0.993	1.83	1.91	2.15	0.897+0.639*C_L ns
t_{PHL}	RB TO T	1.92	3.54	3.69	4.14	1.72+1.30*C_L ns
t_{PLH}	ENB TO T	0.583	1.08	1.12	1.26	0.316+1.78*C_L ns
t_{PHL}		0.865	1.60	1.67	1.87	0.651+1.42*C_L ns
t_r	CK TO Q	1.23	2.28	2.38	2.67	0.781+3.02*C_L ns
t_f		0.983	1.82	1.89	2.12	0.738+1.63*C_L ns
t_r	CK TO T	1.28	2.37	2.47	2.77	0.778+3.36*C_L ns
t_f		1.24	2.30	2.39	2.68	0.872+2.46*C_L ns
t_f	RB TO Q	0.552	1.02	1.06	1.19	0.420+0.881*C_L ns
t_f	RB TO T	1.23	2.28	2.37	2.66	0.864+2.45*C_L ns
t_r	ENB TO T	1.13	2.09	2.18	2.45	0.610+3.48*C_L ns
t_f		1.02	1.89	1.97	2.21	0.636+2.57*C_L ns

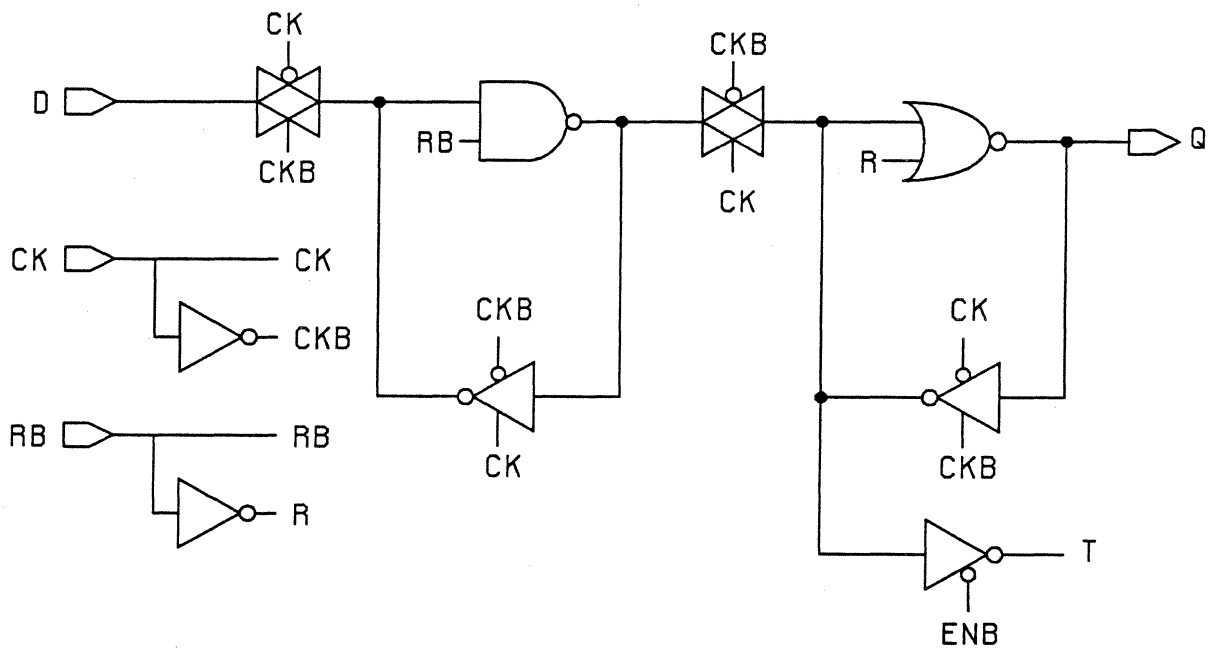
Switching characteristics

DFFRPQT

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.50	ns
t_h	Hold Time CK to D	-0.50	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwl}	RB Pulse Width (low)	4.25	ns
t_{pwl}	Low CK Pulse Width	5.00	ns
rt	RB Recovery Time	0.00	ns
rt		-0.50	ns

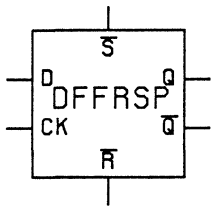
Timing requirements



Functional diagram: DFFRPQT

D Flip–Flop with Set and Reset

DFFRSP is a fully static D-type positive edge triggered flip-flop. SB and RB are asynchronous and active low. This cell is functionally compatible with a TTL 74LS74.



Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.144
D: 0.038
CK: 0.055
RB: 0.144 pF
Cell Size: 26 grids wide, 12 grids high

FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

* Both Q and QB will be high when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	3.83	7.07	7.37	8.27	3.70+0.841*C_L ns
t_{PHL}		3.75	6.92	7.21	8.09	3.62+0.822*C_L ns
t_{PLH}	CK TO QB	3.19	5.90	6.15	6.90	3.07+0.835*C_L ns
t_{PHL}		3.24	5.98	6.23	6.99	3.11+0.806*C_L ns
t_{PHL}	RB TO Q	2.71	5.01	5.23	5.86	2.59+0.822*C_L ns
t_{PLH}	RB TO QB	1.82	3.36	3.51	3.93	1.70+0.831*C_L ns
t_{PHL}		1.60	2.95	3.07	3.45	1.47+0.815*C_L ns
t_{PLH}	SB TO Q	2.10	3.89	4.05	4.54	1.98+0.845*C_L ns
t_{PHL}		1.82	3.37	3.51	3.94	1.70+0.822*C_L ns
t_{PHL}	SB TO QB	3.17	5.86	6.11	6.85	3.05+0.815*C_L ns
t_r	CK TO Q	0.679	1.25	1.31	1.47	0.415+1.76*C_L ns
t_f		0.622	1.15	1.20	1.34	0.402+1.47*C_L ns
t_r	CK TO QB	0.690	1.27	1.33	1.49	0.428+1.74*C_L ns
t_f		0.632	1.17	1.22	1.37	0.413+1.46*C_L ns
t_f	RB TO Q	0.648	1.20	1.25	1.40	0.429+1.46*C_L ns
t_r	RB TO QB	0.708	1.31	1.36	1.53	0.448+1.73*C_L ns
t_f		0.646	1.19	1.24	1.39	0.428+1.45*C_L ns
t_r	SB TO Q	0.691	1.28	1.33	1.49	0.428+1.75*C_L ns
t_f		0.641	1.18	1.23	1.38	0.421+1.46*C_L ns
t_f	SB TO QB	0.653	1.21	1.26	1.41	0.435+1.45*C_L ns

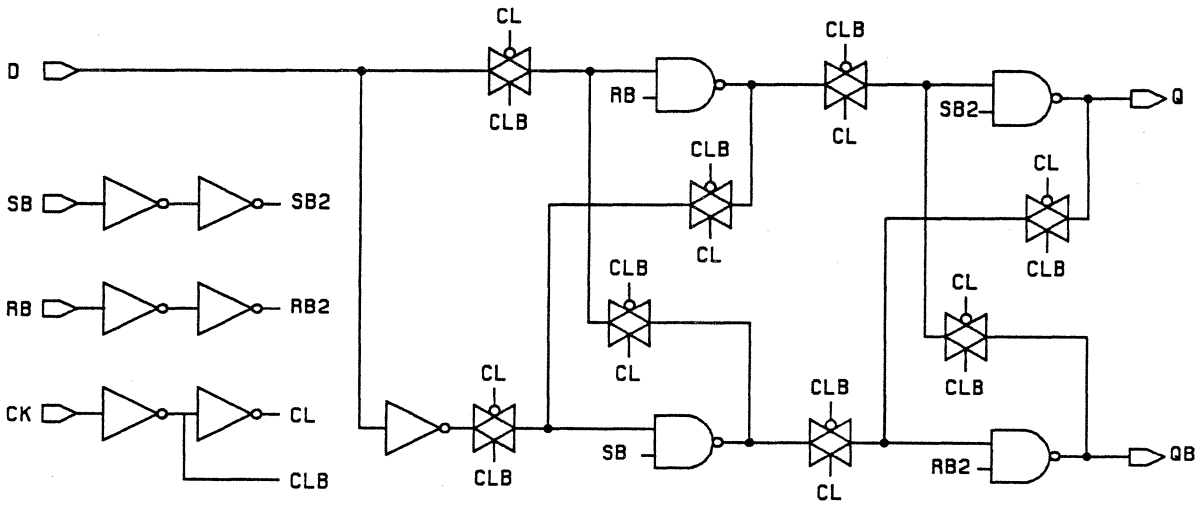
Switching characteristics

DFFRSP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.75	ns
t_h	Hold Time CK to D	−1.00	ns
t_{pwh}	High CK Pulse Width	4.75	ns
t_{pwl}	RB Pulse Width (low)	4.75	ns
t_{pwl}	SB Pulse Width (low)	4.75	ns
t_{pwl}	Low CK Pulse Width	5.00	ns
rt	RB Recovery Time	−2.25	ns
rt	SB Recovery Time	−0.50	ns

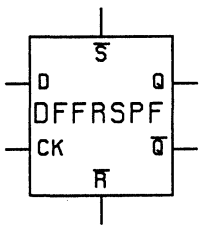
Timing requirements



Functional diagram: DFFRSP

Fast D Flip–Flop with Set and Reset

DFFRSPF is a fully static D-type positive edge triggered flip-flop. SB and RB are asynchronous and active low. This cell is functionally compatible with a TTL 74LS74.



Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.169
D: 0.105
CK: 0.106
RB: 0.169 pF
Cell Size: 30 grids wide, 12 grids high

FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

* Both Q and QB will be high when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.84	3.40	3.54	3.97	1.70+0.895*C_L ns
t_{PHL}		1.67	3.09	3.22	3.62	1.56+0.751*C_L ns
t_{PLH}	CK TO QB	1.84	3.40	3.55	3.98	1.71+0.895*C_L ns
t_{PHL}		1.68	3.09	3.23	3.62	1.56+0.739*C_L ns
t_{PHL}	RB TO Q	3.51	6.49	6.77	7.59	3.20+2.07*C_L ns
t_{PLH}	RB TO QB	2.02	3.73	3.89	4.36	1.89+0.882*C_L ns
t_{PHL}		1.71	3.16	3.29	3.69	1.59+0.776*C_L ns
t_{PLH}	SB TO Q	2.04	3.77	3.93	4.41	1.91+0.890*C_L ns
t_{PHL}		1.73	3.20	3.33	3.74	1.61+0.788*C_L ns
t_{PHL}	SB TO QB	3.54	6.53	6.81	7.64	3.22+2.08*C_L ns
t_r	CK TO Q	0.869	1.61	1.67	1.88	0.598+1.81*C_L ns
t_f		0.771	1.42	1.49	1.67	0.563+1.39*C_L ns
t_r	CK TO QB	0.863	1.59	1.66	1.86	0.593+1.80*C_L ns
t_f		0.766	1.41	1.47	1.65	0.556+1.39*C_L ns
t_f	RB TO Q	1.67	3.08	3.21	3.61	1.42+1.65*C_L ns
t_r	RB TO QB	1.48	2.73	2.85	3.20	1.20+1.87*C_L ns
t_f		1.25	2.32	2.41	2.71	1.05+1.37*C_L ns
t_r	SB TO Q	1.47	2.72	2.84	3.19	1.19+1.87*C_L ns
t_f		1.26	2.33	2.43	2.72	1.06+1.36*C_L ns
t_f	SB TO QB	1.66	3.06	3.19	3.58	1.41+1.66*C_L ns

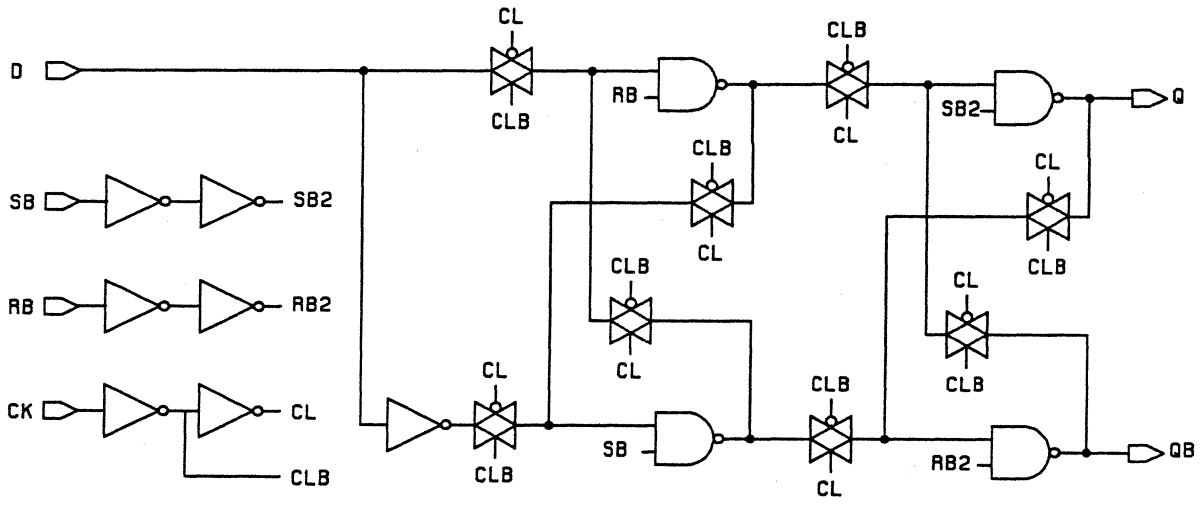
Switching characteristics

DFFRSPF

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	0.50	ns
t_h	Hold Time CK to D	0.50	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwl}	RB Pulse Width (low)	6.00	ns
t_{pwl}	SB Pulse Width (low)	6.00	ns
t_{pwl}	Low CK Pulse Width	4.25	ns
rt	RB Recovery Time	-3.00	ns
rt	SB Recovery Time	-3.00	ns

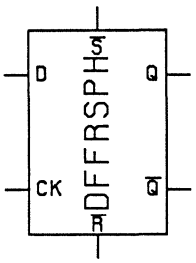
Timing requirements



Functional diagram: DFFRSPF

Buffered D Flip–Flop (High Drive) with Reset and Set, Positive Edge Triggered

DFFRSPH is a fully static D–type, edge triggered flip–flop. It is positive edge triggered with respect to the single phase clock (CK). RB and SB are asynchronous and active low.



Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.163
D: 0.089
CK: 0.105
RB: 0.178 pF
Cell Size: 25 grids wide, 12 grids high

FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

* Both Q and QB will be low when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	SB TO Q	2.35	4.34	4.53	5.08	2.26+0.597*C_L ns
t_{PLH}	RB TO Q	1.15	2.12	2.21	2.48	1.05+0.614*C_L ns
t_{PHL}		1.04	1.91	1.99	2.24	0.942+0.623*C_L ns
t_{PLH}	CK TO Q	2.24	4.13	4.31	4.83	2.14+0.632*C_L ns
t_{PHL}		2.67	4.93	5.14	5.77	2.58+0.613*C_L ns
t_{PLH}	SB TO QB	1.31	2.43	2.53	2.84	1.21+0.695*C_L ns
t_{PHL}		1.17	2.16	2.25	2.53	1.07+0.659*C_L ns
t_{PLH}	RB' TO QB	2.06	3.80	3.96	4.44	1.95+0.674*C_L ns
t_{PLH}	CK TO QB	3.36	6.21	6.47	7.26	3.27+0.602*C_L ns
t_{PHL}		3.04	5.61	5.85	6.56	2.95+0.564*C_L ns
t_r	SB TO Q	0.694	1.28	1.34	1.50	0.526+1.11*C_L ns
t_r	RB TO Q	0.649	1.20	1.25	1.40	0.479+1.13*C_L ns
t_f		0.523	0.965	1.01	1.13	0.373+0.997*C_L ns
t_r	CK TO Q	0.667	1.23	1.28	1.44	0.493+1.15*C_L ns
t_f		0.647	1.20	1.25	1.40	0.506+0.936*C_L ns
t_r	SB TO QB	0.725	1.34	1.40	1.57	0.547+1.19*C_L ns
t_f		0.626	1.16	1.20	1.35	0.478+0.981*C_L ns

Switching characteristics (Sheet 1 of 2)

DFFRSPH

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

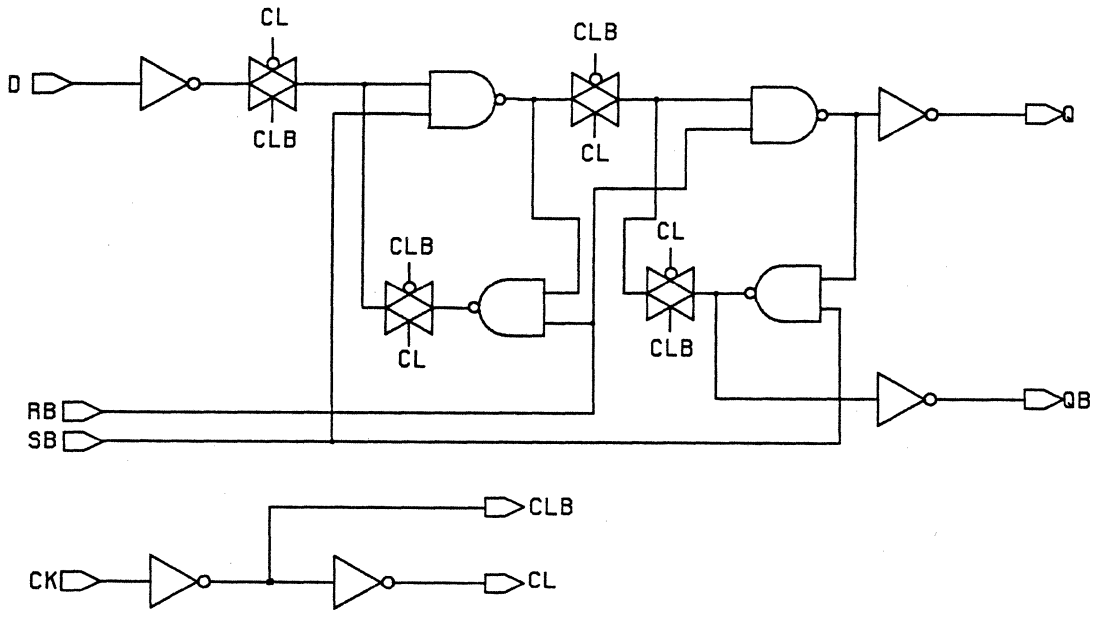
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_r	RB TO QB	0.750	1.39	1.44	1.62	0.574+1.17*C_L ns
t_r	CK TO QB	0.603	1.11	1.16	1.30	0.429+1.16*C_L ns
t_f		0.563	1.04	1.08	1.22	0.420+0.954*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	2.25	ns
t_h	Hold Time CK to D	−1.00	ns
t_{pwh}	High CK Pulse Width	4.75	ns
t_{pwl}	SB Pulse Width (low)	4.50	ns
t_{pwl}	Low CK Pulse Width	5.00	ns
t_{pwl}	RB Pulse Width (low)	4.75	ns
rt	SB Recovery Time	1.00	ns
rt	RB Recovery Time	−2.00	ns

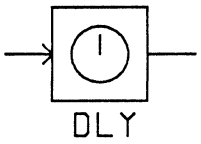
Timing requirements



Functional diagram: DFFRSPH

Delay Cell

Inputs: A
Outputs: X
Input Cap.: A: 0.054 pF
Cell Size: 7 grids wide, 11 grids high



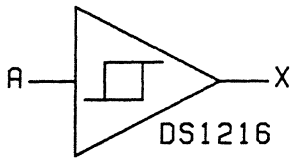
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	4.18	7.72	8.05	9.03	4.05+0.845*C_L ns
t_{PHL}		4.89	9.02	9.41	10.6	4.74+0.971*C_L ns
t_r	A TO X	1.78	3.28	3.42	3.83	1.62+1.04*C_L ns
t_f		2.59	4.78	4.98	5.58	2.43+1.06*C_L ns

Switching characteristics

Schmitt Trigger

DS1216 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.965 pF
Cell Size: 11 grids wide, 11 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 1.6V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 400mV Min: 100mV

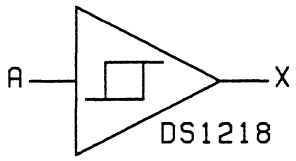
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.902	1.67	1.74	1.95	0.842+0.396*C_L ns
t_{PHL}		3.25	6.00	6.26	7.02	3.12+0.841*C_L ns
t_r	A TO X	0.618	1.14	1.19	1.34	0.489+0.864*C_L ns
t_f		1.37	2.52	2.63	2.95	1.23+0.882*C_L ns

Switching characteristics

Schmitt Trigger

DS1218 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.674 pF
Cell Size: 8 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 1.8V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 600mV Min: 300mV

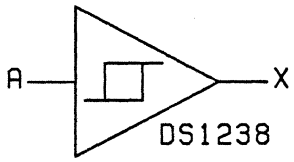
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.982	1.81	1.89	2.12	0.923+0.392*C_L ns
t_{PHL}		3.17	5.86	6.11	6.85	3.04+0.871*C_L ns
t_r	A TO X	0.625	1.16	1.20	1.35	0.493+0.880*C_L ns
t_f		1.38	2.55	2.66	2.99	1.25+0.903*C_L ns

Switching characteristics

Schmitt Trigger

DS1238 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.260 pF
Cell Size: 9 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 3.8V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 2.6V Min: 2.3V

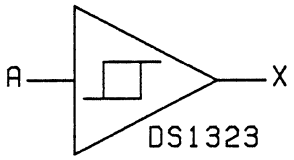
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	4.21	7.78	8.11	9.10	4.09+0.817*C_L ns
t_{PHL}		4.79	8.85	9.22	10.3	4.64+0.970*C_L ns
t_r	A TO X	2.00	3.70	3.86	4.33	1.86+0.978*C_L ns
t_f		2.36	4.36	4.55	5.10	2.21+0.999*C_L ns

Switching characteristics

Schmitt Trigger

DS1323 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.390 pF
Cell Size: 7 grids wide, 12 grids high

DC switching parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.3V ± 300mV
High to Low = 1.3V ± 300mV
Hysteresis: Typ: 1.0V Min: 700mV

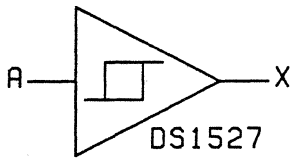
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.39	2.57	2.67	3.00	1.32+0.450*C_L ns
t_{PHL}		2.56	4.72	4.92	5.52	2.44+0.787*C_L ns
t_r	A TO X	0.645	1.19	1.24	1.39	0.509+0.900*C_L ns
t_f		1.22	2.24	2.34	2.62	1.09+0.864*C_L ns

Switching characteristics

Schmitt Trigger

DS1527 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.766 pF
Cell Size: 9 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.7V ± 300mV
High to Low = 1.5V ± 300mV
Hysteresis: Typ: 1.2V Min: 900mV

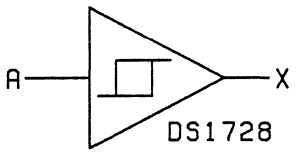
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.85	3.42	3.56	3.99	1.78+0.478*C_L ns
t_{PHL}		2.16	3.99	4.16	4.67	2.06+0.637*C_L ns
t_r	A TO X	1.000	1.85	1.93	2.16	0.859+0.942*C_L ns
t_f		1.10	2.03	2.12	2.38	0.979+0.811*C_L ns

Switching characteristics

Schmitt Trigger

DS1728 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 1.260 pF
Cell Size: 12 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.8V ± 300mV
High to Low = 1.7V ± 300mV
Hysteresis: Typ: 1.1V Min: 800mV

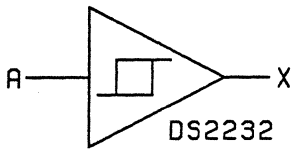
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.90	3.51	3.66	4.10	1.83+0.455*C_L ns
t_{PHL}		1.97	3.63	3.79	4.25	1.88+0.560*C_L ns
t_r	A TO X	1.22	2.25	2.34	2.63	1.08+0.910*C_L ns
t_f		1.08	2.00	2.09	2.34	0.966+0.783*C_L ns

Switching characteristics

Schmitt Trigger

DS2232 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.278 pF
Cell Size: 7 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 3.2V ± 300mV
High to Low = 2.2.V ± 300mV
Hysteresis: Typ: 1.0V Min: 700mV

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.89	3.49	3.64	4.08	1.81+0.548*C_L ns
t_{PHL}		1.75	3.22	3.36	3.77	1.66+0.554*C_L ns
t_r	A TO X	0.776	1.43	1.49	1.68	0.641+0.901*C_L ns
t_f		0.869	1.60	1.67	1.88	0.753+0.769*C_L ns

Switching characteristics

2–Input Exclusive NOR

Inputs: A, B
Outputs: X
Input Cap.: A: 0.221
B: 0.220 pF
Cell Size: 11 grids wide, 12 grids high

$X = A \cdot B + \overline{A} \cdot \overline{B}$

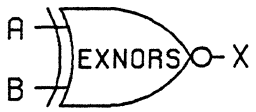
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.45	2.68	2.79	3.14	1.28+1.14*C_L ns
t_{PHL}		1.47	2.72	2.83	3.18	1.32+0.987*C_L ns
t_r	*IN TO X	1.37	2.53	2.64	2.96	0.994+2.51*C_L ns
t_f		1.28	2.37	2.47	2.77	0.994+1.91*C_L ns
* Slowest input						

Switching characteristics

2–Input Exclusive NOR

Inputs: A, B
Outputs: X
Input Cap.: A: 0.151
B: 0.149 pF
Cell Size: 6 grids wide, 9 grids high



$X = A \cdot B + \overline{A} \cdot \overline{B}$

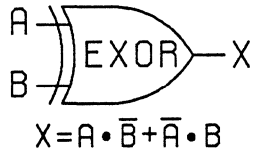
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.11	2.05	2.13	2.39	0.837+1.80*C_L ns
t_{PHL}		1.21	2.24	2.33	2.61	0.995+1.43*C_L ns
t_r	*IN TO X	1.43	2.63	2.75	3.08	0.845+3.87*C_L ns
t_f		1.13	2.09	2.18	2.45	0.713+2.79*C_L ns
* Slowest input						

Switching characteristics

2–Input Exclusive OR Gate

Inputs: A, B
Outputs: X
Input Cap.: A: 0.216
B: 0.217 pF
Cell Size: 11 grids wide, 12 grids high



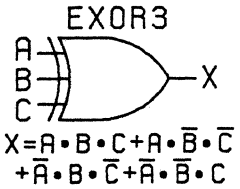
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.44	2.67	2.78	3.12	1.27+1.12*C_L ns
t_{PHL}		1.52	2.80	2.92	3.28	1.37+0.991*C_L ns
t_r	*IN TO X	1.26	2.33	2.42	2.72	0.882+2.51*C_L ns
t_f		1.22	2.26	2.35	2.64	0.934+1.92*C_L ns
* Slowest input						

Switching characteristics

3–Input Exclusive OR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.350
B: 0.477
C: 0.347 pF
Cell Size: 16 grids wide, 18 grids high



FUNCTION TABLE

A	B	C	X
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

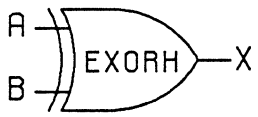
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.86	3.43	3.57	4.01	1.61+1.65*C_L ns
t_{PHL}		1.61	2.97	3.09	3.47	1.39+1.45*C_L ns
t_r	*IN TO X	2.47	4.56	4.76	5.34	1.93+3.61*C_L ns
t_f		2.32	4.28	4.46	5.00	1.89+2.84*C_L ns
* Slowest input						

Switching characteristics

2–Input Exclusive OR Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: All: 0.160 pF
Cell Size: 16 grids wide, 12 grids high



$X = A \cdot \overline{B} + \overline{A} \cdot B$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.53	2.83	2.95	3.31	1.45+0.575*C_L ns
t_{PHL}		1.39	2.57	2.68	3.01	1.30+0.616*C_L ns
t_r	*IN TO X	0.897	1.66	1.73	1.94	0.748+0.991*C_L ns
t_f		0.908	1.68	1.75	1.96	0.783+0.831*C_L ns
* Slowest input						

Switching characteristics

2–Input Exclusive OR Gate

Inputs: A, B
Outputs: X
Input Cap.: A: 0.148
B: 0.140 pF
Cell Size: 6 grids wide, 9 grids high

$X = A \cdot \overline{B} + \overline{A} \cdot B$

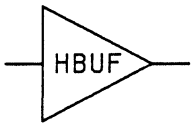
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.14	2.11	2.20	2.47	0.858+1.89*C_L ns
t_{PHL}		1.20	2.21	2.30	2.59	0.993+1.36*C_L ns
t_r	*IN TO X	1.44	2.66	2.77	3.11	0.812+4.17*C_L ns
t_f		1.10	2.03	2.12	2.38	0.717+2.56*C_L ns
* Slowest input						

Switching characteristics

High Drive Noninverting Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.055 pF
Cell Size: 4 grids wide, 11 grids high



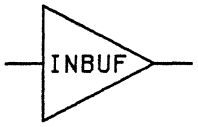
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.06	1.96	2.05	2.30	0.991+0.478*C_L ns
t_{PHL}		1.18	2.17	2.27	2.54	1.10+0.480*C_L ns
t_r	A TO X	0.531	0.980	1.02	1.15	0.401+0.862*C_L ns
t_f		0.554	1.02	1.07	1.20	0.446+0.721*C_L ns

Switching characteristics

Noninverting Input Buffer

INBUF is used to buffer the signal from input and I/O pads, and is compatible with 1.4V ± 300mV threshold voltage (V_{DD} = 5V). INBUF is tested using V_{IL} = 0.8V and V_{IH} = 2.0V.



Inputs: A
Outputs: X
Input Cap.: A: 0.215 pF
Cell Size: 5 grids wide, 12 grids high

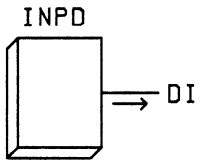
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.558	1.03	1.07	1.20	0.495+0.413*C_L ns
t_{PHL}		1.52	2.81	2.93	3.29	1.44+0.538*C_L ns
t_r	A TO X	0.600	1.11	1.15	1.30	0.488+0.744*C_L ns
t_f		0.985	1.82	1.90	2.13	0.887+0.650*C_L ns

Switching characteristics

Input Pad

INPD is used with INBUF or one of the Schmitt Triggers. Note that the input buffer and the chip package will add additional capacitance to all inputs.



Inputs: PAD
Outputs: DI
Input Cap.: PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

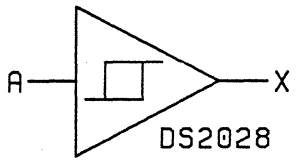
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

Schmitt Trigger

DS2028 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.451 pF
Cell Size: 9 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.8V ± 300mV
High to Low = 2.0V ± 300mV
Hysteresis: Typ: 800mV Min: 500mV

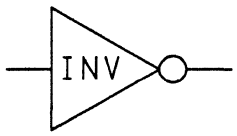
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	2.34	4.32	4.51	5.06	2.26+0.542*C_L ns
t_{PHL}		1.80	3.32	3.46	3.89	1.71+0.576*C_L ns
t_r	A TO X	0.978	1.81	1.88	2.11	0.839+0.930*C_L ns
t_f		0.890	1.64	1.71	1.92	0.775+0.767*C_L ns

Switching characteristics

Inverter

Inputs: A
Outputs: X
Input Cap.: A: 0.055 pF
Cell Size: 2 grids wide, 8 grids high



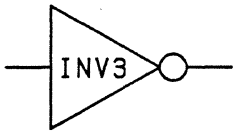
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.584	1.08	1.12	1.26	0.338+1.64*C_L ns
t_{PHL}		0.584	1.08	1.12	1.26	0.351+1.55*C_L ns
t_r	A TO X	0.891	1.65	1.72	1.92	0.348+3.62*C_L ns
t_f		0.758	1.40	1.46	1.64	0.301+3.05*C_L ns

Switching characteristics

Inverter (3X Drive)

INV3 has 3 times the drive of an INV.



Inputs: A
Outputs: X
Input Cap.: A: 0.159 pF
Cell Size: 3 grids wide, 9 grids high

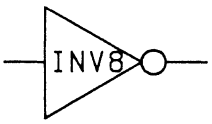
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.362	0.668	0.696	0.781	0.279+0.552*C_L ns
t_{PHL}		0.364	0.672	0.700	0.786	0.284+0.528*C_L ns
t_r	A TO X	0.529	0.977	1.02	1.14	0.363+1.10*C_L ns
t_f		0.467	0.863	0.899	1.01	0.330+0.913*C_L ns

Switching characteristics

Inverting Buffer (8X Drive)

INV8 has 8 times the drive of an INV.



Inputs: A
Outputs: X
Input Cap.: A: 0.421 pF
Cell Size: 5 grids wide, 11 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

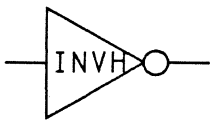
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.263	0.486	0.507	0.569	0.226+0.249*C_L ns
t_{PHL}		0.259	0.478	0.499	0.560	0.222+0.247*C_L ns
t_r	A TO X	0.430	0.794	0.827	0.928	0.374+0.374*C_L ns
t_f		0.398	0.735	0.766	0.859	0.353+0.294*C_L ns

Switching characteristics

Inverter (High Drive)

INVH has 3 times the drive of an INV.

Inputs: A
Outputs: X
Input Cap.: A: 0.157 pF
Cell Size: 3 grids wide, 10 grids high



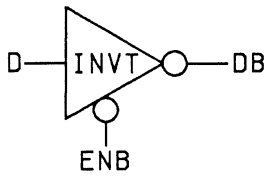
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.371	0.686	0.715	0.802	0.289+0.551*C_L ns
t_{PHL}		0.371	0.685	0.714	0.802	0.292+0.526*C_L ns
t_r	A TO X	0.545	1.01	1.05	1.18	0.379+1.10*C_L ns
t_f		0.473	0.874	0.911	1.02	0.335+0.919*C_L ns

Switching characteristics

Tristate Inverter

INVT inverts the input signal when ENB is low. When ENB is high the output is in a Hi-Z state.



Inputs: D, ENB
Outputs: DB
Input Cap.: D: 0.106
ENB: 0.126 pF
Output Cap.: DB: 0.138 pF
Cell Size: 5 grids wide, 11 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

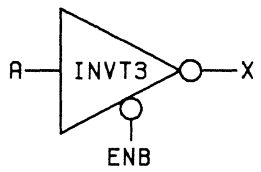
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO DB	0.785	1.45	1.51	1.70	0.546+1.59*C_L ns
t_{PHL}		0.762	1.41	1.47	1.65	0.556+1.37*C_L ns
t_{PLH}	ENB TO DB	0.652	1.20	1.25	1.41	0.415+1.58*C_L ns
t_{PHL}		1.35	2.49	2.59	2.91	1.14+1.38*C_L ns
t_r	D TO DB	1.25	2.31	2.40	2.70	0.714+3.56*C_L ns
t_f		1.09	2.02	2.11	2.36	0.679+2.76*C_L ns
t_r	ENB TO DB	1.19	2.20	2.30	2.58	0.656+3.58*C_L ns
t_f		1.09	2.01	2.09	2.35	0.671+2.77*C_L ns

Switching characteristics

INVT3

Tristate Inverter (3X Drive)

INVT3 is a high drive tristate inverter with 3 times the drive of an INVT and a larger intrinsic delay. INVT3 inverts the input signal when ENB is low. When ENB is high the output is in a Hi-Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.055
ENB: 0.053 pF
Output Cap.: X: 0.160 pF
Cell Size: 12 grids wide, 10 grids high

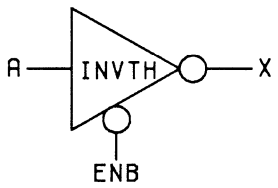
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.61	2.97	3.10	3.47	1.51+0.641*C_L ns
t_{PHL}		1.50	2.76	2.88	3.23	1.40+0.626*C_L ns
t_{PLH}	ENB TO X	1.64	3.02	3.15	3.54	1.54+0.641*C_L ns
t_{PHL}		1.79	3.31	3.45	3.87	1.70+0.625*C_L ns
t_r	A TO X	0.622	1.15	1.20	1.34	0.449+1.15*C_L ns
t_f		0.532	0.982	1.02	1.15	0.383+0.987*C_L ns
t_r	ENB TO X	0.588	1.09	1.13	1.27	0.414+1.16*C_L ns
t_f		0.504	0.931	0.970	1.09	0.354+0.998*C_L ns

Switching characteristics

Tristate Inverter (High Drive)

INVTH is a high drive tristate inverter with 2 times the drive of an INVT and a smaller intrinsic delay. The input signal is inverted when ENB is low. When ENB is high the output is in a Hi-Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.158
ENB: 0.057 pF
Output Cap.: X: 0.158 pF
Cell Size: 9 grids wide, 10 grids high

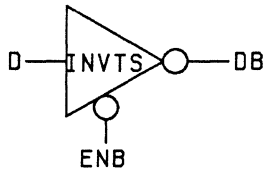
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.550	1.02	1.06	1.19	0.391+1.05*C_L ns
t_{PHL}		0.533	0.985	1.03	1.15	0.397+0.905*C_L ns
t_{PLH}	ENB TO X	0.823	1.52	1.58	1.78	0.661+1.08*C_L ns
t_{PHL}		0.834	1.54	1.60	1.80	0.684+0.995*C_L ns
t_r	A TO X	0.862	1.59	1.66	1.86	0.512+2.33*C_L ns
t_f		0.658	1.22	1.27	1.42	0.387+1.80*C_L ns
t_r	ENB TO X	0.862	1.59	1.66	1.86	0.510+2.34*C_L ns
t_f		0.628	1.16	1.21	1.36	0.355+1.82*C_L ns

Switching characteristics

Tristate Inverter

INVTS inverts the input signal when ENB is low. When ENB is high the output is in a Hi-Z state.



Inputs: D, ENB
Outputs: DB
Input Cap.: D: 0.096
ENB: 0.122 pF
Output Cap.: DB: 0.129 pF
Cell Size: 4 grids wide, 10 grids high

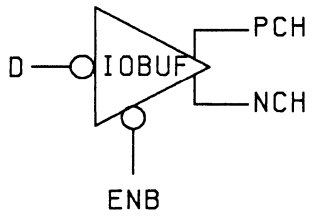
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO DB	0.730	1.35	1.40	1.58	0.476+1.69*C_L ns
t_{PHL}		0.605	1.12	1.16	1.31	0.412+1.28*C_L ns
t_{PLH}	ENB TO DB	0.599	1.11	1.15	1.29	0.320+1.86*C_L ns
t_{PHL}		0.770	1.42	1.48	1.66	0.566+1.36*C_L ns
t_r	D TO DB	1.20	2.22	2.31	2.59	0.651+3.66*C_L ns
t_f		0.902	1.67	1.74	1.95	0.522+2.53*C_L ns
t_r	ENB TO DB	1.15	2.11	2.20	2.47	0.590+3.70*C_L ns
t_f		0.931	1.72	1.79	2.01	0.554+2.51*C_L ns

Switching characteristics

Input/Output Buffer

IOBUF is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.113
D: 0.072 pF
Cell Size: 14 grids wide, 11 grids high

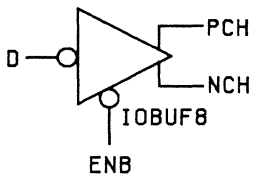
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO NCH	2.55	4.70	4.90	5.50	2.47+0.483*C_L ns
t_{PHL}		1.50	2.78	2.90	3.25	1.43+0.478*C_L ns
t_{PLH}	D TO PCH	1.94	3.59	3.74	4.19	1.87+0.471*C_L ns
t_{PHL}		1.88	3.47	3.62	4.06	1.81+0.484*C_L ns
t_{PLH}	ENB TO NCH	2.32	4.29	4.47	5.02	2.25+0.475*C_L ns
t_{PHL}		1.34	2.47	2.57	2.89	1.26+0.478*C_L ns
t_{PLH}	ENB TO PCH	1.90	3.52	3.67	4.11	1.83+0.470*C_L ns
t_{PHL}		2.02	3.72	3.88	4.35	1.94+0.471*C_L ns
t_r	D TO NCH	0.624	1.15	1.20	1.35	0.499+0.826*C_L ns
t_f		0.594	1.10	1.14	1.28	0.490+0.693*C_L ns
t_r	D TO PCH	0.593	1.10	1.14	1.28	0.468+0.834*C_L ns
t_f		0.579	1.07	1.11	1.25	0.473+0.705*C_L ns
t_r	ENB TO NCH	0.611	1.13	1.18	1.32	0.486+0.832*C_L ns
t_f		0.571	1.05	1.10	1.23	0.466+0.702*C_L ns
t_r	ENB TO PCH	0.532	0.983	1.03	1.15	0.404+0.855*C_L ns
t_f		0.592	1.09	1.14	1.28	0.488+0.694*C_L ns

Switching characteristics

Input/Output Buffer (8X Drive)

IOBUF8 is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.113
D: 0.072 pF
Cell Size: 18 grids wide, 11 grids high

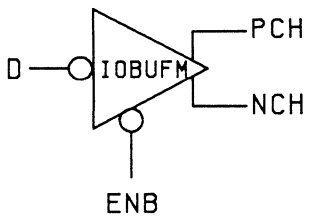
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO NCH	2.94	5.44	5.67	6.36	2.90+0.274*C_L ns
t_{PHL}		1.56	2.88	3.01	3.37	1.52+0.259*C_L ns
t_{PLH}	D TO PCH	2.10	3.88	4.04	4.54	2.06+0.270*C_L ns
t_{PHL}		2.04	3.78	3.94	4.42	2.00+0.298*C_L ns
t_{PLH}	ENB TO NCH	2.55	4.71	4.91	5.51	2.51+0.276*C_L ns
t_{PHL}		1.38	2.55	2.66	2.98	1.34+0.272*C_L ns
t_{PLH}	ENB TO PCH	1.99	3.68	3.83	4.30	1.95+0.278*C_L ns
t_{PHL}		2.11	3.90	4.07	4.56	2.07+0.274*C_L ns
t_r	D TO NCH	0.609	1.12	1.17	1.32	0.549+0.395*C_L ns
t_f		0.568	1.05	1.09	1.23	0.520+0.322*C_L ns
t_r	D TO PCH	0.535	0.989	1.03	1.16	0.474+0.410*C_L ns
t_f		0.530	0.978	1.02	1.14	0.478+0.346*C_L ns
t_r	ENB TO NCH	0.598	1.10	1.15	1.29	0.539+0.392*C_L ns
t_f		0.533	0.984	1.03	1.15	0.482+0.339*C_L ns
t_r	ENB TO PCH	0.499	0.922	0.962	1.08	0.439+0.405*C_L ns
t_f		0.543	1.000	1.05	1.17	0.491+0.345*C_L ns

Switching characteristics

Input/Output Buffer (Medium Drive)

IOBUFM is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.113
D: 0.072 pF
Cell Size: 14 grids wide, 11 grids high

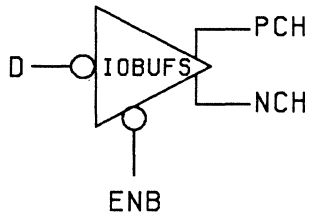
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO NCH	2.57	4.75	4.95	5.55	2.44+0.847*C_L ns
t_{PHL}		1.25	2.30	2.40	2.70	1.17+0.487*C_L ns
t_{PLH}	D TO PCH	1.98	3.66	3.81	4.28	1.85+0.850*C_L ns
t_{PHL}		1.67	3.08	3.21	3.60	1.59+0.480*C_L ns
t_{PLH}	ENB TO NCH	2.32	4.28	4.46	5.01	2.19+0.835*C_L ns
t_{PHL}		1.10	2.03	2.12	2.37	1.03+0.480*C_L ns
t_{PLH}	ENB TO PCH	1.98	3.65	3.81	4.27	1.85+0.845*C_L ns
t_{PHL}		1.81	3.35	3.49	3.92	1.74+0.468*C_L ns
t_r	D TO NCH	0.694	1.28	1.34	1.50	0.432+1.75*C_L ns
t_f		0.503	0.928	0.968	1.09	0.397+0.702*C_L ns
t_r	D TO PCH	0.677	1.25	1.30	1.46	0.413+1.76*C_L ns
t_f		0.498	0.919	0.958	1.08	0.393+0.697*C_L ns
t_r	ENB TO NCH	0.708	1.31	1.36	1.53	0.448+1.74*C_L ns
t_f		0.470	0.868	0.905	1.01	0.363+0.713*C_L ns
t_r	ENB TO PCH	0.654	1.21	1.26	1.41	0.390+1.76*C_L ns
t_f		0.503	0.928	0.968	1.09	0.399+0.690*C_L ns

Switching characteristics

Input/Output Buffer (Small Drive)

IOBUFS is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.113
D: 0.072 pF
Cell Size: 14 grids wide, 11 grids high

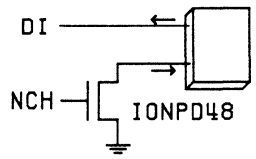
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO NCH	2.71	5.00	5.21	5.85	2.46+1.65*C_L ns
t_{PHL}		1.12	2.07	2.16	2.42	1.05+0.476*C_L ns
t_{PLH}	D TO PCH	2.11	3.89	4.05	4.55	1.85+1.67*C_L ns
t_{PHL}		1.54	2.84	2.97	3.33	1.47+0.467*C_L ns
t_{PLH}	ENB TO NCH	2.47	4.55	4.75	5.33	2.22+1.65*C_L ns
t_{PHL}		0.990	1.83	1.91	2.14	0.920+0.466*C_L ns
t_{PLH}	ENB TO PCH	2.12	3.91	4.08	4.57	1.87+1.65*C_L ns
t_{PHL}		1.67	3.08	3.21	3.60	1.60+0.467*C_L ns
t_r	D TO NCH	0.993	1.83	1.91	2.14	0.452+3.60*C_L ns
t_f		0.464	0.857	0.893	1.000	0.359+0.695*C_L ns
t_r	D TO PCH	0.957	1.77	1.84	2.07	0.413+3.62*C_L ns
t_f		0.463	0.856	0.892	1.000	0.360+0.686*C_L ns
t_r	ENB TO NCH	0.981	1.81	1.89	2.12	0.440+3.61*C_L ns
t_f		0.415	0.767	0.799	0.897	0.307+0.717*C_L ns
t_r	ENB TO PCH	0.947	1.75	1.82	2.05	0.403+3.63*C_L ns
t_f		0.456	0.841	0.877	0.984	0.351+0.694*C_L ns

Switching characteristics

48mA Open Drain Input/Output Pad

IONPD48 is used to form a bidirectional pad that can drive output data, or be put in a Hi–Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD, DI
Input Cap.: NCH: 12.520
PAD: 10.600 pF
Cell Size: 51 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	134	248	258	289	31.3+2.05*C_L ns
t_{PHL}		0.573	1.06	1.10	1.24	0.343+0.005*C_L ns

Switching characteristics

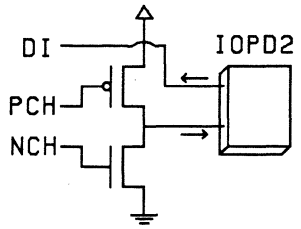
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	48.00	mA

DC specifications

2mA Input/Output Pad

IOPD2 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH, PCH: 0.529
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	5.86	10.8	11.3	12.6	0.767+0.102*C_L ns
t_{PHL}		6.55	12.1	12.6	14.1	0.742+0.116*C_L ns
* NCH or PCH						

Switching characteristics

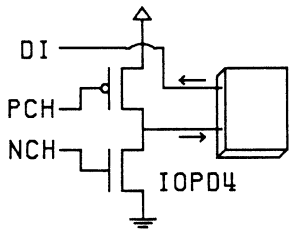
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-1.00	mA

DC specifications

4mA Input/Output Pad

IOPD4 is used to form a bidirectional pad that can drive output data, or be put in a Hi-Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH, PCH: 1.059
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	3.07	5.66	5.90	6.62	0.536+0.051*C_L ns
t_{PHL}		3.39	6.27	6.54	7.33	0.491+0.058*C_L ns
* NCH or PCH						

Switching characteristics

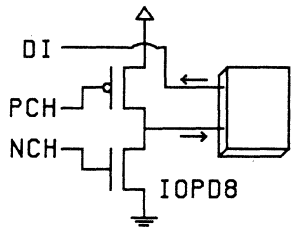
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-2.00	mA

DC specifications

8mA Input/Output Pad

IOPD8 is used to form a bidirectional pad that can drive data or be put in a Hi-Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH, PCH: 2.120
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	1.68	3.11	3.24	3.64	0.419+0.025*C_L ns
t_{PHL}		1.84	3.40	3.54	3.98	0.374+0.029*C_L ns
* NCH or PCH						

Switching characteristics

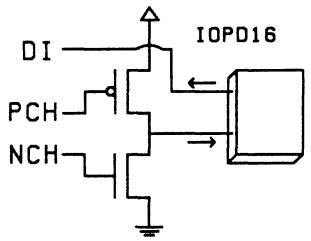
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-4.00	mA

DC specifications

16mA Input/Output Pad

IOPD16 is used to form a bidirectional pad that can drive output data or be put in a Hi–Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH, PCH: 4.240
PAD: 6.900 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.988	1.82	1.90	2.13	0.355+0.013*C_L ns
t_{PHL}		1.06	1.96	2.04	2.29	0.340+0.014*C_L ns
* NCH or PCH						

Switching characteristics

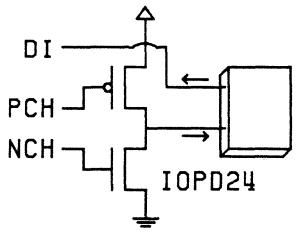
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}–0.5V	–8.00	mA

DC specifications

24mA Input/Output Pad

IOPD24 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH: 6.360
PCH: 5.290
PAD: 9.200 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.891	1.65	1.71	1.92	0.373+0.010*C_L ns
t_{PHL}		0.798	1.47	1.54	1.72	0.309+0.010*C_L ns
* NCH or PCH						

Switching characteristics

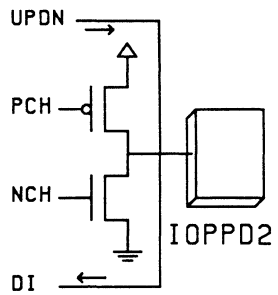
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}-0.5V	-12.00	mA

DC specifications

2mA Input/Output Pad with Pullup/Pulldown Port

IOPPD2 is similar to IOPD2 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH, PCH: 0.529
UPDN: 52.000
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	5.88	10.9	11.3	12.7	0.792+0.102*C_L ns
t_{PHL}		6.58	12.2	12.7	14.2	0.774+0.116*C_L ns
* NCH or PCH						

Switching characteistics

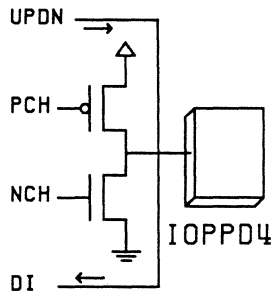
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}-0.5V	-1.00	mA

DC specifications

4mA Input/Output Pad with Pullup/Pulldown Port

IOPPD4 is similar to IOPD4 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH, PCH: 1.059
UPDN: 52.000
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	3.08	5.69	5.93	6.65	0.549+0.051*C_L ns
t_{PHL}		3.41	6.30	6.57	7.37	0.508+0.058*C_L ns
* NCH or PCH						

Switching characteristics

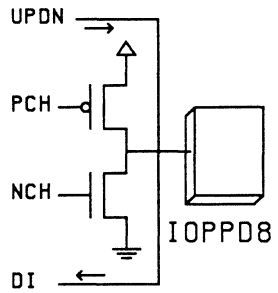
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-2.00	mA

DC specifications

8mA Input/Output Pad with Pullup/Pulldown Port

IOPPD8 is similar to IOPD8 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH, PCH: 2.120
UPDN: 52.000
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	1.69	3.12	3.25	3.65	0.425+0.025*C_L ns
t_{PHL}		1.85	3.42	3.56	4.00	0.383+0.029*C_L ns
* NCH or PCH						

Switching characteristics

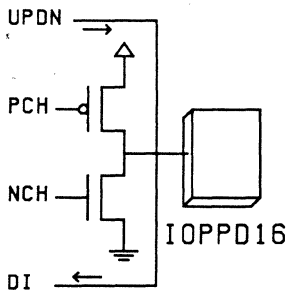
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-4.00	mA

DC specifications

16mA Input/Output Pad with Pullup/Pulldown Port

IOPPD16 is similar to IOPD16 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH, PCH: 4.240
UPDN: 52.000
PAD: 6.900 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	0.991	1.83	1.91	2.14	0.358+0.013*C_L ns
t_{PHL}		1.06	1.96	2.04	2.29	0.343+0.014*C_L ns
* NCH or PCH						

Switching characteristics

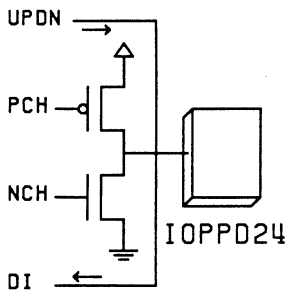
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-8.00	mA

DC specifications

24mA Input/Output Pad with Pullup/Pulldown Port

IOPPD24 is similar to IOPD24 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH: 6.360
PCH: 5.300
UPDN: 52.000
PAD: 9.200 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.23	5.96	6.21	6.97	0.523+0.054*C_L ns
t_{PHL}		9.33	17.2	18.0	20.1	0.816+0.170*C_L ns
t_{PLH}	*IN TO PAD	0.893	1.65	1.72	1.93	0.375+0.010*C_L ns
t_{PHL}		0.802	1.48	1.54	1.73	0.313+0.010*C_L ns
* NCH or PCH						

Switching characteristics

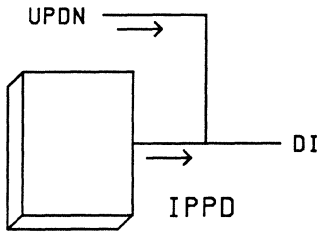
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-12.00	mA

DC specifications

Input Pad with Pullup/Pulldown Port

IPPD is similar to INPD but includes an input port, UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See any PPU/PPD data sheet for pullup/pulldown current information.



Inputs: PAD, UPDN
Outputs: DI
Input Cap.: PAD: 5.500
UPDN: 52.000 pF
Cell Size: 22.5 grids wide, 60 grids high

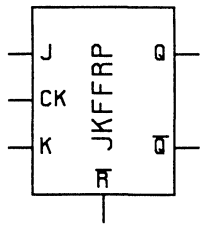
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO DI	3.17	5.86	6.10	6.85	3.14+0.204*C_L ns
t_{PHL}		9.08	16.8	17.5	19.6	9.02+0.323*C_L ns
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

J–K Flip–Flop with Reset, Positive Edge Triggered

JKFFRP is a fully static JK–type edge triggered flip–flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low.



Inputs: J, CK, K, RB
Outputs: Q, QB
Input Cap.: J: 0.055
CK: 0.189
K: 0.055
RB: 0.171 pF
Cell Size: 21 grids wide, 11 grids high

FUNCTION TABLE

J	K	CK	RB	Q	QB
H	H	↑	H	QB_o	Q_o
H	L	↑	H	H	L
L	H	↑	H	L	H
L	L	↑	H	Q_o	QB_o
X	X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.06	1.96	2.05	2.30	0.960+0.682*C_L ns
t_{PHL}		1.26	2.33	2.43	2.73	1.08+1.20*C_L ns
t_{PLH}	CK TO QB	1.96	3.62	3.77	4.23	1.79+1.09*C_L ns
t_{PHL}		2.07	3.82	3.98	4.47	1.98+0.577*C_L ns
t_{PHL}	RB TO Q	3.95	7.29	7.60	8.52	3.74+1.33*C_L ns
t_{PLH}	RB TO QB	1.48	2.73	2.85	3.20	1.31+1.11*C_L ns
t_r	CK TO Q	0.939	1.73	1.81	2.03	0.618+2.13*C_L ns
t_f		0.843	1.56	1.62	1.82	0.571+1.81*C_L ns
t_r	CK TO QB	0.747	1.38	1.44	1.61	0.410+2.25*C_L ns
t_f		0.827	1.53	1.59	1.79	0.593+1.56*C_L ns
t_f	RB TO Q	1.23	2.28	2.38	2.67	0.966+1.79*C_L ns
t_r	RB TO QB	0.708	1.31	1.36	1.53	0.367+2.28*C_L ns

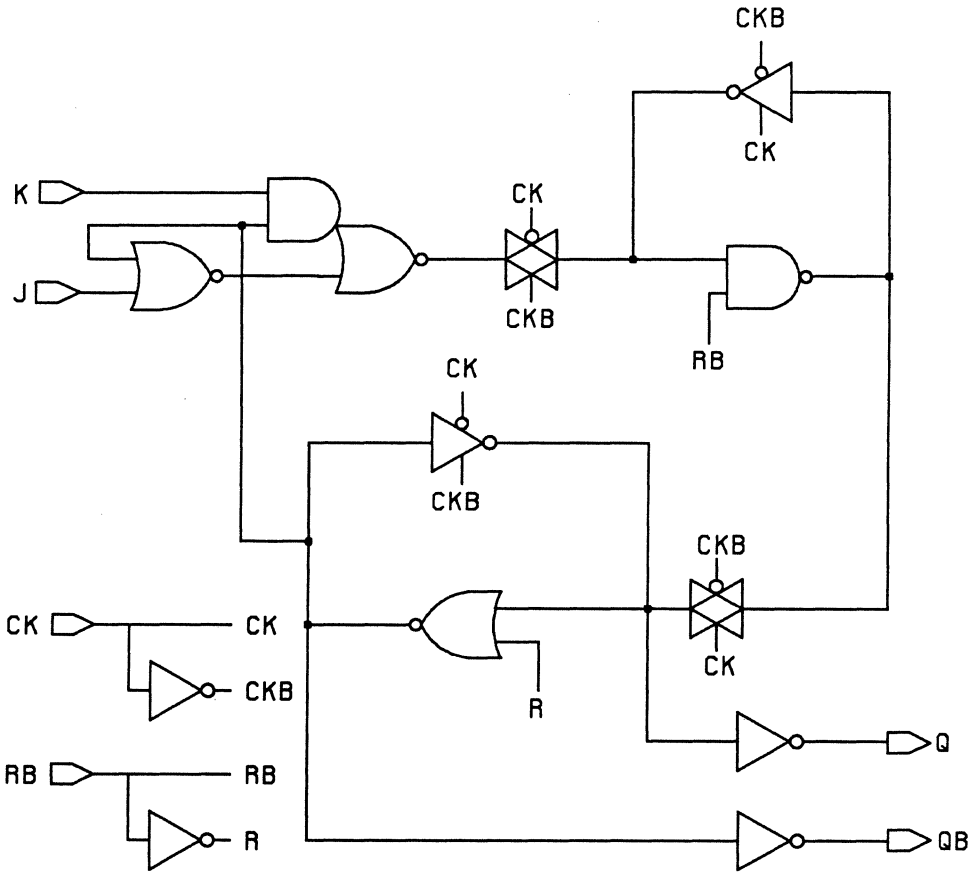
Switching characteristics

JKFFRP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time J to CK	4.00	ns
t_{su}	Setup Time K to CK	3.00	ns
t_h	Hold Time CK to J	-2.75	ns
t_h	Hold Time CK to K	-2.25	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwl}	Low CK Pulse Width	4.00	ns
t_{pwl}	RB Pulse Width (low)	5.00	ns
rt	RB Recovery Time	0.00	ns

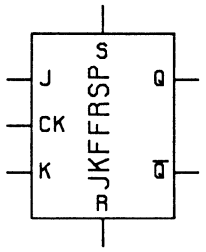
Timing requirements



Functional diagram: JKFFRP

J–K Flip–Flop with Set and Reset, Positive Edge Triggered

JKFFRSP is a fully static JK-type edge triggered flip-flop. It is positive edge triggered with respect to CK. S and R are asynchronous, and active high. For a faster version of this cell, see JKFFRSPF.



Inputs: CK, J, K, S, R
Outputs: Q, QB
Input Cap.: CK, J, K: 0.055
S: 0.118
R: 0.110 pF
Cell Size: 28 grids wide, 12 grids high

FUNCTION TABLE

J	K	CK	S	R	Q	QB
H	H	↑	L	L	QB_o	Q_o
H	L	↑	L	L	H	L
L	H	↑	L	L	L	H
L	L	↑	L	L	Q_o	QB_o
X	X	X	H	L	H	L
X	X	X	L	H	L	H
X	X	X	H	H	*	*

* Both Q and QB will be high as long as S and R are both high, but the output state is indeterminate if both S and R go low simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	4.51	8.33	8.68	9.74	4.39+0.812*C_L ns
t_{PHL}		4.60	8.50	8.86	9.95	4.46+0.967*C_L ns
t_{PLH}	CK TO QB	3.22	5.95	6.21	6.96	3.09+0.895*C_L ns
t_{PHL}		3.43	6.33	6.60	7.40	3.27+1.05*C_L ns
t_{PLH}	S TO Q	1.35	2.50	2.60	2.92	1.21+0.944*C_L ns
t_{PHL}		2.32	4.29	4.47	5.01	2.16+1.07*C_L ns
t_{PHL}	S TO QB	3.36	6.20	6.46	7.25	3.20+1.01*C_L ns
t_{PHL}	R TO Q	3.23	5.97	6.22	6.98	3.07+1.06*C_L ns
t_{PLH}	R TO QB	1.28	2.37	2.47	2.77	1.15+0.882*C_L ns
t_{PHL}		2.02	3.73	3.89	4.36	1.87+1.01*C_L ns
t_r	CK TO Q	0.825	1.52	1.59	1.78	0.570+1.70*C_L ns
t_f		0.902	1.67	1.74	1.95	0.678+1.49*C_L ns
t_r	CK TO QB	0.907	1.67	1.75	1.96	0.655+1.68*C_L ns
t_f		1.05	1.93	2.02	2.26	0.826+1.47*C_L ns
t_r	S TO Q	0.844	1.56	1.63	1.82	0.583+1.74*C_L ns
t_f		1.13	2.09	2.18	2.45	0.903+1.53*C_L ns
t_f	S TO QB	1.08	1.99	2.07	2.32	0.852+1.49*C_L ns

Switching characteristics (Sheet 1 of 2)

JKFFRSP

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

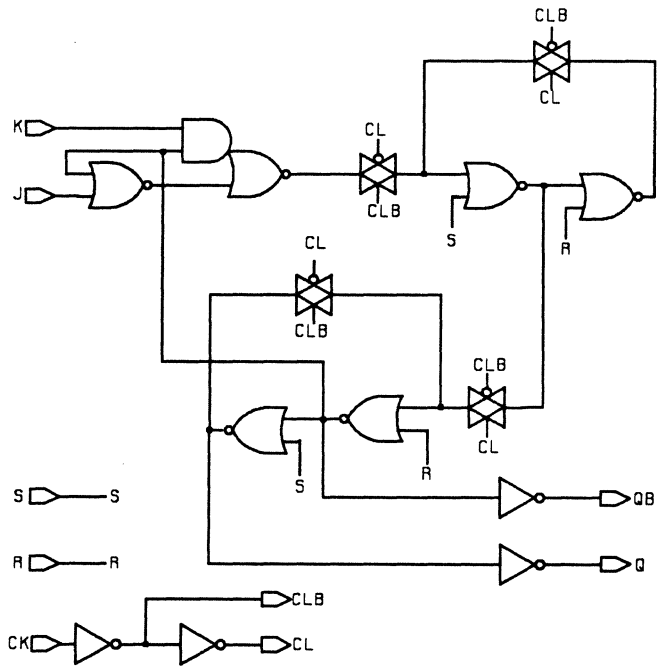
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_f	R TO Q	1.14	2.10	2.19	2.45	0.906+1.53*C_L ns
t_r	R TO QB	0.752	1.39	1.45	1.62	0.490+1.74*C_L ns
t_f		1.02	1.89	1.97	2.21	0.799+1.48*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time J to CK	3.75	ns
t_{su}	Setup Time K to CK	3.75	ns
t_h	Hold Time CK to J	−2.00	ns
t_h	Hold Time CK to K	−2.00	ns
t_{pwh}	High CK Pulse Width	6.00	ns
t_{pwh}	Set Pulse Width (high)	5.00	ns
t_{pwh}	Reset Pulse Width (high)	4.75	ns
t_{pwl}	Low CK Pulse Width	4.75	ns
rt	Set Recovery Time	0.25	ns
rt	Reset Recovery Time	−2.25	ns

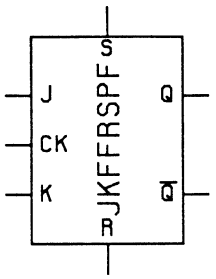
Timing requirements



Functional diagram: JKFFRSP

Fast J–K Flip–Flop with Set and Reset, Positive Edge Triggered

JKFFRSPF is a fully static JK–type edge triggered flip–flop. It is positive edge triggered with respect to CK. S and R are asynchronous and active high.



Inputs: CK, J, K, S, R
Outputs: Q, QB
Input Cap.: CK: 0.106
J: 0.107
K: 0.140
S: 0.107
R: 0.106 pF
Cell Size: 32 grids wide, 12 grids high

FUNCTION TABLE

J	K	CK	S	R	Q	QB
H	H	↑	L	L	QB_o	Q_o
H	L	↑	L	L	H	L
L	H	↑	L	L	L	H
L	L	↑	L	L	Q_o	QB_o
X	X	X	H	L	H	L
X	X	X	L	H	L	H
X	X	X	H	H	*	*

* Both Q and QB will be high as long as S and R are both high, but the output state is indeterminate if both S and R go low simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.84	3.41	3.55	3.99	1.71+0.880*C_L ns
t_{PHL}		1.67	3.08	3.21	3.60	1.55+0.753*C_L ns
t_{PLH}	CK TO QB	2.04	3.77	3.93	4.41	1.90+0.930*C_L ns
t_{PHL}		1.98	3.67	3.82	4.29	1.86+0.842*C_L ns
t_{PLH}	S TO Q	1.37	2.53	2.64	2.96	1.23+0.892*C_L ns
t_{PHL}		1.14	2.10	2.19	2.46	1.01+0.808*C_L ns
t_{PHL}	S TO QB	3.34	6.17	6.44	7.22	3.02+2.17*C_L ns
t_{PHL}	R TO Q	2.83	5.23	5.45	6.12	2.52+2.07*C_L ns
t_{PLH}	R TO QB	1.32	2.43	2.54	2.84	1.19+0.867*C_L ns
t_{PHL}		1.10	2.03	2.12	2.38	0.984+0.777*C_L ns
t_r	CK TO Q	0.865	1.60	1.67	1.87	0.593+1.81*C_L ns
t_f		0.792	1.46	1.52	1.71	0.586+1.37*C_L ns
t_r	CK TO QB	0.936	1.73	1.80	2.02	0.665+1.80*C_L ns
t_f		0.919	1.70	1.77	1.99	0.711+1.38*C_L ns
t_r	S TO Q	1.73	3.19	3.32	3.73	1.44+1.90*C_L ns

Switching characteristics (Sheet 1 of 2)

JKFFRSPF

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

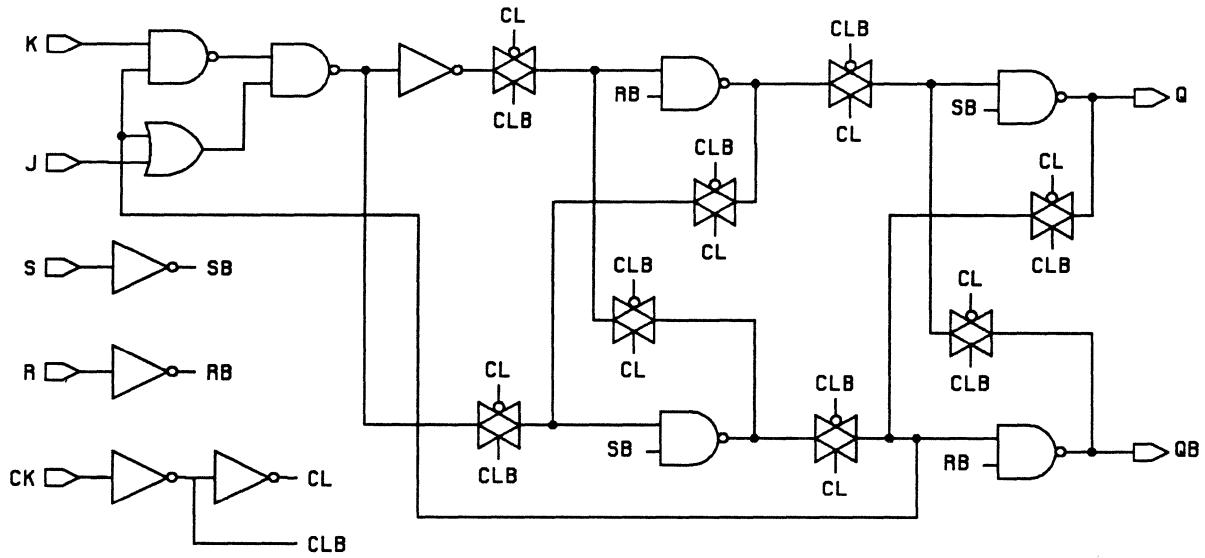
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_f		1.59	2.94	3.07	3.44	1.39+1.37*C_L ns
t_f	S TO QB	1.94	3.58	3.73	4.19	1.69+1.67*C_L ns
t_f	R TO Q	2.07	3.82	3.99	4.47	1.83+1.62*C_L ns
t_r	R TO QB	1.44	2.66	2.77	3.11	1.16+1.87*C_L ns
t_f		1.17	2.16	2.25	2.53	0.960+1.40*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time J to CK	3.25	ns
t_{su}	Setup Time K to CK	3.25	ns
t_h	Hold Time CK to J	-2.25	ns
t_h	Hold Time CK to K	-2.25	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwh}	Set Pulse Width (high)	6.50	ns
t_{pwh}	Reset Pulse Width (high)	6.00	ns
t_{pwl}	Low CK Pulse Width	4.25	ns
rt	Set Recovery Time	-1.75	ns
rt	Reset Recovery Time	-1.75	ns

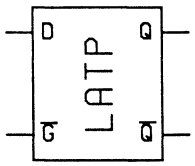
Timing requirements



Functional diagram: JKFFRSPF

Transparent Latch, Positive Edge Triggered

LATP holds data when GB is high and is transparent when GB is low. For a faster version of this cell, see LATPF.



Inputs: D, GB
Outputs: Q, QB
Input Cap.: D: 0.038
GB: 0.055 pF
Cell Size: 12 grids wide, 11 grids high

FUNCTION TABLE

D	GB	Q	QB
L	L	L	H
H	L	H	L
X	H	Q_o	QB_o

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	2.50	4.61	4.81	5.39	2.37+0.818*C_L ns
t_{PHL}		3.17	5.85	6.10	6.84	3.04+0.815*C_L ns
t_{PLH}	D TO QB	2.53	4.67	4.87	5.46	2.40+0.875*C_L ns
t_{PHL}		1.91	3.52	3.67	4.12	1.78+0.850*C_L ns
t_{PLH}	GB TO Q	2.90	5.36	5.59	6.27	2.78+0.828*C_L ns
t_{PHL}		3.55	6.55	6.83	7.66	3.42+0.803*C_L ns
t_{PLH}	GB TO QB	2.90	5.35	5.58	6.26	2.76+0.870*C_L ns
t_{PHL}		2.31	4.27	4.45	4.99	2.18+0.856*C_L ns
t_r	D TO Q	0.681	1.26	1.31	1.47	0.418+1.75*C_L ns
t_f		0.629	1.16	1.21	1.36	0.410+1.46*C_L ns
t_r	D TO QB	0.771	1.42	1.48	1.67	0.511+1.73*C_L ns
t_f		0.700	1.29	1.35	1.51	0.483+1.44*C_L ns
t_r	GB TO Q	0.693	1.28	1.33	1.50	0.430+1.75*C_L ns
t_f		0.622	1.15	1.20	1.34	0.402+1.47*C_L ns
t_r	GB TO QB	0.766	1.41	1.47	1.65	0.505+1.73*C_L ns
t_f		0.686	1.27	1.32	1.48	0.468+1.45*C_L ns

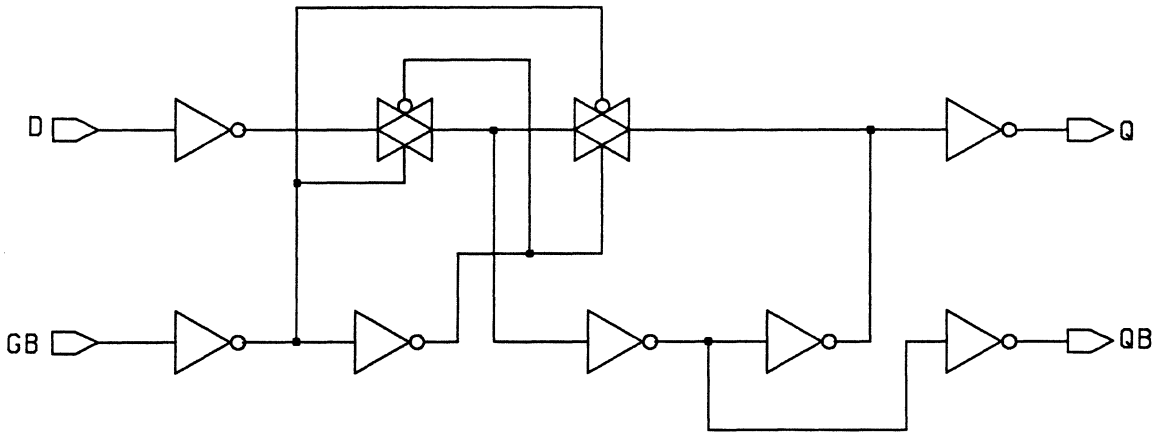
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.25	ns
t_h	Hold Time GB to D	−1.00	ns
t_{pwl}	GB Pulse Width (low)	5.00	ns

Timing requirements

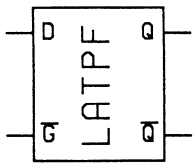
LATP



Functional diagram: LATP

Fast Transparent Latch, Positive Edge Triggered

LATPF holds data when GB is high and is transparent when GB is low.



Inputs: D, GB
Outputs: Q, QB
Input Cap.: D: 0.123
GB: 0.228 pF
Cell Size: 10 grids wide, 12 grids high

FUNCTION TABLE

D	GB	Q	QB
L	L	L	H
H	L	H	L
X	H	Q_o	QB_o

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.01	1.86	1.94	2.18	0.879+0.866*C_L ns
t_{PHL}		1.43	2.65	2.76	3.09	1.30+0.910*C_L ns
t_{PLH}	D TO QB	2.00	3.69	3.84	4.31	1.87+0.807*C_L ns
t_{PHL}		1.58	2.92	3.04	3.41	1.46+0.790*C_L ns
t_{PLH}	GB TO Q	1.39	2.56	2.67	2.99	1.25+0.875*C_L ns
t_{PHL}		1.53	2.82	2.94	3.30	1.39+0.911*C_L ns
t_{PLH}	GB TO QB	2.09	3.86	4.03	4.52	1.97+0.811*C_L ns
t_{PHL}		1.95	3.60	3.75	4.21	1.83+0.801*C_L ns
t_r	D TO Q	0.688	1.27	1.32	1.49	0.422+1.77*C_L ns
t_f		0.787	1.45	1.51	1.70	0.571+1.44*C_L ns
t_r	D TO QB	0.696	1.29	1.34	1.50	0.436+1.73*C_L ns
t_f		0.599	1.11	1.15	1.29	0.381+1.45*C_L ns
t_r	GB TO Q	0.700	1.29	1.35	1.51	0.436+1.76*C_L ns
t_f		0.802	1.48	1.54	1.73	0.587+1.43*C_L ns
t_r	GB TO QB	0.696	1.29	1.34	1.50	0.436+1.73*C_L ns
t_f		0.600	1.11	1.15	1.30	0.382+1.45*C_L ns

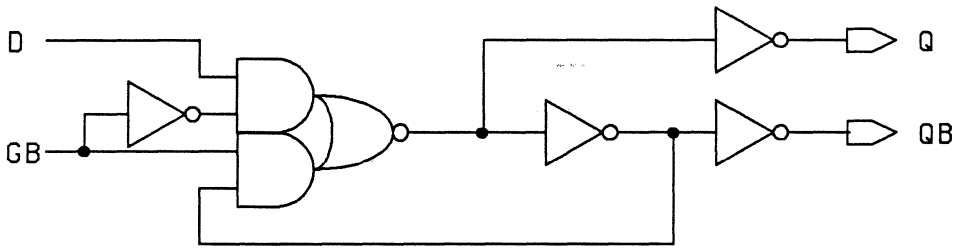
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.50	ns
t_h	Hold Time GB to D	−0.75	ns
t_{pwl}	GB Pulse Width (low)	4.50	ns

Timing requirements

LATPF

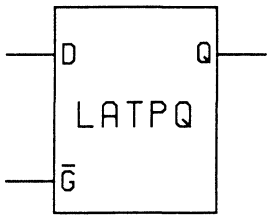


Functional diagram: LATPF

Transparent Latch, Positive Edge Triggered

LATPQ holds data when GB is high and is transparent when GB is low.

Inputs: D, GB
Outputs: Q
Input Cap.: D: 0.062
GB: 0.125 pF
Cell Size: 6 grids wide, 9.5 grids high



FUNCTION TABLE

D	GB	Q
L	L	L
H	L	H
X	H	Q_0

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.15	2.12	2.21	2.47	1.000+0.959*C_L ns
t_{PHL}		1.37	2.53	2.64	2.96	1.30+0.441*C_L ns
t_{PLH}	GB TO Q	1.38	2.55	2.66	2.98	1.24+0.959*C_L ns
t_{PHL}		1.24	2.30	2.39	2.69	1.09+0.987*C_L ns
t_r	D TO Q	0.752	1.39	1.45	1.63	0.464+1.92*C_L ns
t_f		0.730	1.35	1.41	1.58	0.511+1.46*C_L ns
t_r	GB TO Q	0.762	1.41	1.47	1.64	0.474+1.92*C_L ns
t_f		0.720	1.33	1.39	1.55	0.479+1.60*C_L ns

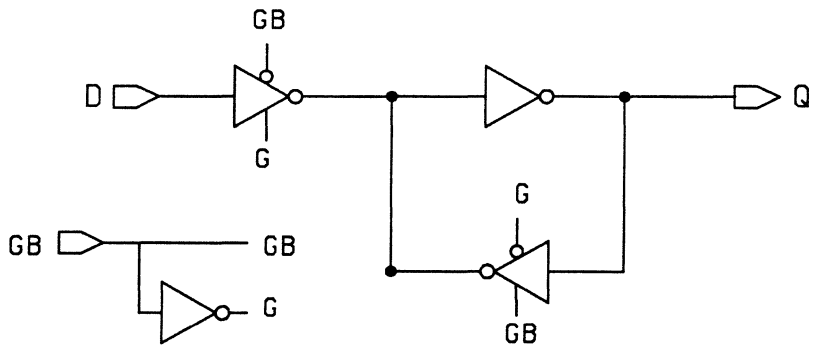
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.00	ns
t_h	Hold Time GB to D	−1.00	ns
t_{pwl}	GB Pulse Width (low)	4.00	ns

Timing requirements

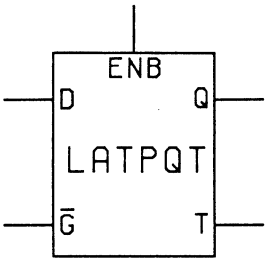
LATPQ



Functional diagram: LATPQ

Transparent Latch with Tristate, Positive Edge Triggered

LATPQT holds data when GB is high and is transparent when GB is low. When ENB is high, the T output is in a Hi–Z state and Q functions as a normal latch using any of the given states defined for Q in the FUNCTION TABLE.



Inputs: ENB, D, GB
Outputs: Q, T
Input Cap.: ENB: 0.121
D: 0.063
GB: 0.126 pF
Output Cap.: Q: 0.000
T: 0.131 pF
Cell Size: 9 grids wide, 10 grids high

FUNCTION TABLE

D	GB	ENB	Q	T
L	L	L	L	L
H	L	L	H	H
X	H	L	Q_o	T_o
L	L	H	L	HiZ
H	L	H	H	HiZ
X	H	H	Q_o	HiZ

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.45	2.68	2.79	3.13	1.29+1.04*C_L ns
t_{PHL}		1.71	3.15	3.28	3.69	1.57+0.897*C_L ns
t_{PLH}	D TO T	1.65	3.04	3.17	3.56	1.40+1.62*C_L ns
t_{PHL}		1.78	3.29	3.43	3.85	1.61+1.17*C_L ns
t_{PLH}	GB TO Q	1.73	3.20	3.34	3.74	1.58+1.04*C_L ns
t_{PHL}		1.74	3.21	3.34	3.75	1.58+1.05*C_L ns
t_{PLH}	GB TO T	1.92	3.54	3.69	4.14	1.67+1.62*C_L ns
t_{PHL}		1.66	3.06	3.19	3.58	1.46+1.33*C_L ns
t_{PLH}	ENB TO T	0.590	1.09	1.14	1.27	0.320+1.80*C_L ns
t_{PHL}		0.853	1.58	1.64	1.84	0.643+1.40*C_L ns
t_r	D TO Q	0.920	1.70	1.77	1.99	0.620+1.99*C_L ns
t_f		0.905	1.67	1.74	1.95	0.665+1.59*C_L ns
t_r	D TO T	1.30	2.41	2.51	2.82	0.784+3.46*C_L ns
t_f		1.16	2.14	2.23	2.50	0.785+2.47*C_L ns
t_r	GB TO Q	0.926	1.71	1.78	2.00	0.625+2.00*C_L ns
t_f		0.911	1.68	1.75	1.97	0.671+1.59*C_L ns
t_r	GB TO T	1.31	2.42	2.52	2.83	0.788+3.46*C_L ns
t_f		1.16	2.14	2.23	2.50	0.786+2.47*C_L ns
t_r	ENB TO T	1.14	2.10	2.19	2.46	0.606+3.55*C_L ns
t_f		0.991	1.83	1.91	2.14	0.613+2.52*C_L ns

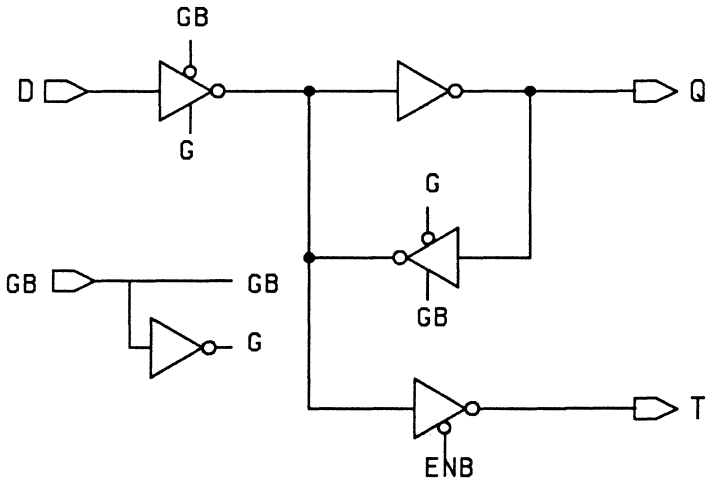
Switching characteristics

LATPQT

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.75	ns
t_h	Hold Time GB to D	−1.25	ns
t_{pwl}	GB Pulse Width (low)	4.75	ns

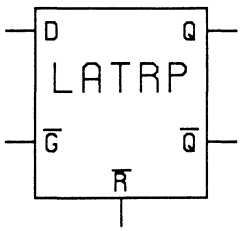
Timing requirements



Functional diagram: LATPQT

Transparent Latch with Reset, Positive Edge Triggered

LATRP holds data when GB is high and is transparent when GB is low. RB is asynchronous, and active low. For a faster version of this cell, see LATRPF.



Inputs: RB, D, GB
Outputs: Q, QB
Input Cap.: RB: 0.055
D: 0.038
GB: 0.055 pF
Cell Size: 14 grids wide, 12 grids high

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q_o	QB_o
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	3.13	5.79	6.03	6.77	3.01+0.811*C_L ns
t_{PHL}		3.29	6.08	6.34	7.12	3.16+0.851*C_L ns
t_{PLH}	D TO QB	2.18	4.03	4.20	4.71	2.06+0.825*C_L ns
t_{PHL}		2.58	4.76	4.96	5.57	2.43+0.980*C_L ns
t_{PLH}	GB TO Q	3.53	6.53	6.80	7.63	3.41+0.794*C_L ns
t_{PHL}		3.62	6.69	6.97	7.82	3.49+0.873*C_L ns
t_{PLH}	GB TO QB	2.51	4.64	4.84	5.42	2.38+0.838*C_L ns
t_{PHL}		2.98	5.50	5.74	6.44	2.83+0.963*C_L ns
t_{PLH}	RB TO Q	2.85	5.27	5.50	6.17	2.73+0.810*C_L ns
t_{PHL}		3.14	5.79	6.04	6.77	2.99+0.972*C_L ns
t_{PLH}	RB TO QB	1.33	2.45	2.55	2.87	1.20+0.829*C_L ns
t_{PHL}		2.30	4.24	4.42	4.96	2.15+0.980*C_L ns
t_r	D TO Q	0.741	1.37	1.43	1.60	0.483+1.72*C_L ns
t_f		0.810	1.50	1.56	1.75	0.594+1.44*C_L ns
t_r	D TO QB	0.698	1.29	1.34	1.51	0.438+1.73*C_L ns
t_f		0.903	1.67	1.74	1.95	0.678+1.49*C_L ns
t_r	GB TO Q	0.756	1.40	1.46	1.63	0.500+1.70*C_L ns
t_f		0.804	1.48	1.55	1.74	0.587+1.44*C_L ns
t_r	GB TO QB	0.679	1.25	1.31	1.47	0.417+1.75*C_L ns
t_f		0.927	1.71	1.79	2.00	0.706+1.47*C_L ns
t_r	RB TO Q	0.737	1.36	1.42	1.59	0.478+1.72*C_L ns
t_f		1.01	1.87	1.95	2.19	0.787+1.51*C_L ns
t_r	RB TO QB	0.622	1.15	1.20	1.34	0.356+1.77*C_L ns
t_f		0.898	1.66	1.73	1.94	0.674+1.49*C_L ns

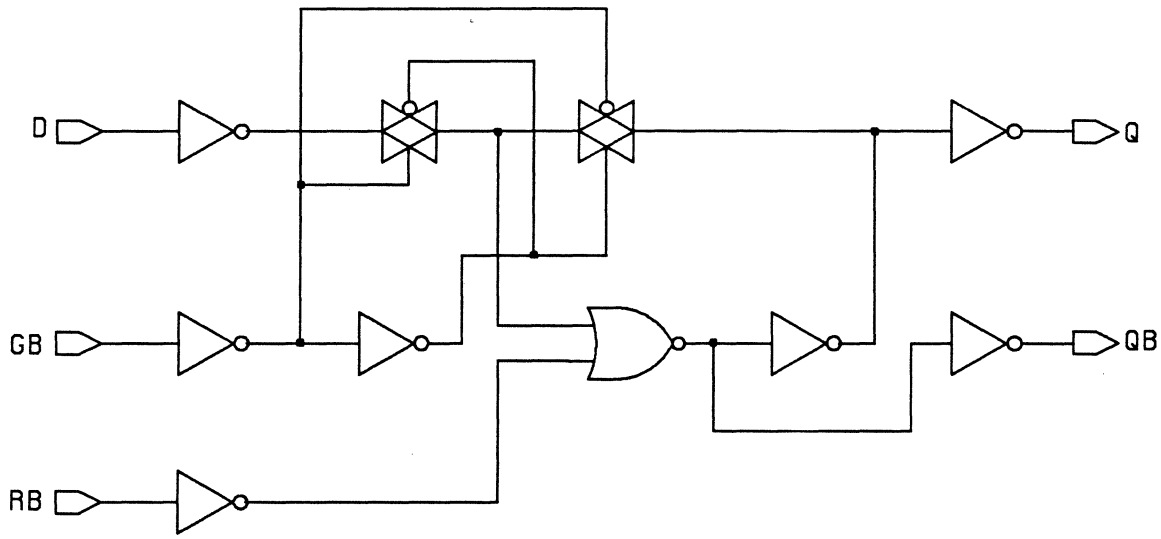
Switching characteristics

LATRP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.25	ns
t_h	Hold Time GB to D	−1.50	ns
t_{pwl}	RB Pulse Width (low)	4.00	ns
t_{pwl}	GB Pulse Width (low)	4.75	ns
rt	RB Recovery Time	1.75	ns

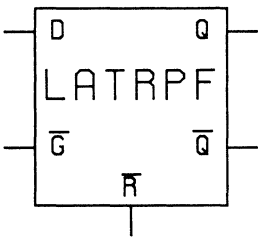
Timing requirements



Functional diagram: LATRP

Fast Transparent Latch with Reset, Positive Edge Triggered

LATRPF holds data when GB is high and is transparent when GB is low. RB is asynchronous, and active low.



Inputs: RB, D, GB
Outputs: Q, QB
Input Cap.: RB: 0.176
D: 0.122
GB: 0.229 pF
Cell Size: 12 grids wide, 12 grids high

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q_o	QB_o
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.19	2.20	2.29	2.57	1.05+0.921*C_L ns
t_{PHL}		1.49	2.76	2.88	3.23	1.35+0.924*C_L ns
t_{PLH}	D TO QB	2.07	3.82	3.98	4.46	1.95+0.802*C_L ns
t_{PHL}		1.78	3.29	3.43	3.85	1.66+0.817*C_L ns
t_{PLH}	GB TO Q	1.62	2.99	3.11	3.49	1.48+0.919*C_L ns
t_{PHL}		1.57	2.90	3.03	3.40	1.43+0.921*C_L ns
t_{PLH}	GB TO QB	2.13	3.94	4.11	4.61	2.01+0.812*C_L ns
t_{PHL}		2.19	4.05	4.22	4.74	2.07+0.793*C_L ns
t_{PLH}	RB TO Q	1.21	2.24	2.34	2.62	1.08+0.913*C_L ns
t_{PHL}		2.40	4.44	4.63	5.19	2.26+0.941*C_L ns
t_{PLH}	RB TO QB	3.01	5.56	5.80	6.50	2.89+0.804*C_L ns
t_{PHL}		1.80	3.33	3.47	3.90	1.68+0.813*C_L ns
t_r	D TO Q	0.762	1.41	1.47	1.65	0.497+1.77*C_L ns
t_f		0.796	1.47	1.53	1.72	0.578+1.45*C_L ns
t_r	D TO QB	0.703	1.30	1.35	1.52	0.444+1.73*C_L ns
t_f		0.617	1.14	1.19	1.33	0.399+1.45*C_L ns
t_r	GB TO Q	0.779	1.44	1.50	1.68	0.515+1.76*C_L ns
t_f		0.827	1.53	1.59	1.79	0.612+1.43*C_L ns
t_r	GB TO QB	0.710	1.31	1.37	1.53	0.452+1.72*C_L ns
t_f		0.613	1.13	1.18	1.33	0.397+1.44*C_L ns
t_r	RB TO Q	0.781	1.44	1.50	1.69	0.518+1.75*C_L ns
t_f		1.23	2.27	2.37	2.66	1.04+1.23*C_L ns

Switching characteristics (Sheet 1 of 2)

LATRPF

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

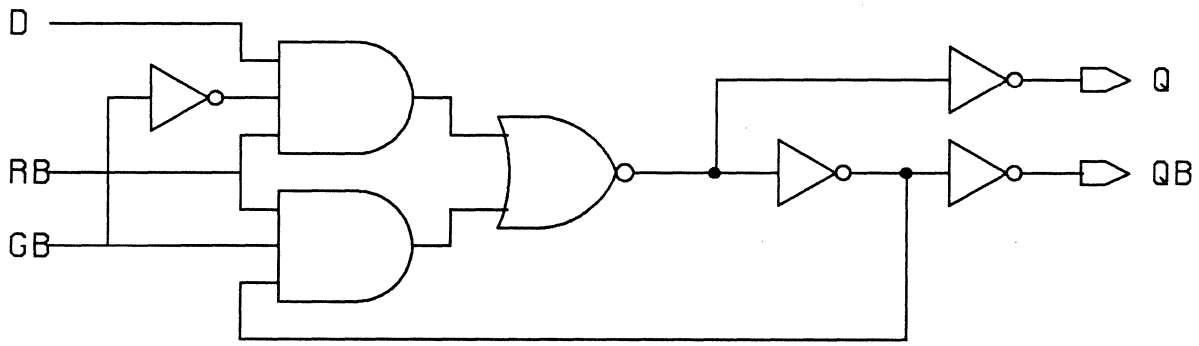
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_r	RB TO QB	0.727	1.34	1.40	1.57	0.470+1.71*C_L ns
t_f		0.612	1.13	1.18	1.32	0.393+1.46*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.50	ns
t_h	Hold Time GB to D	−1.00	ns
t_{pwl}	RB Pulse Width (low)	6.00	ns
t_{pwl}	GB Pulse Width (low)	4.50	ns
rt	RB Recovery Time	1.25	ns

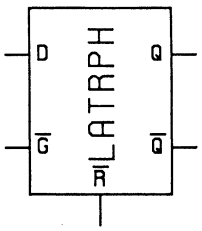
Timing requirements



Functional diagram: LATRPF

D Latch with Reset and Enable (High Drive)

LATRPH holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.



Inputs: D, GB, RB
Outputs: Q, QB
Input Cap.: D: 0.139
GB: 0.054
RB: 0.278 pF
Cell Size: 19 grids wide, 12 grids high

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q_o	QB_o
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	2.48	4.57	4.77	5.35	2.39+0.541*C_L ns
t_{PHL}		2.79	5.15	5.37	6.02	2.70+0.551*C_L ns
t_{PLH}	GB TO Q	2.79	5.16	5.38	6.03	2.71+0.551*C_L ns
t_{PHL}		3.19	5.90	6.15	6.90	3.11+0.540*C_L ns
t_{PLH}	RB TO Q	2.47	4.57	4.76	5.35	2.39+0.543*C_L ns
t_{PHL}		1.16	2.15	2.24	2.51	1.07+0.634*C_L ns
t_{PLH}	D TO QB	2.11	3.90	4.07	4.56	2.01+0.641*C_L ns
t_{PHL}		2.00	3.69	3.84	4.31	1.89+0.668*C_L ns
t_{PLH}	GB TO QB	2.52	4.66	4.85	5.45	2.43+0.629*C_L ns
t_{PHL}		2.32	4.28	4.46	5.00	2.21+0.676*C_L ns
t_{PLH}	RB TO QB	2.53	4.67	4.86	5.46	2.44+0.589*C_L ns
t_{PHL}		2.00	3.69	3.84	4.31	1.89+0.670*C_L ns
t_r	D TO Q	0.585	1.08	1.13	1.26	0.418+1.11*C_L ns
t_f		0.517	0.955	0.995	1.12	0.372+0.961*C_L ns
t_r	GB TO Q	0.584	1.08	1.12	1.26	0.416+1.11*C_L ns
t_f		0.522	0.965	1.01	1.13	0.379+0.952*C_L ns
t_r	RB TO Q	0.585	1.08	1.13	1.26	0.418+1.11*C_L ns
t_f		0.583	1.08	1.12	1.26	0.436+0.976*C_L ns
t_r	D TO QB	0.731	1.35	1.41	1.58	0.563+1.12*C_L ns
t_f		0.699	1.29	1.35	1.51	0.551+0.982*C_L ns
t_r	GB TO QB	0.730	1.35	1.41	1.58	0.563+1.11*C_L ns
t_f		0.685	1.26	1.32	1.48	0.536+0.988*C_L ns
t_r	RB TO QB	0.660	1.22	1.27	1.43	0.490+1.13*C_L ns
t_f		0.699	1.29	1.35	1.51	0.552+0.982*C_L ns

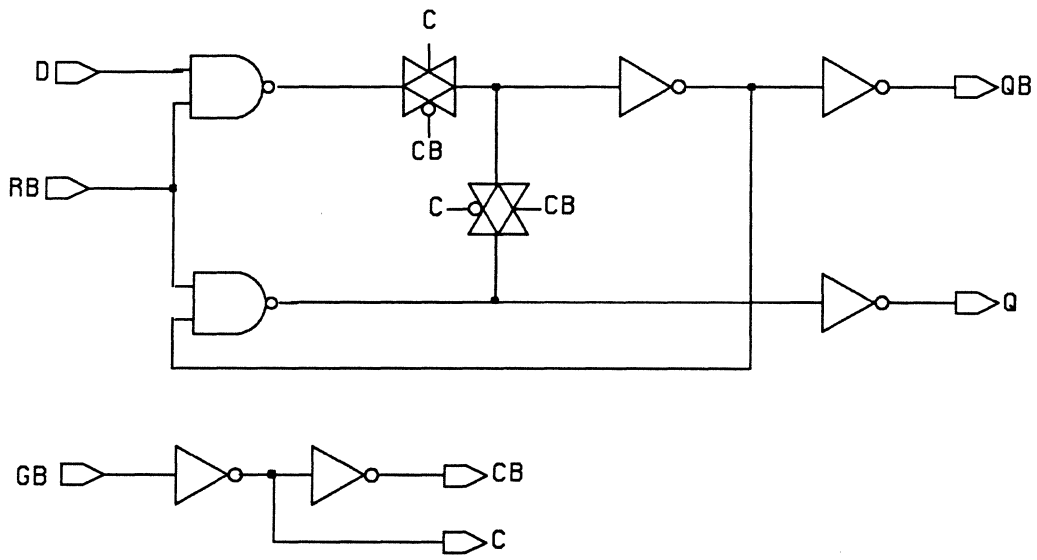
Switching characteristics

LATRPH

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	1.75	ns
t_h	Hold Time GB to D	−1.25	ns
t_{pwl}	GB Pulse Width (low)	4.50	ns
t_{pwl}	RB Pulse Width (low)	4.75	ns
rt	RB Recovery Time	1.50	ns

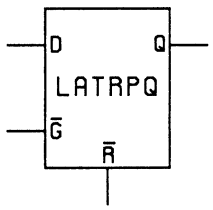
Timing requirements



Functional diagram: LATRPH

Transparent Latch with Reset, Positive Edge Triggered

LATRPQ holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.



Inputs: D, GB, RB
Outputs: Q
Input Cap.: D: 0.065
GB: 0.107
RB: 0.055 pF
Cell Size: 8 grids wide, 10 grids high

FUNCTION TABLE

D	GB	RB	Q
L	L	H	L
H	L	H	H
X	H	H	Q_o
X	X	L	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.11	2.06	2.14	2.40	0.899+1.42*C_L ns
t_{PHL}		1.66	3.06	3.19	3.58	1.49+1.07*C_L ns
t_{PLH}	GB TO Q	1.41	2.61	2.72	3.05	1.19+1.43*C_L ns
t_{PHL}		1.48	2.72	2.84	3.19	1.31+1.08*C_L ns
t_{PLH}	RB TO Q	1.11	2.05	2.13	2.39	0.897+1.40*C_L ns
t_{PHL}		1.14	2.11	2.20	2.47	0.982+1.07*C_L ns
t_r	D TO Q	1.11	2.05	2.14	2.40	0.657+3.02*C_L ns
t_f		0.877	1.62	1.69	1.89	0.613+1.76*C_L ns
t_r	GB TO Q	1.12	2.07	2.16	2.42	0.667+3.02*C_L ns
t_f		0.872	1.61	1.68	1.88	0.607+1.77*C_L ns
t_r	RB TO Q	1.10	2.03	2.11	2.37	0.643+3.03*C_L ns
t_f		0.867	1.60	1.67	1.87	0.572+1.96*C_L ns

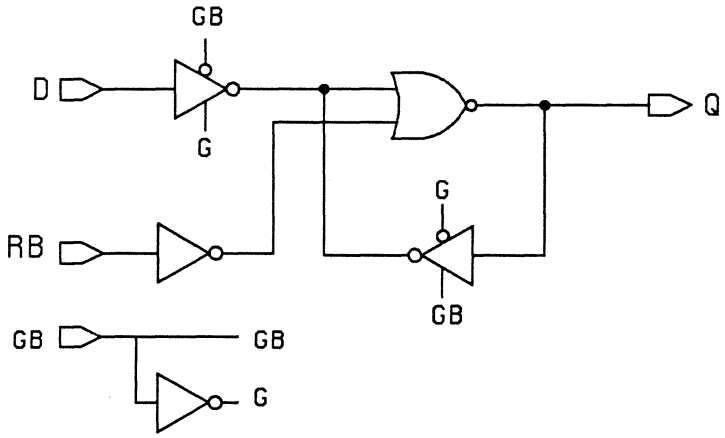
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.75	ns
t_h	Hold Time GB to D	−0.50	ns
t_{pwl}	GB Pulse Width (low)	4.25	ns
t_{pwl}	RB Pulse Width (low)	5.25	ns
rt	RB Recovery Time	0.25	ns

Timing requirements

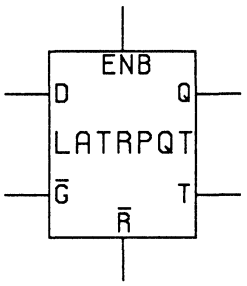
LATRPQ



Functional diagram: LATRPQ

Transparent Latch with Reset and Tristate, Positive Edge Triggered

LATRPQT holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low. When ENB is high, the T output is in a Hi-Z state and Q functions as a normal latch using any of the given states defined for Q in the FUNCTION TABLE.



Inputs: ENB, D, GB, RB
Outputs: Q, T
Input Cap.: ENB: 0.121
D: 0.055
GB: 0.123
RB: 0.055 pF
Output Cap.: Q: 0.000
T: 0.135 pF
Cell Size: 13 grids wide, 10 grids high

FUNCTION TABLE

D	GB	RB	ENB	Q	T
L	L	H	L	L	L
H	L	H	L	H	H
X	H	H	L	Q_o	T_o
X	X	L	L	L	L
L	L	H	H	L	HiZ
H	L	H	H	H	HiZ
X	H	H	H	Q_o	HiZ
X	X	L	H	L	HiZ

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.42	2.63	2.74	3.07	1.20+1.49*C_L ns
t_{PHL}		1.58	2.92	3.04	3.42	1.44+0.945*C_L ns
t_{PLH}	D TO T	2.61	4.81	5.02	5.63	2.11+3.31*C_L ns
t_{PHL}		2.78	5.14	5.36	6.01	2.40+2.56*C_L ns
t_{PLH}	GB TO Q	1.67	3.08	3.21	3.60	1.44+1.49*C_L ns
t_{PHL}		1.45	2.68	2.80	3.14	1.29+1.07*C_L ns
t_{PLH}	GB TO T	2.85	5.27	5.49	6.16	2.36+3.31*C_L ns
t_{PHL}		2.65	4.90	5.11	5.73	2.25+2.69*C_L ns
t_{PLH}	RB TO Q	1.14	2.10	2.19	2.46	0.917+1.46*C_L ns
t_{PHL}		1.20	2.21	2.30	2.58	1.02+1.19*C_L ns
t_{PLH}	RB TO T	2.32	4.28	4.47	5.01	1.83+3.27*C_L ns
t_{PHL}		2.44	4.51	4.70	5.28	2.01+2.89*C_L ns
t_{PLH}	ENB TO T	0.548	1.01	1.05	1.18	0.147+2.67*C_L ns
t_{PHL}		0.827	1.53	1.59	1.79	0.527+2.00*C_L ns
t_r	D TO Q	1.33	2.46	2.57	2.88	0.863+3.13*C_L ns
t_f		0.881	1.63	1.70	1.90	0.610+1.80*C_L ns
t_r	D TO T	1.17	2.16	2.25	2.53	0.640+3.53*C_L ns
t_f		0.958	1.77	1.84	2.07	0.576+2.54*C_L ns
t_r	GB TO Q	1.33	2.46	2.57	2.88	0.866+3.12*C_L ns
t_f		0.875	1.62	1.69	1.89	0.604+1.81*C_L ns

Switching characteristics (Sheet 1 of 2)

LATRPQT

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

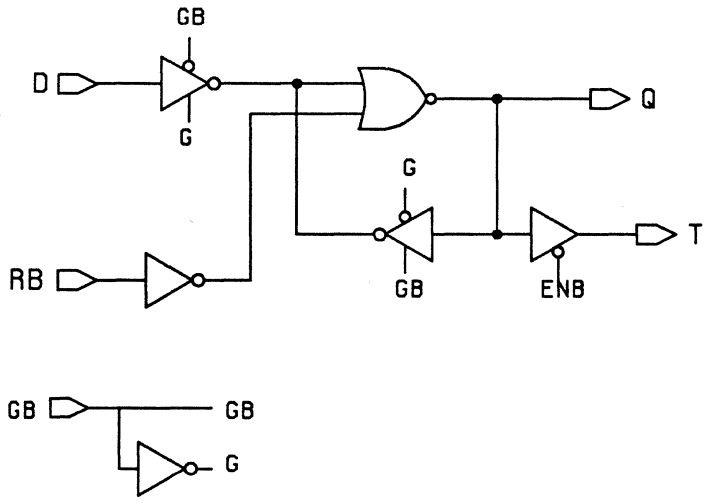
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_r	GB TO T	1.17	2.16	2.25	2.53	0.640+3.53*C_L ns
t_f		0.958	1.77	1.84	2.07	0.576+2.54*C_L ns
t_r	RB TO Q	1.26	2.34	2.44	2.73	0.789+3.17*C_L ns
t_f		0.989	1.83	1.90	2.14	0.650+2.26*C_L ns
t_r	RB TO T	1.17	2.16	2.25	2.53	0.640+3.53*C_L ns
t_f		0.960	1.77	1.85	2.07	0.578+2.54*C_L ns
t_r	ENB TO T	1.14	2.11	2.19	2.46	0.606+3.55*C_L ns
t_f		0.950	1.75	1.83	2.05	0.568+2.54*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.75	ns
t_h	Hold Time GB to D	−1.50	ns
t_{pwl}	GB Pulse Width (low)	4.50	ns
t_{pwl}	RB Pulse Width (low)	4.75	ns
rt	RB Recovery Time	0.00	ns
rt		1.50	ns

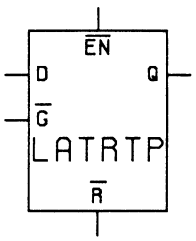
Timing requirements



Functional diagram: LATRPQT

Transparent Latch with Reset, Tristate, Positive Edge Triggered

LATRTP holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low. When ENB is high, the output is in a Hi-Z state.



Inputs: ENB, D, GB, RB
Outputs: Q
Input Cap.: ENB: 0.126
D: 0.038
GB: 0.056
RB: 0.055 pF
Output Cap.: Q: 0.095 pF
Cell Size: 16 grids wide, 12 grids high

FUNCTION TABLE

D	GB	RB	ENB	Q
L	L	H	L	L
H	L	H	L	H
X	H	H	L	Q_o
X	X	L	L	L
X	H	H	L	Z
X	X	X	H	Z

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	3.03	5.60	5.84	6.55	2.80+1.55*C_L ns
t_{PHL}		3.25	6.01	6.26	7.03	3.04+1.38*C_L ns
t_{PLH}	RB TO Q	2.76	5.09	5.31	5.96	2.52+1.55*C_L ns
t_{PHL}		2.57	4.75	4.95	5.55	2.36+1.38*C_L ns
t_{PLH}	GB TO Q	3.44	6.36	6.63	7.44	3.21+1.53*C_L ns
t_{PHL}		3.78	6.97	7.27	8.15	3.57+1.37*C_L ns
t_{PLH}	ENB TO Q	0.633	1.17	1.22	1.37	0.393+1.60*C_L ns
t_{PHL}		0.938	1.73	1.81	2.03	0.726+1.41*C_L ns
t_r	D TO Q	1.44	2.67	2.78	3.12	0.930+3.42*C_L ns
t_f		1.39	2.56	2.67	2.99	0.991+2.63*C_L ns
t_r	RB TO Q	1.43	2.64	2.76	3.09	0.917+3.42*C_L ns
t_f		1.39	2.57	2.68	3.01	0.997+2.62*C_L ns
t_r	GB TO Q	1.44	2.65	2.76	3.10	0.922+3.42*C_L ns
t_f		1.39	2.57	2.68	3.00	0.997+2.61*C_L ns
t_r	ENB TO Q	1.22	2.25	2.35	2.64	0.690+3.53*C_L ns
t_f		1.20	2.22	2.31	2.60	0.786+2.77*C_L ns

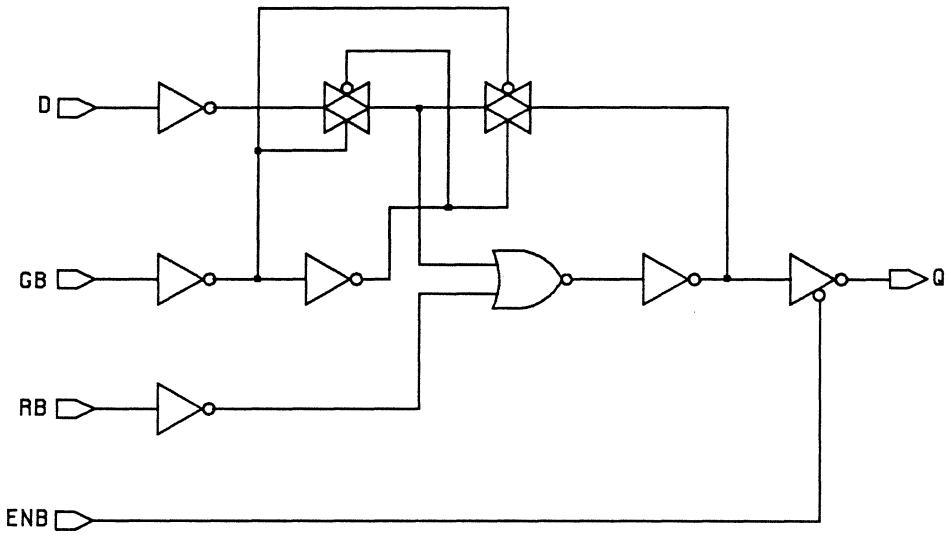
Switching characteristics

LATRTP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	1.50	ns
t_h	Hold Time GB to D	−1.25	ns
t_{pwl}	GB Pulse Width (low)	4.25	ns
t_{pwl}	RB Pulse Width (low)	3.75	ns
rt	RB Recovery Time	0.00	ns
rt		1.00	ns

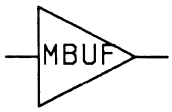
Timing requirements



Functional diagram: LATRTP

Medium Drive Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.055 pF
Cell Size: 3 grids wide, 11 grids high



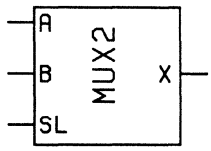
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.975	1.80	1.88	2.11	0.851+0.821*C_L ns
t_{PHL}		1.06	1.95	2.03	2.28	0.936+0.798*C_L ns
t_r	A TO X	0.649	1.20	1.25	1.40	0.384+1.77*C_L ns
t_f		0.630	1.16	1.21	1.36	0.413+1.45*C_L ns

Switching characteristics

2–Input Multiplexer

Inputs: SL, A, B
Outputs: X
Input Cap.: SL: 0.144
A, B: 0.089 pF
Cell Size: 9 grids wide, 12 grids high



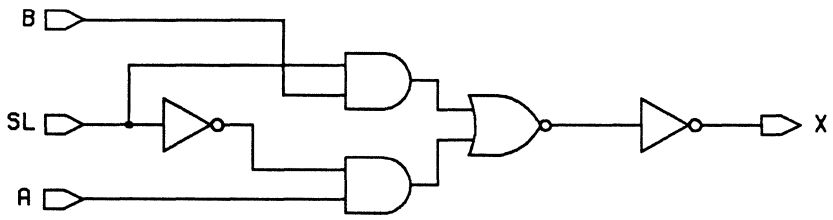
FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.36	2.52	2.63	2.95	1.11+1.67*C_L ns
t_{PHL}		1.34	2.47	2.58	2.89	1.09+1.61*C_L ns
t_{PLH}	SL TO X	1.20	2.22	2.31	2.59	0.949+1.67*C_L ns
t_{PHL}		1.52	2.81	2.93	3.29	1.28+1.64*C_L ns
t_r	*IN TO X	0.969	1.79	1.87	2.09	0.428+3.61*C_L ns
t_f		0.876	1.62	1.69	1.89	0.421+3.03*C_L ns
t_r	SL TO X	0.943	1.74	1.82	2.04	0.399+3.63*C_L ns
t_f		0.911	1.68	1.75	1.97	0.457+3.02*C_L ns
* Slowest of A or B inputs						

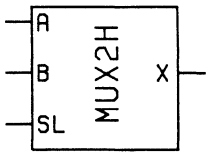
Switching characteristics



Functional diagram: MUX2

2–Input Multiplexer (High Drive)

Inputs: A, SL, B
Outputs: X
Input Cap.: A: 0.106
SL: 0.163
B: 0.105 pF
Cell Size: 8 grids wide, 12 grids high



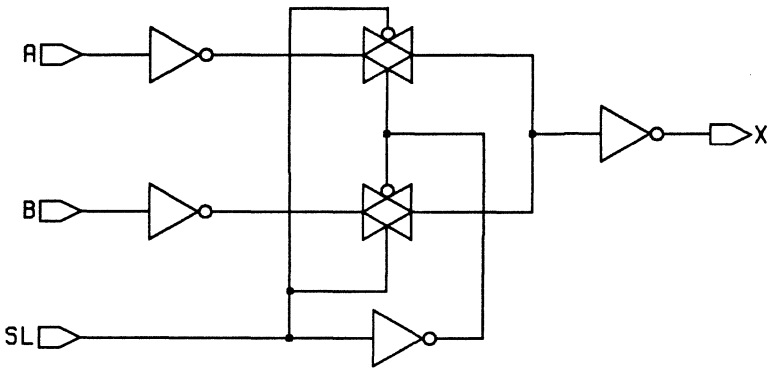
FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.17	2.16	2.25	2.52	1.07+0.626*C_L ns
t_{PHL}		1.26	2.33	2.43	2.73	1.16+0.650*C_L ns
t_{PLH}	SL TO X	1.04	1.91	1.99	2.24	0.941+0.630*C_L ns
t_{PHL}		1.16	2.15	2.24	2.51	1.06+0.658*C_L ns
t_r	*IN TO X	0.635	1.17	1.22	1.37	0.461+1.15*C_L ns
t_f		0.684	1.26	1.32	1.48	0.539+0.967*C_L ns
t_r	SL TO X	0.629	1.16	1.21	1.36	0.455+1.16*C_L ns
t_f		0.657	1.21	1.26	1.42	0.509+0.987*C_L ns
* Slowest of A or B inputs						

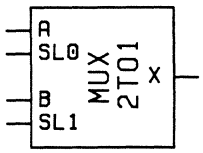
Switching characteristics



Functional diagram: MUX2H

2–Input Multiplexer with Separate Selects

In normal operation, SL1 and SL0 are complementary signals and X = A when SL0 is high, and X = B when SL1 is high.



Inputs: SL1, SL0, A, B
Outputs: X
Input Cap.: All: 0.088 pF
Cell Size: 7 grids wide, 10 grids high

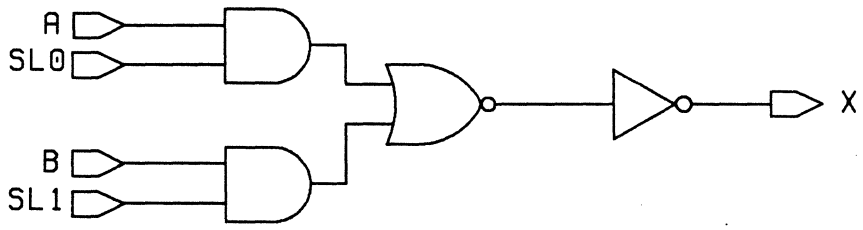
FUNCTION TABLE

SL1	SL0	X
L	L	L
L	H	A
H	L	B
H	H	A + B

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A,B TO X	1.36	2.51	2.62	2.94	1.11+1.67*C_L ns
t_{PHL}		1.34	2.47	2.57	2.89	1.10+1.60*C_L ns
t_{PLH}	*SL TO X	1.35	2.50	2.61	2.93	1.10+1.67*C_L ns
t_{PHL}		1.45	2.67	2.78	3.12	1.20+1.62*C_L ns
t_r	A,B TO X	0.964	1.78	1.86	2.08	0.424+3.60*C_L ns
t_f		0.874	1.61	1.68	1.89	0.421+3.02*C_L ns
t_r	*SL TO X	0.961	1.78	1.85	2.08	0.421+3.60*C_L ns
t_f		0.896	1.66	1.73	1.94	0.444+3.01*C_L ns
* SL timing applies to both SL0 and SL1						

Switching characteristics

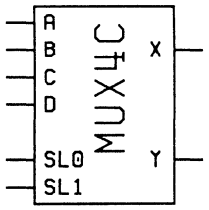


Functional diagram: MUX2TO1

4–Input Multiplexer with Complementary Outputs

SL0 and SL1 cause one of A, B, C, or D to be propagated to the outputs.

Inputs: A, B, C, D, SL0, SL1
Outputs: X, Y
Input Cap.: A, B, C: 0.088
D: 0.089
SL0, SL1: 0.055 pF
Cell Size: 22 grids wide, 12 grids high



FUNCTION TABLE

SL0	SL1	X	Y
L	L	A	$\bar{A}$
H	L	B	$\bar{B}$
L	H	C	$\bar{C}$
H	H	D	$\bar{D}$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

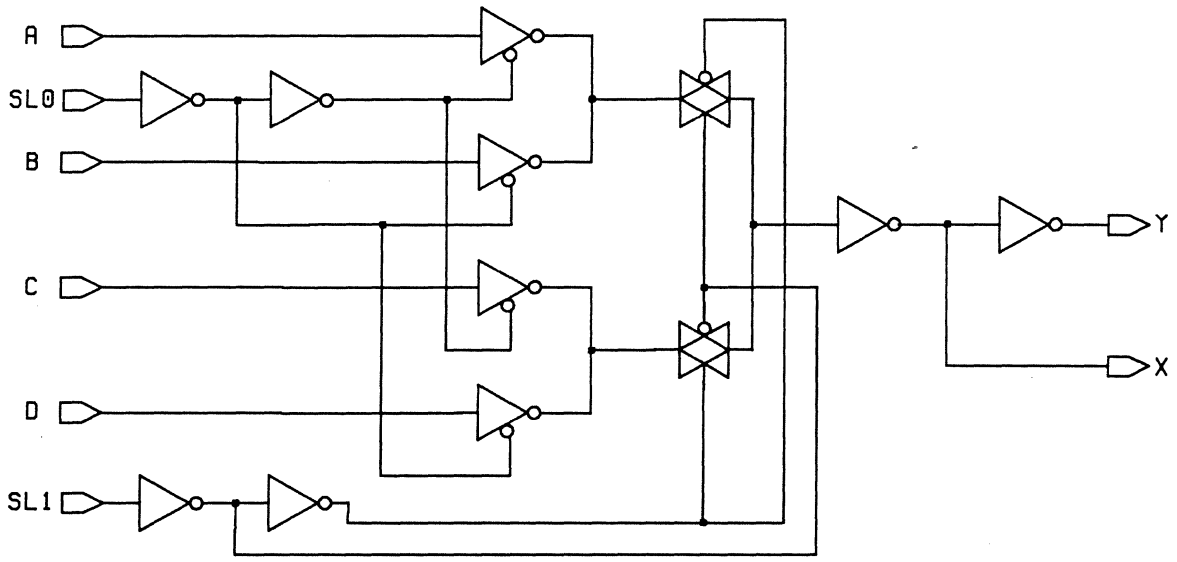
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.82	3.37	3.51	3.94	1.57+1.69*C_L ns
t_{PHL}		2.30	4.26	4.44	4.98	2.05+1.68*C_L ns
t_{PLH}	X TO Y	0.465	0.858	0.894	1.000	0.220+1.63*C_L ns
t_{PHL}		0.539	0.996	1.04	1.16	0.307+1.55*C_L ns
t_{PLH}	**SL TO X	2.07	3.83	3.99	4.48	1.82+1.69*C_L ns
t_{PHL}		2.31	4.26	4.44	4.98	2.05+1.68*C_L ns
t_{PLH}	X TO Y	0.465	0.859	0.895	1.000	0.218+1.65*C_L ns
t_{PHL}		0.547	1.01	1.05	1.18	0.313+1.56*C_L ns
t_{PLH}	*IN TO Y	2.52	4.65	4.85	5.44	2.27+1.63*C_L ns
t_{PHL}		2.11	3.89	4.06	4.55	1.88+1.55*C_L ns
t_{PLH}	**SL TO Y	2.28	4.22	4.40	4.93	2.04+1.65*C_L ns
t_{PHL}		2.60	4.81	5.01	5.62	2.37+1.56*C_L ns
t_r	*IN TO X	1.41	2.60	2.71	3.04	0.874+3.56*C_L ns
t_f		1.47	2.72	2.83	3.18	1.03+2.92*C_L ns
t_r	X TO Y	0.932	1.72	1.79	2.01	0.390+3.61*C_L ns
t_f		0.804	1.48	1.55	1.74	0.348+3.04*C_L ns
t_r	**SL TO X	1.37	2.53	2.63	2.95	0.830+3.58*C_L ns
t_f		1.34	2.48	2.58	2.90	0.893+2.99*C_L ns
t_r	X TO Y	0.912	1.68	1.76	1.97	0.369+3.62*C_L ns
t_f		0.785	1.45	1.51	1.70	0.327+3.05*C_L ns
t_r	*IN TO Y	0.932	1.72	1.79	2.01	0.390+3.61*C_L ns
t_f		0.804	1.48	1.55	1.74	0.348+3.04*C_L ns
t_r	**SL TO Y	0.912	1.68	1.76	1.97	0.369+3.62*C_L ns
t_f		0.785	1.45	1.51	1.70	0.327+3.05*C_L ns

* Slowest of A,B,C, or D inputs
** SL timing applies to both SL0 and SL1

Switching characteristics

MUX4C

NOTE:
The propagation delay for Y is dependent upon the X output delay and rise time. The delays listed and the delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.



Functional diagram: MUX4C

2–Input NAND Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.072 pF
Cell Size: 3 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.755	1.39	1.45	1.63	0.508+1.64*C_L ns
t_{PHL}		0.539	0.995	1.04	1.16	0.336+1.35*C_L ns
t_r	*IN TO X	1.11	2.05	2.14	2.40	0.565+3.63*C_L ns
t_f		0.777	1.44	1.50	1.68	0.361+2.77*C_L ns
* Slowest input						

Switching characteristics

2–Input NAND Gate with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: All: 0.071 pF
Cell Size: 4 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

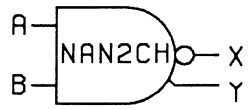
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.786	1.45	1.51	1.70	0.539+1.65*C_L ns
t_{PHL}		0.627	1.16	1.21	1.35	0.422+1.36*C_L ns
t_{PLH}	X TO Y	0.530	0.979	1.02	1.14	0.283+1.64*C_L ns
t_{PHL}		0.556	1.03	1.07	1.20	0.321+1.56*C_L ns
t_{PLH}	*IN TO Y	0.952	1.76	1.83	2.06	0.706+1.64*C_L ns
t_{PHL}		1.09	2.02	2.11	2.36	0.860+1.56*C_L ns
t_r	*IN TO X	1.28	2.36	2.46	2.76	0.733+3.62*C_L ns
t_f		1.02	1.88	1.96	2.20	0.604+2.76*C_L ns
t_r	X TO Y	0.883	1.63	1.70	1.91	0.337+3.64*C_L ns
t_f		0.769	1.42	1.48	1.66	0.309+3.06*C_L ns
t_r	*IN TO Y	0.883	1.63	1.70	1.91	0.337+3.64*C_L ns
t_f		0.769	1.42	1.48	1.66	0.309+3.06*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent on the X output delay. The delays listed for "IN TO Y" and the delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

2–Input NAND Gate (High Drive) with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: A: 0.157
B: 0.158 pF
Cell Size: 7 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

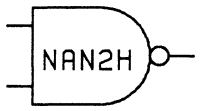
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.535	0.988	1.03	1.16	0.452+0.552*C_L ns
t_{PHL}		0.722	1.33	1.39	1.56	0.589+0.887*C_L ns
t_{PLH}	X TO Y	0.379	0.700	0.730	0.819	0.297+0.545*C_L ns
t_{PHL}		0.346	0.640	0.667	0.748	0.265+0.542*C_L ns
t_{PLH}	*IN TO Y	0.968	1.79	1.86	2.09	0.886+0.545*C_L ns
t_{PHL}		0.798	1.47	1.54	1.72	0.717+0.542*C_L ns
t_r	*IN TO X	1.07	1.98	2.06	2.32	0.914+1.05*C_L ns
t_f		1.26	2.32	2.42	2.72	0.994+1.76*C_L ns
t_r	X TO Y	0.652	1.20	1.26	1.41	0.488+1.09*C_L ns
t_f		0.592	1.09	1.14	1.28	0.459+0.882*C_L ns
t_r	*IN TO Y	0.652	1.20	1.26	1.41	0.488+1.09*C_L ns
t_f		0.592	1.09	1.14	1.28	0.459+0.882*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

2–Input NAND Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: A: 0.157
B: 0.158 pF
Cell Size: 5 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.454	0.839	0.875	0.981	0.372+0.548*C_L ns
t_{PHL}		0.549	1.01	1.06	1.19	0.413+0.907*C_L ns
t_r	*IN TO X	0.683	1.26	1.31	1.47	0.516+1.11*C_L ns
t_f		0.723	1.34	1.39	1.56	0.447+1.84*C_L ns
* Slowest input						

Switching characteristics

3–Input NAND Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.089
B: 0.088
C: 0.089 pF
Cell Size: 4 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.04	1.93	2.01	2.26	0.795+1.66*C_L ns
t_{PHL}		0.648	1.20	1.25	1.40	0.453+1.30*C_L ns
t_r	*IN TO X	1.59	2.94	3.07	3.44	1.05+3.64*C_L ns
t_f		0.934	1.72	1.80	2.02	0.526+2.71*C_L ns
* Slowest input						

Switching characteristics

3–Input NAND Gate with Complementary Outputs

Inputs: A, B, C
Outputs: X, Y
Input Cap.: A: 0.072
B: 0.071
C: 0.072 pF
Cell Size: 5 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.809	1.49	1.56	1.75	0.560+1.65*C_L ns
t_{PHL}		0.850	1.57	1.64	1.84	0.555+1.96*C_L ns
t_{PLH}	X TO Y	0.623	1.15	1.20	1.35	0.372+1.67*C_L ns
t_{PHL}		0.585	1.08	1.13	1.26	0.349+1.57*C_L ns
t_{PLH}	*IN TO Y	1.18	2.18	2.27	2.55	0.928+1.67*C_L ns
t_{PHL}		1.15	2.12	2.21	2.48	0.909+1.57*C_L ns
t_r	*IN TO X	1.33	2.46	2.57	2.88	0.784+3.65*C_L ns
t_f		1.52	2.80	2.92	3.28	0.906+4.07*C_L ns
t_r	X TO Y	0.951	1.76	1.83	2.06	0.408+3.62*C_L ns
t_f		0.795	1.47	1.53	1.72	0.336+3.06*C_L ns
t_r	*IN TO Y	0.951	1.76	1.83	2.06	0.408+3.62*C_L ns
t_f		0.795	1.47	1.53	1.72	0.336+3.06*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

3–Input NAND Gate (High Drive)

Inputs: A, B, C
Outputs: X
Input Cap.: A, B: 0.174
C: 0.175 pF
Cell Size: 7 grids wide, 11 grids high

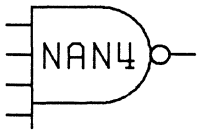
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.539	0.995	1.04	1.16	0.454+0.562*C_L ns
t_{PHL}		0.706	1.30	1.36	1.52	0.556+0.994*C_L ns
t_r	*IN TO X	0.998	1.84	1.92	2.16	0.839+1.06*C_L ns
t_f		1.04	1.93	2.01	2.25	0.748+1.96*C_L ns
* Slowest input						

Switching characteristics

4–Input NAND Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.105 pF
Cell Size: 5 grids wide, 12 grids high



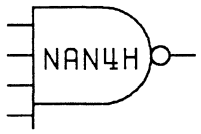
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.38	2.54	2.65	2.97	1.12+1.70*C_L ns
t_{PHL}		0.768	1.42	1.48	1.66	0.578+1.27*C_L ns
t_r	*IN TO X	2.12	3.92	4.09	4.58	1.57+3.65*C_L ns
t_f		1.08	1.99	2.08	2.33	0.677+2.67*C_L ns
* Slowest input						

Switching characteristics

4–Input NAND Gate (High Drive)

Inputs: A, B, C, D
Outputs: X
Input Cap.: A, B, C: 0.211
D: 0.210 pF
Cell Size: 11 grids wide, 12 grids high



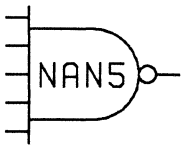
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.724	1.34	1.39	1.56	0.633+0.601*C_L ns
t_{PHL}		0.860	1.59	1.66	1.86	0.732+0.853*C_L ns
t_r	*IN TO X	1.31	2.43	2.53	2.84	1.15+1.10*C_L ns
t_f		1.17	2.16	2.25	2.52	0.906+1.74*C_L ns
* Slowest input						

Switching characteristics

5–Input NAND Gate

Inputs: A, B, C, D, E
Outputs: X
Input Cap.: A: 0.106
B, C, D: 0.105
E: 0.106 pF
Cell Size: 6 grids wide, 12 grids high



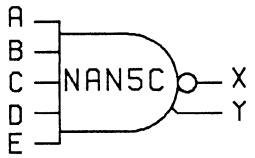
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.57	2.89	3.02	3.39	1.31+1.73*C_L ns
t_{PHL}		1.06	1.96	2.05	2.29	0.826+1.57*C_L ns
t_r	*IN TO X	2.57	4.74	4.94	5.54	2.02+3.66*C_L ns
t_f		1.53	2.82	2.94	3.29	1.03+3.31*C_L ns
* Slowest input						

Switching characteristics

5–Input NAND Gate with Complementary Outputs

Inputs: A, B, C, D, E
Outputs: X, Y
Input Cap.: A: 0.107
B, C: 0.106
D: 0.105
E: 0.106 pF
Cell Size: 7 grids wide, 12 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

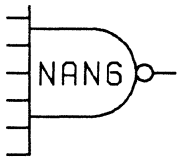
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.70	3.14	3.28	3.68	1.44+1.72*C_L ns
t_{PHL}		1.16	2.15	2.24	2.51	0.926+1.57*C_L ns
t_{PLH}	X TO Y	0.705	1.30	1.36	1.52	0.445+1.73*C_L ns
t_{PHL}		0.830	1.53	1.60	1.79	0.575+1.69*C_L ns
t_{PLH}	*IN TO Y	1.63	3.01	3.14	3.52	1.37+1.73*C_L ns
t_{PHL}		2.27	4.20	4.38	4.91	2.02+1.69*C_L ns
t_r	*IN TO X	2.87	5.29	5.52	6.19	2.32+3.66*C_L ns
t_f		1.80	3.33	3.47	3.89	1.31+3.30*C_L ns
t_r	X TO Y	1.08	1.99	2.07	2.32	0.540+3.57*C_L ns
t_f		1.14	2.10	2.19	2.45	0.693+2.95*C_L ns
t_r	*IN TO Y	1.08	1.99	2.07	2.32	0.540+3.57*C_L ns
t_f		1.14	2.10	2.19	2.45	0.693+2.95*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions see Calculating Standard Cell Timings application note.

6–Input NAND Gate

Inputs: A, B, C, D, E, F
Outputs: X
Input Cap.: A: 0.106
B, C, D, E: 0.105
F: 0.106 pF
Cell Size: 7 grids wide, 12 grids high



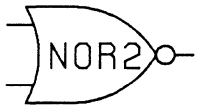
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.69	3.12	3.26	3.65	1.43+1.77*C_L ns
t_{PHL}		1.35	2.49	2.60	2.91	1.07+1.87*C_L ns
t_r	*IN TO X	2.90	5.35	5.57	6.25	2.34+3.68*C_L ns
t_f		1.96	3.62	3.77	4.23	1.37+3.94*C_L ns
* Slowest input						

Switching characteristics

2–Input NOR Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.055 pF
Cell Size: 3 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

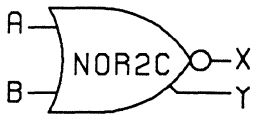
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.958	1.77	1.84	2.07	0.480+3.19*C_L ns
t_{PHL}		0.666	1.23	1.28	1.44	0.432+1.56*C_L ns
t_r	*IN TO X	1.68	3.10	3.23	3.62	0.600+7.18*C_L ns
t_f		0.915	1.69	1.76	1.98	0.459+3.04*C_L ns
* Slowest input						

Switching characteristics

NOR2C

2–Input NOR Gate with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: All: 0.055 pF
Cell Size: 4 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

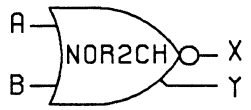
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.19	2.19	2.28	2.56	0.705+3.20*C_L ns
t_{PHL}		0.760	1.40	1.46	1.64	0.524+1.57*C_L ns
t_{PLH}	X TO Y	0.542	1.000	1.04	1.17	0.296+1.64*C_L ns
t_{PHL}		0.690	1.27	1.33	1.49	0.448+1.61*C_L ns
t_{PLH}	*IN TO Y	1.07	1.97	2.05	2.30	0.820+1.64*C_L ns
t_{PHL}		1.40	2.58	2.69	3.01	1.15+1.61*C_L ns
t_r	*IN TO X	2.27	4.19	4.37	4.90	1.19+7.18*C_L ns
t_f		1.14	2.10	2.19	2.46	0.679+3.06*C_L ns
t_r	X TO Y	0.887	1.64	1.71	1.92	0.341+3.64*C_L ns
t_f		0.918	1.70	1.77	1.98	0.467+3.00*C_L ns
t_r	*IN TO Y	0.887	1.64	1.71	1.92	0.341+3.64*C_L ns
t_f		0.918	1.70	1.77	1.98	0.467+3.00*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

2–Input NOR Gate (High Drive) with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: A: 0.195
B: 0.193 pF
Cell Size: 7 grids wide, 12 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

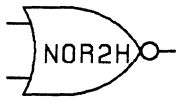
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.662	1.22	1.27	1.43	0.541+0.803*C_L ns
t_{PHL}		0.566	1.05	1.09	1.22	0.486+0.529*C_L ns
t_{PLH}	X TO Y	0.340	0.627	0.654	0.733	0.257+0.546*C_L ns
t_{PHL}		0.390	0.721	0.751	0.843	0.307+0.551*C_L ns
t_{PLH}	*IN TO Y	0.826	1.53	1.59	1.78	0.744+0.546*C_L ns
t_{PHL}		0.931	1.72	1.79	2.01	0.848+0.551*C_L ns
t_r	*IN TO X	1.28	2.36	2.46	2.76	1.03+1.63*C_L ns
t_f		1.01	1.86	1.94	2.18	0.877+0.870*C_L ns
t_r	X TO Y	0.546	1.01	1.05	1.18	0.374+1.14*C_L ns
t_f		0.609	1.12	1.17	1.31	0.469+0.930*C_L ns
t_r	*IN TO Y	0.546	1.01	1.05	1.18	0.374+1.14*C_L ns
t_f		0.609	1.12	1.17	1.31	0.469+0.930*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

2–Input NOR Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: A: 0.160
B: 0.158 pF
Cell Size: 5 grids wide, 10 grids high



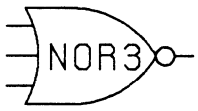
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.580	1.07	1.12	1.25	0.420+1.07*C_L ns
t_{PHL}		0.458	0.847	0.882	0.990	0.379+0.529*C_L ns
t_r	*IN TO X	0.865	1.60	1.67	1.87	0.513+2.35*C_L ns
t_f		0.616	1.14	1.19	1.33	0.476+0.930*C_L ns
* Slowest input						

Switching characteristics

3–Input NOR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.090
B: 0.089
C: 0.090 pF
Cell Size: 4 grids wide, 12 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

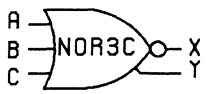
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.06	1.96	2.04	2.29	0.703+2.38*C_L ns
t_{PHL}		0.995	1.84	1.92	2.15	0.753+1.61*C_L ns
t_r	*IN TO X	1.77	3.27	3.41	3.82	0.966+5.35*C_L ns
t_f		1.42	2.62	2.73	3.06	0.955+3.08*C_L ns
* Slowest input						

Switching characteristics

NOR3C

3–Input NOR Gate with Complementary Outputs

Inputs: A, B, C
Outputs: X, Y
Input Cap.: A: 0.073
B: 0.072
C: 0.073 pF
Cell Size: 5 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

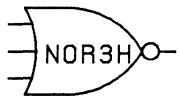
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.45	2.67	2.78	3.12	0.966+3.19*C_L ns
t_{PHL}		0.961	1.77	1.85	2.08	0.721+1.59*C_L ns
t_{PLH}	X TO Y	0.600	1.11	1.15	1.30	0.349+1.67*C_L ns
t_{PHL}		0.745	1.38	1.43	1.61	0.495+1.67*C_L ns
t_{PLH}	*IN TO Y	1.32	2.44	2.54	2.85	1.07+1.67*C_L ns
t_{PHL}		1.71	3.16	3.30	3.70	1.46+1.67*C_L ns
t_r	*IN TO X	2.65	4.90	5.11	5.73	1.58+7.14*C_L ns
t_f		1.48	2.74	2.85	3.20	1.02+3.07*C_L ns
t_r	X TO Y	0.960	1.77	1.85	2.07	0.418+3.61*C_L ns
t_f		1.000	1.85	1.92	2.16	0.549+3.00*C_L ns
t_r	*IN TO Y	0.960	1.77	1.85	2.07	0.418+3.61*C_L ns
t_f		1.000	1.85	1.92	2.16	0.549+3.00*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions see, Calculating Standard Cell Timings application note.

3–Input NOR Gate (High Drive)

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.177
B, C: 0.176 pF
Cell Size: 7 grids wide, 12 grids high



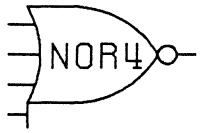
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.907	1.67	1.75	1.96	0.698+1.39*C_L ns
t_{PHL}		0.547	1.01	1.05	1.18	0.463+0.555*C_L ns
t_r	*IN TO X	1.38	2.55	2.66	2.99	0.923+3.06*C_L ns
t_f		0.820	1.51	1.58	1.77	0.676+0.956*C_L ns
* Slowest input						

Switching characteristics

4–Input NOR Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.090
B, C: 0.089
D: 0.090 pF
Cell Size: 5 grids wide, 12 grids high



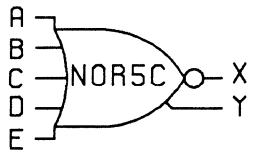
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.53	2.83	2.95	3.31	1.05+3.17*C_L ns
t_{PHL}		1.06	1.96	2.05	2.29	0.812+1.66*C_L ns
t_r	*IN TO X	2.58	4.77	4.98	5.58	1.52+7.09*C_L ns
t_f		1.67	3.08	3.22	3.61	1.20+3.11*C_L ns
* Slowest input						

Switching characteristics

5–Input NOR Gate with Complementary Outputs

Inputs: A, B, C, D, E
Outputs: X, Y
Input Cap.: All: 0.089 pF
Cell Size: 9 grids wide, 11 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

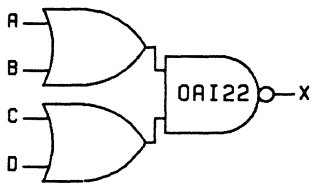
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	Y TO X	0.469	0.866	0.903	1.01	0.220+1.66*C_L ns
t_{PHL}		0.536	0.991	1.03	1.16	0.302+1.56*C_L ns
t_{PLH}	*IN TO Y	1.85	3.41	3.56	3.99	1.58+1.76*C_L ns
t_{PHL}		2.94	5.42	5.65	6.34	2.66+1.86*C_L ns
t_{PLH}	*IN TO X	3.13	5.77	6.02	6.75	2.88+1.66*C_L ns
t_{PHL}		2.12	3.92	4.08	4.58	1.89+1.56*C_L ns
t_r	Y TO X	0.955	1.76	1.84	2.06	0.413+3.61*C_L ns
t_f		0.808	1.49	1.56	1.75	0.352+3.04*C_L ns
t_r	*IN TO Y	1.49	2.75	2.87	3.22	0.952+3.59*C_L ns
t_f		1.65	3.04	3.17	3.56	1.20+3.01*C_L ns
t_r	*IN TO X	0.955	1.76	1.84	2.06	0.413+3.61*C_L ns
t_f		0.808	1.49	1.56	1.75	0.352+3.04*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for X is dependent upon the Y output delay. The delays listed for "IN TO X" and delay equation for X assume no load on the Y output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

2–2 Or–And–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.072
B, C: 0.071
D: 0.072 pF
Cell Size: 5 grids wide, 10 grids high



$X = \overline{(A+B) \cdot (C+D)}$

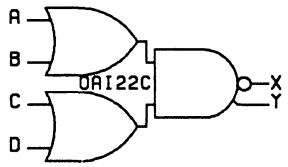
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.79	3.31	3.45	3.87	1.31+3.23*C_L ns
t_{PHL}		0.821	1.52	1.58	1.77	0.614+1.37*C_L ns
t_r	*IN TO X	3.16	5.83	6.08	6.82	2.08+7.16*C_L ns
t_f		1.09	2.01	2.09	2.35	0.671+2.78*C_L ns
* Slowest input						

Switching characteristics

2–2 Or–And–Invert with Complementary Outputs

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: A: 0.072
B: 0.071
C: 0.072
D: 0.071 pF
Cell Size: 7 grids wide, 10 grids high



$X = \overline{(A+B) \cdot (C+D)}$

$Y = (A+B) \cdot (C+D)$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

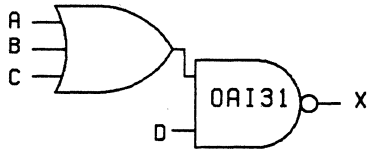
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.88	3.48	3.63	4.07	1.40+3.23*C_L ns
t_{PHL}		0.798	1.47	1.54	1.72	0.592+1.37*C_L ns
t_{PLH}	X TO Y	0.568	1.05	1.09	1.23	0.319+1.66*C_L ns
t_{PHL}		0.806	1.49	1.55	1.74	0.556+1.66*C_L ns
t_{PLH}	*IN TO Y	1.16	2.14	2.23	2.51	0.911+1.66*C_L ns
t_{PHL}		2.20	4.07	4.24	4.76	1.95+1.66*C_L ns
t_r	*IN TO X	3.19	5.89	6.14	6.89	2.11+7.18*C_L ns
t_f		1.17	2.15	2.24	2.52	0.748+2.78*C_L ns
t_r	X TO Y	0.914	1.69	1.76	1.97	0.368+3.64*C_L ns
t_f		1.12	2.07	2.16	2.42	0.680+2.93*C_L ns
t_r	*IN TO Y	0.914	1.69	1.76	1.97	0.368+3.64*C_L ns
t_f		1.12	2.07	2.16	2.42	0.680+2.93*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

3–1 Or–And–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.143
B: 0.142
C: 0.140
D: 0.072 pF
Cell Size: 8 grids wide, 11 grids high



$X = \overline{(A+B+C) \cdot D}$

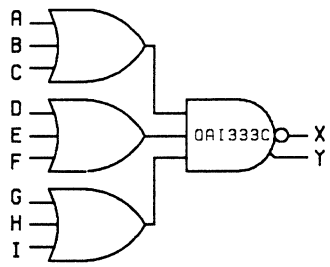
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.15	2.13	2.22	2.49	0.910+1.60*C_L ns
t_{PHL}		1.20	2.21	2.31	2.59	0.984+1.43*C_L ns
t_r	*IN TO X	1.76	3.24	3.38	3.79	1.23+3.53*C_L ns
t_f		1.75	3.23	3.36	3.77	1.33+2.79*C_L ns
* Slowest input						

Switching characteristics

3–3–3 Or–And–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H, I
Outputs: X, Y
Input Cap.: A: 0.105
B: 0.107
C, D: 0.105
E: 0.107
F, G: 0.105
H: 0.107
I: 0.105 pF
Cell Size: 17 grids wide, 12 grids high



$X = \overline{(A+B+C) * (D+E+F) * (G+H+I)}$

$Y = (A+B+C) * (D+E+F) * (G+H+I)$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	Y TO X	0.412	0.762	0.794	0.891	0.167+1.63*C_L ns
t_{PHL}		0.457	0.843	0.879	0.986	0.222+1.56*C_L ns
t_{PLH}	*IN TO Y	2.04	3.76	3.92	4.40	1.77+1.75*C_L ns
t_{PHL}		3.76	6.94	7.23	8.11	3.48+1.81*C_L ns
t_{PLH}	*IN TO X	3.90	7.20	7.50	8.41	3.65+1.63*C_L ns
t_{PHL}		2.23	4.12	4.30	4.82	2.00+1.56*C_L ns
t_r	Y TO X	0.947	1.75	1.82	2.04	0.406+3.60*C_L ns
t_f		0.784	1.45	1.51	1.69	0.325+3.05*C_L ns
t_r	*IN TO Y	1.47	2.71	2.83	3.17	0.942+3.51*C_L ns
t_f		1.80	3.33	3.47	3.89	1.38+2.82*C_L ns
t_r	*IN TO X	0.947	1.75	1.82	2.04	0.406+3.60*C_L ns
t_f		0.784	1.45	1.51	1.69	0.325+3.05*C_L ns
* Slowest input						

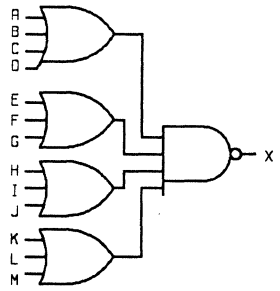
Switching characteristics

NOTE:
The propagation delay for X is dependent upon the Y output delay. The delays listed for "IN TO X" and delay equation for X assume no load on the Y output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

OAI4333

4–3–3–3 Or–And–Invert

Inputs: A, B, C, D, E, F, G, H, I, J, K, L, M
Outputs: X
Input Cap.: A, B, C, D: 0.090
E: 0.105
F: 0.107
G, H: 0.105
I: 0.107
J, K: 0.105
L: 0.107
M: 0.105 pF
Cell Size: 23 grids wide, 12 grids high



$X = \overline{(A+B+C+D) * (E+F+G) * (H+I+J) * (K+L+M)}$

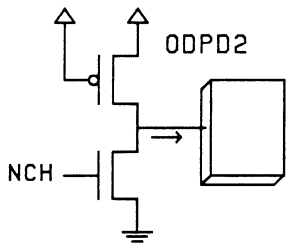
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	2.78	5.14	5.36	6.01	2.54+1.65*C_L ns
t_{PHL}		3.29	6.08	6.33	7.11	3.04+1.62*C_L ns
t_r	*IN TO X	0.962	1.78	1.85	2.08	0.423+3.59*C_L ns
t_f		0.958	1.77	1.85	2.07	0.510+2.98*C_L ns
* Slowest input						

Switching characteristics

2mA 5V Open–Drain Output Pad

ODPD2 is an inverting, open–drain output pad which can have up to 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.529 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	106	195	203	228	9.67+1.92*C_L ns
t_{PHL}		6.53	12.1	12.6	14.1	0.695+0.117*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

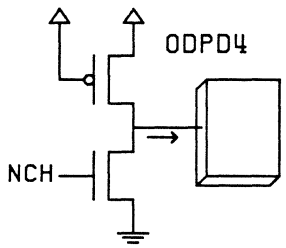
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

4mA 5V Open–Drain Output Pad

ODPD4 is an inverting, open–drain output pad which can have up to 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 1.059 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	108	200	208	234	11.1+1.94*C_L ns
t_{PHL}		3.35	6.19	6.45	7.24	0.449+0.058*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

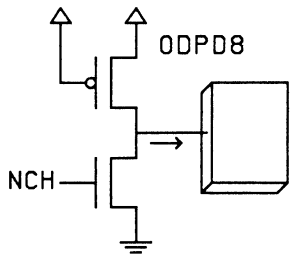
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

8mA 5V Open–Drain Output Pad

ODPD8 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 2.120 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	111	206	215	241	13.5+1.96*C_L ns
t_{PHL}		1.82	3.36	3.50	3.93	0.382+0.029*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

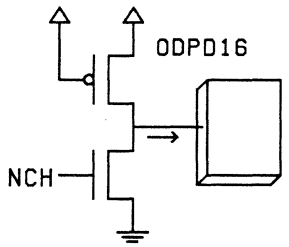
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

16mA 5V Open–Drain Output Pad

ODPD16 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 4.240 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	117	215	225	252	17.9+1.97*C_L ns
t_{PHL}		1.02	1.88	1.96	2.20	0.298+0.014*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

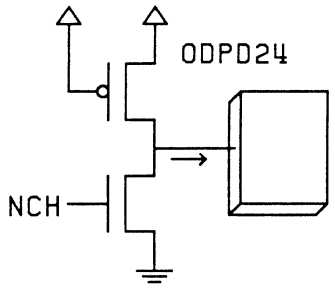
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

24mA 5V Open–Drain Output Pad

ODPD24 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 6.359 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	124	229	238	267	24.1+1.99*C_L ns
t_{PHL}		0.794	1.47	1.53	1.72	0.334+0.009*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

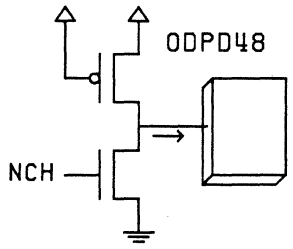
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

48mA 5V Open–Drain Output Pad

ODPD48 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 12.520 pF
Cell Size: 51 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	142	263	274	307	38.8+2.07*C_L ns
t_{PHL}		0.590	1.09	1.14	1.27	0.360+0.005*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

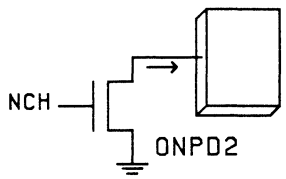
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	48.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

2mA 7V Open–Drain Output Pad

ONPD2 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.529 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	102	189	197	221	6.39+1.92*C_L ns
t_{PHL}		6.29	11.6	12.1	13.6	0.487+0.116*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

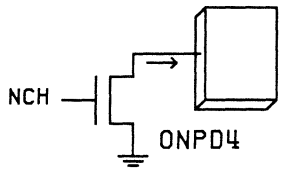
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

4mA 7V Open–Drain Output Pad

ONPD4 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 1.059 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	105	194	202	226	7.72+1.94*C_L ns
t_{PHL}		3.23	5.97	6.22	6.98	0.355+0.057*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

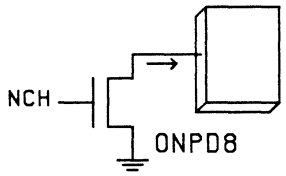
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

8mA 7V Open–Drain Output Pad

ONPD8 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 2.120 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	108	199	208	233	9.84+1.96*C_L ns
t_{PHL}		1.72	3.18	3.32	3.72	0.371+0.027*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

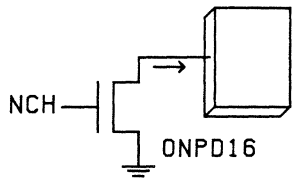
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

16mA 7V Open–Drain Output Pad

ONPD16 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 4.240 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	113	209	218	244	14.3+1.98*C_L ns
t_{PHL}		0.992	1.83	1.91	2.14	0.274+0.014*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

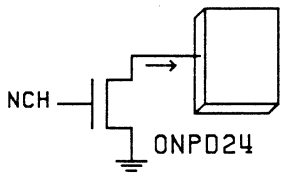
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

24mA 7V Open–Drain Output Pad

ONPD24 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 6.360 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	119	220	229	257	19.5+1.99*C_L ns
t_{PHL}		0.764	1.41	1.47	1.65	0.304+0.009*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

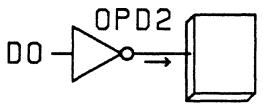
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

2mA Output Pad

OPD2 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 1.060 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	5.81	10.7	11.2	12.5	0.745+0.101*C_L ns
t_{PHL}		6.54	12.1	12.6	14.1	0.730+0.116*C_L ns

Switching characteristics

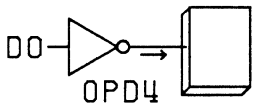
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Output Pad

OPD4 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 2.120 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	3.05	5.64	5.88	6.60	0.524+0.051*C_L ns
t_{PHL}		3.38	6.24	6.50	7.29	0.472+0.058*C_L ns

Switching characteristics

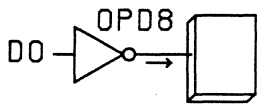
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-2.00	mA

DC specifications

8mA Output Pad

OPD8 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 4.240 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	1.68	3.10	3.23	3.62	0.413+0.025*C_L ns
t_{PHL}		1.83	3.38	3.53	3.96	0.365+0.029*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

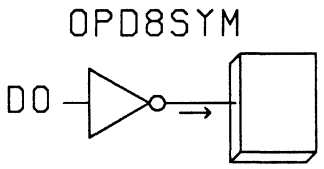
DC specifications

Symmetrical 8mA Output Pad

Features

- Symmetrical hi→low and low→hi drive for off-chip CMOS loads
- Timing specified with input and output at VDD/2
- Drive direct from OSC5402/5502

Symbol



Inputs: DO
Outputs: PAD
Input Cap.: 6.3 pF
Cell Size: 31 grids wide, 60 grids high
Kit Part: OSCARMEYER A

Description

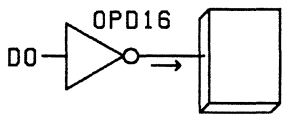
OPD8SYM is functionally similar to the OPD8 cell but with balanced or symmetrical source and sink current drive capability. This results in more closely matched propagation delays between high to low and low to high output swings when driving a CMOS load.

The cell is intended to be driven directly by the OSC5402 or OSC5502 high frequency crystal oscillator cells to provide an off-chip clock signal with the output waveform symmetry from the oscillator preserved as much as possible. In other applications the OPD8SYM can be driven with the same buffers as recommended for an OPD8.

To drive external circuits with an OSC5402 or OSC5502 generated clock, the on-chip oscillator output (OUTB) should drive the OPD8SYM input pin (DO) directly. As with all oscillator cells, the XTLO output should not normally be used to drive external circuits except the crystal and related components.

16mA Output Pad

OPD16 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 8.480 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	0.985	1.82	1.90	2.13	0.352+0.013*C_L ns
t_{PHL}		1.06	1.95	2.03	2.28	0.337+0.014*C_L ns

Switching characteristics

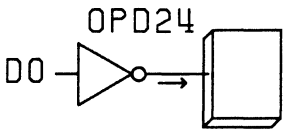
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Output Pad

OPD24 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 11.660 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	0.888	1.64	1.71	1.92	0.371+0.010*C_L ns
t_{PHL}		0.795	1.47	1.53	1.72	0.306+0.010*C_L ns

Switching characteristics

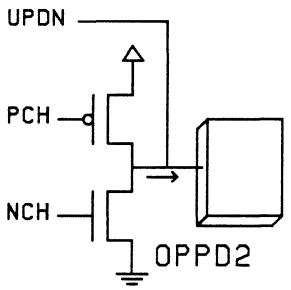
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-12.00	mA

DC specifications

2mA Tristate Output Pad with Pullup/Pulldown Port

OPPD2 is similar to OTPD2 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH, PCH: 0.530
UPDN: 52.000 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	5.86	10.8	11.3	12.6	0.767+0.102*C_L ns
t_{PHL}		6.55	12.1	12.6	14.1	0.742+0.116*C_L ns
* NCH or PCH						

Switching characteristics

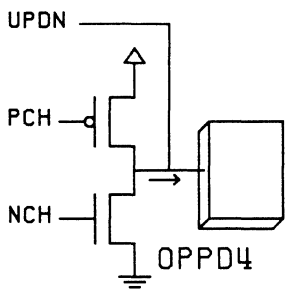
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Tristate Output Pad with Pullup/Pulldown Port

OPPD4 is similar to OTPD4 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH, PCH: 1.059
UPDN: 52.000 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	3.07	5.66	5.90	6.62	0.536+0.051*C_L ns
t_{PHL}		3.39	6.27	6.54	7.33	0.491+0.058*C_L ns
* NCH or PCH						

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

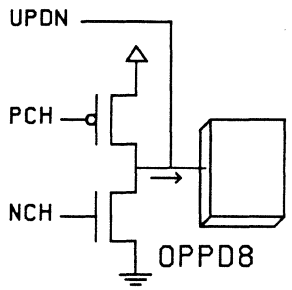
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

OPPD8

8mA Tristate Output Pad with Pullup/Pulldown Port

OPPD8 is similar to OTPD8 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH, PCH: 2.120
UPDN: 52.000 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	1.68	3.11	3.24	3.64	0.419+0.025*C_L ns
t_{PHL}		1.84	3.40	3.54	3.98	0.374+0.029*C_L ns
* NCH or PCH						

Switching characteristics

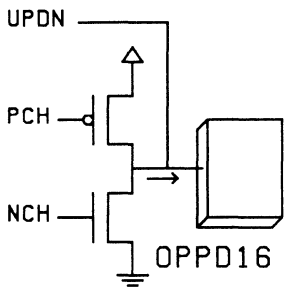
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

16mA Tristate Output Pad with Pullup/Pulldown Port

OPPD16 is similar to OTPD16 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH, PCH: 4.240
UPDN: 52.000 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	0.988	1.82	1.90	2.13	0.355+0.013*C_L ns
t_{PHL}		1.06	1.96	2.04	2.29	0.340+0.014*C_L ns
* NCH or PCH						

Switching characteristics

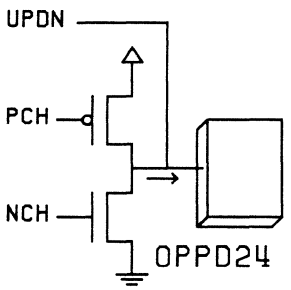
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-8.00	mA

DC specifications

24mA Tristate Output Pad with Pullup/Pulldown Port

OPPD24 is similar to OTPD24 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 6.360
PCH: 5.300
UPDN: 52.000 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.24	5.98	6.23	6.99	0.504+0.055*C_L ns
t_{PHL}		9.31	17.2	17.9	20.1	0.772+0.171*C_L ns
t_{PLH}	*IN TO PAD	0.891	1.65	1.71	1.92	0.373+0.010*C_L ns
t_{PHL}		0.798	1.47	1.54	1.72	0.309+0.010*C_L ns
* NCH or PCH						

Switching characteristics

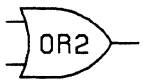
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

2–Input OR Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.055 pF
Cell Size: 4 grids wide, 10 grids high



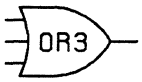
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.08	2.00	2.08	2.34	0.836+1.64*C_L ns
t_{PHL}		1.41	2.61	2.72	3.06	1.17+1.61*C_L ns
t_r	*IN TO X	0.891	1.64	1.71	1.92	0.345+3.64*C_L ns
t_f		0.926	1.71	1.78	2.00	0.475+3.00*C_L ns
* Slowest input						

Switching characteristics

3–Input OR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.073
B: 0.072
C: 0.073 pF
Cell Size: 5 grids wide, 10 grids high



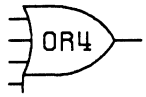
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.32	2.44	2.54	2.85	1.07+1.67*C_L ns
t_{PHL}		1.71	3.16	3.30	3.70	1.46+1.67*C_L ns
t_r	*IN TO X	0.960	1.77	1.85	2.07	0.418+3.61*C_L ns
t_f		1.000	1.85	1.92	2.16	0.549+3.00*C_L ns
* Slowest input						

Switching characteristics

4–Input OR Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.073
B, C: 0.072
D: 0.073 pF
Cell Size: 6 grids wide, 10 grids high



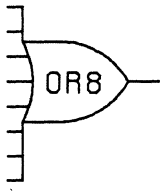
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.39	2.56	2.67	2.99	1.13+1.71*C_L ns
t_{PHL}		2.26	4.17	4.35	4.88	1.99+1.78*C_L ns
t_r	*IN TO X	1.01	1.87	1.95	2.19	0.472+3.61*C_L ns
t_f		1.18	2.17	2.27	2.54	0.726+3.00*C_L ns
* Slowest input						

Switching characteristics

8–Input OR Gate

Inputs: A, B, C, D, E, F, G, H
Outputs: X
Input Cap.: A: 0.055
B, C: 0.054
D, E: 0.055
F, G: 0.054
H: 0.055 pF
Cell Size: 13 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.45	2.67	2.78	3.12	1.19+1.68*C_L ns
t_{PHL}		2.49	4.61	4.80	5.39	2.26+1.54*C_L ns
t_r	*IN TO X	1.23	2.27	2.37	2.66	0.690+3.61*C_L ns
t_f		1.23	2.27	2.36	2.65	0.816+2.74*C_L ns
* Slowest input						

Switching characteristics

Low Power Crystal Oscillator

Features

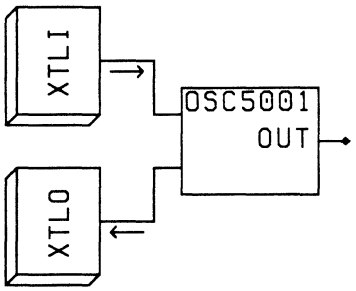
- 10 KHz to 100 KHz operatng range
- Low power (<3 μA at 3.5V)
- 2.7 to 5.5V supply range.
- Amplifier transconductance typically 25–30 μmhos at 3.5V.

Inputs: XTLI
Outputs: OUT, XTLO
Input cap. :XTLI : 5 pF
Output cap. :XTLO : 5 pF
Cell Size: 60 grids high by 63 grids wide
Kit Part: RADAR (X158)

Description

The OSC5001 cell is a low power crystal oscillator core which operates between 10 KHz and 100 KHz. It is well suited for PC real time clock applications. External loading capacitors and an external feedback resistor are required on the XTLI and XTLO pins for proper operation. Cell input and output capacitance values shown are typical values for a packaged part (e.g. RADAR kit part). Figure 2–1 shows a typical application circuit.*

Symbol



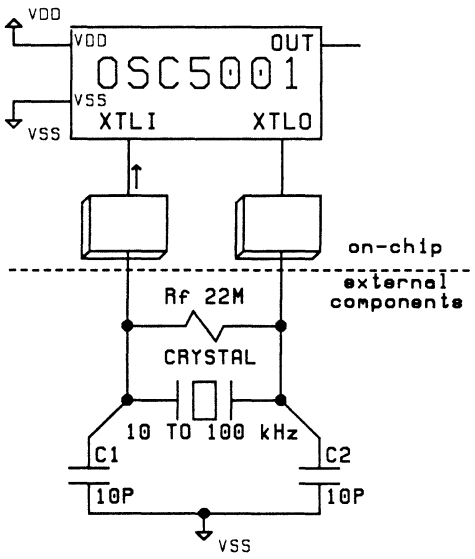


Figure 2–1 Typical application circuit

*See the OSC5001 in the *NCR ASIC Analog Data Book* for further information and complete specifications.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	XTLI TO OUT	308	568	592	664	307+0.924*C_L ns
t_{PHL}		3.49	6.44	6.71	7.53	3.24+1.64*C_L ns
t_r	XTLI TO OUT	16.2	30.0	31.3	35.1	16.1+0.795*C_L ns
t_f		4.14	7.64	7.97	8.94	3.82+2.12*C_L ns

Switching characteristics

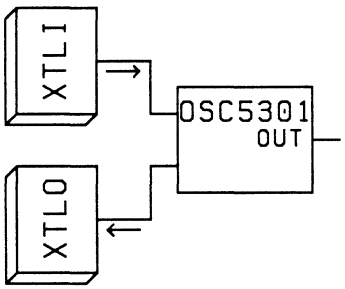
1–10 MHz Crystal Oscillator

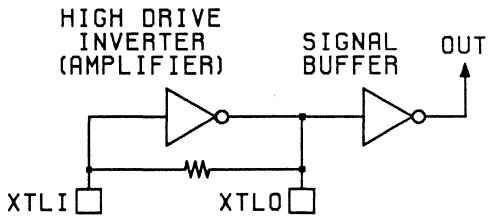
Features

- 1 to 10 MHz operation**
- 40% to 60% output duty cycle
- Buffered on-chip output
- On-chip tuning capacitors
- On-chip bias resistor
- Only requires an external crystal
- Typical gm = 5.2 mA/V

Inputs:	XTLI
Outputs:	OUT, XTLO
Input Cap.:	XTLI: 45 pF
Output Cap.:	XTLO: 50 pF
Cell Size:	109 grids wide, 60 grids high (pad cell)
Kit Part:	VS15_OSC1

Symbol





OSC5301 functional diagram

Description

OSC5301 is a general purpose crystal oscillator cell capable of operation from 1 MHz to 10 MHz.** A fundamental mode quartz crystal is the only external component required since tuning capacitors and a bias (startup) resistor are provided on chip within the cell.

Figure 3–1 shows the internal bias resistor and the load or tuning capacitors required for the crystal pi network. R_B causes the inverter to self bias to approximately $V_{DD}/2$. This is a point where the inverting amplifier has high gain which is necessary for the circuit to oscillate. The value of R_B is approximately 1 MΩ and as such it will not affect the AC performance of the circuit.*

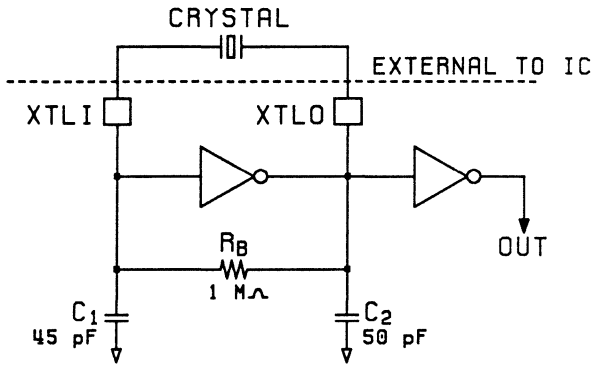


Figure 3–1 Typical fundamental mode circuit

*See the OSC5301 in the *NCR ASIC Analog Data Book* for further information and complete specifications.

**NOTE REGARDING OPERATION AT LESS THAN 3 MHz:

Operation in the range from 1.0–2.9 MHz is discouraged due to limitations of many quartz crystals in that frequency range. The physical size of the quartz blank must be made smaller than the optimum in order to fit into a reasonable standard size package. The result is that non–harmonic modes may be present which vary with temperature and may cause the frequency of oscillation to shift. All modes other than the desired fundamental must be down 6 dB to ensure oscillation at the correct frequency. This means that the equivalent series resistance of undesired modes must be twice that of the fundamental mode.

Most vendors show a 6 dB or better specificatio in their data sheets. In practice, non–harmonic modes have been observed to become the dominate mode (lowest resistance) as a function of temperature, sometimes over a range of only few degrees centigrade. For this reason, NCR recommends using a crystal above 2.9 MHz and dividing down to the desired frequency with on–chip flip–flops.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	XTLI TO OUT	0.331	0.611	0.637	0.715	0.284+0.311*C_L ns
t_{PHL}		0.344	0.636	0.663	0.743	0.299+0.301*C_L ns
t_r	XTLI TO OUT	0.485	0.895	0.933	1.05	0.399+0.566*C_L ns
t_f		0.410	0.756	0.788	0.885	0.336+0.487*C_L ns

Switching characteristics

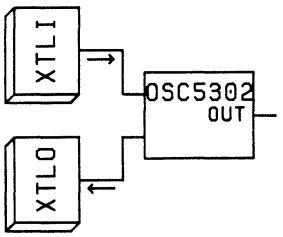
10–25 MHz Crystal Oscillator

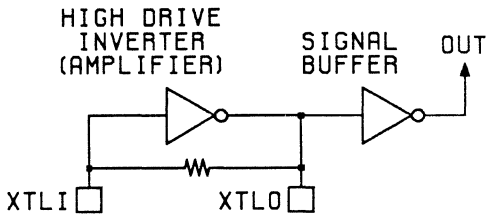
Features

- 10.1 to 25 MHz operation
- 40% to 60% output duty cycle
- Buffered on-chip output
- On-chip tuning capacitors
- On-chip bias resistor
- Only requires an external crystal
- Typical gm = 10.4 mA/V

Inputs:	XTLI
Outputs:	OUT, XTLO
Input Cap.:	XTLI: 45 pF
Output Cap.:	XTLO: 50 pF
Cell Size:	109 grids wide, 60 grids high (pad cell)
Kit Part:	Oscarlater A-G

Symbol





OSC5302 functional diagram

Description

OSC5302 is a general purpose crystal oscillator cell capable of operation from 10.1 MHz to 25 MHz. A fundamental mode quartz crystal is the only external component required since tuning capacitors and a bias (startup) resistor are provided on chip within the cell.

Figure 4–1 shows the internal bias resistor and the load or tuning capacitors required for the crystal pi network. R_B causes the inverter to self bias to approximately $V_{DD}/2$. This is a point where the inverting amplifier has high gain which is necessary for the circuit to oscillate. The value of R_B is approximately 1 MΩ and as such it will not affect the AC performance of the circuit.*

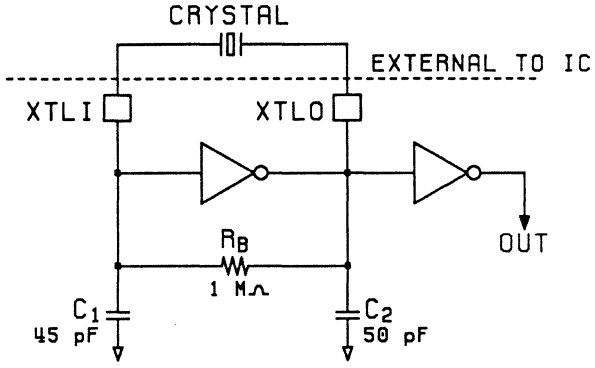


Figure 4–1 Typical fundamental mode circuit

*See the OSC5302 in the *NCR ASIC Analog Data Book* for further information and complete specifications.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	XTLI TO OUT	0.331	0.611	0.637	0.715	0.284+0.311*C_L ns
t_{PHL}		0.344	0.636	0.663	0.743	0.299+0.301*C_L ns
t_r	XTLI TO OUT	0.485	0.895	0.933	1.05	0.399+0.566*C_L ns
t_f		0.410	0.756	0.788	0.885	0.336+0.487*C_L ns

Switching characteristics

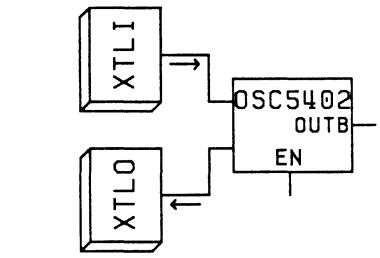
25–50 MHz Crystal Oscillator

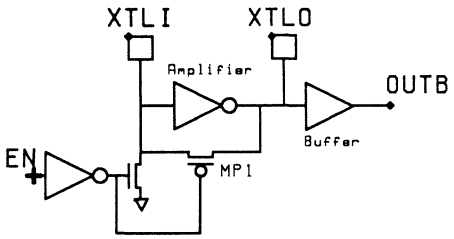
Features

- 25 to 50 MHz operation
- 45% to 55% output duty cycle
- Buffered on-chip output
- Typical gm = 76 mA/V
- Power-down mode

Inputs: XTLI ,EN
Outputs: OUTB, XTLO
Input Cap.: XTLI: 17.143 pF
EN: 0.085 pF
Cell Size: 75 grids by 60 grids high
Kit Part: Oscarmeyer A

Symbol





Functional diagram

Description

OSC5402 is a Pierce type high frequency crystal oscillator cell designed to operate from 25 MHz to 50 MHz. Designs using a fundamental mode crystal require two external tuning capacitors and possibly a resistor to complete the oscillator circuit. Oscillators in this frequency range are often designed to use a third overtone crystal because fundamental mode crystals are not as easy to obtain above 25 or 30 MHz. An additional inductor and coupling capacitor are required for overtone operation.

The power-down mode allows the oscillator to be turned off when it is not needed, to conserve power. This is especially useful in battery powered applications. The EN (ENable) pin must be high for normal operation and low for power-down mode. In power-down mode the self-bias device, MP1, is turned off and the XTLI input is pulled to ground by an open drain n-channel FET. This causes XTLO and OUTB to go to a logic 1.

Preferred locations for OSC5402 are near the center of any side of the packaged part to minimize bond wire and lead frame parasitics.*

*See the OSC5402 in the *NCR ASIC Analog Data Book* for further information and complete specifications.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	XTLI TO OUTB	1.11	2.05	2.14	2.40	1.09+0.167*C_L ns
t_{PHL}		1.07	1.98	2.06	2.31	1.05+0.160*C_L ns
t_{PLH}	EN TO OUTB	1.11	2.05	2.14	2.40	1.09+0.167*C_L ns
t_{PHL}		1.07	1.98	2.06	2.31	1.05+0.160*C_L ns
t_r	XTLI TO OUTB	0.529	0.976	1.02	1.14	0.488+0.269*C_L ns
t_f		0.541	1.000	1.04	1.17	0.515+0.174*C_L ns
t_r	EN TO OUTB	0.529	0.976	1.02	1.14	0.488+0.269*C_L ns
t_f		0.541	1.000	1.04	1.17	0.515+0.174*C_L ns

Switching characteristics

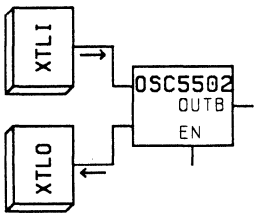
50–70 MHz Crystal Oscillator

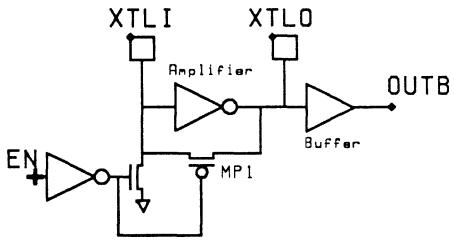
Features

- 50 to 70 MHz operation
- 40% to 60% output duty cycle
- Buffered on-chip output
- Typical gm = 152 mA/V
- Power-down mode

Inputs: XTLI ,EN
Outputs: OUTB, XTLO
Input Cap.: XTLI: 28.780 pF
EN: 0.085 pF
Cell Size: 92 grids by 60 grids high
Kit Part: Oscarmeyer A

Symbol





Functional diagram

Description

OSC5502 is a Pierce type high frequency crystal oscillator cell designed to operate from 50 MHz to 70 MHz. Designs using a fundamental mode crystal require two external tuning capacitors and possibly a resistor to complete the oscillator circuit. Oscillators in this frequency range are often designed to use a third overtone crystal because fundamental mode crystals are not as easy to obtain above 25 or 30 MHz. An additional inductor and coupling capacitor are required for overtone operation.

The power-down mode allows the oscillator to be turned off when it is not needed, to conserve power. This is especially useful in battery powered applications. The EN (ENable) pin must be high for normal operation and low for power-down mode. In power-down mode the self-bias device, MP1, is turned off and the XTLI input is pulled to ground by an open drain n-channel FET. This causes XTLO and OUTB to go to a logic 1.

Preferred locations for OSC5502 are near the center of any side of the packaged part to minimize bond wire and lead frame parasitics. It is also desirable to provide a dedicated V_{DD} and V_{SS} pin next to the oscillator for optimum operation.*

*See the OSC5502 in the *NCR ASIC Analog Data Book* for further information and complete specifications.

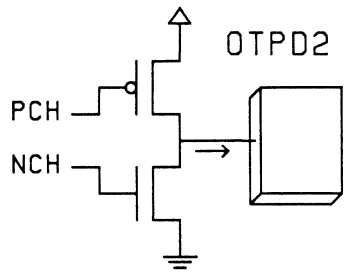
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	XTLI TO OUTB	1.11	2.05	2.14	2.40	1.09+0.167*C_L ns
t_{PHL}		1.07	1.98	2.06	2.31	1.05+0.160*C_L ns
t_{PLH}	EN TO OUTB	1.11	2.05	2.14	2.40	1.09+0.167*C_L ns
t_{PHL}		1.07	1.98	2.06	2.31	1.05+0.160*C_L ns
t_r	XTLI TO OUTB	0.529	0.976	1.02	1.14	0.488+0.269*C_L ns
t_f		0.541	1.000	1.04	1.17	0.515+0.174*C_L ns
t_r	EN TO OUTB	0.529	0.976	1.02	1.14	0.488+0.269*C_L ns
t_f		0.541	1.000	1.04	1.17	0.515+0.174*C_L ns

Switching characteristics

2mA Tristate Output Pad

OTPD2 is an output pad capable of output currents up to 2mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: All: 0.530 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	5.81	10.7	11.2	12.5	0.745+0.101*C_L ns
t_{PHL}		6.54	12.1	12.6	14.1	0.730+0.116*C_L ns
* NCH or PCH						

Switching characteristics

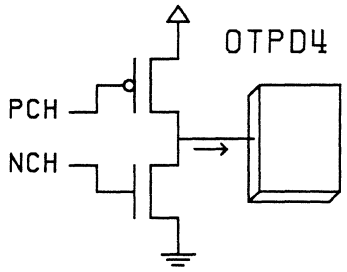
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-1.00	mA

DC specifications

4mA Tristate Output Pad

OTPD4 is an output pad capable of output currents up to 4mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: All: 1.059 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	3.05	5.64	5.88	6.60	0.524+0.051*C_L ns
t_{PHL}		3.38	6.24	6.50	7.29	0.472+0.058*C_L ns
* NCH or PCH						

Switching characteristics

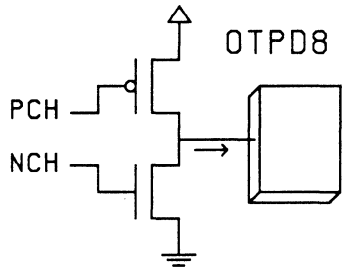
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Tristate Output Pad

OTPD8 is an output pad capable of output currents up to 8mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: All: 2.120 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	1.68	3.10	3.23	3.62	0.413+0.025*C_L ns
t_{PHL}		1.83	3.38	3.53	3.96	0.365+0.029*C_L ns
* NCH or PCH						

Switching characteristics

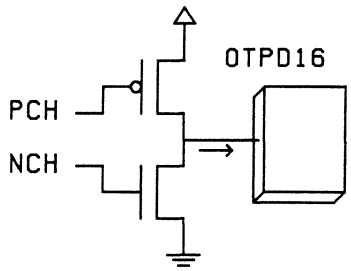
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

16mA Tristate Output Pad

OTPD16 is an output pad capable of output currents up to 16mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: All: 4.240 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.985	1.82	1.90	2.13	0.352+0.013*C_L ns
t_{PHL}		1.06	1.95	2.03	2.28	0.337+0.014*C_L ns
* NCH or PCH						

Switching characteristics

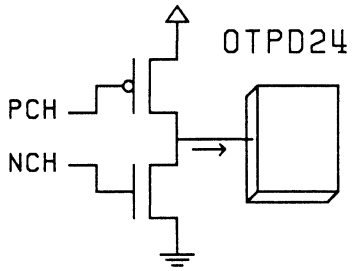
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-8.00	mA

DC specifications

24mA Tristate Output Pad

OTPD24 is an output pad capable of output currents up to 24mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 6.359
PCH: 5.299 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.888	1.64	1.71	1.92	0.371+0.010*C_L ns
t_{PHL}		0.795	1.47	1.53	1.72	0.306+0.010*C_L ns
* NCH or PCH						

Switching characteristics

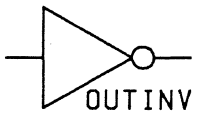
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-12.00	mA

DC specifications

Output Inverter

Inputs: A
Outputs: X
Input Cap.: A: 0.209 pF
Cell Size: 3 grids wide, 11 grids high



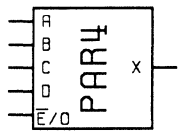
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.321	0.594	0.619	0.694	0.257+0.429*C_L ns
t_{PHL}		0.332	0.613	0.639	0.717	0.271+0.405*C_L ns
t_r	A TO X	0.481	0.888	0.926	1.04	0.359+0.810*C_L ns
t_f		0.443	0.817	0.852	0.956	0.345+0.650*C_L ns

Switching characteristics

4–Bit Parity Checker

Inputs: A, B, C, D, EBO
Outputs: X
Input Cap.: A, B, C: 0.055
D: 0.054
EBO: 0.055 pF
Cell Size: 25 grids wide, 11 grids high



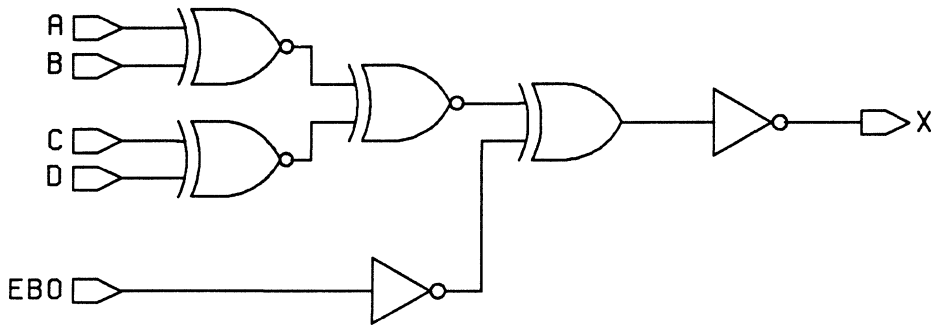
FUNCTION TABLE

EBO	Number of Inputs Which Are High	X
L	0, 2, 4	H
L	1, 3	L
H	0, 2, 4	L
H	1, 3	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

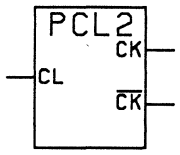
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	4.60	8.49	8.85	9.93	4.35+1.63*C_L ns
t_{PHL}		5.96	11.0	11.5	12.9	5.62+2.23*C_L ns
t_{PLH}	EBO TO X	1.64	3.02	3.15	3.54	1.38+1.68*C_L ns
t_{PHL}		1.94	3.59	3.74	4.20	1.63+2.10*C_L ns
t_r	*IN TO X	1.21	2.24	2.34	2.62	0.698+3.44*C_L ns
t_f		1.79	3.31	3.45	3.87	1.31+3.24*C_L ns
t_r	EBO TO X	0.950	1.75	1.83	2.05	0.405+3.63*C_L ns
t_f		1.29	2.39	2.49	2.79	0.786+3.38*C_L ns
* Slowest of A, B, C, or D inputs						

Switching characteristics



Two–Phase Clock

PCL2 is for use with clocked cells and to produce high drive signals of true and complement value. CK is the noninverted or true output and CKB is the inverted or complement output.



Inputs: CL
Outputs: CK, CKB
Input Cap.: CL: 0.109 pF
Cell Size: 10 grids wide, 11 grids high

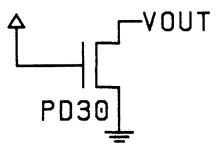
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CL TO CK	1.000	1.85	1.93	2.16	0.929+0.476*C_L ns
t_{PHL}		1.09	2.01	2.10	2.35	1.01+0.485*C_L ns
t_{PLH}	CL TO CKB	1.34	2.47	2.58	2.89	1.27+0.437*C_L ns
t_{PHL}		1.30	2.41	2.51	2.82	1.24+0.451*C_L ns
t_r	CL TO CK	0.563	1.04	1.08	1.22	0.437+0.839*C_L ns
t_f		0.533	0.985	1.03	1.15	0.424+0.725*C_L ns
t_r	CL TO CKB	0.497	0.918	0.957	1.07	0.374+0.821*C_L ns
t_f		0.455	0.840	0.876	0.982	0.351+0.693*C_L ns

Switching characteristics

30μA N–Channel Pulldown Device

PD30 is a weak n–channel pulldown that sinks 30μA when VOUT equals five volts and can be used as a pulldown on internal tristate bus lines. This cell must not be connected directly to Input/Output cells. See the PPD200, PPD400, etc. for that application. To determine current ranges over various process, voltage, and temperature conditions, see application note.



*NOTE: The gate input on the PD30 cannot be used to turn the transistor on or off.

Inputs:
Outputs: VOUT
Input Cap.: : 0.000 pF
Output Cap.: VOUT: 0.034 pF
Cell Size: 12 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	*VOUT	1499	2769	2887	3239	1490+58.6*C_L ns
t_f	*VOUT	37.3	68.9	71.9	80.6	19.0+122*C_L ns
* Timing is from VOUT = 4.5V to VOUT = 2.25V						

Switching characteristics

(V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	30μA typical

DC specifications

Power on Reset

Features

- No external components required
- Retriggerable reset under digital control
- Supply glitch immunity

POR is a digital cell that guarantees a logic low level during power up for the purpose of resetting logic elements to known states. Upon application of the positive supply voltage to the device, POR causes SYS to remain low for approximately 6 µs after the positive supply has exceeded 2.6V. This insures that all digital circuits are operational before the SYS output goes high. An additional input is supplied to the cell which allows the output to be retriggered under external control.

FUNCTION TABLE

V_{DD}	RES	SYS
↑	L	⌐
X	H	L
H	↓	⌐

Inputs: RES
Outputs: SYS
Input Cap.: RES: 0.019 pF
Cell Size: 31 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	RES TO SYS	4717	8712	9082	10189	4713+8.55*C_L ns
t_{PHL}		7.98	14.7	15.4	17.2	7.65+2.19*C_L ns
t_r	RES TO SYS	31.8	58.8	61.3	68.8	30.9+6.31*C_L ns
t_f		1.72	3.18	3.32	3.72	1.17+3.67*C_L ns

Switching characteristics

PARAMETERS AND CONDITIONS	RATING
Supply current (V_{DD} = 5V, V_{RES} = 0V)	74 µA typical
Supply current (V_{DD} = 3V, V_{RES} = 0V)	40 µA typical
V_{DD} trigger voltage	2.6V nominal

Electrical specifications

Application Notes

Reset Timing

The POR cell is not designed for applications requiring precise reset intervals. The duration of the SYS output pulse in a power up condition, or after an external reset input, may vary from the nominal specified timing by 30% or more. Further variations in pulse duration will be observed over varying conditions of supply voltage and temperature. For applications requiring precise timing of a reset signal, an approach utilizing a clocked counter chain is recommended.

No relationship exists between the POR SYS output pulse and the start up time of any crystal oscillator in the NCR standard cell library. In general, the multi-megahertz oscillator cells will require anywhere from 1 ms to 20 ms to reach stable operation after power is applied.

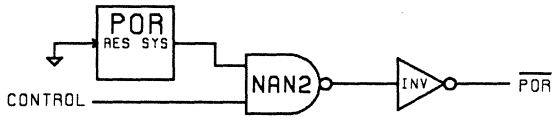
POR provides a certain degree of input glitch immunity. The table given below describes the various situations and responses.

CONDITIONS	RESPONSE
* Glitch-free supply ramp * Supply glitch settles to 2.6V > V_{DD} ≥ 2.0V for at least 100 ns * Supply glitch reaches V_{DD} < 2.0V	SYS output high occurs after V_{DD} = 2.6V + 6.0μs
*Supply glitch settles to V_{DD} ≥ 2.6V *Supply glitch settles to 2.6V > V_{DD} ≥ 2.0V for less than 50 ns	Will not effect SYS output of POR

POR

Testability

NCR requires the chip be simulated and tested with the reset time out feature of the POR disabled. To achieve this, the RESET input on the POR should be grounded, and the POR output should be ANDed with a control signal (NAN2 and INV – see Reset circuit. The control signal should be accessible by the tester during test time at probe and after the chip is packaged. A static pullup may be connected to the control signal path to enable the reset circuit under normal operation. NCR will review the specific implementation of any circuit using the POR at the time of the design review.



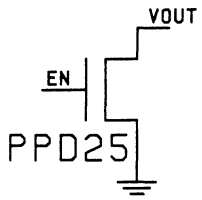
Reset circuit

System Considerations

The NCR POR cell is designed to provide a reset pulse that can be used throughout the chip. If this signal is brought off chip for a system reset, precautions should be taken to insure that all other chips are powered up and functional while the reset pulse is valid.

25μA N–Channel Pulldown Device

PPD25 is a weak n–channel pulldown that sinks 25μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD25 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.891 pF
Output Cap.: VOUT: 0.041 pF
Cell Size: 13 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	5090	9402	9800	10996	18.1+101*C_L ns

Switching characteristics

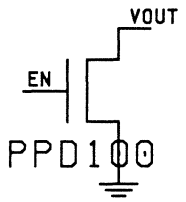
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	25μA typical

DC specifications

100μA N–Channel Pulldown Device

PPD100 is a weak n–channel pulldown that sinks 100μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD100 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.227 pF
Output Cap.: VOUT: 0.044 pF
Cell Size: 12 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	1262	2331	2430	2726	0.914+25.2*C_L ns

Switching characteristics

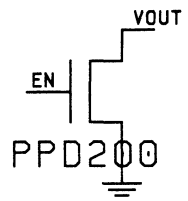
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	100μA typical

DC specifications

200μA N–Channel Pulldown Device

PPD200 is a weak n–channel pulldown that sinks 200μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD200 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.122 pF
Output Cap.: VOUT: 0.038 pF
Cell Size: 8 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	662	1222	1274	1429	0.000+13.2*C_L ns

Switching characteristics

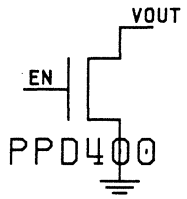
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	200μA typical

DC specifications

400μA N–Channel Pulldown Device

PPD400 is a weak n–channel pulldown that sinks 400μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD400 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.229 pF
Output Cap.: VOUT: 0.045 pF
Cell Size: 9 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	331	611	637	715	0.000+6.62*C_L ns

Switching characteristics

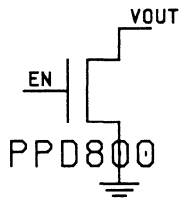
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	400μA typical

DC specifications

800μA N–Channel Pulldown Device

PPD800 is a weak n–channel pulldown that sinks 800μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD800 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.450 pF
Output Cap.: VOUT: 0.086 pF
Cell Size: 10 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	166	306	319	358	0.000+3.31*C_L ns

Switching characteristics

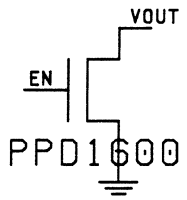
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	800μA typical

DC specifications

1600μA N–Channel Pulldown Device

PPD1600 is a weak n–channel pulldown that sinks 1600μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD1600 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.227 pF
Output Cap.: VOUT: 0.086 pF
Cell Size: 9 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	84.4	156	163	182	0.000+1.69*C_L ns

Switching characteristics

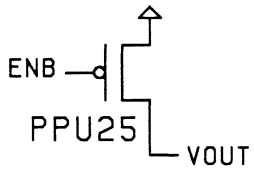
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	1600μA typical

DC specifications

25μA P–Channel Pullup Device

PPU25 is a weak p–channel pullup that sources 25μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU25 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.654 pF
Output Cap.: VOUT: 0.039 pF
Cell Size: 14 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	2164	3997	4166	4674	49.0+42.3*C_L ns

Switching characteristics

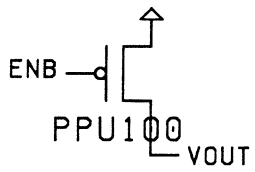
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	25μA typical

DC specifications

100μA P–Channel Pullup Device

PPU100 is a weak p–channel pullup that sources 100μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU100 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.174 pF
Output Cap.: VOUT: 0.048 pF
Cell Size: 8 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	556	1026	1069	1200	11.8+10.9*C_L ns

Switching characteristics

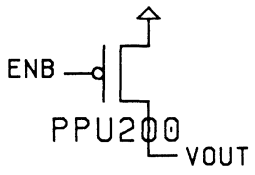
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	100μA typical

DC specifications

200µA P–Channel Pullup Device

PPU200 is a weak p–channel pullup that sources 200µA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU200 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.) . The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.094 pF
Output Cap.: VOUT: 0.032 pF
Cell Size: 9 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	284	525	548	614	5.98+5.57*C_L ns

Switching characteristics

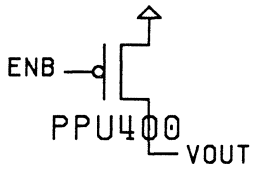
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	200µA typical

DC specifications

400μA P–Channel Pullup Device

PPU400 is a weak p–channel pullup that sources 400μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU400 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.177 pF
Output Cap.: VOUT: 0.061 pF
Cell Size: 9 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	142	262	273	306	3.24+2.77*C_L ns

Switching characteristics

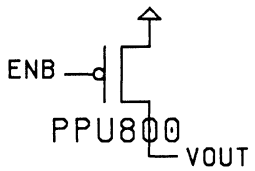
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	400μA typical

DC specifications

800µA P–Channel Pullup Device

PPU800 is a weak p–channel pullup that sources 800µA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU800 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.344 pF
Output Cap.: VOUT: 0.117 pF
Cell Size: 11 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	71.8	133	138	155	1.88+1.40*C_L ns

Switching characteristics

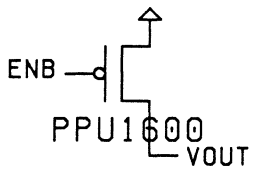
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	800µA typical

DC specifications

1600μA P–Channel Pullup Device

PPU1600 is a weak p–channel pullup that sources 1600μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU1600 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.687 pF
Output Cap.: VOUT: 0.232 pF
Cell Size: 16 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	35.9	66.3	69.1	77.5	1.19+0.694*C_L ns

Switching characteristics

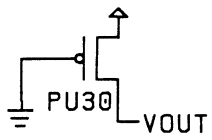
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	1600μA typical

DC specifications

30μA P–Channel Pullup Device

PU30 is a weak p–channel pullup that sources 30μA when VOUT equals zero volts and can be used as a pullup on internal tristate bus lines. This cell must not be connected directly to Input/Output cells. See PPU200, PPU400, etc. for that application. To determine current ranges over various process, voltage, and temperature conditions, see application note.



*NOTE: The gate input on the PU30 cannot be used to turn the transistor on or off.

Inputs:
Outputs: VOUT
Input Cap.: : 0.000 pF
Output Cap.: VOUT: 0.021 pF
Cell Size: 3 grids wide, 11 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*VOUT	1499	2769	2887	3239	1490+58.6*C_L ns
t_r	*VOUT	28.0	51.7	53.9	60.5	9.16+126*C_L ns
* Timing is from VOUT = 0V to VOUT = 2.25V.						

Switching characteristics

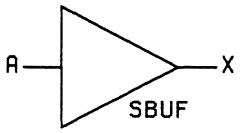
(V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	30μA typical

DC specifications

Small Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.055 pF
Cell Size: 3 grids wide, 11 grids high



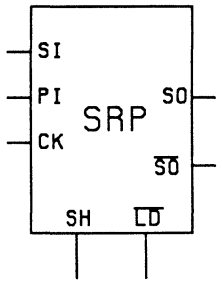
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.981	1.81	1.89	2.12	0.735+1.64*C_L ns
t_{PHL}		1.05	1.93	2.01	2.26	0.811+1.56*C_L ns
t_r	A TO X	0.866	1.60	1.67	1.87	0.318+3.65*C_L ns
t_f		0.770	1.42	1.48	1.66	0.311+3.06*C_L ns

Switching characteristics

Shift Register, Positive Edge Triggered

SRP is a 1-bit shift register. It is positive edge triggered with respect to CK. Serial input is clocked in when SH is high. Parallel input is clocked in when LDB is low. SH and LDB should be tied together for normal operation.



Inputs: SI, SH, PI, LDB, CK
Outputs: SO, SOB
Input Cap.: SI: 0.055
SH: 0.059
PI: 0.056
LDB: 0.059
CK: 0.055 pF
Cell Size: 25 grids wide, 12 grids high

FUNCTION TABLE

SH	SI	LDB	PI	CK	SO	SOB
H	L	H	X	↑	L	H
H	H	H	X	↑	H	L
L	X	L	L	↑	L	H
L	X	L	H	↑	H	L
H	X	L	X	X	*	*
L	X	H	X	X	*	*

* ILLEGAL INPUT COMBINATION

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO SO	2.42	4.47	4.66	5.23	2.30+0.841*C_L ns
t_{PHL}		2.96	5.46	5.69	6.39	2.82+0.912*C_L ns
t_{PLH}	CK TO SOB	3.50	6.46	6.74	7.56	3.38+0.793*C_L ns
t_{PHL}		3.56	6.58	6.86	7.70	3.44+0.834*C_L ns
t_r	CK TO SO	0.734	1.36	1.41	1.59	0.474+1.73*C_L ns
t_f		0.872	1.61	1.68	1.88	0.656+1.44*C_L ns
t_r	CK TO SOB	0.738	1.36	1.42	1.59	0.480+1.72*C_L ns
t_f		0.809	1.49	1.56	1.75	0.591+1.45*C_L ns

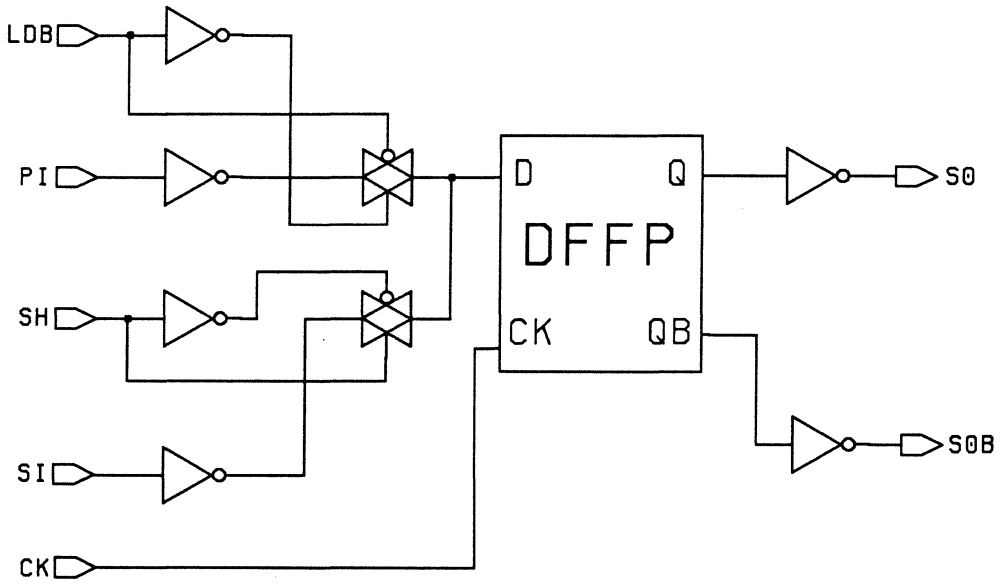
Switching characteristics

SRP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time SI to CK	3.00	ns
t_{su}	Setup Time SH to CK	2.75	ns
t_{su}	Setup Time PI to CK	3.25	ns
t_{su}	Setup Time LDB to CK	2.75	ns
t_h	Hold Time CK to SI	−2.25	ns
t_h	Hold Time CK to SH	−2.00	ns
t_h	Hold Time CK to PI	−2.25	ns
t_h	Hold Time CK to LDB	−2.00	ns
t_{pwh}	High CK Pulse Width	4.50	ns
t_{pwl}	Low CK Pulse Width	5.00	ns

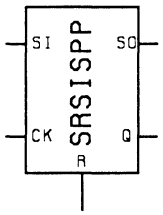
Timing requirements



Functional diagram: SRP

1–Bit Serial–In/Parallel–Out Shift Register

SRSISPP is a single-bit serial input shift register cell. Data on SI is shifted in on the positive edge of CK. Both a serial and parallel output are available to reduce loading on the serial output.



Inputs: SI, CK, R
Outputs: SO, Q
Input Cap.: SI, CK: 0.055
R: 0.054 pF
Cell Size: 26 grids wide, 12 grids high

FUNCTION TABLE

SI	CK	R	SO	Q
X	X	H	L	L
H	↑	L	H	H
L	↑	L	L	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*CK TO OUT	3.61	6.67	6.95	7.80	3.35+1.70*C_L ns
t_{PHL}		2.74	5.06	5.28	5.92	2.50+1.58*C_L ns
t_{PHL}	*R TO OUT	2.01	3.70	3.86	4.33	1.76+1.61*C_L ns
t_r	*CK TO OUT	1.20	2.21	2.30	2.59	0.668+3.52*C_L ns
t_f		0.925	1.71	1.78	2.00	0.476+2.99*C_L ns
t_f	*R TO OUT	0.933	1.72	1.80	2.01	0.483+2.99*C_L ns
* OUT refers to both SO and Q						

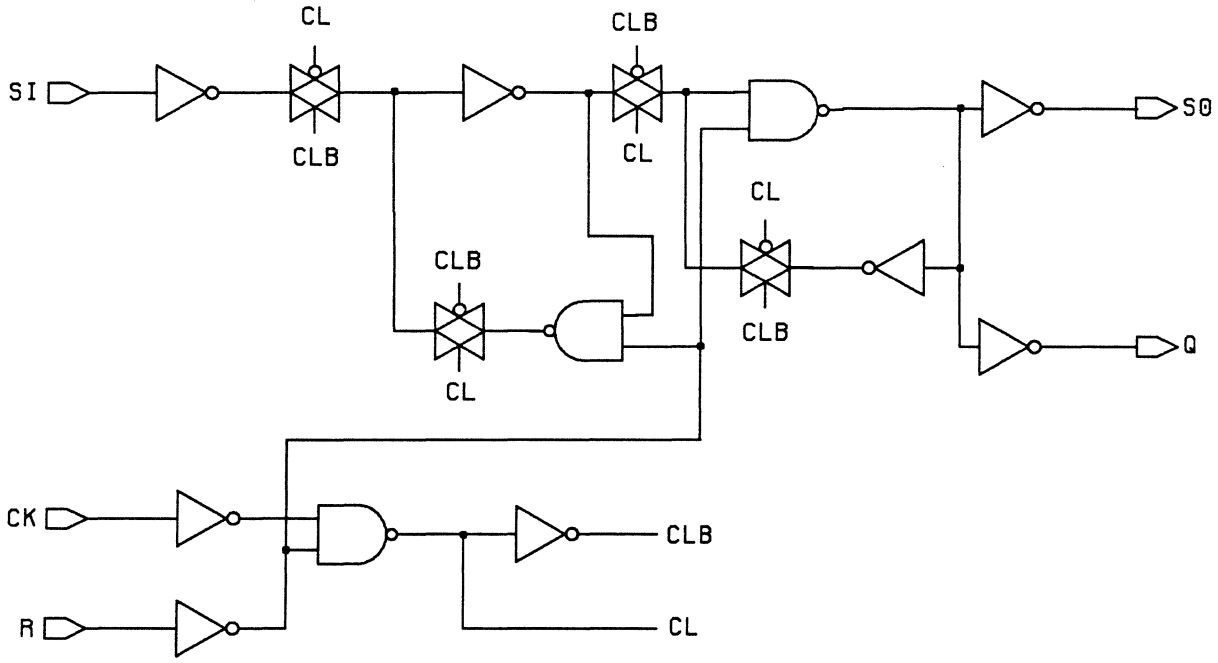
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time SI to CK	0.75	ns
t_h	Hold Time CK to SI	-0.25	ns
t_{pwh}	High CK Pulse Width	4.25	ns
t_{pwh}	R Pulse Width (high)	3.75	ns
t_{pwl}	Low CK Pulse Width	5.00	ns
rt	R Recovery Time	3.50	ns

Timing requirements

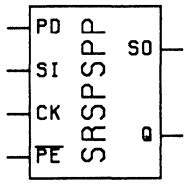
SRSISPP



Functional diagram: SRSISPP

1–Bit Serial/Parallel Shift Register

SRSPSPP is a single–bit serial/parallel input shift register cell. Data on SI is shifted in on the positive edge of CK. Data is loaded asynchronously when PEB goes low. Both serial and parallel outputs are available to reduce loading on the serial output.



Inputs: PEB, PD, SI, CK
Outputs: SO, Q
Input Cap.: PEB, PD: 0.055
SI: 0.056
CK: 0.055 pF
Cell Size: 31 grids wide, 12 grids high

FUNCTION TABLE

CK	PEB	PD	SI	SO	Q
X	L	L	X	L	L
X	L	H	X	H	H
↑	H	X	L	L	L
↑	H	X	H	H	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*PEB TO OUT	4.20	7.77	8.09	9.08	3.96+1.65*C_L ns
t_{PHL}		3.90	7.20	7.51	8.42	3.66+1.58*C_L ns
t_{PLH}	*PD TO OUT	3.99	7.37	7.69	8.62	3.74+1.65*C_L ns
t_{PHL}		3.99	7.37	7.68	8.62	3.75+1.59*C_L ns
t_{PLH}	*CK TO OUT	2.73	5.04	5.25	5.89	2.48+1.65*C_L ns
t_{PHL}		2.86	5.28	5.50	6.17	2.62+1.57*C_L ns
t_r	*PEB TO OUT	0.916	1.69	1.76	1.98	0.370+3.64*C_L ns
t_f		0.877	1.62	1.69	1.90	0.426+3.01*C_L ns
t_r	*PD TO OUT	0.936	1.73	1.80	2.02	0.391+3.62*C_L ns
t_f		0.859	1.59	1.65	1.86	0.405+3.03*C_L ns
t_r	*CK TO OUT	0.910	1.68	1.75	1.96	0.363+3.64*C_L ns
t_f		0.855	1.58	1.65	1.85	0.401+3.03*C_L ns
* OUT refers to both SO and Q						

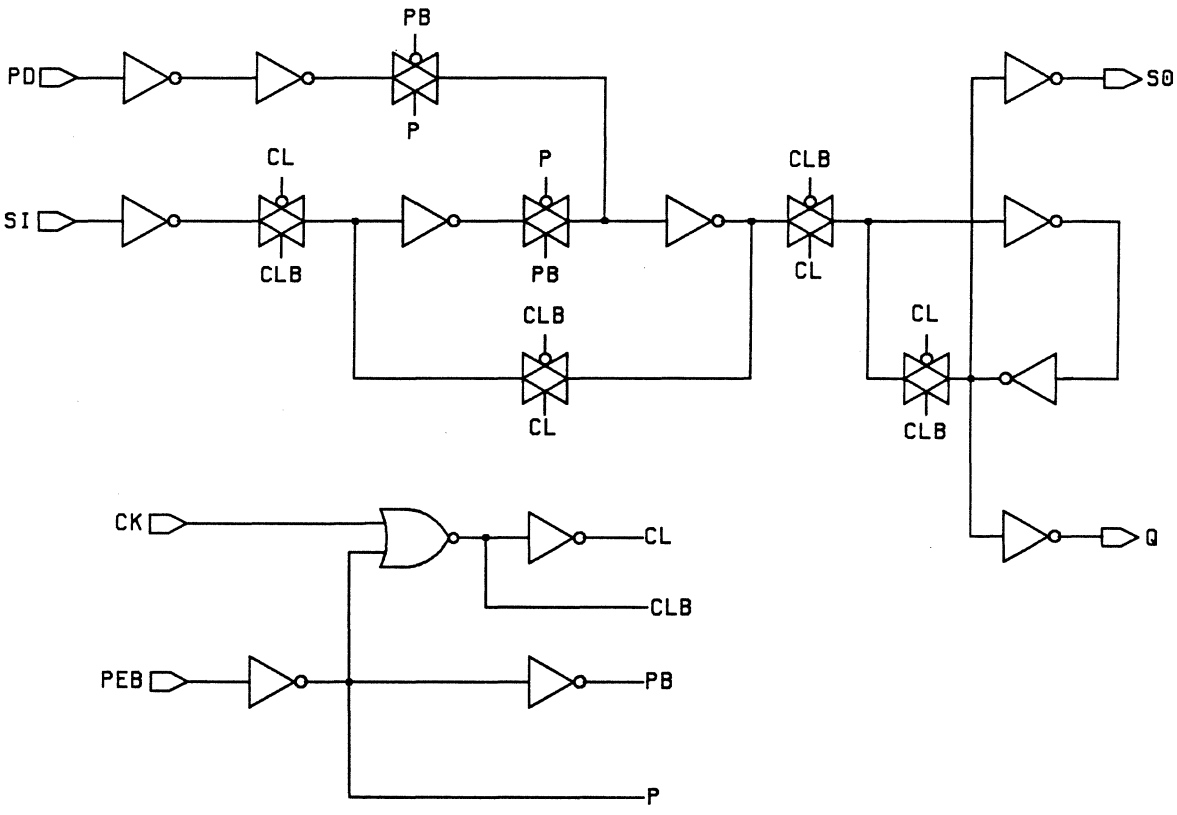
Switching characteristics

SRSPSPP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time SI to CK	2.75	ns
t_{su}	Setup Time PD to PEB	1.50	ns
t_h	Hold Time CK to SI	0.00	ns
t_h	Hold Time PEB to PD	0.00	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwl}	PEB Pulse Width (low)	3.75	ns
t_{pwl}	Low CK Pulse Width	5.50	ns
rt	PEB Recovery Time	4.50	ns

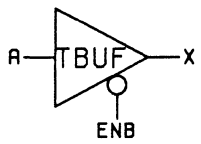
Timing requirements



Functional diagram: SRSPSPP

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi–Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.072
ENB: 0.113 pF
Output Cap.: X: 0.168 pF
Cell Size: 9 grids wide, 11 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

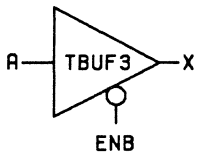
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.19	2.19	2.29	2.57	1.11+0.539*C_L ns
t_{PHL}		1.69	3.13	3.26	3.66	1.59+0.691*C_L ns
t_{PLH}	ENB TO X	1.34	2.48	2.59	2.90	1.27+0.513*C_L ns
t_{PHL}		1.28	2.36	2.46	2.76	1.18+0.677*C_L ns
t_r	A TO X	0.531	0.980	1.02	1.15	0.397+0.891*C_L ns
t_f		0.745	1.38	1.43	1.61	0.617+0.855*C_L ns
t_r	ENB TO X	0.520	0.960	1.000	1.12	0.384+0.903*C_L ns
t_f		0.601	1.11	1.16	1.30	0.470+0.867*C_L ns

Switching characteristics

TBUF3

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi-Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.107
ENB: 0.054 pF
Output Cap.: X: 0.158 pF
Cell Size: 10 grids wide, 10 grids high

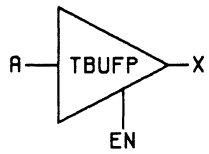
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.05	1.94	2.02	2.27	0.953+0.639*C_L ns
t_{PHL}		1.01	1.87	1.95	2.18	0.920+0.609*C_L ns
t_{PLH}	ENB TO X	1.61	2.98	3.11	3.48	1.52+0.640*C_L ns
t_{PHL}		1.79	3.31	3.45	3.87	1.70+0.621*C_L ns
t_r	A TO X	0.613	1.13	1.18	1.32	0.440+1.15*C_L ns
t_f		0.545	1.01	1.05	1.18	0.398+0.975*C_L ns
t_r	ENB TO X	0.590	1.09	1.14	1.27	0.416+1.16*C_L ns
t_f		0.497	0.917	0.956	1.07	0.346+1.000*C_L ns

Switching characteristics

Noninverting Tristate Buffer

EN is active high. When EN is low, the output is in a Hi-Z state.



Inputs: A, EN
Outputs: X
Input Cap.: A: 0.105
EN: 0.130 pF
Output Cap.: X: 0.168 pF
Cell Size: 8 grids wide, 11 grids high

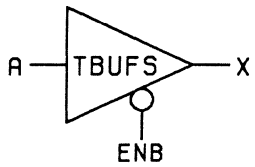
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.13	2.09	2.18	2.44	1.01+0.801*C_L ns
t_{PHL}		1.05	1.95	2.03	2.28	0.946+0.721*C_L ns
t_{PLH}	EN TO X	0.938	1.73	1.81	2.03	0.815+0.817*C_L ns
t_{PHL}		0.388	0.717	0.748	0.839	0.279+0.729*C_L ns
t_r	A TO X	0.907	1.68	1.75	1.96	0.645+1.74*C_L ns
t_f		0.822	1.52	1.58	1.78	0.620+1.34*C_L ns
t_r	EN TO X	1.08	1.99	2.08	2.33	0.835+1.62*C_L ns
t_f		0.669	1.24	1.29	1.44	0.467+1.35*C_L ns

Switching characteristics

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi–Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.069
ENB: 0.106 pF
Output Cap.: X: 0.123 pF
Cell Size: 7 grids wide, 9 grids high

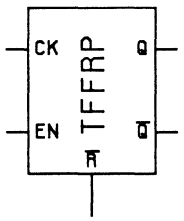
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.914	1.69	1.76	1.97	0.772+0.939*C_L ns
t_{PHL}		1.39	2.57	2.68	3.00	1.32+0.438*C_L ns
t_{PLH}	ENB TO X	1.03	1.91	1.99	2.23	0.892+0.947*C_L ns
t_{PHL}		0.945	1.74	1.82	2.04	0.811+0.885*C_L ns
t_r	A TO X	0.622	1.15	1.20	1.34	0.330+1.94*C_L ns
t_f		0.700	1.29	1.35	1.51	0.504+1.31*C_L ns
t_r	ENB TO X	0.638	1.18	1.23	1.38	0.348+1.93*C_L ns
t_f		0.589	1.09	1.13	1.27	0.380+1.39*C_L ns

Switching characteristics

Toggle Enable Flip–Flop with Reset

TFFRP is a positive edge triggered toggle flip–flop with active high toggle enable and active low reset. For a faster version of this cell, see TFFRPF.



Inputs: RB, EN, CK
Outputs: Q, QB
Input Cap.: RB: 0.150
EN: 0.095
CK: 0.057 pF
Cell Size: 25 grids wide, 12 grids high

FUNCTION TABLE

RB	EN	CK	Q	QB
L	X	X	L	H
H	H	↑	QB_o	Q_o
H	L	↑	Q_o	QB_o

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	RB TO Q	2.10	3.88	4.04	4.54	1.94+1.03*C_L ns
t_{PLH}	CK TO Q	3.61	6.67	6.95	7.80	3.47+0.922*C_L ns
t_{PHL}		4.04	7.46	7.78	8.73	3.90+0.901*C_L ns
t_{PLH}	RB TO QB	3.63	6.71	7.00	7.85	3.50+0.855*C_L ns
t_{PLH}	CK TO QB	2.77	5.13	5.34	5.99	2.64+0.885*C_L ns
t_{PHL}		2.66	4.92	5.12	5.75	2.53+0.894*C_L ns
t_f	RB TO Q	1.03	1.90	1.98	2.22	0.804+1.48*C_L ns
t_r	CK TO Q	0.857	1.58	1.65	1.85	0.595+1.75*C_L ns
t_f		0.804	1.48	1.55	1.74	0.580+1.49*C_L ns
t_r	RB TO QB	0.832	1.54	1.60	1.80	0.575+1.71*C_L ns
t_r	CK TO QB	0.804	1.48	1.55	1.74	0.544+1.73*C_L ns
t_f		0.754	1.39	1.45	1.63	0.532+1.48*C_L ns

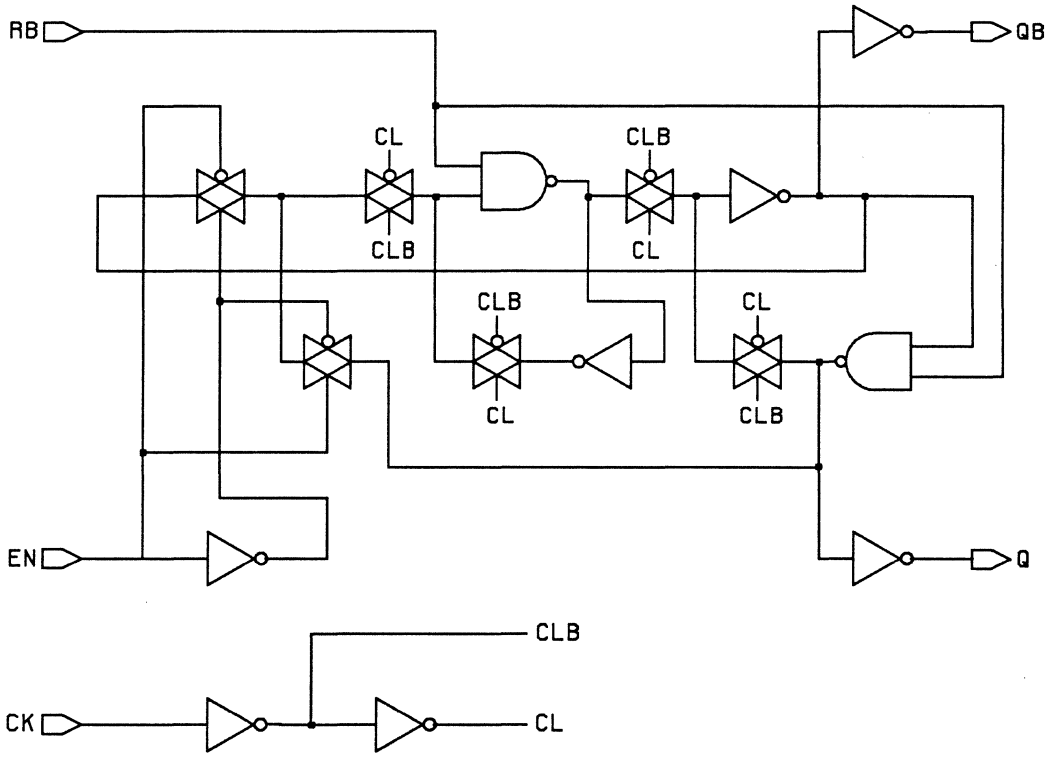
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time EN to CK	2.50	ns
t_h	Hold Time CK to EN	−1.75	ns
t_{pwh}	High CK Pulse Width	5.50	ns
t_{pwl}	RB Pulse Width (low)	6.25	ns
t_{pwl}	Low CK Pulse Width	4.75	ns
rt	RB Recovery Time	−0.50	ns

Timing requirements

TFFRP

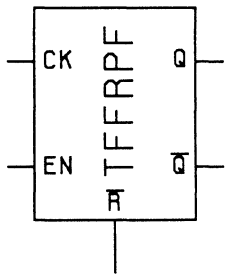


Functional diagram: TFFRP

Fast Toggle Enable Flip–Flop with Reset

TFFRPF is a positive edge triggered toggle flip–flop with active high toggle enable and active low reset.

Inputs: RB, EN, CK
Outputs: Q, QB
Input Cap.: RB: 0.351
EN: 0.126
CK: 0.459 pF
Cell Size: 29 grids wide, 12 grids high



FUNCTION TABLE

RB	EN	CK	Q	QB
L	X	X	L	H
H	H	↑	QB_o	Q_o
H	L	↑	Q_o	QB_o

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	RB TO Q	2.18	4.02	4.19	4.70	2.07+0.690*C_L ns
t_{PLH}	CK TO Q	1.66	3.06	3.19	3.58	1.52+0.928*C_L ns
t_{PHL}		1.72	3.17	3.30	3.71	1.62+0.614*C_L ns
t_{PLH}	RB TO QB	3.03	5.60	5.84	6.55	2.91+0.791*C_L ns
t_{PLH}	CK TO QB	2.45	4.52	4.71	5.28	2.33+0.800*C_L ns
t_{PHL}		1.99	3.68	3.83	4.30	1.92+0.456*C_L ns
t_f	RB TO Q	1.15	2.12	2.21	2.48	1.06+0.601*C_L ns
t_r	CK TO Q	0.919	1.70	1.77	1.98	0.657+1.74*C_L ns
t_f		0.716	1.32	1.38	1.55	0.604+0.747*C_L ns
t_r	RB TO QB	0.717	1.32	1.38	1.55	0.453+1.75*C_L ns
t_r	CK TO QB	0.704	1.30	1.35	1.52	0.440+1.76*C_L ns
t_f		0.526	0.971	1.01	1.14	0.424+0.675*C_L ns

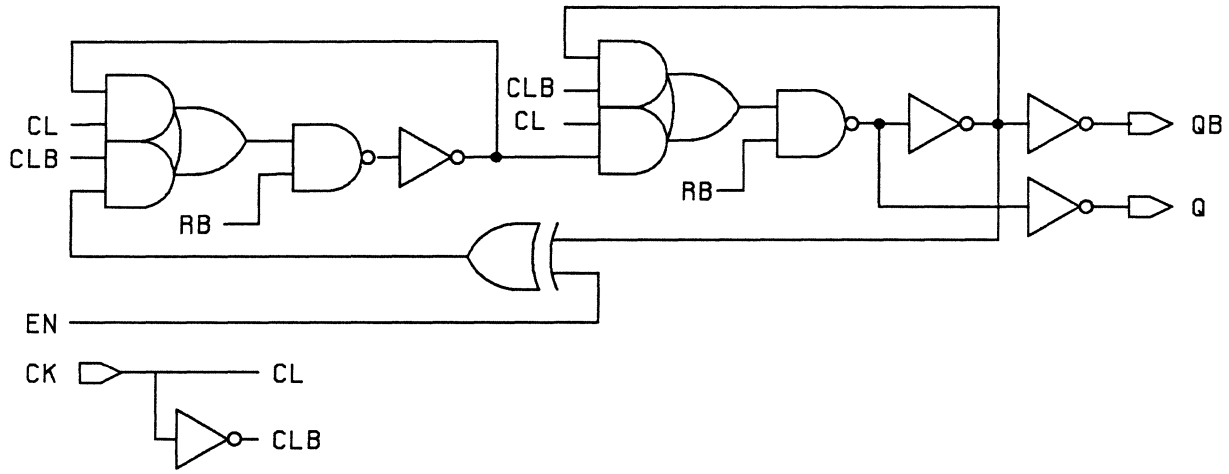
Switching characteristics

TFFRPF

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time EN to CK	4.50	ns
t_h	Hold Time CK to EN	-3.00	ns
t_{pwh}	High CK Pulse Width	4.75	ns
t_{pwl}	RB Pulse Width (low)	6.25	ns
t_{pwl}	Low CK Pulse Width	4.25	ns
rt	RB Recovery Time	1.25	ns

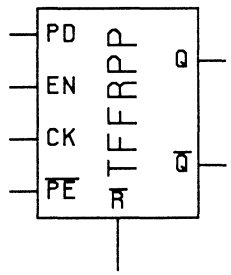
Timing requirements



Functional diagram: TFFRPF

Toggle Enable Flip–Flop with Reset and Synchronous Parallel Load

TFFRPP is a positive edge triggered toggle flip–flop with active low reset and active high toggle enable. Parallel data (PD) is loaded into the flip–flop synchronous to the rising edge of CK when PEB is low.



Inputs: PEB, PD, CK, EN, RB
Outputs: Q, QB
Input Cap.: PEB: 0.057
PD, CK: 0.055
EN: 0.054
RB: 0.055 pF
Cell Size: 41 grids wide, 12 grids high

FUNCTION TABLE

CK	RB	EN	PEB	PD	Q	QB
X	L	X	X	X	L	H
↑	H	X	L	L	L	H
↑	H	X	L	H	H	L
↑	H	H	H	X	QB_o	Q_o
X	H	L	H	X	Q_o	QB_o

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	3.49	6.45	6.73	7.55	3.24+1.67*C_L ns
t_{PHL}		2.96	5.47	5.70	6.40	2.72+1.62*C_L ns
t_{PLH}	CK TO QB	2.12	3.92	4.08	4.58	1.86+1.74*C_L ns
t_{PHL}		2.68	4.95	5.16	5.79	2.39+1.96*C_L ns
t_{PHL}	RB TO Q	3.26	6.03	6.28	7.05	3.02+1.61*C_L ns
t_{PLH}	RB TO QB	2.49	4.60	4.79	5.37	2.23+1.72*C_L ns
t_r	CK TO Q	1.08	1.99	2.07	2.33	0.543+3.56*C_L ns
t_f		0.966	1.78	1.86	2.09	0.520+2.97*C_L ns
t_r	CK TO QB	1.10	2.03	2.12	2.38	0.564+3.57*C_L ns
t_f		1.50	2.77	2.89	3.24	1.05+3.01*C_L ns
t_f	RB TO Q	0.916	1.69	1.76	1.98	0.466+3.00*C_L ns
t_r	RB TO QB	1.13	2.09	2.18	2.44	0.600+3.53*C_L ns

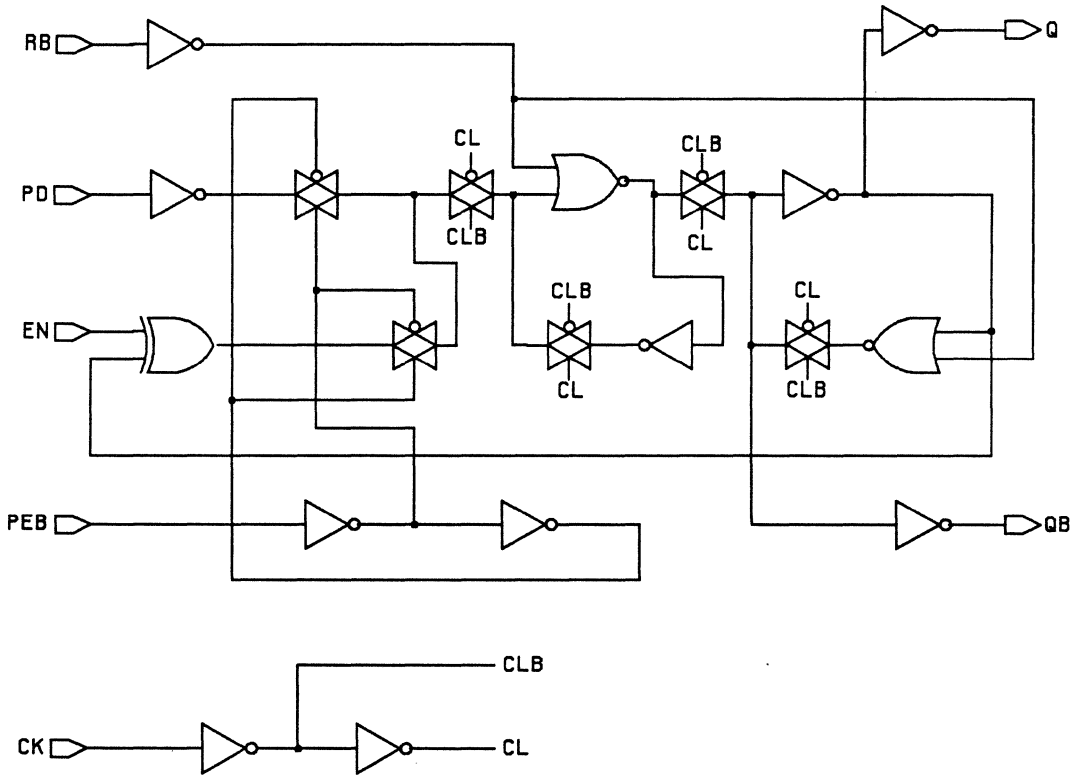
Switching characteristics

TFFRPP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time PEB to CK	4.00	ns
t_{su}	Setup Time PD to CK	3.50	ns
t_{su}	Setup Time EN to CK	6.50	ns
t_h	Hold Time CK to PEB	-3.25	ns
t_h	Hold Time CK to PD	-2.25	ns
t_h	Hold Time CK to EN	-4.25	ns
t_{pwh}	High CK Pulse Width	5.75	ns
t_{pwl}	Low CK Pulse Width	5.50	ns
t_{pwl}	RB Pulse Width (low)	4.75	ns
rt	RB Recovery Time	0.75	ns

Timing requirements



Functional diagram: TFFRPP

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