



MOS BRIEF 6

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ARITHMETIC FUNCTIONS USING MOS REGISTERS

An increasing number of desk calculators (and related equipment) are using MOS shift registers for data storage or memory. In most cases the earlier equipment used delay lines for this function. In the transition, it was a natural tendency to use a configuration similar to that used with delay lines. This was reinforced by the penalty of MOS-bipolar interfacing with the earliest MOS registers.

The use of "100" material by National has produced directly compatible MOS/TTL registers. Now the MM415/515 has a structure that utilizes the freedom of the MOS register with the direct bipolar compatibility to simplify the hardware necessary for arithmetic operations.

MM415/MM515 CONFIGURATION

The MM515 is a triple 64 bit MOS shift register. Each of the three registers has independent control over recirculating data or loading from an external source. In addition to the normal 64 bit output, an early 60 bit output is available for each register. While other functional uses are the primary objective, a number of delay line lengths may be made with the device by connecting the 60 or 64 bit sections in series. The pin diagram of Figure 1 illustrates the ease of interconnection, particularly for a 192 bit delay line. (Input to Pin 1, Pin 3 to Pin 4, Pin 6 to Pin 7, Pins 2, 4, and 9 to GND, Output on Pin 10.)

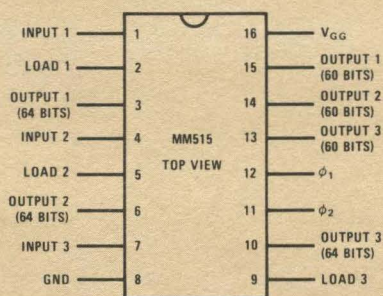


FIGURE 1. 16 Pin DIP

The primary usage of the device is as working registers in a digit and bit serial format of 16, 4 bit, coded numbers. The three registers are sufficient for the basic arithmetic operations. As an example, one contains the multiplier, one the

multiplicand, and the other receives the product. Normally these registers will recirculate with no data change. However during the execution of certain steps of an arithmetic algorithm the data will be loaded under a control command. The input may be a digit from the keyboard, the contents of another register, cleared (or zeroed) data, or the output of an adder. Figure 2 is an example

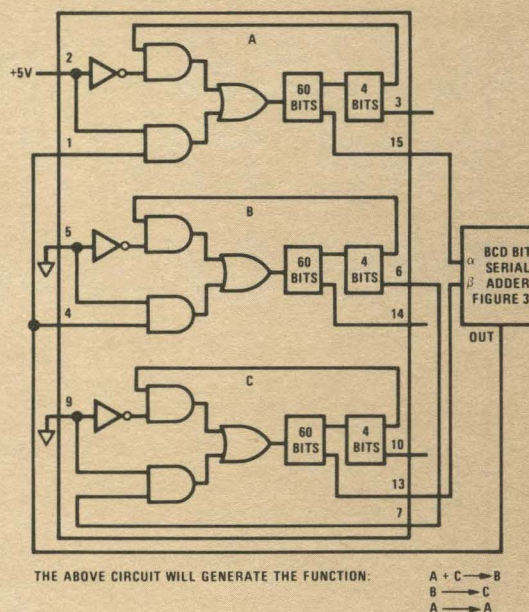


Figure 2. Typical Arithmetic Configuration

showing some of these modes of operation. The three registers are labeled A, B, and C. The data input to A and B is connected to the output of the adder. The load control input to register 1 (Pin 2) is at a logic "0" while the load control for register B (Pin 5) is at a logic "1". This forces the A register to recirculate while the B register is loaded with the output of the adder. With a logic "1" on the load control for C (Pin 9) and the output of B (Pin 6) to the input of C (Pin 7) data would be transferred from the B register to the C register. With these connections and control levels the following data movement occurs during the time the controls are active. A register is recirculated through its internal feedback path. The B register is transferred to the C. The sum of the A and the C registers will be placed in the B.

Special emphasis should be placed on the outputs used for the adder from the A and C registers. To best understand the need for the data out of the 60 bit top, examine Figure 3. In performing coded decimal arithmetic operations, a correction is necessary in addition if the result is greater than 9, or in subtraction, if a borrow is not generated. When a bit serial configuration is used it is necessary to wait until the last bit (T_4) is available before it is known whether correction is needed. One of the simpler methods of handling this is to store the result in a four bit shift register, as shown in Figure 3. During the final bit time of the digit

of the data and it must be right shifted to get it back in "sync" with the remainder of the data. This complicates the timing and control circuitry in addition to taking some time in a synchronous common clock system.

By taking the output from the 60 bit taps, the data is available 4 bits earlier. If the selection of this data is accomplished at the proper time, the output of the adder/subtractor is correct in time to be inserted back into the result register. Referring to Figure 2, the 60 bit output of the A and C registers (Pins 15 and 13) are used for the inputs to the adder.

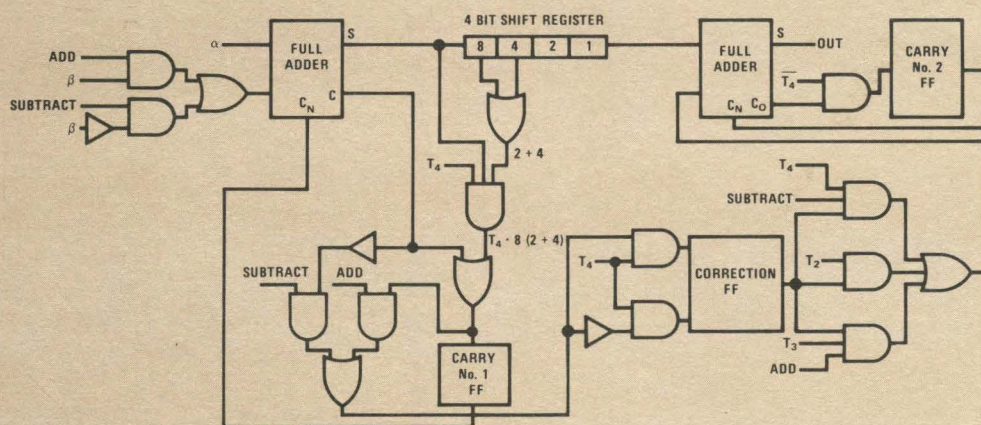


FIGURE 3. Bit Serial Adder/Subtractor

(T_4), the digit is examined for potential correction. If this is required, the correction FF is set and during the next four bit times the proper value is added to the result of this operation so that the output is available four bit times after it went into the adder/subtractor.

If a normal register/adder configuration is used, the result of the addition (or subtraction) is delayed by four bits. This amounts to a left shift

Figure 4 provides a more general configuration for the arithmetic operation. Signals g and h select the second source of data for the adder/subtractor. Addition/subtraction is selected by signal i. These signals must be activated four bit times before the other control signals (a - f) that control data flow.

Write for more information on National's MOS line of shift registers, ROM's, gates, drivers, interface circuits and analog switches.

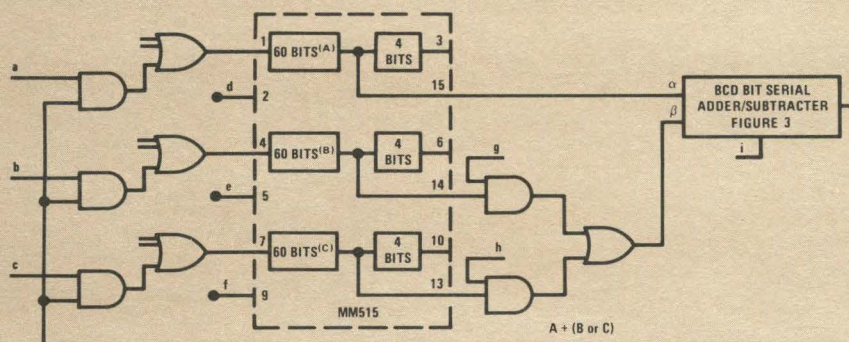


FIGURE 4. BCD Arithmetic Functions Using the MM515 for Register Storage.

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