MOSTEK®

MD SERIES™ MICROCOMPUTER MODULES

Operations Manual

Z80 CENTRAL PROCESSOR MODULE MDX-CPU1, MDX-CPU1A

MOSTEK MDX-CPU1/MDX-CPU1A OPERATIONS MANUAL

MK77850

MK77850-4

MK77855

MK77855-4

Publication Number MK79612

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

SECTION 1

GENERAL INFORMATION

1.1 GENERAL DESCRIPTION

The Mostek MDX-CPU1, shown in Figure 1-1, is the heart of an MD Series Z8Ø system. Based on the powerful Z8Ø microprocessor, the MDX-CPU1 can be used with great versatility in an OEM microcomputer system application. This is done simply by inserting EPROM memories into the sockets provided on the board and configuring them virtually anywhere within the Z8Ø memory map.

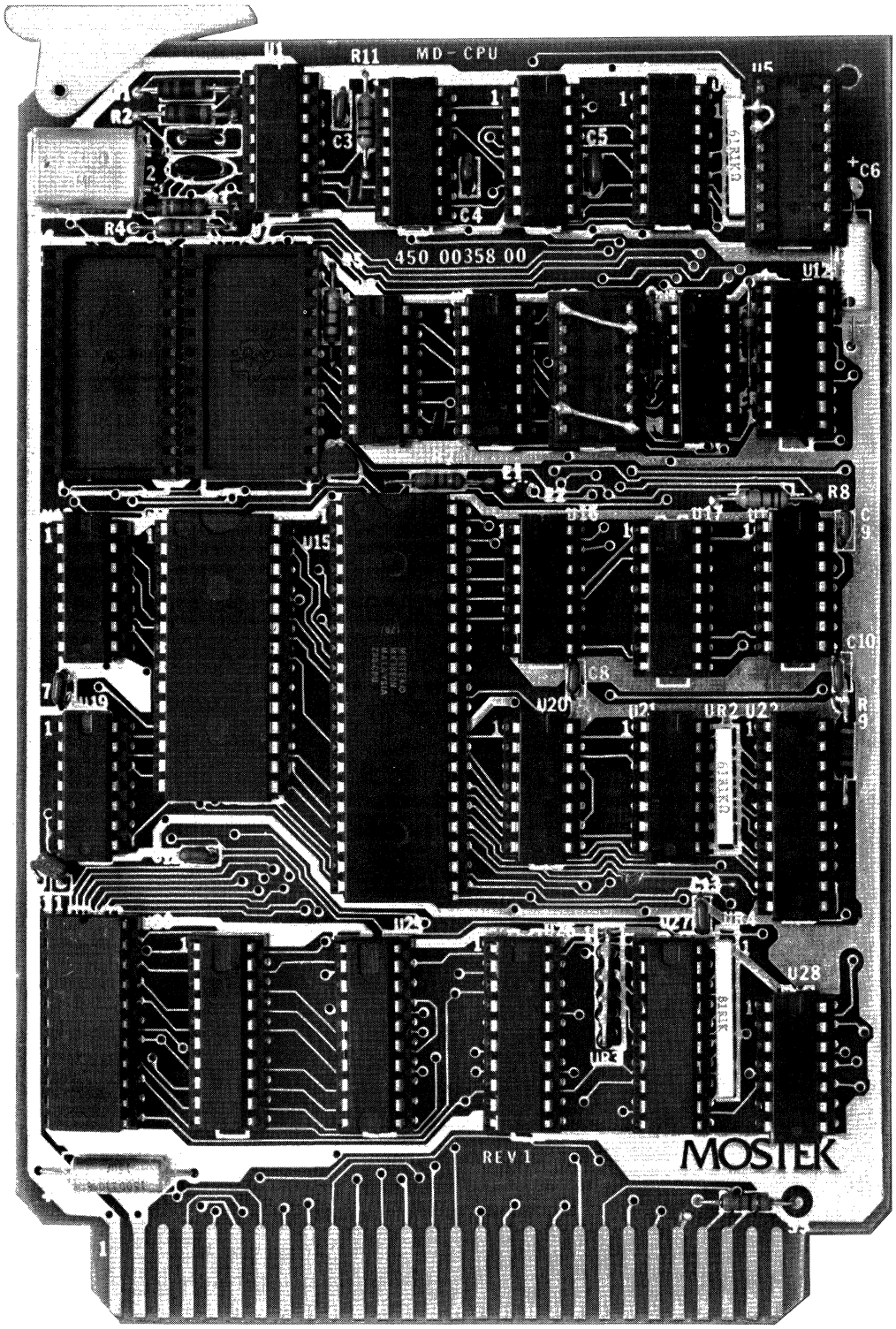
256 bytes of scratchpad RAM are provided on the board and 4K of EPROM can be user provided (2 2716's). In addition, an MK3882 Counter Timer Circuit is included on the MDX-CPU1 to provide counting and timing functions for the Z8Ø. Either 2716 memory maps via a jumper arrangement.

The MDX-CPU1 can be used in conjunction with the MDX-DEBUG and MDX-DRAM modules to utilize DDT-8Ø and ASMB-8Ø in system development.

The MDX-CPU1 is also available in a 4MHz version (MDX-CPU1-4). In this version, one wait state is automatically inserted each time on-board memory is accessed by a read or write cycle. This is necessary to make the access times of the 2716 PROMs and the 3539 scratchpad RAM compatible with the MK3880-4 4MHz Z8Ø-CPU.

There is also a version of this board, CPU1A, which is targeted for the industrial control area. The CPU1A allows system reset to be generated off the board i.e. from the MDX-PFD. CPU1 doesn't incorporate this feature. Due to this difference, the user must be aware of the "one-way" compatibility of these two products. A CPU1A will work in any application in which a CPU1 has been used but the opposite is not the case.

FIGURE 1-1 MDX-CPU1 BOARD



STD-Z8Ø BUS PIN-OUT AND DESCRIPTION

BUS PIN	MNEMONIC	DESCRIPTION
1	+5V	+5Vdc system power
2	+5V	+5Vdc system power
3	GND	Ground - System signal ground and dc return
4	GND	Ground - System signal ground and dc return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	
8	D7	
9	D2	Data Bus (Tri-state, input/output active high).
1Ø	D6	$D_Ø$-D_7 constitute an 8-bit bidirectional data bus.
11	D1	The data bus is used for data exchange with memory and
12	D5	I/O devices.
13	DØ	
14	D4	
15	A7	
16	A15	
17	A6	
18	A14	
19	A5	
2Ø	A13	Address bus (Tri-state, output, active high).
		$A_Ø$-A_{15}

BUS PIN	MNEMONIC	DESCRIPTION
21	A4	make up a 16-bit address bus. The address bus provides the address for memory (up to 65K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. $A_{Ø}$ is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
22	A12	
23	A3	
24	A11	
25	A2	
26	A1Ø	
27	A1	
28	A9	
29	AØ	
3Ø	A8	
31	$\overline{WR}$	Memory Write (Tri-state, output, active low). $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	$\overline{RD}$	Memory Read (Tri-state, output active low). $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device/memory should use this signal to gate data onto the CPU data bus.
33	$\overline{IORQ}$	Input/Output Request (Tri-state, output, active low). The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An $\overline{IORQ}$ signal is also generated with an $\overline{M1}$ signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during $\overline{M1}$ time, while I/O operations never occur during $\overline{M1}$ time.

BUS PIN	MNEMONIC	DESCRIPTION
34	$\overline{\text{MEMRQ}}$	Memory Request (Tri-State, output, active low). The $\overline{\text{MEMRQ}}$ signal indicates that the address bus holds a valid address for a memory read or memory write operation.
35	$\overline{\text{IOEXP}}$	I/O expansion, not used on Mostek MDX cards.
36	$\overline{\text{MEMEX}}$	Memory expansion, not used on all Mostek MDX cards.
37	$\overline{\text{REFRESH}}$	$\overline{\text{REFRESH}}$ (Tri-state, output, active low). $\overline{\text{REFRESH}}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the $\overline{\text{MEMRQ}}$ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle, A7 is a logic zero and the upper 8 bits of the address bus contain the I register.
38	$\overline{\text{DEBUG}}$	$\overline{\text{DEBUG}}$ (Input) used in conjunction with the DDT-8Ø operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the $\overline{\text{DEBUG}}$ line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	$\overline{\text{M1}}$	Machine Cycle One (Tri-state, output, active low). $\overline{\text{M1}}$ indicates that the current machine cycle is in the op-code fetch cycle of an instruction. Note that during the execution of 2-byte op-codes, $\overline{\text{M1}}$ will be generated as each op-code is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. $\overline{\text{M1}}$ also occurs with $\overline{\text{IORQ}}$ to indicate an interrupt-acknowledge cycle.

BUS PIN	MNEMONIC	DESCRIPTION
40	Status Ø	Not used on Mostek MDX cards.
41	$\overline{\text{BUSAK}}$	Bus Acknowledge (Output, active low). Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high-impedance state and the external device can now control the bus.
42	$\overline{\text{BUSRQ}}$	Bus Request (Input, active low). The $\overline{\text{BUSRQ}}$ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high-impedance state so that other devices can control those buses. When $\overline{\text{BUSRQ}}$ is activated, the CPU will set these buses to a high-impedance state as soon as the current CPU machine cycle is terminated and the Bus Acknowledge ($\overline{\text{BUSAK}}$) signal is activated.
43	$\overline{\text{INTAK}}$	Interrupt Acknowledge (Tri-state, output, active low). The $\overline{\text{INTAK}}$ signal indicates that an interrupt acknowledge cycle is in progress, and the interrupt device should place its response vector on the data bus.
44	$\overline{\text{INTRQ}}$	Interrupt Request (Input, active low). The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software-controlled interrupt-enable flip-flop (IFF) is enabled and if the $\overline{\text{BUSRQ}}$ signal is not active. When the CPU accepts the interrupt, an acknowledge signal ($\overline{\text{IORQ}}$ during an $\overline{\text{M1}}$) is sent out at the beginning of the next instruction cycle.

BUS PIN	MNEMONIC	DESCRIPTION
45	$\overline{\text{WAITRQ}}$	WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.
46	$\overline{\text{NMIRQ}}$	Non-Maskable Interrupt Request (Input, negative-edge triggered). The non-maskable interrupt request line has a higher priority than $\overline{\text{INTRQ}}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt-enable flip-flop. $\overline{\text{NMIRQ}}$ automatically forces the CPU to restart to location 0066_H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a $\overline{\text{BUSRQ}}$ will override a $\overline{\text{NMIRQ}}$.
47	$\overline{\text{SYSRESET}}$	System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. A system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00_H, set the R register to 00_H, and set Interrupt Mode 0.

BUS PIN	MNEMONIC	DESCRIPTION
48	$\overline{\text{PBRESET}}$	Push Button Reset (Input, active low). The push button reset will generate a debounced system reset.
49	$\overline{\text{CLOCK}}$	Processor Clock (Output, active low). Single phase system clock.
5Ø	$\overline{\text{CNTRL}}$	Auxiliary Timing
51	PCO	Priority Chain Output (Output, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt-driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt-driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	+12V	-12Vdc system power

SECTION 2

FUNCTIONAL DESCRIPTION

2.1 INTRODUCTION

The MDX-CPU1 is designed around the powerful Z8Ø CPU (MK388Ø) chip. The Z8Ø, with its 158 instructions, single-phase clock input, automatic dynamic memory refresh, advanced set of addressing modes and interrupt structure, is one of the most so-sophisticated microprocessors available today.

The major functions of the MDX-CPU1 are shown in Figure 2-1 and will be explained below:

2.2 CPU

Z8Ø (MK388Ø) generates the address and control signals, communicates with memory, I/O and peripherals, fetches and executes instructions, and provides most of the timing signals for proper operation of the system.

2.3 COUNTER/TIMER CIRCUIT (CTC)

Provides a four-channel counter/timer function under software control.

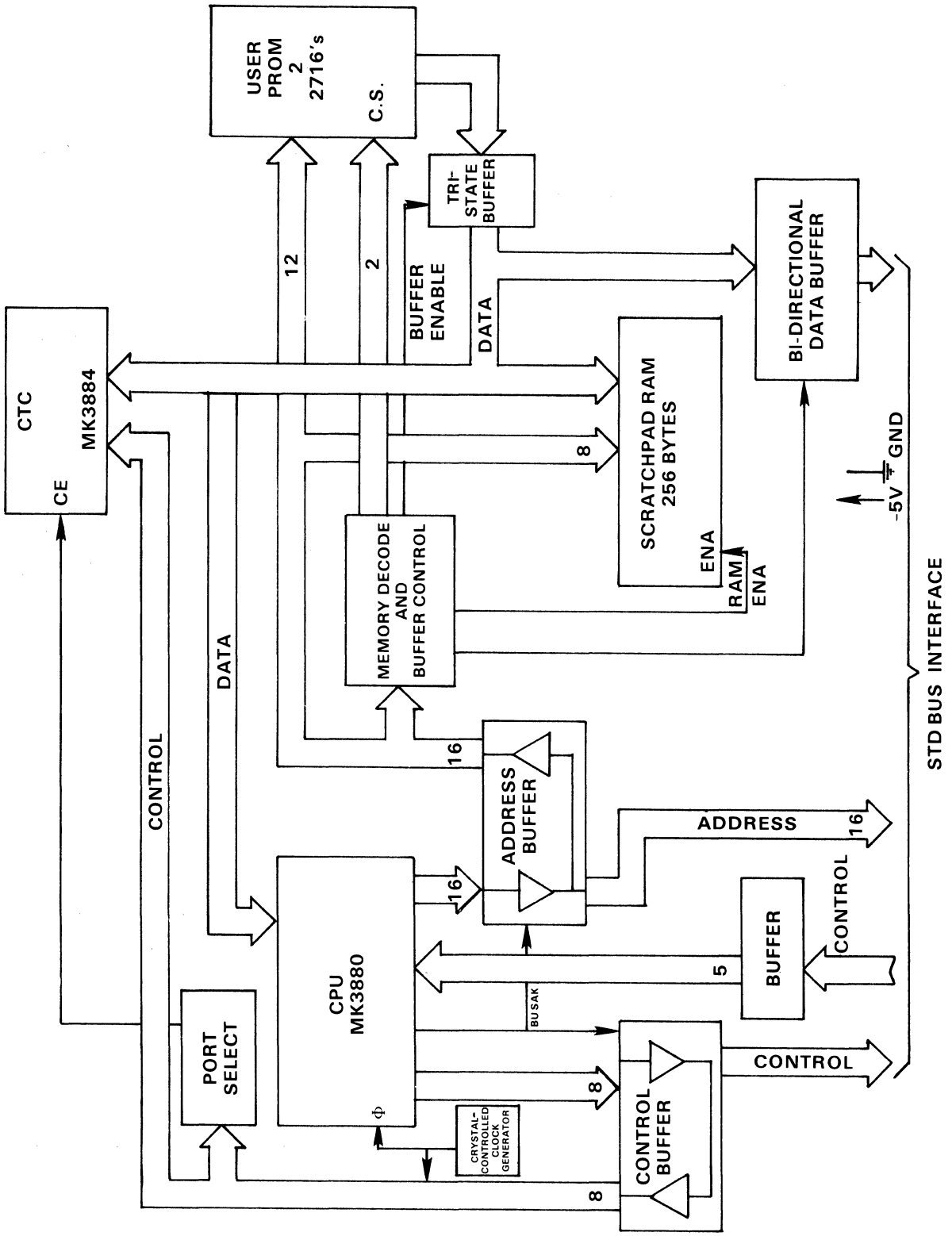
2.4 EPROM

Two 24-pin sockets are provided for use with 2716 EPROMs (+5V only) for an EPROM memory capacity of 4K X 8. This 4K x 8 of EPROM is strappable on any 2K boundary within any 16K block.

2.5 RAM

A 256 x 8 static RAM is provided for general-purpose storage and stack pointer operations. The 256 x 8 RAM is located at FFØØ to FFFF.

FIGURE 2-1 BLOCK DIAGRAM



2.6 CLOCK GENERATOR

The MDX-CPU1 comes with a crystal-controlled clock generator. This clock drives all the necessary components on the board, and is buffered to drive off the board to other system peripherals. The crystal frequency for the standard MDX-CPU1 card is 5.ØMHz and is divided by two to yield a 2.5MHz clock. The MDX-CPU1-4 is the same except that the crystal frequency is 8.ØMHz, divided to 4.Ø MHZ.

2.7 RESET/RESTART

The MDX-CPU1 can be strapped so that after reset execution begins at either $ØØØØ_H$ or $EØØØ_H$. This logic is required for use of standard Mostek hardware and software products including DDT-8Ø, FLP-8ØDOS/, MDX-SST, and MDX-DEBUG.

2.8 BUS LINES - (DATA, ADDRESS, CONTROL)

All lines going onto or off of the board are TTL-buffered and/or terminated. The data bus lines are bidirectional so that data can go in two directions. The direction of the data bus buffer is controlled by the CPU, so that the data bus buffer will always be enabled out when the CPU is accessing on-board memory or the CTC. The data bus buffer will be enabled pointing onto the CPU card when an off-board memory, I/O, or interrupt vector is addressed. The data bus buffer will go to a high impedance whenever a bus-acknowledge signal is issued from the CPU. The address and control lines are unidirectional buffers and will go to a high-impedance level whenever a busacknowledge signal is issued by the CPU.

2.9 WAIT-STATE GENERATOR

This function, if selected, causes on-board memory read and write cycles or I/O cycles to be lengthened by one clock period in order to allow sufficient access time when slow memory or I/O devices are utilized.

SECTION 3

UTILIZATION

3.1 INTRODUCTION

This section will describe the various jumper options for the MDX-CPU1 board.

3.2 MEMORY INTERFACE

The MDX-CPU1 can be populated with up to 4K x 8 of EPROM (two 2716s). It comes with a 256 x 8 static RAM that is decoded at FFØØH to $FFFF_H$.

Memory Decoding Jumpers

Decoding for each of the EPROMs is shown in Table 3-1. The 256 x 8 static RAM may be disabled by disconnecting U5 Pin 2 from U5 Pin 3.

3.3 I/O PORTS

Counter/Timer I/O Ports. The CTC I/O ports are hardwired to respond to I/O Ports $7C_H$, $7D_H$, $7E_H$, and $7F_H$ as shown in Table 3-2. For detailed information on how to program the CTC, refer to the Mostek CTC Technical Manual.

TABLE 3-1

EPROM ADDRESS SELECTION

DECODED ADDRESS	U5 JUMPERS		U1Ø JUMPERS
	EPROM U6	EPROM U7	
Ø-7FF	U5 Pin 5 to Pin 9	U5 Pin 4 to Pin 9	
8ØØ-FFF	" 1Ø	" 1Ø	
1ØØØ-17FF	" 11	" 11	
18ØØ-1FFF	" 12	" 12	Pin 2 to Pin 12
			and
2ØØØ-27FF	" 13	" 13	Pin 5 to Pin 9
28ØØ-2FFF	" 14	" 14	
3ØØØ-37FF	" 15	" 15	
38ØØ-3FFF	" 16	" 16	
4ØØØ-47FF	" 9	" 9	
48ØØ-4FFF	" 1Ø	" 1Ø	
5ØØØ-57FF	" 11	" 11	
58ØØ-5FFF	" 12	" 12	Pin 9 to Pin 1Ø
			and
6ØØØ-67FF	" 13	" 13	Pin 2 to Pin 12
68ØØ-6FFF	" 14	" 14	
7ØØØ-77FF	" 15	" 15	
78ØØ-7FFF	" 16	" 16	
8ØØØ-87FF	" 9	" 9	
88ØØ-8FFF	" 1Ø	" 1Ø	
9ØØØ-97FF	" 11	" 11	
98ØØ-9FFF	Pin 5 to Pin 12	Pin 4 to Pin 12	Pin 5 to Pin 9
			and
AØØØ-A7FF	" 13	" 13	Pin 2 to Pin 3
A8ØØ-AFFF	" 14	" 14	
BØØØ-B7FF	" 15	" 15	
B8ØØ-BFFF	" 16	" 16	
CØØØ-C7FF	" 9	" 9	
C8ØØ-CFFF	" 1Ø	" 1Ø	
DØØØ-D7FF	" 11	" 11	Pin 9 to Pin 1Ø
			and
D8ØØ-DFFF	" 12	" 12	Pin 2 to Pin 3

E000-E7FF	"	13	"	13	
E800-EFFF	"	14	"	14	
F000-F7FF	"	15	"	15	
F800-FFFF	"	16	"	16	

*EPROMS ARE SHIPPED UNSTRAPPED.

TABLE 3-2

I/O PORT NO. VS. CTC CHANNEL NO.

I/O PORT	CTC CHANNEL
$7C_H$	Ø
$7D_H$	1
$7E_H$	2
$7F_H$	3

3.4 RESET/RESTART JUMPERS

The MDX-CPU1 has the capability to reset and begin execution at location $ØØØØ_H$ or $EØØØ_H$. Table 3-3 shows the jumpers for selecting $ØØØØ_H$ and $EØØØ_H$. The reason for selecting a reset to $EØØØ_H$ was primarily to allow the use of Mostek's DDT-8Ø (Designers Development Tool) operating system. However, if DDT-8Ø is not used, then the reset to $EØØØ_H$ can be used for user programs. The jump to $EØØØ_H$ is implemented in hardware and must be reset after it is activated. To reset the jump circuitry the following code must be placed at $EØØØ_H$:

$EØØØ_H$ C3 Ø3 EØ

$EØØ3_H$ DB FF (Any I/O Operation will reset the address modification latch)

$EØØ5_H$ (User program begins)

When using DDT-8Ø, it is not necessary to execute this code since it is already in the ROM.

TABLE 3-3

RESTART JUMPERS

RESET TO:	CONNECT:
$ØØØØ_H$	U1Ø PIN 6 TO 7
$EØØØ_H$	U1Ø PIN 6 to 8

3.5 WAIT-STATE GENERATOR

The Wait-State circuitry was added to allow 4 MHz operation with standard memory and standard I/O devices. When the Wait-State circuit is enabled as shown in Table 3-4, one wait state is inserted in the current timing sequence, either memory access or I/O operation. Refer to the CPU (MK3880) section of the manual for Wait-State timing. The Wait-State circuitry is normally not enabled for 2.5 MHz operation.

TABLE 3-4

WAIT-STATE JUMPERS

OPERATION	WAIT STATE	
MEMORY ACCESS	DISABLED	OPEN U10 Pin 13 to 14 E3 to E4
MEMORY ACCESS	ENABLED	CONNECT U10 Pin 13 to 14 E3 to E4
I/O	DISABLED	OPEN U10 Pin 13 to 14 E5 to E6
I/O	ENABLED	CONNECT U10 Pin 13 to 14 E5 to E6

3-6 Jumper Pins, labeled E7 Pins 1-4, have been provided to allow the Memory Expansion and I/O Expansion Lines to be tied to ground. This option can be implemented by jumpering these pins as shown in Table 3-5.

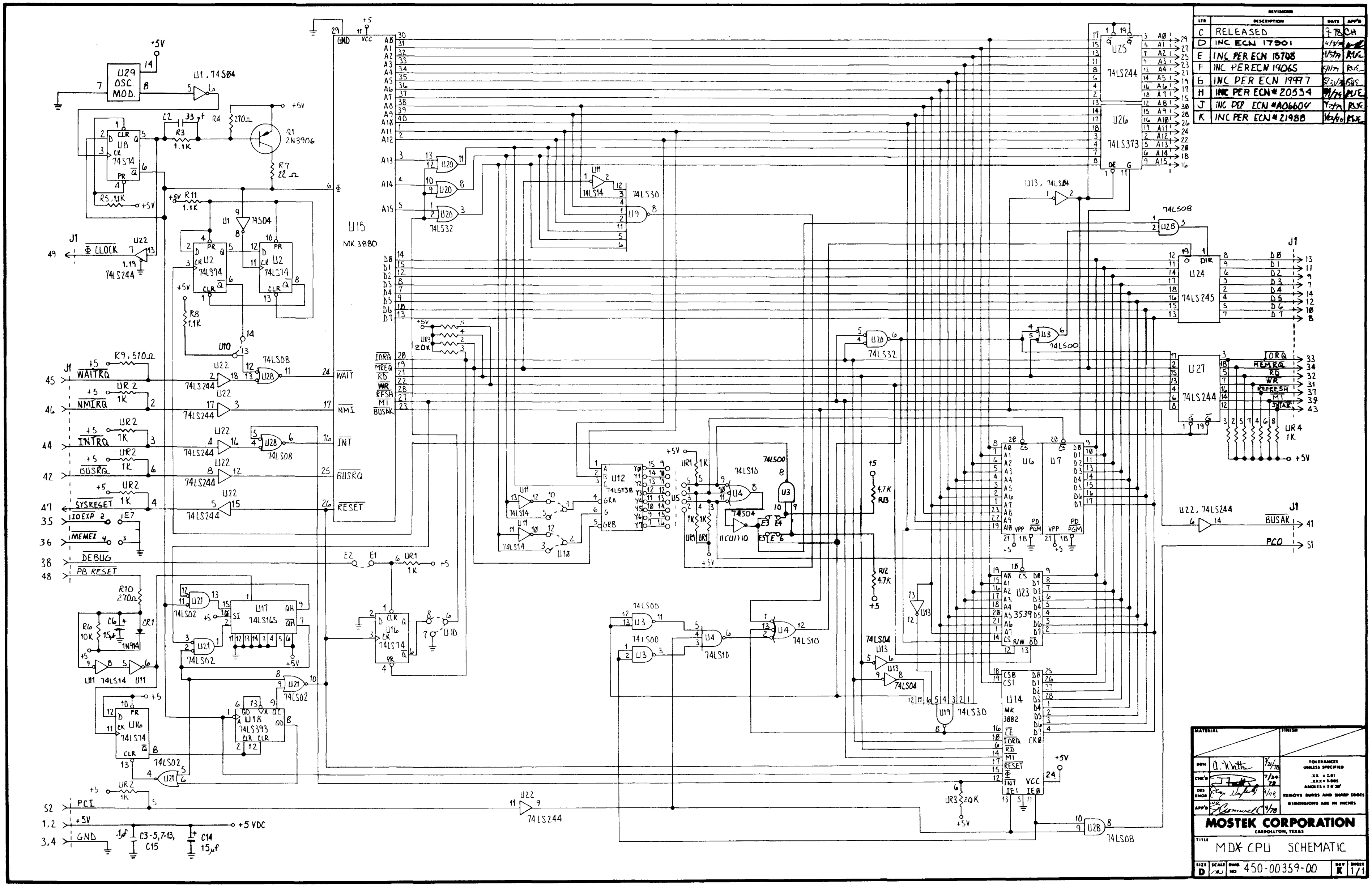
TABLE 3-5

MEMEX and IOEXP JUMPERS

Memory Expansion ($\overline{\text{MEMEX}}$)	I/Ø Expansion ($\overline{\text{I/O EXP}}$)
Connect E7 Pin 3 to Pin 4	Connect E7 Pin 1 to Pin 2

APPENDIX A

SCHEMATIC

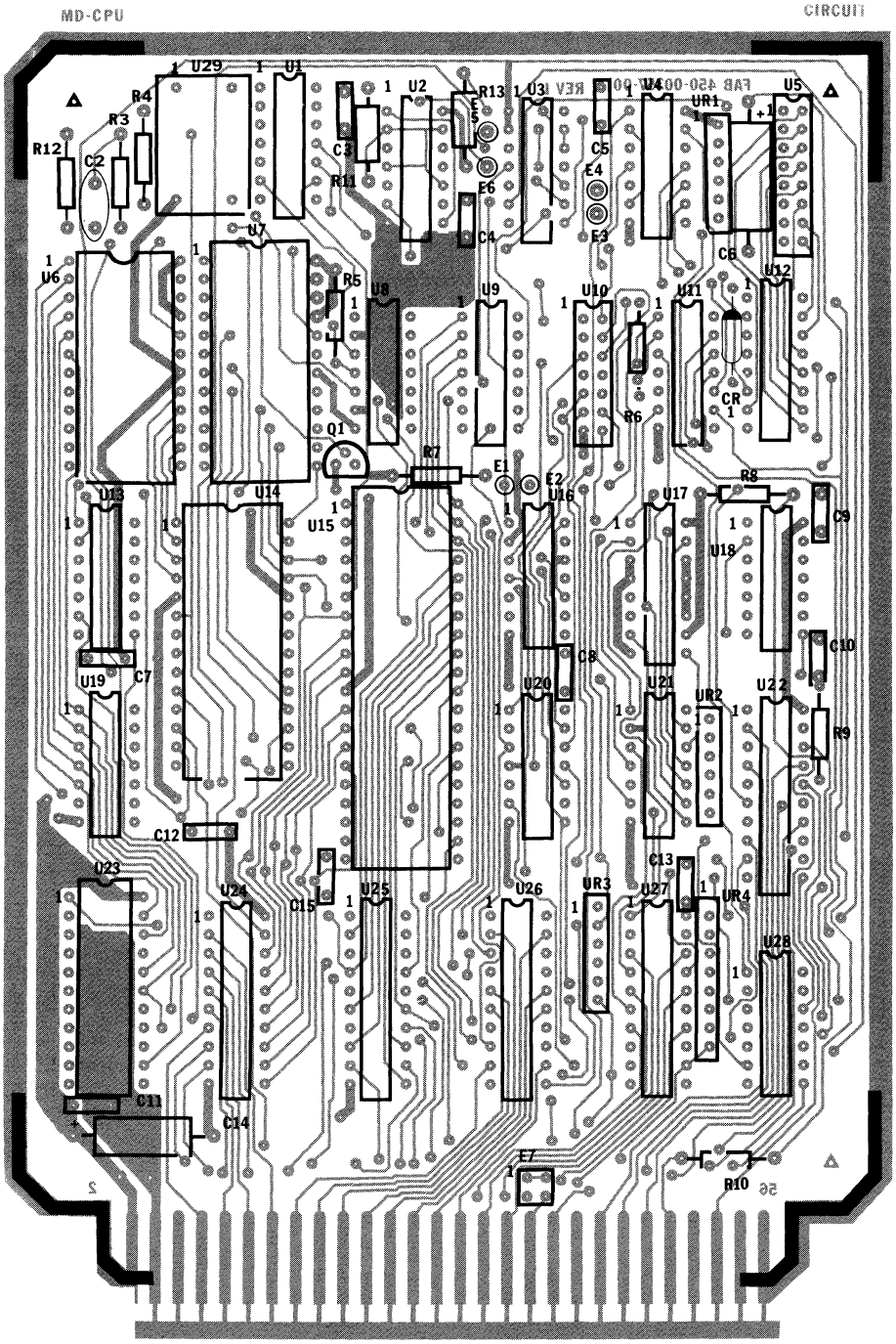

REVISIONS
LTR DESCRIPTION DATE APP'D
C RELEASED
D INC ECN 17901
E INC PER ECN 18708
F INC PER ECN 19065
G INC PER ECN 19997
H INC PER ECN # 20534
J INC PER ECN #A06604
K INC PER ECN # 21988
U15 MK 3880
U29 OSC. MOD.
U8 74S74
U2 74LS74
Q1 2N3906
U25 74LS244
U26 74LS373
U24 74LS245
U27 74LS244
U12 74LS138
U6
U7
U23 3539
U14 MK 3882
U17 74LS165
U18 74LS393
U16 74LS74
J1
Φ CLOCK
WAITRQ
NMIRQ
INTRQ
BUSRQ
SYSRESET
IOEXP
MEMEX
DEBUG
PB RESET
PCI
PCO
BUSAK
+5V
GND
+5 VDC
MATERIAL
FINISH
DRN
CHK'D
DES ENGR
APP'D
TOLERANCES UNLESS SPECIFIED
.XX ± .01
.XXX ± .005
ANGLES ± 0°30'
REMOVE BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES
MOSTEK CORPORATION
CARROLLTON, TEXAS
TITLE
MDX CPU SCHEMATIC
SIZE D
SCALE
DWG NO 450-00359-00
REV K
SHEET 1/1

APPENDIX B

PARTS PLACEMENT DIAGRAM

PARTS LIST

PARTS PLACEMENT DIAGRAM



PARTS LIST

P/N	QTY.	DESCRIPTION	ITEM NO.	DRAWING NO.
000000			AA:NOTE FOLLOWING PARTS USED	77850
000000			AB:WITH 2.5 MHZ MDX-CPU1	77850
4610110	1	FAB 450-00357-00 REV L	AC:	77850
0000000		ASSY 450-00358-10 REVL	AD:	77850
0000000		SCH 450-00359-00 REVL	AE:	77850
4150086	1	CAPACITOR 33PF	C2	77850
4150111	11	CAPACITOR .1UF	C3-5,7-13,15	77850
4150140	2	CAPACITOR 15UF	C6,14	77850
4480026	1	DIODE 1N914	CR1	77850
4210383	6	HEADER PIN	E1-6	77850
4210238	1	HEADER 4 PIN	E7	77850
4480011	1	TRANSISTOR 2N3906	Q1	77850
4470089	2	RESISTOR 4.7 K OHMS	R12,13	77850
4470074	4	RESISTOR 1.1K	R3,5,8,11	77850
4470059	2	RESISTOR 270 OHMS	R4,10	77850
4470097	1	RESISTOR 10K	R6	77850
4470033	1	RESISTOR 22 OHMS	R7	77850
4470066	1	RESISTOR 510 OHMS	R9	77850
4313285	1	IC 74S04	U1	77850
4313291	1	IC 74LS14	U11	77850
4313296	1	IC 74LS138	U12	77850
4313288	1	IC 74LS04	U13	77850
4313259	1	IC MK3882	U14	77850
4313271	1	IC MK3880	U15	77850
4313555	1	IC 74LS165	U17	77850
4313335	1	IC 74LS393	U18	77850
4313413	2	IC 74LS74	U2,16	77850
4313411	1	IC 74LS32	U20	77850
4313300	1	IC 74LS02	U21	77850
4313507	3	IC 74LS244	U22,25,27	77850
4313258	1	IC 35392	U23	77850
4313508	1	IC 74LS245	U24	77850
4313544	1	IC 74LS373	U26	77850
4313289	1	IC 74LS08	U28	77850
4230019	1	OSCILLATOR MOD. 5 MHZ	U29	77850
4313287	1	IC 74LS00	U3	77850
4313301	1	IC 74LS10	U4	77850
4210143	2	HEADER 16 PIN	U5,10	77850
4313266	1	IC 74S74	U8	77850
4313410	2	IC 74LS30	U9,19	77850
4470178	2	RESISTOR SIP 6PIN 1K	UR1,UR2	77850
4470299	1	RESISTOR SIP 6 PIN 22K	UR3	77850
4470179	1	RESISTOR SIP 8 PIN 1K	UR4	77850
4620038	1	SOCKET 28 PIN	X14	77850
4620019	1	SOCKET 40 PIN	X15	77850
4620037	1	SOCKET 22 PIN	X23	77850
4620018	2	SOCKET 24 PIN	X6,X7	77850
4280155	1	EJECTOR	Z	77850
5013004	2	BAG ANTISTATIC	Z:NOTE SHIPPED NOT ASSEMBLED	77850
5013204	1	BOX SHIPPING	Z:NOTE SHIPPED NOT ASSEMBLED	77850
5025266	1	TRAVELER WIP	Z:NOTE, IN HOUSE ONLY	77850
MK79815	1	FACTORY NOTICES	Z:SHIPPED NOT ASSEMBLED	77850
MK79728	1	WARRANTY REGISTRATION	Z:SHIPPED NOT ASSEMBLED	77850
MK79612	1	MDX-CPU1 OPS. MANUAL	Z:SHIPPED NOT ASSEMBLED	77850

PARTS LIST

P/N	QTY.	DESCRIPTION	ITEM NO.	DRAWING NO.
0000000			AA:NOTE:FOLLOWING PARTS USED	778504
0000000			AB:WITH 4 MHZ MDX-CPU1	778504
4610110	1	FAB 450-00357-00 REV L	AC:	778504
0000000		ASSY 450-00358-11 REVL	AD:	778504
0000000		SCH 450-00359-00 REV L	AE:	778504
4150086	1	CAPACITOR 33PF	C2	778504
4150111	11	CAPACITOR .1UF	C3-5,7-13,15	778504
4150140	2	CAPACITOR 15UF	C6,14	778504
4480026	1	DIODE 1N914	CR1	778504
4210383	6	HEADER PIN	E1-6	778504
4210238	1	HEADER 4 PIN	E7	778504
4480011	1	TRANSISTOR 2N3906	Q1	778504
4470089	2	RESISTOR 4.7 K OHMS	R12,13	778504
4470074	4	RESISTOR 1.1K	R3,5,8,11	778504
4470059	2	RESISTOR 270 OHMS	R4,10	778504
4470097	1	RESISTOR 10K	R6	778504
4470033	1	RESISTOR 22 OHMS	R7	778504
4470066	1	RESISTOR 510 OHMS	R9	778504
4313285	1	IC 74S04	U1	778504
4313291	1	IC 74LS14	U11	778504
4313296	1	IC 74LS138	U12	778504
4313288	1	IC 74LS04	U13	778504
4313674	1	IC MK3882-4	U14	778504
4313532	1	IC MK3880-4	U15	778504
4313413	1	IC 74LS74	U16	778504
4313555	1	IC 74LS165	U17	778504
4313335	1	IC 74LS393	U18	778504
4313266	2	IC 74S74	U2,8	778504
4313411	1	IC 74LS32	U20	778504
4313300	1	IC 74LS02	U21	778504
4313557	3	IC 74S244	U22,25,27	778504
4313268	1	IC 35392	U23	778504
4313508	1	IC 74LS245	U24	778504
4313538	1	IC 74S373	U26	778504
4313396	1	IC 74S08	U28	778504
4230020	1	OSCILLATOR MOD. 8 MHZ	U29	778504
4313287	1	IC 74LS00	U3	778504
4313301	1	IC 74LS10	U4	778504
4210143	2	HEADER 16 PIN	U5,10	778504
4313410	2	IC 74LS30	U9,19	778504
4470173	2	RESISTOR SIP 6PIN 1K	UR1,UR2	778504
4470299	1	RESISTOR SIP 6 PIN 22K	UR3	778504
4470179	1	RESISTOR SIP 8 PIN 1K	UR4	778504
4620038	1	SOCKET 28 PIN	X14	778504
4620019	1	SOCKET 40 PIN	X15	778504
4620037	1	SOCKET 22 PIN	X23	778504
4620018	2	SOCKET 24 PIN	X6,X7	778504
4280155	1	EJECTOR	Z	778504
5013004	2	BAG ANTISTATIC	Z:NOTE SHIPPED NOT ASSEMBLED	778504
5013204	1	BOX SHIPPING	Z:NOTE SHIPPED NOT ASSEMBLED	778504
5025266	1	TRAVELER WIP	Z:NOTE, IN HOUSE ONLY	778504
MK79815	1	FACTORY NOTICES	Z:SHIPPED NOT ASSEMBLED	778504
MK79728	1	WARRANTY REGISTRATION	Z:SHIPPED NOT ASSEMBLED	778504
MK79612	1	MDX-CPU1 OPS. MANUAL	Z:SHIPPED NOT ASSEMBLED	778504

APPENDIX C

SPECIFICATIONS

SPECIFICATIONS

C.1 ELECTRICAL SPECIFICATIONS

WORD SIZE

Instruction: 8, 16, 24, or 32 bits

Data: 8 bits

CYCLE TIME

Clock period or T state = Ø.4 microsecond @ 2.5 MHz for MDX-CPU1

= Ø.25 microsecond @ 4.Ø MHz for MDX-CPU1-4

Instructions require from 4 to 23 T States

MEMORY ADDRESSING

On-Board EPROM: jumper-selectable for any 2K boundary within a 16K block of Z8Ø memory map.

On-Board RAM: FFØØ-FFFF

MEMORY CAPACITY

On-Board EPROM - 4K bytes (sockets only)

On-Board RAM - 256 bytes

Off-Board Expansion - Up to 65,536 bytes, with user-specified combinations of RAM, ROM, PROM

MEMORY SPEED REQUIRED

MEMORY	ACCESS TIME	CYCLE TIME
2716*	45Ø nS	45Ø nS

*Single 5-Volt type required

I/O ADDRESSING

On-Board Programmable Timer

PORT ADDRESS (HEX)	MK3882 CHANNEL
7C	Ø
7D	1
7E	2
7D	3

I/O CAPACITY

Up to 252 Port addresses can be decoded off-board. (Four port addresses are on-board. 252+4=256 total I/O ports).

INTERRUPTS

Multi-level with three vectoring modes (Modes Ø,1,2). Interrupt requests may originate from user-specified I/O or from the on-board MK3882 CTC.

STD-Z8Ø BUS INTERFACE

Inputs	One 74LS load max
Outputs	I_{OH} = -3 mA min. at 2.4 Volts
	I_{OL} = 24 mA min. at Ø.4 Volts

SYSTEM CLOCK

	MIN.	MAX.
MDX-CPU1	5ØØ kHz	2.5 MHz
MDX-CPU1-4	5ØØ kHz	4.Ø MHz

POWER SUPPLY REQUIREMENTS

5V $\pm$ 5% at 1.1A maximum

OPERATING TEMPERATURE

Ø°C to 6Ø°C

C.2 MECHANICAL SPECIFICATIONS

CARD DIMENSIONS

4.5 in. (11.43cm) high by 6.5Ø in. (16.51 cm) long

Ø.48 in. (1.22cm) maximum profile thickness

Ø.Ø62 in. (Ø.16cm) printed-circuit-board thickness

CONNECTORS

FUNCTION	CONFIGURATION	MATING CONNECTOR
STD BUS	56-pin dual	Printed Circuit. Viking 3VH28/ICE5
	Ø.125-in. centers	Wire Wrap Viking 3VH28/1CND5
		Solder Lug Viking 3VH28/1CN5

STD-Z8Ø BUS ELECTRICAL SPECIFICATIONS

Bus Receivers

Logical Low: Ø.8V max at -Ø.36 A

Logical High: 2.ØV min at 2Ø u A

Bus Drivers

Logical Low: Ø.5V at 24 mA

Logical High: 2.4V at -3 mA

Off-State Output Current (tri-state): ±1ØØ microamperes

Recommended Bus Drivers and Receivers

Bus Drivers - 74LS24Ø, 74LS241, 74LS373, 74LS374, 74LS244

Bus Receivers - 74LS24Ø, 74LS241, 74LS244

Bus Transceivers - 74LS245, 74LS242, 74LS243

NOTES:

(1) Input/Output designations of the STD-Z8Ø BUS are made with respect to the CPU card.

(2) The following signals have pull-up resistors: $\overline{WR}$, $\overline{RD}$, $\overline{IORQ}$, $\overline{MEMRQ}$, $\overline{REFRESH}$, $\overline{DEBUG}$, $\overline{M1}$, $\overline{BUSRQ}$, $\overline{INTAK}$, $\overline{INTRQ}$, $\overline{WAITRQ}$, $\overline{NMIRQ}$, $\overline{SYSRESET}$, $\overline{PBRESET}$, and $\overline{CLOCK}$. The value of the pull-up resistors are 1k Ohm except for $\overline{WAITRQ}$, which is 5ØØ Ohms, and $\overline{PBRESET}$, which is 1Øk Ohm.

MOSTEK®

1215 W. Crosby Rd. • Carrollton, Texas 75006 • 214/323-6000
In Europe, Contact: MOSTEK Brussels
270-272 Avenue de Tervuren (BTE21), B-1150 Brussels, Belgium;
Telephone: 762.18.80

PRINTED IN USA March 1981
Publication No. MK79612